We consider the verification of lock-free data structures that manually manage their memory with the help of a safe memory reclamation (SMR) algorithm. Our first contribution is a type system that checks whether a program properly manages its memory. If the type check succeeds, it is safe to ignore the SMR algorithm and consider the program under garbage collection. Intuitively, our types track the protection of pointers as guaranteed by the SMR algorithm. There are two design decisions. The type system does not track any shape information, which makes it extremely lightweight. Instead, we rely on invariant annotations that postulate a protection by the SMR. To this end, we introduce angels, ghost variables with an angelic semantics. Moreover, the SMR algorithm is not hard-coded but a parameter of the type system definition. To achieve this, we rely on a recent specification language for SMR algorithms. Our second contribution is to automate the type inference and the invariant check. For the type inference, we show a quadratic-time algorithm. For the invariant check, we give a source-to-source translation that links our programs to off-the-shelf verification tools. It compiles away the angelic semantics. This allows us to infer appropriate annotations automatically in a guess-and-check manner. To demonstrate the effectiveness of our type-based verification approach, we check linearizability for various list and set implementations from the literature with both hazard pointers and epoch-based memory reclamation. For many of the examples, this is the first time they are verified automatically. For the ones where there is a competitor, we obtain a speed-up of up to two orders of magnitude.

Conference Version:
Roland Meyer and Sebastian Wolff. 2020. Pointer Life Cycle Types for Lock-Free Data Structures with Memory Reclamation: Extended Version. Proc. ACM Program. Lang. 4, POPL, Article 68 (January 2020). https://doi.org/10.1145/3371136

1 INTRODUCTION
In the last decade we have experienced an upsurge in massive parallelization being available even in commodity hardware. To keep up with this trend, popular programming languages include in their standard libraries features to make parallelization available to everyone. At the heart of this effort are concurrent (thread-safe) data structures. Consequently, efficient implementations are in high demand. In practice, lock-free data structures are particularly efficient.

Unfortunately, lock-free data structures are also particularly hard to get correct. The reason is the absence of traditional synchronization using locks and mutexes in favor of low-level synchronization using hardware instructions. This calls for formal verification of such implementations. In this context, the de-facto standard correctness property is linearizability [Herlihy and Wing 1990]. It requires, intuitively, that each operation of a data structure implementation appears to execute atomically somewhen between its invocation and return. For users of lock-free data structures, linearizability is appealing. It provides the illusion of atomicity—they can use the data structure as if they were using it in a sequential setting.
Proving lock-free data structures linearizable has received a lot of attention (cf. Section 10). Doherty et al. [2004], for instance, give a mechanized proof of a practical lock-free queue. Such proofs require plenty of manual work and take a considerable amount of time. Moreover, they require an understanding of the proof method and the data structure under consideration. To overcome this drawback, we are interested in automated verification. The CAVE tool by Vafeiadis [2010a,b], for example, is able to establish linearizability for singly-linked data structures fully automatically.

The problem with automated verification for lock-free data structures is its limited applicability. Most techniques are restricted to implementations that assume a garbage collector (GC). This assumption, however, does not apply to all programming languages. Take C/C++ as an example. It does not provide an automatic garbage collector that is running in the background. Instead, it is the programmer’s obligation to avoid memory leaks by reclaiming memory that is no longer in use (using delete). In lock-free data structures, this task is much harder than it may seem at first glance. The root of the problem is that threads typically traverse the data structure without synchronization. Hence, there may be threads holding pointers to records that have already been removed from the structure. If records are reclaimed immediately after the removal, those threads are in danger of accessing deleted memory. Such accesses are considered unsafe (undefined behavior in C/C++ [ISO 2011]) and are a common cause for system crashes due to a segfault. The solution to this problem are so-called safe memory reclamation (SMR) algorithms. Their task is to provide lock-free means for deferring the reclamation/deletion until all unsynchronized threads have finished their accesses. Typically, this is done by replacing explicit deletions with calls to a function retire provided by the SMR algorithm which defers the deletion. Coming up with efficient and practical SMR implementations is difficult and an active field of research (cf. Section 10).

The use of SMR algorithms to manage manually the memory of lock-free data structures hinders verification, both manual and automated. This is due to the high complexity of such algorithms. As hinted before, an SMR implementation needs to be lock-free in order not to spoil the lock-free guarantee of the data structure using it. In fact, SMR algorithms are quite similar to lock-free data structures implementation-wise. This added complexity could not be handled by automatic verifiers up until recently. Meyer and Wolff [2019] were the first to present a practical approach. Their key insight is that the data structure can be verified as if it was relying on a garbage collector rather than an SMR algorithm, provided the data structure does not perform unsafe memory operations. Since data structures from the literature are usually memory safe, the above insight is a powerful tool for verification. Nevertheless, it leaves us with a hard task: establishing that all memory operations are safe in the presence of memory reclamation. Meyer and Wolff [2019] were not able to conduct this check under GC. Instead, they explore the entire state space of the data structure with SMR, restricting reallocations to a single address, to prove ABAs harmless (a criterion they require for soundness). Unfortunately, their state space exploration does not scale well.

In the present paper we tackle the challenge of proving a lock-free data structure memory safe. We present a type system to address this task. That is, we present a syntax-centric approach to establish the semantic property of memory safety. In particular, we no longer need expensive state space explorations that can handle SMR and memory reuse in order to prove memory safety. This allows us to utilize the full potential of the above result: if our type check succeeds, we remove the SMR code from the data structure and verify the resulting implementation using an off-the-shelf GC verifier. The idea behind our type system is a life cycle common to lock-free data structures with manual memory management via SMR [Brown 2015]. The life cycle, depicted in Figure 1, has four stages: (i) local, (ii) active, (iii) retired, and (iv) not allocated. Newly allocated records are in the local stage. The record is known only to the allocating thread; it has exclusive read/write access. The goal of the local stage is to prepare records for being published, i.e., added to the shared state of the data structure. When a record is published, it enters the active stage. In this stage, accesses to
the record are safe because it is guaranteed to be allocated. However, no thread has exclusive access and thus must fear interference by others. It is worth pointing out that a publication is irreversible. Once a record becomes active it cannot become local again. A thread, even if it removes the active record from the shared structures, must account for other threads that have already acquired a pointer to that record. To avoid memory leaks, removed records eventually become retired. In this stage, threads may still be able to access the record safely. Whether or not they can do so depends on the SMR algorithm used. Finally, the SMR algorithm detects that the retired record is no longer in use and reclaims it. Then, the memory can be reused and the life cycle begins anew.

The main challenge our type system has to address wrt. the above memory life cycle is the transition from the active to the retired stage. Due to the lack of synchronization, this can happen without a thread noticing. Programmers are aware of the problem. They protect records while they are active such that the SMR guarantees safe access even though the record is retired. To cope with this, our types integrate knowledge about the SMR algorithm. A core aspect of our development is that the actual SMR algorithm is an input to our type system—it is not tailored towards a specific SMR algorithm.

An additional challenge arises from the type system performing a thread-local analysis, it considers the program code as if it was sequential. This means the type system is not aware of the actual interference among threads, unlike state space explorations. To address this, we use types that are stable under the actions of interfering threads [Owicki and Gries 1976].

In practice, protecting a record while it is active is non-trivial. Between acquiring a pointer to the record and the subsequent SMR protection call, an interferer may retire the record, in which case the protection has no effect. SMR algorithms usually offer no means to check whether a protection was successful. Instead, programmers exploit intricate data structure invariants to perform this check. A common such invariant, for instance, is all shared reachable records are active. A type system typically cannot detect such data structure shape invariants. We turn this weakness into a strength. We deliberately do not track shape invariants nor alias information. Instead, we use simple annotations to mark pointers that point to active records. To relieve the programmer from arguing about their correctness, we show how to discharge annotations automatically. Interestingly, this can be done with off-the-shelf GC verifiers. It is worth pointing out that the ability to automatically discharge invariants allows for an automated guess-and-check approach for placing invariant annotations.

To increase the applicability of our type system, we use the theory of movers [Lipton 1975] as an enabling technique. Movers are a standard approach to transform a program into a more atomic version while retaining its behavior. That the resulting program is more atomic is beneficial for verification. The transformations are practical: Elmas et al. [2009], for example, automate them.

To demonstrate the usefulness of our approach, we implemented a linearizability checker which realizes the techniques presented in this paper. That is, our tool (i) performs a type inference to establish memory safety relying on invariant annotations, (ii) discharges the annotations under GC using cave as a back-end, and (iii) verifies linearizability under GC using cave. Additionally, we implemented a prototype for automatically inserting annotations and applying movers. These program transformations are performed on demand, guided by a failed type inference. Our tool is able to establish linearizability for lock-free data structures from the literature, like Michael&Scott’s lock-free queue [Michael and Scott 1996], the Vechev&Yahav CAS set [Vechev and Yahav 2008], the
Vechev&Yahav DCAS set [Vechev and Yahav 2008], and the ORVYY set [O’Hearn et al. 2010], for the well-known hazard pointer method [Michael 2002b] as well as epoch-base reclamation [Fraser 2004]. We stress that our approach is not limited to CAVe as a back-end but can use any verifier for garbage collection. To the best of our knowledge, we are the first to automatically verify lock-free set implementations that use SMR.

We summarize our contributions and the outline of the paper:

§5 presents our type system for proving lock-free data structures memory safe wrt. a user-specified SMR algorithm,

§7 presents an efficient type inference algorithm,

§8 presents an instrumentation of the data structure under scrutiny to discharge invariant annotations fully automatically with the help of a GC verifier, and

§9 evaluates our approach on well-known lock-free data structures from the literature.

We illustrate our contribution in §2, introduce the programming model in §3, discuss preliminary results in §4, give a comprehensive example in §6, and discuss related work in §10.

2 THE CONTRIBUTION ON AN EXAMPLE

We illustrate our approach on Michael&Scott’s lock-free queue [Michael and Scott 1996], Figure 2, which is used, for example, as Java’s ConcurrentLinkedQueue and as C++ Boost’s lockfree::queue. The queue is organized as a NULL-terminated singly-linked list of nodes. The enqueue operation appends new nodes to the end of the list. To do so, an enqueuer first moves Tail to the last node as it may lack behind. Then, the new node is appended by pointing Tail->next to it. Last, the enqueuer tries to move Tail to the end of the list. This can fail as another thread may already have moved Tail to avoid waiting for the enqueuer. The dequeue operation removes the first node from the list. Since the first node is a dummy node, dequeue reads out the data value of the second node in the list and then moves the Head to that node. Additionally, dequeue maintains the property that Head does not overtake Tail. This is done by moving Tail towards the end of the list if necessary. (There is an optimized version due to Doherty et al. [2004] which avoids this step.) Note that updates to the shared list of nodes are performed exclusively with single-word atomic compare-and-swap (CAS).

So far, the discussed implementation assumes a garbage collector. The nodes allocated by enqueue are not reclaimed explicitly after being removed from the shared list by dequeue: the queue leaks memory. Unfortunately, there is no simple solution to this problem. Uncommenting the explicit deletion from Line 51 avoids the leak. However, it leads to use-after-free bugs. Due to the lack of synchronization, threads may still hold and dereference pointers to the now deleted node. A dereference of such a dangling pointer, however, is unsafe. In C/C++, for example, dereferencing a dangling pointer has undefined behavior [ISO 2011] and may make the system crash with a segfault.

To solve the problem, programmers employ safe memory reclamation (SMR) algorithms. Two well-known examples are epoch-based reclamation (EBR) [Fraser 2004] and hazard pointers (HP) Michael [2002b]. They offer a function retire that replaces the ordinary delete. The difference is that retire does not immediately delete nodes. Instead, it defers the deletion until it is safe. In order to discover whether a deletion is safe, threads need to declare which nodes they access. How this is done depends on the SMR algorithm.

Epoch-based reclamation offers two additional functions leaveQ and enterQ. Threads use the former to announce that they are going to access the data structure and use the latter to announce that they have finished the access. The function names, in particular the Q, refer to the fact that the threads are quiescent [McKenney and Slingwine 1998] between enterQ and leaveQ, meaning they do not modify the data structure. During the non-quiescent period, EBR guarantees that the shared reachable nodes are not reclaimed, even if they are removed from the data structure and retired. To use EBR, the programmer simply replaces delete statements with calls to retire and

Proc. ACM Program. Lang., Vol. 4, No. POPL, Article 68. Publication date: January 2020.
adds calls to `leaveQ` (`enterQ`) at the beginning (end) of data structure operations. Consider Figure 2 for an example; the lines marked by E are the modifications required to use EBR. While easy to use, EBR implementations usually stop reclaiming memory altogether upon thread failure. Hazard pointers do not suffer from this problem.

The hazard pointer method requires threads to declare which nodes they access in a per-node fashion. To that end, HP offers an additional function: `protect`. It signals that a deletion of the received node should be deferred. To be precise, HP guarantees that the deletion of a node is deferred if it has been continuously protected since before it was retired [Gotsman et al. 2013]. While this method is conceptually simple, it is non-trivial to apply.

To use hazard pointers with Michael & Scott’s queue requires to add the code marked by H in Figure 2. As for EBR, delete statements are replaced with `retire`. Moreover, pointers that are accessed need protection to defer their deletion. Simply calling `protect` is usually insufficient as the protect may be too late. A common pattern for protecting pointers is to first protect them...
and then check that they have not been retired since. In Michael & Scott’s queue this is done by testing whether the protected nodes are still shared reachable—the queue maintains the invariant that nodes reachable from the shared pointers are never retired. To make this precise, consider Lines 34 to 36. Line 34 reads in head from the shared pointer Head. The dequeue operation will access (dereference) head. Hence, it has to make sure that the referenced node remains allocated. To do so, a protection of head is issued in Line 35. However, the node pointed to by head may have been dequeue and retired since head was read. To ensure that the protection is successful, that is, not too late, Line 36 restarts the dequeue operation in case head no longer coincides with Head. The remaining protections in the code follow the same principle.

Our contribution is a method for verifying lock-free data structures which use an SMR algorithm, like Michael & Scott’s queue with EBR/HP from Figure 2. At the heart of our method lies a type system which proves safe all pointer operations in the data structure. In the case of hazard pointers, for instance, this requires to prove all pointer accesses appropriately protected. Once this property is established, we show that the actual verification does not need to consider the SMR algorithm: it suffices to verify the data structure under garbage collection; the SMR function invocations can be removed altogether. This allows the use of off-the-shelf GC verifiers.

2.1 A Type System to Simplify Verification

Our main contribution is a type system a successful type check of which proves a given program free from unsafe memory operations. The type assigned to a pointer specifies if it is safe to access that pointer. The types are influenced by both the memory life cycle from Section 1 and the SMR algorithm used. In the case of hazard pointers, a pointer may be protected and thus guaranteed not to be deleted. Hence, the protected pointer can be accessed without precautions. For an unprotected pointer, on the other hand, threads may need to take additional steps to guarantee that the pointer is not dangling, for instance, by establishing that it (to be precise, its address) is in the active stage.

We illustrate our type system on the dequeue operation of Michael & Scott’s queue. The interesting part is the typing of the local pointers head and next in Lines 34 to 40. The type derivation is depicted in Figure 3. Let us assume for the moment that the shared pointers and the nodes reachable through them are in the active stage. We denote this by shared : A. It is the only type binding at the beginning of the operation. The first assignment, Line 34, adds a type binding for head to the type environment. The type for head is copied from the source pointer, Head. However, we remove A immediately after the assignment so that the actual type of head is Ø. The reason for this are interfering threads: as discussed above, an interferer can dequeue and retire the node pointed to by head. As a consequence, we cannot guarantee that head is active; we indeed need to remove A. Next, Line 35 protects head. We set the type of head to $E_{isu}$, encoding that a protection has been issued. Remembering that head is protected is crucial for the subsequent conditional. Line 36 tests whether Head has changed since it was read into head. If it has not, denoted by assume(head == Head) in Figure 3, we join the type of head with the type of Head. That is, head receives A. Now, we know that the protection has been issued before the node pointed to by head has been retired. So the hazard pointer method guarantees that the node is not deleted. The
subsequent code can access head without precautions. We incorporate this fact into the type of head by updating it to $S$, indicating that accesses are safe. (We skip the assignment to tail from Line 37, it does not affect the type check.) Next, Line 38 dereferences head. This dereference is safe since head has type $S$, it is guaranteed to be allocated. The type assigned to next is $\emptyset$ because we do not assign types to pointers within nodes, like head->next. Hence, next cannot obtain any guarantees from the assignment. Line 39 then protects next. Similarly to the above, we set its type to $S_{list}$. The following conditional, Line 40, tests again if Head has changed since the beginning of the operation. Consider the case it has not. If we remember that next is the successor of head, we know that next references a shared reachable node. Hence, we can assign type $A$ to next. As in the case for head, this allows us to lift the type to $S$. That is, using next in the following code becomes safe due to the conditional guaranteeing its activeness. The remainder of the type check is then straightforward since only protected and/or shared pointers are used.

We stress that the actual SMR algorithm is a parameter to our type system—it is not limited to analyzing programs using hazard pointers.

2.2 Data Structure Invariants in the Type System

The type check as illustrated in Section 2.1 is idealized. We assumed that we maintain type $A$ for shared pointers and the nodes reachable through them. Moreover, we assumed that next remains the successor of head during an execution of dequeue. Such invariants of the data structure are notoriously hard to derive. Typically, it requires a state-space exploration of all thread interleavings to find invariants of lock-free data structures. A major challenge in exploring the state space is the need for an effective (symbolic) way of tracking the data structure shape [Abdulla et al. 2013; Brookes 2004; O’Hearn 2004; O’Hearn et al. 2001; Reynolds 2002].

We tackle the above problem as follows: we do not track the data structure shape at all, not even pointer aliases. Instead, we require the programmer to annotate which pointers/nodes are active. This allows the type check to rely on data structure invariants which typically cannot be found by a type system. To free the programmer from manually proving the correctness of such annotations, we automate the correctness check. We give an instrumentation of the program under scrutiny such that an ordinary GC verifier can discharge the invariants. A thing to note is that the simple nature of active annotations and the ability to automatically discharge them makes it possible to find appropriate annotations fully automatically (guided by a failed type check).

Revisiting the previous example, the type environments never contain $shared : A$. To arrive at type $S$ for head in Line 36 nevertheless, we annotate the assume(head == Head) statement with an invariant stating that head is active. Then, the type derivation for Line 36 remains the same as before. We argue that, provided the queue implementation is memory safe, there must be a code location between the protection in Line 35 and the subsequent dereference in Line 38 where an active annotation can be placed. To see this, assume there is no such code location. This means head is not active in Lines 35 to 38. That is, it must have been retired before the protection in Line 35, rendering the protect unsuccessful. Hence, the dereference in Line 38 is unsafe, contradicting our assumption of memory safety. For pointer next, we proceed similarly and add an active annotation to the second assumption (Line 40).

With the above annotations our type system can rely on aspects of the dynamic behavior without requiring the programmer to manually take over parts of the verification. We believe that having annotations makes the type system more versatile (compared to having none) in the sense that data structures need not satisfy implicit invariants like all shared pointers and nodes are active. Moreover, relying on annotations rather than shape invariants allows for a much simpler type system.
2.3 Supporting Different SMR Algorithms

The above illustration focuses on hazard pointers. The actual type system we develop in Section 5 does not—it is not tailored towards a specific SMR algorithm. To achieve this degree of freedom, our type system takes as a parameter a formal description of the SMR algorithm being used. We rely on a recent specification language for SMR algorithms [Meyer and Wolff 2019]: SMR automata. Then, our types capture the locations of the SMR automaton that can be reached after having seen a sequence of SMR calls in the program (control-flow sensitive type system). This allows the types to track the relevant sequences of SMR calls. Moreover, it allows them to detect when the deletion of a node is guaranteed to be deferred in order to infer type $S$.

3 PROGRAMMING MODEL

We introduce concurrent shared-memory programs that employ a library for safe memory reclamation (SMR) and are annotated by invariants. A programming construct that is new to our model are angels, ghost variables with an angelic semantics. Angels are second-order pointers holding sets of addresses. When typing (cf. Section 5), angels will help us track the protected nodes.

3.1 Programs

We define a core language for concurrent shared-memory programs. Invocations to a library for safe memory reclamation and invariant annotations will be added below. Programs $P$ are comprised of statements defined by

\[
\begin{align*}
stmt & ::= \ text{stmt; stmt} \mid \ text{stmt} \oplus \ text{stmt} \mid \ text{stmt}^* \mid \ text{com} \\
\text{com} & ::= \ p := q \mid p := q.\text{next} \mid p.\text{next} := q \mid u := q.\text{data} \mid p.\text{data} := u \mid u := \text{op}(\bar{u}) \\
\text{cond} & ::= p = q \mid p \neq q \mid \text{pred}(\bar{u}) .
\end{align*}
\]

We assume a strict typing that distinguishes between data variables $u, u' \in DVar$ and pointer variables $p, q \in PVar$. Notation $\bar{u}$ is short for $u_1, \ldots, u_n$. The language includes sequential composition, non-deterministic choice, and Kleene iteration. The primitive commands include assignments, memory accesses, memory allocations, assumptions, and atomic blocks. They have the usual meaning. We make the semantics of commands precise in a moment.

Memory. Programs operate over addresses from $Adr$ that are assigned to pointer expressions $PExp$. A pointer expression is either a pointer variable from $PVar$ or a pointer selector $a.\text{next} \in PSel$. The set of shared pointer variables accessible by every thread is $\text{shared} \subseteq PVar$. Additionally, we allow pointer expressions to hold the special value $\text{seg} \notin Adr$ denoting undefined/uninitialized pointers. There is also an underlying data domain $\text{Dom}$ to which data expressions $DExp = DVar \cup DSel$ with $a.\text{data} \in DSel$ evaluate. A generalization of our development to further selectors is straightforward.

The memory is a partial function $m : PExp \cup DExp \rightarrow Adr \cup \{\text{seg}\} \cup \text{Dom}$ that respects the typing. The initial memory is $m_e$. Pointer variables $p$ are uninitialized, $m_e(p) = \text{seg}$. Data variables $u$ have a default value, $m_e(u) = 0$. We modify the memory with updates $up$ of the form $e \mapsto v$. Applied to a memory $m$, the result is the memory $m' = m[e \mapsto v]$ defined by $m'(e) = v$ and $m'(e') = m(e')$ for all $e' \neq e$. Below, we define computations $\tau$ which give rise to sequences of updates. We write $m_\tau$ for the memory resulting from the initial memory $m_e$ when applying the sequence of updates in $\tau$.

Liberal Semantics. We define a semantics where program $P$ is executed by a possibly unbounded number of threads. In this semantics some addresses may be freed non-deterministically by the runtime environment. This behavior will be constrained by a memory reclamation algorithm in a moment. Formally, the liberal semantics of program $P$ is the set of computations $\parallel P \parallel_X^Y$. It is defined
relative to two sets $Y \subseteq X \subseteq \text{Adr}$ of addresses allowed to be reallocated and freed, respectively. A computation is a sequence $\tau$ of actions of the form $act = (t, \text{com}, up)$. The action indicates that thread $t$ executes command $\text{com}$ that results in the memory update $up$. The definition of the liberal semantics is by induction. The empty computation is always contained, $\varepsilon \in \mathcal{P} \mathcal{X}$. Then, action $act$ can be appended to computation $\tau$, denoted $\tau . \text{act} \in \mathcal{P} \mathcal{X}$, if $\tau \in \mathcal{P} \mathcal{X}$, $act$ respects the control flow of $P$, and one of the following holds.

**Assign** If $act = (t, p.\text{next} := q.a.\text{next} \leftrightarrow b)$ then $m_\tau(p) = a$ and $m_\tau(q) = b$. There are similar conditions for the remaining assignments.

**Assume** If $act = (t, \text{assume} \ lhs = \text{rhs}, \emptyset)$ then $m_\tau(\text{lhs}) = m_\tau(\text{rhs})$. There are similar conditions for the remaining assumptions.

**Malloc** If $act = (t, p := \text{malloc, up})$, then $up$ has the form $p \mapsto a, a.\text{next} \mapsto \text{seg}, a.\text{data} \mapsto d$ so that $a \in \text{fresh}(\tau)$ or $a \in \text{freed}(\tau) \cap Y$, and $d \in \text{Dom}$. 

**Free** If $act = (t, \text{free}(a), \emptyset)$ then $a \in X$.

**Atomic** If $act = (t, \text{beginAtomic}, \emptyset)$ or $act = (t, \text{endAtomic}, \emptyset)$.

Note that Rule (Free) may spontaneously emit free$(a)$, although there is no free command in the programming language. Indeed, the free command will be issued by the memory reclamation algorithm defined in the next section (it is not part of $P$). The rule allows us to define the set of allocatable addresses for rule (Malloc) as addresses that have never been allocated in the computation, denoted by fresh$(\tau)$, and addresses which have been freed since their last allocation, freed$(\tau)$.

### 3.2 Safe Memory Reclamation

We consider programs that manage their memory with the help of a safe memory reclamation (SMR) algorithm. In this setting, threads do not free their memory themselves (no explicit free command), but request the SMR algorithm to do so. The SMR algorithm will have means of understanding whether an address is still accessed by other threads, and only execute the free when it is safe to do so. As a consequence, the semantics of the program depends on the SMR algorithm it invokes.

The means of detecting whether an address can be freed safely depend on the SMR algorithm. Despite the variety of techniques, it was recently observed that the behavior of major SMR algorithms can be captured by a common specification language [Meyer and Wolff 2019]: SMR automata.\(^1\)

Intuitively, the SMR automaton models the protection protocol of its SMR algorithm, while abstracting from implementation details. We recall SMR automata and use them to restrict the liberal semantics to the frees performed by the SMR algorithm.

**SMR Automata.** An SMR algorithm offers a set of functions $f(\tau)$ for the programmer to provide information about the intended access to the data structure, like leaveQ, enterQ, and retire in the case of EBR (cf. Section 2). An SMR automaton, as depicted in Figure 4, is a finite control structure the transitions of which are labeled with these function symbols. Additionally, each transition comes with a guard. The guard influences the flow of control in the SMR automaton based on the actual parameters of function calls. To distinguish the parameters, the automaton maintains a finite set of local variables storing thread identifiers and addresses. Guards may then compare the actual parameters with the values of variables.

What makes SMR automata a useful modeling language is their compactness: complex SMR algorithms can be captured by fairly small SMR automata. This is achieved by an interesting definition of the semantics. SMR automata accept bad behavior, free commands that should not be executed after a sequence of SMR function calls protecting the address.

---

\(^1\)Working on compositional verification, Meyer and Wolff [2019] call them observers.
What makes SMR automata interesting for automated verification are two technical restrictions that limit their expressiveness. First, the variable values are chosen only once, in the beginning of the computation, and never changed. This choice is non-deterministic. The idea is that the automaton picks some protection to track. Second, transition guards can only compare for equality. That this is sufficient to properly model the behavior of SMR algorithms can be explained by the fact that SMR algorithms are designed to work with very different data structures, from stacks to queues to trees. Hence, there is no point for the SMR algorithm to store information about the data structure more specific than the equality of pointers.

Syntactically, an SMR automaton $O$ is a tuple consisting of a finite set of locations, a finite set of variables, and a finite set of transitions. There is a dedicated initial location and a number of accepting locations. Transitions are of the form $l^f_g l'$ with locations $l, l'$, event $f(\bar{r})$, and guard $g$. Events $f(\bar{r})$ consist of a type $f$ and parameters $\bar{r} = r_1, \ldots, r_n$. The guard is a Boolean formula over equalities of variables and parameters $\bar{r}$.

Semantically, a (runtime) state $s$ of the SMR automaton is a tuple $(l, \phi)$ where $l$ is a location and $\phi$ maps variables to values. Such a state is initial if $l$ is initial, and similarly accepting if $l$ is accepting. Then, $(l, \phi)\xrightarrow{f_g} (l', \phi)$ is an SMR step if $l^f_g l'$ is a transition and $\phi(g[l \mapsto \bar{v}])$ evaluates to true. By $\phi(g[l \mapsto \bar{v}])$ we mean $\bar{g}$ with the variables replaced by their $\phi$-mapped values and the formal parameters $\bar{r}$ replaced by the actual values $\bar{v}$. As mentioned before, the valuation $\phi$ is chosen non-deterministically in the beginning; it is not changed by steps. A history $h = f_1(\bar{v}_1) \ldots f_n(\bar{v}_n)$ is a sequence of events. If there are SMR steps $s f_1(\bar{v}_1) \ldots f_n(\bar{v}_n) s'$, we write $s \xrightarrow{h} s'$. If $s'$ is accepting, we say that $h$ is accepted by $s$.

Acceptance in SMR automata characterizes bad behavior, and a history $h$ is said to violate $O$ if there is an initial state $s$ and an accepting state $s'$ such that $s \xrightarrow{h} s'$. The specification of $O$ is the set of histories that are not accepted:

$$S(O) := \{ h \mid \forall s, s'. s \xrightarrow{h} s' \land s \text{ initial } \Rightarrow \text{ s' not accepting}\} .$$

We also use a restriction of the specification. The set $F_O(h, a)$ contains those continuations $h'$ of $h$ so that $h, h' \in S(O)$ and moreover at most address $a$ is freed in $h'$. As bad behavior means executing a forbidden free, we assume accepting states can only be reached by transitions labeled with $\text{free}$ and cannot be left.

To give an example, consider the SMR automaton $O_{\text{Base}} \times O_{\text{EBR}}$ from Figure 4. It formalizes the informal specification of EBR from Section 2. Automaton $O_{\text{Base}}$. Figure 4a, forbids an EBR implementation to free addresses that have not yet been retired or have not been retired since their last free. Put differently, it forbids spurious frees and double-frees. Automaton $O_{\text{EBR}}$. Figure 4b, requires the EBR implementation to defer the $\text{free}$ of retired nodes which could still be accessed by some thread. A thread can still access the retired node if it has acquired a pointer to the node before it was retired (following the usage policy of EBR discussed in Section 2). This is the case if the thread started accessing the data structure before the $\text{retire}$, which it announces via a call to $\text{leaveQ}$.

While every SMR implementation has its own SMR automaton, the practically relevant SMR automata are products of $O_{\text{Base}}$ with further SMR automata [Meyer and Wolff 2019], like for EBR in the above example. Our development relies on this.

We also assume that the SMR automaton has two distinguished variables $z_t$ and $z_a$. Intuitively, variable $z_t$ will store the thread for which the SMR automaton tracks the protection of the address stored in $z_a$. All SMR algorithms we know can be specified with only two variables. A possible explanation is that SMR algorithms do not seem to use helping [Herlihy and Shavit 2008] to protect.

---

2The product operation on SMR automata is defined as expected and leads to an intersection of the specifications.
(a) SMR automaton specifying that address \( a_z \) may be freed only if it has been retired and not freed since. The automaton uses one variable \( a_z \).

(b) SMR automaton characterizing when EBR defers frees, using two variables \( z_t \) and \( a_z \). It states that address \( a_z \) must not be freed if it was retired while \( z_t \) is in-between `leaveQ` and `enterQ` calls.

![Diagram](image)

Fig. 4. Epoch-based reclamation (EBR) is specified by the SMR automaton \( O_{\text{Base}} \times O_{\text{EBR}} \). For legibility, we omit self loops on all locations for the events that are not given.

Pointers. We are not aware of an SMR algorithm where the protection of an address would be inferred from communication with another address or, more ambitiously, another thread.

Moreover, we inherit from [Meyer and Wolff 2019] the natural requirement that SMR algorithms do not remember addresses that have been freed in order to detect (and react to) reallocations. Formally, an SMR automaton supports elision if for all histories \( h \) the behavior on address \( a \) after \( h \) (i) is not affected by a free of another address \( b \), \( F_\mathcal{O}(h, \text{free}(b), a) = F_\mathcal{O}(h, a) \), (ii) is not affected by renaming another two addresses \( b \) and \( c \), \( F_\mathcal{O}(h, a) = F_\mathcal{O}(h[b/c], a) \), (iii) is included in the behavior on \( a \) after another history \( h' \) provided \( a \) is fresh after \( h' \), \( F_\mathcal{O}(h, a) \subseteq F_\mathcal{O}(h', a) \), and (iv) contains the behavior on \( a \) after \( h, \text{free}(a) \), \( F_\mathcal{O}(h, \text{free}(a), a) \subseteq F_\mathcal{O}(h, a) \). To understand (iv), note that the task of the SMR algorithm is to protect addresses from being freed. Hence it is safe to delay frees.

For convenience, we summarize our assumptions on SMR automata. All SMR automata we encountered, including the ones from [Meyer and Wolff 2019], satisfy them.

**Assumption 1.** SMR automata (i) reach accepting states only with `free` and do not leave them, (ii) are products with \( O_{\text{Base}} \), (iii) have distinguished variables \( z_t \) and \( a_z \), and (iv) support elision.

It will be convenient to have a post-image \( \text{post}_{p, \text{com}}(L) \) on the locations of SMR automata. The post-image yields a set of locations \( L' \) reachable by taking a \( \text{com} \)-labeled transition from \( L \). The considered transition is restricted in two ways. First, its guard \( g \) must allow \( z_t \) to track thread \( t \) executing \( \text{com} \). Second, if \( p \) appears as a parameter in \( \text{com} \), then guard \( g \) must allow \( a_z \) to track \( p \). Formally, these requirements translate to the satisfiability of \( g \land t = z_t \) and \( g \land p = a_z \), respectively. The parameterization in \( p \) makes the post-image precise. For an example, consider \( O_{\text{Base}} \) and the command \( \text{com} = \text{enter retire}(p) \). We expect the post-image of \( L_2 \) wrt. \( \text{com} \) and \( p \) to be \( \text{post}_{p, \text{com}}(L_2) = \{L_3\} \). The address has definitely been retired. Without the parametrization in \( p \), we would get \( \{L_2, L_3\} \). The transition could choose not to track \( p \).
**SMR Semantics.** To incorporate SMR automata into our programming model, we generalize the set of program commands $\text{com}$ to include calls to and returns from SMR functions: $\text{com} ::= \text{com} \mid \text{enter \ func}(p, \bar{u}) \mid \text{exit \ func}$. We add corresponding actions to the liberal semantics $\llbracket P \rrbracket^X_Y$. They make visible the function call/return but do not lead to memory updates.

$\text{(Enter)}$ $\text{act} = (t, \text{enter \ func}(p, \bar{u}), \emptyset)$. $\text{(Exit)}$ $\text{act} = (t, \text{exit \ func}, \emptyset)$.

To use SMR automata in the context of computations, we convert a computation $\tau$ into a history $h$ by projecting $\tau$ to the enter, exit, and free commands and replacing the formal parameters with the actual values. To be precise, we use as events the function names offered by the SMR algorithm plus free. The parameters to an event are the values of the actual parameters as well as the executing thread. In the case of exit events, we drop the actual parameters and in case of free events we drop the executing thread. For example, $\mathcal{H}(\tau.(t, \text{enter \ func}(p), \emptyset)) = \mathcal{H}(\tau).\text{func}(t, m_x(p))$.

The SMR semantics of a program is the restriction of the liberal semantics to the specification of the SMR automaton of interest. More precisely, given an SMR automaton $O$ and sets $Y \subseteq X \subseteq \text{Adr}$ of reallocatable and freeable addresses, the SMR semantics induced by $O, X, Y$ of program $P$ is $\llbracket P \rrbracket^Y_X := \{ \tau \mid \tau \in \llbracket P \rrbracket^Y_X \land \mathcal{H}(\tau) \in S(O) \}$. SMR algorithms only restrict the execution of free commands, their functions can always be invoked by the program. SMR automata mimic this by including in their specification all histories that do not respect the control flow. In particular, we have the following property. In the absence of frees, the SMR automaton does not play a role. The resulting semantics, $\llbracket P \rrbracket^Y_\emptyset$, is garbage collection (GC).

**Lemma 3.1.** $\llbracket P \rrbracket^Y_\emptyset = \llbracket P \rrbracket^Y_\emptyset$ for every SMR automaton $O$.

To see the lemma, note that only accepting states in $O$ may rule out computations from $\llbracket P \rrbracket^Y_\emptyset$. By Assumption 1, only events free(a) may lead to such accepting states.

Reconsider the SMR automaton $O_{\text{Base}}$. For this automaton to properly restrict the frees in a program, the program should not perform double retires, that is, not retire an address again before it is freed. The point is that SMR algorithms typically misbehave after a double retire (perform double frees), which is not reflected in $O_{\text{Base}}$ (it does not allow for double frees after a double retire). Our type system will establish the absence of double retires for a given program.

### 3.3 Angels

Angels can be understood as ghost variables with an angelic semantics. Like for ghosts, their purpose is verification: angels store information about the computation that can be used in invariants but that cannot be used to influence the control flow. This information is a set of addresses, which means angels are second-order pointers. The set of addresses is determined by an angelic choice, a non-deterministic assignment that is beneficial for the future of the computation.

The idea behind angels is the following. When typing, some invariants of the runtime behavior are not respect the control flow. In particular, we have the following property. In the absence of frees, the SMR automaton does not play a role. The resulting semantics, $\llbracket P \rrbracket^Y_\emptyset$, is garbage collection (GC).

**Lemma 3.1.** $\llbracket P \rrbracket^Y_\emptyset = \llbracket P \rrbracket^Y_\emptyset$ for every SMR automaton $O$.

To see the lemma, note that only accepting states in $O$ may rule out computations from $\llbracket P \rrbracket^Y_\emptyset$. By Assumption 1, only events free(a) may lead to such accepting states.

Reconsider the SMR automaton $O_{\text{Base}}$. For this automaton to properly restrict the frees in a program, the program should not perform double retires, that is, not retire an address again before it is freed. The point is that SMR algorithms typically misbehave after a double retire (perform double frees), which is not reflected in $O_{\text{Base}}$ (it does not allow for double frees after a double retire). Our type system will establish the absence of double retires for a given program.

**3.3 Angels**

Angels can be understood as ghost variables with an angelic semantics. Like for ghosts, their purpose is verification: angels store information about the computation that can be used in invariants but that cannot be used to influence the control flow. This information is a set of addresses, which means angels are second-order pointers. The set of addresses is determined by an angelic choice, a non-deterministic assignment that is beneficial for the future of the computation.

The idea behind angels is the following. When typing, some invariants of the runtime behavior may not be deducible by the type system. Angels allow the programmer to make them explicit in the program and thus available to the type check. Consider EBR’s leaveQ function. It guarantees that all currently active addresses remain allocated, i.e., will not be reclaimed even if they are retired. An angelic choice is convenient for selecting the set. Subsequent dereferences can then use invariant annotations to ensure that the dereferenced pointer holds an address in the set captured by the angel. With this, our type system is able to detect that the access is safe.

To incorporate angels and invariant annotations into our programming model, we generalize the set of commands as follows

\[
\text{com} ::= \text{com} \mid @\text{inv \ angel \ r} \mid @\text{inv \ p = q} \mid @\text{inv \ p \ in \ r} \mid @\text{inv \ active}(p) \mid @\text{inv \ active}(r).
\]

Proc. ACM Program. Lang., Vol. 4, No. POPL, Article 68. Publication date: January 2020.
Angels are local variables $r$ from the set $AVar$. Invariant annotations include allocations of angels with the keyword $\text{angel}$ $r$. Intuitively, this will map the angel to a set of addresses. Conditionals behave as expected. The membership assertion $p \in r$ checks that the address of $p$ is included in the set of addresses held by the angel $r$. The predicate $\text{active}(p)$ expresses that the address pointed to by $p$ currently is neither freed nor retired, and similar for $\text{active}(r)$. We use $x$ to uniformly refer to pointers $p$ and angels $r$.

In the liberal semantics $\llbracket P \rrbracket^\nu_{X}$, the above commands do not lead to memory updates: (Invariant) $\text{act} = (t, @\text{inv} \bullet, \emptyset)$.

Invariant annotations behave like assertions, they do not influence the semantics but it has to be verified that they hold for all computations. To make precise what it means for invariant annotations to hold for a computation $\tau$, we construct a formula $\text{inv}(\tau)$. The invariant annotations are defined to hold for $\tau$ iff $\text{inv}(\tau)$ is valid. The construction of the formula is given in Figure 5. There, $\text{active}(\sigma)$ is the set of addresses that are neither freed nor retired after computation $\sigma$. We only consider programs leading to closed formulas, meaning every angel is allocated (and hence quantified) before it is used. The semantics of the formula is as expected: angels evaluate to sets of addresses, equality of addresses is the identity, and membership is as usual for sets. Section 8 shows how to automatically prove the correctness of invariant annotations for all computations.

### 4 GETTING RID OF MEMORY RECLAMATION

Despite the compact formulation of SMR algorithms as SMR automata, analyzing programs in the presence of memory reclamation remains difficult. Unlike for programs running under garbage collection, ownership guarantees [Bornat et al. 2005; Boyland 2003] and the resulting thread-local reasoning techniques [Brookes 2004; O’Hearn 2004; O’Hearn et al. 2001; Reynolds 2002] do not apply. Meyer and Wolff [2019] bridge this gap. They show that it is sound and complete to conduct the verification under garbage collection provided the program properly manages its memory. So one can establish this requirement and then perform the actual verification under the simpler semantics. Their statement is as follows; we give the missing definitions in a moment.

**Theorem 4.1 (Consequence of Theorem 5.20 in [Meyer and Wolff 2019]).** If the semantics $O[\llbracket P \rrbracket^\nu_{Adr}]$ is pointer-race-free, then $O[\llbracket P \rrbracket^\nu_{Adr}]$ corresponds to $\llbracket P \rrbracket^\nu_{\emptyset}$.

With the above theorem, the only property to be checked in the presence of memory reclamation is the premise of pointer race freedom. However, Meyer and Wolff [2019] report on this task as being rather challenging, requiring an intricate state space exploration of a semantics much more...
complicated than garbage collection. The contribution of the present paper is a type system to
tackle exactly this challenge (cf. Section 5).

We elaborate on pointer races and the correspondence between the semantics.

**Pointer Race Freedom.** Pointer races generalize the concept of memory errors by taking into
account the SMR algorithm [Haziza et al. 2016; Meyer and Wolff 2019]. A memory error is an access
through a dangling pointer, to a pointer that has been freed. Such accesses are prone to
system crashes, for example, due to segfaults. Indeed, the C/C++11 standard considers programs
with memory errors to have an undefined semantics (catch-fire semantics) [ISO 2011].

To make precise which pointers in a computation are dangling, Haziza et al. [2016] introduce the
notion of validity. A pointer is then dangling if it is invalid. Initially, all pointers are invalid. A pointer
is rendered valid if it receives its value from an allocation or from a valid pointer. A pointer becomes
invalid if its address is freed or it receives its value form an invalid pointer. It is worth pointing out
that free(a) invalidates all pointers to address a but a subsequent reallocation of a validates only
the receiving pointer. We denote the set of valid pointers after a computation τ by validτ.

We already argued that dereferences of invalid pointers may lead to system crashes. Consequently,
passing invalid pointers to the SMR algorithm may also be unsafe. Consider a call to retire(p)
requesting the SMR algorithm to free the address of p. If p is invalid, then its address has already
been freed, resulting in a system crash due to a double free. Yet, we cannot forbid invalid pointers
from being passed to SMR functions altogether. For instance, protect may be invoked with invalid
pointers in Lines 16 and 35 of Michael&Scott’s queue from Section 2. To support such calls, one
deems a command enter func(p, u) unsafe, if replacing the actual values of invalid pointer arguments
with arbitrary values may exhibit new (and potentially undesired) SMR behavior. We inherit the
the formal definition from Meyer and Wolff [2019] as it is an integral part of their proof strategy.

**Definition 4.2 (Definition 5.12 in Meyer and Wolff [2019]).** Consider a computation τ with history h.
A subsequent action act is an unsafe call if its command is enter func(p, u) with p_i \notin validτ for
some i, mτ.(p) = ̄a, mτ.(u) = ̄d, and:

\[ \exists c \exists ̄b. \left( \forall i. (a_i = c \lor p_i \in validτ) \implies a_i = b_i \right) \wedge \mathcal{F}_O(h.func(t, ̄b, ̄d), c) \notin \mathcal{F}_O(h.func(t, ̄a, ̄d), c). \]

**Definition 4.3 (Following Definition 5.13 in Meyer and Wolff [2019]).** A computation τ.act is a
pointer race if act (i) dereferences an invalid pointer, (ii) is an assumption comparing an invalid
pointer for equality, (iii) retires an invalid pointer, or (iv) is an unsafe call.

**Correspondence.** Theorem 4.1 establishes a correspondence between the behavior of full \(O[P]_{\text{Addr}}\)
and the simpler, garbage collected semantics \([P]_{\text{G}}\). It states that we find for every computation
τ \in \(O[P]_{\text{Addr}}\) another computation σ \in \([P]_{\text{G}}\) such that σ mimics τ. We denote this by τ \lessdot σ.
Relation \(\lessdot\) requires τ and σ to agree on the control locations of all threads and the valid memory
of τ. Intuitively, this means that any pointer-race-free action after τ has the same effect after σ
because the action cannot access the invalid part of the memory without raising a pointer race. Put
differently, threads cannot distinguish whether they execute in τ or in σ. So they cannot distinguish
whether or not memory is reclaimed.

Technically, τ and σ agree on the valid memory of τ if \(m_τ|_{validτ} = m_σ|_{validτ}\). Here, \(m_τ|_{validτ}\)
denotes the restriction of \(m_τ\) to its valid part \(validτ\). It restricts the domain of \(m_τ\) to \(validτ\) and
to data variables and to data selectors of addresses referenced from \(validτ\). It is worth pointing
out the asymmetry in the definition of \(τ \lessdot σ\): \(m_σ\) is restricted to \(validτ\). This is necessary because
there are no free commands in σ and thus pointer expressions that are invalidated in τ are never
invalidated in σ. The correspondence is precise enough for verification results of safety properties
to carry over from one semantics to the other.
5 A TYPE SYSTEM TO PROVE POINTER RACE FREEDOM

We present a type system a successful type check of which entails pointer race freedom as required by Theorem 4.1. The guiding idea of our types is to under-approximate the validity of pointers. To achieve this, our types incorporate the SMR algorithm in use and the guarantees it provides. It does so in a modular way: a parameter of the type system definition is an SMR automaton specifying the SMR algorithm.

A key design decision of our type system is to track no information about the data structure shape. Instead, we deduce runtime specific information from automatically dischargeable annotations. We still achieve the necessary precision because the same SMR algorithm may be used with different data structures. Hence, shape information should not help tracking its behavior.

5.1 Overview

Towards a definition of our type system, recall the memory life cycle from Section 1. The transition from the active to the retired stage requires care. The type system has to detect that a thread is guaranteed safe access to a retired node. This means finding out that an SMR protection was successful. Additionally, types need to be stable under interference. Nodes can be retired without a thread noticing. Hence, types need to ensure that the guarantees they provide cannot be spoiled by actions of other threads.

To tackle those problems, we use intersection types capturing which access guarantees a thread has for each pointer. We point out that this means we track information about nodes in memory through pointers to them. We use the following guarantees.

- **L**: Thread-local pointers referencing nodes in the local stage. The guarantee comes with two more properties. There are no valid aliases of the pointer and the referenced node is not retired. This gives the thread holding the pointer exclusive access.
- **A**: Pointers to nodes in the active stage. Active pointers are guaranteed to be valid, they can be accessed safely.
- **S**: Pointers to nodes which are protected by the SMR algorithm from being reclaimed. Such pointers can be accessed safely although the referenced node might be in the retired stage.
- **E_L**: SMR-specific guarantee that depends on a set of locations in the given SMR automaton. The idea is to track the history of SMR calls performed so far. This history is guaranteed to reach a location in L. The information about L bridges the (SMR-specific) gap between A and S. Accesses to the pointer are potentially unsafe.

The interplay among these guarantees tackles the aforementioned challenges as follows. Consider a thread that just acquired a pointer p to a shared node. In the case of hazard pointers, this pointer comes without access guarantees. Hence, the thread issues a protection of p. We denote this with an SMR-specific type E. For the protection to be successful, the programmer has to make sure that p is active during the invocation. The type system detects this through an annotation that adds guarantee A to p. We then deduce from the SMR automaton that p can be accessed safely because the protection was successful. This adds guarantee S. (We have seen this on an example in Section 2.)

5.2 Types

Throughout the remainder of the section we fix an SMR automaton O relative to which we describe the type system. The SMR automaton induces a set of intersection types [Coppo and Dezani-Ciancaglini 1978; Pierce 2002] defined by the following grammar:

\[ T ::= \emptyset \mid L \mid A \mid S \mid E_L \mid T \land T. \]
The meaning of the guarantees $L$ to $E_L$ is as explained above. We also write a type $T$ as the set of its guarantees where convenient. We define the predicate $isValid(T)$ to hold if $T \cap \{S, L, A\} \neq \emptyset$. The three guarantees serve as syntactic under-approximations of the semantic notion of validity from the definition of pointer races (cf. Section 4).

There is a restriction on the sets of locations $L$ for which we provide guarantees $E_L$. To understand it, note that our type system infers guarantees about the protection of pointers thread-locally from the code, that is, as if the code was sequential. Soundness then shows that these guarantees carry over to the computations of the overall program where threads interfere. To justify this sequential to concurrent lifting, we rely on the concept of interference freedom due to Owicki and Gries [1976]. A set of locations $L$ in the SMR automaton $O$ is closed under interference from other threads, if no SMR command issued by a thread different from $z_t$ (whose protection we track) can leave the locations. Formally, we require that for every transition $l \xrightarrow{t(x),g} l'$ with $l \in L$ and $l' \notin L$ we have guard $g$ implying $t' = z_t$. We only introduce guarantees $E_L$ for sets of locations $L$ that are closed under interference from other threads.

Type environments $\Gamma$ are total functions that assign a type to every pointer and every angel in the code being typed. To fix the notation, $\Gamma(x) = T$ or $x: T \in \Gamma$ means $x$ is assigned $T$ in environment $\Gamma$. We write $\Gamma, x: T$ for $\Gamma \uplus \{x: T\}$. If the type of $x$ does not matter, we just write $\Gamma, x$. The initial type environment $\Gamma_{init}$ assigns $\emptyset$ to every pointer and angel.

Our type system will be control-flow sensitive [Crary et al. 1999; Foster et al. 2002; Hunt and Sands 2006], which means type judgements take the form

$$\{\Gamma_{pre}\} \text{ stmt } \{\Gamma_{post}\}.$$

The thing to note is that the type assigned to a pointer/angel is not constant throughout the program but depends on the commands that have been executed. So we may have the type assignment $x: T$ in $\Gamma_{pre}$ but $x: T'$ in the type environment $\Gamma_{post}$ with $T \neq T'$.

Control-flow sensitivity requires us to formulate how types change under the execution of SMR commands. Towards a definition, we associate with every type a set of locations in $O = O_{Base} \times O'$. Guarantee $E_L$ already comes with a set of locations. Guarantee $S$ grants safe access to the tracked address. In terms of locations, it should not be possible to free the address stored in $z_a$. We define $SafeLoc(O)$ to be the largest set of locations in the SMR automaton that is closed under interference from other threads and for which there is no transition $l \xrightarrow{\text{free}(a),g} l'$ with $l \in SafeLoc(O)$, $l'$ not accepting, and $g$ implying $a = z_a$. Guarantee $A$ is characterized by location $L_2$ in $O_{Base}$. Indeed, a pointer is active iff $O_{Base}$ is in its initial location. For $L$ we also use location $L_2$. The discussion yields:

$$\begin{align*}
\text{Loc}(\emptyset) & := \text{Loc}(O) & \text{Loc}(E_L) & := L \\
\text{Loc}(A) & := \{L_2\} \times \text{Loc}(O') & \text{Loc}(S) & := \text{SafeLoc}(O) \\
\text{Loc}(L) & := \{L_2\} \times \text{Loc}(O') & \text{Loc}(T_1 \land T_2) & := \text{Loc}(T_1) \cap \text{Loc}(T_2) .
\end{align*}$$

The set of locations associated with a type is defined to over-approximate the locations reachable in the SMR automaton by the (history of the) current computation. With this understanding, it should be possible for command $com$ to transform $x: T$ into $x: T'$ if the locations associated with $T'$ over-approximate the post-image under $x$ and $com$ of the locations associated with $T$. We define the type transformer relation $T, x, com \sim T'$ by the following conditions:

$$\begin{align*}
\text{post}_{x,com}(\text{Loc}(T)) & \subseteq \text{Loc}(T') \\
isValid(T') & \Rightarrow isValid(T) \\
\{L, A\} \cap T' & \subseteq \{L, A\} \cap T .
\end{align*}$$
The over-approximation of the post-image is the first inclusion. The implication states that SMR commands cannot validate pointers. We can, however, deduce from the fact that the address has not been retired ($A$ or $L$) and the SMR command has been executed, that it is safe to access the address ($S$). The last inclusion states that SMR commands cannot establish the guarantees $L$ and $A$. It is worth pointing out that the relation $T, x, \text{com} \sim T’$ only depends on the SMR automaton, up to a choice of variable names. This means we can tabulate it to guarantee quick access when typed a program. We also write $\Gamma, \text{com} \sim \Gamma’$ if we have $\Gamma(x), x, \text{com} \sim \Gamma’(x)$ for all pointers/angels $x$. We write $\Gamma \sim \Gamma’$ if we take the post-image to be the identity. For an example, refer to Section 6.1.

Guarantees $L$ and $A$ are special in that their sets of locations, $\text{Loc}(L)$ and $\text{Loc}(A)$, are not closed under interference. For $L$, the type rules ensure interference freedom. They do so by enforcing that retire is not invoked with invalid pointers. Hence, the fact that $L$-pointers have no valid aliases implies that other threads cannot retire them. So $O_{\text{Base}}$ remains in $L_2$ no matter the interference. For $A$, the type rules account for interference. We define an operation $rm(\Gamma)$ that takes an environment and removes all $A$ guarantees for thread-local pointers and angels:

$$rm(\Gamma) := \{x : T \setminus \{A\} \mid x : T \in \Gamma \land x \notin \text{shared}\} \cup \{x : \emptyset \mid x \in \text{shared}\}.$$ 

The operation also has an effect on shared pointers and angels where it removes all guarantees. The reasoning is as follows. An interference on a shared pointer or angel may change the address being pointed to. Guarantees express properties about addresses, indirectly via their pointers. As we do not have any information about the new address, the pointer receives the empty set of guarantees.

5.3 Type System

Our type system is given in Figure 6. We write $\vdash \{I_{\text{init}}\} \text{stmt} \{\Gamma\}$ to indicate that $\{I_{\text{init}}\} \text{stmt} \{\Gamma\}$ is derivable with the given rules. We write $\vdash \text{stmt}$ if there is an environment $\Gamma$ so that $\vdash \{I_{\text{init}}\} \text{stmt} \{\Gamma\}$. In this case, we say the program type checks. Soundness will show that a type check entails pointer race freedom and the absence of double retires.

We distinguish between rules for statements and rules for primitive commands. We assume that primitive commands $\text{com}$ are wrapped inside an atomic block, like $\text{beginAtomic; com; endAtomic}$. With this assumption, the rules for primitive commands need not handle the fact that guarantee $A$ is not closed under interference. Interference will be taken into account by the rules for statements. The assumption of atomic blocks can be established by a simple preprocessing of the program. We do not make it explicit but assume it has been applied.

The rules for primitive commands, Figure 6a, that are not related to SMR are straightforward. Rule (ASSIGN1) copies the type of the right-hand side pointer to the left-hand side pointer of the assignment. Additionally, both pointers lose their $L$ qualifier since the command creates an alias. Rule (ASSIGN2) ensures that the dereferenced pointer is valid and then sets the type of the assigned pointer to the empty type. The assigned pointer does not receive any guarantees since we do not track guarantees for selectors. Rule (ASSIGN3) checks the dereferenced pointer for validity and removes $L$ from the pointer that is aliased. Data assignments, Rules (ASSIGN4), (ASSIGN5), and (ASSIGN6), simply check dereferenced pointers for validity. Allocations grant the target pointer the $L$ guarantee, Rule (MALLOC). Assumptions of the form $p = q$ check that both pointers are valid and join the type information, Rule (ASSUME1). Guarantee $L$ is removed due to the alias. All other assumptions have no effect on the type environment, Rule (ASSUME2). Similarly, Rule (EQUAL) joins type information in the case of assertions. However, no validity check is performed and $L$ is not removed. Rule (ACTIVE) adds the $A$ guarantee. Note that $x$ is a pointer or an angel. Angels are always local variables. Their allocation does not justify any guarantees, in particular not $L$, as they hold full sets of addresses, Rule (ANGEL). We can also assert membership of an address held by a pointer in a set of addresses held by an angel, Rule (MEMBER).
(ASSIGN1)  \[ T' = T \setminus \{L\} \]
\[ \{\Gamma, p, q:T\} p := q \{\Gamma, p:T', q:T'\} \]

(ASSIGN2)  \[ \Gamma(q) = T \quad isValid(T) \]
\[ \{\Gamma, p\} p := q.next \{\Gamma, p:\emptyset\} \]

(ASSIGN3)  \[ \Gamma(p) = T \quad isValid(T) \]
\[ \{\Gamma, q:T'\} p.next := q \{\Gamma, q:T'\} \]

(ASSIGN4)  \[ \Gamma(q) = T \quad isValid(T) \]
\[ \{\Gamma\} u := op(\bar{u}) \{\Gamma\} \]

(ASSIGN5)  \[ \Gamma(q) = T \quad isValid(T) \]
\[ \{\Gamma\} u := q.data \{\Gamma\} \]

(MALLOC)  \[ p \notin shared \quad T = \{L\} \]
\[ \{\Gamma, p\} p := malloc \{\Gamma, p:T\} \]

(ASSUME1)  \[ isValid(T) \quad isValid(T') \]
\[ T'' = (T \land T') \setminus \{L\} \]
\[ \{\Gamma, p:T, q:T'\} \text{assume } p = q \{\Gamma, p:T'', q:T''\} \]

(ASSUME2)  \[ \text{cond} \neq p = q \]
\[ \{\Gamma\} \text{assume} \text{cond} \{\Gamma\} \]

(EQUAL)  \[ T'' = T \land T' \]
\[ \{\Gamma, p:T, q:T'\} \text{@inv } p = q \{\Gamma, p:T'', q:T''\} \]

(ACTIVE)  \[ T' = T \land \{A\} \]
\[ \{\Gamma, x:T\} \text{@inv } \text{active}(x) \{\Gamma, x:T'\} \]

(ANGEL)  \[ r \notin shared \]
\[ \{\Gamma, r\} \text{@inv } \text{angel } r \{\Gamma, r:\emptyset\} \]

(MEMBER)  \[ \Gamma(r) = T' \quad T'' = T \land T' \]
\[ \{\Gamma, p:T\} \text{@inv } p \text{ in } r \{\Gamma, p:T''\} \]

(EXIT)  \[ \Gamma, \text{exit } \text{func} \sim \Gamma' \]
\[ \{\Gamma\} \text{exit } \text{func} \{\Gamma'\} \]

(a) Type rules for primitive commands.

(INFER)  \[ \Gamma_1 \rightsquigarrow \Gamma_2 \quad \{\Gamma_2\} \text{stmt } \{\Gamma_3\} \quad \Gamma_3 \rightsquigarrow \Gamma_4 \]
\[ \{\Gamma_1\} \text{stmt } \{\Gamma_4\} \]

(BEGIN)  \[ \{\Gamma\} \text{beginAtomic } \{\Gamma\} \quad \text{END} \]
\[ \{\Gamma\} \text{endAtomic } \{\text{rm}(\Gamma)\} \]

(SEQ)  \[ \{\Gamma\} \text{stmt}_1 \{\Gamma'\} \quad \{\Gamma'\} \text{stmt}_2 \{\Gamma''\} \]
\[ \{\Gamma\} \text{stmt}_1; \text{stmt}_2 \{\Gamma''\} \]

(CHOOSE)  \[ \{\Gamma\} \text{stmt}_1 \{\Gamma'\} \quad \{\Gamma\} \text{stmt}_2 \{\Gamma'\} \]
\[ \{\Gamma\} \text{stmt}_1 \oplus \text{stmt}_2 \{\Gamma'\} \]

(LOOP)  \[ \{\Gamma\} \text{stmt } \{\Gamma\} \]
\[ \{\Gamma\} \text{stmt}^* \{\Gamma\} \]

(b) Type rules for statements.

Fig. 6. Type rules.
SMR-related commands may change the entire type environment, rather than manipulating only the pointers that occur syntactically in the command. This is because of pointer aliasing on the one hand, and because of the SMR automaton on the other hand (for instance, enterQ has an effect on all pointers). The post type environment of Rules (ENTER) and (EXIT) simply infers guarantees wrt. the pre type environment and the emitted event. Note that this is the only way to infer SMR-specific guarantees \( B_L \), i.e., these guarantees solely depend on the SMR commands. Moreover, Rule (ENTER) performs a pointer race check as defined in Section 4. Predicate safeEnter(\( \Gamma, \text{func}(p, \bar{u}) \)) evaluates to true iff the command enter func(p, \( \bar{u} \)) is guaranteed to be free from pointer races given the types in \( \Gamma \). The formalization coincides with Definition 4.2 except that it replaces valid by the under-approximation isValid(). A special case of Rule (ENTER) is the invocation of retire(p), which requires the argument \( p \) to be active. This will prevent double retires.

The rules for statements are given in Figure 6b. Rule (INFERR) allows for type transformations at any point, in particular to establish the proper pre/post environments for the Rules (CHOICE) and (LOOP). Entering an atomic block, Rule (BEGIN), has no effect on the type environment. Exiting an atomic block allows for interference. Hence, Rule (EXIT) removes any type information from the type environment that can be tampered with by other threads. Sequences of statements are straightforward, Rule (SEQ). Choices require a common pre and post type environment, Rule (CHOICE). Loops require a type environment that is stable under the loop body, Rule (LOOP).

### 5.4 Soundness

Our goal is to show that a successful type check \( \vdash stmt \) implies pointer race freedom and the absence of double retires. There are two challenges. We already commented on the problematic sequential to concurrent lifting that motivated the definition of interference freedom. The second difficulty is that the type system relies on the program’s invariant annotations. The set of computations ignores these annotations. To reconcile the assumptions about the program, we have to prove the invariant annotations correct. Interestingly, we can use garbage collection for this purpose, meaning the invariant annotations only have to hold in \( \mathcal{P}_{\text{addr}} \), although the following results refer to the computations in \( \mathcal{P}_{\text{addr}}^O \). Intuitively, garbage collection is sufficient because we have elision support (cf. Section 3): it allows us to remove frees from a computation and then apply Lemma 3.1.

Pointer race freedom and the absence of double retires will be consequences of a more general soundness result that makes explicit the information tracked by our type system. We write \( P \vdash \{ \text{stmt} \} \Gamma \) to the semantic soundness relation \( \vdash \) to the semantic soundness relation \( \vdash \).

**Theorem 5.1 (Soundness).** If \( \text{inv}(\mathcal{P}_{\text{addr}}^O) \), then \( \vdash \{ \text{stmt} \} \Gamma \) implies \( \vdash \{ \text{stmt} \} \Gamma \).

**Proof Sketch.** We proceed by induction on the length of computations \( \tau \) from \( \mathcal{P}_{\text{addr}}^O \). During the proof, we need to access the types encountered by thread \( t \) along the execution of stmt. To make them explicit, we define the straight-line version \( stmt(\tau, t) \) of stmt induced by \( \tau \) and \( t \). It is
obtained by projecting \( \tau \) to the commands of thread \( t \). One can show that if we can derive a typing for the program then we can derive it for the induced straight-line program:

\[
\vdash \{ \Gamma_{\text{init}} \} \ \text{stmt} \ \{ \Gamma \} \quad \text{implies} \quad \vdash \{ \Gamma_{\text{init}} \} \ \text{stmt}(\tau, t) \ \{ \Gamma \}.
\]

The implication should be intuitive. The typing of the overall program can be seen as an intersection over the typings of the induced straight-line programs.

The induction hypothesis links the current type environment \( \Gamma \) derived for the straight-line program to the semantic information carried by the computation. The hypothesis strengthens the requirements (i) and (ii) in the definition of soundness by the following two conditions, where we assume \( \Gamma(x) = T \). (iii) If \( L \in T \), then \( x \) is a pointer that does not have valid aliases. That is, \( m_\tau(x) = m_\tau(q) \) implies \( q \notin \text{valid}_\tau \). Note that angels cannot obtain \( L \) according to the type rules. (iv) If \( A \in T \), then thread \( t \) is in an atomic block. The interesting argumentation in the induction step is in the case when another thread appends an action, \( \tau \cdot \text{act} \). It can be summarized as follows.

Property (i) continues to hold for \( \tau \cdot \text{act} \) because the type \( T \) of \( x \) is closed under interference; for \( L \) and \( A \) we argue separately in the following. If \( L \in T \), then \( \text{act} \) cannot use a valid alias of \( x \). In particular, it cannot retire \( x \) according to the premise of Rule (enter). If \( A \in T \), then thread \( t \) is in an atomic block and there is no chance to append action \( \text{act} \) of another thread. The case does not occur. Consider property (ii). Assume \( \text{isValid}(T) \) holds. That is, \( T \) contains one of \( A, L, S \). If \( L \in T \) or \( A \in T \), then the above reasoning for (i) already implies (ii). Otherwise, we have \( S \in T \). It implies (ii) because \( S \) is closed under interference. Property (iii) follows from the fact that \( \text{act} \) cannot contain, and thus cannot create, a valid alias of \( x \). Lastly, to conclude property (iv), note that another thread cannot append an action while \( t \) is inside an atomic block.

The first consequence of soundness is that a successful type check implies pointer race freedom. Phrased differently, the rules from Figure 6 allow for a successful typing only if there are no pointer races. That is, our type system performs a pointer race freedom check indeed.

**Proposition 5.2.** If \( \text{inv}(\{P\}^\circ_{\text{Adr}}) \), then \( \vdash P \) implies that \( O\{P\}^\circ_{\text{Adr}} \) is pointer-race-free.

The proposition gives an effective means of checking the premise of Theorem 4.1: determine a typing using the proposed type system (cf. Section 7) and discharge the invariant annotations using an off-the-shelf verification tool (cf. Section 8).

**Proof Sketch.** To see the proposition, consider \( \tau \cdot \text{act} \in O\{P\}^\circ_{\text{Adr}} \). We focus on the case where the last action is a dereference, say due to command \( \text{com} \) being \( p := q.\text{next} \). The remaining cases in the definition of pointer races are similar. We show that the dereference is safe, \( q \in \text{valid}_\tau \).

Let thread \( t \) perform the dereference. Let \( \text{stmt}(\tau \cdot \text{act}, t) = \text{stmt}; \text{com} \) be the induced straight-line program. As observed above, since the program type checks also \( \text{stmt}; \text{com} \) will type check. Say we can derive \( \{ \Gamma_{\text{init}} \} \ \text{stmt}; \ \text{com} \ \{ \Gamma \} \). The only way to type a composition \( \text{stmt}; \text{com} \) is Rule (seq). It requires an environment \( \Gamma' \) so that \( \{ \Gamma_{\text{init}} \} \ \text{stmt} \ \{ \Gamma' \} \) and \( \{ \Gamma' \} \ \text{com} \ \{ \Gamma \} \) are derivable. The only way to type an assignment \( p := q.\text{next} \) is Rule (assign2). By its premise, \( \Gamma'(q) = T \) with \( \text{isValid}(T) \). Theorem 5.1 yields \( q \in \text{valid}_\tau \). The dereference of \( q \) is safe. \( \square \)

The second consequence of soundness is that a successful type check means the program does not perform double retires. This is the precondition for a meaningful application of \( O_{\text{Base}} \) (cf. Section 3).

**Proposition 5.3.** If \( \text{inv}(\{P\}^\circ_{\text{Adr}}) \), then \( \vdash P \) implies that \( O\{P\}^\circ_{\text{Adr}} \) does not perform double retires.

The argumentation is along the lines of Proposition 5.2. To perform a retire, Rule (enter) requires the pointer to be active. This, in turn, means \( O_{\text{Base}} \) is in state \( L_2 \). The state, however, can only be reached if there were no earlier retires of the address or the earlier retires have been followed by a free. In both cases, we do not have a double retire.
The next section gives an in-depth example on how to apply our type system. The two sections thereafter automate the checks in Theorem 5.1: we give an efficient algorithm for type inference \( \vdash P \) and show how to discharge the invariants \( \text{inv}(\llbracket P \rrbracket_\Theta) \) with the help of off-the-shelf verification tools.

6 EXAMPLE

We apply our type system to Michael&Scott’s queue with EBR from Section 2. Here, a single custom guarantee \( E_{\text{acc}} \) is sufficient. We define \( \text{Loc}(E_{\text{acc}}) \) to be those locations where thread \( z_t \) is guarantee to have returned from a call to \( \text{leaveQ} \) but has not yet invoked \( \text{enterQ} \). That is, \( E_{\text{acc}} \) captures when \( z_t \) is accessing the data structure. The sets of locations represented by \( A, S, \) and \( E_{\text{acc}} \) can be read of the cross-product SMR automaton \( O_{\text{Base}} \times O_{\text{EBR}} \) in Figure 7. It is worth pointing out that \( \text{Loc}(S) \) does not contain location \((L_2, L_4)\). For a set containing \((L_2, L_4)\) to be closed under interference we would need to have \((L_3, L_4)\) in that set. However, \((L_3, L_4)\) allows for a \( \text{free} \) of \( z_a \) and thus must not belong to \( \text{Loc}(S) \) by definition.

In the following, we illustrate the type transformer relation, the use of angels, the typing of programs, and explain how to find suitable annotations for the type inference to go through.

6.1 Type Transformer Relation

We illustrate the computation of the type transformer relation for \( \text{exitQ} \text{leaveQ} \) and the inference of \( \mathcal{S} \).

First, we establish the type transformer relation \( \llbracket \mathcal{S} \rrbracket_{\mathcal{X} \mathcal{Y}} \). This boils down to checking \( \text{post}_{x, \text{exitQ}}(\text{Loc}(\mathcal{S})) \subseteq \text{Loc}(E_{\text{acc}}) \) because the remaining properties of the type transformer relation are trivially satisfied (we do not add any of \( \{A, L, S\} \)). The empty type corresponds to no knowledge about previously executed SMR commands, which means \( \text{Loc}(\mathcal{S}) = L \) with \( L \) the set of all locations of \( O_{\text{Base}} \times O_{\text{EBR}} \). We compute the post-image of \( L \) wrt. \( x \) and \( \text{exitQ} \text{leaveQ} \) in the SMR automaton from Figure 7. To this end, we consider all transitions labeled with \( \text{exitQ}(t) \). The pointer or angel \( x \) does not play a role. We derive the desired inclusion as follows:

\[
\text{post}_{x, \text{exitQ}}(\text{Loc}(\mathcal{S})) = \text{post}_{x, \text{exitQ}}(L) = L \setminus \{(L_2, L_4), (L_3, L_4)\} = \text{Loc}(E_{\text{acc}}).
\]
Second, we show how to infer $S$. From Figure 7 we know that $E_{acc}$ alone does not yield $S$ because of location $(L_3, L_5)$; we also need $A$. We establish $E_{acc} \land A \rightsquigarrow E_{acc} \land A \land S$. Since $E_{acc} \land A$ is valid and we do not add $L$, the key task is to establish $\text{Loc}(E_{acc} \land A) \subseteq \text{Loc}(E_{acc} \land A \land S)$. As $\text{Loc}(E_{acc} \land A) \subseteq \text{Loc}(E_{acc} \land A)$ trivially holds, it suffices to show $\text{Loc}(E_{acc} \land A) \subseteq \text{Loc}(S)$:

$$\text{Loc}(E_{acc} \land A) = \text{Loc}(E_{acc}) \cap \text{Loc}(A) = \{(L_2, L_5), L_8\} \subseteq \{(L_2, L_5), (L_3, L_6), L_8\} = \text{Loc}(S).$$

### 6.2 Angels

To illustrate the use of angels, consider the excerpt of the dequeue operation depicted in Figure 8. Note that calls to SMR functions lead to two consecutive commands. The atomic block ensures the commands are executed without interruption by other threads. To infer it, we rely on standard moverness arguments [Lipton 1975]: command $\text{enter leaveQ()}$ is a right-mover because it does not affect the memory nor the observer $O_{Base} \times O_{ERR}$. The call to $\text{leaveQ}$ guarantees that no currently active address is reclaimed until $\text{enterQ}$ is called. It thus protects an unbounded number of addresses before a thread acquires a pointer to them. Later, when a thread acquired a pointer to such an address in order to access it, the address may no longer be active and thus the type system may not be able to infer $S$ (cf. Section 6.1). To overcome this problem, we use an angel $r$. Given its angelic semantics, $r$ will capture all addresses that are protected by the $\text{leaveQ}$ call, Lines 73 to 77. Later, upon accessing/dereferencing a pointer $p$, we make sure that $r$ captures the address pointed to by $p$, Lines 82 and 85.

### 6.3 Typing

We give a typing for the code from Figure 8 in Figure 9. We start in Line 91 with type $\emptyset$ for all pointers and the angel $r$. The allocation of $r$ in Line 92 has no effect on the type assignment. The same holds when entering an atomic block, Line 94. Line 96 invokes $\text{leaveQ}$. Again, the types are not affected because the SMR automaton has no transitions labeled with $\text{enter leaveQ}$. Next, the invocation returns, Line 98. Following the discussion from Section 6.1, we obtain $E_{acc}$ for $r$, Line 99. It is worth pointing out that $r$ is treated like an ordinary pointer when it comes to the type transformer relation.

To capture in the type system the set of addresses that can be safely accessed in the subsequent code, we want to lift $E_{acc}$ of $r$ to $S$. We annotate $r$ to hold a set of active addresses, Line 100. This yields type $E_{acc} \land A$ for $r$, Line 101. As explained above, we can now lift this type to $E_{acc} \land A \land S$, Line 102. Recall that the allocation of $r$ in Line 92 is angelic. That is, the addresses held by $r$ will indeed be chosen to be active.

In the subsequent code, we already added annotations (cf. Section 6.2) ensuring that accessed/dereferenced pointers are captured by the angel $r$. For instance, Line 112 requires the address of $\text{head}$ to be captured by $r$. That this is the case indeed is established when the annotations are discharged. For the typing, we can copy $E_{acc} \land S$ from $r$ over to $\text{head}$. As a consequence, the dereference of $\text{head}$ in Line 114 is safe. Similarly, we require $\text{next}$ to be captured by $r$ in Line 117 such that the dereference in Line 119 is safe.

---

Fig. 8. Excerpt of dequeue using angel $r$.
6.4 Annotations

We explain our algorithm to automatically add to the program in Figure 2 the annotations in Figure 8 in order to arrive at the typing in Figure 9. We focus on the dereference of head in Line 83. Without annotations, the type inference will fail because it cannot conclude that head is guaranteed to be valid. To fix this, we implemented a sequence of tactics that we invoke one after the other. If none of them fixes the issue, we give up the type inference and report the failure to the user.

The first tactic simply adds an \( @\text{inv active}(\text{head}) \) annotation to Line 83. This makes head valid and the type inference go through for Line 83. However, we should only add the annotation if it actually holds. To check this, we employ the technique from Section 8. In this particular case, we will find that the annotation does not hold; so we try to fix the problem with another tactic.

The second tactic adds an angel \( r \) to the (syntactically) most recent \( \text{leaveQ} \) call. We use a template to transform the sequence \( \text{enter leaveQ}(); \text{exit leaveQ}; \) to the code from Lines 73-78. (A subsequent use of this tactic will skip this step and reuse the existing angel.) Then, we fix Line 83 by adding the annotation \( @\text{inv head in } r \) before it, as shown in Line 82. This makes head valid. Whether the annotation holds is again checked with the technique from Section 8.

It is worth pointing out that the second tactic is EBR-specific. From our experience, every SMR algorithm/automaton comes with a small set of tactics that significantly help finding the right annotations—EBR requires the above tactic and HP requires two specific tactics. We do not believe that there is a silver bullet of tactics since SMR algorithms may vary greatly, as seen in the cases of EBR and HP. Theoretically speaking, one could find the annotations by an exhaustive search (finitely many angels will suffice), but this will not scale.

6.5 Hazard Pointers

Our approach applies to lock-free data structures with hazard pointers just as well as in the case of EBR. The main difference is that HP typically does not require angels because pointers are protected after they are acquired. However, the size of the SMR automaton for HP grows in the number of hazard pointers. For two hazard pointers it consists of 17 locations. Consider Appendix A for details.
7 TYPE INFERENCE

We show that type inference is surprisingly efficient, namely quadratic time.

**Theorem 7.1.** Given a program stmt, the type inference ⊢ stmt is computable in time $O(|stmt|^2)$.

As common in type systems [Pierce 2002], our algorithm for type inference is constraint-based. We associate with the program stmt a constraint system $\Phi(\Gamma_{init}, stmt, X)$. The variables $X$ are interpreted over the set of type environments enriched with a value $\top$ for a failed type inference. The correspondence between solving the constraint system and type inference will be the following. An environment $\Gamma$ can be assigned to $X$ in order to solve the constraint system if and only if $\{\Gamma_{init}\} stmt \{\Gamma\}$. As a consequence, a non-trivial solution to $X$ will show $\vdash stmt$.

Our type inference algorithm will be a fixed-point computation. The canonical choice for a domain over which to compute would be the set of types ordered by $\sim$. The problem is that types of the form $B_{L}$ and $B_{L} \land B_{L'}$ with $L \subseteq L'$ are comparable, $B_{L} \sim B_{L} \land B_{L'}$ and $B_{L} \land B_{L'} \sim B_{L}$. This is not merely a theoretical issue of the domain being a quasi instead of a partial order. It means we compute over too large a domain, namely a powerset lattice where we should have used a lattice of antichains [Wulf et al. 2006]. We factorize the set of all types along such equivalences $\sim \cap \sim^{-1}$. The resulting $\text{AntiChainTypes} := (\text{Types}/\sim \cap \sim^{-1}, \sim)$ is a complete lattice [Birkhoff 1948].

Type environments can be understood as total functions into this antichain lattice. We enrich the set of functions by a value $\top$. The problem is that types are not merely a theoretical issue of the domain being a quasi instead of a partial order. It means we compute over too large a domain, namely a powerset lattice where we should have used a lattice of antichains [Wulf et al. 2006]. We factorize the set of all types along such equivalences $\sim \cap \sim^{-1}$. The resulting $\text{AntiChainTypes} := (\text{Types}/\sim \cap \sim^{-1}, \sim)$ is a complete lattice [Birkhoff 1948].

Type environments can be understood as total functions into this antichain lattice. We enrich the set of functions by a value $\top$ to indicate a failed type inference. The result is the complete lattice of enriched type environments

\[
\text{Envs}_\top := (\text{AntiChainTypes}_{\text{Vars}} \cup \{\top\}, \sqsubseteq) .
\]

Between environments, we define $\Gamma \sqsubseteq \Gamma'$ to hold if for all $x \in \text{Vars}$ we have $\Gamma(x) \sim \Gamma'(x)$. This lifts $\sim$ to the function domain. Value $\top$ is defined to be the largest element.

The constraint system $\Phi(\Gamma_{init}, stmt, X)$ is defined in Figure 10. We proceed by induction over the structure of statements and maintain triples $(X, stmt, Y)$. The idea is that statement $stmt$ will turn the enriched type environment stored in variable $X$ into an environment upper bounded by $Y$. Consider the case of basic commands. We will define $sp(X, com)$ to be the strongest enriched type environment resulting from the environment in $X$ when applying command $com$. The constraint $sp(X, com) \sqsubseteq Y$ requires $Y$ to be an upper bound. Note that $Y$ still contains safe type information. For a sequential composition, we introduce a fresh variable $Z$ for the enriched type environment determined by $stmt_1$ from $X$. We then require $stmt_2$ to transform this environment into $Y$. For a choice, $Y$ should upper bound the effects of both $stmt_1$ and $stmt_2$ on $X$. This guarantees that the type information is valid independent of which branch is chosen. For iterations, we have to make sure $Y$ is an upper bound for the effect of arbitrarily many applications of $stmt$ to $X$. This means the environment in $Y$ is at least $X$ because the iteration may be skipped. Moreover, if we apply $stmt$ to $Y$ then we should again obtain at most the environment in $Y$.

It remains to define $sp(X, com)$, the strongest enriched type environment resulting from $X$ under command $com$. We refer to the typing rules in Figure 6 and extract $pre_{com}$ and $up_{com}$. The former

| $\Phi(X, com, Y)$ | $sp(X, com) \sqsubseteq Y$ |
|-------------------|---------------------------|
| $\Phi(X, stmt_1; stmt_2, Y)$ | $\Phi(X, stmt_1, Z) \land \Phi(Z, stmt_2, Y)$, $Z$ fresh |
| $\Phi(X, stmt_1 \oplus stmt_2, Y)$ | $\Phi(X, stmt_1, Y) \land \Phi(X, stmt_2, Y)$ |
| $\Phi(X, stmt^*, Y)$ | $\Phi(Y, stmt, Y) \land X \sqsubseteq Y$ |

Fig. 10. Constraint system $\Phi(X, stmt, Y)$. |
is a predicate on environments capturing the premise of the rule associate with command \textit{com}. To give an example, for Rule (\textsc{assign2}) the predicate \textit{pre}_{com}(\Gamma) \) is \textit{isValid}(T) with \( T = \Gamma(q) \). The latter is a function on environments. It captures the update of the given environment as defined in the consequence of the corresponding rule. For (\textsc{assign2}), the update \textit{up}_{com}(\Gamma) is \( \Gamma[p \mapsto \emptyset] \). The strongest enriched environment preserves the information that a type inference has failed, \( sp(\top, com) := \top \), for all commands. For a given environment, we set

\[
sp(\Gamma, com) := \text{pre}_{com}(\Gamma) \ ? \ up_{com}(\Gamma) : \top.
\]

We evaluate the premise of the rule. If it does not hold, the type inference will fail and return \( \top \). Otherwise, we determine the update of the current type environment, \( up_{com}(\Gamma) \). We rely on the fact that \( sp(\cdot, com) \) is monotonic and hence (as the domains are finite) continuous.

We apply a Kleene iteration to obtain the least solution to the constraint system \( \Phi(\Gamma_{\text{init}}, \text{stmt}, X) \). The least solution is a function \textit{lsol} that assigns to each variable in the system an enriched type environment. We focus on variable \( X \) that captures the effect of the overall program on the initial type environment. Then \( \textit{lsol}(X) \) is the strongest type environment that can be obtained by a successful type inference. This is the key correspondence.

**Proposition 7.2 (Principle Types).** Consider \( \Phi(\Gamma_{\text{init}}, \text{stmt}, X) \). Then \( \textit{lsol}(X) = \bigcap_{\Gamma} \text{lsol}(\Gamma) \). Hence, \( \textit{lsol}(X) \neq \top \) if and only if \( \vdash \text{stmt} \).

It remains to check the complexity of the Kleene iteration. In the lattice of enriched type environments, chains have length at most \( |\text{Var}| \cdot |\{A, L, S, E_1, \ldots, E_n\}| + 1 \). This is linear in the size of the program as the guarantees only depend on the SMR algorithm, which is not part of the input. With one variable for each program point, also the number of variables in the constraint system is linear in the size of the program. It remains to compute \( sp(\cdot, com) \) for the Kleene approximants. This can be done in constant time. The premise and the update of a rule only modify a constant number of variables. Moreover, we can look-up the effect of commands on a type in constant time. Combined, we obtain the overall quadratic complexity.

**8 INVARIANT CHECKING**

The type system from Section 5 relies on invariant annotations in the program under scrutiny in order to incorporate runtime behavior that is typically not available to a type system. For the soundness of our approach, we require those annotations to be correct. Recall from Section 5 that the annotations need only hold in the garbage collected (GC) semantics. We now show how to use an of-the-shelf GC verifier to discharge the invariant annotations fully automatically. In our experiments, we rely on \textit{cave} [Vafeiadis 2009, 2010a,b].

Making the link to tools is non-trivial. Our programs feature programming constructs that are typically not available in off-the-shelf verifiers. We present a source-to-source translation that replaces those constructs by standard ones. The constructs to be replaced are SMR commands, invariants guaranteeing pointers to be active (not retired), and invariants centered around angels. For the translation, we only rely on ordinary assertions \textit{assert cond} and non-deterministic assignments \textit{havoc}(\textit{p}) to pointers. Both are usually available in verification tools.

The correspondence between the original program \( P \) and its translation \( \text{inst}(P) \) is documented in Theorem 8.1 and as required. Predicate \textit{safe}(-\text{-}) evaluates to true iff the assertions hold, i.e., verification is successful. Recall that \( \llbracket P \rrbracket_{\odot}^{\odot} \) is the GC semantics where addresses are neither freed nor reclaimed. Note that this semantics is the weakest a tool can assume. Our instrumentation also works if the GC tool collects and subsequently reuses garbage nodes.

**Theorem 8.1 (Soundness and Completeness).** We have \( \text{inv}(\llbracket P \rrbracket_{\odot}^{\odot}) \iff \text{safe}(\llbracket \text{inst}(P) \rrbracket_{\odot}^{\odot}) \). The source-to-source translation is linear in size.
we let verification fail. Note that we can derive the facts in arbitrary order.

This resembles the idea of having a strategy to win against an opponent in a turn-based game, a common phenomenon when quantifier alternation is involved [Grädel et al. 2002]. Another source of difficulty is the fact that angels are second-order variables storing sets. We tackle the problem by guessing an element in the set for which verification fails.

The instrumentation proceeds as follows. We consider angels $r$ to be ordinary pointers. For each angel, we add two Boolean variables $\text{included}_r$ and $\text{failed}_r$ that are local to the thread. When we allocate an angel using $\text{@inv angel } r$, we guess the address that (i) will inevitably belong to the set of addresses held by the angel and (ii) for which an active invariant will fail. To document that we are sure of (i), we raise flag $\text{included}_r$. For (ii), we use $\text{failed}_r$. If we are sure of both facts, we let verification fail. Note that we can derive the facts in arbitrary order.

The source-to-source translation is defined in Figure 11. It preserves the structure of the program and does not modify ordinary commands. SMR calls and returns will be taken care of by the type system. They are ignored, except for retire. Invariants guaranteeing pointer equality yield assertions.

The purpose of invariants $\text{@inv active}(p)$ is to guarantee that the address held by the pointer has not been retired since its last allocation. The idea of our translation is to guess the moment of failure, the retire function after which such an invariant will be checked. We instrument the program by an additional pointer $\text{retire_ptr}$ and a Boolean variable $\text{retire_flag}$. Both are shared. A retire translates into a non-deterministic choice between skipping the command or being the retire after which an invariant will fail. In the latter case, the address is stored in $\text{retire_ptr}$ but the flag has not yet been raised. Note that the instrumentation is tailored towards garbage collection. As long as $\text{retire_ptr}$ points to the address, it will not be reallocated. Therefore, we do not run the risk of the address becoming active ever again. The invariant $\text{@inv active}(p)$ now translates into an assertion that checks the address of $p$ for being the retired one and the flag for being raised. A thing to note is that the instrumentation of the retire function is not atomic. Hence, there may be an interleaving where a pointer has been stored in $\text{retire_ptr}$ but the flag has not yet been raised. The assertion would consider this interleaving safe. However, if there is such an interleaving, there is also one where the assertion fails. Hence, atomicity is not needed.

For invariants involving angels, the idea of the instrumentation is the same as for pointers, guessing the moment of failure. What makes the task more difficult is the angelic semantics. We cannot just guess a value for the angel and show that it makes an invariant fail. Instead, we have to show that, no matter how the value is chosen, it inevitably leads to an invariant failure. This resembles the idea of having a strategy to win against an opponent in a turn-based game, a common phenomenon when quantifier alternation is involved [Grädel et al. 2002]. Another source of difficulty is the fact that angels are second-order variables storing sets. We tackle the problem by guessing an element in the set for which verification fails.

The source-to-source translation is defined in Figure 11. It preserves the structure of the program and does not modify ordinary commands. SMR calls and returns will be taken care of by the type system. They are ignored, except for retire. Invariants guaranteeing pointer equality yield assertions.

| $\text{inst}(\text{stmt}^*)$ | $\text{inst(enter func}(p, \bar{u}))$ | $\text{inst(enter retire}(q))$ | $\text{inst(on ret}(\text{inv active}(p))$ | $\text{inst(on ret}(\text{inv active}(r))$ |
|-----------------------------|---------------------------------|-------------------------------|---------------------------------|---------------------------------|
| $\text{inst( stmt)}^*$     | $\text{inst( stmt)}^*$         | $\text{skip}$              | $\text{assert !retire_flag}$    | $\text{assert !failed_}$       |
| $\text{inst( stmt}_1 \oplus \text{ stmt}_2$ | $\text{inst( stmt}_1 \oplus \text{ stmt}_2$ | $\text{skip}$              | $\text{false}$                | $\text{true}$                |
| $\text{inst( stmt}_1; \text{ stmt}_2$ | $\text{inst( stmt}_1; \text{ stmt}_2$ | $\text{inst( exit func)$}   | $\text{false}$                | $\text{true}$                |
| $\text{inst(com)} := \text{com}$ | $\text{inst( enter retire}(q)) := \text{ skip \oplus (retire_{p} := q; retire_{flag} := true)$ | $\text{assert !retire_{flag} \lor \ \text{retire_{p} \neq p}$ | $\text{assume \ q = r; assert !failed_{r}; included_{r} := true$ | $\text{assume retire_{flag} \land retire_{p} = r; assert !included_{r}; failed_{r} := true$ |

Fig. 11. Source-to-source translation replacing SMR commands and invariant annotations.
An invariant \( @\text{inv} \ q \ \text{in} \ r \) forces the angel to contain the address of \( q \). This may establish (i). The reason it does not establish (i) for sure is that the angel denotes a set of addresses, and the address of \( q \) could be different from the one for which an active invariant fails. Hence, we non-deterministically choose between skipping the invariant or comparing \( q \) to \( r \). If the comparison succeeds, we raise \( \text{included}_r \). Moreover, we check (ii). If the address has been retired, we report a bug.

Invariant \( @\text{inv} \ \text{active}(r) \) forces all addresses held by the angel to be active. In the instrumented program, \( r \) is a pointer that we compare to \( \text{retire}_\text{ptr} \) introduced above. If the address has been retired, we are sure about (ii) and document this by raising \( \text{failed}_r \). If we already know (i), the address inevitably belongs to the set held by the angel, verification fails.

9 EVALUATION

We implemented our approach in a C++ tool called \text{seal} \(^3\). As stated before, we use the state-of-the-art tool \text{cave} \cite{Vafeiadis2009, Vafeiadis2010a, Vafeiadis2010b} as a back-end verifier for discharging annotations and checking linearizability. For the type inference, our tool computes the most precise guarantees \( E_L \) on-the-fly; there is no need for the user to manually specify them. To substantiate the claim of usefulness of our approach, we evaluated \text{seal} on examples from the literature. We considered the following data structures: Treiber’s stack \cite{Michael2002b, Treiber1986}, Michael&Scott’s lock-free queue \cite{Michael2002b, Michael1996}, the DGLM queue \cite{Doherty2004}, the Vechev&Yahav CAS set \cite{Vechev2008}, the Vechev&Yahav DCAS set \cite{Vechev2008}, the ORVYY set \cite{O’Hearn2010}, and Michael’s set \cite{Michael2002a}. Our benchmarks include a version of each data structure for hazard pointers (HP) \cite{Michael2002b} and epoch-based reclamation (EBR) \cite{Fraser2004}. We adapted the GC implementations of the Vechev&Yahav DCAS set, the Vechev&Yahav CAS set, and the ORVYY set given in the literature to use HP/EBR.

Our findings are listed in Table 1. The experiments were conducted on an Intel i5-8600K@3.6GHz with 16GB of RAM. The table includes the time taken (i) for the type inference, (ii) for discharging the invariant annotations, and (iii) to check linearizability. We mark tasks with ✓ if they were successful, with ✗ if they failed, and with ☐ if they timed out after 12h wall time.

Our approach is capable of verifying most of the lock-free data structures we considered. Comparing the total runtime with our competitors \cite{Meyer2019}, the only other approach capable of handling lock-free data structures with general SMR algorithms, we experience a speed-up of over two orders of magnitude on examples like Michael&Scott’s queue. Besides the speed-up, we are the first to automatically verify lock-free set algorithms that use SMR.

We were not able to discharge the annotations of the DGLM queue and Michael’s set. Imprecision in the thread-modular abstraction of our back-end verifier resulted in false-positives being reported. Hence, we cannot guarantee the soundness of our analysis in these cases. This is no limitation of our approach, it is a shortcoming of the back-end verifier. \cite{Meyer2019} reported a similar issue that they solved by manually providing hints to improve the precision of their analysis.

The annotation checks for set implementations are interesting. While the HP version of an implementation is typically more involved than the corresponding version using EBR, the annotation checks for the HP version are more efficient. The reason for this could be that EBR implementations require angels. The conjecture suggests that discharging angels is harder for \text{cave} than discharging active annotations although our instrumentation uses the same idea for both annotation types.

For the benchmarks from Table 1 we preprocessed the implementations by applying mover types \cite{Lipton1975}, a well-known program transformation (cf. Section 10). Intuitively, a command is a mover if it can be reordered with commands of other threads. This allows for the command to be moved to the next command of the same thread, effectively constructing an atomic block.

\(^3\)Available at: https://wolff09.github.io/seal/
containing the mover and the next command. What is remarkable in our setting is that SMR commands (enter, exit, free) always move over ordinary memory commands, and vice versa. (Technically, this requires enter commands to contain only thread-local variables, a property than can be checked/established easily.) As a result, we can find movers for memory commands using existing techniques. For SMR commands, movers can be read of the SMR automaton. Our tool is able to find and apply movers. Due to space constraints, we omit a thorough discussion of the matter.

## 10 RELATED WORK

**Safe Memory Reclamation.** Besides EBR and HP there is another basic SMR technique: reference counting (RC). RC extends records with an integer field counting the number of pointers to the record. Safely modifying counters in a lock-free manner, however, requires hazard pointers [Herlihy et al. 2005] or a mostly unavailable CAS for two arbitrary memory locations [Detlefs et al. 2001].

Recent efforts in developing SMR algorithms have mostly combined existing SMR techniques. For example, DEBRA [Brown 2015] is an optimized EBR implementation. Harris [2001] modifies EBR to store epochs inside records. Hyaline [Nikolaev and Ravindran 2019] is used like EBR. Optimized HP implementations include the work by Aghazadeh et al. [2014], the work by Dice et al. [2016], and Cadence [Balmau et al. 2016]. Dynamic Collect [Dragojevic et al. 2011], StackTrack [Alistarh et al. 2014], and ThreadScan [Alistarh et al. 2015] are HP-esque implementations exploring the use of operating system and hardware support. Drop the Anchor [Braginsky et al. 2013], Optimistic Access [Cohen and Petrank 2015b], Automatic Optimistic Access [Cohen and Petrank 2015a], QSense [Balmau et al. 2016], Hazard Eras [Ramalhete and Correia 2017], and Interval-based Reclamation [Wen et al. 2018] combine EBR and HP. Free Access [Cohen 2018] automates the application of Automatic Optimistic Access. While the method promises to be correct by construction, we believe

### Table 1. Experimental results for verifying singly-linked data structures using safe memory reclamation.
The experiments were conducted on an Intel i5-8600K@3.6GHz with 16GB of RAM.

| SMR | Program                  | Type Inference | Annotations | Linearizability |
|-----|--------------------------|----------------|-------------|-----------------|
| HP  | Treiber’s stack          | 0.7s ✓         | 12s ✓       | 1s ✓            |
|     | Opt. Treiber’s stack     | 0.5s ✓         | 11s ✓       | 1s ✓            |
|     | Michael&Scott’s queue    | 0.6s ✓         | 12s ✓       | 4s ✓            |
|     | DGLM queue               | 0.6s ✓ 1s ✓    | 5s ✓        |
|     | Vechev&Yahav DCAS set    | 1.2s ✓         | 13s ✓       | 98s ✓           |
|     | Vechev&Yahav CAS set     | 1.2s ✓ 3.5h ✓  | 42m ✓       |
|     | ORVYY set                | 1.2s ✓ 3.2h ✓  | 47m ✓       |
|     | Michael’s set            | 1.2s ✓ 90s ✓   | — ✓         |

| EBR | Treiber’s stack          | 0.6s ✓         | 10s ✓       | 1s ✓            |
|     | Michael&Scott’s queue    | 0.7s ✓         | 16s ✓       | 5s ✓            |
|     | DGLM queue               | 0.7s ✓ 1s ✓    | 6s ✓        |
|     | Vechev&Yahav DCAS set    | 0.8s ✓ 38s ✓   | 200s ✓      |
|     | Vechev&Yahav CAS set     | 0.8s ✓ 7h ✓    | 42m ✓       |
|     | ORVYY set                | 0.9s ✓ 7h ✓    | 47m ✓       |
|     | Michael’s set            | 0.2s ✓ 22s ✓   | — ✓         |

*[a]False-positive due to imprecision in the back-end verifier.*
that performance-critical applications choose the SMR technique based on performance rather than ease of use. The demand for automated verification remains. Beware&Cleanup [Gidenstam et al. 2005] combines HP and RC. Isolde [Yang and Wrigstad 2017] combines EBR and RC. We believe our approach can handle other SMR algorithms besides EBR and HP as well.

**Memory Safety.** We use our type system to show that a program is free from pointer races, meaning that it is memory safe. There are a number of related tools that can check pointer programs for memory safety. For example: a combination of ccured [Necula et al. 2002] and BLAST [Henzinger et al. 2003] due to Beyer et al. [2005], INVADER [Yang et al. 2008], XISA [Laviron et al. 2010], SLAYER [Berdine et al. 2011], INFER [Calcagno and Distefano 2011], FORESTER [Holik et al. 2013], PREDATOR [Dudka et al. 2013; Holik et al. 2016], and APROVE [Ströder et al. 2017]. These tools can only handle sequential code. Moreover, unlike our type system, they include memory/shape abstractions to identify unsafe pointer operations. We delegate this task to a back-end verifier with the help of annotations. That is, if the related tools were to support concurrent programs, they were candidates for the back-end. We used CAVE [Vafeiadis 2010a,b] as it can also prove linearizability.

Despite the differences, we point out that the combination of BLAST and ccured [Beyer et al. 2005] is close to our approach in spirit. ccured performs a type check of the program under scrutiny which checks for unsafe memory operations. While doing so, it annotates pointer operations in the program with run-time checks in case the type check could not establish the operation to be safe. The run-time checks are then discharged using BLAST. The approach is limited to sequential programs. Moreover, we incorporate the behavior of the SMR. Finally, our type system is more lightweight and we discharge the invariants in a simpler semantics without memory deletions.

Castegren and Wrigstad [2017] give a type system that guarantees the absence of data races. Types encode a notion of ownership that prevents non-owning threads from accessing a node. Their method is tailored towards GC and requires to rewrite programs with appropriate type specifiers. Recently, Kuru and Gordon [2019] presented a type system for checking the correct use of RCU. Unlike our approach, they integrate a fixed shape analysis and a fixed RCU specification. This makes the type system considerably more complicated and the type check potentially more expensive. Unfortunately, Kuru and Gordon [2019] did not implement their approach.

Besides memory safety, tools like INVADER, SLAYER, INFER, FORESTER, PREDATOR, and the type system by Kuru and Gordon [2019] discover memory leaks. A successful type check with our type system does not imply the absence of memory leaks. We believe that the outcome of our analysis could help a leak detection tool. For example, by performing a linearizability check to find the abstract data type the data structure under consideration implements. We consider a closer investigation of the matter as future work.

**Typestate.** Typestate [Strom and Yemini 1986] extents an object’s type to carry a notion of state. The methods of an object can be annotated to modify this state and to be available only in a certain state. Existing analyses checking for methods being called only in the appropriate state include [Bierhoff and Aldrich 2007; DeLine and Fähndrich 2004; Fähndrich and DeLine 2002; Fink et al. 2006; Foster et al. 2002]. Our types can be understood as typestates for pointers (and the objects they reference) geared towards SMR. However, whereas an object’s typestate has a global character, our types reflect a thread’s local perception. Das et al. [2002] give a typestate analysis based on symbolic execution to increase precision. Similarly, we increase the applicability of our approach by using annotations that are discharged by a back-end verifier. For a more detailed overview on typestate, refer to [Ancona et al. 2016].

**Program Logics.** There are several program logics for verifying concurrent programs with heap. Examples are: SAGL [Feng et al. 2007], RGSEP [Vafeiadis and Parkinson 2007] (used by CAVE [Vafeiadis
Program logics are conceptually related to our type system. However, such logics integrate further ingredients to successfully verify intricate lock-free data structures [Turon et al. 2014]. Most importantly, they include memory abstractions, like (concurrent) separation logic [Brookes 2004; O’Hearn 2004; O’Hearn et al. 2001; Reynolds 2002], and mechanisms to reason about thread interference, like rely-guarantee [Jones 1983]. This makes them much more complex than our type system. We deliberately avoid incorporating a memory abstraction into our type system to keep it as flexible as possible. Instead, we use annotations to delegate the shape analysis to a back-end verifier, achieving modularity in verifying the data structure and its memory management separately. Moreover, accounting for thread interference in our type system boils down to defining guarantees as closed sets of locations and removing guarantee $A$ upon exiting atomic blocks.

Oftentimes, invariant-based reasoning about interference turns out too restrictive for verification. To overcome this, program logics like caresl [Turon et al. 2013], fcsl [Nanevski et al. 2014], icap [Svendsen and Birkedal 2014], tada [da Rocha Pinto et al. 2014], gps [Turon et al. 2014], and iris [Jung et al. 2015] make use of protocols. A protocol captures possible thread interference, for example, using state transition systems. (Rely-guarantee is a particular instantiation of a protocol [Jung et al. 2015; Turon et al. 2013].) In our approach, SMR automata are protocols that govern memory deletions and protections, that is, describe the influence of SMR-related actions among threads. Our types describe a thread’s local, per-pointer perception of that global protocol.

Besides protocols, recent logics like caresl, tada, and iris integrate reasoning in the spirit of atomicity abstraction/refinement [Dijkstra 1982; Lipton 1975]. Intuitively, they allow the client of a fine-grained module to be verified against a coarse-grained specification of the module. For example, a client of a data structure can be verified against its abstract data type, provided the data structure refines the abstract data type. Following [Meyer and Wolff 2019], we use the same idea wrt. SMR algorithms: we consider SMR automata instead of the actual SMR implementations.

Some program logics can also unveil memory leaks [Bizjak et al. 2019; Gotsman et al. 2013].

**Linearizability.** Linearizability testing [Burckhardt et al. 2010; Cerný et al. 2010; Emmi and Enea 2018; Emmi et al. 2015; Horn and Kroening 2015; Liu et al. 2009, 2013; Lowe 2017; Travkin et al. 2013; Vechev and Yahav 2008; Yang et al. 2017; Zhang 2011] is a bug hunting technique to find non-linearizable executions in large code bases. Since we focus on verification, we do not go into the details of linearizability testing. However, it could be worthwhile to use a linearizability tester instead of a verification back-end in our approach to provide faster feedback during the development process and only use a verifier once the development is considered finished.

Verification techniques for linearizability fall into two categories: manual techniques (including tool-supported but not fully automated techniques) and automatic techniques. Manual approaches require the human checker to have a deep understanding of the proof techniques as well as the program under scrutiny—in our case, this includes a deep understanding of the lock-free data structure as well as the SMR implementation. This may be the reason why many manual proofs do not consider reclamation [Bäumler et al. 2011; Bouajjani et al. 2017; Colvin et al. 2005, 2006; Delbianco et al. 2017; Derrick et al. 2011; Doherty and Moir 2009; Elmas et al. 2010; Groves 2007, 2008; Hemed et al. 2015; Henzinger et al. 2013; Jonsson 2012; Khyzha et al. 2017; Liang and Feng 2013; Liang et al. 2012, 2014; O’Hearn et al. 2010; Schellhorn et al. 2012; Sergey et al. 2015a,b]. There are fewer works that consider reclamation [Dodds et al. 2015; Doherty et al. 2004; Fu et al. 2010; Gotsman et al. 2013; Krishna et al. 2018; Parkinson et al. 2007; Tofan et al. 2011]. (The work by Gotsman et al. [2013] checks memory safety and discovers memory leaks as well.) For a more detailed overview of manual techniques, we refer to the survey by Dongol and Derrick [2015].
The landscape of related work for automated linearizability proofs is similar to its manual counterpart. Most automated approaches ignore memory reclamation, that is, assume a garbage collector [Abdulla et al. 2016; Amit et al. 2007; Berdine et al. 2008; Segalov et al. 2009; Sethi et al. 2013; Vafeiadis 2010a,b; Vechev et al. 2009; Zhu et al. 2015]. When reclamation is not considered, memory abstractions are simpler and more efficient, they can exploit ownership guarantees [Bornat et al. 2005; Boyland 2003] and the resulting thread-local reasoning techniques [O’Hearn et al. 2001; Reynolds 2002]. Few works [Abdulla et al. 2013; Haziza et al. 2016; Holik et al. 2017; Meyer and Wolff 2019] address the challenge of verifying lock-free data structures under manual memory management. Besides Meyer and Wolff [2019], they use hand-crafted semantics that allow for accessing deleted memory. The work by Meyer and Wolff [2019] is the closest related. We build on their programming model and their reduction result as discussed in Sections 3 and 4, respectively. Moreover, we rely to their results for proving an SMR implementation against an SMR automaton.

Moverness. Movers where first introduced by Lipton [1975]. They were later generalized to arbitrary safety properties [Back 1989; Doeppner 1977; Lamport and Schneider 1989]. Movers are a widely applied enabling technique for verification. To ease the verification task, the program is made more atomic without cutting away behavior. Because we use standard moverness arguments, we do not give an extensive overview. Flanagan et al. [2008]; Flanagan and Qadeer [2003] use a type system to find movers in Java programs. The Calvin tool [Flanagan et al. 2005, 2002; Freund and Qadeer 2004] applies movers to establish pre/post conditions of functions in concurrent programs using sequential verifiers. Similarly, QED [Elmas et al. 2009] rewrites concurrent code into sequential code based on movers. These approaches are similar to ours in spirit: they take the verification task to a much simpler semantics. However, movers are not a key aspect of our approach. We employ them only to increase the applicability of our tool in case of benign pointer races. Elmas et al. [2010] extend QED to establish linearizability for simple lock-free data structures. QED is superseded by Civl [Hawblitzel et al. 2015; Kragl and Qadeer 2018]. Civl proves programs correct by repeatedly applying movers to a program until its specification is obtained. The approach is semi-automatic, it takes as input a so-called layered program that contains intermediary steps guiding the transformation [Kragl and Qadeer 2018]. Movers were also applied in the context of relaxed memory [Bouajjani et al. 2018].

ACKNOWLEDGMENTS
We thank the POPL’20 reviewers for their valuable feedback and suggestions for improvements.

REFERENCES
Abdulla, P. A.; Haziza, F.; Holik, L.; Jonsson, B.; and Rezine, A. 2013. An Integrated Specification and Verification Technique for Highly Concurrent Data Structures. In TACAS (LNCS), Vol. 7795. Springer, 324–338. https://doi.org/10.1007/978-3-642-36742-7_23
Abdulla, P. A.; Jonsson, B.; and Trinh, C. Q. 2016. Automated Verification of Linearization Policies. In SAS (LNCS), Vol. 9837. Springer, 61–83. https://doi.org/10.1007/978-3-662-53413-7_4
Aghazadeh, Z.; Golab, W. M.; and Woelfel, P. 2014. Making Objects Writable. In PODC. ACM, 385–395. https://doi.org/10.1145/2611462.2611483
Alistarh, D.; Eugster, P.; Herlihy, M.; Matveev, A.; and Shavit, N. 2014. StackTrack: An Automated Transactional Approach to Concurrent Memory Reclamation. In EuroSys. ACM, 25:1–25:14. https://doi.org/10.1145/2592798.2592808
Alistarh, D.; Leiserson, W. M.; Matveev, A.; and Shavit, N. 2015. ThreadScan: Automatic and Scalable Memory Reclamation. In SPAA. ACM, 123–132. https://doi.org/10.1145/2755573.2755600
Amit, D.; Rinetsky, N.; Reps, T. W.; Sagiv, M.; and Yahav, E. 2007. Comparison Under Abstraction for Verifying Linearizability. In CAV (LNCS), Vol. 4590. Springer, 477–490. https://doi.org/10.1007/978-3-540-73368-3_49
Ancon, D.; Bono, V.; Bravetti, M.; Campos, J.; Castagna, G.; Denielou, P.; Gay, S. J.; Gesbert, N.; Giachino, E.; Hu, R.; Johnsen, E. B.; Martins, F.; Mascardi, V.; Montesi, F.; Neykova, R.; Ng, N.; Padovani, L.; Vasconcelos, V. T.; and Yoshida, N. 2016.
Behavioral Types in Programming Languages. Foundations and Trends in Programming Languages 3, 2-3 (2016), 95–230. https://doi.org/10.1561/2500000031

Back, R. 1989. A Method for Refining Atomicity in Parallel Algorithms. In PARLE (LNCS), Vol. 366. Springer, 199–216. https://doi.org/10.1007/3-540-51285-3_42

Balmau, O.; Guerraoui, R.; Herlihy, M.; and Zablotschi, I. 2016. Fast and Robust Memory Reclamation for Concurrent Data Structures. In SPAA. ACM, 349–359. https://doi.org/10.1145/2935764.2935790

Bäumler, S.; Schellhorn, G.; Tofan, B.; and Reif, W. 2011. Proving linearizability with temporal logic. Formal Asp. Comput. 23, 1 (2011), 91–112. https://doi.org/10.1007/s00165-009-0130-y

Berdine, J.; Cook, B.; and Ishtiaq, S. 2011. SLayer: Memory Safety for Systems-Level Code. In CAV (LNCS), Vol. 6806. Springer, 178–183. https://doi.org/10.1007/978-3-642-22110-1_15

Berdine, J.; Lev-Ami, T.; Manevich, R.; Ramalingam, G.; and Sagiv, S. 2008. Thread Quantification for Concurrent Shape Analysis. In CAV (LNCS), Vol. 5121. Springer, 399–413. https://doi.org/10.1007/978-3-540-70545-1_37

Beyer, D.; Henzinger, T. A.; Jhala, R.; and Majumdar, R. 2005. Checking Memory Safety with Blast. In FASE (LNCS), Vol. 3442. Springer, 2–18. https://doi.org/10.1007/978-3-540-31984-9_2

Bierhoff, K. and Aldrich, J. 2007. Modular Typestate Checking of Aliased Objects. In OOPSLA. ACM, 301–320. https://doi.org/10.1145/1297027.1297050

Birkhoff, G. 1948. Lattice Theory (revised edition). American Mathematical Society.

Bjizak, A.; Gratzer, D.; Krebers, R.; and Birksdal, L. 2019. Iron: Managing Obligations in Higher-order Concurrent Separation Logic. PACMPL 3, POPL (2019), 65:1–65:30. https://doi.org/10.1145/3290378

Bornat, R.; Calcagno, C.; O’Hearn, P. W.; and Parkinson, M. J. 2005. Permission Accounting in Separation Logic. In POPL. ACM, 259–270. https://doi.org/10.1145/1043035.1043037

Bouajjani, A.; Emmi, M.; Enea, C.; and Mutluergil, S. O. 2017. Proving Linearizability Using Forward Simulations. In CAV (LNCS), Vol. 10427. Springer, 542–563. https://doi.org/10.1007/978-3-319-63390-9_28

Bouajjani, A.; Enea, C.; Mutluergil, S. O.; and Tasiran, S. 2018. Reasoning About TSO Programs Using Reduction and Abstraction. In CAV (LNCS), Vol. 10982. Springer, 336–355. https://doi.org/10.1007/978-3-319-96142-2_21

Boyland, J. 2003. Checking Interference with Fractional Permissions. In SAS (LNCS), Vol. 2694. Springer, 55–72. https://doi.org/10.1007/3-540-44898-5_4

Braginsky, A.; Kogan, A.; and Petrank, E. 2013. Drop the Anchor: Lightweight Memory Management for Non-blocking Data Structures. In SPAA. ACM, 33–42. https://doi.org/10.1145/2486159.2486184

Brookes, S. D. 2004. A Semantics for Concurrent Separation Logic. In CONCUR (LNCS), Vol. 3170. Springer, 16–34. https://doi.org/10.1007/978-3-540-28644-8_2

Brown, T. A. 2015. Reclaiming Memory for Lock-Free Data Structures: There has to be a Better Way. In PODC. ACM, 261–270. https://doi.org/10.1145/2767386.2767436

Burckhardt, S.; Dern, C.; Musuvathi, M.; and Tan, R. 2010. Line-up: A Complete and Automatic Linearizability Checker. In PLDI. ACM, 330–340. https://doi.org/10.1145/1806596.1806634

Calcagno, C. and Distefano, D. 2011. Infer: An Automatic Program Verifier for Memory Safety of C Programs. In NASA Formal Methods (LNCS), Vol. 6617. Springer, 459–465. https://doi.org/10.1007/978-3-642-20398-5_33

Casteen, E. and Wrigstad, T. 2017. Relaxed Linear References for Lock-free Data Structures. In ECOOP (LIPIcs), Vol. 74. Schloss Dagstuhl - Leibniz-Zentrum fuer Informatik, 6:1–6:32. https://doi.org/10.4230/LIPIcs.ECOOP.2017.6

Cerný, P.; Radhakrishna, A.; Zufferey, D.; Chaudhuri, S.; and Alur, R. 2010. Model Checking of Linearizability of Concurrent List Implementations. In CAV (LNCS), Vol. 6174. Springer, 465–479. https://doi.org/10.1007/978-3-642-14295-6_41

Cohen, N. 2018. Every Data Structure Deserves Lock-free Memory Reclamation. PACMPL 2, OOPSLA (2018), 143:1–143:24. https://doi.org/10.1145/3276513

Cohen, N. and Petrank, E. 2015a. Automatic Memory Reclamation for Lock-Free Data Structures. In OOPSLA. ACM, 260–279. https://doi.org/10.1145/2814270.2814298

Cohen, N. and Petrank, E. 2015b. Efficient Memory Management for Lock-Free Data Structures with Optimistic Access. In SPAA. ACM, 254–263. https://doi.org/10.1145/2755573.2755579

Colvin, R.; Doherty, S.; and Groves, L. 2005. Verifying Concurrent Data Structures by Simulation. Electr. Notes Theor. Comput. Sci. 137, 2 (2005), 93–110. https://doi.org/10.1016/j.entcs.2005.04.026

Colvin, R.; Groves, L.; Luchangco, V.; and Moir, M. 2006. Formal Verification of a Lazy Concurrent List-Based Set Algorithm. In CAV (LNCS), Vol. 4144. Springer, 475–488. https://doi.org/10.1007/11817963_44

Coppo, M. and Dezani-Ciancaglini, M. 1978. A New Type Assignment for λ-Terms. Arch. Math. Log. 19, 1 (1978), 139–156. https://doi.org/10.1007/BF02011875

Crary, K.; Walker, D.; and Morrisett, J. G. 1999. Typed Memory Management in a Calculus of Capabilities. In POPL. ACM, 262–275. https://doi.org/10.1145/292540.292564

da Rocha Pinto, P.; Dinsdale-Young, T.; and Gardner, P. 2014. TaDA: A Logic for Time and Data Abstraction. In ECOOP (LNCS), Vol. 8586. Springer, 207–231. https://doi.org/10.1007/978-3-662-44202-9_9
Das, M.; Lerner, S.; and Seigle, M. 2002. ESP: Path-Sensitive Program Verification in Polynomial Time. In PLDI. ACM, 57–68. https://doi.org/10.1145/512529.512538

Delbianco, G. A.; Sergey, I.; Naneyvski, A.; and Banerjee, A. 2017. Concurrent Data Structures Linked in Time. In ECOOP (LIPIcs), Vol. 74. Schloss Dagstuhl - Leibniz-Zentrum für Informatik, 8:1–8:30. https://doi.org/10.4230/LIPIcs.ECOOP.2017.8

DeLine, R. and Fähndrich, M. 2004. Typestates for Objects. In ECOOP (LNCS), Vol. 3086. Springer, 465–490. https://doi.org/10.1007/978-3-540-24851-4_21

Derrick, J.; Schellhorn, G.; and Wehrheim, H. 2011. Mechanically Verified Proof Obligations for Linearizability. ToPLaS 33, 1 (2011), 4:1–4:43. https://doi.org/10.1145/1889997.1890001

Detlefs, D.; Martin, P. A.; Moir, M.; and Jr., G. L. S. 2001. Lock-free Reference Counting. In PODC. ACM, 190–199. https://doi.org/10.1145/383962.384016

Dice, D.; Herlihy, M.; and Kogan, A. 2016. Fast Non-intrusive Memory Reclamation for Highly-concurrent Data Structures. In ISMM. ACM, 36–45. https://doi.org/10.1145/2926697.2926699

Dijkstra, E. W. 1982. On Making Solutions More and More Fine-Grained. Springer New York, New York, NY, 292–307. https://doi.org/10.1007/978-1-4612-5695-3_53

Dinsdale-Young, T.; Dodds, M.; Gardner, P.; Parkinson, M. J.; and Vafeiadis, V. 2010. Concurrent Abstract Predicates. In ECOOP (LNCS), Vol. 6183. Springer, 504–528. https://doi.org/10.1007/978-3-642-14107-2_24

Dodds, M.; Feng, X.; Parkinson, M. J.; and Vafeiadis, V. 2009. Deny-Guarantee Reasoning. In ESOP (LNCS), Vol. 5502. Springer, 363–377. https://doi.org/10.1007/978-3-642-00590-9_26

Dodds, M.; Haas, A.; and Kirsch, C. M. 2015. A Scalable, Correct Time-Stamped Stack. In POPL. ACM, 233–246. https://doi.org/10.1145/2676726.2676963

Doepnner, Jr., T. W. 1977. Parallel Program Correctness Through Refinement. In POPL. ACM, 155–169. https://doi.org/10.1145/512950.512965

Doherty, S.; Groves, L.; Luchangco, V.; and Moir, M. 2004. Formal Verification of a Practical Lock-Free Queue Algorithm. In FORTE (LNCS), Vol. 3235. Springer, 97–114. https://doi.org/10.1007/978-3-540-20322-7_2

Doherty, S. and Moir, M. 2009. Nonblocking Algorithms and Backward Simulation. In DISC (LNCS), Vol. 5805. Springer, 274–288. https://doi.org/10.1007/978-3-642-04355-0_28

Dongol, B. and Derrick, J. 2015. Verifying Linearisability: A Comparative Survey. ACM Comput. Surv. 48 (2015). https://doi.org/10.1145/1480881.1480885

Emmi, M. and Enea, C. 2018. Sound, Complete, and Tractable Linearizability Monitoring for Concurrent Collections. PACMPL 2, POPL (2018), 25:1–25:27. https://doi.org/10.1145/3158113

Emmi, M.; Enea, C.; and Hamza, J. 2015. Monitoring Refinement via Symbolic Reasoning. In PLDI. ACM, 260–269. https://doi.org/10.1145/2737924.2737983

Fähndrich, M. and DeLine, R. 2002. Adoption and Focus: Practical Linear Types for Imperative Programming. In PLDI. ACM, 13–24. https://doi.org/10.1145/512529.512532

Feng, X. 2009. Local Rely-guarantee Reasoning. In POPL. ACM, 315–327. https://doi.org/10.1145/1480881.1480922

Feng, X.; Ferreira, R.; and Shao, Z. 2007. On the Relationship Between Concurrent Separation Logic and Assume-Guarantee Reasoning. In ESOP (LNCS), Vol. 4421. Springer, 173–188. https://doi.org/10.1007/978-3-540-71316-6_13

Fink, S. J.; Yahav, E.; Dor, N.; Ramalingam, G.; and Geay, E. 2006. Effective Typestate Verification in the Presence of Aliasing. In ISSTA. ACM, 133–144. https://doi.org/10.1145/1146238.1146254

Flanagan, C.; Freund, S. N.; Lifshin, M.; and Qadeer, S. 2008. Types for Atomicity: Static Checking and Inference for Java. ToPLaS 30, 4 (2008), 20:1–20:53. https://doi.org/10.1145/1377492.1377495

Flanagan, C.; Freund, S. N.; Qadeer, S.; and Seshia, S. A. 2005. Modular verification of multithreaded programs. Theor. Comput. Sci. 338, 1-3 (2005), 153–183. https://doi.org/10.1016/j.tcs.2004.12.006

Flanagan, C. and Qadeer, S. 2003. A Type and Effect System for Atomicity. In PLDI. ACM, 338–349. https://doi.org/10.1145/781131.781169

Flanagan, C.; Qadeer, S.; and Seshia, S. A. 2002. A Modular Checker for Multithreaded Programs. In CAV (LNCS), Vol. 2404. Springer, 180–194. https://doi.org/10.1007/3-540-45657-0_14

Foster, J. S.; Terauchi, T.; and Aiken, A. 2002. Flow-Sensitive Type Qualifiers. In PLDI. ACM, 1–12. https://doi.org/10.1145/512529.512531
Kuru, I. and Gordon, C. S. 2019. Safe Deferred Memory Reclamation with Types. In *ESOP (LNCS)*, Vol. 11423. Springer, 88–116. https://doi.org/10.1007/978-3-030-17184-1_4

Lamport, L. and Schneider, F. B. 1989. Pretending Atomicity. *SRC Research Report 44* (1989). https://www.microsoft.com/en-us/research/publication/pretending-atomicity/

Laviron, V.; Chang, B. E.; and Rival, X. 2010. Separating Shape Graphs. In *ESOP (LNCS)*, Vol. 6012. Springer, 387–406. https://doi.org/10.1007/978-3-642-11957-6_21

Liang, H. and Feng, X. 2013. Modular Verification of Linearizability with Non-fixed Linearization Points. In *PLDI*. ACM, 459–470. https://doi.org/10.1145/2491956.2462189

Liang, H.; Feng, X.; and Fu, M. 2012. A Rely-guarantee-based Simulation for Verifying Concurrent Program Transformations. In *POPL*. ACM, 455–468. https://doi.org/10.1145/2103656.2103711

Liang, H.; Feng, X.; and Fu, M. 2014. Rely-Guarantee-Based Simulation for Compositional Verification of Concurrent Program Transformations. *ToPLAs* 36, 1 (2014), 3:1–3:37. https://doi.org/10.1145/2576235

Lipton, R. J. 1975. Reduction: A Method of Proving Properties of Parallel Programs. *CACM*, 18, 12 (1975), 717–721.

Liu, Y.; Chen, W.; Liu, Y. A.; and Sun, J. 2009. Model Checking Linearizability via Refinement. In *FM (LNCS)*, Vol. 5850. Springer, 321–337. https://doi.org/10.1007/978-3-642-05089-3_21

Liu, Y.; Chen, W.; Liu, Y. A.; Sun, J.; Zhang, S. J.; and Dong, J. S. 2013. Verifying Linearizability via Optimized Refinement Checking. *IEEE Trans. Software Eng.* 39, 7 (2013), 1018–1039. https://doi.org/10.1109/TSE.2012.82

Lowe, G. 2017. Testing for linearizability. *Concurrency and Computation: Practice and Experience* 29, 4 (2017). https://doi.org/10.1002/cpe.3928

McKenney, P. E. and Slingwine, J. D. 1998. Read-copy Update: Using Execution History to Solve Concurrency Problems.

Meyer, R. and Wolff, S. 2018. Decoupling Lock-Free Data Structures from Memory Reclamation for Static Analysis. *CoRR*. abs/1810.10807 (2018). http://arxiv.org/abs/1810.10807

Meyer, R. and Wolff, S. 2019. Decoupling Lock-free Data Structures from Memory Reclamation for Static Analysis. *PACMPL* 3, POPL (2019), 58:1–58:31. https://doi.org/10.1101/2019.05.16.053071

Michael, M. M. 2002a. High Performance Dynamic Lock-free Hash Tables and List-based Sets. In *SPAA*. ACM, 73–82. https://doi.org/10.1145/564870.564881

Michael, M. M. 2002b. Safe Memory Reclamation for Dynamic Lock-free Objects Using Atomic Reads and Writes. In *PODC*. ACM, 21–30. https://doi.org/10.1145/571825.571829

Michael, M. M. and Scott, M. L. 1996. Simple, Fast, and Practical Non-Blocking and Blocking Concurrent Queue Algorithms. In *PODC*. ACM, 267–275. https://doi.org/10.1145/248052.248106

Nanevski, A.; Ley-Wild, R.; Sergey, I.; and Delbianco, G. A. 2014. Communicating State Transition Systems for Fine-Grained Concurrent Resources. In *ESOP (LNCS)*, Vol. 8410. Springer, 290–310. https://doi.org/10.1007/978-3-642-54833-8_16

Necula, G. C.; McPeak, S.; and Weimer, W. 2002. CCured: Type-safe Retrofitting of Legacy Code. In *POPL*. ACM, 128–139. https://doi.org/10.1145/503272.503286

Nikolaev, R. and Ravindran, B. 2019. Hyaline: Fast and Transparent Lock-Free Memory Reclamation. In *PODC*. ACM, 419–421. https://doi.org/10.1145/3293611.331575

O’Hearn, P. W. 2004. Resources, Concurrency and Local Reasoning. In *CONCUR (LNCS)*, Vol. 3170. Springer, 49–67. https://doi.org/10.1007/3-540-28644-8_4

O’Hearn, P. W.; Reynolds, J. C.; and Yang, H. 2001. Local Reasoning about Programs that Alter Data Structures. In *CSL (LNCS)*, Vol. 2142. Springer, 1–19. https://doi.org/10.1007/3-540-44802-0_1

O’Hearn, P. W.; Rinetzky, N.; Vechev, M. T.; Yahav, E.; and Yorsh, G. 2010. Verifying Linearizability with Hindsight. In *PODC*. ACM, 85–94. https://doi.org/10.1145/1835648.1835722

Owicki, S. S. and Gries, D. 1976. An Axiomatic Proof Technique for Parallel Programs I. *Acta Inf.* 6 (1976), 319–340. https://doi.org/10.1007/BF00268134

Parkinson, M. J.; Bornat, R.; and O’Hearn, P. W. 2007. Modular Verification of a Non-blocking Stack. In *POPL*. ACM, 297–302. https://doi.org/10.1145/1190216.1190261

Pierce, B. C. 2002. *Types and programming languages*. MIT Press.

Ramalhete, P. and Correia, A. 2017. Brief Announcement: Hazard Eras - Non-Blocking Memory Reclamation. In *SPAA*. ACM, 367–369. https://doi.org/10.1145/3087556.3087588

Reynolds, J. C. 2002. Separation Logic: A Logic for Shared Mutable Data Structures. In *LICS*. IEEE, 55–74. https://doi.org/10.1109/LICS.2002.1029817

Schellhorn, G.; Wehrheim, H.; and Derrick, J. 2012. How to Prove Algorithms Linearisable. In *CAV (LNCS)*, Vol. 7358. Springer, 243–259. https://doi.org/10.1007/978-3-642-31424-7_21

Segalov, M.; Lev-Ami, T.; Manevich, R.; Ramalingam, G.; and Sagiv, M. 2009. Abstract Transformers for Thread Correlation Analysis. In *APLAS (LNCS)*, Vol. 5904. Springer, 30–46. https://doi.org/10.1007/978-3-642-10672-9_5

Sergey, I.; Nanevski, A.; and Banerjee, A. 2015a. Mechanized Verification of Fine-grained Concurrent Programs. In *PLDI*. ACM, 77–87. https://doi.org/10.1145/2737924.2737964
68:36 Roland Meyer and Sebastian Wolff

Sergey, I.; Nanevski, A.; and Banerjee, A. 2015b. Specifying and Verifying Concurrent Algorithms with Histories and Subjectivity. In *ESOP (LNCS)*, Vol. 9032. Springer, 333–358. https://doi.org/10.1007/978-3-662-46669-8_14

Sethi, D.; Talupur, M.; and Malik, S. 2013. Model Checking Unbounded Concurrent Lists. In *SPIN (LNCS)*, Vol. 7976. Springer, 320–340. https://doi.org/10.1007/978-3-642-39176-7_20

Ströder, T.; Giesl, J.; Brockschmidt, M.; Frohn, F.; Fuhs, C.; Hensel, J.; Schneider-Kamp, P.; and Aschermann, C. 2017. Automatically Proving Termination and Memory Safety for Programs with Pointer Arithmetic. *J. Autom. Reasoning* 58, 1 (2017), 33–65. https://doi.org/10.1007/s10817-016-9389-x

Strom, R. E. and Yemini, S. 1986. Typestate: A Programming Language Concept for Enhancing Software Reliability. *IEEE Trans. Software Eng.* 12, 1 (1986), 157–171. https://doi.org/10.1109/TSE.1986.6312929

Svendsen, K. and Birkedal, L. 2014. Impredicative Concurrent Abstract Predicates. In *ESOP (LNCS)*, Vol. 8410. Springer, 149–168. https://doi.org/10.1007/978-3-642-54833-8_9

Tofan, B.; Schellhorn, G.; and Reif, W. 2011. Formal Verification of a Lock-Free Stack with Hazard Pointers. In *ICTAC (LNCS)*, Vol. 6916. Springer, 239–255. https://doi.org/10.1007/978-3-642-23283-1_16

Travkin, O.; Mütze, A.; and Wehrheim, H. 2013. SPIN as a Linearizability Checker under Weak Memory Models. In *HVC (LNCS)*, Vol. 8244. Springer, 320–340. https://doi.org/10.1007/978-3-642-39176-7_21

Treiber, R. K. 1986. *Systems Programming: Coping with Parallelism*. Technical Report RJ 5118. IBM.

Turon, A.; Dreyer, D.; and Birkedal, L. 2013. Unifying Refinement and Hoare-style Reasoning in a Logic for Higher-order Concurrency. In *ICFP*. ACM, 377–390. https://doi.org/10.1145/2544174.2500600

Turon, A.; Vafeiadis, V.; and Dreyer, D. 2014. GPS: Navigating Weak Memory with Ghosts, Protocols, and Separation. In *OOPSLA*. ACM, 691–707. https://doi.org/10.1145/2660193.2660243

Vafeiadis, V. 2009. Shape-Value Abstraction for Verifying Linearizability. In *VMCAI (LNCS)*, Vol. 5403. Springer, 335–348. https://doi.org/10.1007/978-3-540-93900-9_27

Vafeiadis, V. 2010a. Automatically Proving Linearizability. In *CAV (LNCS)*, Vol. 6174. Springer, 450–464. https://doi.org/10.1007/978-3-642-14295-6_40

Vafeiadis, V. 2010b. ROSep Action Inference. In *VMCAI (LNCS)*, Vol. 5944. Springer, 345–361. https://doi.org/10.1007/978-3-642-11319-2_25

Vafeiadis, V. and Parkinson, M. J. 2007. A Marriage of Rely/Guarantee and Separation Logic. In *CONCUR (LNCS)*, Vol. 4703. Springer, 256–271. https://doi.org/10.1007/978-3-540-74407-8_18

Vechev, M. T. and Yahav, E. 2008. Deriving Linearizable Fine-grained Concurrent Objects. In *PLDI*. ACM, 125–135. https://doi.org/10.1145/1375581.1375598

Vechev, M. T.; Yahav, E.; and Yorsh, G. 2009. Experience with Model Checking Linearizability. In *SPIN (LNCS)*, Vol. 5578. Springer, 261–278. https://doi.org/10.1007/978-3-642-02652-2_21

Wen, H.; Izraelevitz, J.; Cai, W.; Beadle, H. A.; and Scott, M. L. 2018. Interval-based Memory Reclamation. In *PPOPP*. ACM, 1–13. https://doi.org/10.1145/3178487.3178488

Wulf, M. D.; Doyen, L.; Henzinger, T. A.; and Raskin, J. 2006. Antichains: A New Algorithm for Checking Universality of Finite Automata. In *CAV (LNCS)*, Vol. 4144. Springer, 17–30. https://doi.org/10.1007/11817963_5

Yang, A. M. and Wrigstad, T. 2017. Type-assisted Automatic Garbage Collection for Lock-free Data Structures. In *ISMM*. ACM, 14–24. https://doi.org/10.1145/3092255.3092274

Yang, H.; Lee, O.; Berdine, J.; Calcagno, C.; Cook, B.; Distefano, D.; and O’Hearn, P. W. 2008. Scalable Shape Analysis for Systems Code. In *CAV (LNCS)*, Vol. 5123. Springer, 385–398. https://doi.org/10.1007/978-3-540-70545-1_36

Yang, X.; Katoen, J.; Lin, H.; and Wu, H. 2017. Verifying Concurrent Stacks by Divergence-Sensitive Bisimulation. *CoRR* abs/1701.06104 (2017). http://arxiv.org/abs/1701.06104

Zhang, S. J. 2011. Scalable Automatic Linearizability Checking. In *ICSE*. ACM, 1185–1187. https://doi.org/10.1145/1985793.1986037

Zhu, H.; Petri, G.; and Jagannathan, S. 2015. Poling: SMT Aided Linearizability Proofs. In *CAV (LNCS)*, Vol. 9207. Springer, 3–19. https://doi.org/10.1007/978-3-319-21683-3_1
A EXAMPLE FOR HAZARD POINTERS

We give a brief example on how our type system infers that a pointer can be accessed safely, i.e., how guarantee $\mathcal{S}$ is obtained, when hazard pointers are used. Figure 12 depicts a common usage pattern and its typing. HP is specified by the SMR automaton $O_{\text{Base}} \times O_{\text{HP}}$. For $O_{\text{HP}}$ and the HP-specific guarantees consider Figure 13. We use two HP-specific guarantees $E_{\text{inv}}$ and $E_{\text{isu}}$ that encode the fact that protect for the 0-indexed hazard pointer has been invoked and returned, respectively.

In the beginning, the type of $\text{ptr}$ is $\varnothing$. There are no guarantees. Next, protect is invoked with $\text{ptr}$ as a parameter. Using Rule (ENTER) we obtain type $E_{\text{inv}}$ for $\text{ptr}$, stating that we have definitely invoked protect for $\text{ptr}$. We already discussed in Section 6.3 how this is computed. After protect returns, $\text{ptr}$ obtains type $E_{\text{isu}}$ from an application of Rule (EXIT). It encodes the fact that a protection has been issued. Accessing $\text{ptr}$, however, is not safe at this point since we do not know whether $\text{ptr}$ has been retired in the meantime. To ensure that the protection has been successful, the subsequent code contains an active annotation. It adds $\mathcal{A}$ to the type of $\text{ptr}$, Rule (ACTIVE). An application of Rule (INFER) allows us to infer $\mathcal{S}$ for $\text{ptr}$. The type system successfully discovered that it is safe to access $\text{ptr}$.

B MISSING DETAILS

B.1 Definitions

Definition B.1. The liberal semantics is defined by the following rules, assuming $r \in [P]_X$ and that $\text{act}$ respects the control flow of $P$.

(Assign1) If $\text{act} = (t, p.\text{next} := q, [a.\text{next} \mapsto b])$ then $m_r(p) = a$ and $m_r(q) = b$.

(Assign2) If $\text{act} = (t, p := q, [p \mapsto m_r(q)])$.

(Assign3) If $\text{act} = (t, p := q.\text{next}, [p \mapsto m_r(a.\text{next})])$ with $m_r(q) = a \in \text{Adr}$.

(Assign4) If $\text{act} = (t, u := \text{op}(u'_1, \ldots, u'_n), [u \mapsto d])$ with $d = \text{op}(m_r(u'_1), \ldots, m_r(u'_n))$.

(Assign5) If $\text{act} = (t, p.\text{data} := u', [a.\text{data} \mapsto m_r(u')])$ with $m_r(p) = a \in \text{Adr}$.

(Assign6) If $\text{act} = (t, u := q.\text{data}, [u \mapsto m_r(a.\text{data})])$ with $m_r(q) = a \in \text{Adr}$.

(Assume) If $\text{act} = (t, \text{assume} \text{lhs} \triangleq \text{rhs}, \varnothing)$ then $m_r(\text{lhs}) \triangleq m_r(\text{rhs})$.

(Malloc) If $\text{act} = (t, \text{assume} \text{lhs} \triangleq \text{rhs}, \varnothing)$ then $\text{up}$ has the form $p \mapsto a, a.\text{next} \mapsto \text{seg}, a.\text{data} \mapsto d$ so that $a \in \text{fresh}(r)$ or $a \in \text{freed}(r) \cap Y$.

(Atomic) If $\text{act} = (t, \text{beginAtomic}, \varnothing)$ or $\text{act} = (t, \text{endAtomic}, \varnothing)$.

(Free) If $\text{act} = (\bot, \text{free(a)}, \varnothing)$ then $a \in X$.

(Enter) $\text{act} = (t, \text{enter func}(p, \bar{u}), \varnothing)$, then $m_r(p) \neq \text{seg}$ for every $p$ in $\bar{p}$.

(Exit) $\text{act} = (t, \text{exit func}, \varnothing)$.

(Invariant1) $\text{act} = (t, @\text{inv angel} r, \varnothing)$.

(Invariant2) $\text{act} = (t, @\text{inv p in} r, \varnothing)$.

(Invariant3) $\text{act} = (t, @\text{inv active(p)}, \varnothing)$.

(Invariant4) $\text{act} = (t, @\text{inv p = q}, \varnothing)$.

Fig. 12. A typing example for a typical usage pattern of hazard pointers.
The SMR automaton $O_{HP}$ specifies the Hazard Pointer method for two hazard pointers per thread.

$P_0 := \text{enter protect}(t, a, 0), \ t = z_t \land a = z_a$

$P_1 := \text{enter protect}(t, a, 1), \ t = z_t \land a = z_a$

$!P_0 := \text{enter protect}(t, a, 0), \ t = z_t \land a \neq z_a$

$!P_1 := \text{enter protect}(t, a, 1), \ t = z_t \land a \neq z_a$

$E_0 := \text{exit protect}(t), \ t = z_t$

$E_1 := \text{exit protect}(t), \ t = z_t$

$R := \text{enter retire}(t, a), \ a = z_a$

$F := \text{free}(a), \ a = z_a$

Fig. 13. The SMR automaton $O_{HP}$ specifies the Hazard Pointer method for two hazard pointers per thread.
Definition B.2. The history induced by a computation $\tau$, denoted $H(\tau)$, is defined by:

$H(\varepsilon) = \varepsilon$

$H(\tau.(t, \text{free}(a), \text{up}, \text{pc})) = H(\tau).\text{free}(a)$

$H(\tau.(t, \text{enter} \text{func}(p, \text{up}, \text{pc})) = H(\tau).\text{func}(t, m_r(p), m_r(\text{up}))$

$H(\tau.(t, \text{exit func}, \text{up}, \text{pc})) = H(\tau).\text{exit func}(t)$

$H(\tau.\text{act}) = H(\tau)$

otherwise.

Definition B.3. The fresh addresses in a computation $\tau$, denoted by $\text{fresh(\tau)}$, are defined by:

$\text{fresh}(\varepsilon) = \text{Adr}$

$\text{fresh}(\tau.\text{act}) = \text{fresh}(\tau) \setminus \{a\}$ if $\text{com}(\text{act}) \equiv \text{free}(a)$

$\text{fresh}(\tau.\text{act}) = \text{fresh}(\tau) \setminus \{a\}$ if $\text{com}(\text{act}) \equiv p := \text{malloc} \land m_{\text{r.act}}(p) = a$

$\text{fresh}(\tau.\text{act}) = \text{fresh}(\tau)$ otherwise.

The definition carries over naturally to histories.

Definition B.4. The freed addresses in a computation $\tau$, denoted by $\text{freed(\tau)}$, are defined by:

$\text{freed}(\varepsilon) = \emptyset$

$\text{freed}(\tau.\text{act}) = \text{freed}(\tau) \cup \{a\}$ if $\text{com}(\text{act}) \equiv \text{free}(a)$

$\text{freed}(\tau.\text{act}) = \text{freed}(\tau) \setminus \{a\}$ if $\text{com}(\text{act}) \equiv p := \text{malloc} \land m_{\text{r.act}}(p) = a$

$\text{freed}(\tau.\text{act}) = \text{freed}(\tau)$ otherwise.

Definition B.5. The retired addresses in a computation $\tau$, denoted by $\text{retired(\tau)}$, are defined by:

$\text{retired}(\varepsilon) = \emptyset$

$\text{retired}(\tau.\text{act}) = \text{retired}(\tau) \cup \{a\}$ if $\text{com}(\text{act}) \equiv \text{retire}(p) \land a = m_r(p)$

$\text{retired}(\tau.\text{act}) = \text{retired}(\tau) \setminus \{a\}$ if $\text{com}(\text{act}) \equiv \text{free}(a)$

$\text{retired}(\tau.\text{act}) = \text{retired}(\tau)$ otherwise.

Definition B.6. The active addresses in a computation $\tau$ are:

$\text{active}(\tau) := \text{Adr} \setminus (\text{freed}(\tau) \cup \text{retired}(\tau))$.

Definition B.7 (Angel Denotation). Consider some $\tau \in \prod_{\text{Adr}}^\text{Adr}$. Let $\text{inv}(\tau)$ have the prenex normal form $\exists r_1 \ldots \exists r_n. \phi$, where $\phi$ is quantifier-free. Let $r_n$ be the instance of angel $r$ resulting from the last allocation in $\tau$. The set of addresses possibly represented by angel $r$ after computation $\tau$ is

$\text{repr}_r(\tau) := \{a \in \text{Adr} \mid \exists A_1, \ldots, A_n \subseteq \text{Adr}. a \in A_n \land (A_1, \ldots, A_n) \models \phi\}$. 

Proc. ACM Program. Lang., Vol. 4, No. POPL, Article 68. Publication date: January 2020.
Definition B.8 (Valid Expressions). The valid pointer expressions in a computation \( \tau \in O[\mathcal{P}]_{\text{Adr}} \), denoted by \( \text{valid}_\tau \subseteq P\text{Exp} \), are defined by:

\[
\begin{align*}
\text{valid}_\tau &:= \text{PVar} \\
\text{valid}_{\tau.\text{alloc} (= q, \text{up})} &:= \text{valid}_\tau \cup \{p\} & \text{if } q \in \text{valid}_\tau \\
\text{valid}_{\tau.\text{free}(a, \text{up})} &:= \text{valid}_\tau \setminus \{p\} & \text{if } q \notin \text{valid}_\tau \\
\text{valid}_{\tau.\text{next} (= q, \text{up})} &:= \text{valid}_\tau \cup \{a.\text{next}\} & \text{if } m_\tau(p) = a \in \text{Adr} \land q \in \text{valid}_\tau \\
\text{valid}_{\tau.\text{next} (= q, \text{up})} &:= \text{valid}_\tau \setminus \{a.\text{next}\} & \text{if } m_\tau(p) = a \in \text{Adr} \land q \notin \text{valid}_\tau \\
\text{valid}_{\tau.\text{next} (= q, \text{up})} &:= \text{valid}_\tau \cup \{\text{p}\} & \text{if } m_\tau(q) = a \in \text{Adr} \land a.\text{next} \in \text{valid}_\tau \\
\text{valid}_{\tau.\text{next} (= q, \text{up})} &:= \text{valid}_\tau \setminus \{\text{p}\} & \text{if } m_\tau(q) = a \in \text{Adr} \land a.\text{next} \notin \text{valid}_\tau \\
\text{valid}_{\tau.\text{free}(a, \text{up})} &:= \text{valid}_\tau \setminus \text{invalid}_a & \text{if } \{p \mapsto a\} \in \text{up} \\
\text{valid}_{\tau.\text{assume} (= p, \text{up})} &:= \text{valid}_\tau \cup \{p, a.\text{next}\} & \text{if } \{p, q\} \cap \text{valid}_\tau \neq \emptyset \\
\text{valid}_{\tau.\text{act}(a, \text{up})} &:= \text{valid}_\tau & \text{otherwise.}
\end{align*}
\]

We have \( \text{invalid}_a := \{p | m_\tau(p) = a\} \cup \{b.\text{next} | m_\tau(b.\text{next}) = a\} \cup \{a.\text{next}\} \).

Definition B.9 (Observer Behavior). The behavior allowed by \( O \) on address \( a \) after history \( h \), denoted by \( \mathcal{F}_O(h, a) \), is the set \( \mathcal{F}_O(h, a) := \{h' | h.\h' \in S(O) \land \text{frees}(\h') \subseteq a\} \). If clear from the context, we just write \( \mathcal{F}(h, a) \).

Definition B.10 (Unsafe Access). A computation \( \tau.\text{act} \) raises an unsafe access if \( \text{com}(\text{act}) \) contains \( \text{p.data} \) or \( \text{p.next} \) with \( p \notin \text{valid}_\tau \).

Definition B.11 (Unsafe Assumption). A computation \( \tau.\text{act} \) raises an unsafe assumption if \( \text{com}(\text{act}) \) is of the form assume \( p = q \) with \( \{p, q\} \notin \text{valid}_\tau \).

Definition B.12 (Unsafe Retire). A computation \( \tau.\text{act} \) raises an unsafe retire if \( \text{com}(\text{act}) \) is of the form enter retire \( (p) \) with \( p \notin \text{valid}_\tau \).

Definition B.13 (Pointer Race). A computation \( \tau.\text{act} \) raises a pointer race (PR) if it raises (i) an unsafe access, (ii) an unsafe assumption, (iii) an unsafe call, or (iv) an unsafe retire. It is pointer race free (PRF) if none of its prefixes raises a PR.

Definition B.14 (Renaming). A renaming of address \( a \) and \( b \) in a history \( h \), denoted by \( h[a/b] \), replaces in \( h \) every occurrence of \( a \) with \( b \), and vice versa, as follows:

\[
e[a/b] = e
\]

\[
\begin{align*}
(h.\text{func}(\hat{c}, \hat{d}))[a/b] &= (h[a/b]).(\text{func}(\hat{c}[a/b], \hat{d})) \\
(h.\text{free}(c))[a/b] &= (h[a/b]).(\text{free}(c[a/b])) \\
h.\text{evt}[a/b] &= h[a/b].\text{evt} & \text{otherwise.}
\end{align*}
\]

where \( a[a/b] = b, b[a/b] = a \), and \( c[a/b] = c \) for all \( a \neq c \neq b \).

Definition B.15 (Elision Support). Observer \( O \) supports elision of memory reuse if

(i) \( \mathcal{F}_O(h.\text{free}(a), a) = \mathcal{F}_O(h, b) \) for all \( h, a, b \) with \( a \neq b \) and \( h.\text{free}(a) \in S(O) \),

(ii) \( \mathcal{F}_O(h, c) = \mathcal{F}_O(h[a/b], c) \) for all \( h, a, b, c \) with \( a \neq c \neq b \),

(iii) \( \mathcal{F}_O(h, a) \subseteq \mathcal{F}_O(h[a/b], a) \) for all \( h, a, b \) with \( a \neq \text{retired}(h) \) and \( b \in \text{fresh}(h) \), and

(iv) \( \mathcal{F}_O(h.\text{free}(a), a) \subseteq \mathcal{F}_O(h, a) \) for all \( h, a \).

Definition B.16. The domain of a type environment \( \Gamma \) is defined by \( \text{dom}(\Gamma) = \{x | \exists T. x : T \in \Gamma\} \).
Definition B.17. Consider some $\Gamma$ and $p = p_1, \ldots, p_n$ with $\Gamma(p_i) = T_i$. Then we define:

\[
\text{safeEnter}(\Gamma, \text{func}(p, \bar{u})) = \text{true}
\]

iff \( \forall h \forall \bar{a}, \bar{b}, c, \bar{d}. \ (\forall i. (a_i = c \lor \text{isValid}(T_i)) \implies a_i = b_i) \)

\& \mathcal{FO}(h, \text{func}(t, \bar{b}, \bar{d}), c) \not\subseteq \mathcal{FO}(h, \text{func}(t, \bar{a}, \bar{d}), c) .
\]

Definition B.18 (Post Image). The post image for pointers $p$ and angles $r$ is defined by:

\[
\text{post}_{p, \text{com}}(L) := \{l' \mid \exists \exists m. \ (l, \bar{r}) \xrightarrow{m(\text{com})} (l', \bar{r}) \land l \in L \land \bar{r}(z_a) = t \land \bar{r}(z_a) = m(p)\}
\]

\[
\text{post}_{r, \text{com}}(L) := \{l' \mid \exists \exists m. \ (l, \bar{r}) \xrightarrow{m(\text{com})} (l', \bar{r}) \land l \in L \land \bar{r}(z_a) = t\}
\]

where $m(\text{com}_t)$ means the event that results from thread $t$ executing $\text{com}$ under memory $m$.

Definition B.19 (Relaxed Unsafe Assumption). A computation $\tau.\text{act}$ raises a relaxed unsafe assumption if $\text{com}(\text{act})$ is assume $p = q$ such that there is $x, y \in \{p, q\}$ with $p \not\equiv y$ and $x \not\in \text{valid}_\tau$ and free($m, y) \in \mathcal{H}(\tau)$.

Definition B.20 (Relaxed Pointer Race). A computation $\tau.\text{act}$ is a relaxed pointer race (RPR) if $\text{act}$ is (i) an unsafe access, (ii) a relaxed unsafe assumption, (iii) an unsafe call, or (iv) an unsafe retire.

Theorem B.21 (Generalization of Theorem 4.1). If $\mathcal{O}$ supports elision and the semantics $\mathcal{O}[\mathbb{P}]_{Adr}^\mathcal{O}$ is relaxed-pointer-race-free, then $\mathcal{O}[\mathbb{P}]_{Adr}^\mathcal{O} < \mathcal{O}[\mathbb{P}]_{Adr}^\mathcal{O}$.

Remark 1 (Theorem B.21). In practice, programs use a null constant. Since null is not part of our command language, a program needs to define it itself. Ensuring that null is never written to nor retired can be done easily, using a syntactic checks and assertions, respectively. Then, according to Theorem 4.1, any pointer may be compared to null without risking a (relaxed) pointer race. This can increase the applicability of the type system and ease the implementation of tools.

B.2 Reduction

Definition B.22. We write $m(e) = \perp$ if $e \not\in \text{dom}(m)$.

Definition B.23 (In-Use Addresses). An address $a$ is in-use in memory $m$ if $m$ contains a pointer to $a$. Formally, the addresses in-use are $\text{adr}(m) := (\text{range}(m) \cup \text{dom}(m)) \cap \text{Adr}$ where we use $\{a.\text{next}\} \cap \text{Adr} = \text{adr} = a$ and likewise for data selectors.

Definition B.24 (Restrictions). A restriction of $m$ to a set $P \subseteq \mathbb{P}ex$, denoted by $m|_P$, is a new $m'$ with $\text{dom}(m') := P \cup \text{DVar} \cup \{a.\text{data} \in \mathbb{D}ex \mid a \in m(P)\}$ and $m(e) = m'(e)$ for all $e \in \text{dom}(m')$.

Definition B.25 (Computation similarity). Two computations $\tau$ and $\sigma$ are similar, denoted by $\tau \sim \sigma$, if $\text{ctrl}(\tau) = \text{ctrl}(\sigma)$ and $m_{|\text{valid}_\tau} = m_{|\text{valid}_\sigma}$.

Definition B.26 (Observer Behavior Inclusion). Consider $\tau, \sigma \in \mathcal{O}[\mathbb{P}]_{Adr}^\mathcal{O}$. Then, $\sigma$ includes the (observer) behavior of $\tau$, denoted by $\tau \subseteq \sigma$, if $\mathcal{FO}(\tau, a) \subseteq \mathcal{FO}(\sigma, a)$ holds for all $a \in \text{adr}(m|_{\text{valid}_\tau})$.

Definition B.27 (Computation Relation). Two computations are in computation relation, denoted $\tau \prec \sigma$, if $\text{ctrl}(\tau) = \text{ctrl}(\sigma)$ and $m_{|\text{valid}_\tau} = m_{|\text{valid}_\sigma}$.

Lemma B.28. $\mathcal{P}^Y_X$ is prefix closed by Assumption 1.

Lemma B.29. Consider $\tau \in \mathcal{P}^Y_X$. Then, $\text{adr}(m_{|\text{valid}_\tau}) = (\text{valid}_\tau \cap \text{Adr}) \cup m_{|\text{valid}_\tau}$.

Lemma B.30. Consider $\tau, \sigma \in \mathcal{O}[\mathbb{P}]_{Adr}^\mathcal{O}$. If $\tau \sim \sigma$, then $\text{valid}_\tau = \text{valid}_\sigma$.

Lemma B.31. Let $\text{evt} = \text{func}(t, \bar{a}, \bar{d})$. Then, $h_1 \in \mathcal{FO}(h_2.\text{evt}, a)$ iff $\text{evt}.h_1 \in \mathcal{FO}(h_2, a)$. 
Lemma B.32. Consider $\tau \in \| P \|_{Adr}^{O}$ PRF. Then, $adr(m_{r}[\text{valid}_{r}]) \cap m_{r}(\text{PExp } \setminus \text{valid}_{r}) = \emptyset$.

Lemma B.33. If $\tau \in \| P \|_{Adr}^{O}$ and $m_{r}(\text{pexp}) \in \text{freed}(\tau)$, then $\text{pexp} \notin \text{valid}_{r}$.

Lemma B.34. Let $\tau \in O\| P \|_{Adr}^{O}$ and $a \in (\text{fresh}(\tau) \cup \text{freed}(\tau)) \setminus \text{retired}(\tau)$, and $b \in \text{fresh}(\tau)$. If $O$ supports elision, then $\mathcal{F}_{O}(\tau, a) \subseteq \mathcal{F}_{O}(\tau, b)[b/a]$.

Lemma B.35. Assume $O$ supports elision. Let $\tau \in O\| P \|_{Adr}^{O}$, $a \notin adr(m_{r}[\text{valid}_{r}])$, and $A \subseteq A_{dr}$ with $|A| < \infty$. Then there is $\sigma \in O\| P \|_{Adr}^{O}$ and $b \in \text{fresh}(\tau) \setminus A$ with:

- $\tau \sim \sigma$ and $\tau < \sigma$ and $\text{retired}(\tau) \subseteq \text{retired}(\sigma) \cup \{a\}$ and $a \in \text{fresh}(\sigma)$,
- $b \in \text{fresh}(\sigma) \iff a \in \text{fresh}(\tau)$ and $\text{fresh}(\sigma) \setminus \{a, b\} = \text{fresh}(\tau) \setminus \{a, b\}$,
- $\mathcal{F}_{O}(\tau, a) = \mathcal{F}_{O}(\sigma, b)[b/a]$ and $\mathcal{F}_{O}(\tau, b)[b/a] = \mathcal{F}_{O}(\sigma, a)$,
- $\forall c. a \neq c \neq b \Rightarrow \mathcal{F}_{O}(\tau, c) = \mathcal{F}_{O}(\sigma, c)$, and
- $\forall e, e' \in \text{PVar} \cup \{c.\text{next }| c \in m_{r}(\text{valid}_{r})\}$. $m_{r}(e) \neq m_{r}(e') \Rightarrow m_{\sigma}(e) \neq m_{\sigma}(e')$.

Lemma B.36. Assume that $O$ supports elision and that $O\| P \|_{Adr}^{O}$ is PRF. Then, for every $\tau \in O\| P \|_{Adr}^{O}$ there is some $\sigma \in O\| P \|_{Adr}^{O}$ with $\tau \sim \sigma$, $\tau < \sigma$, and $\text{retired}(\tau) \subseteq \text{retired}(\sigma)$. Moreover, $m_{r}(e) \neq m_{r}(e')$ implies $m_{\sigma}(e) \neq m_{\sigma}(e')$ for all $e, e' \in \text{PVar} \cup \{b.\text{next }| b \in m_{r}(\text{valid}_{r})\}$.

Lemma B.37. If $\tau \in \| P \|_{Adr}^{O}$ and $a \in \text{fresh}(\tau)$, then $a \notin \text{range}(m_{r})$.

Lemma B.38. If $\tau \in \| P \|_{Adr}^{O}$, then $\text{fresh}(\tau) \cap \text{retired}(\tau) = \emptyset$.

Lemma B.39. If $\tau \in \| P \|_{Adr}^{O}$ PRF and $\text{pexp} \in \text{PExp}$ with $\text{pexp} \notin \text{valid}_{r}$, then $m_{r}(\text{pexp}) \notin \text{fresh}(\tau)$ or $\text{pexp} \equiv \text{a.next} \land a \in \text{fresh}(\tau) \cup \text{freed}(\tau)$.

Lemma B.40. If $\tau \in \| P \|_{Adr}^{O}$ PRF and $p \in \text{PVar}$ with $p \notin \text{valid}_{r}$, then $m_{r}(p) \notin \text{freed}(\tau)$.

Lemma B.41. Assume $O$ supports elision. Consider $\tau.\text{act} \in O\| P \|_{Adr}^{O}$ with $\text{com}(\text{act}) = \text{free}(a)$. Let $\mathcal{H}(\tau) = h$. Then, $\mathcal{S}(h.\text{free}(a)) \subseteq \mathcal{S}(h)$.

Lemma B.42. Consider some $\tau \in O\| P \|_{Adr}^{O}$ and some $a \in \text{Adr}$. Let $\varphi = \{z_{a} \rightarrow a\}$. Then:

$$(L_{2}, \varphi) \xrightarrow{\mathcal{H}(\tau)} (L_{2}, \varphi) \iff a \in \text{retired}(\tau)$$

$$(L_{2}, \varphi) \xrightarrow{\mathcal{H}(\tau)} (L_{2}, \varphi) \iff a \notin \text{retired}(\tau)$$

$$a \in \text{active}(\tau) \iff (L_{2}, \varphi) \xrightarrow{\mathcal{H}(\tau)} (L_{2}, \varphi)$$

Lemma B.43. Let $\tau.\text{t.free}(a, \text{up}) \in O\| P \|_{Adr}^{O}$. If $O = O_{\text{Base}} \times O_{\text{Impl}}$, then $a \in \text{retired}(\tau)$.

Lemma B.44. Assume $O$ supports elision. Then, for every $\tau \in O\| P \|_{Adr}^{O}$, there is $\sigma \in \| P \|_{\Sigma}$ with:

(i) $\text{ctrl}(\tau) = \text{ctrl}(\sigma)$, (ii) $m_{r} = m_{\sigma}$, and (iii) $\text{fresh}(\tau) \subseteq \text{fresh}(\sigma)$.

Moreover, if $O = O_{\text{Base}} \times O_{\text{Impl}}$, then

(iv) $\text{retired}(\tau) \subseteq \text{retired}(\sigma)$, (v) $\text{freed}(\tau) \subseteq \text{retired}(\sigma)$, and (vi) $\text{inv}(\sigma) \Rightarrow \text{inv}(\tau)$.

Theorem B.45 (Formalization of Theorem 4.1). If $O$ supports elision and the semantics $O\| P \|_{Adr}^{O}$ is pointer-race-free, then $O\| P \|_{Adr}^{O} < \| P \|_{\Sigma}$.

B.3 Type System

In this section we assume, if not stated otherwise, a fixed program $P$ and a fixed SMR automaton $O$ to avoid notational clutter. A generalization to arbitrary programs is straightforward. Recall from Section 3 that we assume that $O$ is of the form $O = O_{\text{Base}} \times O_{\text{Impl}}$ for some SMR automaton $O_{\text{Impl}}$.

Definition B.46 (skip). We use the skip as syntactic sugar for a command that has no effect, for example, assume $u = u$ where $u$ is some data variable. We assume that $\uparrow \{ \Gamma \}$ skip $\{ \Gamma \}$ holds for all $\Gamma$.  

Proc. ACM Program. Lang., Vol. 4, No. POPL, Article 68. Publication date: January 2020.
variables indexed by $t$.

Definition B.48. The thread-local variables of $t$ is the set $\text{local}_t = \{ p \mid p \notin \text{shared} \}$ of non-shared variables indexed by $t$.

Definition B.49. The initial program counter is $pc_{\text{init}}$ with $pc_{\text{init}}(t) = \overline{p[t]}$ for all threads $t$.

Assumption 2. We assume that ghost variables $r$ are local, that is, $r \notin \text{shared}$.

Definition B.50. The initial type environment for $P$ is $\Gamma_{\text{init}}$. For $\overline{p[t]}$ it is $\Gamma_{\text{init}}[t]$. Formally:

\[
\Gamma_{\text{init}} := \{ \tau : \emptyset \mid \tau \in P\text{Var} \cup A\text{Var} \}
\]

\[
\Gamma_{\text{init}}[t] := \{ p : \emptyset \mid p \in P\text{Var} \cap \text{shared} \} \cup \{ \overline{p[t]} : \emptyset \mid p \in P\text{Var} \setminus \text{shared} \} \cup \{ r : \emptyset \mid r \in A\text{Var} \}
\]

Definition B.51. We define $\text{ctrl}(\tau) = \{ pc \mid (pc_{\text{init}}, e) \rightarrow^* (pc, \tau) \}$ where $\rightarrow^*$ is the transition relation among configurations from Figure 14. Then, $\text{ctrl}_t(\tau) = \{ pc(t) \mid pc \in \text{ctrl}(\tau) \}$.

\[
\begin{align*}
\text{(sos1)} & \quad \text{act} = (t, \text{com}, \text{up}) \\
\text{(sos2)} & \quad \text{(com, } \tau \text{)} \rightarrow t \text{ (skip, } \tau . \text{act) } \\
\text{(sos3)} & \quad i \in \{ 1, 2 \} \\
\text{(sos4)} & \quad \text{stmt}_1 \neq \text{skip} \\
& \quad \text{(stmt}_1, \tau \text{)} \rightarrow t \text{ (stmt}_1', \tau' \text{)} \\
\text{(sos5)} & \quad \text{stmt} \in \{ \text{skip, stmt, stmt}^* \} \\
& \quad \text{(stmt}_i^*, \tau \text{)} \rightarrow t \text{ (stmt}_i^{*'}, \tau' \text{)} \\
\text{(sos6)} & \quad \text{pc}(t) = \text{stmt} \\
& \quad \text{(stmt, } \tau \text{)} \rightarrow t \text{ (stmt}_1', \tau' \text{)} \\
& \quad \text{lock}(\tau) = \{ t \} \\
& \quad \text{(pc, } \tau \text{)} \rightarrow t \text{ (pc[t] , } \tau' \text{)} \\
\text{(sos7)} & \quad \text{pc}(t) = \text{stmt} \\
& \quad \text{(stmt, } \tau \text{)} \rightarrow t \text{ (stmt}_1', \tau, \tau' \text{)} \\
& \quad \text{lock}(\tau) = \emptyset \\
& \quad \text{lock}(\tau, \tau') = \{ t \} \\
& \quad \text{(pc, } \tau \text{)} \rightarrow t \text{ (pc[t] , } \tau' \text{)} \\
\text{(sos8)} & \quad \text{act} = (\bot, \text{free(a), } \emptyset) \\
& \quad \text{lock}(\tau) = \emptyset \\
& \quad \text{lock}(\tau \cdot \text{act}) := \text{lock}(\tau) \cup \{ t \} \quad \text{if act} = (t, \text{beginAtomic, up)} \\
& \quad \text{lock}(\tau \cdot \text{act}) := \text{lock}(\tau) \setminus \{ t \} \quad \text{if act} = (t, \text{endAtomic, up)} \\
& \quad \text{lock}(\tau \cdot \text{act}) := \text{lock}(\tau) \quad \text{otherwise} \\
& \quad \text{(pc, } \tau \text{)} \rightarrow t \text{ (pc, } \tau \cdot \text{act) } \\
\end{align*}
\]

Fig. 14. The SOS rules for the transition relation $\rightarrow$ among configurations.
**Assumption 3.** We assume that computations adhere to the control flow. Formally, this means $\text{ctrl}(\tau) \neq \emptyset$ for all $\tau \in \sem{P}_{\text{Adr}}^O$.

**Remark 2.** Assumption 3 requires that all primitive commands are wrapped inside atomics, that is, occur somewhere between beginAtomic and endAtomic.

**Definition B.52.** A computation $\tau \in \sem{P}_{\text{Adr}}^O$ induces a flat line program for thread $t$, denoted by $\flat_t(\tau)$, as follows:

$$
\begin{align*}
\flat_t(e) & := \text{skip} \\
\flat_t(\tau.\text{act}) & := \flat_t(\tau); \text{com} & \text{if } \text{act} = (t, \text{com}, \text{up}) \\
\flat_t(\tau.\text{act}) & := \flat_t(\tau) & \text{if } \text{act} = (t', \text{com}, \text{up}) \land t \neq t'
\end{align*}
$$

**Definition B.53.** A pointer $p$ has no valid alias in a computation $\tau$, denoted by $\text{noalias}_\tau(p)$, if $\text{seg} \neq m_\tau(p) \notin m_\tau(\text{valid}_\tau \setminus \{p\})$.

**Definition B.54.** Consider some $\tau \in \sem{P}_{\text{Adr}}^O$. Let $\text{inv}(\tau)$ have the prefix normal form $\exists r_1 \ldots \exists r_n. \phi$, where $\phi$ is quantifier-free. Let $r_n$ be the instance of angel $r$ resulting from the last allocation in $\tau$. The set of addresses possibly represented by angel $r$ after computation $\tau$ is

$$
\text{repr}_\tau(r) := \{ a \in \text{Adr} \mid \exists A_1, \ldots, A_n \subseteq \text{Adr}. a \in A_n \land (A_1, \ldots, A_n) \models \phi \}.
$$

**Definition B.55.** The locations reached in $O$ by a history $h$ wrt. to some thread $t$ and some address $a$ is defined by $\text{reach}_{O,t,a}(h) := \{ l \mid \exists \phi. (l_{\text{init}}, \phi) \bot (l, \phi) \land \phi(z_1) = t \land \phi(z_2) = a \}$ where $l_{\text{init}}$ is the initial location in $O$. For seq we define $\text{reach}_{O,t,a}(h) = \top$ to contain all locations of $O$. The definition of reach extends naturally to sets of histories.

**Lemma B.56.** If $\Gamma_1 \leadsto \Gamma_2$ and $\Gamma_2 \leadsto \Gamma_3$, then $\Gamma_1 \leadsto \Gamma_3$.

**Lemma B.57.** Consider $\vdash \Gamma_1 \text{ stmt } \{\Gamma_2\}$ and $(\text{stmt}, \tau) \rightarrow_{t} (\text{stmt}', \tau, \tau')$. Then there is $\Gamma$ such that $\vdash \Gamma_1 \flat_t(\tau') \{\Gamma\}$ and $\vdash \Gamma \text{ stmt}' \{\Gamma_2\}$.

**Lemma B.58.** Let $\vdash \{\Gamma_{\text{init}}\} P \{\Gamma\}$. Consider $(p c_{\text{init}}, e) \rightarrow^* (p c, \tau)$ and some thread $t$. Then there is $\Gamma_1, \Gamma_2$ with $\vdash \{\Gamma_{\text{init}}\} \flat_t(\tau) \{\Gamma_1\}$ and $\vdash \{\Gamma_1\} p c(t) \{\Gamma_2\}$.

**Lemma B.59.** Let $\tau.\text{act} \in \sem{P}_{\text{Adr}}^O$ and $t \neq \text{thrd}(\text{act})$. Let $\vdash \{\Gamma_{\text{init}}\} \flat_t(\tau) \{\Gamma\}$ and $x \in \text{PVar} \cup \text{AVar}$. Then $\emptyset \notin \Gamma(x)$ and $x \notin \text{local}_t \implies \Gamma(x) \cap \{L, S\} = \emptyset$.

**Lemma B.60.** Let $\tau.\text{act} \in \sem{P}_{\text{Adr}}^O$ and $t \neq \text{thrd}(\text{act}) \neq \bot$. Let $p \in \text{PVar} \cap \text{local}_t$. Then, $p \in \text{valid}_\tau$ implies $p \in \text{valid}_{\tau.\text{act}}$. Moreover, $\text{noalias}_{\tau}(p)$ implies $\text{noalias}_{\tau.\text{act}}(p)$.

**Lemma B.61.** Consider $\tau.\text{act} \in \sem{P}_{\text{Adr}}^O$. PRF with act $= (t, \oplus \text{inv} p = q, \text{up})$ and $\text{inv}(\tau.\text{act})$. Then, $\{p, q\} \cap \text{valid}_\tau \neq \emptyset$ implies $\{p, q\} \subseteq \text{valid}_{\tau.\text{act}}$.

**Lemma B.62.** Consider $\tau.\text{act} \in O[\sem{P}_{\text{Adr}}^O$. PRF with act $= (t, \oplus \text{inv} \text{active}(p), \text{up})$ and $\text{inv}(\tau.\text{act})$. Then, $p \in \text{valid}_{\tau.\text{act}}$ and $\text{reach}_{O,t,a}(\mathcal{H}(\tau.\text{act})) \subseteq \text{Loc}(A)$ for $a = m_{\tau.\text{act}}(p)$.

**Lemma B.63.** Consider $\tau.\text{act} \in O[\sem{P}_{\text{Adr}}^O$. PRF with act $= (t, \oplus \text{inv} \text{active}(r), \text{up})$ and $\text{inv}(\tau.\text{act})$. Then, $\text{repr}_{\tau.\text{act}}(r) \cap \text{freed}(\tau.\text{act}) = \emptyset$ and $\text{reach}_{O,t,a}(\mathcal{H}(\tau.\text{act})) \subseteq \text{Loc}(A)$ for all $a \in \text{repr}_{\tau.\text{act}}(r)$.
LEMMA B.64. Let $\tau \in O(P)_{Adr}^\omega$. Let $\Gamma, \Gamma'$ such that $\Gamma \sim \Gamma'$. Let $t$ be some thread. Let $p \in PVar$ and $a = m_r(p)$. Let $r \in AVar$ and $b \in \text{repr}_r(r)$. Then,

\begin{align*}
isValid(\Gamma(p)) & \implies p \in \text{valid}_r \quad \text{implies} \quad isValid(\Gamma'(p)) \implies p \in \text{valid}_r \\
isValid(\Gamma(r)) & \implies b \notin \text{freed}(\tau) \quad \text{implies} \quad isValid(\Gamma'(r)) \implies b \notin \text{freed}(\tau) \\
L \in \Gamma(p) & \implies noalias_s(p) \quad \text{implies} \quad L \in \Gamma'(p) \implies noalias_s(p) \\
reach_{O,t,a}(H(\tau)) & \subseteq \text{Loc}(\Gamma(p)) \quad \text{implies} \quad reach_{O,t,a}(H(\tau)) \subseteq \text{Loc}(\Gamma'(p)) \\
reach_{O,t,b}(H(\tau)) & \subseteq \text{Loc}(\Gamma(r)) \quad \text{implies} \quad reach_{O,t,b}(H(\tau)) \subseteq \text{Loc}(\Gamma'(r))
\end{align*}

LEMMA B.65. Assume $O$ supports elision, and $\text{inv}(P)_{Adr}^\omega$. Consider some thread $t$, some type environments $\Gamma$, and some $\tau \in O(P)_{Adr}^\omega$ PRF with $\text{inv}(\tau)$ and $\bot \{1_{init}\} \text{flat}_s(\tau) \{\Gamma\}$. Then, for every $p \in PVar$, we have $reach_{O,t,a}(H(\tau)) \subseteq \text{Loc}(\Gamma(p))$ and $\text{isValid}(\Gamma(p)) \implies p \in \text{valid}_r$.

LEMMA B.66. Let $O$ supports elision. If $\bot P$ and $\text{inv}(P)_{Adr}^\omega$, then $O(P)_{Adr}^\omega$ PRF and $\text{inv}(O(P)_{Adr}^\omega)$.

LEMMA B.67. Let $O$ supports elision. If $\bot P$ and $\text{inv}(P)_{Adr}^\omega$, $P_{Adr}^\omega$ does not perform double retires.

C PROOFS

C.1 Reduction

PROOF OF LEMMA B.28. Follows immediately from Assumption 1 as it guarantees that continuations of a history not accepted by $O$ are also not accepted. □

PROOF OF LEMMA B.29. Follows from [Meyer and Wolff 2018, Lemma D.5]. □

PROOF OF LEMMA B.30. Follows from [Meyer and Wolff 2018, Lemma D.7]. □

PROOF OF LEMMA B.31. Follows from definition. □

PROOF OF LEMMA B.32. Follows from [Meyer and Wolff 2018, Lemma D.15]. That the semantics from [Meyer and Wolff 2018] sets selectors to $\perp$ for free commands does not affect the result. □

PROOF OF LEMMA B.33. To the contrary, assume there is a shortest $\tau.act \in P_{Adr}^\omega$ with some address $a \in \text{freed}(\tau.act)$ and $a \in m_{r.act}(\text{valid}_{r.act})$. Note that $\tau.act$ is indeed the shortest such computation since the claim is vacuously true for $\epsilon$.

First, consider the case where we have $a \notin \text{freed}(\tau)$. Then, $act$ must execute the command $\text{free}(a)$. As a consequence, we get $pexp \notin \text{valid}_{r.act}$ for all $pexp$ with $m_r(pexp) = a$. So $a \notin m_{r.act}(\text{valid}_{r.act})$. Since this contradicts the assumption, we must have $a \in \text{freed}(\tau)$.

Now, consider the case where we have $a \in \text{freed}(\tau)$. By definition, there is some $pexp \in \text{valid}_{r.act}$ with $m_{r.act}(pexp) = a \neq \text{seg}$. We get $pexp \notin \text{valid}_r$ by minimality of $r.act$. That is, $act$ validates $pexp$. To do so, $act$ must be an assignment, an allocation, or an assertion:

- If $act$ is of the form $act = (t, pexp := qexp, up)$, then $qexp \in \text{valid}_r$ and $m_r(qexp) = a$ must hold in order to establish the desired properties of $pexp$. However, $m_r(qexp)$ leads to $qexp \notin \text{valid}_r$ by minimality of $r.act$. Hence, $act$ cannot be an assignment.
- If $act$ is of the form $act = (t, pexp := \text{malloc}, up)$, then $a \notin \text{freed}(r.act)$ by definition. Hence, $act$ cannot be an allocation targeting $pexp$.
- If $act$ is of the form $act = (t, p := \text{malloc}, up)$ with $m_{r.act}(p) = b$ and $pexp \equiv b\text{.next}$, then $m_{r.act}(pexp) = \text{seg-a}$. Hence, $act$ cannot be an allocation.
- If $act$ is of the form $act = (t, \text{assume } p = q, up)$, then $\text{wlog, } pexp \equiv p$ and $q \in \text{valid}_r$ and $a = m_{r.act}(pexp) = m_r(q)$ must hold. Again by minimality, we get $q \notin \text{valid}_r$ which contradicts the assumption. Hence, $act$ cannot be an assertion.
The above case distinction is complete and thus concludes the claim. □

Proof of Lemma B.34. Let \( \tau \in \mathcal{O}[[P]]_{Adr}^{m}, a \in (\text{fresh}(\tau) \cup \text{freed}(\tau)) \setminus \text{retired}(\tau) \), and \( b \in \text{fresh}(\tau) \). Let \( \mathcal{H}(\tau) = h \). We have \( \mathcal{F}_O(h, b)[b/a] = \mathcal{F}_O(h[b/a], a) \) according to [Meyer and Wolff 2018, Lemma D.26]. If \( a \in \text{freed}(\tau) \), then Definition B.15ii yields \( \mathcal{F}_O(h, a) \subsetneq \mathcal{F}_O(h[b/a], a) \). Thus, \( \mathcal{F}_O(h, a) \subsetneq \mathcal{F}_O(h, b)[b/a] \) as desired. Otherwise, we have \( a \in \text{fresh}(\tau) \). This means \( h[b/a] = h \). So, \( \mathcal{F}_O(h[b/a], a) = \mathcal{F}_O(h, a) \). Hence, \( \mathcal{F}_O(h, a) = \mathcal{F}_O(h, b)[b/a] \) as desired. □

Proof of Lemma B.35. Follows from [Meyer and Wolff 2018, Lemmas D.26, D.27 and D.28]. That the semantics from [Meyer and Wolff 2018] sets selectors to \( \perp \) for free commands does not affect the result. □

Proof of Lemma B.36. Follows from [Meyer and Wolff 2018, Proofs of Proposition C.14, Lemma C.16, and Lemma D.16]. □

Proof of Lemma B.37. Follows from [Meyer and Wolff 2018, Lemma D.9]. □

Proof of Lemma B.38. The claim holds for the empty computation \( \epsilon \). To the contrary, assume the claim does not hold. Then, there must be a shortest computation \( \tau \). act \( \in \mathcal{O}[[P]]_{Adr}^{m} \) such that \( \text{fresh}(\tau \text{. act}) \cap \text{retired}(\tau \text{. act}) \neq \emptyset \). Let \( a \in \text{fresh}(\tau \text{. act}) \cap \text{retired}(\tau \text{. act}) \). By minimality of \( \tau \). act, we must have \( a \notin \text{fresh}(\tau) \) or \( a \notin \text{retired}(\tau) \). If \( a \notin \text{fresh}(\tau) \), then we have \( a \notin \text{fresh}(\tau \text{. act}) \) by definition. Since this contradicts the assumption, we must have \( a \in \text{fresh}(\tau) \) and \( a \notin \text{retired}(\tau) \). To arrive at \( a \in \text{retired}(\tau \text{. act}) \), act must be of the form \( \text{act} = (t, \text{enter retire}(p), \text{up}) \) with \( m_r(p) = a \). By the contrapositive of Lemma B.37, we have \( a \notin \text{fresh}(\tau) \). As before, this gives \( a \notin \text{fresh}(\tau \text{. act}) \) and contradicts the assumption. □

Proof of Lemma B.39. The claim holds for the empty computation \( \epsilon \) by definition. Consider some \( \tau \). act \( \in \mathcal{O}[[P]]_{Adr}^{m} \) PRF with \( \text{act} = (t, \text{com}, \text{up}) \) such that for every \( q \text{exp} \in \text{PExp} \) we have \( q \text{exp} \notin \text{valid}_{\tau} \) implies \( m_r(q \text{exp}) \in \text{freed}(\tau) \) or \( q \text{exp} \notin \text{PVar} \land \{q \text{exp}\} \subsetneq \text{fresh}(\tau) \cup \text{freed}(\tau) \). Let \( p \text{exp} \in \text{PExp} \) be some pointer expression with \( p \text{exp} \notin \text{valid}_{\tau \text{. act}} \). We do a case distinction.

- Consider \( \text{com} \) being an assignment. If \( \text{com} \) does not contain \( p \text{exp} \) at the left-hand side, then \( p \text{exp} \notin \text{valid}_{\tau} \). Hence, we have either \( m_r(\text{act} p \text{exp}) = m_r(\text{act} p \text{exp}) \in \text{freed}(\tau) = \text{freed}(\tau \text{. act}) \) or \( p \text{exp} \notin \text{PVar} \land \{p \text{exp}\} \subsetneq \text{fresh}(\tau) \cup \text{freed}(\tau) = \text{freed}(\tau \text{. act}) \). Moreover, \( \text{com eq} p \text{exp} := q \text{exp} \). If \( q \text{exp} \in \text{PVar} \), then \( q \text{exp} \notin \text{valid}_{\tau} \). Thus, \( m_r(q \text{exp}) \in \text{freed}(\tau) \). We get \( m_r(\text{act} p \text{exp}) \in \text{freed}(\tau \text{. act}) \). Otherwise, \( q \text{exp eq} p \text{next} \) with \( m_r(p) = a \) and \( a \text{next eq} \text{valid}_{\tau} \).

- By Lemma B.37 we have \( a \notin \text{fresh}(\tau) \). So we get \( m_r(q \text{exp}) \notin \text{freed}(\tau) \) or \( a \notin \text{freed}(\tau) \). The latter cannot apply since Lemma B.33 gives \( p \notin \text{valid}_{\tau} \) which means \( \tau \text{. act} \) raises a pointer race contradicting the assumption. In the remaining case we get \( m_r(\text{act} p \text{exp}) \notin \text{freed}(\tau \text{. act}) \) as desired.

- Consider \( \text{com} \) being an assume, an @\text{inv}, an enter, or an exit. Then, we know that \( p \text{exp} \notin \text{valid}_{\tau} \). Let \( \text{com eq} p := \text{malloc} \). The update is of the form \( \text{up} = [p \mapsto a, \text{a.next eq seg, dots}] \) for some \( a \in \text{Adr} \). By the semantics, we have \( a \in \text{fresh}(\tau) \). We get \( \text{fresh}(\tau \text{. act}) = \text{fresh}(\tau) \setminus \{a\} \) and \( \text{freed}(\tau \text{. act}) = \text{freed}(\tau) \setminus \{a\} \). Since \( p \text{exp} \notin \text{valid}_{\tau \text{. act}} \), we have \( p \text{exp} \notin \{p, \text{a.next}\} \). So \( m_r(p \text{exp}) = m_r(\text{act} p \text{exp}) \). If \( m_r(p \text{exp}) \in \text{freed}(\tau) \) we get \( m_r(p \text{exp}) \notin \text{fresh}(\tau) \) and thus \( m_r(\text{act} p \text{exp}) \in \text{freed}(\tau \text{. act}) \). Otherwise, \( p \text{exp eq} \text{a.next} \) and \( b \in \text{fresh}(\tau) \cup \text{freed}(\tau) \) with \( a \neq b \). So we get the desired \( b \in \text{fresh}(\tau \text{. act}) \cup \text{freed}(\tau \text{. act}) \).

- Consider \( \text{com} \) being a free. Let \( \text{com eq} p := \text{free}(a) \). If \( p \text{exp} \in \text{valid}_{\tau} \), then we have \( m_r(p \text{exp}) = a \) or \( p \text{exp eq} \text{a.next} \) since \( \text{act} \) invalidates \( p \text{exp} \). We get either \( m_r(\text{act} p \text{exp}) \notin \text{freed}(\tau \text{. act}) \) or
\[ \text{pexp} \equiv a.\text{next} \land a \in \text{freed}(\tau.\text{act}). \text{Otherwise, we have pexp} \not\equiv \text{valid}_\tau. \text{If} \ m_\tau(\text{pexp}) \in \text{freed}(\tau.\text{act}), \text{then} \ m_{\tau.\text{act}}(\text{pexp}) \in \text{freed}(\tau.\text{act}). \text{Otherwise, pexp} \equiv b.\text{next} \land b \in \text{frehed}(\tau) \cup \text{freed}(\tau). \text{This gives} \ b \in \text{frehed}(\tau) \cup \text{freed}(\tau.\text{act}) \text{because} \ a = b \text{yields} \ b \in \text{freed}(\tau.\text{act}) \text{and} \ a \neq b \text{does not affect the freshness/freeness of} \ b. \]

This concludes the claim. \[\square\]

**Proof of Lemma B.40.** Follows from Lemma B.39. \[\square\]

**Proof of Lemma B.41.** By assumption we have

\[ \forall h \forall a, b. a \neq b \implies \mathcal{F}_O(h.\text{free}(a), b) = \mathcal{F}_O(h, b) \quad (A1) \]

\[ \forall h \forall a. \mathcal{F}_O(h.\text{free}(a), a) \subseteq \mathcal{F}_O(h, a) \quad (A2) \]

Consider some \( h.\text{free}(a) \). We show \( S(h.\text{free}(a)) \subseteq S(h) \) as this implies the claim. Towards a contradiction, assume the inclusion does not hold. That is, there is a shortest \( h' \in S(h.\text{free}(a)) \) with \( h' \not\in S(h) \). If \( \text{frees}(h') = \emptyset \), then we get \( h' \in \mathcal{F}_O(h.\text{free}(a), a) \). By Auxiliary (A2) we have \( h' \in \mathcal{F}_O(h, a) \). This means \( h' \in S(h) \) by definition. This contradicts the choice of \( h' \). So we must have \( \text{frees}(h') \neq \emptyset \).

Consider now \( \text{frees}(h') \neq \emptyset \). That is, there is a decomposition of \( h' \) of the form \( h' = h_1.\text{free}(b).h_2 \) with \( \text{frees}(h_2) = \emptyset \). We derive the following.

- We have \( h_1.\text{free}(b).h_2 \notin S(h) \). That is, \( h_1.\text{free}(b).h_2 \notin S(O) \). By definition, this means \( h_2 \notin \mathcal{F}_O(h.\text{free}(b), c) \) with \( c \neq b \). Now, Auxiliary (A1) yields \( h_2 \notin \mathcal{F}_O(h, h_1, c) \). Since \( \text{frees}(h_2) = \emptyset \), we must have \( h_1.\text{free}(b).h_2 \notin S(O) \). That is, we get \( h_1.\text{free}(b) \notin S(h) \).
- We have \( h_1.\text{free}(b).h_2 \in S(h.\text{free}(a)) \). So, \( h.\text{free}(a).h_1.\text{free}(b).h_2 \in S(O) \). By \( \text{frees}(h_2) \), we get \( h_2 \in \mathcal{F}_O(h.\text{free}(a), h_1.\text{free}(b), b) \). Then, Auxiliary (A2) yields \( h_2 \in \mathcal{F}_O(h.\text{free}(a).h_1, b) \).

So, \( h.\text{free}(a).h_1.h_2 \in S(O) \). That is, we get \( h_1.h_2 \in S(h.\text{free}(a)) \).

Altogether, this means we have \( h_1.h_2 \in S(h.\text{free}(a)) \) and \( h_1.h_2 \notin S(h) \) with \( h_1.h_2 \) being shorter than \( h_1.\text{free}(b).h_2 \). This contradicts the minimality of \( h' \) and thus concludes the claim. \[\square\]

**Proof of Lemma B.42.** Let \( a \in \text{Adr} \) and \( \varphi = \{ z_a \mapsto a \} \). The claim holds for \( \epsilon \). Towards a contradiction, assume there is a shortest \( \tau.\text{act} \in \mathcal{O}[\Psi]_{\text{Adr}}^\varnothing \) with \( (L_2, \varphi) \xrightarrow{\mathcal{H}(\tau.\text{act})} (L_3, \varphi) \) and \( a \notin \text{retired}(\tau.\text{act}) \). If \( \mathcal{H}(\tau.\text{act}) = \mathcal{H}(\tau) \), then we have \( \text{retired}(\tau.\text{act}) = \text{retired}(\tau) \). This contradicts the assumption that \( \tau.\text{act} \) is the shortest such computation. So \( \mathcal{H}(\tau.\text{act}) \) is of the form \( \mathcal{H}(\tau) = h.\text{evt} \) with \( h = \mathcal{H}(\tau) \). We do a case distinction on the state after \( \tau \).

- Consider \( (L_2, \varphi) \xrightarrow{h_3}(L_1, \varphi) \). By definition of \( O_{\text{Base}} \), there is no step \( (L_1, \varphi) \xrightarrow{\text{evt}} (L_3, \varphi) \). Hence, this case cannot apply.
- Consider \( (L_2, \varphi) \xrightarrow{h_4}(L_2, \varphi) \). Then we must have \( (L_2, \varphi) \xrightarrow{\text{evt}} (L_3, \varphi) \). This means \( \text{evt} = \text{retire}(t, a) \) for some thread \( t \). By definition, \( \text{act} = (t, \text{retire}(p), \emptyset) \) with \( m_\tau(p) = a \). Thus, \( a \in \text{retired}(\tau.\text{act}) \). This contradicts the assumption.
- Consider \( (L_2, \varphi) \xrightarrow{h_5}(L_3, \varphi) \). By minimality, we have \( a \in \text{retired}(\tau) \). To arrive at \( a \notin \text{retired}(\tau) \), we must have \( \text{evt} = \text{free}(a) \). This, however, leads to \( (L_3, \varphi) \xrightarrow{\text{evt}} (L_2, \varphi) \). So, \( (L_2, \varphi) \xrightarrow{\mathcal{H}(\tau.\text{act})} (L_2, \varphi) \).

This contradicts the assumption.

The above case distinction is complete and thus proves that \( (L_2, \varphi) \xrightarrow{\mathcal{H}(\tau)} (L_3, \varphi) \) implies \( a \in \text{retired}(\tau) \).

Consider now the reverse direction. To that end, consider some \( \tau \in \mathcal{O}[\Psi]_{\text{Adr}}^\varnothing \) and some \( a \notin \text{retired}(\tau) \). Using the contrapositive of the above, we get \( (L_2, \varphi) \xrightarrow{\mathcal{H}(\tau)} (l, \varphi) \) with \( l \neq L_3 \). By Assumption 1, \( l \neq L_1 \) as for otherwise \( \tau \notin \mathcal{O}[\Psi]_{\text{Adr}}^\varnothing \). Hence, \( l = L_2 \) must hold. This establishes the first equivalence. The second equivalence follow analogously. The remaining property follows from the second equivalence together with the fact that \( a \in \text{active}(\tau) \) implies \( a \notin \text{retired}(\tau) \). \[\square\]
we have to consider one additional case, namely the case where $\tau = \sigma$. The case distinction is complete and thus concludes the claim.

Proof of Lemma B.43. Let $\tau.\text{act} \in O[P]_{\text{adr}}^\sigma$ with $\text{act} = (t, \text{free}(a), \text{up})$. Let $\varphi = \{ z_a \mapsto a \}$. We have $\mathcal{H}(\tau.\text{act}) = h.\text{free}(a)$ with $h = \mathcal{H}(\tau)$. By definition, $h.\text{free}(a) \in S(O_{\text{Base}})$. So we must have $(L_2, \varphi).\mathcal{L}(L_3, \varphi)$ as for otherwise $\text{free}(a)$ would take $O_{\text{Base}}$ to $L_2$ and thus give $\tau.\text{act} \notin O[P]_{\text{adr}}^\varphi$. Now Lemma B.42 yields the desired $a \in \text{retired}(\tau)$. \hfill $\Box$

Proof of Lemma B.44. For $\tau = \epsilon$ we choose $\epsilon = \sigma \in [P]_{\text{adr}}^\varphi$. Then, $\sigma$ satisfies the desired properties. Consider now $\tau.\text{act} \in O[P]_{\text{adr}}^\varphi$. Assume we already constructed $\sigma \in [P]_{\text{adr}}^\varphi$ with:

(P1) $\text{ctrl}(\tau) = \text{ctrl}(\sigma)$,

(P2) $m_\tau = m_\sigma$,

(P3) $\text{fresh}(\tau) \subseteq \text{fresh}(\sigma)$,

(P4) $\text{retired}(\tau) \subseteq \text{retired}(\sigma)$, and

(P5) $\text{freed}(\tau) \subseteq \text{retired}(\sigma)$.

First, assume $\text{com}(\text{act}) \neq \text{free}(a)$. We get $\sigma.\text{act} \in [P]_{\text{adr}}^\varphi$. The reason for this is that $\sigma$:

- performs the same updates in assignments due to Property (P2),
- allows for the same assume commands due to Property (P2),
- emits the same events due to Property (P2),
- allows for the same malloc commands due to Property (P3), and
- nothing can be removed from $\text{retired}(\sigma)$.

Moreover, $\sigma$ satisfies the desired properties. This is because the same update is applied after $\tau$ and $\sigma$. To see that $\text{inv}(\sigma.\text{act}) \implies \text{inv}(\tau.\text{act})$, let $\text{act}$ execute an annotation. There are two cases:

- Consider $\text{com}(\text{act})$ is of the form $\oplus \text{inv} \text{angel} r$. By definition, $\text{inv}(\tau.\text{act}) = \exists r. F_\sigma$ and $\text{inv}(\sigma.\text{act}) = \exists r. F_\varphi$. By induction, we get $\text{inv}(\sigma.\text{act}) \implies \text{inv}(\tau.\text{act})$.

- Consider $\text{com}(\text{act}) \neq \oplus \text{inv} \text{angel} r$. By definition then, $\text{inv}(\tau.\text{act}) = \text{inv}(\tau) \land F_\sigma$ and $\text{inv}(\sigma.\text{act}) = \text{inv}(\sigma) \land F_\varphi$. If $\text{com}(\text{act}) \notin \{ \oplus \text{inv} \text{active}(p), \oplus \text{inv} \text{active}(r) \}$, we have $F_\sigma \equiv F_\varphi$ by Property (P2). Otherwise, we have $F_\sigma \implies F_\varphi$ because Properties (P4) and (P5) gives $\text{active}(\sigma) \subseteq \text{active}(\tau)$. By induction, we get $\text{inv}(\sigma.\text{act}) \implies \text{inv}(\tau.\text{act})$.

The case distinction is complete and thus concludes the claim.

If $\text{com}(\text{act}) \equiv \text{free}(a)$, then $\sigma$ already has the desired properties. This is the case because $\text{free}(a)$ does not affect the memory nor the control. The $\text{free}(a)$ may remove $a$ from $\text{fresh}(\tau)$, thus maintaining $\text{fresh}(\tau) \subseteq \text{fresh}(\sigma)$. Similarly, we maintain $\text{retired}(\tau.\text{act}) \subseteq \text{retired}(\sigma)$. Last, we have $\text{freed}(\tau.\text{act}) = \text{freed}(\tau) \cup \{ a \}$. It remains to show that $a \in \text{retired}(\sigma)$. This follows from Lemma B.43 together with $\text{retired}(\tau) \subseteq \text{retired}(\sigma)$ from induction. \hfill $\Box$

Proof of Theorem B.45. Follows from Lemmas B.36 and B.44. \hfill $\Box$

Proof of Theorem 4.1. Follows from Theorem B.45. \hfill $\Box$

Proof of Theorem B.21. Follows from Lemmas B.36 and B.44. Here, we rely on a generalization of Lemma B.36 that assumes only RPRF in its premise. To prove the generalization of that lemma, we have to consider one additional case, namely the case where $\tau.\text{act} \in O[P]_{\text{adr}}^\varphi$ is a PR but RPRF. (During the proof, we have already constructed $\sigma \in O[P]_{\text{adr}}^\varphi$ with $\tau \sim \sigma$.) That is, $\text{act}$ is of the form $\text{assume} p = q$ such that, without loss of generality, $p \notin \text{valid}_\tau$ and $\text{free}(a) \in \mathcal{H}(\tau)$ where $a = m_\tau(q)$. This means $\tau.\text{act} \in O[P]_{\text{adr}}^\sigma\setminus\{a\}$. So $q \in \text{valid}_\tau$. By [Meyer and Wolff 2018, Lemma D.15] we have $m_\tau(p) \neq a = m_\varphi(q)$. Hence, the case cannot apply. (The remaining cases are identical to the non-generalized version, Lemma B.36). \hfill $\Box$
C.2 Type System

Proof of Lemma B.56. Immediately follows from definition. □

Proof of Lemma B.57. We do an induction over the derivation depth of ⊢ {Γ₁} stmt {Γ₂}.

IB: The derivation is due to one rule application. This means the derivation is not due to one of: (INFER), (SEQ), (CHOICE), or (LOOP). For the remaining, applicable rules we have stmt ≡ com and (com, τ) →₁ (skip, τ.τ'). Thus, flatₜ(τ') = stmt. We immediately get ⊢ {Γ₁} flatₜ(τ') {Γ₂}. Moreover, ⊢ {Γ₂} skip {Γ₂} holds by definition. That is, we choose Γ = Γ₂ as it has the desired properties.

IH: If ⊢ {Γ₁} stmt₁ {Γ₂} and (stmt, τ) →₁ (stmt', τ.τ') hold, then there is some Γ with ⊢ {Γ₁} flatₜ(τ') {Γ} and ⊢ {Γ} stmt₁ {Γ₂}.

IS: Consider a composed derivation of ⊢ {Γ₁} stmt {Γ₂}. Let (stmt, τ) →₁ (stmt', τ.τ'). We do a case distinction on the first rule of the derivation.

Rule (SEQ), part 1. Consider stmt ≡ skip; stmt₂. Then, stmt' = stmt₂ and τ' = ∅. Moreover, there exists some Γ such that ⊢ {Γ} skip {Γ} and ⊢ {Γ} stmt₂ {Γ₂} due to the type rules. Note that flatₜ(τ') = skip. That is, Γ has the desired properties.

Rule (SEQ), part 2. Consider stmt ≡ stmt₁; stmt₂. Let (stmt₁, τ) →₁ (stmt', τ.τ''). By definition, stmt' = stmt₁; stmt₂ and τ' = τ''. The type rules give some Γ with ⊢ {Γ₁} stmt₁ {Γ₁'} and ⊢ {Γ'} stmt₂ {Γ₂}. By induction, there is Γ with ⊢ {Γ₁} flatₜ(τ') {Γ'} and ⊢ {Γ} stmt₁ {Γ'}. The latter gives ⊢ {Γ} stmt₁; stmt₂ {Γ₂}. That is, Γ has the desired properties.

Rule (CHOICE). We have stmt ≡ stmt₁ ⊕ stmt₂. Then, τ' = ∅ and stmt' = stmtᵢ for some i ∈ {1, 2}. Due to the type rules, we have ⊢ {Γ₁} stmt₁ {Γ₂}. Moreover, flatₜ(τ') = skip gives ⊢ {Γ₁} flatₜ(τ') {Γ₁}. That is, Γ = Γ₁ is an adequate choice with the desired properties.

Rule (LOOP). We have stmt ≡ stmtᵢ. Then, τ' = ∅ and stmt' = stmtᵢ for some i ∈ {1, 2}. Due to the type rules, we have ⊢ {Γ₁} stmtᵢ {Γ₂}. Moreover, flatₜ(τ') = skip gives ⊢ {Γ₁} flatₜ(τ') {Γ₁}. That is, Γ = Γ₁ is an adequate choice with the desired properties.

Rule (INFER). There are type environments Γ₁ and Γᵢ such that Γ₁ ⊢ Γᵢ and Γᵢ ⊢ Γ₂. By induction, there is Γ with ⊢ {Γ₃} flatₜ(τ') {Γ} and ⊢ {Γ} stmtᵢ {Γ₄}. Applying Rule (INFER) we get ⊢ {Γ₁} flatₜ(τ') {Γ} and ⊢ {Γ} stmtᵢ {Γ₂} as desired.

The above induction concludes the claim. □

Proof of Lemma B.58. Let ⊢ {Γᵢᵢᵢ} P {Γ}. We proceed by induction over the SOS transitions.

IB: We have (pcᵢᵢᵢ, e) →₀ (pc, τ). That is, pc = pcᵢᵢᵢ and τ = τ. Consider some thread t. We have flatₜ(τ) = skip and pc(t) = P[tᵢᵢᵢ]. The former gives ⊢ {Γᵢᵢᵢ} flatₜ(τ) {Γᵢᵢᵢ}. The latter gives ⊢ {Γᵢᵢᵢ} pc(t) {Γ} due to the premise. So we can choose Γᵢᵢᵢ = Γᵢᵢᵢ and Γ₂ = Γ.

IH: Let the claim hold for sequences of up to n steps.

IS: Consider now (pcᵢᵢᵢ, e) →ₙ (pc, τ) →ₙ (pcᵢᵢᵢ, τ.τ'). Let t ≠ ⊥ be some arbitrary thread. By induction, there are Γᵢᵢᵢ, Γ₂ with

\[ ⊢ \{Γᵢᵢᵢ\} flatₜ(τ) \{Γᵢᵢᵢ\} \quad \text{and} \quad ⊢ \{Γᵢᵢᵢ\} pc(t) \{Γ₂\}. \]

First, assume t ≠ t'. Then, flatₜ(τ.act) = flatₜ(τ) and pcᵢᵢᵢ(t) = pc(t). Thus, the claim follows immediately by induction. So consider t = t' now. We have (pc(t), τ) →ₙ (pcᵢᵢᵢ(t), τ.τ') by definition. Lemma B.57 yields Γᵢᵢᵢ with

\[ ⊢ \{Γᵢᵢᵢ\} flatₜ(τ) \{Γᵢᵢᵢ\} \quad \text{and} \quad ⊢ \{Γᵢᵢᵢ\} pcᵢᵢᵢ(t) \{Γ₂\}. \]

Altogether, we get the desired:

\[ ⊢ \{Γᵢᵢᵢ\} flatₜ(τ.act) \{Γᵢᵢᵢ\} \quad \text{and} \quad ⊢ \{Γᵢᵢᵢ\} pcᵢᵢᵢ(t) \{Γ₂\}. \]
The above induction concludes the claim. □

Proof of Lemma B.59. Let $\tau.\text{act} \in \left[\left[P\right]\right]_{\text{Adr}}^\|$ and $t, t'$ threads with $t \neq t' = \text{thrd}(\text{act})$. Consider some $\Gamma \vdash \{\Gamma^{(t)}\} \text{flat}_t(\tau) \{\Gamma\}$ and $x \in P\text{Var} \cup A\text{Var}$. We have $\text{lock}(\tau) = \{t'\}$ or $\text{lock}(\tau..\text{act}) = \{t'\}$. Hence, $t$ has not yet contributed any actions to $\tau$ or it has finished an atomic section. We do a case distinction.

- Consider the case $\text{flat}_t(\tau) = \text{skip}$. By the type rules there is $\Gamma'$ with:
  \[
  \Gamma^{(t)}_{\text{init}} \leadsto \Gamma' \quad \vdash \{\Gamma'\} \text{skip} \{\Gamma'\} \quad \Gamma' \leadsto \Gamma
  \]
  By definition, $\Gamma^{(t)}_{\text{init}}(x) = \emptyset$. So $\neg is\text{Valid}(\Gamma^{(t)}_{\text{init}}(x))$. Hence, $\neg is\text{Valid}(\Gamma'(x))$ and $\neg is\text{Valid}(\Gamma(x))$ follow from the definition of type inference. So we conclude $\Gamma(x) \cap \{A, L, S\} = \emptyset$.

- Consider the case $\text{flat}_t(\tau.\text{act}) = \text{stmt}; \text{endAtomic}$ for some statement $\text{stmt}$. By the typing rules there are $\Gamma_1, \Gamma_2, \Gamma_3$ with:
  \[
  \vdash \{\Gamma^{(t)}_{\text{init}}\} \text{stmt} \{\Gamma_1\} \quad \Gamma_1 \leadsto \Gamma_2 \quad \vdash \{\Gamma_2\} \text{endAtomic} \{\Gamma_3\} \quad \Gamma_3 \leadsto \Gamma
  \]
  where the derivation $\vdash \{\Gamma_2\} \text{endAtomic} \{\Gamma_3\}$ is due to Rule (END). This means, $\Gamma_3 = \text{rm}(\Gamma_2)$. By definition, $A \notin \Gamma_1(x)$. Hence, type inference provides $A \notin \Gamma(p)$ as desired.

Now, consider the case $p \notin \text{local}_t$. There are two cases. First, assume $p \in \text{shared}$. $\Gamma_3(p) = \emptyset$ by definition. Second, assume $p \notin \text{shared}$. That is, $x$ is local to another thread $t'' \neq t: p \in \text{local}_{t''}$. Then, the claim follows because the initial type binding does not contain local pointers of other threads and the type rules never add type bindings.

The above case distinction is complete and concludes the claim thus. □

Proof of Lemmas B.60 and B.60. Let $\tau.\text{act} \in \left[\left[P\right]\right]_{\text{Adr}}^\|$ and $t, t'$ threads with $t \neq t' = \text{thrd}(\text{act}) \neq \perp$. Let $p \in P\text{Var} \cap \text{local}_t$. By definition, $\text{local}_t \cap \text{local}_{t'} = \emptyset$. Due to the semantics, $p$ does not occur in $\text{com}(\text{act})$. Hence, $p \in \text{valid}_t \iff p \in \text{valid}_{t.\text{act}}$. Moreover, $m_r(p) = m_r.\text{act}(p)$. So every valid alias created by $\text{act}$ requires a valid alias in $t$. This is not possible since $\text{noalias}_t(p)$.

Proof of Lemma B.61. Let $\tau.\text{act} \in \left[\left[P\right]\right]_{\text{Adr}}^\|$ PRF with $\text{act} = (t, \odot \text{inv} \ p = q, \odot)$ and $\text{inv}(\tau.\text{act})$. The latter gives $m_r(p) = m_r(q)$. Towards a contradiction, assume the claim does not hold. Wlog. $p \notin \text{valid}_t$ and $q \in \text{valid}_t$. Lemma B.32 gives $m_r(p) \neq m_r(q)$. This contradicts the premise and thus concludes the claim. □

Proof of Lemma B.62. Let $\tau.\text{act} \in \left[\left[P\right]\right]_{\text{Adr}}^\|$ PRF with $\text{act} = (t, \odot \text{inv} \ \text{active}(p), \odot \text{up})$ and $\text{inv}(\tau.\text{act})$. By definition, this means $m_r(p) \in \text{active}(\tau)$. That is, $m_r(p) \notin \text{freed}(\tau)$. By the contrapositive of Lemma B.40: $p \in \text{valid}_t$ and $p \in \text{valid}_{t.\text{act}}$ by definition. Moreover, we get $m_r.\text{act}(p) \in \text{active}(\tau.\text{act})$. Hence, the remaining property follows from Lemma B.42. □

Proof of Lemma B.63. Let $\tau.\text{act} \in \left[\left[P\right]\right]_{\text{Adr}}^\|$ PRF with $\text{act} = (t, \odot \text{inv} \ \text{active}(r), \odot \text{up})$ and $\text{inv}(\tau.\text{act})$. By definition, we have $\text{repr}_r(r) \subseteq \text{active}(\tau)$. Hence, $\text{repr}_r(r) \cap \text{freed}(\tau.\text{act}) = \emptyset$. Moreover, we have $\text{repr}_{r.\text{act}}(r) \subseteq \text{active}(\tau.\text{act})$ by definition. Let $a \in \text{repr}_{r.\text{act}}(r)$. This means $a \in \text{active}(\tau.\text{act})$. Then, the remaining property follows from Lemma B.42. □

Proof of Lemma B.64. Let $\tau \in \text{O}[\left[P\right]\text{Adr}]$. Let $\Gamma, \Gamma'$ be two type environments with $\Gamma \leadsto \Gamma'$. Let $p \in P\text{Var}$ be a pointer with $a = m_r(p)$. Let $r \in A\text{Var}$ a ghost variable and $b \in \text{repr}_r(r)$. Consider the
possible assumptions:

\[
\begin{align*}
\text{isValid}(\Gamma(p)) & \implies p \in \text{valid}_r & (1) \\
\text{isValid}(\Gamma(r)) & \implies b \notin \text{freed}(r) & (2) \\
L \in \Gamma(p) & \implies \text{noalias}_r(p) & (3) \\
\text{reach}_{O,t,a}(\mathcal{H}(\tau)) & \subseteq \text{Loc}(\Gamma(p)) & (4) \\
\text{reach}_{O,t,b}(\mathcal{H}(\tau)) & \subseteq \text{Loc}(\Gamma(r)) & (5)
\end{align*}
\]

The definition of \( \Gamma \leadsto \Gamma' \) gives:

\[
\begin{align*}
\text{isValid}(\Gamma'(p)) & \implies \text{isValid}(\Gamma(p)) & (6) \\
\text{isValid}(\Gamma'(r)) & \implies \text{isValid}(\Gamma(r)) & (7) \\
L \in \Gamma'(p) & \implies L \in \Gamma(p) & (8) \\
\text{Loc}(\Gamma(p)) & \subseteq \text{Loc}(\Gamma'(p)) & (9) \\
\text{Loc}(\Gamma(r)) & \subseteq \text{Loc}(\Gamma'(r)) & (10)
\end{align*}
\]

Then, we combine

- If (1) holds, then (6) gives \( \text{isValid}(\Gamma'(p)) \implies p \in \text{valid}_r \),
- If (2) holds, then (7) gives \( \text{isValid}(\Gamma'(r)) \implies b \notin \text{freed}(r) \),
- If (3) holds, then (8) gives \( L \in \Gamma'(p) \implies \text{noalias}_r(p) \), and
- If (4) holds, then (9) gives \( \text{reach}_{O,t,a}(\mathcal{H}(\tau)) \subseteq \text{Loc}(\Gamma'(p)) \).
- If (5) holds, then (10) gives \( \text{reach}_{O,t,b}(\mathcal{H}(\tau)) \subseteq \text{Loc}(\Gamma'(r)) \).

This concludes the claim. \( \square \)

**Proof of Lemma B.65.** Let \( \tau \in O\mathbb{P}^\mathbb{P}_{\mathit{Addr}} \). We show:

\[
\text{freed}(\tau) \cap \text{retired}(\tau) = \emptyset
\]

and \( \forall t \forall \Gamma. \vdash \{ \Gamma_{\text{init}}[\tau] \} \text{flat}_t(\tau) \{ \Gamma \} \implies \forall p, r. \left( \begin{array}{c}
\text{reach}_{O,t,m_{\tau}(\mathcal{H}(\tau))} \subseteq \text{Loc}(\Gamma(p)) \\
\wedge \text{isValid}(\Gamma(p)) \implies p \in \text{valid}_r \\
\wedge L \in \Gamma(p) \implies \text{noalias}_r(p) \\
\wedge \forall a \in \text{repr}_r(r). \text{reach}_{O,t,a}(\mathcal{H}(\tau)) \subseteq \text{Loc}(\Gamma(r)) \\
\wedge \text{isValid}(\Gamma(r)) \implies \text{repr}_r(r) \cap \text{freed}(\tau) = \emptyset
\end{array} \right) \)

We proceed by induction over the structure of \( \tau \).

**IB:** Let \( \tau = \epsilon \). Let \( t \) be some thread and let \( \Gamma \) be some type environment such that \( \vdash \{ \Gamma_{\text{init}}[\tau] \} \text{flat}_t(\tau) \{ \Gamma \} \). Note that \( \text{flat}_t(\tau) = \text{skip} \). By definition, \( \text{freed}(\tau) \cap \text{retired}(\tau) = \emptyset \). Consider some thread \( t \), some \( p \in \mathit{PVar} \) and some \( r \in \mathit{AVar} \). By definition, \( p \in \text{valid}_r \). This gives the desired implication \( \text{isValid}(\Gamma(p)) \implies p \in \text{valid}_r \). By the type rules we have:

\[
\vdash \{ \Gamma_{\text{init}}[\tau] \} \text{skip} \{ \Gamma_{\text{init}}[\tau] \} \quad \Gamma_{\text{init}}[\tau], \epsilon \leadsto \Gamma
\]

Since \( L \notin \Gamma_{\text{init}}[\tau] \), we get \( L \notin \Gamma(p) \) by the definition of type inference. So we satisfy the implication \( L \in \Gamma(p) \implies \text{noalias}_r(p) \). Moreover, \( \text{freed}(\tau) = \emptyset \). So \( \text{isValid}(\Gamma(r)) \implies a \notin \text{freed}(\tau) \) is satisfied for every \( a \in \text{Addr} \) as well. By Lemma B.56 we have \( \Gamma_{\text{init}}[\tau] \leadsto \Gamma \). That is, \( \text{Loc}(\Gamma_{\text{init}}[\tau]) \subseteq \text{Loc}(\Gamma(p)) \). By definition, \( \Gamma_{\text{init}}[\tau] = \emptyset \). That is, \( \text{Loc}(\Gamma_{\text{init}}[\tau]) = \top \times \top \). Consequently, \( \text{reach}_{O,t,m_{\tau}(\mathcal{H}(\tau))} \subseteq \text{Loc}(\Gamma_{\text{init}}[\tau]) \). Similarly for \( r \). Altogether, this concludes the base case.
IH: Let the claim hold for \( \tau \).

IS: Consider \( \tau' = \tau.\text{act} \) with \( \text{act} = (t', \text{com}, \text{up}) \), \( \tau.\text{act} \) PRF, and \( \text{inv}(\tau.\text{act}) \). Let \( t \) be some arbitrary thread we establish the claim for. We do a case distinction on \( t' \).

Ad \( t = t' \neq \bot \). We have

\[
\text{flat}_t(\tau.\text{act}) = \text{flat}_t(\tau); \text{com} \quad \text{and} \quad \text{freen}(\tau.\text{act}) \subseteq \text{freen}(\tau).
\]

Assume that \( \tau.\text{act} \) can be typed for \( t \) as nothing needs to be shown otherwise. That is, assume there are \( \Gamma_3 \) such that

\[
\vdash \{ \Gamma_3 \} \text{flat}_t(\tau.\text{act}) \{ \Gamma_3 \}.
\]

Due to the type rules and the above equality, we know that there are some \( \Gamma_1, \Gamma_2 \) such that:

\[
\vdash \{ \Gamma_1 \} \text{flat}(\tau) \{ \Gamma_0 \} \quad \Gamma_0 \rightsquigarrow \Gamma_1 \quad \vdash \{ \Gamma_1 \} \text{com} \{ \Gamma_2 \} \quad \Gamma_2 \rightsquigarrow \Gamma_3
\]

where \( \vdash \{ \Gamma_1 \} \text{com} \{ \Gamma_2 \} \) is derived by neither Rule (SEQ) nor Rule (CHOICE) nor Rule (LOOP) nor Rule (INFER). By induction, the claim holds for \( \Gamma_0 \). So by Lemma B.64 the claim also holds for \( \Gamma_1 \). If the claim holds for \( \Gamma_2 \), then the claim follow for \( \Gamma_3 \) from Lemma B.64 again. So it remains to show that the claim holds for \( \Gamma_2 \) relying on \( \Gamma_1 \). We do a case distinction over the type rules applied for the derivation \( \vdash \{ \Gamma_1 \} \text{com} \{ \Gamma_2 \} \). To that end, let \( p \in \text{PVar} \) be some arbitrary pointer variable and let \( r \in \text{AVar} \) be some arbitrary angel. Let \( m_\tau(p) = c_p \) and let \( c_r \in \text{repr}_\tau(r) \).

\begin{itemize}
  \item \textbf{Case Rule (BEGIN).}
  \begin{itemize}
    \item By definition, we have \( \Gamma_2 = \Gamma_1 \), \( m_\tau = m_\tau.\text{act} \), \( \text{valid}_\tau = \text{valid}_\tau.\text{act} \), \( \text{freen}(\tau) = \text{freen}(\tau.\text{act}) \), \( \text{repr}_\tau = \text{repr}_\tau.\text{act} \), and \( \text{H}(\tau) = \text{H}(\tau.\text{act}) \). Hence, the claim follows by induction.
  \end{itemize}

  \item \textbf{Case Rule (END).}
  \begin{itemize}
    \item By definition, we have \( \Gamma_2 = \text{rm}(\Gamma_1) \). By definition, \( \Gamma_2(p) \subseteq \Gamma_1(p) \) and \( \Gamma_2(r) \subseteq \Gamma_1(r) \). This means we have \( \text{Loc}(\Gamma_2(p)) \supseteq \text{Loc}(\Gamma_1(p)) \) and \( \text{Loc}(\Gamma_2(r)) \supseteq \text{Loc}(\Gamma_1(r)) \). As in the previous case, we have \( m_\tau = m_\tau.\text{act} \), \( \text{valid}_\tau = \text{valid}_\tau.\text{act} \), \( \text{freen}(\tau) = \text{freen}(\tau.\text{act}) \), \( \text{repr}_\tau = \text{repr}_\tau.\text{act} \), and \( \text{H}(\tau) = \text{H}(\tau.\text{act}) \). So the claim follows by induction.
  \end{itemize}

  \item \textbf{Case Rule (ASSIGN1).}
  \begin{itemize}
    \item We have \( \text{freen}(\tau) = \text{freen}(\tau.\text{act}) \) and \( \text{inv}(\tau) \equiv \text{inv}(\tau.\text{act}) \). Hence, Property (G5) holds by induction. If \( \ell \in \Gamma_2(p) \), then \( p \) does not appear in \( \text{com} \) by definition of Rule (ASSIGN1). Hence, no alias of \( p \) is created by \( \text{com} \) and Property (G4) continues to hold by induction. If \( \text{isValid}(\Gamma_2) \) then there are two cases. First, \( \text{com} \equiv p \equiv q \). Then, \( \Gamma_2(p) = \Gamma_1(q) \setminus \{ \ell \} \). Hence, \( q \in \text{valid}_\tau \) by induction. This leads to \( p \in \text{valid}_\tau.\text{act} \) as desired. Second, \( p \) is not assigned to by \( \text{com} \). Then, \( \Gamma_2(p) \subseteq \Gamma_1(p) \). Hence, \( p \in \text{valid}_\tau \) by induction and \( p \in \text{valid}_\tau.\text{act} \) thus. This concludes Property (G3). Note that \( \text{H}(\tau.\text{act}) = \text{H}(\tau) \). Property (G2) remains to hold by induction since \( \tau \) is not affected by \( \text{com} \). It remains to establish Property (G1). If \( p \) does not occur in \( \text{com} \), nothing needs to be show. So assume \( p \) occurs in \( \text{com} \). In the first case, \( p \) occurs on the right-hand side of the assignment in \( \text{com} \). Then, \( \Gamma_2(p) = \Gamma_1(p) \setminus \{ \ell \} \). That is, \( \text{Loc}(\Gamma_1(p)) \subseteq \text{Loc}(\Gamma_2(p)) \). Then, Property (G1) follows by induction. Otherwise, \( p \) appears on the left-hand side of
the assignment in $com$. So $com \equiv p := q$ for some $q$. Then, $\Gamma_2(p) = \Gamma_1(q) \setminus \{L\}$. Moreover, $m_{\tau,act}(p) = m_{\tau}(q) = c_p$. By induction, we have $reach_{O,t,c_p}(H(\tau)) \subseteq Loc(\Gamma_1(q))$. Hence, $reach_{O,t,c_p}(H(\tau)) \subseteq Loc(\Gamma_1(q) \setminus \{L\})$. We get the desired $reach_{O,t,c_p}(H(\tau,act)) \subseteq Loc(\Gamma_2(q))$ by definition.

**Case Rule** (ASSIGN2).

Analogous to the previous case for (ASSIGN1).

**Case Rule** (ASSIGN3).

Analogous to the previous case for (ASSIGN1).

**Case Rule** (ASSIGN4),(ASSIGN5),(ASSIGN6),(ASSUME2).

We have $\Gamma_2 = \Gamma_1$, $m_{\tau} = m_{\tau,act}$, $repr_{\tau} = repr_{\tau,act}$, $valid_{\tau} = valid_{\tau,act}$, $freed(\tau) = freed(\tau,act)$, and $H(\tau) = H(\tau,act)$. Hence, the claim follows by induction.

**Case Rule** (ASSUME1).

We have $freed(\tau) = freed(\tau,act)$ and $inv(\tau) \equiv inv(\tau,act)$. Hence, Property (G5) holds by induction. If $L \in \Gamma_2(p)$, then $L \in \Gamma_1(p)$ due to the type rule. This means $noalias_{\tau}(p)$. Note that $m_{\tau} = m_{\tau,act}$. Moreover, since $\tau,act$ is PRF we know that the pointers in $com$ are valid. Hence, $valid_{\tau} = valid_{\tau,act}$. So we get $noalias_{\tau,act}(p)$ by definition. This establishes Property (G4).

If $isValid(\Gamma_1(p))$, then there are two cases. First, $isValid(\Gamma_1(p))$ holds. This means we have $p \in valid_{\tau}$. As stated above, this results in $p \in valid_{\tau,act}$. Second, $\neg isValid(\Gamma_1(p))$ holds. Then, $p$ is validated by $com$. For this to happen, $p$ must appear in $com$. Since $\tau,act$ is assumed to be PRF, we know $p \in valid_{\tau}$ must hold. So $p \in valid_{\tau,act}$ as before. This gives Property (G3). Note that we have $H(\tau,act) = H(\tau)$ and $repr_{\tau} = repr_{\tau,act}$. So it remains to establish Property (G2) continues to hold by induction since $r$ is not affected. It remains to establish Property (G1). If $p$ does not occur in $com$ nothing needs to be show. So assume $p$ appears in $com$. Wlog. $com$ is of the form $com \equiv assume p = q$. Due to the type rule, we have $\Gamma_2(p) = \Gamma_1(p) \setminus \{L\}$. By the semantics, we have $c_p = m_{\tau,act}(p) = m_{\tau}(p) = m_{\tau}(q) = m_{\tau,act}(q)$. So by induction, $reach_{O,t,c_p}(H(\tau)) \subseteq Loc(\Gamma_1(p)) \cap Loc(\Gamma_1(p)) = Loc(\Gamma_1(p) \wedge \Gamma_2(p)) = Loc(\Gamma_2(p))$. This concludes Property (G1).

**Case Rule** (EQUAL).

If $isValid(\Gamma_1(p))$, then there are two cases. First, $isValid(\Gamma_1(p))$ holds. This means we have $p \in valid_{\tau}$ by induction. Then, $p \in valid_{\tau,act}$ because $valid_{\tau} = valid_{\tau,act}$ by definition. Second, $\neg isValid(\Gamma_1(p))$ holds. Then, $p$ is validated by $com$. For this to happen, $com$ must be of the form $com \equiv @inv p = q$ with $isValid(q)$. By induction, we have $q \in valid_{\tau}$. Then, Lemma B.61 gives $p \in valid_{\tau}$. Hence, $p \in valid_{\tau,act}$ as before. This concludes Property (G3). The remaining properties follow analogously to the previous case for (ASSUME1). For Property (G1) note that $repr_{\tau} \iff repr_{\tau,act}$ by definition together with the fact that $inv(\tau,act)$ holds.

**Case Rule** (ACTIVE) for pointers.

If $isValid(\Gamma_2(p))$, then there are two cases. First, $isValid(\Gamma_1(p))$ holds. This means $p \in valid_{\tau}$ by induction. Then, $p \in valid_{\tau,act}$ because $valid_{\tau} = valid_{\tau,act}$. Second, $\neg isValid(\Gamma_1(p))$ holds. Then, $p$ is validated by $com$. So $com$ must be of the form $com \equiv @inv active(p)$. Since the invariants hold by assumption, $inv(\tau,act)$, we can invoke Lemma B.62. It gives $p \in valid_{\tau,act}$. Altogether, this concludes Property (G3). If $L \in \Gamma_2(p)$, then $L \in \Gamma_1(p)$ due to the type rule.
Hence, the induction hypothesis together with \( m_\tau = m_{r,act} \) and \( valid_\tau = valid_{r,act} \) gives Property (G4). For Property (G5) note that \( \Gamma_0(r) = \Gamma_1(r) \) and that \( repr_\tau(r) = repr_{r,act}(r) \) because \( inv(\tau.act) \) by assumption. So Property (G5) follows by induction. Note that we have \( H(\tau.act) = H(\tau) \). Since \( r \) is not affected, Property (G2) follows by induction. We show Property (G1). If \( com \) does not contain \( p \), nothing needs to be show. Otherwise, \( com \) is of the form \( com \equiv @inv active(p) \). From Lemma B.62 we get \( reach_{Q,t,cp}(H(\tau.act)) \subseteq Loc(A) \). From induction, we get \( reach_{Q,t,cp}(H(\tau.act)) \subseteq Loc(\Gamma_1(p)) \). By definition, this establishes the desired \( reach_{Q,t,cp}(H(\tau.act)) \subseteq Loc(\Gamma_1(p) \land \Lambda) = Loc(\Gamma_2(p)) \) and thus concludes Property (G1).

**Case Rule (ACTIVE) for angels.**

Using Lemma B.63, this case is analogous to the previous, pointer case.

**Case Rule (MALLOC).**

Recall that \( \tau.act \in O[\mathcal{P}]^O_{Adr} \). So \( act \) allocates a fresh address. Hence, \( freed(\tau) = freed(\tau.act) \) by definition. Moreover, \( inv(\tau) \equiv inv(\tau.act) \). Then, Property (G3) holds by induction. Property (G2) remains to hold by induction since \( r \) is not affected. Consider Property (G1). If \( p \) does not appear in \( com \), nothing needs to be shown. Otherwise, \( com \equiv p := malloc. \) From Lemma B.38 we get \( c_p \notin retired(\tau) \). By definition then, \( c_p \notin retired(\tau.act) \). Then, Lemma B.42 gives \( reach_{t,cp}(H(\tau.act)) \subseteq Loc(\Lambda) \). And by definition we have \( \Gamma_2(p) = \{ \Lambda \} \). This concludes Property (G1).

For the remaining properties, we do a case distinction on \( q \). First, consider the case \( p \neq q \). The, \( \Gamma_2(p) = \Gamma_1(p) \) and \( p \in valid_{r,act} \iff p \in valid_\tau \). So Property (G3) follows by induction. Also by induction, we have \( noalias_\tau(p) \). Due to \( up \), we have \( m_{r,act}(p) = m_r(p) \neq seg \). Towards a contradiction, assume \( \neq noalias_{r,act}(p) \). By definition, there is some pointer expression \( pexp \in valid_{r,act} \setminus \{ p \} \) with \( m_{r,act}(p) = m_{r,act}(pexp) \). Since \( m_{r,act}(q) \in fresh(\tau) \) we have \( m_{r,act}(q) \notin range(m_r) \) due to Lemma B.37. Hence, \( pexp \neq q \). Moreover, \( pexp \neq m_{r,act}(q).next \) because \( m_{r,act}(m_{r,act}(q).next) = seg \). Consequently, \( pexp \) is not affected by \( act \). This means we have \( m_{r,act}(pexp) = m_r(pexp) \) and \( pexp \in valid_\tau \setminus \{ p \} \). That is, \( \neq noalias_\tau(p) \). Since this contradicts induction, we conclude the desired \( noalias_{r,act}(p) \). This establishes Property (G4). Second, consider the case \( p = q \). Then, \( \Gamma_2(p) = \{ \Lambda \} \). By Lemmas B.33 and B.37 we have \( a \notin m_r(\text{valid}_\tau) \). Hence, we get \( a \notin m_{r,act}(\text{valid}_{r,act} \setminus \{ p \}) \). This means \( noalias_{r,act}(p) \) holds by definition. This establishes Property (G4). And by definition \( p \in valid_{r,act} \). So Property (G3) holds as well.

**Case Rule (ENTER).**

Note that we have \( m_\tau = m_{r,act} \) and \( repr_\tau = repr_{r,act} \) by definition. By induction, we have \( reach_{Q,t,cp}(H(\tau)) \subseteq Loc(\Gamma_1(p)) \). Type inference gives \( post_{p,com}(Loc(\Gamma_1(p))) \subseteq Loc(\Gamma_2(p)) \). Since \( H(\tau.act) \in S(O) \) due to the semantics, we get \( H(\tau.act) \in post_{p,com}(Loc(\Gamma_1(p))) \). Hence, \( post_{p,com}(Loc(\Gamma_2(p))) \subseteq Loc(\Gamma_2(p)) \) as desired. This concludes Property (G1). Property (G2) follows along the same lines. If \( isValid(\Gamma_2(p)) \), then \( isValid(\Gamma_1(p)) \) by the definition of type inference. Moreover, \( valid_\tau = valid_{r,act} \). Hence, Property (G3) follows by induction. Similarly, \( isValid(\Gamma_1(r)) \) implies \( isValid(\Gamma_1(r)) \). So Property (G5) follows by induction together with \( freed(\tau) = freed(\tau.act) \) and \( inv(\tau) \equiv inv(\tau.act) \). If \( L \in \Gamma_2(p) \), then \( L \in \Gamma_1(p) \) by definition. Note that \( m_\tau = m_{r,act} \). Hence, \( noalias_{r,act}(p) \) follows by induction. This establishes Property (G4).

**Case Rule (EXIT).**
Analogously to the previous case for (ENTER).

**Case Rule (ANGEL).**

By definition, \( m_\tau = m_{\tau, \text{act}} \), \( \text{valid}_\tau = \text{valid}_{\tau, \text{act}} \), and \( \text{freed}(\tau) = \text{freed}(\tau, \text{act}) \). Moreover, the type rule gives \( \Gamma_1(p) = \Gamma_1(p) \). So Properties (G3) and (G4) follow by induction. If \( \text{isValid}(\Gamma_2(r)) \), then \( r \) does not appear in \( \text{com} \). So by the type rule we have \( \Gamma_2(r) = \Gamma_1(r) \). Hence, Property (G5) follows by induction. Since \( p \) is not affected, we get Property (G1) from induction. It remains to consider Property (G2). If \( r \) does not appear in \( \text{com} \), nothing needs to be show because \( \text{repr}_{\tau, \text{act}}(r) = \text{repr}_\tau(r) \). Otherwise, we have \( \Gamma_2(r) = \emptyset \). This concludes Property (G2).

**Case Rule (MEMBER).**

By definition, \( m_\tau = m_{\tau, \text{act}} \), \( \text{valid}_\tau = \text{valid}_{\tau, \text{act}} \), and \( \text{freed}(\tau) = \text{freed}(\tau, \text{act}) \). If \( \text{isValid}(\Gamma_2(r)) \), \( \text{valid}_\tau = \text{valid}_{\tau, \text{act}} \), and \( \text{freed}(\tau) = \text{freed}(\tau, \text{act}) \). Moreover, the type rule gives \( \Gamma_1(r) \) holds since \( \Gamma_2(r) = \Gamma_1(r) \). So Property (G5) follows by induction. If \( \text{isValid}(\Gamma_2(r)) \), then \( L \in \Gamma_1(p) \) since angels cannot acquire guarantee \( L \) due to the type rules. Hence, Property (G4) follows by induction. If \( \text{isValid}(\Gamma_2(p)) \), then there are two cases. First, \( \text{isValid}(\Gamma_1(p)) \) holds. Then, \( p \in \text{valid}_\tau \), by induction and thus \( p \in \text{valid}_{\tau, \text{act}} \). Second, \( \neg \text{isValid}(\Gamma_1(p)) \) holds. Then, \( p \) is validated by \( \text{com} \). For this to happen, we must have \( \text{com} \equiv \top \text{inv} \ p \in r' \) with \( \text{isValid}(\Gamma_1(r')) \). Since \( \text{inv}(\tau, \text{act}) \) hold, we get \( m_\tau(p) \notin \text{repr}_{\tau, \text{act}}(r') \). Moreover, \( \text{isValid}(\Gamma_1(r')) \) gives \( \text{isValid}(\Gamma_2(r')) \). So the already established Property (G5) yields \( m_\tau(p) \notin \text{freed}(\tau, \text{act}) \). Hence, \( m_{\tau, \text{act}}(p) \notin \text{freed}(\tau, \text{act}) \). Now, \( p \in \text{valid}_{\tau, \text{act}} \) by the contrapositive of Lemma B.40. This establishes Property (G3). Consider now Property (G2). If \( r' \) does not appear in \( \text{com} \), nothing needs to be shown. Otherwise, \( \text{com} \equiv \top \text{inv} \ q \in r' \) due to assumption of \( \text{inv}(\tau, \text{act}) \), we have \( m_{\tau, \text{act}}(q) \in \text{repr}_{\tau, \text{act}}(r) \). By definition, \( m_{\tau, \text{act}}(q) = m_\tau(q) \). Again by definition, we get \( m_\tau(q) \in \text{repr}_\tau(r) \) because \( \text{repr}_\tau(r) \) is defined to be the maximal set. This means \( \text{repr}_\tau(r) = \text{repr}_{\tau, \text{act}}(r) \). Hence, we can conclude Property (G2) by induction. It remains to show Property (G1). If \( p \) does not occur in \( \text{com} \), nothing needs to be shown. Otherwise, \( \text{com} \equiv \top \text{inv} \ p \in r' \). Similarly to the above, we get \( c_p \in \text{repr}_\tau(r') \). So we get by induction:

\[
\text{reach}_{\Omega, t, c_p}(\mathcal{H}(\tau)) \subseteq \text{Loc}(\Gamma_1(p)) \cap \text{Loc}(\Gamma_1(r')) = \text{Loc}(\Gamma_1(p) \land \Gamma_1(r')) = \text{Loc}(\Gamma_2(p)).
\]

This concludes Property (G1) by induction together with \( \mathcal{H}(\tau, \text{act}) = \mathcal{H}(\tau) \).

The above case distinction is complete and shows that the claim holds for \( t \) and \( \Gamma_2 \). Hence, the claim holds for \( \Gamma_3 \) as reasoned above.

Now, we show that \( \text{freed}(\tau, \text{act}) \cap \text{retired}(\tau, \text{act}) = \emptyset \) holds. We have \( \text{freed}(\tau, \text{act}) \subseteq \text{freed}(\tau) \) by the fact that \( \text{act} \) cannot be a free due to the fact that \( t' \neq \bot \). If \( \text{retired}(\tau, \text{act}) \subseteq \text{retired}(\tau) \) holds, then the claim follows by induction. Otherwise, we have \( \text{retired}(\tau, \text{act}) = \text{retired}(\tau) \cup \{a\} \) with \( \text{com} \equiv \text{enter retire}(p) \) and \( m_\tau(p) = a \). Since \( t \in \{\Gamma_1\} \) \( \text{com} \in \{\Gamma_2\} \) holds, we know \( p \in \text{valid}_\tau \). By the contrapositive of Lemma B.33, \( a \notin \text{freed}(\tau) \). So by induction, \( \text{freed}(\tau, \text{act}) \cap \text{retired}(\tau, \text{act}) = \emptyset \).

**Ad \( t \neq t' \neq \bot \).** We have

\[
\vdash \{\Gamma_1^{[r]}\} \text{flat}_t(\tau) \{\Gamma_1\} \quad \text{and} \quad \text{flat}_t(\tau, \text{act}) = \text{flat}_t(\tau) \quad \text{and} \quad \vdash \{\Gamma_1^{[r]}\} \text{flat}_t(\tau, \text{act}) \{\Gamma_4\}.
\]

The induction hypothesis applies to \( \vdash \{\Gamma_1^{[r]}\} \text{flat}_t(\tau) \{\Gamma_4\} \). We have to show that the desired properties are stable under interference.

Consider some \( p \in \text{dom}(\Gamma_4) \cap \text{PVar} \). If \( \text{com} \in \Gamma_4(p) \), then \( p \in \text{local}_t \) by the contrapositive of Lemma B.59. By induction, we have \( \text{noalias}_t(p) \). Then, Lemma B.60 gives \( \text{noalias}_{\tau, \text{act}}(p) \). If \( \text{isValid}(\Gamma_4(p)) \), then \( p \in \text{valid}_\tau \) by induction. We invoke Lemma B.60 and get \( p \in \text{valid}_{\tau, \text{act}} \).
Consider some $r \in \text{dom}(\Gamma_i) \cap \text{AVar}$. If $\text{isValid}(\Gamma_i(r))$, then $r \in \text{local}_i$ by the contrapositive of Lemma B.59. By induction we get $\text{repr}_r(r) \cap \text{freed}(\tau) = \emptyset$. Due to $r$ being local to a thread other than the one executing $\text{act}$, $r$ cannot occur in $\text{com}$. Consequently, $\text{repr}_{\tau,\text{act}}(r) = \text{repr}_r(r)$. So $\text{freed}(\tau,\text{act}) \subseteq \text{freed}(\tau)$ due to $t' \neq \perp$ gives $\text{repr}_{\tau,\text{act}}(r) \cap \text{freed}(\tau,\text{act}) = \emptyset$ as desired. It remains to establish $\mathcal{H}(\tau,\text{act}) \subseteq \text{Loc}(\Gamma_i)$. If $\mathcal{H}(\tau,\text{act}) = \mathcal{H}(\tau)$, then the claim follows by induction. So let $\mathcal{H}(\tau,\text{act}) = h.\text{evt}$ with $\mathcal{H}(\tau) = h$. We have $\text{evt} \downarrow_t = \epsilon$. By definition of closedness under interference, we have for all $a$ and $i$:

$$
\begin{align*}
\text{reach}_{O_t,a}(h) &\subseteq \text{Loc}(\emptyset) \implies \text{reach}_{O_t,a}(h.\text{evt}) \subseteq \text{Loc}(\emptyset) \\
\text{and} \quad \text{reach}_{O_t,a}(h) &\subseteq \text{Loc}(\overline{E}_i) \implies \text{reach}_{O_t,a}(h.\text{evt}) \subseteq \text{Loc}(\overline{E}_i)
\end{align*}
$$

Consider some $x \in \text{dom}(\Gamma_i)$. By Lemma B.59 we know $\mathbb{A} \notin \Gamma_i(p)$. If $\mathbb{L} \in \Gamma_i(x)$, then we have $x \in \text{PVar}$ since the type rules do not allow angels to carry $\mathbb{L}$. Moreover, induction gives $\text{reach}_{O_t,m_r(x)}(h) \subseteq \text{Loc}(\mathbb{L})$. To the contrary, assume $\text{reach}_{O_t,m_r(x)}(h.\text{evt}) \not\subseteq \text{Loc}(\mathbb{L})$. By definition, this means that $\text{evt}$ makes $\text{O}_\text{Base} leave its initial location. Since $h.\text{evt} \in S(O)$ due to the semantics, we must have $\text{evt} = \text{enter retire}(t', m_r(x))$. That is, $\text{com} \equiv \text{enter retire}(q)$ with $m_r(q) = m_r(x)$. Since $\tau,\text{act}$ is assumed to be PRF, we must have $q \in \text{valid}_r$. This results in $\neg \text{noalias}_r(x)$ and resembles a contradiction. So we conclude $\text{reach}_{O_t,m_r(x)}(h.\text{evt}) \not\subseteq \text{Loc}(\mathbb{L})$. By the contrapositive of Lemma B.59 we also know that $x \in \text{local}_i$. So $m_r(x) = m_r,\text{act}(x)$. That is, $\text{reach}_{O_t,m_r,\text{act}(x)}(h.\text{evt}) \not\subseteq \text{Loc}(\mathbb{L})$. Moreover, if $x \in \text{PVar}$, then $x \in \text{local}_i$ by Assumption 2. This means $\text{repr}_r(x) = \text{repr}_{\tau,\text{act}}(x)$ since $x$ does not appear in $\text{com}$. So we get $\text{reach}_{O_t,a}(h.\text{evt}) \subseteq \text{Loc}(\Gamma_i)$ for all $a \in \text{repr}_{\tau,\text{act}}(x)$ by induction.

The remaining $\text{freed}(\tau,\text{act}) \cap \text{retired}(\tau,\text{act}) = \emptyset$ follows as in the previous case for $t = t' \neq \perp$. This concludes the case.

Ad $t' = \perp$. We have $\text{act} = (\perp, \text{free}(a), \emptyset)$. Consider some thread $t$ and type environment $\Gamma$ with $\vdash \{ \text{Init}_i \} \text{flat}_i(\tau) \{ \Gamma \}$. By definition, $\text{flat}_i(\tau,\text{act}) = \text{flat}_i(\tau)$. So $\vdash \{ \text{Init}_i \} \text{flat}_i(\tau,\text{act}) \{ \Gamma \}$. We show that $\Gamma$ satisfies the claim. Let $\mathcal{H}(\tau) = h$. Then, $\mathcal{H}(\tau,\text{act}) = h.\text{free}(a)$. By the semantics, we have $h.\text{free}(a) \in S(O)$.

Consider some $p \in \text{dom}(\Gamma) \cap \text{PVar}$. If $\mathbb{L} \in \Gamma(p)$, then $\text{noalias}_r(x)$. Since $m_r = m_r,\text{act}$ and $\text{valid}_{\tau,\text{act}} \subseteq \text{valid}_r$, we get $\text{noalias}_{\tau,\text{act}}(p)$. If $\text{isValid}(\Gamma(p))$, then $\{ A, \mathbb{L}, S \} \not\subseteq \text{valid}_r$. By induction, we have $p \in \text{valid}_r$. Note that we have $\text{reach}_{O_t,m_r(p)}(h) \subseteq \text{Loc}(\Gamma(p))$ by induction. Hence, $a \neq m_r(p)$ must hold as for otherwise $h.\text{free}(a) \not\in S(O)$ by the definition of $\{ A, \mathbb{L}, S \}$. So, we get $p \in \text{valid}_{\tau,\text{act}}$ by definition.

Consider some $r \in \text{dom}(\Gamma) \cap \text{AVar}$. If $\text{isValid}(\Gamma(r))$, then $\text{repr}_r(r) \cap \text{freed}(\tau) = \emptyset$ by induction. By definition, we have $\text{repr}_r(r) = \text{repr}_{\tau,\text{act}}(r)$. Moreover, $\text{freed}(\tau,\text{act}) = \text{freed}(\tau) \cup \{ a \}$. So in order to arrive at $\text{repr}_{\tau,\text{act}}(r) \cap \text{freed}(\tau,\text{act}) = \emptyset$, it suffices to establish $a \notin \text{repr}_r(r)$. To the contrary, assume $a \in \text{repr}_r(r)$. Then, $\text{reach}_{O_t,a}(h) \subseteq \text{Loc}(\Gamma(r))$ by induction. However, similar to the pointer case above, this means $h.\text{free}(a) \not\in S(O)$ because of $\text{isValid}(\Gamma(r))$. Hence, $a \notin \text{repr}_r(r)$ must hold as desired.

It remains to show that $\text{reach}_{O_t,b}(h.\text{free}(a)) \subseteq \text{Loc}(\Gamma(x))$ for every $x \in \text{dom}(\Gamma_i)$ with $a \neq m_r(x)$ for $x \in \text{PVar}$ and $a \notin \text{repr}_r(x)$ for $x \in \text{AVar}$. By definition we have:

$$
\begin{align*}
\text{reach}_{O_t,b}(h) &\subseteq \text{Loc}(\emptyset) \implies \text{reach}_{O_t,b}(h.\text{free}(a)) \subseteq \text{Loc}(\emptyset) \\
\text{reach}_{O_t,b}(h) &\subseteq \text{Loc}(\overline{E}_i) \implies \text{reach}_{O_t,b}(h.\text{free}(a)) \subseteq \text{Loc}(\overline{E}_i) \\
\text{reach}_{O_t,b}(h) &\subseteq \text{Loc}(\emptyset) \implies \text{reach}_{O_t,b}(h.\text{free}(a)) \subseteq \text{Loc}(\emptyset) \\
\text{reach}_{O_t,b}(h) &\subseteq \text{Loc}(\overline{E}_i) \implies \text{reach}_{O_t,b}(h.\text{free}(a)) \subseteq \text{Loc}(\overline{E}_i) \\
\text{reach}_{O_t,b}(h) &\subseteq \text{Loc}(\emptyset) \implies \text{reach}_{O_t,b}(h.\text{free}(a)) \subseteq \text{Loc}(\emptyset) \\
\text{reach}_{O_t,b}(h) &\subseteq \text{Loc}(\overline{E}_i) \implies \text{reach}_{O_t,b}(h.\text{free}(a)) \subseteq \text{Loc}(\overline{E}_i) \\
\text{reach}_{O_t,b}(h) &\subseteq \text{Loc}(\emptyset) \implies \text{reach}_{O_t,b}(h.\text{free}(a)) \subseteq \text{Loc}(\emptyset) \\
\text{reach}_{O_t,b}(h) &\subseteq \text{Loc}(\overline{E}_i) \implies \text{reach}_{O_t,b}(h.\text{free}(a)) \subseteq \text{Loc}(\overline{E}_i)
\end{align*}
$$
Recall from above that \( \{A, \mathbb{L}\} \cap \Gamma(x) \neq \emptyset \) implies \( a \neq m_r(x) \) for \( x \in AVar \). Hence, we conclude the desired \( \text{reach}_{O,T,b}(h.\text{free}(a)) \subseteq \text{Loc}(\Gamma(x)) \) by induction together with \( m_r = m_r.\text{act} \) and \( \text{repr}_r = \text{repr}_r.\text{act} \).

Lastly, we show \( \text{freed}(\tau.\text{act}) \cap \text{retired}(\tau.\text{act}) = \emptyset \). We have \( \text{freed}(\tau.\text{act}) = \text{freed}(\tau) \cup \{a\} \) and \( \text{retired}(\tau.\text{act}) = \text{retired}(\tau) \setminus \{a\} \). Then the claim follows by induction.

\[ \square \]

**Proof of Lemma B.66.** Let \( \vdash \{\Gamma_{\text{init}}\} P \{\Gamma_P\} \) and \( \text{inv}(\{ P \}^\subset) \). Towards a contradiction, assume the claim does not hold. That is, there is a shortest computation \( \tau.\text{act} \in \text{O}[\{ P \}^\subset] \), such that \( \tau.\text{act} \) raises a pointer race or \( \neg \text{inv}(\tau.\text{act}) \). By minimality, \( \tau \) is PRF and \( \text{inv}(\tau) \). Let \( \text{act} = (t, \text{com}, \text{up}) \). (Note that \( \text{com} \) is neither beginatomic nor endatomic due to the assumption.) By Lemma B.58, there is \( \Gamma_3 \) such that \( \vdash \{ \Gamma_{\text{init}}^{[1]} \} \text{flat}_r(\tau.\text{act}) \{ \Gamma_3 \} \). We have \( \text{flat}_r(\tau.\text{act}) = \text{flat}_r(\tau); \text{com} \) by definition. So by the type rules there is \( \Gamma_0, \Gamma_1, \Gamma_2 \)

\[ \vdash \{ \Gamma_{\text{init}}^{[1]} \} \text{flat}_r(\tau) \{ \Gamma_0 \} \quad \Gamma_0 \sim \Gamma_1 \quad \vdash \{ \Gamma_1 \} \text{com} \{ \Gamma_2 \} \quad \Gamma_2 \sim \Gamma_3 \]

First, consider the case where \( \tau.\text{act} \) raises a pointer race. By definition of pointer races, \( \text{act} \) is on of: an unsafe access, an unsafe assumption, an unsafe enter, or an unsafe retire.

- **If \( \text{act} \) is an unsafe access, then \( \text{com} \) contains \( p.\text{next} \) or \( p.\text{data} \) with \( p \notin \text{valid}_r \).** That is, \( \vdash \{ \Gamma_1 \} \text{com} \{ \Gamma_2 \} \) is derived using on of the following rules: (ASSIGN2), (ASSIGN3), (ASSIGN5), or (ASSIGN6). Since the derivation is defined, we must have \( \Gamma_1(p) = T \) with \( \text{isValid}(T) \). By Lemma B.65, this means \( p \in \text{valid}_r \). Since this contradicts the assumption of \( \text{act} \) raising a pointer race, this case cannot apply.

- **If \( \text{act} \) is an unsafe assumption, then \( \text{com} \equiv \text{assume} = q \) with \( \{p, q\} \notin \text{valid}_r \).** That is, \( \vdash \{ \Gamma_1 \} \text{com} \{ \Gamma_2 \} \) is derived using rule (ASSUME1). By definition, we have \( \Gamma_1(p) = T, \Gamma_1(q) = T' \) with \( \text{isValid}(T) \) and \( \text{isValid}(T') \). From Lemma B.65 we get \( \{p, q\} \subseteq \text{valid}_r \). Since this contradicts the assumption of \( \text{act} \) raising a pointer race, this case cannot apply.

- **Consider an unsafe enter, i.e., \( \text{com} \equiv \text{enter} = \text{func}(\bar{p}, \bar{\bar{u}}) \).** That is, \( \vdash \{ \Gamma_1 \} \text{com} \{ \Gamma_2 \} \) is derived using rule (ENTER). Let \( m_r(\bar{p}) = \bar{a} \) and \( m_r(\bar{\bar{u}}) = \bar{d} \). That \( \text{act} \) is an unsafe enter means that there are \( \bar{b} \) and \( c \) with:

\[ \forall i. (a_i = c \lor p_i \in \text{valid}_r) \implies a_i = b_i \]

and

\[ F_O(h.\text{func}(t, \bar{b}, \bar{d}), c) \notin F_O(h.\text{func}(t, \bar{a}, \bar{d}), c) . \]

Let \( \bar{p} = p_1, \ldots, p_n \) with \( \Gamma(p_1) = T_i \). From Lemma B.65 we get \( p_i \notin \text{valid}_r \implies \neg \text{isValid}(T_i) \). Hence, the following holds:

\[ \forall i. (a_i = c \lor p_i \in \text{valid}_r) \implies a_i = b_i \]

implies \( \forall i. a_i = b_i \implies (a_i \neq c \land p_i \notin \text{valid}_r) \)

implies \( \forall i. a_i \neq b_i \implies (a_i \neq c \land \neg \text{isValid}(T_i)) \)

implies \( \forall i. (a_i = c \lor \text{isValid}(T_i)) \implies a_i = b_i \)

So \text{safeEnter}(\Gamma_1, \text{func}(\bar{p}, \bar{\bar{u}})) = \text{false} \). As this contradicts \( \vdash \{ \Gamma_1 \} \text{com} \{ \Gamma_2 \} \), this case cannot apply.

- **Consider an unsafe retire, i.e., \( \text{com} \equiv \text{enter} = \text{retire}(p) \) with \( p \notin \text{valid}_r \).** As in the previous case, \( \vdash \{ \Gamma_1 \} \text{com} \{ \Gamma_2 \} \) is derived using rule (ENTER). It gives \( A \in \Gamma_1(p) \). That is, \( \text{isValid}(\Gamma_1(p)) = \text{true} \). Then, Lemma B.65 yields \( p \in \text{valid}_r \). Hence, this case cannot apply.

The above case distinction is complete. That is, \( \tau.\text{act} \) cannot raise a pointer race. Hence, we must have \( \neg \text{inv}(\tau.\text{act}) \). Since we have \( \text{inv}(\tau) \) as stated before, \( \text{act} \) must be an annotation that does not hold. By Lemma B.44 for \( \tau.\text{act} \) there is \( \sigma \in \{ P \}^\subset \) with \( \text{ctrl}(\tau.\text{act}) = \text{ctrl}(\sigma) \), \( m_r.\text{act} = m_\sigma \), and
inv(σ) ⇒ inv(τ. act). The contrapositive of the latter, gives ¬inv(τ. act) ⇒ ¬inv(σ). That is, we must have ¬inv(σ). This contradicts the assumption of inv([P]_A^σ), concluding the claim thus. □

Proof of Lemma B.67. Let O_SMR supports elision. Furthermore, let ⊢ P and inv([P]_A^σ). By Lemma B.66 we know that O_Env is PRF and that inv(O_Env^σ) holds. Now, to the contrary, assume the overall claim does not hold. Then there is τ. act ∈ [P]_A^σ with a ∈ retired(τ), act = (t, com, up), com ≡ enter retire(p), and m_t(p) = a. Then, Lemma B.36 yields σ ∈ O_Env such that τ ≈ σ and retired(τ) ⊆ retired(σ). From the former we get σ. act ∈ O_Env^σ. Moreover, together with O_Env^σ PRF and thus p ∈ validσ, we get m_t(p) = a = m_σ(p). The latter gives a ∈ retired(σ).

From Lemma B.58 we get some Γ₁ with ⊢ {Γ_init}₁ flat₁(σ. act){Γ₃}. Then, flat₁(σ. act) = flat₁(σ); com by definition. So the typing rules give some Γ₀, Γ₁, Γ₂ with

\[ \vdash \{Γ_init\}₁ flat₁(σ) \{Γ₀\} \quad Γ₀ \sim Γ₁ \quad \vdash \{Γ₁\} com \{Γ₂\} \quad Γ₂ \sim Γ₃ \]

where the derivation for \( \vdash \{Γ₁\} com \{Γ₂\} \) is due to Rule (ENTER). By definition, this means we have A ∈ Γ₁(p). Note that σ is PRF and inv(σ). Moreover, \( \vdash \{Γ_init\}₁ flat₁(σ) \{Γ₁\} \) holds due to Rule (INFER). Now, Lemma B.65 yields reachO,(I,a)(H(σ)) ⊆ Loc(Γ₁(p)). In particular, this means reachO,(I,a)(H(σ)) ⊆ Loc(A). Hence, (L₂, φ) ᵃ→(L₂, φ) with φ = \{z_a ← a\} and h = H(σ). Then, Lemma B.42 gives a /∈ retired(σ). This contradicts the previous a ∈ retired(σ). □

Proof of Theorem 5.1. Follows from Lemmas B.66 and B.67. □

D. TYPE CHECKING

Lemma D.1. AntiChainTypes := (Types/≈, ⊑, ¬, ∪, −→) is a complete lattice.

Proof. The least element is the most precise type containing every guarantee. The join of two guarantees B_L ∪ B_L’ is characterized by the union L ∪ L’, which is again closed under interference. The meet of two guarantees B_L ∩ B_L’ requires care. The intersection L ∩ L’ may not be closed under interference, in which case a corresponding guarantee B_L∩L’ does not exist. Instead, we take the largest set of locations that is closed under interference and lives inside the intersection. It is guaranteed to exist. □

Lemma D.2. sp(·, com) is monotonic.

Proof. The case that requires care is Rule (ENTER). A larger enriched environment has less guarantees, and eventually safeEnter(Γ, func(φ, u)) may fail. In this case, however, we return τ. □

Proof of Proposition 7.2. For Isol(X) ⊆ ∩ \( \{Γ_init\} stmt \{Γ\} \), observe that the least solution to the constraint system yields a type derivation \( \vdash \{Γ_init\} stmt \{isol(X)\} \). Indeed, as the solution assigns a type environment to every control point, it already gives the intermediary environments we should assume for a Rule (SEQ). For the reverse direction, consider \( \vdash \{Γ_init\} stmt \{Γ\} \). One can show that by assigning the environments encountered in the type derivation to the variables of the corresponding control points, we obtain a solution to the constraint system. Since Isol(X) is the least solution, Isol(X) ⊆ Γ. As the reasoning holds for every derivation, Isol(X) will lower bound the meet of the environments. □

Lemma D.3. The Kleene iteration takes time O(n²) where n is the size of the input program.

Proof. We denote the set of program variables by Vars and the set of variables from the constraint system by CVars = \{X₁, ..., X_k\}. The Kleene iteration solving the constraint system works over the product lattice

\[ \left( \text{AntiChainTypes}^{Vars} \cup \{\top\} \right)^{CVars} \]

Proc. ACM Program. Lang., Vol. 4, No. POPL, Article 68. Publication date: January 2020.
where ⊑ is the component-wise ⊑ from the original lattice $EnVs_T$. Following the discussion in Section 7, chains in this lattice have a maximal length of $m$ which is quadratic in $n$. To compute the Kleene iteration, we employ a worklist algorithm.

We introduce notations to ease the formal development. We use $V_i = (V_i^1, \ldots, V_i^k)$ where $V_i^j$ denotes the value of variable $X_j$ in step $i$. Moreover, we maintain a worklist $W_i$ the entries of which are variable indices that need to be recomputed after step $i$. That is, $j \in W_i$ states that the value $V_j$ of $X_j$ is no longer up to date since the variables that $X_j$ depends on have received new values previously. We write $W.W'$ and mean worklist $W$ concatenated with worklist $W'$. We define a total function $Dep : \{1, \ldots, k\} \to 2^{\{1, \ldots, k\}}$ that computes dependencies among the variables from $CVars$. That is, $Dep(j)$ yields the indices of variables that depend on $X_j$. We use $Dep(j)$ during the Kleene iteration to query those variables that we need to compute a new value for after updating the value of $X_j$. For example, the constraint $sp(X_1, com) \subseteq X_2$ implies $2 \in Dep(1)$. Similarly, we define $Req : \{1, \ldots, k\} \to 2^{\{1, \ldots, k\}}$ that computes requirements. That is, $Req(j)$ computes the indices of variables that are required to compute $X_j$. For example, the constraint $sp(X_1, com) \subseteq X_2$ implies $1 \in Req(2)$. Both $Dep$ and $Req$ can be tabulated (in quadratic time) prior to the Kleene iteration.

In the beginning $V_0^j = \bot$ and $W_0$ is empty. In the first step, a new value $V_1^j \in EnVs_T$ for all $X_i \in CVars$ is computed. This is linear in $n$. Next, we perform steps until the worklist is empty again or we have performed $m$ steps—in both cases we are guaranteed to have found a fixed point. To perform a step $i \to i + 1$, let $W_i$ be of the form $W_i = j.W_i^{tail}$. Then, we (i) compute a new value $V_{i+1}^j$ for $X_j$, and (ii) set $W_{i+1} = W_i^{tail}.Dep(j)$. Removing the first element from a list, looking up $Dep(j)$, and appending two list can be done in constant time. Hence, (ii) can be done in constant time. It remains to consider (i). The updated value is:

$$V_{i+1}^j = \bigcup_{l \in Req(j)} g_{j,l}(V_i^l)$$

where $g_{j,l}(V) = V$ or $g_{j,l}(V) = sp(V, com)$ for some $com$, depending on the constraints collected from the input program. Recall from Section 7 that $g_{j,l}$ can be computed in constant time. For $Req(j)$ to yield a set of constant size, we rely on a simple preprocessing of the input program: every primitive command is wrapped inside skip commands, that is, command $com$ is preprocessed to (skip; $com$); skip. This way we introduce fresh variables into the constraint system such that no two branches of the program share constraint system variables and that each nested statement does not share constraint system variables with its parents. The program resulting from the preprocessing is linear in the size of the original program, hence our reasoning so far remains valid for the preprocessed program and carries over to the original one. Altogether, we arrive at (ii) taking constant time. This concludes the claim. \(\square\)