A TEM nanoanalytical investigation of Pd/Ge ohmic contacts for the miniaturization and optimization of n-InGaAs MOSFET devices

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Abstract. In this paper, a nanoanalytical investigation of electron beam evaporated PdGe ohmic contacts onto an n\(^+\) In\(_{0.53}\)Ga\(_{0.47}\)As layer using electron energy loss spectroscopy (EELS) is presented. The chemical information reported in this paper has been obtained using EELS spectrum images (SI) that allow not only depth resolution but also spatial resolution which is essential in such inhomogeneous systems.

1. Introduction
As the size of III-V devices decreases, ohmic contacts and their performance become increasingly important. In addition to low resistance, these contacts need to show thermal stability, reproducibility, as well as lateral and depth uniformity. AuGeNi ohmic contacts have been widely used as they show relatively low specific contact resistivity. Using this approach world leading GaAs MOSFET devices have been realised [1]. However as reported in [2], such contacts have the drawback of poor uniformity due to the Au diffusion into the III-V substrate. Obviously this strongly limits them for scaling purposes. In addition, with the quest for co-integration of III-V and silicon MOSFETs for ultimate CMOS applications, silicon compatible III-V devices process modules, which are gold-free, are required. PdGe ohmic contacts have demonstrated a contact resistance as low as 10\(^{-6}\) Ωcm\(^2\) which is comparable to that shown by AuGeNi approaches. They also show better uniformity along the interface with the III-V substrate [3,4]. PdGe contacts are formed via a solid state reaction between a layer of Pd on the III-V substrate followed by a thicker one of Ge. During the annealing process, the Ge reacts with all the Pd forming PdGe. However some of it will be also incorporated into the InGaAs, preferentially on Ga sites as there is an excess of Ga vacancies [5]. This will determine the formation of a n-type layer beneath the ohmic contact and this is an important issue when n-type devices are being fabricated. The choice of the thickness of Pd and Ge layers is such that it ensures the Ge penetrates across the entire Pd layer forming PdGe and reacting with the surface of the III-V substrate. The behaviour of this type contact will be affected by the nature of the species present at the interface and the degree of roughness along the interface [6]. The contacts of this study are capped with Ti/Pt that acts as barrier to upwards Ge diffusion during the annealing process [7].
The morphology and the chemistry of such ohmic contacts are investigated using scanning transmission electron microscopy ((S)TEM) and, in particular, EELS for the analytical study.

2. Experimental methods

The 70nm Pd, 100nm Ge, 30nm Ti and 40nm Pt ohmic contact stack was deposited by electron beam evaporation onto a 500nm thick In₀.₅₃Ga₀.₄₇As layer silicon doped to 1x10¹⁹ atoms cm⁻³, grown on a semi-insulating InP substrate. The sample was then cleaved and one half went through a rapid thermal annealing for 10 seconds at 400 °C. TEM specimens of both the annealed and unannealed samples were prepared by standard cross-sectioning that involves cutting, grinding, dimpling and ion milling using a Gatan PIPS at 4kV for the initial stages of the process and 0.5kV for the final ones. The final polishing was carried out using a Technorg Linda Gentle Mill at 0.2kV. Conventional TEM images were taken using an FEI Tecnai F20. The chemical analysis was carried out in a scanning transmission electron microscope (STEM) using a probe size of 0.7nm and probe half convergence angle of 9mrad. EELS data were recorded using a Gatan Enfina spectrometer with a half collection angle of 40mrad and an energy loss range from 260eV to 1600eV. This ensures PdM₄,₅-edges at 335eV, In M₄,₅-edges at 443eV, Ga L₂,₃-edges at 1115eV, Ge L₂,₃-edges at 1217eV and As L₂,₃-edges at 1323eV are collected in the same spectrum. Where possible, the edges where extracted after removal of the background using a power law model fitting in front of the edge. However edges such as Ga L₂,₃ at 1115eV and the Ge L₂,₃ at 1217eV overlap. This made the edge extraction by simple removal of the background impossible. This problem can be overcome by using the multiple linear least square (MLLS) fit method available in the Gatan Digital Micrograph package. The spectrum imaging plug-in of Gatan was employed to collect spectrum images starting in the bulk InGaAs and extending ~25nm into the contact region using a step size of 1.8nm. This provides insight into the chemistry at the interface region. An acquisition time of 8 seconds per pixel was used. A spatial drift correction area was applied in order to minimize the effects of drift that usually occur in a TEM microscope. The drift correction was carried out every 3 pixels. Although this material is electron beam resistant, the analysis was carried out using the sub-pixel scanning which is available in Gatan Digiscan package. This consists of scanning the beam within the pixel area while acquiring the EELS spectrum. Thus the electron dose is spread over the pixel area minimizing the dose and any C contamination. The presence of C whose K-edge is at 284eV affects the background of Pd M₄,₅-edges making its extraction...
unreliable. Therefore, it is essential to limit the C contamination.

3. Results and discussion
Figs. 1a,b show bright field images of the whole ohmic contact region in the unannealed and annealed samples respectively. The unannealed sample does not show, at a large scale, any sign of major reactions between the contact and the substrate across the whole contact region. Ge and Pd layers appear to be amorphous although some lattice fringes can be observed at positions more than 10nm from the substrate when the image is taken at higher magnification. On the other hand, in the annealed sample, most of the Ge has reacted with all the Pd forming a PdGe granular structure as shown in Fig. 1b. At the Ti side, some amorphous Ge remains and there is a (Ti, Ge) reaction layer at the Ti boundary. On the substrate side the PdGe approaches the substrate. The interface is now fairly rough and it is also quite difficult to distinguish where the original interface was before the annealing. A marker layer would be useful. Fig. 2 is a high-resolution TEM bright field image of the contact/substrate interface taken from the annealed sample. It confirms that most of the interface region next to the substrate has crystallized with the same orientation as the InGaAs substrate. For the annealed sample, the EELS spectrum images were taken across the selected region shown in Fig. 3. The signal to noise ratio was improved by summing the spectra in lines parallel to the interface Fig. 4 shows the In, Ga, Ge, As and Pd edge intensities extracted from that region. The background fitting windows were chosen in regions of the EELS spectrum where perturbations are not significant. However, their use to process the whole spectrum results in negative counts for the Pd, In and As in some regions. Ge has either directly penetrated the Pd layer or propagated along grain boundaries and diffused into the InGaAs more strongly than the Pd. Ga, In and As have diffused into the contact region with Ga propagating further. In the InGaAs region, a 2nm layer rich in In and deficient in Ga has been detected. This corresponds to the bright line marked 3 in Fig. 3 and the peak in In and dip in Ga marked 3 in Fig. 4. To further explore the mechanism of formation of the In rich layer, two more wafers were prepared. In the first one, referred to as Ge only, 100nm of Ge followed by 30nm of Ti and 40nm of Pt were deposited onto the same InGaAs substrate. In the second one, referred to as Pd only, 70nm layer of Pd followed by Ti and Pt were deposited. Both wafers were cleaved and one half went through the same annealing process described above. Fig. 5 is a high-resolution TEM micrograph of the interface region between the InGaAs and the Ge layer in the Ge only sample after annealing. The interface appears to be very smooth. It seems that the annealing process has not caused major variations in the morphology of the interface nor most likely, of the chemistry. Figs. 6a,b show the In, Ga, Ge and As edge intensities extracted from the interface region in the Ge only unannealed and annealed samples respectively. In the unannealed sample the In, As and Ga lines drop all together and symmetrically with respect to the Ge line. This suggests little or no
interpenetration with beam spreading or roughness causing the width of the transition. However, in the annealed sample the Ga appears to diffuse further to the right making the Ge layer p-doped and this is not good if n-devices are being fabricated. Here it is not clear if the Ge has really diffused into the InGaAs to replace the Ga. Fig. 7 shows a high-resolution TEM micrograph of the interface between the InGaAs and the Pd layer in the Pd only sample after annealing. The interface appears to be fairly sharp but reasonably rough with the presence of granular structures most likely containing Pd that extends into the InGaAs. Here the EELS line spectrum images were taken across the selected region shown in Fig. 8, using 2.5nm step size. Fig. 9 shows the In, Ga, As and Pd lines extracted from the selected region in Fig. 8. As and Ga have penetrated into the Pd layer more strongly than the In and diffused across the whole Pd layer. The region marked A is the InGaAs substrate. In region B, there is a high concentration of Pd with significant Ga and some In, both decreasing with distance from the InGaAs, while the As increases toward region C. Region C is mainly As with some Ga but no Pd or In and corresponds to the darker layer marked C in Fig 8. Region D is Pd with only Ga and As and extends to the Ti layer. Clearly the interaction of Pd with InGaAs is quite complex. When there is a Ge layer on top of the Pd, there will be a competition between the interaction of the Pd with the Ge and that with the InGaAs. Thus there may be a link between the potential to form the In containing layer B in Figs 8 and 9 with the In rich layer marked 3 in Figs. 3 and 4.

4. Conclusions
The results presented in the paper show that it is possible to analyse with spatial and depth resolution inhomogeneous systems such as PdGe ohmic contacts at a nanometer-level using EELS SI. This allows to understand in details the reactions occurring during the contact stack formation and in particular to address the role of both the Ge and the Pd.

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