A High-Power-Factor Dimmable LED Driver with Integrated Boost Converter and Half-Bridge-Topology Converter

Hung-Liang Cheng, Yong-Nong Chang, Lain-Chyr Hwang, Hau-Chen Yen, Shun-Yu Chan and Wen-Fu Yang

1 Department of Electrical Engineering, I-Shou University, Kaohsiung 84001, Taiwan; hlcheng@isu.edu.tw (H.-L.C.); lain@isu.edu.tw (L.-C.H.)
2 Department of Electrical Engineering, National Formosa University, Hu-Wei, Yunlin 63201, Taiwan; joe26433379@yahoo.com.tw
3 Department Electrical Engineering, Far East University, Tainan 74448, Taiwan; yenc66@mail.feu.edu.tw
4 Department of Electrical Engineering, Cheng Shiu University, Kaohsiung 83347, Taiwan; gitanojan@gmail.com

Abstract: This paper proposes a dimmable light-emitting diode (LED) driver featuring a high power factor and zero-voltage switching on (ZVS). The circuit is obtained by integrating a boost converter and a dc-dc converter with half-bridge topology. The high power factor is achieved by operating the boost converter in discontinuous current mode (DCM). The LEDs are dimmed by the control scheme of asymmetrical pulse-width modulation (ASPWM). The developed circuit eliminates the inherited dc-offset current of the transformer in a conventional asymmetrical half-bridge converter by introducing a balance capacitor. Both active switches can operate at ZVS by freewheeling the boost inductor current and the transformer magnetizing current to discharge the energy stored in their parasitic capacitance. The circuit operation is analyzed in detail, and mathematical equations are derived. Finally, a 115-W prototype circuit for driving high brightness LEDs was built and tested. The experimental results verify the feasibility of the proposed LED driver with satisfactory performance. It can achieve a high power factor and ZVS operation.

Keywords: asymmetrical pulse-width modulation (ASPWM); half-bridge converter; light-emitting diode (LED); power-factor correction; zero-voltage switching on (ZVS)

1. Introduction

The amount of power consumption for lighting applications accounts for around 15–20% of the total generated electric power. Therefore, any small increase in lighting efficiency will result in a significant reduction in energy consumption. For improving the illuminous efficiency of lighting sources, vast manpower and resource are engaged to develop light-emitting diodes (LEDs). Compared with traditional lighting sources, LED has the advantages of a small size, high luminous efficiency, and long life span and are the most promising lighting device [1–5].

Owing to the simple circuit topology and easy control, half-bridge converters are widely used in medium and low-power applications. Nevertheless, the active switches of the half-bridge converter suffer from hard switching, resulting in high voltage/current stresses and high switching losses. In order to solve the problem of hard switching, an active clamp and snubber circuits are usually used to make the active switches operate at zero-voltage switching on (ZVS), leading to low voltage and/or current stresses [6–9]. In addition, the circuit efficiency can be effectively improved. However, these techniques...
require the use of additional auxiliary switches, diodes, and passive components to enable the active switch to operate at ZVS or zero-current switching off (ZCS). These soft-switching techniques would increase the complexity and cost of the circuit. Besides, current loops in active clamp circuits or snubber circuits can cause additional conduction losses and even more switching losses.

Recently, in order to comply with the more stringent regulations such as IEC61000-3-2 class C, an additional alternating current-to-direct current (ac/dc) conversion stage is required to cascade in front of the dc/dc converter to perform the function of the power factor correction (PFC). For the sake of reducing circuit costs, many single-stage circuits have been developed for driving LEDs by integrating a PFC converter into the original LED driver [10–15]. Although these single-stage approaches can achieve a high power factor and low total current harmonic distortion (THDi), one or more active switches in these single-stage circuits still suffer from the hard switching problem. On the other hand, an LED driver with dimming capability is needed in many applications. Some single-stage approaches are derived by integration of a boost and a half-bridge resonant converter [14,15]. The half-bridge converters usually use an inductor-inductor-capacitor (LLC) or a capacitor-inductor-capacitor-inductor (CLCL) resonant tank to achieve ZVS. Frequency modulation control is usually used to achieve the dimming operation. Since the boost converter and the resonant converter share the same active switch, the switching frequency of the boost converter also varies to accomplish the dimming operation. Generally, the input power of the boost converter is inversely proportional to the switching frequency. In order to achieve wide dimming operation, the switching frequency should vary in a wide range. The higher the switching frequency, the lower the LED power. Moreover, higher switching frequency would incur more switching losses, leading to low efficiency at low power operation.

In single-stage circuits, a dc-link capacitor is usually required to absorb or release power due to the mismatch between input power and output power. The voltage across the dc-link capacitor varies when the LEDs are dimmed. When the dimming range is large, the voltage of the dc-link capacitor changes greatly. Generally, the methods of symmetrical pulse-width modulation (PWM) or asymmetrical pulse-width modulation (ASPWM) are often used to control the active switches to regulate LED power [16–19]. When both control schemes are compared, the voltage across the dc-link capacitor of the PWM scheme is higher than that of the ASPWM one [18,19]. Although the ASPWM scheme always incurs noticeable dc-offset current in the transformer, resulting in increasing transformer core loss [20], the dc-offset current can be easily eliminated by connecting a dc-balance capacitor in series with the primary winding.

Aiming to develop a dimmable LED driver with the features of a high power factor and ZVS, this manuscript proposes a single-stage circuit based on integrating a boost-type PFC converter and a half-bridge converter. The developed LED driver integrates the advantages of soft switching and PFC techniques, leading to high efficiency and a high power factor. Besides, it can achieve wide dimming range. The circuit operation is analyzed, and the mathematical equations for designing component parameters are generated. Finally, a 115-W prototype LED driver circuit is designed and implemented to validate the feasibility of the proposed circuit.

2. Proposed Circuit Configuration and Operation Analysis

2.1. Circuit Topology

Figure 1 shows the proposed circuit configuration of the LED driver. The half-bridge converter consists of two active switches \((S_1, S_2)\), a transformer \((T_1)\), a capacitor \((C_{i1})\), a diode rectifier \((D_1–D_4)\), an output inductor \((L_o)\), and an output capacitor \((C_o)\). The diodes \(D_{S1}\) and \(D_{S2}\) are the intrinsic diodes of \(S_1\) and \(S_2\), respectively. \(L_m\) represents the mutual inductance of the transformer \(T_1\). \(C_{i1}\) is used to eliminate the dc-offset current in the transformer. \(S_1\) and \(S_2\) are operated by the control scheme of ASPWM to dim the LEDs.
A boost converter performs the function of power-factor correction which consists of an inductor $L_{PFC}$ and the lower arm switch $S_2$. By operating the boost converter in discontinuous-conduction mode (DCM), the peak value of the inductor current $i_{LPFC}$ will follow the track of the rectified input voltage $v_{in}$. The frequency of $i_{LPFC}$ is far greater than the input-line frequency. The inductor $L_f$ and the capacitor $C_f$ form a low-pass filter which is used to filter out the high frequency component of $i_{LPFC}$. In this way, the input current can be close to a sinusoidal waveform and in phase with the input-line voltage, thus achieving a high power factor. The magnetizing current in $L_m$ can be used to remove the energy accumulated on parasitic capacitors of $S_1$ and $S_2$ to attain ZVS operation. Thus, the switching losses can be drastically reduced, and the operating efficiency can be promoted.

2.2. Operation Analysis

For simplifying the operation analysis, the following assumptions are made.

- Ignoring the conduction voltage drop for all switching devices, such as diodes and active switches.
- The switching frequency is much greater than the input-line frequency.
- Ignoring voltage ripples on all capacitors because the $C_{bus}$ and $C_{b1}$ are large enough.
- The output inductor $L_o$ is large enough, and its current is assumed to be a constant $I_L$.

At steady state, the operation of the proposed circuit can be divided into seven modes according to the conducting status of the semiconductor devices in one high-frequency switching cycle. These operation modes and the theoretical voltage and current waveforms of the key components are shown in Figures 2 and 3, respectively. For simplifying the circuit analysis, the low-pass filter and the diode rectifier at the input side are represented by the rectified voltage $v_{rec}$, and the LED string is represented by its equivalent resistance $R_{LED}$. The detailed description of each operation mode is as follows.

A. Mode I ($t_0 < t < t_1$)

As illustrated in Figure 2a, Mode I begins at the time when the gate signal $v_{GS1}$ turns from a high level to a low level. For maintaining the magnetic flux in $L_m$, the magnetizing current $i_{Lm}$ flows via the capacitor $C_{b1}$ and the parasitic capacitance of $S_2$. The parasitic capacitance of $S_2$ is discharged, and the voltage across $S_2$ decreases. Generally, the parasitic capacitance of the active switch is quite small, and it is completely discharged very rapidly. When the energy on the parasitic capacitance of $S_2$ is totally released, $i_{Lm}$ diverts from the parasitic capacitance to the intrinsic diode $D_{S2}$. Hereafter, the voltage across $S_2$, $v_{DS2}$ is clamped at zero volts. Thus, the ZVS operation can be achieved. The voltage across the primary winding is equal to $-V_{CB1}$, and diodes $D_2$ and $D_3$ are on, and the current in the secondary...
winding \( i_{TB} \) flows through \( D_2 \), \( D_3 \) and \( L_o \). During this interval, \( i_{TB} \) is equal to the output inductor current \( I_{Lo} \). The \( i_{Lm} \) and the primary current \( i_{Tp} \) can be written as Equations (1) and (2), respectively.

\[
i_{Lm}(t) = i_{Lm}(t_0) - \frac{V_{CH}}{L_m}(t - t_0), \tag{1}
\]

\[
i_{Tp}(t) = i_{Lm}(t) - \frac{N_S}{N_P}I_{Lo}, \tag{2}
\]

where \( N_S \) and \( N_P \) represent the turns of the primary winding and the secondary winding, respectively.

\[\text{Figure 2. Operation modes. (a) Mode I, (b) Mode II, (c) Mode III, (d) Mode IV, (e) Mode V, (f) Mode VI, (g) Mode VII.}\]

Since \( S_2 \) is clamped at zero volts, the voltage across the PFC inductor is equal to the rectified input voltage. The PFC current increases linearly and is expressed as:

\[
i_{LPFC}(t) = \frac{v_{rec}(t)}{L_{PFC}}(t - t_0) = \frac{V_m|\sin(2\pi f_1 t)|}{L_{PFC}}(t - t_0), \tag{3}
\]
where $V_m$ and $f_L$ represent the amplitude and frequency of the input line voltage, respectively. After a very short deadtime, the gate signal $v_{GS2}$ turns from a low level to a high level in this mode. Based on Equations (1)–(3), $i_{TP}$ decreases. On the contrary, $i_{LPFC}$ increases. The mode ends at the time when $i_{LPFC}$ becomes higher than $i_{TP}$.

**Figure 3.** The theoretic waveforms of key components.

### B. Mode II ($t_1 < t < t_2$)

The current $i_{S2}$ is the difference between $i_{LPFC}$ and $i_{TP}$. Hence, $i_{S2}$ changes its polarity when $i_{LPFC}$ becomes higher than $i_{TP}$ and $S_2$ is turned on at zero voltage. During this mode, the current equations are the same as Equations (1)–(3). Current $i_{LPFC}$ keeps increasing while $i_{TP}$ keeps decreasing. When $i_{TP}$ decreases to zero, the circuit operation enters Mode III.

### C. Mode III ($t_2 < t < t_3$)

The current $i_{TP}$ becomes negative at the beginning of this mode. Both $i_{TP}$ and $i_{LPFC}$ flow through $S_2$. The current $i_{LPFC}$ keeps increasing while the current $i_{TP}$ keeps decreasing. As soon as the gate signal $v_{GS2}$ turns from a high level to a low level, the circuit operation enters Mode IV.

### D. Mode IV ($t_3 < t < t_4$)

Both the current $i_{LPFC}$ and $i_{TP}$ divert from $S_2$ to flow through the parasitic capacitance of $S_1$ when $S_2$ is turned off. The parasitic capacitance of $S_2$ is discharged, and the voltage across $S_1$, $v_{DS1}$ decreases. Since the parasitic capacitance is quite small, it is completely discharged very rapidly. When energy on the parasitic capacitance of $S_1$ is totally released, $i_{LPFC}$ and $i_{TP}$ divert from the parasitic capacitance to flow through the intrinsic diode $D_{S1}$. The voltage across $S_1$, $v_{DS1}$ is clamped at zero volts. Thus, the ZVS
operation can be achieved. During this mode, the voltage across $L_{PFC}$ and the transformer primary winding can be respectively expressed as

$$v_{LPFC}(t) = v_{rec}(t) - V_{Cbus}, \quad (4)$$

$$v_{Tp}(t) = V_{Cbus} - V_{Cb1}, \quad (5)$$

The current $i_{LPFC}$ can be expressed as

$$i_{LPFC}(t) = i_{LPFC}(t_3) + \frac{v_{rec}(t) - V_{Cbus}}{L_{PFC}}(t - t_3), \quad (6)$$

Regarding a boost-type PFC converter, the dc-link voltage should be designed to be higher than the rectified voltage; therefore, the inductor current $i_{LPFC}$ starts to decrease. The magnetizing current $i_{Lm}$ and the primary current can be expressed as

$$i_{Lm}(t) = i_{Lm}(t_3) + \frac{V_{Cbus} - V_{Cb1}}{L_m}(t - t_3), \quad (7)$$

$$i_{Tp}(t) = i_{Lm}(t) + \frac{N_S}{N_P}I_{Lo}, \quad (8)$$

Since the primary voltage is positive, both $i_{Lm}$ and $i_{Tp}$ increase. On the other hand, the voltage across the secondary winding is positive. Therefore, the secondary winding supplies current to flow through $D_1$ and $D_4$ to the output inductor. After a very short deadtime, the gate signal $v_{GS1}$ turns from a low level to a high level. This mode ends when $i_{Tp}$ becomes zero and changes polarity.

E. Mode V ($t_4 < t < t_5$)

In this mode, $i_{Tp}$ is smaller than $i_{LPFC}$. The current flowing through $D_{S1}$ is equal to $i_{LPFC}$ minus $i_{Tp}$. When $i_{Tp}$ becomes higher than $i_{LPFC}$, $S_1$ is turned on at zero volts, and the circuit enters Mode VI.

F. Mode VI ($t_5 < t < t_6$)

In Figure 2f, $v_{GS1}$ remains at high level and $i_{LPFC}$ keeps decreasing. When $i_{LPFC}$ decreases to zero, the circuit enters Mode VII.

G. Mode VII ($t_6 < t < t_7$)

In Figure 2g, the trigger signal $v_{GS1}$ remains at a high state. The dc-link capacitor $C_{bus}$ keeps supplying energy via the transformer to the output. At the instant when $v_{GS1}$ turns into a low state, this mode ends and the circuit operation enters Mode I of the next high-frequency cycle.

3. Circuit Parameter Design

A. Transformer turn ratio $n$

To simplify the analysis, the voltage across the primary windings of the transformer is idealized as a square-wave voltage source with the amplitude swinging between $V_{Cbus} - V_{Cb1}$ and $-V_{Cb1}$, as shown in Figure 4. With the turn ratio of the primary winding to the secondary winding being $n:1$, the peak-to-peak value across the transformer secondary winding is $V_{Cbus}/n$. Referring to Figure 4, it is known that the average value of the voltage across the primary winding is zero.

$$(V_{Cbus} - V_{Cb1})(1 - D)T - V_{cb1}DT = 0, \quad (9)$$

where $D$ and $T$ are the duty ratio and the switching period of the active switch $S_2$. From (9), the following can be obtained:

$$V_{cb1} = (1 - D)V_{Cbus}, \quad (10)$$
At steady-state operation, the average voltage of the inductor is zero, i.e., the average value of the rectified voltage of the secondary winding is equal to the output voltage.

\[ V_{CD} = \frac{(V_{bus} - V_{cb1})(1 - D) + V_{cb1}D}{n} = V_o, \quad (11) \]

Substituting Equation (10) into Equation (11), the transformer turn ratio can be expressed as

\[ n = \frac{2D(1 - D)V_{bus}}{V_o}, \quad (12) \]

B. Output inductor \( L_o \)

The selection of the output filter inductance \( L_o \) is related to its current ripple. During the conducting interval of \( S_2 \), the current variation of \( L_o \) can be expressed as

\[ \Delta i_{L_o} = \frac{DT((1 - D)V_{bus}/n - V_o)}{L_o}, \quad (13) \]

By rearranging Equation (13), the inductance of the output inductor can be expressed as:

\[ L_o = \frac{DT((1 - D)V_{bus}/n - V_o)}{\Delta i_{L_o}}, \quad (14) \]

C. PFC Inductor \( L_{PFC} \)

In order to pursue the high power factor, the boost-type PFC converter should be operated at DCM. The inductance of the PFC inductor is inversely proportional to the output power and can be expressed as follows [21].

\[ L_{PFC} = \frac{\eta D^2 V_m^2}{2P_o f_s} \cdot y, \quad (15) \]

where \( P_o \) is the output power; \( f_s \) is the switching frequency; \( \eta \) is the circuit energy-conversion efficiency, and \( y \) is expressed as Equation (16).

\[ y = \frac{k^3}{\sqrt{k^2 - 1}} \left( 1 + \frac{2}{\pi} \sin^{-1} \frac{1}{k} \right) - k^2 - \frac{2}{\pi} \cdot k \left( k \equiv \frac{V_{bus}}{V_m} \right), \quad (16) \]

4. Illustrative Example and Experimental Results

A prototype of the proposed asymmetrical half-bridge dimmable LED driver was implemented and tested. The driven load is specified as 115 W (96 V/1.2 A), and the associated circuit specification is listed in Table 1. The parameter design, including the transformer turn ratio, the PFC inductor, and the output inductor, is based on the derivation in Section 3. The input filter inductor \( L_f \) and input filter
capacitor $C_f$ are selected with reference to [22]. By assigning the voltage ripple to be less than 5%, the value of the dc-link capacitor $C_{bus}$ is obtained with reference to [23]. The component parameters of the practical implementation are listed in Table 2.

### Table 1. Circuit Specification.

| Parameter                      | Value |
|--------------------------------|-------|
| Input voltage $V_{in}$         | 110 +/- 10% $V_{rms}$, 60 Hz |
| Rated output current $I_o$     | 1.2 A |
| Rated output voltage $V_o$     | 96 V  |
| Rated output power $P_o$       | 115 W |
| Switching frequency $f_s$      | 50 kHz|
| Full-load duty cycle $D$       | 0.45  |
| DC-link Voltage $V_{Cbus}$ at full load | 310 V |

### Table 2. Component parameters.

| Component                                      | Value     |
|------------------------------------------------|-----------|
| Transformer turn-ratio $n$                    | $N_p : N_s = 1.4 : 1$ |
| Block capacitor $C_{b1}$                      | 0.1 µF    |
| PFC inductor $L_{PFC}$                        | 0.340 mH  |
| Input filter inductor $L_f$                   | 2.2 mH    |
| Input filter capacitor $C_f$                  | 0.47 µF   |
| Output filter inductor $L_o$                  | 2.2 mH    |
| Output filter capacitor $C_o$                 | 470 µF    |
| DC-link capacitor $C_{bus}$                   | 100 µF    |
| MOSFET $S_1$, $S_2$                           | TOSHIBA 2SK2611 |

Figure 5 shows the dimming control circuit that mainly consists of a pulse-width-modulation controller (TL494) and a half-bridge driver (IR2302). The TL494 outputs a square-wave voltage of which the oscillation frequency is determined by the capacitor ($C_2$) connected to pin 5 and the resistor connected to pin 5 ($R_2$), and the pulse width is determined by the voltage at pin 4. The output of TL494 is connected to pin 2 of the IR2320. The IR2320 features a high-pulse current buffer stage designed for minimum driver cross-conduction. It outputs two complementary square-wave voltages (HO and LO) used to drive the high and low side MOSFETs ($S_1$ and $S_2$), respectively. The high-side gate driver (HO) is in phase with the logic input (pin 2). Therefore, by varying the resistor $R_1$ to adjust the pulse width of the TL494 output (E1), ASPWM control is achieved with respect to dimming the LEDs.

![Control circuit](image-url)
Figure 6 shows the measured voltages of the active switches $v_{GS1}$, $v_{GS2}$, $v_{DS1}$, $v_{DS2}$. It is obvious that prior to the instant when the gate voltages reach a high level, the voltages across the power switches reach nearly zero. This ensures ZVS operation of the active switches. Figure 7 shows the measured diode currents. As expected, these waveforms are consistent with the theoretical ones.

**Figure 6.** Voltage waveforms of active switches. ($v_{GS1}$ and $v_{GS2}$: 10V/div, $v_{DS1}$ and $v_{DS2}$: 200 V/div, Time: 5 µs/div).

**Figure 7.** Current waveforms of rectifying diodes. ($i_{D1}$, $i_{D2}$, $i_{D3}$, $i_{D4}$: 1 A/div, Time: 10 µs/div).

The LEDs are dimmed from 100% to 4% rated power. Figure 8 shows the waveforms of the gate voltage of $S_2$, the transformer secondary winding current, and the output filter inductor current at different output powers. It can be seen that the LED power is controlled by varying the duty ratio of $S_2$. From (15), for a given PFC inductor, the output power is proportional to the square of the duty ratio. As seen in Figures 7 and 8, there are negative and positive spike currents in the transformer secondary winding and the diodes on its secondary side. In addition, the negative and positive spike currents happen simultaneously. The spike current is the reverse recovery current of the diode. It is seen that the negative spike current happens when a pair of diodes are turned off, and this spike current flows through the transformer secondary winding and the other pair of diodes. Therefore, the positive spike current can be seen in the secondary winding and the other pair of diodes. Figure 9 shows the measured waveforms of the input voltage and PFC inductor current under heavy and light loads. Regardless of a heavy or light load, the peak values of PFC inductor currents always follow the track of the input voltage. Also, the PFC inductor is energized and de-energized at a very high frequency which is hundreds of multiples higher than the input-line frequency. Additionally, the PFC inductor currents coincide well with the input voltage at zero-crossing points, thus warranting the active power-factor correction of the proposed circuit. The measured power factor at different output powers is illustrated in Figure 10. At rated output power ($P_o = 115$ W), the power factor is as high as 0.99. The power factor decreases as the output power decreases and the power factor decreases to about 0.92 at 4% rated power. Figure 11 shows the harmonic spectrum of the input line current at the rated power operation. It can be seen that all harmonics are in compliance with the IEC 61000-3-2 Class C standard. The measured THDi is 12.64%. Figure 12 shows the prototype of the proposed LED driver.
Figure 8. Waveforms of $v_{GS2}$, $i_{Ts}$, and $i_{Lo}$ at (a) 100%, (b) 50%, (c) 25%, and (d) 4% rated power. ($v_{GS2}$: 10 V/div, $i_{Ts}$: 2 A/div, $i_{Lo}$: 1 A/div, Time: 10 µs/div).
Figure 9. Waveforms of the input voltage and PFC inductor current. (a) 100% and (b) 4% rated power. ($v_{in}$: 100 V/div, $i_{PFC}$: 1 A/div, Time: 5 ms/div).

Figure 10. Power factor versus output power.

Figure 11. Harmonic spectrum of the input line current.
5. Conclusions

This study developed and designed a single-stage dimmable LED driver. The circuit topology is derived by integrating a boost converter and an asymmetrical half-bridge converter. The lower-arm switch of the half-bridge converter is shared with the boost converter. The boost converter plays the role of the PFC converter. It operates at DCM to ensure a high power factor at the input line. By freewheeling the PFC inductor and the magnetizing current of the transformer to discharge the parasitic capacitance of the active switches, both active switches can be operated at ZVS, leading to high circuit efficiency. The measured circuit efficiency at rated output power is 92.7%. Experiments are performed to validate the effectiveness of the proposed circuit. The LEDs are dimmed by varying the duty ratio of the active switch. A high power factor is ensured when the LEDs are dimmed from 100% to 4% rated power.

Author Contributions: H.-L.C. and Y.-N.C. conceived and designed the circuit; L.-C.H. and H.-C.Y. performed circuit simulations and designed the parameters of the circuit components; W.-F.Y. carried out the prototype LED driver and measured as well as analyzed the experimental results; H.-L.C. wrote the paper, and S.-Y.C. revised it for submission. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the Ministry of Science and Technology, R.O.C. under the grant MOST 108-2221-E-150-017.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Alonso, J.M.; Perdigão, M.S.; Abdelmessih, G.Z.; Dalla Costa, M.A.; Wang, Y. SPICE modeling of variable inductors and its application to single inductor LED driver design. *IEEE Trans. Ind. Electron.* 2017, 64, 5894–5903. [CrossRef]
2. Rodgaard, M.S.; Weirich, M.; Andersen, M.A.E. Forward conduction mode controlled piezoelectric transformer based PFC LED driver. *IEEE Trans. Power Electron.* 2013, 28, 4841–4849. [CrossRef]
3. Li, Y.C.; Chen, C.L. A novel primary-side regulation scheme for single-stage high-power-factor AC-DC LED driving circuit. *IEEE Trans. Ind. Electron.* 2013, 60, 4978–4986. [CrossRef]
4. Lee, S.W.; Choe, H.J.; Yun, J.J. Performance improvement of a boost LED driver with high voltage gain for edge-lit LED backlights. *IEEE Trans. Circuits Syst. II* 2018, 65, 481–485. [CrossRef]
5. Luo, Q.; Huang, J.; He, Q.; Ma, K.; Zhou, L. Analysis and design of a single-stage isolated AC-DC LED driver with a voltage doubler rectifier. *IEEE Trans. Ind. Electron.* 2017, 64, 5807–5817. [CrossRef]
6. Wang, C.M.; Lin, C.H.; Yang, T.C. High-power-factor soft-switched dc power supply system. *IEEE Trans. Power Electron.* 2011, 26, 647–654. [CrossRef]
7. Mousavi, A.; Das, P.; Moschopoulos, G. A comparative study of a new ZCS DC-DC full-bridge boost converter with a ZVS active-Clamp converter. *IEEE Trans. Power Electron.* 2012, 27, 1347–1358. [CrossRef]
8. Liu, Y.C.; Huang, B.S.; Lin, C.H.; Kim, K.A.; Chiu, H.J. Design and implementation of a high power density active-clamped flyback converter. In Proceedings of the 2018 International Power Electronics Conference, Niigata, Japan, 20–24 May 2018; pp. 2092–2096.

9. Bhatt, K.; Gupta, R.A.; Gupta, N. Average model of isolated bidirectional dc-dc converter with auxiliary isolated clamp. In Proceedings of the 8th IEEE India International Conference on Power Electronics, Jaipur, India, 13–15 December 2018; pp. 1–5.

10. Alonso, J.M.; Viña, J.; Vaquero, D.G.; Martínez, G.; Osório, R. Analysis and design of the integrated double buck-boost converter as a high-power-factor driver for power-LED lamps. *IEEE Trans. Ind. Electron.* 2012, 59, 1689–1697. [CrossRef]

11. Wang, Y.; Guan, Y.; Ren, K.; Wang, W.; Xu, D. A single-stage LED driver based on BCM boost circuit and LLC converter for street lighting system. *IEEE Trans. Ind. Electron.* 2015, 62, 5446–5457. [CrossRef]

12. Chen, S.Y.; Li, Z.R.; Chen, C.L. Analysis and design of single-stage ac/dc LLC resonant converter. *IEEE Trans. Ind. Electron.* 2012, 59, 1538–1544. [CrossRef]

13. Cheng, C.A.; Chang, C.H.; Chun, T.Y.; Yang, F.L. Design and implementation of a single-stage driver for supplying an LED street-lighting module with power factor corrections. *IEEE Trans. Power Electron.* 2015, 30, 956–966. [CrossRef]

14. Wang, Y.; Alonso, J.M.; Ruan, X. A review of LED drivers and related technologies. *IEEE Trans. Ind. Electron.* 2017, 64, 5754–5765. [CrossRef]

15. Ma, J.; Wei, X.; Hu, L.; Zhang, J. LED driver based on boost circuit and LLC converter. *IEEE Access.* 2018, 6, 49588–49600. [CrossRef]

16. Singh, S.; Singh, B. A voltage controlled adjustable speed PMBLDCM drive using a single-stage PFC half-bridge converter. In Proceedings of the IEEE APEC 2010, Palm Springs, CA, USA, 21–25 February 2010; pp. 1976–1983.

17. Ou, S.; Hsiao, H. Analysis and design of a novel single-stage switching power supply with half-bridge topology. *IEEE Trans. Power Electron.* 2011, 26, 3230–3241. [CrossRef]

18. Taheri, M.; Milimonfared, J.; Bayat, H.; Fathi, S.H. Analysis, design and implementation of a new zero-voltage-switching interleaved asymmetrical half-bridge converter using an integrated transformer. *IET Power Electron.* 2012, 1912–1922. [CrossRef]

19. Choi, W.-Y.; Yoo, J.-S. A bridgeless single-stage half-bridge AC/DC converter. *IEEE Trans. Power Electron.* 2011, 26, 3884–3895. [CrossRef]

20. Muhlethaler, J.; Biela, J.; Kolar, J.W.; Ecklebe, A. Core losses under the DC bias condition based on Steinmetz parameters. *IEEE Trans. Power Electron.* 2012, 27, 953–963. [CrossRef]

21. Liang, T.J.; Kang, S.C.; Cheng, C.A.; Lin, R.L.; Chen, J.F. Analysis and design of single-stage electronic ballast with bridgeless PFC configuration. In Proceedings of the 29th Annual Conference on IEEE Industrial Electronics Society (IECON 2003), Roanoke, VA, USA, 2–6 November 2003; pp. 502–508.

22. Moo, C.S.; Yen, H.C.; Hsieh, Y.C.; Chuang, Y.C. Integrated design of EMI filter and PFC low-pass filter for power electronic converters. *Proc. Inst. Elect. Eng. Elect. Power Appl.* 2003, 150, 39–44. [CrossRef]

23. Chang, Y.N. Self-excited single-stage power factor correction driving circuit for LED lighting. *Hindawi Publ. Corp. J. Nanomater.* 2014. [CrossRef]

© 2020 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).