Self-Assembled Monolayers (SAMs)/Al$_2$O$_3$ Double Layer Passivated InSnZnO Thin-Film Transistor

WEI ZHONG$^{1}$, RUOHE YAO$^{1}$, ZHIJIAN CHEN$^{1}$, LINFENG LAN$^{2}$, AND RONGSHENG CHEN$^{1}$, (Senior Member, IEEE)

$^{1}$School of Electronic and Information Engineering, South China University of Technology, Guangzhou 510640, China
$^{2}$State Key Laboratory of Luminescent Materials and Devices, South China University of Technology, Guangzhou 510640, China

Corresponding authors: Rongsheng Chen (chenrs@scut.edu.cn) and Zhijian Chen (chenzhijian@scut.edu.cn)

This work was supported in part by the National Key Technologies Research and Development Program under Grant 2016YFB0401303, in part by the Key-Area Research and Development Program of Guangdong Province under Grant 2019B010140002, in part by the Science and Technology Program of Guangdong Province under Grant 2019A050503005, in part by the Natural Science Foundation of Guangdong under Grant 2019A1515011820 and Grant 2018A030310360, in part by the Program for Guangdong High-level Talents, and in part by the Fundamental Research Funds for the Central Universities under Grant 2018MS12 and Grant 2019XX16.

ABSTRACT We fabricated high-performance InSnZnO (ITZO) thin-film transistors (TFTs) with self-assembled monolayers (SAMs)/Al$_2$O$_3$ double passivation layers (PVLs). The presented SAMs/Al$_2$O$_3$ double passivation leads to high-performance ITZO TFTs with a steep subthreshold slope (\(\sim 85\) mV/dec), a low threshold voltage (\(\sim 0.9\) V), high mobility (\(\sim 19.8\) cm$^2$/V$^{-1}$s$^{-1}$), and high on-off current ratio (\(\sim 8.7 \times 10^9\)). Moreover, compared to devices with Al$_2$O$_3$ PVL, ITZO TFTs with SAMs/Al$_2$O$_3$ double PVLs show better stability in ambient air with a relative humidity of 60% under positive bias stress (PBS) and negative bias stress (NBS). This enhanced stability is attributed to the presence of a high-quality SAM/Al$_2$O$_3$ dual PVL, which not only inhibits Vo-related trap sites and reduces overall trap density, but also protects the back-channel from environmental influences.

INDEX TERMS InSnZnO, thin-film transistors, self-assembled monolayers, double passivation, stability.

I. INTRODUCTION

In recent years, amorphous oxide semiconductor (AOS) transparent thin-film transistors (TFTs) have attracted widespread attention in driving AMLCDs in next-generation flat panel displays and AMOLED displays. Although AOS TFTs have superior performance compared to traditional silicon-based TFTs, their instability is still one of the key issues to be solved because they are sensitive to the environment, such as instability under gate bias.

In the commercial application of AOS TFTs, high-quality performance and high stability in a humid environment are essential [1]–[6]. In order to improve the stability of the AOS TFT, a passivation layer is necessary to protect the AOS active layer from the surrounding environment. As an alumina (Al$_2$O$_3$) passivation layer (PVL) is a good barrier layer, it can effectively reduce atmosphere-induced instabilities in the backchannel of AOS film when it reaches a certain thickness [7]–[9]. In addition, the Al$_2$O$_3$ passivation layer can inhibit the oxygen atoms in the AOS film from escaping to form Vo during the annealing process, thereby significantly improving the stability of the AOS TFT, especially the negative bias stress (NBS) stability [9], [10]. Compared to Al$_2$O$_3$, vapor-phase self-assembled monolayers are an environmental barrier layer with better humidity resistance [11], [12]. Vapor-phase self-assembled monolayers (SAMs), made of organosilane compounds with different functions, can be used to modify the surface characteristics of oxides to form a hydrophobic layer, which helps improve the reliability of the device in humid environments [11]–[15]. For example, the present authors’ research group has successfully applied different self-assembled monolayer films to the backchannel surface of metal oxide TFTs, leading to high positive bias stress (PBS) stability for TFT devices in humid environments [11]. However, since the self-assembled monolayer is very thin (2–6 nm), its ability to inhibit the adsorption and diffusion of oxygen molecules is limited, and the improvement of the negative bias (NBS) stability of TFT devices...
is limited [11]. In this paper, combining the advantages of both SAMs and Al$_2$O$_3$ PVLs, self-assembled monolayers (SAMs)/Al$_2$O$_3$ dual PVLs were designed to improve the reliability of ITZO TFTs. As a result, the electrical performance and device stability of ITZO TFTs have been significantly improved, including the stability of NBS and PBS in a humid environment.

**FIGURE 1. Schematic structure of ITZO thin film transistor with SAMs/Al$_2$O$_3$ dual PVLs.**

**II. EXPERIMENTAL**

Fig.1 shows the device structure of a bottom gate ITZO TFT with SAMs/Al$_2$O$_3$ dual PVLs. A gate electrode was prepared by depositing a 300-nm-thick Al-Nd alloy layer (3 wt% Nd) on a glass substrate by DC sputtering and was patterned by photolithography and a wet etching process. An anodization process is then performed to form a 200-nm-thick AlO$_x$:Nd layer as the gate dielectric layer. Subsequently, a 60-nm-thick ITZO film was deposited on the AlO$_x$:Nd film by a ZnO target and ITO target (90 wt% In$_2$O$_3$ and 10 wt% SnO$_2$) co-sputtering with an Ar/O$_2$ flow rate of 9/6 sccm. During the co-sputtering process, the sputtering power of ITO and ZnO was set to 105 W DC and 130 W RF, respectively. X-ray photoelectron spectroscopy (XPS) analysis revealed that the metal cation ratio of the deposited ITZO film was In: Sn: Zn = 52.9%: 4.2%: 42.9%. The source/drain (S/D) electrodes were prepared by sputtering 240 nm thick ITO in a pure Ar atmosphere. Shadow masks were used to pattern the ITZO channel and S/D electrodes, defining a channel width/length of 300 μm/300 μm. To fabricate the Al$_2$O$_3$ passivation layer, 80-nm thick Al$_2$O$_3$ was deposited by pulsed laser deposition (PLD) with an O$_2$ flow rate of 450 mJ. Subsequently, a post-annealing process of the device was performed on a hot plate of 300 °C in air for 2 hours. For the SAM treatment, n-octyltriethoxysilane (OTES) was used to react with the Al$_2$O$_3$ surface of the device in the vapor phase by heat treatment. The device was inverted on a tungsten evaporation boat, and 0.05 ml of siloxane polymer droplets were dropped on the evaporation boat. This assembly was heated to 120 °C for 2 hours in a vacuum oven, and then the device surface was cooled to room temperature. The thickness of SAMs measured by the ellipsometer is ~6nm.

**FIGURE 2. (a) Transfer characteristics of the ITZO TFTs without a PVL, with an Al$_2$O$_3$ PVL, and with SAMs/Al$_2$O$_3$ dual PVLs. The output characteristics of the ITZO TFT (b) without a PVL, (c) with an Al$_2$O$_3$ PVL, and (d) with SAMs/Al$_2$O$_3$ dual PVLs.**

**TABLE 1. Extracted parameters of the ITZO TFTs without passivation, with Al$_2$O$_3$ PVL, and with SAMs/Al$_2$O$_3$ dual PVLs. The data are collected from 8 TFTs.**

| sample                  | $\mu$FE (cm$^2$/V·s) | $V_{th}$ (V) | SS (V/dec) | $I_{on}/I_{off}$ |
|-------------------------|-----------------------|--------------|------------|-----------------|
| without PVL             | 10.4±0.8              | 2.0±0.2      | 0.145±0.018 | 3.1×10$^7$      |
| Al$_2$O$_3$ PVL          | 15.5±0.5              | 2.9±0.3      | 0.093±0.011 | 3.8×10$^7$      |
| SAMs/Al$_2$O$_3$ dual PVLs | 19.8±0.7              | 0.9±0.2      | 0.085±0.014 | 8.7×10$^7$      |

**III. RESULTS AND DISCUSSION**

Fig. 2(a) shows the transfer characteristics of the ITZO TFTs without a PVL, with an Al$_2$O$_3$ PVL, and with SAMs/Al$_2$O$_3$ dual PVLs. The extraction parameters of the ITZO TFTs with different PVLs are summarized in Table 1. Herein, the field-effect mobility ($\mu_{FE}$) can be obtained by transconductance ($g_m$) at a low drain voltage ($V_{ds}$ = 0.1V), which is given by [16]

$$\mu_{FE} = \frac{L g_m}{W C_{ox} V_{ds}}$$

(1)

$$g_m = \frac{A_{ds}}{\partial V_{gs}}$$

(2)

where $L$, $W$, and $C_{ox}$ are the channel length, width, and gate dielectric unit capacitance, respectively. The threshold swing (SS) is calculated by

$$SS = \left( \frac{d \log (I_{ds})}{d V_{gs}} |_{max} \right)^{-1}$$

(3)

$V_{th}$ is defined as the corresponding gate voltage ($V_{gs}$) when the drain current ($I_{ds}$) reaches W/L×100nA at $V_{ds}$ = 10.1V. As shown in Fig. 2(a), the ITZO TFT without the passivation layer exhibits a large $I_{off}$ (~10$^{-12}$A) and a small $I_{on}$ (~10$^{-5}$A), corresponding small current ratio ($I_{on}/I_{off}$),
and a small field-effect mobility ($\mu_{FE}$), indicating poor electrical performance. While the ITZO TFTs with Al$_2$O$_3$ passivation exhibit dramatically modulated electrical performance, and have low $I_{off}$ ($\sim$10$^{-14}$ A), low subthreshold swing (SS) ($\sim$93 mV/dec), large $I_{on}/I_{off}$ ($\sim$10$^9$), and large $\mu_{FE}$ ($\sim$15.5 cm$^2$/V·s). This result is consistent with previous research results [17], [18]. More importantly, compared with Al$_2$O$_3$ passivation, the device performance is further enhanced after double passivation of SAMs/Al$_2$O$_3$, with a high field-effect mobility ($\mu_{FE}$) of 19.8 cm$^2$/V·s, a large $I_{on}/I_{off}$ of 8.7 $\times$ 10$^9$, and a low subthreshold swing (SS) of 85 mV/dec. The SS value of the oxide TFT devices is closely related to the total charge trap density ($N_T$), including the bulk channel layer ($N_{bulk}$) and the gate insulator/active layer interface traps ($N_{it}$). The relationship between SS and $N_T$ can be expressed as [7]

$$N_T = N_{bulk} + N_{it} = \frac{C_{ox}}{q} \left( \frac{SS \log (e)}{k_B T/q} - 1 \right) \tag{4}$$

where $C_{ox}$ is the gate capacitance per unit area (38 nF/cm$^2$), $q$ is the elementary charge, and $k_B T$ is the thermal energy. Accordingly, the ITZO TFTs with SAMs/Al$_2$O$_3$ dual PVLs exhibit a low $N_T$ value ($1.0 \times 10^{11}$ cm$^{-2}$/eV) compared to unpassivated ($3.4 \times 10^{11}$ cm$^{-2}$/eV) and Al$_2$O$_3$ passivated ($1.3 \times 10^{11}$ cm$^{-2}$/eV) ITZO TFTs. The output characteristics of the ITZO TFT without a PVL, with an Al$_2$O$_3$ PVL, and with SAMs/Al$_2$O$_3$ dual PVLs are shown in Fig. 2(b), (c) and (d), respectively. Comparing the drain current in the saturation region of the ITZO TFT without PVL, with Al$_2$O$_3$ PVL, and with SAMs/Al$_2$O$_3$ double PVL, the ITZO TFT with SAMs/Al$_2$O$_3$ double PVL has the highest drain current. In addition, there is no obvious current crowding in the low source/drain voltage ($V_{ds}$) region, indicating that an excellent ohmic contact is formed between the source/drain electrode and the channel.

Compared to unpassivated devices, the threshold voltage of ITZO TFT with an Al$_2$O$_3$ PVL has a positive shift from 2.0 V to 2.9 V. Threshold voltage is expressed by the following formula [19]:

$$V_{th} = \phi_{ms} - \frac{Q_1}{C_{ox}} - \frac{Q_d}{C_{ox}} + 2\phi_F \tag{5}$$

$$\phi_F = \frac{E_i - E_F}{q} \phi_F = \frac{E_i - E_F}{q} \tag{6}$$

where $Q_1$, $Q_d$, $C_{ox}$, and $\phi_{ms}$ is the effective MOS interface charge per unit area, depletion region charge per unit area, insulation capacitance per unit area, and metal-semiconductor work function potential difference, respectively, and $E_i$ and $E_F$ is the Fermi intrinsic level and the equilibrium Fermi level, respectively. All parameters mentioned above, except $Q_1/C_{ox}$, are affected by the charge carrier concentration of the channel layer, while $Q_d/C_{ox}$ is affected by the total trap density consisting of the bulk trap density and interface trap density [19]. Therefore, the positive shift of $V_{th}$ and the reduction of SS and $I_{on}/I_{off}$ are all benefits from the reduction of oxygen vacancies ($V_O$) and electron concentration in the ITZO channel [17], [18], [20]. It is well known that $V_O$ (as donor-like states) is related to the electrons generated in the ITZO channel. In order to confirm the beneficial effects of the Al$_2$O$_3$ passivation layer, XPS was used to examine the O 1s spectra of the back-channel of the ITZO TFT without a PVL (Fig. 3(a)), with an Al$_2$O$_3$ PVL (Fig. 3(b)), and with SAMs/Al$_2$O$_3$ double PVLs (Fig. 3(c)). As shown in Fig. 3(a)-(c), the XPS spectra of the O 1s peak can be divided into three peaks: O1, O2, and O3, and further fitted by the Gaussian–Lorentzian. The O1 peak centered at $\sim$530.4 eV corresponds to the oxygen bonded in the lattices, such as Zn–O, In–O, and Sn–O [21], [22]. The O2 peak centered at $\sim$531.2 eV corresponds to oxygen deficiencies in the lattices, such as $V_O$. The O3 peak centered at $\sim$532.3 eV is attributed to chemisorbed oxygen, such as adsorbed O$_2$, H$_2$O, and the bonded oxygen in -OH groups [21], [22]. It is shown that the relative area of the O2 peak is reduced from 27.5% to 14.0% after Al$_2$O$_3$ passivation. It is reported that Al$_{3+}$ as an oxygen binder can effectively reduce $V_O$ in AOS film [17], [18]. This could be due to the lower standard electrode potential (SEP) ($\sim$1.66 V) of Al than that of In ($\sim$0.342 V), Zn ($\sim$0.761 V), and Sn ($\sim$0.13 V), which could combine easily with the oxygen vacancies ($V_O$) [17], [19], [20]. This results in a reduction of oxygen vacancy and a decrease of electron concentration in the ITZO channel, and the $V_{th}$ of the device is positively shifted accordingly.

Compared to the ITZO TFT with an Al$_2$O$_3$ PVL, the device performance is further enhanced after double passivation of SAMs/Al$_2$O$_3$, and the device hysteresis has been significantly reduced, as shown in Fig. 2(a). The origin of hysteresis in oxide TFT is related to the shallow trap state produced by the water adsorbed on the semiconductor surface [6], [23]. Reducing the adsorption of water on the back-channel of the device is helpful to reduce the hysteresis of the device and improve the electrical performance of the device, such as the
on current and the field-effect mobility [11], [13], [23]. This can be confirmed by XPS results. Fig. 3(d) shows the XPS depth profile for the back-channel of the ITZO TFT with SAMs/Al₂O₃ dual PVLs. It shows that SAMs only exist with the Al₂O₃ surface and no element diffusion from SAMs to Al₂O₃ and ITZO layer. Comparing the XPS results of the ITZO TFT with Al₂O₃ PVL and with SAMs/Al₂O₃ dual PVLs, the relative area of the O3 peak is reduced from 32.1% to 18.9% after the surface passivation of SAMs, as shown in Fig. 3 (b) and (c). This indicates that the adsorption process of water or oxygen molecules on the back-channel of the ITZO TFT is effectively suppressed [23]. SAMs with silane groups are usually applied to oxide surfaces such as SiO₂, ITZO, and Al₂O₃ to adjust the interface trap density, charge carrier density, work function, surface energy, etc. [11], [24], [25]. To investigate the beneficial effect of SAM treatment on the Al₂O₃ PVL, specific analyses for oxide and hydroxide were done by deconvoluting the O 1s spectra of the Al₂O₃ PVL and SAMs/Al₂O₃ dual PVLs, as shown in Fig. 4 (a) and (b). The O 1s peak was deconvoluted into two peaks centered at 530.3 eV and 531.7 eV, which is corresponded to the binding energy of the oxide and the hydroxyl groups [20]. After SAM treatment, the number of hydroxyl groups has a decrease for the Al₂O₃ PVL, which is from 10.7% to 6.8%. A small number of hydroxyl groups can ensure TFT reliability [20].

For the SAM treatment, the anchor groups of silane SAMs undergo dehydration, condensation reaction with the hydroxyl groups on the surface of the oxide to form a strong chemical bond, while the hydrophobic surface is formed by the hydrophobic functional group (-CH₃) of silane SAMs, as shown in Fig. 5 (d). Since H₂O adsorbed on the backchannel surface of the TFT seriously affects the electrical characteristics of the device, suppressing the adsorption/desorption effect on the backchannel surface is beneficial to the improvement of the device performance [1], [2], [5], [6]. Fig. 5 (a)-(c) shows the water contact angle measurement image of ITZO film without a PVL, with an Al₂O₃ PVL, and with a SAMs/Al₂O₃ dual PVL, respectively. Generally, solid surfaces are divided into hydrophilic and hydrophobic surfaces according to the size of the water contact $\theta$. When $\theta > 90^\circ$, the solid surface appears hydrophobic, and when $\theta < 90^\circ$, the solid surface appears hydrophilic. According to the results of the contact angle test, the surface of ITZO is changed from hydrophilic to hydrophobic after passivation by SAMs/Al₂O₃. It can be seen that compared with the lower hydrophilicity of the Al₂O₃ passivation layer, the modification of the Al₂O₃ passivation layer by SAMs further strengthens the hydrophobic property of the passivation layer and enhances the barrier ability of the passivation layer to water in the air, which is conducive to the improvement of the device performance, especially the stability of the device [11]–[14], [26].

Positive bias (PBS) and negative bias (NBS) tests were used to confirm the stability of TFTs with different passivation layers. For the positive/negative bias stress (PBS/NBS) test, $V_{gs} = +10$ V / $-10$ V was applied to the device, and the relative humidity (RH) of ambient air is 60%. The $V_{th}$ shifts of the ITZO TFTs with different passivation layers under PBS/NBS are compared in Fig. 6. Without passivation, the device shows poor bias stability with a $\Delta V_{th}$ shift of 4.0/1.9 V under PBS/NBS for 3600 s, as shown in Fig. 6 (a) and (b). In contrast, ITZO TFTs with an Al₂O₃ PVL have better bias stability, especially negative bias stability (Fig. 6 (d)), showing only a $\Delta V_{th}$ shift of 0.1 V for 3600 s. The Al₂O₃ PVL significantly improves the stability of ITZO TFTs by suppressing the $V_{gs}$-related trap sites formed in the ITZO film due to the escape of oxygen atoms [8], [18]. However, there is still a large positive bias drift (Fig. 6 (c)), which indicates that Al₂O₃ film with a thickness of 80 nm cannot effectively block the invasion of H₂O molecules in the ambient air [9], [11], [27]. Compared to the ITZO TFT with an Al₂O₃ PVL, the bias stability of the device is further enhanced after double passivation of SAMs/Al₂O₃, as shown in Fig. 6 (e) and (f). This is mainly due to the modification of the Al₂O₃ passivation layer by SAMs, which makes a thin hydrophobic layer formed on the surface of the Al₂O₃ passivation layer. The hydrophobic layer enhances the barrier ability of the passivation layer to H₂O molecules and improves the effect of the passivation layer [11], [12], [26].
The electrical stability of the ITZO TFTs with SAMs/Al₂O₃ dual PVLs under various humidity conditions was also investigated, as shown in Fig. 7 (a). All samples were subjected to different humidity conditions for 2 h. It can be seen that the transfer curves of the ITZO TFTs with SAMs/Al₂O₃ dual PVLs nearly coincide under different relative humidities (RH). Fig. 7 (b) shows the change in Vₜh, SS, and field-effect mobility (μ/μₒ) of the ITZO TFTs with SAMs/Al₂O₃ dual PVLs under different relative humidities. Overall, the Vₜh, SS, and field-effect mobility (μ/μₒ) did not change significantly under different humidity conditions and remained within acceptable ranges, indicating the device with SAMs/Al₂O₃ dual PVLs has excellent humidity resistance [13], [23]. The -CH₃ group of the SAM is hydrophobic, and a dense layer of alkyl chains is capable to serve as a diffusion barrier, which can isolate the surface of the device from H₂O molecules in the environment. Therefore, SAMs/Al₂O₃ dual PVLs can provide stable transistor performance under different humidity environments [13].

IV. CONCLUSION

In summary, ITZO TFT passivated by a SAMs/Al₂O₃ double-layer film is fabricated. The SAMs/Al₂O₃ double-layered passivation structure enhances the performance of ITZO TFTs through the film’s intrinsic properties. The Al₂O₃ passivation acts as an effective carrier suppressor by Al³⁺ acting as an oxygen binder to reduce Vₒ in the back-channel region. The dense alkyl chain layer of SAMs can act as a diffusion barrier, preventing reactive substances such as O₂ and H₂O from reaching the surface. As a result, the ITZO TFT with SAMs/Al₂O₃ dual PVLs has excellent device performance and good bias stability in humid environments. Overall, the SAMs/Al₂O₃ double passivation layer structure combines the advantages of Al₂O₃ passivation and SAMs passivation, while reducing the number of Vo-related trap sites, it can also have a good passivation effect on the device. This provides a new structure for improving the reliability of ZnO-based transparent metal oxide TFTs.

REFERENCES

[1] X. Zhou, Y. Shao, L. Zhang, X. Xiao, D. Han, Y. Wang, and S. Zhang, “Oxygen adsorption effect of amorphous InGaZnO thin-film transistors,” IEEE Electron Device Lett., vol. 38, no. 4, pp. 465–468, Apr. 2017, doi: 10.1109/LED.2017.266881.

[2] B. K. Sharma and J.-H. Ahn, “Instability in an amorphous In-Ga-Zn–O field effect transistor upon water exposure,” J. Phys. D, Appl. Phys., vol. 49, no. 5, p. 55102, 2016, doi: 10.1088/0022-3727/49/5/055102.

[3] J. W. Hennek, J. Smith, A. Yan, M.-G. Kim, W. Zhao, V. P. Dravid, A. Facchetti, and T. J. Marks, “Oxygen ‘getter’ effects on microstructure and carrier transport in low temperature combustion-processed a-InXZnO (X = Ga, Sc, Y, La) transistors,” J. Amer. Chem. Soc., vol. 135, no. 29, pp. 10729–10741, 2013, doi: 10.1021/ja403586x.

[4] D.-H. Lien, J. R. D. Retamal, J.-J. Ke, C.-F. Kang, and J.-H. He, “Surface effects in metal oxide-based nanodevices,” Nanoscale, vol. 7, no. 47, pp. 19874–19884, 2015, doi: 10.1039/c5nr06494c.

[5] K. Hoshino, B. Yeh, and J. F. Wagner, “Impact of humidity on the electrical performance of amorphous semiconductor thin-film transistors,” J. Soc. Inf. Display, vol. 21, no. 7, pp. 310–316, Jul. 2013, doi: 10.1002/jsid.184.

[6] M. Fakhri, H. Johann, P. Görn, and T. Riedel, “Water as origin of hysteresis in zinc tin oxide thin-film transistors,” ACS Appl. Mater. Interfaces, vol. 4, no. 9, pp. 4453–4456, Sep. 2012, doi: 10.1021/am301308y.

[7] A. Abiliz, D. Wan, J.-Y. Chen, L. Xu, J. He, Y. Yang, H. Duan, C. Liu, C. Jiang, H. Chen, T. Guo, and L. Liao, “Enhanced reliability of In-Ga–ZnO thin-film transistors through design of dual passivation layers,” IEEE Trans. Electron Devices, vol. 65, no. 7, pp. 2844–2849, Jul. 2018, doi: 10.1109/TED.2018.2836146.

[8] S.-Y. Huang, T.-C. Huang, M.-C. Chen, T.-C. Chen, F.-Y. Jian, Y.-C. Chen, H.-C. Huang, and D.-S. Gan, “Improvement in the bias stability of amorphous InGaZnO TFTs using an Al₂O₃ passivation layer,” Surf. Coat. Technol., vol. 231, pp. 117–121, Sep. 2013, doi: 10.1016/j.surfcoat.2011.12.047.

[9] D. Zhou, Z. Hu, Q. Wu, L. Xu, H. Xie, and C. Dong, “Light illumination stability of amorphous InGaZnO thin film transistors with sputtered Al₂O₃ passivation in various thicknesses,” Jpn. J. Appl. Phys., vol. 53, no. 12, 2014, Art. no. 121103, doi: 10.7567/JJAP.53.121103.

[10] C. H. Ahn, S. H. Kim, Y. Kim, and H. K. Cho, “Extremely thin Al₂O₃ surface-passivated nanocrystalline ZnO thin-film transistors designed for low process temperature,” J. Amer. Ceram. Soc., vol. 99, no. 4, pp. 1305–1310, 2016, doi: 10.1111/jace.14053.
[11] W. Zhong, G. Li, L. Lan, B. Li, and R. Chen, “InSnZnO thin-film transistors with vapor-phase self-assembled monolayer as passivation layer,” IEEE Electron Device Lett., vol. 39, no. 11, pp. 1680–1683, Nov. 2018, doi: 10.1109/LED.2018.2872352.

[12] A. Rissanen, K. Tappura, M. Laamanen, R. Puurunen, E. Färn, M. Ritala, and M. Leskelä, “Vapor-phase self-assembled monolayers for improved MEMS reliability,” in Proc. 9th IEEE Sensors Conf., Nov. 2010, pp. 767–770, doi: 10.1109/SENSOR.2010.5690769.

[13] T. Lim, J. Bong, E. M. Mills, S. Kim, and S. Ju, “Highly stable operation of metal oxide nanowire transistors in ambient humidity, water, blood, and oxygen,” ACS Appl. Mater. Interfaces, vol. 7, no. 30, pp. 16296–16302, Aug. 2015, doi: 10.1021/acsami.5b03038.

[14] A. Vilan and D. Cahen, “Chemical modification of semiconductor surfaces for molecular electronics,” Chem. Rev., vol. 117, no. 5, pp. 4624–4666, Mar. 2017, doi: 10.1021/acs.chemrev.6b00746.

[15] T. Lim, J. Han, K. Seo, M.-K. Joo, J.-S. Kim, W.-Y. Kim, G.-T. Kim, and S. Ju, “Fabrication of controllable and stable InOx nanowire transistors using an octadecylphosphonic acid self-assembled monolayer,” Nanotechnology, vol. 26, no. 14, 2015, Art. no. 145203, doi: 10.1088/0957-4484/26/14/145203.

[16] J. H. Choi, J.-H. Yang, S. Nam, J.-E. Pi, H.-O. Kim, O.-S. Kwon, E.-S. Park, C.-S. Hwang, and S. H. Cho, “InZnO/AIInSnZnO bilayer oxide thin-film transistors with high mobility and high uniformity,” IEEE Electron Device Lett., vol. 37, no. 10, pp. 1295–1298, Oct. 2016, doi: 10.1109/LED.2016.2602284.

[17] Y. Ding, C. Fan, C. Fu, Y. Meng, G. Liu, and F. Shan, “High-performance indium oxide thin-film transistors with aluminum oxide passivation,” IEEE Electron Device Lett., vol. 40, no. 12, pp. 1949–1952, Dec. 2019, doi: 10.1109/LED.2019.2947762.

[18] P.-T. Liu, C.-H. Chang, and C.-S. Fuh, “Enhancement of reliability and stability for transparent amorphous indium-zinc-tin-oxide thin film transistors,” RSC Adv., vol. 6, no. 108, pp. 106374–106379, 2016, doi: 10.1039/c6ra22423g.

[19] Y. Zhang, H. Zhang, J. Yang, X. Ding, and J. Zhang, “Solution-processed ytrrium-doped ITO semiconductors for high-stability thin film transistor applications,” IEEE Trans. Electron Devices, vol. 66, no. 12, pp. 5170–5176, Dec. 2019, doi: 10.1109/TED.2019.2949702.

[20] S. Hong, S. P. Park, Y.-G. Kim, B. H. Kang, J. W. Na, and H. J. Kim, “Low-temperature fabrication of an HfO2 passivation layer for amorphous indium-gallium-zinc oxide thin film transistors using a solution process,” Sci. Rep., vol. 7, no. 1, 2017, Art. no. 16265, doi: 10.1038/s41598-017-16585-x.

[21] W. Zhong, G. Li, L. Lan, B. Li, and R. Chen, “Effects of annealing temperature on properties of InSnZnO thin film transistors prepared by co-sputtering,” RSC Adv., vol. 8, no. 61, pp. 34817–34822, Oct. 2018, doi: 10.1039/C8RA06692B.

[22] S. Deng, R. Chen, G. Li, Z. Xia, M. Zhang, W. Zhou, M. Wong, and H.-S. Kwok, “Investigation of high-performance ITO-stabilized ZnO TFTs with hybrid-phase microstructural channels,” IEEE Trans. Electron Devices, vol. 64, no. 8, pp. 3174–3182, Aug. 2017, doi: 10.1109/TED.2017.2711199.

[23] W. Xu, D. Liu, H. Wang, L. Ye, Q. Miao, and J.-B. Xu, “Facile passivation of solution-processed InZnO thin-film transistors by octadecylphosphonic acid self-assembled monolayers at room temperature,” Appl. Phys. Lett., vol. 104, no. 17, Apr. 2014, Art. no. 173504, doi: 10.1063/1.4874303.

[24] J. Roh, C.-M. Kang, J. Kwak, C. Lee, and B. J. Jung, “Overcoming tradeoff between mobility and bias stability in organic field-effect transistors according to the self-assembled monolayer chain lengths,” Appl. Phys. Lett., vol. 104, no. 17, Apr. 2014, Art. no. 173301, doi: 10.1063/1.4874263.

[25] R. Acharya, B. Peng, P. K. L. Chan, G. Schmitz, and H. Klauk, “Achieving ultralow turn-on voltages in organic thin-film transistors: Investigating fluorooalkylphosphonic acid self-assembled monolayer hybrid dielectrics,” ACS Appl. Mater. Interfaces, vol. 11, no. 30, pp. 27104–27111, Jul. 2019, doi: 10.1021/acsami.9b04361.

[26] Y. J. Tak, S. T. Keene, B. H. Kang, W.-G. Kim, S. J. Kim, A. Salleo, and H. J. Kim, “Multifunctional, room-temperature processable, heterogeneous organic passivation layer for oxide semiconductor thin-film transistors,” ACS Appl. Mater. Interfaces, vol. 12, no. 2, pp. 2615–2624, Jan. 2020, doi: 10.1021/acsami.9b16898.

[27] P. Xiao, L. Lan, T. Dong, Z. Lin, W. Shi, R. Yao, X. Zhu, and J. Peng, “InGaZnO thin-film transistors with back channel modification by organic self-assembled monolayers,” Appl. Phys. Lett., vol. 104, no. 5, 2014, Art. no. 051607, doi: 10.1063/1.4864313.

WEI ZHONG received the Ph.D. degree in electrical engineering from the South China University of Technology, Guangzhou, China, in 2019. His current research interests include oxide-based-semiconductor TFT and process development on flexible substrate, flexible active matrix display, and flexible electronics.

RUOHE YAO received the B.S. degree in sciences from Sun Yat-sen University, Guangzhou, China, in 1982, and the Ph.D. degree from the Chinese Academy of Sciences, China, in 2004. He was a Professor with the Department of Physics and the Dean of the School of Sciences, Shantou University, Shantou, China. Since 2002, he has been a Professor with the Department of Physics and the Vice-Dean of the School of Physics, South China University of Technology, Guangzhou, where he is currently a Professor with the School of Electronic and Information Engineering. His current research interests include semiconductor device and microelectronics techniques.

ZHIJIAN CHEN received the B.S., M.S., and Ph.D. degrees from the South China University of Technology, Guangzhou, China, in 2001, 2004, and 2016, respectively. Since 2004, he has been a Senior Engineer with IC design companies. Since 2017, he has also been an Associate Professor with the South China University of Technology. He recently focuses his research on high-performance RF front-end circuits, reconfigurable analog and digital circuit theory, and thin film transistors circuits.

LINFENG LAN received the Ph.D. degree from the South China University of Technology, Guangzhou, China, in 2010. He joined the South China University of Technology as a Research Fellow. His current research interests include thin-film transistors based on organic semiconductors or oxide semiconductors and AMOLED displays.

RONGSHENG CHEN (Senior Member, IEEE) received the Ph.D. degree from the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, in 2013. His current research interests include novel compound thin-film transistors based on ZnO, IGZO, GaN, and their application in active matrix displays.