An Accurate Hybrid Delay Model for Multi-Input Gates

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Abstract—In order to facilitate the analysis of timing relations between individual transitions in a signal trace, dynamic digital timing analysis offers a less accurate but much faster alternative to analog simulations of digital circuits. This primarily requires gate delay models that also account for the fact that the input-to-output delay of a particular input transition also depends on the temporal distance to the previous output transitions. In the case of multi-input gates, the delay also experiences variations caused by multi-input switching (MIS) effects, i.e., transitions at different inputs that occur in close temporal proximity. In this paper, we advocate the development of hybrid delay models for CMOS gates obtained by replacing transistors with time-variant resistors. We exemplify our approach by applying it to a NOR gate (and, hence, to the dual NAND gate) and a Muller C gate. We analytically solve the resulting first-order differential equations with non-constant-coefficients, and derive analytic expressions for the resulting MIS gate delays. The resulting formulas not only pave the way to a sound model parameterization procedure, but are also instrumental for implementing fast and efficient digital timing simulation. By comparison with analog simulation data, we show that our models faithfully represent all relevant MIS effects. Using an implementation in the Involution Tool, we demonstrate that our model surpasses the alternative digital delay models for NOR gates known to us in terms of accuracy, with comparably short running times.

I. INTRODUCTION

Digital timing analysis techniques are essential for modern circuit design. Thanks to the elaborate static timing analysis techniques available today, which employ detailed models like CCSM [1] and ESCM [2] that facilitate a very accurate corner case analysis of the delays of the gates making up a digital circuit, essential circuit timing properties like worst-case critical path delays can nowadays be determined very accurately and very fast.

Still, asynchronous digital circuits may contain parts where corner-case delay estimates are not sufficient for understanding the overall behavior and for validating correct operation. We exemplify this by means of the token-passing ring described and analyzed by Winstead, Garviner and Greenstreet in [3]. Stages consisting of a 2-input Muller C gate, with its inputs connected to the previous resp. next stage, implement a self-timed ring oscillator. A detailed analysis revealed that it exhibits two different modes of operation, namely, burst behavior versus evenly spaced output transitions, with unpredictable mode switches between those. The actual operation mode depends on the subtle interplay between two effects that determine the delay of a Muller C gate: the 

drafting effect, a decrease of the delay happening when the resulting output transition is close to the previous output transition, and the Charlie effect, (named after Charles Molnar, who identified its causes in the 70th of the last century), an increase of the delay happening when the two inputs are switching in close proximity in the same direction. Clearly, to analyze the behavior of the ring, the timing relation of successive transitions need to be traced throughout the whole circuit. Since this is outside the scope of static timing analysis techniques, however, one has to resort to analog simulations e.g. via SPICE [4] here. Unfortunately, analog simulation times excessive, even for moderately large circuits. This is caused by fact that the dimension of the system of differential equations that need to be solved numerically increases with the number of transistors in a circuit.

Digital dynamic timing analysis techniques have been proposed as a less accurate but much faster alternative for correctness validation and accurate performance & power estimation [5] of such circuits, which can even be applied at early design stages. This techniques rests on fast and efficiently computable gate delay models, which provide gate delay estimations on a per-transition basis. Single-history delay models like [8], [9], which generalize the popular (equal input-to-output delay) and inertial delay (= constant delay + two short pulses being removed) models [10], have shown their potential for improving accuracy in dynamic timing analysis.

Particularly relevant for us is the involution delay model (IDM) proposed in [11], which consists of zero-time boolean gates interconnected by single-input single-output involution delay channels. By denoting the temporal distance of the current input transition to the previous output transition, i.e., the previous-output-to-input delay, as \( T \), IDM channels are characterized by a delay function \( \delta(T) \) that is a negative involution, in the sense that \( -\delta(-\delta(T)) = T \). Note that the dependence on \( T \) captures the drafting effect introduced in [3].

Unlike all other existing delay models known so far, the IDM faithfully models glitch propagation in the short-pulse filtration problem [11]: it has been proved to be consistent with physics, in the sense that a modeled circuit does not exhibit discontinuities at its output signals when a short pulse at some of its inputs is shrunk to 0 and hence vanishes. Moreover, it has been shown in [12] that one can add “delay noise” to the (obviously deterministic) delay function \( \delta(T) \) without sacrificing faithfulness. As demonstrated in some follow-up work [13], delay noise can even be used for incorporating substantial PVT variations and even aging.

The IDM is accompanied by a publicly available timing analysis framework (the Involution Tool [14]), which allows to compare the accuracy of different delay models. In particular, it allows to randomly generate input traces for a given circuit, and to evaluate the accuracy of IDM predictions compared to SPICE-generated transition times and to other digital delay models. An experimental evaluation of the modeling accuracy of the IDM in [14], using both measurements and simulations, has revealed very good results for inverter chains and clock trees, albeit less so for circuits containing also multi-input gates. Note that, in the case of the clock tree, a speedup of a factor of 250 has been obtained relative to SPICE in

\[ T \]
The authors argued that the degradation of accuracy in the case of multi-input gates is primarily due to the IDM’s inherent lack of properly covering output delay variations caused by multiple input switching (MIS) in close temporal proximity \[16\], i.e., Charlie effects: Compared to the single input switching (SIS) case, delays increase/decrease with decreasing transition separation time on different inputs. Clearly, single-input, single-output delay channels cannot exhibit such a behavior at all. This fuels the need for developing alternative digital delay models that can cope with MIS effects.

Related work: MIS effects have of course been addressed in the literature before, with approaches ranging from linear \[17\] or quadratic \[18\] fitting over higher-dimensional macromodels \[19\] and model representations \[20\] to recent machine learning methods \[21\]. However, the resulting models are either empirical or statistical and hence unsuitable as a basis for dynamic digital timing analysis; moreover, they cannot be proved to be faithful \[11\].

In \[22\], Ebergen, Fairbanks and Sutherland studied the performance of micropipelines, the control logic of which is made up of a chain of RendezVou\(z\) elements. Their analysis rests on a delay model for the RendezVou\(z\) elements, which relies on the Charlie effect exhibited by the constituent Muller \(C\) gate. Rather than providing a model that explains this MIS effect, however, they just considered it as given and used it for analyzing the token propagation performance in successive RendezVou\(z\) elements. The same is true for the already mentioned paper \[3\] by Winstanley, Garivier and Greenstreet.

To the best of our knowledge, the only attempt to develop a delay model that captures MIS effects and is suitable for dynamic timing analysis has been provided in \[23\], where the authors proposed a hybrid model of a 2-input CMOS \(NOR\) gate based on replacing transistors by ideal zero-time switches in the simple RC model shown in Fig. 1. We recall that a hybrid model describes a hybrid automaton \[24\] with several states called modes, in each of which the behavior of the system outputs is guided by some system of ordinary differential equations (ODEs). The automaton may switch instantaneously from one mode to another, according to some conditions on the current state of the system and/or the inputs. Since a \(NOR\) gate has two inputs, it can be described as a hybrid model with 4 modes, one for each possible digital state of the inputs \((A, B) \in \{(0,0), (0,1), (1,0), (1,1)\}\). Each mode is governed by a simple system of constant-coefficient first order ODEs, which are switched (continuously) upon an input state transition. Whereas this leads to an accurate delay model, which has recently even been proved to be also faithful \[25\], it fails to capture one of the MIS effects, namely, for a rising output transition.

Main contributions: (1) A detailed analysis of the shortcomings of \[23\] guided us to a refined approach for developing hybrid delay models for CMOS gates, where transistors are replaced by time-varying resistors. More specifically, rather than replacing transistors by zero-time switches as in \[23\], which would be inadequate for modeling MIS effects in circuits like Muller \(C\) gate implementations, we replace (some of) them by continuously rising resp. falling resistors according to the Shichman-Hodges transistor model \[26\]. We demonstrate the feasibility of this approach by appying it to both a CMOS \(NOR\) gate (which automatically also covers the “dual” \(NAND\) gate), and to a Muller \(C\) gate. Interestingly, it turned out that only the switching-on of the serial transistors needs to be continuous here (using the time evolution function \(R(t) \sim 1/t + R_{on}\); all other switchings are instantaneous.

(2) Rather than including the state of the continuously time-varying resistors in the resulting ODE systems (which would blow up the system dimension), we rely on first-order ODEs with time-varying coefficients instead. We analytically solved the ODEs for all modes, the complexity of which forced us to use some (close) approximations in certain cases, and composed the trajectory functions of different modes, like \((0,0) \to (0,1) \to (1,1)\), to determine analytic formulas for all MIS gate delays.

(3) We provide a procedure for parametrizing our delay model for a given implementation. Given certain MIS delay values, we used crucial insights gained from the analytic MIS gate delay formulas derived in (2) for guiding the process of empirically fitting the various model parameters to match these delay values. To validate our model, we apply it to a CMOS \(NOR\) gate both in a 15 nm technology and in a 65 nm technology, and to a Muller \(C\) gate in 15 nm technology. In all cases, it turned out that the delay predictions of our model match the real delays very well, in particular, also in those MIS case where \[23\] fails.

(4) We implemented our hybrid delay model in the Involution Tool \[14\], and experimentally compared the average accuracy and the simulation times of our model to other analog/digital simulations for one of the circuits studied in \[14\]. Note that the availability of analytic formulas for the trajectory functions and the gate delays eliminates the need for using a numerical solver in dynamic timing analysis, which is important for small simulation times. As expected, our model outperforms all alternative models known to us in terms of accuracy, without an undue performance penalty.

Paper organization: In Section \[III\] we briefly summarize the results of the analog simulations used for quantifying MIS delays for the 15 nm CMOS \(NOR\) gate in \[23\], which provide our baseline. Section \[III\] introduces our hybrid ODE model. In Section \[IV\] we analytically solve the resulting ODEs and derive gate delay expressions from these solutions. Section \[V\] provides our parametrization procedure, which is applied to both our 15 nm and some 65 nm CMOS \(NOR\) gate simulation data for model validation. Using this parametrization, we finally quantify the average modeling accuracy using the Involution Tool in Section \[VI\]. In Section \[VII\] we provide the hybrid delay model for a Muller \(C\) gate and some of the results of our validation experiments. Some conclusions are provided in Section \[VIII\].

II. MULTIPLE INPUT SWITCHING (MIS)

In this section, we provide a summary of the MIS effects in CMOS \(NOR\) gates reported in \[23\]. Let \(t_A\), \(t_B\), and \(t_O\) denote the points in time when the analog trajectories of input signals \(A, B,\) and the output signal \(O\) cross the discretization threshold voltage \(V_{th} = V_{DD}/2\), respectively. Varying \(t_A\) and \(t_B\) allows to study the gate delay \((t_O - t_A\) resp. \(t_O - t_B\), depending on the particular output state) over the relative input separation time \(\Delta = t_B - t_A\).
TABLE I: Integrals $I_1(t)$, $I_2(t)$, $I_3(t)$ and $U(t)$ for every possible mode switch; $\Delta = t_B - t_A$ and $2R = R_{pA} + R_{pB}$.

| Mode | $I_1(t) = \int_{t_0}^{t} \frac{1}{\beta_1 s + \beta_4 s + 2R} \, ds$ | $I_2(t) = \int_{t_0}^{t} \frac{1}{\beta_2 s + \beta_3 s + 2R} \, ds$ | $I_3(t) = \int_{t_0}^{t} \frac{1}{\beta_3 s + \beta_4 s + 2R} \, ds$ | $U(t) = \int_{t_0}^{t} \frac{1}{\beta_3 s + \beta_4 s + 2R} \, ds$ |
|------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|
| $T_1^1$ | $\frac{1}{\beta_1 s + \beta_4 s + 2R}$ | $\frac{1}{\beta_2 s + \beta_3 s + 2R}$ | $\frac{1}{\beta_3 s + \beta_4 s + 2R}$ | $\frac{1}{\beta_3 s + \beta_4 s + 2R}$ |
| $T_2^1$ | $\frac{1}{\beta_1 s + \beta_4 s + 2R}$ | $\frac{1}{\beta_2 s + \beta_3 s + 2R}$ | $\frac{1}{\beta_3 s + \beta_4 s + 2R}$ | $\frac{1}{\beta_3 s + \beta_4 s + 2R}$ |
| $T_3^1$ | $\frac{1}{\beta_1 s + \beta_4 s + 2R}$ | $\frac{1}{\beta_2 s + \beta_3 s + 2R}$ | $\frac{1}{\beta_3 s + \beta_4 s + 2R}$ | $\frac{1}{\beta_3 s + \beta_4 s + 2R}$ |
| $T_4^1$ | $\frac{1}{\beta_1 s + \beta_4 s + 2R}$ | $\frac{1}{\beta_2 s + \beta_3 s + 2R}$ | $\frac{1}{\beta_3 s + \beta_4 s + 2R}$ | $\frac{1}{\beta_3 s + \beta_4 s + 2R}$ |

In the case of a falling output transition, either the nMOS transistor $T_3$ or $T_4$ starts to conduct (is closed), while one of the two pMOS transistors in series stops conducting (is opened). Obviously, closing both $T_3$ and $T_4$ leads to an accelerated discharge of the capacitance $C$ and thus a (substantial) speed-up of the resulting ODE systems (4) while being reasonably close to the Shichman-Hodges transistor model [26], which states a quadratic dependence of the output current on the input voltage. Approximating this model with a suitable time evolution of the currents $I_{A,B}$, the shape of the output signal is essentially independent of $\Delta$; only the position in time varies. Since the gate only switches after both inputs have changed, the gate delay is $\delta_g(\Delta) = t_0 - \max(t_A, t_B)$. The resulting MIS effect is a (moderate) slow-down, i.e., the gate delay increases for $|\Delta| \to 0$, see Fig. 1B.

III. OUR HYBRID MODEL

In this section, we will introduce a model (see Fig. 2b), which replaces transistors by time-varying resistors: The values $R_i(t)$, $i = 1, \ldots, 4$ thereby vary between some fixed on-resistance $R_i$ and the off-resistance $\infty$. This results in a hybrid model with 4 different modes, corresponding to the 4 possible input states $(A, B) \in \{(0, 0), (0, 1), (1, 0), (1, 1)\}$. Crucial for our model is choosing a suitable time variation of the on-resistance $R_i(t)$ in the on- and off-mode, which should facilitate an analytic solution of the resulting ODE systems (4) while being reasonably close to the physical behavior of a transistor. We rely on the very simple Shichman-Hodges transistor model [26], which states a quadratic dependence of the output current on the input voltage. Approximating the latter by $dV/dt \approx V_{out}$, with $d$ and $t_0$ some fitting parameters, leads to the continuous resistive model

$$R_{on}^i(t) = \frac{\alpha_i}{t - t_{on}} + R_i; \, t \geq t_{on},$$

$$R_{off}^i(t) = \beta_i(t - t_{off}) + R_i; \, t \geq t_{off},$$

for some constant slope parameters $\alpha_i [1/\Omega]$, $\beta_i [1/\tau]$, and on-resistance $R_i [\Omega]$. $t_{on}$ resp. $t_{off}$ represent the time when the respective transistor is switched on resp. off.

A. Model development

The arguably most natural idea for developing such a model for the NOR gate would be to maintain $R_{1}(t), \ldots, R_{4}(t)$ explicitly in the state of every ODE system, and switch between those continuously upon a mode switch. However, to begin with, such a “full-state model” would comprise ODE systems with a 5-dimensional state (output voltage $V_{out}$ and the 4 resistors) and thus render finding an analytic solution hopeless.

We therefore use a different approach, namely, incorporating these resistors only in the coefficients of a simple first-order ODE, which hence become non-constant. Moreover, we employ continuously changing resistors (according to (1)) only for switching-on the pMOS transistors. Everything else will be identical to the ideal switch model (which is obtained by setting $\alpha_i = 0$ and $\beta_i = \infty$) already employed in [23]. We will argue in Section III-B what guided us to arrive at this model.

Applying Kirchhoff’s rules to Fig. 2b leads to $C \frac{dV_{out}}{dt} = V_{DD} - V_{out} - R_{1B}(t) R_{2}(t)$, which can be transformed to the non-homogeneous ordinary differential equation (ODE) with non-constant coefficients

$$\frac{dV_{out}}{dt} + \frac{V_{out}}{CR_{B}(t)} = U(t),$$

using $R_{1B}(t) = \frac{1}{R_{1}(t) + R_{2}(t)}$. Note that the entire voltage divider in Fig. 2b is equivalent to an ideal voltage source $V_0 = V_{DD} R_{1B}(t) R_{2}(t)$ and a serial resistor $R_{B}(t)$ sourcing $C$. Consequently, $C(t) = U_0 R_{B}(t)$ in (3) is the short-circuit current, and $U(t) = V_{out}/R_{B}(t)$ the current actually sourced into $C$. It is well-known that the general solution of (3) is

$$V_{out}(t) = V_0 e^{-G(t)} + \int_0^t U(s) e^{G(t) - G(s)} ds,$$

where $V_0 = V_{out}(0)$ denotes the initial condition and $G(t) = \int_0^t (1/C R_{B}(s))^{-1} ds$.

For simplicity, we will subsequently use the notation $R_1 = R_{pA}$, $R_2 = R_{pB}$ with the abbreviation $2R = R_{pA} + R_{pB}$ for the two

![Fig. 2: Schematics and resistor model of a CMOS NOR gate.](image-url)
TABLE II: State transitions and modes. ⊤ and ⊥ (resp. ↓ and ↑) represent the first and the second rising (resp. falling) input transitions. + and − specify the sign of the switching time Δ = t_B − t_A.

| Mode | Transition | t_A | t_B | R_1 | R_2 | R_3 | R_4 |
|------|------------|-----|-----|-----|-----|-----|-----|
| T_{+}^{1} | (0, 0) → (1, 1) | −∞ | −∞ | off | off | on | off |
| T_{-}^{1} | (0, 0) → (1, 1) | −∞ | −∞ | on | off | off | on |
| T_{+}^{2} | (1, 1) → (0, 1) | −∞ | −∞ | off | on | off | on |
| T_{-}^{2} | (1, 1) → (0, 1) | −∞ | −∞ | on | off | on | off |
| T_{+}^{3} | (0, 0) → (1, 0) | −Δ | −Δ | off | aff | on | on |
| T_{-}^{3} | (0, 0) → (1, 0) | −Δ | −Δ | on | aff | off | off |

pMOS transistors T_1 and T_2, and R_3 = R_{A_B}, R_4 = R_{A_B} for the two nMOS transistors T_3 and T_4.

Table II shows all possible state transitions and the corresponding resistor time evolution mode switches. Double arrows in the mode switch names indicate MIS-relevant modes, whereas + and − indicate whether A switched before B or the other way around. For instance, assume the system is in state (0, 0) for quite some time in the past, i.e., A and B switched to 0 at time t_A = t_B = −∞. This causes R_1 and R_2 to be in the on-mode, whereas R_3 and R_4 are in the off-mode. Now assume that, at time t_A = 0, A is switched to 1. This switches R_1 resp. R_3 to the off-mode resp. on-mode at time t_{off} = t_{on} = t_A = 0. The corresponding mode switch is T_{+}^{1} and reaches state (1, 0). Now assume that B is also switched to 1, at some time t_B = Δ > 0. This causes R_2 resp. R_4 to switch to off-mode resp. on-mode at time t_{off} = t_{on} = t_B = Δ. The corresponding mode switch is T_{+}^{1} and reaches state (1, 1); note carefully that the delay is Δ-dependent and hence MIS-relevant.

In Section IV, we will determine analytic formulas for the output voltage trajectories V_{out}(t) given by (4) for every mode switch MS listed in Table II. Note that, due to the particular modes of the resistors in each transition, different expressions for G(t) and U(t) according to Table II will be obtained for every mode switch.

B. Relation to other models

We mentioned already that a 5-dimensional “full-state model” would not allow computing analytic formulas for the trajectories. This is not only disadvantageous for accuracy validation experiments like the ones presented in Section VII, as they must resort to a numerical ODE server, but it also provides no guidance whatsoever for the complex process of model parametrization. Indeed, in Section VII, the availability of analytic expressions of the (inverse) trajectories proved instrumental in developing a successful model parametrization process.

Since we conjectured initially that a full-state model should surpass our model proposed in Section III-A in terms of modeling accuracy, however, we nevertheless tried hard to find a suitable parametrization of the FM for the CMOS NOR gate delays given in Fig. 1a and Fig. 1b. Whereas we succeeded to faithfully model the former, we failed to find a parametrization that also covers the latter. Given the large parameter space, we initially blamed our unguided search for the parameters for this failure.

However, as a consequence of another unsuccessful modeling attempt, we eventually diagnosed a deeper reason for this failure. In more detail, as a precursor of our model, we considered a version of the model in Section III-A where both the switching-on and switching-off resistance of all transistors was continuous, according to (1) and (2). However, besides considerably complicating the analysis, it eventually turned out that this model suffers from the same problem as the full-state model: We could not find a parametrization that faithfully covers both Fig. 1a and Fig. 1b.

Thanks to the analytic formulas developed for this precursor model, however, we eventually realized that the parametrization failures are actually a consequence of using the simple resistor model (1) and (2) in operation regions of a transistor where they do not apply. More specifically, consider a rising output transition, i.e., switching-on the serial pMOS transistors and simultaneously switching-off the parallel nMOS transistors in Fig. 2b. Since (1) is a convex function, i.e., eventually decreases sub-linearly, whereas (2) increases linearly, too much of the current provided by the (slowly opening) pMOS transistors is consumed by the (still conducting) nMOS transistors. Consequently, C cannot be charged as fast as it should be, no matter how large β_A, β_B < ∞ is chosen. Only the immediate switch of the nMOS transistors, i.e., choosing β_A = β_B = ∞, allows to circumvent this problem in our setting.

We note that the issue explained above also arises in the case of falling output transitions, albeit less pronounced: The current supplied by the (still conducting but serial) switched-off pMOS transistors can be reasonably swallowed by the (slowly opening but parallel) nMOS transistors. Nevertheless, we witnessed a trace of this problem, by achieving a lower parametrization and modeling accuracy of the precursor model also for this case.

One other distinguishing feature of our model is its simplicity, besides the need to solve a non-constant coefficient ODE. In particular, whereas the ideal switch model of [23] also incorporates the voltage at the node between the two pMOS transistors (due to the parasitic capacitance C_p), our model has only one state variable, namely, V_{out} (due to the load capacitance C). We initially suspected that ignoring C_{int} in our model could impair its ability to capture some MIS effects, in particular, in the cases of falling input transitions T_{−}^{1} and T_{−}^{3} (recall Section II) where the charge stored in C_{int} does affect the gate delay. Our results in Section VII reveal, however, that this is not the case.

In addition, we tried to keep the number of transistors that actually employ a continuously varying resistance in our model as small as possible: Only the two pMOS transistors T_1 and T_2 in Fig. 2b use (1), all other resistance switches happen instantaneously.

We conclude this section by stressing again that the general approach of replacing (some) transistors with varying resistors advocated in this paper can be readily applied, and sometimes just transferred, to other gates as well. This is particularly true for the CMOS NAND gate, which is obtained from the NOR gate in Fig. 2b by replacing nMOS transistors with pMOS and vice versa, and swapping V_{DD} and GND. Of course, now the nMOS transistors are the serial ones (where the continuous resistance models must be used). All that is needed to make the results of our analysis matching is to invert A_M and B_M in operation regions of a transistor where they do not apply. More specifically, consider a rising output transition, i.e., switching-on the serial pMOS transistors and simultaneously switching-off the parallel nMOS transistors in Fig. 2b. Since (1) is a convex function, i.e., eventually decreases sub-linearly, whereas (2) increases linearly, too much of the current provided by the (slowly opening) pMOS transistors is consumed by the (still conducting) nMOS transistors. Consequently, C cannot be charged as fast as it should be, no matter how large β_A, β_B < ∞ is chosen. Only the immediate switch of the nMOS transistors, i.e., choosing β_A = β_B = ∞, allows to circumvent this problem in our setting.

In order to verify that the ODE model introduced in Section III faithfully covers all the MIS effects described in Section II, we first derive analytic expressions for the trajectories of V_{MS}^{out}(t) for every mode switch MS listed in Table II. Then, we determine the MIS delays for an arbitrary input separation time Δ = t_B − t_A as follows:

2We conjecture that the problem would also disappear if we replaced (1) by a steeper decaying function. However, we do not currently know of a suitable candidate that would render solving our non-constant coefficient ODE possible.
• Compute $V_{out}^{+}(\Delta)$, and use it as the initial value for obtaining $V_{out}^{+}(t)$; the sought gate delay is the time until the latter crosses the threshold voltage $V_{DD}/2$.

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Fortunately, a closer look at Table I and Table II shows a symmetry between the pairs of modes $(T_+^3, T_+^3)$, $(T_+^3, T_+^3)$, $(T_+^3, T_+^3)$, and $(T_+^3, T_+^3)$. Therefore, it is sufficient to derive analytic expressions for the case $\Delta \geq 0$ only, i.e., to consider the pairs of modes $(T_+^3, T_+^3)$ resp. $(T_+^3, T_+^3)$ listed above. The corresponding formulas for $\Delta < 0$ can be obtained from those by exchanging $\alpha_1$ and $\alpha_2$ as well as $R_{nA}$ and $R_{nB}$, respectively.

A. Rising input transitions

In order to compute $V_{out}^{+}(t)$, consider the corresponding integrals $I_1(t)$, $I_2(t)$, and $I_3(t)$, as well as $U(t)$ in Table II. Since $\beta_1 = \beta_2 = \infty$ and $\alpha_3 = \alpha_4 = 0$, we obtain

$$I_1(t) = I_3(t) = U(t) = 0, \quad I_2(t) = \frac{t}{R_{nA}}.$$

Since $G(t) = (I_1(t) + I_2(t) + I_3(t))/C$, we get $e^{G(t)} = e^{G(t)_{\Delta}}$ and $\int_0^{\Delta} e^{G(t)} U(t) dt = 0$. With $V_0 = V_{out}(0)$ as our initial value, (4) finally provides

$$V_{out}^{+}(t) = V_{out}^{+}(0)e^{\frac{t}{R_{nA}}}.$$

Similarly, for the mode $T_+^3$, we obtain

$$I_1(t) = U(t) = 0, \quad I_2(t) = \frac{t}{R_{nA}}, \quad I_3(t) = \frac{t}{R_{nB}},$$

such that $e^{G(t)} = e^{G} e^{-\frac{t}{R_{nA}}}$. and $\int_0^{\Delta} e^{G(t)} U(t) dt = 0$.

Consequently, we obtain

$$V_{out}^{+}(t) = V_{out}^{+}(0)e^{-\frac{t}{R_{nA}}},$$

where $V_{out}(\Delta)$ can be computed via (5).

Due to the symmetry mentioned before, we can immediately conclude the following result for negative $\Delta$:

$$V_{out}^{+}(t) = V_{out}^{+}(0)e^{-\frac{t}{R_{nA}}}.$$

B. Falling input transitions

In this case, we first need to compute $V_{out}^{+}(t)$. Again plugging $\beta_1 = \beta_2 = \infty$ and $\alpha_3 = \alpha_4 = 0$ in the corresponding expressions in Table II provides

$$I_1(t) = I_3(t) = U(t) = 0, \quad I_2(t) = \frac{t}{R_{nB}}.$$

With $V_0 = V_{out}(0)$ as our initial condition, (4) yields

$$V_{out}^{+}(t) = V_{out}^{+}(0)e^{-\frac{t}{R_{nB}}}.$$

Now, turning our attention to $V_{out}^{+}(t)$ confronts us with a more intricate case: Whereas $I_2(t) = I_3(t) = 0$ again, evaluating $I_1(t)$ requires us to study the function

$$f(s) = \frac{1}{\frac{\alpha_1}{s} + \frac{\alpha_2}{s} + 2R},$$

as

$$I_1(t) = \int_0^t f(s) ds, \quad G(t) = I_1(t)/C, \quad \int_0^t e^{G(t)} U(s) ds = \frac{V_{DD}}{C} \int_0^t e^{\frac{t}{c}} f(s) ds.$$

Computing the above integrals is complicated by the fact that $f(s)$ also involves the parameter $\Delta$, which prohibits uniform closed-form solutions of (10) and (11). We hence need accurate approximations for $f(s)$, which will be different for different ranges of $s$ and $\Delta$, which will in turn depend on the unknown parameters $\alpha_1$, $\alpha_2$ and $R$. Fortunately, a closer look at the function $f(t)$ reveals that piecewise approximations can be built on the basis of (1) distinguishing different ranges (cases) for $\Delta$ with the parameters $\alpha_1$, $\alpha_2$ and $R$, and (2) splitting the integration interval $[0, t]$ into certain subintervals, which may depend on the particular case. Note that this splitting typically also involves an additional free parameter $\epsilon = \eta \Delta$ (for some $\eta \in \mathbb{R}$), which takes care of values of $s$ close to $\Delta$. More specifically, we came up with the following four cases and the corresponding approximations for $f(s)$ in the appropriate subintervals:

• Case 1: $(0 \leq \Delta < \frac{\alpha_1}{2R})$

$$f(s) \approx \begin{cases} \frac{s}{\alpha_1} & 0 \leq s < \frac{\alpha_1}{2R} \\ \frac{s}{\alpha_1 + \epsilon} & \frac{\alpha_1}{2R} \leq s < \frac{\alpha_1 + \epsilon}{2R} \\ \frac{s}{\alpha_1 + \epsilon} & \frac{\alpha_1 + \epsilon}{2R} \leq s \leq t \end{cases}$$

• Case 2: $(\frac{\alpha_1}{2R} \leq \Delta < \frac{\alpha_1 + \alpha_2}{4R})$

$$f(s) \approx \begin{cases} \frac{s}{\alpha_1} & 0 \leq s < \frac{\alpha_1}{2R} \\ \frac{s}{\alpha_1 + \epsilon} & \frac{\alpha_1}{2R} \leq s < \frac{\alpha_1 + \epsilon}{2R} \\ \frac{s}{\alpha_1 + \epsilon} & \frac{\alpha_1 + \epsilon}{2R} \leq s \leq t \end{cases}$$

• Case 3: $(\frac{\alpha_1 + \alpha_2}{4R} \leq \Delta < \frac{\alpha_1 + \alpha_2}{2R})$

$$f(s) \approx \begin{cases} \frac{s}{\alpha_1} & 0 \leq s < \frac{\alpha_1}{2R} \\ \frac{s}{\alpha_1 + \epsilon} & \frac{\alpha_1}{2R} \leq s < \frac{\alpha_1 + \epsilon}{2R} \\ \frac{s}{\alpha_1 + \epsilon} & \frac{\alpha_1 + \epsilon}{2R} \leq s \leq t \end{cases}$$

• Case 4: $(\frac{\alpha_1 + \alpha_2}{2R} \leq \Delta < t)$

$$f(s) \approx \begin{cases} \frac{s}{\alpha_1} & 0 \leq s < \frac{\alpha_1}{2R} \\ \frac{s}{\alpha_1} & \frac{\alpha_1}{2R} \leq s \leq t \end{cases}$$

To explain how to determine these approximations, we elaborate on how this is done for Case 1; similar arguments can be used to justify the remaining cases 2–4. (i) For the range $0 \leq s < \Delta - \epsilon$, which expresses the situation where the integration variable $s$ is fairly smaller than $\Delta$, we observe $s + \Delta \approx \Delta$, and therefore, $\frac{s}{\Delta} + \frac{1}{\Delta} \approx \frac{s}{\Delta}$. Assuming that the slope parameters $\alpha_1$ and $\alpha_2$ are approximately the same, this leads us to $\frac{s}{\alpha_1} + \frac{s}{\alpha_2} \approx \frac{s}{\alpha_1}$. Furthermore, since $s < \Delta < \frac{\alpha_1}{2R}$ here, we get $\frac{s}{\alpha_1} + 2R \approx \frac{s}{\alpha_1}$ and hence $f(s) \approx \frac{s}{\alpha_1}$ as asserted. (ii) For the range $\Delta - \epsilon \leq s < \Delta + \epsilon$, where $s$ is relatively close to $\Delta$, we can substitute $s$ by $\Delta$, which leads to $\frac{s}{\alpha_1} + \frac{s}{\alpha_2} \approx \frac{s}{\alpha_1}$. Besides, since $s \approx \Delta < \frac{\alpha_1 + \alpha_2}{2R} < \frac{\alpha_1 + \alpha_2}{2R}$, we get $\frac{\alpha_1 + \alpha_2}{2R} + 2R \approx \frac{\alpha_1 + \alpha_2}{2R}$, which justifies the asserted approximation for $f(s)$. (iii) Turning our attention to the range $\Delta + \epsilon \leq s < \frac{\alpha_1 + \alpha_2}{2R}$, we obtain $\frac{s}{\alpha_1} \approx \frac{s}{\alpha_1}$ and hence $f(s) \approx \frac{s}{\alpha_1}$. Since $s < \frac{\alpha_1 + \alpha_2}{2R}$, this leads to...
\[
\begin{align*}
\text{Case } k \in \{1, 2, 3, 4\}, \quad &i_1 = \frac{(\Delta - \epsilon)^2}{2a_2} - \frac{(\Delta + \epsilon)^2}{2(a_1 + a_2)} + \frac{4a_1}{a_1 + a_2} - \frac{\alpha_1 + a_2}{8R^2}, \\
&i_2 = \frac{4R(\Delta - \epsilon) - (a_1 + a_2)}{8R^2} - \frac{2(\Delta + \epsilon)^2}{a_1 + a_2} + \frac{4\Delta}{a_1 + a_2}, \\
&i_3 = \frac{4R(\Delta + \epsilon) - (a_1 + a_2)}{8R^2} - \frac{2(\Delta + \epsilon)^2}{a_1 + a_2}, \\
&i_4 = -\frac{\alpha_2}{8R^2}.
\end{align*}
\]

which do not depend on \( t \).

Furthermore, \(\int_0^t e^{C(s)} U(s) ds \approx \frac{V_{DD}}{C} \).

For Case \( k \in \{1, 2, 3, 4\}, \):

\[
\begin{align*}
\gamma_1 &= 4R^2C e^{\frac{a_1 + a_2}{A}} \left(1 - \frac{2R(\Delta - \epsilon) - 4R^2C}{\alpha_1 + a_2} e^{\frac{\Delta}{\alpha_1 + a_2}} \right), \\
&\quad + \frac{4R^2C}{\alpha_2} \left(e^{\frac{\Delta}{a_2}} - 1\right), \\
\gamma_2 &= 4R^2C \left(1 - \frac{4R(\Delta - \epsilon) - 8R^2C}{\alpha_1 + a_2} e^{\frac{\Delta}{\alpha_1 + a_2}} \right), \\
&\quad - \frac{4R(\Delta + \epsilon) - 8R^2C}{\alpha_1 + a_2} e^{\frac{\Delta}{\alpha_1 + a_2}}, \\
\gamma_3 &= 4R^2C \left(1 - \frac{4R(\Delta - \epsilon) - 8R^2C}{\alpha_1 + a_2} e^{\frac{\Delta}{\alpha_1 + a_2}} \right), \\
&\quad - \frac{4R(\Delta + \epsilon) - 8R^2C}{\alpha_1 + a_2} e^{\frac{\Delta}{\alpha_1 + a_2}}, \\
\gamma_4 &= 4R^2C \left(1 - \frac{4R(\Delta - \epsilon) - 8R^2C}{\alpha_1 + a_2} e^{\frac{\Delta}{\alpha_1 + a_2}} \right), \\
&\quad - \frac{4R(\Delta + \epsilon) - 8R^2C}{\alpha_1 + a_2} e^{\frac{\Delta}{\alpha_1 + a_2}}.
\end{align*}
\]

Combining the above solutions for (10) and (11) according to (4) provides an accurate expression for the output trajectory \( V_{out}^{T+} (t) \):

\[
V_{out}^{T+} (t) \approx V_{out}^{T+} (\Delta e^{\frac{-2(\epsilon + R_s)}{RC}} + V_{DD}(1 - \gamma_k e^{\frac{-t}{RC}})
\]

for Case \( k \in \{1, 2, 3, 4\}, \) where \( V_{out}^{T+} (\Delta) = \frac{V_{out}^{T+} (0)}{e^{\frac{\Delta}{RC}}}, \) \( i_1, \ldots, i_4, \gamma_1, \ldots, \gamma_4, \) are defined in [9], [12], ..., [19], respectively.

C. Single Input Switching

Whereas the main focus of our model is the proper modeling of MIS effects, it of course also needs to handle the “simple” single input switching case. This is done exactly as in the IDM [9], by continuously switching between the trajectories of the modes \((0, 0)\) and \((1, 0)\) (for input A) resp. \((0, 0)\) and \((0, 1)\) (for input B).

Fortunately, we can adapt the above trajectory formulas for the MIS cases to also obtain the ones for the SIS cases. In fact, in the SIS cases, \(\Delta\) just represents the time difference between the current and the previous transition of the same input. For switching from \((1, 0)\) and \((0, 0)\), for example, it suffices to replace the initial value \( V_{out}^{T+} (\Delta) \).

Case 2

In \( V_{out}^{T+} (t) \) by the initial value \( V_{out}^{T+} (\Delta) \), which gives the output voltage at the time the previous switch from \((0, 0)\) to \((1, 0)\).

V. PARAMETERIZATION AND MODELING MIS EFFECTS

Case 3

Since the ultimate goal of our hybrid model is to develop a basis for dynamic digital timing simulations, our main target is the derivation of explicit analytic formulas for the input-to-output delay functions \(\delta^\downarrow_M (\Delta)\) and \(\delta^\uparrow_M (\Delta)\) for both rising and falling output transitions. Moreover, we have to answer the question how to determine the parameters \(\alpha_1, \alpha_2, C, R, R_{nA}, R_{nB}\), and \(\eta\) for a given technology. Such a parameterization is of course necessary for checking whether and how well our new model is capable of faithfully reproducing the MIS effects described in Section [11].

To accomplish the first task, by inverting the explicit formulas obtained for the trajectories \( V_{out}^{T+} (t) \) and \( V_{out}^{T+} (t) \) resp. for \( V_{out}^{T+} (t) \) and \( V_{out}^{T+} (t) \) obtained in the previous section, we obtain the exact resp. approximate analytic expressions for \(\delta^\downarrow_M, (\Delta) \) (for \(\Delta \geq 0)\), \(\delta^\downarrow_M, (\Delta) \) (for \(\Delta < 0)\) and \(\delta^\uparrow_M, (\Delta) \) (for \(\Delta \geq 0)\), \(\delta^\downarrow_M, (\Delta) \) (for \(\Delta < 0)\) in terms of the model’s parameters 

Theorem 1 (MIS Delay Functions).

For any \( 0 < \Delta \leq \infty\), the MIS delay functions for falling and rising output transitions of our model are given by:

\[
\delta^\downarrow_M, (\Delta) = \left\{ \begin{array}{l l}
\frac{\ln(2) \cdot RC_{nA} \cdot R_{nB} + \Delta R_{nB}}{R_{nA} + R_{nB}} + \Delta & \text{if } 0 \leq \Delta \leq \ln(2) \cdot RC_{nA} \\
\ln(2) & \text{if } \Delta > \ln(2) \cdot RC_{nA}
\end{array} \right.
\]
\[ \delta_{M_-}^k(\Delta) = \begin{cases} \frac{\ln(2)CR_{n_A}R_{n_B}}{R_{n_A} + R_{n_B}} + |\Delta| & |\Delta| < \ln(2)CR_{n_B} \\ \frac{\ln(2)C}{R_{n_B}} & |\Delta| \ge \ln(2)CR_{n_B} \end{cases} \]

and, for Case \( k \in \{1, 2, 3, 4\} \),

\[ \delta_{M_+}^k(\Delta) \approx 2RC\left(\ln(\gamma_\ell) + \ln(2)\right), \]

\[ \delta_{M_-}^k(\Delta) \approx 2RC\left(\ln(\gamma_0) + \ln(2)\right). \]

\( \delta_{M_-}^k(\Delta) \) and \( \delta_{M_-}^k(\Delta) \) can be easily obtained by our symmetry.

**Proof.** We sketch how \( \delta_{M_+}^k(\Delta) \) is computed; the expression for \( \delta_{M_-}^k(\Delta) \) is obtained analogously. Recall that falling output transitions imply rising input transitions and vice versa. Given the trajectory \( V_{out}^{T_1} (t) \) in \( \delta \), we start out from \( V_{out}(0) = V_{DD} \) and need to compute the time \( \delta_{M_+}^k(\Delta) \) when either (i) the already preceding trajectory \( V_{out}^{T_2} (t) \) or else (ii) \( V_{out}^{T_1} (t) \) itself (which is started at time \( \Delta \)) hits \( V_{DD}/2 \). Note that this reflects the fact that already the first rising input (at time \( 0 \)) causes the output to switch to \( 0 \). Since all these trajectories only involve a single exponential, they are easy to invert.

It turns out that case (i) occurs for values \( \Delta \ge -\ln(0.5)CR_{n_A} \), case (ii) for smaller \( \Delta \).

Similarly, for computing \( \delta_{M_-}^k(\Delta) \), we need to consider the trajectory \( V_{out}^{T_2} (t) \). Here, we have to start out from the initial value \( V_{out}(0) = 0 \) and just need to compute the time \( \delta_{M_-}^k(\Delta) \) until \( V_{out}^{T_2} (t) \) hits \( V_{DD}/2 \). This reflects the fact that it is only the second falling input (at time \( 0 \)) that causes the output to switch to \( 1 \).

Whereas the specific initial values \( V_{out}^{T_1}(0) = V_{DD} \) and \( V_{out}(0) = 0 \) used in Theorem \( 2 \) are sufficient for evaluating the MIS behavior of our model, we need generalized expressions for the dynamic digital timing simulation experiments in Section \( VI \). In Theorem \( 2 \) we therefore provide the delay functions for arbitrary initial values.

**Theorem 2** (MIS and SIS delay functions for arbitrary initial values). For any \( 0 \leq \Delta \leq \infty \), the extended delay functions for falling and rising output transitions of our model, when starting from a given initial value \( V_{out}(0) \), are

\[ \delta_{EM,+}^k(\Delta) = \begin{cases} -\frac{\ell CR_{n_A}R_{n_B} + \Delta R_{n_B}}{R_{n_A} + R_{n_B}} + \Delta & 0 \leq \Delta < -\ell CR_{n_A} \\ -\ell CR_{n_A} & \Delta \geq -\ell CR_{n_A} \end{cases} \]

\[ \delta_{EM,-}^k(\Delta) \approx 2RC\left(\ln\left(\frac{V_{DD}V_{out}(0)e^{-\frac{\Delta}{\ell CR_{n_B}}} - V_{DD}}{V_{DD}}\right)\right). \]

where \( \ell = \ln(V_{DD}/2V_{out}(0)) \) and Case \( k \in \{1, 2, 3, 4\} \). \( \delta_{EM,+}^k(\Delta) \) and \( \delta_{EM,-}^k(\Delta) \) can be easily obtained by our symmetry.

The delay functions given in Theorem \( 2 \) that is, in Theorem \( 2 \) not only facilitate fast dynamic timing analysis, but are also instrumental for understanding which parameters affect the which delay value. In fact, the formulas could even be used for explicit parametrization of a given circuit when certain delay values are known.

**A. Parameterization for 15 nm**

In this subsection, we will fit our model to the characteristic MIS delay values \( \delta_{M_+}^k(\infty) \), \( \delta_{M_+}^k(0) \), \( \delta_{M_+}^k(\infty) \) according to Fig. \( 1a \) and the corresponding values \( \delta_{M_-}^k(\infty) \), \( \delta_{M_-}^k(0) \), \( \delta_{M_-}^k(\infty) \) in Fig. \( 1b \) of the CMOS NOR gate implementation described in \( 23 \).

Interestingly, our first attempt to simultaneously fit all six delay values for determining all parameters at once turned out to be naive since impossible. To understand why this is the case, note that the on-resistors of the two nMOS transistors \( R_{n_A} \) and \( R_{n_B} \) should roughly be the same. Consequently, we obtain

\[ \frac{\delta_{M_+}^k(\infty)}{\delta_{M_+}^k(0)} = \frac{R_{n_A} + R_{n_B}}{R_{n_B}} \approx 2. \]

Unfortunately, however, the desired ratio is \( \frac{\delta_{M_+}^k(\infty)}{\delta_{M_+}^k(0)} \approx \frac{14 \text{ ps}}{27 \text{ ps}} \), which cannot fit these two values with reasonable choices for \( R_{n_A} \) and \( R_{n_B} \).

As in \( 23 \), we fixed this problem by adding (that is, subtracting) a suitably chosen pure delay \( \delta_{min} = 18 \text{ ps} \) (foreseen in the original IDM \( 9 \)), which just defers the switching to the new state upon an input transition. This results in an effective ratio of \( 20 \text{ ps} \approx 2 \), which could finally be matched by least squares fitting. Of course, when using our model in digital timing analysis, \( \delta_{min} \) must be added to the computed delay values.

More specifically, starting out from the desired load capacitance \( C \), we first determined \( R_{n_A} \) and \( R_{n_B} \) by fitting \( \delta_{M_-}^k(\infty) \) (or \( \delta_{M_+}^k(\infty) \)) and \( \delta_{M_+}^k(0) \) to match \( \delta_{M_-}^k(\infty) - \delta_{min} \) (or \( \delta_{M_+}^k(\infty) - \delta_{min} \)) and \( \delta_{M_+}^k(0) - \delta_{min} \). Once these parameter values had been obtained, we fixed those and determined the remaining parameters \( R, \alpha_1, \alpha_2 \) and \( \eta \) by fitting \( \delta_{M_+}^k(\infty) \), \( \delta_{M_+}^k(0) \) and \( \delta_{M_-}^k(\infty) \) to match \( \delta_{M_+}^k(\infty) - \delta_{min}, \delta_{M_+}^k(0) - \delta_{min} \) and \( \delta_{M_-}^k(\infty) - \delta_{min} \). Note that the same \( \delta_{min} = 18 \text{ ps} \) is used for both rising and falling output transitions.

The result of our parametrization for the circuit in Section \( II \) is shown in Table \( III \).

**TABLE III:** Model parameter values for the 15 nm CMOS NOR gate used for producing Fig. \( 13 \) and Fig. \( 14 \).

| Parameter | Value |
|-----------|-------|
| \( R_{n_A} \) | 8.30562 + 0.0208 \Omega |
| \( R_{n_B} \) | 8.25562 - 0.0208 \Omega |
| \( C \) | 3.61355/94434278 \text{ fF} |

Utilizing the parameters in Table \( III \) we can finally visualize the delay predictions of our model. Fig. \( 3 \) shows the very good fit for both rising and falling output transitions. We therefore conclude that our new hybrid model fully captures all the MIS effects introduced in Section \( III \) including the case of \( \Delta = 0 \) for rising output transitions where the model proposed in \( 23 \) fails.

As a final remark, we note that some of the modeling inaccuracies visible in Fig. \( 3 \) are caused by the approximation errors introduced by our solutions of \( 10 \) and \( 11 \). One is the lack of perfectly fitting the actual delay with the computed one for \( \Delta = 0 \), which looks quite bad in the figure but actually causes a relative error of about 0.95 % only. Other instances are the small dent shapes around \( 0 \) visible in Fig. \( 3b \).
of the range in Case 3. It could easily be circumvented by slightly moving the border between Case 3 and Case 4 to a smaller value, i.e., to $\frac{\alpha_3 - \alpha_2}{2R} - \epsilon$ for some $\epsilon > 0$. Since the induced error is marginal, however, we did not bother with further complicating our analysis. B. Other parameterizations

A crucial feature of any model is wide applicability. Ideally, our hybrid delay model should be applicable to any CMOS technology, for any supply voltage, temperature, age etc., in the sense that it is possible to determine a parametrization that allows our model to match the MIS delays of any given CMOS implementation. Overall, it is reasonable to conjecture that our model is applicable whenever the Shichman-Hodges transistor model \cite{26}, i.e., \ref{eq:shichman_hodges} and \ref{eq:ideal_switch}, reasonably applies. Whereas it is of course impossible for us to prove such a claim, we can demonstrate that this is the case for some quite different technology and operation conditions, namely the UMC 65 nm technology with $V_{DD} = 1.2$ V supply voltage and a larger load capacitance $C$. The red dashed curves in Fig. 4a (falling output) resp. Fig. 4b (rising output), which correspond to Fig. 3a resp. Fig. 3b, show the gate delays depending on the input separation time $\Delta$ obtained via SPICE simulations.

Parametrizing our model for these 65 nm MIS delays turned out to be remarkable easy: Exactly as for our 15 nm technology, by initially fixing some value for the load capacitance $C$ and trying to match $\delta_{M}^{\uparrow}(\infty)$ (or $\delta_{S}^{\uparrow}(\infty)$) and $\delta_{M}^{\downarrow}(0)$ with $\delta_{S}^{\downarrow}(\infty) - \delta_{\min}$ (or $\delta_{S}^{\downarrow}(\infty) - \delta_{\min}$ and $\delta_{S}^{\downarrow}(0) - \delta_{\min}$, we determined accurate values for $R_{M}$ and $R_{N}$. After fixing the latter, we obtained the values of the remaining parameters by fitting the remaining delay values. Note carefully, however, that we had to use a different pure delay $\delta_{\min} = 10.8$ ps here, since $\frac{\delta_{S}^{\downarrow}(\infty)}{\delta_{S}^{\downarrow}(0)} \approx 2.22$. Table IV provides the resulting list of parameters. Not surprisingly, since the gate delay is considerably higher than for our 15 nm data, we indeed face a significantly larger value for the load capacitance $C$ also in our model.

**TABLE IV:** Model parameter values for the 65 nm CMOS NOR gate used for producing the red curves in Fig. 4.

| $R_{M}$ | $R_{N}$ | $C$ | $V_{DD}$ |
|--------|--------|-----|---------|
| 8.4085628882200 MΩ | 2.0654286282200 MΩ | 30.6315904443276 fF | VDD = 0.8 V |

Utilizing the parameters in Table IV we finally obtained the blue curves in Fig. 4a and Fig. 4b which illustrate the computed delays of our model for the 65 nm technology. It is apparent that they match the real delays very well: We see an ideal fitting for the case of falling output transition as well as for the case of rising output transitions at marginal $\Delta$ values. Moreover, considerably promising is the negligible absolute error value of 0.3% for the mismatch associated with $\Delta = 0$.

VI. MODELING ACCURACY EXPERIMENTS

In this section, we experimentally compare the modeling accuracy of our new model to the ideal switch hybrid model \cite{23}, the IDM and to classic inertial delays, using the publicly available Involution Tool \cite{13}. Albeit it performs dynamic digital timing simulation in VHDL, it also supports delay models implemented in Python. We hence implemented our model, that is, the delay functions given in Theorem 2 in Python.

For our experimental evaluation, we used the same setup as in \cite{23}, namely the 15 nm Nangate Open Cell Library featuring FreePDK15 \textsuperscript{TM} FinFET models \cite{27} ($V_{DD} = 0.8$ V) that has also been used in Section II. Based on a Verilog description of our NOR gate, we performed optimization, placement and routing by utilizing the Cadence tools Genus and Innovus (version 19.11). We also extracted the parasitic networks from the final layout to obtain SPICE models. These models allowed us to perform simulations with Spectre (version 19.1), which are used to produce golden reference digital signal traces, by recording their $V_{DD}/2$ crossings. All simulations in our delay model used the final parameters from Table III. For the ideal switch model and the IDM Exp-channel, the parameters reported in \cite{23} were used.

In order to quantify and compare the typical (average) modeling accuracy of our competing delay models, we stimulated our NOR circuit with randomly generated waveforms. Our experiments targeted both fast (100/50) and slow (200/100) pulse trains on every input, with (LOCAL) and without (GLOBAL) concurrent transitions. For example, the configuration **100/50 - LOCAL** of the Involution Tool generates transitions independently on both input A and B, according to a normal distribution with $\mu = 100$ ps and $\sigma = 50$ ps. The configuration **200/100 - GLOBAL** generates transitions either on input A or on B, with $\mu = 200$ ps and $\sigma = 100$ ps. Each simulation run consisted of 500 transitions and has been repeated 200 times.

As our modeling accuracy comparison metric, we used the area deviation trace, which is the absolute value of the difference between the SPICE trace and the trace generated by the respective delay model integrated over time. However, since the absolute values largely depend on the number of transitions, and are therefore meaningless per se, we normalized them with respect to the inertial delays, which is our baseline model. Consequently, lower bars indicate less area under the deviation trace and hence better results. Fig. 5 shows the results of our experiments. It is apparent that our model outperforms the ideal switch hybrid model \cite{23} in the case of fast pulse trains, where the increased modelling accuracy of the falling output MIS delay comes into effect: Around 5% is gained in the case of **100/50 - LOCAL**. Whereas this improvement appears to be small, it needs to be stressed that it is the average accuracy that we are evaluating: Since the randomly generated inputs are unlikely to create many transitions very close to each other (i.e., small $\Delta$), where the superiority of our model w.r.t. MIS effects for rising output transitions would kick in, one cannot expect much improvement here. In applications like \cite{3}, however, pulse trains containing such transitions do occur.

We conclude this section with noting that the simulation times (in the few second-range) for all our models turned out to be similar. More specifically, the inertial delay model (which is natively...
implemented in ModelSim) is only around 33% faster than both the IDM model and the two hybrid models in all our configurations. Given that both hybrid models have been implemented in Python, we can safely say that predicting gate delays using our new model does not incur a significant overhead in terms of simulation running times. Whereas it appears that the simulation times in SPICE also match the ones of ModelSim in configurations like 100/50 - LOCAL and the ones of our hybrid models in 5000/5 - GLOBAL, this is only due to the fact that the simulated circuit is so small. As already mentioned in Section IV, the SPICE simulation times quickly go up with the number of transistors in the circuit.

VII. HYBRID DELAY MODELS FOR OTHER GATES

In this section, we will demonstrate that our general approach can be applied to other gates as well. We mentioned already at the end of Section III-A that our results for the NOR gate can be transferred to the case of a NAND gate by simply swapping nMOS transistors with pMOS transistors and vice versa, as well as swapping the supply voltage (V_{DD} and GND). In addition, we mentioned that, in some recent work that could not be referenced for anonymity reasons, we extended our model for the NOR gate by adding an RC interconnect and experimentally verified its very good accuracy.

More generally, we believe that it is easy to apply our modeling approach to any CMOS gate that involves serial and parallel transistors only, like Muller C gates and AOI (and-or-inverter) gates. We will demonstrate this for the Muller C gate, which plays a prominent role in many asynchronous circuit designs, like the one [3] already mentioned in Section IV.

We will apply our approach to the CMOS implementation of C shown in Fig. 6a, which involves a state keeper element made up of a loop of two inverters. Whereas this seems to complicate our modeling at first sight, it turns out that we can safely drop it from our considerations altogether. The (ideal) load capacitance C in the corresponding resistor model of Fig. 6b acts as the state keeper for V_{out} in the case the output is in a high-impedance state, i.e., when both at least one of P1 and P2 and at least one of N1 and N2 are switched off. In order to accommodate the negative of the output, we just let R_1 and R_2 correspond to the nMOS transistors N_2 and N_1, and R_3 and R_4 to the pMOS transistors P_1 and P_2.

Similar to the NOR gate, we use continuously varying resistors according to [1] for the switching-on and instantaneous switching-off, but this time for all transistors. Applying Kirchhoff’s rules to Fig. 6b leads to the first-order non-homogeneous ordinary differential equation (ODE) with non-constant coefficients

\[
\frac{dV_{out}}{dt} + \frac{V_{out}}{CR_0(t)} = U(t),
\]

where \(1/R(g(t)) = \frac{1}{R_2(t)} + \frac{1}{R_4(t)} + \frac{1}{R_2(t)} + \frac{1}{R_4(t)} \) and \(U(t) = \frac{V_{DD}}{C(R_2(t))} \). It is not difficult to check that a similar solution approach as described in Section IV leads to the following expressions for the output voltage, for rising resp. falling input transitions and \(\Delta \geq 0\), corresponding to (5) and (6) resp. (8) and (20):

\[
\begin{align*}
V_{out}^{+}(t) &= V_{out}^{+}(0), \\
V_{out}^{-}(t) &= V_{out}^{-}(\Delta) = e^{-\frac{(2R_2 R_4 + t)}{2CR_0(t)}} + V_{DD}(1 - \gamma_n e^{-\frac{t}{2R_0(t)}}), \\
V_{out}^{+}(t) &= V_{out}^{+}(0), \\
V_{out}^{-}(t) &= V_{out}^{-}(\Delta) = e^{-\frac{(2R_2 R_4 + t)}{2CR_0(t)}},
\end{align*}
\]

with \(V_{out}^{+}(0)\) and \(V_{out}^{-}(0)\) as the initial values of the transitions \((0, 0) \rightarrow (1, 0)\) and \((1, 1) \rightarrow (0, 1)\), respectively. Herein, \(\bar{t}_n\) and \(\gamma_n\) are defined exactly as in (12) to (16) with substituting 2R by 2R_n = R_{n, \text{list}}. Similarly, \(\bar{t}_p\) and \(\gamma_p\) are obtained by replacing \(\bar{t}_n\) and \(\gamma_n\) in (12) to (16). Finally, the following theorem, whose proof is very similar to the one for Theorem 2 provides the delay formulas for the C gate.

**Theorem 3** (MIS and SIS delay functions for the C gate, for arbitrary initial values). For any \(0 \leq \Delta \leq \infty\), the delay functions for falling and rising output transitions of our model, when starting from a given initial value \(V_{out}(0)\), are

\[
\begin{align*}
\delta_{E,\text{M},+}(\Delta) &\approx 2R_n C \left(\ln\left(\frac{2V_{DD} + 2\Delta - V_{out}^{+}(\Delta)e^{-\frac{\bar{t}_n}{C}}}\right)\right), \\
\delta_{E,\text{M},-}(\Delta) &\approx 2R_p C \left(\ln\left(\frac{2V_{out}^{-}(\Delta) - V_{DD}}{2\Delta}\right) - \frac{\bar{t}_p}{C}\right).
\end{align*}
\]

As for the NOR gate, the trajectory and delay formulas for \(\Delta < 0\) can be easily obtained by the symmetry mentioned in Section IV.

We demonstrate the good accuracy of this hybrid delay model by comparing the model predictions and the SPICE simulation data for a 15nm CMOS technology C gate. For model parametrization, we could re-use the procedure for the NOR gate, which provided the parameters listed in in Table V. The comparison results are shown in Fig. 6c and Fig. 6d.

**TABLE V:** Model parameter values for the 15nm C gate that produced the dashed red curves in Fig. 6c and Fig. 6d.

| Parameter | Value | Parameter | Value |
|-----------|-------|-----------|-------|
| \(R_n\)   | 33002226 | \(\alpha_3\) | 0.157 \times 10^{-4} |
| \(\alpha_1\) | 2.9122262 | \(\alpha_4\) | 0.061 \times 10^{-4} |
| \(C\)     | 0.0001 |

VIII. CONCLUSIONS

We provided a novel approach for developing hybrid delay models for dynamic timing analysis of CMOS gates, and showed that it is capable of faithfully covering all MIS effects in the case of a NOR gate and a Muller C gate. Relying on a first-order model of dimension 1, the resulting model for the NOR gate is even simpler than the immediate switch hybrid ODE model proposed in [23], albeit it does not share its failure to model the MIS effect for rising output transitions. Thanks to its simplicity, it allows to compute accurate approximation formulas for the gate delays, which makes the model efficiently applicable in dynamic digital timing analysis and facilitates easy model parametrization. An experimental comparison of the modeling accuracy against alternative approaches confirmed its superior performance.
Fig. 6: CMOS 15 nm technology C gate implementation, along with the predicted ($\delta_{13}(\Delta)$) and measured ($\delta_{13}(\Delta)$) MIS delays.

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