Solution processed low-voltage metal-oxide transistor by using TiO$_2$/Li–Al$_2$O$_3$ stacked gate dielectric

Nila Pal$^1$, Utkarsh Pandey$^1$, Sajal Biring$^{2,*}$, and Bhola N. Pal$^{1,2,*}$

$^1$School of Materials Science and Technology, Indian Institute of Technology (Banaras Hindu University), Varanasi 221005, India

$^2$Organic Electronic Research Centre and Department of Electronic Engineering, Ming-Chi University of Technology, New Taipei City 243, Taiwan

Received: 20 March 2021
Accepted: 10 December 2021
Published online: 29 January 2022

ABSTRACT

A solution processed top-contact bottom-gated SnO$_2$ thin-film transistor (TFT) has been fabricated using a TiO$_2$/Li–Al$_2$O$_3$ bilayer stacked gate dielectric that show operating voltage of this TFT within 2.0 V. It is observed that the bilayer dielectric has much higher areal capacitance with lower leakage current density that significantly improve the overall device performance of TFT. The TFT with bilayer gate dielectric shows an effective carrier mobility ($\mu_{sat}$) of 9.2 cm$^2$ - V$^{-1}$ s$^{-1}$ with an on/off ratio of $7.1 \times 10^3$ which are significantly higher with respect to the TFT with a single layer Li–Al$_2$O$_3$ gate dielectric. The origin of this improvement is due to the Schottky junction between the highly doped silicon (p$^{++}$-Si) and TiO$_2$ of bilayer stacked dielectric that induced electrons to the channel which reduces the dielectric/semiconductor interface trap-state. This investigation opens a new path to develop TFT device performance using a suitable bilayer stack of gate dielectric.

1 Introduction

The charge carrier conduction of the channel of a thin-film transistor (TFT) normally occurs within <10 nm thickness of the semiconductor film next to the gate dielectric [1]. Therefore, the field effect charge transport phenomena of a TFT is not only dependent on the microstructures of the semiconductor but is also strongly affected by the surface properties of the gate insulator [2]. Conventional silicon gate dielectric (SiO$_2$) commonly offers smooth surface morphology which is capable of minimizing the defect density of semiconductor–insulator interface. However, the dielectric constant of SiO$_2$ is very low (3.9). Therefore, to reduce the operating voltage of a TFT below 2 V for portable electronics application, it requires very low thickness of SiO$_2$ (<10 nm) which sometime becomes very leaky [3, 4]. Employment of high-k dielectric materials instead of SiO$_2$ is the best alternative which allow us to deposit thicker dielectric film by maintaining the advantage of low operating voltage TFT fabrication [5–9]. However, ionic bonds in high-k dielectrics results in high defect concentrations with oxygen vacancies ($V_O$) being the primary source of traps. These can be source of fixed charges or act as electron traps that decreases the effective carrier
mobility of the device. Moreover, this trap-states can change the threshold voltage ($V_T$) of the device and increases the gate-leakage current [10], decreasing device performance and the stability of devices. To overcome these problems, different approaches like inorganic–organic hybrid dielectric [11, 12], multi-component dielectric [13], bilayer dielectric stack [14–16], composite solid polymer electrolyte (CSPE) [17] have been used. Many of these dielectrics are solution processable and can be printed by different printing technique [18]. To reduce the semiconductor/dielectric interface trap-state, recently, a new method has been developed by implying n-type TiO$_2$ as interface layer between highly doped silicon ($p^{++}$-Si) substrate and high-k ion conducting Li$_5$AlO$_4$ dielectric, which drastically enhance the TFT device performance due to the formation of Schottky junction of $p^{++}$-Si/TiO$_2$ [19]. However, capacitance of that Li$_5$AlO$_4$/TiO$_2$ stacked dielectric reduce rapidly above $10^4$ Hz [19]. To enhance the frequency range and overall performance of TFT, more detailed study is required for different combinations of stacked dielectric.

In this work, we have synthesized Li-doped alumina (Li–Al$_2$O$_3$) thin film by sol–gel method and have used this ionic dielectric to fabricate TiO$_2$/Li–Al$_2$O$_3$ stacked gate dielectric. The variation of areal capacitance of this bilayer stacked gate dielectric reduces only by 20% up to the frequency $10^5$ Hz. To realize the overall improvement of TFT performance and the mechanism of this development, two sets of solution processed SnO$_2$ TFT were fabricated; one with TiO$_2$ gate interface and another without gate interface. Comparative studies of these two TFT reveals a significant improvement of device performance. A schematic presentation of energy bandgap of multilayer thin films and related charge transfer of $p^{++}$-Si/TiO$_2$ Schottky junction explain the probable reason for enhancing device performance.

2 Experimental

2.1 Material synthesis

As mentioned earlier, all TFTs are fabricated by low-cost solution processed technique. In this process, both gate dielectric (TiO$_2$ and Li–Al$_2$O$_3$) and semiconducting layers (SnO$_2$) are deposited from the precursor solution by spin coating method. For TiO$_2$ deposition, a solution of 100 mM was prepared by dissolving Titanium(IV) Butoxide in 2-methoxy ethanol (2ME) followed at the room temperature stirring process by a magnetic stirrer about 30 min. Similarly, to prepare the Li–Al$_2$O$_3$ dielectric, two different solutions of lithium acetate and aluminium nitrate nonahydrate of concentration 500 mM were prepared using 2-methoxy ethanol as solvent. These two homogeneous solutions are mixed with a ratio of 1:11 to maintain the atomic ratio of the final product of Li–Al$_2$O$_3$. This mixture of solutions was left for 24 h for proper gelation before deposition [20]. Finally, solution was filtered by 0.45 µm PVDF filter before spin coating. For semiconductor (SnO$_2$) thin-film deposition, a solution of SnCl$_2$ has been prepared using 2-methoxy ethanol as solvent.

2.2 Device fabrication

Metal-oxide TFTs are fabricated in a top-contact bottom-gate configuration using highly $p$-doped Si wafer ($p^{++}$-Si) as a substrate as well as gate electrode. Initially, all the Si wafers are cleaned with standard cleaning process. After wet cleaning, wafers were treated with an oxygen plasma for 10 min before spin coating. Plasma treatment makes the surface hydrophilic which increases the adhesive property and helps to form pinhole-free smooth film during spin coating. Two types of devices are fabricated without and with TiO$_2$ interface named as Device 1 and Device 2 shown in Fig. 1a and b, respectively. The TiO$_2$ thin film is deposited on $p^{++}$-Si wafer spin coating with a spinning speed of 3500 rpm for 40 s followed by a drying process of a preheated hot-plate (set at 90 °C) to evaporate the solvent. Afterwards, this film was annealed at 350 °C for 30 min to form a polycrystalline thin film of TiO$_2$. On top of this, the precursor solution of Li–Al$_2$O$_3$ was spin coated with a speed 5000 rpm for 50 s followed by annealing process at 350 °C for 30 min. The dielectric film coating was repeated three times to achieve a desired thickness of the dielectric layer. Finally this film was annealed at 500 °C for 1 h to form Li–Al$_2$O$_3$ thin film. For Device 1, the same procedure was followed except the TiO$_2$ layer deposition. After dielectric deposition, the precursor solution of SnO$_2$ was spin coated (4000 rpm for 40 s) and subsequent annealing (500 °C for 30 min) process [17]. Finally, aluminium source/drain electrode are deposited by thermal evaporation method with width-to-length ratio of 118.
In addition to this TFT fabrication, the metal–insulator–metal (MIM) devices (Fig. 1c and d) were fabricated in a similar process for the electrical characterization of single and bilayer dielectric thin films.

2.3 Material and device characterization

Crystal phase/structural analysis of thin films were carried out by grazing incidence XRD (Rikagu, Smart Lab) with monochromatized Cu Kα radiation (λ = 1.5405 Å). Atomic force microscopy (AFM) study has been performed using “NTMDTNTEGRA-prima” to measure the roughness of different thin-film surfaces. Thin films are deposited on p+-Si substrate in both cases. Frequency vs. capacitance (C–f) measurement has been done by LCR meter (Keysight LCR meter E4990A). All the electrical characteristics of TFTs and leakage current measurement of MIM devices have been measured by semiconductor parameter analyzer (KEYSIGHT B1500A).

3 Results and discussion

3.1 Grazing incidence X-ray diffraction pattern of thin films

To analyse the structural properties of spin coated TiO₂, Li–Al₂O₃ and SnO₂ thin film, individually all these thin films were deposited on p++-Si substrate under the same condition of TFT fabrication. Figure 2a shows the GIXRD patterns of TiO₂ thin film which indicates a crystalline peak at 2θ ~ 25.28°, which is corresponding to the (101) plane of stable anatase phase of TiO₂. The GIXRD patterns of Li–Al₂O₃ dielectric which is shown in Fig. 2b did not show any diffraction peak, indicating the amorphous nature of Li–Al₂O₃ dielectric.

The GIXRD pattern of SnO₂ thin film has been shown in Fig. 2c that clearly identified diffraction peaks at the 2θ angle 26.6, 34.2, 52.7, and 54.7 which corresponds the reflection planes of (110), (101), (211), and (220), respectively; justify the tetragonal phase of SnO₂ (JCPDS 88-0287).

3.2 Surface morphology of dielectric thin films

The surface morphologies of single layer Li–Al₂O₃ and bilayer TiO₂/Li–Al₂O₃ dielectrics were studied by atomic force microscopy (AFM). All these dielectric layers were deposited on p++-Si substrates with the same condition as for TFT fabrication. The 2D and 3D morphologies of these two dielectric thin films are shown in Fig. 3a–d. Figure 3a and c represents the AFM images of Li–Al₂O₃ dielectric, whereas Fig. 3b and d represents AFM pictures of TiO₂/Li–Al₂O₃ dielectrics. This study shows that the RMS roughness of both dielectric thin films are < 1 nm which is suitable for high-performance TFT fabrication. However, surface roughness of single layer (Li–Al₂O₃) dielectric (0.26 nm) is little bit smoother than bilayer (TiO₂/Li–Al₂O₃) dielectric (0.46 nm). Similarly, AFM study has been performed on SnO₂ thin film deposited on single and bilayer dielectrics which are shown in Fig. 3e–h, indicating their roughness below 1 nm.

3.3 Dielectric and electrical characterization

The leakage current density and areal capacitance of single layer and bilayer dielectric are measured with metal–insulator–metal (MIM) architecture which is shown in Fig. 4. Figure 4a shows the leakage current density vs. applied voltage graphs of both dielectric thin films. This data indicate that stacked dielectric of p++-Si/TiO₂/Li–Al₂O₃/Al device has one order lower leakage current density than p++-Si/Li–Al₂O₃/Al device at applied voltage 2 V with a current density of 6.2 × 10⁻⁵ A/cm², whereas single layer dielectric MIM device shows a current density of 2.0 × 10⁻⁴ A/cm² at 2.0 V. The dielectric-leakage
The current of bilayer film is reasonably low for TFT fabrication that operates within 2.0 V operating voltage. The reduction of gate-leakage current in case of bilayer dielectric may be resulted from the lattice mismatch of two different materials with different grain shapes at the interfaces, which is well understood from the earlier multilayered dielectric studies [16].

The variation of capacitance per unit area of the same set of MIM devices with frequencies (20 to 10^5 Hz) at room temperature are represented in Fig. 4b. It is well known that the capacitance decreases with frequency due to the different relaxation times originated from different types of polarization contribution [7]. Similar behaviour is observed in both types of MIM devices that reduce significantly > 10^5 Hz. However, the capacitance of single layer p++-Si/Li–Al2O3/Al device changes more rapidly compared to bilayer p++-Si/TiO2/Li–Al2O3/Al MIM device. The measured areal capacitance (C) values of single and bilayer MIM devices are 55 nF/cm^2 and 66 nF/cm^2 at 50 Hz frequency, respectively. This study is the indication of the higher areal capacitance value with wider frequency range of a bilayer stacked dielectric thin film which originated from additional TiO2 layer. The TiO2/Li–Al2O3 bilayer act as series combination of TiO2 and Li–Al2O3 parallel plate capacitor and the resultant capacitance can be written as

\[
\frac{1}{C_{\text{effective}}} = \frac{1}{C_{\text{TiO}_2}} + \frac{1}{C_{\text{Li–Al}_2\text{O}_3}}
\]

The high-k value of TiO2 layer increases the capacitance of TiO2/Li–Al2O3 dielectric with respect to Li–Al2O3 single layer.

### 3.4 Electrical characterization of single and bilayer dielectric thin-film transistor

To realize the performance of these dielectric layers for the application of gate dielectric of TFTs, two sets of devices have been fabricated. Device 1 is the reference TFT without TiO2 gate interface and Device 2 is TFT with TiO2 gate interface in between gate electrode and Li–Al2O3 gate dielectric. A higher channel length of 200 μm with W/L (W = 23.6 mm, L = 0.2 mm) ratio of 118 is chosen to avoid the overestimation of carrier mobility value due to grain boundary effect, which is highly dominating below 25 μm channel length and W/L ratio of 10 [21, 22]. Additionally, high-performance TFT with larger device area demands good quality of dielectric with pinhole-free uniform thin film with very low defect states. Figure 5 shows transistor characteristics of two types of device, and are measured at ambient conditions. The \( I_D-V_D \) characteristics of two sets of devices are compared and the threshold voltage of Device 2 (0.29 V) is significantly lower than Device 1 (0.85 V). Besides, the calculated value of \( I_{\text{ON}}/I_{\text{OFF}} \) ratio for Device 2 is \( 7.2 \times 10^5 \) which is higher than Device 1 (i.e. 10^4).
The effective carrier mobility ($\mu$), subthreshold swing (SS), and dielectric/semiconductor interface trap-states ($N_{\text{MaxSS}}$) of TFT have been calculated by using the following equations [23]:

$$I_D = \mu \frac{W}{2L} (V_G - V_T)^2$$  \hspace{1cm} (1)

$$\text{SS} = \left[ \frac{d \log(I_D)}{dV_G} \right]^{-1}$$  \hspace{1cm} (2)

$$N_{\text{MaxSS}} = \left[ \frac{\text{SS} \times \log(e)}{\frac{\mu q}{kT}} - 1 \right] \frac{C}{q}$$  \hspace{1cm} (3)

where $k$, $T$, and $q$ are the Boltzmann constant, temperature in absolute scale and charge of electron, respectively. The saturation carrier mobilities of both devices are calculated using Eq. 1 and extracted from the linear fitting of $(I_D)^{1/2}$ vs. $V_G$ plot. From comparison of both devices, it is observed that Device 2 shows better performance having saturation electron mobility of 9.2 cm$^2$ V$^{-1}$ s$^{-1}$ than Device 1 that shows saturation electron mobility of 7.7 cm$^2$ V$^{-1}$ s$^{-1}$. Besides, we have calculated carrier mobility by considering the ‘reliability factor ($r_{\text{lin}}$)’ with this calculation that arises due to the faulty capacitance values, erroneous measurement of $V_T$ and irregular shape of the $I_D$ vs. $V_G$ suggested by earlier works which gives only $\sim$ 3% variation with earlier calculation (Table 1) [24, 25]. The subthreshold swing (SS) value of both devices are extracted from the slope at lower gate voltage regime of the log ($I_D$) vs. $V_G$ graphs (shown in Fig. 5e and f and by using Eq. 2). Device 2 has lower SS value (250 mV/decade) than Device 1 (280 mV/decade). The dielectric–semiconductor interface trap-state densities have been derived from Eq. 3. Device 1 has 1.5 times higher interface trap-state density than Device 2. The lower $N_{\text{MaxSS}}$ leads to less trapping of charge carriers in the dielectric–semiconductor interface, resulting in improvement of effective mobility and higher drain current [26]. All the TFT parameters are summarized in Table 1.

To understand the reason behind the higher performance of Device 2 with TiO$_2$/Li–Al$_2$O$_3$ stack dielectric, a schematic diagram of energy bands of two types of SnO$_2$ TFTs have been illustrated in Fig. 6. Since p$^{+}$Si(111)/TiO$_2$ interface forms a Schottky junction at zero gate bias, the electron of TiO$_2$ layer transferred to the p$^{+}$Si gate electrode creates a depleted layer of positive charge at TiO$_2$ thin film. However, hole is not allowed to transfer from p$^{+}$Si to TiO$_2$ layer due to large potential barrier in p$^{+}$Si(111)/TiO$_2$ interface [27, 28]. Hence, the layer of positive charge of TiO$_2$ thin film induces electrons of the channel of TFT (SnO$_2$) to accumulate at the Li–Al$_2$O$_3$/SnO$_2$ interface (Fig. 6a). This phenomenon is happening without gate bias. Therefore, TiO$_2$ thin film effectively reduces the interface trap-states, resulting in a lower subthreshold swing and threshold voltage. Although, these phenomena are not occurring in Device 1 because of the high barrier height of insulating Li–Al$_2$O$_3$ layer. Therefore, electrons cannot be ejected from Li–Al$_2$O$_3$ to p$^{+}$Si gate electrode (Fig. 6c). Under accumulation mode operation, a positive gate voltage is
applied to both of the devices (Fig. 6b and d). However, this bias does not change the depletion layer width of p$^{++}$-Si(111)/TiO$_2$ interface due to the intermediate insulating Li–Al$_2$O$_3$ layer. These

Table 1 Summary of the TFT parameters of SnO$_2$ transistors with single layer and bilayer stack gate dielectrics

| Device            | Threshold voltage (V) | $I_{ON}/I_{OFF}$ | Subthreshold swing (mV decade$^{-1}$) | Saturation mobility (cm$^2$V$^{-1}$s$^{-1}$) | Saturation mobility with reliability factor ($\mu_{lin}$) (cm$^2$V$^{-1}$s$^{-1}$) | Interface trap-state density (cm$^{-2}$) |
|-------------------|-----------------------|-----------------|----------------------------------------|---------------------------------------------|--------------------------------------------------------------------------------|----------------------------------------|
| Si$^{++}$/Li–Al$_2$O$_3$/SnO$_2$/Al | 0.85                  | $3.6 \times 10^3$ | 280                                    | 7.7                                         | 7.9 (2.7%↑)                                                                      | $1.6 \times 10^{12}$                   |
| Si$^{++}$/TiO$_2$/Li–Al$_2$O$_3$/SnO$_2$/Al | 0.29                  | $7.2 \times 10^3$ | 250                                    | 9.2                                         | 9.0 (3%↓)                                                                      | $1.1 \times 10^{12}$                   |
phenomena effectively enhance the accumulation of mobile charge carriers in the channel of Device 2, which improves the device performance over Device 1.

4 Conclusion

In conclusion, high-performance solution processed low operating voltage SnO$_2$ thin-film transistor has been fabricated onto sol–gel derived ion-conduction Li–Al$_2$O$_3$ dielectric using TiO$_2$ gate interface. A comparative study of two sets of SnO$_2$ TFTs with and without TiO$_2$ interface have been demonstrated. The Schottky junction formation between p$^{++}$-Si and n-type TiO$_2$ help to accumulate extra electrons at the Li–Al$_2$O$_3$/SnO$_2$ interface, which essentially fills up the interface trap-states and reduces the subthreshold swing (SS) as well as threshold voltage ($V_T$) and enhance the saturation carrier mobility of the device with compared to the device without TiO$_2$ interface. The high-k value of TiO$_2$ improves the capacitance of the TiO$_2$/Li–Al$_2$O$_3$ stack dielectric as well as it’s leakage current reduced compared to single layered Li–Al$_2$O$_3$ dielectric. We have achieved an effective carrier mobility ($\mu_{\text{sat}}$) of 9.2 cm$^2$V$^{-1}$s$^{-1}$, SS of 250 mV/decade, and $V_T$ of 0.29 V in TiO$_2$/Li–Al$_2$O$_3$ stack TFT with an $I_{\text{ON}}/I_{\text{OFF}}$ ratio of $7.2 \times 10^3$. This investigation opens a new path to develop high-performance TFT devices using a suitable bilayer stack of gate dielectrics.

Acknowledgements

This work was supported by the “Science and Engineering Research Board,” India (Grant No. EMR/2015/000689). The authors are grateful to the Central Instrument Facility Centre, IIT (BHU), for providing the AFM measurement facility. Nila Pal thanks DST-SERB for providing SRF fellowship, and Utkarsh Pandey thanks IIT (BHU) for providing Ph.D. fellowship.
Author contributions

NP did most of the experimental research work, manuscript writing, data analysis. UP did partial experimental research work and data analysis. SB gave some measurement facilities and jointly figure out the outline of this work. BNP supervise this research work.

Funding

Funding was provided by Science and Engineering Research Board (Grant Nos. CRG/2019/001826 and EMR/2015/000689).

Data availability

The datasets generated during and/or analysed during the current study are available from the corresponding author on reasonable request.

Declarations

Conflict of interest The authors declare no competing financial interest.

References

1. J. Zaumseil, H. Sirringhaus, Electron and ambipolar transport in organic field-effect transistors. Chem. Rev 107(4), 1296–1323 (2007)
2. C. Kim, A. Facchetti, T.J. Marks, Gate dielectric microstructural control of pentacene film growth mode and field-effect transistor performance. Adv. Mater. 19(18), 2561–2566 (2007)
3. J. Robertson, R.M. Wallace, High-K materials and metal gates for CMOS applications. Mater. Sci. Eng. R Rep. 88, 1–41 (2015)
4. Committee, I. R., International technology roadmap for semiconductors. 2008.
5. B.N. Pal, B.M. Dhar, K.C. See, H.E. Katz, Solution-deposited sodium beta-alumina gate dielectrics for low-voltage and transparent field-effect transistors. Nat. Mater. 8(11), 898 (2009)
6. N.K. Chourasia, A. Sharma, V. Acharya, N. Pal, S. Biring, B.N. Pal, Solution processed low band gap ion-conducting gate dielectric for low voltage metal oxide transistor. J. Alloys Compd. 777, 1124–1132 (2019)
7. B. Wang, W. Huang, L. Chi, M. Al-Hashimi, T.J. Marks, A. Facchetti, High-k gate dielectrics for emerging flexible and stretchable electronics. Chem. Rev. 118(11), 5690–5754 (2018)
8. A. Sharma, N.K. Chourasia, A. Sugathan, Y. Kumar, S. Jit, S.-W. Liu, A. Pandey, S. Biring, B.N. Pal, Solution processed Li3AlO4 dielectric for low voltage transistor fabrication and its application in metal oxide/quantum dot heterojunction phototransistors. J. Mater. Chem. C 6(4), 790–798 (2018)
9. A. Sharma, N.K. Chourasia, V. Acharya, N. Pal, S. Biring, S.-W. Liu, B.N. Pal, Ultra-low voltage metal oxide thin film transistor by low-temperature annealed solution processed LiAlO2 gate dielectric. Electron. Mater. Lett. 16(1), 22–34 (2020)
10. S. Mohsenifar, M. Shahrokhabadi, Gate stack high-k materials for Si-based MOSFETs past, present, and futures. Microelectron. Solid State Electron. 2, 5 (2015)
11. Q. Li, S. Li, D. Yang, W. Su, Y. Wang, W. Zhou, H. Liu, S. Xie, Designing hybrid gate dielectric for fully printing high-performance carbon nanotube thin film transistors. Nanotechnology 28(43), 435203 (2017)
12. H.S. Kim, P.D. Byrne, A. Facchetti, T.J. Marks, High performance solution-processed indium oxide thin-film transistors. J. Am. Chem. Soc. 130(38), 12580–12581 (2008)
13. J. Martins, A. Kiazadeh, J.V. Pinto, A. Rovisco, T. Goncalves, J. Deuermeier, E. Alves, R. Martins, E. Fortunato, P. Barquinha, Ta2O5/SiO2 multicomponent dielectrics for amorphous oxide TFTs. Electron. Mater. 2(1), 1–16 (2021)
14. J.-W. Jo, K.-H. Kim, J. Kim, S.G. Ban, Y.-H. Kim, S.K. Park, High-mobility and hysteresis-free flexible oxide thin-film transistors and circuits by using bilayer sol–gel gate dielectrics. ACS Appl. Mater. Interfaces 10(3), 2679–2687 (2018)
15. K. Pak, J. Choi, C. Lee, S.G. Im, Low-power, flexible non-volatile organic transistor memory based on an ultrathin bilayer dielectric stack. Adv. Electron. Mater. 5(4), 1800799 (2019)
16. J.-P. Locquet, C. Marchiori, M. Sousa, J. Fompeyrine, J.W. Seo, High-K dielectrics for the gate stack. J. Appl. Phys. 100(5), 051610 (2006)
17. S.K. Garlapati, N. Mishra, S. Dehm, R. Hahn, R. Kruk, H. Hahn, S. Dasgupta, Electrolyte-gated, high mobility inorganic oxide transistors from printed metal halides. ACS Appl. Mater. Interfaces 5(22), 11498–11502 (2013)
18. S.K. Garlapati, M. Divya, B. Breitung, R. Kruk, H. Hahn, S. Dasgupta, Printed electronics based on inorganic semiconductors: From processes and materials to devices. Adv. Mater. 30(40), 1707600 (2018)
19. A. Sharma, N.K. Chourasia, N. Pal, S. Biring, B.N. Pal, Role of electron donation of TiO2 gate interface for developing solution-processed high-performance one-volt metal-oxide
thin-film transistor using ion-conducting gate dielectric. J. Phys. Chem. C 123(33), 20278–20286 (2019)
20. Y. Liu, P. Guan, B. Zhang, M.L. Falk, H.E. Katz, Ion dependence of gate dielectric behavior of alkali metal ion-incorporated aluminas in oxide field-effect transistors. Chem. Mater. 25(19), 3788–3796 (2013)
21. K. Okamura, D. Nikolova, N. Mechau, H. Hahn, Appropriate choice of channel ratio in thin-film transistors for the exact determination of field-effect mobility. Appl. Phys. Lett. 94(18), 183503 (2009)
22. G. Adamopoulos, A. Bashir, S. Thomas, W.P. Gillin, S. Georgakopoulos, M. Shkunov, M.A. Baklar, N. Stingelin, R.C. Maher, L.F. Cohen, Spray-deposited Li-doped ZnO transistors with electron mobility exceeding 50 cm²/Vs. Adv. Mater. 22(42), 4764–4769 (2010)
23. E. Fortunato, P. Barquinha, R. Martins, Oxide semiconductor thin-film transistors: A review of recent advances. Adv. Mater. 24(22), 2945–2986 (2012)
24. H.H. Choi, K. Cho, C.D. Frisbie, H. Sirringhaus, V. Podzorov, Critical assessment of charge mobility extraction in FETs. Nat. Mater. 17(1), 2–7 (2018)
25. N. Cherukupally, M. Divya, S. Dasgupta, A comparative study on printable solid electrolytes toward ultrahigh current and environmentally stable thin film transistors. Adv. Electron. Mater. 6(12), 2000788 (2020)
26. C. Zhu, A. Liu, G. Liu, G. Jiang, Y. Meng, E. Fortunato, R. Martins, F. Shan, Low-temperature, nontoxic water-induced high-k zirconium oxide dielectrics for low-voltage, high-performance oxide thin-film transistors. J. Mater. Chem. C 4(45), 10715–10721 (2016)
27. J. Jhaveri, A.H. Berg, J.C. Sturm, Isolation of hole versus electron current at p-Si/TiO₂ selective contact using a heterojunction bipolar transistor structure. IEEE J. Photovolt. 8(3), 726–732 (2018)
28. S. Avasthi, W.E. McClain, G. Man, A. Kahn, J. Schwartz, J.C. Sturm, Hole-blocking titanium-oxide/silicon heterojunction and its application to photovoltaics. Appl. Phys. Lett. 102(20), 203901 (2013)

Publisher’s Note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.