Ball Misplace Mitigation through Process Optimization of Advanced Leadframe Package

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Authors’ contributions

This work was carried out in collaboration amongst all authors. All authors read, reviewed and approved the final manuscript.

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ABSTRACT

One of the challenging assembly processes in semiconductor manufacturing industry is stencil printing using solder paste as direct material. With this technology, some issues were encountered during the development phase of an advanced leadframe device and one of which is the solder ball misplace or off-centered ball. This paper, hence, focused on addressing the ball misplace issue at stencil printing process. Comprehensive parameter optimization particularly on the print speed and print force was employed to eliminate or significantly reduce the ball misplace defect at stencil printing process. With this process optimization and improvement, a reduction of around 96 percent ball misplace occurrence was achieved.

Keywords: Solder bumping; stencil printing process; off-centered ball; leadframe; assembly.

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1. INTRODUCTION

Stencil printing is the process of depositing solder paste on the printed wiring boards to establish electrical connections. Leadframe package technology is one of the platforms for integrated circuit (IC) packages in semiconductor industry market. The fast pace growth on IC package provides the need for every industry to come up with more innovative packaging solutions to stay competitive in the market. With new and continuous technology trends and breakthroughs, challenges in assembly manufacturing are inevitable [1-5]. In this paper, an advanced leadframe package was able to use solder paste material on the bottom area to provide the electrical connections, however, challenges were encountered. The paper presents a solution to process this type of new technology with ball misplace or off-centered ball issue encountered during the assembly process. To guarantee its integrity during processing, stencil printing is incorporated with criteria such as ball height and ball diameter. This stencil printing criteria is performed after machine setup and conversion to ensure the product is reliable when subjected to a reliability test. Fig. 1 shows the actual defect manifestation of off-centered ball.

2. LITERATURE REVIEW AND PROBLEM IDENTIFICATION

A complete assembly process flow for the device in focus starting pre-assembly to singulation process is shown in Fig. 2. Highlighted is the process where the issue was encountered. Worthy to note that assembly process flow varies with the product and the technology [2,6-9].

Off-centered ball is the top major assembly reject in stencil printing process, and this was seen during lot processing of the package at stencil printing process. This off-centered ball issue is caused by a viscous solder paste material and the issue is occur during stencil process. The solder paste material is a conductive paste used on the package. During stencil printing process, parameter optimization is normally done in this type of technology and it is a very big challenge because we need to run the lot and to supply our customer with speed and quality assurance.
3. PROCESS DEVELOPMENT SOLUTION AND DISCUSSION OF RESULTS

With the improved and enhanced process solution in stencil process is extensively resolved with the combination of print speed and print force parameter optimization. Fig. 3 shows the actual stencil printing process. With the combination of print speed and print force parameter optimization, no off-centered ball reject occurrence was seen in stencil printing process. Fig. 4 shares the actual unit with centered ball formation using the optimized parameter. The optimized parameter would finally have a good reliability test and a good solderability test because the solder ball is now already at the center of the ball pad. A 96 percent improvement in Fig. 5 was achieved for off-centered ball. Note that actual parts per million (PPM) level are intentionally not shown due to confidentiality.

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4. CONCLUSION AND RECOMMENDATIONS

Off-centered ball improvement was successful through complete stencil printing process optimization and characterization for advanced semiconductor leadframe package. Parameter optimization particularly in stencil print process with the combination of print speed and print force parameter were done in this type of new technology in semiconductor assembly manufacturing with the result of around 96 percent improvement on the off-centered ball occurrence reduction.

Process optimization plays an essential role to as early as product development and qualification. Learnings shared in this paper could be used for future works on similar semiconductor devices. Future experiments could include comprehensive and detailed reliability tests of the optimized product. Studies and works discussed in [10-12] are helpful in improving the manufacturability of semiconductor products through process optimization and design of experiments.

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COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Yeap LL. Meeting the assembly challenges in new semiconductor packaging trend. 34th IEEE/CPMT International Electronic Manufacturing Technology Symposium (IEMT). Malaysia. 2010;1-5.
2. Hwang J. Solder paste in electronics packaging: Technology and applications in surface mount, hybrid circuits, and components assembly. Ven Nostrand Reinhold, New York, USA; 1989.
3. Tan CE, et al. Challenges of ultimate ultra-fine pitch process with gold wire & copper wire in qfn packages. 36th International Electronics Manufacturing Technology Conference. Malaysia. 2014;1-5.
4. Saha S. Emerging business trends in the semiconductor industry. Proceedings of PICMET ’13: Technology Management in the IT-Driven Services (PICMET). USA. 2013;2744-2748.
5. Liu Y, et al. Trends of power electronic packaging and modeling. 10th Electronics Packaging Technology Conference. Singapore. 2008;1-11.
6. Geng H. Semiconductor manufacturing handbook. 2nd Ed. McGraw-Hill Education, USA; 2017.
7. Coombs C, Holden H. Printed circuits handbook. 7th Ed., McGraw-Hill Education, USA ; 2016.
8. Nenni D, McLellan P. Fabless: The transformation of the semiconductor industry. Create Space Independent Publishing Platform, USA; 2014.
9. Harper C. Electronic packaging and interconnection handbook. 4th ed. McGraw-Hill Education, USA; 2004.
10. Rodriguez R, Gomez FR. Pick and place process optimization for thin semiconductor packages. Journal of Engineering Research and Reports. 2019; 4(2):1-9.
11. Sumagpong Jr. A, Rada A. A systematic approach in optimizing critical processes of high density and high complexity new scalable device in MAT29 risk production using state-of-the-art platforms. Presented at the 22nd ASEMEP Technical Symposium, Philippines; 2012.
12. Gomez FR, Mangaoang Jr. T. Elimination of esd events and optimizing waterjet deflash process for reduction of leakage current failures on qfn-mr leadframe devices. Journal of Electrical Engineering, David Publishing Co. 2018;6(4):238-243.

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