Upgrade of the LHCb Vertex Locator

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ABSTRACT: The upgrade of the LHCb experiment, planned for 2018, will transform the entire readout to a trigger-less system operating at 40 MHz. All data reduction algorithms will be executed in a high-level software farm, with access to all event information. This will enable the detector to run at luminosities of $1–2 \times 10^{33}/\text{cm}^2/\text{s}$ and probe physics beyond the Standard Model in the heavy sector with unprecedented precision.

The upgraded VELO must be low mass, radiation hard and vacuum compatible. It must be capable of fast pattern recognition and track reconstruction and will be required to drive data to the outside world at speeds of up to $2.5 \text{Tbit/s}$. This challenge is being met with a new Vertex Locator (VELO) design based on hybrid pixel detectors positioned to within 5 mm of the LHC colliding beams. The sensors have $55 \times 55 \mu\text{m}$ square pixels and the VELOPix ASIC which is being developed for the readout is based on the Timepix/Medipix family of chips. The hottest ASIC will have to cope with pixel hit rates of up to 900 MHz.

The material budget will be optimised with the use of evaporative CO$_2$ coolant circulating in microchannels within a thin silicon substrate. Microchannel cooling brings many advantages: very efficient heat transfer with almost no temperature gradients across the module, no CTE mismatch with silicon components, and low material contribution. This is a breakthrough technology being developed for LHCb.

LHCb is also focussing effort on the construction of a lightweight foil to separate the primary and secondary LHC vacua, the development of high speed cables and radiation qualification of the module.

The 40 MHz readout will also bring significant conceptual changes to the way in which the upgrade trigger is operated. Work is in progress to incorporate momentum and impact parameter information into the trigger at the earliest possible stage, using the fast pattern recognition capabilities of the upgraded detector.

The current status of the VELO upgrade will be described together with a presentation of recent beam-test results.

KEYWORDS: Si microstrip and pad detectors; Particle tracking detectors (Solid-state detectors)
1 Introduction

The principal task of the VELO (Vertex Locator) is to enable LHCb to trigger on and reconstruct displaced vertices, as well as playing a significant role in the tracking. It must cover the full angular acceptance of the LHCb spectrometer. Due to the fact that it surrounds the interaction region the VELO adds partial information for tracks falling outside this acceptance, in particular in the backward direction. The currently installed VELO also includes two stations in the backward direction capable of 40 MHz readout. These “Pile-Up” stations provide information for the luminosity analyses and play a role in the first-level hardware trigger. The information from the VELO is critical to identify characteristic displaced vertices of heavy flavored particles, underpinning physics analyses within LHCb. At trigger level the VELO identifies tracks with high impact parameter and is the first handle to reduce the minimum bias rate. The offline performance of the VELO is equally important. The excellent secondary vertex resolution is vital to resolve $B^0_s$ meson oscillations and to allow time dependent CP violation analyses. The impact parameter resolution must remain precise at both trigger and offline stages even at the relatively low transverse momentum regimes of the daughter products of $b$- and $c$-hadrons, and the detector must be fully efficient in order to capture multi-body hadronic final states.

1.1 VELO overview

The currently installed VELO is manufactured with 84 single-sided radial (R) and azimuthal-angle ($\Phi$) measuring strip sensors operated in a secondary vacuum inside the LHC beam pipe. The R and $\Phi$ sensors are mounted on either side of a highly thermally conductive spine which also supports the readout hybrid, and the resulting double sided module is supported on a carbon fiber stand. The
modules are arranged perpendicularly to the beam along a length of about 1 m. Module cooling is provided by evaporative CO$_2$ circulating in stainless steel pipes embedded within aluminium pads which are clamped to the base of the module. The detector is divided into two moveable halves, allowing it to retract during LHC injection. The cabling between the modules and detector hood must be flexible enough to absorb these movements, which occur for every LHC fill. The modules are separated from the primary vacuum with a 300 $\mu$m thin aluminium foil (RF foil). In the beam pipe region the material is corrugated in such a manner as to reduce as much as possible the material traversed by particles before their first measured point. Additional corrugations are provided in order to allow the two sides of the VELO to close completely, ensuring full geometrical coverage. A small overlap is added for alignment purposes. For more details see [1].

1.2 VELO upgrade motivation and challenge

The upgraded VELO must maintain or improve its physics performance while delivering readout at 40 MHz in the operating conditions of the LHC and LHCb upgrade. This can only be achieved by a complete replacement of the silicon sensors and electronics. Following an externally refereed review the collaboration has chosen to install a detector based on hybrid pixel sensors. A new radiation hard ASIC, dubbed VELOPix, capable of coping with the data rates, is under development. The current VELO has around 1.5 interactions per bunch crossing and 50 ns bunch spacing, and for the upgraded VELO we will have in average 5.2 interactions per bunch crossing at 25 ns spacing. The upgraded VELO can easily overcome this thanks to the increased granularity and the pixel design. The module cooling design must be upgraded in order to protect the tip of the silicon from thermal runaway effects after significant irradiation, and to cope with the ASIC power dissipation. For this reason the upgrade cooling is integrated within the module, in contrast to the currently installed detector. The cooling is provided by evaporative CO$_2$ circulating within miniature channels etched into thin silicon substrates which form the backbone of the modules. The upgraded VELO reuses large parts of the current mechanical infrastructure, in particular the vacuum tank, and elements of the very successful mixed phase CO$_2$ cooling system.

The conceptual layout of the detector within the LHCb coordinate system is shown in figure 1. It is very similar to the current VELO layout, however the $z$ positions of the modules have been changed in order to reach similar acceptance given the smaller module size and smaller distance from the beam line to the first measured point on the sensor.

2 VELO upgrade

2.1 Sensors and radiation tolerance

One of the main drivers for the design of the upgrade VELO is the required radiation tolerance. The detectors will have to withstand a maximum hadron fluence of about $8 \times 10^{15}$ 1 MeV n$_{eq}$/cm$^2$ at the innermost tip of the sensors by the end of the experiment. A factor of 40 lower fluence is expected at the opposite side, i.e. at the outermost radius of about 4 cm from the interaction point. The combination of the very high maximum dose and the inhomogeneous irradiation are challenging for the detector design, leading to implementation of a radiation tolerant design. For instance via n-side readout to provide the high electric field region near the readout electrodes (pixel implants)
Figure 1. Schematic layout of the upgraded VELO.

after irradiation [2–5]. N-side readout can be realised on n-type (n-in-n) or p-type (n-in-p) silicon bulk with different solutions for the guard rings. The high fluence significantly reduces the signal due to the trapping of the charge carriers at radiation induced trapping centers. For the upgrade VELO it is intended to use 200 $\mu$m thick sensors as this thickness is the best compromise between the required maximum depletion voltage at the end of lifetime. Another sensor requirement is that it has to withstand the maximum operation voltage (1000 V) prior to irradiation.

2.2 Modules

A VELO pixel module contains twelve VeloPix ASICs, each featuring a matrix of $256 \times 256$ square pixels ($55 \mu$m per side), resulting in a sensitive area of $14.08 \times 14.08$ mm$^2$. Three chips are grouped in a row and bump bonded to a single sensor to form a tile. Subsequently four tiles are arranged in an “L” shape around the LHCb beam pipe, see figure 1.

Two silicon sensors are mounted on each side of the module, thus ensuring full coverage in the inner region, a reasonable balance of heat load for mechanical stability, and allowing for electrical connections to the innermost ASICs, see figure 2. The VeloPix ASICs have very slim edges along three sides, and the sensors are fully efficient within the guard ring (GR) area by virtue of elongated pixel implants between the ASIC boundaries.

Two tiles are glued on each side of the module substrate. The tiles are mounted at right angles such that one tile is read out in the x-direction and the other in the y-direction. This results in the readout columns of the chips pointing towards the beam hole, instead of being laterally exposed. This configuration is chosen in order to obtain a lower maximal column hit occupancy and, as a consequence, a more uniform data rate in the columns. To avoid loss of angled tracks, the sensors on one side have to form an overlap with the sensors on the other side. This displacement amounts
Figure 2. Schematic cross section and top view of a module with sensors, VELOPix chips, microchannel substrate, hybrids and bond wires (not to scale).

to two pixels (110 µm) and is determined by the thickness of the substrate (0.4 mm) and that of the ASICs (twice 0.2 mm).

2.3 ASIC

The readout of the pixel sensors is done by VELOPix ASICs which consist of a matrix of $256 \times 256$ pixels of $55 \times 55$ µm$^2$ each. The VELOPix is a binary pixel readout ASIC and features a data driven readout which means that every hit is time-stamped, labeled and immediately sent off chip. The VELOPix ASIC is based on the Timepix3 ASIC [6], and is also base on the IBM 130 nm CMOS process.

Many tracks give rise to clusters with a size of more than one pixel, so it is beneficial in terms of bandwidth to pack the hits into so-called super-pixels $2 \times 4$ with fixed boundaries. Given the average number of hits in a cluster of 2.2, the packing will reduce the amount of data to be transmitted by 30%, since the redundant timestamp and (pixel) address information are removed.

Because the VELO modules are placed perpendicularly to the beam, the occupancy from ASIC to ASIC varies by almost a factor 10. This effect is shown in figure 3. An average number of 8.5 tracks per bunch crossing, gives rise to an average (peak) pixel hit rate of about 600 (900) million per second. Due to the packing of hits in super-pixel packets the number of packets is smaller than the number of pixel hits, and amounts to a peak of 520 million per second. The total power budget of the ASIC is 3 W, of which about 30% is used by the analog front-end, another 30% by the digital logic, and the remaining 40% is reserved for the high speed serializers. ASICs designed in this 130 nm technology have been shown to be fully operational after a radiation dose of 400 MRad [7].
2.4 Data acquisition

The data acquisition link consists of the following parts. First the signal transfer via the copper flexible cables between module and the vacuum flange at a distance of up to 80 cm. The differential pairs are implemented as edge-coupled strip lines, with characteristic impedance close to 100Ω. The optical to electrical conversion is done outside the vacuum tank. Specially designed flexible cable provides the vacuum feed-through. It will have connectors on both ends to connect to the data readout cables to the Opto&Power Boards. Each silicon module with 12 VeloPix ASICs requires 20–22 optical fibers to send its data to the DAQ boards located at a distance of about 300 meters, see figure 4. Each DAQ board performs the packet receiving, time ordering, event buffering and packet decoding. And finally data from several LHC bunch crossings are packed into Ethernet packets and sent via (up to twelve) 10 Gigabit Ethernet links to a large CPU farm. The only software trigger is used in data acquisition. The data flow from the whole VELO is up to 2.5 Terabits. The full-scale prototype module with electronics and cooling system will be ready to test approximately in early 2016.

2.5 Microchannel cooling

The idea of passing cooling liquid through miniature channels etched within a silicon wafer is not new, and many applications exist [8]. The principle of microchannel cooling is to etch trenches into the surface of a silicon wafer, then atomic bond a cover wafer with suitable exit and entry holes such that liquid can circulate through the capillaries. To fabricate such a microsystem many steps are involved, including photolithography, etching, chemical mechanical polishing, bonding and dicing. The substrates may be silicon, plastic, or glass. For the VELO upgrade application both wafers in the final module are silicon. The trenches are etched to be 120 µm deep in a 260 µm thick wafer, such that when the 140 µm thick cover wafer is bonded the channels sit symmetrically within the 400 µm thick cooling substrate. A schematic diagram of the silicon cooling substrate with the routing of the microchannels is shown in figure 5. The key advantage of a silicon cooling substrate is that there is no difference in the coefficient of thermal expansion (CTE), because the sensor, readout ASIC and cooling substrate are all silicon. The worst case total power of a module

![Figure 3](image-url). Data rate per ASIC in Gbit/s for the most active module. The readout direction is indicated by arrows.
Figure 4. Schematic picture of the VELO electronics. Each opto and power board will serve the two front-end hybrids located at opposite sides of one detector module. The two hybrids are electrically identical but geometrically different due to the asymmetric shape of the module. The granularity of the off-detector electronics is not correctly represented in the figure.

is calculated to be 43 W. The heat dissipation due to the use of the VELOPix ASICs may lead to the temperature difference greater than the temperature difference between the innermost and outermost tips of the module at maximum luminosity. The proposed cooling system has to be fully operable with both sources of heat.

Figure 5. Microchannel layout for one module.

The initial tests have been performed for the VELO cooling prototypes [9]. To stress-test microchannels, a laboratory system has been established to automatically cycle temperature and/or pressure. The pressure is supplied by a bottle of compressed air and the gas is heated by a Peltier unit with a glycol-based heat exchanger. A highest pressure of 170–190 bar is possible at tempera-
tures in the range -40 to 40°C. Two Si-Si samples have been tested in this setup over a two-month period during which they survived over a 1000 temperature cycles (each lasting 800 seconds), and several thousand pressure cycles from zero to ~180 bar at room temperature. These endurance tests are considered important milestones in validating the inherent long-term practical reliability of silicon microchannels.

2.6 RF box

The foils must satisfy a number of conditions for the LHC: they must provide good vacuum conditions in the presence of beam; electrical continuity along the beam direction and not significantly contribute to the impedance of the machine. The experimental requirements are to bring the foil as close to the beam as possible and to reduce its thickness to a minimum. The RF foils can be described as large rectangular boxes (∼1 m × 0.2 m × 0.4 m) with one of the two long faces removed and where the opposite face, which mates closely with the other detector half, has a complex corrugated structure. The boxes must be constructed with tight tolerances to allow the two detector halves to come together and also withstand differential pressure between -2 and +5 mbar. They must also withstand radiation doses of up to 1000 MRad in the regions closest to the interaction point. The requirement to place the sensors as close to the beam as possible means they will be, by necessity, in close proximity to the box. For the upgrade it is proposed to produce the box by milling a solid block of aluminum-magnesium alloy. First the outside profile is milled which is subsequently placed in a mold and evacuated, after which the inside is milled. The milling process offers clear advantages. The shape that is produced is cut at room temperature and can be measured during production using an instrumented arm on the milling machine, obviating some of the problems associated with hot gas forming. Perhaps more importantly the need to weld the sides of the box to the flange is entirely eliminated, as the flange and four sides may be cut from a block also. Small prototypes of the foil have been built. An example of a recent prototype is shown in figure 6. The milling process is such that it is difficult to reliably reduce the thickness of the aluminium to less than 250 µm over the full length of the box. As it remains highly desirable to further reduce the thickness, progress has been made on developing a chemical etching process using sodium hydroxide.

3 Summary

The LHCb VELO has been operating successfully during run-1 of the LHC. The VELO will continue to run with its current configuration in run-2 which will end in 2018. The experiment is actively working on the upgrade of the detector, to be installed and started in 2018–2019, which allows to run at a 5 times higher instantaneous luminosity. The first-level hardware trigger will be replaced by a pure software trigger, and the complete detector will be read out at every bunch crossing of 25 ns. The VELO will be replaced by a pixel based detector that is read out by the VeloPix ASICs which have a data output bandwidth in the order of 15 Gbit/s. The silicon modules will be cooled using microchannels etched in a silicon substrate. Successful results have been obtained both on the thermal performance tests and the pressure tests. Further challenges are in the production of the RF box by milling it out of a solid aluminium block, followed by local thinning.
Figure 6. (left) A photograph of an aluminium block being milled. (right) The finished prototype with a length of about 25% (~30 cm) of the final RF-box. The side walls are approximately 500 µm thick, the corrugated top section is approximately 300 µm thick.

by means of etching. The progress of VELO upgrade is going successfully and mostly on schedule. Details of the VELO upgrade can be found in the technical design report that was recently published [10].

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