All-Digital FPGA-based DAC with None or Few External Components

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Abstract—One of the many limitations with the mixed-signal design is physically testing circuit ideas. While it is easier to test digital circuits with FPGAs, this cannot be done usually with mixed-signal circuits. Although some FPGAs have built-in analog-to-digital and digital-to-analog converters, regular commercial FPGAs development boards and low-cost FPGAs lack built-in data converters. Here we introduce an all-digital FPGA-based DAC, which is one of the main blocks to enable mixed-signal experiments. The DAC can be synthesized entirely in an FPGA and does not require the use of external components. Furthermore, and to extend its range of applications, a discussion regarding the proposed DAC’s problems and possible solutions is presented. Experimental demonstration of a 4-bit and a 5-bit DAC corroborate the theoretical analysis developed in this work. This work also suggests a scheme which includes few external resistors to improve the linearity (DNL ≤ 0.25 LSB and an INL ≤ 0.5 LSB), and the power consumption (5X improvement over the standalone configuration).

Index Terms—FPGA-based DAC, all-digital, analog, mixed-signal, GPIO.

I. INTRODUCTION

One of the main disadvantages of mixed-signal circuits, in comparison with all-digital systems, is the complex design process involved and the many different ways to implement this design. In particular, there is not a simple way to physically construct a proof-of-concept of a mixed-signal system. On the digital counterpart, this can be done easily by synthesizing the digital description in an FPGA. To test mixed-signal circuits ideas and implementations, it is necessary to either construct a discrete circuitry, possibly with an FPGA for the digital part and commercially available integrated circuits (IC) or to fabricate an IC, which is neither a simple nor a cheap process. Many of the signal processing within mixed-signal systems is done in the digital domain, and use analog-to-digital (ADC) and digital-to-analog (DAC) converters to interact with the analog part of the system. Some FPGAs already include internal ADCs and DACs [1]. These FPGAs might be used to test mixed-signal circuits directly. The problem is that standard and low-cost FPGAs do not have internal converters [2], hence limiting their use to digital implementations only. There are also field-programmable analog arrays (FPAs) [3], as well as programmable system-on-chip (PSoC) [4] in the market, which would be the analog counterpart of the FPGAs, but their elevated prices (mainly the FPAs), and their lack of versatility, make these solutions unsuitable for many applications. With the latter in mind, this work is focused on the implementation of an FPGA-based digital-to-analog converter that might be described using an HDL language for synthesis.

There are several ways to implement an FPGA-based DAC: single-bit stream DACs (e.g., PWM and ∆Σ) [5], and multi-bit DACs (e.g., binary-weighted DAC, R-2R DAC) [6]. To the authors’ knowledge, all of the existing FPGA-based DAC implementations need external components. In fact, all multi-bit DACs base their operation on a mixed-signal approach where the FPGA implementation is the control unit used to switch on or off external components. The single-bit counterparts are closer to be called a true FPGA-based DAC implementation, but still, they need external components to filter high-frequency harmonics in order to obtain a proper digital-to-analog conversion [7]. Furthermore, the single-bit implementations usually limit their application to low-frequency operation (as a difference to the multi-bit approach).

This work proposes an FPGA-based DAC completely synthesized and instantiated in a generic FPGA without requiring additional external components. The proposed DAC is a multi-bit implementation whose sampling rate is mainly limited by the FPGA’s GPIO (general purpose input/output) dynamic characteristics. The latter allows its usage in a broader frequency range than other FPGA-based DACs. Furthermore, to expand the DAC’s application to other uses, the problems and non-idealities of the proposed DAC, as well as possible solutions involving the inclusion of few external resistors, are discussed.

II. PROPOSED FPGA-BASED DAC

The FPGA-based DAC is an application of the inverter-based DAC principle [8]. A voltage DAC can be developed by shorting the output of several inverters, as seen in Fig. 1. In a binary-weighted configuration, the less significant bit (LSB) controls one inverter, while the most significant bit (MSB) controls 2^N−1 inverters in parallel, with N being the number of bits.

The PMOS and NMOS transistors of the inverter will be seen as switches with an associated on-resistance. The output voltage can be calculated as:

\[ V_{DAC}(m) = \frac{(D_{\text{max}} - D_m)g_{op}}{(D_{\text{max}} - D_m)g_{op} + D_mg_{on}} \cdot V_{DD} \]  

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Fig. 1: Inverter-based DAC principle. In an ideal case, the DAC behaves like a resistor-DAC voltage divider.

where \( g_{op} = 1/r_{op} \) and \( g_{on} = 1/r_{on} \) are the on-transconductance values of the PMOS and NMOS transistors, respectively. \( D_{\text{max}} \) is the maximum number of levels of the DAC (\( 2^N - 1 \)), and \( D_m \) is the decimal equivalent of the binary word \( (b_{N-1} \ldots b_1 b_0) \) to be converted from digital to analog.

If both transistors are assumed to have the same on-resistance\(^1\) and this on-resistance do not depend on the voltage across it, the ideal DAC voltage can be obtained as:

\[
V_{DAC}(m) = \frac{D_{\text{max}} - D_m}{D_{\text{max}}} \cdot V_{DD} \tag{2}
\]

From equation (2), and Fig. 1 it is clear that the inverter-based DAC behaves like a conventional resistor divider DAC, in the ideal case. Notice that regarding the digital representation with inverters, the DAC voltage is inverted.

Fig. 2 shows the proposed FPGA-based DAC without external components. The basic idea is to use the GPIOs of the FPGA in the same fashion as the inverters in the DAC of Fig. 1. The proposed scheme shorts the outputs of the GPIOs in order to apply the inverter-based DAC principle. Although we introduce here a new approach to implement an FPGA-based DAC, the idea extends to any device where GPIOs are available, for example, in a microcontroller like the ones used in popular developing boards, such as Arduino, or small single-board computers, like the Raspberry-Pi family.

A general GPIO scheme is shown in Fig. 2 as well. For the implementation, the output buffers of the GPIOs are enabled, while the input buffer, as well as the pull-up and pull-down resistors, are disabled\(^2\). Since the output buffer of the GPIO is conformed by two inverters in cascade, the output of the DAC is no longer inverted, and the ideal DAC voltage is no longer given by equation (2), but:

\[
V_{DAC}(m) = \frac{D_m}{D_{\text{max}}} \cdot V_{DD} \tag{3}
\]

In contrast with other FPGA-based DACs, this implementation does not need the use of any external component. Furthermore, since the configurable GPIO output buffers’ strength dictates the maximum frequency, the proposed scheme might achieve higher frequency operation in comparison to other FPGA-based DACs.

A. Problems and non-idealities

Even though the FPGA-based DAC implementation has certain advantages, it has some practical issues. The first one being the power consumption. Since the output buffer of a GPIO is designed to handle relative large capacitive loads (>50pF) while maintaining appropriate frequencies, the output current of a GPIO is usually significant (>10mA) when transitioning from high-to-low, or vice-versa. Taking into account Fig. 1, the latter translates to have low on-resistance values. By shorting outputs of the GPIOs, we placed a direct path from the supply voltage to ground through the inverter chain. Hence, the FPGA-based DAC consumes high-static current values, which finds its peak at DAC’s output mid-range. The current consumption doubles for each bit of resolution added to the DAC, making it only practical for lower resolution implementations (<6-bits). Although some GPIOs also have the capability of adjusting their output strength, still the amount of static-current is considerable.

The other problem is the DAC’s linearity. In the ideal inverter case, the on-resistance of the PMOS and NMOS transistors are the same. Although this may be true, the on-resistances are equal only for a small region of the transfer function. To understand how the DAC’s transfer function behaves, one has to remember that, in reality, the devices used for the construction of the FPGA-based DAC are not resistors, but transistors, which have a non-linear behavior. From equation (1), and without the assumption that the on-

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\(^1\)It is common practice to design inverters to have similar dynamic characteristics for high-to-low and low-to-high voltage transitions.

\(^2\)One may think that the pull-up and pull-down resistors could be used as an ideal resistor DAC. Unfortunately, their enable pins can not be controlled through internal FPGA’s signals, but are hard-configured when synthesizing the circuit in the FPGA. Furthermore, not all FPGAs have both pull-up and pull-down resistors, but just one of them.
Voltage $[V]$ Current $[A]$ Voltage $[V]$

| $V_{\text{Vdd}}$ | $V_{\text{sdp}}$ | $V_{\text{dsn}}$ | $V_{\text{ov(n,p)}}$ | $V_{\text{DD}} - V_{\text{thn}}$ | $|V_{\text{thp}}|$ |

PMOS and NMOS transistors in triode region.

The latter translates to two equivalencies: that their threshold voltages for the whole digital input range.

To simplify the analysis, and as already mentioned, the following discussion will be based on the assumption that the PMOS and NMOS transistors have equivalent static and dynamic characteristics. In the Verilog-A model simplest form, the latter translates to two equivalencies: that their threshold voltages are equal in magnitude ($V_{th} = V_{thn} = |V_{thp}|$), and that their transconductance parameters are equal as well ($\mu_p C_{oz}(W/L)_p = \mu_n C_{oz}(W/L)_n$). With this in mind, Fig. 3 depicts the behavioral simulation results for illustration purposes.

When the digital input code is in the low-end of its range, the DAC will have more NMOS active transistors than PMOS active transistors, which will pull-down the output voltage $V_{DAC}$. At this point, $V_{DAC}$ (NMOS drain-source voltage $V_{dsn}$) is lower than the transistors’ overdrive voltage ($V_{ac}=V_{own}=V_{vpp}$, which is constant across the input range and equals to $V_{DD} - V_{thn}$), the NMOS transistors will be in the triode region (see the middle curve of Fig. 3). Since the source-drain PMOS voltage behavior is complementary to the NMOS one ($V_{sdp}=V_{DD} - V_{DAC}$), the PMOS transistors are in saturation ($V_{sdp}>V_{thn}$). When increasing the number of PMOS active transistors (while proportionally reducing the number of NMOS transistors connected), the $V_{DAC}$ output voltage increases to the point where the PMOS are no longer in saturation. In this region, the NMOS and PMOS transistors are in triode. It is in the triode region where their on-transconductances behave in a similar fashion, hence, it is the most linear region in the transfer function, as it can be appreciated in Fig. 3 (top). Finally, $V_{DAC}$ continues its rise, entering the region where the NMOS transistors are in saturation, while the PMOS transistors are in triode.

Even though power consumption limits the maximum number of bits that can be used, and that this DAC is not the most linear one, the FPGA-based DAC may be used in many applications. Examples of these applications are: those where linearity is not an inconvenient, but a desired feature; in feedback loop systems; to test ideas where analog circuits are implemented with digital cells, i.e., digital low-drop-out regulators implementations; in general, when using FPGAs that does not have internal DACs. Furthermore, the DAC’s output can be characterized and corrected digitally, or its non-linearity behavior could be taken into account in the systems transfer function.

In any case, and if the application requires it, a simple method to linearize the DAC’s output, while solving the power consumption problem in the process, is presented in the following section.

B. Linearity correction and current reduction

With the qualitative description of the previous section, the non-linear behavior of the DAC’s transfer function can be understood. It is important to identify what are the conditions to be in the linear region, in order to apply the necessary corrections. There are two ways of looking at these conditions for linearity. The first one was already discussed in the previous section, and it is the most evident from Fig. 3 (top), as well as a consequence from equation (4) and the relative error factor $\epsilon$ of the on-transconductances: if both transistors are in the triode region, they will behave so similar that $\epsilon \approx 0$, hence, the DAC’s output would approximate to its ideal value. The second way to look at this is to see the cumulative current behavior in Fig. 3 (bottom). In the linear region, the current of the DAC is almost constant but decays the closer it gets to the digital input range edges.

Then, to improve the DAC’s linearity, it is necessary to stretch the triode-triode region condition through the entire digital input range, or/and making the DAC’s current constant throughout the whole range. This can be done with the general configuration of Fig. 4. Two configurations will be analyzed: resistors in parallel only (two resistors, with $r_{sdp} = 0$), and the general configuration including the series resistors (four resistors).

The two resistor configuration improves the linearity by including two external resistors, one between $V_{DD}$ and $V_{DAC}$ ($r_{pp}$), and the other between $V_{DAC}$ and ground ($r_{pn}$). The inclusion of the parallel resistors creates additional current paths than those of the main ones (through the GPIOs). To see the parallel resistor effect, let’s take into consideration the
PMOS transistors with the resistor $r_{pp}$. The $r_{pp}$ path (in a certain way) complements the main path, such that the sum of their currents is almost constant (which depends on the $r_{pp}$ resistance value), as it can be appreciated in Fig. 5 (bottom). In this way, when there are fewer PMOS active transistors, the remaining current flows through the additional path created by the additional $r_{pp}$. The same happens between the NMOS transistors and the resistor $r_{pn}$.

From another point of view, the triode-triode region stretches out by connecting the parallel resistors. By adding the two parallel resistors to the expression in (4), one can obtain:

$$V_{DAC}(m) = \frac{D_m + g_{pp}/g_{op}}{D_{max} - D_m \cdot \epsilon + (g_{pp} + g_{nn})/g_{op}} \cdot V_{DD},$$

(5)

where $g_{p[n]} = 1/r_{p[n]}$. Assuming that the parallel resistors have the same value ($r_{pp} = r_{pn}$), and that in the linear region the on-transconductances of the GPIOs’ NMOS and PMOS transistors are approximately the same ($g_{op} \approx g_{on}$, or

$$\epsilon \approx 0,$$

then:

$$V_{DAC}(m) \approx \frac{D_m + \alpha_g}{D_{max} + 2\alpha_g} \cdot V_{DD},$$

(6)

where $\alpha_g = g_{p[n]}/g_{o[p,n]}$. With the previous equation, it is clear that by selecting the proper $\alpha_g$ value, the linear region can be stretched out to the entire digital input range, or in other words, it can be stretched out from $D_m = 0$ by setting $V_{DAC} = |V_{thp}|$, to $D_m = D_{max}$ by setting $V_{DAC} = V_{DD} - V_{thn}$. With the latter, it is easy to estimate the relation between the parallel resistance value and the transistors’ on-resistance as:

$$\alpha_g = \frac{r_{o[p,n]}}{r_{p[n]}} \approx 1 \cdot \frac{DD}{V_{DD} - 2V_{th}}$$

(7)

All necessary variables in the previous equation can be found experimentally when obtaining the DAC’s transfer function. For example, the $V_{DD} - 2V_{th}$ is the linear’s region dynamic range (see the top plot in Fig. 5, from which the transistors’ threshold voltage $V_{th}$ can be derived (knowing the supply voltage $V_{DD}$), while the on-resistance value can be derived by measuring the current ($I_{o[p,n]}$) through one GPIO at the input’s mid-range.

The two resistor configuration for linearity correction is easy enough to implement since only two external resistors are needed. Not complicated schemes are applied to obtain a more linear transfer function. The relevant issue is its implementation practicality. Fig. 5 summarizes that by adding resistors in parallel, the total current consumption of the system is larger (almost as twice than without the correction). This is even more detrimental when increasing the number of bits of the DAC’s implementation. Besides, the dynamic range of the DAC decreases, which might be no critical depending on the application. It is important to emphasize that the number of bits holds throughout a lower dynamic range, which translates to a higher resolution DAC.
Up to now, the discussion regarding the linearity has focused on the condition that the NMOS and PMOS transistors should be in the triode-triode region. In reality, the conclusion from equation (4) is not that both have to be in the triode region, but both have to behave, if not the same, as similar as possible. In fact, better linear performance could be obtained if the transistors are in saturation since they will be almost independent of the drain-source voltage. With the configurations that have been analyzed until now, a region where both group of transistors could be in saturation at the same time is not possible, since their gate and source voltages are always the same ($V_{gsn} = V_{sgp} = V_{DD}$). This is no longer the case if the general four resistor configuration of Fig. 4 is considered.

First, the effect of the series resistors will be analyzed. By adding these resistors, the $V_d$ and $V_s$ voltages (Fig. 4) can be modified, which changes the gate-source absolute voltages ($V_{gsn} = V_{sgp} = V_{DD} - V_s$). Hence, the overdrive voltage ($V_{ov} = V_{gsn} - V_{thn} = V_{sgp} - |V_{thp}|$) is changed as shown in Fig. 6 (left-center), reducing it at mid-range. By increasing the series resistance value, it is possible to find a region where both transistor groups are in saturation ($V_{dsn} \geq V_{ov}$ and $V_{sdp} \geq V_{ov}$), as it is illustrated in Fig. 6 (left). Furthermore, and as expected, the addition of the series resistors had the advantage of decreasing the current consumption as shown in Fig. 6 (left-bottom).

Finally, by adding the parallel resistors, the circuit will experience the same effect as with the two resistors configuration, but the region to be stretched out is the saturation-saturation region, as shown in Fig. 6 (right). Although the results are similar to the two resistor configuration, three differences can be noticed. The first one is that the four resistor configuration seems to have a linearity improvement, which can be explained by both group of transistors being in the saturation region rather than in triode, as commented before. The second one is that the dynamic range is somehow lower for the four resistor configuration. The dynamic range is heavily dependent on the transistors’ threshold voltage: for the two resistor configuration, the lower the $V_{th}$ the better, while for the four resistor configuration is all the way around. The final difference is the total current of the system. Values as 10X lower than the standalone (no resistors) or two resistor configurations can be obtained. In turn, the series-parallel configuration is slower than the other two, as expected.

Now, to find the resistors’ values, the circuit in Fig. 4 (right) will be analyzed such that the transistors are in strong inversion ($V_{gsn} \geq V_{thn}$ and $V_{sgp} \geq |V_{thp}|$) and saturation condition ($V_{dsn} \geq V_{ov}$ and $V_{sdp} \geq V_{ov}$). With the latter in mind, the following inequalities can be found:

$$V_{DD} - I_T \cdot (r_{sp} + r_{sn}) \geq |V_{th\{n,p\}}|$$

$$V_{DD} - I_T \cdot r_{sp} - V_{thn} \leq V_{DAC} \leq I_T \cdot r_{sn} + |V_{thp}|$$  \hspace{1cm} (8)

Two things can be derived from the previous inequalities: the maximum and minimum values of the DAC’s output ($V_{DAC_{max}}$ and $V_{DAC_{min}}$), and the limits of the total current $I_T$ (supposing $V_{th} = V_{thn} = |V_{thp}|$):

$$\frac{V_{DD} - 2V_{th}}{r_{sp} + r_{sn}} \leq I_T \leq \frac{V_{DD} - V_{th}}{r_{sp} + r_{sn}}$$  \hspace{1cm} (9)

The latter inequality can be used to find the series resistors’ values if a total current specification is set and if both resistors are assumed to have the same value for symmetry. Finally, to find the parallel resistors’ values, the circuit in Fig. 4 (right) is solved to obtain the following pair of equations:

$$V_{DAC} = V_{DD} - I_T \cdot (r_{sp} + r_{sn}) + I_p \cdot r_pp$$  \hspace{1cm} (10)

$$V_{DAC} = I_T \cdot (r_{sp} + r_{sn}) - I_n \cdot r_pnn$$  \hspace{1cm} (11)

where $I_p = D_m \cdot I_{sp}$ and $I_n = (D_{max} - D_m) \cdot I_{dsn}$, as stated in Fig. 4. Replacing $V_{DAC_{min}}$ and $D_m = 0$ in equation (10), and $V_{DAC_{max}}$ and $D_m = D_{max}$ in equation (11), the parallel resistors’ values can be found as:

$$r_{p\{p,n\}} = \frac{|V_{th\{n,p\}}|}{I_T}$$  \hspace{1cm} (12)

All the variables needed to find the solutions to equation (8) and equation (12) can be obtained experimentally.

In this section, it has been shown to be theoretically possible to obtain an FPGA-based DAC without any external components. Far from perfect, current and linearity are the two major drawbacks of the standalone implementation. Still, the DAC could be used for several applications. In any case, two different configurations were proposed to solve such problems by only adding a few external resistors, obtaining interesting results which will be verified in the following (experimental) section.

### III. Experimental results

This section presents the measurement results performed to validate the theoretical foundation described in the previous section. For this, a testbench using the icoboard v1.1, which contains a Lattice FPGA, 100MHz max clock, up to 8 MBit of SRAM, up-to 206 GPIOs, and it is programmable in Verilog by a complete open-source FPGA toolchain (consisting of Yosys and ArachnePnR and icetools) \(^2\). The icoboard is programmed and powered through a Raspberry Pi 3 model B.\(^5\) The complete setup can be seen in Fig. 7.

The following measurements were performed by implementing a 4-bit DAC standalone configuration. Fifteen GPIO outputs were shorted-out as in Fig. 2. To see the DAC’s output in an oscilloscope, a low-frequency periodical stair-case was programmed in the FPGA, and the results are shown in Fig. 8a. The transfer function goes from 0V to 3.3V ($V_{DD}$), and the sampling period was set to $\sim$500µs. As explained in section II-A, the FPGA-based DAC’s output has two non-linear regions and a (quasi) linear region at mid-range, which are shown in the figure. The linear region has a dynamic range 3

\(^5\)Although the concept could have been implemented directly over the Raspberry Pi board, it is simpler to test the concept in an FPGA due to its versatility.
of \sim 1\,V, which in reality could be greater, but since the number of steps in this region is limited to two digital codes, the dynamic range measurement is not the most accurate.

The DAC’s total current was measured as well and presented in Fig. 8. The current consumption peak occurs at mid-range, and it is approximately 300mA, which would give \sim 40mA per GPIO. A 5-bit DAC configuration was still possible, which would consume almost as twice the current (\sim 600mA), but it would have been a problem when trying to implement the two configurations for linearity correction, which would have consumed around four times the current of a standalone 4-bit implementation (\sim 1.2A). Also, it should be noted that the maximum DC current that a single GPIO can drive is rated at 24mA \cite{12}. Hence, the standalone configuration is limited at low frequencies by this maximum.

We extract the variables needed for the equations shown in section II-B from Fig. 8. For instance, the transistors’ threshold voltage can be derived from the linear region’s dynamic range, which would be \( V_{DD} - 2V_{th} \approx 1\,V \). Knowing that the supply voltage is 3.3V, the threshold voltage would be \sim 1.15V (as stated before, the linear region’s dynamic range could be higher, hence \( V_{th} \leq 1.15V \)). Another important variable is the transistors’ on-resistance value. It is possible to obtain this value from Fig. 8, within the linear region. The on-resistance value is calculated to be \( r_{o(p,n)} \approx 40\Omega \).

On the other hand, the maximum frequency is limited by the GPIO’s dynamic performance, e.g., rising and falling times. Fig. 8(a) shows the result for a sampling rate of 20MS/s of a binary DAC implementation. As it can be seen, this result describes a non-monotonic behavior at abrupt bit changes. To avoid the non-monotonicity, a thermometer implementation can be used, as shown in Fig. 8(b). Higher sampling rates can be obtained according to the measured high-to-low transition time (\sim 30ns). The transition time of the standalone DAC is the same as the measured transition time of a single GPIO under normal FPGA operation. The latter may lead to the conclusion that the dynamics characteristics of the DAC is dominated by that of the GPIO, but the dynamic measurements for this setup are heavily dependent on the oscilloscope’s probe load, which is around 85pF-120pF. It is expected to have faster responses in scenarios where the GPIOs are not as heavily loaded. In any case, the possibility to go as fast as the GPIO’s dynamic capabilities is definitely one of the advantages of the proposed FPGA-based DAC compared to other multi-bit implementations.

In section II-B, configurations were proposed to correct the non-linearity behavior. For this, two to four external resistors

![Fig. 7: Measurement setup used to validate the FPGA-based concept. An icoBoard v1.1 was programmed and powered through a Raspberry Pi 3 model B.](image1)

![Fig. 8: Measurement results for a 4-bit FPGA-based DAC implementation.](image2)

![Fig. 9: Measurements for a 4-bit DAC at higher frequencies: (a) binary implementation, (b) thermometer implementation.](image3)
are needed. Fig. 10 shows the results of 4-bit DAC when using the two resistor configuration \( r_{pp} \) and \( r_{pn} \) as shown in Fig. 4 (right). From equation (7), it is possible to calculate the parallel resistance value that is needed with the \( V_{th} \) and \( r_\alpha(p,n) \) values calculated before. The latter gives a resistance of \( \sim 2.3 \Omega \). In the implementation, 2.35\( \Omega \) resistors were used. As it can be seen, the linear region, where the PMOS and NMOS transistors are triode region, is completely stretched out to the entire input range. The linearity improvement is notorious, but to quantify it, Fig. 10(b) shows the differential non-linearity (DNL) and integral non-linearity (INL) comparison between the standalone and two resistors configurations. While the standalone DAC has a DNL \( \leq 1.5 \) LSB and an INL \( \leq 2 \) LSB, the two resistors configuration has a DNL \( \leq 0.5 \) LSB and an INL \( \leq 0.5 \) LSB.

Knowing that the parallel resistance value is 2.35\( \Omega \), at mid-range the current through the resistor is \( \sim 700 \) mA, while the current through the transistors at mid-range is \( \sim 300 \) mA, giving the round total of \( \sim 1.0 \) A, which will be almost constant in the entire input range, as described in section II-B. This is more than three times the current in the standalone configuration, which is a problem that could be even worse for higher resolution implementations.

To solve the current consumption problem, a more general four resistor configuration was proposed. For a practical implementation, several things must be considered. For example, it is common that the GPIO banks do not have independent grounds, but the entire FPGA shares the same ground. For the particular setup case, the ground plane of the icoBoard does not allow the inclusion of the \( r_{sn} \) of Fig. 4 (right), hence \( r_{sn} = 0 \) \( \Omega \). On the other hand, although each GPIO bank has its independent supply voltage (\( V_{DDIO} \) in Fig. 2), the icoBoard has a single supply plane. To include \( r_{sp} \), a cut was done

\[ \text{CH1: } 500 \mu \text{V/div M 500\mu s/div w/o Correction} \]

\[ r_{pp}=r_{pn}=2.35 \Omega \quad r_{sp}=0.0 \Omega \]

\[ 1.0 \text{V} \]

\[ \text{Quasi-Linear Region PMOS and NMOS transistors in triode region} \]

\[ \text{(a) DAC's output for the two resistor configuration.} \]

\[ \text{(b) Measured DNL (top) and INL (bottom) without external components (gray lines) and with parallel resistors (blue lines).} \]

\[ \text{Fig. 10: Measurements for a 4-bit DAC using parallel resistor correction only. The dynamic range is reduced, but the DAC is linear within the whole range.} \]

\[ \text{Fig. 11: Measurements for a 4-bit DAC using series and parallel resistors correction. The DAC is linear within the whole range while the total current is reduced x5 compared to the two resistor configuration.} \]
on the PCB immediately after the board’s regulator. To allow different series resistor’s values, a potentiometer was placed as the \( r_{sp} \).

Fig. 11a and Fig. 11b show the DAC’s output and current consumption, respectively. The 4-bit DAC uses a 10Ω series resistor and 5Ω parallel resistors for linearity correction, allowing 5X lower current than the parallel resistor configuration. Theoretically, lower currents can be achieved by using higher resistor values, but since all FPGA’s supply pins share the same voltage plane, when putting higher values the FPGA’s total current was very limited, causing the FPGA to reset. The impossibility to use higher resistors also limited the dynamic range, and only \( \sim 600 \)mV was achieved. Regarding a final application, a careful PCB design should keep the IO supply isolated from the FPGA core, as the chipmaker usually recommends it. With an IO supply isolated, it might be possible to withhold large voltage drops and, therefore, larger supply series resistors.

Fig. 11c shows the linearity measurement results comparing the standalone and the series-parallel resistors configuration. As expected, the linearity is improved with respect to the parallel resistors configuration, obtaining a DNL\( \leq 0.25 \)LSB and an INL\( \leq 0.5 \)LSB. Since there is some margin in regards to the linearity, it was decided to test several parallel resistors to improve the dynamic range as showed in Fig. 11c. For a better understanding, the measured DNL, INL, dynamic range, and maximum current are plotted against different parallel resistors values in Fig. 12. Although there is an improvement in the dynamic range, as well as a reduction in the current, the linearity is worsened considerably. In any case, the final result is more linear than the standalone configuration, hence depending on the application, placing larger resistors may be beneficial.

Finally, it should be noted that the proposed DAC is not limited to a 4-bits configuration. Theoretically, it is only limited by the number of GPIOs, but practically it is limited by the current, as well as other factors, like how the FPGA’s PCB has been laid out. To show higher resolution capabilities, a 5-bit implementation using the series-parallel resistors configuration was measured. The DAC’s output as well as its current are presented in Fig. 13. In a standalone configuration, the DAC’s maximum current was expected to be twice the current through the 4-bits standalone implementation, but since the series-parallel resistors configuration is used, the current is as low as \( \sim 222 \)mA. On the other hand, although the DAC’s linearity seems better than a standalone configuration, the best series-parallel resistor setup could not be tested due to higher currents involved which were putting on reset the FPGA.

![Fig. 12: Effect of parallel resistor value on the measured DNL, INL, dynamic range (DR) and total current (I_{T}) for a 4-bit DAC implementation with a 10Ω series resistor.](image1)

![Fig. 13: Measurements for a 5-bit DAC implementation using a series resistor of 9Ω and parallel resistors of 5Ω for linearity correction.](image2)

**IV. SUMMARY AND REMARKS**

In this work, we proposed an all-digital FPGA-based DAC. A general qualitative comparison between different FPGA-based DACs is summarized in Table I. The comparison is made with general characteristics of single-bit and other multi-bit DAC implementations. As mentioned throughout the text, the main contribution from the proposed DAC in the standalone configuration is that it does not need external components. As well, higher frequencies can be achieved than other implementations since the standalone proposed DAC depends mainly on the GPIO’s dynamic characteristics, while others are limited by the external components used, not to mention the latency added by the required implementation loops (e.g., \( \Delta \Sigma \)-DAC).

On the other hand, the standalone DAC implementation does not do very well in other metrics. In particular, the number of GPIOs required for the proposed implementation is the highest of all, which becomes its biggest disadvantage. It is also the worst in resolution, linearity, and power consumption, as it was shown in section III. Although these specifications are severely impacted by the external components used in other DAC implementations. For example, the R-2R DAC linearity will be as good as the accuracy of the resistors.
TABLE I: Qualitative comparison between FPGA-based DACs.

| External Components | Single-bit (PWM, ΔΣ) | Other Multi-bit (e.g., R-2R, etc.) | Proposed DAC (standalone) | Proposed DAC (with correction) |
|---------------------|-----------------------|-----------------------------------|---------------------------|--------------------------------|
| Frequency           | YES (-)               | YES (-)                           | NO (++)                   | YES (+)                        |
| Resolution          | LOW (-)               | HIGH (++)                         | HIGH (++), LOW (-)        | HIGH (- -), LOW (-)            |
| Linearity           | HIGH (++), MEDIUM (+) | LOW (-)                           | LOW (-), MEDIUM (+)       | HIGH (- -), MEDIUM (+)         |
| Power               | LOW (++), MEDIUM (+)  | HIGH (-)                          | HIGH (-), LOW (-)         | HIGH (- -), HIGH (-)           |
| Nr. GPIOs           |                       |                                   |                           |                                |

used for the implementation, which translates to more costs in the DAC implementation. On the other hand, the resolution, linearity, and power consumption of a PWM or ΔΣ-DAC depends on the filter used externally. For higher-resolution implementations, higher-order active filter architectures may be required, which increases the implementation costs, power consumption, and complexity.

To improve the DAC’s performance, an entire section was dedicated to discussing the problems and non-idealities of the proposed implementation. From the conclusions obtained, simple configurations were proposed to correct those problems. By including only two to four external resistors, the power consumption was reduced (5X lower), and the linearity was improved considerably (DNL ≤ 0.25LSB and INL ≤ 0.5LSB), at the expense of lower dynamic range. Although the dynamic range is reduced, the effective number of bits is maintained, which in turn improves the DAC’s resolution. Reducing the power consumption also allows the possibility to use more number of bits than those shown in this work (4-bits and 5-bits implementations were demonstrated), limited only by the number of GPIOs available in the FPGA.

To conclude, the fact that the proposed FPGA-based DAC does not need external components enables those FPGAs without internal DACs to be used in analog or mixed-signal systems. But if the application requires it, with the inclusion of few external resistors, better performance can be achieved in terms of power consumption, linearity, and resolution.

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