Numerical simulation of effective light transmission through a photonic memory cell

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Abstract. This paper is devoted to numerical simulation of a non-volatile photonic memory cell based on phase-change material Ge$_2$Sb$_2$Te$_5$. The parameters of light propagation are presented for both crystalline and amorphous Ge$_2$Sb$_2$Te$_5$ phases. The cell structure is optimized for a single TE-mode regime that is suitable for short- and long-distance communication lines.

1. Introduction

Nowadays growth of communication streams leads to increasing requirements for computing, storage, and transmitting devices [1,2]. Despite this fact, most computers are based on von Neumann architecture which has a separate central processing unit (CPU) and memory unit. Therefore, data has to transfer between the CPU and the memory unit in each calculation cycle. The memory unit often uses various types of storage devices for different purposes. Frequently used data temporarily keeps in fast volatile SRAM and DRAM and the remaining data is stored in slow non-volatile SSD and HDD. Different storage locations slow down data processing because of the relatively long transfer time. The proper way out of this situation is to use non-volatile storage devices [3] and the neural architecture [4]. Such devices may be based on a wide range of phase-change materials (PCM). PCM has been studied and used for a long time. For example, these materials have already been used in the field of memory devices on DVDs [5].

However, the use of PCM in the storage devices alone is not enough to overcome the growth of requirements, because well-known solutions to this problem by the microelectronics methods are...
reaching physical limits [6]. In the same time, silicon photonics offers several promising solutions [7-10].

This paper is devoted to optimization parameters of a non-volatile photonic memory cell with optical recording and readout based on phase-change material Ge$_2$Sb$_2$Te$_5$ (GST).

2. Operation principle and purpose
The photonic memory cell consists of a Si strip waveguide with a 10 nm thick GST layer on its top. The operation principle of the photonic memory cell is similar to PCM memory. It is well known that GST has amorphous and crystalline phase states that are both stable at room temperature and have different optical and electrical properties. Switching between these phase states is performed by heating. Usually, GST crystallization is considered an erasing operation, and amorphization after melting is considered a recording one. The difference between the photonic memory cell and PCM memory is in the heating source and reading operation. Indeed, PCM memory uses Joule heating and difference in electrical resistance of GST phase states while the photonic memory cell uses optical sources and difference in refractive indices.

Consider a photonic storage element. It is worth mentioning that GST has a 20 times larger imaginary part of the refractive index in the crystalline phase state than in the amorphous one. Consider that the GST layer is thin enough to be regarded as a slight nonuniformity for the waveguide mode and the waveguide is supposed to be ideal. In this case, all waveguide mode losses are due to internal absorption in GST. Consequently, there will be two different transmission levels of the signal which correspond to “0” and “1” in binary notation. Switching between them can be performed in different ways by changing the source of heating power. An all-optical configuration was chosen for the calculations. This means that data recording, erasing and reading is performed by laser pulses of different amplitude and duration [11]. Erasing signal consists of a sequence of pulses that have enough power to heat GST to the state near the melting point and have enough delay for the subsequent crystallization. Data recording operation is a short high-energy pulse that melts GST with a short delay for GST amorphization. The optical readout is performed for a low energy pulse which does not affect the GST phase. The goal of the present work is to find the best size ratio of the waveguide to provide a clear difference in the transmission levels of the photonic memory cell.

3. Results and discussion
To reach the goal, two stages of numerical calculations were performed. In the first stage 2D, calculations were carried out. The simulated structure had infinite size in the XY plane. The thickness of buried SiO$_2$ was selected 2 μm to ensure low losses to the substrate [12]. The distance from the waveguide side walls to the boundaries of the simulated area was set to 3 μm; the distance from the GST layer to the top boundary of the simulated area was 2 μm. An approximate Sommerfeld condition (1) was used for the case of plane waves:

\[ n(\Delta E_z) + ik_0E_z = 0 \]  

(1)

\[ \begin{array}{c}
\text{(a)} \\
\text{(b)} 
\end{array} \]

Figure 2. TE fundamental mode profile of the different structures: (a) a simple Si strip waveguide, (b) the photonic storage element with crystalline GST.
Figure 3. (a) Optical mode regime of the photonic storage element. Green and hollow dots correspond to amorphous and crystalline phase states. The yellow area corresponds to the “immune” regime. (b) The overlap between mode distributions of the photonic storage element and Si strip waveguide (the area inside the black outline). The light green area provides single TE-mode regime and the blue one corresponds to both TE and TM modes.

As a result, mode distributions of the photonic storage element were obtained for both GST phase states and various waveguide geometry. The resulting mode structure is very similar to the mode structure of a simple Si strip waveguide (figure 2a). It is worth mentioning that the difference between these two mode structures may be explained by Snell’s law. Indeed, a slight upward shift of the waveguide mode core appears due to a large difference between refractive indexes of crystalline GST and Si (figure 2b). Hence there is a lower critical angle of total internal reflection on the air-GST boundary than on the air-Si boundary. It means that fewer light rays will pass through the top border of the waveguide with the GST layer. Therefore, the waveguide mode exists in the photonic storage element if it satisfies the following condition for the simple Si strip waveguide:

\[ n_{\text{buried oxide}} < n_{\text{eff}} < n_{\text{core}} \]  

where \( n_{\text{buried oxide}} \) is SiO\(_2\) refractive index and \( n_{\text{core}} \) is Si refractive index respectively. This allows finding a certain range of the waveguide width and height where single a TE-mode regime is insensitive (so-called “immune”) to switching GST phase state (figure 3a). Furthermore, it was determined that the lower limit of single the TE-mode regime for the crystalline GST phase may be approximated sufficiently accurate by the simple power functions (3):

\[ h = \alpha w^{-\beta} \]  

where \( w \) is the width of the waveguide, \( h \) is the total height of the waveguide with the GST layer, \( \alpha \) and \( \beta \) are real positive numbers. However, light generally enters the photonic memory cell through a Si strip waveguide and its mode distribution should also be taken into account. The overlap between the “immune” regime and the single TE-mode regime of the Si strip waveguide guarantees the single TE-mode regime in the entire photonic memory cell (figure 3b). Also, this overlap eliminates the losses caused by the appearance of TM-mode and its leakage at the end of the GST layer.

Single TE-mode regime provides propagation of only the fundamental TE mode and the rest of the modes, in this case, are unstable due to the limited size of the waveguide structure. The choice of this regime is explained by the following facts. Firstly, many silicon photonics devices are polarization-sensitive (e.g., MMI, MZI, DC, PhC/Grating, AWG, MRR) [13] and the single TE-mode regime prevents the appearance of parasite high-order modes by definition. Therefore, this regime may be useful for the development of silicon photonics integrated circuits. Secondly, both short- and long-distance transmission lines commonly use signals of one polarization to reduce losses. Usually, it is TE polarization [14]. Bragg gratings are used to connect fiber transmission lines and silicon photonics
devices. Bragg condition for a given wavelength and angle of incidence can only be applied for one polarization. As a rule, TE polarization is selected because it corresponds to the fundamental waveguide mode when the width of the waveguide is greater than its height [15]. The possibility of creating Bragg grating for TM polarization was shown, but its efficiency factor was 20% lower than for TE polarization [15,16].

In the second stage of the calculations, transmission characteristics of the photonic memory cell were analyzed. It was determined at what waveguide dimensions the maximum difference between transmission levels is reached.

For this purpose, 2D and 3D numerical calculations were carried out which produced fairly similar results. The structure length was 20 μm to avoid taking into account scattering light. The length of the GST layer was 1 μm. All the other dimensions were the same as in the first stage. A longitudinal section of the photonic storage element was selected for the 2D simulations. Perfectly matched layers (PML) were used in both 2D and 3D numerical calculations as boundary conditions. The key feature of the PML is almost no reflection of the waves that incidents from non-PML material upon the PML. Thus, it was assumed that all light scattered on the GST layer absorbed on the excessively long boundaries of the structure covered by PML.

![Figure 4. 2D simulations of the photonic storage element with different lengths of crystalline GST. Signs (a) and (b) corresponds to 1 μm and 2 μm respectively.](image)

2D numerical calculations of the guiding light in the photonic memory cell showed the main trend: the difference between transmission levels decreases with the waveguide height. Furthermore, these calculations are consistent with the mode structure obtained in the first stage. Figure 4 shows that the waveguide mode gradually attenuates in the crystalline GST layer and shifts closer to the upper boundary as was demonstrated (figure 2b).

![Figure 5. Transmittance versus waveguide height. Dash and solid lines correspond to the crystalline and amorphous GST phases.](image)

3D numerical calculations provided several curves of transmittance versus height for various widths of the waveguide (figure 5). It should be noted that matching between graphs obtained from 2D
and 3D calculations of the guiding light is better for wider waveguides. This is completely logical because the strip waveguide is closer to the thin-film waveguide, the wider it is. Also, only one length of the GST layer was considered in this paper. But figure 4 demonstrates that an increase of the GST layer length leads to a stronger attenuation which may cause a greater difference between the transmission levels of the photonic memory cell.

Summing up the above, the largest difference between the transmission levels of the photonic memory cell appears on the bottom border of the overlap between the “immune” zone of the photonic memory cell and the single TE-mode regime of the Si strip waveguide (bottom black line on figure 3b). It reaches about 80 percentage points in the center of the overlap.

4. Conclusion
In conclusion, the optimal geometry of the photonic memory cell suitable for long- and short-distance communication was determined. Furthermore, the approach of designing single TE-mode devices with a switching refractive index, which may be useful for creating silicon photonics devices or photonic integrated circuits, was shown.

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