Comparison of digital PWM control strategies for high-power interleaved DC–DC converters

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Abstract: Three pulse-width-modulation (PWM) digital control approaches are evaluated to provide the current sharing between phases in high-power dual-interleaved DC–DC converters. The implementation of a digital peak current, multi-sample averaged current and an enhanced single-sample averaged current control in a TMS320F28377D is described. A summary of stability requirements is provided for ACM and experimental results from a 60 kW, 75 kHz silicon carbide DC–DC converter are used to evaluate the steady-state and dynamic performance of the three control methods. Overall the best performance in terms of tracking and speed of response was achieved by the enhanced single-sample method. The multi-sampled technique provided the highest tracking accuracy, but at the expense of the slowest dynamic response. The fastest dynamic response was achieved by the digital peak current control, but this method is limited by poor noise immunity and instability for duty ratios in the region of 0.5.

1 Introduction

By sharing the current between parallel-connected, phase-shifted channels, interleaving techniques provide a method of spreading the thermal load and reducing passive component requirements in high current converter applications. For example, in multi-kW DC–DC converters that might be used in an electric vehicle power train [1]. However, to ensure current sharing between the parallel channels, individual current regulators are normally required, which are often implemented using analogue techniques such as peak current mode (PCM) control [2, 3].

Recent advances in digital technology have resulted in microcontroller units (MCUs) such as the TMS320F28377D with the onboard resources and computational speed to implement direct digital control of high-frequency power converters, potentially bringing benefits of improved noise immunity and flexibility. However, the inherent delays of the analogue-to-digital (A/D) conversion, the computation time and the operation of the digital pulse-width-modulation (DPWM) [4, 5] introduce an extra phase shift in the control-loop which has a detrimental effect on the controller bandwidth and the system stability [6, 7]. Therefore, extensive efforts have been made to reduce the delays of the A/D conversion, the computation time [5, 6, 8] and the DPWM operation using predictive techniques [7, 9–11].

The most common digital current mode controllers aim to regulate either the average current (average current mode, ACM), or the peak current (PCM) that flows through the separate converter phases. ACM control can be classified into two different categories according to the way the current is sampled: single-sample ACM and multi-sample ACM. PCM control can also be classified into predictive and mixed-signal PCM.

The single-sample ACM and predictive PCM techniques avoid the need for continuous sampling and reduce the ADC conversion time. By suitable selection of the sampling instant of the inductor current, the local average current or peak current can be acquired directly and subharmonic oscillations can be avoided if a suitable modulation carrier is employed [9]. The multi-sampling ACM is ideal for noisy environments; by taking the average of multiple samples in each cycle, the true average current is obtained and the noise-related problems are eliminated. However, the computational resources increase with respect to the single-sample method and limit the achievable operating frequency. The major drawback of the ACM techniques is that the control action takes at least one switching period to be executed after the sampling is performed. This is because the duty ratio is updated only once per switching period. Predictive PCM techniques were conceived to overcome this issue by calculating the value of the peak current a cycle ahead using not only the sampled current but other variables as well, such as the input voltage [9].

The mixed-signal PCM replicates the concept of an analogue PCM controller using a combination of digital modules and analogue comparators. A first version of this solution was successfully demonstrated in [12]; however, due to the limited resources of the available MCU, the technique was not extendable to interleaved converters. Another example of mixed-signal PWM implemented in a field-programmable gate array for a single-transistor buck converter is shown in [13].

Although analogue and digital PCM and ACM PWM control techniques are well established for single-transistor topologies, their modelling and application to interleaved converters is still developing. For example, a non-linear analysis and a digital PCM controller with variable slope compensation for interleaved converters has been proposed recently [14], whilst an averaged small-signal model of the dual boost interleaved converter with coupled inductors operating in discontinuous mode is proposed in [15]. Furthermore, the impact of the magnetic coupling on the stability of dual-interleaved boost converters with sampled ACM using the sampler decomposition technique is presented in [16].

This paper compares three digital PWM control strategies for a high-power, high-frequency dual-interleaved DC–DC converter. The control strategies investigated are mixed-signal-based PCM, eight-sample ACM and single-sample ACM. The operating principles are similar to those reported in [7, 11, 12]. However, unlike the implementation in [7], individual current control is used for each phase of the converter with a common current reference. The techniques in [11, 12] have not previously been applied to multiphase converters, and due to the features of the MCU employed [17], the digital PCM is easily implemented for the dual-interleaved converter. Moreover, an enhanced version of the single-sample ACM control technique is implemented.
The three control strategies were implemented in an evaluation platform developed with a dual-core 32-bit TMS320F28377D Delfino MCU from Texas Instruments. The dual real-time control-law accelerators provide 200 MHz of signal processing performance and feature two real-time control-law accelerators to implement time-critical control algorithms. The MCU has integrated analogue and control peripherals allowing further system consolidation. Functions such as the discrete slope compensation and signal averaging are implemented into the co-processors and the available peripherals, enabling the MCU to be dedicated to the main control routine.

The dual-interleaved DC–DC converter topology is shown in Fig. 1 and incorporates an interphase transformer (IPT). Q1–Q4 represent the gate drive signals for the transistors, and the pairs Q1, Q3 and Q2, Q4 can operate in a complementary mode, or in buck/boost mode.

2.1 Digital PCM control

The operation of the digital PCM controller is similar to its analogue counterpart. The comparators, ramp generator circuits and PWM modules are all replaced by MCU functions. Fig. 2a depicts the block diagram of the digital PCM controller. The reference for the phase currents, \( I_{\text{ref}} \), is combined with the digital slope generator waveforms to form the individual phase reference currents. The two digital slope compensating ramps are phase shifted by 180° and subtracted from the value of \( I_{\text{ref}} \) to prevent sub-harmonic instabilities. The resultant internal signals form inputs to independent 12-bit digital-to-analogue converters (D/A) connected to the negative input of on-board analogue comparators. The positive input of each comparator is connected to the measured phase currents, \( i_a(t) \) and \( i_b(t) \), of the IPT, respectively.

Sketches of the idealised waveforms are shown in Fig. 2b depicting the phase currents \( i_a(t) \) and \( i_b(t) \), the outputs of the D/A, \( I_{\text{ref,a}} \) and \( I_{\text{ref,b}} \), which are the difference between the reference current demand \( I_{\text{ref}} \) and its respective compensating slope, and the DPWM signals for the lower switches, \( Q_1 \) and \( Q_2 \). At the start of the switching period, \( T \), the gate drive signal \( Q_1 \) is forced high so the transistor turns on. As the time progresses, the compensating ramp with fixed slope \( M \) is subtracted from the initial set point value, \( I_{\text{ref}} \), and when the resultant meets the phase current level, the comparator sends an interrupt to the PWM module. Then, the gate drive signal \( Q_1 \) is forced low for the remainder of the period, creating a cycle-by-cycle current trip event. At the same time, the output of the digital slope compensator resets to the initial value of \( I_{\text{ref}} \) and remains static until the next switching cycle.

The propagation delay for the interrupt is ∼60 ns [17] and so the operation of the digital PCM controller is not significantly different to an analogue implementation. Consequently, any change in \( I_{\text{ref}} \) will result in a virtually immediate change in the phase currents, resulting in a very high bandwidth [13]; however, average current regulation is not achieved because the peak-to-peak phase current in this topology behaves non-linearly with the duty ratio. Current transients during the turn-on instants are blocked from the controller using a leading-edge blanking window of 25 ns.

2.2 Multi-sample ACM

Fig. 3a shows the block diagram of the multi-sample ACM control where the phase currents are individually sampled by a 12-bit A/D converter. Analogue comparators are not required. Before the A/D, the signals pass through anti-aliasing filters each with a 230 kHz cut-off frequency, which is below one-half of the maximum sampling frequency. In order to calculate the average value of the phase current, the controller acquires eight samples of each channel at equally spaced time points \( T/8 \) apart. The A/D converters are interrupted by signals generated by the PWM modules so high sampling rates along with precise timing can be achieved.

At the end of the acquisition process, the average value of the eight samples over the switching cycle is calculated (AVG) and compared against the reference current, \( I_{\text{ref}} \). The calculated error passes through a digital proportional–integral (PI) compensator, and the computed duty ratio, \( D \), is updated at the start of the next switching cycle while its corresponding gate drive signal is forced high.

The operation of the multi-sample ACM control with a trailing edge modulation is illustrated in Fig. 3b. The waveforms shown are the phase currents \( i_a(t) \), \( i_b(t) \), the counter values \( C_a(t) \), \( C_b(t) \), the duty-ratio values \( D_{a_f}(t) \), \( D_{b_f}(t) \), the sampling instants in both phases and the generated PWM signals for \( Q_1 \) and \( Q_2 \). When the value of the duty ratio, \( D_{a_f} \), in the PWM module is higher than the value of the counter, \( C_a \), then the gate drive signals are forced low. The duty ratio must be updated within the same switching cycle to avoid an extra one switching-cycle delay. The acquisition time for the eight samples, the calculation of the average value and the processing time of the PI controller have a detrimental effect on the bandwidth of the control loop [18], resulting in slower and possibly more oscillatory regulation of the phase currents.

2.3 Improved single-sample ACM

Fig. 4a shows the block diagram of the single-sample ACM control. The phase current is sampled only once in the middle of the transistor conduction intervals (when \( C_a = 0 \)) as shown in Fig. 4b. The acquisition and calculation process starts when the counter \( C_a \) of the PWM module is equal to zero. Owing to the symmetry of the waveforms over the switching cycle, the acquired...
sample is approximately the local-average value of the phase current. The sampled average current is then compared against the reference current $I_{\text{ref}}$, and the error is fed into a discrete PI compensator which calculates the new duty ratio. Finally, the calculated duty ratio is loaded into a digital PWM generator to produce the transistor-driving signals. Due to the operation of the DPWM, the duty ratio is commonly updated at the beginning of the next switching cycle; however, this generates an inherent delay of one switching cycle in the control process. To eliminate this delay, the DPWM generator is updated with the new duty ratio as soon as the calculation is finished, as shown in Fig. 4b. The effect of this modification is examined in Section 5.4, demonstrating that it does not have an impact on the regulation of the average current. In contrast with the multi-sample technique, the processing time of the controller and the latency of the A/D conversion become the only sources of delay, leading to an improved control loop bandwidth [16]. As a result, the phase currents will exhibit smaller oscillations and faster settling times.

3 Comparison of hardware requirements

The hardware resources and the total response time for the three control methods are summarised in Table 1. The comparators, the D/A converters and the slope generators used in the digital PCM control are all on-board the TMS320F28377D MCU. Therefore, the response time is dependent only on the propagation delay from the comparator that feeds the signal into the PWM module. The maximum switching frequency in PCM is limited by the resolution of the compensating ramp generators.

Although the A/D modules have the same configuration for both ACM control methods, the averaging and the simultaneous sampling process in the multi-sample ACM increases the total response time. Since the duty ratio is updated at the beginning of the next switching cycle, the maximum switching frequency is limited to 92 kHz. In contrast, the single-sample ACM only requires the sampling of the phase currents once per switching cycle, and the duty ratio is immediately updated, reducing the response time significantly. It is estimated that the maximum switching frequency is at least five times that of the multi-sample ACM.

4 Controller design

Boost mode operation was assured in the discussion of controller design since its dynamics are more complex than those in buck mode.
The stability regions of the dual-interleaved converter with IPT and PCM are more complicated than for a single converter and are given in [19]. The interaction of the phases through the IPT affects the slopes of the switch currents and consequently, the stability depends not only on the duty ratio, \( D \), but also on the inductance ratio, \( L_\text{d} \), between the differential inductance of the IPT, \( L_\text{diff} \), and the filter inductance, \( L_\text{f} \).

The inductance ratio \( L_\text{d} \) is normally much greater than four to ensure continuous conduction in the filter inductor and under this condition, the analysis in [19] has demonstrated that a minimum value for the compensating slope \( M \) of 0.25\( V_\text{BUS}/2L_\text{d} \) guarantees the stability in the region \( 0.1 < D < 0.9 \).

Table 2 shows the values of the converter’s components. The inductance ratio is 134.6, and assuming a maximum bus voltage of 800 V, the minimum slope required for stability, \( M_{\text{req}} \), is 115.6 kV/s. \( R_\text{s} \) is the current transducer gain. In the prototype, a compensating ramp of 120 kV/s was used.

4.2 Modelling the ACM control methods

The control loops were modelled as shown in Fig. 5. The samplers \( S_c \) and \( S_p \) represent the phase-shifted, A/D conversion of the phase currents. Accurately capturing the interleaved operation of the samplers is important for correct prediction of the closed-loop dynamics [16]. The PI controllers are labelled \( P(z) \), and the computational delay of the control algorithms, \( t_d \), is modelled by the time-delay unit \( e^{-st} \) where

\[
\tau = \begin{cases} 
  t_d & \text{for single - sample ACM} \\
  T & \text{for multi - sample ACM}
\end{cases}
\]

with \( t_d \) as given in Table 1. The DPWM operation is accounted for using a zero-order-hold extrapolator transfer function, \( G_{\text{dpwm}}(s) = (1-e^{-st})/s \) whilst the averaged small-signal dynamics of each phase current are modelled by the control-to-phase transfer functions, \( G_{\text{diff}}(s) \) and \( G_{\text{dpwm}}(s) \), as given in Table 2.

\[
G_{\text{diff}}(s) = \frac{\text{PI}(z)G_{\text{diff}}(z) + \text{PI}(z)G_{\text{dpwm}}(z) + \text{PI}(z)[G_{\text{diff}}(z) - G_{\text{dpwm}}(z)G_{\text{dpwm}}(z)]]}{1 + \text{PI}(z)G_{\text{diff}}(z) + \text{PI}(z)[G_{\text{diff}}(z) - G_{\text{dpwm}}(z)G_{\text{dpwm}}(z)]}
\]

\[
G_{\text{dpwm}}(s) = \frac{\text{PI}(z)G_{\text{dpwm}}(z) + \text{PI}(z)G_{\text{dpwm}}(z) + \text{PI}(z)[G_{\text{diff}}(z) - G_{\text{dpwm}}(z)G_{\text{dpwm}}(z)]]}{1 + \text{PI}(z)G_{\text{diff}}(z) + \text{PI}(z)[G_{\text{diff}}(z) - G_{\text{dpwm}}(z)G_{\text{dpwm}}(z)]}
\]
sample ACM response could be further reduced by increasing $K_i$, but at the expense of reducing the damping of the high-frequency oscillations and increasing the overshoot.

5 Experimental validation and comparison of performance

5.1 Converter prototype and evaluation platform

Fig. 7 shows the dual-interleaved DC–DC converter and the TI MCU used in the experimental validation. This dual-interleaved bi-directional converter with IPT uses 1200 V SiC metal–oxide–semiconductor field-effect transistors (MOSFETs) from CREE (now Wolfspeed) and it is water cooled. The voltage in the battery port can vary from 300 to 380 V, and the maximum bus voltage is 750 V. The continuous rated power is 60 kW, and a switching frequency of 75 kHz was used for the validation of all the control methods.

A host board with the required stages for the conditioning of the current transducers’ signals, filtering, protection, buffers and power supplies was developed for the TI control card. The control card of the MCU is mounted on the main interface PCB to maintain a low profile. The platform is then mounted on top of the gate drivers. The phase currents of the IPT are monitored with 400 kHz magneto-resistive current transducers and the conditioning removes the DC offset and sets the overall current gain. The host board can operate in stand-alone mode with an analogue current reference, or in a digital-interface mode, where the reference current can be set via a USB cable, or via a CAN interface. The software to implement the control strategies in the MCU was developed using TI’s Code Composer Studio and controlSUITE.

Fig. 8 presents a flowchart of the average current control methods in Code Composer.

5.2 Accuracy of the sampling methods

The accuracy of the sampling in the A/D converters of the MCU is controlled by the acquisition window [20] allowed to charge the sample-and-hold capacitors. As shown in Table 1, the acquisition time, $t_{S+H}$, for both sampled methods is equal, and it has been set to 75 ns. By using a first order RC model, the settling accuracy of the sampling for the 12-bit A/D conversion of the MCU can be estimated as [20].

![Fig. 7 SiC DC–DC converter prototype and the TI MCU and host board](image-url)
5.3 Performance in steady state

For each control method, the converter was tested in boost mode at power levels up to 60.5 kW, at the maximum bus voltage, 750 V, and with a maximum inductor current of 160 A. Over the battery voltage range, 300 V ≤ V_{BAT} ≤ 380 V, stable voltage and current waveforms were observed for all the control strategies, and the operation remained stable after changes in load and current reference set-point. No limit cycle oscillations were identified during the operation, confirming that quantisation effects are negligible due to the high-resolution capabilities of the A/D and DPWM modules [21–23]. However, it was found that the operation of the digital PCM was unstable for duty ratios between 0.52 and 0.57 as a result of measurement noise in the current feedback signals and the very small inductor current slope for duty ratios around 0.5. The ACM strategies were able to operate over the whole range of duty ratio of the converter, even near to D = 0.5.

Table 3 compares the most important features of the three control methods for steady-state operation.

The ACM strategies were unable to balance properly the currents when the converter operated in the discontinuous mode, and it was observed that one phase tended to the continuous current mode, whilst the other was in the discontinuous mode. This is because of a larger error in the calculation of the average. However, the current sharing in the discontinuous mode with the digital PCM was good. At different operating conditions in the continuous current mode, the measured DC imbalance between the phases was <5 A, or about 3% of the total input current.

5.4 Dynamic performance: step changes in the reference current

The transient behaviour was examined using step changes in load and reference current. Fig. 9 compares the experimental phase current i_a for the multi-sample ACM, the single-sample ACM and the PCM strategies for two different battery voltage and power conditions when an additional 10 A per phase is demanded at t = 0 s. To facilitate the analysis of the i_a waveforms, their instantaneous average values were plotted and superimposed over the waveforms.

Therefore, the accuracy of the A/Ds is expected to be 0.377 LSB, which translates to ±22 mA given the gain of the current transducers and signal conditioning. However, a more significant source of error is associated with the propagation delays around the control loop, which misalign the current sample locations of the single-sample ACM. As a result, an offset error was observed in the steady-state average value of the phase currents which was directly proportional to the amplitude of the phase current ripple. In the prototype, the estimated total propagation delay of the control loop elements was 1.25 μs ± 0.25 μs, leading to a maximum steady-state error of about 3.7 A ± 0.9 A with the maximum duty cycle.
Compared with the multi-sample ACM, the single-sample ACM response is from 2 to almost 16 times faster and it settles up to four times faster. These results confirm that the enhanced single-sample ACM control strategy offers a good trade-off between the response speed and overshoot compared with the other two methods. The rise time of the single-sample ACM degraded significantly with the operating condition, attributed to the effects of the frequency oscillation; however, the settling time and the overshoot were improved. The estimated controller bandwidth of the enhanced-single sample ACM is up to 12.4% of the switching frequency. After the current step, the averaged phase current waveform showed a high-frequency oscillation of 8.82 kHz followed by a lower frequency oscillation of 1.11 kHz. These frequencies match well the model predictions (Fig. 6b).

**Table 4** Comparison of experimental transient performance to a 10 A step change in the reference current demand per phase

| Control method, step-change transient | Analogue PCM\(^a\) | Digital PCM | Multi-sample | Single-sample |
|--------------------------------------|-------------------|-------------|--------------|---------------|
| \(V_{\text{BAT}}\) voltage, V         | 300               | 380         | 300          | 380           | 300           | 380           |
| rise time, \(t_{(10\%-90\%)}\), µs    | 7.9               | 8.5         | 9.7          | 9.7           | 804           | 590           | 395           | 37.5          |
| settling time, \(t_s\) (10%), ms      | 0.2               | 0.2         | 2            | 1.5           | 6.1           | 4.5           | 1.5           | 1.8           |
| overshoot, OS, %                      | 90.8              | 72          | 87.1         | 81.6          | 0             | 0             | 8.7           | 15.1          |
| estimated bandwidth, BW\(^b\), kHz   | 44.3              | 41.2        | 36.1         | 36.1          | 0.45          | 0.59          | 0.88          | 9.3           |

\(^a\)From SABER simulation.  
\(^b\)Estimated as: 0.35/(\(t_{(10\%-90\%)}\)).

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Fig. 9 Full view (left) and magnified view (right) of the experimental response of \(i_\text{a}\) to a 10 A step change in \(I_{\text{ref}}\).  
(a) Minimum \(V_{\text{BAT}}\) voltage, 30–36 kW: \(I_{\text{ref}}\) from 50 to 60 A, \(V_{\text{BAT}} = 300\) V, \(R_{\text{load}} = 8.6\) Ω.  
(b) Maximum \(V_{\text{BAT}}\) voltage, 49.4–57 kW: \(I_{\text{ref}}\) from 65 to 75 A, \(V_{\text{BAT}} = 380\) V, \(R_{\text{load}} = 8.6\) Ω.
The performance of both ACM methods degraded at different steady-state operating conditions, suggesting that a programmed variation of the PI gains could benefit the converter transient performance when operating over wide voltage and current ranges. Furthermore, an on-line selection of the PWM control strategy could extend the converter operation at light loads – where the PCM ensures the current sharing even with discontinuous phase currents.

6 Conclusions
This work has presented the implementation, evaluation, and comparison of three digital control methods for a dual-interleaved DC–DC converter. These were validated experimentally in a high-frequency, high-power DC–DC converter with SiC MOSFETs at power levels up to 60.5 kW at 750 V with a 75 kHz switching frequency. The conditions for stability were summarised, and the design process of the PI compensators was provided and validated experimentally.

The digital PCM has the fastest dynamic response, but it is unstable in the range 0.52–0.57 due to measurement noise in the current signals and the very low inductor current slope for duty ratios around 0.5. The multi-sampled ACM showed the best tracking of the current demand, but features the slowest response. Finally, the single-sample ACM exhibited an acceptable tracking of current demand and rapid dynamic response.

Fully understanding the advantages and drawbacks of the different digital control strategies is important for converters which have to operate with wide input/output voltage ranges and different load conditions, to enable acceptable steady-state and dynamic performance to be achieved and full use to be made of the MCU.

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8 References
[1] Hegazy, O., Van Mierlo, J., Lataire, P.: ‘Analysis, modeling, and implementation of a multidevice interleaved DC/DC converter for fuel cell hybrid electric vehicles’, IEEE Trans. Power Electron., 2012, 27, (11), pp. 4445–4458
[2] Calderon-Lopez, G., Forsyth, A.J., Gordon, D.L., et al.: ‘Evaluation of SiC BJTs for high-power DC-DC converters’, IEEE Trans. Power Electron., 2014, 29, (5), pp. 2474–2481
[3] Calderon-Lopez, G., Forsyth, A.J.: ‘High power density DC–DC converter with SiC MOSFETs for electric vehicles’. 7th IET Int. Conf. on Proc. Power Electronics, Machines and Drives, PEMD, 2014, pp. 1–6
[4] Bibian, S., Hua, J.: ‘Time delay compensation of digital control for DC switchmode power supplies using prediction techniques’, IEEE Trans. Power Electron., 2000, 15, (5), pp. 835–842
[5] Jingquan, C., Prodic, A., Erickson, R.W., et al.: ‘Predictive digital current programmed control’, IEEE Trans. Power Electron., 2003, 18, (1), pp. 411–419
[6] He, S., Hung, J.Y., Nelms, R.M.: ‘A digital predictive current mode controller using average inductor current’. Proc. IEEE Energy Conversion Congress and Exposition (ECCE), 2014, pp. 1092–1098
[7] Ilic, M., Makinovic, D.: ‘Digital average current-mode controller for DC–DC converters in physical vapor deposition applications’, IEEE Trans. Power Electron., 2008, 23, (3), pp. 1428–1436
[8] Taeed, F., Nyman, M.: ‘A new simple and high performance digital peak current mode controller for DC–DC converters’. Proc. IEEE Applled Power Electronics Conf. and Exposition (APEC), 2014, pp. 1213–1218
[9] Kumar, M., Gupta, R.: ‘Time-Domain analysis of sampling effect in DPWM of DC–DC converters’, IEEE Trans. Ind. Electron., 2015, 62, (11), pp. 6915–6924
[10] Corradini, L., Mattavelli, P.: ‘Modeling of multisampled pulse width modulators for digitally controlled DC–DC converters’, IEEE Trans. Power Electron., 2008, 23, (4), pp. 1839–1847
[11] Zhou, G., Xu, J., Jin, Y.: ‘Improved digital peak current predictive control for switching DC–DC converters’, IET Power Electron., 2011, 4, (2), pp. 227–234
[12] Hallworth, M., Shirsavar, S.A.: ‘Microcontroller-based peak current mode control using digital slope compensation’, IEEE Trans. Power Electron., 2012, 27, (7), pp. 3340–3351
[13] Taeed, F., Nyman, M.: ‘High-performance digital replica of analogue peak current mode control for DC–DC converter’, IET Power Electron., 2016, 9, (4), pp. 809–816
[14] Wu, H., Pickert, V., Giacouris, D., et al.: ‘Nonlinear analysis and control of interleaved boost converter using real-time cycle to cycle variable slope compensation’, IEEE Trans. Power Electron., 2017, 32, (9), pp. 7256–7270
[15] Barry, B.C., Hayes, J.G., Ryan, R.T., et al.: ‘Small-signal model and control of the interleaved two-phase coupled-inductor boost converter’. Proc. IEEE Energy Conversion Congress and Exposition (ECCE), 2016, pp. 1–6
[16] Villarruel-Parra, A., et al.: ‘Digital enhanced average-value modelling of interleaved DC–DC converters using sampler decomposition’, IEEE Trans. Power Electron., 2017, 32, (3), pp. 2290–2299
[17] Texas-Instruments.: ‘TMS320F2837xD Dual-Core Delfino Microcontrollers’, 2015
[18] Buso, S., Mattavelli, P.: ‘Digital control in power electronics’ (Morgan and Claypool, 2006)
[19] Forsyth, A.J., Calderon-Lopez, G.: ‘Sampled-Data analysis of the dual-interleaved boost converter with interphase transformer’, IEEE Trans. Power Electron., 2012, 27, (3), pp. 1338–1346
[20] Texas Instruments.: ‘TMS320F2837xD Dual-Core Delfino Microcontrollers’. Technical Reference Manual’, TMS320F2837xD Dual-Core Delfino Microcontrollers, 2016
[21] Peterchev, A.V., Sanders, S.R.: ‘Quantization resolution and limit cycling in digitally controlled PWM converters’, IEEE Trans. Power Electron., 2003, 18, (1), pp. 301–308
[22] Peng, H., Prodic, A., Alarcon, E., et al.: ‘Modeling of quantization effects in digitally controlled DC–DC converters’, IEEE Trans. Power Electron., 2007, 22, (1), pp. 208–215
[23] Stefanutti, W., Mattavelli, P., Saggini, S., et al.: ‘Energy-based approach for predicting limit cycle oscillations in voltage-mode digitally-controlled dc–dc converters’. Proc. Twenty-First Annual IEEE Applied Power Electronics Conf. and Exposition, APEC, 2006, pp. 1–7