THREE-PORT IMPEDANCE MODEL AND VALIDATION OF VSCs FOR STABILITY ANALYSIS

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Abstract

Modern power system is undergoing a paradigm shift from the synchronous generators-based system to the power electronics converters-dominated system. With the high penetration of converters, serious stability problems are provoked, especially the wideband oscillations (e.g., sub-synchronous oscillations, harmonic oscillations, etc). Various studies have been conducted in this respect, while most of them separate the ac-side stability with the dc-side stability. However, for the stability analysis of the hybrid AC/DC grid, it is necessary to consider the converter’s ac-side and dc-side, simultaneously. In this paper, the stability analysis of voltage source converters (VSCs) considering both ac and dc dynamics is carried out. At first, the three-port AC/DC admittance model of VSCs is established, and the corresponding measurement method from simulations is presented to validate its accuracy. Secondly, based on such three-port model, two stability analysis methods are presented: the one is based on the system open-loop model, where the stability can be judged via the Generalized Nyquist Criterion (GNC); the other one is based on the system closed-loop model, whose stability can be predicted through the pole-zero calculation. At last, a test AC/DC system is built in MATLAB/Simulink, by which the effectiveness of the three-port model-based stability analysis is validated.

1 Introduction

Nowadays, the power system is gradually transformed from pure AC or DC grid into the hybrid AC/DC grid [1], mainly formed by power electronics converters-dominated renewable energy sources. Unlike synchronous generators, the power electronic converters, e.g., voltage source converters (VSCs), exhibit unique characteristics of wideband dynamics and AC/DC couplings, imposing great challenges on the stable operation of the power system [2].

In this respect, the impedance-based stability tools [3] are favoured and numerous studies aimed at characterizing small-signal behaviours of VSCs have been carried out [4]-[6]. For the ac-side stability, the frequency couplings [3] inside the ac port are considered, from which various 2×2 impedance models emerged including dq models [4], complex vector models [5], etc. It has been proved that the accuracy of 2×2 models is enough for the converters’ ac-side stability analysis under symmetrical conditions [5]. For the dc-side stability analysis, the one-dimensional impedance model [6] is adopted to formulate the dc network model, whose stability can be studied via impedance aggregation methods [7].

To further improve the stability analysis accuracy, the influence of ac-/dc- side dynamics on the opposite side is noticed by some scholars and an equivalent ac-/dc- side impedance model [8], [9] is proposed. For example, the Ref [8] incorporate the dc-link dynamics of the Type-III wind turbine system into its ac-side impedance model through an indicator function; the Ref [9] proposed a building block-based modelling method for the Type-IV wind turbine, based on which the ac-side dynamics can be incorporated into the dc-side impedance model. However, neither the ac-side equivalent model nor the dc-side equivalent model is convenient for the stability analysis of large-scale AC/DC interconnected system [10]. To address this issue, this paper presents a three-port AC/DC admittance model so as to consider converters’ AC/DC dynamics, simultaneously. Furthermore, the corresponding measurement method from simulations is also provided. Based on such three-port admittance model, two stability analysis methods, i.e., open-loop method and closed-loop method, are discussed and applied in the converter AC/DC stability evaluation.

The rest of the paper is arranged as follows. Section 2 provides the VSC three-port AC/DC admittance model; Section 3 presents the frequency scanning method and validate the accuracy of the established model; Section 4 demonstrates the open-loop and closed-loop method in the AC/DC stability analysis; Section 5 concludes the paper.

2. Three-port AC/DC Admittance Model

In this section, the three-port admittance model of the VSC is built in a step-by-step manner. The topology of the VSC as well as its control scheme is presented in Fig. 1.

1.1 Main circuit modelling

As shown in Fig. 1, the d-q small-signal admittance model of the ac-side filter can be derived as:

$$\Delta u_{cdq} = -Z_{dq}^s(s) \Delta i_{gdq} + \Delta u_{gdq}$$

(1)
where $\Delta u_{cdq} = [\Delta u_{cdq}]$, $Z_{dq}(s) = \left[ R_i + sL_i \cdot \omega_i L_i \right]$, 

$\Delta i_{gdq} = [\Delta i_{gdq}]$ and $\Delta u_{gdq} = [\Delta u_{gdq}]$.

Since the VSC’s ac-side is coupled with its dc-side via the power balance, the ac-side and dc-side dynamics can be represented in (2) and (3), respectively.

$$\Delta u_{cdq} = \frac{3}{2V_{dc0}} \left( U_{cdq0}^T \Delta i_{gdq} + I_{gdq0}^T \Delta u_{cdq} \right)$$

where $\Delta m_{dq}(s) = \frac{[\Delta m_d]}{[\Delta m_q]}$, $m_{dq0} = \frac{[m_d]}{[m_q]}$.

$$U_{Tdq0} = \left[ U_{cd0} U_{eq0} \right], I_{Tdq0} = \left[ I_{gd0} I_{gd0} \right]$$

1.2 Control part modelling

1.2.1 PLL

The small-signal model of the phase locked loop (PLL) is like:

$$\Delta \theta_{pll}(s) = \frac{H_{pll}(s)}{s + U_{gd0} \cdot H_{pll}(s)} \Delta u_{gdq}$$

The relationship between the converter domain and the system domain is like:

$$\Delta i_{gdq} = \Delta i_{gdq} + I_{Tgdq0}(s) \Delta u_{gdq}$$

$$\Delta u_{gdq} = U_{Tgdq0}(s) \Delta u_{gdq}$$

$$\Delta m_{dq} = \Delta m_{dq} + M_{Tdq0}(s) \Delta u_{gdq}$$

(5)

where $\Delta i_{gdq}$, $\Delta u_{gdq}$ and $\Delta m_{dq}$ are aligned with the converter domain, while $\Delta i_{gdq}$, $\Delta u_{gdq}$ and $\Delta m_{dq}$ are aligned with the system domain. What’s more,

$$F_{pgd0}^\text{PLL} = \left[ \begin{array}{cc} 0 & I_{gd0} \cdot T_{pgd0}(s) \\ 0 & -I_{gd0} \cdot T_{pgd0}(s) \end{array} \right], \\ M_{pgd0}^\text{PLL} = \left[ \begin{array}{cc} 0 & m_{gd0} \cdot T_{pgd0}(s) \\ 0 & -m_{gd0} \cdot T_{pgd0}(s) \end{array} \right].$$

1.2.2 Inner current control loop

The modulation ratio can be represented as:

$$\Delta m_{dq}^c = \frac{1}{2V_{dc0}} \left[ H_{cc} \left( \Delta \phi_{gdq} - \Delta i_{gdq} \right) \right]$$

where $H_{cc} = \text{diag} \left( H_{cc}(s) H_{cc}(s) \right)$ and $H_f = \text{diag} \left( H_f(s) H_f(s) \right)$

By integrating the (5) into (6), the modulation ratio aligned with the system domain can be obtained as:

$$\Delta m_{dq} = \frac{\Delta \phi_{gdq}^c + \Delta i_{gdq}^c}{2V_{dc0} \cdot T_{cc}} + \frac{e^{-\frac{V_{dc0}}{T_{cc}}}}{V_{dc0}} \left( H_{cc}(s) + K_{d} \right) \Delta i_{gdq}^c$$

(7)

By integrating (7) into (2), the converter-side modulation voltage can be obtained as:

$$\Delta u_{cdq} = \frac{T_{cc}^2 \Delta i_{gdq}^c + T_{cc} \Delta i_{gdq} + T_{cc} \Delta u_{gdq} + T_{cc} \Delta T_{pdq0}(s) \Delta u_{gdq} \Delta V_{dc0}}{2V_{dc0} \cdot T_{cc}} + m_{dq0} \Delta u_{gdq}$$

Fig. 1 Main circuit and control scheme of the VSC
1.2.3 Outer control loop

The active power and reactive power can be calculated as:
\[ \Delta p = \frac{3}{2} U_{g dq0} \Delta i_{g dq} + \frac{3}{2} I_{g dq0} \Delta u_{g dq} \] (9)

where \( \Delta p = \left[ \Delta p \over \Delta q \right] \) and \( U_{g dq0} = \left[ U_{g dq0} \ U_{g dq0} \right] U_{g dq0} - U_{g dq0} \)

\[ I_{g dq0} = \left[ I_{g dq0} \ I_{g dq0} \right] \]

The alternating-power control and reactive-power control can be modelled as:
\[ \frac{3}{2} H_{pq} U_{g dq0} \Delta i_{g dq} + \frac{3}{2} H_{pq} I_{g dq0} \Delta u_{g dq} \] (10)

where \( H_{pq} = diag \left( H_{pq} (s) \ H_{pq} (s) \right) \).

The DC-voltage control and reactive power control can be modelled as:
\[ \frac{3}{2} H'_{pq} U_{g dq0} \Delta i_{g dq} + \frac{3}{2} H'_{pq} I_{g dq0} \Delta u_{g dq} \] (11)

where \( H'_{pq} = diag \left( 0 \ H_{pq} (s) \right) \), \( H_{dc} = \left[ H_{dc} (s) \ 0 \right]^T \).

The alternating-voltage control can be modelled as:
\[ \frac{H_{ac} U_{g dq0}}{T_{ac}} \Delta u_{g dq} \] (12)

where \( H_{ac} = diag \left( H_{ac} (s) \ H_{ac} (s) \right) \).

1.3 Three-port admittance model

The three-port admittance models of three commonly-used operating modes are derived in the following part, including the P/Q mode, V/f mode and DC/Q mode.

1.3.1 P/Q mode

By integrating (10) into (8), the converter-side modulation voltage can be represented as:
\[ \Delta i_{g dq} = \frac{3}{2} H_{pq} U_{g dq0} \Delta i_{g dq} + \frac{3}{2} H_{pq} I_{g dq0} \Delta u_{g dq} \] (10)

\[ + \frac{3}{2} H_{pq} U_{g dq0} \Delta i_{g dq} + \frac{3}{2} H_{pq} I_{g dq0} \Delta u_{g dq} \] (11)

By integrating (11) into (1), the ac-side admittance model can be obtained as:
\[ \Delta i_{g dq} = \frac{3}{2} H_{pq} U_{g dq0} \Delta i_{g dq} + \frac{3}{2} H_{pq} I_{g dq0} \Delta u_{g dq} \] (10)

The alternating-voltage control in (12) can be simplified as:
\[ \Delta i_{g dq} = \frac{3}{2} H_{pq} U_{g dq0} \Delta i_{g dq} + \frac{3}{2} H_{pq} I_{g dq0} \Delta u_{g dq} \] (11)

where \( H_{pq} = diag \left( H_{pq} (s) \ H_{pq} (s) \right) \).

The DC-voltage control and reactive power control can be modelled as:
\[ \frac{3}{2} H_{pq} U_{g dq0} \Delta i_{g dq} + \frac{3}{2} H_{pq} I_{g dq0} \Delta u_{g dq} \] (10)

where \( H_{pq} = diag \left( H_{pq} (s) \ H_{pq} (s) \right) \).

1.3.2 Vdc/Q mode

By integrating (11) into (8), the converter-side modulation voltage can be represented as:
\[ \Delta i_{g dq} = \frac{3}{2} H_{pq} U_{g dq0} \Delta i_{g dq} + \frac{3}{2} H_{pq} I_{g dq0} \Delta u_{g dq} \] (10)

By integrating (16) into (1), the ac-side admittance model can be obtained as:
\[ \Delta i_{g dq} = \frac{3}{2} H_{pq} U_{g dq0} \Delta i_{g dq} + \frac{3}{2} H_{pq} I_{g dq0} \Delta u_{g dq} \] (10)

The dc-side admittance model is the same as the (15) except for substituting the \( Y_{dc} \) and \( a_{z1} \) calculated in (17).

1.3.3 V/f mode

Under V/f mode, the system frequency is given by the converter, meaning that PLL dynamics can be ignored. The modulation ratio model in (7) can be simplified as:
\[ \Delta m_{dq} = \frac{e^{-sT_{i}}}{V_{dc0}} H_{cc} \Delta i_{g dq} + e^{-sT_{i}} H_{cc} K_{d} \Delta i_{g dq} \] (18)

By integrating (18) into (8), the converter-side modulation voltage can be represented as:
\[ \Delta u_{g dq} = \left( T_{cc} \Delta i_{g dq} + T_{cc} \Delta i_{g dq} \right) V_{dc0} + m_{dq0} \Delta u_{dc} \] (19)

The alternating-voltage control in (12) can be simplified as:
\[
\Delta i_{g_{dq}} = H_{ac} \Delta u_{g_{dq}} \tag{20}
\]

By integrating (20) into (19), the converter-side modulation voltage can be represented as:

\[
\Delta u_{cd} = \left( T_{ac}^{1} H_{ac} \Delta u_{g_{dq}} + T_{ac}^{2} \Delta i_{g_{dq}} \right) V_{dc0} + m_{dq0} \Delta u_{dc} \tag{21}
\]

By integrating (21) into (1), the ac-side admittance model can be represented as:

\[
\left( -Z_{dq}^{c} - Z_{dq}^{c} V_{dc0} \right) \Delta i_{g_{dq}} = T_{ac}^{1} A H_{ac} V_{dc0} - I \Delta u_{g_{dq}} + m_{dq0} \Delta u_{dc} \tag{22}
\]

\[
\Rightarrow \Delta i_{g_{dq}} = A^{-1} \frac{B}{a_{2+1}} \Delta u_{g_{dq}} + A^{-1} \frac{m_{dq0}}{a_{2+1}} \Delta u_{dc}
\]

The dc-side admittance model is the same as the (15) except for substituting the \( Y_{dq} \) and \( a_{2+1} \) calculated in (22). Based on the (14), (15), (17) and (22), the three-port admittance of the VSC can be represented in complex vector as:

\[
\begin{bmatrix}
\Delta i_{g_{dq}} \\
\Delta i_{dc}
\end{bmatrix} = \begin{bmatrix}
Y_{dq} a_{2+1} & Y_{dc} \\
Y_{dq} & Y_{dc}
\end{bmatrix} \begin{bmatrix}
\Delta u_{g_{dq}} \\
\Delta u_{dc}
\end{bmatrix} \tag{23}
\]

### 3 Model Validation

#### 3.1 Frequency scanning method

The method for obtaining one-dimensional and two-dimensional admittances from simulations has been well discussed [3]. Here, the frequency scanning method for obtaining the above three-dimensional model is introduced. As shown Fig. 2, the first step is to select a vector of frequencies \( f_{dqab} \), i.e., the frequencies at which the admittances shall be calculated. Taking the series voltage injection for example, three perturbation signals will be injected from ac- and dc-side.

\[
AC: v_{inj} = V_{inj} \begin{bmatrix}
\sin (\omega_{inj} t) \\
\sin (\omega_{inj} t + \omega_{1} t) \\
\sin (\omega_{inj} t + \omega_{1} t + 2\pi / 3)
\end{bmatrix}
\]

\[
AC: v_{inj} = V_{inj} \begin{bmatrix}
\sin (\omega_{inj} t - \omega_{1} t) \\
\sin (\omega_{inj} t - \omega_{1} t + 2\pi / 3) \\
\sin (\omega_{inj} t - \omega_{1} t + 2\pi / 3)
\end{bmatrix}
\]

\[
DC: v_{inj} = 2V_{inj} \sin (\omega_{inj} t) \tag{24}
\]

After converting time-domain signals to the frequency domain as described in Fig. 2, the following equations can be used to find the three-port admittances:

\[
\begin{bmatrix}
Y_{dd} & Y_{dq} & a_{1} \\
Y_{qd} & Y_{qq} & a_{2} \\
b_{1} & b_{2} & Y_{dc}
\end{bmatrix} \begin{bmatrix}
v_{d1} & v_{d2} & v_{d3} \\
v_{q1} & v_{q2} & v_{q3} \\
v_{dc1} & v_{dc2} & v_{dc3}
\end{bmatrix} = \begin{bmatrix}
i_{d1} & i_{d2} & i_{d3} \\
i_{q1} & i_{q2} & i_{q3} \\
i_{dc1} & i_{dc2} & i_{dc3}
\end{bmatrix}^-1 \tag{25}
\]

### 3.2 Model validation

The parameters of VSC under three commonly-used control schemes are given in Table 1. The corresponding simulation model is built in the Matlab/Simulink.

| Mode | Parameters | Data |
|------|------------|------|
| VSC  | Bandwidth (PQ; PLL; CC) | 2.5-40; 200 (Hz) |
|      | ac-side filter | 66.7 \( \mu \)F; 2 \( \mu \)H |
|      | dc-side capacitor; control delay | 20mF; 100ms |
|      | power rating (active; reactive) | 300MW; 80MVar |
| VSC  | control bandwidth (AC; CC) | 25; 200 (Hz) |
|      | ac-side filter | 1mF; 66.5 mH |
|      | dc-side capacitor; control delay | 22.5 \( \mu \)F; 100m |
|      | Bandwidth (PQ; DC; PLL; CC) | 3; 40; 200 (Hz) |
| VSC  | control bandwidth (reactive) | 0 MVar |
|      | ac-side filter | 1mF; 66.5 mH |
|      | dc-side capacitor; control delay | 22.5 \( \mu \)F; 100m |
|      | power rating (reactive) | 0 MVar |

The comparisons between the frequency scanning results and the theoretical three-port modelling are presented in Fig. 1. From which, it can be seen that the accuracy of theoretical models is high, which validates the correctness of the established three-port admittance model.
AC network and DC network can be represented as:

4.1.1 Open-loop model-based stability analysis

distribution for the stability analysis. The second one utilizes the
GNC for the stability analysis. The marginal unstable condition is set as: increasing the internal impedance of the ac-grid from 2+j6.28 (20mH) from 2+j9.42 (30mH). The root locus of the det \( Y_{\text{vsc}} \) is shown in Fig. 5. From which, the theoretical results (surround the point (-1, j0)) indicate that the system is unstable with internal impedance equals to 2+j9.42.

4 Simulation analysis

In this section, the stability analysis of a typical AC/DC converter system is given using the above established three-port admittance model. The structure of the studied system is given in Fig. 4, where the converter’s ac-side is connected to an unideal ac-grid, and its dc-side is connected with a dc transmission network.

Fig. 4 The topology of the studied AC/DC system

4.1 Theoretical Analysis

Two commonly-used stability analysis methods are both applied in this part. The first one utilizes the system open-loop model and apply the generalized Nyquist criterion (GNC) for the stability analysis. The second one utilizes the system closed-loop model and calculated the pole-zero distribution for the stability analysis.

4.1.1 Open-loop model-based stability analysis

As shown in Fig. 4, the open-loop impedance models of the AC network and DC network can be represented as:

\[
\begin{bmatrix}
V_{ac} \\
V_{aq} \\
V_{dc}
\end{bmatrix} = \begin{bmatrix}
Y_{ac} & Y_{aq} & 0 \\
Y_{aq} & Y_{aq} & 0 \\
0 & 0 & Y_{dc}
\end{bmatrix} \begin{bmatrix}
I_{ac} \\
I_{aq} \\
I_{dc}
\end{bmatrix}
\]

(26)

The open-loop admittance model of the VSC is like:

\[
\begin{bmatrix}
I_{ac} \\
I_{aq} \\
I_{dc}
\end{bmatrix} = \begin{bmatrix}
Y_{dd} & Y_{dq} & a_1 \\
Y_{qd} & Y_{qq} & a_2 \\
0 & b_1 & b_2
\end{bmatrix} \begin{bmatrix}
V_{ac} \\
V_{aq} \\
V_{dc}
\end{bmatrix}
\]

(27)

According to [5], the impedance ratio of the studied system can be constructed as \( Z_{\text{net}}Y_{\text{vsc}} \), whose stability can be judged via the GNC. The marginal unstable condition is set as: increasing the internal impedance of the ac-grid from 2+j6.28 (20mH) from 2+j9.42 (30mH). The root locus of the det \( Y_{\text{vsc}} \) is shown in Fig. 5. From which, the theoretical results (surround the point (-1, j0)) indicate that the system is unstable with internal impedance equals to 2+j9.42.

4.1.2 Closed-loop model-based stability analysis

The closed loop model of the studied system can be obtained by formulating the system nodal admittance matrix. As can be seen from the Fig. 4, the studied system constitutes of two nodes, which can be modelled as:

\[
Y_{\text{node}} = \begin{bmatrix}
Y_{dd} & Y_{dq} & a_1 \\
Y_{qd} & Y_{qq} & a_2 \\
b_1 & b_2 & Y_{dc} + Y_{dc}
\end{bmatrix}
\]

(28)

According to [11], the stability can be judged by calculating the equation of det \( Y_{\text{node}} = 0 \). The system is stable if and only if there is no RHP-zeros (right-half-plane). The marginal unstable condition is set as the same as the 4.1.1. Fig. 6 presents the system pole-zero distribution. From which, it can be seen that there appear one pair of unstable RHP-zeros with internal impedance equals to 2+j9.42.

4.2 Simulation Validations

From the above analysis, it can be seen that the open-loop-based and the closed-loop-based stability analysis will give the same stability conclusion that the system should be unstable when the ac-grid internal inductance equals to
30mH. The corresponding time-domain simulations are presented in Fig. 7, which are consistent with the theoretical results. The effectiveness of the three-port admittance model-based AC/DC stability analysis has been verified.

5 Conclusion

In this paper, the three-port admittance model of the VSC is developed and its accuracy is validated by the proposed measurement method from simulations. Based on such model, two stability analysis methods (i.e., open-loop and closed loop) are both applied in the converter’s AC/DC stability evaluation. It is found that the above two methods can obtain the identical stability conclusion. In which, the open-loop method relies on the inspection of the Nyquist root locus, while the closed-loop method is based on the calculation of RHP poles-zeros. In the authors’ future work, more complicated AC/DC interconnected system will be considered to broaden the application scope of the three-port admittance model-based stability analysis method.

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