Abstract—Over the past decade a large family of spintronic devices have been proposed as candidates for replacing CMOS for future digital logic circuits. Using the recently developed Modular Approach framework, we investigate and identify the physical bottlenecks and engineering challenges facing current spintronic devices. We then evaluate how systematic advancements in material properties and device design innovations impact the performance of spintronic devices, as a possible continuation of Moore’s Law, even though some of these projections are speculative and may require technological breakthroughs. Lastly, we illustrate the use of the Modular Approach as an exploratory tool for probabilistic networks, using superparamagnetic magnets as building blocks for such networks. These building blocks leverage the inherent physics of stochastic spin-torque switching and could provide ultra-compact and efficient hardware for beyond-Boolean computational paradigms.

Index Terms—

I. INTRODUCTION

HERE has been enormous progress in the last few decades, effectively combining spintronics and magnetics into a powerful force that is shaping the field of memory devices, while new materials and phenomena continue to be discovered at an impressive rate [1]–[6] providing an ever-increasing toolbox for the design of novel functional devices [7]–[14]. It is natural to ask whether these developments can be harnessed to meet the increasing interest in finding new ways to meet the challenge of continuing the celebrated Moore’s law in the coming decades.

Broadly speaking the relevant developments in spintronic materials and phenomena belong in two categories, those that enable conversion of electrical into magnetic information (the WRITE function) and those that enable the reverse process (the READ function). READ and WRITE functions are of course central to memory devices and it has also been shown that they can be integrated into a transistor-like device, with gain and input-output isolation, that we call a “spin switch” which can be used as a building block for logic circuits [8], [15].

A natural question to ask is how such a spin switch compares with a standard switch based on CMOS (complementary metal oxide semiconductor) technology, and several authors have addressed different aspects of this question [16]–[19]. The purpose of this paper is to establish a systematic framework for evaluating the impact of different READ and WRITE units on the key performance criteria for logic devices, namely their static power consumption, switching energy, switching delay and the energy-delay product. This framework is based on Modular Approach to Spintronics [20], [21] whereby different materials and phenomena are represented by experimentally benchmarked modules, whose input and output voltages and currents have four components, one for charge and three for spin (fig. 1a). These modules can then be combined using standard SPICE or SPICE-like platforms to evaluate circuit and system level performance.

In Section II, we analyze a series of spin switches based on a magnetic tunnel junction (MTJ) for the reader and the spin Hall effect (SHE) for the writer providing a direct comparison of switching currents and power with a series of CMOS inverters (fig. 1b). The purpose is to pinpoint the factors underlying the inferior static power and energy-delay product of spin switches relative to a CMOS switch. In Section III using modular approach we evaluate spin switches utilizing several alternative readers and writers (fig. 1c) which show a potential improvement in performance that could be comparable CMOS if optimistic material performance and integration parameters are realized in the future.

Since Moore’s law has been made possible by a doubling of the number of switches in a given area every two years, this cannot continue without a significant reduction in the energy-delay product relative to CMOS which seems difficult based on present state-of-the-art in spintronics. However, it has been noted that from a consumer perspective, Moore’s law represents a doubling of “user value” every two years and this could be enabled through enhanced functionality [22]. It has been recognized that nanomagnets could provide enhanced functionality over CMOS through their unique physics that provides a natural bistability, threshold response and stochastic operation.

We end in Section IV with an evaluation of a simple version of a restricted Boltzmann machine featuring stochastic spin switches (fig. 1d) and is similar to other examples of usage of stochasticity of magnets for computing [23]–[26]. Such “stochastic computers” are commonly implemented virtually using software algorithms on a deterministic hardware platform, but nanomagnets could provide a natural physical hardware for their efficient implementation [27]–[29]. A detailed evaluation of different options and possibilities is beyond the scope of this paper. Our purpose here is simply to use the Modular Approach to establish a common framework for connecting from basic materials and phenomena all the way to circuits and systems, both deterministic and stochastic.
II. SPIN-SWITCHES VS. CMOS

In this section we use the original proposal of the spin switch [8] as an example to examine the physics of power dissipation in spintronic devices. The spin switch uses an MTJ stack for READ, while WRITE is through a GSHE layer driving a ferromagnet (FM) coupled magnetically to the MTJ, providing electrical isolation and coupling, while the GSHE-based writing provides gain. In section III, we systematically go through other variations and possibilities of READ/WRITE units that can be used to build a family of spin switches.

As a reference point, we have used a CMOS inverter built from ASU-PTM models for 14nm HP-FinFETs [30], [31] to highlight the differences and similarities between physics of switching and power dissipation in both charge based and spin based devices. Fig. 2a,b shows a FO-1 inverter chain built using CMOS and the spin-switch respectively. Details on simulation parameters are shown in the supplementary. For details on spin-circuit modeling and to obtain open-source circuit models of the devices used in this work, please see [21].

A. Static Dissipation

Static power dissipation is the Joule heating (I^2R) losses at steady state, i.e. when the device is not switching. It is a critical measure of device performance, since this contributes to the thermal budget of any circuit built using the device.

Insets in fig. 2c,d show a typical switching transient and toggling of the voltages causally (V1 → V2 → V3) in the
logic pipeline. The supply voltage levels used in HP-CMOS are typically 700–900 mV, whereas in spin-switch at minimal overdrive, it can range from 10–100 mV and is sufficient to generate the threshold spin current necessary (100–200 μA) to switch a typical nanomagnet with a 40 kBT stability, given the characteristic resistances of all the components (GSHE, MTJ) are around 0.5 – 2 kΩ (A complete list of parameters are shown in the supplementary).

The static power levels in HP-CMOS are of the order of nW (fig. 2c) as expected from the leakage current levels [32], which is much lower compared to dynamic power levels. However, the static power dissipation in spin-switch is nearly the same as the dynamic power dissipation because the spin-switch does not turn off at steady state (fig. 2d). There is a constant current flow through the MTJs, since the resistance ratio $R_{AP}/R_P$ of the MTJ pair is 3 – 4, compared to CMOS where $R_{OFF}/R_{ON}$ of the PMOS–NMOS pair is $10^4$ – $10^5$.

Additionally, the input side of the spin-switch (GSHE) is a low impedance component, unlike the CMOS where the MOSFET gate terminals are high impedance components that become open circuit at steady state. As a result of these two static current flows, the static power dissipation remains near μW levels for the spin-switch.

### B. Dynamic Dissipation: Energy × Delay

Any alternative to CMOS needs to be competitive in terms of both the switching delay and switching energy. A useful measure of dynamic dissipation is the product of the switching energy $E$ × switching delay $\tau$ per switching event, because a switch can be overdriven for lower switching delay, resulting in higher switching energy or vice versa. It has been shown [33] that the $E \times \tau$ product can be related to the charge consumed during the switching process, i.e. $E \times \tau = Q_{sw} \times R$, where $Q_{sw}$ is the charge drawn over the effective resistance $R$ to switch the device. The $E \times \tau$ metric recast as $Q_{sw}^2/R$ provides a powerful approach to understanding the fundamental limits of dynamic dissipation in a device by quantitatively relating it to its physical properties and opens a pathway to better component design for higher performance.

1) Switching Delay: The timescale of switching in a scaled CMOS inverter, a 14 nm FinFET in this case, is of the order of $\approx 1–10$ ps (fig. 2a). The switching delay for magnets is dependent on the current overdrive: At large overdrive delays the delay can be determined by angular momentum considerations, where a total amount of charge that is twice the number of spins ($M_s \Omega / \mu_B$) needs to be deposited for a complete reversal of magnetization. This means that the switching delay inversely scales with the driving current, i.e. $\tau \sim 2qM_s \Omega / \mu_B I_s$. The exact switching delay is a strong function of the initial angle of the magnetization [34]. In our simulations, the initial angle is chosen to be the rms of the equilibrium deviation from the easy axis [7].

2) Switching Energy and Switching Charge: Switching energy in itself can be calculated by simply integrating the power between the switching window. While this approach does work numerically, to gain better physical understanding of dynamic dissipation, we look at the switching charge, as discussed at the beginning of the section. To do so from our circuit testbench, we first integrate the input current (red arrows indicated in fig. 2a,b) supplied from the sources within the switching window, whose starting point is the the time-point at which the input signal starts changing and the ending point is the time-point at which the output signal is within $1\%$ of its final value. This provides the total charge per switching event. Additionally, we integrate the total current deposited to the CMOS input terminals (gates) and we do the same for the analogous quantity for magnets, the $z$-component of the spin-torque current $(I_{STZ} = (\hat{m} \times \hat{I_s} \times \hat{m})_z)$ which are indicated by the green arrows in fig. 2b.

We find that the area under the green curve for the CMOS (fig. 2e) is about $220$ $e^-$, equivalent to the charge deposited to the CMOS gates $Q_{SW} = (C_{PMOS} + C_{NMOS}) V_{DD}$, whereas the green area for the spin-switch (fig. 2f) is about $Q_{SW} \approx 2qN_s \approx 1,600,000$ $e^-$ where $N_s = M_s \Omega / \mu_B$ is the total number of spins ($\mu_B$). Therefore, reducing the dynamic dissipation for any logic device involves scaling the $Q_{SW}$ through better component design [35], [36].

| Metric                  | HP-CMOS       | Spin-Switch  |
|-------------------------|---------------|--------------|
| Voltage Level           | $\approx 0.8$ V | $\approx 20$ mV |
| Static Power            | $\approx 10^3$ μW | $\approx 10$ μW |
| Dynamic Power           | $\approx 10^3$ μW | $\approx 10$ μW |
| Switching Delay         | $\approx 10^{-2}$ ns | $\approx 10$ ns |
| Switching Charge, Q     | $\approx 10^2 - 10^3$ $e^-$ | $\approx 10^3 - 10^6$ $e^-$ |
| $R_{OFF}/R_{ON}$        | $\approx 10^5$ | $\approx 4$ |

**TABLE I**

**COMPARISON BETWEEN HP-CMOS AND SPIN-SWITCH DISSIPATION**

We summarize the metrics discussed in this section in Table I. While the details of the physics in these examples depend on the specifics of circuit design, material parameters and overdrive conditions, we believe that the measure of static power in terms of $R_{OFF}/R_{ON}$ (READ) and dynamic power in terms of $Q_{SW}$ (WRITE) are general notions that should be applicable to any logic device.

### III. ALTERNATIVE DESIGNS FOR SPIN-SWITCH

In this section, we show how the spin-switch device can be made competitive with CMOS inverter through improvements in device materials, magnetic stack designs, and use of different components based on new phenomena. This allows us to project performance enhancements quantitatively and build
possible roadmaps for optimized spin-switch devices. We have covered only a small sampling of possible optimization and design space for spintronic devices. Our main purpose is to demonstrate the power of Modular Approach in building and evaluating alternative designs.

A. Alternative Design Trajectories

We show 3 example trajectories of how the spin-switch can be optimized by stacking one change on top of the other and observe its effect in reducing the static and the dynamic dissipation. The next few headings describe the changes we introduce to the spin switch design sequentially. While each of these improvements can be applied independent of each other, the presented information shows how the performance of the spin-switch can improve dramatically when these optimizations are applied in succession.

The numbers reported in this section are from the measurements of static power, switching energy and switching delay performed for an FO-1 circuit testbench, as described in the supplementary. These numbers would vary if a different testbench, such as FO-4 or 32-bit adder, is chosen, since it will change the loading conditions. While some of the low $Q_{su}$ spin-switch designs could work with ultra low voltages ($< 20 \text{ mV}$), a conventional circuit may not be able to provide $V_{DD,SS} < 50 \text{ mV}$ due to the inability to deliver sufficient power at such low voltages [37]. Additional transistors could be used in combination with each spin-switch to obtain lower voltages and such transistors will have their own dissipation. We have used a minimum supply voltage level of 35 mV in some of the alternative designs but do not include dissipation numbers of transistors in such cases. Furthermore, in this work our analyses are limited to the devices themselves and we do not measure dissipation in interconnect and supply rails as well as the driver circuitry consisting of CMOS devices. All the material parameters used in these simulations are listed in the supplementary and are optimistic projections which may not have been demonstrated at present. We also list theoretical minimum operating points for the spin switch designs discussed in this section based on analytical model for these devices and the material parameters.

1) Magnet Design—IMA to PMA: The first improvement we make to the device design is the replacement of magnets with in-plane magnetic anisotropy (IMA) with perpendicular magnetic anisotropy (PMA). This reduces the minimum switching current required by getting rid of the large demagnetizing field ($h_d = 4\pi M_s / H_k$) while maintaining the barrier height $U$, since in the monodomain approximation, the in-plane minimum switching current is given by [34]:

$$I_{s:crit} = \frac{4q}{h} \alpha U \left(1 + \frac{h_d}{2}\right)$$ (1)

However, in the case of GSHE-based switching employing PMA magnets introduces the well-known problem of indeterministic switching, since the polarization of the injected spin-current from the GSHE is in the in-plane direction, thereby bringing the magnetization of the free layer to the in-plane hard axis, an unstable equilibrium position. A small magnetic field ($h_{bias} = H_{bias} / H_k$) in the direction of the charge current helps break the symmetry of this equilibrium position and push the magnetization towards an easy axis. This field may be provided either locally [38] or as a small exchange-bias field built within the structure of the magnetic stack [39]. We incorporate this field in our model simply as an additional external field provided to the LLG modules in the spin-circuit model.

In this case, the minimum spin-current necessary to switch the magnet is approximately given by [40]:

Fig. 3. a. Alternative Designs for spin switch: Modular Approach to Spintronics allows us to create alternative designs by replacing an individual module with another, without changing the full spin-circuit model. These alternative designs can be evaluated for their $E \times \tau$ and static power. The figure illustrates modification to the spin switch can be incorporated by swapping appropriate modules in the spin-circuit model, due to the built-in modularity of the spin switch in terms of READ and WRITE units. b. $E \times \tau$ Improvement through Material Optimization: Investigating the improvement of $E \times \tau$ under various alternative materials and device shown in three different design trajectories, and comparison with CMOS. The three trajectories employ innovations such as high $H_k$ scaled PMA magnets, Heusler alloys, high spin-Hall angle (SHA) materials, magneto-electric effect in multiferroics (ME), and synthetic ferrimagnets. The optimizations applied together can bring the performance of spin switches to within an order of magnitude of $E \times \tau$ of both high performance and low standby power CMOS (HP-CMOS, LSTP-CMOS). c. Static Power Improvement through Material Optimization: Investigating the static energy dissipation for the three different design trajectories (same as in b.)
\[ I_{\text{crit}} = \frac{4q}{\hbar} U \left( \frac{1}{2} - \frac{h_{\text{bias}}}{\sqrt{2}} \right) \]  

(2)

It is interesting to note that the threshold current for “hard-axis” switching does not benefit from a one to two orders of magnitude reduction due to the absence of the damping factor \( \alpha \) that is present in eq. 1.

In fig. 3b and fig. 3c we observe that changing the magnetic layer in the spin-switch from IMA to PMA reduces both the switching energy as well the static power dissipation, due to the relatively lower switching currents that allow reduced supply voltages.

2) Magnet Design—High Anisotropy Scaled PMA: Using PMA magnets in spin-switch opens up the possibility of using high anisotropy magnets commonly used in the magnetic recording industry. This is achieved by scaling down the grain volume \( (\Omega) \) and saturation magnetization \( (M_s) \) while increasing the effective anisotropy \( (H_k) \) to maintain a given thermal stability since the barrier height is given by \( U = M_s \Omega H_k / 2. \) While the minimum spin-current necessary to switch remains the same (eq. 2), the supply voltage levels to produce the minimum switching current increase as compared to unscaled PMA magnets due to two reasons: (a) increase in the resistance of the GSHE writer and (b) reduction of the geometrical gain due to a decrease in the length of the GSHE metal.

However, using high \( H_k \) and low \( M_s \Omega \) reduce switching charge \( Q_{sw} = 2qM_s \Omega /\mu_B \) in the magnet, significantly improving the energy-delay as shown in fig. 3b, since \( E \times \tau = Q_{sw}^2 R \). On the other hand, the reduction in \( E \times \tau \) comes at a cost of increase in the static power (fig. 3c) due to increased supply voltages, as shown in both red (medium scaled PMA) and blue (high scaled PMA) trajectories.

Increasing the \( H_k \) of the magnets could necessitate changing the coupling mechanism between the WRITE and the READ units, since dipolar coupling may not provide strong enough interaction necessary for successful device operation. Advancements in magnetic oxides may open a pathway for stronger exchange-interaction based coupling of high \( H_k \) magnets through either indirect exchange coupling mediated through the magnetic oxide [41] or by replacing the metallic FM with an insulating FM [42]. However, the thickness of the oxide layer necessary to provide exchange coupling is a critical issues that may interfere with the electrical isolation of the WRITE and the READ units through leakage currents due to tunneling effect, forming a parasitic MTJ between them. Our analysis presented here did not account for this leakage current in the coupling layer. Additionally, fabricating and creating contacts on highly scaled device could have lithographic challenges that may require change in the device design of the spin switch and is out of scope for our present study. Our focus here is to show how Modular Approach can be used to project performance enhancement assuming such challenges could be met.

3) Reader Design—Heusler Alloys: A major improvement that can be incorporated in the spin-switch designs is the use of high polarization magnets (such as Heusler alloys) to fabricate MTJ or Spin-Valve based readers through an increase of \( R_{OFF}/R_{ON} \). It can be shown from TMR formula \( (R_{AP} - R_P)/R_P = 2P^2/1 - P^2 \) that to achieve the same \( R_{OFF}/R_{ON} \) ratio as a well designed CMOS inverter \( (\sim 10^5) \), the interface polarization that would be required is \( P = 0.99999 \). For the sake of performance projection we choose an optimistic value of \( P = 0.99 \) (close to an experimentally reported value of \( P \approx 0.96 \) at low temperatures [6]) which gives \( R_{OFF}/R_{ON} \approx 100 \).

Use of Heusler alloys helps in reducing the static power loss in the reader by reducing the supply voltages \( V_{DD,SS} \) and bringing \( V_{out} \) closer to the supply voltages (fig. 3a). However, the high \( P \) of the MTJ reader imposes a limit on the overdrive that can be applied to the spin-switch, because the spin-current generated in the MTJ may start switching the device in competition with the GSHE writer, especially in scaled spin-switches where the geometrical gain in GSHE given by \( \theta_{SH} L/t (1 - \tanh(t/\lambda_{sf})) \) is limited by scalability of GSHE thickness \( t \) and spin-flip length \( \lambda_{sf} \) compared to length \( L \) [43].

In fig. 3b and fig. 3c we see the effect of a reduction of both \( E \times \tau \) and static power due to Heusler alloy MTJs in both red (medium scaled PMA) and green (ME spin-switch) trajectories.

4) Writer Design—High Spin Hall Angle: Using materials with large spin Hall angles can help in scaled spin-switches by lowering the voltage levels, since smaller charge currents can produce larger spin-current. For projection purposes, we choose a spin-Hall angle of 1. In both blue (high scaled PMA) and red (medium scaled PMA) trajectories in fig. 3b and fig. 3c, the \( E \times \tau \) is reduced by two orders of magnitude and static dissipation is reduced by one order of magnitude due to lower supply voltage levels.

We have assumed that the resistance of the GSHE material remains the same during this optimization, which is not necessarily true. In fact it has been suggested that resistance of most GSHE materials increase hand in hand with the Hall angle [43], and this may reduce the magnitude of the \( E \times \tau \) and static power improvements projected. However, it was recently suggested that using a composite structure consisting of a spin conduction layer between the GSHE and the magnet, it may be possible to obtain large spin-Hall angles from small spin-Hall angle materials [44]. Such innovations in device engineering could provide a way to obtain large spin-Hall angles without the large resistance penalty.

5) Writer Design—Spin Torque vs. Magnetoelectrics: Instead of the spin-torque mechanism, voltage-controlled magnetoelectric (ME) phenomena based on multiferroic materials could be used for the WRITE in a spin-switch. In particular, BiFeO\(_3\) (BFO) was recently shown to be capable of switching an IMA magnet deterministically [4] by applying a voltage controllable exchange bias field on the adjacent magnetic layer. Indeed, various device proposals have used this mechanism as part of their device designs [11], [45], [46].

The switching process using ME fundamentally requires only \( Q_{sw} = C_{ME} V \) amount of charge, where \( C_{ME} \) is the capacitance of the ME material and \( V \) is the applied voltage. Since the switching mechanism is not spin-torque, it can be much smaller compared to \( Q_{sw} = 2qM_s \Omega /\mu_B \).
opening a pathway for much more efficient switching. This phenomenon is also attractive because it creates a high input impedance device similar to a CMOS inverter and reduces static dissipation. Indeed, it is seen in fig. 3b and fig. 3c that the green trajectory that replacing the GSHE writer with an ME based writer reduces both \(E \times \tau\) and static power drastically.

The ME module used in this work does not consider the ferroelectric polarization caused by the electric field and hence is not a comprehensive model for the multiferroic material. Additionally, the dynamics of the ME based switching was deduced to be a complex 2-step process composed of two partial switchings in two different directions, ultimately causing a full reversal in the experiment [4]. Coupling the LLG with an ME module produces only a single step switching. Since the detailed physics of multiferroic switching is not fully understood at this time, these projections are subject to change as a better understanding of voltage based multiferroic switching develops.

6) Magnetic Stack Design– Synthetic Ferrimagnets: Usage of synthetic ferrimagnet (Sy–AFM) stacks instead of monolayer magnets opens up an avenue of performance improvement of the spin-switch. This is due to a reduction in the effective switching charge \((Q_{sw} = 2qM_s\Omega_{eff}/\mu_E)\), where \((M_s\Omega_{eff} = M_s\Omega_1 - M_s\Omega_2)\) compared to a monodomain magnet \((M_s\Omega_{total} = M_s\Omega_1 + M_s\Omega_2)\) with the same thermal stability, for details see [36]. In the blue trajectories (high scaled PMA) of fig. 3b and fig. 3c we use an Sy–AFM stack where \((M_s\Omega_1 - M_s\Omega_2)/(M_s\Omega_1 + M_s\Omega_2)\) ≈ 1/3. This provides an order of magnitude improvement in \(E \times \tau\) alongside a reduction of voltage levels by 40\% which helps reduce the static power. Optimized designs of Sy–AFM stacks may yield even higher performance gains.

B. Outlook for the Spin-Switch

Overall we find that spin-switches may approach the performance of contemporary scaled FinFET based CMOS if integration of various high performance materials along with careful device engineering and advanced lithographic and fabrication abilities can be achieved. Meanwhile, CMOS technology itself is a moving target, considering recent developments such as negative capacitance [47], therefore it will be difficult for an individual spin device to outperform the CMOS inverter in the near future.

Natural domain of spintronics may be in complex circuits where the inherent physics of a single device can map to a higher order logic function that requires many basic logic gates to implement, as argued in [48]. These devices can then be deployed as compact and efficient computational nodes in complex Boolean and Beyond-Boolean architectures. The next sections explore this possibility using simple proof of concept demonstration.

IV. BEYOND BOOLEAN CIRCUITS: SPINTRONIC PROBABILISTIC NETWORKS

A big thrust of spintronic research is the use of spin devices as ultra-compact deterministic nodes of hardware neural networks [49]–[51] due to inherent majority logic-like behavior (detailed analysis of such a compact majority logic circuit is provided in the supplementary). In this respect, the advantage of spin-switch as nodes of neural networks primarily lie in their ability to reduce dissipation and simpler circuit design due to reduced hardware cost compared to CMOS based implementations. In this section we go beyond the applications of spin-switch as neural network nodes and look at the physics of stochasticity of superparamagnets and its applications in the emerging field of probabilistic spintronic logic [29].

A. Stochastic Magnet Dynamics

Our spin-switch designs discussed up to this point have used magnets with \(U = 40 k_BT\) with state retention of nearly a decade. The state retention and barrier height is related by \(\tau_r = \tau_0e^{U/k_BT}\), where \(\tau_0 \sim 0.1 - 1\) ns. Even though we have not explicitly concerned thermal noise in our analysis so far, when \(U/k_BT \gg 1\), there is only a minor effect on the switching dynamics due to thermal agitation, and the switching delay is largely determined by the initial angle of the magnet. We have approximately taken this initial angle variation into consideration by using mean initial angles that are in consistent with results from equilibrium statistical mechanics [52].

However, reducing the barrier height of these ferromagnets to superparamagnetic values, for example \(\approx 3 k_BT\), makes the magnetization stochastic and the statistical average of the magnetization lies between “up” and “down” states. As an example, fig. 4a shows a transient simulation of a magnet with \(U = 2.75 k_BT\) only under the influence of a thermal noise field. The magnetization keeps flipping back and forth between the up and down states, since the state retention time is of the order of ns. This stochastic behavior along with spin-torque or magnetic field switching can yield building blocks for probabilistic computers [27]–[29] where probabilistic behavior comes naturally due to inherent physics of the device itself.

B. Stochastic Spin Switch: Building Block of Probabilistic Networks

Fig. 4b shows a stochastic spin-switch operating under room temperature conditions. As explained in the previous section, the spin-switch naturally accumulates multiple input signals at its input node (analogous to synaptic addition in a neuron) and switches. When this switching happens at a finite temperature, the output of the neuron instead of being a deterministic function whose output is “0” or “1”, instead turns into a stochastic one whose average is skewed by the input current (blue background curve in fig. 4c). This output when passed through a simple R-C low pass filter circuit \((\tau_{RC} = 225\) ns in the simulation) that extracts the average value produces a transfer function which instead of being a sharp transition, turns into a sigmoidal function (red foreground curve in fig. 4c), useful for building probabilistic and fuzzy logic circuits.

The stochastic regime of operation of the spin-switch and its use as a building block for probabilistic networks was first identified in [27], where it was called a transynapse. The major distinction between the previous work and this paper is our use of spin-switches with in-plane magnets in the
Fig. 4. In this paper, we have performed a systematic analysis of a family of spin-based logic devices using the recently developed Modular Approach framework. By making materials, device and circuit level projections, we have estimated critical circuit metrics such as dynamic (WRITE unit) and static (READ unit) power dissipation of concrete designs available with several technological breakthroughs in the field, optimistic material and design parameters that would only be attempted here. Our main purpose is to demonstrate how another technology is highly implementation dependent and is not attempted here. We mainly focus on how the Modular Approach enables the exploration of stochastic spin-switches to build novel beyond-Boolean circuits.

C. Programmable Stochastic Networks

By connecting the stochastic spin switches together we can create novel beyond Boolean circuits, an example being the Ising network, a computational model that is widely used to solve complex optimization and pattern recognition problems [54]. The nodes of the network interact with each other through the charge currents in the GSHE, which can be controlled by either changing the voltage between the nodes (through sign and magnitude) or by using an external CMOS circuitry. The network can then be annealed to its ground state providing a solution of the problem. While the Ising model in itself is purely deterministic, stochasticity of the superparamagnets helps the system to traverse the configuration space of the network at the speed of the magnet retention time, which could be a few ns or less for superparamagnets.

As an example, fig. 4e,f shows two different solutions mapped in the steady state statistical configuration of the 3-node Ising network (fig. 4d), ferromagnetic and frustrated spin-glass. These two configurations can be obtained by tuning the interaction strength and sign between the three nodes. One way to achieve this is by an external circuitry that implements a weighing logic of the form $V_{in;i} = \sum w_{ij} V_{out;j}$ where $V_{in;i}$ is the input voltage for the $i^{th}$ node, $V_{out;j}$ is the output of the $j^{th}$ node and $w_{ij}$ is the weight logic and the elements of the Ising Hamiltonian for the given problem. In this problem $w_{ij} = 0$ and all positive $w_{ij}$ creates ferromagnetic interaction, whereas all negative $w_{ij}$ creates anti-ferromagnetic interaction. The magnitude of the $w_{ij} = \pm w_0$ is chosen to ensure that the average output of the nodes are in the “saturated” region of the fig. 4a. The circuit is simulated in presence of magnetic thermal noise and the temperature of the system reduced slowly to anneal the circuit to its ground state. The time duration of these simulations were chosen to be three orders of magnitude higher compared to the state retention time of the superparamagnets to obtain stable statistics. The ref. [28] explains the simulation technique in more detail.

If the interactions are tuned to make the network ferromagnetic, the configuration space obtained after a time averaged measurement is shown in fig. 4f where nodes prefer the 000 or 111 state, i.e. all of the nodes are in the same state. However, for antiferromagnetic interaction, the nodes take up the other 6 possible states equally distributed statistically (fig. 4f), forming a frustrated spin-glass, since the interaction strengths are equal in this simulation.

This proof of concept demonstration points towards a possibility of building larger dynamically programmable stochastic networks (as in [28], [29]) that solve algorithms of data mining, optimization, searching, and machine learning (Deep Belief Networks) which at present are commercially implemented as software solutions. These stochastic networks map complex and composite logic functions directly into the physics of the spintronics, paving the way of creating ultra-compact and efficient learning networks.
such as non-volatility that are not captured by the energy-delay product. It is important to point out however, given the enormous rate of discoveries in the field, it is very likely that the conclusions presented in this paper will quickly need to be updated, and as such, one of the key objectives of this paper was to illustrate how the Modular Approach framework can reliably integrate emerging physics into existing physics at the device and circuit level.

As an example of the versatility of the modular approach, we show that even for beyond-Boolean architectures different from what is conventionally discussed in spin-logics proposals, the same framework allows systems-level analyses, once an experimentally benchmarked module for the relevant building blocks (superparamagnets in this case) is available.

ACKNOWLEDGMENT

The authors would like to extend their thanks to Dr. Behtash Behin-Aein for sharing his preprint [27] and for helpful discussions on programmable stochastic networks. The authors would also like to thank Dr. Azad Naeemi for helpful discussions on engineering challenges with the spin-switch and the alternative designs. This work was supported in part by the National Science Foundation through the NCN-NEEDS program, contract 1227020-EEC and in part by C-SPIN, the National Science Foundation through the NCN-NEEDS program, contract 1227020-EEC.

REFERENCES

[1] I. Mihai Miron, G. Gaudin, S. Auffret, B. Rodmacq, A. Schuhl, S. Pizzini, J. Vogel, and P. Gambardella, “Current-driven spin torque induced by the Rashba effect in a ferromagnetic metal layer,” Nat Mater., vol. 9, no. 3, pp. 230–234, Mar. 2010.

[2] L. Liu, C.-F. Pai, Y. Li, H. W. Tseng, D. C. Ralph, and R. A. Buhrman, “Spin-Torque Switching with the Giant Spin Hall Effect of Tantalum,” Science, vol. 336, no. 6081, pp. 555–558, May 2012.

[3] Y. L. Chen, J. G. Analytis, J.-H. Chu, Z. K. Liu, S.-K. Mo, X. L. Qi, H. J. Zhang, D. H. Lu, X. Dai, Z. Fang, S. C. Zhang, I. R. Fisher, Z. Hussain, and Z.-X. Shen, “Experimental Realization of a Three-Dimensional Topological Insulator, Bi2Te3,” Science, vol. 325, no. 5937, pp. 178–181, Jul. 2009.

[4] J. T. Heron, J. L. Bosse, Q. He, Y. Gao, M. Trassin, L. Ye, J. D. Clarkson, C. Wang, J. Liu, S. Salahuddin, D. C. Ralph, D. G. Schomel, J. Igüéez, B. D. Huey, and R. Nemsch, “Deterministic switching of ferromagnetism at room temperature using an electric field,” Nature, vol. 516, no. 7531, pp. 370–373, Dec. 2014.

[5] W.-G. Wang, M. Li, S. Hageman, and C. L. Chien, “Electric-field-assisted switching in magnetic tunnel junctions,” Nat Mater., vol. 11, no. 1, pp. 64–68, Jan. 2012.

[6] H.-x. Liu, Y. Honda, T. Taira, K.-I. Matsuda, M. Arita, T. Uemura, and M. Yamamoto, “ Giant tunneling magnetoresistance in epitaxial Co2MnSi/MgO/Co2MnSi magnetic tunnel junctions by half-metallicity of Co2MnSi and coherent tunneling,” Applied Physics Letters, vol. 101, no. 13, p. 132418, 2012.

[7] B. Behin-Aein, D. Datta, S. Salahuddin, and S. Datta, “Proposal for an all-spin logic device with built-in memory,” Nat Nano, vol. 5, no. 4, pp. 266–270, Apr. 2010.

[8] S. Datta, S. Salahuddin, and B. Behin-Aein, “Non-volatile spin switch for Boolean and non-Boolean logic,” Applied Physics Letters, vol. 101, no. 25, p. 252411, Dec. 2012.

[9] D. E. Nikonov, G. I. Bourianoff, and T. Ghani, “Proposal of a Spin Torque Majority Gate Logic,” IEEE Electron Device Letters, vol. 32, no. 8, pp. 1128–1130, Aug. 2011.

[10] J. G. J. Zhu, D. M. Bromberg, M. Moneck, V. Sokalski, and L. Pileggi, “mLogic: All spin logic device and circuits,” in 2015 Fourth Berkeley Symposium on Energy Efficient Electronic Systems (EES), Oct. 2015, pp. 1–2.
B. Behin-Aein, A. Sarkar, S. Srinivasan, and S. Datta, “Switching energy-delay of all spin logic devices,” *Applied Physics Letters*, vol. 98, no. 12, p. 123510, Mar. 2011.

K. Y. Camsari, A. Z. Pervaiz, R. Faria, E. E. Marinero, and S. Datta, “Ultrafast Spin-Transfer-Torque Switching of Synthetic Ferrimagnets,” *arXiv preprint arXiv:1606.04428*, 2016.

G. Huang, “Compact physical models for power supply noise and chip/package co-design in gigascale integration(gsi) and three-dimensional (3-d) integration systems,” Ph.D. dissertation, Georgia Institute of technology, Dec. 2008.

A. K. Smith, M. Jamali, Z. Zhao, and J.-P. Wang, “External Field Free Spin Hall Effect Device for Perpendicular Magnetization Reversal Using a Composite Structure with Biasing Layer,” *arXiv:1603.09624 [cond-mat]*, Feb. 2016, arXiv: 1603.09624.

A. van den Brink, G. Vermijls, A. Solignac, J. Koo, J. T. Kohlhepp, H. J. M. Swagten, and B. Koopmans, “Field-free magnetization reversal by spin-Hall effect and exchange bias,” *Nat Commun*, vol. 7, p. 10854, Mar. 2016.

K.-S. Lee, S.-W. Lee, B.-C. Min, and K.-J. Lee, “Threshold current for switching of a perpendicular magnetic layer induced by spin Hall effect,” *Applied Physics Letters*, vol. 102, no. 11, p. 112410, Mar. 2013.

V. Sokalski, D. Bromberg, D. Morris, M. Moneck, E. Yang, L. Pileggi, and J.-G. Zhu, “Naturally Oxidized FeCo as a Magnetic Coupling Layer for Electrically Isolated Read/Write Paths in mLogic,” *IEEE Transactions on Magnetics*, vol. 49, no. 7, pp. 4351–4354, Jul. 2013.

P. Li, T. Liu, H. Chang, A. Kalitsov, W. Zhang, G. Csaba, W. Li, D. Richardson, A. DeMann, G. Rimal, H. Dey, J. Jiang, W. Porod, S. Field, J. Tang, M. Marconi, A. Hoffman, O. Myrasov, and M. Wu, “Spin-Orbit torque-assisted switching in magnetic insulator thin films with perpendicular magnetic anisotropy,” *Nature Communications*, vol. 7, no. 12688, Sep 2016.

S. Hong, S. Sayed, and S. Datta, “Spin Circuit Model for 2D Channels with Spin-Orbit Coupling,” *Scientific Reports*, vol. 6, 2016.

S. Sayed, V. Q. Diep, K. Y. Camsari, and S. Datta, “Spin Funneling for Enhanced Spin Injection into Ferromagnets,” *Scientific Reports*, Accepted.

S. Ganguly, M. M. Torunbalci, S. A. Bhave, and K. Y. Camsari, “MESH Nano-Oscillator: All Electrical Doubly Tunable Spintronic Oscillator,” in *Device Research Conference (DRC), 2016 74th Annual*. IEEE, 2016.

M. G. Mankalale, L. Zhaoxin, A. K. Smith, D. Mahendra, M. Jamali, J.-P. Wang, and S. Sapatnekar, “A Fast Magnetoelectric Device Based on Current-driven Domain Wall Propagation,” in *Device Research Conference (DRC), 2016 74th Annual*. IEEE, 2016.

S. Salahuddin and S. Datta, “Use of negative capacitance to provide voltage amplification for low power nanoscale devices,” *Nano letters*, vol. 8, no. 2, pp. 405–410, 2008.

C. Pan and A. Naemi, “A Proposal for Energy-Efficient Cellular Neural Network based on Spintronic Devices,” *arXiv preprint arXiv:1604.04584*, 2016.

M. Sharad, C. Augustine, G. Panagopoulos, and K. Roy, “Spin-Based Neuron Model With Domain-Wall Magnets as Synapse,” *IEEE Transactions on Nanotechnology*, vol. 11, no. 4, pp. 843–853, Jul. 2012.

M. Sharad, D. Fan, and K. Roy, “Spin-neurons: A possible path to energy-efficient neuromorphic computers,” *Journal of Applied Physics*, vol. 114, no. 23, p. 234906, Dec. 2013.

V. Q. Diep, B. Sutton, B. Behin-Aein, and S. Datta, “Spin switches for compact implementation of neuron and synapse,” *Applied Physics Letters*, vol. 104, no. 22, p. 222405, Jun. 2014.

K. Y. Camsari, “Modular approach to spintronics,” Ph.D. dissertation, Purdue University, Jan. 2015.

K. Y. Camsari, R. Faria, B. M. Sutton, and S. Datta, “Stochastic p-bits for probabilistic spin logic,” *arXiv preprint arXiv:1610.00377*, 2016.

Z. Bian, F. Chudak, W. Macready, and G. Rose, “The Ising model: teaching an old problem new tricks,” 2010.
Supplementary Information: Evaluating Spintronic Devices Using The Modular Approach

Samiran Ganguly, Kerem Yunus Camsari, and Supriyo Datta
School of Electrical and Computer Engineering, Purdue University
Emails: \{sganguly, kcamsari, datta\}@purdue.edu

1 Device Equations for the Spin Switch family

For the spin switch with grounded GSHE layer, the minimum logic voltage level \((V_{1,2,\ldots} = V_{LL})\) and supply voltage levels \((V_{DD}, V_{SS})\) necessary for switching are given by the following set of equations.

Basic fundamental material properties:

\[
2U = M_s \Omega H_k
\]

\[
g_{MTJ:P} = g_{MTJ:0}(1 + P_1 P_2 \hat{M} \cdot \hat{m}_r(t))
\]

\[
g_{MTJ:AP} = g_{MTJ:0}(1 - P_1 P_2 \hat{M} \cdot \hat{m}_r(t))
\]

\[
g_{GSHE} = \rho_{GSHE} L_{GSHE}
\]

\[
g_{FM-NM} = \Re(g_{\uparrow\downarrow}) A_{FM}
\]

Critical spin current for IMA magnet:

\[
I_{s;\text{crit}} = 4q \alpha U \left(1 + \frac{2\pi M_s}{H_k}\right)
\]

Critical spin current for PMA magnet:

\[
I_{s;\text{crit}} = 4q U \left(\frac{1}{2} - \frac{H_{w;\text{ext.}}}{\sqrt{2} H_k}\right)
\]

Transport relationship between GSHE charge current and critical spin current for switching the magnet:

\[
k_1 = \theta_{sh} \frac{A_{FM}}{W \tau} \frac{g_{FM-NM}}{g_{GSHE}} \left(\frac{g_{FM-NM}}{g_{GSHE}} \right) + \frac{g_{FM-NM}}{g_{GSHE}} g_{GSHE}
\]
where $W, \tau$ are width and dimensions of the GSHE material.

Voltage divider equation between the READ stage of the spin switch and the next stage (load):

$$k_2 = \frac{g_{MTJ:P} - g_{MTJ:AP}}{g_{MTJ:P} + g_{MTJ:AP} + g_{\text{load}}}
(9)$$

Relationship between the logic voltage level and the critical spin current:

$$V_{LL} = \frac{I_{\text{scrit}}}{k_1}
(10)$$

From the constitutive relationship between the electric and magnetic fields in the ME:

$$\alpha_{ME} = \mu_0 \frac{dM}{dE}
(11)$$

We can derive the relationship between logic voltage level and critical switching field for ME-FM system in ME spin switch (the threshold switching field of a magnet is $H_{sw} = H_k$, in a monodomain approximation) is:

$$V_{LL} = \frac{H_k t_{ME}}{\alpha_{ME}}
(12)$$

Relationship between the logic voltage level and supply voltage levels:

$$V_{DD:SS} = (\pm) \frac{V_{LL}}{k_2}
(13)$$

The symbols are noted in parameters section, $V_{LL}$ is the logic voltage level and is not necessarily the same as the supply voltages $V_{DD:SS}$. The simulation performed for fig. 2 (main paper) are at near minimal overdrive to be close to the numerically conditions described by the analytical expressions at switching threshold.

The $g_{\text{load}}$, in the device equations stands for the output loading on the device and can be substituted (for an FO-1 circuit) with $g_{\text{GSHE}}$ as a reasonable approximation of the input admittance of the next stage due to the GSHE material. We ignore the spin-Hall magnetoresistance effect (SMR effect) due to the write magnet of the next stage and its dynamics while switching. The SMR effect is automatically incorporated in the numerical spin-circuit model through the GSHE module but does not introduce a significant discrepancy from the above analytical expressions at steady state since it is a second-order effect proportional to $\theta_{SH}^2 \ll 1$. For ME based spin switch the $g_{\text{load}} = 0$ at steady state because a charged capacitor behaves as an open circuit.
2 Operating Points for the Spin Switch family

From the device equations above, it is possible to calculate the minimum operating point currents and voltages for the spin switch. The table below lists these operating points for the devices discussed in section III of the main paper. These points are calculated from the equations above and use the parameters provided in the last section of the supplementary.

| Device                        | $I_{s, \text{crit}}$ ($\mu$A) | $V_{LL}$ (mV) | $V_{DD}$ (mV) |
|-------------------------------|-------------------------------|---------------|---------------|
| IMA Spin Switch (SS)          | 401.9                         | 22.7          | 80            |
| Low $H_k$ PMA SS              | 235.8                         | 17            | 55            |
| PMA SS                        | 189.1                         | 42.6          | 138.2         |
| High $H_k$ Scaled PMA SS      | 196.7                         | 88.6          | 287.3         |
| High SHA high $H_k$ PMA SS    | 196.7                         | 26.6          | 86.1          |
| SyAFM SS                      | 65.4                          | 8.8           | 28.7          |
| High SHA PMA SS               | 189.1                         | 12.8          | 41.5          |
| Heusler MTJ PMA SS            | 189.1                         | 12.8          | 20.7          |
| ME SS                         | -                             | 13            | 26.5          |
| Heusler MTJ ME SS             | -                             | 13            | 13.2          |
| High ME SS                    | -                             | 433.3         | 442.2         |

3 Spin-Circuit Modules

The modular spintronic library of the consists of two kinds of modules.

**Transport Modules:** These modules capture the charge and spin transport through various materials, e.g. Normal metal (NM), Ferromagnet (FM), FM–NM Interface, Magnetic Tunnel Junctions (MTJ) and various spin-orbit materials such as Giant Spin Hall Effect (GSHE).

**Magnetics Modules:** These modules capture the physics of magnetic dynamics and interaction and are meant to be coupled with the transport modules. The modules available are: Landau-Lifshitz-Gilbert Equation Solver (LLG), Exchange Coupling, Dipolar Coupling, and Magneto-Electric Effect (ME).

Most of the Spin-Circuit modules used in this work have been described in the previous work [?] and their source code can be obtained from the online repository for the project [?]. In this work we introduced the new magneto-electric module that we briefly describe below.

3.1 Magneto-Electric Module

The magneto-electric effect is given by:

$$\alpha_{ME} = \mu_0 \frac{dM}{dE}$$  \hspace{1cm} (14)
Now:

\[ B = \mu_0 M \] \hspace{1cm} (15)

Therefore,

\[ dB_{ME} = \alpha_{ME} dE_{ME} \] \hspace{1cm} (16)

Where \( E_{ME} = V_{ME}/t_{ME} \) is the electric field on the multi-ferroic material, \( B_{ME} \) is the generated exchange field on an adjacent magnetic layer, and \( \alpha_{ME} \) is the empirically measured coefficient for the effect.

\[ \text{Figure 1: Spin-Circuit model for Magneto-Electric module} \]

The effect is modeled as a parallel plate capacitor and a controlled voltage source whose strength is the magnetic field produced by the ME layer as shown in fig. 1.

| Parameter          | Symbol | Units |
|--------------------|--------|-------|
| Area               | \( A_{ME} \) | m²    |
| Thickness          | \( t_{ME} \) | m     |
| ME Coefficient     | \( \alpha_{ME} \) | s/m   |
| Relative Permittivity | \( \epsilon_r \) | –     |

4 Complex Boolean Functions: Majority Logic

Spintronic phenomena enables many higher order Boolean functions to be implemented using minimal hardware compared to CMOS devices. An example of this is the majority function. In this section we use the Modular Approach to investigate the physics behind this capability.

In fig. 2f (in the main paper) we showed that critical charge necessary to switch a magnet can be related to the number of spins \( 2M_s \Omega/\mu_B \) comprising the magnet, and in the case of ME writer, it is the threshold charge (eq. 17) on the ME capacitor. This charge can be provided through currents coming in from multiple inputs all adding in without any extra circuitry, since it is more natural to add currents in metal interconnects unlike adding voltages. This fan-in capability of spintronic devices leads to the realization that higher level logic functions, such as majority function based logic are a natural domain of spintronics [?,?,?].
4.1 Majority Gate using the Magnetoelectric Spin-Switch

We investigate the physics of a majority function implemented using a single ME spin-switch and show that this may open the pathway for low dissipation complex logic circuits compared to those built using larger number of basic logic gates implemented through CMOS inverters [7]. Fig. 2a shows a 3 input majority function being implemented using an ME spin-switch. The output V4 implements the Majority function over the input signals V1, V2, V3, as can be seen from the simulation in fig. 2b. In the last plot of the fig. 2b we plot the current into the output switch, and the fig. 2c shows the current zoomed in for the second transition event.

4.2 Dissipative Cost of ME-SS Majority Function

It can be shown that the minimum charge necessary to switch the magnet is given by:

$$Q_{\text{crit}} = \epsilon_0 \epsilon_r \frac{A_{ME} H_k}{\alpha_{ME}}$$

For the chosen parameters the critical charge to switch the output device is $Q_{\text{crit}} =$
100 $e^-$. Numerically we find that in the switching window (for either of the switching events): $Q_{ME} = \int I_{ME}dt = \int I_{sw1}dt + \int I_{sw2}dt + \int I_{sw3}dt \approx 190 \ e^-$, which is close to the theoretical limit.

This number demonstrates that for the dissipative cost of just one CMOS inverter, ME spin-switch can implement a majority function as a basis of more complex functions, such as full adders that need a large number of CMOS inverters to implement [?], or neural networks [?].

5 Numerical Parameters For Spin-Circuit Models

We list the baseline parameters for various modules used in this work below. In simulation only one parameter is changed at a time, except for magnet design where the area of the magnet or $M_s$ is changed with $H_k$ to maintain an energy barrier of 40 $kT$. All parametric changes are monotonic. Note: $n$ stands for nano and has been used to reduce visual clutter from the tables.

**MTJ Module**

| Parameter          | Units | Value |
|--------------------|-------|-------|
| Conductance        | S     | 1m    |
| Polarization       | -     | 0.7   |
| In-Plane Coeff.    | -     | 1     |
| OOP Coeff.         | -     | 0     |

**MTJ Module: Heusler Alloy**

| Parameter          | Units | Value |
|--------------------|-------|-------|
| Conductance        | S     | 1m    |
| Polarization       | -     | 0.99  |
| In-Plane Coeff.    | -     | 1     |
| OOP Coeff.         | -     | 0     |

**MTJ Module: Heusler Alloy SV**

| Parameter          | Units | Value |
|--------------------|-------|-------|
| Conductance        | S     | 0.1   |
| Polarization       | -     | 0.99  |
| In-Plane Coeff.    | -     | 1     |
| OOP Coeff.         | -     | 0     |
**GSHE Module: IMA Magnet**

| Parameter          | Units | Value |
|--------------------|-------|-------|
| Width              | m     | 100n  |
| Length             | m     | 80n   |
| Thickness          | m     | 2n    |
| Spin-flip length   | m     | 2n    |
| Resistivity        | Ωm    | 1700n |
| Spin Hall Angle    | -     | 0.3   |

**GSHE Module: Low $H_k$ PMA Magnet**

| Parameter          | Units | Value |
|--------------------|-------|-------|
| Width              | m     | 100n  |
| Length             | m     | 100n  |
| Thickness          | m     | 2n    |
| Spin-flip length   | m     | 2n    |
| Resistivity        | Ωm    | 1700n |
| Spin Hall Angle    | -     | 0.3   |

**GSHE Module: Medium $H_k$ PMA Magnet**

| Parameter          | Units | Value |
|--------------------|-------|-------|
| Width              | m     | 32n   |
| Length             | m     | 32n   |
| Thickness          | m     | 2n    |
| Spin-flip length   | m     | 2n    |
| Resistivity        | Ωm    | 1700n |
| Spin Hall Angle    | -     | 0.3   |

**GSHE Module: High $H_k$ PMA Magnet**

| Parameter          | Units | Value |
|--------------------|-------|-------|
| Width              | m     | 16n   |
| Length             | m     | 16n   |
| Thickness          | m     | 2n    |
| Spin-flip length   | m     | 2n    |
| Resistivity        | Ωm    | 1700n |
| Spin Hall Angle    | -     | 0.3   |
### FM-NM Module: IMA Magnet

| Parameter        | Units | Value                        |
|------------------|-------|------------------------------|
| Conductance      | S     | $80n \times 100n \times 5 \times 10^{15}$ |
| Polarization     | -     | 0.7                          |
| In-Plane Coeff.  | -     | 1                            |
| OOP Coeff.       | -     | 0                            |

### FM-NM Module: Low $H_k$ PMA Magnet

| Parameter        | Units | Value                        |
|------------------|-------|------------------------------|
| Conductance      | S     | $\pi \times 50n \times 50n \times 5 \times 10^{15}$ |
| Polarization     | -     | 0.7                          |
| In-Plane Coeff.  | -     | 1                            |
| OOP Coeff.       | -     | 0                            |

### FM-NM Module: Medium $H_k$ PMA Magnet

| Parameter        | Units | Value                        |
|------------------|-------|------------------------------|
| Conductance      | S     | $\pi \times 16n \times 16n \times 5 \times 10^{15}$ |
| Polarization     | -     | 0.7                          |
| In-Plane Coeff.  | -     | 1                            |
| OOP Coeff.       | -     | 0                            |

### FM-NM Module: High $H_k$ PMA Magnet

| Parameter        | Units | Value                        |
|------------------|-------|------------------------------|
| Conductance      | S     | $\pi \times 8n \times 8n \times 5 \times 10^{15}$ |
| Polarization     | -     | 0.7                          |
| In-Plane Coeff.  | -     | 1                            |
| OOP Coeff.       | -     | 0                            |

### LLG Module: IMA Magnet

| Parameter        | Units | Value                        |
|------------------|-------|------------------------------|
| Area             | m²    | $80n \times 100n$            |
| Thickness        | m     | $2n$                         |
| Damping Coeff.   | -     | 0.01                         |
| Sat. Magnetization | emu/cc | 800                        |
| Aniso. Field Strength | Oe     | 130                         |

### LLG Module: Low $H_k$ PMA Magnet
| Parameter               | Units   | Value         |
|-------------------------|---------|---------------|
| Area                    | m²      | π × 50n × 50n |
| Thickness               | m       | 2n            |
| Damping Coeff.          | -       | 0.01          |
| Sat. Magnetization      | emu/cc  | 800           |
| Aniso. Field Strength   | Oe      | 130           |

**LLG Module: Medium H_k PMA Magnet**

| Parameter               | Units   | Value         |
|-------------------------|---------|---------------|
| Area                    | m²      | π × 16n × 16n |
| Thickness               | m       | 2n            |
| Damping Coeff.          | -       | 0.1           |
| Sat. Magnetization      | emu/cc  | 400           |
| Aniso. Field Strength   | Oe      | 2500          |

**LLG Module: High H_k PMA Magnet**

| Parameter               | Units   | Value         |
|-------------------------|---------|---------------|
| Area                    | m²      | π × 8n × 8n   |
| Thickness               | m       | 2n            |
| Damping Coeff.          | -       | 0.1           |
| Sat. Magnetization      | emu/cc  | 400           |
| Aniso. Field Strength   | Oe      | 10100         |

**LLG Module: High H_k PMA Sy−AFM**

| Parameter               | Units   | Value         |
|-------------------------|---------|---------------|
| Area                    | m²      | π × 8n × 8n   |
| Thickness Assist        | m       | 1.2n          |
| Thickness Free          | m       | 0.8n          |
| Damping Coeff.          | -       | 0.1           |
| Sat. Magnetization      | emu/cc  | 400           |
| Aniso. Field Strength   | Oe      | 10100         |

**LLG Module: High H_k IMA**

| Parameter               | Units   | Value         |
|-------------------------|---------|---------------|
| Area                    | m²      | 8n × 20n      |
| Thickness               | m       | 2n            |
| Damping Coeff.          | -       | 0.05          |
| Sat. Magnetization      | emu/cc  | 400           |
| Aniso. Field Strength   | Oe      | 13000         |
**ME Module**

| Parameter       | Units | Value          |
|-----------------|-------|----------------|
| Area            | m²    | 80n × 100n     |
| Thickness       | m     | 10n            |
| ME Coeff.       | -     | 1 × 10⁻⁸       |
| Rel. Permittivity| -     | 500            |

**High ME Module**

| Parameter       | Units | Value          |
|-----------------|-------|----------------|
| Area            | m²    | 80n × 100n     |
| Thickness       | m     | 10n            |
| ME Coeff.       | -     | 3 × 10⁻⁸       |
| Rel. Permittivity| -     | 500            |

**Dipolar Coupling Module: IMA Magnet**

| Parameter       | Units         | Value                     |
|-----------------|---------------|---------------------------|
| Sat. Magn. 1    | emu/cc        | 800                       |
| Vol. 1          | m³            | 100n × 80n × 2n            |
| Sat. Magn. 2    | emu/cc        | 800                       |
| Vol. 2          | m³            | 100n × 80n × 2n            |
| Dipolar Coeff.  | -             | 0.0256, −0.0128, −0.0128  |

**Exchange Coupling Module: Low Hₖ PMA Magnet**

| Parameter       | Units         | Value                     |
|-----------------|---------------|---------------------------|
| Sat. Magn. 1    | emu/cc        | 800                       |
| Vol 1           | m³            | π × 50n × 50n × 2n         |
| Sat. Magn. 2    | emu/cc        | 800                       |
| Vol 2           | m³            | π × 50n × 50n × 2n         |
| Exchange Field Coeff. | erg/cm² | 5                       |

**Exchange Coupling Module: Medium Hₖ PMA Magnet**
The FM-NM interface conductance values in our modules correspond to half the magnitudes reported in the literature, for instance see [?, ?]. $g_0 = 5 \times 10^{15}$ corresponds to the $Re(g_{\uparrow\downarrow}) = 2.5 \times 10^{15}$.