Design of a High Precision Data Acquisition System of Weak Signal

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Abstract. In order to solve the problem of high precision acquisition of weak signals, a high accurately weak signal acquisition system has been designed in this paper. According to the proposed design requirements of the data acquisition system, the hardware acquisition circuit and the drive circuit as well as the processing of the upper computer are divided into modules. As the central work of this paper, the hardware and software of the drive modules are designed with specific flowcharts are given. And the designs of the system were debugged, analyzed and tested through experiment tests, and the high precision data acquisition of 0.5V DC signal has been obtained with specific datum are provided. The effectiveness of the proposed design to data acquisition of weak signal has been validated by the experimental results, and this design could be used in engineering projects.

Keywords: Weak signal; Data acquisition system; Design.

1. Introduction

With the development of electronic technology and sensor technology, data acquisition systems have been widely used in military, radar system, aerospace and other fields[1]. Analog quantity such as the temperature, the pressure and the flow rate collected by the corresponding sensors are usually transformed into electrical signals which could then be utilized by the systems[2]. Data acquisition technology refers to the process of storing, processing and displaying of digital quantities achieved from electrical signals through AD transformation[3]. Different requirements will put forward different performance requirements for the data acquisition system, especially when the object of the acquisition system is microvolt level, which requires high dynamic range and wide frequency band, therefore, how to design a high precision data acquisition system of weak signal should be carefully considered[4-5]. The wider the frequency band and the greater the noise energy are the reasons why the accuracy and frequency band of the traditional data acquisition system are limited. Luckily, the adaptive filter can dynamically change the parameters of the filter for the adaptive algorithm can eliminate the impact of environmental changes[6-7]. Therefore, it is necessary to design the drive modules of the weak signal acquisition system, and then to test on its data exchange with the upper computer. The purpose of this work is to demonstrate the feasible method of the design of data acquisition system of weak signal, and the specific method proposed has been given in section 3 and section 4 as well as the experiment test has been done in section 5.

2. Overall Design of the Data Acquisition System

Based on the development of 24 bits weak signal acquisition system, the function index of this design has been introduced according to the demand of the data acquisition system, and then the overall...
system scheme has been designed according to the specific index, including the driving module of the hardware and the software as well as the software of upper computer. The overall design block diagram of the system is shown in figure 1.

![Diagram of system overall design](image)

**Figure 1.** The block diagram of system overall design.

The system workflows are as follows: At first, it is necessary to carry on the parameter configuration by the user in the upper computer, then to execute the self-inspection of hardware system. After then the instructions are transmitted to the FPGA (Field Programmable Gate Array) via ARM (Advanced RISC Machines) by clicking the start acquisition button to execute data acquisition. And the adjustable hardware narrowband filter is in a full-pass state in the beginning of data acquisition, then the digital signal collected by FPGA are stored in the SRAM (Static Random Access Memory). Subsequently, the instruction of the completion of data acquisition would be transmitted to ARM passed by digital signal, which then be transported to FPGA after reading. Meanwhile, the frequency of digital signal transported to the upper computer by the same way will be calculated through the adaptive frequency search link, which will be feedback to FPGA via ARM to complete the hardware narrowband filter settings. And then FPGA continue to collect signals, the steps are the same as above.

### 3. Hardware Design of Driver Module

The driving circuit is a data transmission hub of the whole system and an important link connecting the upper computer and the lower computer. The ARM chip is the control core of the drive circuit, which needs to complete the drive of the corresponding hardware module, so it is necessary to concern about many performances of ARM, including the clock frequency, the type of peripheral equipment, the accessible rate and the number of I/O etc. Considering the difficulty of development and the utilization of peripheral resources, the ARM chip of STM32F103ZET6, a 32-bit Cortex-M3 processor, has been adopted as control core in the driving module, which is specially designed for embedded applications with low cost and low power consumption, providing superior computing performance and excellent interrupt system.

As the hub of the acquisition module and the upper computer in the drive circle, it is responsible for STM32 to design the data transmission frame and to execute the data interaction between the upper computer and the data acquisition module. In order to improve the communication rate, STM32 should be driven by the corresponding peripherals separately. After the comparing of various communication protocols, the USB has been chosen as the communication mode between the upper computer and the lower computer, which has the advantages of high speed, excellent stability and small volume. The FT232H designed by FTDI company is a single channel bridging chip based on usb2.0, which runs at a rate of 480Mbps and has a very flexible interface, compatible for Serial or parallel interfaces. And FT232H comes with a EEPROM (Electrically Erasable Programmable Read-Only Memory) interface that can configure the FT232H to the required asynchronous or synchronous serial standard by PROG. Meanwhile, the chip handles the USB protocol without firmware programming, which greatly reduces the development difficulty and cycle. It also provides drivers for various operating systems, reducing the difficulty of upper computer development. In the parallel FIFO transmission mode, the asynchronous transmission rate can up to 8MB/s, and the synchronous transmission rate could as high as 40MB/s, which completely meet the demand of transmission rate of data acquisition system. Besides, there is 1KB sending and receiving cache in the FT232H, which simplifies the design of data
cache of upper and lower computers, and therefore we can pay more attention to the design of data frame format.

According to the above analysis, when the speeds of the two controllers are inconsistent, it is impossible to communicate in real time, and so it is necessary to design a buffer. The reading rate of memory chip is an important indicator of selection, and the sampling rate of ADC in acquisition module is 625KSPs, and each acquisition point is composed of 24-bit binary number and 8-bit state code, that is 32-bit together, as a result, the access rate needs to satisfy the following formula:

\[ v_1 = 625000 \times 32 / 8 / 2.5 \text{ MB/s} \]

(1)

The general Flash chip usually does not meet the demand of the rate in formula (1), so the 23LC1024 produced by Microchip company has been adopted, which is driven by 4-line system SPI, its clock signal line supports 20MHz rate, and its reading and writing type supports three modes: byte mode, page mode and sequence mode. The sequence mode which is the fastest one only need to write the first address, then to write each byte sequentially, where each clock represents one bit of data. In this case, the access rate is shown as follow:

\[ v_2 = 20 / 8 \text{ MB/s} \]

(2)

Through the above analysis, especially according to formula (1) and formula (2), it can be seen that the memory chip completely meets the requirements of reading and writing rate, and of course can be used as a buffer for data interaction between FPGA and STM32.

4. The Software Design of Driver Module and Upper Computer

4.1. Software Design of Driver Module

The main function of driver module software is data interaction, its overall functional architecture mainly includes data upload and reception of USB interface chip, communicating with upper computer about command analysis and data forwarding, reading and uploading of the datum of SRAM memory chip, and data interaction with FPGA acquisition module through the serial port.

4.1.1. Design of USB interface driver software and data frame. The CPU asynchronous FIFO mode has been selected among a multitude of modes of FT232H, which needs 8 data lines and 4 control command lines for communication. There are 1KB bytes for transceiver cache within the chip. It is imperative to setup CS pin and A0 pin to fulfill a certain of specific operations. The corresponding setups are shown in table 1:

| CS | A0 | RD | WR       |
|----|----|----|----------|
| 1  | X  | X  | X        |
| 0  | 0  | Read data pipeline | Write data pipeline |
| 0  | 1  | Read status | Immediately dispatch |

It is obviously shown that the data sent from the upper computer would directly dispatch to the cache in table 1, and it is need to visit the cache to decide weather there is data or not, then to make a decision on the successive operation. However, there are only lower 4 bits of the 8-bit state code that have physical significance, where the 0th bit is 1 means that there are datum in the receiving cache, and when the first bit is 1 standing for there is remaining space in the sending cache, and the second bit represents whether the current chip is suspended or working.

4.1.2. Design of SRAM driver software. The storage capacity of 23LC1024 memory chip selected in this design has 1Mbits, providing three kinds of communication interfaces set through its internal mode register, that is SPI (Serial Peripheral Interface), SDI (Serial Digital Interface) and SQI (Serial Quad Interface) respectively. And it is because STM32 embedded with SPI peripherals that we choose SPI as default mode generally. For there are 1Mbits of storage capacity, that is 128K bytes, and each byte has been addressed, the highest one is 1FFFF, divided into 32 bytes page. And there are three
kinds of read modes, including byte mode, page mode and sequence mode, among of which the fastest read one is the sequence mode, it is only necessary to write the initial address, then the internal address counter increase one by one automatically, avoiding writing addresses each time. The control flow of SRAM is shown in figure 2.

![Figure 2. The control flow chart of SRAM.](image)

There are two memory chips adopted in this design, that is because every digital signal consists of 24 bits digital signal and 8 bits state code, which add up to 32 bits, therefore the high 16 bits would be written into the first block, and the low 16 bits would be written into the second block. And every sample data would be read twice for high sampling rate. When both chips are read, they will be encapsulated into a frame written into FT232H, processed by the upper computer.

### 4.2. Upper Computer Software Design

#### 4.2.1. Design of USB driver module.

FT232H of the USB bridge chip comes with firmware program, providing drivers of various operating systems, and the drivers act as the links between the lower computer firmware program and the upper computer application program.

The communication relationship between the upper computer and the lower computer is master-slave, that is the upper computer actively transmits the data downward and the lower computer receives the data passively, which avoids the trouble of increasing difficulty raised from interaction between the two sides. Data downward transmission is performed by a separate child thread, and the flow chart for performing data downward transmit is shown in figure 3.

![Figure 3. The flowchart of data downward transmission.](image)

According to figure 3, the downward transmitted data thread continuously traverses the instruction array. When a downward transmitted instruction is detected, the address of the instruction, the length of the instruction and the data brought by the instruction are saved firstly, the total length of the three mentioned above is calculated, which acts as a parameter passed into the FT_Write function and would be called to pass down the instruction. After then, it is necessary to wait for the reply data frame sent by the lower computer to safely read the value of instruction array through the lock protection mechanism. When it is 0X00, representing the successful receipt of the reply data frame, and the index
value of the instruction array is assigned to the initial value of 0XFF and the lock is released at the same time. If it is 0X01 which means that the sum check is failure and the instruction needs to be re-delivered. If the initial value is 0XFF that the lower computer has not uploaded the response frame, it needs waiting and to read the instruction array again, if the waiting time exceeds the maximum setting time, it shows that the data frame style is wrong, which mean that the instruction parsing fails, and the instruction needs to be retransmitted.

4.2.2. Interactive module design. The string class control and command button control are mainly used in the upper computer software, where the string control is used to type user name and password information, and there are three command buttons, which are registration button, login button and exit button separately. When the user inputs the account information, then clicks the login button to complete the information verification, and enter the main interface of the software. If the verification does not pass, the error prompt information will show up needed re-entering. The Verified logic code is written in the callback function of the login button. It is necessary for those who first use the software to register, and the registration logic is written in the registration button callback function.

5. Experiment Test
After the design of each module of the acquisition system has been completed, it is necessary to test each module of the system to ensure that the acquisition system could work normally.

5.1. USB Interface Chip Debugging
It is the USB interface chip that completes the data interaction between the STM32 and the upper computer. After the upper computer configured the interface chip, asynchronous FIFO mode, it could be debugged normally. When STM32 sends the frame to the upper computer, the upper computer program would be executed by the way of breakpoint in the Labwindows/cvi, placing the received data in one array and checking the data frame through variable. The input 0.5V DC signal has been selected as the debugging signal input in the low-frequency band of 0-9 KHz. After cutting the four points into 24 bits, the calculated voltage data is shown in Table 3.

According to Table 2, the conversion voltage is not calibrated, and there is a certain deviation from 0.5V. However, the correctness of the data of data upload frame could be completely guaranteed by the data in the table.

| Table 2. Binary complement conversion table for digital signals |
|---------------------------------------------------------------|
| Sequence | 24 bits AD Complementary code | decimal | conversion voltage |
|----------|--------------------------------|---------|-------------------|
| 1        | 0F9C66                         | 1023078 | 0.49954986        |
| 2        | 0F9CB3                         | 1023166 | 0.49959283        |
| 3        | 0F9B6A                         | 1022826 | 0.49942681        |
| 4        | 0F9B9D                         | 1022923 | 0.49947418        |
| 5        | 0F9C2F                         | 1023023 | 0.49952300        |
| 6        | 0F9BE8                         | 1022952 | 0.49948834        |
| 7        | 0F9B91                         | 1022865 | 0.49945856        |
| 8        | 0F9CAC                         | 1023148 | 0.49958404        |
| 9        | 0F9CA2                         | 1023002 | 0.49951275        |
| 10       |                                | 1023138 | 0.49957916        |

5.2. SRAM Memory Chip Debugging
The STM32 executed by the way of breakpoints, and the datum of SRAM has been read by checking the variable, which has been completed by reading the head address of the two memory chips shown in table 3 and table 4 when the input 0.5V DC signal has been selected as the input data. According to the head address of series of 12 datum in the two SRAM chips, it has been illustrated that the higher 16 bits of the sampling data stored in the first block and the lower 8 bits combined with the state code 0X80 stored in the second block, corresponding to the style of sample data of FPGA, and the single-direction of data flow between FPGA and STM32 has been verified.
Table 3. SRAM1 Stored byte sequences

| address | data   | address | data   | address | data   | address | data   |
|---------|--------|---------|--------|---------|--------|---------|--------|
| 0X00    | 0X0F   | 0X03    | 0X9C   | 0X06    | 0X0F   | 0X09    | 0X9B   |
| 0X01    | 0X9B   | 0X04    | 0X0F   | 0X07    | 0X9C   | 0X0A    | 0X0F   |
| 0X02    | 0X0F   | 0X05    | 0X9C   | 0X08    | 0X0F   | 0X0B    | 0X9B   |

Table 4. SRAM2 Stored byte sequences

| address | data   | address | data   | address | data   | address | data   |
|---------|--------|---------|--------|---------|--------|---------|--------|
| 0X00    | 0X48   | 0X03    | 0X80   | 0X06    | 0XB6   | 0X09    | 0X80   |
| 0X01    | 0X80   | 0X04    | 0X94   | 0X07    | 0X80   | 0X0A    | 0X4E   |
| 0X02    | 0XAC   | 0X05    | 0X80   | 0X08    | 0X73   | 0X0B    | 0X80   |

6. Conclusion

In this paper, a high precision acquisition system of weak signal is designed. According to the design requirements of the data acquisition system, the hardware acquisition circuit, the driving circuit and the processing of the upper computer are divided into modules, accomplishing the design of hardware and software of the driving module, realizing the transmission and intercommunication of data in the system. At the same time, the upper computer is also divided into modules realizing the design functions. Finally, the design of this paper is debugged, analyzed and tested. And the experimental results show that the system designed in this paper can meet the design requirements and realize the high precision acquisition function of weak signals.

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