Nanoscale Electrostatic Confinement at Oxide Interfaces

Srijit Goswami, Emre Mulazimoglu, Lieven M. K. Vandersypen, and Andrea D. Caviglia
Kavli Institute of Nanoscience, Delft University of Technology,
P.O. Box 5046, 2600 GA Delft, The Netherlands

We develop a robust and versatile platform to define nanostructures at oxide interfaces via patterned top gates. Using LaAlO$_3$/SrTiO$_3$ as a model system, we demonstrate controllable confinement of electrons to nanoscale regions in the conducting interface. The excellent gate response, ultra-low leakage currents, and long term stability of these gates allows us to perform a detailed study of devices in a split-gate geometry. Electrical transport through such devices displays a distinct threshold associated with depletion directly below the gates, resulting in the formation of a narrow conducting channel even at room temperature. We examine the effects of cross-talk between the gates, and also show that a combination of top gates and back gate can be used to efficiently modulate charge transport through these nanostructures.

Transition metal oxides have been studied for decades, but continue to reveal fascinating and unexpected physical properties that arise from their highly correlated electrons [1]. Propelled by recent developments in oxides thin film technology it has now become possible to create high quality interfaces between such complex oxides, which reveal a new class of emergent phenomena often non-existent in the constituent materials [2, 3]. In particular, there has been a growing interest in interfaces which host a conducting two dimensional electron system (2DES) [4, 5]. This 2DES has been shown to support high mobility electrons [6, 7], magnetism [8] and superconductivity [9]. In addition to this inherently rich phase space, in-situ electrostatic gating can be used not only to alter the carrier density [10], but it can significantly change the spin-orbit coupling (SOC) [11, 12] and even drive transitions from a superconducting to an insulating state [13].

Bulk transport studies of oxide interfaces have played an important role towards building a better understanding of these new material systems. However, it is becoming increasingly evident that in order to fully grasp the details of the complex coexisting phases at the interface, one must probe the system at much smaller length scales. Recent scanning probe experiments have indeed clearly demonstrated that the electronic properties of the interface can change dramatically over microscopic length scales [14, 15]. In this context, nanoscale electronic devices could provide direct information on how such strong local variations in physical properties affect mesoscopic charge transport. Perhaps even more exciting is the possibility of discovering and manipulating new electronic states that are predicted to arise from the interplay between confinement, superconductivity and SOC [17]. Furthermore, the ability to locally drive phase transitions at the interface could potentially yield technologically relevant oxide-based nano-electronic devices with novel functionality.

Existing methods for confinement at the interface involve some form of nanoscale patterning, which renders selected portions of the interface insulating, while others remaining conducting. These include the use of pre-patterned masks [18], physical etching of the interface [19], and AFM-based lithography [20, 22]. These techniques have shown promising results but suffer from issues of ion-beam induced damage and long term stability, which could have a direct impact on device performance. Such problems can be circumvented by the use of local top gates, which can be conveniently integrated with several oxide interfaces where the top oxide layer itself acts as a high quality gate dielectric. Furthermore, in this device architecture the potential profile in the 2DES can be precisely controlled using appropriate gate voltages, thus making it an extremely flexible and robust platform to build tailor-made nanostructures. Such electrostatic confinement is routinely employed to create low dimensional systems in traditional semiconductor based 2DESs. It is therefore somewhat surprising that a similar strategy has not been adopted to investigate confinement at oxide interfaces thus far. Despite sustained efforts towards making large area top-gated devices in oxides [20, 22], scaling these structures down has remained a challenge.

Here, we define nanoscale electronic devices in LaAlO$_3$/SrTiO$_3$ (LAO/STO) using patterned top gates which efficiently modify the potential landscape at the metallic interface. We demonstrate that individual narrow gates (down to 200 nm) can completely pinch off the conducting channel and display large on/off ratios with negligible leakage currents. Using two such gates in a split-gate geometry, we can further tune the flow of charge carriers by restricting them to narrow conducting channels. The excellent stability of these gates allows us to study the effects of cross-talk between them by mapping out the conductivity as a function of the individual gate voltages. Finally, we demonstrate that a combination of such split gates and a global back gate can be used to further control electrical transport through the channel.

Device fabrication involves pulsed laser deposition for the oxide growth in combination with multiple aligned lithography steps (see SI for device specific details).
Single crystal STO (001) substrates first undergo photolithography or electron beam lithography (EBL), followed by the deposition of 45 nm of amorphous LAO (a-LAO). The a-LAO is deposited at room temperature with an O$_2$ pressure of $6 \times 10^{-5}$ mbar and laser fluency of 1 J/cm$^2$ (repetition rate: 5 Hz). Subsequent lift-off in warm acetone creates an a-LAO mask for the crystalline LAO (c-LAO) deposition. We deposit 12 unit cells of c-LAO at 770 °C with an O$_2$ pressure of $6 \times 10^{-5}$ mbar and laser fluency of 1 J/cm$^2$ (repetition rate: 1 Hz). The film growth is monitored in situ using reflection high-energy electron diffraction (RHEED) confirming layer by layer growth. Finally, a one hour long post-growth anneal is performed at 300 mbar O$_2$ pressure and 600 °C, followed by a cooldown to room temperature in the same atmosphere. Under these conditions the 2DES formed at the LAO/STO interface shows sheet densities of about $3 \times 10^{13}$ cm$^{-2}$ and field effect mobilities up to 3500 cm$^2$/Vs. The patterned top gates are finally defined by an aligned EBL step, followed by electron beam evaporation of 100 nm Au directly on the c-LAO surface.

Figure 1 shows a cross-sectional schematic of a device with a single top gate. An optical image of such a device is shown in Figure 1b, where a narrow (1 μm wide) gate runs across a mesoscopic conducting channel defined at the LAO/STO interface. Figure 1c shows the gate characteristics of this device (Dev1) at 300 K (see SI for details). A constant dc voltage bias of 10 mV is applied across S and D ($V_{sd}$) and the current ($I_{sd}$) is measured as a function of the top gate voltage ($V_{gate}$). The black curve (left axis) shows a typical field effect behavior with complete depletion under the gated region resulting in an on/off ratio of nearly 1000 (shown in the inset). The leakage current (blue trace, right axis) remains below 5 pA in this gate voltage range, thus allowing for reliable measurements of very low currents through the device. The gate width can be reduced even further (in this case to 200 nm), as seen in the (false color) scanning electron microscope (SEM) image of Dev2 (Figure 1d). In Figure 1d we compare the gate response of Dev1 and Dev2 at $T = 2$ K. Both devices (Dev1-black trace, right axis; Dev2-red trace, left axis) show comparable threshold voltages. This is consistent with the fact that they were both fabricated on 12 unit cell LAO deposited under the same growth conditions. We note that each curve consist of 10 consecutive sweeps between the on and off states. It is clear that the device completely recovers from the insulating state, and is extremely stable over multiple on/off cycles. This is in contrast with recent measurements on bulk top gated LAO/STO devices where (at low temperatures) going above a critical resistance rendered the interface completely insulating, and conduction could only be revived by thermal cycling [24]. The ultra-low leakage currents and absence of severe hysteretic effects may be related to the fact that our gate area is significantly smaller than previous studies [24, 25].

Having established a reliable gate response from our local top gates we use two such gates to realize a split gate (SG) geometry, using which charge carriers can be confined to narrow conducting channels. SGs have been successfully used to fabricate quantum point contacts (QPCs) in semiconductor-based 2DESs [27, 28], and have provided insights into several aspects of mesoscopic physics (reviewed in [29]) ranging from the quantum Hall effect to the Aharonov-Bohm effect. They are also extremely sensitive charge detectors [30] and spin filters [31], and serve as essential components for the creation of lower dimensional systems such as quantum dots [32]. At the LAO/STO interface, such one-dimensional (1-d) confinement could possibly give rise to exotic electronic states that emerge from the interplay between 1-d superconductivity and SOC [17]. Figure 2a shows an optical micrograph of a SG device on LAO/STO. It consists of a left (L) and right (R) gate, both of which start off 2.5 μm wide and taper down to...
FIG. 2: (a) Optical and (b) SEM images of a split gate (SG) device which comprises of a left (L) and right (R) gate. (c) Four-probe resistance ($R_{4p}$) measurements (at 300 K) comparing the gate action of the individual gates (red and blue curves) with that of both gates together (black curve). Note that the red and blue curves show an excellent overlap, which makes it hard to distinguish between the two in the plot. The labels [(i)-(iv)] mark different transport regimes in the operation of the SG device. The corresponding density variations at the LAO/STO interface are shown schematically in (d), where black/gray represent conducting/insulating regions in the 2DES. (e) Two-probe voltage biased measurements: $I_{sd}$ vs. $V_{L&R}$ at 300 K (black curve) and 4.2 K (red curve).

a narrow point. Figure 2(b) shows an SEM image of the active device region. We have studied devices with tip separations of approximately 400 nm (Dev3) and 250 nm (Dev4), and both show qualitatively similar features. Here we focus on Dev3 (results from Dev4 can be found in the SI).

We begin by studying the room temperature four probe resistance ($R_{4p}$) across the SG, as a function of the individual (L, R) gates. A 100 nA dc current is applied between S and D ($I_{sd}$), and resistance is measured between contacts P1 and P2 (see Figure 2). For these measurements no back gate voltage was applied. When the SG is held at zero ($V_L = V_R = 0$), the carrier density in the entire channel is uniform. This is shown schematically in Figure 2b (top panel), where the uniform black area represents a wide channel with no density variations. The corresponding point in the $R_{4p}$ vs $V_{gate}$ plot (Figure 2c) is marked by the label (i). As one of the gates (say L) is made more negative, the carriers below this gate are depleted, resulting in a sharp increase in $R_{4p}$ (red curve). However, at a critical threshold voltage ($V_{th}$) the region below R is completely depleted, indicated by (ii) in Figure 2c,d (gray areas represent depleted regions in the 2DES). Throughout, we define $V_{th}$ as the gate voltage where the magnitude of this slope is maximum. Beyond $V_{th}$ the gate action is weaker, since depletion must now occur sideways, thereby resulting in a lower slope in the $R_{4p}$ vs. $V_{gate}$ curve. Sweeping only L (instead of R) should be electrostatically equivalent to the situation described above. This is reflected directly in transport by the excellent overlap between the red and blue curves. If both R, L are swept together the response is much stronger (black curve). When $V_L = V_R = V_{th}$ [label (iii)] a narrow constriction is formed in the 2DES, whose width is determined by the geometry of the split gates and the electrostatics of the system. Finally, going to even more negative voltages with L and R together [label (iv)] squeezes this channel further. Thus, through an appropriate device design and suitable gate voltages, it is clearly possible to electrostatically define nanoscale constrictions at an oxide interface, even at room temperature.

Next, we study these SG devices at cryogenic temperatures. Figure 2(e) shows the variation of the current through the channel ($I_{sd}$) with $V_{L&R}$ (i.e., both L and R swept together) at 300 K (black curve, left axis) and 4.2 K (red curve, right axis). These (and all subsequent measurements) have been performed in a two probe configuration, with a constant source-drain bias ($V_{sd} = 1$ mV). Two things are immediately apparent from these plots. Firstly, the conductivity of the system increases significantly as the temperature is lowered, which is expected for such metallic samples. Secondly, $V_{th}$ shifts to less negative voltages upon cooling down. It has been suggested that the sheet density can reduce with temperature as a result of carrier freeze-out [7]. Such a reduction in the sheet density with temperature could qualitatively explain the observed shift in $V_{th}$, since it now becomes much easier for the SG to deplete the carriers. However, at these temperatures an even more striking effect appears in the gate response of the SGs, which only becomes apparent through detailed phase space maps of the conductance vs. the individual gates.

Figure 2a,b show two such maps of $I_{sd}$, at 300 K and 4.2 K respectively. It is worth pointing out that these maps are typically acquired over several hours, during which the device does not show any switches or obvious drifts, confirming the stability and robustness of these gates. Furthermore, both gates (L and R) have a nearly identical influence on the 2DES at the interface. This is evident from the high degree of symmetry across the diagonal (white dashed line). The entire phase space can be
The maximum in the voltage for either gate, with the other held at zero. Symmetry about the white dashed line indicates comparable gate action from both L and R. (c) & (d) show plots of the corresponding numerical derivatives taken along the VR axis (dI/dVR). The maximum in dI/dVR indicates the threshold voltage for gate R. It is independent of V_L at 300 K, but shows a distinct shift at 4.2 K, indicating cross-talk between L and R at low temperatures.

divided into two distinct regions. The blue portion (lower I_{sd}) corresponds to a situation when both L and R have been driven beyond their respective threshold voltages. The red area (higher I_{sd}), thus reflects the complementary scenario, where either one (or none) of the gates have crossed V_{th} (black circles indicate the position of V_{th} for each of the gates with the other held at zero). The narrow white band therefore separates these two electrostatically distinct regimes and provides information about the effective region of influence of the individual gates, and the extent of cross-talk between them. These effects can be examined in a more consistent manner by taking a derivative along one of the gate axes.

Figure 3c,d show the corresponding numerical derivatives taken along the VR axis (dI/dVR). As mentioned earlier, the maximum in dI/dVR occurs at V_{th} associated with gate R. At 300 K, as V_L is made more negative the position of the threshold does not change, indicating that there is practically no cross-talk between the gates. This is perhaps not so surprising considering the fact that the gates are very close (~5 nm) to the interface, and therefore most of the electric field lines go directly downwards, creating a sharp potential profile with minimal spreading of the electric field. However, at 4.2 K the situation is rather different. V_L obviously has a distinct effect on the threshold voltage for R, shifting it to less negative voltages, as V_L becomes more negative. This suggests that V_L has a significant influence on the region below R, in contrast with the observations at 300 K. Such a modification of the electrostatics could possibly be related to the fact that STO is an incipient ferroelectric, thereby exhibiting a strong increase in its dielectric constant at low temperatures [33]. A combination of this large dielectric constant (~10^4 at T = 4 K) along with imperfect screening from the 2DES, could provide a viable mechanism for the observed cross-talk between the gates. As the carrier density below L is reduced, the extent of screening from the 2DES below L reduces. This, in turn, allows electric field lines to go through the STO, resulting in a significant field effect in the region below R. Though a likely explanation, the feasibility of such a scenario ultimately needs to be tested using electrostatic simulations with appropriate parameters for the screening lengths at the LAO/STO interface.

In addition to local top gates, the global back gate can also modify the electrostatics at the interface, thus providing additional control over transport through electrostatically defined nanostructures. Though our SG devices show clear evidence of confinement, the relatively large separation between the gates (as compared to the distance of the gates from the 2DES) makes it difficult to pinch off the channel using just the top gates. However, by reducing the sheet carrier density via moderate negative voltages on the back gate (BG), we could indeed deplete the constriction completely, as seen in Figure 4 At V_{BG} = 0 V the channel remains fairly open in this case.
gate voltage range (blue trace), but shows a clear pinch-off for $V_{BG} = -10.8$ V (red trace). We note that in all the devices studied here, we observed a strong hysteresis in the BG action at low temperatures. As the BG is taken to positive values, $I_{sd}$ typically saturates for $V_{BG} > 20$ V. Subsequently, going back to $V_{BG} = 0$ V renders the sample highly insulating. Such an effect was not observed in larger Hall bars (channel width $\sim 500 \mu m$), fabricated in a similar fashion, but without top gates. This suggests that the effect is related either to the significantly narrower channel widths of these devices ($\leq 10 \mu m$) or to the presence of the top gate itself. However, the exact origin of this hysteresis is unclear at the moment.

In conclusion, we have demonstrated that top gating can be used to successfully create electrostatically confined nanostructures at the LAO/STO interface. These gates show excellent performance and stability from room temperature down to cryogenic temperatures. The inherent flexibility in the design of such top-gated structures opens up a new and versatile platform for creating a variety of gate-tunable nanostructures at oxide interfaces.

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* Electronic address: s.goswami@tudelft.nl

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SUPPLEMENTARY INFORMATION

Figure S1a shows a complete flowchart of the various steps involved in the fabrication of the devices discussed in the main text (Dev1, Dev2, and Dev3) as well those discussed later in the supplementary information. Bold black arrows show the process flow used to fabricate the split gate (SG) device discussed in detail in the main text (Dev3). Figure S1b shows optical images of Dev3 at different stages of the device fabrication corresponding to labels [(i)-(iii)] in Figure S1a. The blue/red arrows correspond to Dev1/Dev2 respectively. Dev4, Dev5 and Dev6 (described in Figure S2) are fabricated in a similar fashion to Dev3, Dev1, and Dev2 respectively.

FIG. S1: (a) Device fabrication flowchart (see text for details). (b) Optical microscope images for Dev3 at various different stages of the fabrication process corresponding to labels (i)-(iii) in (a). The differences in colors between the three images are only a result of different camera settings, and not related to the processes themselves.
Below we describe each of the processes in some detail.

- **Photolithography (PL):** PL is performed using a deep-UV Karl Suss MJB3 mask aligner. The sample is coated with S1805 photoresist followed by UV exposure.

- **Electron beam lithography (EBL):** To prepare the sample for EBL, it is typically coated with a positive resist (double layer: PMMA 495K/950K). For Dev3/Dev4 we used a combination of PMMA 495K and HSQ (negative resist) to define the amorphous LAO (a-LAO) mask. For all EBL steps, the sample is also coated with Aquasave (Mitsubishi Rayon). Aquasave is a water soluble conducting polymer which prevents charging during the lithography process. After lithography, the Aquasave is first dissolved in water, before proceeding with developing.

- **Tungsten (W) sputtering:** In order to do well aligned EBL it is necessary to have good quality markers that can survive the high temperatures during the crystalline LAO (c-LAO) growth. We therefore make use of W [see Figure S1b-(i)], which is deposited using RF-sputtering.

- **Oxygen plasma etching:** This step is only required if a double layer of PMMA/HSQ was used to define the a-LAO mask. After exposure of the HSQ the oxygen plasma is used remove the PMMA from the unexposed regions. The etching is performed with an RF power of 60 W and oxygen flow rate of 40 sccm for 1 minute.

- **Oxides growth:** The details for a-LAO and c-LAO growth have been described in the main text.

- **Argon (Ar) ion milling:** Ion milling is used to drill holes that reach the LAO/STO interface. This is followed by in-situ metal deposition, resulting in good ohmic contacts to the interface. The milling is performed in the load lock of the deposition chamber with an Ar pressure of $1 \times 10^{-3}$ mbar.

- **Metal deposition:** All metals are deposited by electron beam evaporation. Ti/Au (20 nm/50 nm) is deposited after Ar ion milling to make ohmic contacts (in devices where no milling was performed, contacts were made by direct wedge bonding to the interface). For the top gates, only Au (100 nm) was evaporated. The deposition rate was kept low (0.5 Å/s) for the first 20 nm after which it was increased to about 2-3 Å/s.

- **Liftoff:** Post-deposition liftoff (a-LAO, W, Ti/Au, and Au) is usually performed in warm acetone (55 °C). The process can be sped up by putting the samples in an ultrasonic (US) bath. However, after the top gate deposition (Au) this is avoided in order to prevent the Au from peeling off.
FIG. S2: (a) Gate characteristics of a 5 µm wide single gated device (Dev5). (b) 2D map of the current for a device (Dev6) with two gates in series. Inset shows an optical image of the device. (c) Red/black correspond to individual traces taken along the positions marked by red/black arrows in (b). (d) Gate response of a split gate device (Dev4) similar to Dev3, described in the main text. Inset shows SEM image of the device. (e) 2D map of the four-probe resistance ($R_{4p}$) vs. the left (L) and right (R) gate voltages for Dev4. (f) Absolute value of the derivative of (e) along the $V_R$ axis.

Figure S2 shows data from three other devices that complement the results described in the main text. Figure S2 inset shows a device (Dev5) with a 5 µm wide gate across the conducting channel. The device characteristics are very similar to those of Dev1 (described in main text), in terms of the on/off ratio and leakage current. We also study transport through a device with two gates in series (Dev6). The 2D current map in Figure S2 shows that the two gates act independently of one another, with no cross-talk. Figure S2 shows individual traces taken along the positions marked by the red/black arrows in Figure S2. It can clearly be seen that a more negative value of $V_{G1}$ merely reduces the overall conductance of the channel, without affecting the pinch-off voltage for gate G2.

In addition to the split-gate device discussed in the main text (Dev3), we study another device (Dev4) in the same geometry, with a gate separation (tip to tip) of about 250 nm. Figure S2 shows the room temperature variation in four-probe resistance ($R_{4p}$) with just the left gate (L), right gate (R), and both together (L&R). Inset shows a (false color) SEM image of the device. A comparison with Figure 2b (main text) shows qualitatively similar behavior to Dev3, however there is some asymmetry in the action of L and R. This is most likely a result of some local inhomogeneity in the device region. Figure S2 shows a 2D map of $R_{4p}$ vs. $V_L$, $V_R$. Both the $R_{4p}$ map and the derivative along $V_R$ (Figure S2) look very similar to Dev3 (main text), indicating minimal cross-talk between the gates.