Bias-Dependent Intrinsic RF Thermal Noise Modeling and Characterization of Single-Layer Graphene FETs

Nikolaos Mavredakis©, Anibal Pacheco-Sanchez©, Paulius Sakalas, Wei Wei, Emiliano Pallecchi©, Henri Happy©, Member, IEEE, and David Jiménez©

Abstract—In this article, the bias dependence of intrinsic channel thermal noise of single-layer (SL) graphene field-effect transistors (GFETs) is thoroughly investigated by experimental observations and compact modeling. The findings indicate an increase of the specific noise as drain current increases, whereas a saturation trend is observed at very high carrier density regime. Besides, short-channel effects, such as velocity saturation (VS) also result in an increment of noise at higher electric fields. The main goal of this work is to propose a physics-based compact model that accounts for and accurately predicts the above experimental observations in short-channel GFETs. In contrast to long-channel MOSFET-based models adopted previously to describe thermal noise in graphene devices without considering the degenerate nature of graphene, in this work, a model for short-channel GFETs embracing the 2-D material’s underlying physics and including a bias dependence is presented. The implemented model is validated with deembedded high-frequency data from two short-channel devices at quasi-static (QS) region of operation. The model precisely describes the experimental data for a wide range of low-to-high drain current values without the need of any fitting parameter. Moreover, the consideration of the degenerate nature of graphene reveals a significant decrease of noise in comparison with the nondegenerate case and the model accurately captures this behavior. This work can also be of utmost significance from the circuit designers’ aspect since noise excess factor, a very important figure of merit for RF circuits implementation, is defined and characterized for the first time in graphene transistors.

Index Terms—Bias dependence, compact model, excess noise factor, graphene transistor (GFET), intrinsic channel, thermal noise, velocity saturation (VS).

I. INTRODUCTION

GRAPHENE field-effect transistors (GFETs) have been shown to exhibit significant extrinsic maximum oscillation (fmax) and unity-gain (fT) frequencies with fT ≈ 40 GHz and fmax ≈ 46 GHz for SiO2 substrate devices [1] and fT ≈ 70 GHz and fmax ≈ 120 GHz for devices with SiC substrate [2]. This promising performance despite the still early stage of the technology is mainly due to the extraordinary intrinsic characteristics of graphene, e.g., high carrier mobility and saturation velocity, leading circuit designers to consider these devices for analog RF applications whereas the lack of bandgap makes GEFTs unsuitable for digital circuitry [3]. Among such analog RF circuits [4]–[8], a low noise amplifier (LNA) [7], [8] is a key circuit for receiver front-end systems. Hence, understanding of high-frequency noise (HFN) in short-channel GFETs is of great importance and shall be modeled precisely.

In this study, we focus on intrinsic channel drain current noise, generated from the local random thermal fluctuations of the charge carriers, resulting in velocity fluctuations (v2) and diffusion noise. For the two-port noise representation, the channel thermal noise fluctuations should be calculated as drain current noise spectral density (Sd). Under quasi-static (QS) conditions quite below fT [9], channel thermal noise is independent of frequency. First, works on a thermal noise analysis in FETs were reported several decades ago [10]–[12], whereas a long-channel compact model was first proposed by Tsividis [13, (8.5.21)]. Short-channel related effects were shown to increase Sd [14], and to account for this, physics-based compact models embracing velocity saturation (VS) effect were developed for CMOS devices [15]–[21].

A limited number of works dealing with the HFN characteristics of GFETs are available in the literature [22]–[27]. In order to improve the understanding of noise behavior and enhance further the technology, a reliable description of Sd is required. Up to now, simple long-channel empirical models taken from MOSFETs are used to describe Sd in fabricated GFETs [23], [24], [27], which neither considers the degenerate nature of graphene and its effect on noise [28]–[30] nor

Digital Object Identifier 10.1109/TMTT.2021.3105672

0018-9480 © 2021 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See https://www.ieee.org/publications/rights/index.html for more information.
the behavior of noise at different operating conditions. Thus, the main objective of this study is the development of a physics-based compact model for $S_{1D}$ of single-layer (SL) GFETs, which accounts both for the noise bias dependence including the VS effect and the degenerate nature of graphene. The approach presented here is based on an already established chemical-potential-based model, describing the GFET IV and small-signal and $1/f$ noise characteristics [31]–[33]. To our knowledge, this is the first time that such a complete $S_{1D}$ model is proposed and validated with experimental data of short-channel GFETs [34] without the need of any fitting parameter, after appropriate deembedding procedures for both $Y$-parameters [35], [36] and noise data [37], [38]. In Section II, the devices under test (DUT) and the HFN measurement setup are described in detail, while in Section III, the derivation of the $S_{1D}$ model is presented thoroughly. Finally, in Section IV, the behavior of both the model and experiments versus bias is presented where apart from the power spectral density (PSD) of noise, the significant—from circuit designers’ point of view—excess noise factor parameter $\gamma$ [12], [39] and the intrinsic noise resistance $R_{\text{INT}}$ [40] are also shown for the first time in GFETs.

II. DUT AND MEASUREMENT SETUP

Two SL short-channel aluminum back-gated CVD GFETs fabricated on a 300-nm-thick SiO$_2$ followed by 40-nm Al deposition and liftoff process were characterized in this study with a $\sim$4-nm-thick Al$_2$O$_3$ used as a dielectric layer between graphene and gate. The total width was $W = 12$ $\mu$m $\times 2$ $\mu$m $= 24$ $\mu$m$^2$ (where 2 is the number of gate fingers) and gate length $L = 200$ nm (EG5) and $L = 300$ nm (EG8). More details on GFET fabrication can be found elsewhere [34]. On-wafer $S$-parameters and ac standard characteristics (EG8). More details on GFET fabrication can be found elsewhere [34]. On-wafer dc and ac standard characteristics ($S$ ($Y$)$_{\text{DUT}}$) have been measured with a PNA-X N5247A and a Keysight HP4142 Semiconductor Parameter analyzer. Noise parameters (HFN$_{\text{DUT}}$) in source-load matching conditions have been measured using the corrected $Y$-factor technique with a Maury Microwave automated tuner system ATS 5.21 and impedance tuner MT982. Gate voltage $V_{GS}$ was swept from GS matches $g_m$ for both GFETs under test versus $V_{DS}$ at 1 GHz for both EG5 and EG8 GFETs. P-type operation region for $V_{GS} \leq 0.7$ V (EG5) and 0.8 V (EG8). All data in (a)–(d) reported at $V_{DS} = 0.5$ V.

where $K_B$ is Boltzmann’s constant and $T_0$ is the standard reference (290 K) [16] temperature. Notice that only $Y_{21\text{INT}}$ and $R_{\text{INT}}$ are required to extract $S_{1D}$ from experimental data. Fig. 1(a) and (b) shows the measured $S_{\text{DUT}}$ parameters in a Smith chart at $V_{GS} = -0.5$ and 0.5 V and $V_{DS} = 0.5$ V for frequencies from 0.8 to 8.4 GHz for EG5 and EG8 GFETs, whereas Fig. 1(c) and (d) shows $Y_{21\text{DUT,DEV,INT}}$ and $R_{\text{DUT,DEV,INT}}$, respectively, versus $V_{DS}$ for the same DUTs and $V_{GS}$ where the contribution of $R_c$ and $R_G$ (EG5: $R_G = 18$ $\Omega$ and EG8: $R_G = 12$ $\Omega$) to $R_{\text{INT}}$ is significant.

To ensure that the IV model [31], [32] describes accurately the dc operating point at HF operation, the former is validated with $S_{\text{DUT}}$, i.e., the transconductance $g_m$ of the device measured through the HF setup. A model parameter embracing defects affects and the initial state of traps at different lateral fields [43], i.e., a trap-induced hysteresis, has been considered here. Trap-affected performance of the technology used here has been described elsewhere [43] using the same model. Fig. 2 shows the modeled and measured $g_m$ for both GFETs under test versus $V_{GS}$ at $V_{DS} = 0.5$ V. The model agreement with $S_{\text{DUT}}$ is precise, especially in the p-type region, cf. Fig. 2. In this study, we focus on the p-type region where maximum $g_m$ is recorded due to data asymmetries induced by dissimilar mobility and/or contact resistance between p- and n-type regions [33], cf. Figs. 1(c) and 2. The p-type region is defined for $V_{GS} \leq 0.7$ and $\leq 0.8$ V for EG5 and EG8, respectively, as shown in Fig. 1(c). $g_m$ data obtained from the derivative of drain current $I_D$ w.r.t $V_{GS}$ matches $g_m$ (ac), as shown in Fig. 2. The extracted model parameters for both GFETs are listed in Table I where $\mu$ is the carrier mobility, $C_{\text{back}}$ is the back-gate capacitance, $V_{\text{BEO}}$ is the flat-band voltage, $R_c$ is the contact resistance, $\Delta$ is the
and lines the model for (a) EG5 and (b) EG8 GFETs for \( V_{GS} \) model definitions, see [41, SI, Sec. B].

Fig. 2. Transconductance \( g_m \) versus \( V_{GS} \) with markers representing the measurements (red: IV data and purple: \( Y \) parameters data at \( f = 1 \) GHz) and lines the model for (a) EG5 and (b) EG8 GFETs for \( V_{GS} = 0.5 \) V.

### TABLE I

| Parameter          | Units | EG5  | EG8  |
|--------------------|-------|------|------|
| \( \mu \)          | cm\(^2\)/Vs | 200  | 170  |
| \( C_{inv} \)      | \( \mu F/cm^2 \) | 1.87 | 1.87 |
| \( V_{DD} \)       | V     | 0.34 | 0.37 |
| \( R_t \)          | \( \Omega \) | 134  | 134  |
| \( \Delta \)       | meV   | 145  | 154  |
| \( h\varepsilon \) | meV   | 11   | 11   |
| \( K_{sr} \)       |       | 0.35 | 0.5  |

The basic procedure for the derivation of the total \( S_{ID} \) is based on dividing the device channel into microscopic slices \( \Delta x \), calculating all the local noise contributions at each \( \Delta x \) and then integrating them along the gated channel region assuming a small-signal analysis since these local fluctuations are considered uncorrelated [19]–[21], [33], [41, SI, Sec. C1, Fig. S1b]. The different noise sources of the GFET are presented in the small-signal circuit in Fig. 3 where apart from \( S_{ID} \), channel-induced gate current noise spectral density \( S_{ig} \) as well as the noise contributions from resistances \( R_C \) and \( R_G \) are included. Since the main contribution to minimum noise figure (NF\(_{min}\)), the measure of two-port noise property, is stemming from \( S_{ID} \) as \( S_{ig} \) is negligible at \( f = 1 \) GHz [16, Figs. 10–12], in this work, we will enhance the analysis of the spectral density of \( I_D \) fluctuations.

To calculate \( S_{ID} \), a drift-diffusion current approach is used

\[
I_D = -W|Q_{gr}|\mu_{eff}E, \quad \mu_{eff} = \frac{\mu}{1 + \frac{1}{E_C}}, \quad E_C = \frac{\mu_{sat}}{\mu}
\]

where \( |Q_{gr}| \) is the total graphene charge [41, (A22) in SI, Sec. B]. The absolute value of \( Q_{gr} \) indicates the movement of negative charged electrons and positive charged holes in opposite directions, additively contributing to \( I_D \). \( E \), \( E_x \), and \( E_C \) are the electric, the longitudinal electric, and the critical electric fields, respectively, and \( \mu_{eff} \) is the effective mobility representing the degradation of the channel mobility at high electric field regime due to the VS effect. The latter effect is considered in the proposed noise model since it is expected to increase \( S_{ID} \) in short channels at high \( V_{DS} \) values [15]–[21]. A two-branch VS \( \mu_{sat} \) model is used, which is considered constant near CNP below a critical chemical potential value \( V_{c\text{crit}} \) and inversely proportional to chemical potential \( V_c \) above \( V_{c\text{crit}} \) [33], [41, (A24) in SI, Sec. B]. Total \( S_{ID} \) along the gated channel is given by [19, (6.3) and (6.4)]

\[
S_{ID} = \int_0^L S_{id}(\omega, x) dx = \int_0^L G_{CH} \Delta R^2 \frac{S_{id}(\omega, x)}{\Delta x} dx
\]

where \( G_{CH} \) is the channel conductance, \( \Delta R \) is the resistance of the slice \( \Delta x \) of the channel, \( S_{id}(\omega, x) \) is the PSD of the local noise source, and \( S_{id}(\omega, x) \) is the channel noise PSD due to a single noise source [41, SI, Sec. C1]. \( \mu_{eff} \) can be considered a function of both channel potential \( V \) and \( I_D \) through \( E_x(V, I_D) \) where the latter depends on the position \( x \) along the channel [19, Sec. 9.4.1], [20]. Thus, \( I_D \) is defined as

\[
I_D = f(V, I_D) = \frac{W}{x} \int_0^V |Q_{gr}|\mu_{eff}(V, I_D) dV \Rightarrow dI_D
\]

\[
\frac{\partial f}{\partial V} dV + \frac{\partial f}{\partial I_D} dI_D \Leftrightarrow G_S = \frac{di}{dV} = \frac{\partial f}{\partial V} + \frac{\partial f}{\partial I_D} \Rightarrow G_S
\]

\[
= \frac{W|Q_{gr}|\mu_{eff}}{x} \Rightarrow \frac{\partial f}{\partial V} dV + \frac{\partial f}{\partial I_D} dI_D \Rightarrow G_S
\]

\[
= \frac{\partial f}{\partial V} = \frac{W|Q_{gr}|\mu_{eff}}{x} \Rightarrow \frac{\partial f}{\partial I_D} dI_D \Rightarrow dV
\]

since it can be easily shown from \( I_D \) definition in (4) that

\[
\frac{\partial f}{\partial I_D} = \frac{W}{x} \int_0^V |Q_{gr}|\mu_{eff} E \frac{\partial E}{\partial I_D} dv = \frac{W}{x} \int_0^V |Q_{gr}|\mu_{eff} \frac{\partial E_x}{\partial I_D} dv
\]

where \( G_S \) is the transconductance on the source side [41, SI, Sec. C1, Fig. S1b]. The next step would be to calculate \( \frac{\partial \mu_{eff}}{\partial I_D} \) in the denominator of (4) [19], [20]

\[
\frac{\partial \mu_{eff}}{\partial I_D} = \frac{\partial \mu_{eff}}{\partial E_x} \frac{\partial E_x}{\partial I_D} = \frac{\partial \mu_{eff}}{\partial E_x} \frac{\partial E_x}{\partial I_D}
\]

\[
= \frac{\partial E_x}{\partial I_D} \frac{\partial \mu_{eff}}{\partial E_x} = \frac{\partial E_x}{\partial I_D} \frac{\partial \mu_{eff}}{\partial E_x}
\]

(7)

(8)

(9)

(10)

(11)

(12)

(13)

(14)

(15)
\[ \mu_{\text{diff}} = \mu_{\text{eff}} + \mu_{\text{eff}}E_x [19, (9.130)] \] is the differential mobility. By using (6) and (7) in (4), \( G_S \) yields

\[ G_S = \frac{W|Q_{gr}|\mu_{\text{eff}}}{x + \int_0^\mu (\mu_{\text{eff}}E_x/\partial E)/\mu_{\text{diff}} dV}. \]  

(8)

Similarly, the transconductance on the drain side \( G_D \) [19], [41, SI, Sec. C1, Fig. S1b] can be calculated by following an identical procedure as in the \( G_S \) case [19], [20]:

\[ G_D = \frac{W|Q_{gr}|\mu_{\text{eff}}}{L - x + \int_0^\mu (\mu_{\text{eff}}E_x/\partial E)/\mu_{\text{diff}} dV}. \]  

(9)

and thus, \( G_{\text{CH}} \) is given according to (8) and (9)

\[ \frac{1}{G_{\text{CH}}} = \frac{1}{G_S} + \frac{1}{G_D} \Rightarrow G_{\text{CH}} = \frac{W|Q_{gr}|\mu_{\text{eff}}}{L + \int_0^\mu (\mu_{\text{eff}}E_x/\partial E)/\mu_{\text{diff}} dV}. \]  

(10)

(for more details, see [41, (A27) in SI, Sec. C1, (A30) in SI, Sec. C2]). For \( \Delta R \) calculation, (9) is applied from \( x \) to \( x + \Delta x \) [20]. With the help of \( \mu_{\text{diff}} \) definition and \( E, \partial E_x/\partial E = E_x \) as mentioned before

\[ \Delta R = \frac{1}{\Delta G} \frac{\Delta x}{W|Q_{gr}|\mu_{\text{diff}}} \]  

(11)

(for more details, see [41, (A31) in SI, Sec. C2]).

In presence of an electric field, equilibrium does not stand anymore locally in the channel, and thus, the Einstein relation between mobility and diffusion coefficient cannot be applied directly [19], [29], [30]. This can be dealt with the assumption of an Einstein-like expression to stand in nonequilibrium and the definition of a noise temperature \( T_n \approx T_c \), where \( T_c \) is the carrier temperature [19, (9.141) and (9.142)]. For degenerate semiconductors such as graphene, the contributions of total charge carriers to \( I_0 \) and \( S_{\text{diff}} \) are no longer independent [28], [29], and thus, \( S_{\text{diff}} \) must be multiplied with \( \Delta N^2/N = (K_B T_n/n_{gr}) (\partial n_{gr}/\partial E)F \), where \( \Delta N^2 \) is the variance and \( N \) is the average number of carriers [29, eq. (3)], [30]. \( S_{\text{diff}} \) can be calculated if (11) is considered as [19, (6.13)]

\[ S_{\text{diff}}(\alpha, \omega) = \frac{4K_B T_n}{\Delta R} \frac{4K_B T_C \Delta N^2}{N} \]  

(12)

\[ = 4K_B T_C \frac{W_{\mu_{\text{diff}}}}{\Delta x} U_T |V_c| \]  

(for more details, see [41, (A32) in SI, Sec. C2]) where \( T_L \) is the lattice (room) temperature, \( n_{gr} = |Q_{gr}|/e [31] \) is the graphene charge density with \( e \) the elementary charge, \( EF = e|V_c| \) is the shift of the Fermi level [32], [41, SI, Fig. S1a], \( U_T = K_B T_L/e \) is the thermal voltage at room temperature, and \( k \) is a coefficient [31], [41, SI, Sec. B]. Thus, (3) is transformed because of (10)-(12) as

\[ S_{\text{ID}} = 4K_B T_C U_T k \mu_{\text{eff}} W L_{\text{eff}} \int_0^L |V_c| dV_c \]  

(13)

where \( \mu_{\text{eff}}/\mu_{\text{diff}} = \mu [41, (A36) in SI, Sec. C2]. \( M \) is given by [19]

\[ M = \frac{1}{1 + \frac{1}{T_L} (Q_{\text{vac}}/C_{\text{vac}})/L_{\text{eff}}} \]  

\[ = \frac{1}{1 + \frac{\mu_{\text{eff}}}{C_{\text{vac}}}} \left( \frac{L}{L_{\text{eff}}} \right)^2 \]  

(14)

(see [41, (A37) and (A38) in SI, Sec. C2]) where \( C_{\text{vac}} = k|V_c| \) is the quantum capacitance [31]–[33], [41, SI, Sec. B, Fig. S1a], \( C \) is the sum of top and back oxide capacitances, \( L_{\text{eff}} \) accounts for an effective channel length representing the reduction of \( I_D \) due to the VS effect [31]–[33], and thus, two cases shall be considered for its solution according to the two-branch \( u_{\text{sat}} \) model applied in this work [41, (A24) and (A25) in SI, Sec. B]. \( V_c \) and \( V_{\text{sat}} \) are the chemical potentials at source and drain sides, respectively [41, (A23) in SI, Sec. B]. From [19, (9.150)] and [41, (A17) in SI, Sec. B]

\[ \mu_{\text{eff}} = \mu \left( \frac{T_L}{T_C} \right) \frac{T_C}{T_L} = \left( \frac{\mu_{\text{eff}}}{\mu} \right)^2 \left( 1 + \frac{|V_c|}{E_C} \right)^2 \]  

(15)

and (13) becomes due to (14) and (15)

\[ S_{\text{ID}} = 4K_B T_L U_T k \mu_{\text{eff}} W L_{\text{eff}} \int_0^L |V_c| dV_c = 4K_B T_L U_T k \mu_{\text{eff}} W L_{\text{eff}} \times \left[ \int_{V_{\text{vac}}}^{V_{\text{sat}}} \left( \frac{|V_c|}{C_{\text{vac}}} \right)^2 \frac{dV_c}{C_{\text{vac}}} \right] \left( \frac{|V_c|}{C_{\text{vac}}} \right) dV_c \]  

(17)

which again is split into two integrals, \( S_{\text{ID}A1} \) (1st in the brackets) and \( S_{\text{ID}A2} \) (2nd in the brackets) as \( S_{\text{ID}} = S_{\text{ID}A1} - S_{\text{ID}A2} \), where

\[ S_{\text{ID}A1} = 4K_B T_L U_T k \mu_{\text{eff}} W L_{\text{eff}} \int_{V_{\text{vac}}}^{V_{\text{sat}}} \left( \frac{|V_c|}{C_{\text{vac}}} + C \right) dV_c \]  

\[ = 4K_B T_L U_T k \mu_{\text{eff}} W L_{\text{eff}} \left[ \frac{\alpha C V_c^2}{2k} + \frac{\alpha V_c^3}{3} + \frac{CV_c^2}{4} + \frac{k V_c^5}{5} \right] \]  

(18)

where \( g_{\text{vac}} \) is a normalized \( I_D \) term [41, (A21) in SI, Sec. B] and \( \alpha \) is related to residual charge [31]–[33]. The VS effect contributes to \( S_{\text{ID}A1} \) only through \( L_{\text{eff}} \), while for \( S_{\text{ID}A2} \), both \( L_{\text{eff}} \) and \( u_{\text{sat}} \) are included. As in \( L_{\text{eff}} \) solution (see [41, (A25)]]
in SI, Sec. B)], two cases shall be considered for the solution of $S_{\text{IDA2}}$ according to the two-branch $u_\text{sat}$ model [41, (A24) in SI, Sec. B]. Thus, near CNP

$$S_{\text{IDA2}} = 4K_BT UT_k\mu^2 W \int_{V_{cd}}^{V_{ds}} \left( \frac{kV_c^2}{S} \right) dV_c$$

$$= 4K_BT UT_k\mu^2 W \int_{V_{cd}}^{V_{ds}} \left[ \frac{kV_c^3}{S} \right]_{V_{cd}} \to |V_c| < V_{\text{crit}}$$

whereas away CNP

$$S_{\text{IDA2}} = 4K_BT UT_k\mu^2 W \int_{V_{cd}}^{V_{ds}} \left( \frac{kV_c^2}{S} \right) dV_c$$

$$= 4K_BT UT_k\mu^2 W \int_{V_{cd}}^{V_{ds}} \left[ \frac{kV_c^3}{S} \right]_{V_{cd}} \to |V_c| > V_{\text{crit}}$$

(for $S$ and $N$ definition, see [41, (A24) in SI, Sec. B]). The absolute value in the analytical solution of (19) comes from $|dV_c|$ in order to distinguish two cases for $S_{\text{IDA2}}$ depending on the sign of $dV_c$. Thus, in the case of $dV_c < 0 \to V_c > V_{cd}$ ($V_{ds} > 0 \to dV_c = -dV_c$, the integral is solved from $V_{cd}$ to $V_c$, while when $dV_c > 0 \to V_c < V_{cd}$ ($V_{ds} < 0 \to dV_c = dV_c$, the integral is solved from $V_c$ to $V_{cd}$). For the solution of $S_{\text{IDC}}$ [41, (A40) in SI, Sec. C3], the main idea was to express the electric field as: $E = (−dV_{ldx})/(−dV_{ldx})$ [41, (A17) in SI, Sec. B], and then, both sides are integrated after being multiplied with $dV$, which has as a result a double integral notation. $S_{\text{IDC}}$ is directly affected by the square of $u_\text{sat}$, and thus, again two different cases shall be considered. Near CNP

$$S_{\text{IDC}} = 4K_BT UT_k\mu^3 W \int_{V_{cd}}^{V_{ds}} \left( \frac{kV_c^2}{S} \right)^3 \left[ N^2 \right]_{V_{cd}}$$

$$= 4K_BT UT_k\mu^3 W \int_{V_{cd}}^{V_{ds}} \left[ \frac{kV_c^2}{S} \right]_{V_{cd}} \to |V_c| < V_{\text{crit}}$$

and away CNP

$$S_{\text{IDC}} = 4K_BT UT_k\mu^3 W \int_{V_{cd}}^{V_{ds}} \left( \frac{kV_c^2}{S} \right)^3 \left[ N^2 \right]_{V_{cd}}$$

$$= 4K_BT UT_k\mu^3 W \int_{V_{cd}}^{V_{ds}} \left[ \frac{kV_c^2}{S} \right]_{V_{cd}} \to |V_c| > V_{\text{crit}}.$$
The measurement frequency $f = 1$ GHz primarily ensures the QS region of operation, which results in a frequency-independent behavior of $S_{\text{ID}}$. At non-QS regime, one should deal with induced gate noise as well as carrier inertia effects, which would produce different current noise PSDs at source and drain; the latter is not the purpose of the present study. Thus, in the following plots, the attention is focused on the bias dependence of $S_{\text{ID}}$. In Fig. 5, both measured and simulated $S_{\text{ID}}$ are depicted versus $V_{\text{GS}}$ at $V_{\text{DS}} = 0.5$ V from strong p-type to strong n-type regime for both DUTs where asymmetries of IV and $Y$-parameters [cf. Figs. 1(c) and 2] experimental data result in higher measured $S_{\text{ID}}$ at p-type region according to (1) as $|Y_{21\text{INT}}|$ is greater than in n-type region for both DUTs [cf. Figs. 1(c) and 5]. In addition, the reduced gain due to low $|g_{mn}|$ near CNP does not ensure accurate $R_{\text{n}}$ measurements there since a sufficient gain is required for the $Y$-factor HFN measurement method, and thus, $V_{\text{GS}}$ points very close to CNP ($V_{\text{GS}} = 0.6$ and 0.7 V for EG5 and $V_{\text{GS}} = 0.7$ and 0.8 V for EG8) are omitted. Experimental data are extracted from (1) at any bias point since noise and $Y$-parameters are measured simultaneously from the same setup, while simulated data are obtained by solving (16) with (18)–(20). The model provides an accurate description of the experiments for both GFETs in the p-type regime where we focus our analysis since an accurate description of the experiments for both GFETs | $S_{\text{ID}}$ region of operation, which results in a frequency- $f = 1$ GHz. Markers: measured. Solid lines: model. Dashed lines: nondegenerate model.

An important figure of merit (FoM) for RF circuit design for noise performance is an excess noise factor $\gamma$, introduced by van der Ziel [12] and widely investigated in CMOS devices [13], [19]–[21], [39]

$$\gamma = \frac{g_n}{g_{\text{mi}}}$$

where $g_{\text{mi}} = \delta[Y_{21\text{INT}}]$ is the intrinsic transconductance of the device (removed $R_c$ and $R_G$ resistances) and $g_n$ is the noise conductance [19]–[21]. The latter is defined by $S_{\text{ID}}$ in (16) with (18)–(20), divided by $4K_BT_L$. Initially, excess noise factor was referred to as $\alpha$, whereas $\gamma$ was the thermal noise parameter defined as $g_n/g_{\text{do}}$ where $g_{\text{do}}$ is the output conductance at $V_{\text{DS}} = 0$ V [12]–[18]. Thermal noise parameter is not an ideal FoM for analog/RF design since $g_n$ and $g_{\text{do}}$ are evaluated at different operating conditions [19], [21]. Excess noise factor is of utmost importance for noise performance in RF circuits since it accounts for the generated noise at the drain side of the device for a given transconductance [19], [21], [39]. $g_n$ and $g_{\text{mi}}$ can be evaluated for the same bias point and $\gamma$ is important to determine the noise figure (NF) of an LNA [21]. In this work, excess noise factor $\gamma$ is for the first time characterized for GFETs. Consequently, measured and modeled $\gamma$ are shown in Fig. 6(a) versus $V_{\text{GS}}$ at $V_{\text{DS}} = 0.5$ V for the DUTs. Experimental data are extracted by using (1) for $S_{\text{ID}}$ in (21), while model by using (16) with (18)–(20) in (21). Measured $\gamma$ can be up to $\sim$3–4 showing an increasing trend with higher carrier densities. The model precisely captures this behavior. Simulated $\gamma$ for long-channel case is presented with dashed lines by deactivating VS effect ($h\Omega$ parameter) in our model, cf. Fig. 6(a). This leads to an underestimation of $\gamma$ by up to 30%, compared to measured data.

Noise resistance behavior versus bias is shown in Fig. 6(b). Considering (1) and (21), $R_{\text{INT}}$ can be calculated as

$$R_{\text{INT}} = \frac{g_n}{|Y_{21\text{INT}}|^2}$$

and then compared to the measured $R_{\text{INT}}$, cf. Fig. 6(c) and (d), where the consistency of the model versus measured data is apparent, whereas $R_{\text{INT}}$ increases toward the stronger p-type region. For more explicit analysis, $S_{\text{ID}}$, $\gamma$, and $R_{\text{INT}}$ for both investigated DUTs are shown versus $I_D$ and $g_{\text{mi}}$ (insets) in Fig. 7(a)–(c), respectively, at $V_{\text{DS}} = 0.5$ V. The proposed model accounts well the measured data: $S_{\text{ID}}$, $\gamma$, and $R_{\text{INT}}$ dependences on $I_D$, cf. Fig. 7. The presented parameters increase with $I_D$ and such trend agrees with results from MOSFETs [15]–[21]. In terms of $S_{\text{ID}}$, there is a saturation-like trend at higher $I_D$ (or at the strong p-type region as shown in Fig. 5) which also agrees with findings from CMOS [15]–[18], [21]. Moreover, the shortest device (EG5) exhibits higher noise as
it was expected. This is more evident in the insets of Fig. 7 versus $g_m$ since both GFETs appear to have similar $g_m$ while the maximum $g_m$ value corresponds to minimum noise.

V. CONCLUSION

A complete physics-based analytical intrinsic channel thermal noise model in the QS region of operation for GFETs is derived and verified on the measured data. The presented $S_D$ model describes precisely the bias dependence of noise, including VS effect, while it also considers the degenerate nature of graphene for the first time. The proposed model can be easily implemented in Verilog-A for use with circuit simulators.

The model is successfully validated with experimental high-frequency $Y$-parameters and noise data without the need of any fitting parameter, which proves its physical consistency. Noise PSD increases with $I_D$ and saturates at deep $p$-type region similar to CMOS devices. Apart from $S_D$, noise excess factor $\gamma$ is defined for the first time for GFETs. Its value for the short-channel GFETs under test reaches a maximum from $\sim 3$ to 4 at higher $I_D$ (EG5: $\sim 1.8$ mA and EG8: $\sim 1.4$ mA) away from CNP, whereas it is lower for smaller currents near CNP (EG5: $\sim 1.4$ mA and EG8: $\sim 1.1$ mA). This trend is successfully predicted by the model whereas the simulations without VS effect underestimate $\gamma$ around 30%. Furthermore, $S_D$, $\gamma$, and $R_{\text{INT}}$ present a minimum at highest $g_m$, which is very useful information for the circuit design point of view. These quantities are higher for the shortest device and the proposed model fits accurately this characteristic, which is indicative of a proper scaling behavior. GFET HFN studied in this work shows comparable results with CMOS [21], indicating that this emerging technology is on a good track of development and could eventually compete with incumbent devices without facing the scaling limitations of the latter.

REFERENCES

[1] M. Asad, K. O. Jeppson, A. Vorobiev, M. Bonmann, and J. Stake, “Enhanced high-frequency performance of top-gated graphene FETs due to substrate-induced improvements in charge carrier saturation velocity,” IEEE Trans. Electron Devices, vol. 68, no. 2, pp. 899–902, Feb. 2021, doi: 10.1109/TED.2020.3046172.
[2] C. Yu et al., “Improvement of the frequency characteristics of graphene field-effect transistors on SiC substrate,” IEEE Electron Device Lett., vol. 38, no. 9, pp. 1339–1342, Sep. 2017, doi: 10.1109/LED.2017.2734938.
[3] A. C. Ferrari et al., “Science and technology roadmap for graphene, related two-dimensional crystals, and hybrid systems,” Nanoscale, vol. 7, no. 11, pp. 4598–4810, 2015, doi: 10.1039/C4NR01606A.
[4] M. A. Andersson, O. Habibpour, J. Vukusic, and J. Stake, “Resistive graphene FET subharmonic mixers: Noise and linearity assessment,” IEEE Trans. Microw. Theory Techn., vol. 60, no. 12, pp. 4035–4042, Dec. 2012, doi: 10.1109/TMTT.2012.2221141.
[5] H. Lyu et al., “Double-balanced graphene integrated mixer with outstanding linearity,” Nano Lett., vol. 15, pp. 6677–6682, Sep. 2015, doi: 10.1021/acs.nanolett.5b02503.
[6] O. Habibpour et al., “A W-band MMIC resistive mixer based on epitaxial graphene FET,” IEEE Microw. Wireless Compon. Lett., vol. 27, no. 2, pp. 168–170, Feb. 2017, doi: 10.1109/LMWC.2016.2646998.
[7] M. A. Andersson, O. Habibpour, J. Vukusic, and J. Stake, “10 dB small-signal graphene FET amplifier,” Electron. Lett., vol. 48, no. 14, pp. 861–863, Jul. 2012, doi: 10.1049/el.2012.1347.
[8] T. Hanna, N. Deltimple, M. S. Khennis, E. Pallecchi, H. Happy, and S. Fregonese, “2.5 GHz integrated graphene RF power amplifier on SiC substrate,” Solid-State Electron., vol. 127, pp. 26–31, Jan. 2017, doi: 10.1016/j.sse.2016.10.002.
[9] F. Pasadas and D. Jimenez, “Non-quali-static effects in graphene field-effect transistors under high-frequency operation,” IEEE Trans. Electron Devices, vol. 67, no. 5, pp. 2188–2196, May 2020, doi: 10.1109/TED.2020.2982840.
[10] A. van der Ziel, “Thermal noise in field-effect transistors,” Proc. IRE, vol. 50, no. 8, pp. 1808–1812, Aug. 1962, doi: 10.1109/JRPROC.1962.288221.
[11] A. G. Jordan and N. A. Jordan, “Theory of noise in metal oxide semiconductor devices,” IEEE Trans. Electron Devices, vol. 12, no. 3, pp. 148–156, Mar. 1965, doi: 10.1109/T-ED.1965.15471.
[12] A. van der Ziel, Noise in Solid State Devices and Circuits. New York, NY, USA: Wiley, 1986.
[13] Y. Tsividis, Operation and Modeling of the MOS Transistor, 2nd ed. New York, NY, USA: Oxford Univ. Press, 1999.
[14] A. A. Abidi, “High-frequency noise measurements on FETs with small dimensions,” IEEE Trans. Electron Devices, vol. 33, no. 11, pp. 1801–1805, Nov. 1986, doi: 10.1099/T-ED.1986.22743.
[15] C.-H. Chen and M. J. Deen, “Channel noise modeling of deep sub-micron MOSFETs,” IEEE Trans. Electron Devices, vol. 49, no. 8, pp. 1484–1487, Aug. 2002, doi: 10.1109/T-ED.2002.801229.
[16] C.-H. Chen, M. J. Deen, Y. Cheng, and M. Matloubian, “Extraction of the induced gate noise, channel noise, and their correlation in submicron MOSFETs from RF noise measurements,” IEEE Trans. Electron Devices, vol. 48, no. 12, pp. 2884–2892, Dec. 2001, doi: 10.1109/T-ED.2016.2417422.
[17] A. J. Scholten, L. F. Tiemeijer, R. V. Langevelde, R. J. Havens, A. T. A. Z.-V. Duijnhoven, and V. C. Venezia, “Noise modeling for RF CMOS circuit simulation,” IEEE Trans. Electron Devices, vol. 50, no. 3, pp. 618–623, Mar. 2003, doi: 10.1109/TED.2003.810480.
[18] S. Asgarani, M. J. Deen, and C.-H. Chen, “Analytical modeling of MOSFETs channel noise and noise parameters,” IEEE Trans. Electron Devices, vol. 51, no. 12, pp. 2109–2114, Dec. 2004, doi: 10.1109/TED.2004.838450.
[19] C. Enz and E. Vittoz, Charge Based MOS Transistor Modeling. Chichester, U.K.: Wiley, 2006.
[20] A. S. Roy and C. Enz, “An analytical thermal noise model of the MOS transistor valid in all modes of operation,” in Proc. Int. Conf. Noise Fluctuations (ICNF),Salamanca, Spain, Sep. 2005, pp. 741–744, doi: 10.1063/1.2036856.
