Multiple Error Recovery in FIR Filter using Reduced-Precision Redundancy (RPR)

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Abstract: In this paper, Reduced-Precision redundancy (RPR) technique is used to protect FIR Filter against single event upsets (SEUs). One of the radiation effect is Single Event Upset (SEU) which causes a logical bit changing in a device and results in an unrecoverable error in a system. RPR is a redundancy technique similar to TMR that requires less hardware overhead by using reduced-precision modules in two of its three replicas [1]. FIR Filters are common in the analog and digital communications. This paper introduces the RPR Technique to protect the FIR Filter and this is implemented in order to provide lower power consumption & reduced complexity. The performance of the proposed system is compared with SCTMR & SMERTMR in terms of hardware requirements. The proposed method is designed using VHDL on Xilinx ISE simulator

Keywords: SEUs, RPR, FIR, Multiple error recovery, TMR Systems

1. Introduction

In space systems, radiation sources are abundant. The effects of radiation are hard to predict and the combination of effects can destroy a system. The Single Event Upset (SEU) is a radiation effect, which causes a bit changing in a device. A logical bit changing may cause a chain reaction and consequently result in an unrecoverable error of a system.

The Digital Filters are commonly used in analog and digital communication to remove the unwanted noise in the signal thereby providing better quality at the output. As communications are fundamental to space borne applications, digital filters play an important role in space systems such as satellites, unmanned missions, etc [5]. The digital filters produces stabilized signal when compared to the analog filters. So digital filters are more used than the analog one. Transposed-form FIR Filter is generally selected than direct filter because of its lower complexity, higher performance and power efficiency (fig. 1)

Therefore, different methods are presented to protect the FIR Filters from single event upset and to satisfy timing constraints such as triple modular redundancy, SCTMR and SMERTMR and using RPR Technique.

Figure 1: Transposed FIR Filter

Figure 2: Triple Modular Redundancy

Triple Modular Redundancy (TMR)(see fig.2) is proposed by Von Neumann where a module is replicated three times and the output is taken from the majority voter. Whenever an error is detected, the voter in the TMR system will take majority of three outputs. However, TMR system fails when there are multiple faults and a faulty module. Also one of the important drawbacks is area overhead because a same system is designed thrice. To overcome the disadvantages of TMR system, the same system is provided with an additional controller where it can detect and recover the faulty module and it is named as SCTMR. But it fails to detect the multiple faulty modules and latent faults. So SMERTMR is designed such that the same system is modified to detect and recover multiple faulty modules and latent faults [8, 10].

To minimize the area overhead and to increase the performance, another technique that is RPR (Reduced Precision Redundancy) is used in the same system to detect the multiple faults. This technique uses two reduced precision modules, one fully précised module out of three modules and decision blocks and the outputs are also replicated three times to avoid single points of failure in those modules. It takes advantage of the fact that RP arithmetic can be a good estimate of computations that use higher precision. It has an advantage of low area overhead and limits the error at the output of a module [1].
2. Literature Survey

2.1 SCTMR Technique

To overcome the drawbacks of TMR system, the same system is provided with an additional controller where it can detect and recover the faulty module. Block diagram of ScTMR (fig. 3) consists of three redundant modules, voter with an additional controller. When the voter detects an error, the controller will identify the type of error and recover the state of faulty module by copying the output of the fault free module to the faulty module. The recovery process is done through the scan-chain inputs, scan-chain outputs, and scan-chain enable signals instructed by the ScTMR controller [10].

![Figure 3: Block diagram of ScTMR](image)

The state diagram of the ScTMR system is shown in (fig. 4). This technique consists of four modes of operation. Initially the system will be in normal state. When the voter detects an error, it will go to recovery state. In recovery state, controller will detect the faulty module and the error type. If the error is transient, then the output of the fault free is copied to the faulty module. MRFM (most recent faulty module) holds the faulty module number. This number is compared with the new faulty module. If the number is equal, then the NCF (number of consecutive faults) will increment by one otherwise it resets to zero. Whenever the value exceeds the threshold value, the module is considered as permanent. If the fault is permanent, then the system will go to master/checker state. Here that module will be discarded and the other two modules will determine the output. If there are multiple faults, then the system will go to unrecoverable condition.

![Figure 4: ScTMR state diagram](image)

However, there are disadvantages such as it cannot detect the latent faults and cannot recover from the multiple faults. Latent faults means a fault is not propagated to the system output but causes a mismatch at the TMR modules.

2.2 Proposed Voter

The voter will identify the faulty module. This voter can be used for both the ScTMR and SMERTMR systems. The proposed voter is shown in (fig. 5). There are three comparators namely (C12, C13, and C23) and each comparator will check any mismatch occurred. When a mismatch happens, an error signal is activated. For an example, if there is a mismatch between outputs II and III is detected, TE13 and TE12 are activated. In order to detect permanent faults, the proposed voter provides three input signals (named Pr12, Pr13, and Pr23), which are derived by the ScTMR controller. During the normal state and during recovery state, these three signals are deactivated (Pr12 = Pr13 = Pr23 = 0). Output selector circuit uses E12 and E13 signals as the inputs of logical AND gate as the select line of the 2x1 multiplexer. If the module II, or module III is faulty, then the output of module I is selected as the error-free output. If module I is faulty, then Output II will be selected as the error-free output [10].

![Figure 5: ScTMR Voter](image)

2.2 SMERTMR Technique

Scan chain based multiple error recovery for a TMR system was introduced to overcome the drawbacks of ScTMR system. The SMERTMR technique has the ability to detect and remove latent faults in modules and to remove the multiple faults. There is one more mode of operation i.e. comparison mode in SMERTMR apart from the SCTMR. In the comparison mode of operation, bit by bit comparison is done to find the latent faults [10].

![Figure 6: SMERTMR State diagram](image)
State diagram (fig. 6) shows the modes of operation. Initially the system will be in normal mode. Once an error is detected by the voter or when the checkpoint is activated, the system goes to comparison mode of operation. Comparison mode is activated by applying checkpoint signal to remove the latent faults. In comparison mode, bit-by-bit comparison is done to determine the faulty module and the type of error. If no error is found, then system goes to normal mode or else the system goes to recovery mode. Any failure during the operation will end with unrecoverable condition. During recovery process, the state of the fault free module is copied to the faulty module. If it detects a permanent fault, the system enters the Master or checker mode. In the M/C mode, any fault in the master or the checker modules results in an unrecoverable condition [10].

The voter and the block diagram of SMERTMR are similar to SCTMR.

3. RPR Technique to Recover Multiple Errors

RPR is a technique similar to TMR technique where two reduced precision modules are used out of three modules. When the fully précised module fails to give the correct output then the reduced precision output is taken. This is shown in the fig. 9. If the difference between fully précised output value and reduced précised value is greater than the threshold value, the reduced precision output is taken. If the difference is less than the threshold, then fully précised value is taken. The decision blocks and outputs can be triplicate as well to avoid single points of failure in those modules [1].

Fig 7 shows a block diagram of an n-bit FIR filter protected with RPR. The figure shows that the inputs to the filter are triplicated, as with TMR, and that the second and third replicas of the circuit are implemented with RP (k-bit, where k < n) FIR filters [1].

The main advantage of RPR Technique is that the area overhead is less than the other previous techniques. The modes of operation and the voter of the RPR is same as the SMERTMR System.

4. Simulation Results

The proposed RPR Technique is designed using VHDL on Xilinx ISE simulator and compared with SCTMR & SMERTMR. Power consumption is calculated using X-power analyser.

Here the modules are taken as FIR filter, simulation results shows the case when two modules are faulty. If module 2 is faulty then the module 2 output is recovered. The fault free output is copied to the faulty module. However, if module 2 is permanent fault, then module 2 is discarded. If module 3 is also faulty, then the system will be halted.

Fig 8 shows the simulation result of ScTMR.

Fig 9 shows the power analysis results of scan chain TMR. Power is calculated in mill watt (mW) and power consumed by scan chain TMR is 502mW.
Fig 10 shows the simulation result of scan chain multiple error recovery in TMR technique used in FIR filter. During comparison mode, multiple faults can be detected and latent faults can be found out.

![Figure 10: Simulation result of SMERTMR](image)

Table 1: Comparison Results

| System used | Power consumption | Area (Gate count) |
|-------------|-------------------|-------------------|
| SCTMR       | 502mW             | 19,483            |
| SMERTMR     | 483mW             | 20,356            |
| RPR         | 420mW             | 14,030            |

The result shows that the proposed technique has greatly reduced in terms of area and power as compared to SCTMR & SMERTMR. The main advantage of this technique is that it can detect multiple faults with great minimization in terms of area and delay.

Fig.13 shows the power analysis results of multiple error recovery in TMR using RPR Technique. Power is calculated in milli watt (mW) and power consumed by multiple error recovery in TMR using RPR Technique is 420mW.

5. Inferences

Power is calculated in milli Watt (mW) and the comparison result is shown in fig.14. The power consumed and the area used in each of the system are compared and shown in the table.1. given below.

![Figure 14: Power Consumption Comparison](image)

6. Conclusion

The proposed RPR technique is used to protect the Transposed FIR Filter. The Fully précised and other two reduced précised output is compared and the output is taken. The performance is compared the existing systems and found that the new proposed system greatly reduces the power and the area. The power is reduced from 483mW to
420mW. The main drawback i.e area and power of all other systems is reduced greatly.

References

[1] Brian Prattl, Megan Fuller –Reduced-Precision Redundancy For Reliable Fpga Communications Systems In High-Radiation Environments” IEEE Transactions On Aerospace And Electronic Systems Vol. 49, No. 1 January 2013.

[2] P. K. Samudrala, J. Ramos, and S. Katkoori, –Selective triple modular redundancy (STMR) based single event upset (SEU) tolerant synthesis for FPGAs,” IEEE Trans. Nucl. Sci., vol. 51, no. 5, pp. 2957–2969, Oct. 2004.

[3] Levent Aksoy, “Design Of Digit-Serial Fir Filters: Algorithms,Architectures, And A Cad Tool”, IEEE Transactions On Very Large Scale Integration (Vlsi) Systems, Vol. 21, No. 3, March 2013

[4] A. L. J. Hopkins, T. B. Smith, and J. H. Lala, –FTMP— A highly reliable fault-tolerant multiprocess for aircraft,” Proc. IEEE, vol. 66, no. 10, pp.1221–1239, Oct. 1978.

[5] S.M. Parkes, "DSP (Demanding Space-based Processing!): the Path Behind and the Road Ahead”, 6th International Workshop on Digital Signal Processing Techniques for Space Applications, Noordwijk, The Netherlands, September 1998

[6] M. Zhang, S. Mitra, T. M. Mak, N. Seifert, N. J. Wang, Q. Shi, K. S. Kim, N. R. Shanbhag, and S. J. Patel, –Sequential element design with built-in soft error resilience,” IEEE Trans. Very Large Scale Integr.(VLSI) Syst., vol. 14, no. 12, pp. 1368–1378, Dec. 2006.

[7] X. She and K. S. McElvain, –Time multiplexed triple modular redundancy for single event upset mitigation,” IEEE Trans. Nucl. Sci., vol. 56, no. 4, pp. 2443–2448, Aug. 2009.

[8] M. Ebrahimi, S. G. Miremadi, and H. Asadi, –ScTMR: A scan chain based error recovery technique for TMR systems in safety-critical applications,” in Proc. Design Autom. Test Eur. Conf. Exhibit., 2011, pp. 1–4.

[9] X. Wang, –Partitioning triple modular redundancy for single event upset mitigation in FPGA,” in Proc. Int. Conf. E-Product E-Service EEntertain., 2010, pp. 1–4

[10] Seyed Ghassem Miremadi, Mojtaba Ebrahimi, –Low-Cost Scan-Chain-Based Technique to Recover Multiple Errors in TMR Systems”, IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 21, No. 8, August 2013, pp1454-1468.

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