HiKonv: Maximizing the Throughput of Quantized Convolution With Novel Bit-wise Management and Computation

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Abstract—Quantization is proven to be effective for Convolutional Neural Networks (CNN) to reduce the cost of computation and storage with low-bitwidth data representations. However, the current execution of quantized data on the existing full-bitwidth processing units, such as ALU in CPUs and DSP in FPGAs, is through simply extending the lower bitwidth to the supported bitwidth, which leads to the underutilization of the computing unit and delivers low computational throughput. In this study, we propose HiKonv, a unified solution that maximizes the throughput of convolution on a given underlying processing unit with low-bitwidth quantized data as inputs through novel bit-wise management and parallel computation. We establish theoretical framework and performance models using a full-bitwidth multiplier for highly parallelized low-bitwidth convolution and demonstrate new breakthroughs for high-performance computing in this critical domain. For example, a single 32-bit processing unit in CPU can deliver 128 binarized convolution operations (multiplications and additions), thirteen 4-bit convolution operations or five 8-bit convolution operations with a single multiplication instruction, and a single $27 \times 18$ multiplier in the FPGA DSP core can deliver 60, 8 or 2 convolution operations with 1, 4 or 8-bit inputs in one clock cycle. We demonstrate the effectiveness of HiKonv on CPU and FPGA for both convolutional layers and a complete DNN model with our platform-oriented implementations. On CPU, HiKonv outperforms the baseline implementation with 1 to 5-bit inputs and provides up to $7.6 \times$ and $1.4 \times$ performance improvements for 1-D convolution. For the 2-D convolutional layer, HiKonv performs $2.74 \times$ and $3.19 \times$ the baseline implementation for 4-bit signed and unsigned data inputs. HiKonv also provides over $2 \times$ latency improvement for a complete DNN model on both Intel and ARM CPUs. On FPGA, the HiKonv solution enables a single DSP to process the same convolution operations that require multiple DSPs in the conventional convolution method with a shorter processing latency. For binarized input, each DSP with HiKonv is equivalent up to 76.6 LUTs. Compared to the DAC-SDC 2020 champion model for FPGA, HiKonv achieves a $2.37 \times$ throughput improvement and $2.61 \times$ DSP efficiency improvement, respectively.

Index Terms—Quantization, convolution neural network, high throughput, bit-wise management, FPGA, DSP, multiplier.

I. INTRODUCTION

Quantization is typically done by approximating high-precision floating point values to low-bitwidth integers or fixed-point representations. It is commonly used in the deployment of Deep Neural Network (DNN) models to reduce the cost (i.e., memory consumption) and improve performance (i.e., execution time) [1]–[6]. This is particularly important for modern DNN models, as many of them employ convolutional layers, which contain intensive multiplication and accumulation (MAC) operations [5]–[9]. Therefore, many novel quantization methods have been proposed in the literature to reduce the precision of weights, activations, and even gradients to low-bitwidth integers or fixed-point types for DNNs while retaining high model accuracy [2], [3], [6], [8], [10].

Despite the success of quantization for DNNs, the current deployment of quantized convolution to the computing platform is not ideal. To take advantage of the lower bitwidth of data from quantization, existing solutions tend to design new computing architectures that are specific to quantized convolutions [11]–[16], which lose the generality and take long application-specific integrated circuit (ASIC) design cycles. While for computing platforms with given fixed arithmetic units, there is no general support for quantized convolution operation. Most general processing units such as X86/64 CPUs and ARM processors have a high-bitwidth (such as 32 or 64 bits) multiplication-and-accumulation (MAC) unit for either floating-point numbers or integers [17], [18]. When they are used for quantized MACs, most of the bitwidths are left underutilized, wasting precious computing resources [18]–[21]. Even with the 8-bit multi-data processing of the Advanced Vector Extensions (AVX) support in X86/64 architecture, processing a single 4-bit multiplication would still occupy the 8-bit data channel with the remaining 4 bits simply wasted [18]. Waste becomes even more severe when either processing lower bitwidth (such as binary and ternary) data or utilizing a hardware unit with higher built-in bitwidths support. Reconfigurable hardware, such as FPGA, can alleviate some of the waste because of its bit-level flexibility for hardware configuration, but it exhibits similar drawbacks, especially when adopting the high-precision digital signal processing (DSP) units in the FPGAs [8], [17], [22]–[25]. Without careful bit-wise management of inputs and outputs, deploying quantized DNNs on FPGAs with the given DSPs still wastes a lot of their computation capacity [7], [19], [20], [24].

The lack of exploration of the relation of the low-level
computing pattern of existing MAC or multiplication units to convolution constrains further improvement of the processing performance of the given arithmetic units for quantized convolution. In this paper, we propose a novel solution, HiKonv, that maximizes the efficiency of the existing multiplication units when conducting convolution operations with quantized inputs, thus improving the throughput of quantized convolution on the arithmetic unit and reducing the end-to-end DNN computation latency. The major contributions of our HiKonv solution are as follows:

- We first conduct theoretical exploration to show that HiKonv’s bit-wise management is universal, and it adopts a single high-bitwidth multiplier for multiple quantized convolutions in a single multiplication operation. This technique can be applied to arbitrarily quantized bitwidths with a high-bitwidth multiplier unit.
- We then extend it to support arbitrary lengths of 1-D and 2-D convolutions with the corresponding bit management and computation.
- We build the theoretical analysis model that is used to explore the optimal design configurations with the given quantization bitwidths and the arithmetic unit.
- We provide two sets of implementations of HiKonv on general purpose processor and FPGA DSP, respectively, with different design considerations.
- Our experimental results further validate the general applicability of HiKonv, the effectiveness of the analytical model, and the performance improvement of our implementations. For example, our CPU-based implementation of HiKonv achieves up to $2.4 \times$ and $2.03 \times$ latency improvement for a 4-bit quantized DNN model on X86_64 CPU and ARM processor, respectively. The latency of our FPGA-based implementation of the DNN model outperforms the state-of-the-art implementation by $2.37 \times$.

Because of its generality, we believe that HiKonv opens up a new venue for further improving the hardware efficiency of DNN-based inferences. It not only improves the throughput and latency for existing quantized DNN models on existing hardware, but also offers new opportunities for designing new hardware-friendly quantized DNN models or co-designing both the hardware and quantized DNN models.

The rest of the paper is organized as follows. Section II surveys existing solutions for the processing of quantized convolutions. Section III introduces the preliminary information of our HiKonv solution, while Section IV presents the theoretical deduction of the HiKonv solution together with the detailed throughput analysis for optimal design configuration. Section V shows the implementations of HiKonv on general-purpose processors and FPGAs with different design considerations. Section VI presents the evaluation results. Finally, Section VII concludes this paper.

II. RELATED WORKS

The existing solutions for quantized convolution processing rely on the quantized multiply and accumulation support of the underlying processing units. These solutions can be classified into two categories: 1) solutions with dedicated hardware architecture for quantized/low-precision arithmetic and 2) solutions that rely on optimized software libraries to utilize the existing processing units more efficiently. Note that although modern General Purpose Processors (GPP) equipped with Single Instruction Multiple Data (SIMD) floating point processing units can also support certain low-bitwidth data processing, they belong to the software library category because the processing units can also be used for other general arithmetic operations, i.e., AVX2 in X86_64 CPUs and SSE in ARM processors. To support generality, in this work, we will only focus on the main computing structure, such as the Arithmetic and Logic unit (ALU) or the multiplier in the CPU or FPGA DSP, instead of dedicated hardware architectures.

A. Optimized software library

There are methods that pack/insert shorter bitwidth inputs into longer words and attempt to use the existing high-bitwidth computation units to improve the processing efficiency for quantized inputs $[18]$–$[20]$, $[29]$–$[31]$. These solutions are designed as software libraries to fully utilize the existing hardware units such as ALU and Floating Point Unit (FPU) in the X86_64 CPUs or ARM CPUs, etc. Here we consider the methods that do not involve the change of the existing hardware.

A library called Clover $[18]$ adopts the AVX support of X86_64 architecture and further extends it with an optimized 4-bit data container that reduces the memory access overhead. It simply adopts the 8-bit channel supported by the AVX architecture to process 4-bit data, with an online 4-bit to 8-bit extension. Although the performance of the system is improved, the speed-up is constrained by the number of supported channels by the AVX architecture.

CMSIS-NN $[31]$ is a set of software kernels for the execution of neural networks (NNs) on the ARM cortex-M CPUs, where the 16-bit single instruction multiple data (SIMD) MAC unit is used to process the low-bitwidth input data with a low-bitwidth to 16-bit conversion, i.e., 8-bit to 16-bit conversion. As the underlying MAC units only support 16-bit data inputs, all data with bitwidth lower than 16 is converted to 16-bit. Similar to Clover, the performance gain comes from efficient bitwidth conversion and full utilization of the 16-bit MAC channels.

PULP-NN $[30]$ is a software library specifically designed for GAP-8 $[32]$ processors. Each such processor contains 8 RISC-V cores with special DSP extensions. The execution of PULP-NN requires unique bit-wise operations, i.e., low-bitwidth data unpacking, data quantization instructions, etc., that are supported by the processor. It supports sub-word size data to reduce the memory access cost and fully utilizes the SIMD instructions to process data in parallel. It shows great efficiency due to the special instruction set, which also limits its flexibility.

B. Leveraging Reconfigurable Hardware

XILINX INT4 and INT8 $[19]$, $[20]$ support specifically for 4-bit and 8-bit processing on Xilinx FPGAs. They pack multiple inputs to enable multi-channel multiplication and can
be easily extended to process lower bitwidths than 4 and 8 by bitwidth extension. Particularly, both methods adopt existing 28 x 17 DSP units and pack the low-bitwidth data to the input ports to process two or four multiplication operations simultaneously, which improves the processing efficiency of the DSP. Although these solutions require the data to be either packed before sending to the DSP or use dedicated logic paths to pack the data during runtime, they use existing DSP units, and the solutions can be simply wrapped as High Level Synthesis (HLS) libraries.

C. Motivation

Developing dedicated hardware solutions requires long design cycles and also loses the flexibility to handle changing data types if the accelerator’s data path is fixed to a specific bitwidth. Software solutions on existing structures improve processing efficiency for quantized operations only by fully utilizing memory bandwidth or increasing the concurrency by a small factor, e.g., 2 or 4 [19], [20]. Furthermore, none of the existing solutions takes into account the internal relation between multiplication and convolution and the potential to further improve the throughput of quantized convolutions. There are no theoretical studies to guide the flexible management of low-bitwidth convolution computations. Our work, HiKonv, fills these existing gaps and provides theoretical guidance for the best computational efficiency and throughput on either existing hardware architecture or on new bit-efficient processing units for flexible low-bitwidth convolution computation.

III. PRELIMINARY

Our proposed HiKonv solution is inspired by the input packing for multi-channel multiplication on FPGA DSP [19], [20]. It adopts similar definitions as the existing input packing methods with proper extensions and revisions. In this section, we first look into the existing input packing method and then revisit the detailed operational pattern of a 1-D convolution.

A. Single Multiplier Multi-Channel Multiplication

Compared to simply expanding the low-bitwidth data to a higher bitwidth alternative, typically 16 or 32 bits, the multi-channel multiplication is a representative method used by current hardware units to process multiple low-bitwidth inputs concurrently [19], [20]. Particularly, multiple low-bitwidth values are packed together to form larger bitwidth multiplicands. By taking advantage of the shift-addition operation of the intermediate results during the process, the output of the high-bitwidth multiplications, Prod, can be separated into multiple individual channels holding results of low-bitwidth multiplications. The most representative example of multi-channel multiplication is the INT4 optimization for the Xilinx DSP48E2 unit, as shown in Figure 1. Each of the inputs contains two 4-bit integer values and form the inputs to the input ports A and B.

The separation of the four different output channel in Figure 1 provides the opportunity to simply segment out the required multiplication results Prod from the output port P. To avoid the overlapping of the results, some bits are reserved or filled with values during the packing of the low-bitwidth data. Note here, the \{V\} values are all unsigned integers (UINT4), and \{W\} values are signed integers (INT4). An INT4 x UINT4 multiplication generates a result with at least an 8-bit space. Here, the existing methods define the term guard bit as the filling 1s or 0s between the output results for the purpose of preventing the overflow of the multiplication. In this example, the value of guard bit is 3. The multiplication with four low-bitwidth inputs for this example is represented as:

\[
\text{Prod} = A \times B = (V_2 \cdot 2^{11} + V_1) \cdot (W_2 \cdot 2^{22} + W_1)
\]

\[
= V_2 W_2 \cdot 2^{33} + V_1 W_2 \cdot 2^{22} + V_2 W_1 \cdot 2^{11} + V_1 W_1
\]

The output of Equation 1 is the concatenation of four multiplication results with zeros between them due to the guard bits. This process accomplishes four channels of multiplication in one operation cycle with a large bitwidth multiplier.

B. 1-D Convolution

Denote \(F_{N,K}(f,g)\) as the conventional 1-D discrete convolution between an \(N\)-element sequence \(f\) and a \(K\)-element kernel \(g\). Here, we define the infinite-length sequence \(h\) as the extension of \(f\) with zero values to the index range of \((-\infty, \infty)\), as shown in Equation 2. The 1-D convolution is represented in Equation 3. Meanwhile, \(y'\) is the output with \(N+K-1\) non-zero elements.

\[
h[n] = \begin{cases} 
  f[n], & 0 \leq n < N \\
  0, & n < 0 \text{ or } n \geq N 
\end{cases} 
\]

\[
y'[m] = (h * g)[m] = \sum_{k=0}^{K-1} h[m-k]g[k]
\]
addition operations of continuous elements in \( h \) and \( g \), and we denote it as partial convolution.

\[
g[m] = \sum_{k+n=m} h[n]g[k]
\]

(4)

IV. MULTIPLIER FOR CONVOLUTION

There are two observations from the single multiplier multi-channel multiplication and 1-D convolution:

- First, multi-channel multiplication creates a set of multiplications and accumulations of low-bitwidth inputs within the operation of a single large bitwidth multiplication.
- Second, 1-D convolution is constructed with multiplications and accumulations of a set of contiguous data from two different data sequences.

Inspired by these two observations, we further extend multi-channel multiplication with a novel bit-wise management and generalize the solution for using a given hardware unit to process the maximum amount of low-bitwidth convolution operations concurrently. Furthermore, we provide theoretical guarantees for our solution.

First, we define the variables related to our exploration. As shown in Figure 2, we assume a given high-precision hardware unit that can multiply \( L_A \)-bit integer input \( A \) with \( L_B \)-bit integer input \( B \) and generate the product \( \text{Prod} \). The bitwidths of \( A \) and \( B \) define the computation capability of the hardware unit, or more specifically, the multiplier. Convolution input \( f \) and kernel \( g \) are the two sequences of low-bitwidth integer values quantized to \( p \) and \( q \) bits, respectively. Note here, Figure 2 is for the case where all elements of the sequences \( f \) and \( g \) are unsigned integers to ease the presentation of the HiKonv solution, and later we will show the generality of HiKonv for both signed and unsignned values as inputs.

To determine how to load \( A \) and \( B \) with multiple convolution operands from \( f \) and \( g \) and perform the convolution between these operands, we first define the concept of a slice, which is a certain length of consecutive bits in the input to hold the low-bitwidth input data, \( S \) is the size of a slice. Both input \( A \) and \( B \) are segmented with slices, as demonstrated on the left in Figure 2. The lower bits of each slice contains one element from \( f \) or \( g \). To simplify the problem, we assume that \( N \) and \( K \) are the maximum numbers of elements from \( f \) and \( g \) that fit into \( A \) and \( B \), respectively. Hence, the polynomial representations of \( A \) and \( B \) are:

\[
A = \sum_{n=0}^{N-1} f[n] \cdot 2^{S \cdot n}
\]

\[
B = \sum_{k=0}^{K-1} g[k] \cdot 2^{S \cdot k}
\]

(5)

Although the intermediate results of the multiplication are invisible to us, we assume that the processing unit takes the most ideal way of shift-add operations for the multiplication of two inputs, as shown in Figure 2. The entire multiplication is treated as the multiplication of slices in \( A \) with the slices in \( B \) followed by shifting the product left by \( S \) bits and accumulating the shifted result to the previous result. There are always \( N \times K \) products between elements from \( f \) and \( g \) that are calculated and accumulated to form the output.

A. From Multiplication To Convolution

To use the effective results from the product \( \text{Prod} = A \times B \), we need to guarantee that the expected convolution for the different low-bitwidth inputs can be easily segmented out. In order to segment the intermediate results, we extend the guard bits \( G_b \)'s definition that is introduced in Section III [19]. It is introduced in the output to prevent the overflow of the different multiplication results. In our proposed solution, the guard bits are not only to prevent overlaps between the effective product of two adjacent intermediate partial products but also to support the segmentation of the partial accumulations of vertically stacked partial multiplication results. Its length varies according to the maximum number of multiplication terms \( f[n] \cdot g[k] \) that are summed together. For a single multiplier, with \( A \) and \( B \) as inputs, a maximum of \( \min(K, N) \) terms are summed together for each output segment. Therefore, with our newly defined slice, to ensure the correctness of the final results, each slice should be capable of holding both the guard bits and the bits of the production from \( p \)-bit and \( q \)-bit inputs, respectively.

**Theorem 1.** Assuming a multiplier, with given \( A \) and \( B \) input multiplicands constructed from the \( N \)-element sequence \( f \) and the \( K \)-element sequence \( g \), where \( f \) and \( g \) are quantized to \( p \) and \( q \) bits, respectively, with the guard bits \( G_b \), we can obtain \( N + K - 1 \) segments from the product \( \text{Prod} = A \times B \) which are all short partial convolutions in the form of 1-D convolution.

**Proof.** Considering the guard bits, we can obtain:

\[
S = \begin{cases} 
q + G_b, & p = 1, q \geq 1 \\
p + G_b, & q = 1, p \geq 1 \\
p + q + G_b, & \text{otherwise}
\end{cases}
\]

(6)

\[
p + (N - 1)S \leq LA
\]

(7)

\[
q + (K - 1)S \leq LB
\]

(8)

Thus, we represent the \( A \times B \) multiplication with \( K \) intermediate stages. The intermediate stages are shifted left by \( S \) bits for every stage, and the effective vertical accumulation of the partial products in the segments from all the stages stacked together are aligned in the \( S \) bits segment, as shown in Figure 2. Then, the multiplication is represented as:

\[
\text{Prod} = A \times B = \left( \sum_{n=0}^{N-1} f[n] \cdot 2^{S \cdot n} \right) \cdot \left( \sum_{k=0}^{K-1} g[k] \cdot 2^{S \cdot k} \right)
\]

(9)

\[
= \sum_{m=0}^{N+K-2} \left( \sum_{n=m}^{n+K-1} (f[n] \cdot 2^{S \cdot n} \cdot g[k] \cdot 2^{S \cdot k}) \right)
\]

(10)

Different from general multiplications, convolution consists of a sequence of multiplications and accumulations. Referring to the form of the 1-D convolution in Equation 4, the result of \( \text{Prod} \) can be represented as:

\[
\text{Prod} = \sum_{m=0}^{N+K-2} y[m] \cdot 2^{S \cdot m}
\]
where intermediate accumulations form a 1-D convolution of two sequences in each of the output segments, and the total number of convolution segments is $N + K - 1$. With the equations above, we can obtain the minimum value of the guard bits under the condition of a single multiplier as follows:

$$G_b = \lceil \log_2 \min(K, N) \rceil \mid \text{Single multiplier} \hspace{1cm} (11)$$

to ensure that the properly accumulated partial products will not overflow.

According to the above, we can use a high-bitwidth multiplier to process two integers $A$ and $B$ to form $N + K - 1$ convolutions of low-bitwidth sequences.

### B. 1-D Convolution Extension

Now we have presented an efficient algorithm to use the multiplication unit on a hardware platform to perform the $F_{N,K}$ 1-D convolution. However, the size of $N$ is limited by the bitwidth of the hardware multiplier, whereas most real-world applications have much larger input sizes. Moreover, the $F_{N,K}$ 1-D convolution is often used as a unit building block for other larger-scale convolution operations. Thus, we design a new algorithm to use the $F_{N,K}$ 1-D convolution to complete arbitrarily large size 1-D convolutions and any arbitrary convolutions. As shown in Figure 2, the order of the elements for these intermediate production is controlled by the order of the elements packed into the slices in $A$ and $B$; it allows us to devise different accumulation methods to provide flexibility to construct different convolutions beyond the partial convolution on a single multiplier.

Regarding $F_{N,K}$ as a basic operation, we extend it to the $F_{X,N,K}$ convolution of a longer sequence by summing up the elements in output sequences of different $F_{N,K}$ convolutions.

**Theorem 2.** The output sequence $y = F_{X,N,K}$ of a 1-D convolution between an $(X \cdot N)$-element sequence $f$ and a $K$-element filter $g$ can be represented as the sum of index-shifted output sequences $y_x = F_{N,K}(f_x, g)$, as shown in Equation 14. Here, $f_x = f[xN:(x+1)N-1]$ ($x \in [0, X-1]$).

**Proof.** Following Equation 2, we extend $f$ and $f_x$ sequences into zero extension sequences $h$ and $h_x$. Then $h$ is represented as the sum of the index-shifted sequence $h_x$:

$$h[n] = \sum_{x=0}^{X-1} h_x[n - xN] \hspace{1cm} (12)$$

According to Equation 3, the convolution output $y$ is calculated with:

$$y[n] = \sum_{k=0}^{K-1} h[n-k]g[k]$$

$$= \sum_{k=0}^{K-1} \sum_{x=0}^{X-1} h_x[n - xN - k]g[k]$$

$$= \sum_{x=0}^{X-1} \sum_{k=0}^{K-1} h_x[n - xN]g[k]$$

Given that $y_x[n] = \sum_{k=0}^{K-1} h_x[n-k]g[k]$, we can represent the sequence $y$ as the sum of the index-shifted $y_x$ sequences:

$$y[n] = \sum_{x=0}^{X-1} y_x[n - xN] \hspace{1cm} (14)$$

Equation 14 reveals that the extended $F_{X,N,K}$ 1-D convolution is computed by a shift-accumulation pattern with $F_{N,K}$ base operation results. Figure 3 demonstrates how the elements in different $y_x$ are summed up to the elements in $y$. Each computed $y_x$ sequence is shifted $xN$ indices and then summed up to form the element of $y$, which is marked by the red and blue squares. In such a case, the guard bit of

$$G_b = \lceil \log_2 K \rceil \mid \text{1-D convolution} \hspace{1cm} (15)$$

is also adjusted with additional bits to prevent the partial results from overflowing.

### C. DNN Convolution Extension

Commonly, the convolution layer in DNN computes a feature map array $I[C_0][H_0][W_0]$ and a kernel array $W[C_0][C_1][K][K]$ for an output feature map array $O[C_0][H_o][W_o]$ (assuming $H_o = H_0 + K - 1$ and $W_o = W_0 + K - 1$) which can be represented as:

$$O[c_0][h][w] = \sum_{c_1=0}^{C_1-1} \sum_{k=0}^{K-1} \sum_{k_w=0}^{K-1} I[c_1][c][h+k_h][w+k_w]W[c_0][c_1][k_h][k_w] \hspace{1cm} (16)$$
For a DNN convolution, the output feature map $F$ is given by:

$$\left\lceil \frac{W}{N} \right\rceil - N$$

where $y_i$... For the accumulation of $M$ feature maps along the input channel in a convolution.

**D. Maximizing Processing Throughput**

We can derive the total number of effective operations with respect to the multiplications and the accumulations in each $F_{N,K}(f,g)$ convolution. For multiplication, there are a total of $K$ times $N$ product terms summed up to form the intermediate results, so the total number of multiplications performed in the 1-D convolution is $N \times K$. Meanwhile, the $N + K - 1$ sets of product terms are summed up to form one element in the output sequence. By excluding zero products, we calculate the total operation number in one $F_{N,K}(f,g)$ convolution in Equation 24.

$$G_b = \lfloor \log_2(M \cdot \min(K, N)) \rfloor | DNN \ convolution \ (23)$$

A convolution layer in DNN has multiple input and output channels, which require accumulations of channel-wise features to form the final output. By grouping the $F_{N,K}$ output sequences with different $c_i$ but the same $c_{0}, h, k_b$, and $x$ indices and accumulating the corresponding product $Prod$, we can perform the channel-wise accumulation of the feature maps. In this case, the required number of guard bits is

$$G_b = \lfloor \log_2(M \cdot \min(K, N)) \rfloor | DNN \ convolution \ (23)$$

for the accumulation of $M$ feature maps along the input channel in a convolution.

**Theorem 3**. For a DNN convolution, the output feature map can be computed using the $F_{X,N,K}$ 1-D convolution with the following equation:

$$O[c_i][h][w] = \sum_{c_i=0}^{C_i-1} \sum_{k_h=0}^{K-1} y_{c_i,c_0,h,k_h}[w+K-1] \ (17)$$

where $f$ and $g$ are defined as:

$$f[w] = \begin{cases} I[c_i][h+k_b][w] & 0 \leq h < H_i, 0 \leq i < W_i \\ 0 & \text{otherwise} \end{cases} \ (19)$$

$$g = W[c_0][c_i][k_b][K-1]$$

Proof. For abbreviation, we denote the sequence $y_{c_i,c_0,h,k_b}$ as $y'$. According to the definition of the 1-D convolution, the sequence $y'$ can be computed using the following equation:

$$y'[n] = \sum_{k=0}^{K-1} f[n-k]g[k]$$

$$= \sum_{k=0}^{K-1} I[c_i][h+k_b][n-k]W[c_0][c_i][k_b][K-1-k] \ (20)$$

Then, we have

$$y_{c_i,c_0,h,k_b}[n+K-1] = \sum_{k=0}^{K-1} I[c_i][h+k_b][n+k]W[c_0][c_i][k_b][k] \ (21)$$

With Equation 21, Equation 16 could be represented as:

$$O[c_0][h][w] = \sum_{c_i=0}^{C_i-1} \sum_{k_h=0}^{K-1} \sum_{k_w=0}^{K-1} I[c_i][h+k_b][w+k_w]W[c_0][c_i][k_b][k_w]$$

$$= \sum_{c_i=0}^{C_i-1} \sum_{k_h=0}^{K-1} \sum_{k_w=0}^{K-1} I[c_i][h+k_b][w+k_w]W[c_0][c_i][k_b][k_w] \ (22)$$

Subject to:

$$0 < N$$

$$0 < K$$

$$p + (N - 1)(p + q + G_b) \leq L_A$$

$$q + (K - 1)(p + q + G_b) \leq L_B$$

Where in the different convolution conditions, we have different guard bits constraints:

$$G_b = \begin{cases} \lfloor \log_2\min(K, N) \rfloor, & \text{Single multiplier;} \\ \lfloor \log_2(K) \rfloor, & \text{1-D convolution;} \\ \lfloor \log_2(M \cdot \min(K, N)) \rfloor, & \text{DNN convolution.} \end{cases}$$

Then we solve this optimization problem with a straightforward search algorithm by iterating all possible pairs of $N, K$ to find the optimal configuration, as shown in Algorithm 1. After the search, the optimal configuration of $N, K$ with
Algorithm 1 Optimal Throughput Search

1: \( \text{Max}_N = (L_A - p) / (p + q) + 1, \text{Opt}_K = 0 \)
2: \( \text{Max}_K = (L_B - q) / (p + q) + 1, \text{Opt}_N = 0 \)
3: \( \text{Max}_{ops} = 0 \)
4: for \( k = 1, k < \text{Max}_K, k++ \) do
5:   for \( n = 1, n < \text{Max}_N, n++ \) do
6:     \( \text{Cond}_1 = p + (n - 1)(p + q + G_b) \leq L_A \)
7:     \( \text{Cond}_2 = q + (k - 1)(p + q + G_b) \leq L_B \)
8:     \( \text{Cur}_{ops} = n \times k + (n - 1) \times (k - 1) \)
9:     if \( \text{Cond}_1 \& \text{Cond}_2 \& \text{Cur}_{ops} > \text{Max}_{ops} \) then
10:       \( \text{Opt}_N = n, \text{Opt}_K = k, \text{Max}_{ops} = \text{Cur}_{ops} \)
11:   end if
12: end for
13: end for
14: Return \( \text{Opt}_N, \text{Opt}_K, \text{Max}_{ops} \)

the maximum operations performed with a single multiplier is obtained.

Figure 4 shows two examples of multipliers with different bitwidth configurations. For a given high bitwidth processing unit, the maximum supported throughput (multiplication and addition) of a given processing unit varies with \( N \) and \( K \), which are determined by the values of \( p \) and \( q \). For example, when the input bitwidths of a multiplier are 27 and 18 bits, respectively (Figure 4a), according to Equation 6, 7, 8 and 11, we could obtain \( S = 4, N = 9, K = 4 \) when \( p \) and \( q \) are both 1-bit binary values. The maximum supported throughput of this specific multiplier is equivalent to 60 ops per cycle, which are 36 multiplications and 24 additions that are required for computing the convolution if all the computation is carried out in a conventional way following the 1-D convolution algorithm without HiKonv. Here, with HiKonv, one multiplication of high-bitwidth multiplier with our specific slicing/packing solution is equivalent to it. In addition, when \( p \) and \( q \) are both 4 bits, the multiplier provides 8 equivalent operations per cycle (6 multiplication and 2 addition). In Figure 4, we show the configurations for \( p \) and \( q \) from 1-bit to 8-bit, which are the common bitwidths of low-precision quantization. The principle generally applies to all bitwidths. When the inputs for the multiplier are both 32 bits, these values are further increased to 128 ops per cycle and 13 ops per cycle for 1-bit and 4-bit \( p \) and \( q \), as shown in Figure 4b. For the 1-D and DNN convolution layer, we only need to change the \( G_b \) constraint in the searching algorithm and proceed with the straightforward search to obtain the optimal values.

E. Sign Extension for Sign Integers

HiKonv differs from conventional multi-channel multiplication methods [19], [20] with a more comprehensive bit-wise management of the input data and more efficient use of the outputs. To implement HiKonv on the existing computing platforms, including GPP and FPGA, the overall processes are abstracted as input packing, large bitwidth multiplication and output split. Regarding Equation 5, packing the input is equivalent to extending low-bitwidth data to higher bitwidth and then performing accumulation of multiple extended data. However, the two’s complementary representation in modern computing systems performs sign extension when low-bitwidth data is extended to a larger bitwidth length. Therefore, in the form of binary representation, the low-bitwidth input that has been packed into the left segment is a combination of the low-bitwidth data itself with the sign extension of the data in the segment to the right of it.

Same as the input packing, extraction of \( y[m] \) from the \( Prod \) can not be simply processed with bit-wise segmentation because the previous segment’s sign is continuously added to the current segment. More specifically, for \( y[m + 1] \), if \( y[m] \) is a negative value, its sign extension stands for \(-1\), which in turn passes the sign extension to the segment on its left. The sign of the segments must be considered to extract the correct value of \( y[m] \).

V. PLATFORM ORIENTED IMPLEMENTATIONS

Compared to the multiplication operation, the above packing and split operations have different architectural preferences due to the unique bit-wise operations, such as adopting shift registers or using unique hardware logic for efficient processing. In this section, we provide detailed implementations of HiKonv regarding the architectural characteristics of the general-purpose processors and reconfigurable platforms.
Algorithm 2 1-D HiKonv with single multiplier on GPP

```
1: for n = 0, n < N, n++ do            ▷ Pre-packing
2:      A = A + f[n] << (s * n)        
3: end for
4:
5: prev = A * B                         ▷ Prologue multiplication
6:
7: for c = N, c < M, c++ do             ▷ Input data packing
8:      for n = 0, n < N, n++ do       
9:          A = A + f[c+n] << (s * n)  
10: end for
11:
12: this = A * B                        ▷ Intermediate product shifting
13: y = prev << ((s * (N-1)) + this << s)  ▷ Multiplication
14:
15: for n = 0, n < N, n++ do            ▷ Output data splitting
16:      output[c-n] = (y >> (s * (N-n-1))) & (2s-1)
17: // carried_sign = y >> (s * (N-n-1)) - 1
18: // output[c-n] = output[c-n] + carried_sign
19: end for                               ▷ Signed HiKonv: Check for the sign bit
20:
21: end for                               
22: Return output
```

A. HiKonv on General Purpose Processors

We provide two versions of the HiKonv implementation on general-purpose processors, including both Intel X86_64 CPUs and ARM processors. Modern CPUs are usually 64-bit processors that are equipped with 32-bit integer multipliers. With such an architecture, a 32-bit multiplication is performed with 32-bit registers as operands while 64-bit is constructed using two 32-bit registers. The 64-bit product is stored in two 32-bit registers: the upper half in one and the lower half in the other. A 64-bit multiplication is done in the same way, except that the registers are 64-bit registers. Thus, without loss of generality, we use 32-bit multiplication for our HiKonv implementations.

1) Basic HiKonv Operations: HiKonv supports operations between positive and negative integer inputs. Meanwhile, most activations and weights in many modern neural networks can be trained to only positive numbers. It is beneficial to utilize an unsigned version of HiKonv as the implementation is simpler than the signed HiKonv, which requires sign checking in both input packing and output splitting (detailed in the following subsections). Due to the different implementation requirements, we provide two sets of HiKonv implementations, which are the HiKonv implementation that only supports unsigned input and the HiKonv implementation that supports signed inputs, on general-purpose processors. The unsigned HiKonv implementation only operates with positive integer inputs, and the signed HiKonv implementation supports both positive and negative inputs. The implementations of the three main processes are shown in Algorithm 2. Except the major input packing, multiplication and output split operations, there are additional operations named as Pre-packing and Alignment due to the efficient shifting and store-and-accumulate operations on the ALU in GPPs. We explain each step in the following.

1) Input data packing According to Equation 9, we can construct the large bitwidth inputs with shift-add operations. For an input vector with N segments, we need \( N - 1 \) shift-add operations to pack the input data properly. To pack an input, \( f[n] \) needs to be shifted by \( s \times n \) bits to the left and then accumulates to the input bit-vector. Packing the other input to the multiplier follows the same procedure. In the context of computing convolutional neural networks, the features need to be packed during the runtime, whereas the weights can be pre-packed, enabling further optimization opportunities. This step is the same for both the signed and the unsigned implementations of HiKonv.

2) Intermediate product shifting We adopt the horizontal stacking strategy discussed in Section IV. As seen in Figure 2 the output of one block depends on the multiplication results from both the present and the previous iterations. The multiplication operation is inherently multiply-accumulate between the two outputs; however, the two results need to be aligned and accumulated to produce the output correctly in an output segment. Considering the limited length of the shift registers in GPPs, we shift the partial result from the previous iteration to the right and the partial result from the current iteration to the left by the appropriate number of bits, respectively. Once they are properly aligned, we add them together to construct the complete result for this iteration and extract the bits for the output.

3) Output data splitting This step differs between the signed and unsigned implementations, as shown in Algorithm 2. Due to the sign extension in GPP platforms, dealing with signed values requires checking the sign bits in different segments, where we take an additional step to check the sign of the preceding output. As seen in Equation 30 the most effective way is to shift the output and check the sign bit immediately preceding the current output segment. If the sign equals to one, indicating that the segment to the right is a negative number, we need to compensate and adjust the current output. In the unsigned version of HiKonv, since all numbers are positive, there is no need to perform the sign bit checking.

2) 1-D Convolutions with HiKonv: For 1-D convolution, the baseline implementation has nested loops of two levels. The outer loop scans through the input sequence, whereas the inner loop scans through the kernel sequence. In the implementation of 1-D convolution with HiKonv, we only need one loop to compute the convolution, as demonstrated by Algorithm 2. We need a prologue to perform the first multiplication operation and set up the convolution iterations. In each of the iterations, it performs the basic three operations in HiKonv, including input data packing, intermediate product shifting, and output data splitting. There is only one multiplication in each loop; the number of bits to shift and bit-masks can be pre-calculated and pre-defined offline based on Algorithm 2.

To better illustrate the 1-D convolution with HiKonv, we provide the following numerical example in Figure 5. We demonstrate a \( F_{3,2} \) convolution where we convolve the three-element array \( [11, 9, 7] \) with a two-element kernel \( [3, 2] \). The result of the convolution should be \( [33, 49, 39, 14] \). On the left of Figure 5 we show how we pack the inputs into two 32-bit bitstrings and perform the multiplication...
Input data packing

Algorithm 1 based on the target bitwidth of the inputs, Nresource that contains a target the Xilinx FPGA platforms, which provide DSP48E2 flexibility in both input data packing and output splitting with a

Figure 5: A numerical example of a $F_{3,2}$ 1-D convolution.

with binary values. On the right, we show the ideal process in decimals. It is easy to compare and see how the convolution can be converted into one multiplication of which the product contains the results of the convolution output. In practice, the binary multiplicands are 11543559 and 3074 in decimal. Their product is 35484900366, which is 1000100001100010001001110000001110 in binary as shown on the left of Figure 5.

3) 2-D Convolutions with HiKonv: We implement the DNN layer by embedding the 1-D convolution in the six-level nested loops that scan through the input channel, output channel, output height, output width, kernel height, and kernel width according to Theorem 3. The order of the nested loop does not have an impact on the functionality. In order to fit the 1-D convolution algorithm into the context of 2-D convolution, we arrange the order of the loops in such a way that we first compute the partial results of each row and then accumulate them in the channel dimension. HiKonv supports even higher dimensional convolution with a similar approach.

B. HiKonv on Reconfigurable Hardware

Reconfigurable hardware provides a finer granularity control of the data path down to a single bit. We take advantage of the flexibility in both input data packing and output splitting with a small number of additional logic resources to further improve the effectiveness of the required operations. Particularly, we target the Xilinx FPGA platforms, which provide DSP48E2 resource that contains a $27 \times 18$ bits multiplier [19].

1) HiKonv for single DSP: To deploy HiKonv on a single FPGA DSP, we first explore the optimal $N$, $K$, and $S$ values with Algorithm 1 based on the target bitwidth of the inputs, and configure the hardware unit with these parameters.

1) Input data packing Since the packing of the elements is equivalent to performing a long bitwidth shift add operation, if $f$ and $g$ are all unsigned integers, we can construct $A$ and $B$ with bit-wise assignments to the corresponding slice with a simple zero extension:

$$A[S(n+1)-1:S_n] = f[n]$$

$$B[S(k+1)-1:S_k] = g[k]$$

When $f$ and $g$ contain signed integers, instead of performing an extension-shift-addition operation, we simplify the logic to check the sign bit of the low bitwidth data before packing it into the slices. As shown in Figure 6 taking the second slice as an instance, in two’s complement expression, if $f[0]$ is positive, the MSB is 0, and the sign extension part is all zero. On the other hand, if $f[0]$ is negative, the sign extension part is all 1 in the binary representation and represents -1 in the two’s complement representation. To take advantage of the bit flexibility of FPGA devices, we still perform a bit-wise assignment of the input data to the slice but with an online checking of the sign value of the previous slice. Equation 29 shows the packing formula for the signed integers from $f$ and $g$ into the $A$ and $B$ multiplicands.

$$A[S(n+1)-1:S_n] = \begin{cases} f[0], & n = 0 \\ f[n]-A[Sn-1], & n > 0 \end{cases}$$

$$B[S(k+1)-1:S_k] = \begin{cases} g[0], & k = 0 \\ g[k]-B[Sk-1], & k > 0 \end{cases}$$

In such a condition, when packing $f[1]$ into the second slice, we can decrement 1 from $f[1]$ to obtain the value in that slice. To simplify the logic, there only requires a simple 1-bit decrementer before the concatenation of the changed values to form the entire multiplicand; whether enabling this 1-bit decrementer is based on the sign bit from the previous slice, as shown as the Packing Decrementers in Figure 8.

Note here, due to the pre-adder in the Xilinx DSP48E2 module, resource for one of the Packing Decrementers can be saved with this pre-adder, but it is omitted here to simplify the presentation. The packing process works recursively for all the slices. This approach saves the resource from using large bitwidth shift registers and adders and, in return, only costs a small decrementer and single-bit Boolean logic.

2) Large bitwidth production The production is done with the adoption of the multiplier in the FPGA DSP, noted as DSP multiplier in Figure 8; the packed weight sequence and feature sequence are directly provided to the 27-bit and 18-bit input data ports of the multiplier. The output is obtained in a single clock cycle with a pipeline depth of 1. In this way, with a single multiplication, multiple low-bitwidth multiplications and additions are performed.

3) Output split Output split is a reversed process of packing the data into slices. The final output of the production is formed by multiple $y[m]$ values. Each of the current S-bit segmentation carries on the impact of the sign bit from the S-bit segmentation to the right of it, except for the very right segmentation, as shown in Equation 30. Due to the two’s complement representation of the values in modern computing systems, the sign extension mechanism extends the sign value of current $y[m]$ to the MSB of...
the final output, so the value of each \( y[m] \) is a function of the current value in the current segmentation with the sign value in the previous segmentation, as shown in the Equation 30. Similarly, the implementation of Equation 30 adopts a simple incrementer as the input packing instead of using a shift-and-add module that requires more logic resources.

\[
y[m] = \begin{cases} 
  \text{Prod}[S:1:0], & m = 0 \\
  \text{Prod}[S(m+1):Sm] + \text{Prod}[Sm-1], & m > 0
\end{cases}
\]  

(30)

2) Single convolver architecture: For quantized convolution in DNNs, weight data can be compressed prior to inference by discarding the unused bits during quantization [2], [3], [8], as shown in Figure 7. The compressed weights reduce the memory access overhead by a fraction of the reduced bits and also simplify the data transfer logic to save hardware resources. For example, compressing the weights quantized to 4 bits reduces memory to 1/8 compared to the original 32 bits data type for storage. The same compression can also be applied to the feature data during runtime. Both weight and feature data can be extracted at runtime from the compact weight sequence and feature sequence and packed into the slices of the multiplier’s inputs without affecting throughput. With the integration of the input data pack and the output split, the microarchitecture of a new convolver that is mainly built with FPGA DSPs is shown in Figure 8.

A certain number of elements of the compressed weight sequence and the feature sequence are first buffered in Input Registers, and then passed to Packing Decrementer, which is constructed with multiple decrementers, as discussed in the previous section. The two inputs to the multiplier are then packed as multiplicands and passed to the multiplier of the DSP in the FPGA chip. The number of decrementers is based on the previously explored \( N \) and \( K \) with Algorithm 1. The decrementers provide the packed values in a single clock cycle, and Prod is obtained after one clock cycle from the DSP and passed to the incrementer logic to obtain the final output.

With this architecture, we obtain \( N + K - 1 \) partial convolutions from \( N \times K \) segments of intermediate results from a single multiplier to process signed input data. While for unsigned data processing, the Packing Decrementers and Split Incrementers can all be reduced, which in return occupies less logic resource.

3) 1-D & DNN layer Convolution Architecture: The HiKonv 1-D convolution on FPGA is based on Equation 14. Different from the single DSP convolver, the guard bits here need to be adjusted to \( G_b = \lceil \log_2 K \rceil \) so that the partial additions do not overflow. After the adjustment of the guard bits, a single convolver is recursively used to process the input and weight sequences. It requires an additional register to temporarily store the output result of current multiplication to continuously construct new convolution outputs by shifting the stored data and adding it with the new output from the DSP multiplier, as shown in Figure 9.

However, for a convolutional layer in a DNN, a single output involves data from multiple input features even after the input channels are tiled; based on the Equation 22, we first change the guard bits to \( G_b = \lceil \log_2 (M \cdot \min(K, N)) \rceil \), so the \( S \) bit slice is enough to hold the accumulation results from \( M \) feature maps. This also enables us to perform the addition operation between the different input channels before Split Incrementers to further reduce the number of 1-bit incrementers to save resources, as shown in Figure 10.

VI. Evaluations

HiKonv is a general technique that can be adopted for both the GPP and reconfigurable hardware platforms. We demonstrate its efficacy on both platforms with the proposed implementations in Section VI.

A. HiKonv on GPPs

To demonstrate the generality of our proposed HiKonv solution, we test the implementations for GPP on the Intel desktop CPU platform, Intel mobile CPU platform, and ARM platforms. Specifically, the implementations are evaluated on the Intel Core i7-10700K CPU, the i7-10710U CPU, and the Raspberry Pi 3B+ platform with an ARM Cortex A53 processor, respectively.

1) Convolution layer evaluation: We first measure the performance of the 1-D convolution with low-precision bitwidths from 1 to 8 bits. For quantified analyses, we randomly generate feature and kernel vectors. Since modern CPUs are equipped with 32-bit multipliers, without loss of generality, we use \( A = B = 32 \) bits as the multiplication bitwidth. Assuming \( p = q \), we calculate the corresponding \( N \), \( K \), and \( G_b \) and...
Weight sequence: \( w_n \ldots w_2, w_1, w_0 \)

\[
G \quad b \quad f_1 \quad f_0 \quad G_b \ldots y_0 y_1 y_{n-1} \quad \text{Prod}\left[3S-1:2S\right] \quad \text{Prod}\left[3S-1:2S\right] \\
\text{<<} + + \text{ForM input features Intermediate Adder} \quad \text{Dec. Dec. Dec.} \\
\]

64 CPUs. The speedups are

\[
\begin{align*}
\text{HiKonv solution.} & \quad \text{performance improvements demonstrate the generality of our HiKonv solution.} \\
\end{align*}
\]

The same performance improvement has been observed on the ARM processor, as shown in Figure 13a and Figure 13b. Compared to naive implementation on an ARM processor, the speedups for signed and unsigned data input reach 2.21× and 3.06× for 1-D convolution and 2.75× and 2.98× for 2-D convolution. Although all results are magnitude slower than the implementations on Intel X86_64 CPUs, the speedups are only slightly reduced due to the constrained cache size and memory access capability on the ARM processors.

2) Complete model evaluation: To demonstrate the performance of HiKonv in the DNN context, we implement the entire UltraNet with convolution layers based on the HiKonv solution to evaluate on GPPs. In this experiment, we also perform the calculations in integers for both naive and HiKonv implementations to be consistent with the previous experiments and ensure a fair comparison.

Figure 12: Evaluation with 4-bit layers on X86_64 CPUs.

Figure 13: Evaluation with 4-bit layers on ARM.
configured to use DSP resources but without adopting the HiKonv solution is noted as Conv-DSP. We also configure the convolver without adopting HiKonv and DSP resources, noted as Conv-LUT. The DSP and LUT resource utilization data are shown in Table I together with the processing latency of the generated hardware module counted in clock cycles.

Clearly, compared to the conventional convolvers with DSPs, the HiKonv solution uses a single DSP but performs the same amount of computation, whereas the conventional convolvers cost multiple DSPs. HiKonv convolver occupies slightly more LUTs than conventional convolver when customized for 6-bit inputs because the Packing Decrementer and Split Incrementer consume more LUTs; however, when the bitwidth is reduced, the HiKonv convolvers cost even less LUTs than the conventional convolvers. HiKonv-based convolvers always provide shorter processing latency since the multiplication and addition operations all happen in the single multiplication without the loop for accumulation as in normal convolution. The comparison with Conv-LUT further shows the reduced LUT resource with the effective use of DSP. The saving of LUT becomes more significant when the input bitwidth is smaller.

2) Comparison to Binary convolution layer: We then evaluate the extreme case of quantized convolution, which is binary neural networks (BNN). A convolutional layer in a BNN takes the binary inputs for both feature maps and kernel weights, processes the convolution between them, and generates the outputs. Note that the outputs may not be binary due to channel-wise accumulation. We first implement a binary convolution layer with 4-bit outputs without using the DSP resources, denoted as BNN-LUT; we then configure a binary computation module with our HiKonv solution, denoted as BNN-HiKonv. In comparison, we evaluate the resource utilization of these two designs under the same concurrency and the same clock frequency setting, as shown in Table II.

Clearly, compared to BNN-LUT, the LUT usage of BNN-HiKonv is reduced. However, the throughput for each DSP reduces when the concurrency increases because there is more vertical stacking, and it takes more guard bits when the concurrency increases. The equivalent number of LUTs replaced by one DSP (LUT/DSP) varies from 43.7 to 76.6 due to the accumulation logic in the convolution operation. HiKonv creates opportunities to leverage DSPs for high-throughput BNN (or other low-bitwidth models) convolution computations that would help map a larger BNN with high concurrency into the same FPGA. It can also potentially increase the design’s clock frequency since DSPs can run at a higher frequency than LUTs.

3) Complete model evaluation: We apply our HiKonv solution to the entire UltraNet model [33] on the Xilinx Ultra96 MPSoC FPGA. The HiKonv convolution is implemented in the programmable logic as an accelerator for convolutions. The weight and activation of this model are quantized to 4-bit. We execute all the convolution layers on the programmable logic and the other layers on the ARM processor on the FPGA platform. We follow the same layer architecture and system architecture as the original UltraNet design and only change the computation for convolution with our HiKonv

![Figure 14: 4-bit Ultranet full model evaluation.](image)
solution. Besides using DSPs, we also use small adders and shifters constructed by LUTs, taking advantage of the flexible configuration features of the FPGA.

In addition to resource utilization, we also measure the throughput in frame-per-second (fps) and calculate the DSP efficiency in terms of Giga-operations-per-second-per-DSP (Gops/DSP) for comparison as shown in Table III. All the testing data is first loaded into the DDR to leverage the full capacity of the accelerators in our evaluations.

Table III: UltraNet resource and performance.

|             | LUT | DSP | fps | DSP Eff. (Gops/DSP) |
|-------------|-----|-----|-----|---------------------|
| UltraNet    | 4.3k| 360 | 248 | 0.289               |
| UltraNet-HiKonv | 4.8k| 327 | 401/588 | 0.514/0.753       |

UltraNet-HiKonv uses more LUT resources than the original implementation due to the shifting and adding logic; however, it reduces the DSP utilization thanks to the dramatic improvements in the efficiency and the throughput of the DSPs. The original implementation of the UltraNet uses one DSP for two 4-bit MACs that are natively supported by the synthesis tool. It only achieves 248 fps with a 0.289 Gops/DSP efficiency. With our HiKonv solution, the onboard implementation of UltraNet achieves 401 fps with a 0.514 Gops/DSP DSP efficiency. This significant improvement is achieved under the constraint that the software execution on the ARM core is not fast enough to feed the input data to the FPGA accelerator to process, even with our best software optimization of multi-threading and data buffering. If this ARM core bottleneck is removed, the UltraNet-HiKonv accelerator can reach an even higher performance of 588 fps with the DSP efficiency of 0.753 Gops/DSP.

VII. CONCLUSION AND DISCUSSION

In this paper, we present HiKonv, a general technique with theoretical guarantees for using a single multiplier unit to process multiple low-bitwidth convolution operations in parallel for significantly higher computation throughput with flexible bitwidths. It is able to support convolutions in DNNs and achieves the highest possible throughput for quantized convolution with novel bitwise management and computation. As a demonstration of its general applicability and benefits, we show that HiKonv has achieved 3.17× throughput improvement on CPU and 2.37× and 2.61× throughput and DSP efficiency improvements for the DAC-SDC 2020 champion model on FPGA. HiKonv suits both software and hardware optimizations and provides new opportunities for future hardware designs for efficient DNN processing.

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REFERENCES

[1] A. Gholami, S. Kim, Z. Dong, Z. Yao, M. W. Mahoney, and K. Keutzer, “A Survey of Quantization Methods for Efficient Neural Network Inference,” CoRR, vol. abs/2103.13630, 2021.

[2] C. Gong, T. Li, Y. Lu, C. Hao, X. Zhang, D. Chen, and Y. Chen, “µL2Q: An Ultra-Low Loss Quantization Method for DNN Compression,” in Proceedings of the International Joint Conference on Neural Networks. IEEE, 2019, pp. 1–8.

[3] C. Gong, Y. Chen, Y. Lu, T. Li, C. Hao, and D. Chen, “VecQ: Minimal Loss DNN Model Compression With Vectorized Weight Quantization,” Transactions on Computers, vol. 70, no. 5, pp. 696–710, 2021.

[4] X. Zhang, H. Lu, C. Hao, J. Li, B. Cheng, Y. Li, K. Rupnow, J. Xiong, T. Huang, H. Shi, W.-M. Hwu, and D. Chen, “SkyNet: a Hardware-Efficient Method for Object Detection and Tracking on Embedded Systems,” in Proceedings of Machine Learning and Systems (MLSys), 2020.

[5] X. Zhang, J. Wang, C. Zhu, Y. Lin, J. Xiong, W.-m. Hwu, and D. Chen, “DNNBuilder: An Automated Tool for Building High-Performance FPGA Hardware Accelerators for FPGAs,” in Proceedings of the International Conference on Computer-Aided Design, 2018.

[6] C. Hao, X. Zhang, Y. Li, S. Huang, J. Xiong, K. Rupnow, W.-m. Hwu, and D. Chen, “FFPA/DNN Co-Design: An Efficient Design Methodology for IoT Intelligence on the Edge,” in Proceedings of the 56th Annual Design Automation Conference, 2019.

[7] Y. Chen, J. He, X. Zhang, C. Hao, and D. Chen, “Cloud-DNN: An Open Framework for Mapping DNN Models to Cloud FPGAs,” in Proceedings of the 2019 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, 2019.

[8] Y. Chen, K. Zhang, C. Gong, C. Hao, X. Zhang, T. Li, and D. Chen, “T-DLA: An Open-source Deep Learning Accelerator for Ternarized DNN Models on Embedded FPGA,” in Proceedings of 2019 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2019, pp. 13–18.

[9] Y. Li, X. Zhang, and D. Chen, “CSRNet: Dilated convolutional neural networks for understanding the highly congested scenes,” in 2018 IEEE/CVF Conference on Computer Vision and Pattern Recognition, 2018, pp. 1091–1100.

[10] S. Zhou, Z. Ni, X. Zhou, H. Wen, Y. Wu, and Y. Zou, “DoReFaNet: Training Low Bitwidth Convolutional Neural Networks with Low Bitwidth Gradients,” CoRR, vol. abs/1606.06160, 2016.

[11] H. Sharma, J. Park, N. Suda, L. Lai, B. Chau, V. Chandra, and H. Esmaeilzadeh, “Bit Fusion: Bit-Level Dynamically Composable Architecture for Accelerating Deep Neural Networks,” in Proceedings of the 45th Annual International Symposium on Computer Architecture, ser. ISCA ’18, 2018, p. 764–775.

[12] S. Ryu, H. Kim, W. Yi, and J.-J. Kim, “BitBlade: Area and Energy-Efficient Precision-Scalable Neural Network Accelerator with Bitwise Summation,” in Proceedings of the 56th Annual Design Automation Conference 2019, 2019, pp. 1–6.

[13] D. Shin, J. Lee, J. Lee, J. Lee, and H.-J. Yoo, “DNPU: An Energy-Efficient Deep-Learning Processor with Heterogeneous Multi-Core Architecture,” IEEE Micro, vol. 38, no. 5, pp. 85–93, 2018.
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[14] J. Lee, C. Kim, S. Kang, D. Shin, S. Kim, and H.-J. Yoo, “UNPU: An Energy-Efficient Deep Neural Network Accelerator With Fully Variable Weight Bit Precision,” *IEEE Journal of Solid-State Circuits*, vol. 54, no. 1, pp. 173–185, 2019.

[15] S. Sharify, A. D. Lasconz, K. Siu, P. Judd, and A. Moshovos, “Loom: Exploiting Weight and Activation Precisions to Accelerate Convolutional Neural Networks,” in *Proceedings of the 55th Annual Design Automation Conference*, ser. DAC ’18, 2018.

[16] S. Rasoulinezhad, H. Zhou, L. Wang, and P. H. Leong, “PIR-DSP: An FPGA DSP Block Architecture for Multi-precision Deep Neural Networks,” in *2019 IEEE 27th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, 2019.

[17] X. Zhang, A. Ramachandran, C. Zhuge, D. He, W. Zuo, Z. Cheng, K. Rupnow, and D. Chen, “Machine Learning on FPGAs to Face the IoT Revolution,” in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design*, 2017.

[18] A. Stojanov, T. M. Smith, D. Alistarh, and M. P¨uschel, “Fast Quantized S. Rasoulinezhad, H. Zhou, L. Wang, and P. H. Leong, “PIR-DSP: An FPGA DSP Block Architecture for Multi-precision Deep Neural Networks,” in *2019 IEEE 27th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, 2019.

[19] J. Lee, C. Kim, S. Kang, D. Shin, S. Kim, and H.-J. Yoo, “UNPU: An Energy-Efficient Deep Neural Network Accelerator With Fully Variable Weight Bit Precision,” *IEEE Journal of Solid-State Circuits*, vol. 54, no. 1, pp. 173–185, 2019.

[20] A. Stojanov, T. M. Smith, D. Alistarh, and M. P¨uschel, “Fast Quantized S. Rasoulinezhad, H. Zhou, L. Wang, and P. H. Leong, “PIR-DSP: An FPGA DSP Block Architecture for Multi-precision Deep Neural Networks,” in *2019 IEEE 27th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, 2019.

[21] J. Lee, C. Kim, S. Kang, D. Shin, S. Kim, and H.-J. Yoo, “UNPU: An Energy-Efficient Deep Neural Network Accelerator With Fully Variable Weight Bit Precision,” *IEEE Journal of Solid-State Circuits*, vol. 54, no. 1, pp. 173–185, 2019.

[22] A. Stojanov, T. M. Smith, D. Alistarh, and M. P¨uschel, “Fast Quantized S. Rasoulinezhad, H. Zhou, L. Wang, and P. H. Leong, “PIR-DSP: An FPGA DSP Block Architecture for Multi-precision Deep Neural Networks,” in *2019 IEEE 27th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, 2019.

[23] X. Zhang, A. Ramachandran, C. Zhuge, D. He, W. Zuo, Z. Cheng, K. Rupnow, and D. Chen, “Machine Learning on FPGAs to Face the IoT Revolution,” in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design*, 2017.

[24] A. Stojanov, T. M. Smith, D. Alistarh, and M. P¨uschel, “Fast Quantized S. Rasoulinezhad, H. Zhou, L. Wang, and P. H. Leong, “PIR-DSP: An FPGA DSP Block Architecture for Multi-precision Deep Neural Networks,” in *2019 IEEE 27th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, 2019.

[25] X. Zhang, A. Ramachandran, C. Zhuge, D. He, W. Zuo, Z. Cheng, K. Rupnow, and D. Chen, “Machine Learning on FPGAs to Face the IoT Revolution,” in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design*, 2017.

[26] A. Stojanov, T. M. Smith, D. Alistarh, and M. P¨uschel, “Fast Quantized S. Rasoulinezhad, H. Zhou, L. Wang, and P. H. Leong, “PIR-DSP: An FPGA DSP Block Architecture for Multi-precision Deep Neural Networks,” in *2019 IEEE 27th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, 2019.