mmWave Spatial-Temporal Single Harmonic Switching Transmitter Arrays for High back-off Beamforming Efficiency

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Abstract—This paper presents a spatial-temporal single harmonic switching (STHS) transmitter array architecture with enhanced efficiency in the power back-off (PBO) region. STHS is an electromagnetic and circuit co-designed and jointly optimized transmitter array that realizes beamforming and back-off power generation at the same time. The temporal dimension is originally added in STHS to achieve back-off efficiency enhancement, which can be combined with conventional power back-off enhancement methods such as Doherty amplifiers and envelope tracking. The design is validated through a simulation of a two-stage power amplifier in 65-nm CMOS at 77 GHz, which achieves a peak drain efficiency (DE) of 24.2%, a 22% DE at 3-dB PBO, 16% DE at 6-dB PBO and 10.2% at 9-dB PBO. The efficiency exhibits a 57% improvement at 3-dB PBO, 100% improvement at 6-dB PBO, and 190% improvement at 9-dB PBO compared with class A/B amplifier.

Index Terms—Time-modulated array, phased array, spatial-temporal modulation, power amplifiers, back-off efficiency, beamforming.

I. INTRODUCTION

Modern wireless communication system takes advantage of high-order modulation schemes to achieve high spectral efficiency by employing dense constellations. One major drawback of transmitting complex modulated signals is the high Peak-to-Average Power Ratio (PAPRs), which forces the transistors to operate in the linear region with a large input back-off. As an example, 4G communication uses signals with 7-8 dB power back-off (PBO) while in 5G and WLAN IEEE 802.11ax, the signal PBO can be larger than 9.5 dB [1], [2]. Power amplifiers (PAs) suffer from efficiency degradation when working in the PBO region. This raises challenges to wireless system engineers to design highly efficient systems for mobile usage [3], [4].

On the other hand, to get a larger data bandwidth, the carrier frequency will soon enter the mm-Wave band (30-300 GHz). Limited by the Friis transmission equation, the signal will attenuate with the increased signal carrier frequency. In the mm-Wave band, PAs will show even lower efficiency compared to their low-gigahertz counterparts due to inferior transistor performance at higher frequencies [4]. For example, the efficiency of a typical class-A/B power amplifier will degrade from about 60% at low-gigahertz to lower than 30% at mm-Wave band. Consequently, to increase the power of the transmitted signal, beamforming techniques are proposed, that is, to concentrate the signal transmitted to a certain direction so that the spatial efficiency can be significantly enhanced. Conventionally, a decoupled approach is applied in designing a wireless system where the beamforming and power back-off is realized by a phased array with phase shifters and a power-generating circuit, respectively. As shown in Fig. 1, phase shifters with two quadrature paths are implemented in a typical phased array to realize the desired phase shift. On the other hand, a power amplifier is used for controlling the power generation while an efficiency enhancement structure can be used to mitigate PA’s efficiency degradation in the back-off region. However, the system efficiency is unsatisfactory because phase shifters introduce extra power loss while power amplifiers’ efficiency degrades quickly in the PBO region. In this work, an electromagnetic and circuit co-designed transmitter array that includes time as an additional degree of freedom is proposed for back-off efficiency enhancement. To introduce the EM-circuit co-designed approach used in this work, antenna array beamforming efficiency and power amplifier back-off efficiency in the conventional approach are first discussed in the following subsections.

A. Beamforming Efficiency in an Antenna Array

Although phased array offers an additional array gain, it requires complex weight multiplications in different signal paths and, consequently, the beamforming efficiency degrades due to poor matching while the system complexity of a phased array is also unappreciated for small-size mobile usage. To realize beamforming without phase shifters, the concept of time-modulated array (TMA) exploiting time-domain signal processing techniques is proposed [5], [7]. One challenge faced by TMA design is the presence of undesired harmonics induced by the periodic time modulation, which results in a harmonic efficiency reduction [8]. To suppress the sideband level (SBL) while synthesizing desired patterns, different optimization algorithms

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are proposed, such as genetic algorithms [9], simulating annealing [10], particle swarm optimization [11], and differential evolution [12]. An abundance of works can be found in the literature where different applications of the time-modulated array are proposed. Li et al. studied TMA from the view of array factors to realize adaptive beamforming [13] and direction finding [14]. Masotti et al. took advantage of TMA’s real-time beamforming features in the application of wireless power transfer [15]. Also, a system-level design is further proposed by Yao et al. that TMA could be applied together with I/Q modulation to generate a scanning beam at a single positive sideband while suppressing other harmonics [16].

B. Back-off Efficiency for Power Amplifiers

After introducing the beamforming efficiency in antenna arrays, the back-off efficiency for power amplifiers is discussed in this subsection. Multiple techniques have been proposed to enhance the efficiency of PAs while transmitting high PAPR signals including envelope-tracking architecture, Doherty, and outphasing. The essence of those methods is to preserve the operating conditions of power amplifiers in their high-efficiency conditions including bias voltages and impedances and to reduce DC power consumption when operating in the back-off region. The relative pros and cons among those circuit-level back-off efficiency enhancement architectures are summarized in Table I.

Envelope-tracking PA controls the supply voltage of the PA according to the envelope of the transmitted signal to optimize the efficiency of PAs [17], [18]. In this case, systems bandwidth is traded for higher efficiency. The Doherty PA is another popular structure that takes advantage of the load-pull realized by the main PA and the auxiliary PA [19], [20]. When power is delivered at back-off, the auxiliary PA will be turned off, and for increased signal power, the load-pull techniques retain the impedance seen by the main PA at its optimal value. However, the necessity of complex output matching inevitably introduces a loss penalty of about 1.7 dB in a 2 GHz range and this matching loss will increase as the carrier frequency increases. A typical Doherty PA implemented operating at 77 GHz in a 40-nm CMOS process exploits a drain efficiency enhancement of 50% at 3-dB PBO, 100% at 6-dB PBO compared with a typical class-A/B [21]. Outphasing PA uses two PAs driven by signals with different phases so that the system could deliver the desired output power [22]–[24]. Whereas, it has a limited output power dynamic range.

Subharmonic switching is an alternative technique that utilizes the lower magnitude of high-frequency harmonics of the modulation pulses of a class-D power amplifier [25]. The power back-off is realized by lowering the switching frequency of a class-D digital PA to utilize subharmonics of the output signals. Yet, since the relative magnitude of subharmonics is fixed, PA branches need to be used to achieve different power back-off regions, which results in higher system complexity. Also, digital PAs used in subharmonic switching will fail in high-frequency operations due to the low quality factor of the output filtering network.

C. EM-circuit Co-design

As illustrated in Fig. 1 since the decoupled design is used in a conventional phased array, power amplifiers and phase shifters are optimized separately before they are combined. In this work, an electromagnetic and circuit co-designed transmitter array is proposed that realizes spatial beamforming and power back-off efficiency enhancement.
TABLE I
Comparison between circuit-level back-off efficiency enhancement architectures

| Architecture          | Pros                                      | Cons                                      |
|-----------------------|-------------------------------------------|-------------------------------------------|
| Envelope-tracking [17]| Optimal efficiency at the deep PBO regions.| High bandwidth supply needed.             |
|                       |                                           | Accurate envelope signals required.       |
| Doherty [19]          | Relatively high efficiency.               | Complex output matching networks.         |
| Outphasing [24]       | Low system complexity.                    | Low bandwidth.                            |
|                       |                                           | Limited dynamic power range.              |
| Subharmonic switching [25] | High deep PBO efficiency.           | PA branches needed.                        |
|                       |                                           | Low-frequency application only.            |

Fig. 2. A time-modulated PA cell in (a) the peakmode, (b) the pbomode. The first harmonic at $f_c + f_p$ is utilized to deliver signals while the power back-off can be achieved by decreasing the duty cycle of the modulating pulses. However, the harmonic efficiency degenerates significantly because of the existence of other harmonics induced by the modulating pulses.

by exploiting the synergy between circuits and the array. Since this system makes use of the first harmonic signal of the temporal switching pulse, we refer to it as spatial-temporal single harmonic switching (STHS) transmitter array in the following discussion.

It is first noted that the duty cycle of time-domain pulse modulation is viable to control the output signal power. In the ideal case, the PA switches ON and OFF according to the modulating pulses, which is similar to the operation of a class-D power amplifier, leading to an improved efficiency. This shows the potential to achieve beamforming and enhance power back-off efficiency at the same time by combining an antenna array with controllable pulse modulation. However, the energy will be wasted on undesired harmonics induced by the pulse modulation. To deal with this power loss, a carefully designed time-modulated phased array switching sequence is used to improve array beamforming efficiency for both the peakmode and the power back-off mode. By the adoption of the time domain pulse modulation signal in an antenna array, the power on undesired harmonics will be suppressed spatially resulting in a system-level back-off efficiency enhancement. It is also important to notice that, since the STHS optimizes the array factor in the spatial and the temporal domain, additional system efficiency could be further achieved by combining STHS with existing circuit level optimization methods such as the Doherty PA.

The remainder of this paper is organized as follows. The co-design considerations for the proposed STHS array are presented in Section II where the system theoretical model is derived. Section III presents the simulated characteristics for the STHS array. Finally, the conclusion is drawn in Section VI.

II. Co-Design and Optimization

A. Proposed Spatial-Temporal Single Harmonic Switching (STHS) Array

Generally speaking, the PA output impedance is optimized for maximal power efficiency at the peakmode. When the PA goes into the back-off region, the efficiency will degrade since the output power decreases while the DC power remains nearly the same. One way to improve the back-off efficiency is to let the PA either work in the peakmode or be turned off. This concept is illustrated in Fig. 2 where a power amplifier is connected to a voltage-controlled current source modulated by the switching pulse sequence controlling the power generation. Ideally, the PA will work with maximum efficiency when the pulse is high and will be turned off when the pulse is low. The maximum output power is generated when the time-modulated PA cell works in peakmode while the back-off power is delivered in pbomode by decreasing the duty cycle of the modulating pulse. The time domain multiplication between the transmit signal and modulating pulse will
result in a frequency domain convolution, and therefore, the frequency spectrum of the output signal will consist of all the odd harmonics. Although each harmonic could be utilized to deliver the output signal theoretically, the bandwidth is often restricted in the modern communication systems to avoid the cross-talk between channels. In this work, we utilize the first harmonic to deliver signals since it possesses more power as compared with other harmonics. To show how the back-off power is delivered by the modulating pulse, the first harmonic at $f_c + f_p$ is considered where $f_c$ denotes the carrier frequency and $f_p$ denotes the modulating pulse frequency. The $f_c$ and $f_p$ should satisfy $f_c \gg f_p$ and $f_p > 2f_{IF}$ where $f_{IF}$ denotes the intermediate frequency to avoid aliasing. Since the duty cycle determines the duration for the power amplifier to be turned on, it is seen that a decrease in the duty cycle of the modulating pulse signal will reduce the output magnitude of the first harmonic at $f_c + f_p$.

The overall efficiency of the co-designed transmitter array is determined by both the harmonic efficiency $\zeta_{harm}$ of the time-modulated array and the drain efficiency of the circuit $\zeta_{circ}$. Hence, the transmitter array drain efficiency (DE) $\eta$ could be expressed as

$$\eta = \zeta_{harm} \times \zeta_{circ}. \quad (1)$$

If we denote $P_{(m)}$ as the power of the $m^{th}$ harmonic where $m \in \mathbb{Z}$, the array harmonic efficiency $\zeta_{harm}$ being the ratio between the power of the desired first harmonic ($f_c + f_p$), and the total power radiated $P_{tot}$ can be written as

$$\zeta_{harm} = \frac{P_{(1)}}{P_{(tot)}}. \quad (2)$$

In Fig. 4 it is seen that the undesired harmonics ($f_c + 3f_p$, $f_c - f_p$, etc.) will lead to an efficiency degradation. To improve the harmonic efficiency, a properly designed time-modulated pulse eliminating undesired harmonics will be implemented and discussed.

In terms of the circuit efficiency $\zeta_{circ}$, two non-idealities need to be dealt with that degrades the back-off efficiency:

1) When the PA cell is in the "OFF" state, the existence of sub-threshold leakage power degrades the efficiency.

2) During each switching period, there exist dynamic power losses resulting from the charging and discharging process of the parasitic capacitance.

To optimize the circuit efficiency, the efficiency model for the power loss is established and circuit parameters like the size of transistors are optimized to balance the trade-off between switching performance and efficiency degradation.

### B. Harmonic Efficiency Optimization through STHS

In this subsection, the configuration of a 4-path STHS array shown in Fig. 3 is discussed to improve array harmonic efficiency and to realize beamforming. The STHS array utilizes the differential RF signal pair ($RF^+$ and $RF^-$) generated by a double-balanced mixer to realize a pulse modulation with different polarities. Each transmitter is composed of four signal paths with 90° phase differences generated by a quadrature hybrid. Each signal path consists of a time-modulated PA cell to realize independent pulse modulation. The output signal after modulation is recombined and delivered to each antenna element.

As discussed before, the switching waveform contains different harmonics while only the first harmonic will be used in this design for spectral-efficient beamforming.
Therefore, higher efficiency can be achieved by carefully designing the time-modulated pulses such that the first positive harmonic frequency is enhanced while the other harmonics are suppressed. According to [10], multiple modulating pulses can be designed such that a combination of signals modulated by those pulses will lead to suppression of undesired harmonics. The modulation pulses for each path are illustrated in Fig. 3. If we assume that all the elements are isotropic and equally spaced, the array factor can be written as

$$
AF(\theta, t) = e^{j2\pi f_0 t} \sum_{n=1}^{N} I_n \cdot \left[ U_0^n(t) + U_n^\neq(t) + U_n^\pi(t) + U_n^\neq(t) \right] \cdot e^{j\beta(n-1)d\sin\theta} 
$$

(3)

where $f_0$ is the carrier frequency, $T_p$ is the time-modulated pulse period assuming that $f_0 \gg f_p$ ($f_p = 1/T_p$). $\beta = 2\pi/\lambda$ is the free-space wave number, $\lambda = c/f_0$ is the wavelength, and $c$ is the speed of light in vacuum. $I_0$ is the amplitude excitation of the $n^{th}$ element. $\theta$ is the angle observed from the broadside direction, and $d$ denotes the interelement distance. $U_0^n(t), U_n^\neq(t), U_n^\pi(t), U_n^\neq(t)$ are the modulating pulses on signal paths with different phases used to modulate the $n^{th}$ array element. To study the signal in the frequency domain, the pulse functions are expressed through Fourier series with different frequency components

$$
U_0^n(t) = \sum_{m=-\infty}^{+\infty} a_{mn}^0 \cdot e^{2j\pi m f_p t}, \quad m \in \mathbb{Z}
$$

$$
U_n^\neq(t) = \sum_{m=-\infty}^{+\infty} a_{mn}^\neq \cdot e^{2j\pi m f_p t}, \quad m \in \mathbb{Z}
$$

$$
U_n^\pi(t) = \sum_{m=-\infty}^{+\infty} a_{mn}^\pi \cdot e^{2j\pi m f_p t}, \quad m \in \mathbb{Z}
$$

$$
U_n^\neq(t) = \sum_{m=-\infty}^{+\infty} a_{mn}^\neq \cdot e^{2j\pi m f_p t}, \quad m \in \mathbb{Z}
$$

(4)

where $\mathbb{Z}$ is the set of all integers.

Then the array factor becomes

$$
AF(\theta, t) = \sum_{m=-\infty}^{+\infty} e^{2j\pi(f_0 + m f_p)t} \sum_{n=1}^{N} I_n \cdot \left( a_{mn}^0 + a_{mn}^\neq + a_{mn}^\pi + a_{mn}^\neq \right) \cdot e^{j\beta(n-1)d\sin\theta}.
$$

(5)

In the following calculation, given the pulse frequency $f_p$, parameters to be designed include: the duration of each modulating pulse $\tau$ and the switch-ON time of positive and negative pulses for each path, i.e., $t_1, t_2$ for $U_0^n, t_3, t_4$ for $U_n^\neq, s_1, s_2$ for $U_n^\pi$, and $s_3, s_4$ for $U_n^\neq$.

To completely suppress the carrier component, the modulation pulses should have a mean of 0. This means that the duration of $RF^+$ and $RF^-$ should be equal so that the Fourier coefficients for the carrier component will be zero, i.e.,

$$
a_{mn}^0 = a_{mn}^\neq = a_{mn}^\pi = a_{mn}^\neq = 0.
$$

(6)

For $m \neq 0$, the Fourier coefficient for $U_0^n$ can be expressed as

$$
a_{mn}^0 = \frac{1}{T_p} \int_{0}^{T_p} U_0^n(t)e^{-j2\pi m f_p t}dt = \frac{2}{m\pi} \sin \left( \frac{m\pi}{\tau} \right) \sin \left( \frac{m\pi t_2 - t_1}{T_p} \right) e^{-jm\pi \frac{t_2 + t_1}{T_p}} e^{j\frac{\pi t_1}{2}}.
$$

(7)

A similar calculation can be applied to the rest three paths $(a_{mn}^\neq, a_{mn}^\pi, a_{mn}^\neq)$. Then the array factor is written as

$$
AF_m(\theta, t) = e^{j2\pi(f_0 + m f_p)t} \sum_{n=1}^{N} I_n A_{mn} e^{j\beta(n-1)d\sin\theta}.
$$

(8)

According to Parseval’s theorem, the total power from the $m^{th}$ harmonic $P_m$ is given by

$$
P_m = \sum_{n=1}^{N} \sum_{s=1}^{N} \{ I_n I_s \cdot \sin[\beta d(n-s)] \cdot A_{mn} A_{ms}^\ast \},
$$

(11)

which indicates that $A_{mn}$ can be designed to optimize harmonic efficiency by enhancing the power delivered through the first positive harmonic. In the following calculation, harmonics with $m \in \{2k, 3k, 4k-1, \ldots \} \in \mathbb{Z}$ are designed to be eliminated.

To eliminate even harmonics, the coefficients should satisfy

$$
\begin{align*}
\frac{t_{2n} - t_{1n}}{T_p} &= \frac{t_{2n} - t_{1n}}{T_p} = \frac{1}{2}, \\
\frac{s_{2n} - s_{1n}}{T_p} &= \frac{s_{2n} - s_{1n}}{T_p} = \frac{1}{2}.
\end{align*}
$$

(12)

Then $A_{mn}$ can be reformed into:

$$
A_{mn} = \frac{2}{m\pi} \sin \left( \frac{m\pi \tau}{T_p} \right) \sin \left( \frac{m\pi}{T_p} \right) \text{sgn}(m)
$$

$$
\left[ e^{-jm\pi \frac{2t_{1n} + t_{2n}}{T_p}} e^{j\pi \frac{t_{1n}}{2}} + e^{-jm\pi \frac{2t_{1n} + t_{2n}}{T_p}} e^{j\pi \frac{t_{2n}}{2}} \right]
$$

$$
\left[ e^{-jm\pi \frac{2t_{1n} + t_{2n}}{T_p}} e^{j\pi \frac{t_{1n} - t_{2n}}{2}} + e^{-jm\pi \frac{2t_{1n} + t_{2n}}{T_p}} e^{j\pi \frac{t_{2n} - t_{1n}}{2}} \right]
$$

(13)

where $\text{sgn}(m)$ denotes the sign of parameter $m$. It is seen that all even harmonics are eliminated, i.e.,

$$|A_{mn}| = 0, \quad \{ m = 2k, \quad k \in \mathbb{Z} \}
$$

(14)

Similarly, the pulse duration can be set as

$$
\frac{\tau_0}{T_p} = \frac{1}{3}
$$

(15)
to suppress all \( m^{th} \) harmonics with \( m = 3k, \ k \in \mathbb{Z} \), i.e.,
\[
|A_{mn}| = 0, \quad \{m = 3k, \quad k \in \mathbb{Z}\}. \tag{16}
\]

To eliminate harmonics with \( m = 4k - 1 \) with \( k \in \mathbb{Z} \), \( t'_{1n} \) and \( s'_{1n} \) should satisfy
\[
\begin{align*}
t'_{1n} & = \frac{t_{1n}}{T_p} \cdot \frac{1}{4}, \\
s'_{1n} & = \frac{s_{1n}}{T_p} \cdot \frac{1}{4}.
\end{align*}
\tag{17}
\]

Then (13) could be rewritten as
\[
A_{mn} = \frac{4}{m\pi} \sin \left( m\pi \frac{T_p}{T} \right) \sin \left( \frac{m\pi}{2} \right) \text{sgn}(m) \cdot 
\left[ e^{-jm\pi \frac{2\text{tharm} + \pi}{T_p}} e^{j\pi \frac{1-m}{2}} + e^{-jm\pi \frac{2\text{tharm} + \pi}{T_p}} e^{j\pi \frac{1-m}{2}} \right].
\tag{18}
\]

When the STHS array is implemented in the \( PBO \) region, the output power is reduced by shortening the duration of the pulses. The relative pulse duration for the STHS working in the \( PBO \) region is denoted by the duty cycle ratio \( \alpha \) where
\[
\tau = \alpha \tau_0 = \frac{T_p}{3}, \quad \alpha \in [0, 1]. \tag{19}
\]

Ideally, a duty cycle ratio of \( 10\log(\alpha) = -p \) corresponds to a power back-off of \( p \)-dB. While the duty cycle \( \tau \) is designed to eliminate harmonics of \( m = 3k \) for \( k \in \mathbb{Z} \), a change in the duty cycle in the \( PBO \) region will result in a decrease of harmonic efficiency \( \zeta_{\text{harm}} \). To eliminate those harmonics, a systematic method is proposed for harmonic elimination in the back-off region. Generally, to make \( |A_{mn}| = 0 \) for a specific \( m^{th} \) harmonic, according to (18), \( t_{1n} \) and \( s_{1n} \) should satisfy
\[
e^{-jm\pi \frac{2\text{tharm} + \pi}{T_p}} e^{j\pi \frac{1-m}{2}} + e^{-jm\pi \frac{2\text{tharm} + \pi}{T_p}} e^{j\pi \frac{1-m}{2}} = 0, \tag{20}
\]
which means there exists a \( k \) belongs to \( \mathbb{Z} \), such that
\[
-m \left( \frac{2t_{1n}}{T_p} + \frac{\alpha}{3} \right) + \frac{1-m}{2} = -m \left( \frac{2s_{1n}}{T_p} + \frac{\alpha}{3} \right) + \frac{1-m}{2} + 2k + 1.
\tag{21}
\]

To simplify, if we let \( k' = -k \), (21) yields
\[
t_{1n} = \frac{s_{1n}}{T_p} + \frac{k'}{|m|}. \tag{22}
\]

To optimize the harmonic efficiency in the power back-off region, since the power on each harmonic are related to the magnitude of the corresponding Fourier coefficients, \( P_{-3} \) is of our major consideration as it contains the highest unsuppressed harmonic power. Therefore, to ensure \( |A_{-3n}| = 0 \), the relationship between \( t_{1n} \) and \( s_{1n} \) should satisfy
\[
s_{1n} = \frac{t_{1n}}{T_p} - \frac{1}{3}.
\tag{23}
\]

By substituting (23) into (18), the \( A_{mn} \) now becomes
\[
A_{mn} = \frac{4}{m\pi} \sin \left( m\pi \frac{T_p}{T} \right) \sin \left( \frac{m\pi}{2} \right) \text{sgn}(m) \cdot 
\left[ e^{-jm\pi \frac{2\text{tharm} + \pi}{T_p}} e^{j\pi \frac{1-m}{2}} + e^{-jm\pi \frac{2\text{tharm} + \pi}{T_p}} e^{j\pi \frac{1-m}{2}} \right].
\tag{24}
\]

For an STHS array to achieve beam-forming in the first harmonic, \( A_{1n} \) in the peakmode is considered
\[
A_{1n} = \frac{4}{\pi} \sqrt{3} e^{-j\pi \frac{2\text{tharm} + \pi}{T_p}} \cdot (1 + e^{-j\pi \frac{1-m}{2}}).
\tag{25}
\]

Therefore, the array factor of the first harmonic is
\[
AF_1(\theta) = \sum_{n=1}^{N} I_n \frac{4}{\pi} \sqrt{3} e^{-j\pi \frac{2\text{tharm} + \pi}{T_p}} \cdot (1 + e^{-j\pi \frac{1-m}{2}}) e^{j\beta(n-1)d \sin \theta},
\tag{26}
\]

To ensure the power of the first harmonic at given direction
\( \theta \) is maximized, \( t_{1n} \) for each antenna element should satisfy
\[
\frac{t_{1n}}{T_p} = \frac{1}{2} \left[ \frac{(n - 1)/\beta \sin \theta}{\pi} - \frac{1}{2} \right].
\] (27)

The conceptual illustrations of the STHS transmitter array operating in the peakmode and the PBO mode are shown in Fig. 5. Compared with the pulse modulation back-off technique in Fig. 2, it could be seen that all \( m^{th} \) harmonics for \( m \in \{2k, 3k, 4k - 1, \ k \in \mathbb{Z}\} \) are suppressed, and therefore, the array harmonic efficiency is improved. Moreover, in the power back-off region, the undesired \( m = -3 \) harmonic is suppressed leading to an improved back-off harmonic efficiency.

In order to demonstrate the efficiency enhancement of the STHS back-off technique, a simulation is performed in Matlab by choosing a carrier frequency \( f_0 = 77 \) GHz, and a pulse frequency \( f_p = 1 \) GHz. In this simulation, 5 antenna elements are used and the spacing between each antenna is set to be half wavelength (1.95 mm). The mutual coupling between antennas is neglected. The first harmonic \( (m = 1) \) targeted at \( \theta = 20^\circ \) is simulated to demonstrate the change of harmonic power in the peakmode and the PBO mode with a duty cycle ratio of \( 10\log(\alpha) = -6 \), which ideally corresponds to a 6-dB PBO. The radiation patterns of the first harmonic \( (m = 1) \) are shown together with the normalized relative power patterns at other harmonics \( m = \{-3, 5, -7\} \) in Figs. 6 and 7. It is seen that the beamforming without phase shifters is achieved with the first harmonic targeted at \( \theta = 20^\circ \), and due to the harmonic-suppression algorithm deduced in (23), the \( m = -3 \) harmonic is suppressed in both the peakmode and the PBO region, otherwise it will consume much power indicated by the Fourier coefficients.

C. Circuit Efficiency Modeling and Optimization

In the previous subsection, we focused on the array factor and optimize the harmonic efficiency using the pulse modulation technique. In this subsection, the performance of the STHS transmitter array is optimized in the circuit
perspective. As shown in Fig. 5 (a), the time-modulated PA structure consists of a classical common source amplifier with its source connected to another transistor that serves as a voltage-controlled current source. The upper NMOS is biased as a typical class-A/B amplifier and the lower NMOS is used as a switching device. During the 'ON' state, the source of the upper NMOS is connected directly to the GND and it will function as an ordinary class-A/B amplifier. During the 'OFF' state, the output will remain at VDD since the upper NMOS is floating. By switching between the 'ON' and the 'OFF' state at a rate faster than the data bandwidth, this structure is able to realize the pulse modulation of a given RF signal. Compared with the existing structure involving SPST switches along with the signal path, this stacking time-modulated PA structure reduces the insertion loss when the switch is 'ON' and allows smaller power leakage when the switch is 'OFF'.

1) Time-modulated PA Cell Switching performance: In terms of the circuit switching performance, the maximum output power when the switch is at the 'ON' stage \( P_{ON,max} \) and the 'OFF' stage \( P_{OFF,max} \) is examined. A smaller switching unit reduces the \( P_{ON,max} \) because the maximum current the current source can provided is small and the gain of the amplifier is therefore limited. For switching units with a large transistor size, there will be more leakage power during the 'OFF' stage, and \( P_{OFF,max} \) will be larger. Therefore, there exists a design trade-off between the output power and power leakage for the time-modulated PA. In STHS transmitter array design, the size ratio between the switching and the amplifying unit is designed to optimized the switching power ratio (SPR) i.e.,

\[
SPR = \frac{P_{ON,max}}{P_{OFF,max}}. 
\]  

(28)

The simulation result for SPR under different transistor width ratios between the bottom switching NMOS and the top amplifying NMOS is shown in Fig. 9, showing that the maximum SPR can be reached for a transistor width ratio of 6.

Moreover, a 2-stage cascaded power amplifying chain is used to further improve the SPR. The simulated transient response at the output stage is shown in Fig. 10. The SPR increases from 8.7 for an individual time-modulated power amplifier to 809 for a 2-stage cascaded time-modulated power amplifier. This 92 times improvement is because a 2-stage cascaded time-modulated power amplifier will amplify the \( P_{ON,max} \) twice while blocking the \( P_{OFF,max} \) twice.

2) Time-modulated PA Cell Efficiency Model: While the theoretical value for \( \zeta_{harm} \) can be reached by combining (10) and (11) given in the previous section, the remaining \( \zeta_{circ} \) part will be analyzed in the following according to the power and efficiency model of a single time-modulated PA cell established (Fig. 8). Three mechanisms are analyzed separately:

1) 'ON' Stage Efficiency: When the STHS PA cell is at the 'ON' stage, the drain-source voltage \( v_{DS} \) and drain current \( i_D \) can be written as

\[
\begin{align*}
i_D &= I_{DD} - \frac{v_{pk}}{R_L} \cos(2\pi f_c t), \\
v_{DS} &= V_{DD} + v_{pk} \cos(2\pi f_c t)
\end{align*}
\]  

(29)

where \( V_{DD} \) is the system voltage, \( I_{DD} \) is the bias current, and \( v_{pk} \) is the peak voltage of the load. The output power during the 'ON' stage can be expressed as

\[
P_{out,ON} = \frac{v_{pk}^2}{2R_L}. 
\]  

(30)

The power delivered from the DC source during the 'ON' stage is

\[
P_{DC,ON} = V_{DD}I_{DD}. 
\]  

(31)

2) 'OFF' Stage Power Leakage: When STHS PA cell is
We denote $P_{out,ON}$ the output power during the "ON" stage, $P_{DC,ON}$ the power delivered from the DC source during the "ON" stage, $P_{leak}$ the power leakage during the "OFF" stage, and $P_{dyn}$ the dynamic power loss resulting from each switching.

We denote $P_{out,OFF}$ the output power during the "OFF" stage, i.e.,

$$P_{out,OFF} = 0. \quad (32)$$

In this stage, the DC power comes from the leakage current of the switching NMOS. To model subthreshold leakage current in the switching unit, an equivalent switching resistor $R_{sw}$ is used. Then the DC power during the "OFF" stage is

$$P_{DC,OFF} = P_{leak} = \frac{V_{DD}^2}{R_{sw}}. \quad (33)$$

3) Dynamic Switching Loss: The dynamic power should be considered to model the power consumption for each switching period. During the "OFF" stage, since the lower NMOS is in the cutoff region, the source voltage of the upper NMOS ($V_X$) will be equal to the output bias drain voltage, i.e.,

$$V_{X,OFF} = V_{DD}. \quad (34)$$

During the "ON" stage, the lower NMOS will be turned on with $V_X$ shorted to the ground and therefore,

$$V_{X,ON} = 0. \quad (35)$$

To model the power loss resulting from this ON-OFF stage voltage difference, a switching capacitor $C_{sw}$ is used. For each rectangular pulse, the switching capacitor will go through a period of charging and discharging, leading to a dynamic power loss. In terms of the STHS array, there exist two pulses in one modulation period when the STHS technique is adopted. Consequently, the dynamic power can be expressed as

$$P_{dyn} = f_p V_{DD}^2 C_{sw}. \quad (36)$$

Hence, for an STHS PA in the PBO region with a duty cycle of $2\tau/T_p$, the overall drain efficiency of the circuit is

$$\zeta_{circ} = \frac{\frac{2\pi}{T_p} P_{out}}{\frac{2\pi}{T_p} P_{DC} + (1 - \frac{2\pi}{T_p}) P_{leak} + P_{dyn}} \quad (37)$$

$$= \frac{\frac{2\pi}{T_p} V_{DD}^2 I_{DD} + (1 - \frac{2\pi}{T_p}) V_{DD}^2 I_{sw} + f_p V_{DD}^2 C_{sw}}{\frac{2\pi}{T_p} V_{DD}^2 I_{DD} + (1 - \frac{2\pi}{T_p}) V_{DD}^2 I_{sw} + f_p V_{DD}^2 C_{sw}}.$$

This indicates that both an increase of pulse modulation frequency $f_p$ and a decrease of pulse duty cycle $\tau$ degrade the circuit efficiency. Intuitively, faster modulation frequency will lead to an increase in dynamic power and a smaller pulse duty cycle will result in more leakage power.

According to the simulation, the model parameter is set to be $C_{sw}/W \approx 0.35 \, \text{nF/m}$ and $R_{sw}-W \approx 5.4 \, \Omega \cdot \text{m}$, where $W$ is the width of the transistor. Figs. ??, ?? and ?? show the distribution of the power with different modulation frequencies and operation regions. It can be seen that at
peak power mode with modulation pulse frequency at 1
GHz, the dynamic power and leak power counts for 5%
and <1% of the total power consumption, respectively.
As predicted by our model, when the circuit goes into
the PBO region, the simulation at a duty cycle ratio
of $10\log(\alpha) = -6$ (i.e., $\tau \approx 0.25 \times \frac{T_p}{4}$) shows that both leak
dynamic power and leak power begin to increase causing
degeneration of circuit efficiency. Additionally, if the circuit
runs at 2 GHz with a duty cycle ratio of $10\log(\alpha) = -6$,
the dynamic power and leak power counts for 28% and 2%,
respectively, which suggests that a doubling of switching
frequency causes the dynamic power loss to increase by
64% while the leak power remains nearly the same.

D. Further Optimization for STHS harmonic efficiency

According to the array harmonic elimination technique
for $m = -3$ harmonic discussed in (20), (21), and (22), it
is seen that a further improvement in harmonic efficiency
could be achieved by adding four additional paths with
phases $45^\circ$, $135^\circ$, $225^\circ$, and $315^\circ$ to eliminate
$m = 5$ harmonic.

For the implementation where the pulse switch-ON time
for the $45^\circ$ path of $n$th is $r_{1n}$, to eliminate $m = 5$ harmonic,
according to (24), the requirement for $r_{1n}$ is
\[
\left[e^{j\pi \frac{1 - m}{2}} + e^{j\pi (\frac{1 - m}{2} + 2k + 1)}\right] \times
\left[e^{-jm\frac{2\pi r_{1n} + \tau}{T_p}} + e^{-jm\frac{2\pi r_{1n} + \tau - 1}{T_p}}\right] = 0.
\]
\tag{38}

Then the relation between $t_{1n}$ and $r_{1n}$ can be derived as
\[
-m\frac{2t_{1n} + \tau}{T_p} = -m\frac{2r_{1n} + \tau - 1}{4} + 2k + 1, \quad (k \in \mathbb{Z}).
\tag{39}

Take $m = 5$ and $k = 0$, we arrive at
\[
r_{1n} = t_{1n} + \frac{3}{40}.
\tag{40}

A similar simulation is performed with a carrier fre-

quency of $f_0 = 77$ GHz, a pulse frequency of $f_p = 1$ GHz
with 5 antenna elements spaced at half wavelength (1.95 mm). The result is shown in Figs. 16 and 17. Compared with Figs. 6 and 7, it can be seen that both \( m = -3 \) and \( m = 5 \) harmonics are eliminated in the peakmode results in harmonic efficiency improvement from 89.7% to 95.3% in the peakmode and 47.8% to 82.7% in the PBO mode with duty cycle ratio \( 10 \log(\alpha) = -6 \).

### III. Circuit Simulation

#### A. Simulation Setup

In this section, circuit simulation is performed to validate the effectiveness of the STHS array. A 65-nm NMOS process is used in the simulation. The circuit structure of one transmitter path is shown in Fig. 15(a). Design challenges and considerations of major blocks are discussed in this section. The DC voltage is set to be 1.2 V, and the bias base voltage is set to be 0.7 V for a class-A/B operation. The carrier frequency is \( f_0 = 77 \) GHz, and the pulse frequency \( f_p \) is chosen to be 1 GHz. The spacing between each antenna is set to be half wavelength (1.95 mm).

To optimize the tradeoffs between PA maximum output power and efficiency, we design the L-type matching networks according to the load-pull simulation results shown in Figs. 15(b) and 15(c), and the matching network output load impedance for M1 and M2 is designed to be \( 18 + 33 j \) and \( 14 + 15 j \), respectively.

#### B. STHS Array Beamforming Result

The spatial beamforming result with the first harmonic targeted at \( \theta = 20^\circ \) is simulated. The circuit-generated
radiation patterns for STHS array with different duty cycle ratio $\alpha$ are shown in Figs. 16, 17. It is seen that at 6-dB PBO, the $m = -3$ harmonic is suppressed similar to the ideal Matlab simulation. The simulated harmonic efficiency $\zeta_{harm}$ at different power back-off regions are compared with the ideal values in Fig. 18. It is seen that the harmonic efficiency is kept above 80% beyond the 3-dB PBO due to the elimination of $m = -3$ harmonic. In the deep power back-off region, the relative power of other undesired harmonics will increase, which degrades the harmonic efficiency. The simulated harmonic efficiency shows an approximately 5% lower harmonic efficiency compared to the ideal value which can be attributed to the nonidealities of the time-modulated PA such as the switching overshoot, leakage power, etc.

C. STHS Array Back-off Result

Fig. 19 shows how the output power of the desired first harmonic can be controlled by the duty cycle ratio of the modulation pulse $\alpha$. Since the power of the first harmonic also depends on the harmonic efficiency, the slope of the output power is steeper for $10\log(\alpha) < -3$ region where the harmonic efficiency begins to degrade quicker.

The illustration of amplitude and phase for a 16 QAM is shown in Fig. 20. The STHS array works in the peakmode with a duty cycle ratio $10\log(\alpha) = 0$ to generate symbol 1 $(3 + 3j)$. As for symbol 3 $(1 + 1j)$, the IF signal will remain the same as the signal for symbol 1 while the duty cycle ratio for the modulating pulses is adjusted to be $10\log(\alpha) = -4.8$. To generate symbol 4 $(-1 + 1j)$, the I channel changes its polarity from positive to negative while the Q channel and the duty cycle ratio remain the same as the signal for symbol 3. Furthermore, since the power comes in the RF power amplifier should remain the
maximum power for all signals transmitted to achieve high efficiency, to generate the symbol 2 \((3+1j)\), the signal for I channel and Q channel is designed such that a combination of I/Q channel will result in the maximum power for power amplifier and the angle on the constellation should be \(arctan\left(\frac{1}{3}\right)\) as required. The simulated output constellation of the STHS array for raw signals and pre-distorted signals are both shown in Fig. 21. Since the output power on the first harmonic is affected by both harmonic efficiency and circuit efficiency of the STHS array, the amplitude of the generated signal will be distorted if the efficiency degeneration of circuit and array is not taken into consideration when choosing the duty cycle ratio to deliver back-off signal. To have better control of the amplitude of output signal power, the duty cycle ratio should be bigger than the ideal case if the back-off signal is delivered. After modification, an improvement in output power control is observed.

The maximum PA output power and the peak drain efficiency are simulated by sweeping the frequency of the input signal (Fig. 22). The continuous wave (CW) large-signal characteristics of the STHS transmitter array are simulated and plotted in Fig. 23. The peak STHS array DE is 24.2% while a typical class-A/B PA has a drain efficiency of 29.6%. This is contributed by both the efficiency loss of the switching circuit and the existence of higher harmonics. The drain efficiency of the STHS transmitter array is 22% at 3-dB power back-off. This back-off efficiency is 57% larger than a class-A/B amplifier with the same peak drain efficiency. The array has a DE of 16% at 6-dB PBO, showing a 100% improvement compared to a class-A/B. The DE of the STHS array is as high as 10.2% at 9-dB power back-off. This back-off efficiency exhibits a 190% improvement compared to a class-A/B amplifier. The STHS array is also compared with a Doherty PA with normalized drain efficiency. It is seen that the STHS behaves better than the Doherty PA in the deep PBO region of >5-dB. Compared with a Doherty PA, the STHS array DE shows a 12% efficiency enhancement at 7-dB PBO, and a 33% enhancement at 9-dB PBO. Moreover, at the deep PBO region of 13-dB PBO, the array has a DE of 5.9%, showing a 96% improvement compared with a Doherty PA.

It is worth mentioning that if the size of the footprint is not the major design constraint, the 8-path STHS array structure can be utilized to realize a further back-off efficiency enhancement. At 6-dB PBO, an 8-path STHS array achieves a DE of 20% which shows a 35% improvement compared with a Doherty PA and a 170% improvement compared with a class-A/B. At 10-dB PBO, an 8-path STHS array achieves a DE of 12%. This DE has a 99% improvement compared with a Doherty PA and a 290% enhancement compared with a class-A/B.

IV. Conclusion

In this paper, we presented an EM-circuit co-designed and jointly optimized mm-wave transmitter array for back-off efficiency enhancement.

We proposed a 4-path STHS array where the duty cycle of the modulating pulses is utilized to control power generation while other pulse parameters are designed to suppress undesired harmonics in the power back-off region. The 8-path STHS array is also designed while it is favored if the size of the footprint is not the major design constraint to have a further back-off efficiency enhancement.

The stacking time-modulated PA structure is proposed to realize the pulse modulation, and its accurate circuit power and efficiency model with an equivalent switching capacitor is proposed to analyze the energy flow resulting from dynamic switching loss and static leakage current. Compared with the existing structure involving SPST switches along with the signal path, this time-modulated PA structure reduces the insertion loss when the switch is 'ON' and allows smaller power leakage when the switch is 'OFF'.

The design and analysis is validated through the simulation of a two-stage power amplifier simulation in 65-nm CMOS at 77 GHz. The 4-path STHS array DE is 57% larger at 3-dB PBO, 100% larger at 6-dB PBO, and 190% larger at 9-dB PBO compared with class-A/B PA. As for the 8-path STHS array, it achieves a 170% DE improvement at 6-dB PBO, and a 290% DE improvement at 10-dB PBO compared with class-A/B PA.

The STHS transmitter array originally adds spatial and temporal dimensions to realize back-off efficiency enhancement. Furthermore, it is worth emphasizing the compatibility of this method with other existing back-off enhancement structures such as the Doherty amplifiers and envelope tracking to achieve additional enhancement. This will be one potential solution to deal with device limited back-off efficiency.

References

[1] M. S. Afaqui, E. Garcia-Villegas, and E. Lopez-Aguilera, “IEEE 802.11 ax: Challenges and requirements for future high efficiency WiFi,” IEEE Wireless Communications, vol. 24, no. 3, pp. 130–137, 2016.

[2] Y. Cao and K. Chen, “Pseudo-Doherty load-modulated balanced amplifier with wide bandwidth and extended power back-off range,” IEEE Transactions on Microwave Theory and Techniques, vol. 68, no. 7, pp. 3172–3183, 2020.

[3] M. K. Kazimierzczuk, RF power amplifiers. Wiley Online Library, 2008, vol. 1.

[4] S. C. Cripps, RF power amplifiers for wireless communications. Artech house Norwood, MA, 2006, vol. 2.

[5] D. Chowdhury, P. Reynaert, and A. M. Niknejad, “Design considerations for 60 GHz transformer-coupled CMOS power amplifiers,” IEEE Journal of Solid-State Circuits, vol. 44, no. 10, pp. 2733–2744, 2009.

[6] H. Shanks and R. Bickmore, “Four-dimensional electromagnetic radiators,” Canadian Journal of Physics, vol. 37, no. 3, pp. 263–275, 1959.

[7] L. Poli, P. Rocca, G. Oliveri, and A. Massa, “Harmonic beamforming in time-modulated linear arrays,” IEEE Transactions on Antennas and Propagation, vol. 59, no. 7, pp. 2538–2545, 2011.

[8] I. Bregains, J. Fondevila-Gomez, G. Franceschetti, and F. Ares, “Signal radiation and power losses of time-modulated arrays,” IEEE Transactions on Antennas and Propagation, vol. 56, no. 6, pp. 1799–1804, 2008.
[9] S. Yang, Y. B. Gan, A. Qing, and P. K. Tan, “Design of a uniform amplitude time modulated linear array with optimized time sequences,” IEEE Transactions on Antennas and Propagation, vol. 53, no. 7, pp. 2337–2339, 2005.

[10] J. Fondevila, J. Bregains, F. Ares, and E. Moreno, “Optimizing uniformly excited linear arrays through time modulation,” IEEE Antennas and Wireless Propagation Letters, vol. 3, no. 1, pp. 298–301, 2004.

[11] L. Poli, P. Rocca, L. Manica, and A. Massa, “Handling sideband radiations in time-modulated arrays through particle swarm optimization,” IEEE Transactions on Antennas and Propagation, vol. 58, no. 4, pp. 1408–1411, 2010.

[12] Q. Zhu, S. Yang, L. Zheng, and Z. Nie, “Design of a low sidelobe time modulated linear array with uniform amplitude and sub-sectional optimized time steps,” IEEE Transactions on Antennas and Propagation, vol. 60, no. 9, pp. 4436–4439, 2012.

[13] G. Li, S. Yang, Y. Chen, and Z. Nie, “A hybrid analog-digital adaptive beamforming in time-modulated linear arrays,” Electromagnetics, vol. 30, no. 4, pp. 356–364, 2010.

[14] G. Li, S. Yang, and Z. Nie, “Direction of arrival estimation in time modulated linear arrays with unidirectional phase center motion,” IEEE Transactions on Antennas and Propagation, vol. 58, no. 4, pp. 1105–1111, 2010.

[15] D. Masotti, A. Costanzo, M. Del Prete, and V. Rizzoli, “Time-modulation of linear arrays for real-time reconfigurable wireless power transmission,” IEEE Transactions on Microwave Theory and Techniques, vol. 64, no. 2, pp. 331–342, 2016.

[16] A.-M. Yao, W. Wu, and D.-G. Fang, “Single-sideband time-modulated phased array,” IEEE Transactions on Antennas and Propagation, vol. 63, no. 5, pp. 1957–1968, 2015.

[17] B. Kim, J. Kim, I. Kim, and J. Cha, “The Doherty power amplifier,” IEEE microwave magazine, vol. 7, no. 5, pp. 42–50, 2006.

[18] P. Mahmoudian, D. Mandal, B. Bakkaloglu, and S. Kiaei, “Wideband hybrid envelope tracking modulator with hysteretic-controlled three-level switching converter and slew-rate enhanced linear amplifier,” IEEE Journal of Solid-State Circuits, vol. 54, no. 12, pp. 3336–3347, 2019.

[19] V. Camarchia, M. Pirola, R. Quaglia, S. Joe, Y. Cho, and B. Kim, “The Doherty power amplifier: Review of recent solutions and trends,” IEEE Transactions on Microwave Theory and Techniques, vol. 63, no. 2, pp. 559–571, 2015.

[20] E. Kaymaksut, D. Zhao, and P. Reynaert, “Transformer-based Doherty power amplifiers for mm-wave applications in 40-nm CMOS,” IEEE Transactions on Microwave Theory and Techniques, vol. 63, no. 4, pp. 1186–1192, 2015.

[21] F. Raab, “Efficiency of outphasing RF power-amplifier systems,” IEEE Transactions on Communications, vol. 33, no. 10, pp. 1094–1099, 1985.

[22] A. Zhang and M. S.-W. Chen, “A subharmonic switching digital power amplifier for power back-off efficiency enhancement,” IEEE Journal of Solid-State Circuits, vol. 54, no. 4, pp. 1017–1028, 2019.