High-k La$_x$Ce$_y$O$_z$ for Passivation of Si Substrate

Hock Jin Quah$^1$, Kuan Yew Cheong$^2$, Zainovia Lockman$^2$, Zainuriah Hassan$^1$, Way Foong Lim$^1$

$^1$Institute of Nano Optoelectronics Research and Technology (INOR), Universiti Sains Malaysia, 11800 USM, Penang, Malaysia.
$^2$School of Materials and Mineral Resources Engineering, Engineering Campus, Universiti Sains Malaysia, 14300Nibong Tebal, Seberang Perai Selatan, Penang, Malaysia

*way_foong@usm.my/wayfoong317@yahoo.com.sg

Abstract. High dielectric constant rare earth lanthanum cerium oxide (La$_x$Ce$_y$O$_z$) films have been studied as the passivation layers for silicon substrate. Effects of post-deposition annealing time (15, 30, and 45 min) at 700°C towards capacitance-voltage characteristics of the films were investigated. As the annealing time was increased from 15 to 45 min, negative flatband voltage shift was observed, signifying the presence of positive charges in the samples. Interface trap density value calculated for the samples has shown to be the lowest for the film annealed for 45 min, owing to the presence of silicate interfacial layer to improve the overall interfacial quality.

1. Introduction

Low dielectric constant ($k$) silicon dioxide ($\text{SiO}_2$) has long been recognized as the passivation layer-of-choice for silicon (Si)-based metal-oxide-semiconductor (MOS) devices. Nevertheless, as the device dimension has been designed smaller to fit for different applications, SiO$_2$ thickness has encountered its limit to be further scaled down. Alternatively, gate oxide materials with higher $k$ value than SiO$_2$ ($k$ = 3.9), such as Y$_2$O$_3$ [1], Al$_2$O$_3$ [2], CeO$_2$ [3], and La$_2$O$_3$ [4] have been proposed as the replacement oxide for MOS devices. Amongst these materials, particular interest has been placed on CeO$_2$ due to the presence of oxygen vacancies in the CeO$_2$ itself, which made it differentiated from other high $k$ oxides. The origin of having oxygen vacancy formation was due to the reducibility of CeO$_2$ [3].

Literatures have reported about the uniqueness of oxygen vacancies in CeO$_2$ in term of assisting in improving the current-voltage characteristics of the MOS device through an annihilation of positive charges (oxygen vacancies) by the negatively charged electrons injected from the MOS device during forward bias. On the other hands, the capability of CeO$_2$ to accept electrons and neutralize the charges was affected if CeO$_2$ was treated at a temperature higher than 800°C [5] while onset temperature for the CeO$_2$ reducibility was 600°C [6]. Previous studies reported about the introduction of lanthanum (La) as a foreign cation in the CeO$_2$ lattice to yield more oxygen vacancy formation, whereby the presence of La$^{3+}$ could substitute Ce$^{4+}$ in CeO$_2$, causing the neighbouring Ce$^{4+}$ cations to be reduced to Ce$^{3+}$, accompanied with oxygen vacancy formation [7-8]. With these, CeO$_2$ reducibility would not be affected at a higher temperature than 800°C and temperature lower than 600°C. Nonetheless, no attempt was performed at 700°C to investigate the performance of CeO$_2$ in terms of capacitance-voltage characteristics after incorporation of La$^{3+}$. 
2. Experimental Process
Chemical solution precursors of La\(_x\)Ce\(_y\)O\(_z\) were prepared using metal-organic decomposition (MOD) method [3] before spin-coated on Radio Corporation of America (RCA)-cleaned n-type Si(100) substrates at spin rate of 4000 rpm for 30s. The samples were subsequently put in a horizontal tube furnace for post-deposition annealing at 700°C in argon ambient for a certain duration (15, 30, and 45min), followed by slow cooling. Thermal evaporator (AUTO 306) was used to evaporate an array of Al gate electrodes (area = 0.0025 cm\(^2\)) on the samples. Crystalline phases of the samples were determined using X-ray diffraction (XRD, P8 Advan-Bruker) while capacitance-voltage (C-V\(_g\)) characteristics of the Al/La\(_x\)Ce\(_y\)O\(_z\)/Al MOS capacitors were measured using inductance-capacitance-resistance (LCR) meter (Agilent 4248A).

3. Results and discussion
Diffraction patterns of La\(_x\)Ce\(_y\)O\(_z\) films for all of the investigated samples are presented in Figure 1. It could be observed from the figure that a single diffraction peak oriented in (200) was present in the sample annealed for 15 min. As the annealing time was increased from 15 to 30 min, the (200)-oriented diffraction peak became sharper. In the sample annealed for 45 min, additional peaks allied with La\(_x\)Ce\(_y\)O\(_z\) oriented in (220) and (222) planes were detected. This observation suggested that a prolonged annealing time during post-deposition annealing process has encouraged the formation of crystalline phases of La\(_x\)Ce\(_y\)O\(_z\) in the samples.

![Figure 1. XRD patterns of La\(_x\)Ce\(_y\)O\(_z\) films subjected to post-deposition annealing at 700°C for 15, 30, and 45 min.](image1.png)

Figure 2 shows high frequency (1 MHz) capacitance-gate voltage (C-V\(_g\)) graphs of the Al/La\(_x\)Ce\(_y\)O\(_z\)/Al MOS capacitors swept from -2 V to 2 V. As the annealing time was increased from 15 to 45 min, accumulation capacitance level of the capacitors was showing a decreasing trend. The decrease in accumulation capacitance level could be related to the increasing in the formation of La\(_x\)Ce\(_y\)O\(_z\) diffraction peaks, as revealed by XRD analysis, which would be indirectly translated into an increase in the oxide thickness. In addition, all of the capacitors have demonstrated flatband voltage shift to a negative direction, indicating the presence of positive charges in the samples. The anticipation could be evidenced via a calculation of effective oxide charges present in the samples using the following equation (1) [9].
where $C_{ox}$ is the maximum accumulation capacitance, $q$ is the electronic charge, and $A$ is the capacitor area.

\[
Q_{\text{eff}} = \frac{\Delta V_{FB\text{ox}}}{qA}
\]

Effective oxide charges ($Q_{\text{eff}}$) values lying between $10^{11}$-$10^{12}$ cm$^{-2}$ for the investigated samples are depicted in Figure 3. In comparison, the largest $Q_{\text{eff}}$ value was perceived by the sample annealed for 30 min, followed by the sample annealed for 15 min while the lowest one was obtained at 45 min. The acquired $Q_{\text{eff}}$ trend as a function of annealing time could be associated with the fluctuation in the positive charges present in the La$_x$Ce$_y$O$_{z}$ films. As the annealing time was increased from 15 to 30 min, the increase in the positive charges was because of the increase in the formation of La$_x$Ce$_y$O$_{z}$.
along with oxygen vacancies. However, the positive charges were decreased as the annealing time was further increased to 45 min. This observation was plausible if the increased annealing time has also encouraged the formation of SiO$_x$ or LaSiO$_x$ silicate layer at the La$_x$Ce$_y$O$_z$/Si interface in the sample. The presence of silicate layer would decrease much of the positive charges as a result of charge compensation.

Further investigation was carried out by calculating interface trap density ($D_{it}$) present in the samples using Terman’s method, as conveniently shown in equation (2) [10].

$$D_{it} = \frac{C_0 \Delta V_g}{q A d \Phi_s} \quad (2)$$

where $\Delta V_g = V_g - V_{g\text{(ideal)}}$ is the voltage shift of the experimental curve from the ideal curve, $V_g$ is the experimental gate voltage, and $\Phi_s$ is the surface potential of Si at a specific gate voltage. Figure 4 presents the calculated $D_{it}$ values as a function of energy trap level ($E_c - E_t$) for the investigated samples. The lowest $D_{it}$ value was obtained by the sample annealed for 45 min, followed by 15 and 30 min. This observation was in agreement with the aforementioned trend obtained for $Q_{eff}$. The acquisition of the lowest $D_{it}$ for 45 min-annealed sample was an indication to show an improvement in the interfacial quality for the sample, contributed by the existence of SiO$_x$ or LaSiO$_x$ interfacial layer.

![Figure 4](image.png)

**Figure 4.** Interface trap density of the Al/La$_x$Ce$_y$O$_z$ films as a function of $E_c - E_t$.

4. **Conclusion**

Effects of post-deposition annealing time (15, 30, and 45 min) for La$_x$Ce$_y$O$_z$ films at 700ºC were investigated in terms of capacitance-voltage characteristics. The lowest $Q_{eff}$ and $D_{it}$ values have been perceived by the film annealed for the longest duration (45 min). The improvement was related to the formation of silicate layer at the interface between La$_x$Ce$_y$O$_z$ and underlying Si substrate.

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