Abstract

The different cores of state-of-the-art multicore processors are performance asymmetric: they are different in terms of their clock speeds and other capabilities. Such heterogeneous multicore processors pose challenges to existing Dynamic Load Balancers in achieving optimum performance. A load balancer taking the load balancing related decisions assuming all cores to be homogeneous, introduces unnecessary overheads of time, does not exploit the capabilities of higher performance cores, and consequently fails to achieve the possible performance improvement. We, therefore, propose a Capability Aware Dynamic Load Balancer which performs efficient load balancing for asymmetric multicore processors by addressing the aforesaid issues. Considering the difference in clock speeds as the heterogeneity among different cores, the proposed load balancer improves the Turn Around Time of processes significantly as compared to Asymmetry unaware Linux load balancer. The results of experimentation exhibit the performance gain in the range of 4-9%, for three different multicore systems having 32, 64 and 128 cores respectively.
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Index Terms

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Keywords

Dynamic Load Balancing, DLB, Load Balancer, NUMA, Speed Core