Design and process features of CMOS SOI transistors with increased tolerance to the total dose

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Abstract. The paper considers methods to improve integrated circuits' tolerance based on the SOI CMOS technology to total dose radiation. The main effects that occur in SOI CMOS transistors as a result of radiation response with the VLSI are discussed. The final part of the work demonstrated the main methods that make it possible to increase the radiation hardness of ICs based on the SOI CMOS technology. The advantages and disadvantages of each technique will be discussed. The prospects for developing microelectronics products with increased tolerance to external influences will be analyzed under constant process node scaling.

1. Introduction

For more than 30 years, Synova, Honeywell, Lincoln Lab, and many other companies have always been using SOI technology to develop integrated circuits (ICs) for space and special applications. Its significant advantages explain the SOI technology features: a decrease of the active areas of the transistor, increased performance, and complete dielectric isolation of a single transistor [1, 2]. A significant disadvantage of commercial SOI CMOS technology is the decreased tolerance of n-channel transistors to the total dose caused by a presence of buried oxide in the transistor structure that can accumulate an additional positive charge near-surface area [3, 4]. In this context, the role of research work implemented based on SOI CMOS technology in the field of ICs development with increased resistance to accumulated dose is growing.

There are two main groups of hardening methods for CMOS SOI ICs: technological methods – RHbP (Radiation Hardening by Process) and design – RHbD (Radiation Hardening by Design). The lack of necessity to modify the commercial technology has resulted in the predominance of RHbD solutions in radiation-resistant IC design. Despite this, the most significant results regarding the total dose tolerance can be achieved by integrating RHbP methods into production. Transistors with an A- and H-type configuration, which can be considered a classic example of implementing the RHbD techniques, are commonly used to design radiation-hardened ICs based on SOI technology [5].

2. Effects in transistors induced total dose radiation

Currently, the primary technology used to produce modern ICs for space and special applications, subject to increased reliability and resistance to external influences, is SOI CMOS technology. This technology allows the production of partially and fully depleted SOI transistors, the main difference...
being the different depth of the region of space charge in the silicon film, which is ultimately an essential factor in the analysis of the effects related to the influence of the accumulated charge on the degradation of the device's electrical characteristics. The SOI transistor structure can be imagined as the main transistor and two additional parasitic transistors, shown in figure 1.

![Figure 1. Schematic illustration of a SOI n-channel transistor with additional parasitic elements.](image)

The integration of a parasitic MOS transistor into the schematic model SOI transistor is explained by the presence of positive charge in the buried oxide that contributes to the lower transistor's activation at a certain critical total dose ionizing radiation leading to an additional path for the leakage currents. The gate of the parasitic transistor is a substrate, to which, in the general case, any potential can be applied. Figure 2, a shows the parasitic transistor's current dependence on the substrate potential for different ionizing radiation doses. Accordingly, even at zero potential, which is the most common case in practice, the generation of charge in the buried oxide results in significant leakage currents. The characteristics in figure 2, b clearly show that leakage current values can significantly limit the applicability of ICs operating in outer space.

![Figure 2. I_d–V_g characteristics for: a) a back–gate transistor irradiated to 1 Mrad (SiO_2) and its effect on b) the top–gate transistor leakage current. The transistors were irradiated in the OFF (V = V = 0 V; V = 5 V) bias condition [6].](image)
The existence of a bipolar parasitic transistor is explained by the necessity to consider the effect of a floating body characteristic of partially depleted (PD) transistors. The nature of this effect is the generation of the excess charge as a result of impact ionization in high electrical fields on the silicon drain/film junction. In the case of the operation of the ICs in outer space, radiation-induced carriers are added to the non–equilibrium charge carriers resulting from the impact ionization, aggravating the effect. The $I_d$–$V_b$ characteristic is shown in figure 3. This effect shows itself in the form of a sharp step graded, increasing the current at a high potential at the drain.

Figure 3. $I_d$–$V_b$ characteristics versus ionizing dose of a 0.1 pm gate length PD NMOS/SOI transistor processed on medium-dose SIMOX substrate. The front gate is grounded ($V_g = 0$ V), and the drain voltage is equal to 0.1 V (solid symbols) or 2 V (open symbols). During irradiation, the drain is biased at 2 V, and other terminals (gate, source, substrate) are grounded [7].

In the case of a fully depleted transistor, the accumulation of a positive charge in a buried oxide has some features due to the parasitic's electrical coupling and the main MOS transistors. It has been found that the change threshold voltage in the main transistor's is proportional to the shift in the parasitic transistor's threshold voltage and expressed as the $k$ electrical coupling coefficient [8]:

$$k = \frac{C_{Si}C_{box}}{C_{top}(C_{Si}+C_{box})},$$  \hspace{1cm} (1)$$

$$\Delta V_{topgate} = k\Delta V_{backgate}$$  \hspace{1cm} (2)$$

where $C_{Si}$, $C_{box}$, and $C_{top}$ are silicon film, buried oxide, and gate oxide channel capacities. Since the manufacturing technology of fully depleted SOI transistors does not involve a pocket, the charge accumulated in the buried oxide leads to a significant shift in the bottom transistor's threshold voltage, thereby affecting the threshold voltage of the main transistor. It follows from formula (1) that decreased thickness of the buried oxide can also lead to the degradation of the total dose tolerance in SOI transistors, thereby depriving developers of the opportunity to reduce the positive charge's value by thinning the bottom oxide.

3. Methods of increasing the total dose tolerance

As mentioned earlier, radiation effects have a severe impact on integrated circuits' parameters, leading to parametric and functional failures. For this reason, designers have developed several techniques to improve the hardening of IC's to the total dose. Whether to use one or another method primarily depends on the quality of used wafers. Because of that reason, before the execution of the expensive IC process operations, it's necessary to do a thorough analysis of the initial wafers' parameters to avoid the further uncontrollable dispersion of the parameters in the final product.

3.1. Process methods of increasing the total dose tolerance

Comparison bulk and SOI technology show that in addition to the gate and isolating oxide that are actively used in both transistor structures, SOI technology involves the presence of a buried oxide that is generally engaged in the formation of an additional path for leakage currents. In this regard, the appearance of the radiation-hardened buried oxide is an important factor causing the increased tolerance
of ICs based on SOI technology. Following main methods to improve the electrical characteristics of the buried oxide to the total dose can be identified:

- Using of multiphase oxygen implantation at the stage of buried oxide formation by the SIMOX method (Separation by Oxygen Implantation), which allows compensating for the loss of oxygen due to the oxygen diffusion from the oxide at the high-temperature annealing stages, thus increasing the crystalline uniformity of the formed oxide [9];
- The introduction of traps into the buried oxide structure by implanting an acceptor impurity: silicon, aluminum, germanium, boron, and nitrogen. Thus, it is possible to compensate for the positive charge accumulated in the dielectric structure by introducing electron traps [10–11].

Table 1 shows a comparison of the electrical characteristics of the buried oxides based on SIMOX and BESOI (Bonded and Etched-Back Silicon-on-Insulator) technology. Analysis of the results shows that using techniques to optimize the oxide's parameters to resilience the total dose radiation allows influencing the traps' density, thus increasing the level of resistance regardless of the technology of producing the buried oxide.

| Oxide formation technology | Oxide Thickness, $T_{ox}$ (nm) | Density of traps, $N_{th}$ ($cm^{-2}$) |
|----------------------------|----------------------------------|----------------------------------------|
| SIMOX [12]                 | 400                              | $(1.3\pm0.4)*10^{13}$                 |
| Hardened SIMOX [13]        | 370                              | $1.08*10^{12}$                         |
| BESOI [14]                 | 400                              | $(1.5\pm0.2)*10^{13}$                 |
| Hardened BESOI [15]        | 400                              | $5*10^{12}$                           |

Reducing technological node is one of the most promising methods to increase the tolerance of CMOS SOI ICs to ionizing radiation in space. A detailed description of the basic scaling principles is given in the work [16]. Indeed, scaling makes it possible to achieve increased resistance to the total dose of radiation by thinning the gate oxide, lowering the operating voltage, and increasing the pocket's dopant concentration. Despite the seeming universality, the application of this method, as follows from figure 4, is limited by a design level of 32 nm due to using the fully depleted SOI CMOS structures with further scaling, significantly increasing the influence of the trapped charge in a buried oxide on the main transistor parameters.

![Figure 4](image-url) Commercial Technology TID response of off-state current for a dose of 1 Mrad (SiO$_2$) versus technology scaling showing vulnerability turnaround after 32 nm [8].
It should be noted that a decreased total dose tolerance is also observed for FinFET structures with a technological level of 14 nm. For bulk FinFET structure, this phenomenon is supposedly associated with the generation of additional charge carriers in the transistor body, which leads to an increase in leakage currents. Note that the use of a sufficiently thin gate dielectric increases the RILC effect's role (Radiation-induced leakage current). This effect is to increase the leakage current under the action of ionizing radiation through the gate insulator. Presumably, the described leakage current is associated with the oxide's degradation properties, which is reflected in an increase in the number of traps in its volume, facilitating the tunneling of carriers into the gate electrode [17].

3.2. Constructive methods of increasing the total dose tolerance

Transistors with H- and A-type structure are widely used to design radiation-hardened CMOS ICs (figure 5). Unlike standard commercial solutions, using H- and A-type transistors eliminates side leakage currents by optimizing gate geometry and using the p+ guard region. The suppression of the floating body's effect in the presented structures is realized by using a contact to the pocket, which generally increases the area of the ICs. In this regard, the urgent task is to select the optional position of the contacts in the pocket for efficient collection of induced charge by cosmic radiation with a minimum increase of the circuit area. Using of A-type structures is recommended for circuits that have increased requirements for the occupied area of ICs. In contrast, H-type structures are a universal solution for cases when required of symmetry of active regions and the possibility of applying independent contact potentials [5].

![Figure 5. Examples of n-channel SOI MOSFET designs. A) transistor of H-type, B) transistor of A-type [5].](image)

The configuration of the BUSFET (Body Under Source FET) proposed by a group of Sandia laboratory researchers and shown in figure 6 also allows producing radiation-hardened SOI CMOS ICs [18]. Due to the different depth drain/source areas, leakage currents flowing on the buried oxide are reduced, thereby improving the BUSFET structure’s reliability. It should be noted that this method has not been commonly used due to the following disadvantages:

- At the stage of the formation of the drain/source areas, the necessary use of additional masks increases the technology route's difficulty and cost of the final product;
- The creation of additional parasitic capacitances by the source/substrate interface;
- The limitation of the silicon film's maximum allowable thickness is caused by necessity creating the device's active regions with different depths.
Since 1980, Honeywell has been making significant efforts to develop radiation-hardened microelectronic ICs. Today, the company’s most innovative product is 150 nm SOI CMOS process (figure 7), which allows producing SRAM memory cells up to 64 Mb and application-specific integrated circuits (ASICs). To provide radiation tolerance of its products, Honeywell uses RHbP methods aimed at improving the quality of the oxide and using STI (Shallow Trench Isolation) and special design of the CMOS structure. As a result, Honeywell can produce IC with increased requirements to total dose, up to 1 Mrad, with minimal increase in the area [19]. The advantages described above and the possibility of using the scaling lead to a conclusion that presented technology, and its modifications are very promising in the visible future.

Analysis of the X-FAB SOI CMOS structure based on the XT-018 technology (figure 8) shows the possibility of manufacturing ICs with increased total dose tolerance. Such a conclusion is based on the features of the presented structure. We can mention STI's presence, the use of a silicon film with a thickness of several micrometers, and the formation of a double well. The presented design solutions made it possible to completely exclude the latching effect and isolate the active region of the main transistor's device from the influence of the charge accumulated in the buried oxide [20, 21]. However, using a thick silicon film leads to increasing the edge in-transistor leakage currents, which forces developers to use ring gate structures, leading to an increase in the IC area.

Using a generator of the back-biased substrate, which includes a control device and a charge pumping unit, can be considered another design solution that increases the IC’s total dose tolerance. This method’s principle is to apply a back bias to the substrate’s contact, thereby allowing the off-state of the bottom n-channel transistors to be maintained during the accumulation of a positive charge in the buried oxide. Unfortunately, this method has some disadvantages, such as increased circuit area, a limited range of
applied voltages to the substrate, the necessity of forming a high-quality contact to the substrate, and the charge pump unit [22].

![Device schematic cross section of X-FAB XT018](image)

**Figure 8.** Devices schematic cross section of X-FAB XT018 [21].

### 4. Conclusion

An analysis of the literature shows that the charge captured in the volume of a buried dielectric near the Si/SiO₂ interface and on surface states is responsible for the degradation of the electrical parameters of space and special-purpose ICs based on SOI technology. In contrast to the bulk radiation effects controlled by RHbD techniques, surface effects require developers to use both – process and design solutions. One of the most practical methods is using a reverse bias generator on the substrate and scaling principles. This approach allows developers to stay within the framework of the basic technology. However, according to the work results, starting from the 32 nm node, a further increase of the SOI IC tolerance to the total dose radiation becomes problematic. These difficulties are due to the necessity of using fully depleted SOI transistors with lower total dose radiations tolerance because the technology involves undoped silicon film. Summarizing the above, we can conclude that the design of ICs with increased total dose tolerance must be carried out on partially depleted SOI transistors using both process and design solutions.

Despite the conclusion, many companies are actively developing radiation-hardened ICs of 28 nm nodes and lower. BAE, which provides IC design services based on 14 nm FinFET bulk technology, has achieved the greatest success in this direction. The work of the united European consortium DAHLIA, developing a radiation-hardened system on a chip based on the fully depleted 28 nm SOI technology of the STMicroelectronics company also should be noted [23].

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