Operation of thin-film thermoelectric generator of Ge-rich poly-Ge$_{1-x}$Sn$_x$ on SiO$_2$ fabricated by a low thermal budget process

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A thin-film thermoelectric generator composed of p- and n-type poly-Ge$_{1-x}$Sn$_x$ ($x \approx 0.02$) on a Si(001) covered with SiO$_2$ has been successfully fabricated by low thermal budget processes (under 300 °C) and demonstrated for the first time. Both the crystallization and dopant activation were simultaneously performed using pulsed UV laser irradiation in flowing water. A recorded activation ratio of Sb in the poly-Ge$_{1-x}$Sn$_x$ enabled a relatively high power factor (9.2 μW cm$^{-1}$ K$^{-2}$ at RT), which is comparable to the counterparts of n-type Ge$_1$Sn$_x$ layers epitaxially grown on InP (001). © 2019 The Japan Society of Applied Physics

Sequential 3D integration of a thin-film energy-harvesting device in a silicon (Si) chip is strongly desired for realizing a standalone sensing network system, called the internet-of-things society and/or trillion sensor universe, coupled with low-power consumption technologies. The thermoelectric generator (TEG), which could convert waste heat into electricity, is one of the options. Taking the distribution of a huge number of sensors all over the world into consideration, the utilization of the same technology to manufacture next-generation Si-based integrated circuits (ICs) is preferable, including the material. In addition, from a physics viewpoint, a small amount of tin (Sn)-incorporated germanium (Ge), which is called Ge-rich Ge$_{1-x}$Sn$_x$, in this letter, is one of the attractive TEG materials owing to its higher carrier mobility, $^{7,8}$ lower thermal conductivity,$^{9,10}$ and lower polycrystallization temperature $^{11,12}$ than those of Si and Si$_1$Ge$_x$.

Technologies for forming polycrystalline Ge (poly-Ge)$^{11,13-29}$ and Ge-rich poly-Ge$_{1-x}$Sn$_x$ $^{12,30-33}$ layers on an insulating surface have long been intensively studied in the research field of 3D-ICs, specifically, solid-phase crystallization (SPC), $^{11,18,30-32}$ laser annealing, $^{19,21,33}$ chemical vapor deposition (CVD), $^{22,23,29}$ flash-lamp annealing (FLA), $^{24}$ metal-induced crystallization, $^{25,26}$ etc. On the other hand, the thermoelectric studies are limited at the present stage. There are a few reports for only p-type layers of poly-Si$_{1-x}$Ge$_x$ ($x = 0-1$) $^{34}$ and poly-Ge$_{1-x}$Sn$_x$ ($x < 0.02$) $^{35}$ grown by Al-induced layer exchange and SPC, respectively; the poly-Ge (poly-Ge$_{1-x}$Sn$_x$) layers showed maximum high power factors (PFs) of 4.3 μW cm$^{-1}$ K$^{-2}$ ($\sim 1 \mu$ W cm$^{-1}$ K$^{-2}$) at room temperature (RT). From a device perspective, an experimental demonstration of the n-type doping in Ge-rich poly-Ge$_1$Sn$_x$ layers and clarifying its thermoelectric property are desired. However, the property has to date not been obtained, because heavy n-type doping is still under development owing to the low solid solubility $^{36}$ and low activation ratio $^{37}$ of group-V dopants in Ge.

Against such a background, we recently developed a new method to perform dopant activation and polycrystallization simultaneously by using pulsed UV laser annealing (duration: 55 ns, wavelength: 248 nm) through flowing water, for antimony (Sb)-doped amorphous Ge$_1$Sn$_x$ (a-Ge$_{1-x}$Sn$_x$) layers with an initial Sn content of 2%. $^{38,39}$ Thanks to the extremely short penetration depth of the UV laser and cooling effect by the water, the process temperature in the underlying Si substrate covered with a 1-μm-thick SiO$_2$ could be maintained at less than 50 °C. $^{39}$ In addition, it was revealed that the ultra-short-time annealing was effective to suppress a significant segregation of Sb atoms, and thus, a high activation ratio of Sb (64%) could be obtained, resulting in a heavy n-type doping over 10$^{20}$ cm$^{-3}$. It is noted that the obtained activation ratio (64%) is at least five times larger than previous experimental results in Ref. 40, where an activation ratio of 13% was obtained for a phosphorus (P)-doped poly-Ge layer with an initial P content of 1 × 10$^{20}$ cm$^{-3}$ crystallized by FLA. In this letter, we first present the thermoelectric properties of the n-type poly-Ge$_{1-x}$Sn$_x$ layers grown on SiO$_2$ for realizing poly-Ge$_{1-x}$Sn$_x$ thin-film TEGs. 3D integration and operation of the thin-film TEG composed of p- and n-type poly-Ge$_{1-x}$Sn$_x$ ($x \sim 0.02$) on a Si chip have been successfully demonstrated for the first time using low thermal budget processes under 300 °C.

An n-type Si(001) wafer covered with a 1-μm-thick SiO$_2$ layer was used as the substrate; the thickness of the a-Ge$_{0.98}$Sn$_{0.02}$ layers with a dopant on the substrates was fixed as 50 nm. The a-Ge$_{0.98}$Sn$_{0.02}$ layers were deposited at RT using a molecular beam deposition (MBD) method with a solid source at a deposition rate of ~0.04 nm s$^{-1}$. The element for the n- or p-type doping was chosen as Sb or gallium (Ga), respectively, which have oxidation resistance during the pulsed laser annealing (PLA) in flowing water as discussed in the previous works. $^{38,39}$ The dopant concentration of Sb (Ga) was 1–6 × 10$^{20}$ (3 × 10$^{20}$) cm$^{-3}$. To obtain a large grained growth, high-power ($E = 250–270$ mJ cm$^{-2}$) laser irradiation was performed on the a-Ge$_{0.98}$Sn$_{0.02}$ surfaces with a scan speed to correspond to 20-irradiation-times per location. As described above, the maximum temperature of
the Si wafer could be maintained below 50 °C and the temperature in all regions drops to 40 °C only 10 μs after laser irradiation.39) By using such a low thermal budget process, we fabricated poly-Ge_{1−x}Sn_{x}-based thin-film TEGs. The key fabrication steps are summarized in Fig. 1(a). An a-Ge_{0.98}Sn_{0.02} layer with an Sb dopant of 1 × 10^{20} cm^{−3} was deposited on the substrates using MBD. After deposition of a hard mask (HM) of a 200-nm-thick SiO_{2} by plasma enhanced CVD (PECVD) at 300 °C, the stack layers were patterned by wet etching to form island areas (length: 5 mm, width: 0.7 mm). Similarly, islands consisting of an a-Ge_{0.98}Sn_{0.02} layer with a Ga dopant of 3 × 10^{20} cm^{−3} were formed between two islands of the Sb-doped Ge_{0.98}Sn_{0.02} layers. These a-Ge_{0.98}Sn_{0.02} layers were covered with the HM again and then crystallized using the PLA in water at \( E = 250 \text{ mJ cm}^{−2} \). After removing the HM, Al electrodes were formed at the end of the islands using thermal evaporation and a wet etching process to series-connect the n- and p-type islands alternately. The connected number of n- and p-type poly-Ge_{1−x}Sn_{x} islands were two and three, respectively. Note that the maximum substrate temperature (300 °C) was limited by the PECVD process, not the crystallization process by the PLA in flowing water.

For the thermoelectric measurements, two Peltier devices were placed under the substrate, as shown schematically in Fig. 1(b); they produced a thermal gradient \( −\nabla T \) from the heating to cooling region. Two sheathed thermocouples [TC1 and TC2 in Fig. 1(b)] were mechanically contacted at the first and final Al electrodes of the thin-film TEGs to monitor the temperature difference \( \Delta T \), voltage \( V \), and current \( I \) simultaneously, where a semiconductor device analyzer (Keysight B1500A) was used to measure these parameters. The Seebeck coefficient \( S \) of the poly-Ge_{1−x}Sn_{x} layers was determined from the slope of \( \Delta T−\Delta V \) plots before the island patterning; the carrier density and electrical conductivity \( \sigma \) were determined by Hall effect measurements using a micro-Hall-bar structure (length: 7 μm, width: 5 μm).

First, let us discuss the basic thermoelectric properties of \( \sigma \) and \( S \) measured at RT, as a function of the Hall electron density. They are summarized in Figs. 2(a) and 2(b), respectively. Experimental data for the Sb-doped poly-Ge_{1−x}Sn_{x} layers (star symbols) and Sb-doped Ge_{1−x}Sn_{x} layers with various Sn content (0% –14%) epitaxially grown on InP(001) (triangle symbols) are plotted, where the gray-scale intensity in the triangle symbols corresponds to \( x \). In Fig. 2(a), the Irvin curve for n-type bulk Ge (solid line) is also plotted. The \( \sigma \) increases with the electron density and reaches the Irvin curve multiplied by 0.6 (dashed line) over the density of 5 × 10^{19} cm^{−3}, which is owing to improvement of the mobility. In Fig. 2(b), we also

![Fig. 1. (Color online) (a) Key fabrication steps of a poly-Ge_{1−x}Sn_{x}-based thin-film TEG, where the maximum substrate temperature was 300 °C (SiO_{2} HM formation). (b) Schematics of a system for thermoelectric measurements.](image)
show $S$ values of n-type Ge for comparison, which are theoretically calculated by solving the following Boltzmann transport equation\textsuperscript{[23]}

$$
S = -\int_0^\infty \frac{\tau g E (E - E_F) \left( \frac{\partial f}{\partial E} \right) dE}{eT} 
$$

where $e$ is the elementary charge, $T$ is the absolute temperature, $E$ is the electron energy, $E_F$ is the Fermi energy, $f$ is the Fermi–Dirac distribution function, $g$ is the density of states and $\tau$ is the relaxation time, which can be expressed by $1/\tau = \sum_1/\tau_j$ and the $\tau_j$ is proportional to $E^{1.5}$ or $E^{-0.5}$ depending on the scattering processes. Specifically, in a heavily doped region for polycrystals, there are three dominant scattering processes: ionized impurity scattering ($\tau_{\text{imp}} \propto E^{1.5}$),\textsuperscript{[44]} short-range defect scattering ($\tau_{\text{SD}} \propto E^{-0.5}$),\textsuperscript{[45]} and grain boundary scattering ($\tau_{\text{GB}} \propto E^{-0.5}$).\textsuperscript{[46]} The solid (broken) curve in Fig. 2(b) is calculated using Eq. (1) for the relaxation time with an energy dependence of $E^{1.5}$ ($E^{-0.5}$).\textsuperscript{[47]} It is found that the $S$ values for the poly-Ge$_{1-x}$Sn$_x$ layers are in good agreement with the calculated $S$ curve with an energy dependence of $E^{-0.5}$, implying that the short-range defect scattering and/or grain boundary scattering are still dominant even in the region of a relatively high electron density over $10^{20}$ cm$^{-3}$. The trend is similar to the n-type Ge$_{1-x}$Sn$_x$ layers epitaxially grown on InP(001).\textsuperscript{[41]}

To clarify the PFs and compare them with other n-type TEG materials, we replotted the values of $\sigma$ and $|S|$ for the poly-Ge$_{1-x}$Sn$_x$ layers in a logarithmic graph. They are summarized in Fig. 3, where epitaxial Ge$_{1-x}$Sn$_x$ layers,\textsuperscript{[43]} bulk Si$_{1-x}$Ge$_x$,\textsuperscript{[47]} and poly-Bi$_2$(TeSe)$_3$ layers\textsuperscript{[48]} are also shown for comparison. By tuning the $\sigma$ and $S$ in the electron density, a relatively high PF ($=S^2\sigma$) of 9.2 $\mu$Wcm$^{-1}$ K$^{-1}$ was obtained for the poly-Ge$_{1-x}$Sn$_x$ layer. The maximum value is comparable to the counterparts of n-type Ge$_{1-x}$Sn$_x$ layers epitaxially grown on InP(001) (10 $\mu$Wcm$^{-1}$ K$^{-2}$).\textsuperscript{[41]}

Fig. 3. (Color online) Replotted data of $\sigma$ and $|S|$ of the Sb-doped poly-Ge$_{1-x}$Sn$_x$ layers on SiO$_2$ (star symbols) at RT. Data of other n-type TEG materials at RT are also shown for comparison: Ge$_{1-x}$Sn$_x$ layers with different Sn content (0%–14%) epitaxially grown on InP(001) (triangle symbols),\textsuperscript{[43]} Si$_{1-x}$Ge$_x$ bulk used in a radioisotope TEG (open circle symbol)\textsuperscript{[47]} and poly-Bi$_2$(TeSe)$_3$ layers\textsuperscript{[48]} (open square symbol). Gray-scale intensity in the triangle symbols corresponds to the Sn content. Broken lines show equal PFs ($|S| = S^2\sigma$).

however, the obtained maximum value in the present study is still 38% of that for n-type poly-Bi$_2$(TeSe)$_3$ layers (24 $\mu$Wcm$^{-1}$ K$^{-2}$).\textsuperscript{[49]} Note that $\sigma$ in the poly-Ge$_{1-x}$Sn$_x$ is at least twice as low as the expected values from the Sb-doped Ge$_{1-x}$Sn$_x$ layers pseudomorphically grown on Ge(001).\textsuperscript{[41]} Therefore, the present study does not indicate the limitation of n-type Ge$_{1-x}$Sn$_x$. Here, for reference, we estimated values of the thermal conductivity $\kappa$ of 3.0 Wm$^{-1}$ K$^{-1}$ at RT and the dimensionless figure of merit ($zT = S^2\sigma T/k$) of $\sim$0.09 at RT for the poly-Ge$_{1-x}$Sn$_x$ layer with an initial Sb content of $2 \times 10^{20}$ cm$^{-3}$, although the measurement direction of $\kappa$ (perpendicular to the substrate) is different to that of PF (parallel to the substrate). The measurements of $\kappa$ were carried out by using the pico-second thermoreflectance in the front-detection-front-heating configuration (PicoTherm Corp. PicoTR).\textsuperscript{[50]} The $\kappa$ value (3.0 Wm$^{-1}$ K$^{-1}$) is approximately 20 times lower than that for bulk Ge (60 Wm$^{-1}$ K$^{-1}$),\textsuperscript{[51]} and still lower than that for bulk Si$_{1-x}$Ge$_x$ (4.5 Wm$^{-1}$ K$^{-1}$).\textsuperscript{[47]} Consequently, the $zT$ value ($\sim$0.09 at RT) comparable to that for the bulk Si$_{1-x}$Ge$_x$ ($\sim$0.1 at RT)\textsuperscript{[47]} was achieved, although $\sigma$ in the poly-Ge$_{1-x}$Sn$_x$ layer was degraded compared with bulk Ge. By interconnecting the n- and p-type poly-Ge$_{1-x}$Sn$_x$ layers with Al electrodes, a thermoelectric operation was successfully observed, which is the first demonstration of poly-Ge$_{1-x}$Sn$_x$ thin-film TEGs with the in-plane $\pi$-type structure (Fig. 4). We confirmed a reasonable open-circuit voltage of 4.5 mV at $\Delta T = 10$ K, which is almost consistent with the estimated value (5.3 mV) from $S$ in the poly-Ge$_{1-x}$Sn$_x$ layers (n-type: $-126 \mu$V K$^{-1}$, p-type: 93 $\mu$V K$^{-1}$). The obtained short-circuit currents, however, were at least three times smaller than the value expected from $\sigma$ in the poly-Ge$_{1-x}$Sn$_x$ layers (n-type: 119 Scm$^{-1}$, p-type: 223 S cm$^{-1}$), which is caused mainly by a large contact resistance at the interface between the Al and the n-type poly-Ge$_{1-x}$Sn$_x$ layers. This issue will be solved by using the Fermi-level depinning technique, which has been actively discussed in the field of metal contact with Ge.\textsuperscript{[52–59]} Note that the maximum thermoelectric power (40 pW) obtained in the present study has not been optimized, so that the performance could be improved by tuning the carrier densities and reducing the internal and parasitic resistances. Moreover, it should be noted that the maximum substrate temperature is limited by the HM formation process, not the
crystallization process of the PLA in flowing water. Actually, the crystallization method could be applicable to form poly-Si on a flexible substrate of polyethylene terephthalate.60) Therefore, we believe that these results open up a higher degree of freedom for the fabrication of thin-film TEGs, not only on a Si chip, but on flexible substrates such as glass, plastic and paper.

In conclusion, we addressed the thermoelectric properties of n- and p-type poly-Ge0.98Sn0.02 layers on SiO2 and investigated the feasibility of a poly-Ge1−xSnx thin-film TEG with the in-plane π-type structure integrated on a Si substrate covered with SiO2. The key highlight of this work also includes the sub-300 °C method of the PLA in flowing water for the polycrystallization and dopant activation. A relatively high PF (maximum: 9.2 μWcm−1 K−2 at RT) was also achieved even for the n-type poly-Ge0.98Sn0.02 layers owing to an excellent activation ratio of the Sb atoms. These results are quite informative for realizing sequential integration of poly-Ge1−xSnx thin-film TEGs in a 3D-IC without degradation of the underlying circuits.

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E. Machida, M. Horita, Y. Ishikawa, Y. Uraoka, T. Okuyama, and H. Ikenoue, 19th Int. Display Workshops in conjunction with Asia Display, 2012, p. 303.