IMPROVED ANALYTICAL DELAY MODELS FOR COUPLED INTERCONNECTS

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ABSTRACT

With the advance of the process technologies into deep submicrometer domain, crosstalk between adjacent wires of global interconnects has become more severe. The delay caused by the crosstalk becomes a bottleneck to system performance, especially those with global interconnects. To alleviate crosstalk delays, accurate delay models are needed. In particular, analytical models are more desirable for their simplicity and transparency to technology, which lead to efficient crosstalk avoidance code (CAC) designs. Currently, most existing CAC designs are based on the analytical model proposed by Sotiriadis et al., which has limited accuracy. In this paper, we propose new analytical delay models, and our extensive simulations show that they have improved accuracy.

Index Terms— Crosstalk, delay, interconnects

1. INTRODUCTION

With the process technologies scaling down into deep submicrometer, coupling capacitance between adjacent wires becomes more significant and increases the crosstalk delays greatly. Recent International Technology Roadmap of Semiconductors (ITRS) [1] shows that gate delay decreases with scaling while global wire delay increases. The crosstalk delay becomes a major part of the total delay, and greatly affects the overall system performance.

To evaluate and alleviate crosstalk delays, various delay models of interconnects have been proposed recently (see, for example, [2–7]), most of which are based on numerical approaches and offer little insight (see, e.g., [2–5]). Although these numerical models can have high accuracy, they have several drawbacks, such as bulky lookup tables, dependence on technology, poor portability, and high complexity.

In contrast, analytical delay models (see, e.g., [6, 7]) depend on few technology parameters and have very low computational complexities. The model in [6] has much higher accuracy. However, it is not conducive to alleviate the crosstalk. One widely used analytical delay model, proposed by Sotiriadis et al. [7], illustrates the connection between delays of coupled interconnects and transition patterns and appears to be the most comparable previous delay model to our work in this paper. Based on the model in [7], the delay of the \( k \)-th wire \((k \in \{1, 2, \cdots, m\})\) of an \( m \)-bit bus is given by

\[
T_k = \begin{cases} 
\tau_0[(1 + \lambda)\Delta_1^2 - \lambda\Delta_1\Delta_2], & k = 1 \\
\tau_0[(1 + 2\lambda)\Delta_k^2 - \lambda\Delta_k(\Delta_{k-1} + \Delta_{k+1})], & k \neq 1, m \\
\tau_0[(1 + \lambda)\Delta_m^2 - \lambda\Delta_m\Delta_{m-1}], & k = m, \end{cases}
\]

where \( \lambda \) is the ratio of the coupling capacitance between adjacent wires and the loading capacitance, \( \tau_0 \) is the intrinsic delay of a transition on a single wire, and \( \Delta_k \) is 1 for 0 → 1 transition, -1 for 1 → 0 transition, or 0 for no transition on the \( k \)-th wire. We observe that in this model, the delay of the \( k \)-th wire depends on the transition patterns of wires \( k-1, k, \) and \( k+1 \) only. As shown in Eq. (1), all possible values of \( T_k \) are given by \((1 + i\lambda)\tau_0\) for \( i \in \{0, 1, 2, 3, 4\} \). Thus, all transition patterns on wires \( k-1, k, \) and \( k+1 \) can be divided into five classes \( iC \) for \( i \in \{0, 1, 2, 3, 4\} \) according to their corresponding \( i \) (this classification was also used in [8]). By limiting transition patterns over the bus, the worst delay can be reduced. Various crosstalk avoidance codes (CACs) (see, for example, [8–11]) have been proposed based on this model.

Unfortunately, the model in [7] has limited accuracy for the following reasons. To achieve simplicity, only three wires are considered in the derivation of the model. In a bus with more than three wires, the simulated wire delay for \( OC \) transition patterns is much larger than \( \tau_0 \), the delay of \( OC \) given by (1). For example, the scheme to achieve a delay of \( \tau_0 \) in [12] would be ineffective. Furthermore, the Elmore delay, which tends to overestimate the delay [13], is used in the derivation. This is also verified by our simulation results.

In this paper we propose analytical delay models for coupled interconnects with improved accuracy. Based on a distributed RC model, we first derive closed-form expressions of the signals on the bus. Then we approximate the wire delays by evaluating these closed-form expressions. Our delay models differ from the model in [7] in two aspects. First, we use direct evaluations other than the Elmore delay in the model in [7] to approximate the delays. Second, we consider either three wires or five wires in our delay models for improved accuracy. Thus, our models achieve improved accuracy than the model in [7]. Since our delay models use the same classification as the model in [7], they also maintain the simplicity of the model in [7]. Hence, it is easy and conducive to use...
our delay models for the CAC designs. Also, our five-wire model can be applied to buses of any number of wires. Our extensive simulation results show that our delay models have improved accuracy than the model in [7].

2. DELAY MODEL

In this section, we first introduce the system model based on a distributed RC model. Then we propose delay models based on three-wire and five-wire buses, respectively.

2.1. System model

The on-chip buses are often approximated by the distributed RC model [14]. Our delay models do not consider the effects of inductance for two reasons. First, it is difficult to derive a closed-form expression of the signals on the bus based on the RLC model. More importantly, according to the criteria in [15], the inductance effects are negligible for buses with length in some range. This conclusion was also confirmed by other works: the 16b, 32Gb/s, 5mm-long bus and 8b, 16Gb/s, 10mm-long bus in [16] show that the distributed RC model is still accurate to characterize these high-speed long interconnects from 5mm to 10mm. So we use distributed RC model in our derivation for delay models.

In this paper our models do not account for the source resistance and load capacitance. However, they can be readily modified to account for both using the techniques in [17]. In general, source resistance and load capacitance tend to increase the delay. Since the crosstalk delay on the bus is the major part of the whole delay, the delays introduced by other parts are ignored. For this reason, no buffer is used. We assume that ideal step signals are applied on the bus directly.

According to [5], the closed-form expressions of the signals on the bus via a distributed RC model are sums of infinite terms. It was shown in [17] that sums of the two most significant terms provide a very close approximation of signals on the bus. This technique is crucial for the evaluation of the closed-form expressions.

The distributed RC model of an $m$-wire bus is shown in Fig. 1, where $V_i(x, t)$ denotes the transient signal at a position $x$ along wire $i$ for $i \in \{1, 2, \cdots, m\}$, $r$ and $c$ denote the resistance and capacitance per unit length, respectively. Also, $\lambda c$ denotes the coupling capacitance per unit length between two adjacent wires. In this work, we focus on a uniformly distributed bus and hence assume the parameters $r$, $c$, and $\lambda$ are the same for all wires.

Our models are based on the 50% delay, which is defined as the time difference between the respective instants when the input signal and corresponding output signal cross 50% of the supply voltage $V_{dd}$. In this paper, we focus on worst-case patterns leading to the largest 50% delay of the middle wire(s). For some transition patterns, the delay of the middle wire(s) is the greatest among all wires. For other transition patterns, other wires may have a greater delay, but the worst delays of all wires within the same class are close. Hence, our model can also be applied to other wires so as to approximate their delays with high accuracy. For simplicity, we assume $m$ is odd, and hence wire $\frac{m+1}{2}$ is the middle wire. We use $T_{m/2}$ to denote the worst delay of the middle wire (wire $\frac{m+1}{2}$) of an $m$-wire bus for all $iC$ patterns.

We first investigate the case $m = 3$ and then extend our results to the case $m = 5$. There are two reasons for studying the three-wire model. First and foremost, the three-wire model is the foundation of the derivation of our five-wire model. Second, our three-model shows higher accuracy than our five-wire model for buses with only three wires, which are used in partial coding schemes (see, e.g., [8–10]).

2.2. Three-wire model

Based on the same technique in [17], the differential equations characterizing a three-wire bus with length $L$ are given by:

$$\frac{\partial^2}{\partial x^2} V(x, t) = RC \frac{\partial}{\partial t} V(x, t),$$

(2)

where $V(x, t) = [V_1(x, t), V_2(x, t), V_3(x, t)]^T$ and $V_i(x, t)$ denotes the voltage of wire $i$ at distance $x (0 \leq x \leq L)$ at time $t$ for $i = 1, 2, 3$, $R = \begin{bmatrix} r & 0 & 0 \\ 0 & r & 0 \\ 0 & 0 & r \end{bmatrix}$, and $C = \begin{bmatrix} c + \lambda c & -\lambda c & 0 \\ -\lambda c & c + 2\lambda c & -\lambda c \\ 0 & -\lambda c & c + \lambda c \end{bmatrix}$.

The three eigenvalues of $C$ are given by $p_1 = c$, $p_2 = (1+\lambda)c$, and $p_3 = (1+3\lambda)c$, and their respective eigenvectors $e_i$’s are $[1 \ 1 \ 1]^T$, $[1 \ 0 \ -1]^T$, and $[-1 \ 2 \ -1]^T$. Hence, Eq. (2) is transformed to

$$\frac{\partial^2}{\partial x^2} U_i(x, t) = r p_i \frac{\partial}{\partial t} U_i(x, t) \text{ for } i = 1, 2, 3,$$

(3)

where $U_i(x, t) = V^T(x, t) e_i$ for $i = 1, 2, 3$. So $U_1(x, t) = V_1(x, t) + V_2(x, t) + V_3(x, t)$, $U_2(x, t) = V_1(x, t) - V_2(x, t)$, and $U_3(x, t) = 2V_2(x, t) - V_1(x, t) - V_3(x, t)$.

Applying Laplace transform on Eq. (3), we have

$$\frac{\partial^2}{\partial x^2} U_i(x, s) = r p_i \left[ s U_i(x, s) - U_i(x, 0) \right] \text{ for } i = 1, 2, 3.$$

(4)
Using appropriate initial conditions, we solve Eq. (4) for \( U_i(x,t) \) and obtain \( V_2(L,t) = \frac{1}{2}[U_1(L,t) + U_3(L,t)] \). By solving \( V_2(L,t) = 0.5V_{dd} \), we can approximate the 50% delay of a three-wire bus for different transition patterns.

The expressions of wire 2 are given by \( V_2(L,t) = 1 - a_1e^{-\frac{2}{\lambda}t} - a_2e^{-\frac{3}{\lambda}t} \), where \( a_i, i = 1, 2 \) are constant coefficients, and \( \tau = \frac{8}{\pi^2} \tau_0 \). We use “↑” to denote a transition from 0 to the supply voltage \( V_{dd} \) (normalized to 1), “↓” no transition, and “↑” a transition from \( V_{dd} \) to 0. We first identify the worst-case patterns in all classes through simulations, which are shown in Tab. 1. The expressions of wire 2 and the approximate delays of all classes are also shown in Tab. 1, respectively.

2.3. Five-wire model

To further improve the accuracy of delay, we include two extra adjacent wires and consider the influences of all five wires to approximate the delays. There are three kinds of transition: ↑, ↓, and ⇑ for each wire. Thus, for such a five-wire bus, there are \( 3^5 \) transition patterns. To maintain the simplicity of our models, we still categorize them into five classes (\( 5C, i \in \{0, 1, 2, 3, 4\} \)) based on the transition patterns of middle three wires (wires 2, 3, and 4). Hence, there are nine different transition patterns for each pattern of the same class.

Since the bus is a linear system, any pattern could be decomposed into a combination of patterns with single transition. Then the expression of the middle wire equals the sums of expressions of all individual wires on the middle wire. However, this would lead to complicated expressions, which are not easy to solve. We propose to group these individual wires to form some special patterns, reducible transition patterns (RTPs) and single transition patterns (STPs), which are easy to analyze.

An RTP is defined as a transition pattern in the five-wire model which can be reduced to a transition pattern in the three-wire model. \{↑↑↑↑↑, ↑↑↑↑↑, ↑↑↑↑↑, ↑↑↑↑↑, ↑↑↑↑↑\} is the set of RTPs for the five-wire model. For the transition ↑↑↑↑ (similarly for ↓↓↓↓), the expression of wire 3 is approximated by \( V_3(L,t) = 1 - a_1e^{-\frac{2}{\lambda}t} - a_2e^{-\frac{3}{\lambda}t} - a_3e^{-\frac{4}{\lambda}t} - a_4e^{-\frac{5}{\lambda}t} \), and the delay is approximated by \( \tau_3 = \frac{8}{\pi^2} \tau_0 \).

An STP is defined to be a transition pattern with transitions on only one wire in the five-wire model. For our five-wire model, we focus on the set of STPs with transitions on wire 2 or 4, \{↑↑↑↑↑, ↓↓↓↓, ↑↑↑↑↑, ↑↑↑↑↑, ↑↑↑↑↑\}.

The expressions of wire 3 can be approximated by our three-wire model. Set \( \mathcal{L}_j(x,t) \) denote the signal on wire \( j \) due to coupling from wire \( i \). For example, by ignoring coupling from wires 4 and 5 in ↑↑↑↑↑, the output of wire 3 is approximated by \( V_3(L,t) = 1 + \frac{1}{8\pi^2}e^{-\frac{2}{\lambda}t} - \frac{1}{8\pi^2}e^{-\frac{3}{\lambda}t} \), which is obtained by our three-wire model.

We propose the following approaches to derive the delay of the five-wire bus.

(1) We first decompose the worst-case pattern in each class into a combination of an RTP and STP(s).

(2) Then we combine the expressions of the RTP and STP(s) for the middle wire based on our three-wire model.

(3) Finally, we evaluate the expression of the middle wire to approximate its delay.

Since the performance is limited by the worst delay in each class, we only need to approximate the delays of the worst-case patterns in all classes. For classes \( 0C-4C \), we use simulations to identify the worst-case patterns, which are given by \( \scriptstyle\mathcal{L}_{↑↑↑↑↑}, \mathcal{L}_{↓↓↓↓}, \mathcal{L}_{↑↑↑↑↑}, \mathcal{L}_{↑↑↑↑↑}, \text{ and } \mathcal{L}_{↑↑↑↑↑} \), respectively (assuming the middle wire has an upward transition). With RTPs and STPs, we decompose the worst-case pattern in each class as shown in Tab. 2.

The expressions of wire 3 are given by \( V_3(L,t) = 1 - a_1e^{-\frac{2}{\lambda}t} - a_2e^{-\frac{3}{\lambda}t} - a_3e^{-\frac{4}{\lambda}t} - a_4e^{-\frac{5}{\lambda}t} \).
3. PERFORMANCE EVALUATION

To evaluate the performance of our models and compare them with the model in [7], we consider following three scenarios.

First, we focus on three-wire and five-wire buses, where our models are originally derived. This scenario can also be applied to partial coding schemes (see, e.g., [8–10]), where a wide bus is divided into sub-buses with a few wires. Then we consider buses with more than five wires and run extensive simulations with an odd number of wires (up to 33 wires). For brevity, only simulation results for a 17-wire bus are presented.

In the first two scenarios, we only focus on the worst delays of middle wires. In the third scenario, we assume the transition patterns are limited to three families of CACs and consider the worst delays for all wires of a 17-wire bus.

The simulation results are obtained by HSPICE. The coupling factor \( \lambda \) depends on the layer for routing the interconnect, the layer for the ground, the width for each wire, and the space between adjacent wires. We adopt a 0.1 \( \mu \)m process and route the global interconnects in the top metal layer. The bulk capacitance is considered from top metal layer to the substrate, with \( \lambda = 10 \). For the 0.1 \( \mu \)m process, the parasitic parameters are given by [18], and the parameter \( \tau_0 = \frac{t_{0H}}{\lambda} \) for a 5mm long bus is approximately 3.75ps. Though this process is somewhat outdated, we have also tried other process technologies with different values for \( \lambda \) and \( \tau_0 \) such as 45nm technology [19]. For all process technologies, our delay models can be easily adapted and show better accuracy than the model in [7].

### 3.1. Three-wire and five-wire buses

For a three-wire bus, we compare the simulated delays with the delays given by our model and the model in [7] for all classes in Tab. 4, where \( T_d \) denotes the simulated worst delay of wire 2, \( T_3^{\text{ve}} \) the approximate delay for \( iC \) pattern by our three-wire model, and \( T_2 \) by the model in [7]. The error percentages of our model and the model in [7] for each class are also included in Tab. 4. For all five classes of transition patterns in a three-wire bus, the maximum and minimum errors by our model are 1.05% and 0.34%, respectively, as opposed to 726.65% and 30.66% by the model in [7], respectively. As shown in Tab. 4, our three-wire model is much more accurate than the model in [7] for all patterns in a three-wire bus. We remark that the delay of a 1C pattern by our model, \( \ln \frac{3\lambda}{\pi} \tau \), does not depend on \( \lambda \).

For a five-wire bus, we compare the simulated delays with the delays given by our five-wire model and the model in [7] for all classes in Tab. 5, where \( T_d \) denotes the simulated worst delay of wire 3 for all \( iC \) patterns, \( T_3^{\text{ve}} \) the approximate delay for \( iC \) pattern by our five-wire model, and \( T_3 \) by the model in [7]. For a five-wire bus, the maximum and minimum errors by our model are 17.68% and 0.53%, respectively, compared to 83.91% and 10.24% by the model in [7], respectively. As shown in Tab. 5, our five-wire model is more accurate than the model in [7] for all patterns in a five-wire bus. Particularly, we observe that the worst delay for the \( 0C \) patterns are much larger than that given by the model in [7].

\[
a_1 e^{-\frac{\lambda}{\pi} \tau} - a_2 e^{-\frac{\lambda}{\pi} \tau} - a_3 e^{-\frac{\lambda}{\pi} \tau}, \quad \text{where } a_i, i = 1, 2, 3 \text{ are constant coefficients.}
\]

For all worst-case patterns in a five-wire bus, the expressions of wire 3 and the approximate delays are shown in Tab. 5, respectively.

### Table 4. Comparison of simulated delays, our three-wire model, and the model in [7] (\( \tau_0 = 3.75ps, \tau = \frac{2\lambda}{\pi} \tau_0, \text{ and } \lambda = 10 \))

| \( iC \) | Worst-case patterns | Sim. \( T_d \) \( (\text{ps}) \) | Our three-wire model \( T_3^{\text{ve}} \) \( (\text{ps}) \) | [7] \( T_3 \) in \( (1) \) \( (\text{ps}) \) | \( \frac{T_3 - T_d}{T_d} \) |
|---|---|---|---|---|---|
| 0C | \( \uparrow \uparrow \uparrow \) | 2.87 \( (\ln \frac{\lambda}{\pi} \tau) \) | 2.84 \( 1.05\% \) | \( r_0 \) 3.75 | 30.66% |
| 1C | \( \uparrow \uparrow \) | 4.99 \( (\ln \frac{\lambda}{\pi} \tau) \) | 4.94 \( 1.00\% \) | \( (1 + \lambda) r_0 \) 41.25 | 726.65% |
| 2C | \( \uparrow \downarrow \) | 49.70 \( (\ln \frac{\lambda}{\pi} \tau) \) | 49.87 \( 0.34\% \) | \( (1 + 2\lambda) r_0 \) 78.75 | 58.45% |
| 3C | \( \uparrow \uparrow \uparrow \) | 88.61 \( (\ln \frac{\lambda}{\pi} \tau) \) | 88.08 \( 0.60\% \) | \( (1 + 3\lambda) r_0 \) 116.25 | 31.19% |
| 4C | \( \uparrow \uparrow \downarrow \) | 115.89 \( (\ln \frac{\lambda}{\pi} \tau) \) | 115.18 \( 0.61\% \) | \( (1 + 4\lambda) r_0 \) 153.75 | 32.67% |

### Table 5. Comparison of simulated delays, our five-wire model, and the model in [7] (\( \tau_0 = 3.75ps, \tau = \frac{2\lambda}{\pi} \tau_0, \text{ and } \lambda = 10 \))

| \( iC \) | Worst-case patterns | Sim. \( T_d \) \( (\text{ps}) \) | Our five-wire model \( T_5^{\text{ve}} \) \( (\text{ps}) \) | [7] \( T_3 \) in \( (1) \) \( (\text{ps}) \) | \( \frac{T_3 - T_d}{T_d} \) |
|---|---|---|---|---|---|
| 0C | \( \downarrow \downarrow \downarrow \) | 23.30 | 0.165(1 + 3\( \lambda \))\( \tau \) | 19.18 \( 17.68\% \) | \( r_0 \) 3.75 | 83.91% |
| 1C | \( \downarrow \downarrow \uparrow \) | 37.42 | 0.310(1 + 3\( \lambda \))\( \tau \) | 34.99 \( 6.49\% \) | \( (1 + \lambda) r_0 \) 41.25 | 10.24% |
| 2C | \( \downarrow \uparrow \downarrow \) | 56.58 \( (\ln \frac{\lambda}{\pi} \tau) \) | 59.46 \( 5.09\% \) | \( (1 + 2\lambda) r_0 \) 78.75 | 39.18% |
| 3C | \( \uparrow \uparrow \uparrow \downarrow \) | 88.55 \( (\ln \frac{\lambda}{\pi} \tau) \) | 88.08 \( 0.53\% \) | \( (1 + 3\lambda) r_0 \) 116.25 | 31.28% |
| 4C | \( \uparrow \uparrow \uparrow \downarrow \) | 127.29 \( (\ln \frac{\lambda}{\pi} \tau) \) | 115.18 \( 9.51\% \) | \( (1 + 4\lambda) r_0 \) 153.75 | 20.79% |
Table 6. Comparison of simulated delays and delays given by our five-wire model and the model in [7] for wire 9 in a 17-wire bus ($\tau_0 = 3.75\text{ps}$, $\tau = \frac{8}{5}\tau_0$, and $\lambda = 10$). All delays are in ps.

| $iC$ | Worst-case patterns with respect to our assumptions | Sim. $T_d$ | Our model $T_d^{5C}$ | $|T_d^{5C} - T_d| / T_d$ | [7] $T_d$ | $|T_d^{5C} - T_d|$ |
|------|--------------------------------------------------|-----------|----------------|-----------------|----------|----------------|
| $0C$ | ↑↑↑↑↑↓↓↓↓↑↑↑↓↑↑↑↓↑↑↑↓↑↑↑↓ ↑↑↑↑ | 25.07 | 19.18 | 23.49% | 3.75 | 85.04% |
| $1C$ | ↑↑↑↑↑↓↓↓↓↑↑↑↓↑↑↑↓↑↑↑↓↑↑↑↓ ↑↑↑ | 39.13 | 34.99 | 10.58% | 41.25 | 8.42% |
| $2C$ | ↓↓↑↑↓ (-↑- ↓↑↑↓↑↑↑↓↑↑↑↓↑↑↑↓ ↑↑ | 65.93 | 59.46 | 9.81% | 78.75 | 19.44% |
| $3C$ | ↓↓↑↑↓ (-↑- ↓↑↑↓↑↑↑↓↑↑↑↓↑↑↑↓ ↑↑ | 95.39 | 88.08 | 7.66% | 116.25 | 21.87% |
| $4C$ | ↑↑↑↑↑↓↓↓↓↑↑↑↓↑↑↑↓↑↑↑↓↑↑↑↓ ↑↑↑↓ | 130.43 | 115.18 | 11.69% | 153.75 | 17.88% |

Table 7. Comparison of simulated delays and delays given by our five-wire model and the model in [7] for all wire in a 17-wire bus ($\tau_0 = 3.75\text{ps}$, $\tau = \frac{8}{5}\tau_0$, and $\lambda = 10$). All delays are in ps.

| Delays | OLC | FPC | FOC |
|--------|-----|-----|-----|
| [7]    |     |     |     |
| $T_d^{5C}$ | 34.99 | 59.46 | 88.08 |
| Wire $i$ | |
| 1      | 33.96 | 64.31 | 63.00 |
| 2      | 21.59 | 62.52 | 95.06 |
| 3      | 32.37 | 63.73 | 94.90 |
| 4      | 32.40 | 62.14 | 96.56 |
| 5      | 32.16 | 63.40 | 94.30 |
| 6      | 32.49 | 64.63 | 96.99 |
| 7      | 32.55 | 65.00 | 93.69 |
| 8      | 32.50 | 62.26 | 93.31 |
| 9      | 33.18 | 60.74 | 94.93 |
| 10     | 33.27 | 62.21 | 95.94 |
| 11     | 31.92 | 61.10 | 94.74 |
| 12     | 32.07 | 61.55 | 94.33 |
| 13     | 32.02 | 63.31 | 96.56 |
| 14     | 32.97 | 60.22 | 97.24 |
| 15     | 32.83 | 64.70 | 92.01 |
| 16     | 31.61 | 63.52 | 95.29 |
| 17     | 33.61 | 63.52 | 96.83 |

3.2. 17-wire bus

We next compare our five-wire model with the model in [7] for a 17-wire bus. We still focus on the middle wire (wire 9) in the 17-wire bus and identify the worst-case patterns in all classes through simulations. The transition patterns are categorized by the transitions of the middle three wires (wires 8, 9, and 10). Since there are $3^{14}$ transition patterns in each class, it is infeasible to search all transitions to identify the pattern with the longest delay. For any two wires symmetric to wire 9 (wire $i$ and wire $18-i$, $i \in \{1, 2, \ldots, 8\}$), there are nine possible patterns, $\uparrow\uparrow$, $\downarrow\downarrow$, $\rightarrow\rightarrow$, $\leftarrow\leftarrow$, $\uparrow\downarrow$, $\uparrow\rightarrow$, $\downarrow\uparrow$, $\downarrow\leftarrow$, and $\rightarrow\leftarrow$. If the transitions on the two symmetric wires are in opposite direction, we assume the influences of the two transitions will cancel out as a result of symmetry. For other patterns, we assume $\uparrow\uparrow$ has greater influence than $\uparrow$ or $\rightarrow$. Similarly, $\downarrow\downarrow$ has greater influence than $\downarrow$ or $\rightarrow$. Based on the discussion above, we assume the longest delay happens when two symmetric wires have either $\uparrow\uparrow$ or $\downarrow\downarrow$ transitions. So there are only $2^7 = 128$ patterns left to check in each class.

To find the worst-case patterns, we search all possible symmetric transition patterns in each class. The worst-case patterns are listed in the second column of Tab. 6, where the pattern on wires 8, 9, and 10 is shown in the parenthesis. We compare the simulated worst delays with the delays given by our five-wire model and the model in [7] for all classes in Tab. 6, where $T_d$ denotes the simulated worst delay of wire 9 for all $iC$ patterns, $T_d^{5C}$ the approximate delay for $iC$ pattern by our five-wire model, and $T_d$ by the model in [7]. For all five classes, the maximum and minimum errors by our model are 23.49% and 7.66%, respectively, as opposed to 85.04% and 5.42% by the model in [7], respectively. For all classes except $1C$, our five-wire model outperforms the model in [7]. The model in [7] also shows a large error percentage for $0C$. We have also tried other buses with odd number of wires up to 33. Based on the simulation results, we conjecture that our five-wire model would be more accurate than the model in [7] for buses with any number of wires.

3.3. Performance of CACs

In the simulation results above, we only focus on the middle wire of a 17-wire bus. Now we evaluate the delays on all wires of a 17-wire bus for three families of CACs [8–10]: one Lambda codes (OLCs), forbidden pattern codes (FPCs), and forbidden overlap codes (FOCs). Based on our five-wire model, the worst delays of aforementioned CACs are given by $0.310(1 + 3\lambda)\tau$, $(\ln \frac{1}{\tau_0}) (1 + \frac{3}{2}\lambda) \tau$, and $(\ln \frac{1}{\tau_0}) (1 + 3\lambda)\tau$, respectively. Based on the model in [7], the worst delays of aforementioned CACs are given by $(1 + \lambda)\tau_0$, $(1 + 2\lambda)\tau_0$, and $(1 + 3\lambda)\tau_0$, respectively. For each CAC, 1000 codewords from the code book are randomly chosen and transmitted over a 17-wire bus consecutively, thus forming 999 transitions. We compare the simulated worst delays of each wire and the delays given by our five-wire model and the model in [7], respectively, in Tab. 7. For the OLC, the FPC, and the FOC in a 17-wire bus, the largest delays are emphasized in boldface. As shown in Tab. 7, our five-wire model is more accurate than the model in [7] for all three families of CACs. Also, in [20], a new CAC with a smaller worst delay than an OLC has been
proposed based on our five-wire model and a new classification of transition patterns. It shows that our five-wire model enables the design of more effective CACs.

4. CONCLUSIONS AND FUTURE WORK

In this work we propose improved analytical delay models for coupled interconnects, based on the distributed RC model. First the closed-form expressions of the signals on three-wire and five-wire buses are derived, which are also motivated by partial coding schemes. Then delays corresponding to different patterns are approximated by evaluating the closed-form expressions. The simulation results show that our models have better accuracy than that in [7]. Although our models are based on three-wire and five-wire buses, they can also be employed for a bus with more than five wires. Our simulation results also show that our five-wire model could still approximate delays better than the model in [7] for a general bus.

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