TBD: Benchmarking and Analyzing Deep Neural Network Training

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Abstract

The recent popularity of deep neural networks (DNNs) has generated a lot of research interest in performing DNN-related computation efficiently. However, the primary focus is usually very narrow and limited to (i) inference – i.e. how to efficiently execute already trained models and (ii) image classification networks as the primary benchmark for evaluation.

Our primary goal in this work is to break this myopic view by (i) proposing a new benchmark for DNN training, called TBD\textsuperscript{1}, that uses a representative set of DNN models that cover a wide range of machine learning applications: image classification, machine translation, speech recognition, object detection, adversarial networks, reinforcement learning, and (ii) by performing an extensive performance analysis of training these different applications on three major deep learning frameworks (TensorFlow, MXNet, CNTK) across different hardware configurations (single-GPU, multi-GPU, and multi-machine). TBD currently covers six major application domains and eight different state-of-the-art models.

We present a new toolchain for performance analysis for these models that combines the targeted usage of existing performance analysis tools, careful selection of new and existing metrics and methodologies to analyze the results, and utilization of domain specific characteristics of DNN training. We also build a new set of tools for memory profiling in all three major frameworks; much needed tools that can finally shed some light on precisely how much memory is consumed by different data structures (weights, activations, gradients, workspace) in DNN training. By using our tools and methodologies, we make several important observations and recommendations on where the future research and optimization of DNN training should be focused.

\textsuperscript{1}TBD is short for Training Benchmark for DNNs
Table 1: The table above shows a categorization of major computer architecture and systems conference papers (SOSP, OSDI, NSDI, MICRO, ISCA, HPCA, ASPLOS) since 2014. These papers are grouped by their focus along two dimensions: Training versus Inference and Algorithmic Breadth. There are more papers which optimize inference over training (25 vs. 16, 4 papers aim for both training and inference). Similarly more papers use image classification as the only application for evaluation (26 vs. 11).

### Introduction

The availability of large datasets and powerful computing resources has enabled a new type of artificial neural networks—deep neural networks (DNNs)—to solve hard problems such as image classification, machine translation, and speech processing. While this recent success of DNN-based learning algorithms has naturally attracted a lot of attention, the primary focus of researchers especially in the systems and computer architecture communities is usually on inference—i.e. how to efficiently execute already trained models, and image classification (which is used as the primary benchmark to evaluate DNN computation efficiency).

While inference is arguably an important problem, we observe that efficiently training new models is becoming equally important as machine learning is applied to an ever growing number of domains, e.g., speech recognition, machine translation, automobile industry, and recommendation systems. But researchers currently lack comprehensive benchmarks and profiling tools for DNN training. In this paper, we present a new benchmark for DNN training, called TBD, that uses a representative set of DNN models covering a broad range of machine learning applications: image classification, machine translation, speech recognition, adversarial networks, reinforcement learning. TBD also incorporates an analysis toolchain for performing detailed resource and performance profiling of these models, including the first publicly available tool for profiling memory usage on major DNN frameworks. Using TBD we perform a detailed performance analysis on how these different applications behave on three DNN training frameworks (TensorFlow, MXNet, CNTK) across different hardware configurations (single-GPU, multi-GPU, and multi-machine) gaining some interesting insights.

TBD’s benchmark suite and analysis toolchain is driven by the motivation to address three main challenges:

1. **Training differs significantly from inference.** The algorithmic differ-
ences between training and inference lead to many differences in requirements for the underlying systems and hardware architecture. First, \textit{backward pass} and \textit{weight updates}, operations unique to training, need to save/stash a large number of intermediate results in GPU memory, e.g., outputs of the inner layers called \textit{feature maps} or activations \cite{83}. This puts significant pressure on the memory subsystem of modern DNN accelerators (usually GPUs) – in some cases the model might need tens of gigabytes of main memory \cite{83}. In contrast, the memory footprint of inference is significantly smaller, in the order of tens of megabytes \cite{47}, and the major memory consumers are model weights rather than feature maps. Second, training usually proceeds in waves of \textit{mini-batches}, a set of inputs grouped and processed in parallel \cite{43, 101}. Mini-batching helps in avoiding both overfitting and under utilization of GPU’s compute parallelism. Thus, throughput is the primary performance metric of concern in training. Compared to training, inference is computationally less taxing and is latency sensitive.

2. \textbf{Workload diversity.} Deep learning has achieved state-of-the-art results in a very broad range of application domains. Yet most existing evaluations of DNN performance remain narrowly focused on just image classification as their benchmark application, and convolutional neural networks (CNNs) remain the most widely-used models for systems/architecture researchers (Table 1). As a result, many important non-CNN models have not received much attention, with only a handful of papers evaluating non-CNNs such as recurrent neural networks \cite{10, 60, 51}. Papers that cover unsupervised learning or deep reinforcement learning are extremely rare. The computational characteristics of image classification models are very different from these networks, thus motivating a need for a broader benchmark suite for DNN training. Furthermore, given the rapid pace of innovation across the realms of algorithms, systems, and hardware related to deep learning, such benchmarks risk being quickly obsolete if they don’t change with time.

3. \textbf{Identifying bottlenecks.} It is not obvious which hardware resource is the critical bottleneck that typically limits training throughput, as there are multiple plausible candidates. Typical convolutional neural networks (CNNs) are usually computationally intensive, making \textit{computation} one of the primary bottlenecks in single GPU training. Efficiently using modern GPUs (or other hardware accelerators) requires training with large mini-batch sizes. Unfortunately, as we will show later in Section 4.2 for some workloads (e.g., RNNs, LSTMs) this requirement can not be satisfied due to capacity limitations of GPU \textit{main memory} (usually 8–16GBs). Training DNNs in a distributed environment with multiple GPUs and multiple machines, brings with it yet another group of potential bottlenecks, \textit{network and interconnect bandwidths}, as training requires fast communication between many CPUs and GPUs (see Section 4.5). Even for a specific model, implementation and hardware setup pinpointing whether performance is bounded by computation, memory, or communication is not easy due to limitations of existing profiling tools. Commonly used tools (e.g., vTune \cite{80}, nvprof \cite{9}, etc.) have no domain-specific knowledge about the algorithm logic, can only capture some low-level information within their own scopes, and usu-
ally cannot perform analysis on full application executions with huge working set sizes. Furthermore, no tools for memory profiling are currently available for any of the major DNN frameworks.

Our paper makes the following contributions.

- **TBD, a new benchmark suite.** We create a new benchmark suite for DNN training that currently covers six major application domains and eight different state-of-the-art models. The applications in this suite are selected based on extensive conversations with ML developers and users from both industry and academia. For all application domains we select recent models capable of delivering state-of-the-art results. We will open-source our benchmarks suite later this year and intend to continually expand it with new applications and models based on feedback and support from the community.

- **Tools to enable end-to-end performance analysis.** We develop a toolchain for end-to-end analysis of DNN training. To perform such analysis, we perform piecewise profiling by targeting specific parts of training using existing performance analysis tools, and then merge and analyze them using domain-specific knowledge of DNN training. As part of the toolchain we also built new memory profiling tools for the three major DNN frameworks we considered: TensorFlow [10], MXNet [24], and CNTK [102]. Our memory profilers can pinpoint how much memory is consumed by different data structures during training (weights, activations, gradients, workspace etc.), thus enabling developer to make easy data-driven decisions for memory optimizations.

- **Findings and Recommendations.** Using our benchmark suite and analysis tools, we make several important observations and recommendations on where the future research and optimization of DNNs should be focused. We include a few examples here: (1) We find that the training of state-of-the-art RNN models is not as efficient as for image classification models, because GPU utilization for RNN models is 2–3× lower than for most other benchmark models. (2) We find that GPU memory is often not utilized efficiently, the strategy of exhausting GPU memory capacity with large mini-batch provides limited benefits for a wide range of models. (3) We also find that the feature maps, the output of the DNN intermediate layers, consume 70–90% of the total memory footprint for all our benchmark models. This is a significant contrast to inference, where footprint is dominated by the weights. These observations suggest several interesting research directions, including efficient RNN layer implementations and memory footprint reduction optimizations with the focus on feature maps.

The TBD benchmark suite and the accompanying measurement toolchain, and insights derived from them will aid researchers and practitioners in computer systems, computer architecture, and machine learning to determine where
to target their optimizations efforts within each level in the DNN training stack: (i) applications and their corresponding models, (ii) currently used libraries (e.g., cuDNN), and (iii) hardware that is used to train these models. We also hope that our paper will instigate additional follow-up work within the Sigmetrics community aimed at providing DNN research with a more rigorous foundation rooted in measurements and benchmarking.

In the rest of this paper, we first provide some background on DNN training, both single-GPU and distributed training (with multiple GPUs and multiple machines) in Section 2. We then present our methodology, explaining which DNN models we selected to be included in our benchmark suite and why, and describing our measurement framework and tools to analyze the performance of these models (Section 3). We then use our benchmark and measurement framework to derive observations and insights about these models’ performance and resource characteristics in Section 4. We conclude the paper with a description of related work in Section 5 and a summary of our work in Section 6.

2 Background

2.1 Deep Neural Network Training and Inference

A neural network can be seen as a function which takes data samples as inputs, and outputs certain properties of the input samples (Figure 1). Neural networks are made up of a series of layers of neurons. Neurons across layers are connected, and layers can be of different types such as fully-connected, convolutional, pooling, recurrent, etc. While the edges connecting neurons across layers are weighted, each layer can be considered to have its own set of weights. Each layer applies a mathematical transformation to its input. For example, a fully-connected layer multiplies intermediate results computed by its preceding/upstream layer (input) by its weight matrix, adds a bias vector, and applies a non-linear function (e.g., sigmoid) to the result; this result is then used as the input to its following/downstream layer. The intermediate results generated by each layer are often called feature maps. Feature maps closer to the output layer generally represent higher order features of the data samples. This entire layer-wise computation procedure from input data samples to output is called inference.

A neural network needs to be trained before it can detect meaningful properties corresponding to input data samples. The goal of training is to find proper weight values for each layer so that the network as a whole can produce desired outputs. Training a neural network is an iterative algorithm, where each iteration consists of a forward pass and a backward pass. The forward pass is computationally similar to inference. For a network that is not fully trained, the inference results might be very different from ground truths labels. A loss function measures the difference between the predicted value in the forward pass and the ground truth. Similar to the forward pass, computation in the backward pass also proceeds layer-wise, but in an opposite direction. Each layer
uses errors from its downstream layers and feature maps generated in the forward pass to compute not only errors to its upstream layers according to the chain rule [84] but also gradients of its internal weights. The gradients are then used for updating the weights. This process is known as the gradient descent algorithm, used widely to train neural networks.

As modern training dataset are extremely large, it is expensive to use the entire set of the training data in each iteration. Instead, a training iteration randomly samples a mini-batch from the training data, and uses this mini-batch as input. The randomly sampled mini-batch is a stochastic approximation to the full batch. This algorithm is called stochastic gradient descent (SGD) [64]. The size of the mini-batch is a crucial parameter which greatly affects both the training performance and the memory footprint.

2.2 GPUs and Distributed Training via Data Parallelism

While the theoretical foundations of neural networks have a long history, it is only relatively recently the people realized the power of deep neural networks. This is because to fully train a neural network on a CPU is extremely time-consuming [89]. The first successful deep neural network [63] that beat all competitors in image classification task in 2012, was trained using two GTX 580 GPUs [8] in six days instead of months of training on CPUs. One factor that greatly limits the size of the network is the amount of tolerable training time. Since then, almost all advanced deep learning models are trained using either GPUs or some other type of hardware accelerators [60], [44].

One way to further speed up the neural network training is to parallelize the training procedure and deploy the parallelized procedure in a distributed environment. A simple and effective way to do so is called data parallelism [30]. It lets each worker train a single network replica. In an iteration, the input mini-batch is partitioned into $n$ subsets, one for each worker. Each worker then takes this subset of the mini-batch, performs the forward and backward passes respectively, and exchanges weight updates with all other workers.

Another way to parallelize the computation is by using model parallelism [97],
an approach used when the model’s working set is too large to fit in the memory of a single worker. Model parallel training splits the workload of training a complete model across the workers; each worker trains only a part of the network. This approach requires careful workload partitioning to achieve even load-balancing and low communication overheads. The quality of workload partitioning in model parallelism depends highly on DNN architecture. Unlike model parallelism, data parallelism is simpler to get right and is the predominant method of parallel training. In this paper we limit our attention to data parallel distributed training.

2.3 DNN Frameworks and Low-level Libraries

DNN frameworks and low-level libraries are designed to simplify the life of ML programmers and to help them to efficiently utilize existing complex hardware. A DNN framework (e.g., TensorFlow or MXNet) usually provides users with compact numpy/matlab-like matrix APIs to define the computation logic, or a configuration format, that helps ML programmers to specify the topology of their DNNs layer-by-layer. The programming APIs are usually bounded with the popular high-level programming languages such as Python, Scala, and R. A framework transforms the user program or configuration file into an internal intermediate representation (e.g., dataflow graph representation [10, 24, 20]), which is a basis for backend execution including data transfers, memory allocations, and low-level CPU function calls or GPU kernel invocations. The invoked low-level functions are usually provided by libraries such as cuDNN [27], cuBLAS [4], MKL [96], and Eigen [6]. These libraries provide efficient implementations of basic vector and multi-dimension matrix operations (some operations are NN-specific such as convolutions or poolings) in C/C++ (for CPU) or CUDA (for GPU). The performance of these libraries will directly affect the overall training performance.

3 Methodology

3.1 Application and Model Selection

Based on a careful survey of existing literature and in-depth discussions with machine learning researchers and industry developers at several institutions (Google, Microsoft, and Nvidia) we identified a diverse set of interesting application domains, where deep learning has been emerging as the most promising solution: image classification, object detection, machine translation, speech recognition, generative adversarial nets, and deep reinforcement learning. While this is the set of applications we will include with the first release of our open-source benchmark suite, we expect to continuously expand it based on community feedback and contributions and to keep up with advances of deep learning in new application domains.

[A GPU kernel is a routine that is executed by an array of CUDA threads on GPU cores.]

7
| Application                  | Model        | Number of Layers | Dominant Layer | Frameworks                | Dataset               |
|-----------------------------|-------------|------------------|----------------|---------------------------|-----------------------|
| Image classification        | ResNet-50   | 50 (152 max)     | CONV           | TensorFlow, MXNet, CNTK   | ImageNet1K            |
|                            | Inception-v3| 42               |                |                          |                       |
| Machine translation         | Seq2Seq     | 5                | LSTM           | TensorFlow, MXNet        | IWSLT15               |
|                            | Transformer | 12               | Attention      | TensorFlow               |                       |
| Object detection            | Faster R-CNN| 101^a            | CONV           | TensorFlow, MXNet        | Pascal VOC 2007       |
|                            | Deep Speech 2 | 9^b              | RNN            | MXNet                    | LibriSpeech           |
| Speech recognition          | Deep Speech 2 | 9^b              | RNN            | MXNet                    | LibriSpeech           |
| Adversarial learning        | WGAN        | 14+14^c          | CONV           | TensorFlow               | Downsampled ImageNet  |
| Deep reinforcement learning | A3C         | 4                | CONV           | MXNet                    | Atari 2600            |

Table 2: Overview of Benchmarks, including the models and datasets used, number and major layer types, and frameworks with available implementations.

| Dataset                  | Number of Samples | Size                          | Special                                  |
|--------------------------|-------------------|-------------------------------|------------------------------------------|
| ImageNet1K               | 1.2million        | 3x256x256 per image           | N/A                                      |
| IWSLT15                  | 133k              | 20-30 words long per sentence | vocabulary size of 17188                 |
| Pascal VOC 2007          | 5011^d            | around 500x350                | 12608 annotated objects                 |
| LibriSpeech              | 280k              | 1000 hours^e                  | N/A                                      |
| Downsampled ImageNet     | 1.2million        | 3x64x64 per image             | N/A                                      |
| Atari 2600               | N/A               | 4x84x84 per image             | N/A                                      |

Table 3: Training Datasets
Table 2 summarizes the models and datasets we chose to represent the different application domains. When selecting the models, our emphasis has been on picking the most recent models capable of producing state-of-the-art results (rather than for example classical models of historical significance). The reasons are that these models are the most likely to serve as building blocks or inspiration for the development of future algorithms and also often use new types of layers, with new resource profiles, that are not present in older models. Moreover, the design of models is often constrained by hardware limitations, which will have changed since the introduction of older models.

### 3.1.1 Image Classification

Image classification is the archetypal deep learning application, as this was the first domain where a deep neural network (AlexNet [63]) proved to be a watershed, beating all prior traditional methods. In our work, we use two very recent models, Inception-v3 [92] and Resnet [52], which follow a structure similar to AlexNet’s CNN model, but improve accuracy through novel algorithm techniques that enable extremely deep networks.

### 3.1.2 Object Detection

Object detection applications, such as face detection, are another popular deep learning application and can be thought of as an extension of image classification, where an algorithm usually first breaks down an image into regions of interest and then applies image classification to each region. We choose to include Faster R-CNN [32], which achieves state-of-the-art results on the Pascal VOC datasets [41]. A training iteration consists of the forward and backward passes of two networks (one for identifying regions and one for classification), weight sharing and local fine-tuning. The convolution stack in a Faster R-CNN network is usually a standard image classification network, in our work a 101-layer ResNet.

In the future, we plan to add YOLO9000 [79], a network recently proposed for the real-time detection of objects, to our benchmark suite. It can perform inference faster than Faster R-CNN, however at the point of writing its accuracy is still lagging and its implementations on the various frameworks is not quite mature enough yet.

### 3.1.3 Machine Translation

Unlike image processing, machine translation involves the analysis of sequential data and typically relies on RNNs using LSTM cells as its core algorithm. We select NMT [98] and Sockeye [54], developed by the TensorFlow and Amazon Web Service teams, respectively, as representative RNN-based models in this area. We also include an implementation of the recently introduced Trans- former model, which achieves a new state-of-the-art in translation quality using attention layers as an alternative to recurrent layers.
3.1.4 Speech Recognition

Deep Speech 2 \cite{15} is an end-to-end speech recognition model from Baidu Research. It is able to accurately recognize both English and Mandarin Chinese, two very distant languages, with a unified model architecture and shows great potential for deployment in industry. The Deep Speech 2 model contains two convolutional layers, plus seven regular recurrent layers or Gate Recurrent Units (GRUs), different from the RNN models in machine translation included in our benchmark suite, which use LSTM layers.

3.1.5 Generative Adversarial Networks

A generative adversarial network (GAN) trains two networks, one generator network and one discriminator network. The generator is trained to generate data samples that mimic the real samples, and the discriminator is trained to distinguish whether a data sample is genuine or synthesized. GANs are used, for example, to synthetically generate photographs that look at least superficially authentic to human observers.

While GANs are powerful generative models, training a GAN suffers from instability. The WGAN \cite{17} is a milestone as it makes great progress towards stable training. Recently Gulrajani et al. \cite{45} proposes an improvement based on the WGAN to enable stable training on a wide range of GAN architectures. We include this model into our benchmark suite as it is one of the leading DNN algorithms in the unsupervised learning area.

3.1.6 Deep Reinforcement Learning

Deep neural networks are also responsible for recent advances in reinforcement learning, which have contributed to the creation of the first artificial agents to achieve human-level performance across challenging domains, such as the game of Go and various classical computer games. We include the A3C algorithm \cite{70} in our benchmark suite, as it has become one of the most popular deep reinforcement learning techniques, surpassing the DQN training algorithms \cite{71}, and works in both single and distributed machine settings. A3C relies on asynchronously updated policy and value function networks trained in parallel over several processing threads.

\footnote{aWe use the convolution stack of ResNet-101 to be the shared convolution stack between Region Proposal Network and the detection network.}

\footnote{bThe official Deep Speech 2 model has 2 convolutional layers plus 7 RNN layers. Due to memory issue, we use the default MXNet configuration which has 5 RNN layers instead.}

\footnote{cThe architecture for both the generator and discriminator of WGAN is a small CNN containing 4 residual blocks.}

\footnote{dWe use the train+val set of Pascal VOC 2007 dataset.}

\footnote{eThe entire LibriSpeech dataset consists of 3 subsets with 100 hours, 360 hours and 500 hours respectively. By default, the MXNet implementation uses the 100-hour subset as the training dataset.}
3.2 Framework Selection

There are many open-source DNN frameworks, such as TensorFlow [10], Theano [20], MXNet [24], CNTK [102], Caffe [59], Chainer [93], Torch [32], Keras [30], PyTorch [76]. Each of them applies some generic high-level optimizations (e.g., exploiting model parallelism using dataflow computation, overlapping computation with communication) and some unique optimizations of their own (e.g., different memory managers and memory allocation strategies, specific libraries to perform efficient computation of certain DNN layer types). Most of these frameworks share similar code structure, and provide either declarative or imperative high-level APIs. The computation of forward and backward passes is performed by either existing low-level libraries (e.g., cuBLAS, cuDNN, Eigen, MKL, etc.) or using their own implementations. For the same neural network model trained using different frameworks, the invoked GPU kernels (normally the major part of the computation) are usually functionally the same. This provides us with a basis to compare, select, and analyze the efficiency of different frameworks.

As there is not one single framework that has emerged as the dominant leader in the field and different framework-specific design choices and optimizations might lead to different results, we include several frameworks in our work. In particular, we choose TensorFlow [10], MXNet [24], and CNTK [102], as all three platforms have a large number of active users, are actively evolving, have many of the implementations for the models we were interested in and support hardware acceleration using single and multiple GPUs.

3.3 Training Benchmark Models

![Graphs showing model accuracy and training time for different models.](image)

(a) Inception-v3  
(b) ResNet-50  
(c) Transformer  
(d) Seq2Seq  
(e) A3C

Figure 2: The model accuracy during the training for different models.

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Note that implementing a model on a new framework from scratch is a highly complex task beyond the scope of our work. Hence in this paper we use the existing open-source implementations provided by either the framework developers on the official github repository, or third-party implementations when official versions are not available.
To ensure that the results we obtain from our measurements are representative, we need to verify that the training process for each model results in classification accuracy comparable to state of the art results published in the literature. To achieve this, we train the benchmark models in our suite until they converge to some expected accuracy rate (based on results from the literature).

Figure 2 shows the classification accuracy observed over time for five representative models in our benchmark suite, Inception-v3, ResNet-50, Seq2Seq, Transformer, and A3C, when trained on the single Quadro P4000 GPU hardware configuration described in Section 4.2. We observe that the training outcome of all models matches results in the literature. For the two image classification models (Inception-v3 and ResNet-50) the Top-1 classification accuracy reaches 75–80% and the the Top-5 accuracy is above 90%, both in agreement with previously reported results for these models [52]. The accuracy of the machine translation models is measured using the BLEU score [73] metric, and we trained our model to achieve a BLEU score of around 20. For reinforcement learning, since the models are generally evaluated by Atari games, the accuracy of the A3C model is directly reflected by the score of the corresponding game. The A3C curve we show in this figure is from the Atari Pong game and matches previously reported results for that game (19–20) [70]. The training curve shape for different implementations of the same model on different frameworks can vary, but most of them usually converge to similar accuracy at the end of training.

3.4 Performance Analysis Framework and Tools

In this section we describe our analysis toolchain. This toolchain is designed to help us understand for each of the benchmarks, where the training time goes, how well the hardware resources are utilized and how to efficiently improve training performance.

3.4.1 Making implementations comparable across frameworks

Implementations of the same model on different frameworks might vary in a few aspects that can impact performance profiling results. For example, different implementations might have hard-coded values for key hyper-parameters (e.g., learning rate, momentum, dropout rate, weight decay) in their code. To make sure that benchmarking identifies model-specific performance characteristics, rather than just implementation-specific details, we first adapt implementations of the same model to make them comparable across platforms. Besides making sure that all implementations run using the same model hyper-parameters, we also ensure that they define the same network, i.e. the same types and sizes of corresponding layers and layers are connected in the same way. Moreover, we make sure that the key properties of the training algorithm are the same across implementations. This is important for models, such as Faster R-CNN [82].

4In the Top-5 classification the classifier can select up to 5 top prediction choices, rather than just 1.
where there are four different ways in which the training algorithm can share the internal weights.

### 3.4.2 Accurate and time-efficient profiling via sampling

The training of a deep neural network can take days or even weeks making it impractical to profile the entire training process. Fortunately, as the training process is an iterative algorithm and almost all the iterations follow the same computation logic, we find that accurate results can be obtained via sampling only for a short training period (on the order of minutes) out of the full training run. In our experiments, we sample 50-1000 iterations and collect the metrics of interest based on these iterations.

To obtain representative results, care must be taken when choosing the sample interval to ensure that the training process has reached stable state. Upon startup, a typical training procedure first goes through a warm-up phase (initializing for example the data flow graph, allocating memory and loading data) and then spends some time auto-tuning various parameters (e.g., system hyper-parameters, such as matrix multiplication algorithms, workspace size). Only after that the system enters the stable training phase for the remainder of the execution. While systems do not explicitly indicate when they enter the stable training phase, our experiments show that the warm-up and auto-tuning phase can be easily identified in measurements. We see that throughput stabilizes after several hundred iterations (a few thousand iterations in the case of Faster R-CNN). The sample time interval is then chosen after throughput has stabilized.

### 3.4.3 Relevant metrics

Below we describe the metrics we collect as part of the profiling process.
• **Throughput:** Advances in deep neural networks have been tightly coupled to the availability of compute resources capable of efficiently processing large training data sets. As such, a key metric when evaluating training efficiency is the number of input data samples that is being processed per second. We refer to this metric as *throughput*. Throughput is particularly relevant in the case of DNN training, since training, unlike inference, is not latency sensitive.

For the speech recognition model we slightly modify our definition of throughput. Due to the large variations in lengths among the audio data samples, we use the total duration of audio files processed per second instead of the number of files. The lengths of data samples also varies for machine translation models, but the throughput of these models is still stable so we use the throughput determined by simple counting for them.

• **GPU Compute Utilization:** The GPU is the workhorse behind DNN training, as it is the unit responsible for executing the key operations involved in DNN training (broken down into basic operations such as vector and matrix operations). Therefore, for optimal throughput, the GPU should be busy all the time. Low utilization indicates that throughput is limited by other resources, such as CPU or data communication, and further improvement can be achieved by overlapping CPU runtime or data communication with GPU execution.

We define GPU Compute Utilization as the fraction of time that the GPU is busy (i.e. at least one of its typically many cores is active):

\[
\text{GPU utilization} = \frac{\text{GPU active time} \times 100}{\text{total elapsed time}} \%
\]

• **FP32 utilization:** We also look at GPU utilization from a different angle, measuring how effectively the GPU’s resources are being utilized while the GPU is active. More specifically, the training of DNNs is typically performed using single-precision floating point operations (FP32), so a key metric is how well the GPU’s compute potential for doing floating point operations is utilized. We compare the number of FP32 instructions the GPU actually executes while it is active to the maximal number of FP32 instructions it can theoretically execute during this time, to determine what percentage of its floating point capacity is utilized. More precisely, if a GPU’s theoretical peak capacity across all its cores is \(FLOPS_{\text{peak}}\) single-precision floating point operations per second, we observe the actual number of floating point operations executed during a period of \(T\) seconds that the GPU is active, to compute FP32 utilization as follows:

\[
\text{FP32 utilization} = \frac{\text{actual flop count during } T \times 100}{FLOPS_{\text{peak}} \times T} \%
\]

The FP32 utilization gives us a way to calculate the theoretical upper bound of performance improvements one could achieve by a better implementation. For example, an FP32 utilization of 50% indicates that we can increase throughput by up to 2x if we manage to increase the FP32 utilization up to 100%.

In addition to looking at the aggregate FP32 utilization across all cores, we also measure the per-core FP32 utilization for individual kernels, to identify
the kernels with long duration, but low utilization. These kernels should be optimized with high priority.

- **CPU utilization:** While most of the training is typically performed on the GPU, the CPU is also involved, for example, to execute the framework frontends, launch GPU kernels, and transfer the data between CPU and GPU. We report CPU utilization as the average utilization across all cores:

\[
\text{CPU utilization} = \frac{\sum c \text{ total active time of core } c \times 100}{\text{CPU core count} \times \text{total elapsed time}} \%
\]

The ratio between the cumulative active time across all cores and total elapsed time is reported by *vTune*, so CPU utilization can be directly computed from there.

- **Memory consumption:** In addition to compute cycles, the amount of available physical memory has become a limiting factor in training large DNNs. In order to optimize memory usage during DNN training, it is important to understand where the memory goes, i.e. what data structures occupy most of the memory. Unfortunately, there are no open-source tools currently available for existing frameworks that can provide this analysis. Hence we build our own memory profilers for three main frameworks (TensorFlow, MXNet, and CNTK). *We will open source these tools together with our benchmarks, as we expect them to be useful to others in developing and analyzing their models.*

When building our memory profiler we carefully inspect how the different DNN frameworks in our benchmark allocate their memory and identify the data structures that are the main consumers of memory. We observe that most data structures are allocated before the training iterations start for these three frameworks. Each of the data structures usually belongs to one of the three types: weights, weight gradients and feature maps (similarly to prior works [83]). These data structures are allocated statically. In addition, a framework might allocate some workspace as a temporary container for intermediate results in a kernel function, which gives us another type of data structure. The allocation of workspace can be either static, before the training iterations, or dynamic, during the training iterations. We observe that in MXNet, data structures other than workspace are allocated during the training iterations (usually for the momentum computation) as well. We assign these data structures to a new type called "dynamic". As memory can be allocated and released during the training, we measure the memory consumption by the maximal amount of memory ever allocated for each type.

4 Evaluation

In this section, we use the methodology and framework described in the previous section for a detailed performance evaluation and analysis of the models in our TBD benchmark suite.
4.1 Experimental Setup

We use Ubuntu 16.04 OS, TensorFlow v1.3, MXNet v0.11.0, CNTK v2.0, with CUDA 8 and cuDNN 6. All of our experiments are carried out on a 16-machine cluster, where each node is equipped with a Xeon 28-core CPU and one to four NVidia Quadro P4000 GPUs. Machines are connected with both Ethernet and high speed Infiniband (100 Gb/sec) network cards.

As different GPU models provide a tradeoff between cost, performance, area and power, it is important to understand how different GPUs affect the key metrics in DNN training. We therefore also repeat a subset of our experiments using a second type of GPU, the NVidia TITAN Xp GPU. Table 4 compares the technical specifications of the two GPUs in our work. We show the comparative throughput and comparisons of our metrics between TITAN Xp and P4000 in Section 4.3.

| Titan Xp   | Quadro P4000 | Intel Xeon E5-2680 |
|------------|--------------|---------------------|
| Multiprocessors | 30           | 14                  |
| Core Count   | 3840         | 1792                |
| Max Clock Rate (MHz) | 1582         | 1480                |
| Memory Size (GB) | 12           | 8                   |
| LLC Size (MB)  | 3            | 2                   |
| Memory Bus Type | GDDR5X       | GDDR5               |
| Memory BW (GB/s) | 547.6        | 243                 |
| Bus Interface  | PCIe 3.0     | PCIe 3.0            |
| Memory Speed (MHz) | 5705         | 3802                |
|               | 2400         |

Table 4: Hardware specifications

4.2 Performance Analysis

As previously explained, our analysis will focus on a set of key metrics: throughput, GPU and CPU compute utilization, FP32 utilization, as well as a memory consumption breakdown.

Since one of the aspects that makes our work unique is the breadth in application domains, models and frameworks covered by our TBD benchmark suite we will pay particular attention to how the above metrics vary across applications, models and frameworks.

Moreover, we will use our setup to study the effects of a key hyper-parameter, the mini-batch size, on our metrics. It has been shown that to achieve high training throughput with the power of multiple GPUs using data parallelism, one must increase the mini-batch size, and additional work needs to be done on model parameters such as learning rate to preserve the training accuracy [43, 101]. In the single-GPU case, it is often assumed that larger mini-batch size will translate to higher GPU utilization, but the exact effects of varying mini-batch size are not well understood. In this work, we use our setup to quantify in detail how mini-batch size affects key performance metrics.
4.2.1 Throughput

Figure 4 shows the average training throughput for different models from the TBD suite when varying the mini-batch size (the maximum mini-batch size is limited by the GPU memory capacity). For Faster R-CNN, the number of images processed per iteration is fixed to be just one on a single GPU, hence we do not present a separate graph for Faster R-CNN. Both TensorFlow and MXNet implementations achieve a throughput of 2.3 images per second for Faster R-CNN. We make the following three observations from this figure.

Observation 1: Performance increases with the mini-batch size for all models. As we expected, the larger the mini-batch size, the higher the throughput for all models we study. We conclude that to achieve high training throughput on a single GPU, one should aim for a reasonably high mini-batch size, especially for non-convolutions models. We explain this behavior as we analyze the GPU and FP32 utilization metrics later in this section.

Observation 2: The performance of RNN-based models is not saturated within the GPU’s memory constraints. The relative benefit of further increasing the mini-batch size differs a lot between different applications. For example, for the NMT model increasing mini-batch size from 64 to 128 increases training
throughput by 25%, and the training throughput of Deep Speech 2 scales almost linearly. These two models’ throughput (and hence performance) is essentially limited by the GPU memory capacity and we do not see any saturation point for them while increasing the mini-batch size. In contrast, other models also benefit from higher mini-batch size, but after certain saturation point these benefits are limited. For example, for the Inception-v3 model going from batch size of 16 to 32 has less than 10% in throughput improvement for implementations on all three frameworks.

**Observation 3:** Application diversity is important when comparing performance of different frameworks. We find that the results when comparing performance of models on different frameworks can greatly vary for different applications, and hence using a diverse set of applications in any comparisons of frameworks is important. For example, we observe that for image classification the MXNet implementations of both models (ResNet-50 and Inception-v3) perform generally better than the corresponding TensorFlow implementations, but at the same time, for machine translation the TensorFlow implementation of Seq2Seq (NMT) performs significantly better than its MXNet counterpart (Sockeye). TensorFlow also utilizes the GPU memory better than MXNet for Seq2Seq models so that it can be trained with a maximum mini-batch size of 128, while MXNet can only be trained with a maximum mini-batch of 64 (both limited by 8GB GPU memory). For the same memory budget, it allows TensorFlow to achieve higher throughput, 365 samples per second, vs. 229 samples per second for MXNet. We conclude that there is indeed a significant diversity on how different frameworks perform on different models, making it extremely important to study a diverse set of applications (and models) as we propose in our benchmark pool.

### 4.2.2 GPU Compute Utilization

Figure 5 shows the GPU compute utilization, the amount of time GPU is busy running some kernels (as formally defined by in Section 3) for different benchmarks as we change the mini-batch size. Again, for Faster R-CNN, only batch of one is possible, and TensorFlow implementation achieves a relatively high compute utilization of 89.4% and the MXNet implementation achieves 90.3%.

We make the following two observations from this figure.

**Observation 4:** The mini-batch size should be large enough to keep the GPU busy. Similar to our observation 1 about throughput, the larger the mini-batch size, the longer the duration of individual GPU kernel functions and the better the GPU compute utilization, as the GPU spends more time doing computations rather than invoking and finishing small kernels. While large mini-batch sizes also increase the overhead of data transfers, our results show that this overhead is usually efficiently parallelized with the computation.

**Observation 5:** The GPU compute utilization is low for LSTM-based models. Non-RNN models and Deep Speech 2 that uses regular RNN cells (not LSTM) usually reach very high utilization with large batches, around 95% or higher. Unfortunately, LSTM-based models (NMT, Sockeye) cannot drive up GPU uti-
4.2.3 GPU FP32 utilization

Figure 6 shows the GPU FP32 utilization (formally defined by \( \eta \) in Section 3) for different benchmarks as we change the mini-batch size (until memory capacity permits). For Faster R-CNN, the MXNet/TensorFlow implementations achieve an average utilization of 70.9%/58.9% correspondingly. We make three major observations from this figure.

**Observation 6:** The mini-batch size should be large enough to exploit the FP32 computational power of GPU cores. As expected, we observe that large mini-batch sizes also improve GPU FP32 utilization for all benchmarks we study. We conclude that both the improved FP32 utilization (Observation 6) and GPU utilization (Observation 4) are key contributors to the increases in overall throughput with the mini-batch size (Observation 1).

**Observation 7:** RNN-based models have low GPU FP32 utilization. Even with the maximum mini-batch size possible (on a single GPU), the GPU FP32 utilization of the two RNN-based models (Seq2Seq and Deep Speech 2, Figure 6c and Figure 6f, respectively) are much lower than for other non-RNN models. This clearly indicates the potential of designing more efficient RNN layer implementations used in TensorFlow and MXNet, and we believe further research should be done to understand the sources of these inefficiencies. Together with Observation 5 (low GPU utilization for LSTM-based models) this observation explains why in Observation 2 we do not observe throughput saturation for RNN-based models even for very large mini-batches.

**Observation 8:** There exists kernels with long duration, but low FP32 utili-
Table 5: Longest 5 kernels with utilization level below the average (ResNet-50, mini-batch size 32, TensorFlow)

| Duration | Utilization | Kernel Name |
|----------|-------------|-------------|
| 8.36%    | 30.0%       | magma_dds128_gemm_kernel... |
| 8.53%    | 42.3%       | cudnn::detail::bn_bw_IC11_kernel_new... |
| 4.65%    | 46.3%       | cudnn::detail::bn_bw_IC11_kernel_new... |
| 3.12%    | 20.0%       | Eigen::internal::EigenMetaKernel... |
| 2.48%    | 40.0%       | tensorflow::BiasNHWCKernel... |

Table 6: Longest 5 kernels with FP32 utilization below the average (ResNet-50, mini-batch size 32, MXNet)

Observation 9: CPU utilization is low in DNN training. We observe that for all our models the CPU utilization is very low, less than 15% for all but one model, less than 8% for all but two models. For our CPU machines with 28 cores, this means that on average less than 2 cores are usually busy. We believe
that future research should look into how to make CPUs more useful for DNN training. For example, they can be used to compute layers that cannot benefit from the massive GPU compute power, such as batch normalization.

4.3 Hardware Sensitivity

The results presented so far, were based on experiments with the Quadro P4000 GPU. In this section we are interested in seeing how the performance of DNN training will depend on the hardware used. Toward this end we compare the training throughput, GPU utilization, and FP32 utilization for several of our models: ResNet-50, Inception-v3, and Seq2Seq on P4000 GPU and the more powerful Titan Xp GPU. For throughput comparison, we normalized each model result to the throughput of less powerful P4000 card. We make the following observation from this figure.

Observation 10: More advanced GPUs should be accompanied by better systems designs and more efficient low-level libraries. Titan Xp usually helps improving the training throughput (except for Sockeye), however the computation power of Titan Xp is not well-utilized. Both the GPU and the FP32 utilizations of Titan Xp appear to be worse than those of P4000. Hence we conclude that although Titan Xp is more computationally powerful (more multiprocessors, CUDA cores, and bandwidth, see Table 4), the proper utilization of these resources requires a more careful design of existing GPU kernel functions, libraries (e.g., cuDNN), and algorithms that can efficiently exploit these resources.

4.4 Memory Profiling

As we have previously shown, the throughput (and hence the performance) of DNN training can be significantly bottlenecked by the available GPU memory. Figure 9 shows the result of our analysis where the memory is separated in five categories: weights, gradient weights, feature maps, dynamic, and workspace. Where appropriate, we vary the size of the mini-batch (shown in parentheses). The Faster R-CNN model results are similar to image classification models, but only support one batch size (hence we do not plot them in a separate graph).

Observation 11: Feature maps are the dominant consumers of memory. It turns out that feature maps (intermediate layer outputs) are the dominant part of the memory consumption, rather than weights, which are usually the primary focus of memory optimization for inference. The total amount of memory consumed by feature maps ranges from 62% in Deep Speech 2 to 89% in ResNet-50 and Sockeye. Hence any optimization that wants to reduce the memory footprint of training should, first of all, focus on feature maps. This is an interesting observation also because it expands on the results reported in the only prior work reporting on memory consumption breakdown for DNN training by Rhu et al. They look at CNN training only and find that weights are only responsible for a very small portion of the total memory footprint. We extend this observation outside of CNNs, but also observe that there are models (e.g., Deep Speech 2) where weights are equally important.
Figure 8: Throughput, Compute Utilization, FP32 Utilization comparison between P4000 and Titan Xp for different benchmarks.

Observation 12: Simply exhausting GPU memory with large mini-batch size might be inefficient. The memory consumption of feature maps scales almost linearly with the mini-batch size. From observation 11, we know that reducing the mini-batch size can dramatically reduce the overall memory consumption needed for training. Based on observation 1, we also know that the side-effect of throughput loss while reducing the mini-batch size can be acceptable (for non-RNN models) until you do not go below saturation point. One can use the additional GPU memory for larger workspace (can be used for faster implementation of matrix multiplications or convolutions) and deeper models (e.g., ResNet-102 vs. ResNet-50).

4.5 Multi-GPU and Multi-Machine Training

Training large DNNs can be done faster when multiple GPUs and/or multiple machines are used. This is usually achieved by using data parallelism, where mini-batches are split between individual GPUs and the results are then merged, for example, using the parameter server approach. But in order to realize the computational potential of multiple GPUs the communication channels between them need to have sufficient bandwidth to exchange proper weight updates. In our work, we decide to analyze the performance scalability of DNN training using multiple GPUs and multiple machines. We use the ResNet-50 model on MXNet to perform this analysis. Figure 10 shows the results of our
Observation 13: Network bandwidth must be large enough for good scalability. We observe that going from the one machine (1M1G) to the two machine (2M1G (ethernet)) configuration the performance degrades significantly. This is because DNN training requires constant synchronization between GPUs in distributed training. Hence faster networking is required to improve the situation (the 2M1G (infiniband) configuration has 100Gb/s InfiniBand Mellanox networking). In contrast, DNN training on a single machine with multiple GPUs (1M1G, 1M2G, 1M4G) scales reasonably well as PCIe 3.0 gives enough bandwidth (16 GB/s). In summary, this suggests that networking bandwidth is critical for performance of distributed training and different techniques (in both software and hardware) should be applied to either reduce the amount of data sent or increase the available bandwidth.

5 Related Work

There are only a handful of existing open-source DNN benchmark projects, each with a focus that is very different from our work. ConvNet [3], CNN-benchmarks [2] and Shaohuai et al. [89] focus exclusively on convolutional net-
work models mainly for image classification based on the ImageNet data, with
the only exception being one LSTM network in [89]. In contrast the goal of
our work is a benchmark that covers a wide range of models and applications,
beyond just CNNs and image classification.

DeepBench [5] is an open-source project from Baidu Research, which is tar-
geted at a lower level in the deep learning stack than our work: rather than
working with implementations of deep learning models and frameworks, it in-
stead benchmarks the performance of individual lower level operations (e.g.
matrix multiplication) as implemented in libraries used by various frameworks
and directly executed against the underlying hardware.

The Eyeriss project [1] presents evaluations of a few DNN processors [26, 46]
on hardware metrics for several convolutional networks, but their work is focused
on inference, while ours targets training.

Among existing work, Fathom [11] is probably the one closest to our own, as
it also focuses on training and more than a single application (machine trans-
lation, speech recognition and reinforcement learning). However, their focus is
on micro-architectural aspects of execution, breaking down training time into
time spent on the various operation types (e.g. matrix multiplication). In con-
trast, our benchmark pool focuses on system level aspects of execution such as
throughput, hardware utilization, and memory consumption profiling. More-
over, Fathom is based on only one framework (TensorFlow), does not consider
distributed training and uses models that are somewhat out-dated by now.

Driven by the achievements of DNN algorithms and the availability of large
datasets, many frameworks [10, 20, 24, 102, 59, 93, 32, 30, 76] were recently
proposed for users to easily develop new DNN models for different application
domains. These frameworks provide high-level numpy-like APIs or layer-wise
configuration files to promote programmability. They are also able to make use
of modern hardware accelerators (especially GPUs) to speed up the DNN train-
ing process. In our work, we use three of these frameworks: TensorFlow [10],
MXNet [24], and CNTK [102], but we envision to add more frameworks with
more models as we keep developing our benchmark pool and based on the feed-
back we expect from both academia and industry.

Due to the complexity of DNN computations, ML developers usually need
additional profiling tools to understand the training performance characteristics. Some frameworks have their own profiling tools embedded. For example, MXNet allows users to see the timeline for individual layers. However, this layer-level representation hides details inside a layer computation, and provide little information about efficiency of GPU computation. We therefore use the NVIDIA profiling tool called nvprof [9], which enables detailed performance information for each GPU kernel. It also shows a timeline of both CPU and GPU activities at the function/kernel level. Another end-to-end profiling tool we use is the Intel VTune Amplifier. It provides detailed analysis of CPU performance (e.g., identifies the “hotspots”, where the application spends a lot of time) and also supports the metrics we need. At the same time, we can not use these tools directly on the full training process due to memory and time limits, and has to adopt these tools for our need as described in Section 3.

To exploit the GPU computation power and to reduce the programming effort, there are several GPU libraries that provide efficient implementation of basic operations on vectors and multi-dimension matrices. The most notable examples include cuDNN [27] and cuBLAS [4] by NVIDIA, MKL [96] by Intel, and Eigen [6]. NVIDIA also provides the NCCL library [7] which implements multi-GPU and multi-node communication primitives to reduce communication overhead among GPUs. These libraries are widely employed by most mainstream deep learning frameworks and the three frameworks we use in this work (TensorFlow, MXNet, and CNTK). These libraries greatly affect the overall training performance, and hence are an important target of performance analysis and tuning.

Multiple techniques are proposed to reduce the memory usage of DNN, including network pruning [49, 65, 50, 47, 48], parameter quantizing or precision reducing [47, 16, 40, 33, 78].

These are extremely useful for inference since they are very effective in reducing the memory footprint of weights, which enables DNN inference in mobile environment. Rhu et al. [83] has shown that for the state-of-the-art CNN training, weights are only responsible for a very small portion of total memory footprint. We extend this observation outside of CNNs, but also show that there are models (e.g., Deep Speech 2) where weights are equally important. Algorithms designed for training DNN with quantized values [33, 48, 40] suffer from accuracy loss for state-of-the-art models on large datasets. Rhu et al. [83] develops a new mechanism which uses CPU memory as a temporary container for feature maps, which greatly reduces the memory footprint of DNN training.

They also developed a tool to show the GPU memory usage for different data structures, but, unfortunately, this tool is not available outside of NVIDIA. In this work, we aim to build efficient memory profilers that will be available to a wider community as we open source them.
6 Conclusion

In this work, we proposed a new benchmark suite for DNN training, called TBD, that covers a wide range of machine applications from image classification and machine translation to reinforcement learning. TBD consists of eight state-of-the-art DNN models implemented on major deep learning frameworks such as TensorFlow, MXNet, and CNTK. We used these models to perform extensive performance analysis and profiling to shed light on efficiency of DNN training for different hardware configurations (single-/multi-GPU and multi-machine). We developed a new tool chain for end-to-end analysis of DNN training that includes (i) piecewise profiling of specific parts of training using existing performance analysis tools, and (ii) merging and analyzing the results from these tools using the domain-specific knowledge of DNN training. Additionally, we built new memory profiling tools specifically for DNN training for all three major frameworks. These useful tools can precisely characterize where the memory consumption (one of the major bottlenecks in training DNNs) goes and how much memory is consumed by key data structures (weights, activations, gradients, workspace). By using our tools and methodologies, we made several important observations and recommendations on where the future research and optimization of DNN training should be focused. We hope that our TBD benchmark suite, tools, methodologies, and observations will be useful for a large number of ML developers and systems designers in making their DNN training process efficient.

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