High-Speed Magnetoresistive Random-Access Memory Random Number Generator Using Error-Correcting Code

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A high-speed random number generator (RNG) circuit based on magnetoresistive random-access memory (MRAM) using an error-correcting code (ECC) post processing circuit is presented. ECC post processing increases the quality of randomness by increasing the entropy of random number. We experimentally show that a small error-correcting capability circuit is sufficient for this post processing. It is shown that the ECC post processing circuit powerfully improves the quality of randomness with minimum overhead, ending up with high-speed random number generation. We also show that coupling with a linear feedback shift resistor is effective for improving randomness.

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I. INTRODUCTION

In light of the advent of ubiquitous networks, security for mobile applications has become more important and advanced security systems are required. For many security systems, random numbers are widely used to create IDs, passwords, and so on. An on-chip random number generator (RNG) is one of the key elements for a secure system-on-chip. Unpredictability is one of the most important characteristics of random numbers. RNGs capable of generating natural random numbers by means of physical phenomena have recently been investigated and have begun to replace pseudo-random numbers generated by software. Various kinds of on-chip RNG using physical noise signals such as random telegraph noise in transistors, noise in diode junctions, or magnetic tunnel junctions (MTJs) for magnetoresistive random-access memory (MRAM) have been proposed.

Because RNGs based on physical phenomena are affected to a greater or lesser degree by their physical environments and manufacturing processes, for example by variation of device size, after AD-converting physical noise signals, post processing using digital circuits is always needed to balance ‘0’ and ‘1’ to eliminate periodicity and correlation with the original signals. The “rejection method” is most frequently used for the post processing circuit (PPC), where two serial bit sequences ‘01’ and ‘10’ are replaced by ‘0’ and ‘1’, whereas ‘00’ and ‘11’ are discarded. Although this method is simple and clear, when the original physical signals fluctuate, the balance between ‘0’ and ‘1’ easily collapses and leads to a low generation rate of random numbers after wasting a lot of bits to create balanced random numbers. One of the more sophisticated methods for PPC is to apply a data compression method in order to increase the entropy of randomness. Lacharme proposed a PPC using the Bose-Chaudhuri-Hocquenghem (BCH) error-correcting code (ECC). He proved that derivation of probability of ‘0’ and ‘1’ from 1/2, e/2, can be reduced to e^d/2 with a minimal distance d of the ECC code. However, it is unclear whether this PPC improves the quality of randomness sufficiently to pass commercial-level statistical tests. Moreover, compared with the noise sources, the area of an ECC circuit is generally larger and consumes more power. Consequently, the additional ECC circuit for RNGs is inclined to dominate the area and power of the RNG.

In this paper, we present a novel MRAM-based RNG, where, in addition to the conventional memory function of MRAM, the memory system is also used as the physical noise signal, and ECC circuits used for correcting MRAM memory bit error are also converted to PPC when a random number is required (Fig. 1). MRAM produces a random number by reducing the programming current to cause writing errors intentionally in the RNG mode (Fig. 2). The sharing of the memory system including ECC circuits with RNG leads to a reduction of circuit area and an efficient secure memory system for mobile applications.

The remainder of this paper is organized as follows: in §2, we describe our general idea of PPC using ECC circuit including an explanation of the conventional ECC procedure. In §3, we present our MRAM system to create RNG. In §4, we show our experimental results and analyze the ECC PPC process. §5 is a discussion part. Our conclusions are summarized in §6.
II. POST PROCESSING USING ECC CIRCUIT

A. RNG PPC circuit

The data compression by PPC using ECC increases the entropy of random numbers. A block of \( n \) bits is transferred into \( k \) bits by this circuit (\( n > k \)). Figure 1 shows a schematic of a proposed post processing circuit shared by the conventional error-correction linear block. The ECC circuit is usually used for the error correction of memory bits. The key point of our system is that we can change the role of a conventional ECC circuit to PPC by adding only a small number of transistors (Figs. 3 and 4). First, let us remember the conventional ECC. A given message data stream is broken up into blocks, such as \( k \)-symbol data block \( \mathbf{m} = (m_0, m_1, \ldots, m_{k-1}) \). A generating matrix \( \mathbf{G} \) encodes a given message \( \mathbf{m} \) to a code \( \mathbf{c} = \mathbf{mG} \). In a simple form, \( \mathbf{G} \) is the \( n \times k \) generating matrix constituted from a generator polynomial as

\[
G(x) = g_0 + g_1x + \ldots + g_{n-k}x^{n-k},
\]

such as

\[
\mathbf{G} = \begin{pmatrix}
g_{n-k} & g_{n-k-1} & \cdots & g_0 & 0 & \cdots & 0 \\
0 & g_{n-k} & g_{n-k-1} & \cdots & g_0 & \vdots & \ddots & \vdots \\
0 & \cdots & 0 & g_{n-k} & g_{n-k-1} & \cdots & g_0
\end{pmatrix}. \tag{2}
\]

In the present case, the original raw random bit sequence \( \mathbf{y} = (y_0, \ldots, y_n) \) is converted into post-processed data \( \mathbf{z} = (z_0, \ldots, z_c) \) as \( \mathbf{z} = \mathbf{Gy} \). The coefficients of the generator polynomials \( G(x) \) for binary BCH codes for \( n \leq 127 \) are given in Table I.

These encoding and decoding processes of cyclic linear codes are efficiently implemented using exclusive-OR gates, switches, and shift registers that include flip-flops (FF) connected in series. Note that data compression \( \mathbf{z} = \mathbf{Gy} \) for random bits \( \mathbf{y} \) differs from \( \mathbf{c} = \mathbf{mG} \) for code \( \mathbf{c} \) in terms of the position of FFs. Thus, we implement both circuits by adding switching transistors, as shown in Fig. 3. Then, we can change the role of the circuit between error correction of memorized bits and that of RNG post processing by switching transistors expressed by ECC-SW and RNG-SW in Fig. 3. Note also that BCH codes can be chosen appropriately by controlling ON/OFF of transistors \( g_0, \ldots, g_{n-k} \). Figure 4 shows an implemented form of the shared decoder block in Fig. 3 for a generator polynomial of the \((7,4)\) code is given by \( G(x) = x^3 + x + 1 \). In a rejection method, the number of bits is reduced to about one-fourth of the original data [compression rate is about less than \( 1/4 \)]. On the other hand, PPC using the \((n,k,t)\) BCH code transform \( n \) bits to \( k \) bits, and thus the compression rate is \( k/n \) [\( t \) is an error-correcting capability].

B. Coupling with linear feedback shift resistor (LFSR)

Because physical RNGs originate from physical phenomena, there are some cases where physical RNGs does not produce desirable random numbers, such as electrical breakdown of stacked thin films. Thus, in general, some supplementary circuits are always required for commercial use. A linear feedback shift resistor (LFSR) is most frequently used for the support of physical RNGs. LFSR, which produces a sequence of bits, is composed of a shift resistor and a feedback function by XOR of certain bits in the resistor. \( N \)-bit LFSR, which is constituted by \( N \) FFs, can hold \( 2^N \) 1-bit long pseudo-random sequences for appropriate input data. Because each FF includes more than 20 transistors, a smaller \( N \)-bit LFSR is desirable for reducing circuit area. Here, we investigate \( N \)-bit LFSR with \( N \leq 8 \). Concretely, we try \((1,0),(2,1,0),(3,1,0),(4,1,0),(7,1,0),(7,3,0)\) LFSRs, where listing \((1,0)\) means that a new bit is generated by XORing a shifted bit with the next bit, and listing \((7,1,0)\) means that a seven times shifted bit and a shifted bit are XORed with the next bit, and so on. Figure 5 shows \((2,1,0)\)-LFSR and \((3,1,0)\)-LFSR. We found that small LFSR is suitable for MRAM RNG, as shown below.
FIG. 3: Proposed RNG post processing unit which is shared with memory bit error-correcting block. FF is a flip-flop element. In ECC mode, “ECC-SW” is ON and in RNG mode, “RNG-SW” is ON. \( g_0, \ldots, g_{n-k} \) is determined by \( G(x) \). For example, when \( G(x) = x^5 + x^2 + 1 \), \( g_0, g_2, \) and \( g_5 \) are 1 when transistors are ON states.

FIG. 4: Example of a proposed RNG post processing unit shared with ECC decoder. ECC for RNG is easily changed by switching RNG-SW and ECC-SW. Example for (7,4) code. We can also apply the RNG post processing unit to the ECC encoder block.

III. MRAM RNG

MRAM cell arrays are integrated by the 130 nm front process and 240 nm back-end process (Fig. 6). An MRAM random number is generated by controlling the switching current such that the probability of change of magnetism of the free layer is 50\% (Fig. 1). Figure 7 shows the MRAM switching probability \( P_{\text{write}} \) as a function of switching current at various pulse widths. In the present MRAM, the slopes of the change in switching probabilities look similar regardless of the pulse duration rate. This leads to the stable operation of MRAM cells. A closer look at this figure, in particular at the tail parts of the slopes, reveals that the slope of \( P_{\text{write}} \) becomes slightly smaller for a shorter pulse width \( t_{\text{write}} \) (speed-up). This means a shorter pulse is favorable for producing current fluctuation at approximately \( P_{\text{write}} \approx 1/2 \). The applied voltage to the MRAM cell is controlled by checking the ‘0’ and ‘1’ balance of the random data. Here, we prepared three typical types of data (Table II). Data \( A \) (balanced data) is obtained after repeating the adjustment process of voltage control and the estimation of the ‘0’ and ‘1’ balance. Data \( B \) (unbalanced data) is obtained by slightly changing the applied voltage of data \( A \) in order to lose the balance. Data \( C \) (slightly unbalanced data with a higher speed) is obtained by adjusting the applied voltage at a higher pulse generation rate.

IV. RESULTS

Figure 8-11 show the results of statistical tests of randomness after ECC post processing for \( n = 31, 63, \) and 127 codes (Table I) as a function of the error-correcting capability \( t \). For

| Data Balance | \( t_{\text{write}} \) (ns) |
|--------------|-----------------|
| \( A \) 51.1% ‘1’ | 30 |
| \( B \) 27.6% ‘1’ | 30 |
| \( C \) 36.3% ‘1’ | 10 |

FIG. 7: Switching probability as a function of switching current at various pulse durations \( t_{\text{write}} \). The gentle tail part of the slope of shorter pulse such as \( t_{\text{write}} = 10 \) ns is considered to be favorable for generating random numbers, because it contributes to producing larger current fluctuations at approximately \( P_{\text{write}} \approx 1/2 \).
the three types of data (Table II), a rejection method compresses those data to 24.8 % (data A), 20.0 % (data B), and 23.1 % (data C), respectively. In contrast to the rejection method, for ECC post processing, for example, for \( t = 2 \), these rates are fixed to \( k/n \) and given as 90.0 % (\( n = 127 \)), 80.0 % (\( n = 63 \)), and 67.7 % (\( n = 31 \)). The statistical test suite NIST PUB SP 800-22 \[\text{(12)}\] that contains 16 types of tests and judges 160 test results is used for a million bits set to a \( P \)-value of 0.01\[\text{51}\]. Although there are several kinds of Pass/Fail assignments for this test suite, we simply count the number of test failures and judge Pass if it is 2 or less.

Figure \[\text{8}\] shows results for PPC using ECC for balanced data (data A), unbalanced data with \( t_{\text{write}} = 30 \) ns (data B), and slightly unbalanced with higher speed of \( t_{\text{write}} = 10 \) ns (data C). These results prove the improvement ability of the ECC post processing. In particular, unbalanced data (data B and C) are greatly improved by this method. Note that the raw bit sequence just after MRAM unit fails in almost all these tests. Moreover, we could not see any specific correlation between improvement and the error-correcting capability \( t \). This does not follow the prediction of ref.\[\text{10}\] in which better random numbers are obtained as \( t \) (or \( d \)) increases (\( d \) and \( t \) has a relation \( d > 2t \)). Because RNG speed decreases at rate \( k/n \), and \( n - k \) extra redundant memory cells are required, these results show that a small \( t \) can be chosen.

Figures \[\text{9-11}\] show results of ECC post processing with (2,1,0)- and (3,1,0)-LFSR. We examined several lengths of LFSR and found that a length of two or three LFSRs is sufficient. That is, coupling with longer bit LFSRs such as (4, 1, 0), (7, 1, 0), etc. does not always show a greater improvement than 2-bit and 3-bit LFSRs. This might be because LFSR itself does not increase the entropy of randomness and just mix random bit sequences. If transistors can be set to adjust the generating polynomial [eq.(1)] depending on original random signals, the most appropriate \( (n,k,t) \) can be selected. When results of data A are compared with those of data C, it can be seen that the acceleration of current pulse from \( t_{\text{write}} = 30 \) ns to \( t_{\text{write}} = 10 \) ns increases the quality of randomness by ECC post processing. This is considered to be related to the slope of switching probability (Fig. \[\text{2}\]). Finally, we estimate the generation speed of the present RNG. When the read time is 10 ns and four clocks are required for outputting one-bit random number, 25 MHz generation speed is expected for a RNG. Table III shows that the estimated generation speeds of MRAM-based RNGs are much faster than those of state-of-the-art RNGs reported in ref.\[\text{14}\] and\[\text{15}\].

![FIG. 8: Result of statistical test (NIST800-22). Number of failures after ECC post processing for (a) good original random number bits (data A), (b) unbalanced bits (data B) and (c) slightly unbalanced with higher speed (data C), as a function of error correcting capability \( t \) for \( n = 31, 63 \) and 127 BCH codes. Note that raw bit sequence just after MRAM unit fails in almost all these tests. That is, the number of failures for raw data is close to 160.](image)

![FIG. 9: Result of statistical test (NIST 800-22) for data A (balanced bits) coupled with 2-bit LFSR (a) and 3-bit LFSR (b). Both LFSRs improve the quality of randomness compared with Fig. \[\text{8}\](a).](image)

![FIG. 10: Result of statistical test (NIST 800-22) for data B (unbalanced bits) coupled with 2-bit LFSR (a) and 3-bit LFSR (b). Both LFSRs improve the quality of randomness compared with Fig. \[\text{8}\](b).](image)

| TABLE III: Comparison of generation speeds of RNGs. |
|-----------------------------------------------------|
| **RNG** | **Speed (MHz)** |
| Ref.\[\text{14}\] | 2 |
| Ref.\[\text{15}\] | 0.2 |
| MRAM | 25 |

The reason why the PPC using ECC is effective for MRAM RNG is considered to be that MTJ directly outputs discrete two values of current. We also applied this method to RNG based on transistor noise\[\text{15}\], in which the current noise signal is a continuous variable and should be converted to digital signals by an analog circuit. It is found that we need to apply this PPC a couple of times for RNG based on transistor noise to pass statistical tests. Thus, it seems that this method is less effective for RNG based on transistor noise. Thus, direct observation of two distinct physical quantities in MTJ is considered to be related to the efficiency of the PCC using ECC.

We experimentally showed that small error-correcting capability is sufficient such as \( t \leq 2 \). As noted in the introduction, Lacharme only showed that ECC theoretically improved

![FIG. 11: Result of statistical test (NIST 800-22) for data C (unbalanced bits) coupled with 2-bit LFSR (a) and 3-bit LFSR (b). Both LFSRs improve the quality of randomness compared with Fig. \[\text{8}\](b).](image)
consumption of MTJ is 0.05 mW for one bit. If we take 2 ns as a write time, then the power consumption of MRAM RNGs is lower than that of currently used oscillator-based RNGs. In the near future, power consumption will be further reduced by decreasing switching current.

In general, random data are not very large in mobile applications and are used temporarily. Thus, the coexistence of memory data and random data is not a problem as long as each memory address is controlled.

### VI. CONCLUSIONS

We presented a novel MRAM-based RNG using ECC in which ECC post processes random numbers in addition to fulfilling the conventional function of correcting memory bit errors. We have proven that the MRAM-based RNG using ECC post processing efficiently increases both randomness quality and generation speed.

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20. $P$-value is associated with a test statistic and is a probability that a perfect random number generator would have produced a sequence less random than the sequence that was tested, given the kind of nonrandomness assessed by the test. If the $P$-value equals 1, the sequence appears to have perfect randomness and if the $P$-value equals 0 the sequence appears to be completely non-random.
21. International Technology Roadmap for Semiconductors (ITRS) [Table ERD5].