Photoelectric effect on an Al/SiO₂/p-Si Schottky diode structure

E Saloma 1,*, S Alcántara 1, N Hernández-Como 2, J Villanueva-Cab 1, M Chavez 1, G Pérez-Luna 1 and J Alvarado 1,*

1 Benemérita Universidad Autónoma de Puebla, CIDS, Av. San Claudio y 18 Sur, Col. San Manuel, Ciudad Universitaria, C.P. 72570, PO Box 1067, Puebla, Pue. 7200, México
2 Centro de Nanociencias y Micro y Nanotecnologías, Instituto Politécnico Nacional, México
3 Instituto de Física, Unidad Ecocampus-Vallequillo, Benemérita Universidad Autónoma de Puebla, Apdo. Postal J-48, Puebla, Puebla 72570, México
* Authors to whom any correspondence should be addressed.
E-mail: erasmo.salomar@yahoo.com.mx and joaquin.alvarado@correo.buap.mx

Keywords: MIS Schottky diode, photoelectric effect, silicon photovoltaic cell

Abstract
A SiO₂ of 200 nm thickness layer was grown via thermal oxidation to obtain an Al/SiO₂/p-Si MIS Schottky diode structure with top contacts and different active areas. Electrical measurements of MIS Schottky diode structure allow to observe the photoelectric effect only in the device with higher active area, as well as to observe some electrical parameters such as the barrier height, the ideality factor and the density of interface states, which correspond to 0.97 eV, 1.46 and 4.44 × 10¹⁰ eV⁻¹ cm⁻² respectively. Furthermore, a fill factor of 0.202 and power conversion efficiency less than 1%. On the other hand, Capacitance-Voltage (C–V) measurements depict a positive and negative capacitance peaks at low frequencies; this behavior and photoelectric effect are attributed to the density of interface states at SiO₂/p-Si, as well as to the Space-Charge-Limited Conduction process in the insulation layer. Furthermore, the use of this kind of insulator can allows increasing the conversion efficiency if it is used as bottom n-layer or front contact in tandem solar cells and silicon heterojunction solar cells, respectively.

1. Introduction

The metal–insulator–semiconductor (MIS) Schottky diode is extensively used in power and high-frequency electronic devices; nevertheless, the application that has a tendency as an electric power generator by the photoelectric effect. A photoelectric solar power device differs from a photovoltaic device (solid-state) in the nature of its charge transport; however, both devices are based on the charge released by the energy of a photon that overcomes an energy barrier [1]. The control of the spectrum losses of the device, as well as its energy conversion efficiency is performed by the work function ϕ in a photoelectric solar power device, while in the case of the photovoltaic device; it is done by the band gap.

The MIS Schottky diode consists of aluminum as metal contact, a silicon dioxide (SiO₂) layer as an insulator, and p-type silicon as a semiconductor. The insulator layer like SiO₂, SnO₂, Si₃N₄ between the metal and semiconductor generates a potential barrier that suppresses the majority carriers and improves the photogenerated current of the device [2] due to the inhomogeneity in the insulator layer composition. SiO₂ is an insulator material widely used in applications of photovoltaic devices due to its interesting chemical and physical properties like low refractive index, high thermal stability, low thermal conductivity, and low price [2]. Tseng and Wu [3] studied the effect of the insulator layer of SiO₂ on a MIS Schottky diode. They calculated the barrier height and density of interfacial states through the analysis of the I–V curves measured to their system. Cowley and Sze [4] made the first studies on the interfacial insulator layer between metal and semiconductor–metal in MIS Schottky diodes, who estimated the Schottky barrier height has a dependence of the metal work function. Depas et al. [5] proved that the barrier inhomogeneity of the MIS Schottky diodes is due to the
inhomogeneity in the insulator layer composition, non-symmetry of the interfacial charges, and native insulator layer thickness.

The electrical properties of the MIS Schottky diodes are affected by the thickness and degree of crystallinity of the insulator layer between semiconductor and metal, interface states ($N_{SS}$), series resistance ($R_s$), and the barrier height ($\Phi_b$). Theoretically, leakage current across thick insulators is completely blocked regardless of the active area size. However, polycrystalline and amorphous insulators could present some conduction mechanisms that can allow a current flow through it, which depends on the density and energy level of traps in the insulator [6]. Thanks to this behavior, silicon oxide layers can be used to increase the conversion efficiency and stability in tandem solar cells as a contact layer between the perovskite cell (top cell) and silicon substrate (bottom cell) [7], as well as if it is used as front contact to reduce current losses in heterojunction solar cells [7] and [8].

For insulator layers, less than 50 Å thickness, the interface states are in equilibrium with the semiconductor providing better conductivity and charge transport [9]. On the other hand, at high frequencies ($f \geq 500$ kHz), charges at the interface states do not follow an AC signal [10], being only possible to observe the number of charges at low AC frequencies. For that reason, the frequency–dependent dielectric and electrical characteristics are important for obtaining accurate and reliable results [11].

The interface states can modify the $C$–$V$ characteristics of MIS Schottky diode, generating a bending of the $C^{-2}$–$V$ plot and affect the ideality factor. The capacitance method in semiconductor research allows obtaining information about parameters regarding the energy levels [10] and [12]. Some researchers reported anomalous peaks in the forward bias $C$–$V$ characteristics [13–15]. The origin of the anomalous behavior has been associated with the interface states and the series resistance effect [16] and [17].

In the present study, the main objective is to investigate the photoelectric effect on an Al/SiO$_2$/p-Si MIS Schottky diode structure by varying the active area through increasing the separation between the metal contact and the SiO$_2$, whereas the distance between electrodes and the width and length are keeping constant. Obtained electrical characteristics make the proposed MIS Schottky diode device an attractive option for photovoltaic applications based on the $I$–$V$ characterization, used to determine the open-circuit voltage ($V_{OC}$) and the short circuit current ($I_{SC}$), as well as the conduction mechanism and the $C$–$V$ plot to observe changes on the interface states.

### 2. Experimental procedure

The Al/SiO$_2$/p-Si MIS Schottky diode structure was fabricated using p-type silicon (Si) wafer with (100) orientation, thickness 280 µm, 2’ diameter, and resistivity of 1–10 Ω·cm. After the initial wafer cleaning process, the wafer was thermally oxidized in dry oxygen at a temperature of 1, 100 °C in a three-zone oven with an O$_2$ flow of 0.0283 m$^3$/h with 99.5% purity for 173 min, to grow a SiO$_2$ layer of thickness ~ 200 nm. Subsequently, the wafer is cleaned with acetone, isopropyl alcohol, and de-ionized water, after, the positive resin is deposited on the wafer surface by spin coating and dried at 115 °C for 1 min. Immediately the resin is sensitized by one first mask, and the pattern is etched on the SiO$_2$ layer. Aluminum metallization was deposited by sputtering, 99.99% purity, 150 W, 5 mTorr, 13.6 sccm in Argon atmosphere for 110 min. Positive resin is deposited on the aluminum, and the resin is sensitized for a second mask, and the pattern is etched on the Al layer, figure 1.

The thickness of the aluminum, both the one on the SiO$_2$ layer and the one on the p-type silicon are ~200 nm. The tungsten filament lamp of 12 V and 35 W was characterized at a distance of 7 cm using a Kipp & Zonen pyranometer SP LITE Silicon Pyranometer, which results in 82 μW/m$^2$ sensitivity and a power density of 1530 W/m$^2$. The current–voltage and capacitance–voltage measurements were performed using a KEYSIGHT 1500 system.

In order to compare the quality of the SiO$_2$ growth in our laboratory, another Al/SiO$_2$/p-Si MIS Schottky diode structure was fabricated on p-type silicon (Si) wafer with (100) orientation, 280 µm of thickness, 2’ of diameter, and resistivity of 1–10 Ω·cm with 200 nm wet thermal oxide made by the foundry.

### 3. Results and Discussion

#### 3.1. Al/SiO$_2$/p-Si MIS Schottky diode structure

Fabricated Al/SiO$_2$/p-Si structures have four fingers pattern with 150 µm of width of each finger and 200 µm of separation between them. Figure 1 shows the fabricated structure. The Cathode is a metallic contact (aluminum) that is on the p-type silicon, between this contact and the SiO$_2$ there is a separation of 10 µm. The anode is a metallic contact (aluminum) deposited onto the SiO$_2$ surface. In order to obtain different active area sizes, for the proposed device, a variation in the separation between layers (Sbl), i.e. the overlap between SiO$_2$ and the Anode contact, was performed, as shown in table 1.
3.2. Current–voltage (I–V) characteristics

For a MIS Schottky diode, the relation between the applied forward bias and current based on the thermionic emission theory is defined by \[11\] and \[18\]:

\[
I = I_O \exp \left( \frac{qV}{nkT} \right) \left[ 1 - \exp \left( \frac{qV}{kT} \right) \right]
\]

where \(q\) is the electron charge, \(V\) is the applied voltage, \(T\) is the temperature in Kelvin, \(k\) is the Boltzmann’s constant, \(n\) is the ideality factor, \(I_O\) is the reverse saturation current obtained from the interception of the straight line of the \(\ln(I)\)-\(V\) plot at \(V = 0\) and is defined as:

\[
I_O = AA^*T^2\exp \left( -\frac{q\Phi_b}{kT} \right)
\]

where \(A\) is the area of the diode, \(A^*\) is the effective Richardson constant and is equal to 32 A cm\(^{-2}\) K\(^2\) for p-type Si [11] and [15], \(\Phi_b\) is the zero-bias barrier height and can be calculated from equation (2) by

\[
q\Phi_b = kT \ln \left( AA^*T/I_O \right)
\]

The ideality factor is calculated from the slope of the linear region of the forward bias region of the \(\ln(I)\)-\(V\) plot and can be determined from equation (1) as:

\[
n = \frac{q}{kT} \frac{dV}{d(\ln I)}
\]

Table 1. Dimensions of the different geometries of the Al/SiO\(_2\)/p-Si structure.

| Sample | Separation between layers (Sbl)(\(\mu\)m) | Active Area Size (10\(^{-3}\) cm\(^2\)) |
|--------|------------------------------------------|---------------------------------------|
| A      | 5                                        | 4.466                                 |
| B      | 10                                       | 4.134                                 |
| C      | 15                                       | 3.804                                 |
| D      | 20                                       | 3.476                                 |

Figure 1. Schematic diagram of the Al/SiO\(_2\)/p-Si structure, (Sbl=separation between layers).

Figure 2 shows the forward and reverse bias regions of the log \(J\)-\(V\) plot of the fabricated structures at room temperature (Samples A and B), under dark and illumination conditions. In the case of sample A, with the insulator growth in our laboratory, it is possible to observe a significant quasi-symmetric behavior of the forward and reverse characteristics of the log \(J\)-\(V\) plot, which shows linear dependence of low bias voltage. For further
forward voltages, the current density curves quickly become dominated by series resistance from contact wires or bulk resistance of the semiconductor [11]. It is worth to notice that the reverse current density under dark has such behavior due to bulk-limited conduction mechanisms or transport-limited conduction mechanisms, which is explained later. Using equations (3) and (4), the values of the ideality factor and the barrier height under dark were found as 1.46 and 0.97 eV, respectively. On the other hand, the obtained current density curve from sample A fabricated with the insulator growth by the foundry, clearly shows that the insulator limits the current density flow from or to the Anode contact. Furthermore, regarding the samples with smaller active area growth on our laboratory, i.e. B, C, and D, it is possible to observe in figure 2 a further decrease of the measured current density under light and dark conditions, which confirms that the conduction mechanism present in sample A has dependence with the active area.

It is worth to point out that an ideality factor value higher than the unit confirms the presence of an interfacial insulator layer between the Anode and the Si substrate interface [11]. Such behavior of the ideality factor is attributed to a particular distribution of the interface states [19]. Furthermore, the barrier height is a parameter of the electrode-limited conduction mechanisms and it depends on the electrical properties at the electrode-dielectric interface [6]. Table 2 shows the ideality factor and the barrier height in dark conditions of reported MIS Schottky diode devices for comparison with the fabricated structure, in this work. In all listed devices, the ideality factor is greater than the unity indicating the presence of a metal-semiconductor interface.

In electronic devices, the Schottky barrier height indicates the minimum required energy for the electrons in the metal to overcome the energy barrier at the metal-dielectric interface and transferred to the dielectric material [6].

The current in forward bias (0–1 V approximately) quickly increases due to series resistance generated from the metallic contacts or bulk resistance at the semiconductor. According to Tataroğlu et al [11], the effect of the series resistance in the linear region could be neglected, due to at low bias voltage (V ≤ 0.3 V) the series resistance has a small value, and therefore the drop voltage across it can be ignored.

The density distribution profile of the interface state (N_{SS}) in equilibrium with the semiconductor is calculated from the forward bias I–V region plot under dark conditions. With the aid of equations (1) and (4), the voltage-dependent ideality factor n(V) is given by:

**Figure 2. Logarithmic I–V characteristics of fabricated structures.**

**Table 2. Barrier height Φ_b, and ideality factor n in MIS Schottky diode structures in dark conditions.**

| Device                        | Barrier height (eV) | Ideality factor (n) | Insulator thickness (nm) |
|-------------------------------|--------------------|---------------------|--------------------------|
| Al/AzureC2 μl cm^{-2}/p-Si    | 0.64               | 1.15                | 500 [20]                 |
| Al/AzureC4 μl cm^{-2}/p-Si    | 0.65               | 1.26                | 3500 [20]                |
| Al/SiO_{2}/p-Si               | 0.786              | 1.766               | 3.3 [11]                 |
| Au/Au(NPs) doped SiO_{2}/p-Si/Al | 0.63               | 1.28                | 170 [15]                 |
| Al/SiO_{2}/p-Si (SampleA)    | 0.97               | 1.46                | 200                      |
Considering the thickness value of the insulator layer $t_{ox}$ and the depletion layer width $W_D$ relationship with $n(V)$ \[11\],

$$n(V) = \frac{qV}{kT \ln(I/I_0)}$$ \[5\]

where $\varepsilon_s = 11.8\varepsilon_0$ is the permittivity of the semiconductor and $\varepsilon_i = 3.8\varepsilon_0$ of the insulator layer, $\varepsilon_0$ is the free space permittivity, then $N_{SS}$ can be deducted as:

$$N_{SS}(V) = \frac{1}{q} \left( \frac{\varepsilon_s}{t_{ox}} (n(V) - 1) - \frac{\varepsilon_i}{W_D} \right)$$ \[6\]

The energy distribution profile of interface states for the fabricated sample A (Al/SiO$_2$/p-Si structure) was obtained from the experimentally forward bias I-V measurements under dark conditions, showed in figure 3. Notice that a slight exponential increase in $N_{SS}$ from mid gap towards the top of the valence band is evident. $N_{SS}$ varies from $1.43 \times 10^{12}$ to $7.66 \times 10^9$ eV$^{-1}$ cm$^{-2}$.

An essential parameter in the type of conduction mechanism is the trap energy level in the dielectric films; such parameter is obtained by the bulk-limited conduction mechanisms or transport-limited conduction mechanisms. This conduction mechanism depends on the electrical properties of the dielectric itself. The bulk-limited conduction mechanisms include (1) Poole-Frenkel emission, (2) hopping conduction, (3) Ohmic conduction, (4) space-charge-limited conduction, (5) ionic conduction, and (6) grain-boundary-limited conduction \[6\].

Poole-Frenkel emission and hopping conduction are often observed at high temperature (e.g. 300 K to 425 K) and at the high electric field (e.g. 0.25 MV cm$^{-1}$ to 1.65 MV cm$^{-1}$). These conduction mechanisms were discarded due to the complexity of the measurement conditions.

The ohmic conduction is caused by the movement of mobile electrons in the conduction band and holes in the valence band, and there is a linear relationship between the current density and the electric field. In dielectric materials the energy band gap is large, however, a small number of carriers may be generated due to the thermal excitation, i.e. the electrons may be excited to the conduction band, either from the valence band or from the impurity level. The ohmic conduction current generated by mobile charges may be observed at very low voltage in the current–voltage I-V characteristic of the dielectric layer. Another indirect way to observe the linear relationship between current density and electric field, indicating the presence of ohmic current, is when the slope value on the I-V curve in the region of low applied voltages ($V \leq V_{tr}$) approximates to 1 \[6\].

The mechanism of space-charge-limited conduction (SCLC) in a solid material is generated by the injection of electrons at an ohmic contact and is similar to the transport conduction of electrons in a vacuum diode and has dependence with the active area \[6\]. Figure 4 shows the $J$–$V$ characteristics in a log–log curve for the space-charge-limited current of sample A at room temperature. The $J$–$V$ characteristic is bounded by three limited...
curves, ohm’s law, traps-filled-limited (TFL) current, and Child’s law, which are described as in [6] by:

\[ J_{Ohm} = \frac{q n_o \mu}{t_{ox}} \]  
\[ J_{TFL} = \frac{9}{8} \mu \varepsilon_i \frac{V^2}{t_{ox}^2} \]  
\[ J_{Child} = \frac{9}{8} \mu \varepsilon_i \frac{V^2}{t_{ox}^2} \]  
\[ V_{tr} = \frac{8 q n_o t_{ox}^2}{9 \varepsilon_i \theta} \]  
\[ V_{TFL} = \frac{q N_t t_{ox}^2}{2 \varepsilon_i} \]  
\[ \tau_d = \frac{t_{ox}^2}{\mu \varepsilon_i V_{tr}} \]  
\[ \tau_e = \frac{\varepsilon_i}{q n_e \mu \theta} \]  
\[ \theta = \frac{N_C}{g_n N_i} \exp \left( \frac{E_i - E_C}{kT} \right) \]

where \( V_{tr} \) and \( V_{TFL} \) are transition voltage at the departure from ohm’s law and TFL curve, respectively and their values can be observed in figure 4. Based on the SCLC model, it was possible to determine some valuable parameters in the SiO\(_2\) growth in our laboratory. For example at room temperature, the trap density, \( N_t \) is calculated from equation (12), being equal to \( 8.093 \times 10^{15} \) cm\(^{-3}\). The mobility, \( \mu \), and the ratio of the free carrier density to total carrier, \( \theta \), are determined by introducing \( V_{tr} \) in equation (11) on equation (8) through replacing \( n_o \) along with equation (9) to form a linear system resulting in \( \mu = 1.01 \times 10^{-6} \) cm\(^2\)/V·s and \( \theta = 1.803 \times 10^{-3} \). Next, by using equation (11), the concentration of the free charge carriers in thermal equilibrium, \( n_o \), is 2.189 \( \times 10^{12} \) cm\(^{-3}\). Furthermore, the maximum of dielectric relaxation time, \( \tau_d \), is 1.58 \( \times 10^{-5} \) s, and the carrier transient time, \( \tau_e \), is 1.098 s, which were calculated by using equations (14) and (13), respectively. Finally, from equation (15) the effective density of states in the conduction band, \( N_C \), is approximately 7.5 \( \times 10^{19} \) cm\(^{-3}\) and the trap energy level, \( E_i \), is 0.25 eV.

According [21], SCLC mechanism in thick thermally oxidized SiO\(_2\) it is due to the formation of Si\(^{3+}\)\(_n\), which implies an increase in Si-rich bonds like dangling bonds or oxygen defects, thus creating more defect states.

Under light conditions, the induced photo generated current on the structure is observed in the region of the second quadrant of \( I–V \) characteristic and the photovoltaic parameters can be calculated. The obtained data are
presented as the power curve, figure 5, which characterizes a solar cell. The values of the short-circuit current ($I_{SC}$), the open-circuit voltage ($V_{OC}$), the voltage at maximum power point ($V_{M}$), and the current at maximum power point ($I_{M}$), for the fabricated device, were determined as $1.28 \mu A$, $0.3 V$, $0.114 V$, $0.68 \mu A$, respectively.

The fill factor ($FF$) of the device is calculated by the following relation [22], with an obtained value of 0.202.

$$FF = \frac{V_{M}I_{M}}{V_{OC}I_{SC}}$$ (16)

Furthermore, the power conversion efficiency ($\eta$) of a solar cell, is defined as the ratio between the maximum output power and the input power of the incident light, $P_{in}$, and can be calculated by:

$$\eta = FF \frac{V_{OC}I_{SC}}{P_{in}A} \times 100\%$$ (17)

where $P_{in}$ is 153 mW cm$^{-2}$ and $A$ the effective active area equal to 4.466 $\times$ 10$^{-3}$ cm$^2$. The efficiency of the proposed device was calculated by equation (17) and found to be 0.0114%.

Comparing the short-circuit current density ($J_{SC}$) of the Au/p-Si/Al structure reported in reference [15] with sample A, fabricated in this work, the values correspond to 10.16 and 0.286 mA cm$^{-2}$, respectively. For separation between layers of 10 and 15 microns in table 1, the values of the $J_{SC}$ are 4.65 and 0.134 nA cm$^{-2}$, respectively. Table 3 shows the electrical parameters of some reported devices. Although the efficiency is low in the fabricated structure on this work, it should be noted that the fabricated structure has a higher open-circuit voltage compared with most of the previously reported devices, which it is due to the presence of the SCLC effect.

3.3. Capacitance–voltage (C–V) characteristics

The C–V characteristic of sample A measured at 1 kHz under dark and illumination conditions is shown in figure 6, for SiO$_2$ growth at the laboratory and by the foundry. In the case of sample A, with a SiO$_2$ growth at the
laboratory, the capacitances at 1 kHz under dark conditions showed negative peaks, as well as a lower capacitance value in the accumulation region compared with the one with the insulator growth by the foundry. This lower capacitance is very commonly observed in devices affected by the SCLC mechanism. As it is possible to observe, at high negative bias and at the dark condition it is not possible to observe a saturation behavior commonly observed in the accumulation region of MIS structure, which is consistent with the Child’s law observed in figure 4. This means that free charges flow from the Anode contact interface into the bottom Silicon substrate through the insulator. Furthermore, in the deep depletion region ($V > 0V$), a negative capacitance is observed meaning that now free charges flow from the Silicon substrate to the Anode contact, which is due to the decrease of the series resistance known as conductivity modulation [24]. Once the device is illuminated, the higher capacitance value is observed due to photogenerated carriers, which are higher than the electrons provided by the anode contact. The same behavior it is possible to observe in the deep depletion region at forward bias. Also, in the accumulation region, there is a high recombination rate of charges at the insulator-Silicon interface due to the accumulated holes. However, a peak of a maximum positive capacitance is observed in the depletion region, which according to figure 3, corresponds to the Trap-Filled-Limited region, allowing to move the photogenerated carriers not only in the Silicon substrate but also in the insulator to the Anode contact with a lower recombination rate at the SiO$_2$ interface with the Silicon compared with the accumulation condition. A negative capacitance peak is also observed, which is due again by the decrease of the series resistance at a certain bias (see figure 11) [24]. Further, considering this behavior, it was determined the value of the built-in-voltage $V_b$ using the plot ($C^2$–$V$) under dark conditions, shown in figure 7. A straight line that intercepts the abscissa axis [15] on the $C^2$–$V$ was used to extract the value of $V_b$ equal to 0.58 eV.

The capacitance measurements of sample A as a function of the frequency in a range from 1 kHz to 1 MHz at room temperature under illumination conditions are shown in figure 8. It is worth to point out that both negative and positive peak is observed only at 1 and 10 kHz, which is in agreement with the obtained value of $\tau_d$ ($f < \tau_d^{-1}$). At higher frequencies, the release rate due to the traps at the insulator and at the interface becomes negligible. The characteristic curve $C$–$V$ for a frequency of 500 kHz is overlapped with the curve of 1 MHz. The minimum capacitance measured at 1 kHz in the depletion region is $-4.16 \times 10^{-12}$ F. The width of the depletion region $W_D$ was determined by equation (18) [12] and [15].

$$W_D = \sqrt{\frac{2\varepsilon_S\varepsilon_0 V_d}{qN_s}}$$  \hspace{0.5cm} (18)

where $V_d$ is the diffusion potential at zero bias and is calculated for equation (19) [12] and [15].

$$V_d = V_b + \frac{kT}{q}$$  \hspace{0.5cm} (19)

The values of $V_d$ and $W_D$ were found 0.606 eV and 1.66 $\times$ 10$^{-3}$ cm, respectively. Under dark conditions, the density of interface states was calculated by equation (7), and it’s on the order of 4.44 $\times$ 10$^{10}$ eV$^{-1}$ cm$^{-2}$. Under light condition, the values of the built-in-voltage $V_{bn}$, the width of the space charge region, the density of interface
states, and the carrier concentration in the substrate are 0.333 eV, 0.192 \times 10^{-3} \text{ cm}, 7 \times 10^{10} \text{ eV}^{-1} \text{ cm}^{-2}, \text{ and } 1.26 \times 10^{14} \text{ cm}^{-3} \text{ respectively.}

Figure 9 shows the measured $G/\omega-V$ characteristics of sample A as a function of the frequency in a range from 1 kHz to 1 MHz at room temperature. The capacitance and the conductance increase with decreasing frequency. The $C-V$ presents negative capacitance peaks at low frequencies, this is because the interface states follow an ac signal, as well as the conductance peak in low frequency indicates the presence of a continuous distribution of the interface states for an applied ac voltage $[25]$ and $[26]$.

According to $[27]$, the density of states ($N_{SS}$) as a function of the frequency can be calculated by using the following:

$$
\frac{G}{\omega} = \frac{qN_{SS}}{2\omega\tau_T} \ln \left[ 1 + (\omega\tau_T)^2 \right]
$$

where $\tau_T$ is the interface trap time constant and $\omega = 2\pi f$ is the angular frequency. Furthermore, according to $[28]$ and $[29]$ the $\partial(G/\omega)/\partial(\omega\tau_T) = 0$ at the $G/\omega$ maxima, which allows determining $N_{SS}$ from sample A with the SiO$_2$ growth in our laboratory as:
Figure 9 also shows \( \frac{G}{\omega} \) vs. voltage for different frequencies, where the inset figure depicts \( N_{SS} \) vs. frequency taken at the maxima value. As it is possible to observe, \( N_{SS} \) varies from \( 3.34 \times 10^{12} \) to \( 4.95 \times 10^{9} \) eV\(^{-1}\) cm\(^{-2}\), which is in fair agreement with figure 3.

The series resistance \( R_S \) of the fabricated structure can be obtained from measurements of \( G-V \) and \( \frac{G}{\omega}-V \) characteristics for strong accumulation in a range from 1 kHz to 1 MHz, which can be calculated by equation (22) [10] and [25] as:

\[
R_S = \frac{G_m}{G_m^2 + (\omega C_m)^2}
\]  

where \( G_m \) and \( C_m \) are the values of the conductance and capacitance in strong accumulation [25].

Figures 10 and 11 show the conductance \( G \) and the series resistance \( R_s \) characteristics of sample A under light condition, respectively. Regarding low-frequency measurements, the series resistance shows a drop from \(-0.5 \) V to \(0.4 \) V and from \(-0.2 \) V to \(0.4 \) V for 1 kHz and 10 kHz frequencies, respectively, which disappears at high frequencies. This behavior at low frequencies is due to the trapped charges, which have enough energy to escape from the traps located at the metal-semiconductor interface in the Si band gap [25] and are the
responsible for the fast decrease of capacitance (see figure 8), which continues until negative peak \[22\] at positive bias values lower than 0.5 V.

Also, the capacitance of the insulator layer \(C_{ox}\) can be obtained by equation \[23\] in the accumulation region [30], where \(d_{ox}\) is the insulator layer thickness.

\[
C_{ox} = \frac{\varepsilon_1 \varepsilon_0 A}{d_{ox}} = C_{m} \left( 1 + \frac{G_{m}^2}{\omega^2 C_{m}^2} \right)
\]  

Table 4 shows the values of the series resistance and the capacitance of the insulator layer, in the accumulation region, for different frequencies ranging from 1 kHz to 1 MHz using equations \[22\] and \[23\].

| Frequency (kHz) | Series resistance (k\(\Omega\)) | Capacitance \(C_{ox}\) (pF) |
|----------------|---------------------------------|-----------------------------|
| 1              | 1,270                           | 35                          |
| 10             | 153                             | 30.2                        |
| 100            | 125                             | 20                          |
| 500            | 73.3                            | 4.45                        |
| 1000           | 36.3                            | 2.66                        |

It is worth to notice that the series resistance and the capacitance of the insulator layer decrease with increasing frequency. At high frequencies, the values of \(R_S\) are smaller than their values at lower frequencies, which indicate the presence of a conductance element due to the SCLC mechanism.

4. Conclusion

In this study, the photoelectric effect on an Al/SiO\(_2\)/p-Si MIS structure has been investigated by varying the active area of a growth thick layer of SiO\(_2\). Thanks to the defects present in the SiO\(_2\) produced by the formation of Si\(^{3+}\), it was possible to observe a Space-Charge-Limited Conduction process, which allows enhancing the photoelectric effect of this kind of structures by given an increase of \(V_{oc}\). Despite that the \(J_{sc}\) value is really low, by increasing the active area, it can be possible to increase this value. Experimental capacitance measurements under illumination also show the effect of the Space-Charge-Limited Conduction through a high positive peak compared with the capacitance in accumulation. This peak can be explained by the strong contribution of trapping and release of carriers, which becomes negligible at high frequencies. Finally, conductivity modulation due to the presence of interface state density is responsible for the negative capacitance values.
Acknowledgments

This work was supported by Semiconductor Device Research Center, Institute of Science Autonomous University of Puebla, Puebla and by Nanoscience and Micro and Nanotechnology Center, National Polytechnic Institute, México D.F.

ORCID iDs

E Saloma @ https://orcid.org/0000-0001-6135-7490
N Hernández-Como @ https://orcid.org/0000-0003-0964-397X
M Chavez @ https://orcid.org/0000-0002-3491-2759
J Alvarado @ https://orcid.org/0000-0001-7186-4429

References

[1] Bell G and Ramachers Y 2017 Photoelectric Solar Power Revisited Joule 1 639
[2] Pantelides S T 1978 The Physics of SiO2 and its Interfaces (New York: Pergamon)
[3] Tseng H H and Wu C Y 1987 Solid State Electron 30 383
[4] Cowley A M and Sze S M 1965 J. Appl. Phys. 36 3212
[5] Depas M, Van Meirhaeghe R L, Lalère W H and Cardon F 1994 Solid State Electron 37 433
[6] Fu-Chien C 2014 A review on conduction mechanisms in dielectric films Advances in Materials Science and Engineering 2014 578168
[7] Kohnen E et al 2019 Sustainable Energy Fuels 3 1995
[8] Mazzarella L, Morales V A B, Hendriks M, Kirner S, Lortsch M and Stannowski B 2017 IEEE Journal of Photovoltaics 8 70
[9] Kar S and Dahlke W E 1972 Solid State Electron 15 221
[10] Nicollian E H and Brews J R 1982 MOS Physics and Technology (New York: Wiley)
[11] Tatarağlu A and Altundal Ş 2006 Microelectronic Engineering 83 582
[12] Sze S M 1981 Physics of Semiconductor Devices (New York: Wiley)
[13] Şahin B, Çetin H and Aydıldız E 2005 Solid-State Commun 135 490
[14] Karataş Ş 2008 J. Non-Cryst. Solids 354 1
[15] Nawar A M and Makhlouf M M 2018 Journal of Alloys and Compounds 767 1271
[16] Karataş Ş, Altundal Ş, Türüt A and Ozmenn A 2003 Appl. Surf. Sci. 217 250
[17] Chattopadhyay P and Raychaudhuri B 1993 Solid State Electron 36 605
[18] Card H C and Rhoderick E H 1971 J. Phys. D. 4 1589
[19] Altundal Ş, Karadeniz S, Tuğluoğlu N and Tatarağlu A 2003 Solid State Electron 47 1847
[20] Orak I, Turut A and Toprak M 2015 Synthetic Metals 200 66
[21] Lee J, Lim K and Kim Y S 2018 Scientific Reports 8 15905
[22] Makhlouf M M, Radwan A S and Gasheh B 2018 Appl. Surf. Sci. 452 337
[23] Rabchi A, Amrani M, Benamaraz Z, Akkal B and Kacha A H 2016 Optik 127 6412
[24] Bisquert J 2011 Phys. Chem. Chem. Phys. 13 4679
[25] Karataş Ş, Yakuphanoğlu F and Amanullah F M 2012 Journal of Physics and Chemistry of Solids 73 46
[26] Akkal B, Benamaraz Z, Gruzza B and Bideux L 2000 Vacuum 57 219
[27] Zhuangzhuang H et al 2020 ECS J. Solid State Sci. 9 025001
[28] Tatarağlu A and Ergüngör U 2016 Indian J Pure Appl Phys. 54 374 http://jop.ipic.res.in/handle/123456789/34405
[29] Baran H M and Tatarağlu A 2013 Chin. Phys. B 22 047303
[30] Gutierrez L R, Romero J J C, Tapia J M P, Calva E B, Flores J C M and Lopez M O 2006 Mater. Lett. 60 3866