Hardware-aware in-situ Boltzmann machine learning using stochastic magnetic tunnel junctions

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One of the big challenges of current electronics is the design and implementation of hardware neural networks that perform fast and energy-efficient machine learning. Spintronics is a promising catalyst for this field with the capabilities of nanosecond operation and compatibility with existing microelectronics. Considering large-scale, viable neuromorphic systems however, variability of device properties is a serious concern. In this paper, we show an autonomously operating circuit that performs hardware-aware machine learning utilizing probabilistic neurons built with stochastic magnetic tunnel junctions. We show that in-situ learning of weights and biases in a Boltzmann machine can counter device-to-device variations and learn the probability distribution of meaningful operations such as a full adder. This scalable autonomously operating learning circuit using spintronics-based neurons could be especially of interest for standalone artificial-intelligence devices capable of
fast and efficient learning at the edge.

Conventional computers use deterministic bits to operate and encode information. While this approach is effective for well-defined tasks like arithmetic operations, there are many difficult tasks like stochastic optimization, sampling, and probabilistic inference which instead are readily addressed by utilizing stochasticity. A promising approach for solving these difficult tasks is using computers which are naturally probabilistic. In a well-known piece, Feynman\(^1\) suggested that in the same way that the use of quantum computers is important to simulate quantum phenomena, a probabilistic computer could be a natural solution to problems which are intrinsically probabilistic. Recently, utilizing spintronics technology, Borders et al.\(^2\) demonstrated such an autonomously running probabilistic computer consisting of probabilistic bits (p-bits) with a stochastic magnetic tunnel junction (s-MTJ) which can perform computationally hard tasks like integer factorization.

Machine learning is another important field in which probabilistic computation and a large amount of random numbers could be highly beneficial. It holds promise for various tasks like image recognition, medical application and autonomous driving\(^3\)–\(^5\). For these applications, conventional von-Neumann computers are inefficient and novel computing architectures inspired by information processing in the human brain are of interest\(^6\)–\(^10\). Boltzmann machines offer a promising route for hardware learning due to their local learning rule and tolerance to stochasticity\(^11\)–\(^15\). Boltzmann machines are generative stochastic recurrent neural networks having a large application space ranging from optimization to generative machine learning\(^16\)–\(^19\). This suggests that building a compact hardware implementation in the form of a probabilistic computer that resembles a Boltzmann machine could be highly beneficial in terms of energy consumption and training speed. While some hardware implementations have been presented for Restricted Boltzmann machines (RBMs)\(^{14,20,21}\), in this paper we focus on fully-connected unrestricted Boltzmann machines. The
usual problem in learning unrestricted Boltzmann machine is that they are hard to train since the equilibrium samples of the network are harder to extract\textsuperscript{18,22}. In this work we show a system that performs this sampling naturally and could hence make it possible to train unrestricted Boltzmann machines more efficiently using the natural physics of s-MTJs.

A common concern for the development of neuromorphic systems based on emerging devices like s-MTJs is the inevitable device variability\textsuperscript{8,23}. This poses an obstacle to deploy these systems for real-world application on a large scale while preserving high reliability. Several approaches have been proposed to overcome these challenges on a device level for example by applying external magnetic fields\textsuperscript{24}, performing a calibration phase\textsuperscript{2} or by post-processing\textsuperscript{25}. Another interesting approach to counter the effect of variability and realize high-performance in neuromorphic systems is to perform training and inference on the same hardware system\textsuperscript{26,27}. In this paper, we present a proof-of-concept demonstration of a probabilistic computer that can perform in-situ learning allowing to counter device-to-device variations naturally as part of its learning process. Here, device variability is addressed on a system’s level. We show that after weights and biases are learned, even devices with non-ideal characteristics can be used to perform given tasks successfully. Such a natural variation-tolerance could enable large-scaled implementations of MTJ-based probabilistic computers.

**Hardware-aware learning with MTJ-based p-bits**

The main building block of a probabilistic computer is the p-bit, analogous to a binary stochastic neuron (BSN)\textsuperscript{28}. Its activation function can be described by\textsuperscript{29}

\[
m_i(t + \tau_N) = \text{sgn} \left( \tanh \left[ I_i(t) \right] - r \right).
\]

(1)

Here, \( m_i \) is a bipolar random variable, \( \tau_N \) is the time the p-bit takes to perform the activation operation, \( I_i \) is the dimensionless input to p-bit \( i \), and \( r \) is a uniformly distributed random number between -1 and +1. Eq.(1) can also be written in binary notation with a unit step function and a
sigmoid function.

To connect multiple p-bits, a synaptic function computes the input of every p-bit $I_i$ by taking the weighted sum of all p-bit outputs $m_i$,

$$I_i(t + \tau_S) = \sum_j W_{ij} m_j(t)$$

(2)

where $\tau_S$ is the synapse execution time and $W_{ij}$ is the weight matrix that couples p-bit $i$ and p-bit $j$. Here, the bias to p-bit $i$ is subsumed into $W_{ii}$. Given a particular weight matrix, every p-bit configuration has a defined probability given by the Boltzmann distribution where $P(m) \propto \exp[-E(m)]$ with energy $E(m) = -\sum W_{ij} m_i m_j$. To find a fitting weight matrix for a given data distribution, the weights are trained by performing gradient ascent of the log-likelihood\textsuperscript{30}. It is well known that the ideal Boltzmann machine algorithm based on log-likelihood learning is generally intractable since learning time scales exponentially with the size of the system\textsuperscript{18,31}. However, it has been shown that approximate version of the Boltzmann learning rule like the contrastive divergence algorithm\textsuperscript{11,12} can be used to perform approximate learning for large Boltzmann machine systems. This algorithmic scaling motivates the use of domain specific, efficient, and fast hardware accelerators like the p-bit building block that naturally represents the neuron function of the Boltzmann machine in order to accelerate the learning process\textsuperscript{32}.

To map the Boltzmann machine learning algorithm to our hardware system, we use a continuous learning rule similar to the persistent contrastive divergence algorithm given by\textsuperscript{33,34},

$$\frac{dW_{ij}}{dt} = \frac{(v_i v_j) - m_i m_j - \lambda W_{ij}}{\tau_L}$$

(3)

that can be implemented by making use of resistor-capacitor (RC) circuits where each weight is stored as a voltage. Here, $\langle v_i v_j \rangle$ is the average correlation between two neurons in the data distribution, $m_i m_j$ is the correlation of the p-bit outputs and $\tau_L$ is the learning time constant. The discharging of the capacitor through resistor $R$ is used to regularize the weights parametrized by $\lambda$. 
Regularization assures that weights do not become too large and helps the algorithm to converge to a solution. This learning rule only requires the correlation between two p-bits $m_i m_j$ for updating weight $W_{ij}$ which makes this learning algorithm attractive for hardware implementations. Eq.(3) does not change when the system becomes larger. Another important advantage of the presented hardware implementation of the Boltzmann machine is that the computational expensive part of getting the equilibrium samples of the correlation term $m_i m_j$ needed for learning is performed naturally. More information about the learning rule is presented in the supplementary information. Note that while we have chosen a RC network in this proof-of-concept experiment to conveniently represent analog voltages as weights, the synaptic functionality in our system could also be implemented out of memristor crossbar arrays\cite{26,35,36} to support in-situ learning by mapping the weight update rule (Eq. (3)) to an equation of changing conductance $G_{ij}$ instead of changing voltage $V_{ij}$. The use of memristor crossbars would have the main advantage that the weight storage becomes non-volatile.

Eqs.(1),(2),(3) are implemented in hardware to build a probabilistic circuit that performs learning naturally. Fig. 1 a shows the block diagram of the learning circuit. The neurons (Eq.(1)) are implemented with an s-MTJ in series to a transistor and a resistor $R_S$. The drain voltage gets thresholded by using a comparator\cite{2,37}. The synapse (Eq.(2)) is implemented by using a microcontroller in conjunction with a digital to analog converter (DAC). To compute the correlation of p-bit outputs $m_i m_j$ an XNOR gate is needed between the p-bit and the learning block (Eq.(3)) where the weights are updated using an RC array. Fig. 1 b shows the printed circuit board (PCB) with the 5 p-bits and the RC-array with 15 RC elements used in the experiment. In the methods section more details about the experimental implementation are presented.

**Variation-tolerant learning of a full-adder**

We demonstrate the learning of the hardware circuit using the data distribution of a full adder (FA).
A FA has 3 inputs and 2 outputs resulting in $N = 5$ p-bits. To connect these p-bits, 10 weights and 5 biases have to be learned (in total 15 RC elements as shown in Fig. 1 b. For the FA, the binary inputs $[ABC_{in}]$ get added and the outputs are given by the sum $S$ and the carry out $C_{out}$. This corresponds to a data distribution that is given by 8 out of the 32 ($2^N$) possible configurations. In the methods section, the truth table and the mapping from truth table to analog voltages $V_{v,ij}$ is explained in detail. For the FA, the learning is performed for a total of 3000 s. In the supplementary information, learning examples for an AND, OR and XOR gate with less p-bits are shown.

**Full adder learning with ideal MTJ.** Fig. 2 a shows the normalized, time averaged p-bit response of every p-bit using the ideal s-MTJ implementation when the input voltage $V_{IN}$ is swept. These s-MTJs are emulated in hardware with two resistances that are randomly selected by a multiplexer (MUX) to obtain nearly ideal p-bit response characteristics (see methods section for more details). Due to variations in the circuit, every curve is slightly shifted from the ideal 50/50 point at $V_{IN} = 1.95$ V. Even though we are using the MUX model here, it has been shown by Borders et al.\textsuperscript{2} that near ideal p-bit responses can be obtained with real s-MTJs. In previous hardware p-circuit implementations, lateral shifts of the p-bit response had to be eliminated by adjusting synaptic biases to calibrate the experiment\textsuperscript{2,38}. By contrast in this demonstration, since the biases are learned during operation, no calibration phase is necessary. This is a significant advantage since learning can account for transistor and s-MTJ variations between p-bits. After obtaining the response of all p-bits, the learning experiment is performed (see methods section for more detail about the experimental procedure).

The goal of the learning process is that the p-bits fluctuate according to a set data distribution. Since at every point in time the p-bits can just be in one bipolar state, to monitor the training progress, the distribution of the p-bits $P_{Exp}(t)$ is observed over a fixed time window of 60 s, normalized to 1 and compared to the ideal distribution of a full adder given by the 8 lines of the truth table (see Table
To compare two probability distributions the Kullback–Leibler divergence (KL-divergence) defined by 
\[ KL(P_{\text{ideal}}||P_{\text{Exp}}) = \sum_m P_{\text{ideal}}(m) \log\left(\frac{P_{\text{ideal}}(m)}{P_{\text{Exp}}(m, t)}\right) \] 
is commonly used\(^{39}\). Fig. 2 d shows the learning performance measured by the KL divergence versus time \(t\). The difference between the ideal data distribution and the experimental distribution decreases significantly in the first 500 s of learning. At the end of learning the KL divergence reaches a value of around 0.2. The experimental distribution at \(t = 0\), \(P_{\text{Exp}}(t = 0)\) is shown in Fig. 2 b. At the start of learning the weights and biases are small and the distribution is close to a uniform random distribution. However, due to slight mismatches in the p-bit response of every individual p-bit (Fig. 2 a) some peaks are more prominent than others. The distribution at the end of learning \(P_{\text{Exp}}(t = 3000 s)\) is shown in Fig. 2 c, where the highest peaks correspond to the correct distribution for the FA, demonstrating the circuit’s ability to learn the given data distribution. We note that as long as the learned peaks are about equal, the KL divergence can be reduced further by increasing all weight values equally i.e. decreasing the temperature of the Boltzmann machine.

In Fig. 3, the 10 weights voltages across the capacitors \(V_{ij} = V_{v,ij} - V_{C,ij}\) extracted from the circuit are shown. The weights are measured throughout the whole learning process. The blue lines show the weight voltages for the ideal MTJ. After around 500 s the weights saturate and do not change anymore. In the supplementary material, the weights values are compared to the weight matrix commonly used for the FA in logic applications.

**Full Adder learning with non-ideal MTJ.** To examine the effects of variability, we investigate the learning experiment implemented with fabricated s-MTJs (see methods section for more details). Fig. 2 e shows the \(V_{\text{OUT}}\) versus \(V_{\text{IN}}\) characteristics for the 5 MTJ-based p-bits averaged over 15 s. At the transition point between the stochastic and the deterministic region of the response curve, the slope of the response is sharper compared to the center of the curve, which shows a gradual increase. The combination of these two characteristics leads to a non-ideal p-bit response.
that deviates from the ideal response described by Eq. (1). The reason for the distorted shape of the p-bit response is due to the fact that the MTJs show stochastic behavior for a large window of current flow in the order of $> 10 \, \mu A$. The change of the current flow in the MTJ/transistor branch due to change voltage at the gate of the transistor is not large enough to pin the MTJ to $R_P$ or $R_{AP}$ state. This leads to the distorted shape of the p-bit response in Fig. 2 e. For best MTJ characteristics, the stochastic range for current flow should be in the order of around $5 \, \mu A$ in the design used here.

Fig. 2 f and g show the histogram of $P_{Exp}$ during the first and last 60 s of learning. At the end of learning the 8 desired peaks are the largest, showing that even though the learning algorithm is based on an ideal p-bit response derived from the Boltzmann distribution, the circuit can still learn the desired functionality. Despite the noted non-idealities, the KL divergence saturates to a level comparable between ideal and non-ideal MTJ as shown in Fig. 2 d. This can be explained by the fact that in-situ learning has the capabilities to counter device-to-device variations by adjusting weights and biases to fit the system (see supplementary information for more details on the learned bias voltages).

In Fig. 3, the red lines show the weight voltages of the non-ideal MTJ over the duration of the learning process. It can be clearly seen that the weights differ significantly between the ideal and non-ideal p-bit implementation while achieving similar performance in the KL-divergence, leading to the conclusion that feedback in the system between data and p-bit outputs is able to learn around variations, a crucial ingredient to achieve a high level of performance under device variability. In the supplementary information a system simulation on the MNIST dataset is presented to show that the variation tolerance exists when the proposed circuit is scaled up.

The fact that the circuit can learn around variations can be useful not just for classical machine learning tasks like classification or unsupervised learning but also for tasks that have been demonstrated on probabilistic computers like optimization$^{2,40}$, inference$^{41,42}$ or invertible logic$^{24,29}$. Instead of externally setting the coupling between p-bits, an additional learning task could improve
the performance of the p-circuit by assuring that the coupling between the p-bits is adjusted to the exact hardware p-bit response. In addition, the proposed hardware can be used to represent many different distinct probability distributions by adjusting the coupling between p-bits accordingly.

For the particular combination of MTJ and transistor, voltage change at the input can change the output of the p-bit on a transistor response time scale. Because the transistor response can be faster than the implemented synapse, for this particular experiment each p-bit was updated sequentially through the microcontroller instead of autonomously to preserve functionality (see Ref.43 for more details).

**Weight extraction.** In the previous sections, we compared the distribution of the output configurations of the hardware p-bits averaged over 60 s with the ideal distribution by taking the Kullback-Leibler divergence. In this section we compare how the weights extracted as voltages across the capacitors in the circuit would perform on an ideal platform i.e. to the Boltzmann distribution where $P(m) \propto \exp[-\beta E(m)]$ and $\beta$ is the inverse temperature of the system. The temperature in a Boltzmann machine is a constant factor that all weights and biases are multiplied with and represents how strongly coupled the p-bits are with each other. The comparison has particular relevance since the non-ideal effects during learning should have an effect on the weights compared to the weights that would be learned on an ideal machine. Fig. 4 shows the Boltzmann distribution with the weights of Fig. 3. The conversion factor between the voltages $V$ across the capacitors and dimensionless weights $W$ of the Boltzmann distribution represented by the temperature factor $\beta$ was chosen in a way that the relative difference between the peaks of the distribution can be seen clearly. To reduce the effect of noise, the weight values are averaged over the last 10 s of learning. For the example of the FA, it is known from the truth table that an ideal system has no bias. Hence, we do not use the extracted bias but set it to 0 for the Boltzmann distribution. In Fig. 4 a it can be clearly seen that compared to Fig. 2 c the learned distribution differs more from the ideal distribution since the peaks are not as uniform. The peaks for
configuration $[ABC_{\text{in}}] = 000, [C_{\text{out}}S] = 00$ and $[ABC_{\text{in}}] = 111, [C_{\text{out}}S] = 11$ are not as prominent as the other 6 peaks that have been learned. This discrepancy becomes even more visible in Fig. 4 b compared to Fig. 2 g where the weights used in the Boltzmann distribution were learned using a less ideal response of the p-bits. Here, only peaks $[ABC_{\text{in}}] = 000, [C_{\text{out}}S] = 00$ and $[ABC_{\text{in}}] = 111, [C_{\text{out}}S] = 11$ are prominent. This shows that the learned weights fit to the activation of the hardware p-bits but not for the ideal Boltzmann distribution. Hence, we can conclude that the probabilistic computer adapted to the non-ideal p-bit response during the in-situ learning process.

The results presented in this section suggest that learning and inference must be performed on the same hardware to operate reliably. In contrast, initially training on this non-ideal machine, then transferring the weight values to an ideal system to complete convergence and perform the programmed task could allow for a hardware-based speed-up of the typically time-consuming weight training step. This is similar in spirit to using pre-trained weights in a neural network$^{44,45}$. While this can be a disadvantage, the advantages of using the efficient and compact learning circuit that can be used for training and inference should outweigh the problems of transferability between platforms.

In this section, we have shown that device-to-device variations can be countered by performing hardware aware in-situ learning by comparing the learning performance of two systems, one system with ideal p-bit responses and the other with non-ideal p-bit responses that differ significantly compared to Eq.(1). We have shown that the overall performance is the same for both systems after the training is finished while the learned weights (Fig. 3) are different. However, we have also shown that if the weights are extracted from the learning circuit and used to calculate the Boltzmann distribution, the obtained distribution differs substantially from the desired data distribution (Fig. 4 b). These observations show clearly that the circuit can learn around device-to-device variations.

**Discussion**

In this paper, we have presented for the first time a proof-of-concept demonstration of an
autonomously operating fully connected Boltzmann machine using MTJ based p-bits. Furthermore, we have shown how device-to-device variations can be countered by performing hardware aware in-situ learning. In the following paragraphs, we compare the presented probabilistic computer with other platforms like conventional CMOS architectures.

On the device level, the closest digital CMOS alternative to the MTJ-based p-bit is a linear feedback shift register (LFSR), without considering the analog tunability of the p-bit. A detailed comparison between p-bit versus LFSR has been performed by Borders et al.² The compact MTJ-based p-bit uses around 10x less energy per random bit and has about 300x less area than a 32-bit LFSR. Besides these advantages, a standard LFSR is not tunable like the hardware p-bit and relies on pseudo randomness. The p-bit based on an s-MJT relies on thermal noise and is, hence, a true random number generator. This can be significant for applications for which the quality of the randomness is important.

On the system level, the p-bits in combination with the synapse (Eqs.(1) and (2)) are utilized to collect samples of the distribution given by the current weights to update the weights according to the correct gradient. Collecting statistics by sampling drives the learning process since every sample is directly utilized to update the weight voltages (Eq.(3)). Thus, the numbers of samples per unit time are significant for the speed of the learning process. The MTJ fluctuation time of the p-bit \( \tau_N \) is a significant time scale for the generation of samples since it describes how fast Eq.(1) can be computed in hardware. The learning time constant \( \tau_L \) has to be larger than the MTJ fluctuation time \( \tau_N \) to collect enough statistics to ensure convergence of the learning process. To ensure that every p-bit input is correctly calculated based on the state of the other p-bits, it is important that the synapse time \( \tau_S \) is smaller than \( \tau_N \). In this experiment, since the synapse time defined by the microcontroller is in the order of 100 \( \mu s \) to 1 ms, \( \tau_N \) is in the order of 10 – 100 ms which results in slow training in the order of \( 10^3 \) s. However, it has to be noted that the time scales of the circuit can be reduced significantly in an integrated version of the proposed circuit where the synapse
based on crossbar architectures can operate with GHz speeds with execution times down to 10 ps\textsuperscript{43,46,47} and the fluctuation time of s-MTJs can be in the order of 100 ps\textsuperscript{48–50}. This would allow a substantial decrease of $\tau_L$ and an increase of the learning speed by up to 9 orders of magnitude. Regarding energy consumption of the synapse block, the efficient p-bit building block presented here can be combined with any synapse option that provides the most power efficiency. The RC array used here to represent weights as voltages requires a constant memory refresh similar to mainstream dynamic random-access memory (DRAM). To save energy during the learning process, the presented p-bit building block could be combined with non-volatile synapse implementations like memristive crossbar arrays\textsuperscript{13,14,47} The overall power consumption can be estimated using numbers from the literature. The MTJ-based p-bit consumes about 20 $\mu$W\textsuperscript{49}. In a memristive crossbar, each memristor consumes about 1.25 $\mu$W and operational amplifiers around 3 $\mu$W\textsuperscript{26,43,47}. The XNOR operation consumes 10 $\mu$W. For the overall circuit with 5 p-bits, 15 XNOR-gates and memristors, and 5 operational amplifiers would take approximately 294 $\mu$W. This is the projected power consumption of a fully-connected Boltzmann machine hardware shown in this work. For specified applications where less weight connections between neurons are needed (for example restricted Boltzmann machines in digital computers), the number of components can be reduced which results in improved power consumption. In this regard, the estimated power consumption of 294 $\mu$W in our work can also be significantly reduced by employing a higher-level approach.

Another significant advantage of the probabilistic circuit is that due to the compactness and area savings of the p-bit, when scaling up, many more p-bits can be put on a chip compared to CMOS alternatives like LFSRs. In addition, the p-bit hardware implementation does not rely on any clocking in order to function and is hence autonomously operating. This has the advantage that many autonomously operating p-bits can function in parallel leading to an overall acceleration of the operation. In this context, it has to be noted that the information of the current state of a p-bit has to be propagated to all other p-bits that are connected to it on a time scale $\tau_S$ that is much shorter.
than the neuron time $\tau_N$ for the probabilistic circuit to function properly. When the p-bit fluctuation time varies between different p-bit it has to be assured that the fastest p-bit with fluctuation time $\tau_{N,f}$ fluctuates slower than $\tau_S$. Depending on the sparsity of the weight matrix and the ratio of $\tau_S$ to $\tau_N$, the number of parallel operating p-bits has to be adjusted to ensure fidelity of the operation$^{43}$. In a recent paper by Sutton et al.$^{43}$ an FPGA design was implemented that emulates a probabilistic circuit where the MTJ based p-bit is envisioned as a drop-in replacement. In this complete system-level hardware realization of a p-computer that can only perform inference not learning, a drastic reduction in area footprint of the compact p-bit design compared to digital implementations was confirmed. This shows that an integrated version of the proposed learning circuit based on the p-computer architecture could be very beneficial.

While we have addressed that device-to-device variations of the shape and shift of the p-bit response can be accounted for by hardware-aware learning, it is important to note that rate variation of the stochastic MTJ between p-bits cannot be reduced by this approach. The system will in the worst case learn as fast as the fluctuation rate of the slowest p-bit $\tau_{N,s}$ which can slow down the overall operation. However, in the case of p-bits with stochastic MTJs where the thermal barrier of the magnet in the free layer is in the order of $\approx k_B T$, the fluctuation rate does not go exponentially with the size of the magnet making the system less susceptible to rate variations$^{48,49,52,53}$. It has to be noted that a way to reduce rate variation in probabilistic circuits based on stable MTJs that are biased using voltages and magnetic fields has been presented by Lv et al.$^{24}$ As overall design criteria for the autonomous circuit the following conditions have to be met: $\tau_S \ll \tau_{N,f}$ and $\tau_{N,s} \ll \tau_L$.

In conclusion, we have shown a proof-of-concept demonstration of a fully connected probabilistic computer built with MTJ-based p-bits that can perform learning. We have presented multiple learning examples for up to 5 p-bits and 15 learning parameters. The learning is robust and can operate even with strong device-to-device variations due to hardware-aware learning. This shows that when scaled up and with faster fluctuating building blocks, probabilistic computers
could accelerate computation while reducing energy cost for a wide variety of tasks in the machine learning field such as generative learning or sampling, as well as for tasks that could benefit from variation tolerance like optimization or invertible logic.

**Methods**

**MTJ fabrication & Characterization.** The MTJs used in this work are fabricated with a stack structure as follows, from the substrate side: Ta(5)/ Pt(5)/ [Co(0.4)/Pt(0.4)]6/ Co(0.4)/ Ru(0.4)/ [Co(0.4)/Pt(0.4)]2/ Co(0.4)/ Ta(0.2)/ (Co0.25Fe0.75)75B25(1)/ MgO/ (Co0.25Fe0.75)75B25(1.7)/ Ta(5)/ Ru(5)/ Ta(50). The numbers in parentheses are the nominal thicknesses in nanometers. All films are deposited on a thermally oxidized silicon substrate by dc and rf magnetron sputtering at room temperature. The stacks are then processed into circular MTJs with nominal junction size of 20-25 nm in diameter by electron beam lithography and argon ion milling. The samples are annealed at 300°C in vacuum for an hour. MTJs are then cut out from wafers and bonded with wires to IC sockets to be placed in the p-bit circuit board. To determine non-ideal MTJs with suitable characteristics, the MTJ resistance is measured by sweeping the current from negative to positive values, and the time-averaged and high-frequency signals are read across a voltmeter and oscilloscope, respectively. We measure an approximate tunnel magnetoresistance ratio of 65% fluctuating between an average $R_P = 18$ kΩ and $R_{AP} = 30$ kΩ. The current at which the resistance switches by half is determined to be $I_{50/50}$, which is the bias current at which the MTJs will spend equal time in the P and AP states. The $I_{50/50}$ used in this work ranges from 3 to 5 µA. We measure the average fluctuation time $\tau_N$ by performing retention time measurements when the MTJ is in either the high (AP) or the low (P) state using voltage readings from the oscilloscope. To ensure reliable collection of data, the oscilloscope sampling rate is set ten times faster than the fastest recorded fluctuation time of the MTJ. The retention times used in this work range from 10 ms to 100 ms.
Hardware implementation of the p-bit. Eq. (1) is implemented with the s-MTJ based p-bit proposed by Camsari et al.\textsuperscript{37} and experimentally demonstrated by Borders et al.\textsuperscript{2} The p-bit implementation in this paper follows Ref. \textsuperscript{2} and is built with an s-MTJ in series to a transistor (2N7000,T0-92-3 package) and a source resistor $R_S$. The supply voltage is set to $V_{DD} = 200$ mV. The source resistance $R_S$ is chosen so that $I_{50/50}$ is flowing through the circuit when $V_{IN,0} = 1.95$ V. The voltage at the drain of the transistor is then thresholded using a comparator (AD8694, 16-SOIC package). The reference voltage is chosen to be $V_{REF} = V_{DD} - I_{50/50} \frac{R_P + R_{AP}}{2}$. We have used a comparator to add another node where we can fine tune $V_{REF}$. However, in an integrated circuit the transistor should be chosen so that $V_{REF} = V_{DD}/2$ as simulated in references \textsuperscript{34,37,49}. The overall p-bit is then just built with 1 MTJ and 3 transistors. For the experiment with ideal MTJs, the s-MTJ is emulated by a multiplexer (MUX) model that includes all major characteristics of a real s-MTJ and has been developed by Pervaiz et al.\textsuperscript{38} as illustrated in Fig. 5. The s-MTJ is emulated by providing a noise signal to the MUX where the statistics of the noise depend on $V_{IN}$ and are generated using a microcontroller that switches between a resistor $R_P$ and $R_{AP}$ representing the two resistive states of the s-MTJ. Here, the resistors values are chosen to be $R_P = 11$ kΩ and $R_{AP} = 22$ kΩ. The advantage of this approach is that the MTJ parameters like stochastic range and resistance can be easily manipulated in this model. For the MUX, a MAX 394 quad analog multiplexer is used.

Implementation of the synapse. The synapse is implemented with an Arduino MEGA microcontroller and an 8-channel PMOD DA4 Digital-Analog-Converter. The digital output voltages of the p-bits $\{V_{OUT}\}$ are fed into the microcontroller together with the analog weight voltages $\{V_C\}$ of the learning circuit. The internal Analog-Digital-Converter (ADC) of the microcontroller is used for sensing the weight voltages. Eq.(2) is then computed and the analog input voltages $\{V_{IN}\}$ are wired back to the neurons by utilizing the DAC. To reduce the synapse
time in every iteration of the synapse operation, only one of the 15 analog voltages are read out and updated. This does not affect the circuit performance since the capacitor voltages $V_C$ are changing slowly. The synapse operation time $\tau_S$ is $< 1$ ms which is faster than the MTJ fluctuation time. The condition $\tau_S \ll \tau_N$ has to be satisfied to ensure fidelity of the autonomous operation of the p-circuit.

**Implementation of weight updating.** Eq.(3) can be written into circuit parameters$^{34}$

$$C \frac{dV_{ij}}{dt} = \frac{V_{v,ij} - V_{m,ij} - V_{ij}}{R}$$

(4)

with $\langle v_i v_j \rangle = V_{v,ij}/(V_D/2)$ and $m_i m_j = V_{m,ij}/(V_D/2)$. Eqs.(3) and (4) can be converted into each other by setting $W_{ij} = A_v V_{ij}/V_0$, $\lambda = V_0/(A_v V_D/2)$ and $\tau_L = \lambda RC$ where $A_v$ is a voltage gain factor between the voltage across the capacitor and the used weight value for the weighted sum in Eq.(2). This voltage gain is used to adjust the regularization parameter $\lambda$ for the update rule Eq.(3). High $\lambda$ produces smaller weight values during learning. For the FA experiment, $A_v$ is chosen to be 3 which turned out to be a reasonable value for achieving a good degree of regularization while achieving high peaks in the learned distribution. The voltage $V_0$ is the reference voltage of the p-bit response defined by $I_i(t) = V_{IN}(t)/V_0$. The full RC element is depicted in Fig. 1. For proper operation it is important that the learning time constant $\tau_L$ is much larger than the neuron time $\tau_N$. To achieve this, a high RC-constant is chosen with a 1 M$\Omega$ resistor and a 10 $\mu$F capacitor. Since this circuit has a high resistance in series to the capacitor, to ensure that the reading of the weight voltage does not discharge the capacitor, a buffer stage is used between the capacitor and the synapse. The buffer is implemented with an operational amplifier (AD8694, 16-SOIC package).

For learning the correlations $m_i m_j$, represented by voltage $V_{m,ij}$, are crucial. To obtain the current correlations between neuron $m_i$ and $m_j$ their product has to be computed. This is done here by using another microcontroller. Since the output $m$ is bipolar ($m \in \{-1, 1\}$) only negative or positive correlation is possible. Voltage $V_{m,ij}$ is limited by the output voltages of the DAC which
has a range from 0 V to 2.5 V. $V_{m,ij}$ can hence be calculated by solving $V_{m,ij} = (m_im_j + 1)/2 \cdot 2.5$ V. Voltage $V_{m,ij}$ is fed back to the corresponding RC element by utilizing another DAC. The described operation is the same as computing the XNOR operation between two binary variables. Hence, the operation is straightforward and the programmability of the microcontroller not essential for operation of the circuit.

**Experimental procedure.** Before the start of training the capacitor is fully discharged so that $V_{C,ij}(t = 0) = V_{v,ij}$ corresponding to $V_{ij} = 0$ (compare Fig. 3). At $t = 0$ the training starts, and voltage $V_C$ and the p-bit output voltages are measured at sampling frequency $f_S$. The training is run for $T = 3000\text{s}$.

The data is collected with an NI USB-6351 X SERIES DAQ, that has analog inputs for the 15 weights and biases and digital inputs for the 5 p-bit outputs. The software Labview is utilized to record data with a sampling frequency of $f_S = 1 \text{kHz}$.

In this paper we have trained the bias due to mismatch of p-bit responses together with the bias needed to learn the data distribution. In principle, these can be separated to obtain a better bias value that can be used on other platforms. However, this separation of calibration and learning is only possible for the bias of every p-bit and not for the weights connecting them since the calibration cannot be performed with ideal p-bit responses with the hardware system.

**Mapping of truth table to node voltages for learning.** For a fully visible Boltzmann machine with $N$ neurons, $(N + 1)N/2$ weights and biases have to be learned. Depending on the size of the data vectors that should be learned $(N + 1)N/2$ RC elements/memristors and $(N + 1)N/2$ XNOR-gates while $N$ p-bits (3 transistors and 1 s-MTJ) and $N$ operational amplifiers for current summation are needed in the full integrated version of this circuit. The goal for learning is that the fully trained network has the same distribution as the data distribution. For a FA, the data distribution is given by the truth table shown in table I.
The data distribution can be described by a matrix in which the number of columns is equal to the number of neurons \( N \) and the number of rows is equal to the number of training examples \( d \). For the biases, another neuron unit with value 1 is added so that there are \((N + 1)\) columns. For the example of a full adder (FA), \( N = 5 \) and \( d = 8 \) for 8 lines in the truth table. The matrix \( V_{\text{FA}} \) is then a 6x8 matrix where all 0s of the truth table are converted to −1s since we are using the bipolar representation:

\[
V_{\text{FA}} = \begin{bmatrix}
-1 & -1 & -1 & -1 & 1 \\
-1 & -1 & 1 & 1 & -1 & 1 \\
-1 & 1 & -1 & 1 & -1 & 1 \\
-1 & 1 & 1 & -1 & 1 & 1 \\
1 & -1 & -1 & 1 & -1 & 1 \\
1 & -1 & 1 & -1 & 1 & 1 \\
1 & 1 & -1 & -1 & 1 & 1 \\
1 & 1 & 1 & 1 & 1 & 1 \\
\end{bmatrix}
\]

The density matrix is then calculated by computing \( D = V^T V / d \) which is a 6x6 matrix for the FA:

\[
D_{\text{FA}} = \frac{V_{\text{FA}}^T V_{\text{FA}}}{d} = \begin{bmatrix}
1 & 0 & 0 & 0 & 0.5 & 0 \\
0 & 1 & 0 & 0 & 0.5 & 0 \\
0 & 0 & 1 & 0 & 0.5 & 0 \\
0 & 0 & 0 & 1 & -0.5 & 0 \\
0.5 & 0.5 & 0.5 & -0.5 & 1 & 0 \\
0 & 0 & 0 & 0 & 0 & 1 \\
\end{bmatrix}
\]

with \( d = 8 \). The values in the last column of the density matrix correspond to the average value of every neuron in the data distribution and are used to learn the biases. Only the terms above the diagonal of \( D \) are needed and converted to voltages \( V_{v,ij} \) in the circuit. Since the DAC operates with positive voltages in the range of 0 V to 2.5 V, \( V_{v,ij} = (D_{ij} + 1) / 2 \cdot 2.5 \) V.

**Data availability**

The datasets generated and analyzed during this study are available from the corresponding authors on reasonable request.
References

1. Feynman, R. P. Simulating physics with computers. *Int J Theor Phys* 21, (1982).
2. Borders, W. A. *et al.* Integer factorization using stochastic magnetic tunnel junctions. *Nature* 573, 390–393 (2019).
3. LeCun, Y., Bengio, Y. & Hinton, G. Deep learning. *nature* 521, 436 (2015).
4. Schmidhuber, J. Deep learning in neural networks: An overview. *Neural Netw.* 61, 85–117 (2015).
5. Davies, M. *et al.* Loihi: A Neuromorphic Manycore Processor with On-Chip Learning. *IEEE Micro* 38, 82–99 (2018).
6. Hinton, G. E. Training products of experts by minimizing contrastive divergence. *Neural Comput.* 14, 1771–1800 (2002).
7. Aarts, E. H. L. & Korst, J. H. M. Boltzmann machines and their applications. in *PARLE Parallel Architectures and Languages Europe* (eds. Bakker, J. W., Nijman, A. J. & Treleaven, P. C.) vol. 258 34–50 (Springer Berlin Heidelberg, 1987).
8. Osborn, T. R. Fast Teaching of Boltzmann Machines with Local Inhibition. in *International Neural Network Conference: July 9–13, 1990 Palais Des Congres — Paris — France 785–785* (Springer Netherlands, 1990), doi:10.1007/978-94-009-0643-3_76.
9. Srivastava, N. & Salakhutdinov, R. R. Multimodal Learning with Deep Boltzmann Machines. in *Advances in Neural Information Processing Systems* 25 (eds. Pereira, F., Burges, C. J. C., Bottou, L. & Weinberger, K. Q.) 2222–2230 (Curran Associates, Inc., 2012).
10. De Rose, R. *et al.* Variability-Aware Analysis of Hybrid MTJ/CMOS Circuits by a Micromagnetic-Based Simulation Framework. *IEEE Trans. Nanotechnol.* 16, 160–168 (2017).
11. Lv, Y., Bloom, R. P. & Wang, J.-P. Experimental Demonstration of Probabilistic Spin Logic by Magnetic Tunnel Junctions. *IEEE Magn. Lett.* 10, 1–5 (2019).

19
25. Qu, Y. et al. Variation-Resilient True Random Number Generators Based on Multiple STT-MTJs. *IEEE Trans. Nanotechnol.* **17**, 1270–1281 (2018).

26. Li, C. et al. Efficient and self-adaptive in-situ learning in multilayer memristor neural networks. *Nat. Commun.* **9**, 1–8 (2018).

27. Dalgaty, T., Castellani, N., Querlioz, D. & Vianello, E. In-situ learning harnessing intrinsic resistive memory variability through Markov Chain Monte Carlo Sampling. *ArXiv200111426 Cs* (2020).

28. Ackley, D. H., Hinton, G. E. & Sejnowski, T. J. A learning algorithm for Boltzmann machines. *Cogn. Sci.* **9**, 147–169 (1985).

29. Camsari, K. Y., Faria, R., Sutton, B. M. & Datta, S. Stochastic p-bits for invertible logic. *Phys. Rev. X* **7**, 031014 (2017).

30. Koller, D. & Friedman, N. *Probabilistic Graphical Models: Principles and Techniques*. (MIT Press, 2009).

31. Nair, V. & Hinton, G. E. Implicit Mixtures of Restricted Boltzmann Machines. 8.

32. Hamilton, K. E. et al. Accelerating Scientific Computing in the Post-Moore’s Era. *ACM Trans. Parallel Comput.* **7**, 6:1–6:31 (2020).

33. Tieleman, T. Training restricted Boltzmann machines using approximations to the likelihood gradient. In *Proceedings of the 25th international conference on Machine learning - ICML ’08* 1064–1071 (ACM Press, 2008). doi:10.1145/1390156.1390290.

34. Kaiser, J., Faria, R., Camsari, K. Y. & Datta, S. Probabilistic Circuits for Autonomous Learning: A simulation study. *Front. Comput. Neurosci.* **14**, (2020).

35. Ambrogio, S. et al. Equivalent-accuracy accelerated neural-network training using analogue memory. *Nature* **558**, 60 (2018).

36. Mahmoodi, M. R., Prezioso, M. & Strukov, D. B. Versatile stochastic dot product circuits based on nonvolatile memories for high performance neurocomputing and neurooptimization. *Nat. Commun.* **10**, 1–10 (2019).

37. Camsari, K. Y., Salahuddin, S. & Datta, S. Implementing p-bits With Embedded MTJ. *IEEE Electron Device Lett.* **38**, 1767–1770 (2017).

38. Pervaiz, A. Z., Datta, S. & Camsari, K. Y. Probabilistic Computing with Binary Stochastic Neurons. in 2019 IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS) 1–6 (2019). doi:10.1109/BCICTS45179.2019.8972719.

39. Kullback, S. & Leibler, R. A. On Information and Sufficiency. *Ann. Math. Stat.* **22**, 79–86 (1951).

40. Sutton, B., Camsari, K. Y., Behin-Aein, B. & Datta, S. Intrinsic optimization using stochastic nanomagnets. *Sci. Rep.* **7**, (2017).

41. Faria, R., Kaiser, J., Camsari, K. Y. & Datta, S. Hardware Design for Autonomous Bayesian Networks. *ArXiv200301767 Cs* (2020).

42. Faria, R., Camsari, K. Y. & Datta, S. Implementing Bayesian networks with embedded stochastic MRAM. *AIP Adv.* **8**, 045101 (2018).

43. Sutton, B. et al. Autonomous Probabilistic Coprocessing with Petaflips per Second. *IEEE Access* 1–1 (2020) doi:10.1109/ACCESS.2020.3018682.

44. Hinton, G. E. & Salakhutdinov, R. R. A better way to pretrain deep boltzmann machines. in *Advances in Neural Information Processing Systems* 2447–2455 (2012).

45. He, K., Girshick, R. & Dollar, P. Rethinking ImageNet Pre-Training. in *2019 IEEE/CVF International Conference on Computer Vision (ICCV)* 4917–4926 (IEEE, 2019). doi:10.1109/ICCV.2019.00502.

46. Peng Gu et al. Technological exploration of RRAM crossbar array for matrix-vector multiplication. in *The 20th Asia and South Pacific Design Automation Conference* 106–111 (2015). doi:10.1109/ASPDAC.2015.7058989.

47. Cai, F. et al. Harnessing Intrinsic Noise in Memristor Hopfield Neural Networks for Combinatorial Optimization. 24.

48. Kaiser, J. et al. Subnanosecond Fluctuations in Low-Barrier Nanomagnets. *Phys. Rev. Appl.* **12**, 054056 (2019).

49. Hassan, O., Faria, R., Camsari, K. Y., Sun, J. Z. & Datta, S. Low-Barrier Magnet Design for Efficient Hardware Binary Stochastic Neurons. *IEEE Magn. Lett.* **10**, 1–5 (2019).

50. Pufall, M. et al. Large-angle, gigahertz-rate random telegraph switching induced by spin-
momentum transfer. *Phys. Rev. B* **69**, (2004).

51. Li, B. *et al.* Memristor-based approximated computation. in *International Symposium on Low Power Electronics and Design (ISLPED)* 242–247 (2013). doi:10.1109/ISLPED.2013.6629302.

52. Brown, W. F. Thermal Fluctuations of a Single-Domain Particle. *Phys. Rev.* **130**, 1677–1686 (1963).

53. Coffey, W. T. & Kalmykov, Y. P. Thermal fluctuations of magnetic nanoparticles: Fifty years after Brown. *J. Appl. Phys.* **112**, 121301 (2012).

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**Author contribution**

K.Y.C., S.F., H.O. and S.D. planned the study. J.K., K.Y.C. and S.D. developed the mapping of learning algorithm and the experimental setup. W.A.B. and S.F. prepared and characterized the MTJ devices. J.K. and K.Y.C. conducted the learning experiment and collected results. All authors contributed to the writing of the manuscript. All authors discussed the results.

**Competing interests**

The authors declare no competing interests.

**Additional information**

**Supplementary information** is available for this paper.
Figure 1: **Probabilistic Learning Circuit**: a Block diagram of the learning circuit. b A photograph of the PCB with the 5 p-bits (each consisting of an s-MTJ, an NMOS transistor and a source resistor $R_S$) and 15 RC elements and 20 operational amplifiers (5 used as a comparator and 15 as a buffer). The p-bits are interconnected with the RC-array as shown in a.

Figure 2: **Full Adder (FA) learning**: a Response of ideal MTJ for the 5 p-bits used in the FA. Every point is averaged over 15 s. b Experimental distribution of ideal MTJ for the first 60 s of learning. c Experimental distribution of ideal MTJ over the last 60 s of learning. d KL-divergence between ideal and experimental distribution vs. time of ideal and non-ideal MTJ. The experimental distribution is obtained over 60 s of learning. e Response of non-ideal MTJ for the 5 p-bits used in the FA. Every point is averaged over 15 s. f Experimental distribution of non-ideal MTJ for the first 60 s of learning. g Experimental distribution of non-ideal MTJ over the last 60 s of learning.
Figure 3: **Weight voltages during FA learning:** The 10 weight voltages are shown during the 3000 s of learning. Blue lines are the weights learned with the ideal MTJ; red lines show the weights for the non-ideal MTJ. The solid lines in the middle are the moving average of the actual weights taken over a window of 10 s.

Figure 4: **Boltzmann distribution obtained from learned weights:** a Boltzmann distribution computed by using the learned weights of the FA with the ideal s-MTJ p-bits. b Boltzmann distribution computed by using the learned weights of the FA with the real s-MTJ p-bits.
Figure 5: **MUX model**: The s-MTJ based p-bit on the left is modeled by a multiplexer that switches randomly between $R_P$ and $R_{AP}$ but as a function of $V_{IN}$ so that the right statistics are preserved.\(^{46}\)

| $A$ ($v_1$) | $B$ ($v_2$) | $C_{in}$ ($v_3$) | $S$ ($v_4$) | $C_{out}$ ($v_5$) | $P_{Ideal}$ |
|-------------|-------------|------------------|-------------|------------------|------------|
| 0           | 0           | 0                | 0           | 0                | 0.125      |
| 0           | 0           | 1                | 1           | 0                | 0.125      |
| 0           | 1           | 0                | 1           | 0                | 0.125      |
| 0           | 1           | 1                | 0           | 1                | 0.125      |
| 1           | 0           | 0                | 1           | 0                | 0.125      |
| 1           | 0           | 1                | 0           | 1                | 0.125      |
| 1           | 1           | 0                | 0           | 1                | 0.125      |
| 1           | 1           | 1                | 1           | 1                | 0.125      |

Table I: **Truth Table of Full Adder**: $A$ and $B$ are inputs, $C_{in}$ is the carry in, $S$ the sum and $C_{out}$ the carry out. In the Boltzmann machine context, all visible units are equivalent so that inputs and outputs can be written as $v_{1-5}$. $P_{Ideal}$ is the ideal probability distribution where every line's probability is $p = 1/8 = 0.125$. 

\(^{46}\)
Supplementary Information: Hardware-aware in-situ Boltzmann machine learning using stochastic magnetic tunnel junctions

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LEARNED WEIGHTS AND BIASES

In the main manuscript, the learned probability distribution of the full adder is analyzed. In this section the actual weights voltages across the capacitors (Fig. 3 in the main manuscript) are compared to the ideal FA weights. The weight matrix for a FA for an ideal p-computer with ideal sigmoidal p-bit responses is the following and has been part of several works1,2:

\[ W_{FA} = \begin{bmatrix} 0 & -1 & -1 & 1 & 2 \\ -1 & 0 & -1 & 1 & 2 \\ -1 & -1 & 0 & 1 & 2 \\ 1 & 1 & 1 & 0 & -2 \\ 2 & 2 & 2 & -2 & 0 \end{bmatrix} \] (S1)

Since the ideal FA probability distribution is symmetric, the bias vector is 0 and can be disregarded here.
In Fig. 3 of the main manuscript the weights voltages across the capacitors \( V_{ij} = V_{v,ij} - V_{C,ij} \) extracted from the RC-circuit are shown. Since the p-bit response has units of voltage whereas the ideal p-bit response is unitless, there is a constant conversion factor between the \( W_{FA} \) and the weight voltages in Fig. 3. Since the p-bit responses differ for both cases, the learned weights voltages are not identical. The weights are learned to fit to the given non-ideal response of each p-bit. However, it can be clearly seen that the general structure of the different weight voltage matrix extracted from the experiment and \( W_{FA} \) is similar at the end of the learning process for both ideal and non-ideal MTJ system. For example \(-2V_{1,2} \approx -2V_{1,3} \approx 2V_{1,4} \approx V_{1,5} \) which corresponds to \(-2W_{1,2} = -2W_{1,3} = 2W_{1,4} = W_{1,5} \) in Eq.(S1). This makes the point that even though the weights learned in this experiment are not ideal due to the non-ideal p-bit responses, they are related to the weights of an ideal p-computer. Initializing with the weights learned on a hardware probabilistic computer could hence reduce learning time when trying to learn based on an ideal Boltzmann distribution as mentioned in the main manuscript.

In Fig. S1 the learned biases are shown. Since the ideal learned biases are 0, the biases learned in this experiment account for the shifted p-bit responses away from the ideal response center at \( V_{IN} = 1.95 \) V. Since the p-bit responses for the non-ideal MTJ in Fig. 3 a of the main manuscript are shifted to the left all biases are negative and bigger than the biases needed for the ideal MTJ.

**BOLTZMANN MACHINE LEARNING ALGORITHM**

For learning probability distributions in the context of energy-based models like Boltzmann machines the common learning algorithm is gradient ascent of the log-likelihood given by

\[
L(W; V) = \frac{1}{N} \sum_v \log \frac{1}{Z} \exp[-E(v_n; W)]
\]

(S2)

where \( Z \) is the partition function and the data distribution is given by \( V = \{v_n\}_{n=1}^{d34} \). The gradient ascent update rule is given by
\[ W_{ij}(t + 1) = W_{ij}(t) + \epsilon \frac{\delta L(W; V)}{\delta W} |_{W(t)} \]  

(S3)

with the learning rate \( \epsilon \). Solving for the derivative of \( L(W; V) \) gives

\[ W_{ij}(t + 1) = W_{ij}(t) - \langle \frac{\delta E(m)}{\delta W} \rangle_{\text{data}} + \langle \frac{\delta E(m)}{\delta W} \rangle_{\text{model}} \]  

(S4)

The data-term in the derivative evolves from \( \exp(-E(v_n; W)) \) and the model-term from the partition function \( Z \) in Eq.(S2). With energy given by \( E(m) = -\sum W_{ij} m_i m_j \), the Boltzmann machine learning rule is

\[ W_{ij}(t + 1) = W_{ij}(t) + \epsilon (\langle v_i v_j \rangle - \langle m_i m_j \rangle) \]  

(S5)

Eq.(3) of the main manuscript is a time-continuous version of Eq.(S5) where the averaged correlation \( \langle m_i m_j \rangle \) is replaced with the sampled correlation \( m_i m_j \) (compare Ref.5). A similar formula can be derived for the biases.

It has to be noted that the learning rule in Eq.(S5) assumes ideal sigmoidal p-bit responses since it is derived from Boltzmann law. However, in this paper the same learning rule is also applied when p-bit responses are non-sigmoidal with significant variations yet good learning results are achieved.

**LEARNING OF AND, OR AND XOR GATE**

In this section learning examples with smaller numbers of p-bits are presented. The same PCB is utilized but only 3 p-bits and 6 RC elements are used for the AND and OR gate and 4 p-bits and 10 RC elements are used for the XOR gate. Here, the ideal MUX model is used.

**Learning the AND-Gate**

For an AND-Gate the truth table matrix in the bipolar representation \( V_{\text{AND}} \) with an added column with +1 for the bias is given by
The density matrix is then given by
\[
D_{\text{AND}} = \frac{V_{\text{AND}}^T V_{\text{AND}}}{d} = \begin{bmatrix}
1 & 0 & 0.5 & 0 \\
0 & 1 & 0.5 & 0 \\
0.5 & 0.5 & 1 & -0.5 \\
0 & 0 & -0.5 & 1
\end{bmatrix}
\] (S7)
with \(d = 4\). In total 6 parameters have to be learned. Fig. S2 a shows the p-bit response of the 3 p-bits used for AND gate learning. Fig. S2 b shows the KL divergence and Fig. S2 c and d show the histogram at the start and at the end of learning. For the AND gate after learning out of the 8 possible configurations, the 4 desired states become most and equally probable.

**Learning the OR-Gate**

For an OR-Gate the truth table matrix in the bipolar representation \(V_{\text{OR}}\) with an added column with +1 for the bias is given by
\[
V_{\text{OR}} = \begin{bmatrix}
-1 & -1 & -1 & 1 \\
-1 & 1 & -1 & 1 \\
1 & -1 & 1 & 1 \\
1 & 1 & 1 & 1
\end{bmatrix}
\] (S8)

The density matrix is then given by
\[
D_{\text{OR}} = \frac{V_{\text{OR}}^T V_{\text{OR}}}{d} = \begin{bmatrix}
1 & 0 & 0.5 & 0 \\
0 & 1 & 0.5 & 0 \\
0.5 & 0.5 & 1 & 0.5 \\
0 & 0 & 0.5 & 1
\end{bmatrix}
\] (S9)
with \(d = 4\). In total 6 parameters have to be learned. Fig. S3 a shows the p-bit response of the 3 p-bits used for OR gate learning. Fig. S3 b shows the KL divergence and Fig. S3 c and d show the histogram at the start and at the end of learning. For the OR gate after learning out of the 8 possible configurations, the 4 desired states become most and equally probable.

**Learning the XOR-Gate**

For an XOR-Gate even though there are just 2 inputs and 1 output an auxiliary neuron is needed
to be able to learn the XOR functionality. Without an additional p-bit, all non-diagonal entries of the density matrix are 0 which corresponds to no learning at all. Here, we choose the auxiliary neuron to be in the first column of the $V_{\text{XOR}}$ matrix and to be 1 for the first entry and -1 for the last 3 entries of the XOR truth table matrix.

$$V_{\text{XOR}} = \begin{bmatrix} 1 & -1 & -1 & -1 & 1 \\ -1 & -1 & 1 & 1 & 1 \\ -1 & 1 & -1 & 1 & 1 \\ -1 & 1 & 1 & -1 & 1 \end{bmatrix}$$  \hspace{1cm} (S10)

The density matrix is then given by

$$D_{\text{XOR}} = \frac{V_{\text{XOR}}^T V_{\text{XOR}}}{d} = \begin{bmatrix} 1 & -0.5 & -0.5 & -0.5 & -0.5 \\ -0.5 & 1 & 0 & 0 & 0 \\ -0.5 & 0 & 1 & 0 & 0 \\ -0.5 & 0 & 0 & 1 & 0 \\ -0.5 & 0 & 0 & 0 & 1 \end{bmatrix}$$  \hspace{1cm} (S11)

with $d = 4$. It can be clearly seen that without the first column in $V_{\text{XOR}}$ all off-diagonal terms of the $D_{\text{XOR}}$ would be 0. In total 10 parameters have to be learned. Fig. S4 a shows the p-bit response of the 4 p-bits used for XOR gate learning. Fig. S4 b shows the KL divergence and Fig. S4 c and d show the histogram at the start and at the end of learning. The figure just shows the histogram of the 3 of the 4 p-bits (2 input, 1 output) without plotting the states of the auxiliary p-bit. For the XOR gate after learning, the 4 desired states become most and equally probable out of the 8 possible configurations.

**SIMULATIONS OF THE PROPOSED CIRCUIT FOR LARGER NETWORKS**

In this section we use a behavioral model on the MNIST dataset\(^6\) to show that the variation tolerance observed in our proof-of-concept experiment can be transferred to larger scale. It has to be noted that the implemented circuit in our proof-of-concept experiment is a fully visible Boltzmann machine that does not make use of any hidden neurons. This means that the states of all nodes of the Boltzmann machine are given by the data distribution. Hidden neurons add representational power
to a Boltzmann machine and are needed for reaching high absolute accuracy on image recognition tasks like MNIST\textsuperscript{7}.

The MNIST dataset has 60000 training images and 10000 test images with 28x28 pixels with digits from 0 to 9. The fully visible Boltzmann network used here consists of 794 p-bits (28x28=784 + 10 p-bits used as labels). The MNIST dataset is transformed into bipolar values and Algorithm 1 which emulates the circuit's behavior is used for learning. For every iteration of the p-bit update procedure, the behavioral model proposed by Faria et al.\textsuperscript{8} for the hardware p-bit implementation is utilized, a model that has been benchmarked against SPICE simulations. In addition, the activation function is changed to account for device-to-device variations.

To model the behavior of the proposed circuit we use the formula

\[
act(x,k) = \tanh \left[ (1 - k) x + k x^{11} \right]
\]  \hspace{1cm} (S12)

where \( k \in [0, 1] \) parameterizes how ideal the response of the p-bit is.

In Fig. S5 a, Eq.(S12) is compared to a non-ideal p-bit response observed in the experiment. For \( k = 0 \) the ideal p-bit response is observed whereas for \( k = 1 \) the p-bit response looks like a staircase. It can be clearly seen that the model is very close to the observed experimental behavior of the p-bits. To simulate the variation behavior, the factor \( k \) is drawn from a Gaussian distribution with mean \( \mu_k \) and standard deviation \( \sigma_k \) for every p-bit.

In Fig. S5 b the accuracy of the circuit is shown for every iteration of Algorithm 1 for different distributions of \( k \) for each p-bit. To obtain test results, the 784 p-bits that correspond to the pixels are clamped to the bipolar test data and the label p-bits are fluctuating freely. The p-bit with the highest probability of being ‘1’ is used for the classified digit. The learning is performed for different values of \( \mu_k \) and \( \sigma_k \). After around \( 10^5 \) iterations the accuracy saturates to about 81% for all 3 curves shown while the learned weights differ (Fig. S5 c,d). This shows that the circuit can account for non-
ideal p-bit responses by learning the correct weights. The learning can account for the non-ideal p-bit responses and still obtain similar accuracy. The behavioral model simulation suggests that the learning duration of the task shown in Fig.(S5) can be around 100 ns with $\Delta t = 1$ ps and $10^5$ iterations in an ideally optimized integrated circuit using MTJ based p-bits. The 81% accuracy is due to the chosen fully visible network structure without any hidden units. The low performance of this model is not due to the hardware components but due to the low representational power of the fully visible Boltzmann machine$^7$. The same circuit with hidden nodes can be for example implemented by time sharing the p-bit circuit for collecting data and model statistics but is out of the scope of this paper.

REFERENCES

1. Hassan, O., Camsari, K. Y. & Datta, S. Voltage-Driven Building Block for Hardware Belief Networks. *IEEE Des. Test* **36**, 15–21 (2019).

2. Pervaiz, A. Z., Sutton, B. M., Ghantasala, L. A. & Camsari, K. Y. Weighted p-Bits for FPGA Implementation of Probabilistic Circuits. *IEEE Trans. Neural Netw. Learn. Syst.* **30**, 1920–1926 (2019).

3. Carreira-Perpinan, M. A. & Hinton, G. E. On contrastive divergence learning. in *Aistats* vol. 10 33–40 (Citeseer, 2005).

4. Koller, D. & Friedman, N. *Probabilistic Graphical Models: Principles and Techniques*. (MIT Press, 2009).

5. Kaiser, J., Faria, R., Camsari, K. Y. & Datta, S. Probabilistic Circuits for Autonomous Learning: A simulation study. *Front. Comput. Neurosci.* **14**, (2020).

6. LeCun, Y., Cortes, C. & Burges, C. J. C. MNIST handwritten digit database. http://yann.lecun.com/exdb/mnist/.

7. Le Roux, N. & Bengio, Y. Representational Power of Restricted Boltzmann Machines and Deep
Belief Networks. *Neural Comput.* **20**, 1631–1649 (2008).

8. Faria, R., Kaiser, J., Camsari, K. Y. & Datta, S. Hardware Design for Autonomous Bayesian Networks. *ArXiv200301767 Cs* (2020).

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**Figure S1:** Biases voltages during FA learning: **a** Biases voltages across the capacitors for ideal MTJ, **b** Biases voltages for non-ideal MTJ.
Figure S2: **AND-Gate:** a Response for the 3 p-bits used in the AND-Gate. b KL-divergence between ideal and experimental distribution vs. time. The experimental distribution is obtained over 30 s of learning. c Experimental distribution for the first 30 s of learning. d Experimental distribution over the last 30 s of learning. The voltage gain $A_v$ is set to 3.
Figure S3: **OR-Gate**: a Response for the 3 p-bits used in the OR-Gate. b KL-divergence between ideal and experimental distribution vs. time. The experimental distribution is obtained over 30 s of learning. c Experimental distribution for the first 30 s of learning. d Experimental distribution over the last 30 s of learning. The voltage gain $A_v$ is set to 3.
Figure S4: **XOR-Gate**: a Response for 4 p-bits used in the XOR-Gate. b KL-divergence between ideal and experimental distribution vs. time. The experimental distribution is obtained over 60 s of learning. c Experimental distribution for the first 60 s of learning. d Experimental distribution over the last 60 s of learning. The voltage gain $A_v$ is set to 4.
Figure S5: **Learning with behavioral p-bit model** on MNIST dataset: a Experimental p-bit response is compared to the model of Eq. (S12) for different values of $k$ where $x$ is fitted to the input voltage $V_{IN}$. b Test set accuracy on the MNIST dataset during training. c,d Example weights during training. Following parameters are used in the behavioral model: neuron time $\tau_N = 150$ ps, synapse time $\tau_S = 10$ ps, transistor time $\tau_T = 25$ ps and $\Delta t = 1$ ps. The used learning parameters are $\epsilon = 10^{-5}$, $\lambda = 0.0125$ here.
Algorithm 1: Behavioral model of proposed learning circuit.

Given a data set $X$, calculate density matrix $D = XX^T$;
Initialize $W$ to 0 and initialize $m \in \{-1, 1\}$ randomly;

for $t = 0: T$ (number of iterations) do
    Get $m$ from p-bit sampling procedure (Eqs. (1),(2));
    Calculate $M = mm^T$;
    Update $W_{ij} = W_{ij} + \epsilon(D_{ij} - M_{ij} - \lambda W_{ij})$ (Eq.3);
    set diagonal terms of $W$ to 0;
end