A Device for Online Monitoring of the Measurement Accuracy of Digital Electric Energy Meter

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Abstract. The application of smart substation technology has brought many opportunities to the power industry, but also caused many new problems and challenges. At present, with the large-scale promotion of intelligent substation based on IEC61850, there are many engineering problems which will not appear in IEC61850 protocol and are closely related to practical application. A device for online detection of electrical error is designed in the paper for the measurement deviation problem of “IEC61850-9-2 input digital power meter” in the new generation of intelligent substation. The characteristic of the device is that once the meter measurement error is detected within the set time interval, it will record the voltage and current waveform data within the interval in real time for error analysis and problem finding.

1. Introduction

The accuracy of power metering is directly related to the economic interests among power generation enterprises, power grid companies and electricity customers. All metering devices must be checked before they are connected to the power grid. Even if it is verified and qualified in the laboratory, there will still be a large deviation after being connected to the network because the research of electrical energy metering based on IEC61850 is not mature enough presently in [1-6]. The reasons for this situation may be manifold, possible reasons include but are not limited to the following:

- The synchronization of data is not well handled when merging unit works in [7].
- Some of IEC61850 9-2 message are lost or jitter in the transmission process.
- The periodicity problem of power calculation is not properly handled when frequency deviates.
- The influence of harmonics on electric energy metering.

The traditional analog metering system is composed of electromagnetic transformer and electric energy meter with analog input, connected by cable. Its errors mainly come from analog-to-digital conversion and algorithm on the electric energy meter side in [8]. In the smart grid, the analog-to-digital conversion is completed at the transformer or merging unit, and the sampled digital quantity is transmitted to electric energy meter through fiber-optic. The introduction of new error characteristics makes traditional methods no longer applicable. Thus, the paper designs a device which can monitor...
the error change of digital power meters in real time in a set time interval. When the detected error is beyond limiting value, the original signal waveform and 9-2 message in this time interval are saved.

2. Design of power monitoring device system
In the traditional analog metering system, it is assumed that there is no delay in the transmission process, so the voltage signal and current signal are naturally synchronized when they are connected to electric energy meters. However, in IEC61850 digital station, due to the delay of different sampling devices and the resampling in the merging process, the synchronization of digital voltage and current sampling values becomes an important problem [9]. This problem exists in the two classical structures of digital substation metering system at present. In the application of electronic transformer and merging unit, the sampling unit is embedded in the transformer, so the voltage sampler and the current sampler are isolated. They eventually enter the electric energy meter through the same SMV message which will inevitably pass through the merging unit. The other one is that in the application of the traditional electromagnetic transformer and analog sampling value merging unit, the traditional transformer secondary signal is directly connected to the merging unit, that is, the input of the input merging unit is "numerically synchronized", then its outputs are synchronized.

When the digital sampling values of input in electric meter are not synchronized, the measurement of the digital power meter will be abnormal inevitably. For this problem, it is necessary to assume that the input of the merging unit is unreliable when considering the accuracy of online measurement of electric energy meter. So the device designs an electric energy calculation unit for the analog signals before the merging unit, and takes the calculated electric energy as the benchmark to determine whether the electric energy meter value is out of tolerance or not.

Structurally speaking, the digital electric energy meter with IEC61850 9-2 message does not have sampling unit itself. Its errors mainly come from algorithm error and interference of communication fault factors. In order to better record the relationship between communication faults and point energy anomalies, another main function of the device is to record the digital message according to the measurement comparison results. The device includes three power metering modules and a recording module. The structure diagram of the device is shown in figure 1.

![Figure 1. Structural diagram of electric energy monitoring device.](image)

The working process of the device is as follows: Firstly, according to the output of the transformer, calculate the electric energy W1 without merging unit merging. Then, calculate the electric energy W2 based on the SMV message output by the merging unit. Finally, get the measurement result W3 based on the pulse signal output by the digital power meter. When there is a big deviation among three electric values, the recording unit is notified to retain the input of each part.

3. Design of electric energy metering and verification hardware
STM32 and FPGA are used in the bottom layer of the device. Exynos4412 is used to drive SATA hard disk to complete waveform recording and drive 10.1-inch capacitive screen to realize human-computer interaction. The three parts of energy metering unit use common STM32 and FPGA hardware resources. Electric energy metering mainly counts the output pulse of the electric energy meter. Pulse output modes can be divided into two categories: active output and passive output in [10]. The active
output mode does not require the terminal to provide power, the pulse voltage source range is 5±5V, the pulse width is 80±20ms, the meter and the 0.20 terminal have electrical common points. The passive output mode requires power supply from the terminal. The meter and the terminal are separated by optical coupling. The pulse voltage amplitude is same as the power supply provided by terminal, the pulse width is 80± 20ms.

3.1. Calculation of the output electric energy of the transformer
The merging unit of analogical input is still widely used, so the main consideration is to calculate electric energy from analogical signal. The hardware block diagram for calculating the analogical power is shown in figure 2.

![Hardware block diagram for calculating simulated electric energy](image)

Figure 2. Hardware block diagram for calculating simulated electric energy.

The input voltage signal is transformed into a 2.5V signal by the transformer inside the device and input into the PGA amplifier unit. When the converted signal is less than the ADC resolution, STM32 adjusts PGA to enlarge the signal and then sampling it. The voltage sampling process is similar. Through sampling values calculated by suitable algorithms, the electric energy carried by the analogical semaphore output by the transformer can be obtained.

3.2. Calculation of merging unit output electrical energy
According to IEC61850 protocol, when the sampling rate is 4000 samples/ sec, the interval between sampled data messages is 250us. The protocol stipulates that the TLV encoding format is used when the sampled value message is transmitted by Ethernet. The TLV format is shown in figure 3.

![TLV encoding format](image)

Figure 3. TLV encoding format.

The message using the TLV encoding structure is nested layer by layer. The lower layer exists as the upper layer of value, that is, the upper layer of value may exist paralleled with one or more TLV blocks. At the same time, each TLV block has its own tag, length and value. Therefore, when using this structure, the location of any value block is not fixed in different applications. The requirement of hardware processing speed and real-time performance for receiving 250us Ethernet messages is very high. Finally, the device chooses the scheme of directly driving PHY chip by FPGA as the hardware of acquiring W2.

4. Software design of wave recording unit
The system consists of four modules. Message parsing module receives 9-2 signals from merging unit and extracts sampled data from message. Analog sampling is completed by W1 acquisition unit, the sampled data will be sent to the value recording unit through the instrument's internal communication line. Data synchronization and recording module stores the parsed digital sampling value data and the
analogue sampling data sent on the bottom layer synchronously. Data management unit mainly manages the stored waveform data. The block diagram of this part is shown in figure 4.

![Block diagram of recording unit system.](image)

The traditional analog recording devices only need to sample and store analogue signals on copper cables, while the IEC 61850 recording device also needs to have the analytical ability of sampling value message and data model. According to the protocol, SV messages are packaged in ISO/IEC 8802-3 frame format and then transmitted in 100-basex network, which is shown in the figure 5.

![ISO/IEC8802-3 message data frame format.](image)

The type of this message is defined as a broadcast message whose broadcast address is defined as 01-0C-CD-00-00-00 and 01-0C-CD-01-01-FF. VLAN part is added on demand, the ethertype is 0x88BA, APPID is selected between 0x4000-0x7FFF. Length represents the size of the entire Ethernet packet data, and its value is equal to the actual number of bytes occupied by five parts of APPID, length, Reservation1, Reservation2 and APDU. Reservation 1 and reservation 2 are both 00H. The actual distribution of APDU is shown in figure 6.

APDU is used as the actual data part of Ethernet message after passing ASN.1 /BER, it contains only one application service data unit. SmpCnt is a sampling value serial number, ConfRev is the configured version number, SmpSynch is a synchronization marker, svID value type is a string. The Data is the voltage and current sampling value. 8 sets of sampling values in the figure are the value channel, from top to bottom are respectively channel 1 to channel 8.

Since the input of waveform data comes before the judgment result, cyclic recording is adopted in this paper. The specific steps are as follows:

- When the comparison starts, the timer is started. When the timer ends, inform the power comparison and the recording part respectively and stop the action.
- According to the set message parameters, the 9-2 analysis module analyses SmpCnt and sampled voltage and current data needed. The parsed data is stored as a temporary file. The analogical sample value data is transmitted to ARM processor by internal communication mechanism. After analysis, the data is processed in the same way as 9-2 data.
- 9-2 data and analogical sample value data are stored by the same storage module in chronological order for comparison in use.
- Power comparison module performs electric energy comparison and timing according to W1, W2, and W3, and notifies the recording module when the predetermined time is reached.
After reaching the predetermined time, the recording module decides whether to permanently store waveform data based on whether the electrical energy comparison is abnormal.

5. Summary and prospect

The application of this device in the digital metering simulation laboratory does provide a good reference for finding out the fault of metering, and greatly facilitates the positioning of the causes of energy metering errors in the digital substation metering system. However, there are still some limitations in the use of the device. In the future, the improvement of measuring accuracy of equipment in various practical application scenarios can be studied in depth.

6. References

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