Design of wireless voice transmission system based on nRF52833

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Abstract. This article chooses pulse density modulation, 2.4GHZ radio frequency, I2S bus nRF52833 chip as the central processing unit to develop the wireless audio transmission system. And carry on the theoretical design and analysis to the hardware module and software module of the whole system, and test the RF distance and power consumption, as well as the audio delay and fidelity, basically realise the design of the wireless voice transmission system based on nRF52833.

1. Introduction
With the continuous development of self-media and 5G communication technology, realising high-quality audio transmission on portable mobile terminals while having a lower bit rate has become a key research area of audio transmission technology for mobile terminals in the future. Embedded isn't easy to transmit large quantities of data in real-time. The realisation of high-quality, low-bit-rate, and low-delay audio transmission on system-level chips is of particular significance. According to the characteristics of wireless audio information, this paper designs a real-time wireless transmission system that consists of the audio collection, wireless communication, audio output, and other hardware and deploys related codec algorithms to realise voice streaming. Compared with the typical audio transmission systems on the market, this system has the characteristics of low noise, low delay, and high quality. It has a wide range of applications on the self-media live broadcast platform and tour guides[1].

2. System overview

2.1. The working principle of the system
This system mainly uses nrf52833 based on Arm Cortex-M4 with FPU architecture as the central core controller. nrf52833 is a general multi-protocol SoC with a Bluetooth direction finding function. It is the 5th generation product of the nRF52 series. It has a high application value. The system’s overall architecture first uses a silicon microphone at the transmitter to collect voice signals. Compared with other microphones, silicon microphones have the advantages of good consistency, high sensitivity, strong anti-interference ability, and sound call effects. The collected audio signals are passed through the single-chip microcomputer. The built-in pulse density modulation module (PDM) is converted into pulse code modulation (PCM) samples, the audio data is compressed through an encoding algorithm, and the information is sent to the receiving end through radio frequency (RF). After receiving the data, the receiving end decodes it and then transmits it to the audio decoder (DECodec) through the built-in audio bus (I2S) and connects the external headphones or speakers for audio output. The overall block diagram of the system is shown in Figure 1.
3. Hardware system design

For the hardware part of the system, according to the use environment, the electronic components of the integrated circuit should be able to work generally within the range of -20°C to 50°C. The temperature range of the hardware device should have a certain margin during the selection, and the system should be considered. Using durability, usage scenarios, and audio effects must consider the characteristics of low power consumption, trim package, and high quality in device selection. The overall function of the integrated system, the use of Soc chips, silicon microphones, Codec, and power modules that meet the requirements in the selection of hardware, and the design of the overall peripheral circuit.

3.1. nRF52833 chip

The core controller of the system adopts the fifth generation product nrf52833 of Nordic's nRF52 series, which is a general multi-protocol SoC with Bluetooth direction finding function. It can be used for higher-value applications. Scalable 105°C temperature certification, coupled with a large amount of memory and dynamic protocol support, ensure that nRF52833 becomes an ideal device for various commercial and industrial applications. The 1:4 ratio of RAM to flash memory and +8dBm output power make nRF52833 suitable for advanced wearable devices or intelligent homes where strong coverage is essential.

It includes a series of analogue and digital interfaces, such as NFC-A, ADC, full-speed 12Mbps USB 2.0, high-speed 32MHz SPI, UART/SPI/TWI, PWM, I2S, and PDM, and has a power supply voltage range of 1.7V to 5.5V[2-3]. Rechargeable batteries or USB power the device. The two-stage LDO regulator and DC-DC converter, together with the automatic power management system, help provide low power values even in more advanced applications.

3.2. Main peripheral devices

3.2.1. Voice signal acquisition circuit. In the entire audio transmission system, the audio collection is the basis of the whole system. Infineon's IM69D130 silicon microphone is used in the selection of microphones. IM69D130 is designed for applications that require low self-noise (high SNR), wide dynamic range, low distortion, and high acoustic overload point. Short-circuit the left and right channel selection pins with Vdd on the connection of the hardware module to collect the data of the left channel on the rising edge. The connection block diagram of the input module is shown in Figure 2 below. At the same time, the PDM software configuration must be PDM mode is selected as the left channel, rising edge acquisition.
3.2.2. Voice signal output circuit. Cooperate with Cirrus Logic's CS4344 on the audio output to perform digital-to-analogue conversion on audio data to output the signal through speakers or headphones. The CS4344 is based on a fourth-order multi-bit delta-sigma modulator with a linear analogue low-pass filter[4]. At the same time, the pin interface can be powered by a single power supply. It does not require other protocols and instructions for register configuration; simplifying the code simultaneously also reduces the design of integrated circuits. The main hardware framework is shown in Figure 3 below.

4. Software system design

4.1. The overall process of the software system
The entire wireless audio transmission system is mainly built around audio collection, data transmission, data reception, and audio transmission. In the realisation of software services, the memory stack overhead is reduced as much as possible. The time complexity of the code is optimised, thereby improving the operating efficiency of the code, ensuring that the audio stream has a low delay real-time transmission can be realised.

4.2. Implementation of each module of the software system
The silicon microphone transmits the collected voice signal to the microcontroller in PDM format. The bits from the left PDM microphone are sampled on the falling edge of PDM_CLK, and the good bit is sampled on the rising edge of PDM_CLK to generate two-bit streams. Each bitstream is fed into a digital filter that converts the PDM stream into 16-bit PCM samples, then filters and down-samples them to achieve the appropriate sampling rate[5-6]. Use EasyDMA to store samples from the filter in a buffer in RAM. The EasyDMA target address pointer is updated when the previous buffer is filled in the program to ensure continuous PDM sampling. The overall workflow is shown in Figure 4 below.
The PDM is initialised and configured in the main function, including the clock and data frame size and related parameters. The PDM clock is configured by calling the library function nrf_pdm_clock_set (nrf_pdm_freq_t pdm_freq), and nrf_gpio_cfg_output(uint32_t pin_number) is used to configure the clock output pin. To proceed, call nrf_gpio_cfg_input(uint32_t pin_number, nrf_gpio_pin_pull_t pull_config) to configure the data input pin. Configure the PDM clock in the system to be 1.032MHz, select the ratio between the PDM clock and the output sample to be 64, and calculate the audio sampling rate to be 16KHz[7-8]. Turn on the data acceptance interrupt. When the number of samples in one frame is reached, the data is encoded and sent out through the radio module.

4.3. Wireless transmission module
When the system is in working mode, the sender will pre-configure the sender's current device number, address, transmission power, and other parameters. The device number and address are received from the receiver when paired with the receiver. When in the active mode, parameters such as device address and transmission power will be configured for the receiving end, and the device address is the same as that of the transmitting end. When the encoding is completed, it waits for the data sent to the receiving end through RF. The sending end will be received first, waiting for the receiving end to send a signal. Once the call is received, it will be in the frame to be sent. One edge of 60 bytes is transferred to the TX payload. After the transfer is completed, RF starts to send data, and at the receiving end, after sending the signal to TX, it will switch to the receiving state and Wait for a while. If there is data transmitted from TX, RX will receive it. After receiving it, the system will start decoding.

4.4. I2S output signal module
The I2S register is initialised and configured on the software side, including data output pins, master clock settings, sampling clock, and channel configuration. By calling nrf_drv_i2s_init(nrf_drv_i2s_config_t const * p_config, nrf_drv_i2s_data_handler_t handler), the configured parameters are written to the register, and the interrupt processing function address is written. Put data into the buffer to be sent through the function prepare_tx_data(uint32_t * p_block), put the interrupted data packet size into the RXTXD.MAXENT register, enable I2S and start data transmission. The DMA double buffering mechanism enables the real-time transmission of audio streams. After sending the first frame buffer data, the second frame data is transferred to the second buffer. When the first frame of data is sent, the DMA can directly The data address of the second frame buffer starts to be transmitted. The continuous streaming of the audio stream is realised by alternately filling and sending data. The overall sending process is shown in Figure 5 below.
5. System function test
In the testing process of the entire system, the audio delay, restoration, and RF transmission distance are mainly tested. In the audio restoration test, the same audio source was used to record the audio that has not passed through the audio transmission system and the audio that passed through the system to obtain the time-domain waveform and frequency spectrum, as shown in Figure 6 below, the time domain diagram before and after audio encoding. The comparison concludes that the system’s audio restoration and clarity effect is still magnificent.

The audio delay test link picks up the same audio source through professional audio editing software. The time-domain diagram is analysed to show that the overall delay of the system is maintained within 190~200ms, which has certain advantages in terms of uncertainty. As shown in Figure 7 below, the audio input and output are collected by tapping the solid. Observe that the time difference between the top input and the outcome is about 0.2S.
Finally, the RF transmission distance of the wireless audio transmission system is tested. In an open outdoor, the transmission power is 10dBm, and the transmission distance can reach 100m.

6. Conclusion
After actual testing, the wireless voice transmission system proposed in this paper has relatively sound effects on audio reproducibility, delay, and RF transmission distance. Compared with the traditional audio transmission system, it has a specific improvement. The entire system has perfect functions and stable performance. At the same time, it has high application value in today's rapid development of self-media. But there is still some room for improvement. For example, low-power Bluetooth can replace 2.4GHz RF to reduce power consumption, and adaptive noise reduction algorithms can be deployed on the audio input to make the audio smoother.

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