Small-Signal Capacitance and Current Parameter Modeling in Large-Scale High-Frequency Graphene Field-Effect Transistors

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Abstract

The analytical model of the small-signal current and capacitance characteristics of RF graphene FET is presented. The model is based on explicit distributions of chemical potential in graphene channels (including ambipolar conductivity at high source-drain bias) obtained in the framework of drift-diffusion current continuity equation solution. Small-signal transconductance and output conductance characteristics are modeled taking into account the two modes of drain current saturation including drift velocity saturation or electrostatic pinch-off. Analytical closed expression for the complex current gain and the cutoff frequency of high-frequency GFETs are obtained. The model allows describe an impact of parasitic resistances, capacitances, interface traps on extrinsic current gain and cut-off frequency.

1. Introduction

The radio frequency (RF) electronic devices play a central role in modern telecommunication systems. The new communication systems demand high frequency low power consumption with high degree of integration, along with good performance even under harsh environment such as radiation, etc. The unique properties of graphene [1] yield new opportunities to improve radio frequency low noise amplifiers. Graphene exhibits a very large carrier mobility, which is at least one order of magnitude greater than in Si that enables creation of devices with high current density and operational efficiency [2, 3]. The lack of a bandgap put a huge obstacle in applications of large-area graphene field-effect transistor (GFET) in digital circuits due to low on-off current ratios. Nevertheless the GFETs in RF applications are not required good on-off characteristics in itself and can benefit from the high mobility values offered by large-area graphene [4]. The significant progress in fabrication of RF GFETs with high performance characteristics (with frequencies as high as 300 GHz) have been reported [5].

One of the main possible application fields of graphene-based devices is space-borne RF telecommunications systems. Therefore, it is important to study the impact of radiation-induced interface traps on the high-frequency behavior of graphene RF transistors and, particularly, cutoff frequency. We have developed in this work a quantitative model of the capacitive and current small-signal parameters with consideration of interface trap buildup impact.

The paper is organized as follows. Sec.2 is devoted to the model background equations. Analytical I-V model in diffusion-drift approximation with two type of current saturation and a new unified approach to the current saturation mode modeling are briefly described in Sec.3. Capacitance and current small-signal parameters models are derived in Sec. 4-5. Frequency-dependent current gain and cutoff frequency simulations are presented in Sec.6.

2. Model background equations

This paper is based mainly on the physical model of GFET operation described in Ref.[6]. In this section we recall briefly the main equations of the diffusion-drift model for I-V characteristics in graphene presented in. Based on analytical solution of the current continuity equation in a diffusion-drift approximation we have obtained the explicit relationships for the distributions of the chemical and electrostatic potentials along the channel length separately and electrochemical potential as a whole.
\[
\varphi(x) - \varphi(0) = -\frac{\varepsilon_0}{\kappa e} \ln \left[ 1 - \frac{x}{L} \left( 1 - \exp \left(-\frac{\kappa}{1+\kappa} \frac{eV_D}{\varepsilon_D} \right) \right) \right],
\]

\[
\zeta(x) - \zeta(0) = \varepsilon_0 \ln \left[ 1 - \frac{x}{L} \left( 1 - \exp \left(-\frac{\kappa}{1+\kappa} \frac{eV_D}{\varepsilon_D} \right) \right) \right],
\]

\[
\mu(x) = \mu(0) + \frac{1+\kappa}{\kappa} \ln \left[ 1 - \frac{x}{L} \left( 1 - \exp \left(-\frac{\kappa}{1+\kappa} \frac{eV_D}{\varepsilon_D} \right) \right) \right],
\]

where \( \zeta(0), \mu(0) \) and \( \varphi(0) \) are the chemical, electrochemical and electrostatic potentials nearby the source controlled by the gate-source bias \( V_{GS} \), \( \varepsilon_0 = n_s / (dn_s / d\varepsilon) \) is the diffusion energy near the source, and the ratio of diffusion to drift current is expressed through the oxide \( (C_o) \), the quantum \( (C_Q) \) and the interface trap \( (C_i) \) capacitances per unit area

\[
\kappa = \left( \frac{\partial \zeta}{\partial \varphi} \right)_{\tau_0} = \left( \frac{\partial V_G}{\partial \varphi} \right)_{\tau_0} = \frac{C_o}{C_Q + C_i}.
\]

The total drain current at constant temperature can be written as gradient of the electrochemical potential taken in the vicinity of the source

\[
I_D = -W \mu_0 n_s (0) \left( \frac{d\mu}{dx} \right)_{x=0} = e \frac{W}{L} D_o N_s (0) \frac{1+\kappa}{\kappa} \left( 1 - \exp \left(-\frac{\kappa}{1+\kappa} \frac{eV_D}{\varepsilon_D} \right) \right) \\
= I_{DSAT} \left[ 1 - \exp \left(-2 \frac{V_{DS}}{V_{DSAT}} \right) \right]
\]

where \( W \) is the channel width, \( D_o \) is the diffusion constant and the Einstein relation \( D_o = \mu_0 e_D / e \) is employed. Notice that the total two-dimensional charge density \( eN_s = e(n_e + n_h) \approx en_s = e(n_e - n_h) \) practically equals to charge imbalance density excepting the vicinity of the charge neutrality point where diffusion-drift approximation is failed. The characteristic saturation source-drain voltage \( V_{DSAT} \) can be defined as follows [6]

\[
V_{DSAT} = 2 \frac{1+\kappa}{\kappa} \frac{\varepsilon_0}{e} = V_o - V_{NB} + en_s (0) / C_o,
\]

where \( \varepsilon_p = \zeta(0) \) is the Fermi energy (the same chemical potential) nearby the source (recall that \( \varepsilon_D \approx \varepsilon_p / 2 \) far enough from the neutrality point in graphene). The chemical potential near the drain is expressed from Eq.1b as \( \zeta(L) = (1 - V_{DS}/V_{DSAT}) \varepsilon_f \), and the condition \( V_D = V_{DSAT} \) corresponds to zero of the chemical potential and current saturation due to electrostatic blocking which is known as pinch-off for silicon MOSFETs [7]. It is instructive to compare saturation voltages in GFETs and Si-MOSFETs where above the threshold voltage \( V_T \) we have

\[
V_{DSAT} = \varepsilon_f + \frac{en_s}{C_o + C_d} \approx \frac{V_{GS} - V_T}{1 + \xi}.
\]

here \( C_d \) is the depletion layer capacitance and \( \xi = C_d / C_o \) is the Si substrate influence factor. The channel capacitance is defined as

\[
C_CH = e \left( \frac{\partial N_s}{\partial V_G} \right) = \frac{C_o}{1 + \frac{C_o + C_d}{C_Q}}.
\]

Recalling \( en_s = C_Q e_D \) and Eq.2 and 4 one can get useful relations

\[
C_{CH} = \frac{\kappa C_Q}{1 + \kappa} = \frac{2en_s}{V_{DSAT}}; \quad e(n_s - n_i) = C_{CH} V_{DSAT} / 2.
\]
The latter relation corrected at the CNP ($\varepsilon_F = 0$) in homogeneous graphene by residual concentration $n_i = (\pi / 6)(k_B T / h\nu_0)^2$ and connecting the analytic equations for channel capacitance, saturation voltage and charge density yields excellent numerical exactness for all temperatures and oxide gate parameters.

3. **Saturation current DC parameters of GFET**

A. Two modes of drain current saturation

The field-effect transistor is fundamentally non-linear device working at large biases generally on all electrodes. The saturation of the channel current in FETs at high source-drain electric field has two-fold origin, namely, (i) the current blocking due to carrier density depletion near the drain, and (ii) the carrier velocity saturation due to optical phonon emission. The saturation current for pinch-off case arising due to saturation of lateral electric field near the source is represented as follows

$$I_{DSAT} = \frac{W}{L} eD_0 n_s(0) \left( 1 + \kappa \right) = \frac{W e n_s \sigma_0}{C_{CH}} = \frac{W}{L} \sigma_0(0) \frac{V_{DSAT}}{2},$$

where the Einstein relation connecting low-field conductivity $\sigma_0$ near the source, diffusivity $D_0$ and quantum capacitance in a form $D_0 C_Q = \sigma_0$ was used.

Another representation of the pinch-off saturation current is

$$I_{DSAT} = W e n_s(0) v_S,$$

where the characteristic velocity is defined as

$$v_S = \frac{\sigma_0}{L C_{CH}} = \frac{\mu_0}{2L} \frac{V_{DSAT}}{V_D0}. \tag{9}$$

The current saturation for short-channel FETs (typically $L \leq 0.5 \mu m$) is bound to the velocity saturation due to scattering on optical phonons. For the velocity saturation $v_{opt}$ it has experimentally and theoretically obtained the relation $v_{opt} = v_0(\hbar \Omega / \varepsilon_F)$, where $\hbar \Omega_{opt} \approx 50$ meV is of order of the optical phonon energy [8].

The channel current saturates due to velocity saturation at $I_{DSAT} = W e n_s(0) v_{opt}$. Note, that for diffusive channel $v_{opt}$ is a maximum velocity of dissipative motion which is in any case less than the speed $v_0$ of ballistic carriers in graphene. One can introduce the dimensionless parameter discriminating the two types of current saturation in FET [9]

$$a = \frac{v_S}{v_{opt}} = \frac{\mu_0 V_{DSAT}}{2v_{opt} L} = \frac{V_{DSAT}}{V_D0}, \tag{10}$$

where a new characteristic drain voltage is defined

$$V_D0 \equiv \frac{2v_{opt}L}{\mu_0}, \quad V_D0 \equiv 10 \left( \frac{2v_{opt}}{10^8 \text{ cm/s}} \right) \left( \frac{L}{1\mu\text{m}} \right) \left( \frac{10^3 \text{ cm}^2 / \text{V}\text{s}}{\mu_0} \right) \ \text{V}. \tag{11}$$

When $a \ll 1$ (long channels and thin gate insulators, low carrier densities and mobilities) the electrostatic pinch-off prevails, and if $a >> 1$ the carrier velocity saturation determines the saturation current of FETs. Thereby the drain current can be rewritten in a unified manner for both cases

$$I_D = W e n_s v_{SAT} \left[ 1 - \exp \left( - \frac{\mu_0 V_{DS}}{v_{SAT} L} \right) \right], \tag{12}$$

where $v_{SAT} = \min \{ v_{opt}, v_S \}$.

A convenient analytical interpolation can be used

$$v_{SAT} = v_{opt} \tanh \frac{v_S}{v_{opt}} = v_{opt} \tanh \frac{V_{DSAT}}{V_D0} \tag{13}$$

which provides convenient analytical description of crossover between two modes of saturation.
Note, that empirical relationships for high-field drift velocity
\[ v_{DH}(E) = \frac{\mu_0 E}{\left(1 + \left(\frac{\mu_0 E}{v_{SAT}}\right)^n\right)^{1/n}} \equiv \frac{\mu_0 E}{\left(1 + \left(E / E_{SAT}\right)\right)^{1/n}} \] (14)
originating from early work of Thornber [10] and traditionally used in CMOS compact modeling [11] also is nothing but empirical interpolation having besides a significant shortage. This equation does not provide fast saturation and yields only \( v_{SAT} / 2^{1/n} \) at \( E = v_{SAT} / \mu_0 \). To remove this shortage for best fitting with experiments a joint interpolation is typically used in CMOS design practice with \( E_{SAT} = 2v_{SAT} / \mu_0 \) and artificial fitting to obey a formal condition \( v(E_{SAT}) = v_{SAT} \). A use of analytic interpolation Eq.13 allows to get rid of piecewise description and senseless fitting parameter \( n \).

B. Unified model for the two saturation modes

Using Eq.12 and 13 a unified relationship for I-V characteristics can be rewritten as
\[ I_D = Wenv_s v_{opt} \tanh \left( \frac{V_{DSAT}}{V_{D0}} \right) \left( 1 - \exp \left[ - \frac{2V_D}{V_{D0} \tanh \left( V_{DSAT} / V_{D0} \right)} \right] \right). \] (15)
Notice that near the charge neutrality point when \( V_{DSAT} < V_{D0} = 2v_{opt}L / \mu_0 \) the “square law” is valid practically at any parameters due to that that electrostatic pinch-off occurs before velocity saturation. This point has confirmed experimentally in Ref.[12]. Further, introducing convenient notation
\[ V_{S0} = V_{D0} \tanh \frac{V_{DSAT}}{V_{D0}}, \] (16)
meaning the lesser of \( V_{D0} \) or \( V_{DSAT} \), the drain current as function of drain-source voltage can be represented by the relation similar to Eq.7
\[ I_D = \frac{1}{2} g_{D0} V_{S0} \left( 1 - \exp \left( - \frac{2V_D}{V_{S0}} \right) \right) \] (17)
where the maximum value of the low-field output conductance is expressed as follows
\[ g_{D0} = \frac{W}{L} e \mu_0 n_s(0) = \frac{W}{2L} \mu_0 C_{CH} V_{DSAT} = W C_{CH} v_s. \] (18)

The transit time through the whole channel length for \( a > 1 \) \( (V_{DSAT}<V_{D0}) \) was found in Ref.[6] as
\[ \tau_{TT} = \int_0^L \frac{dy}{\mu_0 (1 + \kappa) E(y)} = \frac{L^2}{\mu_0 V_{DSAT}} \coth \left( \frac{V_D}{V_{DSAT}} \right). \] (19)
Velocity saturation requires that the Eq.19 for transit time should be modified as follows
\[ \tau_{TT} = \frac{L^2}{\mu_0 V_{S0}} \coth \left( \frac{V_D}{V_{S0}} \right). \] (20)

4. Small-signal current parameters model

In this section, the calculation of the current small-signal parameters of GFETs based on modified diffusion-drift model is described. In RF applications the transistor in small-signal amplifiers is operated in the on-state and input small a.c. radio-frequency signals are imposed onto the d.c. gate–source voltage. Here we describe a small-signal equivalent circuit model based on a combination of known physics in the small signal limit and generally common behavior for all field effect type devices.
A. Input gate admittance and capacitance

The input gate small-signal admittance may be modeled as an inverse sum of the impedances of the gate oxide capacitance and graphene sheet

\[ Y_i = \left( \frac{1}{Y_s} + \frac{1}{i\omega C_{ox}} \right)^{-1} = i\omega C_g(\omega) + \text{Re}Y_G \]  \hspace{1cm} (21)

Taking into account the interface traps existence the frequency-dependent graphene sheet impedance may be in a single level trap approximation modeled as [13]

\[ Y_s(\omega) = i\omega C_G + \frac{C_u}{1 + i\omega \tau_i} \]  \hspace{1cm} (22)

where \( C_u \) is the low frequency interface trap capacitance, \( \tau_i \) is the characteristic time constant of the interface traps recharging typically smaller than 1 MHz. The frequency-dependent input gate capacitance is determined as

\[ C_g(\omega) = \text{Re}\left(Y_i(\omega)/i\omega\right) \]  \hspace{1cm} (23)

For low frequencies \( \omega \tau_i \ll 1 \) we have the low-frequency gate capacitance

\[ C_g = e \left( \frac{\partial N_G}{\partial V_G} \right) = \left( \frac{1}{C_{in}} + \frac{1}{C_G + C_u} \right)^{-1} \]  \hspace{1cm} (24)

We are interested here in the high-frequency case \( \omega \tau_i \gg 1 \) when \( Y_s \approx i\omega C_G \) and the interface traps do not respond to external a.c. gate signal. In this case the high-frequency gate capacitance is frequency and interface traps independent

\[ C_g\bigg|_{\omega \tau_i \gg 1} = C_{CH}\bigg|_{\omega \tau_i \gg 1} \approx \left( \frac{1}{C_{in}} + \frac{1}{C_G} \right)^{-1} \]  \hspace{1cm} (25)

although the presence of the interface traps distorts the C-V characteristics stretching out the C-V curves along the voltage axes. Frequency-dependent response of interface traps yields a peak for \( \omega \tau_i \sim 1 \) with non-zero \( \text{Re}Y_G \) carrying information about interface traps parameters (so called conduction method of extraction [13]).

B. Small-signal response matrices of GFET represented as two-port network

The RF performance of FETs are characterized in terms of small-signal parameters such as internal gate transconductance (\( g_m \)), the output conductance (\( g_D \)), and the gate-to-source \( C_{GS} \) and the gate-to-drain \( C_{GD} \) capacitances. This is illustrated by a small-signal equivalent circuit in Fig. 1 where \( R_D \) and \( R_S \) are the drain and the source access resistances, respectively [4, 14].

![Fig.1. Common source small-signal equivalent circuit of GFET without parasitic capacitances and gate impedance.](image-url)
Small-signal current equations for two-port pi network

\[
\delta i_D = g_m \delta v_{GS} + i\omega C_{GD} (\delta v_{GS} - \delta v_{DS}) + g_D \delta v_{DS} = \left( g_m + i\omega C_{GD} \right) \delta v_{GS} + \left( g_D - i\omega C_{GD} \right) \delta v_{DS}
\]

\[
\delta i_g = i\omega C_{GS} \delta v_{GS} + i\omega C_{GD} (\delta v_{GS} - \delta v_{DS}) = i\omega \left( C_{GS} + C_{GD} \right) \delta v_{GS} - i\omega C_{GD} \delta v_{DS}
\]

may be rewritten in matrix form

\[
\begin{pmatrix}
\delta i_g \\
\delta i_D
\end{pmatrix} = Y \begin{pmatrix}
\delta v_{GS} \\
\delta v_{DS}
\end{pmatrix},
\]

where admittance matrix is defined as

\[
Y = \begin{pmatrix}
(i\omega(C_{GS} + C_{GD})) & (-i\omega C_{GD}) \\
\left( g_m + i\omega C_{GD} \right) & \left( g_D - i\omega C_{GD} \right)
\end{pmatrix}.
\]

Inversing the admittance matrix we get the intrinsic impedance matrix \( Z = Y^{-1} \) with the components

\[
\begin{align*}
Z_{11} &= g_D - i\omega C_{GD} \\
Z_{12} &= -i\omega(C_{GS} g_D + C_{GD} g_m - i\omega C_{GS} C_{GD}) \\
Z_{21} &= \frac{g_m + i\omega C_{GD}}{C_{GD}} \\
Z_{22} &= \frac{C_{GG} g_D + C_{GD} g_m - i\omega C_{GS} C_{GD}}{C_{GG} g_D + C_{GD} g_m - i\omega C_{GS} C_{GD}}.
\end{align*}
\]

The components of admittance matrix describe high-frequency small-signal response of field-effect transistors.

C. Intrinsic output conductance and transconductance

Ignoring many complications one can conclude that current-voltage characteristics with saturation may easily parameterized by the two parameters: the output conductance and the saturation voltage. The drain conductance as function of the node biases (closely connected with low-field conductance \( g_{DO} \)) can be calculated using Eq.17 as a partial derivative with fixed \( V_{GS} \)

\[
g_D = \left( \frac{\partial I_D}{\partial V_{DS}} \right)_{V_{GS}} = g_{DO} \exp\left( -\frac{2V_{DS}}{V_{SO}} \right),
\]

where \( g_{DO} \) is given by Eq.18.

One of the most important small-signal parameter for high-frequency performance prediction is the intrinsic gate transconductance \( g_m \). Transconductance depends generally on microscopic mobility slightly varying with the gate voltage the underlying mechanism and quantitative description of that has not been yet understood and developed in details. Omitting here this point the microscopic mobility will be considered as to be independent on the gate bias in this paper. Exact view of relation the intrinsic transconductance for arbitrary value of the parameter \( a \) depends on the choice of approximation for current and has awkward form. We will use here a convenient approximation

\[
g_m \approx \frac{W}{2L} \mu_0 C_{ch} \left( V_{SO} \right)^2 \exp\left( -\frac{2V_{DS}}{V_{SO}} \right)
\]

The transconductance \( g_m \) increases linearly with \( V_{DS} \) up to saturation on maximum level

\[
g_{m}^{(\text{max})} \approx \frac{W}{2L} \mu_0 C_{ch} V_{SO} = \frac{W}{2L} \mu_0 C_{ch} V_{DSAT} = \frac{W}{L} \mu_0 e_n (0) = WC_{ch} V_s, \quad V_{DO} > V_{DSAT}
\]

\[
\frac{W}{2L} \mu_0 C_{ch} V_{DO} = WC_{ch} V_{sat}, \quad V_{DSAT} > V_{DO}.
\]
D. Role of the contact resistances

Significant limitation of state-of-the-art GFETs is the substantial access resistance due to the significant gaps between the source-gate and gate-drain electrodes, where a large portion of the graphene channel in the gap area is not gated. Access and parasitic contact resistances can significantly degrade performance characteristics of GFETs. Unfortunately the typical values of state-of-the-art graphene-metal contacts may be as high as hundreds of Ohm×µm and larger [15]. The voltage drops on the source and the drain resistances \((R_S \text{ and } R_D)\) stipulate that internal node voltages \((V_{GS}^{\text{int}} \text{ and } V_{DS}^{\text{int}})\) immediately governing the drain current may be sufficiently smaller than the voltages applied to external contacts \((V_{GS}^{\text{ext}} \text{ and } V_{DS}^{\text{ext}})\). For voltage-independent contact resistances the elementary Kirchhoff laws yield

\[
V_{GS}^{\text{int}} = V_{GS}^{\text{ext}} - I_D \left( V_{GS}^{\text{int}}, V_{DS}^{\text{int}} \right) R_S,
\]

\[
V_{DS}^{\text{int}} = V_{DS}^{\text{ext}} - I_D \left( V_{GS}^{\text{int}}, V_{DS}^{\text{int}} \right) (R_S + R_D).
\]

Taking the derivatives of the drain current as function of two internal voltages \(g_m^{\text{int}} = \frac{\partial I_D}{\partial V_{GS}} + \frac{\partial I_D}{\partial V_{DS}}\) one can obtained useful relationships connecting intrinsic and extrinsic steady-state (DC) parameters (see, for example [16])

\[
g_m^{\text{int}} = \frac{\partial I_D}{\partial V_{GS}} = 1 + g_m^{\text{int}} R_S + g_D^{\text{int}} (R_S + R_D),
\]

\[
g_D^{\text{int}} = \frac{\partial I_D}{\partial V_{DS}} = 1 + g_m^{\text{int}} R_S + g_D^{\text{int}} (R_S + R_D).
\]

The contact and access resistances may be fundamentally limiting predicted gain and THz capabilities of GFETs, since poor contacts can significantly decrease \(g_m\) and \(f_T\) [17, 18]. The formation of the self-aligned source and drain electrodes allows precise positioning of the source–drain edges with the gate edges, and thus substantially reduces the access resistance and improves the performance of the graphene transistor [5].

Fig. 2a. Simulated extrinsic transconductance as functions of \(V_{GS}\) at \(V_{DS} = 1\) V for different contact resistances \(R_S = R_D=400 \Omega \times \mu m\) (lower curves) and \(R_S = R_D=100 \Omega \times \mu m\) (upper curve) for zero interface trap density (solid lines) and \(C_{it} = 3 \text{ fF/} \mu \text{m}^2\) (dashed lines); \(W/L = 1 \mu m/0.5 \ \mu m\), \(\mu_0 = 2000 \text{ cm}^2/V\cdot\text{s}\); \(d_{ox} = 10 \ \text{nm}\), \(e_{ox} = 4\), \(T=300 \ \text{K}\), \(v_{opt} = 0.5 v_0\)

Fig. 2b. Simulated transconductance as functions of \(V_{DS}\) at \(V_{GS} = 1\) V for different contact resistances \(R_S = R_D=400 \Omega \times \mu m\) (lower curves, brown lines online) and \(R_S = R_D=100 \Omega \times \mu m\) (upper curves, green lines online) for zero interface trap density (solid lines) and \(C_{it} = 3 \text{ fF/} \mu \text{m}^2\) (dashed lines); \(W/L = 1 \mu m/0.5 \ \mu m\), \(\mu_0 = 2000 \text{ cm}^2/V\cdot\text{s}\); \(d_{ox} = 10 \ \text{nm}\), \(e_{ox} = 4\), \(T=300 \ \text{K}\), \(v_{opt} = 0.5 v_0\)

Fig. 2c. Simulated extrinsic transconductance as functions of \(V_{GS}\) and \(V_{DS}\) at \(W/L = 1 \mu m/0.2 \ \mu m\), \(R_S = R_D = 500 \ \Omega \times \mu m\), \(\mu_0 = 2000 \text{ cm}^2/V\cdot\text{s}\); \(d_{ox} = 10 \ \text{nm}\), \(e_{ox} = 4\), \(T=300 \ \text{K}\), \(v_{opt} = 0.5 v_0\), \(C_{it} = 0\)
Figs. 2 display simulated transconductance as function of $V_{GS}$ and $V_{DS}$ at different parasitic resistances and interface trap capacitances. Notice that although the interface traps do not respond to input high-frequency small a.c. signals they respond to relatively slow large-signal d.c. $V_{GS}$ variation.

5. Small-signal capacitance model

To obtain mutual capacitances between the gate, source and drain one should derive an explicit dependence of the full channel charge $Q_C(V_{GS}, V_{DS})$ as explicit function of the node voltages. It can only be done using a detailed model of charge and potential distribution in Ref. [6]. The Eq. 1b for the chemical potential distribution can be rewritten as follows

$$
\varepsilon_F(x) = \varepsilon_F(0) + \frac{\varepsilon_F}{2} \ln \left[ 1 - \frac{x}{L} \left[ 1 - \exp \left( - \frac{2V_{DS}}{V_{DSAT}} \right) \right] \right], \quad (33)
$$

where $\varepsilon_F(0)$ is the Fermi energy near the drain imposed by the gate-source voltage. The onset of saturation at $V_{DS} = V_{DSAT}$ corresponds exactly to the zero Fermi energy near the drain $\varepsilon_F(L) = 0$. Once $V_{DS}$ exceeds $V_{DSAT}$ the conduction type at the drain end of the channel switches from n-type to p-type and the chemical potential near the drain becomes the negative. The region of positive charge creeps into the channel as $V_{DS}$ increases and its front is determined by the condition $\varepsilon_F(x_0) = 0$

$$
x_0(V_{DS}) = \frac{1 - e^{-2V_{DS}/V_{DSAT}}}{1 - e^{-V_{DS}/V_{DSAT}}} L, \quad V_{DS} \geq V_{DSAT}. \quad (34)
$$

A. Channel charge as function of the node biases

To obtain the full channel charge $Q_C(V_{GS}, V_{DS})$ one should integrate the channel charge density distribution over the channel length $L$ assuming validity of the gradual channel approximation (i.e. the condition of planar electric neutrality along the channel).

$$
\frac{Q_C(V_{GS}, V_{DS})}{Q_C(0)} = \int_0^{x_0(V_{DS})} \left( \frac{\varepsilon_F(x)}{\varepsilon_F(0)} \right)^2 \frac{dx}{L}, \quad V_{DS} < V_{DSAT} \quad (35a)
$$

$$
\frac{Q_C(V_{GS}, V_{DS})}{Q_C(0)} = \int_0^{x_0(V_{DS})} \left( \frac{\varepsilon_F(x)}{\varepsilon_F(0)} \right)^2 \frac{dx}{L} - \int_0^{x_0(V_{DS})} \left( \frac{\varepsilon_F(x)}{\varepsilon_F(0)} \right)^2 \frac{dx}{L}, \quad V_{DS} > V_{DSAT} \quad (35b)
$$

where $Q_C = Q_C(V_{GS}, V_{DS} = 0)$ and the first and the second terms in Eq. 35b correspond to the full charge of the electron and the hole parts of the channel correspondingly. Performing integration with an explicit dependence $\varepsilon_F(x)$ from Eq. 1 we have found the channel charge as function of dimensionless variable $s = V_{DS}/V_{DSAT}$ introduced for brevity

$$
Q_C = Q_C(0) F(s) \quad (36a)
$$

where dimensionless $F(s)$ function is defined as follows

$$
F(s) = \begin{cases} 
\frac{1}{2} \left[ 1 + (1-s)s(\coth s - 1) \right], & s \leq 1 \\
\frac{1}{4} \left[ \frac{1 + \coth s}{1 - e^{-2}} - \frac{e^{-2} - e^{-4}(1 - 2(1-s)s)}{\sinh s} \right], & s > 1 
\end{cases} \quad (36b)
$$

It is useful to determine the derivative of the $F(s)$
\[
\frac{dF(s)}{ds} = \begin{cases} 
\frac{1}{2} \left[ (2s-1)(\coth s - 1) - \frac{(s-1)s}{\sinh^2 s} \right], & s \leq 1 \\
\frac{e^{-s}}{2\sinh s} \left[ (s-2)(s-1) - e^2 + \left( (s(s-1)+1) - e^2 \right) \coth s \right], & s > 1.
\end{cases}
\] (37)

Despite of its piecewise character the universal \( F(s) \) dependence behaves as a smooth function of its variable (see Fig.3).

![Diagram showing the function \( F(s) \) and its derivative.](image)

**B. Gate-source and gate-drain capacitances**

Neglecting charged oxide defects (interface traps) we have equality of the gate and the channel capacitances \( C_g = C_c = (\partial Q_c / \partial V_{gs}) = (e\partial N_c / \partial V_{gs}) \). For the common source circuit the total gate capacitances \( C_{gg} \) at finite drain-source \( V_{ds} \) is defined as

\[
C_{gg} = C_{gs} + C_{gd} = \left. \frac{\partial Q_c}{\partial V_{gs}} \right|_{V_{gs}} ,
\] (36)

and taking into account \( V_{gd} = V_{gs} - V_{ds} \) one obtains the full gate-drain and the gate-source capacitances \( C_{gd} \) and \( C_{gs} \) as functions of the gate and the drain voltages

\[
C_{gd} = \left. \frac{\partial Q_c}{\partial V_{gd}} \right|_{V_{gs}} = - \left. \frac{\partial Q_c}{\partial V_{ds}} \right|_{V_{gs}} , \quad \quad C_{gs} = \left. \frac{\partial Q_c}{\partial V_{gs}} \right|_{V_{gs}} + \left. \frac{\partial Q_c}{\partial V_{ds}} \right|_{V_{gs}} .
\] (37)

The magnitude of the ratio \( C_{gs} \) to \( C_{gd} \) characterizes an extent of the channel charge control by the gate and absence of the direct coupling capacitance between the gate and drain nodes [19]. Taking into account Eq.7 the direct differentiations yield

\[
C_{gd} = \frac{Q_{gs}(V_{gs})}{V_{dsat}} \left( - \frac{dF(s)}{ds} \right) \frac{WLC_{ch}}{2} \left( - \frac{dF(s)}{ds} \right),
\] (38a)

\[
C_{gg} = WLC_{ch} \left[ F(s) + \frac{1}{2} \left( - \frac{dF(s)}{ds} \right) \left( \frac{\partial V_{dsat}}{\partial V_{gs}} \right) \right],
\] (38b)

\[
C_{gs} = WLC_{ch} \left[ F(s) + \frac{1}{2} \left( - \frac{dF(s)}{ds} \right) \left( s \left( \frac{\partial V_{dsat}}{\partial V_{gs}} \right) - 1 \right) \right].
\] (38c)

The relationship

\[
\frac{\partial V_{dsat}}{\partial V_{gs}} = 1 + \frac{C_{ch}}{C_{ox}},
\]

following from Eq.4, accomplishes a closed set of explicit equations for analytical calculation of small-signal capacitance characteristics. Simulated small-signal capacitance dependencies on \( V_{ds} \) and/or \( V_{gs} \) are depicted in Figs.4-6.
Fig. 4. Simulated gate capacitance as functions of gate-source and drain source voltages.

Fig. 5a. Simulated small-signal capacitances normalized to $C_{ox}$ as functions of $V_{GS}$ ($V_{NP} = 0$) at $V_{DS} = 0.5$ V; $d_{ox} = 10$ nm, $\varepsilon_{ox} = 4$, (room temperature)

Fig. 5b. The same curves calculated at $V_{DS} = 0.001$ V; $C_{GG} = C_{G} = 2 C_{GD} = 2 C_{GS}$ as expected

Fig. 6a. Simulated small-signal capacitances normalized to $C_{ox}$ as functions of $V_{DS}$ at $V_{GS} = 2$ V; $V_{NP} = 0$; $d_{ox} = 10$ nm, $\varepsilon_{ox} = 4$, (room temperature)

Fig. 6b. The same curves calculated at $V_{GS} = 0.2$ V.

The equations can be easily generalized for non-zero interface trap density case noticing that the gate and the channel capacitances are connected with each other as [6]
\[
\frac{C_G}{C_{CH}} = 1 + \frac{C_G}{C_Q}
\]

Of course, there are unavoidably additional parasitic reciprocal capacitive electrostatic couplings between the gate and source/drain electrodes which were not considered above. These parasitic elements limit the drive capability and switching speed of the device and should be minimized but cannot be eliminated entirely.

6. Frequency-dependent current gain and cutoff frequency

This section is devoted to modeling of the complex current gain \( h_{21} \) and the cutoff frequency \( f_T \) which is one of the main figures-of-merit of RF transistors.

A. Intrinsic current gain and cutoff frequency

Neglecting temporarily the problem of parasitic capacitances and series resistances in the source-drain circuit the intrinsic short-circuit current gain can be written as

\[
h_{21}^{(\text{int})} (\omega) = \left( \frac{\partial I_D}{\partial I_G} \right)_{V_{GS}} = - \frac{z_{21}}{z_{22}} = \frac{g_m + ioC_{GD}}{ioC_{GG}}.
\]

The cut-off frequency \( f_T \) defined as the frequency at which the gain becomes unity is the most widely used figure-of-merit for RF devices and is, in effect, the highest frequency a FET is useful in RF applications. The condition \( |h_{21} (\omega_T)| = 1 \) yields

\[
2\pi f_T = \frac{g_m}{\left( C_{GG}^2 - C_{GD}^2 \right)^{1/2}} = \frac{g_m}{C_{GG} \left( 1 - \eta^2 \right)^{1/2}}
\]

where \( \eta = C_{GD} / C_{GG} \). Omitting for brevity the factor \( \eta \) typically small for large \( V_{DS} \) and taking into account Eqs. 30 and 38 the cut-off frequency may be represented as follows

\[
2\pi f_T = \frac{\mu_0 V_{S0}}{2L} \frac{1 - \exp(-2V_{DS}/V_{S0})}{F(s) + \frac{1}{2} \left( \frac{V_{DS}}{V_{DSAT}} \right) \left( 1 + \frac{C_{CH}}{C_{ox}} \right) \left( \frac{V_{DS}}{V_{DSAT}} \right) F \left( \frac{V_{DS}}{V_{DSAT}} \right)}
\]

Simple analysis yields that low \( V_{DS} \) we have \( f_T \propto \mu_0 V_{DS} / L^2 \) and in the current saturation mode (\( V_{DS} > V_{S0} \))

\[
2\pi f_T \approx \frac{\mu_0 V_{S0}}{2L} = \frac{\mu_0 V_{DSAT}}{2L}, \quad V_{DS} > V_{DSAT} > V_{D0}
\]

Naturally, the intrinsic cutoff frequency in any case is determined by the carrier transit time through the channel. Both \( L^{-1} \) in short-channel GFETs \([20, 21]\) and \( L^{-2} \) \([8]\) has been observed experimentally depending on operation mode.

B. Extrinsic current gain and cut-off frequency

Extrinsic short circuit small-signal current gain depends additionally on contact drain and source resistance (\( R_{SD} = R_s + R_n \)). Modifying Eq. 39 we have

\[
h_{21}^{(\text{ext})} (\omega) = - \frac{z_{21} + R_s}{z_{22} + R_{SD}}
\]
Fig. 7. Absolute value of complex current gain $\text{Abs}[h_{21}]$ and the imaginary part of $-1/h_{21}$ simulated as functions of frequency demonstrating typical slopes $20 \text{ dB/decade}$ at $f < f_T$. Intersections with dashed lines correspond to the cutoff frequency $f_T$ (~100 GHz). Simulations performed for $W/L = 1 \mu\text{m}; \mu_0 = 2000 \text{ cm}^2/\text{V-s}; V_{DS} = V_{GS} = 1 \text{ V}, d_{ox} = 10 \text{ nm}, \epsilon_{ox} = 4, T=300 \text{ K}, C_t = 3 \text{ fF/}\mu\text{m}^2$, $R_S = R_D = 1 \text{ k}\Omega, d_{in} = 10 \text{ nm}, v_{opt} = 0.5 v_0$.

Fig. 7 shows simulated dependencies of $\text{Abs}[h_{21}]$ and $\text{Im}[1/h_{21}]$ as functions of frequency exhibiting “ideal” slope -20 dB/decade.

Equating to unity the extrinsic short-circuit current gain modified for non-zero $S_D$,

$$\left| h^e_{21}(\omega^e_T) \right| = \left| \frac{z_{21} + R_S}{z_{22} + R_{SD}} \right| = 1 \quad (42)$$

and neglecting $\omega C_{GD} \ll g_m$ and $\omega C_{GS} C_{GD} \ll C_{GG} g_D + C_{GD} g_m$ one can find the extrinsic cut-off frequency

$$f_T \approx \frac{g_m}{2\pi} \left[ \left( C_{GG} (1 + g_D R_{SD}) + C_{GD} g_m R_{SD} \right)^2 - (C_{GG} g_D + C_{GD} g_m)^2 R_S^2 \right]^{1/2}. \quad (44)$$

In practice, due to unavoidable parasitic capacitance presence the cut-off frequency $f_T$ might be significantly below its theoretical maximum value. We modeled here this modifying Eq.43 as follows $C_{GG} \rightarrow C_{GG} + \text{par} C_{ox} W L$ and $C_{GD} \rightarrow C_{GD} + \text{par} C_{ox} W L$, where $\text{par}$ is dimensionless factor characterizing a fraction of parasitic capacitance.

As can be seen from the Figs.8-9, the cut-off frequency $f_T$ can be maximized through minimization of parasitic capacitances and resistances.
Fig. 10. Simulated cut-off frequency $f_T$ as simultaneous function of $V_{GS}$ and $V_{DS}$ calculated for and $C_i = 0 \text{fF/}\mu\text{m}^2$, $W/L = 1\mu\text{m}/1\mu\text{m}$, $\mu_0 = 1000 \text{cm}^2/\text{V-s}$, $d_o = 10 \text{nm}$, $\varepsilon_{ox} = 4$, $T = 300 \text{K}$, $v_{opt} = 0.5 v_0$, $par = 0.5$, $R_S = R_D = 1 \text{k}\Omega/\mu\text{m}$.

Fig. 10 displays 3D plot for simulated dependence of extrinsic cut-off frequency as function gate-source and drain-source voltages. Characteristic peak of the $f_T$ dependence on $V_{GS}$ [22] is explained by presence of the peak in $g_{m}(V_{GS})$ dependence (see Fig. 2a) appearing mainly because of the parasitic resistances presence.
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