A linear voltage controlled quadrature oscillator implementation using VCII

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Abstract Realisation scheme of a linear voltage controlled quadrature oscillator (LVCQO) using the new second generation voltage conveyor (VCII) is proposed. The topology utilizes a pair of matched analog multiplier devices coupled appropriately with the VCII, as the active building block (ABB). The oscillation frequency \( f_o \) is linearly tunable by the multiplier control voltage \( V \); experimental verification exhibits a linear tuning-range up to \( f_o \approx 10 \text{ MHz} \) with measured THD~2% with satisfactory phase-noise figure.

Key words: VCII, SCNF, variable-Q filter, Linear quadrature VCO, phase-noise.

Classification: Integrated Circuits

1. Introduction

An implementation of linear voltage control quadrature oscillator (LVCQO) is based on the new VCII active element [1, 2], that is coupled appropriately with the readily available analog multiplier devices [3] is proposed. Here the design-topology utilizes the analog multiplier devices for conveniently tuning the circuit pole-frequency by its d.c. control voltage \( k \) (\( k \approx \text{Multiplication constant}= 1/\text{d.c. volt} \) [3]. Literature indicates that previous such oscillator designs with electronically tunable feature had been proposed in the recent literature [4-19], as depicted in Table I; wherein only a few exhibit linear tunability feature. The design in the previous such topologies use either some device bias-current \( I_b \) or device transconductance-parameter \( g_{m} \) or passive tune [20]; therefore the designs need additional current processing circuitry that attracts issues of thermal characteristic equation (CE) leading to the implementation of a linear sinusoid oscillator has been presented.

2. Proposed design

An impedance simulator \( (Z_i) \) based on the VCII(−) is shown in Fig. 1 which is next coupled with a few passive components for the implementation of LVCQO and BP-filter.

![Fig.1](image-url)

The VCII port relations, as shown in Fig. 1(a) are

\[
\begin{bmatrix}
V_x \\
I_x \\
V_y
\end{bmatrix} = \begin{bmatrix}
0 & \pm \beta & 0 \\
\pm \alpha & 0 & I_y \\
0 & 0 & V_z
\end{bmatrix} \begin{bmatrix}
V_x \\
I_x \\
V_y
\end{bmatrix}
\]

(1)

where \( \alpha \approx \alpha_o/(s\tau_1+1) \) and \( \beta \approx \beta_o/(s\tau_r+1) \); ideally \( \alpha_o, \beta_o \approx 1 \) and their pole frequencies are located at few hundreds of MHz[2]. The voltage produced at the X terminal is transferred to the low-impedance voltage output Z terminal, (ideally zero) by a voltage gain \( \alpha \) close to unity (ideally \( \alpha = 1 \)). The input current at the high-impedance Y terminal is transferred to the low-impedance X terminal by a current gain of \( \beta \) which is very close to unity in magnitude correspondingly denoted as VCII(+) and VCII(−).

Analysis of the input impedance \( (Z_i) \) from the voltage...
node-Vi in the proposed configuration in Fig.1(b) is
\[ Z_i = \frac{Z_i}{\alpha_1\alpha_2\beta_1\beta_2} = \frac{Z_i}{\delta} \]  
(2)

Where assuming ideal devices (δ ≈ 1), eq. (2) reduces to
\[ Z_i = \frac{Z_i}{Z_3(k\Omega)} \]  
(3)

A parasitic admittance (YX = gX + jCY) consisting of shunt-RXCX combination, (where RX ≈ 1/gX) appears at the input X-node as shown in Fig. 1. Albeit this YX appears at the Zi simulating x-node, it shares quite a negligible part of the input current to Zi, since as per literature RX~1.5MΩ and CX~3.6fF; its rolloff pole appears at few hundreds of MHz implying a practically high input impedance X-node [2], practically which has zero value. Hence the Zi simulation design remains unaffected at relatively lower frequency (MHz)-ranges wherein nominal values of Z1,2,3 in eq. (2) may be selected in the usual KΩ-pF range. A pair of the AD835/734 type voltage multiplier device [3] may also be conveniently utilized for the desired electronic tunability feature. The proposed circuit in Fig.1(b) has been realized [21, 22] using commercially available CFA (AD844) and analog multiplier (AD 835) as shown in Fig. 2, where a positive and a negative polarity analog multiplier have been utilized. The positive/negative multiplier can be realized using the basic terminal relation of analog multiplier AD 835 [3], where the transfer relation of the multiplier can be represented as
\[ V_o = \pm kVV_i \]  
(4)

where, Vi is the input a.c. voltage and V is the d.c. control voltage.

![Impedance simulator realization using AD 835](image)

Fig. 2. (a) Impedance simulator realization using AD 835
(b) Hardware implementation of Impedance simulator

### Table I. Summary of recent electronically tunable sinusoid oscillators

| Ref. | ABB     | f0 (MHz) | Tuning by | Linear | THD% |
|------|---------|----------|-----------|--------|------|
| 1    | MOCII   | 3.24     | V        | Yes    | 2.1  |
| 2    | MMCC    | 9.3      | V        | Yes    | 3.1  |
| 3    | CDVA    | 2.75     | V        | Yes    | 0.26 |
| 4    | ETDCTA  | 1.5      | V        | No     | 1.59 |
| 5    | CTDA    | 1.87     | V        | No     | 3.0  |
| 6    | DVCCTA  | 3.18     | V        | No     | -    |
| 7    | DVCCTA  | 1.6      | V        | Yes    | 1.4  |
| 8    | ETDCCTA | 8.7      | V        | Yes    | 3.5  |
| 9    | VDBA    | 1.14     | V        | No     | 0.9  |
| 10   | CCFTA   | 4.9      | V        | No     | 4.0  |
| 11   | CDBA2   | 0.13     | MOS-switch-RC | No | 3.7  |
| 12   | DCMOCII | 5.6      | MOS-Gate voltage | No | 3.12 |
| Proposed: VCC(+) and Analog Multiplier | 9.9 | V | Yes | 2.2 |

3. Effect of port rolloff

The errors due to the port roll-off errors (δ) in eq. 2 may be simplified with the following assumptions α1,2 ≈ (1 – εi1,2)/(sτo1,2 + 1) and β1,2 ≈ (1 – εo1,2)/(sτo1,2 + 1). The dc-gain errors are negligible (εi ≪1) [1] while the rolloff poles appear at relatively high frequency (>175 MHz) ranges; these may be assumed equal as they lie at close proximity. Hence writing τi = τo = 1/ω0, we may simplify with
\[ \mu = sτ = j \omega_0 \mu_0; \quad |\mu| << 1 \]
\[ \delta = \alpha_1\alpha_2\beta_1\beta_2 \approx (1 - 6\mu^2 + \mu^4) + 4j\mu(1 - \mu^2) \]  
(5)

i.e., \( \delta \approx \sqrt{(1 + 16\mu^2)} \arctan(4\mu) \; \mu << 1 \)  
(6)

which implies that the effects of device rolloff poles on the simulated impedance would be quite negligible.

4. Linear VCO Implementation

The proposed impedance simulator (Zi) is next being utilized for the linear VCO implementation, as shown in Fig. 3.
The principle of SCNF [24] is being applied to derive the appropriate derivation of the characteristic equation (CE) of the topology. The analysis indicates that the \( Z_i \) simulator may also be utilized for the design of a variable-Q second-order band-pass (BP)-selective filter \( H(s) \), as in Fig. 3(a) choosing \( Z_{i,2} \) as Resistance and \( Z_i \) as Capacitor, with a nominal input signal \( (E_i) \), given by

\[
H(s) = \frac{E_o}{E_i} = \frac{s}{s^2 + 2\xi\omega_0 s + \omega_0^2} \tag{7}
\]

where \( \omega_0 = kV/\sqrt{(R_2R_1C_0)} \approx kV/RC \) \( \tag{8} \)

as \( C_0 = C >> C_x, R_1 = R_2 \approx R \ll R_x \),

and pole-Q: \( Q = \frac{kV}{\omega_0}, \quad b = \frac{R_x}{R} \) \( \tag{9} \)

The frequency-stability (\( S_f \)) of the designed BP-filter indicates high, as derived in Table II.

According to the SCNF [24] concept, if pole-Q in eq. (9) is made large (i.e. \( R_x \) – infinite), then the topology exhibits an imaginary-axis pole pair in the \( j\omega \)-domain. Subsequently, if nominal input is grounded \( (E_i \rightarrow 0) \) then the topology would generate sustained V-tunable sinusoid quadrature oscillator at the natural frequency \( \omega_0 \) as shown in Fig. 3(b); therefore, may yield a dual feature viz. BP-filter and linear sinusoid-oscillator with appropriate design, wherein sustained electronically tunable linear quadrature oscillation is realizable with

\[
f_o = \frac{kV}{2\pi RC} \quad \tag{10}
\]

where \( k=1V/d.c. \) volt and the quadrature sinusoid signals had been obtained between \( V_o \) and \( V_{oq} \) nodes in Fig. 3(b).

Here the oscillator topology has both the capacitors grounded which may be selected equal-valued; hence suitable for IC-adaptation [27]. Effects of fractional change in \( \omega_0 \) due to temperature variation may be expressed [27] as \((\Delta \omega_0/\omega_0) \approx -1(\Delta R/R + (\Delta C/C)) \). Over a range of 0–100°C, component variations are \( \Delta C/C \sim 2\% \) and \( \Delta R/R \sim 2\% \) [28, 29] hence \((\Delta \omega_0/\omega_0) \sim 0 \).

![Diagram](image)

5. Experimental Results

The measured responses of BP-filter and LQVCO with hardware design as shown in Fig. 3(b), keeping in view the temperature insensitivity effect on passive components using thin film technology based SMD components are shown in Fig.4.

![Graph](image)

**Table II. Frequency-stability \( S_f \) of BP filter**

| Parasitic components | \( S_f \) |
|----------------------|----------|
| Capacitors \( C_x \) | \( \sigma = \omega_0/C_x \) |
| \( p = C/C_x \) | |
| Resistors \( R_x \) | \( \sigma = \omega_0/R_x \) |
| \( p = 1/R_x \) | \( \sigma = \omega_0/R_x \) |
| \( \sigma, p \ll 1 \) | \( \sigma = \omega_0/R_x \) |

The BP filter has been designed as in Fig. 3(a) using \( Z_{1,2} = 8200\Omega \), \( Z_o = C = C_0 = 56pF \), \( R_o = 2.2K \) and \( V = 2.3 \) Volt, at center frequency \( f_c \sim 8M \) with \( Q \sim 6 \), shown in Fig. 4(a) with the measured THD of 1.12%. Using SCNF topology LVCO has been observed according to Fig. 3(b) using \( Z_0 = C = C_0 = 56pF \), \( Z_{1,2} = R = 1K \) for graph-A and
C=120pF, R=1.2K for graph-B, as shown in Fig. 4(b). The phase difference in quadrature waveform [between node-$V_{n}$ and $V_{o}$ of Fig. 3(b)] has been measured at $f_{0}=9.4$MHz as 89.3° and the spectrum at node-$V_{o}$ is shown in Fig. 4(c) and (d) respectively, with measured phase noise of $-106$ dBc/Hz @ 64KHz offset. The linearity error ($\Delta$) in oscillator response of Fig. 4(b) had been evaluated following the definition [30]. Measured slope of graph-A for the range 2.8MHz − 9.9MHz is: (9.9 $-2.9$)MHz/(3.5$-1$)V, $\Delta_{o}$ $\approx$ 2.83MHz/V $\approx$ $C_{2}$, Calculated slope $C_{1}$ $= 2.86$MHz/V. $\Delta_{o}$ $=$ $(C_{1} - C_{2})/ C_{1} \approx 1.2\%$. Similar evaluation for graph-B indicates $\Delta_{o}$ $\approx$ 0.2%. Hence low linearity error has been observed due to its negligible parasitic effects.

6. Conclusion

A new VCII-based linear electronically-tunable sinusoid oscillator circuit implementation scheme is presented that utilizes $f_{o}$-tunability feature by the d.c. control voltage of analog-multiplier devices. Appropriate choice of node selection also provides a selective high-Q band-pass filter design in the same topology which subsequently corroborates to linear sinusoid quadrature wave generation by the concept of the SCNF. Effects of the x-node VCII device parasitic are negligible. The design provides the features of improved frequency-stability and satisfactory phase-noise figure of $-106$ dBc/Hz offset frequency of 64KHz at $f_{o} \approx 9.5$MHz; wave harmonic distortion is quite low.

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