Power Efficient Model of PWM Generator for Green Computing and Communication on High Performance FPGAs

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Abstract: PWM generator is one of the core modules of a communication model. Its main function is to control the amplitude of signal and used for reducing average power of the pulses and signals. The PWM generator can also be used in promoting the green computing and green communication other than data and wireless communication if it is made power and energy efficient. In this work we are using different Stub Series Terminated Logic (SSTL) IO with three distinguished FPGAs of different Nano meter (nm) gate size that are 28 nm SPARTAN-7, 20 nm KINTEX-7 Ultra scale, and 16 nm ZYNQ Ultra scale+. The model has been synthesized and implemented on VIVADO ISE tool. From the power analysis it is observed that 16 nm ZYNQ Ultra scale+ requires the highest amount of power for operation with SSTL18_I IO and 28 nm SPARTAN-7 uses least amount of power for the operation with SSTL135 IO, while the 20 nm KINTEX-7 Ultra scale lies in mid of both of these devices.

Keywords: FPGA, PWM generator, Green computing, Green communication, Data communication, Power-efficient design, and SSTL IO.

1. Introduction

Pulses and signals are the building blocks of a communication module system. The telecommunication system uses PWM (Pulse Width Modulation) signal for its operation. These PWM signals are hence generated with the help of the PWM generator. In the communication system the signal is regarded as PWM signal when its width is changed accordingly with respect to the modulated signal [1]. The generation of PWM signal is represented in Fig. 1 and Fig. 2.
In Fig. 1, the PWM waves are generated with the help of three building blocks such as modulator, comparator, and sawtooth generator and four types of signals that are message, carrier, PAM, and ramp [2]. At the first instance the message and carrier waves are modulated with the help of modulator. And in second phase the output of modulator i.e. PAM signal and sawtooth generator i.e. ramp is fed to the comparator. The resultant of the comparator is the PWM signal. The PWM generator reduces the average power of the communication module [3]. PWM uses a rectangular wave signal whose width is varied and the resultant is the reduced average power of the signal [4]. Let’s consider the pulse as \( x(t) \), having time period of \( T \), duty cycle \( D \), low value \( y_{\text{min}} \) and high value \( y_{\text{max}} \) as shown in Fig. 3
Therefore the average reduced power of the waveform is stated as:

\[ \bar{y} = \int_0^T x(t) \, dt \]  \hspace{1cm} \ldots (1)

\( y_{\text{min}} \) for \( x(t) \) is \( D.T < t < T \) and \( y_{\text{max}} \) is \( 0 < t < D.T \), hence the above equation can be realized as:

\[ \bar{y} = \frac{1}{T} \left( \int_0^{DT} y_{\text{max}} \, dt + \int_{DT}^T y_{\text{min}} \, dt \right) \]  \hspace{1cm} \ldots (2)

\[ = \frac{1}{T} (D.T \cdot y_{\text{max}} + T \cdot (1 - D)y_{\text{min}}) \]  \hspace{1cm} \ldots (3)

\[ = D \cdot y_{\text{max}} + (1 - D)y_{\text{min}} \]  \hspace{1cm} \ldots (4)

This outstanding feature of the PWM generator makes it an ideal choice for green communication and green computing \[6-7\]. Hence the power-efficient design of the PWM generator results in proficient green communication as well as data communication. The power-efficient model of the PWM generator for the green computing as well as green communication can be realized by implementing the PWM generator on FPGA device \[8-9\]. FPGA is a Field Programmable Gate Array device, whose inputs and outputs can be varied after its post manufacturing \[10\]. FPGAs are constituted up of Flip-Flops (FF), Memory Blocks (MB), Clock Buffers (BUFGs), Input/output (IO) ports, and Digital Signal Processors (DSPs) \[11-12\]. The building of a FPGA device is illustrated in Fig. 4.
2. Existing Works

This section will cover the existing works done in recent times on PWM generator, green communication and as well power-efficient model with FPGA. In [13] researchers implemented PWM generator on FPGA for high frequency operation. In [14] a FPGA and DSP based PWM generator is designed for rail traction and motor control. With the help of cyclone IV FPGA PWM generator reduces the load of two level inverter [15]. In [16] research described the trade-off between the speed, area, and power for FPGA based PWM generator. In [17] dual boost converter design is introduced by the authors using FPGA based PWM generator. In [18] authors used VIRTEX and SPARTAN FPGAs to design a control unit for promoting green communication. In [19] with the help of FPGA device authors designed a thermal aware and power-efficient control unit for green communication. In [20] power estimated model is designed by researchers for wireless communication using FPGA. In [21] authors have designed a FIR Filter for green communication. This filter is an energy-efficient filter and the efficiency is measured by scaling the capacitance of the output load. In [22] researchers have implemented a FIR filter design on SPARTAN-6 FPGA which is energy-efficient. In [23] authors have used various FPGAs to design a UART communication device for green communication. In [24] researchers have used two FPGAs of SPARTAN family to design a model of power-efficient transceiver. In [25] authors have designed an energy-efficient design of control unit on FPGA with the help of HSUL and HSTL IO standards. In [26] authors with the help of Ultra scale FPGA and POD IO standards designed an efficient design of ALU. In [27] to promote the technologies if green communication, authors have implemented an instruction register on FPGA. In [28] authors have analyzed the performance of FIR filter on various FPGA and SOC for communication channel. In [29] researchers have used LCMOS IO standard to design an energy-efficient model of UART for green communication. In order to improve the wireless green communication authors have proposed a Vedic multiplier circuit [30]. In this work power has been reduced by using the various IO standards on Vedic multiplier implementation. In [31] researchers have implemented an energy-efficient model for green communication using data outage and Channel
State Information (CSI) techniques. In [32] authors have designed a green flip-flop model for wireless green communication using FPGA device. From the recent existing works, it can be clinched that numerous works has been done in past to endorse the green computing and green wireless communication with FPGA with numerous communicating circuits. But almost no work has been done in keeping the aspects like PWM generator, FPGA, and green computing for green communication one a single folio. Therefore this work is all about realizing the above on a single platform, so that there must be an efficient data as well as wireless communication. If the PWM becomes power-efficient then the communication network will also become smooth as well as efficient. The efficient model is shown in Fig. 5.

![Fig. 5 Efficient model for green communication](image)

3. PWM generator design on FPGA

This section will cover the implementation of PWM generator on FPGA device. For making the PWM generator suitable for green computing and communication, we have implemented the design on VIVADO ISE from Xilinx and the power analysis as well as resources utilization are targeted on three different FPGAs which as follows [33]; the Register Transfer Logic (RTL) of PWM generator with three FPGAs is represented in Fig. 6 and the process of implementation is shown in Fig. 7 [34].

- **SPARTAN-7**- It is a 28nm FPGA from SPARTAN family of Xilinx. This device runs on DDR3 800 memory bandwidth. It also provides extra pin-count to logic inputs for IO architecture [35].
- **KINTEX-7 Ultra scale**- It is a FPGA of KINTEX family from Xilinx, which has a gate size of 20nm. It has a memory bandwidth of 2400 with DDR4 architecture [36].
- **ZYNQ Ultra scale+ System on Chip (SoC)**- It is also known as SoC FPGA which has a gate size of 16nm. These FPGAs are mainly used for communication, IoT (Internet of Things) and design SoC architecture [37].
Fig. 6 RTL of PWM generator

Fig. 7 The implementation process on FPGA
3.1 PWM generator design on SPARTAN-7

The realization of PWM generator on SPARTAN-7 involves the utilization of 19 LUTs (Look up Tables), 46 FF, 4 IO, and 1 BUFG; whereas there are 48000 LUTs, 96000 FF, 400 IO, and 32 BUFGs are accessible on the device for the usage [38-39]. The utilization percentage of all the resources is as 0.04 % LUTs, 0.05 % FF, 1 % IO, and 3.13 % BUFG. The resources utilized after post implementation are shown in table 1 and Fig. 8.

Table 1. Resources utilization for SPARTAN-7

| Resource | Utilization | Available | Utilization % |
|----------|-------------|-----------|---------------|
| LUT      | 19          | 48000     | 0.04          |
| FF       | 46          | 96000     | 0.05          |
| IO       | 4           | 400       | 1.00          |
| BUFG     | 1           | 32        | 3.13          |

Fig. 8 Post implementation resources utilization

3.2 PWM generator design on KINTEX-7 Ultra scale

The modeling of PWM generator on KINTEX-7 Ultra scale consist of the consumption of 32 LUTs, 46 FF, 4 IO, and 1 BUFG; whereas there are 203128 LUTs, 406256 FF, 520 IO, and 480 BUFGs are accessible on the device for the usage [40-41]. The utilization percentage of all the resources is as 0.0 % LUTs, 0.01 % FF, 0.77 % IO, and 0.21 % BUFG. The resources utilized after post implementation are shown in table 2 and Fig. 9.

Table 2. Resources utilization for KINTEX-7 Ultra scale
3.3 PWM generator design on ZYNQ Ultra scale+ SoC

The demonstrating of PWM generator ZYNQ Ultra scale+ SoC contains the consumption of 32 LUTs, 46 FF, 4 IO, and 1 BUFG; whereas there are 47232 LUTs, 94464 FF, 180 IO, and 196 BUFGs are accessible on the device for the usage [42-43]. The utilization percentage of all the resources is as 0.07 % LUTs, 0.05 % FF, 2.22 % IO, and 0.51 % BUFG. The resources utilized after post implementation are shown in table 3 and Fig. 10.

Table 3. Resources utilization for ZYNQ Ultra scale+ SoC
4. Power Efficient Techniques

There are numerous methods in order to make the PWM communication power and energy efficient for the development of the green communication. These methods are like dynamic voltage variation at the output and input of the PWM generator, scaling of the capacitance at the output, variation in the frequency of the signal, clock gating techniques, clock mapping, changes in thermal properties, and input output impedance matching with IO standards [44]. In this work the communication model is being made power-efficient by matching the impedance with the help of IO standard. These IO standards are applied at the input and output end of the transmission line, to match the impedance of the input port to the output port [45]. After using the IO standards the communication model will be look like as shown in Fig. 11. There are various IO standards used to make the model power-efficient which is such as LVCMOS (Low Voltage Complementary Metal Oxide), POD (Pseudo Open Drain), SSTL (Stub Series Terminated Logic), HSTL (High-Speed Transceiver Logic), HSUL (High-Speed Unterminated Logic), LVTTL (Low Voltage TTL), and Mobile DDR [46-47]. In this work the IO standard used in making the communication power-efficient is SSTL IO standard [48].

| Resource | Utilization | Available | Utilization % |
|----------|-------------|-----------|---------------|
| LUT      | 32          | 47232     | 0.07          |
| FF       | 46          | 94464     | 0.05          |
| IO       | 4           | 180       | 2.22          |
| BUFG     | 1           | 196       | 0.51          |

Fig. 10 Post implementation resources utilization
4.1 SSTL IO Standard

SSTL is the acronym for Stub Series Terminated Logic IO standard. This is used in FPGA for reducing the power consumption and hence makes the device power-efficient [49]. SSTL IO standard works on DDR and DRAM based ICs and memory modules [50]. This IO standard provides high speed to the device. In this work we have used four major SSTL family IO standards which are as follows:

- SSTL135- This family group provides 1.35 V voltage at the input end [51].
- SSTL15- This family allows 1.5 V voltage for the operation [51].
- SSTL18_I and SSTL18_II- These two IO standards operate at 1.8 V voltage. SSTL18_I is of class I and works for unidirectional signal whereas SSTL18_II is of class II works for parallel transmission [51].

The internal architecture of SSTL IO standard is depicted in Fig. 12. In Fig. 12 it is seen that the IO standard is applied at the input and output port of the transmission lines.
5. Power Analysis

In this section we will cover about the Total Power (TP) used by the device in implementing the efficient PWM generator for green computing and communication. The total power consumed is the total on-chips power, which is also regarded as thermal power. Therefore TP can be equated as the summation of device Dynamic and Static Power.

\[ TP = SP + DP \] \hspace{1cm} \text{(5)}

DP is the device that power which is calculated when all the inputs of the device are in active state. In FPGA it is the summation of IO, Signal (S/g), and Logic (L/g). SP is calculated when there is no response in the circuitry of the device. Power in FPGA it is the Leakage Power (LP).

\[ DP = IO + S/g + L/g \] \hspace{1cm} \text{(6)}

5.1 Power Analysis for SPARTAN-7

For SPARTAN-7 the power is calculated for SSTL135, SSTL15, SSTL18_I, and SSTL18_II IO standard.

A. SSTL135

This IO standard give the input voltage of 1.35 V. when the power is calculated for this then the TP is calculated as summation of DP which is 0.527 W and SP 0.101 W. The TP consumed with SSTL 135 is 0.629 W. Here the DP is the total of IO, S/g, and L/g power. The power consumption for SSTL135 is given in table 4 and represented in Fig. 13.

\[ DP = 0.183 + 0.206 + 0.138 \]
\[ = 0.527 \]

\[ TP = DP + SP \]
\[ = 0.527 + 0.101 \]
\[ = 0.629 \text{ W} \]

| Table 4. Power consumption for SSTL135 |
B. SSTL15

When SSTL15 is used for power optimization then TP consumed is 0.635 W. The DP and SP are 0.527 W and 0.107 W respectively. SSTL15 operates at the input voltage of 1.5 V.

\[
DP = 0.183 + 0.206 + 0.138
\]

(7)

\[
= 0.527
\]

\[
TP = DP + SP
\]

(6)

\[
= 0.527 + 0.107
\]

\[
= 0.635 W
\]

The power consumption for SSTL15 is given in table 5 and represented in Fig. 14.

Table 5. Power consumption for SSTL15
SSTL18_I is of the class I group in SSTL18 family, which operates at input voltage of 1.8 V. The T.P consumed with this is 0.637 W. The DP consumed is 0.529 W and the SP consumed is 0.107 W.

\[
DP = 0.186 + 0.206 + 0.138 \quad \text{From} \quad ... \quad (7)
\]
\[
= 0.529
\]
\[
TP = DP + SP \quad \text{From} \quad ... \quad (6)
\]
\[
= 0.529 + 0.107
\]
\[
= 0.637 \text{ W}
\]

The power consumption for SSTL15 is given in table 6 and represented in Fig. 15.

Table 6. Power consumption for SSTL15
**Total on Chip Power**

|         | Power (W) |
|---------|-----------|
| IO      | 0.186     |
| S/g     | 0.206     |
| L/g     | 0.138     |
| LP      | 0.107     |
| **Total** | **0.637** |

---

Fig. 15 Total Power consumption for SSTL18_I

D. **SSTL18_II**

This IO standard give the input voltage of 1.8 V. when the power is calculated for this then the TP is calculated as summation of DP which is 0.533 W and SP 0.107W. The TP consumed with SSTL18_II is 0.64 W. The power consumption for SSTL18_II is given in table 7 and represented in Fig. 16.

\[
DP = 0.189 + 0.206 + 0.138
\]

(7)

\[
= 0.533
\]

\[
TP = DP + SP
\]

(6)

\[
= 0.533 + 0.107
\]

\[
= 0.64 W
\]
It is detected from the power analysis of the entire 4 SSTL IO standard that as the input voltages raise, the TP consumption for the device also upturns. Therefore there is an increase of 1.74% of TP when the TP consumption is compared between SSTL135 and SSTL18-II. These 2 IOs consume the least and the extreme power in the family. The TP consumed for SPARTAN-7 with SSTL is depicted in Fig. 17.
5.2 Power Analysis for KINTEX-7 Ultra scale

For KINTEX-7 Ultra scale the power is calculated for SSTL135, SSTL15, SSTL18_I, and SSTL18_II IO standard. In this device the TP consumption is equivalent for SSTL18_I and SSTL18_II IO standard.

A. SSTL135

When the TP is calculated with SSTL135 it is observed that there is 51% of the TP consumed by the device when it is in active state i.e. the device DP which is 0.531 W, whereas 49% of the TP is consumed when there is no active signals i.e. the SP which is 0.509 W. Hence the TP consumed is 1.04 W.

\[
DP = 0.173 + 0.214 + 0.144 \quad \text{From} \quad \ldots
\]
\[
= 0.531
\]
\[
TP = DP + SP \quad \text{From} \quad \ldots
\]
\[
= 0.531 + 0.509
\]
\[
= 1.04 \, W
\]

The TP consumed with SSTL135 for KINTEX-7 Ultra scale is described in table 8 and Fig. 18.

Table 8. Power consumption for SSTL135
When the TP is calculated with SSTL15 it is observed that there is 51% of the TP consumed by the device when it is in active state i.e. the device DP which is 0.532 W, whereas 49% of the TP is consumed when there is no active signals i.e. the SP which is 0.509 W. Hence the TP consumed is 1.041 W.

\[
DP = 0.173 + 0.214 + 0.145 \\
= 0.532 \\
TP = DP + SP \\
= 0.532 + 0.509 \\
= 1.041 W
\]

The TP consumed with SSTL15 for KINTEX-7 Ultra scale is described in table 9 and Fig. 19.
Table 10. Power consumption for SSTL18_I and SSTL18_II

| Total on Chip Power | Power (W) |
|---------------------|-----------|
| IO                  | 0.145     |
| S/g                 | 0.173     |
| L/g                 | 0.214     |
| LP                  | 0.509     |
| **Total**           | **1.041** |

C. SSTL18_I and SSTL18_II

For both of these class I and class II IO standards of the SSTL family the TP consumption is equivalent. Both these operates at the input voltage of 1.8 V. Both these IO consumes 51 \% and 49 \% DP and SP of the TP consumption. The TP consumed in this case is 1.042 W. The TP consumed with SSTL18_I and SSTL18_II for KINTEX-7 Ultra scale is described in table 10 and Fig. 20.

\[
DP = 0.173 + 0.214 + 0.146 \quad \text{From} \quad (7) \\
= 0.533 \\
TP = DP + SP \quad \text{From} \quad (6) \\
= 0.533 + 0.509 \\
= 1.042 W
\]
From the power analysis it can be detected that there is just a slight change in power among all the IOs of SSTL. SSTL135 consumes the lowest power while the SSTL18_I and SSTL18_II have the maximum power consumption. There is a raise of just 0.19 % in the TP consumption between SSTL135 and SSTL18_I and SSTL18_II. The TP consumption for KINTEX-7 Ultra scale device with SSTL IOs is described in table 11 and Fig. 21.

Table 11. TP for KINTEX-7 Ultra scale

| SSTL IO | TP (W) |
|---------|--------|
| SSTL135 | 1.04   |
| SSTL18_I| 1.042  |
| SSTL18_II| 1.042 |

![Power Analysis Diagram](image_url)
5.3 Power Analysis for ZYNQ Ultra scale+ SoC

When power is calculated for ZYNQ Ultra scale+ SoC it is found that the TP consumption is equivalent for 2 SSTL IO such as SSTL135 and SSTL15. For the SSTL18_I and SSTL18_II the power consumption is distinguished.

A. SSTL135 and SSTL15

Both of these IO standards give the input voltage of 1.35 V and 1.5 V respectively. When the power is calculated for this then the TP is calculated as summation of DP which is 0.879 W and SP 0.224 W. Hence the TP consumed with SSTL135 and SSTL is 1.103 W. Here the DP is 80 % of the TP consumed while the SP is 20 of the TP. The power consumption for SSTL135 is given in table 12 and represented in Fig. 22.

\[
DP = 0.242 + 0.219 + 0.418
\]
\[
= 0.879 \quad \text{From (7)}
\]
\[
TP = DP + SP
\]
\[
= 0.879 + 0.224
\]
\[
= 1.103 W \quad \text{From (6)}
\]

Table 12. Power consumption for SSTL135 and SSTL15

| Total on Chip Power | Power (W) |
|---------------------|-----------|
| IO                  | 0.418     |
| S/g                 | 0.242     |
| L/g                 | 0.219     |
| LP                  | 0.224     |
| **Total**           | **1.103** |
Fig. 22 Total Power consumption for SSTL135 and SSTL15

B. SSTL18_I

When the TP is calculated with SSTL18_I it is observed that there is 80% of the TP consumed by the device when it is in active state i.e. the device DP which is 0.881 W, whereas 20% of the TP is consumed when there is no active signals i.e. the SP which is 0.224 W. Hence the TP consumed is 1.105 W.

\[
DP = 0.242 + 0.219 + 0.420 \\
= 0.881 \\
(7)
\]

\[
TP = DP + SP \\
= 0.881 + 0.224 \\
= 1.105 W
\]

The TP consumed with SSTL15 for KINTEX-7 Ultra scale is described in table 13 and Fig. 22.

Table 13. Power consumption for SSTL18_I

| Total on Chip Power | Power (W) |
|---------------------|-----------|
| IO                  | 0.420     |
| S/g                 | 0.242     |
| L/g                 | 0.219     |
| LP                  | 0.224     |
| **Total**           | **1.105** |
Fig. 23 Total Power consumption for SSTL18_I

C. SSTL18_II

When the TP is calculated with SSTL18_II it is observed that there is 80% of the TP consumed by the device when it is in active state i.e. the device DP which is 0.870 W, whereas 20% of the TP is consumed when there is no active signals i.e. the SP which is 0.224 W. Hence the TP consumed is 1.094 W. The TP consumed with SSTL18_II for KINTEX-7 Ultra scale is described in table 14 and Fig. 24.

\[
DP = 0.242 + 0.219 + 0.409
\]

\[(7)\]

\[= 0.870\]

\[
TP = DP + SP
\]

\[(6)\]

\[= 0.870 + 0.224\]

\[= 1.094 \text{ W} \]

Table 14. Power consumption for SSTL18_II

| Total on Chip Power | Power (W) |
|---------------------|-----------|
| IO                  | 0.409     |
| S/g                 | 0.242     |
| L/g                 | 0.219     |
| LP                  | 0.224     |
| **Total**           | **1.094** |
In ZYNQ Ultra scale+ SoC TP consumption is equal for SSTL135 and SSTL i.e. 1.103 W. Power consumption gets amplified with SSTL18_I as equated with SSTL135 and SSTL by 0.18 %. But for SSTL18_II TP gets reduced as equated with SSTL135 and SSTL by 0.81 %. The TP consumption for KINTEX-7 Ultra scale device with SSTL IOs is described in table 15 and Fig. 25.

| SSTL IO  | TP (W) |
|----------|--------|
| SSTL135  | 1.103  |
| SSTL15   | 1.103  |
| SSTL18_I | 1.105  |
| SSTL18_II| 1.094  |
6. Results and Discussion

In order to make the PWM generator design suitable of efficient green computing and communication we have implemented the model on 3 distinguished FPGA boards and calculated its power consumption with 4 various IOs of SSTL logic family. It is observed that for SPARTAN-7 and KINTEX-7 Ultra scale FPGAs the TP consumption upturns with amplified value of input voltage with SSTL IO standard. But for ZYNQ Ultra scale+ SoC the TP consumption raises for SSTL18_I as equated with SSTL135 and SSTL15 but gets reduced for SSTL18_II as compared with SSTL135 and SSTL15. For SPARTAN-7 the TP consumption is minimum for SSTL135 and extreme for SSTL18_II i.e. 0.629 W and 0.64 W respectively. Similarly the TP consumption is the minimum for SSTL135 and maximum for SSTL18_I and SSTL18_II i.e. 1.04 W and 1.042 W respectively for KINTEX-7 Ultra scale. And for ZYNQ Ultra scale+ SoC the TP consumption is minimum for SSTL18_II and extreme for SSTL135 and SSTL15 i.e. 1.094 W and 1.103 W respectively. The TP consumption for various FPGA and SSTL IO is explained in table 16 and Fig. 26.

Table 16. TP consumption for various FPGA and SSTL IO

| FPGA       | SSTL135 | SSTL15 | SSTL18_I | SSTL18_II |
|------------|---------|--------|----------|-----------|
| SPARTAN-7  | 0.629   | 0.635  | 0.637    | 0.64      |
| KINTEX-7 Ultra scale | 1.04    | 1.041  | 1.042    | 1.042     |
| ZYNQ Ultra scale+ SoC | 1.103   | 1.103  | 1.105    | 1.094     |
7. Conclusion

From the section 6 it can be concluded that SPARTAN-7 device is suggestively most power-efficient and ZYNQ Ultra scale+ utilizes the highest amount of power consumption. And KINTEX-7 Ultra scale device lies in the mid of both these devices. There is a reduction of 43.07 % TP consumption for SPARTAN-7 device with SSTL135 IO when equated with ZYNQ Ultra scale+ with SSTL18_I IO. Also it can be observed from section 5.1, 5.2, and 5.3 that there is more contribution of DP in TP consumption than SP. Hence the device utilizes additional power when it is on active state than static state. Since PWM generator is an integral part of data and wireless communication, therefore it should requires less power for proficient transmission and well-organized green computing and communication.

8. Future Scope

In this work we are using just approx. 3 % of the total available resources on the FPGA board. And almost 97 % resources are vacant. Hence there is a great chance of implementing the other communication protocols on this FPGA to make an efficient and well-organized communicating device on a single chip. Also later this design can also be converted into small ASIC designs to integrate with latest processor and mobile devices.

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