Investigation of Input-Output Waveform Engineered High-Efficiency Broadband Class B/J Power Amplifier

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ABSTRACT This work introduces a new broadband Class B/J power amplifier (PA) design methodology by considering the input-output waveform shaping due to nonlinear $C_{GS}$-$V_{GS}$ profile in gallium nitride (GaN) radio frequency (RF) devices. A comprehensive time domain modeling of drain voltage and drain current as a function of input nonlinearity is presented to predict continuous Class B/J PA performance. The proposed theory shows that continuous-mode operation can no longer maintain constant PA performance with varying fundamental and second harmonic impedances as predicted by the ideal class-J theory. This paper demonstrates that continuous-mode class B/J operation with input-output waveform shaping yields a new design space with two distinct regions: one advantageous region with capacitive second harmonic load terminations in which PA performance can be enhanced significantly; and another within an inductive second harmonic load area where the performance is degraded compared to that of a classical class B/J PA. For practical validation, source pull measurements and load pull analyses are presented and a broadband Class B/J PA is designed with the proposed second harmonic load and source termination. Source/Load-pull measurements/simulations confirm the theoretical predictions in terms of performance variation across the design space. A high efficiency design space is then identified for broadband PA design. The PA prototype demonstrates drain efficiency of (60-73)% with output power above 40 dBm and corrected adjacent channel power ratio (ACPR) better than −55 dBc with digital predistortion (DPD) using 10 MHz LTE signal across (2.2-3.4) GHz.

INDEX TERMS Class B, continuous mode, continuous class B/J, efficiency, harmonic tuning, input nonlinearity, power amplifier, waveform engineering.

I. INTRODUCTION

The demand of highly efficient, broadband and linear power amplifiers (PAs) urged the designers more than ever in the quest of enabling key 5G features. As such, the established techniques of PA design methodologies are being revisited to meet the higher demands of 5G infrastructure.

To meet such demands, the harmonic tuned load PAs (Class F/F$^{-1}$) had been extensively utilized for efficiency enhancement over tuned load PAs (Class B) [1], [2], [3], [4], [5], [6]. To improve the bandwidth performance, continuous mode of operation were introduced which extended the design space of the Class B/F/F$^{-1}$ PAs and proposed to maintain the output power and efficiency performance over the band of operation [7], [8], [9], [10], [11], [12], [13], [14], [15]. In [3], a Class X PA is proposed where it has been proposed that the different output harmonic termination could have an optimum fundamental termination which are theoretically predicted and proposed load design space high efficiency PA performance. However, all these works were proposed
either by ignoring the input nonlinearity or by avoiding it considering a source second harmonic short circuit at the gate node. But input nonlinearity is inevitable in broadband designs since it is impossible to maintain a harmonic short for a broad frequency range. As such, PA performance analysis with the impact of input nonlinearity is crucial.

Input nonlinearity is introduced by the gate to source capacitance \( C_{GS} \) nonlinearity. Traditionally, input nonlinearity had been reported detrimental to the PA performance and typically avoided by presenting a harmonic short circuit at the input or by a counter-acting nonlinearity [16], [17], [18]. Recently, comprehensive studies on input nonlinearity and its impact on PA performance have been investigated [19], [20], [21], [22], [23], [24], [25], [26]. In [23], the input nonlinearity as a function of second harmonic source terminations is mathematically modeled and utilized to design efficiency enhanced broadband Class F/F\(^{-1}\) PA design [24], [25]. Also, input nonlinearity is considered in continuous mode Class B/J PA design in [26] but lacks the physical correlation to the input nonlinearity generation and source harmonic terminations. Thus, a proper explanation on continuous Class B/J PA behavior with input-output nonlinearity is still missing and proper design methodologies are yet to be explored.

Figure 1 (Case I) shows theoretically predicted ideal Class B/J performance across a second harmonic load \( Z_{2L} \) design space around the short circuit termination, widely adopted to realize broadband PAs. However, in practice, performance variation is observed for the continuous mode Class B/J PAs. Many previous works [27], [28], [29], [30], [31], and load pull studies have shown that capacitive regions on smith chart show higher efficiency than inductive region with second harmonic loading. However, the theoretical explanation behind the phenomenon is still unknown and demands a comprehensive study.

This paper investigates the impact of input-output waveform shaping for broadband Class B/J PAs with new time domain drain current and drain voltage modeling. This new model captures the actual behavior of continuous class B/J PA implementations. To the best of authors’ knowledge, this work is the first to point out to device input nonlinearity as the reason behind performance variation of continuous
II. INPUT HARMONIC CONTROLLED CLASS B/J THEORY

Power Amplifier (PA) performance parameters, like output power and efficiency, are functions of voltage and current waveforms. These voltage and current waveforms can be shaped as per specific requirements with a good understanding and careful control over input-output nonlinearities of the device being used to achieve different PA modes of operation. This section will discuss the impact of input-output nonlinearities on Class B/J PAs.

A. CONVENTIONAL CLASS B/J PA

The time domain gate voltage waveform without any input nonlinearity can be expressed as [1]

\[ v_{GS}(\theta) = V_{GS0} + V_{GS1} \cos \theta \]  

where, \( V_{GS0} \) is the gate bias voltage and \( V_{GS1} \) is the fundamental voltage magnitude. Assuming constant transconductance, the time domain current waveform can be represented as [1]

\[ i_{DS}(\theta) = \begin{cases} I_m \cos \theta & \text{if } |\theta| < \pi/2 \\ 0 & \text{elsewhere} \end{cases} \]  

where, \( I_m \) is the maximum drain current. Similarly, the drain voltage of the conventional continuous Class B/J PA is expressed as [1]

\[ v_{DS}(\theta) = [V_{DD} - (V_{DD} - V_k) \cos \theta] \times [1 - \sigma \sin \theta] \]  

where, \( V_{DD} \) is the drain voltage, \( V_k \) is the knee voltage, and \( \sigma \) is the design continuum factor which varies between -1 to +1. From (2) and (3), the optimum impedance for Class B/J PAs can be calculated as

\[ Z_{1L} = (1 - j\sigma) R_{opt,B} \]  
\[ Z_{2L} = j\sigma \left( \frac{3\pi}{8} \right) R_{opt,B} \]  
\[ Z_{3L} = 0 \]
TABLE 1. Class-J PA under different input nonlinearity Cases.

| Case | Drain Current Waveform | \( (\gamma, \varphi_2) \) |
|------|------------------------|------------------|
| I    | Nominal (\( \beta = 180^\circ \)) | \( \gamma \approx 0 \) |
| II   | Maximum Conduction Angle (\( \beta_{\text{max}} \)) | \( \gamma = 0.49, \varphi_2 = 218^\circ \) |
| III  | Minimum Conduction Angle (\( \beta_{\text{min}} \)) | \( \gamma = 0.43, \varphi_2 = 286^\circ \) |

where, \( R_{\text{opt,B}} = 2(V_{DD}-V_K)/I_m \). The output power and efficiency can be estimated as

\[
P_{\text{out}} = \frac{1}{2} \times (V_{DD} - V_k) \times \left( I_m/2 \right) \tag{7}
\]

\[
P_{\text{DC}} = V_{DD} \times \left( I_m/\pi \right) \tag{8}
\]

\[
\eta_{\text{drain}} = \frac{P_{\text{out}}}{P_{\text{DC}}} \times 100\% \approx 78.54\% \times \left( 1 - \frac{V_k}{V_{DD}} \right) \tag{9}
\]

The waveforms, design space, and drain efficiency (\( \eta \)) are illustrated in Fig.1, (Case I) conventional continuous Class B/J PAs. Theoretically, we can see a constant efficiency across the Class B/J design space.

B. IMPACT OF INPUT NONLINEARITY ON CLASS B/J PAs

Due to the presence of parasitic capacitances of the device being used for any PA design, the performance variation occurs both at small signal as well as large signal in a significant manner. It should be noted that the reference plane of this mathematical analysis is at the \( C_{GS} \) reference plane at the input and at the intrinsic current generator plane at the output. For the FET model, we have considered a constant transconductance characteristic to simplify the analyses. If a sinusoidal input voltage (\( V_{in} \)) is applied to the extrinsic gate terminal of a power FET device, due to its nonlinear \( C_{GS} \) vs \( v_{GS} \) profile, the intrinsic gate voltage (\( v_{GS} \)) waveform is reshaped accordingly. This modified \( v_{GS} \) consequently reshapes the drain current waveforms and impacts PA performance.

Nonlinearity effects can be taken into account by considering higher orders of harmonics being generated due to parasitic capacitances. The gate voltage (\( v_{GS} \)) time domain expression, considering up to second order effects of input nonlinearity, can be redefined as

\[
v_{GS}(\theta, \gamma, \varphi_2) = V_{GS0} + V_{GS1} \left[ \cos \theta + \gamma \cos (2\theta + \varphi_2) \right] \tag{10}
\]

The gate voltage expression can be normalized, \( v_{GS,\text{norm}}(\theta, \gamma, \varphi_2) = \left[ v_{GS}(\theta) - V_{GS0} \right]/V_{GS1} \), as

\[
v_{GS,\text{norm}}(\theta, \gamma, \varphi_2) = \left[ \cos \theta + \gamma \cos (2\theta + \varphi_2) \right] \tag{11}
\]

where, \( \gamma = V_{GS2}/V_{GS1} \), the ratio of second harmonic input voltage (\( V_{GS2} \)) to fundamental (\( V_{GS1} \)), and \( \varphi_2 \) the phase difference between second and fundamental voltage component, are defined as the input nonlinearity parameters. The gate voltage waveforms are shaped due to input nonlinearity and shapes the drain current and drain voltage waveforms which consequently impacts the PA performance.

1) DRAIN CURRET MODELING

In the presence of input nonlinearity, the device conduction angle changes depending on the set of (\( \gamma, \varphi_2 \)) parameters [19]. Considering the modified conduction angle be \( \beta \), the normalized drain current can be expressed as

\[
i_{DS,\text{norm}}(\theta) = \begin{cases} \varepsilon (\gamma, \varphi_2) \left[ \cos \theta + \gamma \cos (2\theta + \varphi_2) \right] & \text{if } |\theta| \leq \frac{\beta}{2} \\ 0 & \text{elsewhere} \end{cases} \tag{12}
\]

where, \( \varepsilon (\gamma, \varphi_2) \) is defined as a limiting function which keeps the drain current within safe operating limits of the device for all sets of (\( \gamma, \varphi_2 \)). For a given value of (\( \gamma, \varphi_2 \)), at \( \theta = \theta_m \) the drain current amplitude becomes maximum. To keep maximum amplitudes of the normalized drain equal to unity for all sets of (\( \gamma, \varphi_2 \)), the limiting factor can be expressed as

\[
\varepsilon (\gamma, \varphi_2) = \frac{1}{\cos (\theta_m) + \gamma \cos (2\theta_m + \varphi_2)} \tag{13}
\]

Substituting \( \theta = \pm \beta/2 \) in (11) gives us

\[
\cos \left( \frac{\beta}{2} \right) + \gamma \cos (\beta + \varphi_2) = 0 \tag{14}
\]

On solving (14) for \( \beta \), we can get the conduction angle variation as function of (\( \gamma, \varphi_2 \)). Fig. 2(a) shows contours of \( \beta \) which indicates that for different values of \( \gamma \) and \( \varphi_2 \), the device conducts more and for others it conducts less.

To understand the impact of input nonlinearity, we consider three cases as defined in Table 1 where Case I represents nominal state of drain current under no input nonlinearity i.e., second harmonic source impedance (\( Z_{2s} \)) as short, giving \( \beta = 180^\circ \) (Class B). Case II and Case III takes impact of input nonlinearity into consideration through two sets of \( \gamma \) and \( \varphi_2 \), which can be practically realized, with former one giving maximum modified conduction angle (\( \sim 220^\circ \) from nominal \( 180^\circ \)) and the later one giving minimum modified conduction angle (\( \sim 155^\circ \) from nominal \( 180^\circ \)).

The blue curve in Fig. 2(a) indicates the values of (\( \gamma, \varphi_2 \)) taken by simulating a nonlinear model of GaN transistor for
FIGURE 4. Drain current components under the presence of input nonlinearity: (a) fundamental real, (b) second harmonic real, (c) third harmonic real, (d) fundamental reactive, (e) second harmonic reactive, and (f) third harmonic reactive.

FIGURE 5. Theoretically estimated load design space with conventional Class B/J drain voltage modeling under the presence of input nonlinearity.

second harmonic source reflection coefficient at the intrinsic gate of magnitude \(|\Gamma_{25}|\) fixed at 0.9 at 2.6 GHz to have a good correlation with practical implemented PAs. For a given device periphery, the \(\Gamma_{25}\) can be evaluated as function of \(\gamma, \varphi_2\) using nonlinear polynomial fitting of gate to source capacitance as given in [23]. Figure 2(b) illustrates the \((\gamma, \varphi_2)\) values realizable with respect to \(\Gamma_{25}\) while keeping the \(|\Gamma_{25}| = 0.9\). Case I, Case II and Case III data points are taken from the blue curve with first case showing \(\beta = 180^\circ\) for which \(\gamma \approx 0\), second case showing maximum and third case minimum conduction angle. For these three cases, Fig. 2(c) and 2(d) shows gate voltage and drain current waveform under the presence of input nonlinearity as per Table 1.

The Fourier expansion of the normalized drain current from (12) gives the dc component as

\[
I_{DC} = \frac{\varepsilon}{2\pi} \left( 2 \sin \beta + \gamma \cos \varphi_2 \sin \beta \right) \tag{15}
\]

FIGURE 6. Voltage gain function contours.

Figure 3 shows contours of the normalized dc current for possible sets of \((\gamma, \varphi_2)\). It shows that dc current increases for \(90^\circ < \varphi_2 < 270^\circ\) and reaches maximum value for \(\varphi_2 = 180^\circ\). The rest of the Fourier coefficients for the normalized
The drain current from (12) are:

\[
I_{1r} = \varepsilon \frac{3\beta + 3\sin\beta + 2\gamma \cos\varphi_2 \left(3\sin\left(\frac{\beta}{2}\right) + \sin\left(\frac{3\beta}{2}\right)\right)}{6\pi}
\]

\[
I_{1q} = \frac{-\varepsilon \gamma}{3\pi} \sin\varphi_2 \left(3\sin\left(\frac{\beta}{2}\right) - \sin\left(\frac{3\beta}{2}\right)\right)
\]

\[
I_{2r} = \varepsilon \frac{2\sin\left(\frac{\beta}{2}\right)}{3\pi} \left(3 - 2\sin\left(\frac{\beta}{2}\right)^2\right) + \varepsilon \gamma \cos\varphi_2 \frac{\cos\varphi_2}{4\pi} \times (2\beta + \sin 2\beta)
\]

\[
I_{2q} = \frac{-\varepsilon \gamma}{4\pi} \sin\varphi_2 (2\beta - \sin 2\beta)
\]

\[
I_{3r} = \varepsilon \frac{2\sin\beta + 2\sin 2\beta}{4\pi} + \varepsilon \gamma \cos\varphi_2 \frac{\cos\varphi_2}{5\pi} \times \left(5\sin\left(\frac{\beta}{2}\right) + \sin\left(\frac{5\beta}{2}\right)\right)
\]

\[
I_{3q} = \frac{-\varepsilon \gamma}{5\pi} \sin\varphi_2 \left(5\sin\left(\frac{\beta}{2}\right) - \sin\left(\frac{5\beta}{2}\right)\right)
\]

where, \(I_{1r}, I_{1q}, I_{2r}, I_{2q}, I_{3r}\) and \(I_{3q}\) are the fundamental real, fundamental reactive, second harmonic real, second harmonic reactive, third harmonic real, and third harmonic reactive components of the normalized drain current respectively.

Fig. 4(a)-4(f) shows contours of drain current components for different combinations of \((\gamma, \varphi_2)\). We observe that for Case I, the current components are as per ideal Class B, while moving from Case I to Case II and then to Case III, the values of both real and reactive current components shift because of which we observe changes in shape of current waveform. This helps in understanding contribution of drain current components to waveform shaping controlled by \((\gamma, \varphi_2)\) which is a function of second harmonic source termination (Z_{2S}).
TABLE 2. Efficiency of a Class-J PA under input nonlinearity for different $x_{2l}$ terminations.

| Nonlinearity Parameters | Capacitive Load ($-j R_{\text{opt},L} \cdot 3\pi/8$) | Shorted Load ($0$) | Inductive Load ($j R_{\text{opt},L} \cdot 3\pi/8$) |
|--------------------------|---------------------------------|----------------------|---------------------------------|
| Case I                   | 78.53 %                         | 78.53 %              | 78.53 %                         |
| Case II                  | 75.59 %                         | 60.29 %              | 32.09 %                         |
| Case III                 | 84.94 %                         | 82.39 %              | 79.91 %                         |

2) CONVENTIONAL CONTINUOUS CLASS B/J VOLTAGE MODELING

Conventionally, the Class B/J drain current and voltage waveforms are expressed as in (2) and (3). In this work, the drain current waveform has been remodeled with input nonlinearity and defined as in (12). It is important to note that with the addition of input nonlinearity, the drain current waveform changes with respect to $Z_{2S}$, affecting performance of continuous Class B/J significantly. Accordingly, the impedances can be calculated for fundamental and second harmonic as

$$Z_{iL} = -\frac{V_{ir} - jV_{iq}}{I_{ir} - jI_{iq}}$$

where, $Z_{iL}$ is the $i$th harmonic impedance for respective harmonic real ($V_{ir}$, $I_{ir}$) and reactive ($V_{iq}$, $I_{iq}$) drain voltage and current components respectively. The impedance design space for the three different cases are shown in Fig. 5 using conventional continuous Class B/J voltage waveform from (3). For $Z_{2S}$ short, i.e., Case I, reactive second harmonic load impedance is obtained as per definition of Class J. However, we can see that the conventional voltage definition as in (3) results in lossy harmonic impedances as well as unrealizable impedance terminations as it goes out of the Smith chart. Although, lossy resistive harmonic terminations are realizable, they cause harmonic power dissipation and degrade efficiency and output power performance. In this regard, a new drain voltage model is necessary for continuous Class B/J PA taking into consideration the impact of input nonlinearity.

3) CLASS B/J VOLTAGE MODELING WITH INPUT NONLINEARITY

We have seen in the previous section that how conventional time domain drain voltage modeling results in unrealistic second harmonic load ($Z_{2L}$) design space under the presence of input nonlinearity. Whereas a designer is free to choose $Z_{2L}$ as desired. For optimum efficiency performance reducing power consumption at harmonics, typically, reactive harmonic terminations are recommended. In this section, we present a generic drain voltage modeling as a function of second harmonic load design space which is more practical and design oriented. To do so, the load impedances can be defined as

$$Z_{1L} = R_{1L} + jX_{1L}$$

$$Z_{2L} = jX_{2L}$$

$$Z_{3L} = 0$$

where, $Z_{1L}$, $Z_{2L}$, and $Z_{3L}$ are the fundamental, second, and third harmonic load impedance, respectively. Considering a broadband Class B/J PA where third harmonic is terminated as short, a generic drain voltage waveform can be represented as

$$v_{DS,IB/J}(\theta) = V_{DD} + (V_{1r} \cos \theta + V_{1q} \sin \theta) + (V_{2r} \cos 2\theta + V_{2q} \sin 2\theta)$$

where, $V_{1r}, V_{1q}, V_{2r}, V_{2q}$ are the fundamental real, fundamental reactive, second harmonic real and reactive voltage components, respectively. The drain voltage components, $V_{1r}, V_{1q}, V_{2r}, V_{2q}$ in (19) can be calculated following the below steps:

1) $V_{DD}$ is the supply voltage chosen by the application and design requirement.

2) From (17) and (18), on solving for drain voltage ($V_{ir} - jV_{iq}$) and equating the real and imaginary coefficients, different voltage components are calculated as

$$V_{1r} = -(I_{1r}R_{1L} + I_{1q}X_{1L})$$

$$V_{1q} = (I_{1r}X_{1L} - I_{1q}R_{1L})$$

$$V_{2r} = -I_{2q}X_{2L}$$

$$V_{2q} = 0$$

FIGURE 8. Flowchart for voltage modeling.
FIGURE 9. Class B/J design space under different $Z_{SS}$ source terminations: (a) Case I- Short $(\gamma, \varphi_2) = (0,0)$, (b) Case II- Maximum $\beta$, $(\gamma, \varphi_2) = (0.49, 218)$ and (c) Case III- Minimum $\beta$, $(\gamma, \varphi_2) = (0.43, 286)$.

FIGURE 10. Class J normalized power and efficiency contours under the effect of input nonlinearity for all possible combinations of $(\gamma, \varphi_2)$: (a), (d) capacitive $(-jR_{opt}/3\pi/8)$, (b), (e) short $(j0.0)$ and (c), (f) inductive $(jR_{opt}/3\pi/8)$ $Z_{SL}$ load terminations respectively.

$$V_{2q} = I_{2r}X_{2L}$$  \hspace{1cm} (20d)

3) For a defined range of $X_{2L}$ as $[-X_{2,lim}, +X_{2,lim}]$, $V_{2r}$ and $V_{2q}$ are calculated for a given value of $X_{2L}$ from (20c) and (20d) knowing $I_{2r}$ and $I_{2q}$ from (16c) and (16d).

4) Now, $(V_{1r}, V_{1q})$ need to be estimated such that the drain voltage remains non-negative for the defined second harmonic load design space. From a generic harmonic tuned (HT) drain voltage expression represented as [1]

$$v_{DS,HT}(\theta) = -\cos\theta - k_2\cos(2\theta) - k_3\cos(3\theta)$$  \hspace{1cm} (21)

where, $k_2$ and $k_3$ are second and third harmonic real voltage components normalized by fundamental HT drain voltage, a voltage gain function defined for each combination of $k_2$ and $k_3$ is expressed as [1]

$$\Delta(k_2, k_3) = \frac{V_{1r}}{V_{DD} - V_k}$$  \hspace{1cm} (22)

As shown in Fig. 6, we can observe $\Delta(k_2, k_3 = 0)$ as function of $k_2$ to keep the generic voltage in (19) as non-zero considering third harmonic load impedance as zero. The voltage gain as a function of $k_2$ can be defined as [1]

$$\Delta(k_2) = \begin{cases} \frac{1}{k_2 + 1/8k_2}, & k_2 \leq -\frac{1}{4} \\ \frac{1}{1+k_2}, & -\frac{1}{4} \leq k_2 \leq 0 \end{cases}$$  \hspace{1cm} (23)

For traditional Class B, voltage gain function becomes unity as $k_2$ and $k_3$ both remains zero, giving a pure
sinusoidal waveform. The generalized drain voltage expression can be rewritten using (22-23) as
\[
v_{DS,B/J}(\theta) = V_{DD} - \Delta \left( k_2 \right) \left( V_{DD} - V_k \right) \\
\times \left[ \cos \theta + k_2 \cos 2\theta \right] + V_{1q} \sin \theta \\
+ V_{2q} \sin 2\theta \tag{24}
\]
The drain voltage from (24) presents a family of drain voltage waveforms depending on the value sets of \((k_2, k_3)\).

5) Calculate \(k_2\) as \(V_{2q}/(V_{DD} - V_k)\).

6) Based on the value of \(k_2\), \(\Delta \left( k_2 \right) \) can be determined from (23) and calculate \(V_{1q}\) as \(\Delta \left( k_2 \right) \left( V_{DD} - V_k \right)\).

7) Now, the remaining drain voltage component \(V_{1q}\) in (24) is estimated satisfying the condition \(\min(v_{DS,B/J}(\theta)) = 0\) which finds the solution for drain voltage to an arbitrary \(Z_{2L}\) termination chosen by the designer.

The drain voltage modeling procedure is summarized in the flowchart shown in Fig. 8. The drain voltage waveforms along with the drain currents for three different cases are shown in Fig. 7 for three different \(Z_{2L}\) terminations modeled by the above steps 1-7. From waveforms we observe that for case II and III, the output voltage swing in capacitive region, is higher as compared to short and inductive terminations. The drain current and voltage waveforms have relatively less overlap in case III for both capacitive and inductive regions as compared to case II and case I, thus ensuring higher efficiency.

This analysis ensures a non-negative drain voltage waveform and provides the fundamental design space as a function of second harmonic reactance \(X_{2L}\). This analysis allows the designer to choose second harmonic load termination as desired under the presence of input nonlinearity. For, \(X_{2L} = 0\) or any value of \(X_{2L}\), the drain voltage calculation is modeled with steps 1-7 described in this section previously.

At this stage, it should be noted that selecting \(X_{2L}\) away from short increases drain voltage maximum which is typical Class B/J PA behavior. However, it is important to select appropriate limits of \(X_{2L}\) such that the device operates reliably in the safe drain voltage region. Thus, it is important to know the maximum limit of \(X_{2L}\).

It has been observed that the maximum drain voltage varies linearly across \(X_{2L}\). For instance, considering the limit as \(3V_{DD} \geq v_{DS,B/J}(\max) \geq 2V_{DD}\), an approximate relationship for Case I can be expressed as
\[
X_{2L,\text{lim}} = \frac{80V_{DS,\max} - 2V_{DD}}{31V_{DD}} \tag{25}
\]
In a similar manner, for a given set of \((\gamma, \varphi_2)\), \([-X_{2L,\text{lim}}, +X_{2L,\text{lim}}]\) can be calculated which allows maximum drain voltage swing.

C. DESIGN SPACE OF CLASS B/J PAs WITH INPUT NONLINEARITY
With the voltage and current waveforms obtained as a function of input nonlinearity, fundamental drain impedance can be estimated for all possible combinations of \((\gamma, \varphi_2)\), using (17). Using the cases defined in Table 1, fundamental impedance is plotted as a function of second harmonic load impedance. As seen in Fig. 9, Case I is conventional continuous Class B/J design space, however, the optimum fundamental impedance changes for Case II and Case III. Due to the contribution of input nonlinearity, the optimum design space for Case II and Case III is asymmetrical across real axis as compared to Case I. This helps us in understanding that fundamental loading varies as a function of second harmonic.
source and design needs a thoughtful matching control to achieve optimum performance from the device.

**D. THEORETICAL ASYMMETRIC CLASS B/J PERFORMANCE**

The dc power for the new drain voltage \( v_{DS,B/J}(\theta) \) and drain current along with the output power and drain efficiency can be estimated as

\[
\begin{align*}
P_{DC}(\beta, \gamma, \varphi_2) &= V_{DD} \times I_{DC}(\beta, \gamma, \varphi_2) \\
P_{out}(\beta, \gamma, \varphi_2) &= -\frac{1}{2} \times \text{Re}(V_1 \times I_1^*) \\
&= -\frac{1}{2} \times (V_{1r}I_{1r} + V_{1q}I_{1q}) \\
\eta_{\text{drain}}(\beta, \gamma, \varphi_2) &= \frac{P_{out}}{P_{DC}} \times 100
\end{align*}
\]

(26)

(27)

(28)

Figure 10 shows calculated normalized power and efficiency contour plots for three extreme limits of \( X_{2L} \) terminations which are \((-j3\pi/8, R_{opt,B}, j0, j3\pi/8, R_{opt,B})\). Though capacitive and inductive \( X_{2L} \) gives us mirror image contours, the realizable/simulated set of \((\gamma, \varphi_2)\) are as shown by the blue curve, with circled dots as data points, in all contours. We observe significant variation in efficiency and power across load terminations, unlike ideal Class B/J (Case I). The efficiency values for fixed load terminations are as shown in Table 2. We had previously observed that current waveforms for all load terminations are same for a given set of \((\gamma, \varphi_2)\). The swing and shape of drain voltage waveforms vary across the loads causing variations in power and efficiency of Class B/J PA under input nonlinearity. Due to which there exists asymmetry in performance across symmetric \( Z_{2L} \) load terminations. Thus, the continuous Class B/J PA with constant power and efficiency does not exist in reality since the input nonlinearity effects on input waveform is inevitable in broadband design.

Considering three cases as per Table 1 for the predefined \( X_{2L} \) range, efficiency is plotted across the load as shown in Fig. 11. As can be seen from Fig. 11, moving from extreme inductive \( Z_{2L} \) termination towards short and upto extreme capacitive \( Z_{2L} \), efficiency performance enhances significantly for both case II and case III. This also gives us an insight that drain efficiency for capacitive \( X_{2L} \) is relatively
less sensitive to variations in $\beta$ than inductive and short $X_{2L}$ terminations.

This theoretical analysis give us an insight that for broad-band design, $Z_{2S}$ transiting between the three cases (I-III-II), capacitive $X_{2L}$ termination offers less variation in efficiency compared to other two terminations, with peak efficiency being higher than that of the inductive $X_{2L}$. Hence, this gives designer the freedom of having less variation in performance across the band in addition to having optimal efficiency. As such, capacitive $X_{2L}$ design space is proposed for broadband Class B/J PAs in this work.

III. LOAD/SOURCE PULL RESULTS

To validate the realistic Class B/J PA performance across $X_{2L}$ terminations under the presence of input nonlinearity, harmonic source and load pull experiments were conducted with a 2-mm GaN device at 2.6 GHz. For Class B loading conditions, source pull measurement data was collected at intrinsic reference plane with maximum efficiency (MXE) fundamental load termination and harmonics short at drain node. Fig. 12 shows power added efficiency (PAE) and output power contours for intrinsic $Z_{2S}$ swept across the whole smith chart. It can be seen from Fig. 12(a) that the efficiency
FIGURE 16. Parasitic network between intrinsic and extrinsic plane at (a) the input side, and (b) the output side of the device.

FIGURE 17. (a) Schematic of the proposed Class B/J PA, (b) Fabricated broadband Class B/J PA, (c) measurement test-bench setup for the designed PA.

performance in Case III is improved by 5% points compared to Case I. On the other hand, the Case II efficiency performance tanks significantly as predicted by theoretical analyses. This proves the necessity of considering input non-linearity in broadband Class B/J PA design.

For efficiency and output power performance, the source harmonic design space is identified for broadband Class B/J PA design. Once $Z_{2S}$ termination is fixed, load pull simulations are carried out with Fig. 13 (a)-(c) showing drain voltage and current waveforms for three fixed $Z_{2S}$ terminations for three fixed $X_{2L}$ terminations. The waveform validates the theoretical Class B/J waveforms. The simulation was carried out at maximum power (MXP) with 3 dB gain compression.

The simulated performance variation across $X_{2L}$ is shown in Fig. 14. To understand the shift in MXP and MXE points across $X_{2L}$ terminations, contours are plotted in Fig. 15 for Case I, Case II and Case III. It is observed that for capacitive $X_{2L}$ termination, Case III offers relatively higher MXE than Case II. Also, for short and inductive $X_{2L}$ terminations, Case III MXE values drops less as compared to Case II. These plots prove and confirm the theoretical prediction of performance shifts.

In Fig. 14, output power and efficiency has been plotted across $X_{2L}$ both at MXP and MXE. We observe that the power remains almost constant around 40 dBm with efficiency being relatively higher for capacitive $X_{2L}$ termination region.
The theoretical time domain analysis typically predicts and falls more in line with MXE than MXP load pull simulations. Comparing Fig. 14(b) with Fig. 11, the variation in efficiency is less in all three cases for load pull simulation for non-short $X_{2L}$ as the time domain modeling presented in this paper rather simplifies the impact of input nonlinearity for the extraction of design space. But even with differences, load pull results follow the trends as per theoretical predictions. This confirms with the theoretically estimated performance variation plot from Fig. 11.

The results in Fig. 14 are significant in that it explains the asymmetry of efficiency performance in Class B/J PAs in practice due to input nonlinearity and also validates that the capacitive $Z_{2L}$ load terminations, in fact, improves the efficiency performance. Thus, it is desirable to realize capacitive $Z_{2L}$ termination when aiming for high efficiency Class B/J PAs in broadband operation.

IV. MEASUREMENT RESULTS

For practical validation of the proposed theory, GaN CG2H40010F device was used to design a broadband Class B/J power amplifier (PA) in a Rogers RO4003C board with a thickness of 32 mils. The quiescent current of the device was set at 25 mA with drain bias voltage of 28 V. The PA was stabilized using an input RC network with $R = 147 \, \Omega$, and $C = 2.4 \, \text{pF}$. Fig. 16 shows the extracted parasitic network which was used to access the intrinsic gate and drain terminal of the device. Using this terminal, intrinsic impedances were controlled across the desired band to realize Class B/J operation. Fig. 17(a) shows the schematic of the proposed PA with realized input matching network (IMN) and output matching network (OMN). Fig. 17(b) shows the picture of the implemented PA prototype.

The measurement of the designed PA was conducted using a test setup consisting of a signal generator EXG and signal analyzer EXA from Keysight as N5172b and N9010b, respectively. A pre-amplifier from Mini-Circuits, a 20W 30 dB attenuator, an isolator, and a power sensor was utilized to make a power drive-up test bench as shown in Fig. 17(c). The realized output matching network (OMN) trajectory of the PA is designed using the large signal model.

To exploit the maximum performance advantage of Class B/J operation, input second harmonic is designed in the region to be non-short, to shape input waveform using region determined by $\gamma$, $\phi_2$. The IMN is designed such that intrinsic $Z_{2L}$ trajectory follows the region on smith chart equivalent to Fig. 12 as shown in Fig. 18(c) at intrinsic node. The OMN is designed, with reference to intrinsic node, for optimal fundamental impedance with $Z_{2L}$ preferred to be in the capacitive region and $Z_{3L}$ to be near short in the smith chart as shown in Fig. 18(b). The extrinsic terminal impedance trajectory was accordingly observed and are as shown in Fig. 18(a). The PA prototype with input and output fundamental and harmonic

![FIGURE 18. (a), (b), (c) Intrinsic and extrinsic impedance trajectories for fundamental and harmonics. (d) Measured efficiency, output power and gain over the frequency. (e) Drain efficiency vs output power, and gain vs output power. (f) Drain voltage and current waveforms for 2.4, 2.6, and 2.8 GHz.](image-url)
match circuitry is shown in Fig. 17(b) implementing Class B/J mode operating in capacitive region for load second harmonic in order to ensure best possible efficiency for the intended frequency band.

As reported in Fig. 18(d), the measured drain efficiency (DE) across 2.2–3.4 GHz frequency band is between 60% and 72.8%, giving a fractional bandwidth of 42%. The PA provides saturated output power and gain above 40 dBm and 10 dB, respectively. The power drive-up for (2.2-3.4) GHz is shown in Fig. 18(e) up to 3 dB gain compression. To confirm the PA class of operation, the simulated drain voltage and current waveforms are reported at 2.4, 2.6 and 2.8 GHz, respectively in Fig. 18(f). As observed, the half sinusoidal voltage has $\sim 2.5xV_{dd}$ voltage swing while current is also half sine confirming the Class B/J mode of operation for the targeted performance over broadband range of frequencies.

Furthermore, the obtained results are benchmarked against the existing works in high-efficiency HT PA design. The purpose of this work is to analyze and find appropriate design space for broadband Class B/J PAs considering only reactive or nearly lossless harmonic terminations unlike bandwidth enhanced extended Class B/J PAs utilizing resistive harmonic loadings. The comparison is reported in Table 3 where the performance of the PA stands out in the literature so far.

The saturated power variation is less than 0.8 dB as compared to previous work without compromising efficiency and linearity across the band of the designed PA.

For assessment of linearity of the fabricated PA, a 10 MHz LTE modulated signal with peak to average power ratio (PAPR) of 10 dB is used at 33 dBm average power. The average efficiency of the PA is measured between 30% to 36% with uncorrected adjacent channel power ratio (ACPR) $-28.5$ dBc to $-32$ dBc as shown in Fig. 20.

The output of the PA is modelled and linearized by memory polynomial DPD model with memory depth of 5 and polynomial order of 7. Fig 19 shows the output spectrum for signal before DPD and after DPD model application. The corrected ACPR is below $-55$ dBc across the bandwidth as shown in Fig. 20.

V. CONCLUSION

For broadband PA design, input nonlinearity is inevitable since a harmonic short termination cannot be maintained in practice over broadband operation. This paper investigates waveform engineered broadband Class B/J PAs under the presence of input nonlinearity. The performance of broadband Class B/J PAs are mathematically modeled and explains
the performance variation in broadband Class B/J PAs in practice. It has been shown that it is indeed the input non-linearity which causes efficiency performance variation in Class B/J PAs across the $2\Delta L$ design space. As such, this work identifies and proposes capacitive $2\Delta L$ design space for broadband Class B/J PAs for optimum efficiency performance. Theoretical findings are validated with extensive load pull results. A proof-of-concept PA prototype implementing the proposed input-output harmonic design space was demonstrated showing efficiency 60−73% over the bandwidth 2.2−3.4 GHz. The PA shows excellent linearizability with corrected ACPR below −55 dBc.

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