Performance of a FPGA-based Direct Digitising Signal Measurement module for MIT

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Abstract. A novel MIT Direct Digitising Signal Measurement (DDSM) module has been developed aiming to replace the centralised NI PXI system and PC processing of the Cardiff Mk2 MIT system, thus offering potentially faster measurement cycles. The proposed module replaces the signal acquisition and offers local processing. The core of the system is a Xilinx Spartan-3 FPGA, paired with a dual 14-bit ADC capable of 120 MS/s. The FPGA provides a flexible and fast platform for data acquisition and processing. The phase is measured using a two channel phase sensitive detection via I/Q demodulation. Built-in averaging reduces the data to a single signal period of 12 samples before multiplying and accumulating the data with the I/Q signals. The system provides the I/Q values for both channels directly, eliminating the long download and processing times required by the centralised NI PXI system currently used in the Cardiff Mk2 MIT system. The module acquires both the measurement and the reference signal and has a phase noise as low as 7.5m° using a measurement time constant of 6ms. The phase drift over 6 hours is considerable at 119m°. Details of the module, circuits and algorithms employed are provided as are the results of the performance measurements.

1. Introduction
Magnetic Induction Tomography (MIT) is a contactless and non-invasive method to obtain cross-sectional images of the conductivity, permittivity and/or permeability of materials. A number of applications for MIT have been identified in biomedical and industrial areas [1]. A biomedical application currently being investigated is the detection and classification of cerebral stroke [2].

A MIT system induces eddy currents via a primary field into an object and the perturbed magnetic field is detected using an array of coils. The detected magnetic field will include both, the primary and the secondary field. For low conductivity materials, such as biological tissues (<5S/m), the secondary signal will typically be in-quadrature to the primary field and much smaller [3]. The measurement of the small in-quadrature signal, via the phase shift, provides a major challenge in biomedical applications of MIT.

A typical MIT measurement system uses an array of excitation coils that are excited sequentially. The received signal is processed with the reference signal to obtain the phase shift for each detection channel. For the classification of cerebral stroke a phase sensitive detection with a high degree of phase stability is required to obtain usable results (phase noise in the order of 1m°) [2]. Direct digitization of the received signals has been used in recent MIT systems using National Instrument (NI) PXI systems [4, 5]. However, the sequential data transfer between the PXI system and the PC, where the data is processed, and the processing time on the PC limits the speed of the overall signal
acquisition. A 14-channel version of the MIT system described in [5] requires 400ms for the data transfer plus a further 800ms for the data processing using an FFT (14-channels, Intel Core Duo) for a data length of 8.5ms (at 60 MS/s).

A novel MIT direct digitization signal measurement module (DDSM) has been developed with the intention to replace the centralized NI PXI system and PC processing [6]. The new module replaces the signal acquisition and offers local processing, thus offering potentially faster measurement cycles.

This paper describes the new module in terms of signal acquisition and signal processing. Phase noise and phase drift measurements are also described and their results are presented.

2. Methods

2.1. System Hardware

At the core of the DDSM is a Xilinx Spartan-3 FPGA with 1Mgates (XC3S1000-4) which is connected to a dual 120 MS/s 14-bit ADC (LTC2285). The external interface of the module is provided by a Microchip PIC microcontroller (PIC18F2480). The data transfer to the PC is done using the serial interface of the microcontroller and a PC application developed in LabWindows/CVI. Mathworks Matlab has been used to analyze the measured data.

Two types of measurement setups have been used for the DDSM. A single channel signal generator, TTi TDA 12101, has been used for the phase drift measurements, while a dual channel signal generator, TTi TGA 1242, has been employed for the phase noise vs. signal voltage level measurements. In both cases a 10MHz sine wave output has been fed to a resistive divider, followed by a set of differential amplifiers (LMH6626) before the ADC. The gain between the input of the amplifier and the ADC was 3.6. The input to the amplifier was varied between 56µVrms and 65mVrms (0.3mVrms – 350mVrms at the signal generator). An ADC input range of 1Vpp was selected. Figure 1 shows the principle of this setup.

![Figure 1. Signal chain for DDSM measurements.](image)

2.2. Phase Measurement Algorithm

The FPGA provides a flexible and fast platform for data acquisition and processing. The algorithm used here is a real-time I/Q demodulation with built-in time-averaging. The ADC samples the two 10MHz signals with 120 MSps simultaneously. Each of the 12 samples per signal period is accumulated during the acquisition cycle (time constant), leading to 12 large samples at the end of the acquisition cycle. These 12 samples are multiplied with the stored I/Q table (14-bit bit length), before being accumulated to give the I/Q value for the channel. The processing overhead is only 167ns per acquisition cycle. However, the pipelined design enables the DDSM to have only a gap of 25ns between cycles.

The algorithm was set up for a time constant of 1ms and 6ms. A total of 25 acquisition cycles were acquired without disabling the DDSM. This was repeated ten times for the phase noise measurement after a short delay (approx. 100ms). The measurement was only done once for the phase drift measurement.

3. Measurements

3.1. Phase linearity

The DDSM was connected to two output channels of the signal generator using identical cables. A signal level of 65mVrms at the input of the amplifier (350mVrms at the signal generator) was set for
both channels. The frequency was set to 10MHz and the phase was varied between 0° – 20°. The average of 16 phase measurements (1ms time constant) was used to determine the phase.

3.2. Phase noise vs. signal voltage level
The phase noise was measured with one of the channels amplitude adjusted between 56µVrms and 65mVrms (0.3mVrms – 350mVrms at the signal generator). The second channel was kept constant at 65mVrms. The phase noise was defined as the standard deviation of 10 measurements. Two sets of measurements with different time constants (1ms and 6ms) were conducted.

3.3. Phase drift
The output of a single channel was split and connected to the two channels of the DDSM. The amplitude for both was kept at 65mVrms, and the phase was measured every minute for 5 hours. The phase drift was defined as the difference between the maximum and the minimum of the measured phase.

4. Results

4.1. Phase linearity
A linear regression fit between the set and measured phase was applied. The R² value was found to be 0.9998.

4.2. Phase noise vs. signal voltage level
The phase noise was measured against the input voltage level at the amplifiers. Figure 2 shows the results from the measurement. The minimum phase noise is 7.5m°, while the maximum phase noise was 119.4m°.

![Figure 2. Measured phase noise vs. RMS input voltage level at amplifier (10MHz, Tc = 6ms, 120MS/s, 10 samples averaged).](image)

4.3. Phase drift
The phase drift was measured over 6 hours and is shown in figure 3 together with the phase noise. The measured phase fluctuated considerably over the period and the maximum difference was observed to be 119m°.
5. Discussion

The direct digitizing signal measurement module described achieves a phase noise as low as 7.5m° with a time constant of 6ms at 10MHz. The drift was considerable and fluctuated largely. The phase noise during the drift measurement was however consistently below 2.5m°. The NI PXI system reported by Wee et al. [5] achieved in comparison sub-milidegree phase noise and 3m° phase drift over 6 hours using a longer time constant (17ms instead of 6ms) and a variable gain amplifier (part of the NI PXI system). The low phase noise of the presented system during the phase drift measurements suggests that improvements can be expected through the optimization of the amplifier design.

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