Research of Coupled Inductance Three-Level Sepic Converter based on Parasitic Resistance

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Abstract. All components are accompanied by some parasitic parameters during the DC converter experiment. These parameters have a certain effect on the voltage conversion rate and efficiency of the converter. In this paper, a three-level Sepic converter with high-voltage gain and low-voltage stress coupled inductor is studied to optimize the performance of existing DC converters. Firstly, constructing the differential equation of the converter according to the state space averaging method. Then, calculate the relationship between voltage gain and converter efficiency under the influence of parasitic parameters for analyzing the impact of each parasitic parameter on circuit performance. At last, through the Saber simulation, a correct result of the parasitic parameters affecting the converter is obtained.

1. Introduction
Parasitic parameters are not negligible during the design of the DC-DC converter. Therefore, a converter operating mode and performance are analyzed under the influence of parasitic parameters based on coupled inductor three-level Sepic converter. As shown in Figure 1, compared to the traditional Sepic basic circuit, the topology first adds switching transistors and capacitors through three-level conversion to maintain symmetry. Therefore, the voltage stress of the switching transistor and capacitor is reduced by half [1-3]. Then, the limit duty cycle can be avoided under the requirement of increasing voltage by introducing a coupling winding [4-6]. Finally, the diodes are connected in parallel to the coupled windings to reduce energy losses.

Figure 1. Coupled Inductor Three-Level Sepic Converter
2. Converter working process

As shown in Figure 2, considering the leakage inductance of the circuit, the working process of the coupled inductor three-level Sepic converter is mainly divided into 8 stages. The key waveform of the Saber simulation is shown in Figure 3.

![Figure 2. Operating mode of the converter](image)

![Figure 3. Key waveform of the converter](image)

3. Steady-state analysis of converters and the influence of parasitic resistance

Steady-state analysis of four main working processes with consideration of some parasitic parameters: The two switching tubes $S_1$ and $S_2$ are simultaneously turned on. The switching tube $S_1$ is turned on, and the switching tube $S_2$ is turned off. The switching tubes $S_1$ and $S_2$ are turned on at the same time. The switch tube $S_2$ is turned on and the switch tube $S_1$ is turned off.

The converter is stable over a stable switching period. According to the volt-second balance law of the inductor, the change of the inductor current in the converter can be kept constant for one cycle. According to the capacitor's ampere-second balance rule, the change of the capacitor voltage of the converter can be kept constant in one cycle. Therefore, the converter has a static operating point and can be expressed as:

$$
\begin{pmatrix}
    di_1/ dt \\
    di_2/ dt \\
    dv_{c1}/ dt \\
    dv_{c2}/ dt \\
    dv_{c3}/ dt \\
    dv_{c4}/ dt 
\end{pmatrix} = A \begin{pmatrix}
    i_{c1} \\
    i_L \\
    v_{c1} \\
    v_{c2} \\
    v_{c3} \\
    v_{c4} 
\end{pmatrix} + B \begin{pmatrix}
    v_{st} \\
    v_{ds1} \\
    v_{ds2} \\
    v_{ds3} \\
    v_{ds4} 
\end{pmatrix}
$$

(1)

According to the formula (7), the matrix $A_1, B_1, A_2, B_2, A_3, B_3, A_4, B_4$ can be obtained by analyzing the above four working states.

Due to:

$$
A = A_1 \left( D - \frac{1}{2} \right)^* + A_2 (1-D) + A_3 (1-D), B = B_1 \left( D - \frac{1}{2} \right)^* + B_2 (1-D) + B_3 (1-D)
$$

(2)

It can be obtained:
After substituting the simplification, the voltage gain and circuit efficiency of the topology can be obtained without considering the leakage inductance:

\[
\eta = \frac{V_{d4}}{V_{d1}} = \frac{1 - D}{(n + 1) \frac{L}{C_0}} \left( a + b R + c R_1 + d R_2 + e R_3 + R_1 \right) + (1 - D) \left( R_{12} + R_{13} \right) \frac{R_1}{R_1}
\]

Where:

\[
\begin{align*}
\alpha &= (2nD - n - 1) \cdot (R_{12} + R_{13}) + (2nD - n + 1) \cdot R_1 + (1 - D) \cdot (R_{12} + R_{13}) + (1 - D) \cdot R_1 + \cdots \\
\beta &= (2nD - n + D) \cdot (R_{12} + R_{13}) + (1 - D) \cdot (R_{12} + R_{13}) + (1 - D) \cdot R_1 + \cdots \\
\gamma &= D \cdot (R_{12} + R_{13}) + (1 - D) \cdot (R_{12} + R_{13}) + (1 - D) \cdot R_1 + \cdots \\
\delta &= D \cdot (R_{12} + R_{13}) + (1 - D) \cdot (R_{12} + R_{13}) + (1 - D) \cdot R_1 + \cdots
\end{align*}
\]

The voltage gain and overall efficiency of the coupled inductor three-level Sepic converter with parasitic parameters can be analyzed by equations (7) and (8). Figure 4 is a comparison of voltage conversion capabilities under the influence of different parasitic parameters. It can be seen that the parasitic resistance of the coupled winding L1 has a great influence on the overall performance of the converter, and the remaining parasitic resistance has little effect on the circuit. Moreover, in the case of an open loop, the change in the load value causes a large change in the circuit. Overall, the trend of all the numerical curves is consistent with the sharp drop after reaching a certain duty cycle value. This indicates that the system should avoid excessive duty cycles to prevent the overall performance of the circuit from dropping rapidly.
It can be seen from Figure 5 that under the influence of parasitic parameters of each device, the overall efficiency is always less than 1. The efficiency curve first increases and then decreases. When D reaches 0.85, the curve begins to drop sharply. The converter should avoid the occurrence of the extreme duty cycle, which not only ensures the safety of the experiment, but also ensures the efficiency of the experiment. When the coupling winding turns ratio n is increased and the parasitic resistance is reduced, it is helpful for the overall efficiency.

Figure 6 is a diagram showing the relationship between the voltage conversion capability and the overall efficiency of a coupled inductor three-level Sepic converter with parasitic resistances of different values.

By analyzing the above three graphs of the important parameters of the coupled inductor three-level Sepic converter, it can be obtained: The parasitic parameters of the coupled winding $L_1$ have the greatest influence on the voltage gain and the overall efficiency of the converter. The load size also affects the system during open loop. Converter should focus on optimizing the parasitic parameters of the coupled winding $L_1$ to improve the overall efficiency and voltage gain. It is necessary to consider the influence of various factors such as parasitic parameters, duty cycle, voltage gain and parameter design efficiency, so that the converter can obtain the best experimental results to ensure its safety and efficiency.

4. Converter simulation analysis and verification
The main working process of the converter is verified by Saber software. Table 1 shows the parameters of the converter-related components during the simulation.
Table 1. The table of converter device parameters

| parameter | Numerical value | parameter | Numerical value |
|-----------|-----------------|-----------|-----------------|
| $L$       | 100μH           | $C_1$     | 470μF           |
| $L_1$     | 95.8μH          | $C_2$     | 470μF           |
| $L_2$     | 366.6μH         | $C_3$     | 1000μF          |
| $L_3$     | 366.3μH         | $C_4$     | 1000μF          |
| $n$       | 2               | $V_g$     | 12V             |
| $L_{ik}$  | 0.05μH          | $f_S$     | 20kHz           |
| $L_{2k}$  | 0.1μH           | $D$       | 0.75            |
| $L_{3k}$  | 0.08μH          | $R_L$     | 64Ω             |

Figure 7 is a schematic diagram of the open loop control simulation of the converter.

![Schematic diagram](image)

Figure 7. The principle diagram of the simulation

(a) and (b) in Figure 8 correspond to converter's input and output voltage simulation waveforms of the parasitic resistance $r_{L1} = 0.003$ Ω and $r_{L2} = 0.015$ Ω.
5. Conclusion
This paper analyses the steady-state working process of the coupled inductor three-level Sepic converter under the influence of parasitic parameters. Establish a state space model and conduct simulation experiments, analyse the effects of various parasitic parameters on circuit performance. It can be concluded that the parasitic parameters of the coupled winding $L_I$ have the greatest impact on the converter voltage gain and converter efficiency.

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