Temperature Dependent Current Dispersion Study in $\beta$-Ga$_2$O$_3$ FETs Using Sub-Microsecond Pulsed IV Characteristics

Abhishek Vaidya, and Uttam Singisetti

Abstract—A comprehensive study of drain current dispersion effects in $\beta$-Ga$_2$O$_3$ FETs has been done using DC, pulsed and RF measurements. Both virtual gate effect in the gate-drain access region and interface traps under the gate are most plausible explanations for the experimentally observed pulsed current dispersion and high temperature threshold voltage shift respectively. Unpassivated devices show significant current dispersion between DC and pulsed IV response due to gate lag effect characterized by time constants in the range of 400 $\mu$s to 600 $\mu$s. An activation energy of 99 meV is estimated from temperature dependent Arrhenius plots. A variable range hopping based slow transport in conjunction with the observed shallow trap level is attributed to the observed slow transient response of drain current with respect to time. Reactive ion etching step during the device fabrication is most likely responsible for introducing the traps. Effect of traps can be minimized by using surface passivation layers, in this case, Silicon Nitride which shows significant improvement in the current dispersion and RF cutoff frequency. This work demonstrates the detrimental effect the traps can have on the current dispersion which significantly limits the high frequency operation of the device.

Index Terms—$\beta$-Ga$_2$O$_3$, current dispersion, Interface traps, Pulsed IV, Virtual gate

1. INTRODUCTION

ETA Gallium oxide has garnered a lot of interest of researchers across the globe because of it’s attractive material properties such as ultra-wide bandgap of $\sim$4.8-4.9 eV [1], [2], good electron mobility, high breakdown field strength of 8 $MV/cm$ [3]–[6], and also the ease of growing high quality epitaxial films with controllable doping [7]–[14] on melt grown bulk crystals. The large breakdown field strength translates to high Baliga’s Figure of Merit ($BFoM$) making it superior candidate for power device applications. Several groups have demonstrated kilovolt class field effect transistors (FETs) and Schottky diodes [15]–[27]. In addition, $\beta$-Ga$_2$O$_3$ also has a high Johnson’s Figure of Merit ($JFoM$) owing to the large calculated electron velocity [28], which has been experimentally verified [29]. High $JFoM$ implies $\beta$-Ga$_2$O$_3$ is also suitable for high frequency devices such as GHz switches and RF amplifiers. Recently a few groups have successfully demonstrated $\beta$-Ga$_2$O$_3$ field effect transistors with current gain cutoff frequencies ($f_I$) in the GHz range [30]–[32]. Xia et al. reported the highest $f_I$ of 27 GHz in a delta doped $\beta$-Ga$_2$O$_3$ ($Ga_2O_3$)FET with regrown ohmic contacts [33].

In addition to the cutoff frequencies, another important factor for high frequency performance of the device is DC to RF drain current dispersion which causes transconductance to collapse as the frequency of operation increases with an associated knee-walk off phenomenon. This is primarily caused by interface and/or bulk traps which act as generation and recombination centers. The time constant associated with the traps dictates the amount of dispersion at an given frequency. Transient response analysis using pulsed current-voltage measurements is a popular method to identify the type and location, both physical and energy, of the trap. This method has been widely used to study dispersion in GaN based devices [34]–[39]. While, only a few reports exist on Ga$_2$O$_3$ devices.

There are two kinds of $\beta$-Ga$_2$O$_3$ RF FET devices reported; namely, (a) the source/drain (S/D) regions are either regrown or ion implanted and (b) the S/D $n^+$ layers grown and then removed from the channel region by reactive ion etching (RIE) which are called recessed gate FETs. The recessed gate process requires channel to be exposed to reactive ion etching which has been identified to introduce plasma damage and interface states [40]–[43]. This makes it vital to study the effect of traps and find ways to mitigate their detrimental effects on the device performance. There have been very few studies specifically on $\beta$-Ga$_2$O$_3$ devices. Moser et al. [44] have reported pulsed large signal power performance of $\beta$-Ga$_2$O$_3$ MOSFET. They have analyzed continuous and pulsed output power to provide evidence of presence of traps for the observed dispersion. In contrast, in a previous report, Moser et al. show pulsed current voltage characterization on a 200 nm bulk channel FET which shows no appreciable current dispersion [45]. A pulsed large signal RF performance was reported by Singh et al. [46] which shows negligible DC-RF dispersion with microsecond pulses. McGlone et al. explore buffer traps in a $\delta$ doped $\beta$-Ga$_2$O$_3$ structure using Deep Level Transient spectroscopy and double pulsed I-V measurements [47]–[49]. Joishi et al. report double pulsed...
current voltage measurement using a 5 µs pulse width on a Si δ-doped β-Ga₂O₃ FET which shows drastic improvement in current after in-situ passivation [50]. Nevertheless, significant knowledge gap exists in the DC-RF dispersion and mitigation strategies for Ga₂O₃ FET devices. In this work, we report a comprehensive temperature dependent DC-RF dispersion analysis in Ga₂O₃ MOSFETs using a minimum pulse width of 200 ns. We provide the origin of the DC-RF dispersion and the nature and location of traps along with the mechanism of capture and emission processes. We also first report the effectiveness of silicon nitride passivation in reducing the DC-RF current dispersion in Ga₂O₃ MOSFETs.

II. Experimental Details

The semi-insulating Ga₂O₃ substrates used in this study were grown by edge defined film fed growth method by Tamura Corporation, Japan. Device quality channel and ohmic capping epitaxial layers were grown homoeptaxially on top of 200 nm unintentionally doped (UID) Ga₂O₃ to act as a buffer layer. All the device layers including UID were grown by ozone molecular beam epitaxy (MBE). A gas mixture of ozone and oxygen was used as the oxygen source. The substrate temperature was 700°C, and the growth rate of Ga₂O₃ was 0.6 µm/hr. The channel and ohmic capping layer were grown with target thickness and doping concentrations of 200 nm / 7 x 10¹⁶ cm⁻³ and 50 nm / 1 x 10¹⁹ cm⁻³ respectively. Fig.1 shows the schematic of the device fabrication, electron beam lithography (EBL) was used in all the steps. Device isolation etch was first performed using inductively coupled plasma reactive ion etching (ICP RIE) with BCl₃/Ar chemistry. Next, Ti/Au/Ni source and drain contacts were deposited by e-beam evaporation followed by a 1 min / 520°C N₂ anneal to aid the formation of ohmic contacts. Followed by this, BCl₃/Ar gate recess etch was performed between source and drain (L sd = 0.5 µm) to remove the highly doped ohmic capping layer. A 20 nm plasma ALD SiO₂ was deposited as a gate dielectric layer and subsequently annealed at 450°C to improve its dielectric properties. Another lithography was performed to remove the oxide from source and drain contact pads, this time, using CF₃/Ar chemistry in ICP RIE. Finally, a Ti/Au gate contact pad and gate were deposited to complete the fabrication for the pre-passivation study. SEM micrographs were imaged using Carl Zeiss AURIGA CrossBeam. A 250 nm thick plasma enhanced chemical vapor deposition (PECVD) silicon nitride (SiNₓ) was deposited to study the passivation of the interface states. The SiNₓ was removed from the source/drain and gate contact pads to facilitate the probing.

For DC current-voltage (I-V) measurements HP4155B semiconductor parameter analyzer was used. A MS-TECH 1000H temperature controlled stage was used to measure up to 300 °C. Pulsed IV measurements were done using an Auriga AU-5 high voltage pulsed IV setup capable of sourcing 100 V/200 ns at input port and 200 V/200 ns at output port with 20 ns rise and fall time. The device was probed using a co-planar waveguide (CPW) RF probes to ensure minimum reflections at the probe-device interface (See Fig. 2).

To analyze the trapping/detraping response of traps, the well known gate-lag and drain-lag measurement technique was implemented as follows:

- **Gate turn-on:** Gate bias is pulsed from off state (V_g = -25 V) to on state (V_g = 0 V) while maintaining a constant drain bias. Complete IV curves are obtained by sweeping V_d from 0 V to 7 V.
- **Drain turn-on:** Drain bias is pulsed from off state (V_d = 0 V) to on state (V_d = 7 V) while maintaining a constant gate bias. Complete IV curves are obtained by sweeping V_g from -25 V to 0 V.

For each study, pulse width was varied from 200 ns to 1 µs with a pulse period of 20 ms to allow sufficient time for the traps to regain their original state after every pulse. The low duty cycle also ensures device self-heating effects are minimized. The number of samples were varied between 40 and 2000 based on the pulse width with highest samples for 1 ms pulse and lowest samples for 200 ns pulse. For each pulsed measurement, the recorded I_d value was averaged over last 10% time window of the pulse. The measurements were repeated for high temperatures up to 200°C before and after passivation.

![Fig. 1. The figure highlights major steps in fabrication process flow of the device in this study.](image)

![Fig. 2.](image)
Fig. 3. (a) SEM micrograph of the device showing large source and drain contact pads. (b) Zoomed in view of the gate recess region showing intrinsic part of the device.

S-parameter measurements were carried out using Agilent E5071 series ENA. The measurements were repeated after passivation.

III. RESULTS AND DISCUSSIONS

The final dimensions of the fabricated device are; gate length (L_g) = 112 nm, Source-Gate spacing (L_sg) = 50 nm and Gate-Drain spacing (L_gd) = 340 nm. Fig. 3 shows SEM micrograph of the fabricated device.

A. DC I-V Analysis

Fig. 4(a) and (b) show the measured I_d-V_d characteristics at room temperature and 200°C respective. At room temperature we see incomplete turnoff even at V_g=-25 V. It is attributed to the moderately high doping in the channel, a thicker channel and a smaller gate length resulting in a reduced control over the channel current. Gate voltages lower than -25 V were avoided to protect devices from gate dielectric electrical breakdown. The short channel effects are also evident due to shorter gate length. A maximum current of 210 mA/mm was recorded for this device at V_g=0 V. Non-ideal behaviour of source-drain contacts can also be seen in the graph which is a consequence of non-optimized contact formation process. This also results in higher source and drain resistances which reduces the net drain current and transconductance. The device shows improved ON/OFF ratio at 200°C for the same V_g as indicated in Fig. 4(b) (solid red line) which is due to a threshold voltage shift that can be attributed to mobile trapped charges in the gate oxide. Contact linearity is improved at this temperature most likely due to reduced thermionic emission barrier. The figures also show that there is a small change in DC I-V characteristics after SiN passivation.

Fig. 4(a) and (b) show temperature dependent I_d-V_g plots before and after passivation at room temperature (blue), 100°C (green), 150°C (orange), and 200°C (red). (c) V_t shift with temperature data before and after passivation shows a similar monotonic positive shift in V_t. (d) Peak g_m vs Temperature data before and after passivation indicates little to no change in maximum static g_m.

B. Pulsed I-V Analysis

As described in the Introduction, pulsed I-V analysis is important to study the DC to RF dispersion that arise from the dynamic response of traps with change in bias. We carried out drain turn on and gate turn on pulsing individually to isolate the effects of interface traps and bulk traps and localize the source of current dispersion.

Drain Turn On: We first discuss the drain pulse measurements, as the bulk traps are expected to respond to drain pulse [51], [52]. Fig. 5 (a) shows device response to drain turn on pulse before and after passivation showing negligible dispersion in the I_d-V_d plots for different pulse widths. Fig. 5 (b) shows the drain current pulse which does not show any delays in either transient edges. This rules out presence of any significant buffer traps. Fe diffusion from substrate has been identified as a trap in MBE grown Ga2O3 devices [47]. However, the ozone MBE growth of the Ga2O3 does not show any appreciable Fe diffusion as seen in Fig. 3 in Ref. [53]. The same growth...
conditions are used in this study and the fabrication flow does not involve high temperature (> 520°C) processes. If both drain and gate are pulsed, we see change in the device characteristics as seen in Fig. 7. This is due to the gate lag effect caused by interface traps which is discussed in the next section.

**Gate Turn On:** Figure 8(a) shows DC and and gate pulsed $I_d-V_d$ characteristics of the unpassivated device, we can clearly see severe DC-RF dispersion and knee-walk off. The current collapse during gate turn on pulse could be related to both traps directly under the gate electrode and the traps in the gate-drain access region [52]. Fig. 8(b) shows the $I_d-V_d$ at a constant $V_{gs}$ as a function of pulse width. The current collapse increases with decreasing pulse widths. As discussed in the previous section buffer traps are ruled out. The dispersion is caused by interface traps under the gate and in the gate-drain access region.

Fig. 9(a) shows the temperature dependent time domain plot of drain current response to a $1 \text{ ms}$ gate turn on pulse. At all temperatures the drain current pulse shows a delayed asymptotic turn on transient which could be associated with emission time constants of electrons from the traps both in the gate-drain access region and the gate region. This pulse profile makes it self-explanatory as to why we see an increased current dispersion between static and pulsed $I_d-V_d$ data with reduced pulse widths. A similar behaviour is seen during the turn off transient edge of $I_d$ data with reduced pulse widths. A similar behaviour is seen for the slight difference in pulse shapes for different temperatures. Inset of Fig. 9(a) shows extended turn off transient for room temperature pulse to illustrate the slow capture process of electrons by traps after the gate voltage pulse returns to it’s base value. As shown in Fig. 2(b), more negative the base voltage of the pulse, greater is the current collapse for the same pulse width. This is obvious since more negative base voltage would trigger more trapping of charges due to which drain current takes longer time to recover.

### C. SiN$_x$ passivation

According to the reports in previous studies on AlGaN/GaN devices [51], [54]–[56], SiN$_x$ passivation has helped create a near ideal semiconductor-dielectric interface by neutralizing the surface charge due to defects, dangling bonds and charged residuals. We explore the effect of SiN$_x$ passivated on RIE treated Ga$_2$O$_3$ devices.

Fig. 10 compares pulsed I-V plots of the device post passivation with that of before passivation. We see a reduced DC-RF dispersion after passivation especially the low frequency dispersion is significantly reduced confirming that the role of traps in the gate-drain access region. While $I_d-V_d$ data corresponding to $1 \mu s$ and $200 \text{ ns}$ pulse widths still show dispersion, they both show considerable improvement in $I_d$ value over unpassivated device. The most likely reason for this dispersion

![Fig. 6. (a) Drain turn on $I_d-V_d$ curves for various pulse widths at $V_{gs} = 0$ showing negligible current dispersion compared to Fig. 8(b). (b) Drain turn on pulse with pulse width of $1 \mu s$ showing no trapping effects which reduces the plausibility of bulk traps causing the current dispersion.](image)

![Fig. 7. Double pulsed transfer curves using a $50 \mu s$ pulse width for both gate and drain voltage pulses using the quiescent bias conditions as indicated in the figure. The black curve represents minimum trapping and hence more drain current levels while the red curve has reduced current due to trapping.](image)

![Fig. 8. (a) Drain current profiles for $V_g = 0V$ to $V_g = -25V$ for DC (red solid lines) and 200 ns pulse width (black dotted lines), before passivation. (b) Complete $I_d-V_d$ profile from DC to 200 ns pulse width before passivation for $V_g = -25V$ shows clear dispersion in drain current with decreasing pulse width.](image)

![Fig. 9. (a)Temperature dependent drain current pulse profile for a $1 \text{ ms}$ gate turn on pulse. Graph indicates how the traps response with temperature affects the drain current transient. Inset is room temperature plot for the same pulse width with extended turn off transient showing delayed effect due to capture time constants related to traps. (b) Change in maximum drain current recorded at $V_{gs} = 0V$ depending on the base voltage of the pulse for varying pulse widths as indicated. A more negative base voltage assists more trapping and thus more current collapse.](image)
is traps under the gate which are still in play. The temperature dependent drain current transients in Fig. [11] clearly show the reduction of low frequency dispersion. Compared to the unpassivated drain current pulse, the passivated data is close to ideal square wave pulse shape except a very small delay at the end of the turn on and turn off transient which is responsible for the current dispersion seen in shorter pulse widths. High temperature pulse also shows a consistent improvement over its corresponding unpassivated pulse.

To get a more quantitative idea of the effect of passivation on current collapse we have calculated percentage current collapse in relation to DC data as a function of temperature before and after (solid lines) passivation for V_{ds} = -0.7V shows significant improvement in drain current dispersion down to 10 µs pulse width.

Following the data and analysis in previous subsections we discuss the origin of the DC-RF dispersion. Since it is highly unlikely that as grown MBE substrate had a high concentration of surface traps, reactive ion etching step is responsible for the defect related interface traps observed in this study. A comparison with other published results shows that similar DC-RF dispersion was seen in [44] which used RIE for the channel layer. There has been report of RIE induced channel depletion in Ga_{2}O_{3} MESFETs [50]. While devices where the channel is not exposed to RIE [45], [46] show negligible DC-RF dispersion. Thus, the most likely cause of the dispersion in these devices are caused by RIE induced traps. During etching, Ga vacancies are created which leave behind three dangling \( O \) bonds that acts as a triple acceptor site according to McClusky et al. [57]. These traps form a virtual gate leading to depletion of electrons in drain access region which has slow turn on time when the gate is turned on.

The detrapping of electrons and hence the time response can occur by two possible methods: 1) thermionic emission from the trap, the rate for which is governed by the temperature of operation and/or 2) variable range hopping as described in [35].

Assuming a discrete or narrow band of traps in terms of energy level, the time constant of the traps can be determined by curve fitting a stretched exponential function in Eq. (3) to the drain current transient as shown in Fig. [13] (a).

\[
I_{d,slow} = 1 - \exp \left( \frac{t}{\tau} \right)^{\beta}
\]

where \( I_{d,slow} \) is the normalized slow transient, \( \tau \) is the time constant and \( \beta \) is the fitting parameter. A slow time constant of 421 µs is obtained. From this time constant, the trap level is calculated [58] using Eq. (4).

\[
E_{c} - E_{t} = kT \cdot \ln \left( \frac{\tau \cdot \sigma_{n} \cdot \nu_{n} \cdot g_{1} \cdot N_{c}}{g_{0}} \right)
\]

where \( E_{c}, E_{t} \) are conduction band edge and trap energy levels respectively, \( \sigma_{n} \) is electron capture cross section of
the trap, \( \nu_0 \) is the thermal velocity of electron, \( g_0/g_1 \) is degeneracy of the trap when it is occupied by 0/1 electron and \( N_c \) is conduction band density of states. Assuming \( \sigma_n = 10^{-15} \, \text{cm}^2, \nu_0 = 10^7 \, \text{cm/s}, N_c = 3.72 \times 10^{18} \, \text{cm}^{-3} \) for this calculation. The calculated trap level is deep with an energy level of 0.41 eV below conduction band. However, a deep trap such as 0.41 eV would present decreasing time constant with increasing temperature according to Shockley-Read-Hall recombination theory. The device performance was degraded by high source drain resistances and trapping which is due to reduced trapping in the access region that improves the cutoff frequency by approximately two times.
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