Capacitance-controlled oscillator optimization for integrated capacitive sensors with time/frequency-based conversion

Jelle Van Rethy\textsuperscript{a,*}, Hans Danneels\textsuperscript{a}, Kristof Coddens\textsuperscript{b}, Georges Gielen\textsuperscript{a}

\textsuperscript{a}K.U.Leuven, Dept. Elektrotechniek ESAT-MICAS, Leuven, Belgium

\textsuperscript{b}Melexis, Tessenderlo, Belgium

Abstract

Technology scaling improves timing resolution, but diminishes voltage resolution, so time-/frequency-to-digital conversion is gaining popularity. In traditional amplitude-based converters, the sensor signal typically has to be pre-processed (amplified, filtered, etc) before feeding it to the converter. In the context of time-based converters, the conversion of the sensor to a frequency/time signal can be seen as pre-processing, after which it is fed to the time-to-digital converter. This paper focuses on the optimized conversion of a capacitive sensor (MEMS) to a time/frequency signal by using a Capacitance-Controlled Oscillator (CCO). In this way the sensor is directly converted to a usable time signal, so other pre-processing such as amplification and filtering can be avoided. Different oscillator topologies are investigated, designed in UMC130 CMOS technology, and compared to each other, based on key parameters such as tuning range, linearity, phase noise and power consumption. It is indicated which oscillators are suited for which applications.

© 2011 Published by Elsevier Ltd. Open access under CC BY-NC-ND license.

Keywords: Capacitive sensor; time-based conversion; integration; capacitance-controlled oscillator

1. Introduction

Due to the ongoing trend towards smaller CMOS technologies, conventional amplitude-based converters suffer from decreased supply voltages and non-idealities [1]. Converting the sensor signal to the time domain can counter most of these problems, because digital circuits suffer less from lower supply voltages and non-idealities due to mismatch, noise, non-linearities, etc. Since time-based converters are gaining popularity, ways have to be investigated to generate a time signal out of a sensor.
One possibility is to generate an amplitude sensor signal (e.g. charge-pumping for capacitive sensors), which is then fed to a Voltage-Controlled Oscillator (VCO). However, the generation of the amplitude signal requires extra building blocks that also consume power and inject extra noise into the sensor signal. Therefore, this work focuses on the total integration of the capacitive sensor into an oscillator (Capacitance-Controlled Oscillator (CCO)), without extra signal processing. The time domain signal can then be digitized by the use of an open-loop time-to-digital converter (TDC), PLL-based structure [1] or other time-to-digital structures.

2. Design parameters and oscillator topologies

To make a fair comparison between different oscillator topologies, different parameters need to be investigated and compared to each other. First, parameters such as sensitivity/tuning range define the dynamic range of the output (time) signal. Increasing the sensitivity of the CCO will mostly result in a higher resolution of the sensor-to-digital conversion. Second, calibration of sensor (interfaces) is almost inevitable but comes with an extra cost. A high linearity of the sensor-to-frequency conversion can result in an easier calibration (e.g. 2-point calibration) and linear blocks are preferred in most systems, making a linear input-output characteristic very interesting. Third, CCO phase noise corresponds to jitter in the time domain and will of course influence the resolution and precision of the time-to-digital conversion. In amplitude-based converters, the noise floor will limit the resolution, whereas jitter in the time domain will do that. Low phase noise values can be achieved at the expense of more power consumption. On the other hand, capacitive sensors are widely used in low-power applications, so a high power consumption of the CCO will ruin the capability of using the sensor interface in this kind of applications. So besides phase noise, power consumption is another important and the fourth and last parameter to be investigated. The tuning range, phase noise and power consumption values will be combined in an already published Figure Of Merit (FOM) [2], revealing the trade-offs in the designs.

![Fig. 1. Unit cell of (a) Standard ring oscillator (7-stage), (b) Current-starved ring oscillator (7-stage, R=1k), (c) Coupled-sawtooth (7-stage), (d) Differential (4-stage)](image)

The investigated CCO topologies are depicted in Fig. 1, and include the standard ring oscillator (7-stage) (a), the current-starved ring oscillator with resistors (7-stage) (b), the coupled sawtooth (7-stage) (c) and a fully differential topology (4-stage) (d). In all of these, a capacitive sensor $C$ with $C_0 = 5\text{pF}$ and a variable range of 1pF is integrated in one stage, while the other stages are loaded with the same capacitance $C_{\text{load}}$, which is swept from 1-5pF, resulting in different designs. This is to investigate the influence of symmetrical and asymmetrical loading on the different stages. To make a valid comparison, every oscillator is designed with equal stages and equal free-running frequency $f_0$, which is 10 MHz.
3. Results

Every oscillator topology is designed for 5 different $C_{\text{load}}$, resulting in 20 different designs in total. The Percentage Tuning Range (PTR), which is defined as $TR/f_0$, is plotted in Fig. 2 (a) for the different oscillator topologies as a function of $C_{\text{load}}$. It is clear that when the stages, besides the stage that is loaded by the sensor, are loaded more symmetrically with respect to the sensor stage, the tuning range decreases (~ sensitivity of the output frequency to the capacitive sensor). However, the linearity of the conversion characteristic increases (Fig. 2. (b)) when the CCO is more symmetrically loaded, revealing a first trade-off. For both parameters, the differential topologies (c) and (d) perform the best. Fig 3. (a) shows the phase noise for the different designs. The phase noise decreases for a more symmetrically loaded design ($f_0 = \text{constant}$), but the power consumption increases (Fig. 3. (b)), which is the second trade-off. If we combine three of the four parameters (PTR, phase noise and power) into a FOM [2], we obtain the plot in Fig. 4. (a). The FOM does decrease slightly as a function of $C_{\text{load}}$, but remind that the linearity (which is not included in the FOM) does improve, so in the end, the trade-offs remain. The single-ended topologies outperform the differential ones, mainly because of the low power consumption (only dynamic) and the better phase noise values. But in standard simulations, only inherent noise of the oscillator is taken into account when computing phase noise and no external noise such as supply and substrate noise.

![Fig 2](image1.png)
![Fig 3](image2.png)
It is known that differential structures are more robust towards supply and substrate noise [3], so when supply noise is added, it is clear the differential ones start to dominate (see Fig 4. (b)). In Table 1, absolute results are summarized for the case where \( C_{\text{load}} = 3 \text{ pF} \) for the different topologies.

![Graph](image)

Fig 4. (a) FOM (\( C_{\text{sensor}} = 5 \text{ pF} \)) as a function of \( C_{\text{load}} \) for the different topologies; (b) FOM for the case \( C_{\text{load}} = 3 \text{ pF} \) as a function of added low-pass filtered supply noise.

\[
FOM = 10 \log \left( \frac{f_c^2}{\Delta f^2 \cdot L(\Delta f)} \cdot \frac{1}{P(mW)} \right) \left( \frac{PTR}{10} \right)^2
\]

Table 1. Comparison of the different oscillator topologies with integrated capacitive sensor for the specific case \( C_{\text{load}} = 3 \text{ pF} \). The FOM is calculated with and without low pass filtered supply noise.

| Osc. | \( f_0 \) [MHz] | Percentage Tuning Range (PTR) | Phase Noise [\( V^2_{\text{s,rms}}=0 \text{mV}^2 \)] | Max. Linearity Error [%] | Power [\( V^2_{\text{s,rms}}=0 \text{mV}^2 \)] | FOM [\( V^2_{\text{s,rms}}=32 \text{mV}^2 \)] |
|------|----------------|-------------------------------|-----------------|------------------------|-----------------|-----------------|
| (a)  | 10.004         | 3.45                          | -116.74         | 0.1118                 | 367             | 151.85          | 124.9           |
| (b)  | 10.002         | 3.42                          | -118.74         | 0.1142                 | 383.7           | 153.58          | 130.69          |
| (c)  | 10             | 3.94                          | -108.91         | 0.0832                 | 1219            | 139.96          | 135.24          |
| (d)  | 9.95           | 6.45                          | -109.70         | 0.1481                 | 2093            | 142.68          | 138.22          |

4. Conclusion

It is clear that trade-offs have to be made when choosing topologies and capacitive loading, depending on the target specifications. More symmetrical structures tend to have better linearity and phase noise, but consume a lot more power and have lower sensitivity to capacitive sensor variations. Differential topologies mostly are preferred over single-ended ones because of the lower sensitivity to substrate and supply noise.

Acknowledgement

The first author is funded by FWO Vlaanderen. The authors also like to thank IWT and Melexis.

References

[1] H. Danneels, F. Piette, V. De Smedt, W. Dehaene and G. Gielen, “A Novel, PLL-based Frequency-to-Digital Conversion Mechanism for Sensor Interfaces”, Sensors & Actuators: A. Physical (2011), available online.

[2] D. Ham, A. Hajimiri, “Concepts and Methods in Optimization of Integrated LC VCOs”, IEEE JSSC, Vol. 36, No. 6, June 2001

[3] A. Hajimiri, S. Limotyrakis, and T. Lee, “Jitter and phase noise in ring oscillators,” IEEE JSSC, vol. 34, no. 6, pp. 790 – 804, 1999.