A 1.2V, 7.5ppm/°C Bandgap Reference with Start-up and Power Down Circuit

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Abstract. A reference voltage is expected to be stable against process variation, voltage supply and temperature. The architecture of bandgap reference circuit in this paper consists of start-up and power down circuit to minimize power dissipation in system on chip application. The circuit is simulated using Cadence tools in 0.18µm Siltegra CMOS technology and operated with 1.8V±8% supply voltage. Based on the post layout simulation, the bandgap reference circuit generated 1.202V stable voltage with temperature coefficient of 7.5ppm/°C over temperature range -40°C to 100 °C and -78.9dB power supply rejection ratio at DC frequency. The simulation results show that the circuit is well function to supply a stable input voltage to another circuit application such as Analog Digital Converter.

1. Introduction
Reference circuit is an important block to provide a constant DC voltage independent and insensitive from process changes, supply voltage and temperature (PVT). It is important that the reference circuit must be precise functioning for example as an input for Analog Digital Converter (ADC) circuit. The resolution of the bit converter is affected by the accuracy of the stability voltage input and temperature range [1].

The reducing transistor size has also stimulated the trend of system integration into a full-chip Silicon-on-Chip (SoC). As the technology growth fast, system integration SoC encourages into many applications. To maintain the operation of the system, the battery frequency replacement will be taken into consideration. The power consumption requirement is a critical issue that every circuit design must be prepared as a main factor for circuit design specification [2]. To reduce the power use in a system, the circuit should have low current voltage and also Power Down (PD) system. This reference circuit will provide start up and power down circuit to minimize battery operation and also fulfills the specification of current consumption, with minimum temperature coefficient, wide temperature range and acceptable Power Supply rejection ratio (PSRR) across corners simulation.

2. Bandgap Reference Architecture
The topology of Bandgap Reference (BGR) has been introduced since 1971 and was followed by Brokaw in 1974. This Bandgap reference circuit designed based on Brokaw topology by using...
characteristic of base-emitter voltage of two Bipolar Junction Transistor (BJT) biased at unequal current densities can provide a temperature independent voltage [3].

2.1 Bandgap Reference Core
A stable BGR voltage with temperature is obtained by Voltage Complementary to Absolute Temperature (VCTAT) derived from the BJT base-emitter voltage (VBE) compensated by the Voltage Proportional to Absolute Temperature (VPTAT) by the difference of VBE voltages of \( n \) number BJT operated under different current densities. Figure 1 shows a basic principle of BGR and can be represented as equation 1. VCTAT is the VBE biased with constant current that has a negative temperature coefficient (TC) of \(-2 \text{ mV/}^\circ\text{C}\) and VPTAT is \( \Delta \text{VBE} \) proportional to the thermal voltage, \((\text{VT})\) that has a positive temperature coefficient of \(0.086 \text{ mV/}^\circ\text{C}\). By appropriately scaling the value of resistance ratio and the numbers of BJT between two difference voltages the stable 1.2V reference voltage can be produced [4].

![Figure 1: Basic principle of bandgap reference [5]](image)

\[
V_{BG} = V_{BE} + V_T \ln \left( 1 + \frac{R_2}{R_1} \right)
\]  

(1)

The architecture of bandgap reference is shown in Figure 2. To produce proportionate temperature of VCTAT, five BJT transistors of Q2 are chosen and 9.375 value of resistance ratio, \((R_2/R_1)\) has been determined to increase the current densities of VPTAT. The two-stages op-amp differential amplifier was used in this design. The loop gain of the op-amp is 70dB resulting the output that sufficient to drive the R1 and R2 resistors. The first stage differential amplifier contains of transistors M8-M14 and transistors M15 is a common-source amplifier transistor. By placing C1 capacitor as a Nested-Miller compensation technique, it can improve BGR circuit phase margin for better stability and faster settling time [6].
2.2 Start-up Circuit and Power Down
To solve the power dissipation of the BGR, this design will use start-up and power down circuit. The start-up circuit will avoid unnecessary operation current of the BGR after stable voltage was reached. Meanwhile, the power down will disable the operation when the BGR circuit is not in use. The enable (EN) input as shown in Figure 2 would power up the circuit when the input is high. The start-up circuit consists of series of diode-connected transistor, M5 and gradually switch on when EN =1 and increase the Vg voltage of M7. With that increasing voltage, transistor M7 will turn ON and the current flows through M7 giving signal to start-up the bandgap core circuit to the stable voltage. Besides that, the current also flows through transistor M6 that pulls down the Vg voltage of M7 and turn it OFF. Hence, the start-up circuit will turn off and the BGR circuit operates.

During the power down mode, EN = 0, the transistors M1-M4 work as switches and transistor M16-M20 will pull down every node of bandgap core transistor to be isolated from the power supply. This technique will reduce the power dissipation during power down mode.

3. BGR Layout design
The layout of BGR has completed with zero Design Rule Check (DRC) and without Layout Versus Schematic (LVS) errors as shown in Figure 3. The post layout simulation results including the parasitic extraction using Calibre view are verified. The layout also consists of common centroid technique for matching purpose and including dummies. The active silicon area of the BGR circuit is 0.027mm² smaller than previous designed [12].
4. Result and Discussion

The BGR circuit was designed by using 0.18\(\mu\)m Silterra CMOS process with the supply voltage of (VDDA) 1.8V with \(\pm8\%\) rate of change and separated bulk source to prevent the short channel effect result. The post-layout result was simulated through five process corners (TT, SS, SF, FS and FF) with temperature variation ranging from -40 to 100\(^\circ\)C. There are nine matrix conditions consist of three conditions of supply voltage (1.65V, 1.8V and 1.95V) and three temperature conditions (-40\(^\circ\)C, 27\(^\circ\)C, 100\(^\circ\)C).

4.1 Temperature Coefficient Analysis

The DC analysis gives bandgap reference voltage, VBG as a function of temperature. Figure 4 shows the VBG variation of typical corners, while Figure 5 shows VBG variation for five corners analysis. The variation of VBG value in typical process is 1.2658mV, maximum variation is 1.3008mV (FF, 27\(^\circ\)C, 1.65V) and minimum is 1.2373mV (SS, -40\(^\circ\)C, 1.95V). By using equation in (2), the temperature coefficient of typical corners is 7.52ppm/\(^\circ\)C and for the most extreme corners is 7.73ppm/\(^\circ\)C. This result shows low temperature coefficient result compared with previous design [9][10][11][12].

\[
ppm/\circ C = \frac{VBG_{max} - VBG_{min}}{VBG_{typ} (T_{max}-T_{min})} \times 10^6
\]  

(2)

Figure 3: Bandgap reference layout design
4.2 Bandgap Reference Transient Analyses

Transient simulation analyses in Figure 6 shows the settling time of BGR output. It is found that the circuit acquired 35µs to produce stable output when the supply voltage ramping up from 0V to 500ns. The enable signal from Figure 7 shows the VBG output when EN signal is high and in power down mode. It can be observed during active mode the current is 53.54µA, and 252.5pA in power down mode for typical condition. Therefore, the power consumption of this circuit is 96.4µW and consume minimum power dissipation during power down mode compare with design in [7]. The value of VBG for typical process is 1.20192V while the maximum value is 1.20199V and minimum value is 1.20058V, thus the constant voltage (CV) for the VBG is 0.135%. The close up graph in Figure 8 shows the stable output of BGR across corners can be observed.
Figure 6: VBG settling time

Figure 7: VBG Power Down analyses

Figure 8: VBG output over five process corners
4.3 Bandgap Reference Power Supply Rejection Ratio (PSRR)

The PSRR value of the circuit is -78.86dB at typical corners at 27°C DC as in the PSSR Vs frequency plot in Figure 9. The maximum value of PSSR is -119.5dB (SF, 27°C, 1.95V) and the minimum value is -71dB (SF, 40°C, 1.65V). The result shows the PSSR values are acceptable for every corners process. The performance metric comparison between propose bandgap reference circuit and a set of other state of the art are shown in Table 1.

![Figure 9: PSRR value of VBG](image)

Table 1. Performance comparison with previous Bandgap reference circuits

| Parameter                     | [7]  | [8] | [9]  | [10] | [11] | [12] | This work |
|-------------------------------|------|-----|------|------|------|------|-----------|
| CMOS process (µm)             | 0.15 | 0.18| 0.18 | 0.18 | 0.18 | 0.18 | 0.18      |
| Power supply(V)               | 3.3  | 1   | 1.25 | 0.536| 1.1 -2.2| 3.3  | 1.7 -1.9 | 1.8±8%    |
| VBG (V)                       | 1.25 | 0.7136| 0.536| 0.8  | 1.25 | 1.176 | 1.202     |
| Temperature Range(°C)         | -55-125| -40-120| -40-85| -40-125| -40 -125 -40 -140 | -40 -100 |
| Total Current(µA)             | 704.84| 49.3 | 0.24 | 13.2 | 84   | 50   | 53        |
| TC (ppm/°C)                   | 0.758| 3.23 | 19.302| 9    | 11.6 | 13   | 7.5       |
| Area(mm²)                     | NA   | 0.03 | 0.0077| 0.04 | 0.014| 0.05 | 0.027     |
| PSRR(dB) @ DC                 | -82  | -57@1kHz | -55@10Hz | -108 | -115 | NA   | -78.9     |

5. Conclusion

A 0.18µm CMOS bandgap reference with start-up and power down circuit was designed and the post layout simulation was verified. The circuit was simulated for five process corners (TT,SS,FS,SF,FF) by using 1.8V ±8% supply voltage over temperature of -40°C to 100°C. A 1.202V stable voltage reference has been produced with TC 7.5ppm/°C and PSRR at DC frequency -78.9dB in typical corners. It can be concluded that the BGR circuit is compatible for system on chip application because it can be operated over wide range of temperature, low temperature coefficient and also high PSRR ratio in all corners. Besides that, with the power down circuit designed, it is well suit for low power dissipation and also occupied layout area of 0.027mm².

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