Design and Implementation of Viterbi Decoder Using VHDL

Akash Thakur and Manju K Chattopadhyay

VLSI Design and Embedded System Lab, School of Electronics,
Devli Ahilya University, Indore, India
E-mail: akashth28@gmail.com

Abstract. A digital design conversion of Viterbi decoder for $\frac{1}{2}$ rate convolutional encoder with constraint length $k = 3$ is presented in this paper. The design is coded with the help of VHDL, simulated and synthesized using XILINX ISE 14.7. Synthesis results show a maximum frequency of operation for the design is 100.725 MHz. The requirement of memory is less as compared to conventional method.

Index Terms—VD, VHDL, RTL, BMU, PMU, ACSU, SMU.

1. Introduction

Encoders and decoders play an important role in the field of communication and data storage industries. There is a need of reliable system with least probability of error and high speed of operation. Error correcting coding [1] has algorithms for expressing a sequence of numbers, so that if any error due to noise arises, it can be detected and corrected (within certain limitations). These algorithms come into operation by converting them into digital design. The digital conversion will work at certain frequency.

Recent developments have contributed towards achieving high reliability required by today’s high-speed digital systems. The use of coding for error control has become an integral part in the design of modern communication and digital storage systems.

A typical transmission or storage system may be represented by the block diagram shown in figure 1.

Efficient error control code in encoder and decode can help in gaining the following advantages:

a. Power gain by coding in power/bit for cellular systems in digital communication.

b. Increase in storage capacity (no. of bits per sq. inch increases)

Even though the concept of Viterbi algorithm is very old, it is still very much researched for its optimization. Jinjin He et al. [2] presented paper on low power design of Viterbi decoder without degrading the decoding speed. K. S Arunlal and S. A Hariprasad [3] shows the reduction in computational time and hardware requirement. The crucial point among the digital design conversion is the operating speed and the power reduction, which is presented by many researchers with variation in operating frequency and reduction in digital complexity [4-9]. D Vaithiyanathan et al. [10] proposed a modified pipelined...
architecture for ACS of Viterbi decoder and shows optimization in frequency of operation, up to 165 MHz with reduced area. The design proposed by us reduce the memory requirement for the trace back of the trellis.

2. Architecture

Viterbi Algorithm is an efficient way to implement the ML Decoding, for both hard and soft decision. It is easy to implement for small constraint length for convolutional encoders which is based on the trellis method. A J Viterbi proposed Viterbi algorithm in 1967 for convolutional codes. The basic architecture of the Viterbi Decoder (VD) based on Viterbi algorithm is shown in figure 2.

![Figure 2. Block Diagram of Viterbi Algorithm](image)

The main components of the VD are Branch Metric Unit (BMU), Path Metric Unit (PMU), Add-Compare and Select Unit (ACSU) and Survivor Management Unit (SMU). Viterbi Decoder decodes the convolutional encoded data on the basis of trellis. An intermediate state of the trellis for a Viterbi decoder of $1/2$ rate convolutional encoder with constraint length $k=3$ is shown in figure 3.

![Figure 3. Intermediate trellis state of the decoder](image)

A Branch Metric Unit-BMU calculates the branch metrics; An Add-compare-Select Unit -ACSU recursively accumulates the branch metrics. Path metrics (PM), compares the incoming path metrics, and makes a decision to select the most likely state transitions for each state of the trellis and generates the corresponding decision bits. Viterbi algorithm is a special case of Bellman Ford shortest distance algorithm.

3. Hardware Description

The proposed digital design of the Viterbi decoder for $1/2$ rate convolutional encoder of constraint length of $k=3$ is shown in the figure 4. In this design, instead of storing the path metric for each stage, the decision is taken directly. Following are the components used in the decoder:
3.1 Branch Metric Unit (BMU)
Branch Metric (BM) calculation is the distance between received and estimated output code word. It is also called the Hamming distance, for e.g. if the received code word is 10 then the hamming distance with 00, 01, 10 and 11 will be 01, 10, 00, 01 respectively. This function is done by the BMU.

3.2 Add Compare & Select Unit (ACSU)
Path Metric (PM) calculation is done by ACSU in iterative manner. It is repeated for every encoder state. Previous path metric will be added to the corresponding branch metric, and the output will be sent to the comparator and select unit. Two paths ending in a given state are compared and the greater metric is dropped, whereas the smaller one is selected for further calculation, known as survivor path.

3.3 Path Metric Unit (PMU)
Path Metric Unit takes input from the output of the ACSU and store it for the next clock pulse. It gives input to ACSU for calculation of next PM. For state a, the path metric for time instant n will:

\[
PM(a,n) = \min \{ PM(a,n-1)+BM(00), PM(b,n-1)+BM(11) \} \quad \ldots \ldots \quad (1)
\]

3.4 RAM
Random Access Memory is used in the design, to store the decisions made by the survivor unit.

3.5 Survivor Unit (SU)
Survivor unit takes the path metrics of all states and select the least of the path metrics. A decision will be made by selecting the least of the path metric of all states for particular time instant and it will be stored in RAM.

The design is coded in VHDL, figure 5 shows the block view and figure 6 shows the RTL view generated after successful synthesis of the Viterbi decoder. Simulation results are taken for input code – 11, 10, 10, 00, 01, 11.

![Figure 4. Proposed digital design of Viterbi Decoder for K=3](image-url)
Figure 5. Block View of Viterbi decoder

Figure 6. RTL View of Viterbi decoder
Figure 7. Simulation Results of Viterbi decoder

Figure 8. Data stored in RAM after 7 clock pulses

Figure 9. HDL synthesis report of the Viterbi decoder
Timing Summary:

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Speed Grade: -4

Minimum period: 9.928ns (Maximum Frequency: 100.725MHz)
Minimum input arrival time before clock: 8.936ns
Maximum output required time after clock: 4.283ns
Maximum combinational path delay: 2.731ns

Figure 10. Timing summary of the Viterbi decoder

4. Conclusion & Future Work
The proposed digital design of the Viterbi decoder for ½ rate convolutional encoder of constraint length k = 3 is successfully synthesized in VHDL and simulated using XILINX ISE 14.7. RTL View of the complete design is shown in figure 6, whereas figure 7 and figure 8 shows the simulation results. Instead of storing the path metric of all four states for a single time instant, a decision is made by the survivor unit and reduce the memory requirement for a complete trellis length. The HDL synthesis report and the timing summary is shown in figure 9 and figure 10.

Future work will be implementing the design and evaluation of speed performance and power consumption of the decoder on different FPGA boards.

5. References
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