The trigger readout electronics for the Phase-I upgrade of the ATLAS Liquid Argon calorimeters

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ABSTRACT: For the Phase-I luminosity upgrade of the LHC a higher granularity trigger readout of the ATLAS Liquid Argon (LAr) Calorimeters is foreseen to enhance the trigger feature extraction and background rejection. The new readout system digitizes the detector signals, grouped into 34000 so-called Super Cells, with 12-bit precision at 40 MHz and transfers the data on optical links to the digital processing system, which computes the Super Cell transverse energies. In this paper, development and test results of the new readout system are presented.

KEYWORDS: Trigger concepts and systems (hardware and software); Front-end electronics for detector readout
1 Introduction

The LHC upgrade is planned to enhance the instantaneous luminosity to \(2 - 3 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}\) during Run 3 from 2021 through 2023. The Phase-I upgrade of the trigger readout electronics for the ATLAS Liquid Argon (LAr) Calorimeters (ref. [1]) will be installed on the ATLAS detector (ref. [2]) during the second long shutdown of LHC in 2019/2020. In this upgrade, so-called Super Cells are introduced to provide higher granularity, higher resolution and longitudinal shower shape information from the LAr calorimeters to the Level-1 trigger processors (ref. [3]). The trigger energy resolution and efficiency will be improved for selecting electrons, photons, tau leptons, jets, and missing transverse momentum, while enhancing discrimination against pile-up. The readout of the trigger signals will process 34,000 Super Cells at every LHC bunch-crossing, frequency of 40 MHz, at 12-bit precision.

The improvement of granularity is shown in figure 1, which compares the energy deposition of an electron in the existing trigger readout system to that of the upgraded system. The Super Cells will provide information for each layer of the calorimeter and a finer segmentation in the front and middle layer. The spatial granularity is thus improved by a factor of 10 compared to the existing Level-1 system.

The architecture of the Phase-I trigger readout is shown in figure 2 (ref. [4]). The original functionality of the Front-end Boards (FEBs) (ref. [5]) is preserved so that the standard readout of the LAr Calorimeter cells and the legacy trigger system can be operated as before. New Layer Sum Boards (LSB) and new base planes are upgraded to replace the existing pieces, and new LAr Trigger Digitizer Boards (LTDB) will digitize the Super Cell signals and send processed data to the back-end electronics, where data are transmitted to the trigger processors. Each LTDB will process up to 320 Super Cell signals, which will be digitized by 12-bit ADCs on the LTDB. The output data connection of an LTDB consists of up to 40 optical fibers, each of which carries the data at
Figure 1. Example of an electron with 70 GeV of transverse energy in the existing Level-1 Calorimeter trigger electronics (left) and the upgraded trigger electronics (right). On the left, trigger towers sum the energy deposition across the longitudinal layers of the calorimeters in an area of $\Delta \eta \times \Delta \phi = 0.1 \times 0.1$. On the right, Super Cells provide information for each calorimeter layer for the full $\eta$ range of the calorimeter, and finer segmentation ($\Delta \eta \times \Delta \phi = 0.025 \times 0.1$) in the middle layers of the calorimeter.

Figure 2. The upgraded LAr trigger readout system architecture. The red outlines indicate the new components.

5.12 Gbps through a custom serializer and optical link to back-end LAr Digital Processing System (LDPS), which converts in real-time the samples to calibrated energies and interfaces to the Feature Extractor (FEX) processors. With a total of 124 LTDBs in the system, the total rate to the backend electronics is approximately 25 Tbps.

2 The LAr Phase-I demonstrator

A demonstrator system has been developed in the LHC long shutdown from 2013 to 2015 (ref. [6]). The demonstrator system that is about 1/60 of the full trigger readout consists of two LTDB
demonstrators, two ATCA test boards for Baseline Acquisition (ABBA) that are used as digital processing boards and receive the data from the LTDB demonstrators via optical links. These boards together with two new base planes were installed on ATLAS in summer 2014.

Measurements and data analysis have been done after the installation of the demonstrator system. Test results show that the observed noise level is consistent with noise levels in the current system. The demonstrator system successfully finished the data taking in 2015. These data are used to understand effect of pileup and to develop new filtering algorithm. The preliminary data analysis shows a good agreement for ATLAS main readout and ABBA readout. Now Atlas restarted data collection using the demonstrator with the start of LHC in May 2016.

3 Phase-I front-end electronics

Three key components are being developed to meet the requirements from the LAr Phase-I upgrade. The new LSB produces finer granularity Super Cell signals in the front and middle layers. The new base planes will allocate new slot(s) for the LTDBs, while keeping the other front-end electronics boards slots intact. The LTDB is the key electronics board to be built for the Phase-I upgrade. It will be responsible for the formation of the legacy layer sum signals as well as the digitization of Super Cell signals. Developments of these components are ongoing, and some of the prototypes are being tested. The design of LTDB is described in detail in the following subsections.

3.1 Radiation-tolerant custom ASICs for LTDB

The LAr front-end electronics will run in higher radiation levels in the upgraded LHC (ref [7]). A radiation-tolerant custom 12-bit Nevis ADC (ref. [8]) and a radiation-tolerant custom serializer LOCx2 (ref. [9]) have been developed for LTDB.

The radiation-hard quad-channel 12-bit 40 MS/s pipeline SAR Nevis ADC consists of four pipeline A/D channels with 12-bit resolution each. The sampling information is derived from the rising edge of the differential input SLVS 40 MHz clock. The data are sent out serially using 320 MHz DDR SLVS clock signaling. The ADC consumes around 43 mW per channel. The I2C interface allows for control of all internal functions of the chip. The final prototypes have been produced and tested on 64-ch LTDB prototype.

The LOCx2 consists of two channels, with each channel encoding ADC data with an overhead of 14.3% and transmits serial data at 5.12 Gbps with a latency of less than 27.2 ns. LOCx2 is fabricated with a commercial 0.25-µm Silicon-on-Sapphire CMOS technology. The power consumption of LOCx2 is around 843 mW. The early prototype has been tested on 64-ch LTDB prototype, and the final prototype is being tested.

3.2 LTDB pre-prototype

In order to evaluate technical and performance aspects, a pre-prototype board has been developed with commercial FPGAs, radiation-tolerant custom ASIC Nevis ADCs and MTx (ref. [10]) optical transmitters. As shown in figure 3, the pre-prototype consists of analog section, digital section and power section. The analog section provides the appropriate gain, shaping, offset and common mode. The digital section digitizes the analog signals and sends processed data to back-end electronics. The digital section has 10 Artix-7 FPGA, 80 Nevis ADCs, 20 MTx modules and 2 GBTx for data
processing, clock distribution, slow control and monitoring. The power section is designed as a mezzanine and supplies power to the board.

Evaluation tests of the digital section have been performed, and results show it functions properly. Long term speed tests with IBERT (ref. [11]) of all optical links at 4.8 Gbps yield bit-error-rates that are better than $10^{-15}$ with good eye diagram openings, demonstrating stable operation of the LTDB pre-prototype board.

3.3 64-ch LTDB Prototype

While the custom ASICs are being designed, an LTDB 64-ch test board has been developed to verify the design and to exercise the radiation-tolerant custom ASICs. The board is 1/5 of the LTDB prototype and will process 64 Super Cell signals. As shown in figure 4, there are 16 custom 12-bit Nevis ADCs and 4 custom LOCx2 devices to interface with the ADC. There are also 4 custom MTx dual channel optical transmitters to transmit the data to the LDPB, 1 GBTx, 1 GBT-SCA and 1 MTRx to configure on-board devices, control the power supply and monitor the voltage, current and board temperature.

Figure 5 shows results from performance tests of the 64-ch LTDB prototype. The RMS of the ADC response, which measures the noise in the system, is less than 1 ADC count. The ADC output value as a function of calibration pulse input amplitude is used to measure the dynamic range and the non-linearity of the analog chain upstream of the ADC. The non-linearity is around 0.12%. Crosstalk between a channel and its neighboring channel is also measured. The maximum crosstalk is around 0.1%.

4 Phase-I back-end electronics

The LTDB sends data to back-end electronics the LAr Digital Processing System (LDPS). It receives 12-bits of ADC data from the LTDBs at 5.12 Gbps/fiber, extracts the transverse energy for each
Super Cell every 25 ns, and transmits these data to the Level-1 calorimeter trigger system (L1Calo) at 11.2 Gbps. There’re two key elements in the LDPS: the LAr Trigger prOcessing Mezzanine (LATOME), and the LAr Carrier (LArC).

The LATOME is an AMC mezzanine card, as shown in figure 6. It has one ARRIA-10 FPGA, 8 MicroPods and 2 Gbits DDR3 SDRAM. The FPGA processes received data and sends it out through optical links. The DDR3 SDRAM buffers the data. The LATOME has been fully tested and the board works as expected. It supports various optical link speeds (6.4, 9.6, 11.2 and 12.8 Gbps) for different applications.
The LArC is an ATCA carrier board (ref. [12]), as shown in figure 7. Each LArC holds four LATOMEs and provides a variety of different communication functionalities. It is a challenge to achieve a reliable high rate of transmission for clock distribution and data rates at 10 GbE on large ATCA boards. The integration tests with LATOME have been successfully done. A baseline link speed of 11.2 Gbps has been selected.

5 Conclusion

To improve the Level-1 trigger performance for all the objects involving the LAr calorimeters, a new trigger readout system for the Phase-I upgrade of the ATLAS LAr Calorimeters is being designed. A demonstrator system has been installed on the ATLAS detector. Preliminary data analysis shows a good agreement for ATLAS main readout and demonstrator readout. Based on the demonstrator system, further prototypes for the trigger readout system with radiation-tolerant custom ASICs are being developed and tested. The full integration of the trigger readout system for the Phase-I upgrade of the ATLAS LAr Calorimeters will take place in 2017.

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