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Highly suppressed interface traps of Al$_2$O$_3$/GaN through interposing a stoichiometric Ga$_2$O$_3$ layer

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Al$_2$O$_3$ is a broadly employed dielectric material in GaN high electron mobility transistors. Nevertheless, at the Al$_2$O$_3$/GaN interface, numerous traps induced by nonidealities of the native GaO$_x$ layer on the surface of GaN can lead to threshold voltage instability and other reliability issues. In this study, after removing the native GaO$_x$ layer, a stoichiometric Ga$_2$O$_3$ layer was sandwiched between Al$_2$O$_3$ and GaN. The interfacial state density of Al$_2$O$_3$/GaO$_x$/GaN can be reduced by more than two orders of magnitude to an extremely low level of $2.4 \times 10^{10}$ eV$^{-1}$ cm$^{-2}$ at the energy level of 0.36 eV.© 2022 The Author(s). Published on behalf of The Japan Society of Applied Physics by IOP Publishing Ltd

In recent years, GaN high electron mobility transistors (HEMTs) have garnered extensive interest in power and radio-frequency applications owing to their high mobility, high breakdown field, and chemical stability.1,2) The metal–oxide–semiconductor field-effect transistor is one of the most commonly used structures in GaN HEMTs to suppress the gate leakage current and enlarge the gate voltage swing, the AlGaN/GaN epitaxial wafer typically consists of a thin GaN-cap layer which can further reduce the gate leakage current.3–5) Among typical gate dielectric materials, such as Al$_2$O$_3$,6–7) HfO$_2$,8) and SiO$_2$,8) Al$_2$O$_3$ is one of the most promising candidates because of its high dielectric constant (8–10), large bandgap (7–9 eV),9) sufficiently large conductivity band offset between GaN and Al$_2$O$_3$, and mature deposition technology.5,10)

However, due to the poor quality of the native GaO$_x$, at the surface of GaN, numerous traps and fixed charges are introduced at the Al$_2$O$_3$/GaN interface, deteriorating the reliability and shifting the threshold voltage of GaN HEMTs.11) Previous research on improving the interfacial quality of GaN by controlling the native GaO$_x$ layer can be classified into two kinds of strategies. One is to remove the native GaO$_x$ through chemical cleaning or in situ inductively coupled plasma cleaning before the gate dielectric deposition.5,11) For example, Ando et al. used an optimized mixture of chemical solutions to clean the GaN surface, obtaining a low interfacial state density ($D_{it}$) value of $3 \times 10^{10}$ eV$^{-1}$ cm$^{-2}$ at the Al$_2$O$_3$/GaN interface.9) Yang et al. removed the native GaO$_x$ using NH$_3$-Ar plasma cleaning before the atomic layer deposition (ALD) Al$_2$O$_3$ process, achieving a high-performance GaN HEMTs with a small hysteresis of 0.09 V.11)

The other strategy is to introduce a high-quality Ga$_2$O$_3$ layer using thermal oxidation and laser irradiation.12,13) Nakano et al. achieved a low $D_{it}$ of $5.5 \times 10^{10}$ eV$^{-1}$ cm$^{-2}$ between Ga$_2$O$_3$ and GaN by oxidizing the GaN in the furnace at 880 °C for 5 h.12) Lee et al. oxidized the n-type GaN sample in a chemical solution under He-Cd laser irradiation, a low interface state density of $2.53 \times 10^{11}$ cm$^{-2}$ eV$^{-1}$ was obtained.13)

Although Ga$_2$O$_3$ is a suitable gate dielectric material due to the low $D_{it}$ between Ga$_2$O$_3$ and GaN, the gate breakdown electric field is often limited by the smaller bandgap of Ga$_2$O$_3$ (~4.6 eV) as opposed to other larger bandgap materials, such as Al$_2$O$_3$ (~8 eV). Therefore, Ga$_2$O$_3$ combined with Al$_2$O$_3$ could be a promising gate dielectric for lower $D_{it}$, suppressed gate leakage current, and enhanced gate voltage swing simultaneously. In addition, Ga$_2$O$_3$ was deposited by the pulsed laser deposition (PLD) technique in this work, and PLD can offer higher temperature and vacuum in comparison with ALD and sputtering, which will benefit to reduce the interfacial state density and enhance the device performance.14)

In this letter, after removing the native GaO$_x$, on GaN, we have grown a thin Ga$_2$O$_3$ interlayer by the PLD technique between Al$_2$O$_3$ and GaN to form the Al$_2$O$_3$/Ga$_2$O$_3$/GaN capacitor. The resulting $D_{it}$ was reduced by more than two orders of magnitude to an extremely low level of $2.4 \times 10^{10}$ eV$^{-1}$ cm$^{-2}$ at the energy level of 0.36 eV compared with the Al$_2$O$_3$/GaN capacitor.

Figure 1(a) illustrates the cross-sectional schematic of the Al$_2$O$_3$/Ga$_2$O$_3$/GaN capacitors. The GaN wafers were 4 μm thick Si-doped n-type GaN epilayers grown on c-plane sapphire substrates, and the doping concentration of GaN is $4.3 \times 10^{16}$ cm$^{-3}$ determined with the Hall measurement. The cross-sectional transmission electron microscopy (TEM) image of the Al$_2$O$_3$/Ga$_2$O$_3$/GaN capacitor is shown in Fig. 1(b), the thickness of the amorphous Ga$_2$O$_3$ interlayer is around 3 nm.

The GaN samples were cleaned with acetone, isopropyl alcohol, deionized water, and piranha solution successively to remove organic surface contamination. Then, the cleaned samples were immersed in diluted hydrogen fluoride (HF) for 2.5 min to etch away the native GaO$_x$.15,16) Immediately after the chemical cleaning process, a thin Ga$_2$O$_3$ layer was deposited on a GaN wafer using PLD (Neocera Pioneer 120) with the oxygen pressure of 1 mTorr, laser pulse density of 100 mJ cm$^{-2}$, and laser pulse frequency of 1 Hz at 650 °C. Subsequently, the sample was transferred to an ALD chamber to deposit a 15 nm Al$_2$O$_3$ layer using the trimethylaluminum (TMA) and O$_2$ plasma as precursors. One ALD cycle comprises 0.015 s TMA dose under the pressure of 80 mTorr, followed by 3 s N$_2$ purge, 3 s O$_2$ plasma treatment with the pressure of 15 mTorr and the power of 300 W and then 3 s N$_2$ purge under the pressure of 80 mTorr.

For the reference Al$_2$O$_3$/GaN, after the same solvent cleaning process, 15 nm Al$_2$O$_3$ was deposited on GaN using...
ALD without removing the native GaO\(_x\). The device structure fabrication was accomplished after e-beam evaporation of the Ni/Au (50/100 nm) stack and lift-off procedure. After that, the experimental and reference samples underwent the same post-gate annealing conditions at 500 °C under N\(_2\) atmosphere for 5 min. Further increasing annealing temperature can lead to the diffusion of Ni and Au to the underlying substrate. A Keithley 4200A-SCS parameter analyzer was used for all electrical analyses including the capacitance–voltage (C–V), conductance–voltage (\(G_p/\omega\)-V), and current–voltage (I–V) characteristics. As series resistance can cause a serious error in admittance-based measured methods, C–V and \(G_p/\omega\)-V data were corrected in this study.

The Ga dangling bonds of the native GaO\(_x\) at the surface of GaN are often considered responsible for numerous \(D_{it}\) between the gate dielectric and GaN. XPS was used to evaluate the number of the Ga dangling bonds of the native GaO\(_x\) on the surface of GaN as well as the Ga\(_2\)O\(_3\) grown by PLD technique which were labeled as “GaN” and “Ga\(_2\)O\(_3\) grown by PLD” respectively in Figs. 2(a) and 2(b). The samples were specially prepared for XPS investigations. For the “GaN” sample, it received the solvent pretreatment, XPS was performed immediately after the cleaning process. For the “Ga\(_2\)O\(_3\) grown by PLD” sample, after the solvent and HF cleaning process of the GaN template, a 3 nm thick Ga\(_2\)O\(_3\) layer was deposited on this template, and XPS was also performed immediately. The O 1s, Ga 3d, and C 1s core-level spectra were acquired at a 45° take-off angle, where C 1s peaks at 284.8 eV were used to calibrate the binding energy positions of the Ga 3d and O 1s XPS signals.

As presented in Fig. 2(a), Ga–N and Ga–O bonds positioned at 19.3 and 20.2 eV are superimposed to fit the Ga 3d signals, consistent with previous publications. No obvious peak lower than 18 eV was observed, implying negligible Ga–Ga bonds, the binding energy position of Ga 3d is located at 20.2 eV as shown in Fig. 2(a).

The O 1s core-level spectra in Fig. 2(b) are deconvolved into \(A_{O_A}\) and \(A_{O_B}\) peaks, where the first peak positioned at 532 eV corresponds to hydroxide groups and the second peak at 530.7 eV is associated with the lattice oxygen of the native GaO\(_x\). Compared with the O 1s XPS signal from the native GaO\(_x\) on GaN, the binding energy position of O 1s from the Ga\(_2\)O\(_3\), shifts from 531.6 to 530.8 eV, suggesting the increasing contribution of the lattice oxygen of the entire detected O 1s intensity.

The O to Ga atomic ratio of the native GaO\(_x\) can be estimated based on Eq. (1), where \(A_x\) (\(x = Ga-O, O_B\)) is the area of the corresponding XPS split peak of Ga 3d, and O 1s divided by the specific relative sensitivity factor of the relevant elements:

\[
\frac{r_{O/Ga}}{A_{O_B}} = \frac{A_{O_B}}{A_{Ga-O}}. \tag{1}
\]

The O to Ga atomic ratio is calculated at 0.5:1, which is far from the stoichiometric value of 1.5:1, implying that numerous Ga dangling bonds of the native GaO\(_x\) layer are on the surface of GaN.

Based on the same computational method above, the O to Ga atomic ratio of the Ga\(_2\)O\(_3\) is calculated at 1.4:1, which is close to the stoichiometric 1.5:1 atomic ratio. The
The bidirectional C–V method with the voltage range of −5 to 5 V and the sweeping rate of 0.05 V s$^{-1}$ was adopted to evaluate the $D_{it}$ of the Al$_2$O$_3$/GaN and Al$_2$O$_3$/Ga$_2$O$_3$/GaN capacitors. For both capacitors, the gate voltage was held at −5 V for 5 min before the measurement to release the trapped electrons. After the capacitance reached the maximum value, the gate voltage was held at 5 V for another 5 min to facilitate the trapping process of electrons under the forward electric field. When the voltage swept back from accumulation to the depletion capacitance region, some trapped electrons did not have enough time to escape from the trapped energy levels. Those trapped electrons could induce an electric field in the capacitor and shift the flat-band voltage to the positive direction in the down sweep C–V measurement. As displayed in Fig. 3(a), the hysteresis can be as large as 0.75 V at the gate voltage of 1.5 V for the capacitor without a Ga$_2$O$_3$ interlayer at 1 MHz, whereas the hysteresis can be reduced to 0.05 V at the same gate voltage for the capacitor with a Ga$_2$O$_3$ interlayer. The small hysteresis in Fig. 3(a) implies the lower $D_{it}$ of Al$_2$O$_3$/Ga$_2$O$_3$/GaN compared with the Al$_2$O$_3$/GaN capacitor.

As displayed in Fig. 3(a), the flat-band voltage of the Al$_2$O$_3$/Ga$_2$O$_3$/GaN capacitor is 0.65 V larger than the Al$_2$O$_3$/GaN capacitor in the up sweep measurement, which is advantageous for the achievement of the enhancement-mode GaN HEMTs. As from the abovementioned discussion, the nonidealties of native GaO can lead to numerous Ga dangling bonds at the interfacial region of Al$_2$O$_3$/GaN. If the interfacial defects induce energy levels between the conduction minimum of Al$_2$O$_3$ and GaN, the Fermi level cannot move past these energy levels under either positive or negative gate bias. These states can behave like positive fixed charges. Therefore, the positive shift of the flat-band voltage can also be attributed to the interfacial quality ameliorating where the defect-induced positive charges were suppressed after introducing the high-quality Ga$_2$O$_3$ interlayer. In addition, Fig. 3(a) reveals that the accumulation capacitance of the Al$_2$O$_3$/Ga$_2$O$_3$/GaN capacitor is smaller than that of its counterpart, resulting from the larger gate dielectric thickness after inserting the Ga$_2$O$_3$ interlayer. Assuming $\varepsilon_{Ga2O3} \approx 10$, the Ga$_2$O$_3$ interlayer thickness is estimated to be 2.88 nm with the C–V measurement which is close the value observed in the TEM image.

As presented in Figs. 3(b) and 3(c), the frequency-dependent C–V measurement with a frequency ranging from 1 kHz to 1 MHz was conducted to further analyze the interface trap properties. The voltage dispersion can be as large as 1.3 V when the frequency increases from 1 kHz to 1 MHz with the Al$_2$O$_3$/GaN capacitor; thus, numerous interfacial traps are present at the Al$_2$O$_3$/GaN interface. In contrast, in Fig. 3(c), a negligible dispersion exists in the weak accumulation region of the Al$_2$O$_3$/Ga$_2$O$_3$/GaN capacitor, and the small frequency dispersion in the strong accumulation region can be attributed to the shunt and series resistance of the capacitor. Therefore, the Ga$_2$O$_3$ interlayer effectively suppressed the frequency dispersion by reducing the Ga dangling bonds induced interfacial traps between Al$_2$O$_3$ and GaN. The conductance method based on the equivalent circuit model was further deployed to quantitatively analyze the interfacial defects of the Al$_2$O$_3$/GaN and Al$_2$O$_3$/Ga$_2$O$_3$/GaN capacitors.

Six gate voltages were biased around the flat-band voltage in the above C–V curves to probe $D_{it}$ using the conductance method so that the Fermi level can only move within the bandgap of GaN under these gate voltages. For a given gate voltage bias, the frequency of the ac anode signal increased from 1 kHz to 1 MHz gradually, and 28 frequency data points were acquired in one measurement. The $G/\omega$ curve can be acquired from Eq. (2), where $\omega$ is the radio frequency of the ac anode signal, $C_{Al2O3}$ is the capacitance in the strong accumulation region of the C–V curves, and $G_m$ and $C_m$ are the measured conductance and capacitance, respectively:

$$\frac{G_p}{\omega} = \frac{\omega G_m}{G_m^2 + \omega^2 (C_{Al2O3} - C_m)^2},$$

$$\frac{G_p}{\omega} = \frac{q \omega \tau_T D_{it}}{1 + (\omega \tau)^2}.$$  

The parallel conductance as a function of the radio frequency is given by Eq. (3), where $\tau_T$ denotes the time constant of the trapped electrons, and $D_{it}$ is the interfacial state density. By fitting the $G/\omega$ versus the $\omega$ curve, $\tau_T$ and $D_{it}$ can be obtained.

As presented in Figs. 4(a) and 4(b), the peak value of the $G/\omega$ curve is much larger for the Al$_2$O$_3$/GaN compared with the Al$_2$O$_3$/Ga$_2$O$_3$/GaN capacitor, an indication of the lower $D_{it}$ of the Al$_2$O$_3$/Ga$_2$O$_3$/GaN capacitor.

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**Fig. 3.** (Color online) (a) C–V hysteresis characteristics of Al$_2$O$_3$/GaN and Al$_2$O$_3$/Ga$_2$O$_3$/GaN capacitors. C–V frequency dispersion characteristics of (b) Al$_2$O$_3$/GaN and (c) Al$_2$O$_3$/Ga$_2$O$_3$/GaN capacitors.
From the derived time constant, the trapped energy levels can be calculated from the Shockley–Read–Hall statistics, as presented in Eq. (4), where $\sigma_T$ is the captured cross section of the interface traps, $N_C$ denotes the density of the states in the GaN conduction band, and $v_T$ represents the average thermal velocity of the electrons in the GaN thin film:

$$\tau_T = (\sigma_T N_C v_T)^{-1} \exp \left( \frac{E_C - E_F}{kT} \right).$$  \hspace{1cm} (4)

Assuming $T = 300$ K, $\nu_T = 2.6 \times 10^7$ cm$^{-1}$, $\sigma_T = 3.4 \times 10^{-15}$ cm$^2$, and $N_C = 2.7 \times 10^{18}$ cm$^{-3}$, $D_n$ can be obtained as a function of the energy levels ($E_C$ to $E_C$).

Figure 4(c) reveals the $D_n$ distribution as a function of the energy levels from the minimum of the conduction band of GaN for the two capacitors with and without a Ga$_2$O$_3$ interlayer. For the Al$_2$O$_3$/GaN capacitor, the high $D_n$ of $9.0 \times 10^{12}$ cm$^{-2}$ eV$^{-1}$ is detected at the energy level of 0.36 eV. In comparison, a significantly lower $D_n$ of $2.4 \times 10^{10}$ cm$^{-2}$ eV$^{-1}$ is achieved at the same energy levels after introducing the Ga$_2$O$_3$ interlayer. Overall, the $D_n$ can be reduced by more than two orders of magnitude in the detected energy levels. As discussed before, compared with the native GaO$_x$, the O to Ga atomic ratio of Ga$_2$O$_3$ is much closer to the stoichiometric value. Therefore, the significantly suppressed $D_n$ can be attributed to the reduced Ga dangling bonds after removing the native GaO$_x$ and sandwiching the Ga$_2$O$_3$ interlayer. From Fig. 4(c), the densities of deep level traps are higher than those of the shallow level traps in the Al$_2$O$_3$/Ga$_2$O$_3$/GaN capacitor. In contrast, the densities of interfacial traps decrease with the increasing energy levels in the Al$_2$O$_3$/GaN capacitor, implying that different interfacial trap types exist after introducing the Ga$_2$O$_3$ interlayer. In the disorder-induced gap state mode, $D_n$ distribution has a U-shaped characteristic, i.e., $D_n$ has a minimum value at charge neutrality level $E_{CNL}$ and increases as it moves away from $E_{CNL}$ to the edges of conduction band $E_C$ and valence band $E_V$. However, only part of the interface states can be detected with the conductance method as many trapped electrons are in “frozen states” at room temperature which cannot respond to the gate voltage bias. Therefore, $D_n$ shows derivation from the U-shaped distribution which is a commonly observed result.

In conclusion, a stoichiometric Ga$_2$O$_3$ layer was interposed between Al$_2$O$_3$ and GaN by the PLD technique. Compared with the native GaO$_x$ on the surface of GaN, a negligible number of Ga dangling bonds were detected using the XPS measurement with Ga$_2$O$_3$. Electrical measurement demonstrated that improved interface quality with the Al$_2$O$_3$/Ga$_2$O$_3$/GaN capacitor, with two orders of magnitude reduced $D_n$ and a positive flat-band voltage shift of 0.65 V compared with the Al$_2$O$_3$/GaN capacitor. These results indicate that the Al$_2$O$_3$/Ga$_2$O$_3$ bilayer is a promising candidate for a gate dielectric material in GaN HEMTs.

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1) D. Kuchta, D. Gryglewski, and W. Wojtasik, Micromachines 11, 398 (2020).
2) J. Wei, G. Tang, R. Xie, and K. J. Chen, J. Appl. Phys. 59, (SO/SG0801) (2020).
3) J. Kotani, J. Yaita, A. Yamada, N. Nakamura, and K. Watanabe, J. Appl. Phys. 127, 234501 (2020).
4) E. J. Miller, A. Z. Dang, and E. T. Yu, J. Appl. Phys. 88, 5951 (2000).
5) D. Biswas, C. Joshi, J. Biswas, K. Thakar, S. Rajan, and S. Lodha, Appl. Phys. Lett. 114, 212106 (2019).
6) Y. Ando, K. Nagamatsu, M. Doki, N. Taoka, A. Tanaka, S. Nitta, Y. Honda, T. Nakamura, and H. Amano, Appl. Phys. Lett. 117, 102102 (2020).
7) C. Liu, E. F. Chor, and L. Seow, J. Semicond. Sci. Technol. 22, 522 (2007).
8) E. A. Alam et al., J. Appl. Phys. 109, 084511 (2011).
9) E. Miyazaki, Y. Goda, S. Kishimoto, and T. Mizutani, J. Solid-State Electron. 62, 152 (2011).
10) Z. Liu, G. Ng, S. Arulkumaran, Y. Muang, and H. Zhou, Appl. Phys. Lett. 98, 163501 (2011).
11) S. Yang, Z. Tang, K. Y. Wong, Y. S. Lin, C. Liu, Y. Lu, S. Huang, and K. J. Chen, IEEE Electron Device Lett. 34, 1497 (2013).
12) Y. Nakano and T. Jimbo, J. Appl. Phys. Lett. 82, 218 (2003).
13) C. T. Lee, H. W. Chen, and Y. H. Lee, Appl. Phys. Lett. 82, 4304 (2003).
14) D. H. Lowndes, D. B. Gavagian, A. A. Pyretuzky, D. P. Norton, and C. M. Rodolus, Science 273, 898 (1996).
15) K. Yuge, T. Nabatame, Y. Irokawa, A. Oh, N. Ikeda, L. Sang, Y. Koiside, and T. Ohishi, J. Semicond. Sci. Technol. 34, 034001 (2019).
16) S. G. Rosenberg, D. J. Pennachio, C. Wagenbach, S. D. Johnson, N. Nepal, A. C. Kozen, J. M. Woodward, Z. Robinson, H. Jorres, and K. F. Ludwig, J. Vac. Sci. Technol. A: Vac. Surf. Films 37, 020908 (2019).
17) S. G. Rosenberg, D. J. Pennachio, C. Wagenbach, S. D. Johnson, N. Nepal, A. C. Kozen, J. M. Woodward, Z. Robinson, H. Jorres, and K. F. Ludwig, J. Vac. Sci. Technol. A: Vac. Surf. Films, 37, 020908 (2019).
18) S. Yang, S. Liu, Y. Lu, C. Liu, and K. J. Chen, IEEE Trans. Electron Devices 62, 1870 (2015).
19) G. V. Benemanskaya, M. N. Lapushkin, and S. N. Timoshnev, J. Surf. Sci. 603, 2474 (2009).
20) J. T. Asubar, Z. Yatabe, D. Gregusova, and T. Hashizume, J. Appl. Phys. 129, 121102 (2021).
21) R. Huang, T. Liu, Y. Zhao, Y. Zhu, Z. Huang, F. Li, J. Liu, L. Zhang, S. Zhang, and A. Sun, Appl. Surf. Sci. 440, 637 (2018).
22) B. Feng, T. He, G. He, X. Zhang, Y. Wu, X. Chen, Z. Li, X. Zhang, Z. Jia, and G. Niu, Appl. Phys. Lett. 118, 181602 (2021).
23) J. He, Y. Zhong, Y. Zhou, X. Guo, Y. Huang, J. Liu, M. Feng, Q. Sun, M. Ikeda, and H. Yang, Appl. Phys. Express 12, 055507 (2019).
24) H. S. Wang, H. Q. Zhang, J. Liu, D. Y. Xue, H. W. Liang, and X. C. Xia, J. Electron. Mater. 48, 2430 (2019).
25) V. Naumann, M. Otto, R. B. Wehrspohn, and C. Hagendorf, J. Vac. Sci. Surf. Technol. A: Vac. Films. 30, 04D106 (2012).
26) S. Liu, S. Yang, Z. Tang, Q. Jiang, C. Liu, M. Wang, B. Shen, and K. J. Chen, Appl. Phys. Lett. 106, 051605 (2015).
27) M. Esposto, S. Krishnamoorthy, D. N. Nath, S. Bajaj, T.-H. Hung, and S. Rajan, Appl. Phys. Lett. 99, 133503 (2011).
28) K. Yang and C. Hu, IEEE Trans. Electron Devices 46, 1500 (1999).
29) X. Ma, J. Zhu, X. Liao, T. Yue, W. Chen, and Y. Hao, Appl. Phys. Lett. 103, 033510 (2013).
30) Y. Hori, Z. Yatabe, and T. Hashizume, J. Appl. Phys. 114, 244503 (2013).
31) C. Mizue, Y. Hori, M. Miczek, and T. Hashizume, Jpn. J. Appl. Phys. 50, 021001 (2011).