A novel receiver design for energy packet-based dispatching

Friedrich Wiegel*, Edoardo De Din, Antonello Monti, Klaus Wehrle, Marc Hiller, Martina Zitterbart, Veit Hagenmeyer

F. Wiegel, Prof. M. Hiller, Prof. M. Zitterbart, Prof. V. Hagenmeyer
Karlsruhe Institute of Technology
76131 Karlsruhe, Germany
Email Address: friedrich.wiegel@kit.edu

E. De Din, Prof. A. Monti, Prof. K. Wehrle
RWTH Aachen University
52062 Aachen, Germany

Keywords: packet-based energy dispatching, power signal dual modulation, phase locked loop

A steadily growing share of renewable energies with fluctuating and decentralized generation as well as rising peak loads require novel solutions to ensure the reliability of electricity supply. More specifically, grid stability is endangered by equally relevant line constraints and battery capacity limits. In this light, energy packet-based dispatching with power signal dual modulation has recently been introduced as an innovative solution. However, this approach assumes a central synchronicity provision unit for energy packet dispatching. In order to overcome this assumption, the present paper’s main contribution is a design of an energy packet receiver which recovers the required synchronicity information directly from the received signal itself. Key implementation aspects are discussed in detail. By means of a DC grid example, simulation results show the performance and applicability of the proposed novel receiver for packet-based energy dispatching.

1 Introduction

Today’s electricity grid is based on the equilibrium principle, i.e. the amount of power generated corresponds to the power consumed at every instant of time. Due to the steadily growing number of renewable energies with fluctuating and decentralized generation as well as increasing peak loads due to the rising use of electric vehicles and heat pumps in the context of the energy transition, it is increasingly challenging to guarantee this instantaneous balance while considering local constraints. Demand Response (DR), Demand Side Management (DSM) and Energy Management Systems (EMS) can be considered as potential solutions to this challenge, at least in the short term [1] [2] [3]. Unfortunately, the possibilities for load shifting in today’s power grids are limited due to equally relevant line constraints and battery capacity limits. For a long-term solution, it is therefore necessary to consider completely new concepts, which operate without overall synchronicity between generation and consumption.

A packet-based energy distribution concept, as presented e.g. in [4] and [5], can be one of such long-term solutions. According to the number of recent publications e.g. [6], [7] and [8], such a packet-based energy distribution approach is highly topical and widely accepted. Inspired by the Internet protocol (IP) known from modern communication technologies, an asynchronous energy distribution is a promising option to solve the problem described above and to make the entire power distribution network future-proof. Equivalent to the data packet from the Internet protocol, an energy packet (EP) is defined as the key element in this concept. An energy packet itself is a defined amount of energy that is exchanged within the distribution network between source and sink asynchronously according to demand or availability. In combination with energy storage elements, this approach enables energy transmission based on the store-and-forward principle known from the IP protocol. The two characteristics of this concept, namely the energy packet definition and the store-and-forward principle, result in two major advantages which contribute significantly to the improvement of the energy supply infrastructure: (i) creating a clear decoupling between demand and generation; (ii) always allowing the best use of the infrastructure capacity, i.e. line limits and storage capacity.

While in [4] the vision and the underlying theoretical considerations are presented in detail, in [5] a possible solution for the realization of energy packets and their transmission via a direct current (DC)
grid is presented. Thereby, for successful transmission of energy packets, synchronicity on the data level is assumed.

The present contribution significantly extends [5] by designing the solution of a practicable receiver for energy packets. The synchronization necessary for the detection of the information part of the energy packet is derived from the received packet itself. This means that the previous central synchronization prerequisite is no longer necessary and the energy packets can therefore be exchanged asynchronously over the distribution network, as demonstrated by the simulation results in section 5.

This paper is organized as follows: Section 2 introduces the concept of packet-based energy distribution and outlines the basic idea of power signal dual modulation (PSDM) for packet-based energy distribution. Furthermore, the advantages and disadvantages of related solutions are discussed. In section 3, the basic idea of a PSDM transmitter is outlined. Section 4 describes in detail which steps have to be taken in the communication part of the PSDM receiver in order to transmit energy packets without global synchronicity and how the required point-to-point synchronization between the participants can be achieved from the received signal. In section 5, the simulation results are summarized. Finally, the main conclusions and an outlook are provided in section 6.

2 Packet-based energy distribution in DC networks

2.1 Concept

Figure 1 visualizes the concept of packet-based energy distribution in a simplified form. Each participant of this simple energy distribution network is connected to a DC bus either via DC/DC (see G1, L1 and L3) or DC/AC converters (see L2). The generator G1 supplies the DC bus with a constant DC voltage $V_{G1}$. Communication paths are represented by transceiver blocks Tx/Rx. All loads are in standby at initial time $t_0$, i.e., the respective input impedance of the converters is very high and no current flows. At time $t_1$, an energy packet is transmitted to the load L3. For this purpose, the load L3 is informed via a communication path that it should switch to the current consumption mode for the duration $T_{L3}$. For the duration $T_{L3}$ a current $I_{L3}$ flows. This process could be interpreted as an energy packet transmission procedure:

$$EP_{L3} = v(t)_{G1} \cdot i(t)_{L3} \cdot t_{L3}$$

Obviously, the same principles apply to the transmission of $EP_{L2}$ at $t_2$ and $EP_{L1}$ at $t_3$. Taking the concept shown in Figure 1 as a basis, it becomes clear that an energy packet is a combination of the energy
2.2 Energy packets metadata providing strategies

The information path for the control of the energy packet transmission mentioned above can be realized in various ways. The use of industrial or conventional wired communication technologies such as EtherCAT or IEEE 802.3(xx) is conceivable. However, this approach results in significant additional installation and cost effort and is therefore not practical in every section of an energy distribution network.

Wireless low-rate communication technologies such as IEEE 802.15.4, Z-Wave or EnOcean for low-rate wireless personal area networks (LR-WPAN) could be a possible solution for dedicated power distribution network subsections such as a house, an industrial building or an industrial plant [9] [10] [11]. These are known among others from several applications in the field of Smart Homes and Home Automation and are becoming more and more popular. These communication technologies provide sufficient high bandwidths for the applications mentioned, have low production costs and enable the plug-and-play expansion of the communication network without installing additional cables.

As described in [12], all these low-cost and low-power radio communication standards unfortunately also have some critical disadvantages that make the use of these techniques problematic in the context of energy packet transmission. Due to the very low transmission power defined by the respective standards and the cost-effective design of the transceivers, the established network is very sensitive to any kind of interference and multipath influences, which are always present in buildings and industrial plants [13]. Therefore, a network created by these communication techniques is called a Lossy Network, i.e. a high number of lost information packets is expected by definition. This is also reflected in the name of the Routing Protocol for low power and lossy Networks (RPL) [14]. Due to the desired high degree of reliability of the power distribution network, lossy networks are not appropriate in this case. In addition, the coverage of such networks is relatively small [13] [15]. Moreover, building topologies such as steel concrete ceilings or electromagnetic shielding are challenging since they can lead to non-accessibility of net-elements by radio. Especially many large loads or generators are installed in rooms with electromagnetic shielding walls. Even in industrial plants, large loads or generators are often not easily accessible by radio.

However, in most cases a power outlet is within reach. Since all participants of the power distribution network have to be connected to the powerline, powerline communication (PLC) is a natural choice for the transmission of the control data at least within certain subsections with a limited extension and a relatively manageable number of participants.

The Powerline communication techniques themselves can be divided in two groups: Broad Band - Powerline Communication (BB-PLC) and Narrow Band - Powerline Communication (NB-PLC). In Europe, BB-PLC communications technology operates in a frequency band between 1.6 MHz and 30 MHz and can provide data rates of several gigabit per second (Gbps) [16]. However, since these data rates can only be achieved under optimal conditions and are not necessary for the transmission of energy packets, and the BB-PLC transceivers are significantly more expensive in production than NB-PLC transceivers, the use of this technology is not considered. In contrast to BB-PLC, NB-PLC technology operates in a frequency band between 3 kHz and 500 kHz and provides data rates of up to one megabit per second, depending on the communication standard and frequency band. The coverage radius is between hundred meters and several kilometers, depending on the standard used [16] [17]. Therefore, NB-PLC is definitely a promising technique in the context of grid element control and smart grid applications, as demonstrated in several studies [18] [19] [20]. Unfortunately, the European Committee for Electrotechnical Standardization (CENELEC) comparatively limits the permissible frequencies and transmission powers for NB-PLCs in

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1 Note that the power part of the energy packet transceiver does not necessarily have to be implemented as a DC system. AC systems with fixed or variable frequency are also conceivable. The only requirement is an inverter suitable for the application needs. The exemplary specification on a DC bus presented in the following is only due to the coherence to the previous publications.
Europe to a very high degree, thus immensely limiting the achievable transmission rates. The European standard (EN) defines the in-band and out-of-band emission limits and states that the CENELEC A band (3-95 kHz) is reserved for energy suppliers and that only the CENELEC B-D bands (95-148.5 kHz) may be used by consumer installations \[21\]. Due to these restrictions, conventional NB-PLC technology operates in Europe exactly within a frequency band where the power electronics required for generating the energy packets have the maximum disturbance emission, and consequently, communication is vulnerable to the switching frequency noise.

### 2.3 Power Signal Dual Modulation based Powerline Communication for Energy Packet distribution

To overcome this problem, powerline communication based on Power-Signal-Dual-Modulation (PSDM) was proposed in the articles \[22\], \[23\], \[24\] and \[5\]. With PSDM, the information signal is embedded into the power signal by manipulating the pulse width modulation signal of the power converter. Either the phase or the frequency of the PWM signal can be manipulated to inject the information. In this way, both data modulation and power conversion are implemented in a single electronic circuit and no explicit analog front ends or coupling units are required like in conventional PLC transmitters. This simplifies the system structure and minimizes implementation costs.

The paper \[5\], on which the present contribution is based on, describes exactly how energy packets can be generated and transmitted using PSDM technology. However, the paper does not answer how the synchronization required for processing the information part of an energy packet can be achieved. Other publications dealing with PSDM also do not give a satisfactory answer to the problem of synchronization in the receiver. For example, the theoretical demodulation process of a DBPSK is described in the \[25\] and it is also pointed out that the symbol clock is crucial for the demodulation of the data, but at the same time it is written: “Still, bit-synchronization is required, which can be easily achieved by program”. However, as described in section 4, bit-synchronization or more precisely symbol-clock recovery is not an easy procedure at all, and is essential for processing and interpreting the received information. In \[23\] a PSK/DSSS modulated signal with suppressed carrier is coherently demodulated. The authors noted that accurate information about the frequency and phase of the carrier is necessary to demodulate the data. To obtain this information, they propose to transform the received PSK/DSSS signal simply into the frequency domain without any pre-operation. However, a non-linear operation has to be applied to a suppressed carrier information signal first to obtain a clear spectral line of the carrier, as can be found in \[26\] or \[27\].

Furthermore, another essential component of a receiving unit, the Adaptive Gain Control, has been completely disregarded in all cited articles, whereby in all of them the interpretation of the data depends on a normalized level.

Hence, the present contribution discusses possible solutions for synchronization and level stabilization in the information path in the context of packet-based energy distribution based on PSDM.

### 3 PSDM Transmitter for Energy Packet generation

To provide an input signal for the implemented receiver, a power signal dual modulation based generator for energy packets as proposed in \[5\] is realized. Figure 2 shows the structure of this generator. As the name implies, the generator performs two tasks: First, it acts as a buck converter, which supplies the DC bus with a constant DC voltage and the energy during the energy packet transmission phase. At the same time, it also acts as an analog part of a powerline transmitter by injecting the information signal into the power line without additional circuits such as an analog front end or coupler. In the following simulation, the output signal of this generator serves as input signal for the realized receiver.

As shown in Figure 2, the information signal is embedded into the power signal by manipulating the duty cycle of the PWM signal used to control the power transistors. The theoretical basics of this procedure are explained in detail in \[5\] or \[23\].
The transmitter responsible for generating the modulated PWM carrier is based on the Direct Sequence Spread Spectrum (DSSS) technology. For this purpose, the data to be transmitted are first DBPSK-coded, then spreaded with an orthogonal pseudo-random sequence based on the Walsh-Hadamard matrix and finally modulated onto the PWM carrier. The use of DSSS transmission technology makes it possible to secure the data connection against the pulse interference and multi-path propagation strongly represented within the power line and thus to design the control path reliably [28] [29]. It also ensures a certain level of security, since only the load that knows the corresponding despreading sequence can decode the data.

4 Receiver for the information part of Energy Packets

Figure 3 shows the implemented powerline communication receiver. In principle, every receiver and also the implemented powerline communication receiver is a transmitter backwards that contains some additional elements, especially several indispensable synchronization units. These are necessary because the receiver generally has no precise information about the symbol, i.e. chip clock, frequency and phase of the carrier and the start point of the data packet. Furthermore, the receiver has to derive this information from the received signal itself. In addition, the clock elements in both the transmitter and receiver have a certain temperature drift, manufacturing tolerances, ageing phenomena, which cause a variable time offset [30].

The resulting time errors have an influence on the signal level within the digital signal processing and can significantly influence the reception quality or even make data transmission impossible [27]. Therefore, the receiver has to perform at least the following synchronization tasks for a successful data transfer [27] [31] [26]:

- Carrier synchronization
- Timing recovery
- Frame synchronization

In general, two additional synchronization stages are required for direct spread spectrum systems:

- Code acquisition
- Code tracking

However, these are only indispensable if one has to deal with strong frequency-selective interference or if one wants to implement a system with code multiplexing media access. However, since we primarily use
spread spectrum technique to assign the messages to the respective load and our intention is to show that the synchronization approaches presented afterwards can also be used for power/signal dual modulation, we can skip with these two synchronization stages in the first step. This is possible because a DBPSK/DSSS signal can be treated for synchronization purposes as a pure DBPSK signal with a data rate increased by the spreading factor. Furthermore, the synchronization approaches described in the following are so generically implemented that they can be modified to a strict DSSS solution with a manageable effort. Among the required adjustments are the replacement of the Timing-Error Detector (TED) by a code phase error detector, the addition of a code acquisition unit and the calculation of the carrier phase error using the despread symbols and not the baseband signal. Thus, the solutions shown in this paper can be considered as the basis for further synchronization steps.

Next, the realized synchronization levels 4.1. Adaptive Gain Control - 4.5. Frame Synchronisation are explained in detail. The corresponding simulation results follow in Section 5. The description of the general elements of the receiver, such as matched filter, demodulation unit, etc., which form the counterpart to the transmitter, is omitted, but reference is made to further literature where these elements are described in detail [20] [27] [32].

### 4.1 Adaptive Gain Control

Phase Locked Loop (PLL) based synchronization algorithms require a constant average signal energy, since this influences the $K_p$ factor of the Phase Error Detector or Timing Error Detector [32]. The level of the threshold value for frame synchronization also depends on the average signal energy of the incoming signal [33]. Thus, a constant signal level is a critical parameter for the realization of a digital transmission system. This is ensured by the Adaptive Gain Control (AGC) unit.

As shown in Figure 3, the signal level correction via AGC takes place in the baseband, i.e. after the down-conversion of the input signal, but before any synchronization. At this point the signal can be described by:

$$u(k) = A(k) \cdot e^{j\varphi_r(k)}$$ \hspace{1cm} (2)

where $u(k)$ represents the input signal, $A(k)$ the amplitude of the symbol and $\varphi_r(k)$ the phase of received symbols. Due to the variable distance between the transmitter and receiver, the used transmission power as well as different attenuation influences within the channel, the amplitude $A(k)$ of the signal is variable and even time-variant. In order to compensate this variance and to adjust the signal level to the reference level, the AGC unit is used. Following difference equations describe the implemented Least Mean Squares (LMS) signal level adaptation algorithm:
4.2 Carrier synchronization

\[ x(k + 1) = x(k) \cdot (1 - \alpha |u(k)|) + \alpha R \] (3)

\[ y(k) = x(k) \cdot u(k) \] (4)

where

- \( u(k) \) represents the complex input signal
- \( R \) represents the reference signal level
- \( \alpha \) represents the step size
- \( x(k) \) represents the divide by factor
- \( y(k) \) represents the output signal of the AGC

To ensure a constant signal level, the magnitude of the AGC output signal \( y \) is compared with a reference signal level \( R \). If the output signal level is too high (low), a negative (positive) signal is fed back, reducing (increasing) the gain. The control parameter \( \alpha \) regulates the amplitude of the feedback signal and is used to control the AGC’s time constant.

Corresponding to Eqn. (3) the calculation of the absolute value of the complex input signal \( |u(k)| \) for determining the amplitude of the input signal is a non-linear process, so the resulting equation is also non-linear. However, based on the assumption that the system is driven by a step \( u(k) = c_k \) with \( c_k > 0 \), the non-linear equation becomes a linear difference equation:

\[ x(k + 1) = x(k) \cdot (1 - \alpha c) + \alpha R \] (5)

From this solution follows that in steady state the gain is \( x(k) = \frac{R}{c} \) and the system time constant is \( \tau = \frac{1}{\alpha c} \).

4.2 Carrier synchronization

A phase deviation of the local oscillator of the down-converter from the carrier wave regardless of whether time-variant or not causes an offset (if time-invariant) or rotation (if time-variant) of the received symbols in the symbol domain \[31\]. Figure 4 shows an example of such a time-variant deviation of the received symbols (blue) from the expected symbols (red). At the shown snapshot the phase shift of the symbols is approx. 45°. If the offset is large enough - in the case of the BPSK more as ±90° - a wrong symbol will be detected.

![Figure 4: Deviation of the symbols from the nominal value when there is a phase offset between the local oscillator and the carrier wave](image)

The task of carrier synchronization is to keep this phase offset as low as possible. In principle, carrier synchronization is a process of tracking the frequency or phase of the local oscillator to the frequency and
phase of the carrier wave. This can be undertaken in different ways [27] [31] [32]. To avoid the need for additional frequency offset estimation and to keep the complexity of the receiver as low as possible, a PLL-based decision-feedback carrier synchronizer is implemented. This has the advantage that it can correct both phase and frequency offset at least within a limited range. As shown in Figure 5, the implemented carrier synchronization unit consists of a carrier phase error detector (PED), a loop filter \( F(z) \), a phase error accumulator as well as a phase rotator.

The carrier phase error detector determines the phase error between the carrier wave and the local oscillator. The loop filter removes the unwanted high-frequency signal components and generates the corresponding control signal for the phase error accumulator. The phase error accumulator is responsible for determining an accumulating phase error. The phase rotator eliminates the estimated phase error.

Since the functionality of the used Proportional–Integral loop filter and phase error accumulator is known from discrete PLLs, only the principle of the used carrier synchronization and the functionality of the implemented carrier phase error detector are presented in the following. For the general functionality of the loop filter and phase error accumulator please refer to the further literature [32] [34].

The received signal can be described by:

\[
    r(t) = G_a \sum_k \{i(k)p(t - kT_s) \cdot \cos(\omega_0t + \phi_e)\} + w(t) \tag{6}
\]

where the representations are

- \( G_a \) gains and losses of the signal
- \( i(k) \) k-th chip
- \( p(t) \) unity-energy pulse shape
- \( \phi_e \) unknown combined phase offset
- \( T_s \) sample period
- \( \omega_0t \) angular frequency of carrier wave
- \( w(t) \) addative white Gaussian noise

Without loss of generality and for simplicity, only the part of the overall function that is relevant for carrier synchronization is used in the following:

\[
    r(k) = i(k) \cdot \cos(\Omega_0k + \phi_e) \tag{7}
\]

The combined phase shift \( \phi_e = \Delta \omega t + \Delta \phi \) consists of a possible frequency shift \( \Delta \omega \) and a constant phase shift \( \Delta \phi \) between the carrier wave and the local oscillator. To eliminate \( \phi_e \), an asynchronous shift of the passband signal into the baseband is first performed by means of the down-converter using a complex signal \( s(k) = 2e^{-j\Omega_0k} \), cf. Figure 3:

\[
    r_{bb}(k) = r(k) \cdot s(k) = i(k) \cdot \cos(\Omega_0k + \phi_r) \cdot 2e^{-j\Omega_0k} \tag{8}
\]

The double-frequency components resulting from the multiplication are then eliminated by the matched filter and the following relation is obtained:

\[
    x(k) = i(k) \cdot e^{-j\phi_r} = |i(k)|e^{j\phi_d} \cdot e^{-j\phi_e} \tag{9}
\]
This means that the symbols $x(k)$ of a signal mixed down asynchronously are shifted in the symbol domain by phase offset $\phi_e$ from the nominal position $\phi_d$ of the symbols as shown in Figure 4. The phase error increment that occurs during a single chip interval is calculated in the implemented Phase Error Detector as follows:

Angle of the received symbol:

$$\phi_r = \tan^{-1} \frac{\text{Im}(y(k))}{\text{Re}(y(k))}$$ (10)

Angle of the nearest possible symbol:

$$\phi_d = \tan^{-1} \frac{\text{Im}(y_d(k))}{\text{Re}(y_d(k))}$$
$$= \tan^{-1} \frac{0}{\text{Re}(y_d(k))}$$
$$= \tan^{-1} \frac{0}{|i(k)| \cdot \text{sgn} \left[ \text{Re}(y_r(k)) \right]}$$ (11)

Resulting phase error:

$$e(k) = \phi_r - \phi_d = \tan^{-1} \frac{\text{Im}(y(k))}{\text{Re}(y(k))} - \tan^{-1} \frac{0}{|i(k)| \cdot \text{sgn} \left[ \text{Re}(y_r(k)) \right]}$$ (12)

The resulting correction phase is then formed using the phase error accumulator by integrating the phase error; subsequently the phase rotator eliminates the offset. Figure 6 shows the S-Curve of the Phase Error Detector. Observe that the S-Curve has two stable locking points at $\phi_e = 0$ and $\phi_e = \pm \pi$. Therefore, a phase ambiguity of $\pi$ exists. This disadvantage is eliminated by difference coding in the transmitter. As mentioned in section 3.

![Figure 6: S-Curve phase error detector](image)

### 4.3 Timing recovery

The output of the matched filter must be sampled periodically at the corresponding chip rate $f_c$ at time $t_k = kT_c + \tau$, where $T_c$ describes the chip period and $\tau$ the time delay due to the signal propagation between the transmitter and the receiver. Since $\tau$ is generally unknown and $T_c$ in the transmitter and receiver are not completely identical, e.g. due to production tolerances of the clocking elements or thermal variance [30], the optimum sampling point is generally unknown. Not sampling the output of the matched filter at this optimum sampling point $t_k$ and with the locally generated asynchronous sampling frequency $\tilde{f}_c$ results

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2 A chip is a single elementary modulation state within the Direct Sequence Spread Spectrum. The sequence of different chips is determined by both the spreading code and the transmitted symbols. The chip rate of the spreading code is typically higher than the symbol rate. The ratio between chip rate and symbol rate is called spreading factor SF and is defined as: $\text{SF} = \frac{f_c}{f_s} \gg 1$. 

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in periodic degradation of the signal level, leading either to a wrong symbol decision or to temporary full signal loss \cite{27} \cite{31}, cf. Figure 16 in Section 5.

The task of the Clock Recovery Unit is to find this optimal sampling point, i.e. to synchronize the receiver with the received signal. Note that since both the installation of a separate clock line between all devices and the reduction of the available signal power (respectively transmission bandwidth) in favor of an explicit clock signal are not viable options, the symbol clock must be derived from the received data. This can be executed both in the time-continuous domain and in the time-discrete domain \cite{32}. In the presented article, a time-discrete solution first introduced by Lars Erup and Floyd M. Gardner is implemented \cite{35} \cite{36}. Figure 7 shows the block diagram of the implemented clock synchronization unit. This consists of a 3rd order Fractional Delay Filter, a Gardner Timing-Error Detector, a loop filter and a Timing Control Unit.

In the first step, the received continuous signal is oversampled discretized with a fixed asynchronous local frequency $f_s = 1/T$. Then, with the aid of the down-converter, it is mixed down into the baseband area and fed to the matched filter. After signal level correction in the AGC unit and carrier synchronization, the signal can be described as follows:

$$x(kT) = \sum_{n} i(n) \cdot r_p(kT - nT_c - \tau)$$ \hspace{1cm} (13)

Thereby $i(n)$ describes the $n$-th chip, $T$ the sampling period, $T_c$ the chip duration and $r_p(u)$ is the auto-correlation function of the pulse shape and $\tau$ the unknown timing delay. The goal of the Timing Recovery Unit is to eliminate $\tau$, i.e. each resulting sample is aligned with the maximum eye opening.

This can be achieved by shifting the asynchronous signal by means of fractional delay interpolation, so that after interpolation the data looks as if it had been sampled at the optimal sampling point. To accomplish this, first the timing error $e(n) = f(\tau)$ is determined in the Timing Error Detector. Then $e(n)$ is fed to the loop filter to determine the corresponding phase and frequency error of local chip clock. Subsequently, the Timing Control Unit generates a fractional delay $\Delta$ from the loop filter output signal. This fractional delay $\Delta$ is required to correct the estimated timing offset $\tilde{\tau} = -\tau$ by sample value correction via interpolation in the interpolator. At the same time, the Timing Control Unit calculates the optimum sampling time in the maximum amplitude of the symbol, i.e. it adjust the local chip clock.

### 4.3.1 Interpolation unit

As mentioned above, the fraction delay filter is used to compute desired samples of $y(nT_c)$ at the optimum sampling instances from the available sample $x(kT)$. To ensure a linear-phase transmission behaviour of the filter, an odd-order polynomial is chosen. However, due to the fact that interpolation with a 1st degree polynomial leads to large deviations, the next option of a 3rd degree polynomial is used. The resulting algorithm for calculating the desired interpolation value is:
4.3 Timing recovery

| i | b_3(i) | b_2(i) | b_1(i) | b_0(i) |
|---|--------|--------|--------|--------|
| -2 | 1/6    | 0      | -1/6   | 0      |
| -1 | -1/2   | 1/2    | 1      | 0      |
| 0  | 1/2    | -1     | -1/2   | 1      |
| 1  | -1/6   | 1/2    | -1/3   | 0      |

Table 1: Fraction delay filter coefficient

\[
y(nT_c) = x ((k + \Delta) T) = \sum_{l=0}^{p} \Delta^l \sum_{i=-2}^{1} b_l (i) x ((\Delta - i) T)
\]  

where \( p \) represents the order of the used interpolation polynomial, \( \Delta \) the fractional delay of the Timing Control Unit and \( b_l (i) \) the corresponding filter coefficient, Table 1.

These filter coefficients are obtained by determining the polynomial coefficients of the 3rd degree interpolation polynomial:

\[
x(k + \Delta) = b_3 [(k + \Delta) T]^3 + b_2 [(k + \Delta) T]^2 + b_1 [(k + \Delta) T] + b_0
\]

as a function of \( \Delta \), taking into account the four given samples, which are arranged in pairs to the left and right of the value to be interpolated, cf. Figure 8.

A detailed description of the calculation of the filter coefficient as well as a deeper description of the functionality of the Timing Control Unit is omitted and reference is made to the corresponding sources [32] [36] [35].

4.3.2 Timing Error Detector

Implemented TED use the Gardner algorithm to determine one timing error value \( e(n) \) per chip. The algorithm is based on a delay difference between the current sample and another sample of the same symbol delayed by half the symbol period and and requires 2 samples per chip. To determine the timing error, 3 consecutive samples are used which are shifted by half a chip to each other. The error signal is finally obtained according to the following equation [37]:

\[
e(n) = y ((n - 1/2) T_c) \cdot [y ((n - 1) T_c) - y (nT_c)]
\]

Where \( y(nT_c) \) are generally complex values. If the sampling is performed at the optimum time point, two values are located in the chip center and one exactly at the transition between two chips, \( e(n) = 0 \). If sampling is premature, then \( e(n) < 0 \), if sampling is delayed, then \( e(n) > 0 \). The advantage of this algorithm is the insensitivity to a carrier frequency offset, thus no previous carrier synchronization is required.
4.3.3 Timing Control Unit

The Timing control unit provides the interpolator with the fractional interval $\Delta$ and the TED with the strobe signal $CLK$ to calculate the correct timing errors once per chip. The interpolation is performed for every sample, and a strobe signal is used to determine if the interpolant is taken as output value. The operation principle of the timing controller is based on the Modulo-1 decrements counter. The counting frequency is determined by the constant $1/N$, where $N$ is the number of samples per chip. The output of the Modulo-1 counter is defined as:

$$\Delta(n) = \begin{cases} N \cdot \delta(k) & \text{CLK} = 1 \\ \Delta(n - 1) & \text{else} \end{cases}$$  \hspace{1cm} (17)

with

$$\delta(k) = [\delta(k - 1) - M(k - 1)] \mod 1$$  \hspace{1cm} (18)

and

$$M(k) = 1/N + \nu(n)$$  \hspace{1cm} (19)

where $\nu(n)$ corresponds the loop filter output and $\delta(k)$ corresponds each sample calculated $\Delta$. The $\nu(n)$ signal from the loop filter adjusts the amount by which the counter decrements and $\delta(k)$ is only passed to the interpolation filter as $\Delta$ if the strobe signal is valid.

4.4 Loop-Filter

For both carrier and clock synchronization, a time discrete Proportional-Integral (PI) filter is used to calculate the control variable for the frequency and phase offset. The filter is a 1st order filter with the following transfer function in the z-domain [38]:

$$F(z) = \frac{C_2 + C_1 (1 - z^{-1})}{1 - z^{-1}}$$  \hspace{1cm} (20)

The gain parameters $C_1$ and $C_2$ define the behavior of the closed loop and are calculated as follows:

$$C_0 = \frac{1}{K_0K_D} \cdot \frac{8\zeta\omega_nT_c}{4 + 4\zeta\omega_nT_c + (\omega_nT_c)^2}$$  \hspace{1cm} (21)

$$C_1 = \frac{1}{K_0K_D} \cdot \frac{4(\omega_nT_c)^2}{4 + 4\zeta\omega_n + (\omega_nT_c)^2}$$  \hspace{1cm} (22)

$\zeta$ is the loop attenuation coefficient, $K_0$ the numerically-controlled oscillator (NCO) gain, $K_D$ the error detector gain, $T_c$ the chip interval and $\omega_n$ natural frequency. Values from Table 2 are used for the carrier synchronization loop respectively timing recovery loop. The NCO Gain $K_0$ correspond to the gradient of characteristic curve of the respective NCO. The Error Detector Gain $K_D$ can be taken from the respective S-curve of Error Detector [32].

4.5 Frame Synchronisation

After successful carrier synchronization and timing recovery, the next step is to locate a structure in the chip stream within which the valid data is located.

For the reliable detection of a frame start within the chip stream, a 78-chip synchronization word is used, which consists of a 64-chip long code word and a 14-chip long guard interval. The code words are
Table 2: Loops parameter

| K₀ | K_D | ζ | B_n | ω_n | T_c |
|----|-----|----|-----|-----|-----|
| 1  | 1.25| 0.7071 | 100 Hz | 1.89B_n | 125μs |

Figure 9: Frame Synchronisation Unit

lines of the Hadamard-Matrix $H_8$ spread with a spreading factor of 8, which are recursively derived from the formation rule:

$$H_{2n} = \begin{pmatrix} H_n & H_n \\ H_n & -H_n \end{pmatrix}$$

with

$$H_1 = 1$$

The selected codewords ($H_{8,3}, H_{8,5}$) have very good aperiodic autocorrelation properties. This ensures a sufficient distance between the maxima of frame start detection and the side lobes.

The detection of the synchronization pattern is performed by a correlator realized in FIR filter structure, which cross-correlates the local version of the synchronization pattern with the incoming baseband symbol stream. The amount of the cross-correlation is then squared. By applying a non-linear function, the distance between the main maxima and the possible sidelobes is further increased. This enables reliable detection even with a very low SNR. If the set threshold value is exceeded, a preamble is detected and valid data follows. The data can then be despreaded and demodulated. The block diagram of the frame synchronization unit is shown in Figure 9.

4.6 Despreading and demodulation

After synchronizing all three levels, the received data must now be despreaded and demodulated. After clock synchronization, chip stream to be treated is now available as chip/sample. The code phase position required for successful despreading of the data is also known due to the detection of the start of frames in the frame synchronization. Now the data is fed to a despreading unit in FIR filter structure. This delivers all $L$ (length of code word) chips the despreaded symbol, which is converted into a data bit in the DBPSK demodulation unit. The resulting data bit stream is then stored in a queue register.

5 Simulation results

Figure 10 shows the structure of the DC grid which was used for the simulative performance analysis of the implemented transmission system. It is a low voltage direct current circuit consisting of two generator converters (G1 and G2) and three consumer converters (L1-L3). Both the converters on the generator side and on the load side are synchronous DC-DC buck converters. This structure is based on the structure
for testing the power/signal dual modulation (PSDM) Techniques for packet based energy dispatching from [5]. This modified simulation example for the power/signal dual modulation technique, which in contrast to the original version is equipped with the transmission system developed in the present article, is intended to show that the information exchange between generator and load required for the exchange of the energy packets does not require a third-party synchronization unit. Furthermore, all parameters required for successful information and energy exchange can be derived from the received signal itself.

Figure 11 (a) shows the output signal of the generator (G1). It supplies the DC bus with 15V DC voltage. In the context of power/signal dual modulation, the existing residual ripple of the DC voltage no longer represents only the unwanted noise; it is used constructively for information transmission. The messages sent by G1 for testing are coded alternately with the unique sequence S1 for load L1 and S2 for load L2. This DC voltage superimposed with the information signal is available as a broadcast signal to all devices connected to the bus.

At the beginning of this simulation example t = 0s, the three loads are operated in listening mode. Simultaneously, L1 and L2 are configured as high-impedance (I_{L1} = I_{L2} = 0) and L3 is operated with a constant nominal current of (I_{L3} = 4A), cf. Figure 11 (d), (g) and (h). As seen from the correlation peaks in Figure 11 (b) L1 detects at time t = 35 ms and t = 185 ms data addressed to him within the received data stream. After the synchronization, decoding and demodulation processes described in section 4 have been performed, the receiver signals the presence of valid data by setting the signal “Valid data available” to high Figure 11 (c) and passes the data to the control unit of load L1 for further processing. After elimination of the metadata by receiver, the data contains the control information regarding the amount of load current required and how long this should be present. This data is interpreted in the control unit and then the current flow enable signal is activated for the required time Figure 11 (c) and the required current level is set for 35 ms. A similar process occurs at time t=110ms for load L2, see Figure 11 (e), (f) and (g). The resulting total current is shown in subplot (i). In the following subsections the results of the realized synchronization level are presented. These enable the asynchronous transmission of energy packets via PSDM and derivation of metadata from the received data.

In order to test the AGC of the implemented receiver, the information part (i.e. high-frequency part) of the broadcast signal undergoes time-variable random amplification (G = 0.5 - 1.25). The change period is 175ms. Figure 12 summarizes the simulation results of the Adaptive Gain Control tests. Subplot (a) shows the received signal in the passband, which varies randomly every 175ms. In subplot (b) the corresponding baseband signal before the AGC is shown, which changes in the same way. In subplot (c) the gain factor is shown which is applied to keep the output signal constant according to the reference. Finally, the subplot (d) shows the nearly constant baseband signal after the AGC.
Figure 11: Simulation results
Next, the results of the phase and frequency offset correction are presented using the carrier synchronization unit. Figure 13 shows the correction process of a phase offset between the carrier wave and the phase of the local oscillator of $\pi/6$. Subplot (a) shows the asynchronously downconverted baseband signal. Due to the phase shift, part of the signal power is transferred to the imaginary part (red). Subplot (b) shows the output of the phase error detector. Subplot (c) shows the resulting correction value $\tilde{\phi}$ and subplot (d) the baseband signal after phase offset correction.

The carrier synchronization results at a frequency offset are shown in Figure 14. The frequency offset that is used is $\Delta f = 5$Hz.

The results of Chip Clock Recovery are summarized below. The sampling frequency offset of $\Delta f = 2$Hz is used to test the Timing Recovery Unit. Subplot (a) of Figure 15 shows the baseband signal of the received signal $r(t)$ sampled without the local clock recovery. As one can see, plot (a) contains samples that should not be present in a DBPSK signal. These result from an asynchronous sampling. In the subplot (b) the same signal is shown but after the chip clock recovery. The constellation diagrams, Figure 16, further clarify the asynchronicity between the received data and the local clock as well as the result of the synchronisation by the clock recovery unit. Figure 17 shows the corresponding estimated timing error and the resulting fractional delay for timing error correction.

Finally, as described in Section 4, the frame synchronization, the despreading of the chips to the DBPSK symbols and finally the demodulation of the data is performed. The results of these operations for two received data frames is shown in Figure 18. Subplot (a) shows the received chipstream. The result of the cross correlation for the preamble detection is shown in the subplot (b). Subplot (c) shows the valid-frame-detected signal and subplot (d) shows the corresponding DBPSK symbols.

In contrast, Figure 19 shows the same procedure but for the 2nd load. Since this load expects data coded with L2 unique sequence, no valid message is detected, which can be seen from the result of the cross correlation.

A series of ten information frames are sent to check the overall functionality of the implemented receiver. The received binary data are then cross-correlated with the transmitted data. The result of the cross-correlation is shown in Figure 20. A complete match of the transmitted and the received data can be recognized by the unique peak at $\tau = 0$. 

Figure 12: Results AGC test
Figure 13: Results carrier synchronization for phase offset

Figure 14: Results carrier synchronization for frequency offset
Figure 15: Baseband signal before and after timing recovery

Figure 16: Received signal constellation diagram. (a) before and (b) after clock recovery

Figure 17: Estimated timing error and the resulting fractional delay
Figure 18: Result frame synchronisation load 1

Figure 19: Result frame synchronisation load 2
6 Conclusion and Outlook

The present paper extends previous contributions [4, 5] regarding packet-based energy transmission by describing a practicable design of an energy packet receiver which recovers the required synchronicity information directly from the received signal itself. The main focus is on the reception and lossless preprocessing and interpretation of the metadata of the information part of the energy packet. For this purpose, implemented solutions for the respective synchronization levels (i) Carrier Recovery, (ii) Clock Recovery and (iii) Frame Recovery are discussed in detail. Drawing upon a DC grid example, simulation results show the performance and applicability of the proposed novel receiver for packet based energy dispatching.

As future work, the proposed approach of packet-based energy distribution will be implemented and validated within the KIT Energy Lab 2.0 infrastructure [39].

References

[1] G. Strbac, *Energy Policy* 2008, 36, 12 4419 , foresight Sustainable Energy Management and the Built Environment Project.

[2] Ming Zhou, Yajing Gao, Gengyin Li, In 2008 Third International Conference on Electric Utility Deregulation and Restructuring and Power Technologies. 2008 545–550.

[3] B. Zhou, W. Li, K. W. Chan, Y. Cao, Y. Kuang, X. Liu, X. Wang, *Renewable and Sustainable Energy Reviews* 2016, 61 30 .

[4] A. Monti, E. De Din, D. Müller, F. Ponci, V. Hagenmeyer, In 2017 IEEE Conference on Energy Internet and Energy System Integration (EI2). 2017 1–6.

[5] E. De Din, A. Monti, V. Hagenmeyer, K. Wehrle, In e-Energy’18, ISBN 9781450357678, 2018 361–365.

[6] M. Chen, H. V. Poor, *IEEE Electrification Magazine* 2020, 8, 3 6.

[7] I. Kouveliotis-Lysikatos, N. Hatziargyriou, Y. Liu, F. Wu, *Journal of Modern Power Systems and Clean Energy* 2020, 1–11.

[8] H. Zhang, H. Zhang, L. Song, Y. Li, Z. Han, H. V. Poor, *IEEE Journal on Selected Areas in Communications* 2020, 38, 1 17.
REFERENCES

[9] T. Sato, D. M. Kammen, B. Duan, M. Macuha, Z. Zhou, J. Wu, M. Tariq, *Smart Grid Standards: Specifications, Requirements, and Technologies*, Wiley, s.l., 1. aufl. edition, 2015.

[10] V. C. Gungor, B. Lu, G. P. Hancke, *IEEE Transactions on Industrial Electronics* 2010, 57, 10 3557.

[11] G. Tuna, V. C. Gungor, K. Gulez, *International Journal of Distributed Sensor Networks* 2013, 9, 2 796248.

[12] F. Wiegel, V. Hagenmeyer, G. Oberschmidt, In *2018 IEEE International Conference on Smart Energy Grid Engineering (SEGE)*. IEEE, ISBN 978-1-5386-6410-0, 8/12/2018 - 8/15/2018 205–211.

[13] J. K. Cavers, *Mobile Channel Characteristics*, volume 555 of *The International Series in Engineering and Computer Science*, Kluwer Academic Publishers, Boston, 2002.

[14] P. Thubert, T. Winter, A. Brandt, J. Hui, R. Kelsey, P. Levis, K. Pister, R. Struik, J. Vasseur, R. Alexander, *IETF 2012, RFC 6550*.

[15] K. Wehrle, *Modeling and Tools for Network Simulation*, Springer-Verlag Berlin Heidelberg, Berlin, Heidelberg, 2010.

[16] C. Cano, A. Pittolo, D. Malone, L. Lampe, A. M. Tonello, A. G. Dabak, *IEEE Journal on Selected Areas in Communications* 2016, 34, 7 1935.

[17] A. M. Tonello, L. Lampe, T. G. Swart, editors, *Power line communications: Principles, standards and applications from multimedia to smart grid*, John Wiley & Sons, Chichester, UK and Hoboken, NJ, second edition edition, 2016.

[18] L. Lampe, A. M. Tonello, D. Shaver, *IEEE Communications Magazine* 2011, 49, 12 26.

[19] A. Pinomaa, J. Ahola, A. Kosonen, *IEEE Communications Magazine* 2011, 49, 12 55.

[20] S. Galli, A. Scaglione, Z. Wang, *Proceedings of the IEEE* 2011, 99, 6 998.

[21] Signalling on low-voltage electrical installations in the frequency range 3 kHz to 148.5 kHz - part 1: General requirements, frequency bands and electromagnetic disturbances, 2011.

[22] J. Wu, J. Du, Z. Lin, Y. Hu, C. Zhao, X. He, *IEEE Transactions on Industrial Electronics* 2015, 62, 2 1291.

[23] R. Wang, Z. Lin, J. Du, J. Wu, X. He, *IEEE Transactions on Power Electronics* 2017, 32, 6 4455.

[24] J. Du, J. Wu, R. Wang, Z. Lin, X. He, *IEEE Transactions on Power Electronics* 2017, 32, 1 693.

[25] Y. Zhu, J. Wu, R. Wang, Z. Lin, X. He, *IEEE Transactions on Industrial Electronics* 2018, 1.

[26] C. R. Johnson, A. G. Klein, W. A. Sethares, *Software receiver design: Build your own digital communications system in five easy steps*, Cambridge University Press, Cambridge and New York, 2011.

[27] J. B. Anderson, *Digital transmission engineering*, IEEE series on digital & mobile communication. IEEE Press Wiley-Interscience and IEEE Xplore, Piscataway, New Jersey and Hoboken, New Jersey and Piscataway, New Jersey, second edition edition, 2006.

[28] A. J. Viterbi, *CDMA: Principles of spread spectrum communication*, Addison-Wesley wireless communications series. Addison-Wesley, Reading, Mass., [nachdr.] edition, 2001.

[29] B. Han, Ph.D. thesis, Karlsruher Institut für Technologie (KIT), 2017.

[30] H. Zhou, C. Nicholls, T. Kunz, H. Schwartz, Carleton University, Systems and Computer Engineering, Technical Report SCE-08-12 2008.

[31] U. Mengali, A. N. D’Andrea, *Synchronization techniques for digital receivers*, Applications of communications theory. Plenum Press, New York, 1997.
[32] M. Rice, *Digital communications: A discrete-time approach*, Pearson international edition. Pearson/Prentice Hall Pearson Education International, Upper Saddle River, New Jersey, 2009.

[33] R. Scholtz, *IEEE Transactions on Communications* 1980, 28, 8 1204.

[34] F. M. Gardner, *Phaselock techniques*, Wiley-Interscience, Hoboken, NJ, 3. ed. edition, 2005.

[35] F. Gardner, *IEEE Transactions on Communications* 1993, 41, 3 501.

[36] L. Erup, F. M. Gardner, R. A. Harris, *IEEE Transactions on Communications* 1993, 41, 6 998.

[37] F. Gardner, *IEEE Transactions on Communications* 1986, 34, 5 423.

[38] B.-Y. Chung, C. Chien, H. Samueli, R. Jain, *IEEE Journal on Selected Areas in Communications* 1993, 11, 7 1096.

[39] V. Hagenmeyer, H. Kemal Çakmak, C. Düpmeier, T. Faulwasser, J. Isele, H. B. Keller, P. Kohlhepp, U. Kühnapfel, U. Stucky, S. Waczowicz, R. Mikut, *Energy Technology* 2016, 4, 1 145.