Information Density in Multi-Layer Resistive Memories

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Abstract—Resistive memories store information in a crossbar arrangement of two-terminal devices that can be programmed to patterns of high or low resistance. While extremely compact, this technology suffers from the “sneak-path” problem: certain information patterns cannot be recovered, as multiple low resistances in parallel make a high resistance indistinguishable from a low resistance. In this paper, a multi-layer device is considered, and the number of bits it can store is derived exactly and asymptotic bounds are developed. The information density of a series of isolated arrays with extreme aspect ratios is derived in the single- and multi-layer cases with and without peripheral selection circuitry. This density is shown to be non-zero in the limit, unlike that of the arrays with moderate aspect ratios previously considered. A simple encoding scheme that achieves capacity asymptotically is presented.

Index Terms—Memristors, combinatorial mathematics, resistance, memory architecture, information theory.

I. INTRODUCTION

COMPACT non-volatile data storage systems are a key component of modern computer systems. With advances in materials science and slowing of the shrinking of the transistor technologies that underlie modern solid-state storage, researchers are increasingly exploring alternative storage technologies. One such technology is the resistive memory array, which has received much attention recently through developments in memristor technology.

Various materials have been considered for resistive memory arrays, including nanowires [3] and, more commonly, memristors (see [4] for a survey). Memristors are passive two-terminal circuit elements whose resistance can be changed when a sufficiently extreme voltage is applied across the terminals. The device maintains its new resistance after the applied voltage is removed, and will function as a resistor when less extreme voltages are applied. Most commonly and most simply, the memristor will change fairly rapidly between a high-resistance state and a low-resistance state, making it a binary device for practical purposes. The memristor was first proposed as a theoretical device by Chua in 1971 [5]. However, it was not until 2008 that a feasible method for fabricating such a device was suggested [6]. Since then, many memristor technologies have been explored (see [4] for an extensive review).

In memory storage systems, memristors are typically organized in crossbar fashion, with resistive material separating some number $n_0$ of parallel rows of wires from some number $n_1$ of parallel columns of wires. A memristor is placed at each row-column intersection, as shown in Figure 1. With this design we have a single layer of memristors in a rectangle of $n_0$ devices by $n_1$. The memristors can be programmed to values in a set of resistances, typically a binary set $\{H, L\}$, where $H$ is a high value, and $L$ is a low value. The ideal case is $H \to \infty$ and $L \to 0$. We will refer to this architecture more generally as a “resistive array,” since it has also been considered in other (non-memristor) resistive memories [3]. This architecture can be generalized to an $\ell$-layer version, with alternating layers of wires of dimensions $n_0 \times n_1 \times \cdots \times n_\ell$ connected by resistive elements. (See, e.g., [7] for a review of current work on this architecture.)

The crossbar architecture has many benefits. First, each memory element has two terminals, which simplifies the device architecture compared to typical transistor-based architectures such as flash. This results in improvements in density and, depending on the encoding method, possible simplifications in reading and writing schemes. Second, for manufacturing technology working at a particular technology node, it is possible to make memristors smaller (i.e., with dimensions closer to the node’s feature length) without encountering many of the problem, such as reliability and leakage, that occur when transistors for data storage are fabricated at the same scale [4].

Despite these advantages, there is a major problem with the crossbar architecture. In a large number of patterns of high and low resistances, low-resistance paths known as “sneak paths” are present in parallel with a single high resistance, with the currents passing through these paths known as “sneak currents”. If data is written into such a pattern, this characteristic can cause ambiguity when trying to read an individual resistance.

As an illustrative example of sneak paths, consider the array diagrammed in Figure 1. Suppose we want to determine the resistance at position $(R_3, C_0)$. In the example, this device is in a high-resistance state, indicated by an unfilled resistor symbol. A natural approach to identifying a resistance is to apply a voltage to the wire in row 3 and, through some sensing device, measure the current flowing out of the wire in column 0. This measurement is clearly a function of resistance at resistor $(R_3, C_0)$. In this example, however, a low resistance path through resistors $(R_0, C_0)$, $(R_0, C_2)$, and $(R_3, C_2)$ runs

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parallel to the high resistance at position \((R_3, C_0)\). Thus we measure a much smaller resistance, most likely much closer to the low resistance value, which is typically very small. Effectively, the high resistance is misread as a low resistance.

The sneak-path problem can be addressed in several ways. Several sensing approaches have been developed, in which the resistance is estimated by taking several measurements in the circuit \([9], [10]\), which have the disadvantage of requiring more circuit measurements per bit read. Electronic approaches include isolating each resistance with a selection device (e.g., a diode or MOS transistor) \([7], [11]\). Another method adds peripheral circuitry for redistributing sneak currents \([12]\). These methods have the disadvantage of increasing the size of the device, although progress has been made with placing selection diodes on top of the resistive elements, sometimes at the cost of increased power consumption \([7]\).

In this paper, we treat this as a problem in information theory. Cassuto et al.’s work \([8]\) shows that an array will contain sneak paths if and only if there exist some coordinates \((R_{x_1}, C_{y_1}), (R_{x_2}, C_{y_2}), \ldots, (R_{x_n}, C_{y_n})\) (i.e., the corners of some rectangle) exactly three of which indicate low resistance. Because of this, an array without sneak-paths is referred to variously as an “isolated zero rectangle free array” \([8]\) or a “\(T\)-avoiding matrix” \([13]\), and the problem may be considered a problem in constrained coding. Cassuto et al. propose an encoding scheme without sneak paths that approaches capacity asymptotically. Their paper in turn has mathematical roots in Sotiriadi’s work on nanoscale crossbar devices \([3]\), which derives exact and asymptotic expressions for the capacity. Similar derivations are made independently in the combinatorics literature \([13]\), generalizing the underlying mathematical problems, and deriving some related generating functions.

Building on this prior work, we will take an information-theoretic approach here. Given a resistive array, we want to develop encoding and decoding schemes that allow us to map a message into a pattern of high and low resistances in the array which may be recovered through a suitable series of measurements. The present work makes three main contributions:

1) We derive exact and asymptotic expressions for the capacity of multi-layer devices: the logarithm of the number of patterns \(T_L(n_0, \ldots, n_L)\) that can be stored in such a device.

2) We derive expressions for the information density of single- and multi-layer devices, and demonstrate that a tiled series of isolated arrays with extreme aspect ratios has an improved information density.

3) We present a simple encoding scheme that achieves capacity asymptotically for such a series of arrays.

The remainder of this paper is divided into five sections. Section II provides a mathematical background. Section III provides a brief overview of existing capacity derivations in single-layer devices, and derives an analogous expression for multi-layer devices. Section IV derives an asymptotic expression for this capacity. Section V motivates the use of information density as an important metric for resistive arrays, as distinct from the capacity metric of \([8]\), and provides an analysis of the optimal size of an isolated array to tile. Section VI proposes encoding schemes in the single- and multi-layer cases that approach capacity asymptotically.

II. Mathematical Background

We will use a graph-theoretical model to describe resistive array states in the idealized model where \(H \to \infty\) and \(L \to 0\). Recall that an undirected bipartite graph \(G\), denoted \(G = (V, W, E)\), consists of two disjoint sets of nodes \(V\) and \(W\), and a set of edges \(E\) of the form \(\{v, w\}\) where \(v \in V\) and \(w \in W\). If \(\{v, w\} \in E\), we say that \(v\) and \(w\) are neighbors.

A. Single-layer Devices

We will first consider single-layer devices. The state of a resistive array with \(n_0\) wires on one edge and \(n_1\) on the other maps naturally to a matrix representation as follows, equivalent to the notion of a “configuration” in \([3]\).

**Definition 1 (Array state matrix):** The array state matrix for a single-layer \(n_0 \times n_1\) resistive array is the matrix \(A \in \{0, 1\}^{n_0 \times n_1}\) with elements \(A_{ij}\) satisfying

\[
A_{ij} = \begin{cases} 
0, & \text{if } R(i, j) = H; \\
1, & \text{if } R(i, j) = L,
\end{cases}
\]

where \(R(i, j)\) is the resistance of the \((i, j)\)th element of the array, with \(i \in \{0, \ldots, n_0 - 1\}, j \in \{0, \ldots, n_1 - 1\}\).

Note that in graph-theoretical terms \(A\) is the biadjacency matrix for the sets of row and column wires (e.g., the sets of \(R_{y}\)s and \(C_{x}\)s in Figure 1). Conceptually, it is often more useful to map the matrix representation of a resistive array to a graph that represents the connectedness of the array. We are interested in the following class of graphs that represent how the layers of wires are connected through any low-resistance path.

**Definition 2 (Connectedness graph):** A connectedness graph is a bipartite graph with the property that if two vertices have a common neighbor, they have all their neighbors in common.

This means that in a connectedness graph \(G = (V, W, E)\), if there is any path connecting \(v \in V\) and \(w \in W\), then \(\{v, w\} \in E\). Such a graph is said to represent an array state matrix \(A\) of an \(n_0 \times n_1\) resistive array if \(V = \{v_0, \ldots, v_{n_0 - 1}\}\),
will need the following definitions. This will correspond to distinguishable array state matrices. This will even though in Figure 1, $G$ device with connectedness graph indicates that wires of the graph. In this example, the upper dot connection between direct connections and sneak paths; this the connectedness graph reflects the reality of making measurements on the array.

The connected components of connectedness graphs are always complete bipartite subgraphs (“bicliques”). These correspond to collections of wires that are connected to each other through low-resistance paths. If we use a connectedness graph to represent an array state matrix, we cannot distinguish between direct connections and sneak paths; this the connectedness graph reflects the reality of making measurements on the array.

Since connectedness graphs always decompose into disjoint complete bipartite subgraphs, we introduce a simplified “dot-graph” representation. Figure 2 gives the dot-graph representation for the array of Figure 1. The dot-graph representation is based on the bipartite graph representation, in which the two parts of the graph (here labeled ‘0’ and ‘1’) are the sets of row and column wires. Instead of indicating connections between individual vertices, we indicate connections between distinct sets of nodes on each side with an edge with a solid dot. Thus we have one dotted edge per connected component of the graph. In this example, the upper dot connection indicates that wires $R_0$, $R_3$, $C_0$, and $C_2$ are all connected, even though in Figure 1 $R_3$ and $C_0$ are connected only through a sneak-path. As we will see, distinct dot-graphs correspond to distinguishable array state matrices. This will lead to a natural way to enumerate all distinguishable array state matrices which will yield the storage capacity of the array.

In order to discuss distinguishable array state matrices, we will need the following definitions.

Definition 3 (Measurement): A measurement between two disjoint wire sets $\Sigma V \subseteq V$ and $\Sigma W \subseteq W$ in a single-layer device with connectedness graph $G = (V, W, E)$ is denoted $M_{G}(\Sigma V, \Sigma W)$ and is defined by

$$M_{G}(\Sigma V, \Sigma W) = \begin{cases} 1 & \text{if some } \{\sigma V, \sigma W\} \in \Sigma V \times \Sigma W \text{ satisfies } \{\sigma V, \sigma W\} \in E \\ 0 & \text{otherwise.} \end{cases}$$

Thus a measurement between two sets indicates whether there is a connection between any pair of their elements. Physically, this corresponds to applying a voltage to the wires corresponding to the elements of $\Sigma V$ and measuring whether this causes a current to flow through any of the wires corresponding to $\Sigma W$.

Definition 4 (Distinguishable array matrices): Two array matrices $A$ and $A'$ are distinguishable if $G(A) \neq G(A')$.

Equivalently, two array matrices are distinguishable if there is some array measurement that yields different measurements when applied to each of the two arrays. For example, if two wires $v_i \in V$ and $w_i \in W$ are in the same connected component in $G(A)$ and different connected components in $G(A')$, we will have $M_{G(A)}(\{v_i\}, \{w_j\}) = 1$ and $M_{G(A')}(\{v_i\}, \{w_j\}) = 0$, differentiating $A$ from $A'$.

B. Multi-layer Devices

One of the attractive features of resistive memory arrays is the fact that they are composed of two-terminal devices. This reduces the number of connectors required, and means that all connectors can be placed at array edges. One may also stack multiple layers of arrays vertically, producing a very dense device. In such a device, we alternate layers of wires and layers of resistive material, so that each layer of resistive material and the adjacent two wire layers locally have the same architecture as a single-layer device. We call these larger devices multi-layer arrays. See 14 and 7 for electronics and materials science perspectives, and some further illustrations of device architectures. When counting layers, we will count the number of resistive layers (not the number of wire layers). Thus, the devices considered so far have been single-layer devices (with two wire layers).
An example of a circuit diagram for a three-layer device is given in Figure 3. In this example, the top layer consists of memristive devices connecting the $R_i$ and $C_i$ wires. The middle layer consists of devices connecting the $C_i$ and $S_i$ wires. The bottom layer consists of devices connecting the $S_i$ and $D_i$ wires. This means that, for instance, devices $(R_0, C_0)$, $(S_0, C_0)$, and $(S_0, D_0)$ all lie in the same vertical column in the layered device. (We have expanded the circuit diagram somewhat to make the connections easier to see, but it should be remembered that these components do not all lie in the same plane.)

This circuit also illustrates how a multi-layer device may have sneak paths across two or more layers. For instance, there is a sneak-path at $(S_0, C_2)$ despite there being no sneak-paths in the local $(S_1, C_1)$ layer.

We now define the equivalent of the array state matrix for the multi-layer devices. We will let $n_i$ denote the number of wires in wire layer $i$.

**Definition 5 (Array state matrix vector):** The array state matrix vector for an $\ell$-layer resistive $n_0 \times \cdots \times n_\ell$ device is a vector of matrices $A = (A^0, \ldots, A^{\ell-1})$ where $A^k \in \{0, 1\}^{n_k \times n_k}$ has elements $A^k_{ij}$ satisfying

\[
A^k_{ij} = \begin{cases} 0 & \text{if } R^k(i, j) = H; \\ 1 & \text{if } R^k(i, j) = L, 
\end{cases}
\]

where $R^k(i, j)$ is the resistance of the $(i, j)$th element in the $k$th layer.

Note that this is just the vector of array state matrices for the individual layers of the device. For instance, the three-layer circuit in Figure 3 has $A = (A^0, A^1, A^2)$, where $A^0$ is the array state matrix for the $R_i$s and $C_i$s, $A^1$ is the array state matrix for the $S_i$s and $C_i$s, and $A^2$ is the array state matrix for the $S_i$s and $D_i$s. We now define the multi-layer generalization of the connectedness graph as follows.

**Definition 6 ($\ell$-layer connectedness graph):** An $\ell$-layer connectedness graph is an $(\ell + 1)$-partite graph

\[
G = (V_0, V_1, \ldots, V_\ell, E_1, \ldots, E_\ell)
\]

where $E_i \subseteq \{(v_{i-1}, v_i) | v_{i-1} \in V_{i-1}, v_i \in V_i\}$, with the property for $i = 1, \ldots, \ell$ that if two vertices in $V_i$ have a neighbor in common, they have all their neighbors in common.

Such an $\ell$-layer connectedness graph is said to represent $(A^0, \ldots, A^{\ell-1})$, the array state matrix vector of a resistive array with $n_i$ wires in wire layer $i$, $i = 0, \ldots, \ell$, if $V_i = \{v_{i,0}, \ldots, v_{i,n_i}\}$ and $A^k_{ij} = 1$ implies $(v_{k-1, i}, v_{k, j}) \in E_k$ and $G$ includes only the edges necessary to meet this condition. Note that $(v_{k-1, i}, v_{k, j}) \in E_k$ does not imply $A^k_{ij} = 1$, rather $(v_{k-1, i}, v_{k, j}) \in E_k$ implies that there is a path between $v_{k-1, i}$ and $v_{k, j}$. The unique connectedness graph representing the array state matrix vector $(A^0, \ldots, A^{\ell-1})$ is denoted $G(A^0, \ldots, A^{\ell-1})$.

The constrained coding problem for the single-layer case extends naturally to the $\ell$-layer case. We may mimic the layout of the circuit diagram in Figure 3 by arranging the elements of the array state matrix vector in a “staircase” shape of the following form:

\[
\begin{align*}
A^0 & \quad (A^1)^\top & A^2 & \quad (A^3)^\top & \quad \cdots & \quad (A^{\ell-3})^\top \\
& \quad (A^{\ell-2})^\top & & & & \quad (A^{\ell-1})^\top
\end{align*}
\]

where in this case $\ell$ is even and $\top$ indicates a matrix transpose. The single-layer isolated zero rectangle constraint must apply to the “staircase” structure in (1). Equivalently, it must apply to each concatenated matrix $[(A^i)^\top | A^{i+1}]$ for $0 \leq i < \ell - 1$. These concatenated matrices and their transposes correspond to each of the horizontal and vertical “steps” in the staircase structure. This constraint is a result of the fact that a sneak-path across three or more wire layers must include a sneak-path across three wire layers, which is contained in some such concatenated matrix.

The dot-graph representation extends naturally to represent this architecture. The graph for the circuit in Figure 3 is shown in Figure 4. As before, a dotted edge between two sets of vertices in this representation corresponds to the complete collection of edges between the two sets of wires in adjacent wire layers (i.e., the biclique).

### III. Counting Sneak-Path-Free Arrays

The capacity of a single-layer device has been derived in several places in the literature [3], [13]. We present another proof here that eases the generalization to the multi-layer case.

#### A. Single-layer Device Capacity

To determine the number of distinguishable resistive array state matrices, we count the number of distinct connectedness graphs. This count is a function of the array dimensions $n_0$ and $n_1$ and we denote it $T_1(n_0, n_1)$. Since this involves partitioning the input and output wires, it will be useful
to recall the following definition, which is applicable when counting partitions.

**Definition 7 (Stirling number of the second kind):** The Stirling number of the second kind, denoted \( \{ n \choose k \} \), is the number of ways in which a set of \( n \) items may be partitioned into \( k \) (non-empty) sets. For \( n > 0 \) and \( k > 0 \) it is equal to

\[
\{ n \choose k \} = \frac{1}{(k-1)!} \sum_{i=0}^{k-1} (-1)^i \binom{k-1}{i} (k-i)^{n-1},
\]

(2)
a reindexed version of the form given in [15, Ch. 1.9], which will be useful in subsequent derivations. Note that \( \{ 0 \choose 0 \} = 1 \), and \( \{ n \choose k \} = \{ 0 \choose k \} = 0 \) when \( n > 0 \) and \( k > 0 \).

Both Sotiriadis and later Ju and Seo derive the value of \( T_1(n_0, n_1) \) using various counting arguments [3], [13]. The proof we present here is similar to the latter, but stated in a form that is more useful to the current application.

**Theorem 8 (Thm. 1)[13 Thm. 3.1]):** There are

\[
T_1(n_0, n_1) = \sum_{k=0}^{\min(n_0+1, n_1)} \binom{n_0+1}{k+1} \binom{n_1+1}{k+1} k!.
\]

distinct \( n_0 \times n_1 \) connected graphs.

**Proof:** Consider the layer of \( n_0 \) wires. Label these wires \( 0, \ldots, n_0-1 \) and partition these labeled wires, plus the symbol \(*\), into \( k+1 \) non-empty subsets. There are \( \{ n_0+1 \choose k+1 \} \) ways to do this. Repeat for the layer of \( n_1 \) wires. In each case, one subset contains the symbol \(*\). Any wires in these subsets will remain unconnected. Connect the \( k \) subsets of the layer of \( n_0 \) wires pairwise with the remaining \( k \) subsets of the layer of \( n_1 \) wires. This can be done in \( k! \) ways. Summing over \( k \) gives the desired final expression for \( T_1 \).

Patterns with different values of \( k \) are distinct, since \( k \) is the number of connected components in the graph. Note that \( T_1(n_0, n_1) = T_1(n_1, n_0) \). The generating function for \( T(n_0, n_1) \) is \( T(x, y) = \exp([e^x-1]e^y-x+y) \) [13] and the sequence \( T(n_0, n_1) \) is number A014235 in the On-Line Encyclopedia of Integer Sequences (OEIS) [16].

**B. Single-layer Capacity Asymptotics**

The exact data storage capacity in bits of an \( n_0 \times n_1 \) array is \( \log T_1(n_0, n_1) \). This expression is difficult to manipulate, however, so it is useful to develop an asymptotic scaling for the capacity. We will consider sequences that are asymptotic in the following sense, following [3].

**Definition 9:** If \( \eta_n \) and \( \zeta_n \) are positive sequences with \( \eta_n, \zeta_n \neq 1 \) for sufficiently large \( n \), we write \( \eta_n \sim \zeta_n \) if \( \log(\eta_n)/\log(\zeta_n) \to 1 \) as \( n \to \infty \).

An asymptotic approximation of the capacity for large \( n_0 + n_1 \) is [3 Thm. 4]

\[
\log T_1(n_0, n_1) \sim (n_0 + n_1) \log(n_0 + n_1).
\]

(4)

While this approximation may be useful for describing the limiting behavior of the system, it does not necessarily give useful numerical results, especially for smaller values of \( n_0 \) and \( n_1 \). For instance, numerical results for the \( n_0 = n_1 \) case suggest that the ratio \( 2n_0 \log(2n_0)/\log T(n_0, n_0) \) is decreasing in \( n_0 \), but only decreases to approximately 1.45 at \( n_0 = 4800 \).

**C. Multi-layer Device Capacity**

We now turn to the \( \ell \)-layer case. Consider an \( \ell \)-layer device with dimensions \( n_0 \times \cdots \times n_\ell \). We will count the number of distinct connected graphs, denoted as \( T_\ell(n_0, \ldots, n_\ell) \) as follows, beginning with a relevant combinatorial definition.

**Definition 10 (Trinomial coefficient):** The trinomial coefficient, denoted \( \binom{n}{i,j,k} \), with \( i + j + k = n \), defined as

\[
\binom{n}{i,j,k} = \frac{n!}{i!j!k!}
\]

is the number of ways in which \( n \) objects may be partitioned into subsets of sizes \( i, j, \) and \( k \).

**Theorem 11:** There are

\[
T_\ell(n_0, \ldots, n_\ell) = \sum_{s_1=0}^{n_0} \cdots \sum_{s_\ell=0}^{n_\ell} \prod_{i=0}^{\ell} \sum_{k_i=\max(s_i, s_{i+1})}^{k_0+1} \binom{n_i+1}{k_i+1} k_i (s_i + s_{i+1} - k_i - k_{i+1}) - s_i
\]

(5)
distinct \( \ell \)-layer connected graphs for an \( n_0 \times \cdots \times n_\ell \) device, where \( s_0 = s_{\ell+1} = 0 \).

**Proof:** We have \( i + 1 \) wire layers of sizes \( n_0, \ldots, n_\ell \) respectively. Consider the layer of \( n_0 \) wires. Label them \( 0, \ldots, n_0-1 \) and partition these wires, plus the symbol \(*\), into \( k_0+1 \) non-empty subsets, as in the single-layer case. There are \( \{ n_0+1 \choose k_0+1 \} \) possible partitions. Repeat for each layer, giving \( \{ n_\ell+1 \choose k_\ell+1 \} \) possible partitions at wire layer \( i \). (These are the partitions that are represented with rounded rectangles in the connectedness graph.)

In wire layer \( i \), we connect the \( k_i \) partitions that do not include the symbol \(*\) to some of the corresponding partitions in layers \( i-1 \) and \( i+1 \) (when they exist). We will connect \( L_i \) of these to partitions in layer \( i-1 \) only, \( U_i \) to partitions in layer \( i+1 \) only, and the remaining \( B_i := k_i - U_i - L_i \) to partitions in both. There are \( B_i \) ways to do this. This means that there are \( s_i := (B_i, L_i, U_i) \) ways to make in \( s_i \) possible pairs. We must therefore sum over all values of

\[
s_i \binom{n_i+1}{k_i+1} \binom{k_i}{k_{i+1}+1} (s_i + s_{i+1} - k_i - k_{i+1} - 1) - s_i
\]

The bounds on the sums in (5) correspond to the terms that give non-zero Stirling numbers and trinomial coefficients.

Since \( s_i \) describes the number of disjoint connections between two wire layers (the number of dots in a layer in the dot-graph representation), and \( k_i \) describes the number of disjoint components in a wire layer (the number of rectangles in a wire layer), connectedness graphs with different values of \( s_i \) or \( k_i \) will always be distinct, and represent distinguishable
array state matrix vectors. Note that when \( \ell = 1 \), \((5)\) simplifies to \( T_1(n_0, n_1) \) given in \((3)\).

To illustrate the idea of the proof, consider the device represented by the graph shown in Figure \((4)\). It has \( n_0 = n_2 = 7 \), and \( n_1 = n_3 = 6 \). Wire layer 0 is partitioned into \( k_0 = 2 \) subsets of sizes 2 and 3, with the remaining 2 wires disconnected. Since this is the first layer, \( B_0 = L_0 = 0 \), so \( U_0 = k_0 = 2 \). There are then \( s_1 = k_0 = 2 \) connections across the first resistor layer. These correspond to the two dot-connections in the first layer in the diagram.

In wire layer 1, we have \( k_1 = 3 \) subsets of wires with one wire disconnected. Out of these 3 subsets, \( L_1 = 1 \) is connected to the lower layer only, \( B_1 = 1 \) is connected to both the lower and upper layer, and \( U_1 = 1 \) is connected to the upper layer only. There are \( s_1 = B_1 + L_1 = 2 \) subsets that connect to the lower layer, and \( s_2 = B_1 + U_1 = 2 \) subsets connecting to the upper layer.

We partition the upper layers similarly, with \( B_2 = L_2 = U_2 = 1 \), \( L_3 = 2 \), and \( B_3 = U_3 = 0 \). Equivalently, \( k_2 = 3 \), \( k_3 = 2 \), and \( s_3 = 2 \).

**D. Multi-layer Capacity Asymptotics**

To develop an asymptotic expression more amenable to interpretation and to manipulation, we first consider the case where all layers have \( n \) wires, analogously to the single-layer derivation in \((3)\). Define \( T_\ell(n) := T_\ell(n, \ldots, n) \) and

\[
Q_n(k, a, b) := a! \left( \frac{k}{a + b - k, k - a, k - b} \right) \left( \frac{n + 1}{k + 1} \right). \tag{6}
\]

Expanding the sums over \( k_0 \) and \( k_\ell \) in \((5)\) gives the alternative form

\[
T_\ell(n) = \sum_{s_1=0}^{n} \cdots \sum_{s_\ell=0}^{n} \left\{ \frac{n + 1}{s_1 + 1} \right\} \left\{ \frac{n + 1}{s_\ell + 1} \right\} s_\ell! \prod_{i=1}^{\ell-1} \min_{i=1}^{\ell-1} \left( n, s_i + s_{i+1} + 1 \right) Q_n(k_i, s_i, s_{i+1}). \tag{7}
\]

We will use the following result from \((3)\).

**Lemma 12** \((3)\), (20)): Given integers \( n \) and \( \rho \), with \( 2 < \rho < n \), define \([n/\rho] := 1 + [n/\rho]\). Then

\[
\left\{ \frac{n}{[n/\rho]} \right\} > \frac{n!}{([n/\rho])! (\rho)^{[n/\rho]}}.
\]

We obtain a lower bound as follows.

**Lemma 13**: For every integer \( \rho \) such that \( 2 < \rho < n \), there exists a function \( L_\ell(n) \) such that \( T_\ell(n) \geq L_\ell(n) \) and \( L_\ell(n) \sim n^{(\ell+1-1)/\rho} \), in the sense of Definition \([3]\).

**Proof**: This proof is analogous to the single-layer proof in \([3]\).

The function \( T_\ell(n) \) is increasing in \( n \). Therefore, using \((7)\).

\[
T_\ell(n) > T_\ell(n - 1) = \sum_{s_1=0}^{n} \cdots \sum_{s_\ell=0}^{n} \left\{ \frac{n}{s_1} \right\} \left\{ \frac{n}{s_\ell} \right\} (s_\ell - 1)! \prod_{i=1}^{\ell-1} \min_{i=1}^{\ell-1} \left( n, s_i + s_{i+1} + 1 \right) \sum_{i=1}^{k_i = \max(s_i, s_{i+1})} Q_{n-1}(k_i - 1, s_i - 1, s_{i+1} - 1).
\]

Take an integer parameter \( \rho \) as in \( \text{Lemma 12} \). Lower bound each sum over \( s_i \) by the \( s_i = [n/\rho] \) term. This gives

\[
T_\ell(n) > \left( \frac{n}{[n/\rho]} \right)^2 \prod_{i=1}^{\ell-1} \min_{i=1}^{\ell-1} \left( n, s_i + s_{i+1} + 1 \right) \sum_{i=1}^{k_i = [n/\rho]} Q_{n-1}(k_i - 1, [n/\rho] - 1, [n/\rho] - 1). \tag{8}
\]

Similarly, lower bound each sum over \( k_i \) by the \( k_i = [n/\rho] \) term, and apply \( \text{Lemma 12} \) giving

\[
T_\ell(n) > \left( \frac{n}{[n/\rho]} - 1 \right)! \ell \left\{ \frac{n}{[n/\rho]} \right\} \ell+1 > \left( \frac{n}{[n/\rho]} - 1 \right)! \ell \left\{ \frac{n}{[n/\rho]} \right\} \ell+1 = \left( \frac{n}{[n/\rho]} - 1 \right)! \ell \left\{ \frac{n}{[n/\rho]} \right\} \ell+1.
\]

Using the properties of the \( \sim \) relationship derived in \((3)\),

\[
L_\ell(n) \sim \frac{(n)!^{\ell+1}}{[n/\rho]!} \sim \frac{n^{(\ell+1)n}}{n^{n/\rho}} = n^{(\ell+1-1)/\rho} n\]

as desired.

To obtain an upper bound, we leverage the following bound, also found in \((3)\).

**Lemma 14** \((3)\), Lem. AI): For \( n \geq m \),

\[
\left\{ \frac{n}{m} \right\} \leq \frac{n!}{m^n (e + 1)^m}.
\]

We now state and prove the upper bound.

**Lemma 15**: There exists a function \( U_\ell(n) \) such that \( T_\ell(n) \leq U_\ell(n) \) and \( U_\ell(n) \sim n^{(\ell+1)/n} \).

**Proof**: Since \( 3^k = \sum_{a,b,c} (a, b, c) \), we may write

\[
T_\ell(n) \leq \sum_{s_1=0}^{n} \cdots \sum_{s_\ell=0}^{n} \left\{ \frac{n + 1}{s_1 + 1} \right\} \left\{ \frac{n + 1}{s_\ell + 1} \right\} s_\ell! \prod_{i=1}^{\ell-1} \min_{i=1}^{\ell-1} \left( n, s_i + s_{i+1} + 1 \right) \sum_{i=1}^{k_i = \max(s_i, s_{i+1})} \frac{n + 1}{k_i + 1}.
\]

Applying Lemma \([3]\) gives

\[
T_\ell(n) \leq \sum_{s_1=0}^{n} \cdots \sum_{s_\ell=0}^{n} \left\{ \frac{n + 1}{s_1 + 1} \right\} \left\{ \frac{n + 1}{s_\ell + 1} \right\} s_\ell! \prod_{i=1}^{\ell-1} \min_{i=1}^{\ell-1} \left( n, s_i + s_{i+1} + 1 \right) \sum_{i=1}^{k_i = [n/\rho]} Q_{n-1}(k_i - 1, s_i - 1, s_{i+1} - 1). \tag{9}
\]

Applying Lemma \([14]\) gives

\[
T_\ell(n) \leq \sum_{s_1=0}^{n} \cdots \sum_{s_\ell=0}^{n} \left\{ \frac{n + 1}{s_1 + 1} \right\} \left\{ \frac{n + 1}{s_\ell + 1} \right\} s_\ell! \sum_{i=1}^{k_i = [n/\rho]} Q_{n-1}(k_i - 1, s_i - 1, s_{i+1} - 1).
\]
The sum in $s_1$ can be bounded by the Taylor series of an exponential. Since the other sums are increasing in the variable of summation, each summand can be bounded by the $n$th term. This gives

$$T(n) \leq (n+1)^{\ell+1} + (n+1)\ell e^{(n+1)} \left( 3^n (e+1)^n \right)^{\ell-1}$$

$$= U(n) \sim n^{(\ell+1)n}.$$

Therefore, $U(n)$ has the desired properties.

We now derive an asymptotic expression for $T(n)$.

**Theorem 16:** The function $T(n)$ satisfies

$$T(n) \sim n^{(\ell+1)n}.$$

**Proof:** From Lemmas [13] and [15] we know that for any integer $\rho$ such that $2 < \rho < n$, we may bound $T(n)$ by $U(n) < T(n) < U(\rho)(n)$. This means that

$$\left(1 - \frac{1}{\ell + 1}\right) \log(\rho) \log(n^{(\ell+1)n}) < \log(T(n)) \leq \log(U(n)) \leq \log(n^{(\ell+1)n}).$$

By Definition [9] and Lemmas [13] and [15],

$$\lim_{n \to \infty} \log(U(n)) \log(n^{(\ell+1)n}) = \lim_{n \to \infty} \log(U(n)) \log(n^{(\ell+1)n}) = 1.$$  

Applying this result to [9] gives

$$\left(\ell + 1 - \frac{1}{\rho} \right) \leq \lim_{n \to \infty} \inf \log(T(n)) \log(n^{(\ell+1)n}) \leq \lim_{n \to \infty} \sup \log(T(n)) \log(n^{(\ell+1)n}) \leq \ell + 1$$

for every $\rho > 2$. Taking $\rho \to \infty$ gives $\lim_{n \to \infty} \log(T(n)) \log(n^{(\ell+1)n}) = \ell + 1$, so $T(n) \sim n^{(\ell+1)n}$.

This asymptotic result reveals a drawback of this type of memory with this uniform geometry: the number of bits stored per unit area is

$$\frac{\log T(n)}{n^2} \sim \frac{(\ell + 1)n \log n}{n^2} = \frac{(\ell + 1) \log n}{n}$$

which goes to zero as $n$ becomes large.

We can make a similar claim for devices whose wire layers differ in size by a constant factor in the limit:

**Theorem 17:** For a multi-layer device with wire layer dimensions $n_0, \ldots, n_\ell$,

$$T(n_0, \ldots, n_\ell) \sim \prod_{i=0}^\ell n_i^{n_i}.$$  

when $n_i \to \infty$ for each $i$, and $n_i/n_j \to a_{ij} > 0$ for each pair $(i,j)$ and some constant $a_{ij}$.

The proof of this is similar to that of Theorem [16] for both bounds, we proceed analogously except that bounds on sums over $s_i$ and $k_i$ are taken in terms of $n_i$ instead of $n$. The requirement that the wire layer aspect ratios stay constant as we take the limit means that our density still goes to zero analogously to [10].

IV. DENSITY OPTIMIZATION

Not all array aspect ratios have an information density that goes to zero, which means that tiling isolated arrays of these sizes will make a larger array with density bounded away from zero. In this section we explore the information density of these arrays, and derive the optimal size for maximizing density.

A. Density of High-Aspect-Ratio Single-Layer Devices

The approximation to single-layer capacity developed in [4] is only applicable when $n_0/n_1$ approaches a finite positive constant as $n_0$ and $n_1$ increase. We know, for instance, that the density is 1 in the case of a $1 \times n_2$ device, since it is impossible to create a sneak path in such a device. Building on this observation, we will consider the case where $n_0$ becomes large while $n_2$ remains fixed. We first derive bounds on $T_1(n_0, n_1)$.

**Theorem 18:** If positive integers $n_0$ and $n_1$ satisfy

$$n_0 \geq \log_2(n_1 + 1) \frac{n_1(n_1 + 1)}{2}$$

then

$$T_1(n_0, n_1) \leq (n_1 + 1)^{n_0 + 1}.$$  

**Proof:** See Appendix [A].

**Theorem 19:** For positive integers $n_0$ and $n_1$,

$$n_1 + 1 \leq T_1(n_0, n_1).$$

**Proof:** The subset of $n_0 \times n_1$ array state matrices having at most a single 1 in any row, of which there are $(n_1 + 1)^{n_0}$, includes only sneak-path-free array state matrices.

Taking logarithms of Theorems [18] and [19] gives the following.

**Corollary 20:** The number of bits

$$B(n_0, n_1) := \log T_1(n_0, n_1)$$

that can be stored in an $n_0 \times n_1$ array with dimensions satisfying [12] satisfies

$$n_0 \log(n_1 + 1) \leq B(n_0, n_1) \leq (n_1 + 1) \log(n_1 + 1).$$

Dividing [13] by the array area $n_0 n_1$ gives the following corollary.

**Corollary 21:** The bit density of an $n_0 \times n_1$ array with dimensions satisfying [12] satisfies

$$\frac{n_0}{n_1} \log(n_1 + 1) \leq B(n_0, n_1) \leq \frac{n_0}{n_1} \log(n_1 + 1).$$

Taking $n_0 \to \infty$ gives the following result.

**Corollary 22:** For $n_1$ fixed and $n_0 \to \infty$, the bit density of an $n_0 \times n_1$ array converges to $n_1^{-1} \log(n_1 + 1)$ from above. This density is bounded away from zero for fixed $n_1$. In particular, it has maximal value 1 at $n_1 = 1$, meaning that we have one bit per resistive cell if we have a $1 \times n_0$ array.

We can also derive an asymptotic expression for $T_1$ for fixed $n_1$.

**Theorem 23:** For any fixed $n_1$,

$$\lim_{n_0 \to \infty} T_1(n_0, n_1) = 1.$$
and this limit is approached from above.

**Proof:** Using (2), we can write

\[
T(n_0, n_1) = \sum_{i=0}^{n_1} \binom{n_0 + 1}{i+1} \binom{n_1 + 1}{i+1} i!
\]

\[
= \sum_{i=0}^{n_1} \binom{n_1 + 1}{i+1} \left( \sum_{j=0}^{i} (-1)^j \binom{i}{j} (i+1-j)^n_0 \right)
\]

\[
= \sum_{k=0}^{n_1} \sum_{i=k}^{n_1} (-1)^{i-k} \binom{n_1 + 1}{i+1} \binom{i}{k} (k+1)^n_0
\]

\[
= \sum_{k=0}^{n_1} a(k, n_1)(k+1)^n_0
\]

where

\[
a(k, n_1) = \sum_{i=k}^{n_1} (-1)^{i-k} \binom{n_1 + 1}{i+1} \binom{i}{k}.
\]

Since \(a(n_1, n_1) = 1\), \(T(n_0, n_1) = (n_1 + 1)^n_0 + \mathcal{O}(n_1^n_0)\), so

\[
\lim_{n_0 \to \infty} T(n_0, n_1)/(n_0+1)^n_1 = 1
\]
as desired.

**B. Tiling Isolated Arrays**

Despite maximizing the limiting density described in Corollary 22, a \(1 \times n_0\) resistive array becomes impractical to use for large values of \(n_0\). A more common solution to the sneak-path problem is to isolate each memory cell with a selection device such as a diode or a transistor (see e.g., \([11]\) and \([7]\)). Using diodes is particularly appealing, since they are two-terminal elements and therefore require less layout and do not need individual switching signals. The density of such a device does not change with its size or shape, but a non-negligible fraction of the circuit area may be used for the diodes themselves rather than the memory cells, thereby reducing the density of memristive devices (though perhaps not the information density). It is possible in some cases to stack a small selection device on top of the memristor, which does not require additional area. This architecture can have increased power consumption, which means it may not be desirable for all applications \([7]\). Another alternative that may increase power consumption involves grounding a large fraction of the wires in one direction \([8]\).

We propose an alternative approach. Consider an \(n_0 \times n_1\) crossbar array with memory cells of unit area. Let us assume the area of each diode is \(\delta\) times the area of a memristive cell. Place diodes on each of the \(n_0 + n_1\) output lines, and tile the resulting isolated array as shown in Figure 5. The diodes isolate the arrays, making it impossible for sneak-paths to form. This architecture will be referred to as an \((n_0, n_1)\) device.

The resulting array has area \(A_{\\text{arr}}(n_0, n_1) := n_0 n_1 + \delta(n_0 + n_1)\). We may bound the array density \(\rho_{\\text{arr}}(n_0, n_1) := B(n_0, n_1)/A_{\\text{arr}}(n_0, n_1)\) using the same approach as in Corollaries 21 and 22, giving the following further corollaries to Theorems 18 and 19.

**Corollary 24:** For an \((n_0, n_1)\) device, if \(n_0\) satisfies (12), then

\[
\frac{n_0 \log(n_1 + 1)}{n_0 n_1 + \delta(n_0 + n_1)} \leq \rho_{\\text{arr}}(n_0, n_1) \leq \frac{(n_0 + 1) \log(n_1 + 1)}{n_0 n_1 + \delta(n_0 + n_1)}.
\]

**Corollary 25:** For \(n_1\) fixed and \(n_0 \to \infty\), the array bit density \(\rho_{\\text{arr}}(n_0, n_1)\) of an \((n_0, n_1)\) device converges to \(P_{\\text{arr}}(n_1) := (n_1 + \delta)^{-1} \log(n_1 + 1)\).

While the value of \(n_1\) that maximizes \(P_{\\text{arr}}(n)\) can be derived using methods from complex analysis, in practice we will usually evaluate it numerically. The optimal integer value \(n_1^*\) is plotted against different values of \(\delta\) in Figure 6. This figure also shows the bit densities at these choices of \(n_1^*\), with the \(\rho = (1 + \delta)^{-1}\) curve from the existing architecture with one diode per array unit for reference. We see that in all cases, the architecture with fewer diodes has a better bit density than the architecture with diodes at all locations.

In Figure 7 we plot density against area for fixed values of the number of row wires \(n_1\) and the number of column wires \(n_0 \geq n_1\). We plot information density for select values of \(n_1\) and \(\delta = 10\). For \(\delta = 10\), the information density as \(n_0 \to \infty\) becomes larger as we increase \(n_1\) up to \(n_1 = 7\) but decreases again and will ultimately approach zero as \(n_1\) becomes large.

**C. Peripheral Circuitry for Single-Layer Devices**

In practice, the array area \(A_{\\text{arr}}(n_0, n_1)\) is not the area of the entire device. In this section, we take the peripheral circuitry needed for array element selection into consideration. Suppose we tile a number of \(n_0 \times n_1\) devices into a rectilinear layout

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Fig. 5. A 2 × 4 crossbar array with diodes along the edges tiled to make a larger array.

Fig. 6. Optimal array dimension \(n_1^*\) versus diode area factor \(\delta\) in the \(n_0 \to \infty\) regime (right axis) and the resulting bit density for this choice of \(n_1\), compared to the naive series diode approach (left axis).
of $N_0$ rows and $N_1$ columns of memristive arrays. To select a wire on each edge of the device, we will need demultiplexers of sizes $\log N_0n_0$-to-$N_0n_0$ and $\log N_1n_1$-to-$N_1n_1$. Since a log-$n$-to-$n$ multiplexer has log $n$ selection lines and $n$ output lines, each multiplexer will have an area that scales as $n \log n$ (see e.g., [17, Sec. 8.3]). This means that the overall device area is

$$A_{\delta, \gamma}(N_0, N_1, n_0, n_1) := N_0N_1[n_0n_1 + \delta(n_0 + n_1)] + \gamma(N_0n_0 \log N_0n_0 + N_1n_1 \log N_1n_1)$$

where $\gamma$ is a positive constant. This constant captures the scaling of the transistors in the demultiplexers with respect to the size of the individual array elements. We also define the device information density as

$$\rho_{\delta, \gamma}(N_0, N_1, n_0, n_1) := \frac{N_0N_1B(n_0, n_1)}{A_{\delta, \gamma}(N_0, N_1, n_0, n_1)}.$$

We can then state the following theorem.

**Theorem 26:** If $n_0 \to \infty$ and $N_1 \to \infty$ subject to the constraint that $N_0^{-1} \log n_0 \to 0$ and $n_0^{-1} \log N_1 \to 0$ with $N_0$ and $n_1$ fixed, then $\rho_{\delta, \gamma}(N_0, N_1, n_0, n_1) \to P_{\text{arr}}^{\text{opt}}(n_1)$.

**Proof:** Using Corollary 20 we have, for sufficiently large $n_0$,

$$\frac{N_0N_1\log(n_1+1)}{A_{\delta, \gamma}(N_0, N_1, n_0, n_1)} \leq \frac{n_0 \log(n_1+1)}{A_{\delta, \gamma}(N_0, N_1, n_0, n_1)} \leq \frac{n_0 \log(n_1+1)}{A_{\delta, \gamma}(N_0, N_1, n_0, n_1)}.$$

As $n_0 \to \infty$ and $y \to \infty$ this simplifies to

$$\frac{\log(n_1+1)}{n_1 + \delta + \gamma(\log n_0)/y + \gamma(n_1/x) \log y} \leq \frac{n_0 \log(n_1+1)}{n_0 + \delta + \gamma(\log n_0)/y + \gamma(n_1/x) \log y}.$$

Since $(\log n_0)/y \to 0$ and $(\log y)/n_0 \to 0$, this means that $\rho_{\delta, \gamma}(N_0, N_1, n_0, n_1) \to \log(n_1+1)/(n_1 + \delta) = P_{\text{arr}}^{\text{opt}}(n_1)$, as $n, y \to \infty$ as desired.

---

### D. Multi-layer Density Optimization

Having derived the capacity of multi-layer devices, we can also analyze their information density. For simplicity, both of analysis and ultimately of circuit layout, let us assume that we have $\ell$ layers of memory cells of alternating dimensions, with $\ell$ an even number, so that our wire layer dimensions have the form $n \times m \times n \times m \times \cdots \times n$, so $n_0 = n$ and $n_{2\ell+1} = m$. We will refer to this as an $(m, n)_{\ell}$ device. We state and prove multi-dimensional equivalents of Theorems 18 and 19.

**Theorem 27:** If positive integers $m$ and $n$ satisfy

$$m \geq \log_2 \left( \frac{1}{27} \frac{n^3}{n_0} \right),$$

and $\ell$ is a positive even integer, then

$$T_{\ell}(m, n) \leq \frac{3^\ell (\beta_n - 1)^{\ell/2 - 1} (n + 1)^\ell}{(2n + 1)^2} \left( 2n + 1 \right)^{\ell(m+1)/2}.$$

where $\beta_n := \frac{0.792(n+1)}{m(n+2)}$.

**Proof:** See Appendix B.

**Theorem 28:** For integers $m, n > 0$,

$$(2n + 1)^{\ell m/2} \leq T_{\ell}(m, n).$$

**Proof:** Consider our device as a stack of $\frac{\ell}{2}$ two-layer $n \times m \times n$ subdevices. We may do this if we respect the partitioning of the layers of $n$ wires shared between one device and the next. The $ith$ subdevice has array state matrix $A = [A^{2i-1}, [A^{2i}], \ldots, [A^{2i}], \ldots, [A^2]]$, which is an $m \times 2n$ matrix. If in each of these subdevices we connect each of the $m$ wires to at most one of the other $2n$ wires we will induce no sneak paths, since this is equivalent to having at most one 1 in each row of $A$. We also respect the partitioning, since each of the $2n$ wires is in a different partition (or disconnected). There are $(2n + 1)^m$ ways of making these connections in each subdevice, for a total of $(2n + 1)^{\ell m/2}$ possible patterns in the device. Now suppose we isolate and tile our devices as before, introducing diodes of size $\delta$ on all wires connecting the tiled devices. This means we add $\frac{\ell}{2}(m+n)$ diodes per tiled device. Taking logarithms in Theorems 27 and 28 and dividing by the array area, $A_{\delta, \text{arr}}(m, n) := mn + \frac{\ell}{2} \delta(m + n)$ gives the following corollaries.
Corollary 29: The number of bits \( B_\ell(m,n) := \log T_\ell(m,n) \) that can be stored in an \( n \times m \times n \times \cdots \times n \) array with an even number of layers \( \ell \) and dimensions satisfying (14) satisfies
\[
\frac{\ell}{2} m \log(2n+1) \leq B_\ell(m,n) \leq \log \left( \frac{3^\ell(n-1)^{\ell/2-1}(n+1)^\ell}{(2n+1)^2} \right) + \frac{\ell}{2} (m+1) \log(2n+1).
\]

Corollary 30: The array bit density \( \rho_{\delta,\text{arr}}^\ell(m,n) \) of an \( (m,n) \) array with dimensions satisfying (14) and \( \ell \) even satisfies
\[
\frac{\ell}{2} m \log(2n+1) \leq \rho_{\delta,\text{arr}}^\ell(m,n) \leq \log \left( \frac{3^\ell(n-1)^{\ell/2-1}(n+1)^\ell}{(2n+1)^2} \right) + \frac{\ell}{2} (m+1) \log(2n+1).
\]

Taking \( m \rightarrow \infty \) gives the following result.

Corollary 31: For \( \ell \) even and \( n \) fixed, letting \( m \rightarrow \infty \), the array bit density of an \((m,n)\) device converges to \( \rho_{\delta,\text{arr}}^\ell(n) := \left( \frac{n + \frac{\ell}{2} \delta}{m + \frac{\ell}{2} \delta} \right)^{\ell} \log(2n+1) \).

This is the result when \( \ell \) is even, and we have an array of dimensions \( n \times m \times \cdots \times n \). If \( \ell \) remains even, but the device has dimensions \( m \times n \times m \cdots m \), the asymptotic bit density is \( (n + \frac{\ell}{2} \delta)^{-1} \log(2n+1) + 2 \log(n+1) \), while if \( \ell \) is odd, the asymptotic bit density is \( (n + \frac{\ell}{2} (\ell+1) \delta)^{-1} \left[ \log(2n+1) + \log(n+1) \right] \).

Corollary 31 shows that we can write the multi-layer asymptotic bit density in terms of the single layer density for an \((m,n)\) device with \( \ell \) even. In particular, \( P_{\delta,\text{arr}}^\ell(n) = \ell T_{\ell,\ell}^\ell(2n) \). This is reasonable, since we are effectively stacking \( 2n \times m \) devices in a total of \( \ell \) layers, each of which still has diodes of size \( \delta \). This also means that we may use the same methods as in the single-layer case to find the value \( n^* \) that maximizes the density.

The density \( P_{\delta,\text{arr}}^\ell(n) \) is an increasing function of \( \ell \), but its derivative is decreasing. This means that while adding more layers will always increase the information density, it will do so less and less efficiently as the layers are added (since the isolating diodes will still take up area on the lowest level in this model). This means that a designer should choose \( \ell \) by considering what fraction of the supremal density they consider acceptable, according to the following theorem.

Theorem 32: The density \( P_{\delta,\text{arr}}^\ell(n) \) satisfies
\[
\frac{\log(2n+1)}{n+\delta} \leq P_{\delta,\text{arr}}^\ell(n) < \frac{\log(2n+1)}{\delta}
\]
for fixed \( n \) and \( \delta \), and for any positive even value of \( \ell \). Furthermore, a density of at least \((1-\epsilon)\delta^{-1} \log(2n+1)\) is obtained by any choice of \( \ell \) satisfying \( \ell \geq \frac{2}{(\epsilon^2-1) n \delta} \) when \( 0 < \epsilon \leq 1 \).

Proof: Since \( P_{\delta,\text{arr}}^\ell(n) \) is an increasing function of \( \ell \), we may substitute \( \ell = 2 \) to obtain the lower bound in (15) and take \( \ell \to \infty \) to obtain the upper bound. Solving \( P_{\delta,\text{arr}}^\ell(n) \leq (1-\epsilon) \frac{\log(2n+1)}{\delta} \) for \( \ell \) completes the proof.

Note that the device area must be at least \( A_{\gamma,\delta,\gamma}^{\ell}(1,1,m,n) \) to fit at least one array of size \( m \times n \), plus the \( \frac{\ell}{2} (m+n) \) diodes and the peripheral circuitry. In practice, when choosing array dimensions and numbers of layers, there may be further concerns about power dissipation or the vertical size of the device, which are beyond the scope of the present model. Note that if it is possible to stack the diodes along with the memristors, the density increases without bound as more layers are added in the limit of large \( m \) and \( N \).

We plot the multi-layer equivalent of Figure 6 in Figure 8. This plot includes the single-layer expression, as well as the \( \ell = 2 \) and \( \ell = 10 \) cases. Note that \( n^* \) is smaller for \( \ell = 2 \) than for \( \ell = 1 \), which is a result of the differences mentioned above between odd and even \( \ell \).

We can make similar arguments regarding peripheral circuitry in the multi-layer case to the single-layer case. Define the device area
\[
A_{\gamma,\delta,\gamma}^{\ell}(M,N,m,n) := MN[mn + \frac{\ell}{2} \delta(m+n)] + \gamma[M\frac{\ell}{2} m \log M + N\frac{\ell}{2} n \log N] - \frac{\ell}{2} \delta(m+n)
\]
and the device information density
\[
\rho_{\gamma,\delta,\gamma}^{\ell}(M,N,m,n) := \frac{MN B_\ell(m,n)}{A_{\gamma,\delta,\gamma}^{\ell}(M,N,m,n)}
\]
where \( M \), \( N \), and \( \gamma \) are defined as in the single-layer case. We can then state the following theorem.

Theorem 33: If \( m \to \infty \) and \( N \to \infty \) such that \( (\log M)/N \to 0 \) and \( (\log N)/m \to 0 \) with \( M \) and \( N \) fixed, then \( \rho_{\gamma,\delta,\gamma}^{\ell}(M,N,m,n) \to \frac{P_{\delta,\text{arr}}^\ell(n)}{n^\ell} \).

The proof is very similar to that of the single-layer case, and is omitted.

Note that taking a limit gives us an asymptotic expression for \( T_\ell(m,n) \) for fixed \( n \) and \( m \to \infty \).

Theorem 34: For any fixed \( n \) and even \( \ell \), we have
\[
\lim_{m \to \infty} \frac{T_\ell(m,n)}{(2n+1)^{\ell m/2}} = 1
\]
and this limit is approached from above.
Proof: The proof of this theorem is largely similar to that of Theorem 23 and is omitted. The relevant observation is that by an analogous series of substitutions for the Stirling numbers of the form \( \sum_{k_{2i+1}}^{m+1} T_k(m, n) = (2n+1)^{m/2} + \mathcal{O}(2n)^{m/2} \).

V. Encoding Schemes

Now that we have seen how the information capacity of a resistive array scales asymptotically, we propose encoding and decoding schemes for storing and retrieving data that achieve this asymptotic capacity. Our encoding and decoding schemes will make use of the following functions.

Definition 35 (Binary conversion function): Given a binary vector \( \{x_0, \ldots, x_{k-1}\} \in \{0, 1\}^k \), define the binary conversion function \( \phi_k : \{0, 1\}^k \rightarrow \{0, 1, \ldots, 2^k - 1\} \) by

\[
\phi_k(x_0, \ldots, x_{k-1}) = \sum_{i=0}^{k-1} x_i 2^i
\]

the value of the vector considered as a binary integer.

Note that \( \phi_k \) has a unique inverse.

Definition 36 (High-bit set): The \( i \)th high-bit set of \( k \)-bit numbers is

\[
\Delta_k(i) = \{ j | \phi_k^{-1}(j)_i = 1, 0 \leq j < 2^k \},
\]

the set of all numbers that can be represented with \( k \) bits, and whose \( i \)th bit is 1 in this representation.

A. Single-layer One-Hot Encoding Scheme

To study questions of density, we need to consider a particular coding scheme. The “at-most-one-hot” scheme that we will study is a simplification of the scheme in [8]. In this scheme we encode \( n_0 \log(n_1 + 1) \) bits into an \( n_0 \times n_1 \) array, where \( n_1 + 1 \) is chosen to be a power of 2. We will encode into a single tile of this size. In practice, many such devices will be tiled, as in Figure 5, but we will encode and decode into each in isolation.

The data we will encode is \( \{r_0, r_1, \ldots, r_{n_0-1}\} \), where \( r_i \in \{0, 1\} \log(n_1+1) \) for each \( i \) (this contains \( n_0 \log(n_1 + 1) \) bits of information). Label the row nodes (wires) \( R_0 \) to \( R_{n_0-1} \) and the column nodes \( C_0 \) to \( C_{n_1-1} \). Then we encode the data into an \( n_0 \times n_1 \) array as follows.

1) Set all array elements to the high resistance state.
2) Set the device at \( (R_i, C_{\phi_k^{\log(n_1+1)}(r_i)}) \) to the low resistance state if \( \phi_k^{\log(n_1+1)}(r_i) < n_1 \) for each \( i \) from 0 to \( n_0 - 1 \).

That is, row \( i \) contains a either a low resistance whose index corresponds to \( r_i \) considered as a binary number, as in pulse-position modulation, or it contains only high resistances (when \( \phi_k^{\log(n_1+1)}(r_i) = n_1 \)). As mentioned in the proof of Theorem 19 having at most one in each row of the array state matrix guarantees that there are no sneak paths.

We decode as follows. To find \( r_i^j \), the \( j \)th bit of \( r_i \), we make the measurement

\[
r_i^j = \mathcal{M}_G(\{R_i\}, \{C_p | p \in \Delta_k^{\log(n_1+1)}(j)\}).
\]

This gives us one bit per measurement.

This is a simpler version of the scheme proposed in [8]. The full scheme is described in Appendix C. Our simplification is motivated by the fact that while the existing scheme achieves capacity asymptotically for arbitrary aspect ratios, it involves more complicated encoding and decoding, and does not allow for unique decoding of all data patterns.

When writing, if the pattern to be overwritten is known a priori, overwriting involves only changing those elements corresponding to the ones in the old and new positions. If the existing pattern is not known or the data is being initialized, the new pattern will be written in \( k \) write operations corresponding to one row of \( n_0 \) array elements.

Note that writing is significantly more efficient when the data is known, since we need only change the old and new “hot” elements, rather than a whole row. In contexts where read speed is a priority we may want first to read the current pattern and then to write, as this will take \( k = \log(n_1 + 1) \) read and at most 2 write operations, instead of \( 2^k = n_1 + 1 \) write operations. The choice of writing strategy will depend on the specifics of the array size, read and write times, and the relative wear on the devices of reads and writes. We leave this as a subject for future work.

B. Multi-layer Encoding Scheme

1) Setup: The exact capacity and density converge asymptotically to those of the at-most-one-hot encoding scheme for layered \( m \times 2n \) devices as described above. It is therefore natural to use such an encoding scheme for our device.

In particular, assume we have an \( \ell \)-layer device, with \( \ell \) even. For ease of encoding and decoding, we will consider a scheme that stores an integer number of bits. However, since \( 2n + 1 \) cannot be a power of 2, we cannot achieve the \( 2^\ell m \log(2n + 1) \) limit exactly. We can, however store \( \frac{1}{2}m \log(2n) \) bits, as will be described below. The ratio between this value and the asymptotic value \( \frac{1}{2}m \log(2n + 1) \) is smallest at \( n = 1 \), where it is approximately equal to 0.63, and rapidly increases to an asymptotic value of 1 as \( n \) increases (reaching 0.9 at \( n \approx 2.5 \), for instance), so this is not a large loss.

If we take \( 2n = 2^N \) for some integer \( N \), the choice of \( N \) which maximizes \( P^\ell_{\delta} \) (\( n \)), which we will call \( N^* \), will depend on \( \delta \). For an \( (n, m) \) \( \ell \)-device we can store \( \frac{1}{2}mN \) bits per tiled \( n \times m \times \cdots \times n \) device, with an asymptotic density of \( P^\ell_{\delta} (N) := \ell N/(2^N + \ell \delta \)). The following theorem will help develop a relationship between \( N^* \) and \( \delta \) by finding values of \( N \) where \( P \) is increasing.

Theorem 37: If \( \ell \) is even, \( P^\ell_{\delta} (N) \) is increasing in \( N \) when \( \ell \delta \geq (N - 1)/2^N \).

The proof is the result of a simple substitution into the expression for \( P \), and is omitted. From this theorem we obtain the following corollary.

Corollary 38: If integer \( N \) has the largest value such that \( \ell \delta \geq (N - 1)/2^N \), with \( \delta \) a fixed positive number and \( \ell \) a fixed even number, then \( N \) maximizes \( P^\ell_{\delta} \).

Optimal choices of \( N \) over a range of values of \( \ell \delta \) are given in Table 4.2

\[2\] The mechanism for changing a memristor’s state varies with the technology, but typically involves applying a large voltage to the device. See [4] for a discussion of some of the alternatives.
2) Encoding scheme: We can now describe the encoding scheme for a device with even \( \ell \) and dimensions \( n \times m \times \cdots \times n \). Similar schemes can be derived for odd \( \ell \) or dimensions \( n \times n \times \cdots \times m \).

We can think of our device as \( \frac{\ell}{2} \) two-layer subdevices of size \( n \times m \times n \). Assign each of these subdevices a unique index \( i \) with \( 0 \leq i < \ell/2 \).

The data we will encode is \( \{r_{i,j}\} \), where \( 0 \leq i \leq \ell/2 \) and \( 0 \leq j < m \), with each \( r_{i,j} \in \{0,1\}^{\log(2n)} \), for a total of \( \frac{\ell}{2} m \log(2n) \) bits. We encode as follows.

1) Set all array elements to the high-resistance state.
2) Consider subdevice \( i \). Label the \( m \) row wires from \( R_0 \) to \( R_{m-1} \) and the \( 2n \) column wires from \( C_0 \) to \( C_{2n-1} \). For \( j = 0, \ldots, m-1 \), set the device at \( (R_j, C_{\phi_{m\log(2n)}(i,j)}) \) to the low-resistance state.
3) Repeat for all values of \( i \).

To decode the bit in \( r_{i,j}^u \), the \( u \)th bit of \( r_{i,j} \), perform the following operations.

1) Consider subdevice \( i \). Label the \( m \) row wires from \( R_0 \) to \( R_{m-1} \) and the \( 2n \) column wires from \( C_0 \) to \( C_{2n-1} \) in the same order as when encoding.
2) Evaluate the measurement

\[
\mathcal{M}_G(\{R_j\}, \{C_p | p \in \Delta_{\log 2n}(u)\})
\]

with \( \Delta \) defined as in Definition 36 and \( G \) the connectedness graph corresponding to the device. This is the desired bit.

This decoding scheme requires one measurement per bit extracted. An example dot-graph for a device using this scheme with \( m = 8 \), \( n = 4 \), and \( \ell = 4 \) is shown in Figure 9.

Note that each wire in the layers of \( m \) wires is attached to exactly one wire in the adjacent layers of \( n \) wires.

### APPENDIX A

#### PROOF OF THEOREM 18

We introduce the following lemmas concerning bounds on sums of log-concave sequences, to help us to bound \( T_1(n_0, n_1) \). The following standard definition will be useful to this analysis (see, e.g., [18]).

**Definition 39 (Log-concave sequence):** A sequence \( f(k) \) is called log-concavically concave (or “log-concavely”) if it satisfies \( f^2(k) \geq f(k-1)f(k+1) \) for all integers \( k \geq 1 \).

We will use this definition in the following lemma.

**Lemma 40:** If \( f \) is a positive log-concave sequence defined over integers between 0 and \( n \), where \( n \) is a non-negative integer such that \( f(n) > f(n - 1) \), then

\[
(n + 1)f(n) \geq \sum_{i=0}^{n} f(i).
\]

**Proof:** Since the summand \( f(i) \) is log-concave, it has exactly one global maximum. Since \( f(n) > f(n - 1) \), the maximum must be at \( i = n \), so we may bound each term by the \( i = n \) term, which gives the desired result.
Note that this is usually not a tight bound, since we are bounding each term by the maximum. We will more often use this lemma in the following form.

**Lemma 41:** If $f$ and $g$ are positive log-concave sequences defined over integers between 0 and $n$, with $f(n) > f(n-1)$, and there exists an integer $m$ such that

$$m \geq \log_{1 + \frac{n}{m+1}} \frac{g(n-1)}{g(n)}$$

then

$$(n+1)g(n)f(m) \geq \sum_{i=0}^{n} g(i)f(i)^m.$$  

**Proof:** If $f$ and $g$ are log-concave, and $m$ is a positive constant, then $g(f)^m$ is also log-concave, by application of the definition. By Lemma 40 (17) holds if

$$g(n) f(m)^m \geq (n-1)f(n-1)^m$$

which is equivalent to (16).

The following lemma is useful for deriving bounds on information density for devices with extreme aspect ratios.

**Lemma 42:** For integers $n$ and $k$ with $n > k$, $\{k\} \leq k^n/k!$.

**Proof:** The expression $k^n/k!$ is the number of mappings from $[n] := \{1, 2, \ldots, n\}$ to $[k] := \{1, 2, \ldots, k\}$, where relabelings of the range correspond to the same mapping. The partitions of $[n]$ into $k$ parts correspond to a subset of size $\binom{n}{k}$ of these mappings, specifically those mappings whose image is the codomain $[k]^k$.

We may now restate and prove Theorem 18

**Theorem 18** If positive integers $n_0$ and $n_1$ satisfy

$$n_0 \geq \log_{1 + \frac{n_1}{n_1}} \frac{n_1(n_1 + 1)}{2}$$

then $T_1(n_0, n_1) \leq (n_1 + 1)^{n_0 + 1}$.

**Proof:** Use Lemma 42 to write

$$T_1(n_0, n_1) = \sum_{k=0}^{n_1} \binom{n_1}{k} \binom{k}{k+1} \binom{n_0}{k+1} k!$$

$$\leq \sum_{k=0}^{n_1} \binom{n_1}{k} \binom{k}{k+1} (k+1)^{n_0}.$$

Since $\binom{n_1}{k+1}$ is log-convex in $k$ [19], we may take $g(k) = \binom{n_1}{k+1}$ and $f(k) = k+1$ in Lemma 41 which we may apply when (18) holds. This gives $T_1(n_0, n_1) \leq (n_1 + 1)^{n_0 + 1}$ as desired.

**APPENDIX B**

**PROOF OF THEOREM 27**

**Theorem 27** If positive integers $m$ and $n$ satisfy

$$m \geq \log_{1 + \frac{n}{m+1}} \frac{n^3}{2^2},$$

and $\ell$ is a positive even integer, then

$$T_\ell(m, n) \leq \frac{3^n(\beta_n - \ell)^{\ell/2-1}(n+1)^\ell}{(2n+1)^2} (2n+1)^{\ell(m+1)/2}$$

where $\beta_n := \left(\frac{0.792(n+1)}{n(n+2)}\right)^{n+1}$.

**Proof:** By Corollary 11

$$T_\ell(m, n) = \sum_{s_1=0}^{n_0} \cdots \sum_{s_{\ell}+1=0}^{n_0} \prod_{i=0}^{\ell/2-1} s_{2i+1}! s_{2i+2}!$$

$$\sum_{k_{2i+1}=\max(s_{2i+1}, s_{2i+2})}^{n} \tilde{Q}_m(k_{2i+1}, s_{2i+1}, s_{2i+2})$$

$$= \sum_{i=0}^{\ell/2-1} \min(n, s_{2i+1}, s_{2i+1}) \tilde{Q}_m(k_{2i}, s_{2i}, s_{2i+1})$$

where $s_0 = s_{\ell+1} = 0$, and

$$\tilde{Q}_m(k, a, b) := \left(\begin{array}{c} k \\ a+b-k, k-a, k-b \end{array} \right) \left(\begin{array}{c} n+1 \\ k+1 \right)$$

Use Lemma 42 to bound $\sum_{k_{2i+1}=\max(s_{2i+1}, s_{2i+2})}^{n}$ and define

$$h_{s_0, s_1}(k) := (s_0 + s_1 - k)^+(k-s_1)^+(k-s_0)^+,$$

where $x^+ := \max(0, x)$. This means that

$$\tilde{Q}_m(k_{2i+1}, s_{2i+1}, s_{2i+2}) \leq \frac{(k_{2i+1} + 1)^m}{h_{s_{2i+1}, s_{2i+1}}(k_{2i+1})}.$$

We apply Lemma 41 for each $i$, with $g_i(k_{2i+1}) = k_{2i+1} + 1$ and

$$f_i(k_{2i+1}) = \left[h_{s_{2i+1}, s_{2i+1}}(k_{2i+1})\right]^{-1}.$$

The tightest of the resulting bounds in (17) is (19). This gives

$$\tilde{Q}_m(k_{2i+1}, s_{2i+1}, s_{2i+2}) \leq \frac{(k_{2i+1} + 1)^m}{h_{s_{2i+1}, s_{2i+1}}(k_{2i+1})}.$$

Substituting (21) into (20) gives

$$T_\ell(m, n) \leq \sum_{s_{2i+1}=0}^{n} \cdots \sum_{s_{2i+1}=0}^{n} \prod_{i=0}^{\ell/2-1} \left(\begin{array}{c} s_{2i+1} + s_{2i+2} + 1 \\ s_{2i+2} + 1 \right)^{m+1}$$

$$\sum_{k_{2i+1}=\max(s_{2i+1}, s_{2i+2})}^{n} \tilde{Q}_m(k_{2i}, s_{2i}, s_{2i+1})$$

Since the sums over $k_0$ and $k_\ell$ each have only one term, $\sum_{k_0} \tilde{Q}_m(k_0, s_0, s_1) \leq \sum_{s_0=0}^{n} \sum_{s_1=0}^{n} \tilde{Q}_m(k_0, s_0, s_1)$ and $\sum_{k_\ell} \tilde{Q}_m(k_\ell, s_\ell, s_{\ell+1}) \leq \sum_{s_\ell=0}^{n} \sum_{s_{\ell+1}=0}^{n} \tilde{Q}_m(k_\ell, s_\ell, s_{\ell+1})$. For the other sums over $k_{2i}$,

$$\sum_{k_{2i}=\max(s_{2i}, s_{2i+1})}^{n} \tilde{Q}_m(k_{2i}, s_{2i}, s_{2i+1}) \leq \sum_{k_{2i}=\max(s_{2i}, s_{2i+1})}^{n} 3^{k_{2i}} \left(\begin{array}{c} n+1 \\ k_{2i} + 1 \right)$$

$$\leq 3^n \sum_{k_{2i}=0}^{n} \left(\begin{array}{c} n+1 \\ k_{2i} + 1 \right) = 3^n (B_{n+1} - 1)$$
where the Bell number \( B_n := \sum_{k=0}^{n} \frac{n!}{k!(n-k)!} \) and we have used 
\[ \sum_{a,b,c} \binom{x}{a,b,c} = 3^x \] to bound the trinomial coefficients.

Substituting into (22) gives
\[
T_\ell(m, n) \leq \left[ \left( \frac{n}{2} \right)^{\ell/2} - 1 \right]^{(n+1)\ell} \left( \frac{n}{2} + 1 \right)^{\ell(m+1)/2},
\]
which the bounds from (16) are all dominated by the bound in (19).

Using (20) Theorem 2.1, we bound \( B_{n+1} \) by \( \beta_n \), giving
\[
T_\ell(m, n) \leq \left[ \left( \frac{n}{2} \right)^{\ell/2} - 1 \right]^{(n+1)\ell} \left( \frac{n}{2} + 1 \right)^{\ell(m+1)/2}
\]
as desired.

**APPENDIX C**

**COMMENTS ON AN EXISTING ENCODING SCHEME**

In (8), the following single-layer encoding scheme is proposed. Given a device of size \( n_0 \times n_1 \) with array state matrix \( A \), select parameter \( \lambda \) to be a power of 2 with \( 0 \leq \lambda < n_1 \). The data is vectors \( \{ r_0, \ldots, r_{n_0-1}, c_0, \ldots, c_{n_1-1} \} \), where \( r_i, c_j \in \{0, 1\}^{\log_2 \lambda} \) for each \( i \) and \( j \). Let \( A_{i,j} \) denote the \( i \)th column of \( A \). Then we encode as follows:

1. Set all \( A_{i,j} \) to 0.
2. For \( i = 0, \ldots, n_0 - 1 \), set \( A_{i, \phi_{\log_2 \lambda}(r_i)} = 1 \).
3. For \( j = 0, \ldots, n_1 - 1 \), set \( A_{i, j} = A_{i, \phi_{\log_2 \lambda}(c_j)} \).

This scheme encodes \( (n_0 + n_1) \lambda \log \lambda \) bits. If we choose \( \lambda \) to be the power of 2 closest to \( (n_0 + n_1) / \log(n_0 + n_1) \), this number of bits approaches capacity asymptotically [8]. This encoding scheme can result in collisions, however, as will be seen in the following example. In addition, multiple measurements are required to decode each of the \( c_j \)s, which complicates decoding.

**Example 4:** Consider the case where \( n_0 = 3, n_1 = 7, \) and \( \lambda = 4 \), and we want to encode the data from row “Data 0” of Table II. This data is encoded into the following array state matrix:
\[
\begin{bmatrix}
1 & 0 & 0 & 0 & 0 & 1 & 0 \\
0 & 1 & 0 & 0 & 1 & 0 & 0 \\
1 & 0 & 0 & 0 & 1 & 0 & 1
\end{bmatrix}
\]

If, instead, we encode the distinct information in row “Data 1” of Table II the same array state matrix is obtained, so we cannot decode uniquely.

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