IMPLEMENTATION OF ELECTRONIC DEVICES OF CMOS FULL ADDER IN LOW POWER VLSI CIRCUITS

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Abstract. Battery-powered devices (for example, mobile phones, digital personal aids, etc) are increasing on the mobile electronic systems market by developing microelectronic circuits with low energy dissipation. The problem of dissipating power could limit the flexibility of the computer system, as the chip's density and complexity keep on increasing. The power supply consumes approximately 35% of the chip power, particularly at the nanometer level. The purpose of this project is to investigate the efficiency of one of the most reliable low power concepts called Power Gating. It is only nanometer-scale CMOS devices that are the most common technology in existing VLSI systems. Leakage power has become an integral component of total power in the nanometer technology regime. The ALU’s basic feature unit is Full Adder. The electricity consumption of an ALU is decreased by decreasing the energy consumption of an ALU, and an ALU will reduce the power consumption by decreasing the total power consumption. So these days, the complete adder designs are becoming more common with low power characteristics. The proposed project shows the concept of the micro wind tool for low power less transistors.

1. Introduction
The design and implementation of optimum sleep transistors are important for an effective power generation design. The sleep transistor architecture is subject to special considerations. Few of them optimise field, leakage and efficiencies with sleep transistor gate duration, width, and body bias. Sleep transistors are used in the power gating as switches to turn off power in standby mode for parts of a design. PMOS is used to monitor the supply of the Vdd to the header switch. PMOS is not as leaky as the NMOS transistor of the same size. The downside of the header switch is to decrease the performance of the PMOS drive to the same degree as NMOS. The implementation of the header switch typically uses more area than the implementation of a footer switch. The footer switch is supplied to control VSS by an NMOS transistor.

The low power VLSI design is significant due to portable electronic products. Reducing threshold voltage and reducing supply voltages are an effective way of reducing power consumption. Adders are the building blocks in arithmetic operations such multiplication, division, subtraction, memory address calculation, Processors and DSP design. Since full adder is the key binary adders block. By improving the performance of full adder, the performance of digital circuits is improved; researchers are highly
interested. The various techniques have been reported and they all concentrated on reducing the area, power dissipation and delay. The transistor count of an adder will largely affect the complexity of many designs like ALU, multiplier and processors. The area and complexity can be reduced by reducing the transistor count. The speed depends on transistor size, delay in the critical path and parasitic capacitance.

![Figure 1: A Power Gating Structure.](image1)

![Figure 2: A DSTN Structure](image2)

The footer switch has the advantage of high drive and therefore smaller area. NMOS, however, is leaking and is more sensitive to ground noise than PMOS. NMOS is more sensitive. An example is given in Figures 1 and 2 for the sleep transistor and distributed sleep transistor network.

ADDER: Digital circuits are adders that add numbers. Adders are a central element of the Logic device Arithmetic. For most numerical representations, adders like Binary Coded Decimal (BCD), Excess – 3, Gray Code, Binary etc. can be constructed, binary add-ons is the most common role among most common add-ons. In addition, adders are used to measure table indexes and addresses in some digital applications.

2. Literature Review

Eitan N. Shauly, (2012), [1], For the past 45, transistor density increases, which driven the CMOS technology. Nevertheless, the energy consumption and leakage of the transistors are increasingly increasing, so that some "classical" scaling laws such as door oxide dilution cannot be preserved again. The increased transistor count per chip and the reduction in dietary lead to a rapid increase in power. Since with each new generation the system clock rate has been higher but the power supply has not been decreased by the same ratio, dynamic power is now the dominant power factor for platforms with 65 nm. Foundries provide platforms with many innovations to solve this issue in most cases. The various "technologies" apply to the parameters and voltage of the thin-oxide transistors by application. In certain cases, FEOL technology would have SL (Standard Logic for General Proposes) with a thinner thickness of gate oxide, reduced voltage, higher drive currents and lower threshold voltages (LP).

Hina malviya, et.al (2013), [2], More gates are to be implemented with Deep Sub-Micron (DSM) technology on a single chip, leading to tiny geometries. But the densities of power and total power are rising rapidly. In a variety of applications, the design of low power circuits has become important. However, a reduction in energy usage requires an interaction of time and region at various design levels.
The efficient power-sensitive design requires that engineers can implement these compromises in a precise and effective manner. Power consumption is currently an important technical issue for the deep submicron phase of the CMOS circuits.

Ankit Mitra, (2014), [3], one of the most interconnected components is a digital signal processor or a microprocessor. The optimization of the speed and power usage of the adder is an extremely computationally intensive part of a device. We developed a dynamic TSPC-based 1 bit complete adder cell for achieving high speed operating. A high threshold voltage transistor is used to reduce static power dissipation in standby mode. The circuit is designed in TSPICE simulated by the TSMC 180nm CMOS process. Average power consumption, time and delay are calculated and the efficiency of current complete adder designs is dramatically improved.

T. Vasudeva Reddy, et.al (2020), [4], The processor speed depends on the SRAM features for reading and writing. The problem that needs to be taken into account during sub-schedule operation with increasing technology leakage capacity. The leakage power that restricts activity at sub-thresholds generally means that SRAM is very large and less effective. In the circuit design, power consumption is mainly dictated by the transistor switching operation, which increases the leakage current at or under the threshold. Some of the challenges such as PVT changes, SEU, SEE and RDF have led to reduced efficiency, higher production, BTI and size. The technical problems and consequences of CMOS & FinFet designs are discussed primarily in research work in this paper. The second part of the paper is the CMOS & FinFET models concept and service. The third component deals with the design agreement of FinFET SRAM. The final components provide a contrast between high quality, low power and near threshold at normal operation.

Kavitha MANICKAM, et.al (2016),[5], In the contemporary age the use of portable battery-powered devices such as laptops and mobile telephones has increased rapidly. The life span of these devices, which has become an inspiring factor for VLSI design, limits operational life. In the past, chip designers had a significant problem with complex energy consumption, comprising about 99 percent of the total power of the chip. As transistors have been scaled in modern CMOS technology, leak power is rising huge and dynamic power is approaching. The aim of the present paper is to reduce the lack of technology in sub nanometers. The following method is proposed. The simulation results show that, compared with traditional techniques, the proposed technique decreases maximum performance by 96%, dynamic power by 33%, drowsy power by 49% and energy by 16%. Even if various operational parameters vary, the methodology suggested provides a strong leak reduction.

Farzan Fallah, et.al (2004) [6], The energy consumption leakage aspect is comparable to many modern high-performance designs' switch. It has already been recorded that 40 or more percent of total electrical consumption is responsible for the transistor leakage. With technological scaling, this percentage will increase unless successful strategies are adopted to manage leakage. To achieve this goal, this article focuses on the improvement of circuits and design automation. The first section gives an overview of general relativity and process scaling patterns which lead to an important increase in the currents of CMOS leakage. The existing leakage standby segment also separates the active components into active ones. The second section of the article discusses a variety of circuit optimization strategies, including the power gates, and body bias control, to control the standby leak current. The third part of the analysis deals with techniques for successful leakage control, including multi-threshold cell, longer-channel systems, the configuration of the input vector, transistor noise stacking and simultaneous threshold and voltage assignment.

Ayesha Firdous, et.al (2017), [7], In this new world there needs to be a strong demand of power efficiency and power-delay goods due to advances in battery-based devices with small power capacities. For electronic designers, these two considerations are a major challenge[1]. The power consumption of the circuit is also of great importance in the VLSI circuit design. Low power requirements are not due solely to the production of mobile apps[3]. The issue of energy use before the smartphone age is a big issue. Researchers have suggested various techniques and methods with respect to architectural, system level and even some higher levels to solve the power dissipation problem.
Reetu, (2018), et.al [8], The rate of dissipation, over a period of time, of energy from the source to the system is mainly called dissipation of energy. It is essentially divided into two categories: 1. Peak Power 2. Average Power Maximum instantaneous power over a period of time is called peak power, which reduces the reliability of the unit by introducing errors which render the system inadequate. Average power influences the cooling and packaging of the device. Reducing electricity consumption is an integrated circuit (VLSI) very wide-range field. The battery derives from most transportable equipment available on the market. Nowadays, low-power architectures are challenging.

T. Tharaneeswaran, et.al (2012), [9], For VLSI digital and analogue technology, CMOS has been the dominant devices. The delivery voltage of such circuits must be further decreased to retain high drives current and boost performance, in reality resulting in a significant increase in sub-threshold leakage current, which is a serious factor in power dissipation, to maintain reliability and decrease power consumption. We have developed a mixed signal system (DAC) for the test kernel since VLSI technology had both analogue and digital circuits. The Minimization Technique Circuit Level Implementations of different CSDAC bits are carried out. CMOS VLSI Technology's leakage power is very significant.

Smt. Sarita Chauhan, et.al (2015), [10], Increased power consumption is challenging the production of digital integrated circuits. The combination of higher speeds, improved functional integration and smaller process geometries led to the large increase in power density. Scaling improves transistor density and flexibility on a chip. Scaling improves operating speed and frequency and thus increases performance. New methods for this were suggested in this paper. The methods suggested will be compared to previous approaches for minimising leakage. This article includes a new technique known as the dual stack for the reduction of leakage and dynamic control.

3. CMOS Technology

The Complementary Metal–Oxide–Halbleiter (CMOS) is the integrated planning technology. CMOS technology is used in microprocessors, microcontrollers, static RAM and others. CMOS technology is commonly used in a number of analogue circuits as image sensors and data converters for many modes of communication. The symmetry of external metal, oxide–semiconductor is also called CMOS (or COS-MOS). The term 'complementary symmetry' implies the use of semi-conductive effect transistors for logical functions of the standard CMOS style for complementary and symmetric P-type and n-type metal oxide (MOSFETs). Two key features of CMOS systems are high noise immunity and low static power consumption. Only when the CMOS transistors are switched on and off between states can substantial power be drawn. As a result, waste heat produced by CMOS devices is less widespread than other logical forms, such as transistor logic (TTL) and NMOS logic. CMOS also permits high logical feature densities on a chip. This was mainly why CMOS has become the most commonly used VLSI chip technology. The term "metal–oxide–semiconductor" which in turn lies on the top of a semi-conductor Material, is a reference to the physical structure of some field-effect transistors, with the electrode on a metal gate. Once used aluminium but now poly silicon has been used. With the advent of high-end dielectric materials in the CMOS process, IBM and Intel announced for the 45-nanometer node and beyond.

3.1 Design and comparative analysis:

3.1.1 Conventional CMOS design

The P-MOS pull-up and N-MOS pull-down [1][3] are based on the standard complementary semiconductor design of metal oxide. It has the advantages of very low power dissipation, but this design requires 28 transistors, thus the silicon area is more and the complexity is more for larger designs. Due to the low mobility of P-MOS block the speed is less compared to other logic designs. The design and simulation result for conventional CMOS 28T full adder is shown in Fig 1(a), and Fig1(b).
3.1.2 Gate Diffusion Input (GDI)

The design consists of 2 XNOR gates designed by 4 transistors. The GDI full adder requires 10 transistors, which is very less compared to CMOS and the speed is more [2]. But the main drawback of GDI technique is it suffers from swing degradation due to threshold loss and it requires silicon on insulator or twin-well process to realize which is expensive to realize [7]. The GDI full adder design and simulation result is shown in the fig 2(a) and 2(b).

3.1.3 Modified GDI

P-MOS pass strong logic ‘1’ and N-MOS pass strong logic ‘0’. In order to reduce the swing degradation problem in conventional GDI, an additional N-MOS is used in parallel to PMOS with inverted gate input. This design requires 17 transistors to realize full adder. Although the transistor count is more compared to GDI technique, it will give accurate output and it has less power dissipation compared with GDI. The design and simulation for Mod GDI full adder is shown in the fig 3(a) and 3(b).
3.1.4 16T Full Adder

The 16T full adder is shown in the fig 4(a). It is the combination of pass transistor logic, transmission gates and low power XOR, XNOR gates[8]. It requires 16 transistors and the power dissipation and delay are less compared to other alternative designs. But this design suffers from swing degradation due threshold loss. The simulation result is shown in the fig 4(b).

![Fig 4(a) Full adder using 16 Transistors](image)

![Fig 4(b) Simulation result for hybrid 16T full adder](image)

4. Power Gated 4-Bit BCD Adder Design

4.1 4-BIT BCD Adder Power Gated With DSTN

Gates in a cluster are connected via virtual ground wires to the sleep transistor in the distributed network of a sleep transistor. This is called the point where inactive transistors are connected to the logical gates. We can construct the DSTN structure by adding more wires to form a mesh that contains all virtual ground wires.

Two sleep transistors are installed while designing the DSTN of the BCD adder for each complete adder track. One for the sum circuit and one for the system of transport. A single cluster is created by the sleep transistor in each whole adder. The sleep transistors in every cluster are linked by a single line called the 'Virtual Field.' By an external sleep signal, the virtual ground line is excited. The BCD adder schematic is shown in the diagram, which is built with the power gate design of DSTN.

![Figure 5: 4-bit bcd adder power gated with dst.](image)
4.2 4-BIT BCD Adder with Clock Gated Power Gating

In the gated clock power transmission structure, an internal clock signal is used to move sleep transistors on the BCD circuit. The frequency of the clock depends partly on the average time it takes. Your clock speed is preset by the intermediate spread rate among the circuit clusters. The speed is defined. Figure 6 demonstrates a clock gated power gate BCD adder scheme. The above circuits are 65nm in scale. The sleeve transistors used have a W L ratio higher than the BCD adder.

Figure 6: 4-bit bcd adder with clock gated power gating

5. Conclusion

The reversible logic circuits are designed to reduce the power dispersion, which eventually increases the circuit's life and speed. The researchers are attracted by reversible logic, which has huge applications in emerging technologies. In this paper we have presented efficient reversible BCD adder designs that primarily optimize quantity cost and power dissipation parameters. The current method requires 61 quantum costs and 5 674 W of power dissipation, but the quantum costs and power dissipation parameters have been reduced in our proposed work. We conclude that it can be extremely advantageous to use special reversible gates to reduce the power dissipation and the quantum cost of the circuit for a particular combining function.

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