Separation of concerning things: a simpler basis for defining and programming with the C/C++ memory model (extended version)

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The C/C++ memory model provides an interface and execution model for programmers of concurrent (shared-variable) code. It provides a range of mechanisms that abstract from underlying hardware memory models – that govern how multicore architectures handle concurrent accesses to main memory – as well as abstracting from compiler transformations. The C standard describes the memory model in terms of cross-thread relationships between events, and has been influenced by several research works that are similarly based. In this paper we provide a thread-local definition of the fundamental principles of the C memory model, which, for concise concurrent code, serves as a basis for relatively straightforward reasoning about the effects of the C ordering mechanisms. We argue that this definition is more practical from a programming perspective and is amenable to analysis by already established techniques for concurrent code. The key aspect is that the memory model definition is separate to other considerations of a rich programming language such as C, in particular, expression evaluation and optimisations, though we show how to reason about those considerations in the presence of C concurrency. A major simplification of our framework compared to the description in the C standard and related work in the literature is separating out considerations around the "lack of multicopy atomicity", a concept that is in any case irrelevant to developers of code for x86, Arm, RISC-V or SPARC architectures. We show how the framework is convenient for reasoning about well-structured code, and for formally addressing unintuitive behaviours such as "out-of-thin-air" writes.

1 INTRODUCTION

C/C++ is one of the most widely used programming languages, including for low-level concurrent code with a high imperative for efficiency. The C (weak) memory model, governed by an ISO standard, provides an interface (atomics.h) for instrumenting shared-variable concurrency that abstracts from the multitude of multicore architectures it may be compiled to, each with its own guarantees and mechanisms for controlling accesses to shared variables.

The C memory model standard is described in terms of a cross-thread “happens before” relationship, relating stores and loads within and between threads, and “release sequences”. The fundamentals of this approach were established by Boehm & Adve [6], and the standard has been influenced and improved by various research works (e.g., [5, 77]). However, because it is cross-thread, verification techniques are often complex to apply, and the resulting formal semantics are often highly specialised and involve global data structures capturing a partial order on events, and rarely cover the full range of features available in C’s atomics.h [8, 46]. In many cases this is because such formalisms attempt to explain how reordering can occur by mixing considerations such as expression optimisations and Power’s cache coherence system, alongside local compiler-induced and processor pipeline reorderings. We instead take a separation-of-concerns approach, where the three fundamental principles involved in C concurrent code – data dependencies, fences, and memory ordering constraints – are specified separately to other aspects of C which may complicate reasoning, such as expression evaluation, expression optimisations, and arbitrary compiler transformations. Provided a programmer steers clear of concurrent code that is subject to these
extra factors, reasoning about their code is relatively straightforward in our framework, but if the full richness of C is insisted upon, our framework is also applicable.

Syntactically and semantically the key aspect is the *parallelized sequential composition* operator, formalising a processor-pipeline concept that has been around since the 1960s, and which has been previously shown to have good explanatory power for most behaviours observed on hardware weak memory models [11, 12]. Reasoning in this setting involves making explicit at the program level what effects the memory model has, either reducing to a sequential form where the use of *atomics.h* features prevents the compiler or hardware from making problematic reorderings, or making the residual parallelism explicit; in either case, standard techniques (such as Owicki-Gries or rely/guarantee) apply to the reduced program. We cover a significant portion of the C weak memory model, including release/acquire and release/consume synchronisation, and sequentially consistent accesses and fences. We demonstrate verification of some simple behaviours (litmus tests), a spin lock implementation, and also explain how two types of related problematic behaviours – out-of-thin-air stores and read-from-untaken-branch – can be analysed and addressed. We argue that this foundation provides a simpler and more direct basis for discussion of the consequences of choices within the C memory model, and in particular for analysing the soundness of compiler transformations for concurrent code.

We explain the main aspects of the C memory model using a simple list-of-instructions language in Sect. 2, covering all relevant aspects of the C memory model’s principles. We then give the syntax and semantics of a more realistic imperative language (with conditionals and loops) in Sect. 3. We give a set of reduction rules for reasoning about the effects of the memory model in Sect. 4, and explain how standard reasoning techniques can be applied in Sect. 5. We show some illustrative examples in Sect. 6, including the often-discussed “out-of-thin-air” behaviours, showing how in our framework an allowed version of the pattern arises naturally, and a disallowed version is similarly disallowed. In Sections 7, 8, and 9 we extend the language of Sect. 3 with other features of programming in C such as incremental (usually called non-atomic) expression evaluation and instruction execution, expression optimisations, and forwarding of values from earlier instructions to later ones. Crucially, despite the complexities these features introduce, the fundamental principles of the C memory model from Sect. 2 do not change. In Sect. 10 we give a formal discussion of the “read-from-untaken branch behaviour” which exposes the often problematic interactions between standard compiler optimisations and controlling shared-variable concurrency.

## 2 A SIMPLE LANGUAGE WITH THREAD-LOCAL REORDERING

In this section we give a simple language formed from primitive actions and “parallelized sequential prefixing”, which serves to explain the crucial parts of reordering due to the C memory model. In Sect. 3 we extend the language to include standard imperative constructs such as conditionals, loops, and composite actions.

### 2.1 Syntax and semantics of a language with instruction reordering

To focus on the semantic point of reorderings we introduce a very basic language formed from primitive instructions representing assignments, branches, and fences, which are composed solely by a prefix operator that allows reordering (early execution) of later instructions.

\[
\begin{align*}
e & ::= v \mid x \mid e \mid e_1 \oplus e_2 \\
f & ::= \text{store}_{\text{fnc}} \mid \text{load}_{\text{fnc}} \mid \text{full}_{\text{fnc}} \mid \ldots \\
\alpha & ::= x := e \mid \{e\} \mid f \\
c & ::= \text{nil} \mid \alpha \rightarrow c
\end{align*}
\]
Expressions $e$ can be base values $v$, variables $x$, or involve the usual unary ($\ominus$) or binary ($\oplus$) operators. A primitive action $\alpha$ in this language is either an assignment $x := e$, where $x$ is a variable and $e$ an expression, guard $\langle e \rangle$, where $e$ is an expression, or fence $f$, where $f$ is some fence type, described below. A command can be the terminated command $\text{nil}$, or a simple prefixing of a primitive instruction $\alpha$ before command $c$, parameterised by some memory model $\mathbb{M}$, written $\alpha \triangleright_c \mathbb{M} \ c$. As we show elsewhere [11, 12, 14], the parameter $\mathbb{M}$ can be instantiated to give the behaviour of hardware weak memory models, but in this paper we focus mostly on C’s memory model, denoted formally by ‘c’, and the special cases of sequential and parallel composition. The $\triangleright$ operator essentially allows the construction of a sequence of instructions that may be reordered under some circumstances, similar to a hardware pipeline.

The semantics of the language is given operationally below. All primitive actions are executed in a single indivisible step.\footnote{Normally called atomic but we avoid that term to keep the notion separate from C’s notion of atomics.}

\[
\begin{array}{ll}
(i) & \alpha \triangleright_c \mathbb{M} \ c \rightarrow c \\
(ii) & \frac{c \xrightarrow{\beta} c' \quad \alpha \triangleleft \mathbb{M} \triangleright_c \mathbb{M} \ c' }{\alpha \triangleright_c \mathbb{M} \ c \rightarrow c' } \\
\end{array}
\]

A command $\alpha \triangleright_c \mathbb{M} \ c$ may either immediately execute $\alpha$, (rule (i)) or it may execute some action $\beta$ of $c$ provided that $\beta$ may reorder with $\alpha$ with respect to $\mathbb{M}$, written $\alpha \triangleleft \mathbb{M} \beta$ (rule (ii)). The conditions under which reordering may occur are specific to the memory model under consideration, and we define these below for C. The memory model parameter is defined pointwise on instruction types. This is a relatively convenient way to express reorderings, especially as it is agnostic about global traces and behaviours. As shown empirically in [12] it is suitable for explaining observed behaviours on architectures such as Arm, x86 and RISC-V. It specialises to the notions of sequential and parallel conjunction straightforwardly.

As an example, consider a memory model $\mathbb{M}$ such that assignments of values to different variables can be executed in either order (as on Arm, but not on x86, for instance), that is, $x := v \triangleleft \mathbb{M} y := w$ for $x \neq y$. Then we have two possible terminating traces (traces ending in $\text{nil}$) for the program $x := 1 \triangleright \mathbb{M} y := 1 \triangleright \mathbb{M} \text{nil}$.

\[
\begin{align*}
x & := 1 \triangleright \mathbb{M} y := 1 \triangleright \mathbb{M} \text{nil} \xrightarrow{x:=1} y := 1 \triangleright \mathbb{M} \text{nil} \xrightarrow{y:=1} \text{nil} \\
x & := 1 \triangleright \mathbb{M} y := 1 \triangleright \mathbb{M} \text{nil} \xrightarrow{y:=1} x := 1 \triangleright \mathbb{M} \text{nil} \xrightarrow{x:=1} \text{nil} \\
\end{align*}
\]

The first behaviour results from two applications of rule (i) above (as in prefixing in CSP [36] or CCS [54]). The second behaviour results from applying rule (ii), noting that by assumption $x := 1 \triangleleft \mathbb{M} y := 1$, and then rule (i).

We define $\text{fence} \triangleleft \mathbb{M} \alpha$ and subsequently treat it as a full fence in $\mathbb{M}$ by defining $\text{fence} \triangleleft \mathbb{M} \alpha$ and $\alpha \triangleleft \mathbb{M} \text{fence}$ for all $\alpha$ (where $\alpha \triangleleft \mathbb{M} \beta$ abbreviates $\neg(\alpha \triangleleft \mathbb{M} \beta)$). Then we have exactly one possible trace in the following circumstance. For convenience below we omit the trailing $\text{nil}$.

\[
\begin{align*}
x & := 1 \triangleright \mathbb{M} \text{fence} \triangleright \mathbb{M} \ y := 1 \xrightarrow{x:=1} \text{fence} \triangleright \mathbb{M} \ y := 1 \xrightarrow{\text{fence}} y := 1 \xrightarrow{y:=1} \text{nil} \\
\end{align*}
\]

The fence has prevented application of the second rule (since by definition both $x := 1 \triangleleft \mathbb{M} \text{fence}$ and $\text{fence} \triangleleft \mathbb{M} y := 1$) and hence restored sequential order on the instructions.

The framework admits the definition of standard sequential and parallel composition as (extreme) memory models. Let the "sequential consistency" model $\mathbb{S}$ be the model that prevents all
reordering, and introduce a special operator for that case. We define the complement of \(SC\) to be \(PAR\), i.e., the memory model that allows all reordering, which corresponds to parallel execution.

\[
\alpha \overset{SC}{\iff} \beta \iff \text{False for all } \alpha, \beta
\]

\[
\alpha \overset{PAR}{\iff} \beta \iff \text{True for all } \alpha, \beta
\]

\[
\alpha \triangleright c \iff \alpha \overset{SC}{\triangleright} c
\]

Using \(\square\) for trace equality (defined formally later),

\[
x := 1 \gg \text{fence} \gg y := 1 \quad \square \quad x := 1 \gg \text{fence} \gg y := 1
\]

Without the fence \(\alpha\) and \(\beta\) effectively execute in parallel (under \(m\)), that is,

\[
x := 1 \gg y := 1 \quad \square \quad x := 1 \parallel y := 1
\]

Whether \(x := 1 \gg y := 1\) satisfies some property depends exactly on whether the parallel execution satisfies the property.

## 2.2 Reordering in C

We now consider the specifics of reordering in the C memory model, which considers three aspects: (i) variable (data) dependencies; (ii) fences; and (iii) “memory ordering constraints”, that can be used to annotate variables or fences. We cover each of these three aspects in turn.

### 2.2.1 Data dependencies/respecting sequential semantics.

A key concept underpinning both processor pipelines and compiler transformations is that of data dependencies, where one instruction depends on a value being calculated by another. To capture this we write \(\alpha \rightsquigarrow \beta\) if instruction \(\beta\) depends on a value that instruction \(\alpha\) writes to. We define a range of foundational syntactic and semantic concepts below. In a concurrent setting we distinguish between local and shared variables, that is, the set \(Var\) is divided into two mutually exclusive and exhaustive sets Local and Shared. By convention we let \(x, y, z\) be shared variables and \(r, r_1, r_2\ldots\) be local variables. For convenience we introduce the syntax \(s_1 \triangleleft s_2\) to mean that sets \(s_1\) and \(s_2\) are mutually exclusive.

\[
s_1 \triangleleft s_2 \iff s_1 \cap s_2 = \emptyset
\]

\[
\text{Local} \cup \text{Shared} = \text{Var}
\]

\[
\text{wv}(x := e) = \{x\} \quad \text{wv}(\{e\}) = \emptyset \quad \text{wv}(f) = \emptyset
\]

\[
\text{rv}(x := e) = \text{fv}(e) \quad \text{rv}(\{e\}) = \text{fv}(e) \quad \text{rv}(f) = \emptyset
\]

\[
\text{fv}(\alpha) = \text{wv}(\alpha) \cup \text{rv}(\alpha)
\]

\[
\text{sv}(\alpha) = \text{fv}(\alpha) \cap \text{Shared} \quad \text{rsv}(\alpha) = \text{rv}(\alpha) \cap \text{Shared} \quad \text{wsv}(\alpha) = \text{wv}(\alpha) \cap \text{Shared}
\]

\[
\mathbb{S} \equiv \{\alpha \mid \text{wsv}(\alpha) \neq \emptyset\} \quad \mathbb{L} \equiv \{\alpha \mid \text{rsv}(\alpha) \neq \emptyset\}
\]

\[
\alpha \rightsquigarrow \beta \equiv \text{wv}(\alpha) \cap \text{rv}(\beta) \neq \emptyset
\]

\[
\alpha \rightsquigarrow \beta \equiv - (\alpha \rightsquigarrow \beta)
\]

\[
\text{interference_free}(\alpha, \beta) \equiv \text{wv}(\alpha) \not\cup \text{fv}(\beta) \land \text{wv}(\beta) \not\cup \text{fv}(\alpha)
\]

\[
\text{load_indep}(\alpha, \beta) \equiv \text{rsv}(\alpha) \not\cap \text{rsv}(\beta)
\]

\[
\text{order_indep}(\alpha, \beta) \equiv \text{eff}(\alpha) ; \text{eff}(\beta) = \text{eff}(\beta) ; \text{eff}(\alpha)
\]
The write variables of instructions (written \( wv(a) \)) are collected syntactically (2.8), as are the read variables (written \( rv(a) \)) (2.9), which depend on the usual notion of the free variables in an expression (written \( fv(e) \), defined straightforwardly over the syntax of expressions). The free variables of an instruction are the union of the write and read variables (2.10). Shared and local variables have different requirements from a reordering perspective and so we introduce specialisations of these concepts to just the shared variables (2.11). We define “store” instructions (\( S \)) as those that write to a shared variable, and “load” instructions (\( L \)) as those that read shared variables (and hence an instruction such as \( x := y \) is both a store and a load).

Using these definitions we can describe various relationships between actions. One of the key notions is of “data dependence”, where we write \( \alpha \rightsquigarrow \beta \) if instruction \( \beta \) references a variable being modified by instruction \( \alpha \) (2.13) (and similarly we write \( \alpha \not\rightsquigarrow \beta \) if there is no data dependence (2.14)). For instance, \( x := 1 \rightsquigarrow r := x \) but \( x := 1 \not\rightsquigarrow r := y \). The former can be expressed as \( x := 1 \) “carries a dependency into” \( r := x \). Two instructions are interference free if there is no data dependence in either direction, and they write to different variables (2.15). Note that instructions that are interference-free may still load the same variables; we say they are load independent if they access distinct shared variables (2.16). Finally, two instructions are “order independent” if the effect of executing them is independent of the execution order (2.17). The “effect” function \( eff(\alpha) \) denotes actions as a set of pairs of states in the usual imperative style (defined later in Fig. 4), using \( \upharpoonright \) for relational composition. Note that order-independence is a weaker condition than non-interference, for example, \( x := 1 \) and \( x := 1 \) are order-independent but not interference-free. All of these definitions or concepts defined for instructions can be lifted straightforwardly to commands by induction on the syntax (see Appendix A).

The key aspect of interference-freedom is the following.

**Theorem 2.1 (Disjointness).**

\[
\text{interference-free}(\alpha, \beta) \Rightarrow \text{order-independent}(\alpha, \beta)
\]

**Proof.** Straightforward: independent actions do not change each other’s outcomes. \( \square \)

We say \( \beta \) may be reordered before \( \alpha \) with respect to sequential semantics, written \( \alpha \not\Rightarrow \beta \), if they are interference-free and load-independent; the latter constraint maintains coherence of loads.

**Definition 2.2 (\( \not\Rightarrow \)).** For instruction \( \alpha, \beta \),

\[
\alpha \not\Rightarrow \beta \quad \equiv \quad \text{interference-free}(\alpha, \beta) \land \text{load-independent}(\alpha, \beta)
\]  

(2.18)

A syntactic check may be used to validate \( \alpha \not\Rightarrow \beta \). Of course one could do a semantic check to establish the weaker property of order-independence, however this is typically not done on a case-by-case basis but rather is used to justify compiler transformations. It is not feasible to check order independence directly for all cases.

We can derive the following, where we assume \( x, y \in \text{Shared}, r, r_1, r_2 \in \text{Local}, \) and all are distinct, and \( v, w \in \text{Val} \). We write \( \alpha \not\Rightarrow \beta \) if \( \neg(\alpha \not\Rightarrow \beta) \).

\[
x := v \not\Rightarrow y := w \quad \text{but} \quad x := v \not\Rightarrow x := w
\]

(2.19)

\[
x := v \not\Rightarrow r := y \quad \text{but} \quad x := v \not\Rightarrow r := x
\]

(2.20)

\footnote{This is a well-known property, the earliest example being Hoare’s disjointness [2, 34, 37], and is also called non-interference in separation logic [7]. This condition, formally discussed since the 1960’s, is remarkably powerful for explaining the majority of observed behaviours of basic instructions types on modern hardware, although this author did not find evidence of cross-over in older references ([75, 76], etc).}
\[ r_1 := x \not\in r_2 := y \quad \text{but} \quad r_1 := x \not\in r_2 := x \quad (2.21) \]
\[ x := r \not\in y := r \quad (2.22) \]
\[ (r = v) \not\in x := w \quad (2.23) \]

This shows that independent stores can be reordered, but not stores to the same variable (2.19); similarly independent stores and loads can be reordered, as can loads, provided they are not referencing the same (shared) variable ((2.20) and (2.21)). Accesses of the same local variable, however, can be reordered (2.22), since no interference is possible. Finally, stores can be reordered before (independent) guards (2.23). Since, as we show later, guards model branch points, this is a significant aspect of c. For hardware weak memory models (2.23) is not allowed, as it implies a "speculative" write that may not be valid if \( r = v \) is eventually found not to hold; however at compile-time whether a branch condition will eventually hold may be able to be predetermined.

2.2.2 Respecting fences. Since the reorderings allowed by weak memory models may be problematic for establishing communication protocols between processes such models typically have their own "fence" instruction types, which are artificial constraints on reordering (as opposed to the "natural" data-dependence constraint). C has fences specifically to establish order between stores, between loads, or between either type. We define \( \not\in \) below, relating fences and instructions.

\[
\begin{align*}
\text{Fence} & \in \text{Fence} \times \text{Instr} \\
\text{store}_{\text{fnc}} & \subseteq \alpha \iff \alpha \in S \\
\text{load}_{\text{fnc}} & \subseteq \alpha \iff \alpha \in L \\
\text{full}_{\text{fnc}} & \subseteq \alpha \quad \text{for all } \alpha
\end{align*}
\]

Eq. (2.24) states that a store fence blocks store instructions (recall (2.12)), while (2.25) similarly states that load fences block loads. Eq. (2.26) states that a "full" fence blocks all instruction types.

We use this base definition to define when two instructions can be reordered according to their respective fences (lifting the relation name \( \not\in \)).

**Definition 2.3 (Fence reorderings).**
\[
\alpha \not\in \beta \iff (\forall f \in |\alpha| \bullet f \not\in \beta) \land (\forall f \in |\beta| \bullet f \not\in \alpha)
\]

where \(|\alpha|\) extracts the fences present in \( \alpha \), i.e.,
\[
|x := e| = \emptyset \quad |(e)| = \emptyset \quad |f| = \{f\}
\]

Hence \( \alpha \) and \( \beta \) can be reordered (considering fences only) if they each respect the others’ fences. Note that all C fences are defined symmetrically so we simply check the pair in each direction.\(^3\)

Based on these definitions we can determine the following special cases, where \( x, y \in \text{Shared} \) and \( r, r_1 \in \text{Local} \).
\[
\begin{align*}
x := 1 & \not\in \text{store}_{\text{fnc}} \not\in y := 1 \quad (2.28) \\
r_1 := x & \not\in \text{load}_{\text{fnc}} \not\in r_2 := y \quad (2.29) \\
x := 1 & \not\in \text{full}_{\text{fnc}} \not\in r := y \quad (2.30)
\end{align*}
\]

Statements of the form \( \alpha \not\in \beta \not\in y \) should be read as a shorthand for \( \alpha \not\in \beta \) and \( \beta \not\in y \). Inserting fences limits the number of possible traces of a program, an outcome which obviously may restore intended relationships between variables.

\(^3\)For asymmetric fences, such as Arm’s \texttt{isb} instruction, both directions need to be specified \([12]\).
2.3 Memory ordering constraints

C introduces “atomics” in the stdatomic library, which includes several types of “memory ordering constraints” (which we herewith call ordering constraints), which can tag loads and stores of variables declared to be “atomic” (e.g., type atomic_int for a shared integer). These ordering constraints control how atomic variables interact. We start with an informal overview of how ordering constraints are intended to work, and then show how we incorporate them into the syntax of the language and define a reordering relation over them.

For the discussions below we use a more compact notation for stores and loads, as exemplified by the following C equivalents.\(^4\)

\[
\begin{align*}
r &= \text{atomic\_load\_explicit}(\&y, \text{memory\_order\_relaxed}) \equiv r := y^{RLX} \quad (2.31) \\
\text{atomic\_store\_explicit}(\&y, 3, \text{memory\_order\_seq\_cst}) &\equiv y^{SC} := 3 \quad (2.32)
\end{align*}
\]

2.3.1 Informal overview of ordering constraints. We describe the six ordering constraints defined in type memory\_order below.

- **Relaxed** (RLX, memory\_order\_relaxed). A relaxed access is the simplest, not adding any extra constraints to the variable access, allowing both the hardware and compiler to potentially reorder independent relaxed accesses. For instance, consider the following program snippet (where ‘; ’ is C’s semicolon).

\[
x^{RLX} := 1; \text{flag}^{RLX} := \text{True} \quad (2.33)
\]

If the programmer’s intention is that the flag variable is set to True after the data \(x\) is set to 1, then they have erred: either the compiler or the hardware may reorder the apparently independent stores to \(x\) and flag.

- **Release** (REL, memory\_order\_release). The release tag can be applied to stores, indicating the end of a set of shared accesses (and hence control can be “released” to the system). Typically this tag is used on the setting of a flag variable, e.g., modifying the above case,

\[
x^{RLX} := 1; \text{flag}^{REL} := \text{True} \quad (2.34)
\]

now ensures that any other process that sees \(\text{flag} = \text{True}\) knows that the update \((x^{RLX} := 1)\) preceding the change to flag has taken effect.

- **Acquire** (ACQ, memory\_order\_acquire). The acquire tag can be applied to loads, and is the reciprocal of a release: any subsequent loads will see everything the acquire can see. For example, continuing from above, a simple process that reads the flag in parallel with the above process may be written as follows:

\[
f := \text{flag}^{ACQ}; r := x^{RLX} \quad (2.35)
\]

In this case the loads are kept in order by the acquire constraint, and hence at the end of the program, in the absence of any other interference, \(f = 1 \Rightarrow r = 1\).

- **Consume** (CON, memory\_order\_consume). The consume tag is similar to, but weaker than, ACQ, in that it is intended to be partnered with a REL, but only subsequent loads that are data-dependent on the loaded value are guaranteed to see the change. Hence,

\[
f := \text{flag}^{CON}; r := x^{RLX} \quad (2.36)
\]

does not give \(f = 1 \Rightarrow r = 1\). However, after

\[
f := \text{flag}^{CON}; y := r^{RLX} \quad (2.37)
\]

\(^4\)In C++, \(r = y.\text{load}(\text{std::memory\_order\_relaxed})\) and \(y.\text{store}(3, \text{std::memory\_order\_seq\_cst})\)
then \( f = 1 \Rightarrow y = 1 \). Data-dependence is maintained by the \( \leq \) relation, and in that sense the \( \text{CON} \) constraint provides no extra reordering information to that of RLX. However the intention is that a \( \text{CON} \) load indicates to the compiler that it must not lose, via optimisations, data dependencies to later instructions. We return to \( \text{CON} \) in Sect. 8.2, in the context of expression optimisations, but for concision in the rest of the paper we omit consideration of \( \text{CON} \), which otherwise behaves as a RLX constraint.

- **Sequentially consistent** (\( \text{sc, memory\_order\_seq\_cst} \)). The sequentially consistent constraint is the strongest, forcing order between \( \text{sc} \)-tagged instructions and any other instructions. For example, the snippet

\[
x^{\text{sc}} := 1; \quad \text{flag}^{\text{sc}} := \text{True}
\]

ensures \( \text{flag} = 1 \Rightarrow x = 1 \) (in fact only one instruction needs the constraint for this to hold). This is considered a more “heavyweight” method for enforcing order than the acquire/release constraints.

- **Acquire-release** (\( \text{acqrel, memory\_order\_acq\_rel} \)). This constraint is used on instructions that have both an acquire and release component, and as will be seen it is straightforward to combine them in our syntax.

**Non-atomics.** Additionally shared data can be “non-atomic”, i.e., variables that are not declared of type \( \text{atomic\_*} \), and as such cannot be directly associated with the ordering constraints above. Programs which attempt to concurrently access shared data without any of the ordering mechanisms of \text{atomics.h} essentially have no guarantees about the behaviour, and so we ignore such programs. For programs that include shared non-atomic variables which are correctly synchronised, i.e., are associated with some ordering mechanism (e.g., barriers or acquire/release flag variables) they can be treated as if relaxed, and are subject to potential optimisations as outlined in Sect. 8. Distinguishing between correctly synchronised shared non-atomic variables is a syntactic check that compilers carry out, which could be carried over into our syntactic framework, but this is not directly relevant to the question of reorderings.

### 2.3.2 Formalising memory order constraints.

The relationship between the ordering constraints can be thought of in terms of a reordering relationship, \( \preceq \), as in the previous sections.

**Definition 2.4 (Memory ordering constraints).**

\[
\preceq = \{ (\text{RLX, RLX}), (\text{RLX, ACQ}), (\text{REL, RLX}), (\text{REL, ACQ}) \}
\]

We write \( \text{oC}_1 \preceq \text{oC}_2 \) if \( (\text{oC}_1, \text{oC}_2) \in \preceq \), and as before \( \text{oC}_1 \preceq \text{oC}_2 \) otherwise. Expressing the relation as a negative is perhaps more intuitive, i.e., for all constraints \( \text{oC}, \text{oC} \not\preceq \text{sc} \not\preceq \text{oc}, \text{oC} \not\preceq \text{REL}, \text{and ACQ} \not\preceq \text{oc} \). Additionally, the \( \text{CON} \) constraint is equal to a RLX constraint for the purposes of ordering (but see Sect. 8.2), and \( \text{ACQREL} \) is the combination of both ACQ and REL. An alternative presentation of the relationship of \( \text{oC}_1 \preceq \text{oC}_2 \) is as a grid, i.e.,

\[
\begin{array}{cccc}
\downarrow \text{oC}_1 & \text{RLX} & \text{REL} & \text{ACQ} & \text{SC} \\
\text{RLX} & \checkmark & \times & \checkmark & \times \\
\text{REL} & \checkmark & \times & \checkmark & \times \\
\text{ACQ} & \times & \times & \times & \times \\
\text{SC} & \times & \times & \times & \times \\
\end{array}
\]

(2.39)

Note that acquire loads may come before release stores, that is, \( C \) follows the \( \text{RC}_{pc} \) model rather than the the stronger \( \text{RC}_{sc} \) model in [26] (it is of course straightforward to accommodate either; see also [12]).
A simpler basis for working with the CC++ memory model (extended version)

\[ x \in \text{Var} \quad \text{ocs} \in \mathbb{P} \text{OC} \]

\[
\begin{align*}
\text{OC} & ::= \text{RLX} \mid \text{REL} \mid \text{ACQ} \mid \text{CON} \mid \text{SC} \\
\text{ACQREL} & ::= \{\text{ACQ}, \text{REL}\} \\
e & ::= v \mid x^{\text{ocs}} \mid e_1 \oplus e_2 \\
\alpha & ::= x^{\text{ocs}} := e \mid (e) \mid f^{\text{ocs}} \\
\text{rel\_fence} & ::= \text{store}_{\text{fnc}}^{\text{REL}} \\
\text{acq\_fence} & ::= \text{load}_{\text{fnc}}^{\text{ACQ}} \\
\text{sc\_fence} & ::= \text{full}_{\text{fnc}}^{\text{SC}} \\
\end{align*}
\]

for \( r \in \text{Local}, \) \( r \) abbreviates \( r^{\emptyset} \)

for \( x \in \text{Shared}, \) \( x^{\text{OC}} \) abbreviates \( x^{(\text{oc})} \), and

\( x \) abbreviates \( x^{\text{RLX}} \)

for \( f \) a fence, \( f^{\text{OC}} \) abbreviates \( f^{(\text{oc})} \)

\[ \text{Fig. 1. Syntax extensions for C ordering constraints} \]

We extend the syntax of instructions to incorporate ordering constraints, allowing variables and fences to be annotated with a set thereof, as shown in Fig. 1. The reordering relation for instructions, considering only ordering constraints, can be defined as below.

**Definition 2.5.** Reordering instructions with respect to ordering constraints

\[ \alpha \leftarrow \beta \triangleq [\alpha] \times [\beta] \subseteq^{\text{OC}} \]

where the \([\cdot]\) function extracts the ordering constraints from the expression and instructions syntax.

\[ \begin{align*}
[ v ] &= \emptyset \\
[ x^{\text{ocs}} ] &= \text{ocs} \\
[ e_1 \oplus e_2 ] &= [ e_1 ] \cup [ e_2 ] \\
[ x^{\text{ocs}} := e ] &= \text{ocs} \cup [ e ] \\
[ (e) ] &= [ e ] \\
[ f^{\text{ocs}} ] &= \text{ocs}
\end{align*} \]

(2.41)

For example, \( [x^{\text{REL}} := y^{\text{ACQ}}] = \{\text{REL, ACQ}\} \). Thus \( \alpha \leftarrow \beta \) is checked by comparing point-wise each pair of ordering constraints in \( \alpha \) and \( \beta \). If \( \alpha \) or \( \beta \) has no ordering constraints then \( \alpha \Leftarrow \beta \) vacuously holds.

For example

\[ x^{\text{REL}} := y^{\text{ACQ}} \Leftarrow x^{\text{RLX}} := 1 \iff [x^{\text{REL}} := y^{\text{ACQ}}] \times [x^{\text{RLX}} := 1] \subseteq^{\text{OC}} \]

\[ \iff \{\text{REL, ACQ}\} \times \{\text{RLX}\} \subseteq^{\text{OC}} \]

\[ \iff \text{REL} \Leftarrow \text{RLX} \wedge \text{ACQ} \Leftarrow \text{RLX} \]

\[ \iff \text{False} \quad \text{by Defn. (2.4)} \]

Note that a locals-only instructions, such as \( r_1 := r_2 \ast 2 \), does not have any ordering constraints, and so is not affected by them, that is \( [r_1 := r_2 \ast 2] = \emptyset \) and hence \( r_1 := r_2 \ast 2 \Leftarrow \beta \) for all \( \beta \).

For convenience we define some abbreviations and conventions at the bottom of Fig. 1: we require every reference to a shared variable to have (at least one) ordering constraint, with the default being \( \text{RLX} \); when there is exactly one ordering constraint we omit the set comprehension.
brackets in the syntax, and typically, when the types are clear, we abbreviate \( x^{RLX} \) to plain \( x \) as RLX is the default. Local variables are by definition never declared “atomic” and hence their set of ordering constraints is always empty; hence, when \( r \) is a local variable, we abbreviate \( r^G \) to \( r \). Similarly we abbreviate ordering constraints on fences. We can now define release, acquire and sequentially consistent fences as the combination of a fence and ordering constraint. A “release fence” (rel_fence) operates according to the REL semantics above, and in addition blocks stores, hence is a combination of a store_{inc} and REL ordering, and similarly an “acquire fence” (acq_fence) acts as a load_{inc} and ACQ ordering. A “sequentially consistent” fence (sc_fence) is also defined straightforwardly; these fences map to C’s atomic_thread_fence(...) definition.

To complete the syntax extension we update the syntax-based definitions for extracting variables from expressions and instructions by defining \( wv(x^{ocs} := e) = \{ x \} \) and \( rv(x^{ocs}) = \{ x \} \), that is, read/write variables do not include the ordering constraints (and \( wv(f^{ocs}) = rv(f^{ocs}) = \emptyset \)).

### 2.4 The complete reordering relation

We can now define the C memory model as the combination of the three aspects above.

*Definition 2.6 (Reordering of instructions in C).*

\[
\alpha \overset{\text{C}}{\Leftarrow} \beta \quad \text{iff} \quad (i) \ \alpha \overset{G}{\Leftarrow} \beta, \ (ii) \ \alpha \overset{\text{FNC}}{\iff} \beta, \text{and (iii) } \alpha \overset{\text{OCS}}{\Leftarrow} \beta
\]

(2.42)

Hence reordering of instructions within a C program can occur provided the sequential semantics, fences, and ordering constraints are respected. We show in later sections how this principle does not change for more complex language features, though, of course, the semantics and hence the analysis is correspondingly more complex.

As examples, for distinct \( x, y \in \text{Shared} \) and \( r, r_1 \in \text{Local} \),

\[
\begin{align*}
x &:= 1 & y &:= 1 & r_1 &:= x & r_2 &:= y \\
y &:= 1 & x^{\text{REL}} &:= 1 & \text{but} & x^{\text{REL}} &:= 1 & r := y \\
r_1 &:= x^{\text{ACQ}} & r_2 &:= y & \text{but} & r_1 &:= y & r_2 := x^{\text{ACQ}} \\
\alpha &\overset{\text{C}}{\Leftarrow} \text{rel\_fence} & \text{rel\_fence} &\overset{\text{C}}{\Leftarrow} r := x & \overset{\text{C}}{\Leftarrow} \text{acq\_fence} & x := 1 & \overset{\text{C}}{\Leftarrow} \text{acq\_fence}
\end{align*}
\]

Hence, following the earlier definitions, we have various ways of enforcing program order using the flag set/check (message passing) pattern from earlier. We leave RLX accesses of shared variables \( x \) and flag implicit.

\[
\begin{align*}
x &:= 1 \overset{\text{C}}{\Leftarrow} \text{rel\_fence} \overset{\text{C}}{\Leftarrow} \text{flag} := \text{True} & \overset{\text{C}}{\Leftarrow} x := 1 \overset{\text{C}}{\Leftarrow} \text{rel\_fence} \overset{\text{C}}{\Leftarrow} \text{flag} := \text{True} \\
f &:= \text{flag} \overset{\text{C}}{\Leftarrow} \text{acq\_fence} \overset{\text{C}}{\Leftarrow} r := x & \overset{\text{C}}{\Leftarrow} f := \text{flag} \overset{\text{C}}{\Leftarrow} \text{acq\_fence} \overset{\text{C}}{\Leftarrow} r := x \\
x &:= 1 \overset{\text{C}}{\Leftarrow} \text{flag}^{\text{REL}} := \text{True} & \overset{\text{C}}{\Leftarrow} x := 1 \overset{\text{C}}{\Leftarrow} \text{flag}^{\text{REL}} := \text{True} \\
f &:= \text{flag}^{\text{ACQ}} \overset{\text{C}}{\Leftarrow} r := x & \overset{\text{C}}{\Leftarrow} f := \text{flag}^{\text{ACQ}} \overset{\text{C}}{\Leftarrow} r := x
\end{align*}
\]

(2.43)

### 3 AN IMPERATIVE LANGUAGE WITH REORDERING

We now show how reordering according to the C memory model can be embedded into a more realistic imperative language that has conditionals and loops, based on the previously described wide-spectrum language IMP+psseq [11, 12, 14]. We give a small-step operational semantics and define trace equivalence for its notion of correctness.
The syntax of IMP is given in Fig. 2, with expressions and instructions remaining as shown in Fig. 1.

Commands. The command syntax (defn. (3.1)) includes the terminated command, nil, a sequence of instructions, \( \overline{\alpha} \) (allowing composite actions to be defined), the parallelized sequential composition of two commands according to some memory model \( M, c_1 \sqcap c_2 \), a choice between two commands, \( c_1 \sqcup c_2 \), or a parallelized iteration of a command according to some memory model \( M, \rho \).

From this language we can build an imperative language with conditionals and loops following algebraic patterns \([23, 44]\). We define the special action type \( \tau \) as a True guard (3.2); this action has no observable effect and is not considered for the purposes of determining (trace) equivalence. We allow the abbreviation \( c_1 \sqcap c_2 \) for the case where the model parameter is \( c \) (3.3). We also introduce abbreviations for strict (traditional) order (3.4) and parallel composition (3.5), based on the memory models sc and par introduced earlier (defns. (2.2) and (2.3)). The (parallelized) iteration of a command a finite number of times is defined inductively in defn. (3.6). Conditionals defn. (3.7) and while loops (3.8) can be constructed in the usual way using guards and iteration. We define an empty False branch conditional, if\(^M\) \( b \) then \( c \), as if\(^M\) \( b \) then \( c \) else nil.

Guards. The use of a guard action type \( \langle e \rangle \) allows established encodings of conditionals and loops as described above. However treating a guard as a separate action is useful in considering reorderings as well, and in particular in understanding the interaction of conditionals with compiler optimisations: the fundamentals of reorderings involving guards are based on the principles of preserving sequential semantics (on a single thread) as in Sect. 2.2.1, and these can be lifted to the conditional and loop command types straightforwardly, without needing to deal with them monolithically. Note that if a guard evaluates to False this represents a behaviour that cannot occur.

Composite actions. Since we allow sequences of instructions \( \overline{\alpha} \) to be the basic building block of the language, with the intention that all instructions in the sequence are executed, in order,
as a single indivisible step, we can straightforwardly define complex instructions types such as “compare-and-swap”. For lists we write ⟨⟩ for the empty list, ∪ for concatenation, and ⟨...⟩ as the list constructor. For notational ease we let a singleton sequence of actions ⟨α⟩ just be written α where the intended type is clear from the context. For brevity we allow ∪ to accept single elements in place of singleton lists. Note that an instruction such as \( x := y \) happens as a single indivisible step, that is, the value for \( y \) is fetched and written into \( x \) in one step. This is not realistic for \( C \), and as such we later (Sect. 7, see also Appendix B) show how instructions can be incrementally executed (in the above case, with the value for \( x \) fetched, and only later updating \( y \) to that value). For now we assume that anything evaluated incrementally is written out to make the granularity explicit, for example, the above assignment becomes \( \text{tmp} := y; \ x := \text{tmp} \), for some fresh identifier \( \text{tmp} \); see further discussion in Sect. 7.3.

The composite compare-and-swap command \( \text{cas}(x, e, e') \) is defined as a choice between determining that \( x = e \) and updating \( x \) to \( e' \) in a single indivisible step, or determining that \( x \neq e \) (defn. (3.9)). This can be generalised to include ordering constraints, for instance, in the \( \text{ACQREL} \) case (3.10). Updates to a local variable can be included to record the result (3.11). It is of course straightforward to define other composite commands, such as fetch-and-add (3.12), which map to \( C \)'s inbuilt functions such as \( \text{atomic_compare_exchange_strong_explicit}(...) \) and \( \text{atomic_fetch_add_explicit}(...) \). We show these to emphasise that the definition of reordering does not have to change whenever a new instruction type is added; we can easily syntactically extract the required elements. For instance, given the above definitions, we can determine the following.

\[
\text{cas}(x, v, v') \xleftarrow{C} r := y \quad \text{but} \quad \text{cas}(x, v, v') \xleftarrow{C} r := x \quad \text{and} \quad \text{cas}(x, v, v') \xleftarrow{\text{ACQREL}} C \xleftarrow{C} r := y \quad (3.13)
\]

since \( \text{wv}(\text{cas}(x, v, v')) = \{x\} \), and \( \text{ACQ} \in [\text{cas}(x, v, v')]^{\text{ACQREL}} \). We lift the write/read variables of instructions to commands straightforwardly (see Appendix A), and as such reordering on commands can be calculated, for example,

\[
(\text{if}^C r > 0 \text{ then } x := 1 \text{ else } y := 1) \xleftarrow{C} z := 1 \quad (3.14)
\]

since the assignment to \( z \) is not dependent on anything in the conditional statement.

### 3.2 Small-step operational semantics

The semantics of \( \text{IMP}^+ \) is given in Fig. 3 (an adaptation of [12]). A step (action) is a sequence of instructions which are considered to be executed together, without interference; in the majority of cases the sequences (actions) are singleton. Rule 3.15 places a list of instructions into the trace as a single list (so a trace is a list of lists). Rule 3.16 states that a nondeterministic choice is resolved silently to either branch (in the rules we let \( r \) abbreviate the action \( \tau \)); alternatively we could define \( \tau \) as the empty sequence). Rule 3.17 nondeterministically picks a finite number \( (n) \) of times to iterate \( c \), where finite iteration is defined in defn. (3.6).
Rule 3.18 is the interesting rule, which generalises the earlier rule for prefixing: a command $c_1 \cdot c_2$ can take a step of $c_1$, or begin execution of $c_2$ if $c_1$ is terminated, or execute a step $\beta$ of $c_2$ if $\beta$ reorders with $c_1$. Reordering of an action (list of instructions) with a command is lifted from reordering on instructions straightforwardly (Appendix A).

As an example, from (3.14) we can deduce the following.

\[(\text{if}^c r > 0 \text{ then } x := 1 \text{ else } y := 1) ; z := 1 \xrightarrow{z := 1} (\text{if}^c r > 0 \text{ then } x := 1 \text{ else } y := 1) ; \text{nil}\]

That is, the assignment to $z$ can occur before the conditional; this represents the compiler deciding to move the store before the test since it will happen on either path.

### 3.3 Trace semantics

Given a program $c_0$ the operational semantics generates a trace, that is, a finite sequence of steps $c_0 \xrightarrow{a_1} c_1 \xrightarrow{a_2} \ldots$ where the labels in the trace are actions5. We write $c \xrightarrow{t} c'$ to say that $c$ executes the actions in trace $t$ and evolves to $c'$, inductively constructed below. The base case for the induction is given by $c \xrightarrow{\langle \rangle} c$.

\[
\begin{align*}
  c \xrightarrow{a} c' & \land \text{visible } a \land c' \xrightarrow{t} c'' & \Rightarrow & & c \xrightarrow{a \cdot t} c'' \\
  c \xrightarrow{a} c' & \land \text{silent } a \land c' \xrightarrow{t} c'' & \Rightarrow & & c \xrightarrow{t} c'' \\
\end{align*}
\]

(3.19) (3.20)

Traces of visible actions are accumulated into the trace (using ‘$\cdot$’ for list concatenation) (3.19), and silent actions (such as $r$) are discarded (3.20), i.e., we have a “weak” notion of equivalence [54]. A visible action is any action with a visible effect, for instance, fences, assignments, and guards with free variables. Silent actions include any guard which is True in any state and contains no free variables; for instance, \(\langle 0 = 0 \rangle\) is silent while \(\langle x = x \rangle\) is not. A third category of actions, infeasible $a$, includes exactly those guards \(\langle b \rangle\) where $b$ evaluates to False in every state. This includes actions such as \(\langle x \neq x \rangle\), with the simplest example being \(\langle \text{False} \rangle\), which we abbreviate to magic [56]. Any behaviour of $c$ in which an infeasible action occurs does not result in a finite terminating trace, and hence is excluded from consideration. Such behaviours include those where a branch is taken that eventually evaluates to False.

The meaning of a command $c$ is its set of all possible terminating behaviours $[c]$, leading to the usual (reverse) subset inclusion notion of refinement, where $c \subseteq d$ if every behaviour of $d$ is a behaviour of $c$; our notion of command equivalence is refinement in both directions (3.21).

\[
\begin{align*}
  [c] & \equiv \{ t \mid c \xrightarrow{t} \text{nil} \} \\
  c \subseteq d & \equiv [d] \subseteq [c] \\
  c \sqcup d & \equiv c \sqsubseteq d \land d \sqsubseteq c \\
\end{align*}
\]

(3.21)

From the semantics we can derive the usual properties such as $[c \cap d] = [c] \cup [d]$ and $[c ; d] = [c] \cdot [d]$ (overloading ‘$\cdot$’ to mean pairwise concatenation of lists). We can use trace equivalence to define a set of rules for manipulating a program under refinement or equivalence; we elucidate a general set of these in the following section.

### 4 REDUCTION RULES

Using the notion of trace equivalence the following properties can be derived for the language, and verified in Isabelle/HOL [12]. The usual properties of commutativity, associativity, etc., for the standard operators of the language hold, and so we focus below on properties involving parallelized

---

5Since infinite traces do not add anything of special interest to the discussion of weak memory models over and above finite traces, we focus on finite traces only to avoid the usual extra complications that infinite traces introduce.
These sort of structural rules help elucidate consequences of the memory model for programmers.

\[
\begin{align*}
c_1 ; c_2 & \sqsubseteq c_1 \cdot c_2 \\
c \cap d & \sqsubseteq c \\
(\alpha \cdot c) \parallel d & \sqsubseteq \alpha \cdot (c \parallel d) \\
(\alpha \cdot c) \parallel d & \sqsubseteq \alpha \cdot (c \parallel d) \\
(c_1 \cap c_2) \parallel d & \sqsubseteq (c_1 \parallel d) \cap (c_2 \parallel d) \\
(c_1 \cdot c_2) ; c_3 & \sqsubseteq c_1 ; (c_2 ; c_3) \\
\alpha \sqsubseteq \beta & \Rightarrow \alpha ; \beta \sqsubseteq \alpha \cdot \beta \\
\alpha \sqsubseteq \beta & \Rightarrow \alpha ; \beta \sqsubseteq \alpha \parallel \beta \\
\alpha \sqsubseteq \beta & \Rightarrow \alpha ; (\beta \cdot c) \sqsubseteq \beta \cdot (\alpha ; c)
\end{align*}
\]

Law 4.1 states that a parallelized sequential composition can always be refined to a strict ordering. Law 4.2 states that a choice can be refined to its left branch (a symmetric rule holds for the right branch). Law 4.3 says that the first instruction of either process in a parallel composition can be the first step of the composition as a whole. Such refinement rules are useful for elucidating specific reordering and interleavings of parallel processes that lead to particular behaviours (essentially reducing to a particular trace). Law 4.4 is an equality, which states that if there is nondeterminism in a parallel process the effect can be understood by lifting the nondeterminism to the top level; such a rule is useful for the application of, for instance, Owiciki-Gries reasoning (Sect. 5.4). Law 4.5 states that parallelized sequential composition is associative (provided the same model \( m \) is used on both instances). Laws 4.6 and 4.7 are special cases where, given two actions \( \alpha \) and \( \beta \), if they cannot reorder then they are executed in order, and if they can it is as if they are executed in parallel. Law 4.8 straightforwardly promotes action \( \beta \) of \( \beta \cdot c \) before \( \alpha \), and depending on the structure of \( c \), further of its actions may be reordered before \( \alpha \).

We can extend these rules to more complex structures.

\[
\begin{align*}
\text{if}^m y \geq 0 & \text{ then } x := y \\
b \notin \text{fv}(e) \cup \text{fv}(f) & \Rightarrow \\
\text{if}^c b \text{ then } x := e \text{ else } y := f & \sqsubseteq \\left( (\llparenthesis b \rrparenthesis) \parallel x := e \cap (\llparenthesis \neg b \rrparenthesis) \parallel y := f \right)
\end{align*}
\]

Law 4.9 shows that (full) fences enforce ordering. Law 4.10 gives a special case of a conditional where the True branch depends on a shared variable in the condition, in which case the command is executed in-order (assuming model \( m \) respects data dependencies). Law 4.11 elucidates the potentially complex case of reasoning about conditionals in which there are no dependencies: theoretically the compiler could allow inner instructions to appear to be executed before the evaluation of the condition.

Assuming \( x \in \text{Shared}, b \in \text{Local}, \) and that \( x \) is independent of commands \( c_1 \) and \( c_2 \) (i.e., \( x \notin \text{wv}(c) \cup \text{wv}(d) \)), we can derive the following.

\[
\begin{align*}
\text{if}^c b \text{ then } c_1 \text{ else } c_2 & \parallel x := v \\
\text{if}^c b \text{ then } (c_1 ; x := v) \text{ else } (c_2 ; x := v) & \sqsubseteq (\text{if}^c b \text{ then } c_1 \text{ else } c_2) \parallel x := v
\end{align*}
\]

These sort of structural rules help elucidate consequences of the memory model for programmers at a level that is easily understood.
The next few laws allow reasoning about “await”-style loops, as used in some lock implementa-
tions.

\begin{align}
\alpha_m^* & \sqsubseteq \alpha_{sc}^* \tag{4.14} \\
\text{while}^c b \text{ do nil} & \sqsubseteq (|b|_c^* \land \neg b) \tag{4.15} \\
sv(b) \neq \emptyset & \Rightarrow \text{while}^c b \text{ do nil} \sqsubseteq \text{while}^{sc} b \text{ do nil} \tag{4.16}
\end{align}

Law 4.14 states that a sequence of repeated instructions in order, according to any model \(M\), can be treated as executing in order. Using this property, and others like \(\text{nil} \sqsubseteq c\) (we omit such trivial laws that do not involve reordering) we can deduce Law 4.16, that states that a spin-loop that polls a shared variable can be treated as if executed in strict order.

**Lifting to commands.** So far we have considered reduction laws that apply to relatively simple cases involving individual actions. Lifting the concepts to commands is nontrivial in general, that is, for \(c_1 ; c_2\) there could be arbitrary dependencies between \(c_1\) and \(c_2\) which mean they partially overlap perhaps with pre- or post-sequences of non-overlapping instructions. Here associativity (Law 4.5) may help, allowing rearrangement of the text to split into sections, for instance,

\[(c_1 ; \text{sc}_f ; c_2) ; (c_3 ; \text{sc}_f ; c_4) \sqsubseteq c_1 \cdot \text{sc}_f \cdot (c_2 ; c_3) \cdot \text{sc}_f \cdot c_4 \tag{4.17}\]

We now consider the cases where two commands are completely independent, and where one is always blocked by the other. Independence can be established by straightforwardly lifting \(c\) from instructions to commands, using lifting conventions in Appendix A. The key property is that

\[c \equiv d \Rightarrow c ; d \sqsubseteq c \parallel d \tag{4.18}\]

This follows from partial execution of the semantics: at no point is there an instruction within \(c\) that prevents an instruction in \(d\) from executing (a trivial case is where \(c = \text{nil}\)).

To define the converse case, where \(c\) always prevents \(d\) from executing, consider the following. We write \(c \searrow d\) to indicate that at no point can \(d\) reorder during the execution of \(c\) (a trivial case is where \(c = \text{full}[inc]\)). If \(c \searrow d\) then one can treat them as sequentially composed. We define these concepts with respect to the operational semantics.

\[c \searrow d \equiv \forall \alpha, d' \bullet (d \xrightarrow{\alpha} d' \land \text{visible } \alpha) \Rightarrow c \not\equiv \alpha \tag{4.19}\]

\[c \searrow d \equiv \forall t, c' \bullet (c \Rightarrow c' \land c' \sqsubseteq \text{nil}) \Rightarrow c' \not\equiv d \tag{4.20}\]

We write \(c \searrow d\) when all immediate next possible steps of \(d\) are blocked by \(c\) (4.19). Thus \(c \searrow d\) holds when, after any unfinished partial execution of \(c\) via some trace \(t\) resulting in \(c'\), \(c'\) continues to block \(d\) (4.20). We exclude from the set of partial executions the cases where execution is effectively finished, i.e., when \(c'\) is \(\text{nil}\) or equivalent (otherwise \(c \searrow d\) would never hold as the final \(\text{nil}\) allows reordering). From these we can derive:

\[c \searrow d \Rightarrow c ; d \sqsubseteq c \cdot d \tag{4.21}\]

Such reduction may lift to more complex structures, for instance, the following law is useful for sequentialising loops when each iteration has no overlap with the preceding or succeeding ones.

\[c \searrow c \Rightarrow \alpha_m^* \sqsubseteq \alpha_{sc}^* \tag{4.22}\]

We now show how the application of reduction laws to eliminate (elucidate) the allowed re-
orderings in terms of the familiar sequential and parallel composition enables the application of standard techniques for analysis.
We can lift effects where it does not violate whatever the desired property is (be that a postcondition, or a condition controlling allowed interference). In such circumstances our framework supports making the allowed reorderings explicit in the structure of the program, with a corresponding influence on the proofs of correctness. Where a violation of a desired property occurs due to reordering, the framework also supports the construction of the particular reordering that leads to the problematic behaviour.

The IMP+psseq language includes several aspects which do not exist in a standard imperative language, namely, fences and the ordering constraints that annotate variables and fences. We start with a simple syntactic notion of equivalence modulo these features, reducing a program in IMP+psseq into its underlying ‘plain’ equivalent (fences and ordering constraints have no effect on sequential semantics directly). We then explain how techniques such as Owicki-Gries and rely/guarantee may be applied.

5 APPLYING CONCURRENT REASONING TECHNIQUES

In this section we show how the reduction rules in the previous section can be used as the precursor to the application of already established techniques for proving properties of concurrent programs. For correct, real algorithms influenced by weak memory models there will be no reordering except where it does not violate whatever the desired property is (be that a postcondition, or a condition controlling allowed interference). In such circumstances our framework supports making the allowed reorderings explicit in the structure of the program, with a corresponding influence on the proofs of correctness. Where a violation of a desired property occurs due to reordering, the framework also supports the construction of the particular reordering that leads to the problematic behaviour.

The IMP+psseq language includes several aspects which do not exist in a standard imperative language, namely, fences and the ordering constraints that annotate variables and fences. We start with a simple syntactic notion of equivalence modulo these features, reducing a program in IMP+psseq into its underlying ‘plain’ equivalent (fences and ordering constraints have no effect on sequential semantics directly). We then explain how techniques such as Owicki-Gries and rely/guarantee may be applied.

5.1 Predicate transformer semantics and weakest preconditions

The action-trace semantics of Sect. 3.3 can be converted into a typical pairs-of-states semantics straightforwardly, as shown in Fig. 4. Let the type $\Sigma$ be the set of total mappings from variables to values, and let the effect function $\text{eff} : \text{Instr} \rightarrow \mathcal{P}(\Sigma \times \Sigma)$ return a relation on states given an instruction. We let ‘id’ be the identity relation on states, and given a Boolean expression $e$ we write $\sigma \in e$ if $e$ is True in state $\sigma$, and $e_\sigma$ for the evaluation of $e$ within state $\sigma$ (note that ordering constraints are ignored for the purposes of evaluation). The effect of an assignment $x^{\text{ocs}} := e$ is a straightforward update of $x$ to the evaluation of $e$ (defn. (5.1)), where $\sigma \{x := v\}$ is $\sigma$ overwritten so that $x$ maps to $v$. A guard $\langle e \rangle$ is interpreted as a set of pairs of identical states that satisfy $e$ (defn. (5.2)), giving trivial cases $\text{eff}(\tau) = \text{id}$ and $\text{eff}(\text{magie}) = \emptyset$. A fence $f$ has no affect on the state (defn. (5.3)). Conceptually, mapping $\text{eff}$ onto an action trace $t$ yields a sequence of relations corresponding to a set of sequences of pairs of states in a standard Plotkin-style treatment [66]. We can lift $\text{eff}$ to traces by composing such a sequence of relations, which is defined recursively in (5.5), and the effect of a command is given by the union of the effect of its traces (5.6).

The predicate transformer for weakest precondition semantics is given in defn. (5.7). A predicate is a set of states, so that given a command $c$ and predicate $q$, $wp(c, q)$ returns the set of (pre) states $\sigma$ where every post-state $\sigma'$ related to $\sigma$ by $\text{eff}(c)$ satisfies $q$ (following, e.g., [19]). We define Hoare

\[
\text{eff}(x^{\text{ocs}} := e) = \{(\sigma, \sigma' \{x := e_\sigma\})\} \quad (5.1)
\]

\[
\text{eff}(\langle e \rangle) = \{(\sigma, \sigma) \mid \sigma \in e\} \quad (5.2)
\]

\[
\text{eff}(f) = \text{id} \quad (5.3)
\]

\[
\text{eff}(\langle \rangle) = \text{id} \quad (5.4)
\]

\[
\text{eff}(a@t) = \text{eff}(a) \circ \text{eff}(t) \quad (5.5)
\]

\[
\text{eff}(c) = \bigcup\{\text{eff}(t) \mid t \in [c]\} \quad (5.6)
\]

\[
wp(c, q) = \{\sigma \mid \forall \sigma' \bullet (\sigma, \sigma') \in \text{eff}(c) \Rightarrow \sigma' \in q\} \quad (5.7)
\]

Fig. 4. Sequential semantics
logic judgements with respect to this definition (note that we deal only with partial correctness as we consider only finite traces). From these definitions we can derive the standard rules of weakest preconditions and Hoare logic for commands such as nondeterministic choice and sequential composition, but there are no general compositional rules for parallelized sequential composition.

Trace refinement is related to these notions as follows.

**Theorem 5.1 (Refinement preserves sequential semantics).** Assuming \( c \sqsubseteq c' \) then
\[
\text{eff}(c') \subseteq \text{eff}(c) \quad \text{and} \quad \text{wp}(c, q) \Rightarrow \text{wp}(c', q)
\]

**Proof.** Straightforward from definitions. \( \square \)

The action-trace semantics can be converted into a typical pairs-of-states semantics straightforwardly, based on the effect function. The relationship with standard Plotkin style operational semantics [66] is straightforward, i.e.,
\[
\text{if } c \xrightarrow{\alpha} c' \text{ and } (\sigma, \sigma') \in \text{eff}(\alpha) \text{ then } \langle c, \sigma \rangle \xrightarrow{} \langle c', \sigma' \rangle
\]

The advantage of our approach is that the syntax of the action \( \alpha \) can be used to reason about allowed reorderings using Rule 3.18, whereas in general one cannot reconstruct or deduce an action from a pair of states.

### 5.2 Relating to standard imperative languages

The language IMP\( ^+ \text{pseq} \) extends a typical imperative language with four aspects which allow it to consider weak memory models: ordering constraints on variables; fence instructions; parallelized sequential composition; and parallelized iteration. The first two have no direct effect on the values of variables (the sequential semantics essentially ignores them), while the second two affect the allowed traces and hence indirectly affect the values of variables. However, both parallelized sequential composition and parallelized iteration can be instantiated to correspond to usual notions of execution; hence we consider a plain subset of IMP\( ^+ \text{pseq} \) which maps to a typical imperative program.

**Definition 5.2 (Plain imperative programs).** A command \( c \) of IMP\( ^+ \text{pseq} \) is plain if:

i all instances of parallelized sequential composition in \( c \) are parameterised by either SC or PAR, i.e., correspond to standard sequential or parallel composition; and

ii all instances of parallelized iteration in \( c \) are parameterised by SC, i.e., loops are executed sequentially.

**Definition 5.3 (Imperative syntax equivalence).** Given a plain command \( c \) in IMP\( ^+ \text{pseq} \), a command \( c' \) in a standard imperative language (which does not contain memory ordering constraints on variables or fences), is imperative-syntax-equivalent to \( c \) if \( c \) and \( c' \) are structurally and syntactically equivalent except that:

i all variable references in \( c \) (which are of the form \( x^{\text{ocs}} \) for some set of ordering constraints \( \text{ocs} \)) appear in \( c' \) as simply \( x \); and

ii no fence instructions are present in \( c' \), that is, they can be thought of as no-ops and removed.

We write \( c \plain \approx d \) if \( c \) is imperative-syntax-equivalent to \( d \), or if there exists a \( c' \) where \( c \sqsubseteq c' \) and \( c' \) is imperative-syntax-equivalent to \( d \).

For example, the following two programs are imperative-syntax-equivalent (where \( ; \) in the program on the right should be interpreted as as standard sequential composition, i.e., \( \langle ; \rangle \) or \( \cdot \cdot \) in this paper).

\[
x^{\text{REL}} := 1 ; \sc \text{ _fence} \sc ; y^{\text{BLX}} := 1 ; r := z^{\text{ACQ}} \plain \approx x := 1 ; y := 1 \parallel r := z \quad (5.8)
\]
The program on the left is plain because all instances of parallelized sequential composition correspond to sequential or parallel execution.

Note that there is no imperative-syntax-equivalent form unless all instances of parallelized sequential composition have been eliminated/reduced to sequential or parallel forms. A structurally typical case is the following, where \( c \) reduces to a straightforward imperative-syntax-equivalent program.

\[
(\alpha_1 \; \text{sc\_fence} \; \alpha_2) \parallel (\beta_1 \; \text{sc\_fence} \; \beta_2) = (\alpha_1 \cdot \text{sc\_fence} \cdot \alpha_2) \parallel (\beta_1 \cdot \text{sc\_fence} \cdot \beta_2) \quad (5.9)
\]

\[
\text{plain} \approx (\alpha_1 \cdot \alpha_2) \parallel (\beta_1 \cdot \beta_2) \quad (5.10)
\]

For reasoning purposes one can use the latter program rather than the former.\(^6\) This is because for a plain program in IMP+pseq the semantics correspond to the usual semantic interpretation of imperative programs, ignoring ordering constraints and treating fences as no-ops.

**Theorem 5.4 (Reduction to standard imperative constructs).** If \( \text{plain} \approx c' \), then \( \text{eff}(c) \) is exactly equal to the usual denotation of \( c' \) as a relation (or sequence of relations) on states; and hence any state-based property of \( c \) based on \( \text{eff}(c) \) can be established for \( c' \) that uses a standard denotation for programs.

**Proof.** From Defn. (5.3) and Fig. 4 we can see that i) ordering constraints have no effect on states; ii) fence instructions are equivalent to a no-op (in terms of states) and hence can be ignored; iii) Rule 3.18 reduces to the usual rule for sequential composition when reordering is never allowed, and for parallel composition when reordering is always allowed; and iv) Rule 3.17 and defn. (3.6) reduce to the usual sequential execution of a loop when instantiated with \( \text{sc} \). \( \Box \)

We introduce some syntax to help with describing examples.

**Definition 5.5 (Plain interpretation).** Given a command \( c \) in IMP+pseq, which need not be plain, we let \( c^- \) be the plain interpretation of \( c \), that is, where i) all instances of parallelized sequential composition and parallelized iteration in \( c \) are instantiated by \( /s.sc/c.sc \), except for instances of parallelized sequential composition instantiated by \( /p.sc/a.sc/r.sc \) (corresponding to parallel composition) which remain as-is; and ii) fences in \( c \) do not appear in \( c^- \).

Establishing properties about programs may proceed as outlined below. Assume for some program \( c \) in IMP+pseq that its plain interpretation \( c^- \) satisfies a property \( P \) under the usual imperative program semantics according to some method \( M \). There are three approaches:

1. **Reduction to plain equivalence.** Show that the ordering constraints (due to variables or fences) within \( c \) are such that it reduces equivalently to \( c^- \) (ie, no reordering is possible within \( c \)). Hence \( c \) satisfies \( P \) using \( M \) in \( C \).
2. **Reduction to some plain form.** Reduce \( c \) equivalently to some plain command \( c' \) and apply \( M \) (or some other known method) to \( c^- \) to show that \( P \) holds.
3. **Reduce and deny.** Refine \( c \) to some plain command \( c' \) and apply \( M \) (or some other known method) to \( c^- \) to show that \( P \) does not hold. This corresponds to finding some new behaviour (due to a new ordering of instructions) that breaks the original property \( P \); in this paper \( c' \) tends to be a particular path and we straightforwardly apply Hoare logic to deny the original property \( P \).

We now explain how standard notions of correctness can be applied in our framework.

\(^6\)Strictly speaking we should not use \( \alpha_1 \), etc., on both sides of \( \approx \) because the plain version of \( \alpha_1 \) does not contain ordering constraints on variables; for brevity we ignore the straightforward modifications required in this case.
5.3 Hoare logic

We define a Hoare triple using weakest preconditions (because we only consider finite traces we do not deal with potential non-termination).

\[ \{p\} c \{q\} \equiv p \Rightarrow \wp(c, q) \]

As with Theorem 5.1 refinement preserves Hoare-triple inferences.

\[ c \sqsubseteq c' \Rightarrow \{p\} c \{q\} \Rightarrow \{p\} c' \{q\} \quad (5.11) \]

Given some plain \( c' \) that is equivalent to \( c \) we can apply Hoare logic.

\[ c \plain \approx c' \Rightarrow \{p\} c \{q\} \iff \{p\} c' \{q\} \]

Traditional Hoare logic is used for checking every final state satisfies a postcondition, but it also useful to consider reachable states, which can be defined using the conjugate pattern (see, e.g., [35, 55, 79]; it is related to, but different from, O’Hearn’s concept of incorrectness logic [61] (which is stronger except in the special case when post-state \( q \) is False)).

\[ \langle\langle p\rangle\rangle c \langle\langle q\rangle\rangle \equiv \neg\{p\} c \{\neg q\} \]

Due to its familiarity we use Hoare logic for top-level specifications, although other choices could be made. However Hoare logic is of course lacking in the presence of concurrency (due to parallelism or reordering), and hence we later consider concurrent verification techniques. At the top level we use the following theorems to formally express our desired (or undesired) behaviours.

**Theorem 5.14 (Verification).**

\[ c \sqsubseteq c' \Rightarrow \{p\} c \{q\} \iff \{p\} c' \{q\} \quad (5.14) \]

\[ c \sqsubseteq c' \land \{p\} c' \{\neg q\} \Rightarrow \neg\{p\} c \{q\} \quad (5.15) \]

\[ c \sqsubseteq c' \land \{p\} c' \{q\} \Rightarrow \langle\langle p\rangle\rangle c \langle\langle q\rangle\rangle \quad (5.16) \]

**Proof.** All are automatic from defn. (3.21) and (5.12) and (5.13). \(\square\)

Theorem 5.14 allows properties of a reduced program (\( c' \)) to carry over to the original program (\( c \)). Alternatively by Theorem 5.15 if any behaviour (\( c' \)) is found to violate a property then that property cannot hold for the original (\( c \)). Finally by Theorem 5.16 if any behaviour (\( c' \)) is found to satisfy a property then it is a possible behaviour of the original (\( c \)).

5.4 Owicki-Gries

The Owicki-Gries method [63] can be used to prove a top-level Hoare-triple specification of parallel program \( c \). If \( c \) involves reordering, then reducing \( c \) to some plain form allows the application of Owicki-Gries; several examples of this approach appear in [11].

For instance, recalling (5.9), given a program of the form \((a_1; \texttt{sc_fence}; a_2) \parallel (\beta_1; \texttt{sc_fence}; \beta_2)\) for which one wants to establish some property specified as a Hoare triple, one can use Owicki-Gries on the plain program \((a_1 \cdot a_2) \parallel (\beta_1 \cdot \beta_2)\) by Theorem 5.4: the fences enforce program order, but can be ignored from the perspective of correctness.
Now consider the following slightly more complex case with nested parallelism, where one process uses a form of critical section. Assume \( \alpha \; c \; \beta \).
\[
c \equiv (y_1 : \text{sc\_fence}; \alpha ; \beta ; \text{sc\_fence}; y_2) \parallel (y_3 : \text{sc\_fence}; y_4)
\]
\[
\square (y_1 \cdot \text{sc\_fence} ; (\alpha \parallel \beta) ; \text{fence} ; y_2) \parallel (y_3 \cdot \text{sc\_fence} ; y_4) \tag{5.17}
\]
Unfortunately the Owicki-Gries method is not directly applicable due to the nested parallelism, but in this simple case we can use the fact that execution of two (atomic) actions in parallel means that either order can be chosen.
\[
\alpha \parallel \beta \; \square (\alpha \cdot \beta) \cap (\beta \cdot \alpha) \tag{5.18}
\]
Given an Owicki-Gries rule for nondeterministic choice this can be reasoned about directly, or alternatively we can lift this choice to the top level. Continuing from (5.17):
\[
\square (y_1 \cdot \alpha \cdot \beta \cdot y_2) \parallel (y_3 \cdot y_4) \cap (y_1 \cdot \beta \cdot \alpha \cdot y_2) \parallel (y_3 \cdot y_4) \tag{5.19}
\]
Now Owicki-Gries can be applied to both top-level possibilities. Clearly this is not desirable in general, however, and in the next section we show how the compositional rely/guarantee method can be used to handle nested parallelism.

### 5.5 Rely/guarantee

Rely/guarantee [39, 40] (see also [10, 27, 29]) is a compositional proof method for parallel programs. A rely/guarantee quintuple \( \{ p, r \} c \{ q, g \} \) states that program \( c \) establishes postcondition \( q \) provided it is executed from a state satisfying \( p \) and within an environment that satisfies (rely) relation \( r \) on each step; in addition \( c \) also satisfies (guarantee) relation \( g \) on each of its own steps. For instance, \( \{ x = 0, x \leq x' \} c \{ y' = y, x \geq 10 \} \) states that \( c \) establishes \( x \geq 10 \) when it finishes execution, and guarantees that it will not modify \( y \), provided initially \( x = 0 \) and the environment only ever increases \( x \). In the relations above we have used the common convention in relations that primed variables \( (x') \) refer to their value in the post-state and unprimed variables \( (x) \) refer to their value in the pre-state. A top-level Hoare-triple specification \( \{ p \} c \{ q \} \) can be related to a rely/guarantee quintuple by noting \( \{ p, \text{id} \} c \{ \text{True}, q \} \Rightarrow \{ p \} c \{ q \} \), that is, if \( p \) holds initially in some top-level context that does not modify any variables, then \( c \) establishes \( q \) (with the weakest possible guarantee).

Reasoning using the rely/guarantee method is compositional over parallel conjunction; for instance, without going into detail about rely/guarantee inference rules, consider the plain program from (5.17). We can show a rely/guarantee quintuple holds provided we can find rely/guarantee relations that control the communication between the two subprocesses; we abstract from these nested relations using different names.
\[
\{ p, r \} c \{ q, g \} \iff \{ p, r \} (y_1 \cdot (\alpha \parallel \beta) \cdot y_2) \parallel (y_3 \cdot y_4) \{ g, q \} \ (\text{by (5.17) and Theorem 5.4})
\]
\[
\iff \{ p, r_1 \} (y_1 \cdot (\alpha \parallel \beta) \cdot y_2) \{ g_1, q_1 \} \land \{ p, r_2 \} (y_3 \cdot y_4) \{ g_2, q_2 \}
\]
\[
\iff \{ p, r_1 \} y_1 \{ g_1, q'_1 \} \land \{ q'_1, r_1 \} \alpha \parallel \beta \{ g_1, q'_1 \} \land \{ q'_1, r_1 \} y_2 \{ g_1, q_1 \} \land \{ p, r_2 \} (y_3 \cdot y_4) \{ g_2, q_2 \}
\]
This is straightforward application of standard rely/guarantee inference rules (where we leave the format of the predicates and relations unspecified). Reasoning may proceed from this point, in particular, analysing the quintuple containing the nested parallel composition \( \alpha \parallel \beta \). The question becomes whether the guarantee and the intermediate relation \( q''_1 \) is satisfied regardless of the order that \( \alpha \) and \( \beta \) are executed, and if not, a fence or ordering constraints will need to be introduced.
to enforce order and eliminate the undesirable proof obligation. While completing the proof may or may not be straightforward, the point is it will be matter of the specifics of the example in question, and not of a tailor-made inference system to manage a complex semantic representation. The initial work (as shown in (5.17)) is to elucidate the allowed reorderings as either sequential or parallel composition.

5.6 Linearisability

Linearisability is a correctness condition for concurrent objects [33], which is not an “end-to-end” property such as Hoare triples and rely/guarantee quintuples, but rather requires that operations on some data structure appear to take place atomically, with weakened liveness guarantees. The following abstract program $\text{op}$ follows a common pattern for operations on lock-free, linearisable data structures (in this case $x$), where there may be other processes also executing $\text{op}$.

\begin{align}
\text{repeat} \\
& r_1 := x; \\
& r_2 := f(r_1); \\
& b := \text{cas}(x, r_1, r_2); \\
\text{until } b
\end{align}

(5.20)

The algorithm repeatedly reads the value of $x$ (into local variable $r_1$), calculates a new value for $x$ (applying some function $f$, and storing the result in local variable $r_2$), and attempts to atomically update $x$ to $r_2$; if interference is detected ($x$ has changed since being read into $r_1$) then the loop is retried, otherwise the operation may complete.

The natural dependencies arising from the above structure naturally maintain order, that is, $r_1 := x \leadsto r_2 := f(r_1) \leadsto b := \text{cas}(x, r_1, r_2) \leadsto \langle b \rangle$, hence $\text{op} \stackrel{\text{plain}}{\approx} \text{op}^-$, and any reasoning about $\text{op}$ executing under sequential consistency – in a vacuum – applies to the $\mathcal{C}$ version of $\text{op}$. (Other algorithms may of course have fewer dependencies which will manifest as more complex parallel structures, which must be elucidated via reduction.) Alternative approaches to reasoning about linearisability under weak memory models typically modify the original definition in some way to account for re-orderings [17, 18].

However when considering a calling context reordering must also be taken into account. That is, assume $c$ is some program which contains a call to $\text{op}$, and that $c$ is just one of many parallel processes which may be calling $\text{op}$. Multiple calls to $\text{op}$ (or other operations on $x$) within $c$ are unlikely to cause a problem because the natural dependencies on $x$ will prevent problematic reordering; however one must consider the possibility of unrelated instructions in $c$ reordering with (internal) instructions of $\text{op}$. For instance, consider a case where $x$ implements a queue and $\text{op}$ places a new value into the queue, and within $c$ a flag $f$ is set immediately after calling $\text{op}$ to indicate the enqueue has happened, i.e.,

\[ c \equiv \text{op}() ; \text{flag} := \text{True} \]

The assignment $\text{flag} := \text{True}$ can be reordered with instructions within $\text{op}$ and destroy any reasoning that uses $\text{flag}$ to determine when $\text{op}$ has been called. Placing a release constraint on the flag update resolves the issue (which can be shown straightforwardly in our framework since $\text{op}() ; \text{flag}_{\text{REL}} := \text{True} \sqsubset \text{op}() \cdot \text{flag}_{\text{REL}} := \text{True}$, or in other words, $c \stackrel{\text{plain}}{\approx} c^-$), but more generally this leaves a question about how to capture dependencies within the specification of $\text{op}$. Hence, while one can argue that $\text{op}$ is “linearisable” in the sense that if it is executed in parallel with other linearisable operations on $x$ it will operate correctly, whether or not a calling context $c$ works correctly will still depend on reordering [4, 74]; this can also be addressed in our framework, using reduction and applying an established technique (e.g., [22, 69, 72]).
6 EXAMPLES

In this section we explore the behaviour of small illustrative examples from the literature, specifically classic "litmus test" patterns that readily show the weak behaviours of memory models, and also examples taken from the C standard.

To save space we define the following initialisation predicate for \(x, y, \ldots\) a list of variables.

\[
0_{x,y,\ldots} \equiv x = 0 \land y = 0 \land \ldots 
\]

(6.1)

6.1 Message passing pattern

Consider the message passing ("MP") communication pattern.

\[
\text{mp} \equiv (x := 1 ; \text{flag} := 1) \parallel (f := \text{flag} ; r := x)
\]

(6.2)

The question is whether in the final state that \(f = 1 \Rightarrow r = 1\), i.e., if the "flag" is observed to have been set, can one assume that the "data" \((x)\) has been transferred? This is of course expected under a plain interpretation (Defn. (5.5)).

**Theorem 6.1 (Message passing under sequential consistency).**

\[
\{0_{x,y,r,f}\} \text{mp} \{ f = 1 \Rightarrow r = 1 \}
\]

(6.3)

**Proof.** The proof is checked in Isabelle/HOL using Nieto’s encoding of rely/guarantee inference [58]; the key part of the proof is the left process guarantees \(x = 0 \Rightarrow \text{flag} = 0\) and \(\text{flag} = 1 \Rightarrow x = 1\) (translated into relational form). □

If we naively code this pattern in C this property no longer holds.

**Theorem 6.2 (Naive message passing fails under C).**

\[
\neg \{0_{x,y,r,f}\} \text{mp} \{ f = 1 \Rightarrow r = 1 \}
\]

**Proof.** By definition of C (Model 2.6) we have both \((x := 1) \equiv (\text{flag} := 1)\) and \((f := \text{flag}) \equiv (r := x)\).

\[
\begin{align*}
\text{mp} & \equiv (x := 1 ; \text{flag} := 1) \parallel (f := \text{flag} ; r := x) \\
\sqn x := 1 & \parallel \text{flag} := 1 \parallel f := \text{flag} \parallel r := x \\
\sqn \text{flag} := 1 & \cdot f := \text{flag} \cdot r := x \cdot x := 1 \\
\end{align*}
\]

(6.4)

(6.5)

(6.6)

All instructions effectively execute in parallel; in the final step we have picked one particular interleaving that breaks the expected postcondition, that is,

\[
\{0_{x,y,r,f}\} \text{flag} := 1 \cdot f := \text{flag} \cdot r := x \cdot x := 1 \{f = 1 \land r = 0\}
\]

(6.7)

Since \(f = 1 \land r = 0\) ⇒ \(\neg(f = 1 \Rightarrow r = 1)\) we complete the proof by Theorem 5.15. □

C’s release/acquire atomic are the recommended way to instrument message passing; we make this explicit below using release-acquire constraints on flag (leaving \(x\) relaxed).

\[
\text{mp}^{RA} \equiv (x := 1 ; \text{flag}^{\text{REL}} := 1) \parallel (f := \text{flag}^{\text{ACQ}} ; r := x)
\]

(6.8)

The new constraints prevent reordering in each branch and therefore the expected outcome is reached.

**Theorem 6.3 (Release/acquire message passing maintains sequential consistency).**

\[
\{0_{x,y,r_{1},r_{2}}\} \text{mp}^{RA} \{ f = 1 \Rightarrow r = 1 \}
\]

(6.9)
We now consider the application of the framework to more realistic code, in this case a lock implementation taken from [32] (Sect. 7.3). Conceptually the shared lock \( \ell \) is represented as a boolean which is True when some process holds the lock, and False otherwise.

\[
\begin{align*}
\text{repeat}^M \ c \ \text{until} \ b & \triangleq c \wedge (\neg b) \quad \text{and} \quad (\neg b) \wedge c \\
\text{lock}() & \triangleq \text{repeat}^C \ c \ \text{taken} := \ell.\text{getAndSet}(\text{True}) \ \text{until} \ \neg \text{taken} \\
\text{unlock}() & \triangleq \ell^{\text{REL}} := \text{False}
\end{align*}
\]

A “repeat-until” command \( \text{repeat}^M \ c \ \text{until} \ b \) repeatedly executes \( c \) (at least once) until \( b \) is true, under memory model \( M \), which we encode using parallelized iteration (defn. (6.13)). A “get-and-set” command \( r := x.\text{getAndSet}(e) \) returns the initial value of \( x \) into \( r \) and updates \( x \) to the value of \( e \), as a single step (defn. (6.14)). The load of \( x \) is defined as an \( \text{ACQ} \) access and the update is a \( \text{REL} \) write. Using these the concurrent \( \text{lock}() \) procedure is defined to repeatedly set \( \ell \) to True, and finish when a False value for \( \ell \) is read. If the lock is already held by another process then the get-and-set has no effect and the loop continues, until the case where \( \ell \) is False (as recorded in the local variable \( \text{taken} \)), when \( \ell \) is updated to True to indicate the current process now has the lock. Unlocking is implemented by simply setting \( \ell \) to False.

We have the following general rule for spin loops of the form \( \text{lock}() \).

\[
\alpha \rightsquigarrow (b) \quad \Rightarrow \quad \text{repeat}^C \ \alpha \ \text{until} \ b \sqsupset \text{repeat}^{SC} \ \alpha \ \text{until} \ b
\]

Intuitively, since each iteration of the loop updates a variable that is then checked in the guard, no reordering is possible, and it is as if the loop is executed in sequential order. This holds by the following reasoning.

\[
\begin{align*}
\text{repeat}^C \ \alpha \ \text{until} \ b & \triangleq \text{defn. (6.13)} \\
\alpha ; (\neg b) ; (\alpha) & \quad \text{and} \quad (\neg b) \wedge (\alpha) \\
\square \text{Using Law 4.6 by assumption } \alpha \rightsquigarrow (b) \text{ (and hence also } \alpha \rightsquigarrow (\neg b)) \\
\alpha ; (\neg b) ; (\alpha) & \quad \text{and} \quad (\neg b) \wedge (\alpha) \\
\square \text{Using Law 4.22, since } \alpha \rightsquigarrow (b) \implies (\neg b) \wedge (\alpha) \implies (\neg b) \wedge (\alpha) \\
\alpha ; (\neg b) ; (\alpha) & \quad \text{and} \quad (\neg b) \wedge (\alpha) \\
\square \text{Similarly using Law 4.21 and } \alpha \approx (\neg b) \wedge (\alpha) \\
\alpha ; (\neg b) ; (\alpha) & \quad \text{and} \quad (\neg b) \\
\square \text{defn. (6.13)}
\end{align*}
\]
We now turn our attention to the "out of thin air" problem, where some memory model specifications allow values to be assigned where those values do not appear in the program. Firstly consider the following program, which appears in the C standard.

\[
\text{oota} \equiv \{ r_1 := x; (\text{if}^C r_1 = 42 \text{ then } y := 42) \parallel r_2 := y; (\text{if}^C r_2 = 42 \text{ then } x := 42) \}
\] (6.18)

Under a plain interpretation neither store ever happens: one of the loads must occur, and the subsequent test fail, first, preventing the condition in the other process from succeeding.

**Theorem 6.5.** \{x, y, r_1, r_2\} oota \(\{ x = 0 \land y = 0 \}\).

**Proof.** Trivial using Owicki-Gries reasoning, checked in Isabelle/HOL [59]. \(\blacksquare\)

However, this behaviour is allowed under the C memory model according to the specification (although compiler writers are discouraged from implementing it!). The behaviour is allowed in our framework, that is, it is possible for both \(r_1\) and \(r_2\) to read 42. This is because (unlike hardware memory models [12]) we allow stores to come before guards (via the \(\equiv\) relation, e.g., (2.23)).

**Theorem 6.6.** \(\langle 0_x, y, r_1, r_2 \rangle\) oota \(\langle x = 42 \land y = 42 \rangle\).

**Proof.** We have \(\langle r_1 = 42 \rangle \overset{c}{\equiv} y := 42\) and similarly for \(x\), hence

- Defn. (3.7) \(r_1 := x; (\langle r_1 = 42 \rangle; y := 42) \parallel (r_1 \neq 42)\)
- Law 4.2 \(r_1 := x; (\langle r_1 = 42 \rangle; y := 42\)
- Law 4.7 \(r_1 := x; (\langle r_1 = 42 \rangle \parallel y := 42)\)
- Law 4.3 (taking the right-hand action); Law 4.8 from \(r_1 := x \overset{c}{\equiv} y := 42\) \(y := 42; r_1 := x; (r_1 = 42)\)

The second process reduces similarly to \(x := 42; r_2 := y; (r_2 = 42)\). Interleaving the two processes (Law 4.3) gives the following reduction to a particular execution.

\[
\text{oota} \not\equiv (y := 42; r_1 := x; (r_1 = 42)) \parallel (x := 42; r_2 := y; (r_2 = 42))
\]

\[
\equiv y := 42; x := 42; r_1 := x; r_2 := y; (r_1 = 42) \parallel (r_2 = 42)
\]
Straightforward sequential reasoning gives the following.

\[ \{x, y, r_1, r_2\} \downarrow r_1 := 42 \land x := 42 \land r_2 := y \cdot (r_1 = 42) \cdot (r_2 = 42) \cdot \{x = 42 \land y = 42\}. \] (6.19)

The final state is therefore possible by Theorem 5.16. □

Under hardware weak memory models (the observable effects of) writes can not happen before branch points, and so out-of-thin-air behaviours are not possible.

Consider the following variant of oota.

\[ \text{oota}_D \equiv (\text{id} \land r_1 := 42 \text{ then } y := r_1) \| r_2 := y \cdot (\text{id} \land r_2 = 42 \text{ then } x := r_2). \] (6.20)

The inner assignments have changed from \( y := 42 \) (resp. \( x := 42 \)) to \( y := r_1 \) (resp. \( x := r_2 \)). Arguably the compiler knows that within the true branch of the conditional it must be the case that \( r_1 = 42 \), and thus the assignment \( y := r_1 \) can be treated as \( y := 42 \), reducing to the original oota\(_D\). But this outcome is expressly disallowed, by both the standard and naturally in our framework. That is, we can show that every possible final state satisfies \( x = y = 0 \).

**Theorem 6.7.** \( \{x, y, r_1, r_2\} \text{ oota}_D \{x = 0 \land y = 0\} \).

**Proof.** The initial load into \( r_1 \) creates a dependency with the rest of the code, i.e., \( r_1 := x \cdot (\text{id} \land r_1 = 42 \text{ then } y := r_1) \) (resp. \( x := r_2 \)). Hence we can sequence the initial load of \( x \) (into \( r_1 \)) with the remaining code.

\[ r_1 := x \cdot (\text{id} \land r_1 = 42 \text{ then } y := r_1) \quad r_1 := x \cdot (\text{id} \land r_1 = 42 \text{ then } y := r_1). \] (6.21)

Although the guard and the assignment in the conditional may be reordered with each other (i.e., \( (r_1 = 42) \equiv y := r_1 \)), the fact that the initial load must happen first means that, similarly to Theorem 6.5, there is no execution of oota\(_D\) in which a non-zero value is written to any variable. □

Note that the C standard allows the behaviour of oota and forbids the behaviour of oota\(_D\), and both results arise naturally in our semantics framework without the introduction of any ad-hoc mechanisms. We return to the question of whether guards should be allowed to simplify instructions in Sect. 10.

## 7 Incremental Evaluation of Code

In this and subsequent sections we consider more complex aspects of the C language and execution where they relate to concurrent behaviour, namely, in this section, non-atomic evaluation of instructions (until now we have assumed all instructions appearing in the text of the program are executed in a single indivisible step), in Sect. 8 optimisations of expressions (reducing expressions to improve efficiency), and in Sect. 9 forwarding (using earlier program text to simplify later instructions). We show how each can be incorporated into the framework straightforwardly without any need for change to the underlying definition of the C memory model, although the consequences for reasoning about particular programs may not be straightforward.

### 7.1 Incremental evaluation of expressions

In C one cannot assume expressions are evaluated in a single state. That is, programmers are allowed to write “complex” assignments and conditions but these may be compiled into multiple (indivisible) assembler instructions. For instance, the assignment \( z := x + y \) may compile into (at least) three separation instructions, one to load the value of \( x \), one to load the value of \( y \), and one to finally store the result to \( z \).

We give an operational semantics for incremental expression evaluation in Fig. 5. (We use the term “incremental” rather than the more usual “non-atomic” to avoid terminology clash with C’s
atomics.) Recall the syntax of an expression $e$ from Fig. 1. Each evaluation step of $e$ either loads a value of a free variable or reduces the expression in some way, and evaluation stops when a single value remains. Rule 7.1 states that a variable access $x^{ocs}$ is evaluated to a value $v$ via the guard $(x^{ocs} = v)$. Any choice of $v$ that is not the value of $x$ will result in a false guard, i.e., leads to an infeasible behaviour, which can be ignored. Only the correct value for $v$ leads to a feasible behaviour. Note that the set of ordering constraints on $x$ also appears in the label. Rule 7.2 evaluates a unary expression $⊖e$ by simply inductively evaluating $e$, while Rule 7.3 similarly evaluates each operand of a binary expression, in either order (it is of course straightforward to instead insist on left-to-right evaluation). Rule 7.4 uses a meta-level functor application method $\text{apply}(\cdot)$ to calculate the final value of an expression once all variables have been evaluated.

As an example, consider the following possible evaluation of the expression $x^{acq} + y^{rlx}$.

$$x^{acq} + y^{rlx} \xrightarrow{\{x^{acq}=3\}} 3 + y^{rlx} \xrightarrow{\{y^{rlx}=2\}} 3 + 2 \xrightarrow{\tau} 5$$

The first step applies Rule 7.3 and (inductively) Rule 7.1, and the second step is similar. The choice of values 3 and 2 are arbitrary, and any values could be chosen, reflecting the behaviour of the code in any state. The third and final step follows from (the assumed interpretation) $\text{apply}(\cdot, +, 3, 2) = 5$. Note that the (relaxed) load of $y$ is not restricted by the acquire of $x$ appearing within the same expression, since we have given a nondeterministic expression evaluation order. Of course, one can change the rule for evaluating binary expressions to evaluate left-to-right and consider constraints appearing “earlier” in the expression.

In practice C is not restricted to “laboriously” evaluating each instruction step by step; in some cases evaluation can be wrapped into a single optimisation. We give such a rule in Sect. 8, which subsumes Rule 7.4.

### 7.2 Incremental execution of instructions

Now consider the incremental execution of a single instruction (for brevity, in this section we assume a single instruction $\alpha$ is the base action of the language, rather than a list $\vec{a}$ as in previous sections (defn. (3.1)); we give a full semantics for incremental execution of lists of instructions in Appendix B). We have the concept of indivisible (indivis) actions, which are the only instructions that may be executed directly in the operational semantics. We define an indivisible instruction as one where there are no shared variables to be read, i.e.,

$$\text{indivis}(\alpha) \equiv \text{rsv}(\alpha) = \emptyset$$
A simpler basis for working with the CC++ memory model (extended version)

From this we can derive

\[
\text{indivis}(x := e) \iff \text{sv}(e) = \emptyset \quad \text{indivis}((e)) \iff \text{sv}(e) = \emptyset \quad \text{indivis}(f) \iff \text{True} \quad (7.6)
\]

For instance, \( x := 1 \) is indivisible, while \( r := y \) is not – \( y \) must be separately loaded and the result later stored into \( r \).

Incremental execution rules for instructions are given in Fig. 6. Rule 7.7 states that an assignment instruction is evaluated by first evaluating the assigned expression, and similarly Rule 7.8 states that a guard is executed by first incrementally evaluating the expression. Rule 7.9 states that directly executable instructions can be executed as a single action. This rule applies for fences, and when evaluation of assignment or guard instructions has reduced them to an indivisible form. Note that we allow the (final) evaluation steps to include an arbitrary number of local variables. We insist only on shared variables being evaluated in separate steps, as these involve interactions with the memory system.

As an example of instruction evaluation, recalling (7.5), we place this expression evaluation in a release write.

\[
\begin{align*}
z^{\text{REL}} &= x^{\text{ACQ}} + y^{\text{RLX}} \\
\text{sv(x)} &= 3 \quad \text{sv(y)} &= 2 \\
z^{\text{REL}} &= 5 \\
\text{z}^{\text{REL}} &= 5 \\
\text{nil}
\end{align*}
\]

The first two steps are inherited from the expression evaluation semantics (via Rule 7.7). The final step is via Rule 7.9, noting \( \text{indivis}(z^{\text{REL}} := 5) \). The individual evaluation of local variables is not affected by the shared memory system and hence the following incremental execution is also allowed (where we leave implicit RLX accesses),

\[
\begin{align*}
z := x + r \quad &\Rightarrow z := x + r \\
\text{z} := 3 + r \quad &\Rightarrow \text{z} := 3 + r \\
\text{nil}
\end{align*}
\]

Incremental execution makes explicit what a compiler might do with C code involving shared variables. Note that, importantly, the reordering relation did not have to change or be reconsidered at all, even though the scope of \( C \) considered was increased (and made more complex to reason about, as is always the case when considering incremental evaluation).

7.3 Reasoning about incremental evaluation

Syntax-directed, general inference rules (e.g., in an Owicki-Gries or rely/guarantee framework) are rare for concurrent languages with incremental evaluation of expressions and instructions, irrespective of weak memory models. For instance, a simple program like \( x := x + 1 \parallel x := x + 1 \) can result in final states where \( x \in \{1, 2\} \) when executed incrementally, but this is not immediately derivable from typical compositional proof rules [28]. The problem is that, in general, syntax-directed proof rules do not directly apply as there are many places where interference may occur, which do not neatly align with syntactic terms. The situation is more complicated again with non-deterministic evaluation order, as specified by the C standard.

From a practical perspective the issue is typically resolved by making the atomicity explicit (possibly requiring the introduction of new temporary variables), i.e., we may rewrite the above program as follows.

\[
(r_1 := x; \ x := r_1 + 1) \parallel (r_2 := x; \ x := r_2 + 1) \quad (7.10)
\]
In this format one can apply standard (non-incrementally evaluated) syntax-directed proof rules, such as Owicki-Gries or rely/guarantee, and show that \( x \in \{1, 2\} \) in the final state (possibly requiring the further introduction of auxiliary variables or other techniques). Of course specialised rules to handle particular forms of incrementally-evaluated instructions can be derived, and these may be applied in some cases, but in general the intent is to precisely deal with communication/behaviour as written in the text of program.

As the difficulty of reasoning about possibly dynamically changing code structure impacts on reasoning about C programs, especially with reordering and incremental evaluation, we make this clearer by expressing it in terms of a definition and some remarks.

**Definition 7.1 (Atomic-syntax-structured code).** A command in standard imperative programming syntax, where all basic building blocks (conditions, assignments) of command \( c \) are evaluated/executed atomically, and execution proceeds in program-order, is **atomic-syntax-structured** code.

Note that a subset of IMP\textsuperscript{pseq} can be atomic-syntax-structured, especially if taking the plain subset (Defn. (5.2)) and using the semantics of Sect. 3.2.

**Remark 7.1.** Most inference systems for concurrent code work on the basis the code is atomic-syntax-structured; it is non-trivial to apply syntax-based approaches if the syntax does not directly map to execution. Often the atomicity is made explicit by introducing temporary variables, or a non-syntax based approach is used for verification, e.g., translating into automaton systems where, again, the atomicity is explicit.

**Remark 7.2.** Many other approaches are still applicable to non-atomic-syntax-structured code, for instance, model checking.

We emphasise that C programs are in general not atomic-syntax-structured, and thus complicates analysis by some techniques, regardless of whether or not the C memory model is taken into account.

It is beyond the scope of this paper to develop rules that handle non-atomic-syntax-structured code but, as before, one may apply such rules after reduction. We argue that the level of granularity should be made explicit, or in other words, programmers (who wish to do analysis) should restrict themselves to instructions that are directly executable. For instance, normal assignments that reference at most one shared variable (see e.g., [30] for rules coping with such situations).

If the developer insists on reasoning about code that is not atomic-syntax-structured then some of the reduction rules need provisos under incremental execution. For instance, Law 4.6 holds only when both instructions are indivisible, i.e., it must be updated to ensure the relevant instructions are indivisible.

\[
\alpha \not\equiv \beta \land \text{indivis}(\alpha, \beta) \Rightarrow \alpha \parallel \beta \parallel \alpha \ast \beta
\]

If either is not indivisible then there may be parts of \( \beta \) that can be incrementally evaluated before \( \alpha \), for instance consider:

\[
x := 1 ; z := x + y
\]

Although \( x := 1 \not\equiv z := x + y \) due to \( x \), the load of \( y \) can come before \( x := 1 \), i.e., it is not the case that \( x := 1 \parallel z := x + y \) under incremental execution. The reference to \( y \) can be incrementally evaluated and reordered before the store to \( x \).

\[
x := 1 ; z := x + y \xrightarrow{\{y=3\}} x := 1 ; z := x + 3 \xrightarrow{\{x=1\}} z := 4 \xrightarrow{} \text{nil}
\]  
(7.11)

As with proof methods, specific reduction rules to handle incremental evaluation can be derived (possibly using a program-level encoding of evaluation as given in [13, 31]).
8 EXPRESSION OPTIMISATIONS

We now consider a further important factor influencing execution of programs under the C memory model: expression optimisations (we consider structural optimisations for instance, changing loop structures, in Sect. 11.2). There are three principles when considering "optimising" expression \( e \) to \( e' \):

- **Value equality.** Expression \( e' \) must be equal to \( e \) in all states. However, as we see below, extra contextual information can be used.

- **Lexicographic simplification.** We say \( e \overset{\text{lex}}{\succ} e' \) if \( e' \) is a "more optimised" expression than \( e \), in the sense that it is less computationally intensive to evaluate. A precise definition of \( \succ \) for C is beyond the scope of this work, but we assume it is irreflexive and transitive, and that intuitive properties such as \( 3 + 2 > 5 \), and \( 0 \times r > 0 \) hold. An important aspect is that \( \succ \) may allow the removal of variables (as in \( \times r \succ 0 \)), and this could have an effect on allowed reorderings according to Model 2.2, \( G \) (i.e., one cannot rely on "false dependencies" [1]).

- **Memory ordering constraint simplification.** We say \( e \overset{\text{oc}}{\succeq} e' \) if \( e' \) does not lose any significant memory ordering constraints. For instance, it may be the case that compilers should not "optimise away" an explicit sc constraint, even if valid according to the other optimisations. Again, the precise definition of this is a matter for the C committee, but we explore some of the options and their consequences below in Sect. 8.1.

These three constraints must be satisfied before an expression \( e \) is 'optimised' to expression \( e' \), written \( e \overset{\text{opt}}{\succ} e' \).

\[
e \overset{\text{opt}}{\succ} e' \iff e = e' \land e \overset{\text{lex}}{\succ} e' \land e \overset{\text{oc}}{\succeq} e'
\]

(8.1)

The following operational rule allows optimisations as an expression evaluation step, supersed-ing Rule 7.4 and in some cases removes the need for Rule 7.3, etc.

**Rule 8.2 (Optimise expression).**

\[
\begin{align*}
& b \Rightarrow e \overset{\text{opt}}{\succ} e' \\
& \quad \langle \|b\| \rangle \Rightarrow e' \\
& b \Rightarrow e \\
\end{align*}
\]

Rule 8.2 states that an expression \( e \) can be optimised to some expression \( e' \), in the process emitting a guard \( \langle |b| \rangle \), where \( b \) provides the context which makes the optimisation valid (the expression \( b \) is used only to show \( e = e' \) in defn. (8.1)). The guard acts as a check that the optimisation is valid in the current state; for many optimisations \( b \) will simply be True.

As an example, assuming a definition of \( \overset{\text{oc}}{\succeq} \) where \( e \overset{\text{oc}}{\succeq} e' \) holds provided \( e \) contains only relaxed or no ordering constraints, and \( e' \) has a subset of those, then the following steps are allowed by Rule 8.2.

\[
x := r - r \rightarrow x := 0 \quad \text{Since True } \Rightarrow r - r = 0 \land r - r \overset{\text{lex}}{\succ} 0 \land r - r \overset{\text{oc}}{\succeq} 0
\]

\[
x := r_1 - r_2 \rightarrow x := 0 \quad \text{Since } r_1 = r_2 \Rightarrow r_1 - r_2 = 0 \land r_1 - r_2 \overset{\text{lex}}{\succ} 0 \land r_1 - r_2 \overset{\text{oc}}{\succeq} 0
\]

\[
r := x^{\text{RLX}} \ast 0 \rightarrow r := 0 \quad \text{Since True } \Rightarrow x^{\text{RLX}} \ast 0 = 0 \land x^{\text{RLX}} \overset{\text{lex}}{\succ} 0 \land x^{\text{RLX}} \overset{\text{oc}}{\succeq} 0 \\
\]

On the other hand, given the above assumption about \( \overset{\text{oc}}{\succeq} \), \( r := x^{\text{SC}} \ast 0 \) cannot be optimised to \( r := 0 \) as this would lose a significant reordering constraint (\( x^{\text{SC}} \ast 0 \overset{\text{oc}}{\succeq} 0 \) and hence \( x^{\text{SC}} \ast 0 \overset{\text{opt}}{\succeq} 0 \)). We consider other examples in the subsequent section.
8.1 Defining allowed changes to ordering constraints

One of the tensions in the development of the C memory model is how accepted compiler optimisations interact with memory ordering constraints. Rather than take a particular position, or try to be exhaustive, we show how different options can be expressed and their consequences enumerated formally and (relatively) straightforwardly.

Consider the following five possible definitions for \( \preceq \). Recall that \([ e ]\) extracts the memory ordering constraints from expression \( e \) (defn. (2.41)). We abbreviate \( /a.sc/c.sc/s.sc \hat{=} \{ /a.sc/c.sc/q.sc, /c.sc/o.sc/n.sc, /s.sc/c.sc \} \), as these are the significant ordering constraints that may appear in expressions (REL constraints appear only on the left-hand side of assignments and thus are not subject to expression optimisation).

\[
e \preceq e' \equiv \begin{cases} 
[ e' ] &= [ e ] & (a) \text{ Do not modify constraints} \\
[ e' ] &\subseteq [ e ] \subseteq \{ \text{RLX} \} & (b) \text{ Simplify/eliminate relaxed} \\
[ e ] &\subseteq \{ \text{RLX} \} & (c) \text{ Strengthening allowed} \\
[ e ] \cap \text{ACS} &= [ e' ] \cap \text{ACS} & (d) \text{ Never optimise ACS away} \\
\text{True} &= \text{True} & (e) \text{ Do not constrain the compiler}
\end{cases}
\]

Option (a) is the most conservative option and simply says the compiler must not change the constraints in \( e \) at all. This would be simple to implement and reason about, but possibly prevents some sensible/expected optimisations.

Option (b) says that only relaxed or non-atomic expressions \( e \) may be removed, and the optimised expression \( e' \) can either remain relaxed or become non-atomic itself. Stronger constraints (ACQ, CON, and SC) will not be “optimised away”.

Option (c) says that only relaxed or non-atomic expressions can be optimised, however, any such constraints can be strengthened (e.g., a RLX access can be strengthen to SC). While more subtle than the other options, it imposes fewer constraints on the compiler writer, and would only have the effect of reducing the number of behaviours of code.

Option (d) requires ACQ and SC constraints to be maintained, if they occur, but other parts of a complex expression can be optimised.

Option (e) allows full freedom to the compiler, leaving the programmer unable to rely entirely on memory ordering constraints to enforce order.

We give some examples in tabular form to understand the consequences of these choices.

| \( e \preceq e' \) | (a) | (b) | (c) | (d) | (e) |
|----------------|-----|-----|-----|-----|-----|
| \( 5 \ast 4 \preceq 20 \) | ✓ | ✓ | ✓ | ✓ | ✓ |
| \( x^{RLX} \ast 0 \preceq 0 \) | ✓ | × | ✓ | ✓ | ✓ |
| \( x^{SC} \ast 0 \preceq 0 \) | × | × | × | × | ✓ |
| \( x^{SC} \preceq x^{RLX} \) | × | × | × | × | ✓ |
| \( x^{RLX} \preceq x^{SC} \) | × | × | ✓ | × | ✓ |

As with incremental evaluation of expressions, while it is straightforward to incorporate optimisations into the semantics, programs may not be atomic-syntax-structured (Defn. (7.1)), and hence a programmer interested in serious analysis is well advised to avoid potential simplification of expressions that a compiler may or may not choose to make.

8.2 The consume ordering constraint

Because C’s consume (CON) constraint has no reordering constraint beyond that of data dependencies we have for brevity not included it in earlier sections. The intent of a CON load is to indicate to the compiler not to lose data dependencies during optimisations. Options (b)-(e) for \( \preceq \) allow RLX
variable accesses to be removed, which may also remove a data dependency to some earlier load. This is the situation that a CON load is intended to avoid. For instance, the following optimisation should not be allowed.
\[ r := x^{\text{CON}} ; y := r \ast 0 \rightarrow r := x^{\text{CON}} ; y := 0 \]

The flow-on effect is that now \( y := 0 \) is independent of \( r := x^{\text{CON}} \) and may be reordered before it (as CON is equivalent to RLX in calculating \( \leq_{\text{ACQ}} \)). To faithfully implement this a compiler must track data dependencies, and apparently this has never been implemented; as such all known compilers translate CON constraints directly to the stronger ACQ constraint (which on many architectures results in a more computationally expensive mechanism than necessary). Such syntactic tracking is straightforward, if tedious, to implement in a formal setting. For instance, by tracing data-dependencies (via write and read variables) from all CON loads, marking them with some special ordering constraint 'CONDEP' (consume-dependent), and requiring the definition of \( \geq \) to never allow CONDEP constraints to be removed. As always, a programmer is well-advised to minimise the use of CON constraints with later code that may allow expression optimisations to break data dependencies.

### 8.3 Examples

We show how the compiler may “optimise-away” an ordering constraint and hence open up more behaviours than the programmer may expect. In the following assume Option (b) above for the definition of \( \geq \). A programmer may choose to enforce order in the mp program (defn. (6.2)) using a data dependency.

\[ x := 1 ; \text{flag} := 1 + (x \ast 0) \]

Although \( x := 1 \leadsto \text{flag} := 1 + (x \ast 0) \) and thus it seems the assignment to \( y \) must occur after the assignment to \( x \), after optimising the second instruction the updates can occur in the reverse order. That is, by Rule 8.2 (within Rule 7.7), \( \text{flag} := 1 + (x \ast 0) \rightarrow \text{flag} := 1 \), and thus we have the following behaviour.

\[ x := 1 ; \text{flag} := 1 + (x \ast 0) \rightarrow x := 1 ; \text{flag} := 1 \rightarrow x := 1 \rightarrow \text{nil} \quad (8.4) \]

As a consequence, for reasoning about the original code, one must accept the following refinement.

\[ x := 1 ; \text{flag} := 1 + (x \ast 0) \leq \text{flag} := 1 \ast x := 1 \]

Alternatively a programmer may choose to avoid the dependence on data and instead enforce order using an SC constraint in the flag expression on an unrelated variable. Under option (e) this would be erroneous, since \( 1 + (y^{\text{SC}} \ast 0) > 1 \), and thus as above,

\[ x := 1 ; \text{flag} := 1 + (y^{\text{SC}} \ast 0) \leq \text{flag} := 1 \ast x := 1 \]

### 9 FORWARDING

A key aspect of hardware pipelines is that instructions later in the pipeline can read values from earlier instructions (under certain circumstances). At the microarchitectural level, rather than waiting for an earlier instruction to commit and write a value to a register before reading that value from the register, it may be quicker to read an “in-flight” value directly from an earlier instruction before it commits. This behaviour may be implemented by so-called “reservation stations” or related mechanisms [76]. Fortunately there is a straightforward way to capture this in a structured program, by allowing later instructions that are reordered to pick up and use values in the text of earlier instructions. For instance, the rules of the earlier section forbid \( r := x \) reordering before \( x := 1 \), i.e., \( x := 1 \nRightarrow r := x \), which is conceptually prevented because reading an
earlier value of \( x \) (than 1) is prohibited by coherence-per-location (formally, \( x := 1 \not< r := x \) because \( \omega v (x := 1) = \{ x \} \subseteq \varphi v (r := x) \)). However processors will commonly just use the value 1 and assign it to \( r \) as well, before any other process has seen the write to \( x \).

In hardware the mechanism of using earlier values in later instructions is called forwarding. Notationally we write \( a \bowtie \beta \) to mean the effect of forwarding (assignment) action \( a \) to \( \beta \), which is just simple substitution (ignoring memory ordering constraints). For instance, in the above situation the value 1 assigned to \( x \) can be “forwarded” to \( r \), written \( (x := 1) \bowtie (r := x) = r := 1 \), avoiding the need to access main memory.

**Definition 9.1 (Forwarding).** Given an assignment instruction \( a \) of the form \( x^{oc} := e \), forwarding of \( a \) to an expression \( f \) (written \( \bowtie f \)) is standard replacement of instances of \( x \) by \( e \) within \( f \), ignoring ordering constraints. This is lifted to forwarding to instructions as below.

\[
\bowtie (y^{oc} := f) = (a^{oc}) f \quad (a^{oc}) (b) = (\bowtie b) \quad a^{oc} f = f
\]

Forwarding to/from commands and traces is similarly straightforward; see Appendix A.2. Note that \( a \not< \bowtie \beta \Rightarrow a^{oc} \bowtie \beta = \beta \), i.e., forwarding is relevant only if there is a data dependence. The following examples show the relatively straightforward application of forwarding.

\[
\begin{align*}
\text{r1} := & 1 \bowtie (r_1 = 1) = (1 = 1) \bowtie (\text{True}) = \text{True} = \tau \\
\text{r1} := & 2 \bowtie (r_1 = r_2) = (r_2 = r_2) \bowtie (\text{True}) = \tau
\end{align*}
\]

(9.1)

To capture the potential for an earlier instruction to affect a later one we generalise reordering to a triple, \( \beta' \bowtie a^{oc} \bowtie \beta \). Whereas earlier we considered whether \( a \not< \bowtie \beta \) directly, we now allow \( a \) to affect \( \beta \) via forwarding, and for the resulting instruction \( (\beta') \) to be considered for the purposes of calculating reordering. More precisely, for instructions \( a \) and \( \beta \),

\[
\beta' \bowtie a^{oc} \bowtie \beta \quad \bowtie \alpha \bowtie \beta' \bowtie \alpha \bowtie \beta \bowtie \alpha^{oc} \bowtie \beta' \bowtie \alpha^{oc} \bowtie \beta
\]

(9.2)

The reordering triple notionally gives the idea of executing \( \beta \) earlier with respect to \( a \), with possible modifications due to forwarding. The new instruction \( \beta' \) is the result of forwarding \( a \) to \( \beta \), and it must be reorderable with \( a \) (note, therefore, that reordering is calculated after applying forwarding). For instance, \( r := 1 \bowtie x := 1 \bowtie r := x \) expresses that \( r := x \) can reorder with \( x := 1 \), after forwarding is taken into account. Additionally the effect of forwarding must not have significantly altered the ordering constraints, i.e., \( \bowtie a^{oc} \bowtie \beta \) (recall the options in Sect. 8.1). For instance, depending on the definition of \( \bowtie \), it may or may not be the case that \( r := 1 \bowtie x := 1 \bowtie r := x^{oc} \), as this depends on whether \( x^{oc} \bowtie \leq 1 \). The reordering triple lifts to traces and commands straightforwardly; see Appendix A.2.

We use this more general triple in place of binary reordering in Rule 3.18.

**Rule 9.3 (Reorder with forwarding).**

\[
c_2 \xrightarrow{b} c_2' \quad c_2 \xrightarrow{b} c_2' \quad \beta' \bowtie c_1 \bowtie \beta
\]

Now, given command \( c_1 ; c_2 \), and that \( c_2 \) can execute step \( \beta \), then the composition can execute the modified \( \beta' \), where \( \beta' \) takes in to account any forwarding that may occur from instructions in \( c_1 \) to \( \beta \).

Consider the simple statement \( x := r_1 - r_2 \), which can be optimised to \( x := 0 \) provided \( r_1 = r_2 \). That is, by Rule 8.2, \( x := r_1 - r_2 \xrightarrow{[r_1 = r_2]} x := 0 \). Let us consider this statement immediately following the assignment \( r_1 := r_2 \). By Defn. (9.1) and by (9.1) we have \( \tau \bowtie r_1 := r_2 \bowtie (r_1 = r_2) \). Hence by applying
Rule 9.3 this program can take an initial silent step, representing an optimisation of the compiler, to simplify the assignment to \( x \).

\[
\begin{align*}
  r_1 & := r_2 ; x := r_1 - r_2 \overset{\tau}{\longrightarrow} r_1 := r_2 ; x := 0 \\
\end{align*}
\]  

(9.4)

From here the assignment to \( x \) can proceed first, despite the data dependence \( r_1 := r_2 \leadsto x := r_1 - r_2 \), that is,

\[
\begin{align*}
  r_1 & := r_2 ; x := r_1 - r_2 \sqsubseteq x := 0 \cdot r_1 := r_2
\end{align*}
\]

### 9.1 Reduction with forwarding

We update some of the reduction rules from Sect. 4 to include forwarding via Rule 9.3, essentially replacing \( \alpha \overset{c}{\leadsto} \beta \) with the more general \( \beta' \overset{c}{\leadsto} \beta \). We assume indivis(\( \alpha \)) and indivis(\( \beta \)). Note that if \( \alpha \not\overset{d}{\leadsto} \beta \) then \( \beta' \overset{c}{\leadsto} \beta' \overset{c}{\leadsto} \beta \). We assume indivis(\( \alpha \)) and indivis(\( \beta \)).

\[
\begin{align*}
  \beta' \overset{c}{\leadsto} \alpha & \iff \alpha ; \beta \sqsubseteq \beta' \cdot \alpha \\
  \beta' \overset{c}{\leadsto} \alpha & \iff \alpha ; \beta \sqsubseteq (\alpha ; \beta) \cap (\beta' ; \alpha) \\
  \beta' \overset{c}{\leadsto} \alpha & \iff \beta' \cdot \beta \sqsubseteq \beta \cdot \alpha \\
  \alpha \overset{c}{\leadsto} \beta & \iff \alpha ; \beta \sqsubseteq \alpha \cdot \beta
\end{align*}
\]

(9.5) (9.6) (9.7) (9.8)

Law 9.5 expresses the reordering of \( \beta \) earlier than \( \alpha \) but with any forwarding from \( \alpha \) to \( \beta \) taken into account in the promoted instruction, while Law 9.6 is the corollary of Law 4.7. Law 9.7 is the generalisation of Law 9.5 to a command on the left. Law 9.8 applies when reordering is not possible even taking into account the effects of forwarding, replacing Law 4.6. The presence of forwarding therefore complicates reduction, however the derived properties for reasoning (Sect. 5) still apply to any reduced program.

A subtlety of a chain of dependent instructions with forwarding is that associativity can be lost.

For instance, consider the program \( x := 1 ; r_1 := x ; r_2 := x \). The behaviours are different depending on how this is bracketed: \( p_1 \overset{\tau}{\leadsto} (x := 1 ; r_1 := x) ; r_2 := x \) or \( p_2 \overset{\tau}{\leadsto} x := 1 ; (r_1 := x ; r_2 := x) \). We have \( p_1 \sqsubseteq p_2 = 1 \cdot r_1 := 1 \cdot x := 1 \) by Law 9.7, however \( p_2 \not\sqsubseteq r_1 := 1 \cdot x := 1 \) because \( r_1 := x \not\overset{\tau}{\leadsto} r_2 := x \). Hence \( p_1 \not\sqsubseteq p_2 \), and so associativity has been broken.

The addition of forwarding also explains why a compiler transformation such as “sequentialisation” [42] is not valid. While it is straightforward that \( c \parallel d \sqsubseteq c \cdot d \), i.e., enforcing a strict order between two parallel processes, it is not the case in general that \( c \parallel d \sqsubseteq c \cdot d \), due to forwarding.

The simplest case is \( x := 1 \parallel r := x \), which has exactly two possible traces (interleavings), however \( x := 1 \parallel r := x \parallel r := x \parallel x := 1 \) by Law 9.5, where \( r \) receives the value 1 before it is assigned to \( x \), which is not possible when executing in parallel.

### 9.2 Example

Forwarding admits some perhaps unexpected behaviours, for instance, in the following code, although \( r := x \) and \( x := 1 \) are strictly ordered locally, it is possible for \( r := x \) to receive that later value, ostensibly breaking local coherence.

**Theorem 9.2.** \( \langle 0 \_r \rangle \langle x \_y <r \rangle \) \( \langle r := x \cdot y := x \rangle \parallel x := y \langle r = 1 \rangle \)

**Proof.** Call the left and right programs \( p_1 \) and \( p_2 \), respectively. Note that in \( p_1 \) although \( r := x \) precedes the assignment \( x := 1 \) (the only occurrence of the value 1 in the program), and \( x := 1 \) cannot be reordered before \( r := x \); this theorem states that \( r := x \) can read that value. Firstly note
that \( y := 1 \leftarrow r := x; x := 1 \leftarrow y := x \), that is, \( y := x \) can read \( x := 1 \) and be reordered before the preceding instructions, and hence by Law 9.7 we have

\[
p_1 \subseteq y := 1 \cdot r := x \cdot x := 1
\]

Hence interleaving \( p_1 \) and \( p_2 \) so that \( x := y \) in \( p_2 \) becomes the second instruction executed gives the following.

\[
p_1 \parallel p_2 \subseteq y := 1 \cdot x := y \cdot r := x \cdot x := 1
\]

This reordering and interleaving satisfies \( \{0_{x,y,r}\} y := 1 \cdot x := y \cdot r := x \cdot x := 1 \{r = 1\} \), and thus the outcome \( r = 1 \) is a possible final state of \( p_1 \parallel p_2 \) by Theorem 5.16. □

It appears that coherence has been broken (indirectly through a concurrent process). However, the intuition is that the compiler (and/or the processor) decides that the programmer intended \( y := 1 \) when they wrote \( y := x \), and it is this value that is read by \( r := x \) via the second process. To make this clearer, consider changing the trailing assignment \( y := x \) in the first process to \( y := x + 1 \). In this case a possible final state is \( r = 2 \) (but not \( r = 1 \)), meaning that the initial load of \( x \) has read the (arguably independent) write to \( y \), not the write to \( x \).

Forwarding of assignments is considered standard, and behaviours such as that shown by this example are accepted (in real code, typically a programmer will try to avoid loading a variable that has already been locally calculated, so this pattern, while certainly valid and has its uses, is not necessarily widespread). However, the situation is more complicated if one wishes to forward guards as well as assignments to later instructions, which we explore in Sect. 10.

#### 9.3 Combining forwarding with optimisation/simplification

To keep the discussion of forwarding relatively simple we separated it from optimisation, but we can generalise defn. (9.2) to incorporate optimisations as well.

\[
\beta' \triangleleft \alpha \triangleleft \beta \equiv \alpha \triangleleft \beta' \land \beta' \triangleright_{\text{opt}} \alpha \triangleright \beta
\]

(9.9)

This definition allows any “optimised” version of \( \beta \) to be reordered before \( \alpha \), provided forwarding is taken into account. It can become the basis for the application of Rule 9.3, and thus the derived reduction rules in Sect. 9.1. For instance, in comparison with the example in Sect. 9, we can reorder, forward and optimise in a single step since, by defn. (9.9), \( x := 0 \triangleleft r_1 := r_2 \triangleleft x := r_1 - r_2 \). The corresponding deduction rules allow us to show, for instance, the following allowed reordering and simplification of code by the compiler.

\[
x := y; z := x - y \subseteq z := 0 \cdot x := y
\]

(9.10)

because \( r \triangleleft x := y \triangleleft (x = y) \). This answers the question “can \( z := x - y \) be reordered before \( x := y \)?”: provided all references are relaxed then \( z := 0 \) can be executed earlier than the update to \( x \). Of course, structured reasoning about code which is susceptible to such compiler transformations may be nontrivial as it is not atomic-syntax-structured.

#### 10 Read-from-untaken-branch (RFUB)/Self-fulfilling prophecies (SFPs)

In this section we separately consider a problematic situation which is debated by the C committee, where what is considered reasonable compiler optimisation leads to complex behaviour which is difficult to reason about. We show how the problematic behaviour is disallowed by the semantics we have given so far, and a small modification – which we call allowing self-fulfilling prophecies (SFP) – can be made which then allows the problematic behaviour; and we also show that allowing SFPs contradicts other, simpler cases which are expressly forbidden. We believe this provides a
firm, accessible basis on which to assess which compiler optimisations should be allowed in the presence of shared-variable concurrency (i.e., C’s atomics). Importantly the framework gives a step-based, relatively intuitive, explanation for the different possible behaviours, and flexibility to accommodate different decisions.

10.1 Read-from-untaken-branch behaviour

Consider the following program, which, for particular compiler optimisations, exposes a “read from untaken branch” (rfub) behaviour.

\[
\text{rfub} \equiv (r := y; (\text{if } c \neq 42 \text{ then } b := \text{True}; \ r := 42); \ x := r) \parallel y := x \quad (10.1)
\]

Taking a plain, sequential execution of rfub, starting with \(\neg b\) and all other variables 0, then both \(r\) and \(x\) are 42 in the final state, and \(y\) is either 0 or 42 depending on when the right-hand process interleaves. The True branch of the conditional is always executed.

**Theorem 10.1.**

\[
\{0, x, y, r \land \neg b\} \text{rfub}^\sim \{x = 42 \land r = 42 \land b \land (y = 0 \lor y = 42)\}
\]

and hence

\[
\neg\langle\langle 0, x, y, r \land \neg b \rangle\rangle \text{ rfub}^\sim \langle\langle x = y = r = 42 \land \neg b \rangle\rangle
\]

**Proof.** Straightforward: the only assignment of 42 is within the conditional, after the read of \(y\), and hence at that point \(y\) cannot be 42. The condition \(r \neq 42\) always holds and the True path is taken, setting \(r\) to 42 and \(b\) to True, and finally setting \(x\) to 42. The final value of \(y\) depends on whether the assignment \(y := x\) occurs before or after the assignment to \(x\). By corollary it is therefore not possible to reach a final state where all variables are 42 and \(\neg b\). \(\Box\)

Given this, in a sequential setting a compiler may choose to optimise the conditional as follows, letting ‘\(\leftrightarrow\)’ stand for a compiler transformation.

\[
(\text{if } c \neq 42 \text{ then } b := \text{True}; \ r := 42) \leftrightarrow b := (r \neq 42); \ r := 42 \quad (10.2)
\]

The conditional is eliminated, and now \(b\) will be True if \(r \neq 42\) when the branch would have been entered, and \(r = 42\) in the final state. More precisely, if we let \(cond\) be the original conditional and \(cond'\) be the optimised version, they both satisfy the following assuming \(\neg b\) initially, and \(r_{\text{init}}\) is the initial value of \(r\).

\[
\{\neg b\} \ cond \{r = 42 \land (b \leftrightarrow r_{\text{init}} \neq 42)\} \quad \text{and} \quad \{\neg b\} \ cond' \{r = 42 \land (b \leftrightarrow r_{\text{init}} \neq 42)\}
\]

The transformed code preserves the expected behaviour of rfub.

**Theorem 10.2.** Let \(\text{rfub'}\) be rfub using the transformed conditional from (10.2). Then

\[
\neg\langle\langle 0, x, y, r \land \neg b \rangle\rangle \text{ rfub'}^\sim \langle\langle x = y = r = 42 \land \neg b \rangle\rangle
\]

**Proof.** Straightforward reasoning as in Theorem 10.1. \(\Box\)

If we consider reordering according to the C model and semantics we have given so far, the above state is still not reachable.

**Theorem 10.3.**

\[
\neg\langle\langle 0, x, y, r \land \neg b \rangle\rangle \text{ rfub} \langle\langle x = y = r = 42 \land \neg b \rangle\rangle
\]

**Proof.** More behaviours are possible, but it is still straightforward in our step-based semantics: if the True branch is never taken there is no way for the value 42 to be forwarded to \(x\) and so \(b = \text{True}\). Making the paths explicit (defn. (3.7)) the left process of rfub is equal to:

\[
(r := y; (r \neq 42) ; b := \text{True}; r := 42; x := r) \quad \square \quad (r := y; (r = 42) ; x := r)
\]
The first case allows \( x = y = r = 42 \), following reasoning from Theorem 10.1, but clearly \( b \) holds in any such final state. In the second case \( x := r \) is blocked by \( r := y \) (but not by \( \langle r = 42 \rangle \)), and since there are no (out-of-thin-air) assignments of 42 to \( y \) in the concurrent process the guard will never be True, and so this branch can never be taken. Although reordering \( x := 42 \) before the guard is possible in the first branch (due to forwarding/optimisations), the guard \( \langle r \neq 42 \rangle \) stays in the program as an “oracle”, preventing inconsistent behaviour. The compiler/hardware can allow the store to go ahead, but it must be checked for validity later. The assignment to \( x \) which, in the False branch, depends on \( x \), and the only way that \( x \) can receive 42 in that case is if \( y \) receives 42, but this is not possible as the only instance of 42 is in the True branch, which is already ruled out. □

However, the compiler transformation makes the state reachable.

**Theorem 10.4.** Recalling rfub’ is rfub using the transformed conditional in (10.2),

\[
\langle 0_{x,y,r} \wedge \neg b \rangle \text{ rfub' } \langle x = y = r = 42 \wedge \neg b \rangle
\]

**Proof.** In the left-hand process of rfub’ the assignment \( x := r \) can be reordered to be the first instruction executed, which by forwarding becomes \( x := 42 \). More formally, by Law 9.7 we get the following.

\[
r := y ; b := (r \neq 42) ; r := 42 ; x := r \sqsubseteq x := 42 \cdot (r := y ; b := (r \neq 42) ; r := 42)
\]

(10.3)

Now consider the effect of interleaving \( y := x \) from the second process immediately after this assignment.

\[
\{ 0_{x,y,r} \wedge \neg b \} x := 42 \cdot y := x \cdot r := y \cdot b := (r \neq 42) \cdot r := 42 \cdot \{ x = y = r = 42 \wedge \neg b \}
\]

Because \( r := y \) reads 42 the value assigned to \( b \) is False, and thus \( \neg b \) holds in the final state. The proof is completed by Theorem 5.16. □

The difficulty with this result is that, since \( \neg b \) in the final state, the True branch of the original conditional from rfub could not have been taken (since it contains \( b := \text{True} \)), therefore the False branch was taken, i.e., the condition \( r \neq 42 \) fails, and hence \( r = 42 \). But the only way for \( r = 42 \) to hold is if the True branch is/was executed, containing \( r := 42 \), but this has already been ruled out.

Since rfub’ has a behaviour which rfub does not, it cannot be the case that rfub \( \sqsubseteq \) rfub’, which suggests the compiler transformation is not valid. Essentially, the transformation eliminates a guard and hence breaks a dependency-cycle check.

The question remains, however, whether the compiler transformation (10.2) is reasonable in the presence of the c memory model, and if so what the implications for the memory model are. We show how we can tweak the framework (specifically, increasing the circumstances under which the concept of forwarding can apply) to allow the possible state using the original version of rfub (thus justifying the compiler transformation). However, there are other consequences. We can straightforwardly accommodate either outcome in this framework, and can do so with a clear choice that has enumerable consequences to other code: can guards be used to simplify expressions?

**10.2 Self-fulfilling prophecies (forwarding guards)**

In Defn. (9.1) we defined \( \alpha \bowtie \beta \), for \( \alpha \) an assignment, to update expressions in \( \beta \) according to the assignment. If \( \alpha \) is a guard (or fence) then \( \alpha \bowtie \beta = \beta \). However, it is reasonable, in the sequential world at least, to allow guards to assist in transformations.
We introduce an extended version of forwarding, where \( \alpha \Rightarrow \beta \) returns a set of possible outcomes.

\[
x := e \Rightarrow \alpha = \{ x := e \alpha \}
\]

(10.4)

\[
\langle b \rangle \Rightarrow \{ e \} = \{ \langle e' \rangle \mid b \Rightarrow (e' \leftrightarrow e) \}
\]

(10.5)

\[
\langle b \rangle \Rightarrow x := e = \{ x := e' \mid b \Rightarrow (e' = e) \}
\]

(10.6)

If \( \alpha \) is an assignment it returns a singleton set containing just \( \alpha \Rightarrow \beta \) (10.4), e.g., \( r := 42 \Rightarrow x := r = \{ x := 42 \} \). However, if \( \alpha \) is a guard \( \langle b \rangle \) then \( b \) can be used as context to modify (optimise) \( \beta \), e.g., \( \langle r := 42 \rangle \Rightarrow x := r = \{ x := 42, […] \} \) by (10.5) and (10.6).

We modify the reordering triple defn. (9.2) to accommodate \( \alpha \Rightarrow \beta \) in place of \( \alpha \Rightarrow \beta \).

\[
\beta' \preceq \alpha, \gamma \Rightarrow \beta \quad \text{defn. (9.2)}
\]

Thus we incorporate using the guards in conditionals to justify reordering via Rule 9.3. For instance, following from above, \( x := 42 \langle \langle r = 42 \rangle \rangle \quad \text{defn. (9.2)} \) we can show that a trailing assignment can be used as context to modify (optimise) \( \beta \), e.g., \( \langle r = 42 \rangle \Rightarrow x := r \). We call this use of a guard to simplify a later assignment as a self-fulfilling prophecy, for reasons which will become clear below.

10.3 Behaviour of read-from-untaken-branch with self-fulfilling prophecies

We now return to the behaviour of \( \text{rfub} \), this time allowing self-fulfilling prophecies via forwarding (defn. (10.7)). To highlight the impact this has we note refinement steps that are allowed under SFPs (using defn. (10.7) for the antecedent of Rule 9.3) using \( \llparenthesis \langle \rangle \llparenthesis \rangle \) and steps that are allowed normally (using defn. (9.2) for the antecedent of Rule 9.3) as \( \llparenthesis \langle \rangle \rrparenthesis \). The following theorem stands in contradiction to Theorem 10.3.

**Theorem 10.5.** Allowing self-fulfilling prophecies,

\[
\llparenthesis \langle 0_{x,y} r \land \lnot b \rangle \rrparenthesis \text{rfub} \llparenthesis x = y = r = 42 \land \lnot b \rrparenthesis
\]

(10.9)

**Proof.** Let \( \text{rfub}_1 \) (resp. \( \text{rfub}_2 \)) refer to the first (resp. second) process of \( \text{rfub} \) (defn. (10.1)).

\[
\text{rfub}_1 \llparenthesis \langle r := y \rangle \lnot \text{rfub} \llparenthesis \langle r := 42 \land \lnot b \rangle \rrparenthesis
\]

(10.10)

\[
\llparenthesis \langle r := 42 \rangle \rrparenthesis \llparenthesis x := r := y \rangle \lnot \text{rfub} \llparenthesis \langle r := 42 \land \lnot b \rangle \rrparenthesis \quad \text{by defn. (9.2)}
\]

(10.11)

\[
\llparenthesis x := 42 \land r := y \rangle \lnot \text{rfub} \llparenthesis \langle r := 42 \land \lnot b \rangle \rrparenthesis \quad \text{by defn. (9.7), Law 4.2}
\]

(10.12)

Now we fix the interleaving.

\[
\text{rfub} \llparenthesis \langle x := 42 \land r := y \rangle \parallel y := x \rangle \llparenthesis \langle r := 42 \rangle \rrparenthesis \llparenthesis y := x \rangle \llparenthesis r := y \rangle \llparenthesis \langle r := 42 \rangle \rrparenthesis
\]

(10.13)

This interleaving reaches the specified state.

\[
\{0_{x,y} r \land \lnot b \} \langle x := 42 \rangle \llparenthesis y := x \rangle \llparenthesis r := y \rangle \llparenthesis \langle r := 42 \rangle \rrparenthesis \llparenthesis x = y = r = 42 \land \lnot b \rangle
\]

(10.14)
The proof is completed by Theorem 5.16. □

This theorem shows that the debated outcome of rfub, which is possible under a seemingly reasonable compiler transformation, arises naturally if conditionals are allowed to modify future instructions. Indeed, this is essentially what is used to justify the transformation itself: if the False branch is taken then already \( r = 42 \), so any later use of \( r \) can be assumed to use the value 42. However, in a concurrent, reordering setting, there may be unexpected consequences.\(^7\)

We do not intend to take a stand about what is ultimately the best choice for \( C \); rather we show that whichever choice is taken can be linked to clear principles about whether or not guards should be allowed to simplify assignments in a concurrent setting. Note that we can explain it in a step-based semantics.

### 10.4 Behaviour of out-of-thin-air with self-fulfilling prophecies

Recall the out-of-thin-air example oota\( _D \) (defn. (6.20)).

\[
oota_D \sqsubseteq r_1 := x ; (\text{if}^C r_1 = 42 \text{ then } y := r_1) \parallel r_2 := y ; (\text{if}^C r_2 = 42 \text{ then } x := r_2) \quad (10.15)
\]

Its behaviour, which is intended to be forbidden, is allowed under SFPs, in contrast to Theorem 6.7.

**Theorem 10.6.** Under SFPs, \( \langle 0_{x,y,r_1,r_2} \rangle \circlearrowright \langle x = 42 \land y = 42 \rangle \).

**Proof.** Focus on the left-hand process, and in particular the behaviour when the True branch is taken. The key step depends on \( y := 42 \langle (r_1 = 42) \land y = r_1 \rangle \), that is, the guard can be used to simplify the inner assignment.

\[
\begin{align*}
r_1 := x ; (\text{if}^C r_1 = 42 \text{ then } y := r_1 \text{ else}) & \sqsubseteq r_1 := x ; (\langle r_1 = 42 \rangle) ; y := r_1 \quad (10.16) \\
& \sqsubseteq \uparrow p r_1 := x ; y := 42 \cdot (\langle r_1 = 42 \rangle) \quad (10.17) \\
& \sqsubseteq y := 42 \cdot r_1 := x \cdot (\langle r_1 = 42 \rangle) \quad (10.18)
\end{align*}
\]

Using symmetric reasoning in the second process and interleaving we have the following behaviour.

\[
oota_D \uparrow p x := 42 \cdot y := 42 \cdot r_1 := x \cdot r_2 := y \cdot (\langle r_1 = 42 \rangle) \cdot (\langle r_2 = 42 \rangle) \quad (10.19)
\]

Here both stores have been promoted to the first instruction executed, which are then read into local registers and subsequently satisfy the guards (a “satisfaction cycle” [4]). The postcondition is straightforwardly reached.

\[
\{0_{x,y,r_1,r_2} \} x := 42 \cdot y := 42 \cdot r_1 := x \cdot r_2 := y \cdot (\langle r_1 = 42 \rangle) \cdot (\langle r_2 = 42 \rangle) \{ x = 42 \land y = 42 \} \quad (10.20)
\]

The proof is completed by Theorem 5.16. □

This demonstrates the problematic nature of allowing SFPs, and unifies the known underlying problem with these two related patterns (oota and rfub).

### 11 FURTHER EXTENSIONS

In this section we discuss some other extensions to the model that may be of interest in some domains; however we emphasise that the definition of the memory model does not need to change, we simply make the language and its execution model richer.

\(^7\)Forbidding branches from simplifying later calculations does not prevent all reasonable compiler optimisations, for instance,

\[
(\text{if}^C b \text{ then } \ldots ; r := 42 \text{ else } \ldots ; r := 42) ; x := r \sqsubseteq x := 42 \cdot (\text{if}^C r \neq 42 \text{ then } \ldots \text{ else } \ldots) ; r := 42
\]

This is because there is a definite assignment to \( r \) in both branches.
11.1 Power and non-multicopy atomicity

IBM’s multicore Power architecture [51, 52, 68] (one of the first commercially available) has processor pipeline reorderings similar to Arm [24], but in addition has a cache coherence system that provides weaker guarantees than that of Arm (and x86): (cached) memory operations can appear in different orders to different processes. For instance, although on ARM the instructions $x := 1$ and $y := 1$ may be reordered in the pipeline of a particular processor, whichever order they occur in will be the same for every other process in the system. On Power, however, one process may see them in one order and another may see the modification in the reverse order (assuming no fences are used). This extra layer of complexity is introduced through cache interactions which allow one processor that shares a cache with another to read writes early, before the memory operation is fully committed to central storage [68].

Programmers targeting implementations on Power architectures must take these extra behaviours into account (C accommodates the lack of multicopy atomicity to be compatible with this hardware). A formalisation of the Power cache system, separate from the processor-level reordering, and compatible with the framework in this paper, is given in [14], which is based on an earlier formalisation of the Power memory subsystem given in [68]. The cache subsystem, and its formalisation in [14] sits conceptually above the processes within the system, and stores and loads interact with it rather than with the traditional variable-to-value mapping. As such, local reorderings, and the influence of ordering constraints and fences are still relevant. However under the influence of such a system, no code can be assumed to be atomic-syntax-structured (Defn. (7.1)), and thus traditional syntax-based reasoning techniques will not directly apply; however by instituting the system of [14] the consequence on behaviours can be determined. We do not devote more time to this feature of the C model in this paper for several reasons.

- Power is still subject to processor reorderings which are captured by the concepts herein; the memory subsystem is governed by separate mechanisms;
- Power is the only commercially available hardware that exhibits such behaviours. Arm once allowed them, but no manufacturer ever implemented them on a real chip, and Arm has since removed these behaviours from its model [67]. A large reason for omitting the possibility of such weak behaviours was due to the complexity of the induced axiomatic models [1], which were difficult to specify and reason about. Arm is generally considered one of the faster architectures, and does not appear to suffer a significant penalty due to not having a similarly weak cache coherence system. (Intel’s Itanium architecture, and mooted memory model (e.g.[81]), was also intended to allow these weak behaviours; however it ceased production in 2020.)
- In practice, Power’s weak behaviours are so difficult to reason about that developers make heavy use of fences to eliminate the effects; and as a result whatever performance gains there may have been are eliminated.
- The behaviours that arise are entirely to do with that micro-architectural feature and not due to compiler transformations or processor reorderings. Reasoning about C memory model features that affect local code (for, say, x86) architectures carries over identically to reasoning about local code in Power.
- Although, theoretically, under the C memory model a compiler could instrument code transformations that mimic the behaviour of Power’s cache system on architectures that do not exhibit them natively, this seems highly unlikely; therefore, only developers targeting Power will ever experience the resulting complexity (which arguably can and must be removed by the insertion of fences).
Outside of such considerations, the C model as we have presented it is relatively straightforward; the behaviour introduced by Power’s cache system is completely separate to pipeline reordering and compiler transformations. It seems unfortunate to complicate the entirety of the C memory model to accommodate one architecture, when its effects can be captured in a separate memory subsystem specification (which can be ignored by developers targeting different architectures). Hence we recommend keeping the extra behaviours induced by this separate mechanism, peculiar to a single currently-in-production architecture, separately specified within the model; we point to [14, 65, 68] as examples of how this can be done, which fulfil similar roles to time-stamped event structures in [42] and the shared action graph of [80].

11.2 Incorporating compiler transformations

Any possible compiler transformation can be straightforwardly incorporated into our framework as an operational rule. For instance, if pattern is some generic code pattern that can be transformed into pattern’ then this can become a rule pattern \( \rightarrow \) pattern’, i.e., a silent transformation that can occur at any time (an example of such a transformation might be to refactor a loop). The downside of including such transformations within the semantics is, of course, depending on the structural similarity of pattern and pattern’, one cannot expect to reason about pattern using syntax-directed proof rules (one has broken the principle of atomic-syntax-structured code, Defn. (7.1)). Of course, trace-based approach can still be applied.

As an example, consider a transformation discussed in Sect. 10.1, which simplifies and removes a conditional. This can be expressed as an operational rule that applies in some circumstances.

**Rule 11.1 (Eliminate conditional).**

\[
(\text{if} \ C \ r \neq n \ \text{then} \ b := \text{True} \ ; \ r := n) \ \rightarrow \ (b := (r = n) \ ; \ r := n)
\]

As discussed in Sect. 10.1, allowing this transformation has significant effects on behaviours in a wider context. Consider also transformations to eliminate redundant loads or stores, the simplest instrumentation of which are given by the following rules.

**Rule 11.2 (Load coalescing).**

\[
r_1 := x \ ; \ r_2 := x \ \rightarrow \ r_1 := x \ ; \ r_2 := r_1
\]

**Rule 11.3 (Write coalescing).**

\[
x := e_1 \ ; \ x := e_2 \ \rightarrow \ x := e_2
\]

These transformations eliminate an interaction with main memory. Rule 11.2 reduces the number of behaviours of the program since \( r_2 \) will always take the same final value as \( r_1 \), whereas in the original code it is possible for them to receive different final values. The transformation encoded in Rule 11.3 reduces the overall behaviours of the system as a parallel process can never receive the value of \( e_1 \) (of course, these transformations could be made dependent on memory ordering constraints using, for instance, the \( \geq \) relation). We believe it should be outside of the scope of the definition of C memory model, and certainly outside the scope of this work, to consider every possible transformation of every possible compiler; however we have provided a framework in which the consequences of a particular transformation can be relatively straightforwardly assessed, separately to the specification and principles of the memory model itself. In particular this may feed in to the development of verified compilers, and the development of a bespoke set of transformations that are valid within concurrent systems.

12 RELATED WORK

The development of the C (and C++) memory model is ongoing and governed by an ISO committee (but heavily influenced by compiler writers [53]), covering the vast range of features of the
language itself and including a semi-formal description of the memory model. Boehm and Adve [6] were highly influential initially, building on earlier work on memory model specifications (e.g., [3, 20, 25, 26, 41, 47, 70]). Since then many formal approaches have been taken to further understand the implications of the model and tighten its specification, especially the works of Batty et. al [4, 5, 38] and Vafeiadis et. al [43, 45, 46, 77]. The model abstracts away from the various hardware memory models that C is designed to run on (e.g., Arm, x86, Power, RISC-V, SPARC), leaving it to the compiler writer to translate the higher-level program code into assembler-level primitives that will provide the behaviour specified by the C model. This behaviour is described with respect to a cross-thread “happens-before” order, which is influenced by so called “release sequences” of events within the system as a whole. As a formalism this is difficult to reason about, and in particular, it removes the ability to think thread-locally – whether or not enough fences or constraints have been placed in a thread requires an analysis of all other events in the system, even though, with the exception of the Power architecture (see Sect. 11.1), any weak behaviours are due to local compiler transformations or instruction-level parallelisation at the assembler level. Our observations of a myriad of discussions on programming discussion boards online is that programmers tend to think in terms of local reorderings, and appealing to cross-thread concepts is not a convenient abstraction. The framework we present here is based on a close abstraction of instruction-level parallelisation that occurs in real pipelined processors or instruction shuffling that a compiler may perform. For simple programs, where enough synchronisations have been inserted to maintain order on the key instructions, reasoning can be shown to reduce to a well-known sequential form; or specific reorderings that are problematic can be elucidated. The underlying semantics model is the standard interleaving of relations on states (mappings from variables to values). We argue this is simpler and intuitive – as far as instruction reorderings can be considered so – than the current description in the C standard. Part of the complication of the standard arises from handling the complexity of the Power cache coherence system, which cannot be encoded in a thread-local manner; however those complications can be treated separately [14, 65, 68], and in any case, the Power model also involves instruction-level parallelism governed by the same principles as the other major architectures (Arm, x86, RISC-V, SPARC).

In comparison with other formalisms in the literature [8, 57, 62], many use an axiomatic approach (as exemplified by [1]), which are necessarily cross-thread specifications based on the happens-before relationship, many use a complex operational semantics, and many combine the two. The Promising semantics [42, 49] is operational in flavour but has a complex semantics [8] involving time-stamped operations and several abstract global data structures for managing events. In these frameworks reasoning about even simple cases is problematic, whereas in our framework the effects of reordering can be analysed by reduction rules at the program-level (Sect. 4), and our underlying model is that of the typical relations on states and so admits standard techniques (Sect. 5). A recent advance in reasoning for the C memory model is that of Wright et. al [80], but that framework appeals to a shared event graph structure, and does not consider memory fences or sc constraints. Very few of the formalisms surveyed have a simple way of address consume (con) constraints (Sect. 8.2); we also argue that our formal approach to understanding pathological behaviours such as out-of-thin-air (Sect. 6.3) and read-from-untaken-branch (Sect. 10.1) provides a clearer framework for understanding and addressing their consequences.

An overarching philosophy for our approach has been that of a separation-of-concerns, meaning that a programmer can consider which mechanisms for enforcing order should suffice for their concurrent code; of course, if their ordering mechanisms are embedded in complex expressions that may be optimised (Sect. 8) or incrementally evaluated (Sect. 7) then the picture becomes more complex, but this can be analysed separately, and without regard to how such features interact with cross-thread, complex, abstract data structures controlling events. The reordering framework we
present here is based on earlier work [11, 12, 14], which provides a model checker (written in Maude [9]) and machine-checked refinement rules (in Isabelle/HOL [60, 64]) for the language in Sect. 3.2 (i.e., ignoring the possibility of incremental evaluation and optimisations) with forwarding (Sect. 9). We straightforwardly encoded the definition of the C memory model (Model 2.6) in the model checker and used it on the examples in this paper as well as those provided by the Cerberus project [21]. The framework has provided the basis for other analyses involving security [15, 73, 78] and automated techniques [16, 71]

13 CONCLUSIONS
We have given a definition of the C memory model which keeps the fundamental concepts involved (fences, ordering constraints, and data dependencies) separated from other aspects of the language such as expression evaluation and optimisations, which are present regardless of whether or not the memory model is considered. Provided programmers keep to a reasonable discipline of programming that aids analysis of concurrent programs, i.e., program statements are generally indivisible (at most one shared variable per-expression), our framework facilitates structured reasoning about the code. This involves elucidating the effect of orderings on the code as-written, and then applying existing techniques for establishing the desired properties. We argue that our framework more closely expresses how programmers of concurrent code think about memory model effects than the abstraction given in the current standard (cross-thread happens-before relationships and release sequences). This is largely because the effects that a C programmer needs to consider are compiler reorderings of instructions for efficiency reasons, or architecture-level reorderings in instruction pipelines. The C language is rich in features and any claim to a full semantics of arbitrary C code with concurrency requires a full semantics of C in general, and as far as we are aware this has not been fully realised as yet; but we intend that our approach can be relatively straightforwardly incorporated into such by virtue of its separation of concerns - the fundamental properties of the memory model are universal and consistent even in the presence of complicating factors.

We note that the difficulties that arise in the attempt to formalise the C memory model stem from the tension between well-established compiler transformations as well as the need to support a multitude of hardware-level memory models seamlessly versus the well-known intricacies of programming correct shared-variable algorithms [48]. This will be an ongoing balancing act that involves many competing factors, especially and including efficiency, and, increasingly, safety and security [50]; if we were to take a position, it would be that sections of code – hopefully, relatively small and localised – can be protected from arbitrary transformations from compiler theory and practice. For instance, a C scoping construct concurrent { ... } which is compiled with minimal optimisations or reorderings, regardless of command-line flags such as -O. The C standard may then be able to provide guarantees about executions for such delimited code, while also allowing the programmer flexibility to make use of optimisations where they have determined they are applicable.

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LIFTING FROM ACTIONS TO TRACES AND COMMANDS

Throughout the paper we have used several functions and definitions based on actions, which for the most part are straightforwardly lifted to commands and traces. For completeness we give these below.

A.1 Extracting variables

For any function fn(.) that simply collects syntax elements into a set (i.e., fv(.), vw(.), rv(.), [], [], etc.) and is defined over instructions can be straightforwardly lifted to commands, actions and traces in the following generic pattern.

\[ fn(\text{nil}) = \emptyset \]  \hspace{1cm} (A.1)
\[ fn(\overline{a}) = \bigcup_{a \in \overline{a}} fn(a) \]  \hspace{1cm} (A.2)
\[ fn(c_1 \cap c_2) = fn(c_1) \cup fn(c_2) \]  \hspace{1cm} (A.3)
\[ fn(c_1 ; c_2) = fn(c_1) \cup fn(c_2) \]  \hspace{1cm} (A.4)
\[ fn(c_{\alpha}^\wedge) = fn(c) \]  \hspace{1cm} (A.5)
\[ fn(\langle \rangle) = \emptyset \]  \hspace{1cm} (A.6)
\[ fn(\alpha \compose t) = fn(\alpha) \cup fn(t) \]  \hspace{1cm} (A.7)

A.2 Lifting forwarding/reordering triples

Forwarding (see Sect. 9) an action \( \alpha \) to action \( \beta \) is defined below. Assume \( x \neq y \).

\[ \alpha \rangle (y^{ocs} := f) = y^{ocs} := (\alpha \rangle f) \]
\[ \alpha \rangle (\langle b \rangle) = \langle (\alpha \rangle b) \]
\[ \alpha \rangle f = f \]
\[ \alpha \rangle v = v \]
\[ \alpha \rangle (\ominus f) = \ominus (\alpha \rangle f) \]
\[ \alpha \rangle (e_1 \ominus e_2) = (\alpha \rangle e_1 ) \ominus (\alpha \rangle e_2) \]
\[ x^{ocs_1} := e \rangle y^{ocs_2} = y^{ocs_2} \]
\[ x^{ocs_1} := e \rangle x^{ocs_2} = e \]

Given \( \alpha \) is an assignment \( x^{ocs} := e \) then \( \alpha \rangle \beta \) essentially replaces references to \( x \) (with any constraints) by \( e \).
The reordering relation can be lifted from actions to commands straightforwardly as below.

\[ \beta' \triangleleft \text{nil} ^{M} \beta \triangleq \beta' = \beta \]  
(A.8)

\[ \beta' \triangleleft \alpha \triangleleft \beta \triangleq \alpha \triangleleft \beta' \land \beta' = ^{C} \alpha \triangleleft \beta \]  
(A.9)

\[ \beta'' \triangleleft c_1 ; c_2 ^{M} \beta \triangleq \exists \beta' \oplus \beta'' \triangleleft c_1 ^{M} \beta' \land \beta' \triangleleft c_2 ^{M} \beta \]  
(A.10)

\[ \beta' \triangleleft c_1 \cap c_2 ^{M} \beta \triangleq \beta' \triangleleft c_1 ^{M} \beta \land \beta' \triangleleft c_2 ^{M} \beta \]  
(A.11)

\[ \beta' \triangleleft c_{m} ^{*} \triangleleft \beta \triangleq \forall i \in N \Rightarrow \beta' \triangleleft c_{i} ^{M} \beta \]  
(A.12)

### B MIXING INCREMENTAL AND NON-INCREMENTAL EVALUATION

In Sect. 7 we gave a semantics for evaluating instructions incrementally, as opposed to treating instructions as indivisible in Sect. 3.2. In this section, for completeness, we show how to mix both possibilities within the syntax of \( \text{IMP} + \text{pseq} \).

We define an instruction \( \mathcal{I} \) to be one of the three basic types of assignment, guard and fence, and an action \( \mathcal{A} \) to be a list of instructions (written \( \sqsubseteq \mathcal{C} \mathcal{I} \)). Actions are the basic type of a step in the operational semantics. We define a “specification instruction” to pair a basic instruction \( \mathcal{I} \) with a designation as to whether it is divisible or indivisible, i.e., whether it is to be executed incrementally or as a single indivisible step. Finally, within the syntax of \( \text{IMP} + \text{pseq} \), instead of a list of actions \( \sqsubseteq \mathcal{A} \) as the base type (defn. (3.1)), we allow a statement \( \mathcal{S} \), which is a list of specification instructions.

\[ \mathcal{I} \in \text{Instr} \quad \mathcal{A} \in \text{Action} \quad \mathcal{I}^{+} \in \text{SpecInstr} \quad \mathcal{S} \in \text{Statement} \]

\[
\begin{align*}
\mathcal{I} & ::= \ x := e \mid (\{e\}) \mid f \\
\mathcal{A} & ::= \ ? \mathcal{I} \\
\mathcal{I}^{+} & ::= \mathcal{I} \times (\text{divisible} \mid \text{indivisible}) \\
\mathcal{S} & ::= \mathcal{I}^{+}
\end{align*}
\]

This gives a significant amount of flexibility in describing the execution mode of composite actions, for instance, \( \langle (x := y), \text{indivis} \rangle, (x := y + z, \text{divis}) \) is a statement that calculates whether \( x = y \) in the current state, and then incrementally evaluates \( y + z \) before assigning the result to \( x \). Of course, this level of flexibility is not necessary for the majority of cases, and syntactic sugar can be used to cover the commonly occurring cases, in particular, letting a singleton list of specification instructions be written as a single specification instruction; and conventions for distinguishing between divisible and indivisible versions of instructions.

We lift defn. (7.6) for indivisible instructions to the new types.

\[
\begin{align*}
\text{indivis}(\langle \mathcal{I}, \text{indivisible} \rangle) & = \text{True} \\
\text{indivis}(\langle \mathcal{I}, \text{divisible} \rangle) & = \text{indivis}(\mathcal{I}) \\
\text{indivis}(\mathcal{S}) & \triangleq \forall \mathcal{I}^{+} \in \mathcal{S} \Rightarrow \text{indivis}(\mathcal{I}^{+})
\end{align*}
\]

Any specification instruction tagged indivis is indivisible, while a specification instruction tagged divis is divisible if its instruction is, but is otherwise indivisible.

The relevant operational semantics for specification instructions and statements is as follows.

\[
\begin{array}{c}
\xrightarrow{\mathcal{A}} \\
\leftarrow
\end{array}
\]

\[
\begin{align*}
\mathcal{I} & \xrightarrow{\mathcal{A}} \mathcal{I}' \\
(\mathcal{I}, \text{divisible}) & \xrightarrow{\mathcal{A}} (\mathcal{I}', \text{divisible})
\end{align*}
\]
Rule B.1 states that any instruction tagged divisible can take an incremental execution step according to the evaluation rules in Sect. 7. This is used to build Rule B.2 for a statement $s$, where specification instructions within $s$ are executed incrementally from left to right: the first divisible specification instruction ($i$) in $s$ may take a step, which becomes a step of the statement. When all instructions within $s$ are indivisible a final, single, indivisible step is taken. This action is formed by simply stripping the indivis/divis tags from the specification instructions, i.e., $\text{strip}((i, \_)) \equiv i$, which is lifted to statements by applying $\text{strip}$ onto each element, i.e., $\text{strip}(s) \equiv \text{map} (\text{strip}, s)$.

A compare and swap command (defn. (3.9)) can be redefined to incrementally evaluate its arguments before executing an indivisible ("atomic") test-and-set step.

$$\text{cas}(x, e, e') \equiv \langle (\langle x = e \rangle, \text{divis}), (x := e', \text{divis}) \rangle \sqcap (\langle x \neq e \rangle, \text{divis})$$

In the successful case first $e$ is evaluated to a value $v$, then $e'$ is evaluated to a value $v'$, and finally the action $\langle x = v \rangle x := v'$ is executed (the divis tags are stripped). This means that $e$ and $e'$ can be incrementally evaluated, but the final test/update remains atomic.