FPGA-optimized Hardware acceleration for Spiking Neural Networks

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Abstract—Artificial intelligence (AI) is gaining success and importance in many different tasks. The growing pervasiveness and complexity of AI systems push researchers towards developing dedicated hardware accelerators. Spiking Neural Networks (SNN) represent a promising solution in this sense since they implement models that are more suitable for a reliable hardware design. Moreover, from a neuroscience perspective, they better emulate a human brain. This work presents the development of a hardware accelerator for an SNN, with off-line training, applied to an image recognition task, using the MNIST as the target dataset. Many techniques are used to minimize the area and to maximize the performance, such as the replacement of the multiplication operation with simple bit shifts and the minimization of the time spent on inactive spikes, useless for the update of neurons’ internal state. The design targets a Xilinx Artix-7 FPGA, using in total around the 40% of the available hardware resources and reducing the classification time by three orders of magnitude, with a small 4.5% impact on the accuracy, if compared to its software, full precision counterpart.

Index Terms—SNN, FPGA, LIF, STDP

I. INTRODUCTION

Artificial Neural Networks (ANN) are used in many application domains, including industrial automation and robotics [1], healthcare [2], automotive [3] and safety-critical systems [4]. Although several applications resort to ANNs, their increasing complexity requires powerful hardware resources. Indeed, An ANN is composed of several building blocks (i.e., neurons) working in parallel during inference and training. Their operation requires tens of billions of operations, making these models extremely compute-intensive. Moreover, for each process, data must be fetched from memory, pushing the memory bandwidth to its limit [5]. In this context, it is clear that general-purpose CPUs are not the most suitable hardware platform for ANN applications, with their limited parallelism, making the GPUs one of the most appealing alternatives to implement these complex models.

However, the rapid expansion of the Internet-of-Things (IoT) [6] introduces new challenges. The high cost of moving information from low-performance peripheral nodes to high-performance computing infrastructures equipped with powerful GPUs, is pushing for additional computing capabilities at the edge [7]. In this scenario, following the common trend of moving from general-purpose architectures toward heterogeneous multi-core architectures [8], ANNs need acceleration provided by alternative technologies, such as FPGAs that are flexible and reprogrammable.

Classical ANNs, e.g., Convolutional Neural Networks (CNN) or Recurrent Neural Networks (RNN) are characterized by non-linear activation functions applied to a weighted sum of real numbers. This kind of computation strongly increases the complexity of hardware acceleration. Spiking Neural Networks (SNNs) are an emerging class of ANNs in which information is exchanged between neurons in the form of binary spikes. SNNs have shown a great potential for achieving high accuracy, requiring a small area footprint, and thus potentially limiting the power/energy consumption due to their sparse spike-based operations [9]. SNNs provide a better-inspired model to the human brain and reduce the width of the connections between neurons to a single bit. Moreover, SNNs can perform unsupervised learning with unlabeled data using the Spike-Timing-Dependent Plasticity (STDP), which is important in several application domains [10].

This paper presents a new low-cost Xilinx-based FPGA SNN hardware accelerator. The proposed architecture introduces hardware optimizations that reduce resources to enable high throughput during inference. The main contributions can be summarized as follows:

- A Simplified neuron architecture based on the Leaky Integrate and Fire model [11] avoiding the use of costly multipliers. By properly tuning the model’s parameters, multiplications are replaced with simple shift operations with negligible loss in the model accuracy. This enables high parallelism in the accelerator.
- The update of the neurons is step-based to make the control unit of the accelerator as simple as possible, thus reducing its area.
- Flexible parallelism architecture. The architecture is general and can be easily customized based on the available hardware resources. This makes it possible to trade-off inference throughput with FPGA occupation.

The capabilities of the hardware accelerator have been tested on a network optimized to work with the MNIST dataset [12]. The training part is performed offline with a high-resolution model, while inference is performed on the accelerator with the simplified neuron structures. Experimental
results show that this simplified model can maintain high accuracy comparable with high-precision models, provide high throughput, and maintain low hardware complexity.

The remaining of the paper is organized as follows: Section II overviews the basic SNN concepts required to understand the behavior of the accelerator. Section III introduces the designed architecture. Section IV experimentally evaluates the capability of the proposed accelerator and section V summarizes the main contributions of the paper and overviews future activities.

II. BACKGROUND

SNNs were born to mimic the behavior of a real brain. A biological neuron is characterized by a membrane potential, which can be increased or decreased by input signals, depending on whether an excitatory or inhibitory neuron transmits the signal. If the potential exceeds a threshold, the action potential takes place. The action potential is a sudden increase in the membrane voltage, which then rapidly tends towards its rest value. The resulting voltage spike propagates to other neurons, modifying their membrane potential. SNNs emulate the described behavior using binary spikes. In particular, if the membrane potential exceeds the threshold, a spike is generated, i.e., the neuron fires. Otherwise, no spike is observed at the output of the neuron. Consequently, time becomes part of the model and encodes more complex information than the one brought by a single spike.

The temporal evolution of the membrane potential in SNNs must be sufficiently simple to implement an efficient hardware accelerator. Many mathematical models have been developed in the last decade, with different degrees of biological plausibility.

The Hodgkin-Huxley model is the most accurate and complex and describes in detail the behavior of ions within the nerve membrane. It is very realistic but too complex for hardware implementations.

The Izhikevich model exploits mathematical properties to simplify the Hodgkin-Huxley model, and some works use this model in hardware accelerators. However, our architecture aims to reduce the area occupation, and the Izhikevich model is too complex to accomplish this goal.

The simplest available model in the literature is the Integrate and Fire (IF) model, which treats the membrane as an ideal capacitance. However, this model is too approximated and leads to behaviors quite different from those observed in a biological neuron.

Eventually, the Leaky Integrate and Fire (LIF) model is a good trade-off between simplicity and biological plausibility. It treats the membrane as a leaky capacitance, including a resistive part that forces the voltage to a rest value in the absence of input stimuli. Equation 1 describes the evolution of the potential in absence of input stimuli, where $V(t_0)$ is the starting value of the membrane potential, which then tends towards $V_{rest}$, $t_0$ is the time instant in which one or more input spikes are received, and $\tau$ is the exponential decay time constant, affected by the membrane capacitance and parasitic resistance.

\[ V(t) = V_{rest} + (V(t_0) - V_{rest}) \cdot e^{-\frac{t-t_0}{\tau}} \]  

When an input spike arrives, the potential increases or decreases according to the excitatory or inhibitory weight of the input synapse. The complete mathematical analysis of the membrane potential temporal evolution is reported in [19].

This paper considers as a reference the LIF implementation developed by Peter Diehl and Matthew Cook, a seminal work for SNNs applied to handwritten digits recognition. The model is simplified to a current-based version, less realistic from the biological standpoint, but preferable to target a hardware accelerator. The result is similar to the one reported in [21]. In this reference application, the employed model’s parameters are $V_{rest} = -65mV$ and $\tau = 100ms$. The reader may refer to [20], and [19] for a detailed explanation of how these parameters were obtained.

The method used to train the network is the STDP. This is an unsupervised method, and to this day, it seems the most promising solution from a biological emulation point of view. The training task is performed offline, and the accelerator expects valid hyperparameters (i.e., neuron weights and thresholds) before performing inference. For this reason, the choice of the specific learning algorithm is left to the user, who can try different solutions, testing them directly in-field.

III. ARCHITECTURE

This section overviews the different building blocks of the proposed accelerator, focusing on the optimizations introduced to reduce the hardware complexity and improve the performance. Figure 1 presents the developed architecture. For the sake of readability, the figure presents an example with a single layer of three neurons.

A. Input and output interfaces

Both the input and output interfaces are included in the accelerator as dedicated components.

The input interface comprises a buffer to store the input data (i.e., pixels of an image). As discussed before, the network works with binary spikes. However, data in the real world are coded in numeric form. So to convert such data into proper input spikes sequences that the network can elaborate an interface is required. The sequences of spikes are created as random Poisson processes with an average frequency that corresponds to the numeric value in the input. To generate the spikes in the form of a Poisson process, an onboard generator of random numbers is necessary. To reduce the complexity, pseudorandom numbers are generated using a Linear Feedback Shift Register (LFSR). An LFSR generates pseudorandom numbers with a period of at most $2^N$, where $N$ is the number of bits of the shift register. Xilinx provides a detailed table to choose the taps to maximize the LFSR period.

While during the training phase, an independent random number for each input guarantees a better learning process,
during inference a single random number can be used to generate spikes for all inputs (i.e., input data with the same value are associated with the same train of spikes). This means that a single LFSR can feed the entire network. In this way the area of the generator is reduced, and therefore a larger LFSR can be used to increase the period.

The output interface consists of counters, one counter for each neuron in the output layer. Each counter increments whenever it receives a spike. Having each neuron associated with a specific label, the inference is performed considering the label associated with the most significant amount of spikes.

### B. Network architecture

The architecture of the accelerator is modular and can be synthesized for a network composed of an arbitrary number of layers, fully connected to form a feed-forward structure.

The network elaborates the sequence of spikes step by step. A central control unit (NETWORK CU) moves the elaboration from one stage to the next one when all layers are ready. Figure 1 shows the signal LAYER READY used for this task. Additionally, it keeps track of the number of processed steps (CYCLES_COUNTER).

Each layer consists of a certain number of neurons updated in parallel. Each neuron must elaborate a set of excitatory and inhibitory spikes. Excitatory spikes (INPUT_SPIKES) are those generated from the input interface (see subsection III-A), while the neurons themselves generate the inhibitory spikes (INHIBITORY_SPIKES). To save area, each neuron can elaborate a single spike at a time (see subsection III-C). Therefore, there is a need to feed the spikes one by one into all the neurons in parallel. This is obtained through three dedicated blocks (SELECT_EXC_SPIKES, SELECT_INH_SPIKES, and EXC_INH_MUX) and a control unit to manage the selection (LAYER CU).

Performing a statistical analysis on the elaboration steps considering all images available in the MNIST dataset, one can see that on average less than the 1% of the elaboration cycles present active spikes and are helpful for the membrane potential update (Figure 2). A similar result holds for the inhibitory spikes.

![Network architecture](image)

**Figure 1. Network architecture**

![Statistics of active elaboration steps](image)

**Figure 2. Statistics of the active elaboration steps (i.e., cycles with at least one spike) on all images of the MNIST dataset. Obtained values have been computed with a window of 3,500 elaboration steps.**
2) Exponentially decay the potential in absence of input spikes, following Equation 1.
3) Reset the potential to $V_{\text{reset}}$ when the threshold is exceeded (V_MUX and V_RESET signals);
4) Reset the potential to $V_{\text{reset}}$ at the end of a complete test to prepare the network to receive a new independent set of data (V_RST_N).

A first optimization introduced to simplify the neuron’s structure consists in translating the rest potential from its nominal value $V_{\text{rest}} = -65.0\, mV$ to $V_{\text{rest}} = 0\, mV$.

This optimization has a positive effect on the complexity of the architecture. Equation 1, governing the behavior of the neuron, is simplified as follows:

$$V(t) = V(t_0) \cdot e^{-\frac{t-t_0}{\tau}}$$

(2)

Following Equation 1 and working with positive and negative weights (related to excitatory and inhibitory connections), the membrane potential assumes values in an interval centered on $V_{\text{rest}}$. If $V_{\text{rest}} = -65.0\, mV$ (see section II), the parallelism used to represent this information must be sufficient to define a voltage range with negative values lower than $-65.0\, mV$. Moving $V_{\text{rest}}$ to $0\, mV$ allows representing only the actual range of variability of the potential, reducing the required parallelism. To interpret the biological meaning of the potential, an offset of $+V_{\text{rest}}$ must be applied to restore the original information at the end of the computation.

Figure 3 shows the datapath of a single neuron. This is associated with a control unit, in charge of deciding which kind of update is required among the four operations mentioned above.

The architecture of the neuron is minimal. The largest components are the signed adder/subtractor (UPDATE_ADD_SUB) and the signed comparator (FIRE_CMP). The first block is used both to add the positive or negative weights to the membrane potential and to compute the exponential decay in a step-based fashion, as:

$$V[n] = V[n-1] - V[n-1] \cdot \frac{\Delta t}{\tau}$$

(3)

where $n$ represents the current elaboration step and $\Delta t$ is approximated to a negative power of two to be able to compute the multiplication as a simple shift. The second block is needed to evaluate if the membrane potential exceeds the threshold.

D. Neuron internal parallelism

Analytically determining the internal neuron parallelism is a complex task that depends on the number of spikes the neuron receives. Through the synapse weights affect the maximum and the minimum value that the membrane potential can assume. The problem here is that their distribution is random.

To correctly size this parameter for a specific application, the first step consists in determining an activity statistic, i.e., how many excitatory or inhibitory spikes are active at the same time. Figure 4 shows the distribution of the active spikes within a single elaboration step on the considered dataset. By knowing or estimating the maximum absolute value of the excitatory and inhibitory weights, it is possible to estimate the required parallelism. In this case, a feasible knob to reduce the parallelism is the activity of the inputs and the neurons. The lower it is, the lower is the required parallelism.

![Fig. 3. Neuron datapath](image)

![Fig. 4. Statistics of the active spikes per elaboration cycle on all images of the MNIST dataset.](image)

However, this analysis alone is not sufficient to precisely estimate the required parallelism because it considers a single elaboration step. The probability of having two or more subsequent steps with active spikes is not negligible and the exponential decay could not be sufficient to compensate the increase or decrease introduced by the synapse weights. For this reason, an empirical analysis is performed to evaluate the overflow errors concerning different parallelisms. Figure 5 shows the results, obtained with parallelism that ranges between five and thirty-two bits. The red dashed line indicates the parallelism which corresponds to zero overflow errors. In this case, it is 16 bit.
One possible alternative is to set the parallelism to a fixed value and to saturate the voltage to the maximum and minimum values when required.

E. Memory requirements

The memory requirements of the accelerator are given by:
- Model parameters: reset potential, inhibitory weight.
- Hyperparameters: excitatory weights, thresholds.
- Status of the neuron: membrane potential.

The reset potential and inhibitory weight are the same for the entire layer, so each of them requires a single memory element, be it an internal register or a memory location. They both have the exact parallelism used inside the neurons, in this case 16 bits.

The threshold must be considered a hyperparameter since it is modified during the training to keep the spiking activity uniform between the various neurons. See [20] for more details. Each neuron contains a dedicated register \(V_{TH\_REG}\) to immediately access its specific threshold value to compare it with the membrane potential.

The membrane potential itself has a dedicated register inside the neuron \(V_{REG}\).

Finally, the main memory contribution is given by the excitatory weights. Each neuron is associated with several weights equal to the number of inputs, so the total amount of weights is generally large. As a consequence, it is not possible to store weights using registers as memory elements. A set of dedicated block RAMs (BRAMs), available in the Xilinx FPGAs, are used to store this information. The parallelism of the BRAMs and the interconnections required to connect the neurons with these memory blocks are the main parameters that limit the maximum parallelism of the accelerator. In other words, the number of weights that can be accessed simultaneously determines the number of parallel computations performed.

To reduce the memory occupation, a quantization of the weights have been performed. An analysis similar to the one reported in Figure 5 was carried out. This time the accuracy has been considered instead of the overflow errors. Different parallelisms have been considered, varying the length of the decimal part and evaluating the accuracy. The result is that three decimal bits are sufficient, with total parallelism of 5 bits for the weights and 16 bits for the neurons. Applying this memory reduction quantization allows accessing more weights in parallel: when accessing a memory word, the smaller is the weights parallelism, the more weights will be contained in the word itself.

IV. EXPERIMENTAL RESULTS

A. Experimental setup

The dataset chosen to evaluate the model is the MNIST [12]. It consists of images representing handwritten digits in a black and white format, with a resolution of 28x28 pixels. The 784 pixels composing the image are provided as input to the spikes generator. Each pixel is represented as an eight-bit integer number.

The temporal step used for the elaboration is \(dt = 100\mu s\). Each pixel is converted into a sequence of spikes of duration \(\Delta t = 350ms\), as in [20], that results in a number of elaboration steps coming from:

\[
\frac{\Delta t}{dt} = \frac{350ms}{0.1ms} = 3500
\]

The network architecture considered for the evaluation consists of a single layer of 400 neurons. The membrane potential of each neuron is reset to its rest potential at the end of each image. The network is trained as a python model using STDP, with full precision. Once obtained the values of weights and thresholds, the model is evaluated in test mode. The model proposed in [20] has been implemented using the brian2 [24] SSN simulator and is taken as a reference to evaluate the impact of the different simplifications introduced to develop the hardware accelerator.

B. Accuracy results

Table I shows a comparison of the accuracy for growing degrees of simplification. It is worth mentioning that the obtained accuracy is lower than other state of the art SNNs, also for the reference model. This is because the chosen structure, with a single layer of neurons, is not an optimal solution. Nevertheless, the goal here is not to show the effectiveness of the model that has been already proven in [20] and [21], with more optimized multi-layer structures, but to study the impact that the different simplifications applied to minimize the area have on the overall accuracy.

| Target                                      | Training | Inference |
|---------------------------------------------|----------|-----------|
| Peter Diehl [20]                            | 80.54%   | 78.58%    |
| Current-based full precision                | 80.22%   | 77.16%    |
| Current-based 1 LFSR                        | -        | 74.97%    |
| Current-based finite precision              | -        | 73.96%    |

First of all, the training accuracy is reported only for the reference and the current-based full precision models. In fact, the training is always performed in full precision and then the various simplifications are applied only during inference, for which the accelerator is designed. Table I shows that:

1) Changing the model from a conductance-based solution to a lighter current-based alternative has no significant impact on the training phase and implies a relatively small 1.42% reduction during inference.

2) Using a single random number generator in the input interface, (Current-based 1 LFSR in Table I), causes an additional 2.19% accuracy reduction.

3) Finally, working with an internal parallelism of 16 bits and quantizing the weights down to a 5 bits width implies a further 1.01% accuracy decrease.

So the overall accuracy reduction of the completely simplified model, when compared to the reference one, is around 4.5%, which is more than acceptable considering the substantial hardware simplification.
C. Area and performance results

The designed accelerator has been synthesized on a medium-size Xilinx Artix-7 FPGA. Table II shows the required hardware resources. The last row summarizes all the available components. Overall, the FPGA usage is around 55% for the LUTs, 25% for the FFs and 32% for the available memory. This is a significant result considering the high number of instantiated neurons.

| HW component     | LUT     | FF      | BRAM |
|------------------|---------|---------|------|
| Single neuron    | 62      | 40      | -    |
| 400 neurons      | 23885   | 15614   | -    |
| Complete layer   | 26038   | 16846   | -    |
| Spikes generator | 6343    | 6311    | -    |
| Weights          | -       | -       | 45   |
| Complete accelerator | 29145 (55%) | 26853 (25%) | 45 (32%) |
| Total FPGA Available | 53200 | 106400 | 140 |

TABLE II
REQUARED AREA

To analyze the throughput for an image classification, one must first compute the average number of active elaboration steps. Figure 2 shows that in our experiments this number is equal to 23 both for the excitatory and inhibitory neurons. With this value and with the structure described in subsection IV-A, the number of clock cycles required to classify an image can be computed as:

\[ N_{cl} = 23 \cdot (784 + 400) + (3500 - 23) \cdot 1 = 30709 \] (5)

In particular, each inactive elaboration step requires a single clock cycle, while each active step needs the elaboration of all spikes (i.e., 784 for the excitatory and 400 for the inhibitory ones).

The target FPGA has a maximum clock frequency of 886 MHz, that leads to an average classification time of:

\[ \Delta t_{\text{classification}} = \frac{30709}{8.86 \cdot 10^6} s \approx 35 \mu s \] (6)

As a reference the classification of a single image using the Brian2 simulation of [20] takes around 0.2 seconds on a 2GHz Intel i5 dual-core processor.

V. CONCLUSIONS

The design process of a very light hardware accelerator for SNNs has been presented, with many techniques used to reduce complexity and improve performance. The design focused on a specific dataset, the MNIST. The future work consists of generalizing the structure to apply it to other datasets. In this sense, different network structures will be analyzed, such as using deeper architectures with more layers to maximize accuracy.

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