L2C2: Last-Level Compressed-Cache NVM and a Procedure to Forecast Performance and Lifetime

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Abstract—Several emerging non-volatile (NV) memory technologies are rising as interesting alternatives to build the Last-Level Cache (LLC). Their advantages, compared to SRAM memory, are higher density and lower static power, but write operations wear out the bitcells to the point of eventually losing their storage capacity. In this context, this paper presents a novel LLC organization designed to extend the lifetime of the NV data array and a procedure to forecast in detail the capacity and performance of such an NV-LLC over its lifetime.

From a methodological point of view, although different approaches are used in the literature to analyze the degradation of an NV-LLC, none of them allows to study in detail its temporal evolution. In this sense, this work proposes a forecast procedure that combines detailed simulation and prediction, allowing an accurate analysis of the impact of different cache control policies and mechanisms (replacement, wear-leveling, compression, etc.) on the temporal evolution of the indices of interest, such as the effective capacity of the NV-LLC or the system IPC.

We also introduce L2C2, a LLC design intended for implementation in NV memory technology that combines fault tolerance, compression, and internal write wear leveling for the first time. Compression is not used to store more blocks and increase the hit rate, but to reduce the write rate and increase the lifetime during which the cache supports near-peak performance. In addition, to support byte loss without performance drop, L2C2 inherently allows N redundant bytes to be added to each cache entry. Thus, L2C2+N, the endurance-scaled version of L2C2, allows balancing the cost of redundant capacity with the benefit of longer lifetime.

For instance, as a use case, we have implemented the L2C2 cache with STT-RAM technology. It has affordable hardware overheads compared to that of a baseline NV-LLC without compression in terms of area, latency and energy consumption, and increases up to 6-37 times the time in which 50% of the effective capacity is degraded, depending on the variability in the manufacturing process. Compared to L2C2, L2C2+6 which adds 6 bytes of redundant capacity per entry, that means 9.1% of storage overhead, can increase up to 1.4-4.3 times the time in which the system gets its initial peak performance degraded.

Index Terms—Non-volatile memories, endurance, reliability, cache memories, memory hierarchy.

I. INTRODUCTION, MOTIVATION AND CONTRIBUTIONS

The goal of the cache subsystem in a shared memory multiprocessor is to reduce the number of main memory accesses. Specifically, the shared last-level cache (LLC) filters requests from the lower-level caches turning slow main memory accesses into fast LLC hits, saving main memory bandwidth, power, and increasing system performance. However, the number of cores/threads integrated on a chip grows faster than the bandwidth with main memory. Therefore, it is necessary to improve the hit ratio of the LLC by increasing not only total size but also size per core/thread. Most LLCs are implemented with 6T-SRAM cells, a technology that does not scale well in terms of density and static power.

In the short to medium term, non-volatile memory (NVM) technologies rise as an alternative to SRAMs due to their higher density and lower static power. Among these technologies we can mention phase change (PCM) 

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most NVMs cause noticeable wear on their bitcells, making their lifetime much shorter than that of SRAMs. The simplest way to deal with an uncorrectable fault in a bitcell is to disable the memory region to which it belongs, with a size that depends on the context: a whole memory page, a cache frame or a byte.

In this paper we present two contributions to the design and evaluation of NV-LLCs made up with memory bitcells that wear out with writes. First, L2C2, a new fault-tolerant last-level cache organization intended for NV technologies that relies on byte disabling and data compression to increase lifetime while keeping performance. The design called L2C2+N is the endurance-scaled version of L2C2 with no more than adding N spare bytes. Second, we introduce a procedure to forecast the time evolution of effective capacity and performance, suitable for modeling either frame disabling or byte disabling with compression.

A. L2C2: Last-Level Compressed-Contents NV cache

Proposals on NV-LLC organizations usually focus on mechanisms to decrease and/or balance the number of writes, seeking to increase the lifetime and at the same time, if possible, counteract the high cost in energy and latency of writes.

To reduce the number of writes, it has been proposed, for example, to reduce the number of inserted cache blocks, using some kind of filtering or collaborating with the private levels. Other techniques to reduce writes are closely tied to particular bitcell designs, supporting e.g., read-before-write or early-write-termination. Finally, it is worth mentioning the proposals for hybrid SRAM/NVM LLCs, which stand out for their great potential to reduce writes, in exchange for a more complex design.
that seeks to send as many write requests as possible to the SRAM part without losing performance or increasing power consumption [7], [40].

Wear-leveling mechanisms focus on evenly distributing write operations throughout all the NV-LLC dimensions: cache sets, ways within sets, and bytes within frames [1], [13], [20], [39]. These works seek to slow down write wear by avoiding the formation of hot spots, but none of them considers how to prolong service in the presence of defective bitcells, possibly allowing for a gradual loss of performance.

The possibility of storing compressed blocks in an NV-LLC has hardly been explored. For example, Choi et al. [9] explores an adaptation of the DCC compression scheme proposed for SRAM caches [35]. Just as in DCC caches their goal is to increase the effective capacity by allowing the total number of compressed blocks stored in a cache set to exceed the nominal associativity. Using a set dueling mechanism they dynamically adjust the activation/deactivation of compression to balance the miss rate vs. write rate tradeoff, concluding that their proposal increases energy efficiency, but decreases lifetime by 8% with respect to a cache without compression.

Thus, in relation to our goal of designing an NVM cache that continues to provide service as bitcells fail, it is appropriate to broaden the scope to look for related solutions that could serve our purpose.

Any memory structure is subject to experience a bitcell fault during its operation, transient or permanent. To avoid a system crash, the memory controller must detect the error and correct it. To do this, fault-tolerant cache memories may protect every cache frame with an error correction code (ECC) mechanism, capable at least detecting up to two errors and correcting one (SECDED). If the error comes from a permanent bitcell fault, the SECDED mechanism no longer ensures correct operation, since a new error in another bitcell of the same frame would be unrecoverable. The simplest solution is frame disabling, already present in commercial processors long time ago [6], [42]. It consists of disabling the entire cache frame when a permanent fault is detected in one of its bitcells. Other approaches propose to add more redundancy, seeking to correct more than one error in each frame. Redundancy can be included in the error correction code itself, allowing to correct N errors instead of just one [21]. However, the overhead required by such ECCs increases rapidly with N, to the point of making it impractical.

Alternatively, redundancy can be added outside the ECC mechanism by noting permanently failed bitcells and correcting their value [35], [37], [45]. For example, Schechter et al., in the context of main memory proposes the Error-Correcting Pointers (ECP) mechanism that stores for each faulty bitcell its frame position and the value it should store, e.g. a 9-bit pointer for a 64-byte memory frame and a one bit data, respectively [36]. The extra storage cost limits this approach to a moderate number of faulty cells. In fact, the authors evaluate the mechanism for up to N=6 defective bitcells (ECP-6).

Other work proposes to take advantage of memory frames with defects without having to disable them entirely. For example, Ipek et al. proposes the Dynamically Replicated Memory (DRM) technique to store a memory page in two partially faulty page frames [18]. Or, with a higher complexity, Jadidi et al. advocate the use of compression to harden main memory [19]. They assume a PCM memory with ECP-6 protection for each 64-byte frame. Their mechanism allows storing a compressed block in a degraded frame, as long as there is a contiguous chunk within the frame, called compression window, of size greater than or equal to the compressed block, and with no more than 6 bitcell faults. This allows a memory frame to be used even if it has more than 6 faults, as long as they are outside the compression window. In summary, this proposal increases memory lifetime by three aggregate effects: it has a repair mechanism, it decreases the write rate by the same amount as the compression rate achieved, and it does not create write hot spots because it has an intra-frame write leveling mechanism. However, although its ideas are inspiring, this proposal has been developed to collaborate with OS paging system and its direct transfer to cache memory hardware is not straightforward at all.

Data compression has also been proposed in the context of caches operating at near-threshold voltage. Ferrerón et al. propose the Concertina cache, which provides each frame with a bit vector or a few pointers identifying the bytes that fault when the supply voltage drops [14]. These metadata are calculated once, by scanning the cache when entering in low-voltage mode, and do not change as long as the supply voltage remains constant. Before inserting a new block, a simple null subblock compression mechanism searches in LRU order for the existence of a frame with enough live bytes. Concertina does not need or seek to level write wear, nor requires a high-coverage compression mechanism, but part of its design will be useful for our proposal.

Contributions. L2C2 is the first NV-LLC capable of tolerating byte faults in NVM bitcells. It uses data block compression and intra-frame write leveling to extend the lifetime of degraded frames. In contrast to current alternatives, it is able to maintain high performance for a longer time, or in other words, for a given time of use it achieves higher performance, and it does so at a reasonable hardware cost. Moreover, its design is inherently scalable in terms of lifetime: simply adding N additional spare bytes to each frame, without modifying the design ideas, results in L2C2+N, the endurance-scaled version of L2C2, which is able to support the nominal capacity for longer.

On the one hand, the design of L2C2 carefully considers previous concepts of non-volatile main memory management and SRAM caches, namely:

- Support for byte disabling [14], by incorporating the necessary metadata to identify non-operational bytes. Besides, a SECDED mechanism is incorporated with the ability to trigger an Operating System routine that disables a byte by modifying such metadata.
- BDI compression [30]. This data compression mechanism is selected because it provides high coverage and a good compression ratio. These two characteristics allow,
simultaneously, to reduce the number of bitcells written (more duration) and to increase the possibilities of saving the block in frames of reduced size (more performance). In addition, its hardware implementation has low decompression latency.

- LRU-Fit replacement algorithm [14]. After appropriate experimentation, this option is selected. LRU-Fit is a locality-aware replacement algorithm, which selects the LRU victim cache frame among all those that are large enough to allocate the incoming compressed block (Fit).

On the other hand, L2C2 incorporates two original enhancements, which are crucial to maintain high performance for a longer time, namely:

- Intra-frame wear-leveling and compressed block rearrangement within the frame. We propose a new mechanism that achieves three key objectives: (a) wear out the live bytes of each frame evenly as the rest is failing, (b) upon inserting a compressed block into L2C2, rearrange the byte layout of the compressed block to write the appropriate subset of live bytes of the frame, and (c) the same but in the reverse direction, i.e., in case of a L2C2 hit, reconstruct the original layout of a compressed block, which is scattered in a partially broken frame, to supply it to the decompressor. Using VLSI synthesis, that circuitry has been shown to be feasible in terms of area, latency and power consumption.

- Because the above mechanism is scalable, it is possible to add an arbitrary number of N redundant bytes to each frame, privately and without any change in the design. L2C2+N, the version of L2C2 with redundancy, thus has frames with 64+N data bytes that cooperate in storing compressed blocks from the beginning, extending the cache lifetime in proportion to the built-in N degree of redundancy.

B. Forecasting capacity and performance evolution of NV-LLCs

Previous work often highlights the difficulty of accurately modeling aging in NV memory and its effects on performance. In the absence of a standard procedure, practical solutions have been proposed, designed to assess specific aspects of one or another mechanism.

A first group of papers related to the evaluation of reliability improvement in NV main memory or cache, focuses exclusively on measuring either the reduction in the number of writes or their variability [11], [29], [39]. For instance, Wang et al. compare wear-leveling mechanisms in NV-LLCs by calculating the elapsed time from startup to the first bitcell fault [39]. Such cache lifetime is computed by dividing the maximum number of writes supported by a bitcell by the number of writes per unit time (write rate) in the cache line that accumulates the most writes. The procedure consists of a single cycle-accurate simulation to record write variability, followed by an aging prediction that assumes such variability to be constant throughout the life of the cache. This procedure is simple, fast and allows the production of performance metrics such as the number of instructions per cycle (IPC), but does not take into account the manufacturing variability in bitcell endurance. More importantly, it also does not allow to calculate the time evolution of the capacity or performance in degraded mode of operation, in which cache frames are progressively lost.

A second group of works, focused on extending the main memory lifetime, already incorporate process variability, modeling bitcell endurance by means of a normal probability distribution [18], [19], [36], [37], [45].

Ipek et al. [18] and Seong et al. [37] assume that writes are spread evenly across the main memory. Their quality metric is the number of writes the memory can receive until the first unrecoverable fault occurs on any of its pages [37] or until the memory loses all its capacity (each page is deactivated when it reaches its write limit) [18]. They do not relate the number of writes to the time elapsed, and therefore do not need to simulate any application. Yoon et al. propose the same quality metric [45], but assume that the page write rate is constant, thus expressing memory lifetime in elapsed time, rather than number of writes.

Schechter et al. [36] and Jadidi et al. [19] simulate a workload on a system whose main memory has no faulty cells. The former to obtain frequency of writes and the latter to obtain traces of memory accesses. Schechter et al. evenly distribute the number of writes among all live pages and calculate the bitcell that will fail first [36]. When the number of faulty cells in a page reaches a threshold, the page is deactivated and its writes are distributed evenly among the remaining live pages. Jadidi et al. use the trace of writes to main memory to accumulate the number of writes to each bitcell, deactivating them when they reach their maximum number [19]. The simulation is repeated several times, until the memory loses half of its capacity. They measure the lifetime by counting the number of times the trace is reinjected. Now, from the execution time of the detailed simulation that produced the trace they can calculate a lifespan in terms of elapsed time, but always assuming that performance does not vary with memory degradation.

In summary, to date no procedure capable of accurately estimating the simultaneous degradation of capacity and performance over time has been proposed.

The essence of the problem is as follows. Memory cells age with writes. And as memory degrades performance and write rates also change. But its detailed simulation, cycle by cycle, requires a time that would far exceed the lifetime of the system under study.

Focusing on the cache, on the one hand its degradation leads to an increase in the miss rate, which results in a loss of performance which in turn results in a decrease of the cache write rate. On the other hand, if a certain cache set degrades more than others, it is not correct to equally distribute the write rate of the whole cache in the new associativity configuration. Let’s quantify how the write rate per frame may change as the NV-LLC degrades. Figure 1 shows the average write rate per frame in a 16MB, 16-way frame-disabling NV-LLC at various
aging stages (see Section [V] for the simulated system details). Each bar depicts the average write rate of all frames belonging to a given group of sets, namely the sets with \( A \) live frames in a degraded NV-LLC with 90%, 75% and 50% effective capacity, respectively.

![Graph showing average write rate per frame in sets with \( A \) live frames as a function of capacity (90%, 75%, and 50%).](image)

At 90% capacity, all sets have between 16 and 7 live frames, but as the effective capacity reduces to 75%, more degraded sets, which have only 6 to 1 live frames, also appear. Regardless of the effective capacity, as \( A \) decreases, the write rate per frame increases noticeably. This increase in write rate has two causes: i) the miss rate increases in the sets with fewer live frames and therefore those sets experience a higher write rate, and ii) the write rate per set will be spread over fewer live frames. On the other hand, when considering the reduction in effective capacity from 75% to 50%, a decrease in the write rate per frame is observed for any value of \( A \), which is due to a noticeable decrease in system performance.

Furthermore, this non-uniform degradation may affect differently the threads sharing the NV-LLC, selectively reducing the IPC of some of them and changing the pattern of writes in the entire cache. The existence of compression further complicates the modeling, as the data set referenced by each thread may have different compression capabilities that will wear cache bytes unevenly. In short, a single simulation cannot capture the complexity of all these interactions.

**Contributions.** Accurately addressing this feedback between degradation and performance loss over the lifetime of the NV-LLC is the second problem we tackle in this work. We provide a forecast procedure to estimate the evolution over time of any metric of interest linked to the LLC (effective capacity, miss rate, IPC, etc.), from the time it starts operating until its storage capacity is exhausted.

The forecast relies on a sequence of epochs that sample the lifetime of the cache. Each epoch starts with a performance simulation and ends with an aging prediction. The *performance simulation* is carried out with cycle detail on a snapshot of the cache at a particular aging stage and obtains performance metrics (miss rate, IPC, etc.) and in particular, all the write rate statistics needed to feed the aging prediction. The *aging prediction* removes from operation the bytes or frames that die, according to the bitcell endurance model, the cache organization and the write rate statistics received. At the end of each aging prediction phase, a new cache snapshot is generated, with lower capacity than the previous one.

Thus, the performance and capacity forecasts take into account the interaction between the workload and the non-uniform degradation of the NV-LLC in its multiple dimensions (bank, set, way, byte). It can be applied to a wide range of NV main memory or cache designs, although in this paper we have focused on L2C2 and related alternatives, taking into account replacement and operation with compressed blocks and degraded frames under different redundancy schemes. Of course performance or capacity forecasts are useful for research purposes, but also can be an industry tool to estimate the life cycle of a NV memory and provide customers with a clear commitment to lifespan and performance.

The rest of the paper is organised as follows. Section [II] lays the groundwork for NV-LLCs. Section [III] describes L2C2, a byte-level fault-tolerant cache capable of handling compressed blocks, showing the storage overhead, the detailed design of the block read and write hardware, and the latency penalty incurred in the block read service. In Section [IV], our forecast procedure is conducted on systems with frame disabling and byte disabling with compression. In Section [V] we demonstrate the validity of the forecast procedure. Section [VI] evaluates the degradation of L2C2 over time and compares it to various NV-LLC configurations. Finally, Section [VII] concludes this study.

**II. BACKGROUND**

This section briefly reviews the background regarding the bitcell resilience model, data compression in the context of NV technologies, with emphasis on BDI compression, and finally, the addition of redundant capacity. The reader familiar with these concepts can skip this section without loss of continuity.

**A. Bitcell endurance model**

Writing 0 or 1 to an NVM bitcell requires to invest some energy for a time period to alter the value of a physical property in one of the bitcell circuit materials, whose structure, components, dimensions and interface are critical to the proper functionality of the memory [26], [31], [34]. Write operations, besides being more costly in time and energy than read operations, eventually degrade bitcells, which render to lose its storage capacity. In this context, the bitcell endurance is defined as the number of writes the bitcell will withstand before it breaks down and loses its storage capability. Bitcell endurance can be approximated by a normal probability distribution of mean \( \mu = 10^k \) writes and coefficient of variation \( \text{cv} = \frac{\sigma}{\mu} \), usually between 0.2 and 0.3 [10], [13], [18], [36], [37], [45]. The coefficient of variation reflects the variability in the manufacturing process. The endurance figures are different for each technology and depend on the manufacturer and the target market. For instance, STT-RAM endurance is subject to some
design parameters tradeoffs such as retention time, area, power efficiency and read/write latency [13], [27]. It is therefore not surprising to find in the literature STT-RAM endurance values from $10^6$ for embedded systems or IoT applications [8], [15], [24], [41] up to $10^{12}$ for general purpose microprocessors [13], [17], [39].

B. Data compression

Data compression reduces the block size. This is beneficial in the NVM context because it allows fewer bits to be written and consequently extends the lifetime of the main memory or cache [9], [11], [19], [29]. Yet, compression has another benefit in the context of a byte-level fault tolerant NV cache such as L2C2: it allows cache frames with dead bytes to hold blocks if compression is high enough [14], [19]. Any compression mechanism that achieves wide coverage even at the cost of a moderate compression ratio can be useful, so that a large percentage of blocks, once compressed, can be stored in degraded cache frames. On the other hand, the decompression latency must be very low in terms of processor cycles, since decompression is on the critical path of the block service and latency must be very low in terms of processor cycles, since the cost of a moderate compression ratio can be useful, so that any compression mechanism that achieves wide coverage even at the cost of a moderate compression ratio can be useful, so that a large percentage of blocks, once compressed, can be stored in degraded cache frames. On the other hand, the decompression latency must be very low in terms of processor cycles, since decompression is on the critical path of the block service and may affect system performance.

The chosen mechanism is Base-Delta Immediate (BDI), as it achieves high coverage, fast decompression (1 cycle) and a substantial compression ratio [30]. BDI is based on value locality, i.e. on the similarity between the values stored within a block. It assumes that a 64-byte block is a set of fixed-size values, either 8 8-byte values, 16 4-byte values, or 32 2-byte values. It determines whether the values can be represented more compactly as a Base value and a series of arithmetic differences (Deltas) with respect to that base.

A block can be compressed with several Base + Delta combinations which are computed in parallel. An example with 14 BDI Compression Encodings (CE) is shown in Table I along with the size values for the Base, Delta and the total compressed size. Thus, the compression mechanism chooses for each block the compression encoding (Base + Delta combination) that achieves the highest compression ratio.

TABLE I: BDI compression encodings and their sizes, in Bytes.

| Name          | Base | Delta | Size  | Name          | Base | Delta | Size  |
|---------------|------|-------|-------|---------------|------|-------|-------|
| All Zeros     | 0    | 0     | 0     | Base          | 2    | 1     | 3    |
| Rep. V(8)     | 8    | 0     | 8     | Base + Delta  | 8    | 4     | 12   |
| BS(8)A1       | 8    | 1     | 16    | BS(8)A5      | 8    | 5     | 21   |
| BS(8)A1       | 4    | 1     | 21    | BS(8)A3      | 4    | 3     | 30   |
| BS(8)A2       | 8    | 2     | 23    | BS(8)A6      | 8    | 6     | 38   |
| BS(8)A3       | 8    | 3     | 30    | BS(8)A7      | 8    | 7     | 38   |
| BS(8)A4       | 2    | 4     | 36    | Uncomp.       | -    | -     | 64   |

C. Addition of redundant capacity

The reliability of the NV-LLC can be improved by adding redundant capacity. This can be done by using classical error detection and correction (ECC) codes or more sophisticated techniques [18], [36], [37], [45]. The maximum number of bit errors that can be detected and corrected is limited by the available area and energy budget. For instance, Schechter et al. propose ECP [36], an ECC mechanism that encodes the location of defective bitcells and assigns healthy ones to replace them.

However, in order to further increase reliability, a substantial portion of the redundant capacity could be dedicated to the replacement or expansion of the rated cache capacity stated in the commercial specification. Both alternatives will be evaluated later in this paper.

III. LAST-LEVEL COMPRESSED-CONTENTS NV CACHE

This section describes the basic organization of L2C2, also showing the adaptation of BDI compression, metadata layout, the details of block rearrangement and replacement, and how to add redundant capacity.

A. Basic organization

1) Content management between the private L1/L2 levels and the shared L2C2: Non-inclusive hierarchies have shown to be specially useful to avoid superfluous block insertions in the LLC [7]. Therefore, a non-inclusive organization is used to minimize writes in L2C2, see Figure 2. A block enters L2C2 by effect of a replacement in L2, provided that the block was not already in L2C2. In case of a write miss in L1 and L2, and a hit in L2C2, the corresponding block is brought to L1/L2 and invalidated in L2C2. Note that in this case, leaving the block in L2C2 does not make sense, because it will eventually have to be written back to L2C2 when it is evicted from L2.

![Fig. 2: Block flow diagram of non-inclusive model.](image)

To select the victim block, L2C2 takes into account the recency order according to the following rules: 1) inserted blocks are placed in an LRU list at the MRU position (lowest replacement priority), 2) a read hit in L2C2 places the block to the MRU position, and 3) replacement of a clean block in the private caches is communicated to L2C2; in case such a block is present, it is also placed at the MRU position.

However, if the LRU cache frame does not have sufficient capacity for the incoming compressed block, it cannot be used as a victim. Then there are two possibilities, either to search in order from least to most recent for the first frame with sufficient capacity (LRU-Fit policy) or to choose the frame with the smallest possible capacity, and if there are several with the same capacity, the LRU one (LRU-Best-Fit policy). Ferrerón et al. test both alternatives and choose LRU-Fit for its better performance [14], but since in their context writes do not produce degradation, the LRU-Best-Fit policy could be advantageous for the L2C2 design. LRU-Best-Fit avoids...
writes on the highest capacity frames, and therefore poorly compressible blocks would see their residency opportunities increase. Therefore, in Section VII-D the two policies will be confronted.

2) Bitcell fault detection: Memory cells lose their retention capacity after a certain number of writes. It is therefore essential to handle these permanent faults without losing information. We assume a SECDED mechanism, able to correct a single-bit error and detect up to two. We assume that this ECC mechanism, upon detecting and correcting a single bit fault, triggers an Operating System exception, notifying the identity of the faulty byte [45]. Then, in order to prevent a second (uncorrectable) error from arising within the same region, the exception routine will disable the appropriate region, a whole frame using frame disabling, or a byte in L2C2. Note that ECC support is already present in many current cache designs; AMD Zen SRAM LLCs, for instance, provide DECTED [38].

3) Wear-leveling mechanism: Writing compressed blocks in a frame is a new source of imbalance in the wear of the cells acting within the frame itself. As we will quantify, if, for example, compressed blocks are always stored from the beginning of the frame, the first bytes of the frame will receive more writes than the last ones.

Therefore, an intra-frame wear-leveling mechanism is needed to evenly distribute the writes within the frame. We assume a global counter modulo the cache frame size [19]. Blocks are stored in the frames starting from the byte indicated by this global counter and using the frame as a circular buffer. Each time the value of the counter is changed, the entire cache must be flushed, but since this must be done every few days or weeks, the impact on performance is negligible. The details and the extension of the mechanism to degraded frames can be found in Section III-D3.

B. BDI adaptation

Pekhimenko et al. focus their application on achieving a large average compression ratio and therefore dispense with compression encodings with small compression ratios [30], those marked with an * in Table I. However, L2C2 incorporates them, because in this way frames with few defective bytes will be able to store low compression blocks and thus performance increases noticeably [14].

To quantify the importance of such low compression blocks, Figure 3 shows a classification of all blocks written in L2C2 according to the achieved BDI compression ratio for the SPEC CPU 2006 and 2017 applications used in this work. On average, 22% of the blocks written are uncompressible (Unc), 29% have low compression ratio (LCR) (compressed block size > 37) and 49% have high compression ratio (HCR) (compressed block size ≤ 37). For instance, if all frames in an L2C2 cache have a faulty byte, and the compression mechanism does not use the low-compression ratio encodings, the chance to store 29% of the blocks would be lost.

C. L2C2 metadata

The tag array undergoes the most write requests as it must keep the coherence and replacement states up to date. Should these bit cells fail, the entire data frame should be deactivated. Therefore, we assume the tag array is built with SRAM technology, free of wear by writing. Our proposal only adds a 4-bit field to store the frame capacity to each tag array entry. This frame capacity is represented in terms of the largest compression encoding the frame can allocate (see Figure 4).

Fig. 3: Block classification regarding its compression ratio for the selected SPEC CPU 2006 and 2017 applications.

The data array is built using NVM technology. Each frame must have a capacity of 66 bytes: 64 data bytes plus one or two metadata bytes: up to 11 ECC bits and 4 bits representing the compression encoding (CE) of the data block. In addition, a fault bitmap is needed next to the data array to identify faulty bytes. This fault bitmap requires 66 bits for each frame. During the life of the frame this bitmap will experience at most 66 write requests, so it can also be implemented with NVM technology.

D. Block processing: compression, ECC, replacement and rearrangement

1) L2C2 miss, block writing: Figure 5 shows the components involved in the processing of a block B to be written in L2C2, from compression to rearrangement. In Figures 5 and 6 the shaded boxes represent what is new and/or has been modified to the Concertina proposal [14].

First, the BDI compression units receive the block B (64 B) [1] Compression. The result of each compression unit is a) whether the block is compressible or not and, if so, b) the compressed block. As a result, the compressed block with the highest compression ratio (CB, 0-64 B) is selected and the corresponding compression encoding (CE, 4 b) is reported.

Next, the ECC bits corresponding to CB are calculated [2] ECC. The ECC mechanism selected in particular is
orthogonal to our proposal. As mentioned above, we assume SECDED protection, which means an overhead between 2 and 11 bits encoded in a field of one to two bytes. We call ECB the concatenation of CB and SECDED bits, whose length ranges from 1 to 66 bytes. The length of this ECB determines the minimum capacity a cache frame must have to accommodate the block.

The replacement logic selects the victim block among the frames with the required minimum capacity \([3)\ Replacement\]. For this, the replacement logic considers the CE of the incoming block B along with the capacities and LRU order of the frames still alive in the involved cache set.

Every frame has an associated fault bitmap that points out the faulty bytes (66 b). This fault bitmap information is initialized to \(1\)'s indicating that all bytes in a frame are non-defective. In addition, the byte number from which to start writing the frame is reported by the Global Counter (GC, values 0-65). According to the GC and CE values and the fault bitmap, the block is rearranged for selective writing (RECB, 1-66 bytes) under a write mask (66 b) \([4) Block rearrangement\]. The next subsection 3) details the rearrangement logic (ECB or RECB Block rearrangement for L2C2 write or read, respectively).

2) L2C2 hit, block reading: Similarly but in the opposite order, Figure 5 summarises the read flow of an L2C2 block. First, the block is rearranged using as input RECB, the fault bitmap and the GC value. Then, the ECC of ECB is checked, and from CB and CE the uncompressed B block is obtained and forwarded to L2/L1 \([3)\ Decompression\].

3) Rearrangement logic: The rearrangement logic is composed of two elements: Index Calculation and Crossbar. The index calculation determines the mapping from ECB bytes to RECB bytes (L2C2 write) or conversely, from RECB bytes to ECB bytes (L2C2 read). The crossbar moves bytes from the input ports to the output ports.

Figure 6 shows an example of rearranging an ECB from the fault bitmap (FM) and the GC and CE values. When writing a frame into L2C2, RECB is an ECB rearrangement consisting of a right rotation starting from the GC value and skipping the faulty bytes. Afterwards, the write is selectively performed on the bytes indicated by the computed write mask.

Algorithm 1 describes the index calculation for writing N-byte frames. It takes as inputs the fault bitmap (FM) corresponding to the destination frame and the values of the global counter (GC) and compression encoding (CE). The outputs are the write mask and the index vector \(I[N = frame \ size]\) that controls the output ports of the crossbar. For example, \(I[7] = 1\) means that byte 1 of ECB will appear in the output port 7 of the crossbar, see Figure 7.

The first for loop (line 2) calculates indexes without considering the global counter value. That is, assuming that ECB is to be rearranged starting with the byte zero of the destination frame. Note that the calculation of each iteration uses the result of the previous one. This implies using N adders in series. Alternatively, our implementation uses a tree of adders, which reduces the computation time to that of \(log_2 (N)\) adders in series. Each adder uses \(log_2 (N)\) bits at most.

The two next loops (lines 5 and 6) adjust indexes considering the global counter value. Now, the iterations within each loop are independent and can be calculated in parallel, so the calculation time of the two iterations is that corresponding to
Finally, the last loop (line 7) calculates the write mask. This loop can be synthesized with an array of 64 7-bit comparators. These comparators act on the calculated indexes and their operation can overlap with the crossbar traversal.

Algorithm 1: ECB → RECB Index Calculation

| Input: |
|--------|
| FM: N-bit vector fault bitmap |
| GC: global counter |
| size: ECB size, computed from CE |
| \( 0 \leq GC, size \leq N - 1 \) |

| Output: |
|--------|
| I[N]: N crossbar output port indexes |
| WM[N]: write mask N-bit vector |

1. I[0] = 0
2. for \( i=1; i<N; i++ \) do I[i] = I[i-1] + FM[i-1];
3. T = I[N-1] + FM[N-1];
4. GCI = I[GC];
5. for \( i=0; i<N; i++ \) do I[i] = I[i] - GCI;
6. for \( i=0; i<GC; i++ \) do I[i] = I[i] + T;
7. for \( i=0; i<N; i++ \) do if I[i] < size && FM[I] == 1 then WM[I] = 1 else WM[I] = 0;

The index vector is calculated when writing and reading in the same way. In the write circuit, the crossbar is an array of multiplexers governed directly by the index vector. In the read circuit, the crossbar acts as right-aligner and is more complex. Our implementation assumes NxN comparators of \( \log_2 (N) \) bits and N output multiplexers of N bytes to 1 byte with decoded control. The decoded control of the multiplexer that produces the byte \( i \) is generated by N comparators between the value \( i \) and the N elements of the index vector.

**VLSI implementation.** To put into context costs and delays of the rearrangement logic we assume an L2C2 built with 22nm STT-RAM technology, the largest scale of integration available in the NVSim tool [12]. Table II shows area, latency and power of the tag SRAM array and the data STT-RAM array that support the 4MB cache banks we are going to use in the experimental section.

| Table II: Hardware cost comparison. |
|-----------------------------------|
| | SRAM Tag Array | STT-RAM Data Array | ECB →RECB 16 nm | RECB →ECB 16 nm |
| Area (mm\(^2\)) | 0.116 | 0.74 | 0.021 | 0.025 |
| Latency (ns) | 0.28 | 2.41 | 0.33 | 0.38 |
| Dynamic read power (mW) | 0.17 | 6.87 | - | 0.49 |
| Dynamic write power (mW) | 0.16 | 18.64 | 0.61 | - |
| Static P (mW) | 109 | 338 | 0.53 | 0.7 |

Both ECB and RECB rearrangement logic are outside the L2C2 core, but the latter is located in the critical path of block delivery to L1/L2. In order to quantify their physical features both have been specified, simulated and laid out with the Synopsys Design Compiler R-2020.09-SP2 and Synopsys IC Compiler R-2020.09-SP2. Due to the lack of a 22nm library, we used the SAED16nm FinFET Low-Vt technology in worst case condition (typical-typical, 125 °C and 0.8 volts). These tools allowed us to estimate post-layout costs in terms of area, latency and power consumption. Dynamic power values were calculated from activity data obtained from our workload simulations. The latency of the RECB → ECB logic (0.38 ns) plus the delay and setup times of the input and output registers, respectively, can be estimated at about two cycles at 3.5 GHz. That is, rearranging and decompression increases the L2C2 load-use latency, with respect to a frame-disabling cache, from 30 to 32 cycles, a 6.7%.

In summary, looking at the figures as a whole, the overhead seems to be affordable on all metrics. Regarding storage costs, Table [V] also provides a comparison between all the evaluated cache candidates.

**E. L2C2+N: adding redundant capacity to L2C2**

Providing L2C2 with a few spare bytes in each frame could be very convenient since it would allow to continue working without loss of performance after the failure of several bytes of each cache frame.

The design presented so far allows to add N spare bytes in a very straightforward way: just increase each frame from 66 to 66+N bytes in the data array, and also increase the bitmaps from 66 to 66+N bits. In addition, the rearrangement logic has to be extended to handle 66+N byte blocks, and the Global Counter has to count modulo 66+N. Without further changes, the wear-leveling logic will take care of distributing the writes among the 66+N bytes available. A frame will only start to impose performance constraints when its effective capacity falls below 66 bytes.

**IV. Forecast procedure**

This section describes a procedure to forecast the capacity and performance evolution of an NV-LLC through time, from its initial, fully operational condition, until its complete exhaustion. Without loss of generality the procedure assumes byte granularity, but extending it to other sizes is straightforward. The maximum number of writes supported by bitcells is modelled by a normal distribution.

The forecast is driven by a detailed, cycle-by-cycle simulation of a workload that can be multiprogrammed, parallel, or a mix of both execution modes. In this paper we opted for a multiprogrammed workload, but the other alternatives can be simulated in exactly the same way.

The forecast procedure determines the live byte configuration in discrete steps of capacity loss, which we call epochs. An epoch starts with a detailed Simulation phase, where performance and write rate measurements are extracted, and continues with a Prediction phase where each byte that fails is disabled and the remaining number of writes of those that are still live is updated.
To the best of our knowledge, this is the first NV-LLC capacity and performance forecast procedure proposed so far.

A. Data structures supporting the forecast procedure

For each byte of the data array it is necessary to keep track of two key attributes, namely the number of per-byte Remaining Writes and the experienced per-byte Write Rate. These attributes are represented in two data structures, called maps and abbreviated as RW map and WR map, respectively.

**RW map.** Each entry of RW map holds the number of remaining writes \( rw_{ijk} \) of byte \( B_{ijk} \) (set \( i \), way \( j \), byte \( k \)), see Figure 8. RW map is initialized according to the statistical endurance model of the memory technology used, as in [10], [13], [18], [36], [37], [45].

**WR map.** An alternative approach, which is nearly as accurate, but with lower simulation cost is the following. After a suitable simulation time we write down in a WR map, the write rate per byte \( wr_{ijk} \), see Figure 8. On the assumption that these per-byte write rates remain constant as long as no further byte is disabled, we can compute the predicted lifetime (PLT) of each byte \( B_{ijk} \) as:

\[
PLT(B_{ijk}) = \frac{rw_{ijk}}{wr_{ijk}}
\]

We can use PLT to predict the next byte that becomes faulty.

B. Basis of the forecast Procedure

The lifetime of an NV-LLC can be forecast using the procedure outlined with black lines in Figure 9. The RW map is first initialized taking samples from a normal statistical distribution of the maximum number of writes a bitcell can endure. Forecast then proceeds through successive epochs which consist of a Simulation phase followed by a Prediction phase.

The Simulation phase requires the development of a microarchitectural LLC model that allows to dynamically configure in each set a variable associativity and, if applicable, a variable number of bytes per frame. So, the simulation will take into account the regions that are still alive, according to the RW map, run the workload for a suitable number of cycles, compute the write rates in each byte, and finally update the WR map.

The Prediction phase combines the values of both maps to calculate \( PLT(B_{ijk}) \), selecting the byte with the lowest remaining lifetime, \( T = \min(PLT(B_{ijk})) \). The prediction consists of advancing the forecasted lifetime by exactly that value \( T \). To do so, it is sufficient to subtract from the number of remaining writes in each byte of the cache, the number of writes that would have occurred in that byte in a time \( T \) (\( \forall \; ijk : rw_{ijk} = rw_{ijk} - T * wr_{ijk} \)). In this way the next simulation will be performed with the corresponding region disabled, cache frame or byte, so that the behavior of the LLC will take into account the degradation experienced in the data array.

Forecast advances through single-prediction epochs until all bytes in the cache are disabled. Each epoch adds the variable time \( T \) to the NV-LLC lifetime, which depends on the initial RW map and the write rate variation. Although the Prediction phase is computationally very light, this alternative approach still requires as many simulations as there are bytes in the cache, and it is also not affordable considering the runtime required for a detailed simulation.

To decrease the number of simulations we propose an approximate procedure that extends the forecast duration within each epoch. This approximate forecast procedure acts as follows. In each epoch, the simulation phase does not change: it receives an RW map and obtains the corresponding WR map. However, the prediction phase has an extension of \( K \) consecutive predictions, corresponding to the failure of \( K \) bytes. After every prediction step the RW map is updated; see \( \Box \) in Figure 9.

The challenge now is that, as bytes die during the multiprediction epoch, the values of the WR map may not reflect the effect of the progressive degradation of the NV-LLC during the epoch.

When a cache byte dies there may be a tiny decrease in hit rate and system performance, which may result in tiny changes of the byte write rate across all cache frames. Our model does not take this reduction into account during the Prediction phase within each epoch. However, if we focus on a shrinking cache set, i.e. one in which a byte has just been disabled, the new write rate in the frames of that set can increase significantly. This effect is evident with frame disabling, see Figure [1] but occurs equally with byte disabling. Consequently, to increase the epoch extension without introducing significant error, a
Thus, during prediction, the aging write rate to consider for
write rates per frame we showed in Figure 1. It corresponds to
the Simulation phase of an epoch that starts with 90% effective
capacity. In that epoch, the Predictions phase handles sets with
7 or more live frames. But before reaching K predictions a
byte belonging to a set with A = 7 may die, appearing a new
health state, that of the sets with A = 6 for which there are
no available write rate data yet. To cope with these cases, we
can stop the prediction, thus ending the epoch prematurely
and starting a new simulation. Alternatively, to keep low
the number of simulations, we can continue the prediction,
also allowing some more error and apply the previous value
wr_avg(7). In this work, we will adopt this second approach.

D. Approximate forecast procedure
for byte disabling plus Compression

Unlike frame disabling, in a cache with byte disabling and
compression, such as L2C2, a write to a frame does not always
imply a write to all the bytes of the frame and therefore the
write rate to the bytes of a frame is lower than the write
rate to the frame. The wear-leveling mechanism ensures an
even distribution of writes among the live bytes of a frame.
Consequently, during prediction, we can assume that the write
rate on all live bytes of a frame is equal, and is calculated as
the average of the write rates on all of them.

Moreover, a fault in one or more bytes of a L2C2 frame
does not preclude storing blocks, as long as their compressed
size is appropriate. Now the health state of its sets is more
diverse than in frame disabling: at any given time there are
not only alive and dead frames, but frames with a very diverse
range of effective capacities.

The number of faulty bytes in a frame limits the compres-
sion encodings it can accommodate. A frame with a certain
effective capacity is associated with a compression class (CC)
if it can accommodate compressed blocks of size CC or
smaller. For example, a frame with 3 defective bytes has an
effective capacity of 61 bytes, which accommodates blocks of
any compression encoding except those of size 64 bytes (see
Table I in page 4) and thus it is associated with CC = 58.

In this context, the prediction of write rate per byte is more
complex. For example, think of a set that has only one frame
of CC = 64. All non-compressible blocks will end up in that
single frame, which can become a hot spot for writes within
the set. But, in another cache set with a majority of frames
with CC = 64, the write rate of the set will be distributed in
a substantially equal way among frames.

With this, our Prediction phase will assume that the write
rate a byte receives depends on the CC of its frame as well
as on the CCs of the rest of the frames in the same cache
set. Therefore, now the health state of a set is abstracted as
a 12-tuple A. It aggregates the compression classes to which
each frame belongs to. For instance, a set with tuple A = (0,
0, 0, 0, 0, 0, 0, 0, 0, 1, 15) has one frame with CC = 58
and 15 frames with CC = 64.

Thus, during prediction, the aging write rate to consider for
the bytes of a given frame \(F_{ij}\) will depend on its compression
class $CC$ and the health state (tuple $\bar{A}$) of the set that contains $F_{ij}$: $\text{wr\_avg}(\bar{A}, CC)$.

More specifically,

$$\text{wr\_avg}(\bar{A}, CC) = \text{average}(\text{wr}_{ijk})$$

$\forall\ ij\ |\ i\ F_{ij} \in \text{set with tuple } \bar{A}$

ii) $F_{ij} \in \text{compression class } CC$

Each time a byte is disabled in a frame $F_{ij}$, CC of the frame and $\bar{A}$ of the set are recomputed. Thereafter, $\bar{A}$, the aging write rate of $F_{ij}$ with compression class $CC$, is approximated by $\text{wr\_avg}(\bar{A}, CC)$; see 3 in Figure 9.

As in frame disabling, as faults are predicted in succession, sets with a tuple value $\bar{A}$ not yet simulated may appear. For instance, suppose a set with the same 12-tuple as before: one frame associated with $CC = 58$, and 15 frames associated with $CC = 64$:

$$\bar{A}_1 = (0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 15).$$

Suppose a byte of one of the fifteen frames with $CC = 64$ fails during the Prediction phase. Now the tuple modeling the set becomes:

$$\bar{A}_2 = (0, 0, 0, 0, 0, 0, 0, 0, 0, 2, 14).$$

But if in the epoch Simulation no $\bar{A}_2$ tuple was tracked, the values of $\text{wr\_avg}(\bar{A}_2, \bar{A})$ are unknown. As in frame disabling, in this work we chose to continue the prediction, tolerating some more error and using for that set the previous values of $\text{wr\_avg}(\bar{A}_1, \bar{A})$ as an approximation of $\text{wr\_avg}(\bar{A}_2, \bar{A})$.

V. METHODOLOGY

Details of the multicore system modeled for the cycle-by-cycle simulation phase of each epoch are shown in Table III. It consists of 4 cores, each with two private cache levels L1 and L2, split into instructions and data. In addition, there is a third cache level (L2C2) which is shared, non-inclusive and distributed in four banks among the cores. The coherence protocol is directory-based MOESI, and the interconnection network is a crossbar connecting the L2 private levels, the banks of the LLC and the directory. The main memory controller is located next to the directory.

**TABLE III: System specification.**

| Cores | 4, ARMv8, out-of-order (up to 8 inst/cycle), 3.5 GHz. |
|-------|--------------------------------------------------|
| Coherence Protocol | MOESI, directory distributed among LLC banks. 64 B data blocks in all levels. |
| L1 | Private, 32 KB D, 32 KB I, 4 ways, LRU. 3-cycles load-use delay, Fetch on write miss. |
| L2 | Private, L1-inclusive, 128 KB D, 128 KB I, 16 ways, LRU. 11-cycles load-use delay, Fetch on write miss. |
| STT-RAM NV-LCC | Shared, non-inclusive, 4 banks, 4MB/bank, 16 ways, LRU. Load-use delay: 30-cycles frame disabling; 32-cycles L2C2. Frames protected by SECDED. Baseline endurance: mean $10^{11}$ wr, $cu = 0.2, 0.25$, and 0.3. |
| Main Memory | 1 memory controller, DDR4. 1 channel, 8GB/channel (1200 MHz). |
| NoC | Crossbar between L2C2 banks and L2s. 32 B flits. |

We use Gem5 along with the Ruby memory subsystem and Garnet interconnection network. In addition, we use NVSim for the L2C2 latency estimations. The workload consists of 10 mixes randomly built by SPEC CPU 2006 and 2017 benchmarks, leaving aside applications with very little activity on the LLC. Fast-forwarding is performed for the first two billion instructions and then 200M cycles are simulated in detail. Table IV shows the applications that make up each mix along with the LLC MPKI of the mix, computed by dividing total cache misses by total number of instructions executed by all applications in the mix. Besides, the top ten memory intensive applications, in terms of accesses per kilo instruction, APKI, are superscripted.

The 10 mixes are run in the simulation phase of each epoch to obtain the WR map for that epoch. The write rate in each byte of the cache is calculated as the average obtained for the 10 mixes.

**TABLE IV: Selected SPEC 2006 and SPEC 2017 applications, with suffixes 06 and 17, respectively and their MPKI. Superscript indicating top-10 memory intensive applications.**

| mix | Applications | MPKI |
|-----|--------------|------|
| #1 | zeusmp06 gobmk06 deallf06 bzip206 | 1.4 |
| #2 | hmmer06 bzip206 wrf06 roms17 | 2.6 |
| #3 | zeusmp06 cactuBSSN17 hmmer06 soplex06 | 6.1 |
| #4 | omnetpp06 star06 milc06 libquantum06 | 4.9 |
| #5 | xalancbmk06 soplex06 bwaves17 mcf17 | 10.4 |
| #6 | libm17 xz17 GemsFDTD06 wrf06 | 6.6 |
| #7 | cactuBSSN17 deallf06 libquantum06 xalancbmk06 | 7.3 |
| #8 | gobmk06 milc06 mcf17 libm17 | 6.0 |
| #9 | xz17 star06 bwaves17 soplex06 | 3.5 |
| #10 | GemsFDTD06 omnetpp06 roms17 leslie3d06 | 10.6 |

VI. FORECAST VALIDATION, COST, AND SPECIFIC SITUATIONS

To validate the forecast procedure it would be necessary to contrast its projections with data from the operation of real NVM caches as they age with a known workload. But unfortunately there is no such information in the public literature. Therefore, in this section we provide tests of the correctness of the assumed hypotheses as a function of the number of epochs employed, evaluating the tradeoff between accuracy and the time spent in the forecast procedure. Finally, we outline forecast alternatives for situations in which some underlying assumptions are not met.

A. Validation

As discussed in Sections IV-C and IV-D, the main source of forecast inaccuracy lies in the Prediction phase, where it is necessary to approximate the write rate of health states that have not yet appeared in the Simulation phase. Forecast with epochs of small extension involves little approximation and may improve the quality of the forecast, but increases its computational cost.

To explore this tradeoff between quality and cost, several experiments have been performed, using epochs of different
extension in each experiment, which predict a certain cache degradation. Specifically, we predict how much time elapses until 50% of the cache, \( T_{50C} \), degrades. The 50% degradation is a common case study \([19], [36], [45]\), and in our experiments we will also focus on it, but any other percentage, including 100%, corresponding to the total degradation could be used.

A different number of epochs of constant extension is used in each experiment. The epoch extension is the number \( k \) of consecutive predictions disabling frames or bytes, depending on the cache model, and is calculated by simply dividing 50% of the cache size, measured in frames or bytes, by the number of epochs.

The Y-axes in Figure 10 shows \( T_{50C} \) as a function of the number of epochs for frame disabling and three L2C2s built with bitcells of different manufacturing variabilities.

Fig. 10: Forecasted \( T_{50C} \) (in years) as a function of the number of epochs for frame disabling and L2C2 caches, with three coefficients of variation: \( cv = 0.2, 0.25, \) and 0.3.

As can be seen, the forecast of \( T_{50C} \) converges as the number of epochs increases for all coefficients of variation. Using a number of epochs greater than or equal to 8 and 16, \( T_{50C} \) varies less than 0.8 and 1.1% for frame disabling (\( k=16384 \) frames) and L2C2 (\( k=524288 \) bytes), respectively.

Previous works perform a single simulation from a fully operational NV memory to obtain the write rate data \([18], [19], [36], [37]\). From this data, they compute the time at which a bitcell dies, and then re-calculate the write rate analytically. In this sense, this methodology is similar to ours when a single epoch is used. But, as Figure 10 shows, in both cases but specially for compression, using a single epoch incurs in a non-negligible error as \( cv \) grows.

Finally, in order to prove that different RW maps do not lead to inconsistent results, five different random seeds have been used. The seeds are used to initialize different RW maps for the three values of \( cv \) and forecast is performed for all of them. Again, the convergence metric is \( T_{50C} \) in a 16-epoch forecast of an L2C2. The standard deviation of the different forecasted times is below 2% of the arithmetic mean.

B. Computational cost

As shown in Figure 10, after a certain number of epochs the forecast error is negligible, but its computational cost increases almost linearly. Table V shows the maximum elapsed times in individual Prediction and Simulation phases, as well as the total, for a forecast reaching up to 50% capacity degradation in an L2C2. These numbers have been obtained in a multicores AMD EPYC 7662 at 2GHz server with 100GB of main memory.

In view of the costs, in the rest of the paper we will perform 16-epoch forecast for all the experimented systems.

| #epochs | Simulation phase, minutes. | Prediction phase, minutes. | Forecast, days. |
|---------|---------------------------|---------------------------|-----------------|
| 16      | 210                       | 38                        | 2.8             |
| 32      | 210                       | 21                        | 5.1             |
| 64      | 210                       | 11                        | 9.8             |

C. Specific situations

In all the experiments performed in this work, our forecast procedure assumes a uniform distribution of writes among sets. This condition is met in most systems either because the workload is diverse over time and produces an even distribution, or because the cache incorporates good wear-leveling mechanisms among sets.

However, in some scenarios it may be important to take non-uniformity into account. As an example, we can think of an embedded system that always runs the same applications. Here the distribution of accesses to the cache sets may well be non-uniform, encouraging the design and comparison of mechanisms to even out the wear between sets.

Certainly, our forecast procedure could also be applied in this context, although the model that approximates the new write rates during the Prediction phase would have to be modified. In particular, the new model could no longer use the average write rate of all frames belonging to sets with a given health state. An alternative could be to obtain the approximation from the distribution of write rates of those frames. We think such specialized forecast is entirely feasible, but it is beyond the scope of this paper.

VII. Evaluation

This section shows the evolution of capacity and performance for several NV-LLC organizations, from 100% to 50% capacity, along with experiments on wear leveling, replacement, cache size and workload. For all tested organizations, the forecast procedure uses 16 epochs of constant extension.

We analyze four NV-LLCs candidates, two based on frame disabling and two on byte disabling plus compression:

- **Frame disabling cache (FD)**. A bitcell failure is just handled by disabling the corresponding frame \([6], [42]\). Frame endurance is increased allowing the failure of up to six bitcells. After the seventh failure, the frame is disabled, because an eighth failure would no longer be recoverable \([36]\). This is achieved by adding six ECPs per frame to the base SECDED mechanism.
L2C2. A bitcell failure is handled by disabling the corresponding byte. Cache blocks are stored compressed with BDI. It has an intra-frame wear-leveling mechanism and an LRU-Fit replacement policy; see Section III.

L2C2+6. An L2C2 with 6 spare bytes per cache frame; see Section III-E.

Two variations of L2C2 are also tested:

L2C2-NWL. It is an L2C2 without the intra-frame wear-leveling mechanism. The Index Calculation circuit has less complexity; see Section III-D3. Writing always starts at the least significant live byte of the frame.

L2C2-BF. It is an L2C2 with LRU-Best-Fit replacement policy instead of LRU-Fit.

Table VI shows the number of storage bits per frame of the tag and data arrays, along with the percentage increments with respect to FD.

### Table VI: Frame costs in bits. Percentage overhead relative to FD.

| SRAM Tag Array | STT-RAM Data Array |
|----------------|-------------------|
| Bits | Overhead, % | Bits | Overhead, % |
| FD | 34 | - | 529 | - |
| FD+6 | 34 | 0 | 595 | 12.5 |
| L2C2 | 38 | 11.8 | 594 | 12.3 |
| L2C2+6 | 38 | 11.8 | 648 | 22.5 |

#### A. Lifetime

Figure 11 shows forecasts of capacity degradation, from start-up until 50% of effective capacity is lost, considering bitcells with increasing manufacturing variabilities for the four NV-LLC candidates. The effective capacity shown on the Y-axis is the one contributing to cache block storage. For example, L2C2+6 has 100% effective capacity as long as its nominal 16MB capacity is available, regardless of whether or not the spare bytes are coming into play. Besides, Table VII shows $T_{50C}$, the time required to lose 50% of the nominal cache capacity.

First of all, it can be seen that FD manufactured with high variability starts with an effective capacity that may be well below the nominal one; i.e., an FD with $cv = 0.3$ starts operating with less than 80% of nominal capacity because many frames come out of production with defective bitcells; see Figure 11. FD+6, in contrast, completely solves this problem by adding redundancy. On the other hand, $T_{50C}$ decreases markedly for FD and FD+6 as the manufacturing variability increases, while for L2C2 and L2C2+6 it is the other way around; see Table VII. This is due to the byte-level disabling capability of L2C2, which tolerates early byte failures and takes advantage of the later ones.

Second, compared to the sharp drop observed in frame-disabling caches, the byte-disabling ones show a much more progressive degradation of capacity, resulting in a longer $T_{50C}$. L2C2 is the longest lived cache, in terms of $T_{50C}$ from 13.7 to 15.4 years, and FD the least, from 2.2 to 0.42 years, depending on $cv$. L2C2+6 last a little less than L2C2, but it is the one that maintains the nominal capacity for the longest time, namely $T_{99C}$, between 5.6 and 3.1 years, depending on $cv$; see Table VII. As an example, in terms of $T_{50C}$, see Table VII, L2C2 is alive 6, 11 and 37 times longer than FD for $cv$ values of 0.2, 0.25 and 0.3, respectively.

Third, as time goes by, and contrary to expectations, the effective capacity of L2C2+6 is no longer greater than that of L2C2, with the curves intersecting at around 7.5-5.5 years, depending on $cv$. As will be seen in the next subsection the explanation is as follows: before the curves cross, the L2C2+6 system maintains a higher IPC, which implies a higher write rate and a consequent earlier degradation.

#### B. Performance

Figure 12 shows the IPC forecast over time from start-up until 50% of effective capacity is lost for the NV-LLC candidates. The IPCs have been normalized to the IPC of a system with a fully impaired NV-LLC, i.e. with zero effective capacity. Before going into the analysis, notice the forecast procedure only provides IPC values after the simulation phase of each epoch, corresponding to the health state computed by the previous epoch. Intermediate IPC values within epochs are obtained by linear interpolation. However, should it be necessary to have a more precise IPC within an epoch, it is sufficient to halve the epoch extension once or several times. For instance, we observe that the first L2C2 epochs are long enough to halve the epoch extension once or several times. Note that the bottom dotted red line (0% EC) represents the IPC of a system with an NV-LLC with all bitcells operational. The bottom dotted red line (0% EC) represents the IPC of a system with an NV-LLC with all bitcells operational. The bottom dotted red line (0% EC) represents the IPC of a system with a fully impaired NV-LLC, i.e. with zero effective capacity.

Four observations can be highlighted from the curves. First, after losing 50% of capacity, the IPC with frame-disabling caches is around 20% higher than that of byte-disabling. This is because having 50% effective capacity with FD or FD+6 implies that 50% of frames can store any block, whereas with L2C2 and L2C2+6, it implies that the capacity of
all frames has been reduced and therefore some blocks cannot be stored in any frame.

Second, consistent with the effective capacity forecasts, the IPC degrades later and more gradually in L2C2 and L2C2+6. The steps seen in their lines correspond to periods in which the possibility of storing blocks of a given compression encoding has been lost.

Third, the crossings in the IPC and capacity curves occur at the same times. After these crossings, L2C2 performs slightly better and lasts slightly longer than L2C2+6. The reason is to be found in the first 4-6 years of operation of L2C2+6 at maximum performance, years that, compared to L2C2, cause a higher write wear.

And fourth, in the first years of operation L2C2+6 keeps the maximum performance, L2C2 loses it progressively, and FD and FD+6 loses it abruptly. The index $T_{99\%}$, the time during which performance holds above 99% of the maximum allows to quantify these facts; see Table VIIc. L2C2+6 excels at $T_{99\%}$ for all $cv$ values, with L2C2 in second place, except for $cv = 0.3$, where FD+6 is better.

From the above analysis, L2C2+6 seems to be the best candidate, followed by L2C2, and at some distance FD+6.

To get more insight, we propose to measure the work performed by the different organizations using the aggregate number of instructions executed by the four cores, with an utilization of 100%, until a certain wear-out condition is reached. We calculate this value with the integral of the CPI curve. Since according to Belkhir et al. the average lifetime of a server is three to five years, we propose the index $I_{50\%C|5y}$ which measures the number of instructions executed until 50% of the capacity is exhausted or until five years have elapsed, whichever is earlier; see Table VIIc.

Regarding this index, we can say that the increase in manufacturing variability is very bad for frame disabling, with reductions of 82 and 42% of $I_{50\%C|5y}$ in FD and FD+6, going from $cv$ 0.2 to 0.3. In contrast, that same increase in $cv$ slightly reduces $I_{50\%C|5y}$ in L2C2 and L2C2+6 by 5.5 and 2.5%, respectively.

In short, L2C2+6 offers the best performance in all indexes, with an additional storage cost over L2C2 and FD+6 of less than 10%. The second option, cheaper but with less performance, is L2C2, which requires about 12.3% more data array storage than FD, the base option without redundancy.

C. Intra-frame wear-leveling impact on lifetime

In this experiment we aim to see the importance of the intra-frame wear-leveling mechanism. In an L2C2 without intra-frame wear-leveling there is an imbalance between the number of writes that receive the low order bytes and the high order bytes of a frame. Concretely, higher order bytes will not be written if the block compressed to some extent. This imbalance will make lower order bytes receive more write operations than higher order ones so they will become faulty before than in a cache with intra-frame wear-leveling.
To model the L2C2 without wear-leveling, L2C2-NWL, the write rate is not averaged across the bytes of a frame. Thus, the rate used to age a byte depends not only on the compression class of the frame it belongs to, \( CC \), and the health state of the set, \( \bar{A} \), but also on the position the byte occupies among the live bytes in the frame.

Figure 13 shows the IPC evolution until the NV-LLC loses 50% of its effective capacity for \( cv = 0.2 \). IPC of L2C2-NWL starts dropping at 3.7 years while L2C2 IPC drops at 4.3 years (16% later). This temporal shift linking points of equal performance is evident throughout the duration studied, being around one year on many occasions.

**Figure 13: IPC evolution until losing 50% of capacity of an L2C2 without intra-frame wear-leveling mechanism, L2C2-NWL, for \( cv = 0.2 \).**

D. **Fit vs. Best-Fit replacement**

In L2C2 an alternative replacement policy to LRU-Fit is LRU-Best-Fit, which consists of choosing the smallest LRU frame capable of holding the incoming compressed block; see L2C2-BF in Figure 14. In principle, LRU-Best-Fit could be advantageous since it would preserve frames with larger capacity from writes, allowing in the long term the hosting of blocks with low compression capacity; see Section III-A1. However, L2C2-BF takes 8.9 years to lose 50% of its capacity, while L2C2 reaches the same loss at 13.7 years, i.e. 54% longer. Besides, the IPC drop L2C2-BF experiences at the early stages (0-2 years) is even more pronounced than that of FD. The explanation for both effects is that when the first frame in a set experiences the first byte failure, all the compressible blocks addressed to this set, 78% of the total, will be allocated to this recently degraded frame; see Figure 3 in page 6. This incurring in substantial conflict misses that degrade performance.

**Figure 14: IPC evolution until losing 50% of capacity of an L2C2 with LRU-Best-Fit replacement policy, L2C2-BF, for \( cv = 0.2 \).**

E. **Sensitivity analysis**

To further add generality to the results presented so far, we elaborate on three aspects; see Figure 15. First, the LLC bank size is increased from 4 to 8 MB per bank. Second, the system is scaled by a factor of 2, going from 4 to 8 cores, from 4 to 8 banks of NV-LLC and from 1 to 2 main memory controllers. And third, the workload mixes are changed, including only the top ten memory intensive applications; see applications with superscript in the Table IV.

Doubling cache capacity with the same number of cores extends performance over time to a similar amount across all cache organizations. For example, for L2C2+6, \( T_{50C} \) goes from 12.9 to 25.3 years when increasing size from 16 to 32 MB; see Figure 12a vs. Figure 15a.

By scaling the system, simultaneously doubling number of cores, cache size and memory bandwidth, the performance-time curves for all cache organizations maintain their shape; see Figure 12a vs. Figure 15b. This is an expected conclusion, which reinforces the possibility of incorporating L2C2-type caches in future generations of on-chip multiprocessors.

When considering more memory intensive applications a first observation is that the performance at full capacity exhaustion is lower, which indicates, not surprisingly, a higher dependence of performance on the quality of the memory hierarchy; see the red baselines (0% EC) in Figures 15c and 12a. In addition, the performance drop is sharper and occurs earlier. For example, for L2C2+6 the first drop is one year earlier and the relative IPC drops from 0.76 to 0.64. Again it can be reasoned that applications that exhibit intensive LLC usage are more sensitive to capacity loss, so overall system performance is more affected.

In summary, this sensitivity analysis shows that both the results and the forecast procedure itself are consistent when varying two significant dimensions, capacity and workload.

F. **Technological projections of lifetime and performance of NV-LLCs**

As we have explained so far, the forward-looking behavior of an NV-LLC can be estimated by applying a forecast procedure that has three key elements, namely, a statistical model of bitcell write endurance, a detailed simulation model of the NV-LLC organization, and a workload. In principle, a
new forecast with a change in any of these three elements requires a feasible, but high computation time.

All the results so far have been obtained for baseline bitcells with given endurances modelled with mean $\mu =$ 10$^{11}$ and $cv = 0.2 - 0.3$. To obtain results concerning other bitcell endurances and/or NV-LLC latencies, of course the whole forecast procedure can be repeated, creating new RW maps and changing the latencies in the simulation model.

However, as long as the NV-LLC latencies are assumed constant, it is possible to take advantage of the properties of the linear transformation of Gaussian distributions to reuse the forecast data and obtain projections for other NVM technologies with a different bitcell write endurance values.

Specifically, if an NV-LLC is built with an improved technology, which offers the same cache latencies, but uses bitcells with $k$ times more endurance ($\mu_i = k \cdot \mu_b$, $\sigma_i = k \cdot \sigma_b$), new capacity and IPC indices as a function of time can be calculated as follows:

- Cap. improved bitcells ($\bar{t}$) = Cap. baseline bitcells ($\bar{t}$)
- IPC improved bitcells ($\bar{t}$) = IPC baseline bitcells ($\bar{t}$)

That is, new indexes with improved bitcells at time ($t$) can be obtained from the forecast made with baseline bitcells at an earlier time ($\bar{t}$); see Appendix A.

Thus, from a few reference forecasts, many technology projections can be obtained. Table VIII is an example that focuses on two arbitrary, but interesting, indices: $T_{90C}$ and $T_{90P}$, calculated from the central column forecasts for $\mu =$ 10$^{11}$ and $cv = 0.2 - 0.3$. $T_{90C}$ and $T_{90P}$ are the elapsed times to reduce the rated capacity and performance, measured in IPC, to 90% of the initial values, respectively. Note that the values of $T_{90C}$ and $T_{90P}$ scale linearly with the value of $\mu$. That is, the value of $T_{90C}$ for $\mu =$ 10$^{12}$ is equal to 10 times the value of $T_{90C}$ for $\mu =$ 10$^{11}$. As it can be seen, $T_{90C}$ always trails $T_{90P}$ and L2C2+6 is the best cache organization.

These types of indices can serve as a basis for signing a Service Level Agreement, SLA, with prospective customers. It is plausible to think that a manufacturer can have a portfolio of NVM qualities and technologies and that a customer can choose the product with the best performance/cost ratio for her/his needs. For example, for a smartphone projected for a daily usage of 6 hours at 100% and with an average product life of 1.8 years several cache organizations and manufacturing variabilities of those shown in the $\mu =$ 10$^{11}$ writes/bitcell columns may fit. These figures could be representative of a technology with moderate write endurance, but comparatively inexpensive.

TABLE VIII: $T_{90C}$ and $T_{90P}$ for FD+6, L2C2 and L2C2+6, varying $cv$ and $\mu$; $m=$ months, $y=$ years.

| $cv$ | Cache | $T_{90C}$ | $T_{90P}$ | $T_{90C}$ | $T_{90P}$ | $T_{90C}$ | $T_{90P}$ |
|------|-------|----------|----------|----------|----------|----------|----------|
|      |       | 0.001    | 0.01     | 0.1      | 1.0      | 10.0     | 100.0    |
| 0.2  | FD+6  | 3.7m     | 3.9m     | 3.1y     | 3.2y     | 30.7y    | 32.2y    |
|      | L2C2  | 7.1m     | 7.2m     | 5.9y     | 6.0y     | 58.9y    | 60.1y    |
|      | L2C2+6| 7.7m     | 7.8m     | 6.4y     | 6.5y     | 63.8y    | 64.7y    |
| 0.25 | FD+6  | 2.8m     | 3.1m     | 2.4y     | 2.5y     | 23.5y    | 25.4y    |
|      | L2C2  | 5.7m     | 5.8m     | 4.7y     | 4.9y     | 47.3y    | 48.7y    |
|      | L2C2+6| 6.4m     | 6.5m     | 5.3y     | 5.4y     | 53.1y    | 54.2y    |
| 0.3  | FD+6  | 2.0m     | 2.2m     | 1.6y     | 1.9y     | 16.4y    | 18.6y    |
|      | L2C2  | 4.5m     | 4.7m     | 3.7y     | 3.9y     | 37.3y    | 39.1y    |
|      | L2C2+6| 5.1m     | 5.3m     | 4.3y     | 4.4y     | 42.3y    | 43.8y    |

VIII. CONCLUSION

We have introduced L2C2, a new fault-tolerant NV-LLC organization that achieves per-byte write rate reduction without performance loss and allows compressed blocks to be placed in degraded frames. L2C2 evenly distributes the write wear in all frames, further extending the time in which the cache remains in degraded frames. L2C2+6 evenly distributes the write wear in all frames, further extending the time in which the cache remains in degraded frames. L2C2+6 is the best cache organization.

These types of indices can serve as a basis for signing a Service Level Agreement, SLA, with prospective customers. It is plausible to think that a manufacturer can have a portfolio of NVM qualities and technologies and that a customer can choose the product with the best performance/cost ratio for her/his needs. For example, for a smartphone projected for a daily usage of 6 hours at 100% and with an average product life of 1.8 years several cache organizations and manufacturing variabilities of those shown in the $\mu =$ 10$^{11}$ writes/bitcell columns may fit. These figures could be representative of a technology with moderate write endurance, but comparatively inexpensive.

Fig. 15: IPC evolution until losing 50% of capacity of FD and L2C2 for $cv = 0.2$, doubling cache size (a), doubling the number of cores while keeping the same 4MB/core (b), and considering the most memory-intensive programs (c).
This methodology has allowed us to compare several NV-LLC organizations in terms of lifetime and performance. It has also allowed us to measure the influence of manufacturing process variability on these results.

Our evaluation shows that, with an affordable hardware overhead, L2C2 achieves a large lifetime improvement compared to a reference NV-LLC provided with frame disabling. The lifetime is multiplied by a factor from 6 to 37 times depending on the variability in the manufacturing process. Increasing redundancy significantly increases the time to loss of performance by one to two years in all configurations, regardless of the variability in the manufacturing process. However, it does not increase the lifetime of the L2C2.

Knowledge of how performance evolves through time could be essential for manufacturers to be able to incorporate NVM technologies with the confidence that they can guarantee certain performance for a reasonably appealing time period.

Finally, the new forecast procedure leaves the door open to detailed evaluation of different cache organizations, varying, for example, content management policy between cache levels, replacement policy, or wear-levelling.

### APPENDIX A. TIME SCALING OF FORECASTED INDEXES WHEN CONSIDERING BITCELLS WITH MORE ENDURANCE

Let

\[ N(w_b; \mu, \sigma) = \frac{1}{\sigma \sqrt{2\pi}} e^{-\frac{(w_b - \mu)^2}{2\sigma^2}} \]  

be the normal probability distribution function that estimates the number of writes \( w_b \) causing failure in a baseline bitcell. Assuming a constant write rate \( WR \) (writes/s) on the baseline bitcell, the probability distribution function of the failure time \( t_b \) can be obtained from Eq. 1 by the linear transformation \( t_b = \frac{w_b}{WR} \).

\[ N(t_b; \frac{\mu}{WR}, \frac{\sigma}{WR}) \]  

We can characterize an improved bitcell, with \( k \) times higher endurance, by applying to Eq. 1 and the linear transformation \( w_i = w_b \cdot k \). Thus, the probability distribution functions of the number of writes and failure time for the improved bitcell are, respectively:

\( N(w_i; \mu \cdot k, \sigma \cdot k) \) and \( N(t_i; \frac{\mu \cdot k}{WR}, \frac{\sigma \cdot k}{WR}) \).

On the other hand, the probability of failure of the baseline bitcell, \( P_b \), at a time \( t_b \leq t \) is:

\[ P_b(t_b \leq t) = \int_0^t N(t_b; \frac{\mu}{WR}, \frac{\sigma}{WR}) dt_b \]  

To know the probability of failure of the improved bitcell, \( P_i \), at a time \( t_i \leq t \) from \( P_b \), it is necessary to apply another linear transformation: \( t_b = \frac{t_i}{k} \). Thus:

\[ P_i(t_i \leq t) = P_b(t_b \leq \text{lin\_trans}_{t_i \rightarrow t_b}(t_i)) = P_b(t_b \leq \frac{t}{k}) \]  

Rewriting the two probabilities as a function of \( t \), we have:

\[ P_i(t) = P_b\left(\frac{t}{k}\right) \]  

To conclude, let us consider a cache with \( c \) baseline bitcells, each with an endurance approximated by the probability distribution of Eq. 1 and subjected to a constant per-cell write rate \( WR \) (writes/s). Assuming bit granularity the decrease of its effective capacity with time, \( C_{eff}(t) \) is:

\[ C_{eff}(t) = C \cdot (1 - P_b(t)) \]  

And for a cache of the same size made with improved bitcells:

\[ C_{eff}(t) = C \cdot (1 - P_b\left(\frac{t}{k}\right)) \]

In this case, with byte granularity and different write rates in each frame, it can be reasoned in the same way. That is, any forecasted index with enhanced cells at time \( t \) matches the same index forecasted with base cells but at time \( \frac{t}{k} \).

### ACKNOWLEDGEMENTS

All authors acknowledge support from grants (1) PID2019-105660RB-C21 and PID2019-107255GB-C22 / AEI / 10.13039/501100011033 from Agencia Estatal de Investigación (AEI) and European Regional Development Fund (ERDF), (2) guZ: T58_20R research group from Aragón Government and European Social Fund (ESF), and (3) 2014-2020 “Construyendo Europa desde Aragón” from European Regional Development Fund (ERDF). The funders had no role in study design, data collection and analysis, decision to publish, or preparation of the manuscript.

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