FPGA based design for online computation of Multivariate EMD (MEMD)

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Abstract—Multivariate or multichannel data have become ubiquitous in many modern scientific and engineering applications, e.g., biomedical engineering, owing to recent advances in sensor and computing technology. Processing these data sets is challenging owing to: i) their large size and multidimensional nature, thus requiring specialized algorithms and efficient hardware designs for on-line and real-time processing; ii) the nonstationary nature of data arising in many real life applications demanding new extensions of standard multiscale non-stationary signal processing tools. In this paper, we address the former issue by proposing a fully FPGA based hardware architecture of a popular multi-scale and multivariate signal processing algorithm, termed as multivariate empirical mode decomposition (MEMD). MEMD is a data-driven method that extends the functionality of standard empirical mode decomposition (EMD) algorithm to multichannel or multivariate data sets. Since its inception in 2010, the algorithm has found wide spread applications spanning different engineering related fields. Yet, no parallel FPGA based hardware design of the algorithm is available for its on-line and real-time processing. Our proposed architecture for MEMD uses fixed point operations and employs cubic spline interpolation within the sifting process. Finally, examples of decomposition of multivariate synthetic and real world biological signals are provided.

Index Terms—Multivariate signals, multivariate empirical mode decomposition, FPGA, time frequency methods

I. INTRODUCTION

Empirical mode decomposition (EMD) [1] is a data-driven technique that is widely used for the decomposition and time-frequency (T-F) analysis of nonlinear and non-stationary signals. Unlike traditional multi-scale data analysis techniques, such as Fourier and Wavelet transform, that use fixed a priori basis function for decomposition, EMD effectively employs local data adaptive basis functions for decomposition of data. To achieve that, EMD adopts an iterative sifting process to decomposes signal into its multiple inherent scales with distinct features, known as intrinsic mode functions (IMFs).

The IMFs are designed such that they are zero-mean and term as multivariate empirical mode decomposition (MEMD). It uses a sifting process, similar to EMD, for decomposition of multivariate signals into multidimensional IMFs.

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For multivariate signals with two channels only (bi-variate signals), the FPGA-based parallel design for computation of bi-variate EMD [25] was proposed in [23]. The design is implemented on Xilinx Kintex 7 FPGA and can operate up to maximum operating frequency of 24 MHz. However, it uses linear interpolation instead of more established cubic spline interpolation (CSI) to implement the sifting process that compromises its accuracy.

There are currently no FPGA based fully hardware architectures for computing the multivariate EMD (MEMD) algorithm. Given the massive appeal of the MEMD method in real life multichannel data sets, we propose the first-ever fully FPGA based fixed-point architecture for multivariate EMD algorithm. The proposed design uses accurate cubic spline interpolation (CSI) scheme for the sifting process within MEMD thus fully ensuring the accuracy of the implementation. Moreover, the parallel structure of the proposed design enables processing of multiple channels of input data simultaneously, resulting in higher throughput of the system. We present a detailed timing analysis, hardware resource utilization of proposed architecture in addition to a thorough comparison with the state-of-the-art. The design is verified and evaluated on a number of synthetic and real life multivariate signals.

The rest of paper is organized as follows: Section II reviews the MEMD algorithm. The implementation of proposed design is presented in Section III. The experimental result of synthetic and real world data sets with discussion is presented in section IV. Finally, Section V presents the conclusions and future avenues for research in this area.

II. REVIEW OF MEMD ALGORITHM

MEMD is multivariate extension of the EMD algorithm that has gained remarkable success in applications involving multichannel data processing e.g. image fusion [26], biomedical engineering [27] and condition monitoring [28]. MEMD decomposes multivariate signal into its intrinsic multiply oscillatory modes, known as multivariate intrinsic mode function (IMFs). MEMD uses the sifting process to decomposes input multivariate data $\bar{X}(t)$ into multivariate finite no of IMFs $\bar{C}_j(t)$, written as:

$$\bar{X}(t) = \sum_{j=1}^{M} \bar{C}_j(t) + \bar{r}(t). \quad (1)$$

where $M$ is the number of decomposed IMFs from the multivariate input data sets and $\bar{r}(t)$ is residue signal. The IMFs $\bar{C}_j(t)$ is defined by function that satisfy the following two conditions:

I. The number of zero-crossings and extrema points must either equal or differ at most by one.

II. The local mean envelopes must be equal to zero which are defined by local maxima and local minima.

In standard EMD, the local mean is calculated by averaging the upper and lower envelope. However, the local mean of multi-dimensional signals cannot be generated like as in standard EMD. In MEMD, multiple n-dimensional envelopes are calculated by projecting the multi-dimensional signal along different directions in n-dimensional space and the corresponding local means are then calculated by averaging the envelopes from those projections. Hammersley sequences are used to acquire quasi-uniform points on high dimensional spheres [29], [30] for uniform set of direction vector. The details of MEMD Algorithm is presented in Algorithm 1. The local mean of MEMD is estimated by computing the multiple real-valued projections and taking the local mean of corresponding envelopes.

Algorithm 1 The Sifting Process in MEMD [13]

1. Generate the point set using Hammersley sequence that used for sampling a $n(n - 1)$ sphere.
2. Calculate a projection of the input signal $\bar{X}(t)$ along the direction vector $K$, giving as the set of direction vector.
3. Locate the extrema (maxima and minima) point from the set of projected signal and its corresponding time instants.
4. Interpolate extrema point corresponding time instants to acquire multivariate envelope curves.
5. The local mean $m(t)$ of multiple envelopes for $K$ direction vector is given by:

$$m(t) = \frac{1}{K} \sum_{n=1}^{K} e^{\theta_n(t)} \quad (2)$$

6. The oscillatory mode $\bar{h}(t)$ is obtain by subtracting local mean $m(t)$ from the input signal

$$\bar{h}(t) = \bar{X}(t) - m(t);$$

7. If $\bar{h}(t)$ meets the stopping criteria as stated above, then define $\bar{C}_j = \bar{h}(t)$ as an IMF, otherwise set $\bar{X}(t) = h(t)$ and repeat the procedures from step 1.

III. FPGA BASED ARCHITECTURE FOR MULTIVARIATE EMD

We exploit the inherent parallelism of the MEMD algorithm to efficiently implement it on FPGA using parallel and pipeline structure. The proposed design employs both fixed-point format and CSI within sifting process of MEMD. FPGA-based design for the on-line computation of multivariate extension of
EMD (MEMD) is presented in this section. The overall block diagram of the proposed architecture is presented first and then subsequent individual modules are discussed in detail.

A. Architectural design of multivariate extension of EMD

Fig. 1 shows the operational flow of the proposed hardware design for the computation of MEMD. The block diagram is divided into two levels. The upper portion of Fig. 1 shows level 1 where different IMFs are calculated using pipeline architecture. At level 2, multiple iteration blocks are cascaded in the pipeline as shown in the lower portion of Fig. 1 where the sifting process is performed.

The input signal \( \bar{X}(t) \) denotes a 16-bit multichannel data which is fed to the multivariate IMF generator block to generate the first IMF \( \bar{C}_1(t) \). The IMF generator block also produces the multi-dimensional residue \( \bar{r}_1(t) \), by subtracting \( \bar{C}_1(t) \) from the input signal \( \bar{X}(t) \). The residue \( \bar{r}_1(t) \) is then fed to the second stage of IMF generator as an input to produce the second IMF \( \bar{C}_2(t) \). In our design, the \( M \) number of IMF generator blocks are cascaded to produce the \( M \) number of IMFs and a residue. This is flexible as multiple IMF generator blocks can be cascaded depending on the number of required IMFs.

The lower portion of Fig. 1 shows the IMF generator block where sifting process is performed by using a pipelined structure. Note that \( S \) number of sifting blocks are used in our design for obtaining a single IMF, in accordance with the \( S \)-number stopping criterion [31] of EMD. The first sifting operation produces the output \( h_1(t) \) that becomes the input to the second iteration block for the computation of \( h_2(t) \). Similarly, the output of the second iteration, \( h_2(t) \), becomes input to the third iteration block and so on. The output \( h_S(t) \) of the last sifting block becomes the first IMF from the sifting process i.e., \( \bar{C}_1(t) = h_S(t) \).

B. Sifting process

The sifting process is the core component for the computation of MEMD. Sifting process involves multiple iteration blocks to compute each IMF. The proposed architecture for a single iteration block to calculate the sifting process within MEMD is shown in Fig 2. The iteration block is composed of a signal projection module, Hammersley sequence generator, extrema identification module, local mean module (for each channel) and different memory units for data storage.

The sifting process starts with the calculation of \( K \) number of direction vectors by using pre-generated Hammersley sequence. Hammersley sequence is pre-generated and stored on the block memory of FPGA. The input signal \( \bar{X}(t) \) is concurrently stored on dual-port block RAM. The signal projection module is next utilized to project \( \bar{X}(t) \) along \( K \) direction vectors to compute the projected signals \( \{y_1(t), y_2(t), ..., y_K(t)\} \).

1) Signal Projection: The signal projection module is shown in Fig. 3. It uses Hammersley sequence which is pre-calculated and stored on a ROM. The input signal \( x_{1}^{N} \) is projected along multiple direction vectors to generate \( K \) number of projected signals. The \( k \)-th such projection is given by:

\[
y_k(t) = a_1^k x_1(t) + a_2^k x_2(t) + ... + a_N^k x_N(t)
\]

where \( a_{ik} \) are the coefficients of the Hammersley sequence that are used to obtain the signal projection along the \( k \)-th direction.

In Fig. 3, the architecture used for the computation of (3) is shown. As the coefficients of Hammersley sequence \( a_{ik}^k \) are fixed values, they are stored in the ROM. We employ canonical signed digit (CSD) based multiplication within the signal projection module as the coefficients of the Hammersley sequence are constants. The multiplication with the constant is replaced by shift operations and additions within CSD multiplication to increase the throughput of the system.

2) Extrema identification: The sifting process of MEMD involves envelope generation for each projected signal \( y_k(t) \). To achieve that, extrema values of the projected signals are detected along with their corresponding time instants. Both sets of values are stored in FIFOs. The extrema points are detected using the extrema identification module, as shown in Fig. 4. The extrema identification module takes three input
data values $y_{n-1}, y_n$ and $y_{n+1}$ to detect an extremum. These input values are sequentially loaded to extrema identification module at every clock cycle.

Two comparators are used to compare $y_n$ with $y_{n-1}$ and $y_{n+1}$ separately. If $y_n$ is greater than or equal to $y_{n-1}$, the first comparator generates a high signal. Similarly, the second comparator generates a high signal whenever $y_n$ is greater than or equal to $y_{n+1}$. The outputs from both comparators become high signal have both extrema as well as minima, therefore, therefore, $2K$ number of extrema generation modules are used in the proposed architecture. The time indices of extrema are further used in local mean module for calculation of local mean, which is explained next.

### C. Local Mean Generation

The local mean of a multivariate signal is generated based on multiple signal envelopes in $K$ number of directions and for $N$ number of input channels. In the proposed design, the local mean is calculated in parallel as shown in right hand side of Fig. 7. The local mean block for each channel is connected in parallel to calculate $h_k(t)$, a potential candidate for IMF. Therefore, the $N$ number of local mean blocks are used to calculate $h_1(t)$ as follows:

$$h_1(t) = \{h^1_1(t), h^1_2(t), ..., h^N_1(t)\}$$  \hspace{1cm} (4)

where $h^1_1(t)$ is the local mean of channel 1 and $h^1_N(t)$ is the local mean corresponding to the channel $N$.

The proposed design to compute local mean $h^1_i(t)$ corresponding to the $i - th$ channel is presented in Fig. 5. The $N$ number of such blocks are required to compute the local mean $h_1(t)$. To compute $h^1_i(t)$, multiple signal envelopes in $K$ number of directions are required. In order to generate those envelopes, firstly, time instants of each projected signals’ extrema are taken from the FIFO and corresponding extrema values are extracted from the input data $x_i(t)$ of $i - th$ channel which is stored in RAM. The extrema value and their associated position for $K$ number of projected signals are stored in $2K$ number of dual-port RAMs. These extrema values and their associated indices are further used to calculate multiple $2K$ number of signal envelopes, denoted by $V_1(t), V_2(t), ..., V_{2K}(t)$, by using cubic spline interpolation (CSI) module that will be discussed in the next section. These multiple signal envelopes are then used to calculate mean
The local mean for a single channel is finally calculated by subtracting mean \( m_i(t) \) from the input signal i.e. \( h_i(t) = x_i(t) - m_i(t) \). Similarly, \( N \) numbers of local mean are calculated using (4) as the local mean module is cascaded in parallel for each channel to complete the sifting process within MEMD.

D. CSI hardware implementation

Cubic spline interpolation (CSI) is one of the most computationally extensive task within any EMD based algorithm. That also applies to MEMD. Therefore, for real time on-line implementation of the MEMD algorithm, we have used the CSI design from our previous published work [22]. It required only three extrema points and their indices for the formation of spline. The cubic spline operation involves third degree powers of the input parameters and involves four coefficients, as shown in the equation below [22]:

\[
q_j(x) = a_j + b_j(x - x_j) + c_j(x - x_j)^2 + d_j(x - x_j)^3.
\]  
(6)

where the coefficients \( a_j, b_j, c_j \) and \( d_j \) are given by

\[
a_j = f(x_j) = f_i,
\]
\[
c_j = k_i,
\]
\[
b_j = \frac{1}{h_j}(a_{j+1} - a_j) - \frac{h_j}{3}(2c_j + c_{j+1}),
\]
\[
d_j = \frac{c_{j+1} + c_j}{3h_j}.
\]  
(7)

Note that \( h_j = x_{j+1} - x_j, f_i \) is the value of function \( f \) at point \( x_j \) and \( k_j \) denotes the derivative of the spline function. It is calculated by using free or natural conditions of the cubic spline and then solved by using tridiagonal matrix algorithm (TDMA), also called the Thomas algorithm [32].

The architectural block diagram of the CSI design module is shown in Fig. 6. The CSI block consists of a tridiagonal matrix algorithm sub-block (TDMA) in addition to the CSI-coefficient and CSI-formation modules. The block takes three extrema values \( M_i \) along with their indices \( X_i \) from the dual port RAM to calculate the spline according to (6).

The Tridiagonal matrix algorithm is used to calculate the \( a_i \) and \( k_i \). The lower portion of the Fig. 6 calculates \( k_i \) by using (7). The division operation in the (7) is implemented through a look-up table. Since \( h_i \) is always a positive number, therefore, a small-sized look-up table can be used to perform the division operation, which decreases the execution time of the proposed design. The CSI-coefficient module is used to calculates \( a_j, b_j, c_j, d_j \), which are the coefficient of the spline, via (7). The CSI-formation block uses the above coefficient along with \( x \) to perform the cubic spline interpolation. Here, \( x \) indicates the time indices of the envelope that need to be interpolated.

Our architecture computes on-line MEMD, therefore, once the CSI process is completed for a certain signal interval, the next three extrema value are taken from the RAM to generate the signal envelope for those extrema values. The process is repeated until the \( K \) signal envelopes are completed.

IV. RESULTS AND ANALYSIS

In this section, we have reported the performance of the proposed design by conducting several experiments on both multivariate synthetic and real-world electroencephalogram (EEG) signals. The IMFs acquired from the proposed hardware design have been validated in terms of their accuracy and execution time.

The proposed hardware for MEMD computation was implemented on Xilinx FPGA (Xilinx Virtex-7 FPGA VC707 Evaluation Kit) using Verilog programming. The Xilinx ISE Design Suite 14.7 was used to synthesize the Verilog code and the results were presented after post-synthesis, place and route procedure. In the proposed design, we used low-discrepancy Hammersley sequence to generate a set of \( K = 8 \) directions vector for taking signal projections. The design was tested for \( N = 4 \) number of input channels. The stopping criteria for the sifting process used \( S = 4 \) number of iterations. Fixed-point data format of Q16.8 was used in our design.

A. Case Study 1: Decomposition of Synthetic Data

The proposed implementation for MEMD was evaluated on a synthetic quadri-variate (four channels) signal. Each channel was constructed from set of four pure tones: \( f_1 = 50 \text{ kHz}, f_2 = 150 \text{ kHz}, f_3 = 350 \text{ kHz} \) and \( f_4 = 800 \text{ kHz} \). One sinusoid signal \( f_3 \) was kept common in all input channels. The \( X(t) \) is the resulting quadri-variate input signal consisting of \( \{x_1(t), x_2(t), x_3(t), x_4(t)\} \) components, which are individually given as

\[
x_1 = 150 \sin(2\pi f_1 t) + 150 \sin(2\pi f_2 t) + 150 \sin(2\pi f_3 t),
\]
\[
x_2 = 150 \sin(2\pi f_1 t) + 150 \sin(2\pi f_4 t),
\]
\[
x_3 = 150 \sin(2\pi f_2 t) + 150 \sin(2\pi f_3 t) + 150 \sin(2\pi f_4 t),
\]
\[
x_4 = 150 \sin(2\pi f_1 t) + 150 \sin(2\pi f_2 t) + 150 \sin(2\pi f_3 t).
\]  
(8)

The sampling frequency of the input signal was taken to be \( F_s = 30 \text{ MHz} \). The input signal \( X(t) \) is shown in Fig. 7.

The \( X(t) \) was given to the proposed MEMD design for the decomposition of the signal into \( M = 4 \) IMFs. The resulting IMFs are shown in Fig. 8. It can be noticed from the Fig. 8 that all original tones, with frequencies \( f_1 = 50 \text{ kHz}, f_2 = 150 \text{ kHz}, f_3 = 350 \text{ kHz} \) and \( f_4 = 800 \text{ kHz} \), have been decomposed accurately by the proposed architecture. We also
such signals. To that end, our work is particularly relevant of applications in biomedical signal processing. Moreover, signals, data-driven multiscale approaches have found a lot of EEG data

TABLE I: Correlation of the decomposed IMF with ground truth (pure tones).

| Correlation coefficient (COR) | Channel (01) | Channel (02) | Channel (03) | Channel (04) |
|-------------------------------|--------------|--------------|--------------|--------------|
| $C_1(t)$& $f_4 = 8000kHz$       | 0.997        | 0.104        | 0.997        | 0.104        |
| $C_2(t)$ & $f_3 = 350kHz$     | 0.989        | 0.992        | 0.988        | 0.99         |
| $C_3(t)$ & $f_2 = 150kHz$     | 0.005        | 0.112        | 0.936        | 0.936        |
| $C_4(t)$ & $f_1 = 50kHz$      | 0.985        | 0.996        | 0.025        | 0.944        |

It can be noticed from the figure that the $10Hz$ frequency component(s), corresponding to alpha rhythms, are decomposed in the fourth IMF ($C_4$) of each channel. The first IMF mostly picks up very high frequency components from EEG which may be present due to noise and/or other unexplained brain phenomenon. There are some cases of mode-mixing across IMFs, however, which may be present due to inherent limitations of the EMD-based approaches. The power spectral density (PSD) of the IMFs of each channel are also shown in Fig. [I] to validate our observations. It is evident from the PSD estimation that the fourth IMF $C_4$ shows a peak around $10Hz$ signal confirming its status as $\alpha$ wave. The overlapping of power spectra from multiple channels of same-index IMFs in Fig. [I] highlight the mode alignment property of MEMD. The ability of MEMD to i) separate nonstationary data into its constituent frequency components, and ii) aligning similar frequency components across multiple channels in same indexed IMFs, makes it a powerful and viable tool in several biomedical related applications.

C. Hardware resources utilization and Timing analysis

Hardware resources utilization and computational timing analysis of the proposed architecture is reported in this section. The prototype of the proposed architecture was developed using Xilinx Vortex-7 FPGA VC707 Evaluation platform (FPGA Vortex-7, XC7VX485T). The detail about hardware resources, the operating frequency and the slices used for the proposed architecture is reported in Table [III]. It can be noticed that the proposed design utilized 73% slice LUTs, 11% slice register and 10% DSP 48EI slices from the available resources.
Fig. 7: Synthetic quadri-variate input signal consisting of channels $x_1(t), x_2(t), x_3(t)$ and $x_4(t)$, from left to right.

Fig. 8: Decomposition of the quadri-variate synthetic signal into multivariate IMFs $\tilde{C}_1, \tilde{C}_2, \tilde{C}_3$ and $\tilde{C}_4$ using the proposed MEMD based architecture.

Fig. 9: Time plot of four channel input EEG signal.

The Table III gives timing analysis of the proposed architecture. Our design decomposes multivariate signals into $M = 4$ IMFs with the maximum operating frequency of 31MHz. The design uses at least three extrema points to start the computation process, hence, there is an initial delay of 0.56 $\mu$s to fill the pipeline stages at the start. Moreover, each iteration of the sifting process is computed using a pipeline architecture that increases the throughput of the system. Similarly, IMFs are also computed in a pipelined fashion for every channel.

Table II: Hardware Utilization Of The Proposed Architecture Using Virtex-7, XC7VX485T-2FFG1761

| Logic Utilisation                  | Used | Available | Total Utilisation |
|------------------------------------|------|-----------|------------------|
| No. of Slice Registers            | 66906| 607200    | 11%              |
| No. of Slice LUTs                 | 222538| 303600   | 73%              |
| No. of fully used LUT-FF pairs    | 13930| 275514    | 5%               |
| No. of bonded IOBs                | 322  | 700       | 46%              |
| No. of BUFG/BUFGCTRLs             | 3    | 32        | 9%               |
| No. of DSP 48E1s                  | 288  | 2800      | 10%              |

The computation time required to decomposition of first IMF for all channels was 36.5 $\mu$s for 1000 samples. Our proposed architecture only took 49.1 $\mu$s to decompose multivariate signals into four number of IMFs and a residue. Moreover, the proposed design attained throughput of 1295 Mbps.
Fig. 10: Decomposition of multivariate EEG signal into IMFs $C_1$, $C_2$, $C_3$, $C_4$ and residue $r$.

Fig. 11: Power spectral density (PSD) of decomposed EEG signal ($C_1$ (top left), $C_2$ (top right), $C_3$ (lower left), and $C_4$ (lower right)).

TABLE III: Timing Analysis Of The Proposed Design

|                              |                  |
|------------------------------|-----------------|
| **Sampling frequency/clock rate** | 31 MHz          |
| **Initial delay for single iteration** | 0.65 µs        |
| **Computational time for IMF1/1000 samples** | 36.5 µs        |
| **Computational time for IMF2/1000 samples** | 40.70 µs       |
| **Computational time for IMF3/1000 samples** | 44.9 µs        |
| **Computational time for IMF4/1000 samples** | 49.1 µs        |
| **Computational time for residue/1000 samples** | 49.1 µs        |
| **Overall data throughput**    | 1295 Mbps       |
V. DISCUSSION AND CONCLUSIONS

We have proposed a parallel FPGA-based hardware architecture for multivariate extension of EMD algorithm. The design is suitable for on-line decomposition of multivariate signals in real-time. The best of our knowledge, no fully FPGA-based hardware for generic multivariate extension of EMD currently exists. For a specific case of bivariate signals, however, a parallel hardware design for computing bivariate extension of EMD (BEMD) was proposed in [23]. Since our design can handle bivariate signals as a special case, it would be pertinent to compare our architecture with [23]. The main algorithmic differences between BEMD and MEMD include: i) Unlike BEMD, MEMD can decompose more than two-channel signals; ii) projection vectors in MEMD are generated in N-dimensional spaces using low-discrepancy Hammersley sequence as opposed to uniform vectors in 2D in the case of BEMD.

In terms of architectural design, the differences are as follows. Firstly, [23] implemented linear interpolation scheme, also termed as sawtooth interpolation (STI), to generate envelopes within sifting process. Our proposed design for MEMD, on the other hand, implements a more accurate and well-established CSI scheme for the sifting process. Secondly, the design in [23] used integer format that severely compromised its accuracy. Our architectural design of MEMD is based on fixed-point format which improves its overall precision and accuracy. The processing time of BEMD [23] for 1000 input samples was 58.4\(\mu\)s whereas the proposed architecture required 49.1\(\mu\)s to decompose 1000 samples of a 4-channel data set. This is because the proposed design uses look-up table for division operation to calculate spline and uses CSD based multiplication within the projection module. The maximum achieved clock rate for the proposed architecture is 31MHz as compared to 25MHz for the BEMD architecture given in [23].

As compared to the graphical processing unit (GPU) based implementation of MEMD [24], the proposed FPGA-based hardware architecture offers the following advantages: i) delivery of high computational density per watt; ii) less power dissipation; iii) on-line and real time processing of multivariate data since the design in [24] can only perform batch processing. GPU based system has one major disadvantage, which is challenging for online real-time applications. i.e., data transfer overhead from host system (CPU) to the memory of GPU. This data transfer overhead increases the overall execution time of the system. All the above attributes make the FPGA based design a more viable option for on-line portable applications such as in biomedical engineering.

One limitation of the proposed architecture is that it could only use up to 8 direction vector within sifting process due to resource limitation on FPGA platforms. Parallel architectures with possibility of even higher number of direction vector can improve the accuracy of the design further; which can be possible to implement on ultra-scale version of the FPGAs.

### TABLE IV: Comparison between state of art design

|                     | BEMD-Lin [23]                        | Proposed design |
|---------------------|--------------------------------------|-----------------|
| Cock rate (MHz)     | 25                                   | 31              |
| No of Input channel | 2                                    | 4               |
| Direction vector    | 8                                    | 8               |
| Processing Time     | 58.4\(\mu\)s for 1000 sample         | 49.1\(\mu\)s for 1000 sample |
| Throughput (Mips)   | 125 for STI                          | 1295 for CSI/STI |
| Hardware Platform   | Xilinx Kintex-7, (XC7K480T)           | Xilinx Virtex-7  |
|                     | FPGA                                 | (XC7VX485T)     |
| Interpolation technique | STI                                   | STI, CSI        |
| Architecture        | Pipeline                              | Pipeline (STI, CSI) |
| Data format         | Integer                              | Fixed point     |

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