A fast and low-power level shifter for multi-supply voltage designs

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Abstract This paper proposes a high-speed and ultra-low power level shifter (LS) capable of realizing wide-range voltage level conversion. Two key features are contained in the presented LS to support its superior performances. First, a novel boost control circuit is proposed to boost input voltage and strengthen pull-down driven capability, which results in significant improvement of operation speed and conversion range. Second, multi-threshold COMS (MTCMOS) and sub-threshold device sizing techniques are employed to reduce the static current, thereby obtaining ultra-low leakage power consumption. Post-layout simulation results demonstrate that the proposed LS implemented with SMIC 55-nm technology can convert 140 mV low-voltage to 1.2 V. Meanwhile, when evaluated with the low supply voltage of 0.3 V at 1 MHz frequency, the transition energy of the presented LS is 87.35 fJ. Moreover, the static power consumption and propagation delay are only 64.2 pW and 18.07 ns, respectively.

Keywords: level shifter, multi-supply voltage, sub-threshold circuit, low power

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

Currently, the power dissipation of system-on-chips (SoCs) has become a prior design concern, driven by increased circuit complexity and miniaturized power sources [1, 2, 3, 4]. Scaling down the supply voltage to near/sub-threshold region is one of the most practical methods to reduce the power consumption of digital circuits [5, 6]. This technique has been widely adopted in many low-power systems, such as wireless sensor nodes, biological systems, and other battery-less applications [7, 8]. There is no doubt that sub-threshold operations make better use of the energy budget. However, the lower voltage increases propagation delay, which is unacceptable for high-performance required systems. Multi-supply voltage (MSV) technology, as an effective solution to this bottleneck, separates a system into several power domains according to timing requirements, and provides different supply voltages [9, 10]. As a result, MSV circuits obtain power consumption reduction without sacrificing performance. Level shifters play an imperative role in MSV circuits, which are ubiquitously inserted into the boundaries of different power domains to realize voltage level conversions [11]. In order to mitigate the performance debasement of the overall system, the power consumption and transmission delay of LS require as small as possible. Moreover, the LS should have a wide conversion range to support sub-threshold operations for low supply voltage domains.

There are two types of conventional LSs, including current-mirror (CM) structure and differential cascade voltage switch (DCVS) structure, as shown in Fig. 1 (a) and (b). The structure based on (a) adopts a current mirror to accelerate converting. However, when the voltage of the input signal is “high” (VDDL), it suffers considerable static power dissipation caused by the leakage current flowing through the transistors of the left branch (MP1, MN1). This structure is not suitable for ultra-low-power systems. The scheme in (b) is based on a cross-coupled pair to accomplish conversion through positive feedback. Meanwhile, it utilizes complementary pull-up network (PUN) and pull-down network (PDN) to eliminate the leakage current of each branch. Thus, the DCVS based LSs have the potential to achieve ultra-low-power voltage conversion. Unfortunately, when the input voltage (IN) reduces below to the threshold voltage of pull-down transistors, the weak pull-down current is incompetent to withstand the strength of PUN, leading to the failure of conversion. Therefore, it is effortful to suppress the current contention to achieve a robust conversion from the sub-threshold to the supra-threshold level.

Several LSs have been proposed to get over the restrictions of traditional architectures. The LSs proposed in [12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23] employ CM-based structures. To minimize leakage power in standby mode, [12] cuts off the static current by a feedback PMOS. However, the feedback PMOS reduces output swing, which significantly increases the leakage power of output inverter when the output is high. In [13], a reduced swing output buffer is applied to lower static power, but the power re-
duction is still limited. This is because the compensating voltage is not sufficient to offset the voltage drop of internal nodes. The optimized DCVS based architectures are used in [24, 25, 26, 27, 28, 29, 30]. The topologies presented in [25] and [26] attempt to decrease the time of transitions through regulated-cross-coupled pair and self-adapting pull-up network, respectively. However, the non-negligible leakage power consumption of these LSs is still a large expense for battery-powered applications. The circuit presented in [27] applies a 2-stack output inverter to suppress short circuit current, but it brings in inverse effect on conversion speed. Despite the successful conversions of above LSs, it is still challenging to achieve both small propagation delay and low power consumption in the sub-threshold region. This paper proposes a DCVS-based LS with abilities of high-speed and low-power voltage level conversions. Benefit from the boost control circuit and MTCMOS technique, the propagation delay and static power are reduced to 18.07 ns and 64.2 pW, respectively.

This paper is organized as follows: the architecture of the proposed LS is shown in Section 2. Section 3 exhibits the simulation and comparisons results. In the end, Section 4 concludes this paper.

2. Proposed level shifter

To ensure a fast and robust conversion even in the sub-threshold range, it is urgent to suppress the severe current contention caused by unbalanced driven strength of the weak-inversion PDN and normal PUN. Thus, a new LS structure based on DCVS, as shown in Fig. 2, is presented in this paper. The proposed topology includes a novel boost control circuit (BCC) for PDN, which is composed of a MOS-capacitor (MP5/MP6), a diode-connected PMOS (MP7/MP8), and control transistors (MP9, MN3/MP10, MN4). The BCC boosts the input voltage to a higher level before the conversion phase and enhances the pull-down strength, which drastically speeds up the conversion and minimizes the low input voltage. For more details, the proposed BCC operates as follows.

When the initial input signal (IN) is at a low level (VSS), MP7 is activated, and the voltage of node NH1 is VDDL-Vt, where Vt is the voltage drop of MP7. Profit from the charging and discharging characteristic of capacitors, for a transient change of IN, the gate-drain voltage difference of the MOS capacitors (MP5) maintains at VDDL-Vt. When IN transits from “low” (VSS) to “high” (VDDL), MP7 is switched off, and the voltage difference of MP5 leads node NH1 to be boosted to a higher-level 2VDDL-Vt, which called pre-conversion voltage (PCV). It is noteworthy that, the parasitic capacitance at node NH1 results in a higher PCV. At the same time, the control transistors MP9 and MN3 are switched on and off, respectively. Then the raised input voltage can enter into the conversion stage through node QIN1 to turn on MN1. Conversely, for the node NH2 of BCC on the right branch, the voltage is 2VDDL-Vt when input signal changes from VDDL to VSS, otherwise it is VDDL-Vt. For the overall LS, the improvement of PCV accelerates the falling transition of node Q1, thereby, enables MP2 to turn on rapidly. Then MP2 pulls up the voltage of node Q2, and MP1 is switched off consequently. So far, positive feedback is triggered in a shorter time, efficiently expediting the completion of the conversion phase. As MP1 is switched off, node Q1 further discharges to VSS. Finally, the output inverter buffer charges the voltage of OUT to VDDH. Similarly, when the IN signal makes a falling transition, the swift discharge speed on node Q2 promotes node Q1 to charge to a high voltage earlier. Besides, two symmetrical input inverters drive the left and right branches of BCC separately to further optimize the delay. Fig. 3 analyzes the conversion speed of the BCC-based LS and the conventional DCVS structure at VDDL = 500 mV. It can be seen that the node Q1 of the traditional DCVS-LS discharges at an extremely slow rate. Due to the improvement of PCV (720 mV), the proposed LS shows a great advantage of conversion delay compared with the traditional scheme.

Fig. 4 indicates the comparison of the conversion range between the presented LS and traditional DCVS-LS. It can be observed that when the input voltage is lower than 500 mV, conventional DCVS-LS fails to implement the voltage conversion. That is because the competition between PUN and PDN significantly intensifies with the voltage difference.
between VDDL and VDDH increases. For the presented LS, diode-connected PMOSs (MP3, MP4) are utilized to limit the current flowing through PUN, which further extends the conversion range to the deep sub-threshold regime. The combination of PMOS diodes and the BCC technique not only limits the strength of PUN but also improves the strength of PDN. Therefore, as shown in Fig. 4, the allowable input signal of the proposed LS is minimized to 140 mV, resulting in a wide conversion range. In addition, the employment of current limiters introduces a new node Q3 with a voltage level higher than Q1. Accordingly, the output inverter is driven by split-input Q1 and Q3. When the voltage of IN is low, node Q3 can completely turn off MP13 to cut off the leakage current. Fig. 5 illustrates the transient waveform of the proposed LS at the low input voltage of 0.3V and the high output voltage of 1.2 V.

In order to significantly reduce the leakage power consumption, this proposed LS is further optimized through MTCMOS technology and sub-threshold device sizing. Since the VDDL domain is powered by an extremely low supply voltage, the leakage power consumption is mainly concentrated in the VDDH voltage domain, where the main conversion stage and an output inverter need to be considered. First, when the input voltage is low, the introduction of current limiter MP3 (MP4) causes a voltage difference between the node Q1 (Q2) and VDDH. Consequently, this condition increases the leakage current of MP2 (MP1). Different from [27], the current limiters in this paper are implemented with LVT transistors instead of HVT devices, thereby effectively eliminating the static current. Second, both the cross-coupled pair (MP1, MP2) and the output inverter adopt HVT transistors to reduce the static power when they are in standby mode. Third, the application of BCC greatly relaxes the size limitation of PDN, so it is possible to apply a small-size pull-down NMOS to save area overhead and power consumption. The minimum size of the transistor is 120 nm/60 nm (W/L) in 55nm-technology. Considering the short-channel-effect, transistors of PDN are implemented with 120-nm channel length to limit the leakage current of pull-down transistors. Meanwhile, using the reverse-short-channel effect, PMOS devices with an increased channel length of 120 nm are employed in the VDDL domain to optimize the delay. In addition, taking the sensitivity of the circuit to process variations led by minimum size into consideration, it is necessary to increase the size of transistors moderately to make a better trade-off between process sensitivity and area overhead. The optimal sizes of transistors are listed in Table I.

3. Simulation results and comparison

Fig. 6 describes the layout of the presented LS. It occupies an area of 16.35 μm² using SMIC 55 nm MTCMOS technology. The simulation conditions are set to 10 ns of input signal transition time and 0.1 pF of output capacitance.

To evaluate the impact of process-voltage-temperature (PVT) deviations, propagation delay simulations are performed across five PVT corners. Fig. 7 illustrates the delay of the presented LS relative to the value of VDDL, at the tt, ff, ss, fnsp, and snfp PVT corners. The typical case includes typical PMOS, typical NMOS, VDDH voltage of 1.2 V, and a temperature of 25°C. Meanwhile, fast NOMS, fast PMOS, 10% decline on VDDH (VDDH = 1.08 V), and a temperature of 125°C forms the best corner. This is because the employment of BCC balances the strength of PDN and PUN to a great extent, which in calculably relieves the contention, as discussed in section 2. Thus, fast NOMS and fast PMOS are utilized to speed up the conversion. Moreover, the shrank voltage difference between the low supply voltage (VDDL) and high supply voltage (VDDH) further improves the performance. Also, a higher temperature results in greater current for the sub-threshold transistors. As a result, the minimum delay occurs at the best corner, as shown in Fig. 7. Conversely, for the worst case, slow NOMS, slow PMOS, a 10% increase in VDDH (VDDH = 1.32 V), and a temperature of −40°C are used to further slowdown the conversion. It can be observed that the propagation delay increases exponentially when the voltage drops below 0.4 V, caused by

![Fig. 5](image1.png)

**Fig. 5** The transient waveform of the proposed LS.

| Transistor | W/L (nm) | Transistor | W/L (nm) |
|------------|----------|------------|----------|
| MP1-MP4    | 120/60   | MP11       | 700/120  |
| MP7-MP8    | 120/20   | MP12       | 200/120  |
| MP9-MP10   | 200/120  | MP13       | 280/60   |
| MN1-MN2    | 200/120  | MN6        | 500/60   |
| MN3-MN5    | 120/60   | MN7        | 200/60   |
| MP5-MP6    | 5000/60  |            |          |

![Fig. 6](image2.png)

**Fig. 6** Layout of the presented LS.

![Fig. 7](image3.png)

**Fig. 7** The propagation delay of the proposed LS at five PVT corners.
the sharply decreased driven current of the pull-down transistors in the sub-threshold region. This degradation is more severe at the worst corner. When VDDL reduces from 0.3 V to 0.2 V, the delay increases by 3.6x in the best case, and this factor raises to 62.5 in the worst case. The main reason for this phenomenon is that when working in a weak inversion region, the leakage current, as the domination of operating current, is significantly influenced by temperature. When VDDL = 300 mV, the worst-corner delay is 921 times higher than that at the best corner. Nonetheless, the proposed LS still achieves proper operations in all PVT cases.

For investigating the effect of device mismatches and global variations on the propagation delay of the proposed LS, Monte Carlo simulations of 1000 points are executed under the condition of low power supply voltage VDDL is 0.3 V. As illustrated in Fig. 8 (a), the average delay and standard deviation are 22.21 ns and 10.03 ns, respectively, which indicate slight sensitivity towards process variation. As mentioned earlier, increasing the size of transistors can improve this situation. Besides, to evaluate the minimum allowable input voltage of the proposed LS, several 500-point MC simulations are carried out at different VDDL voltages. The value of VDDL is swept from 0.1 V to 0.3 V in 0.01 V steps, and the environment is set to the worst PVT corner. The simulation results show that the presented LS can still operate properly when the VDDL voltage is as low as 0.14 V. Fig. 8 (b) exhibits the successful conversion waveform from 0.14 V to 1.2 V, which confirms that the lowest conversion voltage of the proposed LS is 0.14 V.

In order to corroborate the benefits of the presented LS in the sub-threshold region, it is compared with traditional DCVS structure assisted by current limiters (DCVSCL). For a fair comparison, the DCVSLS is accomplished with the same transistor size as the proposed design. Fig. 9 illustrates the comparison results of the propagation delay, static power dissipation, and energy per transition at the typical corner between the above two works. As shown in Fig. 9 (a), at VDDL = 0.3 V, the delays of the proposed LS and DCVSCL are 18.07 ns and 62.3 ns, respectively. Since the BCC effectively accelerates the discharging and charging speed of critical nodes, the proposed design exhibits a 3.4x-decrease of delay. As shown in Fig. 9 (b), the DCVSCL level shifter consumes a static power dissipation up to 2010.3 pW when the low supply voltage is 0.3 V. With the employment of MTCMOS and device sizing techniques, the presented LS reduces the voltage drop of internal nodes and the static current. Moreover, the split-driven output inverter further eliminates the effect of voltage drop. Although the BCC introduces a small amount of leakage current, for the voltage level conversion from 0.3 V to 1.2 V, total static power consumption is still as low as 62.4 pW. As shown in Fig. 9 (c), although BCC-LS consumes slightly high energy when VDDL is above 0.4 V, it is still comparable to the DCVSCL-LS. For the
conversion with a 0.3 V low supply voltage, the presented LS dissipates 87.35 fJ per transition, which is 5.28x less than the DCVSCL scheme.

Table II lists and compares the characteristics of the presented level shifter with a few advanced designs. Generally, since CM structure eliminates the contention between pull-down and pull-up network, the CM based LS obtains high conversion speed. The main disadvantage of this structure is the inevitable static current. For instance, although the LS in [13] shows a low propagation delay, the considerable static power consumption cannot be negligible, which also increases the energy per transition. Moreover, the LS described in [24] consumes less static power with an expense of circuit delay. In [31], a small delay is obtained with a large overhead and energy dissipation. For DCVS structures, deterioration of propagation delay caused by weak PDN is the main drawback. For example, the DCVS-LSs in [27, 30] show a relatively large delay, and the static power consumption is unsuitable for battery-less applications. The proposed design, benefiting from the MTCMOS and sub-threshold devices sizing techniques, achieves minimum static power of 62.4 pW among the listed LS. Meanwhile, with the employment of BCC, the propagation delay of this circuit is 18.07 ns, which is the smallest compared with other DCVS-LSs mentioned above, and far less than CM-LSs in [19, 24]. The energy per transition of the proposed LS is less than [13, 19]. Despite the introduction of the BCC, the area overhead is still comparable to previous designs and much smaller than [31]. Since the proposed LS achieves outstanding improvements in static power consumption and propagation delay, it is more suitable for ultra-low-power systems.

| Ref. | Tech. | Range (V) | Delay (ns) | Static (pW) | Energy/ 
|---|---|---|---|---|---|
| TCASI 12 [30] | 90 | 0.18-1.0 | 21.8 | 6400 | 74 (0.02V) | 36.5 | DCVS |
| TCASI 14 [19] | 65 | 0.2-1.2 | 162.0 | 4056 | 136 (0.07V) | 16.8 | CM |
| TCASE 15 [27] | 65 | 0.14-1.2 | 25.0 | 2500 | 30.7 (0.07V) | 17.6 | DCVS |
| TCASE 16 [31] | 65 | 0.2-1.0 | 12.9 | N.A. | 204 (0.02V) | 1931 | CM |
| VLSI 17 [24] | 40 | 0.2-1.2 | 66.38 | 88.4 | 72.31 (0.07V) | 11.92 | CM |
| VLSI 18 [13] | 65 | 0.1-1.2 | 7.5 | 2640 | 123.8 (0.03V) | 7.45 | CM |
| This work | 55 | 0.14-1.2 | 18.07 | 62.4 | 87.35 (0.02V) | 16.35 | DCVS |

4. Conclusions

This paper presents an ultra-low-power and fast voltage level shifter, which guarantees robust conversion in the sub-threshold region. Taking advantage of the boost control circuit (BCC), the proposed LS effectively addresses the contention issue existing in the sub-threshold regime. The BCC technique significantly expands the conversion range and accelerates the operating speed. Meanwhile, MTCMOS and sub-threshold device sizing technologies are employed to obtain extremely low static power consumption. Post-layout simulations performed in 55-nm technology indicate that the presented LS lowers the minimum input voltage to 140 mV and dramatically reduces the static power and propagation delay compared with prior level shifters. For the conversion from 0.3 V to 1.2 V, it achieves 18.07 ns propagation delay and 64.2 pW static power dissipation. Moreover, the energy dissipation is 87.35 fJ at the input frequency of 1 MHz.

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Table II Performance comparison with prior works.

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