Advanced TEM Characterization for the Development of 28-14nm nodes based on fully-depleted Silicon-on-Insulator Technology

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Abstract. The growing demand for wireless multimedia applications (smartphones, tablets, digital cameras) requires the development of devices combining both high speed performances and low power consumption. A recent technological breakthrough making a good compromise between these two antagonist conditions has been proposed: the 28-14nm CMOS transistor generations based on a fully-depleted Silicon-on-Insulator (FD-SOI) performed on a thin Si film of 5-6nm. In this paper, we propose to review the TEM characterization challenges that are essential for the development of extremely power-efficient System on Chip (SoC).

1. Introduction

The semiconductor industry has continuously been driven by the scaling down of transistor dimensions. Tomorrow’s nomad applications will require higher speed performances with lower power consumption compared to today’s devices. To fulfill these conditions, STMicroelectronics decided to develop the 28-14 nm technological nodes based on fully-depleted Silicon-on-Insulator (FD-SOI). Such a 28 FD-SOI chip, showing all metal levels till Al pads, is presented in the SEM cross-section from Figure 1. FD-SOI technology provides a unique value for extremely power-efficient chips compared to bulk MOS technologies. Actually, transistors run at higher frequencies (30%), are more power efficient (reduced leakage, thus preserved battery lifetime) and are much simpler for the manufacturing process compared to FinFETs [1]. A scanning TEM (STEM) Energy Dispersive X-ray (EDX) 3D reconstruction of a 28 FD-SOI transistor, presented in figure 1, shows the classical transistor parts (source, drain, gate, and channel) and the FD-SOI main process bricks (SiO₂ box and thin Si film). Advanced physical characterization is mandatory to develop FD-SOI technology, in particular to adjust critical process steps. For information purposes, in 2012, the average number of TEM analyses for 28-14 FD-SOI reached ~20 TEM studies per week with a response time of ~ 2.5 days. Specific issues are addressed through these analyses and will be detailed in this paper. Emphasis will be put on: the TEM sample preparation challenges using Focused Ion Beam (FIB), the need for quantified chemical characterization (STEM EDX) and strain/stress measurements by Nano Beam Electron Diffraction (NBED) or Dark Field Electron Holography (DFEH).
2. Characterization Challenges and limitations for 28-14nm FDSOI

2.1. Dedicated 28-14nm FD-SOI sample preparation

TEM lamellae of semiconductor devices are mainly prepared using a Focused Ion Beam (FIB) system, so as to ensure site specific process characterization. In this in-situ sample preparation method, a tab is extracted from the piece of wafer at target location. This tab is section milled to shape the lamella, from top layers to silicon substrate. For 28 FD-SOI devices, TEM lamellae have to be thinned down to typically less than 70nm, to not get overlapping structures, and even smaller for the smallest devices (e.g. SRAM cells). With the even smaller dimensions of the device, the top-down section approach appears not to be the most appropriate direction of observation; in-plane observation brings additional information about dimensions of the devices, while allowing relaxed TEM lamellae dimensions. If cross-sectional TEM observation is required, e.g. to control stacked layers of the process, reduced dimensions of the devices impose even thinner lamellae. This implies the use of low accelerating voltage for the FIB, to minimize the amorphous/damage layer; in case of the conventional top-down approach, this would lead to strong curtaining effects (coming from metal layers). Therefore, inversed sample prep is preferred for front-end device observation: the tab is flipped so that substrate is on top and metal layers at the bottom.

2.2. TEM/STEM morphological studies

In order to ensure a good scalability of SOI technology, the SiO$_2$ box and thin SiGe film thicknesses must be precisely monitored. Actually, for electrostatic control purpose, very low Si film thickness variations may be tolerated along the entire wafer. HR-TEM and STEM analysis have been performed in order to evaluate thin Si film roughness. These two imaging techniques are complementary since TEM enables high spatial resolution while STEM helps for Z-contrast imaging, as described in Figure 2.
2.3. **STEM EDX chemical characterization**

For all the FD-SOI elemental steps development, morphology and composition of the MOS transistors and structures had to be controlled at high resolution. The following TEM and STEM EDX analyses were carried out at 120 keV using Tecnai Osiris combining high brightness Field Emission Gun (FEG) and four EDX Silicon Drift Detectors (SDD). Figures 3, 4, 5 show analytical TEM analyses for the development of 28 and 14 nm FD-SOI technologies. Figure 3 shows STEM-EDX analysis of 28nm FD-SOI when source/drain epitaxy problems were encountered, leading to local defects. The initial interface showed silicon oxidation of a few nanometers, and finally this problem was solved by cleaning optimization.

![Figure 3. STEM ADF image and quantified STEM EDX profiles (Si, O) revealing an epitaxy issue during the raised source drain process of 28 nm FD-SOI technology](image)

Figure 4 shows TEM morphology and STEM-EDX dopant process control of nMOS 14nm FD-SOI. Arsenic doping from the gates is mapped and atom segregation can be measured at nanometer scale.

![Figure 4. TEM bright field (left) and STEM-EDX elemental map (right) showing the dopant distribution in gate (As) 14nm nMOS FD-SOI. See online version for colour code.](image)

Figure 5 shows the complexity of 14nm pMOS FD-SOI alloys integration for channel and source/drain. The channel's SiGe composition should be homogeneous and was targeted at a concentration of 15% Ge. The SiGe raised sources/drains, after Ni(Pt) silicidation are made of quaternary alloys (Si, Ge, Ni, Pt) which must be accurately controlled.

![Figure 5. STEM EDX maps showing pMOS FD-SOI final structure. See online version for colour code.](image)
2.4. *NBED & DFEH* strain characterization

Nowadays, the objectives regarding the performance cannot be achieved without strain engineering and therefore without strain characterization. Two techniques are mostly used in our laboratory: Nano Beam Electron Diffraction (NBED) and Dark Field Electron Holography (DFEH). The FD-SOI technology brings some specific challenges making a classic extension from bulk technology not always possible for strain techniques. The thickness of the film and its misorientation compared to the bulk Si are the two major constraints increasing considerably the complexity in the technique applications and results interpretation. For example, the tilt needed to bring relative good diffraction conditions in DFEH makes all interfaces blur (around 1-2nm). The reliability of the technique can be questioned on a 5nm thick film. For NBED, the probe size is equal to the thickness of the film, therefore very limited information can be extracted from those results. The NBED results taken along a SiGe film made by condensation are presented in figure 6(b). It is possible to see that the film is kept strained after the process in the middle of the area, and major relaxation is observed on its edge.

![Figure 6](image-url)  
**Figure 6** a) High Angle Annular Dark Field (HAADF) STEM picture of the SiGe film with corresponding NBED line profile (dashed). b) NBED relative deformation results from <220> & <004> directions along the SiGe film showing major relaxation at SiGe film edges. c) <004> and d) <220> dark-field holograms acquired in strained sSOI. e) DFEH relative deformation results showing a positive deformation in 220 direction and a negative deformation in 004 (results processed with HoloDark)

To overcome the issues cited above, some relaxed samples can be used to characterize the strain depending on the process steps. For example, the first steps of process use a thicker film (around 9-10nm) which enables more reliable strain characterization. Figures 6 c & 6d present DFEH results on a full wafer tensile strained SOI (sSOI) sample, which are clearly showing in Figure 6 (e) a positive deformation in the 220 direction and a negative one in the 004 direction (results obtained on a F20 TECNAI with Dual Lens configuration [2]). FD-SOI precise strain measurements show high challenges; however, a qualitative approach is an important source of information for process development in order to determine some configuration to keep the strain in the film or anticipate a loss of performance in some devices.

3. Conclusions

This paper demonstrates that advanced TEM characterizations are required and even unavoidable to ensure the development of new transistor generations such as FDSOI technologies. At first, the sample preparation is essential and FIB-based preparations have been optimized. Then, high resolution TEM and STEM are essential to precisely monitor each deposited layer. Finally, chemical analysis (EDX) coupled with strain measurements (NBED, DFEH) information are more and more routinely performed to get a deeper understanding of these materials physics.

References
[1] Skotnicki T et al. 2008 *IEEE Transactions on Electron Devices* **55**, 96-130
[2] Wang Y Y, Li J Domenicucci A and Bruley J 2013 *Ultramicroscopy* **124**, 117-129