Generic Cryo-CMOS Device Modeling and EDA-Compatible Platform for Reliable Cryogenic IC Design

Zawei Wang1,2,3#, Zhidong Tang1,2,3#, Yumeng Yuan1,2,3#, Ao Guo4, Xin Luo4, Renhe Chen1,2,3, Chengwei Cao4, Linlin Liu4, Zhenghang Zhi1,2,3, Weican Wu4, Yingjia Guo5, Yongqi Hu1,2,3, Liujiang Yu4, Ganbing Shang4, Jing Chen4, Jiashi Tang6, Shaqian Hu6, Shoumian Chen4, Yuhang Zhao6, and Xufeng Kou6

1ShanghaiTech University, Shanghai, China, 2Shanghai Institute of Microsystem and Information Technology, Shanghai, China, 3University of Chinese Academy of Sciences, Beijing, China, 4Shanghai IC Research and Development Center, Shanghai, China, 5Huali Microelectronics Corporation (HLMC), Shanghai, China, 6Tsinghua University, Beijing, China

*Email: kouxf@shanghaitech.edu.cn; hushaojian@icrd.com.cn Authors contributed equally to this work.

Abstract—The capability of data processing in quantum computers relies on the CMOS-based cryogenic control and storage systems. This paper outlines the establishment of the generic cryogenic CMOS database in which key electrical parameters and the transfer characteristics of MOSFETs are characterized as functions of device size, temperature/frequency responses, and variation/mismatch statistics. Thanks to the process design kit generated from the cryo-CMOS compact model, the cryogenic 4 kb SRAM and 5-bit flash ADC are designed, and their performance at low temperatures are readily evaluated and optimized on the EDA-compatible platform, hence laying a solid foundation for practical large-scale quantum computer design.

I. INTRODUCTION

Quantum computing has shown great advantages over classical binary computer in dealing with several intractable problems [1]. For most superconductor/silicon-based quantum computer prototypes developed at current stage, the generation of qubits is achieved at deep cryogenic temperatures (T < 1 K) while all the control instruments are externally placed at room temperature along with numerous long connection cables [2]. Considering that qubits are vulnerable to thermal noise and coherent time, such approach cannot be sustainable as the number of physical qubits scales up. Alternatively, it is proposed that scalable quantum computer can be realized in an improved architecture where the key functions of qubits manipulation, conversion, and error correction are implemented by cryo-CMOS integrated circuit modules adjacent to the quantum processor (Fig. 1a) [3]. Accordingly, the aforementioned proposal has led to recent progressive advancements of cryogenic electronics in which electrical properties of MOSFETs have been extensively investigated down to 20 mK [4] and some CMOS periphery circuitries have also been tested at low temperatures [5]-[7]. However, given that most EDA tools do not support simulations below 230 K due to the lack of cryo-CMOS compact model and process design kit (PDK) library, it is thus of great importance to establish a generic cryo-CMOS platform which paves the way for reliable cryogenic integrated circuit design.

In this work, following the standard CMOS modeling process flow (Fig. 1b), we present the temperature-dependent device compact modeling and develop an EDA-compatible cryo-CMOS process design kit library which facilitates highly-efficient design and analysis of large-scale integrated circuits suitable for full-fledged quantum computing applications.

II. CRYOGENIC DEVICE MODELING AND VALIDATION

A. Cryogenic CMOS DC Model and Validation

From our previous report [8], all nano-scale MOSFETs using HLMC 40nm low-power (40LP) technology would experience a substantial improvement on a reduced sub-threshold swing, enhanced channel mobility, and negligible leakage current when the base temperature gradually drops from 298 K to 10 K. Moreover, based on the temperature-driven gate geometry effects, we have proposed a modified Cryo-BSIM model to depict the transfer characteristics of transistors across the device size chart, as re-captured in Fig. 2.

In addition to individual device modeling, global variation due to device manufacturing process also plays a significant role in circuit design. Fig. 3 summarizes the variation statistics of threshold voltage (V_TH) and on-state current (I_D) collected from 50 test-dies. After assigning the mean values of V_TH and I_D as the reference during the device modeling process, we are able to evaluate the accuracy of our compact model. From the extracted relative root-mean-square (RMS) value of the I_D-V_GS data in Fig. 4, it is seen that the device-to-device variation increases in the low-temperature region, and such model error becomes more pronounced among short-channel devices. Nevertheless, we should point out that since RMS_{298K} < 3% is negligible at room temperature, the overall model deviation from experimental data still remains within ±10% at T = 10 K.

More importantly, in view of the critical impact of V_TH on circuit performance, its mismatch behavior is quantitatively examined. Fig. 5 displays the 3D mapping of the mismatch mean value (ΔV_{TH}) collected from 14 MOSFETs with different gate aspect ratios ranging from W/L = 0.12 μm/0.04 μm to 1 μm/1 μm. Given the consistency between V_{TH,10K} and V_{TH,298K}, we further plot the Pelgrom’s law which follows \( \sigma(\Delta V_{TH}) = A_{VTH}/\sqrt{W·L} \), where the slope A_{VTH} represents the threshold voltage factor depending on the fabrication process [9]. According to Fig. 6, it is found that the values of A_{VTH} increases by 2× for L = 1μm and 1.5× for L = 0.04 μm devices when the transistors are cooled down from 298 K to 10 K. Consequently, by incorporating both the \( \sigma(\Delta V_{TH}) \) mismatch model and the global variation behavior (i.e., it follows normal distribution with FWHM affected by the effective channel geometry, as illustrated in Fig. 7) into the modified BSIM model.
model, the validated PDK library can effectively cover the [10 K, 298 K] region. In the meantime, the statistical study also provides a trustworthy direction to mitigate the influence of variation and mismatch effects by adopting appropriate device size engineering during the cryogenic circuit and system design.

B. Cryogenic CMOS RF Characterization and Modeling

In order to elaborate the RF properties of cryo-CMOS devices, we carry out standard S-parameters characterization process on 36 multi-finger gate NMOS and PMOS devices from the HLMC-40LP RF test wafer for device modeling. After careful calibration and de-embedding, Fig. 8a shows the S-parameters polar plots of one NMOS transistor under different DC bias at \( T = 10 \text{ K} \) and 298 K, respectively. In this diagram, the shift of \( S_{21} \) along the \( \pi \)-axis reflects the enhancement of DC trans-conductance \( (g_{m}) \) at lower temperatures, consistent with Fig. 2. On the other hand, as the applied frequency increases from 250 MHz to 40 GHz, the \( S_{21} \) curve propagates clockwise, and the evolution of its corresponding amplitude and phase is determined by the parasitic resistances \( (R_g, R_d) \) and extrinsic capacitances \( (C_{gs}, C_{gb}, C_{gd}) \) associated with the transistor (i.e., as a shown, the passive inductor does not exhibit any temperature dependence as shown in Fig. 8b). Subsequently, we utilize the Cold-FET method [10] to obtain the aforementioned RF parameters based on the \( (V_{GS} = 1.1 \text{ V}, \ V_{GS} = 0 \text{ V}) \) S-parameters data, and reveal distinctive temperature-dependent features from the \( R \) and \( C \) spectra. Specifically, the degenerately-doped drain region gives rise to the metallic-like resistance, namely \( R_d \) becomes smaller with decreased temperature (Fig. 9a); in contrast, the relatively constant \( C_{bg} \) manifests its MOSCAP nature (Fig. 9b).

Finally, with the completion of RF measurements on all transistors from 10 K to 298 K, a generic cryogenic RF compact model based on the HSPICE framework has been developed. In particular, by applying polynomial expressions with only one set of fitting parameters, the equivalent parasitic resistances of transistors with varied gate/channel configurations are calibrated, and our cryo-RF model can accurately match the measured \( Y \)-parameters across the whole frequency domain at \( T = 10 \text{ K} \) (Fig. 10). Additionally, such RF device modeling is further justified by tracing the cut-off frequency \( (f_T) \) of MOSFETs, as emphasized in Fig. 11. Here, the fitted \( f_T \sim T \) data points, which are either obtained from the \( H \)-parameters of our cryo-RF compact model or deduced from the \( f_T \propto g_m/(C_{gs} + C_{gd}) \) equation, match the measurement result quite well, hence addressing the universality of the proposed RF compact model.

Next, we illustrate the design of qubit control blocks (Fig. 13a) with the help of the comprehensive cryogenic PDK library. For instance, considering the strength between NMOS and PMOS transistors would change with temperature due to mobility mismatch, we re-adjust the PMOS-to-NMOS gate-size ratio of the 6T SRAM bit-cell to optimize its drive capacity and static noise tolerance. Meanwhile, the peripheral circuitries (Fig. 13b) are also modified to ensure their correct functions down to 10 K. Fig. 13c shows the post-layout simulation results of the cryogenic 4 kb SRAM designed as the storage module of quantum computer. From these data, we can not only acquire the write/read dynamics and power dissipation of the SRAM array in reference to supply voltage and temperature, but also take full advantage of EDA tool to facilitate the optimization process. As a result, the final taped-out 4 kb SRAM circuit indeed exhibits better performance in terms of speed and power consumption at low temperatures, and its quiescent supply current \( (\text{IDDQ}) \) benchmark is in good agreement with our model estimation (Fig. 13d).

Such EDA-assisted strategy is more effective for the cryogenic 500MSa/s 5-bit flash ADC design. Since the threshold voltage would inevitably increase by ~0.2 V at 10 K [12], the Strong ARM-structure of the dynamic comparator module in conventional RT-ADC design fails to follow the bit switch when the bias level of the input differential pair is below 0.5 V with insufficient pull-down current. To address such challenge, we re-design the dynamic comparator unit by introducing an additional pre-amplifier stage to enlarge the common-mode voltage range and boost the input voltage swing under the guidance of the cryogenic PDK library, and the resulting cryo-ADC circuit can operate in the rail-to-rail mode in the whole [10 K, 298 K] region, as highlighted by the real-time waveforms in Fig. 13f.

IV. CONCLUSIONS

We validate both the DC and RF characteristics of NMOS/PMOS devices with varied gate geometries from sufficient golden die measurement data, and manage to extend the PDK library into the sub-10 K region. Furthermore, we demonstrate the use of such platform to design and optimize high-performance cryogenic SRAM and ADC circuits.

ACKNOWLEDGMENTS

This work is supported by the Strategic Priority Research Program of CAS (XDA18010000) and the NSFC Program (61874172), and the Shanghai Rising-Star Program.

REFERENCES

[1] E. Charbon et al., IEDM, pp. 13.5.1-13.5.4, 2016.
[2] Panu et al., Nature Electronics 4, 64–70, 2021.
[3] B. Patra et al., JSSC, vol. 53, no. 1, pp. 309-321, 2018.
[4] Xue, X. et al., Nature 593, 205–210, 2021.
[5] Y. Peng et al., JSSC, vol. 56, no. 7, pp. 2040-2053, 2021.
[6] G. Kiene et al., JSSC, vol. 53, no. 7, pp. 1433–1439, 1988.
[7] B. Prabowo et al., IEDM, pp. 13.5.1-13.5.4, 2016.
[8] Z. Wang et al., EDL, vol. 41, no. 5, pp. 661-664, 2020.
[9] M. J. M. Pelgrom et al., JSSC, vol. 24, no. 5, pp. 1433–1439, 1989.
[10] K. Dambir et al., IEEE Transactions on Microwave Theory and Techniques, vol. 36, no. 7, pp. 1151-1159, 1988.
[11] Z. Wang et al., IEDS, vol. 36, no. 7, pp. 2040-2053, 2021.
[12] C. Enz et al., IEDM, 2020, pp. 25.3.1-25.3.4.
**PMOS**

\[ W = 0.12 \mu m \]

\[ L = 0.04 \mu m \]

**300 K**

\[ 10 K \]

\[ 10^{-5} \]

\[ 10^{-7} \]

\[ 10^{-9} \]

\[ 10^{-11} \]

**HL 40LP Core Devices**

**V\_DS = 0.05V**

**RT-BSIM Model**

**Cryo-BSIM Model**

**Exp.**

**V\_GS (V)**

**I\_D (A)**

**Fig. 2.** Temperature-dependent \( I\_D - V\_GS \) transfer characteristics of MOSFETs and cryo-BSIM compact model validation.

**Fig. 3.** Variation statistics of (a) \( \Delta V\text{\_TH} = V\text{\_TH,10K} - V\text{\_TH,298K} \) and (b) relative \( I\_D,10K/I\_D,298K \) with NMOS and PMOS transistors of four corner sizes. The Error bars indicate the variation range of the experiment data collected from 50 test-dies, while the solid dots represent the mean values of parameters used in the cryo-CMOS model.

**Fig. 4.** Relative RMS deviation of the \( I\_D - V\_GS \) transfer characteristics between the cryo-CMOS compact model and the experiment data.

**Fig. 5.** 3D mapping of the mismatch mean value counted from 14 MOSFETs with varied gate aspect ratios.

**Fig. 6.** Pelgrom’s plot of \( \sigma(\Delta V\text{\_TH}) \) fits well with the experiment data at both \( T = 298K \) and 10K.

**Fig. 7.** Probability density function (PDF) of \( V\text{\_TH} \) of devices with four different gate geometries at \( T = 298K \) and 10K.
Fig. 8. Experimental $S_21$ characteristics of (a) RF NMOS transistor ($W/L = 1 \mu m$, $L=0.04 \mu m$, and $N=32$) and (b) passive inductor measured at 298K and 10K, respectively. The measured frequency varies from 250 MHz to 40 GHz with the step of 100 MHz.

Fig. 9. Temperature-dependence of (a) $R_s$ and (b) $C_{gg}$ extracted from the $S_{21}$ result of the RF NMOS transistor used in Fig. 8. All data remain almost constant in the entire frequency domain.

Fig. 10. Cryo-RF model verification of (a) real part and (b) imaginary part of the $Y_{21}$ parameter at $T = 10K$ under two bias conditions ($V_{DS} = 1.1 V$, $V_{GS} = 0.275 V$) and ($V_{DS} = 1.1 V$). The measured frequency ranges from 250 MHz to 40 GHz with the step of 100 MHz.

Fig. 11. Cut-off frequency $f_T$ and its fitting curves at 298K, 77K and 10K, respectively.

Fig. 12. Verification of the cryo-CMOS platform on evaluating the 1501-stage RO at different temperatures. Inset: 1501-stage RO circuit diagram.