Abstract: Hybrid DC breakers (HCBs) are crucial components in modern DC systems. Integrated gate-commutated thyristors (IGCTs) are widely used in high-voltage HCBs due to their controllable turn-off capabilities under high-power conditions. The focus of this study is on the optimisation of gate-commutated thyristors (GCTs) for HCB applications, including operation temperature and design parameters. The considerations of GCT design and operating conditions for the use in HCBs are discussed. Under those considerations, a 2D finite element model of GCT is developed to investigate the influence of the GCT design parameters on the maximum controllable current (MCC) and the safe operation area (SOA). Impedance unevenly distributed along the full wafer has been calculated to obtain accurate simulation results. Results show that the P⁺-base, lifetime, and the distance between cathode and gate metallisation can all affect the MCC. In addition, GCTs can provide a higher MCC by operating at a higher temperature.

1 Introduction
In recent years, the rapid development of power electronic technologies based on power semiconductor devices has led to increasing applications in DC systems at both power transmission and distribution levels. The technical and economic benefits of a DC system make it a competitive alternative to an AC system [1, 2], such as the DC-based applications in the marine and traction system [3].

The high-power DC breaker is a crucial component in DC systems. In general, based on power semiconductor devices, there are two types of DC circuit breakers: solid-state circuit breaker (SSCB) and hybrid circuit breaker (HCB) [4, 5]. The use of IGCTs enables fast, arc-less, reliable and maintenance-free switching for high-power HCBs [5]. The IGCT presents advantageous features including (i) larger SOA, (ii) lower on-state loss, (iii) higher thermal capacity and better cooling due to the wafer design, and (iv) higher surge current capacity [5, 6]. In addition, 6-inch diameter GCTs with rated currents up to 8 kA or above can be fabricated. Using IGCTs and other Gate Turn Off thyristors (GTO)-type devices in high-power HCBs has attracted many attentions from both the academia and industry. Some recent applications are summarised in Table 1. Compared to the conventional design of power converters in which reducing losses and cooling arrangement are challenging, the power semiconductor devices in HCBs operate on a non-repetitive basis. The main design constraints of HCBs are power current handling capacity and blocking voltage of power electronics devices. For better use of IGCTs in HCBs, optimisation of GCTs is required.

In this paper, the GCT with a diameter of 91 mm and a voltage class of 6.5 kV is chosen to be optimised. The principle of GCT design and destruction is first summarised in the context of increasing current capacity and blocking voltage. Considering the HCB operation and destruction mechanism of IGCT, the factors determining the maximum control current (MCC) of GCTs are presented. Unevenly distributed impedance along the full wafer is calculated and a 2D finite element model of a GCT structure is developed in Silvaco ATLAS. This model is used to understand the relationship between the structural parameters, junction temperature and the dynamic performance of the GCT in the context of its MCC. A GCT structure with enhanced MCC is also presented. Both simulation and experimental results have shown that the MCC purpose-oriented design and optimisation of GCTs will improve the performance of HCBs.

2 Considerations for parameter optimisation
2.1 Main destruction mechanism of GCTs
The IGCT integrates the GCT chip with its gate drive unit to improve the switching performance. Fig. 1a shows a diagram of a typical 4-inch GCT chip. The entire GCT wafer consists of more than 2200 GCT cathode fingers arrayed in ten concentric rings and surrounded by gate metallisation. The area between Ring 5 and Ring 6 form the annular gate conduct terminal of the GCT [11]. Each of these fingers represents one GCT cell.

The vertical cross-section of a typical GCT cell is shown in Fig. 1b. Three P-N junctions are marked with J1–J3. During turn-on, holes and electrons are injected into the N-base and P-base regions. The distribution of electron concentration in on-state is shown in the red line in Fig. 1c. During turn-off, GCTs perform differently from GTOs. One of the advantageous features of IGCTs
over the original GTOs is their rapid current commutation at turn-off, which is capable of commutating the load current to the gate terminal within 2 μs prior to the blocking voltage is established. This is known as the hard-drive requirement, which is shown as the turn-off current path in Fig. 1b [11, 12]. The hard-drive requirement needs to be achieved in the normal operation and it significantly affects the SOA of IGCTs.

Another factor that affects the SOA is the dynamic avalanche current. Under inductive load conditions, the anode current cannot decrease until the blocking voltage reaches the operating DC voltage ($V_{DC}$). During turn-off, holes are swept through the depletion region by the electric field. When holes current density and the blocking voltage are sufficiently high, the resulting electric field near the reverse-biased junction can produce an avalanche current due to the impact ionisation effect. This avalanche current as the base current in the P and P$^+$ base regions can retrigger the GCT cell [13]. Thus, the holes current density and blocking voltage need to be regulated to avoid generating avalanche current.

### 2.2 Parameter for optimisation

The MCC function-oriented optimisation here is to modify conventional IGCTs for the specific use in HCBs. Parameters that need to be optimised come from the characteristics of HCB operations. Fig. 2a shows the typical topology of HCBs using IGCTs. The currents of system, mechanical switch, IGCTs branch and arrester branch are indicated by $I_0$, $I_1$, $I_2$ and $I_3$, respectively. Fig. 2b shows the current commutation progress in the HCB's operation against a typical DC fault. During the normal state, the current $I_1$ flows through the fast mechanical switch and the IGCTs are in the OFF state. When a DC fault occurs, the IGCTs are turned on, and the load current $I_1$ starts commutating to the IGCT branch where the current is indicated as $I_2$. During $T_2$, the IGCT branch remains in the ON state to avoid upcoming voltage against the mechanical switch operation during this interval. Once the mechanical switch completes its operation, the IGCT branch turns off to start commutating $I_3$ to the arresters where the current is indicated as $I_3$ during the interval of $T_3$. The HCB voltage $U_{MS}$ will rise rapidly as the arresters absorb the fault current from the IGCTs.

As indicated by [7–9], in normal HCB operation, the operation time of the mechanical switch $T_2$ can be up to hundreds of milliseconds. In this period, the IGCTs remain in the ON state, and the thermal loss during this interval will heat up the IGCT devices before their following turn off. The rise of GCT junction temperature is estimated by using the $U$–$I$ curve and the thermal resistance in 5SHY42L6500 IGCT’s datasheet [14], as shown in Fig. 2c.

As shown in Fig. 2c, in HCBs’ normal operation, the junction temperature (Temp) rise is significant before the IGCTs’ turn-off. The external cooling is not effective to cool down the junction temperature of devices due to significantly larger cooling time constant compared to the temperature rising time. In addition, the junction temperature significantly affects the carrier mobility and impact ionisation in GCT, leading to different switching
characteristics. Thus, the consideration of junction temperature is essential to optimise the IGCT for better performance of HCB.

The structural parameters should also be considered to gain higher MCC of GCTs. The thickness of the P⁺-base ($T_{P⁺}$) affects the quantity of the excess carriers injected into the P⁺-base region. In addition, the P⁺-base provides a low resistance path for the load current and the dynamic avalanche current which is related to the retriggering of the GCT during turn-off.

The third parameter to consider is the distance, $D_{G}$, between the gate metallisation and the edge of the cathode, as in Fig. 1a. $D_{G}$ determines the length of current path when the load current is commutated to the gate.

Another parameter to consider is the minority carrier lifetime of eletrons, $\tau_{e}$. The carrier lifetime affects the recombination rate of the excess carriers [15, 16]. The carrier recombination rate affects the carrier diffusion and, therefore, affects the quantity of the excess carriers in the base region.

The fifth parameter to consider is the peak doping concentration of the N-buffer region ($N_{NB}$). A higher $N_{NB}$ leads to a lower injection efficiency ($\gamma$) of J1 and a higher recombination rate of the excess carriers in the N-buffer.

### 3 Model and methodology

#### 3.1 Modelling for GCT

The simulation of the influence of the five parameters discussed in Section 2 on the MCC and blocking voltage of GCT requires a precise whole wafer model. Due to the uneven distribution of parasitic impedance along the current path between different GCT cells and the gate unit, significant current redistribution exists during the turn-off [11]. Such parasitic inductive and resistive impedance is lower in value for the GCT cells that are closer to the gate contact [17, 18]. SPICE components are therefore required to simulate the uneven impedance distribution of gate metallisation along the gate current path on the wafer.

Previous work has proved that the modelling method shown in Fig. 3a combines the numerical model and the SPICE components for the simulation of the current redistribution phenomena [19, 20]. The GCT cell models in Fig. 3a are two-dimensional numerical models, representing each ring of the GCT shown in Fig. 1a. Every GCT cell model has been given the equivalent active area of the specific ring in the GCT it represents. Z1–Z10 represents the parasitic impedance of gate metallisation distributed along the GCT wafer. Other SPICE components represent the test circuit [11]. $L_{load}$ in the test circuit is adjusted to get a current rise rate of 1 kA/ms according to the HCBs’ operation [7–9].

Previous research has presented the results of extracting the impedance, Z1–Z10, using the simulation tool FastHenry [11, 21]; however, the detailed simulation method and process have not been revealed. In fact, the methods in [11, 21] cannot be directly applied to the optimisation here. This is because the actual impedance is closely correlated to the dimension of the gate metallisation and the package design of the IGCT, and these important correlations require further investigation to ensure more convincing results. In the optimisation here, the parasitic impedances distribution is recalculated by using the Ansoft tool from Ansys.

Figs. 3b and c show the cross-section of a GCT package and the current path at turn-off. The current commutation from cathode to gate flows along a loop formed by gate metallisation, gate contact, gate plate, gate unit, cathode metal plate and cathode metal block. The GCT cells of each ring have different current commutation loops due to different distances from gate contact. Figs. 3b and c show the current commutation loops of the GCT cells of the first ring and the tenth ring, respectively.

The material set is based on an actual IGCT device, as shown in Table 2. To simplify the calculation, following assumptions and modifications have been made:

i. The influence of the gate-driven circuit on the magnetic field is neglected in the calculation of the impedance distribution of the GCT cathode rings.
ii. Due to the latch-up of GCT and the resulting high carrier concentration during on-state, and the high doping concentration in the P⁺-base region, the current path in silicon during the rapid turn-off current commutation has low resistance and can be replaced by aluminium without incurring a significant error.

The equivalent impedances extracted from simulation, $Z_{1}–Z_{10}$, are summarised in Table 3. $Z_{1}–Z_{10}$ ideally should be represented using transfer functions for its frequency-domain characteristics. However, there is no simple way to use transfer functions in Silvaco Atlas. So an approximation is made here. The current commutation interval, $t_{c}$, is correlated to the current rise time in the commutation loop, and $t_{c}$ is considered as one-quarter of one sinusoid cycle. The equivalent frequency, therefore, is $f = 1/(4\pi t_{c})$. When IGCT turns off at a load current above 3500 A, $t_{c}$ is in the range of 0.4–0.6 µs, which corresponds to $f$ of 416–625 kHz. The inductances and resistances do not shift much in the range of 416–625 kHz. Therefore the average impedance values in the range of 416–625 kHz are used, with a step interval of 1 kHz.

The simulated inductance values of GCT rings are compared to previous studies reported in [11] (Fig. 3d). However, the values in Fig. 3d are different from Table 3. This is because Fig. 3d presents the actual inductances of the current commutation loops. For example, the inductance of the tenth ring is equal to the sum of inductances from $Z_{10}$ to $Z_{6}$.

The gate contact of the GCT wafer is located between the fifth ring and the sixth ring. Here, the first to the fifth ring are referred to as the inner rings, and the sixth to the tenth ring are referred to as the outer rings. In Fig. 3d, the inner rings have longer current commutating loops than the outer rings. This is due to the current from the inner rings flowing through the inner molybdenum plate, indicating that the current commutating loop is longer. This is demonstrated as the ‘step’ between the fifth and the sixth ring, marked by the square marker in Fig. 3d. However, the inductance values of the fifth and the sixth ring were reported to be equal in previous studies.

Another difference is the change rate of the inductance against the distance from the gate contact. This change rate of the recalculated inductance values of the outer rings is larger than that of the inner ones. The current loops of the inner rings are longer and a small change in the distance of inner rings will result in a relatively small change in the current loop. However, former values shown by the dot marker in Fig. 3d do not reflect such an obvious pattern.

#### 3.2 Simulation procedure

The DC voltage ($V_{DC}$) is set to be 2800 V and the temperature is set to be 300 K. The device is set to turn off at a specific current in the circuit as shown in Fig. 3a. The DC link voltage of 2.8 kV, other than 4 kV, is applied in simulation. This is because when we apply IGCTs in the HCB, extra IGCTs are always used in series for the reliability. For example, four IGCTs of 6.5 kV connected in series can be applied in the HCB of 10 kV with an overvoltage of 20 kV. The DC voltage applied to each of IGCT is 2.5 kV only. So, we apply IGCTs in the HCB of 10 kV with an overvoltage of 20 kV.

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At turn-on, parameters such as emitter efficiency ($\gamma$) and transport coefficient ($\alpha_{T}$) are analysed.

A successful turn-off is marked by the anode current being reduced to a low level after the anode voltage reaches the DC voltage, without any retriggering.

A failure turn-off is indicated by any of the following situations:

i. Hard-drive requirement for a GCT cell is not fulfilled.
ii. Any GCT cell conducts >30% of the on-state load current.
iii. Any GCT cell is retriggered.
Fig. 4 shows the doping profile and the electron distribution of the reference GCT cell with a rated voltage of 6.5 kV in simulation at 4 kA on-state load current.

Using the model in Section 3, simulation results of successful and failed turn-off are shown in Figs. 4b and c. Although the current commutation of the inner rings is slower due to higher commutation loop inductance, the current commutation of the outer rings finishes later due to higher current share. The outer GCT rings, such as the tenth ring, have a higher share of the total device current. This makes it more difficult for the outer GCT rings to fulfil the hard-drive requirement. As explained in Section 2, if the hard-drive requirement is not fulfilled, the tenth GCT ring will not deplete and the current will continue to flow to the middle of the cathodes, as current distribution shown in Fig. 4d.

The simulation results of GCT parameters against MCC are compared with the reference GCT parameters. The collective simulation results of MCC against on-state voltage drop are as shown in Fig. 5.

4.1 Operating temperature (Temp)

It has been found in the simulation that the MCC is increased at higher temperatures as shown in Fig. 5. Here, the GCT hard-drive is simulated at the operating temperature of 300, 320, 360 and 400 K. As shown in Fig. 6a, when temperature becomes higher, the delay for J2 to support the voltage is significantly increased, allowing increasing time for GCT to fulfil the hard-drive requirement. Thus, the MCC can be improved by increased junction temperature.

The effect of temperature on MCC has been verified by experiments. Fig. 3a shows the layout of the experimental circuit. The $V_{DC}$ was set to be 2.8 kV, and the load current was set to be

| Part                  | Material         | Relative permeability | Bulk conductivity (Siemens/m) |
|-----------------------|------------------|-----------------------|------------------------------|
| gate metallisation    | aluminium        | 1.000021              | $3.8 \times 10^7$            |
| (10 μm thick)         |                  |                       |                              |
| molybdenum plate      | molybdenum       | 1                     | $1.76 \times 10^7$           |
| others                | copper           | 0.999991              | $5.8 \times 10^7$           |
3.8 kA. A heating clamp set to be different Temp was used to heat the GCT as shown in Fig. 6b. Using the heating clamp, the GCT was heated for 1 h to ensure that the GCT’s junction temperature is the same to the heating clamp.

A Pearson coil and a differential probe were used to measure the anode current and voltage, respectively. As the GCT chip is in the press packaging, there is no simple way to directly measure the current commutation process. However, when the current commutates through the gate drive, there is a measurable voltage drop through the stray inductance of gate drive. The voltage drop of gate drive can indicate the current commutation, as shown in Fig. 6c.

The anode current and anode voltage waveforms of the IGCT turn-off at Temp = 300, 320, 360 and 400 K are presented in Fig. 6c. The current commutation interval is depicted using the step drops in the gate voltage waveform. In Fig. 6c, the time of anode voltage rising has been delayed by ~0.25 μs as Temp increased from 300 to 400 K, validating that the simulation prediction and extended delay allows GCT to fulfil hard-drive requirements. In addition, at higher Temp, overvoltage was also reduced due to enlarged damping resistance and diminished dv/dt.

Hence, the experiment results agree with the simulation results. At higher Temp, it is easier for GCT to fulfil the hard-drive requirement. At higher Temp, the GCT can obtain a higher MCC.

4.2 P⁺-base thickness (Thp⁺)

Previous studies have shown that Thp⁺ is a highly effective parameter to alter MCC [19]. However, as shown in Fig. 5, if the P⁺-base becomes too thick, the MCC will be reduced, assuming the same peak doping concentration and its roll-off function. For example, at the Thp⁺ of 50 μm, the MCC is reduced to 3.7 kA.

To explain the reduction of MCC, electron distribution in the base region of GCT at the current of 4 kA is plotted in Fig. 7. As Thp⁺ increases from 35 to 50 μm, the excess carriers in the base region near the N⁺-emitter are reduced by nearly 50%, as shown in Fig. 7a. This significant reduction of excess carriers in the P⁺-base and B-region strongly affects the turn-off behaviour of GCT cell. Further explanation can be made using 2D plots of GCT vertical cross-section (Figs. 8a and b). During the turn-off current commutation to gate, excess holes and electrons flow to the N⁺-emitter and the gate, respectively (Fig. 8a). A depletion region begins to form where the excess carriers exhaust, indicated by the electric field in the depletion region at J3 and J2 in Fig. 8b. However, as shown in Fig. 8b, excess carriers at J2 begin to exhaust before the depletion region of J3 expands to the centre of the N⁺-emitter. This indicates that the hard-drive requirement has not been fulfilled. This is because the 50 μm Thp⁺ leads to a significant reduction in the excess carriers at both J2 and J3. Fewer excess carriers at J2 causes J2 to be depleted so rapidly before the cathode emitter became fully reverse biased. In this case, it is more difficult to fulfill the hard-drive requirement at the same current level.

![Fig. 4 Doping profile and electron distribution in the GCT cell of 6.5 kV; successful and failure turn-off waveforms](image)

In the simulation, the optimum Thp⁺ is found to be ~45 μm to reach maximum MCC, although the on-state voltage drop is also affected.

4.3 Distance between cathode to gate metallisation (Dg)

Another parameter to be considered is the distance between cathode and gate metallisation, Dg. The commutating current will concentrate between the edges of the N⁺-emitter and the gate metallisation due to the high doping concentration in the P⁺-base. Using the model developed in this paper, the MCC is simulated for Dg of 15, 35, 55, 85 and 93 μm. The width of half of a GCT cell,

| GCT | Impedance | Active area, % |
|-----|-----------|----------------|
|     | R, mΩ    | L, nH          |
| 1   | 0.3259    | 0.2321         | 2              |
| 2   | 0.2495    | 0.198          | 4              |
| 3   | 0.2159    | 0.1495         | 6              |
| 4   | 0.1994    | 0.0986         | 7              |
| 5   | 0.0549    | 0.5697         | 9              |
| 6   | 0.0417    | 0.191          | 11             |
| 7   | 0.1341    | 0.4362         | 13             |
| 8   | 0.1049    | 0.0411         | 14             |
| 9   | 0.0881    | 0.0343         | 16             |
| 10  | 0.0733    | 0.04           | 17             |
| GU  | 1.3       | 2.1            |                |

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Dw, remains the same, and the width of gate metallisation is altered. Intuitively, a narrower Dg assists the current commutation from the N+-emitter to gate metallisation. However, the MCC is reduced when Dg becomes too small. The MCC values against different Dg are shown in Fig. 5.

The reduction of MCC can also be explained using the hard-drive requirement. When the Dg is reduced to 35 μm, as in Figs. 8c and d, it becomes easier to sweep out the excess carriers in the P+-base because of the shorter current path. However, the excess carriers around J2 exhaust faster and start to support voltage before the N+-emitter is fully reverse biased. Consequently, the hard-drive requirement is not fulfilled. In the simulations here, the optimum Dg for maximum MCC is found to be ∼85 μm.

4.4 Carrier lifetime control (τn0, τp0)

Carrier lifetime control is an effective method to alter the recombination rate of the excess carriers. However, the MCC of GCT with different minority carrier lifetimes can also be reduced as shown in Fig. 5. By controlling the carrier lifetime, different on-state and turn-off characteristics are produced. The reference GCT has the minority carrier lifetime of τn0 = 10 μs for electrons and τp0 = 2.5 μs for holes.

Lifetimes of carriers strongly affect the excess carrier distribution during on-state, as shown in Fig. 7b. From Fig. 7c, the time duration of load current commutation is significantly reduced. This is because a shorter lifetime not only reduces the excess carriers in the base region but also increases the recombination rate of the excess carriers. Therefore if the lifetime reduces too significantly, excess carriers at J2 will exhaust rapidly so it becomes more difficult to fulfil the hard-drive requirement. Thus, simulations have shown that the lifetime control has a contrary effect on the MCC. An optimum set of minority carrier lifetimes is found to be τn0 = 8 μs, τp0 = 2 μs.

4.5 N-buffer peak doping concentration (NNB)

The N-buffer in GCT mitigates the injection of holes from the P+-emitter into the N-base region. An increased doping concentration in the N-buffer region reduces the injection efficiency (γJ1) of the P–N–P structure in GCT, as shown in Fig. 7d. When the current is above 3 kA, γJ1 of different N-buffer tends to converge. This is because when the load current increases, the injection level in the N-buffer region becomes higher and reaches high-level injection, so the effect of the N-buffer to reduce γJ1 is weakened.

During turn-off, impact ionisation occurs in the depletion region when the electrical field becomes sufficiently high. Impact ionisation produces electron and hole pairs, of which the electrons induce the injection of holes from the P+-emitter. With a heavily doped N-buffer layer, this induced injection of holes is mitigated, resulting in the minimum current density so the dynamic avalanche at turn-off can be avoided. Thus, the heavily doped N-buffer layer is especially assistive to the outer GCT rings where current tends to concentrate during turn-off.

The maximum VDC to turn off the same 3.8 kA current is increased from 2.8 to 4.5 kV as a result of the increase of NNB from 9 × 1015 to 5 × 1016 cm−3. However, the on-state voltage is increased by >30% due to the resulting lower injection efficiency of the P–N–P structure in GCT.
5 Discussion and conclusion

The focus of this paper is to optimise the parameters of GCT including Temp and structural parameters to enhance the MCC and SOA of GCTs for its application in HCBs. To achieve these objectives, a combined model including a two-dimensional numerical model of GCT cells with SPICE components has been developed for simulation. The impedance of the gate unit and gate metallisation along the GCT wafer has been precisely calculated and verified. Using this model, the MCC of GCT was simulated, and the physical process inside the GCT wafer during on-state and turn-off is analysed.

Unlike insulator gate bipolar translators (IGBTs), it has been found that IGCTs can provide a higher MCC at higher device junction temperatures in both simulations and experiments.

Fig. 7 Simulation results of GCT with different $T_{thp+}$, lifetime ($\tau_{n0}, \tau_{p0}$) and $N_{NB}$

(a) Electron distribution of GCT with different P$^+$-base thicknesses (4 kA), (b) Electron distribution of GCT with different lifetime, (c) Left shifting of voltage rising time in the tenth GCT cell model when turning off, (d) $\gamma_{J1}$ of GCT cell with different $N_{NB}$

Fig. 8 Physical characteristics in GCT cell with different parameters

(a) Holes current and electrons current distribution in the tenth GCT cell model with 50 $\mu$m $T_{thp+}$ at 0.3 $\mu$s since turn-off begins, (b) E-field distribution under the N$^+$-emitter with 50 $\mu$m $T_{thp+}$ at 0.3 $\mu$s since turn-off begins (area shown under the N$^+$-emitter has been enlarged), (c) Half GCT cell with $D_g = 35$ $\mu$m, (d) Half GCT cell with $D_g = 75$ $\mu$m

The design of the P$^+$-base, the $D_g$ and the carrier lifetimes are found to effectively enhance or reduce the MCC of GCT. Using simulation, an optimum set of those parameters has been obtained to maximise the MCC for HCBs.
The doping concentration of the N-buffer strongly affects the maximum $V_{\text{DC}}$ allowed to turn off a certain load current. Such a higher $V_{\text{DC}}$ can reduce the required number of IGCTs connected in series for HCBs.

By combining the optimisation results, in simulation an MCC of 5.5 kA at $V_{\text{DC}}=4.5$ kV is achieved, using a P$^+$-base thickness of 45 μm, minority carrier lifetimes of $\tau_{\text{P}}=8 \, \mu$s, $\tau_{\text{N}}=2 \, \mu$s, $N_{\text{NB}}$ of $5 \times 10^{16}$ cm$^{-3}$, and $D_0$ of 85 μm, operating at $\text{Temp}=360$ K.

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