Article

Design and Analysis of a Novel 24 GHz Up-Conversion Mixer with Improved Derivative Super-Position Linearizer Technique for 5G Applications

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Abstract: A 24 GHz high linear, high-gain up-conversion mixer is realized for fifth-generation (5G) applications in the 65 nm CMOS process. The mixer’s linearity is increased by applying an Improved Derivative Super-Position (I-DS) technique cascaded between the mixer’s transconductance and switching stage. The high gain and stability of amplifiers in the transconductance stage of the mixer are achieved using novel tunable capacitive cross-coupled common source (TCC-CS) transistors. Using the I-DS, the third-order non-linear coefficient of current is closed to zero, enhancing the linearity. Additionally, a TCC-CS, which is realized by varactors, neutralizes the gate-to-drain parasitic capacitance ($C_{gd}$) of transistors in the transconductance stage of the mixer and contributes to the improvement of the gain and stability of the mixer. The measured 1 dB compression point $O_{P1}$ dB of the designed mixer is 4.1 dBm and $I_{P1}$ dB is 0.67 dBm at 24 GHz. The conversion gain of 4.1 dB at 24 GHz and 3.2 ± 0.9 dB, from 20 to 30 GHz is achieved in the designed mixer. Furthermore, a noise figure of 3.8 dB is noted at 24 GHz. The power consumption of the mixer is 4.9 mW at 1.2 V, while the chip area of the designed mixer is 0.4 mm$^2$.

Keywords: 5G; wireless communication; transmitter; up-conversion mixer; Improved Derivative Super-Position

1. Introduction

In recent studies, the demand for 5G communication systems was shown to have enormously increased. There are many 5G mobile communication devices available; some of them are wireless broadband internet, cellular phones, etc. Low power, low voltage and highly linear RF circuits attract considerable attention in regard to prolonging the battery life of communication systems. The 5G system is becoming a necessity in wireless communication [1,2]. Existing technologies, including LTE and 4G mobile communications, cannot satisfy the increasing demands for a fast data rate, low latency and larger capacity. The 5G system is 1000 times faster than 4G technology. Furthermore, 5G accumulates high data traffic capacity. Many advanced communication applications require a high capacity, high data rate communication system, and the 5G technologies fulfill these requirements. A frequency band from 20 GHz to 30 GHz has been relevant in 5G radar applications [3]. Vehicular Radar systems can give useful insight into the other millimeter-wave applications. Additionally, in the automotive sector, radars are widely employed for the development of cars, which offer the basis for a secure and intelligent transport system [4]. The 5G frequency spectrum gained a great deal of attention because of its prospective usage of automobile vehicles for radar applications [5]. Nowadays, automotive radar is regarded...
as one of 5G technology’s most important vertical markets. Thus, in [6], the author also
describes a 5G transceiver radar application (24 GHz) that achieves a high data rate and
wide bandwidth. The radar applications in automobile vehicles and radar transmitter
design are shown in Figure 1a,b, respectively.

Figure 1. (a) Automobile radar application, (b) radar transmitter design.

High integration, low power, low noise, and high linearity are the main design
requirements in the 5G transmitter design. An up-conversion mixer is the main circuit
block in a 5G radar transmitter design. Designing a highly linear, high-gain up-conversion
mixer is a fundamental challenge in transmitter design. A highly linear, high-gain up-
conversion mixer is compulsory to overcome the transmitter linearity limitation. Linearity
is an essential characteristic of an up-conversion mixer because a transmitter with a mixer
with low linear output requires a buffer amplifier to drive a power amplifier that degrades
the linearity. So, a linear up-conversion mixer with a high-output 1 dB compression
point (OP1dB) benefits the transmitter design. The block diagram and schematic of the
conventional mixer are shown in Figure 2a,b, respectively.

Related Literature Survey

In general, mixers are often categorized as passive and active mixers. Passive mixers
can be used to generate an intermediate frequency (IF) for a local oscillator (LO) driving
signal by using passive switches. Passive mixers could attenuate the signal. On the other
hand, active mixers offer a positive conversion gain (CG), while passive mixers do not [7].
However, passive mixers are simple. They have zero power consumption, are highly linear,
have good NF, but they require a high LO power. Active mixers offer excellent CGs, good
port isolation, and minimum NF and LO power, unlike passive mixers. When analyzing
all these facts, active mixers are preferred over passive mixers.
Recently, many active CMOS up/down mixers [8] were reported with different topologies that enhanced the linearity and gain performances. Zumbahlen et al. [9] proposed a circuit with a minimum amount of noise and strong linearity, while Siddqui et al. [10] described the mixer design as having a minimal NF but inadequate CG and linearity. Additionally, in [11], the proposed mixers have minimal power consumption and high linearity; however, these mixers are often employed at the expense of port isolation, and the shortcoming is that they require a high LO power. In [12], the author designed the most popular Gilbert mixer, showing high isolation. Another previous study [13] described a mixer with high performance in terms of CG and NF but at the expense of linearity. In [14,15], the LO and radio frequency (RF) signals were applied at the drain and gate terminals of the transistor, but these mixers suffered with poor linearity. In [16,17], to enhance the linearity, a CMOS mixer operating at 2.4 GHz with a derivative superposition (DS) technique and a mixer design with input active balun is presented. However, this mixer design increases the power consumption. In [18], a 60 GHz mixer with direct up-conversion architecture achieved a gain of 4.5 dB; however, it had poor linearity and power dissipation of 15.1 mW. Various other up-conversion 24 GHz CMOS mixers are described in [19,20] and showed a degraded linearity performance.

In [21], an up-conversion mixer was designed in a 90 nm CMOS process with dual pMOS and nMOS cross-coupled transistors to gain of 2.1 dB due to the current injection and negative resistance provided by these transistor pairs, but the linearity performance was degraded and it exhibited the 1 dB compression point of $-10$ dBm. Further, a Tanh-mixer with $N = 3$ is reported in [22], achieving a high gain of 3.8 dB. This mixer achieved an excellent gain result but the isolation and power consumption of 21.1 dB and 107 mW, respectively, degraded the overall performance mixer circuit.

For high gain and excellent isolation, the Gilbert-cell mixer circuit is most commonly used [23–27]. The linearity of the Gilbert-cell mixer depends on the input transconductance stage, which consists of a transconductance amplifier (TA). In [25], a mixer design with cross-coupled voltage bias and offset TA is presented, and its transconductance depended on the linearly varied bias offset voltages. However, this technique does not adhere with the technology scaling, which required low supply voltages. In [22,27], a mixer design was fabricated with the implementation of a transconductance stage based on a negative-feedback loop to address the linearity, but the negative-feedback loop decreased the gain of the circuit.

Furthermore, to achieve high linearity and gain, many CMOS mixers are designed by using different linearity techniques such as a dual transconductance ($G_m$) boosting.
path along with dual n/PMOS switches [28], a cascode folded mixer [29], the insertion of source-degenerated resistors [30], a class-AB amplifier $G_m$ stage [31–33], employing a diode linearity technique [34] and integrating high-order harmonic termination [35]. All these linearity techniques either make the mixer circuit complex or lower the gain.

According to the author’s best knowledge, literature based on the design of CMOS up-conversion mixers operating at a particular 24 GHz frequency with high linearity and high gains is not frequently published. Figure 3 describes the literature survey of up-conversion mixers in terms of conversion gain, and OP$_{1\, \text{dB}}$ operating within the frequency range of 15–35 GHz. As our paper deals with the specific 24 GHz frequency, we made a fair comparison between the other published articles in a similar frequency range for the simplicity of the paper. Hence, the prior research shows that while the frequency range is from 15 to 35 GHz, all the authors work on the one specific parameter, i.e., to increase the conversion gain or to enhance the linearity of the up-conversion mixers. Only the previous research in [21] presents a 24 GHz up-conversion mixer that achieved a high conversion gain and high linearity concurrently. This paper’s limitation is that it is confined to this idea, and it does not discuss technical details thoroughly. Furthermore, the application is limited to automotive radar applications, while our work deals with 5G applications at 24 GHz frequencies.

In our work, the novelty lies in the fact that we are able to achieve high gain and high linearity simultaneously, with the help of our newly proposed technique. Hence, the designed up-conversion mixer includes tunable capacitive cross-coupled common source (TCC-CS) transistors to increase the gain. Furthermore, The I-DS technique also boosts the linearity. By using TCC-CS and I-DS techniques, the designed mixer archives high gain and high linearity with moderate power consumption. The up-conversion mixer achieves a peak CG of 4.1 dB at 24 GHz and the measured IP$_{1\, \text{dB}}$ of the designed mixer is 0.67 dBm at frequencies from 20 to 30 GHz, which is one of the highest-frequency up-conversion mixers among 65 nm technologies reported for 5G applications.

The remaining part of the paper is set out as follows. Section 2 describes the proposed up-conversion mixer system design. The results and discussion are shown in Section 3. The conclusion is finally drawn in Section 4.
2. Proposed Up-Conversion Mixer Design

The proposed up-conversion mixer’s schematic is shown in Figure 4. The 2.4 GHz IF input signal is amplified in the Gm stage, which consists of TCC-CS and I-DS. The TCC-CS is implemented with CS transistors M1, M2, and varactors Cv1, Cv2, the varactors are biased with tuning voltage Vt. The I-DS contains primary transistors, Mp, secondary transistors, Ms, dc blocking capacitors, C3-C6 and source-degenerated inductors, Ls1 and Ls2. The Ls1 and Ls2 are source-degenerated inductors of the primary and secondary transistors of I-DS. The linearized and the amplified output signal of the Gm stage is fed into the switching stage of the mixer, which comprises transistors M3–M6, and an LO signal of 21.6 GHz is applied at the gate terminal of these transistors. The Gm stage signal is translated to a 24 GHz RF output signal at the switching stage. At the RF output stage, the RF output buffer (not shown in the mixer schematic (Figure 4) for simplicity) is designed in a push/pull configuration by using a PMOS transistor (Mpb), NMOS transistor (Mnb) and feedback resistor (Rf) to match the 50 Ohm resistance.

In the designed mixer, TCC-CS topology provides a high gain and stability, downgraded in CS topology due to parasitic gate to drain capacitances (Cgd) of transistor M1 and M2. The conventional capacitive neutralization proposed TCC-CS and the realization of a varactor in TCC-CS is shown in Figure 5a–c, respectively. A cross-coupled capacitor Cv1 connected between the drain terminal of M1 and the gate terminal, M2m acts as a negative equivalent to capacitor Cv2, which is connected between the drain terminal of M2 and gate terminal, M1. The capacitance, Cv1 and Cv2, is used to nullify the parasitic capacitance, Cgd1, of M1 and Cgd2 of M2 as the signals across the varactor and Cgd are opposite in phase. The tuning voltage, Vt, of varactors applied at the source of transistor Mcv (Figure 5c) to cancel the effect of Cgd is small so that transistor operates in the subthreshold region and does not contribute much to the overall power consumption of mixer.

While the inclusion of I-DS in between TCC-CS topology and switching stage enhances the proposed mixer’s linearity, in I-DS, secondary transistor, Ms, is connected parallel to the primary transistor, Mp. The secondary transistor of I-DS, Ms, operates in the moderate-inversion region with biasing voltage, Vb1, instead of the conventional DS technique where secondary transistors operate in the weak-inversion region. Meanwhile, primary transistors, Mp, operates in the strong-inversion region with biasing voltage, Vb2. The moderate inversion region biasing of Ms helps to reduce the gate noise, which is inversely proportional to the current Ids3 of Ms. The I–V DC characteristic curve of the

**Figure 3.** Literature survey of up-conversion mixers [14,22,33,36–41] with operating frequencies of 15–35 GHz. (a) Conversion gain, (b) OP1dB.
MOS transistors of 65 nm CMOS technology is shown in Figures 6 and 7. As illustrated by the I–V DC characteristic curve, the transistor operating region can be categorized into three regions: moderate-inversion, strong-inversion and weak-inversion, depending on the transistor’s biasing conditions.

Figure 4. Proposed up-conversion mixer.

Figure 5. (a) Conventional capacitive cross-coupling neutralization, (b) TCC-CS and (c) varactor realization in TCC-CS.
Figure 6. I–V DC characteristic curve of the transistors with drain current $\ln(ID)$ on the vertical-axis.

Figure 7. I–V DC characteristic curve of the transistors with drain current $\sqrt{ID}$ on the vertical-axis.

The small signal model of the transconductance stage of the designed mixer is shown in Figure 8.

Figure 8. Small signal model of the transconductance stage.
The stability factor, $K$, of $M_1$ transistor of TCC-CS is shown in Equation (1) and the simulated $K$ is shown in Figure 9. The amplifier is stable if $K > 1$ [14].

\[
K = \frac{2 + \omega^2 (C_{gd1} - C_{v1})^2}{\omega |C_{gd1} - C_{v1}| \sqrt{\omega^2 (C_{gd1} - C_{v1})^2 + s_{m1}}}
\]  

(1)

Figure 9. Stability Factor $K$.

Equation (1) shows that when varactor’s capacitance $C_{v1}$ is equal to $C_{gd1}$, the stability factor is maximum. As we use a varactor’s capacitance, to neutralize the $C_{gd}$, which can be controlled externally, the PVT variations do not affect the stability of $M_1$. The simulated varactor capacitance versus the voltage, $V_{t}$, is shown in Figure 10. The gain, $G$, of TCC-CS of the transconductance stage is expressed in Equation (2) and the calculated result of $G$ versus the varator capacitance is shown in Figure 11.

Figure 10. Varactor capacitance versus voltage $V_{t}$. 
\[ G = \frac{\sqrt{\omega^2 (C_{gd1} - C_{v1})^2 + s^2_{m1}}}{\left| C_{gd1} - C_{v1} \right|} \left( \frac{2 + \omega^2 (C_{gd1} - C_{v1})^2}{\omega |C_{gd1} - C_{v1}| \sqrt{\omega^2 (C_{gd1} - C_{v1})^2 + s^2_{m1}}} \right) \]

\[ - \left[ \frac{2 + \omega^2 (C_{gd1} - C_{v1})^2}{\omega |C_{gd1} - C_{v1}| \sqrt{\omega^2 (C_{gd1} - C_{v1})^2 + s^2_{m1}}} \right]^2 - 1 \] (2)

Figure 11. Theoretical result of G.

Equation (2) shows that the TCC-CS along with stabilization also enhances the gain of the designed mixer. The device sizes of the designed mixer are shown in Table 1.

Table 1. Designed mixer circuit component values.

| Element     | Dimension      |
|-------------|----------------|
| $M_1, M_2$  | 31 µm/65 nm    |
| $M_p$       | 53 µm/65 nm    |
| $M_s$       | 41 µm/65 nm    |
| $M_3$–$M_6$ | 37 µm/65 nm    |
| $M_{cv}$    | 34 µm/65 nm    |
| $L_1$–$L_2$ | 175 pH         |
| $L_{s1}$    | 70 pH          |
| $L_{s2}$    | 90 pH          |
| $C_3$–$C_6$ | 45 fF          |
| $C_{v1}$–$C_{v2}$ | 29.3 fF @ $V_t = 0.75$ V |

2.1. Linearity Analysis

The simulated fundamental transconductances ($g_{m}$), represented as, “$g_{m1s}$”, “$g_{m1p}$” and “$g_{m1s} + g_{m1p}$” of transistors $M_s, M_p$, the second-order transconductance ($g_{m'}$) mentioned as “$g_{m2s}$”, “$g_{m2p}$” and “$g_{m2s} + g_{m2p}$” of transistors $M_s, M_p$, and the third-order transconductance ($g_{m''}$) noted as, “$g_{m3s}$”, “$g_{m3p}$” and “$g_{m3s} + g_{m3p}$” of transistors $M_s, M_p$, with respect to biasing voltage, $V_b$, are shown in Figures 12–14, respectively.
Figure 12. The simulated $g_{m1s}$, $g_{m1p}$ and $g_{m1s} + g_{m1p}$ of $M_p$ and $M_s$ transistors.

Figure 13. The simulated $g_{m2s}$, $g_{m2p}$ and $g_{m2s} + g_{m2p}$ of $M_p$ and $M_s$ transistors.

Figure 14. The simulated $g_{m3s}$, $g_{m3p}$ and $g_{m3s} + g_{m3p}$ of $M_p$ and $M_s$ transistors.

When it works in the saturation region, the operating region of the CMOS transistor is classified into three different regions: weak/moderate/strong inversion regions. The primary reason for non-linearity in the CMOS transistor is the transconductance ($g_m$) [30]. In the weak-inversion region, the operational speed of the CMOS transistor is
slow, but the ratio of $g_m$ and drain current ($I_d$) is high, while it is reversed in the case of the strong-inversion region of the CMOS transistor. The moderate-inversion region exhibits good operational speed and a good $g_m/I_d$ ratio. The drain to source current ($I_{ds}$) of a CS transistor is shown in Equation (3) [31].

$$I_{ds} = I_{dc} + g_{m1}V_{gs} + g_{m2}V_{gs}^2 + g_{m3}V_{gs}^3 + ... \tag{3}$$

The $g_{m2}$ and $g_{m3}$ are the primary factors on which the IIP3 of the CMOS transistor depends. The IIP3 for the I-DS technique is shown in Equation (4).

$$IIP3 = \frac{2g_{m1}^2\omega^2[L_{s1}(C_{gs} + C_{gss}) + L_{s2}C_{gss}]}{3|\alpha|} \tag{4}$$

$$\alpha = g_{m3p}(1 + j\omega L_{s2}g_{m1s})(1 + j\omega L_{s2}g_{m1s}) \left[1 + \frac{L_{s2}C_{gss}}{L_{s1}(C_{gs} + C_{gss}) + L_{s2}C_{gss}} \right]$$

$$+ g_{m3s} - \frac{2g_{m2s}}{3g_{m1s}} \left(\frac{1}{1 + (1/2\omega(L_{s1} + L_{s2})g_{m1s})}\right) \tag{5}$$

where $C_{gss}$ and $C_{gs}$ represent the parasitic gate-source capacitances of M_s, M_p transistors of I-DS. It is shown from Equation (4) that, by selecting proper values for $L_{s1}$ and $L_{s2}$, the effects of $g_{m2}$ on the IIP3 can be reduced, which helps to improve the linearity of the designed mixer.

By carefully determining the sizes of transistors, source-degenerated inductors of the I-DS technique and with proper biasing conditions, the linearity of the proposed mixer is improved. $L_{s1}$ and $L_{s2}$ tune out the second-order non-linear components. At the same time, the third-order non-linear components can be diminished by choosing proper I-DS transistor sizes and biasing conditions [42].

2.2. Layout Issues

The proposed mixer, which comprises the TCC-CS, I-DS technique, is fabricated in 65 nm CMOS technology. The mixer chip microphotograph is shown in Figure 15. The mixer’s chip size is 0.4 mm$^2$ (0.71 × 0.57 mm$^2$), with the exclusion of chip pads. Chip layout is carried out to ensure the stable permanence of the mixer and to reduce the parasitic resistive, capacitive and inductive effects of interconnecting lines and the parasitic capacitive effects of multiple diffusion strips. The size of transistors is divided into multiple fingers to decrease the series resistance and parasitic capacitances of the gate of transistors. Furthermore, due to multiple finger transistors, the nonlinearity due to shunt capacitance decreases and high gain is achieved. The proposed mixer’s ground layer is designed with a multi-layer technique by using different metal layers to develop a low inductive and resistive ground path. Thick and large power lines are designed to achieve the good analog current (AC) coupling between the ground and also to prevent a voltage drop. The metal insulator metal (MIM) with a capacitance of 2.2 fF/µm$^2$ is used to design a capacitor. Meanwhile, inductors of the mixer with a quality factor (Q) equal to 12 are designed by using metal layer 5 of 65 nm CMOS technology with 12 µm thickness. To mitigate the electromagnetic interference (EMI) in between the inductors, a 16 µm ground plane shield from the inductor coil is implemented.
The up-conversion mixer is fabricated in 65 nm CMOS technology and the operating characteristics of the mixer are simulated and measured. The measuring probes with a ground–signal–ground–signal–ground (GSGSG) pattern are used to measure the characteristics of the mixer. The mixer operates at 1.2 V dc voltage supply, while it consumes power equal to 4.9 mW. The measured return loss of the proposed mixer is depicted in Figure 16. The IF port of the mixer at 2.4 GHz shows a return loss of $-22.6$ dB, the RF port of the mixer at 24 GHz shows a return loss of $-20.7$ dB and the LO-port of the mixer at 21.6 GHz shows a return loss of $-24.8$ dB.

The isolation between LO-port to RF-port, RF-port to IF-port, and LO-port to IF-port of the mixer at 24 GHz is $-35.1$ dB, $-27.3$ dB, $-40$ dB, respectively, and it is shown in Figure 17.
Figure 17. Isolations between mixer’s ports.

The proposed mixer’s conversion gain is simulated and measured for 24 GHz up-converted RF frequency, with the 21.6 GHz LO frequency, and 2.4 GHz IF frequency. The conversion gain increases with the increment of the LO power, but for low power operation, LO is selected to be 2 dBm. The maximum measured conversion gain at 24 GHz RF frequency is 4.1 dB. The conversion gain of a mixer is equal to $3.2 \pm 0.9$ dB, versus frequency from 20 to 30 GHz is illustrated in Figure 18, while conversion gain versus LO power from $-8$ dBm to 8 dBm is shown in Figure 19.

Figure 18. Conversion gain vs. frequency of the mixer.
The linearity result of the proposed up-conversion mixer is illustrated in Figure 20, which shows input power versus output power curves. The mixer shows a measured $OIP_{1}$ of 4.1 dBm, and the $IIP_{1}$ is 0.67 dBm, respectively, demonstrating good linear performance.

The noise figure (NF) performance of the mixer is indicated in Figure 21. The NF of 3.8 dB at RF frequency of 24 GHz is achieved. The NF is comparatively high because of the insertion of extra transistors of I-DS transistors. The up-converted $RF_{out+}$ and $RF_{out-}$ transient wave-forms of the designed mixer are shown in Figure 22, where up-converted RF output signal is 24 GHz. The peak–peak voltage swing of RF signal of the mixer is equal to 80 mV.
Proposed Mixer vs. State-of-the-Art Designs

The result summary of the mixer is listed in Table 2 and compared to already-published state-of-the-art designs of CMOS mixers.

Table 2. Comparison summary for recently reported results.

| Ref. | Process (nm) | RF Freq. (GHz) | Gain (dB) | OP dB | Chip Area (mm²) | Power Consumption (mW) | NF |
|------|--------------|---------------|----------|-------|----------------|------------------------|----|
| [19], 2015 | 130          | 23.4–29.2     | −1.9     | 0.3   | 0.8            | 38                     | NA |
| [21], 2021 | 65           | 24            | 4.7      | 0.41  | 0.42           | 5.2                    | 3.8 |
| [43], 2017 | 65           | 27.5–43.5     | −5       | 0.42  | 0.686          | 14                     | NA |
| [44], 2008 | 65           | 60            | −6.5     | −5    | 0.98           | 29                     | NA |
| [45], 2006 | 130          | 18–28         | 0.7      | −5.2  | 0.46           | 22.8                   | NA |
| [46], 2019 | 65           | 17–43         | 1.6      | NA    | 0.5            | NA                     | 12.4|
| [47], 2006 | 180          | 3.1–10.6      | 10       | NA    | 1              | NA                     | 10 |
| [48], 2012 | 180          | 2.4           | 7.1      | NA    | 0.4            | 4.5                    | 11.9|
| [49], 2007 | 250          | 3.5           | 3.8      | NA    | 0.34           | 3.5                    | 8  |
| [This Work] | 65           | 24            | 4.1      | 4.1   | 0.4            | 4.9                    | 3.8 |
4. Conclusions

A 24 GHz up-conversion mixer using 65 nm CMOS technology is proposed for 5G automobile radar applications. This paper aimed to simultaneously increase mixer gain and linearity in the 24 GHz frequency range. Therefore, we proposed a new tunable capacitive cross-coupled common source technique and linearizing I-DS technique. By using TCC-CS in the transconductance stage of the mixer, the gain and stability of the mixer were improved. Furthermore, the I-DS mitigates the third-order nonlinear coefficient and enhances linearity. The measured OP1dB of the designed mixer is 4.1 dBm, with a conversion gain of 4.1 dB at 24 GHz and 3.2 ± 0.9 dB, at frequencies from 20 to 30 GHz, and a noise figure of 3.8 dB at 24 GHz. The mixer only consumes 4.9 mW at 1.2 V. We believe that the proposed mixer has high linearity, high gain, and low DC power consumption at 24 GHz, and is best suitable for low-power 5G automobile radar applications.

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