Virtual Subspace-based DTC Strategy For Torque Ripple Minimization in Six-phase Induction Motors

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ABSTRACT Classical switching-table-based direct torque control (ST-DTC) of six-phase induction machine (6PIM) drives is seriously penalized by current harmonics as well as torque ripples because of uncontrolled voltage vectors in the low-impedance non-energy subspace and hysteresis torque regulator, respectively. Hence, a virtual subspace-based DTC strategy is proposed to alleviate the impact of low-order current harmonics and torque ripples. The proposed virtual subspace includes 48 virtual voltage vectors (VVs) in the \( \alpha - \beta \) subspace with average volt-seconds of zero in the \( z_1 - z_2 \) subspace, which offers full extent of freedom degrees for 6PIM fed by a two-level voltage source inverter (VSI). The increased number of VVs allows the possibility to design up to nine-level hysteresis torque regulator to minimize the torque ripples. Nevertheless, in this paper, it is found that torque ripple, current harmonics, average switching frequency, and computational burden come to a compromise with a seven-level hysteresis torque regulator. The impact of these VVs on the performance of ST-DTC is experimentally studied and some details of hardware implementation are presented. The performance of the proposed scheme is verified by simulations as well as laboratory experiments, where a complete comparison with recent schemes is made to reveal the superiority of the proposed scheme.

INDEX TERMS Direct torque control (DTC), six-phase induction machine (6PIM), switching table, torque ripple, virtual voltage vectors (VVs), virtual subspace.

I. INTRODUCTION

A. MOTIVATION

Switching-table-based direct torque control (ST-DTC) strategy has much to offer in terms of fast dynamic, simplicity, and low parameter dependency [1], [2]. As frequently mentioned in the literature, the classical ST-DTC suffers from high torque ripple and variable switching frequency due to hysteresis regulators [3]. Modulation-based DTC has been proposed to tackle these problems [4], [5], however, it may overshadow fast dynamic, simplicity, and robustness of ST-DTC [6].

Safety-critical applications, such as fuel pumps, electric vehicle and ship propulsion systems, are the main beneficiary of the multi-phase drives (with more than three phases) due to their inherent fault-tolerant capability without any extra equipment [7]–[9]. Beside aforementioned problems in relation to ST-DTC, simple extension of the classical ST-DTC to multi-phase drives causes an additional problem in term of current harmonics, when only large voltage vectors are selected during the whole sampling period [10]. The reason lies in the fact that the secondary components, i.e., \( z_1 - z_2 \) components, remain uncontrolled when only large voltage vectors are applied. These cases highlight the need for an efficient ST-DTC for multi-phase drives. Among possible choices of multi-phase drives, an asymmetrical six-phase induction machine (6PIM) with two three-phase winding sets, which are spatially shifted by \( \pi/6 \), is a promising structure because the three-phase technologies can be conveniently generalized to six-phase ones [11]. Such a structure is depicted in Fig. 1.

B. LITERATURE REVIEW

There is a fruitful research activity to overcome the problems of classical ST-DTC for multi-phase drives [12]–[17]. Appli-
The duty ratio is calculated to remove the average volt-sec in combination of large, medium, and small voltage vectors. The virtual voltage vectors (VVs), which are defined as a combination of large, medium, and small voltage vectors. The duty ratio control-based ST-DTC has been established in response to current harmonics due to nonzero voltage vectors in the secondary subspace, but not the current harmonics due to dead time, winding asymmetry, and back electromotive force distortion. To overcome later cases, a DTC strategy using proportional-integral-resonant (PIR) current controller has been proposed in [17]. Nevertheless, such a DTC schemes cannot reduce the torque ripple significantly.

Increasing the action points in the hysteresis torque regulator has been found suitable for torque ripple reduction in the multi-phase drives [19]–[22]. Fortunately, further voltage vectors in the multi-phase drives in comparison with three-phase ones offer the possibility to adopt five-phase hysteresis torque regulator, where the outer band is responsible for the good dynamic performance while the inner band is responsible for the torque ripple reduction [20]. Such a scheme with symmetrical and asymmetrical pulse patterns has been proposed in [20] and [21], respectively. Switching frequency and complexity are the main differences between symmetrical and asymmetrical pulse patterns. Furthermore, a seven-level hysteresis torque regulator has been proposed in [22] for 5PIIM fed by the three-level voltage source inverter (VSI), where some improved results can be found against five-level hysteresis regulator. Modifying the switching table [23], [24], improving the three-level hysteresis torque regulator [15], controlling the duty ratio of the active voltage vectors by inserting zero voltage vectors [25], and combining the ST-DTC and space vector modulation (SVM)-based DTC schemes [26] are some other attempts to tackle the problem of high torque ripple in the classical ST-DTC.

C. PAPER CONTRIBUTION

In order to improve the performance of the classical ST-DTC in terms of torque ripples and low-order current harmonics, and at the same time, to retain the fast dynamic and simplicity of ST-DTC, this paper proposes a virtual subspace-based ST-DTC using a seven-level hysteresis torque regulator for a two-level dual three-phase VSI-fed 6PIIM. The proposed virtual subspace contains 48 VVs with partially reduced voltage levels in the $\alpha - \beta$ subspace as compared to actual ones and zero averages in the $z_1 - z_2$ subspace, hence, they can effectively reduce the harmonics mapped into the $z_1 - z_2$ subspace. Since that a two-level dual three-phase VSI has totally 48 unique active voltage vectors, it can be said that the ST-DTC can fully access the additional freedom degrees, i.e., different voltage levels, through defining this virtual subspace. Therefore, torque ripples can be significantly reduced by a multilevel hysteresis torque regulator. To highlight the contribution of the paper, the proposed scheme is experimentally compared with the conventional ST-DTC as well as the prior arts presented in [15], [20], [21] from different viewpoints.

D. PAPER STRUCTURE

The rest of the paper is organized as follows. Section II discusses the feasible VVs in a two-level dual three-phase VSI with their properties. The proposed ST-DTC is presented in section III, where the virtual subspace is firstly defined. Then, the impact of VVs on the dynamic and steady-state (SS) performances of ST-DTC is studied experimentally. Accordingly, a seven-level hysteresis torque regulator-based ST-DTC is investigated. Experimental results and quantitative comparisons are given in section IV. Finally, section V summarizes the findings and concludes the paper.

II. VIRTUAL VOLTAGE VECTORS

There are totally $2^6 = 64$ switching states in two-level dual three-phase VSIs. The switching states constitute 64 non-unique voltage vectors in the $\alpha - \beta$, $z_1 - z_2$, and $o_1 - o_2$ sub-
TABLE 1. Voltage vectors classification of the dual three-phase VSI in $\alpha - \beta$ subspaces.

| Group name | Symbol | Decimal sample | Amplitude | DC-link utilization ($\eta$) |
|------------|--------|----------------|-----------|----------------------------|
| Large      | $V_L$  | 48             | $2V_{dc}\cos(\pi/12)/3$ | 100%                      |
| Medium large | $V_{ML}$ | 57             | $2V_{dc}\cos(3\pi/12)/3$ | 73.21%                    |
| Medium small | $V_{MS}$ | 16(58)       | $V_{dc}/3$           | 51.76%                    |
| Small      | $V_S$  | 54             | $2V_{dc}\cos(5\pi/12)/3$ | 26.79%                    |

In the case of 6PIM with two isolated stator sets, the voltage vectors are mapped into the origin of $a_1 - a_2$ subspace. For this case, the voltage vectors in the $\alpha - \beta$ and $z_1 - z_2$ subspaces are shown in Fig. 2. The $\alpha - \beta$ components contribute towards electromechanical energy conversion, while the $z_1 - z_2$ components only cause losses. Among these vectors, there are four zero voltage vectors and 48 unique active voltage vectors, which are spatially distributed in the $\alpha - \beta$ of $z_1 - z_2$ subspaces. Four voltage levels are formed by these active voltage vectors, which are shown as four nonzero dodecagons in Fig. 2. Each decimal number represents a switching state using a binary sequence as $S = [S_L, S_M, S_M, S_M, S_M, S_M]$, where $S$ is the state of upper switches. The voltage vectors in the $\alpha - \beta$ subspace are categorized according to Table 1. The amplitude of the large and small voltage vectors in the $\alpha - \beta$ subspace is reversed in the $z_1 - z_2$ subspace, while the amplitude of the medium large and the medium small vectors remains constant in both subspaces. Defining the voltage vectors as $V_{hk}$, with $h \in \{L, ML, MS, S\}$ and $k$ is the voltage number corresponding to the $\alpha - \beta$ subspace, if $k$ increases by +1 in the $\alpha - \beta$ subspace, it will increase by +5 or −7 in the $z_1 - z_2$ subspace, because the $z_1 - z_2$ subspace contains fifth and seventh harmonics rotating with $+5\omega_s$ and $-7\omega_s$ frequencies [27], where $\omega_s$ is the fundamental frequency.

For control techniques without modulation strategy such as ST-DTC and predictive torque control (PTC), where the voltage vectors are selected according to the switching table and cost function minimization, respectively, applying the actual voltage vectors during whole sampling period leads to the large current harmonics due to the non-zero voltage vectors in the $z_1 - z_2$ subspace. Replacing the actual voltage vectors by VVs is a promising solution to manage this problem, where VVs are constructed using actual voltage vectors with appropriate action times to make an average volt-seconds of zero in the $z_1 - z_2$ subspace.

The classification of VVs for dual three-phase VSI in the $\alpha - \beta$ subspace is tabulated in Table 2. Furthermore, the normalized VVs in the $\alpha - \beta$ and $z_1 - z_2$ subspaces are shown in Fig. 3. The voltage space vectors are given by

$$v_{\alpha\beta} = \frac{1}{3} [V_{u1} + aV_{u2} + a^4V_{w1} + a^5V_{w2} + a^6V_{v1} + a^9V_{v2}]$$

$$v_{z1z2} = \frac{1}{3} [V_{w1} + a^5V_{w2} + a^6V_{w1} + aV_{w2} + a^4V_{v1} + a^9V_{v2}]$$

where $v_{\alpha\beta} = v_{\alpha} + jv_{\beta}$, $v_{z1z2} = v_{z1} + jv_{z2}$ and $a = e^{j\pi/6}$. The normalized amplitude of the voltage vectors is calculated as

$$|v_{\alpha\beta}| = \sqrt{v_{\alpha}^2 + v_{\beta}^2}$$

and the DC-link utilization rate ($\eta$) is defined as

$$\eta = \frac{|v_{\alpha\beta}|}{2\cos(\pi/12)/3} \times 100$$

The simplest VVs are synthesized using two voltage vectors (2D VVs), where the constructed VVs must include medium large voltage level, due to its opposite direction in $z_1 - z_2$ subspace against large and small voltage vectors. There are two possible groups of 2D VVs, i.e., $G_3$ and $G_2$, which offer two voltage levels in the $\alpha - \beta$ subspace as shown in Fig. 3 (b) and (c). The action times of the actual voltage vectors, used in VVs, are calculated according to a simple vector sum in the $z_1 - z_2$ subspace to provide a zero resultant vector during each sampling period $T_s$. For instance, the

TABLE 2. VVs classification of the dual three-phase VSI in $\alpha - \beta$ subspace.

| Group name | Synth. VVs | Amp. (P.U.) | $\eta$ (%) | Dec. No. | Action time (P.U.) |
|------------|------------|-------------|------------|---------|-------------------|
| 2D VVs     | $G_1$      | $V_L$       | 0.60       | 92.82   | 48                |
|            | $G_2$      | $V_M$       | 0.35       | 53.59   | 57                |
|            | $G_3$      | $V_M$       | 0.35       | 53.59   | 57                |
|            | $G_4$      | $V_M$       | 0.60       | 92.82   | 49                |
|            | $G_5$      | $V_M$       | 0.44       | 67.95   | 57                |
|            | $G_6$      | $V_M$       | 0.31       | 48.05   | 58                |
|            | $G_7$      | $V_M$       | 0.16       | 24.88   | 41                |

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action times of $T_{48}$ and $T_{57}$ (from $G_1$ group) are calculated as

$$
\begin{align*}
T_{57}.V_{48} = T_{54}.V_{57} \\
T_{48} + T_{57} = T_s
\end{align*}
$$

(6)

where superscript $z$ denotes that the amplitude of voltage vector is in the $z_1 - z_2$ subspace. Similarly, the action times of $T_{57}$ and $T_{54}$ (from $G_2$ group) are

$$
\begin{align*}
T_{57} = \frac{\cos(\pi/4)}{\cos(\pi/4)+\cos(5\pi/12)} T_s \\
T_{54} = \frac{\cos(5\pi/12)}{\cos(\pi/4)+\cos(5\pi/12)} T_s
\end{align*}
$$

(7)

As shown in Figs. 3 (b) and (c), the constructed VVs of $G_4$ group, made by three consecutive large voltage vectors, are the same as $G_1$ group. Moreover, VVs of $G_3$ group, made by two consecutive medium small voltage vectors and one medium large voltage vector between them, are the same as $G_2$ group. The differences appear in the hardware implementation, where the switching sequences are different. In order to facilitate the hardware implementation through middle-high switching sequences for upper switches of VSI, a combination of $G_1$-$G_4$ and $G_2$-$G_3$ switching sequences has been proposed [15], [20].

III. PROPOSED ST-DTC SCHEME

A. DEFINITION OF VIRTUAL SUBSPACE

As shown in Fig. 3, three voltage vectors-based VVs (3D VVs) permit utilization of the additional freedom degrees in the dual three-phase VSI through defining more voltage levels in the $\alpha - \beta$ subspace. This offers some merits as further reduction of torque ripple in comparison with classical ST-DTC as well as the proposed ST-DTC in [20] and [21]. Applying three consecutive actual voltage vectors, with the same voltage levels to constitute 3D VVs as $G_4 - G_7$ groups, can also provide a generalized ST-DTC scheme, because the action times of the constructed 3D VVs are uniform regardless of the voltage level, thus it is straightforward in the hardware implementation. Fig. 4 shows an example of VVs construction for $G_3$ group, which can be extended to $G_4$, $G_6$, and $G_7$, as well. According to this figure, the action times of $G_4 - G_7$ groups-based VVs can be calculated as

$$
\begin{align*}
T_{h(k-1)}V_{h(k-1)}\cos(\pi/6) + T_{h(k+1)}V_{h(k+1)}\cos(\pi/6) \\
= T_{hk}V_{h(k)} \\
T_{h(k-1)} + T_{h(k)} + T_{h(k+1)} = T_s \\
V_{h(k-1)} = V_{hk} = V_{h(k+1)} \\
T_{h(k-1)} = T_{h(k+1)}
\end{align*}
$$

(8)

solving (8) yields

$$
\begin{align*}
T_{h(k-1)} = T_{h(k+1)} = \frac{0.5}{1+\cos(\pi/6)} T_s \\
T_{hk} = \frac{\cos(\pi/6)}{1+\cos(\pi/6)} T_s
\end{align*}
$$

(9)
where \( h \in \{L, ML, MS, S\} \), and \( k \) is the sector (voltage) number.

Examining the 3D VVs made by three consecutive voltage vectors in each sector, as depicted in Figs. 3 (b), (d), (e) and (f), which are related to \( G_4, G_5, G_6, \) and \( G_7 \) groups, respectively, it can be seen that the voltage levels of these groups are slightly lower than their corresponding actual voltage vectors in the \( \alpha - \beta \) subspace. In this regard, according to Tables 1 and 2, the amplitude of the mentioned 3D VVs are \( 0.60V_{dc}, 0.44V_{dc}, 0.31V_{dc}, \) and \( 0.16V_{dc} \) for large, medium large, medium small, and small voltage vectors, respectively, while these numbers are \( 0.64V_{dc}, 0.47V_{dc}, 0.33V_{dc}, \) and \( 0.17V_{dc} \) for the actual ones. Therefore, it is possible to replace 48 actual voltage vectors with these 48 3D-VVs to constitute a virtual subspace, where the amplitude of the 3D VVs is slightly lower than the actual ones, while the resultant voltage vectors are zero in the secondary subspace. However, there are still some considerations in the formation of this virtual subspace from hardware implementation, switching frequency, and ST-DTC performance viewpoints. According to Figs. 3 (c) and (e), the VVs of \( G_6 \) group are shifted by \( \pi/12 \) compared to \( G_2 \) group, while their voltage level difference is about 0.04 P.U. The shifted VVs of \( G_6 \) group, which are exactly aligned with the actual medium small voltage vectors with slightly lower voltage level, may differently change the torque and flux in ST-DTC in comparison with remaining groups as well as they increase the average switching frequency. Hence, \( G_6 \) group is replaced with \( G_2 \) group. On the other hand, the \( G_1 \) and \( G_4 \) groups are theoretically the same in terms of torque and flux regulations as well as average switching frequency. However, separate implementation of \( G_4 \) group requires more computational burdens. Hence, the \( G_4 \) group is replaced by \( G_1 \) group in the proposed virtual subspace.

Fig. 5 shows the proposed virtual \( \alpha_v - \beta_v \) and \( z_{1v} - z_{2v} \) subspaces in comparison with the actual subspaces. Accepting the slightly lower DC link utilization rate and the higher average switching frequency, the proposed virtual subspace greatly enrich ST-DTC technique through lower current harmonics and torque ripple viewpoints, due to zero \( z_{1} - z_{2} \) voltage vectors and additional voltage levels, respectively. The proposed virtual subspace contains 48 VVs with zero averages of volt-sec in the \( z_{1} - z_{2} \) subspace, which are spatially distributed in different levels of \( \alpha - \beta \) subspace.

The proposed virtual subspace can be realized in the hardware implementation using totally 10 switching sequences, which are shown in Fig. 6. For the medium large and small levels-based VVs, since that VVs are made by three voltage vectors, there are totally \( 2^3 = 8 \) possible switching sequences (i.e., Case\#0-Case\#6, and Case\#9). Theoretically, these three voltage vectors can be arranged in \( 3! = 6 \) sequences. However, four sequences overlap with the remaining ones, hence, there are two different unique sequences. In this paper, the sequence of \( V_{kh(k+1)} \), \( V_{kh} \), and \( V_{kh(k+1)} \) is adopted for 3D VVs because of its symmetrical pattern. In Fig. 6, Case\#7 and Case\#8 are specific for medium small virtual voltage level, while the other cases are used for large, medium large, and small voltage levels, irrespective of Case\#0 and Case\#9. Accordingly, examples of switching sequences for the constructed VVs in the proposed virtual subspace as well as the switching states of the actual voltage vectors are presented in Table 3. There are totally 48 VVs, but only 12 of which are shown in Table 3. Each VVs is described by a decimal sequence as \( C = [c_{v1}c_{v2}c_{v3}c_{v4}], \) where \( C \in \{0, ..., 9\} \) is the switching sequence of upper VSI’s switches, which was already drawn in Fig. 6. These switching sequences can be implemented using pulse-width modulation (PWM) module in the most micro-controller platforms. The PWM settings for their implementation on TMS320F28335 digital signal controller are tabulated in the Appendix A.
TABLE 3. Example of actual and VVs switching sequences.

| Volt. | L | ML | MS | S |
|-------|---|----|----|---|
| $V_{Vh}$ | 9-9-1-0-0-1 | 9-9-2-1-4-2 | 9-9-8-7-7-8 | 6-3-5-2-2-5 |
| $V_{Vs}$ | 1-1-0-0-0-0 | 1-1-1-0-0-1 | 0-1-0-0-0-0 | 1-1-0-1-1-0 |
| $V_{Vub}$ | 0-0-9-9-9-1 | 0-1-0-0-0-1 | 0-1-0-0-0-0 | 0-1-0-0-0-0 |
| $V_{Vud}$ | 0-0-1-1-1-0 | 0-0-1-1-1-0 | 0-0-1-0-0-0 | 0-0-1-0-1-0 |
| $V_{Vb1}$ | 9-9-0-0-1-6 | 9-3-1-0-2-5 | 9-8-7-0-8-7 | 9-9-8-7-7-8 |
| $V_{Vb2}$ | 1-1-0-0-0-1 | 1-1-0-0-1-0 | 1-0-0-0-0-0 | 1-0-1-0-0-1 |

$^a k \in \{L, ML, MS, S\}$

TABLE 4. Switching Table of DTC scheme.

| $d_{lv}$ | $d_{lv}$ | Selected VVs |
|----------|----------|--------------|
| 1        | 4        | $V_{VL(k+1)}$ |
| 3        | 2        | $V_{VMS(k+1)}$ |
| 2        | 1        | $V_{VS(k+1)}$ |
| 0        | -1       | $V_{VL(k-2)}$ |
| -2       | -3       | $V_{VMS(k-2)}$ |
| -3       | -4       | $V_{VS(k-2)}$ |

$^a k$: sector number

B. EXPERIMENTAL ASSESSMENT OF THE PROPOSED VIRTUAL SUBSPACE

This section experimentally assesses the impact of VVs in the proposed virtual subspace on the SS and dynamic performances of ST-DTC for 6PIM. In this regard, different ST-DTC schemes are separately implemented using actual large voltage vectors as well as VVs belonging to the same voltage level in the virtual subspace (see Fig. 5 and Table 3). For this, three-level hysteresis torque regulator is used in ST-DTC, where the indices 5 to 1, as the output of hysteresis torque regulator, are in relation with $V_L$, $V_{VL}$, $V_{VMS}$, and $V_S$, respectively. For example, in order to study the effect of $V_{ML}$ on the performance of the ST-DTC, only $V_{ML}$ with $k \in \{1, ..., 12\}$ is selected according to the outputs of three-level hysteresis torque regulator and two-level hysteresis flux regulator using a switching table, which is drawn in Table 4.

The experimental study for SS and dynamic performances of ST-DTC of 6PIM for different VVs as well as actual voltage vectors is summarized in Table 5. The adopted hysteresis torque regulators, using appropriate torque indices according to the Table 4, are depicted in the third column of Table 5, while the average switching frequency $f_{sw}$ and voltage levels can be found in the second column of this table. The SS and dynamic results are shown in fourth and fifth columns, respectively. For the SS experiments, speed and flux commands are 100 rpm (in the reverse rotation) and 0.6 Wb, respectively, under about 2 Nm load torque. For the dynamic experiments, a speed step increase from 10 rpm to 400 rpm is imposed under same loading level. All experiments are carried out under same DC link voltage, torque, and flux hysteresis bands, which are set to 3% and 1% of their rated values, respectively.

The SS results clearly shows that the torque ripple is continuously decreased, when the voltage level is decreased. In this regard, small VVs offer the lowest torque ripple, while large VVs impose the highest torque ripple on the drive system. The torque ripple of other VVs is placed in between $V_{VL}$ and $V_{VS}$. On the other hand, as expected, the large VVs guarantee stability and fast dynamic performance during sudden changes of speed as well as load torque, while the small VVs poorly behave under dynamic experiments. Similarly, the fast dynamic property of other groups takes place in between $V_{VL}$ and $V_{VS}$. The average $f_{sw}$ is obtained by counting total number of jumps of switches and calculating every 0.1 s. Obviously, the average $f_{sw}$ is increased, when the number of applied voltage vectors during each sampling period are increased, hence, $V_{VS}$ and $V_{ML}$ impose higher average $f_{sw}$. As shown in Table 5, despite the lowest torque ripple, small VVs have the highest average $f_{sw}$. The reason can be extracted from Table 3 and Fig. 6, where the total number of switching cases 2 or 5 is four for each small VVs. Cases #2 and #5 increase the average $f_{sw}$ more in comparison to other cases. For the same reason, the average $f_{sw}$ of ST-DTC scheme using $V_{ML}$ is higher than $V_{VL}$ and $V_{VMS}$. Not surprisingly, the conventional ST-DTC with $V_L$ offers the lowest average $f_{sw}$.

As discussed, lower voltage level results in lower torque ripples with poor dynamic response, even instability and SS errors. Therefore, a combination of different VVs through a multilevel hysteresis torque regulator is introduced as a promising solution, where the inner bands are responsible for torque ripple reduction and outer bands are responsible for fast and stable dynamic performance. The proposed virtual subspace offers the possibility to design up to nine-level hysteresis torque regulator, due to four levels of VVs arranged in Table 5 and zero voltage vectors, to utilize full extent of freedom degrees of dual three-phase VSI-fed 6PIM and to minimize the torque ripples. However, as it will be discussed in the next section, a seven-level hysteresis torque regulator-based ST-DTC technique is prepared to compromise on the benefits of freedom degrees.

C. ST-DTC BASED ON VIRTUAL SUBSPACE

The schematic diagram of the proposed ST-DTC, ST-DTC of [20] and [21], and conventional ST-DTC is shown in Fig. 7. A two-level hysteresis flux regulator is employed in all schemes. The classical estimation of flux is provided by

$$\psi_s = \int (v_s - R_s i_s) dt = \int u dt \quad (10)$$
where $\psi_s$, $v_s$, $i_s$, and $R_s$ are the stator flux, voltage, current, and resistance, respectively. The electromagnetic torque is expressed by

$$T_e = 3P\psi_s \otimes i_s$$  \hspace{1cm} (11)$$

where $P$ is the number of pole pairs and $\otimes$ represents cross product. Due to problems of pure integration in the classical voltage model (10), a modified voltage model is used as [28]

$$\dot{\psi_s} = \int \left[ u(1 - j\zeta \text{sgn}(\omega_s)) - \zeta |\omega_s| \psi_s \right] dt  \hspace{1cm} (12)$$

where $\zeta$ is a constant gain. The stator voltages in the stationary reference frame can be constructed using the switching states and measured DC-link voltage with a nonlinear inverter model as [29]

$$\hat{S}_m = S_m - (T_d/T_s) \text{sgn}(i_m)$$  \hspace{1cm} (13)$$

where $T_d$ is dead time and $m \in \{u_1, u_2, w_1, w_2, v_1, v_2\}$.

The experimental assessment presented in III-B, regarding the impact of different VVs on the performance of ST-DTC technique, has been mathematically investigated in [20], [21]. Briefly, the time derivative of electromagnetic torque can be

| Voltage Level & $f_{sw}$ | Torque Regulator | SS Results | Dynamic Results |
|------------------------|-----------------|------------|----------------|
| $V_L$ Avg. $f_{sw} = 2.1$ kHz | ![chart] | ![chart] | ![chart] |
| $VV_L$ Avg. $f_{sw} = 3.4$ kHz | ![chart] | ![chart] | ![chart] |
| $VV_{ML}$ Avg. $f_{sw} = 5.2$ kHz | ![chart] | ![chart] | ![chart] |
| $VV_{MS}$ Avg. $f_{sw} = 4.1$ kHz | ![chart] | ![chart] | ![chart] |
| $VV_S$ Avg. $f_{sw} = 6.7$ kHz | ![chart] | ![chart] | ![chart] |
written as [30]
\[
d\psi_s - \frac{3P}{L_s} \psi_r \sigma s + \frac{3P}{L_s} \psi_r \otimes v_s
\]
where \(\psi_r, L_s,\) and \(\omega_r\) are the rotor flux, the stator inductance, and the rotor speed, respectively, and \(\sigma\) represents dot product. It can be seen that the zero voltage vectors only decrease the torque because the third term in (14) becomes zero, while the active voltage vectors may increase or decrease the torque according to the selected voltage vectors. The effect of voltage level on the torque variation can be surveyed by the third term of (14), where larger amplitude of voltage vectors leads to a larger variation of torque because of steeper slopes of torque characteristic. It should be noted that the torque behavior is also speed-dependent due to second term in (14), whereby the absolute torque variation during increasing and decreasing is different, especially at high speeds [20].

Although the small VVs offer the lowest torque ripple, however, there are some problems associated with them. Firstly, the average switching frequency of small VVs is higher than the other VVs, which was described previously. Secondly, consider the 6PIM model in the \(z_1 - z_2\) subspace as
\[
v_{s1} = R_s i_{s2} + L_s \frac{d}{dt} i_{s1}
\]
\[
v_{s2} = R_s i_{s2} + L_s \frac{d}{dt} i_{s2}
\]
where \(L_s\) is the stator leakage inductance. Since that the small voltage vectors appear as large voltage vectors in the \(z_1 - z_2\) subspace, any asymmetries may exacerbate \(i_{s1,2}\) currents, especially when the \(L_s\) is too small. Hence, in this paper, a seven-level hysteresis torque regulator-based ST-DTC is introduced using \(VV_L, VV_M,\) and \(VV_S\). The adopted switching table was shown in Table 4, where \(\diamond\) symbol indicates the VVs used in the proposed ST-DTC scheme. Using the proposed ST-DTC scheme, torque ripple, current harmonics, average switching frequency, and computational burdens reach an agreement.

### IV. RESULTS AND COMPARISON

#### A. PRELIMINARIES

Besides some simulation results which will be presented in the next section, the performance of the proposed ST-DTC based on virtual subspace is experimentally investigated, and a comparison study is carried out using the following schemes:

- **Conventional ST-DTC using actual large voltage vectors with a three-level hysteresis torque regulator** (hereinafter labeled C3LDTC).
- **A modified ST-DTC using large VVs with a three-level hysteresis torque regulator, which has been proposed in [15] (hereinafter labeled 3LDTC).**
- **A modified ST-DTC using large and medium small VVs with a five-level hysteresis torque regulator, which has been proposed in [20], [21] (hereinafter labeled 5LDTC).**
- **Proposed ST-DTC using large, medium large, and medium small VVs with a seven-level hysteresis torque regulator** (hereinafter labeled P7LDTC).

Hysteresis torque regulators for the mentioned schemes are shown in Fig. 8. Although there are some asymmetric hysteresis torque regulators [31] to remove SS torque error, such a comparison is fair because asymmetric changing the hysteresis outputs can be applied for all hysteresis regulators shown in Fig. 8.

#### B. SIMULATION RESULTS

An extensive simulation study was carried out to investigate the performance of the proposed scheme. The simulations are run using Matlab/Simulink software with 10kHz sampling frequency, where some selected results are shown in Figs. 9 (a) and (b) for 5LDTC and P7LDTC, respectively. In these tests, the speed command is set to 70 % rated speed under rated load torque. From top to bottom, the electromagnetic torque, the stator flux, and the stator phase current traces are shown in each row. The results of other schemes, i.e., C3LDTC and 3LDTC, are omitted in this figure, while they will be also included for experimental tests. It is obvious that P7LDTC effectively reduces the average SS torque ripples in comparison with 5LDTC. For a much clearer comparison, the average torque ripple index (index1) is defined as follows:

\[
\text{index1} = \frac{1}{m} \sum_{i=1}^{m} \left( T_{ci} - T_{avg} \right)^2
\]
\[ T_{ei} \text{ and } T_{avg} \] are the instantaneous and the average torque values. Moreover, index2 is defined as a product of index1 and average switching frequency

\[ \text{index2} = f_{sw} \times \text{index1} \]  

(18)

It is worth mentioning here that index1 evaluates the average torque ripple value, while index2 considers this value, together with the average switching frequency. Obviously, lower values of both indices show better performance of the drive system. The values of index1 and index2 in different speeds and load torques for the P7LDTC and 5LDTC are shown in Fig. 10. As can be seen from this figure, the proposed scheme offers lower values of average torque ripples for different drive operating points. On the other hand, although P7LDTC inevitably increases the average switching frequency, index2 can justify the merits of P7LDTC over 5LDTC as a unified index.

C. EXPERIMENTAL TEST BENCH

A photograph of the experimental test bench is shown in Fig. 11. An ezdsp F28335 board based on TMS320F28335 digital signal controller has been used for implementing the control algorithms and generating the PWM signals, which has been programmed through code composer studio (CCS) development environment. The main control algorithm has been executed through a PWM interrupt service routine (ISR) with 10 kHz frequency, and the speed controller and calculation have been executed using a timer interrupt with 100 Hz frequency. The 6PIM is fed from dual three-phase Semikron SKiiP VSI connected to a 250-V dc power supply. An incremental shaft encoder with 2048 pulses/revolution has been used to measure the rotor pulse train. A 4-hp and 8-pole three-phase wound rotor induction motor with 48-slot stator has been rewound to provide a 4-pole asymmetrical 6PIM.

D. STEADY-STATE PERFORMANCE

Figs. 12 (a) and (b) present the SS performance results of C3LDTC, 3LDTC, 5LDTC, and P7LDTC, under no load and 50% rated load torque, respectively. The speed and stator flux commands for both cases are 100 rpm (in reverse rotation) and 0.6 Wb, respectively. From top to bottom, the electromagnetic torque, \( \omega_1 \) current, and phase currents are shown in each oscillogram. High harmonic content of the stator currents due to uncontrolled \( \omega_1 - \omega_2 \) subspace is obvious for C3LDTC. 3LDTC improves the performance of C3LDTC from current harmonic viewpoints, but not torque ripples, because there is no remarkable difference in voltage levels of \( V_L \) and \( VV_L \) used in C3LDTC and 3LDTC, respectively. As can be seen in Fig. 12, 5LDTC reduces the torque ripples in comparison to C3LDTC and 3LDTC, and P7LDTC minimizes the torque ripples to the 6PIM drive system. According to the SS test results, the proposed ST-DTC technique offers 5-10 % (of rated torque) decrease in torque ripple, but not torque ripples, because there is no remarkable difference in voltage levels of \( V_L \) and \( VV_L \) used in C3LDTC and 3LDTC, respectively. As can be seen in Fig. 12, 5LDTC reduces the torque ripples in comparison to C3LDTC and 3LDTC, and P7LDTC minimizes the torque ripples to the 6PIM drive system. According to the SS test results, the proposed ST-DTC technique offers 5-10 % (of rated torque) decrease in torque ripple in comparison with 5LDTC. Amplitude difference of phase currents, which is more visible under no load condition, is due to inherent asymmetry in the 6PIM windings and/or converters, which causes current flow in \( \omega_1 - \omega_2 \) subspace with fundamental frequency.
E. DYNAMIC PERFORMANCE

The oscillograms of Figs. 13 (a), (b), and (c) illustrate the dynamic performance of 3LDTC, 5LDTC, and P7LDTC for loading/unloading, speed reversal at no load, speed reversal under loading experiments, respectively. The electromagnetic torque, phase current, rotor speed, and stator flux modulus are shown in each oscillogram. The stator flux command is 0.6 Wb for all tests. In Fig. 13 (a), the speed command is 200 rpm (in direct rotation), and load torque suddenly increases to the rated value and decreases to zero after a short time passed. In Fig. 13 (b), the speed command is reversed from +200 rpm to -200 as a step function under no load condition. The same experiment is repeated but for 50% rated load torque, which the results are shown in Fig. 13 (c). It can be seen from the results that the P7LDTC has the minimum torque ripple in comparison with 3LDTC and 5LDTC, which was already found from SS tests. Moreover, fast dynamic property of 3LDTC is preserved in the proposed ST-DTC technique for different dynamic test scenarios.

F. SWITCHING FREQUENCY

The average \( f_{sw} \) of C3LDTC, 3LDTC, 5LDTC in [20], 5LDTC in [21], and P7LDTC for SS experiments, their results were shown in Fig. 12, is reported in Table 6. C3LDTC possesses the minimum average \( f_{sw} \) because only one voltage vector is applied to the VSI during each sampling period. 5LDTC of [20] has the maximum average \( f_{sw} \), because in that work, switching sequences have been rearranged to obtain standard middle-high pulse patterns to make it easy for implementation, but with increased average \( f_{sw} \). The average \( f_{sw} \) of 3LDTC and 5LDTC presented in [21] takes place within the medium range, i.e., lower than [20] and higher than C3LDTC. The average \( f_{sw} \) of P7LDTC is higher than 3LDTC and 5LDTC of [21], because of applying medium large VVs based on three voltage vectors in each sampling period, but it is lower than 5LDTC of [20].

| Technique       | \( f_{sw} \) (kHz) in Fig. 12 (a) | \( f_{sw} \) (kHz) in Fig. 12 (b) |
|-----------------|----------------------------------|----------------------------------|
| C3LDTC          | 1.45                             | 1.84                             |
| 3LDTC           | 2.52                             | 2.97                             |
| 5LDTC [20]      | 4.76                             | 5.12                             |
| 5LDTC [21]      | 2.81                             | 3.34                             |
| P7LDTC          | 3.54                             | 4.06                             |

TABLE 6. Switching frequency comparison

G. EXECUTION TIME

In order to investigate the software complexity of the proposed ST-DTC, its average computation burden, for the main control loop, is monitored and compared with the C3LDTC (or 3LDTC), 5LDTC in [20], and 5LDTC in [21]. It should be noted that, since the execution time is hardware dependent and programming dependent, same programming style makes such a comparison fair. The execution time, number of CPU cycles, and the percentage of CPU utilization are tabulated in Table 7. The total number of cycles in every ISR call, considering 10 kHz frequency @150 MHz CPU operating speed is 15000 cycles. As expected, the execution time of P7LDTC is the highest due to enlarged switching table as well as PWM settings, shown in Appendix A. However, the scale of differences between CPU cycles for the compared techniques may marginally overshadow modern and high-speed micro controllers.

| Technique       | Execution Time (ns) | Cycles @150 MHz | CPU utilization @150 MHz (%) |
|-----------------|---------------------|-----------------|-----------------------------|
| C3LDTC (3LDTC)  | 13720               | 2058            | 13.7                        |
| 5LDTC [20]      | 17347               | 2602            | 17.3                        |
| 5LDTC [21]      | 22513               | 3376            | 22.5                        |
| P7LDTC          | 25224               | 3784            | 25.2                        |

TABLE 7. Execution time and CPU utilization @10 kHz ISR frequency.
performs of ST-DTC technique for 6PIM was studied. A seven-level hysteresis torque regulator-based ST-DTC based on virtual subspace was proposed. The proposed ST-DTC has the merits of minimized torque ripples, reduced current harmonics, and fast dynamic property. The performance of the proposed scheme was experimentally compared with prior arts from different viewpoints. The results confirmed that the torque ripple was effectively reduced in comparison with three-level and five-level hysteresis torque regulators, while fast dynamic property of conventional ST-DTC was preserved.

APPENDIX A PWM SETTINGS FOR IMPLEMENTATION OF THE PROPOSED VIRTUAL SUBSPACE

| Case | Z | CA & CB | CMPA | CMNB |
|------|---|---------|------|------|
| 0    | Clear | Toggle | 1 + PRD | 1 + PRD |
| 1    | Clear | Toggle | (1 - k_v1)PRD | 1 + PRD |
| 2    | Clear | Toggle | k_v1PRD | (1 - k_v1)PRD |
| 3    | Clear | Toggle | k_v1PRD | 1 + PRD |
| 4    | Set | Toggle | k_v1PRD | 1 + PRD |
| 5    | Set | Toggle | (1 - k_v1)PRD | 1 + PRD |
| 6    | Set | Toggle | k_v1PRD | (1 - k_v1)PRD |
| 7    | Clear | Toggle | k_v2PRD | 1 + PRD |
| 8    | Set | Toggle | k_v2PRD | 1 + PRD |
| 9    | Set | Toggle | 1 + PRD | 1 + PRD |

\*k_v1 = 2 - \sqrt{3}, k_v2 = \sqrt{3}/3; PRD: specified period.

REFERENCES

[1] I. Takahashi and T. Noguchi, “A new quick-response and high-efficiency control strategy of an induction motor,” IEEE Trans. Ind. Appl., vol. IA-22, no. 5, pp. 820–827, 1986.

[2] M. H. Holakooie, M. Ojaghi, and A. Taheri, “Direct torque control of six-phase induction motor with a novel mras-based stator resistance estimator,” IEEE Trans. Ind. Electron., vol. 65, no. 10, pp. 7685–7696, 2018.

[3] G. S. Buja and M. P. Kazmierkowski, “Direct torque control of pwm inverter-fed ac motors - a survey,” IEEE Trans. Ind. Electron., vol. 51, no. 4, pp. 744–757, 2004.

[4] Yen-Shin Lai and Jian-Ho Chen, “A new approach to direct torque control of induction motor drives for constant inverter switching frequency and torque ripple reduction,” IEEE Trans. Energy Convers., vol. 16, no. 3, pp. 220–227, 2001.

[5] R. Bojoi, F. Farina, G. Griva, F. Profumo, and A. Tencori, “Direct torque control for dual three-phase induction motor drives,” IEEE Trans. Ind. Appl., vol. 41, no. 6, pp. 1627–1636, 2005.

[6] D. Casadei, F. Profumo, G. Serra, and A. Tani, “Foc and dtc: two viable schemes for induction motors torque control,” IEEE Trans. Power Electron., vol. 17, no. 5, pp. 779–787, 2002.

[7] E. Levi, “Multiphase electric machines for variable-speed applications,” IEEE Trans. Ind. Electron., vol. 55, no. 5, pp. 1893–1909, 2008.

[8] A. S. Abdel-Khalik, R. A. Hamdy, A. M. Massoud, and S. Ahmed, “Post-fault control of scalar (v/f) controlled asymmetrical six-phase induction machines,” IEEE Access, vol. 6, pp. 59211–59220, 2018.

[9] M. H. Holakooie and G. Iwanski, “An adaptive identification of rotor time constant for speed-sensorless induction motor drives: A case study for six-phase induction machine,” IEEE Trans. Emerg. Sel. Topics Power Electron., vol. 1, pp. 1–1, 2020.

[10] M. H. Holakooie, M. Ojaghi, and A. Taheri, “Modified dtc of a six-phase induction motor with a second-order sliding-mode mras-based speed estimator,” IEEE Trans. Power Electron., vol. 34, no. 1, pp. 600–611, 2019.
[11] M. Slunjski, O. Dordevic, M. Jones, and E. Levi, “Symmetrical/asymmetrical winding reconfiguration in multiphase machines,” IEEE Access, vol. 8, pp. 12 835–12 844, 2020.

[12] M. Bermudez, I. Gonzalez-Prieto, F. Barrero, H. Guzman, X. Kestelyn, and M. J. Duran, “An experimental assessment of open-phase fault-tolerant virtual-vector-based direct torque control in five-phase induction motor drives,” IEEE Trans. Power Electron., vol. 33, no. 3, pp. 2774–2784, 2018.

[13] Y. Zhou, X. Lin, and M. Cheng, “A fault-tolerant direct torque control for six-phase permanent magnet synchronous motor with arbitrary two opened phases based on modified variables,” IEEE Trans. Energy Conv., vol. 31, no. 2, pp. 549–556, 2016.

[14] L. Zheng, J. E. Fletcher, B. W. Williams, and X. He, “A novel direct torque control scheme for a sensorless five-phase induction motor drive,” IEEE Trans. Ind. Electron., vol. 58, no. 2, pp. 503–513, 2011.

[15] Y. Ren and Z. Q. Zhu, “Enhancement of steady-state performance in direct-torque-controlled dual three-phase permanent-magnet synchronous machine drives with modified switching table,” IEEE Trans. Ind. Electron., vol. 62, no. 6, pp. 3338–3350, 2015.

[16] S. Payami and R. K. Behera, “An improved dtc technique for low-speed operation of a five-phase induction motor,” IEEE Trans. Ind. Electron., vol. 64, no. 5, pp. 3513–3523, 2017.

[17] J. Xu, M. Odavic, z. q. Zhu, Z. Wu, and N. Freire, “Switching-table-based direct-torque control of dual three-phase pmsms with closed-loop current harmonics compensation,” IEEE Trans. Power Electron., pp. 1–1, 2021.

[18] A. Gonzalez-Prieto, I. Gonzalez-Prieto, M. J. Duran, J. J. Aciego, and P. Salas-Biedma, “Current harmonic mitigation using a multi-vector solution for mpc in six-phase electric drives,” IEEE Access, vol. 9, pp. 117 761–117 771, 2021.

[19] L. Gao, J. E. Fletcher, and L. Zheng, “Low-speed control improvements for a two-level five-phase inverter-fed induction machine using classic direct torque control,” IEEE Trans. Ind. Electron., vol. 58, no. 7, pp. 2744–2754, 2011.

[20] Y. Ren and Z. Q. Zhu, “Reduction of both harmonic current and torque ripple for dual three-phase permanent-magnet synchronous machine using modified switching-table-based direct torque control,” IEEE Trans. Ind. Electron., vol. 62, no. 11, pp. 6671–6683, 2015.

[21] J. K. Pandit, M. V. Aware, R. V. Nemade, and E. Levi, “Direct torque control scheme for a six-phase induction motor with reduced torque ripple,” IEEE Trans. Power Electron., vol. 32, no. 9, pp. 7118–7129, 2017.

[22] Y. N. Tatte and M. V. Aware, “Torque ripple and harmonic current reduction in a three-level inverter-fed direct-torque-controlled five-phase induction motor,” IEEE Trans. Ind. Electron., vol. 64, no. 7, pp. 5265–5275, 2017.

[23] K. Hatua and V. T. Ranganathan, “Direct torque control schemes for split-phase induction machine,” IEEE Trans. Ind. Appl., vol. 41, no. 5, pp. 1243–1254, 2005.

[24] R. E. Kodumur Meesala and V. K. Thippiripati, “An improved direct torque control of three-level dual inverter fed open-ended winding induction motor drive based on modified look-up table,” IEEE Trans. Power Electron., vol. 35, no. 4, pp. 3906–3917, 2020.

[25] Y. Zhang and J. Zhu, “Direct torque control of permanent magnet synchronous motor with reduced torque ripple and commutation frequency,” IEEE Trans. Power Electron., vol. 26, no. 1, pp. 235–248, 2011.

[26] X. Wang, Z. Wang, and Z. Xu, “A hybrid direct torque control scheme for dual three-phase pmsm drives with improved operation performance,” IEEE Trans. Power Electron., vol. 34, no. 2, pp. 1622–1634, 2019.

[27] Yifan Zhao and T. A. Lipo, “Space vector pwm control of dual three-phase induction machine using vector space decomposition,” IEEE Trans. Ind. Appl., vol. 31, no. 5, pp. 1100–1109, 1995.

[28] M. Hinkkanen and J. Luomi, “Modified integrator for voltage model flux estimation of induction motors,” IEEE Trans. Ind. Electron., vol. 50, no. 4, pp. 818–820, 2003.

[29] C. Lascu and G.-D. Andreescu, “Sliding-mode observer and improved integrator with dc-offset compensation for flux estimation in sensorless-controlled induction motors,” IEEE Trans. Ind. Electron., vol. 53, no. 3, pp. 785–794, 2006.

[30] Y. Zhang and J. Zhu, “Direct torque control of permanent magnet synchronous motor with reduced torque ripple and commutation frequency,” IEEE Trans. Power Electron., vol. 26, no. 1, pp. 235–248, 2011.

[31] J. Beerten, J. Vervecken, and J. Driesen, “Predictive direct torque control for flux and torque ripple reduction,” IEEE Trans. Ind. Electron., vol. 57, no. 1, pp. 404–412, 2010.

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