Highly Selective Directional Atomic Layer Etching of Silicon

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Following Moore’s Law, feature dimensions will soon reach dimensions on an atomic scale. For the most advanced structures, conventional plasma etch processes are unable to meet the requirement of atomic scale fidelity. The breakthrough that is needed can be found in atomic layer etching or ALE, where greater control can be achieved by separating out the reaction steps. In this paper, we study selective, directional ALE of silicon using plasma assisted chlorine adsorption, specifically selectivities to bulk silicon oxide as well as thin gate oxide. Possible selectivity mechanisms will be discussed.

As the IC industry approaches sub 10 nm devices, the need for atomic scale etch fidelity has been recognized. In the field of deposition, atomic layer deposition (ALD) emerged. The driving forces for advancement of ALD were among others conformal deposition in high aspect ratio structures and deposition of dielectrics and metals with atomic layer control. The idea that an analogous technology for removal of material might exist was proposed over 10 years after the discovery of ALD. The number of publications on this so called atomic layer etch (ALE) increased significantly in recent years and now ALE is transitioning from the lab to the fab.

One highly desirable quality of ALE is selectivity. Recently, Hudson et al. verified that a directional oxide ALE process can etch SiO2 selective to SiNx. Ikeda et al. showed that thermal ALE of germanium can be selective to silicon or SiGe. Thermal etching is isotropic and not directional. Etching of 3D devices requires directionality and selectivity. FinFET gate etching for instance requires overetches of 40 nm and more to clear the silicon between the fins while gate oxide is exposed. As fin heights increase to achieve the required Ion currents while CD’s are shrinking further, the amount of overetch is expected to increase even more. During extended plasma exposure, species from the plasma can penetrate into the fin silicon and cause lattice damage and undesired fin recess. This drives the need for new etching approaches such as ALE.

ALE processes are comprised of single unit steps which repeat in cycles. These single unit steps use the simplest possible chemistry to realize specific surface processes such as activation and removal. In analogy to ALD, ALE single unit steps should have as much self-limitation as possible. Self-limitation or saturation eliminates the influence of transport phenomena which are the root cause of aspect ratio dependent etching or ARDE on a microscopic scale. On an atomic scale, saturation of the single unit steps should lead to atomic level smoothness of the etching surface.

Another important concept which can be adapted from ALD is the existence of an ideal process window. Figure 1a illustrates the so called “ideal ALD window,” which is defined as the region of nearly ideal ALD behavior between non-ideal regions. The graph shows “growth per cycle” or GPC as a function of surface temperature which for chemical surface reactions represents the available energy to overcome reaction barriers. The analogy of an ideal process window for ALE with ion based removal is shown in Fig. 1b. Here, “etch per cycle” or EPC is shown as a function of ion energy. The material to be etched is activated in a first step and the activated layer is removed in a second step by energetic ions. For instance, silicon can be activated by chlorine molecules or radicals and the resulting surface layer of SiClx can be removed by low energy noble gas ions. This particular embodiment of ALE is directional since the removal step is directional due to the use of ions that have been accelerated by a plasma sheath or ion beam source. There are other embodiments of ALE as well. For instance, in the absence of directionality in both, the activation and removal step, the result is isotropic ALE. In this case, surface temperature can be used as control variable of the removal step.

The region called “incomplete removal” in Figure 1b is characterized by ion energies that are insufficient to completely remove the activated surface layer. Under the conditions labeled “ideal ALE window,” the ion energy is chosen to be high enough to remove the activated layer but not the bulk silicon material. A third process regime is labeled “sputtering” and designates a region where the ion energy is high enough to remove bulk material.

The concept of an “ideal ALE window” can be extended to explain etch selectivity. In Fig. 2, material A exhibits an ALE window while material B does not. In the case of material B, the bonding energy of the adsorbed layer is significantly lower than for the bulk material. In this case, the adsorbed species would be removed as atomic species (EPC equals zero) and the removal of the bulk material realized only if the energy reaches the energy needed to sputter the bulk material. If this sputter threshold energy is higher than at least part of the energy range for ideal ALE of material A, high selectivities can be obtained.

Experimental

All experiments were conducted in a high volume production proven 2300 Kyjo plasma etch chamber with a transformer coupled plasma source. Single crystal silicon on oxide (SOI) and thermal silicon oxide wafers were used to collect the etch rates for various process conditions with high accuracy. For the SOI wafers, the silicon thickness was 88 nm and the thickness of the buried oxide layer was 140 nm. The resistivity of the silicon layer was 12.5 Ohm-cm. The thermal oxide was grown by a dry process at 950°C and had a thickness of 100 nm. EPC was measured via ellipsometry. In another set of experiments, samples of 120 nm thick undoped polysilicon on 2 nm gate oxide were etched with an oxide mask. The amount of silicon removal was measured by scanning electron microscopy (SEM) with a resolution of 300 k. The thickness and structure of the gate oxide was studied with transmission electron microscopy (TEM).

Results

Figure 3 shows EPC for single crystal silicon and thermal silicon oxide as a function of RF bias voltage. The chlorination step used a pressure of 60 mTorr without bias power and had a step time of 2 s. The source power was 900 W. The source power in the Ar removal step was 300 W, the pressure 5 mTorr and the step duration was...
Figure 1. a. Ideal process window for ALD adapted from Ref. 3 b. Ideal process window for direction ALE.

Figure 2. Schematic of EPC for material A (e.g. silicon) and material B (e.g., silicon oxide) as a function of ion energy. Hypothetically, infinite etch selectivity can be reached in the energy range that etches material A and not material B.

2.5 s. Under these conditions, the chlorination step contributes less than 10% to EPC. The contribution of the chlorination step can be further reduced to 3% when the chlorination step time is reduced to 0.5 s. As can be seen in Figure 3, silicon has an ALE process window between 40 and 60 volts of RF bias. This translates to 60 to 80 eV average ion energy based on our plasma modelling results. Park et al. reported a region of stabilized etch rates in ion beam experiment for acceleration voltages between 70 and 90 V or ion energies of 70 to 90 eV. The silicon surface was activated with chlorine gas.

The EPC for thermal silicon oxide is essentially zero for RF bias voltages of up to 50 V or ion energies of 70 eV. This result is in good agreement with sputter results for silicon oxide where sputter yields of 5E-2 at/ion at 40 eV and 4E-1 at/ion at 60 eV have been reported. Based on these results, silicon ALE can be achieved with high selectivities to thick oxide for ion energies up to 60 eV.

The selectivity benefit of ALE can be seen in Figure 4 where silicon to silicon oxide selectivity results are compared for ALE and continuous processing with a Cl2/Ar gas mixture. For ALE, no appreciable etch rate was measured for silicon oxide for RF bias voltages up to 40 V or about 60 eV ion energy. This region is labeled “infinite selectivity” in Figure 4. The onset of removal of silicon oxide for RF bias voltages around 40 V or about 60 eV is in good agreement with Figure 3. In contrast, the selectivity decreases immediately for continuous processing under similar conditions for bias voltages above 0 V.

Cl2/Ar ALE processing with 0 V RF bias or 20 eV ion energy was applied to overetch patterned polysilicon wafer with lines and spaces and oxide hardmask. After etching the structures with variable percentage overetch, the samples were treated for 60 s in diluted HF to remove the gate oxide and any damaged bulk silicon. No silicon recess was measured with TEM for overetch times corresponding to removal of 70 nm of silicon.

To study the quality of the gate oxide to silicon interface, TEM analysis was used. Figure 5 compares TEM pictures for a polysilicon / gate oxide structure before and after ALE with 30 nm overetch under further optimized process conditions to minimize silicon damage. In this experiment, Xe plasma without bias power was used in the removal step. The gate oxide between 40 nm gate lines is shown. No gate oxide loss and only slight if any damage of the bulk silicon underneath the gate oxide is visible. The fact that the darker regions
extend to a greater silicon depth than in the pre-etch TEM indicates that there is potentially some lattice damage.

Discussion

Under the conditions labeled “ideal ALE window” in Figure 1b, the ion energy is chosen to be high enough to remove the top chlorinated silicon layer but not the bulk silicon material. The role of chlorine is to weaken silicon-silicon bonds of the top silicon layer to the second silicon layer to make it more easily removable than bulk silicon. This implies that chlorine modifies the silicon surface by chemisorption. The Si-Cl bonding energy of 4.2 eV is indeed stronger than the Si-Si bond of 3.4 eV. Electron transfer by the strongly bound electronegative chlorine lowers the silicon-to-silicon binding energy underneath the SiCl layer further. This reduces the threshold energy for removing the SiCl layer with respect to bulk silicon and ALE conditions are obtained.

The primary ALE selectivity mechanism is based on differences of the binding energies between the participating elements. The bond energy of Si-O is about 6.4 eV vs. 4.2 eV for Si-Cl. This means, substitution of O with Cl atoms is unfavorable from a thermodynamics point of view. While Oostra et al. have shown that Cl2 can dissociatively chemisorb onto a SiO2 surface, the formation of these bonds does not weaken the bond energy of Si-Cl in the subsurface layers enough to allow for removal of Si-Cl directly from a chlorinated SiO2 surface. This is supported by reports of measurable SiO2 sputter yields for Ar ion energies above 40 eV. This is comparable with the data in Figure 3 which show that SiO2 etches with an Ar/Cl2 ALE process for RF bias voltages above 40 V or Ar ion energies above 60 eV. From this, we conclude that the primary mechanism for etching SiO2 for the Cl2/Ar ALE process is sputtering.

The Si damage results in Figure 5 compare very favorably to published results for processes in continuous mode. Vitale and Smith reported a gate oxide loss of 4 nm for a HBr/O2 process. The root cause for this large loss is oxygen implantation through the gate oxide into the interface layer due to the ion energies used in continuous processing. In case of ALE, this silicon damage or recess mechanism is absent.

We observed some silicon recess for longer overetch times corresponding to the removal of more than 70 nm of silicon and attribute this finding to secondary mechanisms. The sputter yields reported for very low Ar ion energies are in good agreement with the assumption that oxygen is preferentially ejected and that silicon limits the sputtering process. Conceivably, the ALE process removes some of the silicon rich surface layer which forms during Ar ion bombardment and eventually the gate oxide layer will be thinned to a critical thickness. Petit-Etienne et al. reported that for chlorine plasma with 100 eV ion energy, Cl penetrates through 2.5 nm thick SiO2 and accumulates as SiCl4 at the interface causing silicon recess and accelerated gate oxide breakthrough. In our experiment, the ion energies during the chlorine activation step were much lower as no RF bias was applied.

It is possible, that a chlorine penetration/accumulation mechanism plays a role during the final stages when the gate oxide is sufficiently thin. Then, silicon recess could be observed post HF clean without complete breakthrough.

Conclusions

The concept of an ideal ALE process window can be adapted from ALD and extended to explain etch selectivity. In this paper, we have reported infinite selectivities of silicon to bulk thermal silicon oxide for a Cl2/Ar ALE process with plasma adsorption. Excellent gate oxide integrity and no silicon recess has been demonstrated for extended overetch times. Selectivity mechanisms based on differences of the binding energies between the participating elements have been evolved for this type of ALE process to explain the findings. Eventually, gate oxide integrity will be compromised due to secondary processes such as preferential sputtering of oxygen and ALE removal of silicon atoms. The experimental results showed that for a 2 nm gate oxide and Ar ion energies of 20 eV, measurable gate oxide recess started after a time equivalent to the removal of 70 nm polysilicon.

Acknowledgments

The authors thank Theo Panagopoulos for the plasma modelling results.

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