A Fully Integrated Clocked AC-DC Charge Pump for Mignetostrictive Vibration Energy Harvesting

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Received: 26 November 2020; Accepted: 17 December 2020; Published: 18 December 2020

Abstract: This paper describes a clocked AC-DC charge pump to enable full integration of power converters into a sensor or radio frequency (RF) chip even with low open circuit voltage magnetostrictive vibration energy transducer operating at a low resonant frequency of 10 Hz to 1 kHz. The frequency of the clock to drive an AC-DC charge pump was up-converted with an on-chip oscillator to increase output power of the charge pump without significantly increasing the circuit area. A model of the system including the charge pump and vibration energy transducer is shown. It was validated by HSPICE simulation and measured, resulting in a prototype chip with an area of 0.11 mm² fabricated in a 65 nm 1 V CMOS process. The fabricated charge pump was also measured together with a magnetostrictive transducer. The charge pump converted the power from the transducer to an output power of 4.2 µW at an output voltage of 2.0 V. The output power varied below 3% over a wide input frequency of 10 Hz to 100 kHz, which suggests that universal design of the clocked AC-DC charge pump can be used for transducers with different resonant frequencies. In a low-input voltage region below 0.8 V, the proposed circuit has higher output power compared with the conventional circuits.

Keywords: AC-DC; IoT; charge pump; energy harvesting; vibration; magnetostrictive

1. Introduction

In recent years, the Internet of things (IoT), in which information possessed by various machines and humans is collected by sensors and shared among objects via the Internet, has attracted attention. Since the IoT requires a lot of sensors, it is desirable for the edge devices to be battery-less in order to reduce maintenance costs. Thus, energy harvesting (EH) obtaining power from surrounding environmental energy is expected to become a power source for IoT sensor devices [1,2]. Vibration energy transducer (ET) converts vibration energy into AC electric power. Table 1 compares three different types in terms of physical characteristics: piezoelectric [3], electrostatic [4], and magnetostrictive [5]. The piezoelectric effect is a phenomenon in which a voltage proportional to the pressure applied to a material is generated. The AC power is extracted by applying vibration to the piezoelectric element. Since a voltage amplitude of 1 V or greater can be obtained, an AC-DC voltage down converter provides DC power to the sensor integrated circuit (IC). In the electrostatic induction power generation, the electrode plate of the capacitor charged by the electret is moved by vibration, and thus an AC power is generated. The output impedance of the generating element is very high, and the output voltage amplitude can be higher than 10 V. It requires high voltage rectifiers followed by a buck converter with many external components [6]. Magnetostrictive power is generated on the basis of the reverse magnetostrictive effect [5]. A high current can be obtained due to the low internal resistance. The amount of power generated per volume is larger than that of the other methods, as shown in Table 1.
When the number of stage is 9 and the AC frequency is 1 kHz. Such a design solution would be practically feasible as a clock, as shown in Figure 1. Input AC voltage is also transferred from one capacitor to the next by inputting a clock signal. Input AC voltage is also treated as a clock, as shown in Figure 1. According to Reference [8], four discrete germanium Schottky barrier diodes and three chip capacitors with 1 µF each were built. AC-DC CPs have been integrated in RFID at HF or RF bands, as discussed in [12, 13]. Conversely, AC-DC CPs have never been integrated in a chip for vEH because of its low frequency. When the capacitance per stage is increased, the amount of charge that can be charged and discharged at one time increases, and thus I\text{OUT} increases even at a low frequency. Figure 2 shows a simulated relationship between C of AC-DC CP and output power P\text{OUT}.

Accordingly, as the frequency of the AC input voltage increases, the output current of CP (I\text{OUT}) increases. In Reference [8], four discrete germanium Schottky barrier diodes and three chip capacitors with 1 µF each were built. AC-DC CPs have been integrated in RFID at HF or RF bands, as discussed in [12, 13]. Conversely, AC-DC CPs have never been integrated in a chip for vEH because of its low frequency. When the capacitance per stage C is increased, the amount of charge that can be charged and discharged at one time increases, and thus I\text{OUT} increases even at a low frequency. Figure 2 shows a simulated relationship between C of AC-DC CP and output power P\text{OUT}.

Let us assume the power supply of the sensor requires 2 V and at least 1 µW at 2 V. When the input voltage amplitude V\text{DD} = 0.5 V and V\text{OUT} = 2 V, C of 700 pF is required to obtain P\text{OUT} of 1 µW. If the AC-DC CP is integrated using metal-insulator-metal (MIM) capacitors with capacitance density of 2 fF/µm², the circuit area would be as large as 3 mm², and P\text{OUT} per area is 0.3 µW/mm² when the number of stage is 9 and the AC frequency is 1 kHz. Such a design solution would be practically impossible for low-cost small form factor IoT edge devices. To solve the problem, AC-DC-DC

| Characteristics of vibration energy transducer. | Piezoelectric [3] | Electrostatic [4] | Magnetostrictive [5] |
|-----------------------------------------------|------------------|------------------|-------------------|
| Nominal output impedance                      | 100 kΩ–1 MΩ      | 100 MΩ–1 GΩ      | 100 Ω–1 kΩ       |
| Nominal output voltage                         | 1 V–10 V         | 10 V–100 V       | 0.1 V–1 V        |
| Output power (mW/cm³)                          | 0.74–3 [7]       | 0.08–0.6 [7]    | 20 [5]          |

![Figure 1. AC-DC charge pump (CP) [8].](image1)

![Figure 2. Simulated P\text{OUT} as a function of C (AC-DC CP, V\text{DD} = 0.5 V, V\text{OUT} = 2 V, N = 9, f\text{IN} = 1 kHz).](image2)

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conversion has been proposed and developed [9,10], which includes AC-DC conversion followed by DC-DC conversion using a CP (see Figure 3).

A rectifying device and an external capacitor are used for AC-DC conversion. Figure 4 shows rectifying devices for AC-DC conversion used in the AC-DC-DC converters.

In References [9,10], AC-DC conversion is performed by an active diode using an operational amplifier, as shown in Figure 4b. DC-DC CP was optimally designed to maximize the output power of the transducer. This solution requires a discrete capacitor \( C_{REC} \) to filter out AC components. In Reference [10], the AC-DC-DC circuit was designed in 0.35 \( \mu \)m complementary metal-oxide-semiconductor (CMOS) process technology. With active diodes, the circuit operated even at an input voltage of 0.5 V. In Reference [11], a switching regulator was designed to have a high output power of 1 mW with a power efficiency of 76%. However, it was not fully integrated due to the use of external capacitors and coils. Therefore, the clocked AC-DC CP was proposed in [14]. It can operate with a variety of transducers whose resonant frequencies can be in a wide range of 10 Hz to 100 kHz without any external components for low cost. Initial measurement results are shown in [15].

In this extended version of the paper, circuit modeling of the system including vibration ET and a clocked AC-DC CP is presented. Analysis of the input power to the charge pump and characteristics of the magnetostrictive ET are also discussed. Detailed measurement results and the comparison with the other systems are shown as well. Section 2 models the proposed circuit and entire system. Section 3 compares measurement results of the proposed circuit with the results of the formulas derived in Section 2 and simulation results. The proposed circuit was also measured with a magnetostrictive vibration ET. In Section 4, the proposed circuit is compared with the existing boosting circuits for vEH. Section 5 describes the future works of the proposed circuit. Section 6 summarizes this work.

2. Clocked AC-DC Charge Pump

2.1. A Modeling of the Intrinsic Part of the System

Figure 5 shows the clock waveforms used in the clocked AC-DC CP.
A sine wave is rectified and is modulated by a high frequency rectangular wave. As described in the Introduction, since the frequency of the AC voltage obtained from the transducer, $f_{IN}$, is about 10 Hz to 1 kHz, sufficient output power could not be obtained without using external devices. However, the clock frequency $f_{CLK}$ of the clocked AC-DC CP is made much higher than $f_{IN}$. As long as the clock period is longer than RC time constant of switching diodes, the output current of CP is proportional to the clock frequency. Therefore, since the CP can operate at a high frequency, it is possible to obtain a sufficient output current even with a small sized capacitor to allow full integration. Furthermore, a discrete capacitor for smoothing the input voltage is not required. In this section, the equation for obtaining the input and output currents of the proposed circuit is modeled.

Figure 6 shows the waveforms of voltage and current in the proposed circuit. The input voltage is a sine wave with an amplitude of $I_{in}$. $\theta_s$ is defined by the phase in which an average output current at $\theta$, $I_{OUT}(\theta)$, starts to flow. $I_{OUT}(\theta)$ varies in amplitude according to the clock amplitude. Assuming that $f_{CLK}$ is much higher than $f_{IN}$, the amplitudes at the rising and falling edges can be considered to be the same. Therefore, $I_{OUT}(\theta)$ is obtained by applying the $I_{OUT}V_{OUT}$ equation of the DC-DC charge pump [16].

$$I_{OUT}(\theta) = \frac{1}{R_{TOT}} \left\{ \left( \frac{N}{1 + \beta} + 1 \right) V_{DD} \sin \theta - (N + 1) V_{TH}^E - V_{OUT} \right\}$$  \hspace{1cm} (1)$$

where $N$ is the number of capacitors, $\beta$ is the ratio of the parasitic capacitance to the pump capacitor $C$, $V_{TH}^E$ is the effective threshold voltage of the diode given by Equation (2) [16], and $R_{TOT}$ is the output impedance of the entire system including ET and CP given by Equation (3) [17].

$$V_{TH}^E = V_T \ln \left( \frac{4 \sqrt{\pi} (1 + \beta) f_{CLK} C V_T}{I_s} \right)$$  \hspace{1cm} (2)$$

$$R_{TOT} = \frac{N}{(1 + \beta) C f_{CLK}} + (N + 1)^2 R_{EH}$$  \hspace{1cm} (3)$$

where $I_s$ is the saturation current of each diode and $V_T$ is the thermal voltage.
When $I_{OUT} (\theta)$ becomes zero at $\theta = \theta_S$, $\theta_S$ can be given by Equation (4).

$$\theta_S = \sin^{-1} \left( \frac{1 + \beta}{V_{DD}(1 + \beta + N)} \left[ V_{OUT} + (N + 1)V_{TH}^{EFF} \right] \right) \quad (4)$$

Figure 7 shows an equivalent circuit for a converter system composed of a clocked AC-DC CP and transducer under the slow switching limit where $I_{OUT}$ is proportional to $f_{CLK}$. $R_{EH}$ and $R_{PMP}$, which are the output impedance of energy transducer, that of CP, and that of entire system including the energy transducer, respectively [17].

Figure 7. Equivalent circuit for the system including AC energy transducer and CP based on [15] for DC energy transducer. (a) can be transformed into (b).

Let us introduce $k$, which meets $\theta = \theta_S + k\pi f_{IN} / f_{CLK}$. One can write down an average output current in the $k$-th pulse, $I_{OUT}^k$, as

$$I_{OUT}^k = \frac{1}{R_{PMP}} \left( \left( \frac{N}{1 + \beta} + 1 \right)V_{DD} \sin \left( \theta_S + k\pi \frac{2f_{IN}}{f_{CLK}} \right) - (N + 1)V_{TH}^{EFF} - V_{OUT} \right) \quad (5)$$
on the basis of Figure 7. The average output current $\overline{I_{OUT}}$ for one input cycle is obtained from Equation (6),

$$\overline{I_{OUT}} = \frac{2}{\pi} \sum_{k=1}^{n} I_{OUT}^k \quad (6)$$

where $n$ is the number to meet $\pi / 2 = \theta_S + n\pi f_{IN} / f_{CLK}$, where $I_{OUT}^n$ becomes the largest at $\theta = \pi / 2$. $\sum_{k=0}^{n} \sin(\theta + \phi)$ can be calculated by Equation (7).

$$\sum_{k=0}^{n} \sin(\theta + \phi) = \frac{\sin \left( \frac{n+1}{2} \phi \right) \sin \left( \frac{n+3}{2} \phi \right)}{\phi} \quad (7)$$

Equation (6) can be simplified with Equation (7) as Equation (8).

$$\overline{I_{OUT}} = \frac{2}{\pi} \times \frac{1}{R_{TOT}} \left( \left( \frac{N}{1 + \beta} + 1 \right)V_{DD} \cos \theta_S - \left( \frac{\pi}{2} - \theta_S \right) \right) \left( (N + 1)V_{TH}^{EFF} + V_{OUT} \right) \quad (8)$$
One can estimate an average output current per cycle $I_{\text{OUT}}$ using Equations (2) and (8) under a specific condition of $V_{\text{DD}}, V_{\text{OUT}}, f_{\text{CLK}}, N, C, \beta, I_S$, and $V_T$.

Next, the input current $I_{CP}$ and the input power $P_{CP}$ are modeled. An equation for the input current of the DC-DC CP was obtained in [18]. By applying it to the proposed circuit, Equation (9) is obtained.

$$I_{CP}(\theta) = \left(\frac{N}{1 + \beta} + 1\right)I_{\text{OUT}}(\theta) + \left(\frac{\beta}{1 + \beta}\right)f_{\text{CLK}}NCV_{\text{DD}}\sin \theta$$

(9)

An average input current over one input cycle, $I_{\text{CP}}$, can be given by integrating Equation (9) from $\theta_S$ to $\pi/2$, resulting in Equation (10).

$$I_{\text{CP}} = \left(\frac{N}{1 + \beta} + 1\right)I_{\text{OUT}} + \frac{2}{\pi}\left(\frac{\beta}{1 + \beta}\right)f_{\text{CLK}}NCV_{\text{DD}}\cos \theta_S$$

(10)

Similarly, an average input power $P_{CP}$, can be calculated as Equation (11).

$$P_{CP} = \frac{2}{\pi} \times \int_{0}^{\pi/2} I_{CP}(\theta)V_{\text{DD}}\sin \theta d\theta = \frac{2}{\pi} \left[ \frac{1}{4}\left(\frac{1}{I_{\text{OUT}}}+1\right)\right] V_{\text{DD}}^2 \left(\frac{N}{2\beta} + \frac{1}{N}\right) + \frac{\beta}{1 + \beta}\right)f_{\text{CLK}}NCV_{\text{DD}}^2 \sin^2 \theta_S -$$

$$\left(\frac{N}{1 + \beta} + 1\right)V_{\text{DD}}\left(\frac{N}{2\beta} + \frac{1}{N}\right)V_{\text{EFF}} + V_{\text{OUT}}\cos \theta_S \right) + \frac{1}{4}\left(\frac{\beta}{1 + \beta}\right)f_{\text{CLK}}NCV_{\text{DD}}^2 \sin^2 \theta_S$$

(11)

Since $V_{\text{OUT}}$ is a DC voltage, the output power $P_{\text{OUT}}$ of the proposed circuit is determined by the product of $I_{\text{OUT}}$ and $V_{\text{OUT}}$.

$$P_{\text{OUT}} = V_{\text{OUT}} \times I_{\text{OUT}}$$

(12)

These equations are verified in Section 3.

2.2. Modeling of Additional Loss Components

The entire system for the proposed circuit is shown in Figure 8. A cross-coupled CMOS bridge circuit [19] is used for a full-wave bridge rectifier (FBR) to rectify the input voltage. A current-controlled ring oscillator (ROSC) is used to generate a clock waveform. $f_{\text{CLK}}$ is proportional to a branch current $I_{\text{OSC}}$ driving the inverter. The circuit is designed so that the value of $I_{\text{OSC}}$ can be changed by externally applying the DC voltage $V_{\text{CTRL}}$. Therefore, it is possible to vary $f_{\text{CLK}}$ by varying $V_{\text{CTRL}}$. For practical use, ROSC must be designed to have an optimum $f_{\text{CLK}}$ for each specification without any external control such as $V_{\text{CTRL}}$. Diode-connected CMOS transistors [20] are used for the diode portion of CP. This configuration has the advantage of significantly reducing the reverse leakage current when reverse biased compared to conventional diode connections. Since the voltage of the CP diode is applied in the forward direction and the reverse direction every half cycle of the clock signal, reduction in the reverse current contributes to increasing the power efficiency of the CP [21].

Figure 8. System diagram of the clocked AC-DC CP.
An average power of ROSC is given by Equation (13).

\[
P_{OSC} = \frac{2}{\pi} \int_0^\pi (V_{DD}\sin \theta \times 2N_{OSC}f_{CLK}C_{INV}V_{DD}\sin \theta)d\theta
\]

\[
= N_{OSC}f_{CLK}C_{INV}V_{DD}^2
\]

where \(N_{OSC}\) is the number of stages of ROSC and \(C_{INV}\) is the gate capacitance of each stage.

Considering a power loss \(P_{OFF}\) due to the off-leak current of the NMOS and PMOS in FBR, the input power of the entire system, \(P_{TOTAL}\), is obtained by summing Equations (11) and (13), and the power loss \(P_{OFF}\).

\[
P_{TOTAL} = P_{CP} + P_{OSC} + P_{OFF}
\]

The power efficiency of the entire system \(\eta_{TOT}\) is obtained by Equation (15) together with Equations (11)–(14).

\[
\eta_{TOT} = \frac{P_{OUT}}{P_{TOTAL}}
\]

A maximum available power of transducer, \(P_{EH}\), can be realized under power matching.

\[
P_{EH} = \frac{V_{DD}^2}{8R_{EH}}
\]

The power efficiency \(\eta_{SYS}\) of the proposed circuit in this work is defined by Equation (17):

\[
\eta_{SYS} = \frac{P_{OUT}}{P_{EH}}
\]

The values obtained from the above equations and the simulation values are compared with the measurement results in Section 3.

3. Validation

3.1. Validation with AC Power Source

The proposed circuit system was fabricated in 65 nm 1 V CMOS, as shown in Figure 9. Because the circuit operates at 1–10 MHz, 65 nm CMOS is not mandatory. One can design the circuit with less advanced technology such as 180 nm or 250 nm without significant performance degradation as far as low-Vt transistors are available. In order to achieve \(I_{OUT} > 1 \mu A\) at \(V_{DD} = 0.5\) V and \(V_{OUT} = 2\) V, we determined \(N\) and \(C\) to be 9 and 10 pF, respectively. The number of inverters in ROSC, \(N_{OSC}\), was 17. In this experiment, the energy transducer was replaced with an AC voltage source with an amplitude of 0.5 V and an impedance of \(R_{EH} = 500\) Ω. The output terminal was connected with an external resistor \(R_{OUT}\) and a capacitor \(C_{OUT}\). \(C_{OUT}\) smooths \(V_{OUT}\) to DC and \(R_{OUT}\) controls \(V_{OUT}\).

Figure 9 shows a chip micrograph. The total area of the whole circuit is about 0.11 mm\(^2\). This size is small enough to fit in sensor ICs. The measured waveforms are shown in Figure 11, where \(R_{OUT}\) and
$C_{\text{OUT}}$ were 1 MΩ and 300 nF, respectively. $V_1$–$V_2$ is the input differential voltage to the circuit. $V_{\text{REC}}$ is the supply voltage of CP and ROSC. Figure 11b shows focused clock waveform. Figure 11c shows the input and output voltages. The input voltage amplitude was 0.5 V while the output voltage $V_{\text{OUT}}$ was about 2 V, indicating that the designed CP was functional as expected. $P_{\text{OUT}}$ was about 4 $\mu$W.

$I_{\text{OUT}}$ was measured with $f_{\text{CLK}}$ and varied from 1 MHz up to about 5 MHz for a fabricated circuit and from 300 kHz up to about 8 MHz for a simulated one under $V_{\text{DD}} = 0.5$ V, $V_{\text{OUT}} = 2$ V, and $f_{\text{IN}} = 1$ kHz, as shown in Figure 12. The simulated and calculated values agreed within an error rate of 5% for $f_{\text{clk}} \leq 1$ MHz. As shown in Figure 11b, actual clock waveform had finite rise and fall times, which were ignored in the model equations. Therefore, the actual critical frequency to maximize $I_{\text{OUT}}$ was lower than that with the model. As a result, the error increased at higher frequencies. The frequency was saturated in the region of $f_{\text{CLK}} \geq 5$ MHz.

![Figure 10. Die photo of the proposed system.](image)

![Figure 11. Measured waveforms (a) $V_1$–$V_2$, $V_{\text{REC}}$ and CLK, (b) CLK and $V_{\text{REC}}$, (c) $V_1$–$V_2$ and $V_{\text{OUT}}$.](image)

![Figure 12. $I_{\text{OUT}}$ as a function of $f_{\text{CLK}}$ ($V_{\text{DD}} = 0.5$ V, $V_{\text{OUT}} = 2$ V, $f_{\text{IN}} = 1$ kHz).](image)
Figure 13 shows $P_{TOT}$ across $f_{CLK}$ on the basis of the model (Equation (14)), measured (MEAS), and simulation (HSPICE). The error rate between the model (Equation (14)) and the simulation value was about 3–30%, and the error rate between the measured value and Equation (14) was about 5–15%. $P_{TOT}$ also increased as $f_{CLK}$. Figure 13 includes each contributor to Equation (14): $P_{CP}$, $P_{OSC}$, and $P_{OFF}$ as well. $P_{OFF}$ became dominant at $f_{CLK} < 500$ kHz in this design. Such a corner frequency strongly depends on Vt of the switching transistors. As Vt decreased, both $P_{OFF}$ and $P_{OUT}$ and thereby $P_{IN}$ increased. The calculation result shows that $I_{OUT}$ started to decrease at $f_{CLK} = 6$ MHz. Since there was a power loss $P_{OFF} = 2.85$ $\mu$W independent of $f_{CLK}$, $P_{TOT}$ in the low frequency region converged to 2.85 $\mu$W.

![Figure 13. $P_{TOT}$ as a function of $f_{CLK}$ ($V_{DD} = 0.5$ V, $V_{OUT} = 2$ V, $f_{IN} = 1$ kHz).](image)

Figure 14 shows $\eta_{TOT}$ across $f_{CLK}$. Since $I_{OUT}$ of the measured values was lower than the simulation values in the range of $f_{CLK} < 4$ MHz, the measured values of $\eta_{TOT}$ within the same range were also lower. The efficiency of the measured values was about 23% at the maximum. Compared with the conventional system shown in Figure 1, the power for ROSC was required, and thus the power efficiency was reduced compared with the conventional circuit. Figure 15 shows the relationship between $I_{OUT}$ and $V_{OUT}$ for $V_{DD}$ of 0.4–1.0 V. ROSC was not able to run at $f_{CLK}$ of 5 MHz when $V_{DD} = 0.3$ V. Because the maximum attainable voltage increased as $V_{DD}$, $I_{OUT}$ increased as $V_{DD}$. $P_{OUT}$ reached 30 $\mu$W at $V_{DD} = 1$ V and $V_{OUT} = 3$ V, for example. Figure 16a,b show $I_{OUT}$ across $V_{DD}$ and $\eta_{SYS}$ across $P_{EH}$ when $V_{OUT} = 2$ V and $f_{CLK} = 5$ MHz, respectively.

![Figure 14. $\eta_{TOT}$ as a function of $f_{CLK}$ ($V_{DD} = 0.5$ V, $V_{OUT} = 2$ V, $f_{IN} = 1$ kHz).](image)
was theoretically expected to be robust against variation in frequency at Ueno lab [5], as shown in Figure 18a. The size of the transducer is about 3.5 cm × 1 cm × 1 cm.

Figure 17 suggests that the proposed circuit has the advantage that even if the frequency of vibration varies by 3% over such a wide frequency range. Since the conventional circuit shown in Figure 1 operates on the basis of only varied by 3% over such a wide frequency range. Since the conventional circuit shown in Figure 1 operates on the basis of \( f_{IN} \) for theoretical verification. Therefore, it is necessary to adjust the circuit parameters depending on the vibration frequency. On the other hand, the proposed circuit was theoretically expected to be robust against variation in \( f_{IN} \), as shown by Equations (8) and (14). Figure 17 shows that the proposed circuit has the advantage that even if the frequency of vibration changes with a different energy transducer, the common circuit design can be used, which contributes to cost reduction.

\[
\begin{align*}
\text{Input Voltage } V_{DD} & \text{[V]} \\
0 & 0.2 \ 0.4 \ 0.6 \ 0.8 \ 1 \ 1.2 \\
\text{Output Current } I_{OUT} & \text{[μA]} \\
0 & 2 \ 4 \ 6 \ 8 \ 10 \ 12 \ 14 \ 16
\end{align*}
\]

Figure 16. (a) \( I_{OUT} – V_{DD} \), (b) \( \eta_{SYS} – P_{EH} \) \( f_{IN} = 1 \text{ kHz}, f_{CLK} = 5 \text{ MHz}, V_{OUT} = 2 \text{ V} \).

Figure 17 shows the measured results of \( f_{IN} – I_{OUT} \). The actual frequency of the vibration was about 10 Hz –1000 Hz, but it was changed from 10 Hz to 100 kHz for theoretical verification. \( I_{OUT} \) only varied by 3% over such a wide frequency range. Since the conventional circuit shown in Figure 1 operates on the basis of \( f_{IN} \), a change in \( f_{IN} \) greatly affects \( I_{OUT} \). Therefore, it is necessary to adjust the circuit parameters depending on the vibration frequency. On the other hand, the proposed circuit was theoretically expected to be robust against variation in \( f_{IN} \), as shown by Equations (8) and (14). Figure 17 suggests that the proposed circuit has the advantage that even if the frequency of vibration changes with a different energy transducer, the common circuit design can be used, which contributes to cost reduction.

\[
\begin{align*}
\text{Input Frequency } f_{IN} & \text{[Hz]} \\
0 & 10^2 \ 10^3 \ 10^4 \ 10^5 \\
\text{Output Current } I_{OUT} & \text{[μA]} \\
0 & 0.5 \ 1 \ 1.5 \ 2 \ 2.5
\end{align*}
\]

Figure 17. Measured \( I_{OUT} \) as a function of \( f_{IN} \) \( \text{V}_{DD} = 0.5 \text{ V}, V_{OUT} = 2 \text{ V}, f_{CLK} = 5 \text{ MHz} \).

3.2. Validation with Magnetostrictive Energy Transducer

The fabricated circuit was validated with magnetostrictive energy transducer, which was developed at Ueno lab [5], as shown in Figure 18a. The size of the transducer is about 3.5 cm × 1 cm × 1 cm.
To extract $f_{IN}$ and $R_{EH}$, we directly connected the energy transducer with $R_L$. The acceleration and frequency of the accelerator were controlled by a controller. Figure 18b shows a block diagram of the measurement system. Vibration was applied to the energy transducer to generate an AC voltage across the load resistor $R_L$.

As shown in Figure 19, the resonant frequency was determined to be 195 Hz. In the subsequent verification, $f_{IN}$ was fixed at 195 Hz. Figure 20 shows $V_{DD}$ across vibration acceleration $\alpha$ when $R_L = \infty$. It can be confirmed that $V_{DD}$ was proportional to $\alpha$. Figure 21a,b show, respectively, the output voltage when $\alpha = 0.28$ G (a) and 0.5 G (b). The data indicate that the effective output resistance of the transducer was about 1 kΩ. The measured waveform validated the assumption that the magnetostrictive energy transducer can be modeled by the AC voltage source and the output impedance, as shown in Figure 3, as long as the load resistance $R_L$ is relatively high. Accordingly, as the output power increased, there could be significant interaction between the mechanical and electrical characteristics, as described in [22]. In such a case, the model of the transducer would need to be modified.

![Figure 18](image1.png)

**Figure 18.** Measurement set-up: photograph (a) and block diagram (b).

![Figure 19](image2.png)

**Figure 19.** Measured $V_{DD}$ as a function of $\alpha$ ($R_L = \infty$, $f_{IN} = 195$ Hz).

![Figure 20](image3.png)

**Figure 20.** Measured $V_{DD}$ as a function of $\alpha$ ($R_L = \infty$, $f_{IN} = 195$ Hz).
I
and GND to limit
f
impedance, as shown in Figure 3, as long as the load resistance
magnetostrictive energy transducer can be modeled by the AC voltage source and the output
controlled to be below 0.7 G. For production, a clamping circuit must be placed between
verification,
It can be confirmed that
approximately 11–16%. The error rate between the simulation result and the measurement was 2–9%.

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Figure 21. Output voltage of power generating element (f
IN
 = 195 Hz): (a) α = 0.28 G, (b) α = 0.5 G.

Figure 22 shows f
CLK
-I
OUT
 in terms of α = 0.28 G and α = 0.5 G. The solid and triangular
plots show the results of Equation (8) and the simulation values when R
EH
 = 1 kΩ, respectively. For both Figure 21a,b, the error rate between the model at f
CLK
 ≤ 2 MHz and the measurement was
approximately 11–16%. The error rate between the simulation result and the measurement was 2–9%.
It is confirmed that the fabricated clocked AC-DC CP can output power of 1 μW at 2 V with α = 0.28 G
at f
CLK
 ≥ 1 MHz. Figures 23 and 24 show the input voltage amplitude of CP and I
OUT
 when α was
changed. Measurement was performed with f
CLK
 = 5.0 MHz and V
OUT
 = 2 V. In this experiment, a
1 V CMOS transistor was used. Therefore, V
DD
 must be limited up to 1 V. As shown in Figure 23, α
was controlled to be below 0.7 G. For production, a clamping circuit must be placed between V
REC
 and GND to limit V
REC
. Although V
DD
 was about 0.4 V when α = 0.2 G, it was confirmed that the
proposed circuit operated to obtain power of 2 μW–30 μW in the range of α = 0.2 G to 0.7 G.

Figure 22. I
OUT
 as a function of f
CLK
 (V
OUT
 = 2 V, f
IN
 = 195 Hz): (a) α = 2.7 m/s², (b) α = 4.9 m/s².

Figure 23. Measured V
DD
 as a function of α (V
OUT
 = 2 V, f
IN
 = 195 Hz, f
CLK
 = 5 MHz).
Therefore, the proposed circuit can have a higher power factor than the AC-DC CP.

4. Comparison with Other Designs

This section compares the proposed circuit with the voltage boosting circuits for vEH that has been reported in past research.

4.1. AC-DC CP

As shown in Figure 2, when the AC-DC CP is used for vEH, C must be increased to compensate for low vibration frequency. An AC-DC CP with \( N = 9 \) and \( C = 10 \) pF was also fabricated together with the clocked AC-DC CP. Figure 25 shows \( V_{\text{OUT}}-I_{\text{OUT}} \) when the AC-DC CP was operated under the condition of \( f_{\text{IN}} = 1 \) kHz and \( V_{\text{DD}} = 0.5 \) V. Both the simulation and the measurement results showed that only \( I_{\text{OUT}} \) at an order of nA could be obtained. \( V_{\text{OUT}} \) was 0.2 V–0.3 V, even with \( V_{\text{DD}} = 0.5 \) V, due to the reverse leakage current being larger than the forward current. In order to obtain \( P_{\text{OUT}} = 4 \) μW with AC-DC CP, it is necessary to set \( C = 3 \) nF (see Figure 3). Therefore, the total capacitance of \( 3 \times 9 = 27 \) nF is required. Since the capacitor has capacitance of \( 2 \, \text{fF/μm}^2 \), an area of 27 nF was estimated to be 14 mm\(^2\). It is too large to implement the AC-DC CP in an IC. Therefore, the pump capacitors must be composed of discrete elements. On the other hand, the proposed circuit can be integrated in a small area of 0.11 μm\(^2\), as shown in Figure 10.

A comparison of the power distribution between the AC-DC CP and the proposed circuit was estimated for \( P_{\text{OUT}} \) of 4 μW, as shown in Figure 26. \( P_{\text{EH}} \) was calculated from Equation (16). \( P_{\text{RE}} \) is reactive power and \( P_{\text{LOSS}} \) is the power consumed by the CP. Compared with the AC-DC CP, the proposed circuit requires more power for OSC. In addition, the power loss due to the parasitic elements increased due to higher clock frequency. However, all the additional power is converted from \( P_{\text{RE}} \). Therefore, the proposed circuit can have a higher power factor than the AC-DC CP.
Even though $P_{OUT}$ increases with the proposed clocked AC-DC CP, there should be room to increase more because the impedance at the interface between EH and CP is significantly mismatched in the current design. The input impedance of CP was estimated to be about 4 kΩ, whereas the output impedance of transducer was 500 Ω. Design optimization would be needed in a future work.

4.2. AC-DC-DC CP

Figure 3 shows an AC-DC-DC CP. AC-DC-DC CP smooths the AC voltage output from the energy transducer to DC, and then boosts the input DC voltage to a higher DC voltage by CP. AC-DC conversion can be performed by an NMOS diode, as shown in Figure 4a. Figure 27 shows the simulation results of $V_{OUT}$-$I_{OUT}$ for the proposed circuit and AC-DC-DC CP with the same parameters as $N = 9$, $C = 10 \text{ pF}$, $f_{IN} = 1 \text{ kHz}$, $f_{CLK} = 1 \text{ MHz}$, $V_{DD} = 0.5 \text{ V}$, and $R_{EH} = 500 \text{ Ω}$. $V_{REC}$ of the AC-DC-DC CP was 0.25 V due to a threshold voltage of the NMOS diode $V_{THD}$ of 0.13 V, whereas that of the clocked AC-DC CP was 0.4 V. A reduction in $V_{REC}$ by 0.15 V resulted in a reduction in the maximum available output voltage by 1.5 V, which can be estimated by $\Delta V_{REC} \times (N + 1)$. $C_{REC}$ of about 500 nF is needed to have a moderate ripple voltage in $V_{REC}$ of 10 mV at $f_{IN} = 1 \text{ kHz}$. As a result, AC-DC-DC CP requires a decoupling capacitor inside in addition to a filtering capacitor for $V_{OUT}$.

![Figure 26. Comparison of power distribution.](image)

**Figure 26.** Comparison of power distribution.

![Figure 27. Simulated $I_{OUT}$ as a function of $V_{OUT}$ ($f_{IN} = 1 \text{ kHz}, f_{CLK} = 1 \text{ MHz}, V_{DD} = 0.5 \text{ V}, R_{EH} = 500 \text{ Ω}$).](image)

**Figure 27.** Simulated $I_{OUT}$ as a function of $V_{OUT}$ ($f_{IN} = 1 \text{ kHz}, f_{CLK} = 1 \text{ MHz}, V_{DD} = 0.5 \text{ V}, R_{EH} = 500 \text{ Ω}$).

Figure 28 shows that $I_{OUT}$ of the AC-DC-DC CP with $N$ diodes started to flow at $V_{DD} = 0.5 \text{ V}$, whereas the proposed circuit can operate at $V_{DD} = 0.3 \text{ V}$. In the case of AC-DC-DC CP, when $V_{DD} < 0.5 \text{ V}$, the voltage becomes lower than the threshold voltage of the MOS transistor, and thus it cannot operate. To have $P_{OUT} \geq 1 \text{ µW}$, the AC-DC-DC CP requires $V_{DD}$ of 0.6 V, whereas the clocked AC-DC CP requires that of 0.4 V. As a result, a cold start voltage can be reduced with the clocked AC-DC CP in comparison with the AC-DC-DC CP. In the range of $V_{DD} > 1 \text{ V}$, if process technology allows, the conventional circuit exceeds $I_{OUT}$ of the proposed circuit. Since the input voltage of the proposed circuit is AC, CP and OSC operate only in a part of one half cycle, i.e., from $\theta_5$ to $\pi - \theta_5$. On the other
hand, the conventional DC-DC CP continues to be driven by a clock with a constant voltage amplitude. Therefore, when the \( V_{DD} \) of the conventional circuit becomes sufficiently high, higher \( I_{OUT} \) is obtained.

![Simulation results of \( V_{OUT} - I_{OUT} \) for the proposed circuit and \( \eta_{TOT} \) as a function of \( V_{DD} \).](image)

**Figure 28.** Simulated \( I_{OUT} \) as a function of \( V_{DD} \) (\( f_{IN} = 1 \text{ kHz}, f_{CLK} = 1 \text{ MHz}, V_{DD} = 0.5 \text{ V}, R_{EH} = 500 \Omega \)).

Figure 29 shows simulated \( \eta_{TOT} \). The clocked AC-DC CP had the highest \( \eta_{TOT} \) of 22% at \( V_{DD} \) of 0.5 V, while the AC-DC-DC CP had \( \eta_{TOT} \) of 18% at \( V_{DD} \) of 0.8 V. The clocked AC-DC CP had a lower operation voltage than the AC-DC-DC CP did in terms of \( \eta_{TOT} \) as well as \( I_{OUT} \). Previous studies [9,10] have reported AC-DC conversion with active diodes that can reduce the voltage drop due to the diode threshold voltage, as shown in Figure 4b. The comparator compared the magnitude of \( V_{REC} \) with that of \( V_{DD} \). When \( V_{REC} \) became lower than \( V_{DD} \), PMOS was turned on with the low gate voltage and \( C_{REC} \) was charged. Figures 28 and 29 respectively show \( I_{OUT} \) and \( \eta_{TOT} \) of the AC-DC-DC CP, which were estimated by assuming \( V_{THD} = 0 \text{ V} \) when the active diode was used. The input power of the operational amplifier was assumed to be 1 \( \mu \text{W} \). In the range of \( V_{DD} \geq 0.5 \text{ V} \), AC-DC-DC CP with active diodes provided higher \( I_{OUT} \) than the proposed circuit. Because the input power of the operational amplifier was required, \( \eta_{TOT} \) became lower in the circuits with active diodes. In order to operate the operational amplifier, it is necessary to provide a power source. If \( V_{REC} \) is used as the power source for the operational amplifier, a passive diode must be connected in parallel with the active diode for cold start. Thus, the proposed AC-DC CP can have a lower cold start voltage than AC-DC-DC CPs with a lower number of discrete components.

![Power Efficiency \( \eta_{TOT} \) as a function of \( V_{DD} \).](image)

**Figure 29.** Simulated \( \eta_{TOT} \) as a function of \( V_{DD} \) (\( f_{IN} = 1 \text{ kHz}, f_{CLK} = 1 \text{ MHz}, V_{DD} = 0.5 \text{ V}, R_{EH} = 500 \Omega \)).

4.3. **Comparison with Previous Research**

Table 2 shows a comparison of the proposed circuit with existing voltage boosting circuits for vibration energy harvesting in the literature.
Table 2. Comparison on the characteristics.

| Ref. | ET* | Boosting Method | Discrete Element (Values)* | Circuit Area | Maximum \( f_{IN} \) | Power Efficiency | CMOS |
|------|-----|-----------------|---------------------------|--------------|----------------|-----------------|-------|
| [8]  | EM  | AC-DC CP        | 3C + 4D (N.A.)            | Discrete     | N.A.           | 25% (\( \eta_{TOT} \)) | N.A. 2 V 30 \( \mu \) W N.A. |
| [9]  | EM  | AC-DC-DC CP     | 1C (10 nF)                | 0.58 mm\(^2\) + 4.84 mm\(^2\) | 10 kHz (Est.) | 37% (\( \eta_{SYS} \)) | 1.2 V 2 V 33 \( \mu \) W 2k \( \Omega \) 0.35 \( \mu \) m |
| [10] | EM  | AC-DC-DC CP     | 1C (1 \( \mu \) F)       | N.A.         | 30kHz          | 13% (\( \eta_{TOT} \)) | 0.5 V 1.8 V 3.2 \( \mu \) W 180 \( \Omega \) 90 \( \mu \) m |
| [11] | EM  | Rectifier + switching regulator | 1L (N.A.) | 1.6 \times 1.6 mm\(^2\) | N.A. | 67% (\( \eta_{SYS} \)) | 0.6 V 1 V 1 \( \mu \) W 120 \( \Omega \) 0.18 \( \mu \) m |
| This work | MS | Clocked AC-DC CP | None | 0.11 mm\(^2\) | 100 kHz or higher | 23% (\( \eta_{TOT} \)), 6% (\( \eta_{SYS} \)) | 0.5 V 2 V 4.2 \( \mu \) W 500 \( \Omega \) 65 \( \mu \) m |

* ET: energy transducer, EM: electromagnetic, MS: magnetostrictive, C: chip capacitor, D: chip diode, L: chip inductor.

Existence of external elements, integrated circuit area, input/output condition, power efficiency, and technology used are shown. The maximum \( f_{IN} \) is defined by the highest frequency at which the output power is reduced by 10% from the nominal value. The proposed clocked AC-DC charge pump allows ET to operate at a frequency at least as high as 100 kHz. Due to the limitation of the measurement tool, we performed the experiment at 100 kHz or lower. Note that each paper used either \( \eta_{TOT} \) or \( \eta_{SYS} \) defined by Equations (15) and (17), respectively, for the definition of power efficiency. Compared with the previously reported circuits, the proposed circuit is only the circuit capable of obtaining an output power of an order of \( \mu \)W at 2 V without discrete elements. It has the smallest integrated circuit area. The authors have no appropriate way to compare power efficiency in different conditions at this point. Although the power efficiency is lower than those of the other circuits, the proposed one can be the best option when the highest priority is to generate a microwatt output power with the lowest cost and the smallest form factor. \( \eta_{SYS} \) of this work is higher than that of [10]. This could simply be because \( P_{EH} \) of this work was smaller due to 2 \( \times \) larger \( R_{EH} \). Technology is not a significant contributor to better performance. The threshold voltage of switching transistors is critical to have a low operating voltage.

5. Future Work

In this study, only a continuous wave at a resonant frequency of the transducer was considered. Under a realistic environment, both acceleration and operating frequency vary in time. Modeling of the proposed circuit and measurement will be required to design a clocked AC-DC CP for actual use. In addition, the output voltage was not regulated internally in this work. For actual use, a control circuit must be designed to stabilize \( V_{OUT} \) in the circuit system as shown in [23]. Furthermore, optimum design methodology needs to be established to design an optimum clocked AC-DC CP under a given condition, taking power matching at the interface between EH and CP into account. A maximum power point tracking was not considered for the clocked AC-DC CP either. It should be considered in the future.

6. Conclusions

A fully integrated clocked AC-DC charge pump circuit system was proposed, designed, and verified for vibration energy harvesting. The frequency of the clock to drive an AC-DC charge pump was upconverted with an on-chip oscillator to increase output power of the charge pump without significantly increasing the circuit area. Even with an energy transducer with \( R_{EH} \) of 500 \( \Omega \) and an open circuit voltage amplitude of 0.5 V, one can obtain 4.2 \( \mu \)W power at 2 V with a minimal area overhead of 0.11 mm\(^2\) without using large discrete capacitors when the input frequency of 1 kHz is increased to 4.8 MHz by the on-chip oscillator. As a result, it is possible to integrate the voltage...
multipliers in IoT chips for vEH. In addition, the proposed circuit has negligibly small dependency of $P_{OUT}$ on $f_{IN}$. A universal design can be applied to various energy transducers with different resonant frequencies. The fabricated clocked AC-DC CP was measured with a magnetostrictive transducer. $P_{OUT}$ of 2 µW–30 µW was obtained with $\alpha$ of 0.2 G to 0.7 G at $V_{OUT}$ of 2 V. Compared with the previously reported circuits, the proposed circuit is only the circuit capable of obtaining an output power of a microwatt order at 2 V without discrete elements.

**Author Contributions:** Conceptualization, T.T.; methodology, H.K. and T.T.; software, H.K.; validation, H.K. and T.T.; formal analysis, H.K. and T.T.; investigation, H.K. and T.T.; writing—original draft preparation, H.K.; writing—review and editing, T.T.; funding acquisition, T.T. All authors have read and agreed to the published version of the manuscript.

**Funding:** This research was partially funded by Micron Foundation.

**Acknowledgments:** This work was supported by VDEC; Synopsys, Inc.; Cadence Design Systems, Inc.; Rohm Corp.; and Micron Foundation. The authors wish to thank T. Ueno for sharing a magnetostrictive transducer for our experiments and M. Futagawa, H. Hirano, and S. Ota for technical discussion.

**Conflicts of Interest:** The authors declare no conflict of interest.

**Nomenclature**

| Symbol | Description |
|--------|-------------|
| $C$ | Capacitance per stage |
| $f_{CLK}$ | Frequency of a clock generated by ring oscillator |
| $f_{IN}$ | Frequency of harvester’s output power |
| $I_{CP}$ | Input current of the charge pump |
| $I_{OSC}$ | Current driving the oscillator |
| $I_{OUT}$ | Output current of the charge pump |
| $I_S$ | Diode saturation current |
| $N$ | Stage number of the charge pump |
| $P_{CP}$ | Input power of the charge pump |
| $P_{EH}$ | Power generated by energy harvesting |
| $P_{LOSS}$ | Power loss in the charge pump |
| $P_{OSC}$ | Power of the oscillator |
| $C_{INV}$ | Load capacitance of the oscillator |
| $P_{OUT}$ | Output power of the charge pump |
| $P_{RE}$ | Reactive power |
| $P_{TOT}$ | Power of the system |
| $R_{EH}$ | Output impedance of energy harvester |
| $R_{TOT}$ | Total output impedance of the system |
| $V_{DD}$ | AC input voltage amplitude |
| $V_{OUT}$ | Output voltage of the charge pump |
| $V_{REC}$ | Rectified voltage |
| $V_{SS}$ | Ground |
| $V_{TH_{EFF}}$ | Effective threshold voltage of diode |
| $V_T$ | Thermal voltage |
| $\beta$ | Ratio of parasitic capacitance to $C$ |
| $\theta_S$ | Phase at which the output current begins to flow |
| $\alpha$ | Vibration acceleration |

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