Proton induced Dark Count Rate degradation in 150-nm CMOS Single-Photon Avalanche Diodes

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Abstract

Proton irradiation effects on a Single-Photon Avalanche Diodes (SPADs) device manufactured using a 150-nm CMOS process are presented. An irradiation campaign has been carried out with protons of 20 MeV and 24 MeV on several samples of a test chip containing SPADs arrays with two different junction layouts. The dark count rate distributions have been analyzed as a function of the displacement damage dose. Annealing and cooling have been investigated as possible damage mitigation approaches. We also discuss, through a space radiation simulation, the suitability of such devices on several space mission case-studies.

Keywords: Single-photon avalanche diode (SPAD), CMOS, radiation effects, displacement damage, dark count rate (DCR), random telegraph signal (RTS), annealing, space radiation environment, SPENVIS.

1. Introduction

Single-Photon Avalanche Diodes (SPADs) are playing a significant role in the development of high-performance detectors for the new era High Energy Physics (HEP) and space experiments. They are semiconductor photon detectors operating in Geiger-mode, i.e., biased above the diode breakdown
due to their working principle, SPADs are capable of a substantial internal gain ($G \sim 10^6$) with no need for pre-amplification, resulting in single-photon sensitivity. Furthermore, they can provide excellent timing and spatial resolution, reaching a few tens of picoseconds and micrometers, respectively [1]. In the early 2000s, SPAD-based pixel arrays realized in CMOS technology have been demonstrated [2]. The use of CMOS technology for the design and the fabrication of SPADs led to the monolithic integration of additional pixel circuitry for avalanche quenching and signal processing, like Counter, Time to Digital Converter, etc. This resulted in a significant advantage in terms of signal temporal response, detector miniaturization and portability, low power consumption, and low fabrication cost. Due to all these extraordinary features, CMOS SPADs are a promising alternative to traditional photon detectors [3].

Many applications in the field of HEP are under investigation, such as vertex detectors for charged particles [4, 5], aerogel RICH detectors [6], ToF detector [7], etc. Even in many space applications, CMOS SPADs are very promising detectors, especially considering their low power dissipation and the possibility of compactness. In particular, SPADs are an appealing alternative to classical PMTs in scintillation light detectors [8, 9] for terrestrial and space cosmic-ray experiments. Even LIDAR, Rendez-vous, Time of Flight 2D reconstruction are possible fields of application.

In spite of all their advantages, CMOS SPADs suffer from a high level of spurious pulses whose mean rate is indicated as Dark Count Rate (DCR). One of the main mechanism responsible for dark counts in SPADs is the thermal generation of free carriers within the depletion region. It is closely related to the presence of impurities and crystal defects that introduce localized energy levels near the middle of the band-gap. These act as efficient electrons and holes generation-recombination (G-R) centers according to the Shockley-Read-Hall (SRH) model [10, 11]. Beyond thermal effects, another major contributor to DCR is band-to-band or trap-assisted tunneling [12, 13], enhanced by the high and shallow doping profiles typical of CMOS implementation.

Defects and impurities can be introduced in the detector not only in the manufacturing process, but also during its use, i.e., if operating in radiation-full environments. It is well known that exposure to particle flux can result in the production of bulk and insulator defects [14]. Therefore, a sufficient radiation hardness is a mandatory requirement for CMOS SPADs in order to withstand many years of operation in a radiation environment. Many
papers in literature report on radiation effects in custom SPADs or in SiPM [15, 16, 17]. Some recent works focused on radiation DCR induced effects in CMOS SPADS [18, 19, 20, 21, 22] while others focused on Random Telegraph Signal effects [23, 24, 25], but state of the art still need further insights.

This work aims to investigate the degradation induced by protons on a given electrical parameter, i.e., the dark count rate of a monolithic SPADs detector fabricated in a 150 nm CMOS process. For this purpose, an irradiation campaign has been carried out with protons of 20 MeV and 24 MeV to induce displacement damage effects on several samples of a test chip containing SPADs arrays with two different junction layouts. The DCR has been measured as a function of the dose on a large amount of SPADs, showing that, for this kind of devices, displacement damage could be a serious issue. Furthermore, we addressed some interesting results on the radiation-induced DCR increase origin and some possible mitigation approaches.

The obtained results have been investigated in the framework of several space mission case-studies. Expected radiation levels have been estimated by means of the web-tool software SPENVIS [26], simulating several space mission orbits, with different inclinations and shield thickness.

2. Experimental

2.1. Device layout

The devices investigated in this work are test chips provided by Fondazione Bruno Kessler (FBK) [27], containing several architectures of SPADs. A first structure is based on a P+/Nwell junction (Fig. 1, top). The guard ring, essential in order to avoid premature periphery edge breakdown, is obtained by blocking both P-well and N-well at the borders of the junction with a deep N-Well implantation. A second SPAD structure is based on a Pwell/Niso junction (Fig. 1, bottom). In this case, the guard ring is obtained by blocking both P-well and N-well at the junction periphery. A poly-Si gate blocks P+ implantation avoiding it to reach the Shallow-Trench-Isolation (STI) region.

Each SPAD is integrated with its relative front-end pixel circuit (Fig. 2). The SPAD is connected to a quenching transistor T2 which acts as a resistor. An enable transistor T1, in series with T2, is used to pull the SPAD below the breakdown voltage and to shut it down. A Schmitt-trigger comparator converts the voltage pulse from the SPAD to a digital output signal. Each
Figure 1: Cross section of SPAD structures: (top) P+/Nwell and (bottom) Pwell/Niso layouts.

Figure 2: Schematic diagram of the SPAD front-end.
SPAD can be individually enabled through row and column decoder and a multiplexer (MUX) is used to connect one SPAD at a time to the output.

The test chip contains SPADs with four different optical window sizes: 5, 10, 15, 20 $\mu$m. Each one is arranged in linear arrays of 20 SPADs and square matrices of 5x5 SPADs. In this paper, we focused on the 10x10 $\mu m^2$ SPADs, arranged in both arrays and matrices. More details about the chip design are given in [28, 29].

2.2. Measurement setup

A schematic layout of the experimental setup is shown in Fig. 3. A dedicated circuit board provides both power supply to the read-out circuit on-chip and the SPAD bias. The chip output signal is sent to an oscilloscope and to a digital counter. In order to enable a certain pixel and connect it to the chip output, a digital serial pattern is sent to the MUX by means of an external micro-controller. In order to have a fully automatized measurement procedure, SPAD power supply, digital counter, and micro-controller have been connected through a serial bus to a personal computer and interfaced by means of a LabVIEW software.

![Figure 3: Schematic diagram of experimental setup.](image)

3. Pre-irradiation characterization

In this section, the DCR characterization of the Devices Under Test (DUTs) before irradiation is showed. DCR measurements have been performed in a dark environment at a controlled temperature of 25 $^\circ$C. After measuring the breakdown voltage from the DCR-voltage characteristics, we obtained the DCR at 3.3V over bias voltage. Table I summarizes the DCR
Figure 4: Cumulative distribution of the DCR for the two SPADs structures.

Table 1: DCR characterization before irradiation.

| Type          | Median | Mean |
|---------------|--------|------|
| DCR [cps]     | DCR [cps] |
| P+/Nwell      | 1938   | 3342 |
| Pwell/Niso    | 1036   | 1448 |

characterization for the two SPADs structures. These results include measurements on all the chips that were irradiated later. It can be observed that P+/Nwell layout exhibits higher DCR values than the Pwell/Niso structures (Fig. 4). This behaviour can be addressed to the electric field shape, more peaked in P+/Nwell type [30].

4. Proton irradiation test

A proton irradiation test has been performed on seven CMOS SPAD chips at the Laboratori Nazionali del Sud (LNS, Italy).

Irradiations have been carried out at Tandem accelerator with a 20 MeV and 24 MeV proton beam extracted in air (Fig. 5). The beam energy on the DUT has been estimated by using both SRIM [31] and FLUKA [32] packages. Taking into account the energy loss along the beam-line and the quartz cover of the chip, the mean beam energy on chip results in 16.4 MeV and 21.1 MeV, respectively. The DUT has been carefully aligned with the beamline center by using a laser pointing system. The beam was collimated through
Table 2: Proton irradiation test summary.

| Chip | Fluence [p/cm$^2$] | Energy [MeV] | TID [krad] | DDD [TeV/g] |
|------|-------------------|--------------|------------|-------------|
| 1    | 6.7×10$^8$        | 16.4         | 2.3        | 45          |
| 2    | 1.4×10$^9$        | 16.4         | 4.8        | 94          |
| 3    | 2.0×10$^9$        | 16.4         | 7.1        | 139         |
| 4    | 2.8×10$^9$        | 16.4         | 9.6        | 188         |
| 5    | 4.1×10$^9$        | 16.4         | 14.5       | 283         |
| 6    | 6.7×10$^9$        | 16.4         | 23.5       | 457         |
| 7    | 9.1×10$^{10}$     | 21.1         | 30.5       | 608         |

Figure 5: Test beam setup at the Tandem accelerator at Laboratori Nazionali del Sud (INFN-LNS, Italy).

a circular collimator. Its spot diameter ($d = 16$ mm) and uniformity at the DUT position have been measured by means of a radio-chromic film. On a region of 10x10 mm$^2$ around the center of the beam spot, the beam intensity had a variation of ± 5% with respect to the average value. This region widely contains, within the alignment error, the tested chip area (2x3 mm$^2$). The delivered proton charge during each irradiation run has been measured using an ionization chamber, and taking into account the beam profile, the corresponding fluence calculated. Table 2 summarizes the dosimetry for each irradiation of the chips. The Total Ionizing Dose (TID) and the Displacement Damage Dose (DDD) have been respectively calculated as TID = LET · Φ and DDD = NIEL · Φ, where the LET has been obtained by means of SRIM, the NIEL by means of a NIEL calculator software [33] and Φ represents the proton fluence.
Figure 6: DCR increase as a function of the displacement damage dose. Case of P+/Nwell (top) and Pwell/Niso (bottom) layouts. The mean DCR values have been fitted with a \( y = ax \) function: P+/Nwell \( a = (1025 \pm 96) \text{ cps}/\text{TeV g} \) - Pwell/Niso \( a = (685 \pm 52) \text{ cps}/\text{TeV g} \). The green band shows the 68% population interval around the median.

During the irradiation, the devices were kept unbiased with all the terminals connected to the ground. The DCR measurements have been performed after a week from the irradiation. For this study, all the measurements were performed at 3.3V over bias voltage at room temperature. In Fig. 6, we report the behaviours of the DCR increase distributions, where the initial DCR was subtracted for every single SPAD, as a function of the delivered displacement damage doses.

Although data are taken from different samples, it is reasonable to assume that the differences are negligible compared to the expected effects. It can
be observed that the DCR increase is almost linear with respect to the DDD for both P+/Nwell and Pwell/Niso. The trend is very similar between the two structures, except for the higher dose point, where a greater degradation is observed for the P+/Nwell junction.

Regarding the origin of the increase in DCR, several hypotheses can be made. It is reasonable to assume that the performances of SPADs front-end circuit are not significantly affected by the ionizing and displacement doses delivered in this test. CMOS transistors under 350-nm node have been demonstrated to be tolerant to ionizing radiation above the Mrad level [34], while no degradation of their operation due to bulk damage is expected [35]. Similar devices to the ones studied in this work, have been tested with a total ionizing dose irradiation, showing that they are quite immune up to Mrad doses [20]. In our irradiation test, the ionizing dose level is kept below 30 krad, furthermore, the devices were kept off during irradiation. Therefore, the observed degradation effects can be safely ascribed mainly to silicon bulk defects induced by displacement damage.

This consideration is supported by the analysis of the DCR increase distribution at different DDD (Fig. 7). After the first step of the irradiation, the
distribution presents a low-DCR peak followed by a long tail of hot SPADs. As the DDD increases, the low-DCR peak is depopulated, while the events in the high-DCR tail increase. This behaviour is consistent with the effect of the typical displacement damage [36]. The reason is to be attributed to the small cross sections of the elastic and inelastic nuclear interactions, which are responsible for the displacement damage. As a consequence, the displacement damage occurrence at low fluence is small, and only a few SPADs are affected, precisely the ones in the high DCR tail. For higher doses, the displacement damage probability per SPAD increases and a large part of the pixel are affected, resulting in a large non-uniformity increase and the creation of hot pixels.

Beyond the mean DCR increase, a further effect that we observed in many of the irradiated pixels is the appearance of a DCR Random Telegraph Signal (RTS) behaviour (Fig. 8). This consists of the discrete fluctuation of the DCR between two or more levels. RTS can also be attributed to the effect of displacement damage, i.e., to the reconfiguration of bulk defects [25].

5. DCR increase mitigation

One of the main advantages of CMOS SPADs compared to the analog ones is the possibility to address single cells. This allows one to disable high DCR pixels, resulting in a reducing of the total DCR. As an example, we report the case of a 5x5 SPADs matrix, irradiated at 94 TeV/g. By disabling

![Figure 8: DCR evolution with time of an irradiated SPADs exhibiting a dark count rate RTS behaviour.](image)

By disabling
the three noisiest cells, the average DCR reduces from 51405 cps to 17600 cps, meaning a percentage decrease of 66%. This method can only be applied at relatively low doses, in fact, when the radiation levels are high, it would require to turn off too many pixels, causing a significant loss of efficiency.

On the other hand, for high DCR levels, a coincidence between several pixels can significantly reduce the DCR. As an example, if we consider the worst DCR level obtained at a DDD = 608 TeV/g, a 3 SPADs coincidence would result in a few Hz false coincidence rate, assuming a time window of 10 ns.

Following, two further techniques to mitigate the DCR are reported, precisely cooling and annealing. Using a climatic chamber we varied the temperature in the range \([-35 °C, +25 °C]\]. Fig. 10 shows the DCR as a function of temperature measured on SPADs irradiated at the maximum dose of 608 TeV/g. As expected, the DCR decreases with temperature, roughly it halves its value by decreasing temperature every ten degrees. On a small subset SPADs, we measured the DCR activation energy and found for the Pwell/Niso layout \(E_a \sim 0.4eV\). The activation energies are lower than the mid-bandgap, suggesting a generation mechanism related to the presence of bulk defects, with an electric field enhancement mechanisms, like Poole-Frenkel effects or Trap Assisted Tunneling (TAT) [37, 38].

After the irradiation, samples have been left at room temperature (25 °C) for a month. The subsequent measurements showed a small decrease (less than 5%) in DCR for almost all SPADs, meaning that self-annealing effects

![Figure 9: DCR maps of a 5x5 SPADs matrix irradiated at a DDD = 94 TeV/g.](image-url)
occurred. In order to deepen this effect, we performed an high temperature isochronal annealing. Likewise to [36], we keep the samples for one hour at each temperature between 50 °C and 250 °C with a 50-degree step. In Fig. [11] we show the DCR unannealed factor for a chip irradiated at 608 TeV/g, namely the mean DCR measured at different annealing steps normalized to the initial value, i.e., before the first annealing step. The annealing procedure is a useful tool for a deep study of the radiation induced defect types. Following [39, 40, 41], the detection of preferential annealing temperature allows to understand the type of defect involved in the DCR generation mechanisms. Most of DCR decrease in the curve (Fig. 11) is spread from 100 °C up to 200 °C. The non-sharp observed decrease, as pointed by [41], could be attributed to the combination of different types of defects with different annealing temperature or due to a strong contribution from cluster defects [14]. According to [39], the defects corresponding to the annealing temperature interval reported in Fig. 11 are dopant related vacancy complexes as V-P and V-As center defects. At the end of the annealing procedure, the average DCR for both SPAD layouts strongly decreases, and it becomes very close to the initial value measured before irradiation.

6. Space Environment Simulation

In order to evaluate the applicability of CMOS SPADs in a space mission, we investigated the expected radiation doses for several space environment
Figure 11: Evolution of unannealed fraction of DCR as a function of the annealing temperature step on proton irradiated SPADs at a DDD = 608 TeV/g.

case-studies. As an example, we considered the Low-Earth Orbits (LEOs) followed by the Fermi Gamma-ray space-telescope and the International Space Station, a typical Medium Earth Orbit (MEO) and a Geostationary Orbit (GEO) exploited by many communication satellites. TID and DDD levels spread significantly by varying orbital altitude and inclination. LEO experiences space radiation mainly in the form of trapped protons and electrons within the Van Allen belts. Due to the much smaller radiation damage factor for electrons with respect to protons, the displacement damage term is dominated by protons. On the contrary, GEO does not experience DDD from trapped proton: the primary radiation sources are from solar protons and trapped electrons of the outer belt. The radiation dose was calculated using the online tools of the ESA Space Environment Information System (SPENVIS) [26]. For Van Allen proton and electron radiation belts modeling, the APS [42] and AE8 [43] models, calculated at the solar minimum, have been used. Fig. 12 shows the expected DDD for typical LEO, MEO and GEO orbits as a function of aluminum shielding thickness for a 10-year mission. Table 3 summarizes the results of this analysis.

On the basis of the previously showed DCR increase analysis and the space environments simulation, we can draw some conclusions about the applicability of the devices in space. Low orbits can be considered safe enough for long lifetime space missions: only a slight DCR increase is expected. On the contrary, results showed a significant increase in DCR at a proton
fluence corresponding to long lifetime, high altitude missions. This could be an issue for using SPADs in most of the applications in long life GEO mission, requiring the implementation of an efficient mitigation procedure.

7. Conclusion

The purpose of this work is the understanding and the modelling of the effects of radiation on the dark count rate in CMOS SPADs. This study has been done in order to check the suitability of CMOS SPADs for future applications requiring single-photon detection in radiation environments, like space or HEP collider experiments. For this purpose, a proton irradiation campaign has been conducted on many samples of a test chip containing two SPADs structures. Samples were irradiated at several doses, demonstrating

Table 3: Expected ionizing and non-ionizing dose for different orbits, calculated for a 10-year mission lifetime and variable aluminum shielding.

| Orbit Type   | Mean Altitude [km] | Inclination [deg.] | Al Shield [mm] | TID [krad] | DDD [TeV/g] |
|--------------|--------------------|--------------------|---------------|-----------|-------------|
| LEO-ISS      | 400                | 51.6°              | 2             | 3.7       | 19.6        |
| LEO-FERMI    | 560                | 26°                | 2             | 3.0       | 64.3        |
| MEO          | 20000              | 56.2°              | 3             | 2196      | 292         |
| GEO          | 36000              | 0°                 | 3             | 355       | 438         |
a strong susceptibility to the radiation damage. We observed that DCR increase is proportional to the amount of energy loss for displacement damage by the incoming particle. The observed DCR increase can be a critical performance issue for CMOS SPADs that are used in a radiation environment. We investigated cooling and annealing, as possible methods of mitigation. After isochronal annealing, the DUTs showed a good recovery of the original DCR behaviour. We also investigated the expected displacement damage doses for several space mission case-studies, and found that CMOS SPADs can be safely employed in low-inclination LEO space missions.

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