A 12 bit 120 MS/s SHA-less pipeline ADC with capacitor mismatch error calibration

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Abstract: In this paper, a 12-bit pipeline Analog-to-Digital (ADC) in 0.13 µm CMOS process with SHA-less structure is presented. Two kinds of high-speed comparators are proposed to reduce settling time of residue amplifier. Meanwhile, the foreground calibration algorithm can correct the mismatch of capacitors and alleviate the effect of finite gain of residue amplifier for better linearity. A single-to-differential reference voltage buffer which can be easily controlled by the reference voltage outside is also designed in this ADC. Measurement results show that the ADC achieves an spurious-free dynamic range (SFDR) of 83.6 dBc, a signal-to-noise ratio (SNR) of 67.16 dB and a signal-to-noise and distortion ratio (SNDR) of 66.9 dB with 9.95 MHz input signal at 120 MS/s. The integral nonlinearity (INL) and differential nonlinearity (DNL) are within ±0.8 LSB and ±0.25 LSB, respectively.

Keywords: pipeline ADC, SHA-less, high-speed comparator, reference voltage buffer, foreground calibration

Classification: Integrated circuits

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1 Introduction

With the development of wireless communication technology, high-speed and high-resolution analog-to-digital converter (ADC) is widely used in wireless communication systems and instrumentation. These ADCs always need at least an accuracy of 12 bit and more than 100 MS/s sample rate. Among the variety of ADC architectures, pipeline ADC is the most popular and satisfying architecture in high-speed and high-resolution applications due to its characteristics.

Traditionally, a dedicated sample-and-hold amplifier (SHA) is used to sample and hold the input signal at the front-end [1, 2]. With the increasing frequency of input signal, it is more difficult to design the SHA with high DC gain and large swing. Especially in the deep-submicron technology, the intrinsic gain and voltage supply constantly decreasing.

A “SHA-less” architecture in which the sample-and-hold circuit is integrated in the first multiplying digital-to-analog converter (MDAC) and without a dedicated amplifier is employed in this paper [3, 4]. This architecture can release the difficulty in amplifier design and significantly reducing power consumption. The disadvantage of SHA-less architecture is aperture errors, which will be worse as the increasing of frequency of input signals. A practical way is to match the sampling networks for the MDAC and the comparators in terms of topology and time constants [5]. Other important factors that influence the ADC performance are finite gain of the residue amplifier, capacitor mismatches between sampling capacitor and feedback capacitor, the offset of residue amplifiers and comparators, and the insufficient settling.
In this paper, a straightforward method of foreground digital self-calibration is proposed to correct the errors caused by capacitor mismatch and finite amplifier gain. The real weight of every capacitor in the first four stages is measured with the backend stages. Because the calibration is realized in the digital domain, it just need a few of analogue circuits and little power consumption. Two kinds of comparators are introduced in the paper. A high speed single-stage full dynamic comparator with low power occupation is used in the first stage to acquire more settling time. The second comparator, consisting of a static pre-amplifier and a dynamic amplifier-based latch, will be used in the backend stages with input offset storage (IOS) technique. And a single-to-differential reference voltage buffer is also presented.

This paper is composed of five main parts. Part 2 introduces the overall architecture of SHA-less pipeline ADC. In Part 3, the detail circuits including the SHA-less front-end, high-speed comparators, the drive circuit of reference voltages and the calibration strategy are described. Part 4 shows the measured results and finally part 5 concludes the paper.

2 ADC architecture

Fig. 1 shows the principle schematic of the proposed SHA-less pipeline ADC. The non-overlapping clock generator circuit provides the appropriate timing margin for pipeline stages and calibration algorithm. The band gap and reference buffer circuits are used to obtain separate comparative levels with high power supply rejection ratio (PSRR) and low temperature coefficient (TC). The core pipeline stages including a 3-bit first stage followed by six 2.5 bit stages and a 3-bit flash ADC in the back end. The redundancy digital techniques are employed to alleviate the requirement for offset voltage. In order to improve the accuracy of capacitor calibration, the backend ADC is with 9 bit resolution. The raw output data of the core stages will be sent to the delay alignment array and output 12 bit data after digital correction.

The 2.5-bit MDAC transfer function (Fig. 2(a)) shows that when the input signal is close to full scale range, a large output swing is necessary for residue amplifier. While a larger swing always means greater difficulty and more power consumption. The first 3-bit stage introduces two additional comparators comparing with the 2.5-bit stage [6]. That means two comparative levels will be added in
the transfer function as shown in Fig. 2(b). The residue voltage over 1/2Vref and under −1/2Vref is folded at the two new comparative levels so that all stage outputs are between ±1/2Vref at the full scale input swing [7].

![MDAC transfer function](image)

**Fig. 2.** MDAC transfer function (a) 2.5-bit (b) 3-bit

## 3 Topologies and implementation

### 3.1 SHA-less architecture

The SHA-less structure with timing diagram is illustrated in Fig. 3. The input signal is sampled by MDAC and comparator simultaneously at the falling edge of CK1, the voltage of the top plate of capacitor Ccmp will be switched to Vref when CKS goes down. The high-speed dynamic comparator starts comparison at the raising edge of CK2. And after a delay time of dt, the compared result will be sent to control the switches connecting to reference levels. The metastability of the comparator will lead to incorrect output. In the actual design, a small time constant of the latch and an appropriate dt is designed to reduce the impact of the metastability.

As mentioned before, aperture errors is the key issue of SHA-less structure. Two ways are used to alleviate the influence. One is to use the same clock CK1 as the sampling clock for the two sampling paths, the input signal is sampled at the falling edge of CK1. The other one is to keep the same time constant by adjusting the size of sampling switches according to the values of Cs and Ccmp.
### 3.2 High speed comparators

In the previous section, the comparison time accounts for most of the delay time $dt$. The more delay time, the less settling time for MDAC. Less time for settling means that a wider bandwidth residue amplifier with more power consumption is needed in MDAC. In order to achieve more settling time, a high speed comparator is introduced in the SHA-less structure. Many methods have been developed to increase the speed of comparator [8, 9]. Fig. 4 shows the schematic of a double-tail comparator with low power cost in reference [8]. The comparator introduces a preamplifier and the output of the preamplifier is directly connected to the next latching nodes to promote regeneration. While the preamplifier consumes static power and the load capacitance will also be increased at the output nodes.

![Fig. 4. Proposed in reference [8]](image)

The proposed high-speed comparator is shown in Fig. 5. The comparator is actually a single-stage dynamic comparator. With no preamplifier stage, the proposed comparator can realize fast comparison with lower power consumption comparing with the reference comparator. The analogue signal is delivered to the latch through current. In the reset phase, M12 and M13 are turned on to reset the output to VDD, M3 and M4 are also turned on to reduce the reset time. In the comparison phase, M9 is turned on and M3, M4, M12 and M13 are turned off. CLK.d delays $dt_1$ at the raising edge compared to CLK so that M10 and M11 are turned on later to accelerate the regeneration time. The time of $dt_2$ advanced at the falling edge can avoid the current flowing through M3 and M11 as well as M4 and M10 at the beginning of reset phase.

![Fig. 5. Proposed dynamic comparator in stage1](image)
To compare the performance of these two comparators, they are designed with the same size of input transistors and latch. And the comparison time is approximately the same as shown in Fig. 6. The current consumption is 1.083 mA and 0.127 mA, respectively. 88.2% power consumption is saved with the proposed comparator. Meanwhile, the proposed comparator can achieve the rail-to-rail output, while the comparator in Fig. 4 can’t.

A similar gm-boosted StrongARM comparator with only one clock signal (CLK) is proposed in [10]. The transistors driven by CLK will drop the voltage of nodes DiP and DiM to a very low voltage level after CLK goes up as shown in [10]. Thus the positive output of the latch will drop rapidly first and then increase to logic “1” (VDD). A little more power is consumed during this process especially with a large input signal. The delay time of dt1 in this paper can prevent the rapid drop of the positive output of the latch. The simulation results prove the conclusion and it also shows that it is worth adding another clock CLK_d.

The redundancy digital technique reduces the sensitivity to the offset voltage of comparator. But it doesn’t mean that there is no need to care for the offset voltage. A comparator with high speed and low offset can improves the overall performance of pipeline ADCs. The comparator as shown in Fig. 7 is used in all the stages except for the first stage and the last stage. The comparator includes a static preamplifier, a dynamic amplifier and a latch. All the switches used in the comparator are CMOS switch which is controlled by two reverse clock.

A lot of efforts have been made to improve the performance of the comparator. First, the input offset storage (IOS) technique is used. When the clock $\phi_2$ and $\phi_3$ go up, the reference voltages (VRP, VRN) associated with the offset of the static preamplifier are stored on the capacitors Cc1 and Cc2. Second, the dynamic amplifier further amplify the input signal and the output is directly connected with the output nodes of the latch so that the regeneration time of latch can be significantly reduced. While, different with the comparator in Fig. 4, two cascade transistors M10 and M11 are added. When $\phi_4$ goes up, the latch starts regeneration and the transistors (M10–M13) are all turned off. Then the load capacitance at the output nodes are reduced and it can been further decreased by using smaller size of M10 and M11. On the other hand, the turn off of M10 and M11 can isolate the output of latch and the input of dynamic amplifier, the kick-back noise of latch can been decreased significantly. Finally, the transistor M20 provides an extra charging
path to help quickly pulling up DP/DN to turn off the reference selection switches. The simulation result in Fig. 8 shows that the two stage preamplifiers can provide a gain of 12.89 dB.

3.3 Calibration algorithm

The ideal residue transfer curve of 2.5-bit is illustrated in Fig. 2(b). The ideal gain of the 2.5-bit stage is 4. While, the capacitor mismatch and the finite gain of residue amplifier will lead to ratiometric errors. Fig. 9 shows one possible residue transfer curve when the non-ideal factors mentioned above occur.

The calibration algorithm used here is to measure the real weight of each sampling capacitor with the backend ADC and replace the raw code with the measured capacitor weight [11]. There are six comparative levels in Fig. 9 and each comparative level corresponds one comparator. The output of each comparator decides the reference voltage connected with the relevant sampling capacitor. The height at each comparative level represents the residue voltage when the relevant
comparator result is 0 and 1, respectively. The height is the real weight and will be quantized with the backend ADC [12].

Assuming $D_{ij}$ represent the output of the $j$th comparator in stage $i$, the value can be 0 or 1. And the weight of the relevant capacitor is $W_{ij}$. The output of ADC can be expressed in formula 1. $D_{be}$ is the output of backend ADC.

$$D_{out} = \sum_{i=1}^{4} D_{ij} \cdot W_{ij} + D_{be}$$

$i = 1, j = 1, 2, 3, 4, 5, 6, 7, 8; i = 2, 3, 4, j = 1, 2, 3, 4, 5, 6$ (1)

The calibration starts with stage 4 and the stage 5–7 with the flash stage is used as the backend ADC. The calibrated stage 4 associated with the last stages is used to calibrate the stage 3. And the calibration algorithm is continued until the first stage is calibrated.

Fig. 10 shows the calibration diagram for $C_{s}[1]$. Two clock cycles with four working phases are used. All the capacitors are reset with common-mode voltage $V_{cmi}$ and $V_{cvm}$ at the first sampling phase. At the amplification phase shown in Fig. 10(b), the bottom plate of $C_{s}[1]$ in the upside is connected with $V_{RP}$ and the $C_{s}[1]$ in the underside is connected with $V_{RN}$. And the feedback capacitors $C_f$ are connected with the output of residue amplifier at the same time. The value of residue voltage is $a_{1}$ and the backend stages generate $D_{a_{1}}$. In the second clock cycle, the capacitors are reset again at sampling phase. At the amplification phase shown in Fig. 10(d), the bottom plate of $C_{s}[1]$ in the upside is connected with $V_{RN}$ and the $C_{s}[1]$ in the underside is connected with $V_{RP}$. Similarly, the feedback capacitors $C_f$ are connected with the output of residue amplifier at the same time. The residue voltage of $b_{1}$ is obtained and $D_{b_{1}}$ is generated by the backend stages. So, the real weight of $C_{s}[1]$ is $W_{i_{1}} = D_{a_{1}} - D_{b_{1}}$. In the same way, all the capacitor weight can be calculated as $W_{ij} = D_{aj} - D_{bj}$. While, in fact, in order to eliminate the
measurement error the average value obtained by multiple measurements is used as the real weight.

3.4 Reference voltage buffer
In this design, besides the common-mode voltage Vcmi and Vcm, eight reference voltages are required as the comparative levels and voltages VRP, VRN are used for residue amplification in MDACs. The reference voltages VRP and VRN with large driving capacity are needed to satisfy the settling requirement. In high speed ADC applications, two methods are often used to design the reference buffer: one is a low bandwidth buffer followed by a very big bypassing capacitor, and the other is a high bandwidth buffer with no bypassing capacitor.

Inspired by the design in [13], an improved on-chip reference voltage buffer is designed as shown in Fig. 11. Two primary reference voltages generated by on-chip bandgap circuit are needed to obtain VRP and VRN in traditional designs. In this schematic, only one reference voltage VBG which can be generated by internal bandgap or be provided from the chip outside is needed. A single-to-differential circuit followed by two source follower branches composes the main reference voltage buffer. The left branch (MP1, MP3, MN1, MN3) just consumes little current to generate the reference voltages. The right branch (MP2, MP4, MN2, MN4) is the mirror of left branch with replication ratio K and we can adjust the value of K to provide enough current to satisfy the settling speed according to the actual requirement. The use of three big capacitors (C2, C3, C4) can reduce the output jitter of op-amp A2 and A3. Two resistors R8 and R9 and another op-amp A5 are added to current balance circuit compared with the reference circuit in [10]. R8 and R9 can counteract the current flowing through R4 and R2 respectively.

From the schematic of Fig. 11 and assuming $R1 = R3 = R_a$, $R2 = R4 = R_b$. The following relationship is valid.
The next formulas can be derived from formula (2), (3) and (4).

\[
\begin{align*}
\frac{VRP}{VX} &= \frac{R_a + R_b}{R_a} \quad (2) \\
\frac{VBG - VX}{VX - VRN} &= \frac{R_a}{R_b} \\
\frac{VX}{R_7} + \frac{VX - VDD}{R_6} + \frac{VX - VBG}{R_5} &= 0 \quad (4)
\end{align*}
\]

\[
\begin{align*}
\frac{VRP + VRN}{2} &= \frac{R_a + R_b}{R_a} \frac{1}{R_6} \left( \frac{1}{R_5} + \frac{1}{R_6} + \frac{1}{R_7} \right) VDD \\
&\quad + \left( \frac{R_a + R_b}{R_a} \frac{1}{R_5} + \frac{1}{R_6} + \frac{1}{R_7} - \frac{R_b}{2R_a} \right) VBG \quad (5)
\end{align*}
\]

\[
\begin{align*}
VRP - VRN &= \frac{R_b}{R_a} VBG \quad (6)
\end{align*}
\]

Thus, if \( R_a = R_b \), and \( R_5 = R_6 = 2R_7 \), the relationship can be further simplified as:

\[
\begin{align*}
VRP - VRN &= VBG \quad (7) \\
\frac{VRP + VRN}{2} &= \frac{VDD}{2} \quad (8)
\end{align*}
\]

As we can see from the formula (7) and (8), the improved reference voltage buffer can not only implement the single-to-differential, but also control the difference voltage (VRP-VRN) with VBG. And the common mode voltage is fixed at \( VDD/2 \).

4 Measurement results

Fig. 12. The die micrograph of the chip

The presented 12-bit pipeline ADC with SHA-less structure is fabricated in a 1P7M 0.13 µm CMOS process and occupies an area of 6 mm². The die micrograph is shown in Fig. 12. The circuits described above are labeled in the picture. In addition, the core 1.2 V power supply is generated from an internal LDO whose supply voltage is 3.3 V. The SPI is used to control the operating mode and a large number of decoupled capacitors are also filled to relax the effect of bonding wire.
The measured results show that the chip achieves an SFDR of 83.6 dB, a SNR of 67.16 dB and a SNDR of 66.9 dB with a 9.95 MHz input signal at 120 MS/s as shown in Fig. 13(a). The INL is within ±0.8 LSB and DNL is within ±0.25 LSB. The dynamic performances vary with frequency of input signal is illustrated in Fig. 13(b). The SNR is still exceed 60.36 dB near Nyquist rate. The total power consumption is 180 mW (including internal LDO and reference buffer) with 3.3 V supply voltage at 120 MS/s. Table I summarizes the chip performance. The figure of merit (FOM) is calculated with the following expression.

\[
FOM = \frac{Power}{2^{\text{ENOB}} \cdot \text{Sample rate}}
\]  

Table I. Performance summary

| Parameter                  | Value          |
|----------------------------|----------------|
| Process                    | 0.13 µm 1P7M CMOS |
| Sample rate                | 120 MS/s       |
| Resolution                 | 12 bit         |
| ENOB                       | 10.81 bit      |
| SFDR (@9.95 MHz)           | 83.6 dB        |
| SNR (@9.95 MHz)            | 67.16 dB       |
| SNDR (@9.95 MHz)           | 66.9 dB        |
| DNL                        | ±0.8 LSB       |
| INL                        | ±0.25 LSB      |
| Die area                   | 6 mm²          |
| Power                      | 180 mW         |
| FOM                        | 0.83 pJ/step   |

Fig. 13. Experimental results of the proposed ADC
The performance of the proposed circuit compared with the previous articles is summarized in Table II. Compared with the references, the presented ADC has the best linearity and achieves a high SFDR of 83.6 dB. Even at the supply voltage of 3.3 V, its FOM is competitive and can be optimized without the internal LDO.

| Parameter            | Ref. [1]  | Ref. [2]  | Ref. [3]  | Ref. [4]  | This work |
|----------------------|-----------|-----------|-----------|-----------|-----------|
| Process              | 130 nm CMOS | 180 nm CMOS | 180 nm CMOS | 45 nm CMOS | 130 nm CMOS |
| Supply (V)           | 2         | 1.8       | 1.8       | 1.1       | 3.3       |
| Sample rate (MS/s)   | 100       | 200       | 100       | 100       | 120       |
| Resolution (bit)     | 14        | 12        | 14        | 12        | 12        |
| ENOB (bit)           | 11.52     | 8.7       | 12.03     | 9.53      | 10.81     |
| DNL/INL (LSB)        | -/4       | -/-       | 0.5/1.5   | 0.58/2.79 | 0.25/0.8  |
| SFDR (dB)            | -         | 68        | 89        | 63.22     | 83.6      |
| SNDR (dB)            | 71.5      | 54.1      | 74.2      | 59.02     | 66.9      |
| Area (mm²)           | 1.25      | -         | 10.4      | 0.39      | 6         |
| Power (mW)           | 105       | 504       | 440       | 30.4      | 180       |
| FOM (pJ/step)        | 0.36      | 6.06      | 1         | 0.41      | 0.83      |

5 Conclusion

In this paper, a 12-bit 120 MS/s pipeline ADC with SHA-less is described. In order to satisfy the settling time requirement, two different kinds of high speed comparators are proposed. And a reference voltage buffer provides huge current for residue amplification in MDACs. Meanwhile, a digital foreground calibration technique is used to eliminate the effect of capacitor mismatch and finite gain of residue amplifier. The experiment results exhibit that 83.6 dB SFDR and 67.16 dB SNR are achieved.