A software framework for pipelined arithmetic algorithms in field programmable gate arrays

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Abstract

Pipelined algorithms implemented in field programmable gate arrays are being extensively used for hardware triggers in the modern experimental high energy physics field and the complexity of such algorithms are increases rapidly. For development of such hardware triggers, algorithms are developed in C++, ported to hardware description language for synthesizing firmware, and then ported back to C++ for simulating the firmware response down to the single bit level. We present a C++ software framework which automatically simulates and generates hardware description language code for pipelined arithmetic algorithms.

Keywords: Software framework, FPGA, Pipelined arithmetic algorithms, VHDL, C++, code generation

1. Introduction

In the modern experimental high energy physics field, detectors with massive number of channels are used to identify physical processes that occur when colliding particles. Because the rate of colliding particles including uninteresting background are in the scale of MHz [1, 2, 3] and data readout from detectors are in the scale of megabytes [4, 5, 6], it is currently impossible to record all the collision data which would be produced in the terabyte per second scale. Therefore a hardware trigger which determines whether the data should be saved or not is required. The trigger should filter the detector data so that only the physics processes in interest are written to a permanent storage at an acceptable rate. The trigger also needs to be quick in making the decision, because each sub-detector can hold it’s data for only a limited amount of time due to hardware limits which is in the scale of micro seconds [1, 7, 8]. The trigger should perform all of it’s logic before this limited amount of time is reached.

Field programmable gate arrays (FPGAs) are integrated circuits that are programmed using hardware description language. Due to their programmable and parallel nature, they have been used for event triggers in the modern experimental high energy physics field [9, 10, 11] extensively. FPGA based trigger algorithms generally use integer based calculations [10, 12, 13, 14]. Although floating-point calculation can be implemented in FPGAs, the calculation latency, FPGA resource usage, and difficulty of implementation are significantly higher [15, 16].

On the other hand, physics related data are generally handled using floating-point calculations with general purpose computers and physics analysis software are built with floating-point calculations for precise results. One needs to use these software to study the performance of trigger algorithms. The implemented trigger should also be simulated in these software in such way that the effects of the trigger on the recorded physics of interest can be studied, as well as to be compared with real hardware down to the single bit level.

Due to these facts, trigger algorithms are usually developed in two software versions. One that uses floating-point calculations and one that uses integer calculations [10, 12, 13, 14]. The floating-point version shows the pure algorithm performance while the integer version shows the degradation of performance due to the constraints of integer calculation and the performance of the FPGA algorithms. Due to the coexistence of the two versions, one constantly needs to synchronize them when the algorithms are modified in one of the versions. To make matters worse, FPGAs are programmed using a hardware description language so that there can even be three versions of the same algorithm.

We have developed a framework that solves the multiple version problem. Once an algorithm is implemented in the framework, one can obtain the floating-point calculation result, integer calculation result, and very high speed integrated circuit hardware description language (VHDL) code simultaneously.

In this work, a framework for pipelined arithmetic algorithms in FPGAs is reported. The goals and design of the framework are explained. The three C++ classes that were developed for the framework are described. Algorithms that were developed using this framework are discussed as examples.

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2. Goals

A typical procedure of firmware algorithm development is shown in Fig. 1. Algorithms are developed and tested in C++ first. After the algorithms are validated they are ported to hardware description language such as VHDL. There are several issues that should be considered when porting to VHDL. Floating-point numbers should be converted to integers. The bit width of all variables should be determined. Division and non-linear operators such as trigonometric operators should be implemented using look-up tables (LUTs). The inputs to an operator should be properly buffered so that the clock cycle between them are in synchronization. Overflow and underflow should be prevented when doing addition, subtraction, and multiplication. In order to reduce FPGA resources, the bit width of the inputs to the multiplication operator should be small enough to be implemented in a digital signal processing (DSP) slice [17]. After porting to VHDL, the resources used by the algorithm should be small enough to fit in to the chosen FPGA. One way to reduce the resource is by controlling the bit widths for the LUTs. Due to the loss of calculation precision when porting, the VHDL codes need to be simulated, a priori to confirm if they can achieve their goals. A floating-point calculation of the algorithm should be performed to confirm the loss of precision due to this integer conversion. The VHDL codes should be simulated in C++ in such a way that the results can be used in studying other algorithms. Simulation in C++ will also help in debugging the firmware algorithm most efficiently. A framework is developed to simplify the entire process of pipelined arithmetic firmware algorithm development. The framework can execute the algorithm using floating-point calculations, simulate the integer-valued version of the algorithm, automatically generate VHDL code, and deal with all the issues described previously for arithmetic algorithms. After an algorithm is developed the framework will handle the rest of the development process most efficiently.

3. Design

Three classes have been developed in total. The first one is for simulating VHDL signals and the second one is for LUTs that use block RAMs (BRAMs) [18]. The third class is to store the information related with our VHDL codes. Clock cycles are taken into consideration so that the signals are properly buffered for the pipelined algorithms in the VHDL code.

3.1. Signal class

The signal class has been implemented to simulate the VHDL signed and unsigned types. Since algorithms generally use floating-point variables but VHDL signals are integer variables, a conversion from floating-point values to integer values are executed when the range of the floating-point variables and bit widths are given. For signed variables, the conversion is done by the following equations

\[ \text{symmetric max} = \max (\text{maximum float value}, \left\lceil \text{minimum float value} \right\rceil) \]  \hspace{1cm} (1)

\[ \text{conversion constant} = \frac{2^{n-1} - 0.5}{\text{symmetric max}} \] \hspace{1cm} (2)

\[ \text{integer variable} = \left\lfloor \frac{\text{float variable} \times \text{conversion constant}}{\text{symmetric max}} \right\rfloor, \] \hspace{1cm} (3)

where \( n \) is a given the bit width, \( \max \) is the maximum function, \( \lceil \cdot \rceil \) is a round-off function, and float refers to a floating-point. For unsigned variables, the conversion is done by the following equation

\[ \text{conversion constant} = \frac{2^n - 0.5}{\text{maximum float value}} \] \hspace{1cm} (4)

\[ \text{integer variable} = \left\lfloor \frac{\text{float variable} \times \text{conversion constant}}{\text{maximum float value}} \right\rfloor, \] \hspace{1cm} (5)

where \( n \) is a given bit width. The real value which the integer value represents can be calculated using following equation

\[ \text{real value} = \frac{\text{integer value}}{\text{conversion constant}}. \] \hspace{1cm} (6)

Addition, subtraction and multiplication operators have been implemented as class methods. The maximum and minimum values are calculated and stored in the class so that bit widths can be reduced to a minimum for each operator. Before adding and subtracting, the input’s conversion constants should be matched. They are similarly matched by multiplying a factor of two which is done by bit shifting. The multiplication method is implemented so that only one DSP slice is used to reduce FPGA resources. One DSP slice can perform 25 bit \( \times \) 18 bit calculations so that the bit width of the input is constrained to 25 bits or 18 bits by applying bit shifts. An if-else method is also implemented to be able to control the flow of the algorithm. It consists of a comparing component and an assigning component. Two signals can be compared with a compare method which receives ==, !=, >, >=, <, <=, & & and | | as an argument and returns a Boolean type signal. Depending on the comparison, different arithmetic operations can be preformed by setting the assigning component.
Each method for this class has logic which can generate VHDL code. To reduce calculation overhead, a flag is used to turn it on and off. All the methods also perform floating-point calculations where the results are stored in the class so that it can be compared with the integer-valued calculations.

The \( \leq \) operator is overloaded to represent that the logic should be performed in one clock cycle as in VHDL. When this operator is used, the clock cycle of the signal in the left-hand side will be assigned with one addition clock cycle compared to the right-hand side.

An example C++ code for pipelined addition using the framework is shown in Listing 1. After two \( \phi \) values are added together in one clock cycle, another \( \phi \) value is added to the sum in the next clock cycle. The automatically generated VHDL code is shown in Listing 2. The signals are defined according to the logic in the implemented C++ code. The buffers required for pipelining the logic are also defined. Sequential VHDL statements are written according to the C++ code. The framework simulated results is shown in Table 1. The simulated floating-point values, integer values and real values for each signal are shown. It demonstrates that the framework simulation is working well.

Listing 1: Example C++ code for a pipelined addition. The \( \leq \) operator is overloaded to represent the logic should be performed in one clock cycle. \( \phi_0, \phi_1, \) and \( \phi_2 \) are defined as signed signals with 10 bits and have a range from \(-3.14\) to \(3.14\). \( \phi_0, \phi_1, \) and \( \phi_2 \)'s current values are \(1.57\), \(-0.785\), and \(0.785\). \( \phi_0 \) and \( \phi_1 \) are added during one clock cycle to obtain \( \phi_{\text{Add}} \). This is added with \( \phi_2 \) to obtain \( \phi_{\text{Add2}} \) on the next clock cycle.

// Define signals
JSN Signal phi_0 \( \leq \) JSignal(10, \(1.57\), -3.14, 3.14, 0, storage);
JSN Signal phi_1 \( \leq \) JSignal(10, -0.785, -3.14, 3.14, 0, storage);
JSN Signal phi_2 \( \leq \) JSignal(10, 0.785, -3.14, 3.14, 0, storage);
// Addition
JSN Signal phiAdd \( \leq \) phi_0 + phi_1;
// Pipelined addition
JSN Signal phiAdd2 \( \leq \) phiAdd + phi_2;

Listing 2: Automatically generated VHDL for a pipelined addition example. The framework defines the signals according to the JSignal properties in the C++ code. There is also a buffer for \( \phi_2 \) to synchronize the clock cycle between \( \phi_{\text{Add}} \) and \( \phi_2 \) when calculating \( \phi_{\text{Add2}} \). The framework writes VHDL according to the logic defined in C++.

```
-- Define signals
signal phi_0 : signed(9 downto 0) := (others=>'0');
signal phi_1 : signed(9 downto 0) := (others=>'0');
signal phiAdd : signed(10 downto 0) := (others=>'0');
signal phiAdd2 : signed(11 downto 0) := (others=>'0');
type S10D1Array is array(0 downto 0) of signed(9 downto 0);
signal phi_2 : S10D1Array := (others=>'0');
-- Sequential logic
phiAdd \( \leftarrow \) resize(phi_0,11)+phi_1;
phiAdd2 \( \leftarrow \) resize(phiAdd,12)+phi_2(b(0));
phi_2(b(0)) \( \leftarrow \) phi_2;
```

Table 1: Results of the pipelined addition example, where float value is the floating-point value, integer value is the converted integer value from the floating-point value, and real value is the value that the integer value represents. Difference between the floating-point values and integer representation values are due to the conversion from floating-point values to integer values.

### 3.2. LUT class

The LUT class generates LUTs with signal instances as input and output which can be used for operations that are not directly possible in VHDL. Division and trigonometric operators can be implemented using this class. The LUTs are implemented using BRAMs. After the LUT class is properly set, it can generate a text file which has all the values to be stored in the BRAM. This text file is then used with a commercial synthesis tool [19]. The input is transformed so that it’s minimum value is zero which reduces the BRAM size in certain cases. The output of the BRAM also shares this property. A constant value is added to get the proper output. Although this process uses a few clock cycles, it can drastically reduce the BRAM size in certain cases. This class has a logic which can generate VHDL code which should be used with a Block Memory Generator IPCORE [19] and the generated text file.

### 3.3. VHDL code storage class

This class stores the entire VHDL generated by the signal class and LUT class, so that the pipelined arithmetic algorithm can be written to a VHDL file. Also VHDL syntax for design entities, signal declaration, and buffers can be optionally added when generating the VHDL file.

### 4. Implementation examples

The Belle II experiment [1] aims to study the charge-conjugation and the parity violation in \( B \) or \( D \) meson system precisely and search for new physics at the SuperKEKB accelerator [20]. Due to the high beam current and small cross section of physics in interest, a fast and highly efficient trigger is required. The level one trigger is implemented using FPGAs to achieve these goals. The level one trigger uses pipelined algorithms to find patterns potentially originated from physics of interest. The pipelined algorithms finds track parameters obtained from the central drift chamber (CDC) hit information and

```
| Name    | Float value | Integer value | Real value |
|---------|-------------|---------------|------------|
| phi_0   | 1.570       | 256           | 1.57153    |
| phi_1   | -0.785      | -128          | -0.78577   |
| phi_2   | 0.785       | 128           | 0.78577    |
| phiAdd  | 0.785       | 128           | 0.78577    |
| phiAdd2 | 1.570       | 256           | 1.57153    |
```

This text file is called COE (coefficient file) within the Xilinx tools.
minimize $\chi^2$ for the track parameter fits. They also include logic for combining CDC track parameters with electromagnetic calorimeter (ECL) cluster parameters. Our framework described above has been used to develop the firmware and C++ code for the simulation in order to implement these algorithms automatically.

4.1. $\chi^2$ minimization fitters

There are two fitters that have been developed using our framework. One fitter minimizes $\chi^2$ defined as

$$\chi^2 = \sum_i \frac{[2(a \cos \phi_i + b \sin \phi_i) - r_i]^2}{\sigma_i^2},$$

(7)

where $a$ and $b$ are fit parameters and $\phi_i$, $r_i$ and $\sigma_i$ are input variables related with charged tracks in CDC. The second fitter minimizes $\chi^2$ defined as

$$\chi^2 = \sum_i \left[ \frac{(\cot \theta \times s_i + z_0) - z_i}{\sigma_i^2} \right]^2,$$

(8)

where $\cot \theta$ and $z_0$ are fit parameters and $s_i$, $z_i$ and $\sigma_i$ are another set of input variables related with charged tracks in CDC. There are analytical solutions to these $\chi^2$ minimization which have been used to calculate the fit parameters. They are

$$a = \sum_i \frac{\sin^2 \phi_i}{\sigma_i^2} \sum_i \frac{r_i \cos \phi_i}{\sigma_i^2} - \sum_i \frac{\sin \phi_i \cos \phi_i}{\sigma_i^2} \sum_i \frac{r_i \sin \phi_i}{\sigma_i^2},$$

(9)

$$b = \frac{2}{\sum_i \frac{\cos^2 \phi_i}{\sigma_i^2} \sum_i \frac{r_i \sin \phi_i}{\sigma_i^2} - \sum_i \frac{\sin \phi_i \cos \phi_i}{\sigma_i^2} \sum_i \frac{r_i \cos \phi_i}{\sigma_i^2}}$$

$$= \frac{2}{\sum_i \frac{\cos^2 \phi_i}{\sigma_i^2} \sum_i \frac{r_i \sin \phi_i}{\sigma_i^2} - \sum_i \frac{\sin \phi_i \cos \phi_i}{\sigma_i^2} \sum_i \frac{r_i \cos \phi_i}{\sigma_i^2}}$$

(10)

and

$$\cot \theta = \frac{\sum_i \frac{1}{\sigma_i^2} \sum_i \frac{s_i^2}{\sigma_i^2} - \sum_i \frac{s_i \phi_i}{\sigma_i^2}}{\sum_i \frac{1}{\sigma_i^2} \sum_i \frac{s_i^2}{\sigma_i^2} - \sum_i \frac{s_i \phi_i}{\sigma_i^2}}$$

(11)

$$z_0 = \frac{-\sum_i \frac{s_i \phi_i}{\sigma_i^2} \sum_i \frac{s_i \phi_i}{\sigma_i^2} + \sum_i \frac{s_i \phi_i}{\sigma_i^2} \sum_i \frac{s_i \phi_i}{\sigma_i^2}}{\sum_i \frac{1}{\sigma_i^2} \sum_i \frac{s_i^2}{\sigma_i^2} - \sum_i \frac{s_i \phi_i}{\sigma_i^2}}. $$

(12)

These solutions consist of addition, subtraction, multiplication, division and trigonometric operations. Division and trigonometric operations are implemented using LUTs. By using the VHDL code generated from our framework, a firmware test bench was developed to compare the results from the synthesized firmware and the simulated results from our framework. The structure of the firmware test bench can be seen in Fig. 2. The firmware test bench has a LUT which holds the input values for the VHDL code. It is fed to the VHDL code clock by clock. The output of the VHDL code is connected to Chipscope [21] to monitor the firmware response which is shown in Fig. 3. The results between the firmware test bench and simulation from the framework are found to be identical down to single bit level which is shown in Fig. 4. The correlation between the firmware test bench and the float-point calculation results from framework are shown in Fig. 5. It shows that our framework performs as expected.

4.2. CDC geometry calculation

By using track parameters, the position of the track at a specific layer of the CDC is required to be calculated. The position is calculated in two steps. The first step calculates the $\phi$ position of the track for the layer of the CDC using the below equation

$$\phi = \pm \arccos \left( \frac{r \rho}{2} \right) + \phi_i \mp \pi,$$

(13)

where $r$ is the radius of the CDC wire layer, $\rho$ is the curvature of the track, and $\phi_i$ is the incident angle of the track. The second step converts the $\phi$ position to a corresponding wire position at a given layer of interest. These calculations consist of addition, subtraction, multiplication and trigonometric operations. The trigonometric operations...
was implemented using a LUT. A firmware test bench confirmed that the synthesized firmware and simulated algorithm using the framework return the same results.

### 4.3. Combining CDC track and ECL cluster parameters

The framework has been used in algorithms that combines CDC trigger and ECL trigger information. The level one CDC trigger outputs track momentum parameters while the level one ECL trigger outputs cluster positions created by the deposited energy from the tracks. The two information can be combined using the position of the track which can increase the performance of the trigger. Using the track momentum parameters from the CDC trigger, the expected position of the track in the ECL detector is calculated which is used to calculate distance between the expected position and the actual cluster position. This distance can be used to relate the CDC tracks and ECL clusters. The ratio between energy and momentum of the track is also calculated which can help to identify the particle. All of these calculations are implemented using the developed framework.

### 5. Conclusions

A framework that allows automatic generation of pipelined algorithms in VHDL is implemented. Our framework can also simulate the algorithms. It was validated with $\chi^2$ minimization, a sub-detector geometry calculation, and combining algorithms of sub-detectors. Development and maintenance of pipelined arithmetic firmware algorithms using this framework is applied to a variety of situations and is demonstrated that the framework we developed is most efficient in dealing with these tasks. Our framework can be used for future trigger development in an efficient way.

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### References

[1] T. Abe, et al., Belle II Technical Design Report arXiv:1011.0352v1.
[2] Pamela Klabbers, Operation and Performance of the CMS Level-1 Trigger during 7 TeV Collisions, Physics Procedia 37 (Supplement C) (2012) 1908 – 1916, proceedings of the 2nd International Conference on Technology and Instrumentation in Particle Physics (TIPP 2011).
[3] Imma Riu and the ATLAS Collaboration, Performance of the ATLAS Trigger with Proton Collisions at the LHC, Journal of Physics: Conference Series 331 (3) (2011) 032027.
[4] R. Itoh, T. Higuchi, M. Nakao, S. Y. Suzuki, and S. Lee, Data Flow and High Level Trigger of Belle II DAQ System, IEEE Transactions on Nuclear Science 60 (5) (2013) 3720–3724.
[5] G. Bauer, et al., The data-acquisition system of the CMS experiment at the LHC, Journal of Physics: Conference Series 331 (2) (2011) 022021.

[6] The ATLAS TDAQ Collaboration, The ATLAS Data Acquisition and High Level Trigger system, Journal of Instrumentation 11 (06) (2016) P06008.

[7] C. Foudas, The CMS Level-1 Trigger at LHC and Super-LHC.

[8] P. B. Amaral, et al., The ATLAS Level-1 trigger timing setup, in: 14th IEEE-NPSS Real Time Conference, 2005., 2005, pp. 4 pp.--.

[9] Y. Iwasaki, B. Cheon, E. Won, and G. Varner, Level 1 trigger system for the Belle II experiment, in: 2010 17th IEEE-NPSS Real Time Conference, 2010, pp. 1–9.

[10] J. Chaves, Implementation of FPGA-based level-1 tracking at CMS for the HL-LHC, Journal of Instrumentation 9 (10) (2014) C10038.

[11] R. Caputo, et al., Upgrade of the ATLAS Level-1 trigger with an FPGA based Topological Processor, in: 2013 IEEE Nuclear Science Symposium and Medical Imaging Conference (2013 NSS/MIC), 2013, pp. 1–5.

[12] E. Won, A hardware implementation of artificial neural networks using field programmable gate arrays, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment 581 (3) (2007) 816 – 820.

[13] E. Bartz, et al., Fpga-based real-time charged particle trajectory reconstruction at the large hadron collider, in: 2017 IEEE 25th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM), 2017, pp. 64–71.

[14] J. Wu, M. Wang, E. Gottschalk, and Z. Shi, Fpga curved track fitters and a multiplierless fitter scheme, IEEE Transactions on Nuclear Science 55 (3) (2008) 1791–1797.

[15] N. Shirazi, A. Walters, and P. Athanas, Quantitative analysis of floating point arithmetic on fpga based custom computing machines, in: Proceedings IEEE Symposium on FPGAs for Custom Computing Machines, 1995, pp. 155–162.

[16] W. B. Ligon, et al., A re-evaluation of the practicality of floating-point operations on fpgas, in: Proceedings. IEEE Symposium on FPGAs for Custom Computing Machines (Cat. No.98TB100251), 1998, pp. 206–215.

[17] Xilinx, Virtex-6 FPGA DSP48E1 Slice, available at https://www.xilinx.com/support/documentation/user_guides/ug369.pdf.

[18] Xilinx, Virtex-6 FPGA Memory Resources, available at https://www.xilinx.com/support/documentation/user_guides/ug363.pdf.

[19] Xilinx, LogiCORE IP Block Memory Generator, available at https://www.xilinx.com/support/documentation/ip_documentation/blk_mem_gen/v7_3/pg058-blk-mem-gen.pdf.

[20] Yukiyoshi Ohnishi, et al., Accelerator design at SuperKEKB, Progress of Theoretical and Experimental Physics 2013 (3) (2013) 03A011.

[21] Xilinx, Chipscope Pro Software and Cores, available at https://www.xilinx.com/support/documentation/sw_manuals/xilinx14_7/chipscope_pro_sw_cores_ug029.pdf.