VERILOG BASED EFFICIENT CONVOLUTION ENCODER AND VITERBI-DECODER

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Abstract

In the todays digital communication Systems, transmission of data with more reliability and efficiency is the most challenging issue for data communication through channels. In communication systems, error correction technique plays a vital role. In error correction techniques, the capacity of data can be enhanced by the addition of the redundant data for the source data at the time of transmission of the data through channel. It mainly focuses on the awareness of convolution encoder and Viterbi-decoder; to decode convolution codes one prefer Viterbi-algorithm.

Key Words: Viterbi Encoder, Convolution Encoder, Xilinx power estimator.
1 Introduction

In the today's digital Communication, data transmitting through the systems play a crucial role. As the growth of the technology is increasing every day, the usage of Viterbi is also increasing. Viterbi-algorithm is one of such methods. It decodes the process by correcting it effectively. For decoding convolution codes, Viterbi-algorithm is the most used and suggestible algorithm. This algorithm can be implemented with both software and hardware implementations. An efficient data should be required in digital systems to implement a well implemented communications. Data corruption is the important thing confronted by the digital communication systems. Error correcting codes are the best technique to decrease the data corruption. In fact every communication systems followed a technique of this kind as it has the better decoding efficiency, even for Viterbi-algorithm very typical hardware is needed. The functioning obstructions will be eliminated when the decoding operation is in advance; it makes an improvement in designing Viterbi-algorithm. This algorithm is beneficial in fast rate functions which could help decoding of codes at a very faster rate. Convolution codes are useful in gaining a possible code sequence. Adaptive viterbi-algorithm uses maximum likelihood decoding process. Hardware description language (HDL) was used to evaluate the desired outcome. This language is employed in designing the electronic systems to semiconductor and electronic design industries as well as for assuring the analog and mixed signal circuit. [3]
2 Convolutional Encoder

Encoding or decoding is a process of modifying the message that can be understood easily. Decoding a message is the process of reconverting the meaning of that message from codeword to words which can be easily understood. It has both verbal and non-verbal means of communication. Nonverbal decoding doesn’t make use of words, but other gestures or signs. One can easily decode the human gestures based on their emotions. For example, some gestures of humans when they are upset, exasperation, or stressed would be a utilization of extortionate hand/arm forms of kineticism, red in the face,. Different massages can be interpreted differently from one person to the other person. Decoding is the process of understanding the information which, depending on the information that is being given in the message being which is received. Convolution code is an error correction code which will generate parity bits by arranging application of a Boolean polynomial function from a stream of data bits. This sliding application is composed of convoluting of the data bits in an encoder, which results in naming the process as convolution coding. The sliding nature of the convolution codes has a prominent attribute in trellis decoding using a time-invariant trellis. The Time invariant trellis decoding will help the convolution codes to have maximum likelihood besides the soft decision decoding with less complexity. Convolution codes are generally specified by the base code rate and the depth (or memory) of the encoder [n, k, K]. The b, K code rate is typically given as n/k. Here n is data rate of input bits and k is the symbol rate of output data stream. The depth is also referred as “constraint length” K; here output is a function of the earlier K-1 inputs. The depth can also be given as number of memory elements ’v’ in polynomial or the maximum possible states of the encoder (especially 2^v) [2]-[12].

![Convolutional encoder](image-url)
3 Viterbi Decoding Algorithm

Decoding is nothing but the reverse Process of encoding. Most computers use encoding for transfer of data, saving it then retrieving and using it. Data is transformed by an encoding mechanism like Binary Hexadecimal and then it is transmitted through a channel. For example, while sending an email, complete data including attachments will be encoded with Multipurpose Internet Mail Extensions (MIME) format. After receiving the data, decoder converts attachment contents to its original form. Viterbi-algorithm can be used in such applications for decoding a bit stream which is encoded with convolution code. Many other algorithms are also available for decoding a convolution encoded stream of data. Shanon-Fano coding/algorithm is a method which can be used in such cases. Viterbi-decoder is most prominent for decoding convolution codes with constraint lengths $k=10$, but in practice up to $k=15$ can be used. Decoding a message is nothing but extracting the meaning of that message such that it can be understood. [3]

Figure 3. Viterbi-decoder- Block Diagram

4 Performance of Viterbi-Decoder

The main stages in the Viterbi decoding process are having the following stages: Branch Metric Unit, Path Metric Unit, and Traceback Unit The fig.3 Block diagram consists of the proposed Viterbi-decoder. This section discusses about different blocks of the Viterbi-decoder. Initially Analog signals are quantized and then they are converted into digital form at the quantization block. [8]
Many other algorithms are also available for decoding a convolution encoded stream of data. Decoding is nothing but the reverse Process of encoding. Most computers use encoding for transfer of data, saving it then retrieving and using it. Data is transformed by an encoding mechanism like Binary Hexadecimal and then it is transmitted through a channel. For example, while sending an email, complete data including attachments will be encoded with Multipurpose Internet Mail Extensions (MIME) format. After receiving the data, decoder converts attachment contents to its original form. Viterbi-algorithm can be used in such applications for decoding a bit stream which is encoded with convolution code. \[10\]

Many other algorithms are also available for decoding a convolution encoded stream of data. Shanon-Fano coding/algorithm is a method which can be used in such cases. However in this dual port memory, One of the port is for writing the data and the second port is for reading the data, which is will be convenient for writing and reading the data simultaneously from various memory addresses. Memory must write the data in parallel while reading the data is asynchronous in order to maintain the lower latency or for better management of synchronous behavior in the entire system. \[9\]

Results of these are written to the memory of trace back unit. It Traces back from the end of any survivor paths to the beginning. \[2\]
5 Simulation Synthesis Results

5.1 Synthesis Report

Synthesis is the process of converting a RTL model of circuits into a gate level enlists which are described in Verilog code. Because of this there will be an increase in the design size complexity also. Because of this design complexity there is a scope to improve the design using synthesis and simulation tools. The two major Hardware Description Languages for synthesis and simulation are Verilog and VHDL.

The above figure is the simulation representation of convolution encoder and Viterbi-decoder at the circuit level. The entire code developed for this work on Xilinx ISE and can be realized on the hardware. Viterbi-algorithm implementation for encoder and decoder can be explained as a step by step process by analyzing the results of implemented system.
The above figures (Fig 5–6) show the RTL schematic of convolution encoder and Viterbi-decoder which consists of different modules like branch metric unit, encoder unit, path metric unit, survival path tracing unit and path metric store unit.

Table 1. Device Utilization of Viterbi-decoder

Table 2. Device Utilization of Viterbi-decoder[11]
5.2 Simulation Waveforms of Convolution Encoder

The Simulation Waveform for a Convolution Encoder with an input 1011 is shown in Fig. 7. Here the data Rate 1/2 and K = 9 and it Encodes the data and the output is given as 11 10 00 01. The simulation results for the implemented system can be observed by using Modelsim simulator or Xilinx ISE simulator.

![Figure 7. Xilinx simulation results for convolution encoder](image)

5.3 Simulation Waveforms of Viterbi-decoder

Viterbi-decoder decoded the encoded bit stream (11 10 00 01) and gives the output(1011) in the second half of the cycle.

![Figure 8. Xilinx simulation results for convolution encoder and Viterbi-decoder](image)
6 Conclusion

Now a day the Viterbi-algorithm becomes more interesting and challenging for the researchers in the field of communications. It also has a broader range of applications in the digital communications field in this modern era of communications. This work helps in making use of efficient coding and decoding techniques with help of Viterbi-algorithm. Also Viterbi-algorithm can be easily understood and can be implemented easily. This work presents the implementation of the Viterbi-algorithm using Verilog coding.

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