HardCoRe-NAS: Hard Constrained differentiable Neural Architecture Search

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Abstract

Realistic use of neural networks often requires adhering to multiple constraints on latency, energy and memory among others. A popular approach to find fitting networks is through constrained Neural Architecture Search (NAS), however, previous methods enforce the constraint only softly. Therefore, the resulting networks do not exactly adhere to the resource constraint and their accuracy is harmed. In this work we resolve this by introducing Hard Constrained differentiable NAS (HardCoRe-NAS), that is based on an accurate formulation of the expected resource requirement and a scalable search method that satisfies the hard constraint throughout the search. Our experiments show that HardCoRe-NAS generates state-of-the-art architectures, surpassing other NAS methods, while strictly satisfying the hard resource constraints without any tuning required.

1. Introduction

With the rise in popularity of Convolutional Neural Networks (CNN), the need for neural networks with fast inference speed and high accuracy, has been growing continuously. At first, manually designed architectures, such as VGG (Simonyan & Zisserman, 2015) or ResNet (He et al., 2015), targeted powerful GPUs as those were the common computing platform for deep CNNs. Many variants of those architectures were the golden standard until the need for deployment on edge devices and standard CPUs emerged. These are more limited computing platforms, requiring lighter architectures that for practical scenarios have to comply with hard constraints on the real time latency or power consumption. This has spawned a line of research aimed at finding architectures with both high performance and bounded resource demand.

The main approaches to solve this evolved from Neural Architecture Search (NAS) (Zoph & Le, 2016; Liu et al., 2018; Cai et al., 2018), while adding a constraint on the target latency over various platforms, e.g., TPU, CPU, Edge-GPU, FPGA, etc. The constrained-NAS methods can be grouped into two categories: (i) Reward based methods such as Reinforcement-Learning (RL) or Evolutionary Algorithm (EA) (Cai et al., 2019; Tan et al., 2019; Tan & Le, 2019; Howard et al., 2019), where the search is performed by sampling networks and predicting their final accuracy and resource demands by evaluation over some validation set. The predictors are expensive to acquire and oftentimes inaccurate. (ii) Resource-aware gradient based methods (Hu et al., 2020; Wu et al., 2019) formulate a differentiable loss function consisting of a trade-off between an accuracy term and a proxy soft penalty term. Therefore, the architecture can be directly optimized using stochastic gradient descent (SGD) (Bottou, 1998), however, it is hard to tune the trade-off between accuracy and resources, which deteriorates the network accuracy and fails to fully meet the resource requirements. The hard constraints over the resources are further violated due to a final discretization step projecting
the architecture over the differentiable search space into the discrete space of architectures.

In this paper, we propose a search algorithm that produces architectures with high accuracy (Figure 1) that satisfy any given hard latency constraint (Figure 3). The search algorithm is fast and scalable to a large number of platforms. The proposed algorithm is based on several key ideas, starting from formulating the NAS problem more accurately, accounting for hard constraints over resources, and solving every aspect of it rigorously. For clarity we focus in this paper on latency constraints, however, our approach can be generalized to other types of resources.

At the heart of our approach lies a suggested differentiable search space that induces a one-shot model (Bender et al., 2018; Chu et al., 2019; Guo et al., 2020; Cai et al., 2019) that is easy to train via a simple, yet effective, technique for sampling multiple sub-networks from the one-shot model, such that each one is properly pretrained. We further suggest an accurate formula for the expected latency of every architecture residing in that space. Then, we search the space for sub-networks by solving a hard constrained optimization problem while keeping the one-shot model pretrained weights frozen. We show that the constrained optimization can be solved via the block coordinate stochastic Frank-Wolfe (BC-SFW) algorithm (Hazan & Luo, 2016a; Lacoste-Julien et al., 2013a). Our algorithm converges faster than SGD, while tightly satisfying the hard latency constraint continuously throughout the search, including during the final discretization step.

The approach we propose has several advantages. First, the outcome networks provide high accuracy and closely comply to the latency constraint. In addition, our solution is scalable to multiple target devices and latency demands. This scalability is due to the efficient pretraining of the one-shot model as well as the fast search method that involves a relatively small number of parameters, governing only the structure of the architecture. We hope that our formulation of NAS as a constrained optimization problem, equipped with an efficient algorithm that solves it, could give rise to followup work incorporating a variety of resource and structural constraints over the search space.

2. Related Work

Efficient Neural Networks are designed to meet the rising demand of deep learning models for numerous tasks per hardware constraints. Manually-crafted architectures such as MobileNets (Howard et al., 2017; Sandler et al., 2018b) and ShuffleNet (Zhang et al., 2018) were designed for mobile devices, while TResNet (Ridnik et al., 2020) and ResNesT (Zhang et al., 2020a) are tailor-made for GPUs. Techniques for improving efficiency include pruning of redundant channels (Dong & Yang, 2019; Aflalo et al., 2020) and layers (Han et al., 2015b), model compression (Han et al., 2015a; He et al., 2018) and weight quantization methods (Hubara et al., 2016; Umuroğlu et al., 2017). Dynamic neural networks adjust models based on their inputs to accelerate the inference, via gating modules (Wang et al., 2018), graph branching (Huang et al., 2017) or dynamic channel selection (Lin et al., 2017). These techniques are applied on predefined architectures, hence cannot utilize or satisfy specific hardware constraints.

Neural Architecture Search methods automate models’ design per provided constraints. Early methods like NASNet (Zoph & Le, 2016) and AmoebaNet (Real et al., 2019) focused solely on accuracy, producing SotA classification models (Huang et al., 2019) at the cost of GPU-years per search, with relatively large inference times. DARTS (Liu et al., 2018) introduced a differential space for efficient search and reduced the training duration to days, followed by XNAS (Nayman et al., 2019) and ASAP (Noy et al., 2020) that applied pruning-during-search techniques to further reduce it to hours. Hardware-aware methods such as ProxylessNAS (Cai et al., 2018), Mnasnet (Tan et al., 2019), FBNet (Wu et al., 2019) and TFNAS (Hu et al., 2020) produce architectures that satisfy the required constraints by applying simple heuristics such as soft penalties on the loss function. OFA (Cai et al., 2019) proposed a scalable approach across multiple devices by training an one-shot model (Brock et al., 2017; Bender et al., 2018) for 1200 GPU hours. This provides a strong pretrained super-network being highly predictive for the accuracy of extracted sub-networks (Guo et al., 2020; Chu et al., 2019; Yu et al., 2020). This work relies on such one-shot model acquired within only 400 GPU hours in a much simpler manner and satisfies hard constraints tightly with less heuristics.

Frank-Wolfe (FW) algorithm (Frank et al., 1956) is commonly used by machine learning applications (Sun et al., 2019) thanks to its projection-free property (Combettes et al., 2020; Hazan & Minasyan, 2020) and ability to handle structured constraints (Jaggi, 2013). Modern adaptations aimed at deep neural networks (DNNs) optimization include more efficient variants (Zhang et al., 2020b; Combettes et al., 2020), task-specific variants (Chen et al., 2020; Tsiligkaridis & Roberts, 2020), as well as improved convergence guarantees (Lacoste-Julien & Jaggi, 2015; d’Aspremont & Pilanci, 2020). Two prominent variants are the stochastic FW (Hazan & Luo, 2016b) and Block-coordinate FW (Lacoste-Julien et al., 2013b). While FW excels as an optimizer for DNNs (Berrada et al., 2018; Pokutta et al., 2020), this work is the first to utilize it for NAS.

3. Method

In the scope of this paper, we focus on latency-constrained NAS, searching for an architecture with the highest validation accuracy under a predefined latency constraint, denoted
by $T$. Our architecture search space $S$ is parametrized by $\zeta \in S$, governing the architecture structure in a fully differentiable manner, and $w$, the convolution weights. A latency-constrained NAS can be expressed as the following constrained bilevel optimization problem:

$$\min_{\zeta \in S} \mathbb{E}_{x, y} \sim D_{\text{val}} \left[ L_{CE}(x, y \mid w^*, \zeta) \right]$$

$$\text{s.t. } LAT(\zeta) \leq T$$

$$w^* = \arg \min_w \mathbb{E}_{x, y} \sim D_{\text{train}} \left[ L_{CE}(x, y \mid w, \hat{\zeta}) \right]$$

where $D_{\text{train}}$ and $D_{\text{val}}$ are the train and validation sets’ distributions respectively, $\hat{\zeta} \sim \mathcal{P}_\zeta(S)$ is some probability measure over the search space parameterized by $\zeta$, $L_{CE}$ is the cross entropy loss as a differentiable proxy for the negative accuracy and $LAT(\zeta)$ is the estimated latency of the model.

To solve problem (1), we construct a fully differentiable search space parameterized by $\zeta = (\alpha, \beta)$ (Section 3.1), that enables the formulation of a differentiable closed form formula expressing the estimated latency $LAT(\alpha, \beta)$ (Section 3.2) and efficient acquisition of $w^*$ (Section 3.3). Finally, we introduce rigorous constrained optimization techniques for solving the outer level problem (Section 3.4).

### 3.1. Search Space

Aiming at the most accurate latency, a flexible search space is composed of a micro search space that controls the internal structures of each block $b \in \{1, \ldots, d \}$, together with a macro search space that specifies the way those are connected to one another in every stage $s \in \{1, \ldots, S \}$.

#### 3.1.1. Micro-Search

Every block is an elastic version of the MBInvRes block, introduced in (Sandler et al., 2018a), with expansion ratio $er \in \mathcal{A}_{er} = \{3, 4, 6\}$ of the point-wise convolution, kernel size $k \in \mathcal{A}_k = \{3 \times 3, 5 \times 5\}$ of the depth-wise separable convolution (DWS), and Squeeze-and-Excitation (SE) layer (Hu et al., 2020) $se \in \mathcal{A}_{se} = \{\text{on}, \text{off}\}$. These blocks are configurable, as illustrated at the bottom of Figure 2, using a parametrization $(\alpha_{er, k, se}^b, \alpha_{b,k}^s, \alpha_{b,se}^s)$, defined for every block $b$ of stage $s$:

$$\alpha_{er,k,se}^b \in \{0, 1\} \quad \forall er \in \mathcal{A}_{er}, k \in \mathcal{A}_k, se \in \mathcal{A}_{se}$$

$$\alpha_{er,k,se}^b \mid \forall er \in \mathcal{A}_{er}, k \in \mathcal{A}_k, se \in \mathcal{A}_{se}; \alpha_{er,k,se} = 1$$

Each triplet $(er, k, se)$ induces a block configuration $c$ that resides within a micro-search space $\mathcal{C} = \mathcal{A}_{er} \otimes \mathcal{A}_k \otimes \mathcal{A}_{se}$, parameterized by $\alpha \in \mathcal{A} = \otimes_{s=1}^S \otimes_{b=1}^d \otimes_{c \in \mathcal{C}} \alpha_{b,c}^s$, where $\otimes$ denotes the Cartesian product. Hence, for each block $b$ of stage $s$ we have:

$$\alpha_{b,c}^s \in \{0, 1\}^{|\mathcal{C}|} \quad \forall s \in \{1, \ldots, S\}$$

#### 3.1.2. Macro-Search

Inspired by (Hu et al., 2020; Cai et al., 2019), the output of each block of every stage is also directed to the end of the stage as illustrated in the middle of Figure 2. Thus, the depth of each stage $s$ is controlled by the parameters $\beta \in \mathcal{B} = \otimes_{s=1}^S \otimes_{b=1}^d \otimes_{c \in \mathcal{C}} \beta_c^s$, such that:

$$\beta_c^s \in \{0, 1\}^d \quad \forall s \in \{1, \ldots, S\}, c \in \mathcal{C}$$

The depth is $b^* \in \{b \mid \beta_c^b = 1, b \in \{1, \ldots, d\}\}$, since:

$$x_{b+1}^s = \sum_{b=1}^d \beta_c^s \cdot x_{b+1}^s$$

#### 3.1.3. The Composed Search Space

The overall search space is composed of both the micro and macro search spaces parameterized by $\alpha \in \mathcal{A}$ and $\beta \in \mathcal{B}$, respectively, such that:

$$\mathcal{S} = \left\{ (\alpha, \beta) \mid \begin{array}{l}
\alpha \in \mathcal{A}, \beta \in \mathcal{B} \\
\alpha_{b,c}^s \in \{0, 1\}^{|\mathcal{C}|} \mid \forall s \in \{1, \ldots, S\}, c \in \mathcal{C} \\
\beta_c^s \in \{0, 1\}^d \mid \forall s \in \{1, \ldots, S\}, c \in \mathcal{C} \\
\end{array} \right\}$$

An input feature map $x_b^0$ to block $b$ of stage $s$ is processed as follows:

$$x_{b+1}^s = \sum_{c \in \mathcal{C}} \alpha_{b,c}^s \cdot O_{b,c}(x_b^s)$$

where $O_{b,c}(\cdot)$ is the operation performed by the elastic MBInvRes block configured according to $c = (er, k, se)$. Having several configurations $O_{b,c}(\cdot)$ share the same values of $\alpha_{er,k,se}^b$ or $\alpha_{b,k}^s$ or $\alpha_{b,se}^s$ induces weight sharing between the common operations of the associated architectures. This weight sharing is beneficial for solving the inner problem (1) effectively, as will be discussed in Section 3.3.
A continuous probability distribution is induced over the space, by relaxing \( \alpha_{b,c}^* \in \{0, 1\}^{|C|} \rightarrow \alpha_{b,c}^* \in \mathbb{R}_+^{|C|} \) and \( \beta_{b}^* \in \{0, 1\}^d \rightarrow \beta_{b}^* \in \mathbb{R}_+^d \) to be continuous rather than discrete. A sample sub-network is drawn \( \hat{\zeta} = (\hat{\alpha}, \hat{\beta}) \sim \mathcal{P}_\zeta(S) \) using the Gumbel-Softmax Trick (Jang et al., 2016) such that \( \zeta \in \mathcal{S} \), as specified in (4) and (5). In summary, one can view the parametrization \((\alpha, \beta)\) as a composition of probabilities in \( \mathcal{P}_\zeta(S) \) or as degenerated one-hot vectors in \( \mathcal{S} \).

Effectively we include at least a couple of blocks in each stage by setting \( \beta_{1}^* = 0 \), hence, the overall size of the search space is:

\[
|\mathcal{S}| = (\sum_{b=2}^{d} |C|^b)^S = (\sum_{b=2}^{d} |A_{ce}|^b \cdot |A_k|^b \cdot |A_{ce}|^b)^S \\
= ((3 \times 2 \times 2)^2 + (3 \times 2 \times 2)^3 + (3 \times 2 \times 2)^4)^5 \approx 10^{27}
\]

### 3.2. Formulating the Latency Constraint

Aiming at tightly satisfying latency constraints, we propose an accurate formula for the expected latency of a sub-network. The expected latency of a block \( b \) can be computed by summing over the latency \( t_{b,c}^* \) of every possible configuration \( c \in A \):

\[
\hat{\ell}_b = \sum_{c \in C} \alpha_{b,c}^* \cdot t_{b,c}^*
\]

Thus the expected latency of a stage of depth \( b' \) is

\[
\ell_{b'} = \sum_{b=1}^{b'} \hat{\ell}_b
\]

Taking the expectation over all possible depths yields

\[
\ell^* = \sum_{b'=1}^{d} \beta_{b'}^* \cdot \ell_{b'}
\]

and summing over all the stages results in the following formula for the overall latency:

\[
LAT(\alpha, \beta) = \sum_{s=1}^{S} \sum_{b'=1}^{d} \sum_{b=1}^{b'} \sum_{c \in C} \alpha_{b,c}^* \cdot t_{b,c}^* \cdot \beta_{b'}^* \quad (3)
\]

The summation originated in (2) differentiates our latency formulation (3) from that of (Hu et al., 2020).

Figure 3 provides empirical validation of (3), showing that in practice the actual and estimated latency are very close on both GPU and CPU. More details on the experiments are provided in Section 4.2.1.

**Remark:** By replacing the latency measurements \( t_{b,c}^* \) with other resources, e.g., memory, FLOPS, MACS, etc., one can use formula (3) to add multiple hard constraints to the outer problem of (1).

### 3.3. Solution to the Inner Problem \( w^* \)

Previous work proposed approximated solutions to the following unconstrained problem:

\[
\min_{\zeta \in \mathcal{S}} \mathbb{E}_{\zeta \sim \mathcal{P}_\zeta(S)} [\mathcal{L}_{CE}(x, y \mid w^*, \zeta)]
\]

\[
\text{s.t. } w^* = \arg\min_w \mathbb{E}_{\zeta \sim \mathcal{P}_\zeta(S)} [\mathcal{L}_{CE}(x, y \mid w, \zeta)]
\]

typically by alternating or simultaneous updates of \( w \) and \( \zeta \) (Liu et al., 2018; Xie et al., 2018; Cai et al., 2018; Wu et al., 2019; Hu et al., 2020). This approach has several limitations. First, obtaining a designated \( w^* \) with respect to every update of \( \zeta \) involves a heavy training of a neural network until convergence. Instead a very rough approximation is obtained by just a few update steps for \( w \). In turn, this approximation creates a bias towards strengthening networks with few parameters since those learn faster, hence, get sampled even more frequently, further increasing the chance to learn in a positive feedback manner. Eventually, often overly simple architectures are generated, e.g., consisting of many skip-connections (Chen et al., 2019; Liang et al., 2019). Several remedies have been proposed, e.g., temperature annealing, adding uniform sampling, modified gradients and updating only \( w \) for a while before the joint optimization begins (Noy et al., 2020; Wu et al., 2019; Hu et al., 2020; Nayman et al., 2019). While those mitigate the bias problem, they do not solve it.

We avoid such approximation whatsoever. Instead we obtain \( w^* \) of the inner problem of (1) only once, with respect to a uniformly distributed architecture, sampling \( \zeta \) from \( \mathcal{P}_\zeta(S) = U(S) \).

This is done by sampling multiple distinctive paths (sub-networks of the one-shot model) for every image in the batch.
in an efficient way (just a few lines of code provided in the supplementary materials), using the Gumbel-Softmax Trick. For every feature map $x$ that goes through block $b$ of stage $s$, distinctive uniform random variables $U_{b,c,x}^s, U_{b,x}^s \sim U(0, 1)$ are sampled, governing the path undertaken by this feature map:

$$\hat{a}_{b,c,x}^s = \frac{e^{\log(a_{b,c,x}^s) - \log(\log(U_{b,c,x}^s))}}{\sum_{c \in C} e^{\log(a_{b,c,x}^s) - \log(\log(U_{b,c,x}^s))}}$$

(4)

$$\hat{\beta}_{b,x} = \frac{e^{\log(\beta_{b,x}^s) - \log(\log(U_{b,x}^s))}}{\sum_{c \in C} e^{\log(\beta_{b,c,x}^s) - \log(\log(U_{b,c,x}^s))}}$$

(5)

Based on the observation that the accuracy of a sub-network with $w^*$ should be predictive for its accuracy when optimized as a stand-alone model from scratch, we aim at an accurate prediction. Our simple approach implies that, with high probability, the number of paths sampled at each update step is as high as the number of images in the batch.

The benefits of such optimization are demonstrated in Figure 5 through a toy problem, described in Section 4.2.3. While GD is sensitive to the trade-off involved with a soft penalty, FW converges faster to the optimum with zero penalty.

All this requires $S_{LAT}$ to be convex. While $P_s(S)$ is obviously convex, formed by linear constraints, the latency constraint $LAT(\zeta) \leq T$ is not necessarily so. The latency formula (3) can be expressed as a quadratic constraint by

$$\min_{\zeta \in S_{LAT}} \mathbb{E}_{x,y \sim D_{val}} [L_{CE} (x, y \mid w^*, \zeta)]$$

(6)

following the update step:

$$\zeta_{t+1} = (1 - \gamma_t) \cdot \zeta_t + \gamma_t \cdot \xi_t$$

(7)

$$\xi_t = \arg\min_{\zeta \in S_{LAT}} \zeta^T \cdot \nabla_{\zeta} L_{CE} (x_t, y_t \mid w^*, \zeta_t)$$

(8)

where $(x_t, y_t)$ are the sampled data and the learning rate at step $t$, respectively. For $S_{LAT}$ of linear constraints, the linear program (8) can be solved efficiently, using the Simplex algorithm (Nash, 2000).

A convex $S_{LAT}$ together with $\gamma_t \in [0, 1]$ satisfy $\zeta_t \in S_{LAT}$ anytime, as long as $\zeta_0 \in S_{LAT}$. We provide a method for satisfying the latter in the supplementary materials.
Figure 5. Objective loss and soft penalty for FW and GD for different values of the penalty coefficient $\lambda$. Solid and dashed curves represent the objective loss (left y-axis) and soft penalty (right y-axis), respectively. FW converges to the optimum much faster than GD.

Most methods use the $\arg\max$ operator:

$$\bar{\alpha}_{b,c} = \{ c | \alpha_{b,c} = \arg\max_{c\in C} \alpha_{b,c} \}$$ (12)

$$\bar{\beta}_{b} = \{ b | \beta_{b} = \arg\max_{b\in \{2,..,d\} } \beta_{b} \}$$

for all $s \in \{1,..,S\}$, $b \in \{1,..,d\}$, $c \in C$, where $(\bar{\alpha}, \bar{\beta})$ is the solution to the outer problem of (1).

For resource-aware NAS methods, applying such projection results in possible violation of the resource constraints, due to the shift from the converged solution in the continuous space. Experiments showing that latency constraints are violated due to (12) are provided in Section 4.2.4.

While several methods mitigate this violation by promoting sparse probabilities during the search, e.g., (Noy et al., 2020; Nayman et al., 2019), our approach completely eliminates it by introducing an alternative projection step, described next.

Viewing the solution of the outer problem $(\alpha^*, \beta^*)$ as the credit assigned to each configuration, we introduce a projection step that maximizes the overall credit while strictly satisfying the latency constraints. It is based on solving the following two linear programs:

$$\max_{\alpha \in \mathcal{S}^*} \alpha^T \cdot \alpha^* ; \quad \max_{\beta \in \mathcal{S}^*} \beta^T \cdot \beta^*$$ (13)

Note, that when there is no latency constraint, e.g., $T \to \infty$, (13) coincides with (12).

We next provide a theorem that guarantees that the projection (13) yields a sparse solution, representing a valid sub-network of the one-shot model. Specifically, a single probability vector from those composing $\alpha$ and $\beta$ contains up to two non-zero entries each, as all the rest are one-hot vectors.

**Theorem 3.1.** The solution $(\alpha, \beta)$ of (13) admits:

$$\sum_{c\in C} |\alpha_{b,c}^*|^0 = 1 \forall (s, b) \in \{1,..,S\} \times \{1,..,d\} \setminus \{(s\alpha_{b}, b\alpha)\}$$

$$\sum_{b=1}^{d} |\beta_{b}^s|^0 = 1 \forall s \in \{1,..,S\} \setminus \{s\beta\}$$

where $|\cdot|^0 = \{ c | > 0 \}$ and $(s\alpha_{b}, b\alpha), s\beta$ are single block and stage respectively, satisfying:

$$\sum_{c\in C} |\alpha_{b,c}^*|^0 \leq 2 ; \quad \sum_{b=1}^{d} |\beta_{b}^s|^0 \leq 2$$ (14)

Refer to the supplementary materials for the proof.

**Remark:** A negligible deviation is associated with taking the $\arg\max$ (12) over the only two couples referred to in (14). Experiments supporting this are described in Section 4.2.4. Furthermore, this can be entirely eliminated by solving an equivalent Multiple-Choice Knapsack Problem (MCKP) as described in the supplementary material.
4. Experimental Results

4.1. Search for State-of-the-Art Architectures

4.1.1. Dataset and Setting

For all of our experiments, we train our networks using SGD with a learning rate of 0.1 with cosine annealing, Nesterov momentum of 0.9, weight decay of $10^{-4}$, applying label smoothing (Szegedy et al., 2016) of 0.1, mixup (Zhang et al., 2017) of 0.2, Autoaugment (Cubuk et al., 2018), mixed precision and EMA-smoothing.

We obtain the solution of the inner problem $w^*$ as specified in sections 3.3 and 4.2.2 over 80% of a random 80-20 split of the ImageNet train set. We utilize the remaining 20% as a validation set and search for architectures with latencies of 40, 45, 50, 55, 60 and 25, 30, 40 milliseconds running with a batch size of 1 and 64 on an Intel Xeon CPU and and NVIDIA P100 GPU, respectively. The search is performed according to section 3.4 for only 2 epochs of the validation set, lasting for 8 GPU hours\(^4\).

4.1.2. Comparisons with other methods

We compare our generated architectures to other state-of-the-art NAS methods in Table 1 and Figure 1. For each model in the table, we use the official PyTorch implementation (Paszke et al., 2019) and measure its latency running on a single thread with the exact same conditions as for our networks. We excluded further optimizations, such as Intel MKL-DNN (Intel, R), therefore, the latency we report may differ from the one originally reported. For the purpose of comparing the generated architectures alone, excluding the contribution of evolved pretraining techniques, all the models (but OFA\(^2\)) are trained from a random initialization with the same settings, specified in section 4.1.1. It can be seen that networks generated by our method meet the latency target closely, while at the same time surpassing all the others methods on the top-1 accuracy over ImageNet with a reduced scalable search time.

4.2. Empirical Analysis of Key Components

4.2.1. Validation of the Latency Formula

One of our goals is to provide a practical method to accurately meet the given resource requirements. Hence, we validate empirically the accuracy of the latency formula (3), by comparing its estimation with the measured latency. Experiments were performed on two platforms: Intel Xeon CPU and NVIDIA P100 GPU, and applied to multiple networks. Results are shown in Figure 3, which confirms a linear relation between estimated and measured latency, with a ratio of 1.003 and a coefficient of determination of $R^2 = 0.99$. This supports the accuracy of the proposed formula.

\(^4\)Finetuning a model obtained by 1200 GPU hours.

| Model            | Latency (ms) | Top-1 (%) | Total Cost (GPU hours) |
|------------------|--------------|-----------|------------------------|
| MobileNetV3      | 28           | 75.2      | 180N                   |
| TFNAS-D          | 30           | 74.2      | 236N                   |
| **Ours 25 ms**   | **27**       | **75.7**  | **400 + 15N**          |
| MnasNetA1        | 37           | 75.2      | 40,000N                |
| MnasNetB1        | 34           | 74.5      | 40,000N                |
| FBNet            | 41           | 75.1      | 576N                   |
| SPNASNet         | 36           | 74.1      | 288 + 408N             |
| TPNAS-B          | 44           | 76.3      | 263N                   |
| TPNAS-C          | 37           | 75.2      | 263N                   |
| **Ours 30 ms**   | **32**       | **77.3**  | **400 + 15N**          |
| TPNAS-A          | 34           | 76.9      | 263N                   |
| EfficientNetB0   | 48           | 77.3      | 150N                   |
| MobileNetV2      | 50           | 76.5      | 150N                   |
| **Ours 40 ms**   | **41**       | **77.9**  | **400 + 15N**          |
| MobileNetV3      | 45           | 75.2      | 180N                   |
| FBNet            | 47           | 75.1      | 576N                   |
| MnasNetA1        | 55           | 75.2      | 40,000N                |
| TPNAS-B          | 60           | 75.8      | 263N                   |
| **Ours 45 ms**   | **44**       | **76.4**  | **400 + 15N**          |
| MobileNetV2      | 70           | 76.5      | 150N                   |
| **Ours 50 ms**   | **50**       | **77.1**  | **400 + 15N**          |
| EfficientNetB0   | 85           | 77.3      | 240N                   |
| **Ours 55 ms**   | **55**       | **77.6**  | **400 + 15N**          |
| FairNAS-C        | 60           | 76.7      | 240N                   |
| **Ours 60 ms**   | **61**       | **78.0**  | **400 + 15N**          |

Table 1. ImageNet top-1 accuracy, latency and cost comparison with other methods. The total cost stands for the search and training cost of N networks.

4.2.2. Evaluating the Solution of the Inner Problem $w^*$

The ultimate quality measure for a generated architecture is arguably its accuracy over a test set when trained as a stand-alone model from randomly initialized weights. To evaluate the quality of our one-shot model $w^*$ we compare the accuracy of networks extracted from it with the accuracy of the corresponding architectures when trained from scratch. Naturally, when training from scratch the accuracy could increase. However, a desired behavior is that the ranking of the accuracy of the networks will remain the same with and without training from scratch. The correlation can be calculated via the Kendall-Tau (Maurice, 1938) and Spearman’s (Spearman, 1961) rank correlation coefficients, denoted as $\tau$ and $\rho$, respectively.

To this end, we first train for 250 epochs a one-shot model $\bar{w}^*$ using the heaviest possible configuration, i.e., a depth of 4 for all stages, with $\epsilon_r = 6, k_1 = 5 \times 5, \sigma_e = \sigma_{on}$ for all the blocks. Next, to obtain $w^*$, we apply the multi-path training of Section 3.3 for additional 100 epochs of fine-tuning $\bar{w}^*$ over 80% of a 80-20 random split of the ImageNet train.
set (Deng et al., 2009). The training settings are specified in Section 4.1.1: The first 250 epochs took 280 GPU hours\(^3\) and the additional 100 fine-tuning epochs took 120 GPU hours\(^4\), summing to a total of 400 hours on NVIDIA V100 GPU to obtain \(w^*\). To further demonstrate the effectiveness of our multi-path technique, we repeat this procedure also without it, sampling a single path for each batch.

For the evaluation of the ranking correlations, we extract 18 sub-networks of common configurations for all stages of depths in \(\{2, 3, 4\}\) and blocks with an expansion ratio in \(\mathcal{A}_{c,r} = \{3, 4, 6\}\), a kernel size in \(\mathcal{A}_k = \{3 \times 3, 5 \times 5\}\) and Squeeze and Excitation being applied. We train each of those as stand-alone from random initialized weights for 200 epochs over the full ImageNet train set, and extract their final top-1 accuracy over the validation set of ImageNet.

Figure 4 shows for each extracted sub-network its accuracy without and with stand-alone training. It further shows results for both multi-path and single-path sampling. It can be seen that the multi-path technique improves \(\tau\) and \(\rho\) by 0.35 and 0.17 respectively, leading to a highly correlated rankings of \(\tau = 0.95\) and \(\rho = 0.99\).

2 for 1 - \(w^*\) Bootstrap:

A nice benefit of the training scheme described in this section is that it further shortens the generation of trained models. We explain this next.

The common approach of most NAS methods is to re-train the extracted sub-networks from scratch. Instead, we leverage having two sets of weights: \(\tilde{w}^*\) and \(w^*\). Instead of retraining the generated sub-networks from a random initialization we opt for fine-tuning \(w^*\) guided by knowledge distillation (Hinton et al., 2015) from the heaviest model \(\tilde{w}^*\). Empirically, we observe that this surpasses the accuracy obtained when training from scratch a fraction of the time. More specifically, we are able to generate a trained model within a small marginal cost of 15 GPU hours. The total cost for generating \(N\) trained models is \(400 + 15N\), much lower than the \(1200 + 25N\) reported by OFA (Cai et al., 2019).

See Table 1. This makes our method scalable for many devices and latency requirements. Note, that allowing for longer training further improves the accuracy significantly (see the supplementary materials).

4.2.3. OUTER PROBLEM: HARD VS SOFT

Next, we evaluate our method’s ability to satisfy accurately a given latency constraint. We compare our hard-constrained formulation (1) with the common approach of adding soft penalties to the loss function (Hu et al., 2020; Wu et al., 2019). The experiments were performed over a simple and intuitive toy problem:

\[
\min_x \|x\|^2 \quad \text{s.t.} \quad \sum_{i=1}^d x_i = 1 \quad ; \quad x \in \mathbb{R}^d
\]

Our approach solves this iteratively, using the Frank-Wolfe (FW) (Frank et al., 1956) update rule:

\[
x_{t+1} = (1 - \gamma_t) \cdot x_t + \gamma_t \cdot \xi_t
\]

starting from an arbitrary random feasible point, e.g. sample a random vector and normalize it. The soft-constraint approach minimizes \(\|x\|^2 + \lambda (\sum_i x_i - 1)^2\) using gradient descent (GD), where \(\lambda\) is a coefficient that controls the trade-off between the objective function and the soft penalty representing the constraint.

Figure 5, shows the objective value for \(d = 10\) and the corresponding soft penalty value along the optimization for both FW and GD with several values of \(\lambda\). It can be seen that GD is very sensitive to the trade-off tuned by \(\lambda\), often violating the constraint or converging to a sub-optimal objective value. On the contrary, FW converges faster to the optimal solution \((x^* = 1/d = 0.1)\), while strictly satisfying the constraint throughout the optimization.

4.2.4. EVALUATING THE DISCRETIZING PROJECTION

Table 2 evaluates the projection of architectures to the discrete space, as proposed in Section 3.4.2. While the commonly used argmax projection violates the constraints by up to 10\%, those are strictly satisfied by our proposed projection.

| Constraint | 35 | 40 | 45 | 50 | 55 | 60 |
|------------|----|----|----|----|----|----|
| argmax     | 36 | 42 | 50 | 54 | 58 | 66 |
| Our Projection | 35 | 40 | 45 | 49 | 54 | 60 |

Table 2. The effect of discretization method on the actual latency shows that argmax method is harmful.

5. Conclusion

The problem of resource-aware differentiable NAS is formulated as a bilevel optimization problem with hard constraints. Each level of the problem is addressed rigorously for efficiently generating well performing architectures that strictly satisfy the hard resource constraints. HardCoRe-NAS turns to be a fast search method, scalable to many devices and requirements, while the resulted architectures perform better than architectures generated by other state-of-the-art NAS methods. We hope that the proposed methodologies will give rise to more research and applications utilizing constrained search for inducing unique structures over a variety of search spaces and resource specifications.
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Appendix

A. More Specifications of the Search Space

Inspired by EfficientNet (Tan & Le, 2019) and TF-NAS (Hu et al., 2020), we build a layer-wise search space, as explained in Section 3.1 and depicted in Figure 2 and in Table 3. The input shapes and the channel numbers are the same as EfficientNet-B0. Similarly to TF-NAS and differently from EfficientNet-B0, we use ReLU in the first three stages. As specified in Section 3.1.1, the ElasticMBInvRes block is our elastic version of the MBInvRes block, introduced in (Sandler et al., 2018a). Those blocks of stages 3 to 8 are to be searched for, while the rest are fixed.

| Stage | Input | Operation | C_out | Act | b |
|-------|-------|-----------|-------|-----|---|
| 1     | 224 × 3 | 3 × 3 Conv | 32    | ReLU | 1 |
| 2     | 112 × 32 | MBInvRes | 16    | ReLU | 1 |
| 3     | 112 × 16 | ElasticMBInvRes | 24 | ReLU [2, 4] | 1 |
| 4     | 56 × 24 | ElasticMBInvRes | 80 | Swish [2, 4] | 1 |
| 5     | 28 × 40 | ElasticMBInvRes | 80 | Swish | 1 |
| 6     | 14 × 80 | ElasticMBInvRes | 112 | Swish [2, 4] | 1 |
| 7     | 14 × 112 | ElasticMBInvRes | 192 | Swish [2, 4] | 1 |
| 8     | 7 × 192 | ElasticMBInvRes | 960 | Swish | 1 |
| 9     | 7 × 960 | 1 × 1 Conv | 1280 | Swish | 1 |
| 10    | 7 × 1280 | AvgPool | 1280 | - | 1 |
| 11    | 1280 | Fc | 1000 | - | 1 |

Table 3. Macro architecture of the one-shot model. "MBInvRes" is the basic block in (Sandler et al., 2018a). "ElasticMBInvRes" denotes our elastic blocks (Section 3.1.1) to be searched for. "C_out" stands for the output channels. Act denotes the activation function used in a stage. "b" is the number of blocks in a stage, where [b, b] is a discrete interval. If necessary, the down-sampling occurs at the first block of a stage.

The configurations of the ElasticMBInvRes blocks c ∈ C are sorted according to their expected latency as specified in Table 4.

| c | er | k | se |
|---|----|---|----|
| 1 | 2 | 3 × 3 | off |
| 2 | 2 | 5 × 5 | on |
| 3 | 3 | 3 × 3 | off |
| 4 | 2 | 5 × 5 | on |
| 5 | 3 | 3 × 3 | off |
| 6 | 3 | 5 × 5 | on |
| 7 | 3 | 3 × 3 | off |
| 8 | 3 | 5 × 5 | on |
| 9 | 6 | 3 × 3 | off |
| 10 | 6 | 5 × 5 | on |
| 11 | 6 | 3 × 3 | off |
| 12 | 6 | 5 × 5 | on |

Table 4.Specifications for each indexed configuration c ∈ C. "er" stands for the expansion ratio of the point-wise convolutions, "k" stands for the kernel size of the depth-wise separable convolutions and "se" stands for Squeeze-and-Excitation (SE) with on and off denoting with and without SE respectively. The configurations are indexed according to their expected latency.

B. Searching for the Expansion Ratio

Searching for expansion ratio (er), as specified in Section 3.1.1, involves the summation of feature maps of different number of channels:

\[ y_{b, er} = \sum_{c \in A_{er}} \alpha_{b, c} \cdot PWC_{b, er}^{c}(x_{b}) \]  \hspace{1cm} (18)

where \( PWC_{b, er}^{c} \) is the point-wise convolution of block b in stage s with expansion ratio er.

The summation in (18) is made possible by calculating \( PWC_{b, er}^{c} \) only once, where \( \bar{e}r = \max A_{er} \), and masking its output several times as following:

\[ y_{b, er} \cdot \sum_{c \in A_{er}} \alpha_{b, c} \cdot PWC_{b, er}^{c}(x_{b}) \cdot \mathbb{I}_{C \leq \bar{e}r \times C_{in}} \]  \hspace{1cm} (19)

where \( \odot \) is a point-wise multiplication, \( C_{in} \) is the number of channels of \( x_{b} \) and the mask tensors \( \mathbb{I}_{C \leq \bar{e}r \times C_{in}} \) are of the same dimensions as of \( PWC_{b, er}^{c} \) with ones for all channels C satisfying \( C \leq \bar{e}r \times C_{in} \) and zeros otherwise.

Thus, all of the tensors involved in the summation have the same number of channels, i.e. \( \bar{e}r \times C_{in} \), while the weights of the point-wise convolutions are shared. Thus we gain the benefits of weight sharing, as specified in Section 3.3.

C. Multipath Sampling Code

We provide a simple PyTorch (Paszke et al., 2019) implementation for sampling multiple distinctive paths (subnetworks of the one-shot model) for every image in the batch, as specified in Section 3.3. The code is presented in figure 6.

```python
import torch
from torch.nn.functional import gumbel_softmax

def multipath(a, ops, x):
    assert C = len(a) == len(ops)
    bs = x.shape[0]
    a = torch.log(a).repeat(bs)
    a = a.reshape(bs, C).transpose(0, 1)
    a_hat = gumbel_softmax(a)
    o = torch.zeros_like(x)
    for ah, op in zip(a_hat, ops):
        o += ah.view(-1, 1, 1, 1) * op(x)
    return o
```

Figure 6. PyTorch Multipath Code
D. A Brief Derivation of the FW Step

Suppose $D$ is a compact convex set in a vector space and $f : D \to \mathbb{R}$ is a convex, differentiable real-valued function. The Frank-Wolfe algorithm (Frank et al., 1956) iteratively solves the optimization problem:

$$\min_{x \in D} f(x).$$  \hspace{1cm} (20)

To this end, at iteration $k + 1$ it aims at solving:

$$\min_{x_k + \Delta \in D} f(x_k + \Delta).$$  \hspace{1cm} (21)

Using a first order Taylor expansion of $f$, (21) is approximated in the neighborhood of $f(x_k)$, and thus the problem can be written as:

$$\min_{x_k + \Delta \in D} \Delta^T \nabla f(x_k)$$  \hspace{1cm} (22)

Replacing $\Delta$ with $\gamma(s - x_k)$ for $\gamma \in [0, 1]$, problem (22) is equivalent to:

$$\min_{x_k + \gamma(s - x_k) \in D} \gamma(s - x_k)^T \nabla f(x_k).$$  \hspace{1cm} (23)

Assuming that $x_k \in D$, since $D$ is convex, $x_k + \gamma(s - x_k) \in D$ holds for all $\gamma \in [0, 1]$ iff $s \in D$. Hence, (23) can be written as following:

$$\min_{s \in D} s^T \nabla f(x_k).$$  \hspace{1cm} (24)

Obtaining the minimizer $s_k$ of (24) at iteration $k + 1$, the FW update step is:

$$x_{k+1} \leftarrow x_k + \gamma(s_k - x_k).$$  \hspace{1cm} (25)

E. Obtaining a Feasible Initial Point

Algorithm 1 requires a feasible initial point $(u_0, \beta_0) \in S_{lat}$, assuming such a point exists, i.e. as $t$ is large enough, a trivial initial point $(u_0, \beta_0) := (\bar{u}, \bar{\beta})$ is associated with the lightest structure in the search space $S \subset \mathcal{P}(\mathcal{S})$, i.e. setting:

$$\bar{\alpha}_{s,c} = \mathbb{I}\{c = 1\}; \quad \bar{\beta}_{s,c} = \mathbb{I}\{b = 2\}$$  \hspace{1cm} (26)

for all $s \in \{1, \ldots, S\}, b \in \{1, \ldots, d\}, c \in C$, where $\mathbb{I}\{}$ is the indicator function. However, starting from this point condemns the gradients with respect to all other structures to be always zero due to the way paths are sampled from the space using the Gumbel-Softmax trick, section 3.1.3.

Hence for a balanced propagation of gradients, the closest to uniformly distributed structure in $S_{LAT}$ is encouraged. For this purpose we solve the following quadric programs (QP) alternately,

$$\min_{u \in S} \sum_{s=1}^S \sum_{b=1}^{d-1} \sum_{c=1}^{|C|-1} (\alpha_{s,b+1} - \alpha_{s,c})^2$$  \hspace{1cm} (27)

using a QP solver at each step.

Sorting the indices of configurations according to their expected latency (see Table 4), the objectives in (27) promote probabilities of consecutive indices to be close to each other, forming chains of non-zero probability with a balanced distribution up to an infeasible configuration, there a chain of zero probability if formed. Illustrations of the formation of such chains are shown in Figure 7 for several latency constraints. Preferring as many blocks participating as possible over different configurations, the alternating optimization in (27) starts with $\beta$. This yields balanced $\beta$ probabilities as long as the constraint allows it.

The benefits from starting with such initial point are quantified by averaging the relative improvements in top-1 accuracy for several latency constraints $T = \{35, 40, 45, 50, 55\}$ milliseconds as following:

$$\frac{100}{|T|} \sum_{T \in T} \frac{Acc_T^{balance \ init} - Acc_T^{lighest \ init}}{Acc_T^{lighest \ init}}$$  \hspace{1cm} (28)

where $Acc_T^{balance \ init}$ and $Acc_T^{lighest \ init}$ are the top-1 accuracy measured for fine-tuned models generated by searching the space initialized with (27) and (26) respectively, under latency constraint $T$. The calculation in (28) yields 8.3% of relative improvement in favour of (27) on average.

F. Proof of Theorem 3.1

In order to prove 3.1, we start with proving auxiliary lemmas. To this end we define the relaxed Multiple Choice Knapsack Problem (MCKP):

**Definition F.1.** Given $n \in \mathbb{N}$, and a collection of $k$ distinct covering subsets of $\{1, 2, \ldots, n\}$ denoted as $N_i, i \in \{1, 2, \ldots, k\}$, such that $\bigcup_{i=1}^k N_i = \{1, 2, \ldots, n\}$ and $\bigcap_{i=1}^k N_i = \emptyset$ with associated values and costs $p_{ij}, t_{ij} \forall i \in \{1, 2, \ldots, k\}, j \in N_i$ respectively, the relaxed Multiple Choice Knapsack Problem (MCKP) is formulated as following:

$$\max_{u,v} \sum_{i=1}^k \sum_{j \in N_i} p_{ij} u_{ij}$$

subject to

$$\sum_{j \in N_i} t_{ij} u_{ij} \leq T$$  \hspace{1cm} (29)

$$u_{ij} = 1 \quad \forall i \in \{1, \ldots, k\}$$

$$u_{ij} \geq 0 \quad \forall i \in \{1, \ldots, k\}, j \in N_i$$

where the binary constraints $u_{ij} \in \{0, 1\}$ of the original MCKP formulation (Kellerer et al., 2004) are replaced with $u_{ij} \geq 0$.

**Definition F.2.** An one-hot vector $u_i$ satisfies:

$$||u^i||_0^0 = \sum_{j \in N_i} |u_{ij}|_0^0 = \sum_{j \in N_i} \mathbb{I}_{u_{ij} > 0} = 1$$

where $\mathbb{I}_A$ is the indicator function that yields 1 if $A$ holds and 0 otherwise.
Lemma F.1. The solution \( u^* \) of the relaxed MCKP (29) is composed of vectors \( u_i^* \) that are all one-hot but a single one.

Proof. Suppose that \( u^* \) is an optimal solution of (29), and two indices \( i_1, i_2 \) exist such that \( u_{i_1}^*, u_{i_2}^* \) are not one-hot vectors. As a consequence, we show that four indices, \( j_1, j_2, j_3, j_4 \) exist, such that \( u_{i_1,j_1}^*, u_{i_1,j_2}^*, u_{i_2,j_3}^*, u_{i_2,j_4}^* \notin \{0, 1\} \).

Define
\[
q = \frac{t_{i_2,j_2} - t_{i_1,j_1}}{t_{i_2,j_3} - t_{i_2,j_4}}
\] (30)
and
\[
f = (t_{i_1,j_1} - t_{i_1,j_2}) \left( \frac{p_{i_1,j_1} - p_{i_1,j_2}}{t_{i_1,j_1} - t_{i_1,j_2}} - \frac{p_{i_2,j_3} - p_{i_2,j_4}}{t_{i_2,j_3} - t_{i_2,j_4}} \right)
\]
and assume, without loss of generality, that \( f > 0 \), otherwise one could swap the indices \( j_1 \) and \( j_2 \) so that this assumption holds.

Set
\[
\Delta = \min \left( (1 - u_{i_1,j_1}^*), \frac{1 - u_{i_2,j_3}^*}{|q|}, \frac{u_{i_2,j_4}^*}{|q|} \right)
\] (31)
such that \( \Delta > 0 \) and construct another feasible solution of (29) \( u_{i_1,j_1}^* \leftarrow u_{i_1,j_1}^* + \Delta \), \( u_{i_1,j_2}^* \leftarrow u_{i_1,j_2}^* - \Delta \), \( u_{i_2,j_3}^* \leftarrow u_{i_2,j_3}^* + q\Delta \), \( u_{i_2,j_4}^* \leftarrow u_{i_2,j_4}^* - q\Delta \).

The feasibility of \( u \) is easily verified by the definitions in (30) and (31), while the objective varies by:
\[
\sum_{i=1}^{k} \sum_{j \in N_i} p_{ij} (u_{ij} - u_{ij}^*)
= \Delta (p_{i_1,j_1} - p_{i_1,j_2}) + q\Delta (p_{i_2,j_3} - p_{i_2,j_4})
= \Delta (t_{i_1,j_1} - t_{i_1,j_2}) \frac{p_{i_1,j_1} - p_{i_1,j_2}}{t_{i_1,j_1} - t_{i_1,j_2}} \frac{p_{i_2,j_3} - p_{i_2,j_4}}{t_{i_2,j_3} - t_{i_2,j_4}}
= \Delta f > 0
\] (32)
where the last inequality holds due to (31) together with the assumption \( f > 0 \). Equation (32) holds in contradiction to \( u^* \) being the optimal solution of (29). Hence all the vectors of \( u^* \) but one are one-hot vectors.

Lemma F.2. The single non one-hot vector of the solution \( u^* \) of the relaxed MCKP (29) has at most two nonzero elements.
Proof. Suppose that \( \mathbf{u}^* \) is an optimal solution of (29) and an index \( \hat{i} \) and three indices \( j_1, j_2, j_3 \) exist such that \( u_{ij_1}^*, u_{ij_2}^*, u_{ij_3}^* \notin \{0, 1\} \).

Consider the variables \( \Delta = (\Delta_1, \Delta_2, \Delta_3)^T \in \mathbb{R}^3 \) and the following system of equations:

\[
t_{ij_1} \cdot \Delta_1 + t_{ij_2} \cdot \Delta_2 + t_{ij_3} \cdot \Delta_3 = 0 \quad \text{(33)}
\]

\[
\Delta_1 + \Delta_2 + \Delta_3 = 0
\]

At least one non-trivial solution \( \Delta^* \) to (33) exists, since the system consists of two equations and three variables.

Assume, without loss of generality, that

\[
p_{ij_1} \cdot \Delta_1 + p_{ij_2} \cdot \Delta_2 + p_{ij_3} \cdot \Delta_3 > 0 \quad \text{(34)}
\]

Otherwise replace \( \Delta^* \) with \( -\Delta^* \).

Scale \( \Delta^* \) such that

\[
0 < u_{ij_1}^* + \Delta_k^* < 1 \quad \forall k \in \{1, 2, 3\} \quad \text{(35)}
\]

and construct another feasible solution of (29) \( u_{ij} \leftarrow u_{ij}^* \) for all \( i, j \) but for the following indices:

\[
u_{ij_1} \leftarrow u_{ij_1}^* + \Delta_1
\]

\[
u_{ij_2} \leftarrow u_{ij_2}^* + \Delta_2
\]

\[
u_{ij_3} \leftarrow u_{ij_3}^* + \Delta_3
\]

Since \( \Delta^* \) satisfies (33) and (35), the feasibility of \( u \) is easily verified while the objective varies by:

\[
\sum_{i=1}^{k} \sum_{j \in N_i} p_{ij}(u_{ij} - u_{ij}^*)
\]

\[
= p_{ij_1} \cdot \Delta_1 + p_{ij_2} \cdot \Delta_2 + p_{ij_3} \cdot \Delta_3 > 0 \quad \text{(36)}
\]

where the last inequality is due to (34). Equation (36) holds in contradiction to \( u^* \) being the optimal solution of (29). Hence the single non one-hot vector of \( u^* \) has at most two nonzero entries.

In order to prove Theorem 3.1, we use Lemmas F.1 and F.1 for \( \alpha \) and \( \beta \) separately, based on the observation that each problem in (13) forms a relaxed MCKP (29). Thus replacing \( u \) in (29) with \( \alpha \) and \( \beta, p \) is replaced with \( \alpha^* \) and \( \beta^* \) and the elements of \( t \) are replaced with the elements of \( \beta^T \Theta^T \) and \( \alpha^T \Theta \) respectively.

Remark One can further avoid the two nonzero elements by applying an iterative greedy solver as introduced in (Kellerer et al., 2004), instead of solving a linear program, with the risk of obtaining a sub-optimal solution.

G. 2 for 1: \( w^* \) Bootstrap - Accuracy vs Cost

In this section we compare the accuracy and total cost for generating trained models in three ways:

1. Training from scratch
2. Fine-tuning \( w^* \) for 10 epochs with knowledge distillation from the heaviest model loaded with \( \tilde{w}^* \).
3. Fine-tuning \( w^* \) for 50 epochs with knowledge distillation from the heaviest model loaded with \( \bar{w}^* \).

The last two procedures are specified in Section 4.2.2.

The results, presented in Figure 8, show that with a very short fine-tuning procedure of less than 7 GPU hours (10 epochs) as specified in Section 4.1.1, in most cases, the resulted accuracy surpasses the accuracy obtained by training from scratch. Networks of higher latency benefit less from the knowledge distillation, hence a longer training is required. A training of 35 GPU hours (50 epochs) results in a significant improvement of the accuracy for most of the models.

![Figure 8. Top-1 accuracy on Imagenet vs Latency measured on Intel Xeon CPU for a batch size of 1, for architectures found with our method trained from scratch and fine-tuned from the pretrained super-network.](image)

H. Solving the Mathematical Programs Requires a Negligible Computation Time

In this section we measure the computation time for solving the mathematical programs associated with the initialization point, the LP associated with the FW step and the LP associated with our projection. We show that the measured times are negligible compared to the computation time attributed to backpropagation.

The average time, measured during the search, for solving the linear programs specified in Algorithm 1 and in Section 3.4.2 and the quadratic program specified in Appendix E is \( 1.15 \times 10^{-5} \) CPU hours.

The average time, measured during the search, for a single backpropagation of gradients through the one-shot model is \( 2.15 \times 10^{-3} \) GPU Hours.

The overall cost of solving the mathematical programs for generating \( N \) networks is about \( 0.02N \) CPU hours, which is negligible compared to the overall \( 400 + 15N \) GPU hours.