The convolutional neural network (CNN) is an important deep learning method, which is widely used in many fields. However, it is very time consuming to implement the CNN where convolution usually takes most of the time. There are many zero values in feature maps and filters, which leads to redundant calculations and memory accesses if dense methods are used to compute convolution. Many works recently have made use of sparsity to skip the calculations for zero values to reduce the inference time of the CNN. On the graphics processing unit platform, current works cannot fully exploit the sparsity of the feature map and achieve satisfactory performance. Therefore, we design a new parallel strategy to transform the feature map into a new storage format to avoid the redundant computation of zero values on graphics processing units. Also considering the sparsity in the feature map, we propose a fused storage format to combine the convolution operation with the following pooling operation, to further improve the performance. We carry out experiments with mainstream CNN models and achieve better performance compared with cuDNN and cuSPARSE. For VGG-19, ResNet-50, DenseNet-121, and RegNetX-16GF, 1.97×, 2.23×, 2.74×, and 1.58× speedups respectively are obtained over cuDNN. The speedups over cuSPARSE respectively are 2.10×, 1.83×, 2.35×, and 1.35× when only using the first method.
1 INTRODUCTION

The Convolutional Neural Network (CNN) plays a crucial role in deep learning, which facilitates the development of computer vision [76], medical image classification [34], natural language processing [70], and recommender systems [95], among others. The CNN is also an essential part of many complex neural network models [14, 51]. However, it is time consuming for training and inference of the CNN. Improving the execution speed of the CNN is of great importance for accelerating its applications. Convolution operations usually take up a large part of the total execution time of the CNN, even more than 70% in well-known CNNs such as VGG, ResNet, and YOLO [47, 75]. Designing specific hardware architectures for convolution computation is a feasible way to accelerate the CNN [90, 91] (e.g., Tensor Cores [59, 96]). Some algorithmic optimization techniques are also developed, such as Im2col [12, 46], Fast Fourier Transform (FFT) [55], and Winograd [41]. The preceding acceleration methods are integrated into cuDNN, which is a state-of-the-art library for deep learning on Graphics Processing Units (GPUs) [58].

The convolution operation in the CNN refers to the process in which the convolution kernel samples on the feature map. The process of convolution contains a lot of multiplications and additions, so reducing these operations is effective for acceleration. Network pruning [66] and ReLU activation are common operations in CNNs, which result in a large number of zero values in the network. For the feature map, the ratio of zero values evolves [16] and can be more than 0.8 in the deep layers of the network after multiple epochs. The pursuit of precision in CNNs leads to dozens of epochs, so the large sparsity in the feature map is inevitable. The calculation of these zero values, however, is useless for the convolution result [71]. In other words, if we can skip the zero-value calculation in the convolution operation, this will reduce operations of multiplication and addition.

Some efforts focus on reducing the calculations of zero values in neural networks by designing new hardware architecture [19, 20, 45, 60, 92], which obtain outstanding acceleration effects. However, new architectures based on FPGA or ASIC have a relatively long development cycle, compared with the CPU or GPU. Some algorithms exploiting sparsity for convolution operations on a CPU are proposed and achieve considerable speedup over their dense counterparts [5, 26, 49, 61, 71]. The GPU is widely used for accelerating the CNN because of its strong computing power for parallelizable processes such as large-scale matrix multiplication based on the highly optimized cuBLAS [44, 67]. Current implementations of sparse convolution on a GPU are usually based on sparse libraries such as cuSPARSE [28, 43]. For the convolution layer, feature maps and filters can be processed with three steps—extension, compression, and sparse matrix computation—by cuSPARSE.

However, exploiting sparsity in convolution operation can hardly achieve satisfactory performance when the CNN is implemented on a GPU [33], and very limited speedup over cuBLAS-based convolution methods is obtained [86, 96]. The reasons are as follows. First, the preceding three steps are separately completed on the GPU, so the data are loaded from and stored into global memory at least three times. When using cuSPARSE, the data even need to be transferred between the CPU and GPU. Second, the cost of real-time compression affects the performance. Third, sparse matrix computation is less efficient than its dense counterparts on GPUs [10].

However, the pooling operation usually starts after the convolution results are transferred from the GPU to the CPU in traditional CNN implementations. This increases traffic not only between global memory and shared memory on the GPU but also between the CPU and GPU. To address this problem, some works [4, 21, 36, 62, 79] consider integrating different CNN layers into one GPU kernel to decrease communication overhead. However, the adjacent layers are simply put together in one kernel, and the sparsity for convolution operation is not considered. In this article, we
propose two novel methods to accelerate the CNN on GPUs. Our contributions can be summarized as follows:

- We propose a novel storage format—**Extended and Compressed Row (ECR)**—for sparse feature maps. We design a convolution algorithm based on ECR, which calculates convolution by skipping zero values and reduces the amount of computation. Furthermore, the ECR method can complete extension, compression, and sparse matrix computation by only accessing global memory once.
- We also propose another storage format: **Pooling-pack Extended and Compressed Row (PECR)**. Besides exploiting sparsity, the convolution layer and pooling layer are computed together, which effectively reduces not only the traffic between the CPU and GPU but also the traffic from off-chip memory to on-chip memory of the GPU.
- We evaluate the proposed algorithms on the GPU platform. The result shows that our methods can achieve state-of-the-art speedup over cuDNN. For VGG-19, ResNet-50, DenseNet-121, and RegNetX-16GF, 1.97×, 2.23×, 2.74×, and 1.58× speedups respectively are obtained over cuDNN. The speedups over cuSPARSE respectively are 2.10×, 1.83×, 2.35×, and 1.35× when only using ECR.

The rest of this article is organized as follows. Section 2 presents the background. Section 3 discusses the related work. Section 4 introduces the motivation. Section 5 describes the proposed ECR format and its convolution method. Section 6 describes the PECR format and the corresponding convolution and pooling method. Section 7 introduces the **Optional Convolution and Pooling Algorithm (OCPA)**, which can use both ECR and PECR for an entire network. Section 8 evaluates the proposed methods on several CNN models. Section 9 concludes this article.

### 2 BACKGROUND

In this section, we first introduce GPUs and **Compute Unified Device Architecture (CUDA)**. Then, we present the convolution operation and the pooling operation for CNNs. The notations used in the article are described in Table 1.

| Notations | Description |
|-----------|-------------|
| B_l       | Block id of the GPU thread block |
| T_i       | Thread id of the GPU thread |
| i_w       | Width of the feature map |
| h_i       | Height of the feature map |
| k_w       | Width of the kernel |
| h_k       | Height of the kernel |
| p_w       | Width of the pooling window |
| h_p       | Height of the pooling window |
| c_s       | Stride size for convolution |
| p_s       | Stride size for pooling |

2.1 GPU/CUDA Platform

GPUs are widely used to meet the needs of high-performance computing for many applications, such as scientific computing, deep learning, bioinformatics [78], and so on. One GPU usually contains multiple **Streaming Multiprocessors (SMs)**, and each SM contains multiple **Streaming Processes (SPs)** [48]. Each SM can access a register file that works at the same speed as the SP. Usually, each SM contains an L1 cache, and all SMs shared an L2 cache. Each SM also has a shared memory that is similar to the L1 cache, but its data replacement is controlled by the programmer. The shared memory is shared between SPs within the same SM. Global memory is off-chip and can be used for data transfer between the GPU and CPU. The CPU can access the global memory through the PCI-E or AXI bus. The latency of transferring data from the CPU to GPU and from global memory to shared memory is very high, so it is beneficial to put reusable data in shared
memory instead of frequently visiting CPU memory or global memory. CUDA is a programming platform designed for GPU architecture. CUDA makes parallel programming on the GPU more acceptable and promotes the development of parallel applications. On the CUDA platform, all threads are contained in a thread grid, which consists of multiple thread blocks. The threads in a thread block share the same shared memory space. According to the GPU’s characteristics, threads are organized in the form of a warp, which generally includes 32 threads [40, 68].

2.2 Convolution on the GPU

Convolution calculations have been converted to **G**eneral **M**atrix **M**ultiplications (GEMM) on the GPU [12]. Using the GPU platform to calculate GEMM has been deeply studied [27, 46]. Im2col is a common way to compute convolutions in CNN frameworks such as Caffe [37], TensorFlow [1], PyTorch [62], and cuDNN [12]. This method needs to transform the input feature maps \( I \) into an extended matrix \( B \) so that the convolution results can be obtained from GEMM:

\[
O = CONV(F, I) = A \cdot B = A \cdot \text{Im2col}(I),
\]

where \( O \) is the output of convolution, \( F \) is the convolution filters, \( A \) is a matrix that contains the filters \( F \), and \( B \) is the result of applying the Im2col transform to the input feature map \( I \) according to the filter size and stride.

As shown in Figure 1, the feature map is divided into three large convolution block rows (B1, B2, and B3), each of which corresponds to one row of final convolution results. One thread block of the GPU is assigned to compute one convolution block row. In each convolution block row, the convolution kernel moves horizontally. Therefore, each convolution block row is divided into three convolution windows, each of which corresponds to one convolution result. Each convolution result is computed by one GPU thread (T1, T2, or T3). The values in the convolution window are extended to one row of a matrix, and the convolution kernel is extended to a vector. In this way, the convolution calculation is converted to matrix-vector multiplication. The result of the matrix-vector multiplication corresponds to a row of convolution results. Matrix-vector multiplication is much faster than convolution operation on GPUs, so the calculation speed is substantially improved. Accordingly, convolution operation with multiple convolution kernels can be transformed to matrix-matrix multiplication, which is also quite suitable for GPU computing. In recent years, there have been some optimization methods for convolution on GPUs, which will be discussed in related work.

2.3 Pooling Operation

To reduce dimensions of the output from convolution layer and prevent overfitting, the pooling layer is added after the convolution layer in most CNNs. CNNs usually have three kinds of pooling operations: mean-pooling, max-pooling, and stochastic-pooling. Similar to the convolution operation, the pooling operation also has a sliding window on the feature map, but no multiplication operation is required in this window. In the sliding window, mean-pooling takes the average value from all values in the window. Max-pooling takes the maximum value from all values in the window. Stochastic-pooling gives a probability to each value in the window, then the one with the highest probability is selected.

3 RELATED WORK

The CNN is an important kind of deep neural network, which can be applied in a broad range of domains. In this section, we summarize and classify the methods for accelerating CNNs.
3.1 Dense Methods for Accelerating CNNs

Dense methods for accelerating CNNs mainly refer to accelerating matrix multiplication for convolution with a dense storage format. The dense methods can be divided into two categories: CPU or GPU and FPGA or ASIC.

3.1.1 CPU or GPU. Direct convolution needs less memory space than the GEMM-based method, but it is not efficient. Im2col first extends the feature maps and filters, then transforms convolution into matrix multiplication. This method gets a good acceleration effect because the GPU is good at accelerating GEMM. However, Im2col cannot achieve satisfactory performance for small feature maps because GEMM for small matrices cannot fully exploit the computation ability of the GPU. Li et al. [46] design a new coordinated tiling and batching algorithm, which significantly improves the computational efficiency of small matrix in deep layers of CNNs. Anderson et al. [6] propose two novel algorithms for convolution using GEMM that respectively require $O(MHW)$ and $O(KW + CH + CW)$ additional space. By reducing the space requirements of convolution, they improve data locality and parallel performance. FFT is a computational tool commonly used for signal analysis. FFT-based methods compute convolutions as pointwise products in the Fourier domain while reusing the same transformed feature map many times [55]. The time
The sparsity of the feature maps for VGG networks. The blue bar is the original feature map, and the gray bar is the feature map after matrix transformation as in lm2col.

complexity of the FFT-based method is reduced compared with direct convolution. FFT-based methods usually perform better at a larger filter size. Winograd is a method based on Winograd minimal filtering algorithms. The Winograd method dramatically reduces the arithmetic complexity compared with direct convolution \[41\]. Winograd-based methods perform well for small kernels and small batch sizes. Although the dense methods that convert convolution to GEMM can better exploit the strong computing power of a GPU, the large sparsity in the feature map is ignored. The methods proposed in this article can skip the zero-value calculation in convolution, which will greatly reduce operations of multiplication and addition.

3.1.2 FPGA or ASIC. New architectures based on FPGA \[56, 69\] or ASIC are usually more efficient than CPU or GPU platforms. Chakradhar et al. \[7\] propose the first CNN architecture to achieve real-time video stream processing. DianNao \[9\] is an accelerator for large-scale CNNs, optimized on both performance and energy. Alwani et al. \[4\] construct a fused-layer CNN accelerator that fully exploits data reuse between adjacent CNN layers. Eyeriss is an accelerator for state-of-the-art CNNs. It optimizes the energy efficiency of the entire system for various CNN shapes \[11\]. PRIME can accelerate a CNN in ReRAM-based main memory with significant performance improvement and energy savings \[13\]. FpgaConvNet is an end-to-end framework for the optimized mapping of CNNs on FPGAs \[77\]. The tensor processing unit is a custom ASIC with a MAC matrix multiply unit and large software-managed on-chip memory \[38\]. Thinker is an energy-efficient reconfigurable hybrid neural network processor fabricated in 65-nm technology \[87\]. Parana is a neural processor for hybrid neural network acceleration in consideration of thermal problem of 3D DRAM \[88\]. PipeLayer is a ReRAM-based PIM accelerator for CNNs that supports both training and testing \[73\]. ShiDianNao is a CNN accelerator that is placed next to a CMOS or CCD sensor \[24\]. Convolution Engine is specialized for the convolution-like dataflow that is common in computational photography, image processing, and video processing applications \[64\]. MAPLE is an accelerator for machine learning algorithms such as the CNN. It has hundreds of simple PEs laid
out in a two-dimensional grid [53]. Peemen et al. [63] propose a memory-centric accelerator for CNNs. nn-X is a scalable and low-power coprocessor for real-time execution of CNNs [29]. UniWiG [39] is a unified architecture where GEMM can be accelerated using PEs. It can efficiently utilize FPGA hardware resources when computing all layers of the CNN. Chang et al. [8] implement a new architecture that applies different quantization schemes for different rows of the weight matrix for accelerating a CNN on the FPGA platform [8]. Tensor Core [54] in GPUs is good at accelerating CNNs by optimizing GEMM. Tensor Cores use mixed precision to compute GEMM, with only a minimal loss of precision in the output.

3.2 Sparse Methods for Accelerating CNNs

The sparsity of CNN mainly comes from the commonly used ReLU activation function and pruning. The sparsity of feature maps in deep network layers is usually more than 0.8, as shown in Figure 2. Therefore, exploiting sparsity has great potential to accelerate CNNs. The methods of accelerating CNNs by sparsity can also be classified into CPU/GPU and FPGA/ASIC.

3.2.1 CPU or GPU. Although the deep layers in CNNs have high sparsity, this unstructured sparsity is difficult to exploit, so some algorithms have been developed to optimize sparse matrix multiplication (SpGEMM) [35, 71]. Niu et al. [57] propose a tiled parallel SpGEMM algorithm named TileSpGEMM. The main feature of TileSpGEMM is that the input and output sparse matrices are stored as multiple non-empty sparse blocks of the same size. SparseRT is a code generator that leverages unstructured sparsity to accelerate sparse linear algebra operations in deep learning inference on GPUs [80]. Balanced Sparsity is a novel fine-grained sparsity approach to achieve high model accuracy with commercial hardware efficiently [86]. PCONV has a new sparsity dimension—fine-grained pruning patterns inside the coarse-grained structures [50]. Zhao et al. [94] effectively bridge the gap between deep learning and the special needs of the high-performance computing problem through a set of techniques on matrix representations, deep learning structure, and cross-architecture model migrations. Daultani et al. [17] propose a new computation- and memory-efficient convolution algorithm for the inference phase (Sparse Direct Convolution) and a new representation for sparse filters (Compressed Sparse Offset) [17]. Skip-Convolutions leverages a large number of redundancies in video streams and save computations [31]. Spartan is a lightweight hardware/software framework for accelerating DNN training on GPUs [22], which can exploit activation sparsity detected during training. Song et al. [74] propose a sensitivity-aware dropout method to achieve greater forward and backward training acceleration for a CNN while retaining the accuracy. FalCon is a novel sparsity computing scheme that can well adapt to the practical sparsity patterns while still maintaining efficient computing [83]. Ahrens et al. [2] propose an automatic asymptotic scheduler for sparse tensor programs. In practice, current implementations of sparse convolution on a GPU are usually based on sparse libraries such as cuSPARSE [28, 42, 43]. The cuSPARSE library contains a set of basic linear algebra subroutines used for handling sparse matrices. When using cuSPARSE to calculate convolution, a three-step processing is performed on the feature maps and convolution kernels, namely extension, compression, and sparse matrix computation. Previous sparse methods can hardly outperform cuBLAS-based convolution methods. Compared with the previous sparse methods, the sparse methods in this article try to further reduce the data transfer not only between the CPU and GPU but also between off-chip memory and on-chip memory of the GPU.

3.2.2 FPGA or ASIC. New hardwares are designed to exploit sparsity in CNNs mostly based on FPGA or ASIC [72]. Earlier works [3, 93] only explore the sparsity of the feature maps, which is caused by the ReLU activation function. These schemes take advantage of one-sided sparsity, with only zeros in the feature maps, while the filter values remain unchanged. However, with the
application of pruning, filters also exhibit sparsity. Gondimalla et al. [30] utilize zeros in both feature maps and filters to achieve more efficient sparse computation. Sparse Tensor Core [96] is an algorithm and hardware co-design, which is implemented on the NVIDIA A100 GPU. PermCNN is an energy-efficient hardware architecture for permuted diagonal structured CNNs [18]. TensorDash is a hardware-based technique that enables data-parallel MAC units to take advantage of sparsity in their input operand streams [52]. Dey et al. [20] propose a reconfigurable hardware architecture to accelerate the training of a CNN by sparsity. EIE is an energy-efficient inference engine that performs inference on the compressed network model and accelerates the resulting Sparse Matrix-Vector Multiplication (SpMV) with weight sharing [32]. Scalpel customizes DNN pruning to the underlying hardware by matching the pruned network structure to the data-parallel hardware organization [89]. FuseKNA eliminates both ineffectual and repetitive additions in bit-serial computation by exploiting bit repetition and bit sparsity in weights, for both convolutional and fully connected layers [84]. GoSPA is an energy-efficient high-performance globally optimized sparse CNN accelerator [19]. SIGMA is a flexible and scalable architecture that offers high utilization of all its PEs regardless of kernel shape and sparsity [65]. CNV uses hierarchical data-parallel units, allowing groups of lanes to proceed mostly independently enabling them to skip over the ineffectual computations [3]. Sparse ReRAM Engine exploits both weight and activation sparsity to eliminate ineffectual computation [85].

4 MOTIVATION

The CNN extracts the characteristic information of input data through convolution layers. The convolution kernel performs multiplications and additions in the sample area throughout the feature map. If the size of feature map is $i_w \times i_h$ and the kernel size is $k_w \times k_h$, a convolution operation requires $num_{mul}$ multiplications and $num_{add}$ additions, according to Equation (1) and Equation (2), respectively.

$$num_{mul} = \left( \frac{i_w - k_w}{c_s} + 1 \right) \left( \frac{i_h - k_h}{c_s} + 1 \right) (k_w k_h)$$  \hspace{1cm} (1)

$$num_{add} = \left( \frac{i_w - k_w}{c_s} + 1 \right) \left( \frac{i_h - k_h}{c_s} + 1 \right) (k_w k_h - 1)$$  \hspace{1cm} (2)

Feature maps of the deeper convolution layers are usually smaller, and the size can be as small as $5 \times 5$. Convolution calculation on a GPU is generally converted into GEMM, which is often more efficient for a large matrix. Because the number of GPU threads is small due to the limited size of the feature map, GEMM cannot fully exploit the GPU’s computation ability.

The sparsity of the deep feature map is relatively large due to ReLU activation and pruning operations. We can see from Figure 2 that the sparsity of the feature map that will enter the convolution layer can reach more than 0.7 for deep layers in the network [81]. When the feature map is extended as in Im2col, the matrix is even more sparse (gray bar). The traditional methods such as Im2col will calculate these zero values, which are useless for the final convolution result.

Although there are some traditional compression formats for sparse matrices such as CSR [25], they cannot fully adapt to the characteristics of convolution operations. Sparse Tensor Core can compute sparse matrix multiplication on GPUs [96]. However, Sparse Tensor Core uses an algorithm that prunes the matrix to a 2:4 sparse pattern. That means that two values must be zero in each contiguous block of four values. Although such a method will improve the inference speed of CNNs, it will cause a decrease in accuracy.

To address the preceding problems, we reduce the number of multiplications and additions in the convolution operation by compressing the feature map. To reduce the time consumption, we transform the traditional matrix conversion operation [12] into a compression operation that does
not affect the accuracy of CNNs. After compression, the feature map is transformed to a storage format fully considering the characteristics of convolution operations, and the convolution calculation is transformed into SpMV [82], which eliminates the calculation of redundant zero values. Furthermore, the process of data format transformation and SpMV only require one-time global memory access.

However, traditionally, convolution layers are usually calculated in an independent GPU kernel. After the convolution results are transferred to CPU memory, the calculation of pooling layer is started, such as in Caffe [37] and PyTorch [62]. This will increase the traffic between the CPU and GPU. As shown in Figure 3, the time for transferring data between the CPU and GPU occupies a considerable proportion in the entire convolution and pooling calculation process, especially for the first several layers. If the time consumption of data transfer between the CPU and GPU during convolution and pooling operations can be reduced, the total time of the CNN can be reduced effectively. Furthermore, the time will be further reduced if the data transfer between global memory and shared memory is reduced on the GPU.

5 SPARSE CONVOLUTION METHOD ON A GPU

In this section, we introduce a sparse convolution method for the CNN on a GPU. First, we present the whole procedure of CNN forward computing with the sparse convolution method. Then, a new storage format suitable for sparse convolution calculation on a GPU is proposed. Last, the convolution method based on the new storage format is described in detail.

5.1 Whole Procedure for CNN Forward Computing

To better understand the proposed method, we design an algorithm procedure with only one-time data transfer to reduce off-chip memory traffic (traffic between the CPU and GPU, and traffic between global memory and shared memory on a GPU) for CNN forward computing. The algorithm procedure is as follows:

Step 0: Transfer input data (images/feature maps and filters) from the CPU to GPU. Start the GPU kernel.

Step 1: Load input data from global memory to shared memory and transform the data into the new format.

Step 2: Perform SpMV for the convolution layer. One thread computes one convolution result.
Fig. 4. A novel storage format (ECR) for one feature map and one kernel. The size of the feature map is $5 \times 5$, the kernel size is $3 \times 3$, and the stride is 1.

**Step 3**: Perform pooling operations if there is a pooling layer after the convolution layer, and output the pooling result to global memory.

**Step 4**: Go to step 1 unless it is the last pooling layer.

**Step 5**: Complete the computation for remaining layers.

**Step 6**: Transfer the result from the GPU to the CPU.

5.2 ECR Storage Format

Zeros in feature maps for the convolution operation can lead to useless multiplications and additions. Therefore, we convert the feature map into a new storage format (ECR), then the convolution can be converted to SpMV. As shown in Figure 4, the feature map is divided into three convolution block rows (B1, B2, and B3) according to the size of the stride $c_s$ and the height of convolution kernel $k_h$. One convolution block row corresponds to one row of final convolution results. One thread block on the GPU is assigned to compute one convolution block row. In each convolution block row, the convolution kernel moves horizontally. Therefore, each convolution block row is divided into three convolution windows, and each convolution window corresponds to one convolution result. Each convolution result is computed by one thread (T1, T2, or T3) on the GPU.

One block row, B1, is extracted to describe the new storage format. We store the three non-zero values in the convolution window of T1 into $F_{data}$ of B1 and store the corresponding values in the convolution kernel into $K_{data}$ of B1. The non-zero values of all remaining convolution windows are stored into $F_{data}$ in turn, along with the corresponding convolution kernel values into $K_{data}$. Additionally, the number of non-zero values in each convolution window is stored in $Ptr$, which is also the number of multiplications required for each thread. If there is no non-zero value for a convolution window, a value of $-1$ should be stored in $Ptr$ of B1 for markup. In all, non-zero values are stored in $F_{data}$, kernel values are stored in $K_{data}$, and the number of non-zeros values are stored in $Ptr$. Because the filter is also extended with a feature map, bank conflicts will be reduced when all threads visit the filter together in shared memory.
5.3 Load and Transform Data

After images/feature maps and filters are transferred from the CPU to the GPU’s global memory, the GPU starts its work. The feature maps are loaded, extended, and transformed into ECR format at the same time (see Figure 4). After that, the feature map and the filter in ECR format are stored in shared memory.

As shown in Figure 5, feature maps are stored in global memory as one-dimensional arrays for continuous access by adjacent threads. In this way, non-zero values of feature maps are loaded from global memory to shared memory, which can reduce the time of global memory access. This advantage of coalesced global memory access performs best when the convolution stride is 1.

For a single feature map, we can allocate \( \frac{h_k - k_h}{c_s} + 1 \) blocks, each of which contains \( \frac{w_k - k_w}{c_s} + 1 \) threads. As shown in Algorithm 1, the algorithm of one thread is described for converting its corresponding map and filter to ECR format. \( F_{data} \) and \( K_{data} \) are declared shared memory. In Algorithm 1, \( temp \) is a counter for non-zero values in the feature map. Each thread needs to read \( k_w \times k_h \) values of feature map from global memory (lines 2 and 3). Line 4 sets the address \( offset \) that this thread needs to access in global memory. \( offset \) equals \( mapping(thread\_idx, data\_idx) \), which calculates the relationship between \( thread\_idx \) in blocks and \( data\_idx \) in global memory. Line 5 judges the data value corresponding to the global memory position \( offset \). If it is a non-zero value, it is stored in \( F_{data} \) with the position \( thread\_idx \times k_w \times k_h + temp \), and the corresponding value in the convolution kernel is stored in the corresponding position of \( K_{data} \) (lines 6–8). After the loop, the number of non-zero values is stored in \( Ptr \), and –1 is stored if there is no non-zero value (lines 12–16).

**Algorithm 1:** Storage format conversion algorithm for ECR

```plaintext
1: temp ← 0
2: for i = 0 to k_h do
3:     for j = 0 to k_w do
4:         offset ← mapping(thread_idx, data_idx)
5:         if input[offset]! = 0 then
6:             F_data[thread_idx * k_w * k_h + temp] ← input[offset]
7:             K_data[thread_idx * k_w * k_h + temp] ← kernel[i + j * k_w]
8:             temp ++
9:         end if
10:     end for
11: end for
12: if temp! = 0 then
13:     ptr[thread_idx] ← temp
14: else
15:     ptr[thread_idx] ← −1
16: end if
```
5.4 Perform SpMV for Convolution

In this section, we describe the algorithm for sparse convolution calculation based on ECR and use Figure 6 as an example to analyze how the number of multiplications and additions is reduced.

In the previous section, we obtained a new data format ECR, $F_{data}$ for the feature map, $K_{data}$ for kernel data, and $Ptr$ for the number of non-zero values. As shown in Figure 6, we can consider $F_{data}$ as a sparse matrix and $K_{data}$ as a vector with varying lengths. The length of the vector is the same as the corresponding value in $Ptr$. Therefore, the convolution operation is converted to a variant of SpMV, and zero values in the feature map are skipped without affecting the convolution result.

As shown in Figure 6, for GPU implementation, one thread multiplies a row in the compressed feature map (A) with the corresponding vector in the kernel map (B) to obtain a value in a convolution result matrix (C). Therefore, a thread block contains $(\frac{tw-kw}{cw} + 1)$ threads and can get one row of the final convolution results. After parallel calculation by multiple thread blocks, the convolution result for the whole feature map can be obtained.

The pseudo-code for a single thread to get a convolution result is described in Algorithm 2. Line 1 accesses the corresponding $ptr$ vector in the shared memory to determine whether there are non-zero values stored in $F_{data}$. If $ptr[\text{thread\_idx}]$ is $-1$, it is immediately judged that no operation is needed, and the output is 0 (line 2). If the value stored in $ptr[\text{thread\_idx}]$ is not $-1$, the values in $K_{data}$ and $F_{data}$ are accessed in turn and multiply-add operations are performed (lines 4–6). The convolution result is finally obtained and stored into global memory for the computation of next layer (e.g., the pooling layer).

As shown in Figure 4 and Figure 6, for three convolution block rows (B1, B2, and B3), the conventional algorithm requires 24 additions and 27 multiplications, whereas our algorithm only requires 7 additions and 10 multiplications, reducing 71% of additions and 63% of multiplications. Additionally, $K_{data}$, $F_{data}$, and $ptr$ are all stored in shared memory. Therefore, the proposed method can greatly improve the speed of convolution and accelerate the whole CNN.

**Algorithm 2**: Convolution algorithm for ECR

```plaintext
if ptr[\text{thread\_idx}] == -1 then
    output[\text{thread\_idx} + \text{block\_idx} * \text{blockDim.x}] \leftarrow 0
else
    for i = \text{thread\_idx} * k_w \ast k_h to \text{thread\_idx} * k_w \ast k_h + ptr[\text{thread\_idx}] - 1 do
        output[\text{thread\_idx} + \text{block\_idx} * \text{blockDim.x}] + = F_{data}[i] * K_{data}[i]
    end for
end if
```
5.5 Other Steps for CNN Forward Computing

The convolution results are processed by ReLU before they are outputted to the global memory. As threads in different thread blocks cannot communicate through shared memory, we have to store the activation results into global memory before the pooling operation starts. Because the pooling operation itself takes up only a little time, we do not discuss its implementation here. After pooling results are outputted to global memory, a new round is started by loading the new feature map and filter to shared memory (Figure 5), and transforming them into ECR format for the next convolution layer. This process is repeated until all convolution layers and pooling layers are finished.

6 COMBINING CONVOLUTION AND POOLING

Traditionally, after the convolution results are transferred from the GPU to the CPU, the calculation of the pooling layer is started. This will increase the cost of data transfer. In this section, we propose an optimization method that not only exploits the sparsity of feature map but also calculates convolution and pooling together without transferring intermediate results.

6.1 Whole Procedure for CNN Forward Computing

For the forward computing of the CNN, the algorithm procedure should also try to ensure one-time data transfer from the CPU to the GPU. Therefore, the traffic between the CPU and GPU is reduced. For better understanding of the proposed method, we present the whole process of CNN forward computing as follows:

**Step 0**: Transfer the images and filters from the CPU to the GPU. Start the GPU kernel.

**Step 1**: Load data (images/feature maps and filters) from global memory to shared memory. At the same time, transform the data to the new format.

**Step 2**: Perform SpMV for the convolution layer. One thread computes one convolution result.

**Step 3**: Several convolution results (e.g., 4 ($2 \times 2$)) are used to get a pooling result, which is stored to global memory.

**Step 4**: Go to step 1 unless it is the last pooling layer.

**Step 5**: Complete the computation for remaining layers.

**Step 6**: Transfer the final result from the GPU to the CPU.

6.2 Sparse Storage Format Considering Both Convolution and Pooling

In the traditional CNN, the result of the convolution operation will enter the pooling layer after the activation operation. If the convolution results are transferred to the CPU side, and then again to the GPU side for pooling operations, it will increase the overall CNN calculation time due to the bandwidth limitation between the GPU and CPU. Therefore, we redesign the calculation process and combine the pooling operation with the convolution calculation by proposing a new storage format that can exploit the sparsity of the feature map.

The new storage format is PECR. As shown in Figure 7, the feature map is horizontally divided into two large pooling-pack rows (B1 and B2) according to the size of the stride $c_s$ and the height of convolution kernel $k_h$. One pooling-pack row corresponds to one row of pooling results. One thread block on GPU is assigned to compute one pooling-pack row. Each pooling-pack row is divided into two pooling windows, and each pooling window corresponds to one pooling result. Each pooling result is obtained by four threads (T1, T2, T3, and T4) on the GPU.

Non-zero values of all convolution windows in the corresponding pooling window are stored into Data in an order of left to right and top to bottom. To complete the convolution calculation, the index pointing to corresponding value in the filter is stored in Index. Using such a storage...
Fig. 7. PECR format. The size of feature map is $5 \times 5$. The size of convolution kernel is $3 \times 3$. The size of pooling window (PW1, PW2, PW3, and PW4) after convolution is $2 \times 2$. The stride of both convolution and pooling is 1.

method, each thread will process a sub-feature map with the size of $k_w \times k_h$ in the original feature map. $k_w \times k_h$ is the size of the convolution kernel. A pooling window with the size of $T_w \times T_h$ will get a pooling result. $T_w$ equals $k_w + c_s(p_w - 1)$, and $T_h$ generally equals $T_w$. Each thread in the pooling window will process one convolution window. For example, there are $2 \times 2$ pooling windows (PW1, PW2, PW3, and PW4), and there are $2 \times 2$ threads in a pooling window (T1, T2, T3, and T4) in Figure 7.

### 6.3 Load and Transform Data

The feature maps and filters are loaded from global memory to shared memory in a coalesced way similar to Figure 5. At the same time, the input data are transformed to PECR format. The process of loading and converting data to PECR format for one GPU thread is described in Algorithm 3. Each thread processes one convolution window. For each convolution window ($k_w \times k_h$) in the feature map, the thread loads non-zero values from global memory to shared memory and computes the according index in the filter. Therefore, the time complexity of Algorithm 3 is $O(k_w \times k_h)$. Each feature map is processed by $p_w \times p_h \times n_o^2$ threads, and $n_o$ is explained by Equation (3).

$$n_o = \frac{(I_w - k_w + c_s - c_s \times p_w + p_s \times c_s)}{p_s \times c_s}$$  \hspace{1cm} (3)

### 6.4 Convolution and Pooling

After the feature map and the filter are transformed to PECR format and stored in shared memory, the convolution and pooling operations are started. Based on PECR format, each thread performs one SpMV operation to get one convolution result (Figure 8). Four threads in the same warp get
Algorithm 3: Convert feature map and filter into PECR format

1: \( \text{pos} \leftarrow \text{thread}_\text{id} \times k_w \times k_h \)
2: \( \text{cnt} \leftarrow 0 \)
3: \( \text{num} \leftarrow 0 \)
4: for \( i = 0 \) to \( k_h \) do
5: for \( j = 0 \) to \( k_w \) do
6: \( \text{offset} \leftarrow \text{mapping} (\text{thread}_\text{id}, \text{data}_\text{id}) \)
7: if \( \text{Input}[\text{offset}] \neq 0 \) then
8: \( \text{Data}[\text{pos} + \text{cnt}] \leftarrow \text{Input}[\text{offset}] \)
9: \( \text{Index}[\text{pos} + \text{cnt}] \leftarrow i \times k_h + j \)
10: \( \text{cnt} + = 1 \)
11: \( \text{num} + = 1 \)
12: end if
13: end for
14: end for
15: \( \text{count}[\text{threadId}_\text{block}] \leftarrow \text{num} \)

Four convolution results in one pooling window. After that, ReLU is used as the activation function, and a value less than zero is set to zero. Then, maximum pooling is used to get the final pooling result. By combining convolution and pooling, the pooling result is obtained without data transfer between shared memory and global memory.

Algorithm 4 describes the convolution and pooling algorithm based on PECR. A thread needs to process one convolution window, \( p_w \times p_h \) threads compute one pooling result by the reduce operation (lines 9–13). Because different thread blocks cannot share data in shared memory, the pooling results are outputted to global memory. However, if only one thread block is started, the pooling results can be outputted to shared memory for computation of the next convolution layer.

7 DISCUSSION

Some CNN-based models have only a few pooling layers after convolution layers, such as ResNet, and some models have more pooling layers, such as VGG. Therefore, we can use the ECR method
for convolution layers without a following pooling layer and use the PECR method for convolution layers with a following pooling layer when we implement the proposed methods for an entire deep neural network model. We refer to the preceding strategy as OCPA.

We describe in detail the sparse convolution algorithm for one feature map and one kernel. The proposed ECR method can complete extension, compression, and sparse matrix computation by only accessing global memory once, which can effectively reduce the off-chip memory traffic. However, in the actual application, multiple feature maps and multiple kernels can be included in one convolution layer. Therefore, we implement different batch sizes in the experiment. The proposed algorithm can be extended to process this case by increasing the number of GPU threads. Since the amount of calculation in a single thread is reduced by the proposed algorithm, the calculation speed can also be improved with more threads. In addition, similar to Sparse Tensor Core in the Ampere architecture [15], the proposed method can also be applied to the hardware design.

We present the convolution and pooling algorithm with PECR for one feature map and one kernel. However, there are sometimes multiple feature maps and multiple filters. In this case, more traffic between the CPU and GPU is needed for cuDNN. Therefore, the time consumption of data transfer between the CPU and GPU can be further reduced with the proposed method, and the speedup will also be improved. It is worth noting that in the multi-channel convolution calculation, the data of other channels follow the same operation in turn. After all channels are compressed, SpMV starts to run to ensure that the calculation results are correct.

8 EXPERIMENTS

In this section, we present and analyze the experimental results of the proposed algorithms with various neural network models on the GPU platform (Table 2). The code for this work has been made open source.¹

8.1 Speed Comparison for Convolution Layers

In this section, we carried out speed comparison experiments for a single convolution layer.

As shown in Table 3, the ECR method is used to process convolution layers from different models, such as LeNet, AlexNet, GoogLeNet, VGG-19, and ResNet-50.

¹https://github.com/sunnchii0/OCPA.
We can see that the speedups for convolution layers are more than 2.2× compared with cuDNN (FAST), which can automatically choose a best implementation in cuDNN. The reasons are mainly in two aspects. First, for feature maps in deep networks, the size is very small compared with the initial input feature map. The traditional GEMM-based method in cuDNN is not suitable for matrix multiplication with small feature maps [41]. The ECR method reduces the amount of computation for a single thread according to the characteristic of sparsity and performs better for these small feature maps. Second, when using cuDNN to calculate convolution layers, it first uses Im2col to extend the feature map, then converts the convolution calculation into matrix multiplication. This increases the number of global memory accesses. By comparison, ECR reads the values used for each convolution result from global memory only once.

Furthermore, ECR achieves up to 3.99× speedup for a single convolution layer compared with the cuSPARSE-based method. Although the cuSPARSE-based method can skip the computation of zero values, it does not reduce the time for global memory accesses. For the cuSPARSE-based method, the feature map is first extended as in Im2col and then is converted to the CSR format that is inputted to cuSPARSE for the final convolution result. These operations are separated, causing the program to repeatedly read data in global memory. Note that the time of data-format conversion is included in the performance measurement of the ECR method.

### 8.2 Speedup for VGG, ResNet, DenseNet, and RegNet

Some convolution layers do not have a following pooling layer in some CNNs, so we can use OCPA to implement the entire network, and compare OCPA with cuDNN and the cuSPARSE-based method.
Fig. 9. Speed comparison between OCPA and other methods for VGG-19, ResNet-50, DenseNet-121, and RegNetX-16GF. The x-axis represents layers of neural networks. The y-axis represents the acceleration effect of different methods over GEMM.

8.2.1 Comparison with cuDNN. We implement the entire network using four cuDNN methods (GEMM, IMPLICIT_GEMM, FFT_TILING, and FAST), the Tensor Core based method, and OCPA. Figure 9(a) shows the time and the speedup of other methods over the GEMM method in cuDNN for VGG-19. There are 16 convolution layers in VGG-19, 5 of which have a following pooling layer. We use C+P to present a convolution layer with a pooling layer that is computed by the PECR method. For a single convolution layer, the ECR method is used. Note that the time of data-format conversion is also included in the performance measurement. We can see that OCPA achieves better performance than four cuDNN methods. On average, the speedup of OCPA over the baseline method cuDNN (GEMM) is 4.14×, and the speedup over cuDNN (FAST) is 3.91× for convolution layers and convolution+pooling layers in the VGG-19 network. In addition, the speedup over GEMM (Tensor Core) is 2.97×. The speedup of OCPA over cuDNN (FAST) is 1.97× for the entire VGG-19.

Figure 9(b) shows the time and the speedup of different methods over GEMM in cuDNN for ResNet-50. We can see that OCPA achieves the best performance. On average, the speedup of OCPA over cuDNN (GEMM) is 3.73×, and the speedup over cuDNN (FAST) is 3.53× for convolution layers and convolution+pooling layers in the ResNet-50 network. Furthermore, the speedup over GEMM (Tensor Core) is 2.44×. Last, we get that the speedup of OCPA over cuDNN (FAST) is 2.23× for the entire ResNet-50. Because VGG-19 has more convolution+pooling layers than ResNet-50, the average speedup of VGG-19 for convolution layers and convolution+pooling layers is larger than that of ResNet-50.

Figure 9(c) shows the speedup of other methods over the GEMM method in cuDNN and the computation time of each layer for DenseNet-121. There are 120 convolution layers in DenseNet-121, 3 of which have a following pooling layer in Transition layers. Several convolution layers are combined to form a DenseBlock, so we use the average time of the convolution layers in one DenseBlock to stand for the time of this DenseBlock. Using OCPA to implement the entire network, we can see that it has better performance than the other five methods. On average, the speedup of OCPA over cuDNN (GEMM) is 3.79×, and the speedup over cuDNN (FAST) is 3.48× for convolution layers and convolution+pooling layers in DenseNet-121. Since the feature maps of the first
few convolutional layers of the model are less sparse, the speedup is smaller than that of the subsequent convolutional layers. Furthermore, the speedup over GEMM (Tensor Core) is 3.74×, and the speedup of OCPA over cuDNN (FAST) is 2.74× for the entire DenseNet-121.

Figure 9(d) shows the speedup and the computation time of each layer using different methods for RegNetX-16GF, which has 71 convolution layers in total. Several convolution layers are combined to form a Block, so we use the average time of the convolution layers in one Block to stand for the time of this Block. SimpleStemIN (SS) is the first part of RegNetX-16GF, which contains a convolution layer. Since this model does not have a pooling layer immediately following the convolutional layer, we only use ECR in OCPA. On average, the speedup of OCPA over cuDNN (GEMM) is 2.96×, and the speedup over cuDNN (FAST) is 2.79× for convolution layers. Furthermore, the speedup over GEMM (Tensor Core) is 3.30×. Last, we get the speedup of 1.58× over cuDNN (FAST) for the entire RegNetX-16GF.

8.2.2 Comparison with cuSPARSE. We also use cuSPARSE to implement VGG-19, ResNet-50, DenseNet-121, and RegNetX-16GF. As cuSPARSE cannot compute pooling, OCPA only uses ECR as a comparison. Figure 10(a) shows the speedup of OCPA over cuSPARSE for VGG-19. On average, the speedup of OCPA over cuSPARSE is 3.28× for convolution layers in VGG-19. For the entire network of VGG-19, OCPA obtains 2.1× speedup. As Figure 10(b) shows, OCPA also gets better performance for ResNet-50 and achieves 3.3× speedup over cuSPARSE for convolution layers on average. For the entire ResNet-50, OCPA gets 1.83× speedup. As shown in Figure 10(c), the speedup of OCPA over cuSPARSE is 3.13× for convolution layers in DenseNet-121 on average. For the entire network of DenseNet-121, OCPA obtains 2.35× speedup. As Figure 10(d) shows, OCPA also gets better performance for RegNetX-16GF and achieves 2.49× speedup over cuSPARSE for convolution layers on average. For the entire RegNetX-16GF, OCPA gets 1.35× speedup. Compared with cuSPARSE, OCPA avoids redundant global memory accesses for extension and compression of feature maps, so OCPA can achieve better performance than cuSPARSE. Note that we only use ECR of OCPA to compare with cuSPARSE, since cuSPARSE cannot compute pooling layers. Based on this situation, the speedup of OCPA over cuSPARSE is lower than cuDNN.

8.3 Sensitivity Analysis for Sparsity

Both ECR and PECR use the sparsity of the feature map to accelerate the CNN, so we try to analyze how the different sparsities can affect the speedup of ECR and PECR. Figure 11(a) describes the
speedup of ECR over cuDNN (FAST). We can see that the speedup broadly becomes larger as the sparsity grows. Figure 11(b) shows the speedup of PECR over cuDNN (FAST). We can see that the speedup also broadly becomes larger as the sparsity increases. A larger sparsity leads to fewer computations for convolution, so the performance of both ECR and PECR becomes better. However, the methods in cuDNN are not affected by the sparsity, so the speedup becomes larger.

8.4 Sensitivity Analysis for Batch Size
We also test how the different batch sizes can affect the speedup of ECR and PECR. Figure 12(a) is the speedup of ECR over cuDNN (FAST). We can see that the speedup broadly becomes smaller as the batch size becomes larger. However, we can still achieve about 1.5× speedup even when the batch size is 128. Figure 12(b) is the speedup of PECR over cuDNN (FAST). We can see that the speedup also broadly becomes smaller as the batch size becomes larger. However, we can still achieve more than 6× speedup even when the batch size is 128. Both the time of our methods and the time of cuDNN increase as the batch size becomes larger. However, cuDNN may better exploit the parallelism of input data than our methods, so the speedup decreases.

8.5 Sensitivity Analysis for Stride
As shown in Figure 13, we also perform experiments with convolution strides of 1, 2, and 3 for all convolution layers of VGG-19 using ECR. Our method can achieve a speedup of 2.51× (stride is 1), 2.70× (stride is 2), and 2.83× (stride is 3) over cuDNN (FAST) on average. This means that a larger speedup is obtained when the stride is larger. Both the time of our methods and the time of cuDNN decrease as the stride becomes larger. The performance of cuDNN is more easily affected by the increase of stride than our methods, so a larger speedup is obtained when the stride is larger. We also find that the speedup increases as the network goes deeper (from conv1 to conv16 in the figure). The main reason is that the sparsity becomes larger as the network goes deeper.

8.6 Overhead of Data-Format Conversion
We carried out the experiment on data-format conversion overhead. As shown in Figure 14(a), the time of data-format conversion takes up 34% (DenseNet), 47% (RegNet), 30% (ResNet), and 17%
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9 CONCLUSION

In this article, two methods were proposed to optimize a CNN on GPUs. First, the method based on ECR skipped the computation for zero values in feature maps. Second, a PECR method was proposed not only to avoid computing zero values but also to compute the convolution layer and pooling layer together, which effectively reduces the time both for transferring data between the CPU and GPU and for loading data from global memory to shared memory on the GPU. Experimental results showed that the proposed OCPA method can reach 1.97×, 2.23×, 2.74×, and 1.58× speedup over cuDNN (FAST) for VGG-19, ResNet-50, DenseNet-121, and RegNetX-16GF, respectively. Over cuSPARSE, OCPA gets 2.10×, 1.83×, 2.35×, and 1.35× speedup for the preceding four CNN models.

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