Optimized Sharing of Coefficients in Parallel Filter Banks

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Abstract—Filters are the basic and most important blocks of most signal processing applications. In many applications, a group of parallel filters are used as filter banks. Parallel filter banks naturally require much more computations. Especially on chip applications, the resources are limited and shared among many algorithms. For this purpose, many filter optimization schemes are proposed to reduce the number of resources that filtering operations require. In this work, a novel optimization algorithm is proposed to decrease the number of operations in a group of parallel filters. The filter coefficients are grouped in a two stage process which enables increased coefficient sharing between different filters. The algorithm is capable of decreasing the number of registers, look-up tables and DSP48s by up to 50% of a regular parallel filter bank, without requiring increased sampling rate.

I. INTRODUCTION

Parallel filter banks consists of several filters that modify the input signal in order to extract information. They are widely used in signal processing applications, such as radar signal processing for target detection, communications for synchronization and matched receiver, image processing and convolutional neural networks.

In radar signal processing applications, matched filter banks are used for both wave compression and as optimum receivers to find the delay and the Doppler shift [1]. In radar systems, having higher bandwidth signals are almost always beneficial for better resolution, but this increases the number of filter coefficients, thus the computation demands [2], [3].

In communication systems, filter banks that consists of several matched filters are needed for the optimum receiver under additive noise [4]. In addition, synchronization is implemented through matched filters. In the synchronization algorithms, relatively long pseudo-random (PN) sequences are often used for low signal to noise ratio (SNR) robustness [5], [6], [7]. In code division multiple access (CDMA) based communication schemes (i.e. GPS), parallel filter banks are widely used as optimum receiver filters [8], [9].

Convolutional neural networks also use filter banks for the so called convolutional layers. In these layers, input data are subject to, mostly two dimensional filters [10], [11]. At each convolutional layer, learned weights form a set of filters. As the number of layers increase, the amount of data processed create a computationally exhausting problem. In addition to this, in neural networks, layers process data in parallel, which leads to parallel filter bank structures. Due to these properties of neural networks, GPUs are often preferred for their high parallel computational power [12], [13].

Traditionally, each filter in a parallel filter bank is implemented as a separate filter. This requires increased number of computation resources as the number of filters and number of coefficients per filter increase. Thus, it is important to decrease the computational needs of filter banks, especially on chip applications, where power and area are both limited and shared among many other algorithms. To the best of our knowledge, efficient filter design algorithms focus around efficient implementation of a single filter. Some of these implementation methods are, polyphase filter structures, sharing of numerically similar coefficients, or design of filter coefficients in order to increase the number of shared coefficients or systolic structures that trade increased sampling frequency with decreased resource usage.

Polyphase filters are one such example of efficient filter implementation, if filtering operation is paired with down sampling (decimation) or up sampling (interpolation) [14]. This type of implementation methods are widely used in multirate signal processing applications. Decimation operation is used in various digital signal processing applications, from speech processing to digital communications [14], [15], [16]. For example, in conventional interpolation applications, first input data is upscaled then is fed into a filter. This requires filter to process data faster than the original sampling rate of the signal. In polyphase representation upsampling and filtering operations are reversed using Noble’s identity. First filtering is applied and then output data is upscaled. This effectively decreases the rate of the filtering operation resulting in a power efficient method. However, polyphase filters simply divide a single filter into parts, effectively implementing them as a parallel filter bank. It does not decrease the number of operations at each clock cycle, thus does not offer area efficiency.

If the absolute value of filter the coefficients are the same, coefficient sharing within a filter is another approach of optimization [17], [18], [19]. Such algorithms are especially useful with symmetric filters. However, this method focuses on optimization of a single filter, not the filter bank as a whole. Moreover, even though the coefficients are shared, they require increased computation rate. These approaches trade number of multiplication operations (i.e. reduce the number of multipliers) with faster computation rate.

Another approach is to optimize the filter coefficients themselves so that they can be shared in an efficient manner. A case of this is the optimization of the filter coefficients itself so that they can be shared using any sharing algorithm. In [20], the filter coefficients are quantized in order to retain the
frequency properties of the filter and to share the polyphase filter coefficients as much as possible. In [21], [22], a pseudo-

random (PN) sequence is specifically designed so that the repeating structures can be efficiently exploited in order to
reduce the overall complexity of the filter.

In filters, the tapped delay line is one of the major resource heavy elements due to number of shift registers it requires. In
[2] the filter coefficients are grouped such that a smaller tapped delay line can be shared between groups and thus the length of the tapped delay line is significantly reduced. However, this algorithm also focuses on optimization of a single filter [22]. In a parallel filter bank, since input is the same for each filter, tapped delay line can be shared among all of the filters, however, this approach also does not decrease the number of computations required.

In this paper, an efficient filter bank design algorithm is presented, which aims to reduce the number of computation operations needed for a set of filters that use PN sequences as filter coefficients. Algorithm presented does not increase the rate of the system like conventional coefficient sharing algorithms as in [17], [18], [19]. Additionally, algorithm also does not require exploitation of polyphase representation as in [14], [15], [16]. The algorithm’s aim is to share coefficients between a number of filters according to a two step procedure. Coefficients of filters are simply grouped and rearranged. The algorithm significantly reduces the number of addition operations with its novel approach. In addition to this, algorithm enables much more flexible applications. It can be combined with any of the optimization algorithms aforementioned in this paper. One major example of coefficient sharing in expense of processing rate is also presented in this paper.

The algorithm can also be extended to filters with any value for their coefficients, from PN sequences by quantizing the absolute value of the coefficients. Such implementation of the algorithm not only reduces the number of summations, but also the number of multiplications.

The paper is organized as follows, in Section II the algorithm is presented for filters with PN sequences as their coeffi-
cients. In Section III optimization bounds of the algorithm is formulated, and in Section IV FPGA implementation for several cases are shown as an example for the efficiency of the algorithm. Finally we conclude this paper in Section VI.

II. COEFFICIENT SHARING BETWEEN FILTERS IN A
PARALLEL FILTER BANK

For a PN sequence filter, coefficients are exclusively ±1, i.e. \( h_k[m] = \pm 1 \forall m \in \mathbb{Z}^+ \).

For a one-dimensional signal \( x \), filtering is defined through the following convolution operation,

\[
y[n] = x[n] * h[n] = \sum_{m=0}^{M} x[n-m]h[m],
\]

where, \( h \) is the filter and \( y \) is the output of the filtering operation for this filter. Since, PN filter coefficients are either 1 or -1 we define the following sets:

\[
S_1 = \{m|h[m] = 1\} \quad \text{(2a)}
\]

and

\[
S_0 = \{m|h[m] = -1\} \quad \text{(2b)}
\]

Rearranging the summation order in Eq (1), we obtain the following operation:

\[
y[n] = \sum_{m \in S_1} x[n-m] - \sum_{m \in S_0} x[n-m] \quad \text{(3)}
\]

The total number of summations to implement Eq (3) is equal to the summations in Eq (1). Rearrangement of the order of the summations as in Eq (3) would only require proper handling of the tapped delay line of the filter structure which does not introduce any additional resource requirement.

Let’s assume there are two parallel filters in a filter bank: \( h_1 \) and \( h_2 \). From the coefficients of such filters we define the following four sets:

\[
S_{00} = \{m|h_1[m] = -1 & h_2[m] = -1\}, \quad \text{(4a)}
\]

\[
S_{01} = \{m|h_1[m] = 1 & h_2[m] = -1\}, \quad \text{(4b)}
\]

\[
S_{10} = \{m|h_1[m] = -1 & h_2[m] = 1\}, \quad \text{(4c)}
\]

\[
S_{11} = \{m|h_1[m] = 1 & h_2[m] = 1\}. \quad \text{(4d)}
\]

We then rewrite the convolution operations for these two filters as follows:

\[
y_1[n] = -\sum_{m \in S_{00}} x[n-m] + \sum_{m \in S_{01}} x[n-m]
- \sum_{m \in S_{10}} x[n-m] + \sum_{m \in S_{11}} x[n-m] \quad \text{(5a)}
\]

and

\[
y_2[n] = -\sum_{m \in S_{00}} x[n-m] - \sum_{m \in S_{01}} x[n-m]
+ \sum_{m \in S_{10}} x[n-m] + \sum_{m \in S_{11}} x[n-m] \quad \text{(5b)}
\]

From Eq (5), we see that in order to implement two different filters in a parallel filter bank we needed to implement only four distinct summations. We then sum or subtract the results of these summations in order to obtain \( y_1 \) and \( y_2 \). We extend the idea further into \( K \) filters. For this we first construct the indices set for each filter as follows:

\[
S_0^k = \{m|h_k[m] = -1\} \quad \text{(6a)}
\]

and

\[
S_1^k = \{m|h_k[m] = 1\}, \quad \text{(6b)}
\]

where \( k \) is the index of the filter. Using these sets, we define the following intersection sets similar to the ones in Eq (4):

\[
\begin{bmatrix}
S_{00,00} & S_{00,01} & \ldots & S_{00,10} & \ldots & S_{01,11}
\end{bmatrix}
= \begin{bmatrix}
S_0^0 \cap S_0^1 \cap \ldots \cap S_0^{k-1} \cap S_0^k
S_0^0 \cap S_0^1 \cap \ldots \cap S_0^{k-1} \cap S_1^k
S_0^0 \cap S_1^1 \cap \ldots \cap S_0^{k-1} \cap S_1^k
\ldots
\ldots
S_1^0 \cap S_1^1 \cap \ldots \cap S_1^{k-1} \cap S_1^k
\end{bmatrix}
\]
The number of subsets is approximately equal to $2^K$. This number can grow fast as the number of parallel filters increase. The efficiency of the proposed algorithm compared to the number of filters and filter size is discussed Section III.

Eq (8) shows the summations over the defined subsets in order to calculate the filter results for each individual filter.

Calculation of summations in one row of the Eq (8) is sufficient to calculate results of each filter since these sums repeat themselves in each row with a different sign. The sets defined in Eq (7) are exclusive. Therefore the total number of summation operations defined in a row of Eq (8) is equal to the number of coefficients of filters in the filter bank. In Eq (8), the filtering operation is divided into two main structures. In the first summation structure, outputs of subset summations, as found in Eq (7), are calculated. In the second structure, subsets are summed once more to calculate the actual filter outputs.

At this stage we reduce the problem into summations of $2^K$ values for each filter. When the number of filters is significantly smaller than the number of coefficients in the filters, Eq (8) reduces the total number of summations required to implement the filter bank.

III. OPTIMIZATION BOUNDS OF COEFFICIENT SHARING IN FILTER BANK

In this section, the optimization performance of the algorithm is discussed. The main focus of efficiency in the proposed method is the reduction of the number of operations needed.

There are two ways to implement Eq (8), the outer summations can be either summed using a simple summation pyramid as in [23] or using multiply-and-accumulate (MAC) structure to map the operations to DSP48 blocks. Optimization bounds for both of the methods are presented in this section.

In order to give a reasonable bound for the optimization performance of the algorithm, all the filter coefficients of the filter bank are assumed to be taken from independent and identically distributed (iid) Bernoulli trials with equal probability of 1 and −1 outcomes.

First assume that there are $K$ filters and $M$ coefficients in each filter with coefficients $±1$. As shown previously in Section II, a filter bank with $K$ filters will have at most $2^K$ coefficient subsets. Statistically, these coefficient subsets will all have equal probability of occurring since coefficients are all iid. Number of coefficient subsets are important since it directly affects the number of operations needed where the subsets are connected to form the actual filter outputs as given in Eq (8).

It is desirable to have each coefficient subset to have high number of elements, since this means more coefficients can be shared. This is possible by either keeping $K$ small or $M$ high. Average number of elements of each coefficient subset can be written as follows:

$$E[|S_{00..00}| + ... + |S_{11...11}|] = \frac{M}{2^K},$$

where, $2^K$ is the total number of subsets. For a given $M$, large $K$ results in better optimization considering the $M$ also large. However as $K$ grows, the number of sets in Eq (7) grows exponentially making the algorithm impractical. It is evident that there is convex optimization surface and it is desirable to find a proper relationship between $K$ and $M$.

A. Number of Operations for the Filter Bank

For an $M/2^K$ number of coefficients in a subset, we need $M/2^K$ MAC operations. Then the expected number of MACs needed to implement all the subsets in a filter bank is given Eq (10).

$$E[\Pi_1] = \left(\frac{M}{2^K}\right) \times 2^K = M$$

With this many MACs, all the subsets are implemented, however additional operations are needed to implement the outer summations given in Eq (8). Outer summations can be computed using either MAC blocks or a summation pyramid as in [23]. Both approaches have their own advantages. Summation pyramid naturally does not use extra MAC operations and thus uses less DSP48s. However, multiply-and-accumulate implementation enables systolic implementation at the cost of increased sampling frequency.

1) Implementation of Outer Summations using MACs: Total number of MACs needed to implement outer summations in the filter bank is as follows:

$$E[\Pi_2] = (2^K) \times K$$

where, first term of the multiplication is the number of MAC operations needed to implement a single filter in the filter bank and second term of the multiplication is the total number of filters in the filter bank.

Hence, the expected number of MAC operations needed is in Eq (12).

$$E[\Pi] = E[\Pi_1] + E[\Pi_2] = M + (2^K) \times K,$$

where the optimization can be done if either of $K$ or $M$ is not given.

$$\min_{K,M} E[\Pi],$$

s.t. $M/2^K \gg 1$ (13)

2) Implementation of Outer Summations using Summation Pyramids: Since inner summations are simply summed or subtracted, it is also possible to not use multiply-and-accumulate operations at all. In order to achieve this, a summation pyramid as in [23] can be built that uses two input summation operations.

Total number of two input summations needed to implement outer summations in the filter bank is as follows:

$$E[\Sigma_2] = (2^K - 1) \times K$$

where, first term of the multiplication is the number of two input summation operations needed to implement a single filter in the filter bank and second term of the multiplication is the
The expected number of multiply-and-accumulate operations needed to implement the whole filter bank is
\[ E[\Pi(G)] = \left( E[\Pi_1(G)] + E[\Pi_2(G)] \right) \times G \]
\[ = G \times M + (2^{(K/G)}) \times K, \]
where \( K \) is the total number of filters in the filter bank, \( M \) is the number of coefficients in each filter, \( G \) is the number of filter bank groups with each filter bank group containing \( \frac{K}{G} \) filters.

Eq \( (19) \) is a convex function. Then, the optimization problem turns into the minimization in Eq \( (20) \).
\[
\min_{G} E[\Pi(G)],
\text{ s.t. } \frac{M}{2^{K/G}} \gg 1
\] (20)

2) Implementation of Outer Summations using Summation Pyramids: In order to implement the filters, the output of the subsets are summed according to the rule defined in Eq \( (5) \) and the filter coefficients are shared among filters of the filter bank group. For this stage, the expected number of summation operations needed is in Eq \( (21) \).
\[
E[\Sigma_2(G)] = (2^{(K/G)} - 1) \times \frac{K}{G}
\] (21)
First term of the multiplication in Eq \( (21) \) is the number of two input summation operations needed to implement a single filter in the filter bank group and second term of the multiplication is the total number of filters in the filter bank group.

Finally, total number of operations needed to implement the whole filter bank is
\[
E[O(G)] = \left( E[\Pi_1(G)] + E[\Sigma_2(G)] \right) \times G
\]
\[ = G \times M + K \times (2^{(K/G)} - 1), \]
where \( K \) is the total number of filters in the filter bank, \( M \) is the number of coefficients in each filter, \( G \) is the number of filter bank groups with each filter bank group containing \( \frac{K}{G} \) filters.

The optimization of the algorithm is done through minimizing the expected number of summation operations. Eq \( (22) \) is a convex function. Then, the optimization problem turns into the minimization in Eq \( (23) \).
\[
\min_{G} E[O(G)],
\text{ s.t. } \frac{M}{2^{K/G}} \gg 1
\] (23)
An important note is that, \( O(G) \) is the total number of operations, multiply-and-accumulates and two input summations combined. Hence an analysis of individual operations is also noteworthy and will be presented.

The solution of the minimization in Eq (20) and Eq (23) for some example cases are in Fig. 2 and Fig. 3 respectively. From Fig. 3, it can be quickly realized that decreasing for some example cases are in Fig. 2 and Fig. 3, respectively. This is because the algorithm has two stages and decreasing the number of operations in first stage increases the operations in second stage and vice versa. Fig. 2 and Fig. 3a are essentially same, because in Fig. 2, two input summations are simply converted to MAC operations.

This optimization is a crude one since it assumes there can be fractional number of filters in a group of filter bank. Thus, a realistic optimization bound is also needed.

C. Discrete Grouping of Filters

In a realistic case, \( \frac{K}{G} \) cannot be a fractional number. The optimization problem is modified using a discrete approach as follows:

1) \( G_1 = \text{mod}(K,G) \) amount of filter bank groups will have \( |G_1| = \frac{K-\text{mod}(K,G)}{G} + 1 \) filters. For these filter bank groups, the expected number of MAC operations in the first stage is in Eq (24) for each filter bank group,

\[
E[\Pi_1(G_1)] = \left( \frac{M}{2|G_1|} \right) 2^{|G_1|} \]  
\( = M \)  

2) The rest of the \( G_2 = G - \text{mod}(K,G) \) amount of filter bank groups will have \( |G_2| = \frac{K-\text{mod}(K,G)}{G} \) amount of filters and the total number of MACs will be,

\[
E[\Pi(G_1)] = \left( E[\Pi_1(G_1)] + E[\Pi_2(G_1)] \right) G_1, \quad (26)
\]

- If the filter stage is implemented using MAC blocks, expected number of summation operations in the second stage for the first \( G_1 \) filter bank groups is in Eq (27) for each filter bank group.

\[
E[\Sigma_2(G_1)] = (2^{|G_1|} - 1)|G_1| \]  
\( = G_1 \)  

and the expected number of operations will be,

\[
E[O(G_1)] = \left( E[\Pi_1(G_1)] + E[\Sigma_2(G_1)] \right) (G_1), \quad (28)
\]

Eq (28) is the total number of operations.
Then the first stage will have expected number of MACs as in Eq (29).

\[
E[\Pi_1(G_2)] = \left( \frac{M}{2^{G_2}} \right) 2^{G_2} \quad (29)
\]

\[
E[\Pi_2(G_2)] = M
\]

- If the filter stage is implemented using MAC blocks, expected number of operations in the second stage for this filter bank group is in Eq (30) for each filter bank group.

\[
E[\Sigma_2(G_2)] = (2^{G_2} - 1)|G_2| \quad (30)
\]

and total number of MAC operations will be,

\[
E[\Pi(G_2)] = \left( E[\Pi_1(G_2)] + E[\Pi_2(G_2)] \right) (G_2) \quad (31)
\]

- If the filter stage is implemented using summation blocks, expected number of summation operations in the second stage for this filter bank group is in Eq (32) for each filter bank group.

\[
E[\Sigma_2(G_2)] = (2^{G_2} - 1)|G_2| \quad (32)
\]

and total number of operations will be,

\[
E[O(G_2)] = \left( E[\Pi_1(G_2)] + E[\Pi_2(G_2)] \right) (G_2). \quad (33)
\]

Again, Eq (33) is the total number of operations.

For the full MAC implementation, using Eq (26) and (31) the total number of multiply-and-accumulates needed to implement the filter bank can be found as follows:

\[
E[\Pi] = E[\Pi(G_1)] + E[\Pi_2(G_2)]. \quad (34)
\]

The optimization problem is then,

\[
\min_G \quad E[\Pi_1(G_1)] + E[\Pi_2(G_2)],
\]

s.t. \( \frac{M}{2^{G_1}} \gg 1 \) \quad (35)

\[
\frac{M}{2^{G_2}} \gg 1
\]

where \(|G_1| = K - \text{mod}(K, G) + 1\) and \(|G_2| = K - \text{mod}(K, G)\).

For the hybrid MAC and summation pyramid implementation, (28) and Eq (33), the total number of summations needed to implement this filter bank can be found as follows:

\[
E[O] = E[O(G_1)] + E[O(G_2)]. \quad (36)
\]

The optimization problem is then,

\[
\min_G \quad E[O(G_1)] + E[O(G_2)],
\]

s.t. \( \frac{M}{2^{G_1}} \gg 1 \) \quad (37)

\[
\frac{M}{2^{G_2}} \gg 1
\]

where \(|G_1| = K - \text{mod}(K, G) + 1\) and \(|G_2| = K - \text{mod}(K, G)\).

Eq (37) is the total number of operations and a breakdown of individual operations is valuable.

An example of Eq (35) and (37) is in Fig. 8 and 9.

The optimization problem is again convex and have clear minimums.

In this section, FPGA synthesis performance of the algorithm is compared to other filter design algorithms referenced in Section I. Comparison is grouped under two main applications, a) FIR filter bank, b) Polyphase filter bank. In each application, other coefficient sharing methods referenced in Sec. II are also implemented. In order to achieve fast prototyping and considering the complexity of our algorithm to implement on FPGA, MATLAB’s HDL Coder Toolbox is used to generate the necessary HDL codes. All of the coefficient sharing algorithms are implemented in MATLAB for a fair comparison. Generated HDL codes are then synthesized in Vivado in order to find the resource cost on an FPGA.

In all sections, direct form FIR design, partially serial systolic architecture, fully serial systolic architecture and our coefficient sharing algorithm are compared with each other. Comparison criteria are, number of lookup tables (LUTs), registers, DSP48s, samping frequency \((F_s)\) of the fastest element in the block and finally the output delay of the algorithm with respect to the Direct form FIR implementation. An algorithm is considered to be efficient if it has low values in all of these criteria.

In the designs for all of the different algorithms, tapped delay line is shared among all filters, in order to further reduce resource cost. In addition to this, for partially systolic architecture, upsample blocks are also shared.

For a sample filter bank with \(K = 4\) and \(M = 60\), block diagram examples of implemented designs in MATLAB Simulink are in Fig. 7a, 7b, 7c, 8a, 8b, and 8c. In 7a and 7b, difference is in the Filter blocks. In 7a, they are implemented via summation tree as depicted in 23 and in 7b, they are implemented via MAC structure to map them to DSP48 blocks on FPGA. In Fig. 7c, MAC structures are implemented via systolic approach in order to show the flexibility of the proposed algorithm.
Fig. 6: Optimization of Eq (37) with respect to $G$ for various $M$ and $K = 8$.

In this example block diagrams, number of subgroups for Figs. 7a, 7b and 7c are found via the optimization method presented in Sec. III.

Polyphase filter banks require preliminary manipulations before using any of these designs. These representations are specifically designed for interpolator or decimator filters. An example FIR interpolator with upsampling ratio $U$ and number of filter coefficients $M$ is in Fig. 9 with its corresponding polyphase representation. Main purpose of polyphase representation is to divide the original filter into subfilters and exploit Noble indentity to reduce the sampling rate of the filter.

In Fig. 9 polyphase representation creates a filter bank, which can be implemented using any of the designs in Fig. 7a, 7b, 7c, 8a, 8b and 8c.

V. FPGA SYNTHESIS PERFORMANCE

In this study Xilinx Zynq UltraScale+ MPSoC ZCU106 is used as the target device. It holds a ZU7EV-2FFVC1156 chip with 230400 lookup tables (LUTs), 460800 registers and 1728 DSP48 elements. This chip is specifically chosen so that synthesis is not bottlenecked by the number of chip resources. Filter coefficients are generated via `randi(-)` function of MATLAB with random number generated seed `rng(50)`. Generated 0’s are simply replaced with -1’s.

As stated previously in Sec. IV comparison is grouped under two main applications, a) FIR filter bank, b) Polyphase filter bank. Filter banks with different number of filters and filter coefficients are implemented using designs in Fig. 7a, 7b, 7c, 8a, 8b and 8c. For our algorithm, the number of filters in groups is chosen via method described in Sec. III. For the polyphase filter, only interpolator structure is implemented since decimator structure is very similar.

1Reader can regenerate the presented algorithms using codes provided in [24].
The resource performance and the sampling frequency is accelerated so that only two methods in Sec. III. For the partially systolic architecture, filter Coefficient sharing algorithm with DSP48 at the filter stage Fig. 7a. This is also the same reason why it needs Carry8s.

From Tables I, II and III, the major advantage of the proposed algorithm is the sampling period of the filter. Without increasing sampling period, proposed algorithm is able to decrease the number of used resources significantly. Coefficient sharing algorithm require more logic resources because it has to implement a summation pyramid at the filter stage as in Fig. 7a. This is also the same reason why it needs Carry8s. Coefficient sharing algorithm with DSP48 at the filter stage

uses much less logic resources in exchange of some DSP48s.

Systolic Coefficient Sharing algorithm on the other hand is much more complex as per resource usage. For the filter bank with \( K = 8 \) and \( M = 120 \) each, the subset stage is accelerated twice where as the filter stage is accelerated four times. This translates to 79 of the MACs having twice the sampling frequency of the input data. 79 MACs are in fact the number of MACs used to implement the subset stage. 32 of the MACs require four times the sampling frequency of the input data, which is the number of MACs used to implement the outer summation stage. Thus a total of 111 DSP48s are used in a multirate manner.

As the number of coefficients decrease, number of DSPs used for the fully systolic design is much less than the systolic coefficient sharing algorithm. This is because the outer summations need a fix number of MACs to compute where as number of MACs needed by fully systolic design is exactly equal to the number of coefficients. This is evident in the \( K = 8 \) and \( M = 90 \) case. Even though fully systolic approach uses less number of DSP48s, its sampling frequency is much higher compared to the systolic coefficient sharing algorithm. In addition to this, systolic coefficient sharing algorithm uses majority of DSP48s in a much lower sampling frequency. Similar comments can be made for \( K = 6 \) and \( M = 60 \) case.

Finally, for the cases in Table II and III coefficient sharing with summation pyramid gives the first output 4 clock cycles late than the direct form FIR implementation. This is due to the way the summation pyramid is implemented with delay blocks.

**TABLE I: Performance of FIR Designs for 8 filters with 120 coefficients each.**
Since there are 4 filters in each group, the summation pyramid has 4 stages with a unit delay block at each stage, resulting in 4 delays. Coefficient sharing with systolic implementation has additional delay of 4 clock cycles because of the pipeline delays and upsampling blocks that are implemented via shift registers. Since for the \( K = 6 \) and \( M = 60 \) case the number of subsets are much smaller, the overall delays for this case are less than the ones in Table I and II. However, any of the proposed coefficient sharing algorithms does not introduce significant delays with respect to the direct form FIR filter.

These synthesis results show the flexibility and efficiency of the proposed algorithm. It not only reduces the number of operations compared to regular filter banks, but also enables application of other algorithms. This is because, the sharing algorithm is based on regrouping and rewriting the regular convolution equation without changing its base structure.

### B. Polyphase Application

As shown in Fig. 9, polyphase representation creates a filter bank structure. An interpolator with \( U = 2 \) upsampling ratio and \( M = 60 \) coefficient filter, and another interpolator with \( U = 3 \) and \( M = 60 \) filter is implemented. Since number of filters in the polyphase representation is determined by the upsampling ratio, partially serial systolic structure is not implemented. The resource performance and the sampling frequency \( (F_s) \) of the algorithms are in Tables IV and V. However, any of the proposed coefficient sharing algorithms does not introduce significant delays with respect to the direct form FIR filter.

Similar to the regular filter bank implementation, coefficient sharing with summation pyramid gives the first output 9 clock cycles later than the direct form FIR implementation for the interpolator with \( U = 3 \) and \( M = 90 \). Coefficient sharing with systolic implementation is on the other hand is the slowest. In addition to the delays in the summation pyramid design, overall data integrity pipelines are the main reasons for increased delay.

### VI. Conclusion

In this paper, a new coefficient sharing algorithm for parallel filter banks, that shares the coefficients between a number of filters is presented. Filter banks are widely used in radar signal processing and signal synchronization in communications field and quickly becomes one of the most resource heavy blocks in an FPGA for long sequences and high number of filters. The algorithm groups the filters and finds the similarities within the specified group. The coefficients are rearranged according to the rules discussed in Section IV.
The optimization bounds of the algorithm clearly shows the efficiency of the algorithm with respect to filter length and number of filters in a group, giving an early idea on how to group the filters in a filter bank in order to achieve better resource usage performance.

Finally the post-synthesis results in an FPGA shows the resource performance with respect to regular filter banks and commonly used systolic architectures. Compared to direct form FIR structure, coefficient sharing algorithm has up to % 50 less resource usage while working at the same sampling frequency. Systolic designs have comparable resource usage however they also require much higher sampling rate, depending on the sharing coefficient. Coefficient sharing algorithm in which filter stage implemented with multiply-and-accumulate increases the efficiency of the approach further. Especially the DSP48 efficiency of the algorithm is clear.

Algorithm presented in this paper is scalable and flexible. Coefficient sharing algorithm simply implements the same filter bank in an elaborate manner, hence enabling usage of other coefficient sharing algorithms. An example of systolic implementation of the coefficient sharing algorithm is presented in this paper, which provides less number of DSP48s used in lesser sampling frequency compared to regular systolic approaches. A further reduction of resource usage is possible using other well known coefficient sharing algorithms that optimizes single filters such as in [17], [18], [19].

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