Cryo-computing is presently severely limited by the absence of a suitable fast and energy efficient cryo-memory. Ideally, such memory should be compatible with single-flux quantum (SFQ) logic in terms of speed, switching energy and matching impedance. Here we present an implementation of non-volatile charge configuration memory (CCM) in a cryo-computing environment by combining it in parallel with a pulse-triggered superconducting nanowire cryotron (nTron). The combined device is modeled in terms of the dynamical response of the SC order parameter in a current-controlled nanowire with a CCM shunt. Analysis of time-dynamics and current-voltage characteristics based on measured device parameters show that single flux quantum (SFQ)-level pulses can drive non-volatile CCM on the picosecond timescale, while allowing the nTron to operate in non-latching mode. The inherent high energy efficiency and ultrahigh speed makes this hybrid device an ideal memory for use in cryo-computing and quantum computing peripheral devices.

**Introduction**

Computing is currently severely limited by processor heat and relatively slow advances in memory performance. Cryocomputing (CC) has been heralded as an obvious solution to heat dissipation and energy-efficient single flux quantum (EESFQ) circuits have recently been developed that also offer very high operating speed and efficiency. However, it is well known that the proliferation of CC technology in general is inhibited by the lack of a suitable fast, energy-efficient cryomemory. The development of such a memory is not only important in SFQ computers, but also in superconducting (SC) quantum computing, where it allows control and error-correction circuits to be placed near the quantum processor, eliminating the need for large number of noise- and heat-generating control cables that lead to decoherence and introduce cosmic-ray noise into the quantum processor. A number of different approaches to the introduction of various types of memory into a CC environment have recently been investigated with various degrees of success, including cryo-CMOS, superconducting memory and magnetic memory. Most recent purely-superconducting memories have relied on low kinetic inductance niobium wiring to reduce overall element size, but at present the problem of fast, scalable, energy efficient memory devices is still wide open. Here we investigate a possible new solution to the cryo-memory problem based on CCM devices fabricated from 1T-TaS$_2$, which have been recently shown to operate down to milli-Kelvin temperatures. The devices rely on ultrafast switching between electronic domain configurations within a charge-ordered material in response to an external electromagnetic stimulus, which results in resistance changes by a factor of $10^3$. The energy required for switching has been shown to be as low as 2.2 fJ/bit, while the switching time ranges from 600 ms to less than 18 ps. Their data retention time is controllable by temperature, and is sufficiently long at low temperatures for the memory device to be considered non-volatile below 20 K. This makes CCM a good candidate for ultrafast low-power non-volatile memory applications demanded by EESFQ circuits. However, the desired switching energies for use in SFQ circuits is set by the very small magnitude of the superconducting flux quantum $\Phi_0 = 2\pi n \Phi_0$ which carries data. For typical currents, the energy of such pulses is $E_{\Phi_0} \sim 10^{-20}$ J. Considering that CCM devices typically require $\sim500$ mV for switching, amplification is needed to drive them by SFQ devices. The amplifiers should be fast, require small amount of energy, and allow control of CCM by single SFQ pulses that carry bits of data. A superconducting nanowire (NW) cryotron (nTron) device, based on gate-controllable switching between the normal and superconducting state of the NW, which is capable of being driven by SFQ pulses was recently reported. The nTron was shown to be capable of driving conventional electronics, connecting single-flux-quantum circuits to CMOS memories. Unfortunately, because of the high dissipation, CMOS memories are too inefficient for practical use in cryocomputing circuits, and more efficient cryomemory devices, such as CCMs are desirable. The nTron can have an output impedance in the ON state of $R_N \gg 10$ kΩ, and produce $>1$ V at the output, which is more than sufficient for driving CCMs. However, nTrons and SC NW switches with passive loads are in general not ideal for driving dynamical circuits because they rely on hotspot-growth process along the length of the nanowire, and are not able to self-reset without external circuitry.

The main idea presented here is to investigate SFQ-switching time-dynamics and current-voltage characteristics of CCM-shunted SC NWs and, by extension, CCM-shunted nTrons shown in Fig. 1. The switchable CCM shunt resistance $R_{\text{CCM}}$ can be used to cause a drop in current through the NW, which – under the right conditions - enables the NW to switch between normal and superconducting state and vice versa. To gain an understanding and the operation of such a ‘parallelotron’ (or ‘pTron’) device, we model the switching behavior using a Josephson junction model previously applied to modelling phase slip dynamics in capacitively and resistively shunted SC NWs. We show that memory protocols using conventional enabling bias currents and SFQ trigger pulses can be used to drive pTrons within a parameter range that is compatible with conventional SFQ circuits and current CCM devices. We investigate the dynamical behavior on the picosecond timescale and discuss the speed limitations of pTron devices due to SC NW quasiparticle diffusion, thermal diffusion and other circuit constraints.

**The dynamical response of a pTron.**

The properties of a resistively and capacitively shunted Josephson junction (RCSJ) models for describing the properties of superconducting NWs were investigated in detail by Brenner et al., who showed two different regimes of operation as the NW approaches the critical current $J_c$, depending on the magnitude of the shunt resistance $R_s$. In one regime, dissipation is caused by the appearance of fluctuating phase slip centers (PSCs) in which the phase $\phi$ of the superconducting order parameter $\psi = \psi_0 e^{-i\phi}$ locally exhibits a shift of $2\pi$ which corresponds to the movement of a quantum of magnetic flux $\Phi_0 = h/2e$ from one side of the wire to the other. In the other, quasiparticles (QP) that are a result of pair-breaking (PB) dissipate energy in a process roughly similar to Joule heating. The shunt resistance $R_s$ that can be presented by CCM devices is typically $10-20$ kΩ in the off state ($R_{\text{ON}}$), and $200-400$ Ω in the on state ($R_{\text{ON}}$), so the contrast in resistance is high enough that in principle the device can be used to switch the system between different voltage-current (V-J) curves, or even between the PB and PSC regimes using single SFQ pulses.
Figure 1. The pTron device. a) Scanning electron microscope images of the CCM device presented in Fig. 2. The thickness of the 1T-Ta$_2$ layer is 80 nm. Its fabrication process is described in Ref. 4. b) A pTron rendering showing individual nTron and CCM devices. c) An equivalent circuit for describing the pTron includes a Josephson junction with a normal state resistance $R_N$ and capacitance $C$. The pTron (dashed box) includes a switchable CCM shunt resistance $R_{CCM}$ in parallel with the NW or nTron. The model circuit includes a bias current source $I$ and a pulsed source $I_{ch}$ for writing data.

Before describing the properties of the pTron, let us briefly describe the operation of a CCM device. It is best described as a current-controlled switchable nonlinear resistor, whose switching threshold currents are typically 50–200 µA, corresponding to voltages across the device of $V_{CCM} = 0.5$–0.6 V. V-J curves corresponding to write (W) and erase (E) cycles for a typical 60 nm CCM device are shown in Fig. 2a and b respectively. The V-J characteristics can be modelled with:

$$V_{CCM} = \frac{R_{CCM}}{R_{W}} \ln \left( \frac{J}{J_W} + 1 \right) \quad J > J_W$$

where $J_W$ is the switching threshold current for writing, $J_{CCM}$ and $V_{CCM}$ are device constants. A similar set of equations apply for the E cycle, and is obtained by replacing $J_W$, $V_{CCM}$ and $J_{CCM}$ by $J_E$, $V_{CCM}$ and $J_{ECM}$ respectively. Fits to the experimental curves for W and E are shown by green lines in Fig. 2a and b respectively. The resistance of the CCM in the HI resistance state is given by $R_{HI} = V_{CCM}/J$. The value of $V_{CCM}$ depends on the CCM device, mainly on the size of the memory cell, while the value of $R_{HI}$ depends mainly on the contact resistance within the CCM device and is typically a few hundred ohms.

For pTron operation the shape of the V-J curve of the CCM is actually not very important, because no current is flowing through the CCM while the NW is superconducting. Only when the NW becomes resistive, a voltage appears across it, switching the CCM to a different state if the applied current is above threshold value for W or E. Thus, to simplify the calculation we can assume typical constant resistance values $R_{HI} \approx 20 \text{k}\Omega$ and $R_{LO} \approx 200 \text{ }\Omega$, shown by the example in Fig. 2.

Figure 2: V-J characteristics for the CCM. Write (W) and Erase (E) cycles are shown in a) and b) respectively. The resistances $R_{HI}$ and $R_{LO}$ are shown by dashed lines. The green line is a fit to Eq. (1) where the switching parameters for the write operation a) are: $J_W = 165 \mu\text{A}$ and $V_{CCM} = 0.63 \text{ V}$.

Now let us turn to the dynamical behavior of the pTron (Fig. 1). As mentioned earlier, in narrow SC NW channels whose widths $w$ are comparable or smaller than the coherence length $\xi$, the critical current $J_c$ is determined by pair-breaking, and the appearance of rapidly fluctuating PSCs along the NW. For example, 100 nm wide NbTiN NWs show characteristic PSC steps in the current vs. voltage curves, particularly at intermediate and high temperatures as $T \rightarrow T_c$. Similar behavior was observed in $\delta$-MoN nanowires. The crossover between the PSC fluctuation regime and the PB regime is described quite well by the Mcumber Josephson junction model. Here we will extend this model to the pTron by including a CCM shunt. We will consider the behavior of a SC NW as well as an nTron, which is effectively a SC NW driven by an external choke whose function is to trigger a local hot-spot in a NW, current biased just below $J_c$. The circuit is shown in Fig. 1, where $R_{CCM}$ is the CCM resistance, $C$ is the circuit capacitance, $R_N$ is the normal state resistance of the nanowire and $J$ is the bias current. $R_N$ and $C$ represent the normal state losses, including those of the quasiparticle tunnel current. $I_{ch}$ represents the choke trigger source that initiates switching. Following ref. 6, the model calculation describes the time-dynamics of the phase $\phi$ of the superconducting order parameter $\psi = \psi_0 e^{i\phi}$ within the SC NW. By applying Kirchhoff’s laws and the Josephson’s relations $J = J_c \sin (t)$ and $V = \frac{J_c}{n_0} \sin(t)$, the equation of motion becomes:

$$Q^2 \frac{d^2 \phi}{dt^2} + d\phi \frac{dt}{dt} + \sin \phi = J,$$

where $J$ is the current through the SC NW channel, $J_c$ is the critical current of the NW, $Q = \frac{R_T}{\sqrt{2}\eta} \frac{C}{\hbar}$ is the quality factor and $R_T = \frac{R_{RL}}{R_{RL} + R_{CCM}}$ is the parallel resistance of $R_N$ and $R_{CCM}$, which are the normal resistance of the NW and the shunt resistance corresponding to the CCM device, respectively. For convenience, time $t'$ is measured in units of $t' = \frac{2eJ_c}{h} t$.

Alternatively, the behavior of the SC NW can also be described in terms of time-dependent Ginzburg-Landau equation (TDGL). Eq. (2) neglects all fluctuations of the superfluid density and considers only dynamics of the phase $\phi$. Therefore it represents the limit of TDGL in the limit of large $u \gg 1$, where $u$ is the ratio of the relaxation time of the superfluid density to the phase relaxation time. The behavior of the nanowire within TDGL approach was discussed in Ref. 6,7,25. Similar as for the TDGL model, for $J < J_c$, the RCSJ model in Eq. (2) has two steady state solutions, defined by the condition $\sin \phi = J/J_c$. One of these solutions is stable until $J = J_c$ and the second is always unstable. When the current reaches critical current value these two steady state solutions collide and a periodic in time stable limit cycle solution emerges. This solution is characterized by the finite voltage in the circuit and Ohmic losses. Without noise the
steady state solution becomes unstable exactly at the depairing critical current. The presence of the current noise leads to a stochastic transition to the normal state at a smaller current which is usually called the switching current $J_{sw}$. The periodic limit cycle solution is stable also below critical current. At the retrapping current $J_{re} < J_c$, the limit cycle collides with the unstable steady state solution and loses its stability.\textsuperscript{26,27} As it was demonstrated in Ref.\textsuperscript{26,27}, the stability of different solutions of both the TDGL model and the RCSJ model described in Eq. (2) depends on the shunt resistance. Decreasing the shunt resistance leads to the decreasing difference between switching and retrapping currents.

We proceed by first considering the behavior of a SC NW without a CCM. Figures 3a and b show the temporal evolution of Eq. 2 for $\phi(t')$ and the resulting voltage $V = J_c R_T \frac{d\phi}{dt}$ for typical NW parameters. As expected, below the NW critical current, when $J < J_{sw}$, the application of a current at $t' = 0$ causes small damped oscillations of $\phi(t')$ and $V$ with a frequency $\nu = 2eJ/(\pi R_T h)$, which revert to zero with a time constant $\tau_{0c} = R_T C$ (Fig. 3a). When $J > J_c$, we observe a transition to the normal state as the phase $\phi(t')$ increases with time and a finite $V$ appears across the NW which settles to a constant value within a time defined by $\sim \tau_{0c}$ (Fig. 3b).

Introducing the CCM shunt resistance into Eq. 2, similar behavior is observed for $V$ until the CCM switching threshold is reached, given by $J_{CCM}^V = V/R_T$. Thereupon the device switches to a low resistance state with a time given by $\tau_{0c} = R_T C (= 0.4 \text{ ps})$ (Fig. 3c) with the CCM in the $R_{LO}$ state. The pTron then remains either in a low-resistance state or the superconducting state, depending on the value of $R_{LO}$ as shown in Fig. 3c. (The parameter values are listed in the figure caption.)

**Figure 3. Temporal pTron switching dynamics with DC and 1 ps SFQ-pulses.** a) The dynamical response of the phase $\phi$ (orange) and voltage $V = J_c R_T \frac{d\phi}{dt}$ (blue) following an instantaneous increase in current $J$ at $t = 0$: a) below SC NW switching threshold ($J = 100 \mu A < J_{sw}$) and b) above threshold ($J = 130 \mu A > J_{sw}$). In both cases $R_N = 600 \Omega$, $R_{CCM} = 2k\Omega$, $J_c = 150 \mu A$. c) Switching with $J = 87\mu A$ DC current. Here $R_N = 20 k\Omega$, $R_{H} = 8.5 k\Omega$, for different $R_{LO} = 4000 \Omega$ (blue), 2000 $\Omega$ (orange) and 700 $\Omega$ (green). d) The voltage $V$ (blue) after switching by a 1 ps $J_{ch} = 5 \mu A$ choke pulse (orange) synchronized with a $\tau_{0} = 100 \text{ ps}$, $J = 87\mu A$ bias pulse (green). The rising and falling edges of the bias pulse were rounded with a Fourier filter. e) Switching by different $J_{ch} = 10 \mu A$ (blue) pulses, 100 $\mu A$ (orange) and 250 $\mu A$ (green) (here again $R_N = 20 k\Omega$, $R_{H} = 8.5 k\Omega$, $R_{LO} = 4000 \Omega$, choke pulse length $\tau_{ch} = 1 \text{ ps}$)

**Switching with $\phi_0$ pulses.**

The ultimate goal is to switch the pTron with single SFQ-like pulses. For this purpose, an ultrashort (~1 ps) SFQ write (W) pulse $J_{ch}(t)$ is applied across a current biased NW (as indicated in Fig. 1). In practical nTron devices the pulse is applied in the middle of the NW through a third terminal called the choke.\textsuperscript{8} The pulse causes the superconductivity of the choke to break and the formation of a hotspot. The hotspot spreads into the channel, effectively decreasing the critical current of the channel.\textsuperscript{2} To model the role of the choke, a pulsed bias current $J_{ch}(t)$ is applied synchronously across the NW, such that the total current through the NW is $J = J_b + J_{ch}$ (see Fig. 1). The resulting switching is shown in Fig. 3d for $J_b = 5 \mu A$, $J_{ch} = 87 \mu A$ and $\tau_{ch} = 1 \text{ ps}$. The bias current is in the form of a 100 ps pulse which is Fourier filtered. (Other parameter values given in the figure caption are from typical nTron devices in the literature). The choke current $J_{ch} = 5 \mu A$ corresponds to one flux quantum $\phi_0$ of width $\tau_w = 1 \text{ ps}$ and amplitude of 2 mV converted to a current by a $R_{set} = 400 \Omega$ resistor in series. The values of $J_{ch}$ and $J_b$ are very close to the recently reported nTron choke switching and channel currents of $\sim 7 \mu A$ and $30\sim120 \mu A$ respectively.\textsuperscript{5,17}

The switching dynamics for different magnitude $J_{ch}$ is shown in Fig. 3e. With appropriate bias, the pTron switching threshold is $< 5 \mu A$, which means that it can easily be switched with a single SFQ pulse. Note that the resulting LO state of the pTron can be either superconducting or in a low-resistance state, depending on the value of $R_{LO}$ as shown in Fig 3c.

**V-J curves for writing, erasing and reading data.**

Having examined the switching dynamics for short SFQ-like pulses, let us examine the V-J characteristics of the NW and the pTron for the W, E and read (R) cycles calculated using Eq. (2). In Fig. 4a we show the NW V-J curves for different shunt resistances $R_s$, illustrating the expected cross-over from the hysteretic regime with high $R_s$ to the non-hysteretic regime for low $R_s$. The switching and retrapping currents are also indicated in Fig. 4a. In the calculation we have used $C = 1fF$, and $J_{c} = 120 \mu A$. With higher values of $R_{LO} \sim 4000 \Omega$, and consequently high $Q \sim 300$, the Josephson term $\sin \phi$ in Eq. 2 is unimportant. A smaller value of $R_{LO}$, with a smaller $Q \sim 7$ as in Brenner et al,\textsuperscript{8} leads to the PCS fluctuation regime as the oscillatory signal $\phi$ becomes relevant. For our purposes, to reach sufficiently high voltages required by the CCM, it is convenient to operate the NW in the hysteretic regime.

For the $V-J$ curve calculation of Fig. 4a we have used the same initial conditions as in Ref.\textsuperscript{8}: $\phi(0) = \frac{d\phi(0)}{dt} = 0$ for increasing current and $\phi(0) = \frac{d\phi(0)}{dt} = 1$ for decreasing current. The switching current in that case corresponds to the value of $J$ for which the point $\phi(0) = \frac{d\phi(0)}{dt} = 0$ of phase space moves from the basin of attraction of the stable steady state solution $\phi = \arcsin(J/J_c)$, to the basin of attraction of the stable limit cycle. Another choice of initial condition when the initial values of phase and its derivative for the new value of current are set to be equal to the final values of the phase and its derivative for the previous value of current\textsuperscript{26,27} leads to a different V-J curve, where the switching current is equal to the critical current $J_c$. This happens because in this case the initial conditions are always in the basin of attraction of the stable steady state solution. Taking into account that initial conditions are defined by the procedure of experimental measurements, the V-J curve of the device will be dependent on how the measurement is done. In a real situation the operation of a memory device is further complicated due to the switching current being dependent on external conditions, such as pulse shape and current noise. All this implies that there is some uncertainty in definition of the switching and retrapping currents for the SC NW.\textsuperscript{26,27} However, it also makes it possible to tune the switching current by tailoring the pulse shape.
The Write (W) process for a pTron is shown in Fig. 4b. In the initial state the NW is superconducting. Increasing $I$ above the switching current $I_{SW}$ causes the NW to revert to the normal state at a value determined by the CCM shunt with resistance $R_{HI}$, at which point a voltage appears across the CCM. With further increasing current, when the current reaches $I_W$ the CCM switches and the overall resistance drops from $R_{HI}$ to $R_{LO}$. The device parameters used for the calculation shown in Fig. 4b are typical values from the literature for the NW (or nTron) and CCM and are given in the figure caption. The plots in Fig. 4b are for three different values of $R_{HI}$ = 12 kΩ (blue), 16 kΩ (orange) and 20 kΩ (green). The switching, writing, and retrapping currents are also indicated.

With an nTron driver configuration, the NW channel is biased with a pulse $I_{p}<I_{SW}$ and the device is in a non-dissipative state. Data is then written by a small SFO-size pulse through the nTron to a current $I_{ch}$ just below $I_{SW}$, and the device is in a non-dissipative state. The Write (W) process occurs at $I_{W}$ just below $I_{SW}$ and the device is in a non-dissipative state. The Write (W) process occurs at $I_{W}$ just below $I_{SW}$ and the device is in a non-dissipative state.

The Erase (E) process. To revert from $R_{LO}$ to $R_{HI}$ the bias current of the channel is increased to approximately $2.2 I_c$ to reach the CCM erase threshold as shown in Fig. 4d (Note that the resistive part of the E cycle is quite similar to that of the CCM on its own as shown in Fig. 2b). The E process of the pTron is governed predominantly by the erase threshold of the CCM. The largest amount of energy is required for the E operation, which is a thermal process. This is determined by thermal characteristics of the device. In practice erase operations are performed in bulk, where speed and dissipation are not of primary importance. Since this is not the subject of the present study it will not be discussed further.

**Figure 4. V-J curves for pTron operations** calculated using Eq. 2 corresponding to the NW, and for W, E and R cycles of the pTron. a) The V-J curves of the NW for different shunt resistances 40, 100 and 400 Ω. The non-hysteretic PSC regime is for 40 Ω. b) The W cycle using $I_{W} = 61 \mu A$ shown for three different values of $R_{HI}$ = 12 kΩ, 16 kΩ and 20 kΩ. Other common circuit parameters are: $R_{HI}$ = 8.5 kΩ, $R_{LO}$ = 4000 Ω, $C$ = 1 nF, and $I_c$ = 120 μA. The return cycle is shown with dashed lines. c) The R cycle. The shaded area indicates where the HI and LO states can be discerned. Note that $R_{LO}$ = 0 between 60 and 68 μA, so the ratio $R_{HI}/R_{LO}$ is infinite. d) The E cycle with $I_c$ = 93 μA and for the same three $R_{HI}$. The return cycle is shown with dashed lines.

**The Read (R) process.** To read the state of the CCM, the required current range is $I_{SW} < I < I_{W}$ shown in Fig. 4c. Note that in the present case a narrow region between 60 μA and 68 μA is superconducting in the $R_{LO}$ state. The maximum R energy is $E_R = \frac{I_{SW}^2 R_{HI}}{2}$, which for the device with $R_{HI}$ = 20 kΩ is in the range $2 J < E_R < 3 J$. In principle the R energy is zero in the $R_{LO}$ state if this is superconducting. The width of this region corresponds to the difference of switching currents in the LO and HI states (Fig. 4c), which can be tuned by the nTron and CCM parameters.

**Discussion**

The desired operating regime of the SCNW is dictated by the Write voltage of the CCM and its HI state resistance $R_{HI}$

$$|V_{CCM}| = 0.3 - 0.6 V \text{ and } R_{HI} = 2 - 10 k\Omega$$

The non-hysteretic regime. If the CCM switches to $R_{HI}$, then the SCNW can either remain in the PB regime or switches over to the PSC fluctuation regime, depending on the value of $R_{HI}^{CCM}$. In our current device, with most typical value of $R_{HI}^{CCM} \approx 400 \Omega$, the NW remains in the PB regime (Fig. 4b). In this regime the readout finds the NW either in the SC or the $R_{LO}$ state of the NW, depending on the readout current. The use of smaller CCM devices with smaller $R_{HI}^{CCM}$ and/or $R_{HI}$ smaller would enable the device to switch between the PB and PSC regimes, which would have the advantage that in the LO state the pTron is superconducting, exhibiting an infinite $R_{HI}/R_{LO}$ ratio. For unshunted NWs, or if $R_{HI}$ is very large, the retraction and switching currents are substantially different. The NW behavior is governed primarily by normal state Joule heating as a result of quasiparticle recombination and thermalization processes involving phonons that provide a mechanism for eventual thermalization of the NW. For low shunt resistances, the system resistance is primarily determined by $R_{HI}$ & $R_{CCM}$, because the overall parallel resistance $R_T$ is much smaller than bare $R_{HI}$.

In principle the R energy is $E_R = \frac{I_{SW}^2 R_{HI}}{2}$, which for the device with $R_{HI}$ = 20 kΩ is in the range $2 J < E_R < 3 J$. In principle the R energy is zero in the $R_{LO}$ state if this is superconducting. The width of this region corresponds to the difference of switching currents in the LO and HI states (Fig. 4c), which can be tuned by the nTron and CCM parameters.

While in our simulations we have used the McCumber Josephson junction model for reasons of simplicity, this model is equivalent to TDGL approach, except that superfluid density fluctuations are neglected. This introduces some restrictions. The main restriction is related to the relaxation time. It is assumed that all microscopic relaxation processes associated with quasiparticle thermalization, phonon reabsorption, hot carrier diffusion are fast in comparison with long Ginzburg-Landau relaxation time. I.e. Eq. (2) assumes that RC-time $t_{RC}$ should be much longer than microscopic relaxation time scales. However, microscopic processes occur on timescales that represent natural limitations for the device switching time, as we shall discuss below.

Several factors play a role in the speed of the pTron which also have bearing on the applicability of the RCSJ model and also the eventual usefulness of the device. Within the model the characteristic response time is controlled by $R_T$ and the circuit capacitance $C$, which in the present example gives an RC constant $0.4 ps < t_{RC} < 6 ps$. In comparison, the CCM intrinsic switching speed is as fast as ~0.45 ps, so this in principle should not limit overall device speed. In the pair-breaking regime, the QP dynamics in the SCNW is governed by QP recombination by optical phonon emission and the subsequent decay of high-energy optical phonons to low-energy dispersive acoustic phonons that carry heat out of the NW volume and eventually escape...
into the substrate. These processes, as well as phonon reabsorption are described by Rothwarf-Taylor (RT) equations\textsuperscript{28} in which the acoustic phonon escape out of the device is the rate-limiting step. These thermalization processes in NbN have been studied in detail within the context of RT equations. Optical pump-probe experiments directly measuring the transition from the SC to the normal state report this to occur within \(<10\) ps in NbN sputtered films\textsuperscript{29}. The phonon escape time \(\tau_{\text{esc}}\) was reported to occur on a timescale \(~100\) ps in a \(15\) nm thick NbN film\textsuperscript{29}, which is also discussed by MacCaughan et al in the NW channel of an nTron device.\textsuperscript{3} This is significantly longer than the phonon escape time in the ballistic limit for acoustic phonons generated by the quasiparticle recombination process can be made. (Assuming a velocity of sound \(v_s \approx 5\) nm/ps, for a film thicknesses \(\theta \approx 15\) nm, a lower limit for the escape time is \(\tau_{\text{esc}} = \frac{\theta}{v_s} \approx 3\) ps.) Clearly the phonon escape process that determines the nTron dynamics is not ballistic, but diffusive\textsuperscript{2,29}. In order to reach high operating speeds, the phonon escape timescale can be optimized either by varying film thickness and/or acoustic impedance matching at the interface, for example by including a buffer layer between the SC film and the substrate\textsuperscript{10}.

Finally, let us compare the QP recombination and diffusion timescales with the response time \(\tau_K = L_K/R_T\) determined from the kinetic inductance \(L_K = \frac{m_e I}{2\pi\epsilon^2 A}\). Here \(l\) is the length of the wire, \(A\) is the device cross-section and \(n_e\) is the electron density. Using values for a typical device \(l = 1\mu m\), \(A = w \times \theta\) nm\(^2\), \(n_e = 10^{24}\) m\(^{-3}\), \(L_K \approx 47nH\), where \(\theta \approx 15\) nm is the NbTiN film thickness and \(w = 25\) nm is the width, which together with \(R_T \approx 6\) k\(\Omega\) gives an estimated \(\tau_K \approx 8\) ps. Kinetic inductance thus does not appear to be a limiting factor. Overall, we may expect pTron switching to be on a \(10-100\) ps timescale based on NbN and related materials' parameters.

**Power optimization.** Since the pTron memory device as a whole is non-volatile, there is no dissipation unless data is read, written or erased. The intrinsically low switching energy (< 2.2fJ)\textsuperscript{1} of the CCM devices is comparable with the SC device drivers. Readout is actually non-dissipative in the \(R_{LO}\) state of the state of the device is read with a current in the superconducting range. For example, while \(R_{LO}\) is zero, \(60\mu\)A < \(I_R < 68\mu\)A for the device shown in Fig. 4c. In the resistive range \(I_R > 68\mu\)A, the readout is dissipative, but can be kept small by using short \(R\) pulses. A possibility of reducing the power which has not yet been explored is by reducing the threshold voltage of the CCM, for example by reducing the contact resistance of the Au-TaSi\(_2\) junctions. In the Hi state, the contact resistance \(R_C\) (typically \(~100\) \(\Omega\))\textsuperscript{11} is negligible, but the \(R_{LO}\) state resistance can be significantly reduced if \(R_C\) can be made smaller through different choice of contact metal or the use of a buffer layer. This will have the effect of reducing the shunt resistance, pushing the pTron more in the direction of the PSC regime.

**Conclusions**

We conclude that SC NW nTrons and CCM devices are a good match both in terms of impedance and switching thresholds to allow full control of memory operations by fine tuning of device parameters. The key parameters for achieving a sufficiently large voltage across the NW itself are the critical current \(I_J\) and \(R_S\) of the SC device. To achieve a sufficiently high voltage \(JR_S \sim 0.5\) V across the SC NW, the critical current density \(J_J\) should exceed \(~10\)MA/cm\(^2\), and the normal state sheet resistivity of the film should be \(R_S \sim 500\) \(\Omega/\)s. Such parameters are easily achievable with present NbN or NbTiN thin film technology.\textsuperscript{9,21,32,33} The high speed of the CCM devices and the possibility of writing data with single SFQ pulses energy \(E_F \sim 10^{-3} J\), combined with the use of low loss superconducting microstrip lines that allow ballistic transfer of the picosecond SFQ signals\textsuperscript{8} opens the way to near-THz data memory write operations. Implementation that follows established cross-bar array device architectures\textsuperscript{29} may be used for a making large number of devices on a chip. Further reduction of energy dissipation may be achieved by optimization of shortening of the QP thermalization time in the superconducting device and lowering switching thresholds of CCM devices. The immediate challenges for advancing this technology lie in the co-fabrication of devices that combine 1T-TaSi\(_2\) and superconducting SFQ-based technology.

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