The key design technology of Successive approximation analog-to-digital converter to improve efficient and precision

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Abstract. Transistor with the advent of the Internet of Things era, high efficiency and high precision SAR ADC (Successive approximation analog-to-digital converter) has become a new research hotspot, and the design has certain challenges. By studying the key techniques for improving the efficiency and accuracy of SAR ADC, it is found that using non-binary DACs can greatly improve efficiency, and resize the size of the key parts of the comparator's transistors, which can greatly improve the precision of SAR ADC. Finally, a 14-bit non-binary SAR ADC was designed by IO transistor (this transistor is connected to 2.5V) and core transistor (this transistor is connected to 1.2V). The ENOB has reached 13.6, SNDR has reached 81.16, SFDR has reached 83.23 through simulation test.

1. Introduction
In the Internet of Things era, every object can be addressed, and every object can communicate, and every object can be controlled[1,2]. This requires constant exchange of information between the natural world and the computer. All signals in the natural world are analog signals, and computers can only process binary digital signals. Therefore, analog-to-digital converters have become a hot research topic[3-7]. The analog-to-digital converter (SAR ADC) of the successive approximation structure has high repetitive utilization of circuit modules, requires less analog circuits, has low circuit complexity[8,9], is simple in design, and has low power consumption and cost. Focus. High-precision, high-speed SAR ADCs are widely used in military, aerospace, medical, and control fields and have high research value.

This paper studies the implementation of a 14-bit 3M/s non-binary ADC and passes the simulation test. The whole circuit of SAR ADC is composed of analog circuit and digital circuit. In order to improve the resolution of the circuit, the sampling switch, non-binary DAC, comparator, etc. are built with IO transistor, and the IO transistor has a higher threshold voltage. And connected to 2.5V, this will make the design a higher margin, more than twice the resolution of all using the core transistor to build the circuit. If all the core transistor are used to build the circuit, then 1LSB=1.2/2¹⁴=73.24mV, when using the IO transistor to build the comparator and other circuits, 1 LSB=2.5/2¹⁴=152.59mV, which means that the comparator only needs to resolve the voltage of 152.59mV. The design difficulty is greatly reduced, and the resolution of the ADC of this architecture is further improved. The SAR logic and clock control module is built with core transistor. The SAR logic is mainly composed of registers, which reduces the power consumption and area of the circuit and greatly increases the sampling speed. The circuit of the core tube and the circuit built by the IO transistor are bridged by the high and low level conversion circuit. The main reason for this part of the circuit design is to make the delay as small as
possible, so that the circuit can be completed in a specified period. Generate a digital code. The full circuit design is shown in Figure 1.

2. The theory of Non-binary DAC

The DAC for SAR ADCs is based on a charge-extended architecture. The traditional DAC capacitors follow the binary weight, that is, the capacitance from small to large follows the distribution $C, 2C, \ldots, 2^{N-1}C$, this DAC lineup energy efficiency ratio is not high, the total capacitance will be relatively large, many designs are currently Following the non-binary capacitance ratio, the value of the proportional coefficient $a$ is determined by studying the non-binary characteristic transfer curve. The transfer curves of the three ratios are as follows.

Figure 2(a) is an ideal binary-scale DAC structure, that is, $C_n:C_{n-1}=2^1$, its output is linear, one voltage corresponds to one digital code, and the voltage input is $VFS/2$, the whole analog conversion The result is 10000... or 01111..., the final codeword corresponding to each input voltage is separated by one LSB. Figure 2(b) shows the DAC structure of a capacitor Super-radix-2, i.e. $C_n:C_{n-1}>2$. Its output is non-linear, most of the voltage corresponds to a digital code, and the final codeword corresponding to each input voltage is separated by one LSB. However, when the voltage input is close to $VFS/2$, the whole analog conversion result will be missed, that is, multiple voltages correspond to one output codeword, so that many analog voltage quantities show the same result, and the information will be lost, even if it is It is impossible to restore the previous information through calibration. It is absolutely not advisable to construct a DAC in this way.

Figure 2(c) shows the DAC structure of a capacitor Sub-radix-2, i.e. $C_n:C_{n-1}<2$. Its output is also non-linear, most of the voltage corresponds to a digital code, and the final codeword corresponding to each input voltage is separated by one LSB. When the voltage input is close to $VFS/2$, the whole analog conversion result will be out of code, that is, one voltage corresponds to multiple output code words, which causes one voltage to correspond to multiple code words, but other voltages are corresponding code word. Some information will be redundant. These redundant input information can be eliminated by calibration. Restore to the information you want before, so that the original analog information is not lost. It is theoretically desirable to build a DAC in this way, and the total capacitance will be much smaller than conventional structures.

In this paper, the DAC structure of Sub-radix-2 is determined. The ratio of the upper and lower capacitors is less than 2. Similarly, the formula can be converted into the following formula:

$$\frac{1-a^N}{1-a} + 1 - 2^{ENOB} - 2.70 \sqrt{\frac{1-a^2N}{1-a^2}} + 1 \geq 0$$

(1)
\( \theta \) is very small and can be regarded as 0. Finally, the scale factor required for the target effective number of bits can be calculated according to the calculation. As shown in Table 2.1, it can be seen that the larger the effective number of bits, the larger the required proportional coefficient. This non-binary capacitive DAC array will have a significant bit of 16 bits, and a 16-bit scale factor will be greater than 2, and the non-binary theory will fail.

| ENOB | \( \alpha \) |
|------|--------|
| 16   | 2      |
| 15   | 1.91   |
| 14   | 1.85   |
| 13   | 1.78   |

Finally, according to the calculation, the proportional coefficient required for the target effective number of bits is obtained. As shown in Table 1, it can be seen that the larger the effective number of bits, the larger the required proportional coefficient. This non-binary capacitive DAC array will have a significant bit of 16 bits, and a 16-bit scale factor will be greater than 2, and the non-binary theory will fail.

Applying the above DAC logic timing and improving to a non-binary type, the scale factor is 1.85 and the unit capacitance is 520aF, so the subsequent capacitance is 970aF and 1.8F, and the ratio of the upper and lower capacitors is 1.85. The result of this DAC quantization is non-binary. The output codeword of the last circuit is converted to a binary output by an external circuit. Since the external circuit is used, the overall circuit and various performances of the SAR ADC are not affected. This type of DAC will bring redundant code words to the conversion result, but by studying many existing algorithms, it can be calibrated using a digital perturbation-based algorithm, completely eliminating the adverse effects of redundancy.

At the same time, non-binary DACs bring many benefits, which can eliminate the adverse effects of some process deviation circuit performance. Moreover, using this non-binary structure can save 10 times more power than a DAC with a binary structure, thereby achieving high energy efficiency conversion. The results of the test power consumption simulation are shown in Figure 3.
3. High precision comparator

The 14-bit 2.5V ADC theoretically needs to recognize a minimum voltage of 160μV. This comparator is built on the simulation platform. The comparator as shown in Figure 4 is amplified in the first stage and latched in the second stage. A number of simulations have been used, mainly to adjust the size of the first stage of the two drive transistor M1 and M2 and the tail current transistor M3 and M4 to increase the gain of the entire first stage, and to increase the size of the second stage input transistor M9 and M10. Through dozens of debugging, the resulting comparator has a minimum comparison voltage of 10μV. Finally, the output of the better swing is obtained. The Monte-carlo simulation of the entire offset voltage and the resolution of the circuit operation. The simulation results are shown in Figure 5.

![Comparator structure](image)

**Figure 4** Comparator structure

![Monte-carlo simulation of the entire offset voltage](image)

**Figure 5** Monte-carlo simulation of the entire offset voltage

It can be concluded that the offset voltage of the comparator is only 1.5mV, and the deviation of the offset voltage is only 3.2mV, and the obtained performance is quite good.

As can be seen from Figure 6, the comparator can pass the test simulation, the obtained waveform can recognize the voltage of 10uv, and the overall accuracy obtained is very high.
4. Simulation results

Figure 7 is a full-chip overall circuit. The number 1 represents the sampler, the number 2 represents the DAC, the number 3 represents the disturbance input calibration circuit, the number 4 is the comparator, the number 5 is the high level to low level circuit, the number 6 is the SAR logic circuit, the number 7 is the clock circuit, and the number 8 is a low level to high level circuit, in addition to some other necessary logic operation modules.

By simulating the ADC, the main performance parameters of the SAR ADC were tested by Cadence software based on the CMOS 65nm process. The output signal was converted into a spectrum signal by the fast Fourier transform method to calculate the parameter value. The following parameters are the performance output spectrum of the SAR ADC tested at a supply voltage of 2.5V/1.2V, a target accuracy of 14 bits, and a 3M/s sampling frequency. The result is shown in Figure 8.
5. Conclusion
Under the SMIC65nm process, through the two key design technologies of SAR ADC (non-binary theory and high precision comparator), greatly improving the efficiency and accuracy of the SAR ADC. The whole circuit of 14-bit non-binary SAR ADC is designed by IO transistor and core transistor. The circuit passed the simulation and performance test. ENOB has reached 13.6, SNDR has reached 81.16, SFDR has reached 83.23.

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