Performance Analysis of InP based Composite Channel e-mode HEMT Device for High Frequency Applications

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Abstract: High Electron Mobility Transistor (HEMT) is presently a very important part in the electronics industries for high frequency applications and for low power applications. In this approach, single gate enhancement mode composite channels of In0.7Ga0.3As/InAs/In0.7Ga0.3As HEMT devices are simulated and analyzed for low power operations which leads to strong DC and RF performance. This can be achieved by working on the composite channel which was lattice matched, gate which was recessed and length of the gate which was optimized. In this paper, for various lengths of the gate with constant barrier thickness, the performance of the device is analyzed symmetrically with the specialized device dimensions with thickness of the barrier (T_B) = 2nm, thickness of the channel (T_CH) = 15nm. The length of the gate can be reduced which supports in decreasing the drain resistance, effects of capacitance and improved average electron velocity in the gate. And this in turn results in the best performance of the device metrics with the values, trans-conductance (g_m) as 1741 µS/µm, drain current (I_d) as 0.553574 mA/µm, cut-off frequency (f_T) as 431 GHz, maximum frequency of oscillations (f_max) as 557 GHz.

1. Introduction
The research of ICs had resulted in the design of very high speed & huge packing density ICs with low short channel effects having high RF and DC performances. In defense, consumer and industrial applications, Si CMOS technique has been widely used in the last few decades. The size of the transistor should be reduced to a certain extent with which the speed of the device and the density of the device will be increased efficiently [1-4]. However, short channel effects will be increasing in Si CMOS technique when the size of the transistor gets decreased. For the difficulties which are caused by this Si CMOS technique, there is an alternate solution in which we can combine the III-V compound semiconductor HEMT devices. At present, more demand for low voltage and high speed operations IC’s exists in modern electronics which results in the attraction of InP based HEMTs mainly because of their properties like high carrier density, high electron mobility and also velocity which are used for millimeter and sub-millimeter wave operations and applications. And they show better performance than other compound semiconductor substances like GaAs, GaN and GaP. Using InP related materials, different structures of HEMT can be designed. The source to drain spacing (L_SD) in the HEMT device characteristics plays a vital role in the simulation of the device. The total distance of the source to drain spacing (L_SD) is the sum of the distances for (LSG), (LG) and (LGD), that is, L_SD = (LSG + LG + LGD), where (LSG) is the source to gate spacing, (LG) is the gate length and (LGD) is the gate to drain spacing. For maintaining the proper ratio of device aspect, in most of the InGaAs/InAs/InGaAs HEMT devices, the performance of the device is increased by decreasing the length between source and drain and also gate length is reduced with the reduction of gate to channel distance. Hence this will be the improvement for...
the performance of the devices with respect to high trans-conductance and also performance of RF. However, simultaneously, it degrades the performance of the breakdown voltage [5] and also adds the effects of a short channel with the high leakage in the gate. The most challenging task here is maintaining a high RF and DC performance with the reduction in the effects of short channel. In this project, a composite channel of InGaAs/InAs/InGaAs HEMT is implemented to increase the RF and DC performances. Besides, the gate is stretched up to the etch stop layer which will make a recessed gate. In the reduction of the gate leakage, the gate dielectric substance has an extreme permittivity in the range of 20-30 which will act as an essential role in the performance.

Therefore, in this work, for various gate to drain spacing, the device parameters like threshold voltage, performance of maximum oscillation frequency, cut-off frequency, drain current, trans-conductance of SG composite channel of InGaAs/InAs/InGaAs HEMT structures are analyzed.

In the upcoming sections (II to IV), we will be discussing the device architecture in Section II, results and discussions in Section III and conclusion in Section IV.

2. Device Architecture

The structure of the composite channel InGaAs/InAs/InGaAs HEMT on an InP device is given in Fig. 1. This structure has the InP substrate whose thickness is 300nm. And above that InP layer buffer layer is grown and it has a thickness of 500nm. To decrease the mismatching of lattice between the composite channel and substrate of the device, a buffer layer is introduced. The composite channel consists of two layers which are In$_{0.7}$Ga$_{0.3}$As which has the thickness of 5nm and 3nm and are located in the top and bottom respectively and 7nm thin of InAs channel is inserted within these two channels. InAs layer is inserted because of improving the mobility of the electrons of the channel. To form a quantum well of 2DEG, above this channel, a barrier layer of In$_{0.52}$Al$_{0.48}$As which has 2nm thickness was introduced.

The barrier layer has a material which has a wider band gap and also it was doped heavily. The channel has a material which has a lower band gap and it was undoped. In the junction, quantum well of 2 dimensional is formed at the condition of equilibrium. The mobility will be decreased because of the barrier layer which was doped heavily and that barrier layer forms a scattering of impurities in the well. Between the barrier and the channel layer, a spacer layer of In$_{0.52}$Al$_{0.48}$As is placed. The spacer layer is introduced to reduce the scattering of impurities and the material of the spacer layer is the same as the barrier layer and it was undoped. And also to decrease the scattering of impurity, instead of doping the barrier layer fully, it was partially doped by using the concept of delta doping. Within the layer of barrier, a 2nm doping layer of delta which is $2 \times 10^{17}$ cm$^{-2}$ is created.

![Fig.1. Structure of the device with Single gate InGaAs HEMT](image-url)
And also a 3nm thickness of InP layer of etch stop is formed in order to increase the behavior of the breakdown voltage. To decrease the parasitic capacitance and resistance effect, a structure of multi cap layer is implemented which is upon the layer of etch stop. In$_{0.6}$Ga$_{0.35}$As (2×10$^{19}$ cm$^{-3}$, 4nm), In$_{0.35}$Ga$_{0.65}$As (2×10$^{19}$ cm$^{-3}$, 15nm) and In$_{0.52}$Al$_{0.48}$As (2×10$^{18}$ cm$^{-3}$, 15nm) are composed in the layer of multi cap. At the top of the multi cap, to safeguard the surface and avoid the contamination, a passivation layer of Si$_3$N$_4$ is created. Performance improvement of threshold voltage can be done by introducing gold in the gate part, because of its huge work function which can exhibit 5.45 eV. For the reduction of channel to gate spacing, the gate is continued till the layer of etch stops, as a recessed gate structure. The values of $L_{GD}$ and $L_{SG}$ are fixed accordingly. A n+ material forms the drain and the source region.

3. Results and Discussions

For the purpose of validation, the reports which are extracted from the experiments, are now compared with the simulation results from the TCAD for the same layers of structure [6]. To validate the results properly, a hydrodynamic model was simulated for better performances. The particular physical effects such as mobility which is dependent on doping, narrowing of band gap and effective mass were also included in the simulation. Once if the performed matching is acceptable for the simulated and experimental results, the model parameters which are obtained can be effectively used for the simulation of the proposed HEMT with Single gate composite channel and it also has a same layer structure.

The characteristics of drain of simulated and experimental HEMT structure of Single gate composite channel HEMT is given in Fig. 2. From the diagram, we can infer that the physical properties of the data which was simulated in TCAD was accurately matched with the experimental data.

![Fig.2. Drain characteristics of simulated and experimental structures of Single gate HEMT](image)

The characteristics of $I_dV_g$ of the InGaAs/InAs/InGaAs single gate HEMT composite channel is given in the Fig. 3. The characteristics of the $I_dV_g$ was obtained by making the thickness of the barrier varied from the range of $T_b=2$nm to $T_b=5$nm and by keeping the value of the length of the gate as constant with the value of $L_g=30$nm. The proposed single gate composite channel HEMT device achieved much better performance in the drain current because of its recessed gate and the composite channel structure. The drain current increases because of reduction of the drain-to-source distance [7-10]. And also it is because of the decrease of the capacitance values in the drain.
Fig. 3. Characteristics of $I_dV_g$ for various values of $T_b$ with constant $L_g$

The characteristics of $I_dV_g$ of the InGaAs/InAs/InGaAs HEMT composite single gate channel with the variations in the parameters is given in the Fig. 4. The characteristics of the $I_dV_g$ was obtained by making the length of the gate varied from the range of $L_g=30$nm to $L_g=90$nm and by keeping the value of the thickness of the barrier as constant with the value of $T_b=2$nm.

From the characteristics of the $I_dV_g$, depicted in the Fig. 3 and Fig. 4, we can conclude that the better performances have been achieved by having the thickness of the barrier as 2nm and the length of the gate as 30nm.

And when the barrier thickness still gets decreased, then there will be short channel effects which will be affecting the performances of the parameters like trans-conductance ($g_m$), threshold voltage ($V_T$). Therefore, by having the value of the thickness of the gate as 2nm, we are able to simulate the results for DC and RF characteristics. The value of trans-conductance has been acquired by differing the length of the gate from $L_g=10$nm to $L_g=90$nm and by keeping the value of the thickness of the barrier as constant with the value of $T_b=2$nm which is shown in the Fig. 5.
At the 90nm length of the gate, the obtained trans-conductance is 1535µS/µm. When the value of $L_g$ is decreased, automatically, the value of the trans-conductance is increased. When the $L_g$ value is reduced further, there is an improvement in the trans-conductance value and at 30nm $L_g$, the trans-conductance is 1741 µS/µm. When it is further reduced to 10nm, the trans-conductance value becomes 1441 µS/µm. This is because of the short channel effects which will be affecting the performance of the trans-conductance. The parameters of the trans-conductance are improved by the improvement in the drain current. Then by keeping the values of the $L_g$ constant as 30nm and by varying the values of $T_b$, the
trans-conductance has been achieved which is shown in Fig.6.

![Fig.6. Characteristics of trans-conductance for various $T_b$ and constant $L_g$](image)

For this scenario also, we have obtained almost the same values for trans-conductance which is much better than the existing works. For different values of $L_g$, the threshold voltage is varied and it is given in the Fig.7. An important point to be noted in every device is whether it works in an enhancement mode or the depletion mode [11-12]. Enhancement mode HEMTs are demandable in most of the applications of the digital environment. The proposed single gate HEMT with composite channel exhibits a threshold value which is positive and therefore it can be used for the enhancement mode applications efficiently. From the Fig.7, it can be seen that when the length of the gate decreased from 30nm to 10nm, negative threshold voltage is appearing and therefore, for the gate length of 30nm, the performances have been improved. The threshold voltage at 10nm is -0.0892 V and at 30nm is 0.0345 V.

The better performance of RF can be achieved by this system because of the composite channel, high mobility, reduction in the barrier and the length of the gate, reduction in the channel to gate spacing with the structure of recessed gate. The $f_T$ (cut-off frequency) and $f_{max}$ (maximum frequency of oscillation) values mainly depend on,

$$f_{max} = \frac{g_m}{2\pi c_{gs} \sqrt{4(R_s + R_i + R_g)(g_{ds} + g_m \frac{c_{gs}}{c_{gs}})}}$$
From the above formula, it can be seen that when the value of the trans-conductance gets increased, the value of the maximum frequency also increases. The capacitance effect also decreases, which in turn increases the frequency. For the different values of $L_g$, with constant $T_h$ the cut-off frequencies have been calculated and it is noted that at $L_g=90\text{nm}$, the $f_T$ is 246 GHz and at $L_g=30\text{nm}$, it was 431 GHz. Performance characteristics of $f_T$ single gate HEMT with composite channel is given in Fig. 8.
For the different values of $L_g$, with constant $T_b$, the maximum frequencies of oscillations have been calculated and it is noted that at $L_g=90$nm, it was found that the $f_{max}$ is 456 GHz and at $L_g=30$nm, it was 557 GHz. Performance characteristics of $f_{max}$ single gate HEMT with composite channel is given in Fig. 9.

![Fig.9. Characteristics of Maximum frequency for various $L_g$](image)

4. Conclusion
In this paper, with respect to RF and DC performances, the results of gate-to-drain distance with respect to several parameters have been analyzed in the Single gate HEMT of In$_{0.7}$Ga$_{0.3}$As/InAs/In$_{0.7}$Ga$_{0.3}$As composite channel with the help of the simulation tool TCAD. Keeping the values of $T_b$ constant as 2nm, the length of the gate has been varied from the range of 30nm to 90nm respectively. From the results, we can conclude that at 30nm, the drain current was 0.553574 mA/µm and at 90nm, it was 0.4839 mA/µm. And the trans-conductance at 30nm was 1741 µS/µm and at 90nm, it was 1535µS/µm. Then the threshold voltage at 10nm is -0.0892 V and at 30nm is 0.0345 V. At 30nm and 90nm, the cut-off frequency calculated are 431 GHz and 246 GHz respectively. And the maximum frequency was calculated as 557 GHz and 456 GHz at 30nm and 90nm respectively. When the length of the gate gets reduced, the drain resistance will be decreased and the values of drain current, cut-off frequency, threshold voltage and the trans-conductance will get improved [13-15]. Reduction of the parasitic capacitance values by the means of multi cap layers and by introducing the structure of recessed gate oxide and by reducing length of the gate, this proposed system had achieved an excellent performance.

References
[1] Ajayan J and Nirmal D 2017 20-nm enhancement-mode metamorphic GaAs HEMT with highly doped InGaAs source/drain regions for high-frequency applications Int. J. Electron. 104 3 pp 504–512
[2] Radhakrishnan S.K, Subramaniyan B, Anandan M, and Nagarajan M 2018 Comparative assessment of InGaAs sub-channel and InAs composite channel double gate (DG)-HEMT for sub-millimeter wave applications AEU - Int. J. Electron. Commun. 83 pp 462–469
[3] Chang E.Y, Kuo C.I, Hsu H.T, Chiang C.Y and Miyamoto Y 2013 InAs thinchannel high-electron-mobility transistors with very high current-gain cutoff frequency for emerging submillimeter-wave applications Appl. Phys. Express 6 3 pp 1–3
[4] Kim T.W and del Alamo J.A 2011 Injection velocity in thin-channel InAs HEMTs IPRM 2011 - 23rd Int. Conf. on Indium Phosphide and Related Materials pp 1–4
[5] Tae-Woo Kim, Dae-Hyun Kim, Sang Duk Park, Geun Young Yeom, Byeong Ok Lim, Jin-Koo Rhee, Jae-Hyung Jang and Jong-In Song 2007 Effect of a Two-Step Recess Process Using Atomic Layer Etching on the Performance of In0.52Al0.48As/In0.53Ga0.47As p-HEMTs IEEE Electron Device Letters 28 12 pp 1086-1088

[6] Chien-I Kuo, Heng-Tung Hsu, Senior Member, IEEE, Edward Yi Chang, Senior Member, IEEE, Chia-Yuan Chang and Yasuyuki Miyamoto 2008 RF and Logic Performance Improvement of In0.7Ga0.3As/InAs/In0.7Ga0.3As Composite-Channel HEMT Using Gate-Sinking Technology IEEE Electron Device Letters 29 4

[7] Saravana Kumar R, Mohanbabu A, Mohankumar N and Godwin Raj D 2018 Simulation of InGaAs Sub-channel DG-HEMTs for analogue / RF applications Int. Journal of Electronics 105 3 pp 446-456

[8] Vasallo B.G 2007 Comparison between the dynamic performance of double and single-gate AlInAs/InGaAs HEMTs IEEE Trans. Electron Devices 54 11 pp 2815–2822

[9] Mimura T, Endoh A, Matsui T, Shinohara K, Hikosaka K and Awano Y 2010 Effect of Gate–Drain Spacing for In 0.52 Al 0.48 As/In 0.53 Ga 0.47 As High Electron Mobility Transistors Studied by Monte Carlo Simulations Jpn. J. Appl. Phys. 49 1 pp 014301

[10] Xu D 2012 50-nm asymmetrically recessed metamorphic high-electron mobility transistors with reduced source-drain spacing: Performance enhancement and tradeoffs IEEE Trans. Electron Devices 59 1 pp 128–138

[11] Nirmal D, Vijayakumar P, Shruti K and Mohankumar N 2012 Nanoscale channel engineered double gate MOSFET for mixed signal applications using high-k dielectric Int. Journal of circuit theory and applications 41 6 pp 608-618

[12] Kharchenko V.A 2017 Buffer layers in heterostructures Mod. Electron. Mater. 3 4 pp 154–157

[13] Farhan Aziz and Siddiqui MJ 2011 Optimization of δ-doped AlInAs/InGaAs HEMT Performance Using Spacer Layer and δ-doping Int. Conf. on Multimedia, Signal Processing and Communication Technologies pp 236-239

[14] Mimura T, Endoh A, Matsui T, Shinohara K, Hikosaka K and Awano Y 2010 Effect of Gate–Drain Spacing for In 0.52 Al 0.48 As/In 0.53 Ga 0.47 As High Electron Mobility Transistors Studied by Monte Carlo Simulations Jpn. J. Appl. Phys. 49 1 pp 014301

[15] Shinohara K, Yamashita Y, Watanabe I and Mimud T 2004 Nanoscale InP HEMT Technology for Ultrahigh-speed Performance Int. Conf. on indium phosphide and related materials pp 721–726