Utilization of a Cryo-Prober System for Operation of a Pulse-Driven Josephson Junction Array

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Abstract. We demonstrated the operation of pulse-driven Josephson junction arrays (JJAs) for AC voltage standard using a wideband cryo-prober system with a 4-K Gifford-MacMahon (GM) cooler. This unique system was originally developed for high-speed network switch applications of rapid-single-flux-quantum (RSFQ) circuits and enables wideband data transmission at bit rates of higher than 10 Gbps between room-temperature and cryogenic environments. JJA chips were fabricated using NbN-based superconductor–normal metal–superconductor (SNS) junctions. A 5-mm chip was mounted on a 16-mm chip carrier using flip-chip bonding technology for probe contact. To obtain bipolar output voltages, we tried two types of testing based on the AC coupling technique proposed by the National Institute of Standards and Technology (NIST). A pulse pattern generator (PPG) with a large memory of 134 Mbit was used for covering a wide frequency range of output signals. As a result, we succeeded in bipolar operation of the JJA, generating waveforms at frequencies from 60 Hz to several tens of kilohertz. The maximum rms voltage obtained for a single array was 12.7 mV. The observed spurious level was lower than $-93$ dBc at 16 kHz.

1. Introduction

The development of next-generation AC voltage standard systems based on the Josephson effect is an important and interesting task for both metrological studies and industrial applications. At present, AC voltages are generally calibrated using their rms values through AC-DC transfer standard based on a thermal converter. On the other hand, the new systems using the Josephson voltage standard (JVS) can realize direct calibration for instantaneous values and waveforms of the AC voltages with higher accuracy. The Josephson arbitrary waveform synthesizer (JAWS) proposed by the National Institute of Standards and Technology (NIST) is one of the most promising techniques to cover a high-frequency range from kilohertz to megahertz [1]. In a JAWS, a Josephson junction array (JJA) is driven with a digital bit stream of pulse currents, instead of a microwave as used for the conventional JVSs. This
pulse-driven-type JJA, a single-bit digital-to-analog converter (DAC), can operate without changing DC biases for the junctions and is free from the transient errors arising in multi-bit DAC type JJs [2]. Benz et al. reported a record rms voltage of 275 mV, aiming at the eventual goal of a 1 V system [3].

For successful operation of JAWS with wide margins, it is essential to achieve high-frequency pulse transmission with low dissipation from room-temperature equipment to a low-temperature JJA device. In addition, thermal inflow via RF cables must be suppressed below the cooling capacity. This requirement is important especially when a mechanical cooler is used.

In this paper, we demonstrate the operation of pulse-driven JJs using a liquid-helium-free 4-K cryo-prober system, which was originally developed by SRL-ISTEC for testing rapid-single-flux-quantum (RSFQ) network switch devices [4]. Our goal is to realize more compact and convenient systems for AC-JVS.

2. Experimental

2.1. 4-K Cryo-Prober System

Figure 1 shows a photograph of our cryo-prober system cooled with a 4-K Gifford-MacMahon (GM) refrigerator (Sumitomo RDK-408D). The system has 32-channel wideband I/O ports (≥ 10 Gbps/ch) with the total thermal inflow via the cables below a cooling power of the cooler, 1 W at 4.2 K [5]. The system enables high-frequency pulse transmission between the room-temperature and the cryogenic environments with low dissipation. A JJA device is packaged on a 4-K cold stage using a wideband probe system (Kawashima Manufacturing Co., Ltd), as shown in the inset of figure 1. Each probe has a co-planer waveguide (CPW) shape; thus, wideband electrical contacts are realized with a low loss and a small impedance mismatch. The system also has a 40-Gbps optical input port connected with a uni-traveling-carrier photodiode (UTC-PD) module (NTT Electronics) at the 4-K cold stage [6]. The system was utilized for another experiment for driving our JJA devices with optical input pulses [7].

Figure 1. Photograph of a 4 K cryo-prober system.

2.2. Josephson Junction Array Chips

Over-damped JJA chips were fabricated using NbN-based superconductor–normal metal–superconductor (SNS) junctions with TiN barriers [8]. The junctions had critical current-normal resistance (IcRn) values of ten to several tens of micro-volts at 4 K. Though the junctions showed hysteresis in current–voltage characteristics at 4 K, it was suppressed by controlling device
temperature with a resistive heater during the testing. A fabricated 5 mm × 5 mm JJA chip was flip-chip bonded to a 16 mm × 16 mm chip carrier with CPW-shaped plated gold pads for probe contact (figure 2). The bonding pads had a diameter of 50 μm and were designed to maintain a transmission-line impedance of 50 Ω [5].

**Figure 2.** Photographs of (a) a JJA chip with three 1600-junction arrays fabricated using a NbN-based SNS junction process and (b) the chip mounted on a chip carrier for probe contact.

2.3. Measurement Setups
To obtain bipolar voltage signals from the JJA, various types of measurement setups have been proposed and tested [9]. In this study, we tried two types of setup (Setups A and B) with different pulse sources, as shown in figure 3. The pulse pattern generator (PPG) used in this study (Anritsu MP1800A) has a large memory of 134 Mbit, enabling the JJA to generate waveforms at commercial frequencies of around 60 Hz when the PPG is clocked at a data rate of 8 Gbps. Data bit patterns, which were programmed to the PPG memory, were calculated based on a second-order delta-sigma modulation method.

**Figure 3.** Block diagrams for (a) an AC coupling measurement [10] (Setup A) and (b) a measurement using a two-channel PPG (Setup B).
In Setup A, which is based on the AC coupling technique proposed by the NIST [10], a digital bit stream in a non-return-to-zero (NRZ) format from a PPG is converted into a return-to-zero (RZ) format by mixing with a sinusoidal signal at a frequency equal to the PPG clock frequency or higher. The resultant pulse train in the RZ format drives the JJA through a capacitance (DC block). To compensate the low-frequency components eliminated with the DC block, a signal generator (indicated as “SG (LF)” in figure 3 (a)) feeds a low-frequency compensation current directly to the JJA from other ports. This setup realizes finely shaped bipolar RZ pulse trains with sufficiently large amplitude (figure 4 (a)), although the number of parameters (e.g., the phase between the PPG and the signal generators) to be adjusted should increase.

In Setup B, outputs from two channels of a PPG were simply mixed using a power divider (figure 3 (b)). We used a “data” output with positive polarity for one channel and a “data bar” output with negative polarity for the other channel. By programming the data bits for each channel in an RZ format appropriately, one can obtain a bipolar pulse train, as shown in figure 4 (b). This setup could reduce the number of parameters, although the amplitude and clock frequency of the output pulses are restricted by the PPG performance.

![Figure 4. Waveforms of bipolar RZ pulse trains in (a) Setup A and (b) Setup B for driving JJAs.](image)

3. Results and Discussion

For both types of setup, we succeeded in generating bipolar sinusoidal voltage waveforms. Figure 5 (a) shows a waveform at a frequency of 16 kHz with peak-to-peak amplitude of 36.1 mV, corresponding to an rms voltage of 12.7 mV, which was synthesized using Setup A. The testing was carried out using a digitizer (National Instruments PXI-5922) with a 1-MΩ input impedance and a 2-V range. The obtained peak-to-peak voltage coincides well with the calculated value of $V = amnf_{clk}/K_J = 0.65 \times 1600 \times 2 \times 8.388 \text{ GHz} / 483597.9 \text{ GHz/V};$ here, $a$ is the modulation ratio of the bit stream, $m$ is the junction number, $n$ is the order of steps (using 1 and −1 steps gives $n = 2$ in this experiment), $f_{clk}$ is the clock frequency of the pulse train, and $K_J$ is the Josephson constant ($K_{J_{90}}$). The frequency spectrum of this signal is shown in figure 5 (b). The highest harmonic peak is 93.2 dB lower than the fundamental (−93.2 dBc).

Figure 6 shows a waveform at 62.5 Hz, close to a commercial power-line frequency of 60 Hz, synthesized using the full memory length of the PPG. The frequency of the waveform was determined as $f_{sig} = f_{clk}/L_{data} = 8.388 \text{ 608 Gbps/134 217 728 bit} = 62.5 \text{ Hz},$ where $L_{data}$ is the memory length of the PPG. In this testing, some system noise still remains, as discussed later; the obtained spurious level is about −60 dBc.
Figure 5. Measured (a) waveform and (b) FFT spectrum of a 16 kHz AC voltage signal synthesized using Setup A. The data was measured at a sampling rate of 4 MS/s.

Figure 6. Measured (a) waveform and (b) FFT spectrum of a 62.5 Hz AC voltage signal synthesized using Setup A. The data was measured at a sampling rate of 100 kS/s.
We also succeeded in synthesizing AC voltage waveforms using Setup B, as shown in figure 7. In this testing, the PPG was clocked at 10.485 760 GHz, which corresponds to the actual clock frequency for the RZ pulse train of 5.242 880 Gbps. The obtained peak-to-peak amplitude of 22.5 mV coincides well with the estimated value. The spurious level was about –87 dBc.

In our present system, which was originally developed for a digital communication network application (i.e., not for metrology), the outers of the signal cables are connected to a common ground. Therefore, unintended ground loops exist, possibly causing various noises associated with, for example, the AC power lines and the mechanical cooler. Moreover, large DC voltages associated with thermal electromotive force appear in the cables in this system. We consider that these system features are one of the causes for the peaky FFT background as shown in figure 7 (b), possibly affecting the operation of the JJAs. We are now attempting to solve these problems in the present system and to develop a new cryo-prober system suitable for the metrological applications.

4. Conclusion
We introduced a unique system for the demonstration of an AC-JVS: a 4-K cryo-prober system originally developed for RSFQ digital network devices. This system has multi-channel wideband I/O ports with CPW-shaped contact probes, enabling the data transmission at bit rates of higher than 10 Gbps between room-temperature equipment and cryogenic JJA devices cooled with a GM refrigerator. To synthesize bipolar AC voltage waveforms, we used two types of measurement setup: (A) a combination of a PPG and signal generators for the ordinary AC coupling measurement and (B) a two-channel PPG. Using these cooling and measurement setups for a pulse-driven JJA, we succeeded in generating AC sinusoidal waveforms in a frequency range from a commercial frequency of 60 Hz to several tens of kilohertz. The maximum rms voltage obtained for the 1600-junction array was 12.7 mV. The spurious level was lower than –93 dBc at 16 kHz. Further improvements in the present system will enable us to obtain higher output voltages at lower spurious levels.

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