FPGA Design Techniques for Stable Cryogenic Operation

Harald Homulle,1, a) Stefan Visser,1 Bishnu Patra,1 and Edoardo Charbon1, b)
QuTech, Delft University of Technology, 2628CD Delft, The Netherlands

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In this paper we show how a deep-submicron FPGA can be modified to operate at extremely low temperatures through modifications in the supporting hardware and in the firmware programming it. Though FPGAs are not designed to operate at a few Kelvin, it is possible to do so on virtue of the extremely high doping levels found in deep-submicron CMOS technology nodes. First, any PCB component, that does not conform with this requirement, is removed. Both the majority of decoupling capacitor types and voltage regulators are not well behaved at cryogenic temperatures, asking for an ad-hoc solution to stabilize the FPGA supply voltage, especially for sensitive applications. Therefore, we have designed a firmware that enforces a constant power consumption, so as to stabilize the supply voltage in the interior of the FPGA chip. The FPGA is powered with a supply at several meters distance, causing significant IR drop and thus fluctuations on the local supply voltage. To achieve the stabilization, the variation in digital logic speed, which directly corresponds to changes in supply voltage, is constantly measured and corrected for through a tunable oscillator farm, implemented on the FPGA. The method is versatile and robust, enabling seamless porting to other FPGA families and configurations.

I. INTRODUCTION

The cryogenic operation of electronic circuits in general and FPGAs in particular has been extensively studied over the past years1–6. The majority of the FPGA building blocks, in Xilinx Artix 7 series for instance, has been shown to operate rather stably over the temperature range from 4 K to 300 K5,6. For example, the delay change in both look-up tables (LUTs) and carry elements has been shown to change by less than 10%.

Although the performance of FPGAs operating at deep-cryogenic temperatures is shown to be stable, this is only demonstrated in specific cases, e.g. when building blocks were tested individually. This tests ignored the influence of voltage drop due to long wires used to bring power supply and also the influence the blocks might have on one another. Furthermore, the behaviour of other components, ancillary to the FPGA, is not well known. This is of particular importance when, as it is the case in this work, a platform is to be implemented to control a quantum processor.

The most important components for such a platform are a power decoupling network and DC power supplies or voltage regulators. Capacitors in general tend to drop significantly in capacitance and they increase the effective series resistance by up to 1000×7–11. Previous studies2,13 have shown some voltage regulators to operate at cryogenic temperatures, as low as 90 K, but no regulators were found to be working stably below that temperature due to either protection circuitries, bipolar transistors14,15 or biasing.

Power networks, that do not behave properly, can pose a burden on optimal FPGA performance, especially at cryogenic conditions where the power is supplied over long wires. While FPGAs switch significant amounts of current at high frequencies, fluctuating IR drop over these wires can be significant. While a static IR drop wouldn’t cause significant problems, the dynamic IR drop alters the internal delays of the FPGA continuously, causing potential glitches and irregularities. Usually, these problems are mitigated using decoupling capacitors, but the performance of capacitors at cryogenic temperatures is not sufficient to compensate for these fluctuations.

In this paper we propose a novel methodology to implement hardware modifications in FPGAs via firmware design, so as to compensate for any potential fluctuations of power dissipation due to sub-optimal structures or biasing in the interior of the FPGA. The same technique can be applied to ASICs, where similar desired effects can be achieved at a wide variety of temperatures. The technique is based on real-time measurements of the variation of cell delay in the carry chain. This fluctuation is mainly caused by voltage drop of the logic supply voltage, but it is also caused by temperature fluctuations. A small farm of oscillators is used to flatten out the power consumption in real-time, so as to automatically stabilize the power supply as well.

Similar techniques have been shown before, but mainly for the purpose of avoiding security attacks. In those systems, the power consumption or heat has to be flattened in order to prevent one from reading data through power or heat changes. For instance,16 proposes the use of a distributed oscillator farm to equalize the heat map from the FPGA seen from outside. Its control is based on the difference in frequency shift of two differently sized ring oscillators, which is proportional to temperature.

In this paper, we first study the behaviour of (passive) decoupling capacitors and (active) voltage regulators in Section II. In Section III we propose an architecture, implemented inside the FPGA to stabilize power consumption. Results showing the effectiveness of the stabilization technique are presented in Section IV.

1 Electronic mail: h.a.r.homulle@tudelft.nl
2 The following article has been submitted to Review of Scientific Instruments. If it is published, it will be available on http://rsi.aip.org.
II. PASSIVES AND ACTIVES

A. Capacitors

Passive components form an important part of any PCB design, whether the PCB houses an FPGA or ASIC as the main embodiment. Especially capacitors, which are not only used for the decoupling networks of power supplies, but also for analog filters, are important. At cryogenic conditions, the material properties can differ significantly, altering the dielectric values and thus the resulting junction capacitance and/or resistance. As this is such an important part of any system, a study was conducted to find the optimal capacitor materials that are commercially available. For some applications, it might be worth investigating the performance of cryogenic specialized materials.

Several studies\textsuperscript{7–11} revealed that significant changes are to be expected, with a large dependency on material dielectric properties. For example high k-dielectric constant materials, such as X5R or X7R, drop almost to zero capacitance, while low k materials, such as NP0, are very stable.

FPGA systems in particular require a large decoupling network, with capacitance values ranging from 1 to 330 µF. With this large diversity, it is impossible to use only one dielectric (due to size and availability), and a solution for the higher values has to be found. Tantalum capacitors seem a good trade-off between performance and available values\textsuperscript{8,10}. There are also special tantalum capacitors available for cryogenic applications, but their performance is only optimal down to 77 K.

In Table I an overview of the tested capacitors is given together with their type and values. Listed are the capacitors currently used on the FPGA PCB and some potential better candidates, with the measured capacitance and effective series resistance at 4 K and 300 K. Tests were executed using a KeySight LCR meter and a test frequency of 100 Hz. The variance of both capacitance and effective series resistance (ESR) are mainly dictated by the material type. Clearly NP0/COG and PPS capacitor materials are ideal with both limited change in capacitance and no significant increase in ESR as a function of temperature. The worst capacitors are based on ceramic materials with high dielectric constants. In these devices, the capacitance drops over 90% and ESR increases over 3000%.

The relative capacitance and ESR over temperature are plotted in Fig. 1(a) for some of the capacitors from Table I. For the ceramic capacitor, the capacitance drops almost linearly with respect to temperature. The ESR on the other hand increases quasi exponentially while lowering temperature as is shown in Fig. 1(b). More extensive characterization results are reported in Appendix A.

For optimal cryogenic performance of the decoupling network, selecting the appropriate capacitor type is important. Special cryogenic capacitors, based on tantalum EPPL2\textsuperscript{17}, were tested and found to be generally better down to 77 K. At 4 K however, those capacitors significantly loose capacitance and increase ESR. Another type of capacitor is based on silicon, which is only available for small values under 1 µF. Those capacitors exhibit a very similar performance to NP0/COG types, with as main advantage, a significantly smaller footprint. As space is limited in dilution fridges, significantly smaller components are preferable.

B. Resistors

Although not as important as capacitors, resistors are commonly used for filters, protection circuits, termination etc. Therefore, the behaviour of resistances at cryogenic temperatures has to be well understood. As for capacitors, several resistive materials have been studied in the past\textsuperscript{10}. Metal film resistors are found to be most stable over temperature, with fairly limited change in resistance (<1%). The resistance over temperature for three SMD resistors, both metal and thick film, is shown in Fig. 2, confirming the extremely stable resistance of metal films over temperature.

C. Voltage regulators

Voltage regulators or DC-DC converters and also voltage references form the core of any power distribution network. Especially for FPGA systems with significant switching currents, the voltage regulation has to be done as close as possible to the FPGA in order to reduce latency and thus increase stability and reduce IR drop. As the wire length into any cryogenic system is generally several meters long, voltage regulation at cryogenic temperatures can significantly improve system stability and performance.

Previous studies have shown operating voltage regulators, however the temperature range was generally limited to 77 K. Simple shunt regulators based on Zener diodes have been shown to operate down to 100K with relatively stable performance\textsuperscript{13}. Also low drop-out

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure.png}
\caption{Relative capacitance and ESR for some of the capacitors from Table I over temperature.}
\end{figure}
TABLE I. Summary of the performance change of several capacitors as used on the FPGA platform PCB and some potential better candidates. All values are measured at a test frequency of 100 Hz.

| Specified capacitance [µF] | Type   | Part number                          | 300 K Capacitance [µF] | ESR [Ω] | 4 K Capacitance [µF] | ESR [Ω] | ΔC [%] | ΔESR [%] |
|---------------------------|--------|--------------------------------------|------------------------|---------|----------------------|---------|--------|----------|
|                           | PP5    | C2200C474J5GACTU                     | 0.475                  | 0       | 0.475                | 0       | 0      | ∞        |
| 1                         | PPS    | SMDIC04100TB00KQ00                    | 1.01                   | 0       | 1.02                 | 0       | 1      | 0        |
| 47                        | X5L    | C1206C475JSNACTU                     | 4.75                   | 6       | 0.32                 | 189     | −93    | 3050     |
| 100                       | Tantalum | 16TQC473M0W                         | 44.5                   | 0.8     | 38.2                 | 0       | −14    | −100     |
| 330                       | Tantalum | T495D107K010ATE050                   | 102.8                  | 0.2     | 91.9                 | 1.8     | −11    | 800      |
|                           | PPS    | SMDIC03470TB00KQ00                    | 0.475                  | 0       | 0.478                | 0       | 1      | 0        |
| 1                         | Silicon| 935133427710-T3N                      | 1.03                   | 1.4     | 1.01                 | 0       | −2     | −100     |

FIG. 2. Relative resistance for different materials (metal and thick film) over temperature. More detailed plots are shown in Appendix A.

(LDO) voltage regulators have been shown to operate down to 77 K. Several voltage regulators have been tested in the temperature range from 4 K to 300 K and the output voltage is plotted versus temperature in Fig. 3(a). Measurements were done at the specified $V_{\text{in}}$ and the regulators were loaded with 100 Ω. As can be seen, none of the regulators are stable in voltage over the complete temperature range. To concretize functionality, a 2.5% margin was allowed on the output voltage with respect to room temperature. The corresponding output voltage plots for all regulators are presented in Appendix B. The best performing regulator was found to be an LDO from Texas Instruments (TPS7A7002, Fig. 14(h)), at least in terms of output voltage. The device is extremely stable down to 90 K, at which temperature it completely turns off.

Besides a stable output, the power consumption is extremely important at cryogenic temperatures, due to limited power budgets in any cryogenic system. The power consumed in the same set of regulators is shown in Fig. 3(b). It is well known that switching voltage supplies outperform other regulator types in terms of power consumption, as is also shown here.

Of course the main trade-off is regulator stability versus noise (output ripple etc.) versus power consumption. In general, switching supplies introduce more noise, while consuming less power. LDOs introduce very limited amounts of noise, while due to the drop-out behaviour, the power consumption is higher.

Extensive characterization results of the various voltage regulators are reported in Appendix B.

In this study, no regulators were found to operate reliably below 60 K, however when operating the FPGA system, it is preferable to operate the regulators at 4 K to be able to integrate them as close as possible to the FPGA. This can be achieved either in the form of a discrete regulator, built from components operating at cryogenic temperatures, or by an FPGA based solution.

In the next section, we propose a technique for stabilizing the FPGA supply voltage from within the FPGA, (partially) eliminating the need for an external regulator.

III. INTERNAL REGULATION ARCHITECTURE

A. Measurement set-up

The problematic IR drop is mainly caused by powering an FPGA over extremely long wires (compared to regulating the voltage on the PCB itself). The wire length is needed, because the power has to be supplied from outside the cryogenic environment, as the power supplies don’t work at these temperatures. The measurement set-up is schematically drawn in Fig. 4. As can be seen, there are roughly 2 meters of wires from supply towards the cryogenic set-up and roughly 1.5 m within the cryogenic set-up. While different cable types have to be used, low ohmic wires do not represent a problem at room temperature, but cause significant heat injection into the cryogenic environment. The main resistive path is therefore the cryogenic cable, which is estimated to be roughly 0.2 Ω for $R_+$ and 0.1 Ω for $R_-$. Besides the problems arising from these resistances, as will be discussed in the next section, latency is the second issue. While the power supplies will have finite reaction time, longer wires will inherently make the reaction time longer and thus the effect of IR drop worse, especially at the time of switching from low to high power consumption.

B. Operating principle

To regulate the voltage from within the FPGA, the power consumed by the FPGA has to be made constant, so as to keep internal delays also constant. To achieve constant power consumption, an architecture was developed to monitor the FPGA’s internal delays and act upon detected variations.

The operation and its results are schematically drawn in Fig. 6. In (a) the operation without regulation is shown. In this example, the system is triggered at a certain time to start with an operation. At that time, the power consumption is suddenly increased, in this example from 0.25 to 0.4 W. The resulting voltage on the FPGA is dropped, with 4% when assuming a resistive...
FIG. 3. Output voltage and consumed power of several DC-DC converters / voltage regulators over temperature. All tested regulators fail operation at temperatures roughly below 90 K when assuming a 2.5% margin on the voltage at 300 K. More complete characterization can be found in Appendix B.

FIG. 4. Schematic drawing of the FPGA operating at cryogenic temperatures while supplying its power through long wires coming from room temperature.

drop in the cable of 0.3 Ω from 1.03 to 0.98 V. As a result, the propagation delay of the carry chain is increased by approximately 16% or 4 ps. This change is significantly more than the 4% drop in voltage thanks to their semi-exponential relationship as shown in Fig. 5.

With the regulation turned on, this effect is effectively smoothed, as shown in Fig. 6(b). The power consumption before the system is triggered is slightly higher than that in the non-regulated system, around 0.5 W, after the trigger, the power consumption remains stable. While this technique can achieve a more stable system, the main drawback is the increased power consumption. This is especially important for designs operating at cryogenic temperatures, for which the power budgets are limited.

FIG. 5. TDC resolution or carry delay versus the internal FPGA supply power (VCC_INT) at both 300 K and 4 K.

FIG. 6. Principal effects of the power stabilizer on the FPGA voltage and the resulting delay of the carry elements, i.e. the resolution of the TDC. The resistive loss in the cables is approximately 0.3 Ω, while the power dissipated by the system is 0.25, 0.4 and 0.5 W, respectively in steady-state, after the trigger and with the stabilizer active.

These problems can be partially addressed with a supply capable of forcing and sensing the voltage through different terminals. In this way, the voltage is measured closer to the FPGA through high-ohmic contacts and the supply can therefore adjust its internal voltage to compensate for the IR drop in the cables. In practice, this technique is limited by the bandwidth of the feedback and the supply is not always capable of acting quickly and accurately enough, especially with a system switching current frequently and at a high rate.
C. Implementation

To achieve the stabilization of the supply voltage, a small oscillator farm is employed together with a regulator consisting of a time-to-digital converter, an IO delay block and some control logic. The complete circuit is shown in Fig. 7.

The internal clock signal, coming from an MMCM (mixed-mode clock manager) digital clock manager, is used as stable reference. It is routed through an IO delay block and a carry chain towards a small TDC. This TDC constantly measures the timing of the clock edge. At system start-up, the IO delay is used to shift the clock edge to the middle of the TDC range. As a result, the output of the TDC should be constantly indicating half of its range, as the position of the clock edge.

However, as a result of IR drop and consequent shifts in logic delay, this is not the case. As the IR drop increases, the delay of the elements increases and the edge will shift to a higher TDC output. On the other hand, with lower power consumption, and thus lower IR drop, the internal logic will be faster and the edge will shift to lower TDC values. As the TDC is one of the most precise elements in the FPGA, the changes can be significant even with slight variations in the power consumption, as discussed in the previous section.

To correct for the changes in power consumption, oscillators in the farm are turned on or off depending on the direction of the shift. With lower measured TDC output, some oscillators are turned on. Higher TDC output will lead to a decrease in the amount of enabled oscillators.

The TDC is operated with a 400 MHz clock, while decisions are made at 6.25 MHz. To average out noise and jitter in the TDC, the result of 64 consecutive measurements is taken as a measure for the required increase or decrease in the number of enabled oscillators. First, four results are added to cross from the 400 MHz to the 100 MHz clock domain. The remainder is processed using an infinite impulse response (IIR) filter before taking a decision to increment or decrement the number of running oscillators.

The oscillators are each implemented with 6 LUTs configured as buffers and one NAND gate as the first stage. The number of oscillators required greatly depends on the remainder of the implemented design and the power consumed in the core circuitry. Firstly, the minimum and maximum power consumption of the core circuitry has to be roughly known. Afterwards, the number of implemented oscillators should be capable of bridging the gap between minimum and maximum power consumption with some margin.

In our design, the core circuit is our analog-to-digital converter\textsuperscript{18}, which dissipates in idle mode 250 mW and at maximum conversion rate about 400 mW. To bridge this gap, four farms were implemented, each containing 128 oscillators. Therefore, the total number of active oscillators out of the 512 oscillators can be incremented or decremented four at a time.

IV. RESULTS

A. Voltage regulation

The implemented system consists of our 1.2 GSa/s ADC\textsuperscript{18} combined with the voltage regulation circuit as discussed in the last section. The ADC is triggered at time $t = 0$ to start converting the analog input and store this data in the internal FPGA memory. At time zero, the power consumption is significantly increased for the non-stabilized system, as shown in Fig. 8. In (a), the ADC starts converting a sinusoidal signal with a 2 MHz frequency, while in (b), the conversion is done with a 40 MHz input signal. Although the difference in power consumption between these two cases is small, about 2.5%, it will still affect the signal-to-noise ratio (SNR). The main problem for our ADC though is the difference between calibration and final conversion. While the calibration is done with signals in the low kHz frequency range, the difference in the power consumption is more significant. In principle, the final conversion system sta-
Figure 8. Measured FPGA current with stabilizer turned on and off at 300 K and 15 K. At time \( t = 0 \), the ADC starts a measurement with an input sinusoid of 2 MHz in (a) and 40 MHz in (a).

B. Calibration and conversion

Although we can indeed see a significantly more stable current over time, the question remains whether that improves the performance of our ADC. To study the performance of the ADC, tests were done in the four operating conditions, with and without stabilization at 300 K and 15 K.

First, the ADC is calibrated at both temperatures. Using the calibrations sets, measurements were performed with an input sinusoidal signal of 2 and 40 MHz. The results for the 2 MHz conversion are shown in Fig. 9. As the ADC is built-up from 12 individual sources, i.e. 6 TDC channels and all measuring rising and falling edges, the calibration is essential. In Fig. 9, the resulting sine wave is shown after merging 12 sources and applying the calibration. The digitized sine waves can be seen to be quasi spur free when the stabilizer is used. However, especially at 15 K, the result is not as clean as at 300 K. This can be partially explained by the non-equalization of the current at 15 K, as shown before in Fig. 8, but is also caused by the decreased decoupling capabilities of our capacitor network and increased jitter in some of the FPGA components.

To quantify the improvement in performance, the sine waves are converted to the frequency domain, as shown in Fig. 10. Clearly, the stabilizer brings significant improvement, especially at cryogenic temperatures.

In summary, the main specifications for our ADC are listed in Table II for the use-cases described before. At 300 K, the stabilizer doesn’t bring significant improvements. The ENOB is improved by 0.4 bit at low frequencies, but at higher frequencies, there is only a minor improvement of 0.1 bit (which is in the error-margin). At cryogenic temperatures however, the improvement is
more significant. For low frequencies, there is a 1.5 bit better ENOB and at high frequencies, the ENOB still improves with 1.2 bit. These results clearly show that the ADC operation at cryogenic temperatures is challenging, especially when not considering power fluctuations and the significant effect of IR drop on the FPGA behaviour. There are still many unknown effects of electronics, materials and the corresponding behaviours while operating at temperatures so far out of the normal industrial temperature range, thus prompting more research in many aspects of cryogenic FPGA design.

V. CONCLUSION

We have demonstrated an approach to circumvent the ineffectiveness of voltage regulators at deep-cryogenic temperatures by regulating the FPGA power consumption internally. This has been done by constantly measuring the cell delay and acting upon change by decreasing or increasing the amount of running oscillators in a small oscillator farm.

The stabilization of the power consumption has been demonstrated and has been quantified by showing significant improvement of the performance of our FPGA ADC system while stabilizing its power consumption and thus its supply voltage. The ENOB of our ADC was at most 1.5 bits higher while using the stabilizer.

Besides the implementation of the FPGA power regulation, a study was conducted on the behaviour of various components needed in the power distribution network at cryogenic temperatures. The best behaving capacitors are those based on low dielectric constant materials, such as NP0/COG, while those with high dielectric constants tend to drop over 90% in capacitance and increase the ESR with over 3000%. Commercial voltage regulators were not found to be working at 4 K, but cease operation around 90 K.

This study shows the complexity of operating at cryogenic temperatures, especially in terms of power supply over long wires, the unavailability of cryogenic regulators and the degraded performance of the decoupling network. Despite these complications, performance of the FPGA system can be significantly improved while regulating its supply voltage from within itself.

1D. Sheldon, G. Burke, A. Argaeta, A. Bakshi, N. Aranki, and M. Sadiqursky. (2011).
2D. Gong, S. Hou, C. Liu, T. Liu, D.-s. Su, P.-k. Teng, A. C. Xiang, and J. Ye, Phys. Procedia 37, 1654 (2012).
3A. Bakhshi, Xcell J. 80, 24 (2012).
4J. M. Hornibrook, J. I. Colless, I. D. Conway Lamb, S. J. Paula, H. Lu, A. C. Gossard, J. D. Watson, G. C. Gardner, S. Fallahi, M. J. Manfra, and D. J. Reilly, Phys. Rev. Appl. 3, 024010 (2015).
5I. D. Conway Lamb, J. I. Colless, J. M. Hornibrook, S. J. Paula, S. J. Waddy, M. K. Frechtling, and D. J. Reilly, Rev. Sci. Instrum. 87, 014701 (2016).
6H. Homulle, S. Visser, B. Patra, G. Ferrari, E. Prati, F. Sebastiani, and E. Charbon, Rev. Sci. Instrum. 88, 045103 (2017).
7R. L. Patterson, A. Hammond, and S. S. Gerber, in IEEE Symposium on Electrical Insulation, Vol. 2 (IEEE, 1998) pp. 468–471.
8A. Teverovsky, “Performance and reliability of solid tantalum capacitors at cryogenic conditions,” (2006).
9P. C. van Niekerk and C. J. Fourie, in AFRICON 2007 (2007) pp. 1–7.
10F. Teyssandier and D. Prêle, in WOLTE11 (2014).
11R. Patterson and A. Hammond, “Performance of a 3.3V SOI voltage regulator under extreme temperatures,” (2006).
12W. A. Basit, S. El-Ghanam, A. A. El-Maksood, and F. Soliman, Phys. Sci. Res. International 1, 15 (2013).
13S. El-Ghanam and W. A. Basit, Cryogenics 51, 117 (2011).
14L. Song, H. Homulle, E. Charbon, and F. Sebastiani, in IEEE Sensors (IEEE, 2016) pp. 1–3.
15W. He, M. Stottinger, E. de la Torre, and V. Diaz, in DCIS (2015) pp. 1–6.
16T. Zednicek, M. Barta, J. Petrazilk, and M. Biler, in 1st Space Passive Component Days (AVX, 2013).
17H. Homulle, S. Visser, and E. Charbon, IEEE Trans. Circuits Syst. I, Reg. Papers 63, 1854 (2016).
18A. Bakhshi, Xcell J. 80, 24 (2012).
38.5 14.1 24.7 32.2
30.8 31.6 22.9 28.8
36.8 38.9 21.3 30.3
28.6 29.3 19.4 26.5
51.4 -57.5 -31.0 -49.6
-36.7 -37.5 -27.1 -35.7
5.8 6.2 3.2 4.7
4.5 4.6 2.9 4.1

TABLE II. Summary of the obtained ADC specifications while converting a 2 and 40 MHz sine at 1.2 GSa/s with the stabilizer turned on or off. The stabilizer improves the performance, especially at cryogenic temperatures, with up to 1.5 bit in terms of ENOB or roughly 9 dB SNDR.

| freq.[MHz] | 2 | 40 |
| Temperature | 300 K | 15 K | 300 K | 15 K |
| Stabilizer | Off | On | Off | On |
| SNR [dB] | 38.5 | 14.1 | 24.7 | 32.2 |
| SNDR [dB] | 36.8 | 38.9 | 21.3 | 30.3 |
| SFDR [dB] | 51.4 | -57.5 | -31.0 | -49.6 |
| ENOB [bits] | 5.8 | 6.2 | 3.2 | 4.7 |
Appendix A: Passives - Detailed results

In Fig. 11 a detailed overview of the capacitance and ESR of various capacitors is given, the standard capacitors are the ones listed before in Table I. While the special capacitors are EPPL2 and sealed caps from AVX for tantalum and silicon type for the 1 $\mu$F (also available in other values). While the special tantalum capacitors perform worse compared to standard tantalum in all cases at 4 K, they (especially the sealed caps) perform indeed better down to 80-100 K temperatures.

In Fig. 12, the measured resistance for the three resistors shown in Fig. 2 are plotted with different testing frequencies.

Appendix B: Voltage regulators - Detailed results

Below all results of voltage regulators over temperature can be found. In Fig. 13 and Fig. 14, the output voltage of switching (buck) regulators, respectively LDOs are plotted versus temperature. For reference, a margin of 2.5% from the average output voltage at room temperature is used to indicate the regulator being too far away from what voltage should be seen over the load resistance ($R_{load} = 100 \, \Omega$). This boundary is indicated with the best temperature at which the device is still in this margin.

In Fig. 15 and Fig. 16, the power consumption of the same set of regulators is shown versus temperature. Clearly, in general the switching supplies consume less power as expected compared to the LDOs. A major exception is the switching regulator ISL80030 (Fig. 15(a)) from Instersil which consumes about 1 W, which is extremely high.
FIG. 11. Detailed study of various capacitor types and values over a wide temperature range from 4 K to 300 K, showing both its capacitance and ESR.
FIG. 11 (Cont.). Detailed study of various capacitor types and values over a wide temperature range from 4 K to 300 K, showing both its capacitance and ESR.
FIG. 12. Resistance of different resistors, value and resistive material type (metal and thick film) over temperature.

FIG. 13. Detailed stability study of switching (buck) regulators over a wide temperature range from 4 K to 300 K.
FIG. 14. Detailed stability study of LDOs over a wide temperature range from 4 K to 300 K.
FIG. 15. Power consumption of the voltage regulators shown in Fig. 13.
FIG. 16. Power consumption of the voltage regulators shown in Fig. 14.