Reflective Parametric Frequency Selective Limiters with sub-dB Loss and $\mu$Watts Power Thresholds

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Abstract—This article describes the design methodology to achieve reflective diode-based parametric frequency selective limiters ($p$FSLs) with low power thresholds ($P_{th}$) and sub-dB insertion-loss values ($IL^{ss}$) for driving power levels ($P_{in}$) lower than $P_{th}$. In addition, we present the measured performance of a reflective $p$FSL designed through the discussed methodology and assembled on a FR-4 printed circuit board (PCB). Thanks to its optimally engineered dynamics, the built $p$FSL can operate around $\sim2.1$ GHz while exhibiting record-low $P_{th}$ (-3.4 dBm) and $IL^{ss}$ (0.94 dB) values. Furthermore, while the $p$FSL can selectively attenuate undesired signals with power ranging from -3.4 dBm to 13 dBm, it provides a strong suppression level ($IS > 80$) with low power thresholds ($P_{in}$ values approaching 28 dBm. Such measured performance metrics demonstrate how the unique nonlinear dynamics of parametric-based FSLs can be leveraged through components and systems compatible with conventional chip-scale manufacturing processes in order to increase the resilience to electromagnetic interference (EMI), even of wireless radios designed for a low-power consumption and consequently characterized by a narrow dynamic range.

Index Terms—Parametric Components, Frequency Selective Limiters (FSLs), Auxiliary Generators, Nonlinear Dynamics, Interference Suppression

I. INTRODUCTION

The growing Internet of Things (IoT) is challenging the sharing of the available spectrum by an increasing number of wireless devices that interfere with each other. As a result, the performance of the existing radios keep being affected more and more heavily by strong electromagnetic interference (EMI) lowering the capability to receive the useful information and threatening the integrity of any receivers (RXs), especially when designed for a low-power consumption. For this reason, adaptive RXs with interference filtering capabilities have received growing attention in recent research efforts. In particular, radio frequency (RF) power-sensitive components known as Frequency Selective Limiters (FSLs [1]) have recently been researched to provide low-power RXs with the unique ability to instinctually suppress received EMI without affecting the capability to simultaneously receive the desired lower-power useful information. Thanks to their power-sensitive electrical response, FSLs can address key operational needs, such as a higher resilience to EMI in modern radars or the protection of any critical communication systems from high-power microwave attacks or jamming. Two main classes of FSLs have been previously discussed. One class relies on ferrite-based components [2]–[12], exploiting different types of nonlinear mechanisms in thin-film magnetic materials. While ferrite-based FSLs employing different technologies have been explored, the intrinsic losses associated with any usable thin-film magnetic materials render these FSLs prone to high insertion-loss values for small signals ($IL^{ss}$ up to 10 dB). In addition, since the magnetic materials used by ferrite-based components cannot be manufactured through fabrication processes compatible to the ones used for Complementary-Metal-Oxide-Semiconductor (CMOS) Integrated Circuits (ICs), ferrite-based FSLs cannot be monolithically integrated with the other active and passive components forming the receive and transmit modules of commercial radios.

Alternatively, diode-based FSLs [13]–[19] have been investigated. Such components rely on the electrostatic nonlinearities of solid-state devices and systems to achieve compact FSLs that can be integrated with the other components of commercial and military RF chains to ensure the highest degree of miniaturization. Yet, the fully-passive diode-based FSLs reported to date exhibit much higher power thresholds than those attained by the state-of-the-art (SoA) ferrite-based counterparts [9], thus not being adequate to protect the majority of the integrated front-ends used by IoT systems. Just recently, a diode-based FSL relying on an active feedback-loop, using a board-level power detection and an electromechanically tunable cavity resonator has been reported [20]. Yet, due to the required intense operations allowing to reconfigure its transmission characteristics and regardless of its exceptionally low threshold granted by the use of a sensitive power detector, this reported FSL is not ideal when miniaturized radios with a low-power consumption are needed.

Driven by the need of developing a new class of passive open-loop phase noise cleaners, known as parametric filters [21], [22], our group has recently investigated the stability of large-signal periodic regimes in diode-based 2:1 parametric frequency dividers (PFDs [23]), even describing a new design methodology to achieve exceptionally low parametric power thresholds ($P_{th}$) attained by the state-of-the-art (SoA) ferrite-based counterparts [9], therefore not being adequate to protect the majority of the integrated front-ends used by IoT systems. Just recently, a diode-based FSL relying on an active feedback-loop, using a board-level power detection and an electromechanically tunable cavity resonator has been reported [20]. Yet, due to the required intense operations allowing to reconfigure its transmission characteristics and regardless of its exceptionally low threshold granted by the use of a sensitive power detector, this reported FSL is not ideal when miniaturized radios with a low-power consumption are needed.

By further exploiting the outcomes of this investigation, we recently developed a new battery-less, chip-less and harvester-free sensor tag [24], referred to as subharmonic tag (SubHT), utilizing a 860 MHz diode-based parametric circuit made of lumped off-the-shelf components assembled on a printed substrate. Through the SubHT, we demonstrated that the proper engineering of the dynamics of diode-based parametric circuits permits to achieve extraordinarily low $P_{th}$ values (~18 dBm for an input frequency of 860 MHz) approaching the power threshold attainable by SoA ferrite-based FSLs, even when relying on low quality factor (<80) components and on packaged diodes with junction capacitance in the $pF$-range. Furthermore, the demonstration of the SubHT
allowed us to unveil a unique dynamical characteristic for parametric circuits. Such circuits, in fact, can exhibit a much lower conversion loss (CL) from an ultra-low power (\(\leq 1\)mW) input signal to a sub-harmonic output signal than the minimum CL obtained by any frequency doubling counterparts relying on the same nonlinear reactance and on the same circuit topology. This powerful feature has been leveraged in this work to achieve a tunable diode-based parametric FSL (pFSL) that can exhibit record-low \(P_{th} \approx 3.4\) dBm for an input frequency close to 2.1 GHz and \(IL^{s-s}\) (as low as 0.94 dB) values, along with a significant interference suppression (IS) reaching 5.4 dB for driving power levels \(P_i\) lower than 13 dBm, even exceeding 12.0 dB for \(P_i > 28\) dBm. In the next sections, we will first present the main design criteria and trade-offs to consider in order to achieve pFSLs with low \(P_{th}\) and low \(IL^{s-s}\). Later, we will discuss the perturbation-based circuit simulation approach that can be followed to predict and optimize the IS value achieved by pFSLs directly from the steady-state circuit simulated electrical response. Finally, we will showcase the measured performance of a \(~2.1\) GHz diode-based pFSL that we designed and built on a FR-4 printed-circuit-board (PCB) in this work.

II. REFLECTIVE pFSLs – DESIGN METHODOLOGY

A pFSL is a nonlinear circuit able to instinctually suppress the power flow between its ports when driven by strong RF signals with power \(P_i\) exceeding a certain threshold (i.e., \(P_{th}\)). In order to do so, pFSLs rely on the nonlinear dynamics of diode-based parametric circuits to trigger a period-doubling mechanism leading to abrupt changes in the pFSLs’ electrical responses for \(P_i\) values exceeding \(P_{th}\). For low-power RF front-ends in particular, pFSLs are well-suited to enhance resilience to interference, especially when combined with circuit-level linearity improvement methods such as those discussed in [25]–[27]. Two main types of pFSLs can be designed, namely the absorptive and the reflective pFSLs. Absorptive pFSLs rely on directional couplers with output and coupled ports terminated on two parametric networks including one or more diodes. The reliance on such a circuit topology renders absorptive pFSLs capable to absorb strong RF signals with power exceeding their \(P_{th}\) value. Yet, absorptive pFSLs are characterized by significant IS values only within a narrow range of input power levels centered around an optimal value \(P_{opt}\) that dynamically minimizes the return-loss (RL) at the input of their parametric networks. Consequently, absorptive pFSLs exhibit just negligible IS levels for \(P_i\) largely exceeding \(P_{opt}\). Hence, they are challenging to use in the presence of continuously varying interference power levels, such as the ones frequently captured by mobile radios in practical electromagnetic scenarios, since they leave cascaded components exposed to severe risks of being damaged by EMI with power higher than \(P_{opt}\). On the contrary, reflective pFSLs exploit the dynamics of diode-based passive circuits to trigger sudden and large increases of RL (at both the pFSLs’ input and output ports) in presence of \(P_i\) values exceeding their \(P_{th}\). Reflective pFSLs also exhibit the highest frequency selectivity around an optimal \(P_{opt}\) value, which depends on the maximum voltage that can be applied across the diode before triggering any periodic transitions between the diode’s reverse and forward conduction. Nevertheless, due to their design characteristics, reflective pFSLs can exhibit a high IS even in presence of much stronger interference signals, thus lowering the chances that any receivers can be damaged by EMI of extraordinary high power. However, up to date, a consolidated and systematic design flow for reflective pFSLs is still missing. Such a lack of information, along with the complexity of adapting the ad-hoc simulation techniques developed for parametric circuits to the algorithms used by commercial circuit simulators [28]–[32], has inhibited the design of reflective pFSLs simultaneously achieving low \(P_{th}\) and \(IL^{s-s}\) values.

In the most simplistic representation, a reflective pFSL can be seen as a two-port passive network including one diode characterized by a biased capacitance \(C_v\) and a corresponding tuning range \(\delta\) (see Fig. 1), together with a set of components forming a stabilization network for the large signal periodic regimes excited in the circuit by \(P_i\). Without any loss of generality, we can assume any reflective pFSL to be representable through a T-network topology including the adopted diode, three one-port complex impedances \((Z_a, Z_b\text{ and } Z_c)\) and a quarter-wave transformer (labeled as \([Z_T]\)) with bandwidth centered around the value \((f_{in}^{opt})\) of the input frequency \(f_{in}\) corresponding to a natural frequency labeled as \(\omega_{in}\) at which the minimum \(P_{th}\) is desired. While the transformation stage can be implemented through any existing lumped or distributed circuit topologies, a third-order lumped implementation is assumed here in favor of a simpler analytical treatment. Also, such a two-port network, uniquely identified by an inductance \(L_T\) and a capacitance \(C_T\) setting the equivalent characteristic impedance \((Z_{tx} = \sqrt{(L_T/C_T)})\), plays a key role to simultaneously achieve the lowest possible \(P_{th}\) and \(IL^{s-s}\) values in pFSLs, as it will be clear in the following section. Furthermore, to match the most frequent
operational scenario, the same termination (Z₀, equal to 50 Ω) can be considered for the input and output ports. As the P₁th exhibited by pFSLs needs to be as low as possible to ensure that even low power RXs characterized by a small dynamic range can be protected from EMI, it is crucial to find the optimal design specifications for [Zₜ], Zₐ, Zₖ and Zₑ (from now on labeled together as Zₑ₁a,b,c) allowing to minimize the achievable P₁th. By relying on the same analytical methodology used to find the P₁th of PFDS in our recent theoretical investigation [23], the P₁th of the reflective pFSL shown in Fig. 1 can be found as:

$$P_{₁th} = \frac{|V_{₁th}|^2}{8Z₀} = \frac{C_v^4}{2Z₀d^2} \left( \frac{G_{eq}(\omega_{₁eq})G_{eq}(\omega_{₁opt})}{\left(\frac{Z₁(\omega₁)}{Z₁(\omega₂)} + \frac{Z₂(\omega₁)}{Z₂(\omega₂)}\right)\left(\frac{Z₃(\omega₁)}{Z₃(\omega₂)}\right)} \right)^2 \quad (1)$$

In (1), V₁th is the voltage level of the input generator with characteristic impedance equal to Z₀ and power available equal to P₁th. Also, Z₁, Z₂ and Z₃ represent the equivalent impedances seen at the half of the driving frequency (f₀, equal to f₁th/2 and corresponding to a natural frequency labeled as ω₁) from node N₁ (see Fig. 1) towards Zₐ and Zₖ respectively, whereas Z₃eq is the equivalent impedance at f₁th seen from N₁ towards Zₖ. Further, Geq(ω₁) and G₁eq [see (2) and (3)] are complex functions of Z₁(ω₁), Z₂(ω₁), Z₃(ω₁) and of the impedances Z₁(ω₂), Z₂(ω₂) and Z₃(ω₂), where Z₁(ω₁), Z₂(ω₁) and Z₃(ω₁) are the impedances seen at f₁th and f₀ from N₁ towards Zₐ, Zₖ and Zₑ.

$$G_{eq}(\omega₃) = Z₂(\omega₃)Z₃(\omega₃) + Z₁(\omega₃)(Z₂(\omega₃) + Z₃(\omega₃)) \quad (2)$$

$$G_{eq}(\omega₃) = Z₂(\omega₃)Z₃(\omega₃) + Z₁(\omega₃)(Z₂(\omega₃) + Z₃(\omega₃)) \quad (3)$$

By replacing (2) and (3) in (1), it is straightforward to notice that the resulting P₁th expression is a function of all the impedances in the circuit (i.e., Zₑ₁a,b,c, Z₀ and the diode impedance) and of the first two coefficients of the linearized capacitance vs. voltage characteristic of the biassed diode (see Fig. 1). Moreover, since all the impedances in (1), (2) and (3) can be extracted through linear algorithms in any circuit simulator, their synthesis can be numerically tackled aiming at the minimization of P₁th without running time consuming nonlinear perturbation-based simulations, such as the ones available to investigate the steady-state large-signal operation of parametric circuits. Nevertheless, similarly to what we showed for PFDS in [23], the inspection of (1) after simplifying Geq(ω₁eq) and G₁eq with their corresponding expressions in (2) and (3) permits to realize that the minimum P₁th at fopt can be attained by ensuring that four resonant conditions are satisfied: i) Z₁(ω₁) + Z₃(ω₁) must be in series resonance at fopt with the lowest real part possible (Rₚ); ii) Z₂(ω₂) + Z₃(ω₂) must be in series resonance at f₁th/2 with the lowest real part possible (Rₖ); iii) Z₁(ω₁) must be in parallel resonance at f₁th with the highest real part possible; iv) Z₁(ω₁) must be in parallel resonance at f₁th/2 with the highest real part possible. In order to satisfy these resonance conditions through the use of a minimum number of lumped components, both Zₐ and Zₖ can be synthesized with parallel LC resonators, resonating at f₁th/2 and f₁th respectively and relying on inductors (capacitors) with inductance (capacitance) Lₑ (Cₑ) and Lₖ (Cₑ) respectively. Furthermore, Zₑ can be synthesized with one inductor whose inductance (Lₑ) is strategically selected to ensure the simultaneous validity of the first two resonant conditions, given the selected Lₑ and Lₖ values. Thus, when the resonant conditions mentioned above are satisfied, (1) can be simplified as:

$$P_{₁th} = \frac{C_v^4}{2Z₀d^2} \left( R_p Rₚ ω_{₁opt}^2 \right)^2 \quad (4)$$

where ω₁opt is equal to 2πf₁th and Rₚ can be expressed in terms of Zₑ [see (5)] when assuming for simplicity [Zₜ] to be lossless.

$$R_p = R_s + \frac{2Z_{₁th}}{Z₀} \quad (5)$$

In (5), Rₛ captures the ohmic losses of both Zₐ and Zₑ along with the ones of the diode. Also, in the derivation of (4) we neglected the impact of Z₈(ω₁) in favor of a simplified analytical treatment and an easier visualization of the main features determining P₁th in reflective pFSLs. The validity of this approximation is granted by the fact that these two impedances, which are synthesized by two notches, just allow to isolate the signals at f₁th/2 and f₁th in dedicated meshes of the circuit. From (4) and (5) it is evident how the transformation stage plays a key role in lowering Rₚ with respect to the value it would have (i.e., Rₛ+Z₀/2) if the resonant conditions were satisfied without using such a transformation stage. Therefore, the adoption of [Zₜ] introduces fundamental means to reduce the lowest P₁th that can be attained by reflective pFSLs. It is useful to simplify (4) by expressing Rₛ and Rₖ in terms of the quality factor of the diode (Qᵥ, related to an f₁th value equal to fopt) and the ones (Q₁ and Q₂) respectively exhibited at f₁th and f₂th by Z₁(ω₁)+Z₃(ω₁) and Z₂(ω₂)+Z₃(ω₂). Also, for pFSLs operating in the Ultra-High-Frequency (UHF) range, like the prototype demonstrated in this work, we can assume Q₁ to be equal to Q₂ (i.e., Q₁=Q₂, being Qᵥ dependent on the technology of the adopted passive components) and to be significantly higher than Qᵥ. This simplification is particularly valid when relying on diodes with wide tuning ranges, such as any available hyperabrupt varactors [33]. Consequently, Rₛ can be considered equal to Rₖ and can be simplified as follows:

$$R_s = R_k = \frac{1}{ω_{₁opt} C_v (\frac{1}{Q₁} + \frac{1}{Qᵥ})} \approx \frac{1}{ω_{₁opt} C_v Qᵥ} \quad (6)$$

By using (6) in (4), P₁th can then be rewritten as:

$$P_{₁th} = \frac{(Z₀ + 2C_vQᵥZ_{₁th}^2ω²_{₁opt})}{2Q₀ Z₀^3δ²} \quad (7)$$

Equation (7) gives us the opportunity to estimate the minimum P₁th value that can be attained by reflective pFSLs for any given fopt of interest and for a chosen diode’s characteristics. As an example, we report a contour-plot capturing P₁th vs. Zₑ and Cₑ in [7] in Fig. 2a, which was analytically derived when assuming: i) the use of an hyperabrupt varactor (i.e., δ ~ 0.4 and Qᵥ ~ 15) with Cₑ ranging from 50 fF to 5 pF,
and ii) an $f_{in}^{opt}$ of 2.1 GHz (in line with our experimental demonstration).

As evident from Fig. 2a, reflective PFSLs can achieve low $P_{th}$ values ($<0$ dBm) through the strategic adoption of diodes with wide tuning range and low capacitance, along with $\lambda/4$ transformation stages characterized by the minimum realizable characteristic impedance. Nevertheless, since PFSLs also need to exhibit the lowest possible insertion loss for power levels that are lower than $P_{th}$, the selection of $Z_{in}$ must also be made to ensure a minimum $IL^{s,s}$. In order to estimate the $IL^{s,s}$ value of the PFSL shown in Fig. 1, we can extract the small-signal scattering parameter ($S_{21}$) for the transmission at $f_{in}^{opt}$ from the PFSL’s input port to the PFSL’s output port, after linearizing the capacitance vs. voltage characteristic of the diode around $V_{DC}$. The expression of $IL^{s,s}$ in dB is provided in (8).

$$IL^{s,s} = -20\log_{10}(S_{21}) = -20\log_{10}\left|\frac{Z_{in}(\omega_{in, opt})}{Z_{in}(\omega_{in, opt}) + Z_{s}}\right|$$ \hspace{1cm} (8)

In (8), $Z_{in}(\omega_{in, opt})$ is the impedance seen at $f_{in}^{opt}$ from the circuit node $N_2$ (see Fig. 1) towards $N_1$ and its value is almost independent of $P_{in}$ for $P_{in}<P_{th}$. Upon validity of the same resonance conditions that minimize $P_{th}$ and $Z_{in}(\omega_{in, opt})$, it can be found that:

$$Z_{in}(\omega_{in, opt}) = \frac{Z_{tx}}{R_s}$$ \hspace{1cm} (9)

Equation (9) allows to simplify $IL^{s,s}$ [(8)] as follows:

$$IL^{s,s} = -20\log_{10}\left|\frac{2Z_{tx}^2}{R_sZ_0 + 2Z_{tx}^2}\right|$$ \hspace{1cm} (10)

By replacing (6) in (10), $IL^{s,s}$ can be finally rewritten as shown in (11).

$$IL^{s,s} = -20\log_{10}\left|1 - \frac{Z_0}{Z_0 + 2C_vQ_vZ_{tx}^2\omega_{in, opt}}\right|$$ \hspace{1cm} (11)

Equation (11) enables us to assess the minimum $IL^{s,s}$ value that can be attained by reflective PFSLs, given a selected $f_{in}^{opt}$ value and based on the DC-biased capacitance of the selected diode. As an example, a contour-plot capturing $IL^{s,s}$ vs. $Z_{tx}$ and $C_v$ is displayed in Fig. 2b, which was derived analytically while assuming the same $\delta$ and $f_{opt}$ and $Z_0$ values used during the derivation of Fig. 2a. By comparing (11) with (7) and Fig. 2a with Fig. 2b, an important design trade-off between the desired $P_{th}$ and $IL^{s,s}$ values can be identified. While relying on high-$Z_{tx}$ values allows to reduce $IL^{s,s}$, it also determines an increase of $P_{th}$ that can be unacceptable unless $C_v$ values in the $fF$-range were used. Since any board-level PFSLs, such as the one we designed and built in this work, can only leverage $C_v$ values close to 1 pF or higher, there exists a fundamental limit for the minimum $P_{th}$ that can be obtained while preserving a low $IL^{s,s}$. Furthermore, $Z_{tx}$ cannot be made arbitrarily large without rendering $[Z_T]$ severely affected by electrical loading, thus also degrading $IL^{s,s}$. This inevitably restrains the pool of usable diodes as it limits the maximum acceptable $R_s$ and consequently the minimum $Q_v$ based on the maximum $IL^{s,s}$ that can be tolerated. Therefore, the strategic selection of the diode and of the other components forming $Z_0$ and $Z_c$ is critical to make sure that the lowest $IL^{s,s}$ can be attained without requiring a large $Z_{tx}$ that would compromise the achievable $P_{th}$-value. Moreover, Fig. 2 provides useful means to assess the performance that would be achieved if PFSLs were designed and built directly on-chip through any available CMOS technologies. In such a scenario, thanks to
the availability of both capacitors and diodes with capacitance in the $fF$-range, any integrated reflective pFSLs would be able to simultaneously rely on extraordinarily low $C_v$ and high $Z_{tx}$ values ($>1\,k\Omega$), thus enabling much lower $P_{th}$ values ($<-20\,\text{dBm}$) than possible with board-level counterparts given a targeted $IL^{*,s}$ value.

A. Evaluation of the maximum $P_{in}$ value for a preserved frequency selectivity

While the achievement of low $P_{th}$ and $IL^{*,s}$ values is certainly crucial, another metric to consider during the design of any pFSLs is the maximum $P_{in}$ value ($P_{in}^{\max} = \sqrt{8Z_0V_{max}^2}$, where $V_{max}$ is the corresponding peak voltage at $f_{opt}^r$) at which a frequency selective attenuation at $f_{opt}^r$ is preserved. In particular, with regards to reflective pFSLs, the existence of a finite $P_{in}^{\max}$ is due to periodic transitions from reverse to forward conduction that any diodes undergo when the voltage across their terminals exceeds the sum of the diode’s DC bias and built-in ($V_{bi}$) voltages. Due to these transitions, the diode’s resistance ($R_v$) undergoes a sudden increase as $P_{in}$ is made larger than $P_{in}^{\max}$, leading to a progressive reduction of the parametrically generated negative resistance at $f_d$ responsible for the rising of the sub-harmonic oscillation in the circuit and, consequently, to a degradation of the pFSL performance at $f_{opt}^r$. As a first-order of approximation, $P_{in}^{\max}$ can be found through a straightforward analysis of the circuit shown in Fig. 1 based on transmission matrices [see (12)] when assuming that $Z_a$, $Z_b$, and $Z_c$ satisfy the resonant conditions minimizing $P_{th}$ and when neglecting (for simplicity) any quadratic or cubic nonlinearities of the diode.

$$P_{in}^{\max} \approx \left( V_{DC} + V_{th} \right) ^2 \left( 2C_vQ_{s.s}Z_{tx}^2 + Z_0 \right) ^2 \left( Q_i \right) ^2 Z_0 Z_{tx}^2$$  \hspace{1cm} (12)

Equation (12) aids the selection of the diode by identifying the minimum $V_{DC}$ allowing to preserve a frequency selective limiting behavior for $P_{in}$ values ranging from $P_{th}$ to any desired $P_{in}^{\max}$ value, given any targeted $C_v$ and $Z_{tx}$ values. As an example, Fig. 3 shows a contour-plot capturing the analytically derived $P_{in}^{\max}$ vs. $Z_{tx}$ and $V_{DC}$ [see (12)], assuming the same $\delta$, $f_{in}$ and $Z_0$ values used during the derivation of Fig. 2, a $V_{th}$ arbitrary set to 0.7 V (i.e., the built-in voltage for silicon diodes) and a $C_v$ value of 2.0 pF [i.e., the same used in our experimental demonstration when considering the additional parasitic capacitance (~0.4 pF) associated to the diode’s package]. As evident from both (12) and Fig. 3, $P_{in}^{\max}$ values lower than 0 dBm and fairly insensitive to $Z_{tx}$ are obtained with low capacitance diodes requiring the use of low $V_{DC}$ values to operate. Nevertheless, significantly higher $P_{in}^{\max}$ values can still be achieved by selecting larger diodes biased with higher DC voltages. By comparing (12) with (7), it can be noticed that $V_{DC}$ represents the most important design parameter to ensure that high $P_{in}^{\max}$ and low $P_{th}$ values can be achieved simultaneously. Furthermore, contrary to any reported absorptive counterparts, reflective pFSLs are able to protect the integrity of any cascaded electronic components even for $P_{in} > P_{in}^{\max}$. Yet, within such high-power operative scenario, reflective pFSLs progressively lose their frequency selectivity as $P_{in}$ is increased, thus ultimately showing strong attenuations across significant portions of their original bandwidth.

![Graph showing $P_{max}$ value vs $Z_{tx}$ and $V_{DC}$ for the reflective pFSL](image)

Fig. 3: $P_{max}$ value (in dBm) vs. $Z_{tx}$ and $V_{DC}$ for the reflective pFSL in Fig. 1, computed through (12) after assuming $Z_0 = 50\,\Omega$, $f_{opt}^r=2.1\,\text{GHz}$, $Q_i=15$, $V_{th}=0.7\,\text{V}$, $C_v=2.0\,\text{pF}$ and upon validity of the resonance conditions minimizing $P_{th}$.

III. DESIGNING pFSLs IN COMMERCIAL CIRCUIT SIMULATORS

In the previous section, it has been shown how the achievement of the minimum $P_{th}$ and $IL^{*,s}$ values in reflective pFSLs can be ensured for any input frequencies of interest by satisfying four resonant conditions and by minimizing $IL^{*,s}$ [see (11)]. Therefore, regardless of the nonlinear characteristics exhibited by pFSLs, the synthesis of the passive impedances [i.e., $\{Z_1, Z_2, Z_3, Z_4\}$ (see Fig. 1)] forming any board-level reflective pFSLs can be accomplished through linear simulation and optimization techniques, after selecting an available diode with the lowest possible $C_v$ and the highest possible $Q_v$, given the minimum tolerated $P_{in}^{\max}$ value. It is worth pointing out that the capability to synthesize the different components of pFSLs through linear methods enables the reliance on conventional algorithms during the optimization of both the pFSLs’ circuit and layout. Consequently, the optimal design conditions for any pFSLs, including those operating at high frequency and consequently more impacted by layout parasitics, can be identified more reliably and more easily than what is possible when only relying on perturbation-based techniques. Nevertheless, such techniques are still required to assess the behavior of pFSLs for $P_{in} > P_{th}$, thus in the operative regime where the evolution of the circuit parameters strongly depends on the nonlinearities of the diode. Among the existing perturbation-based techniques, the power auxiliary generator (pAG [28]) technique provides unique means to extract the steady-state response of any parametric circuits without having to numerically enforce the validity of the non-perturbation condition [34] due to the adoption of an auxiliary generator in the circuit.
A pAG consists of a continuous-wave (CW) voltage generator operating at \( f_d \) and delivering a small non-perturbative power through a generator impedance \( (Z_G) \). When a pAG is used to simulate the response of a pFSL through a commercial Harmonic Balance (HB) circuit simulator, the pFSL’s output termination (i.e., \( Z_0 \) in the circuit in Fig. 1) must be replaced by a pAG with \( Z_G \) also equal to \( Z_0 \). This allows to insert \( f_d \) in the vector of frequencies that HB processors use to evaluate the response of driven RF circuits. In addition, by ensuring that \( Z_G \) matches \( Z_0 \), the adoption of the pAG does not cause variations of the impedance seen by the diode at \( f_d \) or at multiples of \( f_d \), thus preventing any undesired changes in the dynamics of the circuit which would lead to unreliable predictions of the circuit’s response. The extraction of the steady-state response of pFSLs can be achieved by sweeping \( P_{in} \) from a much lower power than \( P_{th} \) up to the maximum power level of interest, while configuring the values of the computed current and voltage phasors for any evaluated power level as initial conditions for the same circuit parameters prior to the computation of the following data point to assess. Through this ad-hoc sweeping strategy, it is possible to extract IS by evaluating the trend of the pFSLs’ insertion-loss for power levels exceeding \( P_{th} \). This also provides the means to fine-tune some of the component values synthesized in the earlier design stage towards the achievement of the highest IS value. In order to do so, it is convenient to look at \( Z_{in} \) (see Fig. 1) while varying some strategically selected circuit components to let the magnitude of this impedance be as small as possible for \( P_{in} > P_{th} \). During this design phase, the components synthesizing \( Z_0 \) are the most adequate to be fine-tuned as they do not affect \( IL^{s,a} \) while only slightly altering \( P_{th} \). It is also important to point out that the ability to accurately predict IS in any pFSLs is heavily influenced by the reliability of the available nonlinear circuit model for the adopted diode.

\[ \begin{align*}
\text{IV. Experimental Results} \\
\text{In order to demonstrate the capability of reflective pFSLs to simultaneously exhibit low } IL^{s,a} \text{, low } P_{th} \text{ and high IS values, we designed a FR-4 Printed Circuit Board (PCB) implementation of a } \sim 2.1 \text{ GHz reflective pFSL (i.e., } f_{in}^{opt} \sim 2.1 \text{ GHz) using a commercial off-the-shelf hyperabrupt varactor (Skyworks SMV1231) as a diode. The assembled pFSL relies on a hybrid implementation of the circuit topology shown in Fig. 1, including a set of lumped components strategically selected together with the optimal geometrical layout characteristics (i.e., the length and width of all interconnecting lines, the shape and footprint of the selected surface-mount connectors, and the radius of each circular via). This allows to achieve a small form factor (2.2 } \text{ cm}^2 \text{ of board area) and the lowest possible } P_{th} \text{ given an } IL^{s,a} \text{ lower than a maximum tolerated value (here set to 1 dB). In particular, } Z_0 \text{ and } Z_{in} \text{ were synthesized through two LC parallel resonators with inductors } L_a \text{ and } L_b, \text{ and capacitors } C_a \text{ and } C_b; \text{ whereas } Z_c \text{ was synthesized through an inductor (} L_c \text{) in series with the selected varactor. Also, a DC-blocking capacitor (} C_{blk} = 12 \text{ pF} \text{) was introduced in series with } L_b \text{ to permit the DC-biasing of the selected diode through a Bias-Tee (Inmet 8800SMF3-06) at the input port, even allowing an analog reconfigurability of } P_{th} \text{ and } f_{in}^{opt}, \text{ as discussed later. The transformation stage at } f_{in}^{opt} \text{ was designed to exhibit a } Z_{tx} \text{ value close to 31 } \Omega \text{ when relying on two lumped capacitors (} C_{tx} \text{ and } C_{in} \text{) and two distributed inductors made of short lines. Such a } Z_{tx} \text{ value was chosen to ensure } P_{th} \text{ and } IL^{s,a} \text{ values lower than } -3 \text{ dBm and 1 dB respectively (see Fig. 2) based on the } C_v (2.0 \text{ pF}) \text{ and } Q_v (\approx 15) \text{ values exhibited by the varactor when } V_{DC} \text{ is set to 1.1 V. Also, the adoption of distributed components in the transformation stage represents the most convenient design solution to ensure that the performance is not degraded by the capacitive coupling.}
\end{align*} \]
between the connectors’ footprint and the rest of the circuit, while preserving the lowest possible form-factor. The designed pFSL is visualized in Fig. 4 together with a photo of its built implementation, where the values and the model numbers of the selected lumped components are listed in the caption. The measured electrical response of the reported pFSL was first characterized through the extraction of its S-parameters for driving power levels (e.g., -30 dBm) much lower than the expected limiting threshold, thus in the operative regime where a linear operation can be assumed. Fig. 5 shows the resulting measured and closely matching simulated plots of the pFSL’s S_21 and S_11 vs. f_in. Evidently, the reported pFSL exhibits a band-pass characteristic with a measured 3-dB fractional bandwidth (BW) of 17%. Also, a minimum IL^a-s of 0.94 dB was measured for a frequency (2.06 GHz) close to the targeted f_in^opt. Such a record-low IL^a-s value closely matches both the corresponding circuit simulated one (0.9 dB) and our analytically derived expectation (0.6 dB, see Fig. 2b).

Later, we characterized the pFSL response for P_in approaching and exceeding P_{th}. In order to most reliably extract P_{th}, we found the minimum P_in value around 2.1 GHz triggering a 2:1 sub-harmonic oscillation in the circuit. In order to do so, we identified the power level at which a bifurcation triggering a 2:1 frequency division occurs from the measured output power (P_{sub}, see Fig. 6) at half of any explored driving frequencies. It is worth emphasizing that P_{sub} is not trivial only for P_in exceeding P_{th}. As shown in Fig. 6, the measured pFSL exhibits a minimum P_{th} of -3.4 dBm at 2.06 GHz (i.e., the same frequency minimizing IL^a-s, see Fig. 5). Such a measured P_{th} value matches closely the predicted one found from the circuit simulated trend of P_{sub} vs. P_in (see the dotted line in Fig. 6). This simulated trend was obtained by utilizing the pAG technique and the extracted electromagnetic model (EM) of the designed board, together with the S-parameters of the selected lumped components. The measured P_{th} is also close to its analytically predicted value (-4.8 dBm, see Fig. 2a), given the capacitance of the selected diode and the value chosen for Z_{tx}. The IS value of the built pFSL at 2.06 GHz was assessed as well. This was done by extracting the corresponding S_21 for P_in values ranging from -10 dBm to 28 dBm (the maximum available power level in our experiment, Fig. 7a). As evident, significant IS values up to 5.4 dB were found for P_in > P_{th} and lower than 13 dBm. Within this power range, the designed pFSL shows a trend of the large signal S_21 vs. f_in that realizes a frequency selective notch centered around 2.06 GHz, clearly indicating the activation of a frequency selective attenuation as P_in is increased above P_{th} (see the inset of Fig. 7a). Furthermore, despite its less frequency selective limiting behavior for P_in > P_{max}, the measured pFSL shows high IS values even for P_in higher than 13 dBm (IS > 12.0 dB for P_in approaching 28 dBm). It is worth emphasizing that the achievement of such high IS value is granted by a parametrically triggered nonlinear mechanism causing the return-loss at the two pFSL’s ports to significantly increase as P_in is made larger than P_{th} (see Fig. 7b).

Nevertheless, both the measured S_21 and S_11 trends vs. P_in (Fig. 7) do not show a fully monotonic behavior, as also expected from the corresponding simulated trends (see the dotted lines in Fig. 7). This is due to changes in the diode’s dynamics becoming more and more significant as the input power approaches P_{max}. In particular, through our circuit simulations, we found that the P_in value associated with the local maximum (minimum) of the S_21 (S_11) for P_in > P_{th} corresponds to a peak voltage level across the adopted diode equal to V_{be} + V_{DC}. This finding provided us with simple means to identify the P_{max} value [13 dBm, close to its estimated analytical value (14 dBm, see Fig. 3)]
of the built pFSL by extracting the \( P_{in} \) level at which the same phenomenological change occurs in both the measured \( S_{21} \) and \( S_{11} \) trends. Finally, we evaluated the performance of the built pFSL when simultaneously driven by a 2.06 GHz signal and by a much lower power (-30 dBm) in-band tone. In order to do so, we relied on a conventional two-tone harmonic test where two RF signals, combined through an external power combiner (Mini-Circuits ZFRSC-42-S+), were simultaneously injected in the circuit from the pFSL’s input port. In particular, the signal at 2.06 GHz, with power labeled as \( P_1 \), emulated the presence of a strong EMI at the pFSL’s input port whereas the second much lower power signal (with -30 dBm), detuned from 2.06 GHz by an amount labeled as \( \Delta \) (i.e., \( f_2 = 2.06 \text{ GHz} + \Delta \)), was used to emulate the presence of a simultaneously received low-power signal carrying useful information. The output power levels at 2.06 GHz (\( P_{out}^{(2)} \)), at \( f_2 \) (\( P_{out}^{(2)} \)) and the one (\( P_{out}^{(3)} \)) at the strongest 3\(^{rd}\)-order intermodulation product (\( f_3 = 4.12 \text{GHz} - f_2 \)) were measured for \( P_1 \) levels ranging from -10 dBm to 21 dBm. It is crucial to emphasize that achieving low \( P_{out}^{(3)} \) values is particularly important in applications where contiguous in-band channels with small frequency separations can be simultaneously received. The measured trends of \( P_{opt}^{out} \), \( P_{out}^{(2)} \) and \( p_{out}^{(3)} \) vs. \( P_1 \) are reported in Fig. 8a and Fig. 8b for \( \Delta \) values varying...
between 2 MHz and 25 MHz. It can be seen that the parametric mechanism responsible for the suppression of $P_{\text{out}}^{\text{opt}}$ also causes an undesired attenuation ($\alpha$) of $P_{\text{out}}^{(2)}$ that is higher for small values of $\Delta$ (see Fig 8b). Yet, $\alpha$ values not exceeding 2 dB and 4 dB were attained for $\Delta$ values of 10 MHz and 5 MHz, thus demonstrating a good frequency selectivity in the limiting operation generated by the circuit. Also, $P_{\text{out}}^{(3)}$ values below -40 dBm were measured for $P_{\text{in}}$ values lower than $P_{\text{max}}$ and for $\Delta$ higher than 10 MHz. It is key to point out that the ability to achieve such low $P_{\text{out}}^{(3)}$ values, regardless of the active parametrically triggered power limiting behavior, is due to the low impact exerted by the varactor’s quadratic nonlinearities on the circuit dynamics for power levels that are lower than $P_{\text{max}}$. Nevertheless, for $P_{\text{in}}$ larger than $P_{\text{max}}$ the compressing and non-frequency-selective diode’s electrical response determines a saturation in the power level at all frequencies in the circuit, causing the observed behavior for $P_{\text{in}} > 13$ dBm. Ultimately, while the observation of $P_{\text{sub}}$ has provided us with reliable means to quantify $P_{\text{th}}$, the corresponding parametrically generated sub-harmonic signal, even if small, can also slightly degrade the signal-to-noise ratio $(\text{SNR})$ at the $p$FSL’s output. Nevertheless, due to the large frequency separation between the $p$FSL’s main operational frequency and its sub-harmonic one, a strong attenuation of $P_{\text{sub}}$ can still be achieved through the adoption of a proper filtering stage at the $p$FSL output, without altering the circuit dynamics.

A. Threshold and frequency reconfigurability

After characterizing the operation of the built $p$FSL at the $V_{\text{DC}}$ value (1.1 V) resulting into the lowest $P_{\text{th}}$ around 2.1 GHz, we investigated the possibility to leverage different biasing conditions for the diode to reconfigure $P_{\text{th}}$ and the frequency at which the highest $\text{IS}$ value is desired. Yet, to ensure that the built $p$FSL can be practically used to suppress EMI with different frequencies or power levels from the originally targeted value, we measured $P_{\text{th}}$, $\text{IL}^{*,s}$ and the maximum $\text{IS}$ for $P_{\text{in}} < P_{\text{max}}$ ($\text{IS}_{\text{max}}$) for a broad range of $V_{\text{DC}}$ and $f_{\text{in}}$ values. This allowed us to construct three corresponding contour plots (see Fig. 9) capturing the value of each performance metric for the analyzed $f_{\text{in}}$ and $V_{\text{DC}}$ values. As evident, through the strategic adoption of $V_{\text{DC}}$, the measured $p$FSL can simultaneously achieve $P_{\text{th}}$ and $\text{IL}^{*,s}$ values lower than 2 dBm and 2 dB respectively, $\text{IS}_{\text{max}}$ values up to 7 dB and a tunable operational frequency ranging from 1.85 GHz to 2.1 GHz.

B. Comparison with the State-of-the-Art

To benchmark the performance attained by our $p$FSL prototype with those attained by other passive diode-based FSLs, we compared (see Table I) the $P_{\text{th}}$, $\text{IL}^{*,s}$, $f_{\text{opt}}^{(3)}$ and $\text{IS}_{\text{max}}^{\text{pFSL}}$ of our built $p$FSL when $V_{\text{DC}}$ is chosen to minimize $P_{\text{th}}$ with the corresponding values exhibited by the most recent demonstrated counterparts. Also, the $\text{IS}$ value ($\text{IS}^{28\text{dBm}}$) of the reported $p$FSL for a much larger $P_{\text{in}}$ value (28 dBm) than $P_{\text{th}}$ was also compared to those of the other counterparts listed in Table I to assess the capability to protect any cascaded electronic components even from exceptionally strong EMI. As evident from Table I, the $p$FSL reported in this work exhibits the lowest $P_{\text{th}}$ and $\text{IL}^{*,s}$ values among all the previously demonstrated diode-based passive FSLs, even though it is operating at one of the highest frequencies. In particular, the $P_{\text{th}}$ value attained by our reported $p$FSL is nearly five times lower than what achieved by the previously reported SoA $p$FSL counterparts operating within the same frequency range. Nevertheless, when $V_{\text{DC}}$ is selected to minimize $P_{\text{th}}$, $\text{IS}_{\text{max}}^{\text{pFSL}}$ is lower than what shown by the other previously reported diode-based FSLs. Yet, as shown in Fig. 9, $\text{IS}_{\text{max}}^{\text{pFSL}}$ can be increased up to 7 dB by relying on slightly different $V_{\text{DC}}$ values, at the cost of higher $P_{\text{th}}$ (still lower than 2 dBm) and $\text{IL}^{*,s}$ (still lower than 2 dB). Furthermore, it is important to point out that, differently from other listed prototypes, the reported $p$FSL exhibits a large $\text{IS}^{28\text{dBm}}$ exceeding 12.0 dB, limiting the maximum output power delivered to any cascaded components to 13 dBm even in those scenarios when strong EMI with power approaching 30 dBm is received. Finally, by looking at the reported area of all the FSLs listed in Table I, it is easy to notice that our reported $p$FSL shows the highest degree of miniaturization.

In the next section an alternative approach not relying on changes of $V_{\text{DC}}$ is introduced and experimentally validated to enhance both $\text{IS}_{\text{max}}^{\text{pFSL}}$ and $\text{IS}^{28\text{dBm}}$ without significantly...
TABLE I: A performance comparison between the reported pFSL and other previously reported diode-based prototypes. Note: the reported $IS_{\text{2dB}}$ values marked with a "*" were estimated through a linear interpolation of available measured data that refer to a maximum $P_{\text{in}}$ value lower than 28 dBm.

| Tech.       | $P_{\text{th}}$ (dBm) | $IL^{s,s}$ (dB) | $f_{\text{in}}$ (MHz) | $IS_{\text{max}}^{P_{\text{max}}}$ (dB) | $IS_{\text{max}}^{P_{\text{max}}}$ (dB) | Component Area (cm²) |
|-------------|----------------------|----------------|----------------------|----------------------------------|----------------------------------|---------------------|
| [13] Parametric | 4.5                  | 3              | 850                  | 9                               | <3 dB*                           | n/a                 |
| [14] BSF     | 3                    | 2              | 1000                 | 13                              | <18 dB*                          | ~9                  |
| [19] BPF     | 24                   | 2              | 1500                 | 10                              | 10                               | 378                 |
| [18] Coupler | 6                    | 1.5            | 2000                 | 8                               | 12                               | ~3.5                |
| This work   | -3.4                 | 0.94           | 2060                 | 5.4                             | 12.0                             | 2.2                 |

C. Increasing IS through multiple pFSL stages

Similarly to what was previously shown for absorptive pFSLs [13], cascading multiple reflective pFSLs provides useful means to increase $IS_{\text{max}}^{P_{\text{max}}}$, augmenting the maximum achievable suppression at $f_{\text{in}}^{\text{opt}}$. Nevertheless, this technique can be practically leveraged only when absorptive or reflective pFSLs with low $IL^{s,s}$ are available, such as the one we designed and built in this work. In fact, since the insertion-loss of a chain of pFSLs ($IL_{\text{chain}}^{s,s}$) grows proportionally with the number of cascaded stages ($M$), there exists an inevitable trade-off between the maximum exploitable $M$ and the highest tolerated $IL_{\text{chain}}^{s,s}$. Also, differently from any chains of absorptive pFSLs whose design and operation inevitably lead to $P_{\text{th}}$ values increasing proportionally to $M$, the high $Z_{\text{in}}$ (see Fig. 1) value exhibited by reflective pFSLs for $P_{\text{in}} < P_{\text{th}}$ renders the voltage at $f_{\text{in}}^{\text{opt}}$ across all the adopted diodes almost independent of $M$, especially when $Z_{\text{in}}$ is chosen to be much higher than $R_0$ in order to minimize $IL^{s,s}$. This key operational feature allows to preserve low $P_{\text{th}}$ values even when multiple reflective pFSL stages are used to enable higher $IS_{\text{max}}^{P_{\text{max}}}$ values. Moreover, contrary to absorptive pFSLs, the adoption of multiple reflective pFSL stages permits to increase even the IS values attained for much higher $P_{\text{in}}$ values than $P_{\text{max}}^s$.

In order to demonstrate the capability to achieve higher $IS_{\text{max}}^{P_{\text{max}}}$ values through the adoption of multiple pFSL stages, we built a copy of the pFSL discussed in the previous section. The two pFSLs were then connected to each other and the modified trends of the $S_{21}$ vs. $P_{\text{in}}$ were extracted (Fig. 10a), along with the corresponding trend of the output power vs. $P_{\text{in}}$ at 2.06 GHz (i.e., the $f_{\text{in}}$ value giving the lowest threshold for a single stage pFSL). As evident from Fig. 10, the chain formed by the two built pFSL stages allows to significantly enhance the maximum $IS_{\text{max}}^{P_{\text{max}}}$ value attained by just one stage, while causing negligible (<1 dB) increases of $P_{\text{th}}$ and $IL^{s,s}$.

V. CONCLUSION

In this article, we discussed the design criteria and measured performance of a ~2.1 GHz diode-based reflective
parametric frequency selective limiter (pFSL) built on a FR-4 printed-circuit-board (PCB) and using commercial off-the-shelf components. Thanks to its engineered dynamics, the reported pFSL prototype can exhibit record-low insertion-loss for low-power signals ($IL_p < -2$ dB), record-low power threshold ($P_{th} < -3.4$ dBm) and a significant suppression (up to 5.4 dB) for input power levels lower than the one forcing the diode to operate in its forward conduction. Furthermore, due to its unique design characteristics and regardless of the inevitable reduction in frequency selectivity, the built pFSL ensures a good protection even from much stronger interference signals with power approaching 28 dBm. In addition, by strategically tuning the DC-biasing voltage of the diode, the reported pFSL allows to reconfigure the frequency at which the maximum $IS_p$ is obtained by nearly 250 MHz (corresponding to a tuning range of ~0.12), while simultaneously preserving low $P_{th} (< 2$ dBm) and $IL_{p,a} (< 2$ dB) values. Finally, by connecting two copies of the same pFSL designed and built in this work, we demonstrated that a significantly larger suppression value (>8 dB) for high-power signals can be attained, while preserving low $P_{th} (< 2.5$ dBm) and low $IL_{p,a} (< 2$ dB).

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