Phosphorene: An Unexplored 2D Semiconductor with a High Hole Mobility

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ABSTRACT We introduce the 2D counterpart of layered black phosphorus, which we call phosphorene, as an unexplored p-type semiconducting material. Same as graphene and MoS₂, single-layer phosphorene is flexible and can be mechanically exfoliated. We find phosphorene to be stable and, unlike graphene, to have an inherent, direct, and appreciable band gap. Our ab initio calculations indicate that the band gap is direct, depends on the number of layers and the in-layer strain, and is significantly larger than the bulk value of 0.31–0.36 eV. The observed photoluminescence peak of single-layer phosphorene in the visible optical range confirms that the band gap is larger than that of the bulk system. Our transport studies indicate a hole mobility that reflects the structural anisotropy of phosphorene and complements n-type MoS₂. At room temperature, our few-layer phosphorene field-effect transistors with 1.0 μm channel length display a high on-current of 194 mA/mm, a high hole field-effect mobility of 286 cm²/V·s, and an on/off ratio of up to 10⁶. We demonstrate the possibility of phosphorene integration by constructing a 2D CMOS inverter consisting of phosphorene PMOS and MoS₂ NMOS transistors.

KEYWORDS: phosphorene · anisotropic transport · transistor · inverter

Phosphorene is a 2D semiconductor with a high hole mobility, which is an important advantage over other 2D materials. It is derived from black phosphorus, a material with a vanishing gap and low mobility. Phosphorene has a direct band gap, which is larger than that of the bulk system, and exhibits superior hole mobility compared to other 2D semiconductors. The high hole mobility of phosphorene makes it suitable for use in high-performance electronic devices. In this study, we demonstrate the feasibility of using phosphorene as an alternative to graphene and MoS₂ in the development of 2D CMOS inverters. The high on-off ratio and high hole field-effect mobility of phosphorene make it a promising material for future electronic applications.
and, furthermore, demonstrate the first CMOS inverter using few-layer phosphorene as the p-channel and MoS$_2$ as the n-channel.

Black phosphorus, the bulk counterpart of phosphorene, is the most stable phosphorus allotrope at room temperature that was first synthesized from white phosphorus under high pressure and high temperature in 1914. Similar to graphite, its layered structure is held together by weak interlayer forces with significant van der Waals character. Previous studies have shown this material to display a sequence of structural phase transformations, superconductivity at high pressures with $T_c$ above 10 K, and temperature-dependent resistivity and magnetoresistivity. Two-dimensional phosphorene is, besides graphene, the only stable elemental 2D material that can be mechanically exfoliated.

**RESULTS AND DISCUSSION**

We have determined the equilibrium geometry, bonding, and electronic structure of black phosphorus, few-layer and single-layer phosphorene using *ab initio* density functional theory (DFT) calculations with the PBE$^{28}$ and HSE06$^{29}$ functionals as implemented in the SIESTA$^{30}$ and VASP$^{31}$ codes. As seen in the optimized structure depicted in Figure 1a–c, phosphorene layers share a honeycomb lattice structure with graphene with the notable difference of nonplanarity in the shape of structural ridges. The bulk lattice parameters $a_1 = 3.36 \, \text{Å}$, $a_2 = 4.53 \, \text{Å}$, and $a_3 = 11.17 \, \text{Å}$, which have been optimized by DFT-PBE calculations, are in good agreement with the experiment. The relatively large value of $a_3$ is caused by the nonplanar layer structure and the presence of two AB stacked layers in the bulk unit cell. The orthogonal lattice parameters $a_1 = 3.35 \, \text{Å}$ and $a_2 = 4.62 \, \text{Å}$ of the monolayer lattice, depicted in Figure 1b,c, are close to those of the bulk structure, as expected in view of the weak 20 meV/atom interlayer interaction that is comparable to graphite. We note that the ridged layer structure helps to keep orientational order between adjacent phosphorene monolayers and thus maintains the in-plane anisotropy; this is significantly different from graphene with its propensity to form turbostratic graphite.

Our calculated band structure in Figure 1d indicates that a free-standing phosphorene single layer is a semiconductor with a direct band gap of 1.0 eV at $\Gamma$, significantly larger than our calculated band gap value $E_g = 0.31 \, \text{eV}$ for the bulk system. These calculations, performed using the HSE06 functional$^{29}$ reproduce the observed bulk band gap value $0.31$–$0.36 \, \text{eV}$$^{17,20,22}$ and are based on the assumption that the same mixing parameter $\alpha$ in HSE06 is appropriate in bulk as well as in few-layer systems. Of particular interest is our finding that the band gap depends sensitively on the number of layers $N$ in a few-layer slab, as shown in Figure 1e. We find that $E_g$ scales as the inverse number of layers and changes significantly between 1.0 eV in a single layer and 0.3 eV in the bulk, indicating the possibility to tune the electronic properties of this system. Equally interesting is the sensitive dependence of the gap on in-layer strain along different directions, shown in Figure 1f. Of particular importance is our finding that a moderate in-plane compression of $\approx 5\%$...
or more, possibly caused by epitaxial mismatch with a
substrate, will change phosphorene from a direct-gap
to an indirect-gap semiconductor with a signifi-
cantly smaller gap. Details of the computational approach are
listed in the Experimental Methods section and in the
Supporting Information.

Atomically thin single-layer or few-layer phos-
phorene was achieved via mechanical exfoliation of
commercially available (Smart-elements) bulk black
phosphorus. A 300 nm SiO$_2$-coated silicon wafer was
used as the substrate. Figure 2a shows the atomic force
microscopy (AFM) image of an exfoliated single-layer
phosphorene crystal. A step height of $\sim 0.85$ nm mea-
sured at the crystal edge con-
fi rms the presence of
single-layer phosphorene. Even though the step height
is slightly larger than the theoretical value of 0.6 nm
for single-layer phosphorene, we generally expect that
the AFM-measured thickness value of a single-layer 2D
crystal on SiO$_2$/Si substrate is higher than the theo-
retical value; this is widely observed in graphene and
MoS$_2$ cases.$^{33}$ Photoluminescence (PL) of exfoliated single-layer phosphorene is observed in the visible
wavelengths as shown in Figure 2b. For 10 nm thick
black phosphorus flakes, no PL signal is observed within
the detection spectrum range because the expected
band gap of bulk black phosphorus is as low as $\sim 0.3$ eV,
falling in the infrared wave region. In contrast, a
pronounced PL signal centered at 1.45 eV with a
$\sim 100$ meV narrow width is obtained on a single-layer
phosphorene crystal. This observed PL peak is likely of
excitonic nature and thus a lower bound on the funda-
mental band gap value. The measured value of 1.45 eV
indirectly confirms that the band gap in the monolayer
is significantly larger than in the bulk. Further studies
are required to properly interpret the PL spectra, which
depend on the density of states, frequency-dependent
quantum yield, the substrate, and the dielectric envi-
noment. We conclude that the predicted increased
band gap value in single-layer phosphorene, caused by
the absence of interlayer hybridization near the top of
the valence and bottom of the conduction band, is
consistent with the observed photoluminescence signal.

Still, we believe to have achieved few-layer phosphor-
en, as confirmed by Raman spectroscopy. Our Raman
spectra of single-layer, bilayer, and bulk black phos-
phorus are presented in Figure 2c. The Raman spectra
show a well-defined thickness dependence, with the
$A_g^1$ and $A_g^2$ modes shifting toward each other in fre-
quency when the thickness is increased, similar to
what has been observed in MoS$_2$.$^{34}$

Although single-layer or bilayer phosphorene can be
physically realized by exfoliation, it is more sensitive to
the environment compared to graphene or MoS$_2$. All attempts to study transport properties or device performance on phosphorene films less than \( \sim 2 \text{ nm} \) thick were not successful. Since single-layer phosphorene is one atomic layer thick, it should be more stable and display a lower defect density than transition metal dichalcogenides such as MoS$_2$. The processes to significantly reduce the defect density in back phosphorus and phosphorene films and to passivate the defects and surfaces need to be further developed. We focus on few-layer phosphorene thicker than 2 nm in the following transport and device experiments.

Anisotropic transport behavior along different directions is a unique property for few-layer phosphorene. A black phosphorus crystal with the thickness of \( \sim 10 \text{ nm} \) was peeled and transferred onto a 90 nm SiO$_2$-capped Si substrate. Metal contacts were symmetrically defined around the crystal with 45° as the angular increment of the orientation, as shown in Figure 3a. We fabricated 1 μm wide 20/60 nm thick Ti/Au contacts to few-layer phosphorene so that the spacing between all opposite bars was 5 μm. We used the four pairs of diametrically opposite bars as source/drain contacts for a transistor geometry and measured the transistor behavior for each of these devices. The maximum drain current at 30 V back gate bias and 0.5 V drain bias, which we display in Figure 3b as a function of the orientation of the contact pair, shows clearly an angle-dependent transport behavior. The anisotropic behavior of the maximum drain current is roughly sinusoidal, characterized by the minimum value of \( \approx 85 \text{ mA/mm} \) at 45° and 225°, and the maximum value of \( \approx 137 \text{ mA/mm} \) at 135° and 315°. In spite of the limited 45° angular resolution, the observed 50% anisotropy between two orthogonal directions is significant. The same periodic trend can be found in the maximum value of the transconductance, which could be partially related to a mobility variation in the \( x \)–\( y \) plane of few-layer phosphorene. This large mobility variation is rarely seen in other conventional semiconductors. It could be partially related to the uniquely ridged structure in the 2D plane of few-layer phosphorene, seen in Figure 1a–c, suggesting a different transport behavior along or normal to the ridges. On the basis of the band dispersion plotted in Figure 1d, we find that perpendicular to the ridges, corresponding to the \( \Gamma \)–\( Y \) direction, the effective mass of electrons and holes \( m_e \approx m_h \approx 0.3 m_0 \) is a fraction of the free electron mass \( m_0 \). Parallel to the ridges, along the \( \Gamma \)–\( X \) direction, the carriers are significantly heavier, with the effective mass of holes amounting to \( m_h \approx 8.3 m_0 \) and that of electrons to \( m_e \approx 2.6 m_0 \) suggesting anisotropic transport behavior.
The observed anisotropy is less pronounced than the prediction because the angle resolution is as large as 45 °C and the fringe current flow in the real device averages out partly the anisotropy.

In order to investigate the nature of the metal/phosphorene junction, we used a three-terminal method, similar to the Kelvin probe, to measure the forward bias $I$–$V$ characteristics of the Ti/phosphorene metal/semiconductor junction at the constant back gate voltage $V_{bg} = -30$ V and display our results in Figure 3c. Current was passed between two Ti/phosphorene contacts of a multi-terminal device with contacts around the perimeter of the phosphorene flake. Voltage was measured between the forward biased contact and a third contact adjacent to it with zero current flowing through the third contact. Under these conditions, the measured voltage difference is equal to the voltage across the forward biased Ti/phosphorene contact. These data show an exponential increase in the current $I$ as the voltage $V$ across the junction increases from 70 to 130 mV. In view of the degenerate doping of the phosphorene sample and the exponential $I$–$V$ characteristics across this junction at temperatures as low as 20 K, we conclude that thermally assisted tunneling through the Schottky barrier is responsible for the transport through the junction. To determine the Schottky barrier height of the Ti/phosphorene contact, we fit the exponential $I$–$V$ characteristics by the equation $I_s = I_s \exp(V_s/\Phi_0)$, where $I_s$ is the characteristic current and $\Phi_0$ the characteristic energy, which characterizes transport across the junction at a particular temperature. Fits of the semilogarithmic plots in a wide temperature range are shown in Figure 3c. The temperature-dependent characteristic current $I_s$ can be furthermore viewed as proportional to $\exp(\Phi_0/\Phi_0)$, where $\Phi_0$ is the height of the Schottky barrier at the metal–semiconductor junction and $\Phi_0$ is a temperature-dependent quantity. This provides a way to use our temperature-dependent $I$–$V$ measurements to determine $\Phi_0$ from the slope of the quantity log $I_s$ as a function of $1/\Phi_0$. Figure 3d shows the corresponding plot, where each data point has been determined by fitting the $I$–$V$ characteristic curve at a particular gate voltage and temperature. The slope of all curves shows an impressive independence of the measurement conditions, indicating the Schottky barrier height $\Phi_0 \approx 0.21$ eV for holes at the Ti/phosphorene junction. We note that the barrier height determined here is the true Schottky barrier height at the metal/phosphorene junction, not an effective Schottky barrier height that is commonly determined for metal/semiconductor junctions via the activation energy method.11

We proceed to fabricate transistors of this novel 2D material in order to examine its performance in actual devices. We employed the same approach to fabricate transistors with a channel length of 1.0 μm as in our previous transport study. We used few-layer phosphorene with a thickness ranging from 2.1 to over 20 nm. The $I$–$V$ characteristic of a typical 5 nm thick few-layer phosphorene field-effect transistor for back gate voltages ranging from +30 to −30 V, shown in Figure 4a, indicates a reduction of the total resistance with decreasing gate voltage, a clear signature of its p-type characteristics. Consequently, few-layer phosphorene is a welcome addition to the family of 2D semiconductor materials since most pristine TMDs are either n-type or ambipolar as a consequence of the energy level of S vacancy and charge-neutral level coinciding near the conduction band edge of these materials.11,14 In only a few cases, p-type transistors have been fabricated by externally doping 2D systems using gas adsorption, which is not easily practicable for solid-state device applications.4,36 The observed linear $I$–$V$ relationship at low drain bias is indicative of good contact properties at the metal/phosphorene interface. We also observe good current saturation at high drain bias values, with the highest drain current of 194 mA/μm at 1.0 μm channel length at the back gate voltage $V_{bg} = -30$ V and drain voltage $V_{ds} = -2$ V. In Figure 4b, we present the transfer curves for drain bias values $V_{ds} = 0.01$ and 0.5 V, which indicate a current on/off ratio of ~10⁴, a very reasonable value for a material with a bulk band gap of 0.3 eV. We also note that, according to Figure 1d, the band gap of few-layer phosphorene is widened significantly due to the absence of interlayer hybridization between states at the top of the valence and bottom of the conduction band.

Inspecting the transfer curves in Figure 4b, we find the maximum transconductance to range from $G_{m} = 45 \mu S/\mu m$ at $V_{ds} = 0.01 \text{ V}$ to 2.28 mS/μm at 0.5 V drain bias. Using simple square law theory, we can estimate the field-effect mobility $\mu_{FE}$ from $G_{m} = \mu_{FE}C_{ox}W/LV_{ds}$, where $C_{ox}$ is the capacitance of the gate oxide, $W$ and $L$ are the channel width and length, and $V_{ds}$ is the drain bias. Our results for $V_{ds} = 0.01 \text{ V}$ indicate a high field-effect mobility $\mu_{FE} = 286 \text{ m}^2/\text{V} \cdot \text{s}$ at room temperature, and our four-terminal measurements suggest a factor of 5 improvement at low temperatures (see the Supporting Information). These values are still smaller than those in bulk black phosphorus, where the electron and hole mobility is $\approx 1000 \text{ cm}^2/\text{V} \cdot \text{s}$ at room temperature and could exceed 15 000 cm²/V·s for electrons and 50 000 cm²/V·s for holes at low temperatures.37 We consider the following factors to cause the mobility reduction in few-layer phosphorene. (i) The exposed surface of few-layer phosphorene is chemically unstable. Chemisorbed species from the process and the environment change the electronic structure and scatter carriers, thus degrading the mobility. (ii) In a particular transistor, the current flow may not match the direction, where the material has the highest in-plane mobility. (iii) The Schottky barrier at the metal/phosphorene interface induces a large contact resistance within the undoped source/drain regions.
We expect that the real mobility of few-layer phosphorene should increase significantly upon appropriate surface passivation and in a high-k dielectric environment.

We further compare field-effect mobility in few-layer phosphorene transistors with various crystal thicknesses. Field-effect mobilities extracted from devices fabricated on phosphorene crystals with various thicknesses are displayed in Figure 4c. Similar to previous studies on MoS$_2$ transistors, the field-effect mobility shows a strong thickness dependence. It peaks at around 5 nm and decreases gradually with further increase of crystal thickness. Such trend can be modeled with screening and interlayer coupling in layered materials, as proposed in several previous studies. A more dispersive mobility distribution is observed for few-layer phosphorene transistors. This is due to the fact of anisotropic mobility in few-layer phosphorene or black phosphorus as discussed in previous parts and the random selection of crystal orientation in device fabrication. Thus carrier transports along at any directions between the two orthogonal ones in the $x$–$y$ plane. Therefore, two curves are modeled for phosphorene transistors, as shown in Figure 4c, where the red and green curves show the fittings with mobility peak and valley, respectively. The current on/off ratio is shown in Figure 4d. It shows a general decreasing trend with increasing crystal thickness, steeply dropping from $\sim 10^2$ for a 2 nm crystal to less than 10 once the crystal thickness exceeds 15 nm. This suggests the importance of crystal thickness selection of phosphorene transistors from the point of view of device applications. Transistors on a 4–6 nm crystal display the best trade-off with higher hole mobility and better switching behavior.

Finally, we demonstrate a CMOS logic circuit containing 2D crystals of pure few-layer phosphorene as one of the channel materials. Since phosphorene shows well-behaved p-type transistor characteristics, it can complement well n-type MoS$_2$ transistors. Here we demonstrate the simplest CMOS circuit element, an inverter, by using MoS$_2$ for the n-type transistor and phosphorene for the p-type transistor, both integrated on the same Si/SiO$_2$ substrate. Few-layer MoS$_2$ and phosphorene flakes were transferred onto the same substrate successively by the scotch tape technique. Source/drain regions were defined by e-beam lithography, similar to the PMOS fabrication described above. We chose different channel lengths of 0.5 $\mu$m for MoS$_2$ and 1 $\mu$m for phosphorene transistors to compensate for the mobility difference between MoS$_2$ and phosphorene by modifying the width/length ratio for NMOS and PMOS. Ti/Au of 20/60 nm was used for both MoS$_2$ and phosphorene contacts. Prior to top growth of a high-k dielectric, a 1 nm Al layer was deposited on the sample by e-beam evaporation.
**EXPERIMENTAL METHODS**

All optical measurements are carried out in ambient atmosphere at room temperature using a microscope coupled to a grating spectrometer with a CCD camera. Optical beams are focused on the sample with a spot diameter of \( \sim 1 \ \mu m \). For the PL study, the samples are excited with a frequency-doubled Nd:YAG laser at a wavelength of 532 nm, and the CCD camera senses photons in the spectrum range between 1.3 and 2.0 eV. Scotch-tape-based microcleavage of the layered bulk black phosphorus and MoS\(_2\) crystals is used for fabrication of all 2D devices containing phosphorene or MoS\(_2\) layers, followed by transfer onto the Si/SiO\(_2\) substrate, as previously described in graphene studies. Bulk crystals were purchased from Smart-elements (black phosphorus) and SPI Supplies (MoS\(_2\)). Degenerately doped silicon wafers (0.01–0.02 \( \Omega \cdot cm \)) capped with 90 nm SiO\(_2\) were purchased from SQI (Silicon Quest International). After few-layer crystals of phosphorene and/or MoS\(_2\) were transferred onto the substrate, all samples were sequentially cleaned by acetone, methanol, and isopropyl alcohol to remove any Scotch tape residue. This procedure has been followed by a 180 °C postbake process to remove solvent residue. The thickness of the crystals was determined by a Veeco Dimension 3100 atomic force microscope. E-beam lithography has been carried out using a Vistec VB6 instrument. The 20/60 nm Ti/Au contacts were deposited using the e-beam evaporator at a rate of 1 Å/s to define contact electrodes and metal gates. No annealing has been performed after the deposition of the metal contacts. The top gate dielectric material was deposited by an ASM F-120 ALD system at 250 °C, using trimethylaluminium (TMA) and H\(_2\)O as precursors. The pulse time was 0.8 s for TMA and 1.2 s for water, and the purge time was 5 s for both.

**Theoretical Methods.** Our computational approach to determine the equilibrium structure, stability, and electronic properties of black phosphorus is based on \textit{ab initio} density functional theory. Our computational approach to determine the equilibrium structure, stability, and electronic properties of black phosphorus is based on \textit{ab initio} density functional theory. We used \textit{ab initio} calculations to determine the equilibrium structure and the interlayer interaction of bulk black phosphorus as well as few-layer phosphorene with \( \sim 1–4 \) layers. Our theoretical results indicate that the band gap is direct, depends on the number of layers and the in-layer strain, and is significantly larger than the bulk value of 0.31–0.36 eV. We have successfully achieved a single-layer phosphorene film. The observed photoluminescence peak in the visible wavelength from single-layer phosphorene indirectly confirms the widening of the band gap as predicted by theory. We find substantial anisotropy in the transport behavior of this 2D material, which we associate with the unique ridge structure of the layers. The overall device behavior can be explained by considering a Schottky barrier height of 0.21 eV for hole tunneling at the junctions between phosphorene and Ti metal contacts. We report fabrication of p-type transistors of few-layer phosphorene with a high on-current of 194 mA/mm at 1.0 \( \mu m \) channel length, a current on/off ratio over \( 10^4 \), and a high field-effect mobility up to 286 cm\(^2\)/V\cdot s at room temperature. We have also constructed a CMOS inverter by combining a phosphorene PMOS transistor with a MoS\(_2\) NMOS transistor, thus achieving heterogeneous integration of semiconducting phosphorene crystals as a novel channel material for future electronic applications.
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