Possible layout solutions for the improvement of the dark rate of geiger mode avalanche structures in the GLOBALFOUNDRIES BCDLITE 0.18 μm CMOS technology

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ABSTRACT: Modern concepts of single photon or charged particle detection systems are based on geiger mode avalanche devices developed in CMOS technology. The key-problem encountered in the fabrication of these devices in CMOS is the dark rate level. The dark rate and single photon signal are not distinguishable. This sets also the limits of the application of geiger mode avalanche devices to single photon or charged particle detection systems. We report the design and fabrication of four possible layouts of these devices using the 0.18 μm BCDLite GLOBALFOUNDRIES process. The devices have an area of 50 × 50 μm². They are characterized by a fast response time and an approximately 60 ns recovery time. The best topology exhibits an average dark rate as low as 3 × 10³ kHz/mm².

KEYWORDS: Photon detectors for UV, visible and IR photons (solid-state); Photon detectors for UV, visible and IR photons (solid-state) (PIN diodes, APDs, Si-PMTs, G-APDs, CCDs, EBCCDs, EMCCDs etc.)
1 Introduction

Geigermodeavalanchestructuresdevelopedincomplementarymetaloxidesemiconductor(CMOS)
representtheultimatefrontierinthefieldofsinglephotondetectionwithastrongimpactonnuclear
medicine, high energy physics, astrophysics and beyond [1]. In the last few years several new
detector concepts for single photons, low photon flux, or charged particles have been developed
on the basis of these devices [2–10]. The key-advantage of CMOS technology is that sensor and
electronics can be developed on a single chip, also with complex digital schemes for artificial
intelligence, in the same production line [11–16].

Several testsofgeigermodeavalanche detectionstructureswerereportedintheliteratureusing
0.8 µm [17–23], 0.7 µm [24], 0.5 µm [25], 0.35 µm [16, 26–34], 0.18 µm [2, 35–37], 0.15 µm [38],
0.13 µm [39–44], 0.09 µm [45, 46] CMOS processes.

One of the key-problems in the development of these structures is a large dark noise rate, due
to either shallow trench isolation or higher doping concentration of the standard CMOS wells. The
dark pulse signal is generated by thermal electron-hole pair excitation and is not distinguishable
from the single photon detection. It is thus required to have a dark rate as low as possible. In order
to have an impression of the problem, the dark rate of the previously cited references is represented
as a function of the technology node on figure 1. Typical values of the dark rate are well above
1000 kHz/mm² and could constitute a problem for single photon detection applications. By way
of example, geigermode avalanchestructures developed at the 0.8 µm CMOS exhibit a dark noise
rate ranging from $3 \times 10^3$ kHz/mm² to $3 \times 10^6$ kHz/mm² [14]. Nowadays the most mature CMOS
scale for the production of geiger mode avalanche detection structure is 0.35 µm. It was recently
shown that an enlarged set of masks in the 0.35 µm technology node allows to overlap highly-
doped and lowly-doped regions and to tune the doping profiles of the standard CMOS wells. As
shown in the figure a dark rate ranging between 90 kHz/mm² and 200 kHz/mm² was obtained [3].
Furthermore a novel approach of perimeter-gated geiger mode avalanche breakdown sensor was
developed in the 0.5 µm CMOS technology node and has shown a dark rate as low as approximately
100 kHz/mm² [9].

The integration of geiger mode avalanche detection structures at a CMOS scale lower than
0.35 µm still presents limited dark rate performances. The lowest reported dark rate is approxi-
mately 500 kHz/mm² and is obtained at a scale of 0.13 µm [39]. Devices realized at the 0.18 µm
Figure 1. Dark rate obtained in geiger model avalanche structures developed at CMOS technology nodes with a scale ranging between 0.8 µm and 0.09 µm.

node showed a dark rate ranging between $10^4$ kHz/mm$^2$ and $10^5$ kHz/mm$^2$ [2, 35, 36]. Recently an improvement of the dark rate down to 680 kHz/mm$^2$ using the TSMC 0.18 µm HV CMOS process has been shown [37].

In this technical note we present four geiger mode avalanche structures fabricated at the BCDLite GLOBALFOUNDRIES 0.18 µm node. Compared to devices designed in more scaled technologies, our best structure has similar performances in terms of dark rate and signal characteristics. Compared to devices designed at the same CMOS scale, our best structure reaches a dark rate as low as $3 \times 10^3$ kHz/mm$^2$ and is showing a clear improvement in the development of geiger mode avalanche structures at the 0.18 µm CMOS node.

2 Materials and methods

The GLOBALFOUNDRIES 0.18 µm BCDLite process is an advanced mixed-signal CMOS process providing six metal layers, two polysilicon layers, high-resistivity polysilicon and two types of transistor gates (3.3 V and 5 V). In this paper we use the Medium Voltage (MV) option. As most of the 0.18 µm available standard CMOS processes at modern foundries, it does not offer an OPTO module and a passivation layer covers also the sensitive region. This process is used for standard electronics components and is suited for the integration of sensor and electronics on a single chip.

The device structure is based on a n-epitaxial layer, on which the geiger mode avalanche structure is formed. The cross section of the four layouts considered in this paper is shown on figure 2. Structure I (a) consists of a p$^+$/nwell junction. A virtual guard ring p$^+$/n-epi is formed on the periphery of the sensitive avalanche area in order to avoid the spontaneous triggering of breakdown avalanche due to the high-gradient electric field. Shallow Trench isolation (STI) is surrounding the sensitive area of the avalanche pixel sensor. This structure is based on the layout proposed in [2] for the BCDLite 0.18 µm CMOS node. We aim here to study any possible improvement using the MV option of this process. Structure II (b) is a variant of structure I. In
order to avoid any contact between the STI and the sensitive area of the device, a polysilicon gate is inserted around the p+ anode. This technique is used also in [39] for a different layout realized at the Chartered 0.13 µm/Tezzaron 3D process in order to reduce the dark rate. We aim here to show possible improvements in the dark rate also in the BCDLite GLOBALFOUNDRIES 0.18 µm node with the virtual guard ring layout under study. Structure III (c) is a variant of structure II. The polysilicon gate is at the same voltage of the p+ anode. Our aim is here to study any difference between floating and not-floating gate. Finally, structure IV (d) has a physical guard ring obtained with a lowly doped pwell implantation inserted around the p+ anode, as proposed for example in [3] for a 350 µm CMOS technology node, and a polysilicon ring to prevent the STI formation as in structure II.

The size of the sensitive cell is 50 × 50 µm². The avalanche in the microcell is quenched with a passive mechanism through a 250 kΩ quenching resistor implemented in the structure using High Resistor Polysilicon (HRP). The resistor width is 0.8 µm and its length is approximately 50 µm.

3 Results

All measurements are performed at a room temperature of 25°C. We evaluate the static current-voltage characteristics of the devices in dark condition using a Keithley 2636A source meter that obtains measurements of the current of the device in reverse bias mode. As reported on figure 3, structure I, structure III and structure IV show a similar behavior. They exhibit a dark current of approximately 1 pA before breakdown. At breakdown the current rises abruptly up to few nanoamperes until it gets limited by the quenching resistor and rises linearly. The breakdown voltage of structure I is approximately 12.6 V and is consistent with the results obtained in [2]. The breakdown voltage of structures III and IV is respectively 13.1 V and 13.2 V. The slight increase of the breakdown voltage shows that both the additional distance of the STI from the p+ implantation

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**Figure 2.** Cross section of the geiger mode avalanche structures produced with the 0.18 µm BCDLite GLOBALFOUNDRIES CMOS technology process.
Figure 3. Current-voltage characteristics of the four geiger mode avalanche devices realized at the MV BCDLite GLOBALFOUNDRIES 0.18 µm node.

![Current-voltage characteristics](image)

with not-floating polysilicon gates and the lightly-doped pwell ring around the p+ implantation have a beneficial smoothing effect to the electric field at the edges of the device. These results satisfy the expectations from previous studies. Breakdown voltages of approximately 12 V are obtained at similar 0.18 µm nodes [35, 36]. Breakdown voltages ranging from 10 V to 14 V are usually obtained at a scale lower than 0.18 µm, as at 0.09 µm [45, 46] and 0.13 µm [39] CMOS nodes. This value depends on the doping of the standard CMOS wells, which is ranging from $2 \times 10^{17}$ cm$^{-3}$ to $5 \times 10^{17}$ cm$^{-3}$. The current-voltage characteristics of structure II exhibits an additional leakage current, draining between n-epi substrate and floating polysilicon gate. The breakdown voltage of structure II is approximately 12.6 V and is thus lower than in structure III. In correspondence to the observations in [9], the definition of the voltage of the polysilicon ring is affecting the smoothing of the electric field at the edges of the structure and consequently the breakdown voltage of the device.

In order to perform a dynamic characterization of the dark noise of the devices, we observe at a 500 MHz bandwidth oscilloscope (DPO5054B) the voltage amplitude of the dark rate signals of the produced structures on a 50 Ω load resistor. The output voltage is connected to a fast amplifier, based on a two stages voltage amplifier obtained with the GALI 66+ wide-band monolithic chip [47].

Figure 4. Block diagram of the experimental setup for the measurement of the time characteristics of the dark rate signals.
The total amplification gain is adjusted to 10 with a voltage divider between the two amplification stages. The block diagram of the experimental setup is shown in figure 4. The signals corresponding to the four structures at an over-voltage of 2.2 V are shown on figure 5. They exhibit the typical features of a Geiger mode avalanche structure, with a very fast rise time, a fast transition glitch at the quenching time due to the capacitance mismatch between microcell and quenching resistor, and a decay corresponding to the discharge time of the device. As the four cells have equivalent area and quenching resistor, they feature an equivalent recovery time of approximately 60 ns, consistent with a device capacitance of approximately 240 fF. The obtained timing performances are competitive with similar structures. By way of example, a Geiger mode avalanche structure developed in 0.35 μm CMOS technology with the same area of the structures studied here and a quenching resistor of 220 kΩ has a capacitance of approximately 190 fF and a decay time of approximately 60 ns [3, 11].
Figure 6. Block diagram of the experimental setup for the measurement of the dark rate of the geiger mode avalanche structures.

Figure 7. Dark rate of the four geiger mode avalanche devices realized at the MV BCDLite GLOBAL-FOUNDRIES 0.18\,µm node.

The average rate of dark pulses is measured sending the signals after amplification to a threshold discriminator (CAEN N844). The number of pulses above threshold is registered within a 1 s observation time window using a scaler. The block diagram of the experimental setup is shown in figure 6. The average dark rate of the four structures measured at an over-voltage $V_{ov}$ of 2.2 V and 2.5 V is shown in figure 7. In order to facilitate the comparison of the reported results with other studies, the measured dark rate is normalized over the sensitive area of the sensors, which is 2500\,µm$^2$. In correspondence with the current voltage characteristics we observe that structure II exhibits a dark rate higher than $10^5$ kHz/mm$^2$. The dark rate of structures I, III and IV is $2 \times 10^4$ kHz/mm$^2$, $10^4$ kHz/mm$^2$ and $3 \times 10^3$ kHz/mm$^2$, respectively. The average dark rate of the four structures with area 2500\,µm$^2$ is 50 kHz, 250 kHz, 25 kHz, 7.5 kHz, respectively. With reference to figure 1, this dark rate level is higher with respect to CMOS technology processes optimized specifically for geiger mode avalanche structures at 0.35\,µm nodes [3]. However, geiger mode avalanche structures
obtained at 0.18 µm scale exhibit usually a dark rate higher than $10^4$ kHz/mm$^2$ [35, 36]. In [2] we obtained a SiPM based on the layout option of Structure I at GLOBALFOUNDRIES BCDLITE 0.18 µm CMOS node without MV option. We measured a dark rate of $20 \times 10^3$ kHz, which is comparable with the values obtained in this study. The MV option does not contribute to an improvement in the dark rate of the device obtained on the basis of Structure I.

A selection of the geiger mode avalanche structures obtained in CMOS processes are shown in the comparative table 1. Three variables are taken in consideration, namely the area of the device, the breakdown voltage and the dark rate at a given over-voltage. The breakdown voltage is typically decreasing when the scale decreases from 800 nm to 180 nm, due to the higher doping of the CMOS wells. However the recently reported structures obtained with the TSMC HV 180 µm CMOS technology [37] are designed using a combination of HV p-well and deep p-well, with a reduced doping concentration and a consequent breakdown voltage ranging between 49.9 V and 82.1 V. Similarly, the 350 nm CMOS node is characterized by a typically higher breakdown voltage, due to the recent development of specific masks suitable to geiger mode avalanche structures [3, 8, 33, 34]. The structures reported in this paper exhibit a breakdown voltage of approximately 12 V, which is well-proportioned to the typical values obtained both in similarly scaled technologies [1, 2].

The dark rate of the structures obtained in CMOS technology is typically higher than in dedicated commercially available custom technologies. Currently the best average dark rate ranging between 75 kHz/mm$^2$ and 200 kHz/mm$^2$ is obtained in the 350 nm CMOS node, using additional masks for the specific sensor implantation [3, 8]. The results obtained here for Structure IV represent an improvement, which follows a trend observed both at TSMC HV 180 µm CMOS technology [37] and at more scaled CMOS technology nodes [38–40].

As for the size of the sensors, a larger area implies clearly larger variation in the dark count rate. When comparing devices implemented in the same wafer, even with the same topologies, a difference in dark rate up to 4 order of magnitudes is possible, due to not-uniformities in the doping profile and to the presence of impurities. In comparison with other devices obtained in CMOS technology, the geiger mode avalanche structures proposed in this paper are designed with an area of 2500 µm$^2$, which is competitive with the results in other similarly scaled technologies.

4 Conclusions

We manufactured a geiger mode avalanche device in the 0.18 µm BCDlite GLOBALFOUNDRIES process with a dark rate down to $3 \times 10^3$ kHz/mm$^2$. We observe that the best layout technique for the reduction of the average dark rate in geiger mode avalanche structures is based on a low-doped p-type guard ring formed around the p$^+$ implantation. The wells are obtained in the standard CMOS process, without any modification of the doping profiles. The next step of this study is the characterization of the temperature dependence of the sensor performance, in order to quantify the tunneling contribution. Furthermore it is needed to improve the dark rate and the photon detection efficiency of the device [2], which is limited by the absence of an optical coupling in the adopted technology. The used CMOS process is suitable to an integrated development of sensors and readout electronics.
Table 1. Comparison of the results obtained in this paper, using a 180 nm MV GF BCDLite CMOS process (in bold), with a selection of geiger mode avalanche structures obtained with standard CMOS technologies.

| Techn. Pixel | Typical | Dark Count |
| node size | Operation | @typ. bias |
| [nm] | [μm²] | [V] | [kHz/mm²] |
| --- | --- | --- | --- |
| 800 [7] | 256 | $BV + 1.5$ | $100 \times 10^5$ |
| 800 [14] | 16–250 | $(19.5)_{BV} + 3$ | $3 \times 10^6$ |
| 800 [14] | 16–250 | $(17.5)_{BV} + 3$. | $4 \times 10^5$ |
| 800 [14] | 13 | $(19.5)_{BV} + 2$. | $3 \times 10^3$ |
| 500 [25] | 484 | $(16.7)_{BV} + 1.5$ | <120 |
| 350 [31] | 314 | $(18.9)_{BV} + 1.$ | $2 \times 10^4$ |
| 350 [34] | 2500 | $(25)_{BV} + 6.$ | $15 \times 10^6$ |
| 350 [33] | 38.5 | $(26)_{BV} + 3.$ | $1.19 \times 10^3$ |
| 350 [8] | 3185.47 | $(27.5)_{BV} + 3$ | 75-100 |
| 350 [3] | 2500 | $(25.8)_{BV} + 3.2$ | 200 |
| 180 [2] | 2500 | $(12)_{BV} + 2$ | $20 \times 10^3$ |
| 180 [1] | 154 | $(10.3)_{BV} + 0.95$ | $175 \times 10^3$ |
| 180 [37] | 314 | $(49.9)_{BV} + 5$ | 680 |
| 180 [37] | 314 | $(82.1)_{BV} + 5$ | $1.06 \times 10^3$ |
| **Structure I** | 2500 | $(12.6)_{BV} + 2.2$ | $2 \times 10^4$ |
| **Structure II** | 2500 | $(12.6)_{BV} + 2.2$ | $10^5$ |
| **Structure III** | 2500 | $(13.2)_{BV} + 2.2$ | $10^4$ |
| **Structure IV** | 2500 | $(13.2)_{BV} + 2.2$ | $3 \times 10^3$ |

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