Adaptive noise cancellation is an extensively researched area of signal processing. Many algorithms have been studied such as least mean square algorithm (LMS), recursive least square algorithm, and normalized LMS algorithm. The statistical characteristics of noise are fast in nature and the algorithms for noise cancellation should converge fast. Since LMS algorithm has slow convergence; in this paper, a variable leaky LMS (VLLMS) algorithm is explored. VLLMS is implemented using the concept of hardware-software cosimulation using Xilinx System Generator. The design is implemented on Virtex-6 ML605 field programmable gate array board. The implemented design is tested for sinusoidal signal added with an additive white Gaussian noise. The design summary and the utilization summary are presented.

**Keywords:** Field programmable gate array, Noise cancellation, Adaptive filter, Variable leaky least mean square algorithm, System generator.

© 2017 The Authors. Published by Innovare Academic Sciences Pvt Ltd. This is an open access article under the CC BY license (http://creativecommons.org/licenses/by/4.0/) DOI: http://dx.doi.org/10.22159/ajpcr.2017.v10s1.19566
between 0 and 1/(N) (signal power), where N is the number of filter taps [12,15]. The LLLS algorithm was designed to alleviate the drifting problem of the LMS algorithm.

Max Kamenetsky and Bernard Widrow introduced new algorithm named VLLMS algorithm [12] to give fast convergence compared to LLMS. The weight update coefficient for the algorithm is given by the equation (4),

\[ w_{k+1} = (1 - 2\mu_k \gamma_k)w_k + 2\mu_k \epsilon_k \hat{y}_k \]  

(4)

Where, \( \epsilon_k = Y_k - \hat{Y}_k \)

Step size \( \mu_k \) is varied for better convergence of the VLLMS algorithm in the presence of noise and \( \gamma_k \) is the leak factor which is a time-varying parameter.

\[ \mu_{k+1} = \mu_k + \gamma R_k^2 \]  

(6)

Where, \( R_k \) is the autocorrelation of \( \epsilon_k \) and \( \epsilon_{k-1} \) and it is calculated as given by equation (7),

\[ R_k = \rho R_{k-1} + (1-\rho)\epsilon_k \epsilon_{k-1} \]  

(7)

Where, \( \rho \) the weighting parameter and it takes values between 0 and 1. \( \gamma_k \) takes value between 0 and 1 and it controls the convergence time [15] and it can be adjusted as given by the equation (8),

\[ \gamma_{k+1} = \gamma_k - 2\mu_k \rho \epsilon_k \hat{Y}_k w_{k-1} \]  

(8)

After updating the leakage factor, an error signal is calculated and filter weights are adjusted accordingly.

**DESIGN AND IMPLEMENTATION**

FDA tool is the important tool of MATLAB which is used to design the filter of required specification. There are different responses (i.e., high pass, low pass, band pass, band stop, differentiator, integrator, etc.) and design method (i.e., IIR, finite impulse response [FIR]) for implementing the filter. By placing the filter order, frequency specifications and magnitude specifications, Filter can be customized. Tools create coefficients in the MATLAB workspace in matrix form through the specifications provided.

The VLLMS algorithm is implemented using digital filter in FPGA. Initially, the linear FIR filter is designed using FDA tool as shown in the Fig. 2 with 3 coefficients cutoff frequency of 300-450 kHz, sampling frequency of 1.5 MHz.

The architecture chosen is direct form FIR filter. The designed FIR filter coefficients are exported to Simulink workspace.

The Xilinx System Generator (XSG) is a high-level design tool which enables the prototype developer to design high-performance DSP systems using FPGAs.

The XSG tool enables us to integrate Xilinx with Simulink, it creates a. ise file which is used in Xilinx using the model file of Simulink. Xilinx block sets work only in the gateway blocks, i.e., gateway-in and gateway-out. Any sample-based input is given to the gateway-in block, the output can be seen on the scope by passing through the gateway out block.

First LMS algorithm based adaptive filter is designed in Simulink as shown in Fig. 3.

Then, the selected adaptive VLLMS is chosen for implementation for this research work. The VLLMS adaptive filter is implemented using system generator. The Simulink model for the same is presented in Fig. 4.

The Simulink model uses Simulink block:
- Gateway in: This block converts the Simulink inputs of integer, double, and fixed point to Xilinx fixed point type of specified bit size.
- Gateway out: This block converts fixed point inputs from the Xilinx blocks to Simulink block outputs of integer, double, or fixed point.
- Other Simulink blocks are basic adder, multipliers, and delay that are used to make the filter.

The designed VLLMS is 3-Tap FIR filter with an adaptive algorithm of VLLMS. The initial filter coefficients are designed using FDA tool for a band pass filter of 300-450 kHz with a sampling frequency of 1500 kHz. The leak factor considered for this paper is 0.8. The convergence \( \mu \) factor considered for this paper is 0.2. The design contains 9 multipliers, 8 adders, and 10 delay blocks.
RESULTS
Initially, the LMS algorithm is implemented using system generator blocks. The noisy input signal as shown in Fig. 5 is applied to designed LMS block.

The filtered output is shown in Fig. 6, the register-transfer level (RTL) schematic of the respective LMS-FIR filter design is shown in Fig. 7.

The VLLMS algorithm is implemented using Virtex-6 ML605 FPGA board. The adaptive filter is evaluated for the noisy input signal as shown in Fig. 8.

The steady state mean square error $e(n)$ is shown in Fig. 9 for the noisy input as shown in Fig. 8.

The RTL schematic of VLLMS adaptive filter is shown in Fig. 10.

The device utilization summary of LMS adaptive filter is given in Table 1. Here, it can be seen that the proposed algorithm is area efficient since the number of slice registers used is 1 out of 54576. The combinational path delay found here is 1.222 ns. The algorithm is found to be area efficient as shown in Table 1.

CONCLUSION
Adaptive noise cancellation is one of the research areas of adaptive filter applications. Adaptive noise cancellations find its application

Fig. 4: Simulink model of variable leaky least mean square adaptive filter

Fig. 5: Noisy input signal

Fig. 6: Filtered output

Fig. 7: Register-transfer level schematic of least mean square adaptive filter

Fig. 8: Noisy input for variable leaky least mean square algorithm

Fig. 9: Mean square error for first iteration

Fig. 10: Register-transfer level schematic of variable leaky least mean square adaptive filter
cockpit control and speech signal. In this research work, LMS algorithm is implemented using system generator. Further, VLLMS algorithm is chosen for implementation because of its fast convergence compared to LMS algorithm. This design is tested for sinusoidal signal added with additive noise (additive white Gaussian noise) on Virtex6 ML605 FPGA board. It is observed that the number of slice registers used is 1 among 54,576 and the area utilized for it is 0% compared to other algorithms. The number of fully used LUTs is 0%. This VLLMS algorithm method is area efficient and the system generator is used for interfacing Simulink blocks and Xilinx blocks. In the future, implementation of VLLMS algorithm explored various digital filter architectures such as parallel FIR filter to further minimize the convergence time.

REFERENCES

1. Subbareddy TV, Reddy SO, Kaushik CS, Elamaran V. Implementation of adaptive filters on TMS320C6713 using LabVIEW – A case study. Indian J Sci Technol 2015;8(22):1-6.
2. Broujeny BF. Adaptive Filter Theory and Application. Chichester, England: National University of Singapore, John Wiley and Sons Ltd.; p. 1998-7.
3. Honade SJ. Review Paper on Adaptive Filters Using VLSI. 2016. p. 1374-8.
4. SyuD, Syu S, Ruan S, Huang Y, Yang C. FPGA Implementation of Automatic Speech Recognition System in a Car. 2015. p. 485-6.
5. Mugdha AC, Rawnaque FS, Ahmed MU. Filter algorithm in noise removal from ECG signals. Informatics, Electronics and Vision (ICIEV), 2015 International Conference. 2015. p. 1-6.
6. Safarian C, Ogunfunmi T, Kozacky WJ. FPGA Implementation of LMS-Based FIR Adaptive Filter for Real Time Digital Signal Processing Applications. 2015. p. 1251-5.
7. Ajiaiah HB, Hunagund PV, Rao BR. Adaptive Filters in Digital Transmission Based on Improved LMS Algorithm. Wireless Communications, Signal Processing and Networking (WSPNET), International Conference. 2016. p. 23-5.
8. Deb A, Kar A, Chandra M. Advanced linear adaptive filtering methods for active noise control: A technical survey. ICACCS 2015 - Proceeding 2nd International Conference Advance Computing Communication System. 2015. p. 3-7.
9. Pujari SS. Design and Implementation of Single Order LMS based Adaptive System Identification on Altera based Cyclone II FPGA. 2014. p. 1605-9.
10. Dong X, Li H, Wang Y. High-speed FPGA Implementation of an Improved LMS Algorithm. No. 61371184. p. 342-5.
11. Bhoyar DB, Dethe CG, Bera S, Mushrif MM. FPGA Implementation of Adaptive Filter for Noise Cancellation. Electronics and Communication Systems (ICECS), International Conference; 2014.
12. Kamenetsky M, Widrow B. A Variable Leaky LMS Adaptive Algorithm. Signals, Systems and Computers, Conference Record of the Thirty-Eighth Asilomar Conference; 2004.
13. Widrow B, Stearns SD. Adaptive Signal Processing. NJ: Prentice Hall; 1985.
14. Nagal R, Kumar P, Bansal P. Performance Analysis of Least Mean Square Algorithm for Different Step Size Parameters with Different Filter Order and Iterations. International Conference on Recent Developments in Control, Automation and Power Engineering (RDCAPE); 2015.
15. Gwadabe TR, Salman MS, Abuhilal H. A modified leaky-LMS algorithm. Int J Comput Electr Eng 2014;6(3):222-5.