Abstract—We introduce a mathematical framework for simulating Hybrid Boolean Network (HBN) Physically Unclonable Functions (PUFs, HBN-PUFs). We verify that the model is able to reproduce the experimentally observed PUF statistics for uniqueness \(\mu\text{Unique}\) and reliability \(\mu\text{Rel}\), obtained from experiments of HBN-PUFs on Cyclone V FPGAs. Our results suggest that the HBN-PUF is a true ‘strong’ PUF in the sense that its security properties depend exponentially on both the manufacturing variation and the challenge-response space. Our Python simulation methods are open-source and available at https://github.com/Noeloikeau/networkm.

Index Terms—Hybrid Boolean Network (HBN), Physically Unclonable Function (PUF), Field Programmable Gate Array (FPGA)

I. INTRODUCTION

Boolean networks (BNs) \(^1\) are connected systems of discrete nodes that exhibit logic-like behavior. They have been used to model gene regulation, design new digital circuits, and have even been studied as a toy model of the human brain. Here, we develop mathematical tools to study a class of BNs that are both challenging to measure experimentally, and useful as cryptography primitives known as Physically Unclonable Functions (PUFs). Specifically we model ultra-fast chaotic circuits known as Hybrid Boolean Networks (HBNs) implemented on Field-Programmable Gate Arrays (FPGAs).

In this context, the nodes of the network are FPGA logic elements, and the edges connecting them are routing resources that conduct the electrical signals representing the analog value of each node state. Unlike standard synchronous designs, nodes exchange signals and perform logical operations continuously - without the control of a global clock or input from the user. Each BN is therefore an autonomous, recurrent electrical circuit that self-oscillates, typically at the maximum frequency allowed by the hardware, which is in the GHz regime for a Cyclone V FPGA. In practice, a clock is used to set the initial state of the system, forming a BN that is a ‘hybrid’ of autonomous and synchronous components (HBN).

These ultra-fast self-oscillations lead to a significant source of entropy generation in HBNs with nonlinear node functions, such as the exclusive-or (XOR) operation. The XOR function is maximally sensitive to individual bit flips, and hence a network of XOR gates can amplify the diverging effects of these bit flips exponentially over time. Thus, chaos has been observed in XOR-HBNs with as little as a single node having two self-loops \(^3\), and more robustly in a system of three nodes \(^4\). Chaos is consistently observed above 8 nodes, and 16-node XOR-HBNs have been used as true random number generators with a 12.8 Gbit/s entropy rate \(^5\).

Recently, XOR-HBNs have been used to develop PUFs on FPGAs \(^6\). PUFs act as ‘digital fingerprints’ by transforming stable environmental information into digital codes used for hardware identification \(^7\). The atomic-scale manufacturing variations present in the physical properties of FPGA logic elements and wires (such as impedance and length) are amplified and transformed into bits by the dynamics of the HBN. Given an \(N\)-bit initial condition or \textit{challenge} specifying the binary state of each labeled node in the HBN \textit{class}, the resulting \textit{final state} or \textit{response} can be used to uniquely identify the individual FPGA or \textit{instance} that created it. A large number of challenge-response pairs (CRPs) is guaranteed, as there are \(2^N\) possible \(N\)-bit responses for each of the \(2^N\) challenges. As a result, the entropy of HBN-PUFs scales super-exponentially with network size, a characteristic of a ‘strong’ PUF.

Due to their super-exponential entropy scaling and sub-nanosecond dynamics, HBN-PUFs stress existing methods of measurement and analysis. Additionally, the FPGA prevents analog readout of the waveform for each node because their primary use is as a digital device. This characteristic significantly limits the amount of information available from experiments. Hence, a model bypassing these limitations is useful for analyzing and certifying the HBN-PUF as an entropy source.

Current HBN models only consider a subset of the realistic experimental conditions present on FPGAs - namely noise on the signal, time-delays on the wires, and differences in logic operation time \(^8\). Each of these prior works on HBNs have emphasized the importance of variations to

1^{st} Noeloikeau Charlot
Physics Department
Ohio State University
Columbus, OH, USA
charlot.5@osu.edu

2^{nd} Daniel J. Gauthier
Physics Department
Ohio State University
Columbus, OH, USA
gauthier.51@osu.edu

3^{rd} Daniel Canaday
Potomac Research, LLC
Alexandria, VA, USA
daniel@potomacresear.ch

4^{th} Andrew Pomerance
Potomac Research, LLC
Alexandria, VA, USA
andrew@potomacresear.ch

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these parameters on the resulting dynamics. Here, we develop a mathematical model connecting these parameter variations to the PUF statistics. Specifically, we extend the Glass model [9] to include time-delayed signals [10], noise, and inhomogeneous time-constants. Our unique contributions follow.

- We introduce a mathematical model and Python library for simulating delay-differential network dynamics, specializing to HBN-PUFs on Cyclone V FPGAs. Drawing parameters randomly with means taken from the literature, we find that the model reproduces average experimental HBN-PUF uniqueness and reliability statistics.
- The model predicts that PUF uniqueness depends exponentially on the inter-die variation of the FPGA parameters, suggesting that the HBN-PUF is a true ‘strong’ PUF.

In Sec. II we introduce the HBN model and define the PUF statistics, then describe our simulation procedure. In Sec. III we simulate HBN-PUFs and compare our results to experimental data. We then use the model to estimate the functional form of the PUF statistics in terms of the amount of manufacturing variation and noise. Finally in Sec. IV we interpret our results in the context of future work and conclude.

II. MODELING FRAMEWORK

We model HBN dynamics as a set of coupled first-order time-delay differential equations with noise, governing the node states $x_n \in [0, 1]$ for each of the $N$ nodes in the network. This is summarized in Fig. 1. Each node $n$ executes a logic function $f_n$ on the states of its neighbors $y_n$. These neighbor states are time-delayed by $\Delta_{nm}$, representing the finite propagation time required for the state of node $m$ to reach node $n$. These time-delayed signals are also rounded toward 0 or 1, as in hardware logic gates, which convert the incoming analog voltages into binary values. Mathematically,

$$\tau_n \frac{dx_n}{dt} = -x_n(t) + f_n(y_n(t)) + \epsilon_n(t), \quad (1)$$

$$y_n(t) = \{X_m(t - \Delta_{nm})\}_{m \in \text{pred}(n)}, \quad (2)$$

where $X_m(t) = \Theta(x_m(t) - 0.5)$ is the Boolean state and $\Theta$ is the Heaviside step function, and pred($n$) are the predecessors or fixed set of nodes with an edge directed toward node $n$. The characteristic timescale $\tau_n$ determines the time required for the node to transition from logic low to logic high or vice-versa, also known as its rise and fall times, respectively. Thermal/charge fluctuations are modeled as Gaussian noise $\epsilon_n(t) \sim N(0, \sigma^2)$ drawn randomly with zero mean and standard deviation $\sigma$ at each time-step.

We integrate Eq. (1) using a first-order Euler method mapping the state from time $t$ to $t + dt$, given by

$$x_n(t + dt) = x_n(t) + \frac{dt}{\tau_n} \left[-x_n(t) + f_n(y_n(t)) + \epsilon_n(t)\right], \quad (3)$$

where all times and delays are integer multiples of $dt$. The optimal PUF read-out time resides in the transient and is within an order-of-magnitude of the node timescale. Therefore, we integrate for only $\sim 10^3 \tau$, and error accumulation due to the first-order approximation is negligible over this interval. Here, $\tau = (1/N) \sum_n \tau_n$ is the mean node time constant.

\[ \bar{\tau} = 1/N \sum_n \tau_n \]

We express all future parameters in units of $\bar{\tau} = 0.25$ ns, a value typical of Cyclone V FPGA logic elements [11].

In an actual FPGA, multiplexers are used to set the initial condition of each node in the network as shown in the top right panel of Fig. 1. These multiplexers are held fixed to the challenge for several thousand ns. During this time, the autonomous portion of the network (the XOR gates) stabilizes and synchronously evaluates the challenge $x(0)$. Thus, the initial output of each multiplexer $n$ is $f_n(y_n(0))$ (the node function evaluated over its input challenge bits). Experimentally, this is the first value observed in memory.

We observe that simulations explicitly modeling these multiplexers reproduce this behavior. Crucially, we observe that these more complex models produce nearly identical PUF statistics to the simpler models which omit multiplexers but account for this change in initial conditions. Therefore, we omit modeling multiplexers explicitly, and instead use $f_n(y_n(0))$ as the initial condition for each node in the simulation.

HBN-PUF challenge-response pairs (CRPs) are multidimensional arrays having indices summarized in Table II. Classes $s$ are characterized by a particular network topology and set of parameters, representing the circuit netlist instantiated on FPGAs. Instances $i$ of a class are characterized by a uniformly random perturbation of that class’s parameters, representing the manufacturing variations present in each FPGA’s physical structure. Challenges $c$ are the binary vectors specifying the initial condition of an HBN-PUF instance. Each integration $r$ of an initial condition is characterized by a different sequence of noise vectors randomly generated at each timestep. Each node $n$ then responds with a Boolean state at time $t$. We label this data as $X_{n,i,c,r}(t) \in \{0, 1\}^{N_s \times N_c \times N_x \times N_x \times T}$.

The PUF uniqueness and reliability statistics $\mu_{inter}$ and $\mu_{intra}$ are averaged pairwise differences between responses.
TABLE I
HBN-PUF CHALLENGE-RESPONSE PAIR (CRP) INDICES.

| Index | Symbol | Description |
|-------|--------|-------------|
| Class | \( s \leq N_s = 15 \) | Circuit netlist/mean values of \( \tau, \Delta \) |
| Instance | \( t \leq N_t = 8 \) | Individual FPGA/exact values of \( \tau, \Delta \) |
| Challenge | \( c \leq N_c = 1000 \) | Initial condition \( x(0) \) |
| Repeat | \( r \leq N_r = 100 \) | Random noise vector \( \epsilon(t) \) |
| Node | \( n \leq N = 256 \) | Single bit of \( X(t) \) |
| Time | \( t \leq T = 20 \) | Register in memory. |

Uniqueness measures the average difference between responses of separate instances to the same challenge. It arises due to manufacturing variations, and ideally \( \mu_{\text{inter}} = 0.5 \). Reliability measures the average difference between responses of the same instance to the same challenge. It arises due to noise, and \( \mu_{\text{intra}} = 0 \) in the ideal noise-free case (\( \epsilon = 0 \)). Let angle brackets denote averages \( \langle X_j \rangle_j = (1/N_j) \sum X_j \), and pairs of indices denote average Hamming distances \( \langle X_j \rangle_{j-j'} = [N_j(N_j + 1)/2]^{-1} \sum_{j<j'} [X_j - X_{j'}] \). Then,

\[
\mu^s_{\text{inter}}(t) = \langle X^s_{i,c,r,n}(t) \rangle_{i-i'},c,r,n
\]

(4)

\[
\mu^s_{\text{intra}}(t) = \langle X^s_{i,c,r,n}(t) \rangle_{i,c,r-r',n}
\]

(5)

For each class there exists an optimal time \( t^s_{\text{opt}} \) to select the response from the network timeseries. This is when the network has coupled enough to the chip manufacturing variation to be unique, while remaining unaffected enough by noise to be reliable. Mathematically \( t^s_{\text{opt}} \) is the point maximizing the difference between the statistics

\[
\Delta \mu^s(t) := \mu^s_{\text{inter}}(t) - \mu^s_{\text{intra}}(t),
\]

(6)

\[
t^s_{\text{opt}} := \arg \max_{t \leq T} (\Delta \mu^s(t)).
\]

(7)

Typically, the class index \( s \) is suppressed, as one is dealing with a single PUF class. However, here we will perform an average over classes, representing the typical statistics of a random network ensemble. In these cases an omission of \( s \) indicates an average over classes, i.e., \( \mu = (1/N_s) \sum \mu^s \).

Simulated HBN-PUF statistics are procedurally generated in the following order: 1. class, 2. instance, 3. CRP. In the first step, class generation, an \( N \)-node network is drawn from the set of all random regular graphs of degree 3. The delay along each edge is drawn from the Uniform Random distribution over the interval \( \Delta t \) nm \( \sim U(0, 10 \bar{\tau}) \). These edge delays represent the location assignment given by the FPGA compiler, which we find can vary from near-zero to several ns depending on the design and routing congestion.

The second step, instance generation, slightly adjusts the parameters of a given class. The node time-constants are \( \tau_{i,n} \sim N(\bar{\tau}, \sigma^2) \), where \( N \) is the Normal distribution with mean \( \bar{\tau} = 0.25 \) ns and standard deviation \( \sigma \). The positive-definite time-delays of instance \( i \) are given by \( \Delta t_{nm} \sim N(\Delta t_{nm}, \sigma^2) \). We interpret \( \sigma \) as a uniform manufacturing variation on all FPGA components, and set \( \sigma = 0.05 \) unless otherwise noted, a value typical of modern FPGAs [12].

The final step, CRP generation, integrates Eqs. [13] to predict the dynamics of the network and formats this data to match the experiment. The integration time \( T_{\text{int}} = 42 \bar{\tau} = 10.5 \) ns and timestep \( dt = \bar{\tau}/25 = 0.01 \) ns are fixed for all simulations. The noise amplitude is fixed to the timestep error \( \epsilon = 0.01 \) unless otherwise noted. For each class, instance, and challenge, Eqs. [3] is integrated \( N_r \) times using the corresponding parameters. Each integration differs by the unique noise vector drawn as \( \epsilon(t) \sim N(0, \sigma^2) \). The resulting timeseries is then decimated to match the measurement interval of the experimental data, which is \( 2 \bar{\tau} = 0.5 \) ns. The first \( 2 \bar{\tau} \) are discarded as they are not observable in experiment, resulting in 20 evenly spaced times over 10 ns from which Eqs. [47] are calculated.

III. RESULTS

Figure 2 displays a comparison between actual HBN-PUF experiments on Cyclone V FPGAs (top row) and our model statistics (bottom row). We stress that no attempt is made to fit the parameters of the model to match the experimental data. Nevertheless, the null hypothesis - that the model does not predict the experiment - should be rejected, due to an RMS Z-score \( Z_{\text{RMS}} = \sqrt{ \langle Z(t)^2 \rangle_t } = 0.59 \leq 2.33 \), where \( Z(t) = \mu_{\text{exp}}^s(t) - \mu_{\text{sim}}^s(t) \) \( \sim 1 \forall t \) and \( \text{std.} \) are the standard deviations of the \( \mu^s(t) \). In other words, to within 72% probability (integrated PDF), the ensemble averages of the model and the experiment can be drawn from the same normal distribution. Additionally, the limiting behavior and curvature of both statistics match, demonstrating that the model can be used to make asymptotic predictions about HBN-PUFs.
arising from skew on the FPGA clock fabric and registers, jitter on the external crystal oscillator, and correlated delays in the routing, none of which we account for in our random parameter draws. All of these factors contribute to the kinks in the experimental curves largely absent in the model. An understanding of these instance-level temporal correlations requires ps-scale intra-FPGA measurement tools such as a waveform capture device [11]. Measuring individual $\Delta_{\text{min}}, \tau_{n}$ and calibrating the model is the subject of future work.

Next, we determine the extent to which the HBN-PUF model scales with manufacturing variation and noise, and how this information quantifies the PUF strength. To this end, we calculate the statistics $\mu_{\text{inter}}$ and $\mu_{\text{intra}}$ as a function of $\sigma$ and $\varepsilon$ by fixing the observed optimal response time $t_{\text{opt}} = 6$ ns. These data are shown in Figure 3.

In both cases, the data are well fit to a saturating exponential function. This provides mathematical evidence suggesting that the HBN-PUF is truly ‘strong’. This is because, in addition to having an entropy that scales super-exponentially with $N$, the HBN-PUF uniqueness statistic $\mu_{\text{inter}}$ scales exponentially with the inter-die manufacturing standard deviation $\sigma$. Furthermore, the exponential rate constant $C$ fit to $\mu_{\text{inter}}(\sigma)$ is roughly three times that of $\mu_{\text{intra}}(\varepsilon)$. This demonstrates that the nonlinear dynamics amplify manufacturing variations to a greater degree than noise, ensuring effective HBN-PUF behavior. Additionally, exponential scaling of $\mu_{\text{inter}}(\sigma)$ indicates that small uncertainties in the system parameters result in large deviations of the modeled response. Log-$\sigma$ simulations (not shown) demonstrate that this uncertainty conservatively approaches the observed noise floor at $\sigma_{\text{min}} = 10^{-3}$, i.e. $\mu_{\text{inter}}(\sigma_{\text{min}}, \varepsilon = 0.01) \approx \mu_{\text{intra}}(\sigma = 0.05, \varepsilon = 0.01)$. We therefore estimate that the dynamics of each node and edge in the HBN-PUF must be resolved to $\sigma_{\text{min}}^{T} \approx 10^{-3}$ s (sub-ps-scale) precision in order for a modeling attack to be feasible. FPGA clock fabrics routinely require ns-scale skew for large recurrent networks like the HBN. However, small, carefully placed networks may be measurable to ps-scale and below over short time periods, and this is the subject of future research.

IV. CONCLUSIONS AND FUTURE WORK

In summary, we accurately predict the class-averaged experimental statistics of HBN-PUFs using stochastic first-order time-delay differential equations and parameter values drawn randomly from the literature. These simulations predict that HBN-PUFs are exponentially sensitive to manufacturing variations to a greater degree than noise. In conjunction with the exponential entropy scaling, our results suggest that the HBN-PUF is a true ‘strong’ PUF. The introduced simulation library supports arbitrary network topologies and logical functions, and in the future we will combine it with 5-ps-resolution experimental measurements using a waveform capture device on the Cyclone V [11]. These measurements will be used to test the predicted sub-ps uncertainty bound required for a modeling attack. We will also present novel theoretical metrics analyzing strong PUF properties, specifically unclonability, entropy, and multidimensional chaos.

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