A New Transformerless Ultra High Gain DC–DC Converter for DC Microgrid Application

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ABSTRACT High gain dc-dc converters are used in several applications which include solar photovoltaic system, switch-mode power supplies and fuel cells. In this paper, an ultra-high gain dc-dc boost converter is proposed and analyzed in detail. The converter has a gain of six times as compared with the boost converter. The high gain is achieved by utilizing switched inductors and switched capacitors. A modified voltage multiplier cell (VMC) with switched inductors is proposed. The converter has a single switch which makes its operation easy. Moreover, the voltage across the switch, diodes and capacitors are less than the output voltage which increases the overall efficiency of the converter. The converter performance in steady-state is analyzed in detail and it is compared with other latest high gain converters. The working of the converter in non-ideal conditions is also discussed in detail. The loss analysis is done using PLECS software by incorporating the real models of switches and diodes from the datasheet. To confirm and validate the working of the proposed converter a hardware prototype of 200 W is developed in the laboratory. The converter achieves high gain at low duty ratios and its performance is found to be good in open and closed loop conditions.

INDEX TERMS Boost converter, DC microgrid, duty cycle, ultra high gain, voltage stress.
Non-isolated converters are favoured where isolation of input from output is not required. They can be classified as coupled and non-coupled types [7]. The coupled inductor topologies can produce very high voltage gain with low stress on the semiconductor switch but the problems with leakage inductance can result in large voltage spikes across the switch for which a clamped circuit needs to be designed.

To achieve a high gain capacitor-diode voltage multiplier cell and cascading of two or more converters is employed. Several new and modified topologies use voltage multiplier circuit (VMC) made of switched capacitors and inductors to increase the gain of the converter. The quadratic boost (QBC) and cubic boost topologies can produce high gain at low duty cycles with reduced stress on switching devices [8]–[10] but at higher duty ratios the efficiency may decrease with an increase in current. Further, the inductor core is more prone to enter saturation at higher duty cycles. In [11] a new quadratic boost converter is proposed with lower inductor current ripple and low stress across the switch. Another class of high gain boost converter is a quasi-z-source or z-source converter that is used to increase the gain of the converter where the inductor is replaced by an impedance network but these converters have a restricted duty cycle [12], [13] operation. Interleaved boost converters are being used to acquire high output voltage and high efficiency [14] with a lesser number of switches. In a multiphase interleaved converter is introduced along with a z-source network to achieve high gain. The input current ripple is low therefore there the need for an input filter does not arise. The problem with interleaved converters is that a voltage boost circuit is needed at the end to increase the gain [15] of the converter. Several new converter topologies have been discussed in [16] with the well-known Cockcroft-Walton voltage multiplier cell. A new single-ended primary inductor converter (SEPIC) is presented in [17] with a single switch is used to achieve high gain. Another new SEPIC converter with both buck and boost topology is presented in [18]. Single input multipoint output is a good way of getting different output voltage using a single input. These converters have better voltage regulation capability and low stress across the output capacitor as compared to single input [19], [20] single-output (SISO) converter. They can be used as individual SISO converters.

A quadratic boost converter is proposed by using the voltage lift technique (VL) in [21]. In [22] VL technique is used to get desired value of gain but the converter utilizes two switches that are switched alternately. A hybrid converter based on voltage multiplier cell (VMC) and switched capacitor cells with high gain is presented in [23]. It overcomes shortcomings such as high voltage and current stress on the power devices. A converter with a similar gain is presented by authors in [24] but the stress on two switches is different and it uses the diode voltage capacitor multiplier and switched inductor voltage multiplier to achieve high gain. A high step-down interleaver is presented in [25] using a similar concept of switched/series capacitor using six switches. A novel switched impedance network-based converter is presented in [26]. It utilizes a voltage doubler-switched capacitor network to achieve higher gain at lower duty ratios. A multistage structure can significantly increase the gain but efficiency can be low due to a greater number of components. A hybrid zeta boost converter with a switched inductor is proposed in [27] but its voltage gain is not very high. A new transformerless active switched network is presented in [28] by using two switches but the gain achieved is lower than the proposed topology in this paper. A switched capacitor network-based topology is presented in the paper [29]. In [30] the switched inductor topology has used two inductor and two switches but the voltage gain is not very high. A modified SEPIC converter is presented in [32] to achieve high voltage gain. In [34] the converter uses parallel input and series output (PISO) technique to increase voltage gain. Furthermore, the stress voltage of switches and diodes has been reduced.

In this article, the proposed high gain converter has a VMC made up of switched inductors. A combination of switched capacitors and VMC achieves ultra-high gain with only one switch and two inductors. High gain topologies proposed in [28]–[31] utilize two switches and have much less voltage gain as compared with the proposed converter in this paper. The attractive features of the proposed converter are:

- The converter achieves a voltage conversion ratio of six times that of the conventional boost converter.
- The converter uses a single switch that has low voltage stress i.e. one-third of output voltage.
- A coupled inductor is not used so the problem of leakage inductance is avoided.
- The voltage stress on all the semiconductor devices is equal. The devices with a uniform rating and low internal resistance can be used.

The paper discusses the structure and principle of operation of the converter in section II. Steady-state operation of the proposed converter in the continuous and discontinuous mode of operation is presented in section III and IV respectively. In section V and VI non-ideal gain analysis
and comparative study of the proposed structure is presented respectively. Experimental results and efficiency of the converter are shown in section VII. In section VIII conclusion is presented.

II. OPERATING PRINCIPLE OF PROPOSED CONVERTER (SC-SL-DC)

A. CIRCUIT DESCRIPTION

The proposed dc-dc converter topology is presented in Figure 2. The converter consists of a single switch (S), two inductors (L₁ and L₂), seven diodes (D₁, D₂, ..., D₇) and six capacitors including one capacitor C₀ as an output filter which filters the output pulsating current and provide a smoothed output voltage. The combination of (L₁, L₂, D₁, D₂ and C₁) is a modified switched capacitor cell while the
combination of \((C_1, D_1, C_3\) and \(D_4)\) is switched capacitor cell. Some important waveforms for the proposed converter are shown in Figure 3. All capacitors are sufficiently large, therefore the voltage across capacitors is assumed to be constant. And all components are assumed as ideal.

**B. MODES OF OPERATION**

This converter can be operated in both CCM and DCM modes of operation. The CCM operation of the proposed converter has two modes. In the first mode when the switch is conducting and the second one is analyzed when the switch is turned OFF. Analysis of the proposed converter for one switching period under CCM mode and in steady-state is as follows.

1) **MODE I: WHEN SWITCH IS ON \((0 < t < DT_S)\)**

Mode I of operation is shown in Figure 4(a). In this interval, the switch is turned ON and the diodes \(D_2, D_3, D_5\) and \(D_7\) are forward biased. The voltage across inductors \(L_1\) and \(L_2\) is equal to the input voltage \((V_{in})\) by which they are magnetized and therefore, inductor currents \(I_{L1}\) and \(I_{L2}\) increase linearly. In this mode, Capacitor \(C_1\) discharges and transfer its energy through capacitor \(C_3\) and load. During this interval, \(C_2\) and \(C_3\) discharge through \(L_2\) and \(C_4\). Thus, related equations can be drawn out as follows:

The voltage across inductors appears as shown (1)

\[
\begin{align*}
V_{L1} &= L_1 \frac{dI_{L1}}{dt} = V_{in} \\
V_{L2} &= L_2 \frac{dI_{L2}}{dt} = V_{in}
\end{align*}
\]

(1)

The voltage across capacitors is derived from Figure 4(a) using KVL and KCL as follows:

\[
\begin{align*}
V_{C2} &= -V_{in} \\
V_{C4} + V_{C5} &= V_o \\
V_{C3} &= V_{in} - V_{C3}
\end{align*}
\]

(2)

Current relations through capacitors, inductors, diodes and switch can be estimated as follows:

\[
\begin{align*}
C_1 \frac{dV_{C1}}{dt} &= I_{C1} = I_{in} - I_{L1} - I_{D3} \\
C_2 \frac{dV_{C2}}{dt} &= I_{C2} = I_{L1} - I_{D2} \\
C_3 \frac{dV_{C3}}{dt} &= I_{C3} = I_{L2} + I_{D2} - I_{S} \\
C_4 \frac{dV_{C4}}{dt} &= I_{D5} \\
C_0 \frac{dV_{C0}}{dt} &= I_{C0} = I_{C5} - I_{o}
\end{align*}
\]

(3)

**C. MODE II: WHEN SWITCH IS OFF \((DT_S < t < T_S)\)**

In this interval, the switch is turned OFF and the diodes \(D_1, D_4\) and \(D_6\) are forward biased and the other three diodes are reversed biased. The circuit diagram is shown in Figure 4(b). During this interval, \(V_{in}\) charges \(C_1\) and \(L_1\) charges \(C_2\). Inductor \(L_2\) transfer its stored energy to \(C_3\). Output capacitor \(C_0\) transfer its energy to load \(R\).

Using KVL and KCL in mode II, the voltage across inductors come out as follows:

\[
V_{L1} + V_{L2} = L_1 \frac{dI_{L1}}{dt} + L_2 \frac{dI_{L2}}{dt} = V_{in} - V_{C2} - V_{C3} \quad (4)
\]

In (2), it is derived that

\[
V_{C2} = -V_{in}
\]

Equation (4) can now be written as

\[
V_{L1} + V_{L2} = 2V_{in} - V_{C3} \quad (5)
\]

The voltage across the capacitors can be written by applying KVL in Figure 4(b)

\[
\begin{align*}
V_{C4} - V_{C5} &= V_{C3} \\
V_{C3} - V_{C1} &= V_{in}
\end{align*}
\]

(6)

Current passing through capacitors relations can be shown as follows:

\[
\begin{align*}
C_1 \frac{dV_{C1}}{dt} &= I_{C1} = I_{in} - I_{L1} \\
C_2 \frac{dV_{C2}}{dt} &= I_{C2} = I_{L1} - I_{L2} \\
C_3 \frac{dV_{C3}}{dt} &= I_{C3} = I_{L2} - I_{D1} \\
C_4 \frac{dV_{C4}}{dt} &= I_{C4} = I_{C5} = I_{C1} - I_{D1} \\
C_0 \frac{dV_{C0}}{dt} &= I_{C0} = -I_{o}
\end{align*}
\]

III. **STEADY STATE ANALYSIS IN CCM**

**A. CALCULATION OF CAPACITOR VOLTAGES AND VOLTAGE GAIN**

Applying the principle of volt-second balance on inductors \(L_1\) and \(L_2\) and using (1), (2), (4) and (6) the voltage conversion ratio, \(M\) can be derived as shown.

\[
\int_0^{DT_S} (V_{L1} + V_{L2}) dt + \int_{DT_S}^{T_S} (V_{L1} + V_{L2}) dt = 0
\]

where, \(T_S\) is switching time period.

Using this equation following results can be drawn out as.

\[
2V_{in}D + (2V_{in} - V_{C3}) (1 - D) = 0
\]

(8)

It is clear from (8), that

\[
V_{C3} = \frac{2V_{in}}{(1 - D)} \quad (9)
\]

From (6) it can be written that

\[
V_{C4} - V_{C5} = V_{C3}
\]

Using (9) in (6) the following equation can be written

\[
V_{C4} - V_{C5} = \frac{2V_{in}}{(1 - D)} \quad (10)
\]

Again from (2)

\[
V_{C4} + V_{C5} = V_{o} \quad (11)
\]
From (19) and (17), it can be written down

\[
\begin{align*}
V_{C4} &= \frac{V_0}{2} + \frac{V_{in}}{(1 - D)} = \frac{2V_0}{3} \\
V_{C5} &= \frac{V_0}{2} - \frac{V_{in}}{(1 - D)} = \frac{V_o}{3}
\end{align*}
\]

(12)

From (2) again,

\[V_{C1} + V_{C5} + V_{C3} = V_o - V_{in}\]

(13)

Also, from (6)

\[V_{C1} = V_{C3} - V_{in}\]

(14)

Putting this value in equation (13), it can be shown that

\[V_{CS} + 2V_{C3} = V_o\]

(15)

Using (12) and (15), it can be drawn out easily.

\[V_{C3} = \frac{V_0}{4} + \frac{V_{in}}{2(1 - D)} = \frac{V_o}{3}\]

(16)

From (9) and (16), voltage gain is derived as,

\[M = \frac{V_0}{V_{in}} = \frac{6}{(1 - D)}\]

(17)

According to (17), it can be seen that the voltage gain of the proposed converter is six times higher than that of the conventional boost converter.

**B. VOLTAGE AND CURRENT STRESSES OF POWER DEVICES**

In Figure 4, by applying KVL the voltage appeared across the switch (V_{SW}), diodes (V_D) and capacitors (V_C) when they are not conducting, can be expressed as

\[
\begin{align*}
V_{SW} &= V_{C3} = \frac{V_0}{3}, \\
V_{D1} &= V_{C4} - V_{C3} = \frac{V_0}{3} \\
V_{D2} &= V_{D3} = \frac{V_0}{3}, \\
V_{D4} &= V_{C3} = \frac{V_0}{3} \\
V_{D5} &= V_{D6} = V_{C5} = \frac{2V_0}{3}, \\
V_{D7} &= V_{C3} - V_{C4} = \frac{V_0}{3}
\end{align*}
\]

(18)

The stress on different semiconductor devices is shown in Figure 9.

Assuming a lossless circuit, it can be written

\[P_{in} = P_{out} \Rightarrow V_{in}I_{in} = V_oI_o\]

(19)

where \(I_{in}\) and \(I_o\) are input and output currents respectively. From (19) and (17), it can be written down:

\[\frac{I_{in}}{I_o} = \frac{V_0}{V_{in}} = M = \frac{6}{(1 - D)}\]

(20)

From (20), dc input current can be calculated as,

\[I_{in} = \left(\frac{6}{1 - D}\right)I_o\]

(21a)

Applying the principle of current balance on the capacitors C1 and C2 and using (3) and (7) it can be written as:

\[\int_0^{DT_S} (I_{in} - I_{L1} - I_{D2}) dt + \int_{DT_S}^{T_S} (I_{in} - I_{L1}) dt = 0\]

\[\int_0^{DT_S} (I_{in} - I_{L1} - I_{D3}) dt + \int_{DT_S}^{T_S} (I_{in} - I_{L1}) dt = 0\]

(21b)

After solving the above equation, the average current through inductors can be found out as

\[I_{L1} = I_{L2} = I_L = \left(\frac{3}{1 - D}\right)I_o\]

(22)

The dc values of current through the semiconductor devices can be found as

\[
\begin{align*}
I_{SW} &= \frac{5 + D}{1 - D}I_o \\
I_{D1} &= I_{D2} = I_L = \left(\frac{3}{1 - D}\right)I_o \\
I_{D3} &= I_{D4} = I_{D5} = I_{D6} = I_{D7} = I_o
\end{align*}
\]

(23)

**C. SELECTION OF INDUCTORS AND CAPACITORS**

For a given suitable value of ripple of inductor currents \(\Delta I_{L1}\) and \(\Delta I_{L2}\) at a fixed value of switching frequency \(f_s\) for this converter, inductances can be extracted from (1) as:

\[
\begin{align*}
L_1 &= \frac{V_{in}D}{\Delta I_{L1}f_s} \\
L_2 &= \frac{V_{in}D}{\Delta I_{L2}f_s}
\end{align*}
\]

(24)

Moreover, within the valid range of voltage ripple, the value of capacitances can be calculated from
(3) and (7) as:

\[
\begin{align*}
C_1 &= \frac{3V_0}{\Delta V_{C1f_s}R}, \\
C_2 &= \frac{3V_0}{\Delta V_{C2f_s}R}, \\
C_3 &= \frac{2V_0}{\Delta V_{C1f_s}R}, \\
C_4 &= \frac{V_0}{\Delta V_{C3f_s}R}, \\
C_5 &= \frac{V_0}{\Delta V_{C4f_s}R}, \\
C_6 &= \frac{3V_0}{\Delta V_{C5f_s}R}, \\
C_7 &= \frac{V_0}{\Delta V_{C6f_s}R}.
\end{align*}
\]

To obtain the desired output voltage at the given input voltage, duty cycle \( D \) can be calculated. From (17), the duty cycle is:

\[
D = \frac{V_0 - 6V_{in}}{V_0}
\]

(26)

IV. EFFECT OF UNEQUAL INDUCTANCES ON VOLTAGE GAIN

The operation of the converter depends on the inductance values of inductor \( L_1 \) and \( L_2 \). The current through the inductor will have different slopes and it will change the current waveform of the inductor due to different values of inductances of \( L_1 \) and \( L_2 \).

A. IF INDUCTANCE VALUE \( L_1 \) IS LARGER THAN \( L_2 \)

The current waveform through the inductor \( L_1 \) and \( L_2 \) is shown in Figure 5. The converter SC-SL-DC is operated in three modes.

1) MODE I: WHEN SWITCH IS ON (0 < \( t < t_1 \))

The Switch is turned ON. This mode is same as Mode I and the equivalent circuit is shown in Figure 4(a). Diode \( D_1 \), \( D_4 \), \( D_5 \) are reverse biased while the diodes \( D_2 \), \( D_3 \), \( D_6 \) and \( D_7 \) are forward biased. The voltage across the inductors \( L_1 \) and \( L_2 \) is equal to input voltage by which they are magnetized and therefore, inductor currents \( I_{L1} \) and \( I_{L2} \) increase linearly with different slopes. The slope of inductor currents of \( L_1 \) and \( L_2 \) can be achieved as

\[
\begin{align*}
\frac{dI_{L1}}{dt} &= \frac{V_{in}}{L_1} \quad (27) \\
\frac{dI_{L2}}{dt} &= \frac{V_{in}}{L_2} \quad (28)
\end{align*}
\]

In this mode the current through \( L_1 \) is less than current through \( L_2 \) because the inductance value of \( L_1 \) is greater than \( L_2 \).

2) MODE II: WHEN SWITCH IS OFF (\( t_1 < t < t_2 \))

Switch is just turned OFF. This mode occurs for a very duration of \( \delta T_s \) as shown in Figure 5(a). The equivalent circuit in this mode is shown in Figure 5(b). Diode \( D_1 \), \( D_3 \), \( D_4 \) and \( D_6 \) are forward biased while the diodes \( D_2 \), \( D_5 \) and \( D_7 \) are reverse biased. Inductor current \( I_{L1} \) is smaller than \( I_{L2} \) as shown in Figure 5(a). The current through \( L_1 \) has positive slope and magnetizes in this period and the current \( L_2 \) has large negative slope and discharges in this period. The current through \( D_3 \) will be difference between inductor current \( I_{L2} \) and \( I_{L1} \).

The slope of inductor currents of \( L_1 \) and \( L_2 \) can be achieved as

\[
\begin{align*}
\frac{dI_{L1}}{dt} &= \frac{V_{C2}}{L_1} = \frac{V_{in}}{L_1} \quad (29) \\
\frac{dI_{L2}}{dt} &= \frac{V_{in} - V_{C3}}{L_2} \quad (30)
\end{align*}
\]

In this mode the current through \( L_1 \) is less than current through \( L_2 \) because the inductance value of \( L_1 \) is greater than \( L_2 \) and this mode ends when \( I_{L1} = I_{L2} \) and converter operates in Mode III.

3) MODE III: SWITCH IS OFF (\( t_2 < t < DT_s \))

Switch is OFF. The equivalent circuit is same as Mode II in CCM as shown in Figure 4(b). Diode \( D_1 \), \( D_4 \), \( D_6 \) are forward biased while the diodes \( D_2 \), \( D_3 \), \( D_5 \) and \( D_7 \) are reverse biased. The inductors \( L_1 \) and \( L_2 \) are in series and the current through inductors \( L_1 \) and \( L_2 \) are equal and demagnetize with equal negative slope which can be achieved as follows

\[
\begin{align*}
\frac{dI_{L1}}{dt} &= \frac{2V_{in} - V_{C3}}{L_1 + L_2} \quad (31) \\
\frac{dI_{L2}}{dt} &= \frac{2V_{in} - V_{C3}}{L_1 + L_2} \quad (32)
\end{align*}
\]

The average of voltage across the inductor is zero. Therefore,

\[
L_1 \rightarrow D (V_{in}) + \delta (V_{in}) + \frac{L_1 (2V_{in} - V_{C3})}{L_1 + L_2} \times (1 - D - \delta) = 0 \quad (33)
\]

\[
L_2 \rightarrow D (V_{in}) + \delta (V_{in} - V_{C3}) + \frac{L_2 (2V_{in} - V_{C3})}{L_1 + L_2} \times (1 - D - \delta) = 0 \quad (34)
\]

Also,

\[
V_{C3} = \frac{V_0}{3} \quad (35)
\]

On solving (33)-(35), the voltage gain of proposed converter SC-SL-DC can be obtained as

\[
\frac{V_0}{V_{in}} \bigg|_{L_1>L_2} = \frac{6}{(1-D)} \quad (36)
\]

The voltage gain is same as equation (17) but the average value of inductor current \( L_1 \) is less than inductor current \( L_2 \).

B. IF INDUCTANCE VALUE \( L_2 \) IS LARGER THAN \( L_1 \)

The current waveform through the inductor \( L_1 \) and \( L_2 \) is shown in Figure 6. The converter SC-SL-DC is operated in three modes as discussed below

1) MODE I: WHEN SWITCH IS ON (0 < \( t < t_1 \))

The Switch is turned ON. This mode is same as Mode I and the equivalent circuit is shown in Figure 4(a). Diode \( D_1 \), \( D_4 \), \( D_6 \) are reverse biased while the diodes \( D_2 \), \( D_3 \), \( D_5 \) and \( D_7 \) are forward biased. The voltage across the inductors \( L_1 \) and \( L_2 \) is equal to input voltage by which they are magnetized and therefore, inductor currents \( I_{L1} \) and \( I_{L2} \) increase linearly with...
different slopes. The slope of inductor currents of \( L_1 \) and \( L_2 \) can be achieved as

\[
\frac{dI_{L1}}{dt} = \frac{V_{in}}{L_1} \\
\frac{dI_{L2}}{dt} = \frac{V_{in}}{L_2}
\]

In this mode the current through \( L_2 \) is less than current through \( L_1 \) because the inductance value of \( L_1 < L_2 \) and this mode ends when \( I_{L1} = I_{L2} \) and converter operates in Mode III.

2) MODE II: WHEN SWITCH IS ON (\( t_1 < t < t_2 \))

Switch is just turned OFF. This mode occurs for a very duration of \( \delta T_S \) as shown in Figure 6(a). The equivalent circuit in this mode is shown in Figure 6(b). Diode \( D_1, D_2, D_4 \) and \( D_6 \) are forward biased while the diodes \( D_3, D_5 \) and \( D_7 \) are reverse biased. Inductor current \( I_{L2} \) is smaller than \( I_{L1} \) as shown in Figure 6(a). The current through \( L_2 \) has positive slope and magnetizes in this period and the current \( L_1 \) has large negative slope and discharge in this period. The current through \( D_2 \) will be difference between inductor current \( I_{L1} \) and \( I_{L2} \).

The slope of inductor currents of \( L_1 \) and \( L_2 \) can be achieved as

\[
\frac{dI_{L1}}{dt} = \frac{V_{in} - V_{C3}}{L_1} \\
\frac{dI_{L2}}{dt} = \frac{V_{in}}{L_2}
\]

3) MODE III: SWITCH IS OFF (\( t_2 < t < DT_s \))

Switch is OFF. The equivalent circuit is same as Mode II in CCM as shown in Figure 4(b). Diode \( D_1, D_4, D_6 \) are forward biased while the diodes \( D_2, D_3, D_5 \) and \( D_7 \) are reverse biased. The inductors \( L_1 \) and \( L_2 \) are in series and the current through inductors \( L_1 \) and \( L_2 \) are equal and demagnetize with equal negative slope which can be achieved as follows

\[
\frac{dI_{L1}}{dt} = \frac{2V_{in} - V_{C3}}{L_1 + L_2} \\
\frac{dI_{L2}}{dt} = \frac{2V_{in} - V_{C3}}{L_1 + L_2}
\]

The average of voltage across the inductor is null. Therefore,

\[
L_1 \rightarrow D(V_{in}) + \delta(V_{in} - V_{C3}) + \frac{L_1(2V_{in} - V_{C3})}{L_1 + L_2} \\
\times (1 - D - \delta) = 0
\]

\[
L_2 \rightarrow D(V_{in}) + \delta(V_{in}) + \frac{L_2(2V_{in} - V_{C3})}{L_1 + L_2} \\
\times (1 - D - \delta) = 0
\]

Also,

\[
V_{C3} = \frac{V_O}{3}
\]

On solving (43)-(45), the voltage gain of proposed converter SC-SL-DC can be obtained as

\[
\frac{V_O}{V_{in}} \bigg|_{L_2>L_1} = \frac{6}{(1 - D)}
\]

From equation (36) and (46) it can be seen that the voltage gain is unaffected with unequal values of inductances \( L_1 \) and \( L_2 \) i.e. six times the traditional boost converter (TBC).

However, the average value of current through the inductors are changed.

**V. STEADY STATE ANALYSIS IN DCM**

**A. MODE I: WHEN SWITCH IS ON (\( 0 < t < DT_s \))**

This mode is the same as Mode I of CCM mode and equivalent circuitry is depicted in Figure 4(a). Both the inductors \( L_1 \) and \( L_2 \) are magnetized by the input source voltage \( V_{in} \). The current rises from zero to maximum value in both the inductors till the time, \( t_1 = DT \).

**B. MODE II: WHEN SWITCH IS OFF (\( DT_s < t < D_1T_s \))**

This mode is equivalent to mode II of CCM. All the inductors demagnetize from their maximum value to zero at time \( t_2 = D_1T \).
C. MODE III: WHEN SWITCH IS OFF AND INDUCTOR CURRENT IS ZERO ($D_1 T_S < t < T_S$)

In this mode, all diodes $D_1$-$D_7$ are reverse biased. Inductor current in this interval ($t_2 < t < t_3$) is zero. Energy is provided by capacitor $C_o$ to load $R$. The equivalent circuit diagram and associated waveforms are depicted in Figure 7 and Figure 8.

Applying the volt-sec balance principle on the inductors yields the following relation

$$D_1 = \frac{6D}{V_{in}} - 6$$  \hspace{1cm} (47)

$$I_L = I_{D1} + I_{D4} + I_{D6} = 3I_O$$  \hspace{1cm} (48)

$$3V_O \frac{R}{R} = \frac{1}{2} D (D + D_1) \frac{V_{in}}{L_f S}$$  \hspace{1cm} (49)

$$V_o \frac{V_{in}}{V_{in}} = \frac{D (D + D_1) R}{6L_f S}$$  \hspace{1cm} (50)

Using the value of $D_1$ from (47) in (50) the following quadratic equation is obtained

$$(V_o \frac{V_{in}}{V_{in}})^2 - 6V_o \frac{V_{in}}{V_{in}} - 6D^2 \frac{V_{in}}{\beta} = 0$$  \hspace{1cm} (51)

Defining $\beta_L = \frac{6L_f S}{R}$ as normalized inductor time constant, the ideal voltage gain ($M_{DM}$) in DCM mode is calculated as

$$M_{DM} = \frac{V_o}{V_{in}} = 3 + \sqrt{9 + \frac{6D^2}{\beta_L}}$$  \hspace{1cm} (52)

If the converter is to be operated at the boundary of CCM and DCM, then the voltage gain of both modes will be equal. The normalized inductor time ($\beta_{L,B}$) constant at the boundary is calculated as

$$\beta_{L,B} = \frac{D(1 - D)^2}{6}$$  \hspace{1cm} (53)

A plot between $\beta_{L,B}$ and duty ratio $D$ is shown illustrated in Figure 8. The converter operates in CCM mode if $\beta_L > \beta_{L,B}$ and the reverse is true for DCM mode.

VI. PRACTICAL MODEL OF THE PROPOSED CONVERTER

The equivalent circuit of the proposed converter is shown in Figure 11. $R_L$ is the equivalent series resistance (ESR) of the inductor $R_{SW}$ is the switch ON-state resistance, $R_{DS}$ and $V_{CN}$ denote the diode internal resistance and voltage drop respectively. $R_C$ is the equivalent series resistance (ESR) of the capacitors.
A. **Effect of Non-Idealities on Voltage Gain**

1) **Effect of Non-Ideal Inductors on Voltage Gain**

The effect of non-ideal inductors having parasitic resistances on voltage gain is analysed and other elements are assumed ideal.

The voltage across inductor $L_1$ and $L_2$ in both modes can be found as:

**MODE I:**

\[
\begin{align*}
V_{L1} & = V_{in} - I_{L1}R_{L1} \\
V_{L2} & = V_{in} - I_{L2}R_{L2} \\
V_{C2} & = -V_{in}
\end{align*}
\]

**MODE II:**

\[
\begin{align*}
V_{L1} + V_{L2} & = V_{in} - V_{C2} - V_{C3} - I_{L1}(R_{L1} + R_{L2}) \\
V_{C3} & = \frac{V_o}{3}
\end{align*}
\]

2) **Effect of Non-Ideal Switch on Voltage Gain**

The voltages across the inductors in both modes can be found as:

**MODE I:**

\[
\begin{align*}
V_{L1} & = V_{in} - I_{SW}R_{SW} \\
V_{L2} & = V_{in} - I_{SW}R_{SW}
\end{align*}
\]
**MODE II:** The useful voltage relations are:

\[ V_{L1} = V_{L2} = \frac{V_{in} - V_{C2} - V_{C3}}{2} \] (63)

\[ V_{C2} = -V_{in} + I_{SW} R_{SW} \] (64)

Since the average value of voltage across the inductor is zero. Therefore, the expression can be derived as follows

\[ D (V_{in} - I_{SW} R_{SW}) + (1 - D) \left( \frac{V_{in} - V_{C2} - V_{C3}}{2} \right) \] (65)

\[ D (V_{in} - I_{SW} R_{SW}) + (1 - D) \left( \frac{2V_{in} - I_{SW} R_{SW} - V_{o}}{2} \right) \] (66)

The ratio of output voltage to the input voltage is derived using (66)

\[ \frac{V_o}{V_{in}} = \frac{6 \left( 1 - \frac{I_s R_s (1 + D)}{2V_{in}} \right)}{(1 - D)} = \frac{6 \left( 1 - \frac{V_{SD} (1 + D)}{2V_{in}} \right)}{(1 - D)} \] (67)

where \( I_s R_s = V_{SD} \) is the voltage drop across the switch.

Using the value of \( I_{SW} \) from expression (23)

\[ \frac{V_o}{V_{in}} = \frac{6 \left( 1 - \frac{(5 + D)(1 + D)}{2V_{in}} R_{SW} \right)}{(1 - D)} \] (68)

\[ \frac{V_o}{V_{in}} = \frac{6}{(1 - D)} \left[ 1 + \frac{3D}{(1 - D)^2} R_{SW} \right] \] (69)

The effect on voltage gain is given by (67) and (69) and the plot of both the expressions are shown in Figure 14 and 15a respectively. From Figure 15a it can be inferred that the gain rapidly decreases with an increase in the parasitic resistance of the switch, especially at higher duty ratios.

3) **EFFECT OF NON-IDEAL DIODES ON VOLTAGE GAIN**

The effect of non-ideal diodes (D1-D7) having parasitic resistance (R_D) and forward cut in voltage (V_CN) on voltage gain is analysed and other elements are assumed ideal.

**MODE I:** The inductor voltage relations are:

\[ \begin{cases} V_{L1} = V_{in} - I_L R_D - V_{CN} \\ V_{L2} = V_{in} - I_L R_D - V_{CN} \end{cases} \] (70)

**MODE II:** The inductor voltage relations are:

\[ \begin{align*} V_{L1} &= V_{L2} = \frac{V_{in} - V_{C2} - V_{C3} - V_{CN} - \frac{I_L R_D}{(1 - D)}}{2} \\ V_{C2} &= -V_{in} + \frac{2I_L R_D}{D} + 2V_{CN} \\ V_{C3} &= V_{O} - \frac{2}{3} \end{align*} \] (71)

Since the average value of voltage across the inductor is null. Therefore, the expression can be derived as follows

\[ D (V_{in} - I_L R_D - V_{CN}) + (1 - D) \times \left( \frac{V_{in} - V_{C2} - V_{C3} - V_{CN} - \frac{I_L R_D}{(1 - D)}}{2} \right) \] (74)

The effect on voltage gain is given by (75)

\[ \frac{V_o}{V_{in}} = \frac{6 \left( 1 - \frac{V_{CN}}{V_{in}} \right)}{(1 - D)} \left[ 1 + \frac{(6 + D - D^2) V_{in}}{R_{SW} (1 - D)^2} \right] \] (75)
4) EFFECT OF ESR OF CAPACITORS ON VOLTAGE GAIN
The ON and OFF state current through the capacitors is found using (3) and (7).

The effect of ESR of capacitors (C₁ to C₅) on voltage gain is analysed and other elements are assumed ideal.

The voltage across inductor L₁ and L₂ in both modes can be found as:

**MODE I:** The useful voltage relations are:

\[
V_{L2} = V_{L2} = V_{in} \\
V_{C2} = -V_{in} + \frac{3I_0R_{C2}}{D} \\
V_{C4} + V_{C5} = VO - \frac{I_oR_{C4}}{D} + \frac{I_oR_{C5}}{D} \\
V_{C1} + V_{C3} + V_{C5} = VO - V_{in} + \frac{2I_o}{D}(R_{C1} + R_{C3} + R_{C5})
\]

**(76)** *(77)** *(78)** *(79)**

**MODE II:** The useful voltage relations are:

\[
V_{L1} = V_{L2} = \frac{V_{in} - V_{C2} - V_{C3} - \frac{3I_0R_{C2}}{(1-D)} - \frac{2I_0R_{C3}}{(1-D)}}{2}
\]

\[
V_{C4} - V_{C5} = V_{C3} + \frac{2I_oR_{C3}}{(1-D)} + \frac{I_oR_{C4}}{(1-D)} + \frac{I_oR_{C5}}{(1-D)}
\]

\[
V_{C3} - V_{C1} = V_{in} + \frac{2I_o(R_{C1} - R_{C3})}{(1-D)}
\]

**(80)** *(81)** *(82)**

Since the average value of voltage across the inductor is zero. Therefore, the expression can be derived as follows

\[
D(V_{in}) + (1-D)(V_{in} - V_{C2} - V_{C3} - \frac{3I_0R_{C2}}{(1-D)} - \frac{2I_0R_{C3}}{(1-D)}) = \frac{2V_{in}}{(1-D)} = V_{C2} + V_{C3} + \frac{3I_oR_{C2}}{(1-D)} + \frac{2I_oR_{C3}}{(1-D)}
\]

**(83)** *(84)** *(85)**

Using (77) in (84)

\[
\frac{2V_{in}}{(1-D)} = V_{C3} + \frac{3I_0R_{C2}}{(1-D)} + \frac{2I_0R_{C3}}{(1-D)}
\]

**(86)**

V₁, V₃, V₅ are obtained using (77),(78) and (79) and putting these relations in (80) the effect of ESR values of capacitors on voltage gain is obtained as (86), as shown at the bottom of the page.

For simplicity, it is assumed that

\[
\frac{R_{C1}}{V_O} = \frac{R_{C2} = R_{C3} = R_{C4} = R_{C5} = R_C}{V_{in}} = \frac{6}{(1-D)} - \frac{(21-2D)I_oR_C}{D(1-D)V_{in}}
\]

**(87)** *(88)**

**Figure 15(b) shows the variation in gain when the capacitor resistance is increased. The gain decreases especially at higher duty ratios and low value of load resistance.**

5) COMBINED EFFECT OF NON-IDEALITIES ON VOLTAGE GAIN
The combined effect of all parasitic elements on voltage gain can be found by considering all the non-idealities of the proposed converter.

The deviation from voltage gain can be obtained as follows

\[
\frac{V_O}{V_{in}} = \frac{6}{(1-D)} - \frac{18I_oR_L}{V_{in}} \frac{3(5+D)(1+D)I_oR_{SW}}{D(1-D)^2V_{in}}
\]

**(89)**

where \(I_o = \frac{V_o}{R_o}\) is output load current.

The combined effect of non-idealities on the voltage gain can be derived as

\[
\frac{V_O}{V_{in}} = \frac{6}{(1-D)} \left[ 1 + a\frac{R_L}{R} + b\frac{R_{SW}}{R} + c\frac{R_D}{R} + d\frac{R_C}{R} \right]
\]

**(90)**

where

\[
\begin{align*}
a &= \frac{18}{(1-D)^2} \\
b &= \frac{3(5+D)(1+D)}{(1-D)^2} \\
c &= \frac{(6+D-D^2)}{D(1-D)^2} \\
d &= \frac{(21-2D)}{D(1-D)}
\end{align*}
\]

B. POWER LOSS ANALYSIS OF THE PROPOSED CONVERTER

1) LOSSES IN PROPOSED CONVERTER DUE TO SWITCH
The practical power switch has conduction and switching losses.

The conduction loss in the switch during the ON state by the parasitic resistance \(R_{SW}\).

\[
P_{SWcond} = I_{SWrms}^2 \times R_{SW}
\]

**(91)**

where \(I_{SWrms}\) is root mean square value of switch current and it is equal to

\[
I_{SWrms} = \frac{5+D}{\sqrt{D(1-D)}} I_o
\]

**(92)**

\[
P_{SWcond} = \frac{(5+D)^2}{D(1-D)^2} I_o^2 R_{SW}
\]

**(93)**

\[
P_{SWcond} = \frac{(5+D)^2}{D(1-D)^2} R_{SW} P_o
\]

**(94)**

where \(P_o\) is the output power of the resistive load.

\[
\frac{V_O}{V_{in}} = \frac{6}{(1-D)} - \frac{1}{D(1-D)} \left( \frac{4I_oR_{C1} + 9I_oR_{C2} + 4I_oR_{C3} + I_oR_{C4} + (3-2D)I_oR_{C5}}{V_{in}} \right)
\]

**(86)**

124570
The switching loss ($P_{\text{Sw\_switching}}$) of the power switch can be calculated with the approximate relation shown in (95).

$$P_{\text{Sw\_switching}} = \frac{(t_r + t_f)(I_{\text{SWavg}}V_s) \times f_s}{2} \quad (95)$$

where, $t_r$ = total rise time of the switch, $t_f$ = total fall time, $f_s$ = switching frequency.

$$V_s = \frac{V_o}{3}, \ I_{\text{SWavg}} = \frac{5 + D}{1 - D} I_o \quad (96)$$

$$P_{\text{Sw\_switching}} = \frac{(t_r + t_f)(5 + D)V_o^2 f_s}{3R(1 - D)} \quad (97)$$

Total loss in the switch ($P_{\text{Sw\_loss\_total}}$) is the sum of conduction and switching loss and can be expressed as

$$P_{\text{SW\_loss\_total}} = P_{\text{Sw\_cond}} + P_{\text{Sw\_switching}} \quad (98)$$

$$P_{\text{SW\_loss\_total}} = \begin{cases} 
(5 + D)^2 R_{SW} & \frac{(t_r + t_f)(5 + D)f_s}{3R(1 - D)} \ P_o \\
\vdots & \vdots \\
3.2W & \vdots 
\end{cases} \quad (99)$$

2) LOSSES IN PROPOSED CONVERTER DUE TO SEVEN DIODES ($D_1$-$D_7$)

As compared to conduction loss the switching loss in the diode is neglected and only conduction losses are taken into consideration. It is assumed that all diodes have equal resistance $R_{DS}$ and equal cut in voltage $V_{CN}$.

The conduction loss due to parasitic resistance ($P_{D_r}$) is calculated using

$$P_{D_r} = I_{D_{rms}}^2 R_{DS} \quad (100)$$

The conduction loss ($P_{D_{CN}}$) due to cut in voltage in forward biased is calculated using

$$P_{D_{CN}} = V_{CN} I_{D_{dc}} \quad (101)$$

Total conduction loss in the diode ($P_{D_{loss}}$) is the sum of both losses

$$P_{D_{loss}} = P_{D_r} + P_{D_{CN}} = I_{D_{rms}}^2 R_{DS} + V_{CN} I_{D_{dc}} \quad (102)$$

Total conduction losses due to in the proposed converter is the sum of all losses in the diodes

$$P_{D_{loss\_total}} = \sum_{i=1}^{7} P_{D_{loss}} = \sum_{i=1}^{7} (I_{D_{rms}}^2 R_{DS} + V_{CN} I_{D_{dc}}) \quad (103)$$

The root mean square value of current through the diodes is expressed as below

$$I_{D1_{rms}} = I_{D4_{rms}} = I_{D6_{rms}} = \frac{I_o}{\sqrt{(1 - D)}} \quad (104)$$

$$I_{D2_{rms}} = I_{D3_{rms}} = \frac{3I_o}{(1 - D)\sqrt{D}} \quad (105)$$

$$I_{D5_{rms}} = I_{D7_{rms}} = \frac{I_o}{\sqrt{D}} \quad (106)$$

$$P_{D1_{loss}} = \frac{I_o^2}{(1 - D)} R_{DS} + V_{CN} I_o$$

$$= \left(\frac{1}{(1 - D)} \frac{R_{DS}}{R} + \frac{V_{CN}}{V_o}\right) P_o$$

$$P_{D2_{loss}} = \frac{9I_o^2}{D(1 - D)^2} R_{DS} + V_{CN} I_o$$

$$= \left(\frac{9}{D(1 - D)^2} \frac{R_{DS}}{R} + \frac{V_{CN}}{V_o}\right) P_o \quad (107)$$

$$P_{D3_{loss}} = P_{D2_{loss}}$$

$$P_{D4_{loss}} = P_{D6_{loss}} = P_{D1_{loss}}$$

$$P_{D5_{loss}} = P_{D7_{loss}}$$

$$P_{D_{loss\_total}} = \sum_{i=1}^{7} P_{D_{loss}}$$

$$= \left(\frac{1}{D(1 - D)^2} \frac{R_{DS}}{R} + \frac{7V_{CN}}{V_o}\right) P_o \quad (108)$$

$$P_{D_{loss\_total}} = 9.48W$$

3) LOSSES IN PROPOSED CONVERTER DUE TO TWO INDUCTORS ($L_1$ AND $L_2$)

The total conduction losses in the two inductors are

$$P_{L_{1\_loss\_total}} = I_{L1_{rms}}^2 r_{L1} + I_{L2_{rms}}^2 r_{L2} \quad (109)$$

Using equation (22) to find the value of root mean square (rms) value of inductor currents.

$$P_{L_{loss\_total}} = \frac{9I_o^2}{(1 - D)^2} (r_{L1} + r_{L2}) \quad (110)$$

or it can be equivalently written as

$$P_{L_{loss\_total}} = \frac{9}{(1 - D)^2} \left(\frac{r_{L1}}{R} + \frac{r_{L2}}{R}\right) P_o \quad (111)$$

It is assumed that the ESR value of both the inductors are equal ($r_{L1} = r_{L2} = r_L$) then total loss in the inductor can be expressed as

$$P_{L_{loss\_total}} = \frac{18}{(1 - D)^2} \left(\frac{r_L}{R}\right) P_o \quad (112)$$

$$P_{L_{loss\_total}} = 5.8W$$

4) LOSSES IN PROPOSED CONVERTER DUE TO SIX CAPACITORS ($C_O$-$C_5$)

The power loss in the capacitors due to series resistance is

$$P_{C_{loss}} = I_{C_{rms}}^2 R_C \quad (113)$$

The total losses in the proposed converter are the sum of losses due to all the capacitors i.e.

$$P_{C_{loss\_total}} = \sum_{i=0}^{5} P_{C_{loss}} = \sum_{i=0}^{5} (I_{C_{rms}}^2 \times R_C) \quad (114)$$
The rms value of current through capacitors can be calculated using the formula

\[
I_{C_{rms}} = \sqrt{\frac{1}{T_S} \left( \int_0^{T_S} I_{C_{rms}}^2 dt + \int_0^{T_S} I_{C_{rms}}^2 dt \right)}
\]  

(115)

The values of rms currents through capacitors can be earned using (3), (7) and (115)

\[
\begin{align*}
I_{C1_{rms}} &= \frac{2I_o}{\sqrt{D(1-D)}}, \quad P_{C1_{loss}} = \frac{4I_o^2 R C_1}{D(1-D)} = \frac{4}{D(1-D)} R C_1 P_O \\
I_{C2_{rms}} &= \frac{3I_o}{\sqrt{D(1-D)}}, \quad P_{C2_{loss}} = \frac{9I_o^2 R C_2}{D(1-D)} = \frac{9}{D(1-D)} R C_2 P_O \\
I_{C3_{rms}} &= \frac{3I_o}{\sqrt{D(1-D)}}, \quad P_{C3_{loss}} = \frac{9I_o^2 R C_3}{D(1-D)} = \frac{9}{D(1-D)} R C_3 P_O \\
I_{C4_{rms}} &= \frac{I_o}{\sqrt{D(1-D)}}, \quad P_{C4_{loss}} = \frac{I_o^2 R C_4}{D(1-D)} = \frac{1}{D(1-D)} R C_4 P_O \\
I_{C5_{rms}} &= \frac{I_o}{\sqrt{D(1-D)}}, \quad P_{C5_{loss}} = \frac{I_o^2 R C_5}{D(1-D)} = \frac{1}{D(1-D)} R C_5 P_O \\
I_{CO_{rms}} &= \sqrt{\frac{1-D}{D}} I_o, \quad P_{CO_{loss}} = \frac{(1-D)I_o^2 R C_O}{D} = \frac{1-D}{D} R C_O P_O
\end{align*}
\]

(116)

Summation of all individual losses occurring in capacitor gives total losses occurring due to capacitors in the proposed converter

\[
P_{C_{loss_{total}}} = P_{C1_{loss}} + P_{C2_{loss}} + P_{C3_{loss}} + P_{C4_{loss}} + P_{C5_{loss}} + P_{CO_{loss}}
\]

(117)

If it is assumed that

\[
R_{C1} = R_{C2} = R_{C3} = R_{C4} = R_{C5} = R_{CO} = R_C
\]

Then

\[
\begin{align*}
P_{C_{loss_{total}}} &= \frac{(D^2 - 2D + 25) R C}{D (1-D)} P_O \\
P_{C_{loss_{total}}} &= 2.52W
\end{align*}
\]

(118)

Hence total in the proposed converter is the sum of all the losses occurring in the proposed converter that is expressed below.

\[
P_{loss_{total}} = P_{SW_{loss_{total}}} + P_{D_{loss_{total}}} + P_{L_{loss_{total}}} + P_{C_{loss_{total}}}
\]

(119)

\[
P_{loss_{total}} = \left( \frac{f_s C_S R}{9} + a \frac{R_{SW}}{R} + b \frac{R_{DS}}{R} + c \frac{r_L}{R} \right) P_O + d \frac{R_C}{R} + \frac{7 V_{CN}}{V_o} P_O
\]

(120)

where

\[
\begin{align*}
a &= \frac{(5 + D)^2}{D(1-D)^2}, \quad b = \frac{(20 - D - D^2)}{D(1-D)^2} \\
c &= \frac{18}{(1-D)^2}, \quad d = \frac{(D^2 - 2D + 25)}{D(1-D)}
\end{align*}
\]

The efficiency (\(\eta\)) of the proposed converter can be expressed as below

\[
\eta = \frac{P_O}{P_O + P_{loss_{total}}}
\]

(121)
\[ n = \frac{1}{1 + \frac{fS C R}{2} + a \frac{R S}{R} + b \frac{R S}{R} + c \frac{R}{R} + d \frac{R}{R} + e \frac{V_{in}}{V_{o}}} \]  

(122)

**VII. PERFORMANCE ANALYSIS WITH SIMILAR CONVERTERS**

A detailed comparative analysis has been carried out and two traditional topologies and a few very recent high gain converter topologies have been considered. The analysis is based on the number of components, voltage gain and voltage stress across switches as given in Table 1. When compared to conventional boost and conventional quadratic boost converter the proposed topology can obtain a higher gain and the switch stress is considerably low. The converter in [8], adopts two switches and four inductors but its voltage gain is found to be lower than the proposed converter. The converter in [11] also has a lower voltage gain and higher switch stress than the proposed topology. The converter in [18] uses a total of four inductors which makes the converter bulky and the voltage gains are also low. Converters in [21], [22] and [28] have a relatively lower component count but the voltage gains are substantially less. The converter in [24], has a total of three switches (which could make the control of the converter complicated) but the voltage gains are less and switch stress is found to be higher. In [27] the topology has employed five inductors, two switches and a total of 18 components, and the increased count of components results in increased size of the converter and inefficiency and its voltage gain is quite low as compared to the proposed topology. Voltage gains of the converter proposed in [31] are also considerably less than the proposed converter. The converter in [32] has a total component count of 16 equal to the proposed converter including 3 inductors and 7 capacitors, but the voltage gains are considerably less than the proposed topology. Converter in [4] has adopted a total of 4 switches in its proposed circuit which can make the converter control very complex as compared to a single switch in the topology in this literature and even then, the voltage gains are lower.

For comparison, a plot of the voltage gain(M) versus the duty ratio(D) for the proposed topology and other similar converters is shown in Figure 16. It can be observed that the proposed topology gives the highest voltage gain even at low values of the duty ratio(D). A gain of almost ten times can be achieved at a duty of 0.4. High gain at a lower duty ratio reduces the current stress of the converter. The voltage gain of converters in [27], [11] is slightly higher than the proposed topology when it is operated at duty ratio values close to D = 0.8 but the switch stress is also high at these extreme values of the duty ratio. The plot of voltage stress vs the voltage gain is shown in Figure 17. It can be inferred from this plot that the proposed converter has one of the lowest voltage stresses across the switch.

Based on the comparison results the proposed converter topology is more advantageous as it can achieve high voltage gain, low voltage stress and is controlled by a single switch.

**VIII. STATE SPACE MODEL OF THE PROPOSED CONVERTER**

To derive the small signal state space model small resistances with capacitors C1, C2 and C5 are considered. These resistances are used to simplify the analysis and to eliminate the invalid variables from the state space representation. Assuming the same value of inductors, the inductor current is represented by a single state variable. All the capacitors except the output capacitor have same value. The dynamic equations in ON and OFF state can be represented as shown in equation (123) and equation (124).

**A. ON STATE**

\[
\begin{bmatrix}
\dot{i}_L \\
v\dot{C}_1 \\
v\dot{C}_2 \\
v\dot{C}_3 \\
v\dot{C}_4 \\
v\dot{C}_5 \\
v\dot{C}_o
\end{bmatrix} = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & \frac{1}{rC} & 0 & \frac{1}{rC} & -\frac{1}{rC} & 0 & 0 \\
0 & 0 & -\frac{1}{rC} & 0 & 0 & 0 & 0 \\
0 & \frac{1}{rC} & 0 & \frac{1}{rC} & -\frac{1}{rC} & 0 & 0 \\
0 & \frac{1}{rC} & 0 & \frac{1}{rC} & -\frac{2}{rC} & -\frac{1}{rC} & 0 \\
0 & 0 & 0 & 0 & \frac{1}{rC} & \frac{1}{rC} & -\frac{1}{rC} \\
0 & 0 & 0 & 0 & \frac{1}{rC_o} & \frac{1}{rC_o} & r + \frac{R}{C_arR}
\end{bmatrix} \begin{bmatrix}
i_L \\
v_{C1} \\
v_{C2} \\
v_{C3} \\
v_{C4} \\
v_{C5} \\
v_{Co}
\end{bmatrix} \times \begin{bmatrix}
\frac{1}{L} \\
\frac{1}{rC} \\
\frac{1}{rC} \\
\frac{1}{rC} \\
\frac{1}{rC} \\
\frac{1}{rC} \\
0
\end{bmatrix} v_{in}
\]

\[ v_o(t) = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 1
\end{bmatrix} \begin{bmatrix}
i_L \\
v_{C1} \\
v_{C2} \\
v_{C3} \\
v_{C4} \\
v_{C5} \\
v_{Co}
\end{bmatrix} \]  

(123)
### B. OFF STATE

\[
\begin{bmatrix}
  \dot{i}_L \\
  \dot{v}_{C1} \\
  \dot{v}_{C2} \\
  \dot{v}_{C3} \\
  \dot{v}_{C4} \\
  \dot{v}_{C5} \\
  \dot{v}_{Co}
\end{bmatrix} = \begin{bmatrix}
  -\frac{r}{2L} & 0 & 0 & -\frac{1}{2L} & 0 & 0 & 0 \\
  0 & 0 & 0 & 0 & \frac{1}{rC} & 0 & 0 \\
  0 & 0 & 0 & 0 & 0 & \frac{1}{rC} & 0 \\
  0 & 0 & -\frac{2}{rC} & \frac{1}{rC} & \frac{1}{rC} & 0 & 0 \\
  0 & 0 & -\frac{1}{rC} & \frac{1}{rC} & \frac{1}{rC} & 0 & 0 \\
  0 & 0 & -\frac{1}{rC} & \frac{1}{rC} & \frac{1}{rC} & 0 & 0 \\
  0 & 0 & 0 & 0 & 0 & 0 & 0 \\
  0 & 0 & 0 & 0 & -\frac{1}{RC_o} & 0 & 0
\end{bmatrix}
\times
\begin{bmatrix}
  \frac{1}{2L} \\
  \frac{1}{rC} \\
  \frac{1}{rC} \\
  \frac{1}{rC} \\
  \frac{1}{rC} \\
  \frac{1}{rC} \\
  0 \\
  0
\end{bmatrix}
+ \begin{bmatrix}
  \dot{v}_{in}
\end{bmatrix}
\]

\[
v_o(t) = \begin{bmatrix}
  0 & 0 & 0 & 0 & 0 & 0 & 1
\end{bmatrix}
\]

The converter operates in ON mode with a time \(d(t)\) and in OFF mode with a time \((1-d(t))\). The averaged model by combining (123) and (124) can be obtained and written as shown in (125), as shown at the bottom of the next page.

After perturbation when all the state variables are written in terms of dc signal and small signals as shown in (126), as shown at the bottom of page 17, the small signal model of the proposed converter neglecting the dc terms can be obtained as shown in (127), as shown at the bottom of page 17.

The open loop dynamic response of \(\frac{\dot{v}_o(s)}{d(s)}\) obtained through PLECS software, plotted in MATLAB for the same values as shown in Table 2. is depicted in Figure 18. From the bode plot of uncompensated system it can be observed that the phase margin at the gain crossover frequency is only 10°.

![Figure 18](image1.png)

**FIGURE 18.** (a) Voltage control Loop. (b) Bode plots of open loop, closed loop and compensator.

![Figure 19](image2.png)

**FIGURE 19.** (a) Hardware prototype of the proposed converter. (b) Experimental set-up.
which is not desirable. For closed loop stability of the system, the desirable phase margin should be between 45° to 65° to achieve good step response of the system.

1) VOLTAGE CONTROLLER DESIGN USING PLECS SOFTWARE

Using PLECS software the uncompensated bode plot can be observed and a proper controller can be designed. A PI controller usually works well for the lower order system. From the uncompensated bode plot it can be observed that the system is stable but it has zeroes in right half plane. To achieve proper phase margin a compensator is designed to remove the steady state error and remove the disturbances at high frequencies, for which the poles are added up at 0 rad/s and 10000 rad/s respectively. Zeroes are added at frequencies of 100rad/s and 1000 rad/s to achieve the desired phase margin. The compensator transfer function is given by (128)

$$G_c(s) = \frac{K(s + 1/\omega_1)(s + 1/\omega_2)}{s(s + 1/\omega_{P1})}$$

$$G_c(s) = \frac{10(s + 1/100)(s + 1/1000)}{s(s + 1/10000)}$$

From the Figure 18 of the compensated closed loop plot it can be observed that phase margin of closed loop system is 63° at the gain crossover frequency which shows that the closed loop system is stable.

IX. LABORATORY PERFORMANCE OF THE PROPOSED CONVERTER

The performance of the proposed converter is determined by building the hardware prototype as shown in Figure 19(a) in the laboratory. The converter is operated at a duty ratio of 40% and 30% in continuous conduction mode at a switching frequency of 50kHz. The design specifications of the presented
converter are listed in Table 2 and the experimental set-up is shown in Figure 19(b).

As depicted in Figure 20 measured input and output voltage are 12V and 117V respectively. The output voltage is reduced due to the effect of the parasitic resistance of the diodes, switch, capacitors and inductors. In the same Figure, the ripple observed in the output capacitor (Co) is two per cent (2%) of V0 that is about 2.24V. The drain to source voltage of the power MOSFET (S) is presented in Figure 20 with respective gate to source signals (Vgs). The maximum value

\[
\begin{align*}
\dot{i}_L &= I_L + \tilde{i}_L \\
\dot{v}_{c1} &= V_{c1} + \tilde{v}_{c1} \\
\dot{v}_{c2} &= V_{c2} + \tilde{v}_{c2} \\
\dot{v}_{c3} &= V_{c3} + \tilde{v}_{c3} \\
\dot{v}_{c4} &= V_{c4} + \tilde{v}_{c4} \\
\dot{v}_{c5} &= V_{c5} + \tilde{v}_{c5} \\
\dot{v}_{co} &= V_{co} + \tilde{v}_{co}
\end{align*}
\]

\[
\begin{bmatrix}
\frac{(1 - D)r}{2L} & 0 & 0 & \frac{(1 - D)}{2L} & 0 & 0 & 0 \\
0 & \frac{D}{rC} & 0 & \frac{1}{rC} & - \frac{D}{rC} & 0 & 0 \\
\frac{1 - D}{C} & 0 & - \frac{D}{rC} & 0 & 0 & 0 & 0 \\
\frac{1 - D}{C} & 0 & 0 & \frac{3D - 2}{rC} & \frac{1 - 2D}{rC} & \frac{1 - D}{rC} & 0 \\
0 & \frac{D}{rC} & 0 & \frac{2D - 1}{rC} & \frac{1 - 3D}{rC} & \frac{1 - 2D}{rC} & \frac{D}{rC} \\
0 & 0 & 0 & \frac{(1 - D)}{rC} & \frac{1}{rC} & \frac{1}{rC} & - \frac{D}{rC} \\
0 & 0 & 0 & 0 & \frac{D}{rC} & \frac{D}{rC} & \frac{D(R + 2r) - r}{RrCo}
\end{bmatrix}
\]

\[
\begin{bmatrix}
\frac{1 + D}{2L} & \frac{2D - 1}{rC} & \frac{D}{rC} & \frac{1}{rC} & \frac{1}{rC} & \frac{1}{rC} & \frac{1}{rC} \\
0 & \frac{1}{rC} & 0 & 0 & - \frac{1}{rC} & 0 & 0 \\
- \frac{1}{C} & 0 & - \frac{1}{rC} & 0 & 0 & 0 & 0 \\
- \frac{1}{C} & 0 & 0 & \frac{3}{rC} & \frac{2}{rC} & \frac{-1}{rC} & 0 \\
0 & \frac{1}{rC} & 0 & \frac{2}{rC} & \frac{-3}{rC} & \frac{-2}{rC} & \frac{1}{rC} \\
0 & 0 & 0 & \frac{1}{rC} & 0 & 0 & - \frac{1}{rC} \\
0 & 0 & 0 & 0 & \frac{1}{rC} & \frac{1}{rC} & \frac{R + 2r}{RrCo}
\end{bmatrix}
\]

\[
\tilde{v}_a(t) = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 & 1
\end{bmatrix}
\]

(126)
TABLE 1. Comparison of proposed converter with other high gain converters.

| Converters | Switch Count (S_e) | Inductor count (L_e) | Capacitor count (C_e) | Diode count (D_e) | M (\frac{\Delta i}{V_{in}}) | M at D=0.5 | Voltage Stress (\frac{\Delta V}{V_o}) |
|------------|-------------------|---------------------|----------------------|------------------|-----------------------------|------------|--------------------------------------|
| TBC        | 1                 | 1                   | 1                    | 1                | \frac{1}{(1-D)}             | 2          | 1                                    |
| TQBC       | 1                 | 2                   | 2                    | 3                | \frac{1}{(1-D)^2}           | 4          | 1                                    |
| [8]        | 2                 | 4                   | 3                    | 7                | \frac{3+D}{(1-D)}           | 7          | S_1; \frac{2}{3+D}, S_2; \frac{1}{3+D} |
| [11]       | 2                 | 2                   | 4                    | 6                | \frac{3-3D+D^2}{(1-D)^2}    | 7          | S_1; \frac{1}{1+3D+D^2}              |
| [18]       | 1                 | 4                   | 6                    | 3                | \frac{3D}{(1-D)}            | 3          | \frac{1}{3D}                          |
| [21]       | 2                 | 2                   | 4                    | 5                | \frac{5+D}{(1-D)}           | 11         | \frac{1}{5+D}                         |
| [22]       | 2                 | 2                   | 2                    | 4                | \frac{1+D}{(1-D)}           | 6          | \frac{1}{1+D}                         |
| [24]       | 3                 | 4                   | 2                    | 5                | \frac{5+D}{(1-D)}           | 11         | S_1; \frac{1}{5+D}, S_2; \frac{1}{(1-D)(5+D)} |
| [27]       | 2                 | 5                   | 3                    | 8                | \frac{1+5D+2D^2}{(1-D)}     | 8          | \frac{1}{1+5D+2D^2}                  |
| [28]       | 2                 | 2                   | 4                    | 4                | \frac{4}{(1-D)}             | 8          | \frac{1}{1+3D}                       |
| [31]       | 2                 | 4                   | 1                    | 9                | \frac{1+3D}{(1-D)}          | 5          | S_1; \frac{1+D}{1+3D}, S_2; \frac{2D}{1+3D} |
| [32]       | 1                 | 3                   | 7                    | 5                | \frac{2+2D}{(1-D)}          | 6          | \frac{1}{1+2D}                       |
| [33]       | 4                 | 2                   | 4                    | 7                | \frac{4D}{(1-D)}           | 4          | \frac{1}{2+2D}                       |
| Proposed   | 1                 | 2                   | 6                    | 7                | \frac{6}{(1-D)}             | 12         | \frac{1}{3}                          |

TABLE 2. Hardware specifications of the converter.

| Elements    | Specification |
|-------------|---------------|
| Maximum Power | 200W           |
| Input Voltage | 12V/16V       |
| Switching Frequency | 50kHz       |
| Duty Ratio    | 30% and 40%   |
| Load Resistance | R=400-600 Ω |
| Inductors     | L_1=330μH     |
| Capacitors    | C_1=100μF/63V, C_2=C_3=C_4=C_5=47μF/200V & C_0=68μF/350V |
| Power MOSFET  | SPW52N50C3    |
| Diodes        | 2NF1000SM     |
| Gate Drivers IC| TLP250H       |
| Microcontroller | STM32 Nucleo H743ZI2 |

is found to be 40V which is approximately 34% of the output voltage (V_o). When the power switch is triggered using the respective gate signal both the inductor L_1 and L_2 magnetize from 1.2A to 1.6A.

The inductor current peak to peak ripple is about 0.2A (15%) which is near to the value used to design the inductors and when the MOSFET is turned OFF the inductor demagnetize with the effect to reduce current linearly. The average value of both the inductor current is found to be 1.36A. The inductor currents are found to be continuous. Figure 22 and 23 shows the voltage across the capacitors C_1, C_2, C_3, C_4 and C_5 and is found to be 25.8V, 10.5V, 38.8V, 78.2 and 35.5V respectively with very low voltage ripple and is much less than the output voltage. The voltage across the output diode D_7 is shown and equal to 40V which is the same as the stress across the switch and less than the output voltage equal to 34%. All the results show that the converter is smoothly working in continuous conduction mode.
Additional results to verify the working are obtained at $D = 0.3$ and $V_{in} = 12\,V$. As depicted in Figure 24 for an input of 12 V the output voltage is found to 96 V. The drop in the voltage is due to parasitic and ON state resistances. As shown in Figure 25, the voltage across capacitors $C_2$, $C_3$ and $C_4$ are found to be 10.2 V, 32 V and 60 V respectively. The capacitor voltages are constant with ripple in the voltage close to 2 V.

As can be seen from Figure 26, the voltage stress across the switch ($V_{sw}$) is observed to be 32 V which is one-third of the $V_o$.

The converter performance is also tested in dynamic conditions when the duty cycle is changed from $D = 0.3$ to
FIGURE 27. Output voltage and the output current when D is changed from 0.3 to 0.4.

FIGURE 28. Effect of the change in loading at $V_{in} = 15$ V and $D = 0.45$.

FIGURE 29. Ideal and experimental gain at different duty ratios.

$D = 0.4$ at $V_{in} = 16$ V. From Figure 27, it can be seen that the output voltage varies from 132 V at $D = 0.3$ to 150 V at $D = 0.4$. From the experimental results, it can be concluded that the converter performance is satisfactory in both steady-state and dynamic conditions. Figure 28 shows the response of the converter when load is decreased to 70% at $D = 0.45$ at $V_{in} = 15$ V. Also, the load current is increased as depicted in the same Figure. This shows that the regulation of the converter is good when load is changed. The output voltage is maintained between 160 V and 150 V. Figure 29 shows the experimental voltage gain with the change in the duty cycle. For the same value of load resistance, the gain decreases at a higher duty cycle due to an increase in losses. The efficiency at different values of output power is shown in Figure 30. It can be seen from the plot that at constant output power as the voltage is increased from 12 V to 24 V the efficiency of the converter increases. This is because to achieve the same power output the current decreases with the increase in output voltage. As a result, the conduction losses decreases and efficiency increases. The power loss in different components in percentage is shown in Figure 31. The maximum loss occurs in diodes as shown in Figure 32. The selection of devices with a low value of parasitic resistances increases the overall efficiency of the converter.

A. CLOSED LOOP VALIDATION USING TYPHOON-HIL REAL TIME EMULATOR

The performance of in closed loop operation is tested using hardware in loop (HIL) operation using Typhoon-HIL-402 real time emulator. The Typhoon-real time emulator is designed to check the performance of controller in real time. The results with change in input voltage and change in load are shown in Figure 32 and Figure 33. From Figure 32 it can be observed that as the input voltage is changed from
the input voltage is increased. The maximum efficiency voltage. The efficiency of the converter is found to improve the stress across switch and diodes is one-third of the output of the converter. The converter stress profile is also good as capacitors leads to the selection of low voltage rating capac-
decreases the gain of the converter. Low voltage stress across the high value of parasitic resistance of switch and inductors gain converters. The converter utilizes only two inductors compared with the quadratic boost converter and other high of the converter is found to be near 9.75 times at a duty multiplier cell made up of switched inductors. The voltage gain with a single switch and voltage multiplier for energy storage system application, ”IEEE Trans. Ind. Appl., vol. 56, no. 3, pp. 2816–2827, May 2020, doi: 10.1109/IEEETIA.2020.2980215.
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12 V to 17 V the output voltage is held constant at 120 V. Similarly, when load current is increased from 1.2 A to 2.2 A by decreasing the load resistance from 120 Ω to 55 Ω the output voltage is held constant by the voltage controller as shown in Figure 33. It can be concluded that the voltage controller is able to maintain the V o reference value.

X. CONCLUSION
In the proposed work, the converter (SC-SL-DC) has produced a voltage gain with a single switch and voltage multiplier cell made up of switched inductors. The voltage gain of the converter is found to be near 9.75 times at a duty ratio of 0.4 and 8 times at a duty of 0.3 which is high as compared with the quadratic boost converter and other high gain converters. The converter utilizes only two inductors which makes the converter light in weight. It is found that the high value of parasitic resistance of switch and inductors decreases the gain of the converter. Low voltage stress across capacitors leads to the selection of low voltage rating capacitors, which increases the efficiency and decreases the cost of the converter. The converter stress profile is also good as the stress across switch and diodes is one-third of the output voltage. The efficiency of the converter is found to improve if the input voltage is increased. The maximum efficiency is found to be 95.4%. The experimental results show that the converter is working in continuous current mode and the results match with the theoretical analysis. The proposed converter belongs to the non-isolated category and hence is suitable for medium power applications.

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