Recently, the use of electronic devices has significantly increased in various environments for Internet-of-things (IoT) applications. If heat-resistant devices were realized, they could be used in factories, fire incidents, and flight recorders. Furthermore, high-temperature memories in applications such as planetary probes could store important information recorded under high-temperature conditions, which would open doors to a new scientific and technological world. However, the typical silicon-based memory is limited to operating temperatures below 473 K because its semiconductors cease to function at high temperatures once the number of thermally induced carriers reaches the doping concentration level. Moreover, the number of thermally induced carriers depends on the semiconductor band gap. Recently, nonvolatile memories with metal nanogap structures have been realized. In a previous study, we realized the first extremely high-temperature heat-resistant memory based on a polycrystalline Pt nanogap. During operation, this memory exhibits a clear on/off ratio even at 873 K. When this is used over a wide temperature range, the resistance states at different temperatures can be misidentified when the resistance is strongly dependent on temperature. Since memory devices such as dynamic random access memory (DRAM) and flash memory generally have semiconductor channels, the conduction mechanism also involves carrier conduction in silicon channels, and temperature dependences are reflected by thermal activations. Therefore, the usual memory devices are at risk of misidentification or require a temperature adjustment system. To the best of the authors’ knowledge, the temperature dependences of resistive random access memory (ReRAM) employing a functional metal oxide sandwiched by metal electrodes were explored at 473 K. In these studies, thermal activation behavior was shown for a low-resistance state (LRS), a high-resistance state (HRS), or both. On the other hand, the conduction mechanism of resistance states of a nanogap memory is reported as tunneling conduction. Because the equation for tunneling conduction contains no temperature term, conductance changes can be neglected for various temperature ranges, and it was expected that a thermally robust memory would be realized using a nonvolatile memory employing Pt nanogaps. However, the conduction mechanism was only investigated below room temperature. At high temperatures, the temperature dependence should be considered not only in relation to the conduction mechanism but also with respect to the environmental surroundings, including current leakage through substrates. In this study, the thermal robustness of resistance states employing Pt nanogaps was investigated from room temperature to 773 K. In our previous study, nonvolatile resistance switching could be observed using nanogaps consisting of only two facing metal electrodes, the gap size of which was fixed using scanning tunneling microscopy feedback. This indicates that the resistance switching was caused only by the metal electrodes. Therefore, we discussed substrate dependence just under the nanogap using samples containing an etched SiO$_2$ layer with masked electrodes. Details of resistance switches using etched samples at room temperature are described elsewhere. A nonvolatile nanogap memory was fabricated on 300-nm-thick SiO$_2$, which was thermally grown on a Si wafer. Multiple Pt nanowires with widths of 400 nm and lengths of 4 µm were patterned by lift-off techniques using high-resolution electron beam lithography. Ti and Pt films with thicknesses of 1 and 20 nm, respectively, were deposited by electron beam evaporation. Electrode pads, containing Ti and Pt layers with thicknesses of 4 and 50 nm, respectively, were also fabricated by lift-off techniques using photolithography and sputter deposition. The fabricated Pt nanowires were then introduced into a vacuum probing station equipped with a source meter (Keithley 2636). Nanogap structures were formed by reconstructing the Pt nanowires using an electromigration method in a gas-containing environment at a pressure of 1 kPa. The gas was hydrogen, diluted to about 3.9% with Ar. The details of the nanogap fabrication are described elsewhere. To etch the SiO$_2$ layer on substrates, an ion etching chamber (ELIONIX EIS-200ER) was used, with CF$_4$ as the etching gas. The SiO$_2$ layer could be removed with high accuracy using the electron cyclotron...
Fabricated nanogap electrodes without and with etched SiO$_2$ nanogap structures functioned as an etching mask. A nanogap structure with the insulating layer removed just below the nanogap could be fabricated as shown in the inset of Fig. 1(b). Electronic property measurements were performed with another vacuum probing station equipped with the source meter and a sample annealing stage.

Figures 1(a) and 1(b) show field emission scanning electron microscopy (FESEM) images and schematics of typical fabricated nanogap electrodes without and with etched SiO$_2$ substrates, respectively. These FESEM images were measured with a tilt angle of 75°. Because the Pt electrodes had faceted structures, as shown in Fig. 1(a), the reconstruction of the Pt grains also occurred as in previous studies.$^6,^{18}$ Such a faceted nanogap has the advantage of suppressing the facile migration of Pt atoms during resistance switching. Side wall structures of the etched SiO$_2$ layer, the height of which was about 50 nm, are clearly shown. Since a valley-like structure was also constructed along the Pt nanogap, this indicates that the SiO$_2$ layer just below the nanogap could be partly removed by etching. In this paper, Pt nanogaps without and with etching are referred to as samples A and B, respectively.

Typical current–voltage ($I$–$V$) curves recorded during resistance switching using samples A and B at 773 K are shown in Fig. 2(a). The red circles indicate the observed current behavior of resistance changes from the HRS to the LRS. Applied voltages were swept from −0.5 to 4 V and then returned to −0.5 V with a current compliance at 10 µA. The black circles indicate the current behavior of resistance switching from the LRS to the HRS. Applied voltages were swept from −0.5 to 4 or 3 V, followed by a rapid voltage drop to 0 V. The applied voltages were smaller for the switching of sample B than for that of sample A. This suggested the occurrence of size dependence.$^{16,23}$ These curves indicated that clear resistance switching, the on/off ratio for which is above 10$^2$ at a voltage below 1 V, was also observed using both samples as with the previous results at room temperature.$^{31}$ Figure 2(b) shows schematic views of the two resistance conditions. The two tunneling distances reflect the two resistance states.$^{3,16}$

The black and red circles in Fig. 3(a) show the temperature dependences of the observed currents at 0.5 V for the two resistance states using samples A and B, respectively. The results indicate that on/off ratios were maintained at values above 100 using both samples, and the misidentification of resistance states could be avoided at 773 K. However, the temperature dependences of the LRS using both samples and the HRS using sample B were almost unchanged at the observed temperature. However, the observed current in the HRS using sample A gradually increased at high temperatures. To investigate this in more detail, Arrhenius plots using the data shown in Fig. 3(a) and a list of estimated activation energies are shown in Fig. 3(b). The activation energies were estimated using the Arrhenius-type thermal activation according to the equation$^{24}$

$$I = A \exp\left(-E_a/k_B T\right),$$

where $A$ is a constant, $E_a$ is the activation energy, $k_B$ is the Boltzmann constant, $I$ is the observed current, and $T$ is the temperature. The results indicated that the thermally activated behavior is clearly significant in the HRS using sample A. The slope of the plots increased slightly above 600 K. However, for sample B, the activation energy was moderate, and it is suggested that the conduction mechanism mainly involved tunneling conduction. These results indicate that the activation energies were caused by the substrate. Generally, leakage current, or the so-called stress-induced leakage current (SILC), was caused by the application of a large electric field above 1 MV/cm to the insulative SiO$_2$ layer.$^{25,26}$ Because voltages of 4 V were applied to the sub-1 nm gap...
width during switching operations for the HRS and LRS, as shown in Fig. 2, the stress-induced part was possibly formed in the SiO$_2$ layer, which is just below the nanogap. It is suggested that the activation energy of the HRS of sample A was related to the SILC. Moreover, the Arrhenius plots are bent as with the conduction of single molecules, which involves a mixture of thermally activated and direct tunneling conductions.$^{27,28}$ This indicates that the conduction behavior involves not only thermally activated conduction but also other mechanisms. At low temperatures, the slopes tended to be small. It can be considered that the conduction mechanism is mainly a simple tunneling conduction. Therefore, the temperature dependence below room temperature is independent of temperature as in the previous study.$^{3}$

Figure 4 shows a conduction model for sample A. Here, we discuss the steps taken to validate the conduction mechanism using a SiO$_2$ layer. Table I shows a comparison of the data from Fig. 3(a) with those from the SILC reported in Ref. 26. We refer to the SiO$_2$ width used in this study as the nanogap length, which was estimated by tunneling equation fitting.$^{29}$ Since direct tunnel conduction is independent of temperature, current changes followed by a change in temperature merely involve direct tunneling currents. Riess et al. reported that the SILC conduction mechanism is a mixture of Fowler–Nordheim tunneling and Schottky currents, which depend on temperature and electric field.$^{26}$ The conduction mechanism observed in this study is similar to that of the SILC. Temperature changes from 300 to 400 K and relative electric fields are identical and quite similar, respectively, between both mechanisms. Therefore, we expect a similar increase in current. Although electrode structures differ significantly and the leak currents generally fluctuate,$^{30}$ these current increases were roughly similar for the two samples listed in Table I. Moreover, the current increase was completely absent when the SiO$_2$ layer was removed by etching. Therefore, the current increase mechanisms are not deducible from the SILC. However, it is important to note that current leaks through the SiO$_2$ layer in this mechanism. For the LRS of both samples, it can be considered that the direct tunneling conduction is too large to represent the behavior of other conductions. The resistance switching behavior using nanogaps is independent of the substrate.$^{16,17}$ These results predict that an excellent thermally robust memory may be realized using Pt nanogaps, the substrate of which is selected to avoid leak-current behavior.

In conclusion, we studied the temperature dependence of conduction mechanisms in Pt nanogaps. On/off ratios were maintained at values above 100 at 773 K; however, the HRS was altered as the temperature increased. The alteration was caused in stress-induced SiO$_2$ substrates and can be neglected by etching the SiO$_2$ layer just under the nanogap. We demonstrated that an excellent thermally robust memory can be realized using the etched Pt nanogap over a wide temperature range from room temperature to 773 K.

**Acknowledgments** This work was supported by JST CREST Grant Number JPMJCR1532 and JSPS KAKENHI Grant Number 17K14100, Japan. The fabrication of the materials in this study was partly supported by the AIST Nano-Processing Facility.

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**Table I.** Comparison of results from Fig. 3(a) with those from SILC in Ref. 26 when current was increased from 300 to 400 K. Relative electric fields were estimated by dividing the applied voltages by the SiO$_2$ width.

|                  | This work | SILC in Ref. 26 |
|------------------|-----------|-----------------|
| Current increases from 300 to 400 K (A) | $8.6 \times 10^{-10}$ | $9.9 \times 10^{-10}$ |
| Applied voltage (V)   | 0.5       | 3.5            |
| SiO$_2$ width (nm)    | 0.79      | 5.5            |
| Relative electric field (V/nm) | 0.63      | 0.64          |

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