Design of high-resolution digital-to-analog converter for 14-bit successive-approximation analog-to-digital converter

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Abstract- Digital to Analog Converter (DAC) is the essential block to convert a digital input signal into an analog signal. The switching technique is the important parameter that will affect the performance of DAC were to ensure the analog output signal can be obtained without any missing code. The capacitor DAC is the most famous architecture used to design the DAC and it produces high power efficiency. But, the number of unit capacitors in DAC increase exponentially due to the increase of resolution, and a DAC block occupies the largest area among many internal blocks in the Successive Approximation Register (SAR) Analog to Digital Converter (ADC). The DAC was designed for 14-bit SAR ADC using a hybrid RC DAC architecture. The design of DAC has been carried out by using the 0.18µm CMOS Silterra process Technology. The simulation results are done with a 3.3V voltage supply and obtained DNL within -0.39 LSB to 0.235 LSB. It occupies an area of 0.76mm^2.

1. Introduction

A wide variety of Analog to Digital Converters (ADCs) exist with differing resolutions, area, speed, architecture, and power requirements. The most popular ADC architectures available today are SAR, Flash, Pipelined, and Sigma-Delta (SD). Each type of ADC has its advantages and disadvantages. The SAR ADC was suitable for 14-bit of resolution in terms of area compared with the flash ADC which is better in terms of speed. Compare with other types of ADC, SAR ADCs exhibit the best energy efficiency for medium to high speed, moderate resolution and low power application [1]. The high resolution and low power ADC are high demand due to the advancement of large-scale integrated circuits [2]. Digital to Analog Converter (DAC) is an important block in SAR ADC, where it would control the energy consumption and area while increasing the accuracy of the SAR ADCs [3]. Nowadays, several types of DACs have been designed to achieve a high resolution such as binary-weighted capacitor DAC, split array capacitor DAC, thermometer DAC. However, the area of capacitor array was increased exponentially due to the increasing of resolutions. One of the techniques to reduce the area is to minimize the value of the unit capacitor but it can cause the degradation of linearity performance [4]. The large unit capacitor can be used to overcome this issue. Most importantly, the Differential Non-linearity (DNL) of DAC should be less than +/-0.5 Least Significant Bit (LSB) to guarantee no missing code. The formula for the LSB and DNL can be simplified as Equation 1 and 2.

\[ V_{LSB} = \frac{V_{FS}}{2^N} \]  

(1)
where,
\[ V_{FS} = \text{full scale output voltage for the DAC} \]
\[ N = \text{the DAC resolutions} \]

\[ DNL = \frac{R_{VLSB} - I_{VLSB}}{I_{VLSB}} \]  \hspace{1cm} (2)

where,
\[ R_{VLSB} = \text{real voltage least significant bit} \]
\[ I_{VLSB} = \text{ideal voltage least significant bit} \]

In this paper, a hybrid RC DAC for 14-bit SAR ADC was designed to achieve a compact area with high accuracy. The combination of 10-bit of resistor string DAC with 4-bit of binary-weighted has been proposed to minimize the value of the capacitor unit.

2. System Level

This section discussed several architectures that have been designed in order to achieve a high-resolution DAC. The first architecture that has been designed is the combination 7-bit of resistor string DAC and 7-bit of binary-weighted capacitor DAC. The output of fifth, sixth and seventh bit for capacitor DAC is the worse results with the DNL above 1 LSB. Next, it comes out with the second design, which is the same bit for resistor string DAC and the split array capacitor DAC (4-bit LSB and 3-bit MSB) has been implemented with the obtained DNL about +/- 0.9. The area can be reduced by implementing the split array capacitor, but the performance becomes decreases. From that, it can be observed that the capacitor unit should be reduced and used for 4-bit only. But, the number of resistors use for resistor string DAC would be increased to 1024 units for 10-bit resolutions. The output obtained with the worse results because of the largest unit resistor and switch. By using segmented architecture which is main and sub resistor string DAC can reduce the unit resistor uses. The arrangement of the resistor is divided into two parts, such as 5-bit for main DAC and 5-bit for sub-DAC. All the simulated designed as shown in Table 1.

### Table 1. The simulated design

| Design          | First    | Second       | Third     | Forth        |
|-----------------|----------|--------------|-----------|--------------|
| Resolution (bit)| 7        | 7            | 10        | 5+5          |
| Resistor        | resistor string | resistor string | resistor string | 5bit main + 5bit sub resistor string |
| Resolution (bit)| 7        | 4+3          | 4         | 4            |
| Capacitor       | binary-weighted | split array  | binary-weighted | binary-weighted |
| DNL (LSB)       | above +1 | about +/-0.9 | worst     | about +/-0.5 |
3. DAC Design

This section discussed the DAC design that consists of 4-bit Binary Weighted CDAC, 10-bit resistor string DAC and 14-bit Hybrid RC DAC. The extra circuit is required to control the input that will enter each block of DAC.

3.1 4-bit Binary Weighted CDAC

The 4-bit binary-weighted CDAC consists of five-set main capacitors in parallel for each bit, such as 8C, 4C, 2C, 1C, and Cdummy. One capacitor unit is used for the first bit, two of the capacitor units for the second bit, four capacitor units for a third bit and eight capacitors binary-weighted for the fourth bit. This design has been added with twenty dummy capacitors with the symmetrical arrangement to protect the other capacitor during the tape out process. Each bit of the connection has been controlled by the switch that has three input voltage supply such as Vrefp, Vrefn, and Vindac as in Figure 1. Two switches are used for the dummy capacitors where one switch is controlled by phi1 and the other switch is controlled by phi2 that would allow the output signal from RDAC.

![Figure 1. 4-bit Binary Weighted CDAC](image)

3.2 10-bit resistor string DAC

A 10-bit resistor string DAC consists of 5-bit main string DAC and 5-bit sub string DAC as shown in Figure 2. The resistor in two strings must be equal, except that the top resistor in the MSB string be smaller of the value of the others. The LSB string consists of 31 resistors rather than MSB string which is 32 resistors. Usually, the worst case for this design is the transition code from substring DAC to the main string DAC due to the loading effect of the substring DAC. The unit of resistor that has been used for this design as mentioned in Table 2.

| Table 2. The resistor unit used for this design |
|-----------------------------------------------|
| Resistor (unit) | Switch (unit) |
| Main string DAC | 33 | 33 |
| Sub string DAC  | 31 | 32 |
Figure 2. 10-bit resistor string DAC

Figure 2 show the connection for 5-bit main string and 5-bit sub string DAC. The first switching network when the voltage supplied across a selected resistor at the main string and across the sub resistor string. The resistor in the sub string produce voltages by the current flow from the main string to the sub string through the first switching networks. The voltage across the sub string network from first resistor to the next resistor by sequent. The connection switch controlled the resistor string DAC in Figure 2 that using several of logic gates to ensure only the desired switch would be closed at that time. The SM switch is the switches for MSB which is the main string and SL switch is the switches for LSB which is the sub string. The desired closed switch as shown in Table 3.

Table 3. The closed switch for each code

| Code          | Closed switches |
|---------------|-----------------|
| 00000 00000   | SM0, SM1, SL0   |
| 00000 00001   | SM0, SM1, SL1   |
| 00000 00010   | SM0, SM1, SL2   |
| 00000 00011   | SM0, SM1, SL3   |
| 11111 11101   | SM31, SM32, SL2 |
| 11111 11110   | SM31, SM32, SL1 |
| 11111 11111   | SM31, SM32, SL0 |
The switching waveform for SL and SM in Figure 3 and Figure 4 are based on the closed switch as mentioned in Table 3 where the SM0, SM1, and SL0 are closed for code 0. For the next code, status for SM0, SM1, and SL1 is closed. Status for SM0 and SM1 remain closed until the SL0 reach SL31. Next, SM0 would be opened where SM1 and SM2 start closed with SL31 and return to SL0. The switching process will continue until the end process where SM31 and SM32 are closed with SL0.

### 3.3 14-bit Hybrid DC DAC

The full design of Hybrid RC DAC consists of ten LSB by implemented 10-bit RDAC and 4-bit CDAC for the other four MSB. The signal would be pass through the resistor string DAC first and the output of the RDAC would be connected to one of the inputs at CDAC. Figure 5 shows the full schematic and connection for overall hybrid RC DAC.
4. Simulation Result

The proposed design is verified in a 14-bit SAR ADC with 0.18μm CMOS technology. The output signal and the DNL should be targeted about +/-0.5 to ensure no missing code. Based on output results as shown in Figure 6, it can be observed that the worst results that be obtained mostly during the transition code from RDAC to CDAC but not too critical. The step size for every stage is close to the exact LSB which is around 201.4μV for 14-bit resolution. The value can be verified by Equation 3

\[ V_{LSB} = \frac{3.3}{2^{14}} = 201.4\mu V \]  

(2)

The DNL that be obtained is about +0.235/-0.39 which achieve the desired value as shown in Figure 7. The total area of the DAC is 0.76mm² (808.275μm x 938.64μm) included the switching digital logic for both resistor and capacitor DAC where 0.03mm² (177.625μm x 178.79μm) occupied by resistor string DAC and 0.44mm² (694.135μm x 637.38μm) for binary weighted capacitor DAC.
In this section discussed the performance comparison of several previous architectures in term of resolution, voltage supply and DNL. In [4] present an asynchronous rail-to-rail pipeline SAR ADC which consist of 6-bit for the first stage and 6-bit for the second stages. This architecture obtained the DNL within -0.676 LSB to +0.536 LSB with 1.8 of power supply. The hybrid RC DAC architecture that has been implemented in [5] use 2.8V of power supply with 0.18um CMOS technology. This architecture was designed using 5-bit for RDAC and 7-bit for CDAC while obtained the DNL within -0.48 LSB to +0.47 LSB. Architecture in [6] use 1.2V of power supply with 0.028um CMOS technology to implemented split array CDAC with linear calibration at the end of that process. The DNL that has been obtained before calibration are within -1 LSB to +0.69 LSB and after calibration are within -0.89 LSB to +0.51 LSB. Table 4 shows the comparison of the resolution, power supply and DNL for each works.
Table 4. Performance comparison with the previous architecture

| Author       | [4]  | [5]  | [6]  | This work |
|--------------|------|------|------|-----------|
| Technology (um) | 0.18 | 0.18 | 0.028 | 0.18      |
| Resolution (bit) | 12   | 12   | 12   | 14        |
| Voltage Supply (V) | 1.8  | 2.8  | 1.2  | 3.3       |
| DNL (LSB)     | +0.536/-0.676 | +0.47/-0.48 | +0.51/-0.89 | +0.235/-0.39 |

5.0 Conclusion

In this work, a high-resolution hybrid RC DAC for 14-bit SAR ADC was designed in 0.18μm CMOS technology under Silterra model library. A hybrid RC topology is implemented for DAC with appropriate switching method to minimize the number of unit capacitors and achieve the 14-bit linearity. The architecture of RDAC only utilizes 64 unit of resistor and 65 unit of switch which less than previous architecture. There are sixteen-unit capacitor has been used for CDAC architecture to perform the desired results. The proposed design was simulated with 3.3V power supply and 5MHz of frequency. The measure results show that the hybrid RC DAC achieves the DNL about +0.235/-0.39 which achieve the targeted value about +/-0.5 LSB with 0.76mm² of area.

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