A64FX – Your Compiler You Must Decide!

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Abstract—The current number one of the TOP500 list, Supercomputer Fugaku, has demonstrated that CPU-only HPC systems aren’t dead and CPUs can be used for more than just being the host controller for a discrete accelerators. While the specifications of the chip and overall system architecture, and benchmarks submitted to various lists, like TOP500 and Green500, etc., are clearly highlighting the potential, the proliferation of Arm into the HPC business is rather recent and hence the software stack might not be fully matured and tuned, yet. We test 3 state-of-the-art compiler suite against a broad set of benchmarks. Our measurements show that orders of magnitudes in performance can be gained by deviating from the recommended usage model of the A64FX compute nodes.

1. Introduction

The HPC community has been testing Arm-based architectures for a few years now [1], [2], [3], and Supercomputer Fugaku [4] is the first large-scale system in the top-end of the TOP500 list, which demonstrates the competitiveness of Arm in a space which recently had been dominated by Intel, AMD, and Nvidia. The benefits of Arm CPUs paired with high bandwidth memory, as in the case of Fujitsu’s A64FX processor [5], for the HPC field are clear: (1) Arm CPUs are highly customizable, energy efficient, and there is an existing ecosystem of software, compilers, tools, etc., which is readily available (unlike for the K computer with its SPARC CPU); and (2) most applications executed on HPC systems tend to be memory-bandwidth-bound, as we have shown in a previous study [6]. Although, a different compute-to-bandwidth ratio, as found in A64FX, might challenge this view in individual cases resulting in a greater influence by the compiler onto the performance. Furthermore, despite the dominance of Arm chips in the embedded and low-power space, the system software and compilers, such as the widely used GNU Compiler Collection for embedded systems, might be tuned for metrics other than wide vectors (e.g., Arm’s Scalable Vector Extension) and high performance.

It is known among benchmarkers and performance analysts, that Intel’s Parallel Studio or AMD’s AOCC compilers, depending on the CPU vendor, usually yield a high baseline performance. However, for Fujitsu’s A64FX, this choice is not that obvious, yet, and options such as Fujitsu’s compiler suite, GNU Compiler Collection, Arm compilers, and HPE/Cray compilers exist, and need to be evaluated.

For example, after Supercomputer Fugaku—or short Fugaku hereafter—was put into production, we experimented with micro kernels, namely PolyBench [7], to debug some unexpected performance discrepancies, especially when compared to an Intel Xeon E5-2650v4 reference CPU. While a compiler-based core-to-core comparison for these single-threaded benchmarks is inherently inaccurate (due to ISA, caches, GHz, etc.), we did not expect the Xeon to execute some tests up to two orders of magnitude faster, see Figure 1. This obviously does not make sense, especially when looking at the 2mm and 3mm matrix multiplication cases which should be compute-bound. We will analyze the reasons in greater depth in Section 3.1, and it initiated this study in which we seek to answer the following questions:

- Is the recommended usage model for A64FX, i.e., compiler+flags as well as number of MPI/OMP ranks and threads, ideal or just a starting point?
- Is there a “silver bullet” compiler choice for A64FX?
- Can performance differences, compared to similar x86-based hardware, be attributed to the compiler?

To answer these questions, our contributions are as follows:

- We execute a broad set of micro benchmarks, procurement proxy applications, and real-world application benchmarks under 5 different compiler environments to determine performance trends.
- A detailed discussion of the performance opportunities arising from different compiler options (which can also create challenges for ordinary users), and recommendations for operators and users of A64FX.
2. Measurement Methodology

The performance discrepancy for the 2mm benchmark was quickly identified. Intel’s C compiler reordered the nested loop construct, while Fujitsu’s C compiler (fch) failed to do so, resulting in a 64x speedup on the Xeon core which has less than ½ of a A64FX cores’s theoretical peak flop/s. Hence, we started investigating alternative compilers to improve PolyBench and also real-world codes on Fugaku.

2.1. Compiler and Compiler Flags

FUJITSU Software Technical Computing Suite (v4.5.0) is the recommended compiler infrastructure for Fugaku supporting C/C++ and Fortran. It supports two modes, traditional and clang, the latter being based on an enhanced version of LLVM 7. We utilize both modes in this study, and link to Fujitsu’s SSL2 library for linear algebra operations whenever necessary. Most application come with build scripts tuned for individual compilers, and we augment them with -Kfast,ocl,largepage,lto for performance, optimization control line (OCL) support, huptages, and link-time-optimization, respectively.

LLVM Compiler Infrastructure (v12) supports C/C++ via clang; however, flang (LLVM’s Fortran frontend) requires currently a host compiler and we experienced many errors using it, and hence we skip flang and directly utilize Fujitsu’s frt compiler. We test two settings with LLVM, the first being -Ofast -ffast-math -fno-strict-aliasing, and the second specifically targeting polyhedral optimizations with -mllvm -poly -mllvm -polly-vectorizer=polly and replacing the thin linker with the full linker, since thin interfered with polly.

GNU Compiler Collection (v10.2.0) supports C/C++ and Fortran, and we use -O3 -march=native -mllvm -polly -mllvm -polly-vectorizer=polly and replacing the thin linker with the full linker, since thin interfered with polly.

2.2. Benchmarks – From Micro to Macro Level

We test over 100 different kernels and scientific codes from 7 benchmark suites, as outlined hereafter:

Micro Kernels are a collection of 22 kernels extracted from RIKEN priority applications (see later in this Section), which have been used during the Fugaku development for testing and validation. These kernels are OpenMP-parallelized, primarily written in Fortran (except 5), and test various performance-relevant aspects of one core memory group (CMG) of the A64FX processor, i.e., 12 cores (+1 assistant/OS core) and a 8 GiB HBM2 module.

Polyhedral Benchmark suite (in short, PolyBench) is a collection of 30 single-threaded scientific kernels written in C. The input sizes can be tuned for different memory hierarchy levels, and we use the LARGE input (exc.: MEDIUM for floyd-warshall) to stress all memory levels of A64FX.

HPL, HPCG, and BabelStream are commonly known to test the system’s compute [8] and memory performance [9], [10], and are used, for example, to rank supercomputers in the TOP500 list. HPL’s and HPCG’s problem sizes are configured to 36,864 and 120^3, respectively, while we use 2 GiB long vectors for the stream benchmark.

ECP proxy-apps and RIKEN Fiber mini-apps are collections of so called proxy applications which are smaller representative codes and inputs for production applications commonly executed on supercomputers in the USA and Japan. We have studied these codes previously [6], [11], and we refer the reader to these publications for details.

SPEC CPU[speed] and OMP are two suites used by HPC centers and vendors to test compute node capabilities. The former comprises 20 tests. One half are single-threaded, integer-intensive computations and the other half tests multi-threaded, floating-point-heavy scientific applications. The latter are 14 science workloads which are OpenMP-parallelized, too. The benchmarks are implemented in C, Fortran, and C++, or a mix thereof. For our (non-compliant) SPEC runs, we universally select the train-ing input sizes.

2.3. Evaluation Environment

All test are performed on 2.2 Ghz A64FX-based nodes of Fugaku [4], [5], and the benchmark’s files are cached to the first-layer storage (a SSD shared among 16 nodes) prior to its execution. We have disabled all power-saving features, and other settings which could limit the performance of individual benchmarks. Furthermore, we submitted all runs to the batch system with the --mpiprocspernode=<n> setting, to instruct the Fujitsu’s MPI runtime to appropriately map the ranks and threads to the CMGs cores of A64FX, i.e., spread and close, respectively. The exception to this rule is PolyBench, whose tests are pinned to one core, and SPEC which comes with its own execution environment. For SPEC, we followed a colleague’s recommendation to further tune the large page settings via XOS_MMM_L_PAGING_POLICY=demand:demand:demand and XOS_MMM_L_ARANALOCK_TYPE=0, and specify OMP_PROC_BIND=close, but left these settings at default values for all other benchmarks.

While theoretically possible, we note that tuning all our 100+ benchmarks individually with the full range of compiler flags, runtime parameters, and manual code refactoring, etc., for optimal performance is outside the scope of this work, which seeks to identify or disproof the existence of a “silver bullet” compiler for the A64FX processor.

1. Compilation scripts & inputs available: github.com/domke/a64fxCvC
2. Source code: github.com/RIKEN-RCCS/fs2020-tapp-kernels; We use earlier snapshot; Referencing them with Kernel 1...22 to avoid confusion.
2.4. Measurement Approach and Metrics

While Fujitsu’s and RIKEN’s recommendation for Fugaku and A64FX is 4 ranks (one per CMG) and 12 OpenMP threads per rank per node, this may not always be ideal, since some codes prefer or even require a power-of-2 for ranks/threads (e.g., SWFFT) or do not scale with many of threads (e.g., SPEC imagick’s sweet spot is 8 threads). Hence, we employ a exploration phase for each compiler and test various MPI and/or OMP combinations for all parallelized, strong-scaling benchmarks (except: weak-scaling MiniAMR and XSbench), using 3 trial runs each. The fastest time-to-solution determines the final MPI/OMP setting (individual per compiler) for the performance runs, which we run again 10 times. We manually instrumented all benchmarks to only report the time-to-solution of the region of interest, i.e., excluding any pre/post-processing phases; except for SPEC CPU/OMP where we rely on SPEC’s runtime reporting. Performing 10 runs should suffice, since we expect low run-to-run variability on A64FX. For example, AMG’s coefficient of variation (CV) in runtime was below 0.114%, and we only see high variability in BellStream with a CV of up to 22% which is still noticeably smaller than the gap between compilers.

3. Evaluation and Result Discussion

We report the fastest runtime across 10 performance runs (cf. Sec. 2.4), and relative comparisons to the recommended compiler, i.e., using Fujitsu’s compiler suite in trad mode. Figure 2 is additionally color-coded with the relative performance gain (see [12]) of each compiler over the FJtrad baseline, with white for similar runtime and dark green indicating 2x speedup. Benmarks exhibiting over 2x speedup are further signalized with a bold name. Furthermore, unsolvable compilation errors, runtime errors, and invalid runs are encoded in dark pink. Additionally, we added the best parallelization configuration, i.e., shown via [#MPI ranks | #OMP threads] for each compiler/benchmark combination, except for the micro, PolyBench, and SPEC CPUInt for which it is universal and written in the header.

3.1. Micro Kernels and Polybench

For the Micro Kernels representing RIKEN’s priority apps, we clearly see the results of the co-design efforts for Fugaku. Fujitsu’s compiler in traditional mode outperforms all other compilers in nearly all test. Only the GNU compiler is able to noticeably beat FJtrad in 4 of the 22 tests, but also produces 6 executables which result in runtime errors. Assuming that we switch always to the best compiler option, then we could reduce the runtime by 17% on average, with a median of 0%, and peak of 2.4x improvement. However, for PolyBench the roles reverse, with LLVM+Polly showing the best results, followed by FJclang in some cases. Especially for mvt the polyhedral optimizations resulted in over 250.000x speedup. Choosing the best compiler over FJtrad
results in a median speedup of 3.8x. It remains to be seen if polly’s gains translate to “real” scientific codes hereafter.

3.2. TOP500, ECP, and Fiber Proxys

HPL gains a minor advantage (≈5%) by using LLVM over Fujitsu’s compilers, despite that most of the calculations are performed within SSL2, which holds true for the convolution kernel of the deep learning proxy, too. BabelStream shows the largest gain from switching to LLVM or GNU with up to 51% lower runtime. With a few exceptions, like FFB and mVMC, Fujitsu dominates the other compilers on Fiber mini-apps, which is consistent with the Micro Kernel results shown earlier. For ECP proxy-apps the conclusions reverses, and the user would be advised to switch to LLVM or GNU in almost all cases. Such a change leads to an average speedup of 1.65x (median 1.09x). The 6.7x speedup for XSBench is salient, because it also demonstrates that polly can have an impact on real workloads.

3.3. SPEC CPU and OMP

The SPEC measurements reveal multiple interesting insights. Firstly, FJtrad outperforms any Clang-based alternative on A64FX on integer-intensive codes; however, the GNU compiler almost universally beats FJtrad at the same single-threaded workloads. We speculate that this advantage is partially a result of GNU’s prevalence in the embedded space where many of the Arm CPUs have no floating-point units, and also a result of Arm’s continued investments into the open-source GNU compilers [13]. By contrast, for multi-threaded and floating-point-based SPEC CPU workloads, as well as SPEC OMP, the GNU compiler is currently the worst choice on A64FX. Furthermore, many of the applications are written in Fortran, and hence there is little benefit (apart from maybe link-time-optimizations) for switching to LLVM. For C/C++ applications on the other hand, LLVM-based compilers (incl. FJclang), and GNU in a few cases, can yield a runtime benefit over FJtrad. We see speedup as high as 16.5x in SPEC OMP simply by switching compilers (e.g., for kdtree), with an average improvement of 49% in SPEC CPU and 2.5x speedup in SPEC OMP. The median runtime improvement from choosing the best compiler across both SPEC suites is 14%.

Overall, across all 108 benchmarks and realistic workloads, we see that a median runtime improvement of 16% is possible by selecting an appropriate compiler, without any changes to the source code or other tuning methods.

4. Related Work

Various publications and reports of A64FX evaluations have been released recently. For example, [14] tested LLVM and its SVE code generation capabilities for DCA++, and [15] compared a limited set of applications with LLVM, GNU, ARM, and Cray compilers and focused on SVE and multi-node scaling. Similarly, [16] investigated OpenMP-scaling of 3 proxy apps on A64FX while comparing 5 compilers, and [17] measured nearly a dozen proxy apps (different from ours) on ARM and x86 for multiple compilers, but lacked LLVM. In [18], the authors analyzed the achievable bandwidth for a set of memory-bandwidth-bound kernels using GNU, and [19] reported a 2x performance advantage of GNU compilers for the E3SM climate code. Lastly, the studies [4], [20], [21] compare A64FX with Fujitsu’s traditional mode to ARM-based ThunderX2 and Intel Xeon CPUs using various priority apps and proxies. All these studies are complementary to our comprehensive compiler comparison for a wide variety of workloads, since they use different apps, compilers, or evaluation approaches.

5. Conclusion

In conclusion, we demonstrate a clear benefit from exploring alternative compilers for the A64FX CPU as a valid first-order tuning method before investing a considerable amount of effort into testing “exotic” compiler flags, environment variables, and performing manual code refactoring. Especially, the performance discrepancy for PolyBench, which we show in Figure 1, was solved by switching from the recommended FJtrad to LLVM 12 compiler, but the polly optimizations seem rarely applicable or beneficial outside this benchmark set. To revisit our initial question, we could not identify a “silver bullet” compiler for A64FX, but our measurements give indications for which compilers work well in which situations, i.e., Fujitsu for Fortran codes, GNU for integer-intensive apps, and any clang-based compilers for C/C++. Furthermore, we noticed that for “legacy” applications, the recommended usage model of 4 ranks and 12 threads per A64FX node results in suboptimal time-to-solution more often than not, and that the Arm software ecosystem for HPC is not as mature as for x86, yet.

Our work is just one among many similar, early explorations of the newly introduced Arm-base CPU for high-performance computing, but it gives reason to believe that potential performance deficiencies, when directly compared against x86 for the same applications, are most likely the results of immature compilers. Hence, our recommendation to administrators and users of A64FX-based supercomputers is to install and test as many different, available compilers as possible to extract the true performance potential from the A64FX CPU. Similarly, it could be worthwhile to revisit how various system libraries, such as for searching, sorting, routing, or MPI libraries, etc., and other OS packages are (pre-)compiled for the A64FX processor.

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References

[1] N. Rajovic, P. M. Carpenter, I. Gelado, N. Puzovic, A. Ramirez, and M. Valero, “Supercomputing with Commodity CPUs: Are Mobile SoCs Ready for HPC?” in Proceedings of the International Conference on High Performance Computing, Networking, Storage and Analysis, ser. SC ’13. New York, NY, USA: Association for Computing Machinery, 2013, event-place: Denver, Colorado.

[2] N. Rajovic, A. Rico, F. Mantovani, D. Ruiz, J. O. Vilarribi, C. Gomez, L. Backes, D. Nieto, H. Servat, X. Martorell, J. Labarta, E. Ayguade, C. Adeniyi-Jones, S. Derradij, H. Glaouaqen, P. Lanucara, N. Sunnu, J.-F. Mehaut, K. Pouget, B. Videau, E. Boyer, M. Allalen, A. Auweter, D. Brayford, D. Tafani, V. Weinberg, D. Börmel, R. Halver, J. H. Meinke, R. Beivide, M. Benito, E. Vallejo, M. Valero, and A. Ramirez, “The Mont-Blanc Prototype: An Approach for HPC Systems,” in SC ’16: Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis, 2016, pp. 444–455.

[3] A. Rico, J. A. Joao, C. Adeniyi-Jones, and E. Van Hensbergen, “ARM HPC Ecosystem and the Reemergence of Vectors: Invited Paper,” in Proceedings of the Computing Frontiers Conference, ser. CF ’17. New York, NY, USA: Association for Computing Machinery, 2017, pp. 329–334.

[4] M. Sato, Y. Ishikawa, H. Tomita, Y. Kodama, T. Odajima, M. Tsuji, H. Yashiro, M. Aoki, N. Shida, I. Miyoshi, K. Hirai, A. Furuya, A. Asato, K. Morita, and T. Shimizu, “Co-Design for A64FX Many-core Processor and “Fugaku”,” in Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis, ser. SC ’20. IEEE Press, 2020, event-place: Atlanta, Georgia.

[5] Fujitsu Limited, “FUJITSU Processor A64FX.” [Online]. Available: https://www.fujitsu.com/downloads/SUPER/a64fx/a64fx_datasheet_en.pdf

[6] J. Domke, K. Matsumura, M. Wahib, H. Zhang, K. Yashima, T. Tsuchikawa, Y. Tsuji, A. Podobas, and S. Matsuoka, “Double-precision FPUs in High-Performance Computing: an Embarrassment of Riches?” in 2019 IEEE International Parallel and Distributed Processing Symposium, IPDPS 2019, Rio de Janeiro, Brazil, May 20-24, 2019, Rio de Janeiro, Brazil, May 2019.

[7] L.-N. Pouchet and M. Taylor, “PolyBench/C 4.2.1 (beta),” May 2016. [Online]. Available: https://sourceforge.net/projects/polybench/

[8] J. Dongarra, “The LINPACK Benchmark: An Explanation,” in Proceedings of the 1st International Conference on Supercomputing, London, UK, UK: Springer-Verlag, 1988, pp. 456–474. [Online]. Available: http://dl.acm.org/citation.cfm?id=647970.742568

[9] J. Dongarra, M. Heroux, and P. Luszczek, “HPCG Benchmark: A New Metric for Ranking High Performance Computing Systems,” University of Tennessee, Tech. Rep. ut-ecs-15-736, Jan. 2015. [Online]. Available: https://library.eecs.utk.edu/pub/594

[10] T. Deakin, J. Price, M. Martineau, and S. McIntosh-Smith, “GPGPU-STREAM v2.0: Benchmarking the Achievable Memory Bandwidth of Many-Core Processors Across Diverse Parallel Programming Models,” in High Performance Computing, M. Tauer, B. Mohr, and J. M. Kunkel, Eds. Cham: Springer International Publishing, 2016, pp. 489–507.

[11] J. Domke, E. Vatali, A. Drozd, C. Peng, Y. Oyama, L. Zhang, S. Salaria, D. Mukuno, A. Podobas, M. Wahib, and S. Matsuoka, “Matrix Engines for High Performance Computing: A Paragon of Performance or Grasping at Straws?” in 2021 IEEE International Parallel and Distributed Processing Symposium, IPDPS 2021, Portland, Oregon, USA, May 17-21, 2021, Portland, Oregon, USA, May 2021, p. 10.

[12] T. Hoeffer and R. Belli, “Scientific benchmarking of parallel computing systems: twelve ways to tell the masses when reporting performance results,” in Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis, ser. SC ’15, Austin, TX, USA, Nov. 2015, pp. 731–7312.

[13] T. Christina, “Blog Post: Significant performance improvements in GCC 10 through Vectorization and In-lining,” May 2020. [Online]. Available: https://community.arm.com/developer/tools-software/tools/b/tools-software-ides-blog/posts/gcc-10-better-and-faster

[14] J. Huber, W. Wei, G. Georgakoudis, J. Doeffert, and O. R. Hernandez, “A Case Study of LLVM-Based Analysis for Optimizing SIMD Code Generation,” Tech. Rep. arXiv:2106.14332v1, 2021. [Online]. Available: https://arxiv.org/pdf/2106.14332.pdf

[15] A. Burford, A. C. Calder, D. Carlson, B. M. Chapman, F. CoSkun, T. Curtis, C. Feldman, R. J. Harrison, Y. Kang, B. Michalow-Icz, E. Raut, E. Siegmann, D. G. Wood, R. L. DeLeon, M. Jones, N. A. Simakov, J. P. White, and D. Orysypow, “Ookami: Deployment and Initial Experiences,” Tech. Rep. arXiv:2106.08987v1, 2021. [Online]. Available: https://arxiv.org/pdf/2106.08987.pdf

[16] B. Michalowicz, E. Raut, Y. Kang, T. Curtis, B. M. Chapman, and D. Orysypow, “Comparing the behavior of OpenMP Implementations with various Applications on two different Fujitsu A64FX platforms,” in Practice and Experience in Advanced Research Computing, ser. PE ARC ’21. New York, NY, USA: Association for Computing Machinery, 2021.

[17] A. Poenaru, “An Evaluation of the Fujitsu A64FX for HPC Applications,” Presentation in AHUG ISC 21 Workshop, Jul. 2021. [Online]. Available: https://a-hug.org/isc-2021-event/

[18] C. Alappat, J. Lautemann, T. Gruber, G. Hager, G. Wellein, N. Meyer, and T. Wettig, “Performance Modeling of Streaming Kernels and Sparse Matrix-Matrix Multiplication on A64FX,” in 2020 IEEE/ACM Performance Modeling, Benchmarking and Simulation of High Performance Computer Systems (PMBS), 2020, pp. 1–7.

[19] S. Sreepathi, O. Guba, and M. Taylor, “E3SM Pathfinding on Fugaku,” May 2021. [Online]. Available: https://e3sm.org/e3sm-pathfinding-on-fugaku

[20] A. Jackson, M. Weiland, N. Brown, A. Turner, and M. Parsons, “Investigating Applications on the A64FX,” in 2020 IEEE International Conference on Cluster Computing (CLUSTER), Los Alamitos, CA, USA: IEEE Computer Society, Sep. 2020, pp. 549–558.

[21] T. Odajima, Y. Kodama, M. Tsuji, M. Matsuda, Y. Manuyama, and M. Sato, “Preliminary Performance Evaluation of the Fujitsu A64FX Using HPC Applications,” in 2020 IEEE International Conference on Cluster Computing (CLUSTER), 2020, pp. 523–530.