Module-per-Object: a Human-Driven Methodology for C++-based High-Level Synthesis Design

Jeferson Santiago da Silva, François-Raymond Boyer and J.M. Pierre Langlois
Polytechnique Montréal, Canada
{jefferson.silva, francois-r.boyer, pierre.langlois}@polymtl.ca

Abstract—High-Level Synthesis (HLS) brings FPGAs to audiences previously unfamiliar to hardware design. However, achieving the highest Quality-of-Results (QoR) with HLS is still unattainable for most programmers. This requires detailed knowledge of FPGA architecture and hardware design in order to produce FPGA-friendly codes. Moreover, these codes are normally in conflict with best coding practices, which favor code reuse, modularity, and conciseness.

To overcome these limitations, we propose Module-per-Object (MpO), a human-driven HLS design methodology intended for both hardware designers and software developers with limited FPGA expertise. MpO exploits modern C++ to raise the abstraction level while improving QoR, code readability and modularity. To guide HLS designers, we present the five characteristics of MpO classes. Each characteristic exploits the power of HLS-supported modern C++ features to build C++-based hardware modules. These characteristics lead to high-quality software descriptions and efficient hardware generation. We also present a use case of MpO, where we use C++ as the intermediate language for FPGA-targeted code generation from P4, a packet processing domain specific language. The MpO methodology is evaluated using three design experiments: a packet parser, a flow-based traffic manager, and a digital up-converter. Based on experiments, we show that MpO can be comparable to hand-written VHDL code while keeping a high abstraction level, human-readable coding style and modularity. Compared to traditional C-based HLS design, MpO leads to more efficient circuit generation, both in terms of performance and resource utilization. Also, the MpO approach notably improves software quality, augmenting parameterization while eliminating the incidence of code duplication.

I. INTRODUCTION

High-level synthesis (HLS) has opened doors to an audience unfamiliar with FPGA hardware design methodology. Indeed, HLS tools can convert high-level and untimed C-based code into a synthesizable register-transfer level (RTL) description, a task that once had to be manually done by hardware (HW) designers. The RTL design flow is known to be much slower than its counterparts in software (SW) [1], since it requires a detailed description of the desired micro-architecture, including synchronization schemes, pipelining, and parallelism. HLS tools, on the other hand, abstract away these micro-architecture aspects allowing a faster design space exploration (DSE) through a SW development flow.

However, achieving good Quality-Of-Results (QoR) in HLS environments is sometimes unintuitive and, in some cases, not straightforward at all. In the HW design context, the ratio between performance and design cost normally defines the QoR standard for a given circuit. In FPGA design, high performance is normally associated with throughput and latency, while design cost refers to circuit area, energy consumption, and development time.

Efforts have been made to improve QoR with HLS with source-to-source transformations and code restructuring [11, 12]. While improving QoR, such approaches lower abstraction and make code maintenance and reuse more difficult. The latter two aspects are well-known problems in HLS design and they have been subject of research as well [3, 4].

Satisfactory HW QoR with HLS-based design and good SW engineering practices are often seen as incompatible [3, 6]. Indeed, the majority of HLS users are HW developers who translate RTL codes into sometimes awkward C-based descriptions. They attempt to reproduce RTL-level microarchitectural expressiveness while still accelerating the FPGA design cycle through HLS design flow. Such HW-oriented C descriptions lead to incomprehensible codes difficult to reuse by other designers.

Although existing HLS approaches can sometimes deliver good code readability and modularity, and still produce good results, this is most often not the case. Normally, HLS development trades off HW QoR and SW quality, following a sort of unidimensional view, as illustrated in Figure 1a. However, a bi-dimensional HLS approach is required. Indeed, a bi-dimensional perspective highlights independence between HW QoR and SW quality. Figure 1b shows the design space of this novel bi-dimensional HLS view. In fact, in the course of this work, we show that using our approach, it is possible to increase HW QoR and SW quality simultaneously by employing modern and high-quality C++ constructs, which leads to cleaner codes and reduces duplication.

In this context, we present design guidelines for C++-based HLS design targeting both HW and SW designers. We present several C++ high-level constructs and, whenever possible, we show their correspondence in the generated HW. The HLS methodology we propose is called Module-per-Object (MpO). It is meant to be human-driven and used by ordinary programmers with limited HW expertise, not only by FPGA experts. We aim to close the gap between QoR and code modularity and readability. We use the results obtained by traditional HLS design as HW QoR metric. We focus on code modularity and readability as SW quality metrics. Code modularity is evaluated by the capability of reuse of a given module while code readability is related to the code expressiveness and conciseness.

As a final goal, we intend to widen FPGA usage by SW programmers by raising the FPGA development abstraction. Indeed, higher design abstractions allow programmers to use a single version of their code to run on an x86 CPU or be synthesized for an FPGA device [2]. To do so, we propose to exploit high-level modern constructs and the Standard Template Library (STL). Such constructs are well known by SW developers to improve code readability [6]. We target QoR and code readability and modularity by exhaustively employing templated classes and structures that can tune the C++ objects according to design needs. In addition, we discuss the possibility of adopting templated C++ classes as an intermediate language to be used alongside a Domain Specific Language (DSL). The main contributions of this work are as follows:

- A methodology called Module-per-Object, a design pattern for HLS-based FPGA development that simultaneously achieves...
high modularity, readability, and QoR (§ III);  
- The extensive use of synthesizable templated C++ data structures and constructs to improve QoR and modularity with HLS (§ III);  
- A case-study on using C++ as an intermediate language for automatic code generation of a packet parser written in the P4 language targeting FPGA implementation (§ IV-A);  
- Based on three specific use-cases, we have identified HLS tools deficiencies that prevent exploiting the full capabilities of high-level constructs, and we propose guidance for HLS designers and hints for future HLS tool releases (§ IV-B); and  
- An evaluation of the benefits brought by the proposed MpO approach on three design examples: a packet parser, a flow-based traffic manager, and a digital-up converter (§ V).

II. RELATED WORK

In this section, we present a review of recent related works. § II-A presents techniques and methodologies to improve QoR in HLS-based design. § II-B presents previous contributions related to high-level programming methodology applied in an HLS environment. Finally, in § II-C we review the use of high-level languages (HLLs) as an intermediate representation for FPGA design.

A. QoR Improvements in HLS-based Design

Recent works have targeted the improvement of QoR with HLS by applying code restructuring techniques and source-to-source transformations. The idea behind code restructuring is that one has to write a high-level code in a way they think it would resemble the HW [1]. Therefore, the programmer must have a good comprehension of hardware design and FPGA architecture to write FPGA-friendly code. Source-to-source transformations alleviate this burden by offering automatized frameworks to restructure the code towards an HW-friendly description.

Liang et al. [8] conducted a study on how to restructure C codes in order to improve QoR with HLS for several different benchmarks. Their results showed up to 126× performance improvement over a pure software implementation, which were obtained after various rounds of code refactoring and #pragma insertions, which requires extensive HW expertise. In addition, when comparing to hand-crafted RTL design, their results are up to 20× worse. Also, the authors affirm that, in some cases, improving QoR conflicts with good SW engineering practices. Matar et al. [11] presented a methodology for code restructuring with HLS targeting FPGA devices. They provide insights on how to combine FPGA-friendly coding style with proper #pragma insertion. However, the transformed codes are unintuitive and not portable. Similar research was conducted by Homsirikamol and Gaj [9] and Liu et al. [10]. Zhou et al. have presented Rosetta [11]. Rosetta is an open-source realistic benchmark suite for HLS-driven FPGA design. All benchmarks have been meticulously coded for FPGA implementation and tuned for state-of-the-art HLS tools. While such practices improve performance and reduce FPGA area, in most cases, the source code is unreadable for a non-FPGA expert.

Source-to-source transformations have been explored by Winterstein et al. [2]. The authors have proposed a framework that performs source-to-source transformations on the original C code in order to ensure synthesizability. The authors claim that the produced code is human-readable. Automated source-to-source transformations can result in descriptions that might not exactly match the original code. Gao et al. [13] and Cong et al. [14] have done similar research.

B. Raising the Abstraction Level in HLS

Cong et al. [7] have conducted a thorough study on HLS methods and tools. They have as well evaluated the performance of the former AutoESL’s Auto Pilot HLS tool. The authors have presented a design methodology for HLS-driven FPGA design, which includes code reusing practices through C++ templates.

Mück and Fröhlich [3, 4] have exploited advanced C++ constructs to create compatible codes for both CPUs and FPGA devices. Their method heavily employs metaprogrammed templated classes in order to provide the required degree of parameterization. Also, the authors present guidelines for FPGA-friendly pointer handling and static polymorphism implementation [15]. According to the authors, the resulting overhead in having reusable and modular unified C++ codes is worthwhile. The area and performance overhead are up to 30% and 50%, respectively, compared to HW-oriented C++ design. Our work leverages their ideas by employing several other C++ constructs and by comparing the achievable results with RTL implementations.

Thomas [15] has presented a DSL library targeting recursion with C++ HLS tools described using C++11 constructs. The author has shown how compile-time metaprogramming and lambda expressions can leverage HLS-driven HW design. Indeed, in our work, we have confirmed that such constructs can be used by HLS designers, eventually leading to higher QoR, while raising the abstraction. Similar research was conducted by Richmond et al. [17].

Zhao and Hoe [18] have assessed HLS-based flow in structural design. Their results for a network-on-chip implementation are comparable with a self-generated RTL approach. The area and performance results vary according to the network topology, ranging from +1% ∼+23% in lookup tables (LUTs), −71% ∼−54% in flip-flops (FFs), and −14% ∼+24% in clock frequency. Their approach does not explore in depth the capabilities of C++ constructs supported by the HLS tool, which improves code modularity and readability.

Oezkan et al. [19] have also exploited templated C++ classes to build an image processing library targeting FPGA devices. The authors make extensive use of templates to generate highly parameterizable C++ classes. One of their final remarks is that the more the code is written in a “hardware design manner”, the better its synthesis is. This “hardware manner” coding style lowers the abstraction, which could be alleviated by exploiting the potential of the available high-level constructs of the STL, augmenting thus code readability, avoiding code duplication, and improving code maintenance.

Modern HLS tools have a common approach for compiling high-level code into HW modules: a platform-independent front-end compiler, and a back-end compiler, where device-dependent optimizations are applied. Such optimizations, however, can be leveraged by the front-end optimization passes. The Clang compiler is a common
front-end used in commercial and academic HLS tools, such as Vivado HLS and LegUp \cite{20}. Vivado HLS was built upon a customized version of Clang where front-end optimizations cannot be configured. LegUp uses standard Clang as front-end compiler and does perform LLVM-level optimizations \cite{21, 22}.

C. HLLs as Intermediate Representation in an FPGA Design Flow

Other researchers have pointed to the use of DSLs for FPGA design \cite{24}. Although increasing the development abstraction, such languages need to be converted into synthesizable RTL code, a process similar to what is done by HLS tools. Examples of such DSLs can be found in most varied domains, ranging from signal and image processing to network applications.

In the network domain, several works have used HLLs, such as P4 \cite{24}, for FPGA implementation. P4FPGA \cite{25} is a framework for fast prototyping of network functions described in P4. While offering a complete compilation chain, P4FPGA uses BlueSpec Verilog as intermediate representation idiom, which requires a proprietary compiler to generate synthesizable RTL. A similar approach was proposed by Khan \cite{26} using off-the-shelf HLS tools, however, it is difficult to evaluate the real impact of this work due to the lack of details provided. While Emu \cite{27} is not used alongside a higher level network DSL, it could have been, since it comprises a set of standard network libraries written in C# in an object-oriented fashion that are compiled to Verilog using Kiwi \cite{28}. This approach is similar to what Silva et al. \cite{29} have done for a P4-compatible packet parser.

III. MPO HLS METHODOLOGY

The next subsections present the methodology followed in this work. First, an overview of the MPO methodology is presented. Then, we introduce a MPO use case. Finally, the five characteristics of an MPO base class are detailed in the following subsections.

A. Overview of the MPO Methodology

We propose the Module-per-Object (MPO) HLS methodology, in which we define the concept of “module” as a C++ object that logically represents a self-contained functional unit. To do so, this work exploits high-level constructs available in C++11, and that are supported by Xilinx Vivado HLS, to improve QoR while keeping a very high level of abstraction.

While previous works have dealt with the modularity or portability aspects in HLS design \cite{9, 10, 19} or have presented HLS methodologies for structural clock-accurate design \cite{13}, we leverage some of their insights with an STL C++-based HLS design towards QoR, code readability and modularity. Inspired by Cong et al. \cite{7}, Table I summarizes the C++ constructs for synthesis used in this work.

To increase code modularity and readability, our approach uses the concept of an MPO base class, which abstracts common functionalities between different modules. Consequently, this approach allows to reuse the same source code to describe functional modules with similar behavior. The five characteristics of an MPO class are as follows:

1) Templates: class parameterization and code modularity (§III-C);
2) Systematic utilization of const and constexpr variables for static objects (§III-D);
3) STL constructs: zero-overhead abstraction, code reuse and modularization (§III-E);
4) Inheritance and static polymorphism (when appropriate): code reuse and modularization (§III-E), and
5) Smart constructors: constant class members initialization (§III-G).

The main idea is to write generic code that is specialized at compile time. Generics codes, exploiting templates (1), STL constructs (3), and inheritance and static polymorphism (5), allows writing more compact and reusable code, reducing code duplication. Specialized objects also helps reducing resource usage by allowing specific pieces of hardware to be precisely inferred. Indeed, const and constexpr variables (2) give hints to the compiler to perform constant propagation that can be used in conjunction with smart constructors (5) for class member initialization.

B. Illustrative Use Case: a Packet Parser

As a use case, a packet parser is used to demonstrate the viability of the proposed methodology of this work. A packet parser determines the set of valid protocols supported by the device and extracts the required header fields that are to be matched in the packet processing pipeline.

A packet parser can be modeled at a high-level with a directed acyclic graph (DAG), where nodes represent protocols and edges are protocol transitions \cite{30}. A parser is implemented as an abstract state machine (ASM), performing state transition evaluations at each parser state. States belonging to the path connecting the first state to the last state in the ASM compose the set of supported protocols of a network equipment. A packet-processing language, such as P4 \cite{24}, can be used to describe such an ASM.

Listing 1: P4 description of a packet parser

```
Listing 1: P4 description of a packet parser

parser start { return parse_ethernet; }
state parse_ethernet {
extract (ethernet);
return select (ethernet.etherType) {
0x0800 : parse_ipv4;
0x86DD : parse_ipv6;
default : ingress;
}
}
state parse_ipv4 {
extract (ipv4);
return select (ipv4.protocol) {
0x11 : parse_udp;
0x86DD : parse_tcp;
default : ingress;
}
}
state parse_ipv6 {
extract (ipv6);
return select (ipv6.nextHdr) {
0x11 : parse_udp;
0x86DD : parse_tcp;
default : ingress;
}
}
state parse_udp { extract (udp); return ingress; }
state parse_tcp { extract (tcp); return ingress; }
```

Figure 2 shows a possible hardware realization of the parser graph described in Figure 2a. In the figure, the supported headers are processed in a pipelined-fashion. Headers that belong to the same graph level are placed in parallel in the pipeline layout. In this example, the packet parser processes five protocol headers, namely Ethernet, IPv4, IPv6, UDP, and TCP. All headers in this example have fixed size with the exception of IPv4, for which the size is only known when a packet is parsed.

For the sake of illustration, this example will be revisited several times throughout the following sections.

C. Specializing Classes with Templates

Templates are fundamental to correctly parameterize an MPO base class. Indeed, class templates allow generic code to be fine-tuned for
### Table I: Summary of C++ features used in this work

| Constructs                  | Benefits                                      | Version                  |
|-----------------------------|-----------------------------------------------|--------------------------|
| Fixed-point types           | Fixed-point arithmetic                        | C++98, vendor dependent  |
| (Variadic) Templates       | Parametrizable design                         | (C++11), C++98           |
| Classes                     | OO paradigm, encapsulation, inheritance, polymorphism | C++98                    |
| Template metaprogramming   | Compile-time calculation, Performance improvement | C++98                    |
| STL                         | Modularity, code reuse, standardization       | > C++98, in constant evolution |
| Data containers             | Data storage and encapsulation                | > C++98, in constant evolution |
| Algorithms                  | Standardization, code reuse                   | > C++98, in constant evolution |
| Iterators, range-based for loops | Syntax sugaring, easier container iteration | C++11                    |
| Lambda expressions          | Function pointer properties                    | C++11                    |
| constexpr variables and functions | Compile-time calculation, performance improvement | C++11                    |
| auto, decltype              | Automatic type inference                       | C++11                    |

### Figure 2: Representation of a packet parser

(a) Equivalent parser graph of the parser described in Listing 1

(b) Pipeline organization of the packet parser of Listing 1

---

Different design instances, favoring code reuse, reducing duplication while generating results compared to hand-tuned codes.

Referring to Figure 2a, the nodes of the parser graph share common properties and may share the same code, being a great starting point for an MpO base class. Listing 2 presents an example of an MpO base class that describes a node of the parser. For simplicity only relevant code fragments are shown and so cannot be compiled as is.

The class presented in Listing 2 is parameterized with four template parameters (line 2). The two first parameters are integers and they are used to configure the arbitrary-sized integers. T_HeaderLayout is a struct type derived from a template. This type is used to declare the class member T_HeaderLayout on line 6, which represents the expected header layout to be processed. The last template parameter, T_DHeader, is also a type. However, this type is used to allow static polymorphism of methods of the Header class; therefore, it represents a type that is derived from the Header class itself [13].

Consequently, with the extensive use of templates, an MpO base class provides a high-degree of configurability to MpO class objects. Thus, MpO base classes contribute to more reusable and compact code. The graph described in Figure 2a is an example since node is a different C++ object, sharing the same source code, described in Listing 2 using different template parameters.

### D. Specializing Operands with constexpr

In MpO, we use constexpr functions and variables to set accurate bus sizes in a generic fashion, which leads to faster and more compact circuits while configurable yet synthesizable C++ descriptions are used. Also, constexpr functions are more comprehensive compared to the their equivalents using older C++ versions. Indeed, they allow template specialization and alleviate a task that before C++11 was only possible through template metaprogramming and partial template specialization.

The type RXBitsType in Listing 2 line 5 is such an example. The functions numbits(), bytes2Bits(), and shift_size_def() in Listing 2 are examples of constexpr functions. Listing 2 shows the implementation of the numbits() function.

---

Listing 2: The Header MpO C++ base class.

```cpp
// Base Header class used to implement different headers
template<size_t N_Size, size_t N_BusSize, typename T_HeaderLayout, typename T_DHeader>
class Header {
    protected:
        typedef ap_uint<numbits(bytes2Bits(N_Size))>> RXBitsType;
        const T_HeaderLayout HeaderLayout;
        const ShiftType stateTransShiftVal;
        const array<bool, ARR_SIZE> HeaderBusCompVal;
        RXBitsType rxBits;
    public:
        template<typename T, typename F>
        const T init_array(const F& func) const {
            // Fills up an array using a callable parameter
            auto arr = func();
            return arr;
        }
        Header (const headerIDType instance_id, const T_HeaderLayout& HLayout) :
            ...,
            HeaderLayout(HLayout),
            stateTransShiftVal(shift_size_def(bytes2Bits(N_Size), N_BusSize, (HLayout.KeyLocation.first + HLayout.KeyLocation.second)),
            ...,
            HeaderBusCompVal();
            init_array<decltype(HeaderBusCompVal)>(){
                [HLayout.size_t t] { return (HLayout.ArrLenLookup[t] >> numbits(N_BusSize)) > 0;
                }
            };
            ...} // end of constructor
    void StateTransition(const PacketDataType& PacketIn);
    void ExtractFields(...);
    void PipelineAdjust(...);
    void HeaderAnalysis(const PacketDataType& PacketIn,
        PHVDataType PHV, PacketDataType PacketOut);
```
function along its verbose equivalent described in C++03. This function returns the size in bits to represent an arbitrary-sized integer.

One can benefit of the compilers’ ability to propagate constants by using constexpr functions to initialize class members in constructors. An example is the protected member stateTransShiftVal of the Header class in Listing 2 line 22, whose value is compile-time resolved when the class constructor is called (line 19), becoming a hardwired value in the HW implementation.

E. Exploiting STL Constructs

STL constructs raise the development abstraction and ease code readability and maintenance, characteristics favored by the MpO methodology.

Listing 3: The numbets() constexpr function

```
constexpr recursive numbets implementation
template<typename T> constexpr T numbets(T n) {
  return (n < 2) ? 1 : 1 + numbets(n >> 1);
}
```

use the decltype keyword. Again, one constexpr function is used, createMask(), to allow constant propagation on variable DataInMask.

Also, STL arrays, such as the HeaderLayout.Key, allow the use of iterators in a range-based for loop to iterate over the array. Such constructs lead to safer and more compact code since it is not required to calculate the iteration indexes or to specify loop bounds.

Such an example is the for statement shown in Listing 4 line 9. In addition, automatic compiler type resolution can be used with the auto keyword to determine the type of the loop iterator, simplifying the code as well.

According to our experiments, using STL constructs did not introduce overhead in terms of QoR. However, the increased code readability and modularity is noticeable, specially when dealing with data containers, such as array, by minimizing the need for raw pointer manipulation as required in C.

F. Inheritance and Static Polymorphism

The MpO methodology favors code reuse by employing inheritance whenever possible. Inheritance greatly improves code modularity and maintainability by reducing code replication. MpO exploits C++ to leverage the DRY (don’t repeat yourself) design guideline. Indeed, C++ offers adequate artefacts for improving inheritance, such as polymorphic methods and virtual classes.

Virtual classes are, to date, not supported by HLS vendors. However, inheritance and static polymorphism are allowed.

In the packet parser example, it is of interest to keep the same MpO method calls even if variable- and fixed-size headers are processed in a slightly different manner. To do so, static polymorphism is a C++ mechanism that can be used with MpO.

To parse fixed-sized headers, all needed information is known at compilation time. When processing variable-sized headers, the header length must be retrieved from the header information itself. To do so, the T_HeaderLayout type in Listing 2 implements static polymorphism to retrieve both fixed- or variable-sized header length information using the same method call. The T_HeaderLayout definition is shown in Listing 5.

In Listing 5 the HeaderFormat is the base struct. The struct varHeaderFormat and fixedHeaderFormat (not shown in the code extract) are derived from HeaderFormat. Note that to allow static polymorphism, we use the Curiously Recurring Template Pattern (CRTP) technique [13] as in [3], [4], where the derived class is passed as a template parameter to the base class (lines 10-11). By doing so, the compiler is able to statically resolve pointer conversions, which results in a synthesizable description. In this example, the implementation of the getSize() method (line 6) is done in the derived struct (line 17).

The base class Header from Listing 2 also supports CRTP to implement static polymorphism. Two classes are derived from the Header class: the FixedHeader class and the VariableHeader class. Similarly to what is done with the HeaderFormat from Listing 5 the classes derived from the Header class have their own implementation for the method PipelineAdjust() (Listing 2 line 35). This method is responsible to keep the output data bus aligned for the next processed header. To process fixed-sized headers, fixed bit-shift operations suffice for this alignment while barrel-shifters are required when dealing with variable-sized headers.

https://godbolt.org/z/xKXXON
A naive barrel-shifter implementation in FPGAs is based on a chain of multiplexers, which results in $O(N \log(N))$ area complexity and $O(\log(N))$ delay. Contrary to ASIC design, implementing wide multiplexers can be costly in FPGAs, having normally the same complexity as an adder. Thus, avoiding wider multiplexers is desired when designing efficient FPGA HW. In the parser, the number of bits to be shifted is a function of the current header size. Once we are dealing with wide data buses and the size of the processed headers well-constrained by a formula (Listing 5 line 13) in which only a few set of values are valid, then a natural choice is to use a small lookup table that holds only the set of valid shift operands.

### G. Smart Constructors

Class constructors can be used to initialize constant class members, which leads to more efficient circuits, as in the constant lookup table of shift values in the previous section.

An example of a smart constructor that makes use of a templated function is shown in Listing 2 line 11. The function is called in the constructor in line 25 to initialize the `const` class member `HeaderBusCompVal`. Note that the templated function uses a lambda expression as a callable parameter.

In C++, templated functions and objects allow callable objects to be passed as parameters to functions. Callable parameters allow functions to be reused, thus reducing code duplication. Such callable parameters can be function pointers, functors (function objects), or lambda expressions, which were introduced in C++11. Functors are objects with a single method, which once constructed can be called as a function. Modern compilers have the ability to optimize the object construction, inlining the code in the scope it is called. More interestingly, lambdas are local functions which are stored as variables, while allowing parameter passage and context capturing. In fact, lambdas are syntax sugar for functors [16]. Indeed, for the same functionality, both the functor and the lambda implementation generate the same assembly (and LLVM) code.

Function pointers are unsynthesizable constructs by most HLS tools. Thus, functors and lambdas are alternative yet synthesizable ways to emulate function pointers. Besides being convenient and elegant, lambdas can contribute to more efficient HW generation by enabling constant propagation when initializing constant class members in class constructors.

### IV. PACKET-PARSER GENERATION FROM P4

This section presents the MpO methodology applied to a real-life problem. First, we present a case-study for generating a packet parser pipeline from a P4 description. Then, we discuss adaptations of the MpO methodology to current HLS tools, including opportunities for improvements in HLS tools.

#### A. Top-Level Pipeline

Until now, we have described how a single HW module can be described using the proposed MpO approach. Several instances of the generic `Header` class from Listing 2 can be specialized to generate different HW modules. Therefore, the proposed MpO methodology from § III can be used to implement a complete packet parser.

Listing 6 shows a possible implementation for the packet parser illustrated in Figure 2. The code in this listing is automatically generated from a P4 description [24]. Details on the internal parser micro-architecture and the optimization steps for code generation are subject of previous work [29].

![Listing 5: Example of static polymorphism](https://godbolt.org/g/uQqU65)

The generated HW architecture from Listing 6 is in accordance to the parser pipeline organization shown in Figure 2b. This is ensured by the static declaration of the parser node objects (lines 5 and 8), in a similar approach to what Zhao and Hoe have proposed [18]. The static keyword is used to declare stateful header objects. The pipeline is therefore inferred according to the data dependency graph. Conditional inputs in a given pipeline stage or in the output are resolved with the ternary (?:) C operator (lines 23, 26, and 29), which generates a multiplexer in the final HW [31].

#### B. Adapting MpO to Current HLS tools

Vivado HLS supports C, C++, and SystemC for synthesis and simulation. The most recent C++ version supported by Vivado HLS dates from 2011. However, Vivado HLS does not fully support this C++ version, limiting the spectrum of standard high-level constructs that can be used to raise the development abstraction.

This work makes extensive use of the C++11 STL. While some constructs available in the library, such as lists and maps, are expected to fail during synthesis, fixed-bounded constructs are well supported. These constructs, such as the standard `array` and `pair`, are described as classes in the STL and their operators are defined as functors in these classes. During synthesis, when facing each of these operators, Vivado HLS performs automatic function inlining for the method describing one operator, which leads to longer synthesis time and memory usage. The decision to use these STL constructs is, therefore, a trade-off between the synthesis time and the flexibility provided by these constructs.

During this work, we have struggled to correctly implement dynamic polymorphism with Vivado HLS. Static polymorphism through CRTP was the only found solution for polymorphism in this work. However, even static polymorphism is limited. Derived classes can access neither local members nor base class members. Such data accesses cause an invalid pointer reinterpretation error under synthesis. The detour for such error is to always pass the necessary operands as function parameters to the callee methods in the derived class. Accessing static members in the base class does not cause any error.

[1] https://godbolt.org/g/uQqU65
Modern compilers are able to devirtualize virtual methods by dynamically polymorphic classes at compile time and to inline the code in derived classes. Clang, for instance, is capable of devirtualizing with the compiler optimization flag set to −O3. However, Vivado HLS does not support the compiler optimization flags. Since the optimization flag has no effect on Vivado HLS, and its own synthesis pass is not able to infer the virtual type, dynamic polymorphism cannot be synthesized. Thus, as already concluded by other researchers [32], borrowing some front-end optimization techniques from modern compilers may be useful in the HLS world.

V. EXPERIMENTAL RESULTS

This section presents the results of this work. We first introduce the experimental setup, then, we present our results. Finally, we close this section with some analysis and discussions of our findings.

A. Experimental Setup

In order to demonstrate the efficacy of the proposed MpO methodology, we conducted three design experiments. The chosen design experiments are as follows:

1) A configurable packet parser [29];
2) A flow-based traffic manager (TM) [33]; and
3) A digital up-converter [34].

The first design experiment is a configurable packet parser briefly introduced in § III-B To enable reproducibility, the code of this experiment is open-source.4

The second design experiment is a flow-based TM architecture proposed by Benáček et al. [33] in the context of SDN. The architecture is made up of a traffic policer, a packet scheduler, a systolic priority queue, and a traffic shaper. This source code is proprietary.

The third design experiment is a digital up-converter retrieved from an application note from Xilinx [34]. The up-converter design is composed of multi-stage FIR filters, a direct digital synthesizer, and a mixer. This implementation is open-source.6

All experiments targeted a Xilinx Virtex-7 FPGA, part number XC7VX690TFFG1761-2. Vivado HLS 2015.4 was used to generate synthesizable RTL code. While we have tested more recent versions of Vivado HLS, according to our experiments, the version 2015.4 is the one that better supports modern C++ constructs. Xilinx Vivado 2015.4 was used for the synthesis and placement and route (P&R). Area and timing results were extracted from post-P&R reports. Latency (in cycles) and pipeline initiation interval (II) were obtained after HLS compilation on Vivado HLS. In the Vivado HLS notation, II means the interval, in cycles, before a design is able to process a new input. An II = 1 means a design can perform one new operation every cycle.

Whenever possible, code complexity is presented in terms of equivalent lines of code (eLOC). The eLOC metric ignores blank and commented lines. LOC, when presented, represents the actual number of lines of code. To measure code reuse we use CCFinderX, an open-source tool7 based on the work by Kamiya et al. [35]. This tool detects code clones and similarity for various programming languages including C++.

B. Results

1) Configurable Packet Parser: Table II presents the results of the configurable packet parser experiment.

In terms of throughput (not show in the table) and latency, this work performs as well as the hand-crafted VHDL implementation reported in [36]. When comparing to the automatic generated VHDL, this work outperforms it in all aspects, except in the number of FFs. The LUTs reduction can be explained by the degree of parameterization that our specialized C++ classes offer. The operations are therefore fine-tuned for each header instance.

We have conducted a different experiment where we mimic Benáček’s architecture using our MpO methodology. This experiment is labelled as “MpO” in Table II! Architectural aspects aside, this hybrid implementation delivers better results than the original Benáček implementation, significantly reducing the latency (−10%) and the number of LUTs (−35%). One takeaway from this experiment is that VHDL lacks in abstraction to be used as a direct conversion language from a high-abstraction DSL, such as P4. On the other hand, C++ offers an adequate dialect to represent network semantics that can be described using P4.

2) Flow-based traffic manager: Table III presents the results of the TM implementation. This TM implementation is able to process 1024 different packet flows. The queue depth of this TM is 128. To provide a fair comparison for this experiment, we have not performed any algorithmic or architectural optimization in the original code. Also, we kept the same optimization directives of the original design.

Besides code modernization using C++11 constructs, we have augmented the degree of parameterization of the TM design. The

---

### Table II: Packet parser results. Adapted from [29]

| Work  | Frequency [MHz] | Latency [ns] | LUTs | FFs | Slice Logic |
|-------|----------------|--------------|------|-----|-------------|
| VHDL  | 195.3          | 27           | 103  | 5537 | 16.640      |
| MpO   | 321.5          | 41.6         | 6650 | 10388 | 17.658      |
| MpO   | 321.5          | 25.6         | 6946 | 8900 | 14.946      |

---
Table III: Flow-based TM results

| Work | Frequency [MHz] | LUTs | FFs | Slices | eLOC |
|------|-----------------|------|-----|--------|------|
|      | Systolic Slice Size = 3 |      |      |        |      |
| [33] | 91.5            | 37,581 | 13,723 | 9,833 | 784  |
| [33] | MpO            | 102.4 | 33,975 | 13,536 | 9182 | 1001 |
|      | Systolic Slice Size = 4 |      |      |        |      |
| [33] | 74.5            | 35,625 | 13,891 | 14,669 | 1001 |
| [33] | MpO            | 44.9  | 11,666 | 14,885 | 31,884 | 1001 |
|      | Systolic Slice Size = 8 |      |      |        |      |
| [33] | 31.0            | 200,450 | 13,930 | 57,876 | 1001 |
| [33] | MpO            | 37.1  | 33,944 | 13,979 | 3472 | 1541 |

Table IV: Digital up-converter HW QoR results

| Work | Frequency [MHz] | Latency [cycles] | LUTs | FFs | Slices |
|------|-----------------|-----------------|------|-----|--------|
| [34] |                | 3394~3395       | 3472 | 7388 | 1641   |
| [34] | MpO            | 3375~3376       | 3010 | 5723 | 1568   |

core component of this TM is a systolic implementation of a priority queue. In the original design, each systolic slice implemented a micro queue of two or three elements. The MpO implementation fully parameterizes these micro queues, not limiting to two or three. This can be seen in Table III in which we show the results of two different versions of the TM, with 4, 8, and 16 elements in each systolic slice.

The MpO version of the TM improved HW QoR. Noticeably, the circuit frequency was improved by more than 10%. The area consumption was as well improved, with a reduction of more than 10% in LUTs and 7% in the number of occupied slices. No HW QoR impact was observed in latency, II, DSPs, and BRAMs.

The MpO implementation augmented eLOC by 27%. Indeed, this was expected because we generalized a wired hardwired implementation of the systolic queue slice to support arbitrary systolic slices. Moreover, a significant contributor to the increased eLOC is a library that can be reused elsewhere. This library has roughly 10% of the total eLOC, in which we implemented type trait classes and generic helper functions.

In both original and MpO-based implementation, CCFinderX has not found code clones.

3) Digital up-converter: Table IV shows the results of the digital up-converter implementation. We have not performed optimizations on the original description. We have only modified the code for the FIR filters. While HW QoR results consider the whole design, the SW quality analysis applies only to the filters.

As shown in Table IV the MpO approach improves QoR metrics compared to the original digital up-converter implementation from Xilinx. There are improvements in the maximum frequency, latency, and area consumption, notably for FFs. The FFs reduction can be explained by the reduced latency, which means that a shorter pipeline was required in the MpO implementation. No effects on BRAM, DSP, and II were observed, thus, not reported in Table IV.

The MpO approach significantly improves software quality as presented in Table V. The measure of eLOC in Table V shows how expressive the MpO is compared to the original design. The MpO-based code is 16% more concise than its original counterpart. Also, we evaluate code reuse by measuring code clone patterns as reported in Table V

We observe that CCFinderX found 6 patterns of code clones in the original design while no clones were found in our implementation. Indeed, the MpO methodology favors code reuse and STL usage, following a DRY methodology to avoid code duplication. In addition, in the original design, CCFinderX found an average of 2.33 replicated instances per clone pattern, with a maximum of 3. CCFinderX also reported an average of 83.5 LOC per clone, with a maximum of 115.

C. Analysis and Discussions

Zhao and Hoe [18] present quantitative results for the design of a network-on-chip. The authors compare their methodology to an auto-generated RTL implementation, while comparisons to hand-crafted RTL are not shown. Their results on average show an overhead of 11% and 8% for the LUTs consumption and the clock period, respectively, while the FF usage is reduced by 58%. Latency results are not presented. Their experiment is similar to the comparison between this work applied to the packet parser and [35]. Using our methodology, the maximum frequency is 1.6× higher, the latency is reduced by 45%, and LUTs by 40%, while increasing the number of FFs by 60%. Yet, these improvements in the LUTs consumption and the maximum frequency are due to our design’s has ability to specialize operations, leading to faster and more compact circuits.

Oezkan et al. [19] present comparative results between their HLS-based image processing library and the results of an image processing DSL that generates C++ code. In that comparison, their results outperform the auto-generated code, which is however expected since their library is directly hand-crafted in C++. Therefore, their results cannot be used as a baseline for a fair comparison against our proposed methodology.

While similar works have exploited modern C++ with HLS design [3], [4], [16], [17], no generalized methodology has been presented to date. Muck and Frohlich [3], [4] have focused on unified CPU-FPGA C++ code-base. Thomas [16] and Richmond et al. [17] have exploited the power of modern C++ to implement features not natively supported by HLS tools, such as recursion and high-order functions. None these works have presented the benefits of using C++ in the generated HW, as we have shown. Also, no SW quality metrics have been presented in these works.

VI. CONCLUSION

HLS is a game changer to spread FPGA usage outside the HW world. However, achieving high QoR with HLS design still relies on detailed FPGA knowledge to generate FPGA-friendly low-level code, an uncommon skill for software developers. Such codes lower the design abstraction level making their comprehension and maintenance tedious even for experienced programmers. This HLS design approach follows a uni-dimensional design perspective, trading-off HW QoR and SW quality.

In this work, we introduce a bi-dimensional HLS design view by proposing the MpO methodology. The MpO methodology targets FPGA development with HLS exploiting standard C++ constructs. The proposed MpO methodology builds on the concept of an MpO base class. The five presented characteristics of an MpO base class leverage HLS design, improving HW QoR, code readability and modularity while raising the abstraction development level. Through three design examples, we showed that using the MpO methodology, a C++ code can deliver results comparable to hand-crafted VHDL design. We as well showed that the code complexity can be reduced using the zero-overhead characteristic of C++.

We hope that the MpO methodology will inspire both software and hardware engineers developing new FPGA applications in a more elegant and modular fashion.
