Proposed New $N$-Multilevel Family of Topologies for T-Type Inverter

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Abstract: This paper proposes a new $N$-multilevel topologies for T-type inverter. The proposed topologies constitute the single bridge legs with the shape of the rotated character “T” and a variable direct current-link circuit. The proposed topologies present higher efficiency and lower number of components compared with NPC topologies and nested multilevel topologies. Also, other topologies have been compared in terms of reduced number of diodes, switches, flying capacitors, and DC supplies. The optimized staircase modulation technique is used to obtain voltage waveforms with high quality and superior output voltages. Furthermore, the principles of the proposed topologies were validated via simulations and experiments.

Keywords: Multi-level T-Type inverter, current commutation strategy, turning off-on devices, power components.

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1 Introduction

Multilevel inverters are becoming increasingly popular for high- and medium-power applications. Thus, numerous topologies and configurations have been proposed and designed to enhance the operation performance of and create multilevel inverters with highly desirable characteristics for high-power application [1-3]. The diode-clamped (NPC) [4, 5], flying capacitor (FC) [6, 7] and cascaded H-bridge (CHB) [8] are the most common inverters and are illustrated in [9-11]. The deviating voltage of neutral-point voltage in NPC, the unbalanced voltage in the direct current (DC) link of FC, and the large number of separated DC supplies in CHB are the main drawbacks to be considered in these topologies [12-14]. For the low power application such as photovoltaic system [15-17], multilevel converters can be used to generate a high-quality waveform with power semiconductor switches. The T- type inverter is one of the most common converters proposed to be an alternative for industrial applications because it has the advantages of both the two-level converter, including low conduction losses, small part count, and simple operation, and the three-level converter, such as low switching losses and superior quality of output voltage quality [18]. The T-type
The converter can be used for the low voltage application with a strong competitiveness to the other types of three-level topologies [4, 19-23].

The principal configuration of nested multilevel topologies which is reported in [14] present a good performance compared to NPC topology in terms of reduced number of diodes and consequently higher efficiency. However, the nested multilevel topologies consist of capacitors and many DC-link voltage supplies, which might lead to voltage imbalance during operations, particularly for high-voltage levels.

This paper presents a new family of topologies for the T-type inverter. The proposed topologies can be extended to the N-level by adding only two switches and one DC voltage supply to the DC-link circuit in every high level, as illustrated in Fig.1. The basic circuit of the proposed family of topologies consists of two parts. The first part is the single bridge legs shaped like an inverted “T,” and the second part is the variable DC-link circuit. Figs. 1. (a)–1(b) show the new multilevel converter for four- and six-level output voltages, respectively.

Compared with nested multilevel topologies applied in [14] and other principal configurations, such as NPC, FCs, cascades, and modular multilevel converters, the advantages of these new family of topologies include low power losses, higher efficiency, reduction of a large number of switches, zero passive components, and simplicity of configurations, particularly for high levels. Furthermore, the proposed family of topologies was validated by simulations and experimental results presented in the following sections.

### 2 Converter description and operation principle

Fig. 1 illustrates the configuration diagram of the new family of topologies for four- and six-level output voltage. Fig. 1(a) shows the configuration of the four-level topology, which consists of two parts. The conventional two-level legs with bidirectional controlled switches (such as S1 and S2) comprise the first part, and the multilevel DC-link with voltage DC supplies comprise the second part. To ensure that a symmetrical output voltage is acquired, the input DC voltages are adjusted to $V_{dc1} = V_{dc2} = V_{dc3}$. Furthermore, all switches are connected one at a time to prevent short circuits from occurring inside the DC-link and two-level conventional leg.

As can be seen from Fig.1, the four-level configuration can be extended to five and six levels by only adding two switches and one voltage DC supply to the DC link at each high level. TABLE I (a)-(b) shows the output voltage levels as a function of the states of the switching for four- and six-level for leg $a$.

Where $S_{a}$ is referring to the switching state for leg $a$ and $V_{an}$ is presenting the output line to neutral voltage for leg $a$. 
TABLE I. Switching states for proposed topologies.

(a) Four Levels

| Sa | Q1 | S1 | S2 | Q2 | T1 | T11 | Van  |
|----|----|----|----|----|----|-----|------|
| 3  | 1  | 0  | 0  | 0  | 1  | 0   | +3Vdc |
| 2  | 0  | 1  | 1  | 0  | 1  | 0   | +2Vdc |
| 1  | 0  | 1  | 1  | 0  | 0  | 1   | +1Vdc |
| 0  | 0  | 0  | 0  | 1  | 0  | 0   | 0    |

(b) Six Levels

| Sa | Q1 | S1 | S2 | Q2 | T1 | T2 | T3 | T11 | T22 | T33 | Van  |
|----|----|----|----|----|----|----|----|-----|-----|-----|------|
| 5  | 1  | 0  | 0  | 0  | 1  | 1  | 1  | 0   | 0   | 0   | +5Vdc |
| 4  | 0  | 1  | 1  | 0  | 1  | 1  | 1  | 0   | 0   | 0   | +4Vdc |
| 3  | 0  | 1  | 1  | 0  | 1  | 0  | 0  | 0   | 1   | 0   | +3Vdc |
| 2  | 0  | 1  | 1  | 0  | 0  | 1  | 0  | 0   | 0   | 1   | +2Vdc |
| 1  | 0  | 1  | 1  | 0  | 0  | 0  | 1  | 0   | 0   | 0   | +1Vdc |
| 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0   | 0   | 0   | 0    |

Fig.1. New multilevel configuration with (a) four-level, and (b) six–level.
Fig. 2 (a)-(d) Current flow through the switches of a leg on four-level topology. Where "●" is referring to the output point of leg \( a \) which might be connected directly to the load.

Time-on delay is implemented during operation to prevent short circuit from occurring inside the bidirectional switches and the DC-link circuit, ensuring that the current will flow through the right path during switching. Fig. 2 illustrates the current flow through the switches of a leg on the proposed four-level topology.

### 3 Modulation Technique

The modulation strategy is a crucial feature in the design of the proposed family of topologies. The staircase modulation technique and modified space-vector modulation are useful because the proposed topologies are unable to operate during the synchronization of the switching state of two legs. The space vector references in the \( d-q \) frame shown in Fig. 3 and its components can be found and represented from the equations below [12]:

\[
V_q = \frac{3 V_{dc}}{3(N-1)} (2Sa - Sb - Sc) \quad (1)
\]

\[
V_d = \frac{3 V_{dc}}{\sqrt{3}(N-1)} (Sc - Sb) \quad (2)
\]

\[
V = V_q - jV_d \quad (3)
\]
Equations (1) ~ (3) are representing the relationship between the switching states \((S_a, S_b, S_c)\) and their corresponding space voltage vectors. Where \(V\) is referring to the reference vector voltage based on its magnitude (length) \(V_q\) in imaginary axis and \(V_d\) in real axis. However, \(S_a, S_b,\) and \(S_c\) are representing the switching states of three phase inverter’s legs. Finally, \(N\) is the number of output voltage level.

Fig. 3. Switching state vectors of the four-level in d-q reference frame [12]

### 4 Component Rating and Selection

The rating of the components and switches is significant in designing the proposed topologies starting from four levels to \(N\) levels; that is, the proposed family of topologies can be extended to \(N\)-high levels by adding only two switches and one voltage DC supply to the DC link circuit without any changes in the main bridge circuit in each high level. These proposed topologies can be used for low- and medium-power applications while considering the voltage stress, efficiency and voltage rating of the components. To obtain the desired output voltage, \(V_{dc}\) must be adjusted to a certain value, and the voltage supplies of the DC link circuit must be equal to \(V_{dc}\), as illustrated by Eqs. (4)–(9) and TABLE II. However, the voltage stress over the switches can be defeated using an insulated-gate bipolar transistor (IGBT) with good performance and high efficiency. Additionally, for the medium-power applications, the single IGBT can be replaced by two IGBTs connected in series, particularly in certain parts of the topology. Thus, the voltage stress can be divided across those switches, and the voltage stress problem can be easily addressed.

| The proposed topologies | Main bridge \(Q_1 \sim Q_6\) | Bidirectional switches \(S_1 \sim S_6\) | DC-link \(T_1 \sim T_n\) |
|-------------------------|-----------------------------|-----------------------------------|--------------------------|
| Switches voltage rating | \((N-1) V_{dc}\)             | \((N-2)V_{dc}\)                    | \(nV_{dc}\)              |

**TABLE II.** Proposed rating requirement of topologies per level \(N\).
5 Generalization and comparisons

As shown in Fig. 1, the proposed configuration consists of two main parts: the inner three-phase legs and the variable DC link. Additionally, the proposed configurations can be applied to high levels using the same principle with consideration of the following conditions:

1) Number of the DC-link switches, which can be identified using the following equation:

\[ N_{\text{sw}-\text{dc}} = 3 + (N - 4) \times 2 \]  \hspace{1cm} (4)

2) Total number of the DC-link voltage supplies, which can be determined using the following formula:

\[ N_{\text{vs}-\text{dc}} = (N - 2) \]  \hspace{1cm} (5)

3) Magnitude of the main voltage DC supply. First, the \( V_{\text{dc}} \) has to be adjusted to the desired value so that each of the DC link magnitude voltage supply must be equal to \( V_{\text{dc}} \), preventing the imbalance of voltage inside the circuit. The following equations illustrate this process in detail:

\[ mV_{\text{dc}} = \left( \frac{N_{\text{sw}-\text{dc}}}{2} + \frac{3}{2} \right) V_{\text{dc}} \]  \hspace{1cm} (6)

Or

\[ mV_{\text{dc}} = (N_{\text{vs}-\text{dc}} + 1) V_{\text{dc}} \]  \hspace{1cm} (7)

By substituting Eq. (4) & Eq. (5) into Eq. (6) & Eq. (7) respectively, the final equation is:

\[ mV_{\text{dc}} = (N - 1) V_{\text{dc}} \]  \hspace{1cm} (8)

so that

\[ m = (N - 1) \]  \hspace{1cm} (9)

where \( mV_{\text{dc}} \) and \( m \) are the magnitude and coefficient of the main voltage supply. \( N_{\text{sw}-\text{dc}} \) and \( N_{\text{vs}-\text{dc}} \) are the total number for the switches and voltage supplies inside the DC link; \( N \) is the number of level; and \( V_{\text{dc}} \) is the adjustable stepped output voltage.

Example:

For the four-level configuration in Fig. 1(a), the following assumptions are applied:

\( V_{\text{dc}} = 100 \text{ V}, N = 4 \).

Based on the above assumptions, the total number of switches \( (N_{\text{sw}-\text{dc}}) \) and voltage supplies \( (N_{\text{vs}-\text{dc}}) \) for the DC link circuit can be easily determined. Also, the magnitude of the main voltage supply \( (mV_{\text{dc}}) \) can be adjusted and determined as follows:

by Substituting \( V_{\text{dc}} \) and \( N \) into Eq. (4), Eq. (5), Eq. (8), and Eq. (9), we obtain:

\( N_{\text{sw}-\text{dc}} = 3, N_{\text{vs}-\text{dc}} = 2, m = 3, mV_{\text{dc}} = 3 \times 100, mV_{\text{dc}} = 3 \times 100 = \text{the main voltage supply} = 300 \text{ V} \).

The proposed family of topologies is designed with simple structures and a
minimum number of components to avoid the drawbacks, including unbalanced voltages across capacitors, voltage deviation, short circuit occurrences, and high conduction losses, of other topologies.

6 Simulated and experimental results

The feasibility of the proposed family of topologies was validated through simulations and experiments. The experimental setup was built and run successfully, as presented in Fig. 4. All items in the experiment are highlighted in this photo. This experimental prototype was designed and built to obtain the outcomes of the four-level inverter. The simulation results for the proposed configuration of the four-level are shown in Fig. 5. As shown from the simulation results, the principle of the proposed topologies is correct because the output voltages for each designed topology are as expected. The rating and specification of the components and equipment used in the experiment are described in TABLE III.

| Items                | Rating                                      |
|----------------------|---------------------------------------------|
| dSPACE              | CP1104                                      |
| Gate deriver        | 5V input - 15V output                      |
| Dc-supply           | Max 1200V                                   |
| IGBT                | HGT20N60B3D, 19A, max 600V                  |
| Motor(load)         | 400V, 0.81A, 0.3 kW, 50Hz, 2800 min⁻¹       |

For easy implementation, the proposed four-level configuration was selected for the experiment. Fig. 5 and Fig. 6 show that the experimental and simulation results are the same, thus ensuring the validity of the principle of the proposed family of topologies. The induction motor had been used in this experiment to ensure that the proposed configuration works with highly inductive loads, as can be seen clearly in Fig. 6 (a) and (b). We therefore conclude that the principle of the proposed topologies is successfully proven via simulation and experiments.
Fig. 5. Simulated results for the proposed family of configuration with four levels. (a) Line to neutral voltages. (b) Line to ground voltage.

Fig. 6. Experimental results for the proposed configuration with four levels. (a), and (b) Output line voltages and current of the the induction motor load.

7 Efficiency analysis and losses comparison
Efficiency is one of the significant features to validate the superiority of the proposed topologies to the other topologies. TABLE IV shows the comparison of the proposed four-level topology and other existing topologies in terms of the reduced number of switching, extra diodes, FCs, and DC supply.

| Topology | Switches | Extra diodes | Flaying Capacitores | DC supplies |
|----------|----------|--------------|---------------------|-------------|
| Fig. 1(a) | 15       | 0            | No                  | 3           |
| [14]     | 18       | 6            | Yes                 | 3           |
| [24]     | 18       | 6            | Yes                 | 3           |
| [25]     | 12       | No           | No                  | 9           |
| [26]     | 24       | 6            | Yes                 | 3           |
| [27]     | 36       | 12           | Yes                 | 9           |
Fig. 7. (a) Nested multilevel configuration with four level. (b) Flying capacitor topology

Apparently, the proposed four-level topology requires the most minimum number of power components compared with the other topologies. In fact, reducing the number of the power components and turn on–off devices results in the reduction of switching and conduction losses. As seen from the statistical analysis shown in TABLE III, the proposed four-level topology operates with good performance and higher efficiency compared with the other topologies because of the absence of extra diodes and FCs, as well as the minimal number of DC-link supply and switches. Furthermore, the comparison of power losses between the proposed topologies and nested multilevel topologies is presented for convenience. The conduction and switching losses for both proposed four-level topology and four-level nested configuration were simulated via PLECS software and tested via experiments [14] under different conditions of loads and DC link voltages. The conditions and cases, which are shown below, applied for the comparison of losses are the same conditions used and studied in [14]:

1) Case 1: 150 V, $R = 65 \, \Omega$, $L = 7 \, mH$, $f_S = 720 \, Hz$.
2) Case 2: 300 V, $R = 142 \, \Omega$, $L = 15.3 \, mH$, $f_S = 720 \, Hz$.
3) Case 3: 600 V, $R = 142 \, \Omega$, $L = 15.3 \, mH$, $f_S = 720 \, Hz$.

TABLE V. Comparison of losses for new proposed topology and nested topology for the four-level configuration.

| Case | SW | Cond | Total losses (W) | SW | Cond | Total losses (W) |
|------|----|------|------------------|----|------|------------------|
| 1    | 0.053 | 0.51 | 0.56             | 0.26 | 2.58 | 2.84             |
| 2    | 0.045 | 0.93 | 0.975            | 0.56 | 2.41 | 2.91             |
| 3    | 0.18  | 3.32 | 3.5              | 1.07 | 2.5  | 3.57             |

As seen from TABLE V, for each case, the proposed four-level topology has less conduction and switching losses compared with the four-level nested configuration. Based on the results shown in TABLE V, the efficiency of the proposed topologies is higher than that of other topologies because of the minimum number of power components used and no extra diodes and FCs were used. Also, reducing the
switching time and number of turn on–off devices during the switching sequence is one of the strategies designed to reduce losses. However, the lack of modularity one of the drawbacks of the proposed topologies especially for medium-voltage applications (1MW–10MW and 1kVdc–8kVdc).

8 Conclusion
The proposed family of topologies were illustrated and demonstrated in detail in this paper. The proposed topologies were designed with a minimum number of components and higher efficiency compared with other existing topologies, such as NPC and nested multilevel topologies proposed in [14]. The advantage of these T-type multilevel topologies is that the configuration can be designed and increased to N-levels with a low number of power components and cost. The proposed family of topologies were proposed as an alternative for low-and medium-power application where switches are capable of withstanding for long duration with good conductivity and high performance. It is not recommended to use these topologies for high-power applications because of the high voltage stress across the switches. We could conclude that the efficiency, simple construction, and low number of components and costing of proposed N-multilevel topologies make it advantageous over other topologies.