Temperature characteristics of FinFET based on channel fin width and working voltage

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ABSTRACT

This paper shows the temperature sensitivity of FinFET and the possibility of using FinFET as a temperature nano sensor based on Fin width of transistor. The multi-gate field effect transistor (MuGFET) simulation tool is used to examine the temperature effect on FinFET characteristics. Current-voltage characteristics with various temperatures and channel Fin width ($W_F = 5,10,20,40$ and 80 nm) are at first simulated, the diode mode connection has been used in this study. The best temperature sensitivity of the FinFET is has been considered under the biggest $\Delta T$ at the working voltage $V_{DD}$ with range of 0–5 V. According to the results, the temperature sensitivity increased linearly with all the range of channel Fin width (5-80 nm), also, the lower gate Fin width ($W_F$=5nm) with higher sensitivity can achieved with lower working voltage ($V_{DD}$=1.25 V).

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1. INTRODUCTION

The industry focus on silicon metal-oxide-semiconductor field effect transistors (MOSFETs) for the past 6 decades, this has been mainly due to the simplicity of manufacture, inherent scalability and high levels of possible integration [1, 2]. Until now the industry has kept up with Moore’s law [3-5] by making transistors smaller and reducing the distance between them. The problem that arises with reducing size is that the transistor will conduct current even when it turned off and thus consume power. To make the chips with high integration, a new structure of transistors has to be used since old MOSFET structure cannot be reduced further in nano dimension size.

Many new field effect transistor (FET) structures have been extensively explored given that the metal oxide semiconductor FET (MOSFET) technology has continued to approach its downscaling limits. One of the relatively newer FETs is the FinFET as shown in Figure 1 [6], a transistor-structured FET that is a popular research topic in the academic field and semiconductor industry [7-9]. The one new promising MOSFET architecture is the FinFET see Figure 1 that have the gate surrounding the channel which gives a better control and therefore reduces current leaking, one way of creating a FinFET is to use a nanowire as a channel and build a gate around it. [10-12]

The best example of sensors for subsumed electronic applications (i.e. used within equipment) is the semiconductor temperature sensor [13]. Transistor-based temperature sensors are designed on the basis of the temperature characteristics of current–voltage curves of nanowire transistors [14-20]. A bipolar transistor can be used as a temperature sensor by connecting its base and collector and operating them in diode mode. Similarly, a transistor with MOSFET structure can be used as a temperature sensor by connecting the gate with either the source or drain as shown in Figure 2. Electronic devices, such as diodes, transistors, capacitors

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and resistors, with nano-dimensions have recently become popular in the electronics industry due to their extremely small electronic circuits.

![FinFET structure](image1)

**Figure 1. FinFET structure [6]**

The performance of new devices, which may correspond to a wide array of new applications, will likely depend on the nano-dimensional characteristics of such devices. The chip generation of these relatively new and powerful electronic devices with ultra-small transistors may be even regarded more trustworthy when new findings from future research are consolidated. However, the new nano-dimensional FET designs and structures are still considered novel technologies and thus necessitate further study and improvement, and they require further innovations despite the limitations in the field of MOSFET science. So, this research explores the effect of width of Fin of FinFET on the temperature sensitivity of transistor and the possibility of using it as a temperature nano-sensor.

2. **METHOD**

Electronic device simulation has become increasingly important in understanding the physics behind the structures of new devices. Thus, simulation tools are adopted in this research for the analysis and evaluation of the temperature sensitivity of FinFET. The simulation tool can be supported the research work for further explore and development of nano-dimensional characterisation [21]. Simulation tools can also help identify device strengths and weaknesses and retrenchment costs and illustrate the extensibility of these devices in the nm range [22, 23].

In this study, MuGFET is used as the simulation tool to explore the characteristics of the FinFET transistor. The output characteristic curves of the transistor under different environmental conditions and with different parameters are considered. The effect of gate Fin width on the temperature sensitivity has been investigated based on the $I_{d}-V_{g}$ characteristics. MuGFET [24] simulation tool has been used for the characterization of FinFET with nano-dimensional structure, MUGFET is created and invented at Purdue University.

MuGFET adopts either PADRE or PROPHET for simulation, both of which were developed by Bell Laboratories. The PROPHET is a partial differential equation profiler for one, two, or three dimensions, and PADRE is a device-oriented simulator for 2D or 3D devices with arbitrary geometry [24, 25]. The software can generate useful characteristic FET curves for engineers to help them fully explain the underlying physics of FETs. MuGFET also provides self-consistent solutions to Poisson and drift-diffusion equations [24, 25] and can be used to simulate the motion of transport objects when calculating FinFET characteristics as shown in Figure 1.

This research used a simulation tool, which is called MUGFET. First the suitable parameters and dimensions will be chosen for simulation of FinFET, the data includes dimensions (length channel ($L_g$), width channel ($W_t$), oxide thickness ($T_{ox}$), doping concentration in channel, source and drain, and finally the temperature ($T$)), Table 1 illustrate all parameters of FinFET that has been used in the simulation, after simulation complete, the I-V data will have produced depending on parameters entered to the software. Finally, the optimized values were found to optimize the FinFET channel as temperature nano-sensor.
Table 1. Parameters of FinFET used in this study

| Parameter                        | Values                                      |
|----------------------------------|---------------------------------------------|
| Temperatures T                   | 250, 275, 300, 325, 350, 375 and 400 K°     |
| Working voltage $V_{DD}$         | 0–5 V with 0.25 V steps                     |
| Channel length $L_g$             | 85 nm                                       |
| Source and Drain lengths         | 50 nm                                       |
| Oxide thickness $T_{ox}$ (SiO$_2$) | 2.5 nm                                     |
| Gate Fin width $W_F$             | 5, 10, 20, 40 and 80 nm                     |
| Channel concentration (Si P-type) | $10^{16}$ cm$^{-3}$                        |
| Source and Drain concentration (Si N-type) | $10^{19}$ cm$^{-3}$                     |

3. RESULTS AND DISCUSSIONS

In this research, the $I_D$–$V_g$ characteristics of FinFET at the temperatures of 250, 275, 300, 325, 350, 375 and 400 K° are simulated with the following parameters: channel length= 85 nm, channel concentration (P-type)=$10^{16}$ cm$^{-3}$, source and drain lengths=50 nm, source and drain concentration (N-type)=$10^{19}$ cm$^{-3}$ and oxide thickness=2.5nm. The gate Fin width values are $W_F$=5, 10, 20, 40 and 80 nm.

Figures 3-7 show the change in $\Delta I$ when the temperature increased at the $V_{DD}$ range of 0–5 V with 0.25 V steps for the $W_F$ values of 5, 10, 20, 40 and 80 nm. As shown by the figures, the maximum sensitivities (max $\Delta I$) are at the relatively lower temperatures, and the values decreased linearly as temperature increased for all $V_{DD}$. Figures 3 and 4 present the maximum temperature sensitivity values at $V_{DD}$=1.25 V ($W_F$=5 nm) and $V_{DD}$=1.5 V ($W_F$=10 nm); followed by Figures 5 and 6 at $V_{DD}$=2 V ($W_F$=20 nm) and $V_{DD}$=3.25 V ($W_F$=40 nm; and finally, Figure 7 at $V_{DD}$=5 V ($W_F$=80 nm).

![Figure 3](image1.png)

Figure 3. $\Delta I$–Temperature characteristics of FinFET ($W_F$=5 nm), $V_{DD}$ range of 0–5 V with 0.25 V steps

![Figure 4](image2.png)

Figure 4. $\Delta I$–Temperature characteristics of FinFET ($W_F$=10 nm), $V_{DD}$ range of 0–5 V with 0.25 V steps
Temperature characteristics of FinFET based… (Yousif Atalla)

Figures 5-7 show the changes in ∆I with decreasing V_{DD} at T=250, 275, 300, 325, 350, 375 and 400 K° and W=5,10,20,40 and 80 nm. The following maximum sensitivities (max ∆I) were observed:

- V_{DD}=1.25 V (W=5 nm),
- V_{DD}=1.5 V (W=10 nm),
- V_{DD}=2 V (W=20 nm),
- V_{DD}=3.25 V (W=40 nm) and
- V_{DD}=5 V (W=80 nm).

Figures 8-12 show the changes in ∆I with decreasing V_{DD} at T=250, 275, 300, 325, 350, 375 and 400 K° and W=5,10,20,40 and 80 nm. The following maximum sensitivities (max ∆I) were observed:

- V_{DD}=1.25 V (W=5 nm),
- V_{DD}=1.5 V (W=10 nm),
- V_{DD}=2 V (W=20 nm),
- V_{DD}=3.25 V (W=40 nm) and
- V_{DD}=5 V (W=80 nm).
Figure 8. $\Delta I$–$V_{DD}$ characteristics of FinFET ($W_F=5$ nm)

Figure 9. $\Delta I$–$V_{DD}$ characteristics of FinFET ($W_F=10$ nm)

Figure 10. $\Delta I$–$V_{DD}$ characteristics of FinFET ($W_F=20$ nm)

Figure 11. $\Delta I$–$V_{DD}$ characteristics of FinFET ($W_F=40$ nm)
Temperature characteristics of FinFET based… (Yousif Atalla)

Figure 12. $\Delta I$–$V_{DD}$ characteristics of FinFET ($W_F=80$ nm)

Figure 13 shows the optimum operating voltage ($V_{DD}$) based on the best temperature sensitivity and channel Fin width, where optimal $V_{DD}$ is associated with the temperature sensitivity peaks shown in Figures 8-12. The temperature sensitivity increased linearly with all the range of channel Fin width (5-80 nm). So, the lower gate Fin width ($W_F=5$ nm) with higher sensitivity can be achieved with lower working voltage ($V_{DD}=1.25$ V).

4. CONCLUSION

The effects of different temperatures (250, 275, 300, 325, 350, 375 and 400 K°) on FinFET characteristics are studied by considering different channel Fin width ($W_F=5, 10, 20, 40$ and 80 nm). For the diode mode transistor connection and increments for the current ($\Delta I$), the working voltage $V_{DD}$ must increase with increasing the gate Fin width to get the best sensitivity, so the lower Fin width has best sensitivity with lower working voltage. The linear relation between temperature sensitivity and working voltage has been result in this study with all range of channel Fin width $W_F=5$-20nm.

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