Development of Multi-Layer Fabrication Process for SFQ Large Scale Integrated Digital Circuits

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Abstract—We have developed a fabrication technology for superconducting integrated circuits with Nb-based Josephson junctions. The standard fabrication process with 10 mask levels includes 3 Nb superconducting layers and a Mo resistor layer. The influence of deposition parameters on film stress, electrical properties, and surface roughness were studied systematically. High quality Nb, Al, Mo, and SiO$_2$ films were successfully deposited for the subsequent fabrication of circuits. The circuit fabrication started with the fabrication of Mo resistors with a target sheet resistance $R_{sh}$ of 2 $\Omega$, followed by the deposition of Nb/Al-AlO$_x$/Nb trilayer Josephson-junction. The target critical current density $J_c$ was set at 6 kA/cm$^2$. Small-scale circuits such as our standard library cells have been successfully fabricated and tested, confirming the capability of our fabrication technology for superconducting integrated circuits.

Index Terms—Josephson device fabrication, SFQ circuits, Superconducting LSI, Superconducting electronics fabrication.

I. INTRODUCTION

RAPID single flux quantum (RSFQ) circuits have received much attention because of their very high processing speeds and low power dissipations. Toward real-world applications of RSFQ large-scale integrated (LSI) circuits, numerous efforts have been made to improve fabrication technologies chiefly based on Nb/Al-AlO$_x$/Nb Josephson junctions (JJs), for example, by MIT Lincoln Laboratory [1]–[3] and HYPRES [4]–[6] in the USA, National Institute of Advanced Industrial Science and Technology in Japan [7]–[9], Leibniz Institute of Photonic Technology in Germany [10].

In this paper, we present development of our standard fabrication process (SIMIT Nb03) aimed at RSFQ LSI circuits with $10^4$ to $10^5$ JJs. The process consists of with 10 mask levels including three Nb superconducting layers and one Mo resistor layer. The targeted $J_c$ for Nb/Al-AlO$_x$/Nb JJs is 6 kA/cm$^2$ and minimum $JJ$ size is 1.4 $\mu$m in diameter. The sheet resistance $R_{sh}$ of the Mo resistor layer is 2 $\Omega$. The deposition parameters for Nb/Al-AlO$_x$/Nb trilayer films were optimized for high flatness, high $T_c$, and low stress [11]. The wafer process flow is described in some detail. We eventually fabricated small-scale RSFQ circuits including our standard library cells [12] which were successfully tested.

II. FABRICATION PROCESS

A. Overview

Table I summaries the parameters of the layers, the mask levels, and minimum feature size (on the mask). The process includes a resistor layer R0, a trilayer MN0/AN0/JN0, a wiring MP1, a ground plane MP2 at the top, and a contact pad metalization PP2. All the metal layers, Mo, Nb, and Al, were deposited by DC magnetron sputtering. SiO$_2$ insulation
layers, CN0, IN0, and IP1 were deposited by plasma-enhanced chemical vapor deposition (PECVD). Photolithography for all the layers was performed using an i-line (365 nm) 5-to-1 stepper and an automatic coater/developer system. $J_c$ of the junction was fixed at 6 kA/cm² which was controlled by an O₂ exposure $E$, a product of O₂ partial pressure and time for Al oxidation. $R_{sh}$ of RN0 layer was 2 $\Omega$. The circuits were fabricated on a 4-inch silicon wafer with 300-nm-thick thermal oxide. A standard chip size was 5.2 mm × 5.2 mm.

The Nb/Al-AlOₓ/Nb trilayer was deposited on the first SiO₂ insulation layer CN0 that isolates the resistor layer RN0 from the junction base electrode MN0. The JJ fabrication in the early stage of the process, where the wafer surface is expected to be sufficiently clean and flat, has several advantages: improving the uniformity and repeatability of JJ parameters, increasing resolution and uniformity of photolithography, narrowing distribution of JJ critical current, and mitigating the impact of stress on JJ quality.

In most of the fabrication processes of Nb/Al-AlOₓ/Nb JJs, the junction barrier Al-AlOₓ layer is etched by ion beam etching (IBE) [9] or wet etching [13]. However, during the IBE process, sidewalls are sometimes formed at the edge of etched profiles due to the re-deposition effect. These sidewalls may create additional conductive paths in the insulation layer to cause a current leakage in the junctions. To avoid the sidewall wall problem due to IBE, we removed the Al-AlOₓ layer by wet etching using the automatic coater/developer system with which a photoresist developer was used as an etchant. Different from manual wet etching [13], [14], the automatic clean track system controls etch parameters such as temperature and time precisely, resulting in a high reproducibility.

**B. Nb/Al-AlOₓ/Nb Trilayer Optimization**

We investigated the deposition parameters in detail for single-layer Nb and Al, and Nb/Al-AlOₓ/Nb trilayer films, which were deposited with a load-locked multi-chamber sputtering system. Nb films were deposited by DC magnetron sputtering at the sample-holder temperature of room temperature. The surface morphology of the Nb film was investigated using an AFM for a scan area of 1 $\mu$m × 1 $\mu$m. Fig. 1 shows the root mean square (RMS) roughness of films deposited with different sputtering currents and Ar pressures. It was revealed that the RMS roughness decreased as the applied sputtering current increases and roughness increased as Ar pressure was increased. Our previous studies showed that the roughness of low Nb films should preferably be less than 2 nm [11]. To avoid an effect of unexpected fluctuations in the process, we chose the parameters that yielded a roughness less than 1.5 nm.

The stress of 150-nm-thick Nb films was measured using a laser-based film stress measurement system (Frontier Semiconductor FSM 128). The results are plotted in Fig. 2 as a function of the Ar pressure $P_{Ar}$ for different sputtering currents. The stress monotonically increases with increasing $P_{Ar}$ in the range of 0.3 Pa to 1.5 Pa. The stress also increases as the sputtering current increases. The optimal stress target of Nb film is between -100 MPa and 100 MPa, which can be achieved adjusting the current and $P_{Ar}$.

Nb films was electrically characterized using a Quantum Design PPMS system by a standard four-point measurement. The superconducting transition temperature $T_c$ and residual resistance ratio RRR = $R_{300K}/R_{9.5K}$ are plotted in Fig. 3, where $R_{300K}$ and $R_{9.5K}$ are resistance at 300 K and 9.5 K, respectively. Our criteria for the lowest $T_c$ and RRR were fixed at 9.18 K and 5, respectively. Most of the films met the criteria. Taking all the measured data into consideration, we determined the standard parameters for the Nb film deposition to be the sputtering current of 2.0 A and Ar pressure of 0.7 Pa.

Al films were deposited by the DC magnetron sputtering system in a different chamber from the Nb deposition chamber. Fig. 4 shows RRR of the 100-nm-thick Al films measured using the Quantum Design PPMS system. To obtain Al films with RRR > 5, we determined the standard parameters for the Al deposition to be the sputtering current of 0.5 A and Ar pressure of 0.5 Pa at which RRR dependence on the Ar pressure is weak.

**C. Circuit Fabrication**

The process started with the deposition of a 40-nm Mo film (RN0) which was then patterned by a reactive ion etching (RIE) with an endpoint detector using SF₆ mixed with O₂ gas at 30 mTorr. A 100-nm SiO₂ film (CN0) was deposited using PECVD. Vias in CN0 layer were fabricated using RIE with CHF₃ at 2 Pa. Then Nb/Al-AlOₓ/Nb trilayer film was fabricated in the multi-chamber DC magnetron sputtering system. First, a Nb film with a 150-nm thickness for the base electrode (MN0) was sputtered.
Fig. 3. Electrical characteristics of Nb films: (a) superconducting transition temperature $T_c$ and (b) residual resistance ratio RRR.

Fig. 4. RRR of Al films as a function of Ar pressure at different sputtering currents.

Fig. 5. Cross-section of a device fabricated by SIMIT standard fabrication process.

at $P_{Ar} = 0.7$ Pa and a sputtering current of 2.0 A, and a 12-nm-thick Al layer was then deposited at $P_{Ar} = 0.5$ Pa and a sputtering current of 0.5 A. An AlO$_x$ tunnel barrier (AN0) was formed by Al oxidation in the load-lock chamber at 4 Pa of a mixed O$_2$ ambient (15% O$_2$ mixed with 85% Ar) for 30 to 40 minutes. Another 150-nm Nb film for the counter electrode (JNO) was deposited using the same conditions as the first Nb film. The Nb films of both the base and counter electrodes were patterned and etched by inductively coupled plasma RIE (ICP-RIE) with an endpoint detector. The AlO$_x$ tunnel barrier (AN0) was removed by wet etching with a photoresist developer in an auto-coating/developing system. After the trilayer patterning, a 250-nm SiO$_2$ was deposited using PECVD, and vias in IN0 were made by RIE with the same parameters as those for the CN0 vias. 300 nm of Nb wiring (MP1) was deposited and then patterned by ICP-RIE with an endpoint detector. Then a 400-nm SiO$_2$ layer (IP1) was deposited using PECVD and vias in IP1 were fabricated with the same parameters as those for CN0 and IN0 vias. A 500-nm Nb ground plane (MP2) was deposited and patterned. Finally, a 100-nm Au contact pad (PP2) with an 8-nm Ti adhesion layer was deposited using electron-beam evaporation and patterned by a lift-off technique. Fig. 5 shows a scanning electron microscope image of a cross-section of the fabricated circuit.

The layer thicknesses and etched depths were measured with the on-wafer process control monitor (PCM) patterns during the wafer fabrication process. The alignment shifts and resolutions for the lithography processes were also monitored for all the layers. Details of the during-fabrication PCM evaluations are presented elsewhere [15].

III. Test Results

The fabrication process has been evaluated by electrical testing using PCM circuits [15]. Circuit parameters such as $J_c$ and $R_{sh}$ as well as the probabilities of the defects were chosen as evaluation criteria. Feedback of the PCM results has been made routinely to improve the fabrication technology.

Parameters related to the junction property were extracted from current voltage curves (IV curves) of un-shunted JJs. We first investigated the IV curve of a single circular un-shunted junction. Fig. 6 shows typical I-V characteristics measured at 4.2 K for a Nb/Al-AlO$_x$/Nb junction with a diameter of 1.6 μm.

To examine the controllability of current density $J_c$, whose values were systematically determined with our PCM junctions, we investigated the dependence of $J_c$ on O$_2$ exposure $E$. Fig. 7 shows the $J_c$ as a function of O$_2$ exposure $E$. $J_c$ can be empirically fitted to $J_c \propto E^{-\alpha}$ [15]. The obtained $\alpha$ values change from about 0.4 in the low-$J_c$ region to 2 in the high-$J_c$ region, which is qualitatively in a good agreement with the previously reported results [16].
Small-scale circuits were designed and fabricated by our standard process described above. Fig. 8 shows a microphotograph of an AND gate in our standard cell library [12] which was successfully tested at low frequencies as shown in Fig. 9. The experimental operating margins for the bias current were -35% to +40% for the AND gate.

IV. CONCLUSION

We have developed our standard fabrication process with Nb/Al-AlOₓ/Nb Josephson junctions for superconducting integrated circuits, which includes three superconducting layers. The critical current density \( J_c \) and minimum diameter of the junction are 6 kA/cm² and 1.4 \( \mu \text{m} \), respectively. The fabrication parameters for the Nb/Al-AlOₓ/Nb trilayer have been systematically optimized in terms of the stress, surface roughness, and electrical properties of the Nb and Al films, achieving high-quality small-area junctions. Small-scale circuits such as RSFQ logic gates in our cell library have been fabricated and successfully tested at low frequencies.

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