An Efficient Runtime Validation Framework based on the Theory of Refinement

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Abstract. We introduce a new methodology based on refinement for testing the functional correctness of hardware and low-level software. Our methodology overcomes several major drawbacks of the de facto testing methodologies used in industry: (1) it is difficult to determine completeness of the properties and tests under consideration (2) defining oracles for tests is expensive and error-prone (3) properties are defined in terms of low-level designs. Our approach compiles a formal refinement conjecture into a runtime check that is performed during simulation. We describe our methodology, discuss algorithmic issues, and provide experimental validation using a 5-stage RISCV pipelined microprocessor and hypervisor.

1 Introduction

Hardware and low-level software designs continue to increase in complexity and as a result verification has become the dominant design cost. According to a recent study by Foster about 70% of designs include embedded processors, SoC designs with over 100 IP blocks are not uncommon, the mean number of verification engineers is more than the mean number of design engineers, and even design engineers spend about half their time on verification [11].

In this paper, we introduce a new approach to dynamic verification, based on refinement. In the last decade, refinement-based methodology has been successfully used to statically verify correctness of several practical systems like pipelined microprocessors, operating systems microkernels and distributed systems [15,12]. Refinement shows that the behaviors of a concrete system, say a pipelined machine, are suitably related to the behaviors of an abstract machine, say an instruction set architecture, that serves as the specification [23]. The idea behind our method is simple. We compile a refinement conjecture into a runtime check that is performed during simulation. This allows us to check for functional correctness during testing using only this one check. To our knowledge, we are the first to propose and study the application of a theory of refinement for dynamic verification. Our approach addresses several challenges facing industry [10,59]. First, we target functional correctness. According to Foster, 50% of flaws resulting in respins are due to logic or functional correctness flaws. Second, it is difficult to determine if the set of properties and tests under consideration is complete: the Foster study that shows that over 40% of of functional flaws are due to incomplete or incorrect specifications. Third, defining oracles for
tests is expensive and error-prone: the Foster study shows that verification engineers spend 24% of their time creating tests and running simulations. Finally, properties and tests are defined in terms of low-level designs, so modifications during the design cycle lead to, possibly significant, changes to the properties being tested. The Foster study shows that over 40% of the functional flaws are due to change in the specification. This is undesirable. Furthermore, the effort to maintain properties for an industrial design can often be very large [24] and cannot be under estimated.

We briefly review refinement in Section 2, followed by the introduction of a running example in Section 3. We present our refinement-based testing method in Section 4, which includes algorithms, a theorem of correctness, some optimizations, and a discussion of the overhead incurred by our method. Experimental validation using two case studies on pipeline machine verification and a case study on the verification of a hypervisor is the topic of Section 5. After a discussion and related work, in Section 6, we end with conclusions and future work in Section 7.

2 Refinement

Refinement allows us to show that a low-level concrete system correctly implements a high-level abstract system by showing that every behavior of the concrete system is allowed by the abstract system. To bridge the gap between the concrete and abstract systems, we use a refinement map, a function that maps concrete states to the abstract states they correspond to. For example, the commitment refinement map [21] takes as an input a pipelined machine state and returns the ISA (Instruction Set Architecture) state obtained by invalidating all partially executed instructions and projecting out the programmer-observable components.

Many different notions of refinement exist ([17,18]) and our approach is quite general, but in this paper we will use WEB (Well-founded Equivalence Bisimulation) refinement [17], a notion of correctness that is well studied in the context of hardware verification [18]. In this section, we provide a brief introduction to WEB refinement. We start by defining transition systems (TS), a general, language-agnostic setting, that we use to model systems.

**Definition 1.** A TS $\mathcal{M}$ is a three-tuple $(S, \rightarrow, L)$, consisting of a set of states $S$, a transition relation $\rightarrow$, and a labeling function $L$ whose domain is $S$.

The labeling function is used to specify what is externally observable in a state. Transition systems are both simple and general, e.g., $\rightarrow$ is an arbitrary relation and there are no cardinality restrictions on $S$. Thus transition systems can be used to model infinite state machines and unbounded nondeterminism.

We now define WEB-refinement, which is defined with respect to a single transition system: the disjoint union ($\top$) of the concrete and abstract TSs.

**Definition 2.** Let $\mathcal{M}_C = (S_C, \rightarrow_C, L_C)$ be the transition system of a concrete system, $\mathcal{M}_A = (S_A, \rightarrow_A, L_A)$ be the transition system of an abstract system and
$r : S_C \rightarrow S_A$ be a refinement map. We say that $M_C$ is a WEB refinement of $M_A$ with respect to $r$, if there exists a binary relation $B$, such that $(\forall s \in S_C :: sB r(s))$ and $B$ is a WEB on $TS (S_C \uplus S_A, \xrightarrow{C \uplus A}, L)$, where $L(s) = L_A(r(s))$ for $s \in S_C$ and $L(s) = L_A(s)$ otherwise.

The definition depends on the notion of a WEB (Well-founded Equivalence Bisimulation) [10], which given a binary relation $B$ checks that any pair of states related by $B$ have identical behaviors up to finite stuttering.

**Definition 3.** $B \subseteq S \times S$ is a WEB on $M = (S, \rightarrow, L)$ iff:

1. $B$ is an equivalence relation on $S$ and
2. $(\forall s, w \in S : sBw : L(s) = L(w))$ and
3. There exist functions rankl : $S \times S \rightarrow \mathbb{N}$, rankt : $S \times S \rightarrow W$, such that $(W, \prec)$ is well-founded, and
   
   $(\forall s, u, w \in S : sBw \land s \rightarrow u :$
   
   (a) $(\exists v : w \rightarrow v : uBv) \lor$
   
   (b) $(uBw \land \text{rankt}(u) \prec \text{rankt}(s)) \lor$
   
   (c) $(\exists v : w \rightarrow v : sBv \land \text{rankl}(v, s) < \text{rankl}(w, s))$)

WEB refinement is equivalent to stuttering bisimulation refinement [10], but requires only local reasoning. This locality is the key that allows us to design efficient algorithms for testing via refinement, because it reduces the refinement problem, which is naturally expressed in terms of infinite traces (that the behaviors of the concrete system are allowed by the abstract system), to a problem expressed in terms of states and their successors.

### 3 Running Example

In this section, we describe our running example, a 3-stage pipeline processor, $MA$, and the instruction set architecture, ISA, the abstract specification for the MA machine. The running example will be used to explain our refinement-based approach to testing. We say that the MA implements the ISA only if all observable behaviors of the MA are behaviors of the ISA machine.

The stages of the MA pipelined processor are (1) fetch stage: the machine fetches an instruction pointed to by the program counter (2) load stage: the machine loads the source registers from the register file or the data memory (3) execute stage: the machine executes the instruction and updates the destination register in the register file or data memory with the result. The MA machine checks for data dependencies between adjacent instructions in the pipeline: in case the destination of the instruction in execute stage is equal to a source register of the instruction in the load stage, the MA machine stalls for one cycle. The ISA machine acts as the specification for the MA machine. It just fetches the instruction pointed to by program counter and executes it in a single step. Notice that both the MA machine and the ISA machine are deterministic.
4 Testing via Refinement

In this section, we show how to test our running example using WEB refinement. The idea is simple: we simulate the design using a test suite of programs. A program is run simultaneously on the ISA and the MA machines and at each step, we check the refinement conjecture.

Let us contrast our approach with prevailing methods used in industry, which include the use of assertions and test cases [11]. To use these methods, a team of engineers is needed to define a set of properties, a set of tests, and oracles that determine when a test passes or fails. With our refinement-based methodology, we only check one property, the WEB refinement property, and the oracle is simply the high-level abstract model (ISA). Our approach can therefore lead to significant savings of time and effort. Our approach has the added advantage that refinement completely characterizes functional correctness, whereas with traditional methods, completeness is very difficult, if not practically impossible, to achieve. We discuss this aspect in more detail in Section 6.

We do not claim that our approach completely eliminates the need for other testing methods. It does not, e.g., low-level tests and properties that check performance are needed. Also, we expect that directed tests will be needed to achieve sufficient code coverage. Nevertheless, we believe that the need for such tests will be significantly reduced if refinement-based testing is used. We provide evidence for this claim in Section 5.

We describe an algorithm for testing the WEB refinement property in Algorithm 1. The algorithm is an online algorithm, i.e., we are checking refinement as the simulation is taking place. It is possible to modify the algorithm to obtain an offline version, which takes as input the trace of the concrete system and the abstract system. The online version has several benefits over the offline version, e.g., it is simpler to describe, we do not need to store traces and we can report errors as soon as they are discovered. An offline algorithm may be easier to incorporate in an existing flow and may be easier to parallelize. In Section 5 we describe a variation of the offline algorithm to check the functional correctness of an open source pipeline processor.

We make one simplifying assumption in Algorithm 1: no pair of abstract states are labeled identically. This is a reasonable assumption, as usually one models abstract states as tuples of state components with the labeling function as the identity function. Such systems trivially satisfy our assumption. With this assumption, we can simply define the equivalence relation $B$ for checking WEB refinement as the equivalence classes induced by the refinement map.

Algorithm 1 accepts as input an initial state $s$ of the concrete system; $n$, a bound on the number of simulation steps to run; $r$, a refinement map; and $rankt$, a function that maps states of the concrete system to a well-founded domain (typically the natural numbers). We start by initializing the abstract machine state $w$ to be $r(s)$ (i.e., we apply the refinement map to $s$), the error flag to $false$, the list partition to $\langle \rangle$ (the empty list) and the two index variables $i$ and $j$ to 0. Next the algorithm loops as long as no error has been detected and $n$, the bound on the number of simulation steps to take, is positive. An inductive
invariant at line 2 is \( w = r(s) \). The body of the loop starts by selecting \( u \) to be a successor state for \( s \) (Select-concrete-next-state). If the concrete machine is nondeterministic, there can be many successors of state \( s \). The correctness of the algorithm does not depend on which state is selected, but as a practical matter, it makes sense to select states randomly using an appropriate distribution. We assume that we can replay the selections of \( u \), say because \( u \) depends on a pseudo-random number generator, but to simplify the presentation, this is not explicitly mentioned in our algorithm. Next the algorithm finds an abstract state \( v \) that is a successor of \( w \) and that matches \( u \) (i.e., \( v = r(u) \)), if such a matching state exists, and sets \textit{match} to \textit{true} (Match-abstract-next-state). How this is done depends on the abstract system. For example, if the abstract system has bounded non-determinism, one simple strategy is to iterate over the successors of \( w \), stopping when a matching state is found. If no such state exists, then \textit{match} is set to \textit{false} and \( v \) can be any abstract state. From an algorithmic correctness perspective, it is crucial that \textit{Match-abstract-next-state} always finds a matching state if it exists. If such a \( v \) exists, then the test in line 5 holds and \( u \) is matched in one step. In this case, we update \textit{partition}, a list of pairs of indices, where the \( i^{th} \) pair contains the indices of states in the concrete and abstract traces corresponding to the beginning of the \( i^{th} \) partition.

Theorem 1 If Algorithm 7 reports an error, then the concrete machine is not a WEB refinement of the abstract machine with respect to the refinement map.

Due to space limitations, the proof is omitted. Notice that given a refinement map \( r \) and a rank function, Algorithm 1 only checks local conditions; the relation between a concrete state \( s \), its successor, an abstract state \( w \) and its successor.

4.1 Optimizations for Deterministic Machines

Algorithm 1 works even when the concrete and abstract machines are nondeterministic. However, it is often the case that the abstract and concrete machines are deterministic. The algorithm can be simplified by exploiting determinism. In Figure 1 we show what the WEB refinement conjecture can be simplified to when the machines are deterministic and the abstract machine does not stutter. In the figure, \( S_C \) is the set of states of the concrete machine; \textit{concrete-step} is the function corresponding to one step of the concrete machine; \( S_A \) is the set of abstract states of the abstract machine; and \textit{abstract-step} is the step function of the abstract machine. For deterministic machines, the \textit{match-abstract-next-state} and \textit{select-concrete-next-state} functions in Algorithm 1 can be replaced by functions \textit{abstract-step} and \textit{concrete-step}, respectively. Furthermore, in case of deterministic machines, it always suffices to use \( \langle \mathbb{N}, < \rangle \) as the well-founded structure.

In our running example, the MA and ISA machine are both deterministic and the ISA machine does not stutter; hence, we can use the simplified algorithm. Next we define a refinement map \( r \), a function from MA states to ISA states that tells us what is observable in a concrete state. Given an MA state, the refinement map \( r \) invalidates all partially completed instructions in the pipeline, updates
Algorithm 1: Online WEB refinement Check

Input: $s$: concrete system state
       $n$: number of steps to run
       $r$: refinement map
       $\text{rank}_t$: rank of concrete state

Output: Partition, Error Status

1. $w \leftarrow r(s)$; $\text{error} \leftarrow \text{false}$; $\text{partition} \leftarrow \langle \rangle$; $i \leftarrow 0$; $j \leftarrow 0$;
2. do
3.   $u \leftarrow $ Select-concrete-next-state($s$);
4.   $\langle \text{match}, v \rangle \leftarrow $ Match-abstract-next-state($w$, $u$);
5.   if $\text{match}$
6.     $\text{partition} \leftarrow \text{partition} :: \langle i, j \rangle$;
7.     $i \leftarrow i + 1$; $j \leftarrow j + 1$;
8.     $s \leftarrow u$; $w \leftarrow v$;
9.   else if $r(u) = w \land \text{rank}_t(u) < \text{rank}_t(s)$
10.    $i \leftarrow i + 1$;
11.    $s \leftarrow u$;
12.   else $\text{error} \leftarrow \text{true}$;
13.   $n \leftarrow n - 1$;
14. while $n > 0 \land \neg \text{error}$;
15. return $\langle \text{partition}, \text{error} \rangle$;

the program counter and projects out the programmer observable components of the state. If neither latch is valid (the pipeline is empty) then the program counter stays the same. Otherwise, it points to the oldest valid instruction in the pipeline (the instruction in the second latch is older than the instruction in the first latch). Furthermore, since no two states of the ISA machine are labeled identically, we define $B$ to be the equivalence relation induced by refinement map $r$. The choice of a refinement map plays a crucial role in the efficiency of the algorithm. We discuss this in detail in Section 6.

$$\forall s \in S_C :: u = \text{concrete-step}(s) \land
\text{rank}_t(s) \land
v = \text{abstract-step}(w) \land v \neq r(u)$$
$$\implies w = r(u) \land \text{rank}_t(u) < \text{rank}_t(s)$$

Fig. 1: A simplified WEB refinement conjecture

Next we define the function $\text{rank}_t$ in Definition 3; given an MA state $s$ $\text{rank}_t(s)$ is the number of MA steps required to commit an instruction, i.e., take an observable step, from $s$. If $s$ has a valid instruction in the second latch, $\text{rank}_t = 0$; otherwise if there is a valid instruction in the latch for the load stage, $\text{rank}_t = 1$. As we discuss later, the ranking functions are not essential for our refinement-based testing method, but their use can help catch errors, including
performance errors. In case a rank function is not available, the algorithm can still be used by removing all references to $rank_t$. The check relating $u$, and $w$ in Algorithm 1 is the safety component and the check $rank_t(u) < rank_t(s)$ is the liveness component.

4.2 Overhead of checking WEB refinement

We now discuss the overhead of checking for WEB refinement during simulation. The overhead costs of checking the WEB refinement conjecture are indicated with a box in Algorithm 1. The cost is primarily determined by the following three factors: (1) computing the refinement map (2) comparing the result of applying the refinement map to an abstract state, and (3) computing the rank of a concrete state.

Refinement maps can be computationally expensive functions; hence, the choice of refinement map plays a crucial role in the efficiency of the algorithm. The refinement map described in Section 4 is obtained by committing an MA state and projecting out the programmer visible components. To efficiently compute the committed state, we instrument the machine using history variables, variable that record the history of programmer-observable components, but do not affect the behavior of the processor. In the MA machine, history variables record the values of the observable components of MA states before they are updated in the pipeline. Notice that for the MA machine, the program counter is the only observable component of the concrete state that is updated by a partially executed instruction. We evaluate the overhead cost of WEB-refinement checking during dynamic validation in section 5 and refer the reader to [22,19] for a detailed comparison of computational efficiency of different refinement maps in formal verification.

5 Experimental Evaluation

In this section we first evaluate the effectiveness of our method to test the functional correctness of the MA machine, our running example, and a small hypervisor. We evaluate the effectiveness of our method in detecting mutations and the overhead costs of refinement checking during simulation. The MA machine and the hypervisor, and the corresponding WEB refinement checkers based on Algorithm 1 are defined in ACL2s, the ACL2 Sedan. Next we evaluate the ease of applying the refinement-based testing methodology to an existing workflow. Towards this, we use the our method to analyze the functional correctness of a 5-stage pipeline processor based on RISC-V instruction set architecture. The processor model is described in Scala and the refinement checker is implemented in Python.

5.1 MA machine

In total we injected 25 errors in different components of the MA machine. These errors can roughly be classified into three classes: (1) Instruction classification:

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1 Experimental artifacts are available on request.
mutations injected in classifying instructions as an arithmetic/logic unit (ALU) instruction, a load/store instruction, or a particular register is meaningful for the instruction; (2) Datapath: mutations injected in computations in ALU and load/store unit (LSU). This class also includes mutations in connecting the ports of the modules; (3) Control logic: mutations injected in detecting stall conditions and stalling the pipeline on data and structure hazards, error in branch recovery mechanism like invalidating instructions in the pipeline on the wrong path, etc.

If we were to check functional correctness of the MA machine using the property-based approach, we would first specify a set of properties to ensure absence of each of the possible bugs. For example, we will have to specify a set of properties to ensure that the machine correctly handles pipeline hazards due to data dependencies between two instructions in the pipeline. For the MA machine, the property can be stated informally as follows: if the two pipeline latches have valid instructions, and if the older register has data dependency on the younger instruction, i.e., the destination register of the older instruction is equal to any of the two source registers of the younger instruction, then a stall signal is asserted in the next cycle. In addition, we need another property that ensures that if the stall signal is asserted in a cycle, the program counter does not change in the next cycle. Similarly, we would need to specify a property for each possible scenario that we want to check during simulation. These properties are then compiled as runtime monitors that check for violations during simulations-based testing.

In contrast, in our approach we specify and check the WEB refinement conjecture (Figure 1) using a test program as input and Algorithm 1. Our test suite consisted of four generic programs: copy an array of memory from one location to another, perform multiplication by iterative addition, perform exponentiation by iterative multiplication, and a short sequence of 10 random addition and subtraction instructions. Notice that our test programs are generic and are not crafted to find any particular error. In an industrial setting, we would expect to have a larger set of programs, which will only make it easier to find errors. Table 2a lists the errors injected in the MA machine. If the bug was detected by refinement testing, we indicate this with a ✓ mark in the second column of the table. In total 18 of the 25 injected errors were detected. Notice that three of the errors marked * in Table 2a are not functional bugs and all of these errors falsely detect pipeline data hazards, resulting in stalling behavior that is not necessary. This is a loss of performance, but not a functional failure. Error in decoding that bez (a conditional branch instruction) uses rb as one of the source register (mutation 7) and error in checking the validity of a branch instruction while invalidating a pipeline latch (mutation 14) are functional bugs that with a more well-rounded set of programs are easy to detect. We also added two difficult-to-detect mutations. One is a failure to stall the pipeline when the values of the two operands are equal (mutation 15) or when the value of an operand is an arbitrary value (mutation 16). The probability of stumbling on these bugs during testing is low (as is the probability of a designer introducing these bugs). Finding such errors requires the use of advanced counter-example generation techniques [5].
We now analyze the overhead cost to check for WEB refinement in simulation. In Figure 2(b) we plot the running times for simulating the MA machine (x-axis) vs the running times for simulation with refinement testing enabled (y-axis). The points shown indicate simulations ranging from 10,000 to 100,000 steps. The slope of the fitting line is $\sim 2$, which amounts to a slowdown of approximately 100%. Also notice that the points in the plot are on either on the fitting line or near it, indicating that the overhead of the checker does not increase as we increase the number of steps in a simulation run.

5.2 Simple Hypervisor

A hypervisor enables multiple operating systems (guests) to share resources without interfering with one another. It achieves this by virtualizing the host processor and the memory; a guest executing on a virtualized system only exhibits behaviors that are admissible when the guest is executing directly on the hardware. In this case study, we implement a model of a simple hypervisor [4] and check its functional correctness using WEB refinement in ACL2s.

A run of the virtualized system is defined as follows: The host processor is time shared among multiple guests. At any given time, only one guest is active (current guest) on the host processor. The hypervisor configures the host proces-
sor to execute in user mode, irrespective of the mode of operation requested by
the current guest, and to use the shadow page-table of the current guest in the
host memory. The current guest directly executes instructions in the instruction
memory on the host processor until execution of an instruction results in an
exception. In case the exception is “real”, i.e., it is not a result of the guest ex-
ecuting in a virtualized environment, the hypervisor passes the exception to the
guest. The exception is then handled by the exception handler designated by the
guest. Otherwise, the exception handled by the hypervisor; the hypervisor saves
the state of the host processor in the processor control block (pcb) for the cur-
rent guest, emulates the instruction, updates the pcb and shadow page-table (if
required), and finally restores the state of the host processor using the updated
pcb. The hypervisor hosts each guest memory into disjoint regions of the host
memory and controls the translation from a guest virtual address to physical
address.

A simple high-level abstract system where each guest executes on a dedicated
processor and memory, serves as a specification for the virtualized system. In-
formally, the virtualized system is correct if an observable behavior of a guest in
the virtualized system is identical to the observable behavior of the guest in the
abstract system. We encode the function correctness of the virtualized system
using WEB refinement. First we define the refinement map; it extracts the state
of the current guest from combination of the state of the host processor and
the current guest’s pcb in the hypervisor. For all other guests, the corresponding
pcb in the hypervisor completely specifies the state of the guest in the abstract
system. The refinement map also extracts the guest memory partition for each of
the guest from the host memory. Next we define the well-founded structure and
the ranking functions. Notice that the abstract system does not stutter. Hence,
like in the pipeline processor case study, we only need to define one ranking func-
tion, rankt to account for stuttering in the concrete system. Furthermore, since
the concrete system is deterministic, it suffices to use $\langle \mathbb{N}, < \rangle$ as the well-founded
structure. We define the rankt as follows: if there is no pending exception in
a MA state, the rank is 1 else it is 0. Under these conditions, we can use the
simplified WEB refinement in Figure 1.

**Mutations:** We manually injected mutations in the virtualized system to eval-
uate the effectiveness of refinement testing to detect bugs. In this case study,
we restrict our attentions to mutations in the hypervisor component of the vir-
tualized system. The mutations are informally classified into four classes: (1)
Save/Restore: mutations injected in save and restore routines of the host pro-
cessor state in the hypervisor; (2) Emulation of a privilege instruction: mutations
injected in hypervisor routines that emulate the execution of privileged instruc-
tions; (3) Shadow Page Table: mutations injected in hypervisor routines that
sync the shadow page-table with the guest page-table; (4) Address Calculation:
mutations injected in the address calculations performed during the translation

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2 For simplicity we assume that host memory is greater than sum of all guest memory
plus memory required to store data-structures for the hypervisor.
of guest virtual address to host physical address. Table 3a shows that refinement testing found all of these errors.

| Errors Injected                  | Detect |
|----------------------------------|--------|
| Save/Restore                     |        |
| 1. wrong pc for inst responsible for exception |        |
| 2. wrong page-table origin       |        |
| 3. check for host mode instead of guest mode |        |
| Simulation of Privileged Inst    |        |
| 4. wrong pc used to fetch the inst to emulate |        |
| 5. do not increment pc on a move immediate value to PTO |        |
| 6. do not increment pc on a move immediate value to PTL |        |
| Sync Shadow Page Table           |        |
| 7. use old pto to sync GPT and SPT |        |
| 8. use old ptl to sync GPT and SPT |        |
| Address calculation              |        |
| 9. physical addr of guest pte in handling page-faults |        |
| 10. addr of page-table entry in host page-table |        |
| 11. addr of page-table entry in SPT |        |
| Hosting multiple guests          |        |
| 12. Scheduler preempting a guest  |        |
| 13. Guest memory separation      |        |
| Others                           |        |
| 14. Fail to update the exception status after emulation |        |

(a) Mutations injected

![Fig. 3: Refinement checker for the Hypervisor](image)

In Figure 3b, we plot the running time for simulating the virtualized system with \((y\text{-axis})\) and without refinement checker \((x\text{-axis})\), where the number of steps ranges from 10,000 to 100,000. The slope of the fitting line (blue) is \(\sim 65\). The reason for the large slow down is the sub-procedure in the refinement map used to compute the guest memory from the host memory; it traverses the host memory and extracts the guest memory for each guest in the system. If the size of the memory is large, which is often the case, this is prohibitively expensive. To reduce the cost of computing the refinement map, we add a history variable to the virtualized system that records the guests accesses to the host memory. Note that augmenting the system with the history variable does not modify its observable behavior. We then modify the refinement map to use the history variable to construct the updated guest memory from the initial guest memory. We again compare the running times for simulating the virtualized system with and without the modified refinement map. In this case the slope of the fitting line (green) is \(\sim 3.6\), i.e., we get over 18 times speed up in the running time of the virtualized system with the modified WEB refinement check. This experiment reaffirms that the refinement map plays a crucial role designing an efficient refinement checker.

Notice that in a property-based testing methodology, we would have to describe a property for each of the mutations described in Table 3a. Furthermore, even such a list of properties is not complete, e.g., it does not check that after handling an exception, the hypervisor eventually resumes executing the guest on the host processor directly. In contrast, WEB refinement check accounts for such liveness properties of the hypervisor.
5.3 RISC-V Based Pipelined Processors

We next evaluate the effectiveness of our methodology to check functional correctness of pipeline processors based on RISC-V instruction set specification [1]. RISC-V is an open source specification, which is being widely adopted both for educational and commercial use. Among several open source implementations available, we choose to evaluate our methodology using the Sodor processor collection, a collection of 2, 3, and 5-stage pipeline processor models [2]. These processors implement the RISC-V 32-bit integer base user-level instructions using different micro-architectural features. The models are described in Chisel, a hardware description language embedded in Scala; it then can be translated to either a fast bit and cycle-accurate C++ simulator or a low-level Verilog description suitable for hardware emulation [7]. The open source community has also developed Spike, an executable model of the RISC-V instruction set specification, that serves as “golden standard” for execution. In addition, the community has also developed an extensive testing infrastructure consisting of several directed tests and benchmark programs. These tests are described in C and can be compiled to execute on both the Spike and Sodor processors.

We evaluate the applicability of the refinement-based testing methodology to check functional correctness of the 5-stage pipeline Sodor processor (5SP). It is a single-issue in-order pipeline processor that supports full bypassing between functional units. We use Spike as a high-level abstract specification for checking functional correctness of the Sodor processor.

As in the previous two case studies (Section 5.1 and 5.2), the correctness of the 5SP processor can be specified by a single WEB refinement check. Moreover, the 5SP processor and the Spike are deterministic systems and the later does not stutter; hence we can use the simplified WEB refinement conjecture (Figure 1) to design an efficient runtime checker.

Before we discuss the challenges in implementation of the refinement checker for the 5SP processor, we first define the refinement map $r$, and the ranking function $\text{rank}_t$. Refinement map $r$ takes as an input a state of the 5SP processor, invalidates all partially executed instructions, then based on the number of partially executed instructions it moves the program counter back, and finally projects all programmer-observable components to return a state of the Spike. In order to efficiently compute the refinement map, we instrument the processor implementation using history variables. We add a valid bit corresponding to each pipeline latch; the valid bit is set to true if the instruction in the pipeline stage is valid. In addition, we also record the program counter for each partially executed instruction in the pipeline. The instrumentation of the 5SP processor to add these history variables required only a few additional lines of code. Next, we define the ranking function $\text{rank}_t$. Given a state of the 5SP processor, its rank is defined by the minimum number of steps the processor needs to commit a partially executed instruction, i.e., take an observable step.

Now we are ready to discuss the implementation of the WEB refinement checker. Notice that the use of Algorithm 1 to implement the refinement checker requires a mechanism to control the stepping of both the 5SP processor and
Spike (Line 3 and 4 in Algorithm 1). Though possible (as in the previous two case studies), it would involve substantial modifications to the existing simulation and testing infrastructure of Sodor processors, an undesirable scenario for adoption of the refinement-based testing methodology. Therefore, we design an alternative implementation of the refinement checker that decouples the execution of the 5SP processor, the Spike simulator, and the computation of WEB refinement check. We spawn three independent threads: (1) the concrete system (Sodor processor) simulation; (2) the abstract system (Spike) simulation; and (3) the refinement checker. Thread (1) and (2) acts as producers and thread (3) acts as the consumer; the communication between the producers and the consumer is asynchronous. This alternative implementation only requires a mechanism in the simulator to communicate its state to the refinement checker in each cycle. For the 5SP simulator and the Spike simulator that are implemented in C++, this is done by simply adding `printf` statements.

We implement the WEB refinement checker in Python. The refinement checker spawns off the 5SP simulator and the Spike simulator as independent processes. In each cycle, the simulator write the state of the system into a FIFO. The refinement checker reads the state of the system from the FIFOs and checks if the WEB refinement conjecture holds. Recall that the WEB refinement check is local and thus only needs to analyze the current state of the systems and their successors. In case the checker detects a violation, it outputs the offending state and quits. Else it evicts the analyzed states of the system from the respective FIFOs. In Figure 4, we plot the running time for simulating the 5SP with (y-axis) and without (x-axis) the refinement checker; the number of cycles range from 300000 to 1500000. The slope of the fitting line is $\sim 1.8$, which amounts to a slowdown of approximately 80%. The memory footprint of the refinement checker is small; this is because the WEB refinement check is local and only

![Fig. 4: Overhead cost for the 5-stage pipeline Sodor processor](image-url)
requires us to analyze states and their successors. Also notice that points on the plot are either on the fitting line, or near it; this indicates that the overhead cost of the refinement checker does not increase with increase in the number of cycles in a simulation run. This is desirable property in long running simulations.

To evaluate the effectiveness of the refinement-based testing methodology to detect bugs, we introduced 20 mutations in 5-state pipeline Sodor processor. These mutations are similar to the ones introduced in the MA machine (Table 2a). We use the generic programs like quick sort and the tower of Hanoi puzzle in the RISC-V test suite [3]. With this test suite, the refinement checker could detect all mutations that could result in functional violations.

6 Discussion and Related Work

In this section, we discuss how our refinement-based testing overcomes several major drawbacks of the standard testing methods. In the previous section, we showed that the formal refinement conjecture can be compiled into an efficient runtime check that can be used to detect bugs in a dynamic validation workflow. Furthermore, unlike temporal properties, that can span multiple steps of the machine, WEB-refinement check is local, i.e., we only check the relation between a state and its successor. This allows us to limit the overhead cost without compromising on the expressivity. The overhead of a refinement checker during simulation can further be improved by exploiting domain specific knowledge (deterministic machines), augmenting the machine with appropriate history variables, choosing an efficient refinement map, and checking only for the safety or the liveness component of the refinement check. In contrast, in a property-based methodology, properties are expressed in an assertion language, like SVA and PSL, and compiled into a (finite-state) automaton. In the worst case, the automaton can be exponential in the size of the property and the overhead of checking the property during simulation can be prohibitively expensive. In [24], it is reported that depending on the number and the kind of properties they express, property checking can degrade simulation speed anywhere from 25% to 100%.

A major concern with current testing methods is how to decide if the set of properties or tests is “complete.” An alert reader would have noticed that the set of properties corresponding to the mutations in Section 5.1 does not include the one that checks that if the pipeline in the MA machine stalls, say due to data dependency, it is eventually un-stalled and resumes fetching new instructions. With this incomplete set of properties, an MA machine that never resumes fetching new instructions will be incorrectly declared as functionally correct. As systems grow in complexity, it becomes increasingly difficult to answer the question of completeness. In [14], the authors describe their experience in a twenty person year effort to formally verify the Execution Cluster, a component of the Intel Core i7 microprocessor that is responsible for functional behavior of all microinstructions. It is reported that at the end of their effort they only missed detecting five bugs found in the fabricated processor. They attributed three of these misses
to “incorrect formal specification” and two of these misses to “formal verification work not being completed early enough”. Both reasons are indicative of the difficulty in specifying a correct and complete set of properties for complex designs. An industry-wide survey in 2014 shows that over 50% of respins are due to logic or functional errors; 40% of these functional flaws are attributed to incorrect/incomplete specifications [11]. In contrast, WEB-refinement completely characterizes the functional correctness of the design and therefore does not suffer from the incompleteness problem.

In section 4 the locality of WEB refinement conjecture (reasoning only about states and their successors) played a key part in designing an efficient runtime checker. This quality of WEB refinement also makes it amenable for automated reasoning using existing formal verification tools [19,20]. Hence, refinement-based approach satisfies a key requirement: a specification must be effectively analyzed both in a dynamic validation workflow as well as in a formal verification workflow. The advantage of such a specification is that it acts as a bridge between dynamic validation and formal verification.

Finally, we note that our refinement-based testing can be used in a variety of ways to combine dynamic and static verification methods. For example, we might prove that a high-level, abstract system satisfies a set of desired properties. This is much easier to do at the abstract level than at the concrete level. If we can statically show that concrete system refines the high-level system, say using WEB refinement, then, since WEB refinement preserves all the CTL\"X properties (both safety and liveness properties), we can infer that the concrete system satisfies all the temporal properties that were validated for the abstract system. Such a proof may be difficult to perform. Instead, we can use refinement-based testing to gather evidence that the concrete system refines the abstract system.

7 Conclusions and Future Work

In this paper we introduced a refinement-based methodology for testing functional correctness of hardware systems and low-level software. We showed that our methodology is effective in detecting bugs and can be easily integrated in existing simulation workflows. We introduced an effective algorithm for checking WEB refinement during simulation. For future work, we plan to explore the use of refinement-based testing to check the functional correctness of nondeterministic systems. Also the notion of WEB refinement is compositional and supports top-down stepwise refinement methodology; we plan to explore how to fully exploit the compositionality of refinement to test complex, hierarchical designs with external IP components.

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