Integration of 3-Level MoS₂ Multibridge Channel FET With 2D Layered Contact and Gate Dielectric

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Abstract—Multi-bridge channel field effect transistor (MBCFET) provides several advantages over FinFET technology and is an attractive solution for sub-5 nm technology nodes. MBCFET is a natural choice for devices that use semiconducting layered materials (such as, MoS₂) as the channel due to their dangling-bond-free ultra-thin nature and the possibility of layer-by-layer transfer. MoS₂-based MBCFET is thus an attractive proposition for drive current boost without compromising on the electrostatics and footprint. Here we demonstrate a 3-level MoS₂ MBCFET, where each vertically stacked channel is dual-gated to achieve a saturation current of 174.9 µA (which translates to 90 µA per µm footprint width (@2.7 µm channel length), a near-ideal sub-threshold slope of 63 mV/dec, and an on-off ratio >10⁸. This work sets the benchmark for layer-material-based MBCFET in terms of the number of parallel channels integrated, simultaneously providing high drive current and excellent electrostatic control.

Index Terms—MBCFET, 2D materials, drive current.

I. INTRODUCTION

The transistor dimensions have shrunk aggressively over the past few decades, helping to improve performance and pack more functionality per unit area. During the scaling pathway, non-planar FinFET technology replaced the planar technology to overcome short channel effects. However, for beyond-5 nm technology nodes, there are several challenges posed by the FinFET technology. This includes continued fin width scaling to control short channel effects, fin height scaling to enhance drivability, and lack of flexibility in enhancing effective width through a discrete number of fins.

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II. PROPOSED DEVICE AND SCALABILITY PROJECTION

The scalability of a transistor to shorter channel lengths is an essential aspect when selecting a suitable device design. To illustrate the electrostatic control at scaled geometry, we perform a 2D simulation of two different MBCFET architectures. In one of the designs, a pair of double-gates control all the three channels of the transistor [see Fig. 1(a)], which we call a double-gated (DG) structure. In the other design, each of the three channels is controlled by dual-gates [Fig. 1(b)], which we call a gate-all-around (GAA) structure.

The simulation is performed by self-consistently solving the 2D Poisson and ballistic transport equations in the device [14]. The predicted sub-threshold slope (SS) of each design is shown in Fig. 1(c), as a function of the channel length. We observe that although the DG structure offers an SS of ~60 mV/dec at longer channel lengths (≥20 nm), the SS of the device increases to ~114 mV/dec at a gate length of 5 nm. In contrast, the SS increase in the GAA device is minimal, and even at a channel length of 5 nm, the device exhibits an SS of 62 mV/dec.

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Fig. 1. Schematic representation of (a) double gate (DG) and (b) gate-all-around (GAA) structure. (c) Simulated sub-threshold slope as a function of channel length for both structures. (d-e) Simulated conduction band profiles of GAA (left panels) and DG (right panels) along the three channels (marked 1, 2, and 3) with a channel length of (d) 20 nm and (e) 5 nm. Simulated transfer characteristics of (f) DG and (g) GAA structures under depletion-mode (normally-on) operation. A threshold shift is found in the central channel of DG structure. We assumed an effective oxide thickness (EOT) of 2 nm for each of the gate insulators.

The conduction band profiles along different channels (marked as 1, 2, and 3) in the GAA and DG structures are shown in Figs. 1(d) and 1(e) with channel lengths of 20 and 5 nm, respectively. Even at a channel length of 20 nm, the DG structure starts displaying drain-induced barrier lowering (DIBL). However, the GAA structure shows no such sign. The simulated band profile of all the channels in a GAA structure is essentially the same, but in the DG structure, the barrier height of the central channel is significantly lower. The lack of electrostatic control on the central channel in the DG structure is further illustrated by the simulated transfer characteristics in Fig. 1(f). This would cause different threshold voltages for different channels, which is undesirable. However, the symmetry of the GAA structure mitigates this problem efficiently [Fig. 1(g)]. This scalability of the GAA structure prompts us to fabricate this design, although this structure has a more involved fabrication procedure.

III. DEVICE FABRICATION AND MEASUREMENT

The step-by-step fabrication process of the MBCFET is schematically illustrated in Fig. 2(a). The fabrication starts with creating Au pads on 285 nm SiO$_2$/Si wafer using optical lithography, metal deposition, and subsequent lift-off. Mechanically exfoliated few-layer-thick hBN is then dry-transferred (using PDMS) onto a pre-patterned Au electrode. An exfoliated 1L-MoS$_2$ flake is then transferred onto the hBN to form the first channel. Few-layer graphene (FLG) flakes with sharp edges are used to make contact from the 1L-MoS$_2$ to the Au electrodes, which form the drain and source contacts. This stack is then capped with another few-layer-thick hBN. The entire stack is annealed in vacuum (pressure $\sim 10^{-6}$ torr) at 200°C for 3 hours to remove trapped air/residues between the layers. Another FLG flake is then transferred on top to form the double gate structure. This FLG layer acts both as the top gate for the first channel and also as the bottom gate of the second channel. The entire stack at this point is schematically illustrated in the left panel of Fig. 2(b). The stack is further built by repeating the above steps to make the two-channel and three-channel device.
The thickness of the hBN gate dielectric is chosen to be $\sim 15$ nm for all the channels. The cross-section of the device and the corresponding optical image at the three different stages are shown in Figs. 2(b) and (c), respectively. A combination of the annealing steps and the atomic smoothness of the thin FLG S/D contact, hBN gate dielectric and FLG gate contact is likely to help maintain the flatness of the channels [15].

Measurements are taken at each of these three stages to obtain the performance of one-, two-, and three-channel device. All the three source electrodes (and similarly, the three drain electrodes and the four gate electrodes) are shorted together in the device. Two such devices (devices A and B) are fabricated and measured. All measurements are performed at 295 K using a Keithley 4200 parametric analyzer, keeping the device in Lakeshore CRX-6.5K probe station under vacuum (pressure $< 10^{-4}$ torr).

### IV. Results and Performance

The effective channel length and width for the two fabricated devices are shown in Table I. The measured transfer characteristics of device A are depicted in Fig. 3(a-b), both in log (left axis) and linear (right axis) scale for two different drain biases ($V_D$), namely 0.05 and 2 V. Each plot contains the characteristics of the one-, two-, and three-channel configurations. The off current ($I_{on}/I_{off}$) of the 3-channel configuration is around $\sim 10$ fA (which is the limit of our measurement accuracy) at $V_D = 50$ mV, which increases to $\sim 100$ fA at $V_D = 4$ V. This leads to a large on-off ratio (I$_{on}$/I$_{off}$) of $> 10^8$ indicating the robustness of the device to suppress the leakage current. The SS obtained from Fig. 3(a-b) is near-ideal, $\sim 63$ mV/dec over several decades of drain current ($I_D$), and does not vary with $V_D$. This is attributed to the exceptional electrostatics due to the atomically thin monolayer MoS$_2$ channels and the clean hBN/MoS$_2$ interfaces.

The output characteristics of the device are plotted in Fig. 3(c-d) for $V_G = 0.5$ and 2 V. We observe linear characteristics at lower $V_D$ indicating ohmic behaviour of the FLG-MoS$_2$ contacts. Due to the vdW nature of the contact interface, we expect a highly de-pinned contact [16], [17]. The good quality of the contact further helps to achieve excellent drain current saturation at higher $V_D$, as depicted by the characteristics.

The scaling of the on current with an increase in the number of stacked channels is clearly illustrated in Fig. 3(c-d), which is an efficient way of effective-width scaling without consuming an additional horizontal footprint.

From Fig. 3(a-b), we note that the threshold voltage ($V_{th}$) of the three different channel configurations exhibits a small variation with the number of channels stacked. This arises due to a variation in the thickness of the gate dielectric and the contact quality between FLG and MoS$_2$. The use of Au (having higher work function compared with FLG) back gate electrode for the first channel may also contribute to the same. As a result of such $V_{th}$ variation with the number of channels, the effective enhancement in the current with the number of channels remains a function of the gate voltage ($V_G$). The inset of Fig. 3(d) shows the scaling of the on-current at $V_G = 2$ V, after normalizing with respect to the channel dimensions.

Note that all the characteristics in Fig. 3 are hysteresis-free (sweep directions indicated by black arrows). MoS$_2$ channel-based FET devices are often prone to hysteresis, which largely arises due to trapping from moisture, residues, and other surface effects. The vacuum annealing steps and all the channels being encapsulated by hBN/graphene from top and bottom effectively removed the hysteresis almost completely.

The transfer and output characteristics of the 3-channel configuration (device A) are shown in Fig. 4(a) for $V_G$ and $V_D$, both varying up to 4 V. The SS remains intact at 63 mV/dec irrespective of the $V_D$, even up to 4 V. The performance of devices A and B is summarized in Table I. We obtain a saturation current of 174.9 $\mu$A from device B under 3-channel configuration at $V_D = 4$ V. This translates to a saturation current of 90 $\mu$A per $\mu$m footprint width, with an on-off ratio $> 10^8$. The performance of devices A and B is compared [18] with other MoS$_2$ based MBCFETs in Table II.

### V. Conclusion

In conclusion, we demonstrated a 3-level MoS$_2$-channel MBCFET with a large drive current while maintaining a near-ideal sub-threshold slope and a large on-off ratio. The ability to perform a layer-by-layer transfer, coupled with the ultra-thin body of the channel shows a path towards integrating several more channels vertically - a viable option to boost the drive current without increasing the footprint. The demonstrated technique, when combined with a more optimized contact process, can further enhance the drive current. This is a promising solution not only for layered material-based highly scaled CMOS technology, but also for low-cost thin-film transistor (TFT) technologies.

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**TABLE I**

| Parameter          | Device A | Device B |
|--------------------|----------|----------|
| $L_{ch}$ (ch1, ch2, ch3) [\(\mu m\)] | 3.5, 4.5, 6.6 | 1.6, 4.5, 3.9 |
| $W$ (ch1, ch2, ch3) [\(\mu m\)] | 2.3, 10, 2.5 | 2.6, 1, 2.2 |
| Gate dielectric (hBN) thickness [nm] | $\sim 15$ | $\sim 15$ |
| FLG S/D thickness [nm] | 10-15 | 10-15 |
| On current ($V_G=4\,V$, $V_D=4\,V$) [\(\mu A\)] | 110.28 | 174.9 |
| Off current [\(\mu A\)] | $< 1$ | $< 1$ |
| $I_{on}/I_{off}$ | $> 10^8$ | $> 10^8$ |
| SS [mV/dec] | 63 | 65 |

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**TABLE II**

| Parameter          | This work (A) | This work (B) | [8] | [11] | [12] |
|--------------------|---------------|---------------|-----|------|------|
| $L_{ch}$ [\(\mu m\)] | 5.4* | 2.7* | 12 | 0.37 | 0.16 |
| Channels | 3 | 3 | 2 | 2 | 2 |
| $I_{on}/I_{off}$ | 50 | 90 | 2.9 | 535 | 700 |
| SS [mV/dec] | 63 | 65 | 130 | 126 |

* $I_{on}$ calculated as the harmonic mean of the lengths of the three channels.
REFERENCES

[1] G. Bae, D.-I. Bae, M. Kang, S. Hwang, S. Kim, B. Seo, T. Kwon, T. Lee, C. Moon, Y. Choi, K. Okawa, S. Masuoka, K. Chun, S. Park, H. Shin, J. Kim, K. Bhawalka, D. Kim, W. Kim, J. Yoo, H. Jeon, M. Yang, S.-J. Chung, D. Kim, B. Ham, K. Park, W. Kim, S. Park, G. Song, Y. Kim, M. Kang, K. Hwang, C.-H. Park, J.-H. Lee, D.-W. Kim, S.-M. Jung, and H. Kang, “3 nm GAA technology featuring multi-bridge-channel FET for low power and high performance applications,” in *IEDM Tech. Dig.*, Dec. 2018, pp. 28.7.1–28.7.4, doi: 10.1109/IEDM.2018.8614629.

[2] S. Barraud, B. Previtali, C. Vizioz, J. M. Hartmann, J. Sturm, J. Lassarre, C. Perrot, P. Rodriguez, V. Loup, A. Magalhaes-Lucas, R. Kies, G. Romano, M. Cassé, N. Bernier, A. Jannaud, A. Grenier, and F. Andrieu, “7-levels-stacked nanosheet GAA transistors for high performance computing,” in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2020, pp. 1–2, doi: 10.1109/VLSITechnology18217.2020.9265025.

[3] S.-Y. Lee, E.-J. Yoon, S.-M. Kim, C. W. Oh, M. Li, J.-D. Choi, K.-H. Yeo, M.-S. Kim, H.-J. Cho, S.-H. Kim, D.-W. Kim, D. Park, and K. Kim, “A novel sub-50 nm multi-bridge-channel MOSFET (MBCFET) with extremely high performance,” in *Proc. Symp. VLSI Technol.*, Jun. 2004, pp. 200–201, doi: 10.1109/VLST.2004.1345478.

[4] X. Huang, C. Liu, Z. Tang, S. Zeng, L. Liu, X. Hou, H. Chen, J. Li, Y.-G. Jiang, D. W. Zhang, and P. Zhou, “High drive and low leakage current MBC FET with channel thickness 1.2 nm/0.6 nm,” in *IEDM Tech. Dig.*, Dec. 2020, pp. 12.1.1–12.1.4, doi: 10.1109/IEDM13553.2020.9371941.

[5] E.-J. Yoon, S.-Y. Lee, S.-M. Kim, M.-S. Kim, S. H. Kim, L. Ming, S. Suk, K. Yeo, C. W. Oh, J. dong Choi, D. Choi, D.-W. Kim, D. Park, K. Kim, and B.-I. Ryu, “Sub 30 nm multi-bridge-channel MOSFET (MBCFET) with metal gate electrode for ultra high performance application,” in *IEDM Tech. Dig.*, Dec. 2004, pp. 627–630, doi: 10.1109/IEDM.2004.1419244.

[6] R. Ritzenhaler, H. Mertens, V. Pena, G. Santoro, A. Chasin, K. Kenis, K. Devriendt, G. Mannaert, H. Dekkers, A. Dangol, Y. Lin, S. Sun, Z. Chen, M. Kim, J. Machiellot, J. Mitard, N. Yoshida, N. Kim, D. Mocuta, and N. Horiguchi, “Vertically stacked gate-all-around Si nanowire CMOS transistors with reduced vertical nanowires separation, new work function metal gate solutions, and DC/AC performance optimization,” in *IEDM Tech. Dig.*, Dec. 2018, pp. 21.5.1–21.5.4, doi: 10.1109/IEDM.2018.8614528.

[7] H. Mertens, R. Ritzenhaler, A. Chasin, T. Schram, E. Kunnen, A. Hikavyy, L.-A. Ragnarsson, H. Dekkers, T. Hopf, K. Wostyn, K. Devriendt, S. A. Chew, M. S. Kim, Y. Kikuchi, E. Rosseel, G. Mannaert, S. Kubiczek, S. Denuwkerck, A. Dangol, N. Bosman, J. Geyten, P. Carolan, H. Bender, B. Barla, N. Horiguchi, and D. Mocuta, “Vertically stacked gate-all-around Si nanowire CMOS transistors with dual work function metal gates,” in *IEDM Tech. Dig.*, Dec. 2016, pp. 19.7.1–19.7.4, doi: 10.1109/IEDM.2016.7838456.

[8] X. Huang, C. Liu, S. Zeng, Z. Tang, S. Wang, X. Chen, D. W. Zhang, and P. Zhou, “Ultrathin multibridge channel transistor enabled by van der Waals assembly,” *Adv. Mater.*, vol. 33, no. 37, Aug. 2021, Art. no. 2102201, doi: 10.1002/adma.202102201.

[9] C.-J. Liu, Y. Wan, L.-J. Li, C.-P. Lin, T.-H. Hou, Z.-Y. Huang, and Y. P.-H. Hu, “2D materials-based static random-access memory,” in *Proc. Adv. Mater.*, Dec. 2021, Art. no. 2107894, doi: 10.1002/adma.202107894.

[10] Y. Xia, L. Zong, Y. Pan, C. Chen, L. Zhou, Y. Song, L. Tong, X. Guo, J. Ma, S. Gou, Z. Xu, S. Dai, D. W. Zhang, P. Zhou, Y. Ye, and W. Bao, “Wafer-scale demonstration of MBC-FET and C-FET arrays based on two-dimensional semiconductors,” *Small*, vol. 18, no. 20, Apr. 2022, Art. no. 2107650, doi: 10.1002/smll.202107650.

[11] R. Zhou and J. Appenzeller, “Three-dimensional integration of multichannel MoS2 devices for high drive current FETs,” in *Proc. 7th Device Res. Conf. (DRC)*, Jan. 2018, pp. 1–2, doi: 10.1109/DRC.2018.8442137.

[12] X. Xiong, A. Tong, X. Wang, S. Liu, X. Li, R. Huang, and Y. Wu, “Demonstration of vertically-stacked CVD monolayer channels: MoS2 nanosheets GAA-FET with $I_{ON} > 700 \mu A$ and MoS2/WSe2 CFET,” in *IEDM Tech. Dig.*, 2021, pp. 7.5.1–7.5.4, doi: 10.1109/IEDM19574.2021.9720533.

[13] K. Majumdar, C. Hobbs, and P. D. Kirsch, “Benchmarking transition metal dichalcogenide MOSFET in the ultimate physical scaling limit,” *IEEE Electron Device Lett.*, vol. 35, no. 3, pp. 402–404, Jan. 2014, doi: 10.1109/LED.2014.2300013.

[14] A. Rahman, J. Guo, S. Datta, and M. Lundstrom, “Theory of ballistic nanotransistors,” *IEEE Trans. Electron Devices*, vol. 50, no. 9, pp. 1853–1864, Aug. 2003, doi: 10.1109/TED.2003.815366.

[15] Z. Cheng, H. Zhang, S. T. Le, H. Abuzaid, G. Li, L. Cao, A. V. Davydyov, A. D. Franklin, and C. A. Richter, “Are 2D interfaces really flat?” *ACS Nano*, vol. 16, no. 4, pp. 5316–5324, Apr. 2022, doi: 10.1021/acs.nano.1c11493.

[16] K. Muraki, M. Dandu, K. Watanabe, T. Taniguchi, and K. Majumdar, “Accurate extraction of Schottky barrier height and universality of Fermi level de-pinning of van der Waals contacts,” *Adv. Funct. Mater.*, vol. 31, no. 18, Feb. 2021, Art. no. 2010513, doi: 10.1002/adfm.202010513.

[17] T. Roy, M. Tosun, J. S. Kang, A. B. Sachid, S. B. Desai, M. Hettick, C. C. Hu, and A. Javey, “Field-effect transistors built from all two-dimensional material components,” *ACS nano*, vol. 8, no. 6, pp. 6259–6264, Apr. 2014, doi: 10.1021/nn501723y.

[18] Z. Cheng, C.-S. Pang, P. Wang, S. T. Le, Y. Wu, D. Shahjrdi, I. Radu, M. C. Lemme, L.-M. Peng, X. Duan, Z. Chen, J. Appenzeller, S. J. Koester, E. Pop, A. D. Franklin, and C. A. Richter, “How to report and benchmark emerging field-effect transistors,” *Nature Electron.*, vol. 5, no. 7, pp. 416–423, Jul. 2022, doi: 10.1038/s41928-022-00798-8.