nanoBench: A Low-Overhead Tool for Running Microbenchmarks on x86 Systems

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Abstract—We present nanoBench, a tool for evaluating small microbenchmarks using hardware performance counters on Intel and AMD x86 systems. Most existing tools and libraries are intended to either benchmark entire programs, or program segments in the context of their execution within a larger program. In contrast, nanoBench is specifically designed to evaluate small, isolated pieces of code. Such code is common in microbenchmark-based hardware analysis techniques.

Unlike previous tools, nanoBench can execute microbenchmarks directly in kernel space. This allows to benchmark privileged instructions, and it enables more accurate measurements. The reading of the performance counters is implemented with isolated pieces of code. Such code is common in microbenchmark-based hardware analysis techniques.

We illustrate the utility of nanoBench at the hand of two case studies. First, we briefly discuss how nanoBench has been used to determine the latency, throughput, and port usage of more than 12,000 instruction variants on recent x86 processors. Second, we show how to generate microbenchmarks to precisely characterize the cache architectures of ten Intel Core microarchitectures. This includes the most comprehensive analysis of the employed cache replacement policies to date.

I. INTRODUCTION

Benchmarking small pieces of code using hardware performance counters is often useful for analyzing the performance of software on a specific microprocessor, as well as for analyzing performance characteristics of the microprocessor itself.

Such microbenchmarks can, for example, be helpful in identifying bottlenecks in loop kernels. To this end, modern x86 processors provide many performance events that can be measured, such as cache and TLB hits/misses in different levels of the memory hierarchy, the pressure on execution ports, mispredicted branches, etc.

Low-level aspects of microarchitectures are typically only poorly documented. Thus, the only way to obtain detailed information is often through microbenchmarks using hardware performance counters. This includes, for example, the latency, throughput, and port usage of individual instructions [1][2][3][4][5]. Microbenchmarks have also been used to infer properties of the memory hierarchy [6][7][8][9][10][11][12][13][14][15][16][17][18]. In addition to that, such benchmarks have been used to identify microarchitectural properties that can lead to security issues, such as Spectre [19][19] and Meltdown [20].

Often, such microbenchmarks consist of two parts: The main part, and an initialization phase that, for example, sets registers or memory locations to specific values or tries to establish a specific microarchitectural state, for example by flushing the caches. Ideally, the performance counters should only be active during the main part.

To facilitate the use of hardware performance counters, a number of tools and libraries have been proposed. Most of the existing tools fall into one of two categories. First, there are tools that benchmark entire programs, such as perf [21], or profilers like Intel’s VTune Amplifier [22]. Tools in the second category are intended to benchmark program segments that are executed in the context of a larger program. They usually provide functions to start and stop the performance counters that can be called before and after the code segment of interest. Such tools are, for example, PAPI [23], and libpfc [24].

Tools from both categories are not particularly well suited for microbenchmarks of the kind described above. For tools from the first category, one obvious reason is that it is not possible to measure only parts of the code. Another reason is overhead. Just running a C program with an empty main function, compiled with a recent version of gcc, leads to the execution of more than 500,000 instructions and about 100,000 branches. Moreover, this number varies significantly from one run to another.

Overhead can also be a concern for tools from the second category. In PAPI, for example, the calls to start and stop the counters involve several memory accesses, branches, and for some counters even expensive system calls. This leads to unpredictable execution times and might, e.g., destroy the cache state that was established in the initialization part of the microbenchmark. Moreover, these calls will modify general-purpose registers, so it is not possible to set the registers to specific values in the initialization part, and use these values in the main part.

For several reasons, microbenchmarks often need to be run multiple times. One reason is the possibility of interference due to interrupts, preemptions or contention on shared resources that are also used by programs on other cores. Another reason are issues such as cold caches that impact the performance on the first runs. A third reason is that there are more performance events than there are programmable counters, so the measurements may need to be repeated with different
counter configurations. Also, the code to be benchmarked itself often needs to be repeated several times. This is typically done by executing it in a loop or by unrolling it multiple times, or by a combination of both. All of this leads to a significant engineering effort that needs to be repeated over and over again.

In this paper, we present *nanoBench*, an open-source tool that was developed to make it very easy to execute microbenchmarks consisting of small, independent pieces of machine code on recent x86 CPUs. *nanoBench* is available on GitHub\(^1\).

There are two variants of the tool: A user-space implementation and a kernel-space version. The kernel-space version makes it possible to directly benchmark privileged instructions, in contrast to any previous tool we are aware of. Furthermore, it allows for more accurate measurements than existing tools by disabling interrupts and preemptions. The tool is precise enough to measure, e.g., whether individual memory accesses result in cache hits or misses.

Microbenchmarks may use and modify any general-purpose and vector registers, including the stack pointer. After executing the microbenchmark, *nanoBench* automatically resets them to their previous values. The loop and unroll counts, as well as the number of repetitions and the aggregate function to be applied to the measurement results, can be specified via parameters.

To demonstrate the usefulness of our tool, we present two case studies.

First, we discuss how *nanoBench* can be used to characterize the latency, the throughput, and the port usage of more than 12,000 instruction variants on recent x86 microarchitectures.

For the second case study, we develop a set of tools that generate microbenchmarks for analyzing caches. These microbenchmarks are then evaluated using *nanoBench*. We focus, in particular, on cache replacement policies, which are typically undocumented. We apply our tools to ten different Intel microarchitectures, and provide detailed models of their replacement policies, including several previously undocumented variants.

II. BACKGROUND

Recent Intel and AMD processors are equipped with different types of performance counters. All of these counters can be read using the *RDMSR*\(^2\) instruction; many of them can also be read using the *RDPMC*\(^3\) instruction. The *RDMSR* instruction is a privileged instruction, and can thus only be used in kernel space. The *RDPMC* instruction, on the other hand, is faster than the *RDMSR* instruction, and it can be directly accessed in user space if a specific flag in a control register is set.

A. Core Performance Counters

Each logical core has a private performance monitoring unit with multiple performance counters.

\(^1\)https://github.com/andreas-abel/nanoBench

\(^2\)“Read from model specific register”.

\(^3\)“Read performance-monitoring counters”.

B. Uncore/L3 Performance Counters

In addition to the per-core performance counters described above, recent processors also have a number of global performance counters that can, in particular, count events related to the shared L3 caches. On Intel CPUs, these counters can only be read in kernel space.

Algorithm 1: Generated Code for a Microbenchmark

```
1 Function generatedCode()
2 saveRegs
3 codeInit
4 ml ← readPerfCtrs // stores results in
5 // memory, does not modify registers
6 for j ← 0 to loopCount do // this line is
7 code // copy #1
8 code // copy #2
9 // omitted if loopCount=0
10 : 
11 code // copy #localUnrollCount
12 m2 ← readPerfCts
13 restoreRegs
14 r ← (m2-ml)/(max(1,loopCount)*localUnrollCount)
15 return r
```

III. nanoBench Features

In this section, we will first give a high-level overview by looking at a simple example that shows how *nanoBench* can be used. We will then describe various features of *nanoBench* in more detail.
Algorithm 2: Running a Microbenchmark

\[\begin{align*}
1 & \text{Function run}(\text{code}) \\
2 & \text{for } i \leftarrow -\text{warm\_up\_count} \text{ to } n\text{Measurements} \text{ do} \\
3 & \hspace{1em} m \leftarrow \text{code()} \\
4 & \hspace{1em} \text{if } i \geq 0 \text{ then } \text{// ignore warm-up runs} \\
5 & \hspace{2em} \text{measurements}[i] \leftarrow m \\
6 & \text{// apply aggregate function} \\
7 & \text{return } \text{agg(measurements)}
\end{align*}\]

A. Example

The following example shows how \textit{nanoBench} can be used to measure the latency of the L1 data cache on a Skylake-based system.

```
./nanoBench.sh -asm "mov R14, [R14]" 
                   -asm_init "mov [R14], R14" 
                   -config cfg_Skylake.txt
```

The tool will first execute the instruction \texttt{mov [R14], R14}, which copies the value of register R14 to the memory location that R14 points to. \textit{nanoBench} always initializes R14 (and a number of other registers) to point into a dedicated memory area that can be freely modified by microbenchmarks; this is described in more detail in Section III-C.

\textit{nanoBench} then starts the performance counters, and executes the instruction \texttt{mov R14, [R14]} multiple times. The number of repetitions can be controlled via parameters; for more information see Section III-F. The instruction loads the value at the address in R14 into R14. Thus, the execution time of this instruction corresponds to the L1 data cache latency. Afterwards, \textit{nanoBench} stops the performance counters.

The entire benchmark is then repeated multiple times to obtain stable results.

The output of \textit{nanoBench} will be similar to the following:

Instructions retired: 1.00
Core cycles: 4.00
Reference cycles: 3.52
UOPS_ISSUED.ANY: 1.00
UOPS_DISPATCHED_PORT.PORT_0: 0.00
UOPS_DISPATCHED_PORT.PORT_1: 0.00
UOPS_DISPATCHED_PORT.PORT_2: 0.50
UOPS_DISPATCHED_PORT.PORT_3: 0.50
MEM_LOAD_RETIRED.L1_HIT: 1.00
MEM_LOAD_RETIRED.L1_MISS: 0.00

The first three lines show the result of the fixed-function performance counters. The remaining lines correspond to the performance events specified in the \texttt{cfg_Skylake.txt} configuration file that was supplied as a parameter in the \textit{nanoBench} call shown above; details on the configuration file are described in Section III-C.

From the results, we can conclude that the L1 data cache latency is 4 cycles. This agrees with the documentation in Intel’s optimization manual \cite{IntelManual}.

B. Generated Code

To execute a microbenchmark, \textit{nanoBench} first generates code for a function similar to the pseudocode shown in Algorithm 1. In line 2, the generated code first saves the current values of the registers to the memory, and initializes certain registers to point to specific memory locations (see Section III-G). Then, the initialization part of the microbenchmark is executed (line 3). In the next line (line 4), the performance counters are read. Unless the noMem option (see Section III-I) is used, this step does not modify the values in any general-purpose or vector registers that were set by the initialization code (technically, it does modify certain registers temporarily, but it resets them to their previous value before the next line is executed). Lines 5 to 9 contain the code for the main part of the microbenchmark. The code is unrolled multiple times (this can be configured via a parameter, see Section III-F). If the parameter \texttt{loopCount} is larger than 0, the code for a for-loop is inserted in line 5. In this case, the code of the microbenchmark must not modify register R15, which is used to store the loop counter. Afterwards, the performance counters are read a second time (line 10), and in line 11 the registers are restored to the values that were saved in line 2. Finally, the difference between the two performance counter values, divided by the number of repetitions, is returned.

C. Running the Generated Code

Algorithm 2 shows how the generated code is run. The code is run a configurable number of times. At the end, an aggregate function is applied to the measurement results, which can be either the minimum, the median, or the arithmetic mean (excluding the top and bottom 20% of the values). A configurable number of runs in the beginning can be excluded from the result; this is described in more detail in Section III-H.

By default, \textit{nanoBench} generates and runs two versions of the code: the first one with \texttt{localUnrollCount} set to the specified \texttt{unrollCount}, and the second time with \texttt{localUnrollCount} set to two times the the specified \texttt{unrollCount}. The reported result is the difference between the two runs. This removes the overhead of the measurement instructions from the result, as well as anomalies that might be caused by the serialization instructions that are needed before and after reading the performance counters (see also Section IV-A1).

\textit{nanoBench} also provides an option that uses a \texttt{localUnrollCount} of 0 for one of the runs instead (i.e., there are no instructions between line 9 and line 10 in this case).

D. Kernel/User Mode

\textit{nanoBench} is available in two versions: A user-space and a kernel-space version.

The kernel-space version has several advantages over the user-space version:

- It makes it possible to benchmark privileged instructions.
- It can allow for more accurate measurement results as it disables interrupts and preemptions during measurements.
It can use several performance counters that are not accessible from user space, like the uncore counters on Intel CPUs, or the APERF and MPERF counters on AMD.

It can allocate physically-contiguous memory. See also Section III-C.

On the other hand, executing microbenchmarks in kernel space can lead to potential data loss and security problems, if the microbenchmarks contain bugs. It is thus recommended to use the kernel-space version only on dedicated test machines.

**E. Interface**

We provide a unified interface to the user-space and the kernel-space version in the form of two shell scripts, nanoBench.sh and kernel-nanoBench.sh, that have mostly the same command-line options.

In addition to that, we also provide a Python interface for the kernel-space version. This interface is used for the case studies in Sections VI and VII.

With all interfaces, the code of the microbenchmarks can be specified either as an assembler code sequence in Intel syntax (like in the example in Section III-A), or by the name of a binary file containing x86 machine code.

**F. Loops vs Unrolling**

For microbenchmarks that have code that needs be repeated several times to obtain meaningful results, there is a trade-off between unrolling the code (i.e., creating multiple copies of it), and executing the code in a loop.

Using a loop has the advantage of keeping the code size small, so that it will fit into the cache. On the other hand, the loop introduces an additional overhead, which can be significant if the body of the loop is small.

Whether unrolling or a loop should be used, depends on the particular benchmark. For benchmarks that measure, e.g., the number of data cache misses, a loop is the better choice, as it does not introduce any overhead in terms of memory accesses. On the other, for a benchmark that measures the port usage of an instruction, using only unrolling is better, as otherwise, the pops of the loop code compete for ports with the pops of the benchmark.

For some benchmarks, a combination of both a loop and unrolling yields the best results.

nanoBench provides two parameters, loopCount and unroll-Count, that control the number of loop iterations, and how often the code is unrolled.

**G. Accessing Memory**

nanoBench initializes the registers RSP (i.e., the stack pointer), RBP (i.e., the base pointer), RDI, RSI, and R14 to point into dedicated memory areas (of 1 MB each) that can be freely modified by the microbenchmarks.

Furthermore, for microbenchmarks needing a larger memory area, like benchmarks for determining cache parameters, the kernel-version of nanoBench provides an option for reserving a physically-contiguous memory area of a specific size that register R14 points to (see also Section IV-D).

**H. Warm-up Runs**

nanoBench provides the option of performing a configurable number of initial benchmark runs that are excluded from the results. This can, for example, be useful to make sure that the code and other accessed memory locations are in the cache. It can also be used to train the branch predictor to reduce the number of mispredicted branches. Furthermore, there are some instructions that require a warm-up period after having not been used for a while before they can execute at full speed again, like AVX2 instructions on some microarchitectures.

**I. noMem Mode**

By default, the code to read the performance counters writes the results to the memory. After a warm-up run, this memory location is usually in the cache, and thus, the time for these memory operations is constant.

However, for microbenchmarks that contain many memory accesses to different addresses that map to the same cache set, writing the performance counter results to the memory can be problematic. One reason for this is that the memory accesses in line 4 may change a cache state that was established by the initialization part of the benchmark. Another reason is that the microbenchmark code may evict the block that stores the performance counter results, which would lead to additional cache misses.

To avoid these problems, nanoBench has a special mode that stores all performance counter measurements in registers instead of in memory. If this mode is used, certain general-purpose registers must not be modified by the microbenchmark.

Moreover, if this mode is used, nanoBench also provides a feature to temporarily pause performance counting. This feature can be used by including special magic byte sequences in the microbenchmark code for stopping and resuming the performance counters. Using this feature incurs a certain timing overhead, so it is in particular useful for benchmarks that do not measure the time but, e.g., the number of cache hits or misses.

**J. Performance Counter Configurations**

The performance events to be measured are specified in a configuration file. The file uses a simple syntax to define the events. Unlike in some previous tools, like libpfc [24], the events are not hard-coded, which makes it easy to adapt nanoBench to future CPUs, as only a new configuration file has to be created.

If the configuration file contains more events than there are programmable performance counters, the benchmarks are automatically executed multiple times with different counter configurations.

We provide configuration files with all events for all recent Intel microarchitectures, and the AMD Zen microarchitecture.

**K. Execution Time of NanoBench**

Evaluating microbenchmarks with nanoBench is very fast. As an example, we consider a benchmark consisting of a
single NOP instruction, that is run with unrollCount = 100, loopCount = 0, nMeasurements = 10, and a configuration file with four events. On an Intel Core i7-8700K, running nanoBench with these parameters takes about 15 ms for the kernel version (assuming that the kernel module is already loaded), and about 50 ms for the user-space version.

L. Supported Platforms

We have successfully used nanoBench on processors from the 1st to the 10th generation of Intel’s Core microarchitecture, and with AMD Ryzen CPUs. All experiments were performed under Ubuntu 18.04, but nanoBench should be compatible with any Linux distribution that uses a recent kernel version.

IV. nanoBench IMPLEMENTATION

In this section, we describe several aspects of our implementation.

A. Accurate Performance Counter Measurements

1) Serializing Instruction Execution: As described in Section II, performance counters can be read with the RDPMC, or the RDMSR instruction. These instructions are not serializing instructions. Thus, due to out-of-order execution, they may be reordered with earlier or later instructions by the processor. For obtaining meaningful measurement results, it is therefore important to add instructions that serialize the instruction stream both before and after any instructions that read performance counters.

Previous approaches (e.g., [26]) often use the CPUID instruction for that purpose. However, for benchmarking short code segments, this is problematic. One reason for this is that the CPUID instruction has a variable latency and µop count. Paoloni [27] observed that the execution time of the CPUID can differ by hundreds of cycles from run to run. The variable µop count can be eliminated by setting the register RAX to a fixed value before each execution of the CPUID instruction; this also reduces the variance in the execution time, but does not fully eliminate it. Moreover, for an instruction sequence of the form A; CPUID; B, the serialization property of the CPUID instruction only guarantees that all µops of A have completed before B is fetched and executed. It does not guarantee that all µops of A have completed before the first µop of the CPUID is executed, and it does also not guarantee that all µops of the CPUID have completed before the first µop of B is executed.

We propose to use the LFENCE instruction instead. This instruction is not fully serializing: it does not guarantee that earlier stores have become globally visible, and subsequent instructions may be fetched from memory before LFENCE completes. However, on Intel CPUs it does guarantee that “LFENCE does not execute until all prior instructions have completed locally, and no later instruction begins execution until LFENCE completes.” [28]. For our purposes, this is sufficient, and the guarantee is even somewhat stronger than that for the CPUID instruction, as it also orders the LFENCE instruction itself with respect to the preceding and succeeding instructions. On AMD CPUs, the LFENCE provides similar guarantees if Spectre mitigations are enabled.

Using the LFENCE instruction for measurements of short durations was also recently recommended by McCalpin [29].

2) Reducing Interference: In the kernel-space version, we disable preemptions and hard interrupts during measurements, as they can perturb the measurement results [30][31]. This is not possible for the user-space version; however, we do pin the process to a specific CPU in this case to avoid the cost of process switches between CPUs.

Furthermore, for obtaining unperturbed measurement results, we recommend disabling hyperthreading. When using performance counters for resources shared by multiple cores, such as L3 caches, we furthermore recommend disabling all cores that share these resources. We provide shell scripts for this in our repository.

For microbenchmarks that measure properties of caches, such as the benchmarks described in Section VI, it can be helpful to disable cache prefetching. On Intel CPUs, this can be achieved by setting specific bits in a model-specific register (MSR). Details on how to do this are available in the documentation of nanoBench.

B. Generating Code

As described in Section III, nanoBench runs microbenchmarks by generating a function that contains the code of the microbenchmark, as well as setup and measurement instructions. This is implemented by first allocating a large enough memory area, and marking it as executable. Then, the corresponding machine code is written to this memory area, including unrollCount many copies of the code of the microbenchmark. If this code contains the magic byte sequences for pausing performance counting as described in Section III-I they are replaced by corresponding machine code for reading performance counters.

Generating the code for executing the microbenchmarks at runtime in this way makes it possible to access the performance counters without having to execute any function calls or branches.

C. Kernel Module

The kernel-space version of nanoBench is implemented as a kernel module. While the module is loaded, it provides a set of virtual files that are used to configure and run microbenchmarks. For example, setting the loop count, or the code of microbenchmark is done by writing the corresponding values to specific files under /sys/nb/. Reading the file /proc/nanoBench generates the code for running the benchmark (as described in Section IV-B), runs the benchmark (possibly multiple times, depending on the configuration), and returns the result of the benchmark.

Note that it is usually not necessary to access these virtual files directly, as we provide convenient interfaces that perform these accesses automatically (see Section III-E).
D. Allocating Physically-Contiguous Memory

In Linux kernel code, the kmalloc function can be used to allocate physically-contiguous memory. With recent kernel versions, this is limited to at most 4 MB.

Some of the microbenchmarks for determining properties of the L3 caches that we describe in Section VI require larger memory areas. We are not aware of a way to directly allocate larger physically-contiguous memory areas. However, we noticed that in many cases, subsequent calls to kmalloc yield adjacent memory areas. This is, in particular, the case if the system was rebooted recently. Moreover, the corresponding virtual addresses are also adjacent.

Based on this observation, we implemented a greedy algorithm that tries to find a physically-contiguous memory area of the requested size by performing multiple calls to kmalloc. If this does not succeed, the tool proposes a reboot. Note that allocating memory is only necessary once when the kernel module is loaded, and not before each microbenchmark run.

V. Case Study I: Instruction Latencies, Throughputs, and Port Usages

We developed an approach to automatically generate assembler code for microbenchmarks that measure the latencies, throughputs, and port usages of x86 instructions on different Intel microarchitectures, which are often undocumented. For the latency, our approach considers dependencies between different pairs of input and output operands; we take into account explicit and implicit dependencies, such as, e.g., dependencies on status flags.

The generated microbenchmarks are then evaluated using nanoBench. Of particular use is nanoBench’s ability to benchmark privileged instructions, the ability to unroll the code multiple times, and the support for microbenchmarks to have an initialization sequence that is not part of the performance measurement. Such an initialization sequence is often needed to, e.g., set registers or memory locations to specific values, for example, valid floating numbers if the microbenchmark uses floating point instructions.

More details on our approach have been published in [1]. We have since extended our tool to also support AVX-512 instructions; with this extension, the tool is now able to automatically obtain latency, throughput, and port usage data for more than 12,000 instruction variants. We have applied the tool to additional microarchitectures, including Intel’s Cannon Lake and Ice Lake microarchitectures, and AMD’s Zen+ and Zen 2 microarchitectures. Our results are available on www.uops.info both in the form of a human-readable, interactive HTML table, and as a machine-readable XML file.

VI. Case Study II: Caches

For our second case study, we develop a set of tools that generate microbenchmarks for analyzing caches. We focus, in particular, on cache replacement policies, which are typically undocumented for recent microarchitectures.

A. Background on Cache Organization

To profit from spatial locality and to reduce management overhead, main memory is logically partitioned into a set of memory blocks of a specific size (typically 64 Bytes). Blocks are cached as a whole in cache lines of the same size. Usually, the block size is a power of two. This way, the block number is determined by the most significant bits of a memory address.

When accessing a memory block, the cache logic has to determine whether the block is stored in the cache (“cache hit”) or not (“cache miss”). To enable an efficient lookup, each block can only be stored in a small number of cache lines. For this purpose, caches are partitioned into \( N \) equally-sized cache sets. The size of a cache set is called the associativity \( A \) of the cache. A cache with associativity \( A \) is often called \( A \)-way set-associative. It consists of \( A \) ways, each of which consists of one cache line in each cache set. Usually, also the number of cache sets \( N \) is a power of two such that the set number, also called index, is determined by the least significant bits of the block number.

In Intel microarchitectures, starting with Sandy Bridge, the last-level cache is divided into multiple slices. Each of the slices is organized as described above. The slices are managed by so called C-Boxes, which provide the interface between the core and the last-level cache, and which are responsible for maintaining cache coherence. Usually, there is one C-Box per physical core. The first microarchitectures that used sliced L3 caches (Sandy Bridge, Ivy Bridge, Haswell) had one slice per C-Box [32,33,34,35,36,37,38]. Skylake and more recent microarchitectures can have multiple slices per C-Box [39,40]. Each C-Box has several performance counters that can, e.g., count the number of lookup events for the corresponding part of the last-level cache. These counters belong to the class of uncore performance counters (see Section II-B).

An undocumented hash function is used for mapping physical addresses to cache slices. Several paper have reverse-engineered this hash function for Sandy Bridge, Ivy Bridge, and Haswell CPUs [32,33,35,36,37,38].

B. Background on Replacement Policies

Since the number of memory blocks that map to a set is usually far greater than the associativity of the cache, a replacement policy must decide which memory block to replace upon a cache miss.

1) Permutation-based policies: Many commonly used policies can be modeled as so called permutation policies. These policies have in common that they

1) maintain a total order of the elements in the cache
2) upon a cache hit, the order is updated; the new order only depends on the position of the accessed element in the order
3) upon a cache miss, the smallest element in the order is replaced.

Permutation policies can thus be fully specified by \( A+1 \) many permutations (one for each position in which a hit can occur, and one permutation for a miss).
Among the policies that can be modeled as permutation policies are, for example, FIFO, LRU, and tree-based pseudo-LRU (PLRU). PLRU is an approximation to LRU that maintains a probability distribution to denote a policy that inserts new blocks with age 0 in the cache where a block is inserted upon a miss. Upon a cache miss, the element that the tree bits currently point to is replaced. After each access to an element, all the bits on the path from the root of the tree to the leaf that corresponds to the accessed element are set to point away from this path.

Permutation policies were introduced by [15], along with an efficient algorithm for inferring them automatically.

2) MRU/QLRU: However, not all popular policies can be modeled as permutation policies. One example is the MRU policy [41]. This policy stores one status bit for each cache line. Upon an access to a line, the corresponding bit is set to zero; if it was the last bit that was set to one before, the block for all other lines are set to one. Upon a cache miss, the leftmost element whose bit is set to one gets replaced. This policy is sometimes also called bit-PLRU [42], PLRUm [43], or not-recently-used (NRU) [44].

A generalization of this policy that uses two status bits per cache line is called Quad-Age LRU (QLRU) [45, 46], or “2-bit Re-reference Interval Prediction” (RRIP) [44]. The two bits are supposed to represent the age of a block.

During our experiments, we found out that some recent Intel CPUs use variants of this policy that were not described in the literature so far. In particular, the variants differ from each other in the hit promotion policy, in the insertion age, in the location in the cache where a block is inserted upon a miss, in how the bits are updated if there is no more block with age 3, and in whether this update occurs only on a miss, or also on a hit. In the following, we will describe these parameters in detail, and we propose a naming scheme for referring to the different variants.

The hit promotion policy describes how the age of a block is updated upon a hit. We assume that the age is always reduced, unless it is already 0. Thus, the hit promotion policy can be modeled by one of the following functions. Let \( x \in \{0, 1, 2\} \), and \( y \in \{0, 1\} \).

\[
H_{xy}(a) := \begin{cases} 
  x, & \text{if } a = 3 \\
  y, & \text{if } a = 2 \\
  0, & \text{otherwise}
\end{cases}
\]

The insertion age is the age that will be assigned to a block upon a miss. For \( x \in \{0, 1, 2, 3\} \), we will use \( Mx \) to denote that the insertion age is \( x \). Furthermore, we will use \( MR_{px} \) to denote a policy that inserts new blocks with age \( x \) with probability \( \frac{p}{2} \), and with age 3 otherwise. Note that the insertion age might be different if blocks are brought into the cache by prefetching. We currently do not consider this scenario.

We consider the following three variants as to where a block will be inserted upon a miss.

- **R0:** If the cache is not yet full (after executing the WBINVD instruction), insert the new block in the leftmost empty location. Otherwise, replace the block in the leftmost location whose status bits are 3. If there is no such block, the behavior is undefined.
- **R1:** Like R0, but if there is no location whose status bits are 3, always replace the leftmost block, independently of its status bits.
- **R2:** Like R0, but insert blocks in the rightmost empty location if the cache is not yet full.

If after an access, there is no more block whose age is 3, the status bits of potentially all blocks will be updated. Let \( i \) denote the location of the block that was accessed. Let \( age(b) \) be the current age of block \( b \), and \( age'(b) \) the new age (after the update). Let \( M \) be the maximum (current) age of any block.

We consider the following variants for \( age' \):

- **U0:** \( age'(b) := age(b) + (3 - M) \)
- **U1:** \( age'(b) := \begin{cases} 
  age(b), & \text{if } b = i \\
  age(b) + (3 - M), & \text{otherwise}
\end{cases} \)
- **U2:** \( age'(b) := age(b) + 1 \)
- **U3:** \( age'(b) := \begin{cases} 
  age(b), & \text{if } b = i \\
  age(b) + 1, & \text{otherwise}
\end{cases} \)

We will use a name of the form \( QLRU_{H11\_M1\_R1\_U2} \) to refer to the corresponding variant.

Some variants do not check after each access whether there is still a block with age 3, as described above, but only upon a miss, before selecting the block to replace. We will refer to such variants by adding the suffix \( \text{UMO} \) (“update on miss only”) to the name.

Note that not all combinations are possible. For example, R0 cannot be combined with U2 or U3, as it always requires at least one block with age 3. Also, some combinations are observationally equivalent; this is, e.g., the case for R0 and R1 in combination with U0.

The 2-bit RRIP-HP policy proposed by [43] would be named \( QLRU_{H00\_M2\_R0\_U0\_UMO} \) according to our naming scheme. The corresponding “bimodal RRIP” (BR-RRIP) policy from the same paper would be named \( QLRU_{H00\_MRp2\_R0\_U0\_UMO} \).

3) Adaptive Policies: Some caches use adaptive replacement policies that can dynamically switch between two different policies. This can be implemented via set dueling [44, 47, 58]: A number of sets are dedicated to each policy, and the remaining sets are follower sets that use the policy that is currently performing better.

C. Cache-Characterization Tools

Based on nanoBench, we have developed a set of tools for analyzing undocumented properties of caches.

The first tool, cacheSeq, can be used to measure how many cache hits and misses executing an access sequence (i.e., a sequence of blocks that map to the same cache set) generates. To this end, cacheSeq automatically generates a suitable microbenchmark that is then evaluated using the kernel-space version of nanoBench.

For each element of the access sequence, it is possible to specify whether the corresponding access should be included in the measurement results. This is implemented using the
feature described in Section III-I that makes it possible to temporarily pause performance counting. Via a parameter, it is possible to specify whether the access sequence should be executed in a specific set, in a list of sets, in a range of sets, or in all sets. Furthermore, for L3 caches, a specific C-Box can be selected. Between every two accesses to the same set in a lower-level cache, cacheSeq automatically adds a sufficient number of accesses to the higher-level caches (that map to different sets and/or slices in the lower-level cache) to make sure that the corresponding lines are evicted from the higher-level cache and the access actually reaches the lower-level cache. These additional accesses are excluded from the performance counter measurements. The tool also provides an option to execute the WBINVD instruction at the start of each access sequence, which flushes all caches. This instruction is a privileged instruction.

The following tools are all based on cacheSeq.

1) Replacement policies: We implemented two tools for automatically determining replacement policies. The first tool implements the algorithm proposed in [15] for inferring permutation policies.

The second tool generates random access sequences, and compares the number of hits obtained by executing them with cacheSeq with the number of hits in a simulation of different replacement policies, including common policies like LRU, PLRU, and FIFO, as well as all meaningful QLRU variants, as introduced in Section VI-B2. If there is only one policy that agrees with all measurement results, the tool concludes that this is the likely policy actually used.

2) Age Graphs: This tool generates a graph showing the “ages” of all blocks of an access sequence. This graph is obtained as follows. For each block B of an access sequence, we first execute the access sequence, then we access n fresh blocks, and finally we measure the number of hits when accessing B again. An example of such a graph can be seen in Figure VI-D.

These graphs are, in particular, useful for analyzing caches with policies that are non-deterministic, and thus cannot be inferred with the tools described above.

3) Tests for Set Dueling: To find the sets with a fixed policy in caches that use set dueling, we implemented an approach similar to [48]. However, unlike their approach, our tool also supports caches in which the fixed sets are not the same in all C-Boxes.

D. Results

We have applied our tools for determining the replacement policies to the CPUs shown in Table II which includes CPUs from the 1st to the 8th generation of Intel’s Core microarchitecture. We did not consider recent AMD CPUs for this case study, as we could not find a way to disable their cache prefetchers, which is required for our cache microbenchmarks (see also Section IV-A2).

The L1 data caches of all CPUs we considered use the PLRU replacement policy. This policy is also used by the

L2 caches of CPUs from the first five generations. The more recent generations use two variants of QLRU replacement. For the Nehalem microarchitecture (1st generation), these results agree with the results reported in [49]. We are not aware of any public description of the L1 and L2 policies for more recent microarchitectures.

The Nehalem and Westmere CPUs use the MRU replacement policy in their L3 caches. This was also reported by [49]. The Sandy Bridge CPU uses a variant of this policy that sets all bits to one if the cache is not yet full (after executing the WBINVD instruction).

The more recent generations use different variants of QLRU replacement.

Of particular interest are the CPUs from the 3rd to the 5th generation (Ivy Bridge, Haswell, and Broadwell), as they use an adaptive policy.

For the Ivy Bridge machine, we found that the sets 512-575, and the sets 768-831 (in all slices) use a fixed policy, whereas the other sets are follower sets. This agrees with Wong [48]. However, Wong was not able to measure which two policies are actually used. According to our results, the sets 512-575 use the QLRU_H11_M1_R1_U2 policy. The policy used by the sets 768-831 appears to be non-deterministic. Figure VI-D shows an age graph for the access sequence “<WBINVD>B0 B1 … B11” (note that the associativity of the the cache is 12). We can see that the curves for B_i and B_{i+1} (i > 0) are similar, but shifted by about 16. Furthermore, for B_0, about \frac{15}{16} of the blocks are evicted immediately when the first fresh block is accessed, while the remaining \frac{1}{16} of the blocks remains in the cache relatively long. This suggests that the policy might be the QLRU_H11_MR16_R1_U2 policy, i.e., a variant of the policy used in sets 512-575 that inserts new blocks with age 1 in \frac{1}{16}th of the cases, and with age 3 otherwise.

The Haswell CPU uses the same sets as the Ivy Bridge CPU as dedicated sets, but only in slice 0. All other sets are follower sets. It uses the QLRU_H11_M1_R0_U0 policy in sets 512-575. The policy in sets 768-831 is likely the QLRU_H11_MR16_R0_U0 policy.

The Broadwell CPU uses the same two policies as the Haswell CPU. However, it uses the first policy in sets 512-
575 in slice 0, and 768-831 in slice 1, and the second policy in sets 512-575 in slice 1, and 768-831 in slice 0.

Our results for the Haswell, Broadwell, Skylake, and Kaby Lake microarchitectures disagree with the results reported by Briongos et al. [46]. The policies they describe would be the \texttt{QLRU}_H21\_M2\_R0\_U0\_UMO and \texttt{QLRU}_H21\_M3\_R0\_U0\_UMO variants according to our naming scheme. Our tool found several counterexamples for these policies. Briongos et al. also stated that the two policies did not agree with all of their observations; however, they assumed that “the errors were due to noise”.

Furthermore, according to Briongos et al., the dedicated sets on the Haswell CPU are distributed over different slices. As, according to the paper, they use an approach from [33], we assume that they also rely on a statement from that paper that “when the number of cores in the processor is a power of two, the set index bits are not used for determining the LLC slice.” This was shown to be incorrect in later work [45]. Thus, their observations rather seem to be an artifact of the hash function used for determining the cache slices.

Further details on all results are available on our website [www.uops.info].

VII. RELATED WORK

\texttt{Perf} [21] and Intel’s \texttt{VTune Amplifier} [22] are two examples of tools that are targeted at analyzing whole programs using hardware performance counters. Tools from this category can often display performance statistics at different levels of granularity, sometimes for individual source code lines. However, this data is usually obtained via sampling, and thus not precise. Such tools are commonly used for identifying the parts of a program that would most benefit from further optimizations.

\texttt{PAPI} [24] is a widely used tool for accessing performance counters. It provides C and Fortran interfaces that provide functions for configuring and reading performance counters. It can be used for measuring the performance of smaller code segments in the context of a larger program. However, reading the performance counters leads to multiple function calls, branches, and memory accesses. Therefore, it is not suitable for the class of microbenchmarks considered in this paper.

\texttt{LIKWID} [50] is a tool suite providing multiple performance analysis tools. It can both benchmark whole programs, as well as, similar to \texttt{PAPI}, specific code region of a larger program. Reading the performance counters requires expensive system calls [51].

\texttt{libpfc} [24] is a library that was designed in a way to make it possible to use performance counters with a very low overhead. It provides macros with inline assembler code for reading the performance counters. Thus, it does not require function calls or branches. Like our tool, it uses the \texttt{LFENCE} instruction to serialize the instruction stream. In fact, a very early version of our tool was based on \texttt{libpfc}. However, \texttt{libpfc} only supports Haswell CPUs, and it does not support accessing uncore performance counters.

Agner Fog [26] provides a framework for running microbenchmarks similar to the microbenchmarks considered in this paper. The code of the microbenchmark, which is not allowed to use all registers, must be inserted into specific places in a file provided by the framework. The overhead for reading performance counters is relatively small; it does not require function calls or branches. However, the tool uses the \texttt{CPUID} instruction for serialization, which can be problematic for short microbenchmarks, as described in Section [V-A1]. The tool only supports a relatively small number of performance events, and it only supports performance counters that can be read with the \texttt{RDPMC} instruction (i.e., it does not support uncore counters on Intel CPUs, or the APERF/MPERF counters).

None of the existing tools that we are aware of allows for executing benchmarks directly in kernel space.

VIII. CONCLUSIONS AND FUTURE WORK

We have presented a new tool that significantly reduces the engineering effort required for evaluating small microbenchmarks in an accurate and precise way.

To illustrate the usefulness of our tool, we have presented two different case studies. First, we showed how it can be used to characterize the latency, throughput, and port usage of x86 instructions. Then, we described microbenchmarks for analyzing cache properties. We applied these microbenchmarks to recent Intel CPUs, and uncovered several previously undocumented replacement policy variants.

There are two main directions for future work: The first direction is to adapt \texttt{nanoBench} to non-x86 architectures, such
as ARM. The second direction is to apply nanoBench to additional use cases. Besides the two examples we considered, many other properties of recent microarchitectures are undocumented. This includes, for example, details on how the TLBs or the branch predictors work. Knowledge of such details is important for optimizing software, and for showing the presence or absence of microarchitectural security problems.

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