Negative Capacitance as Digital and Analog Performance Booster for Complementary MOS Transistors

A. Saeidi,* F. Jazaeri, I. Stolichnov, Christian C. Enz, and Adrian M. Ionescu

Ecole Polytechnique Federale de Lausanne (EPFL), Lausanne, Switzerland

E-mail: ali.saeidi@epfl.ch

Abstract

Boltzmann tyranny poses a fundamental limit to lowering the energy dissipation of conventional MOS devices, a minimum increase of the gate voltage, i.e. 60 mV, is required for a 10-fold increase in drain-to-source current at 300 K. Negative Capacitance (NC) in ferroelectric materials is proposed in order to address this physical limitation of CMOS technology. A polarization destabilization in ferroelectrics causes an effective negative permittivity, resulting in a differential voltage amplification and a reduced subthreshold swing when integrated into the gate stack of a transistor. Recent demonstrations of negative capacitance concerned mainly n-type MOSFETs and their subthreshold slope. An effective technology booster should be capable of improving the performance of both n- and p-type transistors. In this work, we report a significant enhancement in both digital (subthreshold swing, on-current over off-current ratio, and overdrive) and analog (transconductance and current efficiency factor) FoM of commercial 28nm CMOS process by exploiting a PZT capacitor as the negative capacitance booster. Accordingly, a sub-thermal swing down to 10 mV/decade together with an enhanced current efficiency factor up to $10^5 \text{ V}^{-1}$ is obtained in both n- and p-type
MOSFETs at room temperature. The overdrive voltage is enhanced up to 0.45 V, leading to a supply voltage reduction of 50%.

Complementary Metal-Oxide-Semiconductor (CMOS) scaling will be eventually limited by the inability to remove the heat generated in the switching process. The origin of this issue can be traced back to the operation principle of the silicon CMOS devices governed by the non-scalability of thermal voltage (Boltzmann’s tyranny). This results in preventing these devices to achieve a sub-60 mV/decade subthreshold slope (SS) at room temperature. The SS of a MOSFET is obtained by

\[
SS = \frac{\partial V_g}{\partial (\log I_d)} = \frac{\partial V_g}{\partial \psi_s} \times \frac{\partial \psi_s}{\partial (\log I_d)},
\]

where \( \psi_s \) corresponds to the surface potential of the silicon channel. In a conventional MOSFET, the lower limit of the second term in RHS of (1) is \( (k_B T/q) \ln(10) \) and cannot be any lower than 60 mV/decade at 300 K. Since \( V_g \) is linked to \( \psi_s \) through a capacitive voltage divider, the first term that is known as the body factor, \( m \), is obtained as

\[
\frac{\partial V_g}{\partial \psi_s} = 1 + \frac{C_s}{C_{MOS}},
\]

exceeds one, thus limits the SS to 60 mV/decade at \( T=300 \) K. A sub-thermal swing can be achieved using the proposed negative capacitance (NC) of ferroelectric materials. Negative capacitance in ferroelectrics arises from the imperfect screening of the spontaneous polarization. Imperfect screening is intrinsic to semiconductor-ferroelectric and metal-ferroelectric interfaces due to their screening lengths. The physical separation of ferroelectric bound charges from the metallic screening charges creates a depolarizing field inside the ferroelectric and destabilizes the polarization. Hence, intentionally destabilizing this polarization
causes an effective NC that has been proposed as a way of overcoming the fundamental limitation on the power consumption of MOSFETs.\textsuperscript{[4-6]} The negative capacitance, originating from the dynamics of the stored energy in a phase transition of ferroelectric materials, results in an internal voltage amplification in an MOS device when integrated into the gate stack. The concept of NC can be understood by considering the free energy of ferroelectrics. A ferroelectric material is traditionally modeled using a double well energy landscape. The energy characteristic of a ferroelectric capacitor, depicted in Figure 1a, is calculated by
\[ U_{FE} = \alpha P^2 + \beta P^4 + \gamma P^6 + E_{ext}P, \]
where \( P \) is the polarization, \( E_{ext} \) is the externally applied electric field, and \( \alpha, \beta, \text{and} \gamma \) are material dependent parameters.\textsuperscript{[5]} In equilibrium, the ferroelectric resides in one of the wells, providing spontaneous polarization. The capacitance of a ferroelectric material can be determined by
\[ C_{FE} = \left[ \frac{d^2U_{FE}}{dQ_{FE}^2} \right]^{-1}, \quad (3) \]
which is positive at the wells considering the curvature of \( U_{FE} \) vs. \( Q_{FE} \) characteristic (Figure 1a). Nevertheless, the curvature is negative around the origin (\( Q_{FE} = 0 \)). More specifically, a ferroelectric material shows an effective NC while switching from one stable polarization state to the other one.\textsuperscript{[10]} It should be remarked that NC refers to negative differential capacitance due to the small signal concept of the capacitance and relation between \( C_{FE} \) and \( U_{FE} \) (equation 3). The NC has been proven elusive for ferroelectrics in isolation and cannot be observed in experiments, exhibiting hysteretic jumps in the polarization (Figure 1b). However, it has been confirmed that if the ferroelectric placed in-series with a positive capacitor of proper value, the NC segment can be stabilized.\textsuperscript{[11,12]} This NC region can be modeled by the state-of-the-art approach for modeling the dynamics of ferroelectric capacitors relying on Landau-Khalatnikov (LK) equation,
\[ \rho \frac{dP}{dt} + \nabla_p U_{FE} = 0. \]
Figure 1b compares the experimentally measured polarization vs. electric field of a PZT capacitor with the fitting result of the LK equation.
Figure 1: Free energy landscape and polarization characteristic of a ferroelectric. (a) Energy density function of a ferroelectric capacitor in equilibrium, showing an effective NC while switching from one stable polarization state to the other one. (b) Measured polarization vs. electric field for a PZT film (experimental) and the fitting results of LK equation (dashed curve).

A ferroelectric capacitor interconnecting with the gate stack of a MOS transistor creates a series connection between C_{FE} and C_{MOS} (Figure 2a). The ferroelectric capacitor can increase the total capacitance of the gate \((C_{total}^{-1} = C_{FE}^{-1} + C_{MOS}^{-1})\) while it is stabilized in the NC region.\[^{13,14}\] Specifically, the series structure brings an abrupt increase in the differential charge in the internal node \((V_{int})\) by changing the gate voltage, thus providing a step-up voltage transformer.\[^{15,16}\] The internal gain of NC can be defined as \(\beta = \partial V_{int}/\partial V_g = C_{FE}/(C_{FE} + C_{MOS})\). Accordingly, an NC booster can provide an internal voltage amplification \((\beta > 1)\) which results in a body factor reduction, i.e. \(1/\beta\), leading to the improvement of both analog and digital parameters of the transistor:

\[
SS = \left(\frac{\partial \log I_d}{\partial V_g}\right)^{-1} = \frac{\partial V_{int}}{\partial \log I_d} \times \frac{\partial V_g}{\partial V_{int}} = \frac{1}{\beta} \times SS_{ref}, \tag{4}
\]

\[
g_m = \frac{\partial I_d}{\partial V_g} = \frac{\partial I_d}{\partial V_{int}} \times \frac{\partial V_{int}}{\partial V_g} = \beta \times g_{m-ref}. \tag{5}
\]

In order for NC to occur, the charge line of the baseline transistor is acquired to have an intersection with the negative slope of the polarization.\[^{10}\] Otherwise, the device characteristic shows a hysteresis, corresponding to the coercive fields of the ferroelectric without performance boosting.\[^{17}\] Additionally, to bring about the maximum enhancement in the
Figure 2: Negative capacitance MOSFET and stability constraints. (a) Schematic diagram of the experimental configuration of an n-type NC-FET including the capacitance model of the structure. (b) Ferroelectric’s NC is unstable by itself (A), but it can be partially (B) or fully stabilized (C) by placing in-series with a positive capacitor. The NC region of ferroelectric energy landscape is shown inside the dotted rectangular box.

non-hysteretic operation of an NC-FET, the negative value of $C_{FE}$ should be well-matched with $C_{MOS}$ ($|C_{FE}| = C_{MOS}$ while $C_{total} > 0$ in the whole range of operation). Generally, considering that the SS can be expressed as $SS = (60mV/\text{decade} \times (1+C_{MOS}/C_{FE})$, the transistor transfer characteristic becomes steep as $|C_{FE}|$ gets close to $C_{MOS}$. However, a value of $|C_{FE}|$ too close to $C_{MOS}$ gives rise to the hysteretic behavior due to the instability of NC in the strong inversion regime. Additionally, both $C_{MOS}$ and $C_{FE}$ are voltage-dependent, making it extremely challenging to fully satisfy the matching condition. Therefore, the ferroelectric’s NC commonly partially gets stabilized, proposing a trade-off between the hysteretic behavior and the performance-boosting due to the NC effect (Figure 2b). With the validity of NC concept being experimentally established, it is now of paramount importance to understand the challenges involved in the design of NC-FETs, so that the steepness and hysteresis of the device characteristic can be optimized in both n- and p-type MOSFETs. In this respect, a polycrystalline PZT capacitor is fabricated for thoroughly understanding the negative capacitance concept. It is then connected to various commercial MOSFETs, fabricated in 28 nm CMOS technology node. The hysteretic behavior of both n- and p-type NC-FETs is tuned imposing the proposed matching condition. Afterward, the impact of NC on the performance of conventional MOSFETs is investigated by measuring and analyzing the internal node voltage. Sub-thermal swing down to 10 mV/decade is observed in n- and
p-type hysteretic NC-FETs. The paper reports and discusses the trade-off between the steepness of the subthreshold slope and the hysteresis, degrading the performance by reducing the hysteresis. The strong dependence of the NC effect on the source to drain electric field is also evidenced, reducing the impact by increasing the absolute value of $V_{ds}$. Moreover, it is experimentally validated that a poly-domain ferroelectric capacitor in steady states cannot have more than one stable NC domain at the time, showing a different polarization characteristic from the expected S-shape of a single-domain ferroelectric.

**Experimental results and discussion**

As schematically shown in Figure 2a, the experimental results are obtained by connecting an external PZT capacitor to the gate of a MOSFET. This external connection offers a flexibility of testing different series combinations and tuning the hysteretic behavior. High-performance commercial n- and p-type MOSFETs are employed as the baseline transistors. An MIM structure with 45nm of polycrystalline Pb(Zr$_{43}$,Ti$_{57}$)O$_3$ (PZT) is fabricated. High-quality epitaxial ferroelectric layers are commonly considered suitable for NC devices due to the formation of a mono-domain state characterized by a single coercive field. However, the typical behavior of poly-domain ferroelectrics can change dramatically by applying a repetitive voltage stress known as the training procedure of ferroelectrics. This behavior suggests that a poled ferroelectric layer can show a mono-domain like characteristic (see supplementary materials).

**n-type negative capacitance MOSFETs**

Figure 3a illustrates the input transfer characteristic of an n-type NC-FET where the gate of the baseline FET ($W = 200$ nm, $L = 1$ µm) is loaded with a PZT capacitor having an area of $30\times30$ µm$^2$. The gate voltage is swept from $-3$ V to $+3$ V and back to $-3$ V while the drain voltage is set to 0.1 V. It should be noted that the curves are plotted with respect to the
Figure 3: Hysteretic n-type NC-FET. (a) Transfer characteristic of the device shows a super steep transition of 10 mV/decade together with a hysteresis of 4.5 V ($V_{ds} = 100$ mV). (b) A remarkable amplification (defined as $dV_{int}/dV_{g}$) up to 20 V/V is achieved in the regions corresponding to the negative slope of the polarization (c). Extracted current efficiency factor of the device represents a significant boosting, up to $10^5$ V$^{-1}$, in the subthreshold region (d).
effective gate voltage \((V_{gs\_eff} = V_{gs} - V_{th})\), which makes the results to be directly comparable and removes the effect of the two different threshold voltages. With the aid of an internal electrode, a step-up conversion of the internal voltage is explicitly observed as a result of the ionic movement in PZT. In order to qualitatively determine the voltage gain, \(dV_{int}/dV_g\) vs. \(V_g\) is plotted, representing a significant amplification up to 20 V/V (Figure 3b). This internal voltage increase allows the surface potential to be higher than the gate voltage, leading to a body factor below 1. Therefore, an SS of 10 mV/decade is observed over six orders of magnitude of the drain current. Moreover, the overdrive voltage is improved by a value of 0.45 V. Using the internal electrode and imposing the displacement vector continuity, a negative slope of the polarization is extracted in a certain range of the polarization, corresponding to the subthreshold region where a significant boosting of performance is reached (Figure 3c). It should be noted that due to the charge balance conditions, only a small fraction of the polarization get switched. A remarkable enhancement of the current efficiency factor, \(g_m/I_d\), with a peak of \(10^5\) V\(^{-1}\) is demonstrated when the device is operating in the weak-inversion regime (Figure 3d). A significant improvement is achieved in both digital and analog FoM of the baseline MOSFET. The measured input transfer characteristic of the NC-FET shows a hysteresis of 4.5 V caused by the poor matching of the ferroelectric NC and MOS capacitance.

The undesirable hysteretic operation of NC-FETs can be alleviated with a better matching of the ferroelectric and MOS capacitances which ensures the \(C_{total} > 0\) stability condition in a wide range of the applied gate voltage. Considering \(C_{total}^{-1} = C_{FE}^{-1} + C_{ox}^{-1} + C_{si}^{-1}\), where \(C_{ox}\) and \(C_{si}\) correspond to the gate linear dielectric and silicon capacitances, the stability condition can be written as

\[
\left(\frac{S_{gate}}{S_{FE}}\right) < \frac{5\gamma}{4(3\beta^2 - 5\alpha\gamma)} \left(\frac{1}{d_{FE}}\right) \left[\frac{d_{ox}}{\epsilon_{SiO_2}} + \frac{d_{si}}{\epsilon_{si}}\right]. \tag{6}
\]

In equation (6), \(d, S, \) and \(\epsilon\) are the thickness, area, and the permittivity of the corre-
Figure 4: n-type NC-FET with a reduced hysteresis. (a) Performance of an n-type NC-FET with a small hysteresis of 150 mV and a swing below 30 mV/decade while $V_{ds}$ is set to 100 mV (b). A steep off-to-on transition is realized in both positive and negative going branches of the drain current. (c) Internal voltage measurement shows a voltage gain of up to 10 V/V. (d) The extracted P-E curve of the ferroelectric shows a clear S-shape in a wide range of operation with a negligible hysteresis. (e) $g_m/I_d$ is also boosted and reached a factor of 600 V$^{-1}$. 
sponding layer, respectively. Hence, in consideration of (6), another NC-FET with a different baseline FET (W = 100 nm, L = 1 µm) and a PZT capacitor of the same thickness and an area of 20×20 µm² with a better matching of capacitances and a smaller hysteresis is depicted in Figure 4a. A reduced hysteresis of 150 mV is demonstrated while the transistor is operating at a constant drain voltage i.e. 0.1 V. An SS below 30 mV/decade at 300 K is reliably achieved in both positive and negative going branches of the input transfer characteristic (see Figure 4b) where the transistor charge line and the negative slope of the ferroelectric polarization have an intersection. As a result of an average swing well below the thermal limit of MOSFETs, the effective gate voltage can be reduced by 50%, maintaining the same level of the output current. Figure 4c depicts the internal voltage and internal gain plots (V_{int} vs V_g and dV_{int}/dV_g vs V_g). Figure 4d depicts the extracted polarization characteristic of the series connected PZT capacitor, showing an effective NC similar to the ideal expectation of NC by LK equation. The current efficiency factor is also enhanced and reached a maximum value of about 600 V⁻¹ (Figure 4e).

**p-type negative capacitance MOSFETs**

The impact of the same NC booster on p-type commercial MOSFETs is also reported and discussed. The drain-to-source voltage was set at −0.9 V in all measurements performed in this part, otherwise mentioned. Figure 5 depicts the performance improvement that is obtained in a p-type NC-FET (W = 1 µm, L = 90 nm) using a PZT capacitor (40×40 µm²) as an NC booster. The gate voltage swept from +3 V to −3 V and returns back to the initial bias by reverse sweep. Using the NC booster, similar to n-type NC-FETs, the internal voltage is enhanced and reached values greater than the applied gate voltage, so that a steep off-to-on transition of 10 mV/decade is realized over at least 4 orders of magnitude of the drain current (Figure 5a). The NC condition is fulfilled in both forward and reverse sweeps so that a sub-thermal swing is demonstrated in both branches. Due to the poor matching of capacitances, a large hysteresis of 3.5 V is observed. Analyzing the internal electrode
voltage (Figure 5b) shows a considerable internal voltage amplification in the regions where the ferroelectric capacitor provides a clear S-shape negative slope of the polarization (Figure 5c). The $g_{m}/I_d$ FoM is also significantly enhanced, reaching a peak of $10^5 \, V^{-1}$ (Figure 5d).

Figure 5: Hysteretic p-type NC-FET. (a) Transfer characteristic of a p-type NC-FET with a large hysteresis of 3 V ($|V_{ds}| = 900$ mV) and a swing of 15 mV/dec over five decades of current. (b) An internal voltage gain greater than one is measured in both positive and negative going branches (c). Current efficiency factor is also enhanced, reaching a factor of $10^5 \, V^{-1}$.

In a different structure, a p-type NC-FET with a small hysteresis is presented (Figure 6a). A PZT capacitor with an area of $10 \times 10 \, \mu m^2$ is connected to the gate of a p-MOSFET ($W = 3 \, \mu m$, $L = 1 \, \mu m$). A reduced hysteresis of 200 mV is achieved due to the proper matching of capacitances, regarding equation (6). Figure 5b reports the SS vs. $V_g$ plot which is well below the thermal limit of MOSFETs (down to 20 mV/decade) at 300 K. The internal node measurement confirms a voltage gain greater than 1 while having a peak of 10 V/V (Figure 5c). The polarization vs. voltage plot of the PZT capacitor indicates a clear S-like
Figure 6: p-type NC-FET with a reduced hysteresis. (a) Input transfer characteristic of an NC-FET with a small hysteresis of 200 mV at $|V_{ds}| = 900$ mV. (b) A sub-thermal swing well below 60 mV/dec is obtained. (c) Measurement of the internal node shows a significant voltage gain, having a peak of 10 V/V. (d) Polarization characteristic of the ferroelectric capacitor shows an effective NC in both branches. Two discrete NC regions are observable in the reverse sweep of the gate voltage due to the polycrystallinity of the ferroelectric film. (e) $g_m/I_d$ is considerably enhanced and reached a value of 400 V$^{-1}$. (f) shows the impact of the drain-to-source electric field on the steepness and hysteresis of the NC-FET.
curve in the positive going branch while it shows a different behavior in the reverse sweep. The ferroelectric performs two separate NC regions, demonstrating a zig-zag polarization characteristic. This mainly happens due to the following reasons; (i) the polycrystalline PZT is showing two main polarization domains despite the applied training procedure and (ii) a multi-domain ferroelectric can hold one negative capacitance domain at a time. As a result, the manifested polarization characteristic of the multi-domain ferroelectric is different from the S-shaped curve which is expected for a single-domain ferroelectric. Therefore, each domain shows a separate NC region independent of the other one (see Figure 6c), which was also expected from $dV_{int}/dV_g$ vs. $V_g$ curve where two individual peaks of the voltage amplification were clearly observed. Figure 5d illustrates the current efficiency enhancement with a maximum value of 400 V$^{-1}$. Figure 5f investigates the impact of the drain-to-source voltage, $|V_{sd}|$, on the input transfer characteristic of the same NC-FET. Besides the common effect of $V_{sd}$ on the level of the drain current, it is evidenced that the NC-FET under lower lateral electric field provides a more effective NC effect and hence, a steeper off-to-on transition. This is due to the fact that $V_{ds}$ affects the accessible region of the ferroelectric S-curve polarization during the NC-FET operation. An SS of 5 mV/decade is achieved at a $V_{ds}$ of 0.5 V. The off-to-on transition of NC-FETs with reduced hysteresis (both n- and p-type devices) is not as steep as one of the large hysteresis devices, confirming the proposed theory that a trade-off is needed between the steepness and hysteretic behavior. A ferroelectric capacitor that implies a too effective NC results in a large hysteresis together with a sharp transition. Although a super steep switching device is compelling, however, it is not appealing since the reduction of SS is accompanied with a remarkable hysteresis.

**Conclusion**

Energy efficient logic devices are required for the recent advancement of the Internet of Things (IoT) technology. A steep slope field effect transistor with a sub-thermal swing is
expected as a key, enabling technology for IoT applications by operating at supply voltages below 0.5 V. Here, it has been shown that the negative capacitance effect can be effectively applied to enhance both digital and analog FoM of advanced CMOS. The measured input transfer characteristics of n- and p-type MOSFETs using PZT as the NC booster shows a steep subthreshold swing down to 10 mV/decade together with an enhanced efficiency factor up to $10^5 V^{-1}$. The on-current over off-current ration is improved and the overdrive is boosted up to 0.45 V. Therefore, the supply voltage can be reduced by 50%, maintaining the same performance. This is due to the fact that with the aid of a series connected negative capacitor (i.e., with the internal voltage amplification provided by the NC component of the PZT capacitor) the surface potential in MOS devices is increased beyond the applied gate voltage. It has been also demonstrated that the hysteretic behavior of NC-FETs can be tuned considering the proposed stability condition. Both n- and p-type NC-FETs with large (3-4.5 V) and reduced hysteresis (150-200 mV) are implemented, arguing that a trade-off is required between the steepness and hysteretic behavior of an NC-FET. The impact of the drain-to-source electric field on the boosting effect of NC is also demonstrated and discussed, indicating that a lower lateral electric field in the channel results in a steeper off-to-on transition. It is also experimentally evidenced that a poly-domain ferroelectric cannot have more than one NC domain at a time and shows a zig-zag characteristic.

**Acknowledgement**

The authors acknowledge the ERC Advanced Grant Milli-Tech (Grant NO. 695459) for providing the financial support of this research. The authors also greatly appreciate the contributions of Mr. Robin Nigon and Prof. Paul Muralt in the fabrication of the PZT thin film.
References

(1) Takagi, S. et al. Carrier-transport-enhanced channel CMOS for improved power consumption and performance. *IEEE Transactions on Electron Devices* **55**, 21–39 (2008).

(2) Khandelwal, S. et al. Circuit performance analysis of negative capacitance FinFETs. In *VLSI Technology, 2016 IEEE Symposium on*, 1–2 (IEEE, 2016).

(3) Ionescu, A. M. et al. Ultra low power: Emerging devices and their benefits for integrated circuits. In *Electron Devices Meeting (IEDM), 2011 IEEE International*, 16–1 (IEEE, 2011).

(4) Salahuddin, S. & Datta, S. Can the subthreshold swing in a classical FET be lowered below 60 mv/decade? In *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, 1–4 (IEEE, 2008).

(5) Salahuddin, S. & Datta, S. Use of negative capacitance to provide voltage amplification for low power nanoscale devices. *Nano letters* **8**, 405–410 (2008).

(6) Zubko, P. et al. Negative capacitance in multidomain ferroelectric superlattices. *Nature* **534**, 524–528 (2016).

(7) Jo, J. et al. Negative capacitance in organic/ferroelectric capacitor to implement steep switching MOS devices. *Nano letters* **15**, 4553–4556 (2015).

(8) Gao, W. et al. Room-temperature negative capacitance in a ferroelectric–dielectric superlattice heterostructure. *Nano letters* **14**, 5814–5819 (2014).

(9) Ionescu, A. M. Negative capacitance gives a positive boost. *Nature nanotechnology* **13**, 7 (2018).

(10) Khan, A. I. et al. Negative capacitance in a ferroelectric capacitor. *Nature materials* **14**, 182 (2015).
(11) Appleby, D. J. et al. Experimental observation of negative capacitance in ferroelectrics at room temperature. *Nano letters* **14**, 3864–3868 (2014).

(12) Yeung, C. W., Khan, A. I., Sarker, A., Salahuddin, S. & Hu, C. Low power negative capacitance fets for future quantum-well body technology. In *VLSI Technology, Systems, and Applications (VLSI-TSA), 2013 International Symposium on*, 1–2 (IEEE, 2013).

(13) Jain, A. & Alam, M. A. Stability constraints define the minimum subthreshold swing of a negative capacitance field-effect transistor. *IEEE Transactions on Electron Devices* **61**, 2235–2242 (2014).

(14) Khan, A. I., Yeung, C. W., Hu, C. & Salahuddin, S. Ferroelectric negative capacitance MOSFET: Capacitance tuning & antiferroelectric operation. In *Electron Devices Meeting (IEDM), 2011 IEEE International*, 11–3 (IEEE, 2011).

(15) Rusu, A. & Ionescu, A. M. Analytical model for predicting subthreshold slope improvement versus negative swing of S-shape polarization in a ferroelectric FET. In *Mixed Design of Integrated Circuits and Systems (MIXDES), 2012 Proceedings of the 19th International Conference*, 55–59 (IEEE, 2012).

(16) Saeidi, A. et al. Negative capacitance field effect transistors; capacitance matching and non-hysteretic operation. In *Solid-State Device Research Conference (ESSDERC), 2017 47th European*, 78–81 (IEEE, 2017).

(17) Saeidi, A., Biswas, A. & Ionescu, A. M. Modeling and simulation of low power ferroelectric non-volatile memory tunnel field effect transistors using silicon-doped hafnium oxide as gate dielectric. *Solid-State Electronics* **124**, 16–23 (2016).

(18) Saeidi, A. et al. Negative capacitance as performance booster for Tunnel FETs and MOSFETs: an experimental study. *IEEE Electron Device Letters* (2017).
(19) Saeidi, A., Jazaeri, F., Stolichnov, I. & Ionescu, A. M. Double-gate negative-capacitance MOSFET with PZT gate-stack on ultra thin body SOI: an experimentally calibrated simulation study of device performance. *IEEE Transactions on Electron Devices* **63**, 4678–4684 (2016).

(20) Karda, K., Mouli, C. & Alam, M. Switching dynamics and hot atom damage in landau switches. *IEEE Electron Device Letters* **37**, 801–804 (2016).

(21) Li, K.-S. et al. Sub-60mv-swing negative-capacitance FinFET without hysteresis. In *Electron Devices Meeting (IEDM), 2015 IEEE International*, 22–6 (IEEE, 2015).

(22) Jimenez, D., Miranda, E. & Godoy, A. Analytic model for the surface potential and drain current in negative capacitance field-effect transistors. *IEEE Transactions on Electron Devices* **57**, 2405–2409 (2010).

(23) Aziz, A., Ghosh, S., Datta, S. & Gupta, S. K. Physics-based circuit-compatible spice model for ferroelectric transistors. *IEEE Electron Device Letters* **37**, 805–808 (2016).

(24) Hoffmann, M., Pešić, M., Slesazeck, S., Schroeder, U. & Mikolajick, T. Modeling and design considerations for negative capacitance field-effect transistors. In *Ultimate Integration on Silicon (EUROSOI-ULIS), 2017 Joint International EUROSOI Workshop and International Conference on*, 1–4 (IEEE, 2017).

(25) Kidoh, H., Ogawa, T., Morimoto, A. & Shimizu, T. Ferroelectric properties of lead-zirconate-titanate films prepared by laser ablation. *Applied physics letters* **58**, 2910–2912 (1991).

(26) Nakamura, T., Nakao, Y., Kamisawa, A. & Takasu, H. Preparation of Pb (Zr, Ti) O₃ thin films on electrodes including IrO₂. *Applied physics letters* **65**, 1522–1524 (1994).

(27) Khan, A. I., Radhakrishna, U., Chatterjee, K., Salahuddin, S. & Antoniadis, D. A.
Negative capacitance behavior in a leaky ferroelectric. *IEEE Transactions on Electron Devices* **63**, 4416–4422 (2016).

(28) Lin, C.-I., Khan, A. I., Salahuddin, S. & Hu, C. Effects of the variation of ferroelectric properties on negative capacitance FET characteristics. *IEEE Transactions on Electron Devices* **63**, 2197–2199 (2016).

(29) Saeidi, A. *et al.* Effect of hysteretic and non-hysteretic negative capacitance on tunnel FETs DC performance. Tech. Rep., Institute of Physics (2018).

(30) Khan, A. I. *et al.* Negative capacitance in short-channel finfets externally connected to an epitaxial ferroelectric capacitor. *IEEE Electron Device Letters* **37**, 111–114 (2016).

(31) Jo, J. & Shin, C. Negative capacitance field effect transistor with hysteresis-free sub-60-mv/decade switching. *IEEE Electron Device Letters* **37**, 245–248 (2016).

(32) Rusu, A., Saeidi, A. & Ionescu, A. M. Condition for the negative capacitance effect in metal–ferroelectric–insulator–semiconductor devices. *Nanotechnology* **27**, 115201 (2016).

(33) Zhu, Z. *et al.* Negative-capacitance characteristics in a steady-state ferroelectric capacitor made of parallel domains. *IEEE Electron Device Letters* **38**, 1176–1179 (2017).