Visible Light Communication Design and Implementation

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Abstract. There have been many recent technological developments in wireless communication and exponential growth in demand such as lack of sufficient space, bandwidth restriction, and interference. Radio waves have been used to interact conventionally, and there is a growing obligation to look for new technology because of this challenge. Therefore, contact using light is a very motivating vision of wireless communication to solve most challenge. LiFi (Light Fidelity) is the modern contact approach. Visible Light Communication (VLC) simultaneously addresses enlightenment and communication problems. In this paper, a VLC concept was conceived and implemented.

Keywords. Visible Communication, Implementation, LiFi (Light Fidelity), Visible light Communication (VLC).

1. Introduction
The project aims to develop a prototype to create a communication connection that uses the visible transmission spectrum. This is generally called Visible Light Contact (VLC). Moreover, it attempts to balance the inherent trade-off between speed and distance in terms of precision. The goal is to achieve data rates of 1Mbps at 50 cm with an accuracy exceeding 99%. VLC is a modern concept that could influence the future of wireless communication. In VLC, information is conveyed by modulating the visible light spectrum (400–700 nm) used for illumination. Analytical and experimental work has shown VLC’s ability to provide high-speed data transmission with the added benefit of enhanced energy efficiency and security/privacy in transmission. VLC is still in the early investigation stages. There are fewer review papers written on this subject mainly dealing with research in the physical layer. Unlike other articles, this article presents a VLC perspective framework along with the current literature survey and possible obstacles to VLC implementation and integration [1]. Lighting absorbs about 19 percent of the energy used worldwide, and because obsolete lighting sources are still in use worldwide, there is significant potential for saving electricity. There are some drawbacks also for fluorescent lamps, with greater luminous efficiency than incandescent and halogen lamps. This article presents the findings under several aspects of an examination of the ability of light emitting diodes (LEDs) as a light source for use in buildings and compares them to more integrated sources. It involves a summary of the scientific papers, government reports, and product catalogues from seven manufacturing firms for lighting sources. Results showed that LEDs have a long lifetime, a wide range of correlated color temperatures, good luminous efficiency, index of color rendering, and many other similar characteristics to fluorescent lamps. However, the production costs are still higher than those of other lighting systems and too many low-quality LEDs are still available on the market. In addition, LEDs with inefficient heat dissipation can have high lumen depreciation and; thus, a shorter lifetime.
However, despite these limitations, LED technology is rapidly developing and, unlike other light sources, it has tremendous potential for development, and maybe the best option for lighting in the coming years [2-7]. Yet, VLC requires networked multi-cell activity in traditional indoor environments to achieve seamless coverage and high data rate. This kind of cellular network is called an optical atto-cell network. Co-channel interference (CCI) between adjacent optical atto-cells within such network limits network capacity. To optimize device efficiency and improve signal quality across the entire coverage area, mitigation of CCI is required. The multipoint joint transmission (JT) principle is adapted to the cellular VLC network. It can generally be defined as concurrent data transmission to a mobile station (MS) from multiple co-operating base stations (BSs). In a VLC JT system, the co-ordinated transmission prevents heavy CCI and, in addition, a basic feature of intensity modulation (IM) systems is leveraged. This is because signals are often constructively superimposed in direct contrast to radiofrequency (RF) dependent systems. Therefore it is possible to increase the cell-edge consumer signal to interference plus noise ratios (SINRs). The results show that, compared to a complete frequency reuse system [8-15], the JT scheme increases the mean SINR by 16.4 dB. In this paper, there is an urgent need to search for a solution to this spectrum-crunch and its growing demand fuelled by the need for emerging technology such as the Internet of Things. Interestingly, we are facing the one plausible option-visible light. This idea led to an entirely new, rapidly emerging eld of light fidelity, or popularly known as LiFi. It is a concept frequently used in lieu of Visible Light Communication and is a method that attempts to solve together the issue with enlightenment and communication. This is accomplished by manipulating the light sources at high frequencies, rendering a sensitive photodiode indiscernible to the human eye. There are various uses of such a communication device. Imagine a driverless car headlamps interacting with the traffic lights to decide whether to step forward or not. Take the indoor positioning system, where the mobile camera can be used to communicate with the surrounding lights to assess our location in, say, a large shopping.

Thrilled by these varied applications, we agreed to create a Visible Light Communication Based Link prototype. The current project aims to submit the data as quickly as possible while preserving the reception accuracy required. In this case, the project consists of a transmitter, an LED, which will relay the message signal to the receiver.

2. Methodology
The project design aims to create a communication connection using the visible light where the data is taken from a file, sent over the connection, and stored again in a file at the receiving end. The challenge is not only to independently design the hardware and software systems but also to design and incorporate a seamless integration between the two. In terms of hardware, there are two components of a standard communication device, one on the transmission and one on the receiving end. The complexity of the receiver increases also to ensure the synchronous transmission of data. With these broad categorizations in mind, the Project Hardware Module basically consists of 4 sub-systems, namely: the transmitter circuit, the receiver circuit, and the clock synchronization circuit. The second and third components together form the hardware at the receiver while effectively incorporating the fourth element to make the device portable. In essence, the transmitter circuit has to take the input data and send it over the wire. The receiver circuit is designed to collect data and process the waveform from the connection and from the file. As the name suggests, the clock synchronization component allows for synchronous data reception by retrieving the clock. We have a software component in addition to this hardware part. The data from a file is read onto the tivaC board at the transmission end, where the data is encoded using encoding, and then sent to a pin at the appropriate frequency. This pin output acts as the reference to the transmitter circuit. The hardware itself does the decoding at the receiving end and then the tivaC only needs to read the data and extract it and send it to the receiving end through the USB connection to the device. A shift register is used to allow for the simultaneous reading of four pins. Figure 1 and 2 displays the block diagram for the transmitter and the receiver. It also provides a protocol for beginning and stopping the receipt.
3. System implementation

3.1. Communication protocol

In addition to encoding, On-O Keying (OOK) was used. On-O keying simply gives an output of 5V when the output is 1 bit and 0V when the input is 0. Although On-O Keying has the downside of lowering the average light value and thus reducing the power, the primary reasons behind the option were its flexibility in implementation and debugging. Simply, Bit 1 is encoded as 10, and Bit 0 as 01. Naturally, the encoding on top of OOK refers to the PLL circuit, and the PLL circuit gives us the decoded output directly and that was the prime reason for using this encoding. For transmission, a sequence of 0s is sent initially, which gives a sequence of 01 when encoded, and helps lock the PLL. Then it sends a start list, then the actual data is sent, and message is terminated. Both the transmitter and the receiver are aware of these sequences and so the receiver knows when to start saving the data and when to end it.

3.2. Transmitter code

The transmitter's (TivaC) task is to regularly send encoded bits to the Transmitter circuit. Although this seems to be a trivial task at r-s-t using a timer interrupt, there are some issues, especially due to the USB connection. The TivaC has a USB receiving buffer that is filled when something is sent from the Device. This is done with the assistance of Pyserial and PyUSB. As the TivaC receives data from the PC it immediately goes into the interrupt receiving handler which then takes the collected bits and stores them in its memory. Using the Timer Interrupt, this function interrupts the usual transmission and as a result the entire hardware goes hay way. There are also several other problems, such as the initial 30 bytes obtained by the TivaC are garbage value, and some buffer (3-4 seconds) between connecting the USB and sending the bits from the PC must be present. As stated, the TivaC has a sufficiently wide non-volatile memory; it is best for testing purposes to have hardcode the file into TivaC. If it is understood that the data is to be transmitted, the transmitter encodes the data and stores it in a buffer. It initially sends a synchronizing sequence that the PLL uses to lock and, once the PLL is locked, it continues to send the data to be distributed (implemented as a circular array) in a circular fashion. The synchronous circuit also requires few additional bits to operate. A start sequence and end sequence are applied to the data being transmitted at the beginning and end, respectively.
3.3. Transmitter circuit
The transmitter circuit takes the data (to be transmitted) as the TivaC board input and drives the LED according to the input data. The circuit is simple and consists mainly of an LED driver and a resistor to control the light intensity. To drive the signal, our circuit implementation uses the IC SN7440N which is a dual quad input NAND gate. At the input, there are pull-up resistors and similarly pull-down resistors at the output to control the amplitude of the guided signal and thus the average LED strength. This is an important factor since the primary use of the light source is mostly not communication in VLC applications but rather is to provide illumination. Thus, to achieve a dual motive, it is important that we should not be an ecting of the primary intent. The sensitivity of the photodiode is another factor that necessitates regulation of average intensity. The photodiode that is used is always sensitive in a range of intensities and appears to underperform or saturate if we use it beyond this range. Thus, depending on the distance between the transmitter and the receiver, these values will need to be tuned. Any basic logic gate with proper function can be used for the LED driver. Due to its low resistance of the NAND gate, we used a NAND gate in case a low logic is driven at the output which ensures that the output is not an elected.

3.4. Receiver circuit
As the name indicates, the receiver circuit refers to the hardware at the receiving end of the signal which is used to collect and retrieve the signal. This circuit basically captures the data, amplifies the captured signal, and lends the noise to the waveform that can be used to synchronize the clock. A photodiode absorbs the light, producing a current whose magnitude is proportional to the intensity of the light falling on the photodiode. It is important to remember that there is a number of intensities where the photodiode performance is good and it should be ensured that the diode is worked within this range so that the output is not saturated. To this end our circuit implementation uses BPW34 photodiode. One of the key reasons for using this was that it had a relatively small fall and rise time of about 100ns which would allow us to work at higher frequency ranges and transfer data easily allowing for better data rates. The photodiode supplies a very small current of the order of microamperes (10^-6A) to be amplified before use. Therefore, the current is passed through a large resistor to amplify the voltage connected to a bu er voltage for further use of this voltage. The bu er ensures isolation of the remaining portion of the above circuit. This is important since the current in this section of the circuit is very low and, if it was to be connected directly, it could be ected by the other sections of the circuit. The implementation circuit for transmitters is shown in figure 3.

Figure 3. Transmitter implementation.
This program has no high frequency noise but has a low frequency spectrum instead. This is mostly because the noise applied to the device comes from the photodiode light falling on the ambient light. Speed actuations have a frequency variable equal to that of supply frequency equivalent to 50Hz. Thus the removal of the 50Hz portion from the received signal is necessary. If this is not achieved, then the waveform looks like a real wave modulated on a very low frequency wave (which corresponds to 50Hz in fact). Thus, a simple high pass RC filter with a cut-off frequency of 700Hz is passed through the waveform. The waveform has been elevated at this stage and loses its rectangular shape. The output is passed through a comparator to ensure recovery of the original rectangular waveform. The comparator used here is LM361 which works very well up to 1 MHz, well above the range required. The comparator output is then fed to the circuit of clock synchronization and frequency correction.

3.5. Clock synchronization and frequency correction circuit
The functions of clock synchronization and frequency correction to remove the clock from the received signal and synchronize with the received signal in the extracted clock. This particular phase is important as we need to get a reference clock for as we will analyze the data we have obtained. Not only that, but the relation must also be arranged in such a way that the correct sampling takes place, that is, the data will be sampled at the right time. The receiver circuit is shown in figure 4.

![Figure 4. Receiver implementation.](image)

The immediate concern is how the PLL circuit can remember the clock until the actual data is transmitted. The data sent and received will be encoded, as stated earlier. And obviously the data would be an aperiodic sequence of 1’s and 0’s. Depending on the data being sent, the transitions from high to low will occur at any time. The PLL should not react to EVERY transition but only to a selected number of transitions that are periodic and correspond to the actual frequency of the transmitted data.

3.6. Shift register and receiver code
The receiver circuits will emit decoded bits of the clock. This is transmitted into a Ledger of Changes. The researchers selected SN7495 as the Register of Shifts. The shift register has a number of modes and the left and right loads are used for the project serial shift, i.e. it essentially takes in a serial input and gives the right output on 4 pins. It takes the PLL clock and data output as its input and gives the current 4 bits of the data output synchronously; receiver code the receiver has 4 pins from the shift
register going into its 4 gpio pins. The clock is sent to a TivaC gpio pin, and a gpio interrupt is enabled on this pin with the interrupt being called at the edge increases. When an increasing edge is detected, an interrupt function handler is named which reads the 4 gpio pins to get the shift register info. Initially, the receiver (TivaC) checks for a sequence to start. When this start sequence is found, it knows that there will be relevant data after this. Since the shift register gives the performance of 4 pins, the receiver checks in multiples of 4 and uses these data to make up an entire byte. This is done in relation to the start sequence which, after every 4th clock cycle, checks whether to read the data or not. Thus at each \((4k + 1)\) edge it receives the lower nibble, and at each \((4k)\) elevation it receives the higher nibble and combines them to form a byte and increases the array pointer. It also checks whether the end sequence has come along at the same time. When the end sequence is reached it disables the interrupt. All the issues associated with the USB creep there too. Therefore we need to make sure that the USB interrupts are not allowed until they are all obtained. If it receives all that it transfers, the collected data to the PC using a USB connection.

4. Performance evaluation

The sample specifications are below. It has a detailed description of each of the components and the reasons for selecting the same. It is a simple circuit that uses an SN7440N IC NAND gate. It is a dual quad-input IC. The input is connected to the power supply via a 1.5k pull up resistor, while a 220 resistor attaches the output pin to the positive LED terminal. A NAND gate was used to drive the circuit primarily because, when the output is driven to a low, it has a very low resistance which allows it to sink easily in the current and thus does not distort the output. Figures 5 and 6 reflect the circuit transmitter and receiver.

![Figure 5. Transmitter circuit PCB, Note: 1.5k connected to 5V.](image)

The photodiode specifications were rapid response time, a visible spectrum spectral sensitivity, and a broad sensitive radiant field. The size of the sensitive radiant area is crucial and so the photodiode used was a VISHAY BPW34. The spectral bandwidth ranges from 430 nm to 1100 nm, which gives
the intended application a perfect range. It has a linear light strength to the present ratio and the sensitive region of the radiant is 7.5mm², which was larger than most photodiodes. It has an up and downtime of 100 ns each provides a 5 MHz switching frequency. This was accompanied by a high voltage follower to transform the signal to a voltage waveform and also to separate it electrically from the rest of the circuit. Then the output is passed through a high pass filter made using simple passive components of the RC. The filter feature specification was stop frequency = 100Hz, and transfer frequency = 5kHz. Using these values a frequency response was plotted and tested separately. It is important to remember that the condenser serves a double function here. It also serves as a decoupling condenser in addition to the later portion. The waveform was in the range of 0-5V until now since the NAND gate flips between 0 and 5V. After the condenser the system's DC value goes to 0 and the voltage swings in both the positive and negative values equally.

5. Test results
To check the individual components of the complete circuit, the following tests were carried out. The circuit was not complicated in the transmitter circuit, and therefore a simple test was carried out to ensure that the output matched the input without any phase difference. The output was voltage on the pin driving the Lead, again using a simple point-by-point debugging method for this circuit in the receiver circuit. Since the current at the photodiode output is very low and cannot be calculated by simple laboratory instruments, the voltage was measured directly after passing through a large resistor. The voltage buffer work was then tested particularly carefully. All tests up to this point were carried out by sending a pattern of alternating 0s and 1s through the previously tested transmitter. The signal at this stage is a slightly distorted wave of high frequency modulated over a wave of very low frequency due to ambient light which is basically the 50Hz noise. We pass this through a high pass filter to later out this noise and we find that the wave becomes stable with a zero DC value. However, the wave is distorted by imperfect OPAMP and channel frequency response. The comparator is input to the waveform. To try this out we made sure the comparator provided the right output and balanced the zeros of the comparator's distorted waveform and output. This is not important because it guarantees that the width of the bit is not ected, nor is there a step lag. The output of each pin was also tested on the DSO for the shift register, to ensure its proper functioning. Final PCB circuit is shown in Figure 7.

Figure 7. Final project circuit.
6. Conclusion
The project almost attained the expected targets by the end of the semester. The device is reasonably resilient to ambient light and with negligible bit error rate, it provides speeds up to 300 kbps. A number of device limitations are due to the limitation of the hardware used, and thus the expected speculations could not be fully achieved. The current implementation allows use of a torch as a source of illumination. Another option is to use an actual source of light which has a primary function of illumination for communication purposes. This will be a huge step towards making this a truly deployable product.

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