Mobility Enhancement by Sb-mediated Minimisation of Stacking Fault Density in InAs Nanowires Grown on Silicon

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Abstract

We report the growth of InAs$_{1-x}$Sb$_x$ nanowires ($0 \leq x \leq 0.15$) grown by catalyst-free molecular beam epitaxy on silicon (111) substrates. We observed a sharp decrease of stacking fault density in the InAs$_{1-x}$Sb$_x$ nanowire crystal structure with increasing antimony content. This decrease leads to a significant increase in the field-effect mobility, this being more than three times greater at room temperature for InAs$_{0.85}$Sb$_{0.15}$ nanowires than InAs nanowires.

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Semiconductor nanowires are leading candidates for future applications in a wide variety of electronic, photonic and sensing devices. III-V compound semiconductor nanowires including InAs and GaN have a number of potential functional advantages over elemental semiconductor nanowires including high mobility and direct bandgap. Furthermore the magnitude of the bandgap can be modulated by exploiting ternary compound semiconductors (such as InAsP and AlGaAs), allowing the creation of heterostructure nanowires with axially- or radially-modulated electronic properties. Such bandgap engineering is in principle a more powerful tool for nanowire-based devices than thin-film-based devices since the radial relaxation of strain in nanowires allows the growth of heterostructures whose constituent compounds are significantly lattice-mismatched.

The growth of compound semiconductor nanowires directly onto single crystal silicon wafers would be advantageous because (i) it would allow integration of nanowire devices with the established silicon CMOS technology; and (ii) silicon wafers are orders of magnitude cheaper than their compound semiconductor counterparts. Compound semiconductor nanowires are, however, typically grown using the “vapor-liquid-solid” technique in which gold nanoparticle catalysts seed the growth. Gold cannot be combined with silicon since it forms trap states in the silicon bandgap. Nickel has also been used to catalyze InAs nanowire growth on silicon but these nanowires are not functional for direct integration as they grow following random orientations with respect to the substrate. There have therefore been many reports of nanowire growth without the use of heterocatalytic nanoparticle seeds. In the case of the widely-studied narrow-bandgap semiconductor InAs, however, the absence of a heterocatalyst results in the nanowires displaying very high densities of defects including stacking faults, twin boundaries and polytypism, i.e. uncontrolled axial modulation of the crystal structure between the zinc-blende (cubic) and the wurtzite (hexagonal) polytypes of InAs. This in turn leads to an undesirable suppression of the electron mobility.

In this letter, we investigate an approach to reduce the defect density in catalyst-free InAs nanowires via the incorporation of antimony during the growth. We report for the first time the growth of catalyst-free InAs$_{1-x}$Sb$_x$ nanowires ($0 \leq x \leq 0.15$) on silicon. Due to their tunable nar-
row band-gap in the mid-infrared spectrum, InAs$_{1-x}$Sb$_x$ nanowires grown on Si make prime candidates for the fabrication of highly competitive and eco-friendly infrared photodetectors.\cite{23} We quantitatively determine the variations in crystal structure and defect density depending on the antimony incorporation before studying their effect on the nanowire electrical properties. The antimony incorporation suppresses the hexagonal phase and reduces the stacking fault density by up to one order of magnitude. The reduction of the stacking-fault density results in a large increase in the electron mobility above that of pure InAs nanowires. While an enhancement in the mobility of Au-nucleated InAs$_{1-x}$Sb$_x$ nanowires compared to InAs nanowires has previously been observed,\cite{24} this letter is the first report of the combination of advanced structural and electrical characterizations in gold-free InAs nanowires. By advancing crystal phase control in gold-free nanowires, our work will promote the development of future InAs nanowire-based devices directly integrated with silicon CMOS circuits.

**Experimental Details**

All InAs$_{1-x}$Sb$_x$ nanowires were grown on p-type Si (111) substrates without the use of catalysts in a Veeco molecular beam epitaxy (MBE) system equipped with a solid In source and As$_4$ and Sb$_2$ cracker cells. After an initial annealing of the substrate for 8 min at 760 °C under a constant arsenic flux with a beam equivalent pressure (BEP) of $0.8 - 1.0 \times 10^{-5}$ Torr, the temperature is lowered to 450–480 °C. Indium is introduced into the chamber with a BEP of $4.3 \times 10^{-8}$ Torr for 10 min to form 150–200 nm long InAs nucleation nanowires. The antimony supply is then additionally opened to start the InAs$_{1-x}$Sb$_x$ growth with the Sb$_2$ BEP ranging from 0.3 to $1.0 \times 10^{-7}$ Torr. After 110 min the growth is terminated by closing the indium and antimony supplies before cooling down the sample under an arsenic flux. For reference, InAs nanowires were similarly grown via a catalyst-free process on Si (111) substrates.\cite{1} summarizes the growth parameters for different nanowire samples (more details available in Supporting Information). The incorporation of antimony in the nanowires was controlled by varying the antimony fractional
Table 1: Growth parameters and morphology of InAs$_{1-x}$Sb$_x$ nanowires

| $T$ (°C) | FF$_{Sb}$ | diameter (nm) | length (μm) | Sb content (%) |
|----------|-----------|---------------|-------------|----------------|
| InAs     | 450       | 0             | 60-125      | 1.8–4          | 0              |
|          | 480       | 0.40          | 60–180      | 1.7–2.5        | 3.9            |
|          | 480       | 0.72          | 70–120      | 1.3–2.4        | 6.6            |
|          | 480       | 0.98          | 70–115      | 1.4–3.0        | 7.5            |
|          | 480       | 1.31          | 100–210     | 2.2–4.3        | 7.9            |
|          | 450       | 1.53          | 80–130      | 1.0–2.3        | 15.4           |
| InAs$_{1-x}$Sb$_x$ | 480       | 0.98          | 70–115      | 1.4–3.0        | 7.5            |
|          | 480       | 1.31          | 100–210     | 2.2–4.3        | 7.9            |
|          | 480       | 1.53          | 130–200     | 2.0–4.5        | 7.7            |
|          | 450       | 1.53          | 80–130      | 1.0–2.3        | 15.4           |

$\text{a Antimony fractional flux}$

flux (FF$_{Sb}$) representing the ratio of Sb flux to the combined (As and Sb) group-V material flux: $\text{FF}_{Sb} = F(Sb_2) / [F(Sb_2) + F(As_4)]$ where $F(Sb_2)$ and $F(As_4)$ are respectively the fluxes of antimony and arsenic. The Sb-content was extracted from high-resolution X-ray diffraction (HRXRD) measurements. Figure 1(a) shows an SEM image of InAs$_{0.85}$Sb$_{0.15}$ nanowires on a Si substrate after growth. The nanowires are generally vertically oriented on the substrate and have regular hexagonal cross-sections, as shown in Figure 1(b). Their length varies from 1.2 to 4.5 μm. The diameter remains constant along the length of the wire and varies between 60 and 210 nm from one nanowire to another. After growth the nanowires are dispersed in isopropyl alcohol and transferred onto degenerately B-doped silicon substrates coated by a thermally grown 250 nm thick silicon dioxide layer with pre-patterned macroscopic metal pads. An electron-beam sensitive resist (PMMA 950KA4, 4
300 nm thick layer) is spin-coated on the sample. Electron-beam lithography is then used to define contacts in two-point configuration between the selected nanowires and the existing pads. The contacts have a width of 250 nm and are separated by between 0.75 and 1.1 µm. To remove the native oxide surrounding the nanowires and assure highly transparent contacts, the contact area of the nanowires was treated by argon milling with a dose of 0.21 C.cm$^{-2}$. Only the contact area is treated during the argon milling process, as the remainder of the nanowire is protected by the PMMA resist. The argon milling is directly followed by an in situ sputter deposition of a 100 nm thick niobium layer. (c) shows a typical InAs$_{0.85}$Sb$_{0.15}$ device nanowire after connection of the contacts.

**Sb incorporation and structural characterization of InAs$_{1-x}$Sb$_x$ nanowires**

High resolution XRD measurements were used to study the solid composition of the InAs$_{1-x}$Sb$_x$ nanowires. From the angular position of the InAs$_{1-x}$Sb$_x$ peak, the lattice parameter was calculated by using Bragg’s law and the antimony content was subsequently extracted by using Vegard’s law.

![Shows the extracted lattice parameters and antimony content in InAs$_{1-x}$Sb$_x$ nanowires as a function of the Sb fractional flux for different growth temperatures. We estimate an overall uncertainty of less than 0.01 Å in the estimation of the change in lattice constant accounting for sample misalignment, detector and goniometer resolution and uncertainty in the position of the Bragg peak due to the presence of the short InAs stems. The influence of the two-dimensional layer grown along the nanowires was investigated by removing the nanowires from the samples with sticky tape. The peak intensity obtained for the stripped samples was almost two orders of magnitude lower than the peak obtained in presence of nanowires, therefore allowing us to neglect the presence of the two-dimensional layer for the determination of the nanowire lattice constant. For samples grown at 480°C, the nanowire lattice parameter increases when increasing
the Sb fractional flux from 0 to 1.3%. Above 1.3%, the antimony incorporation saturates at around 8.0%. By decreasing the growth temperature to 450 °C, a 15.4% incorporation was achieved. Varying the Sb fractional flux from 1.5% to 28.4% at 450 °C led to a significant increase in the antimony incorporation, up to 52%, as seen in Figure 3. However, nanowires become much shorter (≈0.3–0.7 μm) for higher fractional flux. Clusters develop on the substrate until the formation of a bare InAs$_{0.48}$Sb$_{0.52}$ film. Antimony atoms diffuse more slowly at 450°C than at 480°C which could favor the development of clusters to the detriment of nanowire growth. Surface preparation of the growth substrate with the patterning of holes in a SiO$_2$ mask, as commonly used in selective area epitaxy, could be a possible solution to this issue.

Figure 2: Antimony content and lattice parameter in InAs$_{1-x}$Sb$_x$ nanowires as a function of the Sb fractional flux for two growth temperatures (blue square for 450 °C and red circles for 480 °C).
Figure 3: (a–d) SEM images of InAs$_{1-x}$Sb$_x$ samples grown at 450 °C with various Sb fractional flux. The scale bar is 1 µm for all images. (e) Antimony content and lattice parameter in InAs$_{1-x}$Sb$_x$ samples grown at 450 °C as a function of the Sb fractional flux.
In order to quantify the distribution of polytypes and defects in the nanowires we have used high resolution TEM. III-V semiconductor nanowires usually crystallize either in the hexagonal wurtzite (WZ) phase or in the cubic zinc-blende (ZB) phase. Other specific polytypes such as 4H and 6H have been reported on rare occasions in nanowires. The zinc-blende structure is composed of interpenetrating face-centered cubic lattices corresponding to the stacking sequence “...ABCABC...” while the wurtzite structure consists of interpenetrating hexagonal lattices with a stacking “...ABAB...”. Each letter in this stacking sequence corresponds to a bilayer (i.e. a pair of atomic layers) with vertically stacked group III and V atoms. The planar defects observed in the InAs and InAs\(_{1-x}\)Sb\(_x\) nanowires can be classified in three main categories: rotational twins, stacking faults (SF) and grain boundaries. Details the stacking sequences of all encountered defects depending on the crystal structure. Rotational twins occur when a segment of the structure is rotated by 60° around the <111> growth axis leading to a change in the stacking sequence which becomes a mirror image of the regular lattice. The twin boundary occurs at the interface between the two regions with inverted stacking order. Stacking faults are partial displacements affecting the regular sequence in the stacking of the lattice planes. Intrinsic stacking faults result from a vacant plane while extrinsic stacking faults are due to the insertion of an extra plane in the sequence. In the wurtzite structure, there are two types (I\(_1\) and I\(_2\)) of intrinsic faults and one type (E) of extrinsic faults. The I\(_2\) and E type faults can be treated as short sequences of cubic stacking with I\(_2\) (i.e. ABCA) and E (i.e. ABCAB) corresponding to four and five cubic bilayers respectively. In the zinc-blende structure, there is one type of intrinsic stacking fault and one type of extrinsic fault. The cubic intrinsic stacking fault corresponds to 4 bilayers of hexagonal stacking. Finally, the grain boundary corresponds to a plane interconnecting two extended segments of single crystal phase, as seen in

Representative TEM images of nanowires with varying Sb content are shown in 5(a-d). The crystal phase content of each group of nanowires was estimated from the observation of the bilayers in the TEM pictures. We follow the metrics proposed by Caroff et al. and consider that at least four consecutive bilayers following the same stacking sequence are required to assign a specific
Figure 4: TEM images of InAs and InAs$_{1-x}$Sb$_x$ nanowires showing defect-free regions of wurtzite and zinc-blende structures and the various planar defects that are observed in both structures, including rotational twins, stacking faults and grain boundaries. The black arrow indicates the growth direction. The scale bar is 1 nm for all images.

crystal phase to any segment. An illustration of a minimal ZB segment in an overall WZ structure could be “...ABABABCA...” (i.e. an I$_2$ type fault). Along with the crystal phase content, we estimated the planar defect density – defects consisting of rotational twins, stacking faults and grain boundaries as detailed in 4 – and the distribution of the domain length for each group of nanowires. We define a domain by a stacking of three or more bilayers without defects. 6 shows the distribution of the domain lengths for each group of nanowires.

InAs nanowires show a dominant wurtzite structure and only 17% of the zinc-blende polytype on average. As seen in 5(e), the incorporation of antimony into the InAs crystal completely changes the structure from wurtzite dominant to zinc-blende dominant, even for Sb content as low as 3.9%. All InAs$_{1-x}$Sb$_x$ nanowires are predominantly composed of the zinc-blende polytype: from 75% for InAs$_{0.96}$Sb$_{0.04}$ nanowires to 99% for InAs$_{0.85}$Sb$_{0.15}$ nanowires. InAs and InAs$_{0.96}$Sb$_{0.04}$ nanowires both exhibit a pronounced polytypism and very short domains: more than 82% are less than 2 nm. As commonly found in nanowires grown without the use of catalyst, the nanowires generally present a high density of planar defects – here between 330 and 620 defects per microm-
eter. However, the distribution of defects into the different categories (twins, staking faults and grains) changes considerably with the antimony incorporation as seen in 5(f). For increasing antimony content, the twin density increases from 80 twins per micrometer in the InAs nanowires to 300 twins per micrometer in the InAs$_{0.85}$Sb$_{0.15}$ nanowire. In parallel the stacking fault density drastically decreases, by up to one order of magnitude between the InAs nanowires (360 SF per micrometer) and the InAs$_{0.85}$Sb$_{0.15}$ nanowires (35 SF per micrometer). InAs$_{0.85}$Sb$_{0.15}$ nanowires also present much longer domains: only 33% of the domains are less than 2 nm.

These observations agree with theoretical models and previous works on gold-catalyzed InAs$_{1-x}$Sb$_x$ nanowires grown by MBE, reporting variations in the structure and defect density as a function of antimony content. The tendency of antimony compound semiconductors to form zinc-blende structure over wurtzite is generally attributed to the low ionicity of the atomic bonds and the growth kinetics. Although twin-free ZB phase has been achieved for antimony content in the 10% range for gold-catalyzed InAs$_{1-x}$Sb$_x$ nanowires, the self-catalyzed nature of our process might require an higher incorporation to reach the same crystal quality. Plissard et al. reported a twin-free ZB phase in GaAs$_{0.66}$Sb$_{0.34}$ segments in GaAs/GaAsSb nanowires grown on silicon via a gold-free process.
Figure 5: (a–d) High resolution TEM characterization of catalyst-free InAs and InAs$_{1-x}$Sb$_x$ nanowires with increasing antimony content, all grown on silicon. Twins (T), stacking faults (intrinsic I and extrinsic E) and grain boundaries (G) are indicated in the figures. White arrows show the growth direction. The scale bar is 5 nm for all images (higher resolution available in Supporting Information). (e) Percentage of zinc-blende structure in the InAs and InAs$_{1-x}$Sb$_x$ nanowires as a function of antimony content. (f) Defect density in the InAs and InAs$_{1-x}$Sb$_x$ nanowires as a function of antimony content. The black diamonds represent the total number of defects including twins, stacking faults and grain boundaries. Error bars represent plus or minus one standard deviation.
Figure 6: Distribution of the length of the domains for catalyst-free InAs and InAs$_{1-x}$Sb$_x$ nanowires.
Electrical transport in InAs$_{1-x}$Sb$_x$ nanowires

Electrical characterizations were performed on the same three groups of InAs$_{1-x}$Sb$_x$ nanowires and on the pure InAs nanowires for reference. Electrical transport can take place either in the bulk or at the surface in an accumulation layer, and therefore various characteristics of the nanowires, such as resistivity or carrier concentration, scale with the diameter according to the type of transport. Other diameter-dependent parameters include the gate capacitance (which is used to extract parameters from field-effect measurements) and the crystal structure. To isolate the influence of antimony incorporation on the transport properties, we restricted the study to nanowires with diameter between 110 and 120 nm and assumed exclusively bulk conductivity in our calculations. A two-dimensional model was also investigated (not presented here) and gave results very similar to the bulk conductivity model in terms of resistivity, carrier concentration and mobility. Similarly to our previous work, the contact resistance was found to be almost two orders of magnitude lower than the bulk nanowire resistance, for both InAs and InAs$_{1-x}$Sb$_x$ nanowires, and therefore negligible. The resistivity of the different groups of nanowires was extracted using $\rho = \pi r^2 R / L$ where $r$ is the nanowire radius, $R$ is the nanowire resistance obtained from two-point measurements and $L$ is the distance between the contacts. As seen in the resistivity of the nanowires significantly decreases upon incorporation of antimony. InAs$_{0.85}$Sb$_{0.15}$ nanowires show a resistivity six times smaller than InAs nanowires.

Field-effect measurements were performed to determine the nanowire mobility and carrier concentration. (Inset) shows typical $I_{ds}$ vs $V_{ds}$ output characteristic obtained for an InAs$_{0.92}$Sb$_{0.08}$ nanowire field-effect transistor at room temperature, with $I_{ds}$ and $V_{ds}$ respectively being the drain-source current and voltage, and $V_g$ the back-gate voltage applied through the silicon substrate. The increase of conductivity with the application of a positive gate voltage demonstrates the n-type behavior of the nanowires. All InAs and InAs$_{1-x}$Sb$_x$ nanowires were found to be n-type. shows

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1 Thelander et al. have shown that the dependence of crystal structure upon diameter is much less marked for MBE-grown than MOVPE-grown InAs nanowires.
Figure 7: Average nanowire resistivity at room temperature as a function of the antimony content, calculated assuming a bulk conductivity. Error bars represent plus or minus one standard deviation.

the transfer characteristic \((I_{ds} vs V_g)\) for different \(V_{ds}\) ranging from 5 to 25 mV) of the same device. The field-effect mobility is estimated from \(\mu = g_m (L^2/C)(1/V_{ds})\) where the transconductance \(g_m\).

Figure 8: Transfer characteristic of an InAs\(_{0.92}\)Sb\(_{0.08}\) nanowire field-effect transistor at room temperature. Inset: Output characteristic of the same nanowire.

equals \((dI_{ds})/(dV_g)\) at a constant \(V_{ds}\) and \(L\) is the length of the channel, i.e. the distance between the contacts. \(C\) is the gate-nanowire capacitance which is derived from the metallic cylinder on an infinite plane model: \(C = 2\pi\varepsilon_0 \varepsilon_r L/cosh^{-1}[(r+t_{ox})/r].^{[1]}\) Here \(t_{ox}\) is the gate oxide thickness, \(\varepsilon_r\) is the relative dielectric constant of the dielectric material and \(r\) is the nanowire radius. Details regarding the adjustments to this model to fit semiconductor nanowires can be found in the Supporting Information. The average estimated normalized capacitance was \(5.3 \times 10^{-11} \text{ F.m}^{-1}\) for the InAs and InAs\(_{1-x}\)Sb\(_x\) devices. The peak field-effect mobility is obtained from the maximum value.
of $g_m$ with respect to $V_g$. Applying a negative back-gate voltage reduces the number of free carriers in the n-type nanowire channel until it reaches a complete depletion at the pinch-off point. At this point, the induced charge $Q$ is equal to $CV_{th}$ where $V_{th}$ is the threshold voltage extracted from the transfer characteristic. $Q$ represents the charge in the bulk nanowire and is equal to $e\pi r^2 L n_e$ (once again assuming a bulk conductivity). The carrier concentration $n_e$ is therefore estimated by using $n_e = (CV_{th})/(e\pi r^2 L)$.

Field-effect measurements were performed between 400 and 10 K on the InAs and InAs$_{1-x}$Sb$_x$ nanowires. The temperature-dependence of the extracted peak field-effect mobility and carrier concentration of individual nanowires is plotted in (9a) and (9b) respectively. Following the classic semiconductor behavior, the carrier concentration increases with temperature as the extra thermal energy allows electrons to go to the conduction band. This effect is especially visible for InAs$_{1-x}$Sb$_x$ nanowires compared to InAs nanowires owing to their reduced band gap. We observe an approximately linear enhancement in the mobility as the temperature goes down due to reduced phonon scattering. The mobility starts to saturate at lower temperature at which point it becomes limited by scattering events related to the nanowire structure including planar defects. Similar trends have been observed previously in InAs films, InAs nanowires and InAs-InP and InAs-InAlAs core-shell nanowires.

Figure 9: Temperature dependence of (a) normalized peak field-effect mobility and (b) normalized carrier concentration of InAs and InAs$_{1-x}$Sb$_x$ nanowires with 7.9% and 15.4% antimony. The mobility and carrier concentration have been normalized with respect to the values obtained for each nanowire at room temperature.
The average nanowire carrier concentration and peak mobility extracted from the field-effect measurements are displayed in [10] as a function of antimony content, zinc-blende content and stacking fault density. By taking into account the error bars, the carrier concentration shown in [10] (b) appears to be almost independent of the antimony incorporation. At room temperature, the average carrier concentration varies only very slightly with the Sb incorporation increasing from $2.9 \times 10^{17} \text{ cm}^{-3}$ for InAs nanowires to $3.7 \times 10^{17} \text{ cm}^{-3}$ for InAs$_{0.85}$Sb$_{0.15}$ nanowires. This is probably attributable to the fact that the intrinsic carrier concentration is higher in bulk InSb (2 $\times$ 10$^{16}$ cm$^{-3}$) than in InAs (8 $\times$ 10$^{14}$ cm$^{-3}$).

The catalyst-free InAs nanowires exhibit an average mobility of $\sim$500 cm$^2$/Vs at room temperature and $\sim$2000 cm$^2$/Vs at low temperature. The room temperature mobility is lower than values usually reported for defect-free Au-assisted InAs nanowires grown by MBE or CBE (1000–2000 cm$^2$/Vs range [22,47,48]) but is similar to the value reported for InAs nanowires with high defect density (500–750 cm$^2$/Vs range [22]). Despite a major change in the type of structure from wurtzite-dominant to zinc-blende dominant, the InAs$_{0.96}$Sb$_{0.04}$ nanowires present an average mobility very similar to the InAs nanowires. Both groups of nanowires have a high number of stacking faults ($\sim$350/µm) and especially small domain lengths. For higher antimony content, the mobility significantly increases. It reaches 1600 cm$^2$/Vs at room temperature for InAs$_{0.85}$Sb$_{0.15}$ nanowires presenting longer domains, a low stacking fault density but relatively high twin density. At 10 K, the mobility shows a similar trend, ranging from 1900 cm$^2$/Vs for the InAs$_{0.96}$Sb$_{0.04}$ nanowires to 3750 cm$^2$/Vs for InAs$_{0.85}$Sb$_{0.15}$ nanowires.

Here we consider three different candidate mechanisms that could be causing this marked increase in mobility with antimony content: (i) the different intrinsic electrical properties of InAs$_{1-x}$Sbx as a function of Sb content; (ii) the different electrical properties of the WZ and ZB polytypes of InAs$_{1-x}$Sbx; and (iii) the variation of the planar defect density. It seems unlikely that variation of the intrinsic properties with Sb content have a bearing on the mobility variation in our nanowires since the measured mobilities are two orders of magnitude lower than those of bulk InAs (40000 cm$^2$/Vs) and InSb (77000 cm$^2$/Vs). In addition the fractional change in mobility as
$x$ changes from zero to 0.15 for the nanowires is far greater than that for the corresponding bulk materials. We therefore eliminate the possibility that an intrinsic mechanism could account for the enhancement of mobility with Sb content. From [10](a,ii), the largest difference in the crystal structure polytype is observed between InAs and InAs$_{0.96}$Sb$_{0.04}$ nanowires but there is no significant difference in mobility between these two groups of nanowires. Therefore we can eliminate the possibility that different electrical properties of the WZ and ZB types account for the mobility change. Finally we consider the defect density, meaning twins, grain boundaries and stacking faults. From the combined results presented in [5](f) and [10](a,i), we observe that the mobility of the InAs$_{1-x}$Sb$_x$ nanowires increases with Sb content despite the increasing number of twin boundaries. This indicates that twins are not especially detrimental to the electron mobility. Grain boundaries are present in only one of the studied groups of nanowires thus we cannot determine how they might affect the mobility. Finally as seen in [10](a,iii), the field-effect mobility increases approximately linearly with the reduction of the stacking fault density. The change in mobility therefore seems to be dominated by the stacking fault density and the length of the domains. A stacking fault can lead to a change of structure with the introduction of short foreign domains (i.e. WZ domains in an overall ZB structure and vice versa), while the structure polytype does not change in the presence of a twin. This is in agreement with Thelander et al., who observed in the context of heterocatalysed InAs nanowires that mixtures of extended wurtzite/zinc-blende segments affect the electrical properties more significantly than isolated twin planes.

These measurements strongly suggest that the mobility enhancement in the nanowires originates from the reduction and stacking fault density and the presence of longer domains, although other parameters not investigated in this work such as the surface roughness could also play a role. Repeated type boundaries in the structure act as scattering sources for the carriers and create a strain in the structure modifying the carrier effective mass and therefore affecting the mobility.
Figure 10: (a) Nanowire mobility and (b) carrier concentration as a function of the (i) antimony content, (ii) zinc-blende content and (iii) stacking fault density. Red diamonds are room temperature data, blue squares are results obtained at 10 K. Each point is an average of the results obtained for five to ten nanowires. InAs nanowires are indicated by empty symbols and InAs$_{1-x}$Sb$_x$ by filled symbols. Error bars represent plus or minus one standard deviation.
Conclusion

In summary, we have grown InAs$_{1−x}$Sb$_x$ ($0 \leq x \leq 0.15$) nanowires on silicon substrates via a catalyst-free MBE process. Upon incorporation of antimony, we observed a drastic change in the crystal structure polytype from wurtzite-dominant in the InAs nanowires (17% ZB) to almost pure zinc-blende in the InAs$_{0.85}$Sb$_{0.15}$ (99% ZB). With increasing amounts of antimony, we observed a sharp decrease of the stacking fault density in the InAs$_{1−x}$Sb$_x$ nanowires and a significant increase of the domain length and field-effect mobility. The mobility was not significantly affected by the presence of defects in the form of twins. Through the adjustment of the growth conditions or antimony content, defect-free InAs$_{1−x}$Sb$_x$ nanowires with no polytypism may be achievable without the use of heterocatalytic nanoparticle seeds. This work is important for the development of functional nanowire devices integrated directly with silicon CMOS electronics.

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Supporting Information Available

This material is available free of charge via the Internet at [http://pubs.acs.org/](http://pubs.acs.org/).
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