BrainScaleS Large Scale Spike Communication using Extoll

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Abstract

The BrainScaleS Neuromorphic Computing System is currently connected to a compute cluster via Gigabit-Ethernet network technology. This is convenient for the currently used experiment mode, where neuronal networks cover at most one wafer module. When modelling networks of larger size, as for example a full sized cortical microcircuit model, one has to think about connecting neurons across wafer modules to larger networks. This can be done, using the Extoll networking technology, which provides high bandwidth and low latencies, as well as a low overhead packet protocol format.

1 Introduction

The Extoll network technology \cite{1} is based on the Tourmalet Network Interface Card (NIC). It offers 7 links and implements all the switching and interfacting capabilities, necessary to build an HPC network. Each Extoll link can comprise up to 12 serial lanes of 8 Gbit s\(^{-1}\) each. The NIC can be connected to a host node through a PCIe x16 Gen3 connector. In an Extoll network, the nodes are usually connected in a 3D-Torus topology, which offers good scaling characteristics. Routing of messages through the network is entirely done by the Tourmalet network chips and is based on a given 16 bit destination address in the message header. A BrainScaleS wafer module \cite{2} contains 48 reticles, each reticle comprising 8 HICANN chips which are connected to a Kintex 7 FPGA through 8 1 Gbit s\(^{-1}\) serial links. We consider the topology shown in Figure 1 to be optimal for interconnecting multiple wafers regarding bandwidth utilisation. 6 of these FPGAs are gathered at one of 8 concentrator nodes per wafer module, connecting them to one torus node, respectively.

2 Communication FPGA – Host

The communication between FPGAs and a host node uses the Remote Memory Access (RMA) protocol \cite{3}. Data moving towards an FPGA is immediately consumed by functional units in the FPGA. Data moving back to the host is written to main memory in the host. The arrival of new data at the host is notified to the software by making use of the notification system in the Extoll RMA unit and the low-level driver software.

2.1 Ring-Buffer Communication

In order to avoid additional handshake messages, FPGAs write their data to host memory in a predefined ring-buffer range for software processing. This communication is conducted after the scheme shown in Figure 2a. The ring-buffer is always
Figure 2: (a) The ring-buffer communication scheme implemented in the FPGA for data movement to the host. (b) The event-accumulation buffer, called bucket. Events are deserialised to groups of four to be transmitted to the network. (c) Management of multiple buckets using a map table and free bucket list. The Arbiter selects the most urgent bucket for flushing.

tracked by FPGA logic through the use of a write pointer and space registers. FPGAs exchange notifications with the software, informing each other about the amount of data written to or processed from memory. This implements a kind of credit based flow control [4].

3 Communication FPGA – FPGA

When wafer modules are interconnected to larger neural networks, spike events have to be exchanged between FPGAs in the network. Events coming from the HICANN chips to the FPGA comprise a 12-bit source neuron pulse address and a 15-bit timestamp, stating an arrival-deadline in system-time units [5]. As this does not inherently define a destination in the overall network, a lookup table is indexed to retrieve the respective network destination-address and a generic Global Unique Identifier (GUID) that will be transmitted over the network together with the event itself. At the destination, another lookup table is indexed with the received GUID, yielding a multicast mask to distribute the event among the HICANN chips connected to that FPGA.

3.1 Event Aggregation

Events arrive at the FPGA from the 8 HICANN chips with rates of up to approximately one event per 210 MHz FPGA clock. Due to header-overhead, single 30-bit events, i.e. one event per message, can only be shifted out at a rate of one event every two clocks. This shortcoming can be abated using packet aggregation [6]. In particular, this means accumulating events for the same destination and thereby aggregating bigger messages for transmission. At maximum, an Extoll packet can transport up to 496 B of payload, corresponding to 124 events. Figure 2b shows a bucket buffer which can aggregate events until a flushing condition is met. This is the case when the most urgent timestamp deadline is exceeded or when the buffer is full. In addition a flush can also be triggered by external logic, managing a set of buckets. To avoid large latencies, concurrent flushing and aggregation is implemented. Two counters track the filling level of a bucket. One increments for incoming events while the other one decrements for flushed events. The counters are swapped when a flush is triggered. As there are up to $2^{16}$ possible network destinations, the accumulation buffers need to implement a bucket renaming principle, in analogy to the well-known register renaming [7]. To always select the right buffer for an event with given destination, the buckets are managed by a map table and a list of free buckets. When the lookup table indicates an address to be new to the set of buckets, the address is assigned to the next free bucket. If no bucket is free the next appropriate one is flushed.

4 Summary and Outlook

We have presented a low latency, high bandwidth communication strategy for a waferscale neuromorphic computing system. Wafer modules can be interconnected by communicating spike events between FPGAs connected to HICANN chips. This is done using the Extoll networking technology. So far, the implementation of FPGA to FPGA communication is still work in progress, while the communication between host and FPGAs is currently being tested in the lab. The next step is to develop a simulation model of the event aggregation buckets and verify their functionality. One of the first multi-wafer networks will be a full scale cortical microcircuit model [8, 9].
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