Decanting the Contribution of Instruction Types and Loop Structures in the Reuse of Traces

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Abstract

Reuse has been proposed as a microarchitecture-level mechanism to reduce the amount of executed instructions, collapsing dependencies and freeing resources for other instructions. Previous works have used reuse domains such as memory accesses, integer or not floating point, based on the reusability rate. However, these works have not studied the specific contribution of reusing different subsets of instructions for performance. In this work, we analysed the sensitivity of trace reuse to instruction subsets, comparing their efficiency to their complementary subsets. We also studied the amount of reuse that can be extracted from loops. Our experiments show that disabling trace reuse outside loops does not harm performance but reduces in 12% the number of accesses to the reuse table. Our experiments with reuse subsets show that most of the speedup can be retained even when not reusing all types of instructions previously found in the reuse domain.
I. INTRODUCTION

A strong trend in the design of modern processors regards energetic efficiency of chips. Gate switching was one of the main components of power budgets, but in the last years CMOS technologies have been reducing the size of gates to a point where even leakage current can play an important role. Therefore, even microarchitecture mechanisms for general-purpose processors must take into account optimizations to reduce the amount of spent energy.

Reuse has been proposed as a microarchitecture-level mechanism to reduce the amount of executed instructions, collapsing dependencies and freeing resources for other instructions, thus improving performance and energy consumption. Previous works have considered reuse domains such as memory accesses, integer, or any instruction other than floating point ones, based on the reusability rate. However, these studies have not studied the specific contribution of reusing different subsets of instruction types for performance.

In this work, we intend to improve the understanding of how the performance gains of trace reuse are distributed in the code execution. This knowledge may be used to help reducing the number of accesses to the reuse table and reduce energy consumption, while keeping good performance.

This paper presents these main contributions:

1. The contribution of reuse inside and outside loops is presented, comparing performance and reuse table accesses for those to reusing in the entire code;
2. The sensitivity of trace reuse to subsets such as logical and arithmetic, branches, and memory address calculations is analysed, comparing their efficiency with their complementary subsets;
3. A comparison of trade-offs for memory budgets is discussed, where performance of reuse is compared to a similar area in first-level caches.

Our experiments show that disabling trace reuse outside loops does not harm performance but reduces in 12% the number of accesses to the reuse table. In the experiments with subsets, reusing only logical and arithmetic instructions achieves 92.8% of the speedup of reusing the entire reuse domain, reusing only 42.8% of the instructions. Reusing only branches produces 90.3% of the speedup, reusing only 14.5% of the instructions. Measurements of simulated energy spent in the reuse table support that reducing the number of accesses is much more important than reducing its size. Memory budget comparisons showed that doubling first-level caches is less effective than using the same area for reuse tables.

This paper is divided in following sections. First, related work is discussed in Section II. Then, the Reuse through Speculation on Traces (RST) architecture is revisited in Section III. Section IV briefly presents the simulation methodology and benchmarks used in this work. Section V presents our study about reuse inside and outside loops, while Section VI shows the contribution of different subsets of the reuse domain to performance and in-chip memory accesses. Finally, Section VII presents our concluding remarks and discussion of future works.

II. RELATED WORK

Many different mechanisms based on value reuse have been proposed. The reuse granularity includes instructions [1][2], expressions and invariants [3], basic blocks [4], traces [5][6][7], as well as instruction blocks and sub-blocks of arbitrary size [8]. The techniques vary in terms of their dependence on hardware and compiler support [8][9].

In most studies, memory accesses are not reused because of side effects and aliasing disambiguation difficulties. One approach to implement load and store reuse is to manage registers as a level in the memory hierarchy [10]. Another approach employs instruction reuse to exploit both same instruction and different instruction redundancy [11].

Many variations on value prediction have been proposed, including two-level value prediction [12], hybrid value prediction [12][13], and others, many of which were inspired by branch
prediction. Value prediction based on correlation [12, 14] uses global information about the path in selecting predictions. Prediction of multiple values for traces [13] may be done for only the live-out values in a trace, reducing necessary bandwidth in the predictor. Speculation control [15] is used to balance the benefits of speculation against other possibilities. Confidence mechanisms [16] are employed to improve value prediction by restricting prediction of unpredictable values. Past work that explored the limits of value prediction with trace reuse has shown there is much potential for performance improvement [17].

Wu et al. [9] proposed speculative reuse but requires compiler support. RST has the advantage of being independent of special compiler support, ISA changes, and extra execution engine for misprediction recovery.

Huang, Choi and Lilja [18] proposed a scheme that uses a Speculative Reuse Cache (SRC) and Combined Dynamic Prediction (CDP) to exploit value reuse and prediction. During execution, a chooser picks a prediction from the value predictor or a speculatively reusable value from SRC. With this approach, they have achieved a speedup of 10% in a 16-wide, 6-stage superscalar architecture, with 128 KB of storage for the CDP. RST has higher overall speedups and requires less storage [17, 19, 20].

Liao and Shieh [21] combined instruction reuse and value prediction, using a reuse buffer and a value prediction table, that are accessed in parallel. If inputs are unavailable, the value predictor is used. For a 6-stage pipeline, they achieved an average speedup of 9%. Unlike RST, this approach speculatively reuses instructions, rather than traces, and it requires two tables.

The Contrail architecture [22] used two threads, one with speculative execution running on low-latency functional units, and another thread validating results predicted by the first thread. The speculation thread aims to transform critical paths into non-critical paths, and the execution on slower functional units allow for reductions of up to 40% on energy dissipation. RST does not require an extra thread to validate results from speculation, making it simpler to implement. Trace speculation recovery uses a mechanism similar to those used for branch misprediction.

Our previous work in [19] studied the upper bound limits of RST in a superscalar architecture with oracle prediction. In [20], we did an extensive study on upper bound limits for feasible architectures, proposing a version with a unified reuse table to further reduce die area requirements. In this work, we intended to verify the impact of reducing the reuse domain or by reusing only instructions inside loops in overall performance.

Pratas et al. [23] developed a new constrained loop unrolling technique for reusing instruction inside loops in low power architectures. A controller was designed to identify reusable instructions within loops. This technique is more closely related to Trace Caches [24] than trace reuse, as both do not store operands but just the instruction themselves. However, [23] does not require an extra buffer, using the reorder buffer as source of instructions.

Tsumura et al. [25] identifies reusable regions by tracking subroutine call and return instructions, or by backward branches in the case of loops. This architecture uses threads running on other cores to validate speculative reuse. In our paper, we also tracked loops by observing backward branches, although subroutine calls were not analysed. Oda et al [26] extended Tsumura’s previous work by improving the efficiency of input memoization.

Tsai and Chen [27] proposed a Trace Reuse (TR) Cache to reduce energy consumption in embedded systems. Instead of reusing the computations, TR only reuses the decoded sequences of retired instructions, thus avoiding cache misses and improving overall efficiency. However, this mechanism was evaluated for simple embedded processors and may probably not scale well for use in out-of-order, more complex processors.

Rahimi et al. [28] used spatial memoization to reduce the costs of recovering errors in a SIMD architecture. An interesting feature of this work is the absence of reuse tables, where reuse occurs from an instruction running on a strong lane to the ones on the remaining weak lanes. Experimental results showed that 62% of recovery of errant instructions is avoided using their technique. The authors extended their work for floating points in GPUs [29], with results of energy saving from 8 to 28% for error correction.
III. The RST Architecture

RST (Reuse through Speculation on Traces) improves trace reuse and hides true data dependencies by allowing traces to be (i) regularly reused when all inputs are ready and match previously stored input values or (ii) speculatively reused when there are unknown trace inputs. Therefore, traces that could not be reused in previous approaches may be reused to exploit their redundancy.

Value reuse is non-speculative. After the input values of an instruction are verified against previous values and a match is found, the instruction can be reused without further execution. Resources are never wasted due to reuse and are available to other instructions. In trace reuse, a sequence of instructions—possibly spanning multiple branches—is the granularity of reuse. Input values to a trace are compared against previous values to check for a reuse opportunity, and when the inputs match the previous values, previously recorded outputs are used to update the architecture state. When a trace is reused, its outputs are written to registers, instructions are skipped, and true dependencies are collapsed.

Traces are created during runtime based on sequences of instructions in a reuse domain, which is the set of instruction classes that are allowed to be reused (e.g., integer operations, branches, and address calculations for loads and stores). Each trace has an input and an output context to store live-in and live-out values. The reuse domain is constituted by integer instructions without side effects. Floating-point instructions are not reused because they show little redundancy [6] and because they would require larger registers to be stored in the reuse table. The length of traces may be limited by the number of live-in and live-out values that can be stored, by the number of branches, and by the occurrence of instructions outside of the reuse domain. In loads and stores, the address calculation is split from the actual memory access, and the address calculation can be reused. System calls are not reused because they require a mode change in the processor status.

Figure 1 shows the structure of an entry in the reuse table (Memo_Table_T) [20]. The address of the first instruction of a trace is stored in \( pc \), and the address of the next instruction after the trace is stored in \( npc \). The \( npc \) field is used to set the PC and to skip the instructions belonging to the trace when it is reused. Fields \( icv \) and \( icr \) store the input values and register indexes, while \( ocv \) and \( ocr \) store the output values and register indexes. \( bm \) is a bitmap to mark branches that occur inside the trace, while \( btk \) bits are set when branches are taken. These two last fields are used to update the branch prediction mechanism.

|   | bits | 30 | 30 | 5n | 32n | 5m | 32m | b | b |
|---|------|----|----|----|-----|----|-----|---|---|
| pc | npc  | icr| icv| ocr| ocv | bm | btk|

\( icr_1 \), \( icr_2 \), \( \cdots \), \( icr_n \) and \( icv_1 \), \( icv_2 \), \( \cdots \), \( icv_n \) are the input values and register indexes, respectively.

\( ocr_1 \), \( ocr_2 \), \( \cdots \), \( ocr_3 \) and \( ocv_1 \), \( ocv_2 \), \( \cdots \), \( ocv_n \) are the output values and register indexes, respectively.

Figure 1: Structure of an entry in Memo_Table_T.

In this work, the unified reuse table proposed in [20] is used for the first set of experiments. This implementation uses a single table to store both isolated instructions and traces, reducing size requirements and also the number of table accesses, with performance results similar to using two tables. Besides, a unified table allows for speculative reuse of single instructions.

The second set of experiments rely on two tables, one for instruction reuse (Memo_Table_G), and Memo_Table_T for traces with two or more instructions. Details on trace construction and reuse can be found in [17, 19, 20].
IV. Simulation Methodology

For the studies presented in this paper, two different set of simulation tools based on modifications of sim-rst [20] were used. sim-rst is an out-of-order simulator based on sim-outorder from SimpleScalar [30], implementing in details a speculative trace reuse technique.

The first set included sim-rst-loop and sim-rst-outofloop. They both use backward branches to dynamically detect loop structures. The former simulator enables reuse only when such structures are detected, and disables it when the end of a loop is detected. The later does the reverse, enabling reuse only outside loops. These simulators were used in the first set of experiments to determine how much the natural redundancy in loops contributed to performance.

The second set of simulators based on sim-rst enabled or disabled the reuse of certain subsets of the reuse domain. These simulators were used to investigate the sensibility of trace reuse to instruction type.

The benchmarks bzip2, gcc, gzip, mcf, parser, and vortex from SPEC CPU 2000 benchmarks were simulated in all experiments. These benchmarks were found to be an interesting subset of SPEC CPU 2000 and simulating the entire set would be costly and probably would not bring further insights on the aspects that we were studying, as each simulation with a given configuration takes more than a day. Some of those benchmarks are even common to the SPEC CPU 2006 set.

We did not use sampling, because might break dynamic instruction flows that would produce redundancy, which was the aspect that we were mostly interested. Our previous study on limits of trace reuse used a similar methodology with very good results. In the first set of experiments, each benchmark is run for 1.5 billion instructions, from which 500 million instructions were fast-forwarded and the remaining 1 billion instructions were simulated. In the second set of experiments, from 1.7 to 2.5 billion instructions were simulated for each benchmark.

The baseline architecture configuration is summarized in Table 1.

| Parameter           | Value                                                                 |
|---------------------|-----------------------------------------------------------------------|
| Pipeline width      | 4 (2 ALUs, 2 memory, 1 mult)                                          |
| Pipeline depth      | 19 (4 fetch, 4 decode, 2 dispatch, 5 issue, 1 execute, 2 writeback, 1 commit) |
| IFQ, RUU, LSQ       | 16 instructions, 128 entries, 64 entries                              |
| Branch predictor    | 2-level                                                               |
| First level         | 13-bit register (xorred with PC)                                      |
| Second level        | 8192 entries                                                          |
| BTB                 | 4096 entries, 2-way                                                  |
| Instruction set     | PISA                                                                  |
| L1 cache            | 32KB I & D, 4-assoc, 64B lines, 1 cycle hit                           |
| L2 cache            | 512KB, 8-assoc, 256B lines, 5 cycles hit                              |
| L3 cache            | 2MB, 8-assoc, 256B lines, 20 cycles hit                               |
| Memory              | 200 cycles first chunk, 20 cycles next chunk                         |

In the first set of experiments, the same configuration with a single reuse table entry used in [20] was employed, because of the good balance between performance and table size. For the second set of experiments, larger input and output scopes were employed to avoid limiting reuse of longer traces. Two separated tables for instruction and trace reuse, Memo_Table_G and Memo_Table_T, were used. Table 2 summarizes the configurations for each experiment set.
Table 2: Reuse table configurations.

| Parameter            | First set | Second set |
|----------------------|-----------|------------|
| Trace input scope    | 2         | 4          |
| Trace output scope   | 1         | 4          |
| Memo_Table_T entries | 512       |            |
| Memo_Table_T assoc   | 4-way     |            |
| Memo_Table_G entries | n/a       | 1024       |
| Memo_Table_G assoc   | n/a       | 4          |

V. REUSE INSIDE LOOPS

As loops execute many times the same instructions over a set of variables, they probably execute redundant instructions as input values are limited to a finite set. To test this hypothesis, a subset of SPEC 2000 int benchmarks was analyzed to verify the patterns of instruction reuse and how they are related to loops. For each benchmark, 150 million instructions were executed in \texttt{sim-rst}. The last 100 thousand instructions were logged, with information about whether they were reused or not.

PC addresses of instructions that started traces were stored and then the log was followed backwards, finding common sequences of instructions occurring before these traces and how many times they occurred. These sequences characterize instructions inside loops. To be sure that these instructions were inside loops, the logs were verified for branch instructions with negative offsets, i.e., that jumped back to previous instructions. Preliminary results showed that a large number of traces were inside loops, hence we decided to investigate the contribution to performance of enabling reuse only inside traces.

Modifications in \texttt{sim-rst} made it possible to enable reuse only inside or outside loops, which were dynamically identified by branches with backward addresses.

i. Speedup

One of the main objectives of reusing instructions and traces is to improve performance. Hence, it is important to measure how much reusing traces created only inside loops will reduce performance improvements when compared to the non-speculative reuse mechanism DTM and the speculative reuse RST. A constrained version of RST with a single reuse table can achieve speedups of 1.24 over a baseline architecture without reuse \cite{20}, and even more with separated tables for single instruction and multiple instruction traces. In this subsection, we compare RST-Loop’s performance with those two alternative reuse schemes.

Figure 2 shows the speedup from RST-Loop over the original RST and DTM. The last column shows the harmonic mean (HM) of the speedups. As RST-Loop restricts reuse to loops, it is to be expected that it presents less performance than the original RST. For most benchmarks, the performance hit was not statistically relevant. The only benchmark that presented a significant loss was vortex, with 7.1% less performance than with RST. The harmonic mean speedup for RST-Loop over RST showed only 1.5% loss of performance.

When compared to DTM, which does not have speculative reuse, RST-Loop presented positive speedups for all benchmarks but \texttt{gzip} and vortex. Even for these two benchmarks the performance hit was small and less than 3%. When compared to DTM, it becomes even more clear that RST Loop can achieve most of the performance even if allowing reuse only inside loops, with a harmonic mean speedup of 1.045.

ii. Number of Accesses to Reuse Table

Each access to the reuse table consumes energy, therefore reducing the total number of accesses is expected to improve the overall energy consumption of processors with reuse mechanisms. In
this subsection, we explore how RST-Loop and its complement, RST-Out-Of-Loop, behave in terms of accesses to the reuse tables when compared to the original RST.

Figure 2 shows the percentage of reduction in the number of captured traces when using RST-Loop and RST-Out-Of-Loop (for the vortex benchmark only) compared to RST with unified reuse table [20]. Note that the bar representing vortex is out of scale. In average, there was a reduction of 20.4% in the number of accesses to the reuse table. All benchmarks presented less captured traces, but only mcf, parser, and vortex showed significant reductions.

The benchmark vortex is the one with the most interesting behaviour, with most of the reusable traces outside loops, which helps to explain its performance hit when reusing only inside loops (Figure 2). RST-Loop was able to reduce the percent of table accesses in a range from 1 to 12% for the benchmarks with good performance. In the specific case of vortex and RST-Loop, it was able to achieve 98% of the performance measured with non-speculative reuse (DTM) while reducing Memo_Table_T access by 78.5%, thus reducing energy consumption in a proportional way.

iii. Memory Trade-offs

To further study impact on performance and table access, three different in-chip memory trade-offs were simulated, all for the RST-Loop architecture with the exception of vortex, where RST-Out-of-Loop was employed. The first configuration used the results from the previous
experiments, simulating a 4-way, 512 entries reuse table, and 32 KB for each first level caches. Then, the budget for first level caches was doubled for the second configuration, while the reuse table size was kept the same. Finally, the last experiment uses the same amount of first level cache memory, but doubles the number of entries in the reuse table.

Figure 4 shows the average difference of performance over the first configuration, while Figure 5 presents the difference between the number of in-chip memory accesses when compared to the first configuration. Doubling the first level cache budget does not improve performance, with an average speedup of only 1.02. The number of cache and reuse table accesses decreased only 0.09%. Doubling the reuse table budget does not improve performance by much too, with an average speedup of 1.017. There was a decrease of 0.88% in the total amount of cache and reuse table accesses, which cannot be considered significant. These results show that reuse may be an interesting alternative to larger cache budgets.

![Figure 4: Speedups for memory trade-offs](image)

![Figure 5: In-chip memory access difference for memory trade-offs.](image)

VI. Contribution from Different Instruction Types

In the next experiments, the contribution for reuse performance of different instruction types was studied. Former experiments with DTM and RST have restricted their reuse domain to instructions without side effects (like memory accesses and system calls) and that were not floating-point instructions. The former was due to the increased complexity of implementation.
The later was done because floating-point instructions present less redundancy and require more storage space in the reuse tables.

Previous works considered a reuse domain that included all branches, integer logic-arithmetic instructions, and address calculations. For the measurement of the contribution of each subset of these instruction types, six different reuse domains were exploited: $B$ set, with only branches (conditional or not); $A$ set, with only add-subtract instructions (integer type); $M$ set, with only address calculations. The other subsets are the result of the difference between the $O$ original reuse domain set and the former three subsets: $\overline{B}$, $\overline{A}$, and $\overline{M}$.

Table 3 shows the instruction type distribution by benchmark measured in our simulations of the baseline architecture. Notice that the column *Other* represents a very small percentage of the total.

| Benchmark | Memory Access | Branches | Logic and Arithmetic | Other |
|-----------|---------------|----------|----------------------|-------|
| bzip2     | 32.92%        | 14.46%   | 51.33%               | 1.29% |
| gcc       | 39.32%        | 20.09%   | 39.98%               | 1.62% |
| gzip      | 40.44%        | 15.32%   | 50.97%               | 3.26% |
| mcf       | 34.59%        | 28.16%   | 36.74%               | 0.51% |
| parser    | 35.40%        | 23.12%   | 40.43%               | 1.05% |
| vortex    | 56.84%        | 16.57%   | 24.81%               | 0.36% |

Two main metrics were extracted from the results: the speedup, and the *Efficiency Index* (EI). The Efficiency Index was developed specially for this work and compares the number of reused instructions by the speedup for a given subset of the reuse domain. It can be defined based on the speedup and the Reuse Rate $RR(S)$:

$$EI(S) = \frac{\text{Speedup}(S)}{RR(S)}$$

Where $S$ is one of the reuse domain subsets previously defined. The Efficiency Index correlates the potential of improving performance with each of the reuse subsets.

The Reuse Rate is defined as the fraction of instructions from the subset $S$ that have been reused:

$$RR(S) = \frac{\text{Reused instructions}}{\text{Executed instructions from } S}$$

### i. Speedup

As for the experiments with reuse inside and outside loops, performance is still an important metric when considering the different reuse domains. Figure 6 presents the harmonic mean speedups for the $B$, $A$, $M$, and $O$ domain reuse sets, while Figure 7 shows the same information for the complement subsets $\overline{B}$, $\overline{A}$, and $\overline{M}$. The last column of each graph presents the harmonic mean (HM) for each set of instructions.

In Figure 6 the best performance is achieved with reuse of the full domain $O$, with a speedup of 1.16 over the baseline. The subset $A$ (adds and subs) comes in second, with a speedup of 1.08. The subset $B$ (branches) comes in third, with a speedup of 1.05, while the subset $M$ (memory address calculation) comes in last place, with a speedup of 1.02. Most benchmarks showed the same behaviour, with only mcf and vortex presenting different sensibility to the reuse domain. Excluding full reuse domain, the benchmark mcf was more sensible to reusing address calculations, while vortex was more sensitive to branch reuse.

For the complementary sets shown in Figure 7 where all instructions from the original reuse domain are reusable but for the selected subsets, the best results are obtained with full
Figure 6: Harmonic mean speedups for selected subsets.

Figure 7: Harmonic mean speedups for complement of subsets.
reuse domain, followed by not reusing address calculations ($\mathcal{M}$), then branches ($\mathcal{B}$), and finally add/sub ($\mathcal{A}$). The subset $\mathcal{M}$ presented a speedup of 1.13 over the baseline.

From these results, it is possible to assert that reusing only a limited subset of the instructions may still improve performance, but the benchmarks are very sensitive about which instructions are in the reuse domain. Restricting reuse may also reduce trace length, as instructions outside the reuse domain cannot be included in the trace and thus finish its building.

ii. Efficiency

In this subsection, we discuss the efficiency of reusing each of the reuse domains as a function of the Efficiency Index as defined in the beginning of this Section. The EI presents how much a reuse domain improves performance in comparison with the number of reused instructions. A reuse domain is more efficient when it reuses less instructions but achieves a better speedup. Therefore, larger IE are better.

Figure 8a shows the harmonic means of the Efficiency Index for the three subsets of the reuse domain, $\mathcal{B}$, $\mathcal{A}$, and $\mathcal{M}$. Figure 8b shows the EI for the complement subsets. As expected, the original reuse domain (full domain) presents the lowest efficiency, although it presents the better performance improvements.

The best efficiency was achieved by branch instructions, where only 19.6% of instructions were reused, but the speedup was 1.13. This is 90.3% of the speedup found reusing all instructions. Therefore, we may assert that branch reuse is an important complement to branch prediction.

An unexpected result is the contribution of add and subtract instructions to performance. Even though they are only 42.8% of the reused instructions in average, reusing only these instructions allowed to achieve 92.8% of the performance reusing the full domain. That may be explained by the small number of cycles that these instructions require for execution and how these impact less than branches and address calculations on the critical paths.

iii. Energy

Besides reducing the number of reuse table accesses, not reusing branches allows the reduction of the size of an entry in the trace reuse table $\text{Memo} \_\text{Table} \_T$ (Figure 1). For the configurations simulated in this experiment, that would represent a decrease of 10.7% in the area required for $\text{Memo} \_\text{Table} \_T$ according to CACTI [31]. For configurations with smaller input and output scopes such as the ones simulated in the first set of experiments, this reduction would be even larger.
Simulation of the reuse table configurations using CACTI 5.2 and a 0.35 nm technology showed that the energy required to read a Memo_Table_T entry was 327.7 mW. The same entry without the fields for branch reuse would require 320.6 mW, a reduction of only 2%. Therefore, reducing the number of accesses is more important than reducing the size of an entry in the table. As the subset including branches shows the best EI, leaving branch instructions outside of the reuse domain for such a small reduction in the energy spent in table reads would not compensate the performance loss.

VII. CONCLUSIONS AND FUTURE WORK

In this work, we presented a new evaluation of trace reuse taking into account the possibility of restricting reuse to some situations. Reusing only some classes of instructions or only instructions inside loops allow for reducing the amount of gate switching and required memory without losing much of the reuse potential. Hence, it becomes possible to apply trace reuse mechanisms in designs more restricted than general purpose superscalar processors, such as in the embedded market. Although [27] have already considered using reuse on embedded processors to lower power requirements, we understand that RST is a more flexible technique that can be tailored to different processors from embedded to general-purpose ones.

Studying the sensitivity of the trace reuse mechanism to instruction subsets makes it possible to understand the contribution of each subset within the trace reuse context. The creation of an Efficiency Index (EI), which is obtained from a division of each subset speedup by the percentage of instructions executed in that subset, allows for a more precise evaluation of the importance of each subset within the reuse mechanism. Subsets of logical and arithmetic instructions, branch instructions and memory access instructions were created and simulations were performed with them. We can conclude that logical and arithmetic instructions are very important in reuse mechanism, since they alone produce 92.8% of total reuse speedup, with only 42.8% of the reusable rate.

An important result is that branch instructions have the best EI, since they alone produces 90.3% of total reuse speedup, with only 14.5% of reusable rate, even though a two-level branch predictor was used. Hence, further studies were reuse is focused on leverage branch prediction are highly desirable. An unexpected result is the contribution of add and subtract instructions to performance. Even though they are only 42.8% of the reused instructions, reusing only these instructions allowed to achieve 92.8% of the performance reusing the full domain. Memory access instructions do not participate in trace reuse, only single instructions, but still produce more than twice the total reuse efficiency, using the index created as a comparative benchmark.

As more powerful processors are developed for smartphones and tables but still with strict power constraints, we intend to apply these results to the development of an architecture focused on high-end embedded processors.

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REFERENCES

[1] A. Roth and G. S. Sohi, Register integration: A simple and efficient implementation of squash re-use, in Proc. of the 33rd Annual International Symposium on Microarchitecture, (Los Alamitos, IEEE Computer Society, Monterey, 2000), pp. 223–234.

[2] A. Sodani and G. S. Sohi, Understanding the differences between value prediction and instruction reuse, in Proc. of the 31st Annual International Symposium on Microarchitecture, (Los Alamitos, IEEE Computer Society, 1998), pp. 205–215.
[3] C. Molina, A. González and J. Tubella, Dynamic removal of redundant computations, in *Proc. of the 13th ACM International Conference on Supercomputing*, (New York, ACM, Rhodes, 1999), pp. 474–481.

[4] J. Huang and D. J. Lilja, Extending value reuse to basic blocks with compiler support, *IEEE Transactions on Computers* **49**(April 2000) 331–347.

[5] A. T. da Costa and F. M. G. França, The reuse potential of trace memoization, Technical Report ES–498/99, COPPE–UFRJ (Rio de Janeiro, 1999).

[6] A. T. da Costa, F. M. G. França and E. M. CHAVES FILHO, The dynamic trace memoization reuse technique, in *Proc. of the 9th International Conference on Parallel Architectures and Compilation Techniques*, (Los Alamitos, IEEE Computer Society, Philadelphia, October 2000), pp. 92–99.

[7] A. González, J. Tubella and C. Molina, Trace-level reuse, in *Proc. of the 28th International Conference on Parallel Processing*, (Los Alamitos, IEEE Computer Society, Aizu-Wakamatsu, 1999), pp. 30–37.

[8] J. Huang and D. J. Lilja, Exploring sub-block value reuse for superscalar processors, in *Proc. of the 9th International Conference on Parallel Architectures and Compilation Techniques*, (Los Alamitos, IEEE Computer Society, Philadelphia, October 2000), pp. 100–110.

[9] Y. Wu, D.-Y. Chen and J. Fang, Better exploration of region-level value locality with integrated computation reuse and value prediction, in *Proc. of the 28th Annual International Symposium on Computer Architecture*, (New York, ACM, Göteborg, Sweden, June 2001), pp. 98–108.

[10] S. Önder and R. Gupta, Load and store reuse using register file contents, in *Proc. of the 15th ACM International Conference on Supercomputing*, (New York, ACM, Sorrento, Italy, 2001), pp. 289–302.

[11] J. Yang and R. Gupta, Load redundancy removal through instruction reuse, in *Proc. of the 29th International Conference on Parallel Processing*, (Los Alamitos, IEEE Computer Society, Toronto, August 2000), pp. 61–68.

[12] K. Wang and M. Franklin, Highly accurate data value prediction using hybrid predictors, in *Proc. of the 30th Annual International Symposium on Microarchitecture*, (Los Alamitos, IEEE Computer Society, December 1997), pp. 281–290.

[13] R. Sathe, K. Wang and M. Franklin, Techniques for performing highly accurate data value prediction, *Microprocessors and Microsystems* **22**(November 1998) 303–313.

[14] Y. Sazeides and J. E. Smith, The predictability of data values, in *Proc. of the 30th Annual International Symposium on Microarchitecture*, (Los Alamitos, IEEE Computer Society, December 1997), pp. 248–258.

[15] D. Grunwald, A. Klauser, S. Manner and A. Plezskun, Confidence estimation for speculation control, in *Proc. of the 25th Annual International Symposium on Computer Architecture*, (New York, ACM, Barcelona, June 1998), pp. 122–131.

[16] B. Calder, G. Reinman and D. M. Tullsen, Selective value prediction, in *Proc. of the 26th Annual International Symposium on Computer Architecture*, (New York, ACM, Atlanta, May 1999), pp. 64–74.

[17] M. L. Pilla, P. O. A. Navaux, F. M. G. França, A. T. da Costa, B. R. Childers and M. L. Soffa, The limits of speculative trace reuse on deeply pipelined processors, in *Proc. of the 15th Symposium on Computer Architecture and High-Performance Computing*, (São Paulo, SBC, São Paulo, October 2003), pp. 36–44.
[18] J. Huang, Y. Choi and D. Lilja, Improving value prediction by exploiting both operand and output value locality, Technical Report Technical Report ARCTic 99-06, Laboratory for Advanced Research in Computing Technology and Compilers (July 1999).

[19] M. L. Pilla, B. R. Childer, A. T. da Costa, F. M. G. França and P. O. A. Navaux, A speculative trace reuse architecture with reduced hardware requirements, in Proc. of the 18th Symposium on Computer Architecture and High-Performance Computing, eds. A. F. de Souza, R. Buyya and W. M. Jr. (Los Alamitos, IEEE Computer Society, Ouro Preto, October 2006), pp. 47–54.

[20] M. L. Pilla, B. R. Childer, A. T. da Costa, F. M. G. França and P. O. A. Navaux, Limits for a feasible speculative trace reuse implementation, International Journal of High Performance Systems Architecture 1(April 2007) 69–76.

[21] C.-H. Liao and J.-J. Shieh, Exploiting speculative value reuse using value prediction, in Proc. of the 7th Asia-Pacific Conference on Computer Systems Architecture, (Australian Computer Society, Inc., Melbourne, 2002), pp. 101–108.

[22] T. Koushiro, T. Sato and I. Arita, A trace-level value predictor for contrail processors, SIGARCH Comput. Archit. News 31(3) (2003) 42–47.

[23] F. Pratas, G. Gaydadjievv, M. Berekovic, L. Sousa and S. Kaxiras, Low power microarchitecture with instruction reuse, in Proceedings of the 5th conference on Computing frontiers, CF ’08, (ACM, New York, NY, USA, 2008), pp. 149–158.

[24] E. Rotenberg, S. Bennett and J. E. Smith, Trace cache: a low latency approach to high bandwidth instruction fetching, in Proceedings of the 29th Annual ACM/IEEE International Symposium on Microarchitecture, MICRO 29, (IEEE Computer Society, Washington, DC, USA, 1996), pp. 24–35.

[25] T. Tsumura, I. Suzuki, Y. Ikeuchi, H. Matsuo, H. Nakashima and Y. Nakashima, Design and evaluation of an auto-memoization processor, in Parallel and Distributed Computing and Networks, ed. H. Burkhart (IASTED/ACTA Press, 2007), pp. 230–235.

[26] R. Oda, T. Yamada, T. Ikeyama, T. Tsumura, H. Matsuo and Y. Nakashima, Input entry integration for an auto-memoization processor, in ICNC, (IEEE Computer Society, 2011), pp. 179–185.

[27] Y.-Y. Tsai and C.-H. Chen, Energy-efficient trace reuse cache for embedded processors, Very Large Scale Integration (VLSI) Systems, IEEE Transactions on 19(Sept. 2011) 1681–1694.

[28] A. Rahimi, L. Benini and R. Gupta, Spatial memoization: Concurrent instruction reuse to correct timing errors in simd architectures, Circuits and Systems II: Express Briefs, IEEE Transactions on 60(Dec 2013) 847–851.

[29] A. Rahimi, L. Benini and R. K. Gupta, Temporal memoization for energy-efficient timing error recovery in gpgpus, in Proceedings of the Conference on Design, Automation & Test in Europe, DATE ’14, (European Design and Automation Association, 3001 Leuven, Belgium, 2014), pp. 100:1–100:6.

[30] D. C. Burger and T. M. Austin, The Simplescalar Tool Set, version 2.0, Technical Report CS-TR-1997-1342, University of Wisconsin (Madison, 1997).

[31] S. Thoziyoor, N. Muralimanohar, J. H. Ahn and N. P. Jouppi, CACTI 5.1, Tech. Rep. HPL-2008-20, HP Laboratories (2008).

[32] Proc. of the 9th International Conference on Parallel Architectures and Compilation Techniques (Los Alamitos, IEEE Computer Society, Philadelphia, October 2000).

[33] Proc. of the 30th Annual International Symposium on Microarchitecture (Los Alamitos, IEEE Computer Society, December 1997).