ABSTRACT

The impending termination of Moore’s law motivates the search for new forms of computing to continue the performance scaling we have grown accustomed to. Among the many emerging Post-Moore computing candidates, perhaps none is as salient as the Field-Programmable Gate Array (FPGA), which offers the means of specializing and customizing the hardware to the computation at hand.

In this work, we design a custom FPGA-based accelerator for a computational fluid dynamics (CFD) code. Unlike prior work—which often focuses on accelerating small kernels—we target the entire Poisson solver on unstructured meshes based on the high-fidelity spectral element method (SEM) used in modern state-of-the-art CFD systems. We model our accelerator using an analytical performance model based on the I/O cost of the algorithm. We empirically evaluate our accelerator on a state-of-the-art Intel Stratix 10 FPGA in terms of performance and power consumption and contrast it against existing solutions on general-purpose processors (CPUs). Finally, we propose a data movement-reducing technique which often focuses on accelerating small kernels—we target the entire Poisson solver on unstructured meshes based on the high-fidelity spectral element method (SEM) used in modern state-of-the-art CFD systems. We model our accelerator using an analytical performance model based on the I/O cost of the algorithm. We empirically evaluate our accelerator on a state-of-the-art Intel Stratix 10 FPGA in terms of performance and power consumption and contrast it against existing solutions on general-purpose processors (CPUs). Finally, we propose a data movement-reducing technique which yields significant (700+ Gflop/s) single-precision performance and an upwards of 2x reduction in runtime for the local evaluation of the Laplace operator.

We end the paper by discussing the challenges and opportunities of using reconfigurable architecture in the future, particularly in the light of emerging (not yet available) technologies.

CCS CONCEPTS

- Hardware → Hardware accelerators;
- Computer systems organization → Reconfigurable computing;
- Mathematics of computing → Solvers;
- Computing methodologies → Massively parallel and high-performance simulations.

KEYWORDS

Spectral element method, Field-programmable gate array, Conjugate gradient method, High-level synthesis

1 INTRODUCTION

The end of Dennard’s scaling [25] and the impending termination of Moore’s law [48] is today forcing researchers to actively search for alternative hardware solutions. Several new and intrusive so-called Post-Moore technologies are emerging, including, for example, neuromorphic- or quantum-computing [20, 45]. Unfortunately, many of these are either very niched (e.g., neuromorphic computing) or nonviable for the foreseeable future (e.g., quantum computing). There is, however, one type of post-Moore technology [47] that preserves the most salient properties of the general-purpose computers that we have grown used to, while at the same time offering remedies to overcome the performance- and memory-bottlenecks of the former: the reconfigurable architecture.

Reconfigurable architectures, such as Field-Programmable Gate Arrays (FPGAs) or Coarse-Grained Reconfigurable Architectures (CGRAs) [41], are systems that aspire to provide some form of silicon plasticity and can thus counter the end of Moore’s law—we do not need more transistors; instead, we need to re-purpose the ones we have and specialize them to the application at hand. Reconfigurable systems can also overcome the expensive von Neumann bottleneck (which can incur a near three-orders-magnitude energy consumption overhead inside a CPU [25]) by spatially map the computation without the need for instruction decoding or unnecessary (register-to-register) data transfers.

Today, a large fraction of scientific applications are bound by data movement [21, 34]. Data movement has (historically) been more expensive for several reasons: (i) external memory bandwidth is growing at a slower pace compared to computation, and (ii) the sheer amount of data is increasing in volume. At the same time, emerging technologies such as 3D stacking [49] can be expected to alleviate the impact of data movement. To remedy the cost of data movement, there is thus a dire need to shift towards a more data movement-centric view on optimizations e.g. [32, 33], and it is imperative to model, understand, and optimize for the data movement bounds in which target applications operate. Among the many application domains that suffer from the consequences
of said imbalance in data movement capabilities is computational fluid dynamics (CFD) [46].

This work investigates the opportunities and challenges for accelerating CFD using modern reconfigurable architectures and honoring, in particular, the data movement aspects of said computation. We focus on the spectral element method (SEM) [14], which is a high-order method used in state-of-the-art, high-fidelity CFD solvers such as Nek5000 [18] and (the recent) Neko [23]. While prior works have shown FPGAs to outperform CPUs targeting both single- and double-precision, we propose an algorithm on FPGAs that trades more compute for less memory operations to alleviate the memory-boundness by computing geometric factors on the fly,

- We develop a performance and cost model for generic I/O data movement for our solver,
- We empirically evaluate the performance, the area, and the power-consuming properties of our accelerator design and position it against existing CPUs, and
- We reveal new opportunities and challenges for using reconfigurable systems in CFD applications in the future.

2 FIELD-PROGRAMMABLE GATE ARRAYS

A Field-Programmable Gate Array [31] is a type of programmable logic device whose logical functionality is (unlike, for example, a general-purpose CPU) flexible after it has been manufactured. This is achieved by providing hundreds of thousands of reconfigurable look-up tables (LUTs), onto which logic can be dynamically mapped. The amount of LUTs that are occupied by a particular hardware design is called logic utilization. Connectivity between LUTs is provided by a highly reconfigurable and versatile routing network. The flexible interconnect and LUTs are what made FPGAs an attractive vehicle for developing and testing new hardware. However, compared to ASIC designs, FPGAs often run at an order of magnitude lower frequency (e.g., often in the range 100-500 MHz contra 3-4 GHz of CPUs). Early FPGAs only had LUTs and a frequency lower by an order of magnitude (e.g., often in the range 100-500 MHz). Early FPGAs only had LUTs and a frequency lower by an order of magnitude (e.g., often in the range 100-500 MHz).

Using FPGAs has historically been a very tedious and complex exercise that came with a steep learning curve. Complex EDA tools were often used, and designs were described in low-level hardware description languages, such as VHDL or Verilog. In the early 2010s, the increased maturity in High-Level Synthesis (HLS) facilitated a greater adoption and research of applying FPGAs for HPC. HLS tools enabled the use of abstract programming languages to describe hardware. Today, HLS tools exist for several programming languages and parallel models, such as C/C++ [10, 38], OpenCL [12], OpenMP [39], CUDA [37], and even Java [3]. In this particular study, we use HLS as a method for creating a custom accelerator for the spectral element method.

3 THE SPECTRAL ELEMENT METHOD

The spectral element method has been widely acclaimed for its accuracy and scalability. In this section, we will briefly cover the algorithmic aspects of SEM and how we use it to discretize the Poisson equation in particular. Since the computation of the pressure in incompressible flow corresponds to the Poisson equation, and as it is the main source of stiffness, it frequently dominates the compute time of solvers such as Nek5000 and its successors NekRS [17] and Neko. By solving the Poisson equation we, therefore, capture the core of the entire solver. The Poisson equation with homogeneous zero boundary conditions on a domain $\Omega$ can be written as

$$\nabla^2 u = f, \quad u \in \Omega, \quad u = 0, \quad u \in \partial\Omega. \quad (1)$$

To discretize the system with SEM we introduce the weak form of the Poisson equation; find $u \in V \subset H^1_0$ s.t.

$$\int_\Omega \nabla u \nabla v d\Omega = \int_\Omega f v d\Omega, \quad \forall v \in V. \quad (2)$$

As SEM is a finite element method with high order basis functions we start our discretization by decomposing the domain $\Omega$ into $E$ non-overlapping elements $\Omega = \bigcup_{e}^E \Omega_e$. We then approximate the solution by instead of using the continuous space $V$ we use a discretized space $V^N$ on a reference element with basis functions $l_i$. For basis functions, we use the $N$th order Legendre polynomials $L_N$ interpolated on the Gauss-Lobatto-Legendre (GLL) quadrature points $\xi_i$. The number of GLL points corresponds with the polynomial order as $N + 1$. With these basis functions, the local solution $u^e$ on a hexahedral reference element can then be expressed as a tensor product according to

$$u^e(\xi, \eta, \gamma) = \sum_{i,j,k}^N u^e_{i,j,k} l_i(\xi) l_j(\eta) l_k(\gamma) \quad (3)$$

where we have introduced the weights $u^e_{i,j,k}$ and where $\xi, \eta, \gamma$ correspond to the position in the reference element. Using this discretization we can then rewrite the weak form of the Poisson equation to the following bilinear form

$$\sum_{e}^E (\phi^e)^T D^e G^e D^e u^e = \sum_{e}^E (\phi^e)^T A^e u^e \quad (4)$$

where we introduce the tensor $G^e$ which contains the geometric data mapping the actual element to the reference element and the differential matrix $D$. Of importance for us is that forming this
system is incredibly expensive\cite{14}. It is therefore evaluated in a matrix-free fashion.

### 3.1 Matrix-Free Evaluation of $Ax$

As the entire discrete matrix shown in (4) is very expensive to form we instead split the system into a local computation of $A_L$ and communication along element boundaries. This communication is done in a gather-scatter phase and our system can then instead be described as

$$\sum_{e} (v^e)^T A^e u^e = (Q e)^T A_L Q u$$  \hspace{1cm} (5)$$

where the matrices $Q$, $Q^T$ are never explicitly formed, but only the operation they do is performed in the gather-scatter phase. With the scatter operator we also introduce the local and global representation of $u$, $u_L \equiv Q u$. Going forward we will always use the local representation $u_L$, replicating the values along element boundaries. To avoid cluttering we will drop the subscript $u_L$, as all vectors in the continued discussion will have replicated data along the element boundary. The matrix-free evaluation of the discrete system is described in depth in \cite{14} and is key to the high parallelism and scalability of SEM. Throughout this paper, when we mention Ax in the context of spectral elements we then really talk about the operation $Ax = QQ^T A_L x$ where $QQ^T$ is the gather-scatter and $A_L$ is the local evaluation of the system. In previous works only the local evaluation, $A_L x$, has been considered for FPGAs.

### 3.2 The Conjugate Gradient Method

The preconditioned conjugate gradient (CG) method is one of the most common methods to solve positive-definite linear systems. In our work, we consider the unpreconditioned system as a first step towards using FPGAs for high fidelity computational fluid dynamics. We show the pseudocode for unpreconditioned CG combined with SEM in Algorithm 1 where we denote arrays at iteration $i$ with $x^{(i)}$ and scalars with greek letters and subscript i.e. $\rho_i$. One thing to note is that since we operate on the local arrays, and the boundary values are therefore duplicated, we need to introduce the vector $c$ to perform the correct reductions. Of importance for our further analysis is the prevalence of global reductions/synchronization points on lines 8 and 11. These computations impose constraints on any implementation of CG as the computation cannot progress further until these scalars have been computed. Compared to other Krylov methods, one of the attractive features of CG is its relatively simple implementation and small memory footprint. For an overview of CG and many other iterative methods please see \cite{1}.

### 4 THEORETICAL PERFORMANCE ANALYSIS

When designing a custom accelerator, such as the SEM solver accelerator we incept in this work, it is crucial to first derive a performance model for said computation. An analytical performance model can help design an accelerator in multiple ways: (i) we can easier understand the bottlenecks of the application, (ii) we can derive the theoretically observable peak performance and also use it to model future (today non-existing) architecture (e.g., \cite{26,51}, and (iii) designing an accelerator is a tough optimization problem where we want to optimize performance given certain area constraints, and a model can help driving decisions in the right direction.

Therefore, we will first develop and consider the theoretical performance of our CG solver and our SEM discretization, before going on to the implementation. We know beforehand that CG is notoriously memory-bound \cite{34}, and we aim to link our developed theory with the hardware parameters of the reconfigurable architecture. We base our model from previous findings by V. Elango et al. \cite{15} for the optimal I/O $1$ cost for CG (without preconditioning). We will extend their work to assess the I/O cost of the SEM discretization, which in turn will allow us to evaluate how memory-bound applications (in this case, SEM) can benefit from custom hardware such as FPGAs. Furthermore, we will also cover the expensive gather-scatter operation (including boundary condition masking) and its impact on performance.

#### 4.1 Machine Model

Our machine model for this work will be that of a memory machine with unlimited slow memory and with a small fast memory of size $S$. This model corresponds well to an abstract general-purpose processor (CPU), graphics processing unit (GPU), or FPGAs, where the $S$ memory corresponds to caches (CPUs/GPUs) and Block RAM (FPGAs), and the slow memory is the external DDR or High-Bandwidth Memory (HBM). This abstract machine model can then be used to reason around the I/O cost of a program. This machine model has in particular been used in conjunction with the red-blue pebble game to derive various bounds on the I/O-cost as first introduced by Hong and Kung \cite{24}. As CG is primarily bound by data movement, minimizing the I/O cost is at the core of our optimization process. In our work, we will use previous results obtained regarding the I/O cost of CG, to optimize and evaluate our FPGA implementation of CG and SEM discretization.

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1 We will adopt a fairly general notion of I/O, which include any traffic outside the processing core, in particular, we focus on accesses to DRAM/External memory (the vertical I/O cost).
4.2 I/O cost for the Conjugate Gradient and Spectral Element Method

We will now go on to present our analysis of the I/O cost of SEM and unpreconditioned CG. To begin our discussion we first note that an I/O lower bound for vertical data movement of the unpreconditioned CG was obtained in the excellent work by V. Elango et al. in [15]. In their work, they presented the I/O bound for unpreconditioned CG for many processors when the problem size is much larger than the small memory. For our intents and purposes we will also consider the small memory, but focus on only one processing element and rewrite their results as the following:

After iteration $i$ of unpreconditioned CG, the I/O cost $Q$ is lower bounded by

$$Q \geq i(6n - 4S) \geq i(12n - 4S)$$

where $n$ is the vector length and $S$ is the size of the small fast memory. To understand this result further and its proof, please see section 5.2 in [15]. Of importance to our discussion is that in this particular case, V. Elango et al. considered recomputation of an array to be disallowed, and the computation of $Ax$ to be almost free with regards to data movement, meaning that the I/O cost of evaluating the discrete system $w = Ax$ is equal to the read from $x$ and the write to $w$. This is not true in the case of SEM as the computation of $Ax$ both depends on the geometric factors as well as the gather-scatter operation as we described previously. We, therefore, have several more loads and stores that we need to perform to evaluate $Ax$. As we need to load six geometric factors per point at every iteration we get that the lower bound for SEM instead would be

$$Q_{SEM} \geq i(6n + 6n - 4S) = i(12n - 4S)$$

where $n = E(N + 1)^d$ is the number of points, $E$ is the number of elements, $N$ is the polynomial order, and $d$ is the dimension of the domain. An interesting note here is that while the number of points $n = E(N + 1)^d$ holds for any current implementation of SEM, in reality, the actual number of degrees of freedom are closer to $EN^d$. Because of the matrix-free approach, several points are duplicated along element boundaries. An insight from this bound is that for further computations. This idea of trading computation for a lower I/O cost is also an interesting direction as we go forward with our implementation.

Now that we have covered the theoretical cost of our algorithm and different discretizations in general we must once again point out that it might be unfeasible to achieve an implementation close to our theoretical I/O cost (the issue of obtaining optimal schedules from lower bounds was recently discussed in [32]). While this is true we still think it is important to know what could be achieved. Without this knowledge, the evaluation of any implementation is largely based on intuition. We often showcase results in terms of how much better one is than the state-of-the-art or comparing to a roofline, but of maybe larger importance is how far away an implementation is from some theoretical optimal program. While we did not prove any lower bounds in this section we based our reasoning on previous results and we believe that this line of thought is necessary to achieve performant software on the exascale. As for the results presented in this section, we should also note that there is more to the evaluation of $Ax$ than the geometric factors, it also includes the gather-scatter operation $QQ^T$ which we have currently assigned an I/O cost of 0. The reason we have not covered it is that it does not obey the same rules as the other statements in our CG solver, because of the unstructured nature of our problem the gather-scatter operation is more similar to a graph problem, and obtaining a clear I/O bound is not trivial.

4.3 Gather-Scatter and Masking

The gather-scatter operation is responsible for summing the values across element boundaries, thus maintaining $C_0$ continuity across elements. Looking at the array $w^{(i)}$ it adds any values $w^{(i)}_{j} \in w^{(i)}$ s.t. the points that share the same position in space, $x(w^{(i)}_{j}) = x(w^{(i)})$. While the operation itself is simple, the issue comes down to that the indices connected are not necessarily aligned. Ideally, these indices could simply be summed as $Ax$ is computed in a streaming fashion. However, this is generally not possible because of the unstructured nature of SEM. Assuming that we cannot simply stream the values along element boundaries we must then load and store each element boundary value. For a discretization with polynomial order $N$, on our hexahedral elements, we have that the number of boundary values can be computed as

$$n_{gs} = n \frac{(N + 1)^3 - (N - 1)^3}{(N + 1)^3}$$

Assuming that we need to load and store each of these values this implies an I/O cost of $Q_{gs} = 2n_{gs}$ for the gather scatter operation. Overall, for $N = 7$, this leads to $Q_{gs} \approx n$. This impact is therefore not huge, but the problem is the unaligned accesses. As this is an unstructured problem we cannot guarantee any particular ordering or spatial locality of the elements in the solution vector, posing a potentially significant performance impact. The same argument can be applied for the boundary conditions, but as the number of values along the boundary grow with the surface of $\partial \Omega$ rather than the volume of $\Omega$ their impact for reasonable problem sizes is negligible ($n < n^{2/3}$). We will therefore not consider it in our performance analysis, but rather assume all elements are connected on all sides in the gather-scatter operation.

5 ACCELERATOR IMPLEMENTATION

In this section, we will present our accelerator implementation and design considerations. As our goal is to minimize the I/O cost we will continually relate the performance to our previous theoretical results and let them guide us in our design. Our implementation is made with Intel OpenCL SDK for FPGAs [12], a High-Level Synthesis Tool for Intel FPGAs. We start from our previous work
where we implemented the local $A_L x$ operation without the gather-scatter operation, in that work we also go into more detail on more practical optimization techniques [26]. For general optimization guidelines for FPGAs, see for example [13, 28]. In this work, we go on to extend our implementation of $A_L$ and implement the entire unpreconditioned CG solver on an FPGA, and focus on $N = 7$ in particular. We choose $N = 7$ as Nek5000 and its descendants are most commonly run with a polynomial orders between seven and eleven.

### 5.1 Minimizing the I/O cost

For the CG method when applied to SEM, as we show in Algorithm 1, one of the most important aspects to decrease the I/O cost is to not load any array between our synchronization points/reductions more than once. We accomplish this by loop fusion, fusing lines 5-6 and 9-11, lowering our I/O cost. However, as shown in Algorithm 1 because of the matrix-free evaluation we have introduced a vector $c$ not to count values several times when making the reductions. In addition, we calculate $x^{(i)}$ at each iteration at a cost of $3n$ and execute the gather-scatter operation costing us $Q_G$. As the gather-scatter and masking of boundary conditions operation need to finish before we start the reduction on line 7, this reduction can not be fused with the evaluation of $Ax$ and then also incurs an I/O cost as we reload $p^{(i)}$, $w^{(i)}$. Overall, using the cost from (7) with $S \gg n$ and taking $c$, the computation of $x$, as well as the new cost of the reduction at line 7 and gather-scatter into consideration, the I/O cost $Q_{Ax CG}$ of our implementation is

$$Q_{Ax CG} = (12n + 3n + 3n + 2n + 2ng) i = (20n + 2n_g) i. \quad (10)$$

As for the number of computations per iteration, the vast number of flops can be attributed to the local $A_L x$ computation totaling

$$W_{Ax} = n(12(N + 1) + 15). \quad (11)$$

For the entire solver, we then get (omitting the gather-scatter operation) that the total number of flops is

$$W_{CG} = n(12(N + 1) + 25). \quad (12)$$

However, looking at the results from equation (8) we see that decreasing the I/O cost of $Ax$ can decrease the total I/O cost tremendously. As we precompute $G$ to then compute $Ax$, we could therefore reduce the I/O cost of $A_L$ by recomputing $G$ directly from the information stored in the mesh at each iteration instead. As the geometric factors are only dependent on the mesh, we could tremendously decrease the I/O cost as only eight values (compared to $6(N + 1)^3$ would then be needed per element. We will refer to this idea of recomputing values on the fly to obtain a lower I/O cost as rematerialization as the principles behind it are similar to the compiler technique with the same name [7]. For the computation of $G$ though, we need to compute the Jacobian inverse, $J^{-1}$, and as this involves division the performance penalties are large. However, we can limit ourselves to only precompute $J^{-1}$ and computing $G$ on the fly otherwise. This means that we only need to load $J^{-1}$ instead of the six geometric factors leading to an I/O cost of $n$ instead of $6n$ for the computation of $Ax$ and a total cost of

$$Q_{CG Remat} = (7n + 3n + 3n + 2n + 2n_g) i = (15n + 2n_g) i. \quad (13)$$

This causes the number of computations to increase tremendously though. We should also note that in our implementation we limit ourselves to meshes with hexahedral elements that are not curved but only linearly deformed. For more general meshes with curved elements, rematerialization would be even more expensive. For the whole CG solver we now instead have (omitting computations that take place less than $n/(N + 1)$ times)

$$W_{CG Remat} \approx n(30(N + 1) + 106). \quad (14)$$

For $N = 8$ we then have a more than 3-fold increase in the number of computations compared to (12). However, we should note that this is a rather naive approach and there may be algorithmic improvements that alleviate the increase in floating point operations partially. As the amount of computation necessary increases, we expect that rematerialization can be a potential alternative when the machine imbalance is large. As the operational intensity for $A_L x$ increases to $I = (30(N + 1) + 96)/3 \implies I = 112$ flop/word for $N = 7$ compared to $I = (12(7 + 1) + 15)/8 = 13.8$ flop/word for the original version. We can then clearly see that this operation is only relevant when the amount of computing power compared to the bandwidth is large. As recent Intel FPGAs such as the Intel Stratix 10 have tremendous computing power for single-precision computations we believe that rematerialization may be beneficial for this FPGA when running the solver with FP32.

### 5.2 Maximizing Memory Bandwidth

To utilize the external memory bandwidth as efficiently as possible, we manually place the different arrays on different DRAM memory banks. This enables us to saturate the memory ports to each bank as the local computations in $A_L x$ as well as all the vector additions and reductions have a high degree of spatial locality, enabling large coalesced accesses to DRAM each cycle. There is an issue of balancing the arrays between the memory banks to enable complete utilization though. As for the operation $A_L x$, we can easily balance the 8 arrays among the memory banks between the 4 banks, but as the reductions and vector operations in the solver cannot be as easily split between the different memory banks we cannot saturate the entire memory bandwidth. By examining the algorithm and carefully placing all the vectors on suitable memory banks we expect to achieve 62% of the theoretical bandwidth $\beta$ for the original formulation and 55% for the rematerialization formulation.

As for the nonaligned nature of the gather-scatter operation, this poses a severe problem. The current code structure makes a nonaligned load and store for each boundary value and can thus only utilize a fraction of the global memory bandwidth. As we are mimicking the code structure of previous GPU and CPU implementations this means that we need to execute $2n_g$ unaligned loads and stores. Related work [35] evaluating fully random access patterns with nonaligned loads and stores has shown a performance of around 60M transactions per second per DDR memory bank on the Stratix 10 architecture, corresponding to around 5 clock cycles per pair of read and write operations relative to the 300MHz of the memory interface.

In the gather-scatter operation for SEM, the pattern is not fully random, but also not strictly pairwise, as multiple reads have to be completed before the sums are written back to the respective locations. This slight non-randomness means that roughly 1/3 of the
loads and stores are aligned in memory and can be coalesced. For fully random accesses we observe that it takes around 3 cycles per read/write, but as one-third of the loads and stores are aligned, we can load eight values at the time one-third of the time leading to that it only takes $3 \cdot (2/3 \cdot 1/(3 \cdot 8)) = 2.125$ cycles per load/store operation. However, this difference compared to aligned accesses still greatly impacts the runtime of the kernel and assuming we have a bandwidth of $\beta_{eff}$ words every clock cycle for the rest of the solver this means that our effective utilization of only one value per every 2.125 cycles in the gather-scatter phase can have a large impact. We, therefore, introduce a model parameter $\beta_{gs}$ which is the number of words per cycle loaded in the gather-scatter phase. The modeled computation time can then be expressed as the following for a CG implementation with I/O cost $Q_{CG}$

$$T_C = \frac{Q_{CG}}{\beta_{eff}} + \frac{2n_{gs}}{\beta_{gs}}. \quad (15)$$

This goes to show how impactful the gather-scatter is if we cannot make aligned loads and stores on the FPGA. As the bandwidth $\beta_{gs}$ is not affected by word length, this also implies that the performance benefits of moving to lower precision because of the larger $\beta$ might not be as significant as one might expect.

6 EXPERIMENTAL SETUP

For our measurements, we used the Noctua Cluster at Paderborn Center for High-Performance Computing. In particular, we used Bittware 520N cards equipped with an Intel Stratix 2800 GX FPGAs and 4 banks of DDR-4 memory clocked at 300 MHz and with a memory interface of 512 bits each, giving us a $\beta = 32$ words/cycle for double precision and 64 for single precision. In GB/s the theoretical peak bandwidth $B$ is therefore 76.8 GB/s. For the CPU measurements we used the Beskow supercomputer at KTH, a Cray XC40 equipped with 2x 16 core Xeon E5-2698v3 Haswell CPUs clocked at 2.3 GHz per node. The DRAM bandwidth has previously been measured to a STREAM Triad bandwidth of 90 GB/s giving us a $\beta \approx 5$ words/cycle for double precision and 10 for single precision. We will use the clock frequency of 2.3GHz for our results, but it should be noted that there may be a slight variation because of Intel Turbo Boost technology. For the measurements, we parallelized the code with MPI over all 32 cores. For both the FPGA and CPU measurements, we made use of the pre-release of the spectral element framework Neko[23]. For the FPGA we use Intel OpenCL SDK version 20.2 and Quartus Prime version 19.4 as well as the GNU compiler version 10.2.0. To interface with Fortran, we utilized CLFORTRAN developed by Company for Advanced Supercomputing Solutions[9]. We have also made our implementation available online\(^3\). For the Haswell CPUs, we used the Intel Compiler version 19.1.1.217 and cray-mpich version 7.7.16. We also made performance and power measurements on a Marvell ThunderX2 (TX2) with 32 cores clocked at 2.2GHz at the FDC Center for High Performance Computing. For the TX2 we used GCC 9.2.8 and obtained a STREAM Triad bandwidth of $B = 108$ GB/s. For the power measurements on the TX2, we used the Marvell tx2mon kernel module.\(^3\). For the FPGA power measurements, we used Bittware provided MMD functions that can be accessed through an API in OpenCL. We were unable to make any power measurements on the Cray XC40 nodes.

To assess the performance, we solved the Poisson equation on a cubic domain for different numbers of elements (128-32768). To preserve the generality of the code for different meshes, we did not make any assumptions on the geometry other than that we only had linear deformations for the rematerialization.

7 RESULTS

In this section, we will use our analytical bounds and modeled performance to assess our FPGA implementation of SEM. We will also consider a CPU baseline in Neko and use our performance model from [23] to contrast our FPGA performance with a state-of-the-art CPU implementation.

7.1 $A_L x$ with Rematerialization

In our optimization process, we suggested computing the geometric factors on the fly if the amount of computing power is large. For our FPGA we projected that this could yield a performance improvement and lower runtime for single precision and we show the raw performance numbers in Figure 1. We greatly increase the performance compared to previous implementations and expect to reach even higher if we can increase the clock frequency of the kernel. With regards to total runtime, the computation with rematerialization performs around 2x faster than the original version and requires around 33% fewer cycles to make the computation for inputs larger than 2048 elements. We expect that this optimization can also be of benefit for other similar discretizations and for computing units with a high machine imbalance. The Haswell CPU does not have a large enough amount of compute for this to be beneficial though. Of note for our FPGA is that we can saturate the available memory bandwidth for double-precision much earlier than for single-precision, something that was also noted in our previous work and shown in the appendix to [26].

\(^3\)https://github.com/ExtremeFLOW/poisson_fpga

\(^3\)https://github.com/Marvell-SPIU/tx2mon

| Version       | $f_{max}$ (MHz) | Logic Util. (%) | BRAMs (%) | DSPs (%) |
|---------------|-----------------|-----------------|-----------|----------|
| FP32-A_L x Remat. | 191             | 34              | 40        | 71       |
| FP32-A_L x      | 150             | 29              | 43        | 34       |
| FP64-A_L x      | 274             | 67              | 42        | 41       |
| FP32-CG Remat.  | 156             | 32              | 55        | 74       |
| FP32-CG         | 292             | 30              | 39        | 28       |
| FP64-CG         | 204             | 39              | 52        | 35       |

Table 1: Synthesis results for our designed accelerators in terms of operating frequency ($f_{max}$), logic utilization, on-chip storage (BRAM), and compute resources (DSPs). Note that the HLS tool and its backed was unable to increase the $f_{max}$ for some of the kernels and that further performance can be gained by manually reducing the critical path. Notice the increased DSP utilization for the rematerialized versions.
when making single-precision computations compared to double-

Table 2: The observed contra modeled external bandwidth in words/cycle as experienced by our SEM-based accelerator on both the solver and the gather-scatter phase.

| Version            | $\beta_{eff}$ | Model $\beta_{eff}$ | $\beta_{gs}$ | Model $\beta_{gs}$ |
|--------------------|---------------|---------------------|--------------|---------------------|
| FP32-CG-Remat.     | 21.6          | 35                  | 0.474        | 0.47               |
| FP32-CG            | 22.4          | 40                  | 0.54         | 0.47               |
| FP64-CG            | 16            | 20                  | 0.53         | 0.47               |

Figure 1: Performance for the $A_Lx$ kernel in FP64, FP32, and our new variation where we rematerialize the geometric factors. On the left, we show the raw performance in Gflop/s, and on the right, we show the number of points in the result vector, $w = A_Lx$, computed per second.

7.2 Solver Performance

For the entire unpreconditioned CG solver with our SEM discretization we see in Fig. 2 that the performance gain made from the new $A_Lx$ kernel with rematerialization of the geometric factors lead to potentially higher performance for single-precision, however, our implementation clocked in at a quite low frequency 156MHz, hence the lower raw numbers compared to the achieved performance for only the $A_Lx$ kernel. Comparing the FPGA, Haswell, and the TX2 we see that the FPGA still has ways to go before competing with the two different CPUs, in particular because of the suboptimal gather-scatter. While the gather-scatter is the main difference, the memory system is also an important aspect. We should point out that we do compare one FPGA with one XC40 node, as the main memory system is a deciding factor of the performance. As the XC40 node’s total memory bandwidth was measured to, 90GB/s, it is also no surprise that it beats the FPGA. For the TX2 this is even more amplified as the STREAM bandwidth was measured to 108GB/s. However, it would appear the GCC compiler does not produce as efficient code for the TX2 as the intel compiler does for the Haswell. On the XC40 we get an exactly 2x performance increase when making single-precision computations compared to double-precision. On the TX2 the performance difference is much more modest, implying that it does not fully saturate the bandwidth. Another aspect we should mention is that our focus in this article is on large problem sizes, for CPUs the best performance is achieved when the potential data reuse in the cache is high, i.e. $S$ is comparably large compared to $n$. In the domain when $n \gg S$ we have that the FPGA performs $5\times$ worse than the Haswell node, but more than $6\times$ better than one Haswell core. We expect that the performance for large problem sizes will be even higher for e.g. GPUs with HBM2 than both our CPU and FPGA platforms. Looking at smaller problem sizes per FPGA may be an interesting domain to explore in the future as the FPGA enables us to completely control the usage of on-chip BRAM.

Normalizing the CPU and FPGAs with regard to frequency we see that the FPGA is comparable or better than the CPUs per cycle (Fig. 3) and that the rematerialization performs better than the original single-precision implementation. While it is unrealistic that the CPU and FPGA will run at the same frequency, normalizing the performance with regards to frequency makes it easier to compare FPGA versions with varying frequency. In the plot, we show the measured performance, as well as the modeled performance for each architecture and implementation by combining equations (7) with the maximal bandwidth $\beta$ for each architecture. For the rematerialized version we use equation (13) for the I/O cost and assess the theoretical limit with equation (8) and $n_A = n$. However, as can be seen, is that because of its higher frequency and cache, the CPU implementations are not at all as impacted by the fact that the gather-scatter kernel is limited to very few loads and stores per cycle. The relative impact compared to $\beta$ is not as large as it is for the FPGA. In addition, the cache exploits potential spatial locality that can be used. As for the modeled performance, we are within 10% of the measured performance for all versions on the FPGA and within 2% for the Haswell CPU. For the whole solver we achieved an effective bandwidth of $90 - 100\%$ of STREAM on Haswell, $60\%$ on the TX2, but significantly lower as can be seen in Table 2 on the FPGA.

Overall though, the FPGA performance model as shown in Fig. 3 is likely a bit too good to be true. Looking at Table 2 we see that
the performance model with our expected values of \( \beta_{\text{eff}} \) and \( \beta_{\text{gs}} \) overshoot and undershoot their values respectively. In particular, our utilization of the global memory bandwidth is worse than we suggested in subsection 5.2. The gather-scatter operation seems to perform slightly better than expected though, compensating for the rest of the solver. All-in-all the measured results still confirm our analysis that the gather-scatter operation is incredibly expensive on FPGAs in its current form. If we could utilize the DRAM bandwidth more efficiently for the gather-scatter and decrease the I/O cost of the SEM-CG closer to the limit presented in (8), the performance could increase tremendously.

7.3 Resource Utilization and Power Consumption

The last thing to note is the resource utilization for the different designs. Inspecting Table 1 we see how the resource consumption varies depending on the use of double or single-precision arithmetic. As the Intel Stratix 10 FPGA has DSP blocks tailored to single-precision these results show how this translates to a lot more efficient hardware. Another aspect we must also consider is the relation between a single kernel on the FPGA and synthesizing the whole Poisson solver. For the \( A_{X} \) we can obtain very high performance and use a lot of resources, but to route it and use it in the entire CG solver, there are challenges as we need to decrease the resources necessary for the \( A_{X} \) kernel to obtain a functioning design. One approach would be to use multiple FPGAs for different parts of the solver but as off-chip bandwidth is slower than on-chip this would in reality cripple the performance. Another aspect of these designs is the highly varying frequency. It is possible to increase it, but it is a time-consuming process. Another aspect we saw was that more complex designs could also sometimes malfunction for completely unrelated reasons. The CG version with rematerialization for multiple designs therefore often performed incorrect reductions, even if we only changed the evaluation of \( A_{X} \). This also points to that while HLS makes FPGA programming easier, the reliability and design considerations necessary when using FPGAs are still large. While plenty of work goes on to show good performance of FPGAs for specific kernels for certain applications we in this work showcase that the step from a single high-performing important kernel to a whole application is considerable.

On the bright side, inspecting Table 3, we measure a mere 70-80 Watt of power consumption for our FPGA accelerator, which is considerably less than current CPUs and GPUs. However, it should be noted that even though the power consumption was lower, still the Flop/J is not yet on par with the TX2 we compare against. If the power consumption remains constant though as the gather-scatter operation is improved we expect our FPGA to outperform CPUs in this regard.

8 OPPORTUNITIES AND CHALLENGES

In this section, we will discuss the different hurdles and opportunities we have uncovered as we made this first initial implementation of SEM on FPGAs.

8.1 Memory Bandwidth

As can be seen, is that even as we minimize the I/O cost the other factor that goes into the runtime is the available memory bandwidth \( \beta \). Even if the gather-scatter phase would not be our performance bottleneck, the low memory bandwidth of current FPGAs poses a challenge, and HBM2, recently available for Intel and Xilinx FPGAs, is key for FPGAs to compete for this type of application when the problem size is large. Another complementary challenge is that the memory controller does not make good use of interleaved memory and we need to place it manually on the memory banks[50]. With manual interleaving or partitioning to 32 banks of HBM2-enabled FPGAs, the gather-scatter phase might become up to 32x faster than the current version with a single bank of DDR memory. In addition, our measurements show how the low frequency of the FPGA makes the impact of non-aligned reads and writes even more detrimental than for CPUs with a higher frequency and larger cache.

Future opportunities: The emerging availability of high-bandwidth memory on FPGAs could change the game for FPGAs, but the main challenge is how to distribute data across the many channels on these devices.

8.2 On and Off-chip Memory control

An opportunity that FPGAs offer is the unmatched control of the memory layout, both in DRAM or HBM, but also on-chip memory. Currently, our FPGA implementation runs similar to a GPU with one PE per FPGA, however, one may consider novel approaches where we parallelize over each memory bank instead, treating one connection to the global memory as one PE. One may argue that the single largest benefit of FPGAs is the free control over on-chip BRAM. It is therefore possible that decreasing the problem size so that all arrays can fit into BRAM and use multiple FPGAs as a way forward for higher performance. BRAM is also the key to
achieving higher performance for the gather scatter kernel. As it in essence is a graph computation many of the methods applied to graph processing on FPGAs can be applied on the gather-scatter operation\[4\]. In particular, by pre-partitioning the domain into suitable chunks that fit into BRAM we expect that the gather-scatter performance can increase tremendously. For this, we expect that partitioning the elements with parMETIS or similar \[27\] can be the key to make the decomposition performant. Alternatively, specific sorting strategies can be employed to increase and exploit the locality in the gather-scatter phase, as discussed by Barrio et al. \[2\]. With this type of improvement in place, we expect that the gather-scatter bottleneck could be alleviated.

**Future opportunity:** By re-partitioning the gather-scatter operation into domain chunks that fit into BRAM, which will be more amenable in emerging 3D stacked high-storage chips, we hypothesize that future emerging reconfigurable systems will overcome the current gather-scatter bottleneck that we found through this paper.

### 8.3 Synchronization Points

A challenge that arises because of the structure of the CG method is the synchronization points in the form of global reductions that we mentioned earlier. One aspect of FPGAs often praised is the unique opportunity to utilize available silicon efficiently. Synchronization points by their very nature pose a large issue for this notion as they essentially form a barrier that blocks us from using the entire chip at once. For example, in our case, the resource allocated to \(A_{L\times x}\) are unused more than half of the time because of the synchronization points. As GPUs and CPUs essentially implement very many small kernels an open question is whether FPGAs are suited for compute-heavy tasks with synchronization points. While our work implies that this might be a fundamental issue currently, we can not rule out that with the advent of 3D stacked BRAM and/or faster configuration times that FPGAs will not form serious contenders to other architectures even when synchronization points and large input sizes are considered.

**Future opportunity:** Synchronization points effectively hinder us from using the whole FPGA at once and multi-contexting on FPGAs is today very expensive, as reconfiguring an FPGA takes orders of seconds. With future 3D stacking \[11\], we believe that multiple contexts can be held on-chip, and new contexts can be loaded on the order of microseconds (or less), which could open up new opportunities for remedying the issue of global reductions and synchronization points that are essential in many modern iterative solvers.

### 8.4 HLS and FPGA workflow

What is clear from a developer perspective is that while FPGAs offer many interesting features, the workflow to use them is still quite constrained and poses may be the largest challenge for FPGAs to become mainstream. Currently, while HLS is a large improvement compared to Hardware Description Languages, even
with an understanding of the hardware it is a long path to a high performing FPGA design. This may be expected, but even then the unpredictability of an FPGA design workflow with regard to resource utilization and frequency makes the design process hard and time-consuming. The implementation in this paper took the better part of June and July to implement and optimize, even with previous functioning designs for the $A_{lx}$ kernel.

**Future opportunity:** HLS is often a time-consuming effort, and results are often not available to post place&route, which can take hours. Better early models and feedback to users will be crucial in the future, or perhaps the use of more coarse-grained elements such as FPGA overlays [6] or templates [42] for faster development cycles.

### 8.5 I/O Lower bounds

While we are still far from the theoretically achievable performance, we should make clear that achieving an “optimal” solver is our goal. As we have seen in this work, there are challenges, in particular with regards to the gather-scatter kernel, but even on CPUs, we have ways to go as shown in Fig. 3. We believe that the consideration of I/O cost should be one of the main guiding principles in the application optimization process and in this work we show a path where we start from a theoretical analysis and then use this to understand and optimize our application. In this work, we primarily focused on vertical data movement, but a similar approach also needs to be made when considering multiple processes and nodes and communication between them, so-called horizontal data movement to both design algorithms and future hardware.

**Future challenge:** As machine imbalance grows, and memory-hierarchies grow deeper and more complex, it will be inevitable and crucial to consider I/O bounds to reason around and obtain higher performance.

### 8.6 Floating Point Precision

On the last note, we must also mention the performance impact of floating-point representation. It is clear that regardless if we are memory or compute-bound, decreasing the floating-point precision can increase the performance. In the case of our Haswell CPUs, we see almost exactly 2x by simply going from double to single precision. While there is work on obtaining high accuracy and performance with lower floating-point precision in various Krylov solvers, the users of scientific software are often cautious. Further studies into the actual physical implications of lowering the floating-point precision are therefore necessary. We see that FPGAs offer an unmatched testbed and opportunity for experimenting with new precision formats.

**Future opportunities:** The reduction in numerical representation can yield high-performance, more compute, and better bandwidth utilization (more values per unit BW), and using FPGAs gives the opportunity to empirically evaluate the use of lower precision for future CFD codes.

### 9 RELATED WORK

Analysis of the I/O lower bound for unpreconditioned CG and various other I/O bounds were done in a series of works by V. Elango et al. [15, 16] and also combined with a roofline analysis. However, to our knowledge, we are the first to use these results to reason around the spectral element method.

Recent work on sparse matrix-vector multiplications as a building block for the conjugate gradient method has shown that an FPGA attached to one DDR4 can achieve excellent performance up to the memory roofline here [22]. However, the presented design relies on a custom component that could not have been efficiently implemented using HLS-based design methods yet. In the work of Grigoras et al., sparse matrix multiplication for the finite element method was also accelerated on FPGAs and combined with a performance model to make projections for the Nektar++ solver[19].

As for the implementation of the matrix-free evaluation of SEM on FPGAs, the core computation $A_{lx}$ has been implemented on both Xilinx and Intel FPGAs [8, 26]. However, as these works only optimize the most compute-heavy kernel, and the Xilinx work only evaluates a very high polynomial degree, many of the issues brought up in this work were largely untouched.

Another approach was implemented by Blanchard et al. [5] where they focused on the mini app CMT-bone-BE, which is a compressible flow solver, but where they optimized a similar kernel to $A_{lx}$. There, they offloaded the optimized kernel to the FPGA, achieving performance of 1.5x over one CPU core for the whole application. Their results indicate that off-chip memory bandwidth (over PCIe) quickly becomes a limiting factor.

As for an implementation using FPGAs for unstructured meshes, the closest related work has been done on the discontinuous Galerkin method for electrodynamics [29] and more recently on shallow-water simulations [30]. A flow solver based on the finite volume method was also implemented in [36].

### 10 CONCLUSION

In this paper, we have presented a thorough performance analysis of our unpreconditioned SEM solver on FPGAs. We show initial performance results and point towards a set of opportunities and challenges that exist for FPGAs for this type of application, in particular how data movement, global reductions, and floating-point precision can have a major impact on the utilization and performance of FPGAs. In future work, we also want to evaluate the impact a preconditioner would have on this application on FPGAs. We hope that our insights can be of help as we approach an even more heterogeneous exascale landscape.

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