Scheduling Optimization Techniques for Neural Network Training

Hyungjun Oh
Hanyang University
Korea
tcip15@hanyang.ac.kr

HyeongJu Kim
Hanyang University
Korea
gudwn0520@hanyang.ac.kr

Junyeol Lee
Hanyang University
Korea
shie007@hanyang.ac.kr

Jiwon Seo
Hanyang University
Korea
seojw0n@hanyang.ac.kr

ABSTRACT

Neural network training requires a large amount of computation and thus GPUs are often used for the acceleration. While they improve the performance, GPUs are underutilized during the training. This paper proposes out-of-order (ooo) backprop, an effective scheduling technique for neural network training. By exploiting the dependencies of gradient computations, ooo backprop enables to reorder their executions to make the most of the GPU resources. We show that the GPU utilization in single-GPU, data-parallel, and pipeline-parallel training can be commonly improve by applying ooo backprop and prioritizing critical operations. We propose three scheduling algorithms based on ooo backprop. For single-GPU training, we schedule with multi-stream out-of-order computation to mask the kernel launch overhead. In data-parallel training, we reorder the gradient computations to maximize the overlapping of computation and parameter communication; in pipeline-parallel training, we prioritize critical gradient computations to reduce the pipeline stalls. We evaluate our optimizations with twelve neural networks including a light-weight computer vision model (MobileNet) and large NLP models (BERT and GPT-3) with up to forty eight V100 GPUs. Our scheduling algorithms effectively improve the performance of single-GPU training as well as data- and pipeline-parallel training. Compared to the respective state of the art training systems, the throughput is substantially improved for single-GPU, data-parallel, and pipeline-parallel training.

1 INTRODUCTION

Deep neural networks (DNNs) are now widely used in many domains. Because training and running neural networks are computationally expensive, GPUs are commonly used for the acceleration. While they substantially speedup the performance, GPUs are often underutilized when running neural network tasks. At a single GPU level, many of neural network kernels have low GPU resource utilization [39, 51, 66]; at a cluster level, half of the GPUs running neural network tasks are idle, wasting their computation cycles [32].

Hardware resource utilization is not a new problem. In the 80s and 90s, the increasing transistor density and clock frequency of CPUs made it challenging to efficiently utilize CPU resources. To improve the utilization efficiency, instruction-level parallelism (ILP) had been extensively studied in both hardware and software aspects. Techniques such as instruction pipelining and out-of-order execution are proposed and applied to increase the degree of ILP and thus improve the utilization of functional units in CPUs.

Inspired by the past studies on ILP and carefully investigating DNN tasks, we propose scheduling optimizations for neural network training. Although the GPU underutilization for single- and multi-GPU DNN training is caused by different reasons, we found out that their performance can be significantly improved by scheduling their operations efficiently. We proposed three scheduling algorithms for single- and multi-GPU (data- and pipeline-parallel) training. The three algorithms, while they differ largely in details, apply the same principle of prioritizing critical operations and increasing execution concurrency to improve the GPU utilization and the training performance.

All our scheduling algorithms for single and multi-GPU training is based on our novel scheduling technique, which we call out-of-order backprop. Although existing deep learning systems perform backpropagation strictly in the reverse order of the network layout, we observed that a subset of gradient computations may be executed in an out-of-order manner. By exploiting this property, we schedule the gradient computations such that the critical ones are executed with higher priorities. For single-GPU training, out-of-order backprop helps to mask the kernel launch overhead; for data-parallel and pipeline-parallel training, the technique helps to maximize the overlapping of inter-GPU communication with gradient computations.

This paper contributes out-of-order backprop and the scheduling algorithms based on this technique. We summarize our specific contributions in the following.

Concept of out-of-order backprop. We propose out-of-order backprop as a general principle for scheduling the computations in DNN training. Exploiting the computation dependencies in the training, out-of-order backprop enables the execution of the gradient computations out of their layout order so that more critical computations are executed with higher priorities.

Scheduling algorithms for single and multi-GPU training. We designed three novel scheduling algorithms based on out-of-order backprop and the list scheduling technique. For single-GPU training, we schedule weight- and output-gradient computations in multiple streams and in an out-of-order manner. For data-parallel training, our scheduling algorithm reorders the gradient computations to maximize the overlapping of the communication and computation. For pipeline-parallel training, we prioritize critical gradient computations to reduce the pipeline stalls. All our scheduling algorithms make efficient use of gradient computation reordering (i.e., out-of-order backprop), which no prior work had exploited for both single- or multi-GPU training.

*Corresponding author and principal investigator
Implementation in real-world deep learning systems. We implement out-of-order backprop and our scheduling algorithms in TensorFlow, a widely-used deep learning system. We modified TensorFlow’s execution engine and its compiler XLA to implement our scheduling techniques; we also added an efficient support for an auxiliary GPU stream to concurrently execute a subset of gradient computations. Moreover, we implemented our scheduling algorithms in BytePS, the state of the art parameter-communication system for distributed neural network training [33].

Extensive evaluation and availability. We evaluate out-of-order backprop and the scheduling algorithms with twelve neural network models in computer vision and natural language processing. The evaluation is performed on three different GPU models, with four types of network interconnect, and on a cluster of up to forty eight GPUs. For all (single- and multi-GPU) training methods, our scheduling algorithms largely improve the performance, compared to the respective state of the art systems. For single-GPU training, our scheduling algorithm using multi-stream out-of-order computation improves the training performance by 1.03−1.58× over TensorFlow XLA; compared to Nimble, a state of the art deep learning system for distributed neural network training [33].

Figure 1: Kernel issue overhead of deep learning systems for convolution and ReLU operations in DenseNet-121.

Figure 2: Execution timeline for DenseNet-121 (Intel Xeon E5-2698, NVIDIA V100). The kernel issue overhead (top) and their actual executions on GPU (bottom) are shown.

2 GPU UNDERUTILIZATION PROBLEMS

DNN training requires a large amount of computation and GPUs are widely used for the acceleration. Although they largely speed up the training, GPUs are often underutilized during the training [32, 39, 51, 66]. Here we review the GPU underutilization problems in single- and multi-GPU training; then we describe how these problems can be commonly formulated as a common scheduling optimization problem.

Analysis for single-GPU training. In single-GPU training, the GPU underutilization is mainly caused by kernel issue/execution overhead and idling SMs (Stream Multiprocessors) during kernel executions. Let us first consider the kernel issue overhead. In deep learning systems such as TensorFlow, DNN training is represented by (implicit or explicit) computation graphs with DNN operations and their dependencies. The systems have an executor that traverses the graph and asynchronously issues the GPU kernels. If the executor’s latency of issuing the kernels is longer than their executions on GPU, this overhead may become the performance bottleneck.

In our preliminary experiments, we measured the kernel issue overhead in three systems (TensorFlow, PyTorch, and MXNet). For many DNN models, the overhead is the bottleneck of the training. Particularly, recent convolutional neural networks (CNNs), such as DenseNet or MobileNet, are largely affected by this overhead as they have many light-weight convolutions. Figure 1 shows the kernel issue overhead for DenseNet-121 [29] (on Intel Xeon E5-2698 and NVIDIA V100). For the convolutions in DenseBlock-3 and 4, their issue overhead is up to 4× larger than their execution times; even if the kernel issue overhead is completely masked, there is a 1–2μs idle time between the kernels increases. This overhead is also recently reported in other studies [36, 45].

Specifically, Figure 2 shows the (simplified) actual timeline for training DenseNet-121 in TensorFlow; part of the forward and backward computation is shown. For DenseBlock-3’s forward computation, the kernel issue overhead is masked by the previously issued kernels. However, the masking effect disappears by the end of the next DenseBlock, when the idle time between the kernels increases.

The rest of the paper is organized as follows. Section 2 reviews the existing GPU underutilization problems. Section 3 presents out-of-order backprop, our core scheduling technique. Then Section 4 and 5 describe our scheduling algorithms for single-GPU, data-parallel, and pipeline-parallel training. Section 6 explains our implementation in TensorFlow. Section 7 evaluates out-of-order backprop and our scheduling algorithms based on the technique. Section 8 discusses related work and Section 9 concludes.
As the kernel has a smaller number of thread blocks than the number that the SMs are capable of running at once, the SMs may not be fully utilized. For example, for the weight gradient kernels in DenseBlock-4 (on V100 GPU), half of the kernels run with the same configuration of 448 thread blocks. However, the SMs are capable of running 1,520 of the thread blocks and thus they are underutilized in terms of the thread block capacity. Also, consider the end of the kernel execution when its last thread blocks are scheduled. At this point, the SMs are likely to be underutilized because they are running fewer number of thread blocks than their capacity; this problem is also referred to as tail effect or tail underutilization [10, 42].

### Analysis for GPU clusters

It is reported that the utilization of GPU clusters is less than 52% for neural network tasks [32]. The low cluster utilization is caused by many factors, such as inefficiency of task scheduling or interference of tasks. The primary reason, however, is the communication overhead in data-parallel training and the pipeline stalls in model-parallel (or pipeline-parallel) training.

In data-parallel training, workers communicate to synchronize their weight parameters in each training iteration. Because the forward computation of the next iteration blocks until the parameter synchronization is completed, GPU cycles are wasted during the synchronization. It is reported that the wasted GPU cycles from the synchronization is 15–30% of the total execution time if wait-free backpropagation is applied to overlap the synchronization and gradient computation [64]. Prioritization of parameter communication in critical path [22, 31, 33, 38, 47] may further reduce the cost but still the overhead is 10–25% as our evaluation in Section 5.1 shows.

Recently, asynchronous parameter communication schemes are proposed to improve the training throughput [26, 40, 65]. However, because they may incur accuracy loss, these asynchronous schemes are less widely applied in practice [21, 34, 61].

Now let us consider model-parallel training. For large models such as GPT, cross-layer model-parallelism is commonly used, where each layer is assigned to one of working GPUs for training, which performs the layer’s forward and backward computation. Due to the computation dependency, only a subset of the GPUs perform computation at once. That is, in both forward and backward propagation, most of the GPUs are stalled waiting for the computation result from the GPUs assigned with the earlier (or later in backpropagation) layers.

To mitigate the cost of the execution stalls, pipelining of the GPU computations is further proposed [30, 43]. In pipeline-parallel training, input data (i.e. mini-batch) is split into micro-batches, which are sequentially fed to the GPUs for the concurrent executions of the GPUs. Although using micro-batches increases the number of concurrently in-use GPUs, still a substantial portion of the GPUs are idle during the training as we show in Section 7.4. Recently PipeDream proposed to train with multiple versions of weight parameters to increase the overlapping the computations of different micro-batches [30, 43]. However, this technique causes parameter staleness in a similar manner to the asynchronous communication schemes in data-parallel training, and thus it may negatively affect the learning efficiency [7, 25].

### Formulation of a common optimization problem

The GPU underutilization in single-GPU, data-parallel, and pipeline-parallel training is caused by different reasons, and thus different optimization techniques are previously proposed for them [30, 31, 36, 43]. Although the GPU underutilization in the three training methods seems to be a separate issue, they can be formulated as a same optimization problem. In all three training methods, we need to optimize for the GPU utilization and training throughput. This requires carefully scheduling the operations in the training to maximize, for example, the overlapping of the computation and communication. Commonly for the three training methods, we formulate the problem of optimizing the execution of a single forward and backward propagation as following.

\[
\begin{align*}
\minimize_{C : \mathbb{R}^{|C|}} & \quad T(F_L) + F_L \\
\text{s.t.} & \quad T(\delta O_{L+1}) = 0, (T(\delta W_i), T(\delta O_i)) \geq T(S[\delta O_{L+1}]) + S[\delta O_{L+1}], \\
& T(S[\delta O_i]) \geq T(\delta O_i) + \delta O_i, T(S[\delta W_i]) \geq T(\delta W_i) + \delta W_i, \\
& T(F_i) \geq T(S[\delta W_i]) + S[\delta W_i], T(F_i) \geq T(F_i) + F_i, \\
\end{align*}
\]

- \(F_i, \delta O_i, \delta W_i\) are i'th layer’s forward, output and weight gradient computation; they also denote their execution times.
- \(S[\delta O_i], S[\delta W_i]\) are the synchronization of \(\delta O_i, \delta W_i\). These may be no-op; e.g. \(S[\delta O_i]\) is no-op for data-parallel training.
- \(L\) is the number of layers, \(C\) is the set of all operations, i.e., \(\{F_i, \delta W_i, S[\delta W_i], ..., \}\), and \(\mathbb{R}\) is the set of real numbers.
- \(T : \mathbb{C} \rightarrow \mathbb{R}^{|C|}\) is the scheduling function that determines the start time of the operations; for example, \(T(F_L)\) is the start time of the forward computation of layer \(L\).

The goal is to find the function \(T\) that minimizes the makespan of the executions. Note that we start with the backpropagation and end with the next iteration’s forward propagation; the gradient computation of loss \(\langle \delta O_{L+1}\rangle\) is scheduled at time zero and the completion time of the last layer’s forward computation \(T(F_L)\) is minimized.

This is a variant of job shop scheduling problem [18], which is hard to solve accurately [15, 27]. Heuristic algorithms such as list scheduling [9] or HEFT [58] are generally used to find a good solution that satisfies the constraints. We show in Section 4 and 5 that our algorithm based on the list scheduling technique [9] can find optimized kernel schedules for all three training methods (with different prioritization schemes). Before we present the scheduling algorithms, we first describe our core scheduling technique that allows flexible scheduling of neural network operations.

### 3 Out-of-order Backprop

In forward propagation of DNN training, each layer computes the output with its input, which is the prior layer’s output. The computed outputs are stored for backpropagation. The final output is compared with the target value to compute the loss. In backpropagation, the computation is performed in the backward direction to calculate the output gradient \(\langle \delta O \rangle\) and weight gradient \(\langle \delta W \rangle\) for each layer. The computed output gradient is used to calculate the gradients in the prior layer. However, the weight gradient is not used to compute any other gradients; it is only used to update the layer’s weight parameters. This dependency is shown in Figure 3 (a).

Exploiting the dependencies of gradient computations, we propose out-of-order backprop (ooo backprop in short), which schedules
the weight gradient computations out of their layout order. In conventional backpropagation, the gradient computation and weight update are performed in the reverse order of the layers in a network. That is, the two gradient computations for a layer are completed before starting the previous layer’s gradient computations. Figure 3 (a) shows the execution of conventional backpropagation.

Out-of-order backprop decouples the gradient computation from the structure of a neural network, thus scheduling weight gradient computations and updates in a flexible manner. As a result, more critical (bottleneck-causing) computations can be scheduled with higher priorities. For example, when applied to pipeline-parallel training, ooo backprop schedules all the output gradient computations of a GPU before its weight gradient computations so that the next GPU may promptly start its computation. This is shown in Figure 3 (b). The current GPU computes $\delta O_i$ and $\delta O_{i-1}$, transferring the output to the next GPU assigned with $i-2$th and $i-3$th layers; then it computes $\delta W_i$ and $\delta W_{i-1}$ concurrently with the next GPU computing $\delta O_{i-2}$ and $\delta O_{i-3}$ (not shown).

When scheduling weight gradient computations, we need to consider both GPU utilization and memory overhead at the same time. Because the weight gradient computation of a layer requires the layer’s input and output gradient, those values must be retained in memory until the computation is completed. Our scheduling algorithms in Section 4 and 5 take this memory overhead into account and find efficient execution schedules with minimal memory overhead when applying out-of-order backprop in single- and multi-GPU training.

4 SCHEDULING FOR SINGLE-GPU TRAINING
In single-GPU training the kernel issue execution overhead and idling SMs in kernel executions cause the GPU underutilization. This section presents our multi-stream out-of-order computation that applies concurrent GPU streams and ooo backprop to improve the GPU utilization for single-GPU training.

4.1 Multi-Stream Out-Of-Order Computation
To mask the kernel execution overhead and GPU’s idle cycles, we propose to use two GPU streams, namely main-stream and sub-stream. In main-stream we allocate the operations in the critical path, i.e., output gradient computations and forward computations of all layers; we set this stream’s priority high in the GPU execution engine. In sub-stream we run weight gradient computations and weight updates. Using two GPU streams in this manner requires an additional constraint in the optimization problem in Section 2: $T(\delta W_i) + T(\delta W_j) + T(\delta W_k) \geq T_i(\delta W_i)$.

To solve this optimization problem, we use the list scheduling technique and prioritize the co-scheduling of the kernels with highest speedup when run together. Because the GPU execution engine dynamically determines the SM allocations for the kernels, it is not feasible to apply fine-grained scheduling to exactly overlap the executions of two kernels. Hence we exercise coarse-grained control and apply region-based scheduling. That is, we divide the forward and backward propagation into multiple regions with similar compute characteristics; e.g. a ResNet block can be a single region (forward and backward separately) as it consists of the same repeated convolutions. Then for each region we co-schedule the kernels that give highest speedups.

More specifically our scheduling proceeds as follows:

1. For the possible region pairs we profile their concurrent kernel runs and record the speedups over their sequential runs.
2. We sequentially schedule the main-stream kernels.
3. For the sub-stream kernels, we compute their schedulable time intervals and regions; then we assign the kernels to those regions as the schedulable candidates.
4. For each region, among its candidates we find the sub-stream kernel with the highest speedup for the main-stream kernels in the region. Then we select the region-kernel pair with the highest speedup and schedule the kernel in the region.
5. We repeat step 4 until all the sub-kernels are scheduled.

Note that the overhead of the profiling is minimal because it can be performed as part of the training and also the number of regions that we use is fairly small; in our evaluation we used eight regions for DenseNet-121. This algorithm is a variant of list scheduling, which divides the timeline into multiple regions and jointly schedules for those regions altogether. This region-based approach works well in practice because recent neural networks often have structures with similar operations such as DenseBlocks or ResNet blocks. Algorithm 1 shows the pseudocode for step 4 and 5 above.

Algorithm 1: Multi-Region Joint Scheduling

| Input: $R[1..N]$: main-stream kernel schedule split into $N$ regions, $T_{main}(R[i])$: total exec time of $R[i]$’s main-stream kernels, $T_{sub}(k, R[i])$: exec time of the sub-stream kernel $k$ in $R[i]$. |
| Output: Sub-stream’s schedule $S[1..N]$ for $N$ regions |
| 1 $S[i] = []$, now$[i] = 0$ for $i = 1, ..., N$; |
| 2 $U = \{\delta W_2, \ldots, \delta W_1\}$; $C = (R[1], ..., R[N])$; |
| 3 while $U \neq \emptyset$ do |
| 4 for each region $R[i] \in C$ do |
| 5 find $\delta W_k$ runnable at now$[i]$ with max speedup $p$ in $R[i]$ |
| 6 $tmp[i] = (\delta W_k, p)$; |
| 7 $j = \arg \max_{f(i)} f(i) = tmp[i][2]$; |
| 8 $\delta W_k, P = tmp[j]$; |
| 9 $S[j].append(\delta W_k); C.remove(\delta W_k)$; |
| 10 now$[j] \leftarrow now[j] + T_{main}(R[j])$; |
| 11 if now$[j] \geq T_{main}(R[j])$ then $C.remove(R[j])$; |
| 12 return $S[1..N]$; |

Figure 3: Execution timelines of backpropagation. The dependencies of output/weight gradient computations and weight updates ($\delta O, \delta W, U$) are shown in arrows; (a) is conventional backpropagation and (b) is out-of-order backprop.
with very little overhead using CUDA Graph Launch API. We invoked over and again. NVIDIA released CUDA Graph API [19] that supports collective launching of neural network kernels has been recently used by Nimble [36]; MXNet [3] applies a similar principle but at the framework level without using CUDA kernels. A similar technique of collectively launching neural network kernels has been recently used by Nimble [36]; MXNet [3] applies a similar principle but at the framework level without using CUDA kernels. Nimble [36]; MXNet [3] applies a similar principle but at the framework level without using CUDA kernels. We use the pre-compilation technique together with pre-compiled kernel issue overhead, we apply this technique to reduce the kernel issue overhead so that our multi-stream ooo computation (with multi-region joint scheduling) can effectively reduce the idling SMs and improve the GPU utilization. A similar technique of collectively launching neural network kernels has been recently used by Nimble [36]; MXNet [3] applies a similar principle but at the framework level without using CUDA Graph API. We use the pre-compilation technique together with pre-compiled kernel issue overhead, we apply this technique to reduce the kernel issue overhead so that our multi-stream ooo computation (with multi-region joint scheduling) can effectively reduce the idling SMs and improve the GPU utilization. A similar technique of collectively launching neural network kernels has been recently used by Nimble [36]; MXNet [3] applies a similar principle but at the framework level without using CUDA Graph API. We use the pre-compilation technique together with multi-stream ooo computation to maximize the GPU utilization.

5 SCHEDULING FOR MULTI-GPU TRAINING

In multi-GPU training, the main performance overhead is 1) parameter communication in data-parallel training and 2) pipeline stalls in pipeline-parallel training. This section describes our scheduling algorithms for multi-GPU training.

5.1 Data-Parallel Training

The optimization of data-parallel training is equivalent to the problem we defined in Section 2, if the synchronization of output gradient (\( S[\delta O_k] \)) is set to no-op with empty execution time. Like the single-GPU training case, this problem is NP hard and we propose a heuristic scheduling algorithm.

In data-parallel training, the parameter synchronization overhead (\( S[\delta W_k] \) in the problem definition) is the major performance bottleneck. Figure 4 shows an example execution timeline of data-parallel training. In conventional backpropagation (a), the parameter communication, denoted by the arrows, postpones the forward computations and results in GPU idle cycles (the dark gray boxes in the timeline). If we apply the prioritized parameter communication technique that is proposed in recent studies [22, 31, 33, 38, 47], the performance is slightly improved as shown in Figure 4 (b). The communication of \( \delta W_1 - \delta W_4 \) is prioritized over \( \delta W_5 \) (denoted by the dotted arrow), which reduces the execution time by one unit time. In addition to the communication prioritization, we can further improve the performance by prioritizing the computations in the critical path. Specifically, let us schedule the computation of \( \delta W_2 \) and \( \delta W_3 \) (in this order) after the computation of \( \delta W_1 \) as shown in Figure 4 (c). Then the communication of \( \delta W_1 \) is masked by the computation of \( \delta W_2 \) and \( \delta W_3 \). The training time is reduced by three unit times, improving the performance by 16% compared to conventional backpropagation in (a) and by 12% compared to the prioritized communication in (b). Note that we can obtain this optimal schedule by reversing the computation of \( \delta W_1 - \delta W_3 \); for this example, we can obtain another optimal schedule if we reverse the computation of \( \delta W_1 - \delta W_4 \).

To find the optimal execution schedules such as Figure 4 (c), we need to design a list scheduling algorithm and prioritize the computations in the critical path. However, since parameter synchronization is the dominant factor of the performance, we achieve (mostly) the same effect by simply advancing the gradient computations upon which the critical synchronizations depend. Thus we design a heuristic algorithm, namely reverse first-\( k \)-scheduling, that reversely orders the weight gradient computations of first \( k \) layers. Because those \( k \) layers are computed earlier in the forward propagation than the other layers, the synchronization of their weight gradients are the critical operations; hence prioritizing their gradient computations shortens the critical path and minimizes the total execution time. For example, the executions in Figure 4 (c) is equivalent to the result of applying reverse first-1 scheduling with \( k=3 \). To find the optimal \( k \), we profile the executions of the schedules with multiple \( k \) values.

Algorithm 2 describes reverse first-\( k \)-scheduling. It reorders the backpropagation portion of the training. In lines 1–2, it adjusts the value of \( k \) to satisfy the given memory constraint; function \( M() \) returns the amount of temporary memory that is used by the computation. In lines 3–5, it schedules the gradient computations from layer \( L \) down to layer 1 in the same way as conventional backpropagation (except for the weight gradient computations of layer 1 to layer \( k \) (line 4). Lastly it schedules the weight gradient computations of layer 1 to layer \( k \) in the reverse order (line 6).

![Figure 4: Data-parallel training of a neural network. Execution (a) uses conventional backpropagation; (b) prioritizes the parameter communications. Execution (c) further prioritizes the gradient computations. The dark gray box is GPU idle time.](image-url)
The optimization of pipeline-parallel training is equivalent to training with that may increase the inter-GPU communication. That is, when consecutive layers of a neural network are assigned to the same GPU to minimize inter-GPU communication overhead [30, 43]. Contrary, we further speed up pipeline-parallel training by efficiently partitioning a neural network and allocating the optimizations over micro-batches in the experimental results and see a 21% speedup. For the simplicity of the presentation, we describe in 21% speedup. For the simplicity of the presentation, we describe the total execution time is reduced from 23 to 19 unit times resulting from the communication overhead, our optimizations achieve a large performance gain over the leading edge pipeline-parallel systems (GPipe and PipeDream).

5.2 Pipeline-Parallel Training

In pipeline-parallel training, each GPU is assigned with a subset of layers and executes the computations for the assigned layers. The optimization of pipeline-parallel training is equivalent to the optimization problem in Section 2, if we set \( S[\delta W_i] \) to be no-op.

As in the other training methods, we can improve the performance of pipeline-parallel training by prioritizing the critical computations. As such, we propose gradient fast-forwarding, which prioritizes the executions of the output gradient computations over those of the weight gradient computations in the GPU's allocated layers. This way, the weight gradient computations in one GPU may overlap with the output gradient computations in the next GPU.

The technique of splitting mini-batches into micro-batches is generally used in pipeline-parallel training [30, 43]. With this technique, GPUs can concurrently compute with different micro-batches for their allocated layers. For example, GPU_1 computes with batch B_1 and hands over the output to GPU_2; then GPU_1 computes with the next micro-batch B_2, concurrently with GPU_2 working on B_1. This way, the overall GPU utilization is improved.

Moreover, this technique reduces the (additional) memory overhead. Gradient fast-forwarding, if used with the conventional layer allocation scheme, requires storing output gradients in memory for the delayed weight gradient computations. Modulo layer allocation, however, hands over each layer's output gradient to the next GPU and immediately computes its weight gradient. Because the output gradient is discarded right after this computation, it is unnecessary to store more than one output gradient in each GPU.

One drawback of modulo allocation is the increased inter-GPU communication. In our evaluation, we measured this overhead in low and high-bandwidth network. The details are discussed in Section 7.4 but the short summary is that even with the communication overhead, our optimizations achieve a large performance gain over the leading edge pipeline-parallel systems (GPipe and PipeDream).

### Algorithm 2: Reverse First-K Scheduling

**Input:** \( k \): number of layers to reschedule, \( MXM \): max memory.

**Output:** Optimized schedule \( D \)

1. \( max_k = \text{arg max}_j f(j) = M_{f, \text{softmax}} - \sum_{l=0}^{j-1} M(\delta O_l) + \sum_{l=j}^{L} M(\delta W_l) \) s.t. \( f(j) < MXM \);
2. \( k \leftarrow \min(max_k, k) \);
3. for \( i \leftarrow L \) down to 1 do
   4. if \( i > k \) then \( D.append(\delta W_i) \);
   5. \( D.append(\delta O_i) \);
5. for \( i \leftarrow 1 \) to \( k \) do \( D.append(\delta W_i) \);
7. return \( D \);

If the optimal value of \( k \) is given, Algorithm 2 effectively prioritizes the critical synchronizations. If \( k \) is too small, the synchronizations are not fully masked; if it is too large, the network bandwidth may be underutilized. With profiling the executions, we can find the optimal \( k \) that gives the fastest execution. List scheduling, on the other hand, does not need to find such optimal values but it requires the execution times of the parameter synchronizations. Because it may not be easy to estimate the synchronization time, reverse first-\( k \) scheduling is more effective and suitable in practice.

6 IMPLEMENTATION IN TENSORFLOW

We implemented our optimizations in TensorFlow (v2.4) and its optimizing compiler XLA. To implement out-of-order backprop, we eliminated the use of `tf.group` that puts the weight and output gradient computations of a layer into a single node in the computation graph. By putting them in separate nodes, we remove the unnecessary dependencies for those gradient computations.

To maximize the overlapping of computation and communication, we fixed the runtime enforcement of operation dependencies in TensorFlow. Figure 6 shows a part of an execution timeline with

![Figure 5: Pipeline-parallel training of an 8-layer neural network](image)

(a) is conventional execution, (b) applies gradient fast-forwarding, and (c) further applies modulo allocation.
computations in GPU stream $S_1$ and synchronization in stream $S_2$. When issuing $\text{Send}(\delta O_i)$ in stream $S_2$, TensorFlow enforces the dependency using CUDA event/stream APIs and simply makes it to be executed after any operation just issued in $S_1$. Because $\text{Send}(\delta O_i)$ is issued after $\delta O_{i+1}$, $\delta O_i$, and $\delta W_i$ are issued (in this order), $\text{Send}$ is forced to execute after the computation of $\delta W_i$. We fix this and make $\text{Send}$ to execute after $\delta O_i$’s computation, which makes $\text{Send}$ to overlap with $\delta W_i$’s computation.

Moreover, we implemented an efficient support for an auxiliary GPU stream in TensorFlow. Although TensorFlow has preliminary implementation for multiple GPU streams (which is disabled by default [56]), it uses much more memory compared to the single-stream executions. That is, in single-stream executions, temporary memory that is solely accessed by a kernel may be immediately reclaimed and used by other kernels as soon as the kernel is issued (before its execution finishes). However, with the (generic) multi-stream support in TensorFlow, reclaiming temporary memory in this manner is not feasible because of the complex dependencies between kernels in different streams. Rather than using the generic but expensive multi-stream support in TensorFlow, we implemented a light-weight version that supports only one additional stream (i.e., sub-stream), for running the weight gradient computations. We also assigned a separate memory allocator for the temporary memory used by the sub-stream kernels. We used NVIDIA’s event/stream APIs to enforce the dependency between the main-stream and sub-stream kernels.

Our prototype is based on TensorFlow, but all our techniques can be implemented in MXNet or PyTorch, by modifying, e.g., PyTorch’s autograd engine that dynamically constructs the backward graphs.

Table 1: Models, datasets, and evaluation setup.

| Training Method     | Model                 | Dataset     | GPU        |
|---------------------|-----------------------|-------------|------------|
| Single GPU Training | DenseNet-[121,169]    | CIFAR100    | Titan XP   |
|                     | MobileNet V3 Large    | ImageNet    | V100       |
|                     | ResNet-[50,101]       |             |            |
| Data-Parallel       | DenseNet-[121,169]    |             | Titan XP $\times 8$ |
| Training            | MobileNet V3 Large    | ImageNet    |             |
|                     | ResNet-[50,101,152]   |             | $P_{100} \times 20$ |
| Pipeline-Parallel   | RNN (16 Cell), FFNN   | IWSLT       | V100 $\times 36$ |
| Training            | BERT-[12,24,48]       | MNLI        |             |
|                     | GPT-3 (Medium)        | OpenWebText |             |

7 EVALUATION

In this section, we present a comprehensive evaluation of our scheduling algorithms. We evaluate our optimizations with twelve neural networks and five public datasets on a single and multiple GPUs. Because our optimizations do not change the semantics of neural network training, we only evaluate the training throughput and the memory overhead. The details of the evaluation are described later, but the short summary is that our algorithms with out-of-order backprop effectively improves the performance of single-GPU training as well as data- and pipeline-parallel training. Compared to the respective state of the art systems, we speed up the throughput by 1.03–1.58× for single-GPU training, by 1.10–1.27× for data-parallel training, and by 1.41–1.99× for pipeline-parallel training.

7.1 Experimental Setup

Models and datasets. Table 1 describes the twelve neural networks and five datasets that are used for the evaluation. These models are state of the art neural network models that are commonly used in computer vision and natural language processing (NLP). DenseNet-[121, 169], MobileNet, and ResNet-[50,101,152] are established CNN models in computer vision. DenseNet has growth rate as its hyperparameter (denoted by $k$); we set $k=12, 24, 32$, which are the same as those used by the authors [29]. MobileNet also has a hyperparameter, namely multiplier (denoted by $\alpha$); we use $\alpha=0.25, 0.5, 0.75, 1$, which are also the same as those used by its authors [28]. For the language processing, we used Recurrent Neural Networks (RNNs), BERT-[12,24,48], and GPT-3 (Medium) as they are the representative NLP models. We also experimented with a simple feed forward neural network (FFNN). We used public datasets that are widely used to evaluate CNNs (CIFAR100 [35] and ImageNet [48]) and language models (IWSLT [2], MNLI [59], and OpenWebText [17]).

GPUs and interconnects. We used NVIDIA Titan XP, P100, and V100 GPUs for the training as shown in Table 1. Titan XP GPUs are installed on a small cluster of eight machines. The machines have Intel Xeon E5-2620 v4 running at 2.1GHz and 64GB of DRAM. Each machine has a single Titan XP GPU connected via PCIe 3.0 x16; the machines are connected via 10Gb Ethernet. P100 GPUs are deployed on a cluster of twenty machines, each containing one P100 GPU connected via PCIe 3.0 x16; the machines have Intel Xeon E5-2640 v3 running at 2.6GHz and 32GB of DRAM. The machines are connected via 20Gb Ethernet. V100 GPUs are installed on a public cloud (Amazon AWS). The instance types for the evaluation are shown in Table 2, which summarizes the cluster settings. We used the two private clusters described earlier and two public clusters on AWS. The AWS instances have Intel Xeon E5-2686 v4 running at 2.3GHz. The instances in Pub-A cluster have 244GB of DRAM and four V100 GPUs and the instances in Pub-B cluster have 488GB DRAM and eight V100 GPUs. We used up to forty-eight V100 GPUs in Pub-B cluster and up to thirty six V100 GPUs in Pub-B cluster.

Other training settings. We train with the batch sizes that are used by the authors of the models; we also tested with the maximum batch sizes on the GPUs. For DenseNet, MobileNet, and ResNet models we set the batch size per GPU to be 32, 64, 96, and 128 for...
CIFAR100 and ImageNet [23, 28, 29]. The maximum global batch size that we used is 6,144 for ResNet-50 with 48×V100 GPUs. To evaluate BERT and GPT-3, we set the batch size to be 96 for the fine-tuning [8, 37, 49, 62]; for the pre-training, we set the batch size to be 512–1,872 for BERT and 96–216 for GPT-3, which is similar to commonly used batch size for pre-training the models [16, 24, 41, 49, 50, 52].

We trained the models with multiple optimizers (SGD, momentum, RMSProp, and Adam optimizers) and report the throughput with momentum optimizer as training with other optimizers show similar trend. For BERT and GPT, we use Adam optimizer which is used by its authors [1, 11]. To measure the training throughput, we start the training and wait a few epochs for the training to warm up. Then we measure the throughput by taking the average over ten iterations; we repeat this ten times and report the average and the standard error of the ten runs.

For the memory evaluation, we set TensorFlow’s allow_growth flag as true to compactly allocate the required memory. We used nvidia-smi to measure the memory usage; we also investigate and report the memory allocation of TensorFlow’s bfc_allocator.

### 7.2 Evaluation of Single-GPU Training

We first measured the speedup in single-GPU training brought by multi-stream out-of-order computation and pre-compiled kernel issue. As the optimizations may incur memory overhead, we also report the additional memory usage.

**Training throughput.** We measure the throughput of training DenseNet, MobileNet, and ResNet in Table 1 with CIFAR100 and ImageNet. We evaluate TensorFlow 2.4 XLA (the baseline) and XLA with our two optimizations. For comparison we also evaluate Nimble [36], a state of the art deep learning execution engine based on PyTorch’s JIT compiler; Nimble is reported to largely outperform PyTorch [46], TorchScript [55], TVM [4], and TensorRT [6].

Figure 7 shows the training throughput of the models on NVIDIA V100 normalized by those of the baseline (XLA). The numbers above the x-axis are the actual throughput (images per second). For the models and batch sizes in the figure, our optimized training (denoted by OOo-XLA) improves the throughput of XLA by 1.09–1.21× for DenseNet-121, by 1.07–1.19× for MobileNet, and by 1.03–1.06× for ResNet. The maximum performance gain by OOo-XLA over XLA is (not shown in the figure) 1.54× for DenseNet-121 (k=12 and batch=32) and 1.58× for MobileNet (α=0.25 and batch=32). Compared to Nimble, our optimized training runs faster by maximum 1.35× (DenseNet:k=12 and batch=32, not shown) and minimum 1.07× (DenseNet-121: k=24 and batch=32); Nimble ran out of memory for most of the models with 64 batches (denoted by N/A). When we examined the speedup by multi-stream ooo computation separately, it gives minimum 1–2% (ResNet-[50,101], batch=64) and maximum 15% (MobileNet: α=0.25 and batch=32, not shown) speedup over XLA with our pre-compiled kernel issue.

With 128 batch size, Nimble ran out of memory for all the tested models; XLA and OOo-XLA ran out of memory for most of the DenseNet and ResNet models. For MobileNet, OOo-XLA runs 1.04–1.09× faster than XLA with 128 batches. In Titan XP, the three systems (XLA, Nimble, and OOo-XLA) ran out of memory for all the models with 128 batch sizes; with 32 and 64 batch sizes, the performance gain of OOo-XLA is similar to that of V100.

In summary, OOo-XLA runs 1.03–1.58× faster than XLA over all evaluated GPUs and models with the average speedup of 1.18×. Compared to Nimble, OOo-XLA runs 1.0–1.55× faster in all experiments with the average speedup of 1.28×.

**Memory overhead.** In all the experiments for single-GPU training, we set the memory constraint to be 1.1× of the conventional execution; i.e., OOo-XLA may use 10% more memory for the reordered computations. For all the models, the peak memory usage is only increased by maximum 0.1%, which is the case for DenseNet-121. For this model, the weight gradient computations in DenseBlock-4 are delayed to run with the forward computations in DenseBlock-1 as shown in Figure 9. Because of the delayed weight gradient computations, the intermediate tensors need to be stored in memory.

This memory overhead is illustrated in Figure 8 which compares the memory usage of conventional backpropagation (green line) and our reordered execution (yellow line). The figure aligns the memory usage by the output gradient computations; that is, the memory usage of m at layer Li means that the execution uses temporary memory of m when computing the output gradient of Li. Due to the delayed computations, our execution uses maximum 200MB more memory than the conventional execution (in L5−L1 of the timeline). However, the peak memory is only increased by 10MB (or 0.1%) in the beginning of the backpropagation as shown in the figure. For the other models, the weight gradient computations of the last layers run concurrently with the corresponding output gradient computations, hence no additional memory is used.

---

**Figure 7:** Training throughput normalized by that of XLA for batch size 32, 64. Opt1 is pre-compiled kernel issue; Opt2 is multi-stream ooo computation. The numbers above x-axis are the actual throughput. N/A means out of memory error.

**Figure 8:** Memory usage for training DenseNet-121.
we trained the DenseNet, MobileNet, and ResNet models with 10% speedup for the two regions respectively. The kernel issue overhead is eliminated by pre-compiled scheduling regions, which are mapped to the DenseBlocks.

Discussion. The kernel issue overhead is eliminated by pre-compiled kernel issue; then multi-stream ooo computation further reduces the kernel execution overhead and the idling SMs during kernel executions. We examined the effect of the latter in more detail. Specifically we look into the training of DenseNet-121 and MobileNet where the speedup by multi-stream computation is the highest. As shown in Figure 9, the weight gradient computations in DenseBlock-1–4 are reordered and executed in sub-stream. We examine the execution of the region R2 and R5 in the figure because multi-stream computation gives the minimum (6%) and maximum (10%) speedup for the two regions respectively.

For R2, the output gradient (\(\delta O\)) kernels in DenseBlock-3 are running with the weight gradient (\(\delta W\)) kernels in DenseBlock-3. More than thirty percent of the \(\delta O\) kernels in R2 have the same number of thread blocks as the SM capacity, hence the SMs are running at their maximum thread block capacity. Hence, the performance gain by having the sub-stream kernels is limited to reducing the kernel execution overhead. When we sum up this overhead in R2, it totaled to about 5% of R2’s execution time; this is similar to the 6% speedup achieved by multi-stream computation.

In contrast, the main-stream kernels in R5 have much larger number of thread blocks than the SM’s capacity; for the sub-stream kernels (\(\delta W\) in DenseBlock-4), half the kernels run with the same 448 thread blocks even though the SMs are capable of running 1,520 of them. By running those \(\delta O\) and \(\delta W\) kernels concurrently, we provide the opportunity to make most of the SM resources and achieve 10% speedup.

7.3 Evaluation of Data-Parallel Training

Now we evaluate our reverse first-\(k\) scheduling for data-parallel training. We use three GPU clusters for the evaluation – a small cluster of 8\(\times\)Titan XP, a larger cluster of 20\(\times\)P100, and a public cloud of 48\(\times\)V100 (Pub-A of Table 2). The settings of the GPU clusters are described in Table 2. For the evaluation of data-parallel training, we trained the DenseNet, MobileNet, and ResNet models with ImageNet. We measured the performance improvement and memory overhead of reverse first-\(k\) scheduling. The baseline for this evaluation is BytePS, the state of the art parameter-communication system for distributed training [33]; BytePS is reported to be faster than other communication prioritization systems [22, 31, 33, 38, 47]. We implemented our scheduling optimizations on BytePS and measured its training throughput with and without our reverse first-\(k\) scheduling. For a subset of the experiments, we also evaluate Horovod, an efficient framework for decentralized distributed training. We do not evaluate the performance of other asynchronous training algorithms [26, 40, 65] as they change the training semantics. Note that out-of-order backprop can be used with those asynchronous training algorithms to further improve their performance.

Training throughput. The results of the evaluation for the ResNet models are shown in Figure 10: (a) is the results for Titan XP cluster, (b) is for P100 cluster, and (c) is for V100 cluster on AWS. The figure shows the training throughput with 1 to 8, 20, or 48 GPUs for each cluster.

In Titan XP cluster, our reverse first-\(k\) scheduling (denoted by OOO-BytePS) is up to 15.3% faster than BytePS and up to 89% faster than Horovod (maximum speedup for ResNet-101 on 8 GPUs). In P100 cluster, OOO-BytePS is up to 27.1% faster than BytePS and 3.5x faster than Horovod both for ResNet-101 on 20 GPUs. In V100 cluster, we achieve up to 26.5% speedup for ResNet-50 on 16 GPUs and up to 19.8% speedup for ResNet-101 on 8 GPUs. In summary, OOO-BytePS achieves 1.1–1.27× speedup over BytePS with 16–48 GPUs on P100 and V100 clusters. For smaller models (DenseNet and MobileNet), we achieved up to 10% and 5.3% speedup respectively.

Memory overhead. Our reverse first-\(k\) scheduling may increase the memory usage for delaying the k-1 weight gradient computations. However, because the memory pressure is already reduced by running the gradient computations of last \(L\)-\(k\) layers (where \(L\) is the total number of layers), reordering the computations of the first \(k\) layers does not usually increase the peak memory usage. For example, Figure 11 compares the memory overhead of the conventional execution (green line) and our optimized execution (yellow line) for ResNet-101. For our execution, first fifty five gradient computations are reversed (\(k=55\)) and thus their input tensors are retained in...
We evaluated pipeline-parallel training with NLP models—RNN, weight gradient computations are executed in-order. In all our experiments with the CNN models, the additional memory overhead by reverse first-\(k\) scheduling is less than 1% of the total memory of the conventional backpropagation execution.

**Discussion.** To understand the performance gain of reverse first-\(k\) scheduling we examine the training of ResNet-50 with 16×V100 GPUs in Pub-A cluster. The performance bottleneck is the first layer’s weight synchronization, which is required at the beginning of the forward computation. With sixteen GPUs, BytePS takes 350\(ms\) for this synchronization. Thanks to the communication prioritization, the latency is much shorter than those reported by others using similar network settings [34], but it is still substantial compared to the computation time of 380\(ms\). Our scheduling algorithm reverses first 45 layers’ weight gradient computations to overlap \(\delta W_i\)’s synchronization with the \(\delta W_2−\delta W_45\)’s computations. The execution time of \(\delta W_2−\delta W_45\) is 85\(ms\), which reduces the 350\(ms\) communication time to 265\(ms\). In addition, scheduling \(\delta W_2−\delta W_20\) early in the timeline makes it possible for their synchronization to overlap with part of the backward and forward computation, the effect of which is 65\(ms\) of more overlapping. Thus the communication overhead is reduced to 200\(ms\), achieving total 27% speedup.

### 7.4 Evaluation of Pipeline-Parallel Training

We evaluated pipeline-parallel training with NLP models—RNN, BERT-[12,24,48], and GPT-3. We evaluated their fine-tuning and pre-training. Fine-tuning is evaluated on four V100 GPUs; pre-training is evaluated on up to thirty six V100 GPUs (Pub-B in Table 2).

We measured the speedup of our two optimizations, i.e., gradient fast-forwarding and modulo allocation. The baseline of the experiments is GPipe, which is a state of the art pipeline-parallel training system. We also evaluate PipeDream [43], another leading edge pipeline-parallel training system. PipeDream, however, applies weight stashing that brings about parameter staleness and thus changes the semantics of the training. Hence we report its performance as reference points only. For a subset of the experiments, we evaluated Dapple [14], a state of the art data- and pipeline-parallel training system. We do not evaluate FTPipe [13] (another pipeline-parallel training system), as it is designed for the fine-tuning on commodity GPUs; also its published prototype failed to run in different settings than their evaluated ones [12].

#### 7.4.1 Fine-Tuning Experiments

We run the fine-tuning of RNN and BERT-24 on four V100 GPUs that are interconnected via NVLink. The following four settings are mainly evaluated: a) cross-layer model parallelism, b) GPipe, c) OOO-Pipe1 (GPipe with gradient fast-forwarding), and d) OOO-Pipe2 (OOO-Pipe1 with modulo allocation). We also report the performance of PipeDream for a subset of the experiments. We use the batch size of 1024 for RNN and 96 for BERT, which is commonly used for their fine-tuning [8, 37, 49, 62]. When applying modulo allocation for RNN, we assign \(i\)’th cell to \(\text{GPU}_j \mod 4\); for BERT-24, we assign \(i\)’th encoder to \(\text{GPU}_j \mod 4\).

Figure 12 (a) shows the results. The x-axis shows the execution a−d for RNN and BERT, and y-axis is the throughput normalized by that of the single-GPU training. The numbers on the x-axis are the actual throughput (sequences per second). For the RNN model, OOO-Pipe2 runs 1.99× faster than the baseline (GPipe); compared to (cross-layer) model parallelism, OOO-Pipe2 is 1.47× faster. For BERT-24, OOO-Pipe1 runs 1.15× faster than the baseline and together with modulo layer allocation OOO-Pipe2 is 1.59× faster. Compared to the single-GPU training of BERT-24, we achieve 3.2× speedup with four GPUs.

To better understand the performance impact of the two optimizations, we also evaluate the training of a simple feed forward neural network (FFNN) with 16 fully-connected layers. When applying the same set of optimizations, we obtain the experimental results in Figure 12 (a) denoted by FFNN. With the two optimizations OOO-Pipe2 runs 1.5× faster than the baseline. To study the effect of the two optimizations for FFNN, we illustrated the execution timelines with and without the optimizations. For simplicity we assume that all the computations take the same amount of time and the inter-GPU communication latency is negligible. We show the execution timelines for FFNN with 8 layers for the interest of space, but we report our analysis with the 16-layer FFNN. Figure 13 shows the execution timelines (of 8-layer FFNN); (a) is GPipe, (b) is OOO-Pipe1 (gradient fast-forwarding), and (c) is OOO-Pipe2 (OOO-Pipe1 with modulo allocation). The numbers denote the layer index of the computation and the subscript (A,B,C, and D) denotes the index of micro-batches. If we examine the timelines for the 16-layer FFNN, gradient fast-forwarding gives 1.22× speedup over GPipe and together with modulo allocation our execution is 1.62× faster than GPipe. Compared to these, our experimental results yield reduced speedup (1.18× and 1.5×) because of the inter-GPU communication overhead and non-uniform kernel execution times.

**Communication overhead.** We run another set of experiments to study the impact of the increased communication by modulo allocation. We trained BERT-24 on four V100 GPUs with three different interconnect networks: NVLink (50GB), PCIe 3.0 (16GB), and 10Gb Ethernet (1GB). We measured the training throughput of GPipe, OOO-Pipe2, and PipeDream. Figure 12 (b) shows the results. In all three interconnect settings, OOO-Pipe2 substantially outperforms GPipe by 70% in NVLink, by 58% in PCIe, and by 48% in 10Gb Ethernet. PipeDream applies weight stashing to train with multiple version of weight parameters, and thus the communication overhead of a small cluster is masked by the computation with older or newer parameters. In this four-GPU cluster, the communication overhead of OOO-Pipe2 seems relatively larger in low-bandwidth network. However, in a typical cluster setting for training large NLP models, where a small number of GPUs in a node are interconnected.
With eight GPUs, the transformers are all assigned to the GPUs. We evaluated three systems: GPipe, PipeDream, and OOO-Pipe2. When training the NLP models on four V100 GPUs, the maximum weak scaling and strong scaling experiments. In the weak scaling (ours). For this evaluation, we use the batch sizes of 512–1872 that give the maximum performance for each system.

**Figure 12:** Throughput of NLP models for pipeline-parallel training on 4×V100; (a) is the throughput for RNN, BERT, and FFNN normalized to that of single-GPU training, and (b) is BERT-24 with three interconnect networks. The numbers above x-axis are the actual throughput.

In high-bandwidth network and the nodes are interconnected in low-bandwidth network, the communication overhead for OOO-Pipe2 is not large, as we show in our pre-training evaluation. **Memory overhead.** Gradient fast-forwarding incurs memory overhead for storing the input tensors of the delayed computations. When training the NLP models on four V100 GPUs, the maximum memory overhead incurred by the fast-forwarding is 11% over the baseline. However, modulo allocation eliminates the memory overhead by immediately transferring and discarding the computed outputs, thus using the same amount of memory as the baseline.

### 7.4.2 Pre-Training Experiments

We evaluate the pre-training of BERT-[12,24,48] and GPT-3 (Medium, 24 decoders) on a larger cluster of 36×V100 (Pub-B in Table 2). We set the max sequence length for BERT be 128 and that for GPT-3 be 512 for the pre-training [11, 44]. We used the vocabulary size of 30,522 for the BERT models and 50,257 for GPT-3, which is commonly used for these models [37, 41, 49]. As we are interested in the scalability of the training with increasing number of GPUs, we perform both weak scaling and strong scaling experiments. In the weak scaling experiments, we train with 8–32 GPUs and with BERT-12–BERT-48. We evaluated three systems: GPipe, PipeDream, and OOO-Pipe2 (ours). For this evaluation, we use the batch sizes of 512–1872 that give the maximum performance for each system.

Figure 14(a) shows the results of the weak scaling experiments. With eight GPUs, the transformers are all assigned to the GPUs on the same machine, which are interconnected via NVLink. In this case, OOO-Pipe2 is 1.73× faster than GPipe and 1.63× faster than PipeDream. With 16 to 32 GPUs, we trained larger models (BERT-24 to BERT-48) and the speedup by OOO-Pipe2 is 41–45% over GPipe and 14–25% over PipeDream. When we increased the number of GPUs from 16 to 32, the performance gain of OOO-Pipe2 does not decrease but it either remains similar (compared to GPipe) or increases (compared to PipeDream). This demonstrates that the performance gain by modulo allocation outweighs the overhead of the increased communication for the evaluated cluster setting. For training BERT-48 in PipeDream, we set the maximum number of parameter versions to be 32 as it gives the maximum training throughput. Training with high staleness level of 32 may negatively affect the learning efficiency and slow down the convergence [7, 25].

Now we describe the strong scaling experiments for OOO-Pipe2. We trained BERT-[24,48] with 8–32 GPUs in the same way as the previous experiments. For GPT-3, the size of its last embedding layer (including the intermediate tensors) is large due to its large sequence length and vocabulary size, and thus we separately assign four GPUs to the layer, which is split in the output neuron dimension; the four GPUs compute the last word embedding and the first embedding lookup operations. Figure 14 (b) shows the experimental results. We observe that the performance of training BERT-24 and BERT-48 scales fairly well, with the total number of GPUs for the training increasing from 8 to 32; with 4× number of GPUs, the throughput for the two BERT models is increased by 2.5×. For comparison we also evaluated Dapple for the pipeline-parallel training of BERT-48 with 8 and 16 GPUs; note that Dapple is evaluated with maximum 16 GPUs [14] and their published system does not support larger GPU clusters out-of-the-box [20]. With 8 and 16 GPUs, OOO-Pipe2 is 1.47× and 1.29× faster than Dapple respectively. When we applied both data- and pipeline-parallel training to Dapple and OOO-Pipe2, the performance of the two systems similarly improved by 30–35%. However, finding the optimal hybrid-parallel training with ooo backprop is beyond the scope of this paper and we leave it as our future work. For GPT-3, we used 12 to 36 GPUs with the extra 4 GPUs for the word token embedding layer. The performance for GPT-3 scales in a limited manner because it consists of 24 transformer decoders. That is, the 24 transformers cannot be evenly assigned to 16 or 32 GPUs, hence its scalability from 8 to 16 and from 24 to 32 (transformer) GPUs is limited.

### 8 RELATED WORK

**Optimization of single-GPU training.** Kernel fusion reduces the execution overhead of short-running kernels by combining multiple consecutive kernels into a single one. The technique is applied by optimizing compilers such as XLA [4, 5, 57]. In our evaluation, we show that our optimizations can be applied to XLA to further speedup the executions of the fused kernels. The technique of pre-compiling a group of kernel issues has been recently proposed to reduce the kernel issue overhead [3, 36]. Particularly, Nimble [36] also applies multiple GPU streams for the neural network models that have parallel blocks such as Inception blocks [53] to compute those blocks in parallel. However, Nimble (and other systems supporting multiple GPU streams [45, 63]) do not concurrently execute weight and output gradient computations in an out-of-order manner as our proposed techniques.

**Optimization of data-parallel training.** Hao et al. proposed wait-free backpropagation for data-parallel training [64], which overlaps the parameter synchronization of a layer with the prior layer’s gradient computations. More recently, the technique of prioritizing parameter communication has been proposed to improve the performance by giving higher priority to the parameter communications in critical path [22, 31, 33, 38, 47]. Out-of-order backprop further reorders the critical gradient computations as well as the critical synchronizations to more efficiently overlap the gradient.
computations with their communications. Our scheduling algorithm based on out-of-order backprop largely outperforms BytePS that prioritizes the parameter communications [33].

A number of studies have proposed relaxed schemes for parameter synchronization [26, 40, 65]. For example in AD-PSGD, a worker synchronizes its parameters with only one other worker in each training iteration [40]. While these techniques reduce the synchronization overhead, they are likely to incur accuracy loss in practice [21, 61]. Our optimizations do not change the semantics of the training and thus they can be safely and generally applied without incurring accuracy loss.

Optimization of pipeline-parallel training. For the training of large neural networks that do not fit in a single GPU, pipeline-parallel training is proposed [13, 14, 30, 43]. The proposed systems commonly apply the micro-batch technique that splits a mini-batch into multiple micro-batches and pipelines the executions with those micro-batches. Our two optimizations, i.e., gradient fast-forwarding and modulo layer allocation, are applied on top of the micro-batch technique to further improve the training performance, as we show in our evaluation. PipeDream [43] and FTPipe [13] also support asynchronous pipeline-parallel training, which incurs staleness and thus change the semantics of the training in a similar manner to asynchronous data-parallel training.

9 CONCLUSION

This paper proposes out-of-order backprop, an effective scheduling technique for neural network training. By exploiting the dependencies of gradient computations, out-of-order backprop reorders weight gradient computations to speed up neural network training. We proposed optimized scheduling algorithms based on out-of-order backprop for single-GPU, data-parallel, and pipeline-parallel training. In single-GPU training, we schedule with multi-stream out-of-order computation to mask the kernel execution overhead; we also apply pre-compiled kernel issue to eliminate the kernel issue overhead. In data-parallel training, we reorder the weight gradient computations to maximize the overlapping of computation and parameter synchronizations. In pipeline-parallel training, we prioritize the execution of output gradient computations to reduce the pipeline stalls; we also apply modulo layer allocation, an optimized layer allocation policy. We implemented out-of-order backprop and all our scheduling optimizations in TensorFlow XLA and BytePS. In our evaluation with twelve neural network models, our optimizations largely outperform the respective state of the art training techniques. For single-GPU training, our optimizations outperform XLA by $1.03 \times - 1.58 \times$. For data-parallel training, our technique is $1.1 - 1.27 \times$ faster than BytePS in large GPU clusters. For pipeline-parallel training, our optimizations is $1.41 - 1.99 \times$ faster than GPipe and $1.14 - 1.63 \times$ faster than PipeDream.

REFERENCES

[1] Tom B Brown, Benjamin Mann, Nick Ryder, Melanie Subbiah, Jared Kaplan, Prafulla Dhariwal, Arvind Neelakantan, Pranav Shyam, Girish Sastry, Amanda Askell, et al. Language models are few-shot learners. arXiv preprint arXiv:2005.14165, 2020.
[2] Mauro Cettolo, Jan Niehues, Sebastian Stüker, Luisa Bentivogli, R. Cattoni, and Marcello Federico. The IWSLT 2015 evaluation campaign.
[3] Tianqi Chen, Mu Li, Yutian Li, Min Lin, Naiyan Wang, Minjie Wang, Tianjun Xiao, Bing Xu, Chiyuan Zhang, and Zheng Zhang. Mxnet: A flexible and efficient machine learning library for heterogeneous distributed systems. arXiv preprint arXiv:1512.01274, 2015.
[4] Tianqi Chen, Thierry Moreau, Ziheng Jiang, Ziheng Jiang, and Zheng Zhang, Mxnet: A flexible and efficient machine learning library for heterogeneous distributed systems. arXiv preprint arXiv:1512.01274, 2015.
[5] NVIDIA Corporation. FasterTransformer. https://github.com/NVIDIA/FasterTransformer
[6] NVIDIA Corporation. Tensorrt. https://developer.nvidia.com/tensorrt
[7] Wei Dai, Yi Zhou, Nanqing Dong, Hao Zhang, and Eric Xing. Toward understanding the impact of staleness in distributed machine learning. In International Conference on Learning Representations, 2018.
service/gpu/stream_assignment.cc#L78.

[57] The XLA team. XLA - tensorflow, compiled. https://developers.googleblog.com/2017/03/xla-tensorflow-compiled.html, 2017.

[58] Haluk Topcuoglu, Salim Hariri, and Min-You Wu. Performance-effective and low-complexity task scheduling for heterogeneous computing. IEEE transactions on parallel and distributed systems, 13(3):260–274, 2002.

[59] Adina Williams, Nikita Nangia, and Samuel R Bowman. A broad-coverage challenge corpus for sentence understanding through inference. In 2018 Conference of the North American Chapter of the Association for Computational Linguistics: Human Language Technologies, NAACL HLT 2018, pages 1112–1122. Association for Computational Linguistics (ACL), 2018.

[60] Henry Wong, Mikel-Wyrto Papadopoulou, Maryam Sadooghi-Alvandi, and Andreas Moshovos. Demystifying gpu microarchitecture through microbenchmarking. In 2010 IEEE International Symposium on Performance Analysis of Systems & Software (ISPASS), pages 235–246. IEEE, 2010.

[61] Arissa Wongpanich, Yang You, and James Demmel. Rethinking the value of asynchronous solvers for distributed deep learning. In Proceedings of the International Conference on High Performance Computing in Asia-Pacific Region, pages 52–60, 2020.

[62] Zhulin Yang, Zihang Dai, Yiming Yang, Jaime Carbonell, Ruslan Salakhutdinov, and Quoc V Le. Xlnet: generalized autoregressive pretraining for language understanding. In Proceedings of the 33rd International Conference on Neural Information Processing Systems, pages 5753–5763, 2019.

[63] Peifeng Yu and Mosharaf Chowdhury. Salus: Fine-grained gpu sharing primitives for deep learning applications. MLSys’ 20, 2020.

[64] Hao Zhang, Zeyu Zheng, Shizhen Xu, Wei Dai, Qirong Ho, Xiaodan Liang, Zhiting Hu, Jiliang Wei, Pengtao Xie, and Eric P Xing. Poseidon: An efficient communication architecture for distributed deep learning on GPU clusters. In USENIX Annual Technical Conference (USENIX ATC), pages 181–193, 2017.

[65] Sixin Zhang, Anna E Choromanska, and Yann LeCun. Deep learning with elastic averaging sgd. In Advances in Neural Information Processing Systems (NeurIPS), pages 685–693, 2015.

[66] Keren Zhou, Guangming Tan, Xiaozia Zhang, Chaowei Wang, and Ninghui Sun. A performance analysis framework for exploiting gpu microarchitectural capability. In Proceedings of the International Conference on Supercomputing (ICS), pages 1–10, 2017.