Kraken: An Efficient Engine with a Uniform Dataflow for Deep Neural Networks

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Abstract—Deep neural networks (DNNs) have been successfully employed in a multitude of applications with remarkable performance. As such performance is achieved at a significant computational cost, several embedded applications demand fast and efficient hardware accelerators for DNNs. Previously proposed application-specific integrated circuit (ASIC) architectures strive to utilize arrays of hundreds of processing elements (PEs) and reduce power-hungry DRAM accesses using multiple dataflows requiring complex PE architectures. These consume significant area and reduce the maximum clock frequency. This paper introduces the Kraken architecture, which optimally processes the convolutional layers, fully-connected layers, and matrix products of any DNN through a hardware-friendly uniform dataflow. This enables maximal data reuse of weights, inputs, and outputs, with a bare-bones PE design and on-the-fly dynamic reconfiguration. Kraken is implemented in 65-nm CMOS technology at 400 MHz, packs 672 PEs in 7.3 mm\(^2\), with a peak performance of 537.6 Gops. Kraken processes the convolutional layers of AlexNet, VGG-16, and ResNet-50 at 336.6, 17.5, and 64.2 frames/s, respectively, hence outperforming the state-of-the-art ASIC architectures in terms of overall performance efficiency, DRAM accesses, arithmetic intensity, and throughput, with 5.8× more Gops/mm\(^2\) and 1.6× more Gops/W.

Index Terms—Convolutional neural networks (CNNs), deep learning, dataflow processing, energy-efficient accelerators, spatial architecture, application-specific integrated circuits (ASIC), reconfigurable architecture.

I. INTRODUCTION

D

eep Neural Networks (DNNs) have been widely adopted in modern automation systems that require accurate classification and detection due to their remarkable performance in complex pattern recognition tasks. DNNs have been growing deeper and deeper in the past few years, empowering them with beyond human-level capabilities [1], [2]. However, this has been achieved at the expense of increased computational complexity, while many mobile and edge processing applications require fast inference of such DNNs with low power and low chip area.

In order to address this rising demand for efficient inference, application-specific integrated circuit (ASIC) architectures are developed as arrays of hundreds of processing elements (PEs), where each PE performs a multiply-accumulate (MAC) operation. Since convolutional layers, fully connected layers, and matrix products do not impose an order of performing the MACs, the design space for such hardware architectures and their corresponding spatio-temporal orchestrations of data (called dataflows) is quite large.

The amount of data required for the computation of each layer in modern DNNs is in the order of several megabytes [1], which cannot fit the on-chip memories. While this makes repeated DRAM accesses inevitable, they are primarily responsible for the energy consumption in hardware accelerators. For instance, a 32-bit DRAM access consumes 200 times the energy required for a MAC operation in 45 nm technology [3]. In addition, a PE array can only perform a few hundred operations in parallel, a tiny subset of the hundreds of millions of operations required for a layer in a DNN. Naively mapping the operations of layers of varying shapes to the fixed hardware architecture would result in PEs idling without work. Therefore, it is a challenging task of paramount importance to design a generic dataflow that maximizes the overall performance efficiency by optimally utilizing the fixed PE array architecture, while reducing the number of memory accesses by exploiting data reuse opportunities, or varying shapes and types of DNN layers.

Several architectures and their corresponding dataflows have been introduced in the literature over the past few years to accelerate the inference of DNNs [4]–[6]. Weight-stationary dataflows such as NVDA [7], TPU [8], neuFlow [9], Sankaradas et al. [10], Park et al. [11], Chakradhar et al. [12], Sriram et al. [13], Cambricorn-X [14] and Origami [15] hold the weights in register files or SRAMs inside PEs over multiple operations. Input-stationary dataflows such as SCNN [16] hold input pixels inside PEs while changing weights. Output-stationary dataflows such as DaDianNao [17], DianNao [18], Zhang et al. [19], Moons et al. [20], ShiDianNao [21], and Gupta et al. [22] are designed to minimize the energy consumption of reading and writing partial sums. The DianNao family of accelerators [17], [18], [21], [23] minimize memory accesses by storing the entire neural network within their eDRAM buffers and are hence evaluated only on older, smaller networks.

DNA [24] supports three different dataflows to individually optimize the reuse of inputs, outputs, and weights, resulting in a complex 3-level PE structure with large multiplexers. Chen et al. introduced a row-stationary dataflow with an architecture named Eyeriss [25], [26], which maximizes the reuse of weights, inputs and partial sums using scratchpads inside its 168 PEs. The scratchpads take 46.8% of the total area and 47.9% of the total power, in addition to the global buffers that take 18.8% of area. The 2-D array of PEs is controlled through a network-on-chip structure that orches-
Inspired Dataflow (FID) utilized, and a significant amount of energy being consumed relies on scratchpads (SRAMs inside each of the hundreds of fully-connected layers). FID was then generalized into GFID with corresponding architectures named Multi-Mode Inference Engine (MMIE) [29] and ZASCAD [30] with the ability to process larger filter sizes needed for AlexNet and ResNet-50. While MMIE/ZASCAD reports a high utilization factor (percentage of PEs active in a computational clock cycle), its overall performance efficiency is relatively low due to clock cycles wasted during weight passing and data transfer. Ahmadi et al. introduced an architecture [31] for the convolutional layers of VGG-like CNNs and then generalized it into CARLA [32], implemented as an array of 196 PEs. CARLA can process only the convolutional layers of CNNs, and it is tailored for $3 \times 3$ and $1 \times 1$ convolutional layers where the number of output channels is a multiple of 64. This results in a low performance efficiency for convolutional layers with larger filter sizes. CARLA also uses four different dataflows to maximize its utilization, requiring large multiplexers, resulting in mostly idle datapaths in its architecture.

Another parallel area of research is exploiting sparsity in compressed DNNs. The first published versions of Eyeriss [26], MMIE [29], and Ahmadi et al. [31] focused on dense DNNs. They were later extended to exploit sparsity as Eyeriss v2 [33], ZASCAS [30] and CARLA [32], respectively. Eyeriss v2 and EIE [3] use the Compressed Sparse Column (CSC) scheme, while Cnvlutin [34] uses Compressed Sparse Row (CSR) to exploit the zeros resulting from the Rectified Linear Unit (ReLU) activation function, which is commonly found in early CNNs. ZASCAS [30] and EIE are designed to skip such null activations. Cambricorn-X [14] exploits sparsity in pruned weights, whereas SCNN [16] exploits sparsity in both weights and activations. Moons et al. explored the effects of quantization on CNNs [35] to implement EEPS [36], a precision-scalable processor to exploit sparsity. It was then extended into Envision [37], with dynamic scaling of voltage, accuracy and frequency. DNPU [38] also supports precision scaling, but it has a much larger chip area of 16 mm$^2$. There is also some research in designing analog circuits to accelerate smaller CNNs [39].

An elastic grouping, where $C=96$ cores dynamically reconfigure within one clock, using a header of just 64 bits, to process convolutional layers of different filter sizes while maintaining a high PE utilization.

7) Thorough comparison of performance with prior works, benchmarked on AlexNet, VGG-16, and ResNet-50.

8) Implementation in TSMC 65-nm, which outperforms the state-of-the-art [32] with 5.8× more Gops/mm$^2$ and 1.6× more Gops/W in just 1.2× the area.

II. Preliminaries

A. Convolutional Layers

Convolutional layers of a CNN are primarily composed of high-dimensional convolutions used for feature extraction. In such a layer, a spatial convolution followed by a depthwise dot-product between four-dimensional (4-D) arrays of input ($X_{[N,H,W,C]}$) and kernel weights ($K_{[K_H,K_W,C_{in},C_{out}]}$) yield a 4-D output array ($Y_{[N,H/S_H,W/S_W,C_{out}]}$). The shape parameters of a convolutional layer are $N$ (batch size), $H, W$ (height and width of the input), $K_H, K_W$ (corresponding spatial dimensions of the kernel) and $C_{in}, C_{out}$ (number of input and output channels/filters). Fig. 1 demonstrates the convolution operation and its shape parameters.
For the first layer, the input $X$ is composed of the batch of images, and for the subsequent layers it is made of activations of the previous layer. For each output channel $c_o = 0, 1, \ldots, C_o$ and input channel $c_i$, a 2-D filter of size $(K_H, K_W)$ is strided by $(S_H, S_W)$ along the $(H, W)$ dimensions of input to perform a 2-D convolution. Typically the input pixels are zero-padded to ensure the output has the same spatial dimensions but downsampled by the stride: $(H/S_H, W/S_W)$. The resulting $C_i$ number of such 2-D arrays for each output channel $c_o$ are summed together to produce a feature map. $N$ input images of a batch are processed this way, generating the output array $Y$. This operation is described as

$$Y_{n,h/S_H,w/S_W,c_o} = \sum_{c_i=0}^{C_i-1} \sum_{k_h=0}^{K_H-1} \sum_{k_w=0}^{K_W-1} X_{n,h',w',c_i} K_{[k_h, k_w, c_i, c_o]}$$

(1)

where $h' = h + k_h$ and $w' = w + k_w$. Lowercase terms denote the index variables that range from 0 to their uppercase counterparts, e.g., $n \in [0, N)$ and $c_o \in [0, C_o)$.

### B. Matrix Products and Fully-Connected Layers

A fully-connected layer performs a matrix product between a batched 2-D input array $X_{[N, H, W, C_o]}$ and a 2-D weights array $K_{[C_i, C_o]}$ to produce the batched 2-D output array $Y_{[N, H, W, C_i]}$:

$$Y_{[N, H, W, C_i]} = X_{[N, H, W, C_o]} K_{[C_i, C_o]}$$

(2)

Fully connected layers are used as the last few layers of a typical CNN for feature detection, while matrix products are required in the attention function of transformers, and for training of any kind of neural network.

### C. Neural Network Architectures

Neural networks are built as directed graphs of layers. While Kraken can accelerate other types of DNNs as well, in this work, we focus on CNNs. CNNs are built such that, as an image flows through a CNN, it is downsampled by integer factors in the spatial dimensions $(H, W)$ due to striding and pooling. This ensures the extraction of more global features from local ones as we go deeper into the network. Meanwhile, channels typically increase from 3 at the first layer to 1024 or 2048 near the last layers to extract more complex features.

The number of MAC operations in the $j^{th}$ layer can be calculated as

$$\# \text{MAC}_{w/pad} = N(H/S_H)(W/S_W)K_HK_WC_oC_i$$

(3)

and

$$\# \text{MAC}_{valid} = N(H/S_H)(W/S_W)K_HK_W - Z)C_oC_i,$$

(4)

where $H, W, C_o, K_H, K_W = 1$ for fully-connected layers.

We note that, similar to the analysis by Ahmadi et al. [32], but unlike that of Chen et al. [26] [33] and Ardakani et al. [30], we ignore the MAC operations corresponding to the zero paddings $(Z_j)$ when calculating the valid number of MAC operations. While this results in a lower estimate for actual performance, it better reflects the engine’s capability. Furthermore, the exact number of off-chip memory accesses needed to fetch the input $(M_{X,j})$ and kernel $(M_{K,j})$, and store the outputs $(M_{Y,j})$ of the $j^{th}$ layer can be calculated as

$$M_{X,j} = NHWC_i$$

$$M_{K,j} = K_HK_WC_oC_i$$

$$M_{Y,j} = N(H/S_H)(W/S_W)C_o.$$

The number of memory accesses per layer and per inference can be calculated as their sums.

With AlexNet [41], acing the ImageNet Large Scale Visual Recognition Challenge (ILSVRC) in 2012, the race to build deeper CNNs with higher accuracy began. Today, every few
months, in every subfield of machine vision, a novel state-of-the-art CNN architecture is introduced to outperform the last. While any convolutional or fully-connected layer in such models is characterized by the shape parameters outlined above and can hence be accelerated by Kraken, for the purposes of benchmarking and comparison, AlexNet [41], VGG-16 [42] and ResNet50 [43] are chosen in accordance with the prior works [26], [30], [32].

D. Quantization

Integer quantization with 8-bits [44] has become the industry standard for inference of DNNs. A trained network can be easily quantized (post-training quantization) with a slight reduction of accuracy. Modern machine learning frameworks such as Tensorflow [45] and PyTorch [46] also widely support quantization-aware training, where a trained network is further trained, taking quantization effects into account. This yields 8-bit inference without any noticeable degradation in accuracy for most DNNs [47]. Bias terms ignored in equations (1) and (2) can be folded into the quantization parameters.

III. ARCHITECTURE DESIGN

This section describes the Kraken architecture, co-designed around its dataflow. Therefore, relevant subsections of Sec. IV are referred appropriately. Kraken engine is built as a 2-D array of PEs, statically configured into $R$ rows and $C$ cores. Cores are elastically grouped into $E$ groups, as demonstrated in Fig. 2. Each elastic group computes $S_W$ output channels, such that $R$ among $H/S_W$ rows and $ES_W$ among $C_o$ channels of the output array are calculated in parallel. The $G$ cores in each elastic group compute partial sums (further described in Sec. IV-C), which are shifted and accumulated $K_W$ times to the right inside the same accumulators to perform the horizontal convolution. Therefore, $ES_W R$ full output pixels are computed in parallel and released together every $1 + C_i K_H$ clocks, which are then transferred to the off-chip memory without stalling the engine.

A. Processing Element (PE)

The simplicity of the processing element is a unique and distinguishing feature of Kraken. Traditionally accelerators are built with a large SRAM or a register file inside each of their hundreds of PEs to store partial sums, weights or inputs to make data reuse possible, as further detailed in Sec. VI-B. Due to this complexity multiplied by the sheer number of PEs, these designs fail to pack more PEs in their chip, resulting in a fewer operations per area. The routing complexity inside such complex PEs would also reduce fmax.

Kraken’s uniform dataflow eliminates the need for SRAMs, register files, and large muxes, greatly simplifying the PE. In contrast to previously proposed designs, Kraken’s PE consists of just the bare-bones: a multiplier, an accumulator with bypass, and a 2-way multiplexer (fig. 2) which allows both shift-accumulation of partial sums and elastic grouping.

B. Elastic Group (EG)

For any convolutional layer, $C$ cores of the engine get elastically grouped into $E$ EGs with $G$ cores per group, where

$$G = K_W + S_W - 1$$

$$E = \left\lfloor \frac{C}{G} \right\rfloor$$

As Kraken’s PE array is stateless, the multiplexers at the edges of an EG simply respond to the configuration bits tied to the wide data packets from the weights rotator to group on the fly elastically. As $W$ columns of the input array are loaded sequentially, weights are interleaved to produce partial sums corresponding to $S_W$ number of output channels in each elastic group while maintaining high utilization.

Within each EG, $G$ cores compute the partial sums of horizontal convolution. At the end of every $C_i K_H$ clocks, the multiplexers are set and partial sums are shifted into the accumulator of the core on right. The output filter extracts the results of the appropriate cores of each EG, each of which are the accumulation of $K_W C_i K_H$ products, i.e., the full output convolution sum. The interleaving of channels and strided horizontal convolution are further described in Sec. IV-C.

During the operation, $\%$ cores (if any) remain idle, where % denotes the modulo division. This number is low, as elastic groups can stretch to fill the entire span of all $C$ cores. The lack of rigid boundaries (hence elastic) between groups of cores (unlike CARLA [32] and ZASCA [30]) while maintaining very low routing complexity enables Kraken to achieve high performance efficiency and utilization.

C. Pixel Shifter

A small shift register bank of depth $R + \max\{F\}$ and a bank of AXI-Stream adapters (datawidth converters) make the
pixel shifter. The shift factor \( F \) for a given layer is defined as

\[
F = \lfloor \frac{K_H}{S_H} \rfloor - 1. \tag{7}\]

The first \( R \) registers directly supply data to the engine without any multiplexers, which helps to meet timing at high \( \text{fmax} \). The registers are shifted \( K_H \) times to enable the engine to perform strided vertical convolution optimally, as further described in Sec. IV-A. Only the adapters needed for a given set of \( (K_H, S_H) \) combinations can be instantiated during synthesis. For example, to process AlexNet, VGG-16, and ResNet-50 (Table I), \( 8 \rightarrow R, R+2, R+3, R+4 \) adapters are synthesized and multiplexed into the shift register bank.

**D. Weights Rotator**

Two SRAMs, each \( C \) words wide and \( \max\{S_W C, K_W\} \) rows deep and a 2-stage AXI Stream register pipeline to mask their latency, and an AXI Stream adapter make a weights rotator. It is worth noting that these two global buffers are the only on-chip memories in the system. Memory compilers are able to optimize large, global SRAMs and save on-chip area, in contrast to the prior works that employ hundreds of smaller per-PE SRAMs, in addition to their large global SRAM buffers.

During each iteration \( t \), \( C_i K_H S_W \) kernel words required for the next iteration \( t+1 \) are slowly pre-fetched from the off-chip memory through a low-bandwidth, low-priority AXI-4 bus and filled into W-SRAM. At the end of an iteration, the two SRAMs switch their roles. The newly filled SRAM becomes R-SRAM and delivers the weights through a \( C \) words wide AXI4-Stream bus to the \( C \) cores of the engine. This datapath is registered at the pipeline registers, which helps to meet timing at high \( \text{fmax} \). Inside each core, the same weight value is broadcasted to \( R \) number of PEs. The weights are rotated \( N L W \) times throughout the iteration, maximizing the reuse of weights to minimize DRAM accesses compared to prior works.

**E. Output Pipe**

Without stalling the engine, a shift register bank of \( RC \) words receives a copy of the data from the accumulators of the PE array, and shifts them along its \( C \) dimension. A bank of multiplexers filter the full output sums from these \( C \) groups into the \( \lfloor C/3 \rfloor \) groups of a second shift register bank of depth \( R \lfloor C/3 \rfloor \). The second bank shifts its \( R, ES_W \) valid outputs into an \( R \) words wide AXI4-Stream which is then sent out to DRAM.

**F. Static Configurability**

Kraken’s implementation is highly parametrized. In addition to \( R \) rows and \( C \) cores of PEs, it can be synthesized for any set of word widths. The multiplier latency can be adjusted to improve timing and is set to zero in our implementation. SRAM width of weights rotator can be chosen as \( \max\{S_W C, K_W\} \) for the set of CNNs that needs to be processed. The number of shift registers in the pixel shifter and output filter, AXI-Stream adapters, and the multiplexers can be synthesized either for a given set of \( (K, S) \) values or for all possible combinations.

**G. On-the-fly Dynamic Reconfiguration**

After being implemented in a static configuration, accelerators need to be dynamically reconfigured before processing each layer to assign work to the PEs optimally during runtime. For Kraken, headers of 64 configuration bits are pre-pended to the \( \hat{X} \) (input) and \( \hat{K} \) (kernel) AXI Stream packets and are streamed into the system through the datapath. In a single clock cycle, the pixel shifter and the weights rotator load the configuration bits that specify \( K_H, K_W, S_H, S_W, C_i, F \) for the upcoming layer into their registers. This data, about two bytes wide, is appended to the data stream that is \( R+C=103 \) bytes wide. Each part of the system: multiplexers in AXI Stream adapter banks, pixel shifter, PE array, and the output shifter, each react to the configuration bits available at that point in the system, in a decentralized fashion. In the clock cycle following the completion of feeding the \( \hat{X} \) and \( \hat{K} \) of a layer, the configuration registers are updated with new values without stalling the engine. The modules downstream continue processing the old data and only update their behavior when the new data reaches them. This on-the-fly dynamic reconfiguration allows back-to-back processing of layers without hardware overhead and helps to achieve high \( \text{fmax} \).

**IV. UNIFORM DATAFLOW**

Dataflow is the pattern in which the 4-D arrays of input \( X \), kernel \( K \), and output \( Y \) (each with varying shape parameters) are restructured into \( \hat{X}, \hat{K}, \) and \( \hat{Y} \), respectively, and orchestrated through the fixed architecture of the PE array of \( R \) rows and \( C \) cores. Kraken’s dataflow outperforms prior works in maximizing the reuse of data and utilizing its PEs, using a bare-bones PE architecture. This section describes Kraken’s dataflow in detail, while algorithm 1 presents a summary.

In a nutshell, height (\( H/S_o \)) of the output \( Y \) is split into \( L \) blocks, each \( R \) pixels high. The \( C_o \) output channels are split into \( T \) iterations, each with \( ES_W \) channels. \( R \) rows and \( ES_W \) channels of the output are computed in parallel (fig. 1). Vertical convolution (\( \Sigma^{K_H} \)), depthwise dot product (\( \Sigma^{C_i} \)), and horizontal convolution (\( \Sigma^{K_W} \)) are performed in the said order to produce \( RES_W \) full output pixels every \( q_{ke} \) clock cycles. This is repeated over \( W \) input columns, \( L \) blocks, \( N \) batches and \( T \) iterations to produce the full output array \( Y_l \), where

\[
L = \left\lfloor \frac{H}{RS_H} \right\rfloor \tag{8}
\]

\[
T = \left\lfloor \frac{C_o}{ES_W} \right\rfloor \tag{9}
\]

\[
q_{ke} = 1 + K_H C_i. \tag{10}
\]

Kraken’s data tiling (restructuring) is expressed via a custom notation. Its order is based on the C-style array indices, also known as the row-major order, that specifies how multidimensional arrays are typically stored in a linear computer memory. In addition, two pairs of brackets show the data movement, separating the number of data beats (serial) and number of words in a data beat (parallel). For example, \( \alpha: [1][2][3] \) denotes a 3-D C-style array of 6 elements (C: (type) alpha [1][2][3];) stored in the flattened
order: \( \{ \alpha_{[0,0,0]}, \alpha_{[0,0,1]}, \alpha_{[0,0,2]}, \alpha_{[0,1,0]}, \alpha_{[0,1,1]}, \alpha_{[0,1,2]} \} \) and streamed through a 3-words wide port, in \( 2 \times 1=2 \) clock cycles (data beats). The data orchestration is described in its loop nest representation of parallel and serial nested loops operating on these multidimensional arrays. Therefore, the number of clock cycles required to move data, the shape of data in a parallel bus, and the order in which data is moved are all expressed through the introduced notation. Kraken’s dataflow is first introduced using the shape parameters of convolutional layers. Fully-connected layers and matrix products are then optimally expressed as special cases of the described dataflow.

It should be noted that \( K \rightarrow \hat{K} \) for all layers is performed offline and all \( K \) are stored in the DRAM in advance. Whereas \( X_0 \rightarrow \hat{X}_0 \) is performed once per inference for the first layer, \( Y_j \rightarrow \hat{X}_{j+1} \) is performed per pixel as data is streamed out of the engine, such that no clocks are wasted between layers. Therefore, the restructurings are all \( \mathcal{O}(n) \) in space and time, and have no performance overhead.

### A. Strided Vertical Convolution and Depthwise Dot Product

\( R \) rows of the PE array are tasked with computing the \( R \) consecutive rows of the output \( Y \). Therefore, for vertical convolution, each PE row needs to be fed with \( K \) consecutive rows of the input \( X \), while they calculate the pixels that are \( S \) apart. As a result, while many of the same input pixels are stored in the DRAM in advance, they calculate the pixels that are \( S \) apart. Kraken’s dataflow interleaves the pixels in memory to perform any strided vertical convolution as described below, to avoid additional registers and multiplexers required for nonlinear shifting patterns.

The 4-D array of input pixels \( X \) is first sliced along \( H \) dimension into \( L \) blocks, where each block has a height \( RS_H \), producing \( X_1 \). Each block \( l \) is then padded with \( (K_H - 1)/2 \) bottom rows of the previous block \( l-1 \) and \( F - (K_H - 1)/2 \) top rows of the next block \( l+1 \) to produce \( X_2 \). The height of each block is then reshaped into \( [R+F,S_H] \) to produce \( X_3 \). Finally, the entire array is transposed into \( \hat{X} \) and stored in the off-chip DRAM. This multidimensional transpose operation results in pixel interleaving as demonstrated in Table II.

The tiled input \( \hat{X} \) is pulled from the DRAM into \( R+F \) parallel words. \( S_H \) such data beats are loaded sequentially into a small shift register bank of \( R+F \) words, as demonstrated

| \( \text{reg} \) | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| --- | --- | --- | --- | --- | --- | --- | --- |
| \( R_0 \) | \( x_{h0} \) | \( x_{h2} \) | \( x_{h4} \) | \( x_{h6} \) | \( x_{h1} \) | \( x_{h3} \) | \( x_{h5} \) |
| \( R_1 \) | \( x_{h2} \) | \( x_{h4} \) | \( x_{h6} \) | \( x_{h8} \) | \( x_{h3} \) | \( x_{h5} \) | \( x_{h7} \) |
| \( R_2 \) | \( x_{h4} \) | \( x_{h6} \) | \( x_{h8} \) | \( x_{h10} \) | \( x_{h5} \) | \( x_{h7} \) | \( x_{h9} \) |
| \( R_3 \) | \( x_{h6} \) | \( x_{h8} \) | \( x_{h10} \) | \( x_{h12} \) | \( x_{h7} \) | \( x_{h9} \) | \( x_{h11} \) |
| \( R_4 \) | \( x_{h8} \) | \( x_{h10} \) | \( x_{h12} \) | \( x_{h14} \) | \( x_{h9} \) | \( x_{h11} \) | \( x_{h13} \) |
| \( R_5 \) | \( x_{h10} \) | \( x_{h12} \) | \( x_{h14} \) | \( x_{h16} \) | \( x_{h11} \) | \( x_{h13} \) | \( x_{h15} \) |
| \( R_6 \) | \( x_{h12} \) | \( x_{h14} \) | \( x_{h16} \) | \( x_{h18} \) | \( x_{h13} \) | \( x_{h15} \) | \( x_{h17} \) |

### Algorithm 1: Kraken’s Uniform Dataflow

#### Pixels in DRAM:

\[ X : [N, H, W, C] \]
\[ X_1 : [N, L, RS_H, W, C] \]
\[ X_2 : [N, L, RS_H + FS_H, W, C] \]
\[ X_3 : [N, L, R + F, S_H, W, C] \]
\[ \hat{X} : [N, L, W', C, S_H] \]

\[ R + F \] transpose

#### Pixels via Shifter:

\[ \hat{X}_1 : [N, L, W, C, S_H, F'] \]
\[ \hat{X}' : [N, L, W, C, K_H'] \]

\[ \hat{X} \text{ shifted } F' \text{ times} \]
\[ \hat{X}' \text{ shifted } K_H \text{ times} \]

#### Kernel in DRAM & via Weights Rotator:

\[ K : [K_H, K_W, C, C] \]
\[ K_1 : [K_H, K_W, C, I, T, E, S_W] \]
\[ K_2 : [T, C_i, K_H, E, K_W, S_W] \]
\[ K_3 : [T, C_i, K_H, S_W][E, G] \]
\[ \hat{K} : [T, C_i, K_H, S_W][C] \]

#### Loop Nest Representation of Dataflow:

1. for \( t \in [0, T) \) do
2. for \( n \in [0, N) \) do
3. for \( l \in [0, L) \) do
4. for \( w \in [0, W) \) do
5. for \( c_i \in [0, C_i) \) do
6. do in parallel
7. for \( r \in [0, R) \) do
8. for \( e \in [0, E) \) do
9. for \( g \in [0, G) \) do
10. let \( \hat{x}' = X_{(n, l, w, g + w \cdot S_W / s_w, c_i)} \)
11. for \( s_w \in [0, S_W) \) do
12. if \( (g + w \cdot S_W / s_w = s_w) \) then
13. let \( k = \hat{K}_{(l, c_i, K_R, S_W)}[e, g] \)

\[ A_{[r, e, g]} \]
\[ A_{[r, e, g-1]} \]
\[ A_{[r, e, g]}' \]

Output pipe & DRAM storage:

\[ \hat{Y} : [T, N, L, W, E, S_W, R] \]
\[ \hat{Y}_1 : [T, N, L, W, E, S_W][R] \]
\[ \hat{Y}_2 : [N, L, W, T, E, S_W, R] \]
\[ \hat{Y}_3 : [N, L, W, C, R] \]
\[ \hat{Y} : [N, L, W, C, S_H][R + F] \]

pad & store as next \( \hat{X} \)
in Table II. After each such load (shaded clock cycles), the
registers are shifted $F'$ times, resulting in $X_1$, where

$$F' = \begin{cases} [K_H/S_H] & \text{on } S_H^n \text{ (last) load} \\ F & \text{other loads} \end{cases}$$

First interleaving the pixels and then shifting them $F'$ times
($\tilde{X}$) is equivalent to loading $K_H$ consecutive pixels into
each of first $R$ registers, just in a different order ($\tilde{X}'$). The $R$
registers are directly connected to the $R$ rows of the PE array,
each row gets the input pixels needed to calculate
its strided output pixel, as demonstrated in Table II. This
exploitation of data reuse in the $H$ dimension of input $X$
results in an $(F' + 1) \times$ reduction of DRAM accesses on
the input side of pixel shifter and fewer engine stalls.

Synchronized with this shifting, the weights rotator supplies
$K_H$ kernel words to the $C$ cores, allowing the PE array to first
perform the strided vertical convolution, corresponding to loop
6 in algorithm 1. This operation is repeated over $C_i$ input
channels (loop 5) as the PEs accumulate the depthwise dot-product.
Since input channels vary widely in depth across layers and are
not shared with neighboring pixels, serially processing them
allows 100% utilization across this dimension. After the end of
this operation, which takes $q_{kc}$ clocks, the pixel shifter repeats
it over the next input column ($W$ dimension).

### B. Unstrided Horizontal Convolution ($S_W=1$)

Table III demonstrates the horizontal convolution for a
simplified example, where $W, K_W=8,5$. $C, G=5$ and $S_W, C_p, E=1$. The partial sums resulting from vertical
convolution followed by depthwise dot product are denoted as

$$\sigma_{w, k_w} = \sum_{i=0}^{C_i} K_H \sum X_{[i, w,...]} K_{[i, k_w,...]}.$$
first valid output column with implicit zero padding: \( y_0 \).
Then, in each consecutive such cycle of \( q_{kc} \) clocks, the last core releases the subsequent output column \( y_w \). At the last such cycle, the last \( [K_W/2]=3 \) valid output columns are released in the same clock, with implicit zero paddings. Therefore, exactly \( W q_{kc}=8q_{kc} \) clock cycles are required to compute \( W=8 \) output columns. This operation allows Kraken to perform horizontal zero padding without extra circuitry or extra data fetches. Accumulators flush their registers with new products from multipliers and start processing the next block, on the following clock itself.

**C. Strided Horizontal Convolution (any \( S_W \))**

Equation (1) shows that horizontally strided convolution is equivalent to discarding all but one column in each stride of \( S_W \) after a regular unstrided convolution. This implies that calculations along \( S_W \) of \( 1 \) number of diagonals in Table III are unnecessary when striding. \( S_W \) of \( 1 \) additional output channels are hence calculated through those diagonals, achieving maximal utilization using the same uniform dataflow.

Table IV demonstrates the strided horizontal convolution for a simplified example where \( W, K_W=8, 5, C, G=6, S_W, C_o=2 \) and \( E=1 \). The partial sums after vertical convolution and depthwise dot product are denoted as

\[
\sigma_{w,k_w}^{s_w} = \sum_{K_i} X_{[w',\ldots]} K_{[k_w,\ldots]}.
\]

Generalized for any convolution, \( C=6 \) cores get elastically grouped into \( E=1 \) elastic groups, each with \( G=6 \) cores, computing \( S_W=2 \) output channels in parallel, such that all output channels are computed in \( T \) iterations. The data movement in this horizontally strided convolution is demonstrated in Table IV. The output channel corresponding to each partial sum is denoted by its superscript and their cells are differently shaded to clearly demonstrate the channel interleaving. \( S_W=2 \) adjacent cores perform identical computations on \( S_W=2 \) output channels. Their results \( y_w^{s_w} \) are released in parallel at the same clock cycles. Therefore, after every \( q_{kc} \) clocks, each row of the PE array releases \( ES_W \) full output pixels, such that \( ES_W R \) pixels are released by the engine. Since initial layers have a bigger filter size \( K_W \) (hence smaller \( E \)) and latter layers have more input channels \( C_i \), the data can be streamed out into the DRAM without stalling the engine. At the end of a layer, the \( C \) cores would get dynamically regrouped into a new set of elastic groups without pausing their operation.

**D. Matrix Product and Fully-Connected Layers**

The multiplication between two matrices

\[
M_{1:[H,C_i]} M_{2:[C_i,C_o]} = M_{3:[H,C_o]}
\]

is a special case of the described dataflow, where \( N, W, K_H, K_W, S_H, S_W = 1 \). Kraken’s PE array of size \((R,C)\) computes the full submatrix of \( M_{1:[R,C]} \) in \( C_i \) clocks and releases it without any shifting. In \( TL \) such iterations, all submatrices of \( M_3 \) are computed. Consequently, the inference of a fully-connected layer described in (2) can be performed with \( N, H, C_i, C_o = 1, N^J, C_j^H, C_j^I \). Inference batch size for the fully-connected layers \((H=N^J)\) can be hence chosen as \( R \) to fully utilize the rows of the PE array and reduce the number of memory accesses by reusing the weights.

**E. Stationary-ness**

Dataflows are categorized by the type of data reuse they prioritize [5]. Kraken’s dataflow primarily prioritizes computing \( ES_W R \) complete output pixels inside accumulators (reuse (c) in fig. 1) to simplify the PEs to their bare-bones by eliminating SRAMs and register files. This makes it output-stationary with respect to the engine. Besides, maximizing data reuse of the kernel array \( K \) is of paramount importance as it is responsible for 73% to 96% of all data movement (see Table I). Hence, Kraken is also designed to be weight-stationary with respect to the system. Primarily weight-stationary architectures hold their weights in register files inside their PEs. Avoiding that, Kraken prefetches weights into global SRAMs (reuse (a) in fig. 1) and rotates them thousands of times, maximizing their reuse throughout an iteration. Pixel shifting exploits data reuse in the \( H \) dimension (reuse (b) in fig. 1), and periodic shift-accumulate within an elastic group exploits data reuse in the \( W \) dimension to further lower the input bandwidth requirement. Therefore, Kraken is built to **maximally exploit the reuse of all outputs, weights and inputs**.

**V. Performance Analysis**

This section presents a detailed performance analysis of Kraken for any DNN, deriving the key metrics as exact functions, which are later optimized over a set of CNNs to find the best static configuration.

**A. Clock Cycles (Q)**

When processing convolutional layers with \( K \neq 1 \), after accumulating every \( C_i K_H \) products, the multipliers pause for one clock to allow shifted accumulation. In such layers, the one clock needed to load the configuration bits does not stall the engine as the pixel shifter reduces the necessary bandwidth on the input side. When processing convolutional layers with \( K_W = 1 \), fully-connected layers, and matrix products, there is no pause for shifting; however, the dataflow is stalled for one clock for configuration, i.e.,

\[
q_s = \begin{cases} 
1 & \text{if } (\text{conv} \& \ K_W \neq 1) \\
0 & \text{otherwise,} 
\end{cases}
\]

\[
q_c = \begin{cases} 
0 & \text{if } (\text{conv} \& \ K_W \neq 1) \\
1 & \text{otherwise.} 
\end{cases}
\]

Therefore, the number of clocks required for the \( j^{th} \) layer is

\[
Q_j = T(q_c + NLW(q_s + C_i K_H)).
\]
B. Performance Efficiency ($E$)

In order to evaluate the ability of a dataflow to utilize the processing elements over the entire operation, Performance Efficiency over a DNN or a set of DNNs is defined as

$$E = \frac{\text{Average Gops}}{\text{Peak Gops}} = \frac{\text{Valid Gops of the PE layer}}{\text{Valid Gops of the PE layer}}$$

where $E$ is the performance efficiency of the PE layer.

It is worth mentioning that unlike in prior works [26], [30], only the operations that exclude zero padding are considered valid, while all clock cycles $Q_j$, including those required for reconfiguration, are considered for realistic analysis.

Note that, for fully-connected layers and matrix products, $H, C_i = N^j, C^j_i$ and $N, W, K_H, =1$. Hence, using (4), (8), (9), and (17), the performance efficiency $E_j$ of Kraken over a layer can be derived as a function of the static configuration parameters $R, C$ as

$$E_j(R, C) = \frac{(N K_H K_W H W / (S_H S_W) - Z) C_o C_i}{R C T (q_c + N L W (q_a + C_i K_H))}$$

In order to easily observe the key factors affecting $E_j$, shifting and configuration clock cycles ($q_s, q_c$) can be neglected to yield the simplified function:

$$E_j(R, C) = \frac{(H / R S_H) \cdot C_o K_W}{C S_W}$$

Since $H$ of the layers decrease by integer factors as we progress through a CNN due to pooling and striding, $R$ can be chosen such that $H$ is evenly divisible by $R S_H$ for all layers. Observing that all but the first couple of layers of a CNN have $S_W=1$ and $K_W=3, 1$, $C$ can be chosen as a multiple of 3 (as with the implemented Kraken 7×96 configuration) improving their efficiency into

$$E_{j=0,1} = \frac{(C_o K_W)}{C S_W}$$

C. Memory Accesses ($M$)

The number of memory accesses ($\hat{M}_j$) Kraken requires to compute the $j$th layer is the sum of the data moved as input pixels $M_{X,j}$, weights $M_{K,j}$, and output pixels $M_{Y,j}$, which are also functions of the static configuration parameters $R, C$. The total memory accesses $\hat{M}(R, C)$ can be computed as

$$\hat{M}(R, C) = \sum_j \hat{M}_j(R, C),$$

where

$$\hat{M}_j(R, C) = M_{X,j}(R, C) + M_{K,j}(R, C) + M_{Y,j}(R, C)$$

$$M_{X,j}(R, C) = T N L W C_i S_H (R + F)$$

$$M_{K,j}(R, C) = T C \cdot K_H S_W C$$

$$M_{Y,j}(R, C) = T N L W E S_W R.$$

D. Arithmetic Intensity (AI)

To measure the degree of data reuse facilitated by the dataflow throughout a CNN, AI is defined as

$$AI = \frac{\# \text{Valid Operations}}{\# \text{Memory Accesses}}$$

For Kraken, $AI(R, C)$ can be computed using (4) and (20) as

$$AI(R, C) = \frac{2 \times \# \text{MAC}_{\text{valid}}}{M(R, C)}$$

E. Memory Bandwidth Requirement

The pixel shifter of Kraken requires $R + F$ words of input pixels in every $F'$ clocks. Over iteration $t$, the weights rotator loads $C_i K_H S_W C$ number of words of the weights for the next iteration $t + 1$. Furthermore, the output pipe needs to stream $E S_W R$ words of the previous output column $w-1$ within $S_W (C_i K_H + q_s)$ clocks, before the current output column $j$ is generated by the PE array. Therefore, the bandwidth (words/s) requirement of the input $X$, kernel $K$, and the output $Y$ at frequency $f$ are computed as

$$\text{Bandwidth}_{X} = f (R + F) / F'$$

$$\text{Bandwidth}_{K} = f \left[ \frac{C_i K_H S_W C}{(q_c + N L W (q_a + C_i K_H))} \right] t$$

$$\text{Bandwidth}_{Y} = f \left[ \frac{E S_W R (w-1)}{C_i K_H + q_s} \right] w$$

For fully-connected layers and matrix products, take $C_i = C^j_i$, $C_o = C^j_o$, $F, F', q_s=0$, and $q_c, K_H, S_W, N, L, W, E=1$.

VI. RESULTS AND DISCUSSION

In this section, the implementation of Kraken is described and then compared with the prior works: Eyeriss [26], MMIE/ZASCAD [30], and CARLA [32]. Whereas Kraken can accelerate any DNN with convolutional, fully-connected layers and matrix products, it is benchmarked on AlexNet, VGG-16, and ResNet-50 for comparison.

A. Implementation

Based on the performance analysis presented Sec. V, and optimizing with respect to the performance efficiency in (19) and the memory accesses in (20) over the three CNNs, the static configuration that minimizes the memory accesses with overall optimal performance efficiency is calculated as $R \times C = 7 \times 96$. Although slightly higher performance efficiencies can be achieved by reducing $C$ at $R \times C = 7 \times 15, 7 \times 24$ & $14 \times 24$, these improvements are found to be minimal, at the expense of a much higher number of memory accesses.
The architecture of Kraken was described and verified primarily in SystemVerilog. Interfaces were implemented to comply with the stream and memory-mapped protocols from the industry-standard system bus family of ARM Advanced eXtensible Interface (AXI). After hardware verification on the FPGA: Xilinx Z-7045 Programmable SoC, the design was appropriately modified for ASIC and was synthesized using Cadence Genus with TSMC 65-nm GP CMOS technology. SRAMs generated using Arm Artisan Memory Compiler were packed into banks that are max\{SW C_1 K_W\} = 2048 rows deep and C=96 words wide. Open-source IPs [48] were used for AXI protocol conversion.

As per (23), (24), and (25), the peak bandwidth required for Kraken 7×96 is 26 bytes/clock for the convolutional layers (layer 1 of VGG-16) and 104 bytes/clock for the fully-connected layers. LPDDR4 memory packages offer bandwidths up to 25.6 GB/s (3200 mega transfers per second over a 64-bit IO bus) [49]. Therefore, to operate well within this bandwidth, Kraken is implemented to be run at a frequency of 400 MHz for convolutional layers and 200 MHz for fully-connected layers.

### B. Comparison with State-of-the-Art Implementations

Table V compares the results of Kraken 7×96 with the prior works on convolutional layers of AlexNet, VGG-16, and ResNet-50. Since only ZASCAD reports performance on fully-connected layers, Table VI compares Kraken 7×96 and ZASCAD on them.

Figure 3 presents the performance efficiencies of Kraken, calculated using the exact expressions derived in (19) and (18), with that of the prior works calculated using the number of valid MACs (Table I) and formulae presented in respective papers for the number of clock cycles, when processing each layer of AlexNet, VGG-16, and ResNet-50. Note that, for ResNet-50, only the layer configurations, where Kraken, CARLA, and ZASCAD demonstrate unique (non-repetitive) performance efficiency values, are presented.

We note that Eyeriss [26] [33] and MMIE/ZASCAD [30] have included the wasted operations associated with zero padding when presenting their performance (Gops) and energy efficiency whereas we follow CARLA [32] in ignoring such operations (see (4)). This is because, as Kraken and CARLA perform zero-padding without overhead, inclusion of zero-pads into the operation count yields unrealistic performance efficiencies above 100%. Therefore, for a consistent comparison, these metrics of prior works have been recalculated using

### Table V

| Technology | Methodology | AlexNet | VGG16 | VGG16 ResNet50 | VGG16 | ResNet50 | VGG16 | ResNet50 |
|------------|-------------|---------|-------|---------------|-------|----------|-------|----------|
| TSMC 65nm  | Silicon     | 63.6    | 30.8  | 66.4          | 78.7  | 51.9     | 96.4  | 89.5     |
| TSMC 65nm  | Place & Route | 34.7   | 0.7   | 48.1          | 2.2   | 9.6      | 2.5   | 10.8     |
| TSMC 65nm  | Synthesis   | 115.3   | 4309.5| 20.8          | 421.8 | 103.6    | 396.9 | 92.7     |
| TSMC 65nm  | Synthesis   | 278     | 236   | 265           | 301   | 248      | 247   | 247      |
| Frequency (MHz) | 4            | 3      | 1      | 1              | 1     | 1        | 1     | 1        |
| Bit precision | 16          | 16     | 16     | 16             | 16    | 16       | 16    | 16       |
| Performance Efficiency (%) | 66.4      | 78.7   | 51.9   | 96.4           | 89.5  | 66.4     | 86.8  | 88.3     |
| Throughput (fps) | 34.7     | 0.7    | 48.1   | 2.2            | 9.6   | 2.5      | 10.8  | 336.6    |
| Latency (ms) | 115.3    | 4309.5 | 20.8   | 421.8          | 103.6 | 396.9    | 92.7  | 15.2     |
| Power (mW) | 278       | 236    | 265    | 301            | 248   | 247      | 247   | 1050     |
| Batch size | 4         | 3      | 1      | 1              | 1     | 1        | 1     | 1        |
| Performance (Gops) | 42.8    | 20.7   | 59.3   | 65.3           | 71.0  | 74.2     | 79.8  | 414.8    |
| Performance/Area (Gops/mm²) | 3.5      | 1.7    | 9.9    | 10.9           | 11.8  | 12.0     | 12.9  | 56.6     |
| Energy Efficiency (Gops/W) | 153.8   | 87.6   | 232.7  | 217.0          | 286.2 | 300.5    | 323.3 | 492.5    |
| Memory Access / frame (10⁵) | 2.0       | 56.1   | 8.7    | 205.2          | 102.1 | 129.4    | 69.1  | 6.4      |
| Memory Access / frame (MB) | 3.85     | 107.0  | 16.6   | 375.5          | 154.6 | 258.2    | 124.0 | 7.5      |
| Arithmetic Intensity (Op/MA) | 610.6   | 529.1  | 142.2  | 144.7          | 72.4  | 229.4    | 107.0 | 191.8    |

### Table VI

| Frequency (MHz) | 40 | 200 |
|----------------|----|-----|
| AlexNet        | 96.8 96.6 86.8 | 99.1 99.1 94.7 |
| VGG16 ResNet50 | 131.6 61.0 33.8 | 2.4k 1.1k 62.1k |
| AlexNet        | 7.6 16.4 0.3 | 2.9 6.5 0.1 |
| VGG16 ResNet50 | 37 40 36 | 613 613 613 |
| Batch size     | 1 1 1 | 7 7 7 |
| Perf. (Gops)   | 14.6 15.1 13.5 | 266.5 266.3 254.5 |
| Gops/mm²      | 2.4 2.5 2.3 | 36.3 36.3 34.7 |
| En.Eff. (Gops/W) | 395.0 | 377.1 | 380.8 | 434.8 434.5 415.3 |
| MA/frame (10⁵) | 55.8 124.3 2.1 | 12.2 27.0 0.5 |
| MA/frame (MB)  | 117.8 247.3 4.1 | 11.7 25.9 0.5 |
| AI (Op/MA)    | 2.0 2.0 2.0 | 9.1 9.2 8.6 |

The architecture of Kraken was described and verified primarily in SystemVerilog. Interfaces were implemented to comply with the stream and memory-mapped protocols from the industry-standard system bus family of ARM Advanced eXtensible Interface (AXI). After hardware verification on the FPGA: Xilinx Z-7045 Programmable SoC, the design was appropriately modified for ASIC and was synthesized using Cadence Genus with TSMC 65-nm GP CMOS technology. SRAMs generated using Arm Artisan Memory Compiler were packed into banks that are max\{SW C_1 K_W\} = 2048 rows deep and C=96 words wide. Open-source IPs [48] were used for AXI protocol conversion.

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I. **VGG-16**, (c) **ResNet-50**, and (d) **overall** ($E$)

(a) AlexNet Layers ($j$)

(b) VGG-16 Layers ($j$)

(c) ResNet-50 Unique Layer Configuration (Type: $K,C,O,H$)

(d) Overall ($E$)

Fig. 3. Comparison of performance efficiency: layer-wise ($E_j$) on (a) AlexNet, (b) VGG-16, (c) ResNet-50, and (d) overall ($E$) on the three CNNs.

#MAC_{valid} (see (4) and Table I), their throughputs (fps) and number of clock cycles.

1) **Eyeriss (JSSC’17):** was introduced in [26] as an array of $12 \times 14 = 168$ PEs. Each PE consists of a 224-word deep, 16-bit wide SRAM, a 41-word register bank, 4 FIFOs, 5 registers, 2 two-way multiplexers and a controller, in addition to the multiplier and the adder. This results in 60% of the per-PE area and 47.9% of the total area being utilized for PE scratchpads (SRAM and register bank), while only 9.4% of the per-PE area being used for the multiplier and the adder. In Eyeriss v2 [33], each PE is implemented using seven pipeline stages and five scratchpads, with 288 bytes of SRAM and 98.5 bytes of registers per PE, resulting in only 5.2% of the per-PE area utilized for the two multipliers and adders. In contrast, Kraken’s dataflow eliminates the need for scratchpads inside PEs, resulting in 87.12% of the per-PE area is used by the multiplier and the accumulator, making it possible to pack 4× more PEs, and 2.1× more memory (as global buffer) in 0.6× the area compared to Eyeriss, as shown in Table V. We note that the area and power metrics of Eyeriss is presented from their fabricated chip while Kraken’s metrics are post-synthesis.

The PE array of Eyeriss is assigned work by a Network-on-Chip using either multicast or point-to-point data delivery dictated by their row-stationary dataflow. Reconfiguration after each layer is done by serially feeding a 1794-bit scan chain, which takes about 100 $\mu$s. In addition to the relatively low utilization on processing clock cycles, the PE array is idle during reconfiguration and while data is being transferred from and to off-chip DRAM, resulting in low overall performance efficiencies of 63.6% and 30.8% for AlexNet and VGG-16. Meanwhile, Kraken takes just zero or one clock cycle (2.5 ns) to load the configuration data. In addition, reconfiguration and control paths are decentralized, and relatively smaller buffers are employed, eliminating the need to stall the engine during reconfiguration and data transfer. As a result, while Eyeriss achieves fewer memory accesses and higher arithmetic intensity, Kraken outperforms Eyeriss in terms of performance efficiency, throughput and latency as shown in Table V.

2) **MMIE [29] / ZASCAD [30] (TCOMP’20):** is built as an array of 32 1-D reconfigurable tiles. The 6 PEs of each such tile dynamically group into effective tiles, each tasked with computing one output channel. This limits the reconfigurability to only a handful of $K,S$ combinations and leaves higher percentage of PEs idle on every clock for certain layers. Each of the 192 PEs of ZASCAD contains a 192 bytes of SRAM (64 words deep, 24 bits wide) to store the consecutive pixels to be used in vertical convolution ($2^K \times \Sigma \Sigma \Sigma$). Each PE also has a corresponding 11-word register bank and an 11-way multiplexer in the tile’s weight generator, most of which are unused for most $K,S$ combinations. This results in a much larger per-PE area. Kraken’s novel dataflow performs vertical convolution via interleaved pixel shifting and simplifies PE design. Weights Rotator has two large SRAM banks, which memory compilers optimize better than hundreds of scattered smaller SRAMs, allowing Kraken to pack $3.5 \times$ more PEs and $10.4 \times$ more memory in $1.2 \times$ the area.

We note that [30] calculates the number of clock cycles needed for MMIE/ZASCAD to compute a layer, ignoring
the extra iteration needed to compute $H_{out} \times W_{out}$ pixels in
groups of $N$ ((11) in [30]). Whereas this helps to report a
much higher performance efficiency, it results in unrealistic
estimates of fractional number of clock cycles for several
layers of AlexNet. Since Kraken is evaluated considering
all extra iterations, see (17), (9) and (9), for a fair com-
parison, Fig. 3 demonstrates the performance efficiencies
of MMIE/ZASCAD, using $[(H_{out} \times W_{out})/N]$ to accurately
consider the under-utilized extra iterations as well. Fur-
thermore, while MMIE reports high utilization factors (percentage
of PEs active in a computational clock cycle), it wastes several
clock cycles in a process called weights passing when starting
each new row, and is unable to perform computations when
streaming out output pixels. This results in a low overall
performance efficiency calculated using their reported clock
cycles and valid MACs (see (4)). In contrast, Kraken fetches
weights for the next iteration while rotating weights for the
current one and streams out output pixels without stalling the
engine. Therefore Kraken outperforms MMIE in performance efficiency (Fig. 3) for both convolutional and fully-connected
layers of AlexNet, VGG-16, and ResNet-50.

While ZASCAD/MMIE accelerates fully-connected layers,
it fails to reuse their weights, which dominate the energy con-
sumption by being 94.3% and 76.8% of all memory accesses
required to compute AlexNet and VGG-16, respectively (see
Table I). In contrast, Kraken processes $R$ batches in parallel
using the loaded weights, when computing fully connected
layers, resulting in a much fewer memory accesses per frame
in both fully connected layers and overall network as shown
in Fig. 4 and a much higher arithmetic intensity as presented
in Table VI. Kraken significantly outperforms ZASCAD in
every metric presented in Tables V and VI due to more PEs
operating at higher frequency, and a more efficient dataflow
that maximizes data reuse and overall performance efficiency.

3) CARLA (TCAS’21 [32]): is built as an array of 65
cascaded convolutional units (CUs), where the first 64 contain
3 PEs and the last CU contains 4 PEs. Four distinct dataflows
are employed to achieve performance efficiency in those
layers, requiring each of the 196 PEs to have a pair of 224
word SRAMs and an input register, and each CU to have a
4-way mux, two 3-way muxes, two 2-way muxes and two
registers. Fully-connected layers are not processed, and their
performance is not measured. In contrast, Kraken employs
a single, uniform dataflow which is able to optimally process any
convolutional layer, fully-connected layer or matrix product
to outperform CARLA in overall metrics, eliminating the
need for complex PEs and data routing in its architecture.
Consequently, Kraken’s implementation packs $3.4 \times$ PEs and
$4.5 \times$ SRAM for much better data reuse, in just $1.2 \times$ the area,
running at $2 \times$ the frequency, resulting in a peak performance
of $5.8 \times$ more Gops/mm² and $1.6 \times$ more Gops/W compared
to CARLA, as presented in Tables V and VI.

The architecture of CARLA has been tailored for the
convolutional layers of VGG and ResNet CNNs, such that
SRAM depth, number of PEs and number of CUs are factors
of the dimensions of those networks. Fig. 3 demonstrates
the Kraken $7 \times 24$, similarly optimized for only these CNNs,
outperforming CARLA with 93.3% performance efficiency in
the convolutional layers of ResNet-50 compared to CARLA’s 89.5%. However, the $R_C=7$, 96 configuration is implemented for being efficient over all kinds of CNNs (including AlexNet), while requiring fewer memory accesses.

CARLA’s PE utilization factor (PUF: percentage of PEs active in a computational clock cycle) of 98.46% reported for $3\times3$ convolutional layers is from a reported formula that has been simplified with certain assumptions, which do not hold for all considered $3\times3$ layers. When using the accurate formula presented in [32], some degradation is observed in PUF. While the tailored architecture allows CARLA to achieve over 90% utilization in $3\times3$ and the initial $1\times1$ layers of ResNet-50, its performance efficiency drops to 45% for $7\times7$ and 73% for the latter $1\times1$ layers.

Due to poor utilization over layers with large filter sizes, CARLA is not evaluated on AlexNet, whose $11\times11$ and $5\times5$ convolutional layers contain 49% of its computations. In contrast, Kraken processes convolutional layers with larger filter sizes with acceptable performance efficiencies, due to its elastic grouping. As a result, Kraken $7\times24$ and $7\times96$ achieve performance efficiencies of 79.8% and 73.1% compared to CARLA’s 45% on the first convolutional layer of ResNet-50.

As demonstrated in in Figs. 3 and 4, Table V, the uniform dataflow and generalized architecture of Kraken $7\times96$ outperforms the multiple dataflows and the tailored architecture of CARLA in overall performance efficiency (except for ResNet-50), arithmetic intensity, the number of memory accesses, and energy efficiency, while using simpler and smaller PEs resulting in a much better Gops/area and Gops/W performance.

VII. ACKNOWLEDGMENT

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VIII. CONCLUSION

This paper presents the first generation work to introduce the Kraken architecture and its corresponding dataflow for the inference of dense DNNs, which maximally exploits data reuse in weights, inputs, and outputs with a bare-bones PE design. Furthermore, Kraken’s architecture features dynamic, distributed reconfiguration that takes at most one clock cycle and propagates with data, elastically grouping its cores on the fly, resulting in high overall performance efficiency. A detailed performance analysis is presented, deriving key metrics as exact functions of static parameters, which are then optimized to obtain the static configuration that is then implemented in TSMC 65-nm GP CMOS technology. Kraken’s uniform dataflow is shown to be able to process convolutional layers, fully-connected layers, and matrix products of any shape, outperforming the state-of-the-art in overall performance efficiency, number of memory accesses, and arithmetic intensity, with $5.8\times$ more Gops/mm$^2$ and $1.6\times$ more Gops/W. The implemented system at 400 MHz is shown to have a performance of up to 537.6 Gops, processing the convolutional layers of AlexNet, VGG-16, and ResNet-50 at a throughput of 336.6, 64.2, and 17.5 frames/s, respectively.

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