Abstract—Binary convolutional networks have lower computational load and lower memory foot-print compared to their full-precision counterparts. So, they are a feasible alternative for the deployment of computer vision applications on limited capacity embedded devices. Once trained on less resource-constrained computational environments, they can be deployed for real-time inference on such devices. In this study, we propose an implementation of binary convolutional network inference on GPU by focusing on optimization of XNOR convolution. Experimental results show that using GPU can provide a speed-up of up to $42.61 \times$ with a kernel size of $3 \times 3$. The implementation is publicly available at https://github.com/metcan/Binary-Convolutional-Neural-Network-Inference-on-GPU.

1. Introduction

Deploying deeper neural networks having large number of parameters have been commonplace in the recent years. While this led to state-of-the-art performance, it also came with high computational cost and memory requirements, which has limited their deployment on lower capacity devices. For this reason, there has been an increased interest in development of efficient deep neural network models that can work effectively on devices with limited capabilities. Two fundamental approaches aiming to solve this problem are: designing of smaller Convolutional Neural Network (CNN) models, and pruning existing networks to obtain smaller networks with comparable performance such as MobileNetV2 [1], EfficientNet [2] and ShuffleNet [3]. On the other hand, Binary-Weight-Networks provides a distinct alternative approach to this problem where full-precision operations are replaced with binary-precision operations. The main benefit of these models is that both memory and computation requirements are significantly reduced without changing the parameter size. Even though this comes with a performance penalty, it allows a trade-off between network performance and computational complexity to run such networks on limited capability devices.

In the recent years, an increasing number of binary network models and implementations have been proposed [4]. BitFlow [5] is reported to have $1.8 \times$ speedup against standard binary network implementations, while it has a $11.5 \times$ speedup against full-precision networks. XNOR-SRAM [6] is a hardware solution for ternary-XNOR-and-accumulate (XAC) operations, exhibiting $33 \times$ energy saving. XNOR-Net [7], a prominent type of binary network, has been reported to have $32 \times$ memory saving and $62.7 \times$ theoretical speed-up on CPU. XNOR-Net++ [8] proposed an improved training algorithm for binary networks, achieving 6% higher accuracy on ImageNet compared to XNOR-Net [7].

In this paper, we propose an implementation of binary convolutional network on GPU and optimization of binary XNOR convolution. While training of deep networks have high computational cost, training is generally done once before the deployment of the network. Hence training can be done on systems with higher computational and memory capacity. On the other hand, the inference path of the network is run continuously once it is deployed and the network is generally required to be deployed on cost-effective devices for real-life applications. Hence, inference is desired to have low computational complexity for cost-effective and widespread deployment. In this work, XNOR-Net binary network [7] is taken as the reference method and the forward path of this algorithm, used for the inference, is optimized on GPU.

2. Background

The main bottleneck of CNN models is the high-memory requirement, which hinders their deployment on limited capacity devices. Binary-Weight-Networks [7] binarizes the weight values as opposed to using full-precision and can achieve $32 \times$ memory saving and $2 \times$ speed-up. By approximating both weights and input...
as binary values, X-NOR Net can achieve 58× speed-up in implementation on CPUs. In this section we first describe the binary networks in general and then describe the specifics of XNOR-Net.

2.1. Binary Weight Networks

First, the weight values need to be approximated as binary values so convolution can be implemented with the help of efficient subtraction and addition operations. The binary weights, $B \in \{+1,-1\}^{C \times W \times H}$, are represented by the triplet $c, w, h$, where $w \in [0,W)$ indicates the row, $h \in [0,H)$ the column, and $c \in [0,C)$ indicates the channel. The weights, $W \in \mathbb{W}$, are represented as binary $B \in \{+1,-1\}^{C \times W \times H}$ by the help of a scaling factor $\alpha \in \mathbb{R}^+$ $W \approx \alpha B$. Then the convolution can be approximated as in Eq. 1 where $\oplus$ indicates a convolution without any multiplication.

$$I \ast W \approx (I \oplus B) \alpha$$

(1)

$B = \mathcal{B}_{lk}$ is a binary filter and $\alpha = \mathcal{F}_{lk}$ is a scaling factor and $\mathcal{W}_{lk} \approx \mathcal{F}_{lk} \mathcal{B}_{lk}$ To find optimal solution, the optimization in Eq. 2 is solved.

$$J(B, \alpha) = \|W - \alpha B\|^2$$

$$\alpha^*, B^* = \arg \min_{\alpha, B} J(B, \alpha)$$

(2)

$$J(B, \alpha) = \alpha^2 B^\top B - 2\alpha W^\top B + W^\top W$$

$B \in \{+1, -1\}^n$, $B^\top B = n$ and $W^\top W$ is constant. The parameter that is to be minimized is $-2\alpha W^\top B$ which requires maximization of $W^\top B$. Since $B$ is $\{+1,-1\}$, the maximization can be done by taking the sign of $W$ and multiplying with $W$. By taking the derivative of $J$ with respect to $\alpha$, Eq. 3 and 4 are obtained.

$$B^* = \arg \max_{B} \left\{ W^\top B \right\} \text{ s.t. } B \in \{+1,-1\}^n$$

(3)

$$\alpha^* = \frac{W^\top B^*}{n}$$

(4)

By replacing $B^*$ with $\text{sign}(W)$, this can be written as in Eq. 5 which implies that optimal estimation of binary weight can be computed by taking the sign of weight and scale factor is the average of absolute weight values.

$$\alpha^* = \frac{W^\top \text{sign}(W)}{n} = \frac{\sum |W_i|}{n} = \frac{1}{n} \|W\|_{\ell 1}$$

(5)

2.2. XNOR Networks

In addition to binarization of weights, XNOR-Network also binarizes the inputs. This can be considered as binarizing the inputs of the convolutions by the help of a binary activation function. Since both the weight and input have binary values, convolution operation can then be implemented using XNOR operation. Since both are binary vectors, convolution operation is comprised of shift and dot product operations. In the Binary Weight Network, $W$ is approximated as $\alpha B$ and the input $X$ as $\beta H$. So, it can be written that $X^\top W \approx \beta H^\top \alpha B$, where $H, B \in \{+1,-1\}^n$ and $\alpha, \beta \in \mathbb{R}^+$. This time the optimization process involves two parameters $\alpha$ and $\beta$ as in Eq. 6

$$\alpha^*, B^*, \beta^*, H^* = \arg \min_{\alpha, B, \beta, H} \|X \odot W - \beta \alpha H \odot B\|$$

(6)

where $\odot$ indicates element-wise product. To put the equation into a simpler form, we can define $Y \in \mathbb{R}^n$ as $Y_i = X_i \odot W_i$, $C \in \{+1,-1\}^n$ as $C_i = H_i \odot B_i$, and $\gamma \in \mathbb{R}^+$ as $\gamma = \beta \alpha$. This can be written using the same approach in Binary Weight Networks as in Eq. 7 and 8

$$\gamma^*, C^* = \arg \min_{\gamma, C} \|Y - \gamma C\|$$

(7)

$$C^* = \text{sign}(Y) = \text{sign}(X) \odot \text{sign}(W) = H^* \odot B^*$$

(8)

Since $|X_i|, |W_i|$ are independent this leads to Eq. 9

$$\gamma^* = \sum_{i=1}^n |Y_i| = \sum_{i=1}^n |X_i| |W_i|$$

$$\approx \left( \frac{1}{n} \|X\|_{\ell 1} \right) \left( \frac{1}{n} \|W\|_{\ell 1} \right)$$

(9)

For calculating scale factors, the average of each channel is taken and convolved with 2D filter $k \in \mathbb{R}^{w \times h}$. Expression and final approximation can be defined as in Eq. 10 and 11

$$K = A \ast k, \quad A = \frac{\sum |I_{c,j}|}{c}, \quad k_{ij} = \frac{1}{w \times h}$$

(10)

$$I \ast W \approx (\text{sign}(I) \odot \text{sign}(W)) \odot K \alpha$$

(11)

3. Algorithm Implementation

3.1. Binary Convolution

In this section, we first describe the generic implementation of the XNOR convolution. Then, the CPU and GPU implementations and their differences over the same pipeline are described. Binary convolution has the following steps:

1) XNOR Convolution Bit operations
   - a) Conversion of input data type to binary type
   - b) XNOR bitwise logical operation on binary data with binary weights
c) Summation of output binary bits where 0 values are considered as -1.
d) Converting Binary to float data type.

2) XNOR Convolution Scaling Factor Computation
   a) Channel-wise summation of input data.
   b) Multiplication of matrix \( K \) with the scalar \( \alpha \) value.
   c) Summation of output binary bits where 0 values are masked by bitwise AND operation.

3.1.3. Binary Image to Integer Image. Output of the XNOR convolution is still in binary image format and each convolution result is stored inside a single register. To convert the convolution result into integer, the total number of 1-bits in the register needs to be counted.

In our implementation, in order to count the 1-bits inside the registers, we use the relevant x86_64 instruction and the special function provided by CUDA (\_\_popc) in CPU and GPU implementations respectively.

3.1.4. Multiplication by Scaling Factor. By averaging \( X \in \mathbb{R}^{c \times w \times h} \) across channels, \( A \in \mathbb{R}^{w \times h} \) is obtained. \( A \) is convolved with a matrix \( K \) to get scaling factor matrix \( K \in \mathbb{R}^{w \times h} \), which is multiplied with output.

We implemented multi-threaded versions of both vanilla convolution and XNOR convolution on CPU as baseline methods to compare against the parallelized versions on GPU. In this section, we first describe the CPU implementation. This is followed by the description of GPU implementation.

3.2. Binary Convolution on CPU

The CPU implementation has the following steps.

1) Apply zero padding to the Tensor (3D).
2) Convert the tensor and weights to binary type.
3) Apply bit-wise XNOR operation on binary Tensor.
4) Convert binary Tensor to integer Tensor.
5) Repeat steps 2, 3, 4 for all input channels and sum the results across input channels.
6) Repeat steps 2, 3, 4, 5 for output channels (filters).
7) Summation on input Tensor across channels to find scaling factor.
8) Scalar Multiplication of output result from (5) with \( \alpha \) and scaling factor.

3.2.1. Converting Integer to Binary. The input and image tensors are stored inside registers with unsigned long data type to fully utilize 64-bit CPU registers and benefit from 64-bit operations. Each 64-bit register can hold 64 data elements of a 8 \times 8 matrix. Hence, the input image is divided into 8 \times 8 tiles, each of which is then stored in a single register in binary form. The pseudo-code is provided in Algorithm 1.

### Algorithm 1 Input Image to Binary Image

```plaintext
for j < IMAGE_HEIGHT do
  for i < IMAGE_WIDTH do
    register_image = input_image[j][i] >> Shift
    Shift += 1
  if i mod registerx == 7 then
    i = i - (kernel_sizex - 1)/2
  end if
end for
for j < IMAGE_HEIGHT do
  if j mod regisy == 7 then
    j = j - (kernel_sizey - 1)/2
  end if
end for
```

The theoretical speed-up that can be achieved for this part is 58x for 1 \times 1 kernel size [2]. However, networks used in computer vision use larger kernel sizes to have a receptive field, hence convolutions with larger kernels are needed in practice. In this work, we use a kernel size of 3 \times 3 which results in a more modest speed-up as it necessitates an iterative approach. In [7], convolution kernel weights fill every bit inside a register. For 1 \times 1 kernel size, this involves copying the same sign value for each bit in register. When 3 \times 3 convolution kernels are used, XNOR convolution can not be applied to each of the bit-pixel value since bits at the edge of the registers will require padding. Hence in our implementation, the weight register only contains one meaningful weight value and the other \( \text{Register\_image\_size} - \text{kernel\_size} \) bits are masked by bitwise AND operation.
3.2.2. Binary Convolution. In this part, CPU registers are used since there is up to \( 36 \times \) iterative access to the same register. The pseudo-code is given in Algorithm 2.

3.2.3. Binary Image to Integer Image. Each convolution result is stored inside a single 64-bit register. To convert the convolution result into integer value, the total number of 1s in the register need to be counted. This can be done by using the special built-in function \_builtin_popcount of the GCC compiler, which performs this operation more efficiently than hash mapping.

3.2.4. Multiplication by Scaling Factor. This part is done as described in [X, 22].

3.3. Binary Convolution on GPU

In convolution, XNOR operation and scaling factor calculation are independent, hence they can be run asynchronously in two different CUDA streams. The GPU implementation has the following steps running in two different streams:

Stream 1:
1) Apply zero padding to the Tensor (3D).
2) Convert the tensor and weights to binary type.
3) Apply bit-wise XNOR operation on binary Tensor.
4) Convert binary Tensor to integer Tensor.

Stream 2:
1) Summation on input Tensor across channels to find scaling factor.
2) Scalar Multiplication of \( \alpha \) and scaling factor.

3.3.1. Input Scaling Factor. For calculating the scaling factor of input, the average of channels is taken and convolved with 2D filter \( k \in \mathbb{R}^{w \times h} \) as in Eq. (10). It includes 2 steps: averaging across channels and convolution. For summation, each thread calculates the sum of a pixel across channels.

Computing input scaling factor matrix includes the following steps after copying from host to device:
1) Set grid and block sizes.
2) Average pixels across input channels.
3) Execute memory specified CUDA function to compute kernel convolution.
4) Deallocate GPU memories.

3.3.2. Binary Convolution Operation. Main idea of algorithm is similar to the CPU version. However, while CPU registers are 64-bit, GPU registers are 32-bit and each register now holds a \( (8 \times 4) \) image tile rather than \( (8 \times 8) \) tiles. Each CUDA thread converts a \( (8 \times 4) \) image tile (stored in a single register) to binary in parallel. The total number of threads to launch can be calculated as in Eq. [12] where \( I_w, I_h, R_w, R_h, K_w, K_h \), represents the input image width, image height, register width, register height, kernel width and kernel height respectively.

\[
Total_t = \frac{I_w - R_w}{R_w + 1 - K_w} \times \frac{I_h - R_h}{R_h + 1 - K_h}
\]  

(12)

After converting the image batches to binary, XNOR convolution is applied on all input channels. Denoting the number of input channels and number of output channels by \#in_ch and \#out_ch respectively, a total of \#out_ch different convolutions (having different weights) are calculated for each input channel. For this purpose, two options were explored: (i) using a single kernel to calculate all \#out_ch binary convolutions on all input, (ii) using \#out_ch number of kernels calculating binary convolution for each output channel separately. The first approach results in better utilization as it uses the register space for the whole process without any need for copying the result to global memory. However, this approach prohibits parallelization on output channels. For each input channel, \#out_ch convolution operations needs to be calculated and these operations are executed by the same kernel thread iterating a loop for the \#out_ch times. Therefore, the second approach preferred. In that case, since conversion of integer image to binary image can be stored in global memory, multiple streams can access these data. As a result \#out_ch streams can be run asynchronously, resulting in better parallelization.

3.3.3. Multiplication by Scaling Factor. A straightforward multiplication of \( \text{convolution_result} \times K \times \alpha \) for each CUDA thread.

4. Experimental Evaluation

We have run the experiments on a system having Intel i7700 CPU with 4-cores and Nvidia GTX1080TI GPU. The time measurements take only the computation into account so memory operations like allocation, copying memory and deallocation are excluded.

### Table 1: Comparison of vanilla convolution with XNOR convolution on GPU (ms).

| Input Size   | Vanilla Conv. | XNOR Conv. | Speed-up |
|--------------|---------------|------------|----------|
| 256 × 256   | 0.062         | 0.024      | 2.57×    |
| 512 × 512   | 0.186         | 0.069      | 2.69×    |
| 1024 × 1024 | 0.671         | 0.252      | 2.66×    |
| 2048 × 2048 | 2.641         | 0.986      | 2.68×    |

### Table 2: Comparison of CPU and GPU performance for vanilla convolution (ms).

| Input Size   | CPU   | GPU    | Speed-up |
|--------------|-------|--------|----------|
| 256 × 256   | 3.437 | 0.061  | 56.34×   |
| 512 × 512   | 10.623| 0.186  | 57.11×   |
| 1024 × 1024 | 35.811| 0.671  | 53.37×   |
| 2048 × 2048 | 132.714| 2.641  | 50.23×   |
TABLE 3: Comparison of CPU and GPU performance for XNOR convolution (ms).

| Input Size   | CPU | GPU | Speed-up |
|--------------|-----|-----|----------|
| 256 × 256    | 0.743 | 0.0237 | 31.35× |
| 512 × 512    | 2.531 | 0.0092 | 36.57× |
| 1024 × 1024  | 10.068 | 0.2519 | 40.04× |
| 2048 × 2048  | 42.011 | 0.9859 | 42.61× |

For multi-core CPU implementation, OpenMP has been used. The sub parts that are explained above are made for single channel input matrices. For the GPU implementation, CUDA has been used. We observed that the performance was insensitive to block size, so the experiments have been conducted with a constant block size of 256. We have used a constant 3 × 3 kernel size throughout the experiments for both CPU and GPU versions. All the experiments have been repeated 100 times and average run-times have been calculated.

As shown in Table 1, GPU XNOR convolution provides a speed-up of 2.57× to 2.69× against GPU vanilla convolution. the speed-up remains fairly constant with different image sizes.

When CPU and GPU implementations are compared, it is observed that vanilla convolution has a speed-up of 50.25× to 57.11× on GPU (Table 2). XNOR convolution has a speed-up of 31.35× to 42.61× (Table 3) and speed-up increases with increasing input size due to better utilization of the GPU.

5. Discussion

While the GPU XNOR convolution implementation has better performance than the CPU XNOR and GPU vanilla counterparts, the speed-ups we observed were lower than those reported in [7]. It has to be noted that our design uses a single kernel for each logical operation and as such, lacks the ability to achieve 32× (assuming 32-bit registers) binary logical operation speed. So, further optimizations could leverage bit-wise parallelism. On the other hand, use of separate registers allows easier conversion from binary outputs to integers. XNOR convolution needs binarization of input and multiplication with scaling factor at the end. Converting integer input image values to binary values and restoring integer values from output of the XNOR convolution are costly operations as they require sequential write operation to modify each bit inside a register and read them after convolution. For a deeper network, this process may be optimized by passing the binary outputs to the next kernel without integer conversion.

XNOR convolution involves two processes that can run concurrently, which are computing scaling matrix K and binary convolution operation. As a future work, multiple streams can be used to overlap these operations.

6. Conclusions

We have implemented and optimized the XNOR convolution operation [7] used in binary convolutional networks on CPU and GPU and comparatively evaluated their performance. The experimental results show that up to 42.61× speed-up can be achieved on GPU compared to the multi-threaded CPU implementation.

We implemented the operations required for the whole inference path of the binary network (i.e. scaling factor calculation and multiplication, binary to integer and integer to binary conversion, XNOR convolution) and made the code publicly available at https://github.com/metcan/Binary-Convolutional-Neural-Network-Inference-on-GPU. However, it has to be noted that the operations other than XNOR convolution part are not optimized and developed for testing only. Hence, for a real-life deployment requiring high levels of performance, these parts also need to be optimized.

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