Cryogenic microwave loss in epitaxial Al/GaAs/Al trilayers for superconducting circuits

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Epitaxially-grown superconductor/dielectric/superconductor trilayers have the potential to form high-performance superconducting quantum devices and may even allow scalable superconducting quantum computing with low-surface-area qubits such as the merged-element transmon. In this work, we measure the power-independent loss and two-level-state (TLS) loss of epitaxial, wafer-bonded, and substrate-removed Al/GaAs/Al trilayers by measuring lumped element superconducting microwave resonators at millikelvin temperatures and down to single photon powers. The power-independent loss of the device is $(4.8 \pm 0.1) \times 10^{-5}$ and resonator-induced intrinsic TLS loss is $(6.4 \pm 0.2) \times 10^{-5}$. Dielectric loss extraction is used to determine a lower bound of the intrinsic TLS loss of the trilayer of $7.2 \times 10^{-5}$. The unusually high power-independent loss is attributed to GaAs’s intrinsic piezoelectricity.

Keywords: superconducting quantum computing, TLS loss, resonator, gallium arsenide, piezoelectricity

I. INTRODUCTION

The investigation of the electrical properties of dielectric materials and interfaces in the millikelvin-temperature and single-photon-power regime is a burgeoning field in superconducting microwave circuits and is critical to performance enhancement in superconducting quantum computing. In particular, epitaxially-grown dielectrics are of interest because crystalline materials with low defect density have the potential to exhibit lower two-level-system (TLS) loss, the dominant form of loss in high performance superconducting quantum circuits. In addition, the ultra-high vacuum environment used in epitaxial growth allows for lower TLS loss attributed to cleaner interfaces between materials.

The discovery of a low-loss superconductor/dielectric/superconductor trilayer would allow the implementation of scalable, high-performance quantum computing designs such as the merged-element transmon.

Because the epitaxial growth of GaAs and Al/GaAs heterostructures is well-established, GaAs is a natural candidate for epitaxial growth for superconducting quantum devices.

In this work, we measure the power-independent loss and TLS loss of epi-Al/GaAs/Al trilayers on Al$_2$O$_3$ made using a wafer bonding technique. To determine this loss, we perform cryogenic microwave measurements of lumped element superconducting microwave resonators with parallel plate capacitors formed from these trilayers. We demonstrate that these epitaxial films perform similarly to bulk GaAs in both high- and low-power regimes, and exhibit loss dominated by power-independent loss which we attribute to the intrinsic piezoelectricity of GaAs.

II. DEVICE DESIGN AND FABRICATION

The material under test is a 40 nm epi-Al/40 nm epi-GaAs/40 nm epi-Al trilayer with a 20 nm atomic-layer-deposited (ALD) Al$_2$O$_3$ bonding layer, bonded to...
TABLE I. Parameters extracted from cryogenic microwave measurements of lumped element resonators with Al/GaAs/Al parallel plate capacitors (Trilayer) and interdigitated capacitors (Planar). All measurements were performed in DR1 unless stated otherwise. Values are given with their 95% confidence intervals where available. $N$: number of inductor meanders. $f_0$: resonance frequency. $1/Q_{i,LP}$: inverse high power internal quality factor. $F_0^{TLS}$: resonator-induced intrinsic TLS loss. $1/Q_{i,HP}$: inverse low power internal quality factor. This value is reported if $F_0^{TLS}$ is unavailable. $1/Q_c$: inverse coupling quality factor. Resonator A (B) TLS fit determined critical number of photons $n_c = 50,000$ ($70,000$) and exponential constant $\beta = 3$ (0.37).

| Device Label | Sample | $N$ | $f_0$ (GHz) | $1/Q_{i,HP}$ ($\times 10^{-6}$) | $F_0^{TLS}$ ($\times 10^{-6}$) | $1/Q_{i,LP}$ ($\times 10^{-6}$) | $1/Q_c$ ($\times 10^{-6}$) |
|--------------|--------|-----|-------------|-------------------------------|-------------------------|---------------------------|-------------------|
| A            | Trilayer 1 | 7   | 7.41        | 48 $\pm$ 1                   | 64 $\pm$ 2              | -                         | 15.3              |
| B            | Planar 1   | 7   | 7.92        | 0.3 $\pm$ 0.1                | 6.2 $\pm$ 0.2           | -                         | 2.6               |
| -            | Trilayer 1 DR2 | 17  | 4.79        | 57.8                         | $\sim$ 18.3             | -                         | -                 |
| -            | Trilayer 1  | 9   | 6.39        | 108                          | -                        | $\sim$ 217               | 17                |
| -            | Trilayer 2  | 7   | 7.41        | 92.6                         | -                        | $\sim$ 110               | 163               |

An Al$_2$O$_3$ (0001) substrate. The interfaces are abrupt and epitaxial, and the GaAs is single crystalline as determined by transmission electron microscopy (TEM). More details on the growth, wafer bonding, substrate removal, and regrowth processes, as well as materials imaging and characterization, can be found in Ref. 12. Trilayer lumped element resonators (shown in Fig. 1) are patterned using a six-step lithography and etch process (Fig. 2). First, the top capacitor plate is defined using Megaposit MF26A developer to etch the top layer of Al (Fig. 2 (b)). Then, the GaAs is etched away with Transene GA300 wet etchant heated to 33 $^\circ$C (Fig. 2 (c)). A second MF26A etch is used to remove the next layer of Al as well as the AlO$_x$ bonding layer (Fig. 2 (d)). An undercut of the bottom capacitor plate is performed with Transene D Al Etchant (Fig. 2 (e)). Transene A Al Etchant is used to fully remove residual Al in large blank areas. Finally, a liftoff process of e-beam deposited Al is used to form the feedline and inductors (Fig. 2 (f)).

Auto-spun Megaposit SPR660 photosresist exposed using a maskless aligner is used for lithography in all but the liftoff step, where a trilayer of MicroChem PMMA A2, MicroChem LOR5A, and SPR660 are used. An oxygen plasma ash is used to prepare the surface prior to Al deposition.

The trilayer resonator design is similar to that in Ref. 15. The parallel plate capacitor is designed to have a 10 $\mu$m x 10 $\mu$m top plate and is connected to each end of the inductor by liftoff. The inductor is 15 $\mu$m in width with a gap between inductive meanders of 30 $\mu$m and inductor length varies by varying the number of meanders $N$ between 7 and 17, corresponding to resonance frequencies $f_0$ between 4.7 and 7.5 GHz. Coupling quality factors vary between roughly 10,000 and 100,000 in order to facilitate critical coupling.

About 17% of the total Al top electrode area is liftoff Al, not epi-Al. This could obscure the epi-Al/GaAs/Al loss if trilayer loss is much lower than liftoff interface loss. In addition, the capacitor undercut has an estimated participation of 6% based on the capacitance of that region. In future experiments, the undercut connection will be replaced by an airbridge in order to increase measurement sensitivity to the trilayer loss.

In order to take into account the effect of the inductor circuit element, trilayer resonator measurements are compared to those of planar resonators, for which the same inductor design is used but the trilayer is replaced by an interdigitated capacitor. Planar resonators are fabricated using liftoff e-beam Al on sapphire to imitate the inductor fabrication in the trilayer devices.

III. MICROWAVE MEASUREMENTS AND LOSS EXTRACTION

Samples are clamped into sample boxes made from gold-plated oxygen-free high thermal conductivity copper, with wirebonds used for electrical connection. Measurements are performed in two different cryogen-free dilution refrigerators (DRs): DR1, at a temperature of 12 mK, and DR2, at a temperature below 10 mK. Applied
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Fig. 3. Loss $\delta$ as a function of normalized number of photons in the resonator $\langle n_{\text{ph}} \rangle / n_c$ at $T \approx 12$ mK for resonators (a) A and (b) B, defined in Table I. Data is denoted as circles, and fitting to the total loss model in Eq. 1 is denoted as a solid line. Insets show representations of the measured devices.

Four trilayer resonators and one planar resonator were successfully measured, as shown in Table I and two were able to be fitted at sufficiently high and low powers as to allow TLS model fitting. These two devices are labeled device A (trilayer resonator) and device B (planar resonator). Measurements of the other trilayer resonators in Table I support the values seen in the measurements of device A.

Fig. 3 shows power sweeps of loss $\delta = 1/Q_i$, for resonators A and B as well as fits to the total loss model

$$\delta = \delta_{\text{TLS}}(T, \langle n_{\text{ph}} \rangle) + \delta_{\text{other}}(T),$$

where $\delta_{\text{TLS}}$ is TLS loss as defined in the following equation and varies with temperature $T$ as well as time-averaged number of photons in the resonator $\langle n_{\text{ph}} \rangle$, and $\delta_{\text{other}}$ is a sum of power-independent losses such as quasiparticle loss, vortex loss, and piezoelectric loss. The TLS model is given by

$$\delta_{\text{TLS}} = F\delta_{\text{TLS}}^0 \tanh \left( \frac{\hbar \omega}{2 k_B T} \right) \frac{\langle n_{\text{ph}} \rangle}{n_c},$$

where $\delta_{\text{TLS}}^0$ is the intrinsic TLS loss, $n_c$ is the resonator's critical photon number, $\beta$ is an exponential constant describing the homogeneity of the TLS population, and $F$ is the filling factor of the TLS material. The resonator-induced intrinsic TLS loss, $F\delta_{\text{TLS}}^0$, is the effective loss due to TLS in the low-power, low-temperature limit. TLS model fitting results for Fig. 3 are reported in Table I. $\langle n_{\text{ph}} \rangle$ is estimated using the resonator $Q_c, Q_i, f_0$, and total power, as in Ref. 19.

At high power, where TLS are saturated and power-independent losses dominate, $\delta = 1/Q_i, HP \sim \delta_{\text{other}}$ where $1/Q_i, HP$ is the inverse high power internal quality factor. In this regime, the loss of trilayer resonator A is $(4.8 \pm 0.1) \times 10^{-5}$. This value is only a factor of two different than the loss at low powers (Fig. 3 (a)), demonstrating that power-independent loss sources dominate the total loss of this device. Indeed, this high-power loss is more than an order of magnitude higher than expected, as shown by comparison to a power sweep of resonator B (Fig. 3 (b)), which does not contain an Al/GaAs/Al trilayer. This unusually high loss in the high-power regime is demonstrated repeatably with four trilayer devices on two chips across multiple cooldowns, as shown in Table I.

The high-power loss in this work is within a factor of 3 of the piezoelectric loss measured in bulk GaAs. We believe that this unusually high high-power loss can also be attributed to piezoelectricity. Quasiparticle and vortex loss are unlikely to vary so significantly between samples measured using the same experimental set-up, such as resonators A and B. Another possible materials loss that would present at high-power is loss due to interdiffusion between the Al and GaAs epitaxial layers. This can be ruled out by interface TEM images in Ref. 12 that show these interfaces as abrupt and epitaxial.

The resonator-induced intrinsic TLS loss in resonator...
A is $(6.4 \pm 0.2) \times 10^{-5}$. We can determine a lower bound for the intrinsic TLS loss of the Al/GaAs/Al trilayer, independent of the effect of the resonator wiring, by implementing a modified version of dielectric loss extraction. Details on the simulations used can be found in the supplementary material for Ref. [15]. The resonator-induced intrinsic TLS loss in device A, $\delta_A = F_A \delta_{\text{TLS,A}}^0$, where $F_A$ is the filling factor of the TLS material in device A, is a weighted sum of intrinsic TLS loss in the planar inductor $\delta_L$ and the Al/GaAs/Al trilayer capacitor $\delta_{\text{Al/GaAs/Al}}$, as:

$$\delta_A = \frac{C_L}{C_{\text{tot}}} \delta_L + \frac{C_C}{C_{\text{tot}}} \delta_{\text{Al/GaAs/Al}},$$  \hspace{1cm} (3)

where $C_L$ ($C_C$) is the capacitance of the inductor (capacitor) circuit component, and total capacitance is $C_{\text{tot}} = C_L + C_C$. If we assume all TLS loss in planar resonator B is from the inductor, which is identical in design to the inductor in device A, then $\delta_B = \delta_L$. We can then determine a lower bound on the loss of the epitaxial Al/GaAs/Al trilayer by

$$\delta_{\text{Al/GaAs/Al}} = \frac{C_{\text{tot}}}{C_C} (\delta_A - \frac{C_L}{C_{\text{tot}}} \delta_B)$$  \hspace{1cm} (4)

with trilayer capacitance $C_C = 285 \text{ fF}$ and inductor capacitance $C_L = 37.5 \text{ fF}$, as determined by analysis and simulation, and loss values shown in Table I. For a parallel plate capacitor, $F = 1$, so we can say $\delta_{\text{Al/GaAs/Al}} = \delta_{\text{TLS,Al/GaAs/Al}}^0$.

From Eq. [3] we determine that $\delta_{\text{Al/GaAs/Al}} = 7.2 \times 10^{-5}$, slightly higher than the resonator-induced TLS loss for device A, $\delta_A = (6.4 \pm 0.2) \times 10^{-5}$, verifying that the TLS loss of device A is dominated by the Al/GaAs/Al trilayer. This value includes the loss of the undercut region, the liftoff Al on the capacitor, and capacitor edge effects, which could increase the effective loss. Even so, these values agree within a factor of two with bulk GaAs TLS loss measurements.[10]

For a target qubit lifetime of 50 to 100 $\mu$s, losses must fall within the mid-$10^{-7}$ range. Thus, the measured loss in this materials set in both the high- and low-power regimes is too high for superconducting qubit applications. However, power-independent and TLS losses may be lower in other similar epitaxial trilayers such as Al/Si/Al and Al/Ge/Al, which will be explored in future work.

IV. CONCLUSION AND NEXT STEPS

Due to the presence of significant power-independent loss in thin epitaxial Al/GaAs/Al trilayers, GaAs can be ruled out as a promising dielectric material for superconducting quantum computing applications unless mitigation methods are implemented. In the future, similar growth, fabrication and measurement techniques could be applied to other promising, non-piezoelectric materials sets such as epi-Al/Si/Al trilayers, and could yield substantial performance enhancement.

In future materials measurements of this type, the replacement of the undercut connection with an airbridge could reduce loss from this region and increase measurement sensitivity. In addition, the variation of capacitor size and thickness could allow the extraction of losses for individual regions within the capacitor such as the superconductor/dielectric interfaces and the superconductor and dielectric surfaces.

DATA AVAILABILITY

The data that support the findings of this study are openly available in Boulder-Cryogenic-Quantum-Testbed/data at http://doi.org/10.5281/zenodo.4025406

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