Capacitance–Voltage (C–V) Characterization of Graphene–Silicon Heterojunction Photodiodes

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Heterostructures of two-dimensional (2D) and three-dimensional (3D) materials have been proposed for various technological applications thanks to their simple device architecture and easy fabrication. Heterostructures of Graphene (G) and silicon (Si) can form Schottky diodes and have been demonstrated in different electronic devices, such as chemical and biological sensors,[1–3] rectifiers,[4] solar cells,[5–8] and photodetectors.[9–24] Their thorough characterization is an important subject for the graphene device research community. In particular, it is essential to define precise methods for electrical characterization of the Schottky junctions in order to understand the current transport mechanism in G/Si Schottky diodes, including their similarities and differences with conventional semiconductor technology. To this end, a number of theoretical and experimental studies have been carried out on G/Si Schottky junctions.[19–30] Important diode parameters such as ideality factor (n), Schottky barrier height (SBH), and series resistance (R_s) have been obtained from current–voltage (or rather: current density–voltage, J–V) and capacitance–voltage (C–V) measurement techniques. Many of these studies have reported varying values for n, SBH, and R_s.[19–27] The variations are often attributed to different measurement and fabrication techniques. We have demonstrated in our previous work[22] that in G/Si diodes, the Schottky junction is typically connected in parallel to a graphene/silicon dioxide/silicon area, that have been termed graphene/insulator/semiconductor (GIS) region. This GIS region is essentially a metal–insulator–semiconductor (MIS) capacitor.[22,31] The detailed role of this parallel GIS capacitor has frequently been neglected when analyzing the electrical characteristics of the G/Si diodes.

In this work, we introduce a method for accurate C–V characterization of G/Si heterojunctions with a parallel GIS capacitor. To evaluate the effect of the GIS capacitor, we performed C–V measurements at small AC signal on G/n-type silicon (n-Si) Schottky diodes with varying dimensions of the GIS region and on a reference capacitor without Schottky junctions. From these measurements, we propose a methodology to extract the built-in potential (Φ_b) and the SBH. Figure 1a shows schematics of two G/n-Si diodes, D1 and D2, with varying GIS areas. J–V characteristics of both diodes under dark condition are displayed in Figure 1b in a semi-logarithmic scale. In order to calculate the current density, the measured current is normalized to the G/Si Schottky area, which is marked with a dashed red line in Figure 1c. In the voltage range –2 to +2 V, both diodes exhibit rectifying characteristics in the dark with rectification ratios up to 3.8 × 10^4 and 2.94 × 10^4 for D1 and D2, respectively. The basic parameters of the diodes such as n, SBH, and R_s are obtained from the forward J–V characteristics in dark condition using the Cheung method.[32] For D1 and D2, n of 2.08, and 2.3, SBH of 0.76 and 0.79 eV and R_s of 24 and 14 kΩ have been extracted, respectively. Details of the calculation of the diode parameters are described in our previous work[27] (see Figure S2, Supporting Information therein). It should be noted that the extracted values of SBH slightly differ from the true SBH of the devices. This is because the theoretical value of the Richardson constant (A') for n-Si (112 A cm⁻² K⁻2) was considered in order to obtain the SBHs.[27] For standard Schottky junctions, where a 3D metal is in contact with Si, the Richardson constant is typically estimated by considering the velocity vector component of electrons normal to the barrier plane and with a kinetic energy greater than the barrier height. For 2D-graphene on silicon, the electron is locked-up between a potential well, on one side constituted by electron affinity of the graphene layer, and on the other side, by the silicon energy barrier. Trushin suggested that the current across the G/Si
The barrier can be estimated by considering the tails of electron wave functions pointing into the n-Si conduction band. This motivates a much lower effective Richardson constant than that of 3D-metal/Si junctions. It is then clear from the expression for the reverse saturation current of the thermionic emission model, that a lower Richardson constant results in a slightly lower value of SBH. Thus, in order to obtain a value for SBH with high precision, the Richardson constant must be appointed with care. We have therefore performed C–V measurements to obtain SBH values of devices independent of the Richardson constant. A common approach to estimate the Schottky barrier height and the Richardson constant is the use of the so-called Richardson plot obtained from J–V characteristics at different temperatures, as done in [34,35].

C–V measurements were performed on both devices under study (D1 and D2) and on a test structure (D_test—see Figure 2a) at 10 kHz AC-signal frequency. D_test consists of a MIS and a GIS capacitor in a parallel (Figure 2b). The structure is made...
of chromium (Cr)/nickel (Ni) pad in contact with the graphene electrode, 20 nm thick SiO₂ as insulator and n-Si as semiconductor. As shown in Figure 2a, the MIS bulk contact in D_{test} is located on the top side of the Si chip, similar to D₁ and D₂. Figure 2c displays the measured C–V characteristics of D_{test} in comparison with a theoretical one for an ideal MIS capacitor. The curves have been normalized for easier comparison in the voltage range from −4 to 4 V. Such a comparison allows one to extract the flat-band voltage (V_{FB}) and threshold voltage (V_{th})—the voltage at which the inversion happens—for our non-ideal MIS+GIS structure. The procedure further provides information on the presence of imperfections such as trapped charges in the SiO₂ and/or at the Si/SiO₂ interface. For an ideal MIS capacitor, the oxide/semiconductor interface charges (Q_{it}), the oxide charges (Q_{ox}), and the energy difference between the work function of the metal and n-type semiconductor (Q_{ms}) are all assumed to be zero. The theoretical C–V plot is calculated using N_D = 2 × 10^{15} cm⁻³, t_{ox} = 20 nm, ε_{ox} = 3.9, and ε_S = 11.9, where N_D is the doping concentration of the Si, t_{ox} is the thickness of the SiO₂, ε_{ox} is the permittivity of the SiO₂ and ε_S is the permittivity of the Si. As indicated in Figure 2c (dashed line), V_{FB} and V_{th} for an ideal MIS structure are 0 and −0.6 V, respectively. We observed a 0.4 V positive shift for V_{FB} and V_{th} of the test structure, which indicates the presence of trapped negative charges in the SiO₂. The observed decrease in the capacitance values of the test structure when the semiconductor is in accumulation originates from the high series resistance due to the MIS bulk contact positioned on the top side of the Si chip and at a fairly long distance from the Si/SiO₂ interface.

Small-signal C–V characteristics of the devices under study (D₁ and D₂) in comparison with the test device are shown in Figure 3a. Both D₁ and D₂ display similar C–V characteristics and can be modeled with an equivalent circuit model, containing a Schottky junction diode in parallel with the GIS and MIS capacitors (see up right inset of Figure 3a). The capacitance due to the metal–Si contact (bulk contact) is neglected as the contact is believed to be ohmic. For forward bias voltages (V_{bias}) above Φ_{bi} (calculated below), both diodes are in on-state and the depletion width in the Schottky junction is strongly reduced. Therefore, the Schottky junction capacitance is boosted, resulting in a strong increase in the measured capacitance. The decreasing capacitance in the range of −0.6 V to qΦ_{bi} (Figure 3a) due to the growing depletion layer capacitance (C_{depletion}) of the G/Si junction that overcomes the MIS+GIS capacitance. For V_{bias} < −0.6 V, the bias-independent capacitance shows that the MIS+GIS junction, which is now in deep inversion, dominates the Schottky diode. Therefore, V_{th} for both devices (D₁ and D₂) is around −0.6 V. At this voltage range,
the MIS+GIS junction capacitance \( C_{\text{MIS}} + C_{\text{GIS}} \) of \( 1.8 \times 10^{-9} \) and \( 2.4 \times 10^{-9} \) F cm\(^{-2}\) is calculated for D1 and D2, respectively. These values are calculated using the test device (the second part of Equations (4) and (5)). For a clear visualization of the low capacitance part of the curves, the comparison among the C–V characteristics of D1, D2, and D\(_{\text{test}}\) is shown in semi logarithmic scale in Figure 3b.

\( \Phi_{\text{bi}} \), SBH, and \( N_D \) of the devices can be determined from the measured C–V data. Generally, the extracted SBH is expected to be equal to somewhat higher than the SBH estimated from J–V measurements due to spatial inhomogeneities which affect mainly the SBH from J–V measurements\([36]\). The estimated value for \( N_D \) should be in the same range as the doping density of the Si substrate used to fabricate the devices. The relation between C and \( V_{\text{bias}} \) can be expressed by Equation (1) for a non-ideal Schottky diode with an ideality factor \( n \) and an interfacial oxide layer between the metal and the semiconductor\([37]\):

\[
\frac{1}{C^2} = \frac{2n}{qeN_D} \left( \frac{k_B T}{q} + V_{\text{bias}} - \Phi_{\text{bi}} \right)
\]  

where \( q \), \( T \), and \( k_B \) are the elementary charge, the absolute temperature, and the Boltzmann constant, respectively. Hence, a linear graph is expected when plotting \( 1/C^2 \) versus \( V_{\text{bias}} \) for a Schottky junction with a constant \( N_D \) within the depletion layer. In addition, the SBH can be obtained using Equation (2)\([37]\):

\[
\text{SBH} = q \left( \frac{\Phi_{\text{bi}}}{n} + \frac{k_B T}{q} + \Phi_n - \Delta \Phi \right)
\]

where \( \Delta \Phi \) is the effect of SBH lowering and \( \Phi_n \) is the potential difference between the conduction band and Fermi level of Si. \( \Phi_n \) can be estimated using Equation (3)\([34]\):

\[
\Phi_n = k_B T \ln \frac{N_C}{N_D}
\]

where \( N_C \) is the effective density of the states in the conduction band of Si, which is equal to \( 2.8 \times 10^{16} \) cm\(^{-3}\).

Devices D1 and D2 feature combined G/Si, GIS, and MIS structures. Thus, the contribution of the GIS and MIS capacitors must be deducted from the measured capacitance in order to obtain the capacitance of the Schottky junction (G/Si). Afterwards, \( \Phi_{\text{bi}} \) and \( N_D \) can be extracted from the intercept on the \( V_{\text{bias}} \)-axis and the slope, respectively, of the “1/C\(^2\) versus \( V_{\text{bias}} \)” plot. Then, the SBH can be calculated using Equation (2). To obtain the C–V characteristics of the Schottky junction, we assumed that the MIS and GIS capacitors of the present devices behave similar to that of the test structure. Therefore, the Schottky junction capacitance for D1 and D2 can be estimated with Equations (4) and (5):

\[
C_{\text{SK1}} = C_{\text{lat1}} - \frac{A_1}{A_{\text{Dtot}}} \times C_{\text{Dtot}}
\]  

\[
C_{\text{SK2}} = C_{\text{lat2}} - \frac{A_2}{A_{\text{Dtot}}} \times C_{\text{Dtot}}
\]

where \( C_{\text{SK1}} (C_{\text{SK2}}) \) is the Schottky junction capacitance of D1 (D2), \( A_1 (A_2) \) is the area of GIS+MIS area in device D1 (D2), \( A_{\text{Dtot}} \) is the total area of the test device, which is equal to the graphene area plus area of the metal electrode connected to graphene, and \( C_{\text{Dtot}} \) is the measured capacitance of the test structure.

The “1/C\(^2\) of Si as estimated from the “1/C\(^2\) versus \( V_{\text{bias}} \)” plots for both devices D1 and D2 is shown in Figure 3b. It exhibits the linear characteristics expected for a Schottky junction. \( N_D \) of Si as estimated from the slopes of the plots, is \( 2 \times 10^{15} \) and \( 2.7 \times 10^{15} \) cm\(^{-3}\) for D1 and D2, respectively. These values are within the range of the doping concentration specified for the Si wafer (between \( 2 \times 10^{14} \) and \( 4 \times 10^{15} \) cm\(^{-3}\)). Using Equation (3), we calculated \( \Phi_n = 0.24 \) V for D1 and \( \Phi_n = 0.23 \) V for D2. Moreover, \( \Phi_{\text{bi}} \) values of 0.44 V for D1 and 0.47 V for D2 can be extracted from the intercept on the \( V_{\text{bias}} \)-axis in Figure 3d. Finally, SBH of the devices were obtained by applying Equation (2) and using ideality factors determined from the J–V measurements. SBH values of 0.68 and 0.70 eV were extracted for D1 and D2, respectively. Here, we have neglected the SBH lowering effect (\( \Delta \Phi \)) in our calculations since the reverse saturation current densities are almost constant in both diodes (see Figure 1c). It should be noted that the SBHs determined from the C–V measurements are about 0.1 eV less than those extracted from the J–V measurements, although we would have expected them to be slightly higher based on the inhomogeneities as discussed above. We attribute this small difference to the literature value of the long-term (112 A cm\(^{-2} \) K\(^{-2}\)) considered when calculating the SBHs from the J–V measurements. A\(^{\text{exp}}\) for G/Si junctions are expected to be smaller than this value considered and that will result in a smaller SBH. We therefore believe that this small difference between the SBHs extracted from J–V and C–V measurements would vanish when using the correct value of A\(^{\text{exp}}\). The observed 0.1 eV inconsistency between the results from the two methods is not that significant when one accounts for experimental errors in electrical measurements in general. Nevertheless, we believe that the SBH extraction from C–V measurements is currently more precise and more reliable than the J–V method, as the latter is influenced by the choice of the effective Richardson constant value, which is not yet clearly known for G/Si Schottky junctions.

C–V measurements were performed on G/Si Schottky diodes with inherent parallel GIS and MIS capacitors. We introduced a method for precisely evaluating the C–V characteristics of these structures. The method provides an alternative way of determining the Schottky barrier height and can be used to crosscheck the consistency of values obtained from analyses of measured J–V data, which may be prone to errors because of an unclear exact value of the A\(^{\text{exp}}\).

**Experimental Section**

**Device Fabrication:** A phosphorus-doped Si wafer with a resistivity of 1–20 Ω cm was used as the initial substrate. Then, 20 nm SiO\(_2\) has been grown on the Si surface using a thermal oxidation process and the wafer has been diced into 20 × 20 mm\(^2\) chips. The n-Si substrate was then partially exposed by etching the SiO\(_2\) layer using buffered oxide etchant (BOE) after a first UV-photolithography step. This step was not performed for the fabrication of the test structures. Afterwards, metal...
electrodes have been formed through a second photolithography step, followed by the deposition of (15/85 nm) Cr/Ni and a liftoff process. Large-area graphene was grown on a copper (Cu) foil in a Moorfield NanoCVD rapid thermal processing tool using the chemical vapor deposition (CVD) method.[8] A polymer-supported wet chemical etching transfer technique was used to transfer graphene films onto the pre-patterned substrates immediately after native oxide etching in BOE to ensure a pure G/Si Schottky junction for the diodes.[9] During transfer, the graphene on Cu foil was spin-coated with Poly methyl methacrylate (PMMA) and baked for 5 min at 85 °C. After cutting it into ≈7 mm² pieces, Iron (III) chloride (FeCl₃) was used to etch the Cu foil and the polymer-supported graphene films were rinsed in HCL followed by DI-water. Then, the chips were baked on a hotplate for 35 min at 180 °C, followed by removal of the PMMA layer in hot acetone (55 °C) for 1 h. Afterwards, they were cleaned with isopropanol and dried with nitrogen. Finally, graphene was patterned through a last photolithography step, followed by etching of graphene in oxygen plasma.

Electrical Characterization: J–V measurements were performed on the diodes using a Karl Süss probe station connected to a Keithley semiconductor analyzer (SCS4200) under ambient condition. The voltage was swept from 0 to +2 V for forward (Vf) and from 0 to −2 V for reverse (Vr) biasing, for all the diodes. C–V measurements were carried out using the same probe station connected to an HP Impedance Analyzer (HP 4294A). The measurements were performed using a small AC signal amplitude of 25 mV at 10 kHz frequency superimposed to a DC bias voltage, which was −25 mV at 10 kHz frequency superimposed to a DC bias voltage, which was

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

capacitors, graphene, Richardson constant, Schottky barrier height, Schottky diodes

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