Hardware Support for FPGA Resource Elasticity

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Abstract—FPGAs are increasingly being deployed in the cloud to accelerate diverse applications. They are to be shared among multiple tenants to improve the total cost of ownership. Partial reconfiguration technology enables multitenancy on FPGA by partitioning it into regions, each hosting a specific application’s accelerator. However, the region’s size can not be changed once they are defined, resulting in the underutilization of FPGA resources. This paper argues to divide the acceleration requirements of an application into multiple small computation modules. The devised FPGA shell can reconfigure the available PR regions with those modules and enable them to communicate with each other over Crossbar interconnect with the Wishbone bus interface. For each PR region being reconfigured, it updates the register file with the valid destination addresses and the bandwidth allocation of the interconnect. Any invalid communication request originating from the Wishbone master interface is masked in the corresponding master port of the crossbar. The allocated bandwidth for the PR region is ensured by the weighted round-robin arbiter in the slave port of the crossbar. Finally, the envisioned resource manager can increase or decrease the number of PR regions allocated to an application based on its acceleration requirements and PR regions’ availability.

I. INTRODUCTION

With the advent of 3D ICs based on Stacked Silicon Interconnect (SSI) technology, the FPGA manufacturers are offering devices that are very rich in resources. Dedicating one large FPGA to a single user leads to poor utilization of the FPGA resources and a drastic increase in the infrastructure cost. To alleviate this, several proposals exist to support multitenancy on FPGAs, where FPGA’s internal resources are statically divided into multiple partitions [1]–[10], each of which can be dynamically re-configured with the bitstreams using partial reconfiguration technology. The partial bitstreams of the requested accelerator are either made available by the framework in the database [1], [3], [6], [7] or generated at runtime [2], [5], [8]–[12] by synthesizing the user-provided accelerator files described at RTL level, OpenCL or HLS level. The solutions target different CPU-FPGA architectures; i) PCIe attached FPGA [1], [3], [5]–[7], [9], [11], [12], ii) Network-attached FPGA [2], [8], [13], [14] and iii) System on Chip comprising of ARM CPUs and programmable logic [10]. They provide isolation among multiple processes [3], [5], [9], OpenCL tasks [10] and virtual machines [1], [2], [6], [11], [12], which are orchestrated via OpenStack.

Nevertheless, partially reconfigurable (PR) regions are fixed in size; it is not possible to dynamically increase or decrease the resources of PR once it is defined. This can lead to either underutilization of resources or not having PR regions large enough to host the application. In other words, the PR region might contain much more resources compared to the acceleration requirements of the application; thus, wasting some resources. On the other hand, it might also be the case that the application requires more resources than any PR region has; thus, not being able to host it. Therefore, the question is how to dynamically adjust PR regions accordingly to the application’s needs. While outlining our proposal, we make following contributions:

• We provide a system architecture that enables expanding and contracting the FPGA resources allocated to an application by expressing application accelerators into multiple smaller computation modules. These modules are configured into multiple reconfigurable regions as assigned to the application dynamically. Next, it provides a low-area-overhead, configurable, and isolated communication mechanism among those reconfigurable regions by adjusting the crossbar interconnect and WISHBONE (WB) interface.

• Compared to the prior-art [15], our communication mechanism among PR regions is area efficient, i.e. consumes 61% fewer lookup tables (LUTs) and 95% fewer flip-flops (FFs). It also improves the latency to complete the request by 69%.

II. BACKGROUND

A. Multiprocessor Interconnection Methods

Crossbar and Network-on-Chips (NoCs) are more effective ways of interconnection among multiple processors or chips compared to the shared bus. Since only one processor can access the bus at a time, a shared bus results in limited bandwidth and increased latency.

Fig. 1: Multiprocessor Interconnection on a Chip

(a) 3x3 NoC with Mesh Topology  (b) 4x4 Crossbar Switch
1) NoCs: Inspired by computer networks, in this scheme each module is considered as a node and has a router; then, routers are connected following one of the network topologies such as mesh (see Figure 13), torus, butterfly, and so on. To communicate, a node (represented in red) directs its data to its router (shown in green) and the router divides data into packets and forwards them into the next router. Thus, a packet travels through several routers until it reaches its destination. Routers can use either routing algorithms (random, weighted random, adaptive, etc.) or routing tables to decide which path to follow [16]. Since there are multiple paths and routers available in network topology, parallel transmissions can happen.

2) Crossbar Switch Interconnection: It consists of switches arranged in a matrix form and connects the source module to a destination. As displayed in Figure [15] all modules are connected to a common set of bus lines; however, their communications are prevented by switches illustrated as blue boxed. A master can initiate a request, upon which necessary switches are enabled to recover the physical link between a master and destination slave. Since there exist separate bus lines for each destination, in crossbar interconnection it is possible to do the parallel transmission.

The crossbar switch is more flexible and scalable than the shared bus; however, less than NoCs. The flexibility and scalability result in increased resource usage for crossbar switch compared to shared bus [17]–[19] but it still consumes less area resource than NoCs. In other words, it stays in the middle of the trade-off between area and flexibility/scalability. Its area usage mainly comes from its arbitration logic [19]. Crossbar can support parallel transmissions without incurring the protocol overhead as in NoCs. It can also demonstrate adequate latency and throughput in pipelined and global communication patterns [20].

B. WISHBONE Interconnection Architecture [17]

It enables increased reusability of IP cores in system-on-a-chip, connected in one of the supported communication interconnection modes (point-to-point, shared bus, data flow, and crossbar [17]), by providing standard data exchange protocol. This protocol is implemented as bus interfaces. The interface operates with master-slave logic, where the master can initiate either read or write requests to a slave. For high throughput, a master sends all data if a slave has not asserted stall and then waits for acknowledgments from a slave.

WB interconnection has small design complexity and therefore, it can operate in high frequencies while consuming less area [17] and energy [18]. Hardware modules can be adapted easily to interact with it, thereby increasing the re-usability of the interconnection architecture. Moreover, it has a built-in handshaking protocol, eliminating the need for extra logic to ensure transmission safety.

III. RELATED WORK

Prior art on supporting resource elasticity inside the FPGAs [10] provide various implementations consuming different amount of resources in reconfigurable region for each application. Next, it selects kernel versions and number of instances based on the fairness of resource allocation for each application and reconfigures the FPGA. It relies on bitstream manipulation to change the location of a module, increase/decrease allocated resources, etc. However manipulating bitstreams is device specific as different FPGA devices have different bitstream file formatting.

There exists several communication schemes in the literature to allow interaction among the partially reconfigurable regions. For example, a pipelined shared bus architecture with encapsulated WB (E-WB) interface for PR regions and 5-layer communication protocol [21]. Another technique [15] proposes NoCs among virtual regions. The network offers bufferless routers with no virtual channels. However, each virtual region contain additional access monitor, wrapper, registers, and the communication interface with buffers beside the partially reconfigurable module. A different strategy explored in [22] extends reconfigurable multiple bus on chip for NoCs to overcome extra communication overhead. It provides physical communication link between a source and destination of NoCs’ nodes. The link is divided into multiple bus segments, controlled by bus controllers deployed for each section.

The studies aforementioned, either based on NoCs [16], [23], [24] or shared bus [21] can potentially expand or contract the FPGA resources allocated to application. Nevertheless, those architectures have several disadvantages. The shared bus method is neither flexible in supporting different communication patterns and parallel transmissions nor scalable to higher number of modules due to its bandwidth limitations. On the contrary, NoC’s large network protocol overhead, area usage and power consumption are disadvantageous [18], [25].

IV. OUR DESIGN

Our approach enables resource elasticity in the FPGA by providing effective communication method among PR regions. A user’s request for acceleration is expressed in the form of small computational modules, which are partially reconfigured to small-sized regions. This would improve resource under-utilization. By allocating extra PR regions if needed and enabling them to communicate using WB Crossbar Switch interconnection (see Figure 2), the number of allocated resources to the application can be also increased.

Our solution enables dynamically changing FPGA PR region resources allocated to the application. It provides an easy way of managing communication isolation for different user requests and provides a simpler way of handling dynamic bandwidth allocation inside the FPGA device. It has low area usage due to optimized implementation. It incurs low communication or protocol overhead and is flexible to be used with different hardware modules due to the usage of the standard interface.

A. FPGA Elastic Resource Manager:

User requests are sent to the FPGA Elastic Resource Manager which keeps track of PR regions that are available and the regions are allocated to specific user’s application. The
manager analyzes the user request in terms of required PR regions to handle it and then, reconfigure the particular regions in the FPGA accordingly. Furthermore, it also sends user data to PR regions, provides configuration information to and recovers status information from the register file.

Here is how reconfiguration and elasticity are achieved. The manager allocates the available amount of PR regions to the application’s computation modules through the internal configuration access port (ICAP). If there are not enough PR regions to host all modules, the remaining ones run on the server (referred to as on-server modules). Then, the manager provides configuration data to PR regions and the crossbar such as allowed modules, destination modules, and allowed number of packages. In this phase, the last module’s destination address is sent back to the server for the purpose of receiving its results and continuing the computation on the server. Afterward, it sends user data to start the computation process. When the on-server module finishes its computation, the FPGA manager checks again if there are any PR regions released so that it can run the on-server module on the FPGA, as well. If so, then it reprograms the available PR region with the on-server module and updates the other module’s destination addresses so that they communicate with the newly available module, as well. Thus, resource elasticity is achieved; the allocated resource for the user is increased by the means of communication interconnection among PR regions.

B. XDMA IP Core & ICAP:

Since the AXI-ST interface allows using each channel of XDMA (Xilinx Direct Memory Access) IP core [26] separately, the design dedicates a separate channel to continuously stream partial bitstreams over the PCIe bus to saturate ICAP bandwidth [27]. Moreover, FIFO is added before the ICAP to prevent data loss due to a mismatch in the clock frequency of ICAP (125 MHz) and of the rest of the system (250 MHz). Likewise, a separate AXI-Lite bypass link is enabled to access the register file to avoid interference between users’ application data and configuration information.

C. Reset System

Global reset is provided by buffering asynchronous reset signal of XDMA IP core. On the other hand, resets for computation modules and their associated crossbar ports are fetched from the register file, thus during the partial reconfiguration process, the module can be isolated from the rest of the system and the crossbar port would be prevented from making any grant decisions.

D. Register File:

The register file plays an important role in providing configuration data and storing necessary status information. Configuration data consists of the number of packages each module can send to each other and the destination address of each module. Firstly, when ICAP does reconfiguration of PR regions it stores the status data on the register file regarding whether the reconfiguration process was successful or failed. Secondly, the WB Crossbar switch and PR regions are served by the register file, too. For the crossbar, the purpose of having the register file is to provide the allowed bandwidth to applications and to enable communication isolation. Moreover, error codes marking communication failure due to either wrong destination address or timeout due to unresponsive destination are also registered. Finally, reset signals for PR modules are provided through the register file too.

E. Crossbar Switch Architecture

Figure 2 shows each crossbar port consists of 2 different parts; these are called master and slave ports accordingly. The block diagrams of those ports are displayed in Figure 3 considering four-by-four crossbar interconnection.

1) Slave Port: A slave port is responsible for giving grants based on requests coming from master ports. It also keeps the track of exchanged package numbers between a slave and a master. Additionally, it informs a master about the given grant and enables a slave for communication. This is done via an arbiter in each slave port serving masters, making the
 circulation logic in this crossbar architecture decentralized. Finally, it connects granted master’s data signals to a slave interface through multiplexers.

**Arbitration Logic – Weighted Round Robin:** To support bandwidth requirements of different accelerators, we propose Weighted Round Robin (WRR) arbiter based on leading zero counters (LZC) [28], which operates at higher frequencies and has less area overhead [29] compared to priority encoders based arbitration logic.

The arbiter ensures the customized bandwidth allocation. It tracks the number of packages rather than the time period via package counter, which looks up the registers holding the maximum number of packages each master is allowed to send. When the maximum number of packages is reached, it switches the grant to the next master. Having a decentralized arbitration scheme simplifies the arbiter logic and management of multicast data transmission.

2) **Master Port:** It receives a communication request from a master interface together with the destination slave’s address. If a destination address is invalid it prevents the communication, returning an error signal. Otherwise, it directs a request to a slave port and waits for a grant. If a grant is given, it connects a target slave’s data lines to a master interface through multiplexers.

**Communication Isolation:** It is done with the help of configuration registers which provide a master port with allowed slaves. It has high bits for allowed slaves’ bit number while low bits for unallowed ones. Slave addresses are sent in one-hot encoding form by a master; for instance, to access slave 1, “0010” is sent. This eases the communication isolation as sent slave addresses and allowed addresses are compared with AND operator; if the result is 0, it means a master has sent an invalid slave address. In that case, the input port sends an error signal to a master and does not issue any request to a slave.

This method reduces the overhead of the configuration process because configuring a new module would require only updating the registers serving this module and the modules belonging to the same application. Moreover, validating the address on the slave side would incur extra clock cycles (ccs) from the arbiter logic on making a grant decision on an invalid master and then on generating an error signal.

**F. WB Interfaces**

Next, we discuss the modified WB features desired to meet the needs of elastic resource management at reduced area overhead.

1) **WB Master Interface:** Firstly, it initiates the request and provides the destination address to the crossbar upon receiving the request signal from a module, and then, it starts its watchdog timers. If it receives an error signal from the master port due to an invalid destination address or if the waiting time for a grant signal time out, it provides the error code back to a module. If a master is granted access to a slave, it issues data words together with their register addresses. Next in order, if the slave cannot serve the request currently; the master interface stops transmission and waits for the slave to become available. However, if the destination slave does not respond in a defined period, a timeout error happens. Otherwise, when all data is sent successfully it waits for acknowledgment signals for all transmitted data sets.

2) **WB Slave Interface:** Upon receiving a valid request from a master, the slave interface enables its registers to store incoming data provided those registers currently do not contain any unread data, and sends an acknowledgment to a master. When registers become full, and a master still wants to send data, slave interface stalls and desserts the acknowledgment informing a master that it needs to wait before sending new data and disables its registers. Meanwhile, it informs the computation module that its data buffer is full and waits for the module to read the data. The module triggers the slave interface once it has read the data, which causes the slave interface to reset its registers and start registering new data. Whenever the request is de-asserted, the slave interface goes into idle mode indicating either the master has no more data to send or it has sent the allowed number of packages by weighted round robin arbiter or the master gives timeout error waiting long enough for the acknowledgment from a stalled slave.

3) **AXI-to-WB and WB-to-AXI:** Together with one of the crossbar’s ports, these modules transfer data between computation modules and the user application. User data tagged with an application ID is received via any of the 3 host-to-card channels and stored in their FIFO buffers, each with an AXI interface. WB master interface in AXI-to-WB module serves each FIFO periodically through AXI interface. It looks up the ID in the register file, extracts destination modules, and delivers data to the destined PR region. This prevents other applications to access unallocated PR regions even though the crossbar port has access to any PR region. Moreover, a master initiates a request as soon as the AXI side buffer becomes half full. It receives one 32-bit data word from FIFOs each cycle taking it 8 clock cycles to receive complete user data. Master also delivers 1 data word each clock cycle to the slave upon receiving the grant at best after 3 clock cycles. Therefore, overlapping 3 clock cycles of grant latency and 1 clock cycle of sending first data word with the second half of buffer receiving data from AXI end, the latency to deliver user data from FIFO to a computation module is reduced to 15 clock cycles compared to 19 clock cycles for the case where AXI side buffer becomes full for a master to send request.

Similarly, computation results can be read from any of the 3 card-to-host channels. WB slave interface in WB-to-AXI module sends these results to one of card-to-host channels through AXI-streaming interface. The selection of the interface is done based on the shift register which has 3 bits and only 1 bit enabled at a time. Consequently, each channel is targeted in a round-robin fashion.

**G. Computation Module Template**

We provide a standard template for the computation modules to have the same interfaces. However, depending on ap-
plication requirements or the nature of computation modules, the implementation can be different, which means interfaces need to be adapted to be operable with WB. Our standard template comprises input and output registers, error status register, computation units, and control logic.

Upon receiving the buffer full signal from a slave interface, the control logic saves incoming data to input registers and signals the slave interface to register further incoming data. Since the first data word here indicates application ID, it is directly forwarded to the output register. Next, it enables the output registers to store the output of multiple computation units operating in parallel on the input data. Once the output is ready, it requests the master interface with output results and destination address. The status of the request is stored in the error register. If the request is successful, the output registers are reset. If a slave interface has new data, it registers new data; otherwise, it becomes idle. Furthermore, the error status is forwarded to the register file; hence, FPGA elastic resource manager can see if the status of the last request is successful or not.

V. EXPERIMENTAL RESULTS AND DISCUSSION

A. Tools

We use Xilinx KCU1500 [30] acceleration development board to test our prototype. The board contains a Kintex Ultrascale XCKU115 FPGA device and is connected with a PCIe Gen3 to the server running Ubuntu 20.4 and XDMA drivers 2020.1.8 [31]. We rely on Xilinx Vivado tool version 2018.3 [32] to implement system architecture and describe different components in VHDL.

B. System Implementation

The proposed system architecture contains an ICAP module to enable partial reconfiguration feature of the FPGA device; however, it has not been implemented in the current prototype as the overhead of partial reconfiguration on the same FPGA device has been covered in our earlier work [33]. Instead, the features of the proposed 32-bit WB Crossbar interconnect, are tested using statically allocated modules. The data width of WB Crossbar interface is chosen for fair comparison with related work e.g. [15].

The features of the implemented system architecture are summarized here; i) Configurable 4 port WISHBONE Crossbar communication interconnection, which enables to increase or decrease the number of resources allocated to an application, allows dynamic bandwidth allocation for different applications, and provides communication isolation, ii) XDMA IP Core with 6 AXI-ST channels to exchange user data, iii) Three different statically implemented computation modules; the multiplier, the hamming code encoder, and the hamming code decoder together with WISHBONE master and slave interfaces, iv) AXI-WB and WB-AXI modules and v) Register file to serve computation modules and the crossbar with configuration data and to save status data from computation and AXI-WB modules.

C. Results

In this section, the results of the system architecture implemented are assessed.

1) Resource Elasticity: To show how elasticity improves the execution time of the application, we consider a use-case where 16 KB data is sent to be processed by the constant multiplier, the Hamming code (31, 26) encoder, and decoder sequentially. We compare three cases; 1) Multiplication is done on the FPGA while the CPU runs the rest. 2) The encoder becomes available; multiplier and encoder run on the FPGA while the decoder is on the CPU. 3) The decoder becomes available, as well, having all computations running on the FPGA. For each case, the experiment is repeated 10 times and the average execution time is reported in Figure 4. While the average execution time is 16.9 ms for the 1st case, as the user gets more resources it improves to 10.87 ms due to resource elasticity.

![Comparison of Execution Time](image)

Fig. 4: Comparison of Execution Time

2) Dynamic Bandwidth Allocation: To show the effect of dynamically configuring the WB Crossbar bandwidth allocated to computation modules, we consider the three cases mentioned above and repeat experiments at 16 and 128 packets, each packet of size 4 bytes, per accelerator by updating the register file and reporting the total execution time in the respective cases. One can see that by increasing the number of packets allocated to accelerators, the execution time improves from 5.24% when one accelerator (multiply) is configured in the FPGA to 6% when all three accelerators are configured on FPGA to communicate with each other over the WB Crossbar.

3) Communication Overhead: Time-to-grant is the number of clock cycles from the time when a computation module initiates a request to the time when a master interface starts to send the first data. It is 4 ccs in the best case, where the slave does not serve any request concurrently. It takes 2 ccs for the module’s request to reach the master interface and for it to initiate a request. Then, an arbiter spends 2 ccs to grant the request and enable the slave interface. If a computation module has 8 packages to deliver, the request completion latency is therefore 13 ccs. Here, the last clock cycle is used to register the error status of the transaction. Along with this, the worst-case time-to-grant occurs when all 3 computation
modules target the fourth one at the same time. The master being served the last would have to wait for the first 2 masters to be served. In this case, 13 th cc for each previous master module can be ignored because a master interface releases the bus as soon as it completes sending its packages; thus, registering error code only on a master side. Consequently, the last computation module time-to-grant would be 28 ccs (12 ccs for each previous master and 4 ccs for time-to-grant) and request completion latency would be 37 ccs.

4) Area & Power Usage: As reported in Table I, the overall LUT and FF usage of the WB Crossbar together with computation modules and bus interfaces is 0.19% and 0.1% of KCU 1500’s LUT and FF resources. The WB crossbar interconnection itself uses 0.07% LUTs and 0.004% FFs. Depending upon the computation module, on average master and slave interfaces have 196 and 85 LUTs respectively, and correspondingly 117 and 628 FFs. In addition, the LUT usage of the whole system architecture is 5.46% whose 5.04% comes from XDMA IP Core. Correspondingly, the overall FF utilization is 2.75% where XDMA IP contributes 2.32%. WB Crossbar interconnection and a single master interface consume 1 mW power individually. However, a slave interface consumes less than 1mW. FPGA system consumes 5.03W whose 44% comes from GTH transceivers.

### TABLE I: Area Usage of All Components

| Component                  | LUT  | FF   | BRAM |
|----------------------------|------|------|------|
| XDMA IP Core               | 33441| 5.04 | 30843| 2.32 | 62 | 2.87 |
| WB Crossbar                | 475  | 0.07 | 60   | 0.004| 0  | 0    |
| WB Hamming Decoder         | 432  | 0.07 | 646  | 0.05 | 0  | 0    |
| WB Master Interface        | 213  | 0.03 | 27   | <0.01| 0  | 0    |
| WB Slave Interface         | 115  | 0.02 | 220  | 0.02 | 0  | 0    |
| Hamming Decoder            | 104  | 0.02 | 399  | 0.03 | 0  | 0    |
| WB Hamming Encoder         | 233  | 0.04 | 99   | 0.01 | 0  | 0    |
| WB Multiplier              | 138  | 0.06 | 624  | 0.05 | 0  | 0    |
| AXI-WB–FIFO System         | 975  | 0.15 | 1842 | 0.14 | 13.5| 0.62 |
| WB-AXI-FIFO System         | 389  | 0.06 | 2274 | 0.17 | 13.5| 0.62 |
| Register File              | 265  | 0.04 | 560  | 0.04 | 0  | 0    |
| Total                      | 36348| 5.47 | 36948| 2.79 | 89 | 4.12 |

D. Discussion

First and foremost, the resulting 32-bit width configurable crossbar communication interconnection enables dynamic resource allocation, dynamic bandwidth configuration, and communication isolation. Moreover, it takes a very small area (see Table I), which is 475 LUTs, 60 FFs, and no BRAMs while consuming 1 mW power to connect 4 modules. This number varies between 305 and 495 LUTs for a single 32-bit router in [15]. Correspondingly 4 3-ports routers in a 2x2 NoC [15] would occupy 1220 LUTs and 1240 FFs to serve the same number of modules (see Table I). Consequently, our implementation takes 61% less LUTs and 95% fewer FFs than its equivalent NoC architecture. It also consumes 80x less power.

Scaling the area usage of a single master-slave E-WB shared bus architecture [21] by a factor of 4 and comparing it to our 4x4 crossbar interconnection with WB master and slave interfaces, we find that our solution occupies 48.6% more LUT resources and 46.4% fewer FFs (see Table II). A high LUT usage percentage is expected since, in general, crossbars occupy more area than the shared bus.

Next, time-to-grant in our design varies from 4 ccs constant in the best case to 28 ccs in the worst case, which might change depending on the bandwidth allocated to other modules. The current number assumes each module sends 8 packets. Compared to [22], a single command is processed in 8 ccs in the best case, 2 commands need to be exchanged between modules to start a communication, making it 16 ccs for time-to-grant.

Finally, our solution takes 69% less ccs than NoC based design [15] to complete a request. Because, a network package contains a head flit, tail flit, and body flits [16]. Sending 8 sets of data, as in our case, would require sending 10 flits. The first flit takes 2 ccs to pass from one router. Due to pipelining, the remaining flits would take 1 cc each. Thus, traversing the flits only in source and destination routers would take 22 ccs as opposed to 13 ccs in our case.

VI. CONCLUSION

In this work, we have designed a low-area, low-communication overhead, configurable communication interconnection to enable FPGA resource elasticity. The resulting interconnection has intended features; supporting dynamically increasing or decreasing FPGA PR resources to an application while providing communication isolation. Moreover, dynamic bandwidth allocation to the application inside FPGA is one of the other important features of the resulting system. As expected, the resulting crossbar occupies much less area than NoCs and slightly more area than the shared bus. Future work includes integrating the current implementation with PR technology and the Kubernetes engine to exploit the true potential of elasticity of FPGAs in the Cloud.

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