A tunnel FET compact model including non-idealities with verilog implementation

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We present a compact model for Tunnel Field Effect Transistors (TFET), that captures several non-idealities such as the Trap Assisted Tunneling (TAT) originating from interface traps ($D_{it}$), along with Verilog-A implementation. We show that the TAT, together with band edge non-abruptness known as the Urbach tail, sets the lower limit of the sub-threshold swing and the minimum achievable current at a given temperature. Presence of charged trap states also contributes to reduced gate efficiency. We show that we can decouple the contribution of each of these processes and extract the intrinsic sub-threshold swing from a given experimental data. We derive closed form expressions of channel potential, electric field and effective tunnel energy window to accurately capture the essential device physics of TFETs. We test the model against recently published experimental data, and simulate simple TFET circuits using the Verilog-A model. The compact model provides a framework for TFET technology projections with improved device metrics such as better electrostatic design, reduced TAT, material with better transport properties etc.

I. INTRODUCTION

Tunnel Field Effect Transistors are promising candidates for low power logic applications [1]. They have the potential to reduce energy dissipation by relying on Band To Band Tunneling (BTBT) for carrier injection, achieve steep turn-ON and thus reduce the supply voltage. Under ideal conditions, device simulations consistently reported switching at sub-thermal rates [2–8]. Even though the output current from TFET may be low, a sub-thermal sub-threshold swing has the potential to drastically reduce power dissipation and therefore it is attractive for low power applications. Many compact models have been developed in the past to facilitate circuit simulation in Spice [9–13]. However, in most cases the models are tested against results from device simulators instead of experimental devices [9, 11, 14–18]. This is likely due to the fact that most experimental results deviate substantially from ideal device simulations and do not produce sub-thermal switching behavior. Therefore there is a clear disconnect between experimental results and compact models and the realistic potential of TFET based circuits is still unknown.

In this paper, we address this disconnect by developing a physics based compact model that 1) fits experimental data, 2) explains the physics of non-idealities with compact expressions and 3) describes circuit performance for different levels of non-idealities and therefore lays a pathway for studying low power circuits based on TFETs. The main reasons of non-ideal switching behavior in TFETs is the existence of interface traps and non-abrupt density of states (Urbach tail) at the band edges. In the past we developed numerical models explaining the impact of trap assisted tunneling (TAT) [19] and how, combined with non-abrupt Urbach tail, it increases the sub-threshold swing of TFETs. In this paper, we present compact expressions of TAT based on Shockley-Read-Hall formalism. We also present simple expressions of channel potential and electric field and explain how they capture the details of TFET device physics such as the TFET quantum capacitance, super-linear output current and current saturation mechanism.

We implement the model in Verilog-A and present TFET based inverter and oscillator circuit performance based on existing TFET data. The paper is organized as follows: Section II gives a brief overview of the impacts of TAT and the compact expressions of current from TAT. Section III describes the electrostatic model and Section IV describes the BTBT model that includes the Urbach tail. In Section V, we provide model fits to experimental data. The final Section (VI) describes the circuit simulation results using the compact model in Verilog-A.

II. TRAP ASSISTED TUNNELING MODEL

Fig. 1 shows the device structure of a top-gate TFET and the position of the traps. The trap assisted tunneling is only strong where the electric field is high, in this case the source-channel junction. Below the threshold voltage, $V_t$ (when BTBT is triggered), electron excitation by
a phonon from the valence band to a trap state followed by tunneling into the conduction band (Fig. 1b) can give rise to leakage current. The problem is to find how much is the leakage floor compared to the BTBT current and how the overall sub-threshold swing is affected. From the SRH formalism, the electron generation rate from a trap to the conduction band can be written as, 

\[
e_n = \frac{1}{\sigma v_{th}} D_{th}\]

where \(\sigma\) is the carrier capture cross section, \(v_{th}\) is the thermal velocity and \(D_{th}\) is the density of traps. Under high electric field, we have substantial band bending and in addition to thermal emission, electrons can partially be excited by phonons and then tunnel into the conduction band via tunneling. The overall process can be quantified by the original transition rate times an enhancement factor due to tunneling. The new rate becomes, 

\[
e_n = e_{n0} \times \Gamma,
\]

where \(\Gamma\) accounts for the tunneling process. At energy \(E\), the emission probability is enhanced since electrons are emitted into a lower energy level \(E_c\) than they would normally emit to. The emission rate is therefore enhanced to 

\[
e_{n0} \exp\left(\frac{(E_c - E)}{k_BT}\right)
\]

Accounting for the transmission probability \((Tr)\) through the triangular barrier (from \(x\) to \(x')\) and integrating over the energy range \(\Delta E\), \(\Gamma\) is calculated as \([21]\). 

\[
\Gamma_{n,p}(x) = \frac{1}{k_BT} \int_{E_c - \Delta E_{n,p}(x)}^{E_c} \exp\left(\frac{E_c - E}{k_BT}\right) Tr(E) dE
\]

\[
\Gamma_{n,p}(x) = \frac{\Delta E_{n,p}(x)}{k_BT} \int_0^1 \exp\left[\frac{\Delta E_{n,p}(x)}{k_BT} u - K_{n,p} u^{3/2}\right] du
\]

where 

\[
K_{n,p} = \frac{3}{4} \frac{\sqrt{2m^*_{n,p} \Delta E_{n,p}}}{q\hbar^2}, \quad \Delta E_{n,p} \quad \text{defines the range of energy to which the electron (or hole) can tunnel to and from the trap.}
\]

The subscript \((n,p)\) indicates that the equations are equally applicable to both electron and holes.

Once \(\Gamma\) is calculated, the current can be obtained from the net generation rate following the same method as the conventional SRH formalism,

\[
G^n(x) = \int \frac{n_i^2 - np}{\tau p + \tau_n} \frac{D_{th}}{\pi F(e^{x/F} + K)}\]

\[
I = qW \int G^n(x) dx
\]

where \(n_i\) is the intrinsic carrier concentration, \(n\) and \(p\) are the electron and hole densities. With \(\Gamma = 0\), Eq. 3 reduces to the conventional SRH formalism.

**A. Compact expression of TAT**

Eq. 2 involves integration and therefore is not suitable for circuit simulation. Assuming that lifetimes and electric field enhancement factors are the same for electron and hole, and that the channel is depleted of free carriers \((n = p = 0)\) near the source-channel junction where most of the generation takes place, and constant generation rate over a length \(d_{gen}\), we can simplify the above formalism into a compact form as below,

\[
I_{TAT} = qW \frac{n_i}{2\pi} \Gamma d_{gen} \left[1 - e^{-2n_i/k_BT}\right]
\]

The integration over energy is eliminated because only the midgap traps contribute significantly to the TAT. Typical channel electric field in TFETs vary around 1 MV/cm. In this high electric field regime \((K < 2/3\Delta E/k_BT)\), the \(\Gamma\) expression can be simplified as following,

\[
\Gamma = \frac{\Delta E}{k_BT} \sqrt{2\pi F(e^{x/F} + K)}
\]

where \(F\) is a fitting parameter. Thus \(\Gamma\) depends on the temperature \(T\), electric field \(E\), and the material parameters effective mass \((m^*)\), bandgap \((E_g)\). Fig. 2 shows the comparison of the calculation of \(\Gamma\) from Eqs. 2 and 6 at room temperature, assuming \(\Delta E = 0.4\) eV, \(m^* = 0.04m_0\). The compact expression (Eq. 6) shows good agreement with the exact numerical calculation (Eq. 2) above \(E = 2 \times 10^7\) V/m with \(F = 2\). However, \(\Gamma\) in Eq. 6 represents an average enhancement factor over the entire generation volume (where the TAT takes place) and thus \(\Delta E\) loses its direct physical meaning.

**III. ELECTROSTATICS MODEL**

The TFET surface potential is strongly influenced by the drain voltage since the channel is primarily populated
with drain injected carriers. At low drain bias, the carrier injection is high and therefore the channel potential is pinned due to high quantum capacitance. At the high drain bias limit, the injection is low and the potential is controlled primarily by the gate voltage (Fig. 3). We capture the surface potential including these effects with the following empirical compact expression,

$$\psi = \frac{k_B T}{\xi} \left\{ \log \left[ \log \left( \frac{V_{GS,\text{internal}} - \phi}{k_B T / \xi} \right) \right] + ... \right\}$$

(7)

where $\phi = \phi_0 + \xi V_{DS}$ and $\phi_0$ sets the zero bias ($V_{DS} = 0$) surface potential. $\xi$ sets the rate of change of surface potential with $V_{DS}$. We show that this is a powerful expression that can capture the details of TFET transport, such as the transconductance, output resistance, super-linear drain current at low $V_{DS}$ etc. The fitting parameters for the potential are the zero-bias maximum potential $\phi_0$, the smoothness parameter $\xi$ and the bias control parameter $\xi$. For small gate voltage ($V_{GS} << \phi$), Eq. 7 gives $\psi \approx k_B T / \xi \{ \log[\exp(V_{GS,\text{internal}} - \phi) / (k_B T / \xi)] + \phi / (k_B T / \xi) \} \approx V_{GS}$. For $V_{GS} >> \phi$, we find $\psi \approx k_B T / \xi \{ \log[(V_{GS,\text{internal}} - \phi) / (k_B T / \xi)] + \phi / (k_B T / \xi) \} \approx \phi$. Therefore $\phi_0$ essentially sets the maximum potential that can be achieved in the device at low drain bias (high carrier injection). If the device is initially in p-i-n regime, $\phi_0$ is roughly equal to half of the bandgap. Such drain bias dependence of the channel potential does not originate from any short channel effects and it is intrinsic to TFET. The parameter $\xi$ reflects the control of drain bias on the channel potential. The surface potential saturates roughly at $\phi_0$ plus the drain bias ($\xi = 1$), however, materials with low quantum capacitance will have lower values of $\xi$. Fig. 4 shows how the channel potential varies with drain bias for different values of the fitting parameters used in $\psi$. For instance, as the smoothness parameter $\xi$ is increased, $\psi$ changes more slowly and smoothly. For smaller and smaller values of $\xi$, $\psi$ changes more slowly with the drain bias. Finally, as $\xi$ is increased, the initial value (zero bias) of $\psi$ increases. We will later show how these parameters affect the current-voltage characteristics.

The electric field in the channel can be expressed as,

$$|E| = \mathcal{E}_0 + \frac{\psi}{\lambda}$$

(8)

where $\mathcal{E}_0$ is the initial electric field (at zero gate voltage, set to $E_g / 2\lambda$ for an intrinsic channel) and $\lambda$ is the characteristic scaling length, which is a function of semiconductor and oxide thicknesses. The internal gate voltage is found ($V_{GS,\text{internal}} = \eta t V_{GS}$) after accounting for the gate efficiency limited by charged traps,

$$\eta = \frac{C_{ox}}{C_{ox} + C_{it}}$$

(9)

$$C_{it} = \varepsilon^2 \int D_{it} \frac{\partial}{\partial E} dE$$

(10)
valid for positively charged donor trap states, where $f_s$ is the Fermi-Dirac distribution function $[22]$. 

IV. BAND TO BAND TUNNELING MODEL

From Kane’s model for tunneling $[23]$

$$I_{BTBT} = A W V_R \left( \frac{E}{e_0} \right)^P e^{-\frac{E}{k_B T}}$$ (11)

where $A, B, P$ are material fitting parameters. $V_R$ is the effective bias controlled by both gate and drain biases by $V_R = F_{\text{sat}} E_{\text{TW}}/q$. $F_{\text{sat}}$ (shown below) captures the superlinearity in $I_{DS} - V_{DS}$ and controls $V_R$ when $V_{DS}$ is lower than the tunneling energy window, $E_{TW}$. From the Landauer formalism and using $F_{\text{sat}} = I_{DS}(V_{DS})/I_{DS_{\text{max}}}$,

$$F_{\text{sat}} = \frac{k_B T}{\mu_s - E_{cch}} \log \left[ \frac{\exp \left( \frac{E_{vs}}{k_B T} \right) + \exp \left( \frac{\mu_s - q V_{DS}}{k_B T} \right)}{\exp \left( \frac{E_{cch}}{k_B T} \right) + \exp \left( \frac{\mu_s - q V_{DS}}{k_B T} \right)} \times \frac{\exp \left( \frac{E_{sat}}{k_B T} \right) + \exp \left( \frac{\mu_s - q V_{DS}}{k_B T} \right)}{\exp \left( \frac{E_{cch}}{k_B T} \right) + \exp \left( \frac{\mu_s - q V_{DS}}{k_B T} \right)} \right]$$ (12)

where $\mu_s$ is the source Fermi energy, and $E_{vs}$ and $E_{cch}$ are the source valence and channel conduction band edges respectively. The above expression works for both degenerately and non-degenerately doped sources and for all gate voltages. For a non-degenerate source ($E_{vs} - \mu_s < 0$), the drain current does not initiate until the Fermi window ($\mu_s - q V_t$) is large enough to penetrate the valence band of the source. As a result the output current is non-linear for small drain bias (black curve in Fig. 3). For degenerate source, the Fermi window is already inside the tunnel window (at zero drain bias) and therefore the output current increases linearly. Transport for all such conditions is captured with the above $F_{\text{sat}}$ function.

However, the denominator, which is a normalizing factor, $\mu_s - E_{cch}$ in the expression of $F_{\text{sat}}$ is valid for above threshold only ($V_{GS} > V_t$) and therefore for $V_{GS} < V_t$, the above expression of $F_{\text{sat}}$ predicts an incorrectly low value. Below $V_t$, the tunnel window is extremely small and therefore $F_{\text{sat}}$ should be 1 for all practical purposes. We solve this problem by introducing a function $FF$ which is 1 below threshold and 0 above threshold and take the weighted average as below,

$$F_{\text{sat,combined}} = FF + (1 - FF) \times F_{\text{sat}}$$ (13)

$$FF = \frac{1 - e^{-V_{DS}/k_B T}}{1 + e^{-V_t/V_t}}$$ (14)

where $V_t$ is of the order of a few $k_B T$, fitted to get the correct transition. The combined function along with the original $F_{\text{sat}}$ is shown in Fig. 6

The tunnel energy window can be found from

$$E_{TW} = U_0 \log \left[ 1 + e^{\frac{V_t}{U_0}} \right]$$ (15)

$U_0$ is a parameter that defines the sharpness of the band edge (Urbach tail times the geometric gate efficiency). In principle, $U_0$ should be temperature dependent, however previous studies on Urbach tail reveals weak temperature dependence $[24, 25]$. We use $U_0 = K_B T_0/\gamma_t$, where $T_0 = 300$ K, and $\gamma_t = \gamma(T_0/T)^\beta$, where $\gamma$ and $\beta$ are fitting parameters. Before the bands
FIG. 7. As the TFET goes from OFF to ON state, the energy tunnel window $E_{TW}$ changes from an exponential function (Urbach-tail-limited) to a linear function at voltages above threshold, $V_t$. Overlapped (at $V_{GS} = V_i$), it can be assumed that the tunnel window increases exponentially, instead of an abrupt turn-ON (at $V_{GS} = V_i$) as a result of the exponentially decaying states above the valence band in the source (for an n-channel TFET). Above $V_t$, the window increases linearly, which is captured by Eq. 15, as expected (Fig. 7). For materials with high density of states (such as silicon), $\phi_0$ will be lower, resulting in stronger super-linear behavior. The super-linearity can diminish if $\phi_0$ is already high at small drain bias and therefore $\psi$ changes little as bias is increased. The super-linear behavior can also diminish if the value of $\xi$ is sufficiently low ($\xi = 0.1$ in Fig. 8), regardless of $\phi_0$. However in this case $\phi_0$ strongly influences the energy tunnel window (Eqs. 7-15); above $V_t$, $E_{TW, highV_{DS}} = \psi_{highV_{DS}} - V_t$, and therefore change of $\phi_0$ changes the ON current.

Since $\phi_0$ changes the energy tunnel window and the current, the transconductance is also dependent upon this parameter. Fig. 9 shows the transfer characteristics for various $\phi_0$ values and two different drain biases. Higher values of $\phi_0$ lead to higher transconductance and the low drain bias transconductance is always lower than the higher bias. This is because of the higher quantum capacitance at low drain bias and the slow increase of $\psi$ with $V_{GS}$ (Fig. 3). Since the carrier density is a function of temperature, the parameter $\phi_0$ is also temperature dependent.

V. MODEL FIT OF EXPERIMENTAL DATA

Fig. 10 shows the experimental transfer characteristics along with the model fits for an InGaAs/GaAsSb quantum well vertical TFET [26]. The fitting procedure is summarized as following. The bandgap, effective mass and carrier capture cross-section due to the traps are adopted from the literature for the particular channel material (Table I). The TAT parameters ($d_{gen}$, $\Delta E$, $D_{it}$)...
FIG. 9. (a) Transconductance varies strongly with $\phi_0$, since it affects the tunnel window and the ON current. Smaller values of $\phi_0$ (for small drain bias) pins the surface potential (for $V_{GS} >> \phi$, $\psi \approx \phi = \phi_0 + \xi V_{DS} \approx \phi_0$, as discussed in the text) and the current saturates at low values.

FIG. 10. Model fit (line) of the experimental data (symbols) in Ref. [26] - a InGaAs/GaAsSb heterostructure TFET. The model yields good fit at different temperatures with parameters shown in Tables I and II.

are varied to fit the leakage current of the device at different temperatures. The extracted interface trap density is found to be $D_{it} = 3 \times 10^{15}$/cm$^2$-eV, which signifies the interface trap density between the GaAsSb source and InGaAs channel. The interface between the two epitaxially grown structures defect density is lower than the oxide - III-V interface. The intrinsic band steepness parameters ($\gamma$, $\beta$) are then varied to match the sub-threshold swing at different temperatures. The electrostatic parameters ($t_{semi}$, $\xi$, $\zeta$, $\phi_0$) are tuned to match the current magnitudes in the ON state and the transconductance. The model parameters to fit the data shown in Fig. 10 are shown in Tables I and II.

With the extracted BTBT parameters ($\gamma$, $\beta$), we extract the intrinsic sub-threshold swing as a function of temperature as shown in Fig. 10. As discussed earlier, the TAT contribution obscures the intrinsic, steep BTBT as evident from Fig. 10. The intrinsic BTBT is found to be around 50 mV/dec (in the sub-threshold regime, below $10^{-4}$ $\mu$A/$\mu$m), which can be considered as the product of the Urbach tail and the geometric gate efficiency. Reported values of Urbach tail are around 30 mV/dec, therefore our estimate of the geometric gate efficiency is $\sim$0.6. The low gate efficiency can be justified by the particular device structure, where the source-channel interface is deliberately placed far from the gate oxide-channel interface (with the InP cap) to minimize the impact of oxide interface traps.

In order to make sure the model can simultaneously fit both transfer and output characteristics, we have fitted data at $T = 94$ K as shown in Fig. 11. The model deviates from the data for this particular device for low $V_G$ values due to possible other leakage paths that were not included in the model.

FIG. 11. Simultaneous fitting of $I_{DS}-V_{GS}$ and $I_{DS}-V_{DS}$, symbols are experimental data from Ref. [26].

| Symbol | Value |
|--------|-------|
| $E_g$  | 0.7 eV|
| $m^*$  | 0.041m|
| $t_{ox}$ (EOT) | 1 nm |
| $t_{semi}$ | 31 nm |
| $\xi$  | 0.05 |
| $deq$  | 15 meV (degenerate) |
| $D_{it}$ | $3 \times 10^{15}$/cm$^2$-eV |
| $\beta$ | 0.03 |

| $\Delta E$ | 0.194 eV |

TABLE I. Temperature independent parameters used in Fig. 10

| T (K) | $v_{shift}$ ($V$) | $\phi_0$ ($V$) | $\zeta$ | $\gamma$ | $\sigma$ ($\times 10^{-17}$/cm$^2$) |
|-------|----------------|----------------|-------|--------|----------------------------------|
| 300   | 0.07           | 0.04           | 0.25  | 0.7    | 5                                |
| 240   | 0.02           | 0.04           | 0.15  | 0.7    | 2.5                              |
| 191   | -0.025         | 0.04           | 0.08  | 0.9    | 2                                |
| 140   | -0.11          | 0.09           | 0.08  | 0.9    | 2                                |

TABLE II. Temperature dependent parameters used in Fig. 10
VI. VERILOG-A MODEL AND CIRCUIT SIMULATION

In this section, we demonstrate a Verilog-A implementation of our compact model in Advanced Design System (ADS) circuit simulator.

In Fig. 12, we show TFET-based inverters using the N-TFET devices and symmetric P-TFETs. We implement the model described in this work in Verilog-A and calibrate against measured DC-currents shown in Fig 11 along with capacitances. We perform the inverter simulations in ADS. The resulting voltage-transfer-characteristics of the inverter are shown in the figure along with terminal current as a function of input voltage. The simulations show the convergence robustness of the Verilog-A model.

The inverter is used as a building block to simulate a 21-stage ring oscillator (RO) whose output voltage waveforms are shown in Fig. 13. TFET shown in Fig. 11, the baseline TFET at $T = 300$ K, shows oscillation frequency of about 500 MHz at $V_{DS} = 1$ V. The low frequency (or transit-time) in the baseline TFET is because of low ON-current and high OFF-current (limited by the TAT). Better electrostatic design along with a reduction in $D_{it}$ yields improved SS. Use of channel material that can provide lower bandgap and carrier-effective mass can boost ON-current. The model that incorporates these improvements at the device-level can yield a reduction in transit-time and an increase of 30% in oscillation frequency (solid line in Fig. 13). The Verilog-A model developed in this work can thus provide a tool-guide for innovative device design for desired system performance.

VII. CONCLUSION

We present a compact model with the inclusion of trap assisted tunneling allowing studies of surface trap effects on TFET circuit performance. The model captures the structural and material parameters that influence TAT. We provide compact expressions of channel potential and electric field that accurately capture the TFET quantum capacitance. The model can also be used to extract intrinsic sub-threshold swing from a given experimental data. We implement the model in Verilog-A and present simulation of simple circuits based on TFETs. The model for the first time evaluates the impact of non-idealities on TFET circuit performance.

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