Supporting information for-
On the use of scalable NanoISFET-arrays of silicon with highly reproducible sensor performance for biosensor applications

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1. Measurements of film-thicknesses:

The thickness of different layers on SOI wafers was measured using SEN850 ellipsometry from SENTECH GmbH, Berlin. Figure S11A shows the snapshot ellipsometry tests carried out for the thickness measurement of top silicon layer and buried oxide layer after wafer cutting process (A). The initial thickness of silicon and underlying buried oxide is measured at 87nm and 145nm respectively.

The oxidation process is carried out at 1000°C for 1 hr to convert the top Si layer to SiO₂. The thickness of Si consumed by the oxidation process is given by-

\[ t_{Si} = 0.44t_{SiO_2} \]

Where, \( t_{Si} \) is the thickness of Si consumed in order to get \( t_{SiO_2} \) i.e thickness of SiO₂.

As seen from figure S11B, the thickness of the SiO₂ layer after oxidation is measured at 45 nm. Therefore, the thickness of Si consumed in the oxidation process-

\[ t_{Si} = 0.44 \times 45 = 19.8\text{nm} \]

Initial thickness of Si was measured at 87 nm; therefore leftover Si thickness is in the order of 67nm which lay in accordance with the results obtained from ellipsometry measurements (Fig. S11B).
SI1: Thickness measurement of different layers of SOI wafer represented as amplitude ratio PSI (Ψ) and phase change (Δ). A) thickness of top silicon layer and buried oxide layer after wafer cutting process; and B) thickness of top oxide, Si, and buried oxide layer after thermal oxidation step.
2. Calculation of resistance and capacitance values for contact lines:

Equal resistance and capacitances are exerted on the drain contact lines in order to minimize the parasitic effects and achieve uniform transport characteristics. While using a common source contact, drain contact lines are intricately designed to render equal surface area. For doping concentration of the order of $10^{20}$/cm$^3$ Boron ions, the resistivity for $p$-type Si is calculated at $10^{-5} \Omega \cdot m$.\(^{[1]}\)

The sheet resistance ($R_s$) = resistivity / thickness.

Therefore, for 70nm thick Si, $R_s = 10^{-5} \Omega \cdot m / 70 \times 10^{-9} m = 143 \Omega$.

Since sheet resistance is measured in Ohms per square; we needed to calculate the number of squares for common Source and individual Drain contacts. Total number of unit squares for Source contact on the sensor chip = 11. Sheet resistance of Source contact therefore $R_s = 11 \times 143 = 1573 \Omega = \text{around } 1.6 \text{k} \Omega$.

Total number of unit squares for each Drain contact line on the sensor chip = 50. Therefore the sheet resistance of Drain contacts = $50 \times 143 = 7.15 \text{k} \Omega$.

For the measurement of capacitances, a parallel plate capacitor model is used where Capacitance is given by $C = E_0 \epsilon_r \frac{A}{d}$

where $E_0$ is the vacuum permittivity ($8.8541 \times 10^{-12} \text{ Fm}^{-1}$), $\epsilon_r$ is dielectric constant of SiO$_2$ (3.9) and $A$ is unit square area ($3 \times 10^5 \mu m^2$ and $5 \times 10^5 \mu m^2$ for Drain and Source respectively) of the dielectric material and $d$ is the thickness (8 nm) of dielectric material i.e. SiO$_2$ used as passivation layer. From the above mentioned formula, the capacitance for drain and source contact lines can be calculated at $13 \times 10^{-10} \text{ F}$ and $22 \times 10^{-9} \text{ F}$ respectively.

2. Field-effect mobility calculations:

The field-effect mobility ($\mu_{fe}$) of the nanoISFET-arrays are calculated using the formula-

$$\mu_{fe} = \frac{dI}{dV} \cdot \frac{A}{C_{edl} \times V_d}$$

Where $dI/dV$ is transconductance, $C_{edl}$ is the electrical double layer capacitance, $V_d$ is the drain-source bias and $A$ is the unit square area of the trapezoidal nanowire surface. For the trapezoidal shape of nanowire arrays as shown in the schematic below a parallel plate capacitor model was used for the calculation of $C_{edl}$ using $C_{edl} = \epsilon_0 \epsilon_r A/d$ where $\epsilon_0$ is the permittivity of the vacuum, $\epsilon_r$ is the relative permittivity of the buffer solution, $A$ is the surface area of trapezoidal nanowire and $d$ (1 nm) is the thickness of the electrical double layer.
3. Ion implantation of contact lines:

SRIM-software (Stopping and Range of Ions in Matter) was used for the calculation of implantation energy defining the optimal projection ranges in the sample and the dose of ions.[2] With SRIM program, stopping and range of ions into matter is calculated using quantum mechanical treatment of ion-atom collisions. For 40nm projection range in Si in order to implant the top Si layer, 10keV energy was calculated for the implantation with boron ions as shown in graph A in the figure SI3. The dose of ion implantation for a degenerate semiconductor (conductivity similar to metal) is calculated in the order of order of $10^{20}$ atoms/cm$^3$. From 2008 version of SRIM -TRIM calculation program as shown in a plot in graph B in figure SI2 was obtained and a required implantation dose of approximately $10^{15}$ atoms/cm$^2$ was calculated.
SI3: Plots showing boron implantation energy, A and dose, B obtained from SRIMS and TRIM software respectively.
5. Inherent issues with procurements and how it may affect properties of the sensor platform (nanoISFET-arrays):

The top-down nanofabrication approach involving nanoimprint lithography tools and photolithography processes may eventually lead to some inherent issues that shall be avoided in the future work and further refine the process for the realization of nanoISFET-arrays based sensor platform. The nanoimprint mould and photolithography masks when procured from different sources may result in alignment problems which may necessary not have adverse effect on the sensor properties yet may give rise to minimal device-to-device variations. In our work, we observed such variation in sensor properties arising from the misalignment occurring between the nanoimprint mould and lithography masks which resulted in the shifting of passivation mask for nanowire-arrays towards drain contact lines. This shift in the alignment may also arise from tiny variations in the structural features of the components of the nanoimprint tool such as loader plate and boarders of nanoimprint stamp during the imprint process. The shifting of this passivation area on the nanowire arrays was seen towards the edges of the wafers. Two optical images in figure SI4A and B compare the centre-aligned and left-aligned passivation masks on the nanowire arrays before carrying out the ion-implantation process. In figure SI4C, threshold voltages of nanoISFET-array’s sensor response measured in buffer solution at pH 7, we observe a unique trend among nanoISFET-arrays where threshold voltages shift into opposite directions after carrying out the silanization process. The threshold voltage values before silanization are shown in black dots and after silanization in red dots. NanoISFET-arrays with lower threshold voltages tend to show an increased threshold (moving towards negative gate voltages) while those with relatively higher threshold voltages before silanization tend to show a decrease in the threshold voltages (moving towards positive gate voltages) afterwards. The fact that position of the passivation mask changes effective channel lengths of the nanoISFET-arrays explains the variation in threshold voltage values between nanoISFET-arrays where passivation mask was ‘centre-aligned’ and ‘aligned towards the drain contacts’. [3,4]
SI4: Variation in sensor properties related to alignment of passivation mask onto nanoISFET-arrays before carrying out ion-implantation for the highly conductive contact lines. Optical images show the passivation masks used for protecting nanowire-arrays before carrying out the implantation process where the mask is (A) centre-aligned and (B) shifted slightly towards the drain contact lines. (C) The threshold voltages for all the nanoISFET-arrays measured are plotted where slight variation in Vth is associated with the positioning of passivation mask on the nanoISFET-arrays (D) pH sensor characteristics for the nanoISFET-arrays where passivation mask was aligned towards the drain contact lines, (E) Average Vth values plotted for all nanoISFET-arrays before and after silanization process with error bars. (F) Average Vth values plotted only for centre-aligned nanoISFET-arrays with error bars.

However, the pH sensing characteristics of nanoISFET-arrays with passivation mask aligned towards drain contacts show a similar behaviour to the ‘centre-aligned’ nanoISFETS which is shown in the figure SI4D. The change in threshold values of the nanoISFET-arrays is plotted against buffer
solutions changing pH values from 5 to 9. The nanoISFET-arrays with passivation mask aligned towards drain contacts show slightly more variation in the pH sensor response with pH sensitivity of 48±19 mV/pH which is much higher sensitivity as compared to the centre-aligned nanoISFET-arrays however with larger variations. Here it is interesting to note that the devices were subjected to the gas-phase silanization process altogether leaving little room for the variations arising from the process itself. A comparison made between the threshold values of the devices before and after silanization process is shown in two different histograms in figures SI4E and SI4F for all the nanoISFET-arrays and the arrays with centre-aligned passivation mask, respectively. It may be inferred from these histograms that the creation of an ion-selective molecular layer over the nanoISFET-arrays exerts a new surface-charge equilibrium which compensates to the variation in the threshold voltages to an extent.

Figure SI5 compares the real-time pH measurement characteristics of the nanoISFET-arrays that were carried out on the hand-held readout tool. We first evaluated the transconductance of the nanoISFET-arrays and operated them at a set gate-voltage at the Ag-AgCl reference electrode associated with the maximum transconductance values while applying a fixed bias. In this way, drain-source currents are measured while changing the buffer solutions with pH values 4 to 10. From the drain-source current values, we calculated the equivalent gate voltages and the corresponding plots for the real-time pH sensing are shown in figure SI5A and B. The transcondutance values for the devices as show in figure A and B were 0.7 microS and 1.7 microS corresponding to gate voltages -1.5 V and -1.6 V respectively while applying drain-source bias at -1.0 V. After operating for several cycles of changing the buffer solutions show very similar behaviour with average change in equivalent gate voltage of 10±6 mV/pH and 9±3 mV/pH were measured for the nanoISFET-arrays with passivation mask ‘centre-aligned’ and ‘alignment towards drain contacts’ respectively. In figure E and F, while plotting the real-time pH sensor characteristics for nanoISFET-arrays equivalent gate voltage for the devices was taken at different time intervals after changing the buffer solutions showing a stable sensor response.
S15: Real-time pH sensing characteristics of nanoISFET-arrays with centre-aligned and left-aligned passivation mask. (A) Real-time pH sensing using buffer solutions ranging from pH4 to pH10 where output characteristic of the nanoISFET-arrays (drain current here at fixed bias and gate) is recorded. (B) Real-time pH sensing characteristics for the nanoISFET-arrays where passivation-mask was aligned towards drain contacts; (C and D) pH sensitivity of the realtime measurements is plotted as change in the equivalent gate voltages against buffer pH values over multiple cycles for two different kinds of chips respectively; (E and F) Equivalent gate voltage change over multiple cycles and data-points taken at different times after changing the buffer solution plotted against pH.
Effect of the position of reference electrode in the microfluidic well on the threshold voltages of the nanoISFET-arrays:

SI6: Change in threshold voltage depending on the relative position of the reference electrode in the microfluidic well. (A) Schematic showing the dimensions of the microfluidic wells used for the measurements. The red dots represent the position of the tip of reference electrode in the microfluidic well namely Centre-down, Centre-up, Left and Right. (B) The threshold voltages were measured for three different nanoISFET-arrays while switching the position of the reference electrode. (C) The threshold average of the three nanoISFET-arrays show very small variation calculated at 0.45 percent ($V_{th} = 0.6653 \pm 0.003V$ at $V_{ds} = 1V$) at different reference electrode positions.

Further details on the Nanoimprint lithography process:

The NIL mould was patterned using an electron beam lithography process on a 5-inch SiO$_2$ (200nm)/Si wafer. Reactive-ion etching process was used for the etching of SiO$_2$ layer forming vertical side-wall profiles on the mould as shown in the SEM cross section of a mould (figure SI7A). For a target configuration of nanowire-arrays, one has to take account of ‘imprint proximity effects’ in the nanoimprint process. Since a polymer resist (a thermal resist in our case) works as a matrix to replicate the features onto a substrates from the mould, the ‘proximity effects’ for a process are determined by the size-distribution of the features on the mould, their density, aspect-ratio in all three dimensions and finally the properties of the resist itself used in the process. A narrow size distribution of the features on the mould would result in an even and homogeneous filling of the spaces in-
between the features and therefore high reproducibility. For this reason, we employed one single type of nanowire-arrays as detailed in the main text of this manuscript requiring easier control of imprint parameters for better yields.

SI7: Proximity effects in a nanoimprint process require careful optimization of imprint parameters. (A) A SEM image of cross-section of the nanoimprint mould showing the ‘trenches’ of nano-size features after the RIE process (B) An example where a wider size-distribution on the imprint mould may in some cases result in the incomplete filling of the spaces in-between the micron sized features and therefore resulting in surface irregularities.

For the production of nanoISFET-arrays, as described in the main text, nano-size (nanowire arrays) and micron-sized (contact line regions) features, the depth of the trenches was kept at 210 nm, as shown in figure SI7A, resulting in around 160 nm height for the features after all the steps carried out in the imprint process as measured from the AFM and SEM measurements. An example of inhomogeneous filling due to wider size-distribution of mould features and therefore incomplete etching of Si in some parts is given in the figure SI7B where one can see residual structures on the chip as a result of proximity effects. Such issues were overcome during the imprint optimization process by changing the resist layer thicknesses and imprint parameters. Similarly, features with low height-to-width ratio are advantageous for efficient filling of the in-between spaces in the vertical direction. A resist with low viscosity and low glass-transition temperature is advantageous for nanoimprint process. The height to width ratio of the nano-patterns in the SiO$_2$/Si mould was kept low (approximately 4:3) in order to prevent pattern fracture after demoulding process due to high shear stress at the vertical interface between the polymer and the mould.$^{[7,8]}$ Furthermore in order to prevent any sticking problem between the resist and the stamp, prior to the NIL process, the stamp is coated with an anti-sticking silane layers e.g. FOCTS.$^{[9]}$
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