Safety Verification of Parameterized Systems under Release-Acquire

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Abstract

We study the safety verification problem for parameterized systems under the release-acquire (RA) semantics. It has been shown that the problem is intractable for systems with unlimited access to atomic compare-and-swap (CAS) instructions. We show that, from a verification perspective where approximate results help, this is overly pessimistic. We study parameterized systems consisting of an unbounded number of environment threads executing identical but CAS-free programs and a fixed number of distinguished threads that are unrestricted.

Our first contribution is a new semantics that considerably simplifies RA but is still equivalent for the above systems as far as safety verification is concerned. We apply this (general) result to two subclasses of our model. We show that safety verification is only $\text{PSPACE}$-complete for the bounded model checking problem where the distinguished threads are loop-free. Interestingly, we can still afford the unbounded environment. We show that the complexity jumps to $\text{NEXPTIME}$-complete for thread-modular verification where an unrestricted distinguished ‘ego’ thread interacts with an environment of CAS-free threads plus loop-free distinguished threads (as in the earlier setting). Besides the usefulness for verification, the results are strong in that they delineate the tractability border for an established semantics.

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1 Introduction

Release-acquire (RA) is a popular fragment of C++11 [14] (in which reads are annotated by acquire and writes by release) that strikes a good balance between programmability and performance and has received considerable attention (see e.g., [3,4,11,17,49,51,53,60,63,64]). The model is not limited to concurrent programs, though. RA has tight links [52] with causal consistency (CC) [7], a prominent consistency guarantee in distributed databases [55]. Common to RA implementations and distributed databases is that they tend to offer functionality to multi-threaded client programs, be it means of synchronization or access to shared data.

We are interested in verifying such implementations on top of RA. For verification, we can abstract the client program to invocations of the offered functionality [20]. The result is a so-called instance of the implementation in which concurrent threads execute the code of interest. There is a subtlety. As the RA implementation should be correct for every client,

1 This work was done when Adwait Godbole was a final year undergraduate student at IIT Bombay
we cannot fix the instance to be verified. We have to prove correctness irrespective of the number of threads executing the code. This is the classical formulation of a parameterized system as it has been studied over the last 35 years [20].

We are interested in the decidability and complexity of safety verification for parameterized programs under RA. The goal is to identify expressive classes of programs for which the problem is tractable. There are good arguments in favor of this agenda. From a pragmatic point of view, even if the implementation at hand does not fall into one of the classes identified, we may hope for a reasonably precise encoding. From a conceptual point of view, tractability of verification is linked to programmability, and understanding the complexity may lead to suggestions for better consistency notions [50] or programming guidelines, e.g. in the form of type systems [56]. Safety verification is a good fit for linearizability [43], the de-facto standard correctness conditions for concurrency libraries, and has to be settled before going to more complicated notions.

To explain the challenges of parameterized verification under RA, it will be helpful to have an understanding of how to program under RA. The slogan of RA is never read “overwritten” values [52]. Assume we have shared variables g and d, initially 0, and a thread first stores 1 to d and then 1 to g. Assume a second thread reads the 1 from g. Under RA, that thread can no longer claim \( d = 0 \). Formulated axiomatically [7], the reads-from, modification order, program order, and from-read should be acyclic [52]. While less concise, there are operational formulations of RA that make explicit, information about the computation which will be useful for our development [47,48,59]. The mechanism is as follows. Program and modification order are encoded as natural numbers, called timestamps. Each thread stores locally a view object, a map from shared variables to timestamps. This map reflects the thread’s progress in terms of seeing (or as above hearing from) stores to a shared variable. The communication is organized in a way that achieves the desired acyclicity. Store instructions generate messages that decorate the variable-value pair by a view. This view is the one held by the thread except that the timestamp of the variable being written is raised to a strictly higher value. The shared memory is implemented as a pool to which the generated messages are added and in which they remain forever. When loading a message from the pool, the timestamp of the variable given by the message must be at least the timestamp in the thread. The views are then joined so that the receiver cannot load values older than what the sender has seen.

The timestamps render the RA semantics infinite-state, which makes algorithmic verification difficult. Indeed, the problem of solving safety verification under RA in a complete way has been studied very recently in the non-parameterized setting and proven to be undecidable even for programs with finite control flow and finite data domains [1]. With this insight, [1] proposes to give up completeness and show how to encode an under-approximation of the safety verification problem into sequential consistency [54]. Lahav and Boker [50] drew a different conclusion. They proposed strong release-acquire (SRA) as a new consistency guarantee under which safety verification is decidable for general non-parameterized programs. Unfortunately, the lower bound is again non-primitive recursive. Also the related problem of checking CC itself for a given implementation has been studied. It is undecidable in general, but \( \text{EXPSPACE} \)-complete under the assumption of data independence [22].

To sum up, despite recent efforts [1,22,50] we are missing an expressive class of programs for which the safety verification problem under RA is tractable. The parameterized verification problem has not been studied.

**Problem Statement.** The parameterized systems of interest have the form \( \text{env} \parallel \text{dis}_1 \parallel \cdots \parallel \text{dis}_n \). We have a fixed number of distinguished threads collectively referred to as dis and
executing programs $c_{\text{dis}}^1, \ldots, c_{\text{dis}}^n$, respectively. Moreover, we have an environment consisting of arbitrarily many threads executing the same program $c_{\text{env}}$. We obtain an instance of the system by also fixing the number of number of environment threads. The safety verification problem is as follows:

Safety Verification for Parameterized Systems:
Given a parameterized system $\text{env} || \text{dis}_1 || \cdots || \text{dis}_n$, is there an instance of the system and a computation in that instance that reaches an assertion violation?

The complexity of the problem depends on the system class under consideration. We denote system classes by signatures of the form $\text{env} \left( \text{type}_{\text{env}} \right) || \text{dis}_1 \left( \text{type}_1 \right) || \cdots || \text{dis}_n \left( \text{type}_n \right)$, where the types constrain the programs executed by the threads. The parameters are the structure of the control flow, which may be loop-free, denoted by acyc, and the instruction set, which may forbid the atomic compare-and-swap (CAS) command, denoted by noca. We drop the type if no restriction applies. If a thread is not present, we do not mention it in the signature. With this, $\text{dis}_1 \left( \text{acyc} \right) || \text{dis}_2 \left( \text{noca} \right) || \text{dis}_3$ is a non-parameterized system (without $\text{env}$ threads) having three $\text{dis}$ threads executing: a loop-free $c_{\text{dis}}^1$, $c_{\text{dis}}^2$ which does not have CAS instructions, and $c_{\text{dis}}^3$ which is free of restrictions, respectively.

Justifying the Parameters. In [1], the safety verification problem under RA has been shown to be undecidable for non-parameterized ($\text{env}$-free) systems from $\text{dis}_1 \left( \text{noca} \right) || \text{dis}_2 \left( \text{noca} \right) || \text{dis}_3$ and non-primitive-recursive for systems from $\text{dis}_1 \left( \text{noca} \right) || \text{dis}_2 \left( \text{noca} \right)$. There are several conclusions to draw from this.

With distinguished threads, we cannot hope to arrive at a tractable verification problem. We take the bounded model checking [28] approach and consider loop-free code. Acyclic programs, however, are not very expressive. Fortunately, RA implementations tend to be parameterized, and, as we will see, this frees us from the acyclicity restriction. The fact that parameterization simplifies verification has been observed in various works [5,33,39,46,62] that we discuss below.

Restricting the use of CAS requires an explanation. The class $\text{env}$ of unconstrained environment threads enables what we call leader isolation: an $\text{env}$ thread can distinguish itself from the others by acquiring a CAS-based lock. Even just $t$ CAS operations allows for the isolation of $t$ distinguished threads, which takes us back to the results of [1] for $t = 2$ resp. $t = 4$. Acyclicity will not help in this case, in section 5 we show that safety verification for $\text{env}(\text{acyc})$ is undecidable.

Contributions. We state our main results and present the technical details in the later parts.

A Simplified Semantics. We consider parameterized systems of the form $\text{env} \left( \text{noca} \right) || \text{dis}_1 || \cdots || \text{dis}_n$. Our first contribution is a simplified semantics (Section 4) that is equivalent with the standard RA semantics as far as safety verification is concerned. The simplified semantics uses the notion of timestamp abstraction, which allows us to be imprecise about the exact timestamps of the $\text{env}$ threads. Note that we do not make any assumptions on the form of the distinguished threads but support cyclic control flow and CAS. So the result in particular applies to the intractable classes from [1], even when extended with a parameterized environment. Supporting CAS in the distinguished threads is important. Without it, there is no way to capture the optimistic synchronization strategies used in performance critical programming [42].

We continue to apply the simplified semantics to prove tight complexity bounds for the safety verification problem in two particular cases of $\text{dis}$ programs.
Safety Verification of Parameterized Systems under Release-Acquire

**Loop-Free Setting.** In Section 5 we show a PSPACE-upper bound for the safety verification problem of parameterized programs from $\text{env}(\text{nocas}) \parallel \text{dis}_1(\text{acyc}) \parallel \cdots \parallel \text{dis}_n(\text{acyc})$. The class reflects the bounded model checking problem [28], which unrolls a given program into a loop-free under-approximation. Interestingly, we can squeeze into PSPACE the unbounded environment of cyclic threads. Our decision procedure is not only optimal complexity-wise, it also has the potential of being practical (we do not have experiments). We show how to encode the safety verification problem into the query evaluation problem for linear Datalog, the format supported by Horn-clause solvers [17,18], a state-of-the-art backend in verification.

**Leader Setting.** We continue to show an NEXPTIME-upper bound for $\text{env}(\text{nocas}) \parallel \text{dis}_1(\text{acyc}) \parallel \cdots \parallel \text{dis}_n(\text{acyc}) \parallel \text{ldr}$ in Section 6. These systems add an unconstrained distinguished thread, called the leader (denoted ldr), to the system from Section 5. The class is in the spirit of thread-modular verification techniques [35,57], where the safety of a single ‘ego’ thread is verified when interacting with an environment.

We note that these results delineate the border of tractability: adding another dis thread results in a non-primitive-recursive lower bound [1], and adding CAS operations to env results in undecidability (section 3).

**Lower Bounds.** Our last contributions are matching lower bounds for the two classes. Interestingly, they hold even in the absence of CAS. We show that the safety verification problem is PSPACE-hard already for $\text{env}(\text{nocas},\text{acyc})$, while it is NEXPTIME-hard for $\text{env}(\text{nocas},\text{acyc}) \parallel \text{ldr}(\text{nocas})$.

**Related Work.** There is a vast body of work on algorithmic verification under consistency models. Since our interest is in decidability and complexity, we focus on complete methods. We have already discussed the related work on RA and CC.

**Other Consistency models.** Atig et al. have shown that safety verification is decidable for assembly programs running on TSO, the consistency model of x86 architectures [11]. The result has been generalized to consistency models with non-speculative writes [12] and very recently to models with persistence [3]. It has also been generalized to parameterized programs executed by an unbounded number of threads [4]. Behind the decision procedures are (often drastic) reformulations of the semantics combined with well-structuredness arguments [6]. A notable exception is [5], showing that safety verification under TSO can be solved in PSPACE for cas-free parameterized programs, called $\text{env}(\text{nocas})$ here. On the widely-used Power architecture safety is undecidable [2].

The decidability and complexity of verification problems has been studied also for distributed databases and data structures. Enea et al. considered the problem of checking eventual consistency (EC) [66] of replicated databases and developed a surprising link to vector addition systems [23] that yields decidability and complexity results for the safety and liveness aspects of EC. For concurrent data structures, the default correctness criterion is linearizability wrt. a specification [43]. While checking linearizability is EXPSpace-complete in general [10,40], important data structures (for which the specification is then fixed) admit PSPACE-algorithms [21].

**Parameterized Systems with Asynchronous Communication.** We exploit a pleasant interplay between the asynchronous communication in RA and the parameterization of our systems in the number of threads. Kahlon [46] was the first to observe that parameterization simplifies verification in the case of concurrent pushdowns. Hague [39] showed that safety verification remains decidable when adding a distinguished leader thread. Esparza, Ganty, Majumdar studied the complexity of what is now called leader-contributor systems [33]. It is surprisingly
We model the individual threads in our system as (non-deterministic) sequential programs. Assume a standard while-language A parameterized system consists of an unknown and potentially large number of threads, all running the same program. Threads compute locally over a set of registers and interact like a leader. Moreover, our simplified semantics relies on an infinite-supply property the proof of which gives a copycat variant for RA. Our Datalog encoding is reminiscent of the notion of Strahler number

Leader-contributor systems are closely related to broadcast networks. Also there, safety verification has been found to be surprisingly cheap, namely PTIME-complete. For liveness verification, there was a gap between EXPSPACE and PTIME that was settled recently with a non-trivial polynomial-time algorithm. What is new in broadcast networks and neither occurs in leader-contributor systems nor in our setting is the problem of reconfiguration

2 The Release-Acquire Semantics

A parameterized system consists of an unknown and potentially large number of threads, all running the same program. Threads compute locally over a set of registers and interact with each other by writing to and reading from a shared memory. The interaction with the shared memory is under the Release Acquire (RA) semantics.

2.1 Program Syntax

We model the individual threads in our system as (non-deterministic) sequential programs. Assume a standard while-language Com defined by:

```
c ::= skip | assume e(r) | assert false | r ::= e(r) | c; c | c ⊕ c | c∗ |
r ::= x | x ::= r | cas(x, r1, r2)
```

The programs compute on (thread-local) registers r from the finite set Reg using assume, assert, assignments, sequential composition, non-deterministic choice, and iteration.
tionals if and iteratives while can be derived from these operators, and we use them where convenient. The shared memory variables $x$ are accessed only by means of load, store and compare-and-swap (CAS) operations as $r := x, x := r$ and $\text{cas}(x, r_1, r_2)$, respectively. These instructions are also referred to as events. We have a finite set $\text{Var}$ of shared variables, and work with the data domain $\text{Dom} = \mathbb{N}$. We do not insist on a shape of expressions $e$ but require an interpretation $[e]: \text{Dom}^n \to \text{Dom}$ that respects the arity $n$ of the expression.

### 2.2 Release-Acquire (RA) Semantics

We give the semantics of parameterized systems under release-acquire consistency. We opted for an operational [48, 59] over an axiomatic [52] definition, and follow [1]. What makes the operational definition attractive is that it comes with a notion of configuration or state of the system that we use to reason about computations. We first define thread-local configurations, then add the shared memory, and give the global transition relation.

**Local Configurations.** The RA semantics enforces a total order on all stores to the same variable that have been performed in the computation. We model these total orders by $\text{Time} = \mathbb{N}$ and refer to elements of $\text{Time}$ as timestamps. Using the total orders, each thread keeps track of its progress in the computation. It maintains a view from $\text{View} = \text{Var} \to \text{Time}$, a function, that for a shared variable $x$, returns the timestamp of the most recent event the thread has observed on $x$. Besides, the thread keeps track of the command to be executed next (which can be represented as program counter) and the register valuation from $\text{RVal} = \text{Reg} \to \text{Dom}$. The set of thread-local configurations is thus

$$\text{LCF} = \text{Com} \times \text{RVal} \times \text{View}.$$ 

**Unbounded Threads.** The number of threads executing in the system is not known a priori. As long as we restrict ourselves to safety properties, there are two ways of modeling this. One way is to define instance programs for a given number of threads, and then requiring correctness of all instances, as has been done in [19]. The alternative is to consider an infinite number of threads right away. We take the latter approach and define $\text{TID} = \mathbb{N}$ to be the set of thread identifiers. The thread-local configuration map then assigns a local configuration to each thread:

$$\text{LCFMap} = \text{TID} \to \text{LCF}.$$ 

**Views.** The views maintained by the threads are used for synchronization. They determine where in the (appropriate) total order a thread can place a store and from which stores it can load a value. To achieve this, the shared memory consists of messages, which are variable value pairs enriched by a view, with the form $(x, d, vw)$:

$$\text{Msgs} = \text{Var} \times \text{Dom} \times \text{View}.$$ 

**Shared Memory.** A memory state is a set of such messages, and we use $\text{Mem} = 2^{\text{Msgs}}$ for the set of all memory states. With this, the set of all configurations of parametrized systems under release-acquire is

$$\text{CF} = \text{Mem} \times \text{LCFMap}.$$ 

**Transitions.** To define the transition relation among configurations, we first give a thread-local transition relation among thread-local configurations $\rhd \subseteq \text{LCF} \times \text{LAB} \times \text{LCF}$ in Figure [1]. Thread-local transitions may be labeled or unlabeled, indicated by $\text{LAB} = \{\varepsilon\} \cup \{(\text{ld}, \text{st}, \text{cas}) \times \text{LAB} \times \text{LAB}\}$.
Mgs). The unlabeled transitions capture the control flow within a thread and properly handle assignments and assumes. They are standard. The message-labeled transitions capture the interaction of the thread with the shared memory. We elaborate on the load, store, and CAS transitions by which a thread with local view vw, interacts with the shared memory.

**Load.** A load transition \( r := x \) picks a message \( (x, d, vw') \) from the shared memory where \( d \) is the value stored in the message and updates its register \( r \) with value \( d \). The message should not be outdated, which means the timestamp of \( x \) in the message, \( vw'(x) \), should be at least the thread’s current timestamp for \( x \), \( vw(x) \). The timestamps of other variables do not influence the feasibility of the load transition. They are taken into account, however, when the load is performed. The thread’s local view is updated by joining the thread’s current view \( vw \) and \( vw' \) by taking the maximum timestamp per address; \( (vw \cup vw') = \lambda x, \max(vw(x), vw'(x)) \).

**Store.** When a thread executes a store \( x := r \) it adds a message \( (x, d, vw') \) to the memory, where \( d \) is the value held by the register \( r \). The new thread-local view (and the message view), \( vw' \), is obtained from the current \( vw \) by increasing the time-stamp of \( x \). We use \( vw <_x vw' \) to mean \( vw(x) < vw'(x) \) and \( vw(y) = vw'(y) \) for all variables \( y \neq x \).

**CAS.** A CAS transition is a load and store instruction executed atomically. \( \text{cas}(x, r_1, r_2) \) has the intuitive meaning \( \text{atomic}(r := x; \text{assume } r = r_1; x := r_2) \). The instruction checks whether the shared variable \( x \) holds the value of \( r_1 \) and, in case it does, sets it to the value of \( r_2 \). The check and the assignment happen atomically. Under RA, this means the timestamp \( ts \) of the load instruction and the timestamp \( ts' \) of the store instruction involved in the CAS should be adjacent, \( ts' = ts + 1 \).

The transition relation among configurations \( \rightarrow \subseteq CF \times TID \times \{Mgs \cup \{\epsilon\}\} \times CF \) is defined in Figure 2. It is labeled by a thread identifier and possibly message (if the transition interacts with the shared memory). The relation expects a thread \( t \) which performs the transition. In the case of local computations, there are no more requirements and the transition propagates to the configuration. In the case of loads, we require the memory to hold the message to be loaded. In the case of stores, the message to be stored should not conflict with the memory. In the case of CAS, we require both of the above, and that the two messages should have consecutive timestamps. We defer the definition of non-conflicting messages for the moment until we can give it in broader perspective.

Fix a parametrized system of interest \( c \). The initial thread-local configuration is \( \text{lcf}_\text{init} = (c, r_0, vw_0) \), where the register valuation assigns \( r_0(r) = 0 \) to all registers and the view has \( vw_0(x) = 0 \) for all \( x \in \text{Var} \). The initial configuration of the parametrized system is \( cf_0 = (\text{Mem}_\text{init}, \text{lcf}_\text{init}) \) with an initial memory \( \text{Mem}_\text{init} \) consisting of messages where all shared variables store the value \( d_{\text{init}} \in \text{Dom} \), along with the initial view which assigns time stamp 0 to all shared variables, and \( \text{lcf}_\text{init}(t) = \text{lcf}_\text{init} \) for all threads. A computation (or a run) is a finite sequence of consecutive transitions

\[
\rho = cf_0 \xrightarrow{(t_1, \text{msg}_1)} cf_1 \xrightarrow{(t_2, \text{msg}_2)} \ldots \xrightarrow{(t_n, \text{msg}_n)} cf_n.
\]

The computation is initialized if \( cf_0 = cf_\text{init} \). We use \( TS(\rho) \) for the set of all non-zero timestamps that occur in all configurations across all variables. We use \( TID(\rho) \) to refer to the set of thread identifiers labeling the transitions. For a set \( TID' \subseteq TID \) of thread identifiers, we use \( \rho \downarrow_{TID'} \) to project the computation to transitions from the given threads. With \( \text{first}(\rho) = cf_0 \), \( \text{last}(\rho) = cf_n \) we access the first/last configurations in the computation.

**Example 1.** Consider the program given in Figure 3 which implements a simplified version of the Dekker’s mutual exclusion protocol for two threads. There are two shared variables \( x \)
8 Safety Verification of Parameterized Systems under Release-Acquire

and y. Both x, y are initialized to 0, and at instructions λ₀, λ₀' the registers r₁, r₁' are initialized to 1. The first thread t₁ signals that it wants to enter the critical section by writing the value 1 to x. It then checks if thread t₂ has asked to enter the critical section by reading the value of y and storing it into the register r₁. The thread t₁ is allowed to enter the critical section only if the value stored in the register r₁ is 0. The second thread t₂ behaves in a symmetric manner.

Variables x and y have been initialized to 0

| Thread t₁                  | Thread t₂                  |
|---------------------------|---------------------------|
| λ₀ : r₁ := 1              | λ₀' : r₁' := 1            |
| λ₁ : x := r₁             | λ₁' : y := r₁'            |
| λ₂ : r₁ := y             | λ₂' : r₁' := x            |
| λ₃ : if(r₁ == 0) :        | λ₃' : if(r₁' == 0) :      |
|                          |                          |
| m_{init}                 | m_{init}                 |
| [x, y] := [0, 0]          | [x, y] := [0, 0]          |
| m_{merge}                | m_{merge}                |
| [x, y] := [10, 7]         | [x, y] := [10, 7]         |
| m_{l₁}                   | m_{l₁}                   |
| x := r₁, y := r₁'        | x := r₁, y := r₁'        |
| m_{l₂}                   | m_{l₂}                   |
| x := r₁', y := r₁        | x := r₁', y := r₁        |

Figure 2 On the top, is a simplified version of Dekker’s mutual exclusion protocol. Below, is a partial execution sequence under RA. The rectangles show the contents (messages) of the shared memory. Messages have three components - (1) the variable, (2) value of the message and (3) the message view - a map from \{x, y\} to the set of timestamps \text{Time}(\mathbb{N}). The lines below show the thread-local state - instruction-pointer, register valuation and thread-local view.

Under Sequential Consistency (SC) [54], which is a stronger notion of consistency, the mutual exclusion property (i.e., at most one thread is in the critical section at any time) is preserved. However, this is not the case under the RA memory model. To see why, consider the execution sequence presented in Fig 2. At each instant, the figure shows where the instruction-counter (i.e., the label of the next instruction to get executed) resides in each of the threads, along with the values of the registers. The black arrows with instruction labels λ₁, λ₁' show the evolution of the run on executing the instruction labeled λ₁, λ₁' respectively. Let mₐ represent the memory obtained after executing the instruction labeled λ, and let msgₐ be the unique new message (if any) that is part of mₐ after the execution of the instruction labeled λ. The initial memory is m_{init} where x, y have values and timestamps 0; msgₓ, msgᵧ represent the messages in m_{init} corresponding to x, y. The execution of the instruction labeled by λ₁ results in the addition of a new message msgₓ₁ to the memory whose timestamp (10) is higher than 0 (which is the current timestamp of the variable x for t₁). The view of t₁ is then updated to x := 10, y := 0. Likewise, the execution of the instruction labeled by λ₁' results in the addition of a new message msgᵧ₁ to the memory with a higher time stamp (7). This will result in the update of the view of t₂ to x := 0, y := 7, wrt. the variable y. The read instruction labeled by λ₂ is then allowed to use the message msgᵧ to fetch the value of y, since the view of t₁ wrt. y is 0. Likewise, in the case of t₂ concerning the execution of the instruction labeled by λ₂', the message msgₓₜ is used since the view of t₁ wrt. x is 0. After these steps, both threads enter their respective critical section.
2.2.1 Conflict

We need a notion of conflict not only for messages, but also for memories, configurations, and computations. Two messages are non-conflicting, denoted by \((x_1, d_1, \text{vw}_1) \neq (x_2, d_2, \text{vw}_2)\), if either their variables are different, \(x_1 \neq x_2\), the timestamps are different, \(\text{vw}_1(x_1) \neq \text{vw}_2(x_2)\), or the timestamps are zero, \(\text{vw}_1(x_1)=0=\text{vw}_2(x_2)\). Observe that initial messages do not conflict with any other message.

Two memory states are non-conflicting, \(m_1 \neq m_2\), if for all \(\text{msg}_1 \in m_1\) and all \(\text{msg}_2 \in m_2\) we have \(\text{msg}_1 \neq \text{msg}_2\). Two configurations are non-conflicting, \(\text{cf}_1 \neq \text{cf}_2\), if their memory states are non-conflicting. Two computations are non-conflicting, denoted \(\rho \neq \rho'\), if they use different threads and non-conflicting messages, \(\text{TID}(\rho) \cap \text{TID}(\rho') = \emptyset\) and \(\text{last}(\rho) \neq \text{last}(\rho')\).

3 Undecidability of \(\text{env}(\text{acyc})\)

In this section, we establish the undecidability of the class \(\text{env}(\text{acyc})\), that is the class with loop-free \(\text{env}\) threads (which can execute arbitrarily-many CAS operations) and without any \(\text{dis}\) threads. This result essentially shows that even with the loop-free assumption, allowing \(\text{env}\) threads to perform CAS operations is in itself intractable from a safety verification viewpoint. Hence, the \(\text{nocas}\) restriction that we impose on \(\text{env}\) threads is a justified means of achieving tractability.

In fact, we will show a stronger result. We will show that we can transform a non-parametrized system consisting of \(k\) distinguished threads having full instruction set and loops under RA (the class \(\text{dis}_{\text{acyc}}\)) to a parameterized system corresponding to the class \(\text{env}(\text{acyc})\) such that, control-state reachability is preserved. With this equivalence, the claim would follow by the undecidability result of [1].

3.1 Constructing the equivalent loop-free program

To show this result, we transform an input of \(n\) programs \(\{c_1, c_2, \cdots, c_n\}\) and a failure state label \(\lambda_{\text{fail}}\) in some \(c_i\) (with possibly full instruction set and loops) and transform them into a single program \(c_{\text{env}}\) and failure state \(\lambda_{\text{fail}}\), the control flow for which is loop-free but uses the full instruction set including CAS operations. We claim that the state label \(\lambda_{\text{fail}}\) is reachable in \(\text{dis}_{1} \parallel \cdots \parallel \text{dis}_{n}\) with \(\text{dis}_{i}\), executing \(c_i\) if and only if the state label \(\lambda_{\text{fail}}\) is reachable in the system \(\text{env}(\text{acyc})\) with the environment threads executing \(c_{\text{env}}\). Let the variable set, data domain and register set of the original system be \(\text{Var}, \text{Dom} \text{ and } \text{Reg} = \{r_1, \cdots, r_k\}\) as usual.

We assume that the memory is initialized to 0 on all variables.

Converting a single program \(c_i\) to \(c'_i\) We show how we can convert one thread program \(c_i\) into a loop-free program \(c'_i\) and then show how we can combine all the programs together into a single loop-free program \(c_{\text{env}}\). Consider for an \(i\), the program \(c_i\). For the purposes of this construction, we will assume that the program \(c_i\) has been specified as a transition system rather than in the while-language syntax. It is clear that both representations are equivalent and can be interconverted with only polynomial overhead. Hence we assume that \(c_i = (Q, \Delta, \iota)\) where \(Q\) is the set of control states, \(\Delta\) is the transition relation and \(\iota\) maps each transition to its corresponding instruction from \(\{	ext{skip}, \text{assume } e(\bar{r}), r := e(\bar{r}), r := x, x := r, \text{cas}(x, r_1, r_2)\}\). We transform \(c_i\) to a loop-free program as follows. Let \(Q' = \{q_0, \cdots, q_n\}\) and with \(q_0\) as the initial state.

In this conversion, we add extra variables and values such that \(\text{Var}' = \text{Var} \cup \{t_1, t_2, \cdots, t_{\text{Reg}}\}\) and \(\text{Dom}' = \text{Dom} \cup \{0, \cdots, |Q| - 1, \lambda^+\}\) where \(\cup\) denotes disjoint union. Now we specify the new transition system \(c'_i\) which needs to be loop-free. For each transition
\( \vartheta = (q_0, q_0) \in \Delta \), with source and end states \( q_0 \) and \( q_0 \) respectively and instruction \( i(\vartheta) \), we transform it into the following three transition sequence (a sequence of green transitions starting with a CAS, followed by \( k \) load operations; the transition corresponding to \( i(\vartheta) \), followed by the sequence of pink transitions consisting of \( k \) store operations ending with a CAS) denoted as \( f(\vartheta) \).

\[
\begin{align*}
    f(\vartheta) &= q_{\text{start}} \xrightarrow{\text{cas}(t, a, \lambda^+)} q_0 \xrightarrow{t_1 := t_1^i} q_0^i \xrightarrow{\ldots} q_0^i \xrightarrow{k_{i-1}} q_0^i \xrightarrow{\ldots} q_0^i \xrightarrow{k_i} q_0^i \xrightarrow{i(\vartheta)} q_0^i \xrightarrow{k+1} \ldots \quad (\text{contd. below})
    
    \ldots \xrightarrow{q_0^i} q_0^i \xrightarrow{k+2} \ldots q_0^i \xrightarrow{2k_{i-1}} q_0^i \xrightarrow{t_k := t_k} q_0^i \xrightarrow{\text{cas}(t, \lambda^+, b)} q_0^i \xrightarrow{q_\text{end}}
\end{align*}
\]

We construct \( f(\vartheta) \) for each transition \( \vartheta \) in \( \Delta \) to get the complete transition system. The initial/final (collectively called terminal) nodes of this transition system are \( q_{\text{start}}, q_{\text{end}} \) (which are common to all \( f(\vartheta) \)). The internal \( q_0^i \) states are all distinct across the \( f(\vartheta) \) for different \( \vartheta \). The transition system that we obtain has size \( O(|\text{Reg}| \cdot |\Delta|) \) (each original transition from \( q_0 \) to \( q_0 \) is transformed into a sequence of \( 2|\text{Reg}| + 3 \) transitions between \( q_{\text{start}} \) and \( q_{\text{end}} \)). It is clearly loop-free. See Figure 3 showing an example if we start with \( \text{dis}_i \parallel \text{dis}_j \).

**Combining individual** \( c_i \) We construct programs \( c_i \) as described above for each thread \( \text{dis}_i \). Now we combine these individual programs into a single program \( c_{\text{env}} \). We ensure that the newly added shared variables (\( t_i, t_j \) for \( \text{dis}_i \)) are also disjoint across threads. Hence the variable set is now \( \text{Var}' = \text{Var} \cup \{ t_1, \ldots, t_n \} \cup \{ t_i' \}_{i \in [n], j \in |\text{Reg}|} \) (where \( \text{Var} \) was the original variable set \( \{ c_1, c_2, \ldots, c_n \} \) were operating with). Finally, the combined data domain is simply a union of individual data domains (which possibly overlap). We combine the individual programs as

\[
c_{\text{env}} = c_1 \oplus c_2 \oplus \cdots \oplus c_n
\]

where \( \oplus \) denotes non-deterministic choice. It is clear that \( c_{\text{env}} \) is loop-free. Additionally, \( |c_{\text{env}}| \), and the new \( |\text{Dom}'| \) and \( |\text{Var}'| \) is polynomial in \( \sum_i |c_i| \) and previous \( |\text{Var}| \) and \( |\text{Dom}| \).

**Figure 3** Examples of two \( \text{dis} \) threads \( \text{dis}_i \) and \( \text{dis}_j \) executing programs \( c_i \), \( c_j \) and the corresponding transformed programs \( c_i' \), \( c_j' \). The program \( c_i \) has 2 transitions while \( c_j \) has 3 transitions. Note how the read-write value for CAS operations in the transformed program match with the transitions in the original program.

### 3.2 Proof of Equivalence

We now prove that the system \( \text{env}(\text{acyc}) \) with the \( \text{env} \) threads executing the program \( c_{\text{env}} \) as defined above respect the original system. We defer the notion of ‘maintaining reachability’
for a bit later. We first observe the program $c_{\text{env}}$ and make some observations.

### 3.2.1 Simulation of individual threads

**Locking/unlocking of $c'_i$.** For any single transformed program $c'_i$, we note that at any given point, only one thread can be in any internal (not initial/final) state of $c'_i$. To see this, note the two atomic CAS operations flanking each 3-path in $c'_i$. All these CAS operations are on the same variable $t_i$ and moreover there are no other operations on $t_i$. Hence at any given point in time, there is only one message on $t_i$ (the most recent write) that is available for a CAS operation. The value of this message dictates whether the operation will succeed. When it succeeds, the most recent write value changes to the value written by the CAS.

Now note that $t_i$ is initialized with value 0; hence initially one thread, say $t$ can take perform a CAS and change the recent value to $\Lambda \bot$. Now, there is no transition from $q_{\text{start}}$ that performs a CAS with a read of $\Lambda \bot$. Hence all other threads are kept waiting until the recent value on $t_i$ changes from $\Lambda \bot$. This is possible only when the initial thread $t$, executes the final transition and reaches $q_{\text{end}}$, maintaining the claim. Hence these CAS operations perform the role of a mutual-exclusion lock. But then they perform another function too.

**State transference.** We now know that for each $i$, only one thread may execute $c'_i$ at any given time. However the locking/unlocking operations using CAS also enable threads to transfer their state to their successors. There are three components to the state, which we handle in turn:

- **Control-state:** Note that the recent value on variable $t_i$ is $v \neq \Lambda \bot$ only if the previous thread terminated after simulating some transition ending at $q_v$. Additionally, a locking CAS operation for $f(\partial)$ reads value $v$ only if $\partial$ is a transition from $q_v$ to some other state. Hence, it is guaranteed that the successive thread will execute some transition that emerges from a state where the previous thread left off. Note how this is true for the first thread as well since the initial value on all variables is 0 and the initial state of the transition system is $q_0$.

- **View:** The second component that we consider is the view. This also is transferred from a thread to its successor through the CAS operation. In particular, when a thread $t$ executes the final CAS operation to reach $q_{\text{end}}$, it generates a message on $t_i$ which is read by its successor. This read implies that the successor will take the join on its own (initial) view with that of the message and hence essentially accumulate the exact view that the previous thread left with. So, the view is transferred as well.

- **Register valuations:** The previous thread $t$ stores its register valuations in the shared variables $r_{ij}$ in the final sequence of store operations before terminating. These are then accessed by the successor thread through the initial sequence of load operations.

In this way we see that not only is exclusion ensured, but the thread states are transferred from one thread to the next. Together, these sequences of threads simulate the entire run of the original $\text{dis}_i$ in fragments. The above holds for all $i \in [n]$. Hence at any given point, there are at most $n$ threads simulating the original ones.

### 3.2.2 The Complete Simulation

Now we formalize the notion of equivalence in reachability. We say that an original state with the threads $\{\text{dis}_1, \cdots, \text{dis}_n\}$ is equivalent to a new state when we have the following.

- if the control states of threads $\{\text{dis}_1, \cdots, \text{dis}_n\}$ are $(q_{i_1}, q_{i_2}, \cdots, q_{i_n})$ respectively then in the new system with $\text{env}$, the recent value of shared variable $t_j$ is $i_j$. 


the register valuation of each original \( \text{dis}_i \) is reflected (\( r_j = \text{most recent write to } r_{i,j} \)) in the most recent writes to the variables \( r_{i,j} \) for each thread \( i \),
- the view of \( \text{dis}_i \) is the view stored in the most recent message to \( t_i \) (again projected on the original variable set) and
- the global memory (projected) is identical across the original and \( \text{env} \) states.

We claim the following: a state in the original system can be reached if and only some equivalent state in the new system can be reached. We can prove this by induction. The base case is that all threads are in their initial states, registers and views with the memory only with initial messages (0 on each variable). This trivially satisfies the requirement, both in the forward and reverse directions.

Now for the inductive case (\( \Rightarrow \)). Assume that it was true at some instant. Let some \( \text{dis}_i \) execute an instruction for the transition \( \partial \). In the new system, we can simulate this as a new \( \text{env} \) thread \( t \) taking the path corresponding to \( f(\partial) \) in \( c'_i \). We note by the observations above that the invariants for the thread-local state (control-state, register valuations and view) is maintained. Additionally, if \( \text{dis}_i \) wrote a message to the memory, then so can \( t \). In particular, since the view of \( t \) is obtained from the CAS read, it matches that of \( \text{dis}_i \). Hence the message added by \( t \) can have the same timestamps as \( \text{dis}_i \).

Inductive case (\( \Leftarrow \)). The same argument works in the reverse direction. Assume that a pair of equivalent states have been reached. Now, consider a \( \text{env} \) thread path \( f(\partial) \) in \( c'_i \) where \( \partial = (q_a, q_b) \). Then, by the induction hypothesis this means that \( \text{dis}_i \) is in state \( q_a \) in the original run. Given the equality of thread and memory state initially, it too can take the transition \( (q_a, q_b) \). Once again, the invariant follows from the earlier observations.

This gives a sketch of the proof. In particular, note that even though we give an equivalence between the control state in the original system and a variable value in the new system, this can be easily converted to an equivalence between control states themselves. This means that the reachability problem for \( \text{dis}_1 \parallel \cdots \parallel \text{dis}_n \) can can converted to a reachability problem for \( \text{env} \text{(acyc)} \). This prompts us to restrict \( \text{env} \) threads to a reduced (cas-free) instruction set and motivates the idea of modelling CAS instructions in a run via computations of the \( \text{dis} \) threads.

## 4 A Simplified Semantics

In this section, we propose a simplified semantics for the class of systems given by \( \text{env}(\text{nocas}) \parallel \text{dis}_1 \parallel \cdots \parallel \text{dis}_n \). The core of this result relies on the *Infinite Supply Lemma* which shows that if some \( \text{env} \) thread could generate a message \( (x, \text{val}, \text{vw}) \), then a clone of that thread could generate the message \( (x, \text{val}, \text{vw}') \) with \( \text{vw}' = \text{vw}[x \mapsto t] \) for some \( t > \text{vw}(x) \).

There are two assumptions that the infinite supply lemma and hence our semantic simplification result rely on:

- arbitrarily many \( \text{env} \) threads executing identical programs.
- the \( \text{env} \) threads do not have atomic instructions (CAS).

The first assumption allows us to have clone \( \text{env} \) threads that duplicate the computation and hence the messages generated in it. The second assumption is required for the duplicated computation to remain valid under RA.

While performing the duplication, one must keep in mind the dependency between stores and loads across threads. The fact that \( \text{dis} \) threads are not replicatable (their messages cannot be duplicated) adds to the challenge. To ensure that the clone threads can follow in the footsteps of the original computation we require that \( \text{dis} \) messages can be read by the
**env** clones whenever they can be read by the original **env** threads. This necessitates that we respect relative order among timestamps between **env** and **dis** threads.

We develop some intermediate concepts that help us in developing a valid duplicate run. In order to accommodate the clone threads, we must make space (create unused timestamps) along **Time** for clones to write messages. We do this via *timestamp liftings*. Having done this, we need to define how we can combine the original computation with that of the clones. We develop the concept of *superposition* of computations to do this. Finally, the infinite supply (of messages) lemma shows how, using the earlier two concepts, we can generate copies of messages, with higher timestamps.

This ‘duplication-at-will’ of **env** messages means that we need not store the entire set of **env** messages produced. Those with the smallest timestamps act as good representatives of the set. Additionally when any thread reads from an **env** message, we need not be bothered about timestamp comparisons since we could always generate a copy of that message with as high timestamp as required. It is this observation that gives us the timestamp abstraction and with it the simplified semantics.

### 4.1 Infinite Supply

We now make these arguments precise. Our strategy is to split up the timestamps (hence the computation) and separate the part originating from the **dis** threads from the **env** part (which can be duplicated at will). We write \( \rho^\downarrow_{\text{env}} \) and \( \rho^\downarrow_{\text{dis}} \) to denote the projections of \( \rho \) to **env** and **dis** respectively.

#### 4.1.1 Timestamp Lifting

In our development we will make use of *timestamp transformations* \( \text{tf} : \text{Time} \rightarrow \text{Time} \). We extend these to views \( \text{vw} \) with *per variable* timestamp transformations \( \text{tf} = \{ \text{tf}^x \}_{x \in \text{Var}} \), where \( \text{tf}^x \) only transforms the timestamps for the variable \( x \). The transformed view \( \text{tf}(\text{vw}) : \text{Var} \rightarrow \text{Time} \) is defined by \( \text{tf}(\text{vw})(x) = \text{tf}^x(\text{vw}(x)) \) for every variable \( x \).

As an example consider shared variables \( x,y \) and views \( \text{vw}_1, \text{vw}_2 \) such that \( \text{vw}_1 = [x \mapsto 2,y \mapsto 5] \) and \( \text{vw}_2 = [x \mapsto 10,y \mapsto 0] \). Using the timestamp transformation \( \text{tf} = \{ \text{tf}^x, \text{tf}^y \} \) where \( \text{tf}^x(0) = \text{tf}^x(t) = t+2 \) and \( \text{tf}^y(t) = t+7 \) for \( t > 0 \), we obtain \( \text{tf}(\text{vw}_1) = [x \mapsto 4,y \mapsto 12] \) and \( \text{tf}(\text{vw}_2) = [x \mapsto 12,y \mapsto 0] \). We also apply the timestamp transformation to messages, memories, configurations, and computations by transforming all view components.

**RA-valid timestamp lifting.** An **RA-valid timestamp lifting** for a run \( \rho \) is a (per variable) timestamp transformation \( \mathcal{M} = \{ \mu^x \}_{x \in \text{Var}} \) satisfying two properties for each \( x \in \text{Var} \): (1) it is strictly increasing, \( \mu^x(0) = 0 \); for all \( t_1, t_2 \in \mathbb{N} \) with \( t_1 < t_2 \) we have \( \mu^x(t_1) < \mu^x(t_2) \) and (2) if there is a CAS operation on \( x \) with (load, store) timestamps as \( t, t+1 \) then \( \mu^x(t+1) = \mu^x(t) + 1 \), i.e. consecution of CAS-timestamps is maintained. Note that \( \mu(\text{cf}_{\text{init}}) = \text{cf}_{\text{init}} \). In the example above, \( \text{tf} \) is a **RA-valid timestamp lifting**.

**Lemma 2** *(Timestamp Lifting Lemma).* Let \( \mathcal{M} = \{ \mu^x \}_{x \in \text{Var}} \) be an **RA-valid timestamp lifting**. If \( \rho \) is a computation under **RA**, then so is \( \mathcal{M}(\rho) \). Hence if a configuration \( \text{cf} \) is reachable under **RA** then so is \( \mathcal{M}(\text{cf}) \).

**Proof.** This result follows since timestamp lifting is just a relabelling of timestamps for each shared variable. The lemma relies on the following facts/observations:
There are no timestamp comparisons across variables, $\forall \mathbf{x} \forall \mathbf{x}' \, \forall \mathbf{w}(\mathbf{x}) \neq \forall \mathbf{w}(\mathbf{x}')$ for $\mathbf{x} \neq \mathbf{x}'$.

The relative order between timestamps on the same variable is preserved due to the strictly increasing property. Additionally, $\mu(0) = 0$, maintaining the timestamps of the init messages.

The load, store timestamps of (CAS-LOCAL) operations still remain consecutive.

In particular the lemma can be formally proven by induction on the length of the run. The base case is trivial and the inductive case follows by showing that each instruction - read, write, CAS - that can be executed in $\rho$ can be executed in the lifted run, $\mathcal{M}(\rho)$.

The duplication of messages by the clone $\text{env}$ threads requires us to copy computations and then merge them such that the RA semantics are not violated. This requires (1) timestamps of merging computations to not conflict and (2) the reads-from dependencies between threads are respected. With this in mind, we introduce the idea of superposition.

4.1.2 Superposition

We define the superposition $\rho \triangleright \rho'$ of two computations $\rho, \rho'$ as the computation that first executes $\rho$ and then $\rho'$. This requires us to combine the memory in $\text{last}(\rho)$ with that of every configuration in $\rho'$. Moreover, the threads transitioning in $\rho, \rho'$ must be disjoint. Given these considerations, the operation requires the computations to be non-conflicting, $\rho \neq \rho'$ (see Section 2.2.1), and is defined as follows:

$$\rho \triangleright \rho' = \rho; (\text{last}(\rho) + \rho').$$

The addition of a configuration $\mathbf{cf}$ to a computation $\rho = \mathbf{cf}_0 \xrightarrow{(t_1, \text{msg}_1)} \ldots \xrightarrow{(t_n, \text{msg}_n)} \mathbf{cf}_n$ yields the new computation

$$\mathbf{cf} + \rho = (\mathbf{cf} + \mathbf{cf}_0) \xrightarrow{(t_1, \text{msg}_1)} \ldots \xrightarrow{(t_n, \text{msg}_n)} (\mathbf{cf} + \mathbf{cf}_n).$$

Addition of configurations $\mathbf{cf}_1 = (\mathbf{m}_1, \text{lcfm}_1)$ and $\mathbf{cf}_2 = (\mathbf{m}_2, \text{lcfm}_2)$ is the configuration $\mathbf{cf}_1 + \mathbf{cf}_2 = (\mathbf{m}_1 \cup \mathbf{m}_2, \text{lcfm})$, where $\text{lcfm}(t) = \text{lcfm}_1(t)$ if $\text{lcfm}_1(t) \neq \text{lcfm}_2(t)$ and $\text{lcfm}(t) = \text{lcfm}_2(t)$ otherwise.

When $\rho \neq \rho'$ holds, we have: (1) for any thread $t$, if it has transitioned in $\rho$, then it cannot in $\rho'$; likewise, if it has not transitioned in $\rho$, then it can in $\rho'$.

(2) $\text{last}(\rho) \neq \text{last}(\rho')$, and since the memory in earlier configurations of $\rho$ is a subset of that in $\text{last}(\rho)$, the memory unions performed above involve nonconflicting memories. An initial configuration is neutral for addition, in particular $\text{last}(\rho') + \text{first}(\rho) = \text{last}(\rho')$. The operation of concatenation $\rho_1; \rho_2$ expects two computations $\rho_1$ and $\rho_2$ that satisfy $\text{last}(\rho_1) = \text{first}(\rho_2)$ and returns the sequence consisting of the transitions in $\rho_1$ followed by the transitions in $\rho_2$. This need not be a valid computation under RA, but under the following conditions it is.

Let $\text{Msgs}(\rho)$ be the memory in $\text{last}(\rho)$. Likewise, let $\text{Msgs}(\rho \downarrow \text{dis}) \subseteq \text{Msgs}(\rho)$ be the subset of memory in $\text{last}(\rho)$, which have been added by $\text{dis}$ threads during $\rho$.

\textbf{Lemma 3 (Superposition).} Consider valid computations $\rho, \rho'$ of a parametrized system under RA such that $\rho \downarrow \text{env} \# \rho' \downarrow \text{env}$ and that $\text{Msgs}(\rho \downarrow \text{dis}) = \text{Msgs}(\rho' \downarrow \text{dis})$. Then the superposition $\rho \triangleright \rho' \downarrow \text{env}$ is a valid computation under RA.

\textbf{Proof.} Since there are arbitrarily many $\text{env}$ threads, we distinguish apart the $\text{env}$ threads in $\rho'$ from the $\text{env}$ threads in $\rho$. By doing so we ensure that the threads operating (changing state) in $\rho$ and $\rho' \downarrow \text{env}$ are disjoint.
Now consider the global state obtained after executing $\rho$ (which is a valid run under RA). By hypothesis, the memory state contains messages from $\rho \downarrow_{\text{dis}}$, which are identical to those in $\rho' \downarrow_{\text{dis}}$. After execution of $\rho$ is complete, we claim that we can execute $\rho' \downarrow_{\text{env}}$ one step at a time.

- Whenever a $\text{dis}$ thread loads from a message generated by an $\text{env}$ thread in $\rho$, the same can happen in $\rho \triangleright \rho' \downarrow_{\text{env}}$. Likewise, the relative time stamps between the $\text{dis}$ threads and the $\text{env}$ threads in $\rho'$ are the same; so $\rho' \downarrow_{\text{env}}$ can be executed after $\rho$.
- Likewise, reads made by some $\text{env}$ thread on $\rho, \rho'$ either from another $\text{env}$ thread or a $\text{dis}$ thread also continues exactly in the same way in $\rho \triangleright \rho' \downarrow_{\text{env}}$, since the messages added by $\text{dis}$ threads are exactly same in $\rho, \rho'$, and the $\text{env}$ threads are disjoint.
- The above two points show that we have exactly the same reads-from dependencies ($\text{dis} \leftrightarrow \text{env}$ in $\rho$, $\text{dis} \leftrightarrow \text{env}$ in $\rho'$) in $\rho \triangleright \rho' \downarrow_{\text{env}}$. The reason is that $\text{env}$ threads are disjoint and the messages added by $\text{dis}$ threads are the same in $\rho, \rho'$. Finally, all writes made by the respective $\text{env}$ threads of $\rho, \rho'$ can be done in $\rho \triangleright \rho' \downarrow_{\text{env}}$; likewise, all writes made by the $\text{dis}$ threads in $\rho$ can also be made in $\rho \triangleright \rho' \downarrow_{\text{env}}$. The reason is that $\rho \downarrow_{\text{env}} \# \rho' \downarrow_{\text{env}}$, and trivially, we have $\rho' \downarrow_{\text{dis}} \# \rho' \downarrow_{\text{env}}$. This ensures no conflict of write-timestamps.

Formally this can be proven by induction on the length of $\rho'$.

Now we develop the infinite supply lemma. Recall that our goal is to generate arbitrarily many copies of $\text{env}$ messages with the same variable and value but higher timestamp. Let us fix a message, $\text{msg} = (x, d, v\nu)$, for our discussion here and see how we can replicate it. Towards this end, consider a computation $\rho$ in which it is generated. We ‘spread-apart’ the timestamps of $\text{Msgs}(\rho)$, using timestamp liftings so that we create ‘holes’ (unused timestamps) along $\text{Time}$. Then we generate copies of $\text{env}$ threads, denoted as $\text{copy}(\text{env})$ (possible since $\text{env}$ threads can be replicated).

The holes accommodate for the timestamps of $\text{copy}(\text{env})$ and the (higher) timestamp of the copy of $\text{msg}$. Throughout this, we preserve the order of timestamps of $\text{env}, \text{copy}(\text{env})$ threads relative to those of $\text{dis}$ threads. This ensures that reads-from dependencies are maintained - $\text{copy}(\text{env})$ can read a $\text{dis}$ message whenever $\text{env}$ can do so.

We define the computation $\tilde{\rho}$ as a copy of $\rho \downarrow_{\text{env}}$ executed by $\text{copy}(\text{env})$ threads. The write timestamps used by $\text{copy}(\text{env})$ threads are the unoccupied timestamps generated by the timestamp lifting operation $\mathcal{M}(\rho)$. We show an example of this via a graphic. Let $eT^1$ and $dT^1$ respectively denote the timestamps chosen by $\text{env}$ and $\text{dis}$ along $\rho$ (first row).

$$
\rho: \text{init } dT^0 \quad eT^0 \quad dT^1 \quad eT^1 \quad eT^2
$$

$$
\mathcal{M}(\rho): \text{init } dT^0 \quad eT^0_a \quad eT^0_b \quad dT^1 \quad eT^1_a \quad eT^1_b \quad eT^1_c \quad eT^1_d \quad eT^1_e
$$

$$
\tilde{\rho}: \text{init } dT^0 \quad eT^0_a \quad eT^0_b \quad dT^1 \quad eT^1_b \quad eT^1_c \quad eT^1_d \quad eT^2_b \quad eT^2_c
$$

The second row shows lifted timestamps (with subscript $a$) of $\mathcal{M}(\rho)$ and the holes (faded). The third row shows holes being used by $\text{copy}(\text{env})$ for $\tilde{\rho}$ (these have subscript $b$). The construction guarantees $\mathcal{M}(\rho) \not\approx \tilde{\rho}$ and superposition $\mathcal{M}(\rho) \triangleright \tilde{\rho}$ is allowed. In this computation, $\tilde{\rho}$ generates a copy of $\text{msg}$, $\text{msg}' = (x, v, v\nu')$ with higher $\nu\nu'(x)$. Additionally, since $eT^1_a, eT^1_b$ have the same position relative to all $dT^1$ timestamps, so will $\nu\nu'(y)$, $\nu\nu'(y)$ for $y \neq x$.

Now we state the Infinite Supply Lemma. As helper notation, for a run $\rho$ and each variable $x$, we denote the timestamps of stores of $\text{dis}$ threads on $x$ as $ts^*_0 < ts^*_1 < \cdots$.

**Lemma 4 (Infinite Supply).** Let $\rho$ be a valid run under the RA semantics, in which the message $(x, d, v\nu)$ has been generated by an $\text{env}$ thread. Then for each timestamp $i^* \in \mathbb{N}$, there
exist two timestamp lifting functions \( M_1, M_2 \) and a run \( \rho_1 \) such that \( M_1(\rho_1) \triangleright M_2(\rho_{\text{env}}) \triangleright \rho_1 \) is a valid run. This run contains a message \((x, d, vw')\) satisfying \((ts \text{ is from } \rho)\)

1. \( \forall i \ (t^* \leq ts^i \wedge vw(x) \leq ts^i_x) \implies vw'(x) \leq \mu^i_v(ts^i_x) \)
2. \( \forall i \ (vw'(x) \geq \mu^i_v(ts^i_v)) \)
3. \( \forall x' \neq x, \forall i \ (vw(x') \leq ts^i_{x'}) \implies vw'(x') \leq \mu^i_v(ts^i_{x'}) \)

**Proof.** Without loss of generality, we assume that in the run \( \rho \), the timestamps on each variable are consecutive. If that is not the case, we can always use a timestamp lowering operation that ‘fills in the gaps’ between non-consecutive timestamps, while maintaining consecution of the load/store timestamps of \((\text{CAS-local})\) operations.

We will give a constructive proof. We specify \( M_1(\rho) \triangleright M(\rho_{\text{env}}) \triangleright \rho_1 \) by defining \( M_1, M_2 \) and \( \rho_1 \), and showing that the resulting run is valid under RA. Then we show how a copy of the message \((x, d, vw)\) can be obtained as claimed.

First, we describe how to copy runs.

1. **Copying a run.** For a variable \( x \), we define the lifting functions as follows. With the consecuteness assumption, the messages on \( x \) have consecutive timestamps and are generated by either \( \text{dis} \) or \( \text{env} \), which we will denote below as \( \text{dis}^T \) and \( \text{env}^T \) respectively. For developing intuition quickly, consider the following sequence of consecutive timestamps on some variable.

\[
\text{init } \text{dis}^T_0 \text{ dis}^T_1 \text{ env}^T_0 \text{ dis}^T_2 \text{ env}^T_1 \text{ dis}^T_2 \text{ env}^T_2 \text{ dis}^T_3
\]

Intuitively, the new interleaved run is obtained by triplicating each \( \text{env}^T \) timestamp into three adjacent timestamps, \( \text{env}^T_a, \text{env}^T_b, \text{env}^T_c \). The \( \text{env}^T_a \) timestamps belong to the lifted run \( M_1(\rho) \), the \( \text{env}^T_b \) timestamp belongs to \( M_2(\rho) \) and the \( \text{env}^T_c \) timestamp belongs to \( \rho_1 \). The \( a, b, c \) copies are ordered as \( b < c < a \) giving us the following timestamp sequence from the one above.

\[
\text{init } \text{dis}^T_0 \text{ dis}^T_1 \text{ env}^T_0 \text{ env}^T_c \text{ env}^T_a \text{ dis}^T_2 \text{ env}^T_1 \text{ env}^T_b \text{ env}^T_c \text{ env}^T_a \text{ env}^T_b \text{ env}^T_c \text{ env}^T_a \text{ dis}^T_3
\]

We can formalize \( M_1 \) and \( M_2 \) by counting the number of \( \text{dis}^T \) timestamps smaller than the \( \text{env}^T \) timestamp, but for ease of presentation, we will keep this implicit. The total shift can be done for instance, using the function which maps a time stamp \( p \in \mathbb{N} \) corresponding to a \( \text{env} \) thread to the (number of \( \text{dis} \) threads appearing before \( p \)) + 3(number of \( \text{env} \) threads appearing before \( p \)) + 3. For instance, the \( \text{env}^T_0 \) at timestamp 3 moves to the \( \text{env}^T_0 \) time stamp 5, while the \( \text{dis}^T_3 \) moves to the \( \text{dis}^T_3 \) time stamp 3 + 3(3)+1=13.

\( M_1 \) maps the timestamp \( \text{env}^T_0 \) to the timestamp \( \text{env}^T_1 \) timestamp. Similarly, \( M_2 \) maps the \( \text{env}^T_1 \) timestamp to the timestamp \( \text{env}^T_2 = \text{env}^T_1 - 2 \). Finally, we have \( \text{env}^T_2 = \text{env}^T_1 - 1 \).

We call these adjacent timestamps ‘triplets’. Additionally, \( M_1 \) and \( M_2 \) map the \( \text{dis}^T \) timestamp to the corresponding \( \text{dis}^T \) timestamp in the expanded run.

We first note that \( M_1 \) satisfies the premise of the timestamp lifting lemma, that for \((\text{CAS-local})\) operations, consecutive load/store timestamps for CAS remain consecutive. This follows since only \( \text{dis} \) can perform \((\text{CAS-local})\) and under \( M_1 \), consecution is maintained both for \((\text{dis}^{T-1}, \text{dis}^T)\) timestamps as well as \((\text{env}^T_a, \text{dis}^T)\) as depicted in the
following timestamp sequence. Thus, by the timestamp lifting lemma, \( M_1(\rho) \) is a valid run under RA.

\[
\text{init} \ disT^0 \ disT^1 \ envT_a^0 \ envT_a^1 \ envT_b^0 \ envT_b^1 \ envT_c^0 \ envT_c^1 \ envT_d^0 \ envT_d^1 \ disT^3
\]

2. **The first superposition gives a valid run.** We now claim that the run \( M_1(\rho) \triangleright M_2(\rho \downarrow_{\text{env}}) \) is a valid run under RA. For a \( \text{env} \) thread \( t \) in \( \rho \) we denote by \( \text{copyB}(\rho) \) as its ‘copy’ (TID distinguished apart) in \( M_2(\rho \downarrow_{\text{env}}) \) (B since it occupies the b timestamps). We will show that \( \text{copyB}(\rho) \) copies the transitions that \( t \) took. We use the following invariant relating the view \( \text{vw}_1 \) of thread \( t \) in \( \rho \) with the view \( \text{vw}_2 \) of \( \text{copyB}(\rho) \) for showing this. Let \( TS(t) \) denote the set of timestamps used by thread \( t \) in a run \( \rho \).

For every shared variable \( x \), if \( \text{vw}_1(x) \in TS(\text{env}) \), then \( \text{vw}_2(x) = \text{vw}_1(x) - 2 \), else if \( \text{vw}_1(x) \in TS(\text{dis}) \) then \( \text{vw}_2(x) = \text{vw}_1(x) \)

Now we can reason by induction on the length of the run that whenever \( t \) takes a transition in \( \rho \), \( \text{copyB}(\rho) \) can replicate it but with the view as given by the above invariant. More precisely, whenever a \( \text{env} \) thread \( t \) makes a store with timestamp \( \text{env}T \), \( \text{copyB}(\rho) \) will make a store with timestamp \( \text{env}T - 2 \). Similarly, when a \( \text{env} \) thread \( t \) makes a load,

a. if the load is from a message by a \( \text{dis} \) thread, \( \text{copyB}(\rho) \) also loads from the same message

b. if the load is from a message by some \( \text{env} \) thread \( t' \) in \( \rho \), \( \text{copyB}(\rho) \) loads from \( \text{copyB}(\rho') \)

It is easy to check that the view invariant is maintained through this simulation. Crucially we have \( \text{env}T_a^i < \text{dis}T_j \iff \text{env}T_b^i < \text{dis}T_j \). Thus \( t \) and \( \text{copyB}(\rho) \) can always read the same set of \( \text{dis} \) messages. Thus we have that \( M_1(\rho) \triangleright M_2(\rho \downarrow_{\text{env}}) \) is valid under RA. Now we focus on message generation by \( \rho_1 \). Intuitively, \( \rho_1 \) will also be a copy of \( \rho \) but will occupy the \( \text{env}T_e \) timestamps.

3. **Generating a copy of the message.** Now we will describe how we can use \( \rho_1 \) to generate the message \( (x, d, \text{vw}) \). Let \( \rho_p \) be the prefix of \( \rho \) just (one transition) before the message \( (x, d, \text{vw}) \) is generated. We generate the run \( \rho' \) by copying the \( \rho \downarrow_{\text{env}} \) using the c-timestamps. The run obtained is \( M_1(\rho) \triangleright M_2(\rho \downarrow_{\text{env}}) \triangleright \rho' \). Using similar reasoning as earlier, we can show that this is a valid run under the RA semantics.

Now let \( \text{env} \) thread \( t \) be the thread which generates the message \( (x, d, \text{vw}) \) in \( \rho \). Then there is a copy of \( t \), thread \( \text{copyC}(t) \) in \( \rho' \), that is now in a control state enabling it to generate a message on variable \( x \) with value \( d \) (since the transitions have been replicated exactly across \( \text{env} \) and \( \text{copyC}(\rho) \)). Now we need to reason about the view of the message generated by \( \text{copyC}(t) \). If the view of \( t \) is \( \text{vw}_a \) and that of \( \text{copyC}(t) \) is \( \text{vw}_c \) we have the following, which again follows from the invariant mentioned above.

For each variable \( x' \), if \( \text{vw}_a (x') \in TS(\text{env}) \), then \( \text{vw}_c (x') = \text{vw}_a (x') - 1 \), else if \( \text{vw}_a (x') \in TS(\text{dis}) \) then \( \text{vw}_c (x') = \text{vw}_a (x') \)

Observe how this satisfies the condition (3) in the lemma immediately since in both cases above, we have \( \text{vw}_c (x') \leq \text{vw}_a (x') \). Now the thread \( \text{copyC}(t) \) will choose the timestamp for variable \( x \), \( \text{vw}'(x) \). Assume \( t^* \in \mathbb{N} \) has been given. We have two cases, (i) \( t^* \leq \text{vw}(x) \) and (ii) \( t^* > \text{vw}(x) \).

(i) In this case there is nothing to prove as the original message is lifted to \( (x, d, \text{vw}') \) where \( \text{vw}'(x) = \mu_2^1(t^*) \) which satisfies both conditions (1) and (2).

(ii) We choose \( \text{vw}'(x) = \mu_2^1(t^*) + 1 \), which satisfies (2). Note that this timestamp is higher than \( \text{vw}_c (x) \) since \( \mu_2^2(t^*) \geq \mu_2^1(\text{vw}(x)) = \text{vw}_a (x) > \text{vw}_c (x) \). We have \( \text{vw}'(x) = \mu_2^1(t^*) + 1 = \mu_2^2(t^*) \).
\[ \mu_i^*(t^*) - 1 \] due to the construction of \( \mathcal{M}_1, \mathcal{M}_2, \rho_1 \). Additionally, \( ts_i^* \geq t^* \implies \mu_i^*(ts_i^*) \geq \mu_i^*(t^*) > vw'(x) \) satisfying condition (1). In this case \( \rho_1 \) is defined as \( \rho' \) extended by the store transition generating the message. Note that since it is a \( c \)-type message, the timestamp is available.

Thus in both cases, we have a message \((x, d, vw')\) with \( vw' \) satisfying the required conditions. This proves the theorem.

\[ \Box \]

To sum up, we interpret the infinite supply as this: \( \mathcal{M}_1(\rho) \) is the lifted run with holes. \( \mathcal{M}_2(\rho \downarrow_{env}) \) is the \( \text{copy}(\text{env}) \) run and \( \rho_1 \) is obtained by running another copy that generates the new message. We note that run triplication is not strictly necessary for message duplication, but makes the proof easier. We note, points (1) and (3) above refer to relative ordering between \( \text{env} \) and \( \text{dis} \) timestamps and (2) refers to the new message with an arbitrarily high timestamp.

### 4.2 Abstracting the Timestamps

We introduce the timestamp abstraction, which is a building block for the simplified semantics. Let us call a message \( msg \) an \( \text{env} \) (\( \text{dis} \)) message if it is generated by a \( \text{env} \) (\( \text{dis} \)) thread. With the intuition that \( \text{env} \) messages can be replicated with arbitrarily high timestamps, while \( \text{dis} \) or initial messages cannot be, we distinguish the write timestamps of the two types of messages.

**Timestamp Abstraction.** If a \( \text{env} \) thread has read a message \((x, d, vw)\) from a \( \text{dis} \) thread with a timestamp \( ts = vw(x) \) and has generated a message \( msg \) on \( x \), then copies of \( msg \) are available with arbitrarily high timestamps at least as high as \( ts \). To capture this in our abstraction, we assign the \( \text{env} \) message \( msg \), a timestamp \( ts^+ \) that is by definition, larger than \( ts \).

We define the set of timestamps in the simplified semantics as \( \mathbb{N} \cup \mathbb{N}^+ \), where \( \mathbb{N}^+ \) contains for each \( ts \in \mathbb{N} \), a timestamp \( ts^+ \). The timestamps are equipped with the order \( \preceq \) in which \( ts^+ \) is greater than \( ts \) and smaller than \( ts + 1 \):

\[
0 \prec 0^+ \prec 1 \prec 1^+ \prec \ldots
\]

Timestamps of form \( ts \in \mathbb{N} \) are used for the stores of \( \text{dis} \) threads while those of form \( ts^+ \) are used for stores of \( \text{env} \) threads. We allow multiple stores with the same timestamp of form \( ts^+ \), while allowing at most one store for timestamps of form \( ts \). This abstracts timestamps of multiple \( \text{env} \) messages between two \( \text{dis} \) messages by a single \( ts^+ \) timestamp. Initial messages have timestamp 0 as usual.

We utilize this timestamp abstraction by defining a simplified semantics; note that this simplification is not per se a simpler formulation but rather is simple in the sense that it will pave the way for efficient verification procedures (as detailed in Section \( \Box \) Section \( \Box \)). We then show that a run \( \rho \) in the classical RA semantics has an equivalent run in the simplified semantics where the timestamps are transformed according to some timestamp transformation \( \mathcal{M} \) as defined above. We show that reachability across the two semantics is preserved since both order and consecution between timestamps is maintained.

**RA semantics, simplified.** As in the classical RA semantics, the transition rules of the simplified semantics will require us to increase timestamps (upon writing messages). We define the function \( \text{raise}(\cdot) \) on \( \mathbb{N} \cup \mathbb{N}^+ \) by

\[
\text{raise}(ts) = \text{raise}(ts^+) = ts^+, ts \in \mathbb{N}.
\]
The definition of the simplified semantics replaces the domain $\text{Time}$ by $\mathbb{P} = \mathbb{N} \cup \mathbb{N}^+$. We use the term *abstract* to refer to the resulting views, messages, memory, local configurations, and configurations and use a superscript $\text{de}$ (shortened $\text{dis}$/env) to indicate that an element is abstract. So an abstract view is a function, $\text{vw}^{\text{de}}$ that maps shared variables to $\mathbb{P}$. We now specify the transitions in the abstract semantics. Owing to their different nature (one is replicatable, the other is not) the $\text{dis}$ and $\text{env}$ threads will have different transition rules in the simplified semantics.

For storing a value, the $\text{env}$ threads use a rule $(\text{ST-LOCAL}^{\text{env}})$ that coincides with rule $(\text{ST-LOCAL})$ from the RA semantics (Figure 1) except that it replaces relation $<_x$ by $<_x^{\text{env}}$ defined as follows:

$$\text{vw}_1 <_x^{\text{env}} \text{vw}_2 \iff \begin{cases} \text{raise(}\text{vw}_1(x)\text{)} \leq \text{vw}_2(x) \in \mathbb{N}^+ \\ \text{vw}_1(y) = \text{vw}_2(y) \text{ for } y \neq x. \end{cases}$$

Additionally, for stores of $\text{env}$ threads, we no longer require the timestamp of the message to be unused. So we disregard the $\text{msg}\#m$ check in the global $(\text{ST-GLOBAL})$ rule (note crucially this is for $\text{env}$ only). The $\text{dis}$ threads use $(\text{ST-LOCAL})$ from the RA semantics without modifications, and hence choose a timestamp in $\mathbb{N}$, not a raised value.

For load instructions, we distinguish between messages generated by $\text{dis}$ and $\text{env}$ threads. This is a natural consequence of the different nature of timestamps, $\text{ts}$ for $\text{dis}$ and $\text{ts}^+$ for $\text{env}$ messages. For loading a $\text{dis}$ message, we use rule $(\text{LD-LOCAL})$ (Figure 1) from the RA semantics without changes.

For loading from $\text{env}$ threads, we introduce a new rule $(\text{LD-LOCAL}^{\text{env}})$. It is defined by replacing $\sqcup$ in $(\text{LD-LOCAL})$ by $\sqcup^{\text{env}}$. We drop the check on the order of timestamps (overwrite it by true); a $\text{env}$ message may always be read, independent of the reading thread’s view. The join is dependent on the variable being read from, $x$. To define $\text{vw}_1 \sqcup^{\text{env}} \text{vw}_2$, let $\text{vw}_1$ be the view of the thread loading the message and $\text{vw}_2$ be the view in the message.

$$\text{vw}_1 \sqcup^{\text{env}} \text{vw}_2 = (\text{vw}_1[x \mapsto \text{raise(}\text{vw}_1(x)\text{)})] \sqcup \text{vw}_2$$

Thus, if $\text{vw}_1(x) = 4$ and $\text{vw}_2(x) = 2^+$, then $(\text{vw}_1 \sqcup^{\text{env}} \text{vw}_2)(x) = 4^+$. The update to $\text{raise(}\text{vw}_1(x)\text{)}$ ensures that if it the timestamp on $x$ was $\text{ts}$, it is at least $\text{ts}^+$, and hence it cannot read a (dis) message with timestamp $\text{ts}$ again. We note that the above join operation is not commutative.

Now we consider the atomic operation - $(\text{CAS-LOCAL})$ - which can only be performed by $\text{dis}$. We have two cases depending on whether $(\text{CAS-LOCAL})$ loads from a $\text{dis}$ or $\text{env}$ message. If it is the latter, then the transition is identical to $((\text{LD-LOCAL}^{\text{env}}); (\text{ST-LOCAL}))$ with the additional condition that the load and store timestamps must be $\text{ts}^+$ and $\text{ts} + 1$ for some $\text{ts}$.

If it is the former (load from $\text{dis}$) then the load and store timestamps must be $\text{ts}$ and $\text{ts} + 1$. Consequently, there cannot be any messages with timestamp $\text{ts}^+$. Conversely, if there is (atleast one) message with timestamp $\text{ts}^+$, then the $(\text{CAS-LOCAL})$ operation with load and store timestamps $\text{ts}$ and $\text{ts} + 1$ is forbidden. We keep track of such ‘blocked’ intervals ($\text{ts}, \text{ts} + 1$) by adding a set $\mathcal{B}$ to the global state in the simplified semantics. The global and local transition relations of the full simplified semantics are in Figure 6, 7.

We formally proof equivalence w.r.t. reachability of the simplified semantics with the original RA semantics. But before that, we give an example to illustrate timestamp abstraction in the simplified semantics.
Variables \( x \) and \( y \) have been initialized to 0

\[
\begin{align*}
\lambda_1 : & \quad r_1 := y \\
\lambda_2 : & \quad \text{if}(r_1 == 1) : \\
\lambda_3 : & \quad x := 1 \oplus \cdots \oplus x := l
\end{align*}
\]

\[
\lambda_1' : \quad y := 1 \\
\lambda_2' : \quad \text{for } i \in 1..z : \\
\lambda_3' : \quad r'_1 := x \\
\lambda_4' : \quad \text{assume } r'_1 = (i \mod l) + 1
\]

**Figure 4** Above is a (non-parameterized) producer-consumer program, and below is a sample execution snippet with threads \( t_1 \) and \( t_2 \) playing the roles of producer and consumer respectively.

**Simplified Semantics, on an Example.** In Figure 5 we give an example of a computation under the simplified semantics by parameterizing the program from Figure 4. The parameterized program has a single distinguished \( \text{dis}_1 \) thread which runs the program \( \text{consumer} \), and arbitrarily many \( \text{env} \) threads which run \( \text{producer} \). We consider a computation in which \( \text{dis}_1 \), and \( l \) (out of the unboundedly many) \( \text{env} \) threads participate. We label different instances of the \( \text{env} \) threads (and their instruction labels) by superscripts from \( \{1, \ldots, l\} \) (eg., \( \lambda_1^1, \ldots \lambda_1^l \) for \( \lambda_1 \)).

The \( \text{consumer} \) generates write timestamps of the form \( ts(i) \) (1 in example), while \( \text{producer} \) threads have write timestamps of the form \( ts^+ \). While the timestamp 1 is now occupied, there can be several writes with timestamps of the form \( ts^+ \), (in particular some \( ts^+ \) may be equal). Additionally, when reading from these \( \text{producer} \) generated messages, \( \text{consumer} \) does not perform any timestamp checks, rather simply updates its view by taking joins. Hence we point out that the load with value 2 during the second loop iteration \( (i=2) \), is feasible even if \( ts^+_2 < ts^+_1 \); unlike the classical RA semantics. In this example, the \( \text{dis} \) thread, after looping around \( l \) times and reading from \( \text{env} \) messages, has the view on \( x \) as \( \max \{ts^+_i\} \). Due to the lack of timestamp comparisons, \( \text{consumer} \) can perform the loop arbitrarily many times \( (z > l \text{ times}) \), moreover, the number of \( \text{env} \) threads needed is independent of \( z \). We see that this relieves the burden of timestamp comparisons, for \( \text{env} \) messages.

The simplified semantics exactly captures reachability of the original semantics. Define \( \alpha_{de} \) to be a function which drops all views from messages and local configurations, and define \( =_{de} \) as equality of the local configurations modulo views.

**Theorem 5 (Soundness and Completeness).** If a configuration \( cf \) is reachable under RA, then there is an abstract configuration \( cf^{de} \) reachable in the simplified semantics so that \( cf^{de} =_{de} \alpha_{de}(cf) \). Conversely, if a configuration \( cf^{de} \) is reachable in the simplified semantics, then there is a configuration \( cf \) reachable under RA such that \( \alpha_{de}(cf) =_{de} cf^{de} \).

**Proof.** At the outset, we note that the only component of the configuration that differs between the classical and simplified semantics is that of the timestamps and hence the view map, \( vw \) in concrete and \( vw^{de} \) in the abstract configuration. We now give a relation between these timestamps. With this relation being clear, the formal equivalence between the semantics can be shown by considering a case analysis of the transitions that the threads can take. Once again for quick intuition we take the example of timestamps on a single
Execution under the simplified semantics. producer transitions and messages in red, consumer transitions and messages in blue. The execution begins with the consumer thread generating a message on y with value 1 and timestamp 1 leading to the memory $m_{\lambda_1^1}$. The producer threads executing $\lambda_1^1$ read from this message and reach states $\lambda_1^1, \lambda_1^2$. They generate messages on x with values $\{1, \ldots, l\}$ shown in memory $m_{\lambda_3}$. These are then read by the consumer as it loops around $\lambda_3^4, \lambda_3^5$ for different iterates $i$ ($i=1, i=2, i>2$) as shown along the transition edge.

shared variable x as follows.

\[
\begin{array}{cccccccc}
\text{init} & \text{disT}^0 & \text{disT}^1 & \text{envT}^0 & \text{disT}^2 & \text{envT}^1 & \text{disT}^3 \\
0 & 1 & 2 & 3 & 4 & 5 & 6 & 7
\end{array}
\]

This sequence of timestamps corresponds to the following sequence in the abstract semantics.

\[
\begin{array}{cccccccc}
\text{concrete} & \text{disT}^0 & \text{disT}^1 & \text{envT}^0 & \text{disT}^2 & \text{envT}^1 & \text{disT}^3 \\
0 & 1 & 2 & 3 & 4 & 5 & 6 & 7
\end{array}
\]

In this fashion the $\text{ts}^+$ are abstracted env timestamps between any two dis timestamps. We define the abstraction (similarly concretization) function as the function that transforms all timestamps in the run as shown above. With the above timestamp abstraction/concretization in mind we show that abstract and concrete configurations are equivalent in terms of reachability.

We prove this by induction on the length of a run. We show that a concrete (similarly abstract) configuration is reachable if and only if it has some abstraction (similarly concretization) that is reachable.

**Base Case.** In the base case equivalence is maintained as the initial concrete configuration is equivalent to its simplified configuration where all timestamps are 0. Recall that all timestamp transformations maintain 0 as a fixpoint. Hence the initial thread-local states and memory are equivalent for the concrete and abstract semantics.
Figure 6 Simplified semantics. Global transition relation. B is a set of blocked time stamps. For an env thread making a store operation, the time stamp $ts^+ \in \mathbb{N}^+$ can be chosen only when $ts$ has not been blocked ($ts \notin B$). $ts^+$ is added to $B$ whenever a env thread makes a store operation adding a message $(x, d, ts^+)$. Likewise, when a dis makes a CAS operation on loading from a message $(x, d, vw^d)$ with $vw(x) = ts^+$, then it must be checked that $ts^+ \notin B$, ensuring that there are no time stamps between $ts$ and $ts + 1$. $ts \in \mathbb{N}$ is added to $B$ when a dis thread makes a CAS, loading from a message $(x, d, vw)$ with $vw(x) = ts \in \mathbb{N}$.

Inductive Case - Concrete to Abstract For the inductive case, assume that we have the result after $n \in \mathbb{N}$ steps in a computation. Now we induct by considering cases over types of the $n+1$ th instruction in the computation.

- Silent: Silent (thread-local) instructions are handled trivially. They only change the thread local state identically for the concrete and abstract configurations.
- Load: A load transition can be either from a dis or a env. For both the cases, we note that the timestamp abstraction maintains (including equality) the relative order of timestamps. Hence whenever a concrete message is readable, so is the corresponding abstract message.
- Store: This follows since the corresponding thread in the abstract configuration can simulate the store using the corresponding timestamp $(ts^+ \in \mathbb{N}^+ \text{ in case of a env store, and } ts \in \mathbb{N} \text{ in case of a dis store})$. Note once again that, the abstraction preserves order on the timestamps and consequently, a store is allowed in the abstract semantics if it was allowed in the concrete computation.
- CAS: In this case, we note that the set $B$ keeps track of which timestamps are allowed for CAS operations. If the CAS operation read from a env message, the semantics follows from $(LD-LOCAL, env)$ $(ST-LOCAL)$. However, if the CAS load is performed using the store of a dis, then it implies that there are no env timestamps between the load,store timestamps $(ts, ts + 1)$ of the CAS (similar to $dist^0$ and $dist^1$ in the figure above). Consequently, we see that the set $B$ in the abstract semantics does not contain the timestamp $ts^+$ $(ts^+ \text{ is added to } B \text{ the moment a env makes a store with the timestamp } ts^+ \text{ to disallow a CAS with load})$. 

\[
\begin{align*}
(LD-LOCAL) & \quad \frac{\text{lcfm}(t) = \text{lcf} \quad \text{lcf} \quad \text{ldmsg} \quad \text{lcf'}}{\text{msg} \in m} \quad (m, \text{lcfm}, B) \quad (\text{tmsg}) \quad (m, \text{lcfm}[t \mapsto \text{lcf'}], B) \\
(UNLABELLED) & \quad \frac{\text{lcfm}(t) = \text{lcf} \quad \text{lcf} \quad \text{lcf'}}{\text{m}, \text{lcfm}, B} \quad (\text{tmsg}) \quad (m, \text{lcfm}[t \mapsto \text{lcf'}], B) \\
(ST-GLOBAL) & \quad \frac{t \in \text{dis} \quad \text{lcfm}(t) = \text{lcf} \quad \text{stmsg} \quad \text{lcf'}}{\text{msg} \in m} \quad (\text{msg}) \quad (m, \text{lcfm}, B) \quad (\text{tmsg}) \quad (m \cup \{\text{msg}\}, \text{lcfm}[t \mapsto \text{lcf'}], B) \\
(ST-GLOBAL) & \quad \frac{t \in \text{env} \quad \text{lcfm}(t) = \text{lcf} \quad \text{stmsg} \quad \text{lcf'}}{\text{msg} \in m} \quad (\text{msg}) \quad (m, \text{lcfm}, B) \quad (\text{tmsg}) \quad (m \cup \{\text{msg}\}, \text{lcfm}[t \mapsto \text{lcf'}], B \cup \{ts^+\}) \\
(CAS-GLOBAL) & \quad \frac{\text{lcfm}(t) = \text{lcf} \quad \text{casmsg} \quad \text{msgur} \quad \text{lcf'}}{\text{msg} \in m \quad \text{msgur} \in m} \quad (\text{msg}) \quad (m, \text{lcfm}, B) \quad (\text{tmsgur}) \quad (m \cup \{\text{msgur}\}, \text{lcfm}[t \mapsto \text{lcf'}], B \cup \{\text{ts} + 1\}) \\
\end{align*}
\]
Figure 7 Simplified semantics. Thread-local transition relation. Margin annotations provide description. The store rules refer to the thread type (dis/env) executing the instruction; the load rules refer to the thread type which generated the message that is being loaded (similarly for the load part of CAS operations which can only be executed by dis threads). In Rule (ST-LOCAL\env), we use $w_1^d <^\env w_2^d$ to mean $\text{raise}(w_1^d(x)) \leq w_2^d(x) \in \mathbb{N}^+$ and $w_1^d(y) = w_2^d(y)$ for all variables $y \neq x$. In Rule (LD-LOCAL\env), $w_1^d \sqcup^\env w_2^d$ is defined as $w_1^d[x \mapsto \text{raise}(w_1^d(x))] \sqcup w_2^d$. The join $\sqcup$ always means an element wise max over the relevant domain.

store timestamps $ts$ and $ts + 1$). Thus the equivalent CAS operation is also allowed under the abstract semantics.

**Inductive Case - Concrete to Abstract**

- **Silent:** Silent instructions are handled trivially they only change the thread local state identically for the concrete and abstract configurations.

- **Load:** We consider two cases depending on whether the load happens from a dis thread or an env thread.

  - In the case where we load from a dis message, the semantics are equivalent between the abstract and concrete transitions, since we compare the timestamps $ts^+ < ts + 1$ and $ts < ts + 1$ (see the rule (LD-LOCAL) in Figure 7). Given that the concretization function (like the abstraction) maintains relative order between dis and env timestamps, the load is also feasible in the concrete semantics.

  - In the second case, the load is from an env. By inductive hypothesis, we have the concrete computation till the load transition. In particular, the message $(x, d, wv)$ we wish to load has already been generated in the concrete computation. To this concrete computation $\rho$ obtained by inductive hypothesis, we invoke the infinite supply lemma with $t^*$ as the reading thread’s local view on $x$ to generate the computation $M_1(\rho) \triangleright M_2(\rho_{\env}) \triangleright \rho_1$ with the fresh message $(x, d, wv')$. By point (2) in the lemma the message is loadable, $wv'(x) \geq \rho_2^t(t^*)$. Note how we apply the timestamp lifting function to $t^*$ since the reading
thread’s new concrete timestamp has changed. Additionally by points (1) and (3) the relative order of timestamps in $vw'$ in variables other than $x$ remain the same w.r.t the $\text{dis}$ thread messages. This implies that after reading the message, the view of the reading thread will only increase on $x$. Hence for all other variables it will remain the same thus maintaining equivalence between the timestamps in the concrete and abstract run.

- **Store:** The store transition for $\text{dis}$ is identical to its concrete counterpart. For a $\text{env}$ thread, we note that we generate copies of the abstract $\text{ts}^+$ timestamp to get a sequence of concrete timestamps. Here we can generate an arbitrary number of copies and hence the thread, will always find a vacant timestamp for its store.

- **CAS:** When a $\text{dis}$ thread makes a CAS, it can either read from a $\text{env}$ or from the store of a $\text{dis}$ thread. In the latter case let the timestamps of the load/store in the CAS be $\text{ts}, \text{ts} + 1$. Then in the abstract semantics we require that $\text{ts}^+ \notin B$. This implies that in the concrete semantics too, there are no $\text{env}$ timestamps between the load/store timestamps and hence CAS is possible in the concrete semantics too. In the former case we again use the infinite supply lemma as we did in the case of loads, to generate a loadable $\text{env}$ message.

5 Safety Verification with Loop-Free Threads

This section discusses the safety verification problem for the class $\text{env}(\text{nocas}) || \text{dis}_1(\text{acyc}) || \cdots || \text{dis}_n(\text{acyc})$ consisting of a set of $n$ distinguished $\text{dis}$ threads executing a loop-free program in the presence of an unbounded number of $\text{env}$ threads. We show that the safety verification problem for this class of systems can be decided in $\text{PSPACE}$ by leveraging the simplified semantics from Section 4. We will assume that the domain $\text{Dom}$ is finite. Parallely, we demonstrate the ability to improve automatic verification techniques by showing how to encode the safety verification problem (of whether all assertions hold) into Datalog programs. The encoding is interesting for two reasons: (1) it yields a complexity upper bound that, given [1], came as a surprise; (2) it provides practical verification opportunities, considering that Datalog-based Horn-clause solvers are state-of-the-art in program verification [17,18].

Theorem 6. The safety verification problem for $\text{env}(\text{nocas}) || \text{dis}_1(\text{acyc}) || \cdots || \text{dis}_n(\text{acyc})$, $n \in \mathbb{N}$ is non-deterministic polynomial-time relative to the query evaluation problem in linear Datalog (NP$^{\text{PSPACE}}$), and hence is in $\text{PSPACE}$.

We note that the theorem mentions non-deterministic polynomial time relative to the linear Datalog oracle. We provide a non-deterministic poly-time procedure $\text{Algo}$, that, given a verification instance converts it to a Datalog problem $P$ s.t. (1) for a ‘yes’ verification instance, atleast one execution of $\text{Algo}$ results in $P$ having successful query evaluation and (2) for a ‘no’ verification instance, no execution of $\text{Algo}$ leads to the resulting $P$ to have successful query evaluation.

Linear Datalog is a syntactically restricted variant of Datalog for which query evaluation is easy to solve (PSPACE) at the cost of being inconvenient as an encoding target. Given that we show a $\text{PSPACE}$ upper bound on the parameterized safety verification for the class $\text{env}(\text{nocas}) || \text{dis}_1(\text{acyc}) || \cdots || \text{dis}_n(\text{acyc})$, in principle, we could have directly encoded the parameterized safety verification problem instance as a linear Datalog program. For convenience of encoding, we do not directly reduce safety verification into query evaluation in linear Datalog, but use an intermediate notion of Cache Datalog. To make the ideas behind our reduction clear, we proceed in three steps.
1. We introduce Cache Datalog, which is Datalog with an additional parameter, called the Cache, that turns out decisive in controlling complexity of encodings in the following sense: every Cache Datalog program can be turned into a linear Datalog program at a cost that is linear in the size of the program plus that of the Cache (Lemma 7).

2. We then show that Algo generates Cache Datalog problems that satisfy the description from the previous paragraph (Lemma 8), and

3. We then argue that for all Cache Datalog instances generated by Algo, a Cache of polynomial size is sufficient for query evaluation (Lemma 9).

This shows Theorem 6.

**Linearizing Datalog** A Datalog program $\text{Prog}$ consists of a predicate set $\text{Preds}$, a data domain $\text{Data}$, and a set $\text{Rules}$ of rules (also called clauses). Each predicate comes with a fixed arity $> 0$. A predicate $P$ of arity $j$ is a mapping from $\text{Data}^j$ to $\{\text{true, false}\}$. An atom consists of a predicate $P(t_1, \ldots, t_j)$ and a list $t_1, \ldots, t_j$ of arguments, where each $t_i$ is a term. A term is either a variable or a constant; a term is a ground term if it is a constant, and an atom is a ground atom if all its terms are constants. A positive literal is a positive atom $P(t_1, \ldots, t_j)$ and a negative literal is a negative atom $\neg P(t_1, \ldots, t_j)$, and a ground literal is a ground atom. A rule has the form

$$\text{head} : - \text{body}_1, \ldots, \text{body}_t$$

where $\text{head}$ and $\text{body}_i$ are positive literals. A rule with one literal in the body is a linear rule, one without a body is called a fact. A linear Datalog program is one where all rules are linear or are facts. An instantiation of a rule is the result of replacing each occurrence of a variable in the rule by a constant. For all instantiations of the rule, if all ground atoms constituting the body are true then the ground atom in the head can be inferred to be true. All instantiations of facts are trivially true. We write $\text{Prog} \vdash g$ to denote that the ground atom $g$ can be inferred from program $\text{Prog}$.

**Query Evaluation Problem.** The query evaluation problem for Datalog is, given a query instance $(\text{Prog}, g)$ consisting of a Datalog program $\text{Prog}$ and a ground atom $g$, to determine whether $\text{Prog} \vdash g$. When studying the combined complexity, both $\text{Prog}$ and $g$ are given as input [65]. It is known [38] that combined complexity of query evaluation for linear Datalog is in PSPACE, while allowing non linear rules raises the complexity to $\text{NEXPTIME}$ ([65] and [44]). Motivated by verification, there has been interest in linearizing Datalog [45].

**Adding Cache to Datalog: Cache Datalog.** We introduce to Datalog the concept of a Cache. A Cache is a set of ground atoms that is used to control the inference process. The resulting program is called a Cache Datalog program. In the presence of a Cache, the semantics of Datalog is adapted by the following two rules.

**Add:** For an instantiated rule, the ground atom in the head can be inferred and added to Cache only when all the ground atoms in the body are in Cache.

**Drop:** Atoms in Cache can be dropped non-deterministically.

The standard semantics of Datalog can be recovered by monotonically adding all inferred atoms (starting with facts) to the Cache and never dropping anything. To show the upper bound, we use a notion of inference that takes into account the size of the Cache and minimizes it. For a Cache Datalog program $\text{Prog}$ and $k \in \mathbb{N}$, we write $\text{Prog} \vdash_k g$ to mean that ground atom $g$ can be inferred from $\text{Prog}$ with a computation in which $|\text{Cache}| \leq k$, the number of atoms in Cache is always at most $k$. The Cache size measures the complexity of linearizing Cache Datalog as follows.
Lemma 7. Given a Cache Datalog program \( \text{Prog} \), a ground atom \( g \), and a bound \( k \), in time quadratic in \( |\text{Prog}| + |g| + k \) we can construct a linear Datalog program \( \text{Prog}' \) so that \( \text{Prog} \models_k g \iff \text{Prog}' \models g \).

Proof. To go from Cache Datalog to linear Datalog, the idea is to simulate the Cache using a new predicate \( \text{CachePred} \) of arity \( k \) in the constructed linear Datalog program \( \text{Prog}' \). We know that a Cache of size \( k \) suffices in the Cache Datalog program, so any rule

\[
\text{head} : - \text{body}_1, \ldots, \text{body}_p
\]

in the Cache Datalog is s.t. \( p < k \).

1. Simulating Cache Intuitively, the predicate \( \text{CachePred}(t_1, t_2, \ldots, t_k) \) represents that the terms \( t_i \) are members of the Cache. We can simulate the set Cache by reshuffling terms using rules that swap the \( i \)th and \( j \)th elements with rules of the form,

\[
\text{CachePred}(t_1, \ldots, t_j, \ldots, t_i, \ldots, t_k) : - \text{CachePred}(t_1, \ldots, t_i, \ldots, t_j, \ldots, t_k)
\]

There are quadratically many such rules.

2. Rules Consider a rule \( R \) with a body of size \( p \) in Cache Datalog as follows.

\[
\text{head} : - \text{body}_1, \ldots, \text{body}_p
\]

We convert this into a rule which matches the first \( p \) terms of \( \text{CachePred} \) with the elements of the body. If there is such a matching, the term \( \text{head} \) can be inferred and added into Cache. This is simulated by replacing some term amongst \( t_i \) with the term in the \( \text{head} \) while keeping other terms the same.

\[
\text{CachePred}(t_1, \ldots, t_i = \text{head}, \ldots, t_k) : - \text{CachePred}(t_1 = \text{body}_1, \ldots, t_p = \text{body}_p, t_{p+1}, \ldots, t_k)
\]

There are \( k \) choices for the term to be replaced. Thus we have \( k \) new rules per rule in the original program.

3. Final Inference Finally, since we know that each element of Cache is true, we add the inference rules,

\[
t_i : - \text{CachePred}(t_1, t_2, \ldots, t_p) \quad \text{for } 1 \leq i \leq p
\]

Now, \( g \) can be generated if \( g \) ever enters Cache, i.e. \( \text{CachePred}(t_1, t_2, \ldots, g, \ldots, t_p) \) for some other terms \( t_i \). Then we can use the above inference rule to infer \( g \).

This shows that we need at most quadratically many rules each with a single body, to give us a linear Datalog program.

5.1 Datalog Encoding

Theorem 5 tells us that safety verification under RA is equivalent to safety verification in the simplified semantics. Safety verification in the simplified semantics, in turn, can be reduced to the Message Generation (MG) problem.

Given a parametrized system \( c \) and a message \( \text{msg}^\# = (x^*, d^*, \_\,) \) called goal message, does there exist a reachable configuration \( \text{cf}^\# = (m^\#, \text{lcfm}^\#) \) such that \( \text{msg}^\# \in m^\# \) (for some \( \text{vw}^\# \))?

To see the connection between MG and safety verification, note that we can replace each \text{assert false} statement in the program by \( x^* := d^* \) for variable \( x^* \) and value \( d^* \) unused elsewhere. The system is unsafe if and only if a \text{goal message} \( \text{msg}^\# = (x^*, d^*, \text{vw}^\#) \) is generated for some \( \text{vw}^\# \).
While encoding into Datalog, we non-deterministically guess \( \text{vw}^{de} \). For this, we crucially show that there are only exponentially-many choices of \( \text{vw}^{de} \) which need to be enumerated. Henceforth we assume that the queried goal message \( \text{msg}^g \) can have arbitrary \( \text{vw}^{de} \). Given \( c, \text{msg}^g \), our non-deterministic poly-time procedure \( \text{Algo} \) satisfies the following, the proof of which is in Sections 5.1.2.

**Lemma 8.** Given a parametrized system \( c \) and a goal message \( \text{msg}^g \), Message Generation (MG) holds iff there is some execution of \( \text{Algo} \) that generates a query instance \( (\text{Prog}, g) \) such that \( \text{Prog} \vdash g \). The construction of \( \text{Prog} \) and \( g \) is in (non-deterministic) time polynomial in \(|c|\).

The procedure \( \text{Algo} \) generates one query instance \( (\text{Prog}, g) \) per execution. We postpone the full description of \( \text{Algo} \) and first give some intuition. Since the parameterized system consists of \( n \) loop-free \( \text{dis} \) threads, each can execute only linearly-many instructions in their size. The total number of instructions executed (and hence the total number of timestamps used) by the \( \text{dis} \) threads is polynomial in \(|c_{\text{dis}}|\), the combined size of \( \text{dis} \) programs (concretely the sum of sizes of individual \( c_{\text{dis}} \) programs). \( \text{Algo} \) guesses the \( \text{dis} \) threads part of the computation and generates a query instance \( (\text{Prog}, g) \).

\( \text{Prog} \) itself uses four main predicates. The environment message predicate \( \text{emp}(x, d, \text{vw}^{de}) \) represents the availability of a \( \text{env} \) message on variable \( x \) with value \( d \) and view \( \text{vw}^{de} \). The environment thread predicate \( \text{etp}(l, r, \text{vw}^{de}) \) encodes the \( \text{env} \) thread configuration, where \( l \) is the control-state, \( r \) is the register valuation and \( \text{vw}^{de} \) is the thread view. We also have similar message and thread predicates for \( \text{dis} \) threads. The distinguished message predicate \( \text{dmp}(x, d, \text{vw}^{de}) \) represents the availability of a \( \text{dis} \) message. Additionally, for each \( \text{dis} \) thread \( i \in [n] \), we have a distinguished thread predicate \( \text{dtp}[i](l, r, \text{vw}^{de}) \) that encodes the configurations of \( \text{dis}[i] \).

In the set of rules, we have the fact \( \text{dmp}(x, d_{\text{init}}, \text{vw}^{de}_{\text{init}}) \) for each \( x \in \text{Var} \) with \( d_{\text{init}} \) the initial value and \( \text{vw}^{de}_{\text{init}} \) the initial view. We also have (i) facts \( \text{etp}(l_{\text{init}}, r_{\text{init}}, \text{vw}^{de}_{\text{init}}) \) and \( \text{dtp}[i](l_{\text{init}}, r_{\text{init}}, \text{vw}^{de}_{\text{init}}) \) representing the initial states of both \( \text{env} \) and \( \text{dis} \) threads, (ii) rules corresponding to the \( \text{env} \) transitions and the guessed \( \text{dis} \) thread run fragments. Finally, the query atom \( g \), is a ground atom \( \in \{\text{emp}, \text{dmp}\} \) and captures the goal message \( \text{msg}^g \) being generated. The instances generated in the non-deterministic branches of \( \text{Algo} \) differ only due to the guessed \( \text{dis} \) run and the atom \( g \).

We now describe the full Datalog program, also proving Lemma 8.

### 5.1.1 Procedure \( \text{Algo} \) for query instance generation

We discuss the details of the procedure \( \text{Algo} \) which generates the query instance \( (\text{Prog}, g) \) non-deterministically. We use the following predicates in the constructed Datalog program.

- \( \text{emp}(\text{msg}) \): the message generation predicate for \( \text{env} \) threads, where \( \text{msg} \) is a message;
- \( \text{etp}(l, r, \text{vw}^{de}) \) : the thread generation predicate for \( \text{env} \) threads
- \( \text{dmp}(\text{msg}) \): the message generation predicate for \( \text{dis} \) threads, where \( \text{msg} \) is a message;
- \( \text{dtp}[i](l, r, \text{vw}^{de}) \) : the thread state predicate, one for each \( \text{dis} \) thread
- \( \text{avail}(x, ts^+) \) : the timestamp availability predicate, which indicates that a timestamp \( ts \) is not blocked by a CAS operation, per variable.

The Datalog program generated has two parts, one does not depend on the non-deterministic choices made by \( \text{Algo} \), while the other does. We describe the former part first, these rules for the Datalog Program are in Figure 8. The second set of rules, depending on the nondeterministic choice of \( \text{Algo} \) is in Figure 9.
The first set of rules in the Datalog program (Figure 8). The facts, in green, provide the ground terms for the init messages as well as initial state of the dis and env threads. The orange rules capture the thread local transitions of the env threads. We deviate a bit from the standard notation for programs here, and instead view them as labelled transition systems. It is easy to see that the two notions are equivalent. The initial state labels are $\lambda_{\text{init}}^{\text{env}}$ for the env threads and $\lambda_{\text{init}}^{\text{dis}}$ for the dis threads. For a pair of labels, we write $\lambda_1 \xrightarrow{e} \lambda_2$ to denote that $\lambda_2$ can be reached from $\lambda_1$ by executing $e$. In the Datalog program, we have a rule for each such transition in the program. The thread-local transitions are in orange. Loads are in violet (first corresponding to loads from env messages, the second for loading from dis messages). For loads, the rule requires a term with the message predicate (from which the thread is reading) in the body of the rule. Stores are in pink, the first rule corresponds to the new thread-local state after execution of the store. The second rule corresponds to the generation of a term for the new message (in the head). Though we use some higher order syntax for rules such as assume, $\cup$, and $<^e$ we note that these can be easily translated to pure Datalog with small overhead given the polynomial size of the domain and the constant arity of the predicates.

| rule | condition on program of env threads, $c_{\text{env}}$ |
|------|--------------------------------------------------|
| $\text{etp}(\lambda_2, rv, vw'^{\text{dis}}) := \text{etp}(\lambda_1, rv, vw'^{\text{dis}})$ | if $\lambda_1 \xrightarrow{\text{dis}} \lambda_2$ |
| $\text{etp}(\lambda_2, rv, vw'^{\text{dis}}) := \text{etp}(\lambda_1, rv, \exists e[(rv|e(\tau)) \neq 0, vw'^{\text{dis}}])$ | if $\lambda_1 \xrightarrow{\text{assum} \cup \tau} \lambda_2$ |
| $\text{etp}(\lambda_2, rv \leftarrow d, vw'^{\text{dis}} \cup d, vw'^{\text{dis}}) := \text{etp}(\lambda_1, rv, vw'^{\text{dis}})$ | if $\lambda_1 \xrightarrow{\text{dis}} \lambda_2$ |
| $\text{etp}(\lambda_2, rv \leftarrow d, vw'^{\text{dis}} \cup d, vw'^{\text{dis}}) := \text{etp}(\lambda_1, rv, \exists x, d, vw'^{\text{dis}}), wv'^{\text{dis}}, <, wv'^{\text{dis}})$ | if $\lambda_1 \xrightarrow{\text{dis}} \lambda_2$ |
| $\text{etp}(\lambda_2, rv, vw'^{\text{dis}}) := \text{etp}(\lambda_1, rv, vw'^{\text{dis}}), \text{avail}(x, vw'^{\text{dis}}(x))$ | if $\lambda_1 \xrightarrow{\text{dis}} \lambda_2$, with $wv'^{\text{dis}} <^e wv'^{\text{dis}}$ |
| $\text{emp}(x, rv(e), vw'^{\text{dis}}) := \text{etp}(\lambda_1, rv, vw'^{\text{dis}}), \text{avail}(x, vw'^{\text{dis}}(x))$ | if $\exists \lambda_2, \lambda_1 \xrightarrow{\text{dis}} \lambda_2$, with $wv'^{\text{dis}} <^e wv'^{\text{dis}}$ |

(a) The (fixed) set of rules in the Datalog program encoding the transition system of the env threads. Silent transitions (in orange); memory accesses: loads (in violet) and stores (in pink).

| fact | comment |
|------|---------|
| $\text{dmp}(x, d_{\text{init}}, vw_{\text{init}}^{\text{env}})$ | : $-$ for all variables $x$ |
| $\text{etp}(\lambda_{\text{init}}^{\text{env}}, rv_{\text{init}}, vw_{\text{init}}^{\text{env}})$ | : $-$ $\lambda_{\text{init}}^{\text{env}}$ is initial state of env threads |
| $\text{dtp}[i](\lambda_{\text{init}}^{\text{dis}}, rv_{\text{init}}, vw_{\text{init}}^{\text{dis}})$ | : $-$ $\lambda_{\text{init}}^{\text{dis}}$ is initial state of dis thread |

(b) First set of facts in the Datalog program; these do not depend on the non-deterministic guess made by $\mathcal{A}$ for the computation of dis threads. These facts encode the initial configurations of the threads and the initial messages.

**Figure 8** First set of rules for the Datalog Program. This fixed rule set is independent of non-determinism of $\mathcal{A}$.

These rules capture completely the env thread component of the run. As we had mentioned earlier, the component of the query instance that differs due to non-determinism of $\mathcal{A}$ is the dis part of the run. Essentially, $\mathcal{A}$ guesses in polynomial time the executions of all the dis threads. This is possible since they are loop-free and hence execution lengths are linear in the size of their specifications. We now describe this second part of the Datalog query instance.
Second set of rules in the Datalog program (Figure 9): We have a bound on the number of write timestamps that can be used by the \( \text{dis} \) threads - an easy bound is the combined number of instructions in \( \text{dis} \) threads, \(|c_{\text{dis}}|\). We will refer to this bound as \( T \). By the simplified semantics it suffices to consider the timestamps \( \{0, 0^+, \ldots, T, T^+\} \). This follows since, the \( \text{dis} \) threads perform atmost \( T \) writes. Hence we need only \( T \) timestamps of the form \( \mathbb{N} \). Additionally, we have only one timestamp of the form \( \mathbb{N}^+ \) between any two timestamps of the form \( \mathbb{N} \). This shows that the view terms in the predicates of the Datalog program can be guessed in polynomial space (since \( T \) is polynomial in the input).

Now for each \( \text{dis} \) thread \( i \), the procedure \( \text{Algo} \) non-deterministically guesses the computation \( \rho_i \) for \( \text{dis}[i] \). That is, \( \text{Algo} \) guesses the timestamps and the register valuations of \( \text{dis}_i \) at each configuration in this run, along with the messages \( \text{dis}_i \) loaded from. Post this, it converts \( \rho_i \) to a set of rules which are then added to the earlier set from Figure 8.

Consider the computation \( \rho_i \equiv \lambda_{\text{init}} \xrightarrow{1_i} \lambda_1 \xrightarrow{2_i} \lambda_2 \cdots \xrightarrow{|\rho_i|} \lambda_{|\rho_i|} \) of length \(|\rho_i|\). Let the views of \( \text{dis} \) thread \( i \) at point \( j \) in the run be given as \( \text{vw}_j \). Additionally, if \( 1_j \) is a load instruction, \( \text{Algo} \) also guesses the message that was read by the \( \text{dis} \) thread \( i \). Each instruction \( 1_j \) in this computation is then converted into one amongst the rules in Figure 9a depending on the instruction \( 1_j \) executed, represented in the figure as ‘condition’. Additionally to encode the \( \mathbb{N}^+ \) timestamps that have not been occupied by CAS operations (and hence are free to use by the \( \text{dis} \) threads), we have the rule in 9b.

Since we have the polynomial bound on \( T \), it is easy to see that the rules above for the run \( \rho_i \) executed by each \( \text{dis} \) thread \( i \) can be generated in polynomial-time after nondeterministically guessing \( \rho_i \). These (non-determinism dependent) rules along with the rules from Figure 8 together form the complete Datalog program.

5.1.2 Invariants for (Datalog Inference \( \leftrightarrow \) Computations in the Simplified Semantics) and proof of Lemma 8

Now we see how an inference process in the (complete) Datalog program corresponds to a computation in the simplified semantics. To do this, we give invariants which relate the inference of atoms in the Datalog program with the existence of events in the computation. These invariants together imply the equivalence between an inference sequence in the Datalog program and a computation of \( c \) under the simplified semantics. Finally, if the goal message \( \text{msg}^\# \) is reachable at the end of a computation \( \rho \) of \( c \), then correspondingly, thanks to the invariants we obtain, we can also infer the ground term \( g \) being \( \text{dmp}(\text{msg}^\#) \) or \( \text{emp}(\text{msg}^\#) \) in the Datalog program depending on whether the goal message was generated by a \( \text{dis} \) thread or \( \text{env} \) thread in the computation.

1. \text{env} thread-local state invariant

The ground atom \( \text{etp}(\lambda, rv, \text{vw}^{de}) \) can be inferred iff some \text{env} thread can reach the \( \text{lef} = (\lambda, rv, \text{vw}^{de}) \).

This says that some \text{env} thread is able to reach the state from its transition system with label \( \lambda \) such that the thread-local view and the register valuation at that time are \( \text{vw}^{de} \) and \( rv \) respectively. We can prove that this holds by induction on the length of the run and by noting from the Datalog rules (Figure 8) that there is a transition \( \lambda \xrightarrow{5} \lambda' \) whenever there is a rule corresponding to that. Additionally, the load rules (in blue) require that the corresponding message atoms (\( \text{emp}/\text{dmp} \)) holds which as we will see below implies the possibility of the generation of a message in the memory.

2. \text{env} thread message invariant
(a) These rules are chosen depending upon the nondeterministic choice made by \texttt{Alg0} of the computation \(\rho_i\) of thread \(i\). Each instruction \(i_j\) executing in \(\rho_i\) is then mapped to one of the rules from above depending upon which condition (right column) is satisfied. Rules for silent \(i_j\) (in orange); memory accesses, loads and stores (in pink), and CAS (gray). The second pink rule corresponds to message generation by the thread \(i\) executing a store instruction. The first two CAS rules correspond to the case where the load is from an env message and the last two correspond to a dis message. The first rule for each case is the thread-local state change rule while the second rule generates the ground atom corresponding to the message generated by the CAS operation.

| Rule | Condition on thread transition \(i_j\) of computation \(\rho_i\) for thread \(\text{dis}\) |
|------|-----------------------------------------------|
| \(\text{dtp}((\lambda, rv, vw^*)\langle i \lambda \rangle, \text{msg} = (x, d, vw^*)\rangle\) | \(i_j = \text{skip}\) |
| \(\text{dtp}((\lambda, rv, vw^*)\langle i \lambda \rangle, \text{msg} = (x, d, vw^*)\rangle\) | \(i_j = \text{assume } (\rho_i \land \text{env}(\text{msg} = (x, d, vw^*)\langle i \lambda \rangle)) \neq 0\) |
| \(\text{dtp}((\lambda, rv, vw^*)\langle i \lambda \rangle, \text{msg} = (x, d, vw^*)\rangle\) | \(i_j = r = \text{emp}(\lambda)\) |
| \(\text{dtp}((\lambda, rv, vw^*)\langle i \lambda \rangle, \text{msg} = (x, d, vw^*)\rangle\) | \(i_j = r = \text{emp}(\lambda)\) |
| \(\text{dtp}((\lambda, rv, vw^*)\langle i \lambda \rangle, \text{msg} = (x, d, vw^*)\rangle\) | \(i_j = r = x \land \text{thread loads msg} = (x, d, vw^*) \land \text{env}(\text{msg} = (x, d, vw^*)\langle i \lambda \rangle) \in \mathbb{N}^+\) |
| \(\text{dtp}((\lambda, rv, vw^*)\langle i \lambda \rangle, \text{msg} = (x, d, vw^*)\rangle\) | \(i_j = r = x \land \text{thread loads msg} = (x, d, vw^*) \land \text{env}(\text{msg} = (x, d, vw^*)\langle i \lambda \rangle) \in \mathbb{N}^+\land \text{env}(\text{msg} = (x, d, vw^*)\langle i \lambda \rangle) < vs^+\) |
| \(\text{dtp}((\lambda, rv, vw^*)\langle i \lambda \rangle, \text{msg} = (x, d, vw^*)\rangle\) | \(i_j = r = x \land \text{thread loads msg} = (x, d, vw^*) \land \text{env}(\text{msg} = (x, d, vw^*)\langle i \lambda \rangle) \in \mathbb{N}^+\land \text{env}(\text{msg} = (x, d, vw^*)\langle i \lambda \rangle) < vs^+\) |
| \(\text{dtp}((\lambda, rv, vw^*)\langle i \lambda \rangle, \text{msg} = (x, d, vw^*)\rangle\) | \(i_j = r = x \land \text{thread loads msg} = (x, d, vw^*) \land \text{env}(\text{msg} = (x, d, vw^*)\langle i \lambda \rangle) \in \mathbb{N}^+\land \text{env}(\text{msg} = (x, d, vw^*)\langle i \lambda \rangle) < vs^+\) |
| \(\text{dtp}((\lambda, rv, vw^*)\langle i \lambda \rangle, \text{msg} = (x, d, vw^*)\rangle\) | \(i_j = \text{cas}(x, d, r) \land \text{env}(\text{msg} = (x, d, vw^*)\langle i \lambda \rangle) \in \mathbb{N}^+\land \text{env}(\text{msg} = (x, d, vw^*)\langle i \lambda \rangle) < vs^+\) |
| \(\text{dtp}((\lambda, rv, vw^*)\langle i \lambda \rangle, \text{msg} = (x, d, vw^*)\rangle\) | \(i_j = \text{cas}(x, d, r) \land \text{env}(\text{msg} = (x, d, vw^*)\langle i \lambda \rangle) \in \mathbb{N}^+\land \text{env}(\text{msg} = (x, d, vw^*)\langle i \lambda \rangle) < vs^+\) |
| \(\text{dtp}((\lambda, rv, vw^*)\langle i \lambda \rangle, \text{msg} = (x, d, vw^*)\rangle\) | \(i_j = \text{cas}(x, d, r) \land \text{env}(\text{msg} = (x, d, vw^*)\langle i \lambda \rangle) \in \mathbb{N}^+\land \text{env}(\text{msg} = (x, d, vw^*)\langle i \lambda \rangle) < vs^+\) |

(b) This fact corresponds to the availability of a \(\mathbb{N}^+\) timestamp for stores by env threads, which is known once all the dis computations have been guessed. These rules are not generated on a per-dis thread basis but rather once the computations \(\rho_i\) for all dis threads have been non-deterministically guessed. Referring to the simplified semantics, this rule captures \(ts \not\in B\), the fact that there is no CAS operation with timestamps \((ts, ts + 1)\). Note that the avail predicate plays a role in inferring the env thread state and message predicates as seen in the last two rows in Figure 8: we can infer the env thread state and message predicates with a view \(vw(x)\) only when the respective timestamp is not blocked. This in turn is used in the first CAS operation (first gray row, Figure 9(a)) when loads happen from an env thread: the merged view \(vw^{env}(x) = vw^{env}(x) \sqcup env(vw^{env}(x))\) is \(ts^+\), and the new timestamp after CAS is \(ts + 1\). Note that this is possible since (i) if the timestamp of the env thread for \(x\) from where we load was \(ts^+\), then there is no dis thread with a timestamp \(ts\) for \(x\) and, (ii) if the timestamp of the env thread from where we load was \(< ts^+\), then the timestamp of the dis thread performing the CAS was \(ts\) for \(x\). In both cases, the timestamp after CAS will be \(ts + 1\).

Figure 9 Second set of rules for the Datalog Program. This rule set depends on the nondeterministic choice made by \texttt{Alg0} for the computations of the env threads

The ground atom \(\text{emp}(x, d, vw^{dis})\) can be inferred if the corresponding message \(\text{msg} = (x, d, vw^{dis})\) can be generated in the simplified semantics by some env thread.

Note that a ground atom of the form \(\text{emp}(x, d, vw^{dis})\) can only be inferred using the last rule in Figure 8. The body of this rule contains the term \(\text{etp}(\lambda, rv, vw^{dis})\). This, if true, implies that some env thread can reach the corresponding thread-local state by the first invariant (above). An env thread in this thread-local state can generate the message \((x, rv(r), vw^{dis})\) since there is an outgoing transition from \(\lambda\) with instruction \(x := r\). Note that we have the check on the existence of the transition to ensure that the message can indeed be generated. This is required for the last rule to exist in the program. This implies that the message can indeed be generated.

3. \textbf{dis thread-local state} For each dis thread \(i\), we have the following invariant.
The ground atom \( \text{dtp}[i](\lambda, \text{rv}, \text{vw}^{\text{de}}) \) can be inferred iff the \text{dis} thread \( i \) can reach the lcf = \((\lambda, \text{rv}, \text{vw}^{\text{de}})\).

This is just the \text{dis} analog of the first invariant for \text{env} threads. This can also be proved by induction on the length of the run (or the inference sequence). Also analogous to the invariant for the \text{emp}, we have an invariant for \text{dis} messages.

4. **dis thread message** invariant

The ground atom \( \text{dmp}(x, d, \text{vw}^{\text{de}}) \) can be inferred if the corresponding \((\text{dis})\) message \( \text{msg} = (x, d, \text{vw}^{\text{de}}) \) can be generated in the simplified semantics by some \text{dis} thread.

5. **avail timestamp availability** invariant

If the fact \( \text{avail}(x, ts^+) \) is in the Datalog program then we have \( ts \not\in B \) throughout the computation \( \rho \) of the simplified semantics.

The base case for message predicates holds since the facts \( \text{dmp}(x, d_{\text{init}}, \text{vw}_{\text{init}}^{\text{de}}) \) for all variables are given in the Datalog program. The base case for thread state predicates holds due to the fact \( \text{etp}(\lambda_{\text{init}}, r_{\text{init}}, \text{vw}_{\text{init}}^{\text{de}}) \) which captures the initial state of the thread. The inductive steps can be formally proved by considering a computation \( \rho \) under the simplified semantics and mapping each transition in \( \rho \) to an inference step in the Datalog program. For the converse, we assume an inference sequence (a sequence of invocations of the rules) and, for each rule invoked to infer a new ground atom, we show that a corresponding transition can be taken by a thread in the simplified semantics so that the invariants are maintained. This in turn, is done by taking cases on the next instruction to be executed.

The equivalence between transitions in a computation (hence a computation \( \rho \)) of the simplified semantics and the application of rules/facts in the Datalog program, leading to reachability of some message \( \text{msg} \) in \( \rho \) iff the corresponding ground term \( \text{dmp}(\text{msg}) \) or \( \text{emp}(\text{msg}) \) is inferred in Datalog is sufficient to prove Lemma 8. In particular, the generation of \( \text{msg}^{\text{de}} \) in some computation \( \rho \) of \( \mathcal{C} \) gives a sub-computation \( \rho \downarrow_{\text{dis}} \) performed by the \text{dis} threads. We consider the Datalog query instance \( (\text{Prog}, g) \) generated where \( \text{Alg} \) correctly guesses \( \rho \downarrow_{\text{dis}} \). By the message generation invariant, the ground atom \( \text{dmp}(\text{msg}^{\text{de}}) \) or \( \text{emp}(\text{msg}^{\text{de}}) \) corresponding to \( \text{msg}^{\text{de}} \) can be inferred, \( \text{Prog} \vdash g \), giving the forward direction of the lemma.

For the reverse direction, we note that \( \text{Prog} \vdash \text{emp}(\text{msg}^{\text{de}}) \) or \( \text{Prog} \vdash \text{dmp}(\text{msg}^{\text{de}}) \) immediately implies that the message can be generated in some computation of the system \( \mathcal{C} \) (the \text{dis} computation is already determined in the guessed program \( \text{Prog} \)).

### 5.2 Cache Size

Having described the encoding(s), the challenge now is to provide a polynomial bound on the cache size for the query instances generated by \( \text{Alg} \). The Cache behaves like a memoized set of atoms which are used for the inference process. The reason why a polynomial sized Cache suffices is that we can “forget” (remove from Cache) previously inferred atoms when they are not being actively used. We use this crucially in the context of \text{env} predicates, \text{emp}, \text{etp}.

Technically this is possible since the arbitrary replication property of \text{env} threads allows us to “forget” the state of the previously simulated \text{env} thread and simulate a fresh copy instead.

Let \( Q_0 = |\text{Dom}| |\text{Var}| + |\text{dis}| \). We show that a Cache of size \( O(Q_0^2) \) is sufficient to infer \( g \).

\begin{lemma}
For each \((\text{Prog}, g)\) generated by \( \text{Alg} \), \( \text{Prog} \vdash g \) if and only if \( \text{Prog} \vdash_k g \) with \( k \in O(Q_0^2) \).
\end{lemma}

An inference sequence performed on \( \text{Prog} \) corresponds to a computation of the parameterized system \( \mathcal{C} \) in the simplified semantics (Section 5.1.2). Hence, to see that the above size of
Consider a computation \( \rho^{de} \) ending in the configuration \( \text{last}(\rho^{de}) = (m^{de}, \text{lcfm}^{de}) \). For every message \( \text{msg}^{de} \) in \( m^{de} \), we define \( \text{genthread}(\text{msg}^{de}) \) as the first thread which added \( \text{msg}^{de} \) to the memory \( m^{de} \). (Recall that the simplified semantics admits repeated insertions for \( \text{env} \) messages due to reuse of timestamps from \( \mathbb{N}^+ \)). We define \( \text{depend}(\text{msg}^{de}) \) as the set of messages which \( \text{genthread}(\text{msg}^{de}) \) reads from, before generating the first instance of \( \text{msg}^{de} \).

We define the notion of a dependency graph for a computation \( \rho^{de} \). The dependency graph of a computation \( \rho^{de} \) with \( \text{last}(\rho^{de}) = (m^{de}, \text{lcfm}^{de}) \) is the directed graph \( G_{\rho^{de}} = (V,E) \) whose vertices \( V = m^{de} \) are the messages in the final configuration and whose edges reflect the dependencies, \( (\text{msg}^{de}_1, \text{msg}^{de}_2) \in E \) if \( \text{msg}^{de}_1 \in \text{depend}(\text{msg}^{de}_2) \).

As \( \text{depend}(\cdot) \) is based on the linear order of the computation, the dependency graph is acyclic. The cyclicity of dependency graphs follows immediately from the definition of \( \text{depend} \). If there is a cycle, then all the threads involved in the cycle would be dependent on each other for the first generation of the respective message, thus causing a deadlock. We denote the sets of sink and source vertices of \( G \) by \( \text{sink}(G) \) resp. \( \text{source}(G) \). A path in \( G \) is also called a dependency sequence. A path or dependency sequence \( m_1 \rightarrow m_2 \rightarrow m_3 \rightarrow \ldots \rightarrow m_{n-1} \rightarrow m_n \) thus says that \( m_1 \) was read by some thread which generated \( m_2 \), \( m_2 \) in turn was read by a thread which generated \( m_3 \) and so on till the thread which generated \( m_n \) read \( m_{n-1} \). Given such a sequence, we say \( m_i \) is an ancestor of \( m_j \) if \( i < j \). The height of a vertex \( v \) is the length of a longest path from a source vertex to \( v \). The maximal height over all vertices is \( \text{height}(G) \). See Figure 10 for an example.

**Figure 10** Two possible dependency graphs for the code snippet. \( T_1, T_2 \) are both \( \text{env} \) threads. The color of each message \( \text{msg}^{de} \) signifies \( \text{genthread}(\text{msg}^{de}) \) (\( T_1 \) orange, \( T_2 \) violet, init gray). We denote the view as a vector \( T_y T_x \). Since we only consider the thread adding a message for the first time \( \text{genthread}(y,2,0+0^+) \) can be either \( T_1 \) (left graph) or \( T_2 \) (right graph).

**Compact Computations.** Unfortunately, dependency graphs may contain exponentially many vertices (due to the views), and given the \( \text{PSPACE} \)-hardness in Section 7 there is no way to reduce this to polynomial size. Yet, there are two parameters that we can reduce, the ‘fan-in’ of each vertex \( v \) (number of messages read by \( \text{genthread}(v) \) before generating \( v \)), and and the ‘height’ of the dependency graph (longest dependency sequence). A computation \( \rho^{de} \) is compact if its dependency graph \( G_{\rho^{de}} \) satisfies the following two bounds. (1) Every message \( v \) depends on a small number of other messages, \( |\text{depend}(v)| \leq Q_0 \). (2) The dependency sequences are polynomially long, that is, \( \text{height}(G_{\rho^{de}}) \leq Q_0 \). The following lemma says that compact computations are sufficient:

▶ **Lemma 11.** Any message that can be generated in the simplified semantics, can be generated by a compact computation.
Fan-in

Figure 11 Fan-in reduction: the dependency graph on the left can be converted to the one on the right by eliminating the redundant dependency of thread \( \text{genthread}(\text{msg}) \) on \((x, d, [\ldots, x \rightarrow ts_2, \ldots])\) when \(ts_2 > ts_1\).

Proof. We prove both parts (fan-in and height) of this lemma by showing that if there exists a computation whose dependency graph violates the bound for fan-in (similarly height), then there must exist a computation whose dependency graph has a lower fan-in (height) with the rest of the graph (fan-ins of other vertices) unchanged. We first show this for fan-in. We will assume that the programs \(c_{\text{dis}}\) executed by \(\text{dis}\) threads have been specified as a transition system (note that we can interconvert between the while-language and transition system representation with only polynomial blowup). Then \(|c_{\text{dis}}|\) is an upper bound on the total number of transitions in all \(\text{dis}\) threads together.

1. Fan-in. Suppose to the contrary, we had \(|\text{depend}(v)| > 2|\text{Dom}||\text{Var}| + |c_{\text{dis}}|\) for some message \(v\). Consider the thread \(p = \text{genthread}(v)\) which generated the message represented by vertex \(v\) for the first time. There are only \(|\text{Dom}|\) distinct \((\text{variable}, \text{value})\) pairs, \(|\text{Dom}|\) many \(\text{init}\) messages and only \(|c_{\text{dis}}|\) many \(\text{dis}\) messages \(|c_{\text{dis}}|\) is an upper bound on the number of transitions the \(\text{dis}\) thread can take). Hence by a pigeonhole argument, \(p\) must have read two \(\text{env}\) messages with same \((\text{variable}, \text{value})\) pair but distinct abstract views. Let these messages be \(m_1 = (x, d, vw_{1}^{de})\) and \(m_2 = (x, d, vw_{2}^{de})\) where the abstract views are unequal. Without loss of generality assume that \(p = \text{genthread}(v)\) read \(m_1\) first, and \(m_2\) later (in order) before it generated \(v\).

It can be seen that any time \(p\) read \(m_2\), it could have read \(m_1\) instead. This follows since timestamp comparisons are irrelevant when reading from \(\text{env}\) messages. The thread-local view obtained on replacing a read of \(m_2\) with that of \(m_1\) will only decrease or remain the same. From the simplified semantics, after reading \(m_1\) once, the thread view \(vw_{1}^{de}\) satisfies \(vw_{1}^{de} \supseteq vw_{1}^{de}\) (per-variable). Hence reading from \(m_1\) again leads to the thread view being \(vw_{1}^{de} >_{\text{env}} vw_{1}^{de}\). On the other hand, after reading \(m_2\), the view will be \(vw_{2}^{de} \|_{\text{env}} vw_{2}^{de}\) which is clearly higher than \(vw_{1}^{de}\). Indeed, instead of reading from \(m_2\), the loading thread can read from \(m_1\), resulting in a lower view for \(x\) (compared to reading from \(m_2\)).

Let \(\rho'\) denote the subcomputation starting from the position right after reading from the \(\text{env}\) message \(m_2\). We can see that if we replace this read operation by reading from \(m_1\), we can continue on \(\rho'\) as before.

= Indeed, all store operations on \(\rho'\) are independent of this load from \(m_1\) (or \(m_2\)).

= Consider a load operation along \(\rho'\). A load on a variable \(y \neq x\) is not affected clearly.

Consider now a load on \(x\) performed by loading some message \(m_3\). Assume the load is performed by \(p\). The view of \(x\) along \(\rho'\) for thread \(p\) was coming from \(m_2\) which was a least that given by \(m_1\); indeed if loading from \(m_3\) was possible in \(\rho'\) when the view on \(x\) was at least \(vw_{2}(x)\), it definitely is possible now with a lower view on \(x\).

= Lastly, consider a CAS operation on variable \(x\), along \(\rho'\). Assume the load was made from \(m_2\). If \(vw_{2}(x) = ts_{2}^{x}\) in \(m_2\), then the CAS operation will add a new message \(m_3\) on
Let there be a dependency sequence of length greater than \(|\text{Dom}|\text{Var}| + |\text{dis}|\). There are only \(|\text{Dom}|\text{Var}|\) variable, value pairs, \(|\text{Dom}|\text{Var}|\) many init messages and at most \(|\text{dis}|\) many dis messages. Hence by a pigeonhole argument, for a dependency sequence longer than \(2|\text{Dom}|\text{Var}| + |\text{dis}|\) there exists a (variable, value) pair \((x, d)\) such that there are two env messages \(m_1 = (x, d, \text{vw}_1^{\text{de}})\) and \(m_2 = (x, d, \text{vw}_2^{\text{de}})\) along it. Without loss of generality, let \(n_1\) be an ancestor of \(m_1\). So, \(n_1\) has been read before generating \(m_1\). Then we must have \(\text{vw}_1^{\text{de}} \sqsubseteq \text{vw}_2^{\text{de}}\) by the RA Semantics (since the thread generating \(m_1\) indirectly accumulates the view of \(n_1\)). Then the thread reading from \((\text{depending-upon})\) \(m_1\) could have directly read from \(n_1\) instead (note that since \(m_1\) itself depends on \(n_1\), by the time \(m_1\) has been generated, \(n_1\) must have been as well). By reading from \(n_1\) its view may only decrease or remain the same thus not affecting the run (as justified above). Thus we can eventually reduce the dependency sequences so that all have length at most \(2|\text{Dom}|\text{Var}| + |\text{dis}|\).

This gives us the result.

In Cache Datalog, the inference of an atom \(g\) from the program \(\text{Prog}\) involves a sequence of applications of the Add (to Cache) and Drop (from Cache) rules that ends with \(g\) being inferred. Such a sequence for \(\text{Prog} \vdash g\) corresponds to a run \(\rho^{\text{de}}\) under the simplified RA semantics. We show that this follows by the structure of the query instance \((\text{Prog}, g)\). The run \(\rho^{\text{de}}\) can be compacted to \(\rho^{\text{de}'}\) by Lemma \([11]\). From the dependency graph of \(\rho^{\text{de}'}\) we can read off an inference strategy that keeps the Cache size polynomial in \(|\text{Var}|, |\text{Dom}|\) and \(|\text{dis}|\). The following lemma formalizes this argument and so proves Proposition \([9]\). We now proceed by showing Lemma \([12]\). This lemma along with Lemma \([11]\) together gives Proposition \([9]\) and will lead to the coveted \(\text{PSPACE}\)-bound. Since the term \(2|\text{Dom}|\text{Var}| + |\text{dis}|\) will occur repeatedly, we denote it by the the quantity \(Q_0\). From here on, \(Q_0 = 2|\text{Dom}|\text{Var}| + |\text{dis}|\).

\[\textbf{Lemma 12 (Datalog Inference Strategy).}\] Let \(\text{Algo}\) generate the query instance \((\text{Prog}, g)\). The inference for \(\text{Prog} \vdash g\) implies the existence of an execution \(\rho^{\text{de}}\) under the simplified
semantics, which can be compacted to \( \rho^{def} \). The computation \( \rho^{def} \) can be mapped back to a new inference sequence such that \( \text{Prog} \vdash_k g \) for \( k \in \Theta(Q_0^2) \).

**Proof.** This lemma has two parts: (1) it states that computations in the simplified semantics and inference sequences in the Cache Datalog program are related and (2) it says that compact computations can be mapped to an inference sequence with a small Cache size.

Let \( (\text{Prog}, g) \) be generated by the procedure \( \text{Algo} \) with \( \text{Prog} \vdash g \). We need to show that \( g \) can also be inferred from \( \text{Prog} \) with a small Cache. Recall that when generating the Datalog program \( \text{Prog} \), the procedure \( \text{Algo} \) guesses the computations of the dis processes. Consider some inference sequence for \( \text{Prog} \vdash g \). For each application of an inference rule in the sequence, we can find a corresponding transition of a thread in the simplified semantics. This follows from the invariants in section 5.1.2. Hence we can convert the sequence of inferences to a run \( \rho^{def} \). This run in turn can be compacted by the arguments in Lemma 11 to get a smaller run \( \rho^{def'} \). Now we need to see how this compact run implies the existence of an inference sequence with smaller sized Cache. To do this we consider the dependency graph of \( \rho^{def'} \).

We proceed by induction on the height of messages in the dependency graph. We strengthen the statement and show that for every message \( msg^{de} \) at a height given by \( \text{height}(msg^{de}) = h \), we have \( \text{Prog} \vdash_k \text{emp}(msg^{de}) \) \( (\text{Prog} \vdash_k \text{dmp}(msg^{de})) \) for \( k = h \times Q_0 \). The lemma follows by the definition of compactness, which guarantees \( h \leq \text{height}(G^{de}_\rho) \leq Q_0 \).

The base case is trivial, since all messages in \( \text{sink}(G^{de}_\rho) \) are facts in the Datalog program \( \text{Prog} \). We now show the inductive case for a message \( v \in G^{de}_\rho \) at height \( h + 1 \). The messages \( v' \) in \( \text{depend}(v) \) have height at most \( h \). The inductive hypothesis thus yields \( \text{Prog} \vdash_h Q_0 v' \). We infer these messages one at a time, store them in the Cache, and discard all atoms in the Cache used for the inference of the \( v' \). Hence at each step in the inference sequence, the Cache contains a subset of \( \text{depend}(v) \) which has already been inferred, and, additionally some atoms which are currently being used for the inference of the next member of \( \text{depend}(v) \). The former is bounded by \( Q_0 \) by the compactness (Lemma 11) \( |\text{depend}(v)| < Q_0 \) while the latter is bounded by \( hQ_0 \) by the induction hypothesis. Together the size of the Cache never exceeds \((h + 1)Q_0\). Thus by reusing the space in the Cache to infer members of \( \text{depend}(v) \), we only require an additional space of \( Q_0 \). At the end of this process, the size of the Cache equals \( |\text{depend}(v)| \) and the space consumption of the dependencies is at most

\[
(h + 1)Q_0 - 1
\]

Now we want to infer the message corresponding to \( v \), having inferred and inserted into Cache atoms corresponding to messages from \( \text{depend}(v) \). This inference of \( v \) from the messages in \( \text{depend}(v) \) requires us to simulate the run of \( \text{genthread}(v) \) using the rules of the Datalog program (by mapping each transition executed by \( \text{genthread}(v) \) to its corresponding rule from the Datalog program). We note that at all points in the simulation it suffices to store exactly one extra atom either of \( \text{etp} \) or of \( \text{dtp} \) (depending upon the type of \( \text{genthread}(v) \)) corresponding to the local state of \( \text{genthread}(v) \). The additional atom can be accommodated along with \( \text{depend}(v) \) since \( |\text{depend}(v)| + 1 < (h + 1)Q_0 \) (since \( |\text{depend}(v)| < Q_0 \)).

Hence a Cache of size at most \( 2(h + 1)(|\text{Dom}||\text{Var}| + |c_{dis}|) \) is sufficient, and by induction the lemma follows.

Lemma 11 along with the compact inference sequences, Lemma 12 together show that for all the query instances generated by \( \text{Algo} \), inference is possible if it is possible with a small Cache. This shows Lemma 9 giving us PSPACE-membership.
6 Safety Verification with Leader

In this section our goal is to support compositional verification methods prominent in program logics and thread-modular reasoning style algorithmic verification. Such approaches focus on a single thread and study its interaction with others.

We extend the system from section 5 by adding a single distinguished ‘ego’ thread, which we refer to as the leader, denoted by the symbol ldr. Amongst the n dis threads only the ldr can execute loops, while the others, like section 5 are required to be loop-free.

The environment once again consists of arbitrarily many identical env threads that are required to be cas-free. We can represent this as env(nocas) || dis1 || dis2(acyc) || · · · || disn(acyc) which we refer to as the leader setting.

Note that the simplified semantics presented in Section 4 applies here. This allows us to leverage Theorem 5 by which we can operate on the simplified semantics instead. The main challenge of this section then is to go from the simplified semantics in the presence of a leader to an NEXPTIME verification technique, by means of a small model argument.

6.1 Dependency Analysis

As discussed before, the safety verification problem amounts to solving the message generation problem (MG) (section 5.1). Let the goal message be denoted msg#.

We demonstrate that the simplified semantics helps solving the problem.

Our main finding is that message generation has short witness computations (assuming the domain is finite). The proof of Theorem 13 is in Section 6.3.

\[ \text{Theorem 13. In the leader setting, a message can be generated in the simplified semantics if and only if it can be generated by a computation of length at most exponential in the input specification, } |c_{dis}| \cdot |c_{env}| \cdot |Reg| \cdot |Dom| \cdot |Var|. \]

\[ \text{Corollary 14. In the leader setting, the message generation problem for RA is in NEXPTIME.} \]

We establish the result in two steps. First we show that every computation in the simplified semantics has a “backbone”, which is made up solely by some threads called essential threads (Lemma 16). Then we show how to truncate this backbone to obtain a short computation (Section 6.2).

Analyzing Dependencies in the Dependency Graph. The following study of dependencies generalizes the one in Section 5.2. In a computation of the simplified semantics, messages from the dis threads have unique timestamps whereas messages from env threads may have identical timestamps. We recall genthread(msg), the thread which first generated message msg, and the dependency set of a message msg, denoted by depend(msg) as defined earlier in Section 5.2.

We define depend(msg) = ∅ for initial messages. We write depend*(msg) for the reflexive and transitive closure of depend, the smallest set containing msg and such that for all msg′ ∈ depend*(msg) we have depend(msg′) ⊆ depend*(msg).

Similar to Lemma 11 we now show that we can focus on computations where any write event directly depends on a small number of other events, and where dependency sequences are short. The main difference with Section 5.2 is that since the leader has loops, we cannot apriori bound executions w.r.t. |c_{dis}|. Keeping this in mind, we provide an alternative notion for compact computations.
Compact Computations. We call a computation $\rho$ compact if for every env message $msg \in \text{depend}^*(msg^\#)$ in the computation (1) $|\text{depend}(msg) \cap \text{Msgs}(\rho \downarrow_{\text{env}})| \leq |\text{Dom}|\text{Var}$ and (2) for every $msg' \neq msg$ from $\text{depend}^*(msg) \cap \text{Msgs}(\rho \downarrow_{\text{env}})$ either the variable or the value is different from $msg$. The first point addresses the situation where an env thread reads two messages with the same variable and value but different views: it says that the thread could have chosen to read one of the messages twice. The second point says there is no need to generate two env messages with the same variable and value along a dependency sequence. A thread reading the second message could equally well read the first message, the $ts^+$ timestamp for env messages would make it available forever.

Lemma 15. In the leader setting, if the message $msg^\#$ can be generated in the simplified semantics, then it can be generated by a compact computation.

In a compact computation, both fan-in (size of depend set) and depth (along a dependency sequence) of env messages is $O(|\text{Dom}|\text{Var})$ since there are only as many distinct (variable, value) pairs. Hence $O(|\text{Dom}|\text{Var})^{|\text{Dom}|\text{Var}}$ many env messages are sufficient to generate $msg^\#$. Our goal is to derive a similar bound on dis messages. First, we consider the dis messages read by env threads, i.e. the dis-env reads-from dependencies. The dis-dis dependencies will be handled later.

Essential Messages and Threads. Given a computation $\rho$ in the simplified semantics, the essential messages for generating message $msg$, denoted by $\text{edepend}(msg)$, is the smallest set that includes $msg$ and is closed as follows.

1. (1) $\forall$ messages $msg' \in \text{edepend}(msg) \cap \text{Msgs}(\rho \downarrow_{\text{env}})$ we have $\text{depend}(msg') \subseteq \text{edepend}(msg)$.
2. $\forall$ $msg' \in \text{edepend}(msg) \cap \text{Msgs}(\rho \downarrow_{\text{dis}})$ we have $\text{depend}(msg') \cap \text{Msgs}(\rho \downarrow_{\text{env}}) \subseteq \text{edepend}(msg)$.

Note the asymmetry, for the env threads we track all dependencies, for the dis threads we only track the dependencies from env.

For a computation $\rho$, the threads generating essential messages of $msg^\#$ for the first time and the set of dis threads are essential threads; $\text{ethread}(\rho) = \{\text{genthread}(m) | m \in \text{edepend}(msg^\#)\} \cup \text{dis}$.

We claim that projecting $\rho$ to essential threads yields a valid computation in the simplified semantics. Essential messages thus form the backbone of the computation mentioned above. We now give the proof of Lemma [16] and Corollary [17].

Lemma 16. If $\rho$ is a computation in the simplified semantics, so is $\rho \downarrow_{\text{ethread}(\rho)}$.

Proof. To prove this theorem it suffices to show that there is no thread in $\text{ethread}(\rho)$ that reads from some thread $t' \notin \text{ethread}(\rho)$. Then we simply can project away the threads not in $\text{ethread}(\rho)$ and all the reads-from dependencies will still be respected.

This follows trivially from the definition of $\text{edepend}(\ )$. Indeed we have that for an essential env thread $t$ the messages (and hence threads) that $t$ reads from are also essential. All dis threads are essential by definition. Additionally, for any dis thread, we add all its env dependencies to the essential set. The set $\text{ethread}(\rho)$ is then closed under reads-from dependencies and hence the computation $\rho \downarrow_{\text{edepend}(\rho)}$ is valid under RA.

Now we discuss bounding of essential messages. Essential env messages and (essential env threads) are almost exponential, bounded by $Q_1 = |\text{Dom}|\text{Var}^{|\text{Dom}|\text{Var}}$ using the earlier compactness argument. We show that the number of essential dis messages is bounded as well. Firstly, each env thread has a state space (control-state, registers) bounded by $Q_2 = |c_{\text{env}}||\text{Reg}|^{|\text{Dom}|}$. Given the earlier bound on total number of essential env messages
(and hence those by a single thread), an env thread run of length greater than $O(Q_1Q_2)$ implies that there will exist a sub-run in which (1) no essential message was generated and (2) the thread revisited the same local state twice. We can truncate this sub-sequence since the absence of essential messages implies that external reads-from dependencies are not affected. Hence the computation for a single env is $Q_1Q_2$-bounded. Given the $Q_1$-bound on env threads, the total number of dis messages consumed by the env threads can be atmost $Q_1^2Q_2$. This implies sufficiency with exponentially many essential dis messages.

**Corollary 17.** Let the goal message msg$^\#$ be generated in a computation of system c. Then for some compact computation, $|\text{edepend}(\text{msg}^\#)|$ is at most exponential in $|c|$.

**Proof.** Recall the notation genthread(msg) which refers to a thread which generated the message msg for the first time. In the following, if $t = \text{genthread}(\text{msg})$, we also refer to t as the “first writer” of msg.

First we observe that $\text{edepend}(\text{msg}) \subseteq \text{depend}(\text{msg})$. Hence in particular, we have $\text{edepend}(\text{msg}^\#) \cap \text{Msgs}(\rho_{\downarrow_{\text{env}}}) \subseteq \text{depend}(\text{msg}^\#) \cap \text{Msgs}(\rho_{\downarrow_{\text{env}}})$. This is shown to be at most exponential ($O(Q_1)$) by Lemma 17, since both the height and the env fan-in of the dependency graph restricted to env is polynomial. Given that each essential message is generated for the first time by a unique essential thread, the number of essential env threads is also bounded by $O(Q_1)$.

Now, consider the fragment $\rho'$ of the computation between two consecutive first-writes (first points of generation) of two essential env messages. Now if any env thread performs more than $O(Q_2) = O(|\text{cenv}| |\text{Reg}||\text{Dom}||)$ many transitions within $\rho'$ it would imply that there are two configurations $lcf_1, lcf_2$ within $\rho'$ at which the local-states of the thread (modulo view) are identical - this follows since $|\text{cenv}|$ is the program size and $|\text{Reg}||\text{Dom}||$ is the number of distinct register valuations. Additionally note that the view at lcf cannot be greater than that at lcf (monotonicity of views in RA). Hence we can simply truncate the sub-computation between lcf_1 and lcf_2 while keeping the computation still valid under RA (the thread with lower view can still perform all its remaining transitions). In this truncation no essential messages will be lost and hence the reads-from dependencies will be respected.

To explain further, suppose to the contrary that some thread $t$ which is the first writer of an essential message executed more than $O(Q_1Q_2)$ number of transitions $lcf_t lcf_1 \cdots lcf_l$. Since the total number of essential messages is only $O(Q_1)$, there must exist a subsequence $\sigma$ such that no essential env messages were generated (for the first time) in $\sigma$. Additionally, since the state-space of each thread is $O(Q_2)$, by a pigeon-hole argument, it follows that two local configurations $lcf_t, lcf_j$ of $t$ in $\sigma$ are equal. We can simply truncate the fragment of the run between these configurations since no essential messages have been generated for the first time.

Then it suffices for each first writer env thread to take at most $O(Q_1Q_2)$ many transitions and consequently read at most exponentially many dis messages. Recall that the dis messages that are read by first writers of essential env messages are essential themselves. Since the number of essential env threads which are first writers itself is bounded by $O(Q_1)$, the number of essential dis messages is bounded by $O(Q_1^2Q_2)$, which is exponential in the input. Since $\text{edepend}(\text{msg}^\#)$ is a union of essential dis and env messages we get the exponential bound on essential messages.

Combined with Lemma 17, the corollary says it is sufficient to focus on computations with atmost exponentially many essential threads and essential messages. We now want to bound the computation of the dis threads.
6.2 Short Witnesses

The computation truncation idea as applied to env threads earlier does not apply to the leader. Recall the asymmetry in the definition of essential dependencies; we did not include the dis-dis load dependencies. The dependencies come in two forms: (1) those involving (either as message writer or as reader) some non-leader dis thread and (2) ldr-ldr dependencies. The former are poly-sized owing to the loop-free nature of the non-leader dis threads. Hence, we focus on ldr-ldr dependencies. For a memory $m^{de}_1$, let $m^{de}_1 \downarrow_{ldr}$ be the set of ldr messages in it. Assuming $vw^{de}$ is the view of the ldr, let selfRead($vw^{de}, m^{de}$) denote the $(x, d)$ pairs in messages of $m^{de}_1 \downarrow_{ldr}$, which can be read by ldr.

Definition 18. selfRead($vw^{de}, m^{de}$) = \{(x, d) \mid (x, d, vw^{de}_1) \in m^{de} \downarrow_{ldr}, vw^{de}(x) = vw^{de}_1(x)\}.

We note that a pair $(x, d)$ is in selfRead when this pair is the last store by the ldr on x following which $vw^{de}(x)$ has not changed. Observe that there can be at most $|\text{Var}|^{|\text{Dom}|}$ many distinct selfRead functions. Consider a sub-computation of the leader between two generations of essential messages. We call configurations $cf^{de}_1$ and $cf^{de}_2$ ldr-equivalent if (1) the local configurations of the leader coincide except for the views $vw^{de}_1$ resp. $vw^{de}_2$ and (2) the memories $m^{de}_1$ and $m^{de}_2$ satisfy

\[\text{selfRead}(vw^{de}_1, m^{de}_1) = \text{selfRead}(vw^{de}_2, m^{de}_2)\]

Then the computation of the leader between $cf^{de}_1$ and $cf^{de}_2$ can be projected away while retaining a computation in the simplified semantics. Since there are only $O(|\text{ldr}|(|\text{Reg}||\text{Var}|)^{|\text{Dom}|})$ many distinct configurations that are not ldr-equivalent, after projecting away the redundant part, the leader will have an at most exponentially long computation between generations of two consecutive essential messages. Given the exponential bound on all essential messages, we see that post projection, the leader computation is reduced to exponential size. Combined with the argument for the env and non-leader dis threads, gives Theorem 13. Note that the resulting non-deterministic algorithm does not run in polynomial space as there may be exponentially many essential ldr messages which need to be generated concurrently with the env threads.

6.3 Theorem 13: NEXPTIME-membership of safety verification in the leader case

We now move on to Theorem 13. It suffices to show that we only need to consider computations of exponential length in order to verify safety properties of a parameterized system under the simplified semantics in the leader case. For this, we show exponential bounds on the env and dis components of the computation.

We have already seen that for the essential env threads, $O(Q_1^2 Q_2)$ is an upper bound on the number of transitions they need to make. Additionally this bound also applies to the number of essential dis messages. Note that the non-leader dis threads are loop-free and hence their number of transitions is polynomial in $|\text{dis}|$. Hence we now focus on computations of the leader. We denote $Q_3 = |\text{ldr}|(|\text{Reg}||\text{Var}|)^{|\text{Dom}|}$ which is a bound on the number of distinct (non equivalent) leader configurations and use it below in the proof.

For the ldr, we need to maintain more states (as compared to the env threads) to ensure that the truncated run is valid. This is so as we also want to capture ldr-ldr dependencies as
well. The selfRead function does precisely this - at each point in the run it tracks the set of ldr messages that can be read by the ldr itself.

Assume once again that there is a (super-exponential) leader computation with length greater than $O(Q_1^2 Q_2 Q_3)$. Then since $O(Q_1^2 Q_2)$ is a bound on the number of total dis essential messages (and in particular essential ldr messages), there must exist a sub-computation of the ldr of length greater than $O(Q_3)$ that is free of essential message generation. Let this sub-computation be lcf_1 lcf_2 ... lcf_i. Assume the memory states along this sub-computation to be $m_1^e m_2^e ... m_i^e$.

We augment each configuration lcf_i with the respective memory state $m_i^e$ obtaining an augmented configuration as explained below. Consider the configurations obtained by augmenting lcf = $(c, rv, vw^e)$ to the set selfRead($vw^e, m^e$). That is, given $lcf_i = (c_i, rv_i, vw_i^e)$, on augmentation with selfRead($vw_i^e, m_i^e$) we obtain the augmented state as $\langle c_i, rv_i, selfRead(vw_i^e, m_i) \rangle$. Now, selfRead can take atmost $|Var^{Dom}|$ many values, while the leader local-state (modulo view) has only $|c_{ldr}| |Reg^{Dom}|$ values. This implies, (by a pigeon-hole argument), the existence of a pair $i, j$ such that $\langle lcf_i, selfRead(vw_i^e, m_i) \rangle$ and $\langle lcf_j, selfRead(vw_j^e, m_j) \rangle$ are equivalent.

Now, the view of the ldr thread is monotonic. This implies that if for $i \neq j$ we have $\langle c_i, rv_i, selfRead(vw_i^e, m_i) \rangle = \langle c_j, rv_j, selfRead(vw_j^e, m_j) \rangle$ then the sub-computation between $i$ and $j$ may be truncated. Thus the run lcf_1 ... lcf_i lcf_{i+1} ... lcf_j is also a valid run of the thread. Moreover it does not affect other threads since once again no essential messages are lost.

Hence for any super-exponential (order greater than $O(Q_1^2 Q_2 Q_3)$) leader computation, there exists a shorter computation which also preserves reachability. Thus for safety verification it suffices to consider runs of atmost exponential length, immediately giving an NEXPTIME upper bound.

7 Limits of Semantic Simplification I: PSPACE-hardness of env(nocas, acyc)

We show that the applications of semantic simplification to the loop-free and leader settings are tight, and further simplification is not possible.

Having shown that safety verification of env(nocas) $\parallel$ dis_1(acyc) $\parallel$ ... $\parallel$ dis_n(acyc) is in PSPACE, we give a matching lower bound. For the lower bound, it suffices to consider the variant with no dis threads and loop-free env threads, env(nocas, acyc). In fact, this result captures the inherent complexity in Parameterized RA, termed as PureRA, i.e. RA in its simplest form. The simplicity of PureRA comes from (1) disallowing registers, and (2) stores can only write value 1 and the memory is initialized with 0 values. We obtain PSPACE-hardness even with this reduced form, which is surprising, given that in its full form it is in PSPACE. Notice that the PSPACE-hardness with registers is trivial, since PSPACE can be encoded in valuations of registers.

7.1 Pure RA

In this section, we elaborate on the PSPACE-hardness of checking safety properties of parameterized systems under RA in the absence of dis threads (and loop-free, cas-free env threads), which we can denote as env(nocas, acyc). In fact, we investigate the inherent complexity in RA, by removing all extra frills like registers, as well as arbitrary data domains. So what we have is, Pure RA, which is basically, RA in its simplest form. The simplicity of Pure RA comes from the fact that we do not use registers, and the only writes that are
allowed are that of writing value 1 to any shared variable, where we assume that the memory was initialized to 0 so that we have a data domain of \{0,1\}. The remarkable thing about this result is that we obtain PSPACE-hardness, which is surprising, given that in its full form it is in PSPACE by Section 5. Notice that the PSPACE-hardness with registers is trivial, since computations can be encoded in register operations themselves.

\[
\begin{align*}
\mathbf{c} &= \mathbf{c_{AG}} \oplus \mathbf{c_{SATC}} \oplus \mathbf{c_{FE[0]}} \oplus \cdots \oplus \mathbf{c_{FE[n-1]}} \oplus \mathbf{c_{assert}} \\
\mathbf{c_{AG}} &= \text{choose}(u) = (t_0 := 0) \oplus (f_u := 0) \\
\mathbf{c_{SATC}} &= \text{assert}(s = 1); \text{check}(\Phi); \\
&\quad \quad ((\text{assume}(t_{u_0} = 0); a_{n,1} := 0)) \oplus ((\text{assume}(f_{u_0} = 0); a_{n,0} := 0)) \\
\mathbf{c_{FE[i]}} &= \text{assume}(a_{i+1,0} = 1); \text{assume}(a_{i+1,1} = 1); (\text{assume}(f_{i+1} = 0) \oplus \text{assume}(t_{i+1} = 0)); \\
&\quad \quad ((\text{assume}(t_{u_i} = 0); a_{i,1} := 1) \oplus (\text{assume}(f_{u_i} = 0); a_{i,0} := 1)) \\
\mathbf{c_{assert}} &= \text{assume}(a_{0,0} = 1); \text{assume}(a_{0,1} = 1); \text{assert false}
\end{align*}
\]

Figure 13 The parametrized system used in the reduction

### 7.1.1 A QBF Encoding

To show the PSPACE-hardness of checking safety properties of parameterized systems of the class env(nocas, acyc), we establish a reduction from the canonical PSPACE-complete problem, QBF. The QBF problem is described as follows. Given a quantified boolean formula \( \Psi = \forall u_0 \exists e_1 \forall u_1 \exists e_2 \cdots \exists e_n \forall u_n \Psi(u_0, e_1, \ldots, u_n) \), over variables \( Vars(\Psi) = \{u_0, \ldots, u_n, e_1, \ldots, e_n\} \), decide if \( \Psi \) is true. \( \Psi \) has \( n+1 \) universally quantified variables and \( n \) existentially quantified variables. To establish the reduction, we construct an instance of the parametrized reachability problem for RA (in fact Pure RA) consisting of the parametrized system \( \mathbf{c} \), such that \( \mathbf{c} \) is unsafe if and only if the QBF instance is true. We assume that the QBF instance \( \Psi \) is as given above and now detail the construction.

The program \( \mathbf{c} \) executed by the env threads (given in Figure 13) consists of functions (sub-programs), one of which may be executed non-deterministically:

\[
\mathbf{c} = \mathbf{c_{AG}} \oplus \mathbf{c_{SATC}} \oplus \mathbf{c_{FE[0]}} \oplus \cdots \oplus \mathbf{c_{FE[n-1]}} \oplus \mathbf{c_{assert}}
\]

### 7.2 Infrastructure

**Gadgets used.** The task of checking the satisfiability of \( \Psi \) is distributed over the env threads executing these functions. Each function has a particular role, which we term as gadgets and now describe.

- **\( \mathbf{c_{AG}} \)** The *Assignment Guesser* guesses a possible satisfying assignment for \( Vars(\Psi) \).
- **\( \mathbf{c_{SATC}} \)** The *SATisfiability Checker* checks satisfiability of \( \Phi \) w.r.t. an assignment guessed by \( \mathbf{c_{AG}} \).
- **\( \mathbf{c_{FE[i]}} \)** The \( \forall \exists \) (ForallExists) *Checker* at level \( i \), \( 0 \leq i \leq n-1 \) (\( \mathbf{c_{FE[i]}} \)) verifies that the \( (i+1) \)th quantifier alternation \( \forall u_i \exists e_{i+1} \) is respected by the guessed assignments. This proceeds in levels, where the check function at level \( i+1 \), \( \mathbf{c_{FE[i+1]}} \) ‘triggers’ the check function.
at level \( i \), \( c_{FE[i]} \), till we have verified that all assignments satisfying \( \Phi \) constitute the truth of \( \Psi \).

\( c_{assert} \) The Assertion Checker reaches the `assert false` instruction when all the previous functions act as intended, implying that the formula was true.

Due to the parameterization, an arbitrary number of threads may execute the different functions at the same time. However, there is no interference between threads, and there is a natural order between the roles: \( c_{SATC} \) requires \( c_{AG} \) to function as intended, and \( c_{FE[i]} \) requires the functions \( c_{AG} \), \( c_{SATC} \) and \( c_{FE[j]}, n \geq j > i \).

**Shared Variables.** We use the following set of shared variables in \( c \): For each \( x \in Vars(\Psi) \), we have boolean shared variables \( t_x \) and \( f_x \) in \( c \). These variables represent true and false assignments to \( x \) using the respective boolean variables in a way that is explained below. All the shared variables used are boolean, and the initial value of all variables is 0. We also have a special (boolean) variable \( s \).

**Encoding variable assignments of \( \Psi \): the essence of the construction.** Recall that the messages in the memory are of the form \((x, d, vw)\) where \( x \) is a shared variable, \( d \in \{0,1\} \), and \( vw \) is a view. To begin, the views of all variables are assigned time stamp 0. An assignment to the variables in \( \Psi \) can be read off from the \( vw \) of a message \((s,1,vw)\) in the memory state. For \( v \in Vars(\Psi) \), if \( vw(t_v) = 0 \), then \( v \) is considered to have been assigned true, while if \( vw(f_v) = 0 \), then \( v \) is assigned false. Our construction, explained below, ensures that exactly one of the shared variables \( t_x, f_x \) will have time stamp 0 in the view of the message \((s,1,vw)\). The zero/non-zero timestamps of variables \( t_x \) and \( f_x \) in the view of \((s,1,vw)\) can be used to check satisfiability of \( \Phi \) since only a thread with a zero timestamp can read the initial message on the corresponding variable.

**Checking a single clause.** As an example, consider the \( i^{th} \) clause \( e_1 \lor \neg u_3 \lor u_5 \). The satisfiability check is implemented in a code fragment as follows. \( check(i) = (assume \ t_{e_1} = 0) \oplus (assume \ t_{u_3} = 0) \oplus (assume \ t_{u_5} = 0) \lor check(1) \lor check(2) \lor \cdots \lor check(l) \). Finally, we have the boolean variables \( a_{i,0} \) and \( a_{i,1} \) for \( i \in \{0, \cdots, n\} \); these are \( 2(n+1) \) ‘universality enforcing’ variables that ensure that all possible assignments to the universal variables in \( Vars(\Psi) \) have been checked.

### 7.3 The Construction

First we describe the various gadgets.

#### 7.3.1 The Gadgets

We now detail the gadgets (functions) mentioned in Figure 13.

**Assignment Guesser:** \( c_{AG} \): The job of the Assignment Guesser is to guess a possible assignment for the variables. This is done by writing 1 to exactly one of the variables \( t_x, f_x \) for all \( x \in Vars(\Psi) \). Each such write is required to have a timestamp greater than 0 by the RA semantics, and the view \( vw \) of the writing thread is updated similarly. After making the assignment to all variables in \( Vars(\Psi) \) as described, the writing thread adds the message \((s,1,vw)\) to the memory.

Consequently, the view \( vw \) of the writing thread (and hence the message) satisfies

\[
\forall x \in Vars(\Phi), \quad vw(t_x) = 0 \oplus vw(f_x) = 0
\]

We interpret this as: the assignment chosen for \( x \in Vars(\Phi) \) is true if \( vw(t_x) = 0 \) and is false if \( vw(f_x) = 0 \). The chosen assignment is thus encoded in \( vw \) and hence can be incorporated
by threads loading 1 from s using the message \((s, 1, vw)\), \((s, 1, vw)\), (see \(c_{SATC}\)). This follows since load operations of the RA semantics cause the thread-local view to be updated by the view in the message loaded.

**SAT Checker**: \(c_{SATC}\): The SAT Checker reads from one of the messages of the form \((s, 1, vw)\) generated by \(c_{AG}\). Using the code explained in Figure 13, it must check that the assignment obtained using the \(vw\) satisfies \(\Phi\). The crucial observation is that \(: assume (t_x = 0) (assume (f_x = 0)) being successful with the timestamp of \(t_x (f_x)\) in \(vw\) being 0. This holds since \(\text{assume (v = 0)}\) requires the ability to read the initial message on \(v\) which in turn requires the thread-local view on \(v\) to be 0. Timestamp of \(t_x (f_x)\) in \(vw\) itself being 0 is equivalent to \(x\) being assigned the value true (false) by \(c_{AG}\).

Finally it checks that either \(t_{u_n}\) or \(f_{u_n}\) had timestamp 0 in \(vw\), and writes 1 to \(a_{n,1}\) or \(a_{n,0}\) correspondingly in Figure 13. For insight, we note prematurely that we will enforce both these writes to \(a_{n,1}\) and \(a_{n,0}\) as a way of ensuring the universality for the variable \(u_n\).

The main task is to verify the ‘goodness’ of the assignments satisfying \(\Phi\). One of the things to verify is that, we have satisfying assignments for both values true/false of the universal variables \(u_i\).

If the \(\text{assume (t_{u_n} = 0)}\) evaluates to true in \(c_{SATC}\) then in the view of the message \((s, 1, vw)\) obtained at the end of \(c_{AG}\), \(vw(t_{u_n}) = 0\). We now need a \(c_{AG}\) function (executed by some thread) to make an assignment such that in the view of the message \((s, 1, vw)\), we have \(vw(f_{u_n}) = 0\), and the formula \(\Phi\) is satisfiable again. The next step is to check if these assignments which differ in \(u_n\) are sound with respect to the \(\forall u_{n-1} \exists c_n\) part of \(\Psi\) : that is, the assignment to \(c_n\) is independent to that of \(u_n\). This procedure has to be iterated with respect to all of \(u_0, u_1, \ldots, u_{n-1}\) by (1) first ensuring that \(\Phi\) is satisfiable for both assignments to \(u_i\), \(0 \leq i \leq n - 1\) and (2) verifying that such assignments are sound with respect to the quantifier alternation in \(\Psi\) for \(1 \leq i \leq n - 1\), (that is the choice of assignment to \(c_i\) is independent of all variables in \(\{u_i, e_{i+1}, \ldots, u_n\}\)).

**ForallExists Checker**: \(c_{FE[\_]}: The n \forall \exists Checkers c_{FE[0]}, \ldots, c_{FE[n-1]}\) take over at this point, consuming the writes made earlier. In general, for each \(i \in \{0, \ldots, n-1\}\), we have \(\forall \exists Checker\) function of \(n\) kinds, \(c_{FE[0]}, \ldots, c_{FE[n-1]}\) that operate at levels \(0, \ldots, n-1\). \(c_{FE[i]}\) operates at level \(i\) by reading 1 from \(a_{i+1,0}, a_{i+1,1}\) variables, and making writes to \(a_{i,0}, a_{i,1}\) variables for \(0 \leq i \leq n-1\).

**Universality Check**: \(c_{FE[i]}\) first verifies that all possible valuations to the universally quantified variable \(u_{i+1}\) made \(\Phi\) satisfiable : the two statements \(\text{assume (a_{i+1,0} = 1); assume (a_{i+1,1} = 1)}\) verify this by reading 1 from \(a_{i+1,0}\) and \(a_{i+1,1}\) (note how all higher \(c_{FE[j]}: j > i\) level functions enforce this by generating a dependency tree such as the one in Figure 14).

**Existentiality Check**: Next, \(c_{FE[i]}\) checks that the satisfying assignments of \(\Phi\) seen so far agree on the existentially quantified variable \(e_{i+1}\) : the statements \((\text{assume (f_{e_{i+1}} = 0)} \oplus \text{assume (t_{e_{i+1}} = 0)})\) check this. Assume that we have satisfying assignments of \(\Phi\) which do not agree on \(e_{i+1}\). Then we have messages \((a_{i+1,0,1}, vw_1)\) and \((a_{i+1,1,1}, vw_2)\) such that \(vw_1(t_{e_{i+1}}) > 0 (e_{i+1} \text{ assigned false})\) but \(vw_2(t_{e_{i+1}}) = 0 (e_{i+1} \text{ assigned true})\). Now when \(c_{FE[i]}\) reads from these messages, its view \(vw\), will have both, \(vw(t_{e_{i+1}}) > 0\) and \(vw(f_{e_{i+1}}) > 0\). This will disallow \(c_{FE[i]}\) from executing \((\text{assume (f_{e_{i+1}} = 0)} \oplus \text{assume (t_{e_{i+1}} = 0)})\) since the messages in the memory where \(t_{e_{i+1}}\) and \(f_{e_{i+1}}\) have value 0 (and time stamp 0) cannot be read. This enforces that the choice of the existentially quantified variable \(e_{i+1}\) is independent of the choice of the assignments made to the variables in \(\{u_{i+1}, e_{i+2}, \ldots, u_n\}\), and hence the proper semantics of quantifier alternation is maintained.

**Propagation** Finally, the \(c_{FE[i]}\) function ‘propagates’ assignments to the next level, that
is, to \( c_{FE[i-1]} \) after a last verification. Let \( A_{i+1,j} \) contain all assignments satisfying \( \Phi \) which agree on \( e_{i+1} \), and where \( u_{i} \) is assigned value \( j \in \{0,1\} \). Such assignments are propagated to the next level by a \( c_{FE[i]} \) function which writes 1 to \( a_{i,j} \). \( c_{FE[i-1]} \) is accessible only when \( A_{i+1,0} \) and \( A_{i+1,1} \) are both propagated.

![Figure 14](image)

The dependency tree for the case of \( \forall u_{0} \exists e_{1} \forall u_{1} \exists e_{2} \forall u_{2} \Phi \). The same color of sibling nodes \( c_{FE[i]} \) represents that the value of \( e_{i+1} \) is same at both of these.

**Assert Checker:** \( c_{assert} \): After the \( n \) 3-Checkers finish, the Assertion Checker reads 1 from the variables \( a_{0,0} \) and \( a_{0,1} \) and reaches the assertion \texttt{assert false}. This is possible only if all the earlier functions act as intended, which in turn is only possible if the QBF evaluates to true.

### 7.3.2 Roles played by the threads

The non-deterministic branching between the choices of the gadgets above means that each \texttt{env} thread executes exactly one of the gadgets. However together they check \( \Psi \) in a distributed fashion as one thread passing on a part of its state to the next one by the load-stores for the \( a_{n,0/1} \) variables as mentioned above. Hence a computation that reaches the assertion requires each thread to play a part in this tableau. We now describe this.

First a set of \( 2^{n} \) threads run the \( c_{AG} \) gadgets and they guess one assignment each such that all possible assignments for the universally quantified variables are covered and such that the existentially quantified variables are chosen such that the semantics of quantifier alternation is respected. Essentially this means the the \( 2^{n} \) assignments guessed would be a sufficient witness to the truth of \( \Psi \).

Now, \( 2^{n} \) threads execute \( c_{SATC} \) and check that each of the assignments guessed (one thread checks one assignment) satisfies \( \Phi \). They produce a ‘proof’ that this check is complete by writing to variables \( a_{n,0/1} \). This also checks the innermost universality is respected. At level \( n-1 \), \( 2^{n-1} \) threads execute \( c_{FE[n-1]} \). Each \( c_{FE[n-1]} \) reads 1 from both \( a_{n,0} \) and \( a_{n,1} \) and reads 0 from exactly one of \( t_{e_{n}} \) or \( f_{e_{n}} \). Depending on the view read from the level below, they either write 1 to \( a_{n-1,0} \) or to \( a_{n-1,1} \). (Prematurely this corresponds to the assignments \( A_{n,0} \) and \( A_{n,1} \) in the proof below.) In essence these threads check that the last quantifier alternation (\( \forall u_{n-1} \exists e_{n} \)) is respected. \( 2^{n-2} \) threads then execute \( c_{FE[n-2]} \) at level \( n-2 \), reading 1 from both \( a_{n-1,1} \) and \( a_{n-1,0} \), and reading 0 from exactly one of \( t_{e_{n-1}} \) or \( f_{e_{n-1}} \). These threads then write 1 to either \( a_{n-2,0} \) or to \( a_{n-2,1} \), (representing assignments \( A_{n-1,0} \) and \( A_{n-1,1} \) in the proof below). These threads check that the second last quantifier alternation \( \forall u_{n-1} \exists e_{n-1} \) is respected. This continues till two threads execute \( c_{FE[0]} \), and writes 1 to \( a_{0,1} \) or \( a_{0,0} \). These two writes are read by a thread executing \( c_{assert} \). The views of these threads are all stitched together by the stores and loads they perform on the variables \( s \) (for guessing assignments) and \( a_{n,0/1} \) for checking proper alternation. Figure 14 illustrates how the view (in which the assignments are embedded as described earlier) propagate through these threads for the case of the QBF \( \forall u_{0} \exists e_{1} \forall u_{1} \exists e_{2} \forall u_{2} \Phi \). The nodes represent individual
threads executing the corresponding gadget and the edges represent the variable which a child writes to pass on its view to its parent.

- **Lemma 19.** $\Psi$ is true iff the assert `false` statement is reachable in $c$.

This gives us the main theorem

- **Theorem 20.** The verification of safety properties for parametrized systems of the class $\text{env}(\text{nocs}, \text{acyc})$ under RA is $\text{PSPACE}$-hard.

### 7.4 Correctness of the Construction: Proof of Lemma 19

We prove that reaching `assert false` is possible in the parameterized system $c$ iff the QBF $\Psi$ is satisfiable. First we fix some notations. Given the QBF $\Psi = \forall u \exists e_1 \ldots \exists e_n \forall u \Phi(u_0, e_1, \ldots, u_n)$, we define for $0 \leq i \leq n$, the level $i$ QBF corresponding to $\Psi$ as follows.

1. For $0 \leq i \leq n - 1$, the level $i$ QBF, denoted $\Psi_i$ is defined as
   $$\Psi_i \equiv \forall u_i \exists e_{i+1} \forall u_{i+1} \exists e_{i+2} \ldots \forall u_n \exists e_1 \exists e_2 \ldots \exists e_i \exists u_0 \exists u_1 \ldots \exists u_{i-1} \Phi(u_0, e_1, \ldots, u_n)$$

2. For $i = n$, the level $n$ QBF, denoted $\Psi_n$ is defined as
   $$\Psi_n \equiv \forall u_n \exists e_1 \ldots \exists e_n \exists u_0 \exists u_1 \ldots \exists u_{n-1} \Phi(u_0, e_1, \ldots, u_n)$$

Note that $\Psi_0$ is the same as $\Psi$. To prove Lemma 19, we prove the following helper lemmas.

**Lemma 20.** $\Psi_n$ is true iff we reach the label $\lambda_1$ of the $c_{\text{SAT}}$ gadget (ref. Figure 16) in some thread, and the label $\lambda_2$ of the $c_{\text{SAT}}$ gadget in some thread.

**Lemma 21.** For $0 \leq i \leq n - 1$, $\Psi_i$ is satisfiable iff we reach the label $\lambda_3$ in the $c_{\text{FE}[i]}$ gadget (ref. Figure 17) in some thread, and the label $\lambda_4$ in the $c_{\text{FE}[i]}$ gadget in some thread.

**Lemma 22.** `assert false` is reachable iff we reach the label $\lambda_3$ in the $c_{\text{FE}[0]}$ gadget in some thread, and the label $\lambda_4$ in the $c_{\text{FE}[0]}$ gadget in some thread.

In the following, we write $\Phi$ for $\Phi(u_0, e_1, \ldots, e_n, u_n)$ since the free variables of $\Phi$ are clear.

**Proof of Lemma 21**

Assume $\Psi_n$ is satisfiable. Then there are satisfying assignments $\alpha_1$ and $\alpha_2$ s.t. $\alpha_1(u_n) = 0$, $\alpha_2(u_n) = 1$, such that $\alpha_1, \alpha_2 \models \Phi$. These assignments $\alpha_1, \alpha_2$ can be guessed by $c_{\text{AG}}$ gadgets in two threads, resulting in adding messages $(s, 1, \text{view}_1)$ and $(s, 1, \text{view}_2)$ to the memory, such that $\text{view}_1(f_{\alpha_1}) = 0$ and $\text{view}_2(f_{\alpha_2}) = 0$. Correspondingly, there are $c_{\text{SAT}}$ gadgets which read from these views, (they read 1 from $s$), and check for the satisfiability of $\Phi$ using the $\text{view}_1, \text{view}_2$ values of $t_x, f_x$ for $x \in \text{Vars}(\Psi)$. Since both are satisfying assignments, the
\[ c_{\text{SATC}} = \text{assume } (s = 1); \text{check}(\Phi); \lambda_0 : \text{skip}; \]
\[ \vdash (\text{assume } (t_{u_n} = 0); a_{n,1} := 1; \lambda_1 : \text{skip} ;) \]
\[ (\text{assume } (f_{u_n} = 0); a_{n,0} := 1; \lambda_2 : \text{skip} ;) \]\n
\[ \text{Figure 16} \] Implementation of the SAT Checker \( c_{\text{SATC}} \) gadget with labels \( \lambda_0, \lambda_1, \lambda_2 \)

Label \( \lambda_0 \) is reachable in both \( c_{\text{SATC}} \) gadgets. One of them will reach the label \( \lambda_1 \) reading \( t_{u_n} = 0 \) (using \( \text{view}_2 \)) and the other will reach the label \( \lambda_2 \) reading \( f_{u_n} = 0 \) (using \( \text{view}_1 \)).

Conversely, assume that the label \( \lambda_1 \) of \( c_{\text{SATC}} \) is reachable in one thread, while the label \( \lambda_2 \) of \( c_{\text{SATC}} \) is reachable in another thread. Then we know that in one thread, we have read a message \((s, 1, \text{view}_1)\), checked for the satisfiability of \( \Phi \) using \( \text{view}_1 \), and also verified that \( \text{view}_1(t_{u_n}) = 0 \), while in another thread, we have read a message \((s, 1, \text{view}_2)\), checked for the satisfiability of \( \Phi \) using \( \text{view}_2 \), and also verified that \( \text{view}_2(f_{u_n}) = 0 \). Thus, we have 2 satisfying assignments to \( \Phi \), one where \( u_n \) has been assigned to 0, and the other, where \( u_n \) has been assigned 1. Hence \( \Psi_n \) is satisfiable.

\[ \text{Definition 24.} \] Let \( \text{view} \) be a view. We say that an assignment \( \alpha : \text{Vars}(\Psi) \rightarrow \{0, 1\} \) is embedded in \( \text{view} \) iff for all \( x \in \text{Vars}(\Psi) \), \( \text{view}(t_x) = 0 \Leftrightarrow \alpha(x) = 1 \) and \( \text{view}(f_x) = 0 \Leftrightarrow \alpha(x) = 0 \). The term “embedded” is used since the view also has (program) variables outside of \( t_x \) and \( f_x \).

For \( 0 \leq i \leq n \), let \( A_i \) and \( B_i \) respectively represent the set of assignments which are embedded in the views reaching the labels \( \lambda_3, \lambda_4 \) of the \( c_{\text{FE}[i]} \) gadget. Thus, we know that
\[ A_n = \{ \alpha \models \Phi \mid \alpha(u_n) = 1 \} \] and \( B_n = \{ \alpha \models \Phi \mid \alpha(u_n) = 0 \} \)

\[ \text{Figure 17} \] \( \forall \exists \) Checker at level \( i \), \( c_{\text{FE}[i]} \), with labels \( \kappa_1, \kappa_2, \lambda_3, \lambda_4 \). We have \( n \) such gadgets, one for each level \( 0 \leq i \leq n - 1 \).

\[ \text{Lemma 25.} \] For \( 0 \leq i \leq n - 1 \), define sets of assignments
\[ A_{i,0} = \{ \alpha \in A_{i+1} \uplus B_{i+1} \mid \alpha(u_i) = 1, \alpha(e_{i+1}) = 0 \} \]
\[ A_{i,1} = \{ \alpha \in A_{i+1} \uplus B_{i+1} \mid \alpha(u_i) = 1, \alpha(e_{i+1}) = 1 \} \]
\[ B_{i,0} = \{ \alpha \in A_{i+1} \uplus B_{i+1} \mid \alpha(u_i) = 0, \alpha(e_{i+1}) = 0 \} \]
\[ B_{i,1} = \{ \alpha \in A_{i+1} \uplus B_{i+1} \mid \alpha(u_i) = 0, \alpha(e_{i+1}) = 1 \} \]
where \( \uplus \) denotes disjoint union. Then \( A_i \) is equal to one of the sets \( A_{i,1} \) or \( A_{i,0} \). Similarly, \( B_i \) is equal to one of the sets \( B_{i,1} \) or \( B_{i,0} \).
Proof of Lemma 25. We already know the definitions of $A_n$ and $B_n$. Consider the case of $A_{n-1}$ and $B_{n-1}$. By construction, to reach label $\lambda_3$ of $c_{FE}[n-1]$, 

(a) we need to have reached labels $\lambda_3, \lambda_4$ of $c_{FE}[n]$. The view (say $view_A$) on reaching the label $\kappa_1$ in $c_{FE}[n-1]$ has embedded assignments from $A_n \cup B_n$.

(b) To reach the label $\kappa_2$ of $c_{FE}[n-1]$, we need either $f_{e_n}$ to have time stamp 0 or $t_{e_n}$ to have time stamp 0 in $view_A$. If we had $view_A(t_{e_n}) > 0$ and $view_A(f_{e_n}) > 0$, then the label $\kappa_2$ is not reachable. That is, the assignments embedded in $view_A$ agree on the assignment of $e_n$.

(c) To reach the label $\lambda_3$ in $c_{FE}[n-1]$, the assignments embedded in $view_A$ agree on the assignment of $u_{n-1}$, such that $u_{n-1}$ is assigned 1. Thus, $A_{n-1}$ is obtained from $A_n \cup B_n$ by keeping those assignments which agree on $e_n$ and where $u_{n-1}$ is true.

Similarly, to reach label $\lambda_4$ in $c_{FE}[n-1]$, 

(a) we need to have reached the labels $\lambda_3, \lambda_4$ of $c_{FE}[n]$. The view (say $view_B$) on reaching the label $\kappa_1$ in $c_{FE}[n-1]$ has embedded assignments from $A_n \cup B_n$.

(b) To reach label $\kappa_2$, we need either $f_{e_n}$ to have time stamp 0 or $t_{e_n}$ to have time stamp 0 in $view_B$. If we had $view_B(t_{e_n}) > 0$ and $view_B(f_{e_n}) > 0$, then the label $\kappa_2$ is not reachable. That is, the assignments embedded in $view_B$ agree on the assignment of $e_n$.

(c) To reach the label $\lambda_4$ in $c_{FE}[n-1]$, the assignments embedded in $view_B$ agree on the assignment of $u_{n-1}$, such that $u_{n-1}$ is assigned 0. Thus, $B_{n-1}$ is obtained from $A_n \cup B_n$ by keeping those assignments which agree on $e_n$ and where $u_{n-1}$ is false.

The proof easily follows for any $A_i, B_i$, using the definitions of $A_{i+1}, B_{i+1}$ as above. ▶

Proof of Lemma 22.

We give an inductive proof for this, using Lemma 21 as the base case. As the inductive step, assume that $\Psi_{i+1}$ is satisfiable if we reach the label $\lambda_3$ of the $c_{FE}[i+1]$ gadget in some thread, and the label $\lambda_4$ of the $c_{FE}[i+1]$ gadget in some thread.

Assume $\Psi_i$ is satisfiable. We can write $\Psi_i$ as $\forall u_i \exists e_{i+1} \Psi_{i+1}$. We show that there is a thread which reaches label $\lambda_3$ of the $c_{FE}[i+1]$ gadget with a view that has $A_i$ embedded in it, and there is a thread which reaches the label $\lambda_4$ of the $c_{FE}[i]$ gadget with a view that has $B_i$ embedded in it.

By inductive hypothesis, since $\Psi_{i+1}$ is satisfiable, there is a thread which reaches the label $\lambda_3$ of the $c_{FE}[i+1]$ gadget with a view $view_A$ that has $A_{i+1}$ embedded in it, and there is a thread which reaches label $\lambda_4$ of the $c_{FE}[i+1]$ gadget with a view $view_B$ that has $B_{i+1}$ embedded in it. Note that $a_{i+1,1}, a_{i+1,0}$ have been written 1 by these threads respectively, such that $view_A(a_{i+1,1}) > 0$ and $view_B(a_{i+1,0}) > 0$. Thanks to this, there is a thread which can take on the role of the $c_{FE}[i]$ gadget now. This thread begins with a view $view_C$ which is the merge of $view_B$ and $view_A$. The label $\kappa_1$ of this $c_{FE}[i]$ gadget is reachable by reading 1 from both $a_{i+1,1}$ and $a_{i+1,0}$, and we want $view_C(t_{e_{i+1}}) = 0$ or $view_C(f_{e_{i+1}}) = 0$. As seen in item (b) in the proof of observation 25, this is possible only if $view_B(t_{e_{i+1}}) = 0$ and $view_B(f_{e_{i+1}}) = 0$.

By assumption, since $\Psi_i$ is satisfiable, there exists assignments from $A_{i+1}$ and $B_{i+1}$ which agree on $e_{i+1}$ and $u_i$. In particular, the satisfiability of $\Psi_i = \forall u_i \exists e_{i+1} \Psi_{i+1}$ says that we have a set of assignments $S \subseteq A_{i+1} \cup B_{i+1}$ which satisfy $\Psi_i$, such that for all $\alpha \in S$, $\alpha(u_i) = 1$ and $\alpha(e_{i+1})$ is some fixed value. Similarly, the satisfiability of $\Psi_i$ also gives us a set of assignments $S' \subseteq A_{i+1} \cup B_{i+1}$ such that for all $\alpha \in S'$, $\alpha(u_i) = 0$ and $\alpha(e_{i+1})$ is some fixed.
value. It is easy to see that \( S = A_i \), while \( S' = B_i \). Thus, the satisfiability of \( \Psi_i \) implies the feasibility of the assignments \( A_i \) and \( B_i \). This in turn, gives us the following.

Thus, starting with a view \( \text{view}_C \) which has embedded assignments \( A_{i+1} \uplus B_{i+1} \), it is possible for a thread to

1. read 1 from \( a_{i+1,1} \) and \( a_{i+1,0} \) (these are present in the \( \text{view}_C \)),
2. Check that either \( t_{e_i+1} \) has time stamp 0 in \( \text{view}_C \) or \( f_{e_i+1} \) has time stamp 0 in \( \text{view}_C \) (this is possible since the embedded assignments agree on \( e_{i+1} \)),
3. Check that \( t_u \) has time stamp 0 in \( \text{view}_C \) (this is possible since the embedded assignments are such that \( u_i \) is assigned 1)

This ensures that the thread reaches the label \( \lambda_3 \) of \( \text{cFE}[i] \) with a view having \( A_i \) embedded in it (notice that the last two checks filter out \( A_i \) from \( A_{i+1} \uplus B_{i+1} \)).

In a similar manner, starting with a view \( \text{view}_C \) which has embedded assignments \( A_{i+1} \uplus B_{i+1} \), it is possible for a thread to

1. read 1 from \( a_{i+1,1} \) and \( a_{i+1,0} \) (these are present in the \( \text{view}_C \)),
2. Check that either \( t_{e_i+1} \) has time stamp 0 in \( \text{view}_C \) or \( f_{e_i+1} \) has time stamp 0 in \( \text{view}_C \) (this is possible since the embedded assignments agree on \( e_{i+1} \)),
3. Check that \( f_u \) has time stamp 0 in \( \text{view}_C \) (this is possible since the embedded assignments are such that \( u_i \) is assigned 0)

This ensures that the thread reaches the label \( \lambda_4 \) of \( \text{cFE}[i] \) with a view having \( B_i \) embedded in it (notice that the last two checks filter out \( B_i \) from \( A_{i+1} \uplus B_{i+1} \)).

Conversely, assume that we have two threads which have reached respectively, labels \( \lambda_3 \) and \( \lambda_4 \) of \( \text{cFE}[i] \) gadget having views in which \( B_i \) and \( A_i \) are embedded. We show that \( \Psi_i \) is satisfiable.

By the definition of \( A_i \), we know that we have assignments from \( A_{i+1} \uplus B_{i+1} \) which agree on \( e_{i+1} \), and which set \( u_i \) to 1. The fact that we reached the label \( \lambda_3 \) of \( \text{cFE}[i] \) gadget with a view having \( A_i \) embedded in it shows that these assignments are feasible. Similarly, reaching the label \( \lambda_4 \) of \( \text{cFE}[i] \) with a view having \( B_i \) embedded in it shows that we have assignments from \( A_{i+1} \uplus B_{i+1} \) which agree on \( e_{i+1} \), and which set \( u_i \) to 0. The existence of these two assignments proves the satisfiability of \( \Psi_i \).

**Proof of Lemma 23**

Assume that we reach \texttt{assert false}. Then we have read 1 from \( a_{0,0} \) and \( a_{0,1} \). These are set to 1 only when the labels \( \lambda_4 \), \( \lambda_3 \) of \( \text{cFE}[0] \) have been visited. The converse is exactly similar: indeed if we reach the labels \( \lambda_4 \), \( \lambda_3 \) of \( \text{cFE}[0] \), we have written 1 to \( a_{0,0} \) and \( a_{0,1} \). This enables the reads of 1 from \( a_{0,0} \) and \( a_{0,1} \) leading to \texttt{assert false}.

▶ **Theorem 26.** Parameterized safety verification for \( \text{env}(\text{noca}, \text{acyc}) \) is \( \text{PSPACE}-\text{hard} \).

### 8 Limits of Semantic Simplification II: \( \text{NEXPTIME-} \text{hardness of} \)

\[ \text{env}(\text{noca}, \text{acyc}) \parallel \text{dis}_1(\text{noca}) \]

In this section we show an \( \text{NEXPTIME} \) lower bound on the safety verification problem in the presence of a single leader \( \text{dis} \) thread, \( \text{env}(\text{noca}, \text{acyc}) \parallel \text{dis}(\text{noca}) \). The lower bound is obtained with a fragment of RA which does not use registers and surprisingly in which \( \text{dis} \) also does not perform any compare-and-swap operations. As in the case of the \( \text{PSPACE}-\text{hardness}, \)
we work with a fixed set of shared memory locations $X$ (also called shared variables) from a finite data domain $D$. We show the hardness via a reduction from the succinct version of 3CNF-SAT, denoted SuccinctSAT. Following the main part of the paper, we refer to the distinguished dis thread as the ‘leader’ and individual threads from env as ‘contributors’.

8.1 SuccinctSAT: succinct satisfiability

The complexity of succinct representations was studied in the pioneering work [37] for graph problems. Typically, the complexity of a problem is measured as a function of some quantity $V$, with the assumption that the input size is polynomial in $V$. If the underlying problem concerns graphs, then $V$ is the number of vertices in the graph, while if the underlying problem concerns boolean formulae, then $V$ is the size of the formula. [37] investigated the complexity of graph problems, when the input has an exponentially succinct representation, that is, the input size is polylog in $|V|$, where $V$ is the number of vertices of the graph, and showed that succinct representations rendered trivial graph problems NP-complete, while [58] showed that graph properties which are NP-complete under the usual representation became NEXPTIME-complete under succinct representations. SuccinctSAT is essentially an exponentially succinct encoding of a 3CNF-SAT problem instance. Let $\phi(x_0, \cdots, x_{2^n-1})$ be a 3CNF formula with $2^n$ variables and $2^n$ clauses. Assume an $n$ bit binary address for each clause.

A succinct encoding of $\phi$ is a circuit $D(y_1, \cdots, y_n)$ (with size polynomial in $n$), which, on an $n$ bit input $y_1 \cdots y_n$, interpreted as a binary address for clause $c$, generates $3n + 3$ bits, specifying the indices of the 3 variables from $x_1, \cdots, x_{2^n}$ occurring in clause $c$ and their signs (1 bit each). Thus, the circuit $D$ provides a complete description of $\phi(x_1, \cdots, x_{2^n})$ when evaluated with all $n$-bit inputs. Define SuccinctSAT as the following NEXPTIME-complete [58] problem.

Given a succinct description $D$ of $\phi$, check whether $\phi$ is satisfiable.

Adopting the notation above, we assume that we have been given $n$, the formula $\phi$ with $2^n$ boolean variables $BVars = \{x_0, \cdots, x_{2^n-1}\}$, and the succinct representation $D$ with input variables $\{y_1, \cdots, y_n\}$. Denote the variables in clause $c$ as $var1(c), var2(c), var3(c)$ and their signs as $\text{sig1}(c), \text{sig2}(c), \text{sig3}(c)$. We denote the $n$-bit address $\bar{c}$ of a clause $c$ as a (boolean) word $\bar{c} \in \{0, 1\}^n$ and commonly use the variable $\alpha$ to refer to clause addresses. We denote the variable addresses also as $n$-bit (boolean) words and commonly use the the variable $\beta$ to represent them. We construct an instance of the parametrized reachability problem consisting of a ldr leader thread running program $c_{ldr}$ and the env contributor threads running program $c_{env}$. We show that this system is ‘unsafe’ (an assert false is reachable) if and only if the SuccinctSAT instance is satisfiable.

8.2 Key features

The leader running program $c_{ldr}$ guesses an assignment to the boolean variables in $\phi$. The contributors running the program $c_{env}$ will be tasked with checking that the assignment guessed by the leader does in fact satisfy the formula $\phi$. They do this in a distributed fashion, where one clause from $\phi$ is verified by one contributor. Then similar to the PSPACE-hardness proof, the program $c_{env}$ forces the contributors to combine checks for individual clauses as a dependency tree. This is so that the root of the tree is able to reach an assertion failure only if all threads could successfully check their clauses under the leader’s guessed assignment. However since all the contributors run the same program, the trick is to enforce that all clauses will be checked.
Safety Verification of Parameterized Systems under Release-Acquire

\[ \text{CL} = \text{choose}(u_0); \text{choose}(u_1); \ldots; \text{choose}(u_{n-1}); s := 1 \]

\[ \text{SAT} = (\text{assume } s = 1); \text{CV}; \text{Check}; \]

\[ ((\text{assume } t_{u_{n-1}} = 0); a_{n-1,1} := 1) \oplus (\text{assume } f_{u_{n-1}} = 0); a_{n-1,0} := 1) \]

\[ \text{assert} = (a_{0,0} = 1); \text{assume } (a_{0,1} = 1); \text{assert } \text{false} \]

\[ \text{Cassert} = (a_{0,0} = 1); \text{assume } (a_{0,1} = 1); \text{assert } \text{false} \]

\[ \text{C}_{\text{env}} = \text{C}_{\text{CL-ENC}} \oplus \text{C}_{\text{SAT}} \oplus \text{C}_{\text{Forall}[0]} \oplus \ldots \oplus \text{C}_{\text{Forall}[n-1]} \oplus \text{C}_{\text{assert}} \]

\[ \text{choose}(u) = (t_u := 1) \oplus (f_u := 1) \]

\[ \text{CL-ENC} = \text{choose}(u_0); \text{choose}(u_1); \ldots; \text{choose}(u_{n-1}); s := 1 \]

\[ \text{SAT} = (\text{assume } s = 1); \text{CV}; \text{Check}; \]

\[ ((\text{assume } t_{u_{n-1}} = 0); a_{n-1,1} := 1) \oplus (\text{assume } f_{u_{n-1}} = 0); a_{n-1,0} := 1) \]

\[ \text{assert} = (a_{0,0} = 1); \text{assume } (a_{0,1} = 1); \text{assert } \text{false} \]

\[ \text{C}_{\text{assert}} = (a_{0,0} = 1); \text{assume } (a_{0,1} = 1); \text{assert } \text{false} \]

\[ \text{Figure 18} \] The contributor program \( \text{c}_{\text{env}} \) used in the reduction. The sub-routines \( \text{C}_{\text{CV}} \) and \( \text{C}_{\text{Check}} \) are described later.

**Gadgets.** \( \text{c}_{\text{env}} \) consists of a set of gadgets (modelled as ‘functions’ in the program), only one of which may be non-deterministically executed by the contributors, while \( \text{C}_{\text{ldr}} \) is the program executed by the leader.

\[ \text{c}_{\text{env}} = \text{C}_{\text{CL-ENC}} \oplus \text{C}_{\text{SAT}} \oplus \text{C}_{\text{Forall}[0]} \oplus \ldots \oplus \text{C}_{\text{Forall}[n-1]} \oplus \text{C}_{\text{assert}} \]

Recall that in the PSPACE-hardness proof too, there were similar gadgets which were executed by the \( \text{env} \) threads. The gadgets in \( \text{c}_{\text{env}} \) do execute various tasks as follows.

\( \text{C}_{\text{CL-ENC}} \) guesses an \( n \) bit address \( \bar{c} \) of a clause \( c \) in \( \phi \),

\( \text{C}_{\text{SAT}} \) (1) acquires a clause address \( \bar{c} \) generated by \( \text{C}_{\text{CL-ENC}} \), (2) uses the circuit \( D \) to obtain the indices of variables \( \text{var}1c, \text{var}2c, \text{var}3c \) in clause \( c \), along with its sign (this is done by the sub-routine \( \text{C}_{\text{CV}} \)), (3) accesses the assignment made to the variables by the leader (sub-routine \( \text{C}_{\text{Check}} \)) and (4) the assignment is such that \( c \) is satisfied.

\( \text{C}_{\text{Forall}[i]} \) \( (0 \leq i \leq n - 2) \) together ensure that the satisfiability of all the clauses in \( \phi \) has been checked. This is done by instantiations of \( \text{C}_{\text{SAT}} \), in levels (similar to the proof of PSPACE-hardness). At the \( i \)th level, \( \text{C}_{\text{Forall}[i]} \) checks the \( \forall \) universality of the \( i \)th address bits of clause \( c \).

\( \text{C}_{\text{assert}} \) finally reaches \( \text{assert } \text{false} \), if all the previous functions execute faithfully, implying that the \text{SuccinctSAT} instance is satisfiable.

The non-deterministic branching implies that each \( \text{env} \) thread will only be able to execute one of these gadgets. The check for satisfiability of \( \phi \) is distributed between the \( \text{env} \) threads much like the PSPACE-hardness construction. For this distributed check, threads are allocated roles depending upon the function (gadget) they execute. Additionally, the distinguished leader thread is tasked with guessing the assignment. We now describe this.

**Role of the leader.** We have one leader thread which guesses a satisfying assignment for the boolean variables \( \text{BVars} \) as a string of writes made to a special program variable \( g \). The writes made to \( g \) have \( n+2 \) values \( d_1, d_2, 1, \ldots, n \) in a specific order. Let the initial values of all variables in the system be init \( \notin \{d_1, d_2, 1, \ldots, n\} \). To illustrate a concrete example, consider the case where \( n = 3 \). Let the guessed assignment for \( \text{BVars} \) be \( w = \text{ftfttttt} \in \{t,f\}^2^7 \), where \( t \) denotes true and \( f \) false. Then the writes made by the leader are as below, where \( d_t \) and \( d_f \) are macros for data domain values (other than \( \{\text{init}, 1, \ldots, n\} \)) representing true and false respectively.

\[ d_t \ 1 \ d_t \ 2 \ d_t \ 1 \ d_t \ 3 \ d_t \ 1 \ d_t \ 2 \ d_t \ 1 \ d_t \]
The leader alternates writing a guessed assignment for $x_0, \ldots, x_7$ (in red) with writing a value from $\{1, \ldots, n\}$ (in blue). The values in $\{1, \ldots, n\}$ (here $\{1, 2, 3\}$) in blue are written in a deterministic pattern as $1 2 1 3 1 2 1$, which we call a ‘binary search pattern’ with 3 values, denoted $BSP(3)$ for short. $BSP(n)$ is a unique word of length $2^n - 1$ over $\{1, \ldots, n\}$, defined inductively as follows.

\[
\begin{align*}
BSP(1) &= 1 \\
BSP(n) &= BSP(n - 1) \cdot n \cdot BSP(n - 1) \quad \text{for } n \geq 2
\end{align*}
\]

The assignments for $x_0, \ldots, x_{2^n-1}$ are interspersed alternately with symbols in $BSP(n)$ by the leader while writing to $g$. Formally, let $S(n, w) = BSP(n) \cup w$ represent the perfect shuffle (alternation) of $BSP(n)$ with the guessed assignment $w \in \{d_1, d_2\}^{2^n}$. The leader writes the word $S(n, w)$ to $g$. From the example above, $S(3, ftftttttf) = d_1 1 d_2 1 d_1 3 d_1 1 d_2 1 d_1 2 d_1 1 d_2$. We show that the shuffle sequence which need to be generated is easily implementable by the leader with a polysize program.

**Lemma 27.** There exists a program $c_{dr}$, which nondeterministically chooses $w \in \{d_1, d_2\}^{2^n}$ and generates the write sequence $S(n, w)$ on a shared memory location $g$, with the size of the program growing polynomially with $n$.

**How contributors access variable assignments, intuitively.**

Each contributor wants to check a single clause for which it needs to access the 3 variables and their signs occurring in that clause. Since it pertains to the BSP, we first understand this task and discuss the others (selecting clause, acquiring variable address and sign, etc.) later. For now we assume that the contributor has a variable $x$ with address $\beta$ and sign $\sigma$ wants to access the assignment made to variable $x$ by the leader.

For boolean variable $x$, the contributor uses the $BSP(n)$ pattern to locate the assignment made to $x$, by reading a subword of $S(n, w)$. From program variable $g$, the contributor reads $n + 1$ values $\{d_1, 1, \ldots, n\}$ or $\{d_1, 1, \ldots, n\}$ without repetitions, depending upon the sign of $x$ in the clause ($d_1$ if sign is negative, $d_2$ if positive). In the running example, if contributor wants to access $x_2$ from $d_2 1 d_1 2 d_2 1 d_1 3 d_1 1 d_2 2 d_2 1 d_1$, it reads the sequence $2 d_2 1 3$. Likewise, the value of $x_0$ is obtained by reading $3 2 d_1 1$, while for $x_0$, the contributor must read $d_2 1 2 3$. We note that for each $x \in BVars$, there is a unique ‘access pattern’, which forces the thread to acquire the assignment of exactly $x$ and not any other variable. In this search, it is guided by the BSP, which acts as an indexing mechanism. It helps the contributor narrow down unambiguously, to the part which contains the value of $x$.

### 8.2.1 Formal description of contributors

The contributors check that each clause in $\phi$ has been satisfied in a distributed fashion. Each contributor executes one of the functions in $c_{env}$. They do this as follows.

**Clause Encoding:** $c_{CL-ENC}$: A thread executing $c_{CL-ENC}$ selects, nondeterministically, a clause address $\alpha \in \{0, 1\}^n$. This is done by writing 1 to either $t_u$, or $f_u$, for all $0 \leq i \leq n - 1$. Finally, 1 is written into a special variable $s$. The function $c_{CL-ENC}$ in Figure 18 describes this. The view of the message $(s, 1, vw)$ encodes the address $\alpha$ of a clause satisfying

\[(vw(t_u)) > 0 \iff \alpha[i] = 0 \quad \text{and} \quad (vw(f_u)) > 0 \iff \alpha[i] = 1 \quad \text{for} \quad 0 \leq i \leq n - 1\]

Recall that this is the same encoding technique as used for the PSPACE-hardness proof. Each bit is encoded in the view of a message. Overall $2^n$ threads will execute $c_{CL-ENC}$ to cover all the clauses in the formula.
Satisfaction checking (for one clause): \( c_{\text{SAT}} \): A thread executing \( c_{\text{SAT}} \) acquires the address \( \bar{c} \) of a clause \( c \) through the view \( \text{vw} \) by reading the message \( (s, 1, \text{vw}) \) generated by \( c_{\text{CL-ENC}} \). This thread has to check the satisfiability of the clause with address \( \bar{c} \). For this, it needs to know the 3 boolean variables \( \text{var}_1(c), \text{var}_2(c), \text{var}_3(c) \) appearing in \( c \). Recall that we have been given, as part of the problem, the circuit \( D \) which takes an \( n \) bit address \( \alpha \) corresponding to some clause as input, and outputs the \( 3n + 3 \) bits corresponding to the 3 variables appearing in the clause, along with their signs. We use \( D \), and the encoding of a clause address \( c \) stored in \( \text{vw} \), to compute \( D(\alpha) \). We have a polysize sub-routine \( c_{\text{CV}} \) (CV for circuit value) that can compute the circuit value of \( D \).

Circuit Value: \( c_{\text{CV}} \): The \( c_{\text{CV}} \) sub-routine takes the address \( \alpha \) (of a clause \( c \)) and converts it into the index of one of the variables in \( c \). Thus in essence, \( c_{\text{CV}} \) evaluates the circuit-value problem \( D(\alpha) \) by simulating the (polynomially-many) gates in \( D \). The idea is to keep two boolean program variables for each node in \( D \), and propagate the evaluation of nodes in an obvious way (for instance, if we have \( \land \) gate with input gates \( g_1, g_2 \) evaluating to 0, and 1 respectively, then \( t_\alpha \) will be written 1). We now briefly explain how circuit value can be evaluated, by taking an example of a single gate.

For each node \( p \) in \( D \) we use two boolean program variables, \( t_p \) and \( f_p \). We say that a view \( \text{vw} \) encodes the value at node \( p \) if the following holds. We write \( \text{encAddr}(\text{vw}) \) to denote the value the view values for boolean variables encoded in \( \text{vw} \).

\[
(\text{vw}(t_p) > 0 \iff p = 0) \text{ and } (\text{vw}(f_p) > 0 \iff p = 1)
\]

Now assume a thread has a view \( \text{vw}_1 \) when it wants to evaluate a logic (NAND) gate \( G \), with output node \( o \) and input nodes \( i_1 \) and \( i_2 \). We assume \( \text{vw}_1 \) must encode the values of \( i_1 \) and \( i_2 \) (the thread has evaluated inputs of \( G \)) and the thread must not have evaluated \( G \) before (we have that \( \text{vw}_1(t_o) = \text{vw}_1(f_o) = 0 \)). Assuming that these conditions hold, the thread executes instructions such that the new view \( \text{vw}_2 \) of the thread (1) differs from \( \text{vw}_1 \) only on \( t_o \) and \( f_o \) and (2) \( \text{vw}_2 \) correctly encodes value of \( o \). The function in Figure 19 evaluates \( G \). The main observation is that a thread can read init from a variable only if its view on that variable is 0 (since there is only one init message with timestamp 0). Claim (1) holds trivially since only timestamps of only \( t_o \) or \( f_o \) may be augmented (reading from init will not change timestamp). By a little observation we see that the thread can write to \( f_o \) if one of \( f_{i_1(1,2)} \) have timestamp 0, implying that one of the inputs to the gate is 0 by the assumption. Then it checks out that the new view on \( f_o \) is greater than 0, thus claim (2) holds. The case for \( t_o \) may be checked similarly. Since \( D \) has polynomially many gates, any thread can evaluate them in topological order, and hence eventually will end up with the evaluation of \( D(\alpha) \). Also note that since the thread relied on its internal view, the same set of program variables \( \{t_p, f_p | p \in G \} \) may be used by all threads (hence crucially avoiding the number of variables to vary with the thread count).
Lemma 28. There exists a sub-routine $c_{CV}$ that starting with the view $vw$ from $(s, 1, vw)$, evaluates the circuit value $D(\alpha)$, where $\alpha$ is the clause address encoded in the variables $t_{ui}$ and $f_{ui}$ in $\text{encAddr}(vw)$. Also, $c_{CV}$ is polysized in $n$.

Once $D(\alpha)$ has been computed, the thread can nondeterministically choose one of the three variables appearing in clause $c$, say $x \in \{\text{var1}(c), \text{var2}(c), \text{var3}(c)\}$. For simplicity we include this as a part of the routine $c_{CV}$ itself. The address $\beta$ of the variable $x$, the contributor accesses the assignment made by the leader to $x$ and checks if it satisfies clause $c$. This is done by the routine $c_{Check}$.

Clause Check: $c_{Check}$: Having acquired the address $\beta = \beta_{n-1}, \ldots, \beta_0$ and sign $\sigma$ of variable $x$, by executing $c_{CV}$, the thread checks that variable $x$ satisfies clause $c$. To faithfully access the assignment to $x$ from the variable $g$, the BSP guides the thread. The ‘access pattern’ for $x$ denoted by $AP(n)$ ($\beta, \sigma$ implicit) which is recursively defined as

$$\begin{align*}
    \text{for } 0 < i \leq n & \quad AP(i) = \begin{cases} 
    i \cdot AP(i-1) & \text{if } \beta_{i-1} = 1 \\
    AP(i-1) \cdot i & \text{if } \beta_{i-1} = 0 
    \end{cases} \\
    \text{for checking satisfiability } AP(0) & = \begin{cases} 
    d_1 & \text{if } \sigma = 0 \\
    d_2 & \text{if } \sigma = 1 
    \end{cases}
\end{align*}$$

For example if $x_6$, with negative sign ($\sigma = 0$), was to be accessed, then the access pattern would be $AP(3) = 3 \cdot AP(2) = 3 \cdot 2 \cdot AP(1) = 3 \cdot 2 \cdot AP(0) = 3 \cdot 2 \cdot d_1 = d_1$; likewise, for $x_4$, with negative sign ($\sigma = 0$), the access pattern would be $AP(3) = 3 \cdot AP(2) = 3 \cdot 2 \cdot AP(1) = 3 \cdot 2 \cdot d_1 = d_1$.

Going back to our example, if $d_2, d_1, 2, d_2, 1, d_2, 2 d_1, 1 d_2$ was written to $g$ by the leader, it is easy to see that the reads with access pattern for $x_6 (3 \cdot 2 \cdot d_1)$ would be successful, since $x_6$ had been assigned to $\text{false}$ by the leader while that for $x_4 (3 \cdot 2 \cdot d_1 \cdot 2)$ would fail since it was assigned $\text{true}$ while the contributor wished to read $d_2$. $AP(0)$ is defined to ensure satisfiability of the clause, $AP(0) = d_1$ iff $f_{sign} = 0$ (the sign of the variable in the clause is negative) and $AP(0) = d_2$ if $t_{sign} = 0$ (the sign of the variable in the clause is positive).

The above recursive formulation gives us a poly-sized sub-routine which reads values matching the $AP$ sequence. We thus have the following lemma.

Lemma 29. There exists a sub-routine $c_{Check}$, which, starting with a view $vw$ encoding (in $t_{d_0}, f_{d_0}, \ldots, t_{d_{n-1}}, f_{d_{n-1}}$ and $t_{sign}, f_{sign}$) the address and sign of boolean variable $x$ in clause $c$, terminates only if $c$ is satisfied under the assignment to $x$ made by the leader.

Until now, a thread which reads a clause from $c_{CL-ENC}$ has checked its satisfiability with respect to the assignment guessed by the leader, using the $c_{SAT}$ module. However, to ensure satisfiability of $\phi$, this check must be done for all $2^n$ clauses. This is done in levels $0 \leq i \leq n - 2$ using $c_{Forall[i]}$, exactly as in the $\text{PSPACE}$-hardness proof. Finally, we reach $\text{assert false}$ reading 1 from both $a_{0,0}, a_{0,1}$. However, in this case we do not have to check for alternation, but only for the universality in the assignments.

Forall Checker: $c_{Forall[i]}$: The $c_{Forall[i]}$ gadget checks the ‘universality’ with respect to the second-last bit of the clause address, $c_{Forall[n-3]}$ gadget does this check with respect to the third-last bit, and so on, till $c_{Forall[0]}$ does this check for the first bit, ensuring that all clauses have been covered.

$2^n$ threads execute $c_{SAT}$, and write 1 to $a_{n-1,1}$ and $a_{n-1,0}$, depending on the last address bit of the clause it checks. Next, $2^{n-1}$ threads execute $c_{Forall[n-2]}$. A thread executing
54 Safety Verification of Parameterized Systems under Release-Acquire

\[ c_{\text{forall}[n-2]} \] reads 1 from both \( a_{n-1,0} \) and \( a_{n-1,1} \) representing two clauses whose last bits differ; this thread checks that the second last bits in these two clauses agree: it writes 1 to \( a_{n-2,0} \) (if the second last bit is 0) or to \( a_{n-2,1} \) (if the second last bit is 1). When \( 2^{n-1} \) threads finish executing \( c_{\text{forall}[n-2]} \), we have covered the second last bits across all clauses. This continues with \( 2^{n-2} \) threads executing \( c_{\text{forall}[n-3]} \). A thread executing \( c_{\text{forall}[n-3]} \) reads 1 from both \( a_{n-2,0} \) and \( a_{n-2,1} \) representing two clauses whose second last bits differ and checks that the third last bits in these two clauses agree. Finally, we have 2 threads executing \( c_{\text{forall}[0]} \), certifying the universality of the first address bit, writing 1 to \( a_{0,0} \) and \( a_{0,1} \).

**Assertion Checker:** \( c_{\text{assert}} \): The assertion checker gadget in Figure 18 reads 1 from \( a_{0,0}, a_{0,1} \). If this is successful, then we reach the **assert false.**

### 8.2.2 Compare and contrast with PSPACE-hardness proof

As is evident there are many things common between the two proofs. We now recapitulate the similarities and differences.

- In the PSPACE-h we wanted to check for truth of the QBF, hence guessing an assignment was not necessary. Here the leader is tasked with guessing an assignment to the boolean variables.
- In PSPACE-h we want to check for quantifier alternation in the boolean variables in \( \Psi \). Here we want to also check for universality of addresses, i.e. the fact that all clauses have been checked. This makes the \( c_{\text{forall}[\_]} \) gadget a bit simpler than its \( c_{\text{FE}[\_]} \) counterpart.
- In the PSPACE-h, the CNF formula, \( \phi \) was given in a simple form and hence all threads executing \( c_{\text{SAT}} \) checked the formula. Additionally, given the exponential size of the formula, the task is distributed between (exponentially) many threads. Here CNF formula also was in an encoded form, hence we had to devise the circuit value machinery to extract it from the succinct representation \( D \).

### 8.3 Correctness of the construction

The proof of this lemma is very close to that of Lemma 19. Some of the terminology we use in this proof is borrowed from the proof of Lemma 19. As in the case of section 7.4, we add some labels in the function descriptions for ease of argument in the proof. We describe the notations and key sub lemmas required for the proof.

**Notation and Interpretation of Boolean Variables involved in the construction**

- We denote by \( \alpha_U \), an assignment on the (boolean) variables \( \{u_0, u_1, \ldots, u_{n-1}\} \), interpreted as the (n-bit) address of a clause. Here \( u_{n-1} \) is the most significant bit (MSB) and \( u_0 \) as the least significant bit (LSB). We view the assignment so generated as \( \overline{\alpha_U} \in \{0,1\}^n \) as an n-bit vector. \( \alpha_U(u_i) \) gives the assignment to \( u_i \).
- We denote by \( \alpha_D \), an assignment on (boolean) variables \( \{d_0, d_1, \ldots, d_{n-1}, d_{\text{sign}}\} \), interpreted as the (n-bit) index of a variable in \( \text{Vars}(\Psi) \) and one sign bit. Here \( d_{n-1} \) is the MSB and \( d_0 \) is the LSB. We view the assignment as \( \overline{\alpha_D} \in \{0,1\}^{n+1} \) as an \( (n+1) \)-bit vector.
- For an assignment \( \overline{\pi} \in \mathbb{B}^n \), \( D_1(\overline{\alpha_U}) \) (similarly \( D_2(\overline{\alpha_U}) \) and \( D_3(\overline{\alpha_U}) \)) are the \( n+1 \) bits signifying \( \text{var1}(\overline{\alpha_U}), \text{sig1}(\overline{\alpha_U}) \) (\( \text{var2}(\overline{\alpha_U}), \text{sig2}(\overline{\alpha_U}) \) and \( \text{var3}(\overline{\alpha_U}), \text{sig3}(\overline{\alpha_U}) \)) respectively.
Let the view of the thread be $\alpha$. We observe that each thread executing a clause with index $n$ makes writes to one of the program variables or $a\alpha$. Finally the thread makes writes to one of the program variables.

### 8.3.2 Checking Satisfiability of Clause

Lemma 31. For all $\lambda_i$ such gadgets, one for each level $0 \leq i \leq n-2$.

#### 8.3.1 Acquiring Variable Index and Sign

We observe that each thread executing a $c_{\text{CL-ENC}}$ function makes a (single) write to $s$, with the message $(s, 1, \text{view})$ where $\text{view}$ has embedded in it an assignment $\alpha_U$. We write $\alpha \circ \text{view}$ to denote that the assignment $\alpha$ is embedded in $\text{view}$. Now a thread $p$ executing a $c_{\text{SAT}}$ function acquires the assignment $\alpha_U$, and computes (non-deterministically) one amongst $D_1(\overline{\alpha_U})$, $D_2(\overline{\alpha_U})$, $D_3(\overline{\alpha_U})$ reaching the label $\lambda_1$. The correctness invariant involved is formalized in the following lemma.

- **Lemma 30.** Let a thread $p$ executing the $c_{\text{SAT}}$ function read a message $(s, 1, \text{view})$ with $\alpha \circ \text{view}$. When the $p$ reaches the label $\lambda_1$ computing $D_i$ ($i \in \{1, 2, 3\}$) with $\alpha_D = D_i(\overline{\alpha_U})$. Let the view of the thread be $\text{view}'$. Then we have $\alpha_D \circ \text{view}'$.

#### 8.3.2 Checking Satisfiability of Clause

Continuing from above, let $p$ compute $D_i$ in $c_{\text{CV}}$ reaching $\lambda_1$. Then by lemma 30, we have $\alpha_D = D_i(\overline{\pi})$ embedded in the view of the thread. Now, using $c_{\text{Check}}$, $p$ checks that the clause with index $\overline{\pi}$ is satisfied by the $n + 1$ bits $\pi_D$ representing a variable and the sign of the variable in the clause. Finally the thread makes writes to one of the program variables $a_{n-1,0}$ or $a_{n-1,1}$. We have the following lemma that shows correctness of this operation.

- **Lemma 31.** A thread $p$ can make the write $(a_{n-1,0}, 1)$ (similarly $(a_{n-1,1}, 1)$) if and only if, clause $\overline{\alpha_U}$ is satisfied and if $\alpha_U(u_{n-1}) = 1$ (similarly $\alpha_U(u_{n-1}) = 0$).

### 8.3.3 Checking all Clauses

In section 8.3.1 and section 8.3.2 we have discussed how the system can check satisfiability of a single clause. Now, we need to check that each clause satisfied. We do this via additional modules to the PSPACE construction.

Towards this goal, define a level predicate $\text{IsSAT}(u_{n-1}, u_{n-2}, \ldots, u_0)$ denoting that the clause $\overline{\alpha_U} = u_{n-1} \ldots u_1 u_0$ is satisfiable. Now very similarly to section 7.4 we define the following formulae:

For $0 \leq i \leq n - 1$,

$$\Upsilon_i \equiv \forall u_i \exists u_{i+1} \ldots \forall u_{n-1} \exists u_0 \ldots \exists u_{i-1} \text{IsSAT}(u_{n-1}, u_{n-2}, \ldots, u_0)$$

And we claim the following lemma,
Lemma 32. For $0 \leq i \leq n - 2$, $\Upsilon_i$ is true $\iff$ the labels $\lambda_3, \lambda_4$ in the gadget $c_{\text{forall}[i]}$ can be reached.

The proof of Lemma 32 follows exactly in similar lines to that of Lemma 21 and Lemma 22. Finally, note that $\Upsilon_0$ is equivalent to the SuccinctSAT instance being satisfiable. We have the following final lemma to show correctness of the entire construction.

Corollary 33. We can reach the assert false assertion in the $c_{\text{assert}}$ gadget $\iff \Upsilon_0$ is true.

This gives us the main theorem

Theorem 34. The verification of safety properties for parameterized systems of the class $\text{env}(\text{nocas}, \text{acyc}) \parallel \text{dis}(\text{nocas})$ under RA is NEXPTIME-hard.

9 Conclusion

Atomic CAS operations are indispensable for most practical implementations of distributed protocols, yet, they hinder verification efforts. Undecidability of safety verification in the non-parameterized setting \cite{1} and even in the loop-free parameterized setting $\text{env}(\text{acyc})$, are a testament to this.

We tried to reconcile the two by studying the effects of allowing restricted access to CAS operations in parameterized systems. Systems which prevent the $\text{env}$ threads from performing CAS operations and allow only either (1) loop-free $\text{dis}$ programs or (2) loop-free $\text{dis}$ programs along with a single (‘ego’) program with loops lead to accessible complexity bounds. The simplified semantics based on a timestamp abstraction provides the infrastructure for these results. The PSPACE-hardness gives an insight into the core complexity of RA (PureRA) that stems from the consistency mechanisms of view-joining and timestamp comparisons.

We conclude with some interesting avenues for future work. A problem arising from this work is the decidability of CAS-free parameterized systems, $\text{env}(\text{nocas})\parallel\text{dis}_1(\text{nocas})\parallel\cdots\parallel\text{dis}_n(\text{nocas})$ which seems to be as elusive as its non-parameterized twin $\text{dis}_1(\text{nocas})\parallel\cdots\parallel\text{dis}_n(\text{nocas})$. We believe that ideas in this paper can be adapted to causally consistent shared memory models \cite{50} as well as transactional programs \cite{15} in the parameterized setting. On, the practical side, the Datalog encoding suggests development of a tool, considering that Horn-clause solvers are state-of-the-art in program verification.

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