A Comprehensive and Cross-Platform Test Suite for Memory Safety
Towards an Open Framework for Testing Processor Hardware Supported Security Extensions

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ABSTRACT
Memory safety remains a critical and widely violated property in reality. Numerous defense techniques have been proposed and developed but most of them are not applied or enabled by default in production-ready environment due to their substantial running cost. The situation might change in the near future because the hardware supported defenses against these attacks are finally beginning to be adopted by commercial processors, operating systems and compilers. We then face a question as there is currently no suitable test suite to measure the memory safety extensions supported on different processors. In fact, the issue is not constrained only for memory safety but all aspect of processor security. All of the existing test suites related to processor security lack some of the key properties, such as comprehensiveness, distinguishability and portability.

As an initial step, we propose an expandable test framework for measuring the processor security and open source a memory safety test suite utilizing this framework. The framework is deliberately designed to be flexible so it can be gradually extended to all types of hardware supported security extensions in processors. The initial test suite for memory safety currently contains 160 test cases covering spatial and temporal safety of memory, memory access control, pointer integrity and control-flow integrity. Each type of vulnerabilities and their related defenses have been individually evaluated by one or more test cases. The test suite has been ported to three different instruction set architectures (ISAs) and experimented on six different platforms. We have also utilized the test suite to explore the security benefits of applying different sets of compiler flags available on the latest GNU GCC and LLVM compilers.

1 INTRODUCTION
It is widely known that the lack of memory safety in low-level languages like C/C++ enables attackers to maliciously access data in the memory, alter the value of key variables such as code pointers, hijack the behavior of applications, or even take full control of a computer system [92]. In addition to the endless endeavor to discover and then fix the individual bugs scattered around the enormous software ecosystem, researchers have proposed a multitude of defense techniques in recent decades to thwart one or multiple types of attacks exploiting memory bugs. However, memory safety remains a critical and widely violated property in reality as most of the operating systems (OSes) and applications running on the off-the-shelf computers are not adequately defended.

Some of the early defense techniques, such as stack canary [28], data execution prevention (DEP) and address space layout randomization (ASLR) [93], have been widely adopted by commercial processors, operating systems (OSes) and compilers, which in turn triggers the evolution of the more complicated and evasive variants of attacks, such as return-oriented programming (ROP) [84, 95], jump-oriented programming (JOP) [12], counterfeit object-oriented programming (COOP) [81] and data-oriented programming (DOP) [23, 47]. To battle with these new attacks, numerous defense techniques have been proposed and developed. Some of the extensively studied techniques include type enforcement by tagging the pointers [8, 34, 53, 65, 104], pointer authentication (PA) [27, 59], code-pointer integrity (CPI) [52], control-flow integrity (CFI) [1, 16] and data-flow tracking [22, 89]. Yet most of them are not applied or enabled by default in production-ready environment due to their substantial running cost. For example, CFI has been implemented in LLVM and GCC [94] but it is almost disabled by default. The support of Intel MPX (memory protection extension) [76] was added but later dropped by major compilers. As
a result, even naive buffer overflow bugs can be exploited without being detected.

On the bright side, the situation might change in the near future, since the hardware supported defenses against the more complicated and evasive variants of attacks are finally beginning to land on commercial processors, OSes and compilers. The Intel control-flow enforcement technology (CET) [48], initially drafted in 2016 to thwart ROP and JOP related attacks, is included in the 11th generation Tiger Lake processors (expected in the middle of 2021). It will be supported by Windows 10 through the hardware-enforced stack protection. The Arm pointer authentication (PA) was added in the ARMv8.3-A [15] to facilitate defenses like CPI. It has already been implemented in the Apple A-series processors after A12 and supported in LLVM from version 8 [7]. The Arm memory tagging extension (MTE) was proposed in ARMv8.5-A [9] to further enhance memory safety in general and Google has announced its willingness to support it in Android [83].

With no doubt, hardware supported security extensions would significantly reduce the cost of applying defenses and gradually spread to all computer architectures and processor implementations. This tide of changes would bring us a new set of questions:

- **Q1:** How to compare the security provided by different processors? When picking a proper processor (actually a minimal platform comprising of a processor, an OS and a compiler) for a specific system to be developed, a system designer may desire to choose the one providing the maximum security protection from all candidate processors within the performance and cost budget.
- **Q2:** How to choose the right compiler and compiler flags (OS features) for the best security-performance trade-off? When shipping an application to a target processor, an application designer might wish to apply a proper set of compiler flags on a suitable compiler that enables the most security extensions available on the target processor while maintaining the performance target.
- **Q3:** How to evaluate the security benefit of a new defense on a certain processor? As security researchers, we would also like to systematically evaluate the security benefit of a newly proposed defense on a target processor.

We believe the answer is to create a test suite which is comprehensive enough to quantitatively evaluate the safety of a processor while also portable enough to comparatively evaluate multiple processors and be expanded to evaluate new defenses, vulnerabilities and architectures. Obviously, this will be an extremely challenging while long-lasting work.

As an initial step, we propose an expandable test framework for measuring the processor security and open source a memory safety test suite utilizing this framework. The framework is deliberately designed to be flexible so it can be gradually extended to all types of security features supported by the processor architecture and hardware (micro-architecture), such as defenses targeting the cache side-channels and speculative execution attacks.

The initial test suite for memory safety currently contains 160 test cases covering spatial and temporal safety of memory, memory access control, pointer integrity and control-flow integrity. Each type of vulnerabilities and their related defenses have been individually evaluated by one or more test cases. The test suite has been ported to three different instruction set architectures (ISAs) and experimented on six different platforms. We have also utilized the test suite to explore the security benefits of applying different sets of compiler flags available on the latest GNU GCC and LLVM compilers.

The rest of this paper is organized as follows: Section 2 explains the motivation behind this work. Section 3 describes the assumptions made in this paper. Section 4 illustrates the testing framework proposed to construct and run the test suite. The available test cases are summarized in Section 5 with the implementation challenges illustrated in Section 6. Section 7 analyzes the test results on the six ported platforms. Section 8 discusses the related and future work. Finally, the paper is concluded by Section 9.

## 2 MOTIVATION

This work is motivated by the lack of testing for processor security in both industry and academia.

### 2.1 The Lack of Testing in Industry

The systematic testing for processor security is almost non-existing in industry. Major processor manufacturers and OS vendors may have internal tests but they are not in any way shared or publicized. They normally sit on the back seat and are passively driven to respond to vulnerabilities only when they are discovered and even already publicized. Take the discovery of Meltdown and Spectre for example, it was reported that Intel did not inform the U.S. National Security Agency until they were made public [66]. Microsoft eventually mobilized hundreds of people across the company and urgently brought in external experts in response and negotiated an extension of the disclosure date to 120 days [41]. All of these indicate that the transient execution vulnerabilities have struck the whole industry off guard. If processor designs and the manufactured central processing units (CPUs) were systematically and regularly tested for hardware security, the situation might be significantly improved, at least the response would be much more prompt. However, there is no evidence of such testing facility being proposed or developed. The mitigation of processor vulnerabilities are still internally evaluated, responded and potentially resolved by individual processor manufacturers. This would leave the smaller players, who cannot spare engineers to respond to these security concerns or simply are not knowledgeable enough to handle these concerns, out in the insecure wild along with their customers.

The situation on the customer side is even more stark. End customers are forced to unconditionally trust the security claims from processor manufacturer without any means to verify them. Even governments may have very limited ways to measure the security of the processors deployed on the safety critical infrastructures.

If there is a generic testing framework capable of measuring the processor security, even if the measurement covers only the publicized hardware vulnerabilities, processor manufacturers may benefit from it by obtaining an early warning on the potentially unprotected vulnerabilities and the customer can earn extra confidence on the security claims produced by the manufacturers, as well as a mean to compare the security levels of different CPUs.

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### 2.2 Insufficient Testing in Academic Research

The research in academia is normally more advanced and open than those in industry, which is the same for the security evaluation for processors. However, the existing research is still insufficient.

Some test suites have already been proposed in the literature. The Juliet C/C++ and Java test suite \[13\] is a widely used collection of flawed programs to test the effectiveness of static analyzers in compilers. RIPE (runtime intrusion prevention evaluator) \[103\] provides a combination of synthetic buffer overflow attacks as a way to test the effectiveness of related defenses. RIPE is perhaps the most relevant and well-known test suite for processor security and has already been extensively used in architectural researches to verify their defenses against control-flow attacks \[52, 89\], especially the ROP variants. Each test case in RIPE is a relatively complete attack specified by five factors: the location of the buffer to overflow, the type of code pointer to corrupt, the type of overflow attack, the type of shell code and the function to be abused in the overflow attack. Since each factor has multiple choices, RIPE contains as many as 850 test cases to cover the ROP variants of control flow alteration caused by buffer overflow. It is obvious that this way of testing (by relatively complete attacks involving multiple attack factors) and reaching coverage (by exhausted testing) is very hard to be extended into a full-fledged suite for all aspects related to processor security.

None of the existing test suites can, or be expanded to, conduct a thorough measurement of the safety of a processor due to the lack of some of the following key properties:

- **Comprehensiveness**: The test suite should have a wide coverage of all types of vulnerabilities and defense techniques especially those potentially supported by the processor hardware. Most of existing test suites either cover only a portion of the vulnerabilities and protections, such as RIPE, or concentrate on only the software defenses, such as Juliet.
- **Distinguishability**: To provide a quantitative evaluation, the test suite should provide per-vulnerability and per-defense test cases which concentrate on a single attack factor (such as one type of target or one attack technique). Such level of distinguishability is not available in RIPE.
- **Structure**: The test suite should be produced in a structured way rather than a collection of ad-hoc test for individual vulnerabilities or defenses. This structure is crucial for the test suite to reach a coverage which is understandable and reasonable.
- **Portability**: The test suite should be able to be ported to multiple platforms using various computer architectures, OSes and compilers with a minimum effort. Once ported to a certain type of platforms, the test suite should run out-of-the-box on all variants of the same platform. When a new type of attacks or protection emerges, individual test cases should be able to be added with a minimum effort. None of the existing test suites maintain good portability.

In this work, we seek to provide these key properties in a expandable testing framework by the following method.

- **Comprehensiveness**: It is impossible to bring up a comprehensive test suite for all aspects of processor security in a short period of time but we can gradually grow the aspects covered by the test suite. As in the initial test suite, major aspects of the memory safety are covered.
- **Distinguishability**: Every test case in the test suite is made concentrating on a single type of vulnerabilities or defenses. The runtime context of individual test cases are created by a rather brutal forced way, as shown in Section 4.3, to deliberately avoiding introducing extra vulnerabilities. To some extent, each test case is a partial attack that is normally executed as a single step in a relatively complete attack.
- **Structure**: The dependence of individual types of vulnerabilities and defenses are analyzed and recorded using a relation graph, as described in Section 4.2. By utilizing this graph, test cases can collect crucial pre-knowledge from the results of other tests and use it to improve test accuracy. The order of testing and a reasonable coverage are also derived form this relation graph.
- **Portability**: The code of individual test cases are divided into platform independent and dependent parts. All the platform dependent parts are moved to a shared platform-specific library as described in Section 4.3. This significantly improves the portability of the test suite.

### 3 Threat Model

**Adversarial capability**: We assume unprivileged attackers with the ability to execute and control the input of user programs on an OS. It is also assumed that user programs commonly contain memory safety vulnerabilities which might be exploited to achieve arbitrary reads and writes into the program address space. As a consequence, any attacks utilizing the existing memory safety vulnerabilities to leak information, corrupt data, and hijack control flow are in scope. We limit the current test suite to attacks utilizing the existing memory safety vulnerabilities to attack the user level data space. Therefore, attacks that using side-channels, such as cache side-channels \[108, 109\] and transient execution attacks \[19\], and attacks targeting the kernel space are out of the scope of this paper but, of course, they are the targeted attacks for the future expended version of this test suite.

**Definition of a platform**: The safety of a processor is measured by running the test suite on a minimum running environment, namely a platform, comprising the processor under test and a minimum OS running on it. This minimum OS includes a kernel and a small number of runtime libraries just enough for the execution of the user programs potentially under attack. All user programs are assumed to be compiled by a common compiler using similar compiler flags.

**Hardening assumptions**: We assume some memory safety protection features have been implemented by either software or hardware but the exact details of these features may not make available to the test suite unless they are visible to user-level programs (through environmental variables) or indicated by compiler flags fed to the test suite. If a safety protection feature is implemented, it should have already been supported by the OS and the compiler; therefore, the protection is enabled by default or can be switched on by compiler flags.
4 THE FRAMEWORK OF TESTING

This section proposes a flexible testing framework suitable for measuring the security provided by a processor. While in the description, we use memory safety as the targeted aspect of security for measurement.

4.1 Scope of Testing

Memory safety could be viewed as a set of memory safety properties. All memory corruption vulnerabilities and exploitation techniques rely on the absence of certain memory checks on one or more properties which allow values in memory to be maliciously leaked or altered against their original meaning in the program.

For example, a buffer overflow attack happens when the action of modifying the value of a buffer goes beyond its boundary. Modifying beyond the buffer boundary is the memory safety property that has been violated due to the lack of a proper boundary check. The fact that the modifying of the buffer can be made beyond the boundary is a vulnerability. To eliminate this vulnerability, the specific buffer can be patched with the missing boundary check in the source code, or this check can be universally added to all buffers to prevent them from being exploited by the same type of vulnerabilities. We consider the latter as a defense. A defense can be implemented purely by software but with significant slowdown [64, 82], or it can be enforced by hardware through memory tagging or fat pointers while with the help of compilers and libraries [62]. We consider the former as a pure software defense while the latter as a hardware supported security enhancement.

Memory safety is not the responsibility of the processor hardware but the whole system, including the programming language, the compiler, the operating system, the runtime libraries, the architecture and finally the processor hardware. Not all memory safety properties are enforceable by the processor hardware but when they are, adopting the hardware supported enforcement normally brings significant benefit in performance. The objective of the proposed test suite is to measure the security boost brought by the security enforcement potentially implemented in the processor under test. For this reason, the aforementioned buffer overflow attack should be tested because the missing boundary check can be enforced by the processor hardware through memory tagging or fat pointers. In other words, if the absence of a memory check can be exploited by attackers and the check can be efficiently enforced by the processor hardware (and architecture) with (or even without) the help of software, this check is considered a potential hardware supported security enhancement that should be covered by the test suite.

Although the concept might be easy to digest, the reality is still very much complicated. At least for memory safety, most architectural security enhancements require software (especially the compilers) involvement. The test suite aims to discover whether certain checks have been enforced with the support from the processor hardware: however, the fact that a test suite must be executed in a software environment blurs the boundary between software and hardware. A test might find the existence of a check but it cannot simply tell whether it is hardware supported or purely software enforced. As a result, the test suite should be considered as a best-effort approach to measure the memory safety supported by the processor hardware. The test suite should be compiled by compilers pre-installed in the production-ready OS and run on the OS with a minimal execution environment where only the necessary libraries are installed. In this scenario, checks (defenses) found by the test suite are likely to be enforced with the support from processor hardware (or at least the essential runtime library) rather than some third-party software.

With all the above in mind, we consider the processor hardware, the ISA, the kernel of the production-ready OS, the default compiler, and the essential runtime libraries as the scope of testing. This leaves the security features available in some binary-level translation and execution tools, and kernel patches (such as Grsecurity® [69]) out of the scope. Defenses that are usually implemented and enforced purely by software are not deliberately evaluated while each hardware enforceable memory check (defense) should be covered by a specific test case. Similarly, the test suite does not verify the existing software running on the target platform, including the kernel and the runtime libraries, is free of vulnerabilities. In fact, it assumes all programs may contain vulnerabilities but they would become difficult to exploit when proper defenses are enforced.

4.2 Definition of Coverage

Existing test suites choose to launch complete attacks exploiting a number of vulnerabilities and utilizes multiple attack techniques at different stages [71, 103]. If a coverage is defined as all possible ways of attacks, it would need to cover all the potential combinations of vulnerabilities and attack techniques, which becomes a task impossible to fulfill. As a result, existing test suites normally cover only a set of related types of vulnerabilities, leaving a significant amount of attack variants uncovered [55].

Instead of trying to reach a partial coverage by launching complete attacks, this test suite tries to cover a wide range of vulnerabilities with a large number of small and concentrated test cases. Each test cases endeavors to check the existence of a single type of memory vulnerabilities or the absence of a specific memory check. By doing this, the test suite satisfies the requirement for the first two key properties, comprehensiveness and distinguishability, as described in Section 2.

Since each test case concentrates on a single type of vulnerabilities, which is normally exploited as a step in a complex attack, test cases are not mutually isolated but rather rely on each other to provide key information. We try to describe this relationship between vulnerabilities by a graph, which then helps the test suite execute all test cases with a proper order and reach a coverage faster. More importantly, we can derive a clear definition of coverage based on this graph. Three types of relations have been considered:

- **Dependency**: If a type of vulnerabilities $A$ can be exploited only when another type $B$ is exploitable, $A$ depends on $B$. Take the classic ROP attack as an example. To alter the return address stored on the stack and make it point to a code gadget, the attacker needs to know the address of the gadget, which usually depends on that some code pages are readable as ASLR is enforced. In this case, $A$: alteration of return address depends on the $B$: readability of code pages.

- **Specialization**: If a constraint is applied on a type of vulnerabilities $B$, which creates a new type of vulnerabilities $A$, $A$ is a special case of $B$. Let us use the same ROP example. Since the
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A comprehensive and cross-platform test suite for memory safety is presented. The test suite is designed to be comprehensive and cross-platform, covering a wide range of vulnerabilities and defenses related to memory safety.

The test suite is based on the concept of a relation graph, which is used to depict the prerequisites of all test cases. The relation graph is a directed graph, where each node represents a test case, and the edges represent the prerequisites.

The test suite includes four special cases of ROP (any code): code injection in rodata, data, heap and stack.

The prerequisites for ROP (call site) are complicated. It has six prerequisites but it is enabled when one of ASLR and read code page passes, and one of the four over/underflow tests passes. This is literally a two-level relationship: Prerequisites are divided into subsets. In each subset, the prerequisite is met if one of the test cases passes. The final prerequisite is met when the results of all subsets are ANDed together.

To utilize the test suite at runtime, the relation graph is stored in a configuration JSON file and analyzed at runtime by a simple test scheduler written in Python. Listing 1 demonstrates a part of the configuration file describing Figure 1. Every record is a test case depicted as a node in the relation graph, with the name mapping.
Table 1. The prerequisites are listed in the “require” property, which is a list of lists. Each inner list contains prerequisites within the same subset while results of all inner lists of are ANDed together to decide whether the case is tested.

| Node Name       | JSON record name          |
|-----------------|---------------------------|
| read code page  | read-func                 |
| ASLR            | check-ASLR                |
| overflow (index)| overflow-write-index-stack|
| underflow (index)| underflow-write-index-stack|
| underflow (pointer)| underflow-write-ptr-stack|
| ROP (call site) | return-to-wrong-call-site |
| ROP (any code)  | return-to-non-call-site   |
| ROP (function)  | return-to-func            |
| code injection (rodata) | return-to-instruction-in-rodata |
| code injection (data)  | return-to-instruction-in-data |
| code injection (heap)   | return-to-instruction-in-heap |
| code injection (stack)  | return-to-instruction-in-stack |

Listing 1: configure.json

```json
{
  "return-to-wrong-call-site": {
    "require": [ [ "read-func", check-ASLR"],
      "overflow-write-index-stack",
      "underflow-write-index-stack",
      "overflow-write-ptr-stack",
      "underflow-write-ptr-stack" ]
  },

  "return-to-non-call-site": {
    "require": [ [ "return-to-wrong-call-site" ]
  },

  "return-to-func": {
    "require": [ [ "return-to-wrong-call-site" ]
  },

  "return-to-instruction-in-rodata": {
    "require": [ [ "return-to-non-call-site" ]
  },

  "return-to-instruction-in-data": {
    "require": [ [ "return-to-non-call-site" ]
  },

  "return-to-instruction-in-heap": {
    "require": [ [ "return-to-non-call-site" ]
  },

  "return-to-instruction-in-stack": {
    "require": [ [ "return-to-non-call-site" ]
  },

  ... // omit some code
```

4.3 Construction of Test Cases

Portability is one of the major concerns in the construction of test cases. There is no doubt that new types of vulnerabilities will be discovered in the future, along with new defense techniques. The test suite tries to cover all the known types of vulnerabilities while allowing new test cases to be easily added. The case by which new test cases can be added is then crucial for the usefulness of the test suite. In addition, new computer architectures and ISA extensions will be constantly proposed. Instead of painstakingly re-implement all test cases whenever a new ISA is added or a new OS is supported, the test suite should try to reuse the platform-independent part while limiting the platform-specific part to relatively small code segments. For these reasons, the test suite is composed of two parts: individual platform-independent test cases and a shared platform-specific support library.

Each test case is written in a short (and usually malformed) C++ program trying to test a single type of vulnerabilities. If the vulnerabilities exist, the test case should exploit the vulnerability and return zero; otherwise, a non-zero exit code is used to indicate when and where the test fails or crashes. Whenever possible, the related vulnerabilities involved in each test cases is minimized by directly creating a vulnerable context at runtime. Most code is written in a portable and compiler-independent manner. However, when a (usually malicious) behavior might be detected and disturbed by a compiler, extra code might be added to prevent the compiler optimization and snippets of assembly code might be used to replace the C++ code as most compilers would not analyze the embedded assembly, let alone optimize it. Since the added assembly code snippets are unavoidably platform-specific, they are extracted from test cases and moved to the shared support library.

For example, Listing 2 illustrates the test for return-to-wrong-call-site which hijacks the return address to a valid call site within static analysis. The main() function is a bare minimum. It first reads offset from input as it is later needed by helper(). The value of this offset is actually selected by the test scheduler, which will be explained in details in Section 6.1. The main() function then calls helper() twice (line 17 and 23) with the latter one trying to alter its own return address. If the helper() function succeeds, it would return to line 19 labeled by main_mid, and exit with a 0. Otherwise, the program may exit with a non-zero code 2, indicating the test fails to override the return address. The exit code is initialized to 0 and stored in a volatile global variable grv to escape compiler optimization.

The helper() function is also straightforward. FORCE_NOINLINE stops the function from being inlined using a compiler attribute. ENFORCE_NON_LEAF_FUNC inserts some code to guarantee that helper() is not a leaf function and the return address is always pushed on the stack even on RISC (reduced instruction set computer) machines. The embedded assembly MOD_STACK_LABEL(main_mid, offset) replaces the return address with the address of main_mid when the function is called the second time (grv == 2). The location of the return address on the stack is pinpointed by the program input offset, which is the global parameter collected by the main() function indicating the offset to the stack pointer. As the value of offset varies on different platforms or even with different compiler flags.

1 An assembly label is used because C++ labels are invisible outside the function body.
This is why it is detected by other tests and then provided by the test scheduler (see Section 6.1 for more details). Finally, helper() revises the exit code to 0 just before return. If the return address is successfully modified and helper() indeed returns to main_mid, the program would exit as normal (code 0) in the main() function.2

Most platform-specific codes are written in embedded assembly and referenced by macros, which are defined in the shared support library. As shown in Listing 3, the header file included in test cases (include/assembly.hpp) is just a wrapper pointing to the correct header prepared for the target platform. Assuming the target platform is a x86-64 machine, macro __x86_64 is predefined by most compilers and x86_64/assembly.hpp is then included by detecting this predefined macro.

Listing 4 reveals parts of support library for the x86-64 architecture (x86_64/assembly.hpp). FORCE_NOINLINE is short for a built-in attribute for non-inline functions. To enforce the non-leaf condition, ENFORCE_NON_LEAF_FUNC inserts an irremovable external call. MOD_STACK_LABEL(label, offset) is used to replace the return address stored at [$$rsp+$$offset] with the address of label in a rather brutal forced manner. This avoids the use of traditional buffer overflow attacks and probably escapes from most compile-time detection, and allows the test case to concentrate on the modification of return address to a non-call-site vulnerability itself.

Assuming the functions of the macros defined in the shared support library are modular enough, supporting a new platform should be an easy task. A new “assembly.hpp” header file should be created to define all the platform-specific macros and functions using the new architecture. Currently there are only around 20 macros that are needed to be ported for each new architecture. This new header file is then added to the common header file include/assembly.hpp while checked by a predefined macro unique to the new platform. Adding a new test case for a newly discovered type of vulnerabilities may involve three steps: (1) Implement the test case using the shared support library. (2) If new macros are needed, they should be added to all supported platforms. (3) A record is added in the configuration file.

5 SUMMARY OF TEST CASES

This section summarizes the individual test cases provided by the initial test suite for memory safety.

5.1 Spatial Safety

Spatial safety refers to the property that memory accesses are always in compliance with the proper data boundaries and the scope of visibility defined by the program. Any access outside the boundary or the scope of visibility is considered insecure. It is violated by classic buffer overflow attacks [91], which is then used to smash the stack and alter the stored return address [6]. Heap attacks also resort to buffer overflow to access/alter data across the object boundary [25]. Currently, the test suite has 98 test cases to measure spatial safety.

2We use exit() (from stdlib) here as the call stack is corrupted.
5.1.1 General read out-of-boundary. 16 test cases in total.

Both buffer overflow and underflow reads have been tested. We consider two potential ways to access data out-of-boundary: One is to access with a valid buffer pointer but an out-of-boundary offset (index) and the other one is to directly make a previously valid buffer pointer point to an out-of-boundary location (ptr). For defenses using memory tags [74] or fat pointers [33, 53, 64], these two ways may result in exceptions being triggered at different locations depending on whether the pointer [27] or the buffer memory [74] is tagged. Since the defense mechanisms on stack, heap, global data and read-only data sections might be different, they are tested separately. These tests are the most general cases for out-of-boundary reads that read only the neighbors of the buffer (overflow by one) without going too far.

5.1.2 General write out-of-boundary. 12 test cases in total.

Similar to out-of-boundary read tests, these tests try to write out-of-boundary. Both buffer overflow and underflow writes have been tested. Both index and pointer ways of accesses have been considered. Buffers on stack, heap and global data sections have been tested separately.

5.1.3 Access cross the object boundary. 20 test cases in total.

All tests are special cases of the general read out-of-boundary and the general write out-of-boundary cases. Some defenses may choose to put invalid data between objects as a tripwire or enforce the boundary check at the granularity of objects [33]. In these cases, the general overflow vulnerabilities exist but the more severe form of them, accessing crossing the object boundary, is disabled. To check these types of vulnerabilities, the test suite tests both read and write accesses, both index and pointer ways of accessing, and objects on stack, heap, global data and read-only data.

5.1.4 Access cross the stack frame. Four test cases in total.

All tests are special cases of the general read out-of-boundary and the general write out-of-boundary cases. To thwart overflow attacks against variables over the frame boundary, some defenses choose to put padding bytes between the frames [10] while some other defenses use fat-pointers to enforce data integrity at the frame granularity [30]. Data compartmentalization at the frame granularity is also effective [68]. The test suite tests both read and write accesses across the frame boundary using indices or pointers.

5.1.5 Access cross pages. Four test cases in total.

All tests are special cases of the access cross the stack frame cases. Page table attributes have long been used to enforce access permissions. System software or memory allocation library may use the page accessing property to partially thwart overflow attacks. Since pages are normally larger than stack frames, we consider these as special cases of access cross the stack frame. The test suite tests both read and write access cross the page boundary using indices or pointers.
5.1.6 Access cross sections. 36 test cases in total.

| Test Case | Description |
|-----------|-------------|
| read-cross-section-stack-to-heap-index | Access cross-section stack to heap index |
| read-cross-section-stack-to-data-index | Access cross-section stack to data index |
| read-cross-section-stack-to-rodata-index | Access cross-section stack to rodata index |
| read-cross-section-stack-to-data-data | Access cross-section stack to data data |
| read-cross-section-stack-to-rodata-data | Access cross-section stack to rodata data |
| read-cross-section-stack-to-data-stack | Access cross-section stack to data stack |
| read-cross-section-stack-to-rodata-stack | Access cross-section stack to rodata stack |
| read-cross-section-stack-to-data-stack-ptr | Access cross-section stack to data stack ptr |
| read-cross-section-stack-to-data-data-ptr | Access cross-section stack to data data ptr |
| read-cross-section-stack-to-rodata-data-ptr | Access cross-section stack to rodata data ptr |
| read-cross-section-stack-to-data-stack-ptr | Access cross-section stack to data stack ptr |
| read-cross-section-stack-to-rodata-data-ptr | Access cross-section stack to rodata data ptr |
| read-cross-section-stack-to-data-data-ptr | Access cross-section stack to data data ptr |
| read-cross-section-stack-to-rodata-stack-ptr | Access cross-section stack to rodata stack ptr |
| read-cross-section-stack-to-data-stack-ptr | Access cross-section stack to data stack ptr |
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| read-cross-section-stack-to-data-data-ptr | Access cross-section stack to data data ptr |
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| read-cross-section-stack-to-rodata-stack-ptr | Access cross-section stack to rodata stack ptr |
| read-cross-section-stack-to-data-stack-ptr | Access cross-section stack to data stack ptr |
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| read-cross-section-stack-to-rodata-stack-ptr | Access cross-section stack to rodata stack ptr |
| read-cross-section-stack-to-data-stack-ptr | Access cross-section stack to data stack ptr |
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| read-cross-section-stack-to-data-stack-ptr | Access cross-section stack to data stack ptr |
| read-cross-section-stack-to-rodata-data-ptr | Access cross-section stack to rodata data ptr |
| read-cross-section-stack-to-data-data-ptr | Access cross-section stack to data data ptr |
| read-cross-section-stack-to-rodata-stack-ptr | Access cross-section stack to rodata stack ptr |
| read-cross-section-stack-to-data-stack-ptr | Access cross-section stack to data stack ptr |

All tests are special cases of the general read out-of-boundary and the general write out-of-boundary cases. Attackers can manipulate the stack data using a heap pointer [26] and probably vice versa. To test these special attack variants, the test suite checks all possible scenarios for accessing cross section boundaries.

5.1.7 Spray attack. Six test cases in total.

| Test Case | Description |
|-----------|-------------|
| spray-cross-object-stack | Spray cross object stack |
| spray-cross-object-heap | Spray cross object heap |
| spray-cross-object-data | Spray cross object data |
| spray-cross-frame | Spray cross frame |
| spray-cross-page-stack | Spray cross page stack |
| spray-cross-page-heap | Spray cross page heap |

All tests are special cases of the general write out-of-boundary cases. In the access tests, out-of-boundary data are directly accessed using indices or pointers and leave all the data in between untouched. While in spray tests, all the data between the buffer to the out-of-boundary target are rewritten. Such behavior is more likely to be detected by memory padding [10, 33] and marking [99] than a direct out-of-boundary access. The test suite currently tests six spray attacks: spray cross the object boundary on stack, heap and global data, spray cross stack frames, and spray cross pages on stack and heap.

5.2 Temporal Safety

Temporal safety refers to the property that data accessed in memory happens only within the lifetime of the data. Any access before (uninitialized) or after (use-after-free, UAF) the lifetime is considered insecure. These types of vulnerabilities potentially lead to corrupted values in memory [23], return-to-libc [70], and arbitrary memory read and write eventually.

Since the target of this test suite is to measure the safety supported by the processor hardware as described in Section 4.1, its test cases concentrate on whether a general out-of-lifetime access can happen and consider attacks specialized to certain memory allocation algorithms [105] out of the scope.

5.2.1 Access after free on heap. Three test cases in total.

| Test Case | Description |
|-----------|-------------|
| read-after-free-org-heap | Read after free on heap |
| read-after-free-alias-heap | Read after free on heap alias |
| write-after-free-heap | Write after free on heap |

After an object is released, all pointers pointing to this object become dangling pointers and should not be used afterward. However, attackers may utilize these dangling pointers to read the previously released object, leading to information leakage. Even worse, attackers may write to the just released memory which potentially causes data corruption. To thwart these threats, defenses can deliberately nullify all dangling pointers [54, 110] or checking whether a pointer is dangling at the dereference point [62, 63]. The three tests here exam the possibility of reading/writing a heap object after it is released. For reading the released object, both the original pointer or a copy of it (alias) have been tested as a way to measure the completeness of pointer nullification.

5.2.2 Reclaim on heap. Only one test case.

| Test Case | Description |
|-----------|-------------|
| reallocate-heap | Reallocate heap |

Once a dangling pointer falls into the control of attackers, it can be used to launch targeted data corruption if the released memory is reallocated to the same type of objects. Some secure memory allocators try to prevent objects from reclaiming the previously released memory [4, 67] but attackers may force the memory allocator to do so [54]. To measure this vulnerability, this test tries to force the memory allocator to place an object with the same type at the same location where it is previously released.

5.2.3 Access after reclaim on heap. Three test cases in total.

| Test Case | Description |
|-----------|-------------|
| access-after-reclaim-heap | Access after reclaim heap |
| write-before-reclaim-heap | Write before reclaim heap |
| write-after-reclaim-heap | Write after reclaim heap |

All tests depend on the reclaim on heap test. Assuming attackers have successfully forced an object to reclaim the same memory space previously released, they would then try to manipulate the object using a dangling pointer. access-after-reclaim-heap tests whether an uninitiated variable belonging to the newly allocated object retains its previous value. In case the memory is safely cleaned when it is released, write-before-reclaim-heap tries to maliciously initiate this uninitiated variable just before the memory is reclaimed. Finally, write-after-reclaim-heap tests whether a dangling pointer can be used to corrupt an object after it reclaims the same memory space.

5.2.4 Access after free on stack. Two test cases in total.

| Test Case | Description |
|-----------|-------------|
| read-after-free-alias-stack | Read after free on stack alias |
| write-after-free-stack | Write after free on stack |

UAF attacks happen on stack as well. When a function returns, the stack frame is released for the next function call. If a dangling pointer pointing to the released stack frame is mistakenly leaked by
a function argument, a global variable or even the return value, it allows attackers to manipulate the frame when it is reclaimed [110]. Similar to the tests for UAF on heap, the tests start with reading a released stack variable to see if it retains its value and then write it to see whether the released frame space is protected.

5.2.5 Reclaim on stack. Only one test case.

- reallocate-stack

The memory structure of the stack frame for the same function is normally the same every time the function is called. This potentially allows attackers to precisely manipulate the variables on the stack using a dangling pointer. Fine-grained runtime stack layout randomization [2] may stop such attacks by locating stack variables at different positions whenever a function is called again. This test verifies whether the stack layout is changed when a function is called again.

5.2.6 Access after reclaim on stack. Three test cases in total.

- access-after-reclaim-stack
- write-before-reclaim-stack
- write-after-reclaim-stack

All tests are dependent on the reclaim on stack test. Assuming the stack layout remains the same for the same function, access-after-reclaim-stack tests whether an uninitiated variable keeps its value from the previous function call, write-before-reclaim-stack tries to maliciously initiate the uninitiated variable before the next function call. Finally, write-after-reclaim-stack tests whether a dangling pointer can be used to alter a stack variable when the stack frame is reclaimed by a new function call.

5.3 Access Control

We consider all defense techniques that exert restrictions on accesses as access control related defenses. ASLR [42] normally acts as the first level of defense against code-reuse attacks. It prohibits attackers from collecting the addresses of the required gadgets by static binary analysis. DEP is another widely adopted defense that disallows codes in writable pages from being executed. To thwart the dynamic code-reuse attacks which collect gadgets at runtime [88], both code randomization [87] and read exclusive execution (ReX) [72] have been proposed to forbid attacker from reading executable pages.

5.3.1 Access control. Three test cases in total.

- check-ASLR
- read-func
- read-GOT

check-ASLR checks whether the address space is randomized, read-func checks whether the body of a function (in a code page) can be read, and finally read-GOT checks whether an entry in the global offset table (GOT) can be read.

5.4 Pointer Integrity

We consider all attacks that directly cause a malicious alteration of control flow as control-flow related attacks and treat all defense techniques against such attacks as control flow related defenses. Most defenses fall into two categories: pointer integrity and control-flow integrity. The former prevents pointers (mostly code related) from being maliciously modified [52] while the latter tries to stop those altered pointers from affecting the control flow [1].

Since most control-flow attacks rely on the alteration of certain key pointers, the tests for pointer integrity are considered as prerequisites for the tests for control-flow integrity. This set of tests aim to cover the alteration of different types of key pointers. Note that the alteration of return addresses is closely related to ROP attacks and is thus tested there.

5.4.1 Function pointer. Two test cases in total.

- func-pointer-assign
- func-pointer-arithmetic

Function pointers are one of the most frequently attacked targets. func-pointer-assign checks whether a function pointer can be altered with embedded assembly (therefore bypassing the analysis and potential protections from compilers through pointer authentication [59] or tagging [52, 89]). It is very rare that arithmetic operations occur on function pointers [24]. Function pointers are normally cloneable but not mutable. By applying unnecessary arithmetic operations on a function pointer, func-pointer-arithmetic tests whether such behavior raises any exceptions.

5.4.2 VTable pointer. Two test cases in total.

- read-vtable-pointer
- write-vtable-pointer

Virtual table (VTable) pointers are the major targets in COOP attacks [81]. Defenses like CPI can protect VTable pointers just like function pointers [52] and prevent them from being modified. This protection is tested by write-vtable-pointer. Since VTable pointers should not be explicitly accessed by any source-level program, and COOP attacks usually need to read and reuse VTable pointers, read-vtable-pointer checks whether deliberately reading a VTable pointer would trigger any exceptions.

5.4.3 Global offset table. Only one test case.

- modify-GOT

GOT is used by dynamically linked programs to search for (function and data) symbols defined in shared libraries at runtime. Since the content of the GOT is updated at runtime, GOT might be stored on a writable page. This potentially allows attackers to hijack library functions by altering the corresponding GOT entries [18]. The provided test modify-GOT checks whether an entry in the GOT can be hijacked to an attacker controlled function.

5.5 Control-Flow Integrity

Control flow refers to the indirect jumps caused by function returns, function calls and other compiler added jumps. By altering the return address stored on the stack, attackers can redirect the control flow to code chosen or injected by them, which is the basis for ROP attacks [84]. Similarly, maliciously affecting the pointers used in these indirect calls and jumps [12, 81] can hijack the control flow as well. Currently, the test suite has 41 test cases to measure the backward control-flow integrity:
5.5.1 Return to injected code. Four test cases in total.

- return-to-instruction-in-stack
- return-to-instruction-in-heap
- return-to-instruction-in-data
- return-to-instruction-in-rodata

All tests are special cases for return-to-non-call-site. Although attacks relying on direct code injection are largely thwarted by DEP, the same defense may not be available on legacy systems and embedded systems. As a result, this test suite still checks whether a function can be hijacked and returned to an injected code. Note that injecting code using constant texts (read-only data) remains viable on most systems unless some forms of ROP attacks are enforced [72].

5.5.2 Return to existing code. Six test cases in total.

- return-to-wrong-call-site-within-static-analysis
- return-to-wrong-call-site
- return-to-non-call-site
- return-to-libc
- return-to-libc
- return-without-call

All tests are relaxed cases of return-to-wrong-call-site-within-static-analysis. return-to-non-call-site represents the common ROP attacks that use arbitrary code snippets as gadgets. To avoid the detection of coarse-grained CFI checks, attackers may be forced to use call preceded gadgets (return-to-wrong-call-site) [21] long and benign code segment (return-to-libc [44] and return-to-libc [70]), or even previously returned locations (replay attack, return-to-wrong-call-site-within-static-analysis [77]). When multiple gadgets are chained together, the call-return pair becomes unbalanced, which should be easy to detect by a shadow stack [17, 29]. This type of unbalance is tested by return-without-call.

5.5.3 Call to injected code. Four test cases in total.

- call-instruction-in-stack
- call-instruction-in-heap
- call-instruction-in-data
- call-instruction-in-rodata

All tests are special cases of call-mid-func. Similar to the tests for backward control-flow integrity, these tests check whether a function call can be hijacked to a code injected by attackers.

5.5.4 Call to existing code. Three test cases in total.

- call-wrong-func-within-static-analysis
- call-wrong-func
- call-mid-func

All tests are special cases of call-wrong-func-within-static-analysis. call-mid-func is the most general case as the function pointer is hijacked to an arbitrary location. Such attacks can be easily detected by most CFI checks [1, 16] as the arbitrary location is rarely a function entry point. To avoid detection by coarse-grained CFI checks [31], call-wrong-func hijacks a function pointer to another function while the function chosen by call-wrong-func-within-static-analysis also falls in the valid set of targets collected by static control-flow analyses (thus is detectable only to path-sensitive CFI defenses [35, 111]).

5.5.5 Call with wrong arguments. Nine test cases in total.

- call-wrong-num-arg-func
- call-wrong-type-arg-int2double-func
- call-wrong-type-arg-op2double-func
- call-wrong-type-arg-fp2dp-func
- call-wrong-type-arg-dp2fp-func-stack
- call-wrong-type-arg-dp2fp-func-heap
- call-wrong-type-arg-dp2fp-func-data
- call-wrong-type-arg-dp2fp-func-rodata
- call-wrong-type-arg-dp2fp-func-xxxx

All the call-wrong-type-arg-dp2fp-func-xxxx test cases depend on the call-instruction-in-xxxx. Some research claims that even the fine-grained CFI defenses can be circumvented by corrupting only the arguments of functions [39] while the types of arguments can be used to enhance the accuracy in detecting COOP attacks [98]. To cover these attack and defense variants, call-wrong-num-arg-func checks whether a function can be called with a mismatched number of arguments. Extra tests are provided for function calls with mismatched types of arguments, such as providing an integer for a double argument (int2double), providing an object pointer for a double or an integer pointer (op2double and op2intp), and providing a function pointer to a data pointer (fp2dp). The last four tests check whether injected code can be called by placing a data pointer in the place for a function pointer (dp2fp).

5.5.6 VTable injection. Three test cases in total.

- call-wrong-func-vtable-stack
- call-wrong-func-vtable-heap
- call-wrong-func-vtable-data

Modern compilers put VTales on read-only pages to prevent them from being altered. However, attackers can forge fake VTales in other writable spaces and using them to dislodge the real ones [81]. These three tests check whether VTales can be replaced with a fake one created on stack, heap and global data.

5.5.7 Replace VTales with existing tables. Seven test cases in total.

- call-wrong-func-vtable-parent
- call-wrong-func-vtable-child
- call-wrong-func-vtable-sibling
- call-wrong-func-vtable
- call-wrong-func-vtable-released
- call-wrong-func-vtable-offset
- call-wrong-num-arg-vtable

Assuming VTales cannot be forged, an attacker would try replacing them with existing ones inside the memory. To thwart this type of COOP attacks, class hierarchy analysis [49] tries to limit the tables that are available to attackers. call-wrong-func-vtable checks the most general case where a VTable is replaced by an arbitrary table existing in memory. The test suite then checks whether the VTales from a parent class, a child class or a sibling class can be used for replacement. call-wrong-func-vtable-released tests whether a VTable pointer of a released object can be reused in a live object [80]. call-wrong-func-vtable-offset checks whether a VTable pointer can be added with a small offset. Finally, call-wrong-num-arg-vtable checks whether the virtual function can be replaced with another one with different number arguments; therefore, allowing attackers to manipulate the arguments.
In this test suite, the value of offset is obtained from a blind testing using return-to-wrong-call-site, which is the common prerequisite for allROP tests, and fed to all depended tests as an input argument. As shown in Listing 2 and described in Section 4.3, the test gets an offset from input and checks whether the return address can be hijacked to a seemly valid return site main_mid. Since this offset is unknown, the test suite tries to get the correct value by launching the same test multiple times with different values of offset. Such behavior is defined in the configuration file through an extensions illustrated in Listing 5.

The list recorded in property arguments (line 6 in Listing 5) defines the input arguments for a test. Arguments are simply attached to the test case except for the special ones starting with "-r".

These special arguments always take the form of "-rNAME", where r denotes the type and NAME identifies the property defining this argument. Currently, we support three types: range ("r"), list ("l") and variable ("v"). When an argument takes the form of "-rNAME", it actually defines a range ("-r") defined in a property named "NAME". In the case of return-to-wrong-call-site, a range of [0:7] ([0, 8, 1] in python) is defined by property offset (line 8 in Listing 5) and used as an argument, which means the test would be launched eight times for each value in the range. The final property set-var denotes that the variable stack-offset would be assigned with the offset resulting a success test. For example, if test return-to-wrong-call-site succeeds with argument 3, stack-offset is then set to 3 and all other test cases using this variable would get an argument of 3. return-to-non-call-site is one of these cases (line 11). Its input argument is therefore defined to use the value of stack-offset (line 13 in Listing 5). Since return-to-wrong-call-site is listed as a prerequisite, the value of stack-offset must have been assigned when return-to-non-call-site is tested. In other words, the test scheduler and the JSON configuration ensure that stack-offset is initiated before testing all the test cases depending on it.

6.2 Fight Against Compiler Optimization

Since test cases usually contain deliberately malformed code and the behavior of the embedded assembly is commonly unexpected by compilers, we often find that the attacking behavior of a test case is silently disarmed by compiler optimizations. To avoid this, the test suite utilizes certain code patterns and compiler directives to disable compiler optimization at precise locations rather than forcefully applying compiler flags to disabling certain optimization to all code. Here we describe some of the techniques utilized in this test suite.

When a function is simple enough or seemly dead, with or without an embedded assembly, compiler would trying to eliminate the function call by function inlining, dead code elimination, constant propagation, or even return value prediction. To prevent these optimizations, we use compiler attributes to disable the inlining of key functions. Some key variables are declared volatile to stop dead code elimination and return value prediction. In some extreme cases, key values are fed to the test case through input arguments to avoid constant propagation.

Compiler may choose to reorder instructions which breaks the assumptions in certain test cases. One of such examples is the read-GOT test shown in Listing 6. Function get_got_func() on line 3 tries to obtain the address of the GOT entry for rand(). A reliable way to get this address is to call rand() immediately after get_got_func(). The address of the corresponding PLT (procedure linkage table) entry is then saved as the return address for get_got_func(). To our surprise, some Arm variants of GCC swap the calling of rand() and the following dereference of the obtained GOT address (got), which usually leads to a segment error, resulting in an incorrect detection of a non-existent defense. To avoid such unexpected behavior, which might lead to an incorrect detection of a non-existent defense, we add a compiler barrier on line 5 to prevent instruction reorder on this particular location.

In this section, we describe the challenges encountered during the implementation and our solutions to resolve them.

6.1 Obtain Parameters at Runtime

Some test parameters are only reliably available at runtime. One such example is the offset of the return address on the stack from the stack pointer, as mentioned in Section 4.3. The value of offset depends on the ABI (application binary interface) definition of the target architecture, whether the frame pointer is pushed on the stack, and whether code instrument affects the stack, such as initializing the canary for stack smashing protection [28]. The value of this offset is therefore hardly fixed but allROP related test cases rely on this parameter.

In this test suite, the value of offset is obtained from a blind testing using return-to-wrong-call-site, which is the common prerequisite for all ROP tests, and fed to all depended tests as an input argument. As shown in Listing 2 and described in Section 4.3, the test gets an offset from input and checks whether the return address can be hijacked to a seemly valid return site main_mid. Since this offset is unknown, the test suite tries to get the correct value by launching the same test multiple times with different values of offset. Such behavior is defined in the configuration file through an extensions illustrated in Listing 5.

The list recorded in property arguments (line 6 in Listing 5) defines the input arguments for a test. Arguments are simply attached to the test case except for the special ones starting with "-r".

5.5.8 Indirect jump. Five test cases in total.

| jump-instruction-in-stack | jump-instruction-in-heap | jump-instruction-in-data | jump-instruction-in-rodata | jump-mid-func |

jump-mid-func checks whether an arbitrary code snippet existing in memory can be used by a general JOP attack. All jump-instruction-in-xxxx test cases are special cases of jump-mid-func. Similar to the tests for ROP and COOP attacks, these four tests check whether a JOP attack [12] can hijack the jump target to an injected code.

6 CHALLENGES IN IMPLEMENTATION

In this section, we describe the challenges encountered during the implementation and our solutions to resolve them.
with a direct call by calculating an offset at compile time. The result
Although some coding techniques have been applied to avoid these
visible only at runtime.

### 6.3 Interpret Test Results

It is actually a big challenge to interpret the results of test cases. As
indicated by the examples shown in Section 6.2, unexpected compiler
optimizations may fail a test case and indicate the existence of an
actually non-existent defense. In fact, the reverse could happen as well,
such as that a defense may replace a dangling pointer with a
random number pointing to a still readable memory location.
Although some coding techniques have been applied to avoid these
errors, removing all of them for all compilers is difficult. When a
test indeed fails due to a defense, it is also hard to tell who imple-
ments this defense, the compiler, the runtime library, the kernel, or
the hardware. Considering a ROP attack as an example, it might
be defeated by software implemented canary or a shadow stack,
or hardware supported pointer authentication or memory tagging.
In this test suite, two mechanisms are utilized to reduce ambiguity
and potentially warn about misinterpretation:

```
// part of main() in read-GOT.cpp
void *got = NULL;
get_got_func(&got, offset);
rand();
COMPIlER_BARRIER;
return *(uintptr_t *)(got);

// part of assembly.hpp
asm volatile("": : "memory")
```

### Listing 6: Read GOT entries

```
... // omit some code

class Fake {
public:
  virtual void virtual_func() { exit(0); }
... // omit some code
int main () {
  Base *orig = new Base();
  Fake *fake = new Fake();
  write_vtable_pointer(orig, *((void_t *)fake));
  orig->virtual_func();
  return 4;
}
```

### Listing 7: Fake VTable

```
unsigned char m[] = DIVIDE_BY_0_CODE ;
begin_catch_exception(m+4 , 0 , 0 , SIGFPE);
int rv = helper(m); // hijacted to m by ROP
end_catch_exception ();
end_catch_exception ();
exit(rv);
```

### Listing 9: Code injection (stack)

Another interesting case is related to the hijacking of VTable
pointers as illustrated in Listing 7. The genuine VTable of the victim
object orig is replaced with the VTable from an irrelevant object
fake on line 11. Supposing this replacement is successful, the fol-
lowing `orig->virtual_func()` should call the wrong function
defined in Fake which exits with a code 0. However, the compiler
seemly believes `orig->virtual_func()` should always call the
genuine virtual function and replaces the VTable based indirect call
with a direct call by calculating an offset at compile time. The result
is a failed test case with an arguably successful attack. To avoid
such compile time (possibly link time as well) optimization, we
hide the definition of the victim classes to a shared library which is
visible only at runtime.

(1) Different exit codes are used for all exiting points of the
program, such as the code 4 used on line 13 of Listing 7. Code 0 is
returned only when the test is considered successful. Exit codes for
known defenses are listed in the configuration file, such as the code
16 in Listing 8. During the test, the scheduler silents the output for
all tests returning 0 or known codes while highlighting the results
for tests returning unexpected code as a way to indicate the need
for further investigation.

(2) When a test ends with an exception, the test suite tries to
catch it with extra checks. An example (case `return-to-instruc-
tion-in-stack`) is demonstrated in Listing 9, which checks
whether the return address can be hijacked to a code injected on
stack by a ROP attack. Similar to `return-to-wrong-call-site`
(Listing 2), the actual attack is launched by `helper(m)` on line 6. On
most platforms, such attack is easily thwarted by DEP. A segment
error is thrown immediately when the address of the injected code
(m) is assigned to PC. This behavior is caught by the outer pair of
catch_exception() functions, which specifically watches the
SEGV_ACCERR error on address m. The test then exits with code 16
to indicate DEP (with test termination by exception). In the rare
condition when stack is executable, the test would succeed with
executing the code on stack. To improve the platform independence
and avoid recovery from a corrupted call stack, the test injects a
divide-by-zero instruction sequence with the division instruction on
m+4. The division would raise an exception of type SIGFPE, which
is caught by the inner pair of catch_exception(). The exit code
is then set to 0. All codes other than 0 and 16 would need further
investigation.
7 TEST RESULTS

7.1 Testing Platforms

The test suite has been applied on six platforms using three different ISAs, including Intel x86-64, Arm AArch64 and RISC-V. Intel x86-64 represents the most used ISA in personal computers (PC) and servers. Arm AArch64 is currently the most utilized ISA on smartphones. RISC-V [37] is a newly proposed and promising open architecture which has been quickly adopted by the opensource community and processor manufacturers.

Table 2 illustrates the parameters of the six platforms. For Intel x86-64, a relatively old i7-3770 with Ubuntu 16.04 and a recent Xeon 8280 with Ubuntu 18.04 are chosen as two representative platforms. We have managed to run the test suite on two Arm single board computers which we have access to. One is a Jetson Nano board with a Ubuntu 18.04 running on an Arm Cortex-A57 processor and the other is a Raspberry Pi 4B board with a Ubuntu 20.10 running on an Arm Cortex-A72 processor. Both processors comply with the ARMv8.0-A ISA but are equipped with different operating systems. As for RISC-V, we have managed to borrow a HiFive Unleashed board mounted with a SiFive u540 processor [85]. Although HiFive Unleashed was released in 2018, it is still one of the most powerful RISC-V computers ever produced. The operating system running on the HiFive Unleashed is a standard pre-compilation of the OpenEmbedded Linux [86] recommended by SiFive inc. To compensate for the lack of a relatively new RISC-V platform, we have compiled and installed all the necessary libraries in a latest Linux kernel image using buildroot [106] and run it on Spike [100], which is officially the golden reference model and simulator for the latest RISC-V ISA.

7.2 Comparison Between Platforms

To answer the question Q1 raised in the introduction, our first set of tests try to evaluate the security provided by different platforms. To produce a fair comparison, we use the default setting on all platforms. The test suite is compiled using the default GNU g++ compiler distributed by the OS with the compiler flags set as -O2 -std=c++11 -Wall. Table 3 provides a summary of the test results while detailed test results are revealed in Appendices A. Each figure in the table denotes the number of test cases succeed in the specific category. The success of a test case indicates that one type of vulnerabilities is tested exploitable due to the lack of a memory check. Consequently, a lower figure indicates better security as less tests succeed. The name and the total number of cases of each category are provided in the first column of Table 3.

7.2.1 Spatial safety. The results show that there is currently no defense detected on all platforms against the buffer overflow and memory spray attacks tested in this suite. All test cases succeed without exception or error. This reflects that, although numerous defense techniques have been proposed and some of them have been incorporated into compilers in recent years, no defense is applied by default probably due to performance concerns.

7.2.2 Temporal safety. Although most test cases related to temporal safety still pass on all platforms, all heap-based read-after-free and write-before-reclaim tests fail on platforms using GLIBC version newer than 2.32. A detailed look reveals that the memory allocation algorithm comes along with the latest C library refills the memory space with garbage during both the allocation and the release processes, which effectively prevent data leakage after free and malicious initialization for uninitiated variables. However, the new memory allocation algorithm can still be forced to relocate the same object at the same memory region released previously. UAF attacks using dangling pointers are still viable. Meanwhile, stack based UAF attacks are rarely defended.

7.2.3 Access control. To our surprise, the tests indicate that ASLR is not deployed on Intel i7-3770 and Spike. With some further investigation, both platforms do support user-level ASLR but the default compilers have the position independent executable (PIE) feature disabled by default. The test case check-ASLR would fail as expected if it is compiled with -pie -fPIE. As for the test cases reading a part of a function (read-func) or reading the content of a GOT (read-GOT), no defense is detected on any of the platforms.

7.2.4 Pointer integrity. The test suite detects no defense against maliciously reading and modifying a code pointer. Although compilers do warn about the arithmetic on a function pointer, the test case still finishes without exception. There is no defense found for protecting the VTable pointer as well. The only type of defense is related to modifying an entry in the GOT. Although GOT can be read on all platforms, they are placed on read-only pages on Intel Xeon 8280, Jetson Nano and Raspberry Pi 4B complying with the relocation read-only (RELRO) protection. Note that most Linux distributions support partial RELRO by default. For the platforms where modify-GOT succeeds, the partial RELRO fails to cover the entry for the library function (rand()) hijacked. The success of modify-GOT on HiFive Unleashed and Spike indicates potential security issues that have not been properly resolved in the latest RISC-V compilers.

7.2.5 Control-flow integrity. It seems like most CFI related defenses are disabled by default on all platforms. All tests that hijack the return address to a code exiting in memory succeed without exception. Only the code injection tests are prevented by DEP as expected. One extra benefit of using the latest RISC-V ISA (on Spike) is the failure of return-to-instruction-in-rodata which tries to execute a code injected in constant data (read-only pages). Starting from RISC-V privileged specification version 1.11 [38], read-only pages are no longer executable by default as a separate “E” flag is defined in the page table entry. Since the privileged specification adopted by HiFive Unleashed is version 1.10, such feature is not supported yet and the test succeeds just like on other platforms. However, to our surprise, the test still passes on Spike when PIE is disabled (–no-pie). Some parts of the global constant data might be put in the code section for a reduced memory footprint.

Similar to the tests for backward control-flow integrity, all tests that hijack a function pointer succeed without a hitch except for the code injection tests. The latest RISC-V provides the extra benefit of preventing code execution on read-only but non-execution pages. The current situation on the protection of VTables is worrying. It is found that not only can attackers replace a Vtable with another existing one as expected but also fabricate a table in writable memory sections such as stack, heap and global data. There is no check on whether a VTable is stored on read-only pages although
compilers are doing so to avoid direct modification. The only defense that has been found is a protection against malicious reuse of VTable pointers enforced by the memory allocation algorithm. The memory allocation algorithm does provide some protection against malicious VTable replacement. According to the result of call-wrong-func-vtable-released, when an object is released, the VTable pointer is zeroed by the memory allocator. Reusing a VTable pointer from a released object is therefore prevented.

### 7.2.6 Summary of Results
Comparing across platforms, there is currently no significant difference for the provided security with default settings while newer architectures (RISC-V) using the latest compiler and runtime libraries show marginal security benefit thanks to the support of RDSX in page tables and the protection against common heap-based UAF attacks implemented in the newer C library.

### 7.3 Test with Different Flags and Compilers
It is common that a defense is added to a compiler but disabled by default due to performance concerns. As described in Q2 and Q3 of the introduction, application designer may wish to explore their choices on different combination of compilers and defenses, and security researchers would like to evaluate the strength of a certain defense on a specific platform. The test suite would be a good tool for these kind of explorations.

For the investigation of different compiler flags, we have compiled and installed the same version of the GCC compiler (version 10.3.0) and the C library (GLIBC 2.32) on both Intel Xeon 8280 and Raspberry Pi 4B to cover Intel x86-64 and Arm AArch64. No RISC-V platform is tested in this experiment because some important defenses, such as the VTable verification (VTV) [94], have not been ported to RISC-V yet. We have also installed a latest LLVM 13 on Intel Xeon 8280 to explore the differences between compilers.

After a small survey on the available security features in both compilers, Table 4 lists the sets of compiler flags being explored:

- **Default**: Test using the latest compiler with the default compiler flags.
- **RELRO**: Similar to VTV, apply the LLVM variant of defense against COOP attacks.
- **CFI**: Similar to VTV, apply the LLVM variant of defense against all forward CFI attacks [94].
- **All**: Apply all the above defenses.
- **ASan**: Enable the full address sanitizer at runtime.
- **None**: Deliberately disable all protections, including the one applied by the kernel, such as ASLR.

Some defenses are supported in compilers by not evaluated. Intel CET [48] is supported by the latest compiler but the hardware is not ready yet. Intel MPX [76] has been removed from GCC in recent years. Arm PA [7] and Arm MTE [9] are supported in LLVM but unfortunately we do not have access to a compatible Arm platform for the test. Stack clash protection has been tested but does not affect the result.

Table 4 reveals the total number of passed test cases with different flags and compilers while more detailed results are provide in Appendix B.

For the test of using different compiler flags, it is found that enabling security features does defeat the targeted types of attacks and there is no significant difference on the effectiveness of these features on different platforms, at least for the platforms we have tested. For the default setting using GCC, Intel Xeon 8280 and Raspberry Pi 4B have exactly the same result of 142 passed tests. Compared with the results in Table 3, the hijacking of GOT entry passes on both platforms as the full protection of GOT is deliberately disabled in the compilation of the compiler, and four UAF on heap
AArch64 is marginally safer than Intel x86-64. Nearly the same AArch64 even when execution on stack is allowed. As a result, Arm VTV has exactly the same effect on both platforms that six COOP has very limited protection on both platforms because protection not only activates the full GOT protection but also ASLR RELRO tests passed for the cutables by default but arithmetic operations on function pointers enabled as the distribution provided LLVM produces non-PIE exe-
distribution provided LLVM has almost no protection compared with GCC. Enabling CFI has almost no protection according to the result; however, we believe the test suite in the current form cannot provide an accurate estimation for this protection. The implementation of CFI protection on LLVM resorts to the link time optimization and requires visibility to all definitions of virtual classes at link time. This requirement forces the static linking of class definition mentioned in Section 6.2 rather than dynamic linking through a shared library as in GCC. As a result, we suspect that all the illegal modifications on VTable pointers and function pointers are taken as valid operations by the link time analysis. Consequently, enabling all the mentioned protection using LLVM results higher number of passed tests than GCC. LLVM’s address sanitizer (ASan) is seemingly less effective than it on GCC. It catches all ROP and COOP attacks but let go COP and JOP attacks. It also fails to detect the modification on GOT entries. On the good side, it catches nearly all UAF attacks, including the UAF on stack attacks missed by GCC’s ASan. Finally, when all protections are disabled (case none), LLVM and GCC have the same result except that the test applying arithmetic operations on function pointers fails to compile on LLVM.

### 8 DISCUSSION

#### 8.1 Related Work

Computer architectures have for decades been constantly improved to satisfy our thirst for performance. To quantitatively evaluate the performance gain brought by each improvement, a number of test suites have been carefully designed and widely utilized. LINPACK [36] was introduced in the 1970s to measure the computing power for numerical linear algebra and is still used to rank today’s supercomputers. Dhystone [101] provides a suitable indicator for the general integer performance of computers. CoreMark [43] specializes in the performance of micro-controllers while the more powerful general-purpose computers are normally compared using the SPEC benchmark suite [45]. PARSEC [11] concentrates on the performance of shared memory and multi-thread applications.

Using a test suite to measure the security of a certain system is not new either. They began to appear in 2005, when two papers [51, 112] proposed to use corpora of small and synthetic buffer overflow attacks (291 in [51] and 55 in [112]) to test whether they can be detected by the then state-of-the-art software defenses, such as CRED [78] and CCured [65]. Later in 2006, BASS [71] adopted an approach similar to the SPEC CPU test suite. It contained seven relatively large test cases embedded with different types of vulnerabilities related to memory spatial safety. It then provided a framework for the automatic generation of attacks exploiting the embedded vulnerabilities. To our best knowledge, BASS was the first attempt for measuring the security of a computer platform while its scope is limited to several types of memory spatial errors. RIPE [103] is probably the most utilized security test suite for defenses related to memory safety. By exhausting the possible combinations of several attacking techniques, RIPE is able to cover 850 forms of buffer overflow and ROP attacks. It has already been extensively utilized to verify the strength of various hardware supported defenses against control-flow attacks [52, 89]. However, as PIE is enabled. The stack protection provided by LLVM has exactly the same effect as GCC. Only the test trying to fake a call frame fails. To our surprise, enabling CFI almost has no protection according to the result; however, we believe the test suite in the current form cannot provide an accurate estimation for this protection. The implementation of CFI protection on LLVM resorts to the link time optimization and requires visibility to all definitions of virtual classes at link time. This requirement forces the static linking of class definition mentioned in Section 6.2 rather than dynamic linking through a shared library as in GCC. As a result, we suspect that all the illegal modifications on VTable pointers and function pointers are taken as valid operations by the link time analysis. Consequently, enabling all the mentioned protection using LLVM results higher number of passed tests than GCC. LLVM’s address sanitizer (ASan) is seemingly less effective than it on GCC. It catches all ROP and COOP attacks but let go COP and JOP attacks. It also fails to detect the modification on GOT entries. On the good side, it detects nearly all UAF attacks, including the UAF on stack attacks missed by GCC’s ASan. Finally, when all protections are disabled (case none), LLVM and GCC have the same result except that the test applying arithmetic operations on function pointers fails to compile on LLVM.

### Table 5: Test results with different flags and compilers

|                  | Intel Xeon 8280 (GCC) | Raspberry Pi 4B (GCC) | Intel Xeon 8280 (LLVM) |
|------------------|------------------------|-----------------------|------------------------|
| Default          | 142                    | 142                   | 142                    |
| RELRO            | 141                    | 141                   | 140                    |
| Stack protection | 141                    | 140                   | 141                    |
| VTV              | 136                    | 136                   | N/A                    |
| CFI              | N/A                    | N/A                   | 141                    |
| All              | 134                    | 133                   | 138                    |
| ASan             | 8                      | 8                     | 21                     |
| None             | 155                    | 147                   | 154                    |
the fact that it uses as many as 850 test cases to cover only buffer overflow and ROP attacks indicates that reaching a full coverage by exhausting all possible combinations of vulnerabilities and attack techniques is unrealistic. This partially motivates us to produce a new testing framework.

The design of security test suites has been revived in recent years. The concept of a CPU security benchmark was introduced in [113] which proposed several testing techniques also utilized in our test suite. Unfortunately, the benchmark is not available for comparison, no detail was revealed with regard to its internal structure, and no result is provided in the paper. CONFIRM [107] was a recently proposed test suite to evaluate the compatibility and applicability of various control-flow integrity defenses for different applications but it provides very little information on the security provided by the evaluated defenses. Motivated by the lack of security evaluation by CONFIRM, CBench [55] was introduced to measure the gap between the practical security strength and the claimed security of different control-flow integrity defenses. It followed a similar approach with BASS. A total of eighteen vulnerable programs were provided in seven categories. By running the vulnerable programs and attacking them at runtime, CBench measures the security level of the applied CFI defense. Compared with the test suite proposed in this paper, CBench experiments with full-fledged attacks while overlooking the relationship between individual vulnerabilities. It concentrates on evaluating the strength of the defense mechanisms themselves but not the platform implementing them. Consequently, CBench does not need to support multiple platforms and runs only on x86-64.

8.2 Future Work

The testing framework proposed in this paper is far from finished. It would need some significant extensions to become a full-fledged test suite measuring the security supported by the processor hardware.

8.2.1 Missing test cases for memory safety. One category of vulnerabilities missing in the current test suite is related to data racing in multi-threaded applications [55]. When the integrity check on a pointer and the following pointer dereferencing do not operate atomically, an attacker running on a parallel thread might hijack the pointer just after the integrity check but before the pointer dereferencing. Currently, all test cases are single threaded. Supporting multi-threaded tests for data racing conditions is one of our immediate future works.

Test cases for DOP attacks [47] are being gradually added. The number of test cases for type confusion and malicious initialization of uninitiated variables will be substantially increased to cover all possibilities. It is also reported that a significant portion of DOP attacks violate the visibility scope of variables [68]. Applying fine-grained compartmentalization of data memory to enforce the visibility scope of variables is a promising defense against DOP attacks and is not yet fully covered by the test suite.

8.2.2 Missing test cases for other types of safety. Although important, memory safety is only one of the many categories of security that can be supported by the processor hardware. At least two other categories of defenses should be included in this test suite: hardware supported defenses against the software-based side-channel attacks and the transient attacks [19].

The software-based side-channel attacks include all side-channel or covert channel attacks that can be launched purely by software. They include both the conflict-based [108] and flush-based [109] cache side-channel attacks. They contain also the attacks causing timing channels inside the processor core by maliciously competing resources, such as the recent port smash attack [5]. Although cache side-channel attacks against the traditional level-one caches are thoroughly evaluated by [32], this test suite has not covered the more prevalent attacks against the last-level caches, cannot be easily ported to other non-x86 architectures, and still misses coverage on the new variants of side-channel attacks [14, 73, 90] targeting the recently revived randomized caches [75, 102].

The term transient execution attack was first introduced in [19] and used to summarize all attacks that exploit the speculative execution in modern out-of-order processors. It includes all variants of the Meltdown [56] and the Spectra [50] attacks. New variants of transient execution attacks [20, 96, 97] are still being found in recent years along with various new defense proposals [3, 58, 79]. A proper test suite to systematically evaluate the remaining attack vectors left by the different defenses is urgently needed.

8.2.3 Vulnerability scoring system. We still need a vulnerability scoring system to interpret the test result and translate it into a score quantitatively indicating the security supported by the processor.

Every vulnerability recorded in the common vulnerabilities and exposures (CVE) database [61] is assigned with a vulnerability score measured by the common vulnerability scoring system (CVSS) [40]. However, we cannot directly adopt this scoring system for evaluating architectural vulnerabilities as the metric used is strictly software oriented. We have also investigated the common weakness enumeration (CWE) [60] and found 58 related CWEs. By averaging the CVSS scores of the CVEs related to each CWE, we might be able to calculate an equivalent score for each test case using the existing scores from CVEs. Unfortunately, most of the 58 CWEs are linked to the test cases regarding to spatial and temporal safety of memory, while most of the control flow related test cases have no connected CWE. As a result, we cannot directly borrow the existing CVSS to score the architectural vulnerabilities. This is another open challenge that requires solutions.

9 CONCLUSION

A comprehensive and cross-platform test suite has been produced to measure memory safety. It is also our first step in producing a fully-fledged test suite to measure the security supported by the processor hardware. The initial test suite currently contains 160 test cases covering spatial and temporal safety of memory, memory access control, pointer integrity and control-flow integrity. Each type of vulnerabilities and their related defenses have been individually evaluated by one or more test cases. To show its usefulness, the test suite has been ported to six platforms using three different ISAs, including Intel x86-64, Arm AArch64 and RISC-V. According to our experiment results, most memory safety vulnerabilities are still exploitable with the default compiler settings. Enabling extra security features in compilers does defeat the targeted types of
attacks. Although address sanitizer is often a tool for debugging and not a practical production-phase protection measure, it is indeed effective in catching attacks. Comparing across platforms, newer architectures using the latest compiler and runtime libraries show marginal security benefit, at least for the platforms we have tested. Comparing between compilers, LLVM has similar security support with GCC but its address sanitizer is seemingly weaker.

AVAILABILITY
The benchmark has been open sourced on GitHub at https://github.com/comparch-security/cpu-sec-bench.

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A RESULTS FOR DIFFERENT ARCHITECTURES

✓: test passes (no defense detected);
×: test failed;
*: exception raised;
⊕: not tested due to failed prerequisites.

A.1 Spatial Safety

| Condition | Intel i7-3770 | Intel Xeon 8260 | Jetson Nano | Raspberry Pi 4B | HiFive Unleashed | Spike |
|-----------|---------------|-----------------|-------------|-----------------|------------------|-------|
| overflow-read-index-stack | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| overflow-read-index-heap | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| overflow-read-index-data | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| overflow-read-index-rodata | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| overflow-read-ptr-stack | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| overflow-read-ptr-heap | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| overflow-read-ptr-data | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| overflow-read-ptr-rodata | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| underflow-read-index-stack | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| underflow-read-index-heap | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| underflow-read-index-data | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| underflow-read-index-rodata | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| underflow-read-ptr-stack | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| underflow-read-ptr-heap | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| underflow-read-ptr-data | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| underflow-read-ptr-rodata | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

A.2 Temporal Safety

| Condition | Intel i7-3770 | Intel Xeon 8260 | Jetson Nano | Raspberry Pi 4B | HiFive Unleashed | Spike |
|-----------|---------------|-----------------|-------------|-----------------|------------------|-------|
| read-after-free-heap | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| read-after-free-alias-heap | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| write-after-free-heap | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| reallocate-heap | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| access-after-reclaim-heap | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| write-before-reclaim-heap | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| write-after-reclaim-heap | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| read-after-free-alias-stack | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| write-after-free-stack | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| reallocate-stack | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| access-after-reclaim-stack | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| write-before-reclaim-stack | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| write-after-reclaim-stack | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
A.3 Access Control

|                     | Intel i7-3770 | Intel Xeon 8280 | Jetson Nano | Raspberry Pi 4B | HiFive Unleashed | Spike |
|---------------------|--------------|----------------|-------------|-----------------|------------------|-------|
| check-ASLR          | ✓            | ×              | ×           | ×               | ×                | ✓     |
| read-func           | ✓            | ✓              | ×           | ×               | ×                | ×     |
| read-GOT            | ✓            | ✓              | ✓           | ✓               | ✓                | ✓     |

A.4 Pointer Integrity

|                     | Intel i7-3770 | Intel Xeon 8280 | Jetson Nano | Raspberry Pi 4B | HiFive Unleashed | Spike |
|---------------------|--------------|----------------|-------------|-----------------|------------------|-------|
| func-pointer-assign | ✓            | ✓              | ✓           | ✓               | ✓                | ✓     |
| func-pointer-arithmetic | ✓         | ✓              | ✓           | ✓               | ✓                | ✓     |
| read-vtable-pointer | ✓            | ✓              | ✓           | ✓               | ✓                | ✓     |
| write-vtable-pointer| ✓            | ✓              | ✓           | ✓               | ✓                | ✓     |
| modify-GOT          | ✓            | ×              | ×           | ×               | ×                | ✓     |

A.5 Control-Flow Integrity

|                     | Intel i7-3770 | Intel Xeon 8280 | Jetson Nano | Raspberry Pi 4B | HiFive Unleashed | Spike |
|---------------------|--------------|----------------|-------------|-----------------|------------------|-------|
| return-to-instruction-in-stack | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| return-to-instruction-in-heap | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| return-to-instruction-in-data | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| return-to-instruction-in-rodata | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| return-to-wrong-call-site-within-static-analysis | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| return-to-wrong-call-site | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| return-to-non-call-site | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| return-to-func | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| return-to-libc | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| return-without-call | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| call-instruction-in-stack | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| call-instruction-in-heap | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| call-instruction-in-data | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| call-instruction-in-rodata | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| call-wrong-func | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| call-wrong-func | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

B RESULTS FOR DIFFERENT COMPILER FLAGS

B.1 GCC on Intel Xeon 8280

B.1.1 Summary

|                     | Default | RELRO | Stack protection | VTIV | All | ASan | None |
|---------------------|---------|-------|------------------|------|-----|------|------|
| Spatial safety (98) | 98      | 98    | 98               | 98   | 98  | 0    | 98   |
| Temporal safety (13)| 2       | 2     | 2                | 2    | 2   | 2    | 2    |
| Access control (3)  | 2       | 2     | 2                | 2    | 2   | 2    | 2    |
| Pointer integrity (5)| 5      | 4     | 5                | 5    | 4   | 0    | 5    |
| CFI (41)            | 28      | 28    | 28               | 27   | 22  | 21   | 0    |
| Total (160)         | 142     | 141   | 141              | 136  | 134 | 8    | 155  |

B.1.2 Spatial Safety
### B.1.6 Control-Flow Integrity.

| Function                              | Default | RELRO | Stack protection | VTV  | ASan | None |
|---------------------------------------|---------|-------|------------------|------|------|------|
| spray-cross-object-stack              | ✓       | ✓     | ✓                | ✓    | ✓    | ✓    |
| spray-cross-object-heap                | ✓       | ✓     | ✓                | ✓    | ✓    | ✓    |

### B.1.5 Pointer Integrity.

| Function                              | Default | RELRO | Stack protection | VTV  | ASan | None |
|---------------------------------------|---------|-------|------------------|------|------|------|
| fun-pointer-assign                    | ✓       | ✓     | ✓                | ✓    | ✓    | ✗    |
| fun-pointer-arithmetic                | ✓       | ✓     | ✓                | ✓    | ✓    | ✗    |
| read-vtable-pointer                   | ✓       | ✓     | ✓                | ✓    | ✓    | ✗    |
| write-vtable-pointer                  | ✓       | ✓     | ✓                | ✓    | ✓    | ✗    |
| modify-GOT                            | ✓       | ✓     | ✓                | ✓    | ✓    | ✗    |

### B.1.4 Access Control.

| Function                              | Default | RELRO | Stack protection | VTV  | ASan | None |
|---------------------------------------|---------|-------|------------------|------|------|------|
| check-ASLR                            | ✗       | ✓     | ✓                | ✓    | ✓    | ✗    |
| read-func                             | ✓       | ✓     | ✓                | ✓    | ✓    | ✗    |
| read-GOT                              | ✓       | ✓     | ✓                | ✓    | ✓    | ✗    |

### B.1.3 Temporal Safety.

| Function                              | Default | RELRO | Stack protection | VTV  | ASan | None |
|---------------------------------------|---------|-------|------------------|------|------|------|
| realloc-heap                          | ✓       | ✓     | ✓                | ✓    | ✓    | ✗    |
| access-after-reclaim-heap             | ✗       | ✓     | ✓                | ✓    | ✓    | ✗    |
| write-after-reclaim-heap              | ✓       | ✓     | ✓                | ✓    | ✓    | ✗    |
| realloc-stack                         | ✓       | ✓     | ✓                | ✓    | ✓    | ✗    |
| access-after-reclaim-stack            | ✗       | ✓     | ✓                | ✓    | ✓    | ✗    |

### B.1.1 Security Controls.

| Property                              | Default | RELRO | Stack protection | VTV  | ASan | None |
|---------------------------------------|---------|-------|------------------|------|------|------|
| read-cross-object-index-stack         | ✓       | ✓     | ✓                | ✓    | ✓    | ✓    |
| read-cross-object-index-heap          | ✓       | ✓     | ✓                | ✓    | ✓    | ✓    |

### B.1.2 Pointer Integrity.

| Function                              | Default | RELRO | Stack protection | VTV  | ASan | None |
|---------------------------------------|---------|-------|------------------|------|------|------|
| read-cross-section-stack-to-heap-index| ✓       | ✓     | ✓                | ✓    | ✓    | ✓    |
| read-cross-section-stack-to-data-index| ✓       | ✓     | ✓                | ✓    | ✓    | ✓    |

### B.1.0en

| Property                              | Default | RELRO | Stack protection | VTV  | ASan | None |
|---------------------------------------|---------|-------|------------------|------|------|------|
| read-cross-frame-heap                  | ✓       | ✓     | ✓                | ✓    | ✓    | ✓    |
| read-cross-frame-ptr                   | ✓       | ✓     | ✓                | ✓    | ✓    | ✓    |

### A Comprehensive and Cross-Platform Test Suite for Memory Safety

| Feature                              | Default | RELRO | Stack protection | VTV  | ASan | None |
|--------------------------------------|---------|-------|------------------|------|------|------|
| read-cross-section-stack-to-heap-index| ✓       | ✓     | ✓                | ✓    | ✓    | ✓    |
| read-cross-section-stack-to-data-index| ✓       | ✓     | ✓                | ✓    | ✓    | ✓    |

| Feature                              | Default | RELRO | Stack protection | VTV  | ASan | None |
|--------------------------------------|---------|-------|------------------|------|------|------|
| spray-cross-frame                     | ✓       | ✓     | ✓                | ✓    | ✓    | ✓    |
### B.2 GCC on Raspberry Pi 4B

#### B.2.1 Summary.

|                        | Default | RELRO | Stack protection | VTV | All | Asan | None |
|------------------------|---------|-------|-------------------|-----|-----|------|------|
| return-to-wrong-call-site-within-static-analysis | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| return-to-wrong-call-site | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| return-to-non-call-site  | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| return-to-func         | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| return-to-lib           | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| return-without-call     | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-instruction-in-stack | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-instruction-in-heap | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-instruction-in-data | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-instruction-in-rodata | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-func-within-static-analysis | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-func         | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-mid-func           | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-num-arg-func | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-num-arg-unsigned | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-data | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-stack | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-heap | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-rodata | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-heap | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-stack | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-data | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-stack | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-heap | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-data | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-stack | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-heap | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-data | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-stack | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-heap | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-data | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-stack | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-heap | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-data | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-stack | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-heap | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-data | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-stack | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-heap | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| call-wrong-type-arg-func-data | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |

### B.2.2 Spatial Safety.

|                        | Default | RELRO | Stack protection | VTV | All | Asan | None |
|------------------------|---------|-------|-------------------|-----|-----|------|------|
| overflow-read-index-stack | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| overflow-write-index-stack | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| read-cross-frame-index | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| read-cross-page-index | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |
| write-cross-frame-index | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   | ✔️   |

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### Temporal Safety

| Operation                                      | Default | RELRO | Stack protection | VTV | All | ASan | None |
|------------------------------------------------|---------|-------|------------------|-----|-----|------|------|
| read-cross-section-rodatora-to-stack-index     | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| read-cross-section-rodatora-to-heap-index      | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| read-cross-section-rodatora-to-data-index      | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| read-cross-section-stack-to-heap-ptr           | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| read-cross-section-stack-to-data-ptr           | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| read-cross-section-heap-to-stack-ptr           | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| read-cross-section-data-to-stack-ptr           | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| read-cross-section-data-to-heap-ptr            | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| read-cross-section-data-to-data-ptr            | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| read-cross-section-data-to-stack-ptr           | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| read-cross-section-stack-to-rodatora-data-ptr  | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| read-cross-section-stack-to-rodatora-heap-ptr  | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| read-cross-section-stack-to-rodatora-data-ptr  | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| write-cross-section-stack-to-heap-index        | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| write-cross-section-stack-to-data-index        | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| write-cross-section-stack-to-data-ptr          | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| write-cross-section-data-to-stack-index        | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| write-cross-section-data-to-data-index         | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| write-cross-section-data-to-stack-ptr          | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| write-cross-section-data-to-data-ptr           | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| write-cross-section-stack-to-rodatora-heap-ptr | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| write-cross-section-stack-to-rodatora-data-ptr | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| write-cross-section-stack-to-rodatora-data-ptr | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| spray-cross-object-stack                       | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| spray-cross-object-heap                        | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| spray-cross-object-data                        | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| spray-cross-frame                              | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| spray-cross-page                              | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| spray-cross-page-heap                          | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |

### Access Control

| Operation                                      | Default | RELRO | Stack protection | VTV | All | ASan | None |
|------------------------------------------------|---------|-------|------------------|-----|-----|------|------|
| check-ASLR                                     | ×       | ×     | ×                | ×   | ×   | ×    | ×    |
| read-func                                      | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| read-GOT                                       | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |

### Pointer Integrity

| Operation                                      | Default | RELRO | Stack protection | VTV | All | ASan | None |
|------------------------------------------------|---------|-------|------------------|-----|-----|------|------|
| func-pointer-assign                            | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| func-pointer-arithmetic                        | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| read-rodatora-pointer                          | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| write-rodatora-pointer                         | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| modify-GOT                                     | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |

### Control-Flow Integrity

| Operation                                      | Default | RELRO | Stack protection | VTV | All | ASan | None |
|------------------------------------------------|---------|-------|------------------|-----|-----|------|------|
| return-to-instruction-in-stack                 | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| return-to-instruction-in-heap                  | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| return-to-instruction-in-data                  | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| return-to-instruction-in-rodata                | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| return-to-wrong-call-site-within-static-analysis| ×       | ×     | ×                | ×   | ×   | ×    | ×    |
| return-to-wrong-call-site                      | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| return-to-non-call-site                        | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| return-to-func                                 | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| return-to-lib                                  | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| return-without-call                            | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-instruction-in-stack                      | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-instruction-in-heap                        | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-instruction-in-data                        | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-instruction-in-rodata                      | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-wrong-func-within-static-analysis          | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-malicious-func                            | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-wrong-num-arg-func                        | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-wrong-type-arg-int2double                  | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-wrong-type-arg-op2double                   | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-wrong-type-arg-op2int                    | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-wrong-type-arg-dp2dp-func-stack            | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-wrong-type-arg-dp2fp-func-heap             | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-wrong-type-arg-dp2fp-func-data             | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-wrong-type-arg-dp2fp-func-rodata           | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-wrong-func-heap                            | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-wrong-func-heap                            | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-wrong-func-heap                            | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-wrong-func-heap                            | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-wrong-func-parent                          | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-wrong-func-child                           | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-wrong-func-sibling                         | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-wrong-func-heap                            | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-wrong-func-heap                            | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-wrong-func-released                        | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-wrong-func-offset                          | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-wrong-num-arg-heap                         | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
| call-wrong-num-arg-heap                         | ✔       | ✔     | ✔                | ✔   | ✔   | ☐    | ✔    |
## B.3 LLVM on Intel Xeon 8280

### B.3.1 Summary.

| Condition                        | Default | RELRO | Stack protection | CFI | All | ASan | None |
|----------------------------------|---------|-------|------------------|-----|-----|------|------|
| Spatial safety (98)              | 98      | 98    | 98               | 98  | 0   | 98   |      |
| Temporal safety (13)             | 9       | 9     | 9                | 9   | 4   | 9    |      |
| Access control (3)               | 3       | 2     | 3                | 3   | 3   | 3    |      |
| Pointer integrity (5)            | 4       | 4     | 4                | 3   | 2   | 4    |      |
| CFI (41)                         | 28      | 28    | 27               | 26  | 12  | 40   |      |
| Total (160)                      | 142     | 140   | 141              | 141 | 138 | 21   | 154  |

### B.3.2 Spatial Safety.

| Condition                        | Default | RELRO | Stack protection | CFI | All | ASan | None |
|----------------------------------|---------|-------|------------------|-----|-----|------|------|
| jump-instruction-in-stack        | ×       | ×     | ×                | ×   | ×   | ×    | √    |
| jump-instruction-in-heap         | ×       | ×     | ×                | ×   | ∗   | ×    | √    |
| jump-instruction-in-data         | ×       | ×     | ×                | ×   | ∗   | ×    | √    |
| jump-instruction-in-rodata       | ×       | ×     | ×                | ×   | ∗   | ×    | √    |
| jump-mid-func                   | ×       | ×     | ×                | ×   | ×   | ×    | √    |

| Condition                        | Default | RELRO | Stack protection | CFI | All | ASan | None |
|----------------------------------|---------|-------|------------------|-----|-----|------|------|
| read-cross-object-ptr-rodata     | √       | √     | √                | √   | √   | ∗    | √    |
| read-cross-object-index-rodata   | √       | √     | √                | √   | √   | ∗    | √    |
| read-cross-object-ptr-data       | √       | √     | √                | √   | √   | ∗    | √    |
| read-cross-object-index-data     | √       | √     | √                | √   | √   | ∗    | √    |
| read-cross-object-ptr-heap       | √       | √     | √                | √   | √   | ∗    | √    |
| read-cross-object-heap           | √       | √     | √                | √   | √   | ∗    | √    |
| read-cross-object-heap-heap      | √       | √     | √                | √   | √   | ∗    | √    |
| read-cross-object-heap-stack     | √       | √     | √                | √   | √   | ∗    | √    |
| read-cross-object-heap-heap-stack| √       | √     | √                | √   | √   | ∗    | √    |
| read-cross-object-ptr-heap-stack | √       | √     | √                | √   | √   | ∗    | √    |
| underflow-write-ptr-data        | √       | √     | √                | √   | ∗   | ∗    | √    |
| underflow-write-ptr-heap        | √       | √     | √                | √   | ∗   | ∗    | √    |
| underflow-write-ptr-stack       | √       | √     | √                | √   | ∗   | ∗    | √    |
| underflow-write-ptr-heap-stack  | √       | √     | √                | √   | ∗   | ∗    | √    |
| overflow-write-ptr-data         | √       | √     | √                | √   | ∗   | ∗    | √    |
| overflow-write-ptr-heap         | √       | √     | √                | √   | ∗   | ∗    | √    |
| overflow-write-ptr-stack        | √       | √     | √                | √   | ∗   | ∗    | √    |
| overflow-write-ptr-heap-stack   | √       | √     | √                | √   | ∗   | ∗    | √    |
| underflow-write-ptr-index       | √       | √     | √                | √   | ∗   | ∗    | √    |
| underflow-write-ptr-index-heap  | √       | √     | √                | √   | ∗   | ∗    | √    |
| underflow-write-ptr-stack-index | √       | √     | √                | √   | ∗   | ∗    | √    |
| underflow-write-ptr-index-heap-stack | √ | √ | √ | √ | ∗ | ∗ | √ |
| underflow-write-index-heap       | √       | √     | √                | √   | ∗   | ∗    | √    |
| underflow-write-index-data       | √       | √     | √                | √   | ∗   | ∗    | √    |
| underflow-write-index-stack      | √       | √     | √                | √   | ∗   | ∗    | √    |
| underflow-write-index-data-stack | √       | √     | √                | √   | ∗   | ∗    | √    |
| read-cross-object-index-stack    | ×       | ×     | ×                | ×   | ∗   | ×    | √    |
| read-cross-object-index-heap     | ×       | ×     | ×                | ×   | ∗   | ×    | √    |
| read-cross-object-index-data     | ×       | ×     | ×                | ×   | ∗   | ×    | √    |
| read-cross-object-index-stack    | ×       | ×     | ×                | ×   | ∗   | ×    | √    |

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### B.3.3 Temporal Safety

|                                | Default | RELRO | Stack protection | CFI | All | ASan | None |
|--------------------------------|---------|-------|------------------|-----|-----|------|------|
| read-after-free-org-heap       | x       |       | x                | x   | x   | x    | x    |
| write-after-free-heap          |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| reallocate-heap                | ✓       | ✓     | ✓                | ✓   | ✓   | ✓    | ✓    |
| access-after-reclaim-heap      | x       | x     | x                | x   | x   | x    | ✓    |
| write-before-reclaim-heap      | x       | x     | x                | x   | x   | x    | ✓    |
| read-after-free-alias-stack    | ✓       | ✓     | ✓                | ✓   | ✓   | ✓    | ✓    |
| write-after-free-stack         | ✓       | ✓     | ✓                | ✓   | ✓   | ✓    | ✓    |
| reallocate-stack               | ✓       | ✓     | ✓                | ✓   | ✓   | ✓    | ✓    |
| access-after-reclaim-stack     | ✓       | ✓     | ✓                | ✓   | ✓   | ✓    | ✓    |
| write-before-reclaim-stack     | ✓       | ✓     | ✓                | ✓   | ✓   | ✓    | ✓    |

### B.3.4 Access Control

|                                | Default | RELRO | Stack protection | CFI | All | ASan | None |
|--------------------------------|---------|-------|------------------|-----|-----|------|------|
| check-ASLR                      | ✓       |       | x                | x   |     | x    | ✓    |
| read-func                       | ✓       | ✓     | ✓                | ✓   | ✓   | ✓    | ✓    |
| read-GOT                        |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |

### B.3.5 Pointer Integrity

|                                | Default | RELRO | Stack protection | CFI | All | ASan | None |
|--------------------------------|---------|-------|------------------|-----|-----|------|------|
| func-pointer-assign            | ✓       | ✓     | ✓                | ✓   | ✓   | ✓    | ✓    |
| func-pointer-arithmetic        | x       | x     | x                | x   | x   | x    | x    |
| read-vtable-pointer            | ✓       | ✓     | ✓                | ✓   | ✓   | ✓    | ✓    |
| write-vtable-pointer           | ✓       | ✓     | ✓                | ✓   | ✓   | ✓    | ✓    |
| modify-GOT                     | ✓       | ✓     | ✓                | ✓   | ✓   | ✓    | ✓    |

### B.3.6 Control-Flow Integrity

|                                | Default | RELRO | Stack protection | CFI | All | ASan | None |
|--------------------------------|---------|-------|------------------|-----|-----|------|------|
| return-to-instruction-in-stack |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| return-to-instruction-in-heap  |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| return-to-instruction-in-data  |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| return-to-instruction-in-rodata|         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| return-to-wrong-call-site-within-static-analysis | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| return-to-wrong-call-site      |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| return-to-non-call-site        |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| return-to-func                 |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| return-to-libc                 |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| return-without-call            |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| call-instruction-in-stack      |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| call-instruction-in-heap       |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| call-instruction-in-data       |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| call-instruction-in-rodata     |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| call-wrong-func-within-static-analysis | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| call-wrong-func                |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| call-mid-func                  |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| call-wrong-num-arg-func        |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| call-wrong-type-arg-int2double |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| call-wrong-type-arg-op2double  |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| call-wrong-type-arg-op2intp    |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| call-wrong-type-arg-fp2dp      |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| call-wrong-type-arg-dp2fp-func-stack | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| call-wrong-type-arg-dp2fp-func-heap | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| call-wrong-type-arg-dp2fp-func-data | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| call-wrong-type-arg-dp2fp-func-rodata | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| call-wrong-func-vtable-stack   |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| call-wrong-func-vtable-heap    |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| call-wrong-func-vtable-data    |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| call-wrong-func-vtable-parent  |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| call-wrong-func-vtable-child   |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| call-wrong-func-vtable-sibling |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| call-wrong-func-vtable-released|         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| call-wrong-func-vtable-offset  |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| call-wrong-num-arg-vtable      |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| jump-instruction-in-stack      |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| jump-instruction-in-heap       |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| jump-instruction-in-data       |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |
| jump-instruction-in-rodata     |         |       | ✓                | ✓   | ✓   | ✓    | ✓    |