Design of 2.4GHz Two Stages Cascode Class E Power Amplifier for Wireless Application

Koh Siang Yi, S.A. Z Murad and S.N. Mohyar

Faculty of Electronic Engineering Technology (FTKEN), Universiti Malaysia Perlis (UniMAP), Alam Unimap Campus, 02600 Arau, Perlis, MALAYSIA.

E-mail: siangyi@studentmail.unimap.edu.my

Abstract. A low-power consumption internet-connected device has received considerable attention in recent years. Power amplifier (PA) is the most significant block in radio frequency (RF) transceivers because the PA consumes high power. Therefore, an efficient and low power consumption (PA) are necessary for wireless applications. This paper presents the design of 2.4 GHz two stage with cascode class E power amplifier for wireless application using CMOS 0.13-µm technology. The proposed design employed two stage topology with cascode class E configuration in order to achieve high efficiency. The simulation results show that the proposed PA delivers 35 % power added efficiency (PAE) and 22.6 dBm output power with 3.3 V power supply into a 50 Ω load.

1. Introduction

Nowadays, low power and low-cost wireless devices are having significant demand by the market. Transceiver plays an important role in wireless devices. A transceiver builds up by some blocks, which are power amplifier (PA), analog to digital converter (ADC), low noise amplifier (LNA), mixer, etc [1], [2]. The PA is the main part in a radio frequency (RF) transceiver because it consumes the highest power [3], [4]. Implementation of transistors in large size and inductors for PA designing will decrease the efficiency and increase power consumption at the same time.

Recently, most PA designer prefer CMOS technology as compared with BiCMOS, GaAs, GaN and SiGe technology [5]. This is because CMOS technology is low cost and high integration in RF PA design. In deep sub-micron process, low breakdown voltage causes the drain to gate voltage limited. Therefore, it is the main challenging part in CMOS PA design. Basically, the drain voltage can achieve two times than the supply voltage. Hence, low supply voltage causes the transistor to become low efficiency and low power. In a RF transceiver, PA is the last and main part in the transmitter front-end. PA is an electronic amplifier which convert a low signal power into a large signal power of RF to transmit the antenna in a transmitter [5].

The first class E PA was designed in year 1975 [6]. By theory, a class E PA can obtain 100% drain efficiency (DE), so it becomes a popular choice in PA design for researchers. This is because class E PA has simpler circuitry and high efficiency as compared to other classes of switching type Pas, which are class D and class F PA. Theoretically, switching type amplifiers are able to obtain high power added efficiency (PAE) as compared with linear amplifiers [7]. By shaping the current and voltage waveform, both waveforms will not be overlapping with each other, thus PA achieved high efficiency [7]. In general, the switching mode class E PAs are suitable for systems with constant envelop
modulation scheme, such as FSK (or FM), because of its poor linearity [8]. In summary, a well-designed CMOS PA is required in order to achieve low power consumption, long battery life and high efficiency PA which are highly demanding.

The objective of this research is to design a high efficiency CMOS PA using Silterra CMOS 0.13-\(\mu\)m technology. The proposed PA implemented two stage topology with cascode class E configuration in order to minimize the power loss, therefore increase efficiency.

The structure of this paper is arranged by four sections. Section 1 presents the introduction, Section 2 presents the analysis of the proposed CMOS PA circuit design, Section 3 provides the simulation results obtained from the proposed CMOS PA circuit design and finally the conclusion is given in Section 4.

2. Proposed CMOS PA Circuit Design

The proposed CMOS PA is designed with two-stage topology which include driver stage and power stage and cascode class E configuration at power stage. Fig. 1 shows the schematic of complete proposed CMOS PA. The input stage (driver stage) consists of one transistor, M1. While the output stage (power stage) uses two transistors M2 and M3, which arranged in cascode configuration to attain sufficient output gain and high PAE [9]. Biasing is occurred at transistor M1 and M2, while M3 undergoes self-biasing. The proposed circuit consists of one capacitor and two inductors at input stage, while three capacitors and three inductors at output stage. C1, C2 and C4 are used to block DC signal, prevent DC flow to input and allow AC signal pass to next stage [5]. C2 is for interstage matching. The combination of C1 and L1 are implemented for input matching, while C3 and L4 are implemented for output matching. L3 act as a Radio Frequency Choke (RFC), which is a basic inductor used to choke radio frequencies (AC current), while allow DC current to pass through it [5]. The proposed PA is working at 2.4 GHz. Capacitor C2 is implemented to build matching network between two stages. The independent bias supply gives more constant DC power to the proposed PA as compared with simple bias circuit structure. The supply voltage (Vdd) at driver stage is 2.5 V, while power stage is 3.3 V with bias voltage (Vdc) at driver stage is 500 mV, while power stage is 900 mV. Input and output impedances are matched to 50 ohms [10].

![Fig. 1. Schematic of complete proposed CMOS PA.](image)

3. Simulation Result

This section presents the proposed CMOS PA’s simulation results at 2.4 GHz. Cadence Virtuoso software is used to simulate the result for the proposed design. Fig. 2 presents the simulated result for
S-parameters (S11, S21 and S22). The input return loss (S11) obtained -42.3 dB, peak voltage gain (S21) achieved 28.4 dB and output return loss (S22) obtained -12.8 dB at 2.4 GHz. The simulated result for output power (Pout) and PAE at 2.4 GHz is presented in Fig. 3, the output power (Pout) is 22.6 dBm and PAE is 35%.

Fig. 2. Simulated S-Parameters.

Fig. 3. Simulated Pout & PAE vs input power.
From the simulated result, we can see that the current and voltage graph will not overlap with each other, this is the unique of class E configuration. Besides, the voltage and current will not reach peak level at the same moment, this allow a reduction for power dissipation, thus PA can attain high efficiency. The transistor’s on-resistance allow the minimum voltage to become non-zero. Fig. 4 presents the simulated drain voltage and current at the power stage.

![Graph of Current and Voltage](image)

**Fig. 4.** Transient response for drain current and drain voltage of M3.

*Table I* presents the performance summary between this work and previous literature. From the review, we can see that most of the reference employed two stage, cascode with class E topology. This is because those topologies provide high efficiency with simple circuit design. *Table I* shows that the highest PAE of previous work is 67%. This is because the author applied off-chip components in the design and operating at 1.7 GHz [11]. Although this design performed highest PAE, but off-chip components are discrete components which not built on the chip or connect externally, this also means that it is required to import another library when doing schematic design using software. In addition, PA design from reference [12] also implemented off-chip inductors and capacitors on their schematic and performed 40% PAE with 3.3 V supply voltage at 2.4 GHz.

Besides, reference [11] and [12] designed CMOS PA using off-chip component. According to [13], the design consumes high input DC power, which is 4.2 V. Moreover, the reference [14] implemented Chireix combiner which combined two PAs together, therefore the die size increase.

In this work, the designed CMOS PA using 0.13-µm CMOS technology performed 35% PAE, 22.6 dBm output power and 26 dB power gain with 3.3 V supply voltage at 2.4 GHz.

**TABLE I: PERFORMANCE SUMMARY BETWEEN THIS WORK AND PREVIOUS LITERATURE**

|           | Freq (GHz) | Tech (um) | Vdd (V) | PAE (%) | Gain (dB) | Pout (dBm) |
|-----------|------------|-----------|--------|---------|----------|------------|
| [11]      | 1.7        | 0.13      | 2.5    | 67      | -        | 23         |
| [13]      | 2.4        | 0.18      | 4.2    | 55      | 34.6     | -          |
| [15]      | 2.4        | 0.13      | 2.5    | 44.67   | 42.73    | 20.03      |
| [12]      | 2.4        | 0.18      | 3.3    | 40      | 14.3     | 21.3       |
| [14]      | 2.4        | 0.18      | 2.5    | 29.9    | 38.8     | 21.4       |
| **This work** | **2.4**    | **0.13**  | **3.3**| **35**  | **26**   | **22.6**   |
4. Conclusion
A 2.4GHz two stage with cascode class E PA for wireless application using 0.13-µm CMOS technology is presented in this paper. All circuit components were designed on-chip. The proposed CMOS PA achieved 35 % PAE, 22.6 dBm output power and 26 dB power gain with 3.3 V supply voltage at 2.4 GHz. The proposed design is suitable for wireless application. However, the results can be improved in the future.

Acknowledgment
The author would like to acknowledge the support from the Fundamental Research Grant Scheme (FRGS) under a grant number of FRGS/1/2018/TK04/UNIMAP/02/8 from the Ministry of Education Malaysia.

References
[1] Kim Joonhyung 2018 Linear CMOS power amplifier using continuous gate voltage control (Kunsan: ResearchGate) pp 337-341
[2] Chenyuan Zhao, Jian Liu, Fangyang Shen and Yang Yi 2016 Low power CMOS power amplifier design for RFID and the Internet of Things (Kansas: Elsevier) pp 157-170
[3] Mehrdad Harifi-Mood, Abolfazl Bijari, Hossein Alizadeh and Nabeeh Kandalafi 2020 A New Highly Power-Efficient Inverse Class-D PA for NB-IoT Applications (Birjand: IEEE) pp 0458-0462
[4] A. R. Ghorbani and M. B. Ghaznavi-Ghoushchi 2016 A 35.6dB, 43.3% PAE Class E differential Power Amplifier in 2.4GHz with Cross Coupling Neutralization for IoT Applications (Tehran: IEEE) pp 490-495
[5] S.A.Z. Murad, Mohd N. Md Isa, Faizah A. Bakar1 and Rohana Sapawi 2016 High Efficiency 2.4 GHz CMOS Two Stages Class-F Power Amplifier for Wireless Transmitters (Perlis: Bentham Science) pp 63-67
[6] Nathan O. Sokal, and Alan D. Sokal 1975 Class E- A New Class of High-Efficiency Tuned Single-Ended Switching Power Amplifiers (Cambridge: IEEE) pp 168-176
[7] S.A.Z Murad, R.C Ismail, M.N.M. Isa, M.M Shahimin and M.F Ahmad 2014 High Efficiency CMOS Class-E Power Amplifiers in Gigahertz Frequencies: A Review (Perlis: ResearchGate) pp 1-6
[8] S.A.Z. Murad, Ramesh K. Pokharel, Haruichi Kanaya, Keiji Yoshida and Oleg Nizhnik 2009 A 2.4-GHz 0.18-um CMOS Class E single-ended switching power amplifier with a self-biased cascode (Fukuoka: Elsevier) pp 813-818
[9] A. Azizan, S.A.Z Murad, Muhammad M. Ramli and R.C Ismail 2015 Design of a 2.4 GHz CMOS LNA using two-stage forward body bias technique for WSN application (Perlis: IEEE) pp 415-417
[10] Selvakumar Mariappan, Jagadheswaran Rajendran, Norlaili Mohd Noh, Harikrishnan Ramiah and Asrulnizam Abd Manaf 2020 Energy efficiency in CMOS power amplifier designs for ultralow power mobile wireless communication systems (Penang: ResearchGate) pp 1-16
[11] Andrea Mazzanti, L. Larcher and Riccardo Bramà 2006 Analysis of Reliability and Power Efficiency in Cascode Class-E PAs (Modena: IEEE) pp 1222-1229
[12] Ville Saari, Pasi Juurakko, Jussi Ryynanen and Kari Halonen 2005 Integrated 2.4 GHz Class-E CMOS Power Amplifier (Espoo: IEEE)
[13] Ayyaz Ali, Syed Waqas Haider Shah and Khalid Iqbal 2018 Design of an Efficient Single-Stage and 2-Stages Class-E Power Amplifier (2.4GHz) for Internet-of-Things (Rawalpindi: IEEE) pp 111-116
[14] Sichun Du and Xionghui Zhu 2016 A Low-Power CMOS Class-E Chireix RF Outphasing Power Amplifier for WLAN Applications (Changsha: Springer) pp 1547-1561
[15] Shridhar R. Sahu and Dr. A. Y. Deshmukh 2013 Design of High Efficiency Two Stage Power Amplifier in 0.13µm RF CMOS Technology for 2.4GHz WLAN Application (Nagpur:
