ATAC: A Tool for Automating
Timed Automata Construction
– Extended Version –

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Abstract. In this paper, we focus on the design of timed automata
(TA) and introduce a new tool for automating TA construction. Our
tool generates TA models from descriptions and specifications given in
structured natural language. We define a sufficient set of high-level En-
lish sentences to express system properties and specifications. From
these sentences, the tool generates a detailed TA model that can be im-
ported to a verification tool. Hence, ATAC automates TA construction,
which can be very useful especially during the initial phases of the design
process and help system designers to avoid erroneous models.

Keywords: Timed Automata · Automation · Design · Optimization.

1 Introduction

Cyber-physical systems (CPS) are everywhere and they are getting increasingly
more attention from the research community as well as the industry. As their
application areas increase, models representing CPS are getting more complex
and sophisticated. Systems with timing requirements, i.e., real-time systems
(RTS), are an essential part of CPS. Timed automata (TA) [2,3,4], a widely-
used and well-known formalism for RTS, is used for modeling, designing, and
verifying CPS. From railroad crossing systems [12,16] to cardiac pacemakers [13]
to scheduling of real-time systems [10,11,18], TA are used to model and analyze
numerous systems. Algorithms for verifying TA against formal specifications
such as temporal logics exist and implemented in various tools including UP-
PAAL [7], a widely-used tool for modeling, designing, simulating, and verifying
TA models.

As CPS get more complicated, designing reliable TA models is getting tedious
and error-prone. Since most of the RTS are safety-critical, errors in the design
of TA models are not tolerable. However, since there is no automated way of
TA design and no well-defined design procedure to follow, designing TA models
inherently requires human creativity and knowledge, which is an unavoidable
source of error and extremely dangerous for safety-critical systems.

⋆ This work has received funding from the European Union’s Horizon 2020 research
and innovation programme under the Marie Skłodowska-Curie grant agreement No
798482.
This paper. We introduce a new tool, ATAC (Automated Timed Automata Construction), to automate TA design. Our tool constructs TA models from descriptions and specifications given in structured natural language. We restrict description and specification sentences to a limited set of English sentences. The identified set of sentences are sufficient to model a system. However, they are at a high-level and implementation details are not expressed explicitly. That is, given an input sentence, ATAC extracts any implied timing, synchronization, transition description of the system as well as any implied specification the system has to follow, then constructs a TA model following these descriptions and creates queries for checking the model against specifications. Hence, the tool makes a non-trivial mapping from input sentences to TA models by taking care of any low-level design choice, i.e., clock allocations, usage of committed locations, and synchronizing TA models, without any explicit statement. We believe that our tool can be useful for initial design phases and help designers to avoid erroneous models. The tool is implemented as a Python program which outputs an XML file along with a query file (if there is any implied specification in the input sentences). The resulting XML and query files can be imported to UPPAAL.

Related Work. To the best of our knowledge, our tool is the first attempt to automate TA construction. Although, there has been lots of work done on different aspects of TA, no prior work has been focused on the automation of TA design. In [2], writers present a theoretic approach to the problem of automatic synthesis of real-time systems. In their solution, from a given set of timed models and a real-time logical specification, they check the existence of a real-time model which can yield a network satisfying given specification. In LTLMop Project [9], a set of sentences are mapped to LTL specifications for robot control by defining a formal grammar. However, no work has been done on automating TA design.

The paper is outlined as follows. Sec. 2 presents some basic definitions of TA and UPPAAL. Sec. 3 includes details of the formal grammar that is used for the input language. Sec. 4 reveals implementation details of the tool. Sec. 5 gives two examples from the tool. Finally, Sec. 6 concludes the paper.

2 Timed Automata

A timed automaton (TA) [11,15] is a finite-state machine extended with a finite set of real-valued clocks that progress monotonically at the same rate and measure the time spent after their latest resets. For a set of clocks $C$, $\Phi(C)$ is a set of clock constraints over $C$. A clock constraint $\phi \in \Phi(C)$ is given by the grammar: $\phi ::= x \leq c \mid x \geq c \mid x < c \mid x > c \mid \phi \land \phi$, where $x \in C$ and $c \in \mathbb{Q}$.

Definition 1 (Timed Automata). A timed automaton $\mathcal{A} = (L, l_0, \Sigma, C, I, T)$ is a tuple, where (i) $L$ is a finite set of locations, (ii) $l_0 \in L$ is an initial location, (iii) $\Sigma$ is a finite set of labels, (iv) $C$ is a finite set of clocks, (v) $I$ is a mapping from $L$ to $\Phi(C)$, and (vi) $T \subseteq L \times \Sigma \times 2^C \times \Phi(C) \times L$ is a set of transitions. $t = (l_s, \alpha, \lambda, \phi, l_t) \in T$ is a transition from $l_s$ to $l_t$ on symbol $\alpha$. $\lambda$ is a set of clocks reset to zero on $t$ and $\phi$ is a clock constraint tested for enabling $t$. 
Traditional TA formalism has been extended with several concepts, e.g., commited locations, synchronization channels. UPPAAL \cite{6,7,14}, a tool for modeling, designing, simulating, and verifying TA, implements extended TA. In our tool, we use some of these extensions: (i) TA models in a network of timed automata communicate through synchronization channels by sending and receiving signals and (ii) whenever a state includes a committed location, the next transition must be an outgoing transition from one of the committed locations.

3 Grammar

In this section, we define a formal grammar for constructing TA from a set of structured English sentences. In general, sentences generated by the grammar are used for the design of the system model. Some of the sentences can be mapped to temporal logic expressions for verification. There are three types of sentences: (i) initialization sentences, (ii) system sentences, and (iii) specification sentences.

We present the grammar rules in Table 1. In the table, variable names are given in box (1), grammar rules for TA and each sentence type are given in box (2), and helper rules are given in box (3). While defining a TA, an initialization sentence must be given first, then the description may continue by using both system and specification sentences. The grammar rule for a TA definition is given by $\phi_{TA}$ in box (2). In Table 1, bold font indicates variable names, italic font indicates strings appering in the rules, and $\epsilon$ is the empty string.

| temp := A TA model name |
| loc := A location name |
| synch := A signal name |
| $N$ := A natural number |

$\phi_{TA}$ := $\phi_{loc}$ $\phi_{min}$

$\phi_{min}$ := $\phi_{max}$ | $\phi_{spec}$ | $\phi_{max}$ | $\epsilon$

$\phi_{max}$ := temp can only be loc |
| temp can be $\phi_{loc}$ and it is initially loc |

$\phi_{loc}$ := $\phi_{min}$ | if $\phi_{cond}$ then $\phi_{max}$ |

$\phi_{spec}$ := it goes to loc in every $N$ |
| the time spent in loc cannot be more than $\phi_{d}$ |
| loc must be reached from loc |
| loc must be reached from loc within $N$ |

$\phi_{loc}$ := $\phi_{loc}$ |

$\phi_{max}$ := it can go to $\phi_{loc}$ from $\phi_{loc}$ |
| it can send synch and go to $\phi_{loc}$ from $\phi_{loc}$ |

$\phi_{cond}$ := $\phi_{cond}$ | $\phi_{cond}$ | $\phi_{cond}$ and $\phi_{cond}$ |

$\phi_{cond}$ := it receives synch |

$\phi_{cond}$ := the time spent after $\phi_{d}$ loc is $\phi_{cond}$ |
| the time spent after $\phi_{d}$ loc is $\phi_{cond}$ and $\phi_{cond}$ |

$\phi_{cond}$ := more than $\phi_{d}$ $N$ | less than $\phi_{d}$ $N$ | equal to $N$

$\phi_{d}$ := entering | leaving |

$\phi_{d}$ := or equal to | $\epsilon$

Table 1. Grammar Rules

3.1 Initialization Sentences

Initialization sentences are used for declaring the name of the TA model, its locations, and the initial location. In Table 1 corresponding grammar rule is given by $\phi_{init}$ in box (2). Below, we explain how ATAC interprets these sentences by presenting the high-level behavior of the tool against distinct examples.
Light can be Off, Dim, Bright and it is initially Off.

- Name of the TA model is Light.
- TA has three locations: Off, Dim, and Bright.
- The initial location of the TA is Off.

Presser can only be Pressing.

- Name of the TA model is Presser.
- TA has only one location: Pressing.
- The initial location of the TA is Pressing.

### 3.2 System Sentences

These sentences are used for declaring transitions of the TA model. Transitions may have guards of the form \( \phi \) where \( \phi \in \Phi(C) \) and they can be both sending and receiving synchronization signals. In Table 1, corresponding grammar rule is given by \( \phi_{sys} \) in box (2).

In theory, the rule for system sentences can create infinitely many sentences since \( \mathbb{N} \) appearing in the rule \( \phi_{constr} \) is a natural number and \( \phi_{cond} \) rule can be conjuncted with itself infinitely many times. Hence, below, we only explain the mappings of a small set of sentences; however, notice that, any other sentence that can be generated by the rule is a trivial extension of these.

- It can go to Dim from Off.
  - There is a transition from Off to Dim.

- It can send press and go to Dim from Off.
  - There is a transition from Off to Dim sending press signal.

- If it receives press, then it can go to Dim from Off.
  - There is a transition from Off to Dim receiving press signal.

- If it receives press, then it can send synch and go to Dim from Off.
  - There is a new committed location, assume it is uniquely named as Com.
  - There is a transition from Off to Com receiving press signal.
  - There is a transition from Com to Dim sending synch signal.

- If the time spent after entering Dim is more than or equal to 2, then it can go to Off from Dim.
  - There is a new clock variable, assume it is uniquely named as \( x \).
  - \( x \) is reset to zero on incoming transitions of Dim.
  - There is a transition from Dim to Off with the constraint \( x \geq 2 \).

- If the time spent after leaving Dim is less than 2, then it can go to Bright from Dim.
  - There is a new clock variable, assume it is uniquely named as \( x \).
  - \( x \) is reset to zero on outgoing transitions of Dim.
  - There is a transition from Dim to Bright with the constraint \( x < 2 \).
3.3 Specification Sentences

In addition to describing the TA model, these sentences also indicate specifications of the resulting system needs to satisfy. These specifications can be mapped to queries in UPPAAL and checked at the end of the design. These queries will be given to the user along with the output XML file as a separate query file. User can check whether the model satisfies the specifications implied by the sentences using the provided query file. In Table 1, corresponding grammar rule is given by \( \phi_{\text{spec}} \) in box (2). Below, we give interpretations of the specification sentences.

- **It goes to Off in every 4.**
  - There is a new clock variable, assume it is uniquely named as \( x \).
  - \( x \) is reset to zero on outgoing transitions of \( \text{Off} \).
  - \( x \) is checked in all locations except \( \text{Off} \) with the constraint \( x \leq 4 \).
  - Every location is checked whether it is graphically connected to \( \text{Off} \). If not, a transition is added to the model from that location to \( \text{Off} \).
  - **Specification Query:** \( A[] !(!\text{Light.Off and } x > 4) \)

- **The time spent in Dim cannot be more than 2.**
  - There is a new clock variable, assume it is uniquely named as \( x \).
  - \( x \) is reset to zero on incoming transitions of \( \text{Dim} \).
  - \( x \) is checked in \( \text{Dim} \) with the constraint \( x \leq 2 \).
  - **Specification Query:** \( A[] !(\text{Light.Dim and } x > 2) \)

- **The time spent in Dim cannot be more than or equal to 2.**
  - There is a new clock variable, assume it is uniquely named as \( x \).
  - \( x \) is reset to zero on incoming transitions of \( \text{Dim} \).
  - \( x \) is checked in \( \text{Dim} \) with the constraint \( x < 2 \).
  - **Specification Query:** \( A[] !(\text{Light.Dim and } x >= 2) \)

- **Dim must be reached from Off.**
  - If there is no path from \( \text{Off} \) to \( \text{Dim} \), a transition between them is added.
  - **Specification Query:** \( \text{Light.Off} \rightarrow \text{Light.Dim} \)

- **Dim must be reached from Off within 4.**
  - There is a new clock variable, assume it is uniquely named as \( x \).
  - \( x \) is reset to zero on outgoing transitions of \( \text{Dim} \).
  - \( x \) is checked in all locations except \( \text{Dim} \) with the constraint \( x \leq 4 \).
  - If there is no path from \( \text{Off} \) to \( \text{Dim} \), a transition between them is added.
  - **Specification Query:** \( \text{Light.Off} \rightarrow (\text{Light.Dim and } x <= 4) \)

As it can be observed, implementation details are not given by the input sentences. The tool extracts implied details from the sentences and constructs the model accordingly, i.e., allocation of clocks, usage of committed location, synchronizing models in a network of TA, and generating specification queries are done automatically without any explicit statement given in the input.
4 Tool Architecture

The tool is implemented as a single-threaded Python program. While the user enters input sentences, ATAC creates locations and transitions and it assigns a new clock variable for each sentence with a timing requirement uninformedly. At the end of the input, it completes details of the model according to the final structure. However, assigning a new clock for each sentence with a timing requirement causes the initial model to have too many clock variables and some of them can be redundant. To avoid such an issue, in our previous work [17], we proposed a novel clock reduction algorithm. In the tool, we implemented this algorithm and used it to reduce the number of clocks. After reducing the number of clocks and finalizing the model, the resulting TA is mapped to an XML file and its specifications are mapped a query file. Pyuppaal [8] module is used for mapping TA models to XML files.

5 Examples

In this section, we give three examples from ATAC. The first example is a gate system which consists of two TA models. The first model is the Gate which is initially open. If it receives a signal, it closes the gate for exactly ten seconds and then opens it again. The second model is the Closer which non-deterministically sends signals to the Gate. Our second example is a light system which consists of two TA models. The first TA model is called the Light which is initially off. If it receives two consecutive press signals in two seconds, then it lights bright, and if it receives only one press signal in two seconds, then it lights dim. If it receives press signal while it is dim or bright, then it becomes off. The second model is the Presser which non-deterministically sends press signals to the Light. The third example is taken from the example models provided with the UPPAAL download package. It is the train-gate model which consists of two TA models. The first model is a generic model representing a train and the second model is a gate. Since the example contains various UPPAAL extensions, i.e., integers variables, C-like functions, arrays of signals, select statements, which are not included in the scope of ATAC, the resulting model is an initial model for the design process and it can be easily modified for the final model. Notice that, other than the mentioned extensions, the output TA given by ATAC is complete and models all given features of the system. In the examples below, we give input sentences for these systems and implied specifications.

Example 1. Input: Gate can be Open Close and it is initially Open. If it receives signal, then it can go to Close from Open. If the time spent after entering Close is equal to 10, then it can go to Open from Close. The time spent in Close cannot be more than 10. Closer can only be Closing. It can send signal and go to Closing from Closing. Output TA: Fig. (a). Queries: A[]!(Gate.Close and x > 10).
Example 2. Input: Light can be Off, Dim, Bright and it is initially Off. If it receives press, then it can go to Dim from Off. If it receives press and the time spent after leaving Off is less than 2, then it can go to Bright from Dim. If it receives press and the time spent after leaving Off is more than or equal to 2, then it can go to Off from Dim. If it receives press, then it can go to Off from Bright. Presser can only be Pressing. It can send press and go to Pressing from Pressing. Output TA: Fig. 1 (b). Queries: None.

Example 3. Input: Train can be Safe, Cross, Appr, Start, Stop and it is initially Safe. It can send appr and go to Appr from Safe. If it receives stop and the time spent after entering Appr is less than or equal to 10, then it can go to Stop from Appr. If it receives go, then it can go to Start from Stop. If the time spent after leaving Stop is more than or equal to 7, then it can go to Cross from Start. If the time spent after entering Cross is more than or equal to 3, then it can send leave and go to Safe from Cross. If the time spent after entering Appr is more than or equal to 10, then it can go to Cross from Appr. The time spent in Appr cannot be more than 20. The time spent in Start cannot be more than 15. The time spent in Cross cannot be more than 5. Gate can be Free, Occ and it is initially Free. If it receives appr, then it can go to Occ from Free. It can send go and go to Occ from Free. If it receives leave, then it can go to Free from Occ. If it receives appr, then it can send stop and go to Occ from Occ. Output TA: Fig. 1 (c). Queries: A[]!(Train.Appr and x > 20), A[]!(Train.Start and x > 15), A[]!(Train.Cross and x > 5).
6 Conclusion

In this paper, we presented ATAC, a tool for automating TA construction. ATAC constructs TA models and queries from high level descriptions and specifications given in structured natural language. The generated models and formal specifications can be imported to UPPAAL for verification. We gave a brief introduction to the basic concepts of TA and UPPAAL, and then explained the grammar for the input sentences of ATAC. Finally, we gave two examples from the tool for demonstration.

References

1. Alur, R.: Timed automata. In: International Conference on Computer Aided Verification. pp. 8–22. Springer (1999)
2. Alur, R.: Principles of Cyber-Physical Systems. The MIT Press (2015)
3. Alur, R., Courcoubetis, C., Dill, D.: Model-checking in dense real-time. Information and computation 104(1), 2–34 (1993)
4. Alur, R., Dill, D.L.: A theory of timed automata. Theoretical computer science 126(2), 183–235 (1994)
5. Andersen, J.H., Kristoffersen, K.J., Larsen, K.G., Niedermann, J.: Automatic synthesis of real time systems. In: International Colloquium on Automata, Languages, and Programming. pp. 535–546. Springer (1995)
6. Behrmann, G., David, A., Larsen, K.G.: A tutorial on uppaal. In: Formal methods for the design of real-time systems. pp. 200–236. Springer (2004)
7. Behrmann, G., David, A., Larsen, K.G., Hakansson, J., Pettersson, P., Yi, W., Hendriks, M.: Uppaal 4.0. In: Proceedings of the 3rd International Conference on the Quantitative Evaluation of Systems. pp. 125–126. QEST ’06, IEEE Computer Society, Washington, DC, USA (2006)
8. Caldwell, B.: Pyuppaal. https://github.com/bencaldwell/pyuppaal (2015)
9. Cornell Verifiable Robotics Research Group: Ltlmop project page (2013), https://ltlmop.github.io/
10. David, A., Illum, J., Larsen, K.G., Skou, A.: Model-based framework for schedulability analysis using UPPAAL 4.1. In: Model-based design for embedded systems, pp. 117–144 (2009)
11. Guan, N., Gu, Z., Deng, Q., Gao, S., Yu, G.: Exact schedulability analysis for static-priority global multiprocessor scheduling using model-checking. In: Proc. of SEUS. pp. 263–272 (2007)
12. Heitmeyer, C., Lynch, N.: The generalized railroad crossing: a case study in formal verification of real-time systems. In: 1994 Proceedings Real-Time Systems Symposium. pp. 120–131 (Dec 1994)
13. Kwiatkowska, M., Mereacre, A., Paoletti, N., Patanè, A.: Synthesising robust and optimal parameters for cardiac pacemakers using symbolic and evolutionary computation techniques. In: Abate, A., Šafránek, D. (eds.) Hybrid Systems Biology. pp. 119–140. Springer International Publishing, Cham (2015)
14. Larsen, K.G., Pettersson, P., Yi, W.: Uppaal in a nutshell. International Journal on Software Tools for Technology Transfer (STTT) 1(1), 134–152 (1997)
15. Larsen, K.G., Yi, W.: Time abstracted bisimulation: Implicit specifications and decidability. In: International Conference on Mathematical Foundations of Programming Semantics. pp. 160–176. Springer (1993)
16. Wang, F.: Formal verification of timed systems: a survey and perspective. Proceedings of the IEEE 92(8), 1283–1305 (Aug 2004)
17. Yalcinkaya, B., Aydin Gol, E.: Clock reduction in timed automata while preserving design parameters. In: Proceedings of the 7th Conference on Formal Methods in Software Engineering. p. to appear. IEEE/ACM (2019)
18. Yalcinkaya, B., Nasri, M., Brandenburg, B.B.: An exact schedulability test for non-preemptive self-suspending real-time tasks. IEEE/ACM Design, Automation and Test in Europe (DATE) (2019)