Automated Analysis of Multi-View Software Architectures

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ABSTRACT
Software architectures usually are comprised of different views for capturing static, runtime, and deployment aspects. What is currently missing, however, are formal validation and verification techniques of multi-view architecture in very early phases of the software development lifecycle. The main contribution of this paper therefore is the construction of a single formal model (in Promela) for certain stylized, and widely used, multi-view architectures by suitably interpreting and fusing sub-models from different UML diagrams. Possible counter-examples produced by model checking are fed back as test scenarios for debugging the multi-view architectural model. We have implemented this algorithm as a plugin for the Enterprise Architect development tool, and successfully used SPIN model checking for debugging some industrial architectural multi-view models by identifying a number of undesirable corner cases.

KEYWORDS
multi-view architecture analysis, SPIN model checker

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1 INTRODUCTION
Software architectures usually are comprised of different views for capturing static, runtime, and deployment aspects [1, 4]. The static/component view describes the logical decomposition of the system into building blocks (e.g., packages, components, classes), whereas the runtime view describes the behavior and interaction of the building blocks as runtime elements in the running system, using diagrams such as sequence diagrams, activity diagrams, or state machines, and the deployment view shows how software is assigned to hardware processing and communication elements.

In the current state-of-the-practice, architectural models are analyzed in early phases in the software development cycle, mainly by means of manual and resource-intensive review frameworks such as the Architectural Trade-off Analysis Method (ATAM) [4]. What is currently missing, however, are formal analysis techniques of multi-view architectures for early and automated detection of, say, unwanted behavior due to under-specification.

In this paper, we therefore reconstruct a single model of a multi-view architecture, which is suitable for formal analysis, by fusing sub-models of different views in UML diagrams [15], as provided, for example in architectural development tools such as Enterprise Architect. Our fusion algorithm proceeds by taking deployment views as skeletons to offer basic communication structure over processes and channels in the actual system. The concrete behavior of each deployed software component — as documented in the static view — is captured by run-time views. One notable challenge is to cope with under-specification among views, as dynamic architectural views often only capture certain scenarios but not the complete component behavior and all possible interactions. To this end, semantic extrapolation is needed for constructing a model-checkable verification model and we enumerate possible extrapolation strategies.

We have implemented our fusion algorithm as a plug-in for Enterprise Architect (EA). This plug-in generates verification models in the Promela language, which are used as inputs to the SPIN model checker [6]. Counter-examples generated by the model-checkers are used as test cases for debugging the multi-view architectural model. We evaluated this EA plug-in in early phases of developing two mission-critical distributed software systems in industrial projects, and successfully identified undesired corner cases due to under-specification in the model.

(Related work) There is a rich literature on the verification of UML-like diagrams. For example, refinement of activity diagrams has been based on LTL model checking [13], and state machine diagrams have been translated to hierarchical automata as the basis for model checking [11, 14, 16]. Moreover, sequence diagrams have a straightforward correspondence to communicating processes and process algebras [3, 10, 17]. Use case diagrams can be checked for consistency or containment by means of viewing them as programs with constraints [7] or by a translation into activity diagrams [8]. Lastly, using annotations such as UML Marte profile [5], one may verify extra-functional properties such as timing [12]. In contrast to these approaches we are analyzing multi-view architectural models, which include static, runtime, and deployment views, being restricted to a certain stylized use and linking between
views. We therefore do not address or even try to solve the general multi-view consistency problem under UML [9].

2 MULTI-VIEW SOFTWARE ARCHITECTURE AND VIEW LINKING

Using architectural development tools such as Enterprise Architect (EA), the designer may maintain links among multiple views by creating components in the static view, by building runtime and deployment view using components in the static view, and by associating each diagram with a component or a sub-structure.

Figure 1 illustrates these concepts using a simple architectural example. There are three software components SC1, SC2, and SC3 in the static view. In the deployment view, three devices Device1, Device2, Device3 are included in the final deployed system, where for each device, the underlying software components are created (using drag-and-drop in EA) as an instantiation of components in the static view. For example, for the Device2 in Figure 1, C2 is an instance of the software component SC1 from the static view.

For each software component in the static view there is a state machine or activity diagram in the behavioral view, where each of the states provides behavioral scenarios for different execution modes (for example, normal and error modes). Behavior and interaction in each state (or mode) are expressed in terms of scenarios expressed as sequence diagrams. In Figure 1, for example the behavior of component SC1 is refined to StateMachine1, where internally, State1 is further refined into SequenceDiagram1. Notice also that in SequenceDiagram1, the actor act0 is surrounded by a dashed component. This is often used in UML modeling as a modeling trick to capture system boundary. Such a boundary allows modeling the interaction of multiple instantiations of the same component, as commonly seen in fault-tolerant systems where redundancy and distributed voting are applied.

Table 1: Constructs in verification model and their corresponding formulation in Promela.

We are now providing a formal signature for these multi-view architectural concepts; hereby, A,B is used to denote the projection of A with respect to B. A multi-view architectural model Arch is a triple ⟨ComponentView, RuntimeView, DeploymentView⟩. ComponentView consists of set of software components where SCi ∈ ComponentView can again be refined to a set of components; for expressing, for example, a "uses" structure. For the purposes of this paper, such a hierarchical component view can always considered to be in flattened form. The DeploymentView is a pair ⟨Devices, Network⟩ of sets. First, every device Devicei ∈ Devices is a set itself of instantiated software components, and for every Ci ∈ Devices is of type SCj where SCj ∈ ComponentView. We use Ci.type to denote the typing information. Second, pairs of devices Devicei, Devicej ∈ Network, where Devicei, Devicej ∈ Devices, are interpreted as directed (from left-to-right) edges between devices. Finally, the RuntimeView is a quadruple ⟨StateMachine, SequenceDiagrams, mapSC → State, mapState → Seq⟩.

- StateMachines is the set of state machines with each element SMi := statesi, s0i, transi having a set of states statesi, an initial state s0i, and the set of transitions transi. We use SMi.s to denote a state s in state machine SMi.
- SequenceDiagrams is the set of sequence diagrams. Again for simplifying formulation, let elements in sequence diagrams be variable-free, straight-line (i.e., no if-else or while) programs. An element SeqDiagram ∈ SequenceDiagrams is a tuple Act, act0, where Act is the set of actors and act0 is the one that is in the system boundary (cf. act0 in Figure 1). Each actor acti ∈ Act is a tuple ⟨typei, Msgi⟩ where typei ∈ ComponentView indicates the typing of the actor by referencing the element in component view, and Msg is the finite concatenation of messages msg0, msg1, ..., msgk, where for all j = 0, ..., k, msgj ∈ {!, ?} × {syn, asyn} × Σ → Act. In message msgj, {!, ?} indicates if the message is being sent
Algorithm 1: View fusing algorithm

Input : Multi-view architecture model
             (ComponentView, RuntimeView, DeploymentView)
Output : Verification model: Processes, Channels, Messages

foreach SeeDiagram ∈ SequenceView.SequenceDiagrams do
    for act = SC_i, Msg ∈ SeqDiagram.Act do
        Messages := Messages ∪ Msg;
    endforeach
foreach Device_i, Device_j ∈ DeploymentView.Network do
    Channels := Channels ∪ {ChanDevice_i→Device_j}
endforeach
foreach Device ∈ DeploymentView.Network do
    for C_j, C_k ∈ Device, do Channels := Channels ∪ {ChanC_j→C_k};
    endforeach
foreach Device, ∈ DeploymentView.Network do
    foreach C_j ∈ Device, do
        let SM_j = mapSC→SM(C_j,type);
        let Pr_i = (Goto{so_i}), where so_i be the initial state of SM_j;
    endforeach
    Process State s ∈ SM_j, states do
        if κ = "!" then
            Pr_j := Pr_j · (ChanC_j→C_k !0), where C_k ∈ Device_j s.t.
            C_k.type = act’.type;
        elseif κ = "?" then
            Pr_j := Pr_j · (ChanDevice_i→Device_k ?0), where
            C_k ∈ Device_k s.t. i ≠ j and C_k.type = act’.type;
        else
            Pr_j := Pr_j · (ChanDevice_i→Device_k ?0), where
            C_k ∈ Device_k s.t. i ≠ j and C_k.type = act’.type;
        /\ Jump to successor in state-machine diagram.
        end
        Processes := Processes ∪ {Pr_i};
end

(!) or received (?), \{syn, asyn\} indicates synchronous/asynchronous message passing, \Sigma is used to capture all possible message contents, and the last item is the entity being communicated. Consider act0 in Figure 1, it is represented as \(SC_1, act0\), \{act0\}. For the example in Figure 1, we use the generated verification model to explain the concept, where Messages is the set of messages, Channels is the set of (synchronous or asynchronous-with-fixed-buffer) channels, and Processes is a set of processes. Hereby, each process Process is a sequence of atomic actions, including labels, non-deterministic goto primitives, and message send/receive. The semantics of a verification model is based on Promela [6]. For the purpose of reference, however, we are listing some correspondence of constructs in the architectural model and corresponding verification models in Table 1.

3 MULTI-VIEW FUSION

Based on signatures for multi-view architectural models as defined above, we are now describing the process of providing a behavioral semantics based on fusing multiple views. A verification model is a triple Messages, Channels, Processes, corresponding to the formal definition of a multi-view architecture in Figure 2 to explain the concept, where comments in Figure 2 indicates corresponding actions done
in Algorithm 1. Notice that the presentation of the translation algorithm is simplified in that it does not support variables, branches and loops. These kinds of extensions are straightforward and are also supported in our prototype implementation.

Most interestingly, lines 16-20 in Figure 1 make various assumptions about the architectural model under consideration, and semantic extrapolation is used to determine choices being made during the translation. Such a semantic extrapolation, due to lack of proper semantics in (combining) UML and sometimes due to underspecification in modeling, can be explicitly stated and controlled. Table 2 enumerates some important cases and corresponding strategies for semantic extrapolation in order to complete translation.

4 EVALUATION AND CONCLUDING REMARKS

We have implemented a plug-in for the Enterprise Architect development tool based on the presented translation. We summarize our findings on using this tool in the architectural design and analysis for two industrial developments.

- The first case study is a modular adaptive automotive runtime environment. Since this platform has been designed to be fault-tolerant, we annotate possible faults in the deployment view, such as power-outage of a device (fail silent) or lost communication messages. Our tool translates these faults annotation by non-deterministically injecting faults into the generated verification model. In one deployment scenario, a counter-example generated by the SPIN model checker demonstrates that the overall system does not function correctly whenever there are certain faults during start-up, thereby preventing consensus to be reached between computing nodes.

- Our second case study is a control automation architecture based on the concept of micro-services and a cloud platform. Again, test cases as generated from SPIN model checking of the fused Promela model were instrumental in debugging and improving the design at an early phase in the development.

On the other hand, we have also been experiencing a number of "automation surprises" due to implicit assumptions on the architecture and the generated fused model. For example, the fused model does not capture the fact that service handlers may be viewed as a non-terminating while-loop program that can handle various requests using switch statements, even though (at least) some designers made such an implicit assumption. These kinds of automation surprises might be hard to avoid when applying formal analysis to architectural notations with ambiguous semantics.

It would be most interesting to specify some of the encodings presented here also in a theorem proving environment such as PVS, and to experimentally compare the proposed semantic extrapolation of the behavior of architectural designs with logic- and constraint-based approaches for partially specified systems.

| Under-specification scenarios | Mitigation strategies |
|------------------------------|-----------------------|
| In the deployment view, allow components within a device to communicate with each other? | Allow / Disallow / Trigger the designer for actions |
| Operation over variables both in a state of a state-machine diagram and in the refinement sequence diagram of that state? | Variable operations over variables in a state should appear (before) after actions in sequence diagram |
| Unclear requirement in communication buffer size, for asyn. communication? | Use pre-defined value / Trigger the designer for actions |
| An actor sends to one entity in the sequence diagram, while multiple receivers exists in the deployment view? | Send to all entities / Send to one randomly selected entity / Trigger exception |

Table 2: Semantic extrapolation for handling under-specification in diagrams; the underlined items are strategies used in creating the Promela model in Figure 2.

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