Hierarchical Single-Objective Model Predictive Control with Reduced Computational Burden in Cascaded H-Bridge Converter based on 3-level Flying Capacitor Unit Cell

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This research was supported by the Korea Electric Power Corporation under Grant R20X002-4.

ABSTRACT This paper presents a control algorithm to reduce the computational burden of model predictive control in a grid-connected single-phase N-cell cascaded flying capacitor H-bridge (CFCHB) multilevel converter of a solid-state transformer. The proposed control algorithm is a finite-control-set model predictive control (FCS-MPC) that is based on a hierarchical structure controlling the grid current, DC-link voltage, and flying capacitor voltage, using each cost function through three layers. Unlike the conventional multi objective cost function that evaluates and compares all candidates to determine the optimal state, the proposed method uses a single-objective cost function by separating the control variables to determine the optimal state through calculation without comparison. Therefore, the amount of computation is significantly reduced compared with that of the conventional method, and the execution time is shortened. Thus, the sampling period can be shortened and the switching frequency can be increased. Further, it can lead to using a smaller inductor to produce a high-quality grid current, which can help reduce the system size and cost. The execution time is not large, even if the voltage level increases and the effect of time reduction is large compared to the existing method, because the computational burden of the proposed method is linearly proportional to the number of cells. The voltage level expansion is easy and suitable for digital system implementation, and the control performance is not affected. The effectiveness of the proposed method is verified through the simulation of a single-phase 250 kW 9-cell CFCHB multilevel converter using PSIM and an experiment with a single-phase 2 kW 3-cell CFCHB multilevel converter at the laboratory scale.

INDEX TERMS Finite-control-set model predictive control (FCS-MPC), cascaded flying-capacitor H-bridge, multilevel converter, solid-state transformer (SST)

NOMENCLATURE

| Symbol | Description |
|--------|-------------|
| N      | The number of unit cells |
| Vg     | Grid voltage |
| ig     | Grid current |
| Lg     | Grid reactor |
| Rg     | Parasitic resistance of grid line |
| Vọf    | Total AC-side terminal voltage |
| nọf    | Total AC-side terminal voltage level |
| Vọ     | AC-side terminal voltage |
| nọ     | AC-side terminal voltage level |
| Vọpj   | Pole voltage |
| nọpj   | Pole voltage level |
| k      | Timing at the instant of sampling |
| Vfpj   | Flying capacitor voltage |
| Vdj    | DC-link voltage |
| Vdc,avg| Average DC-link voltage |
| Tpj    | Switching state of the power device |
| ipj    | Current flowing through the power device |
| ippj   | Current flowing through a flying capacitor |
| nọr    | The number of remaining cells |
| nọj    | Remaining AC-side terminal voltage levels |
| nọj,lim| Upper limit bound of voltage level |
| nọj,min| Lower limit bound of voltage level |
| Kpj    | Difference between the two switching states |
| Ts     | Sampling period |
I. INTRODUCTION

Global interest in low-carbon emissions has grown recently, and the transition to eco-friendly vehicles, especially electric vehicles (EVs), has witnessed rapid progress [1]. EVs convert electricity to power; no pollutants are emitted during this process, and the power conversion efficiency is superior to that of internal combustion engine vehicles. However, EVs are faced with challenges such as insufficient charging infrastructure and an excessively long charging time compared with gasoline. A DC extreme fast charging (XFC) station that connects a solid-state transformer (SST) to the MV line for fast charging has been studied to compensate for these shortcomings [2]-[3]. The low-frequency transformer (LFT) can be replaced by a high-frequency transformer (HFT), which is a cascade structure with a three-level full bridge (HFT) because of the SST structure, thereby reducing the system size. Thus, it is possible to install more charging ports in the same area, and faster charging can be achieved owing to the higher power capacity of the charger. Further, the number of power converters is reduced compared to the existing charging stations because there is no need for an AC/DC converter per charger, which increases efficiency and reduces installation costs [4].

The SST structure in the XFC Station consists of two stages. Stage 1 converts AC to DC as an active rectifier and performs power factor correction (PFC) through active power control; it also enables bidirectional power transmission. Stage 1 is composed of a multilevel converter using a high-voltage power device because it is connected to an MVAC.

A modular isolation architecture, which is a structure with several independent DC sources, can be easily replaced in the case of failure and provides scalability in terms of voltage and current compared to a single isolation architecture structured with a common DC source; this is because the unit cell is connected in cascade in the form of a module. The cascaded H-bridge (CHB), which is a representative topology among modular isolation architectures, has been widely used because it can employ the control method applied to the two-level converter [5]-[6]. However, there is a disadvantage in that the number of HFTs increases with an increase in the number of DC sources, i.e., the system size and weight increase with an increase in the number of unit cells.

The number of cells and HFTs can be reduced compared to CHB by cascading the unit cell structure using a three-level topology instead of a two-level full bridge to compensate for this drawback [7]-[8]. Among the three-level topologies, a flying-capacitor converter (FCC) is superior in terms of efficiency because there is no diode, unlike a neutral-point clamped converter (NPC); further, it is relatively easy to control the FCC because its structure is not complicated [9]. It is difficult to control the flying capacitor (FC) voltage because the switching frequency is limited to achieve high efficiency in high-voltage applications. However, with the recent advent of wide-bandgap power devices, it is now possible to increase the switching frequency by applying SiC MOSFETs to SST [10]-[12]; thus, the FC voltage control performance can be improved.

A cascaded flying capacitor H-bridge (CFCHB), which is a cascade structure with a three-level FCC full bridge as a unit cell, can be considered a good alternative in terms of easy voltage level expansion, size, and price.

Finite-control-set model predictive control (FCS-MPC) can be easily applied to nonlinear systems based on its intuitive characteristics; it does not require pulse-width modulation. Therefore, they have recently attracted considerable attention in the field of power electronics with a limited number of switchings [13]-[15]. However, FCS-MPC requires a large number of calculations because it is an online optimization problem. Furthermore, it should be completed within a short sampling period, which limits its implementation on hardware platforms. A multilevel converter with a large number of redundant states to be compared because of a large number of power devices suffers from the problem of limiting the switching frequency. This is attributed to a long sampling period when applied in a real-time hardware platform because of the large amount of calculation, which lowers the current quality. Thus, research has been conducted to reduce the calculation time by efficiently reducing the number of calculations.

FCS-MPC can be implemented with the field-programmable gate array (FPGA) that can reduce the execution time by using parallel operation [16]-[18]. However, this benefit can only be achieved using an FPGA. The most important approach for reducing the computational burden is to decrease the number of comparisons. The number of comparisons can be reduced by targeting only adjacent voltage levels [19]-[21] and by applying FCS-MPC to each unit cell in a two-cell CFCHB [22]. Algorithms based on FCS-MPC using dynamic programming [23], a pipeline scheme for one cell by one cell [24], and a simplified branch and bound [25] for CHB are presented. However, the cost function comprises multiple control objectives that include current and voltage control, and therefore, laborious tuning and trade-offs are inevitable because of the weighting factor. A method for separating the cost function for current and voltage control using stratification has been studied to eliminate weighting factors [26]-[28]. The weighting factors disappear because the...
This paper proposes a single-objective model predictive control based on a hierarchical structure for a single-phase N-cell CFCHB for the active rectifier of SST to overcome the above problems. Unlike the conventional control method based on a hierarchical structure, in the proposed method, the cost function still comprises multi objective variables; therefore, the number of comparisons increases exponentially when the voltage level increases, significantly increasing the computational burden.

The dynamic characteristics equation of the grid current $i_g$ can be expressed using Kirchhoff’s voltage law as

$$v_g = L_g \frac{di_g}{dt} + R_g i_g + v_{oT}$$  

Assuming that the input and output powers of each cell have no loss in the converter, the input and output powers are the same according to the law of the conservation of energy. Therefore, the dynamic characteristics equation of $V_{dij}$ can be expressed as

$$v_{dij} i_g = V_{dij} C_{di} \frac{dV_{dij}}{dt} + \frac{V_{dij}^2}{R_{dij}}$$  

where $C_{di}$ represents the DC-link capacitance and $R_{dij}$ represents the load of the $j$-th unit cell. The current flowing through the power device is determined using $T_{pil}$ and $i_g$. The current flowing through the power device in leg $A$ $i_{a0j}$ can be expressed by (5). The current flowing through the power device in leg $B$ $i_{b0j}$ can be expressed by (6).
because the direction of the grid current flowing through the power device in leg $B$ is opposite to that of leg $A$.

$$i_{gb} = T_{gb} i_a$$
$$i_{lg} = -T_{lg} i_a$$

According to Kirchhoff’s current law, the current flowing through an FC $i_{fb}$ is obtained by the switching states of the two upper power devices adjacent to the FC, as indicated in (7)–(8). Therefore, it is essential to select appropriate switching states that satisfy the charge balance to control the FC voltage because the direction of the current flowing through the FC is determined according to the two upper switching states connected to the FC.

$$i_{fb} = \left( T_{ib2} - T_{ib1} \right) i_a$$
$$i_{fb} = \left( T_{ib1} - T_{ib2} \right) i_a$$

The current flowing through the FC can be expressed as the dynamic characteristics equation of the FC voltage as

$$i_{f} = C_i \frac{dV_{f}}{dt}$$

where $C_i$ denotes the FC capacitance.

### III. PROPOSED ALGORITHM BASED ON FCS-MPC

Fig. 3 shows a block diagram of the proposed algorithm. The proposed block diagram shows an analog-to-digital (A/D) conversion block, a power control block, and a hierarchical FCS-MPC block. In the A/D block, $i_b$, $v_{fb}$, $V_{b6}$, and $V_{ff}$ are converted to digital values represented by $i_{gb}^k$, $v_{fb}^k$, $V_{b6}^k$, and $V_{ff}^k$, respectively; here, $k$ represents the time at the instant of sampling. In the power control block, the error between the average of all DC-link voltages and the command voltage of the DC-link voltage $V_{dfc}^*$ generates the d-axis grid current command $I_d^*$ through the PI controller. The phase angle of the grid voltage $\theta^*$ is estimated using $v_{fb}^k$ and the phase-locked loop (PLL). The grid current command $i_d^*$ is created by synchronizing $\theta^*$ with $I_d^*$.

The hierarchical structure of the FCS-MPC block comprises three layers. Layer I determines the optimized total AC-side terminal voltage level $n_{df}^k$ to control the grid current. Layer II determines the optimized AC-side terminal voltage level of the $j$-th cell $n_{oj}^k$ for regulating $V_{dj}$. The cell priority $P_c$ is evaluated using a sorting algorithm to determine the voltage level for one cell. Finally, Layer III determines the switching states suitable for maintaining the FC voltage balance by separating $n_{oj}$ into each leg.

#### A. LAYER I: GRID CURRENT CONTROL

The differential term of (3) is transformed into a discrete-time model using the forward Euler method (10) to control the grid current using the FCS-MPC. A discrete-time model for $i_b$ is derived as (11) by substituting (10) into (3), and the grid current after one sampling period $i_{gb}^{k+1}$ can be predicted as

$$\frac{di_b}{dt} = \frac{i_b^{k+1} - i_b^k}{T_s}$$

It is necessary to use a predicted value after two sampling periods to compensate for the computational delay that occurs in digital hardware platforms [29]. The grid current after two sampling periods $i_{gb}^{k+2}$ can be expressed as

$$i_{gb}^{k+1} = 1 - R \frac{T_c}{L_g} i_b^k + T_c \left( v_{fb}^k - \frac{1}{2} \sum_{j=1}^{N} V_{dcj} n_{oj}^k \right)$$

The error between $V_{dcj}$ and $V_{dfc}^*$ is assumed to be small; therefore, $V_{dcj}$ is equal to the average of all $V_{dcj}$ values. The sum of the output voltage levels of all cells is $n_{b6}$ and therefore, by substituting (14) into (13), $i_{gb}^{k+2}$ can be expressed by (15).

$$\nu_{oj}^{k+1} = \sum_{j=1}^{N} n_{oj}^{k+1}$$

$$i_{gb}^{k+2} = 1 - R \frac{T_c}{L_g} i_b^k + T_c \left( v_{fb}^k - \frac{1}{2} V_{dcj}^* n_{oj}^k \right)$$

Like $i_b^{k+1}$, a discrete-time model of $V_{dcj}$ can be predicted using the forward Euler method (16). $V_{dcj}^{k+2}$ can be predicted using (17) by substituting (16) into (4) and rearranging it. The
average DC-link voltage after one sampling period, $V_{dc,avg,k+1}$ (18), can be obtained using $V_{dc,k+1}$.

$$\frac{dV_{dc}}{dt} = \frac{V_{dc}^{k+1} - V_{dc}^k}{T_d}$$

(16)

$$V_{dc}^{k+1} = \frac{T_s}{C_{dc}} \left( \frac{n_{dc}^{k+1}}{2} - \frac{V_{dc}^k}{R_{dc}} \right) + \frac{T_s}{C_{dc}} \left( \frac{V_{dc}^{k+1}}{R_{dc}} - \frac{V_{dc}^k}{R_{dc}} \right)$$

(17)

$$V_{dc,avg}^{k+1} = \frac{1}{N} \sum_{j=1}^{N} V_{dc}^{k+1}_j$$

(18)

$\theta$ is estimated using PLL. $\theta$ is expressed in the form of the cosine of the grid peak voltage $V_g$ and $\theta$ as

$$v_g^k = V_g \cos(\theta)$$

(19)

The grid frequency is fixed at 60 Hz, and therefore, the phase angle of the grid voltage after one sampling period is equal to $\theta$ plus $\omega T_d$; therefore, $v_g^k$ is expressed as

$$v_g^k = V_g \cos(\theta + \omega T_d)$$

(20)

According to (15), $i_{g,k+1}$ can be predicted using $i_{g,k+1}$, $V_{dc,avg,k+1}$, $V_{dc,k+1}$, and $n_{oj,k+1}$. Substituting (12), (18), and (20) into (15), $i_{g,k+1}$ is determined only by $n_{oj,k+1}$. A single-objective cost function $J_g$ that shows the error between the average DC-link voltage and $V_{dc,k+1}$ is defined in (21) to control the grid current and to determine $n_{oj,k+1}$ that minimizes the error.

$$J_g = (i_{g}^* - i_{g,k+1})^2$$

(21)

$J_g$ is a quadratic function of $n_{oj,k+1}$ because $i_{g,k+1}$ has only one variable, i.e., $n_{oj,k+1}$. Therefore, the global minimum of $J_g$ is at the critical point at which the partial derivative becomes zero. The optimized $n_{oj}$ can be obtained as an integer value close to the critical point using the ceiling function because $n_{oj}$ is an integer type. To prevent out-of-range errors, the optimal $n_{oj}$ is limited to the feasible region: $-2N \leq n_{oj} \leq 2N$.

$$\min J_g(n_{oj}) \text{ s.t. } n_{oj} \in [-2N, 2N]$$

(22)

$$n_{oj,ceil}^{k+1} = \left\lceil \frac{2}{V_{dc,avg,k+1}} \left( \frac{L^c}{R} i_{g,k+1} + v_{g,k+1} - \frac{L_o}{T_e} i_{g,k+1} \right) - 0.5 \right\rceil$$

(23)

$[x]$ represents the ceiling function and is the smallest integer greater than or equal to the real number $x$; $[x] = \min \{x \in \mathbb{Z}: x_i \geq x \}$.

B. LAYER II: DC-LINK VOLTAGE CONTROL

In the proposed algorithm, Layer II consists of two steps to select $n_{oj}$ using the greedy algorithm.

1) SORTING TO SET THE PRIORITY OF CELLS

The priority of the cells is determined by the DC-link voltage error to control $V_{dc,j}$. The sum of $n_{oj,k+1}$ should be $n_{oj,k}^t$, which was determined in Layer I, and therefore, the probability that there is no best option in terms of DC-link voltage control increases as the priority order returns. Therefore, the larger the DC-link voltage error, the higher is the priority order. The priority order is determined by sorting the DC-link voltage error of the cells in descending order using quick sort with divide and conquer.

2) DETERMINING THE OUTPUT VOLTAGE LEVEL FOR EACH CELL

The DC-link voltage after two sampling periods $V_{dc,k+2}$ is predicted to determine $n_{oj}$ using (17) as

$$V_{dc}^{k+2} = V_{dc}^{k+1} + \frac{T_s}{C_{dc}} \left( \frac{n_{oj}^{k+2}}{2} - \frac{V_{dc}^{k+1}}{R_{dc}} \right)$$

(24)

Substituting $i_{g,k+1}$ and $V_{dc,k+1}$ obtained from (12) and (17) into (24), $V_{dc,k+2}$ is determined by $n_{oj,k+1}$. A single-objective cost function $J_{dc,j}$ that shows the error between the average DC-link voltage and $V_{dc,k+2}$ is defined in (25); it is used to determine $n_{oj,k+1}$ that minimizes the error.

$$J_{dc,j} = (V_{dc,avg,k+2} - V_{dc,j})^2$$

(25)

Similar to $J_g$, $J_{dc,j}$ is a quadratic function of $n_{oj,k+1}$ because $V_{dc,k+2}$ has only one variable, i.e., $n_{oj,k+1}$. Therefore, the critical point at which the partial derivative becomes zero is the global minimum. $n_{oj}$ can be obtained using (27) as an integer close to the critical point with the ceiling function.

$$\min J_{dc,j}(n_{oj}) \text{ s.t. } n_{oj} \in [n_{oj,ceil}, n_{oj,ceil+1}]$$

(26)

$$n_{oj,ceil}^{k+1} = \left\lceil \frac{2}{V_{dc,avg,k+2}} \left( \frac{C_{dc}}{T_s} \left( V_{dc,k+2} - V_{dc,j} \right) + \frac{V_{dc}^{k+1}}{R_{dc}} \right) - 0.5 \right\rceil$$

(27)

However, $n_{oj}$ should be limited to make the sum of all $n_{oj}$ equal to $n_{oj}$: The limit range is determined by the number of remaining cells $N_r$ for which $n_{oj}$ should be selected and the remaining AC-side terminal voltage levels $V_{ac}$. In the case of the $m$-th order ($P_c = m$), $N_r$ is expressed using the total number of cells $N$ as (28), and the AC-side terminal voltage level determined in the $m$-th order is expressed as $n_{ac,k+1}^{i+1}$ when $n_{ac}$ can be obtained (29) as the subtraction between $n_{oj}$ and the sum of the AC-side terminal voltage levels obtained up to the previous order.

$$N_r = N - i + 1$$

(28)

$$n_{ac} = n_{oj}^{i+1} - \sum_{m=1}^{i} n_{oj,m}^{i+1}$$

(29)
The minimum and maximum output voltage levels for each cell are determined by \( N_r \) and \( n_o \), as summarized in Table I. For example, for \( N_r = 2 \) and \( n_o = 4 \), the sum of the output voltage levels of the two cells should be 4. Since the range of \( n_o \) is \([-2, 2]\), the output voltage level of both cells should be 2. Therefore, in this case, the maximum and minimum levels of \( n_o \) are determined to be same value 2. When \( n_o = 3 \), the maximum level \( n_{oj,\text{max}} \) is set to 2 and the minimum level \( n_{oj,\text{min}} \) is set to 1 because the output voltage level of both cells is composed of 1 and 2. For \( N_r = 1 \), the output voltage level of the last remaining cell is \( n_o \). Therefore, in this method, the higher the priority, the wider is the output voltage level selection range; thus, the level that is more suitable for regulating \( V_{dc} \) can be selected. The range of the optimized \( n_o \) obtained using (27) can be limited to \([n_{oj,\text{min}}, n_{oj,\text{max}}]\) using the minimum and maximum levels obtained in this manner.

C. LAYER III: FLYING CAPACITOR VOLTAGE CONTROL

In this layer, the switching states suitable for FC voltage control are identified while determining \( n_{oj} \) in Layer II. However, unlike the conventional FCS-MPC method, cells are divided into two legs and the switching state of each leg is sequentially determined to reduce the number of switching state combinations to be compared; the starting order of the legs is alternated. If the \( k \) sampling instant starts from leg \( A \), the next \( k+1 \) sampling instant starts from leg \( B \). The two-leg output voltage levels must be set according to the \( n_{oj} \) determined in Layer II because \( n_{oj} \) is determined by \( n_{oa} \) and \( n_{ob} \) as in (30).

\[
n_{oj}^{k+1} = n_{oa}^{k+1} - n_{ob}^{k+1}
\]  

It is necessary to predict the FC voltages to select suitable switching states for the FC voltage control. The current flowing through the FC is expressed by the differential term of the FC voltage. After substituting (7) or (8) into (9), it is transformed into a discrete time model (32)–(33) using the forward Euler method (31).

\[
dV_{jo}^{k+1} = \frac{V_{jo}^{k+1} - V_{jo}^{k}}{T_f} \tag{31}
\]

\[
V_{jo}^{k+1} = V_{jo}^{k} + \frac{T_f}{C_f} \left( T_{a2j} - T_{a1j} \right) t_g^k \tag{32}
\]

\[
V_{jo}^{k+1} = V_{jo}^{k} + \frac{T_f}{C_f} \left( T_{b1j} - T_{b2j} \right) t_g^k \tag{33}
\]

According to (32)–(33), \( V_{jo}^{k+1} \) can be predicted with \( V_{jo}^{k} \) and \( t_g^k \) sensed by A/D conversion and the switching state \( T_{ij} \). For time-delay compensation, the FC voltage after two sampling periods \( V_{jo}^{k+2} \) is predicted as (34) and (35).

\[
V_{jo}^{k+2} = V_{jo}^{k+1} + \frac{T_f}{C_f} \left( T_{a2j} - T_{a1j} \right) t_g^{k+1} \tag{34}
\]

\[
V_{jo}^{k+2} = V_{jo}^{k+1} + \frac{T_f}{C_f} \left( T_{b1j} - T_{b2j} \right) t_g^{k+1} \tag{35}
\]

\[
V_{jo}^{k+2} \text{ is determined using } T_{ij} \text{ because } t_g^{k+1} \text{ and } V_{jo}^{k+1} \text{ are obtained using (11), (32), and (33). The magnitude of the voltage error between the command of the FC voltage, which is half of } V_{dc,\text{avg}}^{k+1} \text{ and } V_{jo}^{k+2} \text{ is defined as the cost function } J_{jo}. \tag{36}
\]

\[
J_{jo} = \left( \frac{1}{2} V_{dc,\text{avg}}^{k+1} - V_{jo}^{k+2} \right)^2 \tag{36}
\]

Assuming that the difference between the two switching states \( K_{jo} \) is expressed as (37)–(38), \( J_{jo} \) is a positive quadratic function of \( K_{jo}^{k+1} \). Therefore, the global minimum is the critical point at which the partial derivative becomes zero.

\[
K_{jo}^{k+1} = \frac{C_f}{T_{ij}} \left[ \left( V_{jo}^{k+1} - \frac{1}{2} V_{dc,\text{avg}}^{k+1} \right) - 0.5 \right] \tag{39}
\]

Table II lists the switching state combinations according to \( n_{oj} \) when leg \( A \) has priority and the method to select the appropriate switching states of leg \( A \). A list of possible candidates comprises switching state combinations that make it possible for \( n_{oa} \) to satisfy \( n_{oj} \) calculated in Layer II. By calculating \( K_{oj} \), (39), suitable switching states for the FC voltage control are selected.
For example, in the case where leg A has priority and \( n_{a|j} \) is 2, the possible \( n_{a|j} \) is 1; therefore, there is only one possible combination of switching states: \( \{T_{a|j}, T_{a|j}\} = \{1, 1\} \). Thus, the switching states were determined as \( \{1, 1\} \). However, when \( n_{a|j} \) is 1, \( n_{a|j} \) can be 0 or 1; therefore, the selectable switching state combinations are \( \{0, 1\}, \{1, 0\} \), and \( \{1, 1\} \). By calculating \( K_{a|j} \) (39), one switching-state combination is determined among the three combinations. If \( K_{a|j} = 1 \), \( \{1, 0\} \) is selected; if \( K_{a|j} = 0 \), \( \{1, 1\} \) is selected and if \( K_{a|j} = -1 \), \( \{0, 1\} \) is selected. Likewise, the other case of \( n_{a|j} \) proceeds in the same manner to select a switching state combination. However, when \( n_{a|j} \) is 0 and \( K_{a|j} = 0 \), there are two possible combinations of switching states: \( \{0, 0\} \) and \( \{1, 1\} \). In this case, \( \{0, 0\} \) is selected. Through this process, the switching states of leg A are determined.

Table III shows how to determine the combination of the switching states of leg B when leg A has a priority. \( n_{b|j} \) is obtained using (30) and the switching state combinations that make \( n_{b|j} \) are listed as possible candidates to determine the switching states of the remaining leg. Using \( K_{b|j} \) (39), an appropriate switching state combination was selected among the possible candidates. The case where leg B has priority is conducted in the same manner; however, it is skipped for the sake of brevity.

Fig. 4 shows a flowchart of Layer I and Layer II in the proposed FCS-MPC. Fig. 4 (a) is a flowchart of Layer I, and it identifies \( n_{a|j}^{k+1} \) that causes the error in the grid current to be small without comparison and only by calculation using pre-

![Table II](https://creativerecommons.org/licenses/by/4.0/)

![Table III](https://creativerecommons.org/licenses/by/4.0/)

**FIGURE 4.** Flowchart of the proposed FCS-MPC: (a) Layer I, (b) Layer II

**FIGURE 5.** Flowchart of the proposed FCS-MPC in Layer III when leg A has priority

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causes the error of the FC voltage to be small without comparison and only by calculation using prediction.

D. ANALYSIS OF COMPUTATIONAL BURDEN

Table IV lists the maximum number of calculations for the cost function based on the number of cells. In addition, the cost function is expressed as a directed weighted graph for a visual comparison of the maximum number of comparisons between the two methods. Figs. 6, 7, and 8 show each layer of the hierarchical FCS-MPC as a graphical structure. The nodes are represented as selectable candidates of \( n_{oT} \), and the number of nodes is equal to the number of \( n_{oT} \) candidates. The weight is expressed as the cost function of the corresponding node. The direction proceeds from the start node \( S \) to the end node \( E \), and the node with the smallest weight among the candidate nodes is selected using greedy selection when moving from node to node.

Fig. 6 shows Layer I of FCS-MPC based on a hierarchical structure as a graph structure. Fig. 6 (a) shows a conventional FCS-MPC, which evaluates all candidates to find the optimized \( n_{oT} \) that minimizes the cost function \( g \) defined in [28]. The number of evaluations of the cost function is \( 4N + 1 \) because the range of \( n_{oT} \) is \([-2N, 2N]\). However, the proposed method obtains the optimized \( n_{oT} \) using only one calculation (23), without comparison. Therefore, even if the number of unit cells increases, there is no significant difference in the execution time required for Layer I.

Fig. 7 shows Layer II of the hierarchical FCS-MPC as a graph structure. The number of cases in which the sum of \( n_{oT} \) becomes zero (i.e., \( n_{oT} = 0 \)) is the largest. Fig. 7 (a) shows that the \( n_{oT} \) combinations of all cells that result in \( n_{oT} = 0 \) in the conventional method. One combination that minimizes the cost function \( g_{Vdc} \), which is defined in [28], is selected by comparing all combinations, and therefore, the number of \( n_{oT} \) combinations causes \( n_{oT} \) to increase exponentially with an increase in the number of cells. For example, the number of \( n_{oT} \) combinations is 19 for 3 cells; however, it increased to 381 for 5 cells and 8135 for 7 cells. Thus, it is not easy to expand the voltage because the number of calculations for the cost function increases exponentially during the voltage expansion. However, the proposed method determines the optimized \( n_{oT} \) for \( V_{dcj} \) control for one cell while making the sum of \( n_{oT} \) for all cells equal to \( n_{oT} \). This is determined through calculations using a single-objective cost function. Therefore, it does not affect the performance of \( i_c \) control, and only the \( (N-1) \) number of cost functions are evaluated without comparison. Therefore, the execution time does not increase dramatically because the number of calculations for the cost function increases linearly with the number of cells, regardless of the voltage expansion.

Fig. 8 shows Layer III in the hierarchical FCS-MPC as a directed weighted graph. The maximum number of combinations of switching states is in the case of \( n_{oT} = 0 \). Fig. 8 (a) shows the conventional method, where a node is a combination of the four upper switching states of the \( j \)-th unit cell that results in \( n_{oT} = 0 \). In this case, all six candidate nodes are compared because there are six combinations, and the node that causes the cost function \( g_{Vfcj} \), which is defined in [28], to become small is selected. Therefore, the total maximum number of calculations for the cost function is \( 6N \) because a maximum of six switching-state combinations are compared to determine the switching state of one cell. However, each node consists of two upper switching states because the proposed FCS-MPC in Fig. 8 (b) separates one cell into legs.
Finally, two calculations for the cost function are required for the switching state combination of one cell because one cost function is calculated for each leg. Thus, the total number of comparisons is $2^N$. Table IV shows that the maximum number of calculations for the cost function in the proposed FCS-MPC has a linear relationship with the number of cells, unlike the conventional exponential characteristics, and therefore, it is easy to expand the voltage level. Furthermore, the larger the voltage level, the greater is the effect of reducing the execution time compared with the conventional method.

### IV. PERFORMANCE VERIFICATION

#### A. SIMULATION RESULTS

A single-phase 9-cell CFCHB was simulated using PSIM to verify the proposed algorithm. The simulation parameters are the same as those listed in Table V. The grid frequency is 60 Hz, and the AC grid voltage is 13.2 kV using a single-phase in a three-phase 22.9 kV system. The DC-link voltage and FC voltage of each cell are controlled to 2.2 kV and 1.1 kV respectively.

Fig. 9 shows the simulation waveform of the proposed algorithm in a steady state. Fig. 9 (a) shows $v_g$ and $i_g$ and they coincide at same frequency so that the power factor can be controlled to 1. Fig. 9 (b)-(d) show the DC-link voltages of each cell. $V_{dij}$ are regulated by the command voltage of 2.2 kV, and the magnitude of voltage ripple is regulated within 5%. Fig. 9 (e) shows $v_{oi}$ and it is output by stacking the 1.1 kV unit voltage to 37 levels. Fig. 9 (f)-(h) show the FC voltages of each cell. $V_{fpj}$ are controlled at 1.1 kV, which is half of $V_{dij}$.

#### B. EXPERIMENTAL RESULTS

A 2 kW laboratory-scale single-phase 3-cell CFCHB prototype is shown in Fig. 10. The experimental stack is reduced to perform experiments in the laboratory, with a focus on verifying the effectiveness of the proposed algorithm. For the power semiconductor, a 1200 V, 10 A rated ROHM SCT2450KE SiC MOSFET was used, and the control algorithm is tested by programming the CPU 1 core of the TMS320F28377D. The turn-off signal of the power device is transferred from TMS320F28377D to the gate driver using a fiber-optic cable. The waveform is observed using a LeCroy Wavesurfer-4034HD oscilloscope. The experiment is conducted at the same sampling time of 100 μs and dead-time of 1 μs to compare the conventional and proposed methods. The parameters used in the experiment are listed in Table V.

| Parameters | Simulations | Experiments |
|------------|-------------|-------------|
| Number of unit cells | 9 | 3 |
| AC grid voltage $v_g$ | 13.2 kVrms | 230 Vrms |
| Grid frequency $f_g$ | 60 Hz | 60 Hz |
| Grid side reactor $L_g$ | 80 mH | 20 mH |
| DC-link voltage $V_{dij}$ | 2.2 kV | 120 V |
| Flying capacitor voltage $V_{of}$ | 1.1 kV | 60 V |
| DC-link capacitor $C_{dij}$ | 1.640 μF | 1.640 μF |
| Flying capacitor $C_{of}$ | 820 μF | 820 μF |
| Sampling Period $T_s$ | 100 μs | 100 μs |
| Load resistor $R_L$ | 400 Ω | 80 Ω |

**TABLE V. PARAMETERS OF THE SIMULATION AND EXPERIMENTAL SETUP**
Fig. 11 shows the steady-state experimental waveform when the proposed FCS-MPC is applied. \( i_g \) is synchronized to the frequency of \( v_g \) and controlled with a power factor of 1. The DC-link voltages are controlled to 120 V, which is the command voltage; the flying capacitor voltages are controlled to half of that at 60 V, and therefore, the \( v_{oc} \) is output at 13 levels. Fig. 12 shows the steady-state waveforms obtained using the conventional and proposed methods. There is no significant difference in the DC-link voltage ripple or grid current when compared to that of the conventional method.

Fig. 13 shows the experimental waveform under load variation from 160 Ω to 80 Ω. Fig. 13 (a) shows the waveform when the conventional method is applied, and Fig. 13 (b) shows the waveform when the proposed method is applied. When the load is changed, the DC-link voltages momentarily decrease and then return to the command voltage of 120 V and are regulated. Fig. 14 shows the experimental waveform change from 80 Ω to 160 Ω. When the load is changed, the DC-link voltages increase momentarily and then return to the command voltage of 120 V and are regulated. The proposed algorithm has a good control performance like that of the conventional method.

Table VI and Fig. 15 show the maximum execution times of the hierarchical FCS-MPC measured by TMS320F28377D in the 3-cell CFCHB. The existing method takes 4.46 μs for comparing all 13 states; however, the proposed method requires only one calculation without a comparison computation, taking 0.96 μs. This is a reduction of 78.4%. Layer II compares 19 states and takes 11.90 μs when using the conventional method; because the proposed method calculates sequentially after sorting, the cost function is calculated twice, which reduces the times by 38.8% to 7.28 μs. For the conventional method, Layer III requires 12.80 μs because a maximum of 18 states are compared by comparing six of each
of the three-unit cells. However, since the proposed method requires only two cost function calculations per unit cell, it takes 7.06 μs, which is a reduction of 44.8%. The proposed algorithm reduces the total execution time of hierarchical FCS-MPC by 47.5% compared to that of the conventional method; thus, the sampling frequency can be increased. In addition, Table IV indicates that, in the proposed method, the amount of computation increases linearly even when the number of cells increases; therefore, the effect of reducing the amount of computation is dramatically increased.

To compare the current harmonics, THD was measured using a power analyzer PPA5530 from N4L, and is represented in Table VII. At the same sampling period of 100 μs, the THD was measured to be 2.63 % in the conventional method, and it was measured to be 2.64 % in the proposed method. Since the grid current THD is similar, it can be seen that the performance of the current control is not significantly different. Furthermore, since the proposed method can shorten the sampling period due to shorter execution time, the THD at the sampling period of 66 μs was measured to be 2.24%. Therefore, the proposed method can improve the grid current THD compared to the conventional method.

V. CONCLUSION

This study proposes a control method to reduce the amount of computation based on FCS-MPC in a grid-connected single-phase N-cell CFCHB. The prediction models of the grid current, DC-link voltage, and FC voltage are derived through the mathematical modeling of the CFCHB to predict the values at a future sampling instance. The control algorithm is designed with a three-layer hierarchical structure of the FCS-MPC, and the optimal objectives for regulating the grid current, DC-link voltage of each cell, and FC voltage are determined in each step without comparison computation. The optimal value is determined only by calculation and without a comparison operation by composing the cost function of each step as a single objective. Therefore, the computational burden is significantly reduced compared to the conventional method without affecting the control performance; thus, the calculation time can be shortened and the sampling frequency can be increased. Compared to the conventional method, the computational burden is significantly reduced, the execution time can be shortened, and the sampling frequency can be increased. It is easy to apply the proposed method to high-voltage applications and digital systems because the computational burden increases linearly even when the number of cells increases. The effectiveness of the proposed algorithm is verified through a 9-cell CFCHB simulation and a 3-cell CFCHB experiment.

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