Inter-IC for Wearables (I²We): Power and Data Transfer over Double-sided Conductive Textile

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Abstract—We propose a power and data transfer network on a conductive fabric material based on an existing serial communication protocol, Inter-Integrated Circuit (I²C). We call the proposed network Inter-IC for Wearables (I²We). Continuous dc power and I²C-formatted data are simultaneously transferred to tiny sensor nodes distributed on a double-sided conductive textile. The textile has two conductive sides isolated from each other and is used as a single planar transmission line. I²C data are transferred along with dc power supply based on frequency division multiplexing (FDM). Two carriers are modulated with the clock (SCL) and the data (SDA) signals of I²C. A modulation and demodulation circuit is designed to enable using off-the-shelf I²C-interfaced sensor ICs. One significant originality of this work is that a special filter to enable passive modulation is designed by locating its impedance poles and zeros at appropriate frequencies. The proposed scheme enables flexible implementation of wearable sensor systems in which multiple off-the-shelf tiny sensors are distributed all over a wear.

Index Terms—Body sensor networks, e-textiles, frequency division multiplexing, serial communication, wearable networks.

I. INTRODUCTION

SMART fabrics, or e-textiles [1], that are capable of biomedical sensing on user’s body surface while eliminating a number of individual wires is one of the key technologies for wearable health monitor systems. Distributing various sensors for measuring temperature, accelerometer, electrocardiography/ electromyography (ECG/EMG), etc., all over a sensing wear will yield rich information for health care [2] and will be also applicable to human-computer interfaces [3].

Powering the distributed sensors and gathering the sensor readings on the wear are a critical issue to implementing such wearable sensor systems. Although functionalizing a fiber itself, e.g., piezoelectric fibers [4], [5] and strain sensing fibers [6], [7], is a promising approach to embed sensors into clothing without sacrificing comfortability, an entire system still needs some silicon-based circuit components to include amplifiers and digital communication interfaces. Therefore, integration of textiles and silicon-based circuitry, which are separately produced, is essentially needed to build a complete wearable sensing system. The motivation of this work is to present a practical method to integrate off-the-shelf silicon-based sensors and textiles.

One modern, straightforward approach is radio-based wireless communication. Each sensor operates with a tiny battery and sends data over the air. However, recharging the batteries is a significant problem especially for densely distributed sensors. More frequent radio transmission results in higher power consumption, and it requires more battery capacity. Besides, other issues with over-the-air data transfer include interference with other communication systems and latency due to multihop, listen-before-talk, and collision followed by retransmission, depending on protocols.

Another approach to avoid these difficulties in terms of batteries and latency is wire-based communication. For physical connection in wearable systems, circuit patterning on fabric with conductive yarns [8], [9], conductive screen printing ink [10], [11], or iron-on conductive fabric patches [12], instead of copper tracks on conventional printed circuit boards (PCBs), is one of the most straightforward and practical approaches. This approach requires separated conductive lines individually connecting leads/pads of electronic components, as in conventional PCBs. A possible vulnerability is that fraying/whiskering the fabric would cause a fatal breakdown, such as disconnection of tracks and short-circuit between neighboring conductive tracks.

An alternative approach to such one-to-one wiring is connecting all the devices on the clothing with a single bus. A double-sided conductive fabric sheet, i.e., both sides of the sheet are conductive and are insulated from each other, can be used as the bus [13]–[18]. The two conductive surfaces work as a signal transmission line shared by all devices mounted on the fabric.

The most important advantage of this approach is that the conductive textile is uniformly patterned without depending on the sensor node locations. Therefore, the textile and electronic circuitry can be designed and fabricated independently from each other. The same textile can be commonly used in various products and will be cost effective. Since the sensor nodes do not require being precisely located on the textile, they can be detached and reassembled in daily use, and then the wear can be washable even if the sensors are not waterproof. Note that uniform pattern is not mandatory, and any other artwork patterns with conductive yarns/ink can be used if they are preferred.

As a simple implementation using commercially available iButton [19] devices, MicroLAN [20] sensor network on a layered conductive fabric has been presented in [13]. TextileNet [15] enables dc power supply and serial communication on the
transmission line by temporally switching the power supply state and the pulse transfer state; thus, the power supply is intermittent and only singleplexed signal transfer is supported. Wade et al. proposed a dc powerline communication (DC-PLC) on a layered conductive textile [14], [21], using a modulation/demodulation (modem) circuitry specially developed by themselves [22]. Continuous dc power supply and amplitude modulated signal, using a carrier in a frequency range of 2-10 MHz, are simultaneously transferred on the same textile medium. Based on a similar concept, continuous dc power supply combined with multiplexed signal transfer [18], which derives from multiplexed ac power transfer [17], have been presented, based on frequency division multiplexing (FDM). In those works, three-channel on/off control of slave devices was demonstrated by on-off modulation of three carriers. This scheme requires $N$ carriers at different frequencies to achieve $N$-channel on-off control, i.e., $N$-bit signal transfer.

In this paper, the FDM scheme is utilized to transfer a pair of clock and data signals of a serial communication protocol, Inter-Integrated Circuit (I²C) [23]. I²C is commonly adopted in various digital-interfaced ICs and microcontrollers (MCUs). Therefore, the I²C-compatible data transfer scheme proposed in this paper can be implemented with various off-the-shelf sensor ICs. It provides compatibility with a significantly wider range of commercially available sensor ICs and MCUs, compared with iButton devices or especially designed modems presented in the previous works mentioned above.

The major contribution of this paper is to propose Inter-IC for Wearables (I²We), which combines I²C data transfer and dc power supply on a double-sided conductive textile. As illustrated in Fig. 1, the dc power and I²C signals are simultaneously transferred on the same planar transmission line using FDM, in a manner similar to other PLCs [22], [24], [25]. One important advantage of the proposed method has a small footprint and low power consumption achieved by passive modulation. I²C-interfaced ICs send the output data by modulating the carriers externally supplied, in a manner similar to passive radio frequency identification (RFID) [26] and other backscatter communications [27], [29]. Carrier generator is separated from modulation circuitry and eliminated from each tiny sensor nodes. A specially designed LC filter, described in Section III enables the passive modulation. The filter design considering the location of its impedance poles and zeros at appropriate frequencies is a significant originality of this work. The carriers are directly modulated with the I²C interface outputs of a digital IC and also demodulated with a simple carrier detector and a data slicer, without any additional digital signal processor or buffer memories.

Contrary to conventional radio links, the proposed I²We link can eliminate the latency due to listen-before-talk and to collision followed by retransmission. In radio-based wireless sensor networks, such latency causes out-of-order arrival of data from distributed sensor nodes, and disturbs processing such as sensor fusion, at the sink node. To recover the order of the data as they are acquired by sensors, a common timebase must be shared in the sensor network for timestamping, and it requires additional resources on each node. In an I²We network, as well as I²C, the master fully initiates data transfer transactions and receives sensor data in order, therefore no additional processing for data ordering is required.

Another important feature from a practical viewpoint is, as stated above, that the I²We network is implemented with off-the-shelf I²C-enabled ICs and MCUs. Engineers familiar with the I²C network can easily reuse the same ICs and MCUs, as well as software libraries implemented in MCUs. Besides, some of commercially available low-cost sensor ICs, e.g. inertial measurement units (IMUs), provide well-engineered sensor fusion functionalities integrated into a single chip. I²We enables reusing such functions and provides a way to avoid reinventing the same functionalities.

The rest of the paper is organized as follows. Section II briefly describes the structure of a double-sided conductive textile and a tack connector. Section III explains the operation principle of the proposed I²We network. A design example and a demonstration system are presented in Section IV and Section V, respectively. Finally, conclusions are presented in Section VI.

II. DOUBLE-SIDED CONDUCTIVE TEXTILE

This section briefly describes a double-sided conductive textile and a tack connector used in this work. The proposed I²We communication is applicable to any two-conductor transmission lines including coaxial, twisted-pair, and parallel-pair cables. Nonetheless, combination with a double-sided conductive textile would be suitable for wearable systems, because it provides freedom of sensor location along with lower resistance and higher current capacity while using a fairly flexible conductive textile for comfortable wearability. Advantages of such a two-dimensional (2-D) conductive material over a 1-D conductive strand are discussed in detail in [14]. The resistance between two points on the 2-D material is approximately proportional to the logarithm of the distance between the two points, while the resistance of a 1-D conductor is proportional to its length. Besides, on the 2-D material, current paths are redundant, and the connection is robustly retained even if the material is partially damaged.

An example of the textile is shown in Fig. 2. The base textile is nonconductive, and on both of its sides square mesh patterns are embroidered with conductive yarns. A cross sectional view of the structure is illustrated in Fig. 3. Conductive yarns on one
Fig. 2. An example of double-sided conductive textile. Square mesh patterns are formed on both the sides of the base fabric with silver-plated conductive yarns.

Fig. 3. Cross sectional view of a wearable signal/power transfer sheet and a tack connector. Although the mesh conductors are represented with separate dots (and a dotted line connecting them) in this figure, each of them is electrically continuous. The top and the bottom mesh conductors are isolated from each other.

side are all electrically connected together and isolated from the conductive mesh on the other side. The square mesh is not mandatory and any other artwork patterns can be used. Alternatively, conductive yarns can be integrated at the stage of the textile fabrication, i.e., the textile can be woven/knitted with both conductive and nonconductive yarns. Piling up conductive and nonconductive textile sheets or printing conductive ink on both the sides of a nonconductive base textiles sheet are also acceptable. Regardless of the fabrication method, an essential requirement is that the conductive materials are exposed on both sides, and both the conductive surfaces are isolated from each other.

As shown in Fig. 3, a special connector consisting of a tack (needle) and a socket is used in this work. The back side of a sensor node PCB directly contacts one side of the textile, and the conductive needle-and-socket connector enables electrical connection between the PCB and the other side of the textile. To avoid shorting both the conductive surfaces, the needle should be partially insulated or should be put in a nonconductive area, i.e., inside an aperture of the mesh. This configuration allows the physical mounting of a device and its electrical connection to be integrated into a single action, i.e., just sticking the needle through the textile and mating the needle with the socket.

Fig. 4. $I^2C$ bus configuration.

III. PRINCIPLE OF OPERATION

A. Inter-Integrated Circuit (I$^2$C)

This subsection briefly explains the operation and implementation of I$^2$C. Descriptions below assume the Standard-mode or Fast-mode, with clock frequencies up to 100 kHz or 400 kHz, respectively, defined in the I$^2$C specification [23].

An I$^2$C bus consists of two signal lines: clock (SCL) and data (SDA). One or more masters and one or more slaves can be connected to the bus in parallel. Only one master can initiate the communication at a time, and all the other slaves on the bus listen to the master’s signal; then, only a slave addressed by the master responds to the signal during the transaction. The bus is bidirectional, i.e., the data can be transferred from the master to the slave, and vice versa. For both the directions, the master generates the clock signal, and thus takes the initiative in the communication. The data signal is generated by the master or the slave, depending on the master’s transmit mode or receive mode.

An I$^2$C bus configuration including output transistors inside the master and the slave is shown in Fig. 4. The SCL and SDA pins of each node are bidirectional and are internally connected to an input circuitry and an open-drain transistor output. The SCL and SDA lines are individually pulled up to the positive supply voltage with resistors. While no signal is transferred on the bus, all the output transistors are in the off state, and SCL/SDA lines are nearly at the positive supply voltage, i.e., the logical high. When any one of the output transistors is turned on, the signal line is inverted nearly to the ground level, i.e., the logical low.

Note that the output pins only sink the current, but do not actively source the current. The dc voltage needed to interpret the transistors’ off/on states to logical high/low levels is externally supplied.

B. Clock and Data Multiplexing on Conductive Textile

As described in Section II, a single transmission line is formed with a double-sided conductive textile. In this work, the SCL/SDA signals and dc power supply are simultaneously transferred on the same transmission line using FDM. For SCL/SDA transmission, two frequency carriers are respectively modulated with SCL and SDA, in the manner of amplitude shift keying (ASK).

The proposed I$^2$We bus configuration including the output transistors inside the master and the slave is shown in Fig. 4.
Similar to the external dc supply to the signal lines via pull-up resistors in conventional I2C, the RF carriers are externally supplied to the bus via "pull-up" impedances. The carrier generator can be separated from the master and the slave. The SCL and SDA pins of each node are connected to the bus through a special bandpass filters (BPFs), and the output transistors’ off/on states are directly interpreted into high/low states in the RF carrier amplitude on the signal line. In each of the master and the slave, the amplitude shift is interpreted into logical high/low levels by ASK demodulation circuitry. Thus, the SCL/SDA pins of an off-the-shelf I2C-enabled ICs directly modulate the carriers and receive digital SCL/SDA signal via the demodulation circuitry.

C. Filter Design for Passive Modulation

In this subsection, the ASK modulation operation and the filter design to achieve the operation are described in detail.

The basic idea for passive ASK modulation in the configuration shown in Fig. 5 is, similar to the conventional I2C, to switch the impedance connected to the signal line between open and short, depending on the logical state of the SCL/SDA pin. To modulate two carriers independently, the impedance element should achieve an open/short switch at the frequency of the carrier to be modulated and should stay open at the other frequency.

An equivalent circuit that represents one of the two (SCL and SDA) signal inputs/outputs (I/Os), its associating filter and a carrier source is illustrated in Fig. 6. We define the impedance matrix of the two-port filter as follows:

\[
\begin{pmatrix}
V_1 \\
V_2
\end{pmatrix} = \begin{pmatrix}
z_{11} & z_{12} \\
z_{21} & z_{22}
\end{pmatrix}
\begin{pmatrix}
I_1 \\
I_2
\end{pmatrix},
\]

where \(V_1\) and \(V_2\) are respectively the voltage across ports 1 and 2, and \(I_1\) and \(I_2\) are the current flowing into ports 1 and 2, respectively. For reciprocal network, \(z_{12}\) and \(z_{21}\) are identical. Therefore, by defining \(z_m \equiv z_{12} = z_{21}\), \(1\) is rewritten as

\[
\begin{pmatrix}
V_1 \\
V_2
\end{pmatrix} = \begin{pmatrix}
z_{11} & z_m \\
z_m & z_{22}
\end{pmatrix}
\begin{pmatrix}
I_1 \\
I_2
\end{pmatrix}.
\]

The secondary port is connected to the SCL/SDA pin. Let \(Z_{IO}\) denote the input impedance of the SCL/SDA pin, then

\[
V_2 = -Z_{IO}I_2 = z_mI_1 + z_{22}I_2,
\]

therefore

\[
\frac{I_2}{I_1} = -\frac{z_m}{Z_{IO} + z_{22}}.
\]

The impedance seen looking into the filter at the primary port, \(Z_{in}\), is calculated as follows.

\[
Z_{in} = \frac{V_1}{I_1} = z_{11} + z_m\frac{I_2}{I_1} = z_{11} - \frac{z_m}{Z_{IO} + z_{22}}
\]

Thus, the filter primary port impedance depends on \(Z_{IO}\), which is determined by the on/off-state of the open-drain transistor, i.e., the logical high/low output. Let \(Z^H_{IO}\) and \(Z^L_{IO}\) represent the impedance of the I/O at the logical high and low states, respectively. While the \(\omega_1\) carrier with a constant voltage amplitude \(V_0\) is supplied via a pull-up impedance \(Z_P\), the voltage appearing at the primary port of the filter is calculated as follows:

\[
V_1 = \frac{Z_{in}}{Z_P + Z_{in}}V_0
\]

From \(5\) and \(6\), \(V_1\) is determined by \(Z_{in}\) depending on \(Z_{IO}\). Thus, the \(\omega_1\) carrier is ASK modulated directly depending on the logical output of the SCL/SDA pin. Note that the filter for modulating the \(\omega_1\) carrier should keep high impedance at \(\omega_2\), regardless of the logical pin state.

Requirements on \(Z_{IO}(\omega)\) to modulate the \(\omega_{mod}\) carrier and to avoid cross-talk modulation of the \(\omega_{stop}\) carrier are as follows:
1) For logical high-state, \( Z_{\text{in}}(\omega_{\text{mod}}) \) should be open, to avoid a decrease in the joint impedance of all the filters connected to the same transmission line.

2) For logical low-state, \( Z_{\text{in}}(\omega_{\text{mod}}) \) should be short, to achieve higher modulation depth for clearly distinguishable symbols.

3) Regardless of the logical state, \( Z_{\text{in}}(\omega_{\text{stop}}) \) should be open, to avoid cross-talk modulation.

The above requirements are summarized in Table I.

Suppose that the filter consists of lossless, passive reactances. All the elements of the impedance matrix in (2) are therefore pure imaginary numbers. Then, the impedance matrix is realized with a T-network shown in Fig. 7 where the reactance on each branch is defined as follows:

\[
x_1 = \text{Im}(z_{11} - z_m) \\
x_2 = \text{Im}(z_{22} - z_m) \\
x_m = \text{Im}(z_m).
\]

The three elements in the T-network are determined by considering the requirements, as described below.

Since the I/O pin is a parallel network of the digital input circuitry and the open-drain transistor at off-state, \( Z_{\text{IO}}^H \) is almost pure capacitive reactance, i.e.,

\[
Z_{\text{IO}}^H \approx -jX_{\text{IO}}^H, \quad (10)
\]

where \( X_{\text{IO}}^H \) is positive real number.

The first requirement stated above, \( Z_{\text{in}} \rightarrow \infty \) for the logical high state, can be satisfied if \( z_m \neq 0 \) and \( Z_{\text{IO}}^H + z_{22} = 0 \) in (5). Therefore, \( z_{22} \) is determined as

\[
z_{22} = jX_{\text{IO}}^H, \quad (11)
\]

which is a pure inductive reactance.

The second requirement, \( Z_{\text{in}} = 0 \) for the logical low, is achieved by \( z_{11} = z_m^2/(Z_{\text{IO}}^H + z_{22}) \). This can be approximated as \( z_{11} \approx z_m^2/z_{22} \), because \( |z_{22}| = |Z_{\text{IO}}^H| \gg |Z_{\text{IO}}^L| \). Therefore,

\[
z_{11} - z_m \approx \frac{z_m^2}{z_{22}} - z_m = \frac{-z_m}{z_{22}} (z_{22} - z_m). \quad (12)
\]

By substituting (11), (13) and (12) are respectively rewritten as

\[
x_2 = X_{\text{IO}}^H - x_m \quad (13)
\]

| TABLE I | IDEAL INPUT IMPEDANCE OF FILTER, \( |Z_{\text{in}}(\omega)| \) |
|---|---|
| \( \omega = \omega_{\text{mod}} \) | \( 0 \) |
| \( \omega = \omega_{\text{stop}} \) | \( \infty \) |
| \( \omega = \omega_{\text{in}} \) | \( \infty \) |

1), 2), 3): Correspond to the enumerated items in the body text.

\[
x_1 = -\frac{x_m}{X_{\text{IO}}^H} x_2. \quad (14)
\]

Relationship among \( x_1, x_2 \) and \( x_m \), and combinations of inductive/capacitive reactances satisfying the above equations are shown in Fig. 8.

For the third requirement, to stop the \( \omega_{\text{stop}} \) current flow through the filter primary port regardless of the logical state of the I/O pin, an LC parallel resonant network should be placed at the \( x_1 \)-branch. Joint impedance of a parallel connection of inductance \( L_1 \) and capacitance \( C_1 \), satisfying \( \omega_{\text{stop}}^2 = (L_1C_1)^{-1} \), at \( \omega = \omega_{\text{mod}} \) is calculated as follows.

\[
j\omega_{\text{mod}} C_1 + (j\omega_{\text{mod}} L_1)^{-1} \quad \Rightarrow \quad \frac{1}{1 - \alpha^2} = \frac{1}{1 - \omega_{\text{stop}}^2 C_1}, \quad (15)
\]

where \( \alpha \equiv \omega_{\text{mod}}/\omega_{\text{stop}} \). Thus, \( x_1(\omega_{\text{mod}}) \) is inductive for \( \omega_{\text{mod}} < \omega_{\text{stop}} \), and \( x_2(\omega_{\text{mod}}) \) is capacitive for \( \omega_{\text{mod}} > \omega_{\text{stop}} \). An appropriate configuration should be chosen depending on \( \alpha \). For example, \( x_1 \) is inductive in configuration (a) shown in Fig. 8, therefore this configuration is applicable only to the condition \( \omega_{\text{mod}} < \omega_{\text{stop}} \). On the other hand, for \( \omega_{\text{mod}} > \omega_{\text{stop}} \), configuration (b) is applicable.

As a summary of the above discussions, minimal filter configurations are listed in Table I (a), (b), (c), and (d) on the top row of the table correspond to those in Fig. 8. Configuration (d), in which \( x_1(\omega_{\text{mod}}) = x_2(\omega_{\text{mod}}) = 0 \), is realized by series resonance at the \( x_1 \)-branch. The additional reactance element connected in series to the parallel LC is inductive or capacitive, depending on \( \alpha \). Configuration (e) shown in Fig. 8 is inappropriate and is therefore excluded from the table, because all of the current flowing into the filter from the primary port flows through \( x_m = 0 \) and no current appears at the secondary port.

D. ASK Demodulator

In order to interpret the carrier amplitude shift into logical high/low that is comprehensive for the digital IC, an ASK demodulator is needed for each SCL/SDA pin, as shown in Fig. 5.
The demodulator input is ac-coupled with a capacitor and the output is RF-decoupled with an inductor. The demodulator therefore operates without any positive/negative feedback effects such as oscillation and self-holding, although the input and output are connected together to the same SCL/SDA pin.

A block diagram of the demodulator is shown in Fig. 9. The \( \omega_{\text{mod}} \) carrier is fed into the RF detector via the filter described in the previous subsection, and the \( \omega_{\text{stop}} \) carrier is blocked by the filter. The RF detector extracts the envelope of the \( \omega_{\text{mod}} \) carrier. The analog envelope waveform is binarized by a data slicer \( [30] \). The data slicer automatically tunes the \( \omega_{\text{mod}} \) carrier is fed into the RF detector via the filter (LPF). The binary output of the data slicer is accepted by the SCL/SDA pin. The comparator waveform, via a lowpass filter (LPF). The binary output of the data slicer is RF-decoupled with an inductor. The demodulator input is ac-coupled with a capacitor and the output is RF-decoupled with an inductor. The demodulator therefore operates without any positive/negative feedback effects such as oscillation and self-holding, although the input and output are connected together to the same SCL/SDA pin.

A block diagram of the demodulator is shown in Fig. 9. The \( \omega_{\text{mod}} \) carrier is fed into the RF detector via the filter described in the previous subsection, and the \( \omega_{\text{stop}} \) carrier is blocked by the filter. The RF detector extracts the envelope of the \( \omega_{\text{mod}} \) carrier. The analog envelope waveform is binarized by a data slicer \( [30] \). The data slicer automatically tunes the \( \omega_{\text{mod}} \) carrier is fed into the RF detector via the filter (LPF). The binary output of the data slicer is accepted by the SCL/SDA pin. The comparator output terminal should be RF-decoupled from the filter and the SCL/SDA pin by using an RF choke (RFC), so that the comparator output impedance does not affect the filter design.

**IV. DESIGN EXAMPLE**

This section presents an example of an \( \omega_{\text{mod}} \) carrier. The analog envelope waveform is binarized by a data slicer \( [30] \). The data slicer automatically tunes the reference voltage of the comparator depending on the input waveform, via a lowpass filter (LPF). The binary output of the data slicer is accepted by the SCL/SDA pin. The comparator output terminal should be RF-decoupled from the filter and the SCL/SDA pin by using an RF choke (RFC), so that the comparator output impedance does not affect the filter design.

**A. Carriers and I/O Capacitance**

In order to design the filters, the carrier frequencies and the capacitance of SCL/SDA pin are required to be specified. Here we choose the carrier frequencies as 20 MHz and 50 MHz for SCL and SDA, respectively. The two frequencies should avoid being an integer multiple of each other, to minimize crosstalk due to harmonics. The lower bound of the carrier depends on the frequency of the SCL signal. For the Standard-mode with 100 kHz SCL, the carrier frequencies are required to be significantly higher than 100 kHz. The upper bound is determined so that the wavelength in the textile medium is significantly longer than the size of the textile. If the wavelength is comparable to or shorter than the size of the textile, the carrier signal strength at each receiver significantly depends on the location and the frequency, because of standing waves. The received signal strength fluctuation requires a more complicated configuration of the demodulator.

In this work we used a development board Teensy 3.2 [51] with a 32-bit MCU, MK20DX256VLH7 [32]. Measured capacitance of the SCL/SDA pin of the MCU, including stray capacitance of PCB copper tracks, was approximately 8 pF at the logical high state. For the carrier frequencies 20 MHz and 50 MHz, the reactance of the capacitance is approximately \(-j1 \text{ k}\Omega\) and \(-j400 \Omega\), respectively.

**B. Filter Design**

Filter configurations should be selected from those shown in Table II. Here we choose (a) and (b) for the lower carrier (20 MHz) and for the higher carrier (50 MHz), respectively.

The theoretical analyses of the filter presented in the previous section assumed lossless reactance components. There is one degree of freedom and \( x_m \) can be arbitrarily determined to satisfy \( x_m > X_m^H \) in (a) and \( 0 < x_m < X_m^H \) in (b). For actual filter design, the one degree of freedom enables choosing appropriate inductors and capacitors so that the filter possesses significantly high/low impedance to approximately achieve the characteristics shown in Table II. The highest/lowest impedance that can be achieved by the filter depends on the specific characteristics of inductors and capacitors including loss factors.

One significant factor that dominates the filter characteristics is the frequency of impedance zero between two impedance poles. When the SCL/SDA pin is at logical high state, two poles of \( Z_{\text{in}}(\omega) \) are required to be located at \( \omega = \omega_{\text{mod}} \) and \( \omega = \omega_{\text{stop}} \). From the Foster’s reactance theorem [33], there must be an impedance zero at \( \omega = \omega_{\text{stop}} \), where \( \omega_{\text{mod}} < \omega_{\text{stop}} < \omega_{\text{mod}} \) for configuration (a) and \( \omega_{\text{stop}} < \omega_{\text{mod}} \) for configuration (b). The zero should be significantly separated from the two poles on the frequency axis, because a pole can be almost canceled by the closely located zero and the magnitude of impedance will be significantly reduced. The frequency of the impedance zero can be tuned with \( x_m \).

**TABLE II**

| Frequency condition | (a) \( \omega_{\text{stop}} > \omega_{\text{mod}} \) | (b) \( \omega_{\text{stop}} < \omega_{\text{mod}} \) | (c) \( \omega_{\text{stop}} > \omega_{\text{mod}} \) | (d)-1 \( \omega_{\text{stop}} > \omega_{\text{mod}} \) | (d)-2 \( \omega_{\text{stop}} < \omega_{\text{mod}} \) |
|---------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|
| Configuration       | ![Configuration](image) | ![Configuration](image) | ![Configuration](image) | ![Configuration](image) | ![Configuration](image) |
| Equivalent circuit  | at \( \omega = \omega_{\text{mod}} \) | ![Equivalent circuit](image) | ![Equivalent circuit](image) | ![Equivalent circuit](image) | ![Equivalent circuit](image) |
| Equivalent circuit  | at \( \omega = \omega_{\text{stop}} \) | ![Equivalent circuit](image) | ![Equivalent circuit](image) | ![Equivalent circuit](image) | ![Equivalent circuit](image) |
The filter configurations including the equivalent impedance of SCL/SDA pins are shown in Table [IV]. An example of selection of inductors and capacitors is shown in Table [IV] which include exact values calculated with (13) and (14) and approximated values selected from the E12 series. Note that \( C_H \) is increased by adding an external shunt capacitor in configuration (a) to reduce the inductance of \( x_m \approx X_{H1} \) so that the inductor can be chosen from commercially available high-Q wire-wound tiny chip inductors, which are typically lower than 10 \( \mu \)H at maximum. Terminals 1-1’, 2-2’, and 1-2 are required to be isolated at dc; therefore, dc block (DCB) capacitors are inserted as shown in Table [IV]. The impedance of DCBs at carrier frequencies are negligible. The simulated impedance-frequency curves of the designed filters are presented in Fig. 10. The simulations were performed with LTspice XVII. Simulation results for both lossless and lossy models are plotted. The lossless simulations were conducted with the exact calculated inductances/capacitances in Table [IV] Besides, \( R_H \) was replaced with an open circuit and \( R_L \) was replaced with a short circuit. For lossy simulations, we used the E12 series values and manufacturer-supplied inductor SPICE models [34], which well represent realistic characteristics including losses and self-resonance. The capacitors were modeled as ideal capacitances because their loss factors are negligible compared with the inductors at the frequencies of interest. Based on our preliminary measurement results, we decided \( R_H = 10 \text{k\Omega} \) and \( R_L = 10 \text{\Omega} \) for the lossy models. The result shows that the lossless models achieve ideal open and short at the carrier frequencies and the lossy models also achieve significant impedance changes more than two orders of magnitude at \( \omega = \omega_{\text{mod}} \).

The filters (a) and (b) were fabricated as shown in Fig. [IV] and their input impedances were measured with a vector network analyzer (VNA), Agilent Technologies E5071B. The measurement results shown in Fig. 12 reasonably agree with the simulation results of the lossy models. Let \( Z_{\text{in}}^H \) and \( Z_{\text{in}}^L \) denote \( Z_{\text{in}} \) at the logical high and low states, respectively.\( Z_{\text{in}}^H/Z_{\text{in}}^L \) is approximately 44 at 20 MHz for filter (a), and 87 at 50 MHz for (b).

In Fig. 6 let \( V_{1H}^L \) and \( V_{1L}^L \) denote the voltage across the primary port of the T-filter at the logical high and low states, respectively. The ratio \( V_{1H}^L/Z_{\text{in}}^L \) determines the maximum ratio of \( V_{1H}^L \) to \( V_{1L}^H \). When the carrier is supplied from a voltage source via a pull-up impedance \( Z_P \), \( V_{1H}^L/V_{1L}^L \) is calculated as follows.

\[
\frac{V_{1H}^L}{V_{1L}^L} = \frac{Z_{\text{in}}^H/(Z_P + Z_{\text{in}}^H)}{Z_{\text{in}}^L/(Z_P + Z_{\text{in}}^L)}
\]

If \( Z_P \) is significantly greater than \( Z_{\text{in}}^H \) and \( Z_{\text{in}}^L \),

\[
\frac{V_{1H}^L}{V_{1L}^L} \approx \frac{Z_{\text{in}}^H}{Z_{\text{in}}^L}
\]

Thus, the ratio (17) can achieve 44 and 87 at a maximum, for SCL and SDA, respectively. However, the supplied carrier voltage significantly attenuates with \( Z_P \gg Z_{\text{in}} \). \( Z_P \) is required to be tuned depending on the carrier source voltage and the RF detector sensitivity.

### Table IV

| Inductors and Capacitors | Calculated | E12 series | Calculated | E12 series |
|--------------------------|------------|------------|------------|------------|
| \( C_{1a} \)            | 18 pF      | (8 pF + 10 pF) | 8 pF      |
| \( L_{ma} \)            | 4.7 \( \mu \)H | 1.0 \( \mu \)H | 1.10 \( \mu \)H |
| \( C_{1a} \)            | 7.64 pF    | 8 pF       | 57.3 pF    |
| \( C_{2a} \)            | 53.6 pF    | 56 pF      | 0.267 \( \mu \)H |

* An external shunt capacitor is added.

### Table III

| Frequency condition | \( \omega_{\text{stop}} > \omega_{\text{mod}} \) | \( \omega_{\text{stop}} < \omega_{\text{mod}} \) |
|---------------------|---------------------------------|---------------------------------|
| Configuration       | ![Diagram](example.png)         | ![Diagram](example.png)         |
| Equivalent circuit  | ![Diagram](example.png)         | ![Diagram](example.png)         |
| at \( \omega = \omega_{\text{mod}} \) for logical high | ![Diagram](example.png)         | ![Diagram](example.png)         |
| at \( \omega = \omega_{\text{mod}} \) for logical low | ![Diagram](example.png)         | ![Diagram](example.png)         |

\( L/C \) represents parallel connection of \( L \) and \( C \).
Fig. 10. Simulated filter input impedance of configurations (a) and (b). The impedance values were simulated at both the logical high (H) and low (L) states for each of lossless and lossy models. Filters consisting of lossless components with exact values calculated from (13) and (14) become either ideal open or short at the carrier frequencies. The lossy models also achieve significant impedance changes by two orders of magnitude.

Fig. 11. Impedance measurement of fabricated T-filters.

C. ASK Demodulator Design

A design example of the ASK demodulator is shown in Fig. 13. The secondary port of the T-network filter is connected to the input of an RF detector via DCB capacitors. The envelope of the RF signal is detected and is fed to a data slicer via a low pass filter (LPF).

Although the DCB and RFC suppress feedback from the slicer output to the detector input as explained in Section III-D, a transient voltage spike is induced at the detector input when the logic level of the SCL/SDA pin is toggled and stimulates the RF detector. This can cause latch-up of the data slicer output as follows. When the RF amplitude shifts to the low level, the RF detector output decreases, and the data slicer output turns to low. The voltage step from the high to the low level causes the above described voltage spike at the RF detector input, then the detector output increases again, and the data slicer output turns to the high. Thus, the slicer output holds the logical high, regardless of the actual RF amplitude.

To prevent the latch-up fault, an anti-parallel diode pair is connected to the input of the detector. The diodes clip off the spike at ±$V_F$ as shown in Fig. 14, where $V_F$ denotes the forward voltage drop of the diode. The desired RF signals $\omega_1$ and $\omega_2$ are correctly detected across the diodes, because the voltage amplitude of the RF signal is smaller than $V_F$. 

Fig. 12. Measured filter input impedance of configurations (a) and (b).

Fig. 13. Design example of the ASK demodulator. Labels B and C correspond to those in Fig. 5. The demodulator input and output are not directly shorted at any frequencies, because the RF detector input is dc (baseband)-decoupled and the comparator output is RF-decoupled.
Fig. 14. Operation of diode clipper. (a) A spike waveform is induced when the slicer output is toggled. (b) The unwanted spike is clipped off by the diodes, while desired signals with the amplitude smaller than $V_F$ remain.

Fig. 15. Fabricated modem module PCB.

As the RF detector, Linear Technology LT5534 was used. It is a log-scaled RF detector with the output slope of 44 mV/dB at 50 MHz and the input impedance of 2 kΩ [35]. The high input impedance is desirable to reduce the change in the impedance that is connected to the secondary port of the T-filter. Relatively small DCB capacitance, a series connection of two 10 pF capacitors, is to further increase the impedance.

The data slicer can be composed with general comparator ICs that operate with a bandwidth significantly greater than the SCL frequency, typically 100 kHz. In this example, Rohm BU5265HFV [36] was used. The resistor at the data slicer output is for limiting shoot-through current. Although the slicer output and the SCL/SDA pin basically hold the same logical level, they can cause a discrepancy for a short period at a transition of logical state and cause shoot-through current. The capacitor connected to the resistor and the RFC is for stabilization of RF impedance seen looking into the demodulator from the output terminal, regardless of the logical state of the output.

A modem module PCB was fabricated as shown in Fig. 15. A pair of filters and a pair of demodulators for SCL and SDA were integrated into a single PCB. Measured waveforms on this module are shown in Fig. 16. In the measurement, 20 MHz and 50 MHz carriers with about a 10–20 mV amplitude were supplied to the textile, and they were modulated with another modem module connected to the SCL/SDA ports of a Teensy 3.2 MCU board. For power supply, 3.3 V dc voltage was also applied to the textile via RFC inductor.

Fig. 16. Waveforms measured on the fabricated modem module. C1 (the second from the top) and C2 (the bottom) channels are the demodulated waveforms measured at the SCL and SDA pins, respectively. C3 (the top) and C4 (the third from the top) are lowpass-filtered RF detector outputs measured at the positive input terminals of the comparators of SCL and SDA demodulators, respectively. C1 and C2 waveforms swing between approximately 0 V and 3.3 V. C3 and C4 were measured with ac-coupling, and their peak-to-peak amplitude excluding high-frequency spikes were approximately 170 mV and 120 mV, respectively. The period of SCL signal (between two adjacent down-edges) is approximately 12 µs.

Fig. 17. Demonstration system with distributed temperature sensors on a double-sided conductive textile with a dimension of 40 cm × 30 cm.

V. DEMONSTRATION SYSTEM

This section presents a demonstration system. The master device collects sensor readings from multiple sensor nodes and the data are visualized on a PC, as shown in Fig. 17. A brief report on the same system has been published at a previous conference [37].

A batteryless sensor node can be composed with the modem module shown in Fig. 15 and a commercially available I²C-enabled sensor IC, which operates as an I²C slave. A master device, which initiates the I²C communication and collects sensor data, can be composed with the modem module and an MCU board. We used Teensy 3.2 and a temperature sensor IC, Microchip MCP9808 [38], as the master and the slaves, respectively.

The entire system is essentially the same as Fig. 5. A 3.3 V dc voltage was supplied to the bus via a 47 µH RFC.
inductor. 20 MHz and 50 MHz carriers were generated with a clock generator, Silicon Laboratories Si5351A \[39\]. The output clock signal is not a pure tone but a rectangular wave containing harmonics. To suppress the harmonics, the carriers were supplied via LC series resonant circuits. Each of Pull-up containing harmonics. To suppress the harmonics, the carries inductor. 20 MHz and 50 MHz carriers were generated with series connection of a 3.3 $\mu$H inductor, a 22 pF capacitor, and a 2.0 k$\Omega$ resistor. \(Z_{P1}\) is a series connection of a 3.3 $\mu$H, a 2.2 pF, and a 2.0 k$\Omega$.

The master MCU board was connected to a PC with a universal serial bus (USB) cable and collected temperature data were visualized by a plotting software.

Since the \(I^2C\) slave addresses are preset, when the batteryless slaves are attached on the textile, they can immediately join the network, i.e., plug-and-play operation is achieved.

VI. CONCLUSION

We proposed \(I^2W\), which enables \(I^2C\)-formatted signal transfer along with continuous dc power supply on a single transmission line. Double-sided conductive textiles can be used as the transmission line. \(I^2W\) enables simple implementation of a body sensor network, in which a number of batteryless and antennaless sensors are distributed over clothing. Individual wires connecting devices one by one are eliminated. Each device is attached on the textile medium with a tack connector, which integrates physical mounting and electrical connection into a single action.

The key component for \(I^2W\) implementation is the T-network filters, which enable passive modulation of carriers with SCL and SDA signals. The passive modulation approach enables separating carrier generators from each device and contributes to the smaller footprint and lower power consumption of each device. This paper described the design procedure and the operation of the T-filters in detail. The reactivity of each branch of the T-network is determined by considering impedance poles and zeros. 

\(I^2C\) is the de facto standard of serial communication between sensor ICs and MCUs, and various sensor ICs equipped with the \(I^2C\) interface are commercially available. Additionally, software libraries of MCUs for \(I^2C\) communication with sensor ICs can be also used for \(I^2W\) without any modification. Therefore, the proposed \(I^2W\) is expected to be widely used for wearable sensor systems.

REFERENCES

[1] D. Marculescu, R. Marculescu, N. H. Zamora, P. Stanley-Marbell, P. K. Khosla, S. Park, S. Jayaraman, S. Jung, C. Lauterbach, W. Weber, T. Kirstein, D. Cottet, J. Grzyb, G. Troster, M. Jones, T. Martin, and Z. Nakad, “Electronic textiles: A platform for pervasive computing,” in Proceedings of the IEEE, vol. 91, no. 12, pp. 1995–2018, Dec 2003.

[2] K. Yasser, O. A. E., L. C. M., P. Adrien, and A. A. C., “Monitoring of vital signs with flexible and wearable medical devices,” Advanced Materials, vol. 28, no. 22, pp. 4373–4395, 2016. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/adma.201504366

[3] M. Georgi, C. Amma, and T. Schultz, “Recognizing hand and finger gestures with imu based motion and emg based muscle activity sensing,” in Proceedings of the International Conference on Bio-inspired Systems and Signal Processing (BIOSIGNALS-2015), 2015, pp. 99–108.

[4] S. Egusa, Z. Wang, N. Chocat, Z. Ruff, A. Stolyarov, D. Shenmuy, F. Sorin, P. Rakich, J. Joannopoulos, and Y. Fink, “Multimaterial piezoelectric fibres,” Nature materials, vol. 9, no. 8, p. 643, 2010.

[5] Y. Tajitsu, “Piezoelectret sensor made from an electro-spin fluoropolymer and its use in a wristband for detecting heart-beat signals,” IEEE Transactions on Dielectrics and Electrical Insulation, vol. 22, no. 3, pp. 1355–1359, June 2015.

[6] H. Zhang, X. Tao, T. Yu, and S. Wang, “Conductive knitted fabric as large-strain gauge under high temperature,” IEEE Sensors and Actuators A: Physical, vol. 126, no. 1, pp. 110–114, 2006. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0924424705005832

[7] W. Chun, L. Xiang, G. Enlai, J. Muqiang, X. Kailun, W. Qi, X. Zhiping, R. Tianling, and Z. Yingying, “Carbonized silk fabric for ultrastretchable, highly sensitive, and wearable strain sensors,” Advanced Materials, vol. 28, no. 31, pp. 6640–6648, 2016. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/adma.201601572

[8] B. Buechley and M. Eisenberg, “The LilyPad Arduino: Towards Wearable Engineering for Everyone,” IEEE Pervasive Computing, vol. 7, no. 2, pp. 12–15, April 2008.

[9] Q. Li and X. M. Tao, “Three-dimensionally deformable, highly stretchable, permeable, durable and washable fabric circuit boards,” Proceedings of the Royal Society of London A: Mathematical, Physical and Engineering Sciences, vol. 470, no. 2171, 2014. [Online]. Available: http://rspa.royalsocietypublishing.org/content/470/2171/20140472

[10] Y. Kim, H. Kim, and H. J. Yoo, “Electrical characterization of screen-printed circuits on the fabric,” IEEE Transactions on Advanced Packaging, vol. 33, no. 1, pp. 196–205, Feb 2010.

[11] N. Matsuhisa, M. Kaitzenbrunner, T. Yokota, H. Jinno, K. Kuribara, T. Sekitani, and T. Someya, “Printable elastic conductors with a high conductivity for electronic textile applications,” Nature Communications, vol. 6, p. 7461, 2015.

[12] L. Buechley and M. Eisenberg, “Fabric pcb’s, electronic sequins, and socket buttons: Techniques for e-textile craft,” Personal Ubiquitous Comput., vol. 13, no. 2, pp. 133–150, Feb. 2009. [Online]. Available: http://dx.doi.org/10.1007/s00779-007-0181-0

[13] K. V. Laerhoven, N. Villar, and H.-W. Gellersen, “A layered approach to wearable textile networks,” IET Conference Proceedings, pp. 61–66(5), January 2003. [Online]. Available: http://digital-library.theiet.org/content/conferences/10.1049/ic:20030148

[14] E. Wade and H. Asada, “Conductive fabric garment for a cable-free body area network,” IEEE Pervasive Computing, vol. 6, no. 1, pp. 52–58, Jan 2007.

[15] J. AkitA, T. Shimamura, and M. Toda, “Flexible network infrastructure for wearable computing using conductive fabric and its evaluation,” in 26th IEEE International Conference on Distributed Computing Systems Workshops (ICDCSW’06). IEEE, 2006, p. 65.

[16] H. Shinoda, M. Makino, N. Yamahira, and H. Itai, “Surface sensor network using inductive signal transmission layer,” in Proceedings of the Fourth International Conference on Networked Sensing Systems, Braunschweig, Germany, June 2007, pp. 201–206.

[17] Y. Tajima, A. Noda, and H. Shinoda, “Signal and power transfer to actuators distributed on conductive fabric sheet for wearable tactile display,” in Proceedings of AsiaHaptics 2016, Kashiwanoha, Japan, November 2016, pp. 163–169.

[18] A. Noda and H. Shinoda, “Frequency-division-multiplexed signal and power transfer for wearable devices networked via conductive embroi-derries on a cloth,” in 2017 IEEE MTS-IF International Microwave Symposium Proceedings, Hawaii, USA, June 2017, pp. 1–4, TUFFI-21.

[19] Maxim Integrated. Application note AN3808: What is an iButton device? [Online]. Available: https://pdfserv.maximintegrated.com/en/an/AN3808.pdf

[20] Dallas Semiconductor. 1-Wire MicroLAN evaluation kit. [Online]. Available: https://datasheets.maximintegrated.com/en/ds/DS09/1K1.pdf

[21] E. Wade and H. H. Asada, “Wearable dc powerline communication network using conductive fabrics,” in Robotics and Automation, 2004. Proceedings. ICRA ’04. 2004 IEEE International Conference on, vol. 4, April 2004, pp. 4085–4090 Vol.4.

[22] E. R. Wade and H. H. Asada, “Design of a broadcasting modem for a dc plc scheme,” IEEE/ASME Transactions on Mechatronics, vol. 11, no. 5, pp. 533–540, Oct 2006.

[23] NXP Semiconductors, “UM10204: I2C-bus specification and user manual, Rev. 6,” 2014. [Online]. Available: https://www.nxp.com/docs/en/user-guide/UM10204.pdf

[24] H. C. Ferreira, H. M. Grove, O. Hooijen, and A. J. H. Vinck, “Power line communications: an overview,” in AFRICON, 1996., IEEE AFRICON 4th, vol. 2, Sep 1996, pp. 558–563 vol.2.

[25] C. Kashiwanoha, E. Wade, and H. H. Asada, “Reduced-cable smart motors using dc power line communication,” in Proceedings 2001 ICRA. IEEE International Conference on Robotics and Automation (Cat. No.01CH37164), vol. 4, May 2001, pp. 3831–3838 vol.4.
[26] K. V. S. Rao, P. V. Nikitin, K. V. S. Rao, and P. V. Nikitin, “Theory and measurement of backscattering from RFID tags,” IEEE Antennas and Propagation Magazine, vol. 48, no. 6, pp. 212–218, Dec 2006.

[27] D. Bharadia, K. R. Joshi, M. Kotaru, and S. Katti, “BackFi: High Throughput WiFi Backscatter,” in Proceedings of the 2015 ACM Conference on SIGCOMM (SIGCOMM ’15), London, UK, August 2015, pp. 283–286.

[28] B. Kellogg, V. Talla, S. Gollakota, and J. R. Smith, “Passive Wi-Fi: Bringing Low Power to Wi-Fi Transmissions,” in Proceedings of the 13th USENIX Symposium on Networked Systems Design and Implementation (NSDI ’16), Santa Clara, CA, USA, March 2016, pp. 151–164.

[29] Microchip Technology, Tip #6 Data Slicer, 2009, ch. 4, pp. 4–7. [Online]. Available: http://ww1.microchip.com/downloads/en/DeviceDoc/01146B.pdf

[30] PJRC.COM, LLC. Teensy USB Development Board. [Online]. Available: https://www.pjrc.com/store/teensy32.html

[31] NXP Semiconductors. (2012) Kinetis K20: 72MHz Cortex-M4 up to 288KB Flash (64 pin) (REV 3). [Online]. Available: https://www.nxp.com/docs/en/data-sheet/K20P64M72SF1.pdf

[32] R. M. Foster, “A reactance theorem,” The Bell System Technical Journal, vol. 3, no. 2, pp. 259–267, April 1924.

[33] EPCOS AG. Inductors - LTspice. [Online]. Available: https://en.tdk.eu/tdk-en/523002/design-support/design-tools/inductors/model-libraries-for-smt-and-leaded-inductors/ltspice

[34] Linear Technology. LT5534: 50MHz to 3GHz RF Power Detector with 60dB Dynamic Range Data Sheet. [Online]. Available: http://www.analog.com/media/en/technical-documentation/data-sheets/5534fc.pdf

[35] Rohm Co., Ltd. (2016) Input Full Swing, Push-pull Output CMOS Comparators - BUS265HFV. [Online]. Available: https://www.rohm.com/datasheet/BU5265HFV/bu5265xxx-e

[36] A. Noda and H. Shinoda, “I2C-enabled batteryless sensors on double-layered conductive fabric,” in Proceedings of the 15th IEEE Conference on Body Sensor Networks, Las Vegas, NV, USA, Mar. 2018, p. 1.

[37] Silicon Laboratories. Si5351A/B/C-B I2C-Programmable Any-Frequency CMOS Clock Generator + VCXO Datasheet. [Online]. Available: https://www.silabs.com/documents/public/data-sheets/Si5351-B.pdf