Development of Frequency Discriminated Simulative Target Generator Based on DRFM for Radar System Performance Evaluation

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Abstract

Simulative target generators are needed for testing and calibrating various radar systems. The generator in this study discriminates the transmitting frequency from a radar and simulates parameters like target range, range rate, and atmospheric attenuation using the digital RF memory technique. The simulative target echo is then sent to the radar for testing and evaluation. This paper proposes a novel architecture for controlling the digital RF memory so it continually writes ADC data to the memory and reads it for the DAC with increasing one step address in order to control the delay of target range in a simple way. The target echo is programmed according to various preprogrammed scenarios and is generated in real time using a wireless local area network (LAN). To analyze the detected and generated target information easily, the system times for the radar and simulative target generator are synchronized using a global positioning system (GPS).

Key words: Doppler Radar, Digital Radio Frequency Memory (DRFM), Simulative Target Generator, Test Equipments.

I. Introduction

Radar is a critical element of many surveillance systems that are utilized both by civilians and the military. Its roles include target detection and identification, navigation and mapping, target tracking, and weapons guidance. Modern radar is capable of extracting surprisingly accurate parametric information about its targets including range, bearing, velocity, configuration, and identity.

A simulative target generator is essential to test and calibrate various radar systems under real operational environments [1]–[3]. The simulative target generator picks up radar transmitting signals and re-transmits them with variable parameters to the target. The major parameters of the radar signals, such as the apparent range, velocity, and atmospheric attenuation, are adjusted [4]–[6]. The generator can normally simulate a point air target as well as clutter and jamming signals.

This kind of target generator works with either analog delay technology using a fiber-optic device or digital delay technology using digital RF memory (DRFM). The fiber-optic delay method is generally used for short range radars due to the limitation of range delay; its utility depends on the (typically short) physical length of fiber-optic line. For medium and long range radars, DRFM technology is widely applied because it theoretically has no limitation of range delay. DRFM is a technique in which high speed sampling and digital memory are used for the storage of radio frequency signals. The incoming RF waveform is downshifted in frequency and sampled in a large number of data that must be acquired at very high speed over the duration of a received radar pulse.

The sampled waveform is stored in high speed memory, recalled with an appropriate delay, and is then re-transmitted with a target Doppler frequency for a Doppler radar system [7].

Although it has seemingly desirable properties, in practice a DRFM-based simulative target generator is vulnerable to the generation of the spurious signals from broad out-of-band signals aliased into the system bandwidth. The spurious signals generate the wrong target information, such as the incorrect position of a target, if the radar has various kinds of pulsewidth, PRI (Pulse Repetition Interval), and dwell characteristics. Therefore, when implementing a DRFM system, it is very difficult to control an appropriate time delay after radar time-tags pulse and to modulate the exact Doppler frequency without knowing the RF frequency in a wideband system.

This paper describes the development of a frequency
discriminated simulative target generator based on DRFM. A frequency discriminator (FD) located at the RF front-end of a system for a medium PRF radar automatically identifies the radar frequency in order to minimize spurious signals by reducing instantaneous bandwidth and to calculate the exact Doppler frequency in accordance with how frequency changed with each burst. This paper proposes a novel architecture for controlling the digital RF memory that continuously writes ADC data and reads it for the DAC with increasing one step address in order to control the delay of target range in a simple way. An appropriate time delay is easy to apply by using the differences in addresses between the writing and reading times in digital RF memory instead of relying on external time delay counts after each time-tag pulse. The Doppler frequency can also be modulated with RF frequency information in the FD because that information is put into a high-speed digital direct synthesizer and changes the local reference signal in the simulative target generator. The target echo is preprogrammed for different scenarios and is generated in real time during the test using a wireless local area network (LAN). To analyze the detected and generated target information easily, the system times for the radar and simulative target generator are synchronized using a global positioning system (GPS).

II. Frequency Discriminated Simulative Target Generator Based on DRFM (FDSG)

In a DRFM-based simulative target generator, it is difficult to avoid spurious signals and to modulate the exact Doppler frequency without knowing the RF frequency in a wide instantaneous bandwidth system. It is also difficult to implement the delay line of the key function of DRFM using a delay count method from input time-tags. To overcome these disadvantages, we propose a new FDSG; its block diagram is shown in Fig. 1.

The FDSG is designed using a DRFM that converts a radar waveform into a digital signal and inserts a function that automatically identifies radar frequency in order to minimize instantaneous bandwidth. A frequency discriminator located at the RF front-end of the system identifies the radar frequency channel code and converts the RF received radar signal into IF. A digital memory processing part performs the time delay function for the received radar signal. The frequency and Doppler calculations and MPRF processing are also performed using FPGA logic in accordance with the operating data processing program, found in a single board computer (SBC). A high speed frequency synthesizer performs Doppler modulation that changes the local reference signal. For example, an atmospheric attenuation part adjusts the target power and makes it constant or inverse 4th power of distance. In the output stage the noise source generates the noise jamming signals to measure radar ECCM capabilities.

2-1 Frequency Discriminator (FD)

The simulative target generator is designed to identify a radar frequency in accordance with a channel number because of knowing the frequency of the radar system before test. After downshifting the RF frequency channel, the parallel \( M \) down-mixer modules are deployed to generate four kinds of IF signals by using different heterodyne frequencies. Generally a down-converter generates two kinds of detecting signals, \((f_r - f_{local})\) and \((f_{local} - f_r)\), due to the mixing function of the converter with an imaginary band. It is difficult to identify the exact frequency in a FD. In this instance, two combinations in matrix \( M \times 4 \) designate the identical radar frequency. \( M \) down-converter modules are divided into two parts; the allocated heterodyne frequencies for avoiding discrimination error are allocated in Table 1. \( f_{lo} \) is a local frequency of a first down-mixer module. Because an imaginary band of the down-mixer module should be rejected, only one combination in matrix \( M \times 4 \) discriminates a frequency of radar signal.

The \( M \) parallel outputs of the down-mixer module are combined into one signal line through each \( M/2 \)-to-1 combiner and applied to each four different filters characteristics. One of the received radar frequency channels is determined by using the \( M/2 \times 4 \) matrix combination from \( M/2 \) down-mixer modules and four filter outputs. Therefore two \( M/2 \) down-mixer signals with imaginary signal transfers to second each four filter outputs, which define individual image signals from matrix \( M \times 4 \). The block diagram of the proposed FD is shown in Fig. 2.
The filters cannot completely reject the whole out-of-band signals, though; further complicating the problem is that the spectrum properties near the carrier frequency are widened as the inverse of radar pulse width. Because of these characteristics, the accuracy and stability performance of the frequency discriminator worsens. In the developed FDSG, the priority order algorithm that is adopted discriminates image signals from matrix \( M \times 4 \) using the empirical data sheets to minimize the error of discrimination. The discrimination time is a critical element of the minimum detection range in radar performances. The shorter time is good for a minimum detection range but it increases the possibility of generating a discriminating error. Here the priority order algorithm is based on the clock counter, so the discriminating time could be about 3 \( \mu s \) in this FD.

2-2 Digital Memory Processing (DMP)

The FPGA’s DMP part controls the 16-bit ADC, DAC, and a high speed memory. The sampling frequency for the ADC and the DAC is a critical factor in radar resolution. In this DMP the sampling frequency is 100 MHz, so memory data stores every 10 ns. In other words, the range resolution of this system is 1.5 m. In this novel target simulator, the proposed operation principles of the high speed memory are shown in Fig. 3 and Fig. 4. The DMP always operates the ADC process, storage, reading, and DAC for all continuous input signals without an external trigger signal. The storage space for memory

![Fig. 3. The operating concept of a circled digital RF memory access.](image3)

![Fig. 4. An operational example of 30 ns time delay.](image4)
becomes full due to size limitations. If a circular structure for memory storage is adopted (as it is in Fig. 3), it is possible to block the saturation of memory space by relocating the zero address again at the end of the address. The addresses are relocated because the data is useless after the maximum delay time.

The conventional DRFM structure needs an external trigger to determine the starting point of ADC and the storage duration to control target range information. The designed DRFM structure in which the memory is continuously operating offers great stability because no phase error related to generating an external trigger occurs. The structure is also easily applicable to simple timing circuit implementation by using the address differences between the writing and reading times for DRFM.

2-3 MPRF (Medium PRF) Processing

The digital range delay method utilizing the memory address information is needed to develop an additional control of generating pulse signals applicable to the latest MPRF radar. In MPRF radar some range delay is so long that the previous burst pulse signal can be alive even during the new burst timing period. In order to resolve this problem, additional memory is allocated to store the designated target scenario information such as radar frequency, Doppler frequency and range are delayed as soon as a new pulse signal comes into the system. The block diagram of the MPRF processing is shown in Fig. 5.

When a new pulse signal comes in, the RF frequency is discriminated within a few μs and the MPRF processing system maintains the previous RF frequency information until all pulse signals are less than the current designated range delay. If the previous pulse signals disappear as compared with the range delay, the MPRF processing system updates the current frequency data and sends current pulse signals.

Fig. 5. The block diagram of the MPRF logic.

Fig. 6. The block diagram of the frequency synthesizer.

2-4 High-speed Frequency Synthesizer

A frequency synthesizer is needed to generate a LO (Local Oscillator) signal that is then added to Doppler frequency for up-converting an input signal. The synthesizing time of the frequency synthesizer is critical factor for system performance for a minimum target range. PLL that is mainly used for frequency synthesizers is inappropriate for systems that request high speed frequency synthesizers on account of lock time, from dozens of μs to numerous ms. Meanwhile, a DDS (Digital Direct Synthesizer) can synthesize rapidly, but it is limited by digital circuits that generate microwave band signals. Therefore, this simulative target generator makes it possible to produce a high frequency output rapidly by using the frequency multiplication of the DDS output. Fig. 6 shows the block diagram for the high speed frequency synthesizer.

2-5 Atmospheric Attenuation

The signal strength of FDSG is based on radar range equations like Eq. (1) and Eq. (2). Eq. (1) represents the expected radar receiver power level in relation with the simulative target range. Eq. (2) represents the expected radar receiver power level in relation with the installation parameters for the radar and simulative target generator.

\[
P_r = \left( P_i \lambda^2 G_r G_a \right) / \left( 4\pi R^4 \right)
\]  

(1)

where

- \( P_i \): radar Tx power (dBm)
- \( \lambda \): wavelength (m)
- \( G_r \): radar Tx antenna gain (dBi)
- \( G_a \): radar Rx antenna gain (dBi)
- \( \sigma \): RCS (m²)
- \( R \): target range (m)

\[
P_r = P_i G_r G_a G_{\text{Rx}} G_{\text{gain}} \frac{\lambda^4}{(4\pi R^4)}
\]  

(2)

where

- \( G_{\text{Rx}} \): target simulator Rx antenna gain (dBi)
- \( G_a \): target simulator Tx antenna gain (dBi)
- \( G_{\text{gain}} \): target simulator system gain (dB)
- \( R_i \): distance between radar and simulator (m)

The signal strength of the FDSG can be calculated
from Eq. (3) by equalizing two expected receiver power levels of the radar. All parameters except the target range and RCS are constant values determined from installation conditions in Eq. (3). Therefore, the signal strength level of FDSG can be adjusted under a given target range and RCS represents atmospheric attenuation.

\[ G_{\text{signal}} = \frac{4\pi R^4}{R^2 G_p G_r \lambda^2} \]  

(3)

III. Fabrication and Test Results

3-1 Fabrication

To test and evaluate the developed medium range radar system, two frequencies discriminated simulative target generators based on DRFMs (FDSGs) are fabricated. The FDSGs are operated in a far-field radar test range to evaluate the accuracy and resolution performance of the radar. The test range is located in the Radar Simulative T&E Laboratory (RSTEL), located in the Agency for Defense Development in Korea. Fig. 7 shows the photograph of the fabricated FDSG, with dimensions of 550 (W)×520 (D)×410mm (H).

![Fig. 7. The photograph of the fabricated FDSG.](image)

3-2 Test Results

The time delay from the output pulse trigger is displayed for the simulated 100 km target range; it is 666 \( \mu \)s as shown in Fig. 8.

![Fig. 8. Test result of the delay of 100km target range.](image)

For the operation of receding scenarios, the received target signals are displayed by the inverse fourth power of radar distances as shown in Fig. 9.

![Fig. 9. Test result of the target receiver power related to the target range.](image)

The spurious signal level within the system bandwidth is \(-50\) dBc, as shown in Fig. 10.

![Fig. 10. Test result of the spurious signal level.](image)

The test results for calculating Doppler frequency are shown in Fig. 11. Even though the target velocity is constant, the Doppler frequency should be changed depending on the radar frequency in accordance with the Doppler equation \( f_d = \frac{2v}{\lambda} \). After discriminating the radar frequency the FDSG calculates the Doppler values.
IV. Conclusion

In this paper, the development of the FDSG based on DRFM for testing and calibrating the MPRF radar systems are described. Each part of the FDSG performs well and can be adjusted according to particular design requirements. DRFM technology developed in this simulative target generator can be applied to the next generation of radar environment simulators and wideband receiver signal processors [8]. As demands for sustainable progressing test environments increase, experiments such as this one provide guidance to meet these different requirements.

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