Measurement of single event effect cross section induced by monoenergetic protons on a 130 nm ASIC

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ABSTRACT: Designing integrated circuits in radiation environments such as the High Luminosity LHC (HL-LHC) is challenging. Integrated circuits will be exposed to radiation-induced Single Event Effects (SEE). In deep sub-micron technology devices, the impact of SEEs can be mitigated by triple modular redundancy. The triplication of the most sensitive data is used to recover most of the data corruption induced by interacting particles. One type of SEE, called single event upset (SEU), is studied in this paper. The SEU cross-section and the performance of the triplication are estimated using an ASIC prototype exposed to a beam of protons. The SEU cross-section is measured and systematic difference between $1 \rightarrow 0$ and $0 \rightarrow 1$ bit flip rates is observed. The efficiency of the mitigation method is investigated.

KEYWORDS: Radiation-hard electronics; Digital electronic circuits; Radiation-hard detectors

ArXiv ePrint: 2112.05720

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1 Introduction

Designing integrated circuits in radiation environments such as the High Luminosity LHC (HL-LHC) is challenging. Integrated circuits will be exposed to radiation-induced Single Event Effects (SEE), especially Single Event Upsets (SEU). In deep sub-micron technology devices, the impact of SEE can be mitigated by triple modular redundancy [1, 2]. The triplication of the most sensitive data is used to recover the data corruption induced by interacting particles.

SEU can be studied with different types of ionizing particles [3]. Heavy Ions can be used, offering the advantage of testing an extensive range of Linear Deposit Energies (LETs). However, a model has to be used to extrapolate the measurements to the final environment. Protons of at least 20 MeV can be used to estimate the SEU effect, especially for the HL-LHC environment where the detector components are shielded against low-energy particles and where the expected fluences are usually expressed in unit number of 1 MeV neutrons equivalent per squared centimeter, $n_{eq}^{1\text{MeV}} \text{cm}^{-2}$ unit. The energy dependence can be taken into account to refine the predictions.

In this paper, the SEU cross-section and the performance of the triplication are estimated using an ASIC prototype exposed to a monoenergetic beam of protons. This tested ASIC mainly contains a static random-access memory (SRAM) system made of flip-flops, capable of handling a latency of 38.4 $\mu$s, required by the trigger system of the experiment. This SRAM is naturally sensitive to SEU, mitigated by auto-correction using triplication.

This paper aims to determine the bit flip rate on a 130 nm technology. The corresponding SEU cross-section $\sigma_{SEU}$ was measured in [4] and is expected to be in the order of $\sigma_{SEU} = (6 \pm 1) \times 10^{-14} \text{cm}^2$. This rate, combined with a triplication design, leads to a residual auto-correction failure rate. This
failure rate is estimated for an 1600 bits ASIC, and it has to be negligible during an average data-taking period of 1 day.

Section 2 describes the facility and the setup used to collect the data. The data are analyzed in section 3, and three results are presented:

- the SEU cross-section for single bits,
- an estimate of the triplication failure rate using as a study case a 1600 triplicated bit ASIC at the HL-LHC, and
- the direct measurement of triplication failures.

2 Experimental setup

2.1 The MEDICYC facility and beam monitoring

The SEU cross-section was measured during a test beam campaign at the Centre Antoine Lacassagne (CAL) in 2021, where the MEDICYC cyclotron [5, 6] provides proton beams. MEDICYC is equipped with several proton beamlines, two of which are in operation at the moment. A clinical beamline provides proton therapy of ocular melanoma. A research beamline has recently been equipped and is proposed to researchers and industry for R&D programs.

The subsequent measurements were performed using the low energy treatment line, where a 62.0 MeV proton beam was produced with up to 300 nA intensity. This energy corresponds to a LET value of 8.7 keV cm²/mg in silicon dioxide. The beamline calibration and monitoring control the intensity at the 3 per mil level at the highest intensity.

2.2 Integrated circuit and data taking

The 130 nm TSMC ASIC prototype was designed to test the performances of digital blocks when exposed to radiation. One of these tests is dedicated to the SEE study. Sixty-four 8-bit registers were implemented and accessible through an I²C port. They are fully dedicated to SEU counting, and their outputs have no other function in the chip. Each bit of a register is triplicated, and automatic corrections are applied to every triplicated-bit of the register at 40 MHz using a majority voter logic.

Each triplicated flip-flops are physically spaced by 15 μm in the layout and shown in figure 1. The implementation of the Register Transfer Level (RTL) is done with a 2008 version of the CERN TMRG tool [7]. It is integrated with the digital flow to automatize the process of triplication. The TMRG toolset generates constraints that ensure that triplicated items are not placed too close to each other while allowing the designer to decide which blocks or signals will be triplicated. The clock, reset, and control signals are not triplicated in the ASIC prototype. The reset is synchronous with the 40 MHz clock, and each register can have a different reset value. If only one flip-flop has its value changed due to SEU, the voted value is overwritten inside the faulty flip-flop thanks to the auto-correction system. The voter also raises an error flag if the three flip-flops do not have the same value. This error flag is then used to increment counters to count SEU. Four counters are associated with the correction mechanism. Each counter covers 16 registers, called groups, and is incremented by one if a correction is applied to any one of them. The four counter values are stored in triplicated registers. The total number of bits monitored in the SEU rate measurement is 1536.
Figure 1. View of the ASIC where the flip-flops are highlighted by white rectangles.

Figure 2. View of the ASIC (located under a black resin) on its host board mounted on the beamline.

The ASIC is mounted on a custom board, shown in figure 2, that routes the power supplies, the clock and various probe signals.

A microcontroller, linked to an I²C, is used to communicate with the ASIC, read or reset the counters, and control the register contents. External devices ensure a 40 MHz clock as well as a power supply. The various counters were readout, and the registers reinitialized, after each reading, with predefined words at a typical frequency of 100 Hz.

The ASIC was aligned with the proton beam covering the device surface with a homogeneity better than 5%. Data were recorded using two beam intensities during several data-taking periods, four at high intensity and one at low intensity. The ASIC was exposed to a total fluence of \(8.7 \times 10^{14} \text{ p cm}^{-2}\).
Figure 3. Cumulative number of auto-corrections before (top) and after (bottom) offline corrections from data corruption and overflow in the counter.

3 SEU cross-section measurement and auto-correction failure

Two methods are presented to measure the SEU cross-section. The first one relies on the error rate measurement (section 3.1). The second method exploits the randomness of the SEU, which must result in duration between two consecutive errors $\Delta t$ distributed according to a decreasing exponential (section 3.2).

Two methods are presented to estimate the auto-correction failure rate. The first one is based on the probability of having two simultaneous SEUs in a triplicated system. It is computed from the measured SEU cross-section (section 3.3). The second method consists in counting the actual number of events in which the auto-correction failed (section 3.4). For completeness, a Monte Carlo simulation is performed and compared to data (section 3.5).

3.1 SEU cross-section

The registers were set to 0 during one period and to 1 during four periods. The SEE rate estimate relies on the auto-correction counters. These SEE counts are expected to be mainly induced by SEU. A few jumps in the counters were observed and are interpreted as non-corrected SEEs on the counter itself. These jumps are then filtered in order to keep only jumps related to SEU. Also, when a counter reaches 255 it goes back to zero at the next incrementation. These resets are also corrected. The number of errors before and after treatment is shown in figure 3 as a function of time for one of the periods and groups. The number of errors normalized to the beam intensity is used to extract the SEU cross-section per bit, as summarized in table 1. A rate is computed for each period and group, and a global rate is obtained by fitting these individual values assuming an
error occurrence following a Poisson distribution. The rate as a function of time, as well as the fit result for the sixteen datasets at high intensity, are shown in figure 4. The final rate value, and its uncertainty is derived from the mean and the mean error over the different periods and groups. The average cross-section is estimated to be

$$\sigma_{\text{SEU}^{1-0}} = (7.90 \pm 0.13) \times 10^{-14} \text{ cm}^2$$

$$\sigma_{\text{SEU}^{0-1}} = (6.77 \pm 0.41) \times 10^{-14} \text{ cm}^2.$$

The systematic difference between $1 \rightarrow 0$ and $0 \rightarrow 1$ bit flip rates is significant and already reported, eg. in ref. [4]. The dependency to the LET, and therefore to the beam energy, as shown in refs. [3, 8], has to be considered for extrapolations at different energy scales.

### 3.2 Distribution of time duration between two errors

The probability that SEE occurs is assumed to be constant. In that case, one can show that the distribution of the time between two consecutive errors follows a decreasing exponential

$$p(\Delta t) \propto \exp(-\Delta t/\tau)$$

where $\tau^{-1}$ corresponds directly to the probability. Looking at the $\Delta t$ allows then to verify the assumption of a constant probability, and to extract this probability.

In practice, error counters of every single bit are incremented every 25 ns, but these individual counter values are summed to form one counter per group, every $\sim 8$ ms. These values are

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**Figure 4.** SEU cross-section computed every second for the four groups (row) of the four periods (column). The red line corresponds to the fit result over the whole period. The index of the group and period and the fitted value are specified on top of each sub-figure.
Table 1. SEE cross-sections, $\sigma_{\text{SEU}}$, per bit for all the registers and different periods, measured using two beam intensities, $I$. The 64 registers are combined in four groups numbered from 1 to 4. The uncertainties assigned to the measurement from individual periods combines the statistical error with the uncertainty on the beam intensity. The uncertainty on the average is computed using the spread of the individual measurements.

| $I$ [nA cm$^{-2}$] | Period | Group | $\sigma_{\text{SEU}}$ [10$^{-14}$ cm$^2$] |
|-------------------|--------|-------|----------------------------------|
| 3.1 ± 0.1         | period 1 | 1     | 7.97 ± 1.13                      |
|                   |        | 2     | 6.37 ± 1.01                      |
|                   |        | 3     | 5.74 ± 0.96                      |
|                   |        | 4     | 7.01 ± 1.06                      |
| Average           |        |       | 6.77 ± 0.41                      |
| 299.9 ± 1.3       | period 1 | 1     | 6.88 ± 0.25                      |
|                   |        | 2     | 7.50 ± 0.25                      |
|                   |        | 3     | 7.30 ± 0.25                      |
|                   |        | 4     | 7.11 ± 0.25                      |
| period 2          | 1     | 8.52 ± 0.36 |
|                   | 2     | 7.74 ± 0.34 |
|                   | 3     | 8.64 ± 0.36 |
|                   | 4     | 8.61 ± 0.36 |
| period 3          | 1     | 7.60 ± 0.12 |
|                   | 2     | 7.75 ± 0.12 |
|                   | 3     | 7.82 ± 0.12 |
|                   | 4     | 7.89 ± 0.12 |
| period 4          | 1     | 8.21 ± 0.30 |
|                   | 2     | 8.48 ± 0.31 |
|                   | 3     | 8.13 ± 0.30 |
|                   | 4     | 8.20 ± 0.30 |
| Average           |       | 7.90 ± 0.13 |

read out and saved every 10 ms. Therefore, the smallest measured $\Delta t$ value is 10 ms. A counter incrementation translates the number of errors, $n$, that occurred during this time window. When there is more than one error $n > 1$ in a time window, it is assumed that those errors are equally distributed in time, meaning there are $n$ time intervals of $10/n$ ms each. The distribution of $n$ for all the 10 ms time windows, and the distribution of the time interval $\Delta t$ for which the counter incrementation is at least one are shown on figure 5.

The distribution and the fitted exponential function for all analyzed data are shown on figure 6. As for section 3.1, the final value and uncertainty are taken from the average over the various datasets.
Figure 5. Time difference between two consecutive errors (left) and error multiplicity between two consecutive errors (right).

Figure 6. SEU cross-section computed from exponential fit of $\Delta t$ distribution for the four groups (line) of the four periods (column). The red line corresponds to the fitted exponential distribution. The index of the group and period as well as the fitted cross-section values are specified on top of each sub-plot.

The obtained value of $\tau$ corresponds a SEU cross-section of $\sigma_{SEU}^{1\rightarrow0} = (7.44 \pm 0.16) \times 10^{-14}$ cm$^2$. This value depends on the number of bins chosen to fit the $\Delta t$ distribution, increasing by 12% when moving from 30 bins (used for the above value) to 100 bins. As a consequence, this result is compatible with the measurement described in section 3.1.
Table 2. Predicted number of auto-correction failures due to uncorrelated SEUs, assuming an instantaneous fluence of $10^8 \text{n}_{\text{eq}}^1 \text{MeV cm}^{-2} \text{s}^{-1}$. $N_{\text{trip-bit}}^{\text{HL-LHC}}$ is the expected number of auto-correction failures for one triplicated-bit. $N_{\text{ASIC}}^{\text{HL-LHC}}$ is the expected number of auto-correction failures for a 7200 triplicated-bits ASIC during 1 day.

| $N_{\text{trip-bit}}^{\text{HL-LHC}}$ | $N_{\text{ASIC}}^{\text{HL-LHC}}$ |
|------------------------------------|----------------------------------|
| 1 → 0                             | $(4.0 \pm 0.1) \times 10^{-13}$  |
| 0 → 1                             | $(2.9 \pm 0.1) \times 10^{-9}$   |

3.3 Auto-correction failure due to time-overlapping SEU

One mechanism that induces auto-correction failures is when two replicas of a single bit are affected by two SEUs during the correction cycle of 25 ns. The rate of the auto-correction failure can be deduced from the SEU rate. The probability of two cell flips within a triplicated bit system can be written as:

$$P = C_2^2 \int_0^{T_c} \sigma_{\text{SEU}} f \, dt \int_0^{T_c} \sigma_{\text{SEU}} f \, dt = 3 \sigma_{\text{SEU}}^2 f^2 T_c^2$$

where $T_c$ is equal to 25 ns and $f$ the instantaneous fluence. Inner detectors in the ATLAS [9] and CMS [10] experiments will be exposed to a typical integrated fluence of $10^{15} \text{n}_{\text{eq}}^1 \text{MeV}$ [11, 12] during the HL-LHC. As indicated by equation (3.2), uncorrelated double flips depend quadratically on the instantaneous fluence. The auto-correction failure rate is estimated assuming an instantaneous fluence of $10^8 \text{n}_{\text{eq}}^1 \text{MeV s}^{-1}$ and given in table 2. Each ASIC will have a negligible number of alterations of its registers during its lifetime due to uncorrelated double bit flips.

3.4 Observation of auto-correction failures

The auto-correction failure rate was measured by seeking changes in the 64 register contents. Three measurements were performed with high intensity proton beam, using three register configurations:

- registers filled with 1,
- registers filled with a 11111110 frame,
- registers filled with 0.

The associated countings are provided in table 3. Significant statistical uncertainties are assigned to this measurement due to the small number of total errors. When no error is measured, a limit is set with a 95% confidence level.\(^1\) It was checked that the failures affect single bits of different registers with no identified pattern. The location of these registers is shown on figure 7. The observed rate was extrapolated to HL-LHC integrated luminosity assuming a quadratic dependence to the fluence, as described by equation (3.2). Comparing table 2 and 3, one can see that the observed $0 \rightarrow 1$ uncorrected errors are of the order of $10^6$ larger than what is expected from double SEUs. This rate suggests that other mechanisms should be considered, including Single Event Transients (SET). Additional measurements should be done in the future to confirm this rate.

\(^1\)It can be shown that an upper limit of $\approx 3$ is assigned to the counting of 0 under a Poisson law with a confidence level of 95%.
Figure 7. View of the ASIC where the flip-flops are highlighted by white rectangles. The 9 registers where a data corruption was observed are shown.

Table 3. Number of auto-correction failures over all the registers, measured using three data frame configurations. $N_{\text{trip-bit}}^{\text{HL-LHC}} (N_{\text{ASIC}}^{\text{HL-LHC}})$ is the expected number of failures per triplicated-bit (per 7200-triplicated bits ASIC) when extrapolating the observed errors to the HL-LHC fluence.

| Frame     | Duration [s] | Errors | $N_{\text{trip-bit}}^{\text{HL-LHC}}$ | $N_{\text{ASIC}}^{\text{HL-LHC}}$ |
|-----------|--------------|--------|--------------------------------------|------------------------------------|
| 11111111  | 610          | 0      | < $1.1 \times 10^{-7}$               | < $0.8 \times 10^{-3}$            |
| 111111110 | 740          | 0      | < $0.9 \times 10^{-7}$               | < $0.7 \times 10^{-3}$            |
| 000000000 | 530          | 9      | $(3.9 \pm 1.3) \times 10^{-7}$       | $(2.9 \pm 0.9) \times 10^{-3}$    |

3.5 Cross-checks based on simulation

The simulation randomly generates SEE events every 1 ms for each of the 1536 bits, with a given probability. Every 8 ms, the counters of individual bits are summed together to form the four general counters, as in the experimental data. Every 10 ms, the cumulative error counts are written for each of these four counters.

Figure 8 shows a comparison between the observed data and the simulation for three observables, namely the number of errors as a function of time, the distribution of the time between two consecutive errors, and the error multiplicity between two consecutive errors. The assumption of a time-independent probability of error occurrence describes quite well the observed data. However, the simulation does not explain the error rate at a very short time since the observed number of 4 errors in 10 ms interval is much larger than the predicted one. This observation goes in the same direction as the tension mentioned in section 3.4, where the number of explicit double errors measured every 25 ns is much higher than the double error rate computed from the single error probability.

4 Conclusion

An ASIC prototype was designed to monitor the impact of radiation-induced errors on a 130 nm technology. It was exposed to a high-intensity proton beam. Using specific counters, the SEU
cross-section was measured using 62 MeV protons considering both $1 \to 0$ and $0 \to 1$ bit flip observations. It was also shown that SEEs can be significantly mitigated by triple modular redundancy. While the single error rate obtained with a 130 nm TSMC technology follows the expectations, the significant uncorrected error rate observed in the direct measurement requires further studies. A new prototype with an improved implementation of the triplication using the latest TMRG tools will be designed and tested.

Acknowledgments

We would like to thank the MEDICYC staff from the Centre Antoine Lacassagne for their availability and their precious help before and during the irradiation period.

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