Ball-grid array architecture for microfabricated ion traps

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State-of-the-art microfabricated ion traps for quantum information research are approaching nearly one hundred control electrodes. We report here on the development and testing of a new architecture for microfabricated ion traps, built around ball-grid array (BGA) connections, that is suitable for increasingly complex trap designs. In the BGA trap, through-substrate vias bring electrical signals from the back side of the trap die to the surface trap structure on the top side. Gold-ball bump bonds connect the back side of the trap die to an interposer for signal routing from the carrier. Trench capacitors fabricated into the trap die replace area-intensive surface or edge capacitors. Wirebonds in the BGA architecture are moved to the interposer. These last two features allow the trap die to be reduced to only the area required to produce trapping fields. The smaller trap dimensions allow tight focusing of an addressing laser beam for fast single-qubit rotations. Performance of the BGA trap as characterized with $^{40}$Ca$^+$ ions is comparable to previous surface-electrode traps in terms of ion heating rate, mode frequency stability, and storage lifetime. We demonstrate two-qubit entanglement operations with $^{171}$Yb$^+$ ions in a second BGA trap.

I. INTRODUCTION

Trapped atomic ions are a leading platform in quantum information research, offering the advantages of precise optical manipulation and long qubit coherence times. The transport architecture proposed for scalable trapped-ion quantum computing requires a complex system in which large numbers of ions are shuttled to various locations in the trap structure. Towards this goal, microfabrication techniques have enabled miniaturization of ion traps that allow for the incorporation of arrays of microfabricated electrodes on a planar substrate (see, for example, Refs.3–9). In the typical trap, surface electrode structures are fabricated on a thin chip that sits atop a commercial ceramic pin-grid array (CPGA) carrier. To supply DC trapping potentials for each electrode, pads on the CPGA are wirebonded to pads on the trap chip. Capacitors on the surface of the chip or bonded at the perimeter of the carrier are used to filter out radio frequency (RF) pickup on the electrodes.

Existing fabrication techniques will limit scaling surface-electrode ion traps far beyond those in use today. Recent trap designs have grown to incorporate nearly 100 DC control electrodes9. For linear traps with as few as 50 electrodes10, the capacitors and bond pads can consume a majority of the overall trap chip area and perimeter, strongly constraining the layout of electrode structures and DC/RF lead traces. Wirebonds must be carefully arranged to minimize obstructions to laser access, as beams for trapping and qubit manipulation must interact with ions confined $\approx 100 \mu$m above the chip surface. The large periphery (non-trap area) of the trap die presents geometric limitations to focusing these lasers onto the ion while maintaining the narrow beam waists preferred for operations such as addressing individual ions in a chain or driving hyperfine Raman transitions11–13. For example, a 729 nm beam for single qubit addressing, focused to a waist of 3.4 $\mu$m as in Ref.11, has a Rayleigh range of 0.05 mm and would diverge to a beam radius of 100 $\mu$m within 1.5 mm, incompatible with existing traditional surface trap dimensions. Novel trap architectures remove portions of the trap in several dimensions but are still constrained by wirebonds along two edges14.

We demonstrate here a new architecture for microfabricated ion traps, built around ball-grid array (BGA) connections. The BGA design (Fig. 1) mitigates scalability concerns related to the capacitors and wirebond connections, providing a flexible architecture for traps of increased complexity. Electrodes in the BGA trap are connected with through-substrate vias (TSVs) to pads on the back side of the trap die. Gold-ball bump bonds then connect these back-side pads to traces on an interposer. The interposer is wirebonded to a CPGA carrier for signal routing. The 100-pin Kyocera CPGA used here is compatible with our existing test setups; alternate carriers would require only a redesign of the relatively simple interposer, rather than modifications to the trap chip itself. Trench capacitors are fabricated into the trap die, similar to a proposal in Ref.15, reducing the trap die area by a factor of thirty over traps with planar capacitors. Filter capacitors located at the edge of the CPGA would be less effective in this architecture, due to distance from the trap. With the wirebond connections relocated to the interposer, the surface of the BGA trap chip remains unobstructed for laser access. Gold is utilized for the electrode surfaces, minimizing oxide formation which is

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Figure 1. Overview of the BGA design: (a) Die bond region of the CPGA showing the BGA trap and the interposer footprint. (b) Side view. (c) Fully packaged BGA trap. The long bond wire supplies the trap RF signal.

II. FABRICATION

A. Overview

The BGA trap includes 48 trench capacitors and 48 TSVs connected to a total of 48 DC electrodes. A schematic cross section of the BGA trap is shown in Figure 2, highlighting the metal and insulator layers, trench capacitors, and TSVs. The trap die is bonded to an interposer (Sec. II B 2), which serves to elevate the trap above the carrier for improved laser access and to route electrical connections from the package to the trap die.

B. Processing Details

1. Trap Die Fabrication

The process for making the trap die begins with a 500 µm-thick p++ (heavily boron-doped) silicon wafer with a resistivity of 0.001 – 0.005 Ω-cm. The key fabrication steps are described below.

(i) Making TSVs: Figure 3 shows the complete process for forming the TSVs. Scanning electron microscope (SEM) images of the TSV features are shown in Fig. 4. The outlines for the TSVs are patterned with donut-shaped features and etched ≈ 340 µm into the wafer using a Deep Reactive Ion Etch (DRIE) tool (Fig. 3, step 1). The side and bottom walls of the TSVs are oxidized in a thermal oxidation furnace to a thickness of 1.5 µm (step 2). The trenches are filled with ≈ 6 µm of highly conductive p++ polysilicon, completely sealing the tops of the holes (step 3). A Chemical Mechanical Polish (CMP) is performed from the front side to expose the original bulk silicon wafer (step 4). Much later in the fabrication process (after front-side metallization), a back-side CMP operation (step 5) reduces the wafer thickness to 300 µm and exposes the TSV donut. The TSV resistances are 40 ± 2 Ω, with breakdown voltages in excess of 380 V, above the range of the test equipment used.

(ii) Making Trench Capacitors: Fabrication of the trench capacitors begins with DRIE of trenches arranged in concentric rings around the TSVs, 55-70 µm into the silicon wafer. Thermal oxide of thickness 60 nm is grown on the sidewalls of the trenches. The trenches are then filled with 0.5 µm of highly conductive p++ polysilicon, completely sealing the tops of the holes (step 3). A Chemical Mechanical Polish (CMP) is performed from the front side to expose the original bulk silicon wafer (step 4). Much later in the fabrication process (after front-side metallization), a back-side CMP operation (step 5) reduces the wafer thickness to 300 µm and exposes the TSV donut. The TSV resistances are 40 ± 2 Ω, with breakdown voltages in excess of 380 V, above the range of the test equipment used.

We characterize the BGA trap by loading single and multiple 40Ca+ ions. Performance of the trap is comparable to previous microfabricated surface traps in terms of ion heating rate, axial mode stability, and storage lifetime for one and two trapped ions. We take advantage of the reduced trap die size and improved optical access to demonstrate tighter focusing of a 729 nm laser beam with resulting speedup in single-qubit rotation rates. Results from the BGA ion trap testing are presented in Section III. We present in Section IV an initial demonstration of two-qubit entanglement with 171Yb+ ions in a second BGA trap.
itor processing (Fig. 5d), the trench capacitors remain electrically isolated from the TSVs by a thin oxide layer.

We measure capacitance values of $103.5 \pm 1.2 \, \text{pF}$ for the 48 trench capacitors on a trap die. Capacitance values in the final packaged trap increase to $118 \pm 3 \, \text{pF}$, with variation dominated by differences in the lengths and widths of lead traces and electrodes. Typical breakdown voltage for a trench capacitor is $\approx 18 \, \text{V}$, determined by testing 100 capacitors on a test wafer.

(iii) Making Ohmic Contacts to TSVs and Trench Capacitors: Once the trench capacitors and TSVs have been formed, a 1.0 $\mu$m layer of chemical vapor deposition (CVD) SiO$_2$ is deposited on top of the wafers. A layer of photoresist is patterned connecting the TSV cores and radial arms of the trench capacitors. The wafers are then etched using a RIE (Reactive Ion Etch) process. Once the underlying silicon has been reached, we form a platinum silicide layer, creating ohmic contacts on the tops of the trench capacitors and TSV cores. Front-side metallization, described below, then makes the electrical connection between each TSV and its associated trench capacitor.

(iv) Patterning Metal Layers: The three front-side metallization and dielectric layers are shown schematically in Fig. 2. The bottom most metal layer (M1) is essentially a large ground plane, interrupted only where there are TSVs. The second metal layer (M2) forms the trap DC and RF electrodes. A 10 $\mu$m oxide layer between M1 and M2 limits the capacitance of the RF electrodes. The last metal layer (M3) forms a top ground plane. Appendix A 1 provides additional fabrication details of the front-side metallization.
After M3 is patterned, a > 2 hour RIE step anisotropically removes exposed SiO₂ by etching in the vertical direction. A 3 µm BOE (Buffered Oxide Etch) process then etches the SiO₂ laterally, leaving overhanging metal features which aid in screening dielectric from laser light during trap operation and which shield the ion to some extent from stray fields caused by trapped charge on the dielectrics.

On the back side of the trap die (Fig. 6), 48 silicided contacts make electrical connections to the cores of the TSVs and to bond pads; 28 contacts make ground connections to the bulk silicon part of the die. Gold and tin are deposited on the bond pads for gold/tin eutectic solder-bonding to the interposer (Sec. II C).

(v) Making Loading Slots: Slots in the trap die allow passage of a thermal flux of neutral atoms for ion loading (Sec. III A). The loading slot is coated with gold to minimize the potential for charge build-up. The etch that defines the loading slots also opens up the perimeters of each die so that the die are singulated (separated from one another and from the bulk wafer). Figure 7 shows a completed trap die after it has been removed from its carrier wafer.
2. Interposer Processing

The interposer is a separate die (1 cm × 1 cm by 1.3 mm-thick) whose purpose is to elevate the trap die above the rim of the package and to carry electrical signals from the package to the trap die. Signals are routed on two metal layers, each 1.7 µm Au with Ti and Pt adhesion/barrier layers above and below. Top and bottom ground layers (1.7 µm Au) provide electrical shielding. Slots for ion loading are DRIE-etched 300-350 µm into the front side of the interposer wafer and 1000 µm in from the back side, meeting to create a continuous opening that aligns with the loading slot in the trap die. Appendix A 2 provides details of the interposer fabrication process.

C. Assembly

For final assembly of the ion trap, we bond together the separately fabricated trap die and interposer, then package the combined unit into a CPGA carrier. A conventional gold ball bonder, programmed to leave short bond wires (≈ 75 µm from base to tip), attaches gold studs to the bond pads on top of the interposer (Fig. 8a). With the gold studs as interconnects, the trap die is bonded with a solder-reflow process to the interposer with previously deposited gold and tin layers acting as a gold/tin eutectic solder. A separate layer of gold studs is placed on the base of the CPGA package, and the interposer (plus trap) is ultrasonically bonded to the CPGA. Wirebonds are then attached from the interposer to the trap die, providing a low-resistance routing for the trap RF signal. The final packaged trap is shown in Figure 1c.

III. TESTING

A. Overview

We test the BGA trap by trapping ⁴⁰Ca⁺ ions, using techniques discussed in Refs. 10,20. An oven located below the CPGA carrier supplies neutral Ca atoms which pass through the loading slots in the interposer and trap chip and are photoionized 60 µm above the trap surface. A potential \( V_0 \cos(\Omega_{RF} t) \) is applied to the RF electrodes (Fig. 9), where \( V_0 = 95 \) V and \( \Omega_{RF} = 2\pi \times 55.14 \) MHz. This creates a ponderomotive pseudopotential which confines ions radially. Ions are confined axially by applying voltages to the DC electrodes and are transported by varying these voltages to translate the axial potential minimum.

For the following measurements, the axial mode frequency (Sec. III B) is 1.0 MHz and the radial frequencies are 4.2 MHz and 3.7 MHz. The experiments described below are performed with the ion at \( z = 488 \) µm (see Fig. 9).

Ions are manipulated with laser light directed parallel to the trap surface. We use a 397 nm laser tuned near the \( ^2S_{1/2} \rightarrow ^2P_{1/2} \) transition for Doppler cooling and state detection. Fluorescence is collected onto a charge-coupled device (CCD) camera and a photomultiplier tube. An 866 nm laser repumps ions out of the metastable \( ^2D_{3/2} \) level. With the Doppler cooling beam on, the storage lifetime for a Ca⁺ ion is several hours. With the Doppler cooling beam mechanically shuttered, the ion dark lifetime (50% average survival fraction) is 450 s for a single trapped ion (Fig. 10).

By measuring shifts in the ion equilibrium position as the harmonic trapping potential is varied, we map out stray axial electric field strength \( E_z \) over the length of the trap (Fig. 11). We are able to trap and transport the ion within a 1.2 mm region. Stray fields near the load zone edge reach several hundred V/m but drop well below 100 V/m at a distance of 100 µm from the load slot. These axial stray fields are comparable to those
Figure 9. Schematic of the BGA trap, showing RF electrodes (red), ion loading slot (white), ground planes (gray), and DC electrodes (teal). Positions are labeled along the trap symmetry axis ($z$).

Figure 10. Ion lifetime measurement without Doppler cooling. The dark lifetime (50% survival fraction) is 450 sec for a single ion (red triangles) and 35 sec for two co-trapped ions (black circles).

Figure 11. Stray axial field $E_z$ measurements over the BGA trap. Light blue box indicates region of the loading zone.

Figure 12. Carrier transition and motional sidebands for a trapped Ca$^+$ ion as a function of the 729 nm laser frequency. Gray peaks are due to adjacent carrier transitions (between different Zeeman sublevels) and their sidebands.

Axial mode stability is measured by repeatedly scanning over the axial red and blue sideband transitions (labeled “1st axial” in Fig. 12). The axial mode frequency remains within a range of 200 Hz (0.02%) over three hours (Fig. 13). Small shifts of $\approx 100$ Hz (0.01%) are observed due to ion reload events, which may result from charging of the trap surface by the loading beams. These reload shifts typically decay on a timescale of 5-10 minutes.

We use the average phonon occupation number $\bar{n}$ in the axial mode to determine ion heating rates. For low temperatures, $\bar{n}$ may be measured by comparing strengths of the 1st axial red and blue sidebands; i.e. $\bar{n} = x/(1 - x)$ where $x = I_{red}/I_{blue}$ is the ratio of sideband strengths$^{22}$. The ion is sideband cooled to $\bar{n} \approx 0.25$, then allowed to sit without any cooling for a controlled duration. Follow-
C. Multiple Ions

We load multiple-ion chains in a single potential well (Fig. 15). After calibrating transport waveforms to correct for stray electric fields in the $z$ direction (Fig. 11), we reliably co-transport multiple ions out of the load slot to our experiment zone at $z = 488 \, \mu m$. Transport success rates are near 100% for co-transport of two or three ions at speeds of 0.33 m/s or slower.

In the experiment zone, the two-ion storage lifetime is typically 1-2 hours with Doppler cooling and 35 seconds without (Fig. 10). Note that for a two-ion chain we define lifetime by the loss of either ion. The two-ion center-of-mass ($f_{z} = 1.0 \, MHz$) and stretch ($f = 1.73 \, MHz$) axial sidebands are identified in Fig. 16. In preparation for two-qubit operations, we sideband cool both axial modes to near the motional ground state, $\bar{n} < 0.5$ quanta in each mode.

D. Beam Focusing

A key advantage of the BGA architecture is the possibility to focus laser beams more tightly on the ion. Tighter focus of a gate beam can speed up qubit rotation times by increasing intensity at the ion while also reducing crosstalk to neighboring ions. A focused Gaussian beam will diverge in inverse proportion to ultimate beam waist; that is, a beam tightly focused above the trap surface will exhibit large angular spread as it enters and exits the trapping region. The dimensions of the trap chip and carrier thus impose a limit on how tightly we may focus the beam before scattering off some surface enroute.

We use various lens combinations to focus our 729 nm gate beam onto the trapped ion. The carrier Rabi rate
for single qubit rotations is proportional to the amplitude of the driving electric field (square root of laser intensity) at the ion. The laser beam profile is measured by translating the ion while holding the 729 nm laser fixed and measuring the associated Rabi frequency; beam waist radius is defined as the 1/e² half-width of intensity profile. Results for four different beam waists are shown in Fig. 17. The 729 nm beam is incident at 45° to the trap axis, giving rise to a factor of $\sqrt{2}$ between the physical beam waists and the effective beam waists as measured by this technique.

![Figure 17](image)

Figure 17. Effect of 729 nm gate beam focus on single qubit transition rate. Correcting for the 45° angle of incidence, the Gaussian fits indicate physical beam waist radii of 24.1 µm (red), 12.2 µm (black), 9.9 µm (blue), and 8.0 µm (green).

We model these results by measuring the collimated input beam with a beam profiler, then treating the focusing lenses as ideal optical elements to calculate effective beam waists at the ion. The tightest waist shown in Fig. 17 represents the approximate limit of beam focusing lenses as ideal optical elements to calculate effective beam waists at the ion. The laser beam profile is measured by translating the ion while holding the 729 nm laser fixed and measuring the associated Rabi frequency; beam waist radius is defined as the 1/e² half-width of intensity profile. Deviations from the Gaussian fit are evident in the wings of the 8 µm beam (green) in Fig. 17, indicating beam distortion. Beam waists of 10 µm or larger, meanwhile, are predicted to experience less than 1% power loss due to scattering.

### IV. ENTANGLING GATES

Two qubit entangling gates in Ca⁺ are highly sensitive to magnetic field noise in the laboratory. Subsequent to the Ca⁺ testing (Sec. III), we trapped $^{171}$Yb⁺ in a second BGA trap (see Refs. 23,24 and references therein for details on $^{171}$Yb⁺). The $F = 0, m_F = 0$ to $F = 1, m_F = 0$ clock transition of $^{171}$Yb⁺ is magnetic field insensitive at zero field and these states serve as our $|0\rangle$ and $|1\rangle$ qubit states, respectively. We trap pairs of qubits at $z = 548 \mu$m with axial frequency 0.6 MHz and radial frequencies 1.7 MHz and 2.1 MHz. Following the work in Refs. 25–27, we span the hyperfine qubit with a pulsed 355 nm Raman laser. The Raman lasers are counter propagating along the surface of the trap with approximately 10 mW in the first beam at a waist of 15 µm and 30 mW in the second beam at a waist of 7 µm.

![Figure 18](image)

Figure 18. (a) Population evolution of the $^{171}$Yb⁺ qubit during the Mølmer-Sørensen gate: $P_{00}$=both ions in $|0\rangle$; $P_{01}$=first ion in $|0\rangle$, second ion in $|1\rangle$; $P_{10}$=first ion in $|1\rangle$, second ion in $|0\rangle$; $P_{11}$=both ions in $|1\rangle$. (b) Parity measurement ($P_{00}+P_{11}-P_{01}-P_{10}$) of the entangled ions at gate time of 50 µs.

Starting in the $|00\rangle$ state, we implement a Mølmer-Sørensen gate 28 on the 1.7 MHz radial mode to entangle the two ions into the state $(|00\rangle - i|11\rangle)/\sqrt{2}$. Figure 18 shows the population evolution during the entan-
gling gate. It also shows the parity signal at a gate time of 50 µs as a function of the phase of a subsequent π/2 pulse on the carrier transition. Following Ref.29, the resulting two qubit entanglement fidelity is 93(2)%.

V. SUMMARY AND CONCLUSIONS

A ball-grid array architecture offers significant improvements in size and scalability for microfabricated ion traps. Trench capacitors fabricated into the trap die replace surface filter capacitors, providing a 30× reduction in trap die area over traps with planar capacitors. Through-substrate vias connect the electrodes to pads on the back side of the trap die, eliminating wirebonds from the trap surface. The trap die is bump-bonded to a separate interposer chip for signal routing to a CPGA carrier, the trap surface. The trap die is bump-bonded to a separate interposer chip for signal routing to a CPGA carrier. Optical access to a trapped ion is improved by the reduced BGA trap chip area and the absence of wirebond obstructions, allowing tighter focusing of laser beams for qubit operations and addressing.

BGA ion trap performance is characterized with 40Ca+ ions. We measure stray axial electric fields, motional mode stability, heating rate with and without ion transport, and dark lifetimes for one and two ions. By all measures, the BGA trap equals or exceeds results from earlier GTRI surface-electrode traps fabricated with aluminum electrodes and standard wirebonding10,18 and the heating rate is competitive with most microfabricated traps from other groups30. We demonstrate focusing of an addressing 729 nm laser beam to a waist of ≈ 8 µm, approaching the separation distance for two co-trapped ions, with minimal power loss due to scattering off trap surfaces. Further improvements in ion addressing could be obtained with cylindrical optics to tighten focus along the trap axis while maintaining beam divergence in the vertical direction relevant to scattering loss. In a second BGA trap, we demonstrate a Mølmer-Sørensen gate with 93% entanglement fidelity, enabled by tight focusing of 355 nm Raman beams onto a pair of 171Yb+ ions.

The BGA architecture extends readily to traps of increasing complexity. BGA techniques could simplify fabrication of intricate junction traps, such as the NIST Racetrack31 and Sandia MUSIQC Circulator32, which feature rings of RF rails encircling isolated islands of control electrodes; in such designs it becomes impossible to route leads to all electrodes on a single metal layer. BGA interposer design is flexible and easily modified for signal routing from carriers other than the standard CPGA presented here. The BGA architecture could be integrated with recently demonstrated in-vacuum electronics18 to produce ion traps with significantly larger numbers of electrodes at manageable physical size.

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Appendix A: Fabrication Details

1. Trap Die Front-side Metallization

The bottom-most metal layer (M1) is a 1.5 µm-thick layer of gold surrounded below by a TiW/Pt adhesion/diffusion barrier and above by a Ti adhesion layer. At the locations of TSVs, M1 is patterned into 50 µm-diameter discs that are separated from the ground plane by 5 µm gaps. The discs are connected to the TSVs below through contacts and to the above metal layer (M2) by vias. The dielectric between the TSVs and M1 is 1.5 µm thick; the dielectric between M1 and M2 is 10 µm thick. Vias in the second dielectric are formed by thermally sloping photoresist and etching the vias in a recipe that transfers the slope into the SiO2.

M2 forms the trap DC and RF electrodes. M2 is 1.5 µm of gold with 30 nm of Ti above and below to ensure good adhesion to the SiO2 dielectric. After M2 has been patterned, CVD SiO2 is deposited over the entire wafer, and a CMP operation is performed to remove most of the topography associated with M2 and the M1-to-M2 vias. After CMP an additional layer of 1.5 µm of TEOS SiO2 is deposited.

The last metal layer (M3) is also 1.5 µm of gold. A via is etched through the 3.5 µm SiO2 prior to 3rd metal deposition. A via plug (also 3.5 µm thick) is used to fill the via and thereby improve the planarity of the 3rd metal surface. There is minimal print-through into M3 of features other than the via plugs. A temporary layer of Ti and Pt protects M3 during the subsequent oxide etch.

2. Interposer Fabrication

The process for making the interposer involves 9 individual steps, summarized below:

1. 1st metal: 1st metal forms a uniform ground plane beneath the signal carrying lines. 1st metal is 1.7 µm of Au, with Ti and Pt adhesion/barrier layers above and below. A blanket layer of 4 µm of SiO2 is deposited above.
2. 2nd metal: 2nd metal, also 1.7 μm of Au surrounded by Ti and Pt, carries electrical signals from the interposer to the trap region. A blanket layer of 6 μm of SiO2 is deposited above.

3. 1st via: The 1st via process etches holes through the SiO2 dielectric down to the metal layer beneath. In cases where there is a 2nd metal feature under the via, the etch stops on 2nd metal. Otherwise the etch continues down to 1st metal (ground).

4. 3rd metal: 3rd metal (1.7 μm Au) carries electrical signals to 2nd metal from the edges of the interposer. A blanket layer of 3 μm of SiO2 is deposited above.

5. 2nd via: 2nd via opens up holes though the 3 μm of SiO2 down to 3rd metal. Holes near the perimeter of the interposer expose 3rd metal pads for wire-bonding to the package. Holes near the center of the interposer expose 3rd metal pads for solder-bonding to the trap die.

6. 4th metal: 4th metal (1.7 μm Au) is primarily a ground plane, with additional metal pads at the locations of 2nd vias to create larger areas for solder connections to the trap die.

7. Bond pads: An additional layer of metal is deposited, with thickness and properties optimized for bonding.

8. Front-side loading slots: Holes for the ion loading slots are DRIE-etched 300-350 μm into the front side of the wafer.

9. Back-side loading slots: Holes for the ion loading slots are DRIE-etched 1000 μm in from the back side of the wafer, meeting the front-side loading slot holes 300 μm from the front surface of the interposer to create a continuous opening.

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