On MOSFET Threshold Voltage Extraction Over
the Full Range of Drain Voltage Based on Gm/ID

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Abstract—A MOSFET threshold voltage extraction method
covering the entire range of drain-to-source voltage, from linear
to saturation modes, is presented. Transconductance-to-current
ratio is obtained from MOSFET transfer characteristics mea-
sured at low to high drain voltage. Based on the charge-based
modeling approach, a near-constant value of threshold voltage
is obtained over the whole range of drain voltage for ideal,
long-channel MOSFETs. The method reveals a distinct increase
of threshold voltage versus drain voltage for halo-implanted
MOSFETs in the low drain voltage range. The method benefits
from moderate inversion operation, where high-field effects, such
as vertical field mobility reduction and series resistances, are
minimal. The present method is applicable over the full range
of drain voltage, is fully analytical, easy to be implemented,
and provides more consistent results when compared to existing
methods.

Index Terms—Halo implant, Long-channel DIBL, MOSFET,
Threshold voltage, Transconductance-to-current ratio.

I. INTRODUCTION

Threshold voltage extraction methods for MOSFETs that
cover the full range of drain voltage are rare, mainly
due to the regional approaches underlying many conven-
tional methods [1]. Moderate inversion in MOSFETs, where
diffusion and drift transport components have comparable
magnitude, covers an important range of current. The recogni-
tion that $G_m/I_D$ has a quite universal behavior over tech-
nology, bias ranges (mostly in saturation), and temperature
[2], [3], enhances the interest in related techniques.

The transconductance-to-current ratio change (cTCR) methods
relate the extremum of $\partial(G_m/I_D)/\partial V_G$ to threshold voltage
in [4], [5], [6] and may be applied from linear to saturation
operation. A drawback of these methods is the increased
noise due to the necessary successive derivations. Methods
relaying directly on transconductance-to-current ratio [7], [8]
emphasize on linear mode operation. The adjusted constant-
current (ACC) [9] and generalized constant-current (GCC)
[10] techniques relate a threshold current criterion directly to
$G_m/I_D$. The ACC method is applicable over the full range
of drain voltage [9]. All the aforementioned methods relate
to $G_m/I_D$ and hence share a sound physical basis. None of
them, to the best of our knowledge, has been demonstrated in
detail over the full range of drain voltage.

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II. MOSFET THRESHOLD VOLTAGE EXTRACTION
METHOD FOR FULL DRAIN VOLTAGE RANGE

The charge-voltage relation in a long-channel MOSFET is
given in [11] as,

$$v_p - v_{d,s} = 2q_{d,s} + \ln(q_{d,s})$$

where $v_{p,g,s,d} = V_{P,G,S,D}/U_T$ are the pinch-off, gate, source
and drain voltages (all referred to local substrate), and thermal
voltage is $U_T = kT/q$. The pinch-off voltage $V_P$ is estimated
as in [9].

$$V_P \approx (V_G - V_T)/n$$

where $V_T$ and $n$ is the threshold voltage and slope factor,
respectively. $q_{g,d}$ are the normalized mobile charge densities
at source and drain sides [9], respectively. Solving for mobile
charges results in,

$$q_{s,d} = (1/2)L_W \left(2e^{v_p-v_{s,d}}\right)$$

where $L_W$ is the Lambert W (product logarithm) function.

An analytical approximation with sufficient accuracy is [14]

$L_W(z) \approx \ln(1+z)\left(1 - \ln(1 + \ln(1 + z))/(2 + \ln(1 + z))\right)$.

Using the definition of threshold voltage in [9], [10] whereas
threshold voltage is defined as the gate voltage for which the
minimum potential in the channel ($v_s$) becomes equal to the
pinch-off voltage $v_P$. Utilizing $v_p = v_s$ in (3) gives,

$$q_s = (1/2)L_W(2) \approx 0.4263$$

$$q_d = (1/2)L_W(2e^{-v_{d,s}})$$

A novel, simple, and fully analytic method of threshold
voltage extraction based on transconductance-to-current ratio
(TCR) is introduced in this work. The latter is obtained from
$I_D - V_G$ measured at different values of $V_{DS}$. The method
is based on the theory of the charge-based model [11], [12].
While formally equivalent to the ACC [9] method, the usage
of the Lambert W function renders the procedure analyti-
cally explicit. The method is among the few with which threshold
voltage may be consistently obtained over the whole range
of drain voltage, from linear mode to saturation. The method
is shown to yield a threshold voltage independent of drain
voltage for ideal long-channel MOSFETs. For halo-doped
MOSFETs, the method reveals a characteristic increase of
threshold voltage at $V_{DS} < 4 \cdot U_T$. The method is particularly
suited for the investigation of DIBL effects including long-
channel DIBL [13].
we obtain $v_{gs} = V_{DS}/U_T$. Using the general charge-based expression for the transconductance-to-current ratio for MOSFETs,

$$\frac{G_m U_T}{I_D} = \frac{g_m}{i_d} = \frac{1}{n \cdot (1 + q_s + q_d)}$$  \hspace{1cm} (5)

where $n$ is the weak inversion slope factor, evaluated from $n = \left[\text{max} \left(\frac{G_m U_T}{I_D}\right)\right]^{-1}$ in weak inversion. Utilizing (4) we obtain $g_m/i_\text{d}$ at threshold,

$$g_m \left|_{v_t} \right. = \frac{1}{n \cdot (1.4263 + \frac{1}{2}L_W (2e^{-v_t})^n)}$$  \hspace{1cm} (6)

Hence (6) provides an explicit, analytical criterion to determine threshold voltage over the full range of $V_{DS}$, that does not require any numerical iterations. In particular, for $v_{ds} = 0$ in linear region (6) gives $(1/2)L_W (2e^0) = 0.4263$, $g_m/i_\text{d} \approx 0.54/n$, while for saturation, $(1/2)L_W (2e^{-\infty}) \approx 0$,

$$g_m \left|_{v_{t, \text{sat}}} \right. \approx \frac{0.7}{n}$$  \hspace{1cm} (7)

Hence, the threshold voltage is determined as the gate voltage at which $G_m U_T/I_D$ corresponds to a certain fraction of its maximum value in weak inversion, depending solely on $V_{DS}$. The extraction takes place in moderate inversion so series resistance and mobility degradation have minimum effect on extracted threshold voltage.

### III. Experiment and Discussion

To validate our method, TCAD simulation and measurements are utilized. A long-channel ($L = 10\mu m$) NMOS device with oxide thickness $T_{ox} = 3.45\text{ nm}$ and uniform substrate doping $N_{sub} = 10^{17}\text{ cm}^{-3}$ was simulated with Silvaco Atlas, at room temperature, using CVT mobility and Shockley-Read-Hall (SRH) recombination models. Two cases without and with pocket/halo implants are considered, where the halo implants are uniformly doped areas ($2 \cdot 10^{18}\text{ cm}^{-3}$) placed below drain and source extensions.

Transconductance-to-current ratio for the whole range of drain voltage, from $V_{DS} = 10mV$ to $1.5V$, measured from a long-channel ($L = 10\mu m$) NMOS transistor of a $110\text{ um}$ CMOS technology is shown in Fig. 1(a). To confirm that the extracted $V_T$ is compatible with the used charge-based approach, $g_m/i_d$ is evaluated from (5) and demonstrated in Fig.1(a). The normalized charges $q_s$ and $q_d$ in (5) are calculated using (3) where $v_p$ is evaluated from (2) using the extracted values of $V_T$ and $n$. The model fits measured characteristics adequately, confirming the consistency of procedure and model. The transconductance-to-current-ratio $n \cdot G_m U_T/I_D$ which corresponds to $V_T$ vs. $V_{DS}$ and its asymptotic behavior in linear and saturation modes according to (7) and (8) is shown in Fig. 1(b). The extracted threshold voltage $V_T$ vs. $V_{DS}$ is shown in Fig. 1(c). The latter also shows results of TCAD simulations. The case without halo implant features an almost invariable threshold voltage [9], within $\pm 0.4mV$. The case with halo implant shows a characteristic increase of $V_T$ at $V_{DS} < 4 \cdot U_T$ when the device is in non-saturation. The same qualitative increase observed in the real device may therefore clearly be attributed to halo implant.

Extraction methods are compared in Fig. 2(a)-(b) for the long-channel TCAD-simulated device with and without halo implant. For the CC method used here, the current criterion to extract $V_{T,CC}$ is $I_{T,\text{sat}} = 0.618 \cdot I_{D} \cdot (W/L)$ with technology current $I_0 = 605nA$ ($621nA$) in halo (non-halo) cases. $I_{spec} = I_{D} \cdot (W/L)$ is the specific current obtained as in [9]. For the GCC method, the threshold criterion $V_{T,GCC}$ is determined as $V_{G[V_T=0]}$, corresponding to an inversion coefficient $IC = I_{D}/I_{spec} = 0.608$ i.e. $n g_m/i_d = 0.7$ [10]. The procedure is repeated for each value of $V_{DS}$. Both CC and GCC methods are implemented for saturation conditions (i.e. $V_{ds} > 4 \cdot U_T$ in moderate inversion). In the cTCR [5] method, $V_{T,\text{cTCR}}$ is the gate voltage corresponding to the peak of $\partial(G_m/I_D)/\partial V_G$. To obtain the needed resolution, we use a polynomial fitting of the data near the peak. The cTCR and this work’s TCR methods provide $V_T$ in the full range of $V_{DS}$. The different behavior of the extracted threshold voltage is immediately apparent. For the non-halo device, $V_{T,\text{cTCR}}$ shows variation when departing from saturation, compared to the almost constant $V_{T,\text{TCR}}$, while the CC and GCC methods in saturation yield practically the same $V_T$ as cTCR and TCR methods (within $2mV$). For the case with halo implants, the
different behavior becomes more apparent due to the nature of each method. A common point to CC, GCC and TCR methods is the same estimation of change in $V_T$ at highest $V_{DS}$ among halo and non-halo cases.

In Fig. 2(c), the data of the long-channel device of Fig. 1 are compared to a short-channel device of the same 110nm CMOS process. The short-channel device shows the same qualitative increase of $V_T$ at low $V_{DS}$, while exhibiting a clear drain-induced barrier lowering (DIBL) at higher $V_{DS}$.

The present method is applicable to a wide range of purposes, from process characterization to extraction of parameters in charge-based compact models, such as EKV [15], ACM [16], or BSIM-bulk [17] models, but may be easily adapted for use in other compact models. The method is based on the $G_m/I_D$ characteristic in moderate inversion, which is universal in many ways among different geometry, device types, temperature, and to some extent even for different types of FETs. A distinct feature is its applicability over the full range of $V_{DS}$ combined with moderate inversion operation, making it highly suitable for the investigation of DIBL and long-channel DIBL [13] effects.

**IV. CONCLUSION**

A novel, fully analytical method for the extraction of threshold voltage in bulk MOSFETs over the full range of drain voltage has been presented. The method is based on the transconductance-to-current ratio $G_m/I_D$ in moderate inversion, and hence benefits from a low impact of high-field effects and series resistance. The charge-based modeling approach provides an explicit criterion for extracting $V_T$ directly from $G_m/I_D$ consistently for all $V_{DS}$. A practically constant value of threshold voltage $V_T$ is obtained in the full range of $V_{DS}$ from linear to saturation modes for ideal, long-channel devices. Halo-implanted devices show a characteristic increase of threshold voltage at low drain voltage, which is attributed to pocket/halo doping. The method is furthermore applicable to investigate DIBL effects.

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