Abstract—It is generally observed that the fraction of live lines in shared last-level caches (SLLC) is very small for chip multiprocessors (CMPs). This can be tackled using promotion-based replacement policies like re-reference interval prediction (RRIP) instead of LRU [3], dead-block predictors [4], or reuse-based cache allocation schemes [5]. In GPU systems, similar LLC issues are alleviated using various cache bypassing techniques. These issues are worsened in heterogeneous CPU-GPU systems because the two processors have different data access patterns and frequencies. GPUs generally work on streaming data, but have many more threads accessing memory as compared to CPUs. As such, most traditional cache replacement and allocation policies prove ineffective due to the higher number of cache accesses in GPU applications, resulting in higher allocation for GPU cache lines, despite their minimal reuse.

In this work, we implement “The Reuse Cache” approach [5] for heterogeneous CPU-GPU systems. The reuse cache is a decoupled tag/data SLLC which is designed to only store the data that is being accessed more than once. This design is based on the observation that most of the cache lines in the LLC are stored but do not get reused before being replaced. We find that the reuse cache achieves within 0.8% of the IPC gains of a statically partitioned LLC, while decreasing the area cost of the LLC by an average of 40%.

I. INTRODUCTION

Due to the end of Dennard Scaling, heterogeneous chip multiprocessors (CMPs) are becoming increasingly more popular as a way to increase energy efficiency while avoiding performance losses to dark silicon. By having multiple types of cores on the same chip, work can be offloaded to cores that are specialized for a task, which has been shown to increase performance over typical, homogeneous CMPs [7].

In a heterogeneous CPU-GPU CMP, the CPU and GPU share both an address space and a last-level cache (LLC). This can lead to issues of cache thrashing and dead blocks in the LLC. Typically, CPU applications have significant amounts of data reuse whereas GPU applications have massively parallel thread blocks that access significant amounts of memory with minimal reuse. This indicates that GPUs often end up overloading the LLC, evicting useful cache lines that the CPU would reuse in the future. This cache thrashing can significantly decrease the performance of the CPU in the system [7].

The reuse cache is a decoupled tag and data cache that only allocates cache blocks that are being referenced more than once. Prior works have implemented the reuse cache design in the last level cache of multi-core CPU [5]. We propose to adopt the reuse cache in a CPU-GPU system. We believe that due to the streaming nature of GPU applications, adopting the reuse cache could limit the amount of the GPU accesses that enter the LLC and reduce the number of dead blocks while significantly decreasing the LLC power and area cost.

Our key contributions are as follows:

• We apply the reuse cache approach to heterogeneous CPU-GPU systems. This approach has been previously applied to homogeneous CMPs, but not for heterogeneous systems.
• We analyze the performance and area impact of this system compared to two other popular caching schemes for shared LLCs in heterogeneous systems.

II. RELATED WORK

Several LLC caching schemes exist for heterogeneous CPU-GPU systems. In this section, we present each and analyze their benefits and drawbacks.

A. Cache Partitioning

In order to protect the CPU’s cache lines from being evicted by the GPU, many have proposed partitioning the LLC into two sections, one for the CPU and one for the GPU [6]. This way, the GPU will only evict the block from its partition, leaving the CPU’s partition unaffected. Therefore, this approach could completely eliminate the cross-core thrashing between CPU and GPU. This can
be done statically by pre-defining the cache partitions, or dynamically by taking into account program and hardware information [1] [2]. However, static partitioning can limit the effective LLC size, and dynamic partitioning requires additional hardware in order to both predict cache usage and adjust cache partitions.

B. Cache Bypassing

Since the nature of GPU applications is mostly streaming without reuse, prior work has proposed bypassing the LLC entirely for GPUs [8]. Even though this approach could remove all cross-core cache thrashing in the LLC, GPU applications that are not streaming-based and do have data reuse will not benefit from this approach.

III. THE REUSE CACHE DESIGN

The reuse cache is designed to prevent dead blocks in the LLC by only allowing data to be placed in the cache if it is accessed more than once. In order to keep track of which lines have been re-referenced, the LLC’s tag array is decoupled from the data array. Each tag array entry contains a tag as well as a pointer to the corresponding data in the data array. The data array would also contain a reverse pointer to the tag array entry to set the tag entry pointer to NULL during data eviction. Figure 1 shows the tag array and the data array entry of the reuse cache.

Figure 2 shows an example of the first access and second access in the reuse cache. During the first LLC miss (Figure 2(a)), after getting the data from the memory, the tag is then looked up in the tag array. Since the tag is not found, it is added to the tag array and the pointer is set to NULL. The fetched data is then sent directly to the private cache without being placed in the LLC. Figure 2(b) shows a second LLC miss on the same address. In this case, the tag is already present in the tag array and the address is considered as being reused. Upon noticing the tag hit, the data that is brought from the memory will then be placed into the data array and the tag pointer will be updated accordingly. Subsequent accesses after this step will be a cache hit.

For LLC eviction, the tag and data arrays are handled separately. During tag eviction, the tag pointer is checked to determine if the corresponding data is present in the data array. If it does, the cache line will also be evicted from the data array. Otherwise, only the tag array’s line is evicted. On the other hand, during data eviction, the reverse pointer in the data array will look for the corresponding tag entry. The tag pointer will then be set to NULL and the data entry will be evicted from the LLC.

IV. EXPERIMENTAL METHODOLOGY

We used the AMD APU model in the gem5 [9] simulator for implementing static partitioning (50:50 cache ratio between CPU-GPU), GPU bypassing, and reuse-cache policies. The system parameters used in gem5 were as follows:

| CPU | Core | Dual-core TimingSimple CPU |
| L1 Cache | Private 4-way, 64B line, 32KB I/D, PseudoLRU |
| L2 Cache | Unified 8-way, 64B line, 256KB, PseudoLRU |
| GPU | Core | 4 compute units (CUs), 64-thread wavefront |
| L1 Cache | 64B line, PseudoLRU, Writethrough Private 4-way, 4KB Data, Shared 8-way, 32KB Instruction (4 CUs per instruction cache) |
| L2 Cache | Unified 8-way, 64B line, 4KB, PseudoLRU, Writeback |
| Shared Components | LLC | 16-way, 64B line, 512KB–4MB, LRU |
| DRAM | 2GB |

**TABLE I** CONFIGURATION FOR THE HETEROGENEOUS SYSTEM EVALUATION

Heterogeneous workloads were prepared using different combinations of CPU/GPU benchmarks shown in ta-
ble II, taking into account their memory access behaviour. The benchmark classifications are determined using a parameter called "reuse-distance", which quantifies how frequently an address is accessed by the program.

| CPU Benchmarks         |
|------------------------|
| Cache-friendly         | Queens, SHA          |
| Cache-sensitive        | Blocked matrix-multiplication |
| Large working set     | BFS                  |

| GPU Benchmarks         |
|------------------------|
| Cache-friendly         | Mini-nbody (gravitational simulation) |
| Cache-sensitive        | Convolution, Floyd Warshall, Recursive Gaussian |
| Streaming              | Histogram            |

**TABLE II**

CPU-GPU BENCHMARK CLASSIFICATION

V. EVALUATION AND RESULTS

In this section, we will compare CPU/GPU IPCs, LLC MPKIs, system data-bus utilization and cache area across various cache sizes and benchmark combinations for the three cache allocation policies.

A. Performance

We start our evaluation by comparing the impact of these cache allocation policies on CPU and GPU performance. We use throughput as our metric, which indicates the sum of IPCs of individual cores. Figure 3 shows the CPU-GPU IPCs across various benchmark combinations.

It can be observed that GPU IPC is always lower for LLC bypassing, except for one workload combination. On the other hand, static partitioning is significantly better (45.6%) than the reuse cache for BFS-Convolution combination and 2% better for Matmul-Recursive Gaussian combinations. For rest of the workloads, the reuse cache achieves mostly the same performance as static-partitioning and better compares to cache bypassing.

For the CPU IPC, bypassing slightly helps in some cases, which can be attributed to the fact that CPU access could consume the entire LLC. On the flip side, static-partitioning and reuse cache still perform within 0.8% of bypassing or better for all workloads.

B. LLC Misses

Figure 4 shows the GPU and CPU MPKI comparison for the reuse cache and all the baselines. For CPU MPKI, both static-partitioning and the reuse cache have a higher MPKI than GPU LLC bypassing, since CPU has lesser effective cache space and thus leads to more misses. For the GPU MPKI, the reuse cache performs reasonably well, reducing GPU misses over bypassing for 3 out of 5 workloads. For the histogram workload, the reuse cache does not reduce the MPKI due to the streaming nature of the workload.

C. LLC Area

This section details the area savings provided by the reuse cache. Cacti 6.5 was used to get area numbers for conventional and reuse cache structures at 32 nm technology node.

| Cache Configuration                          | Area (in mm²) |
|---------------------------------------------|---------------|
| Conventional 1MB (Static/Bypass)            | 2.43          |
| 512KB Data, 1MB Tag Reuse Cache             | 1.33          |
| 512KB Data, 2MB Tag Reuse Cache             | 1.55          |

**TABLE III**

LLC AREA COMPARISON ACROSS SCHEMES

It is evident from table III that the reuse cache provides 45% and 36% reduction in area respectively (for equal and double tag-array sizes) due to halved data-array size. The area numbers include the overhead of adding extra pointers required by tag/data entries in the reuse cache.
D. Data-bus Utilization

Figure 5 shows the comparison of data-bus utilization for the three cache allocation schemes. Since the GPU will bypass the LLC in cache bypassing, the DRAM accesses should also increase. This leads to GPU LLC bypassing having the maximum bus utilization out of the three cache allocation schemes. Static-partitioning has the least data-bus utilisation for most cases since it provides both CPU-GPU with a definite cache space. On the other hand, the reuse cache is able to achieve within 32% data bus utilization for 4 of the 5 workload mixes.

VI. Conclusion

LLC Management is an important problem in today’s heterogeneous processors. The reference stream observed by the shared-LLC (SLLC) from the CPU/GPU exhibits little temporal locality, but instead, it exhibits reuse locality. As a consequence, a high proportion of the SLLC lines is useless because the lines will not be requested again before being evicted, and most hits are expected to come from a small subset of already reused lines. This proportion could be particularly high for the GPU accesses.

In this work, we looked to minimize counterproductive insertions and evictions in the SLLC by implementing a reuse cache. We evaluate our proposal by running heterogeneous CPU-GPU workloads on the gem5 AMD APU model. We use static partitioning and GPU LLC bypassing as our baseline comparison. Our major observations are: (i) Static-partitioning performs best when the GPU application working set fits into LLC and the CPU application is not cache-sensitive (ii) For the reuse cache, a performance of within 0.8% (or better when GPU application is cache-sensitive) was achievable for most cases, providing average 40% reduction in area (iii) A tag-to-data cache ratio of 2:1 (where data-array is half of a conventional cache) is a good starting point for reuse-cache design space exploration (iv) Simple LLC bypassing degrades performance for GPU in most cases, though it could improve CPU IPC.

Static-partitioning hard-partitions the cache, while GPU LLC-bypassing does not provide space to GPU in LLC. We think reuse cache incorporates properties from both, hence could adapt to a wider range of applications.

VII. Future Work

In this paper, we have achieved comparable or slightly better application performance with reuse cache in most cases, at significant area reduction. Further reuse cache performance improvements might be closely linked with data/tag replacement policies and memory-access rate (and thread-awareness) in heterogeneous systems. Potential performance improvement might also be obtained by adding a “Tag-only” coherence state in the reuse cache coherence protocol, and increasing the reuse hysteresis. Reuse cache could be combined with cache compression techniques where we have more tags than data blocks, thereby reducing data-array size further.
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APPENDIX

| Name              | Contribution                                           |
|-------------------|--------------------------------------------------------|
| Tejas Shah        | Static-partitioning implementation, Evaluation and benchmark analysis |
| Bobbi Yogatama    | Reuse cache implementation, GPU LLC bypassing implementation |
| Kyle Roarty       | gem5 setup for running CPU-GPU programs, Benchmark setup |
| Rami Dahman       | Benchmark setup, Evaluation and benchmark analysis |

TABLE IV
INDIVIDUAL CONTRIBUTIONS OF TEAM MEMBERS