A novel transformerless high step-Up DC-DC converter with active switched-inductor and quasi-Z-source network

Jiawei Zhao | Daolian Chen | Jiahui Jiang

Abstract
Conventional dc–dc boost converters have limited boosting capabilities, and the main switching device may suffer relatively high voltage stress and current stress. A novel transformerless dc- dc boost converter is proposed in this paper. The proposed topology, which combines the traditional active switch-inductor and quasi-Z-source network, can increase the voltage gain without limiting the duty cycle or increasing the voltage and current stresses of the power switches. The detailed analysis including working principles, steady-state characteristics, non-ideal element analysis and a comprehensive comparison is also presented in this paper. To verify the proposed converter’s performance, a prototype circuit with 20–30 V input voltage, 200 V output voltage, and 200 W output power is implemented in the laboratory. Experiment results confirm the theoretical analysis and advantages of the proposed converter.

1 | INTRODUCTION
A dc–dc converter with high step-up capability is used for many applications, such as distributed generation resources, hybrid electrical vehicles, battery backup systems for uninterruptible power supplies, and LED lighting systems. Generally, the conventional boost converter appears as a suitable candidate for these applications. However, the power device is subjected to high voltage stress and current stress, which will lead to high losses and serious reverse recovery problems [1]. As a result, its maximum voltage transfer ratio is only about five in practice, rather than infinity in theory.

Many topologies have been proposed to improve the boost capabilities of the dc–dc converters, which can be generalized as the isolated type and non-isolated type. The isolated topologies, such as flyback, forward, push-pull, half-bridge, and full-bridge type, can increase the voltage gain by adjusting the turn ratio of the transformer [2, 3]. However, the switches of these converters may suffer extremely high voltage spikes due to leakage inductance of the transformer. To resolve this problem, a snubber circuit [4] or clamping circuit [5] is often required. However, these techniques are complex with low efficiency or high cost. Moreover, transformer-isolated converters tend to be more expensive because of increasing manufacturing costs.

A transformerless dc–dc converter with a high step-up ability may be more attractive because of the lower cost and higher efficiency, which can be generalized as the coupled-inductor-based type [6, 7] and noncoupled-inductor based type [8–13]. The coupled-inductor converters can achieve high step-up voltage gain and minimize the voltage stress on the power switch. However, compared to other structures, the converter is relatively bulky. Moreover, the problems mentioned in isolated topologies also exist for this type of converter. Many high step-up dc–dc converters without a coupled-inductor have been proposed. The focus of the research studies include the voltage-lift [8], cascade techniques [9], switched-inductor [10, 11], switched-capacitor [11, 12] and impedance-network-based topologies [13–15].

The voltage-lift circuit is first proposed in [8], then by merging the main power switch, the relift circuit and triple-lift circuit with enhanced boost ability are also proposed. However, the voltage stress on the switch is relatively high, and the number of capacitors and semiconductors will increase as the voltage gain increases. A high voltage gain can also be obtained through the two cascaded boost converters. However, an additional power switch is required. The two switches are integrated into one in [9] to reduce circuit complexity and cost, but the drawbacks mentioned for [8] also exist for this converter. Although...
A novel ASL-based dc–dc converter is proposed in this paper. In the proposed structure, quasi-Z-source network (QZSN) and ASL are utilized to improve the overall voltage gain. And the high voltage gain is achieved without increasing the voltage stresses and current stresses of the power switches. Compared to other structures, the proposed structure can provide a higher voltage gain with the same duty ratio and achieve lower device voltage stress and device current stress under the same output condition. What is more, the proposed structure has the capability of adding extra stages to get higher voltage gain. The rest of this paper is constructed as follows. In Section 2, the structure of the proposed converter is proposed, and the circuit operation modes including continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are analysed. In Section 3, the steady-state characteristics including voltage gain, device voltage stress, device current stress, boundary conditions and external characteristics are analysed. In Section 4, the voltage gain and converter efficiency considering non-ideal elements are calculated. In Section 5, the cascaded topology is proposed and analysed. In Section 6, a comprehensive comparison between the proposed and other converters is presented to show the proposed converter’s advantages. In Section 7, the experimental results are provided to verify the theoretical analysis and practicality of the converter. In Section 8, the overall conclusion of this article is presented.

2 | OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

The circuit topology of the proposed converter is shown in Figure 2, which contains one active switch-inductor (L1-S1-L2-S2) circuit and two quasi-Z-source networks (L1-C1-L2-C2-D1 and L3-C3-L4-C4-D2). Switches S1 and S2 are controlled simultaneously by using one control signal. Additionally, the proposed converter comprises an output diode D0, an output capacitor C0, and load R.

The operating principles of CCM and DCM are analysed in this section. In the following analysis, the following assumptions are assumed. (1) All the capacitors are large enough. Thus, the voltage of the capacitors is considered as constant in one switching period. (2) The devices are ideal, and the parasitic elements are neglected. (3) Considering the symmetries of the proposed topologies, the inductors L1 and L2 possess the same level of inductance, the same applies to L11 and L21. The typical waveforms for CCM and DCM are shown in Figure 4.
2.1 CCM operation

State 1 \([t_0-t_1]\): Switches \(S_1\) and \(S_2\) are turned on, all diodes work in off-state. The current flow path is shown in Figure 3(a). \(L_1\) and \(L_2\) are charged by the dc source. \(L_{11}\) is charged by the dc source and \(C_{12}\) via \(C_{11}, L_{21}\) is charged by the dc source and \(C_{22}\) via \(C_{21}\), the output capacitor \(C_o\) provides its energy to load \(R\). According to KVL, the voltages of the inductors can be expressed as

\[
\begin{align*}
    u_{L1} &= U_{in} \\
    u_{L2} &= U_{in} \\
    u_{L11} &= U_{in} + U_{C12} - U_{C11} \\
    u_{L21} &= U_{in} + U_{C22} - U_{C21}
\end{align*}
\]  

(1)

State 2 \([t_1-t_2]\): Switches \(S_1\) and \(S_2\) are turned off, all diodes work in on-state. The current flow path is shown in Figure 3(b). Inductors \(L_1, L_2, L_{11}\) and \(L_{21}\) are series-connected to charge the load and capacitor \(C_o\). \(C_{12}\) and \(C_{22}\) are charged by \(L_1\) and \(L_2\) respectively. According to KVL, the following relationships can be obtained

\[
\begin{align*}
    u_{L1} &= -U_{C12} \\
    u_{L2} &= -U_{C22} \\
    u_{L11} &= -U_{C11} \\
    u_{L21} &= -U_{C21}
\end{align*}
\]  

(2)

\[
\begin{align*}
    U_{C1} &= U_i + U_{C21} + U_{C22} \\
    U_{C2} &= U_i + U_{C11} + U_{C12} \\
    U_o &= U_i + U_{C11} + U_{C12} + U_{C21} + U_{C22}
\end{align*}
\]  

(3)

Additionally, the following equations can be obtained due to the symmetries of the topology.

\[
\begin{align*}
    U_{C11} &= U_{C21} \\
    U_{C12} &= U_{C22}
\end{align*}
\]  

(4)

2.2 DCM operation

State 1 \([t_0-t_1]\): The equivalent circuit is similar to state 1 of the CCM operation. The difference is that the currents of \(L_{11}\) and \(L_{21}\) flow in both directions. During this time interval, \(i_{L1}\) and \(i_{L2}\) first fall from the reverse peak to zero, and then rise from zero to the forward peak.

State 2 \([t_1-t_2]\): The equivalent circuit is similar to state 2 of the CCM operation, but the currents of \(L_{11}\) and \(L_{21}\) still flow in both directions, which is similar to state 1. At the end of state 2, \(i_{L1}(t_2)\) and \(i_{L11}(t_2)\) possess the same amplitude but opposite directions, which can be expressed as

\[
\begin{align*}
    i_{L1} &= -i_{L11} = I_M \\
    i_{L2} &= -i_{L21} = I_M
\end{align*}
\]  

(5)

State 3 \([t_2-t_3]\): During this time interval, all switches and diodes work in off-state. The current flow path is shown in Figure 3(c). The currents of \(L_{11}\) and \(L_{21}\) flow in reverse. \(C_o\) provides its energy to load \(R, L_3\) and \(L_{11}\) freewheel via \(C_{11}\) and \(C_{12}, L_2\) and \(L_{21}\) freewheel via \(C_{21}\) and \(C_{22}\).

3 STEADY-STATE ANALYSIS OF THE PROPOSED CONVERTER

3.1 CCM operation

We assume that \(T_0 = DT_0\) is the time interval of state 1, where \(D\) is the duty ratio, \(T_1 = (1-D)T_0\) is the interval of state 2. By applying the voltage-second balance principle to the inductors, we obtain

\[
\begin{align*}
    U_{C11} &= U_{C21} = U_{C12} = U_{C22} = \frac{D}{1-D}U_{in} \\
    U_o &= \frac{1 + 3D}{1-D}U_{in}
\end{align*}
\]  

(6)

According to KVL and applying the calculated voltage relationships of capacitors, the voltage stress on the power switch (drain to source) and diodes (cathode to anode) can be calculated as

\[
\begin{align*}
    U_{S1} &= U_{S2} = \frac{1}{1-D}U_{in} \\
    U_{D1} &= U_{D2} = \frac{1}{1-D}U_{in} \\
    U_{Do} &= \frac{2}{1-D}U_{in}
\end{align*}
\]  

(7)
The efficiency of the converter is assumed to be 100%. Then, the output current can be expressed by the average input current as

\[ I_o = \frac{1 - D}{1 + 3D} I_{in} \]  

(8)

The average current of the inductors is expressed by \( I_{L1}, I_{L2}, I_{L11} \) and \( I_{L21} \) respectively, the average current of \( D_1, D_2 \) and \( D_o \) is expressed by \( I_{D1}, I_{D2} \) and \( I_{D0} \) respectively, and the average current of switches are expressed by \( I_{S1} \) and \( I_{S2} \) respectively. According to the charging balance of the capacitors, Equations (9) and (10) can be obtained. Besides, Figure 5 shows the average current equivalent circuit of the converter.

\[
\begin{align*}
  I_{L1} &= I_{L2} = \frac{I_{in} + I_o}{2} \\
  I_{L11} &= I_{L21} = I_o \\
  I_{D1} &= I_{D2} = I_o \\
  I_{S1} &= I_{S2} = \frac{I_{in} - I_o}{2} \\
  I_{D0} &= I_o
\end{align*}
\]

(9)

\[
\begin{align*}
  I_{D1} &= I_{D2} = I_o \\
  I_{S1} &= I_{S2} = \frac{I_{in} - I_o}{2} \\
  I_{D0} &= I_o
\end{align*}
\]

(10)

3.2 | DCM operation

We assume that \( T_1 = DT_s \) is the interval of state 1, \( T_2 = D_M T_s \) is the interval of state 2. Then the time corresponding to state 3 is \( T_3 = (1-D-D_M) T_s \). The voltages across the capacitors as well as the output voltage \( U_o \) can be expressed by

\[
\begin{align*}
  U_{C11} &= U_{C12} = U_{C21} = U_{C22} = \frac{D}{D_M} U_{in} \\
  U_o &= \frac{D_M + 4D}{D_M} U_{in}
\end{align*}
\]

(11)
From Equation (11), the voltage gain is expressed as

$$ G = \frac{U_o}{U_{in}} = \frac{D_M + 4D}{D_M} $$

(12)

Assuming $L_1 = L_2 = L_0$, $L_{11} = L_{21} = L$, the average current of the inductors is given by Equation (13). From Figure 4(b), the average currents of the inductors during each switching period are given by Equation (14), according to Equation (12), $D_M$ can be rewritten as Equation (15)

$$ \begin{cases} I_{L,1} = I_{L,2} = \frac{D_M + 2D}{D_M} \times \frac{U_o}{R} \\ I_{L,11} = I_{L,21} = \frac{U_o}{R} \end{cases} $$

(13)

$$ \begin{cases} I_{L,1} = I_{L,2} = \frac{DT_S}{2L_0} U_{in} + I_M \\ I_{L,11} = I_{L,21} = \frac{DT_S}{2L} U_{in} - I_M \end{cases} $$

(14)

$$ D_M = \frac{4D}{G - 1} $$

(15)

From Equations (13)–(15), the duty cycle $D$ can be derived as

$$ D = \frac{(G+3)G}{2} \times \frac{2L_0L}{(L_0 + L) R T_S} $$

(16)

Then, a dimensionless constant $\tau$ is defined as

$$ \tau = \frac{2L_0L}{(L_0 + L) R T_S} $$

(17)

Substitute Equation (17) into Equation (16), the voltage gain is given by

$$ G = \frac{U_o}{U_{in}} = \sqrt{\frac{2D}{\tau} + \frac{9}{4} - \frac{3}{2}} $$

(18)

The curve of the voltage gain is shown in Figure 6. It can be seen the voltage gain in DCM operation will increase as $\tau$ decreases.

### 3.3 Boundary operating condition between CCM and DCM

We assume that the converter works under the boundary of DCM and CCM operation, the voltage gain of DCM operation is equal to that of CCM operation. The boundary dimensionless constant $\tau_B$ can be derived as

$$ \tau_B = \frac{D(1 - D)^2}{2(1 + 3D)} $$

(19)

Figure 7 shows the boundary condition for DCM and CCM operation. If $\tau$ is smaller than $\tau_B$, the proposed converter is operated in DCM operation.

### 3.4 External characteristic of the proposed converter

In order to represent the parameterized converter output current, a dimensionless parameter $\gamma$ is defined as

$$ \gamma = \frac{2L_0L L_o}{(L + L_0) R T_S U_i} $$

(20)

Suppose that the converter is operating under the boundary conditions of CCM and DCM. The following equation can be
According to Equations (13)–(15), the voltage gain in DCM operation can be obtained as

\[ G = \frac{2D}{\gamma} - 3 \]  

(22)

Combine Equations (21) and (22), the external characteristic of the proposed converter is depicted in Figure 8. The proposed converter will be more likely to work in DCM operation when \( D = 0.5 \).

4 | NON-IDEAL ELEMENT ANALYSIS OF THE PROPOSED CONVERTER

The parasitic parameters of all elements are ignored in the above analysis. However, the losses of each component could influence the efficiency and boost ability of the proposed converters. In this section, the effects of non-ideal elements on the proposed converter are analysed. Also, the power loss, efficiency, and nonideal voltage gain expressions are calculated in detail. We assume the equivalent series resistance of the capacitors is \( r_C \), the forward voltage drops of the diodes are \( U_D \), the on-resistance of the switches is \( r_S \), the dc resistance of the inductors is \( r_L \) and \( r_{L0} \). Figure 9 shows the equivalent current loops of the proposed converter in CCM operation.

4.1 | Power loss and efficiency

The power switch’s conduction loss is related to the on-resistance and root-mean-square (RMS) value of the switch current. The current pass through the switch can be expressed by

\[ i_s = \begin{cases} \frac{1}{2}I_{\text{in}} + \frac{3}{2}I_o & 0 \leq t \leq DT_s \\ 0 & DT_s \leq t \leq T_s \end{cases} \]  

(23)

According to Equations (8) and (23), the conduction losses of the switches can be calculated as

\[ P_{on} = \frac{8D_I^2r_s}{(1-D)^2} = \frac{8Dr_s}{(1-D)^2}P_o \]  

(24)

The switching loss can be estimated by linearizing the current and voltage of the switches when they are changing the states [13], as

\[ P_{\text{off}} = \frac{1}{6}fS U_s I_s t_{\text{off}} \]  

(25)

(26)

Where \( U_S \) is the voltage stress on the switch before it is turned on, \( I_S \) is the current through the switch after it is turned on, \( f_s \) is the switching frequency, \( t_{\text{on}} \) is the turn-on delay of the switch. \( t_{\text{off}} \) is the turn-off delay of the switch. Then, using Equations (24)–(26), the total power loss in the main switches can be calculated as follows

\[ P_S = P_o \cdot \left( \frac{8Dr_s}{(1-D)^2} + \frac{2f_s(t_{\text{on}} + t_{\text{off}})D}{3(1+3D)(1-D)} \right) \]  

(27)

The losses of the diodes depend on the magnitude of the current flow and their forward voltage drops. Therefore, the currents of diode \( D_1 \) and diode \( D_2 \) can be expressed as
follows.

\[ i_{D1} = i_{D2} = i_{D0} = \begin{cases} \frac{I_o}{1-D} & 0 \leq t \leq DT_S \\ 0 & DT_S \leq t \leq T_S \end{cases} \] (28)

Substituting Equation (8) into (28), the power loss associated with the forward voltage drop \( U_D \) is

\[ P_{D1} = P_{D2} = P_{D0} = I_o U_D \] (29)

Consequently, the total power loss in the diodes is obtained by

\[ P_D = P_{D0} + P_{D1} + P_{D2} = 3I_o U_D = P_o \times \frac{3U_D}{U_o} \] (30)

The losses of the inductors in the PWM converter are mainly the conduction loss. According to Equation (9), the conduction losses of the inductors are given by

\[ P_{L1} = P_{L2} = \frac{(1 + D)^2}{(1 - D)^2} I_o^2 r_{L,0} \] (31)

\[ P_{L11} = P_{L21} = I_o^2 r_{L,0} \] (32)

Then, the total power loss of the inductors is calculated as

\[ P_L = P_{L1} + P_{L2} + P_{L,3} + P_{L,4} = P_o \times \left( \frac{2(1 + D)^2 r_{L,0} + 2r_L}{(1 - D)^2 R} \right) \] (33)

The capacitors’ power losses depend on the equivalent series resistance of the capacitors and root-mean-square value of the currents. According to the charging balance of the capacitors, the currents passing through the capacitors can be approximated by

\[ i_{C11} = \begin{cases} I_o & 0 \leq t \leq DT_S \\ -\frac{D}{1-D} I_o & DT_S \leq t \leq T_S \end{cases} \] (34)

\[ i_{C12} = i_{C21} = i_{C22} = i_{C0} = \begin{cases} -I_o D & 0 \leq t \leq DT_S \\ -\frac{I_o D}{1-D} & DT_S \leq t \leq T_S \end{cases} \] (35)

According to Equations (34) and (35), the power losses of the capacitors can be obtained as Equation (36), then, the total power loss of the capacitors is calculated as Equation (37)

\[ P_{C11} = P_{C21} = P_{C12} = P_{C22} = P_{C0} = P_o \times \frac{D r_C}{(1 - D) R} \] (36)

\[ P_C = P_o \times \frac{D}{1-D} \times \frac{5r_C}{R} \] (37)

We assume that the input voltage range is 20–30 V, the output power is 200 W, and the output voltage is 200 V. The power loss considering the nominal specifications and selected components (shown in Table 1) is calculated, shown in Figure 10. It can be seen the inductor loss presents the most significant impact on the power loss, followed by the diode loss and switch loss. This analysis proves that the overall efficiency can be improved by optimizing parasitic parameters.

![FIGURE 10 Calculated power loss of the proposed converter](image)

The efficiency related to input voltage and duty cycle is shown in Figure 11, it can be seen that (1) for a constant duty ratio, the efficiency will increase as the input voltage \( U_i \) increases; (2) for a constant input voltage, the efficiency will first increase and then decrease as the duty ratio increases.

| Parameter | \( r_s \) | \( t_{on} \) | \( t_{off} \) | \( U_D \) |
|-----------|------------|-------------|-------------|-------------|
| Value     | 9.1 mΩ    | 30 ns       | 44 ns       | 0.58V-0.63V |

| Parameter | \( r_L \) | \( r_{L,0} \) | \( R \) |
|-----------|----------|--------------|--------|
| Value     | 0.08 Ω   | 0.058 Ω     | 200 Ω |

TABLE 1 Parasitic parameters for calculation
4.2 Non-ideal voltage gain of the proposed converter

The ideal voltage gain of the proposed converter can be expressed as

\[ G = \frac{U_o}{U_{in}} = \frac{1 + 3D}{1 - D} \]  \hspace{1cm} (39)

The non-ideal voltage gain will be decreased due to the limitation of parasitic parameters. But the current transfer function is true for ideal and non-ideal conditions, which can be expressed as

\[ G_I = \frac{I_o}{I_{in}} = \frac{1 - D}{1 + 3D} \]  \hspace{1cm} (40)

Thus, the non-ideal voltage can be calculated as

\[ G_{(nonideal)} = \frac{U_o}{U_{in}} = \frac{I_{in}}{I_o} \eta \]

\[ = \frac{1 + 3D}{1 - D} \times \frac{1}{\lambda + 1} \]  \hspace{1cm} (41)
TABLE 2  Performance index of the proposed converter with $N$ quasi-Z-source networks

| Index                                      | Value                                                                 | Index                                      | Value                                                                 |
|--------------------------------------------|----------------------------------------------------------------------|--------------------------------------------|----------------------------------------------------------------------|
| Voltage gain in CCM                        | $\frac{1 + (N + 1)D}{1 - D}$                                        | Average inductor current $I_{L1}, I_{L2}$  | $\frac{(1 + \frac{N}{2})D}{1 - D}I_o$                                |
| Capacitor voltage $U_{C11}, U_{C21}, \ldots, U_{C_{N1}}$ | $D$                                                                  | Average inductor current $I_{L11}, I_{L21}, \ldots, I_{L_{N1}}$ | $I_o$                                                                |
| Capacitor voltage $U_{C12}, U_{C22}, \ldots, U_{C_{N2}}$ | $\frac{D}{1 + (N + 1)D}U_o$                                         | Current ripple of the inductors $\Delta I_{L11}, \Delta I_{L21}, \ldots, \Delta I_{L_{N1}}$ | $\frac{D(1 - D)T_1U_o}{1 + (N + 1)D}I_o$                                |
| Diode voltage stress $U_{D1}, U_{D2}, \ldots, U_{D_N}$   | $\frac{1}{1 + (N + 1)D}U_o$                                         | Average diode current stress $I_{D1}, I_{D2}, \ldots, I_{D_{N}}$ | $I_o$                                                                |
| Switch voltage stress $U_{S1}, U_{S2}$         | $\frac{1}{1 + (N + 1)D}U_o$                                         | Average switch current stress $I_{S1}, I_{S2}$ | $\frac{D + \frac{N}{2}D}{1 - D}I_o$                                  |

FIGURE 14  Characteristics of the cascaded topology. (a) Voltage gain. (b) Device voltage stress. (c) Inductor current ripple

The voltage gain curve considering the selected components is shown in Figure 12. It can be seen the proposed converter can maintain a high boost capacity when $G < 35$. Also, the measured voltage gain for experiment matches well with the theoretical analysis.

5 | EXTENSION OF THE PROPOSED CONVERTER

The cascaded topology is proposed in this section, which is obtained by cascading the multiple quasi-Z-source networks, as shown in Figure 13. $N$ is an even number to maintain the symmetry of the topology. We assume that the proposed converter is operated in CCM operation. Using the same analysis method in Section 3, some steady-state characteristics can be obtained, which are summarized in Table 2. Since there are 3 diodes, 5 capacitors, 2 switches and 4 inductors in the basic structure, it is expected that there are $N + 1$ diodes, $2N + 1$ capacitors, 2 switches and $N + 2$ inductors in the topology with $N$ switched-capacitor cells.

According to Table 2, the voltage stresses of the capacitors are decreased when increasing the number of quasi-Z-source networks. In addition, the current stresses of the inductance and diodes in the cascade QZSNs are relatively low (equal to the output current $I_o$), which can improve the efficiency and reduce the size.

To give a graphical presentation, Figure 14 is depicted, in which the voltage gain, device voltage stress and current ripple of the inductors are present to illustrate the characteristics of the cascaded topology. It can be seen that the cascaded circuit can achieve higher voltage gain with the same duty ratio, and the voltage stresses of switches and diodes as well as the current ripple of the inductors are reduced under the same output condition.

6 | COMPARISON

This section compares the proposed converter with other existing transformerless high step-up converters. The comparisons are performed on their boost factors, component numbers, voltage stress and current stress on devices shown in Table 3. Besides, graphical comparisons are shown in Figure 15.

Generally speaking, compared with other high step-up dc–dc converters, the proposed converter can provide higher voltage gain with the same duty ratio and maintain lower device voltage stress and device current stress under the same output condition.
TABLE 3 Comparison between the proposed and other transformerless high step-up converters

| Reference | [10] | [14] | [15] | [16] | [21] | [22] | [23] | Proposed |
|-----------|------|------|------|------|------|------|------|----------|
| Voltage gain (G) | \(\frac{1 + D}{1 - D}\) | 1 | \(\frac{2 - 2D}{1 - 3D}\) | \(\frac{1 + 2D}{1 - D}\) | \(\frac{D^2}{(1 - D)^2}\) | \(\frac{3D}{1 - D}\) | \(\frac{3 + D}{1 - D}\) | \(\frac{1 + 2D}{1 - D}\) |
| \(D_{\text{max}}\) | 1 | 0.25 | 0.333 | 1 | 1 | 1 | 1 | 1 |
| Number of switches | 2 | 1 | 1 | 2 | 1 | 1 | 2 | 2 |
| Number of capacitors | 1 | 4 | 4 | 1 | 3 | 4 | 7 | 5 |
| Number of inductors | 2 | 4 | 4 | 4 | 3 | 4 | 1 | 4 |
| Number of diodes | 1 | 7 | 3 | 7 | 5 | 3 | 6 | 3 |
| Maximum diode voltage stress | \(G + 1\) \(U_o\) \(U_o\) | \(\frac{3G - 2}{2G}\) \(U_o\) | \(G + 1\) \(U_o\) \(U_o\) | \(\frac{(\sqrt{G} + 1)^2}{G}\) \(U_o\) | \(G + 3\) \(U_o\) \(U_o\) | \(\frac{1}{G}\) \(U_o\) | \(\sqrt{G}\) \(U_o\) \(U_o\) |
| Switch voltage stress | \(G + 1\) \(2G\) \(V_o\) \(V_o\) | \(\frac{3G - 2}{2G}\) \(V_o\) | \(G + 1\) \(2G\) \(V_o\) \(V_o\) | \(\frac{\sqrt{G} + 1}{G}\) \(V_o\) | \(G + 3\) \(V_o\) \(V_o\) | \(\frac{1}{G}\) \(V_o\) | \(\sqrt{G}\) \(V_o\) \(V_o\) |
| Total diode current stress | \(I_o\) | \((3G + 1)I_o\) | \(2GI_o\) | \((2G^2 + 5G + 5)I_o\) | \(G + 3\) \(I_o\) | \(12I_o\) | \(3I_o\) |
| Total switch current stress | \((G - 1)I_o\) | \((G - 1)I_o\) | \((G - 1)I_o\) | \((G - 1)I_o\) | \(G + \frac{\sqrt{G} + 1}{G}I_o\) | \(3I_o\) | \(2GI_o\) | \((G - 1)I_o\) |
| Total inductor current stress | \((G + 1)I_o\) | \((4GI_o)\) | \((2G + 1)I_o\) | \((G + 1)I_o\) | \((G + \sqrt{G} + 1)I_o\) | \((G + 3)I_o\) | \(I_o\) | \((G + 3)I_o\) |

FIGURE 15 Comparison between the proposed and other high step-up dc–dc converters. (a) Comparison of voltage gain. (b) Comparison of switch voltage stress. (c) Comparison of diode current stress. (d) Comparison of inductor current stress

condition. Although the impedance network based converter proposed in [14] and [15] can achieve high voltage gain at a lower duty ratio. Their duty ratio is limited, and the device voltage stress and device current stress are higher than other structures. Besides, the high voltage gain is achieved as the duty ratio reaches the \(D_{\text{max}}\) boundary. Operating at such a high duty cycle will increase the current ripple and deteriorate the efficiency. As a result, the practical voltage boost capability of these two converters will be affected.

Compared with the buck-boost quadric converter [21], the proposed converter can provide a higher voltage when \(D < 0.81\). Besides, the proposed converter can achieve lower device voltage stress and total device current stress under the same output condition.

The Sepic-based high step-up dc–dc converter [22] can provide a higher voltage gain among the compared structures, and the total diode current stress and total inductor current stress are relatively low. Besides, the proposed structure is capable of achieving a higher voltage gain by adding extra stages. However, the capacitor voltage stress will increase as the number of stages increases. Compared to the Sepic-based high step-up dc–dc converter, the converter proposed in this article has lower capacitor voltage stress, resulting in lower cost and smaller size.

Among the compared structures, the switched-capacitor converter proposed in [23] can provide the same voltage gain with the lowest current and voltage stresses on power switches, and only one magnetic element is employed. However, its voltage gain is difficult to adjust (no less than 3, no more than 4), and one more switch is required. Also, if higher voltage gain is required, the number of stages will increase, resulting in an unexpected increase in the number of devices.
7 | EXPERIMENT VERIFICATIONS

7.1 | Parameter design

Assuming the maximum allowed current ripple of the inductance is $x_L\%$, inductance $L_1$ and $L_2$ can be designed as

$$L_1 = L_2 = \frac{nL_t dt}{di_L} = \frac{U_{in}DT_S}{x_L\%I_L} = \frac{D(1 - D)^2RT_S}{(1 + 3D)(1 + D)x_L\%}$$  \hspace{1cm} (42)

Where $dt = DT_S$ is the time interval when the switch S is turned on, and $di_L = x_L\%I_L$ is the variation of the inductor current during this time interval. Similarly, the inductance $L_{11}$ and $L_{21}$ can be designed as

$$L_{11} = L_{21} = \frac{D(1 - D)RT_S}{(1 + 3D)x_L\%}$$  \hspace{1cm} (43)

If the proposed converter is designed to operate in DCM, the following equation can be obtained.

$$\frac{L_oL}{L_0 + L} \leq \frac{D(1 - D)^2RT_S}{4(1 + 3D)}$$  \hspace{1cm} (44)

Taking the $x_C\%$ peak-to-peak capacitor voltage ripple into consideration, the capacitance $C_o$ can be designed as

$$C_o = \frac{i_C dt}{du_C} = \frac{I_oDT_S}{x_C\%U_o} = \frac{DT_S}{x_C\%R}$$  \hspace{1cm} (45)

Where $dt = DT_S$ is the time interval when the switch S is turned on, and $du_C = x_C\%U_C$ is the voltage ripple of $C_o$. Similarly, other capacitors can be designed as

$$C_{11} = C_{12} = C_{21} = C_{22} = \frac{(1 + 3D)T_S}{x_C\%R}$$  \hspace{1cm} (46)

7.2 | Experiment results

A prototype of the proposed converter in Figure 2 is built to verify the proposed converter’s operation principles and practical boost capacity. The experimental parameters are shown in Table 4. And the principle prototype is shown in Figure 16.

Figure 17 shows some typical experimental waveforms under $U_{in} = 20$ V. The operating duty ratio is 0.7, which is basically in line with the theoretical calculation value ($D \approx 0.692$). In addition, the measured voltage across $C_{11}$ and $C_{21}$ are 44.5 and 46.3 V, respectively. Besides, the switch voltage stress $u_{SS}$ is 65 V. The diode voltage stresses $U_{D1}$ and $U_{D2}$ are 65 V and 130 V, respectively. The average current of the diode $D_o$ is 1.03 A. The average currents of inductors $L_1$ and $L_{11}$ are 5.75 and 1.03 A, respectively. Besides, the experiment results for $U_{in} = 30$ V are shown in Figure 18. The measured device voltage stress and device current stress of the components all match the theoretical analysis. Consequently, the correctness of the theoretical analysis is confirmed.

The experiment results for DCM operation under $D = 0.25$ are shown in Figure 19, the dimensionless constant $\tau$ and the voltage gain G under the selected parameters are calculated as $\tau = 0.011$ and $G = 5.37$. The measured output voltage and voltage gain of the prototype are $U_o = 102$ V and $G = 5.1$, respectively. Besides, it can be seen the inductor current $i_{L1}$ and $i_{L11}$ are equal and opposite in the freewheeling phase. Also, the experiment results for $D = 0.4$ are shown in Figure 20. Considering the inherent loss of the converter, the theoretical analysis is proved to be correct.

It is worth mentioning that the inductor current has a relatively low sinusoidal pulsation at state 3 (freewheeling phase), which is caused by the resonance between the inductors and the junction capacitance of the power semiconductors. And this resonance will not occur in either state 1 or state 2, because it can be suppressed by a complete capacitor loop in these two states. For example, in state 1, diode $D_1$ works in off-state, the voltage across $D_1$ is clamped by $U_{in}$ + $U_{C12}$. In state 2, switch $S_1$ works in off-state, the voltage across $S_1$ is also clamped by $U_{in}$ + $U_{C12}$. While in state 3, although both $D_1$ and $S_1$ work in off-state. There is no complete capacitor loop to clamp the voltage of the junction capacitance. Therefore, resonance will occur at this stage, as shown in Figure 19(b) and Figure 20(b). In Section 2,
since all components’ parasitic element is ignored, the amplitude of the resonance is equal to zero. Thus, the inductor current can be approximated as flat in the freewheeling phase.

The measured efficiency curve of the proposed converter under $U_o=200$ V is shown in Figure 21. It can be seen the efficiency is improved when increasing input voltage. Besides, the voltage gain-efficiency comparison is given in Table 5. Compared with other high step-up dc–dc converters with the same power level. The proposed converter can achieve higher efficiency with the same voltage gain.
TABLE 5 Voltage gain and efficiency comparison between the proposed and other high step-up dc–dc converters

| Parameters for experiment | Voltage gain and efficiency |
|---------------------------|-----------------------------|
| Input voltage $U_{in}$ = 20–40 V | 91.3% for 20 V input voltage, 95.8% for 40 V input voltage, 93.8% for 25 V input voltage, 100 W output power. |
| Output voltage $U_{out} = 200$ V | 200 V output voltage, and 200 W output power. |
| Full-load: $P_o = 200$ W | Switching frequency: $f_s = 50$ kHz |
| Switching frequency: $f_s = 50$ kHz | 89% for 25 V input voltage, 110 V output voltage, and 200 W output power. |

| Reference | [16] | [22] | [24] | Proposed converter |
|-----------|------|------|------|-------------------|
| Voltage gain: $U_{out} = 25$ V | 92% for 25 V input voltage, 200 V output voltage, and 198 W output power. |
| Full-load: $P_o = 200$ W | Switching frequency: $f_s = 50$ kHz |
| Switching frequency: $f_s = 50$ kHz | 94.3% for 20 V input voltage, 200 V output voltage, and 200 W output power. |
| Input voltage $U_{in} = 20–30$ V | 96.2% for 30 V input voltage, 200 V output voltage, and 200 W output power. |

8. CONCLUSION

This paper has proposed a novel transformerless high voltage gain dc–dc converter. By utilizing the active switched-inductor converter and quasi-Z-source network, the higher voltage gain is achieved without increasing the voltage stress on power switches and output diode.

Circuit operation principles, steady-state analysis and non-ideal elements analysis are presented. It was seen that the working mode of the proposed converter is similar to that of cuk dc–dc converter. The discontinuous conduction mode refers to the diodes $D_1$ and $D_2$ which are turned off in state 3, rather than a discontinuous current of the inductor.

The cascaded topology was proposed in Section 5. Some desirable features exist in the cascaded topology, such as higher voltage gain, lower device voltage stress and lower current ripple of the inductors. A comparison considering the proposed and other structures was also provided. Considering the results, the superiority compared to other converters is confirmed.

Finally, experimental results were given to verify the characteristics of the converter and theoretical analysis. Considering the approved advantages, such as high voltage gain, high efficiency, and low device voltage stress and current stress, it could be a suitable choice for uninterruptible power supply systems, LED lighting systems, fuel cells, and electric vehicles, where high voltage gain is often required.

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