Optimization and implementation of a surface-electrode ion trap junction

Chi Zhang, Karan K Mehta and Jonathan P Home
Institute for Quantum Electronics, ETH Zürich, Otto-Stern-Weg 1, 8093 Zürich, Switzerland
E-mail: zhangc@phys.ethz.ch and jhome@phys.ethz.ch
January 2022

Abstract. We describe the design of a surface-electrode ion trap junction, which is a key element for large-scale ion trap arrays. A bi-objective optimization method is used for designing the electrodes, which maintains the total pseudo-potential curvature while minimizing the axial pseudo-potential gradient along the ion transport path. To facilitate the laser beam delivery for parallel operations in multiple trap zones, we implemented integrated optics on each arm of this X-junction trap. The layout of the trap chip for commercial foundry fabrication is presented. This work suggests routes to improving ion trap junction performance in scalable implementations. Together with integrated optical addressing, this contributes to modular trapped-ion quantum computing in interconnected 2-dimensional arrays.

Keywords: quantum computing, scalable ion traps, quantum CCD architecture, integrated optics

1. Introduction

Trapped ions are a leading platform for quantum computation. All the elementary building blocks for a quantum computer have been realized in these systems with high quality, including efficient and robust state preparation and readout [1], high-fidelity universal quantum gates [2, 3] and long qubit memory times [4, 5]. This has allowed the demonstration of small-scale computation tasks [6, 7, 8], as well as elements of fault-tolerant control [9, 10] and quantum error correction [11, 12], which establish reliable primitives for scaling.

To build a trapped-ion quantum computer capable of outperforming its classical counterpart in practically useful applications, a much larger number of ions are required [13]. Scaling up the number of ions in a single linear trap faces several challenges, such as difficulty in individual ion addressing due to the reduced inter-ion spacing [14], slowing down of multi-qubit gates [15], and crowding of motional modes [16] that can reduce the fidelity of quantum logic operations due to the thermal occupation
Optimization and implementation of a surface-electrode ion trap junction

of spectator modes [16, 17] or cross-Kerr coupling between modes [18]. These challenges necessitate interconnected ion-trap modules, each hosting a relatively small number of ions, to maintain the low error rates when scaling up.

One way of interconnecting elementary trapped-ion logic units is via photonic links [19, 20, 21], which is likely to be a necessary step for establishing a truly large-scale trapped-ion quantum computer. The quantum charge-coupled device (QCCD) architecture [22] provides an intermediate level of trap interconnection that is promising for controlling > 100 trapped-ion qubits, where the interconnection among elementary logic units is realized by ion shuttling. Basic quantum error correction and quantum algorithms can be realized on QCCD nodes, and photonics links could then be used to mediate communication between several modules [23, 24].

Small-scale qubit control based on the QCCD architecture have been demonstrated on linear traps with up to 20 ions [12, 25, 26, 27]. In the largest such demonstrations, swap operations were used to change the order of the ion chain and bring two arbitrary ions into the interaction zone [12]. In a larger system, such a 1-dimensional QCCD architecture demands a large number of swap operations to interact two arbitrary ions, especially when there are intermediate ion crystals between them. For applications with more irregular communication patterns, a 2-dimensional grid of ion traps interconnected by junctions is likely to provide significant performance benefits [15].

Junction traps have been demonstrated, for instance transportation with 0.05 to 0.1 quanta of average motional excitation per junction traverse has been realized using a 3-dimensional trap fabricated from a stack of laser-machined alumina wafers [28, 29]. More advanced laser machining technologies [30] have been used to implement a 3-dimensional wafer trap with double junctions [31]. However, the complexities in assembling these 3-dimensional wafer traps hamper their scalable reproduction. By contrast, lithographic methods allow asymmetric Surface-Electrode (SE) traps [32], where all trap electrodes are patterned on a single plane, to leverage advanced and scalable semiconductor manufacturing technologies [27, 33, 34]. Several SE junction traps have been designed and fabricated [34, 35, 36], but by far the best reported performance in junction transportation is 37 to 150 quanta of motional excitation per junction traverse [37]. This is much higher than the ∼ 0.1 quanta level achieved in the 3-dimensional trap [29] and limits the realization of QCCD architecture based on SE junction traps, pointing to the need for further research in this area.

In the direction perpendicular to the trap surface, SE traps lack the mirror or rotation symmetry compared to their 3-dimensional counterparts. This naturally reduces the trap depth [32] and induces anharmonicity at the ion position [38], imposing more challenges in ion transport. Despite these challenges, ion transport with sub-quantum excitation has been realized on the linear section of the SE junction trap [37] or linear SE traps [27]. This suggests the sub-optimal junction transport on SE traps is limited by the junction design, rather than the fundamental trap symmetry.

Early SE junction designs mainly emphasized the minimization of the pseudo-potential barrier [34, 35, 36], an inevitable feature near the junction center for a radio
Optimization and implementation of a surface-electrode ion trap junction

Consequently, the total pseudo-potential curvature is also reduced near the junction center. This enforces a reduction of the secular frequencies or the lowering of the ion height from the initially optimized transport path [36], and makes the trap operations more susceptible to stray electric fields [35, 36]. In the designs presented here, we decided to follow an alternative approach, placing more weights on maintaining sufficient pseudo-potential curvature during the optimization of the RF electrodes close to the junction. In this paper, we describe the design process for this trap, considering also the use of integrated optics on each arm of the X-junction trap to facilitate laser beam delivery, a feature which will be of increasing importance as the number of trapping zones increases. The designs have been recently fabricated in a commercial photonic foundry.

The rest of this paper is organized as follows. Section 2 presents the design principle of the RF electrodes, the optimization procedures, and the verification of the design. Section 3 describes the design of the control electrodes. In Section 4, we present the integrated optics implemented on the junction traps. The full trap chip layout is presented in section 5. In section 6, we conclude with an outlook for experiments with such junction traps and other technologies that can potentially benefit the future iterations.

2. RF electrodes of junction trap

Since the quasi-static trapping potential can typically be flexibly adjusted during the experiment, whereas the spatial RF potential is fixed by the electrode geometry for a single non-adjustable RF drive, in the design process of the junction trap we mainly focused on the RF electrodes. Once this design stage is complete, we then focus our attention on optimizing the patterning of the control electrodes, to verify that the desired total trapping potential can be created with static voltages feasible for typical Digital-Analog Converters (DACs) used in experiments today [39, 40].

2.1. Design principle

To achieve zero electric field everywhere along two intersecting ion transport paths that are confining, a hexapole is the lowest electric multipole term allowed at the intersection [41]. Unfortunately, an ion at the center of a pure hexapole potential has zero harmonic motional frequency [42]. If a junction trap creates non-zero RF quadrupole confinement at the intersection, there is inevitably non-vanishing RF field along any ion path in vicinity of the intersection. Due to the broken axial translational symmetry near the intersection, this non-vanishing RF field is inhomogeneous along the trap axes, giving rise to the pseudo-potential barrier [28], with the pseudo-potential given as [43]

\[ \phi_{PP} = \frac{Q}{4m\Omega_{RF}^2} |E_{RF}|^2 \] (1)
for an ion of mass $m$ and charge $Q$ within an RF field $\vec{E}_{RF}$ of angular frequency $\Omega_{RF}$. For several reasons, it is beneficial to reduce the height of the pseudo-potential barrier. A high $\phi_{PP}$ causes a large amplitude of the driven motion of the ion (typically referred to as micromotion), which could break down the pseudo-potential approximation [44]. The gradient of $\phi_{PP}$ associated with the pseudo-potential barrier can cause heating of the secular motional modes when noise on the RF potential is present [28, 36, 45]. Due to the mass dependence of $\phi_{PP}$, the pseudo-potential barrier may also cause segregation of ions of different species when transporting a mixed-species crystal across the junction [45].

Despite the pseudo-potential barrier, an RF quadrupole trap has advantages over higher-order traps in offering a higher overall curvature and intrinsic trap depth [32]. Since the pseudo-potential barrier has been demonstrated not to be a fundamental limit of high-quality ion transport across junction [28, 29], we have taken the approach of designing an RF quadrupole trap.

The pseudo-potential curvature is one important factor often overlooked in junction designs. The total quasi-static potential can be written as the superposition of the pseudo-potential $\phi_{PP}$ and the quasi-static potential $\phi_{st}$ from the control electrodes

$$\phi_{total}(\vec{r}) = \phi_{PP}(\vec{r}) + \phi_{st}(\vec{r}).$$

Because $\phi_{st}$ satisfies the Laplace equation, the Laplacian of $\phi_{total}$ follows

$$\nabla^2 \phi_{total}(\vec{r}) = \nabla^2 \phi_{PP}(\vec{r}),$$

which suggests that the overall positive curvature for confining the ions in three dimensions is created solely by the pseudo-potential. The quasi-static potential $\phi_{st}$ can redistribute the total pseudo-potential curvature among the three directions, but does not affect the net confinement of the trap. If the pseudo-potential confinement is sacrificed in the minimization of the pseudo-potential barrier, the secular frequencies must be reduced close to the junction center. The ions will thus be more susceptible to the drift of stray field [35] and is likely to experience higher static motional heating due to electric noise [46].

In the numerical optimization of the junction RF electrodes, we therefore seek for a balanced performance in the pseudo-potential barrier height and the total confinement. Our numerical optimization is based on the SurfacePattern software package [47, 48], which solves the electrostatic potential of planar electrodes assuming

(i) that there is no gap between electrodes;
(ii) that the entire plane is covered by conducting electrodes.

As will be seen in section 2.4, the positions of pseudo-potential minima obtained with SurfacePattern model agrees to within 5% with the Finite Element Method (FEM) model of the trap, and the worst-case discrepancy in pseudo-potential is about 20% around the junction center. These discrepancies are well understood to be due to the 5 µm gaps between the trap electrodes in our fabrication technology. We chose to use the SurfacePattern model at the initial stage of the design process, because its analytical expressions of the electric potentials allow for faster evaluations and iterations of the
design. The more precise FEM model is used to verify the optimized RF electrode geometry.

### 2.2. Parameterization of electrode geometry

To establish a parametric description of the electrode geometry, we first took the control point approach similar to [35, 36, 45, 49], where the electrode boundaries are defined by straight line segments connecting neighbouring control points. We noticed two limitations with this approach: (1) Sharp corners were formed at the control points, which will likely create high RF field emission that reduces the breakdown voltage of the trap [50], although these structures with high spatial frequency $k_s$ will not significantly affect the potential landscape at the ion position $r \gg (2\pi)/k_s$, as their contributions exponentially decrease as $\exp(-k_s r)$ [32]. (2) To avoid creating self-intersecting boundaries, the allowed range for each control point had to be chosen with care, which made it difficult to ensure the obtained geometry is close to a global optimum in the full parameter space.

A parameterization based on spline functions [45] solves these problems. Our optimized geometry using the spline parameterization is shown in figure 1. The inner and outer boundaries of the RF electrode are respectively described by a B-spline function of cubic order. Each spline function is defined by 5 control points, with reflection symmetry about the diagonal line $y = x$ in figure 1. Hence only the 3 independent control points are shown for each spline. The coordinates of these control points and their independent variables are listed in table 1. During the numerical optimization, we sample each spline function with 21 points evenly distributed in the spline parameter space (green points in figure 1), and define the RF electrode as a polygon by connecting the neighbouring sample points with a straight line segment.

| Point | Coordinate | Independent variable |
|-------|------------|----------------------|
| $I_1$ | $(d_{in}, d_{in})$ | $d_{in}$ |
| $I_2$ | $(x_{i2}, y_{i2})$ | $x_{i2}$, $y_{i2}$ |
| $I_3$ | $(w_g/2, y_{i3})$ | $y_{i3}$ |
| $O_1$ | $(d_{out}, d_{out})$ | $d_{out}$ |
| $O_2$ | $(x_{o2}, y_{o2})$ | $x_{o2}$, $y_{o2}$ |
| $O_3$ | $(w_g/2 + w_{RF}, y_{o3})$ | $y_{o3}$ |

We chose the target ion height to be $h = 50 \mu m$. Using the analytical expressions for the trapping potential assuming gapless, infinitely extended surface electrodes [51], we optimized the geometry of RF electrodes on the linear sections for maximal pseudo-potential curvature at fixed height $h$. The resulting width ($w_{RF}$) and separation ($w_g$) of the RF electrodes are listed in table 2, which agree with [45] to within 99.5% with
Figure 1. Spline function parameterization of the X-junction. The colored areas indicate the RF electrode. The rest of the surface is modeled to be RF grounded. The independent control points of the inner (outer) spline are indicated with red (blue) dots. The 21 sample points of each spline are indicated in green. The independent variables of the control points are listed in table 1. The origin of the coordinate system is set at the center of the junction. z axis is defined upwards perpendicular to the trap surface.

the slight discrepancy due to numerical truncation errors in the intermediate calculation steps.

Table 2. Optimal RF geometry on the linear arm for maximal pseudo-potential confinement at fixed ion height $h$.

| Expression          | Value for $h = 50\, \mu m$ |
|---------------------|-------------------------------|
| $w_g$               | $0.83h$                       | 41.5 |
| $w_{RF}$            | $4h^2 - w_g^2 / (2w_g) \approx 1.99h$ | 99.5 |

2.3. Numerical optimization

For the parameterized junction RF geometry, we performed a bi-objective optimization using the Nelder-Mead algorithm. The cost function is evaluated along the horizontal trap axis in figure 1 denoted by $x$, at the target trap height $h$. One objective is to minimize the variance of the pseudo-potential confinement along the arm

$$f_1 = \text{Var}\left(\nabla^2 \phi_{PP}(\vec{r})\right). \quad (4)$$

The second objective is to minimize the axial gradient of the pseudo-potential

$$f_2 = \int_0^{x_{\text{max}}} \left| \frac{\partial \phi_{PP}(x, 0, h)}{\partial x} \right| \, dx, \quad (5)$$

which can cause heating of the axial motional mode in the presence of RF noise. This second objective also serves as a proxy for reducing the pseudo-potential barrier along
the trap axis, but is more efficient in evaluation, which saves the need to find the peak of the pseudo-potential barrier first. Similar to [45], we approximated (5) as a summation over 101 evaluation points evenly distributed along the trap axis with a spacing of \( \Delta x = 0.1h = 5 \mu m \), from the junction center \( x = 0 \) to \( x_{\text{max}} = 10h = 500 \mu m \). We used these evaluation points to calculate the variance of the pseudo-potential confinement in (4) as well.

In the numerical optimization, we used dimensionless length normalized with \( h \), and a dimensionless pseudo-potential defined as [45]

\[
\phi'_{\text{PP}} = \frac{4m\Omega^2_{\text{RF}}h^2}{Q^2V^2_{\text{RF}}} \varphi_{\text{PP}} = |\nabla \Theta_{\text{RF}}|^2,
\]

(6)

where \( \Theta_{\text{RF}} \) is the basis function for the RF electrodes [52] that solely depends on their geometry. The overall cost function was a weighted sum of the two contributions

\[
f_{\text{cost}} = w_1f_1 + w_2f_2 = w_1 \text{Var}(\nabla^2 \phi'_{\text{PP}}(x, 0, h)) + w_2 \sum_{i=0}^{100} \left| \frac{\partial \phi'_{\text{PP}}(x_i, 0, h)}{\partial x} \right| \Delta x,
\]

(7)

with the weights \( w_1 \) and \( w_2 \). The final junction geometry shown in figure 1 was optimized for balanced weights \( w_1 = w_2 \).

To reduce the chance of getting trapped in local minima of the parameter space, we ran the same numerical optimization with 16 different random seeds, which determine the starting points in the parameter space, and selected the outcome with the lowest cost as the final result. Qualitatively, we also verified that other seeds resulted in geometries similar to the chosen one, indicating a better chance that our chosen solution approaches the global optimum. The values of the independent variables defined in table 1 for the final geometry are listed in table 3.

| Variable | Expression | Value for \( h = 50 \mu m \) (\( \mu m \)) |
|----------|------------|--------------------------------------------|
| \( d_{\text{in}} \) | 0.07460h | 3.73 |
| \( x_{i2} \) | 0.29428h | 14.71 |
| \( y_{i2} \) | 0.54857h | 27.43 |
| \( y_{i3} \) | 2.46382h | 123.19 |
| \( d_{\text{out}} \) | 1.03774h | 51.89 |
| \( x_{o2} \) | 1.78611h | 89.31 |
| \( y_{o2} \) | 2.43434h | 121.72 |
| \( y_{o3} \) | 4.98629h | 249.32 |

Table 3. Specification of the independent variables in table 1, for the final junction geometry put into fabrication as shown in figure 1.
2.4. Verification of the final RF geometry

To verify the RF geometry in figure 1 and table 3, we performed an FEM simulation‡ of its RF field, taking into account of the extra 5 µm gaps between electrodes imposed by the fabrication process. In the FEM simulation, we kept the RF electrodes the same as the SurfacePattern model described in last section, and subtracted the width of the gaps from the RF-grounded electrodes. For instance, in the linear regions, the width of the middle control electrode $w_g$ is reduced from 41.5 µm (table 2) to 31.5 µm (in future trap designs, a better approach would be to subtract half the gap width from both neighboring electrodes, as discussed in the appendix of [51].) In what follows, the pseudo-potentials are calculated for $^{40}$Ca$^+$ with 40 V peak RF voltage at $\Omega_{RF} = 2\pi \times 40$ MHz applied to the RF electrodes.

2.4.1. Transport path with minimal pseudo-potential Figure 2(a) shows the transport path in which the ion is always placed at the corresponding pseudo-potential minimum for each axial position. Figure 2(b) and figure 2(c) show the corresponding pseudo-potential and the pseudo-potential confinement along this transport path. In the linear region, the FEM model predicts lower heights of the pseudo-potential minima by about 2.7 µm and stronger pseudo-potential confinements than the SurfacePattern model. These discrepancies are due to the 5 µm gaps between the electrodes, which are only present in the FEM simulation. We confirmed this with an FEM simulation of a simpler linear trap with the same RF geometry as in table 2. When the gaps between electrodes are reduced to 1 µm, the FEM model agrees with the SurfacePattern model to within 0.7% in the height of pseudo-potential minima, and within 0.1% in the pseudo-potential confinement evaluated at 50 µm above the trap surface. Close to the junction center, the discrepancy between the two models in figure 2(a) becomes larger. This is likely due to the stronger contribution from the gaps, as the spacing between the RF electrodes is narrower than in the linear region whereas the gap is fixed at 5 µm. The small slope $dz/dx$ in the linear region of figure 2(a) is due to both the junction structure around $x = 0$ and the termination of the RF electrodes at $x = 750$ µm.

Approaching the junction center (35 µm $\leq x \leq 100$ µm), lowering the ion height can reduce the pseudo-potential, as shown in figure 2(b), where the pseudo-potential at the constant height of 50 µm is drawn in dashed line for easier comparison. Close to the junction center, the ion has to be lifted above the target trap height $h$ in order to achieve the minimal pseudo-potential.

The minimal pseudo-potential confinement along this transport path is 0.2 meV/µm$^2$, as shown in figure 2(c). If the anti-confinement of a 1.5 MHz axial static trapping potential is equally distributed to the two radial modes, this confinement allows for 2.29 MHz radial modes. Therefore, this SE junction trap is fully confining and provides sufficient confinement to maintain a 1.5 MHz axial frequency, even when one opts for the transport path with minimal pseudo-potential. Other transport strategies

‡ Using Comsol Multiphysics 5.5
that are more favorable for the overall confinement are presented in the next sections.

For a better understanding of the pseudo-potential profile in figure 2(b), we plot the
direction of the RF field in the symmetric plane $y = 0$ in figure 3. The background color
indicates the pseudo-potential. Close to the junction center ($0 < x \leq 63 \mu m$), the RF
field has an $x$-component towards the island of RF ground at the junction center (see
figure 1). On the other hand, far enough from the junction center, the RF field has to
point outwards. This is because the electric potential created by a certain electrode at
the ion position is proportional to the solid angle seen from the ion [32, 53], and the area
of the RF electrode is larger at the junction center than at the end of the linear arm. In
figure 3, the cross-over between the inward and outward RF fields happens at $x = 63 \mu m$.
Hence there is a pseudo-potential null at $x = 63 \mu m$ in figure 2(b) splitting the pseudo-
potential barrier into two peaks. The RF field has the largest horizontal component in
the region $25 \mu m < x < 40 \mu m$, corresponding to the pseudo-potential barrier shown in
figure 2(b). Closer to the junction center, the horizontal RF component reduces due to
the cancellation from the opposite arm at $x < 0$. At the junction center, the horizontal
RF field is zero due to symmetry, so there exists a height with zero pseudo-potential.

To estimate the influence of the pseudo-potential barrier on ion transport, we
evaluated the ion motion at $(x, y, z) = (30 \mu m, 0, 53.7 \mu m)$, corresponding to the peak

Figure 2. The transport path with minimal pseudo-potential (a), the corresponding
pseudo-potential (b), and the pseudo-potential confinement (c) along this path. The
red traces are for the SurfacePattern model, on which the numerical optimization is
based. The blue traces are evaluated with the FEM simulation. The dashed line in (b)
shows the pseudo-potential at constant height $z = 50 \mu m$ (FEM model) for comparison,
the same as figure 4(a).
Optimization and implementation of a surface-electrode ion trap junction

10

Figure 3. The direction of RF field (black streamlines) evaluated in the symmetric plane y = 0 of the junction trap. Because of the mirror symmetry, the y-component of the RF is zero in this plane, so only the x and z components are plotted. The background color indicates the pseudo-potential.

of pseudo-potential barrier shown in figure 2(b). After finding the principal axes of the RF potential by diagonalizing its Hessian matrix, we found that the RF field is primarily along the direction of the least pseudo-potential curvature (0.26 mV/µm²), with a projection of 3.2 × 10⁴ V/m. The projections of the RF field along the orthogonal directions are smaller by more than one order of magnitude. We therefore focused on the 1-dimensional excess micromotion (EMM) [54] driven by the non-vanishing RF field along this direction.

Keeping the electric potential up to quadrupole terms, the ion motion driven by the non-vanishing RF field is described by the inhomogeneous Mathieu equation [54]. If a static potential is applied to create ω₀ = 2π × 1.5 MHz trap frequency along the direction under investigation, the pseudo-potential curvature along this direction is negligible compared to the curvature of the static one, similar to the axial mode in a standard linear trap. We can thus simplify the 1-dimensional ion motion in this direction as a driven harmonic oscillator

\[ m \frac{d^2r}{dt^2} + m \omega_0^2 r = Q E_{RF} \cos(\Omega_{RF} t), \]

whose particular integral can be obtained using the technique of variation of parameters [55, 56] as

\[ r(t) = \frac{Q E_{RF}}{m(\omega_0^2 - \Omega_{RF}^2)} \cos(\Omega_{RF} t) \approx -\frac{Q E_{RF}}{m \Omega_{RF}} \cos(\Omega_{RF} t) = -\sqrt{\frac{4Q \phi_{PP}}{m \Omega_{RF}^2}} \cos(\Omega_{RF} t), \]

which predicts 1.2 µm amplitude of the EMM. For comparison, the EMM amplitude at the peak of pseudo-potential barrier in [29] is estimated to be 6.9 µm.

2.4.2. Transport with fixed height If the ion is transported at a fixed height of 50 µm above the trap surface, the pseudo-potential and pseudo-potential confinement are shown in figure 4 as functions of the axial displacements from the junction center x = 0. The ion experiences larger total pseudo-potential confinement than in the path

§ The relevant parameters are: ⁹Be⁺ ion, 0.3 eV pseudo-potential, and 83 MHz RF drive.
in figure 2(a), at the price of higher pseudo-potential barrier. The minimal pseudo-potential confinement along this ion path (0.3 meV/µm²) allows for a 1.5 MHz axial mode and two 2.84 MHz radial modes, assuming the confinement is equally distributed between the two radial modes.

![Figure 4](image-url) **Figure 4.** The pseudo-potential (a) and the total pseudo-potential confinement (b) evaluated at a fixed height of 50 µm as a function of axial displacement from the junction center x = 0.

The discrepancy in pseudo-potentials in figure 4(a) between the two models is mainly a consequence of the different positions of the pseudo-potential minima shown in figure 2(a). The evaluation height, z = 50 µm, is closer to the pseudo-potential minima of the SurfacePattern model, in particular towards the end of the junction arms. In figure 4(b), the pseudo-potential confinements predicted by the two models show a good agreement when evaluated at the same height.

For comparison, in an optimization where the cost term $f_1$ for pseudo-potential confinement is made to be dominant by setting $w_1 = 10w_2$ in (7), the minimal pseudo-potential confinement along the constant-height transport path for the optimization output (0.67 meV/µm²) is more than two times higher than in figure 4(b), but the maximal $\phi_{PP}$ increases to 58 meV. On the other hand, the geometry optimized mainly for the minimal pseudo-potential gradient (for $w_2 = 10w_1$) leads to a lower pseudo-potential barrier (3.8 meV) than in figure 4(a) whereas the minimal pseudo-potential confinement decreases to 0.1 meV/µm².

### 2.4.3. Transport path with constant confinement

Another strategy of ion transport is to maintain a constant pseudo-potential confinement along the path. The transport paths shown in figure 5(a) maintain a pseudo-potential confinement of 1.0 meV/µm². Approaching the junction center, the ion height has reduced by $\sim 7$ µm to maintain the same confinement, which is qualitatively the same observation as in [36]. Figure 5(b) shows the pseudo-potential along this path. The ion will experience a higher pseudo-
potential (33.9 meV), which corresponds to 2.28 µm EMM amplitude estimated using (9).

Because of the larger deviation from the pseudo-potential minima in figure 5(a) than in the previous two transport paths, the validity of the pseudo-potential approximation becomes one concern. Within the pseudo-potential approximation, the electric potentials are expanded up to 2nd order, but when the ion is far enough from the saddle point of the electric potentials, the higher order anharmonic terms could have non-negligible influence on the ion motion. To verify the ion confinement along the transport path in figure 5 and to better estimate the amplitude of the ion’s driven motion, we numerically calculated the ion trajectory at the position of largest pseudo-potential \((x, y, z) = (15 \mu m, 0, 43.52 \mu m)\) without making the pseudo-potential approximation.

First of all, we diagonalized the Hessian of the pseudo-potential at this position to find its principal axes, which are listed in table 4 together with the corresponding eigenvalues and the projections of the RF field along these directions. We then optimized the static voltages applied to the control electrodes (whose layout will be introduced in section 3) to redistribute the confinement, which results in \((6.51, 4.03, 1.5)\) MHz secular frequencies along the three principal axes in table 4. To keep the time-averaged ion position at the specified position, the static voltages were used to compensate the ponderomotive force due to the gradient of the pseudo-potential. The largest magnitude of the static voltage involved is 2.48 V.

With this set of static voltages, we numerically solved the equation of ion motion

\[
m \ddot{\mathbf{r}} = Q \left[ \mathbf{E}_{st}(\mathbf{r}) + \mathbf{E}_{RF}(\mathbf{r}) \cos(\Omega_{RF}t) \right]
\]  

using the analytical expressions for \(\mathbf{E}_{st}\) and \(\mathbf{E}_{RF}\) from SurfacePattern. The \(x\) and \(z\) components of the solution are shown in figure 6. Due to the strong RF field, the 40 MHz EMM is the dominant motional component. The modulation of the EMM
Table 4. Principal axes of the pseudo-potential Hessian, the corresponding eigenvalues, the secular frequencies, and the RF electric field at $\vec{r} = (15\,\mu\text{m}, 0, 43.52\,\mu\text{m})$.

| Principal axis $(x, y, z)$ | Eigenvalue (meV/µm$^2$) | Secular frequency (MHz) | Electric field (V/m) |
|---------------------------|--------------------------|-------------------------|----------------------|
| $(0.195, 0, 0.981)$      | 0.991                    | 7.79                    | 53218                |
| $(0, 1, 0)$               | 0.104                    | 2.53                    | 188                  |
| $(-0.981, 0, 0.195)$     | −0.099                   | —                       | −28627               |

envelop is due to the secular motion. The EMM amplitude obtained from the numerical integration is 2.34µm, 3% larger than the estimation from (9). Hence, the pseudo-potential approximation remains a good approximation in this extreme case.

Figure 6. Numerical simulation of the ion trajectory in the presence of a strong RF field close to junction center. The static voltages are designed to keep the time-averaged ion position at $\vec{r} = (15\,\mu\text{m}, 0, 43.52\,\mu\text{m})$, where the pseudo-potential is largest in figure 5.

2.5. Comparison with a simple junction

To benchmark the optimized junction geometry, we can compare it with a simple junction constructed by crossing two linear traps in right angle, as shown in figure 7(a). The RF geometry of the linear traps are the same as listed in table 2. The pseudo-potential and the total pseudo-potential confinement evaluated at fixed height of 50µm are plotted in figure 7(b-c). The maximal pseudo-potential in figure 7(b) is one order of magnitude higher than the optimized geometry as in figure 4.

To keep a minimal pseudo-potential along the transport path, the height of the ion has to be lifted up to 84µm (figure 8(a)), which reduces the maximal pseudo-potential along the transport path by one order of magnitude (figure 8(b)), to roughly the same level as the optimized geometry in figure 2(b). However, as the ion is lifted higher above the trap surface, the minimal available pseudo-potential confinement along this
Optimization and implementation of a surface-electrode ion trap junction

Figure 7. (a) An X-junction constructed by simply crossing two linear traps, each with 99.5 µm wide RF electrodes spaced by 41.5 µm, same as in table 2. The pseudo-potential (b) and the total pseudo-potential confinement (c) are evaluated using SurfacePattern at a fixed height of 50 µm. The same curves as in figure 4 for the optimized junction geometry are shown in dashed lines for comparison.

path drops to $0.07\,\text{meV/µm}^2$, which is about 30% that of the optimized geometry in figure 2(c). If one motional mode is kept at 1.5 MHz, such a total confinement only allows for 1.06 MHz frequency on the other two modes.

2.6. Final layout of RF electrode

In the final layout of the RF electrode (see figure 10 for the overall layout also including the control electrodes), we chose three arms of the junction trap to be 750 µm long, and elongated one arm to 2.7 mm. The long arm allows for a working zone far from the junction to reduce the residual axial RF field from the pseudo-potential barrier. The wirebonding pad for the RF electrodes is placed at the end of the long arm, and thus it is also preferable to make this arm long to minimize the extra RF field from the wirebonds in the working regions. The height of pseudo-potential minima and the corresponding pseudo-potential are plotted in figure 9. The pseudo-potential of $1.8 \times 10^{-4} \,\text{meV}$ at $-1000 \,\mu\text{m}$ would give rise to 5.2 nm EMM.

Although it is technically feasible to make separate electrical connections to the four RF electrodes using vias and other metal layers underneath the trap surface, we decided to interconnect them using the top metal layer on this trap chip. This ensures low impedance of the connections and minimizes the phase difference of the RF fields from different RF electrodes. The second available metal layer in our fabrication technology (see section 5) is RF grounded and shields the silicon substrate of the trap chip from the RF tracks, reducing the RF loss [49] and potential laser-induced photo-effects due to the photoionization of atoms in the substrate by the UV lasers involved in the experiments [33].
The two long RF electrodes are connected by the same wire bonding pads. To connect the other two RF electrodes with minimal variation in RF impedance, we made arc structures with the same width as the RF electrodes (see figure 10), which keeps the width of this interconnection piece constant. As can be seen from figure 9, the arc interconnection structures also flatten the pseudo-potential profile close to the termination of the RF electrodes (orange points).

3. Control electrodes

After finalizing the geometry of the RF electrodes, we patterned the control electrodes for creating the quasi-static trapping potential and for transporting the ion according to the shape of the RF electrodes.

To keep a fixed 5 µm gap from the non-trivial outline of the RF electrodes, we first sampled the spline functions defining the RF electrodes at 100 points, with about 1 µm spacing between each two. For each line segment connecting the neighbouring sample points, we calculated its transverse direction in the trap plane, along which we shifted the line segment by 5 µm. Finally, we interpolated the shifted sample points to obtain the outline of the control electrodes.
Figure 9. Height of the pseudo-potential minima (a) and the corresponding pseudo-potential (b) for the final RF electrode geometry, evaluated in the symmetry plane of each arm with SurfacePattern. The negative displacements are along the long arm. The wirebonding pad at $-2700 \mu m$ is responsible for the rise of pseudo-potential on that end. There is an 8 nm discontinuity at $-1665 \mu m$ in (a) due to numerical imprecision, which causes the discontinuity in (b). The positive displacements are along the 750 $\mu m$ short arms. The orange points are for the two arms with the arc interconnection structure, which flattens the pseudo-potential profile compared to the straight termination.

3.1. Segmented middle electrodes

Leveraging the flexibility in electrical connections using the second metal layer (see section 5), we segmented the middle electrodes to realize the 5-wire geometry of SE traps [32, 57], which has two advantages over the segmentation of the outer two wires. The number of control electrodes is roughly halved for achieving the same level of flexibility in ion transport along the trap axes. Furthermore, since the middle segments are closer to the ions, they can create stronger curvatures at the ion position with a fixed voltage [32]. To create 1 MHz axial frequency, the outer segmentation method would require $\sim 20$ times higher voltages than the middle segmentation for our RF geometry.

The segmented middle electrodes are shown in blue in figure 10. When operating the trap, smaller segments are preferable as they allow for fine adjustments of the trapping potential. However, the number of control electrodes is limited by the space for their wirebonding pads on the perimeter of the trap chip, which imposes a lower bound to the minimal length of each control electrodes. Due to this limitation, we divided the middle control electrodes into segments of 75 $\mu m$ length in the linear regions. For more flexibility in the junction transport, we reduced the length of the 4 control electrodes adjacent to the center to 40 $\mu m$. The control electrode at the center is a 30 $\mu m$ wide square, whose corners are removed due to the extrusion of the RF electrodes. The width of the middle control electrodes in the linear region is 31.5 $\mu m$, whereas in vicinity of the junction center they have variable widths following the outline of the RF electrodes.
There are overall 48 segmented middle electrodes, with 9 on each short arm, 20 on the long arm, and 1 at the junction center.

As a verification of the segmented middle electrodes, we calculated the voltages required to create 1.5 MHz axial frequency along the minimal pseudo-potential transport path in figure 9(a). All the required voltages are within −2 V to 5 V and should be straightforwardly obtainable from typical DACs.

3.2. Outer control electrodes

Doppler cooling of the ion motion requires the wave vector of the laser beam to have non-zero projections along the modes to be cooled, and that the trap frequencies are non-degenerate [58]. In the linear region of the trap, the two radial modes are parallel and perpendicular to the trap surface respectively when the trapping potential possesses mirror symmetry about the trap axis. Hence, for a Doppler cooling laser beam running parallel to the trap surface, the principal axes of the trapping potential have to be rotated to cool the out-of-plane mode. To rotate the principal axes of the trapping
potential, differential voltages need to be applied onto the outer electrodes to break the mirror symmetry about the trap axis. Furthermore, to simultaneously keep the potential minimum on the trap axis, the outer electrodes must be segmented transversely (see figure 10).

The junction structure automatically tilts the principal axes of the pseudo-potential and lifts the degeneracy of motional modes in its vicinity (see e.g. table 4). At the junction center, the central-most control electrodes can tilt the principal axes more effectively than the outer ones. Hence, the geometry of the transverse segmentation of the outer electrodes is most important for the operation at the linear regions of the trap. Therefore, to optimize this transverse segmentation, we simulated a simple linear trap with the RF geometry shown in table 2.

From the simulation, we found that lifting the degeneracy of the radial modes is more demanding than merely rotating the principal axes. Thus we fixed the rotation angle to 20° and used the attainable maximal radial mode splitting to benchmark different segmentation ratios of the outer electrodes. For a fixed voltage range from $-10 \text{ V}$ to $10 \text{ V}$, we adjusted the segmentation ratio such that the thinner (light green in figure 10) and the wider (dark green in figure 10) outer electrodes reach their limiting values roughly at the same time when creating the maximal mode frequency splitting. In the final geometry shown in figure 10, the thinner outer electrodes are $49.75 \mu m$ wide at the linear region, whereas the wider ones are $580 \mu m$ wide. We can intuitively understand such a ratio from the fact that the thinner electrodes are closer to the ion and thus are relatively more influential, whereas the segments far from the trap axis need a larger area to make a comparable impact on the ion. Using $\pm 10 \text{ V}$, such a geometry can create about $700 \text{ kHz}$ splitting for degenerate radial modes at $6.06 \text{ MHz}$, resulting in two radial modes at $6.24 \text{ MHz}$ and $5.54 \text{ MHz}$ with the radial principal axes rotated to $20°$ and $70°$ to the $z$-axis.

It is worth noting that this final geometry of outer electrodes is obtained heuristically from simulation. The analytical expressions for the electric field from SE in [51] can potentially be used to find the theoretically optimal geometry.

### 3.3. Transport waveform

To verify that junction transport can be realized within our feasible voltage range, we optimized a transport waveform, as shown in figure 11. To obtain a smooth waveform, the voltage changes between subsequent steps are penalized, which was not taken into account in the voltage checks at individual axial positions performed in section 3.1.

The waveform generation is based on the Python library CVXPY with the MOSEK solver backend. We formulated the optimization problem using the electric fields and curvatures at the ion positions. We discretized the transport path into a set of $N$ positions $\{r_i\}, i \in [1, N]$, at which a sequence of static trapping wells are described. The trap model based on SurfacePattern was used for the waveform generation. For
Figure 11. A voltage waveform of junction transport (a) and the resulting secular frequencies (b). The full waveform transports the ion from the linear region of the upper arm \((y = 500 \mu m)\) to the long arm on the other side of the junction \((y = -95 \mu m)\). For clarity, only part of the waveform and only the voltages exceeding ±2 V are shown. The voltages applied to arm L are identical to those on arm R.

Each control electrode \(j\), we exported to the optimizer its electric field
\[
\{E_x^{(j)}(\vec{r}_i), E_y^{(j)}(\vec{r}_i), E_z^{(j)}(\vec{r}_i)\}
\]
and the 6 elements of its Hessian
\[
\{H_{xx}^{(j)}(\vec{r}_i), H_{xy}^{(j)}(\vec{r}_i), H_{xz}^{(j)}(\vec{r}_i), H_{yy}^{(j)}(\vec{r}_i), H_{yz}^{(j)}(\vec{r}_i), H_{zz}^{(j)}(\vec{r}_i)\}
\]
evaluated at \(\vec{r}_i\) for 1V applied voltage. The pseudo-potential gradients \(\vec{E}^{(PP)}\) and curvatures \(\mathcal{H}^{(PP)}\) from the RF electrodes were exported analogously. The optimizer then seeks for the control voltages at each step \(i\) that minimize the cost function under the constraints specified below. The same optimization procedure can be applied to the FEM trap model as well, after pre-processing the FEM simulation to construct a similar look-up table of fields and curvatures at \(\{\vec{r}_i\}\).

The constraints used in the optimization of the waveform shown in figure 11 are:

(i) Zero time-averaged field at each \(\vec{r}_i\)
\[
\vec{E}^{(PP)}(\vec{r}_i) + \sum_j E^{(j)}(\vec{r}_i) = \vec{0}.
\]

(ii) One principal axis of the trapping potential is exactly along the trap axis, which is \(y\) in this example
\[
H_{xy}^{(PP)}(\vec{r}_i) + \sum_j H_{xy}^{(j)}(\vec{r}_i) = 0,
\]
\[
H_{yz}^{(PP)}(\vec{r}_i) + \sum_j H_{yz}^{(j)}(\vec{r}_i) = 0.
\]
(iii) The axial Hessian element equals the certain value $H_{\text{axial}}(\vec{r}_i)$ that results in the specified axial frequency, 1.5 MHz in this example

$$H_{yy}^{(PP)}(\vec{r}_i) + \sum_j H_{yy}^{(ij)}(\vec{r}_i) = H_{\text{axial}}(\vec{r}_i).$$

(iv) Radial curvatures are above a certain limit, which is chosen to be $3H_{\text{axial}}(\vec{r}_i)$ here

$$H_{xx}^{(PP)}(\vec{r}_i) + \sum_j H_{xx}^{(ij)}(\vec{r}_i) \geq 3H_{\text{axial}}(\vec{r}_i),$$

$$H_{zz}^{(PP)}(\vec{r}_i) + \sum_j H_{zz}^{(ij)}(\vec{r}_i) \geq 3H_{\text{axial}}(\vec{r}_i).$$

The cost function is formed as the weighted sum of the following contributions:

(i) The 1st and 2nd order time derivatives of the control voltages. This cost term ensures a smooth voltage waveform, reducing its high-frequency components that can cause motional excitation and impose higher technical requirements for the waveform generator hardware. In this preliminary waveform example in figure 11, time is implicitly represented by the axial position of the ion.

(ii) The distance from $\vec{r}_i$ to the active control electrodes. This cost term penalizes the use of distant control electrodes, since in the QCCD architecture parallel operations are necessary and thus the transport of the communication ion should minimally affect the potential well for the static memory ions.

(iii) The residual electric field at $\vec{r}_i$. Although already specified by the constraint condition (11), the outcome from numerical optimization can still have a residual electric field at the desired trapping position. This term penalizes such residual field to ensure the ion is transported along the desired path.

For the waveform shown in figure 11, only the segmented middle electrodes were used to generate the potential wells. Involving the outer electrodes in the transport results in smaller voltages fulfilling the same constraints. We excluded them because for parallel operations these outer electrodes are responsible for maintaining the tilt of radial axes in the linear regions. In future traps, these outer electrodes can be segmented along the axial direction to provide more flexible controls in parallel operations. Radial mode tilting and splitting are not imposed in the preliminary waveform shown in figure 11, but can be achieved independently using the redundant degrees of freedom from the outer electrodes.

Figure 11 confirms that the control electrode layout in figure 10 allows for a junction transport with a constant 1.5 MHz axial frequency and at least 2.75 MHz radial frequency. The required voltage range $-4.5 \text{ V}$ to $7.0 \text{ V}$ can be conveniently obtained from typical DACs. We therefore took such a layout as the final design for the trap fabrication.
4. Optics integrated into the junction trap

Conventionally, the laser beams for controlling the trapped ions are delivered in free space. To avoid hitting the trap chip, for SE traps the free-space laser beams have to propagate parallel to the trap surface. Such a geometrical constraint imposes challenges in parallel operations on a SE junction trap, as the laser beams addressing one arm have to avoid the ions on the other arms. For a single X-junction, it is still in principle possible to arrange the laser beams for parallel operation. For instance, every laser beam can be aligned perpendicular to the arm it is addressing. However, in a larger-scale trap array connected by multiple junctions, such a strategy becomes invalid since there will be junction arms parallel to each other. The density of usable trap modules will eventually be limited by the available optical access.

Nanophotonics devices integrated on the trap chip offer a promising approach for scalable laser beam delivery [59, 60, 61, 62]. The laser light can be routed through waveguides inside the trap chip, and focused to the ions by grating couplers [63]. Since the laser beams are emitted from the ion trap, they can be directed to individual trap zones without affecting the parallel operation in the other zones. Aside from the parallelizability, the integrated optics also improves the stability of light delivery since the optics are rigidly fixed to the ion trap, and the efficiency of laser power usage due to the tighter beam foci [60].

On our junction traps, we used Si₃N₄ integrated optics to deliver the 729 nm coherent manipulation light and the 854 nm and 866 nm repumping light for the Ca⁺ qubits. These junction traps are fabricated on the same wafer as our experimentally tested linear traps [60]. A thin Si₃N₄ layer (25 nm thick) 3.5 µm below the ground plane extends to the edge of the trap chip. The low-confinement optical mode it supports matches the mode of a standard single-mode fiber for optical input. A vertical adiabatic taper couples light from the 25 nm Si₃N₄ layer to a 170 nm thick Si₃N₄ core separated by 50 nm from the thinner one, which creates a higher confinement of the optical mode for waveguide routing [60, 64]. After the light is routed to the trap zone, a lateral taper expands the mode size, and a diffractive grating patterned by electron beam lithography emits the light to the ions above the trap chip [60]. The thickness of silicon dioxide below the gratings is chosen such that the reflection from the silicon substrate constructively interferes with the upwards-radiated light, to enhance the out-coupling efficiency of the gratings [63].

By equipping trap sites with the corresponding integrated optics, elementary units of different functionalities in quantum information processing can be realized. Further interconnecting them with junctions enables a modular approach to large-scale trapped-ion computing. We have made two versions of junction traps featuring integrated optics for different tasks. On each arm of one junction trap, we placed the same two-ion interaction optics as experimentally tested in [60], as shown in figure 12(a). The gratings are designed to focus light to 50 µm above the trap surface. The upper grating coupler is for 729 nm light, which focuses the beam to 3.7 µm Gaussian beam waist (1/e² radius).
perpendicular to the trap axis. Along the trap axis, the beam waist is relaxed to 6.5 \( \mu \text{m} \) for illuminating two ions and driving two-qubit gates using the axial motional mode. The lower coupler delivers the 854 nm and 866 nm light for laser cooling and resetting the qubit states. The designed beam waist is about 20 \( \mu \text{m} \), and hence this grating coupler takes a smaller area than the 729 nm one. The openings on the metal layers are symmetric for the two couplers, such that their perturbation to the axial RF field is canceled at the center of the interaction zone where the beams are focused.

The other junction trap features different optics on its long arm and short arms. On its long arm we implemented a five-ion quantum register, shown in figure 12(b). The five couplers for 729 nm light are designed to focus the beams to 2 \( \mu \text{m} \) beam waist along the trap axis, with the beam foci matching the positions of five ions in an harmonic potential with an axial center-of-mass mode frequency of 422 kHz [64]. The same coupler for 854 nm and 866 nm light as in figure 12(a) resides between the two 729 nm couplers on the left side. The openings on the metal layers have mirror symmetry about the trap axis. The RF electrodes are deformed to compensate the perturbation of pseudo-potential from the openings on them for light transmission [64]. On each of the three short arms, we placed one single-ion addressing optics for 729 nm light and one coupler for repumper light the same as figure 12(b), as shown in figure 12(c).

![Figure 12](image)

**Figure 12.** The grating couplers implemented on the junction traps. The Si\(_3\)N\(_4\) waveguides and the lateral tapers for expanding the optical modes are shown in red. The electron beam lithography region used for the gratings are indicated in blue. The openings on the metal layers for light transmission are symmetric in each interaction zone. (a) shows a 2-qubit interaction zone with the upper coupler for 729 nm and the lower for 854 nm and 866 nm light, implemented on 4 arms of one junction trap. The other junction trap features a 5-ion interaction zone (b) on its long arm and the same 729 nm individual ion addressing optics (c) on its three short arms.

5. **Trap chip layout and fabrication**

We fabricated the integrated-optics traps at a commercial photonics foundry (LioniX International) using Si\(_3\)N\(_4\) technology [65]. The layer stackup of this technology has previously been reported in [60, 64]. The trap electrodes are patterned on 300 nm thick top gold layer which lies on SiO\(_2\). A platinum layer forms an RF ground plane 3 \( \mu \text{m} \)
below the gold to isolate the Si$_3$N$_4$ layers and silicon substrate from the RF tracks. Here we also used this platinum layer to route the electric connections to the segmented middle electrodes. The Si$_3$N$_4$ layers for the integrated optics are 3.5 µm below the platinum plane.

The layout of the trap chip is created in the CADENCE VIRTUOSO™ layout suite. To create electrodes of irregular shapes, we sampled their outlines to line segments, exported the coordinates of the sample points to text files, and used a script to connect them into polygons in CADENCE VIRTUOSO. The full chip layout is shown in figure 13.

![Figure 13.](image.jpg)

Figure 13. The layout of the junction trap chip. The left edge is dedicated to the fiber array for optical input. The waveguides (red) route the light to the interaction zones on each junction arm. Wirebonding pads for electrical input are patterned on the other three edges, allowing for free-space beam access along ±45° on each arm and one extra axial beam along the long arm of the junction. The trap electrodes and the wirebonding pads are patterned on the top gold layer (outlined in gold). Except for the RF drive, the electric connections from the wirebonding pads to the corresponding electrodes are routed on the platinum layer (shaded). The rest of the platinum layer is made a ground plane. Vias (green) connect the gold and the platinum layers.

The trap chip is 5 mm wide and approximately 8.2 mm long. The trap electrodes are patterned on the top gold layer, outlined in gold. The left edge of the chip is dedicated to the fiber arrays for optical input. The Si$_3$N$_4$ waveguides (red) in-couple the optical inputs from single-mode fibers attached to the edge and route them to the interaction zones located on the four junction arms.

The wirebonding pads (200 µm-by-120 µm) for electric inputs are located on the other three edges of the chip. They are patterned such that ±45° free-space beam accesses are allowed on each junction arm, and one axial beam is allowed along the long arm.

The RF electrodes directly extend to their wirebonding pad on the gold layer. The electric connections from the rest of the electrodes to their wirebonding pads are routed
Optimization and implementation of a surface-electrode ion trap junction

on the platinum layer (shaded grey). The platinum tracks are 10µm wide, limited by the density of connections in proximity of junction center. The clearance between the platinum tracks and the neighbouring ground plane is 5µm. To minimize the exposure of the RF electrodes to the underlying silicon substrate from such 5µm gaps, we tried to reduce the overlap between the platinum tracks and the RF electrodes while routing. To reduce the crosstalk between neighbouring tracks, we arranged at least 30µm wide ground plane between neighbouring tracks. The tracks were routed manually, and the rest of the platinum ground plane was created using the Boolean logics of CADENCE VIRTUOSO.

Vias (green) form the electric connection between the gold and the platinum layers. Square vias 30µm wide connect the gold wirebonding pads to the platinum tracks. We reduced the width of vias to 5µm on the trap electrodes, since they indent the top gold surface and can potentially cause trapping potentials to deviate from the simulations.

All blank space on the top gold layer is covered by a ground plane. The platinum ground plane is removed over the region where the vertical tapering of the Si₃N₄ waveguides take place. This is to reduce the insertion loss of input light before the optical modes are adiabatically coupled to the tightly confining thick Si₃N₄ waveguides. The two ground planes are electrically connected by five small vias 5µm wide, as well as a bigger one 30µm wide on the corresponding wirebonding pad. The wirebonding pad is used to connect the ground planes to the ground reference of the experiment, or alternatively to a voltage source for applying a bias voltage.

Figure 14 shows an optical micrograph of the finished junction trap featuring the integrated optics in figure 12(c).

![Figure 14. Optical micrograph of the fabricated junction trap. The vias are visible due to the indentation of the top gold surface they cause.](image-url)
6. Summary and Outlook

We presented the design of a SE junction trap based on a numerical optimization of the trap electrode shape, parameterized using B-spline functions. Equal weights were used in the bi-objective cost function to minimize the pseudo-potential curvature variation and the axial pseudo-potential gradient along the ion transportation path at a fixed ion height. The optimization was based on SurfacePattern, and the final result was verified with an FEM simulation. To facilitate parallel operation in multiple trap zones, we implemented integrated optics on each arm of this X-junction. The traps are fabricated in a commercial foundry. The linear traps fabricated on the same wafers and the optics integrated on them have been tested experimentally in other work, serving as the basic proof of principle for the photonic foundry processes.

In an actual junction transport experiment, modifications of the transport paths and waveforms are likely needed relative to those presented in this article. The DAC update rate [29, 37] and slew rate [40] can be key aspects in low-excitation junction transport, which we have not considered in the preliminary waveform yet, and would be closely related to the exact experimental parameters.

Depending on the exact experimental limitations, the weights in the bi-objective optimization of the RF electrodes can be adjusted in the future iterations of junction design, and other objectives may be introduced as well.

To operate the current version of junction traps, the ultra-violet lasers for the cooling, detection and photo-ionization of $^{40}$Ca$^+$ still rely on the conventional free-space delivery. This is due to the high material absorption of Si$_3$N$_4$ in the low 400 nm wavelength range [66]. Aluminium oxide [66, 67] is a CMOS-compatible material with higher bandgap energies, and is a potential choice for the full optical integration of the lasers controlling $^{40}$Ca$^+$ qubits in future iterations.

In case the requirement for free-space laser access is relaxed by the full optical integration, the available space for wirebonding pads roughly doubles. This allows a larger number of control electrodes, which can provide finer control of the trapping potentials and more flexibility in parallel operations. For instance, the outer electrodes could be segmented along the trap axis, so that the radial tilt of different zones on the same arm can be adjusted independently.

Through-Substrate Vias (TSVs) [68] provide a promising approach to further increased density of control electrodes and a larger-scale ion-trap array connected by multiple junctions. Unlike the wirebonding pads that have to be located on the perimeter of the trap chip, the TSVs can make use of the surface area on the backside of the trap chip to form higher number of electrical connections. The implementation of TSV on silicon photonics chips is successfully demonstrated in [69], where the TSVs are created by masked etching and copper filling after the fabrication of the integrated photonics and before the formation of metal layers. Therefore, such a process should, in principle, be made compatible to the Si$_3$N$_4$ technology utilized in our integrated-optics ion traps.
7. Acknowledgements

We thank Jason Amini and Curtis Volin for helpful discussions about the design principle of the junction trap, and Frank Gürkaynak at ETH for support with the CAD software. We acknowledge funding from the Swiss National Science Foundation (grant no. 200020 165555), the National Centre of Competence in Research for Quantum Science and Technology (QSIT), ETH Zürich.

References

[1] T. P. Harty, D. T. C. Allcock, C. J. Ballance, L. Guidoni, H. A. Janacek, N. M. Linke, D. N. Stacey, and D. M. Lucas. High-fidelity preparation, gates, memory, and readout of a trapped-ion quantum bit. Phys. Rev. Lett., 113:220501, 2014.

[2] Craig R. Clark, Holly N. Tinkey, Brian C. Sawryr, Adam M. Meier, Karl A. Burkhardt, Christopher M. Seck, Christopher M. Shappert, Nicholas D. Guise, Curtis E. Volin, Spencer D. Fallek, Harley T. Hayden, Wade G. Rellergert, and Kenton R. Brown. High-fidelity bell-state preparation with \(^{40}\text{Ca}^+\) optical qubits. Phys. Rev. Lett., 127:130505, 2021.

[3] R. Srinivas, S. C. Burd, H. M. Knaack, R. T. Sutherland, A. Kwiatkowski, S. Glancy, E. Knill, D. J. Wineland, D. Leibfried, A. C. Wilson, D. T. C. Allcock, and D. H. Slichter. High-fidelity laser-free universal control of trapped ion qubits. Nature, 597(7875):209–213, 2021.

[4] Ye Wang, Mark Um, Junhua Zhang, Shuoming An, Ming Lyu, Jing-Ning Zhang, L.-M. Duan, Dahyun Yum, and Kihwan Kim. Single-qubit quantum memory exceeding ten-minute coherence time. Nature Photonics, 11(10):646–650, 2017.

[5] M. A. Sepiol, A. C. Hughes, J. E. Tarlton, D. P. Nadlinger, T. G. Ballance, C. J. Ballance, T. P. Harty, A. M. Steane, J. F. Goodwin, and D. M. Lucas. Probing qubit memory errors at the part-per-million level. Phys. Rev. Lett., 123:110503, 2019.

[6] S. Debath, N. M. Linke, C. Figgatt, K. A. Landsman, K. Wright, and C. Monroe. Demonstration of a small programmable quantum computer with atomic qubits. Nature, 536(7614):63–66, 2016.

[7] Thomas Monz, Daniel Nigg, Martinez A. Esteban, Matthias F. Brandl, Philipp Schindler, Richard Rines, Shannon X. Wang, Isaac L. Chuang, and Rainer Blatt. Realization of a scalable shor algorithm. Science, 351(6277):1068–1070, March 2016.

[8] Yunseong Nam, Jwo-Sy Chen, Neal C. Pisenti, Kenneth Wright, Conor Delaney, Dmitri Maslov, Kenneth R. Brown, Stuart Allen, Jason M. Amini, Joel Apisdorf, Kristin M. Beck, Aleksy Blinov, Vandyver Chaplin, Mika Chmielewski, Coleman Collins, Shantanu Debath, Kai M. Hudek, Andrew M. Ducore, Matthew Keesan, Sarah M. Kreckemeier, Jonathan Mizrahi, Phil Solomon, Mike Williams, Jaime David Wong-Campos, David Moehring, Christopher Monroe, and Jungsang Kim. Ground-state energy estimation of the water molecule on a trapped-ion quantum computer. npj Quantum Information, 6(1):33, 2020.

[9] Laird Egan, Dripto M. Debroy, Crystal Noel, Andrew Risinger, Daiwei Zhu, Debopriyo Biswas, Michael Newman, Muyuan Li, Kenneth R. Brown, Marko Cetina, and Christopher Monroe. Fault-tolerant control of an error-corrected qubit. Nature, 598(7880):281–286, 2021.

[10] Lukas Postler, Sascha Heußen, Ivan Pogorelov, Manuel Rispler, Thomas Feldker, Michael Meth, Christian D. Marciniak, Roman Stricker, Martin Ringbauer, Rainer Blatt, Philipp Schindler, Markus Müller, and Thomas Monz. Demonstration of fault-tolerant universal quantum gate operations. arXiv preprint arXiv:2111.12654, 2021.

[11] V. Negnevitsky, M. Marinelli, K. K. Mehta, H.-Y. Lo, C. Flißmann, and J. P. Home. Repeated multi-qubit readout and feedback with a mixed-species trapped-ion register. Nature, 563(7732):527–531, 2018.

[12] C. Ryan-Anderson, J. G. Bohnet, K. Lee, D. Gresh, A. Hankin, J. P. Gaebler, D. Francois, A. Chernoguzov, D. Lucchetti, N. C. Brown, T. M. Gatterman, S. K. Halit, K. Gilmore, J. A.
Optimization and implementation of a surface-electrode ion trap junction

Gerber, B. Neyenhuis, D. Hayes, and R. P. Stutz. Realization of real-time fault-tolerant quantum error correction. *Phys. Rev. X*, 11:041058, Dec 2021.

[13] John Preskill. Reliable quantum computers. *Proceedings of the Royal Society of London. Series A: Mathematical, Physical and Engineering Sciences*, 454(1969):385–410, 1998.

[14] Daniel F. V. James. Quantum dynamics of cold trapped ions with application to quantum computation. *Applied Physics B*, 66:181–190, 1998.

[15] Prakash Murali, Drpto M. Debroy, Kenneth R. Brown, and Margaret Martonosi. Architecting noisy intermediate-scale trapped ion quantum computers. In *Proceedings of the ACM/IEEE 47th Annual International Symposium on Computer Architecture*, ISCA ’20, page 529–542, Virtual Event, 2020. IEEE Press.

[16] David J Wineland, C Monroe, Wayne M Itano, Dietrich Leibfried, Brian E King, and Dawn M Meekhof. Experimental issues in coherent quantum-state manipulation of trapped atomic ions. *Journal of Research of the National Institute of Standards and Technology*, 103(3):259, 1998.

[17] Yukai Wu, Sheng-Tao Wang, and L.-M. Duan. Noise analysis for high-fidelity quantum entangling gates in an anharmonic linear paul trap. *Phys. Rev. A*, 97:062325, 6 2018.

[18] X. Rebecca Nie, Christian F. Roos, and Daniel F.V. James. Theory of cross phase modulation for the vibrational modes of trapped ions. *Physics Letters A*, 373(4):422–425, 2009.

[19] C. Monroe, R. Raussendorf, A. Ruthven, K. R. Brown, P. Maunz, L.-M. Duan, and J. Kim. Large-scale modular quantum-computer architecture with atomic memory and photonic interconnects. *Phys. Rev. A*, 89:022317, 2 2014.

[20] D. Hucul, I. V. Iulek, G. Vittorini, C. Crocker, S. Debnath, S. M. Clark, and C. Monroe. Modular entanglement of atomic qubits using photons and phonons. *Nature Physics*, 11(1):37–42, 2015.

[21] H. J. Stephenson, D. P. Nadlinger, B. C. Nichol, S. An, P. Drmota, T. G. Ballance, K. Thirumalai, J. F. Goodwin, D. M. Lucas, and C. J. Ballance. High-rate, high-fidelity entanglement of qubits across an elementary quantum network. *Phys. Rev. Lett.*, 124:110501, 3 2020.

[22] D. Kielplinski, C. Monroe, and D. J. Wineland. Architecture for a large-scale ion-trap quantum computer. *Nature*, 417(6890):709–711, 2002.

[23] Naomi H. Nickerson, Joseph F. Fitzsimons, and Simon C. Benjamin. Freely scalable quantum technologies using cells of 5-to-50 qubits with very lossy and noisy photonic links. *Phys. Rev. X*, 4:041041, 12 2014.

[24] Ramil Nigmatullin, Christopher J Ballance, Niel de Beaudrap, and Simon C Benjamin. Minimally complex ion traps as modules for quantum communication and computing. *New Journal of Physics*, 18(10):103028, 10 2016.

[25] Jonathan P Home, David Hanneke, John D. Jost, Jason M. Amini, Dietrich Leibfried, and David J. Wineland. Complete methods set for scalable ion trap quantum information processing. *Science*, 325(5945):1227–1230, September 2009.

[26] H. Kaufmann, T. Ruster, C. T. Schmiegelow, M. A. Luda, V. Kaushal, J. Schulz, D. von Lindenfels, F. Schmidt-Kaler, and U. G. Poschinger. Scalable creation of long-lived multipartite entanglement. *Phys. Rev. Lett.*, 119:150503, 10 2017.

[27] J. M. Pino, J. M. Dreiling, C. Figgatt, J. P. Gaebler, S. A. Moses, M. S. Allman, C. H. Baldwin, M. Foss-Feig, D. Hayes, K. Mayer, C. Ryan-Anderson, and B. Neyenhuis. Demonstration of the trapped-ion quantum ccd computer architecture. *Nature*, 592(7853):209–213, 2021.

[28] R. B Blakestad, C. Ospelkaus, A. P. VanDevender, J. M. Amini, J. Britton, D. Leibfried, and D. J. Wineland. High-fidelity transport of trapped-ion qubits through an X-junction trap array. *Phys. Rev. Lett.*, 102:153002, 4 2009.

[29] R. B Blakestad, C. Ospelkaus, A. P VanDevender, J. H Wesenberg, M. J Biercuk, D. Leibfried, and D. J Wineland. Near-ground-state transport of trapped-ion qubits through a multidimensional array. *Phys. Rev. A*, 84:032314, 09 2011.

[30] Simon Ragg, Chiara Decaroli, Thomas Lutz, and Jonathan P. Home. Segmented ion-trap fabrication using high precision stacked wafers. *Review of Scientific Instruments*, 90(10):103203, October 2019.
Optimization and implementation of a surface-electrode ion trap junction

[31] Chiara Decaroli, Roland Matt, Robin Oswald, Christopher Axline, Maryse Ernzer, Jeremy Flannery, Simon Ragg, and Jonathan P Home. Design, fabrication and characterization of a micro-fabricated stacked-wafer segmented ion trap with two x-junctions. *Quantum Science and Technology, 6*(4):044001, jul 2021.

[32] J. H. Wesenberg. Electrostatics of surface-electrode ion traps. *Phys. Rev. A*, 78:063410, 12 2008.

[33] K. K. Mehta, A. M. Eltony, C. D. Bruzewicz, I. L. Chuang, R. J. Ram, J. M. Sage, and J. Chiaverini. Ion traps fabricated in a cmos foundry. *Appl. Phys. Lett.*, 105(4):044103, July 2014.

[34] D L Moehring, C Highstrete, D Stick, K M Fortier, R Haltli, C Tigges, and M G Blain. Design, fabrication and experimental demonstration of junction surface ion traps. *New Journal of Physics, 13*(7):075018, 7 2011.

[35] J M Amini, H Uys, J H Wesenberg, S Seidelin, J Britton, J J Bollinger, D Leibfried, C Ospelkaus, A P VanDevender, and D J Wineland. Toward scalable ion traps for quantum information processing. *New Journal of Physics, 12*(3):033031, 3 2010.

[36] Kenneth Wright, Jason M Amini, Daniel L Faircloth, Curtis Volin, S Charles Doret, Harley Hayden, C-S Pai, David W Landgren, Douglas Denison, Tyler Killian, Richard E Slusher, and Alexa W Harter. Reliable transport through a microfabricatedX-junction surface-electrode ion trap. *New Journal of Physics, 15*(3):033004, 3 2013.

[37] G. Shu, G. Vittorini, A. Buikema, C. S. Nichols, C. Volin, D. Stick, and Kenneth R. Brown. Heating rates and ion-motion control in a Y-junction-surface-electrode trap. *Phys. Rev. A, 89*:062308, 6 2014.

[38] J P Home, D Hanneke, J D Jost, D Leibfried, and D J Wineland. Normal modes of trapped ions in the presence of anharmonic trap potentials. *New Journal of Physics, 13*(7):073026, 7 2011.

[39] Fastino DAC from creotech, https://creotech.pl/product/fastino/.

[40] Ludwig Erasmus de Clercq. *Transport Quantum Logic Gates for Trapped Ions*. PhD thesis, ETH Zürich, 2015.

[41] J. H. Wesenberg. Ideal intersections for radio-frequency trap networks. *Phys. Rev. A, 79*:013416, 1 2009.

[42] Nikolai Konenkov, Frank Londry, Chuanfan Ding, and D.J. Douglas. Linear quadrupoles with added hexapole fields. *Journal of the American Society for Mass Spectrometry, 17*(8):1063–1073, 2006.

[43] H.G. Dehmelt. Radiofrequency spectroscopy of stored ions i: Storage. In *Advances in Atomic and Molecular Physics*, volume 3, pages 53–72, 1968.

[44] Dieter Gerlich. *Inhomogeneous RF Fields: A Versatile Tool for the Study of Processes with Slow Ions*, pages 1–176. John Wiley & Sons, Ltd, 1992.

[45] A Mokhberi, R Schmied, and S Willitsch. Optimised surface-electrode ion-trap junctions for experiments with cold molecular ions. *New Journal of Physics, 19*(4):043023, 4 2017.

[46] M. Brownnutt, M. Kumph, P. Rabl, and R. Blatt. Ion-trap measurements of electric-field noise near surfaces. *Rev. Mod. Phys.*, 87:1419–1482, 12 2015.

[47] Roman Schmied, Janus H. Wesenberg, and Dietrich Leibfried. Optimal surface-electrode trap lattices for quantum simulation with trapped ions. *Phys. Rev. Lett.*, 102:233002, 6 2009.

[48] Roman Schmied. Electrostatics of gapped and finite surface electrodes. *New Journal of Physics, 12*(2):023038, 2 2010.

[49] S Charles Doret, Jason M Amini, Kenneth Wright, Curtis Volin, Tyler Killian, Arkadas Ozakin, Douglas Denison, Harley Hayden, C-S Pai, Richard E Slusher, and Alexa W Harter. Controlling trapping potentials and stray electric fields in a microfabricated ion trap through design and compensation. *New Journal of Physics, 14*(7):073012, 7 2012.

[50] John David Jackson. *Classical electrodynamics*. J. Wiley & Sons, New York, third edition, 1999.

[51] M. G. House. Analytic model for electrostatic fields in surface-electrode ion traps. *Phys. Rev. A, 78*:033402, 9 2008.

[52] D. Hucul, M. Yeo, S. Olmschenk, C. Monroe, W. K. Hensinger, and J. Rabchuk. On the transport of atomic ions in linear and multidimensional ion trap arrays. *Quantum Info. Comput.,*
Optimization and implementation of a surface-electrode ion trap junction

8(6):501–578, July 2008.

[53] Mário H Oliveira and José A Miranda. Biot-savart-like law in electrostatics. European Journal of Physics, 22(1):31–38, 1 2001.

[54] D.J. Berkeland, J.D. Miller, James C Bergquist, Wayne M Itano, and David J Wineland. Minimization of ion micromotion in a paul trap. Journal of applied physics, 83(10):5025–5033, 1998.

[55] Norman W McLachlan. Theory and application of Mathieu functions. Clarendon Press, Oxford, 1951.

[56] J.A. Richards. Analysis of periodically time-varying systems. Springer-Verlag, 1983.

[57] J. Chiaverini, R. B. Blakestad, J. Britton, J. D. Jost, C. Langer, D. Leibfried, R. Ozeri, and D. J. Wineland. Surface-electrode architecture for ion-trap quantum information processing. Quantum Info. Comput., 5(6):419–439, September 2005.

[58] J.M. Amini, J. Britton, Leibfried D., and D.J. Wineland. Micro-Fabricated Chip Traps for Ions, chapter 13, pages 395 – 420. WILEY-VCH Verlag GmbH & Co. KGAA, Weinheim, 2011.

[59] Karan K. Mehta, Colin D. Bruzewicz, Robert McConnell, Rajeev J. Ram, Jeremy M. Sage, and John Chiaverini. Integrated optical addressing of an ion qubit. Nature Nanotechnology, 11(12):1066–1070, 2016.

[60] Karan K. Mehta, Chi Zhang, Maciej Malinowski, Thanh-Long Nguyen, Martin Stadler, and Jonathan P. Home. Integrated optical multi-ion quantum logic. Nature, 586(7830):533–537, 2020.

[61] R. J. Niffenegger, J. Stuart, C. Sorace-Agaskar, D. Kharas, S. Bramhavar, C. D. Bruzewicz, W. Loh, R. T. Maxson, R. McConnell, D. Reens, G. N. West, J. M. Sage, and J. Chiaverini. Integrated multi-wavelength control of an ion qubit. Nature, 586(7830):538–542, 2020.

[62] M. Ivory, W. J. Setzer, N. Karl, H. McGuinness, C. DeRose, M. Blain, D. Stick, M. Gehl, and L. P. Parazzoli. Integrated optical addressing of a trapped ytterbium ion. Phys. Rev. X, 11:041033, 11 2021.

[63] Karan K. Mehta and Rajeev J. Ram. Precise and diffraction-limited waveguide-to-free-space focusing gratings. Scientific Reports, 7(1):2019, 2017.

[64] Karan K. Mehta, Chi Zhang, Stefanie Miller, and Jonathan P. Home. Towards fast and scalable trapped-ion quantum logic with integrated photonics. In Proc. SPIE, volume 10933, March 2019.

[65] Kerstin Wörhoff, René G. Heideman, Arne Leins, and Marcel Hoekman. Triplex: a versatile dielectric photonic platform. Advanced Optical Technologies, 4(2):189–207, 2015.

[66] Cheryl Sorace-Agaskar, Dave Kharas, Siva Yegnanarayanan, Ryan T. Maxson, Gavin N. West, William Loh, Suraj Bramhavar, Rajeev J. Ram, John Chiaverini, Jeremy Sage, and Paul Juodawlkis. Versatile silicon nitride and alumina integrated photonic platforms for the ultraviolet to short-wave infrared. IEEE Journal of Selected Topics in Quantum Electronics, 25(5):1–15, 2019.

[67] Gavin N. West, William Loh, Dave Kharas, Cheryl Sorace-Agaskar, Karan K. Mehta, Jeremy Sage, John Chiaverini, and Rajeev J. Ram. Low-loss integrated photonics for the blue and ultraviolet regime. APL Photonics, 4(2):026101, 2019.

[68] Nicholas D. Guise, Spencer D. Fallek, Kelly E. Stevens, K. R. Brown, Curtis Volin, Alexa W. Harter, Jason M. Amini, Robert E. Higashi, Son Thai Lu, Helen M. Chanhvongsak, Thi A. Nguyen, Matthew S. Marcus, Thomas R. Ohmstein, and Daniel W. Youngner. Ball-grid array architecture for microfabricated ion traps. Journal of Applied Physics, 117(17):174901, May 2015.

[69] Yan Yang, Mingbin Yu, Qing Fang, Junfeng Song, Xiaoguang Tu, Patrick Guo-Qiang Lo, and Rusli. 3d silicon photonics packaging based on tsv interposer for high density on-board optics module. In 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), pages 483–489, 2016.