High-Performance Tensor Contraction without BLAS

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Abstract—Tensor computations—in particular tensor contraction (TC)—are important kernels in many scientific computing applications (SCAs). Due to the fundamental similarity of TC to matrix multiplication (MM) and to the availability of optimized implementations such as the BLAS, tensor operations have traditionally been implemented in terms of BLAS operations, incurring both a performance and a storage overhead. Instead, we implement TC using the much more flexible BLIS framework, which allows for reshaping of the tensor to be fused with internal partitioning and packing operations, requiring no explicit reshaping operations or additional workspace. This implementation achieves performance approaching that of MM, and in some cases considerably higher than that of traditional TC. Our implementation also supports multithreading using an approach identical to that used for MM in BLIS, with similar performance characteristics. The complexity of managing tensor-to-matrix transformations is also handled automatically in our approach, greatly simplifying its use in SCAs.

I. INTRODUCTION

Tensors are an integral part of many scientific disciplines \[36], \[28], \[2], \[20], \[19]. At their most basic, tensors are simply a multidimensional collection of data (or a multidimensional array, as expressed in many programming languages). In other cases, tensors represent multidimensional transformations, extending the theory of vectors and matrices. The logic of handling, transforming, and operating on tensors is a common task in many scientific codes, often being reimplemented many times as needed for a particular project. Calculations on tensors also often account for a significant fraction of the running time of such tensor-based codes, and so their efficiency has a significant impact on the rate at which the resulting scientific advances can be achieved.

In order to perform operations on tensors, such as tensor contraction, there are currently two commonly used alternatives: (1) write explicit loops over the various tensor indices (this is the equivalent of the infamous triple loop for matrix multiplication), or (2) “borrow” efficient routines from optimized matrix libraries such as those implementing the BLAS interface \[21], \[9], \[8]. Choice (1) results in a sub-optimal implementation just as in the matrix case, and also generally requires hardcoding the specific tensor operation, including the number of indices on each tensor (which means that code cannot be efficiently reused as there are many possible combinations of number and configuration of tensor indices). Choice (2) may provide for higher efficiency, but requires sometimes complicated logic to manipulate the tensors and set up the necessary matrix operation. Additionally, in most cases the tensors must be physically altered (meaning that the cost of moving a large amount of data is incurred), or only a subset of the indices may be operated on at a time (this is akin to writing a matrix multiplication routine with only the level 1 or 2 BLAS).

Several libraries exist that take care of part of this issue, namely the tedium of encoding the logic for treating tensors as matrices during various operations. For example, the MATLAB Tensor Toolbox \[1] provides a fairly simple means for performing tensor contractions and other operations without exposing the internal conversion to matrices. The NumPy library \[33] provides a similar mechanism in the Python language. Both libraries still rely on the mapping of tensors to matrices and the unavoidable overhead in time and space (and when a pre-packaged solution is not available, significant complexity) thus incurred.

A natural solution to this problem is to create a dedicated tensor library implementing a high-performance, “native” tensor contraction implementation (without the use of the BLAS), but with similar optimizations for cache reuse, vectorization, etc. as those used for matrix multiplication. For a particular instance of a tensor contraction this is a feasible if not tedious task, using existing techniques from dense linear algebra (DLA). However, making a general tensor library is another proposition altogether, as such a library must handle any type of tensor contraction the user chooses at runtime (this discounts the possibility of static code transformation/compilation techniques such as in Built-to-Order BLAS \[3] and DxTer \[25]). Since the number of possible contraction types grows exponentially with the number of indices, explicitly treating each instance of tensor contraction is a futile endeavor.

The newly-developed BLIS framework \[35], \[29], \[34] implements matrix operations with a very high degree of efficiency, including a legacy BLAS interface. However, unlike common BLAS libraries, especially commercial libraries such as Intel’s Math Kernel Library, BLIS exposes the entire internal structure of algorithms such as matrix multiplication, down to the level of the micro-kernel, which is the only part that must be implemented in highly-optimized assembly language. In addition to greatly reducing the effort required to build a BLAS-like library, the structure of BLIS allows one to
view a matrix operation as a collection of independent pieces. The default matrix multiplication algorithm in BLIS is like building a LEGO kit by following the provided instructions. One may, however, throw the instructions aside and use the available pieces to build a custom framework for purposes beyond traditional dense linear algebra, an example of which is given in [39]. We will illustrate exactly how this the flexibility of this approach may be used to implement high-performance tensor contraction by breaking though the traditionally opaque matrix multiplication interface.

The specific contributions of this paper are:

- A novel logical mapping from general tensor layouts to a non-standard (neither row-major nor column-major) matrix layout.
- Implementations of key BLIS kernels using this novel matrix layout, eliminating the need for explicit transposition of tensors while retaining a matrix-oriented algorithm.
- A new BLIS-like framework incorporating these kernels that achieves high performance for tensor contraction and does not require external workspace.
- Efficient multithreading of tensor contraction within the aforementioned framework.

II. MATRIX MULTIPLICATION

Before delving into tensor contraction, let us first review the basic techniques used in high-performance matrix multiplication, expressed generally as $C = \alpha A \cdot B + \beta C$. The matrices $A$, $B$, and $C$ are $m \times k$, $k \times n$, and $m \times n$ respectively. We refer to the length and width of each matrix as its shape, and refer to individual elements of each tensor as $A_{ip}$, $C_{ij}$, etc. where $0 \leq i < m$, $0 \leq j < n$, and $0 \leq p < k$. Written element-wise, the basic matrix multiplication operation is then, $C_{ij} = \sum_{p=0}^{k-1} A_{ip} B_{pj} + \beta C_{ij}$. This element-wise definition of matrix multiplication is critical to relating it to tensor contraction.

Most current high-performance implementations follow the approach pioneered by Goto [11], [12], in which the matrices $A$, $B$, and $C$ are successively partitioned (sub-divided) into panels which are designed to fit into the various levels of the cache hierarchy, and then panels of $A$ and $B$ are packed into temporary buffers $A_i$ and $B_p$ in a non-standard (not strictly row- or column-major) storage format to facilitate vectorization and memory locality. These packed buffers are then used in a matrix multiplication sub-problem executed by a (typically hand-coded assembly) inner kernel. The BLIS approach [35] extends this by exposing two additional partitioning loops in the inner kernel and instead using a much simpler (although still generally hand-coded assembly) micro-kernel, which performs a sequence of outer-product operations on a micro-tile of the output matrix $C$ which fits in the machine registers. The BLIS approach is illustrated schematically in Figure 1.

The ordering of the partitioning loops in the Goto and BLIS approaches defines the points in the algorithm at which $A$ and $B$ are packed as well as the form of the micro-kernel. This ordering is one of a family of such approaches [14], but in each approach there are necessarily three common characteristics:

1) The matrices $A$, $B$, and $C$ are successively partitioned into smaller and smaller pieces.
2) $A$ and/or $B$ are packed into contiguous buffers in a special storage format, and in some orderings contributions to $C$ are accumulated in a packed buffer which must then be unpacked and accumulated into memory.
3) The basic unit of computation is a micro-kernel that acts on packed portions of two of the three matrices, and a very small micro-tile of the third.

These characteristics will serve as basic points of interface between matrix-based and tensor-based algorithms in the following sections.

III. TENSOR CONTRACTION

A tensor, in most basic terms, is simply a multi-dimensional array. For example, vectors, being one-dimensional arrays, and matrices, being two-dimensional arrays, are instances of tensors. However, tensors may have an unlimited number of
dimensions (though a finite number in numerical applications), or as few as zero dimensions (representing a scalar value). We denote a general $d$-dimensional tensor $T$ of shape $n_{i_0} \times \ldots \times n_{i_{d-1}}$ by referring generically to its elements,

$$T \equiv T_{i_0 \ldots i_{d-1}}, \quad 0 \leq i_k < n_k \forall 0 \leq k < d$$

Notationally, the symbols $i_0 \ldots$ will be used to label particular dimensions of a tensor, rather than refer to specific values for each tensor dimension, and mnemonic symbols $abc \ldots$ will usually be used for simplicity. The specific labels given to the dimensions are arbitrary, so that, for example, a 4-dimensional tensor $G$ may equivalently be written as $G_{abcd}$, $G_{pqrs}$, $G_{(trqz)}$, etc.

Tensor contraction generalizes the concept of matrix multiplication to higher dimensions (numbers of indices), just as tensors generalize the notion of matrices. Given two input tensors $A$ and $B$ and an output tensor $C$, a tensor contraction is formed by 1) concatenating the tensors $A$ and $B$ into an intermediate tensor $\hat{C}$, and 2) contracting some number of the dimensions of $\hat{C}$ coming from $A$ with an equal number of dimensions (of the same length) of $C$ coming from $B$. If $A$ is of dimension $d^A$ and $B$ is of dimension $d^B$, then concatenation simply produces a tensor of dimension $d^A + d^B$,

$$\hat{C}_{ab\ldots cd\ldots} = A_{ab\ldots} \cdot B_{cd\ldots}$$

where the elements of $\hat{C}$ are the product of the elements of $A$ and $B$ according to the above formula taken element-wise. Choosing the dimension $b$ from tensor $A$ and the dimension $c$ from tensor $B$ for example, the contraction procedure produces the tensor $C$ of dimension $d^A + d^B - 2$ defined by inserting a Kronecker delta $\delta_{bc}$ ($\delta_{bc} = 1$ if $b = c$ and 0 otherwise), and a sum over both $b$ and $c$,

$$C_{a\ldots d\ldots} = \sum_{b,c=0}^{n_k-1} \delta_{bc} \hat{C}_{ab\ldots cd\ldots} = \sum_{b=0}^{n_k-1} A_{ab\ldots} \cdot B_{bd\ldots}$$

In general, the dimension of $C$ will be $d^A + d^B - 2c$ where $c$ is the number of dimension pairs contracted.

The final equality gives a convenient definition for tensor contraction, and a simple element-wise formula for computing the elements of $C$. Additionally, this form begins to reveal the similarity of tensor contraction to matrix multiplication. When the additional dimensions (represented by $\ldots$) are removed, the example above is indeed simply matrix multiplication.

Note that the order of the dimensions appearing in a tensor is important throughout the operation. While we may assign any arbitrary labels to the dimensions to begin with, interchanging (transposing) labels in an expression refers to different elements of the tensor in general, just as, for example, $M_{ab} \neq M_{ba}$ in general for matrices. With this in mind, the above definition of tensor contraction is in fact somewhat too restrictive for general use, as the indices $a \ldots$ in $C$ must appear in the same order as in $A$ and likewise for $d \ldots$, and the indices $a\ldots$ must all appear before the indices $d\ldots$ in $C$.

To be completely general, we extend the definition above in a more precise and flexible way. Let us group the dimensions of an input tensor $A$ into two bundles $I = i_0 \ldots i_{r-1}$ and $P = p_0 \ldots p_t$. Likewise the dimensions of $B$ are grouped into bundles $J = j_0 \ldots j_{s-1}$ and $P$ (which are dimensions in common with $A$, i.e. they carry the same labels and are of the same length). The dimensions in these bundles may appear in any order in $A$ and $B$,

$$A \equiv A_{\{IP\}}, \quad B \equiv B_{\{PJ\}}$$

where $\{\ldots\}$ denotes an arbitrary ordering of the enclosed dimensions. The general tensor contraction of $A$ and $B$ into $C$ is then given by,

$$C_{\{IJ\}} = \sum_P A_{\{IP\}} \cdot B_{\{PJ\}}$$

where $\sum_P = \sum_{p_0=0}^{n_{p_0}-1} \ldots \sum_{p_{r-1}=0}^{n_{p_{r-1}}-1}$. Now the connection to matrix multiplication is readily apparent. The ordering of the dimensions in $A$, $B$, and/or $C$ takes the place of explicit transposition of the operations, much as for matrices $C = A^T \cdot B$ can be written $C_{ij} = \sum_{p=0}^{n_p-1} A_{ip} B_{pj}$ for example. The dimensionality of the tensors is easily computed from the size of the bundles: $d^A = r + t$, $d^B = t + s$, and $d^C = r + s$. If each of the dimensions is $O(n)$, then the tensor contraction operation requires $O(n^{r+s+t})$ FLOPs.

In computational applications, it is important to define the data layout of tensors (and matrices). The data layout provides a mapping between elements of the tensor and locations in (linear) memory. For matrices, the two main data layouts are row-major and column-major, where elements are assigned successive locations in memory moving across the first row and then continuing across subsequent rows in the former, and moving down the first and then subsequent columns in the latter. For element $M_{ij}$ of an $m \times n$ matrix, this gives a location (relative to element $M_{00}$ of $i \cdot n + j$ and $i + j \cdot m$ respectively. These layouts may be readily extended to tensors. For a general row-major layout, the tensor element $T_{i_0 \ldots i_{d-1}}$ for $T$ of shape $n_{i_0} \times \ldots \times n_{i_{d-1}}$ is at location $loc(i_0, \ldots , i_{d-1}) = \sum_{k=0}^{d-1} i_k \prod_{l=k+1}^{d-1} n_{i_l}$. In generalized column-major layout this element is at location $loc(i_0, \ldots , i_{d-1}) = \sum_{k=0}^{d-1} i_k \prod_{l=k+1}^{d-1} n_{i_l}$. However, in general the data layout may be more flexible than this to support situations where a sub-tensor is being referenced, or to implicitly transpose dimensions of a tensor for example. In the most general case, the location of element $T_{i_0 \ldots i_{d-1}}$ is given by $loc(i_0, \ldots , i_{d-1}) = \sum_{k=0}^{d-1} i_k \cdot s_i^T_k$, where $s_i^T_k$ is the stride of dimension $i_k$ in $T$. These strides can theoretically be any integral value, but positive values are usually most useful. Additionally, it is often advantageous to require that the product $n_{i_k} \cdot s_i^T_k$ be less than or equal the the next largest stride for each value $k$, so that elements of the tensor have unique locations in memory. If the smallest stride has value 1, then the tensor is said to have stride-1 access. For matrices, which have two strides, we refer to the row stride of matrix $M_{ij}$, $rs^M \equiv s_i^M$ and the column stride, $cs^M \equiv s_j^M$. 

IV. Tensors as Matrices

A. Traditional Methods

If each of the bundles $I$, $J$, and $P$ contains only one dimension, then the above definition of tensor contraction becomes matrix multiplication with possible transposition of $A$, $B$, and $C$. The question then arises, “Can we relate a bundle of more than one dimension to a single dimension of a matrix?” This is indeed trivially possible if the dimensions in the bundle are contiguous. We say that dimension $j$ follows dimension $i$ contiguously in $T$ if $n_i \cdot s_i^T = s_j^T$. In this case, all of the $n_i \cdot n_j$ elements spanned by $i$ and $j$ may also be addressed by a single index $k$ of length $n_k = n_i \cdot n_j$ with stride $s_k^T = s_i^T$. In other words, the tensors $T_{...ij...}$ and $T_{...ik...}$ contain the same elements at the same locations in memory, although they are of different dimensionality. A bundle of dimensions $i_0 \ldots i_m-1$ is then mutually contiguous in $T$ if $i_k$ follows $i_{k-1}$ contiguously in $T$ for all $0 < k < m$.

If a bundle of dimensions $B$ is mutually contiguous in all of the tensors in a computation (in which its dimensions appear), and the dimensions in $B$ are either all contracted or all not contracted, then it may be functionally replaced with a single dimension $B$ (i.e., the computation using $B$ instead of $B$ results in the same values for all elements in the output tensor). So, if in the tensor contraction $C_{IJ} = \sum_p A_{Ip} B_{pJ}$, all bundles $I$, $J$, and $P$ are mutually contiguous, then the operation reduces to matrix multiplication,

$$C_{IJ} = \sum_{p=0}^{n_P} A_{IP} B_{pJ}$$

where $n_P = \prod_{k=0}^{t-1} n_{p_k}$ and similarly for $n_I$ and $n_J$.

The condition for mutual contiguity is trivially met for successive dimensions in a generalized column-major or row-major layout, so that for example $A_{i_0 \ldots i_{t-1} p_0 \ldots p_{t-1}}$ stored in a column-major layout may be treated as a matrix $A_{IP}$ with no further changes. In a general layout, or if the dimensions in $A$ are not ordered properly even in a column-major layout, then $A$ must be transposed (permuted) into a new layout or into a new tensor with the proper ordering,

$$A'_{IP} = A_{i_0 \ldots i_{t-1} p_0 \ldots p_{t-1}} = A_{IP}$$

This transposition will require elements to be moved to new memory locations. Performing this transposition in-place (not requiring any additional storage) is only possible with great complexity \[7, 17\] or under special circumstances. Usually, a new storage area for $A'$ is created and then all of the elements are copied into their new locations. Thus, the TTDT (transpose-transpose-DGEMM-transpose) algorithm in Figure 2 for computing a tensor contraction can be derived that uses matrix multiplication internally, which is highly desirable due to the availability of high-performance matrix multiplication implementations.

This method has been used to implement tensor contraction in a vast number of scientific applications over the past few decades, and is the implementation used by popular tensor packages such as NumPy \[33\] and the MATLAB Tensor Toolbox \[1\]. However, there are some drawbacks to this approach:

- The storage space required is increased by a factor of two, since full copies of $A$, $B$, and $C$ are required. This storage space may either be allocated inside the tensor contraction routine or supplied as workspace by the user, complicating user interfaces.

- The tensor transpositions require a (sometimes quite significant) amount of time relative to the matrix multiplication step. For example, after aggressively reordering operations to reduce the number of transpositions needed in a quantum chemistry application \[26\] (transpositions can be elided if the ordering required for one operation matches that required for the next), we still measure 15-50% of the total program time spent in tensor transposition.

- If a comprehensive tensor contraction interface is not available (e.g. in FORTRAN or C), or if tensor transposition must be otherwise handled by the calling application to ensure efficiency, significant algorithmic and code complexity is required which increases programmer burden and the incidence of errors, while obscuring the scientific algorithms in the application. In the aforementioned quantum chemistry example, approximately 20% of the code is directly related to implementing tensor contraction using TTDT.

These deficiencies motivate our implementation of a “native” (i.e. acting directly on general tensors) high-performance tensor contraction algorithm.

B. New Matrix Representations of Tensors

Using the notion of contiguity, tensors can be manipulated as if they were simple matrices in certain conditions. In the general case, though, how can we represent the mapping from tensor to matrix without physical movement of the tensor elements? Put another way, how can we relate the logical layout of a matrix $M_{IJ}$ (i.e. the values of the dimensions $I$ and $J$) to the data layout of a related tensor $T_{I(J)}$ for two bundles $I$ and $J$?

When stored in column-major layout, both the matrix $M_{IJ}$ and the tensor $T_{IJ}$ have elements in the same memory locations, and so using the definitions of the column-major
layout we have,

\[
\vec{I} + n_i \vec{J} = \sum_{k=0}^{d_j-1} i_k \prod_{l=0}^{k-1} n_{i_l} + \sum_{k=0}^{d_j-1} j_k \left( \prod_{l=0}^{k-1} n_{i_l} \right) \left( \prod_{l=0}^{k-1} n_{j_l} \right)
\]

Since this hold for all tensor lengths (values of \( n \)), then the following are true,

\[
\vec{I} = \sum_{k=0}^{d_j-1} i_k \prod_{l=0}^{k-1} n_{i_l}, \quad \vec{J} = \sum_{k=0}^{d_j-1} j_k \prod_{l=0}^{k-1} n_{j_l}
\]

This gives a relationship between the logical layouts of \( M_{\vec{I},\vec{J}} \) and \( T_{\vec{I},\vec{J}} \) (and \( T_{\vec{I},\vec{J}} \)) since it shares the same dimensions, i.e. given the value of \( \vec{I} \) we can determine the values of \( \{i_k\}_{k=0}^{d_j-1} \) and vice versa, and similarly for \( \vec{J} \).

This tells us nothing new for \( T_{\vec{I},\vec{J}} \) since we already know that its elements share memory locations with \( M_{\vec{I},\vec{J}} \), but for \( T_{\vec{I},\vec{J}} \) we can use the information about the logical layout along with a general stride data layout (\( \{s_{i_k}^T\}_{k=0}^{d_j-1} \) and \( \{s_{j_k}^T\}_{k=0}^{d_j-1} \)) to relate to the physical data layout of \( T_{\vec{I},\vec{J}} \). Using this mapping we can represent the locations of elements in \( T_{\vec{I},\vec{J}} \) in a matrix-oriented form,

\[
\text{loc}(i_0, \ldots, i_{d_j-1}, j_0, \ldots, j_{d_j-1}) = \sum_{k=0}^{d_j-1} i_k s_{i_k}^T + \sum_{k=0}^{d_j-1} j_k s_{j_k}^T = rscat^T_k + cscat^M_k
\]

where \( rscat^M \) is evaluated by computing \( \{i_k\}_{k=0}^{d_j-1} \) from \( \vec{I} \) as above and then multiplying by the strides \( \{s_{i_k}^T\}_{k=0}^{d_j-1} \), and similarly for \( cscat^M \) (these quantities are labeled with \( M \) because they describe a matrix layout). The general tensor \( T_{\vec{I},\vec{J}} \) may then be represented by a matrix \( M_{\vec{I},\vec{J}} \) imbued with a scatter-matrix layout defined by the vectors \( rscat^M \) and \( cscat^M \) instead of scalar values \( rs^M \) and \( cs^M \).

This layout allows for any matrix code, in particular the partitioning and packing routines in BLIS, as well as an adapter to the micro-kernel (an adapter must be used because assumptions about matrix layout are hard-coded into the micro-kernel) to be written to access general tensor elements in-place while retaining a matrix-based logical flow. We have written scatter-matrix-based versions of these routines and incorporated them into a BLIS-like framework (the reason for not using BLIS directly will be discussed later), and we term this the Scatter-Matrix Tensor Contraction (SMTCT) algorithm.

The scatter-matrix layout leaves some room for improvement in performance, however, since for each matrix (tensor) element, an additional scatter value must be loaded from memory (assuming access to the scatter value in the other dimension can be amortized). This roughly doubles the memory traffic and removes many opportunities for efficient vectorization in the packing kernels and in the micro-code. Because of this, we have defined an additional matrix layout which allows for column-major- and row-major-like access as much as possible.

Since the micro-kernel is the basic unit of work in BLIS, the size of a micro-kernel update defines a natural blocking of the matrix dimensions \( m \) and \( n \). These block sizes are denoted \( m_R \) and \( n_R \) and are usually 4, 6, or 8 for double-precision real numbers. So, while the values of the scatter vectors \( rscat^M \) and \( cscat^M \), in particular \( rscat^A \) and \( cscat^C \) which define element positions dependent on \( i \), and \( cscat^B \) and \( cscat^C \) which depend on \( j \) are in general not "well-behaved" (monotonically increasing, regularly spaced, etc.) over their entire range, they may often be well-behaved for short stretches. More specifically using the example of \( rscat^A \), the first \( n_{i_0} - 1 \) values (after the first) will be separated by \( s_{i_0}^A \), then the next element separated by \( s_{i_0}^A - (n_{i_0} - 1) s_{i_0}^A \) (which may be negative), followed by another stretch of \( n_{i_0} - 1 \) regularly-spaced values, and so on. Thus, if \( n_{i_0} \gg m_R \), we can partition \( rscat^A \) into blocks of size \( m_R \), most of which will be well-behaved.

We introduce a second vector \( rs^A \) (not to be confused with the scalar of the same name) of length \( n_{i_0} m_R \), \( rs^A_{k} = S \) if the scatter values \( rscat^A_{k m_R} \ldots rscat^A_{(k+1) m_R - 1} \) are regularly spaced by some stride \( S \), and zero otherwise to denote an invalid block row stride. A similar block stride vector is added to augment the remaining scatter vectors. For \( cscat^A \) and \( cscat^B \) which depend on \( p \), we do not do any blocking and \( cs^A \equiv rs^B \equiv \{0\} \) with an implicit block size of \( k \). In future work, an additional blocking parameter \( k_R \) could be added to facilitate transpose vectorization during packing and other optimizations. The combination of scatter vectors \( rscat^M \) and \( cscat^M \) and block stride vectors \( rs^M \) and \( cs^M \) w.r.t some blocking parameters \( I_R \) and \( J_R \) define a block-scatter-matrix layout. We denote the tensor contraction implementation using this approach as the Block-Scatter-Matrix Tensor Contraction (BSMTC) algorithm. An example of a block-scatter-matrix layout is given in Figure 3.

The scatter-matrix and block-scatter-matrix layouts require storage of additional vectors of length \( \mathcal{O}(n) \). We wish to avoid allocating these vectors inside the tensor contraction implementation for several reasons:

- This requires at least one general memory allocation (\( malloc \)) per call which may involve virtual memory operations (e.g. \( mmap \)).
- This requires unbounded additional storage (although the amount is still much less than in \( TTDT \)).
- This complicates the interface because users may want to supply external workspace or precomputed scatter vectors etc.

Instead, we delay the transition to a scatter- or block-scatter-matrix layout until the input and output matrices have been partitioned into panels of fixed (bounded) size. For the matrices \( A \) and \( B \) this occurs when panels \( A_i \) and \( B_j \) are packed into contiguous storage (see Figure 1), and for \( C \) this occurs just before entry into the inner kernel (macro-kernel in BLIS parlance). At this stage, the maximum size of the scatter vectors is known, and they can be allocated from persistent
storage in the same manner as the pack buffers of \( A \) and \( B \). In our implementation, the size of the \( A \) and \( B \) pack buffers is increased slightly to accommodate the scatter vectors, and a memory acquire operation (which does not require allocation on repeated use) is only required for the scatter vectors of \( C \).

We then have four layout types which are encountered during the contraction algorithm: general tensor layout, scatter-matrix layout, block-scatter-matrix layout, and packed matrix layout (for \( A_1 \) and \( B_2 \)). The way these layout types are handled in the key operations in the BLIS approach are summarized in Figure 4, along with a comparison to a normal matrix layout.

### C. Implementation Details and Multithreading

The SMTC and BSMTC algorithms we have implemented use a BLIS-like framework and the actual BLIS micro-kernels. The reasons we did not pursue using the BLIS framework directly are subtle. On one hand, the BLIS framework does offer substantial flexibility in defining custom operations such as packing kernels, but not quite the level of flexibility we require especially with regards to the loops inside the macro-kernel and at the level of the micro-kernel. On the other hand, we also wished to explore alternative techniques for implementing the BLIS approach. One significant difference of our implementation to BLIS is that where BLIS uses a recursive data structure to specify the necessary partitioning and packing operations at runtime (the control tree), we use a C++11 variadic template structure which enables the compiler to automatically select the appropriate partitioning and packing operations based on the type of the tensor or matrix object passed to each step. For example, all operands begin as Tensor<T> objects, are wrapped in matrix-aware TensorMatrix<T> objects, are eventually “matriﬁed” into BlockMatrix<T> objects, and then \( A \) and \( B \) are packed into regular Matrix<T> objects. Overloaded packing and micro-kernel wrapper functions handle each of these types as appropriate. Our implementation does use the various assembly micro-kernels and blocking parameters from BLIS, though, and in testing we have found no measurable difference in performance of matrix multiplication. Nearly-complete C++ code for the BSMTC driver is given in Figure 5.

In this template implementation, the data type (float, double, etc.) is a template parameter, but the number of dimensions in each tensor is not. We have found requiring this parameter to be a compile-time constant to be overly restrictive in practice. However, because the dimensionality is not known a priori (or bounded), the interface layer must perform some small memory allocations to manipulate arrays of dimension lengths, strides, labels, etc. Most malloc implementations contain optimizations for very small allocations however (for example, Apple’s OS X has a per-thread pool for blocks of up to 992 bytes), and indeed we do not measure a signiﬁcant overhead in our implementation due to these allocations. Additionally, dimension labels (represented by a string type) almost always fall in the range of the small string optimization (SSO).
TensorMatrix<T> A, B, C;

GEMM<PartitionN<NC>,
    PartitionK<KC>,
    MatrifyK<MC>,
    MatrifyAndPackAB<MR,KR>,
    MatrifyC<MR, NR>,
    PartitionN<NR>,
    PartitionM<MR>,
    MicroKernel<MR,NR>>::run<T> gemm;

// comm is the thread communicator
// (threading details not shown)
gemm(comm, alpha, A, B, beta, C);

Figure 5. Variadic template implementation of BSMTC. The steps specified in the GEMM<...> template can be directly compared to those in Figure 1 with the addition of tensor “matrification” (conversion from TensorMatrix<T> to BlockScatterMatrix<T>).

which eliminates some allocations. If handling short vectors becomes an issue, it is also feasible to enforce a maximum dimensionality for tensors so that a static allocation or the stack may be used.

Run-time information controlling the tensor contraction operation is stored in the variadic template object on a per-thread basis. This information includes the address of the packing buffers and the desired level of parallelism at each loop, but also information about the current thread communicator. The thread communicator is a concept that was adopted in BLIS to aid in parallelization [29], [34], and closely resembles the communicator concept from MPI. Each communicator references a shared barrier object which the threads utilize for synchronization. Parallelism is managed at each level by splitting the communicator into a set of sub-communicators to which work is assigned. As in BLIS, there are five parallelizable loops as can be seen in Figure 1 although the loop over dimension p (with block size kC) is not parallelized since this would require additional synchronization and/or temporary buffers with reduction.

For both matrices and tensors, it is important to attempt to access elements in a way that maximizes temporal locality of the data. For matrices where one of the strides is 1 (as is always true in the BLAS interface), this means simply ordering loops such that the stride-1 dimension is iterated over in the inner loop. This affects access during packing and during the update to C in the micro-kernel. Since the micro-kernel is usually hand-written in assembly, it is simpler to assume that $rs^C = 1$ and to compute the equivalent operation $CT = \alpha B^TA^T + \beta C^T$ in the case that $cs^C = 1$ instead. This assures high performance for all eight variants of matrix multiplication depending on transposition of each operand. For tensors, however, the number of possible types and combinations of transpositions is enormous. Additionally, it may not be possible to simultaneously guarantee stride-1 access in all operands if dimensions appear in different orders in two tensors. For example, in the contraction $C_{ijk} = \sum_{l=0}^{n-1} A_{jil}B_{lk}$ in column-major layout it is impossible to achieve stride-1 access in both $A$ and $C$ simultaneously.

Because of this complication, we order the dimensions within each bundle $I$, $J$, and $P$ heuristically. Additionally, while the dimensions are being processed, any dimensions of length 1 may be removed since the stride along these dimensions is meaningless. The heuristic steps employed are:

1) Remove any dimensions of length 1.
2) Sort the dimensions in $I$ and $J$ by increasing stride in $C$.
3) If $s_{j_0}^C = 1$, swap $A$ with $B$ and $I$ with $J$.
4) Sort the dimensions in $P$ by increasing stride in $A$.

The optimal ordering of dimensions to reduce the number of cache and TLB misses may differ from that achieved by the above heuristics, but these steps at least ensure that $C$ has $rs^C = 1$ if possible, enabling efficient updating in the micro-kernel, and ensure that $A$ has priority for stride-1 access over $B$ since it is packed more frequently.

The data layout and ordering of dimensions specified by the user can have a significant impact on performance for tensor contraction, since certain orderings may prohibit stride-1 access. As for matrices, ensuring that at least one stride in each tensor is unit is the simplest condition that the user can check for performance. However, there are several other guidelines for tensor layout which can aid in maximizing tensor contraction efficiency:

- Dimensions should be ordered the same in each tensor (or more generally, dimensions should have strides in each tensor which are ordered the same in magnitude).
- Dimensions should be mutually contiguous where possible. Alignment of the first leading dimension (the stride of the second dimension) may be influential on some architectures.
- The dimensions of largest size should have the shortest strides, and the dimension with stride 1 should especially be as long as possible.

Related work on explicit tensor transpositions (see for example [31]) may also provide a systematic way to optimize the ordering of tensor dimensions and help overcome inefficiencies in tensor layout.

D. Related Work

As mentioned previously, there are a variety of tensor-related packages available for popular programming platforms such as NumPy [33] for Python, the Tensor Toolbox [1] in MATLAB, the template libraries Eigen [13] and Blitz++ [37] in C++, among many others. These libraries provide a simple and intuitive interface for creating and manipulating tensors, for example providing traditional array-style access to individual elements, managing transposition and reshaping, etc. Tensor contraction facilities are provided in many of these.
libraries, either using explicit (although sometimes compiler-generated) loop-based code, or using the TTDT algorithm. In many applications this approach is sufficient, although the deficiencies of the TTDT approach outline above still apply, especially for high-performance code. Additionally, the quality of and interface provided for tensor operations varies significantly from library to library. It is our hope that the high-performance and self-contained (since it does not require large amounts of workspace) implementation provided by (B)SMTC can provide a standard level of performance and functionality.

Within specific scientific domains, high-performance libraries have appeared that implement the TTDT approach. For example, in quantum chemistry there are software packages such as the Tensor Contraction Engine (TCE) [18], Cyclops Tensor Framework [30], libtensor [10], and TiledArray [4], [5] that provide general tensor and in some cases specific quantum chemistry-related functionality. Many of these libraries could benefit directly from a native tensor tensor contraction kernel since they focus primarily on distributed-memory algorithms and tensor blocking for algorithmic and space efficiency. Other approaches such as Direct Product Decomposition (DPD) packing [22] are specifically focused on improving the efficiency of the TTDT approach, but could also be used on top of the (B)SMTC algorithm.

Other research has focused on improving the efficiency of the TTDT approach through optimization of the tensor transposition step (and other associated operations in quantum chemistry). Explicit searches of the space of tensor transpose algorithms along with code generation techniques has been used to generate high-performance tensor transpose kernels [31]. Tensor transposition along with handling of index permutation symmetry in the TTDT approach has been addressed specifically in the chemistry community [16], [15], [23].

One alternative to TTDT not previously discussed is the use of tensor slicing. In this approach, the dimensionality of each tensor in the contraction operation is successively reduced by explicitly looping over lower-dimensional tensor contraction sub-problems. When enough dimensions have been eliminated in this way, the inner kernel becomes one of the standard BLAS operations, although depending on which dimensions have been eliminated the inner kernel may be a level 2 (matrix-vector) or even level 1 (vector-vector) operation rather than matrix multiplication. Analysis of the resulting inner kernel can be used to optimally eliminate indices to produce an efficient algorithm [6], [27], while for certain contraction types performance modeling and auto-tuning have been used to generate efficient parallel implementations [22]. Tensor slicing has also been applied to tensor contraction on GPUs [24]. These approaches can also be considered native tensor contraction algorithms since they do not require explicit tensor transposition and may offer an alternative path to high-performance implementations; however we do not directly compare to tensor slicing since no standard approach or library has emerged for this approach.

V. RESULTS

A. Experimental Setup

All of the experiments performed were run on an Intel Xeon E5-2680 processor. This processor has a Sandy Bridge architecture supporting the AVX instruction set, which is taken advantage of in the BLIS sandybridge micro-kernel. The processor has eight cores with private 32KB L1 data and 256KB L2 caches, while the 20MB L3 cache is shared among all eight cores. The blocking parameters used were: \( m_R = 8 \), \( n_R = 4 \), \( m_C = 96 \), \( n_C = 4096 \), and \( k_C = 256 \) for double-precision elements, which is consistent with those used in BLIS. We compiled the BLIS micro-kernel and our own framework with the Intel Composer XE 2015 Update 2 compilers. Each experiment was run a number of times to warm the caches, and the run with the lowest time (highest performance) is reported. The multithreaded experiments used the Intel OpenMP runtime with threads pinned to their respective cores (single-threaded runs were pinned to an arbitrary core). All experiments were performed on double-precision data types. The unmodified BLIS library was used for all matrix multiplications, since it is directly comparable to our tensor contraction algorithms. BLIS was shown to achieve performance within a few percentage points of widely-used alternatives such as OpenBLAS [40], [38] and Intel Math Kernel Library (MKL) on similar processors [35], [34].

In each performance graph, the \( y \)-axis runs from zero to the peak theoretical performance for one core of the processor, running at the maximum Turbo Boost frequency. The peak performance at the base processor frequency is given by a black horizontal line. Since the Turbo Boost feature of newer Intel processors can produce highly dynamic performance properties, we attempted to control for this effect by running all of the experiments in our suite twice, and then reporting the numbers from the second run. This process should cause the processor to heat up sufficiently to bring the frequency down to near the base frequency, although as is evident in some graphs the peak performance at the base frequency is still exceeded in some cases.

B. Regular Tensor Contractions

As a well-structured yet non-trivial example of tensor contraction, we use the tensor contraction \( C_{abcd} = \sum_{e=0}^{n_a-1} \sum_{f=0}^{n_b-1} A_{abe} \cdot B_{cfed} \) stored in column-major order. This contraction does not have any contiguous dimensions in any of the \( J = ab, J = cd, \) or \( P = ef \) bundles, but does follow the guidelines above for an efficient tensor layout, since the dimensions \( a \) and \( e \) have stride 1 and the dimensions in each bundle appear in the same order in all tensors. The TTDT and (B)SMTC implementations of this tensor contraction were compared to matrix multiplication in the form \( C_{ij} = \sum_{p=0}^{n_e-1} A_{ip} \cdot B_{pj} \). In order to directly compare these two computations, we assign “effective” matrix lengths \( \hat{m} = n_a \), \( \hat{n} = n_j \), and \( \hat{k} = n_p \), and then assign tensor lengths \( n_b = n_d = n_f = 10 \) and \( n_a = \hat{m}/10 \), \( n_c = \hat{n}/10 \), \( n_e = \hat{k}/10 \), so that the number of FLOPs required for both
cases is the same ($2\tilde{m}\tilde{n}\tilde{k}$). In addition to comparing to matrix multiplication alone (referenced in the graphs as the “BLIS” algorithm), we also compare to matrix multiplication plus allocation of temporary matrices with copies of $A$ and $B$ before, and $C$ after multiplication, which we refer to as the “BLIS+copy” algorithm. This serves as an estimate of the upper-bound for TTDT performance since the speed of tensor transposition is inherently limited by the speed of a vector copy given the same optimizations. Results for sequential execution of BLIS, BLIS+copy, SMTC, BSMTC, and TTDT for various values of $\tilde{m}$, $\tilde{n}$, and $\tilde{k}$ are given in Figure 6.

From these results we can see that the cost of copying $A$, $B$, and $C$ in the BLIS+copy approach is between 5-10%. The tensor transpose is slightly more expensive, from 10-15%. The sawtooth shape to many of the curves (in particular TTDT) is probably due to alternate alignment and mis-alignment on a 32-byte boundary necessary for aligned AVX loads and stores. On the other hand, the SMTC algorithm either closely reproduces the performance of BLIS+copy or slightly out-performs it. Going to the BSMTC algorithm increases performance further, roughly halving the performance gap between BLIS and SMTC. While the performance penalty of tensor contraction relative to matrix multiplication is relatively small even for TTDT in these measurements, the SMTC and BSMTC algorithms offer uniformly improved performance without the workspace requirement or code complexity of TTDT.

C. Random Tensor Contractions

In addition to highly-regular tensor contractions as in the previous section, we also measured the performance of randomized tensor contractions. For each of the matrix multiplication problems examined in the previous section, we randomly generate three similarly-shaped tensor contractions. For each matrix dimension, we choose between one and three tensor dimensions for the corresponding bundle, where the product of the tensor dimensions is close to the original matrix dimension. In our algorithm, this gives a combined edge length within a factor of $2^{d/2}$ of the matrix length for $d$ corresponding tensor dimensions. The order of the dimensions in each tensor is then randomized. The effective matrix lengths for the random tensor contractions is determined by the lengths of a matrix multiplication of the corresponding shape requiring the same number of Flops. The performance results reproducing the BLIS and BLIS+copy data from above and adding measurements for these random tensor contractions computed with BSMTC and TTDT are given in Figure 7.

The performance of the BSMTC algorithm is similar to that for regular tensor contractions, generally out-performing BLIS+copy and averaging between BLIS+copy and BLIS. This is encouraging since the generated tensor contractions are often in opposition to the guidelines stated above. The TTDT algorithm in some cases performs as well as BLIS+copy, but has a much wider range of variability, averaging about 75% of the performance of BLIS and dropping as low as 50% efficiency. For both small and large problem sizes,
Figure 7. Performance of matrix multiplication and random tensor contractions on one core of a Xeon E5-2680 processor.

BSMTC significantly out-performs TTDT, although highly-optimized tensor transpose routines [31] may reduce some of the variability exhibited by the latter.

D. Parallel Performance

Our tensor contraction implementation also supports multithreading, and so we repeated the experiments from section V-B using all eight cores of the processor. Since our tensor transpose implementation is not parallelized, we focus on comparing the parallel efficiency of BLIS and BSMTC. The performance per core of these algorithms using one and eight cores is given in Figure 8.

For the “square” and “panel-panel multiply” shapes, the results on eight cores display a slower ramp-up than for one core, which is to be expected as the available parallelism at small sizes of \( \tilde{m} \) and \( \tilde{n} \) is limited. For the “rank-\( k \) update” shape, these dimensions are fixed at a large number and the parallel efficiency is similar across the range of \( \tilde{k} \) values. All of the examples show a maximum parallel efficiency of about 90% for BLIS and about 85% for BSMTC, although changes in processor frequency under heavy load may suggest a higher efficiency for a fixed processor frequency. The similarly high parallel efficiency of BLIS and BSMTC shows that the transformation from tensors to matrices is not a scalability bottleneck.

VI. SUMMARY AND CONCLUSIONS

We have presented two novel mappings from a general tensor data layout to a matrix layout, which allow for tensor elements to be accessed in-place from within matrix-oriented computational kernels. We have shown how kernels using these mapping within the BLIS approach to matrix multiplication produces new tensor contractions algorithms which we denote Scatter-Matrix Tensor Contraction (SMTC) and Block-Scatter-Matrix Tensor Contraction (BSMTC). These approaches achieve an efficiency uniformly higher than that of the traditional TTDT algorithm, approaching that of matrix multiplication using the BLIS framework. Our implementations of these algorithms also achieves excellent parallel scalability when using multithreading.

Since the SMTC and BSMTC approaches do not have any of the major drawbacks of TTDT: variability in performance, excessive workspace requirements, and complicated program logic in user applications in some circumstances, we conclude that these algorithms should be considered as high-performance alternatives to existing tensor contraction algorithms. The efficiency and simplicity of these algorithms also highlights the utility and flexibility of the BLIS approach to matrix multiplication.

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on eight cores of a Xeon E5-2680 processor.

Figure 8. Performance of matrix multiplication and regular tensor contraction on eight cores of a Xeon E5-2680 processor.

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