Quantum error correction (QEC) is essential for quantum computing to mitigate the effect of errors on qubits, and surface code (SC) is one of the most promising QEC methods. Decoding SCs is the most computational expensive task in the control device of quantum computers (QCs), and many works focus on accurate decoding algorithms for SCs, including ones with neural networks (NNs). Practical QCs also require low-latency decoding because slow decoding leads to the accumulation of errors on qubits, resulting in logical failures. For QCs with superconducting qubits, a practical decoder must be very power-efficient in addition to having high accuracy and low latency. In order to reduce the hardware complexity of QC, we are supposed to decode SCs in a cryogenic environment with a limited power budget, where superconducting qubits operate.

In this paper, we propose an NN-based accurate, fast, and low-power decoder capable of decoding SCs and lattice surgery (LS) operations with measurement errors on ancillary qubits. To achieve both accuracy and hardware efficiency of the SC decoder, we apply a binarized NN. We design a neural processing unit (NPU) for the decoder with SFQ-based digital circuits and evaluate it with a SPICE-level simulation. We evaluate the decoder performance by a quantum error simulator for the single logical qubit protection and the minimum operation of LS with code distances up to 13, and it achieves 2.5% and 1.0% accuracy thresholds, respectively.

I. INTRODUCTION

Quantum computers (QCs) are becoming an attractive computing paradigm as the number of implementable qubits increases because of their potential to solve meaningful quantum algorithms. One of the most important challenges to practical quantum computation is the fragility of qubits. As quantum error correction (QEC) is the unique method to reduce the effective error rate of quantum gates in a scalable manner, it has been extensively studied so far [1–5]. QEC codes encode fault-tolerant logical qubits by using a set of multiple faulty physical qubits. Surface code (SC) [3] is a promising candidate in practical QEC coding schemes. SC is implemented on a square grid of qubits and only requires interactions between geometrically adjacent physical qubits. These features simplify the hardware implementation and provide high reliability in QEC. The decoding procedure is known to be a non-trivial task and requires a large amount of computational cost in classical computers.

In order to achieve a practical fault-tolerant quantum computation (FTQC), we need an SC decoder that satisfies the following three requirements: accuracy, latency, and scalability. The accuracy requirement indicates that the decoder must estimate both errors on physical qubits and measurement processes with high probability. The latency requirement indicates that the decoder should correct errors within a QEC cycle to prevent the accumulation of errors. The scalability requirement indicates that the decoder must support hundreds of logical qubits with interactions between them[5, 6]. Thus, the QEC coding/decoding schemes should be optimized in algorithmic and implementation perspectives to meet all requirements.

When targeting superconducting QCs, practical decoders must also satisfy a power requirement. A superconducting quantum circuit is one of the most promising QC implementations [7, 8], and state-of-the-art superconducting QCs have over 100 qubits. They are operated in a cryogenic environment with an effective temperature of around ten milliKelvins to eliminate thermal noises in the device. While we place the qubits at the milliKelvin stage of a dilution refrigerator, the associated control electronics, including a QEC decoder, are supposed to be located at a higher temperature stage or outside the cryostat[9]. The spatial distance between the components demands many cables between different temperature stages, leading to the hardware complexity in wiring and latency in QEC. This point hinders scaling up QCs. Although the QEC processing unit right next to the qubit chip alleviates this problem [10], it is usually unrealistic under the restricted power budget in the lower temperature stages of a cryostat (e.g., tens of µW or around 1 W in the millikelvin stage or the 4-K stage, respectively). Therefore, an extraordinary low-power decoder is necessary.

In the decoding process of SCs, many works have proposed accurate decoding algorithms such as minimum weight perfect matching (MWPM) [11], union find...
(UF) [12], and renormalization group (RG) [13]. These software-based decoders guarantee a polynomial-time solution; however, they are slow and not hardware efficient due to their high computational cost and do not meet the latency and power requirements. Several fast and low-cost decoding algorithms and their hardware-efficient implementations [12, 14–18] have been proposed to reduce the computational burden. In particular, the previous works based on a greedy matching algorithm and high-speed and low-power superconducting digital circuits [15, 16, 18] operate in a cryogenic environment to alleviate wires between superconducting qubits and satisfy the latency and power requirements. Among them, the QULATIS decoder [18] also meets the scalability requirement because it supports lattice surgery (LS) [6]. However, while these decoders have the desirable properties previously described, their decoding accuracy is lower than that of software decoders due to their greedy nature.

For the last several years, researchers have studied neural network (NN) techniques for decoding SCs [19–25]. Generally, the performance of NN-based decoders is expected to be superior to that of conventional software decoders, such as MWPM or UF because they can incorporate the correlation between X- and Z-errors into decoding SCs. In addition, several works proposed methods of constructing an accurate and scalable decoder by combining NNs with other decoders [23–25]. However, all previous NN-based decoders do not meet the latency and power requirements.

In this paper, we propose a new neural network based decoding scheme called Neural network Enhanced Online Quantum Error Correction (NEO-QEC) that meets the four requirements required for superconducting QCs. We extend the previous NN decoder based on convolutional neural networks (CNNs) [25] and combine it with the superconducting-digital-circuits-based decoders [16, 18]. We aim to design a decoder based on the algorithm to achieve the following features simultaneously:

1. Improved error correction performance.
2. Low latency to prevent the accumulation of errors.
3. Capability for decoding three-dimensional (3-D) complex SC lattices to handle LS with measurement errors.
4. Power efficiency suitable for operation in a cryogenic environment.

There are many problems in satisfying the latency and power requirements for NN-based decoders because NNs generally require heavy computational resources. To design a fast and low-power NN decoder, we use quantization [20] or binarization [27] techniques.

The contributions of this paper are summarized as follows:

- We propose the NEO-QEC decoding algorithm that is capable of LS with measurement errors by combines NNs and existing decoders.
- We use a binarization technique to implement a lightweight NN decoder with moderate accuracy degradation.
- We evaluate the error correction performance of the NEO-QEC by a quantum error simulator.
- We design an ultra-low-power and fast neural processing unit (NPU) with superconducting digital circuits and evaluate its performance with a SPICE-level simulator.

The remainder of the paper is organized as follows: we begin with a background of this paper in Section II. Then, we show an overview of prior NN-based decoders and superconducting-digital-circuits-based decoders in Section III. In Section IV, we describe our new decoding algorithm. In Section V, we show the superconducting circuit design of the NPU. We then show the evaluation results of our decoder performance in Section VI and conclude the paper with future works in Section VII.

II. BACKGROUND

A. Surface code

Surface code (SC) [4, 28] is one of the most promising QEC codes; SC can reduce logical errors effectively and be implemented simply with physical operations on geometrically adjacent qubits located on a two-dimensional (2-D) grid. SC consists of two types of physical qubits: data and ancillary. Data qubits are used to represent a logical qubit. Ancillary qubits are utilized to check the parity of errors on the neighboring data qubits. This parity check is called a stabilizer measurement, and its binary outcome is called a syndrome value.
To deal with both bit-flip (Pauli-$X$) and phase-flip (Pauli-$Z$) errors, QEC needs two types of stabilizer measurement: $X$ and $Z$. $X$- and $Z$-stabilizer measurements can detect the Pauli-$Z$ and -$X$ errors on the neighboring data qubits, respectively. Note that Pauli-$Y$ errors are considered to be a combination of bit- and phase-flip errors because the Pauli operators $X$, $Y$, and $Z$ have the following relationship: $Y = iZX$. Fig. 1(a) shows a schematic picture of the SC with code distance $d = 3$. Here, data and ancillary qubits for $X$-(Z-) stabilizer measurements are represented as circles and blue (red) squares, respectively. $X$-(Z-) stabilizer measurements detect Pauli-$Z$(-$X$) errors when the corresponding parity of the neighboring qubits is odd.

The decoding process of SCs is to estimate errors on physical qubits from outcomes of stabilizer measurements and commonly reduced to the following MWPM problem [5]. Suppose a 2-D grid graph where its nodes and edges correspond to the syndrome values and data qubits, respectively. An example is shown in Fig. 1(b), where erroneous data qubits are represented as red edges, and detected syndromes are represented as nodes with red rims. The two lattices for $X$- and $Z$-stabilizer measurements have two distinct boundaries: smooth and rough boundaries, respectively. We construct a weighted complete graph where its nodes correspond to the detected syndromes or boundaries, and the weights of its edges are determined from the noise model. We find an MWPM of the complete graph, and the estimated errors are represented as edges between each pair of syndromes of the matching. Error estimation success is determined by the properties of the occurred and estimated errors. If we estimate errors as a perfect matching, the resultant error chain consists of topologically trivial and non-trivial chains, as shown in Fig. 1(c). The odd number of non-trivial chains indicates the failure of error estimation.

Even when ancillary qubits also suffer from noise, we can reliably estimate errors by extending the decoding task to a 3-D lattice, i.e., by considering stacked 2-D snapshots as shown in Fig. 1(d). A procedure to generate a 2-D snapshot is called a code cycle. A practical decoding algorithm must be capable of decoding these sequentially captured 2-D snapshots every code cycle.

### B. Lattice surgery

During the computation, we need to perform a universal set of logical gates (Hadamard, CNOT, and $T$-gates) on logical qubits. While logical Hadamard gates are straightforwardly implementable, the implementation of logical CNOT and $T$-gates only with neighboring physical operations is not trivial. The lattice surgery (LS) technique enables us to efficiently implement these two logical gates [6].

LS provides a way to implement logical Pauli measurements on multiple logical qubits via the following merge-and-split operations. The minimum example of the LS, a logical Pauli-$XX$ measurement on two logical qubits, is shown in Fig. 2. In this figure, (Step 1) we initialize all the sandwiched physical qubits to physical $|0\rangle$ states, (Step 2) two surface codes are merged by performing another set of stabilizer measurements and repeating them for $d$ code cycles, and (Step 3) split the merged codes into two planes by performing the original stabilizer measurements and measure all the sandwiched physical qubits on Pauli-$Z$ basis. These operations are known to be equivalent to a logical Pauli-$XX$ measurement on the two logical qubits. The outcome of the logical Pauli measurement is calculated from the parity of the outcomes of Pauli-$X$ stabilizer measurements in the first cycle of LS. Since this procedure merges two rough boundaries, this operation is called a rough merge. The Pauli-$ZZ$ measurement can also be achieved in a similar way by merging smooth boundaries. Note that a logical CNOT operation can be achieved through logical Pauli-$XX$ and Pauli-$ZZ$ measurements and feedback of logical Pauli operations; hence, the logical CNOT operation is implemented with two merge-and-split operations. In addition, a logical $T$-gate can be efficiently implemented with LS and gate teleportation with magic states. See Refs. [29, 30] for details of this formalism.

During the merge-and-split operations for rough boundaries, we obtain a stacked 2-D lattice to be decoded, as shown in the left side of Fig. 2. As in the case of the figure, a Pauli error connecting a boundary to another distinct one with the same color is undetectable with stabilizer measurements and modifies the logical states or flips the result of the logical measurement. We keep $d$ code cycles during the merge phase since the distance between two U-shaped red boundaries corresponds to the code cycles during the merge.

### C. Single Flux Quantum logic

A single flux quantum (SFQ) logic [31] is a pulse-driven digital circuit composed of superconductor devices. It is one of the most practical technologies with the poten-
Information processing in SFQ circuits is performed with magnetic flux quanta stored in superconductor rings; the presence or absence of an SFQ in the ring represents a logical ‘1’ or ‘0’, respectively. In SFQ circuits, an SFQ is stored or transferred using Josephson junctions (JJs) in the ring; the JJ has a “superconductor–insulator–superconductor” structure, as shown on the right side of Fig. 3(a). JJs in the ring act as a switching device similar to transistors in ordinary CMOS circuits. Figure 3(b) shows the equivalent circuit diagram of the superconductor rings with JJs shown in Fig. 3(a). The inductors and cross marks represent superconductor parts of the ring and JJs, respectively. The circle with a cross means an SFQ stored in the superconductor ring. Multiple rings connected in series form a Josephson transmission line (JTL), a type of SFQ wiring.

Figure 3(c) shows the transmission of an SFQ on a JTL. In step (1) of Fig. 3(c), an SFQ is stored in the left ring and generates a circulating current in the ring. The sum of the circulating current of the SFQ (green arrow) and bias current (blue arrow) exceeds the critical current $I_C$ of the left JJ. In step (2), the left JJ is switched, and the SFQ moves to the next ring. Then, the central JJ is similarly switched, and the SFQ moves to the right ring in step (3).

Figure 3(d) shows the electrical characteristic of the JJ in the red circle of Fig. 3(c). In step (1) of Fig. 3(c), only the bias current flows in the JJ, and it is smaller than the critical current $I_C$. In steps (2) and (3), the sum of the circulating current and bias becomes greater than $I_C$. Then, the JJ is switched. While switching, the voltage of the JJ becomes zero, and it generates an impulse-shaped voltage pulse named an SFQ pulse, as shown on the right side of Fig. 3(d).

An SFQ pulse has a quantized area $\Phi_0$, which is established by the following formula:

$$\int V(t)dt = \Phi_0 \approx 2.07 \times 10^{-15} \text{ Wb}.$$  \hspace{1cm} (1)

The typical width and height of the SFQ pulse are a few picoseconds and a few hundred microvolts, respectively, as shown in Fig. 3(d). The signal transmission based on SFQ pulses releases the SFQ circuits from the charging/discharging process required for the signal transmission of CMOS circuits, and it enables SFQ circuits to perform ultra-fast and low-energy information processing.

In the RSFQ circuit, the power consumption is calculated as follows:

$$(\text{RSFQ power consumption})_{[W]} = (\text{Bias voltage})_{[V]} \times (\text{Bias current})_{[A]}.$$  \hspace{1cm} (2)

Most of the power of the RSFQ circuit is consumed statically, almost independent of the switching activities of JJs.

ERSFQ is a promising technology that completely excludes the static power dissipation of RSFQ. In ERSFQ, bias resistors are replaced with JJs, by which we can eliminate the large static power consumption in exchange for doubled dynamic power consumption by JJs. Because the JJ’s dynamic energy consumption is roughly represented by bias-current × $\Phi_0$ per switch, we can estimate the power consumption of ERSFQ on the basis of the bias current of RSFQ logic design and the power model of ERSFQ as follows:

$$(\text{ERSFQ power consumption})_{[W]} = (\text{Bias current})_{[A]} \times (\text{Frequency})_{[Hz]} \times \Phi_0 [\text{Wb}] \times 2.$$  \hspace{1cm} (3)

III. RELATED WORKS

A. Online decoder with SFQ circuits

Cryogenic computing, such as SFQ and Cryo-CMOS, has been actively studied to design peripherals of QC...
controllers [10, 15, 36]. Holmes et al. [15] proposed an algorithm named approximate quantum error correction (AQEC) where they devised a power-efficient and high-speed SFQ-based decoder for SC. Their implementation consists of multiple units corresponding to each data and ancillary qubit of an SC logical qubit to detect and correct errors by propagating simple signals between the units with a distributed processing scheme. Their implementation is capable of correcting Pauli errors on the data qubits. In 2021, we proposed the QECOOL decoder, an extension of AQEC to deal with measurement errors of ancillary qubits [16]. We implemented an SFQ-based decoder that achieves a lower power consumption than AQEC. Furthermore, we proposed the QULATIS [18] decoder by extending the QECOOL to deal with LS [6].

To cope with the measurement error, we also proposed the concept of online-QEC, where the stabilizer measurements and decoding processes are performed simultaneously, in contrast to the conventional batch-QEC, where the decoding process is done after all the measuring processes. The vast amount of error information in batch-QEC makes QEC latency worse, which causes errors to accumulate. Moreover, batch-QEC requires a large amount of memory to store error information proportional to the cube of code distance, which leads to decoders with a large hardware cost. By contrast, online-QEC uses part of a syndrome lattice to decode SCs. Therefore, it has the potential to be fast enough to avoid error accumulation and requires only a constant amount of memory independent of code distance. Our previous SFQ-based decoders [16, 18] used the online-QEC technique; however, due to their greedy nature and inability to process the entire 3-D syndrome lattice, they have lower accuracy than that of software decoders such as MWPM and the hardware efficient decoder based on the UF algorithm [17]. Therefore, we extend the previous SFQ-based decoders with NNs to build a lightweight and high-performance online decoder with SFQ circuits in this paper.

B. Neural network-based decoders

Decoders for SCs and other topological codes using NNs are widely studied and expected to achieve a near-optimal decoding performance by utilizing the correlation between Pauli X- and Z-errors [14, 20, 23, 25, 37, 39]. When NN-based decoders were first proposed, many approaches trained NNs to predict the most probable physical errors or the required recovery operation for input syndrome values [14], and we refer to these approaches as end-to-end NN decoders. However, generally, the result of a recovery operation inferred by end-to-end NN decoders is not necessarily a codeword. In addition, it has been reported that these end-to-end approaches are not scalable because the problems become more complex as the code distance increases, rendering training NNs more difficult [23, 25].

In contrast to end-to-end NN decoders, several studies use NNs combined with other decoding algorithms to build a hierarchical decoder [22, 25, 40]. These approaches use NNs at the first stage to correct small distance errors by a part of a syndrome lattice, and remaining long-distance errors are corrected with a conventional decoding algorithm, such as MWPM or UF, at the second stage. The second-stage decoder guarantees that its output is a codeword. In addition, the size of the syndrome input to NNs is small, independent of code distance, which keeps NNs size constant and their training easy. We call these approaches two-stage NN decoders.

Meinerz et al. [23] proposed a two-stage NN decoder that combined a fully-connected NN decoder with a UF decoder that focuses on decoding problems of 2-D and 3-D Toric Code [3]. The decoding process of Toric code is similar to that of SC except for the boundary condition of logical qubits. Their work achieved scalability and high accuracy by dividing the decoding process into two stages: NN preprocessing for local error corrections and longer-range error corrections with the UF decoder. For the 2-D (3-D) Toric code, the X- and Z-syndromes within the square (octahedral) L on a side surrounding a certain data qubit are input to the NN decoder in the first stage, where L is a constant independent of code distance d. The NN decoder outputs the most probable error among \{I, X, Y, Z\} on the central data qubit of the square (octahedral). This procedure is performed for all data qubits, and the error chains smaller than L are expected to be corrected. The remaining errors are corrected in the second stage with the UF decoder.

Gicev et al. [25] also proposed a two-stage NN decoder that combined an NN with a hard-decision renormalization group (HDRG) decoder [41]. They focused on decoding SCs under depolarizing noise on data qubits without measurement errors of ancilla qubits. Although their approach is similar to the previous one by Meinerz’s group [23], the NN used in the first stage is different; their NNs consist of only convolutional layers, whereas those of Ref. [23] have only fully-connected layers. Figure 4 shows the overview of their NN-based decoder for 2-D SCs with an example of code distance d = 3. As shown in the figure, their NN decoder consists of several convolutional layers. The fully convolutional decoder uses a four-channel input with binary values; the first two channels correspond to the X- and Z syndromes, and the last two channels correspond to the X- and Z- boundary information. The input value of 1 represents a hot syndrome or a boundary data qubit, as shown in the example of Fig. 1. They explicitly use boundary information of logical qubits as input of NNs, which leads to the robustness of the NNs to boundary changes, including LS [6] and braiding [5]. The decoder has several hidden convolutional layers between the input and output layers. The output shape of each layer is set to the same shape as the input except for channel numbers. The output layer is a convolutional layer with two kernels, and its activation function is a sigmoid function, whose re-
IV. NN-BASED TWO-STAGE DECODER

In this section, we propose the NEO-QEC algorithm by extending the QECOOL and QULATIS decoders with the existing NN-based two-stage decoder [25]. We construct the first stage NN-based decoder with the decoding capability for 3-D SC lattices by extending the previous work [25] and use the QECOOL or QULATIS as the non-NN decoder in the second stage.

A. Construction of NN-based decoder for 3-D SCs

Figure 4. Overview of the NN decoder of the previous work [25].

Figure 5. Overview of our NN-based decoder.

We extend the NN decoder of the previous work [25] to handle measurement errors. Figure 5 shows an overview of our NN-based decoder for 3-D SCs with an example of code distance $d = 3$.

Decoding SCs with measurement errors requires measuring ancilla qubits multiple times and stacking each result temporally to create a 3-D SC lattice. To simplify the process of the NN decoder, we train the NN to infer errors on a specific layer (called the target layer) on the 3-D syndrome lattice rather than the entire 3-D lattice. We introduce an integer parameter $K$, which represents the number of layers of the syndrome lattice used as an input for the NN decoder. In other words, the input of the NN decoder is a $K$-layer syndrome lattice that includes the target layer as the lowest layer. In addition, the input includes the boundary information of the target layer, similar to the previous study [25], resulting in a $2K + 2$ channel input. The decoder is a fully convolutional network with several hidden layers, and each convolutional layer has several constant-size kernels independent of code distance $d$. Its output has four channels, and each channel corresponds to $X$- and $Z$-errors on data qubits and measurement errors on $X$- and $Z$-ancilla qubits, respectively. Table I summarizes the differences between our method and that proposed in the previous study [25]. Note that our NN decoder is capable of processing 3-D SC lattices with various code distances and shapes.
Table I. Comparison of NEO-QEC and the method proposed in the previous work [25].

| Lattice | Meas. error | Input channels | Output channels |
|---------|-------------|----------------|----------------|
| Previous work [25] | 2-D SC | No | 4 | 2 |
| NEO-QEC (this work) | 3-D SC | Yes | 2K + 2 | 4 |

infer errors on a target layer and does not have to wait until all measurement processes are performed, which is suitable for online-QEC as explained in Section IV C.

B. Binarization of NN-based decoder

In general, NNs require heavy computational resources. Therefore, many techniques, such as knowledge distillation [12] or pruning [13], are proposed to develop fast and lightweight NNs with slight accuracy degradation. Quantization is a technique that converts 64- or 32-bit floating numbers in the model parameters of NNs to 8-bit integers or lower bitwidth representations [26]. This technique enables for compact NN models and has shown tremendous and consistent success in implementing high-speed and low-power NNs [14].

Binarization of NNs is the most extreme quantization method, where 1-bit values represent both weights and input data of NNs [27, 45–47], thereby drastically reducing the memory requirement compared with floating-point representations. In addition to the memory space advantages, binary (1-bit) operations can often be computed efficiently with bit-wise arithmetic and achieve significant acceleration.

In XNOR-net [27], one of the implementations of binarized NNs, the costly floating-point multiplications on NNs are replaced with lightweight XNOR operations followed by bit counters. XNOR-net requires binarization of input data and model parameters, which generally leads to significant accuracy degradation. However, since each element of input and output in the proposed NN decoder is originally binary data, the effect of binarization on accuracy is expected to be less significant. In this work, we implement an NN decoder with XNOR-net-based binarized convolutional NN.

C. Online decoding with NN decoder

We combine the NN decoder with the QECool or QULATIS decoder as the NEO-QEC decoder architecture for online SC decoding. Figure 6 shows the workflow of our NEO-QEC decoder. Note that the second-stage decoder is not limited to QECool and QULATIS, and any online SC decoders are suitable.

We explain the online decoding workflow of the NEO-QEC algorithm as follows. The SC measurement process is repeated at a specific interval, and syndrome values are extracted every code cycle to build an SC lattice until the logical measurement. Suppose that the bottom layer of the lattice is set to the target layer as shown in Fig. 6. After the first K times measurement, the syndrome values for K layers of the syndrome lattice and the boundary information of the target layer are input to the NN decoder. The NN decoder infers errors on the target layer, and we update the syndrome of the target layer and the Pauli frame [48] on the basis of the inferred recovery operation as shown in the figure. The updated syndrome values are saved in the buffer of the second-stage decoder. After the subsequent measurement, the target layer is changed to the next layer from the previous one, and the same aforementioned procedure is performed. Then, the buffer of the second-stage decoder stores the updated syndromes of the first and second layers. After the aforementioned procedure is repeated several times, if the second-stage decoder stores sufficient syndrome layers to perform online decoding, e.g., the number of syndrome layers exceeds the threshold value denoted as $t_{th_1}$ in QECool or QULATIS, the second-stage decoder decodes the stored syndrome values; otherwise, the second-stage decoder waits for the completion of the NN decoder process. Thus, the second-stage decoder perform with a $K$-cycles delay for the NN decoder.

To achieve online processing of the whole architecture of NEO-QEC, the processing times of both NN and the second-stage decoders for a single layer of the SC lattice must be less than the code cycle (e.g., approximately 1 μs for a QC with superconducting qubits).

Figure 6. Workflow of the NEO-QEC decoder.

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1 The basic idea of Pauli frames is to track error correcting operations represented by Pauli gates as classical information rather than applying them to physical qubits by leveraging the fact that error correcting operations are commutative with logical Pauli and Clifford operations.
V. HARDWARE IMPLEMENTATION

In this section, we design a neural processing unit (NPU) with SFQ digital circuits. Although several SFQ arithmetic units supporting floating-point operations have been proposed [27–29], they consume a large amount of power. Thus, NPUs with floating-point operations are not suitable for the NEO-QEC decoder. As described in Section IV B, the binarization technique based on XNOR-net [27] is an effective approach in this study because of its simple structure consisting of SFQ-friendly bit-wise arithmetic. Therefore, we design an NPU based on XNOR-net.

A. XNOR-net-based NN with SFQ logic

Figure 7 (a) shows an example of an XNOR-based convolutional layer. Here, inputs, weights, and activation values are represented by 0 or 1, while the original work uses -1 or 1 [27]. Multiply-and-add operations to calculate activation values are replaced with “XNOR-and-add operations”, where the activation value is 1 if the majority of the XNOR results are 1, and 0 otherwise.

Figure 7 (b) illustrates an SFQ implementation of an XNOR-net-based convolutional calculation with the example of (a). As shown in the figure, binarized input and weight values are converted to bit-serial pulse trains where the absence and presence of a pulse at each time interval represent 0 and 1, respectively. The NPU receives pulse trains of input and weight values and outputs a pulse if the activation value is 1.

B. Design of NPU with SFQ circuit

As shown in Fig. 8, our SFQ-based NPU consists of an XNOR arithmetic unit and k-bit binary counter. The detailed descriptions of the submodules are as follows.

1. XNOR arithmetic unit: The XOR gate receives pulses representing input data and NN weight simultaneously. The negation of its output is used as the input signal of the k-bit binary counter. Note that the XNOR arithmetic unit outputs “XNOROut” with one cycle delay to the inputs because all the SFQ logic gates used in the XNOR arithmetic unit are clocked gates.

2. k-bit binary counter: The k-bit binary counter consists of k T flip-flops (TFFs) and one D flip-flop (DFF) connected in series and counts the number of “XNOROut” pulses from the XNOR arithmetic unit to calculate the activation value. The DFF holds the output pulse of $B_{k-1}$ and sends it as “ActivationValue” after receiving the “Readout” pulse. Note that the initial value of the counter must be adjusted so that $B_{k-1}$ outputs a pulse after the counter receives half of the total number of input pulses.

The bit length $k$ of the binary counter is determined by the maximum number of XNOR operations in a convolutional operation to be performed; the binary counter must be sufficiently large to count half the number of XNOR operations in a single convolution operation. In this paper, we target small- and medium-scale CNNs and evaluate decoder performance on the basis of the NPU with a 9-bit binary counter.

C. NPU implementation based on RSFQ logic

We designed the NPU with a 9-bit binary counter based on an RSFQ cell library [54] developed for a niobium nine-layer, 1.0-µm fabrication technology [55, 56]. Table II summarizes the SFQ logic gates used in this paper. Because the essential element of SFQ that affects power consumption and hardware cost is the JJ, Table II

| Cell   | JJs | Bias current (mA) | Area ($\mu$m²) | Latency (ps) |
|--------|-----|-------------------|---------------|--------------|
| DFF    | 6   | 0.720             | 900           | 5.1          |
| TFF    | 13  | 1.085             | 3600          | 6.5          |
| XOR    | 11  | 1.068             | 3600          | 6.5          |
| NOT    | 11  | 0.848             | 3600          | 6.5          |
Table III. Total number of logic elements, number of JJs, and latency of each XNOR-net-based NPU \[27\] based on the AIST 10-kA/cm² ADP cell library \[54\].

| Cell   | Binary counter (9-bit) | XNOR arithmetic unit | Total (9-bit) |
|--------|------------------------|----------------------|---------------|
| DFF    | 1                      | 1                    | 1             |
| TFF    | 9                      | 9                    | 9             |
| XOR    | 1                      | 1                    | 1             |
| NOT    | 1                      | 1                    | 1             |
| Total JJs | 123                  | 28                   | 151           |
| Total bias current (mA) | 7.99                  | 3.23                 | 11.2          |
| Latency (ps) | 6.5                  | 7.3                  | 13.8          |

shows the number of JJs for each gate and the bias current required for operation. The operating temperature and designed supply voltage are 4-K and 2.5 mV, respectively.

We used the Josephson simulator (JSIM) \[57\], a SPICE-level simulator, to verify the functionality of the designed NPU with a 9-bit binary counter and evaluate its latency. Table III shows the total number of JJs, total bias current, and latency of each submodule. The NPU consists of 151 JJs in total, and its total bias current is 11.2 mA. The maximum delay of the designed circuit is 13.8 ps, resulting in a maximum operating frequency of approximately 70 GHz. Note that Tab. III shows the design results before detailed routing and does not include the wiring cost. Therefore, the power consumption and delay are estimated to be lower than the actual circuit to be designed.

VI. EVALUATION

A. Evaluation setup

In this section, we numerically evaluate the QEC performance of the NEO-QEC algorithm for single logical qubit protection and an LS procedure. We assume a depolarizing noise model, where Pauli-\(X\), -\(Y\), and -\(Z\) errors occur on each data and ancillary qubit independently in each QEC cycle, which is called the phenomenological noise model. Since a Pauli-\(Y\) error is considered as the combination of Pauli-\(X\) and -\(Z\) errors, there is a correlation between decoding Pauli-\(X\) (bit-flip) and Pauli-\(Z\) (phase-flip) errors.

We repetitively sample error patterns for a given physical error rate, simulate the propagation of errors and decoding procedure, and evaluate the probability of logical failures. Although a complete simulation of quantum circuits requires time that scales exponentially with the number of qubits, we can efficiently simulate the propagation of Pauli errors because we assume Pauli errors and QEC circuits consist of Clifford gates and Pauli measurements \[58\].

| Parameter                  | Configuration |
|---------------------------|---------------|
| Epochs                    | 100           |
| Training dataset size \(N_{\text{train}}\) | Idling: \(1 \times 10^6\), LS: \(2 \times 10^5\) |
| Validation dataset size \(N_{\text{val}}\) | \(1 \times 10^5\) |
| Training error rate \(p_{\text{train}}\) | Idling: 0.04, LS: 0.006 |
| Training lattice size \(d_{\text{train}}\) | 9 |
| Input syndrome layers \(K\) | 3, 4, 5 |
| Input layer shape \((C, H, W)\) | \((2K + 2d_{\text{train}} - 1, 2d_{\text{train}} - 1)\) |
| Output layer size \((C, H, W)\) | \((4d_{\text{train}} - 1, 2d_{\text{train}} - 1)\) |
| \# of total conv layers | 2, 3 |
| \# of hidden layer channels | 9, 16 |
| Kernel size | \(5 \times 5, 5 \times 7\) |
| Optimizer | ADAM |
| Learning rate | FP32: 0.01, BNN: 0.001 |
| Loss function | Binary cross-entropy |

B. Training

We use standard supervised learning techniques to train NNs consisting of two or three convolutional layers for single logical qubit protection or an LS procedure, and the training parameters are shown in Tab. IV. As explained in Section IV, we use \(K\) layers of a SC syndrome lattice and \(X\)- and \(Z\)-boundaries information of the target layer as input data, which consists of \(2K + 2\) channels. We use error information of each data qubit and measurement process on the target layer as label data. For the idling operation of a single logical qubit, the training data set is generated by simulating a depolarizing noise model with error probability \(p_{\text{train}}\) on a distance-\(d_{\text{train}}\) SC during \(d_{\text{train}}\) code cycles. For the merge-and-split operation, we generate the training data set by simulating the merge-and-split operation with two distance-\(d_{\text{train}}\) logical qubits during \(3d_{\text{train}}\) code cycles. In other words, the pair of input and label data is generated by performing the opposite operation of decoding, where the syndrome values are calculated from the randomly provided physical error information. This procedure is performed very efficiently, and we can create a large dataset to reduce the chance of overfitting. Note that NN structures are common for the two different tasks of single logical qubit protection and LS, while the training data sets are generated for each task. The starting learning rate is shown in Tab. IV, and we decrease it exponentially during training, and its schedules are optimized by hand. The NNs are built with the PyTorch v1.8 platform \[59\].

C. NN-based decoder

First, we show the error correction performance of the NEO-QEC algorithm for the idling operations of a single logical qubit during \(d\) code cycles assuming the existence of measurement errors and compare it with the existing decoding algorithms. Here, the NNs of NEO-QEC are trained with 32-bit precision, and no quantization technique is used.

Table V shows the accuracy of NEO-QEC with vari-
ous configurations of the NN decoder. Compared with the QECOOL, pseudo thresholds of NEO-QEC improve in all cases verified here. Although the parameter size of the NN decoder varies widely depending on the configuration of the NN, a large NN decoder does not necessarily achieve high performance. We chose the NN configuration with the best balance between the number of total parameters and performance as the base model.

Figure 9 (a) shows the results of NEO-QEC with the baseline NN of Tab. IV (solid lines), QECOOL (dotted lines), and MWPM (dash-dot lines). The performance of the NEO-QEC is still low compared with MWPM, which is a software-based decoder with a batch-processing manner. The NEO-QEC performance is higher than that of the original QECOOL for any code distance \(d\). The pseudo threshold values, which represent intersections of each plot and break-even line, improve by 70% compared with those of the QECOOL. In addition, the threshold value of NEO-QEC is \(p = 2.5\%\), whereas those of MWPM and QECOOL are 4.5% and 1.5%, respectively.

Next, we show the performance of the NEO-QEC algorithm for merge-and-split operations on two logical qubits described in Fig. 2. Figure 9 (b) shows the results of NEO-QEC with the baseline NN for the LS procedure. The NEO-QEC performance is higher than that of the QULATIS decoder for any code distance \(d\), and the pseudo threshold values improve by 3 to 13 times compared with QULATIS. The threshold values of NEO-QEC, QULATIS, and MWPM are 1.0%, 0.6%, and 2.0%, respectively.

D. Binarized NN decoder

In this subsection, we demonstrate the performance of the NEO-QEC with a binarized NN. The QEC workload is the same as that in the previous subsection. We evaluate the error correction performance of NEO-QEC when XNOR-net-based binarization[27] is used. Figure 9 (a) compares the performances of the NEO-QEC with FP32 and XNOR-net-based binarized NNs (solid and dashed lines, respectively) and QECOOL (dotted lines) for the idling operations of a single logical qubit. The base model NN decoder of Tab. IV is used for both FP32 NEO-QEC and binarized NN. The performance of the NEO-QEC with the binarization techniques is better than that of the original QECOOL for any code distance \(d\), and its degradation is moderate compared with FP32. The threshold value of NEO-QEC with binarized NN is \(p = 2.3\%\), whereas that of FP32 NEO-QEC is 2.5%.

Figure 9 (b) shows the result of the binarized NEO-QEC and QULATIS for LS. The results have the same trend as in the case of single logical qubit protection; the threshold values of NEO-QEC with FP32 and binarized NNs are approximately equal at 1.0%, and the pseudo threshold values are slightly degraded due to binarization.

E. Estimation of computational cost for NN-based decoder

In this subsection, we estimate the computational cost of the NN decoder for the case of a single qubit operations. The number of multiplications per convolutional layer \(M_{\text{conv}}\) is calculated as follows:

\[
M_{\text{conv}} = (\text{kernel size})^2 \times (\text{input channels}) \times (\text{output channels}) \times (\text{output size})^2.
\]

Then, we estimate the number of multiplications required for one inference of the base NN model in the case of code distance \(d\) as follows.

- (1st layer) \(7^2 \times 10 \times 16 \times (2d - 1)^2 = 7840(2d - 1)^2\),
- (2nd layer) \(5^2 \times 16 \times 16 \times (2d - 1)^2 = 6400(2d - 1)^2\),
- (3rd layer) \(5^2 \times 16 \times 16 \times (2d - 1)^2 = 1600(2d - 1)^2\),
- (Total) \((7840 + 6400 + 1600)(2d - 1)^2 = 15840(2d - 1)^2\).

Therefore, sufficient number of NPUs are required to perform \(15840(2d - 1)^2\) multiplications within 1 \(\mu s\) for online decoding.

Here, we assume an NN decoder architecture consisting of \((2d - 1)^2\) NPUs and estimate the power consumption of the decoder. Because the process of a convolutional layer can be easily parallelized, the required throughput for each NPU is 15840 multiplications per 1 \(\mu s\) with the architecture. Hence we assume a 16 GHz clock frequency of NPU that meets the required throughput.

To achieve a lower power decoder, we use ERSFQ logic to design our decoder[34]. As we explained in Section II C, we can estimate power consumption of the ERSFQ circuit with Eq. 4. Therefore, the power consumption of the NPU in a 4-K environment \(P_{\text{NPU}}\) is as follows:

\[
P_{\text{NPU}} = 11.2_{[\text{mA}]} \times 16_{[\text{GHz}]} \times (2.068 \times 10^{-15})_{[\text{W/\mu W}]} \times 2 = 0.742_{[\mu \text{W}]}.
\]

We assume the idling operations of a distance-9 single logical qubit and the operating frequency of NPUs and QECOOL units are 16 and 2 GHz, respectively.

The power consumption of the NN decoder per logical qubit \(P_{\text{NN}}\) is

\[
P_{\text{NN}} = 0.742_{[\mu \text{W/NPU}]} \times (2 \times 9 - 1)^2_{[\text{NPUas/logical qubit}]} = 214.6_{[\mu \text{W/logical qubit}]}.
\]

The power consumption of QECOOL units per logical qubit \(P_{\text{QECOOL}}\) is 400.3 \(\mu \text{W}\) from the results of Ref. 10. Therefore, the total power consumption of the NEO-QEC decoder per logical qubit \(P_{\text{decoder}}\) is as follows:

\[
P_{\text{decoder}} = P_{\text{NN}} + P_{\text{QECOOL}} = 214.6 + 400.3 = 614.9_{[\mu \text{W/logical qubit}]}.
\]
Figure 9. Logical error rate performance of MWPM, QECOOL/QLATIS, and NEO-QEC (FP32 and XNOR-net-based binarized one) with base model NN decoder for (a) single logical qubit protection and (b) the merge-and-split operation of two logical qubits.

Table V. Total parameter sizes and pseudo thresholds of NEO-QEC (FP32) for various NN configurations.

| K | Layer | Kernel sizes | Hidden channels | Note | # of total parameters | Pseudo threshold (×10⁻²) |
|---|---|---|---|---|---|---|
| 2 | 7 × 7, 5 × 5 | 9 | Most lightweight | 4,425 | 0.018 | d = 5 |
| 2 | 7 × 7, 7 × 7 | 9 | | 7,872 | 0.118 | d = 7 |
| 3 | 7 × 7, 5 × 5, 5 × 5 | 16 | | 9,408 | 0.112 | d = 9 |
| 2 | 7 × 7, 7 × 7, 7 × 7 | 16 | | 21,952 | 0.117 | d = 11 |
| 4 | 7 × 7, 5 × 5 | 16 | | 9,440 | 0.122 | d = 13 |
| 5 | 7 × 7, 5 × 5, 5 × 5 | 16 | Base model | 15,944 | 0.129 | d = 5 |
| 2 | 7 × 7, 7 × 7, 7 × 7 | 16 | | 17,408 | 0.117 | d = 7 |

The power budget of the 4-K temperature region of dilution refrigerators is supposed to be 1 W[9]. Thus, we expect that

\[1 \times 614.9 \mu W/\text{logical qubit} \approx 1626\] logical qubits

can be protected in a cryogenic environment with our NEO-QEC architecture.

VII. SUMMARY AND DISCUSSION

In this paper, we proposed a NN-based online-QEC algorithm named NEO-QEC for decoding SC and LS with measurement errors by combining a convolutional NN and an existing online greedy decoder. We evaluated the decoder performance for a single logical qubit idling operation and an LS procedure with code distances up to 13. The decoder demonstrated logical error thresholds of about 2.3% and 1.3% for a single logical qubit and LS, respectively. The binarized NN technique enables us to implement the lightweight NN decoder with moderate accuracy degradation. Our decoder performance is comparable to the MWPM decoder. Furthermore, we designed an SFQ logic-based NPU for binarized NNs with XNOR operations. We evaluated the circuit characteristics of our architecture supporting NEO-QEC and the error-correcting performance of the algorithm. NEO-QEC has low latency and sufficient power efficiency to operate online decoding in a cryogenic environment.

In this work, we aimed to design a hardware-efficient NN-based decoder rather than an accurate one. Hence we used a simple CNN with a reasonable number of parameters. The maximum operating frequency (approximately 70 GHz) of the designed NPU indicates its potential to construct more accurate and low-latency NN-based decoders with a large number of parameters or with more complex NN techniques, such as 3-D convolutional or convolutional LSTM layers.

Although we assume a depolarizing noise model, where errors occur on each data and ancillary qubit independently in each QEC cycle, experimental results of real quantum devices have shown that the relaxation and dephasing times of qubits are different, which has a significant impact on the QEC performance with SCs[60]. NN-based decoders have the potential to handle non-uniform errors on qubits by learning a bias of qubits on the real device, either explicitly or implicitly. Our future work will extend our lightweight NN-based decoder to handle a realistic biased noise on real quantum devices.

Overall, we have designed a fast and ultra-low-power decoder for SC and LS by taking advantage of the binarized NN technique, and it has been shown to have the
potential to operate in a cryogenic environment. It has achieved an essential milestone toward practical FTQC.

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