Aluminum Single Electron Transistors with Islands Isolated from a Substrate

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The low-frequency noise figures of single-electron transistors (electrometers) of traditional planar and new stacked geometry were compared. We observed a correlation between the charge noise and the contact area of the transistor island with a dielectric substrate in the set of Al transistors located on the same chip and having almost similar electric parameters. We have found that the smaller the contact area the lower the noise level of the transistor. The lowest noise value ($\delta Q_x = (8 \pm 2) \times 10^{-6}e/\sqrt{Hz}$ at 10Hz) has been measured in a stacked transistor with an island which was completely isolated from a substrate. Our measurements have unambiguously indicated that the dominant source of the background charge fluctuations is associated with a dielectric substrate.

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1. INTRODUCTION

Numerous experiments with the Single Electron Tunneling (SET) devices have shown that the offset charge noise caused by fluctuations of the polarization charge on small conductive islands located between the tunnel junctions presents a serious problem\textsuperscript{1,2,3}. These background charge fluctuations dominate over the intrinsic shot noise of SET devices\textsuperscript{4} at low frequencies ($f < 0.1 \sim 1kHz$). They considerably impair the performance of SET electrometers, pumps\textsuperscript{5}, traps\textsuperscript{6}, etc. and do not allow the concept of digital SET devices to be developed\textsuperscript{7}.

For example, in a metallic SET structure the transistor island is in contact with the dielectric surrounding, namely the substrate from a bottom, the tunnel barrier layers and, as in the case of Al, the native oxide on the
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open surface of the structure. This surrounding apparently contains many trapping centers capable of producing random low-frequency variations of the polarization charge on the transistor island.

The idea of our study has been to effectively diminish the substrate component of noise in a SET transistor. We solved this problem by using the non-traditional (stacked) design of the transistor, in which the contact area of the island to the substrate was minimized. A small metallic island of the SET transistor was placed onto the oxidized base electrode(s), which efficiently screened the electric field of charge impurities located in the substrate.

2. FABRICATION OF THE SAMPLES

The Al transistors (see Fig. 1) with Al/AlO\textsubscript{x}/Al tunnel junctions were fabricated on Si substrate buffered by a sputtered Al\textsubscript{2}O\textsubscript{3} layer 200 nm thick. Shadow evaporation at three or four angles was used. The peculiarity of our method was that each electrode (the base and counter electrodes and the island) was formed individually.

Fig. 1. SEM image of the typical transistor of stacked geometry. Triple shadows resulted from three successive depositions of Al through the same mask.
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We fabricated and studied the three three types of samples. The transistors of type I (Fig. 2a-d) were fabricated in three deposition steps \textit{in situ}. After the first and second depositions the structure was oxidized to form tunnel barriers of the transistor junctions. We used a series of masks which allowed a gradual transformation from the planar transistor structure (Fig. 2a) to the stack geometry (Fig. 2d) to be realized. For stack transistors, particular attention was paid to precisely aligning the island and the base electrode to avoid contact between the electrodes.

Fig. 2. Geometry of the series of the type I transistors with different contact area between the transistor island and the substrate (a-d). The contact area is expressed as percentage of the whole island area. The junctions of type I transistors are of almost identical sizes. Their electric parameters are \( R_\Sigma = 200 - 450 \text{k}\Omega, \; C_\Sigma = 350 - 450 \text{ aF}, \; C_1/C_2 \approx R_2/R_1 \approx 3 - 5 \) and \( C_\Sigma \sim 0.8 - 0.2 \text{ aF} \). The transistor of type II (e), the sequence of fabrication steps (f-h) and the equivalent electric circuit (i) are shown. In this sample, the island (see also (d)) is completely placed on the base electrode. The device has a small shunting tunnel junction \( (R_{sh} \approx 1.9\text{M}\Omega) \). The electric parameters of the transistor are \( R_\Sigma = R_1 + R_2 \approx 3.9\text{M}\Omega, \; C_\Sigma = C_1 + C_2 + C_g \approx 270 \text{ aF}, \; C_\Sigma \approx 0.2 \text{ aF} \) and \( C_1/C_2 \approx R_2/R_1 \approx 20 - 30 \).
In contrast to type I, the transistor of type II (Fig. 2e) was intentionally fabricated to have a shunting tunnel junction between the outer electrodes. This was the price to be paid for the complete and reliable isolation of the island from the substrate. The base electrode of this device was deposited (Fig. 2f) in two steps, without oxidation between depositions. The island was formed in the third (Fig. 2g) deposition step at the same angle and through the same opening in the mask as in the previous (second) deposition. This self-aligned method and the fact that the mask opening shrinks during deposition guarantees that the island is deposited exactly on top of the base electrode with no contact to the substrate. As a result, a shunting junction between the base and counter electrodes was formed after the last, fourth deposition (Fig. 2h). The presence of the shunting junction has testified the absence of contact between transistor island and substrate.

The design of the sample of type III is depicted in Fig. 3. This transistor also has a tunnel junction shunt and the island is not in contact with the substrate. The structure consists of two touching fingers (electrodes) with an island positioned on top of these fingers. It has been fabricated by shadow evaporation at three different angles, with an oxidation after the first and second deposition steps.

![Fig. 3. Top view (a) and cross-section (b) of the type III transistor with an island placed onto the outer electrodes, thus isolated from the substrate. The device has the small-size shunting tunnel junction (\(R_{sh} \approx 1.1\ \text{M}\Omega\)). The electric parameters of the transistor are \(R_\Sigma = R_1 + R_2 \approx 0.75\ \text{M}\Omega\) and \(C_\Sigma = C_1 + C_2 + C_g \approx 250\ \text{aF}\). A dotted line shows a possible shift of the transistor island from its nominal position (solid line), giving rise to small-area contact between island and substrate.](image)
3. EXPERIMENT

The electric and noise characteristics of all samples were measured in a dilution refrigerator at the bath temperature of $T = 25$ mK. The magnetic field $B = 1$ T was applied to suppress superconductivity in the Al films. A voltage bias configuration was chosen and an output current $I$ measured by a transimpedance amplifier.

To observe the noise influence of the dielectric substrate on the electrometer performance, we have measured and compared the equivalent charge noise figures of the set of our devices. In most of the cases the magnitude of the noise signal depended on a slope $dI/dV_g$ of the modulation curve at a working point (see, for instance), pointing to the charge nature of the noise. We measured the low frequency ($f < 100$ Hz) noise spectra and characterized our samples by the magnitude of the charge fluctuations at $f = 10$ Hz. The results are presented in Figs. 4-6.

3.1. Devices of type I

The transistors of type I and type II, both of stacked geometry, had the lowest noise figure. The diagram in Fig. 4 demonstrates the gradual

![Fig. 4. Charge noise in the transistors of different geometries (shown in Fig. 2a-e) measured at small currents ($I \approx 10 – 20$ pA) and low frequency ($f = 10$ Hz). The transistors with the contact areas of 50%, 30% and 20% (Fig. 2a-c) and one of the stacked transistors (Fig. 2d), with a noise level of $7 \times 10^{-5}e/\sqrt{Hz}$, were fabricated on the same chip.](image)
decrease of the charge noise in the set of transistors (type I) with decreasing the island-substrate contact area. Since the perfect Coulomb blockade was observed in all stack transistors of type I investigated (Fig. 2d), i.e. they did not show any sign of a shunt between the base and counter electrodes, we cannot exclude the existence of small areas where the edge of the island is in contact with the substrate. These areas potentially contribute to the total noise of transistors, and this could explain the noticeable difference in the noise levels (see Fig. 4) of these devices.

The lowest charge noise level among the series of stacked transistors of type I, measured at $f = 10$ Hz, was found to be $2.5 \times 10^{-5}e/\sqrt{\text{Hz}}$ or, in energy units, $\sim 230\hbar$. Note that this level is still considerably higher than the fundamental white noise floor whose value estimated for our case is about $3 \times 10^{-6}e/\sqrt{\text{Hz}}$ or $\sim 4\hbar$. On the other hand, the noise figure obtained is substantially lower than the best one obtained for an electrometer of traditional (planar) geometry: $7 \times 10^{-5}e/\sqrt{\text{Hz}}$ or $\sim 1000\hbar$.

3.2. Devices of type II

The result obtained for the transistor of type II turned out to be superior to that obtained for the series of stacked transistors of type I (see Fig. 4). The presence of the shunting junction strongly modified the $I - V$ curves within the Coulomb blockade range (see Fig. 5a), but it did not hinder the gate modulation of the transistor current (Fig. 5b). The total current ($I = I_{tr} + I_{sh}$) through the structure (see Fig. 2i) consists of two components: the first ($I_{tr}$) depends strongly on the gate and bias voltages ($V_g$ and $V$) whereas the second ($I_{sh}$) depends linearly on bias voltage $V$ only. This fact resulted in that the $I - V$ curve of the device (Fig. 5a) was a superposition of the $I - V$ curve of SET transistor and a linear $I - V$ curve of the single junction. The only modification of the resulting $I - V$ curves (Fig. 5b) was their additional vertical shift of $I_{sh} = V/R_{sh}$.

At sufficiently low $I$ (corresponding to $I_{tr} = 5 - 10\text{pA}$), the noise level (see Fig. 6) did not show substantial dependence on the gate voltage, while at large $I$ the magnitude of the output noise depended, as is usual for the planar devices, on the value of the transfer function $dI/dV_g$ in a working point indicating the charge nature of the noise in the latter case. The fact that in the former case the difference between the noise spectra measured at working points A, B and C in Fig. 6b was insignificant, indicated that the charge noise component in the total transistor noise was not dominant. The evaluation of the noise contribution of the amplifier ($\delta I_{amp} = 5 - 6\text{fA}/\sqrt{\text{Hz}}$) to the total noise signal ($\delta I = 8 \pm 2\text{fA}/\sqrt{\text{Hz}}$) led to a very low value of the
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Fig. 5. Typical $I - V$ (a) and $I - V_g$ (b) curves of the type II transistor. $I - V$ curves are presented in the blockade (solid line) and open (dotted line) states of the transistor. The presence of a non zero conductance between the counter electrodes leads to a finite slope of the $I - V$ curve in the blockade state of the transistor and to the shift of $I - V_g$ curves depended on voltage bias $V$.

electrometer noise related to the input charge: $\delta Q_x = (8 \pm 2) \times 10^{-6} e/\sqrt{\text{Hz}}$ or, in terms of energy sensitivity, $\sim 30\hbar$ at 10 Hz\footnote{3}. This value is even below the level $[1.2 \times 10^{-5} e/\sqrt{\text{Hz}} or 41\hbar]$ recently attained by the so-called rf-SET transistor\footnote{16} at much higher ($f = 1.1 \text{ MHz}$) frequency where the offset charge noise should be obviously roll-off. Moreover, the lowest noise figure measured in a "shunted" stacked transistor at 10 Hz is close to its fundamental white noise floor\footnote{13} whose level for this sample was estimated to be $\delta Q_x = (2 \div 3) \times 10^{-6} e/\sqrt{\text{Hz}} or 3\hbar$. Since the measured noise magnitude still shows a trend to decrease with frequency, we believe that the electrometer sensitivity can approach its fundamental noise limit at frequencies of some ten Hz. The extremely small signal corresponding to the white noise floor could be measured with the aid of a less noisy (presumably cold) amplifier.

3.3. Devices of type III

The charge noise level of the transistor of type III (Fig. 3) was also found to be relatively low: $\delta Q_x = 7 \times 10^{-5} e/\sqrt{\text{Hz}}$ at $f = 10\text{ Hz}$, although it is considerably higher than that of the type II transistor. We believe that this is because of incomplete screening of the island from noise sources
Fig. 6. $I - V_g$ curve (a) and the output noise spectra (b) measured in the sample of type II at small current (6 pA) and at points (A, B, C) with different values of the current-to-charge ratio $dI/dQ_0$, where $Q_0 = C_g V_g$.

of the substrate. We assume that the island was placed so that its small part contacted the substrate (as shown in Fig. 3 by dotted line) because of imperfect alignment. Nevertheless, this design has obvious advantages: first, it is easier to fabricate than that of devices of types I and II and secondly, what is even more important, it gives the opportunity to reduce further the dimensions of the tunnel junctions and, hence, to increase an operation temperature of the SET electrometer.

4. DISCUSSION

Our experiments with metallic SET transistors of different design clearly show that the dominant contribution to the background charge noise is associated with a "noisy" substrate.

The stacked samples in which the island-substrate contact area was minimized (devices of types I, II and III) exhibit pretty low noise at low transport current. In some cases (transistor of type II) this residual low-frequency noise was insensitive to the gate voltage and this behavior might be associated with fluctuations of junction conductance. At high transport currents and bias voltages, the usual gate dependence of noise in these samples is restored and the noise level increases (see Fig. 7). Such behavior can be explained by activation of the charge traps inside the dielectric barriers.
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![Graph showing charge noise for different biases and frequencies.]

Fig. 7. The charge noise of the type II transistor obtained for different biases $V$ at frequency $f = 10$ Hz.

and the natural Al oxide covering the whole sample surface. In particular, the perimeter area of the island seems to be most sensitive to random recharging of traps located nearby, because a charge induced on a metallic surface of small radius of curvature strongly depends on a distance to the source-charge. As regards the tunnel barriers, their charge noise behavior (if any) at low currents $I_{tr}$ is remarkable. Even for very small $I_{tr}$, the electric field inside the barriers oscillates with the SET rate $I_{tr}/e$ and amplitude of $A = e/(dC_\Sigma)$, where $d$ is the barrier thickness. However, this rather strong field does not produce an appreciable random switching of the barrier traps. On the other hand, a strong alternative field can possibly re-charge the potential traps with the rate of SET oscillations.

In conclusion, we have proposed two possible ways (devices of types II and III) which allow the noise characteristics of SET devices to be drastically improved. In particular, the obtained charge noise level of the SET electrometer, with an island isolated from a substrate, $\delta Q_x = (8 \pm 2) \times 10^{-6} e/\sqrt{Hz}$ is the lowest one ever reported. The noise measurements of the device which island are not in contact with the substrate give justified hope that SET devices of traditional planar design with Al/AlO$_x$/Al tunnel barriers can potentially have much lower offset charge noise provided that an appropriate (noiseless) material for the substrate can be found.
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