Compact embedded device for lock-in measurements and experiment active control

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We present a multi-purpose toolkit for digital processing, acquisition and feedback control designed for physics labs. The kit provides in a compact device the functionalities of several instruments: function generator, oscilloscope, lock-in amplifier, proportional-integral-derivative filters, Ramp scan generator and a Lock-control. The design combines Field-Programmable-Gate-Array processing and microprocessor programing to get precision, ease of use and versatility. It can be remotely operated through the network with different levels of control: from simple out-of-the-shelve Web GUI to remote script control or in-device programmed operation. Three example applications are presented in this work on laser spectroscopy and laser locking experiments. The examples includes side-fringe locking, peak locking through lock-in demodulation, complete in-device Pound–Drever–Hall modulation and demodulation at 31.25 MHz and advanced acquisition examples like real-time data streaming for remote storage.

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I. INTRODUCTION

The demand for stabilization systems in optics, atomic and molecular physics experiments is increasing more and more with time. The realization of high accuracy measurements relies often on the fine control of several variables at a time in the same experiment: light intensities, emission wavelength, temperature, modulation depth, mechanical stress or position of elements; are just some examples of variables that need to be controlled for that purpose.

The standard approach in control theory for a stabilization and control procedure is a feedback scheme. This is accomplished by measuring certain variables of the system-under-control and acting on it with a set of control-parameters. The most common procedure is to measure outcomes, compare them to some preset desired values and then act on the system with a chosen strategy to compensate the deviations. The realization of this strategy is the core of the control system and its instrumentation has evolved from welded electronics analog circuits to more sophisticated and versatile digital processing systems. Probably, the most popular strategy used for control is the proportional-integral-derivative (PID) filter. Though it is known not to be the optimal strategy for all systems, its ease of use and understanding, as well as its satisfactory results makes it the usual workhorse in most practical setups and the one here chosen. Moreover, one can combine various PID filters to control multiple inputs and multiple outputs (MIMO), add filters and signal processing to any stage making the uses of PID control a versatile and intuitive platform for control.

The advent of fast microprocessor devices and field programmable gate arrays (FPGA) has paved the way to the implementation of the digital processing feedback schemes in experiment control setups. For example, PIDs filters were implemented on pure-FPGA boards. Also pre-processing information like phase detectors was also accomplished with FPGA. A pure microprocessor implementation of the feedback controller has been showed to be more versatile and less complex in some simple or slow tasks. Most of the experiences show the need to get a compromise between the fast and robust FPGA processing and the versatile and easy re programmable microprocessor global functions and control. This way, the FPGA can handle time sensitive functions often also in parallel, while the microprocessor provides the user higher level functions and control in an on-site configurable manner.

Embedded devices with FPGA and microprocessor were successfully used to achieve similar tasks as we show here. However they were developed in the framework of proprietary, platform-dependent software that limits the available tools for developing custom solutions and modifications. An open-source system and open-hardware solution has also been presented with servo and loop-back control system in pure FPGA for AMO.

In this work we present a versatile general purpose toolkit for system control instrumentation built on a FPGA and microprocessor embedded device that is ready for simple out-of-the-shelve usage and also for high complex integrated schemes of acquisition and control. The hardware is based on Red Pitaya STEMlab 125-14 board, which makes it a compact solution with a credit card size that can be acquired on web store. The FPGA and software design is all open-source and can be accessed through a web repository. The toolkit includes oscilloscope, ramp/scan controller, two lock-in amplifiers, modulation generators, PID filters and an overall control module which includes automatic locking, lock-watch and re-lock. A big difference with previews implementations...
FIG. 1: Layer structured design for the client-server architecture of the toolkit. The elements are grouped horizontally by site and type. In columns, the possible strategies are shown. The first column follows the Red Pitaya STEMLab original design philosophy. The dashed line separates the client part (end-user device) and the server part (STEMLab device). The arrows show communication direction between elements.

is the availability of a lock-in module which works with frequencies up to 31 MHz. All stages of the high frequency lock-in are implemented in the Red Pitaya module without the use of any extra components.

This device works as a stand-alone device that can be remotely controlled through Ethernet-TCP/IP network connection via a web-based interface, and is therefore platform independent. Moreover, one can log in to the embedded operative system via SSH protocol and set operation parameters through a communication bus to the FPGA, enabling different types of usage going from predefined easy configuration to low level user-defined programed control.

The present report is divided in two parts. In the first part we describe the toolkit hardware, software and usage. We describe the user strategies options and the toolkit design in section II A the architecture organized in layers in section II B and the usage logic organized in “instruments” in section II C.

In the second part, the toolkit is tested in several example applications in an atomic, molecular and optical (AMO) physics laboratory. We show a Rubidium absorption spectroscopy scheme in section III A with a Vertical-Cavity Surface-Emitting Laser (VCSEL), using the toolkit for acquisition of transmission signal and for side-fringe locking stabilization. Then we use an External Cavity Diode Laser (ECDL) to implement a saturated absorption spectroscopy scheme, in section III B using lock-in phase sensitive acquisition to lock laser emission frequency to spectral peak maximum. Finally, we present a Pound–Drever–Hall locking scheme for another ECDL, in section III C. The inlayers goals of this proposal is the lock-in operation at 31 MHz, enabling the implementation of the complete lock-in modulation and demodulation scheme in only one device, something which has never been reported so far.

II. SYSTEM DESIGN

The toolkit is based on a commercial system on chip (SOC) device known as Red Pitaya v1.1 (STEMLab 125-14) with a Xilinx Zynq 7010 integrated circuit core, that includes FPGA and a dual core ARM Cortex-A9 Processor, integrated to peripherals suitable for signal acquisition and generation (fast ADCs, DACs, DIOs, and communication ports). The device operation follows a client-server architecture that can be thought as a layer structure. The client side is the user front-end running on clients own device. The server side is the STEMLab device, including Operative System, programmable electronics and hardware peripherals. The layers can be controlled on different levels depending on the user’s requirements. In the following we describe possible application strategies and the layer architecture, both depicted in figure 1.

A. User Strategy

We present here three different user strategies with growing complexity and versatility. Depending on the needs, an user can choose from simple pre-defined working modes to modifying instrument cabling or programming complex measurement and feedback routines.

The “GUI predefined operation” option allows to perform most of the tasks here described from a web browser in the user device. The front-end is part of the client-side and is built over HTML+JS page and presents a friendly interface for several instruments operation: two lock-in amplifiers, two PID loops with different locking and re-locking routines, an on-screen oscilloscope and cabling between them. These allow to perform a wide variety of measurement and control tasks which we describe in detail in part III with several examples which include low and high frequency lock-in measurements and active stabilization of lasers.
An even greater versatility can be achieved via the “programmed and remote acquisition and control” option. All the instruments can be remote controlled and data can be acquired through user commands, enabling the possibility of incorporating them to algorithms designed by the user in various programming languages. Example code can be found in the project repository for Python and Matlab, including two channels oscilloscope acquisition, on-demand multichannel reading of several signal values and instruments operation by writing control register values.

The user commands are Python scripts executed in Red Pitaya shell that implement the basic procedures for reading and writing RAM addresses values linked to FPGA registers. The remote execution can be done by any remote-shell tool, using serial communication (microUSB) or Ethernet (RJ45 port). The examples provided on-line use SSH protocol over TCP/IP network, being a secure and versatile option that can be incorporated to almost any already working computer network. Moreover, open-source implementations of SSH protocol are available for all possible operative systems of the client, enabling the operation from any device or programming language.

The on-demand read and write procedures are only limited by network communication delays and microprocessor process priority. The provided examples include combined operation of instruments for tasks like ramp/scan configuration, lock-in acquisition of system response, PIDs configuration and launching a triggered controlled stabilization scheme.

We also provide an API for Python to simplify code writing of user designed “resident programs”, running in server side. This enables the operation of instruments with lower latency and enables the design of algorithms for fast decision making, faster multichannel acquisition and stand-alone working without client side. In this way, data acquisition and instruments commands can be made with a latency of ~ms order.

The “resident programs” advantages can exploited to implement different integration strategies of the toolkit in the lab. For example, acquired data can be pre-processed on server-side and stored in the STEMLab device for later user retrieval. On the other hand, the raw or the pre-processed data can be streamed to client side for on-line monitoring and storage. The user can choose these or other options, depending on whatever suits the experimental scheme better. In subsection we report an example of long accumulated measurements streamed to the client-side, used for Allan-deviation calculation.

B. Layer architecture

The system design can be understood in a 4 layer scheme (see figure [1]). The lower three layers are part of the server side and take place in different parts of STEM-Lab board hardware.

The lowest one is the “Welded electronics layer”, that provides the connection to digital and analog input/output ports and the access to peripherals, including some analog electronics for signal conditioning. Signals in this layer are converted from continuous analog voltage signals on wires to digital clocked buses of data, suitable for FPGA reading. For this purpose the board includes two fast Analog to Digital Converters (ADC), associated with in1 and in2 FPGA buses, and two fast Digital to Analog Converters (DAC), associated with out1 and out2 FPGA buses, working at 125 MSa/s with 14 bits of resolution, on the range of ±1 V. ADC inputs can work in the range of ±10 V with hardware jumper configuration. Also, 16 input/output digital pins are included, with a maximum refresh rate of 125 MSa/s, on a LVC-MOS 3.3 V logic. It also includes four slow outputs of 0–1.8 V, 1 MSA/s build from low pass filtered PWM signals, and four slow inputs with the same sample rate.

The “Programmable electronics layer” stores the digital electronic FPGA circuits for real-time processing, like filters, mixers, adders, etc, that build up the core of each instrument implementation. In this layer the signals data flow through digital buses that represent signed integer values of 14 bits resolution. The circuits were designed in Verilog language, synthesized using Xilinx Vivado 2005.2 software and implemented on the Zynq-7010 FPGA chip on the Red Pitaya board. The Xilinx development tools for this chip are available for free, so no additional costs are incorporated on development licenses if the design should be modified. This layer also provides connectivity between the microprocessor and “Welded electronics layer” through specialized data buses.

The FPGA design was made with simplicity in mind, to ease the user understanding of the electronic logic. Also, the implementation was made trying to prioritize direct wire processing, reducing the usage of registers in the middle of input-output signal flow. This decision was taken because each register adds a clock period delay (8 ns) to the data flow. Closed-loop control schemes are bandwidth limited by this delay value. The achieved delay for device input-output using one PID filter was 130 ns, which imposes a theoretical limit to the feedback bandwidth of 3.8 MHz.

The “Operative system layer” stores the back-end logic that controls the operation of the digital circuits. It runs a GNU/Linux operating system with a set of RAM memory addresses mapped to FPGA registers that are used by the instruments circuits to set their configurations or store data. The back-end logic reads and writes these registers and makes some data conditioning, like conversion from FPGA integer rawData to end-user float-voltage data values. This logic is implemented in the API (programmed in Python) and also in the Nginx web server (programmed in a C extension module). The web server provides the client access and control from user web browser, exchanging data using JSON standard format and HTTP/POST protocol. The API is used by the user commands introduced in the section.

The “User Front-end” layer is only provided for the “GUI predefined operation” strategy, and it consists of a dynamic web page loaded in the client device. The data acquired in FPGA layer, and conditioned in the back-end layer, is shown here in an intuitive way, as can be seen in [6].
C. The instruments

The functionalities of the toolkit have been organized in logical units called “instruments”, that allows the user to interact with it. Each instrument provides some of the functionalities of typical laboratory equipments used for acquisition and control. The instruments implemented are:

1. Two Lock-in amplifiers
2. Two Proportional-Integral-Derivative (PID) controllers
3. A Ramp/Scan function generator
4. A general Lock-control helper, with event monitor and re-lock routine
5. An Oscilloscope

Each instrument is composed by a set of HTML controls in the Web GUI, grouped in panels, and a set of Verilog modules for the FPGA layer. Instruments 2 and 5 are modified versions of the open-source applications developed by Red Pitaya community and released with a BSD license. Instruments 1, 3 and 4 were developed for this work.

In the FPGA layer, the instruments are composed by logical modules whose behavior is controlled and monitored by registers. The modules are independent interconnected circuits which handle signal acquisition, processing and generation. They also include internal memory which allows implementing filters and control loops. The base modules include: function generators, ramp generator, multipliers, demodulators, low-pass filters, multiplexers, etc.

The control registers can be set and read from Red Pitaya local shell, from remote software or from the application Web GUI. The last one includes user friendly options for operation, described with more detail in section.

A set of buses and multiplexers allow the interconnection of the different instruments. The buses transport the ADC input signals and the instruments outputs signals. The multiplexers are controlled by the user through register values to chose the instruments inputs or the DAC outputs signals. In this way, several instruments can be combined into a system with dedicated purpose, such as lock-in demodulation and PID control for stabilizations schemes.

Core design of the instruments is described in this section and usage information is documented in the project web page.

1. The lock-in amplifiers

Two lock-in amplifiers were implemented to cover different kinds of applications: a “standard” harmonic lock-in, with a frequency range that goes from 3 Hz to 49.6 kHz, and a square wave lock-in with wider frequency range, from 30 mHz to 31 MHz.

![FPGA designed logic for the lock-in demodulation paths.](image)

**FIG. 2:** FPGA designed logic for the lock-in demodulation paths. The Lock-in input is a signal selector common to all the demodulation paths: signal_i. The part inside the dashed line box is repeated 7 times, changing the ref_i name and the elements parameter ranges.

**TABLE I:** Reference of lock-in demodulation paths depicted in figure 2. The 1–5 paths are part of the harmonic lock-in, and the 6–8 are part of the square wave lock-in.

| i ref name | signal equation | out27 name | out14 name |
|------------|-----------------|------------|------------|
| 1 cos_ref  | cos(2π ft)      | X          | Xo         |
| 2 sin_ref  | sin(2π ft)      | Y          | Yo         |
| 3 cos1f    | cos(2π ft − φ)  | F1         | F1o        |
| 4 cos2f    | cos(2π ft − 2φ) | F2         | F2o        |
| 5 cos3f    | cos(2π ft − 3φ) | F3         | F3o        |
| 6 sq_ref   | sgn(cos(2π fsq t)) | sqX | sqXo |
| 7 sq_quad  | sgn(sin(2π fsq t)) | sqY | sqYo |
| 8 sq_phas  | sgn(cos(2π fsq t − φ)) | sqF | sqFo |

Figure 2 shows the scheme of the FPGA implementation logic of a lock-in demodulation path. The input signal signal_i is multiplied by a local oscillator ref_i signal that settles the frequency and phase reference, and then is filtered by a low pass filter (LPW) with a cut-off frequency of fcut. The LPF output out27i is a 27 bit signed int register which is available for recoding measurements and which can be monitored via the web GUI. A bus-trim applied to the register reduces it to a 14 bits signal out14i. The selection of the trimmed bits has the net effect of an amplifier by powers of 2, controlled by the amp_i parameter. This 14 bit signal can then be connected to either the PIDs, the output DACs or the oscilloscope input channels.

The Harmonic Lock-in is composed of five demodulation paths like the depicted in figure 2. Each path has its own ref_i signal and buses names, showed in table I that can be used in the application for DAC outputs or oscilloscope visualization. The cos_ref and sin_ref paths have their reference in quadrature, so the X and Y outputs provide the full phase and amplitude information of the signal_i filtered frequency component. The other three paths allow to set a fixed phase relation respect to cos_ref and also obtain information about the first (2f) and second (3f) harmonics. The φ parameter, which can be configured through the Web GUI phase control, sets a phase displacement of φ = 2π f_in/2930.

Each local oscillator signal is made from 2520 signed integers values proportional to a sine period. They are stored in a memory module implemented as various lookup tables. The reading addresses for the memories modules are set by counter modules, driven by a con-
2519
\[ \sum_{i=0}^{2519} f[i] \cdot g[i] = 0 \quad \text{for } f \neq g \quad \text{and } f, g = \begin{bmatrix} \cos & 0 \\ \sin & 0 \\ \cos 3f & 0 \end{bmatrix} \] (1)

The square wave lock-in is composed of three demodulation paths: 6-8 from table 1. Two local oscillators in quadrature (sq_ref and sq_quad) allow the acquisition of the complete quadrature information in the sqX and sqY registers. Also, another oscillator path, sq_phas, with configurable phase relation is available, with output value stored in sqF.

The square wave signals are build on run-time, switching a bit that represents the ±1 values. The working frequency \( f_{sq} \) is set by defining the semi-period time length, counting steps the base FPGA clock. In this way, the period can be set with a resolution of 8 ns, starting from 32 ns (31.25 MHz) and expanding the possible values up to 68 seconds. The \( \varphi \) phase relation is set as an integer factor of 8 ns. The multipliers of these paths are mapped from the binary values to \( \pm 1 \). The sq_ref binary signal is available in one of the fast binary outputs of the extensions pins of STEMLab device, and all the signals can be used on the DACs outputs, where they are mapped from the binary values to \( \pm 0.5 \) volts.

The out27 register enables lock-in measurements with a full resolution of 27 bits and a sensitivity of 59.6 \( \mu \)V. The sensitivity can be enhanced with pre-amplification, as is shown in experience of section [III.B].

2. PID controllers

Two PID modules were implemented for use in feedback stabilization schemes. The circuit design is based on the PID included in the free software applications of Red Pitaya community[10]. They were modified to extend the working parameters range over several orders of magnitude, by incorporating scale registers. The output control was enhanced by adding features like output value freezing and integrator memory freezing, useful for re-lock routines (see [I.C.4]).

Both modules have a common error signal as default input, that can be selected from different input buses, as is shown in figure 3. The input can be shifted by a user-controlled error_offset value that can be interpreted as a working setpoint. Also, independent input signals for each module can be chosen (not shown in the figure).

Each module implements three filters, proportional, integral and derivative, that sums up to build the output signal pidX_out \((X = A, B)\), as it is showed in figure 3. The summed result is stored in a register which allows to freeze the value at command.

The behavior of the three filters depends on the value of three parameters: \( k_p, k_i, k_d \) and \( \tau_d = \tau_d \). Two registers allow the user to control each of them: one 14 bit signed int value changes the parameter linearly while the second value allows to change the order of magnitude of the parameter, working as a scale control. For example, the \( k_p \) parameter is controlled by the pidX_kp register value, and by the scale factor set by the register pidX_PSR, that allows to choose uno of the predefined values for \( n_p \) in equation (2a). The same logic is applied to control \( k_i, k_d \) using pidX_ki, pidX_kd and pidX_ISR, pidX_DSR respectively, as is shown in equations (2b) and (2c):

\[
k_p = \frac{\text{pidX}_\text{kp}}{2^n_p} \quad \text{with } n_p = \{0, 3, 6, 10, 12\} \quad (2a)
\]

\[
\tau_i = \frac{2^{n_i} \cdot 8 \text{ns}}{\text{pidX}_\text{ki}} \quad \text{with } n_i = \{0, 3, 6, 10, 13, 16, 20, 23, 26, 30\} \quad (2b)
\]

\[
\tau_d = \frac{2^{n_d} \cdot 8 \text{ns}}{\text{pidX}_\text{kd}} \quad \text{with } n_d = \{0, 3, 6, 10, 13, 16\} \quad (2c)
\]

The linear coefficient register lets the user have fine control over the PID parameters, while the power of two factor, implemented efficiently through shift registers, expands the parameters scope over several orders of magnitude. This dual scale allows controlling systems with time constants ranging from a few \( \mu \)s to many seconds.

The derivative module of the PIDs was completely rewritten to avoid high frequency noise amplification. The new design ensures that spikes and frequency components whose characteristic times are below the order of magnitude settled by the \( n_d \) value won’t induce undesired perturbations that can make the feedback scheme
unstable. The implemented design includes a down-sampling procedure and a slope calculation sub-module, called slope9. The PID input signal is down-sampled taking the mean value of $2^{n_d}$ consecutive data samples, so the processed signal that feeds the slope9 sub-module has a ladder shape with a $T_d = 9 \cdot 2^{n_d} \cdot 8\text{ns}$ step time length. The net effect of this procedure is similar to the application of a low pass filter with time constant of $T_d$ before the derivative calculation. The slope9 sub-module calculates the signal derivative by taking the slope of a linear square least regression of the last nine steps values of the down-sampled signal.

The parameters $k_p$, $\tau_i$ and $\tau_d$ can be used for prediction of an ideal PID response to an $e(t)$ input signal using the equation (3a). The equation (3b) provides a more accurate prediction of the implemented PID response in clock steps of 8 ns. The “slope9out” function represents the slope9 submodule output signal that can be simulated by an algorithm following the procedure described above.

\[
\text{pid}_{out}(t) = k_p \cdot e(t) + \frac{1}{\tau_i} \cdot \int_0^t e(t') \, dt' + \tau_d \cdot \frac{d}{dt} e(t)
\]

\[
\text{pid}_{out}[n + 1] = k_p \cdot e[n] + \frac{8\text{ns}}{\tau_i} \cdot \sum_{i=0}^{n} e[i] + \frac{\tau_d}{8\text{ns}} \cdot \text{slope9out}(e[n, \ldots, n - 9 \cdot 2^{n_d} + 1])
\]

### 3. Ramp function generator for Scanning

A triangle wave-shape generator was implemented for scanning purposes. Two synchronized signals are built on run-time, ramp_A and ramp_B, useful to control two system parameters at the same time.

The ramp_A behavior is controlled by setting the triangle sweep range and the time length $T$ of each step of the ladder-shaped signal (see figure 4). The registers ramp_hig_lim and ramp_low_lim control the top and bottom limits, and the ramp_step register sets $T = \text{ramp_step} \cdot 8\text{ns}$, all of them accessible from Web GUI. After each $T$ time period the ramp_A value increases/decreases by 1 int until it reaches one of the limits, and then changes the slope sign. ramp_B is generated multiplying ramp_A by the factor ramp_B_factor/4096.

The instrument allows the user to select the ramp slope and limits. Since the acquired signal waveform may change with sweeping speed, affected by bandwidth limits of intermediate elements, the slope is kept constant when the range limits are changed by the user. This lets the user see the same waveform through all the process. This design has been helpful when using the ramp for spectroscopy acquisition schemes, making it easier to choose the scanning range.

The ramp generator can be started and stopped in any time through the ramp_enable register, can be reseted to ramp_A=0 value, and the starting slope sign can be set. Also, the Lock-control module can take control of the start/stop command and the ramp limits for locking and re-locking procedures.

### 4. Lock-control

A device meant for locking to a given error signal normally requires switching between different behaviors: scanning, locking, re-locking on events, etc. Changing from one state to the other requires timed interaction between the previous modules. This interaction is handled by the Lock-control module. Figure 5 shows the schematic inter-cabling of the modules.

![FIG. 5: Lock-control links to PIDs and Ramp instruments. Red lines are signal data buses and turquoise lines represents sets of buses for parameters configuration. All the Lock-in outputs and the ADC inputs can be used in the PIDs for signal processing and in the Lock-control for event identification and trigger.](image)

A typical example of this behavior is what we call Trigger Lock. Here the system switches from a scan-mode, where one can see the error signal by sweeping the control parameter, to a lock-mode where the scan is turned off and the PIDs are turned on to stabilize the error signal. That is, on a trigger event, the ramp’s outputs are frozen and the PID’s outputs are enabled. The trigger can be set to a given value of the ramp period (time trigger), to a given value of the signal (level trigger) or the fulfillment of both conditions (level+time trigger). The values for these triggers can be selected graphically on the Oscilloscope screen or manually settled.

The module also provides a Re-lock routine which tries to automatically re-lock on eligible events. This submod-
ule will consider the system is out-of-lock when the absolute value of the error signal exceeds a set value or when one of the inputs \((\text{in}_1, \text{in}_2, \text{in}_1-\text{in}_2, \text{or any lock-in demodulated signals})\) drops below a set threshold. When any of these conditions is met the re-locking routine is started. The re-locking procedure was inspired on a recent work\(^2\) and consists on freezing the PIDs and starting a ramp scan increasing the scan limits on a two factor in each half period. If during scanning the system reaches a lock condition, the submodule stops the scan and turns on the PIDs again. If the lock condition is never met, the submodule will continue increasing the scan amplitude until it makes a semi-period sweep with the longest width \((1 \text{ V} \equiv 8192 \text{ int})\), and then will stop ramp.

Finally, a submodule which carries out a Step Response Measurement allows the user to evaluate the system response to an abrupt change in the control value. This information can then be used to calibrate the parameters of the PID modules.

5. Oscilloscope

The Oscilloscope instrument is a modified version of Scope Application from Free Software Red Pitaya developers community\(^\text{10}\). It’s composed of two memory arrays with a length of 16384 for storing 14 bit signed int values, modules for triggering, decimation control and anti-aliasing filters, and it allows to make acquisitions on FPGA clock sample rate (125 MSa/s). Here we extended the functionality of the basic oscilloscope to allow the display of various internal and external signals. These include the ADC inputs \((\text{in}_1, \text{in}_2)\), instruments outputs (PIDs and Ramp), important link buses \((\text{error, ctrl}_A, \text{ctrl}_B)\) and all the lock-in paths outputs and local oscillators. With this extension, the oscilloscope is useful not only for external data acquisition but also for internal data flow and processing inspection, essential for debugging and tuning the parameters of each module.

Also, some acquisition options were added. We included the possibility to disable the anti-aliasing FPGA module filter and to incorporate more triggers from useful signals. The external trigger is extended for user selectable event list, including out-of-lock, triggered lock-start, ramp\(A\) at limit reach and lock-in oscillators period start. Also, some web GUI options were added, like an R-\(\phi\) (absolute and phase) run-time calculation option for lock-in \(X, Y\) and \(sqX, sqY\) visualization and switch between Volts and int units. By default, the acquired curve values are expressed in Volts, using the ADC/DAC conversion factor (signed 14 bits int resolution): \(8192 \text{ int} \equiv 1 \text{ V}\). This can be switched to raw int values.

D. The Web GUI

The Web GUI frontend design is also based in free software Scope application\(^\text{10}\). It provides the out-of-the-shel functionality showed in the first column of figure\(^\text{1}\). It is structured in columns with dropdown panels that groups configurations settings by functionality. We improved the interface adding several useful functions, like data save/load, configuration save/load, stop button, etc.

A left column was added for placing the instruments panels designed for this work, and two bottom panels for the lock-in amplifiers outputs visualization (figure\(^\text{3}\)). The instruments controls were designed with the philosophy of keeping simplicity without compromising the low-level accuracy. Most of the controls use integers numbers for input data type, that allows the user define the precise value of the FPGA registers that the circuits will use, and includes text displays that translates this values to the physical magnitudes involved (i.e., seconds, volts).

The oscilloscope screen is in the middle of the page. It displays two channels for plotting user selected signals. In the sample applications discussed below, in part III one channel shows the spectral response of the system while the other displays the error signal. This provides a fast way to view and evaluate the performance of the system on lock, entering a lock, and re-locking.

III. EXAMPLE APPLICATIONS

We report a set of experimental applications of the toolkit presented in order of complexity to show the instruments usability and potential. In the first one (section IIIA) we introduce the usage of the Ramp and the Oscilloscope to take the absorption spectrum of an atomic vapor, with a simple scheme of one control parameter and one measured variable. Also, we implement a side-of-fringe locking scheme using a PID controller an the Lock Control instrument. In the second application (section IIIB) we add the Harmonic Lock-in amplifier to the measure and stabilization scheme, in a saturated absorption experiment. We used two output ports and measure two input variables, in a multi-input-output control system, but with only one control parameter. In the third one (section IIIC) we show the Square Lock-in amplifier working at 31 MHz for a Pound-Drever-Hall stabilization application. Some advanced capabilities are shown here, like multiple controlled variables, in-device programing for special measurements and different hardware implementations of same stabilization scheme. Finally, we discuss some potential applications of the toolkit.

A. Absorption spectroscopy: Ramp, Oscilloscope & PIDs

We tested the out-of-the-shel capabilities of the toolkit in an atomic vapor absorption spectroscopy experiment with Rubidium. A tunable laser that goes across an atomic vapor cell is used to make a optical-frequency scan around one of the atomic electronic transitions. A photodiode is used to measure the intensity decay at the cell output (figure\(^7\)), as a result of the absorption on transition resonance. We used a VCSEL, what ensures mode-hop-free scanning using only one control parameter: the diode current\(^12\). The laser wavelength is centered in 795 nm, suitable for Rubidium D\(1\) line \((5^2S_{1/2} \rightarrow 5^2P_{1/2})\) spectroscopy.
FIG. 6: Web page GUI frontend, organized in three columns and panels. The left one contains one panel per instrument with the configurations options for each one. The right one contains the oscilloscope visualization options. The middle one contains the oscilloscope screen and panels for out27 lock-in measured values visualization.

FIG. 7: Scheme of the Rubidium absorption spectroscopy experience. Only one system parameter is controlled (laser diode current) trough out1 output, and one variable is sensed (photodiode response) trough in1 input port. M: mirror; PD: photodiode; Rb: Rubidium vapor cell.

The Ramp instrument was used to make the frequency scan, by performing a voltage-controlled sweep of the current driver. The Oscilloscope instrument was used for photodiode signal acquisition.

The Ramp was configured to make a scan of $\sim 1$ V through out1 DAC at 7 Hz. In figure 6 the transmitted signal measured by the photodiode is shown with blue line. The base slope of the curve is related to the laser power increment along the scan because of the current variation. The four dips in the curve are the absorption lines for each of the hyperfine-split transitions.

This experiment was used to test the most simple stabilization scheme: side-fringe locking. The variable to stabilize is the transmitted signal, measured from in1 port. The PID instrument was used to make the feedback response and the Lock Control instrument was used to control loop-close event.

The locking set-point was configured on $\text{error}_{\text{offset}} = 2620 \text{int} \approx 0.32 \text{V}$ to lock the side of the last spectrum dip in the Ramp scan, making

FIG. 8: Absorption spectroscopy of Rubidium. The transmitted intensity across the Rubidium cell is plotted for a complete Ramp scan measurement (blue line) and for a lock-start event (orange line). The curve dips corresponds to $^{87}\text{Rb}$ and $^{85}\text{Rb}$ hyperfine absorption lines.
\[ \text{error} = \text{in1} - 3300. \] To prevent the lock on the first
cross-over of \text{error_offset} the Lock-control instrument
was configured to close the loop on \text{level+time}
trigger. The loop-close procedures was configured to
stop the Ramp scan and enable the pidA_out. The
PID parameters were set to \( \tau_i [\text{ki}=600] \equiv 895 \mu s \) and
\( k_p [\text{kp}=1024] = 1. \)

The result after reaching Lock-control \text{level+time} trig-
ger condition is shown in the figure 8 (orange line). The
transmitted signal remained in the configured set-point
level with a standard error of \( \sigma = 1.85(3) \) mV.

\section*{B. Saturated absorption spectroscopy:
Harmonic Lock-in}

In this experience we extended the previous setup to
make a Saturation Absorption Spectroscopy \text{[13]} scheme,
that allows to measure transitions with resolution ex-
ceeding the limit posed by Doppler broadening \text{[13]}. This
scheme uses a pump and probe configuration, imple-
mented here with the same beam reflected in a mirror,
as it’s shown in figure 9. The pump saturates the trans-
ition and induces transparency, sensed by the probe as a
transmission peak. This technique enables the possi-
bility of laser frequency locking to absolute references with
higher accuracy.

![Diagram](image)

**FIG. 9:** Scheme of saturated absorption spectroscopy of
Rubidium. The ECDL emission wavelength is controlled
through two parameters: PZT voltage and diode current. A
harmonic modulation is incorporated through current driver.
The lase going from right to left is the pump beam. The
reflection is the probe beam. Two polarization rotations
with the QWP and the PBS are used to recover the
outgoing probe beam and measure it with the photodiode.
Direct photodiode voltage and an AC amplified line are
registered by the FPGA fast input potrs. M: mirror; QWP:
quater wave plate; PBS: polarizing beamsplitter; FI:
Faraday isolator; PD: photodiode; Rb: Rubidium vapor cell.

We used an ECDL at 780 nm wavelength, suitable for
Rubidium D2 line \((5^2S_{1/2} \rightarrow 5^2P_{3/2})\) spectroscopy.

In this kind of lasers, the diode current and the posi-
tion of the diffraction grating are controlled to tune the
laser. The position of the grating is controlled with a
piezoelectric (PZT) element. If both parameters are con-
trolled simultaneously mode-hop-free tuning range of sev-
eral GHz can be achieved \text{[13]}. Figure 10 shows an example
laser frequency scan (blue line) around the transitions
\( F_e = 3 \rightarrow F_a = 2, 3, 4 \) for \(^85\text{Rb}\) isotope. In the figure,
the optical frequency increases with \text{ctrl_A}. The sub-
Doppler hyperfine transitions peaks and the cross-over
\text{[13]} peaks were marked with vertical gray lines.

For the stabilization of the emission frequency a lock-in
scheme was implemented, to get a \text{error} signal suitable
for peak maximum locking, and demodulated from the
signal sensed by the photodiode. An harmonic modula-
tion \text{cos_ref} was introduced through current driver.

Two fast inputs and two fast outputs were used in this
scheme (figure 9). The in2 port was used for direct pho-
diode signal digitalization, to measure the transmitted
laser intensity. The in1 port was used to measure AC
components of the photodiode signal, using an analog
high pass filter and amplifier, what allows to improve
the sensitivity of lock-in demodulation. The acquisition
was made using the Oscilloscope instrument, registering
the transmitted intensity and the demodulated signal.
The \text{ctrl_A} signal on out1 port was used to control
the laser frequency. The Ramp instrument was used for
frequency scanning and PID for frequency stabilization,
trough feedback loop. The current and PZT sweep ampi-
tudes were tuned through drivers hardware. The out2
port was used to produce the modulation of the laser
current.

The Harmonic Lock-in was configured to demodulate the
in1 signal. Demodulated signals \( X_0, Y_0, F_{10}, F_{20} \) and
\( F_{30} \) were available for visualization and acquisition.
The first three of them are proportional to the first deriv-
ate of the transmitted signal in2 (at first order of mod-
ulation depth \text{[13]}) and the last two are proportional to
the second and third derivative, respectively. The odd
derivatives expose in2 minimum and maximum as zero
crossing points. This characteristic makes them suitable
as an \text{error} signal for min/max peak locking.

In figure 10 the \( F_{10} \) and \( F_{30} \) signals are shown. The
\( F_{30} \) is not sensible to first derivatives offsets, like the lin-
ear power increment of the current sweep, and less sensi-
tible to peak base line contributions that shift the mini-
um / maximum positions of the transmitted signal re-
spect to ideal ones, which is why it was selected as \text{error}
signal for the PID input. The filter was configured with a
proportional component with constant \( k_p = 1.56 \cdot 10^{-2} \),
for fast corrections, and an integral component with con-
stant \( k_i = 5.59 s^{-1} \). The Lock-Control instrument was
configured to trigger the loop-close event whenever \( F_{30} \)
gets over 2048 int (red line), with the “level trigger”. An
example of lock start is presented in figure 10 with or-
ange line superimposed to the normal scan signal. In
this example, an stability of \( 226(13) \) kHz of the optical
frequency was achieved after lock, on a 10 minutes mea-
surement. The frequency deviation was estimated from
\( F_{30} \) standard deviation and the knowledge of the \( F_{30} \)
slope on the locked peak position \text{[13]}. The \text{CTRL_A} was
used to measure the corrections made to the system, as
an estimation of the frequency deviation the laser would
have had if it had worked in open-loop configuration:
54(4) MHz RMS over 10 minutes.
FIG. 10: Relevant signals for a saturated absorption spectroscopy open-loop scan (blue) and a triggered closed-loop stabilization scheme to an peak maximum (orange). in2 is the transmitted signal sensed by the photodiode. in1 is in2 DC-decoupled and amplified (see figure 7), and is used for lock-in demodulation. F1o and F3o is the demodulated signals at 1f and 3f respectively. ctrl_A is the control signal, running a Ramp scan. The demodulated signals show the first and third derivative-like behavior, with zero-crossing points on in2 peaks maximum. F3o was used for error signal and the red line shows the level threshold for lock-start trigger. The left V_signal axis represent the voltage scale of this signals in the photodiode output.

C. Pound-Drever-Hall technique: Square Lock-in

In this experience an ECDL (centered at 854 nm wavelength) was stabilized to a reflection dip of a high finesse Fabry-Pérot (FP) cavity using the Pound-Drever-Hall (PDH) technique. This stabilization scheme uses lock-in demodulation of the laser intensity reflected from the interferometer to produce the error signal. The modulation frequency must be greater than the cavity’s bandwidth, which are both typically chosen to be in the few MHz range. The laser is modulated producing sidebands that lay out of the transmission peak bandwidth of the interferometer, so their reflection produces a beating that can be measured by a fast photodiode. This technique is often used for laser stabilization in AMO Labs.

The experimental setup is depicted in figure 11. Two control signals were used for laser control: ctrl_A for current driver and ctrl_B for PZT driver. The radio frequency modulation was incorporated directly into the laser diode using a bias-T configuration and passive electronic components. The reflected signal was measured by a fast photodiode with DC-decoupled output and digitalized, using port in1, for lock-in demodulation. Another photodiode was used to measure the transmitted signal through in2 port for system state reference. An example measurement for demodulated signal error and in2

FIG. 11: Scheme of the Pound-Drever-Hall stabilization technique implemented for this work. Includes two control signals for the ECDL and a modulation signal (sq_ref) incorporated directly to the current line with a bias-T configuration. The transmitted and reflected signals are collected by photodiodes. The QWP and PBS are combined for polarization rotation and reflected beam isolation. M: mirror; QWP: quarter wave plate; PBS: polarizing beamsplitter; FI: Faraday isolator; PD: photodiode; FPD: fast photodiode; L: lens; FP: Fabry-Pérot interferometer.
input is shown in figure 12.

Two configurations of hardware ports were used in the implementation. Both of them dedicated one of the 14 bits fast outputs (out1) to the current driver. In the first configuration, the other 14 bits fast output (out2) was used for sq_ref modulation signal and one of the 12 bits slow outputs of the extension bus (slow_out1) was used for PZT driver. The slow output update speed is enough for a PZT driver, whose bandwidth limit is in the order of tens of kHz, but with the downside that the output signal has a high frequency ripple, that comes from the original PWM signal. To reduce side-effects of the ripple we included a second order passive low-pass-filter before the PZT driver. The second configuration option was to use the out2 port for the ctrl_B signal of PZT, without any filter. In this case, the sq_ref signal was supplied through one of the extension digital pins (3.3 V at 125 MSa/sec) as a square function. A DC-decoupling capacitor and a second order passive low-pass-filter were used to build a band-pass filter, for signal conditioning: suppression of high frequency components, zero-centered signal and power attenuation.

The sq_ref modulation signal was configured on 31.25 MHz, the higher available frequency for Square Lock-in. A second order filter with a frequency cut of $f_c = 38.856$ kHz was used for demodulation, that produces a time lag of $\Delta t \sim 8.2 \mu$s over the error signal. This imposes an upper bound to the feedback gain and/or to the feedback bandwidth, but with no fundamental limits to achieve stabilization up to $\frac{1}{\Delta t} \sim 61$ kHz, resilient to acoustic and mechanical perturbations.

The Ramp instrument was used for PDH spectrum acquisition, configuring the triangle functions ramp_A and ramp_B with a proportional relation ramp_B_factor tuned for optimal mode-hop-free scanning. The proportional constant was selected considering the hardware configuration option selected. The feedback scheme was built using one error signal and two PIDs, one for each ctrl signal. The PID for current setup used proportional and integral terms, while PZT PID only used integral term, avoiding undesired fast corrections over the piezoelectric line. Sample transmitted and error signal are presented in figure 12 for one FP transmission peak, showing the characteristic PDH pattern.

Next, we will present two advanced usage cases of the toolkit for continuous data acquisition and re-lock procedures.

1. Allan deviation: in-device measurements

A measurement of the Allan deviation was made to make a detailed analysis of the stabilization performance. The Allan deviation $\sigma_y(\tau)$ provides a detailed description of the stability of a system in several orders of magnitude of time. The value $\sigma_y(\tau)$ is the standard deviation of the differences of successive mean values of $y$, presented in equation (4), where $y$ is the fractional frequency of an oscillator under study.

$$\sigma_y(\tau) = \sqrt{\frac{1}{2} \langle (\bar{y}_{n+1} - \bar{y}_n)^2 \rangle}$$ (4)

The measurement of $\sigma_y(\tau)$ requires the continuous acquisition of data channels at high sample rate for long time range. This kind of acquisition cannot be done by the Oscilloscope instrument, limited on total time range, nor by a remote acquisition procedure, with sample rate limited because of high communication latency.

To make this acquisition we implemented an in-device program, running from a Python script in the Red Pitaya operative system. The sample script is published in the on-line documentation. The program consists in a large loop that reads values directly from RAM memory mapped registers that corresponds to the signals that should be saved and prints them on the standard output. This simple approach allows one to redirect the output for local storage or network streaming and remote storage, using the operative system tools. The RAM memory access and the identification of memory addresses are simplified by the usage of the local API. A set of FPGA registers can be frozen for each read procedure, so all the acquired values keep coherence (in the sense that they correspond to the same clock time bin). A 64 bit counter running in the FPGA layer is used to register the accurate internal clock time value of each acquisition.

This implementation allowed to take large measurements of error, ctrl_A and ctrl_B signals with a sample rate of at least 50Sa/s along several hours, which were stored in binary files of hundreds of Mbytes in a remote computer. With this information, the Allan deviation of the fractional frequency of the stabilized laser (calculated from error signal) was measured, shown in figure 13. Also, the ctrl_A and ctrl_B signal allow to estimate the open-loop behavior the laser would have had.
by taking into account the corrected deviations during the stabilization time. The fractional frequency Allan deviation derived from this signals were also plotted. The vertical dashed lines mark the PIDs integrators time constants associated with each ctrl signal, as a reference. For \( \tau_i \) larger than these references, the curves derived from ctrl signals can be interpreted as frequency corrections. The increment on ctrl_A derived values on short times is related with the proportional term of the PID used for current control, and tends to reflect the behavior of error signal. An improvement of three orders of magnitude in the stability at 1 second time range can be seen from the plot.

2. Re-lock system

The Lock-control instrument includes the feature to identify locking events and actuate on them, already described in subsection IIC4. The PDH example provides a case study to test it. With the system locked to a transmission peak, the re-lock tool was configured to trigger when error > 1000 int or when transmitted signal error < 3000 int \( \cong \) 366 mV (gray line). The triangular sweep increase the scan amplitude on each semi-period until it reaches the lock condition again. This feature is described in subsection [ITC4].

IV. CONCLUSION

We presented an embedded toolkit for digital processing, acquisition and feedback control through MIMO control design. The combination of FPGA fast deterministic-timing for signal processing and microprocessor with operative system for overall monitoring and control provides a balance between programmable electronic precision and algorithm versatility. This allowed the implementation of several usage strategies going from simple out-of-the-shelf gross-control to in-device programmed fine-control, as shown the experimental examples.

The in-device operative system provides portability and multi-platform GUI access through web browser. The PIDs, designed to work on several orders of magnitude, enable the usage on several control applications, even beyond the ones belonging to AMO labs presented in this work. The design of two lock-in instruments enabled usage for precision measurements and for large working frequency range, including the possibility of the implementation of the complete PDH modulation and lock-in demodulation at 31.25 MHz in one device, something that had not been reported so far.

The selection of an economical commercial board may ease the acquisition and fast implementation of this toolkit by a third party in new experiments. The toolkit FPGA design and software are in public domain, and even the board operative system and applications framework are open-source, what encourages others to use, modify and add new features or bugfix. Also, the compact design and remote programmable feature make the toolkit useful for mass implementation on experiments with several control systems with centralized monitoring and operation.
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