Pinpointing the Memory Behaviors of DNN Training

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Abstract—The training of deep neural networks (DNNs) is usually memory-hungry due to the limited device memory capacity of DNN accelerators. Characterizing the memory behaviors of DNN training is critical to optimize the device memory pressures. In this work, we pinpoint the memory behaviors of each device memory block of GPU during training by instrumenting the memory allocators of the runtime system. Our results show that the memory access patterns of device memory blocks are stable and follow an iterative fashion. These observations are useful for the future optimization of memory-efficient training from the perspective of raw memory access patterns.

Index Terms—DNN Training, Memory Access Patterns, Workload Characterizing

I. INTRODUCTION

Nowadays, DNNs trend to go deeper and wider for higher accuracy [1], [2]. The statistics from OpenAI show that the computation and memory requirements of DNNs are doubled every 3.4 months in recent years [3]. However, the memory capacity constraint of DNN accelerators limits the upper bound on the size of DNNs that can be offloaded to and trained. For instance, the DRAM size of Nvidia GPU with the latest Ampere architecture is 40GB [4]. Even such a large memory capacity fails to satisfy the demand of some DNNs. For example, the typical Inception-V4 [5] requests up to 45GB of device memory to keep the entire DNN on the GPU during training [6]. It is important to reduce the memory pressures of DNN training. Characterizing the memory behaviors of DNN training is critical to optimize the memory usage of DNN workloads.

II. BENCHMARKING METHOD

To work around the memory pressures of DNN training, we carefully pinpoint the memory behaviors (including malloc, free, read, write) of each device memory block by manually instrumenting the memory allocators of PyTorch’s runtime system. We firstly conduct a case study of the trivial MLP to show the memory access patterns of DNN training. To see where the device memory is spent and which kinds of memory content is the bottleneck, we also make a detailed memory occupation breakdown for the typical linear and non-linear [6] DNNs with different batch size and layer structures.

Fig. 1: Layer topology of MLP. Note that star means the mat_mul operator, plus is add_bias, f is ReLU activation.

III. EXPERIMENTAL RESULTS

Iterative Memory Access Patterns. Due to space limit, we only use a trivial MLP to show the memory access patterns of DNN training (our observations are also applicable to other DNNs). Its layer topology is shown in Fig. 1. The shape of $W_0$ is $(2, 12288)$, $b_0$: $(12288)$, $W_1$: $(12288, 2)$, $b_1$: $(2)$. In Fig. 2, each rectangle represents the memory access to a certain device memory block of GPU. Width of the rectangle is the elapsed time from the allocation time to the free time of current device memory block, which can be regarded as the lifetime of current memory block. Height of the rectangle denotes the size of current device memory block. We observe

Fig. 2: Gantt chart of the first five iterations in MLP training on the Nvidia Titan X Pascal GPU.
that there are obvious iterative memory access patterns in the first five rounds of MLP training. Besides, the overlap between rectangles along the y-axis represents the overlap of the live ranges of different memory blocks. The blank space between two rectangles along the y-axis represents the memory fragments of GPU. We can also observe that there are fewer memory fragments during MLP training.

![Diagram](image)

(a) CDF [7]. (b) Violin plot [8].

Fig. 3: CDF and violin plot of the memory block access intervals in MLP training on the Nvidia Titan X Pascal GPU.

Furthermore, Fig. 3 shows the distributions of these memory behaviors. The access time interval (abbr ATI) is the elapsed time between two adjacent memory access to the same memory block. As presented in Fig. 3b, the ATIs of most memory behaviors range from 10us to 25us, and their distributions are relatively concentrated. Besides, Fig. 3a shows that the ATIs of 90% of the memory behaviors are less than 25us. Suppose we want to reduce the device memory pressure by swapping data back and forth between the host CPUs and the device GPUs [9], [10], the ATI of current device memory block is $T$. Assume the memory bandwidth from device GPU to host CPU is $B_{d2h}$ and that of host to device is $B_{h2d}$. Then the maximum value of memory swapping size $S$ without sacrificing the runtime performance should meet the following equation:

$$\frac{S}{B_{d2h}} + \frac{S}{B_{h2d}} \leq T,$$

$$S \leq \frac{1}{1/B_{d2h} + 1/B_{h2d}}$$  \hspace{1cm} (1)

We measured the `memcpy` bandwidth between the device GPU and host CPU with the `bandwidthTest` tool from CUDA SDK samples [11]. The pinned memory transfer bandwidth from host to the device is 6.3GB/s, from device to host is 6.4GB/s. So the maximum value of memory swapping size without sacrificing the runtime performance is about 79.37KB (by equation 1, $S \leq \frac{25\text{us}}{1/6.4\text{GB/s} + 1/6.3\text{GB/s}} = 79.37\text{KB}$). This is just a drop in the bucket for reducing the memory footprint of MLP training. It seems that memory swapping is promising less.

The detailed memory behaviors of Fig. 4, including ATIs along with the corresponding memory block size in MLP training, show that the ATIs of most memory access behaviors are negligible, which is consistent with the observation from Fig. 3. However, there are some outliers whose access time interval is larger than 0.8s and the corresponding memory block size is larger than 600MB. For example, the ATI and the corresponding memory block size of the red marked outlier is 840211us and 1200MB, respectively. In this case, the boundary data swapping size without sacrificing the runtime performance between the host and device is about 2.54GB (by equation 1, $S \leq \frac{0.8s}{1/6.4\text{GB/s} + 1/6.3\text{GB/s}} = 2.54\text{GB}$), which is much larger than 1200MB. This indicates that these outlier memory behaviors with high ATIs and large memory block size ought to be the focus of attention. They are the major contributors in terms of reducing the memory pressure of DNN training. In the future, we plan to build an automatic cost model to sift out these memory access behaviors to reduce the device memory pressure during training.

**Device Memory Occupation Breakdown.** During training, the memory consumption falls into three categories from the perspective of device memory storage contents, i.e., input data, parameters and intermediate results [12]. We observe from Fig. 5 that, for most DNNs, parameters only account for a small fraction of the total memory footprint during training. This indicates that weight pruning or quantization techniques are not efficient for reducing the memory pressures of DNN training [13], [14]. In training, the intermediate results are the primary contributor to the device memory footprint. To show the detailed effects of datasets, batch size and model layer structures over the memory footprint, we explored the enumeration space of these involving factors. Due to space limit, we only report the data of one linear DNN (AlexNet [15]) and one non-linear DNN (ResNet with different numbers of residual layer blocks [16]) with CIFAR-100 and ImageNet dataset under different batch size. As shown in Fig 6, for AlexNet, with the growth of batch size, those intermediate results gradually dominate the device memory consumption and the occupation of parameters is gradually weakened. Meanwhile, the impact of input data increases slightly. This observation is also applicable to the non-linear ResNet with different numbers of residual layer blocks (Fig. 7).

**IV. Conclusion & Future Directions**

From our characterizing results, we highlight the following observations. The memory behaviors of DNN training illustrate obvious iterative patterns (Fig. 2). Besides, the distributions of the ATIs of most memory behaviors are relatively concentrated. Especially, the ATIs of most memory access behaviors are negligible, which can be filtered out by the bandwidth between host and device memory (Fig. 3). Most importantly, those outlier memory behaviors with high ATI and large memory block size ought to be the focus of attention (Fig. 4). They are the major contributors to reduce the memory pressure of DNN training.

Based on these observations, and inspired by the swapping-based memory pressure reduction schemes [9], [10], we plan to propose a more general approach that takes the memory access patterns as input to automatically address the device
memory pressure issues of DNN training with small runtime overhead.

Fig. 4: Pair-wise ATI and the corresponding device memory block size of each memory behavior during MLP training on the Nvidia Titan X Pascal GPU. Note that the x-axis is the index of each memory behavior.

Fig. 5: Memory occupation breakdown of typical DNN training on the Nvidia Titan X Pascal GPU.

Fig. 6: Memory occupation breakdown of linear DNN (AlexNet) with different batch size.

Fig. 7: Memory occupation breakdown of non-linear DNN (ResNet) with different layer structures (ResNet18, 34, 50, 101, 152).

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