Design of double ring lock ring in extensible frequency clock generator chip

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Abstract: With the continuous development of computer technology and the continuous improvement of interface data rate, the clock frequency has reached the demand of several gigahertz, which makes the electromagnetic interference problem very serious. Spread spectrum clock is an effective method to reduce electromagnetic interference of digital chips. Therefore, this paper designs a double-loop phase-locked loop that can spread spectrum and has strong anti-electromagnetic noise interference ability. The designed dual-loop phase-locked loop can be used in the clock generator chip. The overall structure of the circuit consists of a main loop and a secondary loop. The main loop is an adjustable phase-locked loop circuit that can provide an output with a center frequency of 500MHz. The secondary loop can realize the spread spectrum function by charging and discharging the filter capacitor of the main loop loop, and at the same time, the spreading depth can be set by the feedback based on the frequency division. The dual-loop phase-locked loop designed in this paper has a good effect in spread spectrum and anti-electromagnetic interference noise.

1. Introduction

Today's computer technology continues to develop, and high-speed data transmission is used more frequently in computer technology. Therefore, with the continuous improvement of the interface data rate, the clock frequency has reached the demand of several gigahertz, which makes the chip electromagnetic interference problem very serious. How to eliminate electromagnetic interference is a hot issue in current research. Clock spread spectrum is a very suitable technical method to solve this problem. The application of clock spread spectrum to clock generator chip technology can be studied in depth. The clock generator chip is widely used in a circuit in various fields, which is an important part of the entire circuit structure [1]. The clock generator can stabilize the clock frequency pulse signal, and the composition of the product component needs this clock [2][3]. For digital chips, for the control of the clock, the accurate and error-free processing for various digital signals can be performed, and if the clock chip generated, the clock signal generated will cause huge errors to the processing of the digital signal. The core module in the entire clock chip is the design of the phase-locked loop, the conventional single-loop lock loop in the realization of the capacity of the exhibition [4] and the electromagnetic interference ability [5] [6]. The dual-loop phase-locked loop designed in this paper is improved on the original single-loop phase-locked loop[7] [8], and the spread spectrum and anti-interference effect have been greatly improved, and the timeliness and accuracy of the entire clock chip have been better improved[9].
2. Design of double ring lock ring
The block diagram of Figure 1 is a functional block diagram of a double-ring lock ring design in this paper. The two cyclo lock ring is mainly a primary loop and a sub-loop configuration. The main loop is a modulatable phase-locked loop circuit, mainly by passing the phase of the camera PFD, the charge pump CP1, the loop filter LPF, the voltage of the embedded loop, based on the voltage controlled oscillator based on the ring oscillator VCO and digital logical frequency divider are composed. The sub-loop is charged with the main loop filter capacitor charging and discharge, and the extension depth is set by the feedback based on the frequency division (time).

![Figure 1 Function block diagram of the double ring lock](image)

3. Main module circuit design

3.1 Tannaming Fair design
The PFD structure in the double-ring lock in this paper is shown in Figure 2. This paper is designed with the syncatoscopes of nine and non-door structures. The signals thereof include REF and DIV signals. When the REF signal is leading the DIV signal, the period pulse signal of the UP signal is output, and the period pulse of the DN signal is output. Signal.
3.2 Charge pump design

The circuit structure of the charge pump is shown in Figure 3. The pump can be described as a circuit composed of two switched current sources, and the output UP and DN signals of the diagram and DN signals respectively control the two current sources of the charge pump, which controls the current source to filter capacitance. Charging and discharging. Transform the width of the phase difference pulse into the average voltage of the control VCO. For the core module charge pump of the phase-locked loop, focus on their current loss. The target is to obtain a good current pump that pulls the match with the pull-down current in a wide output voltage range. The vertical cascade structure (Cascode structure) of the charge pump in this design is to perform such a designed purpose is to make the output resistance of the small signal of the Cascode structure of the common source, which makes the output current more stable.

3.3 Circuit design of voltage controlled oscillator

The VCO circuit structure is shown in Figure 4 below. By shown below, the VCO circuit structure design of this paper is connected in series by five inverters, and by the structural circuit design is to output 500 MHz oscillation frequency.
3.4 Frequency Function Circuit Module Design
The circuit design of the exhibition is shown in Fig. 5, which is the principle of the circuit to change its output frequency by directly changing the control voltage of the circuit VCO, and changes its output frequency; ensuring that the bandwidth of the main loop is much smaller than the modulation voltage. The frequency, the adjustment signal can be injected normally. Building a circuit structure to achieve the function of the frequency of the frequency through this principle.

4. Experimental simulation results
This article simulates the design of the two-ring lock in the simulation software. When the sub-ring charge current is 75-Na, the output extension depth is approximately 0.5%, and the output spectrum (including noise) is as follows:
5 Conclusion

With the continuous development of computer technology and the continuous improvement of interface data rate, the clock frequency has reached the demand of several gigahertz. How to better solve the electromagnetic interference technology is the focus and difficulty of research. Clock spread spectrum technology is an effective method to solve this problem. The dual-loop phase-locked loop designed in this paper with spread spectrum and strong anti-electromagnetic noise interference ability can meet the requirements after simulation verification results, and can be further tested and verified in the actual chip.

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