Accelerating Binarized Neural Networks via Bit-Tensor-Cores in Turing GPUs

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Abstract—Despite foreseeing tremendous speedups over conventional deep neural networks, the performance advantage of binarized neural networks (BNNs) has merely been showcased on general-purpose processors such as CPUs and GPUs. In fact, due to being unable to leverage bit-level-parallelism with a word-based architecture, GPUs have been criticized for extremely low utilization (1%) when executing BNNs. Consequently, the latest tensorcores in NVIDIA Turing GPUs start to experimentally support bit computation. In this work, we look into this brand new bit computation capability and characterize its unique features. We show that the stride of memory access can significantly affect performance delivery and a data-format co-design is highly desired to support the tensorcores for achieving superior performance than existing software solutions without tensorcores. We realize the tensorcore-accelerated BNN design, particularly the major functions for fully-connect and convolution layers — bit matrix multiplication and bit convolution.

Evaluations on two NVIDIA Turing GPUs show that, with ResNet-18, our BTC-BNN design can process ImageNet at a rate of 5.6K images per second, 77% faster than state-of-the-art. Our BNN approach is released on https://github.com/pnnl/TCBNN.

1 INTRODUCTION

BINARIZED-neural-network (BNN) [1, 2, 3] is an alternative type of deep-neural-networks (DNNs). Compared to general DNNs, such as multi-layer-perceptrons (MLPs) and convolution-neural-networks (CNNs), the major difference of BNN is that it uses a single bit to represent each entry of the input and weight matrices. BNN evolved from DNN through binarized-weight-network (BWN) [4]. It was firstly observed that if the weight matrix can be binarized to +1 and −1, the floating-point (FP) multiplications can be degraded to addition (i.e., mul +1) and subtraction (i.e., mul −1). Later, it was further observed that if the input matrix can be binarized as well, then even the floating-point additions and subtractions in BWN can be degraded to logical operations (i.e., xnor for bit dot-product and popc for bit accumulation) [1, 2, 3].

BNNs bring several advantages over full-precision DNNs: (a) Reduced and simplified computation. Through binarization, each segment of 32 FP fused-multiply-add (FMA) operations can be aggregated into an xnor operation and a popc operation, leading to theoretically 16× speedups; (b) Reduced data movement and storage. Through binarization, the whole memory hierarchy and network, including registers, caches, scratchpad, DRAM, NoC, etc. can accommodate 32× in both bandwidth and capacity; (c) Reduced cost which comprises energy reduction from simplified hardware design and smaller chip area; (d) Resilience. It has been reported that compared with differentiable DNNs, the discrete BNNs exhibit superior stability and robustness against adversarial attacks [5, 6].

On the flip side of the coin, binarization reduces the model’s capacity and discretizes the parameter space, leading to certain accuracy loss. With the tremendous effort from the machine learning community [2, 7, 8, 9], accuracy of BNNs have been dramatically enhanced. The top-1 training accuracy of BNN-based AlexNet and ResNet-18 on ImageNet dataset has achieved 46.1% [8] and 56.4% [10] (54.3% and 61% with boosting [11]), with respect to 56.6% and 69.3% for full-precision DNN [12]. A latest BNN work even reported a top-1 accuracy of 70.7% [13].

Although BNN is not likely to substitute DNNs because of reduced model capacity, for many HPC [14, 15, 16, 17] and cloud applications [18, 19], when certain accuracy levels can be achieved, alternative factors such as latency, energy, hardware cost, resilience, etc. become more prominent. This is especially the case for practical deployment.

Despite featuring various advantages, the expected performance gain of BNN has rarely been demonstrated on general purpose processors such as GPUs. This is mainly because: (i) the fundamental design mismatch between bit-based algorithms and word-based architecture; (ii) BNN designs at this stage are mainly driven by the algorithm community on how to improve training accuracy; little system and architectural support have been provided on high performance delivery. Due to (i), most existing BNN implementations are realized as hardware accelerators (e.g., through FPGA [20, 21, 22, 23, 24, 25]) where the operand bit-width can be flexibly adjusted. Due to (ii), BNN developers are still relying on full-precision software frameworks such as TensorFlow and PyTorch over CPUs and GPUs to emulate the BNN execution. As a result, the lack of architectural & system support hinders the performance delivery and the general adoption of BNNs.

This situation has been lately changed for GPUs. On the software side, a recent work [26] proposed the so-called binarized software tensor core or BSTC, relying on GPU’s low-level hardware intrinsics for efficient 2D bit-block processing, such as bit matrix multiplication (BMM) and bit convolution (BConv). On the hardware side, the latest NVIDIA Turing GPUs started to support BMM experimen-
and throughput constraints when deploying BNNs in HPC, and energy cost [20], [21], [22], [23], [24], [25], [26], [27], [28], [29]. Most of these implementations focus on FPGA [20], [21], [22], [23], [24], [25] due to FPGA’s design flexibility at the bit level. Regarding general-purpose platforms, an existing CPU work [41] relies on the AVX/SSE vector instructions to derive good bit computation performance. It focuses on BMM and transforms bit-convolution to BMM through im2col() with costly pre- and post-processing. Another evaluation work [22] compares CPU, GPU, FPGA and ASIC based BNN designs, clarifying that the major performance restriction of CPUs and GPUs is the extremely low utilization due to the challenge in extracting fine-grained parallelism. Noticeably, the reported GPU utilization is 1% only [22]. To improve GPU utilization and extract bit-level-parallelism, a recent work [26] proposed the binarized-soft-tensor-core (BSTC) on top of GPU’s SMs and leverages low-level hardware intrinsics for harvesting the bit-processing capability of GPUs. For BSTC, the performance gains from better utilization of the conventional integer/logic units (i.e., INTUs and SFUs, see Figure 1). This work is different because we focus on the brand new bit computation capability of the latest Turing TCUs, and showcase how to harvest the most performance from this new functional units.

**GPU Tensorcore** Driven by the demand of training large-scale DNNs, designing specialized low-precision dense matrix-matrix multiplication accelerators has become a popular trend. Particularly, Google presented Tensor-Processing-Units (TPUs) [43]; Intel announced the Nervana Neural-Network-Processors (NNPs) for tensor operations; NVIDIA integrated the Tensorcore Units (TCUs) into their Volta and Turing GPUs; Qualcomm included the Hexagon-Tensor-Accelerator (HTA) into their Hexagon 855 system-on-chip.

This work focuses on the tensorcores of GPUs (see Figure 1). Since being firstly introduced in the Volta architecture [44], the tensorcore becomes one of the spotlight for GPGPU research. The relevant works can be summarized in two categories: (a) **Characterization.** In [45] and [46], Jia et al. dissected the Volta (Tesla V100) and the Turing (Tesla T4) GPUs through microbenchmarking. They depicted the detailed mapping mechanism from elements of a matrix tile to registers of a warp-lane in the HMMA instructions for FP16 matrix multiplication. They found that the 32 threads of a warp are essentially divided into 8 thread groups, where the 4 threads per group cooperatively work on the same regions of matrix $C$ by fetching elements from different parts of matrix $A$ and matrix $B$. Markidis et al. [47] studied the programmability, performance and precision of the

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**TABLE 1: Bit-Software-Tensor-Core (BSTC)** [26] vs. Bit-Tensorcore (BTC). **unit32** refers to unsigned int, **unit64** refers to unsigned long long int. **INTU** refers to integer units. **SFU** refers to special function units.

| Functionality | BSTC | BTC |
|---------------|------|-----|
| Bit-Matrix Multiplication | Bit Matrix Multiplication | Bit Matrix Multiplication |
| Tile-A size | 32 x 32 or 64 x 64 | 8 x 128 |
| Tile-B size | 32 x 32 or 64 x 64 | 128 x 8 |
| Tile-C size | 32 x 32 or 64 x 64 | 8 x 8 |
| Hardware units | INTUs and SFUs | TensorCore Units (TCUs) |
| Processing level | per warp | per warp |
| GPU Platforms | Kepler or later (≥CC-3.0) | Turing GPUs (≥CC-7.5) |

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1. To the best of our knowledge, this feature has not appeared in vendor’s library like cuBLAS, cuDNN, TensorRT or other library up to now except Cutlass in which it is supported as an experimental, unverified function.
Volta tensorcores and proposed a technique to compensate the accuracy loss due to precision degradation from FP32 to FP16. Raihan et al. [45] investigated the design details of the tensorcores in Volta and Turing GPUs and built an architecture model for the tensorcores in GPGPU-Sim. They characterized the WMMA APIs and clarified how the operand sub-matrix elements were mapped for FP16 GEMM in Volta tensorcores, and FP16/Int8/Int4 GEMM in Turing tensorcores. However, they did not investigate the 1-bit computation mode. Hickmann and Bradford [49] proposed a testing method for assessing the compliance of IEEE standard, hardware microarchitecture, and internal precision of the Volta tensorcores. (b) Application. Haidar et al. [50] proposed a mixed-precision iterative refinement method to approach FP64 precision using FP16-based GPU tensorcores in LU factorization, acting as the first effort to apply GPU tensorcores for non-machine-learning applications. Sorna et al. [51] applied FP16 tensorcores for FFT acceleration. Blanchard et al. [52] thoroughly analyzed the rounding error of matrix multiplication and LU factorization when using the tensorcores. Dakkak et al. [53] showed that the tensorcores, which were originally designed for 2D FP16 GEMM, can be adopted for 1D array reduction and scan.

Most of these works, however, focused on FP16 mixed-precision matrix-multiply in Volta tensorcores. They either evaluated their performance, programmability, accuracy, hardware design, or looked into alternative applications other than GEMM, aiming to preserve higher precision. None of them have investigated the latest bit computation capability of the GPU tensorcores. In addition, no existing works have ever reported the potential performance impact from the stride of segmented memory load, and how to circumvent the challenges in accelerating convolutions through the tensorcores. Furthermore, until writing the paper, we have not seen any works leverage GPU tensorcores for the acceleration of BNNs.

3 GPU Bit Tensorcores

3.1 GPU Tensorcores

Since the Volta architecture (CC-7.0), NVIDIA GPUs have introduced a novel type of function units known as Tensorcores into the streaming multiprocessors (SMs) for accelerating low-precision general matrix multiplication (GEMM). In Volta, each tensorcore processes 64 FP16 FMA operations per cycle [54]. The only supported datatype for Volta tensorcores is FP16. For Turing (CC-7.5), more datatypes are supported, including FP16, signed/unsigned int-8, int-4, and recently a bit as well. Please refer to [45], [48], [54] for more details about the hardware features of Volta and Turing GPU tensorcores.

3.2 CUDA WMMA

Since CUDA Runtime-9.0, the Warp Matrix Multiplication API (WMMA) has been introduced for operating the tensorcores in Volta and Turing GPUs. The idea is to partition the three input and one output matrices into tiles, where each warp processes the multiplication of one tile \((T_D = T_A \times T_B + T_C)\). WMMA provides the necessary primitives to operate on the bit-tiles (e.g., loading input tiles, tiled multiplication, storing output tile): load_matrix_sync,mma_sync,store_matrix_sync. These primitives are executed by the 32 threads of a warp cooperatively. For FP16, the tile is further partitioned into 32 fragments while each thread fetches a fragment of data into its register files. Although the vendor’s official documents have not revealed the exact mapping schemes, existing works have figured them out through microbenchmarking [45], [48].

3.3 Cutlass Library

Currently the vendor’s high-performance linear-algebra library cuBLAS has not supported BMM on Turing tensorcores. However, their open-source GEMM library – Cutlass [31] has integrated it as an experimental and non-verified feature. BMM is realized using the WMMA API. The input matrix \(A\) is in row-major bit format (compacted as 32-bit unsigned int), \(B\) is in column-major bit format (also compacted as 32-bit unsigned int). The accumulated input matrix \(C\) and the result matrix \(D\) are in row-major 32-bit signed int format. \(C\) and \(D\) are usually the same matrix. BMM in Cutlass conducts 0/1 dot-product while BNN demands +1/-1 dot-product, we discuss this later.

4 BTC CHARACTERIZATION

To operate on the bit datatype for Turing GPUs, CUDA WMMA defines the 1-bit precision and the bit operations in an independent “experimental” namespace, as listed in Listing 1. XOR and POPC for bits (+1/-1) correspond to multiply and accumulate for floating-point/integer datatypes.

Five APIs are provided for loading the bit-tile \(A\), the bit-tile \(B\), the int-tile \(C\), and storing the int-tile \(D\), as well as the multiplication: \(D = C + A \times B\). For the bit-matrix-multiply-API (BMMA), only a single computation paradigm is defined: the bit-tile \(A\) is in row-major of size \((8, 128)\), the bit-tile \(B\) is in column-major of size \((128, 8)\); the int-tile \(C\) and \(D\) are square matrices in row-/column-major of size \((8, 8)\). The bit-tile \(A\) and \(B\) are compacted as 32 unsigned ints, each with 32 bits. Therefore, the bit-tile \(A\) and \(B\) each occupies 128 bytes. The int-tile \(C\) and \(D\) each occupies \(8 \times 8 \times 4 = 256\) bytes. Listing 2 shows the Parallel Thread Execution (PTX) – the low-level GPU virtual machine ISA code for the five BMMA APIs. The shape qualifier “m8n8k128” in Line 2-6 indicate that the bit-tile-multiplication processed per warp is in size \((8,128) \times (128,8)\). “sync” means the instruction wait for all warp lanes to synchronize before proceeding. The “layout” qualifier specifies if the tile is stored with a row-major or column-major order in memory. “type” indicates the precision of the tile. Using int32 for tile-C and D is to avoid potential overflow during the accumulation.
For matrix-multiplication, tile-C and tile-D are usually in the same size. Thus, the five APIs can be categorized into three groups: load, store, and computation. We investigate each of them in the following subsection to figure out potential design guidelines. Regarding the hardware platform, see Section VII and Table 2.

4.1 BMMA Load

We first concentrate on bmma_load, as memory load is the most crucial factor for GEMM on GPU. The load API is:

```c
void bmma_load_sync(const fragment &tileA, const fragment &tileB, const fragment &tileC, layout layout);
```

It waits for all the threads of a warp to arrive, and then loads a bit tile (i.e., a matrix fragment) from the device memory. It has three parameters. “mem_ptr” is a 256-bit aligned pointer pointing to the first element of the matrix in memory. The memory here can be global or shared memory. “layout” can be row- or column-major, but for BMMA, there is only a single choice — mem_row_major for matrix-A and mem_col_major for matrix-B. “ldm” is the stride in element between consecutive rows (in row major) or columns (in column major) and must be a multiple of 16 bytes), according to [56]. We find that for shared memory, this is the case; but for global memory, a multiple of 32 is also feasible (despite with unpredicted results). To see the impact of mem_ptr (i.e., memory type) and ldm on the performance of the load primitive, we measure its average per-thread latency using the clock() instruction. We add a memory fence operation before the measurement to ensure that the data fetching has finished.

Figure 2, 3, 4, 5 show the average latency with respect to different values of ldm for load_matrix_sync() on global and shared memory of RTX-2080 and RTX-2080Ti GPUs. As ldm is the stride between consecutive rows of the matrix, it should be application dependent (e.g., for a 1024 × 1024 × 1024 BMM, ldm should be 1024) and the raw latency should be irrelevant to ldm. However, counterintuitively it has a strong impact on the performance of fetching a bit-tile from the global memory. As can be seen in Figure 2 and Figure 4 ldm=128 and ldm=384 exhibit the shortest latency. Regarding shared memory, (1) accessing shared memory exhibits more than 5x less latency than accessing global memory; (2) the latency for RTX2080Ti is less than RTX2080, and is unchanged with ldm.

We then consider “tileA”, and see how the bit-tile (128×8 bits) is distributed among the lanes of a warp. Similar to [49], we let each lane print out the value of data it fetches. Based on the value, we can identify the mapping mechanism. We find that, similar to FP16 and Int8, lanes in BMMA also establish 8 thread groups — 4 consecutive lanes per group. Each thread group corresponds to a 128 bit row. Within a 128 bit row, each lane accounts for a 32-bit portion (4 bytes). This partially explains why ldm=128 delivers the shortest latency: the 32 lanes of the warp constitute a coalesced memory access, where the 32 4-byte access are merged as a single memory request. Regarding why ldm=384 also exhibits good performance, we suspect this might be because the Turing L1 data cache is essentially partitioned into two sectors with independent ports, similar to the L1/Tex cache in Maxwell and Pascal GPUs. It conserves the data in an interleaving way at a step of 32B. Consequently, ldm=256 (32B) may trigger a sector-port conflict for simultaneous memory fetches from the same warp but ldm=384 may not. This is confirmed by the observation that ldm=128+256×x (e.g., 384, 640, 896) all demonstrate relatively low latency in Figure 2 and 5.

4.2 BMMA Store

The store operation is different from load in that every element is a 32-bit signed integer. The store API is:

```c
void bmma_store_sync(const fragment &tileA, const fragment &tileC, unsigned ldm, layout layout);
```

Again, it waits until all warp lanes arrived before storing tileC into memory. “mem_ptr” must be a 256-bit aligned pointer referring to the first element. “ldm” describes the stride in elements between consequent rows in C, and must be a multiple of 16 bytes (with integer, it corresponds to 4 elements). “layout” can be row-major or column-major.

We measure the average latency with respect to the stride ldm on global and shared memory of RTX-2080 and RTX-2080Ti GPUs, as shown in Figure 6, 7, 8, 9, respectively. Unlike load, the latency histograms for store do not exhibit obvious patterns. We also attempt to figure out how the resulting int-tile tileC is distributed among the lanes. Our findings show that: (i) If it is row-major, then within the 8 × 8 int tile, each two consecutive elements (from a row) are stored in two adjacent registers of a lane. For example, suppose the 8 × 8 elements are E0 to E63 and each lane uses R4 and R5 to store the integer tile, then (E0, E1) are stored in R4 and R5 of lane-0, (E2, E3) are stored in R4 and R5 of lane-1, and so on. (ii) If it is column-major, then each two consecutive elements (from a column) are stored in two adjacent registers of a lane (i.e., transposed from the row-major layout). When storing, the two adjacent registers are encoded as one STG.E.64 memory store for the entire warp, as if storing an FP64 data.

4.3 BMMA Computation

Finally, we discuss the bit-matrix-multiply API:

```c
void bmma_bit_opx(const fragment &tileA, const fragment &tileB, const fragment &tileC, layout layout)
```

It waits until all lanes arrive before computing the BMMA operation: tileD = POPC(tileA XOR tileB) + tileC. Unlike the condition for FP16 and Int8 where a group of SASS assembly operations are generated [45, 46, 48], bmma_sync is only translated into a single SASS code:

```asm
BMMA.BB8128.XOR.POPC R2, R6, ROWN, R9, COL, R2;
```

Our idea here is to measure its raw latency and estimate how much parallelism, including warp-level-parallelism (WLP) and instruction-level-parallelism (ILP), are required to saturate the tensorcore pipeline and hide the latency.

Figure 10, 11, 12, 13 illustrate the total latency of increasing the number of repeated bmma_sync operations for the same tileC/tileD, and different tileC/tileD on the two GPUs. The raw latency of bmma_sync is ~201 cycles on RTX2080 and ~190 cycles on RTX2080Ti. As shown in the figure, the incremental latency with each one more bmma_sync operation is 10 cycles when tileC & tileD are identical for all operations, and is 4 cycles when tileC & tileD are different on both platforms. This implies that the pipeline stage delay is around 4 cycles. When using the same accumulator, 6 extra
cycles are needed. Given the raw latency of ~200 cycles, and the fact that Turing GPU SM comprises four sub-cores (each subcore can issue one instruction per cycle), with at maximum 32 warps per SM for Turing (so WLP=32), we roughly require ILP=200/4×4/32=7 to saturate the entire tensorcore pipeline. In other words, with 8 independent *bmma_sync* operations, we should approach the theoretical computation bandwidth of the tensorcores.

5 MBM and BConv with BTC

We present our designs for BTC-based BMM and BConv, which are the core functions for the fully-connected layer and convolution layer of BNNs.

5.1 FSB Data Format for BTC

In Section IV-A, we have observed that the value of *ldm* can strongly affect the performance of *load_matrix_sync* from global memory, where *ldm*=128 and 384 exhibit the best performance. Our idea thus is whether we can essentially fix the value of *ldm* firmly to 128 or 384. As a result, rather than storing the bits completely sequential and using the matrix width for *ldm*, as practiced by the Cutlass library and suggested by CUDA programming guide, we propose a new 2D bit data format where bits are stored in a unit of 128 × 8 bit-tile. An analogous example is shown in Figure 14.

From the 1D general format to the 2D new format, an array of 8 × 4 bits (H=4, W=8) is converted with a tile size of 4 × 2 (BH=2, BW=4). For BTC, since 384 is not a power of 2, dividing 384 may incur troublesome reminder handling, we thus use 128 as BW and 8 as BH for the new format. If the original bits are organized in row-major, both the inner and tile-wise order of the new format are in row-major (as the case in Figure 14); otherwise, both are organized in column-major. Since the new format only changes the way how bits are stored and fetched, no extra space is needed. However, if the width of the original matrix (i.e., W) cannot be divided by 128 (i.e., BW), for the convenience of index calculation, we pad the row to be a factor of 128, which may occupy some extra space. Note, in order to load via *load_matrix_sync*( ), such a kind of padding is required anyway. Similar requirement has been imposed by *pitch* in *cudaMempcy2D*( ). The temporal overhead only occurs at array index calculation, which is almost negligible.

5.2 BMM for FC Layer

BMM in BNN is different from GEMM because: (a) Input. The elements of matrix-A and B are binary values: +1 and -1. A normal floating-point or int number is binarized via:

\[ x^b = \text{sign}(x) = \begin{cases} 1 & \text{if } x \geq 0 \\ -1 & \text{otherwise} \end{cases} \]

In an FC layer, both A and B have to be binarized ahead of BMM. However, the binarization of B (i.e., weights) can be performed offline after the training; only the binarization of A is in the critical path of inference. Existing work has shown that such a binarization can be achieved efficiently through the _ballot_ function of GPUs [26]. (b) Computation. The dot-product of GEMM is \( y_{i,j} = \sum_{k=0}^{n} a_{i,k} b_{k,j} \) where \( n \) is the vector length. In terms of BMM, as a and b become bit-vectors, if using bit-1 to denote +1, and bit-0 to denote -1, it can be shown that the \( \pm \) dot-product becomes:

\[ v = a \cdot b = n - 2 \times \text{popc}(a \text{ xor } b) = 2 \times \text{popc}(a \text{ xor } b) - n \]

where \( n \) is the bit-vector length. xor and xnor are logical exclusive-or and exclusive-nor. The xnor expression has widely been used for BNN algorithm research [1], [3] and
Listing 3: BMM baseline implementation

FPGA/ASIC implementation [20], [21] while GPU tensorcores currently only support xor for bit computation. popc stands for population count, which counts the number of bit-1s in the bit vector. (c) Output. The elements of the output matrix-C are full-precision integer values. However, in an FC layer, it can be binarized after a threshold operation (discussed later), reducing memory access. Therefore, the third difference with GEMM is that the output-C can be binarized before the store.

Design-1 Now we present our three BMM designs based on WMMA, which is the only API for operating the tensorcores. The baseline design is shown in Listing 5. Each thread block comprises two warps and each warp processes BMM for a 128×8-bit tile in Line 10. Having two warps per thread block is for achieving the full occupancy of Turing SMs.

Design-2 As memory load is the most important factor for matrix multiplication on GPU [55], Design-2 aims at improving the efficiency of memory load. On one hand, using a whole warp to fetch only 128 bits is too lightweight. On the other hand, if coalescing memory access is enforced with each lane fetches 32bits, the total bit length becomes 32×4×8=1024 bits, which is probably too coarse-grained for a BNN FC layer given the matrix size is usually less than 2048. Therefore, motivated by [48], we increase the load granularity per warp-lane to its max value of 128 bits, leveraging the effective LDG.E.128 SASS instruction. With each lane fetching 128 bits, a warp of 32 lanes would fetch a bit segment of 4096 bits, which is sufficient for 4 warps to perform WMMA simultaneously. As a result, we use a representative warp to fetch 4096 bits of A and 4096 bits of B from global memory to shared memory, which are then dispatched to 16 warps for WMMA execution, as listed in Listing 4. Essentially, each thread block processes a BMM of (128×32)×(32,128) while each warp processes (128,8)×(8,128). Line 11-12 show how to invoke 128-bit global memory load through vectorization [45]. Note that

Listing 5: BMM in new format with binarized output

load_matrix_sync

Selecting FLIPBIT(S)苯 (16<<((b1−b2)−1) flip the last b bits of a

global void BMM(uint32_t A, uint32_t B, uint32_t C, int A_width, int B_width, int C_width)

Listing 6: BTC-based BConv design

load_matrix_sync

5.3 BConv for Convolution Layer

The convolution operation here is to cross-correlate a 4D input tensor (batch, input_height, input_width, input_channels) with a 4D weight tensor (weight_height, weight_width, input_channels, output_channels). We use H to denote input_height, W to denote input_width, N to denote batch, C to denote input_channels, K to denote weight_height and O to denote output_channels. TensorFlow uses NHWC for input and KCKC for filter. PyTorch uses NCHW for input and OCKK for filter. Traditionally, a 2D convolution can be transformed
into GEMM through the \textit{im2col} process \cite{17,18}, which can then be accelerated by the tensorcores. However, for BConv, directly converting to BMM is not feasible due to the challenge in padding \cite{28}. Different from normal convolution where the padded zeros shall not affect the correctness, in BConv the element zero actually denotes -1. Therefore, after the \textit{im2col} process, we are unable to distinguish the padded 0s from the meaningful zeros representing -1, leading to inaccurate results.

Thus, the objective here is how to design BConv so that the padding issue can be well-managed but can still be accelerated by the bit tensorcores of Turing GPUs. On one hand, motivated by existing work \cite{26}, if the entire filter window is processed sequentially by a single GPU thread, a status variable can be allocated to track how many entries of the filter window fall out of the frame of the input image, which can be used later to make an amendment accordingly for ensuring the correctness of bit-padding. On the other hand, if we ignore the image size and filter size for now but looking at a particular point \([i,j]\) of the input image, the batch of \(N\) images at that point cross-correlating with an entry of the filter window \([r,s]\) is essentially to calculate the following output point \([p,q]\):

\[
\text{Output}_{[p,q]} = \sum_{k=1}^{C} \text{input}(N,k)_{[i,j]} \times \text{filter}(k,O)_{[r,s]} \quad (3)
\]

This is just equivalent to multiplying a bit matrix in size \((N,C)\) with another matrix in size \((C,O)\), which can be performed by the bit-tensorcores. To summarize, our idea is to change the input tensor to \texttt{HNWC}, the filter tensor to KKCO, and perform BMM along the last two dimensions of these two tensors.

Our first design is shown in Listing 6. We use each warp to traverse the input channel space at Line 28 and perform the computation for 8 input images over 8 output_channels (i.e., \((8, C) \times (C, 8))\) using the bit-tensorcores in Line 30-32. We use “exclude” to track the number of entries outside the filter frame at Line 33 and amendment the results at Line 36 for padding and the ±1 logic (see Eq 2). We use \(c\_frag\) for storing the partial results of convolution. Eventually, the \(8\times8\) resulting matrix tile stored in \(c\_frag\) is written back to the global memory in row-major at Line 38-39.

Our second BConv design leverages the new bit data format. We reform the last two dimensions of the input tensor \((N,C)\) in a bit-tile of \(128\times8\) bits in row-major, and the filter tensor \((C,O)\) in a bit-tile of \(128\times8\) bits in column-major. Then, we can adjust the \(ldm\) in Line 30-31 from “\textit{in\_channels}” to 128, later we will see the impact of this adjustment.

6 BNN Design with BTC

We present the overall BNN structure and our BTC-based BNN implementation.

6.1 BNN Network Structure

Figure 15 illustrates the network structure of an example ResNet. To avoid losing too much non-recoverable information at the beginning, if the input images are in full-precision (e.g., after preprocessing), the first layer of BNN is not binarized \cite{2,3,7}. BWN is adopted here in which only the weight matrix is binarized. Consequently, we are unable to use BTC to accelerate the first layer. Also because the input channels of the first layer is usually very small (e.g., red, green, blue), to avoid alignment issue and fully leverage data locality, we binarized the weight matrix into a 4D bit tensor in KKCO format and buffer the weight into the shared memory for reuse. Then, by extracting each bit of the weight, depending on whether it is 1 or 0, we add or subtract the corresponding element of the input matrix. The output matrix is binarized and stored in particular bit-format as the input for the next layer.

Shown in Figure 15 regarding training, a BNN convolution layer typically comprises binarization \((\text{sign})\), bit-convolution \((\text{conv})\), batch-normalization \((\text{bn})\), hard-tanh \((\text{tanh})\), and pooling \((\text{pool})\). Binarization is the sign function following Eq 1. Batch-normalization \((\text{BN})\) is to reduce the batch noise:

\[
y_{i,j} = \frac{x_{i,j} - \mathbb{E}[x_{i,j}]}{\sqrt{\text{var}[x_{i,j}]} + \epsilon} \cdot \gamma_j + \beta_j \quad (4)
\]

Note that \(\text{bn}\) is essential for BNNs, as missing it will render the training unable to converge. Additionally, having \(\text{bn}\) brings two extra benefits: (1) bias is thus not necessary for the bit convolution or fully-connected layer, as bias can be integrated with \(\beta_j\) in Eq 3; (2) the scaling layer proposed in \cite{3,7} for BNN is also not necessary as it can be integrated with \(\gamma_j\) in Eq 4. Hard \(\text{tanh}\) is a piecewise linear function:

\[
\text{Htanh}(x) = \text{Clip}(x, -1, 1) \quad (5)
\]

Since \(\text{tanh}\) is immediately followed by the \(\text{sign}\) function, it has none effect on inference or the forward pass of training. The major purpose of \(\text{tanh}\) is to constrain the gradient of the \(\text{sign}\) function between -1 and +1 in the backward pass \cite{1}. Otherwise, if the full-precision activation is too large, the gradient will be zeroed-out. Additionally, since the \(\text{sign}\) binarization function has already imposed non-linearity into the network, no other activation function such as \text{ReLU} \cite{3} and \text{PReLU} \cite{7} is actually needed for BNN. Conversely, extra activation functions can be harmful based on our tests.

Regarding the order of these functions, it should be \(\text{tanh}\rightarrow\text{sign}→\text{bconv}→\text{pool}→\text{bn}→\text{tanh}→\text{sign}\) for the training, as it has already been shown that placing \text{pool} before \text{bn} can lead to increased training accuracy \cite{3,30}. However, for inference it would be much faster if equivalently \text{pool} is located after \text{bn} and even the binarization of the next layer to convert a max pooling into a logic-OR operation \cite{21,26}. Additionally, for inference, \text{bn} and \text{sign} of the next layer can be aggregated as a simple threshold comparison operation (i.e., returns +1 if greater than a threshold \(\tau\) and -1 otherwise) \cite{21,26}, labeled as \(\text{thrd}\) in Figure 15. In this way, \(\text{thrd}\) can be further fused with \text{bconv} or \text{bn}\_\text{mm} to reduce the volume of data access if the residual is not saved. Finally, \(\text{tanh}\) is not required for inference as discussed. Consequently, the ultimate function order becomes \(\text{thrd}→\text{bconv}→\text{thrd}→\text{pool}→\text{bconv}\) for inference. Similar condition is also applied for the FC layers.

Traditionally, the last layer of BNN is also in full-precision \cite{1,3}. However, Tang et al. \cite{7} showed that binarizing the final layer with a learned scaling layer could significantly compact the model as FC layers comprises the most parameters. Our observation here is that such a scaling layer can be absorbed by adding a \(\text{bn}\) function for the last layer, which may provide even better performance due to
more constraint output range for the following softmax function. Note, for the final layer, since the output is real-valued and there is no future binarization, bn cannot be converted into a thrd function.

In terms of more advanced models such as ResNet, to avoid gradient diminishing or explosion, the cross-layer shortcut connections become vital. Here, the main performance concern is that these residuals are real-valued (bit-residual cannot convey gradient), which may incur substantial extra memory load & store compared with directly saving the bits after thrd. In addition, the residual may need a pooling layer before the injection. Furthermore, it is also possible that the number of channels needs to adjust. In those scenarios, we use the type-A shortcut of ResNet [58].

6.2 BTC based Implementation

Similar to [26], we have also fused all the layer functions into a single GPU kernel so the repeated kernel invocation & release overhead (as long as 20 µs per invocation [59]) can be eliminated. We implement each layer function as a GPU device function. These device functions are called from a global function where the BNN network model is defined. Due to data dependency across the layers, to ensure consistency, we rely on CUDA’s cooperative-groups for global synchronization among all SMs. There are two major challenges for the overall design here: (i) Achieving high SM utilization. Since WMMA is executed at the warp level, with 32 warps per SM for Turing GPUs and 68 SMs in RTX2080Ti for instance, the overall parallelism offered by the hardware is 2176 warps, implying 2176 BMMs sized (8,128)×(128,8) per round. Consequently, the task granularity per warp should be as small as possible in order to use all the SM warp slots and achieve workload balance; (ii) Adapting to WMMA format. As BTC can only process BMM sized (8,128)×(128,8)=(8,8), we need to ensure the row of the FC input matrix, the column of the weight, the batch of the BConv image, and the output channel can all divide 8, while the column of the FC input matrix, the row of the weight, the input channel of BConv can all divide 128. Both requirements need to be consistent across all layers. Given the BNN model can be in arbitrary configuration and we internally use our own FSB format, the address translation and calculation become more complicated. There is another format change after the final Conv layer and ahead of the first FC layer to ensure correct format transition.

7 Evaluation

We evaluate our BTC-based BNN design in this section. We first describe the experiment configurations. Then, we show the evaluation results for BMM and BConv. Finally, we discuss the performance of BNN using different models and datasets.

7.1 Experiment Configuration

We use two NVIDIA Turing GPUs with CC-7.5 for evaluation. Their information is listed in Table 2. The RTX2080 GPU is in a Linux 3.10.0 system with Intel Xeon E5-2680 CPU at 2.80 GHz, 128 GB DDR3 DRAM and gcc-4.8.5. The RTX2080Ti GPU is in a Linux 2.6.32 system with Intel Xeon E5-6230 CPU at 2.10 GHz, 384 GB DDR4 DRAM and gcc-4.8.5. All the results reported are the average of 10 times’ execution.

7.2 BMM Evaluation

For BMM evaluation, we randomly generate square matrices with increased sizes from from 128 until 16K. We use the full-precision GEMM from cuBLAS as the baseline for validation and performance comparison. We compare our three BTC-based BMM designs with the BTC approach from [8], the four BSTC BMM designs from [26], and the BTC uint-4 and BMM designs from Cutlass [51]. We conduct two types of testing: (1) General BMM where both the input matrices and the output matrix are floating-points. It includes binarization for A and B, but excludes the binarization for C. The tested schemes are listed in Table 3. (2) BNN-specific BMM where both the input matrices and the output matrix are binarized. It includes binarization for A and B, but excludes the binarization for C. This test reflects how BMM actually behaves in a BNN FC layer. The schemes are listed in Table 4.

Figure 16, 17, 18 and 19 show the results of the two BMM tests on TU104 RTX2080 GPU and TU102 RTX2080Ti GPU, respectively. For general BMM in Figure 16 and 18, we have three major observations: (I) No single approach dominates the entire matrix range — For small matrices (n<≤4K), Design-1 based on the proposed FSB-format obtains the best performance, particularly at 4K. For large matrices (n>4K), the performance of all BTC based designs drop. This is due to the fierce competition in BTC and reduced data reuse in the L0/L1 cache. Nevertheless, the size of FC layers of most BMMs fall in the medium range. (II) Comparing among Design-1, 2, and 3, while Design-2 is always better than Design-1 due to improved load efficiency and shared memory reuse, the new-format based Design-3 significantly outperforms Design-1/2 except on very large matrices. Overall, without this new FSB format, BTC may not deliver any performance advantage over existing BSTC software solutions. For BNN-specific BMM in Figure 17 and 19, the avoidance of binarizing A & B, and reduced memory store after binarizing C, dramatically amplify the supremacy of Design-3. The speedup is more than 20× over the full-precision cuBLAS at 4K on RTX2080. (III) Comparing between BMMs and uint-4 based GEMM over the same TCUs,
TABLE 2: Evaluation Platforms. "Reg" refers to the number of 4-byte registers. "Thds" refer to threads. "Dri/Rtm" refer to CUDA driver and runtime versions.

| GPU       | Arch/CC | Code | SMs | CTAs/SM | Warps/SM | Thds/CTA | Regs/SM | Shared/SM | TCUs/SM | Memory   | Mem Bandwidth | Dri/Rtm |
|-----------|---------|------|-----|---------|----------|----------|---------|-----------|---------|----------|--------------|---------|
| RTX-2080Ti| Turing-7.5 | Tu102 | 68  | 16      | 32       | 1024     | 64K     | 64K       | 8       | 11GB CDDRx6 | 616 GB/s     | 10.1/10.0 |
| RTX-2080  | Turing-7.5 | Tu104 | 46  | 16      | 32       | 1024     | 64K     | 64K       | 8       | 8GB CDDRx4  | 448 GB/s     | 10.0/10.0 |

![Fig. 16: General BMM on RTX2080](image1)
![Fig. 17: Specific BConv on RTX2080](image2)

TABLE 3: BMM full-precision output schemes.

| Schemes  | Description          | Algorithm | Input & Output Channel Size |
|----------|----------------------|-----------|-----------------------------|
| cuBLAS   | Simulating BMM via SGEMM | SGEMM     | 32bit 32bit                 |
| xnor     | BMM design in [1]    | BMM       | 32bit 32bit                 |
| bmma32   | 32bit BTC BMM in [20] | BMM       | 32bit 32bit                 |
| bmma64   | 64bit BTC BMM in [20] | BMM       | 32bit 32bit                 |
| bmma32f  | Fine-grained 32bit BTC BMM in [20] | BMM       | 32bit 32bit                 |
| bmma64f  | Fine-grained 64bit BTC BMM in [20] | BMM       | 32bit 32bit                 |
| cutlass  | BTC BMM in Cutlass library [25] | BMM       | 1bit 32bit                  |
| un       | BMM via unsigned 4-bits MM [20] | 4bit-MM   | 4bit 32bit                  |
| bmma1     | Design-1: basic BTC implementation | BMM       | 32bit 32bit                 |
| bmma128   | Design-2: 128bit load and shared memory | BMM       | 32bit 32bit                 |
| bmmafmt   | Design-3: new format | BMM       | 32bit 32bit                 |

TABLE 4: BMM bit output schemes.

| Schemes  | Description       | Algorithm | Input & Output Channel Size |
|----------|-------------------|-----------|-----------------------------|
| bmma32_y | 32bit BTC BMM in [20] with bin output | 1bit 1bit |
| bmma64_y | 64bit BTC BMM in [20] with bin output | 1bit 1bit |
| bmma32f_y | Fine-grained 32bit BTC BMM in [20] with bin output | 1bit 1bit |
| bmma64f_y | Fine-grained 64bit BTC BMM in [20] with bin output | 1bit 1bit |
| bmma1   | Design-1: basic BTC implementation with bin output | 1bit 1bit |
| bmma128 | Design-2: 128bit load with bin output | 1bit 1bit |
| bmmafmt | Design-3: new format with bin output | 1bit 1bit |

7.3 BConv Evaluation

For BConv, there are much more parameters than BMM: input_height, input_width, weight_height, weight_width, batch, input_channels, output_channels, stride, pooling, etc. We compare our two BTC-based designs (Note that we use bmma to denote Design-1 and bmmafmt to denote Design-2) with full-precision cuDNN-base (no workspace), cudnn-fast (plenty workspace), and two BTCST designs (bconv32 and bconv64) from [26]. We use cuDNN-base as the baseline and perform the two types of test: (1) General BConv where the input, filter and output tensors are all floating-points; (2) BNN-specific BConv where all of them are binarized.

Figure 20 and 21 show the results of the two types of tests with batch=16, input_size=64, weight_height=3 and stride=1 on the two GPUs. We increase both input_channels (C) and output_channels (O) from 128 to 2048. As is shown, our two BTC-based approaches exhibit considerable speedups over existing methods. Particularly, the FSB new format design achieves about 25× over the full-precision cuDNN with C=O=640 on RTX2080Ti. Comparing between the two BTC designs, we can see that (i) when C=O=128, the two designs are just equivalent, so they show similar performance; (ii) When C=O=384, Design-1 is better possibly because ldm=384 is also a good choice for memory load (see Section IV). (iii) For the other points, Design-2 shows obvious advantages.

7.4 BNN Evaluation

Finally, we evaluate the overall BNN implementation. Table 5 lists the six models we used for evaluation. Table 6 and 7 list the latency and throughput we obtained for the six models on the two NVIDIA Turing GPUs, respectively. The latency is measured under a batch size of 8 since 8 is the smallest value to leverage the bit-tensorcores so essentially the latency is for the inference of 8 images. The throughput is measured under a batch of 1024 images for MNIST and Cifar10, and 512 for ImageNet. We compare our performance with the four approaches from the latest BSTC SBNN work (from [26]). Overall, compared with the best approach SBNN-64-Fine from SBNN, our BTC using the default format design achieves on average 2.10× in latency and 1.65× in throughput on RTX2080Ti, and 2.08× in latency and 1.62× in throughput on RTX2080 across the six models. Our proposed BTC new format achieves 2.33× in latency and 1.81× in throughput on RTX2080Ti, and 2.25× in latency and 1.77× in throughput on RTX2080. The best speedup has been achieved by the FSB-format based design on RTX2080Ti for ResNet-14 on Cifar10 — 3.79× in latency and 2.84× in throughput.

Regarding this result, we have three observations: (I) Our BTC design generally achieves more 2× over existing work except for MNIST-MLP and ImageNet-Alexnet where the throughput is actually a little bit worse. The reason is...
Table 5: BTC Inference Performance on NVIDIA Turing RTX 2080 GPU.

| Network Structure               | Throughput | Latency | BNN | Our BNN | Full-Precision |
|---------------------------------|------------|---------|-----|---------|----------------|
| MNIST-MLP                       | 1.03       | 1.05    | 1.97| 4.38    | 3.85           |
| Cifar10-MLP                     | 0.22       | 0.22    | 1.36| 2.87    | 2.36           |
| Cifar10-ResNet14                | 0.08       | 0.08    | 0.72| 1.54    | 1.29           |
| VGG-16                          | 0.07       | 0.07    | 0.48| 0.77    | 0.58           |

Table 6: Comparing with FPGA works using AlexNet on ImageNet.

| Scheme | Throughput | Latency | BNN | Our BNN | Full-Precision |
|--------|------------|---------|-----|---------|----------------|
| SBNN-32| 4.953 ms   | 7.69 ms | 8.3%| 13.2%   | 9.0%           |
| SBNN-32-Fine | 4.953 ms | 7.69 ms | 8.3%| 13.2%   | 9.0%           |
| SBNN-64 | 4.953 ms   | 7.69 ms | 8.3%| 13.2%   | 9.0%           |
| BTC    | 4.953 ms   | 7.69 ms | 8.3%| 13.2%   | 9.0%           |

Table 7: BTC Inference Performance on NVIDIA Turing RTX2080 GPU.

| Network Structure               | Throughput | Latency | BNN | Our BNN | Full-Precision |
|---------------------------------|------------|---------|-----|---------|----------------|
| MNIST-MLP                       | 1.03       | 1.05    | 1.97| 4.38    | 3.85           |
| Cifar10-MLP                     | 0.22       | 0.22    | 1.36| 2.87    | 2.36           |
| Cifar10-ResNet14                | 0.08       | 0.08    | 0.72| 1.54    | 1.29           |
| VGG-16                          | 0.07       | 0.07    | 0.48| 0.77    | 0.58           |

Table 8: Comparing with FPGA works using AlexNet on ImageNet.

| Scheme | Throughput | Latency | BNN | Our BNN | Full-Precision |
|--------|------------|---------|-----|---------|----------------|
| SBNN-32| 4.953 ms   | 7.69 ms | 8.3%| 13.2%   | 9.0%           |
| SBNN-32-Fine | 4.953 ms | 7.69 ms | 8.3%| 13.2%   | 9.0%           |
| SBNN-64 | 4.953 ms   | 7.69 ms | 8.3%| 13.2%   | 9.0%           |
| BTC    | 4.953 ms   | 7.69 ms | 8.3%| 13.2%   | 9.0%           |

Table 9: Comparing with GPU and FPGA using VGG-16 on ImageNet.

| Scheme | Throughput | Latency | BNN | Our BNN | Full-Precision |
|--------|------------|---------|-----|---------|----------------|
| SBNN-32| 4.953 ms   | 7.69 ms | 8.3%| 13.2%   | 9.0%           |
| SBNN-32-Fine | 4.953 ms | 7.69 ms | 8.3%| 13.2%   | 9.0%           |
| SBNN-64 | 4.953 ms   | 7.69 ms | 8.3%| 13.2%   | 9.0%           |
| BTC    | 4.953 ms   | 7.69 ms | 8.3%| 13.2%   | 9.0%           |

Table 10: Layer-wise Synchronization Overhead.

| Network Structure               | Throughput | Latency | BNN | Our BNN | Full-Precision |
|---------------------------------|------------|---------|-----|---------|----------------|
| MNIST-MLP                       | 1.03       | 1.05    | 1.97| 4.38    | 3.85           |
| Cifar10-MLP                     | 0.22       | 0.22    | 1.36| 2.87    | 2.36           |
| Cifar10-ResNet14                | 0.08       | 0.08    | 0.72| 1.54    | 1.29           |
| VGG-16                          | 0.07       | 0.07    | 0.48| 0.77    | 0.58           |

that for MLP, a batch of 1024 is still insufficient for fully leveraging the bit-tensorcores, as will be discussed later. For Alexnet, the delay of the first layer remains too large (77.4%) while the other convolution layers are relatively smaller than alternative networks, which cannot fully utilize the BTCs. (II) Although showing better performance, the speedup led by the new FSB format is not as good in BMM and BConv, the major reason is that both the batch size and the channels are relatively small (batch≤1K, channels≤512) which is not the region that the FSB format can demonstrate its best speedups (Section VII).

Table 8 and 9 compare the single image raw latency and throughput of our BTC-based new format design with existing BNN approaches for CPU, GPU, Xeon-Phi and FPGA using Alexnet and VGG-16 on ImageNet. As can be seen, our design achieves the best single-image raw latency and throughput on Alexnet, and more than 5x throughput enhancement on VGG-16 over the existing works as listed.

7.5 Sensitivity Study

To further investigate the performance delivery, we perform several sensitivity studies in this subsection.

Latency Breakdown: Figure 24 illustrates the percentage breakdown of the latency (measured by clock(i) on GPU) for the inference of 8 images over the six models on the RTX-2080 GPU. Clearly, the first layer contributes the most delay for the three ImageNet models due significantly larger image size than the other two datasets. For Alexnet, the percentage can be as high as 77.4%. It is also over 35% for VGG-16 and ResNet-18. This is different from existing belief that the first layer is often not a big issue due to the least parameters and communication [2], [26]. The latency for other layers are roughly balanced.

Synchronization Overhead: As we enforce global synchronization through cooperative-groups per layer to ensure data consistency, such global synchronizations can introduce extra overhead and idle waiting of SMs. Table 10 shows the percentage of this synchronization overhead, which is measured by removing all the synchronization primitives. As can be seen, this overhead is the most for the medium network models, e.g., the two on Cifar10, which are 14.1% and 13.2%, respectively.

Shortcut Overhead: We then focus on the two ResNet models and measure the overhead incurred by handling the cross-layer residual. Figure 25 show the latency and throughput of the two ResNet models on RTX-2080 regarding four scenarios: (a) with residual; (b) save the residual without fetching them; (c) fetch the residual without saving them; and (d) without the residual at all. For ResNet-14 on Cifar10, if eliminating the residual-related operations, we can gain 9.7% speedup in latency and 14% in throughput. For ResNet-18 on ImageNet, we can gain 9.0% in latency and 8.3% in throughput.

Utilization: Finally we investigate the impact of batch size over the throughput. If the batch size is too small, the hardware such as the bit-tensorcores might be under-utilized. Figure 25 shows the inference throughput of the
six models with different batch sizes (normalized to the throughput with a batch of 1024 for MNIST and Cifar10, and 512 for ImageNet) on RTX2080. As can be seen, for ImageNet, a batch of 128 is sufficient to achieve the best throughput while for Cifar10, a batch of 512 is necessary. For MNIST, even with batch size arising from 16K to 32K, the throughput is still increasing. The maximum throughput is obtained at 32K, which is $7.62 \times 10^6$ fps.

8 CONCLUSION

In this paper we investigate and characterize the new bit computation capability of the tensorcores in NVIDIA Turing GPUs. We found that the stride of memory access can significantly impact the performance of memory access. Based on this observation, we propose a new bit data format for efficient design of Bit-Matrix-Multiplication and Bit-Convolution. We built the full implementation for the inference of binarized neural networks. Evaluations using six network models (MLP, VGG-like, AlexNet, VGG-16, ResNet-14/18) on three datasets (MNIST, Cifar10 and ImageNet) over two latest Turing GPUs (RTX2080 and RTX2080Ti) show that our design can bring on average $2.33 \times$ (up to 3.79×) in latency and $1.81 \times$ (up to 2.84×) in throughput compared with state-of-the-art BNN design for GPUs, leading to super realtime performance. As a future work, we are planning to exploit the bit-tensorcore for alternative utilization such as BLAS-based graph computation.

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