Design of load-independent class-E inverter with MOSFET gate-to-drain and drain-to-source parasitic capacitances

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Abstract: This paper presents a numerical design approach of the load-independent class-E inverter with MOSFET gate-to-drain and drain-to-source parasitic capacitances. The design curves of the load-independent class-E inverter are also given. A design example is shown along with its LTspice simulation and laboratory experiment. By applying the proposed design approach, there are no changes in the output-voltage waveforms and all the switch-voltage waveforms satisfy the zero-voltage-switching (ZVS) condition even the load-resistance value varies from the desired one without applying any tuning processes. Additionally, the results obtained from the LTspice simulation and laboratory experiment show quantitative agreement with the numerical predictions, which shows the effectiveness of the proposed design approach and design curves of the load-independent class-E inverter with MOSFET gate-to-drain and drain-to-source parasitic capacitances given in this paper.

Key Words: load-independent, class-E inverter, zero-voltage-switching condition, MOSFET drain-to-source parasitic capacitance, MOSFET gate-to-drain parasitic capacitance

1. Introduction

The class-E inverter is one of switching-mode inverters and it adapts single-end circuit topology [1–32]. The advantage of the single-ended circuit topology is that it requires only one switch, which is conducive to the realization of the driving circuits, especially at high frequencies. Additionally, since its switch voltage satisfies the ZVS condition, a high power-conversion efficiency can be obtained at high frequencies. Therefore, it has been widely concerned by academics and industrialists.
The class-E inverter, however, imposes restrictions on practical applications due to its sensitive characteristic to the load variation. In general, the loads are dynamic in the practical applications. In the class-E inverter, once the load varies from the desired value, the output-voltage waveform changes and the ZVS loses, which result in a degradation of the performance and efficiency. To solve the issue, a new design conception was shown in [29, 30]. The circuit topologies of the class-E inverter with the new design conception introduced in [29] and [30] and the typical class-E inverter are identical. The input inductor based on the load-independent design conception, however, works as a finite inductor instead of a RF bulk choke, which has the input current changed to provide a required amplitude and phase shift that the output-voltage waveform and the ZVS operation can be kept even the load varies. Meanwhile, it is possible to obtain a faster transient performance and smaller circuit scale because of the adoption of the finite input inductor in the load-independent class-E inverter compared with the typical class-E inverter.

[29, 30], however, did not consider the effects of the MOSFET parasitic capacitances. The shunt capacitance, which is connected between the drain and the source of the MOSFET in parallel, is an important element of the class-E inverter to satisfy the ZVS condition. In general, the shunt capacitance is composed of both the external capacitance and the MOSFET drain-to-source parasitic capacitance. At low frequencies, the MOSFET drain-to-source parasitic capacitance can be neglected because the external capacitance is dominant in the shunt capacitance. The value of the total shunt capacitance, however, decreases as the operating frequency increases. In other words, the ratio of the MOSFET drain-to-source parasitic capacitance to the total shunt capacitance increases as the operating frequency increases [8–17]. On the other hand, the gate-to-drain parasitic capacitance is connected in series to the driving signal source, which are connected between the MOSFET drain port and source one. Therefore, the gate-to-drain parasitic capacitance can be regarded to possess the same function as one of the shunt capacitance and it’s necessary to consider its effect. In other words, it is important to consider the effects of both the MOSFET gate-to-drain and drain-to-source parasitic capacitances at high-frequency operations [8–12]. There are, however, no research works to consider the effects of the MOSFET gate-to-drain parasitic capacitance and the drain-to-source parasitic capacitance of the load-independent class-E inverter for achieving the class-E ZVS condition and constant output ac voltage.

This paper presents a numerical design approach of the load-independent class-E inverter with MOSFET gate-to-drain and drain-to-source parasitic capacitances. And its design curves are given. A design example is also shown along with its LTspice simulation and laboratory experiment. There are no changes in the output-voltage waveforms and all the switch-voltage waveforms satisfy the ZVS condition even the load-resistance value varies from the desired one. Additionally, the results obtained from the LTspice simulation and laboratory experiment show quantitative agreement with the numerical predictions, which has shown the effectiveness of the design approach and design curves of the load-independent class-E inverter with MOSFET gate-to-drain and drain-to-source parasitic capacitances.

2. Load-independent class-E inverter

Figure 1(a) shows the circuit topology of the load-independent class-E inverter. The load-independent class-E inverter has a simple circuit topology just like the typical class-E inverter and is composed of a dc-supply voltage source \( V_I \), an input inductor \( L_i \), MOSFET as a switching device \( S \), a shunt

![Fig. 1. Load-independent class-E inverter. (a) Circuit topology. (b) Equivalent circuit.](image)
capacitor \( C_S \), a series resonant filter \( L - C \), and load resistor \( R \).

Figure 2 shows the example waveforms of the load-independent class-E inverter for the switch-on duty ratio \( D = 0.5 \). In this figure, \( \theta = \omega t = 2\pi f \) represents the angular time and \( f \) is the operating frequency. For the load-independent class-E inverter, the switch \( S \) is driven by the input voltage \( Dr \) as shown in Fig. 2 and turns on and off alternately. When the switch \( S \) turns off, the sum of the currents through the input inductor and the output series resonant filter flows through the shunt capacitance \( C_S \) and produces the switch voltage \( v_S \). And when the switch is at the turns-on instant, the switch voltage \( v_S \) satisfies the ZVS condition,

\[
v_S(\pi) = 0.
\]  

(1)

Because of the ZVS condition, the switching power losses are minimized. Therefore, the load-independent class-E inverter can achieve a high efficiency at high frequencies.

3. Design procedure

In this section, we consider the effects of the MOSFET gate-to-drain and drain-to-source parasitic capacitances and give the design procedure for the load-independent class-E inverter. The design approach is based on the design procedure in [31]. By applying this numerical design procedure, it is possible to obtain the accurate design values easily for achieving multiple design restrictions.

3.1 Assumptions

In this paper, the load-independent class-E inverter is designed with the following assumptions:

1) The shunt capacitance is composed of the external capacitance \( C_{ext} \) and the MOSFET drain-to-source parasitic capacitance \( C_{ds} \). Additionally, the MOSFET drain-to-source parasitic capacitance has nonlinear characteristic and is expressed as [11–17]

\[
C_{ds} = \frac{C_{j0}}{\left(1 + \frac{v_S}{V_{bi}}\right)^m},
\]  

(2)

where \( V_{bi} \) is the built-in potential, which typically ranges from 0.5 to 0.9 V, \( C_{j0} \) is the capacitance at \( v_S = 0 \), and \( m \) is the grading coefficient of the diode junction.

2) The MOSFET gate-to-drain parasitic capacitance \( C_{gd} \) is regarded as a linear one [8–12]. The assumptions 1) and 2) follow PSpice MOSFET models, which have a nonlinear drain-to-source parasitic capacitance and a linear gate-to-drain parasitic capacitance.

3) The equivalent series resistances (ESRs) of all the inductors are considered. The ESRs of all the capacitors, however, are ignored because they are much smaller than ESRs of the inductors.

4) All the passive elements except the MOSFET drain-to-source parasitic capacitance work as linear elements.
Table I. Switching pattern of the load-independent class-E inverter with MOSFET gate-to-drain and drain-to-source parasitic capacitances.

| $D_f$ | $0 < \theta \leq \pi$ | $\pi < \theta \leq 2\pi$ |
|-------|------------------------|------------------------|
|       | OFF                    | ON                     |

5) The switch $S$ has zero switching time, infinite off resistance, and on resistance $r_{on}$.

6) The switch $S$ turns off at $\theta = 0$ and the switch-on duty ratio $D = 0.5$. Therefore, its switching patterns are given as Table I.

7) The driving signal source is an ideal voltage source as shown in Fig. 1(a).

Using the above assumptions, the equivalent circuit of the load-independent class-E inverter with the MOSFET gate-to-drain and drain-to-source can be obtained as shown in Fig. 1(b).

3.2 Parameters

In this paper, following parameters are defined for the inverter designs.

a) $A = f_o/f = 1/(2\pi f \sqrt{LC})$: The ratio of the resonant frequency to the operating frequency.

b) $B = C/(C_{gd} + C_{ext})$: The ratio of the resonant capacitance to the sum of the MOSFET gate-to-drain capacitance and external capacitance.

c) $H = L/L_i$: The ratio of the resonant inductance to the input inductance.

d) $Q = \omega L/R$: The loaded quality factor in the series resonant filter.

e) $B_{non} = C_j/(C_{gd} + C_{ext})$: The ratio of the MOSFET drain-to-source capacitance at $v_S = 0$ to the sum of the MOSFET gate-to-drain capacitance and external capacitance.

3.3 Circuit equations

The operations in the range of $0 < \theta \leq 2\pi$ are considered for the design of the load-independent class-E inverter with MOSFET gate-to-drain and drain-to-source parasitic capacitances and its circuit equations are given as follows,

\[
\begin{align*}
\frac{di_i}{d\theta} &= \frac{H}{QR} (V_I - v_S - r_{Li}i_i) \\
\frac{di_o}{d\theta} &= \frac{1}{QR} [v_S - v_C - (R + r_L)i_o] \\
\frac{dv_S}{d\theta} &= A^2 BQR \left( i_i - \frac{v_S}{r_S} - i_o \right) / (1 + v_S/V_{bi})^m \\
\frac{dv_C}{d\theta} &= A^2 QR i_o
\end{align*}
\]

where $r_{Li}$ and $r_L$ are the ESRs of the input inductor $L_i$ and resonant inductor $L$, respectively. And $r_S$ is the equivalent resistance of the switch $S$. In this paper, $r_S$ is expressed as

\[
r_S = \begin{cases} r_{on} & \text{if } r_S \text{ is in the on state} \\ \infty & \text{if } r_S \text{ is in the off state} \end{cases}
\]

Additionally, when we define $x(\theta) = [x_1, x_2, x_3, x_4]^T = [i_i, i_o, v_S, v_C]^T \in \mathbb{R}^4$. (3) can be rewritten as

\[
\frac{dx}{d\theta} = f(\theta, x, \lambda)
\]

where $\lambda = [A, B, H, Q, B_{non}, r_S, R, V_{bi}, m]^T \in \mathbb{R}^9$. 

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Table II. The parameters of MOSFETs.

|   | \( r_{on} \)  | \( C_{j0} \)  | \( C_{gd} \)  | \( V_{bi} \)  | \( m \) |
|---|--------|--------|--------|--------|--------|
| IRF510 | 0.54 \( \Omega \)  | 367 pF  | 40.1 pF | 0.8 V  | 0.5    |
| IRF520 | 0.27 \( \Omega \)  | 622 pF  | 137 pF | 0.8 V  | 0.5    |
| IRF530 | 0.16 \( \Omega \)  | 1151 pF | 178 pF | 0.8 V  | 0.5    |

3.4 Design conditions

The load-independent class-E inverter with MOSFET gate-to-drain and drain-to-source parasitic capacitances should operate in the steady state, achieving the switching condition. The steady-state conditions of the driver are

\[ x(2\pi) - x(0) = 0 \in \mathbb{R}^4 \]  

which are the boundary conditions at \( \theta = 0 \) and \( \theta = 2\pi \). The ZVS condition shown in (1) is mandatory to achieve. Additionally, the phase shift of the output current is zero. This is also one of the restrict conditions, which guarantees a constant output voltage even the load changes [29, 30].

\[ \varphi = 0, \]  

where \( \varphi \) is the initial phase shift of the output current.

From the above, it can be seen that the design of the load-independent class-E inverter with MOSFET gate-to-drain and drain-to-source parasitic capacitances is regarded to solve the algebraic equations shown in (1), (6), and (7). In these equations, there are 6 algebraic equations and 4 unknown parameters. Therefore, 2 parameters can be set as the design parameters from \( \lambda \). In this paper, we selected the parameters \( A \) and \( B \) as the unknown parameters and gave the other parameters as design specifications. In order to obtain the values of the unknown parameters, the Newton’s method is applied to solve the algebraic equations. It is possible to derive the algebraic-equation solutions numerically. The algorithm of the Newton’s method was presented in [31] in detail. Additionally, for obtaining the initial values of the currents and voltages of the circuit equations in (3), the Runge-Kutta method is used.

4. Design curves

In this section, design curves of the load-independent class-E inverter with the MOSFET gate-to-drain and drain-to-source parasitic capacitances are shown by using the design procedure presented in the previous section. Firstly, the design specifications of the load-independent class-E inverter with MOSFET gate-to-drain and drain-to-source parasitic capacitances were given as follows: \( D = 0.5 \), \( f = 4 \) MHz, \( R = 20.0 \) \( \Omega \), and \( Q = 10.0 \). Additionally, IRF510, IRF520, and IRF530 MOSFETs by International Rectifier were selected as examples for considering the effects of their parasitic capacitances. And from the PSpice model of IRF510, IRF520, and IRF530 MOSFETs, their parameters were obtained as shown in Table II. IRF510, IRF520, and IRF530 MOSFETs’ PSpice models are given in the Appendix, respectively. The parameters \( V_{bi}, m, \) and \( C_{j0} \) are identical to \( P_{b}, M_{j}, \) and \( C_{bd} \) in the MOSFET model, respectively. In addition, the MOSFET gate-to-drain parasitic capacitance is obtained as \( C_{gd} = W \times C_{gdo} \) [12]. Note that all the ESRs of the inductors are zero for calculating the design curves.

Figure 3 shows the design parameters as functions of \( H \) for fixed values of \( V_{I}/V_{bi} \) and three types of MOSFETs, respectively. It is seen from Fig. 3(a) that \( A \) increases as \( H \) increases and \( A \) increasingly approaches to 1 with the increase of \( H \). Namely, the resonant frequency of the series resonant filter \( L - C \) is closer to the operating frequency with the increase of \( H \). Additionally, \( A \) increases as \( V_{I}/V_{bi} \) increases. It is seen from Figs. 3(b) and (c) that \( B \) and \( B_{non} \) increase with \( H \) decreases regardless of \( V_{I}/V_{bi} \) and MOSFET type. In particular, the larger \( C_{j0} \) and \( C_{gd} \) are, namely, the larger the MOSFET parasitic capacitances are, the more significantly \( B \) and \( B_{non} \) vary for small \( H \). It can be also seen from Figs. 3(b) and (c) that the smaller \( V_{I}/V_{bi} \) is, the larger \( B \) and \( B_{non} \) are for the same MOSFET when \( H \) is small.
5. Output power and power output capability

Figure 4 shows the normalized peak values of both the switch voltages and the switch currents, output powers, and power output capabilities. $V_{SM}$ and $I_{SM}$ are the peak values of the voltages and currents at the MOSFETs, which can be expressed as

$$V_{SM} = \max \{ v_S \} \quad \text{and} \quad I_{SM} = \max \{ i_S \}. \quad (8)$$

The normalized output powers can be obtained as

$$\frac{P_o R}{V_I^2} = \left( \frac{V_o}{V_I} \right)^2, \quad (9)$$

where $V_o/V_I$ is a root-mean-square value of the normalized output voltage $v_o/V_I$ and can be given by

$$\frac{V_o}{V_I} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} \left( \frac{v_o(\theta)}{V_I} \right)^2 d\theta}. \quad (10)$$

And $c_p$ is the power output capability and can be expressed as

$$c_p = \frac{P_o}{V_{SM} I_{SM}}. \quad (11)$$

It is seen from Figs. 4(a) and (b) that the peak values of the switch voltages decrease as $H$ increases, on the contrary, the peak values of the switch currents increase as $H$ increases regardless of $V_I/V_{bi}$ and MOSFET type. It is also seen from Fig. 4(c) that the normalized output powers decrease as $H$ increases regardless of $V_I/V_{bi}$ and MOSFET type. Additionally, the larger the MOSFET parasitic capacitances are, the larger the normalized output powers are. Figure 4(d) shows the power output capabilities as functions of $H$ for fixed $V_I/V_{bi}$ and three types of MOSFETs. It can be seen from
Fig. 4. Characteristics as functions of $H$ for fixed values of $V_I/V_{bi}$ in the load-independent class-E inverter. (a) Normalized maximum switch voltages $V_{SM}/V_I$ as functions of $H$. (b) Normalized maximum switch currents $I_{SM}/I_I$ as functions of $H$. (c) Normalized output powers $P_{oR}/V_I^2$ as functions of $H$. (d) $c_p$ as functions of $H$.

Fig. 4(d) that the maximum power output capabilities occur near $H = 10$ regardless of $V_I/V_{bi}$ and MOSFET type.

In this paper, the effects of only the Si MOSFET’s parasitic capacitances were discussed. If the SiC/GaN MOSFET’s PSpice model can be provided, it is also possible to use the design procedure. When the SiC/GaN MOSFET is applied as a switching device in this design procedure and its PSpice model is available, there are two adjustments. Firstly, a new equivalent circuit should be rebuilt with the SiC/GaN MOSFET’s PSpice model. Secondly, according to the rebuilding equivalent circuit, the circuit equations of the currents and voltages are rewritten. By using the design conditions shown in the paper and the rewritten circuit equations, the design procedure with the SiC/GaN MOSFET can be reconstructed. The SiC/GaN MOSFET has attracted much attention from both academic and industry communities because of its many favorable capabilities such as low on-resistance, high breakdown voltage, and high-speed operation and so on. Therefore, it should address the effects of the SiC/GaN MOSFET’s parasitic capacitances in the future.

6. Design example

In order to demonstrate the validity of the proposed design procedure and design curves, the load-independent class-E inverter with MOSFET gate-to-drain and drain-to-source parasitic capacitances was designed in this section. First, the design specifications were given as ones mentioned in Section 4. We chose dc-supply voltage $V_I = 10$ V and IRF530 MOSFET as the switching device. Therefore, $V_I/V_{bi}$ is equal to 12.5. Additionally, $H = 10.8$ was selected in which the power output capability is maximum for $V_I/V_{bi} = 12.5$ and IRF530 MOSFET from Fig. 4(d). Because of $Q = \omega L/R$ and $H = L/L_i$, $L = 7.96 \, \mu H$ and $L_i = 0.734 \, \mu H$ were obtained. Therefore, we made inductors prior to the numerical calculations for solving the design equations. By using Impedance Analyzer KEYSIGHT E4990A, $r_{Li} = 90.6 \, m\Omega$ and $r_L = 0.608 \, \Omega$ were measured, which were also used in the design.
Fig. 5. Experimental setup of the implemented circuit.

Table III. Design values of the load-independent class-E inverter with the MOSFET gate-to-drain and drain-to-source parasitic capacitances for \( Q = 10 \).

| Numerical | Measured | Difference |
|-----------|----------|------------|
| \( L_i \) | 0.734 \( \mu \)H | 0.737 \( \mu \)H @ 4MHz | 0.39 % |
| \( r_{Li} \) | - | 90.6 m\( \Omega \) @ 4MHz | - |
| \( L \) | 7.96 \( \mu \)H | 7.92 \( \mu \)H @ 4MHz | -0.48 % |
| \( r_L \) | - | 0.608 \( \Omega \) @ 4MHz | - |
| \( C_{ext} \) | 799 pF | 799 pF @ 4MHz | 0.00 % |
| \( C \) | 205 pF | 203 pF @ 4MHz | -0.98 % |
| \( R \) | 20.0 \( \Omega \) | 20.0 \( \Omega \) | 0.00 % |
| \( V_I \) | 10.0 V | 10.0 V | 0.00 % |
| \( I_I \) | 0.631 A | 0.631 A | 0.00 % |
| \( V_o \) | 10.8 V | 10.7 V | -0.93 % |
| \( V_{SM} \) | 37.4 V | 40.5 V | 8.29 % |
| \( \eta \) | 93.2 % | 90.4 % | - |

Table IV. Comparisons for the measurements of \( R = 20 \, \Omega \), \( 30 \, \Omega \), and \( 40 \, \Omega \).

| \( R = 20 \, \Omega \) | \( R = 30 \, \Omega \) | \( R = 40 \, \Omega \) |
|-----------------|-----------------|-----------------|
| \( V_{SM} \) | 40.5 V | 39.6 V | 39.2 V |
| \( V_o \) | 10.7 V | 10.9 V | 11.1 V |
| \( \eta \) | 90.4 % | 91.1 % | 91.5 % |

calculation. By using the design specifications mentioned in the above and the design procedure shown in Section 3, the design values were obtained as given in Table III.

Figure 5 shows the experimental setup of the implemented circuit. The Micrometals iron-powder toroidal cores T-80 and T-106 were used as cores of the input inductor and series resonant inductor, respectively. Additionally, the polyurethane copper wire whose diameter is 1.0 mm was used as the winding wire. The turn numbers of the two inductors were 8 and 22, respectively.

Figure 6 shows the waveforms obtained from the numerical calculations, LTspice simulation, and laboratory experiment, respectively. The experimental waveforms were obtained from the oscilloscope Tektronix MDO4034-3. In Fig. 6, the results in which the load resistance \( R \) was varied from 20.0 \( \Omega \) to 30.0 \( \Omega \) and 40.0 \( \Omega \) but the other parameter values are the same, were also shown. It is seen from Fig. 6 that there were no changes in the output-voltage waveforms and all the switch-voltage waveforms satisfied the ZVS condition even the load-resistance value was changed from the desired one.

Table III also gives the measured results for the laboratory experiment. In this table, the dc-supply voltage \( V_I \) and the average value of the input current \( I_I \) were obtained from the regulated dc power supply of KIKUSUI PMX18-2A. Additionally, the root mean square value of the output voltage \( V_o \) was obtained from the oscilloscope Tektronix MDO4034-3. It is seen from Table III that the measured results agreed with the numerical calculations well.

Table IV gives the measured peak values of the switch voltages \( V_{SM} \), root mean square values of
Fig. 6. Waveforms of the load-independent class-E inverter with the MOSFET gate-to-drain and drain-to-source parasitic capacitances. (a) For numerical calculation. (b) For LTspice simulation. (c) For laboratory experiment.

the output voltages $V_o$, and power-conversion efficiencies $\eta$ of $R = 20 \, \Omega$, $30 \, \Omega$, and $40 \, \Omega$. It can be seen from Table IV that there are no significant changes in the peak values of the switch voltages, root mean square values of the output voltages, and power-conversion efficiencies for the effects of variations in the load resistance. The measured power-conversion efficiency increased a little with the load resistance increased. This is because the ESRs of the inductors are intrinsic values and their effects weaken with the load resistance increase, though the ESRs of the inductors are one of loss sources. It can be stated from these results that the design approach and design curves of the load-independent class-E inverter considering the effects of the MOSFET gate-to-drain and drain-to-source parasitic capacitances presented in this paper are effective.

7. Conclusion
This paper has presented a numerical design approach of the load-independent class-E inverter with MOSFET gate-to-drain and drain-to-source parasitic capacitances. The design curves were derived. A design example was also shown along with its LTspice simulation and laboratory experiment. There were no changes in the output-voltage waveforms and all the switch-voltage waveforms satisfied the ZVS condition even the load-resistance value was changed from the desired one. Additionally, the results obtained from the LTspice simulation and laboratory experiment show quantitative agreement with the numerical predictions, which showed the accuracy of the proposed design approach and design curves given in this paper and demonstrated the importance of considering the load-independent class-E inverter with MOSFET gate-to-drain and drain-to-source parasitic capacitances.

Acknowledgments
The IRF510, IRF520, and IRF530 MOSFET models used in this paper is obtained from the default package of PSpice, which are licensed by Cadence. The IRF510, IRF520, and IRF530 MOSFET parameters are shown as follows,

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.model IRF510 NMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0.2 Vmax=0 Xj=0
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