Comparison of JFET/MOS/HEMT Based Low Noise Charge Sensitive Preamplifiers for HPGe Detectors in Cryogenic Temperature

Li He¹, Jiajun Hao¹,², Zhi Deng¹,², Feng Liu¹,², Yinong Liu¹,², Yulan Li¹,², and Qian Yue¹,², Jian Cai⁴

¹Department of Engineering Physics, Tsinghua University, Beijing, 100084, China
²Key Laboratory of Particle & Radiation Imaging, Ministry of Education, Beijing, 100084, China
³Joint Research Center, Nuctech Company Limited, Beijing, 100084, China
⁴Institute of microelectronics, Tsinghua University, Beijing, 100084, China
dengz@mail.tsinghua.edu.cn

Abstract. The paper presents development of three different types of low noise charge sensitive preamplifiers (CSA) for HPGe detectors for basic physics experiments such as CDEX (China dark matter search experiment) and spectroscopy applications, based on JFET, MOS and HEMT transistors respectively. For the JFET and HEMT based CSAs, only the input transistor of the corresponding type was used and their secondary amplifiers were designed with commercial opamps and worked at room temperature. For the MOS based CSA, a monolithic ASIC of CMOS CSA was developed using a 350 nm CMOS process. The noise performances of these CSAs were optimized for a point-contact HPGe detector with ~2 pF input capacitance and were tested at liquid nitrogen temperature. JFET suffered from the ‘freeze-out’ effect and the noise performance of the JFET CSA degraded from 64 electrons to 134 electrons when the temperature went from 120 K to 77 K. For comparison, the noises of the MOS and HEMT based CSAs kept getting better down to 77 K. The serial noises of the MOS and HEMT CSAs were similar and the HEMT CSA showed significant parallel noise contribution. The CMOS CSA has also been tested with a 0.5 kg point-contact HPGe detector. The energy spectrum was measured and the electronics noise was monitored to be 186 eV, corresponding to 26 electrons ENC (equivalent noise charge) in rms.

1. Introduction
The HPGe (High purity germanium) is an ionizing radiation detector or energy spectrometry of gamma ray. For its extremely high energy resolution, it is the first choice of gamma ray spectrometer which is widely used in environmental monitoring, homeland security and so on [1]. Besides, the HPGe also has an ultra-low radiation background which makes it be very suitable for dark matter detection and neutrinoless double beta decay experiment. [2] - [5]
For controlling the detector’s leakage current, the HPGe should work under cryogenic condition and the liquid nitrogen is used to cool down the detectors in most applications. And the same time, the front-end readout electronics need to be mounted very close to the detector for reducing the stray capacitance of connecting which will degrade the noise performance of charge sensitive preamplifiers. So the preamplifier is required to work at 77K properly. [6]

Depending on the shape of the detector’s readout electrode, the HPGe detectors are sort of coaxial type [7], planar type, and point contact type [8] etc. Different types of electrodes are with different size of detector capacitance, so the noise optimization of preamplifiers for different type detectors should be well considered.

Three types of preamplifier implemented for HPGe detector readout will be compared: JFET [9] [10], MOS process ASIC (Application Specific Integrated Circuit) [11] [12] and HEMT [13]. The characteristics and noise performance of each type of front-end electronics will be discussed and compared in the following sections.

2. JFET preamplifier

Conventional charge sensitive amplifier for the HPGe detector front-end readout is using JFET as the input transistor. Due to the low flicker noise, the noise capacitance slope of JFET preamplifier is relative small which make the JFET preamplifier be convenient for large size readout electrode detector such as coaxial type, planar type HPGe detector.

However, the JFET is not inclined to be mounted very close to the detectors since the “freeze out” effect. Such effect will degrade the JFET’s noise performance by decreasing the transconductance. So the optimum working temperature of JFET is about 120K to 150K. [14]

The reason that the JFET suffers the “freeze out effect” is the dopants of JFET require some energy to ionize and produce carriers in the semiconductor. This energy is usually thermal and if the temperature is too low, the dopants will not be sufficiently ionized.

2.1. Circuit implementation

For evaluating the noise performance of JFET, a pulse reset structure charge sensitive preamplifier has been designed. This preamplifier is using JFET 2n4416 which is used for HPGe detector front end readout conventionally as the input transistor. By using this structure, the parallel white noise introduced by feedback resistor can be eliminated. By controlling the source voltage of JFET, the gate and source of JFET can break over and the charge accumulated on the feedback capacitor can be released. With this pulse reset scheme, no additional stray capacitance will be introduced at the input of preamplifier. The secondary amplifier has been employed for obtaining higher open loop gain to guarantee the linearity and stability of this circuit. The schematic of this preamplifier is shown in Figure 1.

![Figure 1. The schematic of JFET pulse reset charge sensitive preamplifier](image-url)
2.2. Noise performance
This circuit has been tested at 77K. The output signal of preamplifier is shaped and amplified by a commercial spectroscopy amplifier (CANBERRA 2026).

By measuring the JFET noise with different shaping time, the noise components of JFET can be deduced. The measured serial white noise and the flicker noise of JFET have been represented in Figure 2. The theoretical white noise which is calculated through the transconductance value given by the datasheet [19] has been shown in this figure as well. The larger measured white noise is because of the decreased transconductance caused by “freeze out” effect. The measured flicker noise is much higher than anticipated. The secondary amplifier may be the primary flicker noise source. Both the serial white noise and the flicker noise are worse than theoretical which will also lead to much higher noise capacitance slope. The noise capacitance slope has been fitted with different values of the input capacitance, as shown in Figure 3. The minimum noise capacitance slope is about 7.2e/pF which was obtained by using 12μs shaping time.

![Figure 2. The JFET noise components tested at 77K](image1)

![Figure 3. The JFET noise capacitance slope tested at 77K](image2)

3. MOS process ASIC
As enhancement type MOSFETs, the carriers needed for conduction in the channel can be ionized by an electric field from gate. So, the MOSFETs can operate to the lowest temperatures.

The schematic with pulse resets structure of the MOS process preamplifier ASIC is shown in Figure 4. The core amplifier was implemented using classical cascode structure with a PMOS as the input transistor. Its size was optimized for 2pF input capacitance which was verified by circuit simulation. The bias current can be adjusted by an external resistor to guarantee the chip working at cryogenic temperature. The layout of the ASIC is shown in Figure 5.
3.1. Noise optimization

The noise theory of the CMOS charge sensitive preamplifier (CSP) has been well studied and can be described as the equation below.

$$ ENC^2 = (C_g + C_S)^2 \cdot \left( \frac{4\gamma KT}{g_m t_p} + \frac{\pi K_f}{C_{ox} W L} \right) $$

Where ENC is the Equivalent Noise Charge, \( C_S = C_d + C_p + C_f \) is the sum of the detector capacitance \( C_d \), the parasitic capacitance of the interconnection \( C_p \) and the feedback capacitance \( C_f \), \( C_g \approx C_{ox} W L \) is the gate capacitance of the input transistor, \( \gamma \) is the thermal noise coefficient ranging from 1/2 to 2/3, \( K \) is the Boltzmann constant \((= 1.38 \times 10^{-23} \text{ J/K})\), \( T \) is the absolute temperature in Kelvin, \( g_m \) is the transconductance of the input transistor, \( t_p \) is the peaking time of the shaper, \( K_f, C_{ox}, W \) and \( L \) are the flicker noise coefficient, the unit gate capacitance, the width and the length of the input transistor respectively.

Comparing with JFET, the handicap of MOS process ASIC is the higher flicker noise which will determine the minimum ENC for CMOS CSP. For reducing the flicker noise as much as possible, the input transistor has been optimized. First, the PMOS was adopted as input transistor which has 10 times lower flicker noise than NMOS. From the equation we can learn that the optimum ENC for flicker noise can be achieved when the detector capacitance is equal to the gate capacitance of the input transistor. The optimization for thermal noise is more complicated since the transconductance of the input transistor depends on its working condition. For small size electrode HPGe detector, such as the point contact HPGe detectors, the input transistor is designed to work under velocity saturation condition for practical power consumption and the flicker noise can be optimized at the same condition. The details about the CMOS CSP noise optimization has been discussed in [15] - [17].

3.2. Noise performance test

An evaluation PCB has been developed and used for the chip performance test. The ENC noises were measured with different shaping time at 77K for noise components analysis. As shown in Figure 6, the serial white noise of ASIC fits well with the simulation results [18]. It can be neglected when using large shaping time values (12μs). The flicker noise is slightly higher than the simulation prediction. The additional flicker noise may be induced by the test PCB materials.

The noise capacitance test result is shown in Figure 7. The minimum noise slope is 4.5e/pF which is obtained at 12μs shaping time. The noise slope of ASIC is mainly determined by flicker noise. The
noise slope tested result of ASIC is even better than JFET since the relatively small flicker noise and the ultra-low serial white noise benefiting from the immunity of ‘freeze out’ effect.

![Figure 6. The ASIC noise components tested at 77K](image)

![Figure 7. The ASIC noise capacitance slope tested at 77K](image)

4. HEMT

Another option for the cryogenic front-end read-out is using HEMT as input transistor. In fact, the HEMT is based on a two-dimensional electron gas which is realized in a heterostructure with a high purity material interface and hence the carriers of HEMT don’t need thermal energy to ionize the dopants. However, for cryogenic read-out electronics, commercially available HEMTs are used in a frequency range above a few hundreds of kHz and suffer a relatively high noise current and especially a large low frequency noise. With the improvement of the material quality and an appropriately designed heterostructure and gate configuration, extremely low noise voltage and noise current can be obtained under cryogenic conditions. [13]

4.1. Noise analysis

The equation shown below is employed for HEMT’s serial white noise and flicker noise calculation.

\[
e n^2 = \frac{8KT}{3g_m} + \frac{A_F}{f}
\]

(2)

The transconductance \(g_m\) of the HEMT has been given directly in the datasheet. [13] As for the flicker noise coefficient \(A_F\), it can be extracted from the noise voltage spectrum.

The noise of HEMT can be calculated with equation (3) after shaping amplifier. The ENC is obtained by considering the gain of the shaping amplifier and the preamplifier. [11]

\[
ENC = \frac{2e^3}{9} \sqrt{\frac{KTC^2_e}{24g_m}} \frac{1}{\tau} + \frac{A_FC^2_e}{6} \times 6.25 \times 10^{18}
\]

(3)

This ENC noise calculation equation can be shown as Figure 8. The red curve is the serial white noise at 77K which can be as low as 2e with 12µs shaping time. The black line is the calculated flicker noise. The theoretical flicker noise of HEMT is about 6e.
4.2. **Noise performance test**

The evaluated board for HEMT noise performance test under cryogenic condition is shown in Figure 9. This board is like the JFET test board that means a secondary amplifier has been employed as well. The layout of the HEMT is shown in Figure 10.

![Figure 9](image.jpg)  
**Figure 9.** The evaluation board for HEMT

![Figure 10](image.jpg)  
**Figure 10.** The layout of HEMT

The measured HEMT noise components have been shown in Figure 11. The measured white noise component value at 77K is in good agreement with the theoretical results that suggest that the HEMT doesn’t suffer the ‘Freeze out’ effect. The test flicker noise is about 25e and is much higher than calculated results. The test result of HEMT flicker noise is quite similar with the JFET’s which imply that the main contribution of the flicker noise is from the secondary amplifier. More test work will be carried out in the future.

![Figure 8](image.jpg)  
**Figure 8.** The theoretical HEMT noise components at 77K
5. Comparison of the three preamplifiers

All of these three low noise readout electronics has been tested at 77K. The noise components of each preamplifier have been analysed and the noise capacitance of JFET preamplifier and MOS process ASIC have been measured. In this section, the comparison results of these 3 low noise preamplifiers will be discussed.

5.1. Noise components comparison

All these three low noise preamplifiers have been tested at 77K and the serial white noise and the flicker noise components have been analysed. For comparison, the measured white noise components of each preamplifier have been shown in Figure 12(a) at the same time and these three preamplifier’s test flicker noise have been shown in Figure 12(b).

As shown in Figure 12(a), the HEMT is with the lowest serial white noise for the HEMT have the largest transconductance and is immune to the ‘freeze out’ effect. As for the flicker noise, all of these three preamplifiers’ test results are larger than anticipation: the additional flicker noise of ASIC may be from the test board PCB material which can be reduced by using low dielectric dissipation factor material for PCB fabrication. Meanwhile, the flicker noise test results of JFET and HEMT are quite
close and much larger than theoretical value. The most possible reason for such condition is the secondary amplifier’s flicker noise contribution.

5.2. Noise capacitance slope comparison
The test noise slope of JET and the ASIS are shown in Figure 13. The noise slope of JFET with 12us shaping time is about 7.2e/pF while the noise slope of ASIC with 12us shaping time is about 4.5e/pF. The noise slope JFET is much higher than anticipation which may be results of the transconductance degradation caused by freeze out effect and the higher flicker noise introduced by secondary amplifier.

![Figure 13. Noise capacitance slope comparison of JFET and ASIC](image)

6. Conclusion
As the most sensitive ionizing radiation detector, the HPGe put forward an extremely high requirement for frond end readout electronics’ noise performance. 3 types of low noise CSP have been implemented for HPGe front end readout and the noise performance of each preamplifier have been analyzed and test.

Because of the ‘freeze out’ effect, the JFET exhibited the worse serial white noise of all at 77K. For the relative large designed transconductance and being immune to the ‘freeze out’, the white noise test results show that implementation of MOS process ASIC and HEMT for HPGe detector readout is quite promising. The flicker noise test results of these types CSP are higher than expected more or less. And the additional flicker noise may be introduced from the test board PCB material and the secondary amplifier.

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