ALDO2, a multi-function rad-hard linear regulator for SiPM-based HEP detectors

P. Carniti\textsuperscript{a,b}, C. Gotti\textsuperscript{a,b}, G. Pessina\textsuperscript{a,b}

\textsuperscript{a}University of Milano-Bicocca, Piazza della Scienza 3, 20126, Milan (Italy)
\textsuperscript{b}INFN of Milano-Bicocca, Piazza della Scienza 3, 20126, Milan (Italy)

Abstract
ALDO2 is a multi-function, adjustable, low dropout linear regulator designed in onsemi I3T80 0.35 $\mu$m HV CMOS technology for use in HEP detectors that adopt silicon photomultipliers (SiPMs). The chip features four independent regulators, two low voltage channels (max 3.3 V) used to filter and stabilize the power supply of front-end chips, and two HV channels (max 70 V), specifically designed to provide the bias voltage to arrays of SiPMs. Each regulator can be independently shut down and is protected for overcurrent and over-temperature. The HV regulators also implement a circuit to monitor the bias current of the SiPM arrays, allowing to perform I-V curves and thus to fine-tune the working point of the SiPM arrays during the detector lifetime. The chip adopts radiation hardening techniques and has been fully qualified up to a TID of 20 Mrad, a 1-MeV-equivalent neutron fluence of $10^{15}$ cm$^{-2}$, and with heavy ions up to 40 MeV cm$^{-2}$ mg$^{-1}$ LET and $10^{16}$ cm$^{-2}$ cumulative fluence. The chip will be installed in two CMS detectors in the HL-LHC phase, the Barrel Timing Detector (BTL) and the High Granularity Calorimeter (HGCAL).

Keywords: Voltage regulator, LDO, CMOS, Rad-hard, SiPM, MPPC, Bias voltage, HL-LHC, Barrel Timing Layer, High-Granularity Calorimeter

1. Introduction
Starting after Long Shutdown 3, the Large Hadron Collider (LHC) at CERN will enter the so-called high-luminosity phase (HL-LHC). The maximum instantaneous luminosity will be increased by a factor of 10, hence all the experiments operating at LHC will require a substantial re-design of their detectors to cope with the increased number of collisions, which translates into increased pile-up and radiation levels.

Two new detectors of the CMS experiment will adopt arrays of silicon photomultipliers (SiPMs, also known as multi-pixel photon counters, MPPCs) to detect the light produced in scintillators. These two detectors are the Barrel Timing Layer (BTL)\textsuperscript{[1]}, a minimum-ionizing particle timing detector in the barrel part of the experiment, and the High Granularity Calorimeter (HGCAL)\textsuperscript{[2]}, in the outer region of the endcap.

The use of SiPMs in highly radioactive environments is particularly challenging since radiation damage induces a sharp increase in the dark count rate (DCR) up to several GHz per device at the detector end-of-life, and a shift in the breakdown voltage that adds to the intrinsic spread between different samples. Devices are thus usually cooled at low temperatures to minimize the effect of DCR\textsuperscript{[3]}. In these difficult working conditions, it is essential for the overall performance of the detector – especially when aiming at tens of ps of timing resolution like in the BTL – that the bias voltage is adequately filtered and precisely regulated to the required value throughout the detector lifetime. The high currents involved when several SiPMs are biased in parallel and the dense packing of these detectors are two other important aspects that encourage the adoption of a point-of-load regulation of the bias supply, close to where the power is dissipated. Moreover, it is required to perform I-V curves and periodically characterize the SiPM response during the detector lifetime to set each SiPM array’s working point as the radiation damage accumulates.

Another need that is common to these detectors is to provide additional low-voltage supplies to the front-end chips with increased filtering, lower noise, and better stability than those provided by DCDC regulators.

The ALDO2 chip was specifically designed to address all these issues for the BTL and HGCAL detectors, and it is the first of this kind in the HEP electronics community.

The device must withstand high radiation levels, especially in BTL, where the radiation will reach a TID of 3.2 Mrad, a 1-MeV-equivalent neutron fluence of $1.9 \times 10^{14}$ cm$^{-2}$, and a charged hadron fluence of $1.5 \times 10^{13}$ cm$^{-2}$ at the end of its life.

In the following, we will describe the chip design and its features, together with selected measurements to demonstrate its performance.

2. Chip description

The chip is designed in I3T80 0.35 $\mu$m HV CMOS technology from onsemi, which provides both PMOS and NMOS transistors with drain-to-source tolerance of up to 70 V. This technology was already used in the past by other projects at CERN, and its radiation hardness has been successfully qualified up to the radiation levels required by this application\textsuperscript{[4]}. A previous version of the chip, ALDO1\textsuperscript{[5]}, was designed in a different

\textsuperscript{[1]} Corresponding author
Email address: paolo.carniti@mib.infn.it (P. Carniti)
0.35 µm CMOS technology limited to 3.3 V and provided the basis for the design of ALDO2.

The ALDO2 chip features four independent and fully adjustable low dropout (LDO) linear regulator channels. They are all based on the standard LDO topology with an error amplifier driving a PMOS pass transistor that provides the current drive capability to the load. Figure 1 shows the ASIC block diagram, on the left the low voltage regulators, on the right the HV ones.

The first regulator provides the main power to front-end chips and thus features low voltage (max 3.3 V input) and high current (max 0.6 A). The dropout can be as low as 550 mV even at full load and after irradiation up to the levels expected in these detectors. The second regulator is low voltage and low current (max 20 mA) and can be used to power sensitive circuitry of the detectors. The second regulator is low voltage and low current (max 0.6 A) and can be used to power sensitive circuitry of the detectors. The compensation for all the four regulators is external, using low ESR tantalum capacitors. The BTL detector will adopt low profile (1.8 mm) 50 V ones, given the tight space constraints.

The voltage reference of these two regulators can be selected among three internal bandgap references, one based on PNP bipolar transistors, one on NPN, and one on dynamic-threshold MOSFETs (DTMOS). In the final application, the chip will use the one that offers the best compromise between radiation hardness and stability.

Both regulators are adjustable, and the user can then set the desired output voltage with the external feedback network from the output to the feedback node of the error amplifier.

The last two regulators, out of the four included in the ALDO2, are those used to generate the bias for SiPM arrays. They are two identical high voltage regulators with a maximum input voltage of 70 V and a maximum output current of 45 mA. They allow complete flexibility to the user by tuning both the gain (through the external resistive divider, like for the LV regulators) and the reference voltage (using an external DAC). In this way, the user would choose a custom, but fixed, output voltage range with the voltage divider and then tune the output voltage during detector operation by programming different values of the reference with the DAC. In BTL this DAC is implemented in the front-end chip (TOFHIR) [6], while in HGCAL the DAC is implemented in the slow control ASIC (GBT-SCA) [7]. The bias voltage regulators also provide a measurement of the output currents, allowing to periodically perform I-V scans and thus determine the breakdown voltage of each array. This measurement is performed with two ranges (×20 ratio) by mirroring the output current and converting it to a voltage with a precise external resistor.

All the regulators are protected against over-current and over-temperature to avoid self-damage in a faulty condition of the load. Furthermore, the three main regulators (the LV high-current one and the HV ones) can be individually disabled using external digital signals, allowing power cycling of front-end chips or disabling faulty SiPM arrays. For BTL, for example, this last feature limits the propagation of the fault of one single SiPM to just one array of 16 SiPMs, rather than to all the 768 SiPMs that share the same bias line. Unlike readout node trimming solutions, the regulation on the high side of the SIPM bias allows good filtering of noise coming from the supply and does not add parasitics to the input of the readout chip.

The compensation for all the four regulators is external, using low ESR tantalum capacitors. The BTL detector will adopt low profile (1.8 mm) 50 V ones, given the tight space constraints.

In addition to the choice of onsemi I3T80 technology, radiation hardness is also improved with specific design choices: enclosed layout NMOS transistors (ELTs), “guarded” HV NMOS transistors, use of guard-rings and large spacing, abundant substrate contacts, strict anti-latchup rules.

The chip die dimension is about 2.5 × 2 mm² and it is packaged in QFN64 9 × 9 mm². Figure 2 shows two photographs of the ALDO2 die inside an OpenPak QFN.

The chip prototyping phase took three iterations. ALDO2v0, produced in 2019, was the first prototype but already implemented all the chip functionalities. It was produced in 80 samples and packaged in OpenPak QFN. The second iteration, ALDO2v1, had a few minor improvements related to over-current limits, bandgap trimming, and over-temperature protection circuit. About 1000 samples were produced from 8 different wafers, which allowed to test the wafer-by-wafer spread. ALDO2v1 was packaged in the final molded plastic (punched) QFN64 by ASE. The last iteration, ALDO2v2, is the one that was sent for production. The only change was an optional (thereby fail-safe) feature to generate the bias voltages of the

Figure 1: Block diagram of the ALDO2 ASIC. On the left: low voltage part of the chip. On the right: one of the two (identical) high voltage regulators.
HV regulators internally.

3. Measurements

The ASIC’s performance has been thoroughly characterized on stand-alone test boards and when mounted on the prototype boards designed for BTL and HGCAL detectors that integrate front-end chips and the final SiPM arrays. These boards were also used successfully during test beam campaigns, proving the ALDO2 functionalities on the field.

In the following, the main results will be presented.

3.1. Thermal stability and spread

The thermal stability of the bandgap voltage references was tested in a climatic chamber. The PNP-based bandgap showed the best stability, about 20 ppm/°C from −40 °C to 80 °C, with flat slope around 0 °C, as expected. The DTMOS-based one was the second-best, with about 50 ppm/°C drift and a higher quadratic slope. The NPN-based shows a drift of about 120 ppm/°C. The output voltage shows the same stability of the bandgap used to provide the reference to the error amplifier, confirming that no additional drifts are introduced by the error amplifier or by the pass transistor. Figure 3 shows the thermal drift of the output voltage in the range from −40 °C to 50 °C, using the DTMOS bandgap as reference. The curve is fitted with a 4th-grade polynomial and then differentiated to get the thermal coefficient as a function of temperature (right axis).

The spread of the bandgap voltages, and consequently the outputs, is about 0.7% RMS even with chips coming from different wafers. Thus there will be no need to trim the value of the bandgap chip by chip. Figure 4 shows the spread of the DTMOS-based bandgap reference voltage in the 105 chips tested from the ALDO2v1 prototyping run.

3.2. Line regulation, PSRR, and load regulation

Another important parameter of the ALDO2 is the capability to maintain the output stable, regardless of any input voltage variation, both in DC (line regulation) and over frequency (power supply rejection ratio, PSRR). These parameters largely depend on the output load and dropout, and are also sensitive to the radiation hardness, as will be shown.

On the LV regulator, line regulation is about −46 dB at 500 mA load, and PSRR is better than −26 dB over the entire frequency range up to 10 MHz, as shown in Figure 5 with a dropout of 600 mV. The HV regulator has a line regulation of −48 dB at a load of 43 mA and 2 V dropout.

The load regulation (the output voltage variation with different output loads) is 5 mV/A (0.42 %/A with 1.2 V output) for the LV regulator and 0.3 mV/mA (7.5 ppm/mA with 40 V output) for the HV regulator. Figure 6 shows two oscilloscope screenshots with load steps on LV (top) and HV (bottom) output, where it is also possible to appreciate the high stability of the regulators since little or no ringing is present.

Figure 3: Thermal drift of the main output voltage between −40 °C and 50 °C.

Figure 4: Distribution of the DTMOS-based bandgap reference voltage in the 105 chips tested from the ALDO2v1 prototyping run.

Figure 5: PSRR of the main low voltage regulator at different loads.

Figure 6: Load current steps on LV (top) and HV (bottom) outputs. The steps are 500 mA on the LV and 20 mA on the HV. Some ground noise on the oscilloscope probe is visible due to the SPI communication to set the output load.
3.3. Noise

ALDO2 is able to effectively filter any input noise thanks to its high PSRR. Its intrinsic noise at the outputs is 27 $\mu$V RMS for the LV regulator and 350 $\mu$V RMS for the HV regulator (at 500 mA and 20 mA load, respectively), in a bandwidth between 10 Hz and 100 MHz. In the detectors, the main contribution to the HV output voltage noise will come from the DAC reference noise, which cannot be fully filtered due to board space constraints. The DAC noise is amplified by a factor of about 40 to generate the typical SiPM bias voltage, resulting in an output RMS noise of less than 2 mV RMS.

4. Radiation hardness tests

The highest radiation levels that the ALDO2 will have to experience during its operation are those in the BTL detector: a TID of 3.2 Mrad, a 1-MeV-equivalent neutron fluence of $1.9 \times 10^{14}$ cm$^{-2}$, and a charged hadron fluence of $1.5 \times 10^{13}$ cm$^{-2}$ after the nominal integrated luminosity of 3000 fb$^{-1}$. The HGCAL, although being in the endcap sector, is in fact much further from the interaction point and most of the radiation is already shielded by the inner part of the calorimeter itself.

The radiation hardness qualification was performed in several laboratories. The TID irradiation with X-rays was done at the Karlsruhe Institute of Technology (Germany) in 2 steps, one at 7 Mrad and one at 20 Mrad, which correspond to a factor 2 and 6 above the expected levels. The neutron irradiation was performed at LENA nuclear reactor in Pavia (Italy), with 1-MeV-equivalent fluences of $2.5 \times 10^{14}$ cm$^{-2}$ and $1 \times 10^{15}$ cm$^{-2}$ ($\times 1.3$ and $\times 5$). The heavy-ion irradiation for single-event effects was done at the SIRAD facility in Legnaro (Italy), using several ion types with LETs up to 40 MeV cm$^2$ mg$^{-1}$ and a cumulative fluence of $10^{10}$ cm$^{-2}$.

The chips were monitored online during the X-ray and heavy-ion irradiations to check any drift or transient at nominal operating loads. Single event transients (SETs) were observed at high LET (28 MeV cm$^2$ mg$^{-1}$ and above), initially with an estimated cross-section of $10^{-3}$ cm$^{-2}$. The cause was then identified, and mitigation was put in place by improving the filtering of the over-temperature protection threshold. The cross-section of these SETs was thus lowered to $2 \times 10^{-2}$ cm$^{-2}$, which would correspond to a rate below 1 mHz in the final detector. It is also worth noting that the amplitude and duration of these transients are very small, 20 mV and 10 $\mu$s for the LV regulator and 80 mV and 100 $\mu$s for the HV regulator, and they are not expected to affect the detector performance. Figure 7 shows an example of SETs on the HV output voltage.

Measurements on the bandgaps of irradiated devices confirmed that the one that offers the best compromise between radiation hardness and stability is the one based on DTMOS, with drifts below 2% even after 7 Mrad of TID. Measurements of the line and load regulation of the irradiated devices allowed to set the minimum dropout to 550 mV for the LV regulator and 3 V for the HV regulator at nominal loads.

5. Conclusions and prospects

The chip development has been completed and the measured performance has fulfilled the requirements of BTL and HGCAL detectors. The production of the 19k chips required will be completed by mid-2022. Due to the selling of the I3T80 onsemi fab in Belgium, where all the prototypes were manufactured, there will not be another possibility to produce more chips in this fab, which demonstrated adequate radiation tolerance. It was thus decided to manufacture many more chips than needed (45k), just to be prepared in case of unexpectedly low production or packaging yields. However, a second I3T80 fab is still operating in the USA, although using this one would require to re-do all the radiation hardness qualification, which is not acceptable for the schedule of BTL and HGCAL, but could be pursued if other users would be interested in adopting the ALDO2 ASIC in their detectors.

Acknowledgments

The authors would like to thank all the colleagues at KIT (Karlsruhe), LENA (Pavia), and LNL (Legnaro) for their invaluable help and support during the irradiation campaigns.

References

[1] The CMS Collaboration, A MIP Timing Detector for the CMS Phase-2 Upgrade, Tech. rep., CERN (2019). URL https://cds.cern.ch/record/2687187
[2] The CMS Collaboration, The Phase-2 Upgrade of the CMS Endcap Calorimeter, Tech. rep., CERN (2017). URL http://cds.cern.ch/record/2293646
[3] M. Calvi, et al., Single photon detection with SiPMs irradiated up to $10^{15}$ cm$^{-2}$ 1-MeV-equivalent neutron fluence, Nucl. Instrum. Meth. A 922 (2019) 243–249. doi:10.1016/j.nima.2015.10.054
[4] F. Fascio, et al., TID and Displacement Damage Effects in Vertical and Lateral Power MOSFETs for Integrated DC-DC Converters, IEEE Transactions on Nuclear Science 57 (4) (2010) 1790–1797. doi:10.1109/TNS.2010.2049584
[5] P. Carniti, et al., ALDO: A radiation-tolerant, low-noise, adjustable low drop-out linear regulator in 0.35 $\mu$m CMOS technology, Nucl. Instrum. Meth. A 824 (2016) 258–259. doi:10.1016/j.nima.2015.10.054
[6] E. Albuquerque, et al., TOFHIR2: The readout ASIC of the CMS Barrel MIP Timing Detector, in: 2020 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2020, pp. 1–7. doi:10.1109/NSS.2020.9507749
[7] A. Caratelli, et al., The GBT-SCA, a radiation tolerant ASIC for detector control and monitoring applications in HEP experiments, Journal of Instrumentation 10 (03) (2015) C03034–C03034. doi:10.1088/1748-0221/10/03/c03034