A Memory Window Expression to Predict the Scaling Trends and Endurance of FeFETs

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Abstract—The commercialization of non-volatile memories based on ferroelectric transistors (FeFETs) has remained elusive due to scaling, retention, and endurance issues. Thus, it is important to develop accurate characterization tools to quantify the scaling and reliability limits of FeFETs. In this work, we propose to exploit an analytical expression for the Memory Window (MW) as a tool to: i) identify a universal scaling behavior of MW regardless of the ferroelectric material; ii) predict endurance and explain its weak dependence on writing conditions; iii) give an alternative explanation for MW being lower than theoretical limits; and, based on this, iv) devise strategies to maximize MW for a given ferroelectric thickness. According to these findings, the characterization and analysis of MW would enable the systematic comparison of next-generation FeFET based on emerging ferroelectric materials.

Index Terms—Ferroelectric MOSFETs (FeFETs), Non-Volatile Memories, Memory Window, Scaling, Endurance

I. INTRODUCTION

The first demonstration of a thin-film ferroelectric transistor (FeFET) by Moll and Tarui in the early 1960s fueled the tantalizing promise of Non-Volatile Memories (NVMs) based on such technology [1]. Successive generations of FeFETs have revived the interest of the community [2]–[4], only to realize that the issues of the technology related to scaling, retention, and endurance hindered commercialization. Although FeFETs offer better nonvolatility, scaling potential, higher read-write speeds and lower dissipation power over other memory devices such as DRAM, SRAM, and Flash memory [2], their reduced retention and endurance compared to other novel NVMs such as Resistive RAMs and Phase-Change RAMs [5] have restricted their adoption. Nonetheless, the successful demonstration of a CMOS-compatible FeFET would advance a broad range of applications, such as: i) Logic-In-Memory (LiM) circuits [6]; ii) artificial neural networks [7], [8]; and iii) Ternary Content Addressable Memories (TCAMs) [6], [8]. Given the 50+ years history and the potential of the technology, it is important to develop accurate characterization tools to quantify endurance/retention and identify the limits of latest generation FeFETs based on HfO$_2$ and ZrO$_2$ binary oxides [9].

In this work, we derive an analytical expression for the MW that can be used to interpret experiments, quantify the scaling limits of FeFETs as well as the endurance of such devices. The MW is a useful metric that allows comparing the performance of FeFETs regardless of the application or the specific technology. The theoretical framework for ferroelectric MOSFETs employed in this work is based on the Landau-Devonshire theory, which was originally developed to explain the operation of Negative Capacitance transistors (NCFETs) [10] and later exploited to model the operation of hysteretic ferroelectric transistors with a simplified structure [11]. Here, we generalize the approach presented in [11] to realistic Metal-Ferroelectric-Insulator-Semiconductor (MFIS) stacks to derive a simple expression for MW that under specific assumptions and approximations can be used as a tool to: i) identify a universal scaling behavior regardless of the ferroelectric material; ii) predict endurance and explain its weak dependence on writing conditions; iii) and devise strategies to maximize MW for a given ferroelectric thickness. The analysis provides insights into the features of FeFET that generally are left unveiled by results based on TCAD simulations.

The paper is organized as follows. In Section II we discuss the derivation of the analytical model, the limits of validity of the approach, and the design guidelines to maximize MW. In Section III we present the results in terms of MW scaling and endurance. In Section IV we draw the conclusions of the work. In the Appendix we show the validation of the analytical expressions with numerical simulations and the comparison with another FeFET model.

II. ANALYTICAL MODEL

A. Derivation of $V_{th,on}$, $V_{th,off}$ and MW Expressions

In this section, we present the derivation of the on- and off-threshold voltage, $V_{th,on}$, $V_{th,off}$, and MW analytical expressions for the Metal-Ferroelectric-Insulator-Semiconductor
(MFIS) stack, which is the most common device structure for FeFETs [3] (another option includes an additional metal layer between the ferroelectric and the insulator (MFMIS) [10], [12], [13]). From a physical point of view, $MW$ is determined by the polarization switching of the ferroelectric layer present in the gate stack and the state of the memory is encoded as the channel conductance at a particular gate bias, i.e., $V_{\text{READ}}$ (for Non-Volatile Memories, $V_{\text{READ}} \approx 0$). In this context, the $MW$ is defined simply as $MW = V_{\text{h.on}} - V_{\text{h.off}}$. The $MW$ is derived by generalizing the approach followed in [11], with the inclusion of i) the SiO$_2$ interface layer between the ferroelectric layer and the semiconductor channel, and ii) the linear component of the ferroelectric layer [14]. The analytical $MW$ expression allows identifying the key parameters that influence the scaling trends of FeFETs, as explained later.

The derivation starts with the model of the electrostatic behavior of the FeFET, obtained by coupling the classical MOSFET surface potential equation (SPE) with the Landau-Devonshire theory [11], [15]:

$$V_{\text{GS}} - V_{\text{FB}} = V_{\text{ins}} + \psi_i$$

(1)

where $V_{\text{GS}}$ is the applied gate bias, $V_{\text{FB}}$ is the flatband voltage, $V_{\text{ins}}$ is the insulator voltage (including both ferroelectric and oxide interface layer), and $\psi_i$ is the surface potential. $V_{\text{ins}}$ is expressed as follows:

$$V_{\text{ins}} = Q_s \left( \frac{1}{C_{\text{LD}}} + \frac{1}{C_{\text{ox}}} \right)$$

(2)

where $C_{\text{ox}} = \varepsilon_{\text{ox}}/t_{\text{ox}}$ is the oxide interface layer capacitance and

$$C_{\text{LD}} = \frac{1}{t_{\text{FE}} (2\alpha + 12\beta Q_s^2)}$$

(3)

are the capacitance components of the ferroelectric due to polarization (obtained from Landau-Devonshire theory), $C_{\text{LD}}$, and linear dielectric behavior [14], $C_{\text{FE}}$, respectively. $Q_s$ is the semiconductor charge, $\alpha$, $\beta$ are the Landau parameters for the ferroelectric layer, $\varepsilon_{\text{FE}}$ is the linear dielectric constant of the ferroelectric layer, $t_{\text{FE}}$ is the ferroelectric thickness.

As mentioned in Section II, the Landau-Devonshire formalism is conventionally adopted to describe the behavior of NCFETs [10], [14], [15] which occurs under particular conditions leading to $\psi_i$ amplification (for a given $V_{\text{GS}}$) and sub-threshold swing, $SS$, below the Boltzmann limit of 60mV/dec. The theory, however, allows describing also the hysteretic behavior of ferroelectrics that occurs when the total gate capacitance is negative [16], [17]. Mathematically, FeFET memory operation is guaranteed by the following inequality:

$$MW > 0 \Leftrightarrow \left( \frac{1}{C_{\text{LD}}} + \frac{1}{C_{\text{ ox}}} \right) < 0$$

(4)

which can be more conveniently expressed in terms of $t_{\text{FE}}$ and $t_{\text{ox}}$ as follows (by neglecting higher-order terms):

$$t_{\text{ox}} < t_{\text{FE}} = \frac{2|\varepsilon_{\text{ox}}|}{1 - 2|\alpha|\varepsilon_{\text{FE}}}$$

(5)

The constraint defined by (5) imposes a maximum allowed $t_{\text{ox}}$ for a given $t_{\text{FE}}$ (or vice-versa, a minimum $t_{\text{FE}}$ for a given $t_{\text{ox}}$), to achieve $MW > 0$. This is visualized in Fig. 1 that shows the transition between hysteretic regime (i.e., $MW > 0$) and negative capacitance regime: (5) is in fact the opposite condition to that of stable negative-capacitance operation [14].

To reach closed-form expressions for $V_{\text{h.on}}$, $V_{\text{h.off}}$ and $MW$, we simplify the $Q_s$ expression by considering only the inversion layer charge [11]. The on-threshold voltage, $V_{\text{h.on}}$, is obtained by solving for $\partial Q_s / \partial \psi_i = 0$, which is the condition at which the FeFET is about to enter the so-called negative capacitance region [10]. Because the total gate capacitance is negative, and therefore unstable, the ferroelectric switches to the saturated polarization value (skipping the negative capacitance region), turning on the device: this is the $V_{\text{h.on}}$ condition. The final expression is then written as [neglecting higher-order terms in (2) and (5)]:

$$V_{\text{h.on}} = V_{\text{FB}} + 2V_i \ln \left( \frac{Q_s}{Q_0} \right) - 2V_i$$

(6)

where $V_i = kBT/q$ is the thermal voltage, $k_B$ is the Boltzmann constant, $T$ is the device temperature, $q$ is the elementary charge, and $a = 2\alpha t_{\text{FE}} / (1 + 2\alpha_{\text{FE}}) + 1/C_{\text{ox}}$. $Q_0 = \sqrt{2e k_B T n_i^2 N_a}$ is the pre-exponential term of the inversion charge expression, namely $Q_s = Q_0 \exp(\psi_i / 2V_i)$, where $\psi_i$ is the semiconductor dielectric constant, $n_i$ is the intrinsic carrier density, and $N_a$ is the substrate doping density (we consider a p-type substrate for a NMOS device). The off-threshold voltage, $V_{\text{h.off}}$, is obtained instead by solving for $\partial Q_s / \partial V_{\text{ms}} = 0$ (with $Q_s > 0$). At this condition the FeFET load-line is again at the boundary of the negative capacitance region, but in the opposite direction with respect to the previous case (for $V_{\text{h.on}}$), and the ferroelectric switching causes the device to turn off. (A more detailed discussion on why the condition for on- and off-switching are non-symmetrical is found in Section II-C).

The final expression is as follows:

$$V_{\text{h.off}} = V_{\text{FB}} + 2V_i \ln \left( \frac{Q_{sw}}{Q_0} \right) - V_{sw}$$

(7)

where $V_{sw}$ is the switching voltage, defining the boundary between the positive and negative capacitance region, occurring at the switching charge $Q_{sw}$. Considering $\varepsilon_{\text{FE}} = 0$ allows
writing a simple expression for $V_{sw}$ and $Q_{sw}$:

$$V_{sw} = \left(-aQ_{sw} + bQ_{sw}^2\right) = \frac{2}{3}a|Q_{sw}| \quad (8a)$$

$$a = 2\alpha C_{FE} + \frac{1}{C_{ox}} \quad b = 4\beta C_{FE} \quad Q_{sw} = \sqrt{\frac{|a|}{3b}} \quad (8b)$$

Finally, the memory window expression, $MW$, is obtained simply by subtracting (7) from (6):

$$MW = 2V_i \ln \left|\frac{2V_i}{|a|Q_{sw}}\right| + (V_{sw} - 2V_i). \quad (9)$$

This expression is the key result of the paper, determined by the $\psi_t$ and the $V_{th}$ difference between the on- and off-switching conditions, corresponding to the first and second term in (9), respectively. Interestingly, the $MW$ does not depend on $V_{FB}$, nor on the doping of the substrate because $V_{th, on}$ and $V_{th, off}$ are both affected by them. As highlighted by (9), $MW$ primarily depends on $V_{sw}$ which gives rise to a universal scaling trend for the $MW$. This is one of the main contributions of this work. In Section 3-A we will exploit (9) to predict the scaling trends and endurance limits of FeFETs.

**B. Applicability Limits of the Modeling Approach**

As specified in Section 1 the derivation of the analytical expressions (6)-(7), (9) was carried out starting from the Landau-Devonshire phenomenological theory (also known as single-domain approximation) which treats ferroelectric as an homogeneous layer where, under the specific conditions discussed in Section 1-A, switching occurs between the two stable saturated polarization values [10]. In general, non-uniform polarization present in realistic ferroelectric thin layers can only be captured only with the generalized Landau-Ginzburg theory that includes a domain interaction term in the expression of the free-energy [14]. However, recent attempts in the literature such as [18], demonstrate that it is possible to equivalently reproduce the effect of multi-domain interaction (which leads to gradual polarization switching) with the single-domain model by considering finite ferroelectric switching time. In this work, we restricted the analysis to ‘empirically’ reproduce $MW$ of realistic FeFETs with effective $\alpha$, $\beta$ parameters that are able to capture the switching behavior of the saturated loops and neglecting the non-idealities that could reduce $MW$ (i.e., counteracting trapping phenomena, wake-up of ferroelectric and other effects [4]).

Another important aspect related to ferroelectric HfO$_2$ is the polycrystalline (i.e., amorphous) structure of realistic layers, which leads to fluctuations in properties of ferroelectric (such as the coercive field, $E_C$) [19]. Although beyond the scope of this work, we mention that the analytical model can be used to investigate the effect of $E_C$ variations, for example, by carrying out the derivation of (9) with respect to both $\alpha$, $\beta$ considering that $E_C \approx -4/3\alpha \sqrt{-\beta/6\beta}$ with $\varepsilon_{FE} = 0$ [15].

**C. Non-Symmetric Switching Conditions**

The lack of symmetry between $V_{th, on}$ and $V_{th, off}$ expressions is essentially caused by the non-linear $\psi_t$ and $Q_t$ vs $V_{GS}$ curves, see Fig. 2. At $V_{th, off}$, see Fig. 2(b) $Q_t$ is equal to the critical $Q_{sw}$ value and this leads to a linear dependence of $V_{th, off}$ on $V_{sw}$ as expressed by (7). Conversely, since $Q_t(V_{th, on}) > 0$, $V_{th, on}$ cannot be proportional to $V_{sw}$ because this would require $Q_t < 0$ (if $Q_{sw}$ is positive then $V_{sw}$ is negative, and vice-versa). $Q_t < 0$ could only occur in the accumulation region, for $V_{GS} < V_{FB}$.

**D. Guidelines to Maximize MW**

The most obvious design strategy to increase $MW$ is to increase $t_{FE}$, as reported in [20], where a 20-nm-thick ferroelectric was employed to roughly double $MW$. However, this solution goes in contrast with the need of scaling the technology. In the following, with the aid of the analytical model we discuss other possible strategies to maximize $MW$ without compromising FeFET scaling.

The first is based on the consideration that non-symmetric switching conditions reduce the maximum $MW$ because $V_{th, on}$ is not proportional to $V_{sw}$, as discussed in Section 1-C. As also pointed out in [11], the theory predicts that another hysteresis loop can form between accumulation and depletion region that is basically symmetrical to the one from inversion to depletion discussed previously (as the accumulation charge also depends exponentially on $\psi_t$). Thus, in principle, if a FeFET could switch from accumulation to inversion (and vice-versa), skipping the depletion region, then the switching conditions would become symmetrical and $MW$ would consequently increase. To achieve this, the condition $V_{th, on} < V_{FB}$ [with $V_{th, on}$ defined as in (6)] would have to be satisfied.

Another possible way to increase $MW$ at the same $t_{FE}$ and approaching the maximum theoretical limit [21], [22]:

$$MW_{MAX} = 2E_C \times t_{FE}, \quad (10)$$

to engineer the insulator layer between the ferroelectric and the semiconductor. This goal can be achieved by either scaling $t_{ox}$ or increasing $\varepsilon_{ox}$ (i.e., by employing high-$\kappa$ insulators).

In the limit, the oxide layer should be removed to maximize $MW$: in fact, with $t_{ox} \rightarrow 0$ then $MW$ would increase of $\approx 50\%$ for $t_{FE} = 10$nm and the ferroelectric parameters reported in Table II.
Fig. 3. (a) comparison of the calculated $MW$ values vs $t_{FE}$ with Eq. (9) with experimental data from [4]. (b) comparison of the same $MW$ data from [3] plotted vs $V_{sw}$ revealing a similar trend regardless of the particular ferroelectric material. This suggests an universal scaling behavior with $V_{sw}$, which is physically connected to the ferroelectric and transistor parameters.

### III. Results

#### A. Geometrical and Universal Scaling of $MW$

To verify the scaling trends of $MW$ vs $t_{FE}$ predicted by (9) we compared the analytical results with experimental data on FeFET scaling trends recently published in [4] for Zr- and Si-doped HfO$_2$ (i.e., HZO and HSO) ferroelectrics. Fig. 3(a) shows the experimental $MW$ vs $t_{FE}$ data points (symbols) taken from [4] and the results obtained from (9) (lines). The ferroelectric parameters were set as follows: $\alpha_{HZO} = -3 \times 10^{9}$ m/F, $\beta_{HZO} = 5 \times 10^{10}$ m$^2$/F/C$^2$ and $\alpha_{HSO} = -3 \times 10^{9}$ m/F, $\beta_{HSO} = 1.2 \times 10^{10}$ m$^2$/F/C$^2$, respectively. In both cases, $\varepsilon_{FE}$ was set to 16. Since $V_{sw} \propto t_{FE}$ and $MW \sim V_{sw} \propto t_{FE}$, our model correctly anticipates the universal trend of the measured $MW$ (symbols) as a function of $V_{sw}$ (lines). This important result comes from the fact that $V_{sw}$ embeds the specific ferroelectric and geometric parameters and implies that regardless of the technology the scaling follows the same trend.

#### B. Assessing Endurance from $MW$ Expression

As discussed in Section II commercialization of FeFET has been hindered by the limited retention and endurance with respect to other technologies. Retention is defined as the time taken for the different states to no longer distinguishable during a prolonged read operation. Instead, endurance is the time taken before states are indistinguishable after repeated program/erase operations. HfO$_2$-based FeFETs have reduced trapping and lower depolarization over coercive field ratio with respect to PZT- or SBT-based devices leading to improved retention time [25]. However, endurance is still a major issue for this technology imposing an upper limit of $\sim 10^8$ - $10^9$ writing cycles [20], [26] that is far from meeting the International Roadmap for Devices and Systems (IRDS) requirements of $10^{12}$ cycles [27]. At the basis of the limited endurance lies the increasing trapping due to the generation of oxide and interface states in the layer between the ferroelectric and the semiconductor body [28]. This is a consequence of the lower dielectric constant of SiO$_2$ compared to that of doped-HfO$_2$, that causes the local electric field to increase, accelerating generation of defects.

In the following, derive an expression for the degraded $MW$ during endurance tests. Fast $MW$ decay due to depolarization fields and trapping/detrapping was not explicitly included in the model as it is expected to mainly influence retention rather than endurance [25], [28]. Our analysis focuses on both oxide and interface traps generation during these tests, were the gate voltage is cycled with program and erase pulses to induce ferroelectric switching. The prolonged effect of high voltage pulses over time induces degradation in the form of generation of defects, and this is modeled with the analytical formula derived in Section II by adding the contribution due to the defects in the right-hand side of the SPE [29]:

$$V_{ot} = -\frac{q \Delta N_{ot}}{C_{ox}} \quad V_{b} = \frac{q \Delta D_{it}}{C_{ox}} (\psi_s - \phi_b)$$

where $\Delta N_{ot}$ is the generated trap concentration in the oxide interface layer (cm$^{-2}$), $\Delta D_{it}$ is the generated interface trap density of states (cm$^{-2}$eV$^{-1}$), and $\phi_b$ is the body potential. These expressions assume that the charge neutrality level for the interface traps is located at Si mid-gap [29]. The stress causing generation of traps is induced by positive and negative pulses on the gate performing erase and program operations in the FeFET, respectively. Hence, $V_{th,on}$ will tend to decrease and $V_{th,off}$ to increase [24]. The concentration of generated defects during writing of the memory is in general different depending on the sign of the writing pulse, therefore the shifts in $V_{th,off}$ and $V_{th,off}$ will not be symmetric. Thus, we will use different symbols to indicate the generated defects during program and erase cycles, namely $\Delta N_{ot,PE}$ and $\Delta D_{it,PE}$ for oxide and interface traps, respectively.

The degraded $V_{th,on}$, $V_{th,off}$, and $MW$ expressions are derived by rewriting the threshold conditions, taking into account the additional potential drop due to defects expressed in (11) (the algebraic manipulations for the derivation of these expressions are straightforward and are omitted for brevity). The $V_{th}$’s and $MW$’s degradation is expressed as follows:

$$\Delta V_{th,on} = 2V_i \ln \left( 1 + \frac{q \Delta D_{it,PE}}{C_{ox}} \right) \times \left( 1 + \frac{q \Delta D_{it,P}}{C_{ox}} \right)$$

$$- \frac{q}{C_{ox}} \times \left\{ \Delta N_{ot,P} - \Delta D_{it,P} \right\} \left[ 2V_i \ln \left( \frac{2V_i}{|\psi_s|Q_0} \right) - 2V_i - \phi_b \right\}$$

$$\Delta V_{th,off} = -\frac{q}{C_{ox}} \left\{ \Delta N_{ot,E} - \Delta D_{it,E} \right\} \left[ 2V_i \ln \left( \frac{Q_{sw}}{Q_0} \right) - \phi_b \right\}$$

$$\Delta MW = 2V_i \ln \left( 1 + \frac{q \Delta D_{it,PE}}{C_{ox}} \right) \times \left( 1 + \frac{q \Delta D_{it,P}}{C_{ox}} \right)$$

$$- \frac{q}{C_{ox}} \left\{ \Delta N_{ot,P} - \Delta N_{ot,E} - 2V_i \Delta D_{it,P} \ln \left( \frac{2V_i}{|\psi_s|Q_0} \right) - 1 \right\}$$

$$+ 2V_i \Delta D_{it,E} \ln \left( \frac{Q_{sw}}{Q_0} \right) + (\Delta D_{it,P} - \Delta D_{it,E}) \phi_b \right\}.$$
Calculated (dashed lines) and measured (symbols) \( \Delta V_{\text{th, on}} \) and \( \Delta V_{\text{th, off}} \) vs program/erase cycle number. Experimental data is taken from [24]. The different panels show different program/erase pulse amplitude. (a) \( |V_{P/E}| = 4.2 \text{ V} \), (b) \( |V_{P/E}| = 4.85 \text{ V} \), and (c) \( |V_{P/E}| = 5.5 \text{ V} \), respectively.

The trend of the degraded thresholds and MW is fully captured by \( V_{ot} \) and \( V_{d} \) only. This happens because degradation primarily occurs in the insulator layer, as discussed previously. From this observation, simplified formula can be derived for \( \Delta V_{\text{th, on}}, \Delta V_{\text{th, off}} \) and \( MW \). By neglecting \( V_{\text{ins}} \) variations in [12a]-[12c] we obtain the following:

\[
\Delta V'_{\text{th, on}} \sim \frac{-q}{C_{\text{ox}}} \{ \Delta N_{a,t} - \Delta D_{\delta,t} \left[ 2V_{t} \ln \left( \frac{2V_{t}}{a|Q_{0}|} \right) - \phi_{c} \right] \} 
\]

\[
\Delta V'_{\text{th, off}} \sim \frac{-q}{C_{\text{ox}}} \{ \Delta N_{a,E} - \Delta D_{\delta,E} \left[ 2V_{t} \ln \left( \frac{Q_{\text{in}}}{Q_{0}} \right) - \phi_{c} \right] \} 
\]

\[
\Delta MW' \sim \frac{-q}{C_{\text{ox}}} \left\{ \left( \Delta N_{a,t} - \Delta N_{a,E} \right) - \Delta D_{\delta,t} \right. \\
+ \Delta D_{\delta,E} \left[ 2V_{t} \ln \left( \frac{Q_{\text{in}}}{Q_{0}} \right) \right] \left\} \right. \\
+ \left( \Delta D_{\delta,t} - \Delta D_{\delta,E} \right) \phi_{c} \right. 
\]

Note that \( \Delta V'_{\text{th, on}}, \Delta V'_{\text{th, off}}, \) and \( MW' \) are proportional to the variation introduced by the generation of both oxide and interface defects. The surface potential \( \psi_{s} \) [corresponding to the logarithmic terms in square brackets in (13a)-(13b)] is calculated differently according to the two threshold conditions defined in Section II. As intuition suggests, if the degradation were symmetric, i.e., the generated defects were giving equal and opposite in sign \( V_{ot} \) and \( V_{d} \), the MW variation would be \( \sim -2q/C_{\text{ox}} \times [\Delta N_{a,t} - \Delta N_{a,E} (\psi_{s} - \phi_{c})] \).

The good agreement between analytical and experimental results in Figs. 4 and 5 was obtained by extracting the generated oxide and interface trap concentrations from \( \Delta V_{\text{th, on}} \) and \( \Delta V_{\text{th, off}} \) data in [24] following the approach described in [30]. That is, \( N_{a,t} \) and \( D_{\delta} \) were extracted by separating the threshold voltage shifts due to oxide (\( \Delta V_{\text{ox}} \)) and interface traps (\( \Delta V_{\text{it}} \)) separately. The former is obtained from the mid-gap voltage, \( V_{mg} \), that correlates with \( N_{a,t} \)-induced \( V_{th} \) drifts as at \( V_{G} = V_{mg} \Rightarrow \psi_{s} = \phi_{c} \) and \( \Delta V_{d} = 0 \), see (11); the latter is obtained by \( \Delta V_{d} = \Delta V_{\text{th}} - \Delta V_{\text{ox}} \) [24], [30]. To summarize, (12a)-(12c) transparently connect the FeFET parameters to the stress-dependent oxide and interface trap generation. As such, (12c) offers a powerful new MW-based characterization tool for extracting oxide and interface defects. This could serve either as an alternative to traditional techniques, or a stand-alone method to characterize defect densities under a variety of stress conditions. For instance, notice that when only
Normalized MW degradation calculated from (13c) with only the contribution of ∆N_{ot,p} extrapolated from Fig. 7(a) and ∆N_{ot,E} shown the dependence for different |V_{P/E}| and t_{P/E} values, respectively. A minimum MW threshold is identified.

N_{ot} generation affects MW degradation then it is possible to estimate the net generated traps from (13c):

$$\Delta N_{ot,net} \equiv \Delta N_{ot,p} - \Delta N_{ot,E} \approx -\Delta MW^s C_{ox} \frac{q}{q}$$

This expression allows to simply and directly correlate MW measurements with generated traps. In the next section, we will exploit (13) to provide endurance predictions.

C. Writing Conditions Agnostic Endurance

In the following we will show that, the endurance extrapolated from the equations derived previously is not influenced by the writing conditions (in terms of |V_{P/E}| and t_{P/E}). With the N_{ot} and D_{th} data extracted in Section II-B it is possible to extrapolate the generated trap concentration for an arbitrary number of writing cycles. For simplicity and clarity of presentation, we will assume that the MW degradation is induced by oxide traps only (as supported by the experimental data in [24]) and neglect the generation of interface traps. The generated oxide trap density, N_{ot} is shown in Fig. 6(a) for both program and erase operation that set V_{th, on} and V_{th,off}, respectively. By fitting the experimental data in Fig. 6 it is found that generated oxide trap concentration follows a power law with respect to writing time (the duration of a single writing cycle being t_{cycle} = 200 ns [24]):

$$\Delta N_{ot} \sim N_0 \times (t_{cycle})^\beta$$

where N_0 and \beta are coefficients to fit experimental data, whose values for different writing conditions are collected in Table I. Exponent \beta in the range 0.3 – 0.5 might be a signature of enhanced TDDB due to repeated cycling as reported in [31]. The extrapolated MW degradation obtained by using the predicted \Delta N_{ot} from the generation model is shown in Fig. 4(a) for different |V_{P/E}| and t_{P/E} values, respectively. Note that MW values are normalized to the respective initial value for a fair comparison with different writing conditions. The FeFET is considered to fail to retain its memory operation after reaching the arbitrary minimum MW threshold set as the 20% of the initial value, see Fig. 7. Interestingly, from Fig. 4(a) it appears that |V_{P/E}| increase does not degrade endurance significantly (at least for the range of values as in [24]). This is because higher |V_{P/E}| leads to higher initial MW [4] but also higher ΔN_{ot}, see Fig. 7. Similarly, Fig. 4(b) shows that increasing the pulse duration negligibly influences endurance. Note that in this case it was assumed that t_{P/E} increase leads to the same increase in MW and initial N_{ot} to that caused by |V_{P/E}|. This was done for the specific purpose of illustrating that if both MW and initial N_{ot} increase with program conditions, then the combined effect leads to negligible variation in endurance. Note that in general, if the assumption regarding MW and N_{ot} increase with V_{P/E} (or t_{P/E}) is not satisfied, then the endurance limit will be affected by the writing conditions. The model can also predict the endurance improvement that can be obtained if the generated trap are decreased, either by improving the SiO_2/Si interface quality or by reducing the field in the oxide layer. For example, if N_0 is decreased by one order of magnitude (and assuming every other parameter constant) then endurance can be extended to 10^6 cycles. These considerations can be helpful to develop next generation FeFET with extended endurance.

IV. Conclusions

In this paper, we derived an analytical expression of the Memory Window, MW, that can be used to investigate the scaling trends and endurance limits of FeFETs. Based on the Landau-Devonshire formalism, we arrived at closed-form expressions for the threshold voltages, V_{th, on, off}, and MW for a conventional Metal-Ferroelectric-Insulator-Semiconductor (MFIS) structure that depends on critical technological and geometrical parameters. The MW expression also includes the effect of generated interface and oxide traps to assess the endurance limits of FeFETs. The key findings of this work are as follows:

1) MW as expressed in (9) is a material-independent universal function of switching voltage, V_{sw}, embedding the dependence on critical design parameters.

2) Constraints on minimum ferroelectric thickness (t_{FE}) for a given oxide interface layer thickness (t_{ox}), see (5), impose a trade-off between scaling and MW amplitude.

3) MW can be used to extract oxide and interface trap concentration that are generated during endurance tests, see (14).
4) The generated traps increase as a power-law, see (15), with time exponent $\sim 0.3 - 0.5$. Under specific assumptions, the endurance limit is essentially independent of writing conditions.

5) The $MW$ being lower than the theoretical limit expressed in (10) is due to the non-symmetrical switching conditions.

6) From the $V_{th, on/off}$ analytical expressions in (6)-(7), guidelines can be devised for $MW$ maximization (for a given $t_{FE}$) by engineering the non-symmetric switching conditions or the oxide interface layer.

**APPENDIX I**

**VALIDATION OF THE ANALYTICAL MODEL**

To validate the accuracy of the derived expression and the validity of the underlying assumptions, we compared the analytical result of (9) with numerical simulations. The comparison was done with simulations based on the Landau-Devonshire theory employed in Section II to quantify the discrepancy with the analytical results. Moreover, a comparison was carried out with numerical simulations based on the Preisach model as well, to verify the dependability of the results.

1) **Comparison with Numerical Simulations:** Simulations compute the self-consistent solution for $\psi$, from (1) coupled with the $Q_1$ expression [32]. We considered the ferroelectric parameters for a Si-doped HfO$_2$ (i.e., HSO) as those used in Section II-A (the full parameter set is collected in Table II). The solution for $\psi$, and $Q_1$ was then used to calculate the drain current via the Pao-Sah double integral [11], [32], see Fig. 8 from which the trend of $MW$ with varying $t_{FE}$ was extracted, as shown in Fig. 9. Note that $t_{ox} = 1\, \text{nm}$ was chosen small enough to ensure hysteresis for the whole $t_{FE}$ range considered (as discussed in Section II-A). The agreement between the simulations and the analytical expressions, see Fig. 8 shows that the approximations made in the derivation of (6)-(7) are remarkable. Remotely, the analytical expressions predict a weak decrease of $V_{th, on}$ with increasing $t_{FE}$, whereas $V_{th, off}$ decreases linearly, see Fig. 8(c) (6). This behavior follows from the consideration made in Section II-C on the non-symmetric switching, regarding the different conditions under which $V_{th, on}$ and $V_{th, off}$ are derived.

**APPENDIX II**

**COMPARISON WITH PREISACH MODEL**

Ferroelectric switching behavior is described in the literature also by other models besides the one discussed in this work. Here we focus on the Preisach model [16] which is broadly employed to interpret experimental results of FeFETs. In the framework of this model, the fact that measured $MW$ is lower than the theoretical limit, see (10), is attributed to sub-hysteresis trajectories in the $P-V$ loop followed depending on the writing conditions [21], [33], [34]. The theoretical limit is thus not reached due to switching events with $E < E_C$. In the case of the Landau formalism followed in this work, the same result of $MW$ being lower than $MW_{\text{MAX}}$ can be ascribed to non-symmetric switching conditions, as explained also in Section II-C. This is supported by the comparison of the analytical $MW$ results with numerical simulations carried out with a commercial software [35] on an MFIS structure.
with the Preisach model (the same parameter set was used, see Table I). We performed numerical simulations with the Preisach model because, unlike with (9), it is not possible to derive a closed-form solution for the \( MW \), because the switching points for the inner loops depend on the ferroelectric history and cannot be determined \textit{a priori}. The comparison between the analytical expression derived in this work, the Preisach model and experimental data (from [4], [20]) shown in Fig. 4 confirms the fact that \( MW \) obtained both with Preisach and Landau model is below the theoretical limit \( MW_{\text{MAX}} \).

**APPENDIX III**

**OUTLINE OF THE DERIVATION OF (12a)–(12b)**

As mentioned in Section III-B, the expressions for \( \Delta V_{\text{th,off}} \), \( \Delta V_{\text{th,on}} \), see (12a)–(12b), were derived by following the same procedure of Section III-A by modifying (1) as follows:

\[
V_{\text{GS}} - V_{\text{FB}} = V_{\text{ins}} - \frac{q \Delta N_{\text{d,p}}/E}{C_{\text{ox}}} + \frac{q \Delta N_{\text{d,p}}/E}{C_{\text{ox}}} \left( \psi_s - \phi_0 \right)
\]

(16)

with the same symbols as previously defined. For \( \Delta V_{\text{th,off}} \), the expression for the charge at the switching condition \( (\partial V_{\text{GS}}/\partial \psi_s = 0) \) reads:

\[
Q_s(\Delta V_{\text{th,off}}) = -\frac{2V_s}{a} \left( 1 + \frac{q \Delta N_{\text{d,p}}/E}{C_{\text{ox}}} \right).
\]

(17)

By substituting (17) and the corresponding \( \psi_s \) (obtained as \( \psi_s = 2V_{\text{ss}} \ln \left( Q_s/Q_0 \right) \)) in (16), one obtains (12a). For \( \Delta V_{\text{th,on}} \), the switching condition \( (\partial Q_s/\partial V_{\text{ins}} = 0) \) does not alter \( Q_{\text{sw}} \) and corresponding \( \psi_s \) expressions. Thus, (12b) is simply obtained by substituting \( \psi_s = 2V_{\text{ss}} \ln Q_{\text{sw}}/Q_0 \) in (16). The expression for \( \Delta MW \), see (12c), is obtained by subtracting (12b) from (12a).

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