Modeling of Negative Capacitance of Ferroelectric Capacitors as a Non-Quasi Static Effect

Borna Obradovic, Titash Rakshit, Ryan Hatcher, Jorge Kittl, and Mark S. Rodder

Abstract—Pulse-based studies of ferroelectric capacitor systems have been used by several groups to experimentally probe the mechanisms of apparent negative capacitance. In this paper, the behavior of such systems is modeled through SPICE simulation with a delayed-response Preisach model, and the results are compared to available data. It is found that a simple ferroelectric domain delay model can explain much of the observed behavior, capturing the qualitatively different effects of bipolar and unipolar switching, as well as the voltage dependence of said switching. The observed behavior and its modeling suggests that the observed negative capacitance is in fact associated with ferroelectric switching, and its presence is highly sensitive to the switching frequency and other details of the ferroelectric system.

Index Terms—Ferroelectric, FeCap, Negative Capacitance

I. INTRODUCTION

NEGATIVE capacitance has been postulated theoretically [1] and extensively studied experimentally ([2], [3], [4]). The theoretical basis for Negative Capacitance (NC) is an assumed Energy-Charge (U-Q) relationship with a region of negative curvature (U-Q ansatz) [1]. As a consequence of the negative curvature, a switching path with negative capacitance (Fig. 1b) becomes available. This is in contrast to the standard Preisach model of a ferroelectric capacitor (Fig. 1a). However, this path is unstable and not directly observable in stand-alone FeCaps. Arguments have been made [1] that this unstable path can be stabilized by connecting the FeCap in series with a standard (positive U-Q curvature) capacitor which satisfies specific matching criteria [5], thereby making the negative capacitance branch traversable. As a consequence, using such a capacitor arrangement in the gate stack of a FET would result in increased stack capacitance and sub-60 mV/dec subthreshold slope ([1], [2]). However, precisely how the stabilized state is established at the microscopic level is unclear and challenging to explain. In the face of this difficulty, the goal of this paper is to investigate whether some of the key experimental findings can in fact be reproduced without the U-Q ansatz, consequently doing away with the need for a microscopic model of the stabilized state. The alternative conceptual model proposed herein is simply a Preisach Ferroelectric ([6], [7]) in which domain switching takes place with a delay. The existence of a switching delay of ferroelectric domains is itself well known and characterized, with little ambiguity with regards to the microscopic model ([10], [11], [12]).

While experimental studies range from basic FeCap measurements to full CMOS Ring Oscillator circuits [8], a particularly data-rich set of experiments have been performed by studying the transient response of FeCap stacks to pulse waveforms ([2], [4]). The basic experimental setup for such measurements is illustrated schematically in Fig. 2a. A stack of dielectrics is used to form the overall capacitor, which is then pulsed using a square-wave voltage waveform of varying amplitude and frequency. The voltage across the overall stack is observed as a function of time.

Fig. 1. The quasi-static Q-V curves for FeCaps are shown, based on the Preisach model (sub-plot a), and the stabilized Negative Capacitance model (sub-plot b). Saturation loops are shown. In the Preisach model, traversal of the saturation loop is always in the indicated direction; reversing the traversal direction prior to full saturation creates minor loops. Quasi-static capacitance is positive along the solid portion of the path.

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The qualitative behavior of the measurements (valid for all groups cited in references) is illustrated in Fig. 2b. As noted in all the studies which perform experiments of this type, the observed voltage waveform is quite anomalous from the standpoint of a “positive capacitance” RC behavior. Specifically, instead of a monotonic response, the voltage initially spikes,
followed by a dip with a subsequent gradual rise (or fall) to VDD (or -VDD) (Fig. 2b). This “spike” behavior has been characterized as “inductive-like” [2], and NC has been used to explain it. In this paper, the anomalous behavior is investigated using a delayed Preisach model instead.

Experiments of this sort have been performed by several groups, but the recent measurements of [4] are particularly helpful due to their more comprehensive parametric sweeps. Specifically, the measurements in [4] are performed for both bipolar and unipolar switching, across a range of pulse voltages. The data from [4] are therefore used as the primary source of for model calibration and evaluation.

II. MODEL DESCRIPTION

The overall conceptual model for the FeCap consists of two components: a delayed ferroelectric polarization capacitance, and a quasistatic non-ferroelectric capacitance (as shown in Fig. 3). The ferroelectric response is delayed due to the intrinsic switching dynamics of the Fe domains, while the non-ferroelectric component is governed by fast electronic polarization. The delayed ferroelectric response itself is modeled as a quasistatic Preisach FeCap combined with an explicit delay. The approach is somewhat different than that of recent work using a delayed Preisach model instead. Experiments of this sort have been performed by several groups, but the recent measurements of [4] are particularly helpful due to their more comprehensive parametric sweeps. Specifically, the measurements in [4] are performed for both bipolar and unipolar switching, across a range of pulse voltages. The data from [4] are therefore used as the primary source of for model calibration and evaluation.

The quasi-static ferroelectric polarization is described next. The “raw” response function is given by:

$$F^\pm(V_{int}) = \theta^\pm \cdot \tanh \left( \frac{V_{int} \mp V_c^\pm}{V_{sc}^\pm} \right)$$  \hspace{1cm} (1)

where $V_{int}$ is the voltage representing the internal state of the FeCap (related to the applied voltage, as described next), and $V_c^\pm$ and $V_{sc}^\pm$ are model parameters describing the coercive voltages and the voltage scales, respectively. Likewise, $\theta^\pm$ is a model parameter which sets the polarization strength in each state. Each quantity in Eqn. (1) has a “plus” and “minus” label, depending on whether the capacitor last experienced an increase or decrease in applied voltage (respectively). This is referred to as the “state” of the FeCap. The actual ferroelectric polarization $P_{FE}$ is computed using Eqn. (2)

$$P_{FE}(V_{int}) = \left( F^\pm(V_{int}) - F_j^\pm \right) \cdot \left[ \frac{P_j - P_i}{F_j^\pm - F_i^\pm} \right] + P_j$$  \hspace{1cm} (2)

where the indices $i, j$ denote the currently active turning points, with $V_j > V_i$. Likewise, the quantities $F_j^\pm$, $F_i^\pm$, $P_j$, and $P_i$ are evaluated at the current active pair of turning points. Eqn. (2) simply provides scaling and shifting of the raw response of Eqn. (1) to ensure that the polarization curve passes through the active pair of turning points (this is necessary to provide reasonable minor-loop behavior). As is standard for turning-point models, turning points are created and destroyed dynamically as the internal voltage of the FeCap switches. The ferroelectric response is thus modeled as a quasi-static function of the “internal” voltage of the FeCap (described by $V_{int}$). The overall behavior of the FeCap is therefore dependent on the dynamics of $V_{int}$. The quasistatic parameters of the FeCap model are calibrated using the data of [4], as shown in presented in [12]. The implementation of the model is not explicitly time-dependent, so it is applicable under arbitrary biasing conditions. Furthermore, the hysteretic nature of the model enables the exploration of history-dependent effects, such as the transition from bipolar to unipolar switching.
where the natural frequency $\omega_0$ and the damping ratio $\gamma$ are calibration parameters of the model. The “memory” property of the FeCap is handled by the model though the turning point history and the active state. Both are changed in a discrete manner, when the temporal derivative of $V_{\text{int}}$ changes sign. This ensures that the state itself is not experiencing the second-order dynamics described in Eqn. 3, the dynamics merely provide a delay for an abrupt switching of the state. Finally, the total charge of the capacitor is computed as:

$$Q_{\text{tot}}(V_{\text{int}}, V_{\text{app}}) = \left( P(V_{\text{int}}) + C_{\text{lin}}V_{\text{app}} \right) \cdot A$$  \hspace{1cm} (4)

where $C_{\text{lin}}$ is the non-ferroelectric capacitance, and $A$ is the total capacitor area. The non-ferroelectric response is modeled as being driven by the instantaneous applied voltage $V_{\text{app}}$, since the non-ferroelectric response is assumed to be much faster than any modulation of the applied voltage. For the purpose of this work, the complete model is implemented in Verilog-A and used within Synopsys HSPICE.

III. RESULTS AND DISCUSSION

The FeCap model described in Sec. II is next applied to the SPICE simulation of the experimental setup. The cases of bipolar and unipolar switching are considered separately. The parameters which govern model dynamics ($\omega_0$, $\gamma$) are calibrated for the best match to the overall transient data set. The obtained values (as shown in Sec. III-A) are $\omega_0 = 12 \cdot 10^6$ rad/sec, $\gamma = 3$. The corner frequency of $2 \text{ MHz}$ is consistent with values reported in the literature for HfZrO and HfO systems ([3], [12]). Strong damping is needed to prevent unphysical “ringing”. The full set of model parameters is summarized in Table I. The initial fitting is performed against the P-V data (Fig. 4). Parameters which govern switching dynamics ($\gamma$, $\omega_0$) are obtained purely from pulse data.

| Parameter | Units | Fit to P-V Hysteresis | Fit to Transient Pulse |
|-----------|-------|------------------------|------------------------|
| $\theta^+$ | $\mu\text{C/cm}^2$ | 14 | 15 |
| $\theta^-$ | $\mu\text{C/cm}^2$ | -10 | -10 |
| $V_c^+$ | V | 3.3 | 3.3 |
| $V_c^-$ | V | 1.2 | 2 |
| $V_{sc}^+$ | V | 0.75 | 0.75 |
| $V_{sc}^-$ | V | 0.9 | 0.9 |
| $C_{\text{lin}}$ | fF/\mu m$^2$ | 17.5 | 17.5 |
| $\gamma$ | rad/sec | 3 | 12 - $10^6$ |

For best agreement to pulse data however, some modification of the parameters obtained from P-V data is required. Most of the parameters show good consistency between the “DC” fitting of the P-V hysteresis and transient data (Table I). The only notable discrepancy is that of $V_c^-$. A possible explanation for this discrepancy is the weakness of the Preisach model in “data-free” prediction of minor loop behavior. Since the calibration was actually done on a minor loop, the saturation loop may be in error. Experience with fitting the model

![Image of graph showing P-V characteristics](image-url)

Fig. 4. The measured and simulated P-V characteristics of the HfZrO FeCap are compared. The data (shown as red diamonds) is sampled from [4]. The data does not appear to be on the saturation loop. Saturation loop model parameters are estimated so that the minor loop simulation using the Preisach data does not appear to be on the saturation loop. Saturation loop model is shown in Fig. 5.

![Image of graph showing simulated capacitance characteristics](image-url)

Fig. 5. The simulated quasistatic capacitance characteristics of the HfZrO FeCap are illustrated, based on the calibration of Fig. 4. Both the linear and Ferroelectric polarizations are included. The quasistatic capacitance is always positive in the model.

In this work, $V_{\text{int}}$ is governed by a second-order delay of the applied voltage across the FeCap. This is simply an empirical dynamical system, establishing the relationship between the “internal” and applied voltages across the FeCap. A 2nd order system is chosen to provide a more explicit delay, as opposed to 1st order “damping”. However, this should not be interpreted as arising from microscopic physical considerations; a detailed, physically-based voltage-dependent delay model is yet to be developed. The differential equation relating the “internal” voltage $V_{\text{int}}$ and the applied voltage $V_{\text{app}}$ is given as:

$$\dot{V}_{\text{int}} + 2\gamma\omega_0 V_{\text{int}} + \omega_0^2 V_{\text{int}} = \omega_0^2 V_{\text{app}}$$  \hspace{1cm} (3)
suggests that the real data shows a more skewed P-V curve with stronger \( \theta^+ \) polarization than is currently being modeled, requiring the use of a larger \( V_{c^-} \) for best fit to the pulse data. Further measurements and modeling will be needed to resolve this discrepancy.

A. Bipolar Switching

For bipolar switching, the square waveform ranges from \(-VDD\) to \(+VDD\), exercising both the positive and negative domain switching thresholds. The sampled data and simulation results for \( VDD=5V \) are shown in Fig. 6. As discussed in Sec. I the measured data exhibits an initial voltage spike, followed by a more gradual rise to the peak pulse voltage. As can be seen in Fig. 6, SPICE simulation indicates a very similar behavior. Arguing from the standpoint of a delayed ferroelectric response, the "spike" behavior can be understood in the following sequence (numbered phases illustrated in Fig. 7).

1) Initial Rise. The input waveform has a rise time that is short on the timescale of ferroelectric switching (for the particular material in question). The initial response is therefore due to the non-ferroelectric polarization component, which is quasistatic on the timescale of the input risetime.

2) Initial Ferroelectric Response. A few \( \mu s \) after the initial pulse, the ferroelectric domains begin to switch. This is the expected timescale for the ferroelectric response of HfZrO materials [12]. As the domains begin to switch, the capacitance of the Fe layer increases dramatically, increasing the charging current and resulting in a increased voltage drop across the access resistor. As a consequence, the voltage across the capacitor stack drops.

3) Final Ferroelectric Response. After the delayed rapid increase in ferroelectric capacitance, the ferroelectric capacitance gradually falls (the expected behavior, based on the P-V curve of Fig. 4). The stack voltage continues to rise (but on a slower timescale), eventually reaching VDD.

The qualitative behavior of the "spike" is captured well by the delay model. The final phase of the pulse response (phase 3) is captured only approximately; the empirical delay model indicates a "standard" exponential-like RC response, whereas the data show a more gradual (almost linear) rise. This is not surprising, from the standpoint of ferroelectric delay. In the final stages of switching, only domains with a high switching threshold remain unswitched. These domains also have the slowest response. The empirical delay model does not treat the response of the various domains on an individual basis; instead, the switching dynamics are lumped into a single, unified response. This simplification makes it difficult to precisely capture the switching waveform. The basic separation of the response into the non-ferro initial response followed by the delayed ferro response is nevertheless clear.

The data (and simulation) also reveal an asymmetry in the switching response in the positive and negative direction. Whereas the positive "spike" occurs with a stack voltage of approximately 4V, the negative one occurs much sooner, with a stack voltage of about -2V. This asymmetry in transient response is a consequence of the asymmetry of the coercive voltages of the FeCap (which are approximately -1.5V and 3V, respectively). Since the peak of the "spike" takes place shortly after the onset of ferroelectric switching, it is to be expected that the negative spike should occur much sooner than the positive one.

Additional insight into the switching behavior is gained by examining the VDD behavior of the switching. The same square-pulse waveform is applied, but with varying amplitudes. The data and simulation results are compared in Fig. 8 and the VF-Q switching characteristic is shown in Fig.
Fig. 8. The measured [4] and simulated transient responses for the ferroelectric capacitor stack to bipolar square-pulses of various amplitudes are shown. The "anomalous" spikes are diminishing in magnitude with reducing input pulse amplitude (in both data and simulation). At a pulse voltage of 2V, the spikes are absent. The inset shows the spike magnitudes ($\Delta V$) as a function of the applied voltage pulses, for both positive and negative pulses. As in the main plot, the diamonds are from measured data [4], the lines are from simulation.

It is apparent that the "spike" effect is diminishing with decreasing pulse amplitude. While quite pronounced at 5V, it is completely gone at 2V. This diminishing trend is reproduced in simulation. Arguing using the ferroelectric delay model, the reason is simply that at low pulse voltages the voltage drop across the FeCap is too small to trigger ferroelectric domains. From Fig. 4, it is evident that very little ferroelectric switching happens in the voltage range of [-1.5V, 1.5V], which is the approximate voltage range across the FeCap during the 2V pulse. In the Verilog-A model, the delay is associated only with ferroelectric switching, so absent switching, there is negligible delay (and hence no spike). An additional expected effect (though not modeled) is the increased switching time for domains at low voltages [12]. This is currently being further investigated. At the $\mu$s timescale of the present data and simulations, the simple absence of domains in the small voltage range appears to be enough to explain the data.

B. Unipolar Switching

For unipolar switching, the square input waveform is modified to range from 0 to VDD. The results are qualitatively different than for the bipolar case. As can be seen in Fig. 10, the "spike" is observed only on the first unipolar pulse of the waveform. Subsequent pulses (in either the positive or negative direction) exhibit no spike (even at the highest VDD of 5V). This behavior is reproduced in simulation, and is in fact largely independent of the details of the delay model. The reason for the behavior of the stack voltage is apparent from Fig. 11. While the polarization undergoes large changes during bipolar switching, the only large polarization change during unipolar switching is during the transition from bipolar to unipolar mode. After this initial pulse, the FeCap operates on a tight minor loop, and the polarization changes are small and mostly due to non-Ferro polarization. As previously discussed, non-Ferro polarization is essentially quasistatic, and the ferroelectric $\Delta P$ is very small. Together, the two effects cannot generate the transient spike. Modeling this behavior does not require a detailed delay model, just one that delays only ferroelectric switching. Additionally, the transition to a tight minor loop must be captured, but this is reasonably straightforward with the Preisach model.

Fig. 9. The simulated hysteresis for bipolar switching for several VDDs is shown. Regions of apparent negative capacitance ($dQ/dV < 0$) are shown shaded. At 5V and 4V, there are clear NC regions (though transient in nature), while the 2V hysteresis loop is too tight to produce NC.

Fig. 10. The measured [4] and simulated transient response for the ferroelectric capacitor stack to unipolar square-wave pulses is shown. The stack is initialized by a sequence of bipolar pulses (shaded blue region), followed by a sequence of unipolar pulses. On the first unipolar pulse, the "anomalous" spike is observed. On subsequent pulses, the spike is absent.
Fig. 11. The P-V trajectory of the stack during bipolar and unipolar pulsing is shown. The initial pulses are bipolar (blue solid line), establishing a wide loop with a large $\Delta P$. Subsequent pulses are unipolar (red dashed line), resulting in a tight minor loop with minimal ferroelectric $\Delta P$ (the initial portion of the unipolar curve matches the bipolar since it switches from -5V to +5V). No apparent NC is exhibited on the minor loop.

IV. IMPACT ON SUBTHRESHOLD SLOPE

The technological impetus for investigating the NC-effect is the potential improvement in FET subthreshold slope (SS). As argued in [1], a negative capacitance gate layer can result in a sub-60 mV/dec SS, by introducing “amplification” into the surface potential ($\psi$). Specifically, if the applied gate bias is $V_g$, the long channel slope of the $I_d-V_g$ curve is proportional to $d\psi/dV_g$. With ordinary capacitors, this derivative is never greater than unity (equal to unity only for long-channel, fully-depleted devices). As shown in [1], NC effects can push the derivative beyond unity, thereby reducing the SS below the usual theoretical limit.

As can be seen in Figs. 12 and 13, driving the capacitor stack with a frequency similar to the ferroelectric switching frequency $\omega_0$ results in amplification over portions of the rising and falling input voltage. The actual magnitudes of the slope $d\psi/dV_g$ are shown in Fig. 13, $d\psi/dV_g$ of approximately 1.5 is observed, resulting in a predicted SS of 40 mV/dec. It should be noted that the improved SS is manifested only over small portions of the switching characteristic. Most of the simulated points show un-amplified values of $d\psi/dV_g$. The latter are generally below unity because the underlying semiconductor is not fully depleted (swinging from accumulation to inversion). Furthermore, before the ferroelectric domains start to switch, the gate capacitance is small (only the non-Ferro component is present), resulting in unfavorable voltage division between the (temporarily) small gate capacitance and the semiconductor (particularly true in regions where the FET channel is in inversion). Consequently, $\psi$ is considerably smaller than $V_g$ in this region, and so is $d\psi/dV_g$.

The simulation of $d\psi/dV_g$ amplification was performed at VDD=5V; as seen in Fig. 8, voltages much below 5V do not result in the apparent NC effect for input pulse frequencies on the order of a $\mu$s. It was argued that this is due to a lack of domain switching at low voltages. However, it was shown in [4] (and elsewhere) that low-voltage $d\psi/dV_g$ amplification is indeed possible, but at much longer timescales (approximately $10^4$ to $10^5$ times longer than simulated here). This may simply be a consequence of the much longer switching times of ferroelectric domains at low voltage ([10], [11], [12]). The voltage dependence of the switching frequency characteristics...
is not modeled in the present work, and is the subject of current investigation.

V. CONCLUSION AND FUTURE DIRECTION

A ferroelectric switching delay model is proposed to explain the “anomalous” transient response of ferroelectric capacitor stacks. While the “anomalous” spike observed in the transient response has been attributed to the NC effect, it is argued herein that this is not in fact necessary. By constructing an FeCap model which consists of a delayed and quasistatic component (the ferroelectric and electronic polarization components, respectively), it is possible to reproduce the measured data in simulation with reasonable fidelity. This suggests that the observed NC effect in the data may simply be a dynamic (non-quasi static) effect of the natural ferroelectric delay. Furthermore, there is clear evidence that the NC “spike” is tied directly to ferroelectric switching:

- The onset of the end of the “spike” is correlated to the ferroelectric coercive voltage (as evidenced in Sec. III-A).
- The magnitude of the “spike” (or its presence) is correlated to the extent to which ferroelectric domains switch (as evidenced in Sec. III-A Fig. 3).
- The presence of the “spike” is correlated to conditions in which large changes in ferroelectric polarization are observed, i.e. bipolar and not unipolar switching (as evidenced in Sec. III-B). Furthermore, the presence or absence of the “spike” correlates with the polarization history.

While the ferroelectric delay model does successfully reproduce the transient pulse data, it must be recognized that there are numerous other phenomena in the literature associated with NC. Additional experimental and modeling work is required to fully explain all observations. Of specific interest is the apparent voltage amplification and the associated sub-60 mV/dec SS behavior of FeFETs with capacitor stacks such as those explored in this paper. While the delay model predicts amplification and sub-60 mV/dec behavior for the stack in question, it suggests that it cannot occur on the timescale of the experimental data and technologically desired low voltages (VDD ≈ 1V). This is obvious from the VDD behavior of the pulse data in Sec. III-A. However, amplification may well occur even at low VDD on a much slower timescale, given the much slower ferroelectric switching at low voltages. It is therefore desirable to further investigate experimentally the long-timescale, low-voltage regime. The ferroelectric delay model will likewise need to improved to capture the effects of slow switching at low voltage.

From a scaled technology perspective, an individual device and inverter switches on a few-ps timescale. This limits the usefulness of sub-60 mV/dec transistors as a general purpose scaled device, if indeed these devices switch at a much slower timescale. FeFETs with moderately high RO frequencies have already been reported [8], but the reduced RO frequency relative to standard dielectrics suggests than only non-Ferro switching is taking place (consistent with a decrease in power, in spite of the obviously high DC gate capacitance). In order to properly explore the frequency dependence, a pulse train similar to [12] needs to be applied to the gate terminal of the FeFET transistor with varying voltage magnitude and pulse duration both in forward and reverse direction. This set of measurements is the key to decipher the underlying mechanism, whether it is truly NQS or not, and uncover the technology implications for FeFETs. Barring the aforementioned measurements, a technological evaluation of FeFETs will remain incomplete. Evolution of the sub-60 behavior as a function of temperature may shed light on the underlying physics as well. Another point worth noting is that the range of Vg for which the SS is less than 60 mV/dec is a critical parameter to track for possible technology implications. If indeed the Vg range is very small for a SS reduction to say 40 mV/dec, significantly lower leakage or lower Vt may not be realized for the entire voltage range of technological interest, limiting applicability of these devices even for a slower applications.

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