Testing and Evaluation of a 20-Gsps High-Resolution Waveform Digitizer Based on TIADC Technique

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Abstract. Time-Interleaved Analog-to-Digital Conversion (TIADC) is one of the significant technique in high speed waveform digitization systems. In our latest work, a 20-Gsps 12-bit TIADC system is designed and a series of tests are conducted on the proposed system and a broadband mismatch error correction is implemented. The test methods and results are specifically presented in this paper. The test results show that the -3dB bandwidth of the proposed system is 6 GHz and the ENOB performance is about 8.7 bits at 647 MHz and 7.6 bits at 6 GHz which is significantly enhanced by the mismatch error correction process.

1. Introduction

Time-Interleaved Analog-to-Digital Conversion (TIADC) is a significant technique in high speed waveform digitization systems [1]-[4]. Sampling rate is one of the most important parameters in a waveform digitization system. The TIADC technique can greatly improve the system sampling rate by employing multiple Analog-to-Digital Converters (ADCs). It can be supposed that the number of the paralleled ADC channels in a system is denoted as $M$ while the sampling rate and the sampling period of each ADC channel are denoted as $F_s$ and $T_s$, separately. In this case, if the sampling time of each ADC channel is delayed by $T_s/M$ in sequence, the equivalent sampling period of the whole system comes to be $T_s/M$ and the sampling rate comes to be $M \times F_s$, where the sampling rate increases to $M$ times.

Another important parameter in the waveform digitization system is the Effective Number of Bits (ENOB). In a TIADC system, due to the existence of the mismatch error between different ADC channels, the ENOB performance is supposed be deteriorated comparing with that of a single ADC, inevitably. Aimed at this issue, many methods for mismatch error correction have been developed [5],[6]. In our previous work, a broadband correction method based on the perfect reconstruction algorithm was proposed [5], and this method especially conduces to the mismatch error correction when the input signal has a wide frequency band.

In our latest work, a 20-Gsps 12-bit TIADC system was carefully designed and tested. In this paper, the test methods and results are presented explicitly. The tests verified that a 20-Gsps sampling is successfully realized by the system. The performance of ENOB and bandwidth were tested and efforts were made on the mismatch error correction.

The rest of the paper is organized as follows: In section 2, there is a brief introduction on the structure of the proposed system. In section 3, the test methods on the proposed system are introduced and the
test results of the key parameters are presented in detail. In section 4, the conclusions are given for this paper.

2. 20-Gsps 12-Bit TIADC System

2.1. A brief introduction on the system structure

The structure of the proposed 20-Gsps 12-bit TIADC is shown in Figure 1. In general, two 10-Gsps 12-bit ADCs are employed for a time-interleaved sampling. There are four sub-channels in each separated ADC. A high-precision 5 GHz sampling clock is required for each ADC for a double-edge sampling and the clock skew between the two sampling clocks is set as 90 degrees. In this case, there are totally 4 sampling clock edges with a time interval of 50 ps so that an equivalent sampling rate of 20 Gsps is achieved. A high bandwidth analog signal transmission circuit, which composed of a power splitter and two transformers, is designed for the input signal splitting and transforming into two differential signals. A clock generating circuit is proposed for the generation of low-jitter ADC sampling clocks on 5 GHz, together with the reference clocks for data alignment. The JESD204B interface is set up for high-speed serial data transformation to a Field Programmable Gate Array (FPGA). The sampling data are deserialize in the FPGA and hardware logic are programmed for data handling and buffering. In the end, the data are transferred to PC through an SFP interface.

2.2. Mismatch error correction

In a TIADC system, there are three kinds of typical mismatch errors, that is, gain error, skew error and offset error. The gain error reflects the amplitude inconsistency on the signals which being sampled by different ADC channels. The gain error of the \( m \)th channel can be expressed as \( A_m/A_{ref} \) where \( A_m \) denotes the signal amplitude of the \( m \)th channel and \( A_{ref} \) denotes that of the reference ADC channel. The skew error delivers the sampling time error of each ADC channel. In an M-channel interleaved TIADC system where the sampling period of a single ADC channel is \( T_s \), the ideal sampling time of the \( m \)th channel is supposed to be \( T_s + ((m-1)/M)T_s \). The difference between the actual sampling time and the ideal sampling time can be defined as the skew error of the \( m \)th channel. The offset error reflects the DC offset of the sampling result of each ADC channel. Among which, the values of gain error and skew error usually correlates with frequency while the offset error is usually supposed to be a constant value without correlation with frequency.

In our previous work, a real-time broadband mismatch error correction method based on the perfect reconstruction algorithm was developed [5]. This method is based on the Finite Impulse Response (FIR) filters to correct the sampling data and it can be implemented on either software or hardware. In the proposed system, as there are four sub-channels in a single ADC, the system can be regarded as an eight-channel interleaved system. In this case, an eight-channel correction process can be implemented in our test.
3. Tests and Results

3.1. System bandwidth test

A series of tests were conducted to evaluate the performance of the proposed system. A test platform was constructed and the system being tested is shown in Figure 2. A high performance RF signal generator, which covers an output frequency range from 800 kHz to 6 GHz, was employed to generate sinusoidal waves as the input signal. The signal was connected to the proposed system through a one-meter coaxial test cable with low insertion loss. The input signal was sampled by the system and the sampling data from both ADCs were readout by a PC.

Before the test on the proposed system, a calibration test on the coaxial test cable is conducted beforehand to evaluate its insertion loss. A network analyzer was employed for the S-parameter testing of the cable. The S21 parameter of the test cable was calibrated at first and the screen capture of test result from the network analyzer is shown in Figure 3. It can be verified that the test cable is of high bandwidth where the insertion loss is about 1 dB at 18 GHz.

Later on, the bandwidth performance of the system was tested. The output power of the signal generator was set as a fixed value and it was ensured that the sampling waveform at 50 MHz sine signal input was -1 dBFS on amplitude. The output frequency of the signal generator was adjusted from 50 MHz to 6 GHz and the sampling waveforms at a series of frequencies were acquired. A sine-wave fitting was conducted at each frequency point being tested and the amplitude of the sampling waveform was obtained. The amplitude-frequency response (AFR) can be calculated by:

\[ \text{Amp}(f) = 20 \log \left( \frac{A_f}{A_{nor}} \right), \]  

where \( \text{Amp}(f) \) denotes the AFR at the frequency of \( f \); \( A_f \) denotes the waveform amplitude at the frequency of \( f \) and \( A_{nor} \) denotes the waveform amplitude at 50 MHz, which was set as the standard of normalization.
for the bandwidth performance test. The test result is shown in Figure 4. The dashed line is the AFR of the entire test platform where the test cable was included. The AFR excluding the influence of the test cable can be calculated by subtracting the insertion loss of the test cable from the result of the whole platform and it is shown as the solid line. According to the result, the -3dB bandwidth of the proposed 20 Gsps TIADC system was up to 6 GHz.

![Figure 4. AFR test result of the proposed 20-Gsps TIADC system](image)

### 3.2. Mismatch error test

According to the perfect reconstruction algorithm based broadband mismatch error correction, the block diagram of the correction process can be shown as Figure 5. The mismatch error correction can be divided into two separated processes, the calibration process and the correction process. During the calibration process, a frequency sweep on sine waveform was made at first. A series of frequencies with a number of K was chosen as the calibration frequencies. These frequency points covered the range from 50 MHz to 6 GHz and the signal was sampled at each of the frequency points. The sine signal of the $k$th calibrated frequency is denoted as $x_{cal_k}(t)$ and the sampling array is denoted as $X_{cal_k}[n]$. Each sampling array was split into eight channels, according to the ADC sub-channels and a four-parameter sine fitting was set up for each sub-channel. The fitting function of the $m$th sub-channel at the $k$th calibrated frequency is $G(f_k, \Delta t_{f_k}^{m}, G(f_k, \Delta t_{f_k}^{m-1})$, and so on. The mismatch error can be calculated as $\Delta f_{(k,m)}$ and $\Delta t_{(k,m)}$.
frequency point can be expressed as \( x_{fit,mk}(t) = A_{mk} \sin(\omega_{mk}(t - t_{mk})) + o_{mk} \). In this case, the gain error and the skew error of the \( m \)th sub-channel can be calculated. Channel 0 was set as the reference channel and the gain error can be expressed as \( G_{m}(f_k) = A_{mk}/A_{0k} \). The skew error can be expressed as \( \Delta t_{m}(f_k) = t_{mk} - t_{0k} - (m - 1)T_s \), where \( T_s \) is the system sampling period of 50 ps. The mismatch error calibration result is shown in Figure 6 and Figure 7. Moreover, the offset error \( o_m \) is regarded as a constant value for each channel and it can be obtained by calculating the average value of the noise waveform.

Then, a certain matrix function which correlated with the mismatch errors at every calibrated frequencies was calculated [5]. A numerical expression of the FIR filters on frequency domain was acquired from the matrix function for each sub-channel, where it can be denoted as \( F_m(\omega) \). An Inverse Fast Fourier Transform (IFFT) process was deployed on each filter expression to transform it into the expression on time domain which was denoted as \( F_m[n] \). Finally, a truncation was given for each \( F_m[n] \) and the coefficients for an N-order FIR filter were given out for each channel.

In the correction process, the sampling data was also split into eight channels. The data of each channel was corrected by an N-order FIR using the coefficients obtained from the calibrating process. The test result of the mismatch error correction will be presented together with the dynamic performance test results in the next sub-section.

3.3. Dynamic performance test
The evaluation on the dynamic performance of the proposed system was performed according to the IEEE Std. 1241-2010 [7]. The sampling results under a series of input frequencies, which covered the range from 50 MHz to 6 GHz, were tested. At each frequency, the output power of the signal generator was adjusted to an appropriate value to maintain the amplitude of the sampling data is -1 dBFS. The output data were analyzed with the Fast Fourier Transformation (FFT) where 65536 data points were calculated for each FFT section and the averaged spectrum was acquired by 16 sections. Figure 8 shows the frequency spectrum of one of the ADC sub-channels at 647 MHz input; Figure 9 shows the frequency
spectrum of a separated ADC where there are four sub-channels interleaved; Figure 10 shows the frequency spectrum of the ADC1 and ADC2 interleaved sampling result where there are eight sub-channels interleaved in total. It can be seen that there are mismatch error peaks on the multi-channel interleaved frequency spectrums and the number of the mismatch error peak becomes more when there are more channels interleaved.

Next, the mismatch error correction on the ADC1 and ADC2 interleaved sampling was implemented, where the FIR coefficients was obtained by the calibration process. Figure 11 shows the frequency spectrum after an 80-order correction at 647 MHz input. Comparing with Figure 10, it is obvious that the mismatch error peaks had been eliminated in a large extent.

With the frequency spectrum, the dynamic performance of Signal-to-Noise Ratio (SNR), Spurious-Free Dynamic Range (SFDR), Signal-to-Noise and Distortion Ratio (SINAD) and Effective Number of Bits (ENOB) can be evaluated. Since there were 65536 sampling points being calculated as an FFT section, the frequency spectrum, which was denoted as \( X[f] \), was a discrete function where \( f \) had a number of value of 32769 in the first Nyquist zone from DC to \( f_s/2 \). A certain value of \( f \), which was denoted as \( f_{signal} \), corresponded with the input signal frequency. The input signal power can be calculated by:

\[
P_{signal} = \sum_{f_{signal}-\text{win}}^{f_{signal}+\text{win}} X[f],
\]

where \( \text{win} \) denotes the window of integration and there were 20 frequency points integrated in this test. Similarly, the power of the second to the tenth harmonic distortion can be calculated by:

\[
P_{\text{harmonic}_n} = \sum_{f_{\text{harmonic}_n}-\text{win}}^{f_{\text{harmonic}_n}+\text{win}} X[f],
\]

where \( f_{\text{harmonic}_n} \) denotes the frequency points of \( n \)th harmonic distortion on the frequency spectrum. The total power of the harmonic distortion, \( P_{\text{harmonics}} \), integrated the power of the second to the tenth harmonic distortion.
distortion. The rest of the power values on frequency spectrum were integrated as the noise power which was denoted as $P_{\text{noise}}$, where the mismatch error peaks were also included in it. In this case, the SNR, SINAD and ENOB can be calculated by:

$$SNR = 10 \log \left( \frac{P_{\text{signal}}}{P_{\text{noise}}} \right),$$

(4)

and

$$SINAD = 10 \log \left( \frac{P_{\text{signal}}}{(P_{\text{noise}} + P_{\text{harmonics}})} \right) \approx 6.02 \times ENOB + 1.761.$$  (5)

Meanwhile, the SFDR was calculated by:

$$SFDR = 10 \log \left( \frac{P_{\text{signal}}}{P_{\text{spurs,h}}} \right),$$

(6)

where $P_{\text{spurs,h}}$ denotes the power of the highest spurs on the frequency spectrum. The test result of the SNR, SFDR, SINAD and ENOB are shown in Figure 12 to Figure 15. It can be verified that the dynamic performance of the proposed system was significant enhanced by the correction. When the number of FIR order was 150, the ENOB performance achieved 8.7 bits at 647 MHz, 8.1 bits at 3 GHz, and 7.6 bits at 6 GHz, which coincided well with the ENOB performance of a single ADC sub-channel.
3.4. Transient waveform test

Finally, the test results on transient waveform is given. The transient waveforms of sinusoidal signal input had already been obtained by the test above and the waveforms at 647 MHz and 2247 MHz input are shown in Figure 16 and Figure 17 as examples.

The pulse signal is common in physics experiments. A typical pulse waveform with the rising edge of 1 ns and falling edge of 2 ns was generated by an arbitrary signal generator where the screen capture of the waveform on an oscilloscope is shown in Figure 18. We sampled the signal by the proposed 20-Gsps TIADC system and the sampled waveform is shown in Figure 19. It can be verified that the input pulse signal can be depicted well with a sampling time interval of 50 ps.
4. Conclusion
In this paper, a series of tests are conducted on the proposed TIADC system to evaluate its performance. A high sampling rate of 20-Gsps is successfully achieved. The bandwidth performance of the proposed system is up to 6 GHz. The mismatch error is calibrated and the dynamic performance is tested. The mismatch correction is implemented on the sampling data and the ENOB performance of 8.7 bits at 647 MHz and 7.6 bits at 6 GHz are verified.

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