Impact of Program/Erase Cycles, Total Ionizing Dose and Data Bake on Data Retention of 55nm SONOS Flash

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Abstract. In this paper, the data retention capability of 55nm SONOS Flash under the worst condition is studied by superimposing experiments of program/erase cycles, total ionizing dose (TID) and data bake. The results show that after 100k program/erase cycles and data bake, the data retention of the memory transistor is basically not affected. After 100k program/erase cycles, 200Krad(Si) TID and data bake, the data retention of the SONOS memory transistor is mainly reflected in the radiation-induced charge leakage. If the data is rewritten after TID, irradiation has basically no impact on its data retention capability.

1. Introduction
Flash is a non-volatile memory, which is widely used in consumer electronics and military aerospace fields. In the space radiation environment, electronic devices will have ionizing radiation effects such as total ionizing dose and single event effect, and their reliability will be seriously affected. Flash has two main types: floating gate and SONOS. Due to the difference in charge storage methods, SONOS Flash has stronger radiation resistance than floating gate type, and is more suitable for use in space radiation environments [1].

The reliability of Flash has two basic indicators: endurance and data retention. The endurance refers to the ability of Flash to rewrite data under the premise of meeting functional and electrical parameters. It is usually characterized by the number of program and erase cycles, and the value is usually 10k~100k. Data retention refers to the ability of Flash to retain data after a period of time. It is usually characterized by the data retention time, which is usually 10 years at 55°C.

At present, many studies have focused on the TID of SONOS Flash [2-3], but there are still gaps in the research on the superimposing impact of program/erase cycles, TID and data bake on the data retention of SONOS Flash. In this paper, we studied the data retention capability of the 55nm process SONOS Flash by superimposing three experiments.

2. Devices and Methods
2.1. Devices
The experimental device is a radiation-hardened SONOS flash test chip developed by Beijing Microelectronics Technology Institute. Its process size is 55nm and its memory capacity is 64Mb. Figure 1 shows the SONOS structure. It has programmed and erased two states. Programmed state SONOS stores electrons in the Nitride as data "0"; while erased state SONOS stores holes in the Nitride as data "1".
2.2. Experimental methods
In order to study the data retention capability of 55nm SONOS Flash under the worst condition, the order of the experiment is 100k program/erase cycles first, then 200Krad(Si) TID, and finally data bake. A total of 4 experimental groups are set up, each group contains 3 devices. Ensure all test devices function properly before the experiments.

2.2.1. Program/erase cycles experiment
According to the Flash endurance target, the experimental samples were subjected to 100k program/erase cycles, and each program data was 00h. After completion, write data 00h into the sample for subsequent operations.

2.2.2. TID experiment
The TID experiment was conducted with $^{60}$Co $\gamma$-ray source, and the radiation dose rate was 50 rad(Si)/s. The total radiation dose was 200Krad(Si). The data stored in the samples before irradiation was 00h. During the irradiation process, the chips were in a static bias condition, which is the worst bias condition of SONOS Flash under total dose irradiation. Test the chips within 1 hour after the irradiation to ensure that the annealing time at room temperature is very short and will not have a significant impact on the test result of the chips.

2.2.3. Data bake experiment
The data bake experiment was carried out under the conditions of 150 °C high temperature, and the longest test was 168 h (if $E_a$ is 1.1 eV, according to the Arrhenius formula, it can be equivalent to keeping the data at 55 °C for 120 years). In the data bake experiment, some samples were directly subjected to the high-temperature baking without rewritten data after the TID experiment; the other part of the samples was erased first, then be rewritten 00h data. At last the data bake experiment was performed.

The specific experimental conditions are shown in Table 1.

| Group | P/E Cycles | Data | TID | Rewrite | Temperature |
|-------|------------|------|-----|---------|-------------|
| A     | NA         | 00h  | NA  | NA      | 150°C       |
| B     | 100k       | 00h  | NA  | NA      | 150°C       |
| C     | 100k       | 00h  | 200Krad(Si) | NA     | 150°C       |
| D     | 100k       | 00h  | 200Krad(Si) | rewrite | 150°C     |
3. Results
The samples of group A have only undergone the data bake experiment at 150°C, and no data errors occurred during the test after baking at a high temperature for 168 hours.

Group B samples have undergone 100k program/erase cycles and 150°C data bake experiments, and no data errors occurred during the test.

After two groups of samples C and D went through 100k program/erase cycles and 200Krad(Si) TID, a small amount of data errors appeared. Then the samples in group C were not rewritten the data, and the 150°C data bake experiment was carried out directly; the samples in group D were erased and rewritten with 00h data, and then the data bake experiment was carried out. During the test, it was found that the number of data errors in group C samples increased compared with that after irradiation, while there were no data errors in group D samples.

The average data error rate of samples C and D after program/erase cycles and TID experiments are counted, and the average error rate of data bake experiment after that, the result is shown in Figure 2.

![Figure 2. After program/erase cycles, TID and data bake experiments, the average data error rate of the two groups of samples C and D.](image)

4. Discussion
4.1. Program/erase cycles experiment
Both programming and erasing of this SONOS Flash use F-N tunnelling effect. The electrons enter the silicon nitride storage layer and the substrate through the tunnel oxide layer to change the threshold voltage. After repeated programming and erasing, the tunneling stress will damage the tunnel oxide layer, and the trapped electrons accumulated in the tunnel oxide are difficult to erase. This will cause the difference between the threshold voltages of the programmed state and the erased state to be reduced, that is, the storage window is reduced. However, it can be seen from the experimental results
of the B group samples that 100k program/erase cycles did not significantly reduce the storage window. It is basically no effect on the data retention capability of the SONOS memory transistor. This shows that the SONOS memory transistor has well endurance characteristic.

The well endurance characteristic has a certain relationship with the structural characteristics of the SONOS device itself. The thinner tunnel oxide layer does not generate a large number of charge traps during repeated programming and erasing. The silicon nitride charge trapping layer is insulated, and will not cause the entire stored charge to be completely lost due to the charge leakage at a certain point in the repeated programming and erasing process [4]. In addition, well endurance properties are also related to the selected programming and erasing mechanism. The F-N tunneling mechanism is a uniform operation of the full channel charge. Compared with the hot electron injection method of the CHEI mechanism, the damage of the tunnel oxide is less.

4.2. TID experiment
After the program/erase cycles experiment, the samples of groups C and D were irradiated with a total dose of 200Krad(Si), and a small amount of data errors appeared. The reasons for the error of SONOS Flash data caused by TID are the following two points:

The first reason is that the number of electrons stored in the silicon nitride trap of SONOS is reduced, which causes the threshold voltage of the programmed SONOS to shift negatively. The main mechanism of the negative shift of the threshold voltage under TID irradiation is: γ-ray irradiation ionizes the ONO layer materials to generate electron-hole pairs, and the electrons stored in Si3N4 traps are excited to the conduction band; Si3N4 stores a large number of electrons, generating an electric field directed to the Si3N4 layer from the tunnel oxide and the blocking oxide, sweeping electrons out of the Si3N4 layer; holes are trapped to form trap charges; part of the electrons or holes recombine; part of the electrons or holes are trapped by the traps in the Si3N4.

The second reason is that the leakage current of the SONOS memory transistor increases. Because STI is used to achieve isolation between transistors, it can be considered that two parasitic transistors are connected in parallel on both sides of the SONOS memory transistor. The thickness of the gate oxide of the parasitic transistor is large, the threshold voltage is large before irradiation, and the leakage current is small; after the irradiation, the oxide generates positive trap charges due to the accumulation of holes, and the parasitic transistor threshold voltage drifts significantly negatively, forming a leakage path.

The above two reasons work together in the TID irradiation, causing the read current of the programmed state SONOS memory transistor to increase. When it exceeds the reference current, the originally stored data "0" will change to "1", and a data error will occur.

4.3. Data bake experiment
The samples of group C were directly subjected to 150°C data bake experiment without rewriting data after the program/erase cycles and TID experiments. The amount of data errors increased compared with that after irradiation. The main reason was the radiation-induced leakage charge (RILC) effect [5]. Part of the charge in the silicon nitride leaks, the threshold voltage of the programmed state decreases, and the number of data errors increases.

The samples of group D were erased and rewritten to 00h data before the data bake experiment, eliminating the effect of TID on the stored charge in SONOS. The experimental results found that after the data was rewritten, the samples of group D had no data errors after the data bake experiment. It shows that the oxide and interface trap charges introduced by the TID are few. After eliminating the effect of RILC, TID has little effect on the data retention capability of the SONOS memory transistor itself, and it is not enough to cause the loss of stored data.

5. Conclusions
In this paper, the data retention capability of 55nm SONOS Flash is studied through the superimposing experiments of program/erase cycles, TID and data bake. The results show that after 100k
program/erase cycles and data bake, the data retention of the memory transistor is basically not affected. The endurance characteristic of SONOS memory transistor is well. After 100k program/erase cycles, 200Krad(Si) TID and 150℃ data bake, the data retention of the SONOS memory transistor is mainly reflected in the RICL effect. If data is rewritten, TID has basically no effect on the data retention capability of the SONOS memory transistor itself. In the worst case of the superimposing of program/erase cycles, TID and data bake, SONOS Flash also has a strong data retention capability and is suitable for radiation-resistant non-volatile memory applications in space environments.

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