A Study of Energy and Locality Effects using Space-filling Curves

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Abstract—The cost of energy is becoming an increasingly important driver for the operating cost of HPC systems, adding yet another facet to the challenge of producing efficient code. In this paper, we investigate the energy implications of trading computation for locality using Hilbert and Morton space-filling curves with dense matrix-matrix multiplication. The advantage of these curves is that they exhibit an inherent tiling effect without requiring specific architecture tuning. By accessing the matrices in the order determined by the space-filling curves, we can trade computation for locality. The index computation overhead of the Morton curve is found to be balanced against its locality and energy efficiency, while the overhead of the Hilbert curve outweighs its improvements on our test system.

I. INTRODUCTION

Cooling systems and technology scaling challenges make power consumption an increasingly important cost factor in HPC systems [2], with estimates of approximately 50% of total annualized system cost reported already in 2009 [1]. Techniques such as clock gating and dynamic voltage and frequency scaling (DVFS) have mitigated this development architecturally, but software developments are not expected to contribute similarly [3], [4]. This suggests that with present systems the optimization for program performance is equivalent with achieving energy efficiency [4], [5], [6].

Processor and memory subsystems account for the two biggest components in a total system power budget [7], and program memory access patterns correlate both with power and energy. Specifically, higher spatial and temporal locality increase power consumption, but also improve energy efficiency [8] by reducing the energy lost waiting for memory operations and improving the execution time.

For matrix manipulation, tiled algorithms improve utilization of the memory hierarchy by increased reuse of submatrices fetched into cache memory, but their effectiveness is highly dependent on cache parameters and problem size [9].

Another way to improve spatial locality is to alter the ordering of matrix elements in memory according to a space-filling curve that implies a multi-level tiling pattern. This type of technique does not achieve the performance levels attainable by explicitly tiled, automatically tuned approaches like ATLAS [15], but is favorable in contexts where cache-oblivious behavior is desired. Examples include software deployed as identical binaries on multiple target architectures, or when the additional computational effort of automatically tuning an installation is impractical. Two well known curves that exhibit an inherently tiled access pattern are the Morton and Hilbert curves, shown for 4 × 4 matrices in Figure 1.

The advantage of reducing the dependency on architecture-specific parameters comes at the expense of increased computational cost, because calculating the memory address of an element from its matrix coordinates in these orderings requires computations which take logarithmic and linear time with respect to address length, as opposed to the constant cost of conventional row- or column-major orders. Motivated by the optimization guideline that memory operations can be orders of magnitude more expensive than computation on recent and future architectures [14], the recent addition of energy counters in mainstream architectures [13] enables us to empirically investigate the energy impact of this trade-off between general and architecturally specialized methods in an energy-efficiency context.

In this paper, we apply the Morton and Hilbert orderings to general matrix-matrix multiplication, and compare their utility to naive row-major indexing, in order to quantify their impact on computation time and energy consumption. We find that both curves improve spatial locality, but that the Hilbert ordering replaces the avoided memory accesses with an amount of computation that negates its utility on our test platform.

The rest of the paper is organized as follows: Section II discusses the procedure of constructing Morton and Hilbert curves, and relates their definitions to the complexity of computing memory addresses from coordinate pairs in both
orders, Section III describes our test platform, instrumentation methods and experimental setup, Section IV summarizes related work, and Section VI concludes with a summary of our findings, and suggestions for future investigation.

II. SPACE-FILLING CURVES

Informally, the Morton and Hilbert curves are inductively constructed from basic $2 \times 2$ squares by replication and rotation, as illustrated in Figure 2. In order to use these curves as encodings of matrices in a linear memory array, procedures for mapping the two-dimensional indices onto one-dimensional memory arrays are required. The remainder of this section outlines these procedures and the computational complexities of their algorithms.

A. Serialization of Quadrant Indices

The inductive constructions of the Morton and Hilbert curves share the feature that both are defined by a traversal order of the 4 quadrants in a square. This suggests that the indexing scheme to serialize matrix elements in a linear memory array should similarly partition the array into quarters, making the memory address of an element equivalent to a sequence of successively refined quadrant selections. Each 4-way selection is thus encoded as a pair of bits.

The serialized index of a coordinate pair $(y, x)$ with $y$ as the major coordinate can be found by a bitwise interleaving of the coordinate pair, combining the most significant bit of both coordinates to select which partition of the array to address, the next pair to select which part within it, and so on. Figure 3 illustrates the mapping for the coordinate pair $(y = 3, x = 5),$ with $y$ representing the major coordinate, and varying vertically in the figure.

Interleaving two arbitrary-length bit patterns asymptotically requires computation time linearly proportional to their length. Observing that these bit patterns represent memory addresses, we restrict our considerations to lengths that fit within address registers of a target machine, providing constant-time operations to combine pairs of binary strings. Moreover, we note that as the serialized bit pattern $s$ is as long as the sum of its constituent coordinates, this restricts coordinates to half the size of machine registers, admitting pairs of 32-bit coordinates on a 64-bit architecture. As 32-bit coordinates provide ample space for matrix sizes that outgrow the last-level caches of modern processors, we will assume that register level operations can be used to interleave them, and sacrifice some generality to the advantage of assuming that bit patterns can be dilated and combined in pseudo-logarithmic time with respect to their length. Dilation of integers has been thoroughly studied in the literature [11]. We use an algorithm due to Raman and Wise [12] which our implementations adopt as a constant sequence of 5 shifting and 5 masking operations, involving 5 constant values and 1 register.

B. Morton and Hilbert Orders

Although the serializations of Morton and Hilbert indices work according to the same recursive decomposition of a 2-dimensional area, they are differentiated by applying different traversal orders of the quadrants at each level. Table I lists their respective traversal sequences. Note that the Morton order essentially applies the same straightforward ordering as row-major order, but does so recursively, which gives a tiling effect that improves spatial locality. As this pattern essentially amounts to following the same order as conventional binary counting, interleaving the major and minor coordinates already completes the index translation for this scheme. The resulting index calculation cost is higher than row-major ordering, but remains constant for indices within register size, at the cost of introducing minor discontinuities between quadrants $(1, 2)$ and $(3, 4),$ and a larger gap between quadrants $(2, 3),$ as was already seen in Fig. 1.

The Hilbert order eliminates these gaps by following a traversal order that also steps between neighboring elements across quadrant boundaries. This results in further improvement of spatial locality, but it comes at an additional computational cost, as interleaved coordinates must be further rearranged by additional computation, because the traversal orders for quadrants rotate as a function of their position and depth in the recursive decomposition.

Lam and Shapiro [9] give an iterative description of this function which scans coordinate bit pairs, and produces the
rotation as a series of swap and bitwise complement operations applied to the bits trailing the examined pair. This adds a linear term to the overall complexity of the index serialization.

III. METHODOLOGY

A. Execution Platform

We conduct our experiments on an Intel Sandy Bridge architecture with the specifications shown in Table II. The processors feature Running Average Power Limit (RAPL) Model Specific Registers [13], which gather the energy consumed by the CPU package and memory module. By default, these performance counters provide estimates of consumed energy in multiples of 15.3\(\mu\)J. We obtain estimates using the PAPI 5.3.0 library\(^1\) which provides a high-level interface for reading performance counters.

B. Software Implementations

The experimental programs are written in C, parallelized using OpenMP, and compiled using gcc 4.7.2, with -O3 -mavx -fopenmp optimizations enabled. In dual socket experiments, all threads are evenly distributed between the sockets. Power estimates are derived from periodically measuring RAPL Model Specific Registers at a rate of 10Hz and checked against the power measurements of a Yokogawa WT210 power measurement device operating at the same sampling rate. Energy estimates are obtained from the power logs through numerical integration, by applying the trapezoidal rule. The intervals of the time integration were obtained from the timestamps of the power estimates.

C. Experimental Procedure

Table III gives an overview of our experiments. We implemented the naive matrix multiplication for three different element layouts (row-major, Morton order and Hilbert order). All multiplications were performed on square matrices of 2\(^n\) double precision elements, for \(n = 10, 11, 12\). The range of sizes is selected to expose the transition from problems that fit entirely into the last-level cache on a single socket, through to memory-bound application behavior. Clock frequency is varied either by fixing it to predetermined values of 1200MHz, 1800MHz or 2600MHz, or leaving it to vary in proportion to computational load, at the discretion of the Linux ondemand power governing mechanism. Multithreaded experiments were controlled with the thread/core affinity settings of the GNU OpenMP library. Different configurations are either denoted by \(s\) where all threads are bound to the cores on a single socket, or by \(d\) where they are distributed evenly between two sockets.

\(^1\)http://icl.cs.utk.edu/papi/

We also conducted experiments with enabled hyperthreading, however, their outcomes proved to be only marginally different from the configurations with the highest thread counts, and we therefore omitted them from the paper.

IV. RESULTS AND DISCUSSION

Our exhaustive search of the parameter space described in Section III results in a set of 216 sample points, each featuring a large number of recorded time and energy measurements. In the interest of brevity, we therefore begin this section by noting that generally, all results show execution time varying in proportion to problem size, and inversely with clock frequency and thread count.

Adding the row-major indexing cost of 1 multiplication and addition to the discussion in Section III we can sort the costs of computing row-major (RM), Morton order (MO), and Hilbert order (HO) indexing in ascending order with respect to operation counts. Recorded execution times most notably reflect this by HO indexing giving the consistently longest completion time, while the faster of the RM and MO schemes is determined by sample configuration.

A. Computational Performance

Figure 4 shows the parallel speedup of each ordering scheme with variable core counts and problem sizes. Figure 5 shows the speedup of row-major ordering with variable clock frequencies and problem sizes. Both figures show dual socket configurations, but similar tendencies were evident in the single socket results, albeit less pronounced.
From the in-cache problem size $2^{10}$ (10), differences in parallel scalability are barely distinguishable, demonstrating that the ordering of the memory access pattern is insignificant, making the superior execution time of the RM pattern favorable.

Problem sizes 11 and 12 clearly show the transition to memory-bound behavior for the RM and MO schemes: 3 double-precision square matrices of dimension $2^{11}$ (11) amount to total problem sizes of 96MB and 348MB respectively, and from the straightforward $n^3$ matrix multiplication routine, we can infer that access to the A and B matrices dominate memory access cost. The aggregate amount of last-level cache in our dual-socket configuration is 40MB, and the degradation is expected. As the speedup curves are relative to a single-thread baseline per curve, the effect on absolute speed is not visible in the figure, but as Table IV shows, the favorable access pattern of the MO overtakes RM in terms of absolute performance.

As the extreme case of trading locality for computation, the scalability and execution time of HO displays the interesting property that while its absolute execution time is an order of magnitude higher than RM and MO, its speedup curve shows slight superlinearity with increasing parallelism, specifically, at 8 threads for problem size 11, and both 8 and 16 threads for size 12.

We mainly attribute the favorable scalability of the HO experiments to the fact that the additional computation it requires parallelizes trivially, which suggests that the HO computations would become memory bound in a similar fashion to the MO computations, if the test platform supported a sufficient number of threads. This does not account for superlinear speedup, however, so a further examination aimed to establish whether this is a consequence of deviations in the measurements of the single-threaded baseline, or a consequence of the data locality properties of the Hilbert curve.

| Size  | Single Socket | Dual Socket |
|-------|---------------|-------------|
| 10    |               |             |
| 1.2   | 7.2           | 1.8         |
| 1.8   | 4.8           | 0.6         |
| 2.6   | 3.3           | 0.8         |
| od    | 2.8           | 0.6         |
| 1.2   | 22.9          | 35.3        |
| 1.8   | 108.4         | 28.0        |
| 2.6   | 91.9          | 24.6        |
| od    | 84.5          | 22.7        |
| 1.2   | 214.9         | 356.9       |
| 1.8   | 996.2         | 276.9       |
| 2.6   | 910.1         | 254.1       |
| od    | 873.7         | 244.4       |

### MO

| Size  | Single Socket | Dual Socket |
|-------|---------------|-------------|
| 10    |               |             |
| 1.2   | 13.6          | 3.4         |
| 1.8   | 9.1           | 2.3         |
| 2.6   | 6.2           | 1.6         |
| od    | 5.1           | 0.7         |
| 1.2   | 125.3         | 32.1        |
| 1.8   | 87.4          | 22.4        |
| 2.6   | 63.5          | 16.4        |
| od    | 51.6          | 13.8        |
| 1.2   | 1011.3        | 259.1       |
| 1.8   | 706.2         | 180.8       |
| 2.6   | 514.6         | 122.9       |
| od    | 419.7         | 113.4       |

### HO

| Size  | Single Socket | Dual Socket |
|-------|---------------|-------------|
| 10    |               |             |
| 1.2   | 90.0          | 22.3        |
| 1.8   | 59.5          | 14.8        |
| 2.6   | 41.4          | 10.2        |
| od    | 32.6          | 8.4         |
| 1.2   | 865.4         | 212.7       |
| 1.8   | 583.3         | 143.1       |
| 2.6   | 409.9         | 100.2       |
| od    | 324.4         | 83.6        |
| 1.2   | 7661.9        | 1887.1      |
| 1.8   | 5155.4        | 1267.4      |
| 2.6   | 3619.0        | 886.6       |
| od    | 2861.4        | 734.5       |

Fig. 5. Speedup of RM order with variable clock frequency

| TABLE IV
A B SO E C T EXECUTION TIMES S | |
|----------------------------------|-----------------|
| Size    | Single Socket | Dual Socket |
| 1       | 1              | 4            |
| 8       | 2              | 8            |
| 16      | 1              | 4            |
| 10      | 7.2            | 1.8          |
| 1.8     | 4.8            | 0.6          |
| 2.6     | 3.3            | 0.8          |
| od      | 2.8            | 0.6          |
| 11      | 22.9           | 35.3         |
| 1.8     | 108.4          | 28.0         |
| 2.6     | 91.9           | 24.6         |
| od      | 84.5           | 22.7         |
| 12      | 214.9          | 356.9        |
| 1.8     | 996.2          | 276.9        |
| 2.6     | 910.1          | 254.1        |
| od      | 873.7          | 244.4        |
| 1.2     | 13.6           | 3.4          |
| 1.8     | 9.1            | 2.3          |
| 2.6     | 6.2            | 1.6          |
| od      | 5.1            | 0.7          |
| 1.2     | 125.3          | 32.1         |
| 1.8     | 87.4           | 22.4         |
| 2.6     | 63.5           | 16.4         |
| od      | 51.6           | 13.8         |
| 1.2     | 1011.3         | 259.1        |
| 1.8     | 706.2          | 180.8        |
| 2.6     | 514.6          | 122.9        |
| od      | 419.7          | 113.4        |

framework. It allows matching of memory hierarchy effects to specific locations in the source program. An instrumentation overhead of an approximate factor 100 made it prohibitive to fully run our largest scale computation to completion in this manner, but an estimate can be obtained by restricting the ZO and HO codes to complete a small number of rows in the output matrix, thereby ensuring that several complete traversals of one entire input matrix have been performed, to elicit effects of any significantly different locality properties of its encoding.

Performing this additional experiment for 5 rows near the middle of the C matrix in a size 12 problem resulted in a total of $16.78 \times 10^6$ last-level data read misses for HO compared to $17.06 \times 10^6$ for MO, suggesting that while the superior data locality is far from significant enough to amortize the additional computation cost of Hilbert indices on our test system, it is a measurable effect that makes its applications
more amenable to parallelization.

B. Energy Consumption

The RAPL register results collected from each run are displayed in Figure 6, which plots total energy vs. execution time. Individual points represent particular energy figures, with dashed and solid lines grouping points by the processor feature they represent, and the 4 points of each line representing tests at different clock frequencies.

Package curves represent the sum of energy from the individual packages situated on each socket. Power plane curves reflect the portion of the package total that is due to the processing cores. DRAM curves are the sum of energy consumption from the memory modules attached to both sockets; these are reported in sum for all configurations, because the virtual memory abstraction of the operating system prevents programs from explicitly controlling the placement of the memory allocations that belong to a given application.

The samples from the 8d and 8s configurations are representative of tendencies throughout our results, but were selected because these configurations permit comparisons of identical thread counts distributed on 1 and 2 sockets. Results are shown for the RM and MO patterns only, as the computational overheads of the HO cases are substantially larger, and would therefore require a figure scale which would complicate comparisons.

Subfigures c) and f) show the largest problem size, where the computation is memory bound, making the locality improvement of the MO most significant. The RM results are interesting in these cases, because they show that while speed advantages are attained at higher clock frequencies, the impact in energy consumption is greater; a similar tendency can also be seen in subfigures b) and e). Noting that the effect appears from frequencies 1800MHz and higher, it appears as a consequence of raising the processing rate higher than the memory bus clock, which operates at 1600MHz. Thus, the common assumption that optimal execution speed can be equated with optimal energy efficiency must be refined in the case of memory-bound computations, as the attainable speed improvements in this region come at an energy cost that is disproportionate to their gains. Note also that the MO curve does not equally saturate the memory system, and continues to attain improvements with rising frequency.

Subfigures a) and c) display the in-cache problem size 10, where the order of data element access is practically insignificant, making the RM indexing the faster implementation, and this translates to lower energy consumption. We can also note that the in-cache problem size displays another effect: the RM figures for powerplane and package grow closer with rising clock frequencies, suggesting that the powerplane takes up an increasing fraction of the package power budget with increasing computational speed. This can be contrasted with the memory bound computations, where the package energy consumption follows that of the powerplane, suggesting increasing loads on both the processing cores and their shared on-chip resources.

DRAM energy consumption is nearly constant, except for a slight shift towards lower total energy usage for higher frequencies where computations complete faster. The most significant observation from these measurements is that total DRAM power consumption is small in comparison to that of the processing cores’ consumption, differing by factors close to 4 for high frequencies.

Contrasting single socket and dual socket results, we observe that the difference in execution time becomes quite noticeable for large problem sizes, resulting in a difference of nearly 50 seconds between subfigures c) and f). This reflects that the synchronization overhead of the implicit barrier following a straightforward parallel OpenMP loop implies a greater latency when threads are scattered across multiple sockets, and the energy impact is most notable at low frequency.

The exact consequences of enabling the ondemand power governor mechanism are difficult to establish without more detailed traces of run time behavior, but already from the presented results, we note that our test system processors feature Intel’s Turbo Boost performance enhancements, which places the system at liberty to selectively overclock individual cores when doing so does not exceed the package thermal design point. This allows it to produce superior run times compared to results from maximal fixed frequency settings, but it consistently makes energy efficiency deteriorate for out-of-cache problem sizes.

We took samples from our power estimates and compared them to the full system power measurements obtained from the Yokogawa WT210. In our test system, the memory and the two CPUs account for approximately 38% of the total system consumption when all cores are utilized.

For completeness, we also performed comparisons with ATLAS. As expected, the ATLAS library outperformed our multiplications by an order of magnitude, but at the cost of a one-time investment of a two hour auto-tuning process.

V. RELATED WORK

Space-filling curves have been studied extensively throughout the years, and have found use in several application areas such as heuristics for combinatorial problems, data-bases and geographical information systems as well as signal processing. Bader et al. 16 present an algorithm for cache oblivious dense matrix-matrix multiplication based on the Peano curve 17. It uses a recursive block multiplication scheme to exploit the recursive nature of the Peano curve, and is asymptotically optimal in the number of cache misses for an ideal cache. Efficient parallel implementations have been developed 18, 19, and an extension for sparse matrix-matrix multiplications exists 20. In computer graphics, space-filling curves are used as scanning orders for images, preserving some of the spatial information of the scanned multi-dimensional space within the single dimension of the scan. Witten et al. 21 used this technique to construct a dither with a low cumulative error over large and small regions of the image, whereas Ansari et al. 22 and Yang et al. 23 employ the Peano scan 24.
Fig. 6. Energy and time samples from experiment configurations 8s and 8d
for clustering highly correlated data before compression, and therefore achieving a higher compression ratio. A thorough treatment of space-filling curves along with their applications can be found in Michael Bader’s book [10].

Over the last years there has been considerable research into reducing energy consumption of workloads through the help of hardware counters. Ge et al. [24] use them to periodically collect events such as retired instructions, L1/L2 data cache accesses and memory data accesses for identifying on-/off-chip phases in workloads and adjusting the CPU’s frequency with DVFS such that energy usage is minimized while performance retained. Hsu et al. [23] make similar predictions based on MIPS (millions of instructions per second). Huang et al. [27] use the CPU’s decoder/dispatch stall cycles in addition to L2 cache misses, and stall cycles due to branch misprediction. Porterfield et al. [28] use the RAPL interface to dynamically throttle the number of threads to reduce the energy consumption in OpenMP programs.

VI. CONCLUSIONS AND FUTURE WORK

In this paper, we studied the energy and locality effects of the Morton and Hilbert space-filling curves, with application to dense matrix-matrix multiplication. We showed that energy consumption is only exclusively proportional to the execution time when the computation is CPU bound. When memory traffic begins to dominate computation, increasing the frequency results in higher energy consumption in exchange for diminishing run time improvements. The results also revealed that the energy spent accessing DRAM is small and constant compared to the amount spent by caches and CPU. We conclude that the gap between memory and CPU performance has significant impact on energy efficiency, making improvements in the utilization of the memory hierarchy as important as minimizing execution time.

Selecting appropriate data structures is one way to improve memory hierarchy utilization, and we investigated the application of Morton and Hilbert orders to matrix multiplication. We found that while both orders improved spatial locality, Morton order results in practical improvements over naive approaches on our test platform, while the greater computational requirements of the Hilbert ordering render it impractical.

Although the locality properties of the Hilbert ordering were eclipsed by the associated indexing cost, we observed that its locality effect offers a moderate improvement over that of the Morton order. The additional computational cost of Hilbert ordered indexing amounts to simple bitwise register manipulations. An interesting direction for future work would be to investigate the benefit of dedicated hardware support for the required operations, as this would greatly reduce the overhead.

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