Anomalous Subthreshold Behaviors in Negative Capacitance Transistors

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Abstract—Recent measurements on ultra-thin body Negative Capacitance Field Effect Transistors have shown subthreshold behaviors that are not expected in a classical MOSFET. Specifically, subthreshold swing was found to decrease with increased gate bias in the subthreshold region for devices measured over multiple gate lengths down to 30 nm. In addition, improvement in the subthreshold swing relative to control devices showed a non-monotonic dependence on the gate length. In this paper, using a Landau-Khanatnikov ferroelectric gate stack model calibrated with measured Capacitance-Voltage, we show that both these anomalous behaviors can be quantitatively reproduced with TCAD simulations.

Index Terms—Negative Capacitance, Ferroelectric, Short Channel Effects

I. INTRODUCTION

NEGATIVE capacitance field effect transistors (NCFET) rely on a ferroelectric gate insulator to provide an amplification of the gate signal [1]–[3]. This boost, which depends on the capacitance matching between the ferroelectric and Si underneath, in turn, reduces the power supply voltage requirements. In a properly designed MOSFET, such a boost can also lead to a sub-thermal subthreshold swing (SS). However, the strong function of Si capacitance with voltage and inadequacy of available ferroelectric materials makes it difficult to obtain a sub-thermal subthreshold swing without hysteresis [4], [5].

On the other hand, the objective of reducing supply voltage can be achieved by improving the swing near the threshold and this can be done without violating the condition necessary for zero hysteresis [6]. NCFET so designed can show obvious non-classical behaviors.

Indeed, substantially improved I-V characteristics and non-classical subthreshold behavior have recently been observed in Zr doped HfO₂ gate stack (HZO) [7]–[11] that has a polar order [12], [13]. Despite the same thermal processing, doping, and MOSFET geometry (Fig. 1(a)), the HfO₂ (Control) and HZO (NCFET) gate stack devices demonstrate opposite trends of subthreshold swing with respect to gate bias (Fig. 1(b)) [7]. Figure 2 shows that for all gate lengths (L_G) at V_DS=0.05V, the NCFET SS is similar to SS of the Control of the same geometry at low drain current (I_D=10pA/µm) but is lowered as the gate bias increases. The I_D at which NCFET subthreshold swing reaches its minimum is almost 4 orders of magnitude larger than the OFF current. In addition, the difference in the subthreshold swing between Control and NCFET devices (measured in the range I_D=0.1nA~1nA/µm) increases significantly from L_G=100nm to L_G=50nm but decreases from L_G=50nm to L_G=30nm (Fig. 3).

Remarkably, these two trends for the HZO devices cannot be explained by assuming a “higher-κ” linear dielectric gate stack which would lead to monotonically increasing improvement of SS as L_G shrinks. Neither are they explainable with a better interface quality than the Control, as it would result in a constant SS reduction over different L_G. In contrast with normal dielectric theory, these anomalies indicate that NCFET gate capacitance (C_G) (Fig. 1(c)) is affected significantly by both V_GS and L_G, of which the explanation lies in the non-linear polarization response to the applied electric field for the HZO gate stack layer [4], [14].

II. TCAD MODEL CALIBRATIONS

Sentaurus TCAD [15] simulator parameters are calibrated to C-V and I-V data from [7]. For both Control and NCFET,
the gate insulator constitutes of a chemical oxide (8) and 2.8nm layer of HfO2 or HZO. HfO2 MOSCAP Accumulation C-V measurements can be well matched by a 1.1 nm EOT gate stack in the TCAD model (Fig. 2a). The HZO stack demonstrates a higher capacitance which could be fitted with very high dielectric constant for the HZO stack. However, this would require an effective dielectric constant (>100) that is much higher than any theoretical predictions for Hf and Zr-based dielectric phases [16–20]. In addition, this hypothetical “super-high κ” dielectric would not be able to replicate the anomalous subthreshold behaviors that we observed. Instead, the capacitance boost is captured by the potential amplification effect [11], [14], [21] induced by a the presence polar phase inside the HZO layer.

The calibrated simulation reproduces the experimentally observed subthreshold behavior for the Control MOSFET (Fig. 2a). NCFETs are simulated by introducing the Landau-Khalatnikov (LK) model for simulating the gate stack, but non-gate-stack parameters are unchanged from the Control devices. The LK parameters are chosen such that the Ferroelectric in the positive capacitance (PC) region results in the same gate stack EOT (1.1 nm) as the Control. Therefore, the SS in the low $I_D$ (10-100pA/μm) region are matched between Control and NCFET devices. As the gate bias is increased, the Ferroelectric enters into the negative capacitance (NC) region, which results in a reduced gate stack EOT of 0.9nm in accordance with the HZO C-V. This transition from positive to negative capacitance regime successfully captures the near-threshold SS reduction (Fig. 2) with respect to $I_D$ as well as the non-monotonic SS improvement trend with respect to $L_G$ (Fig. 3b inset). This is discussed in more details later.

III. RESULTS AND DISCUSSIONS

Fig. 3b) shows threshold voltage ($V_t$) calibration results with tungsten work-function set to 4.6eV according to C-V calibrations (Fig. 4a). Note that Control MOSFET $V_t$ would be underestimated by 0.18V if no net defect charges are assumed, and this discrepancy is insensitive to geometry and doping profiles when SS scaling trend is captured. Therefore, the difference between the MOSCAP and MOSFET $V_{FB}$ is ascribed to additional defect charges introduced by transistor fabrication process. A fixed charge density of -0.6μC/cm² at the Si/SiO2 interface can not only account for the $V_t$ shift but also explain the small measured $V_t$ difference between Control and NC devices (Fig. 4b). The voltage drop on the gate stack induced by the charges is less for the NCFET than the Control because of mitigated short channel effects. Note that, the introduction of negative fixed charges into the model is consistent with our previous work as described in [22] where the transistor fabrication followed essentially the exact same procedure.

Fig. 5 shows the transitions from positive to negative capacitance region of the HZO stack. When $V_{GS}$ ramps up, both $I_D$ and the external electric field on the gate stack ($E_{ext} = Q_G/\epsilon_0$) increases. The HZO polarization is directly determined by $E_{ext}$ if polarization gradient energy is negligible. The $Q_G-I_D$ slope in the subthreshold regime is associated
Fig. 5. (a) Extracted Q-E relation for the polar layer of the gate stack at the mid-channel of NCFETs at $V_{DS}=50\text{mV}$. For each gate length, the gate voltage is ramped at which ID is from 0.1nA/\mu m to 1nA/\mu m. (b) Simulated relations between drain current and (left axis) local gate charge density / (right axis) local external electric field at $V_{DS}=0.05\text{V}$ for NCFETs. For each gate length, the solid line is extracted at mid-channel gate stack region, and the dash line is extracted at the region 15nm laterally from mid-channel toward the drain. The white-background region corresponds to bias conditions at which the polar layer exhibits negative capacitance, while the dark background stands for positive-capacitance regime.

with input capacitance $C_{gg} = \left( \frac{1}{C_g} + \frac{1}{C_s+C_d+C_Q} \right)^{-1}$, which increases for reduced $L_G$ because of $C_s$ and $C_d$ increase. As the device enters the negative capacitance region, a voltage amplification ensues and drives down the subthreshold swing. This explains why, for the NCFET, the subthreshold swing gets steeper in the subthreshold regime as $V_{GS}$ or $I_D$ increases. To fully understand the observed anomalous behaviors, especially the effect of $L_G$, one needs to consider the inner fringing field that plays a crucial role on the capacitance matching effect [22], [23]. This field leads to the gate stack-to-source and gate stack-to-drain capacitive coupling which reduces $Q_G$ to balance the positively ionized source and drain donor charges for n-MOSFET in subthreshold regime. When $L_G$ shrinks, mid-channel $Q_G$ corresponding to the same $I_D$ decreases because of the increased inner fringing field. As a result, although the mid-channel gate stack is in the negative capacitance regime for $L_G$ from 50nm to 100nm at $I_D=0.1\text{nA}/\mu \text{m}$, it remains in the positive capacitance regime for the 30nm case (Fig. 5). Therefore, the improvement in the subthreshold swing for NCFETs drops for $L_G=30\text{nm}$ as shown in Fig. 3(b).

Notably, the extracted $Q_G$ at which the HZO gate stack starts to exhibit negative capacitance is approximately 0.5\mu C/cm² (Fig. 5(a)). In other words, the S curve is pushed up in the charge axis. This is a consequence of the negative fixed charge that simultaneously explains the $V_t$ trend for both Control and the NCFET. The atypical response can be a result of antiferroelectric behavior of the tetragonal phase [13] in the HZO or a small but finite leakage that induces positive charge trapping at the SiO₂/HZO interface and effectively shifts the S-curve [24], [25].

IV. CONCLUSION

To summarize, we developed an FE model that simultaneously explains (i) SS getting steeper with increasing $I_D$ in the subthreshold regime, and (ii) non-monotonic behavior of SS improvement with $L_G$ trends that cannot be explained by a classical “high-κ” scaling theory. Our results show that the capacitance matching leads to (i), while the inner fring field induces change in the capacitance matching in short channel MOSFETs and leads to (ii). This model supports the notion that Ferroelectric material optimization with appropriate device design [26] to maximize near threshold capacitance matching may lead to significant reduction in $V_{DD}$. 


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