Review of Modern Field Effect Transistor Technologies for Scaling

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Abstract—This paper mainly reviews the field-effect transistor technology most involved in the modern electronics industry. Short channel effect promotes the continuous update of the field effect transistor structure. Therefore, the principle and influence of the short channel effect is first introduced. This paper focuses on the development history and current status of fin structure and gate-all-around field effect transistors, as well as their respective technical difficulties. By reviewing these two main technologies, the development process and technical difficulties of the technology are basically clarified. At the same time, the applications of these technologies in the enterprise are introduced. And finally, the future development trend of the technology is proposed.

1. INTRODUCTION
Nowadays, integrated circuits exist in all aspects of our lives, from personal computers to mobile devices. With the development of economy and the improvement of electronic technology, people have put forward higher requirements for high performance and portability of these electronic devices. According to the latest authoritative data and predictions, the revenue of consumer electronics products is expected to be US$365,538 Million in 2020, and the market size will reach US$450,387 Million in 2024 [1]. These devices have become more and more miniaturized owing to the application of very large-scale integration (VLSI). Metal oxide semiconductor field-effect transistors (MOSFETs) are the basic units in VLSI. As FET technology keeps scaling down, extremely large-scale integration (ELSI) become possible.

With the continuous improvement of the manufacturing technology, planar MOSFET is processed smaller and smaller, making the channel length shortened. As a result, the short channel effect (SCE) becomes an unavoidable problem. To solve this critical problem, scientists and engineers attempted to change the materials and structures between the gate and the channel, and proposed a three-dimensional (3D) FET structure instead of the conventional two-dimensional (2D) FET [2]. FinFET technology has been dramatically developing in many chipmakers and Intel adopted it in their Core I series of processors. However, mature technologies cause problems with practical development. The unique structure of FinFET and the narrowing distance of each gate bring challenges to the manufacturing process. Thereupon, a new evolution of FinFET technology, gate-all-around (GAA) technology, has attracted people’s attention.

This article first introduces SCE which is the main reason for the development of FET from 2D to 3D, and then respectively reviews the development history of FETs with Fin and GAA structure. Some challenges and difficulties for future development of these technologies are also presented.
2. SHORT CHANNEL EFFECT
The planar structure of MOSFET is continuously reduced to improve the performance of the chip. When the length of the channel is equal to the width of the depletion layer in the source and drain junctions, MOSFET would suffer from a specific effect called SCE [2]. In the channel, the SCE influences the threshold voltage, drain-induced barrier lowering, velocity saturation of carrier and hot carrier degradation [3]-[4].

The SCE affects the threshold voltage. A large number of experimental results have proved that the surface electric field reaches a maximum in the middle of the channel region at a lower drain voltage. When the drain voltage becomes more extensive, the maximum point of the surface electric field moves toward the source. Fig. 1 shows narrowing the channel causes the source and drain to interact with each other, resulting in a reduced threshold voltage [5].

![Fig. 1 Schematic of various regions involved in charge sharing. Regions I, II, and III are the source, gate, and drain-induced depletion regions, respectively.](image)

Fig. 2 illustrates the model of SCE in silicon-on-insulator (SOI) MOSFET [2]. Through this figure and formulas (1) and (2) (given below), it can be seen that the impact of SCE on the threshold voltage.

![Fig. 2 SOI MOSFET structure with a simple charge-sharing representation.](image)

The depletion charge $Q_{b\text{(eff)}}$ controlled by the front and back gates can be expressed as

$$Q_{b\text{(eff)}} = (1-d/L)Q_b$$  (1)

where $L$ is the channel length of MOSFET, $d$ is the distance over the back-surface potential and $Q_b=qN_{D}t_b$ is the total charge per unit area in the fully depleted film, in which $q$ is the amount of charge and $N_D$ is the uniform body doping fabricated on the thin SOI film with thickness of $t_b$. The reduction in threshold voltage can be expressed by

$$\Delta V_T(L, t_b) = |V_T(Q_b) - V_T(Q_{b\text{(eff)}})| = d/L \cdot q/2 \cdot N_D / L \cdot t_b / C_{of}$$  (2)

in which $C_{of}$ is the front-oxide capacitance.

Due to the SCE, the depletion region of the drain is close to the diffusion region of the source, resulting in a significant field penetration from drain to source. This field penetration leads to a lower
barrier for the source. This process is called drain-induced barrier lowering (DIBL), which results in an increased injection of electrons by the source over the reduced channel barrier and consequently a raised source to drain current [6]. In Fig. 3, $\Delta \phi_s$ shows the potential barrier lowering [7].

![Fig. 3 Potential distribution along the channel surface for a long- and short-channel MOSFET device at $V_{GS}=V_{BS}=0$, in which $V_{GS}$ and $V_{BS}$ are gate and base to source voltages, respectively.](image)

Velocity saturation and hot carrier degradation are also concerning about the SCE. As the size of the chip continues to decrease, the electric field and the velocity of the carrier increases. However, the velocity of the carrier no longer exists a linearly relationship with the electric field when gradually saturated [4]. Besides, the continuous shrinking of MOSFETs would bring about a problem of hot carrier degradation. The mechanism of hot carrier degradation is the hot hole and electron injection, which adversely affects the life of electronic components [8].

Based on above description, we can see that as MOSFETs shrink, the impact of SCE is manifold, and all side effects related to SCE seriously hinder the performance improvement of chips. Also, controlling the impact of SCE means increased manufacturing costs. In such a context, a revolution of MOSFET structure with 3D gate happened.

3. OVERVIEW OF FINFET

3.1 Development History

In 1991, Hisamoto et al. proposed a vertical ultra-thin-gate structure for MOSFET and proved that it could suppress SCE [10], which provides a foundation for FinFET structure that developed later. Fig. 4 exhibits the basic structure of FinFET [11], from which it can be seen that the FinFET structure transforms the gate control of the channel into 3D in both the horizontal and vertical directions.

![Fig. 4 3D view of FinFET structure.](image)
SOI MOSFET, of which the gates are distributed on the narrow channel sidewalls in both the horizontal and vertical directions [12]. Since then, FinFET has been developing rapidly. Through successive researches and experiments, FinFET technology has been improving continuously.

From 1998 to 2002, the physical structure of FinFET reached a gate length of 10 nm. Prof. Chenming Hu played a crucial role in the development of the FinFET during this period. He pointed out that not only can FinFET scale down further, but also the physical properties can be improved by changing the gate material such as high-k material or metal gate [13]-[14]. “For a distinguished career of developing and putting into practice semiconductor models, particularly 3D device structures, that have helped keep Moore’s Law going over many decades”, he was awarded the IEEE Medal of Honor Award in 2020.

Bohr and Mistry reported in May 2011 that processors using 22 nm Tri-Gate transistors had been proved to work in system, which had 37% performance increase at low voltage and greater than 50% power reduction at the consistent performance [15]. This processor with a code-named of Ivy Bridge, that is part of the Core I series of Intel processors, launched the era of full application of FinFET technology. Nowadays, the competition in the chipmaker market is fierce, especially between Taiwan Semiconductor Manufacturing Company (TSMC) and Samsung. TSMC and Samsung are ramping up 5 nm chips and other half-nodes offerings [16].

3.2 Challenges and Difficulties
FinFET technology has been put into practice, however, there are several challenges and difficulties in the manufacturing process. FinFET structure has high access resistance, which is caused by the very thin structure and the difficulties in the formation of 3D junctions [17]. Fig. 5 shows the implant damage and problematic recrystallization during post-implant anneal [17]. The structure of FinFET will affect the voltage and current characteristics of the device. Metal gate granularity (MGG) and fin edge roughness (FER) will cause threshold voltage variability, whereas line edge roughness (LER) will lead to the maximum drive current variability [18]. These possible manufacturing difficulties would affect the performance of FinFET.

![Fig. 5 Implant damage and problematic recrystallization.](image)

Slight doping in the channel can change the threshold voltages in certain devices or better control of under-the-fin leakage current. However, this process also damages the structure of fin. High temperature (300-400 K) implants or plasma-based doping can reduce this damage [19].

The technical requirements of the manufacturing process for FinFET are more stringent when compared to planar FET. Pal et al. pointed out that for the length of gate under 20 nm, uniformity of about 1 nm for fin width <10 nm is necessary to maintain low threshold voltage variations [9]. At the same time, FinFETs have changed the structure from the traditional two-dimensionalities to the construction of fin with three-dimensionalities, which needs to satisfy both mechanical and electrical properties.
4. OVERVIEW OF GAAFET

4.1 Development History

For FinFETs of 5 nm, the channel control capability is not sufficient due to SCE. Thereupon, people tend to develop a FET structure of GAA, further improving the form of interaction between the gate and the source and drain. The GAA structure was first reported by Toshiba ULSI Research Center in 1988. Takato et al. proposed a surrounding gate transistor (SGT) structure with a gate surrounding the channel as shown in Fig. 6 and proved the advantages for VLSI over planar structure [20].

For the first time in 2006, Lee et al. successfully produced a sub-5 nm all-around gate FinFET with 3 nm fin width [21], as shown in Fig. 7. Singh et al. demonstrated that Si nanowire-based GAA n- and p-FETs structure shows excellent electrical performance, and the gate length can be further reduced using new channel materials [22].

Samsung redesigned the GAA structure and applied for the multi bridge channel FET (MBCFET) patent. Fig. 8 displays the FET development path and MBCFET structure. MBCFET is a version of GAAFET, which has better performance than the conventional GAAFET [23], such as better gate control of channel, higher DC performance under certain conditions and better design flexibility that means designers can easily convert FinFET to GAAFET [24]. When compared to 7 nm-node FinFET technology, advanced node MBCFETs consume 50% less power, improve 30% better performance and reduce 45% less area. For these reasons, Samsung and Intel have turned to GAAFET technology instead of FinFET.
4.2 Challenges and Difficulties

The GAA realizes a more exceptional transistor structure, but also brings about many challenges to processing and manufacturing. Since FinFET technology has been developed for many years, chipmakers demand a large amount of cost for process switching to GAAFET. And the introduction of new materials makes the process more elaborate and requires higher environmental conditions. Besides, the continuous shrinking of GAA structure gives rise to several manufacturing problems. Backend-of-the-line (BEOL) is where the copper interconnects are made in chips. The interconnect is becoming more and more compact at each node, which leads to serious resistance-capacitance delay [16].

Another challenge for GAAFETs is more difficult detection and measurement due to the increase density of FETs. As the manufactured chips become more and more refined, changes in the internal structure become more and more difficult to detect, and even minor changes will cause the system to slow down [26]. In higher-end chips, chipmakers need a variety of different measurement tools to ensure non-destructive measurement during production. For MBCFETs, measuring the replacement of a single nanosheet is the most difficult. The nanosheet with the worst performance determines the quality of the entire transistor. Fortunately, certain artificial intelligence techniques may assist in these non-destructive testing [25].

Lithography is an essential process for manufacturing chips. The current extreme ultraviolet lithography (EUV) technology hardware cannot meet the needs of 3 nm-nodes GAAFET. A new EUV technology called high-numerical aperture EUV (high-NA EUV) would solve this situation [27]. Technological innovations often bring updates to the entire process.

5. Conclusions

At present, both Samsung and Intel have decided to adopt GAAFET technology as the development direction for the next-generation semiconductor chips. Whereas TSMC follows the technical route of FinFET in 3 nm-node which is more mature for them, although it would definitely face many challenges as FinFETs further shrink. It has been proven that GAAFETs are emerging as the successors to FinFETs for extremely scaled process nodes. However, in view of the current technology level, volume production of chips based on GAAFET requires a lot of costs in design and manufacturing, and several new issues are also worth paying attention to. In short, what is the right technical route for scaling of FETs depends on the market, which is worth looking forward to.

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