The Analysis of DC Fault during the Hybrid MMC Start-up Process

Lei Han *, Junfeng Jiang a and Haitao Yao b

School of Electrical and Information Engineering, Jiangsu University, Zhenjiang 212013, China.

* Corresponding author: 1294119299@qq.com, a2724792281@qq.com, b15670351387@163.com

Abstract. The hybrid Modular multilevel converter (MMC), which includes both full-bridge sub-modules (FBSM) and half-bridge sub-module (HBSM), has DC fault ride-through capability and is receiving more and more attention. Current researches are focused on the DC fault in the normal operation of the system. However, there is a lack of analysis of the DC fault during start-up process. This paper introduces the characteristics of the pole to pole fault during the start-up process and analyzes the effect of the pole to pole fault on the sub-module charging. Simulation in PSCAD/EMTDC is implemented to verify the correctness of analysis in this paper. Based on that, new suggestions for DC fault protection are proposed.

Key words: hybrid MMC; HBSM; FBSM; start-up process; DC fault.

1. Introduction

MMC has become more and more popular due to its advantages in recent years [1-3]. At present, half-bridge sub-modules (HBSM) structures are mostly used in engineering. When the DC fault occurs, the IGBT in the half-bridge sub-module will be turned off. Due to the characteristics of the diodes of the sub-modules, the AC system forms a short circuit with the fault point [7]. Therefore, MMC based on half-bridge sub-modules cannot block DC faults by themselves. So the research on improving the DC fault capability of the MMC has become a focus, including the improvement of the MMC topology [8]. A modular multilevel converter based on full-bridge sub-module (FBSM) can output a negative voltage to block the DC fault current after DC fault [9]. The power dissipation is greatly improved since the power switching device of the HBSM is twice that of the HBSM. Current blocking method for pole to pole fault during normal operation has been proposed in [10-11]. The hybrid sub-module combining the HBSM and the FBSM has both their advantages and therefore is very promising in engineering application.

The condition for the operation of the MMC is that the sub-module capacitor must have a certain voltage, so the pre-charging problem of the MMC is the most basic problem. In the hybrid MMC charging process, the charging speed of FBSM is twice that of HBSM. That is to say, the voltage of two kinds of sub-modules will be different after uncontrolled charging stage. Thus it is necessary to adopt an appropriate strategy to eliminate the voltage difference.
This paper is structured as follows. Section II introduces the hybrid MMC start-up process. Section III analyses the influence of DC fault on sub-module in the different charging stage. The simulation in PSCAD/EMTDC and correlation analysis are present in section IV. Section V concludes this paper.

2. Hybrid MMC Start-Up Process

The topology of hybrid MMC and sub-module is shown in Fig. 1.

![Figure 1. Topology of the hybrid MMC and SM](image)

Each arm consists of \(N\) SMs, including \(N_h\) HBSMs and \(N_f\) FBSMs. \(k\) indicates the proportion of the FBSM in each arm. Rated voltage of the sub-module during normal operation is \(U_{cr}\). \(M\) represent the modulation index. When the system in the normal operation mode, \(M\) can be given as

\[
M = \frac{2U_p}{U_{dc}} = \frac{2U_p}{NU_{cr}} \quad (1)
\]

\(U_p, U_{dc}\) represent peak phase voltage and dc-link voltage. Then the rated capacitor voltage is

\[
U_{cr} = \frac{U_{dc}}{N} = \frac{2U_p}{MN} \approx 1.36 \frac{U_l}{N} \quad (2)
\]

The start-up process consists of uncontrollable precharging stage and controllable precharging stage.

2.1. Uncontrollable Precharging

The charging of MMC is a RLC circuit. There are three stages of uncontrolled charging of hybrid MMC. The charging circuit of \(U_{ab}\) is shown in Figure 3. Obviously, the charging current reaches its maximum when the system starts. Therefore, it is necessary to connect current limiting resistance to reduce charging current \(I_{max}\).

![Figure 2. Ac uncontrolled charging loop](image)

1) Stage I: Since HBSM and FBSM are blocked at the beginning of the start-up process, current can only flow into the capacitor through the anti-parallel diode. As can be seen from the figure 2, the FBSM is always in charge regardless of the current direction and the HBSM is only charged when the current is positive. Therefore, the voltage of FBSM is twice that of HBSM after stage I.

2) Stage II: Bypass the FBSM and charge the HBSM uncontrollable. This stage is to raise the HBSM voltage to the same level as FBSM.
3) Stage III: Keep T4 switch on. At this time, the charging characteristics of FBSM are the same as that of HBSM. At the end of this stage, all SM capacitors are charged to the uncontrollable steady-state voltage.

2.2. Controllable Precharging
In this stage, the control module is used to keep the sub-module capacitors charging balanced until it is charged to the rated level. Constant DC voltage control method is used to charge capacitors to nominal value. The current limiting resistor is bypassed.

3. DC Fault Analysis During Charging Process
The pole to pole fault is one of the most serious faults of DC transmission. After the fault occurs, the sub-module will continue to discharge until the MMC is blocked. After that, the system is equivalent to a three-phase short-circuit fault.

3.1. Pole to Pole Fault during Uncontrolled Charging
Since the sub-module during this process is uncontrolled, the analysis principles is similar to the pole to pole fault after the sub-module is blocked during normal operation.

3.1.1. DC Fault in Stage I. When the fault occurs, the capacitor will continue to charge. At this time, the upper and lower arms of each phase are equivalent to parallel connection. The equivalent diagram of the new charging circuit formed by the $U_{ab}$ as a short circuit is shown in Fig.4.

![Figure 3. Charging circuit when fault occurs](image)

The current reference direction of each arm is indicated in the figure4. FBSM provides back electromotive force regardless of current flow while HBSM provides back electromotive force only when current is positive. Since the charging speed of each phase is the same, the voltage difference of the sub-modules can be neglected. Combined with the figure, we can obtain $U_{AF}=U_{BF}=U_{ab}/2$. So the arm will stop charging when the sum of the the sub-modules voltage reaches half of the line voltage amplitude. When the current direction is opposite to the reference, the HBSM capacitor is bypassed by the anti-parallel diode. Therefore, the number of sub-modules between the upper and lower arms participate in charging is different. That is to say, the back electromotive force provided by the two arms are different. The HBSM will no longer be charged when the sum of all sub-modules voltage in the arm reaches $U/2$ and the charging of FBSM will continue until the fault is blocked. When the pole to pole fault is blocked, the FBSM voltage is

$$U_{df} = \frac{U_i}{2N_f} = \frac{U_i}{2kN}$$

(3)

If $k<0.37$, the voltage of FBSM will exceed the rated value. The voltage may exceed the capacitor withstand voltage and the capacitor is at risk of breakdown.

3.1.2. DC Fault in Stage II and Stage III. The working state of FBSM in these two stages does not have the ability to block the DC fault. When the sub-module voltage reaches a steady state, there is still a fault current flowing through the fault point.

3.2. Pole to Pole Fault during Controllable Charging
When the fault occurs during normal operation of the system, the fault process can be divided into two stages. The arm current increases rapidly when the fault occurs. It is a superposition of the AC short-
circuit current and the sub-module capacitor discharge current, wherein the sub-module capacitance discharge accounts for a larger proportion. The discharge circuit is shown in Fig.4. Considering that the voltage of the sub-module in the controllable charging stage has not reached the rated voltage, the discharge current of the capacitor is much lower than that during normal operation. When the MMC is locked, the AC side charges the capacitors of the FBSM until the DC fault is blocked. Since there is no current limiting resistor, the short circuit current is very large before the fault is isolated.

**Figure 4.** Equivalent diagram of sub-module discharge loop

### 4. Simulation Result

In order to verify the previous analysis, the pole to pole fault during the hybrid MMC start-up process was simulated in PSCAD/EMTDC. The system parameters of the hybrid MMC-HVDC are shown in Tab.1.

| Items                  | Values |
|------------------------|--------|
| AC side voltage/kV     | 500    |
| Number of HBSM         | 12     |
| Number of FBSM         | 12     |
| Sub-module capacitor C/μF | 5000  |
| Arm inductor L0/mH     | 10     |
| DC side voltage/kV     | ±280   |

**Figure 5.** DC fault occurs during uncontrolled precharging process: (a) bridge arm current (b) positive DC current

As shown in Fig.5, a pole to pole fault occurs at 0.5s, the system is in the stage I of uncontrollable precharging process. It can be seen that the arm current is single-passed after the DC fault occurs. That's because the back electromotive force provided by the two arm sub-modules is different. The DC current rises rapidly at 0.5s, but the current limiting resistor in each arm limits the DC current to a small value. With the increase of sub-module voltage, the magnitude of both the DC current and arm current will decrease.
When a DC fault occurs during controllable charging process, as shown in Fig.6, the sub-module capacitor discharge causes the arm current and DC current to rise rapidly. As the energy in the sub-module is gradually released, the fault current is correspondingly reduced. Therefore, the discharge of sub-module is the main cause of current rise, which is consistent with the previous analysis. After the MMC is locked, the AC system will charge the FBSM until the DC fault is blocked.

5. Conclusion
The start-up of MMC-HVDC is an important part of the system operation, the DC fault during this process cannot be ignored. DC fault characteristics are different between start-up process and the normal operation. Although FBSM has the ability to block the DC fault, it does not work in the stages II and stages III of uncontrolled charging process.

When the fault occurs during uncontrolled charging process, the current limiting resistor limits the DC current to a small value. Taking over-current protection as an example, the DC line current rises rapidly but may be lower than the current criterion of protection. The protection may refuse to operate at this time. Therefore, the setting value of over-current protection should consider the case of DC fault during start-up, and adopt different current protection settings during start-up and normal operation.

After the DC fault is blocked, the voltage of FBSM may exceed the normal operating voltage rating \( U_{cr} \). Therefore, it is necessary to increase the proportion of FBSM to ensure its fault block ability while avoiding the risk of capacitor breakdown.

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