H-cluster: a hybrid architecture for three-dimensional many-core chips

Huafeng Sun¹, Huaxi Gu¹(a), Yintang Yang², and Jian Zhu³
¹ State Key Laboratory of ISN, Shenzhen CU-Xidian Joint Center, Xidian University, Xi’an, China
² Institute of Microelectronics, Xidian University, Xi’an, China
³ Shenzhen Research Institute, CUHK, Shenzhen, China

Abstract: With more and more cores integrated in a single chip, three-dimensional network-on-chip (3D NoC) based on through-silicon-via (TSV) is a good way to deal with the problem of large network diameter. But if the number of cores increase to several hundreds or even thousands, the large number of TSV cannot be neglected any more due to the low yield and high overhead of TSV. Therefore, it is necessary to obtain a balance point between cost and performance. In this letter, we propose H-cluster that applies a hybrid vertical interconnect scheme. It minimizes the number of TSV by sharing vertical links through vertical routers. The simulation results shows that the H-cluster can improve the yield of many-cores chip and provide a better performance.

Keywords: network-on-chip, many-cores, TSV

Classification: Integrated circuits

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1 Introduction

Muti-core chips with tens of cores plays an increasingly important role in big data processing. Network-on-chip (NoC) has emerged as a promising paradigm for the
design of multi-core chips. With the development of data processing, many-core chips with hundreds of cores will appear in the future. However, with hundreds of cores integrated in a single chip, the performance of system is again hindered by wire delay and power consumption due to the longer average distance between cores. 3D Integrated Circuit (3D IC) that stacks multiple silicon dies is emerging as a promising solution to overcome the limitations in the degree of integration. 3D NoC, a combination of 3D IC and NoC, is the best choice for the design of many-core chips.

2D mesh is known for its regular structure and short wire. From this structure, a variety of 3D topologies can be derived. The straightforward extension of this popular planar structure is 3D mesh by adding two additional ports to each router [1]. However, it does not exploit the negligible inter-layer distance and the router significantly increases the overhead of the area and power. Stacked mesh is a hybrid between a packet-switched network and a bus which takes advantage of the short inter-layer distance and requires router [1]. Whereas concurrent communication in the third dimension is prohibited by bus, contention and blocking may increase critically in a high network load.

2 Motivations

Choosing vertical interconnect method is a key process in the design of 3D NoC since both the manufacturing cost and network performance rely heavily on the amount of through silicon via (TSV). The more TSV applied, the better performance 3D NoCs get. Unfortunately, the manufacturing cost of 3D NoC grows exponentially with the increase of TSV number owning to the immaturity [2]. For 3D many-core chips the severe economic penalty brought by the low yield of TSV must be considered seriously. Hence, it’s necessary to find an efficient vertical interconnection method to reduce the number of TSV but ensure the excellent performance of 3D NoC.

Vertical interconnect serialization technique is proposed as one way to minimize the number of TSV [3]. But it increases the complexity and area of router because of the converters between parallel and serial mode. The squeezing scheme is proposed to minimize the amount of TSV by applying sharing logics between current and destination layers [4]. The packets have to reserve all of the TSV sharing logics for inter-layer communication.

3 H-cluster

To hit a right balance between cost and performance, hybrid cluster (H-cluster) is proposed in this letter. It applies a hybrid vertical interconnection method to reduce the number of TSV by sharing vertical links among routers.

3.1 Topology

Unlike 3D mesh in which all routers are connected with up/down routers by abundant TSV. The proposed H-cluster reduces the amount of TSV by sharing vertical link (VL). Router applied in H-cluster is a hybrid of horizontal router (HR) and vertical router (VR). To get a balance of cost and efficiency of vertical
communication, three vertical routers: VR1, VR2 and VR3 are applied in a basic cluster. The coordinate of router is labelled as \( (T, X, Y, Z) \), \( T \) is the type of router (0 for HR, 1 for VR1, 2 for VR2, 3 for VR3) while \( X, Y \) and \( Z \) is the position of router in \( x, y \) and \( z \) dimension. Four horizontal routers and three vertical routers compose a basic cluster as shown in Fig. 1(a). \( X \) and \( Y \) coordinates of VR use the minimum coordinates of HRs in the same cluster. Horizontal routers \( (0, i, j, z) \), \( (0, i + 1, j, z) \), \( (0, i, j + 1, z) \) and \( (0, i + 1, j + 1, z) \) are connected to the central vertical routers \( (1, i, j, z), (2, i, j, z) \) and \( (3, i, j, z) \) through planar links, respectively (\( i \) and \( j \) are even number). Moreover, horizontal routers are connected to each other like a mesh.

H-cluster extends in terms of mesh on the plane. Fig. 1(b) shows the layout of H-cluster in a single layer. It’s composed by \( m \times n \) basic clusters. Horizontal routers on the same row or column are connected to each other through planar links forming a \( m \times n \) H-mesh. Then VR1s on the same row or column are connected to each other forming an \( \frac{m}{2} \times \frac{n}{2} \) sub-mesh1. Similarly, VR2s and VR3s located in different clusters forming an \( \frac{m}{2} \times \frac{n}{4} \) sub-mesh2 and sub-mesh3, respectively.

Vertical link is a hybrid of TSV1, TSV2 and TSV3. TSV1 is utilized to link the same planar position VR1s located in two adjacent layers, i.e., \( (1, i, j, z) \) and \( (1, i, j, z \pm 1) \), while TSV2 is utilized to link the same planar position VR2s located in every other layers, i.e., \( (2, i, j, z) \) and \( (2, i, j, z \pm 2) \). And TSV3 is utilized to link the same planar position VR3s located in every two layers, i.e., \( (3, i, j, z) \) and \( (3, i, j, z \pm 3) \). The vertical connection is based on the value of absolute difference \( V_{ad} \) of two different layers. If \( V_{ad} \) is less than 3, the two layers are connected by TSV1, TSV2 and TSV3 directly. When \( V_{ad} \) is greater than 3, there is no direct connection between two layers but the combination of TSV1, TSV2 and TSV3. Fig. 1(c) shows a \( 4 \times 4 \times 5 \) H-cluster. Compared with 3D mesh, H-cluster eliminates the amount of TSV greatly by sharing the vertical links. An apparent benefit is the increase in yield.

Both horizontal router and vertical router applied in H-cluster are classic virtual channel router, which consisting of input port, routing logic module, virtual channel allocator, switch allocator and crossbar. Horizontal router connect with two intellectual property (IP) cores, neighboring horizontal routers and central vertical routers in the same cluster, while vertical router connect with horizontal routers located in the same cluster and vertical routers have same \( X \) or \( Y \) coordinate with it.
The difference between them in architecture are port number and crossbar degree: horizontal router is $9 \times 9$ router and has a $9 \times 9$ crossbar while vertical router is $10 \times 10$ router and has a $10 \times 10$ crossbar.

3.2 Routing algorithm

Routing in H-cluster can be divided into two parts: intra layer and inter layer. XY routing is used to route packet in the same layer. Since only vertical routers are connected to TSV, inter-layer communication should be realized by vertical routers. Packet should be sent to proper vertical router according to $V_{ad}$ between source layer and destination layer first. If $V_{ad}$ is 1, packet will be sent to VR1. If $V_{ad}$ is 2, packet will be sent to VR2. If $V_{ad}$ is equal 3, packet will be sent to VR3. When packets arrive at vertical router they are sent to the destination layer through the TSV. If $V_{ad}$ is greater than 3, packet will be first sent to the next two layer through VR3. Then if $V_{ad}$ between current layer and destination layer is equal or greater than 3 still, packet will be sent to the next two layers through VR3 again. Otherwise, the packet will be sent to the proper vertical router according to $V_{ad}$ between current layer and destination layer through one of HRs connected with VR3. In destination layer packet will be delivered in sub-mesh until to the vertical router which connected with destination router. Finally, packet will be delivered to destination IP core through horizontal router. Fig. 2 shows the pseudo-code of routing for H-cluster.

![Fig. 2. The routing algorithm for H-cluster.](image-url)
4 Simulation results

We build a cycle-accurate network simulator with OPNET to evaluate the manufacturing cost and performance of NoCs in scale of 128 cores (16\(\times\)8 for 2D mesh, 8\(\times\)4\(\times\)4 for 3D mesh and stacked mesh, 4\(\times\)4\(\times\)4 for H-cluster) and 256 cores (16\(\times\)16 for 2D mesh, 8\(\times\)8\(\times\)4 for 3D mesh and stacked mesh, 4\(\times\)8\(\times\)4 for H-cluster). Energy and area parameters are obtained from the simulator Orion [5].

4.1 Costs comparison

H-cluster is proposed to improve the yield of chip by reducing the number of TSV. We first analyze the yield relationship between chip and TSV. Fig. 3(a) shows the yield relationship between 3D chip and TSV. Due to the reason that the height of TSV variations of point-to-point link and bus are equal, the amount of TSV is the only important factor contributes to the yield of a TSV bundle. Therefore, the yield of chip can be obtained from the equation: 

\[ Y_C = Y_b^{N_b(N_l-1)} \]

where \(Y_C\) means the yield of chip, \(Y_b = Y_{TSV}^{N_l} \) [6] means the yield of TSV bundle, \(Y_{TSV}\) means the yield of TSV, \(N_b\) means the number of TSV bundle in each layer and \(N_l\) means the number of layers. It is evident that the improvement in the chip yield brought by...
reducing the number of TSV is notable for the reason that the yield of TSV is the only considered factor. The amount of TSV will be a huge impact factor of 3D NoC until the yield of TSV is higher than 99.99%.

To be fair we also analyze the other costs of chips including power and area. Fig. 3(b) shows the comparison of power and area, chip area consists of router, link, and TSV pad which can get from equation: 

$$A_{pad} = \frac{p^2 \times N_{TSV}}{C^2} \quad [7],$$

where \(A_{pad}\) is the area of TSV pad, \(p\) which is obtained from TSV height variation means the pitch of TSV and \(N_{TSV}\) is the amount of TSV in a TSV bundle. The result shows the area of H-cluster has a 32.73% rise compared with 3D mesh. The main reason is that routers applied in H-cluster have more ports than that in other topologies although the overhead of TSV pad has a reduction and the number of routers applied in H-cluster is lesser. Since the power consumed by \(9 \times 9\) router is approximately two times than that of \(7 \times 7\) router, the power of Hmesh grows by 32.8% compared to 3D mesh.

4.2 Performance comparison

Fig. 3(c)–(f) show end-to-end (ETE) delay under uniform and hotspot traffic pattern in the scale of 128 and 256 IP cores. For the scale of 128 cores, the saturation points of H-cluster gain an improvement of 35% and 40% of 3D mesh under uniform traffic pattern and hotspot traffic pattern, respectively. For the scale of 256 cores, the saturation points of H-cluster gain an improvement of 17% and 14% of 3D mesh under uniform traffic pattern and hotspot traffic pattern, respectively. The ETE delay performance improvement is mainly brought by the hybrid vertical link that makes a minimum hop communication between any layers is possible.

5 Conclusion

In this letter, H-cluster is proposed to reduce the amount of TSV by sharing the hybrid vertical links. It not only reduces the number of TSV, but also enables inter-layer communication with the minimum hop count. The simulation results show that H-cluster can improve the yield of many-cores chip and has a much better performance. Moreover, H-cluster is of good performance in extension, hence it is flexible to enlarge the scale of network to hundreds even thousands cores.

Acknowledgments

This work is supported partly by the National Science Foundation of China under Grant No. 61472300 and 61334003, Shenzhen Research Funding No. JCYJ20130401171935815, the 111 Project under Grant No. B08038.