Static and Dynamic Oxide-Trapped-Charge-Induced Variability in Nanoscale CMOS Circuits

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Abstract—The inter-device mismatch and intra-device temporal instability in the nanoscale CMOS circuits is examined from a unified point of view as a static and dynamic parts of the variability concerned with stochastic oxide charge trapping and de-trapping. This approach has been benchmarked on the recent evidence of the radiation-induced increase of inter-transistor mismatch in 60 nm ICs. A possible reliability limitation in ultrascale circuits concerned with the single or a few charged defect instability is pointed out and estimated.

Index Terms—Variability, CMOS, MOSFET, oxide traps, Random Telegraph Noise, 1/f noise, mismatch, total ionizing dose

I. INTRODUCTION

Mature technologies rely upon production of identical copies of some basic components. For example, the digital CMOS technology is based on replication of a large number of preferably identical copies of the MOSFETs. The MOSFET’s typical drain current is approximately invariant under the constant aspect ratio size shrinking. This fundamental physical property of 2D devices has provided an opportunity for the aggressive geometrical scaling with an improvement of performance. As the feature size of microelectronic chips is reducing, the variability of electronic components has become a very significant issue for contemporary chips [1, 2, 3]. The major source of static variability is due to the discrete nature of the charged impurities in the devices. For example, the variation in the number and position of the dopant atoms underneath the MOSFET’s gates makes each transistor different, introducing device-to-device statistical spread in the device’s parameters. Particularly, the random dopant fluctuations in the depletion region of the bulk MOSFETs are the cause of mismatch in their threshold voltage [1]. Modern highly-scaled digital circuits have rather low noise margins and the threshold voltage mismatch could seriously degrade their functionality especially for the ultra-low-power systems, operating in the subthreshold mode [4]. The maximum clock speeds have saturated at < 5GHz partly because of the variance of FETs and circuits at < 40 nm [5].

In contrast to the static inter-transistor variability, the intratransistor dynamic variability is closely related with the time-dependent drain current fluctuations due to the trapping/de-trapping of carriers in the gate dielectrics. The near-interfacial (“border”) traps are responsible for such fluctuations over wide temporal ranges. The impact of the low-frequency and random telegraph noise on the dynamic variability of a single SRAM cell is examined in [6, 7]. The ionizing irradiation is able to significantly enhance the device variability due to the buildup of the random charged defects in the isolation oxides and at the Si-SiO₂ interface. Different aspects of such radiation-induced variability have been discussed in [8, 9, 10, 11]. Gerardin et al. investigated experimentally in [12] the interrelations between inter-device static variability and the total dose effects in commercial 65-nm CMOS technology.

The aim of this paper is to consider all these effects from a unified physical point of view.

II. MODEL FORMULATION

A. Screening of external oxide charge

The external oxide charge is screened by the image charges in the channel, substrate and the gate. For the charge \( \delta Q_{ox} \), trapped near the silicon (we will denote the total charges and capacitances by the capitalized indices), we have a shift of the surface potential \( \varphi_s \) at a fixed gate voltage \( V_g \)

\[
\delta \varphi_s = \frac{\delta Q_{ox}}{C_{ox} + C_D + C_{irr} + C_Q}
\]

where \( C_{ox} \) is the gate oxide capacitance, \( C_D = dQ_D / d\varphi_s \) is the depletion layer capacitance, \( C_{irr} \) is the interface trap capacitance, \( C_Q = dQ_{inv} / d\varphi_s \) is the inversion layer (‘quantum’) capacitance [13]. Due to a strong dependence of \( Q_{inv} \) on the surface potential \( \varphi_s \) in the subthreshold region, the \( C_Q \) does not practically affect the silicon FET gate capacitance

\[
C_{inv} = \left[ C_{inv}^{-1} + \left( \frac{C_D + C_{irr} + C_Q}{C_{ox}} \right)^{-1} \right]^{-1}
\]

(see the inset in Fig. 1), since it is extremely low in the subthreshold operation mode (\( C_Q \ll C_D \)) and very high in the above threshold strong inversion regime (\( C_Q \gg C_D \)). Under such circumstances, the quantum capacitance could be well estimated in practice in a non-degenerate approximation [14]

\[
C_Q \approx \frac{Q_{inv}}{2\varphi_T} \left( 1 + \frac{Q_{inv}}{Q_C + Q_D} \right),
\]

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where \( \varphi_i = kT / q \) is the thermal potential, \( Q_C, Q_D \) are the total charge in the inversion and depletion layers respectively. Provided a weak dependence of the carrier’s mobility on \( V_G \), the inverse logarithmic slope can be calculated as a function of the relevant capacitances and the channel charge in the following way

\[
S = \left. \frac{dV_G}{dI_D} \right|_{Q_C} = \frac{Q_C}{dQ_C/d\varphi_S} \frac{dV_G}{d\varphi_S} = \varphi_D \left( 1 + \frac{C_D + C_{IT} + C_Q}{C_{OX}} \right) = \varphi_D \left( 1 + \frac{C_D + C_{IT}}{C_{OX}} \right) + \frac{Q_C}{C_{OX}},
\]

where the diffusion potential \( \varphi_D \) is defined and could be estimated as follows

\[
\varphi_D = \frac{Q_C}{dQ_C/d\varphi_S} = \frac{Q_C}{C_{OX}} \approx 2\varphi_i \left( 1 + \frac{Q_D}{Q_C + Q_D} \right)^{-1}.
\]

As can be seen in (3) an absolute value of \( \varphi_D \) is important only in the subthreshold mode, where \( \varphi_D \approx \varphi_i \).

It is instructive to consider \( S \) in two limiting cases. First, in the subthreshold region \( (Q_C << Q_D) \) it corresponds to the well-known subthreshold slope measured in Volts per decade of gate voltage

\[
SS = S \ln 10 = \varphi_i \ln 10 \left[ 1 + (C_D + C_{IT})/C_{OX} \right] = m \varphi_i \ln 10,
\]

where \( m \) is often referred to as an ideality factor. Second, in the strong inversion region, we have \( S \approx Q_C/C_{OX} \propto V_G - V_T \).

The inverse logarithmic slope \( S \) is closely related with the transconductance \( g_m = dI_D/dV_G \)

\[
S = I_D (dV_G/dI_D) = I_D / g_m.
\]

Fig. 1 shows the physical meaning of \( S \) and illustrates its interrelation with \( g_m \).

![Fig. 1. Field-effect transistor transfer characteristics and graphical representation of the transconductance \( g_m \) and the inverse logarithmic slope \( S \).](image)

Thus defined logarithmic slope describes in a unified way both the strong inversion and the weak inversion regions. In contrast to the extensive transconductance (i.e., dependent on \( W/L \)), the inverse logarithmic slope \( S \) is a thermodynamically intensive variable, i.e., independent of the channel size and shape.

The quantum capacitance \( C_Q \) determines the channel charge fluctuation \( \delta Q_C = C_Q \delta \varphi_S \) in all operation modes. Using (1)-(4), one could obtain a general relation

\[
\frac{\delta Q_C}{Q_C} \approx \frac{\delta \varphi_S}{\varphi_S} = \frac{\delta Q_{OX}}{Q_{OX}} S
\]

where \( Q_{OX} \) and \( Q_C \) are the variances of the oxide and the channel charge fluctuations, and \( varV_T = varQ_{OX}/C_{OX}^2 \) is the variance of the threshold voltage \( V_T \). This result can be used for analysis of the static and the dynamic kinds of the oxide-trapped-induce variability in nanoscale MOSFETs.

### III. MISMATCH AS STATIC VARIABILITY

#### A. Static variability of the threshold voltage

Equation (8) allows describing the sample-to-sample static drain current fluctuations for all MOSFET’s operational modes. Actually, taking into account (8), one gets

\[
\frac{var I_D}{I_D^2} \approx \frac{var Q_C}{Q_C^2} = \frac{var V_T}{S^2} = \frac{g_m^2 var V_T}{I_D^2},
\]

where the threshold voltage variance is assumed to be distributed by a set of transistors. For the above threshold mode \( (V_G > V_T) \) we have \( S \approx Q_{OX}/C_{OX} \propto V_G - V_T \) and typically low levels of the drain current inter-device mismatch \( var I_D/I_D^2 \ll var V_T/(V_G - V_T)^2 \ll 1 \), while the subthreshold mode \( (V_G < V_T) \) corresponds to \( S \approx \varphi_i m \), that could provide a wide drain current spread \( \delta I_D/I_D > 1 \).

The variations of the threshold voltage \( u_r \) around their mean values \( V_T \) are normally described in MOSFETs by the Gauss distribution

\[
P_{\varphi_T}(u_r) = \frac{1}{\sqrt{2 \pi var V_T}} \exp \left( -\frac{(u_r - V_T)^2}{2 var V_T} \right).
\]

The threshold voltage variance \( var V_T \) can be calculated summing up presumably independent terms, corresponding to the dopant atoms in the silicon substrate and to the radiation-induced charged traps in the oxide.
where \( \var{Q_ox} \) and \( \var{Q_{ox}} \) are the variances of the random dopant amount (RDF) and the charged oxide trap numbers.

Since the variance equals the average for the Poisson distribution, the dopant charge fluctuation can be written as \( \langle \var{Q_{ox}} \rangle = q \var{Q_ox} \) and then we have an expression for the RDF part of the threshold voltage variance

\[
\var{V_{r}}^{\text{RDF}} = \frac{q \var{Q_ox}}{C_{ox}} \left( \frac{4 \var{\varphi_\var{T}} \varepsilon_\var{ox} \varepsilon_\var{in}}{q} \right)^{1/2} \frac{t_{ox}^2}{W L},
\]

(12)

where \( N_d \) is a doping level of the p-Si substrate, \( \var{\varphi_\var{T}} = \var{\varphi_\var{f}} \ln N_d/n_i \) is the bulk Fermi potential, \( n_i \) is the intrinsic concentration, \( \varepsilon_\var{ox} \) and \( t_{ox} \) are the gate insulator’s permittivity and thickness. The RDFs are significantly suppressed in modern 3D FET configurations and typically unaffected by impacts of ionizing irradiation, hot electrons or other non-equilibrium external influences.

The charge trapping in the oxide is a stochastic factor concerned with an impact of ionizing radiation, single event radiation effects in space, or in other hazardous environments. The threshold voltage shift under irradiation is determined by the net oxide charge

\[
\Delta V_T = \left( \frac{Q_{ox}^+ - Q_{ox}^-}{C_{ox}} \right) \var{Q_{ox}},
\]

(13)

where \( Q_{ox}^+ \) (\( Q_{ox}^- \)) is an effective amount of the positive (negative) charge trapped near the Si-SiO\(_2\) interface. The positive radiation-induced oxide-trapped charge is often (especially under the low dose rate irradiation) strongly compensated due to the tunnel relaxation and/or interface trap buildup in n-MOSFETs [15]. The very thin gate oxides also make \( \Delta V_T \) negligible even at rather high doses. At the same time, the variance of the oxide charge number is not by a net charge but by a sum of the charged defects with different signs \( \var{Q_{ox}} = q \left( Q_{ox}^+ + Q_{ox}^- \right) = q^2 N_{ox} \). Then we have

\[
\var{V_{r}} = \var{Q_{ox}} / C_{ox} = q^2 N_{ox} / C_{ox},
\]

(14)

Thus, the ionizing radiation may have a little effect on the average I-V characteristics of modern MOSFETs, greatly increasing at the same time the spread of their parameters.

B. Lognormal current distribution in subthreshold modes

The drain current in the subthreshold region (\( V_g < V_T \)) of MOSFET with a random threshold voltage \( u_T \) is well described by a simple exponential approximation

\[
i_D(u_T) \approx I_T \exp \left( \frac{V_g - u_T}{S} \right),
\]

(15)

where the subthreshold slope is expressed via a constant ideality factor \( S \equiv m \var{\varphi_\var{T}} \). The Gaussian (normal) distribution of the threshold voltages (10) in this mode is transformed into a lognormal distribution of the subthreshold drain currents

\[
P_i(i_D) = P_T \left( V_T(i_D) \right) \frac{dV_T}{di_D} = \frac{m \var{\varphi_\var{T}}}{\sqrt{2\pi} \var{V_T} \var{I_D}} \exp \left( \frac{-\var{V_T} \ln^2 (i_D/\var{I_D})}{2m^2 \var{\varphi_\var{T}^2}} \right),
\]

(16)

where \( T_p \) is a median parameter of the lognormal distribution, corresponding to a mean threshold voltage \( \var{I_D} = I_T \exp \left[ (V_g - V_T)/m \var{\varphi_\var{T}} \right] \). The subthreshold drain current averaged over an ensemble of \( N \) transistors with the scattered threshold voltages [16] can be calculated as an averaged over a lognormal distribution

\[
\langle i_D \rangle = N^{-1} \sum_{i=1}^{N} i_D^i P_i(i_D) \, di_D = T_p \exp \left( \frac{m \var{I_D}}{2m^2 \var{\varphi_\var{T}^2}} \right).
\]

Fig. 2 shows the shapes of current distribution calculated at a fixed current with different values of \( \var{V_T} \).

![Image](https://via.placeholder.com/150)

**Drain current, A**

Fig. 2. Drain current distributions \( P_i(i_D) \) calculated at a fixed \( T_p = \) \( 3 \times 10^{-7} \) A (\( W/L=120 \, \text{nm}/60 \, \text{nm}, \quad N_d = 10^{15} \, \text{cm}^{-2} \)) at (a) \( N_{ox} = 0 \); (b) \( N_{ox} = 10^{22} \, \text{cm}^{-2} \); (a) \( N_{ox} = 2 \times 10^{19} \, \text{cm}^{-3} \). A feasible shift of the threshold voltage is set to be zero.

Strictly speaking, the applicability of the Gaussian and lognormal distributions is valid only for the large area devices. To take into account a discrete nature of the trapped charge, one has to average the drain current over Poisson’s distributions with the expected numbers for the trapped charge of both signs \( Q_{ox}^+ = q \langle n \rangle \).

\[
\langle i_D \rangle = I_T e^{-m \var{\varphi_\var{T}} \sum_{n=0}^{N_{ox}} \frac{\left( \begin{array}{c} N_{ox} \\ n \end{array} \right) \left( \begin{array}{c} \langle n \rangle - n \\ m \end{array} \right)}{n!} e^{-m \var{\varphi_\var{T}}} \exp \left( \frac{q \langle n - m \rangle}{C_{ox} m \var{\varphi_\var{T}}} \right) = \left( \frac{N_{ox}^{n_{ox}}}{q} \right) \left( \frac{e^{e_{m \var{\varphi_\var{T}}}} - 1}{e^{e_{m \var{\varphi_\var{T}}} - 1}} \right)
\]

(18)

Expanding an exponent in powers of \( q/C_{ox}m \var{\varphi_\var{T}} \) (typically \( \ll 1 \)) to a square term, one gets the result

\[
\langle i_D \rangle = I_T e^{m \var{\varphi_\var{T}}} \left[ \frac{Q_{ox}^- - Q_{ox}^+}{m \var{\varphi_\var{T}}} \right] + \frac{q (Q_{ox}^+ + Q_{ox}^-)}{2m^2 \var{\varphi_\var{T}^2}},
\]

(19)

that, in view of \( V_T = V_{T_0} - (Q_{ox}^+ - Q_{ox}^-)/C_{ox} \), is essentially the same as (17). The average drain current exceeds the median.
value due to the current distribution in the subthreshold region is skewed to the right at a sufficiently large \( \text{var} V_T \). This means that a relatively small portion of transistors with negatively shifted \( V_T \) provides a significant contribution to average current because of strong dependence of drain current on \( V_G \) in the subthreshold region.

**C. Numerical simulation of inter-device fluctuations of static drain currents**

Characterization of the drain current variability can be generally addressed as the ratio of the standard deviation to the mean current \( \left( \langle I_D^2 \rangle - \langle I_D \rangle^2 \right)^{1/2} / \langle I_D \rangle \), calculated via a straightforward averaging of the I-V characteristics. We have numerically simulated the drain current variance at any operation mode using a general formula

\[
\text{var} I_D(V_G) = \int I_D^2(V_G - u_T) P_T(u_T) du_T - \left[ \int I_D(V_G - u_T) P_T(u_T) du_T \right]^2,
\]

where the threshold voltage variance can be specified for different channel sizes, doping levels, and oxide-trapped charges. Such approach requires an analytical dependence of the drain current on gate and drain biases for all operation modes. We use in this case the compact MOSFET model, described in [17]. Figure 3 shows the standard deviation to the mean value drain current ratio simulated as functions of the gate voltage. The amplitudes of the current standard deviations are significantly larger in the subthreshold operation modes due to lesser values of the inverse logarithmic slope \( S \) in (8).

![Fig. 3. The drain current standard deviation to mean values simulated as functions of gate voltage at different oxide trap concentrations \( N_{\text{ox}} \): (a) \( 10^5 \) cm\(^{-2}\), (b) \( 3 \times 10^5 \) cm\(^{-2}\), (c) \( 10^6 \) cm\(^{-2}\) for a 60 nm nFET \( \varphi_i = 3 \text{ nm, W/L=120 nm/60 nm, } V_T = 0.7 \text{ V, } N_{\text{ox}} = 3 \times 10^5 \text{ cm}^{-2}\).](image)

The normalized standard deviation of the on-current (at \( V_G = V_{DD} \)) has to be an increasing function of \( N_{\text{ox}} \). This is illustrated by the simulation results in Fig. 4.

For the low oxide charge density, the relative current fluctuations are constant due to the dominance of the RDF in (11). The height of the plateau in Fig. 4 is determined by \( \text{var} V_T^{RDF} \) in (12). A noticeable increase in the drain current fluctuations at large \( N_{\text{ox}} \) is caused by fluctuations of the oxide charge \( \text{var} V_T^{\text{ox}} \).

![Fig. 4. The standard deviation to mean values of on-current \( (V_G = V_{DD} = 1.2 \text{ V}) \) simulated as functions of trap concentration \( N_{\text{ox}} \) at different sizes (a) \( W/L=60 \text{ nm/60 nm} \) (b) \( W/L=120 \text{ nm/60 nm} \) (c) \( W/L=240 \text{ nm/60 nm} \) for the same nFET as in Fig. 3.](image)

Thus, ionization may cause additional inter-device threshold voltage mismatch. The trapped charge compensation could strongly suppress the net threshold voltage shift making it sublinear or negligible for contemporary nanoscale circuits with the thin gate oxides. At the same time, the total density of the charged oxide traps \( N_{ox} = N_{ox}^+ + N_{ox}^- \) could be considered as a function approximately proportional to the total ionizing dose. Particularly, the dose dependence of the relative drain current fluctuations, measured for the 120/60 nm nMOSFETs (see Fig. 6 in Ref. [12]), is almost identical with the curve (b) in Fig. 4, intentionally simulated with the authentic transistor’s parameters. Evidently, the severity of this problem would increase with a shrinking of transistor sizes.

**IV. DYNAMIC VARIABILITY**

**A. Dynamic variability**

Dynamic variability can be considered as a form of dynamic mismatch. Actually, the oxide-trapped charged is not fixed due to carrier exchange with the silicon substrate. Following the changes in the Fermi energy position at the Si-SiO\(_2\) interface, the near-interfacial charged defects could change their occupation number (trapping/de-trapping), contributing both to the interface trap capacitance and the threshold voltage instability [18, 19, 20].

The trap response times have a very wide range and delayed kinetics. The auto-correlator of the dynamical threshold voltage can be derived for uniformly distributed traps in approximation of a stationary temporal process [21, 22]

\[
K_{\tau_T}(\Delta \tau) = \langle \delta V_T(0) \delta V_T(\Delta \tau) \rangle = \frac{\text{var} Q_{\tau_T} \lambda}{C_{\text{ox}}} \frac{1}{\ell} \left( E_1 \left( \frac{\Delta \tau}{\tau_{\text{max}}} \right) - E_1 \left( \frac{\Delta \tau}{\tau_{\text{min}}} \right) \right),
\]

where \( \text{var} Q_{\tau_T} \) is the variance of total number of the traps \( Q \), recharged per gate voltage sweep averaged over all temporal scales, \( E_1(y) \) is the integral exponent function \( E_1(y) = -0.577 - \ln y \) at \( y \ll 1 \), the maximum and minimum times of the tunneling recharging are related as \( \tau_{\text{max}} = \tau_{\text{min}} \exp(\ell / \lambda) \), \( \ell \) is a thickness of the trap location.
near the Si-SiO₂ interface (typically, a few nanometers), $\lambda$ is the tunnel attenuation length ($\leq 0.1$ nm).

The quasi-static interface trap capacitance $C_{IT}$ and the trap energy density $D_{IT}$ are defined as follows:

$$C_{IT} = -qdQ_{OX}/d\phi_T = q^2D_{IT}. \quad (22)$$

The total variance $\operatorname{var}(Q)$ at a single voltage sweep can be estimated as

$$\operatorname{var}(Q) = q\bar{C}_{IT} \Delta \phi_T, \quad (23)$$

where $\Delta \phi_T \equiv \phi_T \ln N_s/n_i$ is a typical interval of the surface potential (or Fermi energy) change under gate sweep, $\bar{C}_{IT}$ is the interface trap capacitance averaged over this interval.

Such a spread in $Q$ could lead to a variety of measured threshold voltages. In contrast to the static mismatch, the dynamical variability of threshold voltages essentially depends on the sweep time $t_s$. All the high-frequency fluctuations are self-averaging over time scales less than $t_s$. Given $t_s \ll \tau_{max}$ equation (21) takes an asymptotic form

$$K(t_s) \equiv q\bar{C}_{IT} \Delta \phi_T \left(1 - \frac{\lambda}{\ell} \ln \frac{t_s}{t_r}\right), \quad (24)$$

where $t_r$ is the reference time scale. We found in [21] that $t_r$, $\bar{C}_{IT}$ and $\ell$ are not independent parameters, and they can be consistently recalculated with a renormalization procedure depending on the experimental conditions.

Actually, as it was experimentally found in [19, 23], the dynamic standard deviation of the threshold voltage approximately logarithmically decreases with increase in the sweep time $t_s$. Such single device dynamic variability could be added to the static mismatch contribution and could amount up to $\pm 30\%$ of static variability sources. The lack of dynamic stability in the nanoscale memory circuits can lead to read/write failures or power supply limitations.

B. Flicker noise

The 1/$f$, or flicker noise and the random telegraph noise belong to a class of intra-device variability defined as time-dependent fluctuations of the drain current around its fixed average value. In fact, the flicker noise is due to the same processes as dynamical variability. Indeed, in view of (9) and (21), we derived with the McWhorter model [24] the current auto-correlation noise function

$$S_{I_D} (\Delta t) = \frac{qC_{IT} \left(\phi_T \Delta t\right)}{C_{OX} S^2} \left(1 - \frac{\lambda}{\ell} \ln \frac{t_s}{t_r}\right)\left(E_1 (\Delta t/\tau_{max}) - E_1 (\Delta t/\tau_{min})\right), \quad (25)$$

where the dispersion of trapped oxide charge is controlled by the interface (border) trap energy density at a fixed Fermi level $C_{IT} (\phi_T)$ [25]. According to the Wiener-Khinchine theorem, the power spectral density is defined by a cosine-transform of the auto-correlation function

$$S_{I_D} (\omega) = \frac{4\int_{-\infty}^{\infty} S_{I_D} (t) \cos (\omega t) dt}{T_D^2} = \frac{4qC_{IT} \left(\phi_T \Delta t\right) \tan^{-1}\left(\omega \tau_{max}\right) - \tan^{-1}\left(\omega \tau_{min}\right)}{C_{OX} S^2} \frac{1}{\ell} \ln \left(\frac{\tau_{max}}{\tau_{min}}\right), \quad (26)$$

It is worth to note that the thermal relaxation time constants can have a huge scatter in magnitude also due to a spread in the activation energy $E_{max} > E > E_{min}$, $\tau \approx e^{E/E_{min}} / e^{E/E_{max}}$. The mathematical structure of the response function for the tunnel ("horizontal") and the thermal ("vertical") relaxation for the traps, uniformly distributed in position and energy, is equivalent each other up to a substitution $k_B T / (E_{max} - E_{min}) \leftrightarrow \lambda/\ell \leftrightarrow \ln \left(\frac{\tau_{max}}{\tau_{min}}\right) [21]$. It is well known that the 1/ frequency noise is a superposition of the Random Telegraph Noise (RTN) originating from the trapping/de-trapping of the separate defects [26]. Besides, the Negative Bias Temperature Instability (NBTI) is found to be caused by the same reasons [27, 28, 29].

C. Ultimately scaled circuits

The stochastic oxide-trapped charge could have a huge impact on the reliability of the ultimately scaled circuit. The drive current in transistors of contemporary technologies can be estimated as follows

$$I_D = \frac{Q_0}{L} V_{max} \quad (27)$$

where $V_{max}$ is the maximum carrier speed ($\sim 10^7$ cm). Then the relative current fluctuation is given by

$$\frac{\delta I_D}{I_D} = \frac{\delta Q_{OX}}{C_{OX} S} \approx \frac{\delta Q_{OX}}{C_{OX} (V_G - V_T)}, \quad V_G > V_T, \quad \frac{\delta Q_{OX}}{m \phi_T}, \quad V_G < V_T. \quad (28)$$

For transistors with 10nm×10nm sizes, the total channel charge comprises of several electrons even at maximum gate voltages. The trapping/de-trapping process even in a single defect ($\delta Q_{OX} \geq q$) could lead in this case to a noticeable variation in drive current of such transistors. These fluctuations become critical on the condition $\delta Q_{OX} \approx q - C_{OX} S$. The critical channel area for strong inversion can be estimated via the equivalent oxide thickness (EOT) as follows

$$A_{crit} \sim \frac{q}{C_{ox} (V_{DD} - V_T)} = \frac{q \text{ EOT}}{e_{ox} (V_{DD} - V_T)}. \quad (29)$$

Taking $V_{DD} - V_T = 0.5$ V and EOT = 1 nm, one gets $A_{crit} \approx 9$ nm$^2$. In the subthreshold region the impact of an individual charged oxide trap should be noticeable even for modern 10 nm technology

$$A_{crit} \sim \frac{q \text{ EOT}}{e_{ox} \phi_T} = 180 \text{ nm}^2. \quad (30)$$
We claim in this way that $A_{\text{crit}} \sim 10 \text{ nm}^2$ is the ultimately minimal channel area, limited by unavoidable variability due to stochastic charge instability of a single defect in surrounding insulators.

V. SUMMARY

The static and dynamic variability, flicker noise and RTN in nanoscale CMOS has been treated in this work from a single standpoint. A distinctive general feature of all these effects is the Pelgrom’s dependence $\propto \frac{1}{\sqrt{WL}}$ for the standard deviation of the amplitude [30]. This dependence is a direct consequence of the Poisson statistics for the charged defects distributed without correlations on the transistor’s channel area $A = WL$. For the channel area less than approximately 10 nm$^2$ the static and dynamic variability effects may become unacceptably large due to the fluctuations may be comparable with the average values. The advanced technologies (e.g., FinFETs, or, FD SOI FETs) allow excluding or minimizing the RDF effect, but no technology can prevent the emergence of several unstable defects in even a very thin surrounding insulator. This issue represents a fundamental limit on the reliability of the ultra-scale devices and circuits.
