Interfacial Band Engineering of MoS$_2$/Gold Interfaces Using Pyrimidine-Containing Self-Assembled Monolayers: Toward Contact-Resistance-Free Bottom-Contacts

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Bottom-contact architectures with common electrode materials such as gold are crucial for the integration of 2D semiconductors into existing device concepts. The high contact resistance to gold—especially for bottom contacts—is, however, a general problem in 2D semiconductor thin-film transistors. Pyrimidine-containing self-assembled monolayers on gold electrodes are investigated for tuning the electrode work functions in order to minimize that contact resistance. Their frequently ignored asymmetric and bias-dependent nature is recorded by Kelvin probe force microscopy through a direct mapping of the potential drop across the channel during device operation. A reduction of the contact resistances exceeding two orders of magnitude is achieved via a suitable self-assembled monolayer, which vastly improves the overall device performance.

Schottky and tunneling barriers between commonly employed electrode materials and 2D semiconductors give rise to high contact resistances, which deteriorate device performance. In order to gain access to the full potential that 2D semiconductors have to offer, a reliable and scalable contact engineering method needs to be established, especially for low-power and GHz range operation and for flexible and wearable electronics applications.

Many different approaches have been utilized to address the issue of high contact resistances, in particular for MoS$_2$ as a prototypical model system. Low work function (WF) metals were employed to achieve a better match between the metal Fermi level and the conduction band of MoS$_2$. Reduced contact resistances were also reported after thermal annealing. High-temperature annealing is, however, not always possible, especially when submicrometer channels and ultrathin gate dielectrics are used, or when thin film transistors (TFTs) are realized on polymer-based substrates.

Graphene contacts to MoS$_2$ result in reduced carrier-injection barriers compared to commonly used metals, while the atomically sharp and clean interfaces prevent detrimental Fermi-level pinning and lower the tunneling barrier. Moreover, graphene has been employed as an interfacial layer between MoS$_2$ and metals. Hexagonal boron nitride was also used as a tunneling layer between electrodes and MoS$_2$, offering the benefits of a smooth and clean interface. It also triggers the formation of two dipole layers (between the metal electrode and hBN and between hBN and MoS$_2$), which lowers the injection barrier. Incorporation of another 2D material between MoS$_2$ and electrodes, however, generally involves an additional transfer step and can suffer from low yields. As a high-yield alternative, selective chemical functionalization of MoS$_2$ by thiol molecules has been proposed.

All of the above-mentioned approaches are almost exclusively developed for top-contact architectures, while MoS$_2$ has rarely been integrated into TFTs using bottom contacts, with most of the reported examples realized with graphene electrodes. This is unfortunate, as using prepatterned transistor-substrates containing bottom-contact structures significantly simplifies...
the device-fabrication procedure and, thus, allows for a straightforward integration of 2D semiconductors into established technologies.

Implementing self-assembled monolayers (SAMs) to modify surface properties of electrodes has been demonstrated in organic electronics.\(^\text{[20–26]}\) The SAM formation process is scalable and fully compatible with flexible substrates.\(^\text{[20]}\) By a proper choice of the molecules, their anchoring, and their functional groups it is possible to fine-tune the electrode’s WF.\(^\text{[21–26]}\) Although the implementation of SAMs in organic electronics is well-understood, there is a lack of knowledge transfer to the field of 2D materials. This would, however, be highly attractive, as devices based on 2D semiconductors have already demonstrated GHz operation speeds, which is much more challenging to achieve in organic or metal-oxide TFETs.\(^\text{[3]}\)

The devices employed in this study constitute of gold (Au) source and drain electrodes with channel lengths of \(\approx 10\) \(\mu\)m, and aluminum bottom-gates with \(\text{Al}_2\text{O}_3\) gate dielectrics (see Figure 1a). This architecture allows low operation voltages due to the particularly small thickness (18 nm) of the gate dielectric, which is also crucial for simultaneously performing electrical and Kelvin probe force microscopy (KPFM) measurements. MoS\(_2\) flakes were prepared by micromechanical exfoliation. Selected single-crystalline flakes were aligned with the transistor-substrates such that only one flake bridges the source and drain pads.\(^\text{[11]}\) A step-by-step fabrication scheme is provided in Figure S1 (Supporting Information). 3–10 nm thick multilayer MoS\(_2\) flakes (4–14 layers; see also Figure S2, Supporting Information) were selected since in this thickness range only small flake-to-flake variations of the electron affinity are expected.\(^\text{[3]}\) Further, within the selected thickness range, the dependence of carrier mobility on thickness in the MoS\(_2\)-TFTs is much less pronounced\(^\text{[3]}\) and the mechanical robustness of the flakes is enhanced (compared to monolayers) allowing easier sample handling and higher transfer yield. Moreover, multilayer flakes are less sensitive to their environment than monolayers. This makes them particularly well suited for the present study, where the SAMs are used to change the electronic properties of the electrodes (especially their work functions) rather than to chemically alter the MoS\(_2\) layers.\(^\text{[17]}\) For more details on the suitability of multilayer MoS\(_2\), see Section S2 (Supporting Information).

As carrier layer for the transfer, either the tape commonly used for exfoliation with acrylic-based adhesives (Nitto) or polydimethylsiloxane (PDMS) films were employed. In most experiments, the carrier layers remained on the device for encapsulation. For KPFM measurements, the transfer layers were peeled off, leaving the top surface of the flake accessible.

WF engineering of Au electrodes was carried out prior to the transfer of MoS\(_2\) by functionalization with aromatic SAMs. The SAM-forming molecules covalently anchor to the top-most gold atoms via a thiolate group, and the resulting SAM is sufficiently robust for allowing ambient exposure and MoS\(_2\) transfer without compromising its functionality. A SAM backbone introduces a small tunneling barrier between Au and MoS\(_2\), but the impact of this barrier can be minimized by avoiding aliphatic spacers in the SAM-forming molecule and by keeping the aromatic backbones short.\(^\text{[26,27]}\) The SAMs employed here exactly follow that design principle. In the parent SAM, the backbone consists of biphenyl; by substituting one of the phenyl-rings with a pyrimidine, a permanent dipole is embedded, which points along the long axis of the molecule and whose orientation can be

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**Figure 1.** a) Schematic cross-section of the device indicating the thickness of the relevant layers and optical micrograph of a MoS\(_2\)-TFT without encapsulation. b-top) WF range of SAM-treated electrodes compared to the electron affinity range of MoS\(_2\) flakes assuming vacuum-level alignment (values taken from Refs. \([3,26]\)). b-bottom) Chemical structure of the three SAM-forming molecules; red arrows indicate the direction of the dipole. c–f) Typical output characteristics of MoS\(_2\)-TFTs with bare, as well as BP0-down, BP0, and BP0-up covered Au electrodes. To enable a direct comparison of the transistors, \(I_D\) values were scaled with the transistors’ lengths (L) and widths (W). Solid (dashed) lines represent forward (backward) sweeps. Dotted straight lines and red arrows in (c,d) highlight the “S”-shape of the output characteristics.
controlled by the arrangement of the pyrimidine (see Figure 1b). The dipoles in the SAM pointing downward (upward) cause a WF increase (decrease) with respect to the dipole-free SAM-treated electrodes.[26,27] Overall, four different electrode treatments were tested: O₂ + H₂ plasma treated gold without SAMs as a reference, as well as 2-phenylpyrimidine-3-thiol (BP0-down), biphenyl-thiol (BP0), and 4-(2-mercaptophenyl)pyrimidine (BP0-up) treated Au electrodes. The expected WF range for the SAM-treated Au electrodes[26,27] is presented in Figure 1b. Assuming vacuum-level alignment and an electron affinity of MoS₂ between 4.2 and 4.6 eV[3] either BP0 or BP0-up should provide suitable band alignment with a low Schottky barrier. Notably, the exact magnitude of the electron affinity of MoS₂ depends on both, the layer number and possible doping of a particular flake. BP0-down SAMs serve as “negative example” to highlight the importance of the Schottky barrier between the electrodes and the MoS₂ layer for device operation.

Typical electrical output characteristics (\(I_D(V_{SD})\)) of MoS₂-TFTs are presented in Figure 1c–f. A clear “S” shape of the output characteristics at lower \(V_{SD}\) is observed, both for the bare Au reference and BP0-down treated electrodes (red arrows). This indicates a large Schottky barrier at the carrier injection point (grounded source electrode).[28] In order to extract ohmic and nonlinear components of the contact resistances, a fitting approach—as described in Refs.[26,29]—was applied to the sets of electrical output and transfer characteristics for the devices presented in Figure 1c–f. This fitting approach allows for a direct comparison to contact resistances obtained by KPFM, and provides data comparable to the transfer line method (TLM).[26,29] The details on the fitting of electrical characteristics and their relation to TLM are provided in Section S3 (Supporting Information). A hysteresis between forward and backward sweeps (Figure 1d) was observed in the case of Nitto-tape encapsulated devices, with more details provided in Section S4 (Supporting Information). Besides output characteristics, transfer curves (\(I_D(V_{SG})\)) and extracted apparent linear electron mobilities (\(\mu_{lin}(V_{SG})\)) are presented in Figures S5 and S6 (Supporting Information). An aging experiment (in an Ar glovebox) is presented in Figure S7 (Supporting Information).

A detailed analysis of the transfer characteristics was conducted to extract performance parameters of MoS₂-TFTs (see Figure 2). The scatter in the data mainly results from flake-to-flake variations in width, thickness, and doping, originating from the exfoliation process. Figure 2a presents the ON/OFF ratios as a function of electrode treatment, taken from transfer curves at \(V_{SD} = 1\) V as: \(I_D(V_{on}+2}\) \(V)/I_D(V_{on})\), where \(V_{on}\) represents the turn-on voltage. BP0 or BP0-up SAMs increase the ON/OFF ratio by over one order of magnitude compared to BP0-down and over two orders of magnitude compared to the Au-reference. Flank-width scaled ON/OFF ratios and ON-state \(I_D\)’s are provided in Figure S8 (Supporting Information).

The corresponding apparent linear mobility (\(\mu_{lin}\)) values (obtained employing the gradual channel approximation without explicitly considering the contact resistance) are presented in Figure 2b. \(\mu_{lin}\) values were taken at a specific operation point: \(V_{SD} = 0.2\) V; \(V_{SG} = V_{on}+0.5\) V (for \(\mu_{lin}(V_{SG})\) see Figure S5, Supporting Information). The highest apparent mobility values (between 78 and 11.6 cm² V⁻¹ s⁻¹) were obtained for BP0-down treated electrodes, while devices containing reference Au and BP0-down treated electrodes exhibit \(\mu_{lin} < 1\) cm² V⁻¹ s⁻¹.

Besides the impact on device-hysteresis (Figure S4, Supporting Information), the choice of the top encapsulation layer of the device primarily affects the turn-on voltages (Figure 2c), which were extracted from the transfer characteristics (at \(V_{SD} = 0.2\) V) as the source-gate voltage, \(V_{SG}\), at which \(I_D\) starts to continuously rise above the gate-leakage current. For both, PDMS and air/Ar, \(V_{on}\) values near \(V_{SG} = -1\) V indicate low levels of unintentional doping. PDMS does not induce significant charge transfer doping of MoS₂ and preserves its intrinsic doping levels. Interestingly, with Nitto tape encapsulation, \(V_{on}\) shifts below \(V_{SG} = -5\) V. The fact that mobilities and ON/OFF ratios remain unaffected, points toward

Figure 2. a,b) ON/OFF ratio (logarithmic plot) and apparent linear mobility (\(\mu_{lin}\)) as a function of the electrode treatment. c) \(V_{on}\) as a function of the MoS₂ encapsulation layer. Each point represents a different device, presenting a total of 24 MoS₂-TFTs.
charge transfer doping\cite{30} from the acrylic-based adhesive to the MoS$_2$ flake. Threshold voltage engineering in MoS$_2$-TFTs has already been demonstrated via molecular doping or SAM-functionalization of the MoS$_2$\cite{31,32} modifications of the gate-dielectric surface\cite{33} or using ferroelectrics\cite{34}.

To directly measure the potential drops across the channels, KPFM measurements have been performed in organic-, graphene-, and MoS$_2$-TFTs\cite{35-38}. Here, we employed KPFM during device operation to obtain contact resistances at well-defined points of operation of our devices. Contact potential difference (CPD) profiles ($V_{\text{CPD}}$) across both electrodes and the active area of the device were recorded at each of these points of operation, while recording transfer and output characteristics. The $V_{\text{CPD}}$ profiles were then normalized\cite{36} (further technical details are provided in Figures S9–S13, Supporting Information). For the Au-reference and BP0-down treated samples, asymmetric $V_{\text{CPD}}$ profiles were observed (Figure 3a,b). Most of the applied potential drops at the source ($V_S$) as a result of a high injection barrier. Changing the direction of the applied bias results in a similarly high voltage drop at the other electrode (Figure S12, Supporting Information). For BP0-treated electrodes (Figure 3c), the applied bias drops mainly across the channel ($V_{\text{ch}}$), exhibiting almost negligible contact resistances, supporting the notion mentioned above that BP0 SAMs are ideally suited for realizing bottom-contact MoS$_2$ TFTs. For BP0-up treated electrodes (Figure 3d), $V_S$ and the potential drop at the drain contact ($V_D$) are asymmetric for the chosen operation conditions. This is insofar surprising, as the WF of BP0-up SAM covered contacts is expected to be resonant with or even smaller than the electron affinity of MoS$_2$ (where the latter in thermodynamic equilibrium ought to trigger interfacial charge transfer processes). Notably, the contact resistances for BP0-up SAMs also display a nonlinearly bias-dependent component, as discussed in Section S13 of the Supporting Information (c.f., Figure S13, Supporting Information). This points to more complex interfacial processes governing the properties of this particular interface.

Additional features—like wrinkles—occasionally introduced during the transfer, become apparent only in cases with low contact resistances. As shown in Figure 3c, changes in the slope of $V_{\text{CPD}}$ across the channel coincide with positions of the wrinkles. Considering all samples, where it was possible to observe $V_{\text{CPD}}$ drops that correspond to wrinkles, the width-scaled resistance of the wrinkles was estimated to be 20–40 $\Omega$ cm. Similar topographical features are also shown in Figure 3a. However, due to the much smaller values of $I_0$ the associated potential drops could not be observed.

In Figure 3e, the observed potential drops were converted to width-scaled resistance values for better comparison, where relative contributions of the injection ($R_S$) and extraction electrodes ($R_D$) are presented (note the logarithmic scale). The contact resistance drops by two orders of magnitude between BP0-down

![Figure 3. a–d) Typical $V_{\text{CPD}}$ profiles (solid lines) across the channel for the different electrode treatments at $V_{\text{SD}} = 0.5$ V; $V_{\text{SG}} = V_{\text{on}} + 3$ V. The measured drain currents are also provided. The arrows right of the graphs indicate, how the total potential applied between source and drain is split into drops at the source, across the channel, and at the drain, $V_S$, $V_{\text{ch}}$, and $V_D$. Dotted lines in (a–d) present topography cross-sections, where channel-electrode steps are $\approx$50 nm. Shaded areas mark the electrodes. e) Logarithmic plot of the width-scaled contact resistances obtained from (a–d). Black circles with horizontal lines in (e) represent the values extracted by fitting the electrical output and transfer characteristics of the devices shown in Figure 1c–f, and in (Figure S3, Supporting Information). Bars without black circles refer to situations with fitted contact resistance values that are lower than the plotting range of panel (e).](image-url)
and BP0 treated electrodes and by almost three orders of magnitude when comparing Au-reference devices and devices containing BP0-treated electrodes. The lowest contact resistance values observed are on the order of 10 Ω cm, i.e., comparable to top-contact architectures.[1,14] Black circles with horizontal lines in Figure 3e represent the width-scaled contact resistances obtained from the device characteristics with the above-described fitting procedure (see also Section S3, Supporting Information). They are reported for the same point of operation used for the KPFM measurements. The fitting analysis fully corroborates the distinction between large, mostly nonohmic resistances for Au and BP0-down treated contacts and profoundly reduced resistances for BP0 and BP0-up treated contacts. The differences between the contact resistances (especially in the BP0 case) obtained by the fitting approach and those measured by KPFM fall within the observed sample-to-sample variation (see also Figure 2). All \( W \cdot R_{SD} \) values obtained by the fitting approach are listed in Table S1 (Supporting Information).

In summary, minimization of contact resistances between Au bottom-contacts and MoS\(_2\) was demonstrated via electrode engineering employing dipolar SAMs. For the best matching SAMs, a reduction of the contact resistance exceeding two orders of magnitude was achieved compared to bare Au reference electrodes. This increases the ON/OFF ratio of the transistors by over two orders of magnitude and the apparent linear mobility by more than one order of magnitude. KPFM measurements during device operation—and independently the fitting of the electrical characteristics—revealed nonohmic contribution to contact resistances, highlighting the influence of the SAM-treatment on the reduction of the injection barrier. The proposed concept of SAM-based electrode modification is fully scalable, allowing a reliable integration of 2D semiconductors into bottom-contact architectures, while avoiding high-temperature annealing. It allows the realization of low contact resistance values (\( \approx 10 \) Ω cm) comparable even to carefully engineered top-contact devices.[1,14]

**Experimental Section**

**Transistor Substrates:** Transistor substrates were fabricated in a bottom-gate, bottom-contact architecture following the process-flow illustrated in Figure S1 (Supporting Information).

**SAM Treatment:** SAM treatment was done by immersion of freshly prepared samples into 100–500 × 10\(^{-6}\) m ethanol (\( \approx 99.9 \% \), HPLC grade, VWR) solutions, for 18–72 h. Subsequently, the samples were rinsed several times with the pure solvent and dried in \( N_2 \) flow. Longer immersion times improved adhesion of MoS\(_2\) however, for immersions longer than 72 h, a roughening of the surface suggested the formation of molecular clusters. Data on surface energies (from contact angle measurements) and high-resolution X-ray photoelectron spectroscopy of SAM-treated Au electrode surfaces can be found in Refs. [26,27]. The XP spectra testify to the integrity of the films and the bonding of the thiols to the Au surface.[27] They also provide in-depth insight into the electronic structure of the SAMs.[26] The surface energies for BP0-down and BP0 SAMs are virtually identical (\( \approx 44 \) mJ m\(^{-2}\)), while the surface energy of BP0-up is somewhat larger (\( \approx 57 \) mJ m\(^{-2}\)).[26] This is primarily a consequence of a larger polar component of the surface energy, which is expected, as in BPO-up SAMs the polar bonds around the N-atoms in the pyrimidine ring are closer to the surface. Further, contact angle measurements, comparing reference to BP0-treated Au and Al\(_2\)O\(_3\) surfaces are provided in Section S14 and Table S2 (Supporting Information).

**Supporting Information**

Supporting Information is available from the Wiley Online Library or from the author.

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**Conflict of Interest**

The authors declare no conflict of interest.
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MoS$_2$, thin-film transistors, Schottky barrier, self-assembled monolayers, work-function engineering

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