A Thermodynamic Perspective of Negative-capacitance Field-effect-transistors

Sou-Chi Chang, Uygar E. Avci, Dmitri E. Nikonov Senior Member, IEEE, and Ian A. Young Fellow, IEEE

Abstract—Physical phenomena underlying operation of ferroelectric field-effect transistors (FeFETs) is treated within a unified simulation framework. The framework incorporates the Landau mean-field treatment of free energy of a ferroelectric and the polarization dynamics according to Landau-Khalatnikov (LK) equation. These equations are self-consistently solved with the one-dimensional metal-oxide-semiconductor (MOS) structure electrostatics and the drift-diffusion solution for the current in the semiconductor channel. Numerical simulations demonstrate, depending on the ferroelectric (FE) thickness, both regimes of hysteresis switching (relevant for a non-volatile memory) and of higher on-currents and steeper subthreshold slope (SS) with a negligible hysteresis (relevant for logic) via the negative capacitance effect.

Index Terms—ferroelectric field-effect transistor (FeFETs), logic, memory, negative capacitance, depolarization field

I. INTRODUCTION

Over the past four decades, the computing power of microprocessors has been exponentially increasing thanks to the relentless pursuit of Moore’s law, stating that the number of transistors in an integrated circuit has doubled approximately every two years [1]. However, as the complementary metal-oxide-semiconductor (CMOS) technology is scaled to single nanometer sizes, the static power component becomes approximately every two years [1]. However, as the complementary metal-oxide-semiconductor (CMOS) technology is scaled to single nanometer sizes, the static power component becomes increasingly dominant share of total energy dissipation due to the reduction of the on-off current ratio (I\textsubscript{on}/I\textsubscript{off}) in CMOS transistors [2]. It has been well known that the high on-off current ratio can be achieved by minimizing the subthreshold swing of a transistor, which is defined as

\[
SS = \left( \frac{\partial \psi_s}{\partial V_g} \frac{\partial \log_{10} I_{ds}}{\partial \psi_s} \right)^{-1},
\]

where \(\psi_s\) and \(V_g\) are the surface potential of the transistor’s channel and the gate voltage, respectively, and \(I_{ds}\) is the source-to-drain current. In the expression of SS,

\[
E_s = \frac{\partial \psi_s}{\partial V_g}
\]

\[
C_s = \frac{\partial \log_{10} I_{ds}}{\partial \psi_s} - \frac{E_s}{T}
\]

are the factors related to the electrostatic control in a MOS capacitor and the amount of current that can be provided by the channel’s band structure, respectively. In CMOS transistors, the upper limit of \(E_s\) is 1 because the gate voltage has to be dropped in each layer of the stack - the high-k dielectric, SiO\textsubscript{2} under-layer, and semiconductor channel. The upper limit of \(C_s\) is typically 2.3\(\frac{k_B T}{e}\) since the transport mechanism in the subthreshold region is dominated by thermionic emission of carriers from the source terminal. As a consequence, the minimum of SS that can be achieved in a CMOS transistor is \(~ 60\text{mV/dec} at room temperature.

To drive SS below 60\text{mV/dec} at room temperature, tunnel field-effect transistors (TFETs) have been proposed to improve \(C_s\) by changing the channel conduction mechanism from diffusive transport to quantum-mechanical tunneling [3], [4], [5]. Nevertheless, there are still several issues associated with TFETs such as low on currents, relatively complicated process flow, and needs for circuit schematics modifications. On the other hand, recently achieving \(E_s > 1\) has been extensively explored by several research groups by way of the negative capacitance (NC) effect of the ferroelectric (FE). In these devices, known as NCFETs [6], the only required modification is replacing high-k dielectric (DE) with the FE oxide. The main idea of NCFETs can be understood in a fairly simple way as follows. For a gate with the ferroelectric layer, the channel structure factor can be expressed as

\[
E_s = \left( 1 + \frac{C_{\text{semi}}}{C_{\text{ox}}} \right)^{-1},
\]

where \(C_{\text{semi}}\) and \(C_{\text{ox}}\) are the capacitors associated with semiconductor and gate oxide, respectively. Then it is possible to have \(E_s > 1\) if \(C_{\text{ox}}\) becomes negative.

Over the past few years, NC in the FE has been under extensive discussion [6], [7], [8], [9], [10]. Some groups claimed that NC originates from the down-pointing curvature of energy barrier between two stable polarization states in the thermodynamic free energy profile and can be directly measured during polarization reversals in a FE capacitor [6], [7]. Others argued that NC observed during polarization reversals is a pure electrostatic effect, rather than thermodynamic one [10]. As will be explained in details below, observing NC directly in a single FE capacitor is actually prohibited by laws of thermodynamics; however, NC effects in the FE do result from the negative curvature of energy barrier and can still be deduced from the enhancement of overall capacitance as a FE capacitor is in series with other capacitors.

In addition to the promise of the NC effect to improve \(I_{on}/I_{off}\) ratio of logic transistors, it also has been well known that a pronounced shift in the threshold voltage (\(\Delta V_{th}\)) can be achieved by incorporating the FE into the gate stack [11]. In this case the current-voltage characteristics exhibits a hysteresis. Such an unique property makes FeFETs a promising candidate for memory applications due to its non-destructive read, fast read and write operation, and non-volatility [11].

S. -C. Chang, U. E. Avci, D. E. Nikonov, and I. A. Young are with Components Research, Intel Corporation, Hillsboro, OR 97124, USA.
[12]. As a result, it is of importance to have a clear picture for the underlying physics behind FeFETs for both memory and logic operation regimes. Unlike previous works focusing solely on the particular application: (i.e., presuming that initially FeFETs are in the NC regions [6], [13], [14], [15] or a clear hysteresis loops are established in FE oxides [16]), this paper does not assume any particular operation region initially and provides a unified picture of how FeFET operation transitions from memory to logic devices due to the change of thermodynamic free energy profiles. This picture is verified by numerical simulations incorporating MOS electrostatics and polarization dynamics self-consistently.

The rest of this paper is organized as follows. In Sec. II, capacitance enhancement using FE NC effects in series capacitors is demonstrated. Also the importance of the double-well free energy profile to memory devices is illustrated. Next, in Sec. III, a theoretical model describing both charge and current-voltage characteristics in FeFETs is presented in detail. Section IV shows the numerical results to support the key features observed from the free energy profiles and points out some issues that need to be addressed in FeFETs for both logic and memory applications in the future. Conclusions are formulated in Section V.

II. THERMODYNAMIC FREE ENERGY IN CAPACITORS

In this section, charge distribution in several capacitors-in-series systems is determined from thermodynamic free energy point of view. We start from two DE capacitors in series to show the results from free energy aspect are consistent with those from the conventional circuit theory. Next a concept of super capacitor implemented by FE and DE capacitors in series is introduced using their free energy profiles. Finally, similarly to super capacitors, a superior MOS capacitor can be achieved by forming a FE thin film on top of a conventional MOS capacitor. As the FE thickness varies, a capacitor may or may not have the hysteresis effects. These two regimes are important in memory and logic applications.

A. Two dielectric capacitors in series

When two DE capacitors are connected in series, the total free energy of the system, $U_{tot}$, can be written as

$$U_{tot} = U_1 + U_2 + U_V,$$

where $U_1 = \frac{Q^2}{2C_1}$ and $U_2 = \frac{Q^2}{2C_2}$ are the energies stored in each capacitor, respectively, and $U_V = -QV$ is the energy due to the applied voltage, $V$. $Q$ is the free charge on metallic plates, and $C_1$ and $C_2$ are capacitance of the two capacitors. In equilibrium ($V = 0$), if we express $U_{tot}$ in terms of free energy and total capacitance, $C_{tot}$, Eq. (5) becomes

$$\frac{Q^2}{2C_{tot}} = \frac{Q^2}{2C_1} + \frac{Q^2}{2C_2}.$$
From Eq. 6, it can be seen that the inverse of total capacitance for two capacitors in series is simply equal to the sum over the inverse of that for each capacitor. That is, \( \frac{1}{C_{\text{tot}}} = \frac{1}{C_{\text{FE}}} + \frac{1}{C_{\text{DE}}} \), which is consistent with the well-known circuit theory result.

With voltage applied, the total energy becomes

\[
U_{\text{tot}} = \frac{Q^2}{2C_{\text{tot}}} - QV, \tag{7}
\]

In Eq. 7 the steady-state charge \( Q \) at a given voltage can be found via the extreme condition \( \frac{\partial U_{\text{tot}}}{\partial Q} = 0 \). This results in \( Q = C_{\text{tot}}V \) which is also consistent with the circuit theory. Consequently, the total energy for series capacitors is simply the sum over the free energy of individual components.

### B. Ferroelectric and dielectric capacitors in series

As a capacitor is fabricated by depositing a FE thin film on top of a DE layer, its total energy is similar to the previous case

\[
U_{\text{tot}} = U_{\text{FE}} + U_{\text{DE}} + U_V, \tag{8}
\]

where

\[
U_{\text{FE}} = t_{\text{FE}} \left( \alpha_1 Q^2 + \alpha_{111} Q^4 + \alpha_{1111} Q^6 \right) \tag{9}
\]

is the free energy of a FE layer under the single-domain approximation \( [17] \). \( U_{\text{DE}} = \frac{Q^2}{2C_{\text{DE}}} \) is the free energy of a DE layer, and \( U_V = -QV \) is the free energy due to the applied voltage. Note that \( U_{\text{FE}} \) here is expressed assuming that \( Q = \epsilon_0 E_{\text{FE}} + P \approx P \) with \( \epsilon_0 \) being the vacuum dielectric constant, \( E_{\text{FE}} \) being the electric field across a FE thin film, and \( P \) being the FE polarization. In the following results for free energies, lead zirconate titanate (PZT) and SiO\(_2\) are used as example FE and DE materials to illustrate the conceptual idea, and the corresponding parameters are given in Table. I. In equilibrium (\( V = 0 \)), the free energy profiles for each component are shown in Fig. (b), where no charge is accumulated on either DE or DE-FE capacitors. That is, the minima of free energy are located at zero charge.

If we focus on the curvatures near the minima of free energy profiles, it can be seen that the DE-FE capacitor has larger capacitance compared to the regular DE as obvious from the definition \( C = \left( \frac{\partial^2 U}{\partial Q^2} \right)^{-1} \). When the same voltage is applied to both capacitors, as shown in Fig. (c), it can be seen that larger charge is induced in a DE-FE capacitor. This can be alternatively understood either as a smaller curvature near the free energy minimum of a DE-FE capacitor or as the global free energy minimum located at a larger value of charge. As a result, a better capacitor (or super capacitor) can be achieved by simply adding a FE layer on top of a regular DE capacitor or having a FE capacitor with inevitable dead layers as discussed by several previous works [18], [19], [20], [21]. Note that the idea of a super capacitor works only when...
the total free energy profile has only one global minimum. That is, the dominant component in the overall system is still the DE and not the FE layer. Therefore as the FE thickness is increased, the total free energy profile get a more double-well-like shape as shown in Fig. 1(d), hysteresis effects start showing up in DE-FE capacitors.

C. Ferroelectric and metal-oxide-semiconductor capacitors in series

Similar to the concept of a super capacitor mentioned above, it is also possible to achieve a superior MOS capacitor by having a FE thin film on top of a regular MOS capacitor (FeMOS). As can be seen in Fig. 2(b), the free energy associated with a nonlinear semiconductor capacitor \( U_{\text{semi}} = \frac{Q\psi_s}{2} \) with \( \psi_s \) being the surface potential drop within a semiconductor is now included in the total free energy profile. Here PZT, SiO\(_2\), and Si are used as FE, DE, and semiconductor materials to illustrate the concept. The parameters for SiO\(_2\) and Si can be found in Table. 1. The total free energy of the system is given as

\[
U_{\text{tot}} = U_{\text{FE}} + U_{\text{DE}} + U_{\text{semi}} + U_{V_s},
\]

Near equilibrium \( (V_g \approx 0) \), with a proper FE thickness, it can be seen in Fig. 2(b) that the capacitance of a FeMOS capacitor is greater than that of the regular MOS one. This improvement is mainly due to the global minimum of a FE energy located where the curvature of a FE thin film energy is negative. As a result, at a given gate voltage, more charge can be accumulated on a FeMOS capacitor compared to other capacitors as shown in Fig. 2(c). Hence, a FET structure with a FeMOS capacitor can generate more drain currents if no significant mobility degradation is produced by the FE thin film. This benefits both high-performance and low-power logic applications since it is possible to control the charge boost at different gate-voltage regions. As the FE material becomes thicker, the free energy profile of a FeMOS capacitor starts transforming from one global minimum to double local minima (see Fig. 2(d)), and thus the hysteresis effects become more pronounced. In general, a good memory device can be built based on significant hysteresis effects in FeMOS capacitors [22].

III. Theoretical Model

In this section, we introduce a mathematical model for FeFETs combining 1-D MOS electrostatics (along the gate direction) with FE polarization dynamics to justify the idea we discussed in the previous section. Here we use n-FETs as an example for a proof of concept, though a qualitatively same behavior occurs in p-FETs as well. The FeFET structure simulated below is shown in Fig. 3, where a gate stack is composed of metallic, FE, DE, and p-type semiconducting materials and highly n-doped semiconductors are used for the source and drain. The material parameters are also summarized in Table. 1.

![Fig. 3. Schematic of an n-FeFET structure described by the theoretical model introduced in Sec. III. Along the gate direction, the device is composed of a metal, a FE layer, a DE layer, and a p-type semiconductor. Highly-doped n-type semiconductors are used for the source and drain.](image)

To simulate a FeFET under steady-state conditions which correspond to the local or global minima in free energy profiles, at a given voltage, we start from an initial guess for \( \rho_s \), the free charge density on the metal side. By assuming that the electrical displacement along the gate direction is continuous, the following equations are satisfied.

\[
\rho_s = P = \epsilon_{DE}\epsilon_0E_{DE} = -Q_s,
\]

where \( \epsilon_{DE} \) is the relative dielectric constant of a DE layer, \( E_{DE} \) is the electric field across the DE layer, and \( Q_s \) is the charge in the semiconductor channel. Note that \( Q_s \) can be related to the semiconductor surface potential, \( \psi_s \), through the following equation [23]

\[
Q_s = \pm \sqrt{2\epsilon_{\text{semi}}\epsilon_0 k_B T N_a} \left[ \left( \frac{n_i}{N_a} \right)^2 \left( e^{\frac{e\psi_s}{k_B T}} - \frac{e\psi_s}{k_B T} + 1 \right) \right]^{\frac{1}{2}},
\]

where \( \epsilon_{\text{semi}} \) is the relative dielectric constant of a semiconductor, \( k_B \) is the Boltzmann constant, \( T \) is the temperature, \( N_a \) is the p-type dopant concentration, \( n_i \) is the intrinsic concentration of a semiconductor, and \( e \) is the elementary charge. The ± sign in Eq. 12 represents depletion/inversion or accumulation charge. Since the gate voltage, \( V_G \), has to be shared within a FeMOS capacitor, the electric field across the FE layer, \( E_{FE} \), can be obtained by Eq. 13

\[
E_{FE}t_{FE} = eV_G - (\phi_1 - \phi_2 - E_F - \delta) - E_{DE}t_{DE} \quad \text{and} \quad \psi_s - \frac{\rho_s\lambda_m}{\epsilon_m\epsilon_0},
\]

where \( t_{FE} \) is the FE thickness, \( \phi_1 \) and \( \phi_2 \) are conduction band discontinuities at the metal-FE and DE-semiconductor interfaces, respectively, \( E_F \) is the Fermi energy in the metal, \( \delta = E_F - \mu \) is the energy difference between the conduction band \( (E_c) \) and chemical potential \( (\mu) \) in the semiconductor, \( t_{DE} \) is the DE thickness, \( \lambda_m \) is the screening length of metal, and \( \epsilon_m \) is the dielectric constant of the metal. Note that \( \delta \) is obtained by using the Joyce-Dixon approximation [24] given as.
\[\delta = k_B T \left[ \ln \left( \frac{N_c}{n} \right) - \left( \frac{n}{\sqrt{2}N_c} \right) + \left( \frac{3}{16} - \frac{\sqrt{3}}{9} \right) \left( \frac{n}{N_c} \right)^2 \right], \tag{14}\]

where \(N_c\) is the effective density of states (DOS) in the conduction band given as \(N_c = 2 \left( \frac{2\pi m_e^* k_B T}{h^2} \right)\) with \(m_e^*\) being electron DOS effective mass and \(h\) being Planck constant, and \(n\) being the electron density in a bulk semiconductor. For simplicity, the Boltzmann approximation is assumed for \(n \approx \frac{N_c}{2}\). In Eq. (13) the potential energy drop within the metal is described under the Thomas-Fermi approximation \[25\]. For a given \(E_{FE}\), it is assumed that the FE polarization follows the Landau-Khalatnikov (LK) equation under the single-domain approximation given as \[26\], \[27\], \[28\], \[29\], \[17\].

\[\gamma \frac{\partial P}{\partial t} = -\frac{\partial}{\partial \psi} \left( \alpha_1 P^2 + \alpha_{11} P^4 + \alpha_{111} P^6 \right) - E_{FE} P, \tag{15}\]

with \(\gamma\) being the viscosity coefficient describing how fast the polarization in a FE thin film can follow an external electric field. As discussed in the previous section, the concept of superior MOS capacitors is established based on the state located right at the minimum of free energy profile, which corresponds to the steady-state solutions to the LK equation; that is, \(\frac{\partial P}{\partial t} = 0\). Hence, the iteration between Eqs. (11) to (15) is required to obtain the steady-state quantities such as charge and voltage drop in FeFETs for a given gate voltage, and the charge in a semiconductor channel (or \(\psi_a\)) can be converted into drain currents at a given drain-to-source voltage by using Pao and Sahs integral given as \[23\].

\[I_D = \frac{e \mu_n W}{L} \int V_{DS} \int_{\psi_a}^{\psi_s} \left( \frac{n_i^2}{N_a} \right) e^{-\frac{(\psi_a - \psi_s)}{k_B T}} \frac{\partial \psi \partial V}{E(\psi, V)}, \tag{16}\]

with

\[E(\psi, V) = \sqrt{\frac{2N_a k_B T}{\varepsilon_{Si} \varepsilon_0} \left\{ \left( \frac{n_i}{N_a} \right)^2 \left( e^{\frac{\psi_a - \psi_s}{k_B T}} - 1 \right) + \frac{e^{\psi_s}}{k_B T} + \frac{e^{\psi_a}}{k_B T} - 1 \right\}^{\frac{3}{2}}}, \tag{17}\]

being the channel electric field, \(V_{DS}\) being the voltage across the source and drain terminals, \(\mu_n\) is the effective electron mobility, \(W\) and \(L\) being the channel width and length, respectively, and \(\psi_B\) being an infinitesimal number. Figure 4 summarizes the procedure (flow-chart) to simulate FeFETs. Note that for the simulation results shown in the next section, we also include MOSFETs with high-k gate DE as a baseline (see the parameters in Table 1), and the corresponding changes in the model are simply replacing \(P\) in Eq. (11) with \(\epsilon_{high-k} \varepsilon_0 E_{high-k}\) and that no iteration is required.

### IV. RESULTS AND DISCUSSION

#### A. Steady-state behavior of ferroelectric field-effect-transistors

In this section, first, the theoretical model introduced in the previous section is applied to simulate FeFETs and to justify the concept discussed from the free energy point of view. Without losing the essential physics in FeFETs, in the following simulations, \(\psi_1\) is adjusted such that \(\psi_1 - \psi_2 - E_{FE} - \delta\) makes the off-current (~ \(10^{-10}\) A) for both Fe and high-k FETs occur at about the same gate voltage. Next, the steady-state and transient negative capacitance effects for FeFETs are discussed to provide a better understanding on device operations.

As discussed in Sec. II, the capacitance enhancement in a FeMOS capacitor mainly comes from the fact that the steady state of entire system is close to the negative capacitance.
region of the FE, which implies that the charge induced on the MOS capacitor is opposite to the voltage across the FE or the voltage across the FE is reduced as the gate voltage increases as shown in Figs. 5(a) and (b), respectively. As a result, for a given positive gate voltage, a larger surface potential drop in the semiconductor can be established in FeFETs compared to conventional high-k MOSFETs if the voltage across the FE layer is negative as shown in Fig. 5(c). Note that as the FE thickness is increased, the hysteresis effects in the devices become more pronounced because the overall free energy profiles are more double-well-like as explained previously.

To convert the surface potential to drain currents, we assume electron mobility is not degraded significantly as the FE oxide is deposited on the DE layer; that is, the same mobility is used for all the cases in Fig. 6. Consequently, the current improvements in FeFETs come from the charge boost because of larger capacitance in the FeMOS stack. As shown in Fig. 6(a) depending on the FE thickness, FeFETs can exhibit quite different $L_d$-$V_g$ characteristics and are potentially useful in both logic and memory applications. For thin FE films, a significant boost to on-currents compared to high-k MOSFETs is useful for high performance digital switches. As the FE film gets thicker, a great charge-boost in the subthreshold region appears at the expense of a weak hysteresis effect, which can decrease the gate voltage that is required to drive circuits. If we increase the FE thickness further, due to the double-well free energy profile as shown in Fig. 6(d), a large difference between threshold voltages during forward and backward gate voltage sweeps is created and can be useful in memory designs due to non-destructive readouts [22]. Furthermore, free energy profiles as functions of both charge and gate voltage are shown in Figs. 6(b) and (c). We emphasize again the importance of a single free energy minimum over the entire gate voltage sweep to the hysteresis-free $L_d$-$V_g$ characteristics. In other words, sudden jumps in $L_d$-$V_g$ result from the fact that the negative curvature of free energy profile is not a thermodynamically stable state and thus the polarization switching is required. On the other hand, due to the depolarization field contributed from the DE layer, there is no negative curvature presented in the free energy profile, and therefore no abrupt switching is observed in $L_d$-$V_g$. Note that in real devices, charging defects at the FE/DE interface or within the DE layer due to a strong electric field may significantly reduce charge boost or memory window established by the FE layer [36]. Consequently, having a proper ratio between FE and DE layers not only makes FeFETs work in the correct mode, but also minimizes the unwanted charging effects.

### B. Transient behavior in ferroelectric field-effect-transistors

As discussed previously, NC in FE thin films plays an extremely important role to enhance FeFET logic performance (i.e., charge-boost with no hysteresis). However, this improvement can only be achieved when the device reaches its steady-state condition under a given bias situation; that is, local or global minima located at the FE NC region in the free energy profile. How fast the steady state can be achieved is expressed by the viscosity coefficient ($\gamma$) in the LK equation, which largely depends on both material intrinsic and extrinsic properties such as FE domain wall nucleation and propagation rates as well as on thin film quality [29]. As a result, the charge-boost in FeFETs may be significantly modified as the operation frequency goes too high. To capture this transient behavior correctly, a rigorous material calibration for $\gamma$ to FE switching dynamics is necessary. The effects of different viscosity coefficients on $L_d$-$V_g$ are given in Fig. 7 in which a larger viscosity coefficient implies a slower FE response. Note that for both forward and backward gate voltage sweeps, $1 \mu s$ is given for the polarization dynamics at each gate voltage in this work. As shown in Fig. 7 when the FE response becomes so slow such that the polarization cannot reach its steady state at a given voltage, the hysteresis effects become more significant even though a FE film is thin enough to form a single minimum in the free-energy profile.

Next, we discuss the recent experimental demonstration on transient NC in FE capacitors [7]. Note that the NC measured in such a resistance-capacitance (RC) setup is mainly from electrostatic effects, rather than thermodynamic energy profile. This is because the transient NC response shown in Ref. [7] can be modulated significantly with different series resistance. In other words, the measured NC is simply due to the fact that the polarization switching in the FE is too fast such that the free charge provided from the external circuit cannot follow...
DE as a baseline. The under layer thickness is 0.5nm and the doping density of semiconductor is free energy profiles as functions of both charge and gate voltage for FeFETs with thickness of Fig. 6. (a) Source-to-drain current vs. gate voltage in FeFETs with different FE thicknesses. The red curve with circles shows MOSFETs with 1nm high-k DE as a baseline. The under layer thickness is 0.5nm and the doping density of semiconductor is free energy profiles as functions of both charge and gate voltage for FeFETs with thickness of

![Fig. 6](image)

(b) and (c) show free energy profiles as functions of both charge and gate voltage for FeFETs with thickness of 6nm and 10nm, respectively.

\[ V_{FE} = t_{FE}E_{FE} = t_{FE} \left( \frac{\rho_{ext} - P}{\epsilon_0} \right) , \tag{18} \]

Here \( \rho_{ext} \) is the measured charge, whose frequency response is limited by external RC circuits. From Eq. \( [18] \) when \( \rho_{ext} \) cannot follow to the polarization switching (i.e., \( \rho_{ext} \) is assumed constant unlike \( P \)) the voltage across the FE can be reversed and thus transient NC is observed. Here we argue that this transient NC due to the mismatch between external charge and FE polarization responses cannot lead to an improvement in drain currents. This is mainly because charge in the semiconductor channel, which is proportional to the drain current, has to be always equal and opposite to that on the metal side due to charge neutrality. Note that the transient \( I_{ds} - V_{gs} \) response discussed in Fig. 7 results from the fact that FE polarization cannot reach its global minimum during a given gate voltage pulse, rather than the charge-polarization mismatch mentioned above, and thus a significant change in I-V characteristics can be induced.

V. Conclusion

We have presented a systematic understanding of FeFETs operating as memory and logic components from the thermodynamic point of view. It is shown that, in order to have significant charge boost of channel charge and non-hysteresis behavior in FeFET-based high performance logic, a free energy profile with a single global minimum is required for the gate stack. On the other hand, for useful memory devices, significant \( \Delta V \) in FeFETs can be established by double-well-like free energy profile. Furthermore the transition from a single global to a double local minima in free energy profiles can be achieved by varying the ratio between FE and DE thickness in FeFETs. These FeFET features deduced from thermodynamics are justified by numerical simulations including 1-D MOS electrostatics and FE polarization dynamics, and it is shown that, depending on the ratio between FE and DE thickness, the FeFET can potentially offer (i) higher drive current without hysteresis or steeper subthreshold swing with negligible hysteresis - for digital logic or (ii) significant memory windows - for memory applications. Also, the transient response of FeFETs and the effect on FET performance due to recent direct NC measurements are discussed.

### References

[1] G. E. Moore, “Cramming more components onto integrated circuits,” Proceedings of the IEEE, vol. 86, no. 1, pp. 82–85, Jan 1998.
[2] N. S. Kim, T. Austin, D. Baauw, T. Mudge, K. Flautner, J. S. Hu, M. J. Irwin, M. Kandemir, and V. Narayanan, “Leakage current: Moore’s law meets static power,” Computer, vol. 36, no. 12, pp. 68–75, Dec 2003.
[3] A. S. Grove and D. J. Fitzgerald, “The origin of channel currents associated with pregions in silicon,” IEEE Transactions on Electron Devices, vol. 12, no. 12, pp. 619–626, Dec 1965.
[4] T. N. Theis and P. M. Solomon, “It’s time to reinvent the transistor!” Science, vol. 327, no. 5973, p. 1600, Mar 2010. [Online]. Available: http://science.sciencemag.org/content/327/5973/1600.abstract
[5] A. M. Ionescu and H. Kiel, “Tunnel field-effect transistors as energy-efficient electronic switches,” Nature, vol. 479, no. 7373, pp. 329–337, Nov 2011. [Online]. Available: http://dx.doi.org/10.1038/nature10679
[6] S. Salahuddin and S. Datta, “Use of negative capacitance to provide voltage amplification for low power nanoscale devices,” Nano Letters, vol. 8, no. 2, pp. 405–410, 2008, pMID: 18052402. [Online]. Available: http://dx.doi.org/10.1021/nl801804g
[7] A. I. Khan, K. Chatterjee, B. Wang, S. Drapcho, L. You, C. Serrao, S. R. Bakaull, R. Ramesh, and S. Salahuddin, “Negative capacitance in a ferroelectric capacitor,” Nat Mater, vol. 14, no. 2, pp. 182–186, Feb 2015, letter. [Online]. Available: http://dx.doi.org/10.1038/nmat4148
[8] P. Zubko, J. C. Woidel, M. Hadjimichael, S. Fernandez-Pena, A. Sene, I. Lukyanchuk, J.-M. Triscone, and J. Ignuez, “Negative capacitance in multidomain ferroelectric superlattices,” *Nature*, vol. 534, no. 7608, pp. 524–528, Jun 2016, letter. [Online]. Available: http://dx.doi.org/10.1038/nature17659

[9] C. M. Krowne, S. W. Kirchoefer, W. Chang, J. M. Pond, and L. M. B. Allredge, “Examination of the possibility of negative capacitance using ferroelectric materials in solid state electronic devices,” *Nano Letters*, vol. 11, no. 3, pp. 988–992, Mar 2011. [Online]. Available: http://dx.doi.org/10.1021/nl1037215

[10] G. Catalán, D. Jiménez, and A. Gruverman, “Ferroelectrics: Negative capacitance detected,” *Nat Mater*, vol. 14, no. 2, pp. 137–139, Feb 2015. news and Views. [Online]. Available: http://dx.doi.org/10.1038/nmat4195

[11] S. L. Miller and P. J. McWhorter, “Physics of the ferroelectric nonvolatile memory device, metal-ferroelectric—,” *Analysis and compact modeling of negative capacitance transistor*, *IEEE Transactions on Electron Devices*, vol. 62, no. 12, pp. 5999–6010, 1992. [Online]. Available: http://dx.doi.org/10.1063/1.351910

[12] S.-Y. Wu, “A new ferroelectric memory device, metal-ferroelectric-semiconductor transistor,” *IEEE Transactions on Electron Devices*, vol. 21, no. 8, pp. 499–504, Aug 1974.

[13] H. P. Chen, V. C. Lee, A. Ohoka, J. Xiang, and Y. Taur, “Modeling and design of ferroelectric mosfets,” *IEEE Transactions on Electron Devices*, vol. 58, no. 8, pp. 2401–2405, Aug 2011.

[14] G. Pahwa, T. Dutta, A. Agarwal, S. Khandelwal, S. Salahuddin, C. Hu, and Y. S. Chauhan, “Analysis and compact modeling of negative capacitance transistor with high on-current and negative output differential resistance: part i: Model description,” *IEEE Transactions on Electron Devices*, vol. 63, no. 12, pp. 4918–4925, Dec 2016.

[15] ——, “Analysis and compact modeling of negative capacitance transistor with high on-current and negative output differential resistance; part ii: Model validation,” *IEEE Transactions on Electron Devices*, vol. 63, no. 12, pp. 4986–4992, Dec 2016.

[16] H.-T. Lue, C.-J. Wu, and T.-Y. Tseng, “Device modeling of ferroelectric memory field-effect transistor for the application of ferroelectric random access memory,” *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 50, no. 1, pp. 5–14, Jan 2003.

[17] R. Kretschmer and K. Binder, “Surface effects on phase transitions in ferroelectrics and dipolar magnets,” *Phys. Rev. B*, vol. 20, pp. 1065–1076, Aug 1979. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.20.1065

[18] A. M. Bratkovsky and A. P. Levanyuk, “Very large dielectric response of thin ferroelectric films with the dead layers,” *Phys. Rev. B*, vol. 63, p. 132103, Mar 2001. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.63.132103

[19] P. S. Bratkovsky and A. P. Levanyuk, “Depolarizing field and real hysteresis loops in nanometer-scale ferroelectric films,” *Applied Physics Letters*, vol. 89, no. 5, p. 253108, 2006. [Online]. Available: http://dx.doi.org/10.1063/1.2408650

[20] I. Ponomareva, L. Bellaiche, and R. Resta, “Dielectric anomalies in ferroelectric nanostructures,” *Phys. Rev. Lett.*, vol. 99, p. 227601, Nov 2007. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevLett.99.227601

[21] M. Stengel, D. Vanderbilt, and N. A. Spaldin, “Enhancement of ferroelectricity at metal-oxide interfaces,” *Nat Mater*, vol. 8, no. 5, pp. 392–397, May 2009. [Online]. Available: http://dx.doi.org/10.1038/nmat2429

[22] X. Yin, A. Aziz, J. Nahas, S. Datta, S. Gupta, M. Niemier, and X. S. Hu, “Exploiting ferroelectric fets for low-power non-volatile logic-in-memory circuits,” in *2016 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Nov 2016, pp. 1–6.

[23] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. New York, NY, USA: Cambridge University Press, 1998.

[24] S. C. Chang, S. Manipatruni, D. E. Nikonov, I. A. Young, and A. Naemi, “Design and analysis of si interconnects for all-spin logic,” *IEEE Transactions on Magnetics*, vol. 50, no. 9, pp. 1–13, Sept 2014.

[25] S.-C. Chang, A. Naemi, D. E. Nikonov, and A. Gruverman, “Theoretical approach of the negative capacitance in ferroelectric tunnel junctions,” *Phys. Rev. Applied*, vol. 7, p. 024005, Feb 2017. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevApplied.7.024005

[26] Y. Qi and A. M. Rappe, “Designing ferroelectric field-effect transistors based on the polarization-rotation effect for low operating voltage and fast switching,” *Phys. Rev. Applied*, vol. 4, p. 044014, Oct 2015. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevApplied.4.044014

[27] S. C. Chang, S. Manipatruni, D. E. Nikonov, and I. A. Young, “Clocked domain wall logic using magnetoelectric effects,” *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 2, pp. 1–9, Dec 2016.

[28] Y. Liu, X. Lou, M. Bibes, and B. Dkhil, “Effect of a built-in electric field in asymmetric ferroelectric tunnel junctions,” *Phys. Rev. B*, vol. 88, p. 024106, Jul 2013. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.88.024106

[29] G. Vizirli, S. Ducharme, V. M. Fridkin, and S. G. Yudin, “Kinetics of ferroelectric switching in ultrathin films,” *Phys. Rev. B*, vol. 68, p. 094113, Sep 2003. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.68.094113

[30] A. Aziz, S. Ghosh, S. Datta, and S. K. Gupta, “Physics-based circuit-compatible spce model for ferroelectric transistors,” *IEEE Electron Device Letters*, vol. 37, no. 6, pp. 805–808, June 2016.

[31] B. El-Kareh, *Silicon Devices and Process Integration: Deep Submicron and Nano-Scale Technologies*, 1st ed. Springer Publishing Company, Incorporated, 2009.

[32] M. Salmani-Jelodar, H. Ilatikhameneh, S. Kim, K. Ng, P. Sarangapani, and G. Klimeck, “Optimum high-k oxide for the best performance of ultra-scaled double-gate mosfets,” *IEEE Transactions on Nanotechnology*, vol. 15, no. 6, pp. 904–910, Nov 2016.

[33] F. G. Pikus and K. K. Likharev, “Nanoscale field-effect transistors: An ultimate size analysis,” *Applied Physics Letters*, vol. 71, no. 25, pp. 3661–3663, 1997. [Online]. Available: http://dx.doi.org/10.1063/1.120475