Fabrication of ultrathin poly-crystalline SiGe-on-insulator layer for thermoelectric applications

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Abstract
For realizing high power generator efficiency based on thermoelectricity, Si, Ge and SiGe nanostructures have attracted attention. In this paper, we have investigated a new approach to fabricate an ultrathin polycrystalline SiGe-on-insulator (pc-SGOI) substrate by a simple process based on Si and Ge deposition followed by thermal diffusion suitable for thermoelectric devices. A 45-nm-thick SGOI layer with a Ge fraction of nearly 0.45 was fabricated, and the Ge fraction was homogeneous in plane over the layer. Its thermal conductivity was 0.87 W mK\(^{-1}\), lower than that of a single-crystalline SGOI layer. This is caused by the enhancement of scattering of phonons at grain boundaries in the pc-SGOI layer.

1. Introduction

Si has been attracted considerable attention as one of thermoelectric materials. Si has some advantages such as high purity, inexpensiveness, abundance, and earth-friendliness. Moreover, considering that Si is used for most of sensors and processors under rapid progress of Internet of Things (IoT), the realization of Si-based thermoelectric power generator is of great significance for self-powered devices. From a thermoelectric standpoint, however, it has unfortunately high thermal conductivity while its Seebeck coefficient is desirably large. There are mainly two ways for overcoming this weak point. One is the introduction of nanostructures since they are expected to suppress the thermal conductivity and to enhance the Seebeck coefficient \([1\text{--}9]\). The other is the utilization of Si compounds such as SiGe alloy which is effective for suppressing the thermal conductivity because the scattering rate in phonon transport is promoted by lattice disturbance and strain originating from random arrangement of Si and Ge atoms \([10\text{--}14]\). Of course, the approach of combining the nanostructure with the SiGe alloy has been already reported \([15\text{--}22]\). For example, the thermal conductivity of \(\text{Si}_{1-x}\text{Ge}_x (x = 0.4)\) nanowire with a diameter of 50 nm is theoretically expected to be 1/100 comparing with that of bulk Si \([23]\).

An ultrathin SiGe-on-insulator (SGOI) layer is essential to fabricate the SiGe nanowire by lithographic technology. In the field of ULSI devices, such as a metal-oxide-semiconductor transistor, there are a variety of fabrication methods of single-crystalline SiGe (sc-SiGe) thin film grown on SiO\(_2\)/Si substrates \([24\text{--}32]\). Most of them are difficult and costly since their process is complicated and is not fit for a large-area formation. Remember that the sc-film is not necessarily required for thermoelectric applications. This is because the grain boundary in poly-crystalline material (pc-material) plays a role of a barrier in phonon transport when the grain size is set to be less than the mean-free-path of phonons, which leads to the reduction in thermal conductivity. Although there is another way for fabricating a pc-SGOI layer, such as conversion of a sc-SiGe layer into a pc-SiGe layer using ion implantation, it will require more fabrication process and cost. In the present paper,
therefore, we propose a simple and inexpensive method for fabricating an ultrathin pc-SGOI layer and characterize its crystallographic properties and thermal conductivity.

2. Experimental

A physical vapor evaporation system was constructed for the formation of Ge film, as shown in figure 1. In this system, a turbo molecular pump was used to get high vacuum $2 \times 10^{-7}$ Pa. A power source was used to heat a W boat to evaporate Ge source. A quartz crystal digital thickness monitor (DTM) was set to monitor the film thickness and deposition rate. A substrate holder capable to keep 4 samples of $1 \times 1$ cm$^2$ simultaneously was attached on a rotatable rod to change its direction during Ar$^+$ ion exposure and Ge deposition. An Ar$^+$ ion gun was used to clean the sample surface and to make defects on it. Ge chunk of 99.9999% purity was used as a source material and the deposition time was controlled by a shutter.

To fabricate an ultrathin pc-SGOI layer by a simple process, thermally-oxidized Si($100$) wafer with an oxide layer thickness of 103 nm was used as a substrate, as shown in figure 2. The SiO$_2$/Si substrate was chemically cleaned with the standard piranha solution. The amorphous Si($\alpha$-Si) thin film of 30 nm thick with a deposition rate of 6 nm min$^{-1}$ was formed by using an ECR sputtering system at room temperature. The Si-deposited substrate was then placed in the physical vapor deposition system. We introduced one more step before Ge deposition, which is the etching of the $\alpha$-Si surface by Ar$^+$ ions in vacuum not only for removing the native oxides but also for forming more defects on the surface to enhance the intermixing of Si and Ge atoms. A thin Ge film of 30 nm thick was deposited by physical vapor deposition on the etched $\alpha$-Si layer with a deposition rate of 3 nm min$^{-1}$ at room temperature. The Ge-Si interdiffusion was performed in a thermal annealing system at various heating conditions. After optimizing the annealing temperature, annealing time and heating/cooling rate, the interdiffusion was appropriately carried out at 880 °C for 10 and 120 min with a heating rate of 15 °C s$^{-1}$ and a cooling rate of 0.75 °C s$^{-1}$.

The thickness of Si and Ge thin film was measured by ellipsometry (Mizojiri optical DHA-OLXS). The crystallographic characteristics of prepared SGOI layers were observed by grazing incidence x-ray diffraction (GIXRD) (RINT-Ultima III, CuKα radiation) at an incident angle of 0.5°, with a scan speed of 2° min$^{-1}$ and a sampling step of 0.02°. Raman spectra were obtained using a Raman spectrometer (JASCO NRS-7100) with a green laser excitation with a wavelength of 532.6 nm and a spot size of 1 μm. After annealing process, the thickness of ultrathin SiGe layers was measured by transmission electron microscope (TEM) (JEOL JEM 2100F) with an accelerating voltage of 200 kV. The surface roughness of the film was measured by dynamic force microscopy (DFM) (Seiko Instruments SPI-3800). The in-depth compositional analysis was performed by x-ray photoelectron spectroscopy (XPS) (Shimadzu Axis Ultra DLD) with etching of SiGe layer with Ar$^+$ ions. The Si and Ge compositions were calculated using a ‘vision processing’ software built in the XPS instrument from their peak intensity and area. The chemical composition in plane was measured by field emission electron probe micro-analyzer (EPMA) (JEOL JXA-8530F).

The picosecond time-domain thermoreflectance (TDTR) with a front-heating front-detection method [33, 34] was used to determine the thermal conductivity of prepared samples, where a Mo layer of 100 nm thick was deposited on the SGOI layer by using radio frequency magnetron sputtering to get the reflection of laser from the sample surface. In analyzing the thermal conductivity, the specific heat capacity and the density of both Mo and SiGe layers were taken the same values as those of bulk values. Hall effect measurement (HL-5500 PC,
BIO-RAD was performed to determine the electrical properties of fabricated SiGe layers. The Seebeck coefficient was measured using our handmade measurement system [35], and the electrical conductivity was evaluated from the Hall-effect measurement.

3. Results and discussion

Figure 3 shows the Raman spectra of the fabricated SGOI layers annealed at 880 °C for 10 min and 120 min, together with those after the Si sputtering and the Ge deposition. For comparison, the results for the SiGe layer annealed at 400 °C, 500 °C and 600 °C for 30 min with a heating rate of 10 °C s\(^{-1}\) are also shown in figure 3. In the spectrum of the sputtered Si sample, there are broad peak at 470 cm\(^{-1}\) and sharp peak at 521 cm\(^{-1}\), corresponding to the Si-Si bond in \(\alpha\)-Si film and crystalline-Si (c-Si) substrate, respectively. After Ge deposition, peaks of Ge-Ge atomic vibrations in \(\alpha\)-Ge and c-Ge are observed at 270 cm\(^{-1}\) and 295 cm\(^{-1}\), respectively, and the Si-Si peaks become lower. When we confirmed XRD profile of this sample, there is no significant peak of Ge. Therefore, the deposited Ge film is mainly amorphous and includes a small fraction of c-Ge formed by the heat of the Ge source itself. It is found from the spectra that as increasing annealing temperature up to 600°C, the Ge-Ge peaks gradually decrease, and the Si-Si peaks become larger. Besides there is no peak originating from Si-Ge atomic vibration around 400 cm\(^{-1}\). The spectrum for the 600°C-annealed sample is very similar to that for the as-deposited Si sample. These results strongly suggest that the deposited Ge atoms desorb from the substrate and no mixing of Si and Ge atoms occurs in this temperature range. The similar phenomena were reported by Zhang et al where Ge desorption occurs by annealing above 500°C and then a decrease in Ge composition and the void formation on the SiGe surface were observed [36].

The Raman spectra for the sample annealed at 880 °C have significant peaks related to the Ge–Ge, Si–Ge, and Si–Si bonds at 283, 400, and 483 cm\(^{-1}\), respectively, together with a peak from Si substrate at 521 cm\(^{-1}\). This apparently indicates that the SiGe alloy can be formed by annealing at 880 °C for 10 min and 120 min Figure 4 depicts the XRD profiles before and after thermal interdiffusion process. While the as-deposited Ge/Si sample has only peaks related to the Si substrate in its profile, the profiles of the sample annealed at 880 °C show SiGe peaks at 27.92°, 46.8° and 55.12°, which are respectively close to the positions of (111), (220) and (311) planes expected from Si\(_1-x\)Ge\(_x\) layer. The indices of the SiGe-related peaks and their intensity ratio were in good agreement with the theoretical expectation of particle sample, suggesting the formation of pc-SGOI layer. From the (111) major peak position based on the Vegard’s law [37, 38],

\[
a_{\text{SiGe}} = 5.4309 + 0.20032x + 0.02674x^2, \tag{1}
\]

the lattice constant and the Ge fraction of the prepared SiGe layers are evaluated to be \(a_{\text{SiGe}} = 5.53 \text{ Å}\) and \(x = 0.46\), respectively, assuming that the SiGe layer is fully relaxed owing to the pc-SiGe phase. Although the
density of $\alpha$-Si and $\alpha$-Ge depends on the growth condition, the expected Ge fraction is calculated to be $x = 0.431$ if we use the reported density values, $\rho_{\alpha\text{-Ge}} \sim 4.3 \text{ g cm}^{-3}$ and $\rho_{\alpha\text{-Si}} \sim 2.2 \text{ g cm}^{-3}$ [39–41]. That is, the number of atoms per unit volume for $\alpha$-Ge is smaller than that for $\alpha$-Si, which leads to the Ge fraction below $x = 0.5$ in the case of Ge and Si layers with the same thickness. Based on the Ge composition evaluated from XRD profiles, $x = 0.46$, the Si-Si and Si-Ge peak positions in the Raman spectra were evaluated to be 488 cm$^{-1}$ and 406 cm$^{-1}$, respectively [42, 43]. These values are higher than those observed in the spectra (f) and (g) of figure 3, 483 cm$^{-1}$ and 400 cm$^{-1}$, respectively. The deviation from the expected peak positions is considered to be due to softening by poly-crystallization [37, 42, 43].
From these findings, it can be said that the annealing temperature, 880 °C, just below the melting point of Ge, 937 °C, and the rapid heating rate, 15 °C s⁻¹, play a crucial role to promote the intermixing and the crystallization of Si and Ge atoms before the Ge desorption occurs. Once the Si-Ge bond is formed, the Ge desorption may be suppressed since the Si-Ge bond is stronger than the Ge-Ge bond [44, 45].

The XPS spectra of Si 2p and Ge 3d peaks of the SiGe layer annealed at 880 °C for 10 min are shown in figure 5. It is evident from the XPS spectra that no oxide peaks of Si (∼104 eV) [46] and Ge (∼33 eV) [47] are observed, which indicates that no oxidation occurs during our fabrication processes. Using these peak intensity and area, the Si and Ge contents along the depth of the SiGe layer are evaluated and shown in figure 6, for the sample annealed at 880 °C for 10 min. The Ge content is found to decrease gradually as closing to the bottom of the SiGe layer. This result is consistent with the fact that the thermal diffusion of Ge atoms from top to down and vice versa for Si atoms. The average Ge fraction of the fabricated SiGe layer is obtained from figure 6 to be $x \sim 0.45$, which is in good agreement with the XRD results. Hence, the assumption that the fabricated pc-SiGe layer is fully relaxed is valid. Figure 7 shows the elemental distribution of Si and Ge over the sample surface, measured by EPMA for the SiGe sample annealed at 880 °C for 10 min. From the compositional profile, the average Ge fraction is evaluated to be $x = 0.434 \pm 0.005$. In EPMA analysis, the obtained Ge fraction is averaged in depth of SiGe layer due to its probe penetration depth, which results in the smaller Ge fraction comparing with that at the film surface in figure 6. It can be concluded that the fabricated SGOI layer is compositionally homogeneous in plane while there is gradual compositional distribution in depth.

Figure 8 shows a cross-sectional TEM image for the SGOI sample annealed at 880 °C for 10 min. It is found that a uniform SiGe/SiO₂ interface can be obtained. However, the thickness of SiGe layer obtained from the TEM image is 45 nm, which is less than the sum of the thicknesses of the as-deposited Si and Ge layers. The reduction in the thickness of the prepared SiGe layer is considered to be due to the difference in the density.
between amorphous and crystalline materials. That is, the density increases by the crystallization of \(\alpha\)-Ge and \(\alpha\)-Si, resulting in the reduction of film thickness [40, 41]. The root-mean-square (RMS) roughness of the sample surface determined by DFM is shown in figure 9, as a function of annealing time. The typical surface morphology image for the 10-min-annealed sample is also shown as an inset. The surface roughness is found to increase with increasing the annealing time. It is suggested that during the heat treatment, the SiGe particles coalesce and form larger SiGe islands, which leads to the enhancement of the surface roughness.

Figure 10 shows the thermal conductivity of our fabricated samples as a function of annealing time. This figure includes the result for a 50-nm-thick sc-Si\(_1-x\)Ge\(_x\)-on-insulator layer (\(x = 0.5\)) layer. It is found that the low thermal conductivity is observed in the as-deposited Ge/Si to be 0.79 W m K\(^{-1}\), comparing with the sc-SGOI layer, 1.4 W m K\(^{-1}\). This result is consistent with the fact that the as-deposited sample consists of \(\alpha\)-Ge and \(\alpha\)-Si bilayer. On the other hand, the 10- and 120-min-annealed SGOI layers have 0.87 and 0.90 W m K\(^{-1}\), respectively, which are higher than the as-deposited sample and lower than the sc-SGOI layer. This result originates from the suppression in the phonon velocity due to the enhancement of scattering at the grain boundaries in the pc-SGOI layer. From the full-width-half-maximum (FWHM) analysis [48] of the SiGe peaks
in XRD profiles of figure 4, the crystallite size was evaluated to be about 18 nm. This value is much smaller than the mean free path of phonon in Si about 300 nm [49]. Consequently, it can be said that an ultrathin SGOI layer with a lower thermal conductivity is successfully fabricated by a simple procedure since the fabricated pc-SGOI layer has smaller grain size than the phonon mean-free-path.

We performed Hall-effect measurement and Seebeck measurement for our samples. Unfortunately, we could not get any value due to high resistance of the samples because the prepared SiGe layer does not contain any dopant material. In the present study, we can obtain an ultrathin pc-SGOI layer with low thermal conductivity. Therefore, we will optimize impurity doping process and demonstrate the Seebeck coefficient, electrical conductivity, and figure-of-merit ZT in future.

4. Conclusion

With the aim of fabricating SiGe nanostructures for thermoelectric applications, an ultrathin SiGe layer was successfully formed on a SiO₂/Si substrate by a simple thermal evaporation method. The thickness of the fabricated SGOI layer was 45 nm and it had compositionally homogeneous in plane with a Ge fraction of \( x = 0.45 \) and however, there is gradual compositional distribution in depth. The prepared SiGe thin layer had a polycrystalline phase, where the crystallite size was about 18 nm much lower than the mean-free-path of phonon

Figure 9. RMS surface roughness of samples measured by DFM, as a function of annealing time. The inset shows a typical surface morphological image of the sample annealed at 880 °C for 10 min.

Figure 10. Thermal conductivity of fabricated pc-SGOI samples as a function of annealing time. The value obtained for a commercial sc-SGOI substrate is also plotted.
in bulk Si. The RMS surface roughness of the 880 °C-annealed SGOI layer was evaluated to be 2.68 nm while a uniform SiGe/SiO₂ interface was formed and there were no oxides of Si and Ge. The thermal conductivity of the fabricated SGOI layer annealed at 880 °C for 10 min was 0.87 W mK⁻¹ at room temperature, which was less than that of a sc-Si₀.₃Ge₀.₇ layer (1.4 W mK⁻¹). Therefore, our simple preparation procedure can give an ultrathin pc-SGOI layer with low thermal conductivity appropriate for nanostructured thermoelectric applications.

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