Coexistence of Grain-Boundaries-Assisted Bipolar and Threshold Resistive Switching in Multilayer Hexagonal Boron Nitride

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The use of 2D materials to improve the capabilities of electronic devices is a promising strategy that has recently gained much interest in both academia and industry. However, while the research in 2D metallic and semiconducting materials is well established, detailed knowledge and applications of 2D insulators are still scarce. In this paper, the presence of resistive switching (RS) in multilayer hexagonal boron nitride (h-BN) is studied using different electrode materials, and a family of h-BN-based resistive random access memories with tunable capabilities is engineered. The devices show the coexistence of forming free bipolar and threshold-type RS with low operation voltages down to 0.4 V, high current on/off ratio up to 10^6, and long retention times above 10 h, as well as low variability. The RS is driven by the grain boundaries (GBs) in the polycrystalline h-BN stack, which allow the penetration of metallic ions from adjacent electrodes. This reaction can be boosted by the generation of B vacancies, which are more abundant at the GBs. To the best of our knowledge, h-BN is the first 2D material showing the coexistence of bipolar and threshold RS, which may open the door to additional functionalities and applications.

1. Introduction

Digital information storage is one of the most demanded electronic applications in modern societies, as its capacity doubles every year and the total data storage capacity by 2020 is expected to reach 44 ZB.[1] Among all nonvolatile memory technologies to date, the resistive random access memory (RRAM) is the most promising due to its high performance and simple structure. The RRAM basically consists of a matrix of metal/insulator/metal (MIM) capacitors, in which the electrical resistance of the dielectric can be tuned by applying electrical stresses between the electrodes, allowing cyclical switching between a high resistive state (HRS) and a low resistive state (LRS).[2] These two states can be used to simulate the zeros and ones of the binary code, and therefore to store digital information. To date, RRAMs with high operation speeds (≈300 ps per transition),[3] low power consumption (≈0.1 pJ per transition),[4] good endurance (>10^12 cycles),[5] long data retention times (>10 years),[6] small size (down to 10 nm × 10 nm),[7] and high integration capacity (>1 × 10^{11} bits cm^{-2})[2] have been developed. These performance advances have been achieved using transition metal oxides (TMOs) as dielectric in the MIM structure (mainly HfO_{2},[8–11] Al_{2}O_{3},[12–15] TiO_{2},[16–19] and TaO_{X}[20,21]); the metallic
electrodes most commonly used in MIM cells for RRAMs are Ti, Pt, Ag, Cu, and Ni.[28] Unfortunately, to date no one RRAM device has simultaneously shown all these high performance qualities, which is strongly hindering the mass production of RRAMs. Some commercial products may currently be found on the market,[23,24] but their capacities are still very limited (i.e., they are just recommended for controlling sensors). Moreover, cycle-to-cycle and device-to-device variability is still a recognized problem of RRAM technologies.[25,26] To solve these problems, one promising methodology is to replace the metallic or insulating films in the MIM cells by other materials with advanced capabilities. Until now, the use of 2D materials has been very successful to develop field effect transistor and capacitors,[27,28] providing additional capabilities to the devices, such as flexibility and transparency. Several 2D materials including graphene, graphene oxide, MoS2, MoSe2, and even black phosphorous have been introduced in RRAM prototypes with the aim of enhancing their switching characteristics and providing additional functionalities.[29–34] However, graphene is conductive and needs to be complemented by an insulator (with which it usually forms a poor interface),[35] plus it requires a difficult transfer process; graphene oxide (GO) is not an excellent insulator (i.e., it can be easily degraded with the time, and for this reason GO-based RRAMs showed a poor endurance <100 cycles)[36,37] and its synthesis process (usually Hummers method and liquid phase exfoliation) is not compatible with the semiconductor industry.[38] The same applies to MoS2, MoSe2, and BP, which furthermore are not insulators, meaning that they are not able to provide large current on/off ratios in RRAM devices.[33] Hexagonal boron nitride (h-BN) may be a good solution enabling the fabrication of RRAMs and other logic devices given its insulating properties. With a band gap of ~5.5 eV[39,40] and a dielectric constant of ~3,[41] it can generate essential device functionalities, including the generation of electrical fields and capacitance effects.

On the one hand, compared to other 2D conductive and semiconducting materials, h-BN does not require any transfer process to build an RRAM, as it can be grown on a metallic substrate (which acts as bottom electrode) using scalable chemical vapor deposition (CVD) technique, and the top electrodes can be easily evaporated on it to form the MIM cells. This strongly simplifies the fabrication process, as well as it avoids the generation of cracks during 2D material manipulation[42] and the presence of contaminants from polymer scaffolds.[43] Moreover, the insulating nature of h-BN should result in a larger current on/off ratio in RRAMs.

On the other hand, compared to traditional dielectrics like SiO2 or TMOs, h-BN can be prepared with a very flat/uniform surface that may reduce variability effects.[44] Its superior chemical stability may inhibit interaction with adjacent layers, and its large thermal conductivity could favor heat dissipation in electronic devices.[41] Moreover, h-BN shows better reliability than HfO2 when exposed to electrical stresses,[45] and at the same time it is known that the grain boundaries (GBs) in polycrystalline CVD-grown h-BN sheets can serve as leaky paths.[46,47] The local generation of hot spots in a robust dielectric is a very interesting behavior in the field of resistive switching (RS), as that may limit dielectric breakdown (BD) lateral propagation, which should enhance the endurance of the RRAMs.

In this work we investigate the presence of RS in multilayer h-BN stacks using different top electrodes, and develop a complete family of scalable RRAM devices using multilayer h-BN as active RS medium. The devices show forming-free bipolar and threshold RS depending on the current limitation (CL) used, which is driven by the GBs in h-BN, as they allow easy B vacancies generation and metallic ion penetration. We achieve good control of the device properties by tuning the thickness and grain size of the h-BN stack, as well as by inserting interfacial graphene electrodes. The use of an entirely scalable fabrication process (i.e., mechanical exfoliation and electron beam lithography are avoided, and 2D material transfer is not required) is an important added value toward industry-compatible applications. We also demonstrate stable RS operation in flexible/transparent RRAM devices under bending. These results may represent an important milestone toward the use of 2D dielectrics in logic devices.

2. Results and Discussion

Multilayer h-BN stacks of different thicknesses (thin 5–7 layers and thick 15–20 layers) have been grown by CVD on Cu and Ni-doped Cu substrates (which also served as bottom electrode), and top squared electrodes of different sizes and materials have been evaporated on top using a shadow mask (see the Experimental Section and Figures S1 and S2 in the Supporting Information). In total six different types of RRAM devices have been fabricated (see Table 1 and the Experimental Section) and more than 300 cells have been characterized. Figure 1a shows the schematic representation of a Ti/thin h-BN/Cu device. Figure 1b displays the typical current versus voltage (I–V) curves collected in this device, which show forming-free bipolar RS with very low set and reset voltages (VSET and VRESET) below 0.4 V and ~0.8 V (respectively), and current on/off ratios of more than one order of magnitude. The cycle-to-cycle variability is very small, as corroborated in the Weibull plot of the resistance read at 0.1 V during more than 350 cycles (see Figure 1c). The reset process takes place in two phases: (i) first, a sudden current decrease occurs at ~0.28 V, and (ii) from that point until ~0.8 V the resistivity increases progressively. This is indeed indicating that the charge transport is governed by one completely formed conductive filament (CF) that coexists with several partially formed CFs. It should be highlighted that in some cycles (<25% of the total) we have observed several small sudden jumps that fit different levels of conductance during the reset process (see Figure S3 in the Supporting Information), indicating the presence and sequential disruption of multiple partially/completely formed CFs. More information about the current fittings using the quantum point contact (QPC) model can be found in the Supporting Information. In any case, the most repetitive reset behavior was the presence of a sudden initial current decrease followed by a progressive resistivity increase (as shown in Figure 1b), indicating the presence of a dominant CF; this observation is supported by the negligible area dependency observed in these devices (see Figure S4b in the Supporting Information)—this feature shows an important
downscaling potential. It is worth noting that, despite the amount of partially/completely formed CFs may vary during some (<25%) cycles, the currents in HRS and LRS showed low cycle-to-cycle variability (see Figure 1c).

Cross-sectional transmission electron microscope (XTEM) images collected in the fresh devices (Figure 1d) reveal the presence of many atomically thin defective paths formed across the layered h-BN stack, which are related to the well-known formation of defective GBs during the CVD growth process. This is in good agreement with the observation of forming-free RS (Figure 1b). Figure 1d further confirms that the GBs of each layer within the h-BN stack vertically align. In order to find out the chemical species involved in the switching, XTEM analyses coupled with electron energy loss spectroscopy (EELS) have been conducted. The typical EELS profiles at both nondefective (layered) and GB/CF locations of a Ti/thin h-BN/Cu device in LRS are plotted in Figure 1e,f (respectively). As it can be observed, at nondefective locations (Figure 1e) the B and N signals are quasi symmetric with respect to their maximum, overlap, and appear confined between the Cu and Ti profiles, i.e., no metallic impurities at the h-BN region have been observed. On the contrary, the EELS profiles collected at the GB/CF locations of the sample in LRS (Figure 1f) show clear migration of B toward the Ti electrode (the shape of the B profile is asymmetric), and at the same time, penetration of Ti into the h-BN stack is observed. It should be highlighted that the EELS cross sections (Figure 1e,f) overestimate the thickness of the layers compared to TEM images (Figure 1d); this was an expected behavior related to the lower accuracy and resolution to EELS compared to TEM. Therefore, the horizontal scales in Figure 1e,f should be qualitatively interpreted: i.e., the signals in Figure 1f spread in depth due to severe B and Ti migration.

The migration of B toward the Ti electrode is consistent with the lower activation energy calculated for B ion/vacancy diffusion, which could be even lower at the GBs. The ability of Ti to react with other species (e.g., O atoms in TMOs) and its capacity to migrate in/out of a dielectric to form/disrupt CFs have been already observed in other RRAM devices. Under top electrode positive polarization, Ti\textsuperscript{V} ions may move toward the cathode across the RRAM cell, leading to the formation of a Ti or TiN based CF through the h-BN stack. This observation is in agreement with the lack of temperature dependence displayed in Figure S4a (Supporting Information). The Ti\textsuperscript{V} ions are expected to diffuse preferentially at GB locations, where the lower density of the material and the larger density of B and N vacancies favor their migration. It is worth noting that GBs-free exfoliated h-BN does not exhibit RS, as corroborated by Hattori et al., thus confirming the key role played by GBs in the RS. The presence of GBs in the dielectric reduces the energy-to-breakdown and the overall assertiveness of the whole BD process, allowing its reversibility. It is worth noting that the GB-to-GD distance observed in h-BN (between 2 and 8 nm in Figure 1d) is much smaller than that observed in polycrystalline TMOs (>60 nm in Al\textsubscript{2}O\textsubscript{3}). Therefore, while the need for a GB may represent a concern when building nanosized TMO-based RRAMs, this is not a problem in h-BN based RRAMs. Furthermore, note that (unlike in TMOs) the size of the grains can be easily controlled with the CVD growth parameters (as it will be explained later), making possible tuning the amount of GBs per cell.

The switching mechanism observed in Ti/h-BN/Cu devices is different than those observed in TMO-based ones, in which the charge transport is governed either by O vacancies or metal ions movement. The Ti/thin h-BN/Cu RRAM devices here presented show a combination of both phenomena: B vacancies migration and mobile Ti\textsuperscript{V} ions penetration in the h-BN stack may occur simultaneously (see Figure 1f). Despite O vacancies migration in TMOs and B vacancies migration in h-BN may present certain parallelism, we are not aware of other works reporting RS based on B vacancies migration in h-BN. The large density of Ti at the CF region and the unaltered N profile indicate the formation of a TiN-based CF, although this hypothesis should be confirmed by ab initio calculations (which is out of the scope of this report). Then, under negative top electrode polarization the B ions and Ti\textsuperscript{V} ions may diffuse back to their original positions (h-BN stack and Ti electrode, respectively) disrupting the CFs created across the h-BN and increasing the overall resistance of the Ti/thin h-BN/Cu cell (reset process). The importance of Ti/h-BN interactions for the RS is supported by the absence of RS when using top Pt or Au electrodes (see Figure S5a in the Supporting Information) because noble metals with lower diffusivity do not allow interaction with other species. On the contrary, when the set event is induced using

### Table 1. Comparison of the performances observed for all the h-BN-based RRAM devices here studied. The devices in rows 5 and 6 were fabricated by transferring thin h-BN previously grown by CVD on CuNi substrates; the devices in rows 1–4 are flexible; and the devices in row 5 are also transparent. The symbol ‘\texttextsuperscript{−}’ indicates that this property has not been investigated. The endurance column shows the maximum number of cycles measured, and it does not represent the lifetime of the devices, as degradation was not observed. In general, very good correlation between fabrication parameters and device properties can be observed: (i) the need of forming and the presence of threshold RS can be controlled by using Cu or CuNi substrates, and (ii) the presence of high current on/off ratios and bipolar RS under negative set can be enabled using thick h-BN stacks.

| Row | Structure | Transfer needed | Bipolar RS under positive set | Forming process needed | V\textsubscript{SET} (V) | V\textsubscript{RESET} (V) | I\textsubscript{ON}/I\textsubscript{OFF} | Endurance cycles | Retention time (s) | Bipolar RS under negative set | Threshold RS |
|-----|-----------|-----------------|-------------------------------|------------------------|-------------------------|-------------------------|--------------------------|----------------|---------------------------|-----------------------------|-------------|
| 1   | Ti/thin h-BN/Cu | No               | Yes                           | No                      | 0.4 V × 10\textsuperscript{−} A | −0.3 V × 10\textsuperscript{−} A | 10                       | >350           | –                         | No                         | Yes          |
| 2   | Ti/thick h-BN/Cu | No               | Yes                           | No                      | 0.7 V × 10\textsuperscript{−} A | −0.7 V × 10\textsuperscript{−} A | 10\textsuperscript{4}    | >600           | –                         | Yes                        | Yes          |
| 3   | Ti/thin h-BN/CuNi | No               | Yes                           | Yes                     | 0.7 V × 10\textsuperscript{−} A | −0.4 V × 2 × 10\textsuperscript{−} A | 15                       | –              | –                         | No                         | No          |
| 4   | Ti/thick h-BN/CuNi | No               | Yes                           | Yes                     | 2.2 V × 10\textsuperscript{−} A | −1.3 V × 6 × 10\textsuperscript{−} A | 10\textsuperscript{4}    | –              | –                         | Yes                        | No          |
| 5   | Ti/thin h-BN/ITO  | No               | Yes                           | No                      | 0.5 V × 10\textsuperscript{−} A | −0.3 V × 10\textsuperscript{−} A | 10                       | >180           | –                         | No                         | No          |
| 6   | Ti/MLG/thin h-BN/MLG/Au | Yes              | Yes                           | Yes                     | 2.3 V × 10\textsuperscript{−} A | −0.6 V × 4 × 10\textsuperscript{−} A | 10\textsuperscript{4}    | >450           | 4 × 10\textsuperscript{4} s | No                         | No          |
negative polarity, none of the Ti/thin h-BN/Cu RRAM devices showed bipolar RS (see Figure S5b, Supporting Information), e.g., the subsequent positive top electrode biasing did not produce the reset of the devices. We also used different CLs ranging from $10^{-6}$ to $10^{-1}$ A, but no bipolar RS was observed under negative set in any Ti/thin h-BN/Cu device. This is surprising because Cu$^{n+}$ ions movement is known to be the driving force behind bipolar RS in electrochemical metallization cells using TMO dielectrics and Cu electrodes.\cite{56} This observation may be related to the large diffusivity of Cu$^{n+}$ ions, which may massively penetrate in the h-BN stack during the negative BD event, leading to irreversible BD. This rules out the involvement of Cu$^{n+}$ ions in the bipolar RS observed in Figure 1b, and further supports that B and Ti$^{n+}$ ions migration are the atomic rearrangements behind the switching in Ti/thin h-BN/Cu RRAM devices.

The involvement of oxygen in the switching has been discarded through ionic liquid gating experiments,\cite{57} which reveal no remarkable conductivity changes when h-BN stacks are exposed to air after ionic liquid gating experiments. Similar experiments performed in TiO$_2$ and other oxides\cite{58} revealed dramatic conductivity decrease after exposure to room environment due to the absorption of oxygen. Such a phenomenon did not take place in h-BN stacks. The influence of oxygen in RRAM devices capped with (60 nm thick) metallic top electrodes should be even lower (i.e., negligible).

With the aim of increasing the current on/off ratio, we follow three strategies: (i) use h-BN stacks with different

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**Figure 1.** a) Schematic of a Ti/thin h-BN/Cu RRAM device. b) Typical I–V curves in a 100 µm × 100 µm device showing bipolar RS. c) Cumulative distribution of the resistance per cycle in HRS and LRS read at 0.1 V. d) Cross-sectional TEM image showing defective paths (GBs) through the h-BN. e,f) EELS cross-sectional analyses of a pristine and GB/CF locations (respectively) for a device in LRS.
thicknesses, (ii) reduce the amounts of defects by increasing the h-BN grain size, and (iii) use of graphene interface electrodes. First, the thickness of the h-BN stack grown on Cu was increased by just enlarging the CVD growth time. The resulting Ti/thick h-BN/Cu devices show bipolar RS with enhanced current on/off ratios up to 10^4 (see Figure 2a). Interestingly, this behavior is not accompanied by the need of a forming process, and the device-to-device variability is very small (see Figure S6 in the Supporting Information). The pronounced sharp shape of the reset and the lower currents in HRS (compared to the thin h-BN sample, Figure 1b) indicate the presence of less totally/partially formed CFs in the h-BN stack, as well as that the BD recovery may have a different physical origin most probably related to thermal heat. The small current decrease at \( \approx -0.4 \) V right before the sudden reset indicates filament thinning before the complete disruption. Interestingly, unlike thin h-BN cells, Ti/thick h-BN/Cu devices showed bipolar RS when the set was induced under negative top electrode polarization (see Figure 2b), but only under lower CLs, e.g., 70 \( \mu \)A for negative set (Figure 2b) and 10 mA for positive set (Figure 2a). The explanation behind this observation may be as follows: when the thin h-BN is subjected to negative top electrode bias the large diffusivity of Cu may produce severe contamination of the thin h-BN, leading to an irreversible BD, as seen in Figure S5b of the Supporting Information. On the contrary, similar electrical stresses applied to thick h-BN produce less damage. The fact that bipolar RS using negative set is only observed under CLs smaller than those used under positive set is consistent with this hypothesis: under the same CL (10 mA) the large diffusivity of Cu produces irreversible BD.

We further explore the RS capabilities of Ti/thick h-BN/Cu RRAM devices by tuning the current limitation, which revealed interesting additional performances. When the current compliance is lowered to values between 10^-6 and 10^-4 A, threshold-type RS with current on/off ratios up to three orders of magnitude has been observed (see Figure 2c). For all current levels, the voltage windows are enough large and ensure no data mismatch. Larger CLs induce smaller \( V_{\text{SET}} \) and \( V_{\text{RESET}} \), indicating good tunability of the CF size. The recovery of the HRS in the absence of bias indicates that h-BN is a stable and reliable dielectric, which may be related to the enhanced chemical stability of the h-BN stack. To the best of our knowledge, this is the first 2D material based RRAM device showing threshold RS; probably, previous devices made by using graphene, MoS2, MoSe2, and BP did not show this capability because they are not insulators, and graphene oxide may not be enough robust to restore its resistivity when the bias is switched off. The observation of threshold-type RS in h-BN opens the door to its use as selector in RRAM devices.

As a strategy to further reduce the currents in HRS, the multilayer h-BN stacks have been grown on Ni-doped Cu substrates, which increases the size of the domains and reduces the amount of defective GBs per unit area (see Figure 3a). All the devices fabricated with this substrate required a forming

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**Figure 2.** Typical RS behavior observed for the Ti/thick h-BN/Cu when inducing the set process under (a) positive and (b) negative top electrode polarization. (c) Typical threshold-type RS measured in Ti/thick h-BN/Cu devices under positive and negative top electrode polarization using current limitations of 10^-6, 10^-5, and 10^-4 A. For negative top electrode biasing the plot at 10^-4 A is missing because at such CL the devices do not show RS (the BD event becomes irreversible).

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**Figure 3.** (a) Cross-sectional TEM image showing the improved structure of the h-BN stack grown on CuNi. Typical RS behavior observed in (b) Ti/thin h-BN/CuNi and (c) Ti/thick h-BN/CuNi RRAM devices.
process (see Figure S7a in the Supporting Information), and the forming voltage increased with the h-BN stack thickness. It is worth noting that the forming process in layered 2D insulators differs from that of 3D insulators, as the layered material shows novel anisotropic speed for defect formation,[31] due to the different type of spatial interactions (covalent bonding in-plane and van der Waals interactions out-of-plane). The pre-BD currents show clear area dependence (see Figure S7b in the Supporting Information), indicating that no completely formed CFs are created during the CVD growth. The post-BD I–V curves show bipolar RS behavior (see Figure 3b,c), and the devices using thicker h-BN stacks show higher $V_{\text{SET}}$ and $V_{\text{RESET}}$ voltages (2 V and ~1.5 V, respectively), as well as larger current on/off ratios (up to six orders of magnitude). Compared to the h-BN/Cu counterparts, the devices using bottom Ni-doped Cu electrodes show lower currents in HRS ($I_{\text{HRS}}$), probably due to the lower amount of partially formed CFs (and GBs, see Figure S8 in the Supporting Information).

The ability of h-BN to build flexible and transparent RRAM devices has been proved by using Indium Tin Oxide/Polyethylene terephthalate (ITO/PET) substrates. These devices have been fabricated transferring thin h-BN (grown by CVD on Cu) onto flexible PET polymer with an ~185 nm thick film of ITO on top, followed by electrodes evaporation (see the Experimental Section). Then, the devices have been tested in the probe station under different bending radius (see Figure 4a). For all tests, the Ti/h-BN/ITO devices showed reproducible bipolar RS during more than 180 cycles (see Figure 4b), and no RS degradation was observed. The progressive reset is similar to the one observed in Ti/h-BN/Cu devices (Figure 1b). The observation of RS in Cu-free Ti/h-BN/ITO devices supports that Cu is not necessary for inducing state transitions, in agreement with the EELS profiles (Figure 1f). After more than 180 cycles, the cumulative probability plot of the resistance in HRS and LRS measured at 0.1 V shows acceptable variability without resistance mismatch in both states (Figure 4c).

Finally, the RS phenomenon has been studied by inserting a sheet of multilayer graphene (MLG) between the h-BN and the metallic electrodes. Graphene interfacial electrodes have demonstrated to reduce the power consumption of RRAM devices thanks to graphene’s high out-of-plane electronic resistance, stabilize the RS response by blocking oxygen diffusion, protect the dielectric from environmental moisture, provide superb transparency, and allow mechanical bending without performance degradation.[29,30,62] Ti/MLG/h-BN/MLG/Au RRAM devices have been fabricated with assistance of standard transfer process.[63] The entire fabrication process is schematically described in Figure S9 (Supporting Information). Basi- cally, a wafer of 300 nm SiO$_2$/Si has been coated with 10 nm Ti (first) and 50 nm Au (second). Then, the surface of the Au has been functionalized via oxygen plasma etching process for 1.5 min in O$_2$ atmosphere using a power of 200 W to increase the roughness of the substrate, which favors the adhesion of the 2D material and reduces the amount of wrinkles.[64] Then, first an MLG sheet, second a thin h-BN sheet (previously grown on Ni-doped Cu), and third another MLG sheet have been sequentially transferred, and Au/Ti electrodes have been evaporated on top by shadow mask and e-beam evaporator (as in previous devices). More details can be found in the Experimental Section and Figure S9 of the Supporting Information. At this step, the samples have been characterized via optical microscope (not shown) scanning electron microscopes (SEM; Figure S10, Supporting information) and atomic force microscope (AFM; Figure S11, Supporting information), which reveal smooth surface of each layer. In the AFM topographic maps, we intentionally displayed some areas where wrinkles were formed to demonstrate the presence of 2D material. The XTEM images (Figure 5a) show the thick 2D layered (van der Waals) heterogeneous stack. By means of EELS cross sections (Figure 5b) we prove the correct fabrication of the Ti/MLG/h-BN/MLG/Au devices. As it can be observed, the B and N signals are confined between the two C peaks corresponding to MLG electrodes. After this, the top MLG sheet has been removed by plasma etching to isolate all the MIM cells (keeping top MLG only under the top metallic electrodes; see Figure S9 of the Supporting Information) and the resulting devices have been tested in the probe station.

From an electrical point of view, compared to metal/h-BN/metal counter devices (Figure 3b), the use of MLG interfa- cial electrodes increased the forming voltage up to ~8 V (see Figure 5c), and the reset process turned into sharp. More information about the size of the partially formed CF (constriction) before and after the forming is given in the Supporting Information. In the following cycles, the devices showed improved current on/off ratios up to four orders of magnitude with low cycle-to-cycle variability (no HRS/LRS data overlap; see Figure 5d), as well as long state retention times (Figure 5e). The device-to-device variability is also very small, as these results

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**Figure 4.** a) Photograph of the Ti/thin h-BN/ITO devices during probe station test. b) Typical RS behavior observed in these cells under a curvature radius of 4 cm. c) Cumulative distribution of the resistance during HRS and LRS during 180 cycles (read at 0.1 V).
have been successfully reproduced in more than 35 devices (see Figure S12 in the Supporting Information). It is worth noting that $V_{\text{SET}}$ is larger and $I_{\text{HRS}}$ is lower than in graphene-free devices using the same type of h-BN (see Figure 3b). These observations could be explained as follows: the MLG film acts as blocking layer which makes it quite hard for atoms to diffuse through it, i.e., B migration toward the Ti electrode and Ti$^{3+}$ ions penetration in the h-BN stack (see Figure 1f). Nevertheless, at graphene point defects the penetration of Ti$^{3+}$ ions is possible. Lübben et al. observed that, in both Ta/graphene/TaO$_x$/Pt and Pt/graphene/TaO$_x$/Pt devices, the interactions between Ta ions and the TaO$_x$ film can take place during the RS process (even with the presence of interfacial graphene). This larger difficulty for metal ions migration into the h-BN film results in a larger forming voltage (up to $\approx 8$ V) compared to graphene-free devices (in which $V_{\text{FORMING}}$ was below 3 V, as shown in Figure S7a of the Supporting Information).

The sharper nature of the reset process and the lower $I_{\text{HRS}}$ in Ti/MLG/h-BN/MLG/Au devices can be easily explained by the lower amount of filaments through the h-BN stack; the larger $V_{\text{SET}}$ currents compared to graphene-free cells may also be related to the well-known higher out-of-plane resistance offered by the graphene film, which should be also a factor contributing to lower $I_{\text{HRS}}$. These hypotheses have been confirmed by XTEM and EELS. After the electrical stresses, almost all locations of the sample showed undamaged structure (similar to that displayed in Figure 5b). However, at some spots of the sample, partial h-BN degradation was observed (Figure 5f), and just a few locations revealed complete CF formation (Figure 5g). The EELS profiles collected at the partially degraded and CF locations reveal clear penetration of Ti into the h-BN stack (Figure 5h), which reaches the bottom graphene electrode (orange circle).
highlighted that the shifts of the B and N signals observed in Figure 5h,i are not representative, as important variability from one CF to another has been observed. The only repetitive and meaningful atomic rearrangement in all the EELS profiles collected for the Ti/MLG/h-BN/MLG/Au samples is the penetration of Ti$_{X}$ ions into the h-BN. Probably the more abrupt HRS/LRS/HRS state transitions (driven by the Ti$_{X}$ ions migration) lead to more uncontrollable rearrangements in the B and N signals. Interestingly, the shape of the filament is conical with the narrower end at the anode side, indicating the migration of Ti$_{X}$ ions (or clusters of ions) toward the cathode under positive set biasing (see Figure 5g), in agreement with the EELS profile.\[67]\] This is indeed indicating that the Ti diffusivity in the bulk h-BN is larger than at the top MLG/h-BN interface, otherwise the Ti$_{X}$ ions would accumulate at the MLG/h-BN interface, moving slowly toward the bottom h-BN/MLG interface and producing a filament with opposed shape (narrower end at the cathode). This is consistent with the blocking nature of the MLG stack, and further explains the small migration of B toward the top Ti electrode observed in Figure 5i. Interestingly, when the set is induced under negative top electrode polarization, the Ti/MLG/h-BN/MLG/Au RRAM devices do not show stable RS (just three cycles, not shown); this should be related to the poorer mobility of Au ions in the h-BN stack, and further supports that the RS observed in Figure 5c is related to the migration of Ti$_{X}$ ions. In the case of metal/h-BN/metal devices, metallic ion migration is always accompanied by B vacancies movement, while the devices using graphene interfacial electrodes show RS even without the diffusion of B toward the electrodes. As in the flexible/transparent device (Figure 4) the absence of Cu in these devices indicates that this element is not necessary for observing RS.

Until today no RRAM device using 2D materials has achieved a performance comparable to that of the TMO-based technology.\[11,68\] Nevertheless, the extraordinary properties of 2D materials make them very promising in the field of RRAMs. Compared to 2D metals and semiconductors, in RRAM technology h-BN shows the advantage of no need of a transfer process, as well as higher current on/off ratios (as demonstrated above). Jain et al.\[69\] observed unipolar RS transitions in planar nanogap-based h-BN nanosheets obtained by mechanical exfoliation, but these devices are not scalable and no endurance tests were shown; moreover, exfoliated nanosheets are not polycrystalline, which implies a different mechanism. Qian et al. observed bipolar resistive switching in amorphous boron nitride.\[70\] but the absence of a layered structure (like the one we show in Figures 1d and 3a) may jeopardize the chemical stability and thermal heat dissipation in the h-BN film. Compared to Qian et al.,\[70\] our devices show forming-free bipolar RS, which coexists with threshold type RS in some devices. We also include additional information about the effect of h-BN thickness, h-BN grain sizes and interfacial MLG electrodes in the performance of the devices. The novel switching mechanisms here reported seem to be different to that observed in ref.\[70\] as in that work the migration of B and the key role of the GBs are not demonstrated. The performances of all h-BN based RRAM devices here reported have been summarized in Table 1. Future works in this field should concentrate on the development of 2D materials based RRAM devices on metal coated wafers.

3. Conclusion

Multilayer h-BN stacks grown by CVD have been used for engineering a new class of 2D RRAM devices. The fabrication of the metal/h-BN/metal devices involved only scalable techniques and did not require 2D material transfer, i.e., the h-BN was grown by CVD on Cu (which served as bottom electrode) and top electrodes were patterned on top via shadow mask and e-beam evaporator. The resulting h-BN based RRAM devices show coexistence of forming-free bipolar and threshold type RS, which is a local phenomenon related to the formation of conductive filaments at the grain boundaries of the h-BN stack. By using different electrode materials we conclude that the RS is assisted by metallic ion penetration in the h-BN stack, which can be boosted by the generation of B vacancies. We developed three different strategies to tune the properties of the devices: (i) h-BN stack thickness modification, (ii) GBs density adjustment by substrate doping, and (iii) insertion of interfacial graphene electrodes. As a result, the RRAM cells exhibited forming-free RS, low $V_{SET}$ and $V_{RESET}$ down to 0.4 and 0.8 V (respectively), high current on/off ratios up to six orders of magnitude, long retention times above 10 h, and low device-to-device variability. The possibility of building flexible and transparent devices, as well as the fabrication of the first RRAM devices based on graphene/h-BN/graphene van der Waals structures, has been also demonstrated. The observation of threshold type RS in h-BN may enable its use as selector in RRAM devices.

4. Experimental Section

Material Synthesis: The h-BN/Cu samples were grown at the company Graphene Supermarket using borazine as precursor and a 20 µm thick Cu foil as substrate, following the procedures detailed in ref.\[41\]. Two different items (Nos. A121913 and A120415) were bought and upon close inspection by XTEM it was determined that their thicknesses were between 5 and 7 layers and 15–20 layers. In both cases the h-BN contained large amounts of GBs (see Figure 1d). The h-BN/CuNi samples were grown by us using Ni doped Cu substrates, following the methodologies reported in previous work.\[81\] This type of h-BN contains a very low amount of defects due to the larger size of its grains (less amount of GBs per unit area or device). In total, two different batches of h-BN/Cu were used. The first batch had a thickness of 15–20 layers, and the second one between 5 and 7 layers. The materials sources were purchased in Resemir Co. Ltd.

Device Assembly: After material growth, a matrix of top square electrodes consisting of 40 nm Au (top) on 20 nm Ti (bottom) and with sizes ranging from 100 µm × 100 µm down to 10 µm × 10 µm were deposited using an electron beam evaporator (Kurt J Lesker Company, PVD75) and a laser-patterned shadow mask (from Tencan, UK). The deposition rate in the evaporator was 0.5 Å s$^{-1}$. Some MIM structures using Pt or Au electrodes (without Ti) were also fabricated. In this investigation, six different sets of RRAM devices using two different types of h-BN were fabricated (see Table 1). No transfer process was required for devices type 1–4, while devices type 5 and 6 required transfer. The h-BN used for devices type 5 and 6 was the 5–7 layers thick (film) grown on CuNi. For the fabrication of devices type 6, a substrate consisting of 300 nm SiO$_2$ on Si was covered with 20 nm Ti (first) and 40 nm Au (second). After that, the surface of the Au/Ti/SiO$_2$/Si wafer was exposed to oxygen plasma treatment (200 W during 1.5 min) to increase the roughness of the surface, which remarkably reduced the amount of wrinkles in subsequently transferred 2D films.\[84\] Then, an 8–12 layers thick MLG sheet grown at Hangzhou Gelaefang Nanotechnology was transferred on the Au/Ti/SiO$_2$/Si sample using PMMA as rigid
media. First, the liquid PMMA was spin-coated on the surface of the multilayer graphene with a two-step spin-coating process, 500 rpm for 6 s and 4500 rpm for 1 min. After that, the Cu foil was etched in FeCl₃ (0.1 g mL⁻¹) and the PMMA/MLG stack was washed in HCL (2 wt%) and pure water. The PMMA/MLG stack was picked up with the target substrate, and it was dried at 50 °C for 3 h. Finally, the whole sample was immersed in the acetone for 24 h to remove the PMMA. For the transfer of the successive h-BN and MLG, a similar process was followed. The size of each transferred 2D material was smaller than that of the previous one, so that the interfaces can be characterized (as shown in Figures S10 and S11 of the Supporting Information). Top Au/Ti electrodes similar to those of devices type 1–5 were evaporated on the top graphene layer to allow a good connection to the probe station. Finally, the capacitors were isolated from each other by etching the top MLG between them using oxygen plasma at 200 W during 1 min. The whole fabrication process is indicated in Figure S9 (Supporting Information).

Device Characterization: The devices were analyzed with two different SEM, the Carl Zeiss Supra 55 and the Quanta 200 FEG. The AFM characterization was conducted using a Bruker Dimension Icon and a Multimode V AFM from Veeco. The topographic characterization was done in tapping mode using standard silicon tips from Nanoworld (item No. 78131F6L965), and the nanoscale electrical characterization was conducted using a Bruker Dimension Icon and a Multimode V AFM from Veeco. The topographic characterization was available from the Wiley Online Library or from the author.

Supporting Information
Supporting Information is available from the Wiley Online Library or from the author.

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[1] Crossbar Inc., http://crossbar-inc.com/(accessed: September 2016).
[2] International Technology Roadmap for Semiconductors, 2013 Edition, Process Integration, Devices, and Structures section, www.itrs.net (accessed: February 2015).
[3] H. Y. Lee, Y. S. Chen, P. S. Chen, P. Y. Gu, Y. Y. Hsu, S. M. Wang, W. H. Liu, C. H. Tsai, S. S. Sheu, P. C. Chiang, W. P. Lin, C. H. Lin, W. S. Chen, F. T. Chen, C. H. Lien, M. J. Tsai, in 2016 International Electron Devices Meeting (Ed: P. W. Mahoney), IEEE, Piscataway, NJ, 2016, 19.7.1.
[4] C. Ahn, Z. Jiang, C.-S. Lee, H.-Y. Liang, L. S. Liyanage, H.-S. P. Wong, IEEE Trans. Electron Devices 2015, 62, 2197.
[5] M. J. Lee, C. B. Lee, D. S. Lee, S. R. Lee, M. Chang, J. H. Hur, Y. B. Kim, C. J. Kim, D. H. Seo, S. Seo, U. I. Chung, I. K. Yoo, K. Kim, Nat. Mater. 2011, 10, 625.
[6] S. R. Lee, Y. B. Kim, M. Chang, K. M. Kim, C. B. Lee, J. H. Hur, G. S. Park, D. Lee, M. J. Lee, C. J. Kim, U. I. Chung, I. K. Yoo, K. Kim, in 2012 Symp. on VLSI Technology (VLSIT) (Ed: P. Mahoney), IEEE, Piscataway, NJ, 2012, 71.
[7] B. Govoreanu, G. S. Kar, Y. Y. Chen, V. Paraschiv, A. Fantini, I. P. Radu, L. Goux, S. Clima, R. Degraeve, N. Jossart, 2011 International Electron Devices Meeting, (Ed: P. Mahoney), IEEE, Piscataway, NJ, 2011, 31.6.1.
[8] B. Gao, H. Zhang, S. Yu, B. Sun, L. Liu, X. Liu, Y. Wang, R. Han, J. Kang, B. Yu, IEEE Symp. on VLSI Technology (Ed: P. Mahoney), IEEE, Piscataway, NJ, 2009, 10826827.
[9] S. S. Sheu, P. C. Chiang, W. P. Lin, H. Y. Lee, P. S. Chen, Y. S. Chen, T. Y. Wu, F. T. Chen, K. L. Su, M. J. Kao, K. H. Cheng, M. J. Tsai, in 2009 Symp. on VLSI Circuits, IEEE, Piscataway, NJ, 2009, 82.
[10] U. Chaud, K. C. Huang, C. Y. Huang, C. H. Ho, C. H. Lin, T. Y. Tseng, J. Appl. Phys. 2015, 117, 184105.
[11] D. Duncan, B. Magyari-Köpe, Y. Nishi, Appl. Phys. Lett. 2016, 108, 043501.
[12] B. Sarkar, B. Lee, V. Misra, Semicond. Sci. Technol. 2015, 30, 105014.
[13] C. Ahn, Z. Jiang, C. S. Lee, H. Y. Chen, J. Liang, L. S. Liyanage, H. S. P. Wong, IEEE Trans. Electron Devices 2015, 62, 2197.
[14] J. Zhou, F. Cai, Q. Wang, B. Chen, S. Gaba, W. D. Lu, IEEE Trans. Electron Devices 2016, 37, 404.
[15] L. G. Wang, X. Qian, Y. Q. Cao, Z. Y. Cao, G. Y. Fang, A. D. Li, D. Wu, Nano Res. Lett. 2015, 10, 135.
[16] H. Y. Jeong, S. K. Kim, J. Y. Lee, S. Y. Choi, J. Electrochem. Soc. 2011, 158, 979.
[17] J. Shim, I. Kim, K. P. Biju, M. Jo, J. Park, J. Lee, S. Jung, W. Lee, S. Kim, S. Park, H. Hwang, J. Appl. Phys. 2011, 109, 033712.
[18] I. J. Huang, C. W. Kuo, W. C. Chang, T. H. Hou, Appl. Phys. Lett. 2010, 96, 262901.
[19] H. Y. Jeong, Y. I. Kim, J. Y. Lee, S. Y. Choi, Nanotechnology 2010, 21, 115203.
[20] C. Chen, C. Song, J. Yang, F. Zeng, F. Pan, Appl. Phys. Lett. 2012, 100, 253509.
[21] Z. Wei, Y. Kanzawa, K. Anta, Y. Katoh, K. Kawai, S. Muraoka, S. Mitani, S. Fujii, K. Katayama, M. Iijima, in 2008 IEEE International Electron Devices Meeting (Ed: P. Mahoney), IEEE, Piscataway, NJ, 2008, 1.
[22] S. Mei, M. Bosman, R. Nagarajan, X. Wu, K. L. Pey, Microelectron. Reliab. 2016, 61, 71.
[23] Website of Panasonic: (Microcontrollers), https://na.industrial.pana- sonic.com/products/semiconductors/microcontrollers/8-bit-low-power-microcomputers-mn101i-series (accessed: September 2016).
[24] Website of adesto technologies, http://www.adestotech.com/products/mavriq/(accessed: September 2016).
[25] H. S. P. Wong, H. Y. Lee, S. Yu, Y. S. Chen, Y. Wu, P. S. Chen, B. Lee, F. T. Chen, M. J. Tsai, Proc. IEEE 2012, 100, 1951.
[26] A. Fantini, L. Goux, R. Degraeve, D. J. Wouters, N. Raghavan, G. Kar, A. Belmonte, Y. Y. Chen, B. Govoreanu, M. Jurczak, in 5th IEEE International Memory Workshop (Ed: P. Kalavade), IEEE, Piscataway, NJ, 2013, 30.
[27] Y. Ji, S. Lee, B. Cho, S. Song, T. Lee, ACS Nano 2011, 5, 5995.
[28] N. Guo, J. Wei, Y. Jia, H. Sun, Y. Wang, K. Zhao, X. Shi, L. Zhang, X. Li, A. Cao, Nano Res. 2013, 6, 602.
