Study of Reversible Logic Synthesis with Application in SOC: A Review

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Abstract: The prime concern in today’s SOC designs is the power dissipation which increases with technology scaling. The reversible logic possesses very high potential in reducing power dissipation in these designs. It finds its application in latest research fields such as DNA computing, quantum computing, ultra-low power CMOS design and nanotechnology. The reversible circuits can be easily designed using the conventional CMOS technology at a cost of a garbage output which maintains the reversibility. The purpose of this paper is to provide an overview of the developments that have occurred till date in this concept and how the new reversible logic gates are used to design the logic functions.

Keywords: SOC, Reversible logic, CMOS, power dissipation

1. INTRODUCTION

The power dissipation is one of the 3 design metrics of a typical SOC application. The technology scaling has led power dissipation to be of prime concern in modern circuits. The reversible logic first came into mention in the decade of 60’s and Rolf Landauer proposed a link between thermodynamics and the current computing machines. He stated that for every bit lost in the computation process energy of at least $K*T*\ln2$ J/bit will be dissipated. Later, however it was proved that the reversible machines dissipate even much less energy per bit [2]. But still, today, as the Moore’s law struggles to hold up, there is a need for potential alternatives like reversible logic which seems to be a promising candidate.

The current technology computers consume almost 2.5% of the total generated energy [10] of the world and are still far away from the lowest possible energy consumption [1]. The optimization of current computers cannot achieve the lowest possible limit of energy dissipation per bit ($K*T*\ln2$) with time. Since then a lot of work has been done using reversible logic and both reversible combinational and sequential circuits have been proposed. These designs were completely designed using reversible logic gates. Table I describes the four basic reversible logic gates along with their properties. The figure below describes the gap between the feasible low power dissipation and the dissipation in the current technology.
Some important figure of merits [3] of the reversible logic gates are:

**Balanced functions:** The multiple output Boolean function is called reversible, if:

a. The total number if inputs are equal to the total number of outputs.
b. There exists a one-to-one mapping between these ports.

**Garbage output:** Reversible logic gates are circuits designed out of standard CMOS in which number of outputs is equal to the number of inputs and there is a one-to-one mapping between these terminals. It helps to maintain the reversibility of the circuit by disposing the unnecessary outputs of the whole circuit into a single output i.e. garbage output which could be left unused.

**Quantum cost:** In reversible logic quantum cost means the total number one-by-one (1x1) reversible gates and two-by-two (2x2) reversible gates used in the reversible circuit design. It should be as low as possible.

Design Constraints: There exist some design constraints whereas designing reversible circuits, which produce a similar effect of using this concept for low power dissipation to the design metrics of VLSI design. These are:

i. Fan-outs in the circuit is not possible: This is so because whereas using fan-out, the current would flow through two different paths, which would mean duplicating the particle which is not possible in quantum physics.
ii. Feedback is not allowed: The reason for this can be traced back to quantum physics. In feedback, the particle would be forced back in the loop. This would mean the particle would travel back in time and which is obviously not possible.

It was in 2012, when after almost 40 years, the original proposal made by Landauer on irreversibility came into light once again, verified this work experimentally. The basic reversible logic gates are Feynman gate, Fredkin gate, Toffoli gate, Peres gate which are drawn below:

![Basic reversible logic gates](image)

| Reversible gates | Quantum cost | Number of ports |
|------------------|--------------|-----------------|
| Feynman gate [21]| 1            | 2*2             |
| Toffoli gate [15]| 5            | 3*3             |
| Fredkin gate [22]| 5            | 3*3             |
| Peres gate [23]  | 4            | 3*3             |

2. THEORETICAL VERIFICATION OF REVERSIBLE LOGIC

Landauer [1] in his work on irreversibility has discussed that logical functions are inevitably used in a computing machine and don’t have single-valued inverse. Information processing is always accompanied by heat dissipation. In order to transfer a particle from its stable potential well in logic ‘1’ state to logic ‘0’ or vice-versa, a push is required and when it reaches the desired state, a
retarding force is also required. The computer operates by pushing information around in a manner that is independent of exact data.

The present computing machines don't have output which uniquely defines the inputs and hence are irreversible. Each particle has defined entropy in its space. Also, the entropy of the computer cannot decrease which has to appear somewhere else in the system and hence appears in the form of heat. A logical irreversible function can become reversible only by “embedding” it in a truth function of larger number of variables. Hence, more inputs and outputs are required to hold the information for providing reversibility.

Soon after that a study [2] proved that it is possible to achieve a much lower level of dissipation per bit than specified by Landauer. He showed that a lower power dissipation is possible if the circuit design is made entirely using reversible logic gates. Further a study [3] derived a relationship between reversible 3 x 3 gates and corresponding symmetric groups. Further, it highlighted the role of this concept in quantum computing. Later, [4] proposed a study which mapped irreversible and reversible logic functions which was applicable to both quantum and classical model of computation. They derived an associated theory of irreversible computations that indirectly paved the way for the desired output and a garbage output which is unnecessary accumulation of intermediate outputs and help in maintaining the reversibility.

3. COMBINATIONAL REVERSIBLE ELEMENTS

Different adders like carry look ahead, carry skip adders, ripple carry adder using different reversible logic gates [5] such as Fredkin gate, Feynman gate, Toffoli gate which are introduced initially to the proposal of the adder circuit designs. A more significant study [6] explained the design of reversible ALU which is very crucial in a computing machine. It was a 1-bit ALU designed using MG and HNG gates and was verified and simulated using VHDL in Xilinx 12.4. Moreover, they also proposed a 4-bit ALU using modified Kogge-stone adder. Another study [6] proposed a novel design of a reversible binary 2-to-4 decoder that realizes appreciable improvement over the existing reversible decoder design in quantum cost, garbage outputs and constant inputs.

Lekshmi viswanath [7] proposed a novel 16-bit reversible ALU which were simulated in modelsim SE 6.5 and synthesized using Xilinx ISE 12.2. A study on low power fault tolerant reversible decoder using MOS [8] showed simulations of the proposed decoder which were designed and verified in DSCH 2.7. Various studies on ALU [11] - [13] and adders [12] can also contribute to the work on this concept.

4. SEQUENTIAL REVERSIBLE ELEMENTS

Different sequential circuits are proposed in [14] - [20] with designs from the most basic flip-flop to a reversible control unit of a processor. [14] proposes an algorithm to optimize the figure of merits of the reversible latch, whereas [15] presents an asynchronous counter on 0.35 µm technology in Tanner tool. An efficient reversible RAM [16] is presented using a novel decoder and a write enable reversible master-slave D-flip-flop, which is found to be superior in each
figure of merit. Further, reversible flip-flops [18] are proposed and verified in cadence virtuoso and H-spice tools. [17], [19] - [20] proposes complex reversible sequential circuits like shift register, SRAM cell, sequence counter, 3x8 decoder, instruction register and a reversible control unit of a processor is designed.

5. CONCLUSION

The reversible logic seems to be a potential candidate in dealing with the power dissipation in SoC circuits. However, this requires a complete new set of reversible designs and reversible programming languages, hence implying a huge need of research. It can also be called as an aid of the future technology as it has its applications in various advanced applications like DNA computing, quantum computing, low power CMOS design and so on. This work can be easily verified on the existing HDL languages as well as on the CAD tools.

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REFERENCES

[1] Landauer R., “Irreversibility and Heat Generation in the Computing Process”, IBM Journal of Research and Development, p: 183-191, 1961.
[2] C. H. Bennett, “Logical Reversibility of Computation”, IBM Journal of Research and Development, p: 525-532, 1973.
[3] Majid Mohammadi and Mohammad Eshghi “On figures of merit in reversible and quantum logic designs” Springer Science+Business Media, 298-318, February 2009
[4] Alexander S. Green and Thorsten Altenkirch “From Reversible to Irreversible Computations” Electronic Notes in Theoretical Computer Science 210 65–74, 2008
[5] P. K. Lala, J.P. Parkerson and P. Chakraborty “Adder Designs using Reversible Logic Gates”, Wseas Transactions on Circuits and Systems, Issue 6, Volume 9, 369-378, June 2010
[6] Matthew Morrison, Matthew Lewandowski, Richard Meana and Nagarajan Ranganathan, “Design of a Novel Reversible ALU using an Enhanced Carry Look-Ahead Adder” 11th IEEE International Conference on Nanotechnology, August 15-18, 2011.
[7] Lekshmi Viswanath, Ponni.M, “Design and Analysis of 16 Bit Reversible ALU” IOSR Journal of Computer Engineering (IOSRJCE) Volume 1, Issue 1, PP 46-53, May-June 2012
[8] Md. Shamsujjoha and Hafiz Md. Hasan Babu “A Low Power Fault Tolerant Reversible Decoder Using MOS Transistor” 26th International Conference on VLSI Design and 12th International Conference on Embedded Systems, 2013.
[9] Antoine Be’rut, Artak Arakelyan, Artyom Petrosyan, Sergio Ciliberto, Raoul Dillenschneider & Eric Lutz, “Experimental verification of Landauer’s principle linking information and thermodynamics”, p: 187-190, volume 483, Nature, 8 March, 2012
[10] Dell Client Energy Savings Calculator Methodology Paper.
[11] Kamaraj Arunachalam, Marichamy Perumalsamy, C. Kalyana Sundaram, and J. Senthil Kumar, “Design and implementation of a reversible logic based 8-bit arithmetic and logic unit”, International Journal of Computers and Applications, Vol. 36, No. 2, 2014.
[12] Rigui Zhou, Manqun Zhang, Qian Wu & Yang Shi, “Designing novel reversible BCD adder and parallel adder/subtraction using new reversible logic gates”, International Journal of Electronics, volume 99, no. 10, p: 1395–1414, October 2012.
[13] Chinmaye R., Amrutha C., Vishwanath S., Soumya S. Ghosh, Shouryadipta Sarkar, “Design of Optimal Reversible Arithmetic Logic Units”, International Journal of Engineering and Innovative Technology (IJEIT) Volume 4, Issue 12, June 2015
[14] Abu Sadat Md. Sayem and Masashi Ueda “Optimization of reversible sequential circuits” Journal of computing, Volume 2, Issue 6, June 2010
[15] Prashant R. Yelekar and Prof. Sujata S. Chiwande “Design of sequential circuit using reversible logic” IEEE-International Conference on Advances in Engineering, Science and Management (ICAESM -2012) March 30-31, 2012
[16] Md. Selim Al Mamun and Syed Monowar Hossain “Design of Reversible Random Access Memory” International Journal of Computer Applications, Volume 56– No.15, October 2012
[17] Lafifa Jamal Md. Masbaul Alam, Hafiz Md. Hasan Babu “An efficient approach to design a reversible control unit of a processor”, Sustainable Computing: Informatics and Systems 3, 286– 294, 2014
[18] R. Jayashree, M. Kiran Kumar and Prof. Dr. J. Selvakumar “Design and analysis of flip-flops using reversible logic” International Journal of Advanced Information Science and Technology (IJAIST) Vol.23, No23, March 2014
[19] S Dinesh Kumar and Noor Mahammad Sk “A Novel SRAM Cell Design Using Reversible Logic”, 3rd International Conference on Eco-friendly Computing and Communication Systems, 2014
[20] A. Majumder, P.L Singh, B. Chowdhury, R. Rai and V. Anand “Efficient design and analysis of N-bit reversible shift registers” 3rdInternational Conference on recent Trends in Computing, 2015
[21] R. Feynman, “Quantum Mechanical Computers”, Optical News. 1985, pp. 11-20
[22] T. Toffoli., Reversible Computing, Tech memo MIT/LCS/TM-151, MIT Lab for Computer Science (1980).
[23] A. Peres, Reversible Logic and Quantum Computers, Physical Review A, vol. 32, pp. 3266-3276, 1985.

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