Performance analysis of a modified reduce component count multilevel inverter

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Abstract. Reducing component in circuitry is desirable in many innovations. In multilevel inverter (MLI) perspective, the increasing of switching devices for a higher-level output will significantly increase power losses, thus affected the output harmonic distortion. In this paper, an extended and simplified three-phase reduce component count multilevel inverter (RCCMLI) structure adapted from S. S. Lee, Cascaded Compact-Module Multilevel Inverter (CCM-MLI) is demonstrated and analysed. Symmetrical reduce component structure with H-bridge inverter is considered in this work. For simplification purpose, the current path conduction for reverse current is not demonstrated in this paper. A simulation-based result is presented to observe the performance of RCCMLI with regards to its output voltage harmonic content. Related predetermined parameter values are included in this report. Particularly, this paper verified the aforementioned RCCMLI, but in higher level and three-phase application, which will further improve the pseudo-sinusoidal inverter output as it eliminates the triplens harmonic component compare to single-phase environment. As for the lower order odd harmonics elimination, computational algorithm namely Particle Swarm Optimization (PSO) has been implemented in the RCCMLI control strategy. In comparison to the traditional Cascaded H bridge (CHB), this work finds that employing the switching angle optimization in the proposed RCCMLI produce comparable improvement in minimizing the output voltage harmonic and able to bring the output quality closer to comply with IEEE 519 distortion limit with fewer components and compact size inverter.

1. Introduction

The MLI topology is currently emerging with compact, less cost, more efficient inverter system is desirable and increasingly in demand\textsuperscript{[1]}. Multilevel inverter (MLI) usually used in high power drives \textsuperscript{[2]} and implemented in various application namely flexible AC transmission system (FACTS) devices \textsuperscript{[3]}, renewable energy sources (RES) \textsuperscript{[4]} and numerous industrial handling equipment\textsuperscript{[5]}. MLI known to eliminate harmonic efficiently by mechanical approach, making it suitable for those applications.

The invention of power switch array with dc sources to produce staircase shape signal near to sinusoidal is termed as MLI \textsuperscript{[6]}. The control switches in MLI generates output voltage per small step. Each stage-up level means the summation of an additional dc voltage than the previous level.
MLI topologies are less expensive solution and since the evolution started, many structural modifications are made to fit industries application. The sum of dc sources, power switches and components count on the MLI configuration depends on its output voltage level [7]. Cascaded H-Bridge MLI (CHB-MLI), Flying Capacitor MLI (FC-MLI) and Diode Clamped MLI (DC-MLI) are well known traditional MLI topologies [4,9,10] and later breakthrough include reduce component count MLI (RCCMLI) [6,11,12] to categorize the growing invention of modified structured and part reduction MLI.

Development of new topologies, modulation strategies and control schemes in MLI always refer back to the structural root of traditional MLI. Ideally, the way to achieve a higher-level output is by proportionally multiplying the existing sum of traditional MLIs circuit. So, the requirement of dc sources, power switches, its drivers and related protection parts are multiplied which lead to the increasing system size, complexity and price [12,13]. This problem opportune for the entrance of reduce component count (RCC) topologies. Even though many topologies have existed on the RCC, new topologies are still emerging. A large number of papers published in new MLI topology show on-going high interest in this topic as observation in Scopus database in Figure 1. The trend analysis illustrates reduce component, compact size and new MLI topology related publication in rapid growth starting 2012.

![Publication by year](image.png)

**Figure 1.** Publication in relation to multilevel structural topology evolution (2002 to 2019)

The concept of designing a new MLI topology describes by the modification of structural assembly arrangement, equal or unequal dc source and combination of component used to generate the staircase output of each level. Different researchers employ equal or unequal dc source in MLI for many reasons. Symmetric MLI as it called, for equal dc sources structure is producing equal voltage step. Despite the fact asymmetric MLI employ unequal dc sources may produce uneven stepping output and more complex control scheme, by appropriate conducting sequence, the asymmetrical MLI structure also able to yield equal step output. With that being said, this unequal arrangement able to increases the number of output level with employing fewer dc sources.

Improvement in topology structure is validated by its performance. In MLI, harmonic distortion is the famous variable in quantitively measurement of the inverter power quality. A sinusoidal harmonic distortion series in different frequencies is usually mathematically identified using Fourier representation [14]. This periodic function eased the recognition of the targeted lower harmonics group for undesired distortion elimination.

Lower order harmonics are the set of frequency approaching the fundamental component. Symmetrical signal property cancelled even harmonics, and a balanced three-phase system removed the triplen harmonics leave the 5th and 7th frequency as the most dominant odd harmonics to be eliminated. In low voltage applications for a system rated 120 V to 69 kV, harmonic distortion in the power system is targeted to meet the power quality setting by IEEE-519 standard (maximum THD, 8%) [15].
The study aims to reduce the number of component count by means power switches and drivers in compare to same level traditional CHBMLI, then further optimized by switching angles manipulation. This paper presentation is layout as; Section 2 outlines the RCCMLI topology with its basic module for extension reference of this topology and intended optimization method, Section 3 provides a quantitative comparison of the presented topology with the traditional CHBMLI to produce the same number of levels in three-phase application. Section 4 elaborates the result obtained in this study and Section 5 conclude the paper.

2. Basic structural model of the proposed topology

As per basic MLI topology, the proposed topology consists of dc sources, power switches and drivers. Equal dc sources \( V_{DC,1} = V_{DC,2} = \cdots = V_{DC,n} \) and symmetrical multilevel structure are considered for each cascaded level of this RCCMLI construction as per adaption in [16].

The basic module of the presented topology is shown in Figure 2. This design unit involves two main structure; (a) additive structure to increase level and (b) designated structure. These two structures serve its importance by switch \( S_5 \), pair switches \( S_6 - S_7 \) and pair switches \( S_i - S_{i+1} \) are switching state to produce staircase level voltage. Note that, \( S_5 \) conduction only occurs during the initial zero voltage mode.

Complementary switching conduction \( S_1 \) to \( S_4 \) in (b) is mean to isolate different polarity of power connector from short circuit. Hence, the basic unit of this topology is designated to have this arrangement.

![Figure 2. Basic module, (a) additive structure set to meet m-level MLI (b) designated structure for alternate electrical conduction](image)

*Note I, \( m \)-level \((m-1)/2 = n \); number of dc voltage, *Note II, \( i \) is subsequent value (switches)

Cascading basic structure will increase the number of levels at the output[17]. Figure 3 defines the cascaded connection of the proposed topology to form the desired level RCCMLI module. The output voltage, \( V_o \) is the sum of the voltage source generated by each additive module connected in cascade.

![Figure 3. Basic illustration of the output voltage generation for the proposed RCCMLI](image)

\[
V_{o(p)} = V_{DC,1} + V_{DC,2} + \cdots + V_{DC,n} \] (1)
2.1. Proposed RCCMLI topology demonstration

11-level RCCMLI per phase module is demonstrated as in Figure 4 as the subject in this paper analysis. Total 13 switches and 9 drivers are required for this single-phase RCCMLI application.

![Figure 4. Extended 11-level reduce component count multilevel inverter](image)

Noted in Section 2, switches in additive structure will be in conduction to project desired staircase output, while the designated each half-bridge switches will conduct in complementary on-off as illustrated in Table 1. From the tabulated sequence, it is demonstrated that complementary \( S_2 \) and \( S_4 \) only starring in positive level, while \( S_1 \) and \( S_3 \) conduct in negative output level.

| \( S_1 \) | \( S_2 \) | \( S_3 \) | \( S_4 \) | \( S_5 \) | \( S_6 \) | \( S_7 \) | \( S_8 \) | \( S_9 \) | **Staircase Output, \( V_o \)** |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | \( V_1 = V_{DC} \) |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | \( V_1 + V_2 = 2V_{DC} \) |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | \( V_1 + V_2 + V_3 = 3V_{DC} \) |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | \( V_1 + V_2 + V_3 + V_4 = 4V_{DC} \) |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | \( V_1 + V_2 + V_3 + V_4 + V_5 = 5V_{DC} \) |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | \( V_1 + V_2 + V_3 + V_4 = 4V_{DC} \) |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | \( V_1 + V_2 + V_3 = 3V_{DC} \) |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | \( V_1 + V_2 = 2V_{DC} \) |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | \( V_1 = V_{DC} \) |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | \( V_2 + V_3 + V_4 = -2V_{DC} \) |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | \( V_2 + V_3 = -V_{DC} \) |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | \( V_2 + V_3 = -V_{DC} \) |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | \( V_2 + V_3 + V_4 = -3V_{DC} \) |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | \( V_2 + V_3 = -V_{DC} \) |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | \( V_2 + V_3 = -V_{DC} \) |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | \( V_2 + V_3 = -V_{DC} \) |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | \( V_2 = -2V_{DC} \) |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | \( V_2 = -V_{DC} \) |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
2.2. Extended RCCMLI application in three-phase model

As part of the cumulative study, it is important to analyse module in three-phase application for an extended investigation. Each identical module is connected in cascade as in Figure 5 to maintain per phase modulatory by mean each phase assembled with the equivalent number of switches, drivers and dc sources. The optimization of this assembled structure is discussed in Section 3.

![Diagram](image)

**Figure 5.** Connected module of the presented multilevel inverter to perform in three-phase application

2.3. Optimization for the presented RCCMLI

The optimization technique by switching angle manipulation is known to suppress the lower order harmonics. The selected algorithm will compute the switching angles by solving the nonlinear transcendental equations [12]. The optimal switching angles for 11-level RCCMLI are obtained by defining the output voltage in limitation of switching angles; \(0 < \theta_1 < \theta_2 < \theta_3 < \theta_4 < \pi/2\). In generic, the solution focus on the symmetrical trend of quarter wave property \((0 < \pi/2)\) in which the full wave expression in the subsequent quarter is performed by the appropriate linear equation to these referral angles. The output voltage performance is defined by periodic Fourier Series up to 50th harmonic,

\[
THD_v = \sqrt{\sum_{n=5,7,11...(2n+1)}^{}(V_n)^2} / V_1
\]  

Mostly, the main intention of harmonic filtration is to eliminate the lower order harmonics from the output waveform. Computational based Particle Swarm Optimization (PSO) algorithm as presented in[18,19] is used to find the optimal switching angles. According to [20] PSO is utilized for regulating the output voltage and to enhance the harmonic profile which controlling the linearity of switching angle and result in lower THD value.

By selecting the \(n^{th}\) lower odd harmonic elimination in the transcendental equation, a series of switching angle values are retrieved (outlined in Table 2). This study selected modulation values, \(m_a = 0.75, 0.87\) and \(0.92\), as these three \(m_a\) applications give the lowest harmonic effect. The THD attainment is presented in section 4.

| \(m_a\) | \(\theta_1\) | \(\theta_2\) | \(\theta_3\) | \(\theta_4\) | \(\theta_5\) |
|---|---|---|---|---|---|
| 0.75 | 12.75 | 21.02 | 35.78 | 56.50 | 61.39 |
| 0.87 | 1.00 | 10.14 | 19.63 | 26.90 | 42.73 |
| 0.92 | 2.38 | 9.35 | 19.62 | 25.96 | 41.60 |
3. Physical structure comparison of RCCMLI versus CHBMLI

A quantitative structural comparison of presented RCCMLI with CHBMLI (three-phase module) is depicted in Table 3. By this evaluation, it is shown that a significant number of switches and drivers are reduced by implementing the proposed RCCMLI structure for a same output level.

| Type                  | Conventional CHBMLI | RCCMLI |
|-----------------------|----------------------|--------|
| No. of level          | 21                   | 21     |
| No. of DC Sources     | 15                   | 15     |
| No. of switches       | 60                   | 42     |
| No. of drivers        | 60                   | 27     |

Table 3. CHBMLI versus RCCMLI component count

4. Simulation Result

The analysis model for the extended three-phase RCCMLI is performed in PSIM environment. Related parameters are predetermined to perform the simulation analysis (as in Table 4). The main performance index measure in this experiment is the total harmonic distortion (THD). Presented result show three-phase line to line output voltage waveform and Fast Fourier Transform (FFT) for \( m_s \) 0.75, 0.87 and 0.92. The extended RCCMLI is able to generate in total 21-level staircase output as shown in Figure 6(a), 7(a) and 8(a) respectively. The projected switching angles which eliminate targeted odd harmonics result in significant system improvement approximately around 5% (4.31, 3.98 and 3.78 respectively). Lower THD value is achieved by this triplens and non-triplens low order harmonic elimination as illustrate in FFT analysis in corresponding Figure 6(b), 7(b) and 8(b).

| Parameter Type     | Value |
|--------------------|-------|
| \( R_{\text{Load}} \) | 100 \( \Omega \) |
| \( V_{\text{DC}} \)  | 100 V  |
| Fundamental frequency, \( f_s \) | 50 Hz |

Table 4. Predetermined simulation parameters.
Figure 6(a). 21-level three-phase line to line output voltage by $m_a = 0.75$ application

Figure 6(b). FFT analysis of 21-level three-phase line to line output voltage by $m_a = 0.75$ application
Figure 7(a). 21-level three-phase line to line output voltage by $m_a = 0.87$ application

Figure 7(b). FFT analysis of 21-level three-phase line to line output voltage by $m_a = 0.87$ application
Figure 8(a). 21-level three-phase line to line output voltage by $m_a = 0.92$ application

Figure 8(b). FFT analysis of 21-level three-phase line to line output voltage by $m_a = 0.92$ application

In compliance of IEEE 519 standard, the output THD profile is targeted to meet at least 5% distortion limit. Optimization implementation in both structure as in Table 5 shows the highest distortion 4.31% is achieved by $m_a = 0.75$ while more effective output 3.78% THD is obtained by $m_a = 0.92$. The first substantial lower odd distortion shown on the 17th harmonic frequency of the FFT spectrum.

| Optimal Angle | THD (%) | THD (%) |
|---------------|---------|---------|
| $m_a = 0.75$  | 4.31    | 4.31    |
| $m_a = 0.87$  | 3.98    | 3.98    |
| $m_a = 0.92$  | 3.78    | 3.78    |
5. Conclusion

This paper shows the extendable of RCCMLI topology in three-phase applications with resistive load in 21-level output. The successful system optimization fulfilled the harmonic reduction verdict with the lowest harmonic profile is 3.78%. The result analysis shows the THD value is decrease with significant reduction of power switches (only 42 power switches and 27 drivers) compared to the same level conventional cascaded H-bridge multilevel inverter with the sum of 60 power switches and 60 drivers.

Acknowledgments

The authors would like to acknowledge School of Electrical System Engineering, Universiti Malaysia Perlis for the funding of this publication.

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