Liquid Si-induced 4H-SiC surface structuring using a sandwich configuration

Y. Jousseame\textsuperscript{1,a}, F. Cauwet\textsuperscript{1,b}, G. Ferro\textsuperscript{1,c}

\textsuperscript{1}Laboratoire des Multimateriaux et Interfaces, Université de Lyon, 6 rue Victor Grignard, 69622 Villeurbanne, France
\textsuperscript{a}yan.jousseame@univ-lyon1.fr, \textsuperscript{b}francois.cauwet@univ-lyon1.fr, \textsuperscript{c}gabriel.ferro@univ-lyon1.fr

Despite the attractive properties and already wide use of silicon carbide for power electronics, the performances of SiC metal-oxide-semiconductor field effect transistors (MOSFETs) remain limited due to low channel mobility. Electrically active defects at the SiO\textsubscript{2}/SiC interface are being held accountable for this limitation. While the origin of these interface defect states (D\textsubscript{a}) is still under debate, recent experimental studies attribute them to the stepped morphology inherent to commonly used off-axially grown epitaxial surfaces [1]. Indeed, step-controlled growth induces the formation of so-called microsteps on the substrate surface, and that of macrosteps resulting from microsteps bunching [2]. Such a morphology is expected to crucially impact the creation of the SiO\textsubscript{2}/SiC interface as the thermal oxidation process is related to crystallographic orientation. This could eventually initiate non-ideal oxidations and nonstoichiometric near-interface regions [3].

Recent studies have shown that a MOS capacitor fabricated on macrostepped surfaces shows a systematic decrease of Dit of \textasciitilde 10-15\% compared to “standard” samples [4]. A simple way for fabricating such 4H-SiC macrostepped surface is to put it in contact with a liquid Si drop [5,6]. The induced atomic rearrangement reconstructs the 4°off surface with parallel terraces of a few \(\mu\)m width. But if such Si drop approach works for \textasciitilde 1 cm\textsuperscript{2} area, its extrapolation to industry-scale areas (full 4-6” wafer) is clearly not feasible. That is why one needs to investigate a set-up where the liquid silicon would be more spread out on the SiC surface.

In the present work, a sandwich configuration (Fig. 1) is used, where a bulk piece of silicon is melted between two 4H-SiC (0001) 4°off Si-face wafers. The experiments are performed at 1550-1600°C for 15-120 min in a homemade vertical cold wall CVD reactor working under H\textsubscript{2} or Ar atmosphere. The effects of liquid-solid interaction duration and temperature on SiC surface morphology are being explored.

Fig. 2 shows a typical result obtained using this configuration. Both top and bottom SiC wafers of the sandwich display systematically terraces with average 2-4 \(\mu\)m widths (Fig 2.a), while the straightness of the steps is generally unequally distributed along the liquid-solid interaction area of the substrates. An interesting feature of these restructured surfaces resides in the dissolution and growth pattern. The bottom SiC wafer being directly in contact with the graphite susceptor that heats the sandwich, it is expected to be hotter than the top SiC wafer, and therefore dissolution should occur on the bottom substrate. Carbon should then be transported in the liquid silicon along the thermal gradient up to the top SiC wafer where growth would occur. The observed trend is however quite divergent. For a sample treated at 1550°C for 30 min with \textasciitilde 400 \(\mu\)m of molten silicon thickness, the profile of the bottom SiC wafer shows trenches along the edges of the liquid-solid interaction area with a depth of several micrometers, and growth zones of the same order of magnitude at the center. Regarding the top SiC wafer of the same sample, a similar shape is observed: both top and bottom wafers exhibit a butterfly-like topography (Fig 2.b). In such set-up, the transport of carbon within the molten silicon seems to occur from the edges to the center of the same SiC wafer rather than from the hottest surface to the coldest one, raising interrogations on which factors actually drive the dissolution and growth mechanisms in this configuration.

Lastly, the straightest steps and largest terraces are for the most part observed on growth zones of the substrates reconstructed surfaces. The effects of experimental parameters such as time and temperature treatment on the surface topography and on the step bunched morphology will be discussed.
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Fig. 1. Schematic of the investigated sandwich set up and expected thermal gradient direction.

(a) [Image]

(b) [Image]

Fig. 2. a) Optical images and b) 3D profilometry maps of the reconstructed surfaces of the bottom (left) and top (right) 4H-SiC wafers after liquid Si interaction at 1550°C for 30 min with ~400 µm of molten Si thickness.