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4-bit digital to analog converter using R-2R ladder and binary weighted resistors

J. Diosanto¹, M.L. Batac², K.J. Pereda³, R. Caldo⁴
Gokongwei College of Engineering, De La Salle University, 2401 Taft Ave, Malate, Manila, 1004 Metro Manila, Philippines
E-mail: ¹jocelyn_diosanto@dlsu.edu.ph, ²marielle_batac@dlsu.edu.ph, ³krizzle_pereda@dlsu.edu.ph, ⁴rionel.caldo@dlsu.edu.ph

Abstract. The use of a 4-bit digital-to-analog converter using two methods; Binary Weighted Resistors and R-2R Ladder is designed and presented in this paper. The main components that were used in constructing both circuits were different resistor values, operational amplifier (LM741) and single pole double throw switches. Both circuits were designed using MULTISIM software to be able to test the circuit for its ideal application and FRITZING software for the layout designing and fabrication to the printed circuit board. The implementation of both systems in an actual circuit benefits in determining and comparing the advantages and disadvantages of each. It was realized that the binary weighted circuit is more efficient DAC, having lower percentage error of 0.267% compared to R-2R ladder circuit which has a minimum of percentage error of 4.16%.

1. Introduction
Connecting digital circuitry to sensor devices is simple if the sensor devices are inherently digital themselves. Switches, relays, and encoders are easily interfaced with gate circuits due to the on/off nature of their signals. However, when analog devices are involved, interfacing becomes much more complex. What is needed is a way to electronically translate analog signals into digital (binary) quantities, and vice versa [1]. In communication system, digital transmission is faster and convenient but the digital signals should be converted back to analog signals at the receiving terminal [2]. This paper focuses on the digital to analog converter, implementing two different circuit designs.

Fig 1: Block Diagram of a Digital-to-Analog Converter

DACs can be used in applications such as it can be found in the processing of computer data by a modem into audio-frequency tones that is transmitted over the use of telephone lines. DAC is common in music players, throughout its use for the generation of audio signals from the digital information. While for the use of TVs and cellular phones, the digital video signals are converted into analog to
display colors and shades. In VoIP applications, the source is first digitized for the transmission through an ADC and is reconstructed back using DAC at its receiving end [4].

1.1 Binary Weighted Resistors
The binary weighted resistors DAC consist of \( n \) number of switches, one for each bit applied to the input. The resistors for the binary weighted DAC are inversely proportional to the numerical significance of the corresponding binary digital. A reference voltage and a summing amplifier is to be used that adds current flowing to the resistive network. The current that flows can develop a signal that is proportional to its digital input. Its advantage is considered as an economical D/A converter as it is simple in construction [5] on the resistor network due to the number of resistors that are in the circuit as well as it can provide faster conversion time. It also has disadvantages wherein having resistors with wide range of values, thus having difficulty to ensure the absolute accuracy and stability of all the resistors as well as matching the temperature coefficient of all the resistors. This factor is especially important in D/A converters operation over a wide temperature range. Equation 1 shows the computation for the output voltage of the binary weighted resistors.

\[
V_o = \left[ a_1 2^{n-1} + a_2 2^{n-2} + a_3 2^{n-3} + \cdots + a_n \right] \frac{V_R}{2^n} \quad \text{(eqnt. 1)}
\]

1.2 R-2R Ladder Resistor
An alternative to the binary weighted input DAC is the R-2R Ladder, which uses fewer unique resistor values thus does not require precision resistors. A disadvantage of the former DAC design was its requirement of several different precise input resistor values: one unique value per binary input bit [3]. Its advantage comparing to the binary weighted is it only has two values of resistors, thus the actual values used is relatively less important if it is extremely large values. The staircase voltage result is more likely to be monotonic as the effect of the MSB resistor is not many times greater than that for LSB resistor [2].

\[
V_o = \frac{R_f}{R_o} \frac{N}{2^n} V_R = \frac{N}{2^n} V_R \quad \text{(eqnt. 2)}
\]

2. Objectives
The expected output for this research are stated below:
1. To design a 4-Bit Digital to Analog converter using R-2R Ladder
2. To design a 4-Bit Digital to Analog converter using Binary Weighted Resistors
3. To compare the output of both circuits to determine which of the two methods is more accurate and efficient to use as a Digital-to-Analog converter

3. Project Specification
3.1 Materials
In the construction of the circuit for this research, the components enumerated below are needed for a 4-bit Digital to Analog converter circuit along with the materials for the fabrication of both circuits.
- LM741
- 1kΩ resistor
- 1.25kΩ resistor
- 2.5kΩ resistor
- 5kΩ resistor
- 10kΩ resistor
- 20kΩ resistor
- Single Pole Double Throw Switches
- 3.5x2.5 PCB
- Ferric chloride
- Connecting wires
3.2 Circuit Design

3.2.1 MULTISIM Layout. The circuits shown in Figure 2 and Figure 3 are simulated through the design software, Multisim. The digital-to-analog converter circuit design uses different resistor values and an operational amplifier with the value of LM741.

- Binary Weighted Resistors

![Binary Weighted Resistors](image1)

Fig 2: Simulation of a DAC using Binary Weighted Resistors using MULTISIM

- R-2R Ladder

![R-2R Ladder](image2)

Fig 3: Simulation of a DAC using R-2R Ladder using MULTISIM

3.2.2 Fritzing Layout for PCB

![Fritzing Layout for PCB](image3)

Fig 4: Fritzing Layout for PCB

The layout design shown in Figure 4 is simulated through an open-source designing software tool called Fritzing. Fritzing is used to design the schematic circuit; the layout consists of both the binary weighted resistors and the R-2R Ladder circuit. These layout designs will be used for the fabrication of the circuit in printed circuit board.

3.2.3 Printed Circuit Board (PCB) Layout. Figure 5 shows the binary weighted resistors and the R-2R Ladder circuit on the PCB. The PCB was etched and drilled in accordance to the layout design in
Figure 4, followed by soldering the components into the board. Lastly, the circuit was evaluated to check if it has proper connections.

![Fig 5: PCB Layout](image)

3.2.4 Testing Set-up. Figure 6 shows the testing set-up of the fabricated R-2R Ladder and Weighted Binary circuit. This process helped in determining failed connections, and proper layout circuit. Testing the circuit helps in determining the output of the DAC, thus, identifying its proper use as well as its advantages and disadvantages.

![Fig 6: Testing Set-up](image)

4. Data and Results

| Table 1: DAC using Binary Weighted Resistors Results |
|---------------------------------------------------|
| 4-Bit Digital to Analog Converter using Binary Weighted Resistors |
| **Input** | **Ideal (V)** | **Actual (V)** | **Percentage Error (%)** |
|-----------------|-----------------|-----------------|--------------------------|
| 0000            | 0.000           | 0.009           | ----                     |
| 0001            | -0.500          | -0.491          | 1.800                    |
| 0010            | -1.000          | -0.969          | 3.100                    |
| 0011            | -1.500          | -1.469          | 2.067                    |
| 0100            | -2.000          | -2.016          | 0.800                    |
| 0101            | -2.500          | -2.516          | 0.640                    |
| 0110            | -3.000          | -2.992          | 0.267                    |
| 0111            | -3.500          | -3.490          | 0.286                    |
| 1000            | -4.000          | -3.872          | 3.200                    |
| 1001            | -4.500          | -4.373          | 2.822                    |
| 1010            | -5.000          | -4.848          | 3.040                    |
| 1011            | -5.500          | -5.346          | 2.800                    |
| 1100            | -6.000          | -5.890          | 1.833                    |
| 1101            | -6.500          | -6.380          | 1.846                    |
| 1110            | -7.000          | -6.860          | 2.000                    |
| 1111            | -7.500          | -7.350          | 2.000                    |
Table 1 shows the results gathered from the DAC binary weighted resistors circuit. It includes the ideal and the actual voltage output of the given digital inputs. The theoretical least significant bit value is -0.5V while the actual least significant value is -0.491V. It can be seen on Table 1 that the binary weighted resistor circuit has a minimum percentage error of 0.267% and the maximum percentage error is 3.2%.

Table 2: DAC using R-2R Ladder Results

| Input | Ideal (V) | Actual (V) | Percentage Error (%) |
|-------|-----------|------------|----------------------|
| 0000  | 0         | 0          | ----                 |
| 0001  | -0.625    | -0.669     | 7.040                |
| 0010  | -1.250    | -1.302     | 3.600                |
| 0011  | -1.875    | -1.970     | 5.067                |
| 0100  | -2.500    | -2.629     | 5.160                |
| 0101  | -3.125    | -3.297     | 5.504                |
| 0110  | -3.750    | -3.930     | 4.800                |
| 0111  | -4.375    | -4.597     | 5.704                |
| 1000  | -5.000    | -5.216     | 4.320                |
| 1001  | -5.625    | -5.884     | 4.604                |
| 1010  | -6.250    | -6.520     | 4.320                |
| 1011  | -6.875    | -7.180     | 4.436                |
| 1100  | -7.500    | -7.840     | 4.533                |
| 1101  | -8.125    | -8.510     | 4.738                |
| 1110  | -8.750    | -9.140     | 4.457                |
| 1111  | -9.375    | -9.810     | 4.640                |

Table 2 shows the results that was attained using the DAC R-2R ladder circuit. It states the ideal and the actual voltage outputs of the given digital inputs. The least significant bit of the input, has a value of -0.625V theoretically while its actual result with the use of the circuit was -0.669V. With the difference of both the ideal and actual values, it can be seen on Table II that the R-2R Ladder Circuit has a minimum of 4.16% and the maximum percentage error is 7.04%

5. Analysis

In accordance to the results gathered, the proponents determined that the digital-to-analog circuit using binary weighted resistors is more accurate than the R-2R Ladder. For the completion of the research, the percentage error was computed by comparing the actual results with the theoretical values. Figure 7 shows the table of the comparison of these errors.
Binary Weighted Resistors provide better results because this circuit delivers faster conversion time compared to the R-2R Ladder Circuit. However, the R-2R Ladder is cheaper since it only uses two values of resistors while the binary weighted resistors use more values of resistors and these values are usually not available in the market. The group had to series different values of resistors to get the exact values needed for the binary weighted resistors. Other factors are to be considered as well on determining which circuit is more efficient, but in considering the resistor values of both circuits, the use of the R-2R ladder circuit is more practical in converting digital to analog.

6. Conclusion

In conclusion, the researchers were able to design a digital to analog converter using two different circuits. A DAC using R-2R Ladder was designed and implemented having only two different values of resistors, thus having an advantage based on the number of components unlike the binary weighted resistors DAC wherein different resistor values were used hence having difficulty in attaining the needed output required. In addition to that, both circuits were monotonic. Nevertheless, both circuits were properly designed, fabricated, tested and compared in this research and in conclusion, the binary weighted circuit is considered as a much more efficient DAC circuit as shown in Figure 7 having a lower percentage error and converts faster compared to the R-2R Ladder circuit despite the latter having easier resistor values.

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