Interleaved entropy coders

Fabian Giesen

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Abstract

The ANS family of arithmetic coders developed by Jarek Duda has the unique property that encoder and decoder are completely symmetric in the sense that a decoder reading bits will be in the exact same state that the encoder was in when writing those bits—all “buffering” of information is explicitly part of the coder state and identical between encoder and decoder. As a consequence, the output from multiple ABS/ANS coders can be interleaved into the same bitstream without any additional metadata. This allows for very efficient encoding and decoding on CPUs supporting superscalar execution or SIMD instructions, as well as GPU implementations. We also show how interleaving without additional metadata can be implemented for any entropy coder, at some increase in encoder complexity.

1 Introduction

Duda’s recent paper [3] describes a family of entropy coders based on what he calls “Asymmetric numeral systems” (ANS for short). They are closely related to conventional arithmetic coders [8] or “range coders” [7] and have very similar coding performance. However, the underlying construction is quite different: classical arithmetic coders conceptually view the bitstream as encoding a dyadic fraction in [0, 1), and proceed by a process of interval subdivisions. “Infinite-precision” ANS encoders, by contrast, view the bitstream as a single integer $x \in \mathbb{N}$ that encodes the entire message, where the coded symbols are derived from the value of the remainder $x \mod m$ for some integer $m$. Finally, “streaming” ANS encoders perform the same process using fixed-width integer arithmetic ($x < 2^p$ for some integer $p$; often $p = 32$ or $p = 64$ for machines with 32- or 64-bit word sizes, respectively), which allows for efficient implementations.

Streaming ANS coders are based on a fairly unique construction that ensures that a decoder reading bits will always be in the exact same state
the corresponding encoder was in while writing these bits; all buffering of
“not yet final” bits is completely identical between encoder and decoder.
This property makes it possible to run multiple encoders concurrently and
interleave them into a single bit stream in a way that can be reconstructed
on the decoder side without additional metadata. The decoder can likewise
read these multiple interleaved streams concurrently, provided the streams
are independent. The resulting algorithms are both simple and efficient, and
can be vectorized given a suitable instruction set.

We will first review ANS coders and their unique construction. It will
be shown how they can be interleaved easily, and how this property can be
exploited for SIMD and GPU applications.

2 Streaming ANS coding

Let \( A := \{0, 1, \ldots, n - 1\} \) be a finite symbol alphabet. Furthermore, let
\( \{p_s\}_{s \in A} \) be the probabilities of the respective symbols, \( \sum_{s \in A} p_s = 1 \). In
ANS, the encoding and decoding processes revolve around a pair of functions

\[
C : A \times \mathbb{N} \to \mathbb{N}
\]

and

\[
D : \mathbb{N} \to A \times \mathbb{N}.
\]

\( C \), the coding function, takes a symbol \( s \) and the current state \( x \) and pro-
duces a new value \( x' = C(s, x) \) that encodes both the new symbol \( s \) and the
original state \( x \). \( D \), the decoding function, is \( C \)'s inverse: \( D(x') = (s, x) \) and
\( C(D(x)) = x \). Different choices of \( C \) and \( D \) correspond to different coder
variants; \cite{3} covers a wide variety of options with different constraints on the
alphabet and probability distributions, and different trade-offs of memory
usage vs. computational complexity.

By construction, \( x \) acts like a stack: the last value encoded will be first
value returned by the encoder. This is a direct result of \( D \) being the inverse
of \( C \), since for example:

\[
D(C(b, C(a, x))) = (b, C(a, x))
\]

The same also holds for the encoded bit stream: the last bits written by
the encoder will be consumed first by the decoder. This article will use the
convention that the encoder processes symbols backwards, from last to first,
and also writes the bit stream backwards, while the decoder runs forwards.
Algorithm 1 Streaming ANS decoder/encoder

Require: \( x \in I \)

Ensure: \( x \in I \)

function \textsc{Decode}(iobuf)
  \[ s, x \leftarrow D(x) \]
  while \( x \not\in I \) do
    \[ x \leftarrow bx + \text{iobuf.read()} \]
  end while
  return \( s \)
end function

procedure \textsc{Encode}(s,iobuf)
  \[ \text{while } C(s,x) \not\in I \text{ do} \]
  \[ \text{iobuf.emit}(x \mod b) \]
  \[ x \leftarrow \lfloor x/b \rfloor \]
  \[ \text{end while} \]
  \[ x \leftarrow C(s,x) \]
end procedure

As more and more symbols get encoded into \( x \), its value will, eventually, grow beyond all bounds. But for an efficient implementation, we must have fixed bounds on the size of \( x \); usually \( x < 2^p \) for some \( p \). To this end, we define a “normalized interval”

\[
I := \{L, L + 1, \ldots, bL - 1\}
\]

where \( L \) is an arbitrary positive integer and \( b \) an integer \( \geq 2 \) that defines the “radix” of the coder: a coder with \( b = 2 \) emits individual bits, one with \( b = 256 \) writes 8-bit bytes at a time, and so forth. We then require that both encoder and decoder maintain the invariant that \( x \in I \), by writing some of the bits from \( x \) and reducing it when it gets too large in the encoder, or reading additional bits when it gets too small in the decoder. Algorithm 1 illustrates the general idea. Note that the encoder is the exact inverse of the decoder: it performs the inverses of the individual decoder steps, in reverse order. The final state of the encoder (which corresponds to the state after coding the first symbol in the message, since the encoder iterates over the message backwards) needs to be transmitted along with the rest of the bitstream so the decoder knows what state to start in.

It is not at all clear that this approach works, and in fact given an arbitrarily chosen pair of mutually inverse \( C \) and \( D \) it usually will not. For example, given an arbitrary \( C \), there is no guarantee that the loop in \textsc{Encode} will terminate, or that encoder and decoder will always go through the same sequence of states \( x \). However, it can be shown that if the precursor sets

\[
I_s := \{x \mid C(s,x) \in I\}
\]

are of the form \( I_s = \{k, k + 1, \ldots, bk - 1\}, k \geq 1 \)—a property that Duda calls “\( b \)-uniqueness” in [3]—the encoder and decoder in algorithm 1 will stay
synchronized. Duda gives several general constructions (uABS, rANS/rABS, tANS/tABS) that are guaranteed to produce valid $C$ for different types of alphabets and probability distributions. For the purposes of this paper, it does not matter which particular $C$ is chosen.

2.1 Example

For a concrete example, suppose we wish to code a message from the two-symbol alphabet $A = \{a, b\}$ with $p_a = 1/4$, $p_b = 3/4$. We define:

$$C(a, x) = 4x$$

$$C(b, x) = 4\lfloor x/3 \rfloor + (x \text{ mod } 3) + 1$$

Note that $a$ gets sent to values that are divisible by 4, whereas $b$ gets sent to values that are not. Furthermore, in both cases, the original value of $x$ is easy to recover from the new value, and we have the straightforward inverse:

$$D(x) = \begin{cases} 
(a, x/4) & \text{if } x \equiv 0 \mod 4, \\
(b, 3\lfloor x/4 \rfloor + (x \text{ mod } 4) - 1) & \text{otherwise.}
\end{cases}$$

When an $a$ is coded using $C$, $x$ grows by a factor of $4 = 1/p_a$; when a $b$ is coded, $x$ grows by a factor of approximately $4/3 = 1/p_b$. More generally, in an ANS coder, coding the symbol $s$ will grow $x$ by a factor of approximately $1/p_s$. This is a rough equivalent to the size of the range in a regular arithmetic coder, which shrinks by a factor of approximately $p_s$ for every coded symbol.

Now suppose we define $L = 16$ and $b = 2$, making our normalization interval $I = \{16, 17, \ldots, 31\}$. Some computation shows that $a$ and $b$’s precursor sets are given by

$$I_a = \{4, 5, 6, 7\}$$

$$I_b = \{12, 13, \ldots, 23\}$$

and both of them are $b$-unique. Therefore, algorithm 1 is guaranteed to work. Figure 1 on page 5 shows a worked-through example of encoding, then decoding, the message “babba” with this choice of parameters. Note that encoder and decoder go through the same sequence of states, just in opposite order. This is true by construction, since encoder and decoder are designed as exact inverses of each other. The rest of this paper describes several ways to exploit this fact.
| Encoder | x (state) | Decoder |
|---------|-----------|---------|
| write final state | read final state | |
| $\uparrow$ | $\downarrow$ | $\downarrow$ |
| encode 'b' | decode 'b' | |
| $\uparrow$ | $\downarrow$ | $\downarrow$ |
| $x \not\in I_b$; emit(0) | $x \not\in I$; read()=0 | |
| $\uparrow$ | $\downarrow$ | $\downarrow$ |
| encode 'a' | decode 'a' | |
| $\uparrow$ | $\downarrow$ | $\downarrow$ |
| $x \not\in I_a$; emit(1) | $x \not\in I$; read()=1 | |
| $\uparrow$ | $\downarrow$ | $\downarrow$ |
| $x \not\in I_a$; emit(0) | $x \not\in I$; read()=0 | |
| $\uparrow$ | $\downarrow$ | $\downarrow$ |
| encode 'b' | decode 'b' | |
| $\uparrow$ | $\downarrow$ | $\downarrow$ |
| encode 'b' | decode 'b' | |
| $\uparrow$ | $\downarrow$ | $\downarrow$ |
| encode 'a' | decode 'a' | |
| $\uparrow$ | $\downarrow$ | $\downarrow$ |
| $x \not\in I_a$; emit(0) | $x \not\in I$; read()=0 | |
| $\uparrow$ | $\downarrow$ | $\downarrow$ |
| $x \not\in I_a$; emit(0) | $x \not\in I$; read()=0 | |
| $\uparrow$ | $\downarrow$ | $\downarrow$ |
| initial state | (all done) | |

$L = 16, b = 2, I = \{16, 17, \ldots, 31\}$

$C(a, x) = 4x$

$I_a = \{4, 5, 6, 7\}$

$C(b, x) = 4\lfloor x/3 \rfloor + (x \mod 3) + 1$

$I_b = \{12, 13, \ldots, 23\}$

$D(x) = \begin{cases} 
(a, x/4) & \text{if } x \equiv 0 \mod 4, \\
(b, 3\lfloor x/4 \rfloor + (x \mod 4) - 1) & \text{otherwise.}
\end{cases}$

Figure 1: ANS example: Coding “babba” with $p(a) = 1/4$, $p(b) = 3/4$. Encoder proceeds from bottom to top, decoder from top to bottom (as indicated). Both go through the exact same sequence of states and perform I/O in the same places.
3 Interleaving ANS coders

Streaming ANS, as constructed above (and illustrated in the example), has the rather unique property that decoder and encoder perform the same sequence of state transitions and do IO operations at the exact same time (except for the encoder doing it all in reverse order, that is).

The decoder does not only produce the original message that was passed into the encoder; it produces it by “unwinding” all operations performed by the encoder, one by one. After decoding the \(i\)th symbol \(s_i\) in the message, the decoder “winds back time” to the state the encoder was in right before it encoded symbol \(s_{i+1}\).

Thus, encoder and decoder are always in lockstep. Regular arithmetic coders do not have this property: the decoder is always ahead of the encoder, in the sense that the decoder’s state while decoding \(s_i\) will already contain bits that the encoder only sent after \(s_i\) was encoded—sometimes, much later. The resulting asymmetry makes it hard to mix arithmetic-coded with non-arithmetic-coded data in the same bit stream without performing an expensive (in terms of rate) flush operation—motivating designs like the “bypass coding mode” in CABAC [6], a special fast path in a binary arithmetic coder to accelerate encoding (and decoding) of near-equiprobable binary symbols.

With ANS, this is not an issue. Because the decoder and encoder proceed in lockstep, an encoder can just write raw bits (bytes, …) into the output bitstream whenever it makes sense; the decoder will be at the same position in the bitstream at the same time and there is no need for an explicit bypass coding mechanism. For example, suppose that in figure 1, we have four different “subtypes” of symbol \(a\) called \(a_0\) through \(a_3\), all of which are equally likely. In a regular arithmetic coder, we would need to use a bypass mechanism to encode the two bits denoting which of the four types it is. In an ANS coder, we can just agree that after reading an \(a\), the decoder will read two additional bits that denote the subtype—and likewise, that before encoding an \(a\), the encoder sends the subtype number using two bits.

Suppose we do just this in figure 1, for the first \(a\) in the message. After decoding \(a\), the decoder is in state 30—the same state the encoder was in before encoding the \(a\). Writing and reading our two extra bits as just described corresponds to inserting an extra row right below state 30: the encoder emits two bits, and the decoder reads two bits. The two sides are still perfectly symmetric; unique decodability is still guaranteed.

By the same argument, a bitstream can interleave not just an ANS coder with a “raw” binary coder, but also multiple ANS coders—or, in fact, any
mixture of ANS and raw binary coders. By “interleave”, I mean that there are two or more distinct decoders with distinct states reading from (or likewise, two or more encoders with distinct states writing to) the same buffer:

\[
\begin{align*}
s_1 & \leftarrow \text{coder1}.\text{Decode}(\text{iobuf}) \\
s_2 & \leftarrow \text{coder2}.\text{Decode}(\text{iobuf})
\end{align*}
\]

No additional metadata is necessary for this, provided that the sequence of coders and models used is the same between encoder and decoder.

The advantage of using distinct coders (with distinct states) over just having different models is that they are truly independent and can be processed concurrently, provided that their probability distributions are either static or evolve independently. This allows for faster implementations on superscalar processors, and, once we interleave a larger number of streams—say somewhere between 4–64—also enables use of SIMD instructions or even performing entropy coding on a GPU. We will cover both these use cases shortly.

Interleaving multiple streams is not a panacea; the “independent model evolution” requirement precludes certain kinds of context models. It is, however, very interesting for applications such as image and video coding that deal with large amounts of data that have a homogeneous structure (e.g. transform coefficients) and are generally coded using independent contexts anyway.

4 Interleaving arbitrary entropy coders

Note that any entropy coder can, without modification, support the less constrained scenario

\[
\begin{align*}
s_1 & \leftarrow \text{coder1}.\text{Decode}(\text{iobuf1}) \\
s_2 & \leftarrow \text{coder2}.\text{Decode}(\text{iobuf2})
\end{align*}
\]

where “iobuf1” and “iobuf2” correspond to two physically distinct streams. However, this is not quite equivalent: say we want to produce a single output, like a file or a TCP stream. Multiplexing these multiple streams into a single container requires extra work, and it’s not obvious that this can be done without additional metadata at all.

But in fact, the design of ANS shows precisely how an encoder can be modified to support such “free” interleaving. The key to the normalization procedure in algorithm 1 is that the encoder knows precisely how the decoder will react to any given input.

We can do the same thing with any entropy coder: it may not be practical to make the encoder directly aware of exactly what the decoder will do,
but luckily this is not necessary—the encoder can just run (simulate) the decoder to figure out what the actual sequence of reads will be.

To elaborate: suppose we have a multi-stream encoder as above, writing data into multiple buffers, one per stream. Then, to produce the final bitstream, the encoder runs an instrumented version of the decoder. For simplicity, suppose we have two streams, one of which receives the symbols at even positions, with the other one receiving the symbols at odd positions. Then we run the instrumented decoder:

\[
s_1 \leftarrow \text{coder1.DecodeInstrumented}(\text{iobuf1, iobuf_mux})
\]

\[
s_2 \leftarrow \text{coder2.DecodeInstrumented}(\text{iobuf2, iobuf_mux})
\]

Here, \text{DecodeInstrumented} is just a slightly modified version of \text{Decode} (for whatever entropy coder is used): it reads from the stream passed in as its first argument, but whenever it reads something, it immediately writes that value to the buffer given as the second argument.

Once the instrumented decoder finishes, \text{iobuf_mux} contains the bits from all streams, in exactly the order that the decoder on the receiving end will be trying to read them. Moreover, it is not necessary to wait for all streams to “finish” before starting the instrumented decoder; it can run along with the encoders as a coroutine, and one might hope that doing so can reduce the memory requirements to a constant amount of storage per stream. However, there is a small catch; suppose the encoder does something like:

\[
\text{for } i \leftarrow 1 \text{ to } 1000000 \text{ do}
\]

\[
\text{coder2.Encode}(s_i, \text{iobuf2})
\]

\[
\text{end for}
\]

\[
\text{coder1.Flush(\text{iobuf1})}
\]

\[
\text{coder2.Flush(\text{iobuf2})}
\]

In this case, it is highly likely that an instrumented decoder running as a coroutine will get stuck reading the very first symbol, right until the very end when coder1 calls \text{Flush}; thus, the instrumented decoder will not actually make any forward progress until the entirety of “iobuf2” has been written, and the encoder will require enough memory to buffer all of it. This can happen whenever the output rates of different streams are highly un-balanced.

We can reduce these memory requirements to a predictable amount by requiring flushes periodically; say we flush at least once every million symbols. This resolves the problem and guarantees bounded memory usage, at the cost of some increase in bit rate.
This approach is fully general and works with any entropy coder; that said, encoding to multiple streams (and then later running the instrumented decoder to produce the final bit stream) adds extra buffering and complexity to the encoder; worst-case memory usage is proportional to the size of the output data. The situation with ANS is similar: Its reverse encoding requirement means that in practice, the input streams will have to be buffered in some way, at (generally) even higher cost in memory than the output streams would be. However, interleaving ANS streams is simple on both the encoder and decoder sides; this simplicity enables efficient vectorized implementations.

5 SIMD implementation

Algorithm 1 is written as a serial program; however, like any serial program, it can be systematically converted into vectorized form: integer arithmetic turns into arithmetic on vectors of integers, memory loads and stores turn into gather/scatter operations, and control flow can be turned into SIMD data flow by using predication; see e.g. [4] for details.

This (entirely mechanical) process is guaranteed to preserve the meaning of the original program if (and only if) there are no data dependencies between the computations running simultaneously in different SIMD lanes.

Assuming that static models are used, $C$ and $D$ are pure functions and free of side-effects; they can be vectorized safely. For adaptive models, they can still be vectorized safely as long as no two SIMD lanes ever try to update the same model at the same time; one way to ensure this is to keep separate contexts for every SIMD lane.

Once $C$ and $D$ are taken care of, the only remaining problem is how to implement the emit and read operations in the encoder and decoder, respectively.

For concreteness, suppose $b = 2^8 = 256$ (i.e. byte-aligned IO) and that the target SIMD width is $N = 4$. Listing 1 illustrates how such a decoder can be implemented.

This code uses the following utility functions:

- $x = \text{select}(a, b, \text{cond})$ is a SIMD version of C’s ternary operator: $x_i = b_i$ if $\text{cond}_i = \text{true}$, $x_i = a_i$ otherwise.
- $\text{count_true}(x)$ returns how many of the lanes of $x$ are true.
- $\text{packed_load_U8(ptr, mask)}$ performs byte loads from increasing addresses for all lanes where mask is true; where mask is false, the
Listing 1 SIMD decoder with byte-wise normalization

```c
1: // Decoder state
2: Vec4_U32 x;
3: uint8* read_ptr;
4:
5: Vec4_U32 Decode()
6: {
7:   Vec4_U32 s;
8:
9:   // Decoding function (uABS, rANS etc.).
10:  s, x = D(x);
11:  
12:   // Renormalization
13:   // L = normalization interval lower bound.
14:   // NOTE: not quite equivalent to scalar version!
15:   // More details in the text.
16:   for (;;) {
17:     Vec4_U32 new_bytes;
18:     Vec4_bool too_small = lessThan(x, L);
19:     if (!any(too_small))
20:       break;
21:     
22:     new_bytes = packed_load_U8(read_ptr, too_small);
23:     x = select(x, (x << 8) | new_bytes, too_small);
24:     read_ptr += count_true(too_small);
25:   }
26:  
27:  return s;
28: }
```

return value is zero and the load address is not incremented. For example, suppose that mask = \{true,false,true,true\}; then the packed load would return \{ptr[0],0,ptr[1],ptr[2]\}.

The details of how to map these pseudo-instructions (packed_load in particular, “borrowed” from Intel’s ISPC compiler [10]) to an efficient sequence of real instructions are architecture-dependent. The example implementation benchmarked in section 7 uses SSE 4.1 instructions running on x86; the technique used in this implementation (building a bit mask denoting which lanes are active and then using a mask-dependent shuffle on the results of an unaligned memory load) is fairly universal.
As noted in the listing, this SIMD decoder is not fully equivalent to having \( N \) interleaved scalar decoders reading from the same bitstream: suppose that at least one of the SIMD lanes needs two or more renormalization steps—that is, it reads more than one byte from the encoded bitstream.

The regular decoding algorithm will read all bytes for a single stream before it moves on to decoding the next one. That is, suppose that \( N = 2 \), with lane 0 reading two bytes and lane 1 reading only one byte. The regular encoder from algorithm 1 will first write both bytes for stream 0, followed by the byte for stream 1—depth-first order, so to speak.

By contrast, the SIMD decoder in listing 1 expects breadth-first order: the first byte from stream 0, followed by the first byte for stream 1, followed by the second byte from stream 0.

It is possible to account for this on the encoder side, by either using a corresponding SIMD encoder that emits bytes in the same way, or by performing the breadth-first traversal “by hand” in a scalar encoder. Both strategies work, but have the unfortunate consequence that the target SIMD width \( N \) is now effectively baked into the bit stream (since it determines how exactly bytes get interleaved).

An alternative solution is to simply require that no lane ever execute more than one iteration of the normalization loop per symbol—thus turning the loop into a simple \texttt{if} statement. This places some requirements on the model probabilities; for example, with rANS, we can guarantee that no symbol will ever need to go through more than one normalization iteration when \( b \geq m \), where \( b \) is the radix of the encoder and \( m \) is the least common denominator of all symbol probabilities \( p_s \). With \( b = 256 \) as in the example listing, this is impractical for typical alphabet sizes; forcing \( m = 256 \) would mean that a 256-symbol alphabet could only use a uniform distribution! However, for an encoder working in 32-bit integers, we can choose \( b = 2^{16} \) while retaining a decent probability resolution of 12–14 bits.

The big advantage of choosing our coding parameters such that one iteration of the normalization loop is always sufficient is that the resulting bitstreams are exactly the same between the regular serial version and the SIMD variants; it is not necessary to encode the bitstream in any special way, and the result is not tied to any particular SIMD width \( N \). Thus, this is the option used in the example code discussed in section 7.

This section covers only the decoder; because ANS decoder and encoder are symmetrical, we can use the same technique on the encoder as well, this time using a \texttt{packed_store} instead of a \texttt{packed_load} operation.
6 GPU implementation

Although the typical programming model for GPUs is quite different from SIMD instructions on general-purpose CPUs, the underlying hardware is not: GPUs are, in essence, wide SIMD processors with built-in support for predication and relatively high-performance gather/scatter operations.

As a result, the SIMD approach described above is suitable for use on GPUs too, and the translation is, for the most part, quite straightforward. However, just as with the regular SIMD implementation, we need to come up with an efficient strategy to perform “packed” loads and stores.

The underlying idea is to determine in advance which invocations (in GLSL parlance) are going to perform a renormalization step; if all invocations know which invocations are going to perform a read, the packed load (or packed store) offset computation reduces to a prefix sum per invocation, which can be done very efficiently. Listing 2 illustrates the idea; this time, the decoder uses the loop-free approach with $b = 2^{16}$ discussed in the previous section (a looping version would loop over the entire renormalization code and break once `renorm_mask` becomes zero).

The listing assumes a work group size of 32 invocations (or smaller), so that a 32-bit integer is sufficient to hold `renorm_mask`. It uses the CUDA `ballot` instruction to compute `renorm_mask`, which is used both for the prefix sum offset computation and to advance the read pointer afterwards. `ballot` evaluates the given condition on all threads in a warp and returns a bit mask that has a 1 bit in the $i^{th}$ position if the condition was true on thread $i$. When a `ballot` instruction is not available (or in case the work groups are larger than the warp size / hardware SIMD width), its functionality can be synthesized—at some cost in efficiency—using atomic operations in group shared memory, as illustrated by listing 3; similarly, larger work groups might require using 64-bit integers (or arrays of integers) to store `renorm_mask`, but the general approach remains the same.

No matter which “ballot” approach is used, this results in a fully vectorized entropy coder, with predictable and well-coalescable memory access patterns, using a small number of GPU registers and shared memory space—and therefore well-suited for integration into other decompression kernels, if so desired.

As with the SIMD version, an encoder can be designed using the same technique, and the bitstreams are fully compatible between interleaved scalar, CPU SIMD, and GPU implementations, as long as the version with at most one renormalization step per symbol is used.
Listing 2 GPU decoder with 16-bit normalization

```c
1: // Decoder state
2: uint x;
3: uint16 in_buf[];
4: uint read_pos;
5: uint invoc_id; // ID for this invocation
6:
7: uint Decode()
8: {
9:   // Decoding function (uABS, rANS etc.).
10:  uint s;
11:  s, x = D(x);
12:
13:   // Renormalization
14:  uint invoc_bit = 1 <<< invoc_id;
15:  uint renorm_mask = ballot(x < L);
16:  uint offs = bitCount(renorm_mask & (invoc_bit-1));
17:  if (x < L)
18:    x = (x << 16) | in_buf[read_pos + offs];
19:  read_pos += bitCount(renorm_mask);
20:  return s;
21: }
```

Listing 3 Forming renorm_mask without ballot

```c
1: shared uint renorm_mask;
2:
3: // Form renorm_mask
4: if (x < L)
5:   atomicOr(renorm_mask, invoc_bit);
6: else
7:   atomicAnd(renorm_mask, ~invoc_bit);
8:
9: // Make sure all invocations finish modifying renorm_mask.
10: // groupMemoryBarrier();
11: barrier();
```
7 Evaluation

An implementation of rANS (one of the coders belonging to the ANS family) that shows 2-way interleaving and SIMD (SSE 4.1) decoding of an 8-way interleaved rANS stream is available at https://github.com/rygorous/ryg_rans. This version implements a simple order-0 model with static probability distribution (determined once per file).

Table 1 shows the resulting decompression rates on an Intel Core i7-2600K CPU (3.4GHz) on various test files from the Calgary Corpus [2] (book1, book2, pic), the Canterbury Corpus [1] (E.coli, world192.txt), and finally the source code for the Linux kernel version 3.14-rc1.

As is evident from the table, 2-way interleaving consistently achieves speed-ups of 1.6× or more over the non-interleaved decoder in this test, despite there being no significant difference in the number of operations executed per symbol. The reason is that the interleaved decoder benefits greatly from superscalar and out-of-order execution, while the non-interleaved version has a long chain of dependent operations and thus can’t utilize most of the CPU’s available execution resources.

The 8-way interleaved SIMD version is faster still (despite only using 4-wide SSE4.1 instructions, the code uses 8-way interleaving to, again, benefit from superscalar execution), although its performance is somewhat limited by the lack of a fast SIMD “gather” instruction that has to be simulated using scalar loads. Additionally, the SIMD version is entirely free of branches in the decoder, resulting in performance that is almost completely independent of the data being processed; compare the steady performance of the SIMD version against the much more variable throughput for the scalar versions.

8 Conclusion

The ANS family of coders has the unique advantage over regular arithmetic coders that all buffering of information is identical between encoder and decoder; the timing of input/output operations only depends on the coder’s state variable x, and both encoder and decoder go through the same sequence of states and perform IO at the same time.

Consequently, ANS coders can easily support efficient bypass coding as well as interleaving of data from multiple encoders without any additional metadata. Inspired by ANS, we show how the same property can be achieved with any entropy coder, by (conceptually) running an instrumented version
Table 1: Decompression performance of differently interleaved rANS decoders on various test files (all speed-ups relative to non-interleaved serial decoder).

| File             | serial MiB/s | 2-way MiB/s | speed-up | 8-way, SIMD MiB/s | speed-up |
|------------------|--------------|-------------|----------|-------------------|----------|
| book1            | 219.2        | 364.8       | 1.66     | 565.6             | 2.58     |
| book2            | 202.4        | 355.4       | 1.76     | 565.6             | 2.79     |
| pic              | 244.9        | 445.6       | 1.82     | 565.4             | 2.31     |
| E.coli           | 265.9        | 500.6       | 1.88     | 570.8             | 2.15     |
| world192.txt     | 209.0        | 337.7       | 1.62     | 564.3             | 2.70     |
| linux-3.14-rc1.tar| 217.6        | 359.0       | 1.65     | 573.2             | 2.63     |

Interleaving multiple independent ANS coders enable both much faster scalar entropy coders (with speed-ups of over 1.6× compared to the baseline), and SIMD implementations (with speed-up factors above 2×). The same technique is easily adapted to GPUs.

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References

[1] Ross Arnold and Tim Bell. A corpus for the evaluation of lossless compression algorithms. In *Data Compression Conference, 1997. DCC’97. Proceedings*, pages 201–210. IEEE, 1997.

[2] Timothy Bell, Ian H Witten, and John G Cleary. Modeling for text compression. *ACM Computing Surveys (CSUR)*, 21(4):557–591, 1989.

[3] Jarek Duda. Asymmetric numeral systems: entropy coding combining speed of Huffman coding with compression rate of arithmetic coding. *CoRR*, abs/1311.2540v2, 2014. URL http://arxiv.org/abs/1311.2540v2.
[4] Ralf Karrenberg and Sebastian Hack. Whole-function vectorization. In *Code Generation and Optimization (CGO)*, 2011 9th Annual IEEE/ACM International Symposium on, pages 141–150. IEEE, 2011.

[5] John Kessenich and LunarG, editors. *The OpenGL Shading Language, version 4.30*. The Khronos Group, Inc., 2013. URL http://www.opengl.org/registry/doc/GLSLangSpec.4.30.8.pdf.

[6] Detlev Marpe, Heiko Schwarz, and Thomas Wiegand. Context-based adaptive binary arithmetic coding in the H.264/AVC video compression standard. *Circuits and Systems for Video Technology, IEEE Transactions on*, 13(7):620–636, 2003.

[7] G Nigel N Martin. Range encoding: an algorithm for removing redundancy from a digitised message. In *Proc. Institution of Electronic and Radio Engineers International Conference on Video and Data Recording*, 1979.

[8] Alistair Moffat, Radford M Neal, and Ian H Witten. Arithmetic coding revisited. *ACM Transactions on Information Systems (TOIS)*, 16(3):256–294, 1998.

[9] Nvidia. Compute Unified Device Architecture programming guide. 2007.

[10] Matt Pharr and William R Mark. ispc: A SPMD compiler for high-performance CPU programming. In *Innovative Parallel Computing (InPar), 2012*, pages 1–13. IEEE, 2012.