IntersectX: An Accelerator for Graph Mining

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Abstract—Graph mining applications try to find all embeddings that match specific patterns. Compared to the traditional graph computation, graph mining applications are computation-intensive. The state-of-the-art method, pattern enumeration, specifically constructs the embeddings that satisfy the pattern, leading to significant speedups over the exhaustive check method. However, the key operation intersection poses challenges to conventional architectures and takes substantial execution time.

In this paper, we propose IntersectX, a vertical approach to accelerate graph mining with stream instruction set extension and architectural supports based on conventional processor. The stream based ISA can considered as a natural extension to the traditional instructions for ordinary scalar values. We develop the IntersectX architecture composed of specialized mechanisms that efficiently implement the stream ISA extensions, including: (1) Stream Mapping Table (SMT) that records the mapping between stream ID and stream register; (2) the Stream Cache (S-Cache) that enables efficient stream data movements; (3) tracking the dependency between streams with a property of intersection; (4) Stream Value Processing Unit (SVPU) that implements sparse value computations; and (5) the nested intersection translator that generates micro-op sequences for implementing nested intersections. We implement IntersectX ISA and architecture on zsim\textsuperscript{42}. We use 7 popular graph mining applications (triangle/three-chain/tailed-triangle counting, 3-motif mining, 4/5-clique counting, and FSM) on 10 real graphs. Our experiments show that IntersectX significantly outperforms our CPU baseline and GRAMER, a state-of-the-art graph mining accelerator. IntersectX’s speedups over the CPU baseline and GRAMER\textsuperscript{43} are on average 10.7\times and 40.1\times (up to 83.9\times and 181.8\times), respectively.

I. INTRODUCTION

Graph processing, which attempts to extract the underlying unstructured information of the massive graph data, has attracted significant attention in the recent decade\textsuperscript{12}, \textsuperscript{39}, \textsuperscript{43}, \textsuperscript{48}. The graph processing workloads can be categorized into two classes\textsuperscript{47}—graph computation and graph mining. Different from the traditional iterative graph computation (e.g., PageRank, BFS, SSSP, etc.) with simple computations, graph mining applications are computation-intensive\textsuperscript{6}, \textsuperscript{19}, \textsuperscript{20}, \textsuperscript{34}, \textsuperscript{47}, \textsuperscript{49}. The goal of graph mining is to find all embeddings that match specific patterns. The tasks are more challenging since the number of embeddings could be large. For example, in WikiVote, a small graph with merely 7k vertices, the number of vertex-induced 5-chain embeddings can reach 71 billion.

Different from graph computation systems’ think like a vertex (TLV) model\textsuperscript{9}, \textsuperscript{16}, \textsuperscript{31}, \textsuperscript{32}, \textsuperscript{35}, \textsuperscript{45}, \textsuperscript{56}, graph mining systems take an embedding-centric computation model, i.e., think like an embedding (TLE)\textsuperscript{47}. Current systems mainly adopt two approaches, and they differ in how candidate embeddings are generated. Arabesque\textsuperscript{47} pioneered the first approach based on exhaustive check. The system by default enumerates all possible embedding candidates up to the pattern size—oblivious to the specific patterns. The second approach is based pattern enumeration, which can effectively reduce the computation cost. It specifically constructs the embeddings that satisfy the pattern, avoiding checking infeasible embeddings. It is adopted by recent systems, i.e., AutoMine\textsuperscript{34}, GraphZero\textsuperscript{33}, GraphPi\textsuperscript{44} and Peregrine\textsuperscript{20}, which achieved significant speedups over Arabesque. RStream\textsuperscript{49} is a single-machine system that allows users to express patterns using relational algebra, which is implemented by a runtime engine efficiently with tuple streaming. While better than exhaustive check, it is not the same as pattern enumeration because the join operation does not precisely construct patterns and the checking is still needed.

Due to its importance, graph computation has been intensively investigated for acceleration with specialized architecture. In graph computation, the actual computation involved is typically lightweight, leading to the low ratio between computation and data movement time. As a result, the accelerators mainly focus on improving memory access efficiency, hiding communication latency, and/or reducing load imbalance. Recently, several domain-specific architectures are developed for graph computation, including Processing-In-Memory (PIM) based architectures\textsuperscript{8}, \textsuperscript{46}, \textsuperscript{55}, \textsuperscript{57}, accelerator for asynchronous\textsuperscript{56}, \textsuperscript{51}, \textsuperscript{52} and iterative\textsuperscript{38} graph processing.

However, to the best of our knowledge, there is only one existing graph mining accelerator proposed recently. GRAMER\textsuperscript{53} is the first graph mining architecture designed for the exhaustive-check method. Due to the nature of the method, the execution exhibits substantial random accesses from not only vertex dimension but also edge dimension, significantly affecting the performance. To tackle this problem, the paper proposed to use a heuristic algorithm to classify graph data into high and low priority by approximately simulating the vertex and edge accesses during exhaustive-check in a pre-processing step. Then, the high-priority data are permanently stored in the fast memory while the low-priority data
are organized in the cache with a specialized data replacement policy. GRAMER achieves impressive speedups compared to two graph mining frameworks on CPU—1.11× ~ 129.95× over RStream [49] and Fractal [11]. However, the state-of-the-art graph mining system AutoMine [34], which is based on pattern-enumeration method, has likely achieved higher speedups than GRAMER even on an unmodified CPU-based commodity machine. Even for small patterns like triangle counting, Automine can be 68.6× faster than RStream; for more complex patterns, it can achieve 777× speedup. It reveals the importance of the superior algorithm, and it is critical to develop architectural supports based on the state-of-the-art method.

How to accelerate pattern enumeration based graph mining algorithm is still an open problem. First, with pattern enumeration, the edge level random accesses are mostly eliminated because edge lists are mostly sequentially accessed. The key problem of random edge accessing that GRAMER tried to optimize is trivial with the pattern-enumeration method. Second, pattern enumeration poses a new challenge due to the frequent intersection operations between two edge lists for constructing patterns. Section II-B shows an example of the code pattern and analyzes the challenges for conventional architectures due to the branches and data dependencies. More importantly, Figure 3 shows that the execution time for the intersection operations is substantial in mining several representative graph patterns. Thus, to accelerate pattern enumeration method, efficient execution of intersection operation is the key.

Can existing architectures focusing on intersection help? There are three recent relevant architectures targeting irregular and sparse computations. Extensor [17] uses intersection as the building block to construct sparse tensor algebra kernels, and developed a general architecture to efficiently execute this operation. SparTen [15] is a more specific sparsity-aware DNN accelerator that performs dot-products of two vectors using intersection. Sparse Processing Unit (SPU) [7] proposes specialized supports for stream-join (similar to intersection) based on a systolic decomposable granularity reconfigurable architecture (DGRA). Unfortunately, three architectures can efficiently support graph mining for two reasons. First, it is almost impossible to port graph mining algorithms to Extensor or Spartan which are specialized for tensor kernels and BLAS routines. Second, the key for achieving high performance of graph mining applications is to explore computation reuse and symmetric breaking [33], [34], [44], creating complex code patterns that are infeasible to execute efficiently without significant efforts on SPU. Thus, existing architectures cannot be leveraged to accelerate pattern enumeration.

With the understanding of the challenge and requirement of pattern enumeration based graph mining, we propose IntersectX, a vertical approach to accelerate graph mining with stream instruction set extension and architectural supports based on conventional processor. We define a sparse vector as a stream, which can be a key or (key, value) stream. Our novel IntersectX ISA extension intrinsically operates on streams, supporting data movement and computation. It can be considered as a natural extension to the traditional instructions for ordinary scalar values. The IntersectX architecture is composed of specialized mechanisms that efficiently implement the stream ISA extensions, including: (1) Stream Mapping Table (SMT) that records the mapping between stream ID and stream register; (2) the Stream Cache (S-Cache) that enables efficient stream data movements; (3) tracking the dependency between streams with a property of intersection; (4) Stream Value Processing Unit (SVPU) that implements sparse value computations; and (5) the nested intersection translator that generates micro-op sequences for implementing nested intersections.

We implement IntersectX ISA and architecture on zsm [42]. We use several popular graph mining applications (triangle/hyper-edge/hyper-edge counting, 3-motif mining, 4/5-clique counting, and FSM) on 10 real graphs. Our extensive experiments show that IntersectX can be up to 83.9× and 181.8× faster than our CPU baseline and GRAMER (on average 10.7× and 40.1×), respectively.

II. BACKGROUND

A. Graph and Graph Mining Problems

A graph \( G \) is represented by its vertex set \( V \) and edge set \( E \). Vertices and edges may have labels, which are required by some graph mining applications. A graph \( G' = (V', E') \) is defined as an edge-induced subgraph of \( G = (V, E) \) if and only if \( V' \subseteq V, E' \subseteq E \). Furthermore, if all edges in \( E \) whose endpoints are both in \( V' \) are also included in \( E' \), \( G' \) is considered as a vertex-induced subgraph. Typically, graph mining applications take one or multiple graphs as input, enumerate all subgraphs matching a user-provided pattern, and extract useful information from them. The subgraphs matching (i.e., isomorphic with) the pattern are named embeddings.

Exhaustive-check based systems, such as Arabesque [47], enumerate all subgraphs with size up to the pattern size and perform isomorphism checks to discover those matching Fig. 1: Two Graph Mining Methods

Fig. 1: Two Graph Mining Methods

Exhaustive Check
Pattern Enumeration

v :1
v :2
result:
3
3 ...
6 ...
3 4 ...5

intersect()
v :3
v :4
v :5
1
2
2 ...
...
2 ...
v1
v3
v6
v2
v3
v4
v5

Edge List

Edge List

v :1
v :2
v :3
v :4
v :5

v1
v2
v3
v4
v5
v6

check()

v :3

v :4

v :5

v1

v2

v3

v4

v5

v6

v :1

v :2

v :3

v :4

v :5

v :6

check()

v1

v2

v3

v4

v5

v6

The pattern-enumeration-based systems can achieve considerably higher performance for three reasons. First, the pattern-enumeration method totally eliminates the computation-intensive isomorphism tests. Second, pattern-enumeration systems avoid checking the subgraphs not matching the pattern, which leads to a significant performance gain. Finally, at architecture
level, exhaustive checking systems suffer from edge-dimension random accesses due to the connectivity checking — examining whether a newly added vertex is connected to the other vertices. This problem does not exist in the pattern-enumeration method since the embedding construction algorithm already ensures connectivity of discovered subgraphs.

Pattern-enumeration systems heavily rely on vertex set intersection/subtraction operations. Takes 5-clique (a size-5 complete graph) as an example, its pattern-enumeration process to construct all 5-clique embeddings are shown in Figure 2, where \( N(v) \) is the neighbor vertex set of vertex \( v \). \( v_1, v_2, \ldots, v_5 \) are the five vertices of a 5-clique embedding. First, all vertices in the input graph are enumerated to match \( v_1 \). Afterwards, since vertex \( v_2 \) must be directly connected with \( v_1 \), it is enumerated from \( v_1 \)’s neighbor vertex set \( N(v_1) \). \( v_3 \) should be a common neighbor of both \( v_1 \) and \( v_2 \), thus it is enumerated from \( N(v_1) \cap N(v_2) \). Similarly, vertex \( v_4 \) and \( v_5 \) are enumerated from \( N(v_1) \cap N(v_2) \cap N(v_3) \) and \( N(v_1) \cap N(v_2) \cap N(v_3) \cap N(v_4) \), respectively.

B. Architecture Challenges

For pattern enumeration method, the key challenge is the intersection operations. Figure 3 shows the example code that performs the intersection operation. We abstract the edge lists as stream1 and stream2, which contains the indices of the neighbors. If the end of streams have not been reached, the processor reads from stream1 and stream2, and compare the values. If they match, the processor advances the output pointer, writes back to the output array, advances pointers of stream1 and stream2, and checks for boundary for both pointers. If the values mismatch, the processor advances the pointer of one of the streams, checks the boundary, fetches stream data, and compares again. In general, this code pattern contains branches and data dependencies in a tight loop, making it difficult to predict the branches and exploit instruction level parallelism. Note that the three branches at line 3,6,8 are performed based on the data-dependent comparison results. Figure 3 shows the number of cycles in a real machine for executing intersection operations for mining four patterns—Triangle(T), Three chain(TC), Three motif(TM), and Tailed triangle(TT)—on five data sets: patent(P), social-bitcoinalpha(B), email-eu-core(E), socfb-Haverford76(F), and wiki-vote(W). We see that intersection operations incur substantial instruction overhead for graph mining algorithms.

C. Can Existing Architectures Help?

Notably, the support for intersection has been proposed in the recent accelerator architectures for DNNs and sparse matrices because it is a key primitive to identify the effective computations, e.g., the multiplication of two non-zeros. Specifically, Extensor [17] uses intersection as the building block to construct sparse tensor algebra kernels, and developed a general architecture to efficiently speed up this operation. Based on Extensor, it is also possible to build specific DNN accelerators, where the key computations of convolutional and fully-connected layers are based on matrices. SparTen [15] is a more specific sparsity-aware DNN accelerator that performs dot-products of two vectors using intersection. The two architectures differ in (1) how the intersection operation is implemented: content addressable memory (CAM) based scan and search in Extensor versus prefix-sum in SparTen; and (2) the generality: an architecture for the general sparse matrix computation or specifically targeting DNN acceleration. On the other side, Sparse Processing Unit (SPU) [7] proposes specialized supports for stream-join (similar to intersection) based on a systolic decomposable granularity reconfigurable architecture (DGRA). It uses pipeline to hide the latency of stream-join with a novel design of dataflow control model [7].

However, none of the three architectures can efficiently support graph mining. First, unlike the traditional graph computation problems such as PageRank, SSSP, BFS, etc., graph mining algorithms cannot be expressed as matrix operations. Thus, it is almost impossible to port graph mining algorithms to Extensor or Spartan which are specialized for tensor kernels and BLAS routines. Second, and more importantly, the key for achieving high performance of graph mining applications is to explore computation reuse and symmetric breaking [33], [34], [44], creating complex code patterns that are infeasible to execute efficiently without significant efforts on the more “general” specialized architectures such as Extensor. Specifically, SPU requires manually rewriting C codes and describing data flow graph (DFG) with the language extensions for DGRA. The computations are mapped to the systolic DGRA by analyzing the DFGs. The complexity of graph mining algorithms leads to large DFGs, making it extremely difficult to port to SPU, except the simple patterns like triangle counting. Moreover, managing intermediate results for computation reuse requires sophisticated synchronization between the control core and SPU.

The most closely related work is GRAMER [53], which is the first graph mining architecture. It is designed for the exhaustive-check method. Specifically, a heuristic algorithm is used to to classify graph data into high and low priority by approximately simulating the vertex and edge accesses during exhaustive-check in a pre-processing step. Then the
high-priority data are permanently stored in the fast memory while the low-priority data are organized in the cache with a specialized data replacement policy. While GRAMER achieves impressive speedups compared to two recent graph mining frameworks on CPU—1.11× ~ 129.95× over RStream [49] and Fractal [11]. However, as discussed in Section II-A, the state-of-the-art graph mining system is Automine [34], which is based on the pattern-enumeration method. Based on the results of GRAMER, its improved performance is likely lower than Automine on the unmodified architecture. Even for small patterns like triangle counting, Automine can be 68.6× faster than RStream; for more complex patterns, it can achieve 777× speedup. This comparison reveals the importance of the superior algorithm, and it is critical to develop architectural supports based on the state-of-the-art method. As illustrated in Figure 3, the bottleneck for pattern-enumeration is no longer memory access but rather the intersection operations. Intuitively, with pattern-enumeration, the edge level random accesses are mostly eliminated because pattern-enumeration is doing sequential reads through edge lists. The only random access in pattern-enumeration is accessing the vertex information. Compared with sequential reading through an edge list, random access to a vertex is trivial. Thus the key problem of random edge accessing that GRAMER tried to solve is trivial with our pattern-enumeration method. In this sense, the problem we try to solve in this paper—the architectural supports for pattern-enumeration—is still open.

D. Design Principle

Based on the discussion of pattern-enumeration method and current relevant architectures, our design principle is to develop architectural supports based on the conventional processor, instead of designing an accelerator for graph mining from the ground up. It is justified by the complex control flows and code patterns of the state-of-the-art graph mining algorithms with important optimizations. In the next two sections, we will describe our novel vertical approach, IntersectX, from the instruction set extension for streams (Section III) to the architecture components that implement the new instructions (Section IV).

III. INSTRUCTION SET EXTENSION FOR STREAMS

For graph mining, the key operation is the intersection between two sparse vectors, e.g., edge lists. In general, we define a sparse vector as a stream, which can be: (1) a key stream—a list of key, such as the edge list in graph representation; or (2) a (key,value) stream—a list of (key,value), such as the pair of indices of non-zero elements and their values in a sparse matrix representation. We propose a novel instruction set extension that intrinsically operates on streams, supporting data movement and computation. The proposed IntersectX ISA for streams can be considered as a natural extension to the traditional instructions for ordinary scalar values. In the following, we describe the new registers, the operation of each instruction, and provide three examples of using the new instructions to implement different algorithms.

A. Register Extension

IntersectX ISA represents stream as the basic data type. The processor uses $N$ stream registers to maintain stream information, where $N$ is the maximum number of active streams supported by the processor. A stream is active between its initialization and free—each can be performed by an instruction. A stream register stores the stream ID, the stream length, the start key address, the start value address, and a valid bit. Note that the stream registers cannot be accessed by the instructions and the information is setup up when the corresponding stream is initialized. The program can refer to a stream by the stream ID, the mapping between a stream ID and its stream register is managed internally in the processor with the Stream Mapping Table (SMT) (see details in Section V-B). The key and value address of a stream register are only used by the processor to refer to the keys and values when the corresponding stream ID is referenced.

We also add three registers to keep the information about compressed sparse row (CSR) graph format. They hold pointers to CSR index, CSR edge list, and CSR offset and can be initialized by an instruction. The CSR offset stores the offset of the the smallest element larger than the vertex itself in the neighbor list. They are used to support the nested intersection, and the symmetric breaking. We assume CSR as the illustration and the design can be adapted to other sparse representations.

B. Instruction Set Extension

Table I lists the instruction set extension for streams. All the instructions can be classified into three categories: (1) stream initialization and destroy; (2) stream computation; and (3) stream element access. The input operands for all instructions are general purpose registers. Thus, the input values, such as stream ID, should be first moved to the registers before executing the stream instructions. There is no reason immediate values cannot be used directly as the inputs—we just assume the register operands for simplicity, the same architecture can support both scenarios.

S_READ and S_VREAD are the instructions to initialize a key stream and (key,value) stream, respectively. The operands are general purpose registers containing start key address (also start value address for S_VREAD), stream length, and stream ID. After they are executed, if the stream ID is not active, an unused stream register (valid bit is 0) will be allocated to the stream and the new mapping entry is created and inserted into SMT. If the stream ID is already active, the previous mapping is overwritten with the current stream information. After creating the mapping to a stream register, both instruction will also trigger the fetching of key stream to the stream cache (see details in Section IV-C). Thus, if the current stream overwrites the previous one, the content in the stream cache will also be updated. Note that S_VREAD does not load the values, which will be triggered when the computation instruction for (key,value) stream (V_VINTER) is executed. The values are accessed and fetched through the ordinary memory hierarchy rather than the stream cache. S_FREE is used to free a stream.
When it is executed, the processor finds the SMT entry for the stream ID indicated by the operand and set the valid bit to 0. If such entry is not found, an exception is raised.

Our ISA extension contains six instructions for stream computation. _S INTER_, _S INTER.C_, _S SUB_, _S SUB.C_ perform the simple computation on key stream—intersection and subtraction. The suffix ".C" indicates the variants of the corresponding instructions that do not output the result stream but just the count of non-zeros in the result stream. If the output is a stream, the stream ID is given in one of the input registers and the stream is initialized and an entry is added into SMT. Next, we explain the two more complex instructions.

The first one is _S VINTER_, which performs the user-defined intersected value computations. Specifically, the instruction first computes the intersection of the keys of the two input (key,value) streams, and then performs the computation on the values corresponding keys. For example, if the two streams are \([1,4,5,3,21,7,13])\) and \([2,14,5,36,7,2])\), then the instruction first identified the intersection of the keys \([1,3,7])\) and \([2,5,7])\), which is 7. Then it performs the computation on the corresponding values: assuming the computation is multiply-accumulation (MAC) specified in IMM, the result is 13 \(\times\) 2 = 16 in R2.

The second complex instruction is _S NESTINTER_, which performs the nested intersection. It is an instruction specialized for graph mining. Let the input stream (an edge list) be \(S = [s_0, s_1, ..., s_k]\), where each \(s_i\) corresponds to a vertex. Let us denote the edge list of each \(s_i\) as \(S(s_i)\), and the result of the instruction as \(C\). This instruction performs the following computation: \(C = \sum_{i=0}^{k} count((S \cap S(s_i)))\), where \(\cap\) is the intersection between two key streams, and \(count\) returns the length of a stream. Thus, this instruction implements a kind of dependent stream intersection. Given a stream \(S\), the other streams to be intersected with it are determined by the keys (vertices) of \(S\). The instruction captures an important code pattern in graph mining. The generation of the dependent streams corresponding to each \(s_i\) is performed by the processor using the information in the three CSR registers, which are loaded once using _S_CSR_ before processing a graph.

Finally, _S FETCH_ instruction perform the stream element access—returning the element with a specific offset in a stream, which can be either the output stream of an intersection operation or a stream initialized and loaded from memory. Typically, the offset is incremented to traverse all elements in a stream. When it reaches the end of the stream, _S FETCH_ will return a special “End Of Stream (EOS)” value.

### C. Code Examples

In the following three examples, we skip the normal assembly instructions and just indicate the function of the skipped assembly code using comments.

```
1 for(Vertex vi : graph){
2   Set n1 = vi.neighbor();
3   for(Vertex v2: n1){
4      Set n2 = v2.neighbor();
5      counter += Intersect(n2,n1).get_num();
6   }
7 }
```

(a) Triangle counting in C

```
1 loop_start:
2 //new start addr, len, id of i to R5-810
3 _S READ R5, R6, R12
4 //new start addr, len, id of i to R5-810
5 _S MRU R5, R6, R12
6 _S NVlea R5, R6, R5, R5
7 //new id of i to R5-810
8 _S FILE R5
9 //new id of i to R5-810
10 _S FILE R5
11 //loop end
12 RQD EAX, EAX, loop_end:
13 JMP loop_start
14 loop_end:
```

(c) Triangle counting with our ISA

```
1 loop_start:
2 //new start addr, len, id of i to R5-810
3 _S READ R5, R6, R12
4 _S_NESTINTER R5, R6, R0
5 //new id of i to R5-810
6 _S_CSR R2, R5, R2
7 //loop end
8 RQD EAX, EAX, loop_end:
9 JMP loop_start
10 loop_end:
```

(d) Nested Triangle counting with our ISA

Figure 4 (a) shows a basic implementation of triangle counting using intersections. We first get the edge list of \(v_1\), then we get the edge list corresponding to every element in \(v_1\)’s edge list (\(v_2\)). The intersection is performed between \(v_1\) and each \(v_2\), the number of triangles is the sum of the output stream sizes of all these intersections. Figure 4 (c) shows the implementation using our stream ISA extension. The stream for \(v_2\) is initialized in line 6 and we omit the codes to generate its start key address (as a part of the functionality in line 5). Each loop iteration operates on two streams and they are active only when _S INTER_ is executed. Note that different loop iterations can use the same stream IDs, similar to the same variable names. The processor internally keeps track of the active streams in both front-end (after instruction decoding) and back-end (at instruction commit time), and will recognize the same stream IDs in different iterations as different streams. The details will be discussed in Section IV.B.
Figure 4 (b) is a refactoring of the basic codes using the NestedIntersect function, which can be implemented precisely using the S_NESTINTER instruction shown in Figure 4 (d). Here there is only one active stream whole ID is stored in R10. The multiple intersections performed by S_NESTINTER do not take stream registration resource. In addition, there is only one level of loop. Such specialization based on the understanding of the graph mining code pattern is critical to achieving high performance.

```java
while (true) {
    cmp = stream1[i1] - stream2[i2];
    if (cmp == 0) {
        i1++; i2++;
        output += ...
    ...
```

Figure 5 (a) and (b) show the vector multiplication implementation with our stream ISA extension. At line 3 and 5, we initialize two (key,value) streams using the address of two sparse vectors with S_VREAD. Line 7 performs the multiply-accumulation on the values of the intersected keys.

IV. INTERSECTX ARCHITECTURE

A. Overall Architecture

The IntersectX architecture is composed of specialized structures built on conventional processor architecture and memory hierarchy that implement the stream ISA extensions. Figure 6 shows a detailed overview with stream related components highlighted in gray color. All instruction in Table 1 except S_NESTINTER occupies one entry in the Reorder Buffer (ROB). To support the ISA extension, the architecture needs to solve a number of problems: (1) the mapping between stream ID and stream register, which is handled by the Stream Mapping Table (SMT); (2) the movement of stream data, which is supported efficiently by the stream cache (S-Cache); (3) the dependency between streams, which is tracked with a property of intersection and minor supports in S-Cache; (4) the implementation of S_VINTER, which is realized by the coordination among the Intersection Unit (IU), Stream Value Processing Unit (SVPU), and the load queue augmented with stream information; (5) the implementation of S_NESTINTER, which is realized by the nested intersection translator that generates the micro-op sequence, similar to the contemporary implementation of CISC instructions with RISC-style micro-ops. In the following sections, we discuss the details of the above problems and solutions.

B. Stream ID Mapping

In IntersectX, each stream ID (Sid) specified in an instruction is mapped to an internal stream registers (Sreg). This mapping is performed at the front-end after instruction decoding and the mapping relation is kept in SMT. Besides the stream ID and its mapped stream register, each SMT entry contains: (1) two valid bits: Vp, indicating the define point of the stream, and VA, indicating whether the stream is active; (2) the start (s) and produced (p) bit, which indicate whether the S-Cache contains the keys from the start of the stream and whether the data for the whole stream is produced (so that it can be used by the dependent streams); and (3) the pred0 and pred1: the IDs of the stream that the current stream depends on. In this section, we explain the two valid bits and the others will be discussed together with S-Cache and dependence handling.

Initially, both Vp and VA are 0 and SMT is empty. Both VD and VA are set after decoding a S_READ or a S_VREAD instruction and the SMT entry indicates that the Sid_i in the last operand of the instruction is mapped to Sreg_j. Both VD and VA are set to one, they indicate that the instruction defines Sid_i and it is active. Later, when S_FREE Sid_i is decoded, the SMT is examined and an entry for Sid_i should be found (otherwise an exception is raised), and its VD is reset, while VA is unchanged. This means that Sid_i is no longer defined—the instructions after S_FREE Sid_i should not be able to reference Sid_i—but the stream is still free since S_FREE Sid_i has not been retired. When S_FREE Sid_i is retired, VA is reset and the entry becomes free. When a new stream is mapped, the processor checks SMT and finds an entry with VA = 0, which implies VD = 0. Note that is not true vise versa—VD = 0 does not imply VA = 0.

Our design expects the codes to call S_FREE after a stream is no longer used, so that its SMT entry can be released. In Section V-B we will describe the APIs for programmers, who do not need to directly write assembly codes, thus this requirement can be easily achieved. When all stream registers are occupied (VA = 1), the instruction that initializes a new stream will be stalled. The larger (or even unlimited) number of stream IDs can be supported by virtualization—by saving some SMT entry to a special memory region to release SMT
space. Due to the space limit, we do not discuss this in detail. In fact, using 16 stream registers is enough for all our applications. The design can naturally support the stream operations in loop iterations. Typically, inside an iteration, some streams are initialized and computations on them are performed before S_FREEs at the end of the iteration (refer to Figure 4(c) for an example). The different iterations can use the same stream IDs, which will be mapped to different SMT entries with our SMT mechanisms.

C. Stream Cache

In IntersectX, the keys for each active stream are loaded into a special stream cache (S-Cache), which is on top of L2 cache together with L1. Note that the values in (key, value) stream are still fetched through the normal memory hierarchy. Thus, when the stream keys are accessed using the stream instructions, the data will not pollute L1. Such specialization enables efficient stream data movements while avoiding cache evictions by other data. Since the keys of a stream are accessed sequentially, the data can be effectively prefetched to S-Cache without a complex prefetcher, thanks to the known access pattern. The organization of S-Cache is simple: each stream register has a slot that holds a fixed number keys of the stream. We use the 64-key slot which leads to 256 byte slot size. With 16 stream registers, the total size of S-Cache is 4KB.

When an S_READ is executed, the first 64 keys are fetched to the S-Cache, and the start bit in SMT for the stream is set. Unless the length of the stream is not more than 64, at this point the S-Cache only contains the first portion of the stream. The start bit indicates that the instructions that depend on the stream can use the data in the S-Cache slot. Referring to Table 1, our ISA does not contain any instruction that explicitly stores to a stream: only S_INTER and S_SUB produce the results in the destination stream. When these instructions are executed, the result keys are written to the S-Cache slot in group of 64. If the result stream contains more than 64 keys, the slot will contain the most recently produced 64 keys while the previous slot is written back to L2 and the start bit is cleared. When the whole result stream is generated by the computation instruction, the produced bit is set, which is used to trigger the dependent instructions.

The typical code pattern is that two streams are initialized by S_READ before the intersection operation is performed. In this case, data fetching from L2 to S-Cache and transfer to IUs for computation can be pipelined. To support that, we use the idea of double buffer and divide each slot into two sub-slots. When a sub-slot is fetched from L2, the keys in the other sub-slot can be prefetched to IU simultaneously and the intersection computation can be overlapped. We assume that the bandwidth between the stream cache and IU is 4 keys (16 bytes) per cycle, which is similar to the read bandwidth of L1 cache of Intel Nehalem at 128 bits per cycle [18].

Typically, the intersection computation time of a sub-slot (e.g., 32 to 64 cycles) is longer than fetching data from L2 on cache hits (e.g., 20 cycles). With multiple IUs, the parallel execution time of multiple intersections can be better overlapped with the data fetching time of these streams. When multiple IUs (4 in our design) need data to perform computations, S-Cache has to schedule the data transfer to different IUs. We use a simple round-robin policy: at each cycle, S-Cache schedules the transfer of 4 keys to a different IU that is waiting for the data. Each IU is able to perform the intersection on the partial key streams received.

D. Stream Data Dependency

Two streams may have dependency due to: (1) stream ID, where an instruction uses the output stream of a previous computation (S_INTER or S_SUB); or (2) the overlapped memory regions of two streams. It is easy to handle the first scenario: after the stream IDs are available after decoding, the dependency can be handled in the similar manner to the data dependency on general registers. When a dependency is identified, the consumer instruction can only execute after the producer instruction. It is enforced by filling the pred0 and pred1 in SMT of the consumer instruction. When the producer instruction finishes, its SMT entry’s produced bit is set. Each cycle the processor checks the status of the producer instruction(s) and triggers the consumer instruction when all operands’ produced bit are set. If the key stream produced is less than 64 keys, the whole stream is in S-Cache with the start bit set, the consumer instruction reads directly from S-Cache; otherwise, the slot will be refilled from L2.

For the second scenario, we can check the potential dependency conservatively by leveraging the fact that the length of the output stream is less than the minimum length of the two input streams. Thus, we can conservatively deduct the maximum length of the output stream. The possibly overlapped stream memory regions can be detected using the start key address and stream length of different streams. The dependent stream instructions need to be executed sequentially, which is enforced using the same mechanism as the first scenario.

E. Sparse Computation on Values

The sparse computation on values is supported by the coordination between IU, value buffer (vBuf), load queue, and Stream Value Processing Unit (SVPU). When S_VINTER is executed, an IU starts with key intersection calculation and the output keys are given to the Value Address Generator (VA_gen) associated with the IU (refer to Figure 6). VA_gen generates the value addresses for each key in the intersection. These addresses are sent to load queue to request the values through the normal memory hierarchy, rather than S-Cache. Each value request is also allocated with an entry in the vBuf, which will collect the two values returned from the load queue (val0 and val1). Each entry has a ready bit (r) for each value, which is set when the load queue receives the value. We assume that the operation is commutative (e.g., multiply-accumulate) thus the computation using val0 and val1 can be performed by SVPU as soon as both ready bits are set. We do not need to enforce any order. The acc_reg is used to keep the accumulated partial results. While performing substantial amount of computations, this instruction only takes one entry in ROB, when the final
result is produced in the acc_reg of the corresponding IU, it will be copied to the destination register, and the instruction is ready to retire from the processor when it reaches the head of ROB.

F. Nested Intersection

The _S_NESTINTER is the most complex instruction and we use the _Nested Instruction Translator to generate the instruction sequence based on other instructions of IntersectX ISA to implement it. Based on the input key stream, the translator will first generate the stream information based on each key element. Based on the CSR registers, the memory addresses of the stream information is calculated, then the memory requests are sent through load queue. While waiting for the stream information, an entry is created in the translation buffer, its ready bit (rdy) is set when the data arrive at load queue. Similar to the pointer to vBuf entry, each load queue also keeps a pointer to the translation buffer entry. For each nested stream, three instructions are generated: _S_READ, _S_INTER.C, and _S_FREE. Moreover, an addition instruction is generated to accumulate the counts. Each instruction will take an entry in the translation buffer. The start address and stream length fields are only used in the entry for _S_READ. When the stream information is ready, the three instructions following it will also become ready and inserted into ROB. When the translation is stalled when the translation buffer is full, which can be due to either ROB full or waiting for the stream information. In either case, the space will eventually released because eventually the instructions in ROB will retire and the requested data will be refilled. These events do not wait for the translation procedure and there is no deadlock.

V. IMPLEMENTATION AND PROGRAMMING MODEL

A. Implementation Considerations

The _S_NESTINTER is translated into a variable length instruction sequence by the processor and will take multiple ROB entries. To ensure the precise exception, the processor takes a checkpoint of registers before the instruction. If an exception is raised during the execution of the instruction sequence, the processor rolls back to the checkpoint and raises the exception handler. It is similar to the mechanisms for transactional and atomic block execution [5], [27]. Besides the normal information such as general registers, the checkpoint includes the content of SMT, stream registers and CSR registers. Another assumption in IntersectX architecture is that, the stream cache does not participate in the coherence protocol. Thus, the potential modifications of other cores on key elements do not propagate in time to stream cache. However, for the applications that IntersectX will accelerate, this cache does not participate in the coherence protocol.

VI. EVALUATION

A. Simulator and Configuration

We simulate IntersectX on zsim [42], a fast and scalable simulator designed for x86-64 multicore. We integrate our all the proposed architectural components including Stream Cache and Intersection Unit into the simulator. Our configuration is listed in Table III.

B. Graph Mining Algorithms and Data Sets

| Number of cores | 8 |
| ROB size | 128 |
| loadQueue size | 32 |
| l1d cache size | 64KB |
| cache line size | 64B |
| 12(last level) cache size | 2MB |
| stream cache latency | 1 cycle |
| stream cache bandwidth | 16B |
| stream cache slot size | 256B |
| l1d latency | 4 cycles |
| l2(last level) cache latency | 10 cycles |
| memory controllers number | 3 |
| memory controller latency | 40 cycles |
| memory type | DDR3-1333-CL10 |

Table II: IntersectX APIs

| Function prototype |
|--------------------|
| VertexSet RegisterVertexSet (Vertex* addr, Length len) |
| void ReleaseVertexSet (VertexSet handler) |
| Length NestCounting (VertexSet handler) |
| Vertex EnumerateVertexSet (VertexSet handler, Length offset) |
| void SubtractVertexSet (VertexSet A, VertexSet B, VertexSet C) |
| Length SubtractVertexSetCount (VertexSet A, VertexSet B) |
| void IntersectVertexSet (VertexSet A, VertexSet B, VertexSet C) |
| Length IntersectVertexSetCount (VertexSet A, VertexSet B) |
| Vector RegisterVector (Index* addr, Value* addrV, Length len) |
| void ReleaseVector (Vector handler) |
| Value VectorCompute (Vector A, Vector B, Op type) |

Fig. 7: API Example: Three Chain

VI. EVALUATION

A. Simulator and Configuration

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B. Graph Mining Algorithms and Data Sets

| TABLE III: IntersectX Architecture Configuration |
|------------------------------------------------|
| name | #V | #E | avg D | max D |
|------|----|----|-------|-------|
| cityseer (C) | 13,12 | 17,12 | 3.3K | 4.5K | 1.39 | 99 |
| email-en-core (E) | 25,13 | 23 | 1.09K | 16.1K | 25.4 | 345 |
| soc-sign-bitcoinalpha (B) | 12,21 | 22 | 3.85K | 24K | 6.4 | 511 |
| p2p-Gnutella08 (G) | 29,40 | 6K | 21K | 3.3 | 97 |
| socfb-Haverford76 (F) | 24,41 | 1.4K | 60K | 41.3 | 375 |
| wiki-vote (W) | 25,26 | 7K | 104K | 14.6 | 1085 |
| wiki-vote (M) | 13 | 96K | 1.1M | 1.12 | 1399 |
| com-youtube-Y1 | 11,10 | 1.1M | 3.0M | 2.6 | 28784 |
| patent (P) | 27,50 | 3.8M | 16.5M | 8.8 | 993 |
| livejournal-L | 24,10 | 8.8M | 42.9M | 17.7 | 20335 |

TABLE V: Graph Datasets
We choose several popular graph mining applications listed in Table IV to evaluate IntersectX. They can be divided into four categories. (1) Pattern counting applications, which include triangle (T), three-chain (TC), and tailed-triangle counting (TT). These three workloads aim to count the number of triangle/three-chain/tailed-triangle embeddings, respectively. We use T, 4C, and 5C to denote the nested implementations while TS, 4CS, and 5CS refer to the corresponding stream implementations without nested support. (2) k-motif mining, which counts the embeddings of all connected patterns with a given size \( k \). We choose \( k \) to be 3 in our experiments. (3) k-clique mining, which discovers all size-\( k \) complete subgraphs of the input graph. (4) Frequent subgraph mining (FSM), which aims to discover all vertex-labeled frequent patterns. A pattern is considered as frequent if and only if its support is no less than a user-specified threshold. Pattern support could have different definitions. However, all of them should satisfy the Downward Closure Property, which requires that one pattern should never have a greater support than its subpatterns. This key property is used in FSM to prune the searching space efficiently—if one pattern is infrequent, it can be safely discarded since it cannot be extended to any frequent patterns. Similar to previous systems like Peregrine [20], we choose the minimum image-based support metric [4] and only discover frequent patterns with no more than three edges. Besides, it is worth noting that GRAMER mistakenly used the pattern count (i.e., the number of embeddings) as the pattern support for FSM, which violates the Downward Closure Property. We also implement this incorrect FSM algorithm for performance comparison purposes and refer to it as simple-FSM (sFSM) in our experiments. Table IV lists the real-world graphs we used from various domains, ranging from social network analysis to bioinformatics.

### C. Overall Performance

We compare IntersectX with GRAMER [53] and our CPU baseline on different datasets and algorithms.

1) **Comparison with GRAMER:** We also implemented GRAMER on zsim. To simplify the comparison, we only enable one PU/CPU core in both GRAMER and IntersectX. In order to make a fair comparison, we configure GRAMER’s on-chip RAM access latency to be the same as IntersectX’s first level cache latency.

We compare the performance of IntersectX, the CPU baseline, and GRAMER in Figure 8. The applications involved are Triangle Counting, 4/5-Clique, 3-motif, and sFSM with 2K/4K support thresholds. IntersectX significantly outperforms both the CPU baseline and GRAMER. It is worth noting that GRAMER is even slower than our CPU baseline. The performance gap is majorly attributed to the algorithmic difference. Our CPU baseline implements the pattern enumeration method, which is much faster than the exhaustive check method in GRAMER. The architectural supports in GRAMER cannot benefit pattern enumeration method.

Another key observation is that IntersectX achieves higher speedups over GRAMER for more complex patterns, such as 4/5-clique counting. On average, IntersectX outperforms GRAMER by 85.5×, 121.3× for 4-Clique and 5-Clique counting, respectively. By contrast, for triangle counting, the speedup is only 32×. The speedup difference is reasonable. As we have discussed in Section II, one major source of exhaustive check method’s inefficiency is their connectivity check operations. A larger pattern incurs more connectivity checks. For instance, to extend a size-\( k \) subgraph \((v_0, v_1, \ldots, v_{k-1})\), the exhaustive check method typically selects an existing vertex \( v_i (0 \leq i \leq k-1) \), and choose one of its neighbor \( v_k \in N(v_i) \) to be the new vertex. \( k-1 \) connectivity checks are needed to determine whether \( v_k \) is connected with the existing vertices except for \( v_i \). As a result, to enumerate a larger subgraph, exhaustive check systems/accelerators like GRAMER suffer more from the overhead caused by connectivity checks. This explains IntersectX’s higher speedup over GRAMER for the larger pattern since it is based on pattern enumeration and totally avoids connectivity checks.

2) **Comparison with CPU:** Further performance comparison among IntersectX (with/without nested intersection) and the CPU baseline are shown in Figure 9. TS, 4CS, and 5CS refer to the triangle counting, 4-clique, and 5-clique implementations without nested intersection. On average, enabling nested intersection speeds up these applications by 1.357×. It is because with nested intersection instructions, the normal instructions used to explicitly manage the corresponding loops, graph structure accesses, and embedding counting are eliminated. Besides, note that IntersectX achieves less speedup for FSM. It is because the support calculation in FSM is costly, and thus the intersection/subtraction operations that our architecture accelerates take a smaller portion of execution time.

Comparing across different datasets, IntersectX achieves higher speedups on graphs with higher average degree. This could be explained by Amdahl’s law. On graphs with higher degrees, the operand lengths of intersection/subtraction operations are generally longer. As a result, these operations are more computation-intensive and take up a larger portion of execution time. Recall that IntersectX only speedups intersection/subtraction operations, and thus achieves higher

| Name                | Triangle counting (T) | Three chain counting (TC) | Tailed triangle counting (TT) | 3-motif (TM) | 4-clique (4C) | 5-clique (5C) |
|---------------------|-----------------------|---------------------------|------------------------------|-------------|--------------|--------------|
| Table IV: Graph Mining Applications |

**TABLE IV:** Graph Mining Applications

- Triangle Counting (T)
- Three Chain Counting (TC)
- Tailed Triangle Counting (TT)
- 3-motif (TM)
- 4-clique (4C)
- 5-clique (5C)
- Frequent Subgraph Mining (FSM)

**Fig. 8:** Speedup of IntersectX and CPU (pattern enumeration) over GRAMER (exhaustive check) (log scale)
We observe that intersection operations still take up a large portion of execution time even though we have significantly speedup graph mining applications via optimizing intersections.

**D. Analyzing the Execution Time of Intersection Operations**

We analyze the execution time dedicated for intersection operations in IntersectX. The results are shown in Figure 10. We observe that intersection operations still take up a large portion of execution time even though we have significantly accelerate them. This indicates that there are still research opportunities to speedup graph mining applications via optimizing intersections.

**E. The Distribution of Stream Lengths**

We further analyze the length distribution of involved streams in different graph mining algorithms. Figure 11 shows the cumulative distribution function (CDF) of stream lengths in different graph mining algorithms on the email-eu-core graph. Even on the same graph dataset, different applications could lead to different stream length distributions. We notice that clique applications (i.e., 4-clique/5-clique counting) in general introduce shorter stream lengths. The reason is that in clique applications, the input operands of intersection operations are usually the intersection of several streams (e.g., t2 in Figure 2). And these operands tend to have short stream lengths.

We also fix the graph mining application to triangle counting and analyze the stream length distribution on various datasets. The results are reported in Figure 12. The observation is intuitive—the longest stream length on datasets with larger maximal degrees (e.g., LiveJournal, Youtube) are longer. Besides, there are more long streams on denser datasets like E (email-eu-core) and F (socfb-Haverford76).

**F. Varying the Number of Intersection Units (IUs)**

We characterize the performance of IntersectX by varying the number of IUs. Figure 13 shows the results with 1 to 16 intersection units. When the number of IUs is no more than 4, increasing it will generally improve IntersectX’s performance. However, with more than 4 intersection units, adding IUs introduces significantly less benefit or even slight performance degeneration due to the read port contention of S-Cache. This indicates that the different architecture components need to be matched based on performance characterization.

**G. Analysis on S-Cache Bandwidth**

We further characterize IntersectX’s performance with different S-Cache bandwidths. Figure 14 shows the performance of IntersectX with S-Cache bandwidth varying from 2 elements (64 bits) per cycle to 32 elements (1024 bits) per cycle. In general, increasing S-Cache bandwidth can improve IntersectX’s performance. However, there is a point of diminishing return. For example, for the TC (three-chain counting) application, increasing the bandwidth from 8 to 32 elements/cycle introduces almost no benefit. It is because there are not enough concurrent active stream intersection/subtraction operations to saturate the S-Cache bandwidth. The number of concurrent active stream operations is determined by the application and implementation. Triangle counting (T) and 4/5-Clique (4/5C) counting use the nested intersection instruction to trigger intersection operations in a bursty manner, and thus there are more simultaneously on-the-fly intersections. Hence, T/4C/5C benefits more from S-Cache bandwidth increase than other algorithm/implementation without the nested instruction (e.g., 4CS, 5CS).

**H. Sparse Value Computation**

To evaluate \( S_{\text{VINTER}} \), we implemented sparse matrix multiplication with the output stationary method via our (key,value) stream interfaces. We evaluated IntersectX with matrices listed in VI.
The speedup of IntersectX against the CPU baseline is shown in Figure 15. IntersectX achieves on average 5.7 times speedup. For matrices with higher density, IntersectX can achieve higher speedup. The reason is, since there are more non-zeros, denser matrices lead to more intersection computation, which can be accelerated by IntersectX architecture.

VII. CONCLUSION

This paper proposes IntersectX, a vertical approach to accelerate graph mining with stream instruction set extension and architectural supports based on conventional processor. We develop the IntersectX architecture composed of specialized mechanisms that efficiently implement the stream ISA.
extensions. We implement IntersectX ISA and architecture on zsm [42]. We use several 7 popular graph mining applications (triangle/three-chain/tailed-triangle counting, 3-motif mining, 4/5-clique counting, and FSM) on 10 real graphs. Our extensive experiments show that IntersectX outperforms our CPU baseline and GRAMER significantly. The average speedups could be up to 83.9 and 181.8 and on average 10.7 and 40.1, respectively.

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