Abstract—We report CMOS-compatible quantized current sources (electron pumps) fabricated with nanowires (NWs) on 300 mm SOI wafers. Unlike other Al, GaAs or Si based metallic or semiconductor pumps, the fabrication does not rely on electron-beam lithography. The structure consists of two gates in series on the nanowire and the only difference with the SOI nanowire process lies in long (40 nm) nitride spacers. As a result a single, silicided island gets isolated between the gates and transport is dominated by Coulomb blockade at cryogenic temperatures thanks to the small size and therefore capacitance of this island. Operation and performances comparable to devices featuring e-beam lithography is demonstrated in the non-adiabatic pumping regime, with a pumping frequency up to 300 MHz. We also identify and model signatures of charge traps affecting charge pumping in the adiabatic regime. The availability of quantized current references in a process close to the 28FD SOI technology could trigger new applications for these pumps and allow to cointegrate them with cryogenic CMOS circuits, for instance in the emerging field of interfaces with quantum bits.

I. INTRODUCTION

ELECTRON pumps are devices which, driven at a frequency \( f \), transfer a well defined number of elementary charges \( e \) per cycle: \( I = Nef \), where \( N \) is an integer. These ultimate charge-coupled devices will be the natural candidates for the mise en pratique of the upcoming re-defined ampere, since the new definition will be based on a flux of charges per unit time, the value of \( e \) being fixed. The first generation of devices were made with metallic tunnel junctions defined by e-beam lithography and reached the very high precision of 15 part per billion but at the low frequency of 5 MHz (hence delivering small currents, \( I \lesssim 8 \text{ pA} \)) \[1\], \[2\]. Although originally developed at the same time \[3\], \[4\], semiconductor devices recently triggered a new era in which new and faster pumping schemes have been explored \[5\]–[7]. All devices however relied so far on e-beam lithography, hence limiting the throughput and restricting the application to specific fields such as quantum metrology. Here we demonstrate all optical lithography made electron pumps which can be produced on a large scale with commercial CMOS technology. This could open new perspectives for applications, for instance in the emerging field of cryogenic electronics designed to interface quantum bits \[8\]–[12]. Indeed here operation near or below 1 K is not an issue.

II. DEVICE FABRICATION

The top layer of the [100] SOI wafers with buried oxide (BOX) 145 nm is first thinned down to \( \approx 8 \text{ nm} \). Patterning of [110]-oriented NWs is realized with deep-UV (193 nm) optical lithography in air, with a direct resolution of 80 nm. Then resist trimming is performed in order to further decrease their width, which ranges from 10 to 60 nm (60 nm for the results presented hereafter) \[13\]. High-k/metal gates are then deposited as a stack of 0.8 nm of \( \text{SiO}_2 \) oxide, 2 nm of CVD \( \text{HfO}_2 \), 5 nm of ALD TiN and 50 nm of poly-silicon. The gates wrap around the channel, and photo-resist trimming is again used to achieve gate lengths down to 15 nm. Thick (40 nm) self-aligned nitride spacers are then formed on sidewalls of the gates, highlighted in green in Fig. 1a,b. For comparison, the standard thickness for spacers in industrial devices is slightly below 10 nm in order to minimize serial access resistance while preventing short channel effects. Although the minimal spacing between gates is limited to 170 nm with our equipment

Design and operation of CMOS-compatible electron pumps fabricated with optical lithography

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and process, the unusual thickness of the spacers allows to create a silicided island of length $\lesssim$100 nm, as illustrated in Fig. [1]. Raised source/drain are realized by epitaxy ($T_{Si}$=18 nm) prior to implantation, activation spike annealing and silicidation (NiPtSi).

III. DEVICE OPERATION

Room temperature characteristics of a device of width 60 nm and gates length 85 nm are shown in Fig. [2] left. An excellent sub-threshold slope of 70 mV/decade is measured for 0 and 20 V of backgate voltage $V_{bg}$, as a result of the good electrostatic control of the NW by the wrapping gate [13]. At cryogenic temperatures the thick spacers create a low doped region in the NW which is long enough to behave as a tunnel barrier [14], as illustrated in Fig. [1]. If the substrate is not biased, a Coulomb island is created under each gate. As a result, a complex structure with 3 dots in series controlled by biased, a Coulomb island is created under each gate. As a barrier [14], as illustrated in Fig. 1b. If the substrate is not

Fig. 2. (a) Source-drain current as a function of each gate voltages, $I(V_{g})$ for 2 values of $V_{bg}$: in red when sweeping both gates together ($V_{g} = V_{g1} = V_{g2}$), in green and blue when sweeping respectively $V_{g1}$ and $V_{g2}$, with the other kept at +0.8 V. Increasing the backgate voltage increases the conductance around the value of the conductance quantum $\frac{e^2}{h} = 3.9 \times 10^{-5}$ S, indicated by the black triangle. (b) 2D map of the current as a function of both gate voltages, recorded with a drain bias $V_{d}=50 \mu V$ at base temperature $T=90$ mK and $V_{bg}=28.5$ V. The observed pattern of anti-diagonal high conductance lines is typical of a single Coulomb island equally controlled by two gates.

regime, the number of electrons on the island will change right after each crossing of a resonance line and a pumping contour. Which lead (or impurity) the corresponding single electron is exchanged with depends on the ratio of the corresponding tunnelings rates [26]. In the blue (red) shaded area of Fig. [4]a transport under gate 1 (gate 2) dominates, while in the white area the island is effectively disconnected. An impurity-caused resonant spike in conductance under gate 1 extends the source-dominated (blue) region to the right, opening the possibility for current quenching or even reversal [22]. An additional factor is impurity-island capacitive coupling which results in charge stability regions characteristic of a double-dot, see Fig. [4]b. If the pumping ellipses are sufficiently narrow to go between the electron and the hole triple points, we can expect both current polarities, a hallmark feature of adiabatic pumping with double dots, whether intentional [1], [24] or not [27].

In Fig. [5]a a 2D map of the pumped current measurements
is shown. Each point corresponds to a particular position of the center of an ellipse. The results support interpretation of the pumping mechanism predicted by Fig. 4(a). In particular, the anti-diagonal regions of $-ef$ current in the lower left corner are unaffected by the impurities (cf. the lower left ellipse in Fig. 4h), while the top-right regions show sign alternation consistent with impurity-island double dots formation.

For simulation of the experimental results, we extend the deterministic model of Ref. [22] to include additional capacitive couplings and non-resonant transport. The source, impurity 1, the island, impurity 2 and the drain are connected in series, see Fig. 5a. Electrostatic energies of the corresponding trapped charge configurations $(n_1, n_2)$ with $n_{1,2} = 0, 1$ and $n = 0, 1, 2, \ldots$ are computed as functions of $V_{g1}$ and $V_{g2}$ using capacitances estimated from d.c. measurements in Fig. 2(b) and from the measurements of Coulomb diamonds (not shown). The simulation keeps track of allowed transitions to lower energy configurations as the pumping contour is traversed. Exchange of an electron with the source (drain) is allowed only if $V_{g1} > V_{g1}$ ($V_{g2} > V_{g2}$), where cut-off values $V_{g1} = 0.132 \text{ V}$ and $V_{g2} = 0.100 \text{ V}$ act as effective thresholds. All transitions rates are simplified as either instantaneous or zero (below threshold), hence the computed charge transfer per period is an integer. Fig. 5(c) shows simulation results in general agreement with the measurements (d): pumping with contours going below thresholds is not perturbed while sign reversal for above-threshold (adiabatic) pumping occurs in a complex alternating pattern which is sensitive to microscopic details.

We find that adiabatic current quantisation mechanism is sensitive to above-threshold impurities near sign-reversal (occurs at $\Delta \phi \approx \pi$) due to impurity-island capacitative coupling. Optimal operation is expected for larger $|\Delta \phi - \pi|$ with the contour minor axis matching the distance between consecutive Coulomb valleys. Since the charging energy of the island is dominated by its capacitance to the gates, robust operation for optimised contours is feasible.

IV. CONCLUSION

We have developed a fabrication scheme for electron pumps based solely on optical (deep UV) lithography. The only modification to the standard process flow lies in long spacers which effectively reduce the size of the central island. This pump is operated in the same fashion as e-beam devices. The role of single dopant resonances with can give rise to sign reversal in pumping has been elucidated in the adiabatic regime by extending a recent model [22] to account for competition between direct and dopant-mediated transport paths. Optical lithography could allow for parallelization to increase output current [28], although more investigations are required to assess the variability at low temperature. This work opens the way for the design of functional cryogenic devices realized within a commercial technology such as 28FDSOI.

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