A 42 mV startup ring oscillator using gain-enhanced self-bias inverters for extremely low voltage energy harvesting

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This paper presents a ring oscillator (ROSC) capable of operating at an extremely low supply voltage. The proposed ROSC consists of gain-enhanced self-bias inverters. The voltage gain of the proposed inverter is improved by controlling the body bias voltages. Measurements of a prototype chip demonstrated that our proposed ROSC can operate at an extremely low supply voltage of 42 mV.

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1. Introduction

One of the challenging research areas in microelectronics is the development of Internet of Things (IoT) devices that collect various data from our surroundings and utilize them for the purpose of improving lifestyle, industry, agriculture and medical science.¹⁻⁶ A low-power and highly efficient power management system (PMS) using environmental energy will be a key component in the construction of such devices. Its invention also presents a technical challenge because of the large number of IoT devices to be installed worldwide.⁷⁻⁻²⁰

Thermoelectric generators (TEGs) have attracted attention as an alternative energy source because they can generate energy from a subtle temperature difference.²¹⁻⁻²⁴ However, the output voltage of a TEG is too low to operate application circuits and systems. To address this issue, DC-DC converters are used to generate a sufficiently higher voltage.²⁵⁻⁻³⁵

As a first step in the realization of such converters, an extremely low voltage oscillator is required to start the PMS.³²⁻⁻³⁹ A ring oscillator (ROSC) consisting of CMOS inverters is widely used because it can operate at lower supply voltages. However, the voltage gain of the inverter decreases as the supply voltage decreases, and thus it is difficult to operate at a sub-100 mV supply voltage, which is the typical output voltage range of a TEG with a small temperature difference.

In light of this background, we propose an ROSC capable of operating at an extremely low supply voltage. In contrast to our previous work,⁴⁰ here, we discuss its circuit operation and analyze its effectiveness in more detail. In addition, we demonstrate that our proposed ROSC can operate at an extremely low voltage of 42 mV. Our ROSC consists of gain-enhanced self-bias inverters (SBIs). The voltage gain of the proposed SBI is improved by controlling the body bias voltages.

This paper is organized as follows. In Sect. 2, we present our proposed self-bias inverter. In Sect. 3, we discuss the simulated results. In Sect. 4, we show the measured results of our prototype chip. In Sect. 5, we conclude the paper.

2. Proposed gain-enhanced inverter

Figure 1 shows a schematic of the ROSC. An odd number of inverters are connected in series and the output node is fed back to the first-stage input node. For oscillation to begin, the voltage gain of the inverter (|A_{INV}|) must be greater than unity.⁴¹

\[ |A_{INV}| \geq 1. \] (1)

Figure 2 shows a schematic of a CMOS inverter and an illustration of the voltage transfer curve (VTC) at a low supply voltage V_{DD}. The V_{DD} is set to a lower voltage than the threshold voltage V_{TH} of the MOSFET and thus MOSFETs are operated in the subthreshold region. In the subthreshold region, the drain current of the MOSFET is given by

\[ I_D = I_0 \exp \left( \frac{V_{GS} - V_{TH}}{\eta V_T} \right) \left( 1 - \exp \left( -\frac{V_{DS}}{V_T} \right) \right). \] (2)

where \( I_0 = -\mu C_{OX}(W/L)(\eta - 1)V_T^2 \) is the pre-exponential factor of the subthreshold current, \( \mu \) is the carrier mobility, \( C_{OX} (= \varepsilon_{OX}/L_{OX}) \) is the gate-oxide capacitance, \( \varepsilon_{OX} \) is the oxide permittivity, \( t_{OX} \) is the oxide thickness, \( W/L \) is the aspect ratio, \( W \) is the channel width, \( L \) is the channel length, \( \eta \) is the subthreshold slope factor, \( V_T (= k_B T/q) \) is the thermal voltage, \( k_B \) is the Boltzmann constant, \( T \) is the absolute temperature, \( q \) is the elementary charge, \( V_{GS} \) is the gate-source voltage, and \( V_{DS} \) is the drain-source voltage of the MOSFET.⁴¹⁻⁻⁴²

![Fig. 1. Schematic of the ring oscillator (ROSC).](image-url)
The switching voltage of the CMOS inverter can be derived on the condition that currents flowing into both the nMOSFET and pMOSFET are equal ($I_N = I_P$), and is given by

$$V_{IN} = \frac{V_{DD} + (V_{THN} - |V_{THP}|)}{2} + \frac{\eta V_T}{2} \ln \left[ \frac{I_{OP}}{I_{ON}} \left( 1 - \exp \left( \frac{V_{OUT} - V_{IN}}{V_T} \right) \right) \right]. \quad (3)$$

From Eq. (3), the voltage gain of the inverter $A_{INV} (=\partial V_{OUT}/\partial V_{IN})$ can be calculated as

$$A_{INV} = \frac{2}{\eta} \left\{ 1 - \exp \left( \frac{V_{OUT} - V_{IN}}{V_T} \right) \right\} \left\{ 1 - \exp \left( -\frac{V_{OUT} - V_{IN}}{V_T} \right) \right\}. \quad (4)$$

The $A_{INV}$ becomes maximum ($|A_{INV}|_{MAX}$) when $V_{OUT} = V_{DD}/2$, and is expressed as

$$|A_{INV}|_{MAX} = \frac{1}{\eta} \left\{ \exp \left( \frac{V_{DD}}{2V_T} \right) - 1 \right\}. \quad (5)$$

Note that, as shown in Eq. (5), the voltage gain of the CMOS inverter decreases as $V_{DD}$ decreases.

As shown in Eq. (3), the VTC strongly depends on the threshold voltage difference $\Delta V_{TH} (=V_{THN} - |V_{THP}|)$ between the nMOSFET and pMOSFET. The VTC shifts according to the value of $\Delta V_{TH}$ [see Fig. 2(b)]. Thus, we consider using this characteristic to improve the voltage gain of the inverter.

Figure 3(a) shows a schematic of our proposed self-bias inverter (SBI). The SBI consists of two inverters. The output voltage of the feedback inverter is connected to the body of the main inverter and controls the $V_{TH}$ of the main inverter’s MOSFETs. The threshold voltage is expressed as

$$V_{TH} = V_{TH0} + \gamma (\sqrt{2}|\phi_F| - V_{BS} - \sqrt{2}|\phi_F|), \quad (6)$$

where $V_{BS}$ is the body-source voltage, $V_{TH0}$ is the threshold voltage at $V_{BS} = 0$ V, $\gamma$ is the proportional factor, and $\phi_F$ is the surface potential.43)

When $V_{IN}$ is low, $V_{OUT}$ and the output voltage of the feedback inverter become high and low, and $V_{THL}$ and $V_{THN}$ become low and high, respectively. Therefore, $\Delta V_{TH}$ is higher than 0 V ($\Delta V_{TH} > 0$). On the other hand, when $V_{IN}$ is high, $V_{OUT}$ and the output voltage of the feedback inverter become low and high, and $V_{THL}$ and $V_{THN}$ become high and low, respectively. Therefore, $\Delta V_{TH}$ is lower than 0 V ($\Delta V_{TH} < 0$). Thus, the VTC of our SBI comes close to two curves and the voltage gain is significantly improved, as shown in Fig. 3(b).

The maximum voltage gain of the SBI can be calculated by differentiating Eq. (3) with $V_{IN}$ and is given by
Transistor sizes of our circuit.

| Transistor | L/W       |
|------------|-----------|
| pMOSFET    | 1.0 μm/10 μm |
| nMOSFET    | 1.0 μm/3.3 μm |

\[
[|\text{INV}|_{\text{MAX}} = \frac{\partial V_{\text{OUT}}}{\partial V_{\text{IN}}} \]

\[
= \left\{ 1 - \frac{1}{2} \frac{\partial (\Delta V_{\text{TH}})}{\partial V_{\text{IN}}} \right\} \left\{ 1 + \exp \left( \frac{V_{\text{DD}}}{2V_T} \right) - 1 \right\}. \tag{7}
\]

By comparing Eq. (7) with Eq. (5), the voltage gain of the SBI is improved by \(1 - (1/2) \cdot \partial (\Delta V_{\text{TH}})/\partial V_{\text{IN}}\). From Eq. (6), the term can be calculated as

\[
\left\{ 1 - \frac{1}{2} \frac{\partial (\Delta V_{\text{TH}})}{\partial V_{\text{IN}}} \right\}
\]

\[
= 1 + \frac{1}{4} \left( \frac{1}{\sqrt{2} |\phi_F| - V_B} + \frac{1}{\sqrt{2} |\phi_F| - V_B + V_{\text{DD}}} \right) \frac{\partial V_B}{\partial V_{\text{IN}}}. \tag{8}
\]

where \(V_B\) is the body bias voltage. In Eq. (8), \(\partial V_B/\partial V_{\text{IN}}\) is positive because the \(V_B\) is generated by using the feedback inverter, and thus the term shown in Eq. (8) is larger than 1. Therefore, the maximum voltage gain of the SBI is improved compared with that of the conventional inverter.

Note that as a similar body bias technique, the dynamic threshold-voltage MOSFET (DTMOS) can also improve the voltage gain of the inverter.\(^{44}\) The DTMOS controls the body bias voltage by using \(V_{\text{IN}}\). Therefore, the maximum voltage gain can also be given by Eq. (7). However, the maximum voltage gain is less than that of our proposed SBI. This is because \(\partial V_B/\partial V_{\text{IN}}\) in our SBI is larger than 1 thanks to the feedback inverter, while \(\partial V_B/\partial V_{\text{IN}}\) in DTMOS is equal to 1. Therefore, \(\{1 - (1/2) \cdot \partial (\Delta V_{\text{TH}})/\partial V_{\text{IN}}\}\) in the DTMOS inverter is given by

\[
\left\{ 1 - \frac{1}{2} \frac{\partial (\Delta V_{\text{TH}})}{\partial V_{\text{IN}}} \right\}
\]

\[
= 1 + \frac{1}{4} \left( \frac{1}{\sqrt{2} |\phi_F| - V_B} + \frac{1}{\sqrt{2} |\phi_F| - V_B + V_{\text{DD}}} \right). \tag{9}
\]

By comparing Eq. (8) with Eq. (9), the voltage gain of the SBI is larger than that of using DTMOS.

### 3. Simulation results

The proposed SBI was simulated with 0.18 μm standard CMOS technology. Table I shows the transistor sizes of the proposed circuit. The supply voltage \(V_{\text{DD}}\) was set to 60 mV. For comparison, the conventional inverter [Fig. 2(a)] and the DTMOS inverter\(^{44}\) were also evaluated with the same technology and sizing.

Figure 4(a) shows the simulated VTCs. The amplitudes of the conventional inverter, the DTMOS inverter, and the SBI were 48, 53 and 53 mV, respectively. In addition, the output voltage of the SBI changed steeply around the switching voltage. This means that the voltage gain of the SBI is higher than those of the others. Figure 4(b) shows the simulated voltage gain derived from Fig. 4(a). When \(V_{\text{IN}} = V_{\text{DD}}/2 = 30\) mV, the voltage gains reached their maximum values. The maximum gain of the SBI was 119 and it was 15 times higher than that of the DTMOS inverter, 7.7.

An ROSC using the proposed SBIs was designed and simulated with the same technology. For comparison, an ROSC using conventional inverters was also evaluated. Figure 5 shows the simulation test circuits of the ROSCs. The proposed and conventional ROSCs used 31 SBIs and 51 inverters, respectively, to obtain the same frequency.

Figure 6 shows the simulated transient waveforms. The supply voltage \(V_{\text{DD}}\) was set to 60 mV; the amplitude and frequency of the conventional ROSC were 47.5 mV and 64 Hz, respectively, while those of the proposed ROSC were 53.8 mV and 59 Hz, respectively. Figure 7(a) shows the simulated normalized amplitude as a function of \(V_{\text{DD}}\). The amplitude of the proposed SBI was higher than that of the conventional one. The proposed circuit was able to oscillate at an extremely low supply voltage of 40 mV. Figure 7(b) shows the frequency as a function of \(V_{\text{DD}}\). The frequencies of the ROSCs were almost the same as designed.

### 4. Experimental results

We fabricated a prototype chip of our proposed ROSC using 0.18 μm, 1 poly, 6 metal CMOS technology. The conventional ROSC was also fabricated in the same chip. Figure 8 shows a micrograph of our chip. The proposed and conventional ROSCs used 31 and 51 inverters, respectively, to
Fig. 5. Simulation test circuits of ROSCs.

Fig. 6. (Color online) The simulated waveforms of (a) the conventional and (b) the proposed ROSC at $V_{DD} = 60$ mV.

Fig. 7. (Color online) The simulated (a) normalized amplitude and (b) frequency of the ROSCs as a function of $V_{IN}$. 

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obtain the same frequency, and their areas were 0.015 and 0.0029 mm², respectively. The SBI occupied a larger area because the bodies of the main inverters needed to be separated from the substrate in order to control the body bias voltages. In the measurement, we used source follower buffers to sufficiently drive off-chip parasitics. The bias current of the source follower buffer was set to 500 nA.

Figure 9 shows the measured waveforms of (a) the conventional and (b) the proposed ROSC at \( V_{DD} = 60 \) mV. The amplitudes were 52.0 and 41.9 mV, respectively. A higher amplitude was obtained by using our proposed SBI.

Figure 10 shows the measured normalized amplitudes as a function of \( V_{DD} \). The proposed circuit had a higher amplitude than the conventional one, and was able to oscillate at an extremely low supply voltage of 42 mV, while the conventional one oscillated at 51 mV. Figure 11 shows the measured count that was able to oscillate successfully as a function of \( V_{DD} \) in nine samples. In all samples, the proposed ROSC was able to oscillate successfully at \( V_{DD} = 42 \) mV. On the other hand, the minimum \( V_{DD} \) of the conventional one was 52 mV.

Figure 12 shows the measured normalized amplitude of the proposed ROSC as a function of \( V_{DD} \) at different temperatures. The amplitude of the ROSC decreased and the minimum \( V_{DD} \) increased as the temperature increased. This was because the subthreshold leakage currents of the off-state MOSFETs increased and the voltage gains of the inverter degraded. Figure 13 shows the measured minimum \( V_{DD} \) of the ROSCs as a function of temperature. Both circuits showed almost the same temperature dependence.

Figure 14 shows the measured (a) frequency and (b) power consumption as a function of \( V_{DD} \). The measured frequency and power of our proposed ROSC was slightly slower and higher, respectively, because of the additional feedback inverters. Figure 15 shows the measured (a) frequency and (b) power consumption as a function of \( V_{DD} \) at different temperatures. The frequency and power increased because the current increased with temperature.
Fig. 11. (Color online) The measured count of $V_{DD}$ where (a) the conventional and (b) the proposed ROSCs were able to oscillate (nine samples in total).

Fig. 12. (Color online) The measured normalized amplitude of the proposed ROSC as a function of $V_{DD}$ with temperature as a parameter.

Fig. 13. (Color online) The measured minimum $V_{DD}$ of the ROSCs as a function of temperature.
For comparison, Table II summarizes the performance of the proposed ROSC and others. The proposed ROSC achieved the lowest minimum supply voltage, 42 mV.

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