A 101 dB dynamic range, 2 kHz bandwidth delta-sigma modulator with a modified feed-forward architecture

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Abstract: This paper presents a modified feed-forward (FF) delta-sigma modulator architecture that simplifies the switched-capacitor network of an analog adder in front of the quantizer. By eliminating the internal FF path from the first integrator output, the number of capacitors in the analog adder is reduced and the load capacitance of the first integrator becomes independent of the quantizer resolution. To verify the proposed modulator architecture, a three-bit second-order delta-sigma analog-to-digital converter (ADC) is implemented. The prototype ADC is fabricated in a 0.18 µm CMOS process with an active die area of 0.095 mm². It achieves a dynamic range (DR) of 101.0 dB and a peak signal-to-noise and distortion ratio (SNDR) of 97.1 dB in a 2 kHz signal bandwidth while consuming 63.4 µW from a 1.8 V/1.65 V power supply.

Keywords: analog-to-digital converter, delta-sigma modulator, switched-capacitor, low-distortion, feed-forward

Classification: Integrated circuits

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1 Introduction

A delta-sigma analog-to-digital converter (ADC) is well suited for high resolution sensor interface systems with a narrow input signal bandwidth as it can make oversampling more attractive [1, 2, 3, 4]. Among the various architectures, the low-distortion feed-forward (FF) modulator shown in Fig. 1 [5] has been widely used. In this architecture, the design requirement of analog circuit is relaxed since each integrator processes only quantization noise. Meanwhile, a modulator with a multi-bit internal quantizer not only reduces the quantization noise but also linearizes the feedback loop, thus further relaxing the design requirement of the loop filter. Combining the FF architecture with a multi-bit quantizer is beneficial particularly in a scaled-down low-voltage technology, as it reduces the signal swing range of the integrator.

However, the conventional FF architecture with a multi-bit quantizer suffers from the complex design of an analog adder that is placed in front of the quantizer. A switched-capacitor passive adder is favored in low-power applications since it does not use an additional amplifier that is required in an active adder [6, 7, 8, 9]. For the passive summation in [6], the signal attenuation caused by the charge sharing increases the comparator accuracy requirement. Furthermore, the load capacitance of the first integrator increases in proportion to the quantizer resolution, thus deteriorating the power efficiency. In [7], the signal attenuation caused by the input parasitic capacitance of the comparator is compensated by using extra capacitors. However, the input of the comparator is attenuated by one-fourth due to the charge sharing between the sampling capacitors of each signal path. In [8],

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the passive adder is simplified by removing the internal FF path, thus the signal attenuation factor is reduced from one-fourth to one-half. But, it requires an additional multi-bit switched-capacitor digital-to-analog converter (DAC) at the input of the second integrator.

In this paper, an area and power efficient second-order FF delta-sigma modulator architecture is presented. By employing only one extra capacitor, the internal FF path is removed thus the switched-capacitor network of the passive adder is simplified while maintaining the benefits of the conventional FF architecture. The load capacitance of the first integrator becomes independent of the quantizer resolution.

The rest of this paper is organized as follows. Section 2 introduces the architecture of the proposed modulator. The circuit implementation details are described in Section 3. Measurement results are presented in Section 4, followed by the conclusion in Section 5.

2 Architecture

Fig. 2 illustrates the z-domain block diagram of the proposed second-order FF delta-sigma modulator. The modulator consists of two integrators, a quantizer with an adder and an analog signal processing block, $H_A(z)$, whose transfer function is equal to $2 - z^{-1}$. The internal FF path from the first integrator in [5] is removed by employing the $H_A(z)$. Each integrator output of the proposed architecture contains only quantization noise as given by

$$V_1(z) = Q(z) \cdot z^{-1/2} \cdot (1 - z^{-1}) \quad (1)$$

$$V_2(z) = Q(z) \cdot z^{-1} \cdot (2 - z^{-1}) \quad (2)$$

where $V_1(z)$ and $V_2(z)$ denote the outputs of the first and the second integrator, respectively.

In this architecture, the switched-capacitor network of the quantizer is simplified by removing the internal FF path, thus minimizing the number of unit capacitors for the passive adder. Moreover, the load capacitance of the first integrator becomes independent of the quantizer resolution. To verify the proposed architecture, a second-order delta-sigma modulator with an oversampling ratio (OSR) of 256 and a three-bit quantizer is designed. The gain coefficients of both integrators in the modulator are set to unity. The maximum achievable
The signal-to-quantization noise ratio (SQNR) is 125.6 dB with the chosen modulator architecture.

### 3 Circuit implementations

The schematic diagram of the proposed modulator is illustrated in Fig. 3 with its timing diagram. The loop filters are composed of stray-insensitive switched-capacitor integrators operating with two-phase non-overlapping clocks $\phi_1$ and $\phi_2$. The input sampling switches are implemented as constant-$V_{GS}$ bootstrapped switches [10] to reduce the sampling switch nonlinearity. A chopper stabilization technique [11] is employed to reduce the low frequency noise in the band of interest. Moreover, a data weight averaging (DWA) technique [12] is adopted to reduce the distortion resulting from the capacitance mismatch of an eight-level capacitive DAC. The total sampling capacitance of the first integrator is chosen as 2 pF by considering the $kT/C$ noise requirement.

The transfer function $H_A(z)$ in Fig. 2 is implemented with the switched-capacitor network of the second integrator. An additional capacitor $C_{S2A}$ and a clock phase $\phi_{ON}$ are used. The operation of the second integrator is as follows. During the $\phi_1$ phase, the first integrator output $V_1[n - 1/2]$, which is equal to the previous output $V_1[n - 1]$, is sampled in $C_{S2}$. During the following $\phi_2$ phase, $V_1[n]$ is connected to both $C_{S2}$ and $C_{S2A}$ and the second integrator output $V_2[n]$ is increased by $2 \cdot V_1[n] - V_1[n - 1]$.

A three-bit flash type quantizer is used in the proposed modulator. Each comparator consists of four unit capacitors and a regenerative latch as shown in Fig. 3. Since the number of unit capacitors is reduced by half compared to that in [5], the attenuation factor resulting from the charge sharing is reduced, thus the accuracy requirement of the comparator is relaxed.

In the proposed FF delta-sigma modulator, the output swing range of the amplifiers in each integrator is less than 20% of the full-scale, and, thus an efficient single-stage telescopic amplifier is employed. The NMOS input devices are adopted to maximize the $g_m/I_D$ efficiency. Both input devices are designed to operate in a subthreshold region to enhance the noise performance [13].
4 Measurement results

The prototype delta-sigma modulator was fabricated in a 0.18 µm CMOS process. Fig. 4 shows the die photograph of the prototype delta-sigma modulator. It occupies an active area of 0.095 mm². The measured output spectrum of the prototype modulator is shown in Fig. 5. A 101.0 dB dynamic range (DR) is measured with the shorted input. The prototype chip achieves a peak signal-to-noise ratio (SNR) and a signal-to-noise and distortion ratio (SNDR) of 98.2 dB and 97.1 dB, respectively, with a 497 Hz, −2 dBFS sinusoidal input. Fig. 6 shows the measured SNR and SNDR versus the input signal amplitude. Operating at 1.024 MHz of clock frequency, the modulator consumes 63.4 µW from a 1.8 V and a 1.65 V power supply, achieving a Schreier’s figure of merit (FoMS) of 176.0 dB. The measured performance of the prototype chip and comparison with previous works are summarized in Table I.
Table I. Performance summary

|                      | This work | [3]  | [4]  |
|----------------------|-----------|------|------|
| Process [µm]         | 0.18      | 0.35 | 0.18 |
| Supply voltage [V]   | 1.8/1.65  | 5.0  | 1.8  |
| Sampling frequency [MHz] | 1.024    | -    | 5.0  |
| Bandwidth [kHz]      | 2         | 1.2  | 1.67 |
| DR [dB]              | 101.0     | 113.7| 96.5 |
| SNR [dB]             | 98.2      | 105.2| 96.3 |
| SNDR [dB]            | 97.1      | -    | 91.8 |
| Power consumption [mW] | 0.063    | 12.6 | 0.083|
| FoMS\(^\dagger\) [dB] | 176.0    | 163.4| 169.5|
| Area [mm\(^2\)]     | 0.095     | 5.320| 0.350|

\(^\dagger\)FoMS = DR + 10 \cdot \log_{10}(BW/Power)
5 Conclusion

This paper presents a modified FF delta-sigma modulator topology. The proposed architecture simplifies the switched-capacitor passive adder by eliminating the internal FF path from the first integrator output to the quantizer input. It enables a smaller-sized passive adder for a multi-bit quantizer with relaxed design requirements of the comparator. Furthermore, the load capacitance of the first integrator becomes independent of the quantizer resolution. The prototype chip achieves a peak SNDR of 97.1 dB and a DR of 101.0 dB over a 2 kHz signal bandwidth while consuming 63.4 µW of power.

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