Quality Control of Thick Film Hybrid Integrated Circuit Process Design and Manufacturing

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Abstract. With the continuous upgrading of the technological content of electronic products, higher requirements have been put forward for the manufacturing process of thick film hybrid integrated circuits, resulting in the manufacturing process of thick film hybrid integrated circuits. Thick-film hybrid integrated circuits are an important realization method of microelectronic components. They are widely used in many fields such as civil, military, and aerospace satellites. An important reason is that the thick film process has a super high cost performance compared with other process realization methods. Thick film conductive paste is the most core material in the thick film process. Its interconnection performance such as sintering and welding directly affects the performance of the finished thick film components. Therefore, the thick film conductive paste interconnection under specific process conditions is evaluated. Related performance is crucial. In the mass production process of thick film hybrid integrated circuits, it is particularly important to control the quality and increase the product growth rate. This paper introduces the description of the quality management of the rear-film hybrid integrated circuit production line in the aspects of thick-film hybrid integrated circuit quality system construction, raw material procurement, supplier management, project quality management, on-site management, etc. The manufacturing process of the back-film hybrid integrated circuit briefly introduced has stable performance, high reliability and wide application fields in terms of manufacturing characteristics. Studies have shown that the manufacturing process is suitable for mass automated production, and has the advantages of simple process, low investment, and quick results.

Keywords: Thick Film Hybrid Integrated Circuits, Circuit Process Design, Quality Control, Thick Film Components

1. Introduction
Various fields of modern society favor small, durable and cheap electronic products with high cost performance. With the continuous upgrade of actual needs, the requirements for the packaging field are becoming increasingly strict. There are also such problems in the development and application of thick film devices [1-2]. The thick-film hybrid integrated circuit technology it relies on has been developed by leaps and bounds over the years, and has become an important means for the mass production of widely used microelectronic devices. Thanks to the increasingly advanced semiconductor-related processes, the maturity of thick film technology is indispensable, and the core material surrounding the thick film process is the thick film paste [3].

Thick film hybrid integrated circuit (THIC) refers to the use of thick film technology on an insulating substrate to generate manual components and their interconnections. In order to install semiconductor devices and other manual components, functional microcircuits using thick film assembly technology [4-5]. It can be seen from here that thick film assembly technology is full of SMT technology. Thick-film hybrid integrated circuits are basically micro-assembly technology. The basic content of micro-assembly is to assemble parts on the substrate, assembling the substrate and the metal shell [6]. Among them, the assembly parts on the substrate mainly include Bell chip assembly and chip component assembly. The two main methods of assembling chip components on a substrate are conductive epoxy soldering and terminal soldering. Compared with the welding process, the obvious advantage of conductive epoxy welding is that there is no residue after welding and no additional cleaning process is required [7]. Most thick film hybrid integrated circuits have PIND control requirements, so strict internal visual inspection and internal overload are required. Therefore, conductive epoxy soldering is widely used in thick film hybrid integrated circuits in order to realize the assembly of chip components[8].

In practical applications, thick film hybrid integrated circuits have shown better performance than semiconductor integrated circuits in many aspects such as analog and digital circuit hybrids, high power circuits, high voltage circuits, microwave circuits, and fixed dense linear circuits. High-frequency linear circuit, high stability indifferent network, low-noise circuit, etc. [9]. Due to the development of the chip scale of semiconductor integrated circuits, thick-film hybrid integrated circuits have more multi-functional and high-density external components [10]. Hybrid integrated advanced assembly technology and thick film multilayer wiring technology have become the main development direction of thick film hybrid integrated circuits in the future.

2. Algorithm Establishment

2.1. The Establishment of Particle Swarm Algorithm

First set in a D-dimensional vector space. Since the i-th particle shown in a search set composed of N different particles is represented as a D-dimensional vector, as shown in formula (1):

$$X_i = (x_{i1}, x_{i2}, ..., x_{iD}) , i = 1, 2, ..., N$$

(1)

Then the flying speed of the i-th particle is also a D-dimensional vector which is the same as formula (1), which is recorded as formula (2):
\[ V_i = (v_{i1}, v_{i2}, ..., v_{iD}), \ i = 1,2, ..., N \] (2)

The optimal position of the i-th particle searched from the beginning to the current position becomes the individual extreme number, which is recorded as the formula (3):

\[ P_{best} = (P_{i1}, P_{i2}, ..., P_{iD}), \ i = 1,2, ..., N \] (3)

\[ g_{best} = (g_{1}, g_{2}, ..., g_{D}), \ i = 1,2, ..., N \] (4)

When the searched number is the ideal extreme value, the speed and position information of the particles are updated according to formula (5) and formula (6).

\[ v_{ij}(t + 1) = v_{ij}(t) + c_1 r_1 (p_{ij}(t) - x_{ij}(t)) + c_2 r_2 (p_{g}(t) - x_{ij}(t)) \] (5)

\[ x_{ij}(t + 1) = x_{ij}(t) + v_{ij}(t + 1) \] (6)

In the above formula, c_1 and c_2 are two different learning factors in the particle swarm optimization algorithm, r_1 and r_2 are two randomly generated numbers between 0 and 1. The postgraduate entrance examination increases the particle search. The process randomness at the optimal time. v_{ij} (t) represents the velocity of a particle in a group, and the user can set the maximum value of the particle velocity according to their actual problems.

2.2. Improved Particle Swarm Optimization Algorithm

Then the velocity and position change formula of the d-dimensional component of the i-th particle in the target search space is as follows:

\[ v_{id}(t + 1) = w v_{id}(t) + c_1 r_1 (p_{id}(t) - x_{id}(t)) + c_2 r_2 (p_{g}(t) - x_{id}(t)) \] (7)

\[ x_{id}(t + 1) = v_{id}(t + 1) + x_{id}(t) \] (8)

\[ w = w_s - (w_s - w_e) \cdot \frac{g}{g_{max}} \] (9)

The update formula of particle velocity is as follows:

\[ v_{id}(t + 1) = w v_{id}(t) + c_1 r_1 (p_{id}(t) - x_{id}(t)) + c_2 r_2 (p_{g}(t) - x_{id}(t)) + c_3 r_3 (s_{id}(t) - x_{id}(t)) \] (10)

2.3. Optimization of Particle Algorithm Speed and Position Update

Define similarity

The rules for determining the similarity between particles and other particles in the population are as follows:

\[ S_1 = F_i \cap F_j \]

\[ S_2 = F_i \setminus F_j \] (11)

At the same time, to measure the characteristics of other particle species in the algorithm
population and the characteristics and degree of particle i against the defined index, calculate according to formula (12):

\[
\text{Con}_1 = \frac{|S_i|}{|F_i|} \tag{12}
\]

In the above formula (12), the larger the value of [Con]_1, the larger the proportion of the number of common features between particles to the number of features of the particle i.

Based on the above-mentioned similarity rule, the known number of the similarity of particle i is calculated according to formula (13):

\[
\text{SIM}_i = \frac{|\text{Sim}_i|}{N} \tag{13}
\]

Finally, perform interactive operations on the particles, but before the interactive operations, the user must first calculate the interaction probability of particle i according to formula (14) as shown in (14):

\[
\text{Interrate}_i = (1-\text{SIM}_i) \times e^{-\text{SIM}_i} \tag{14}
\]

3. Modeling Method

3.1. The Original Gray Gm(1,1) Prediction Model

Assume that the original sequence 3.1 The original gray GM(1,1) prediction model where \(x^{(0)}(k) \geq 0\), \(k=1,2,...,n\) do 1-AGO to the original sequence, that is, accumulate \(X^{(0)}\) to generate a sequence \(X^{(1)}\), and get the sequence:

\[
X^{(1)} = \{X^{(1)}(1),X^{(1)}(2),...X^{(1)}(n)\} \tag{15}
\]

Among them

\[
x^{(1)}(k) = \sum_{i=1}^{k} x^{(0)}(i) \tag{16}
\]

Make the immediate mean change on the sequence \(X^{(1)}\) to get:

\[
z^{(1)} = \{z^{(1)}(2),z^{(1)}(3),...,z^{(1)}(n)\} \tag{17}
\]

Among them:

\[
z^{(1)}(k + 1) = 0.5x^{(1)}(k + 1) + 0.5x^{(1)}(k) \quad (k = 1,2,...,n) \tag{18}
\]

Definition: Let \(x^{(0)}(k)\) and \(z^{(1)}(k)\) as described above, say:

\[
x^{(0)}(k) + a z^{(1)}(k) = b \tag{19}
\]
It is the mean value form of the gray differential equation of the GM(1,1) model or the gray differential equation of the gray model GM(1,1) model.

The traditional gray modeling process calculates parameter variables using the least square method to estimate:

\[ x^{(0)}(k) + az^{(1)}(k) = b \]  

(20)

GM(1,1) has the whitening differential equation of the GM(1,1) model equivalent to the gray differential equation of the model, also known as the whitening type of the GM(1,1) model:

\[ \frac{dx^{(1)}}{dt} + ax^{(1)} = b \]  

(21)

Finally, a first-order cumulative reduction of \( x^{(1)}(k) \) is performed to obtain the final simulation and predicted value:

\[ \hat{x}^{(0)}(k + 1) = \hat{x}^{(1)}(k + 1) - \hat{x}^{(1)}(k) \]  

(22)

4. Evaluation Results and Research

The thick film circuit conduction band provides the connection between the various components on the circuit. Due to the use of layered screen printing and sintering, it is easy to produce defects such as pattern defects or uneven film thickness during the production process, resulting in open circuits and layers. However, semiconductor chips are more expensive, and components can hardly be removed and repaired after mounting. Therefore, in order to obtain a high initial yield, the electrical interconnection inspection before device assembly is particularly important. The interconnection test of the circuit is carried out after each sintering. The resistance test method is adopted, that is, a certain voltage is applied between the tested circuits, the current value passing through the interconnection line is tested, and the resistance value of the conduction band is calculated.

After the thick film hybrid integrated circuit is assembled, when the working voltage is 5.03V, the measured working current is 37.4mA, and the output in three directions when placed horizontally. Table 1 shows the sensor output values calculated based on the output waveform of the thick film hybrid integrated circuit.

| Axial | Design range (g) | Stop bit | AD output | Start bit | Decimal | Reference voltage (V) | Output value (V) | Theoretical value (V) |
|-------|------------------|----------|------------|-----------|---------|----------------------|------------------|----------------------|
| X     | 500              | 1        | 01011100   | 0         | 92      | 3.36                 | 2.415            | 2.425                |
| Y     | 500              | 1        | 01011000   | 0         | 88      | 3.36                 | 2.310            | 2.296                |
Stability is an important indicator that determines whether thick film hybrid integrated circuits can be used. For the unstable factors of the thick-film hybrid integrated circuit itself, the necessary stability treatment should be carried out on the materials, components or the entire thick-film hybrid integrated circuit. The main indicators investigated are sometimes drift stability and temperature drift stability. The zero time drift of the thick film hybrid integrated circuit is calculated as follows:

\[
\text{Zero time drift } = \frac{\Delta Y_0}{Y_{FS}} \times 100\%
\]

Among them: \( \Delta Y_0 \) —— Maximum zero point deviation;

\( Y_{FS} \) —— full-scale output value.

The time-drift test starts to test output after the thick film hybrid integrated circuit is powered on for 30 minutes, and the reading interval is 20 min. The test data is shown in Figure 1, which includes the effects of room temperature changes and power supply voltage fluctuations.

![Graph](image)

**Figure 1.** Time drift test of thick film hybrid integrated circuit

The calculated time drift is: X: 0.24% Y: 0.13% Z: 0.27%

The temperature drift indicates the deviation degree of the output value of the thick film hybrid integrated circuit when the temperature changes. It can be calculated as follows:

\[
\text{Temperature drift } = \frac{\Delta \text{max}}{Y_{FS} \cdot \Delta T} \times 100\%
\]

Among them: \( \Delta \text{max} \) —— output maximum deviation;

\( \Delta T \) —— The temperature change range.

In the zero temperature drift test, the thick film hybrid integrated circuit is placed in a high and low
temperature box, when the working temperature is -40 C to 60. Measure the output of the thick-film hybrid integrated circuit during C-crossing, and the measurement interval is 20°C. The test result is shown in Figure 2.

![Figure 2. Temperature drift test of thick film hybrid integrated circuit](image)

The calculated temperature drift is: X: 0.96% Y: 0.88% Z: 0.86%

It can be seen from the test results that the thick-film hybrid integrated circuit has better stability.

Although the thick film hybrid integrated circuit has completed the production of samples, some problems have also been exposed during the hybrid integration and testing of the circuit, mainly as follows:

1. For the adhesion of the mixed-bonded conductor, after 10 times of sintering, the adhesion is reduced by about 10-15%, because the glass component in the conductor continuously penetrates into the semi-porous alumina ceramic during multiple sintering processes. In the substrate, the glass in the metal layer is continuously reduced, which reduces the bonding force. The dielectric properties also change with the increase of the number of sintering, the dielectric constant and dielectric loss will increase, but the insulation resistance and dielectric strength will decrease.

2. The medium slurry is too long during storage, and the viscosity is too large, which will block the mesh during printing.

3. The use of chip resistors for the bridge leveling resistors in the circuit cannot achieve high accuracy. If thick film printed resistors are used and combined with laser active resistance trimming, the resistance value can reach high accuracy, which can make thick film The zero bias of the hybrid integrated circuit is very small.

4. In the mixed assembly process, the epoxy glue needs to be heated at 150° C to cure for 1 hour during each placement. Relevant data and practice show that the chip component resistors, capacitors and operational amplifiers can withstand multiple thermal curing.
5. Conclusion

The quality control of thick film hybrid integrated circuits is a meticulous and huge project. The whole process completely shows the whole process of thick film hybrid integrated circuit process design and quality control. It also reflects the continuity of the process, and it must be strict The quality control system is guaranteed. Through the technical research of typical thick-film hybrid integrated circuits, this paper proves the correctness of thick-film hybrid integrated circuits and the feasibility of processing technology. However, many research and experimental work are needed to put into practical application. In the process of realization, there were some unconsidered problems, so a large number of process matching tests were included in the production process. During the research period of the subject, due to the limitations of technology and experimental conditions, as well as many factors that affect the performance of thick film hybrid integrated circuits, there are many related details that have not been discussed and studied in depth, and more practical experience is required. Carry out device design and process adjustment.

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