Tuesday October 27

12:00  Opening

12:20  Keynote 1

Compressive sensing (CS) Circuits and Systems for Intelligent Biomedical Signal Processing

Andy Wu, National Taiwan University, Taiwan

13:20  Plenary 1

13:20  HyVE: A Hybrid Voting-based Eviction Policy for Caches

Akshay Srivatsa, Sebastian Nagel, Nael Fasfous, Nguyen Anh Vu Doan, Thomas Wild, Andreas Herkersdorf, Technical University of Munich, Germany

13:40  Multi-threshold voltage and dynamic body biasing techniques for energy efficient ultra low voltage subthreshold adders

Somayeh Zadeh, Trond Ytterdal, Snorre Aunet, NTNU, Norway

14:00  Break

14:20 – 16:00 Parallel sessions

14:20  Data Converters

14:20  A 10b 1GS/s Inverter-Based Pipeline ADC in 65nm CMOS

Timmy Sundström1, Javad Bagheri Asli2, Christer Svensson2, Atila Alvandpour2

1) SAAB AB Linköping, Sweden; 2) Linköping University, Sweden

14:40  A 10-bit 3.75-GS/s Binary-Weighted DAC with 58.6-pJ Energy Consumption in 65-nm CMOS, Oscar Morales1, Jacob Wikner1, Atila Alvandpour1, Liter Siek2

1) Linköping University, Sweden; 2) Nanyang Technological University, Singapore

15:00  Digital Timing Error Calibration of Time-Interleaved ADC with Low Sample Rate

Marko Neitola, University of Oulu, Finland

14:20  Scheduling, Approximation and Error Resilience

14:20  Low Power Scheduling of Periodic Hardware Tasks in Flash-Based FPGAs

Cornelia Wulf, Michael Willig, Diana Göhringer, Technische Universität Dresden, Germany

14:40  Model-Based Design Space Exploration for Approximate Image Processing on FPGA

Manu Manuel1, Arne Kreddig2, Simon Conrady1, Nguyen Anh Vu Doan1, Walter Stechele1

1) Technical University of Munich, Germany; 2) SmartRay GmbH, Germany;

3) Arnold & Richter Cine Technik, Germany

15:00  Novel Lockstep-based Approach with Roll-back and Roll-forward Recovery to Mitigate Radiation-Induced Soft Errors

Server Kasap, Eduardo Weber Wächter, Xiaojun Zhai, Shoaib Ehsan, Klaus D. McDonald-Maier, University of Essex, United Kingdom
Amplifiers

15:20 Schmitt Trigger Based Single-Ended Voltage Amplifier with Positive Feedback Control for Ultra-Low-Voltage Supplies
Luis Henrique Rodovalho, Federal University of Santa Catarina, Brazil

15:40 On the Design of a CMOS-integrated Load Modulated Balanced Amplifier
Ted Johansson, Srivatsa Samji, Linköping University, Sweden

FPGA Applications

15:20 A FPGA-based Hardware Accelerator for Bayesian Confidence Propagation Neural Network
Lizheng Liu¹,², Deyu Wang¹, Yuning Wang¹, Anders Lansner², Ahmed Hemani², Yu Yang²,
Xiaoming Hu², Zhuo Zou¹, Lirong Zheng¹
1) Fudan University, Shanghai, China;
2) Royal Institute of Technology (KTH), Stockholm, Sweden

15:40 A Parallel and Pipelined Implementation of a Pascal-Simplex Based Two Asset Option Pricer on FPGA using OpenCL
Aidan O Mahony¹, Gil Zeidan², Bernard Hanzon¹, Emanuel Popovici¹
1) University College Cork, Ireland; 2) Intel Corporation, Massachusetts, USA

15:20

15:40

16:00 Break

16:20

Keynote 2

Approximate Computing: Test and Reliability issues and opportunities
Alberto Bosio, INL-ECL, France

17:20 End of day 1

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Wednesday October 28

12:00

Keynote 3

to be confirmed

Tim Constandinou, Imperial College, UK

13:00

Plenary 2

13:00 A Design Method to Minimize the Impact from Bit Conversion Errors in SAR ADCs
Siyu Tan¹, Mattias Palm², Daniele Mastantuono², Roland Strandberg², Lars Sundström², Sven Mattisson¹,², Pietro Andreani¹
1) Department of Electrical and Information Technology, Lund University, Lund, Sweden;
2) Ericsson Research, Lund, Sweden

13:20 Break
13:40 – 16:40 Parallel Sessions

13:40 **Biomedical/Bioinspired**

**13:40 A Low Power Front-end for Biomedical Fluorescence Sensing Applications**
Seyed Ruhallah Qasemi, Maryam Rafati, Atila Alvandpour, Linköping University, Sweden

**14:00 A Power Efficient, High Gain and High Input Impedance Capacitively-coupled Neural Amplifier**
Erwin Habibzadeh Tonekabony Shad1, Tania Moeinfard2, Marta Molinas1, Trond Ytterdal1
1) NTNU, Norway; 2) York, Canada

**14:20 Design of a Current Mode Multiplexed Circuit for Integrate & Fire Neuromorphic Systems**
Fausto Sargeni, Vincenzo Bonaiuto, University of Rome Tor Vergata, Italy

13:40 **Digital Circuits and Systems**

**13:40 Comparative Study of Single, Regular and Flip well Subthreshold SRAMs in 22 nm FDSOI Technology**
Somayeh Hossein Zadeh, Trond Ytterdal, Snorre Aunet, NTNU, Norway

**14:00 A 90nm PVT Tolerant Current Mode Frequency Divider with Wide Locking Range**
Madhusudan Maiti1, Shubhro Chakrabartty2, AlaaDin Al-Shidaifat2, Hanjung Song2, Bidyut Kumar Bhattacharyya3, Alak Majumder1
1) Integrated Circuit & System Lab, Department of ECE, National Institute of Technology Arunachal Pradesh, Yupia 791112, India;
2) Department of Nanoscience and Engineering, Centre for Nano Manufacturing, Inje University, Gimhae 50834, Korea;
3) Packaging Research Center, Georgia Institute of Technology, Atlanta, GA 30332, USA

**14:20 Electro-Optic Reversible Toffoli Gate with Optimal Count of LiNbO3 Mach-Zehnder Interferometers**
Shashank Awasthi1, Saurav Sharma2, Sanjeev Kumar Metya1, Alak Majumder1
1) National Institute of Technology Arunachal Pradesh;
2) Galgotias College of Engineering & Technology Greater Noida

14:40 **Analog Circuits**

**14:40 Low Power Class-AB Line Driver with Adaptive Digital Impedance Control for Fast Ethernet**
Simon Buhr, Martin Kreißig, Christian David Matthus, Florian Protze, Frank Ellinger
Technische Universität Dresden, Germany

**15:00 Origins of Intermodulation Distortion in A Pseudo-differential CMOS Beamforming Receiver**
Negar Shabanzadeh1, Mahmoud Shehab2, Rehman Akbar1, Aarno Pärssinen1, Timo Rahkonen1
1) University of Oulu, Finland; 2) Nokia Oyj

14:40 **Digital Applications**

**14:40 Matrix Decomposition for Massive MIMO Detection**
Shahriar Shahabuddin1, Muhammad Hasibul Islam1, Mohammad Shahanewaz Shahabuddin2, Mahmoud A. Albreem1,3, Markku Juntti1
Digital Architecture for MUAPs Propagation Speed Estimator triggered by Foot Plant Switch
Giovanni Mezzina, Daniela De Venuto, Politecnico di Bari, Italy

15:20 Break

15:40 Microwave Circuits

A 500 mV, 4.5 mW, 16 GHz VCO with 33.3% FTR, designed for the 5G application
Piyush Kumar1, Dario Stajic1, Enno Boehme2, Erkan Nevzat Isa2, Linus Maurer1
1) University Bundeswehr; 2) Fraunhofer Research Institution for Microsystems and Solid State Technologies EMFT, Munich, Germany

A Voltage Controlled Oscillator with Inductive Divider Design and Analysis at Frequencies Above 100 GHz
Yasir Shafiullah, Rehman Akbar, Mikko Hietanen, Aarno Pärssinen, University of Oulu, Finland

16:00 A Study of the Impact of Formulation of Cost Function in Task Mapping Problem on NoCs
Jesse Barreto de Barros1, Nidhi Anantharajaiah2, Mauricio Ayala-Rincon3, Carlos Humberto Llanos4, Jürgen Becker5
1) Universidade de Brasilia, Brazil; 2) Karlsruhe Institute of Technology (KIT); 3) Universidade de Brasilia, Brazil; 4) Universidade de Brasilia, Brazil; 5) Karlsruhe Institute of Technology (KIT)

16:20 Synthesizable Synchronization FIFOs Utilizing the Asynchronous Pulse-Based Handshake Protocol
Ameer M.S. Abdelhadi, University of Toronto, Canada

15:40 Network-on-Chip

Exploring Task and Channel Mapping Strategies in Fail-Operational and Hard Real-Time NoCs
Max Koenen, Nguyen Anh Vu Doan, Thomas Wild, Andreas Herkersdorf
Technical University of Munich, Germany

16:00 A Study of the Impact of Formulation of Cost Function in Task Mapping Problem on NoCs
Jesse Barreto de Barros1, Nidhi Anantharajaiah2, Mauricio Ayala-Rincon3, Carlos Humberto Llanos4, Jürgen Becker5
1) Universidade de Brasilia, Brazil; 2) Karlsruhe Institute of Technology (KIT); 3) Universidade de Brasilia, Brazil; 4) Universidade de Brasilia, Brazil; 5) Karlsruhe Institute of Technology (KIT)

Keynote 4

Software-Defined Radio Education and the Next Generation of Wireless Communications Innovators
Alexander Wyglinsky, Worcester Polytechnic Institute, MA, USA

17:40 Awards and Closing