New modulation scheme for bidirectional qZS modular multi-level converters

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Abstract: This study proposes a dedicated modulation scheme for a bidirectional quasi-Z-source (qZS) modular multi-level converter. The operation principle and a suitable pulse-width modulation method are proposed. The relation between the modulation index and shoot-through duty ratio for any number of voltage levels is derived. A formula for calculating the required value of qZS capacitance is given. The simulation results presented in the study validate the operation and the performance of the proposed topology.

1 Introduction
Multi-level inverters (MLIs) are preferred due to their attractive features compared with two-level voltage source inverters (VSIs) [1] such as better AC voltage quality, low voltage stress on semiconductors, possibility to produce significantly higher voltages than a single-switch voltage rating. The modular multi-level converter (MMC) is a relatively new competitive concept which has been proposed in 2002 [2]. It provides several features such as modularity, voltage, and power scalability and failure management capability in the case of device failures [3]. These advantages favour the MMC for various applications, such as an interface between high-voltage direct current (HVDC) [4] and flexible AC transmission (FACT) systems [5], driving medium-voltage (MV) motors [3], and connecting renewable energy sources such as photovoltaics [6] and wind energy system [7] to MV grids. The output voltage of most renewable energy sources fluctuates with working conditions; therefore, having a converter that can adapt to these fluctuation by being able not only to step down but also to step up the voltage in order to regulate the voltage at the DC-link terminals may be quite useful. Power converter topologies based on the use of the impedance network concept have been proposed in [8] which proposes the implementation of a quasi-Z-source (qZS) MMC. The basic structure of the quasi-Z-source inverter (qZSI) as proposed in [9] is shown in Fig. 1. The operating principle of the qZS network relies on producing a short circuit (shoot through, ST) at inverter DC-link terminals in order to increase the stored energy in the inductors that is later transferred in the qZS capacitors and, finally, this extra voltage adds up to the DC source voltage and provides voltage boosting capability.

There are two operation modes for the qZS network which are ST and non-ST (NST) modes. In the ST mode, the DC-link terminals are shorted by gating both the upper and lower devices of at least one inverter leg, which forces the qZS diode to become reverse biased and therefore behave like an open circuit as shown in Fig. 2a. Hence, the stored energy in the capacitors begins to transfer into the inductors. In the NST mode, the inverter operates by producing active and null voltage states [10] and then D will be forward biased as shown in Fig. 2b; the stored energy in the inductors begins to transfer to the load, which sees \( V_{po} = V_{c1} + V_{c2} \) as its DC-link voltage, and qZS capacitors begin to charge.

Khera et al. [8] proposed the integration of the qZS network with a single-phase MMC to provide voltage boost capability. The proposed circuit faces some limitations which were identified in the same paper, and a solution was proposed by modifying the qZS-MMC to be a bidirectional one (BqZS-MMC).

This paper gives a detailed circuit analysis of the proposed BqZS-MMC. The equivalent circuit of the qZS-MMC with the proper implemented sinusoidal pulse-width modulation (SPWM) boosting scheme is presented which can be extended to any number of output voltage levels. The relation between the modulation index and ST duty ratio for any number of voltage levels is derived. A guideline for choosing the value of qZS capacitance is proposed. Finally, the operation and analysis of the proposed modulation scheme are validated using results simulation from a MATLAB/PLECS model.

2 Operation principles of the bidirectional quasi-Z-source modular multi-level converter
The topology of a single-phase qZS-MMC is shown in Fig. 3. The MMC leg consists of the upper and lower arms where each arm consists of series-connected sub-modules (SMs), and an arm inductor \( L_a \). Each SM has a half-bridge inverter configuration with one DC-link capacitor. The two switches \( S_{ax} \) and \( S_{ax} \) in SM are controlled by complementary gating signals. When \( S_{ax} \) is on, the SM capacitor is bypassed and the SM terminal voltage is zero. If \( S_{ax} \) is off, \( S_{ax} \) is on; therefore, SM terminal voltage is \( V \), and the SM capacitor is inserted into the circuit. Each SM capacitor needs to be charged by a fraction of the DC bus voltage \( E/N \), where \( N \) is the number of SMs per arm. Therefore, the output voltage \( (V_{po}) \) swings between \(-V_{po}/2 \) and \( V_{po}/2 \) and each arm should aim to produce the
In this study, phase disposition SPWM (PD-SPWM) is used to generate these states will be explained in Section 4.

The number of inserted cells in the upper arm by 

$$n_u = \frac{V_{an} - V_{pa}}{2} + \frac{V_{pa} - V_{mn}}{2}$$  \(1\)

From (1), if the upper qZS network is shorted via \(S_{pu}\) i.e. \(v_{pu} = 0\), the upper arm voltage \(v_{pa}\) should be reduced to keep the required output voltage at a certain level which can be achieved by reducing the number of inserted cells in the upper arm by \(N/2\). The same procedure is followed if the lower qZS network is shorted via \(S_{pn}\). In this study, phase disposition SPWM (PD-SPWM) is used to control the MMC arms [11]. \(S_u\) and \(S_n\) have been modulated using the proposed technique as follows.

### 3 MMC capacitors voltage balancing and modulation scheme

#### 3.1 Capacitor voltage balance

MMC requires a voltage balancing strategy to balance and keep the SM capacitor voltages at their desired average values. The implementation of balancing strategies depends on the presence of the redundant states in the MMC arm [10]. The redundant switching state with the strongest effect in facilitating voltage balancing is always selected. The MMC arm capacitor balancing can be achieved by different strategies [10]. The most widely used balancing strategy is based on the sorting method [6] which is summarised in four steps as follows:

1. Measure and sort the upper and lower capacitor voltages.
2. From modulation scheme, determine the number of inserted cells \((n_p, n_n)\) from the upper and lower arms, respectively.
3. If the upper (lower) arm current is positive where the current direction as shown in Fig. 3 is considered as positive, choose the \(n_p\) \((n_n)\) cells with a lower voltage to be inserted. Therefore, the corresponding cell capacitor is discharged and its voltage increases.
4. If the upper (lower) arm current is negative, choose the \(n_p\) \((n_n)\) cell with a higher voltage to be inserted. Therefore, the corresponding cell capacitor is discharged and its voltage decreases.

#### 3.2 Modulation scheme

To synthesise \(n\)-level voltage waveform at the converter AC side where \(n\) equals \(2N−1\), phase disposition SPWM (PD-SPWM) with two complementary reference signals \((v_{mu}, v_{mn})\) is used in this study to control the BqZS-MMC as indicated in Fig. 4. Each carrier is responsible for producing the gating signals of two cells (one from upper and one from lower arm). The reference signals are compared against the carriers to define which leg switches are conducting. The upper (lower) qZS networks can be in the ST mode if the number of upper (lower) inserted cells equals or is higher than \(N/2\). Therefore, the number of inserted cells can be reduced by \(N/2\) to obtain the required voltage level. According to this concept, this modulation scheme can be named as the reduced voltage level waveform at the converter AC side

$$V_{sh,u} = \begin{cases} M_{sh} & 0 < \omega t \leq \theta_1; \pi - \theta_2 < \omega t \leq 2\pi \\ N/2 \times M_{sh} \sin \omega t & \theta_1 < \omega t \leq \theta_2; \pi - \theta_2 < \omega t \leq \pi - \theta_1 \\ 1 & \theta_1 < \omega t \leq \pi - \theta_1 \\ 1 - M_{sh} & \pi < \omega t \leq 2\pi \end{cases}$$  \(2\)

where \(M_{sh}\) is the ST modulating signal height as shown in Fig. 4. In the range from \(\Omega_1\) to \(\pi - \Omega_1\), the number of inserted SMs per arm became lower than \(N/2\), where the ST interval should set at zero, and \(\Omega_1\) is defined by

![Fig. 3 Typical topology of an N-cell single-phase MMC](image)

![Fig. 4 PD-PWM with double reference waveforms, the ST modulation signals and the generated pulses for the RNIC technique](image)

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Table 1 Available voltage levels with clarifying the number of inserted SMs in both the upper and lower arms

| Level number | Voltage level | Number of SMs inserted N = 4 (upper, lower) | (S_u, S_l) |
|--------------|--------------|------------------------------------------|----------|
| 1            | \(-V_{pn}/2\) | 4, 0                                     | 2, 0 (1, 0) |
| 2            | \(-V_{pn}/8\) | 4, 1                                     | 2, 1 (1, 0) |
| 3            | \(-V_{pn}/4\) | 3, 0                                     | 1, 0 (0, 1) |
| 4            | \(-V_{pn}/8\) | 3, 1                                     | 1, 1 (0, 0) |
| 5            | 0             | 2, 1                                     | 0, 1 (0, 1) |
| 6            | \(V_{pn}/8\)  | 2, 2                                     | 0, 2 (0, 1) |
| 7            | \(V_{pn}/4\)  | 2, 3                                     | 0, 3 (0, 1) |
| 8            | 3 \(V_{pn}/8\) | 0, 3                                     | 1, 1 (0, 1) |
| 9            | \(V_{pn}/2\)  | 0, 4                                     | 0, 2 (0, 1) |

![Fig. 5 Modified output voltage reference waveforms according to the ST pulses for the RNIC technique](image)

\[
\begin{align*}
\theta_u &= \sin^{-1}\left(\frac{2}{NM_{sh}}\right) \\
\theta_l &= \sin^{-1}\left(\frac{2}{N}\right)
\end{align*}
\]

The lower ST signal \(V_{sh-l}\) waveform is of the same shape as \(V_{sh-u}\) but shifted by 180° as shown in Fig. 4. The pulses of \(S_u\) and \(S_l\) are generated if the carrier signal \(C_{sh}\) is higher than \(V_{sh-u}\) and \(V_{sh-l}\), respectively. According to \(V_{sh-u}\) and \(V_{sh-l}\) signals, the output voltage reference waveforms \(V_{a+}\) and \(V_{a-}\) for the upper and lower arms are modified as shown in Fig. 5 in order to provide a reduction in the number of inserted cells during these intervals by two cells \((N/2)\). From (2), the instantaneous value of the duty ratio is given by

\[
d_{sh,u} = \begin{cases} 
1 - M_{sh} & 0 < \omega t < \theta_u; \pi - \theta_u < \omega t < 2\pi \\
1 - N/2 \times M_{sh}\sin \omega t & \theta_u < \omega t < \pi - \theta_u; \pi < \omega t < \pi - \theta_u \\
0 & \theta_u < \omega t < \pi - \theta_u
\end{cases}
\]

By integrating (4), the average ST duty ratio \(D_{sh}\) can be calculated which is given by

\[
D_{sh} = \frac{(\pi + 2\theta_u)\left(1 - M_{sh}\right)/2\pi + (\theta_u - \beta)\pi + N M_{sh}(\cos \theta_1 - \cos \beta)}{\pi}
\]

From (5), The DC-link voltage can be expressed by

\[
V_{pn} = \frac{1/(1 - 2D_{sh})}{E/2}
\]

\[
= \frac{\pi}{2\theta_u + M_{sh}(2N(\cos \theta_1 - \cos \beta) - 2\theta_u - \pi)} E
\]

![Fig. 6 Normalised DC-link voltage \(V_{pn}/E\) versus ST modulation index \(M_{sh}\)](image)

Fig. 6 shows the normalised peak DC-link voltage versus ST duty ratio \(M_{sh}\) when \(N = 2, 4, 6, 8,\) and 10. By increasing the number of SM, higher \(M_{sh}\) is required at the same DC-link voltage. The qZS-capacitor voltages are given by

\[
V_{a+} = V_{a-} = (1 - D_{sh}) V_{pn}/2
\]

\[
V_{a+} = V_{a-} = D_{sh} V_{pn}/2
\]

For \(N\) of SMs per arms, the SM capacitor voltages are given by

\[
V_{c-\text{arm}} = V_{pn}/N
\]

From (8), the peak value of the fundamental output voltage is given by

\[
V_n = MNV_{c-\text{arm}}/2 = GE/2
\]

Where \(G\) is given as a function of \(D_{sh}\) (or \(M_{sh}\)) and the output voltage modulation index \(M\) is given by

\[
G = M/(1 - 2D_{sh})
\]

\[
= 3\pi M/[4\pi + 6\sqrt{3} - 12\cos \beta + M_{sh} - 6\theta_1]
\]

4 Choosing values of a passive element

According to [8], using an IGBT in antiparallel to the diode \(D\) in the qZS-network allows the converter to operate with small values of inductance without disturbing the operation of the circuit, being able to completely avoid the undesirable operation modes found in [8], consequently, eliminating any drops in the DC-link voltages that affected the output harmonic distortion. However, the
capacitor voltages any single-phase converters and to \([12]\). The arm inductance and SM capacitance are calculated according to the relevant study and the relations given in \([13]\). In this section, the general relation for determining the proper qZS-capacitance value should be chosen for limiting the ripples to a reasonable level (20%) to reduce the current stress on the converter devices.

The inductance value of the four inductors is chosen according to \([12]\). The arm inductance and SM capacitance are calculated according to the relevant study and the relations given in \([13]\). In this section, the general relation for determining the proper qZS-capacitance value has been obtained. According to \([8]\), the qZS-capacitor voltages \(V_{cu1}\) and \(V_{cu2}\) decrease when the arm current value \(i_{pa}\) decreases than the average value of the inductor current \(I_L\) during both ST and NST modes as indicated in Fig. 7. The interval when the arm current is higher than the average value is from \(0\) to \(\theta_a\) and \(\theta_b\), where \(\theta_a\) and \(\theta_b\) are the two instants when the arm current is equal to \(I_L\). The upper and lower arm currents can be expressed by

\[
i_{pa} = i/2 + i_f + I_{dc}; \quad i_{na} = -i/2 + i_f + I_{dc}
\]

(11)

where \(I_{dc}\) is the DC component in arm currents which is responsible for transferring real active power from the supply to the load. \(i_{2f}\) is the second-order harmonic usually present in any single-phase converters and \(i_L\) is the AC load current component. In the following analysis, the value of the second-order harmonic is not a significant as \(i_{sa}\), so \(i_{2f}\) is not considered and set to zero in (11). From the power balance equation, the maximum value of the load current \(I_{pa}\) can be calculated by

\[
I_a = \frac{2EI_L}{V_{dc}\cos\Phi} \sin(\omega t - \Phi)
\]

(12)

where \(\Phi\) is the load displacement angle, \(I_{dc}\) is the DC component in the arm current which can be calculated as a function of the average value of the qZS-inductor current by

\[
I_{dc} = \frac{1}{1 - D_{sh}} I_L
\]

(13)

Substituting \( (12) \) and \( (13) \) into \( (11) \), and equating the resultant equation by \(I_L\), \(\theta_a\), and \(\theta_b\) can be calculated by

\[
\theta_a = \frac{\sin^{-1}\left(\frac{D_{sh}}{2(1 - 2D_{sh})}\cos\Phi\right)}{2\pi} + \Phi
\]

\[
\theta_b = \frac{\pi - \sin^{-1}\left(\frac{D_{sh}}{2(1 - 2D_{sh})}\cos\Phi\right)}{2\pi} + \Phi
\]

(14)

The capacitance \(C_{u1}\) can be obtained by

\[
C_{u1} = \frac{L_{pa}\Delta t}{\Delta V_{cu1}}
\]

(15)

According to Fig. 7, \(\Delta\) and \(\Delta V_{cu1}\) can be defined as

\[
\Delta V_{cu1} = k_{V_{cu}}\Delta t = \frac{\theta_a - \theta_b}{2\pi} + \frac{1}{f_o}
\]

(16)

where \(V_{cu}\) is the average value of the qZS capacitor voltage, \(k_{V_{cu}}\) is the ratio between peak-to-peak capacitor voltage \(\Delta V_{cu1}\) and \(V_{cu}\), and \(f_o\) is the output load frequency. The capacitor current \(I_c\) during the interval from \(\theta_a\) to \(\theta_b\) is given by

\[
i_c(t) = \begin{cases} I_L - i_{pa} & \text{non-shoot-throughmode (1 - D_{sh})} \\ -I_L & \text{shoot-through mode D_{sh}} \end{cases}
\]

(17)

The average value of \(i_c(t)\) over a switching period is given by

\[
I_{c-\text{ave}} = -D_{sh}I_L + (1 - D_{sh})(I_L - \bar{i}_{pa}(t))
\]

(18)

Substituting \( (11) \)–\( (13) \) into \( (18) \), and integrating from \(\theta_a\) to \(\theta_b\), the average value of \(i_c\) over the interval from \(\theta_a\) to \(\theta_b\) is given by

\[
I_c = \frac{4(1 - 2D_{sh})\cos(\theta_b - \Phi)}{\cos(\Phi(\theta_b - \theta_a))} I_L
\]

(19)

Substituting \( (7) \) and \( (19) \) into \( (15) \), the minimum required capacitance to provide a \(k_{V_{cu}}\) voltage ripple can be obtained as

\[
C_{u1} \geq \frac{4(1 - 2D_{sh})\cos(\theta_b - \Phi)\rho}{\pi k_{V_{cu}} f_o \cos(\Phi(1 - D_{sh})E)}
\]

(20)

5 Simulation results

To verify the validity of the proposed modulation scheme for the BqZS-MMC, a simulation model is implemented in MATLAB/PLECS for the proposed configuration shown in Fig. 2 with a number of SMs equal to 6. The parameters used in the simulation models are given in Table 2. The simulation study has been carried out using a passive \((R + L)\) load and considering that all system components and switches are ideal.

The optimum qZS-capacitors \((C_{u1}\) and \(C_{u2}\)) were calculated in order to provide the voltage ripple factor \(k_{V}\) of ~10%. Based on the parameters in Table 2, the required value of the qZS capacitor is ~3.15 mF which is calculated by \((20)\).

The converter modulation index \(M\) is set at 1 and the ST modulation index \(M_{sh}\) is set to 0.8 (boost), 0.6 (boost), and 1, (buck) and consequently the ST duty ratio \(D_{sh}\) is equal 0.124, 0.256, and zero, respectively. Figs. 8 and 9 show the upper, lower, and overall DC-link voltage, and their zooming. By lowering \(M_{sh}\) from 0.8 to 0.6, the peak value of the overall DC-link voltage is increased from 4 to 6.2 kV. Also, to check the operation in the buck mode, \(M_{sh}\) is set at 1, where the peak value of the overall DC-link voltage becomes 3 kV that is equal to the DC source voltage \(E\).

The simulation results of the qZS-network capacitor \((V_{cu1}, V_{cu2}, V_{cu2}, V_{cu2})\) and arm capacitor voltages are shown in Fig. 10, and Fig. 11 illustrates their zooming. These capacitors are charged according to the relations given in \((7)\) and \((8)\). The ripple factor \(k_{V}\)
of $V_{cu1}$ and $V_{cu1}$ is ~10% which confirm the validity of the proposed capacitance formula. Load voltage and current are shown in Fig. 12. For the proposed BqZS-MMC, by lowering $M_{sh}$ from 0.8 to 0.6, the peak value of the output voltage fundamental component is increased from 2 to 3.1 kV. However, for traditional MMC, the peak value of the output voltage is limited to the half-value of the supply voltage ($E/2 = 1500$ V). The output current shown in Fig. 12 does not show low-order harmonics, which is a sign that the proposed modulation works as expected.

6 Conclusion

This paper proposed a modulation scheme for a bidirectional qZS MMC topology that is able to achieve buck and boost voltage capabilities. The relation between the modulation index and average ST duty ratio has been derived and verified by simulation at different modulation indices in both the buck and boost modes. An analytical design methodology for calculating the required values of qZS capacitors has been proposed, and the resulting ripples in the simulation match the ripple imposed in the design.
7 References

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