DC-DC buck converter with reduced impact

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Abstract

One of the most constraints in DC-DC converter is the supply bouncing caused by the fast switching of power MOSFET. The purpose of this paper is to present a DC-DC buck converter using slew-rate modulator to increase the slew times of the PWM output instead the conventional output stage in order to minimize the bouncing. It does not constitutes a trivial task. This paper presents preliminary results of supply bouncing simulations made with a Slew-Rate Modulator. These simulation results show a very good agreement with the expected results.

Keywords: Supply bouncing; MOSFET power transistor; Buck converter; Slew-rate modulation; CMOS technology.

1. Introduction

Nowadays, the most important electronic devices that sharing the day-to-day of society, such as cellular phones, tablets and laptops are supplied by batteries and it require a very high autonomy. They have a lot of electronic circuits that should be supplied with different voltage levels, which is created the necessity to have circuitry capable of managing and distributing the voltages necessary for the proper operation of the electronic device [1].

Regarding the current scenario, with respect to the requirements of the new electronic devices, there is a growing need for improving the overall efficiency of a system through the development of these management blocks and power distribution that allow the minimization of losses. This is accomplished using topologies of DC-DC converters and their control schemes, so its integration in CMOS technology brings new challenges [1]. DC-DC
DC-DC converters can be realized as linear, switched-capacitor, and inductive converters that temporarily store the energy transferred between the input source and the load.

DC-DC converters have been developed using increasingly improved methods makes them as a whole life support system, which must exhibit high power efficiency, high performance, together with a contribution significant reduction in area that can reduce overall system cost. In addition to the DC-DC converters allow generate multiple voltage levels from a single power source, they are used to attenuate ripples regardless the change in load current or input voltage [6]. Typically, they use pulse width modulation, PWM, to control one or more transistors (depending on the topology used). The switching of the power MOSFET controlled by the PWM usually causes supply bouncing. This kind of phenomenon will cause noise in remaining circuits. It can be reduced using a slew-rate modulation that allows increasing of slew times [7].

The main objective of this paper is to present a solution to reduce supply bouncing created by the transistor switching of power stage of CMOS inductor-based switch-mode DC–DC converters, based on the slew rate modulation of the signal which attacks the power gates. The slew rate modulator is presented in Section 2, including a timing analysis of the output signal provided by this modulator. The power loss model based in [1], [2], [3] is defined in Section 3. In Section 4 is showed an analysis of the efficiency of the converter versus the design parameters, and circuit simulation results for a 3.3–1.8V, 30mA buck converter working at a switching frequency of 100MHz, designed with the UMC 180nm CMOS technology.

2. Reducing supply bounce in DC-DC converters

The proposed work consists on a study of power electronics switched circuit topologies, followed for the development of a power circuit for the DC-DC buck converter with a technique to minimize the bouncing effect and based in the design methodology for DC-DC converters presented in [2], [3]. The main objective is the study and development of a circuit capable to minimize the supply bouncing caused by the switching of the power transistors. The idea presented by H. Jiao and V. Kursun in [4], [5] related activation and deactivation within blocks of microprocessors, as a way to reduce consumption, can be applied to switched converters. It consists in slew-rate modulation technique divide in three phases. The inclusion of a circuitry in addition to the non-overlap circuit which minimizes this effect, it has very high importance as way to reduce the impact of the introduction of this type of converters in a system on a chip, SoC.

Figure 1. Schematic of the triple-phase slew rate modulator [4].
Figure 1 shows the triple-phase slew rate modulator presented in [4], where it’s possible identify the three transistors $M_1$, $M_5$ and $M_{11}$, which are used for tuning the slew rate of input signal during reactivation events that occur in three distinct phases. These transistors are configured to the cut off in low level of the rising edge of the input signal. When there is a transition from low to $V_{dd}$, the transistor $M_1$ is turned on and the output signal starts to rise till when reach the threshold voltage defined by transistor $M_4$. This corresponds to the phase 1, $PH_1$, showed on the transient analysis illustrated in Figure 2. This simulation was performed for an input signal with period of 20ns.

After that, the $M_1$ is placed to the cut off and the phase 2, $PH_2$, is started with $M_5$ turned on. In this phase, the slew rate of output signal is reduced as it is possible to observe in Figure 2. The delay chain presented in Figure 1 allows defining the time of $PH_2$. The end of delay chain marks the third phase, $PH_3$. In this last phase, the transistor $M_{11}$ is turned on and the slew rate of output signal is raised faster toward $V_{dd}$.

Figure 3. Circuit model of the power stage of a buck DC–DC converter, including parasitic impedances.

3. Power loss model

There are some approaches that show a circuit model developed to analyze the efficiency in function of the frequency [1], [2], [3]. The proposed circuit model for the parasitic impedances of the power stage of buck converter
is presented in Figure 3, and it is based on that works. However, it will be not considered the inclusion of gate drivers as mentioned, with the parasitic resistors and capacitors, because they cannot be used after the slew-rate modulator. This model will be centered just on the study of the dissipated energy due to conduction and switching losses in the power stage.

Assuming the conduction losses in the power stage are proportional to the conduction resistance of power MOSFET, $P_{\text{cond}} \propto R_{\text{on}} \times I_{\text{rms}}^2$, and switching losses are proportional to the intrinsic capacitances, $P_{\text{sw}} \propto C_{\text{int}} \times f_s$, it's possible to create a relationship between the cutback of both type of losses. The conduction losses for the two power MOSFETs ($P_1$ and $N_1$ in Figure 3) can be determined by the follow equations (1) and (2), where $i_{\text{rmsPMOS}}$ and $i_{\text{rmsNMOS}}$ are the effective current that flows through the PMOS and NMOS transistors, respectively, $R_{\text{onPMOS}}$ and $R_{\text{onNMOS}}$ are the PMOS ON-resistance per unit length, and $W_{P1}$ and $W_{N1}$ are the transistors width in μm. $D$ is the duty-cycle, $I$ the output current, and $\Delta i_L$ is the current ripple in the filter inductor.

$$E_{\text{PMOSconduction}} = \frac{R_{\text{onPMOS}}}{W_{P1}} i_{\text{rmsPMOS}}^2, \quad E_{\text{NMOSconduction}} = \frac{R_{\text{onNMOS}}}{W_{N1}} i_{\text{rmsNMOS}}^2$$

where:

$$i_{\text{rmsPMOS}} = \sqrt{D \cdot \left( I^2 + \frac{\Delta i_L^2}{3} \right)}, \quad i_{\text{rmsNMOS}} = \sqrt{(1-D) \cdot \left( I^2 + \frac{\Delta i_L^2}{3} \right)}$$

To get a fundamental understanding of the switching losses of the power stage, it is necessary to analyse the parasitic capacitance disposal resulting from the MOSFET physical process used on the design. The switching dissipated energy for the power transistors $P_1$ and $N_1$, which compose the power stage are given by the equations (3) and (4), where $C_{gb0}$, $C_{gd0}$, $C_{gs0}$ and $C_{db0}$ are the gate-bulk, gate-drain, gate-source overlay and drain-bulk capacitances per unit length, respectively.

$$E_{P1\text{TOTALswitching}} = \left( C_{gb0PMOS} + C_{gd0PMOS} \right) V_I^2 - V_{gp}^2 + 2 C_{gd0PMOS} \left( -V_I V_{gp} + V_I^2 + \frac{V_{gp}^2}{2} \right) + 2 C_{db0PMOS} V_I^2$$

$$E_{N1\text{TOTALswitching}} = \left( C_{gb0NMOS} + C_{gd0NMOS} + C_{ds0NMOS} \right) i_{\text{rmsNMOS}}^2 + \left( C_{gd0NMOS} + C_{db0NMOS} \right) V_I^2$$

The total power losses associated to $P_1$ and $N_1$ represented in Figure 3 are obtained as follows:

$$P_{P1\text{TOTAL}} = \frac{R_{\text{onPMOS}}}{W_{P1}} i_{\text{rmsPMOS}}^2 + W_{P1} E_{P1\text{TOTALswitching}} f_s$$

$$P_{N1\text{TOTAL}} = \frac{R_{\text{onNMOS}}}{W_{N1}} i_{\text{rmsNMOS}}^2 + W_{N1} E_{N1\text{TOTALswitching}} f_s$$

Choosing the transistors widths according to (7) will minimize the power losses (maximize efficiency) in the buck converter through an equilibrium between conduction and switching losses described on the Eqs. (5) and (6), where it’s possible verify relationships between the losses, width for the power transistors and frequency.

$$W_{P1\text{opt}} = \sqrt{\frac{R_{\text{onPMOS}} i_{\text{rmsPMOS}}^2}{f_s E_{P1\text{TOTALswitching}}}}, \quad W_{N1\text{opt}} = \sqrt{\frac{R_{\text{onNMOS}} i_{\text{rmsNMOS}}^2}{f_s E_{N1\text{TOTALswitching}}}}$$
4. Simulated results

Figure 3 shows the circuit diagram of the DC-DC converter. The power circuit consists in a conventional synchronous buck configuration. Due to the focus on bouncing reduction, the prototype is implemented with a basic voltage mode PWM control and dominant pole compensation that generates corrective control signal to maintain the output voltage constant. These signals are modulated with triple-phase slew-rate modulator and it’s applied to the power MOSFET. The output signal generated by slew-rate modulator is illustrated in Figure 2. The buck converter is being designed to be prototyped in a twin-well UMC 0.18um CMOS process. In this implementation, it is assumed that the buck converts 3.3V into 1.8V with 30mA of output current, output voltage ripple ($\Delta V_{out}$) less than 1% of the output voltage, inductor current ripple ($\Delta I_L$) below 50% of output current, and the switching frequency is 100MHz. The filter components are external.

$$L_{min} = \frac{V_{out}}{\Delta I_L \cdot f_s} (1 - D)$$  \hspace{1cm} (8)

$$\Delta V_{out} = \frac{V_{out} \cdot (1 - D)}{8 \cdot L \cdot C \cdot f_s^2}$$  \hspace{1cm} (9)

For the buck DC-DC converter, the required inductor and output capacitor are determined by the equations 8 and 9, respectively, where $V_{out}$ is the output voltage, $C$ is the capacitance value, and $L_{min}$ is the inductor minimum value [1]. The values determined for the filtering capacitor is 1.67nF, and for the filtering inductor is 545nH. With the selected components, it’s possible to calculate the system efficiency.

The dc-dc converter efficiency is in most cases a primary specification for any design target, because it is strongly dependent on the switching frequency, $f_s$. Regarding (3) and (4), it’s verified that the values of $L$ and $C$ required to satisfy the target output voltage and current are reduced if $f_s$ is increased. The converter efficiency is given by the (10), where the $P_{out}$ is the output power and $P_{buck}$ is the power losses.

$$\eta = 100 \times \frac{P_{out}}{P_{out} + P_{buck}}$$  \hspace{1cm} (10)

Using the MATLAB tool and the equations on (7), it was possible generate 3-D graphs that correlate the power transistors width with the switching frequency and duty-cycle. The gate width of the switches P1 and N1 for target specifications are designed to be 660 um and 404 um, respectively, by equating the conduction loss and switching loss of the switches. However, regarding the following 3-D graphs (Figure 4 and Figure 5), it’s observed that the transistors width decrease with the increasing of switching frequency.

![Figure 4. NMOS transistors width.](image1)

![Figure 5. PMOS transistors width.](image2)
By the use of same analysis, in Figure 6 it’s illustrated the buck converter efficiency according to the switching frequency and the duty-cycle. The calculated efficiency is 80.28% for a conversion from 3.3V to 1.8V with 30mA of output current, at a 100MHz switching frequency.

![Figure 6. Buck converter efficiency.](image)

Figure 6 shows the effect of different values of switching frequency on the converter’s power efficiency where it’s possible to see that the capacitive losses dominate at higher switching frequencies.

As can be seen the maximum efficiency is achieved when the frequency is about 5 MHz (more than 95% @ frequency 5 MHz) after this frequency the efficiency is decreased due to higher capacitive losses in the output power stage. From the same figure it’s possible to conclude that the duty cycle variation on the buck converter have low influence on the buck DC-DC converter power efficiency.

An output voltage transient analysis of the buck converter is showed in Figure 7 belongs to the circuit presented in Figure 3, whereas can be seen the voltage drop across the load and the converter output stabilizes for 1.8V at 300ns. However, this value is not final, the work still under progress.

Figure 8 shows the output voltage ripple waveform of DC/DC buck converter circuit under following conditions (using type I compensation network); $V_{in} = 3.3V$, $V_{ref} = 1V$, $L = 545nH$, $C_L = 1.67nF$, $R_{load} = 60\Omega$ and switching frequency $f_s = 100MHz$. The simulated ripple of output voltage is 10mV. This value is less than the theoretical value of 18mV, which is 1% of output voltage. Figure 9 shows the transient response of inductor’s peak-to-peak current ripple ($\Delta i_L$) and the load current which is equal to average of $\Delta i_L$, 30mA.

![Figure 7. Output voltage transient analysis of the buck converter.](image)
In Figure 10 it’s represented the transient response result, validating the supply bouncing reduction from 800mV to 250mV by applying the slew rate modulation technique that corresponds to 65% of supply bouncing reduction, when compared with buck DC-DC converter with a conventional output stage. However, this value is a preliminary result because the work still under progress.

Concerning to the total power delivered to the load is 53.2mW at maximum current, and the power supplied is 71mW, this means that the obtained efficiency is around the 75%.

5. Conclusions

In general, the supply bouncing caused by the fast switching of power MOSFET the converter constitutes a big problem during the design phase. This kind of issue will cause noise in all circuits that composes the DC-DC converter. To capitalise on the full advantage of the high frequency switching and low supply bouncing, a slew rate modulator integrated on the converter control has been proposed and simulation result shows that the proposed
The proposed DC-DC buck converter shows a supply bouncing of 65% even at 100 MHz whereas [7] has only 40% at 500 kHz.

| Reference | [7] | Simulations on this work |
|-----------|-----|--------------------------|
| Switching frequency | 500kHz | 100MHz |
| Input range | 3.3V | 3.3V |
| Output voltage | 1.8V | 1.8V |
| Output current | 700mA | 30mA |
| Supply bouncing reduction | 40% | 65% |
| Efficiency | - | 75% |
| Area | 2.3mm² | - |
| Process | 0.35um | 0.18um |

The focus of this work is the supply bouncing reduction. All results presented on this paper are preliminary. This design work is ongoing.

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