Dual-Sensitivity Mode CMOS Image Sensor for Wide Dynamic Range Using Column Capacitors

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Abstract

A wide dynamic range (WDR) CMOS image sensor (CIS) was developed with a specialized readout architecture for realizing high-sensitivity (HS) and low-sensitivity (LS) reading modes. The proposed pixel is basically a three-transistor (3T) active pixel sensor (APS) structure with an additional transistor. In the developed WDR CIS, only one mode between the HS mode for relatively weak light intensity and the LS mode for the strong light intensity is activated by an external controlling signal, and then the selected signal is read through each column-parallel readout circuit. The LS mode is implemented with the column capacitors and a feedback structure for adjusting column capacitor size. In particular, the feedback circuit makes it possible to change the column node capacitance automatically by using the incident light intensity. As a result, the proposed CIS achieved a wide dynamic range of 94 dB by synthesizing output signals from both modes. The prototype CIS is implemented with 0.18-µm 1-poly 6-metal (1P6M) standard CMOS technology, and the number of effective pixels is 176 (H) × 144 (V).

Keywords: CMOS image sensor, wide dynamic range, dual-sensitivity mode, column capacitor, feedback structure

1. INTRODUCTION

In recent years, CMOS image sensors (CISs) have been implemented in various applications such as digital still cameras, surveillance, and safety systems [1,2]. Wide dynamic range (WDR) CISs are required in the camera market for security systems to capture various scenes ranging from dark to bright conditions without loss of information. To achieve a higher spatial resolution, small size pixel is desired, such smaller pixel leads to a reduction of full well capacity (FWC) [3]. Thus, the dynamic range (DR) of conventional CISs, which are used in mobile applications, has been gradually decreasing. To solve this problem, several techniques have been reported [4-15]. The logarithmic response image sensor achieved a very wide DR of 120 dB [4-6]. However, it suffers from a small output swing, large dark current, and low sensitivity, despite the DR extension. The DR and sensitivity of the CISs have been improved by using a self-adaptive operation with a photodiode and a photogate at low light intensity [7]. However, the output voltage from the both types of active pixel sensor (APS) has a knee point variation in each pixel. Moreover, this type of imager offers a poor image quality at strong light intensity. The self-reset technique has also been used for the extension of the DR [8,9]. In this case, the signal processing circuit is quite complex, because in-pixel memory and a comparator are required. This makes shrinking the pixel's size difficult. Wide dynamic range CIS using lateral overflow integration capacitors (LOIFIC) can capture an extremely high illumination range by combining three different types of integration, which maintain high full well capacity [15]. However, they need an additional capacitor and additional transistors in each pixel.

In this paper, we propose a new type of readout circuit to extend the DR of the CIS. The developed CIS has dual-sensitivity modes, which were designed for high-sensitivity (HS) and low-sensitivity (LS) operation. In particular, the proposed DR extension technique is very effective in the bright light conditions by using large additional column capacitor. In comparison with reference paper [15], the proposed CIS was implemented without any additional fabrication processes, and the DR of the proposed CIS is determined by effect of the readout circuits. Most importantly, the added large column capacitor contributes when capturing image in high light intensity conditions. The size of the column...
capacitance can be controlled by a comparator’s output in the proposed column-parallel readout circuits. As a result, the dual-sensitivity outputs are obtained and synthesized through off-chip signal processing. Therefore, a wide DR is achieved by using the proposed DR extension technique.

The rest of this paper is organized as follows. In Section 2, we describe the architecture and operation of the proposed CIS. Section 3 contains the simulation results, measurement results and discussion. The conclusions are summarized in Section 4.

2. ARCHITECTURE AND OPERATION

2.1 Design of the proposed image sensor

Fig. 1 shows both a block and a schematic diagram of the designed image sensor. It consists of a pixel array, a bypass switch array, a column-parallel readout circuit, and vertical and horizontal shift registers. The proposed pixel was designed with a four-transistor (4T) to implement the dual-sensitivity operation (HS and LS modes). The pixel is composed of a reset transistor (M1), a source follower amplifier (M2), a HS mode selection transistor (M3), a LS mode selection transistor (M4) which is located between the sensing node and the column node, as shown in Fig. 1. In particular, a thick oxide transistor was used for M4 because thick-oxide transistor has a high threshold voltage ($V_T$) characteristic and lower leakage current when the transistor is off [9]. The readout circuit consists of mode selection switches (SW1, SW2), a column node reset transistor (Col_RST), a source follower amplifier, a comparator, column capacitor ($C_L$), a feedback switch (SW3), and a feedback capacitor ($C_F$).

2.2 Operational principle

Fig. 2, Timing diagram for dual-sensitivity operation.

Fig. 3, Simulated output as a function of photocurrent: (a) HS mode, (b) LS mode, and (c) LS mode with feedback operation.

Generally, the DR of CISs is limited by their maximum FWC. To extend the DR, we proposed a dual-sensitivity operation with different FWCs. Fig. 2 shows the timing diagram of the control signals. The HS mode is implemented using M1, M2, and M3 transistors and the bypass switch. The pixel signal is sampled before resetting the sensing node of the pixel. The DR in HS mode is determined by the FWC of the sensing node. The signal charge generated in the PD is integrated at the sensing node under
weak light conditions, as shown in Fig. 3 (a). Fig. 3 shows the simulated output as a function of the photocurrent. Under strong light conditions, the sensor in HS mode could not detect the screen anymore because of the small FWC in this sensing node. On the other hand, the LS mode works with the M1 transistors, M4 transistors and the proposed readout circuit. The photocurrent flows into the column capacitor through the M4 transistor, and the slope of output signal is gradually decreased by increasing the photocurrent as shown in Fig. 3 (b). It is possible to detect strong light conditions using the column capacitor while in LS mode. To reset the column capacitor, the switch SW2 and the column reset pulse (Col_RST) are turned on. If not reset, charge is continuously accumulated row by row. During this time, the column capacitor is set to the external voltage Col_REF. Then, the column reset pulse is turned off before M4 is turned on. Because the charge is integrated by using a large FWC value, the sensor could capture in very bright light conditions. However, a large FWC value results in decreased sensitivity that makes it difficult to obtain signals in weak light conditions. The trade-off between DR and sensitivity can be adjusted by obtaining both results.

2.3 Feedback operation in the LS mode

In LS mode, the output is obtained under strong light conditions using a column capacitor. Even though the column capacitor has a large FWC, the sensor could be saturated in very bright light conditions. To overcome this problem, we have developed a feedback structure. By using this structure, the column node capacitance can be changed to control the reference voltage (V_{CMP}). During the integration, the output is compared using a comparator. When the output is lower than the reference voltage, the comparator output, which is the input of switch SW3, is high and switch SW3 is turned on. Thus, the column node capacitance becomes C_{L} + C_{F}. By using this capacitor, the CIS can capture even under stronger light intensity. Fig. 3(c) shows the output variation when the reference voltage is applied. The output can be simply expressed in the following equation:

\[ V_{out} = \frac{T_{int}}{C_{node}} I_{ph} \quad (1) \]

In this equation, \( I_{ph} \) is the photocurrent, \( T_{int} \) is the integration time and \( C_{node} \) is the node capacitance. The sensor output is determined the node capacitance, which, in turn, is \( C_{sensing node} \), \( C_{L} \), \( C_{L} + C_{F} \), depending on the operation mode. By using the feedback structure, the developed CIS can achieve a wider DR.

3. RESULTS AND DISCUSSIONS

The prototype CIS was fabricated using a 0.18-µm 1-poly 6-metal (1P6M) standard CMOS process for machine vision chips. The layout of the proposed image sensor is shown in Fig. 4. The chip consists of a 176 (H) × 144 (V) (QCIF) pixel array with a pixel size of 5.6 µm² and a fill factor of 34.5 %, a bypass switch array, column-parallel readout circuits, and a horizontal/vertical shift register. Chip size is 1.8 mm × 2.1 mm. In the measurement, this sensor was tested under a 2.8 V power supply at 30 frames per second (fps) and 15 fps. The C_{L} and C_{F} are approximately 350 fF and 240 fF, respectively.

Fig. 5 shows the simulation and experimental results for various reference voltages (V_{ref}) at 30 fps. A series of V_{ref} value ranging from 0 V to 1.5 V with a 0.5 V step were applied. The results obtained from the developed CIS are in good agreement with simulation. The response curves were changed because of the reference voltage levels. When the reference voltage was applied, the slope changed because of changes in capacitance. In the case where V_{ref} is 0.5 V (blue line), the slope is the same as in the case in which the feedback structure had no effect (red line) up until the analog output reached 0.5 V. After that, for analog outputs below 0.5 V, the signals are integrated by both the column capacitor and the feedback capacitor. As can be seen in Fig. 5, the saturation light intensity increases from \( 3 \times 10^{3} \) lux to \( 14 \times 10^{3} \) lux by increasing the reference voltage. From these results, we can conclude that, the developed CIS can operate under a wide light intensity range. Compared with the simulation results, however, the output swing of the CIS slightly decreased around 1.1 V.

![Fig. 4. Chip layout of proposed CIS.](image-url)
Hence, there is a reduction in the operating range when the reference voltage is 1.5 V.

Fig. 6(a) and (b) show the digital and the synthesized outputs at 15 fps, respectively, for various light intensity. The analog output is converted into digital data by an off-chip analog-to-digital converter (ADC) with 8-bit resolution. The digital data was obtained from the average output of 100 acquisitions. The sensor chip measured light intensity from $2 \times 10^{-1}$ lux to $2.3 \times 10^3$ lux in HS mode. Without the feedback operation, the maximum incident light measured in LS mode was around $6.4 \times 10^4$ lux. In contrast, using the feedback operation, the maximum incident light measured increased to $8.6 \times 10^4$ lux. Therefore, the developed CIS can detect light with intensity ranging from $2 \times 10^{-1}$ lux to $8.6 \times 10^4$ lux and achieve a wide DR of 94 dB with a 0.9 LSB (= 7 mV) noise level.
Fig. 7 shows the images captured by the prototype CIS chip at 15 fps under strong light conditions. Fig. 7(a) shows the captured image in HS mode. Most pixels are saturated except for the background and the black board. Fig. 7(b) shows the image captured in LS mode under the same light conditions. The image now shows the text (“Image sensor”) and the shape of the objects, but it shows non-uniformity because of the vertical offset mismatch. Finally, Fig. 7(c) shows the image in WDR mode. The WDR image is obtained by synthesizing output signals from both the HS and LS modes. In order to reduce offset variation, off-chip digital calibration was performed, which is equal to the correlated double sampling (CDS) method. Even though off-chip calibration was implemented, some vertical fixed pattern noise (vFPN) remained due to the offset mismatch caused by the effect of the coupling capacitor and capacitance mismatch. The sensor’s characteristics and performances are summarized in the Table 1.

In this study, the DR of the developed CIS was extended by developing a dual-sensitivity mode and a feedback structure. The proposed CIS can easily control its dynamic range by changing the capacity of column capacitors. In particular, the proposed DR extension technique is very effective for bright light conditions, up to 90klux. As a result, the developed CIS is suitable for scientific applications such as surveillance and safety systems.

### Table 1. Performance summary of the sensor.

| Parameter       | Value                                      |
|-----------------|--------------------------------------------|
| Process technology | CMOS 1-poly 6-metal 0.18μm                   |
| Power supply    | 2.8 V                                      |
| Chip size       | 1.8 mm × 2.1 mm                             |
| Pixel size      | 5.6 μm × 5.6 μm                             |
| Pixel array     | 176 (H) × 144 (V)                          |
| Fill factor     | 34.5 %                                     |
| Frame rate Max. | 30 fps                                     |
| ADC resolution  | 8 bits (off-chip ADC)                       |
| Dark level      | 0.9 LSB (= 2.4 mV)                          |
| Vertical FPN    | 1.07 % (After calibration in LS mode)       |
| Dynamic range   | 94 dB (synthesized at Vref = 1.5 V)         |

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REFERENCES

[1] M. Bigas, E. Cabruja, J. Forest, and J. Salvi, “Review of CMOS image sensors,” *Microelectron. J.*, Vol. 37, No.2, pp.433-451, 2006.
[2] E. Raphael, R. Kiefer, P. Reisman, and G. Hayon, “Development of a camera-based forward collision alert system,” *SAE International Journal of Passenger Cars*, Vol. 4, No. 1, pp.467-478, 2011.
[3] S. F. Yeh and C. C. Hsieh, “Novel Single-Slope ADC
Design for Full Well Capacity Expansion of CMOS Image Sensor, Sensors Journal, IEEE, Vol. 13, No. 3, pp. 1012-1017, 2013.

[4] H. Amhaz and G. Sicard, “A high output voltage swing logarithmic image sensor designed with on chip FPN reduction,” Conference in Ph.D. Research in Microelectronics and Electronics (PRIME), Vol. 4, pp. 1-4, 2010.

[5] S. Kavadias, B. Dierickx, D. Scheffer, A. Alaerts, D. Uwaeerts, and J. Bogaerts, “A logarithmic response CMOS image sensor with on-chip calibration,” IEEE J. Solid-State Circuits, Vol.35, No.8, pp. 1146-1152, 2000.

[6] M. Loose, K. Meier, and J. Schemmel, “A self-calibrating single-chip CMOS camera with logarithmic response,” IEEE J. Solid-State Circuits, Vol.36, No.4, pp.586-596, 2001.

[7] S. Lee and K. Yang, “High dynamic-range CMOS image sensor cell based on self-adaptive photosensing operation,” IEEE Trans. Electron Devices, Vol.53, No.7, pp.1733-1735, 2006.

[8] D. Park, J. Rhee, and Y. Joo, “A wide dynamic-range CMOS image sensor using self-reset technique,” IEEE Electron Device Lett., Vol.28, No.10, pp.890-892, 2007.

[9] C. Jun, R. Feng, Y. Hui, and X. Meihua, “A CMOS Image Sensor with Self-reset Circuit in Active Pixel,” CISP’09, 2nd international congress on, pp.1-4, 2009.

[10] T. Lule, S. Benthien, H. Keller, F. Mutze, P. Rieve, K. Seibel, M. Sommer, and M. Bohm, “Sensitivity of CMOS based imagers and scaling perspectives,” IEEE Transactions on Electron Devices, Vol.47, No.11, pp.2110-2122, 2000.

[11] S. Lee, S. H. Jo, M. Bae, B. S. Choi, H. Kim, E. Shin, and J. K. Shin, “Dynamic Range Extension of CMOS Image Sensor with Column Capacitor and Feedback Structure,” J. Sensor Sci. & Tech., Vol.24, No.2, pp.131-136, 2015.

[12] B. S. Choi, S. H. Jo, M. Bae, J. Kim, P. Choi, J. K. Shin and Y. Joo, “A Complementary Metal Oxide Semiconductor Image Sensor with Increased Dynamic Range Using Feedback Reset Mechanism,” Sensor Letters, Vol.13, pp.658-662, 2015.

[13] Liu, W.J., Yeh, H.F. and Chen, O.T.C., “A High Dynamic Range CMOS Image Sensor with Locally Adjusting Charge Supply Mechanism,” 48th Midwest Symposium on Circuits and Systems, Vol.1, pp.384-387, 2005.

[14] M. Bae, B.-S. Choi, S.-H. Jo, H. H. Lee, P. Choi, and J.-K. Shin, “A Linear-Logarithmic CMOS Image Sensor With Adjustable Dynamic Range,” IEEE Sensors Journal, Vol. 16, pp. 5222–5226, 2016.

[15] N. Ide et al., “A Wide DR and Linear Response CMOS Image Sensor with Three Photocurrent Integrations in Photodiodes, Lateral Overflow Capacitors, and Column Capacitors,” IEEE Journal of Solid-State Circuits, Vol.43, No.7, pp.1577-1587, 2008.