ABSTRACT
As the complexity of modern processors has increased over the years, developing effective verification strategies to identify bugs prior to manufacturing has become critical. Undiscovered micro-architectural bugs in processors can manifest as severe security vulnerabilities in the form of side channels, functional bugs, etc. Inspired by software fuzzing, a technique commonly used for software testing, multiple recent works use hardware fuzzing for the verification of Register-Transfer Level (RTL) designs. However, these works suffer from several limitations such as lack of support for widely-used Hardware Description Languages (HDLs) and misleading coverage-signals that misidentify “interesting” inputs.

Towards overcoming these shortcomings, we present ProcessorFuzz, a processor fuzzer that guides the fuzzer with a novel CSR-transition coverage metric. ProcessorFuzz monitors the transitions in Control and Status Registers (CSRs) as CSRs are in charge of controlling and holding the state of the processor. Therefore, transitions in CSRs indicate a new processor state, and guiding the fuzzer based on this feedback enables ProcessorFuzz to explore new processor states. ProcessorFuzz is agnostic to the HDL and does not require any instrumentation in the processor design. Thus, it supports a wide range of RTL designs written in different hardware languages.

We evaluated ProcessorFuzz with three real-world open-source processors – Rocket, BOOM, and BlackParrot. ProcessorFuzz triggered a set of ground-truth bugs 1.23× faster (on average) than DIFUZZRTL. Moreover, our experiments exposed 8 new bugs across the three RISC-V cores and one new bug in a reference model. All nine bugs were confirmed by the developers of the corresponding projects.

KEYWORDS
processor, greybox fuzzing, verification, coverage

1 INTRODUCTION
As the complexity of processor designs has continuously grown over the years, verification has become one of the most challenging tasks in processor manufacturing. The state-space of a complex processor is extremely large, while the processor vendors have limited time and resources for verification. An exhaustive verification (i.e., testing each and every scenario) is an unrealistic goal to achieve, and therefore, a high-quality verification methodology is essential to discover bugs before fabrication. A timely, pre-silicon bug discovery can circumvent potentially millions-of-dollars of losses [33]. Otherwise, undiscovered bugs can manifest as severe security vulnerabilities in both proprietary and open-source processors such as transient execution vulnerabilities (e.g., Spectre [40], Foreshadow [74]), x86’s guest privilege escalation bug [77], Intel’s TSX bug [36] that breaks KASLR, Intel’s machine check vulnerability [34] that enables denial-of-service attacks, and Pentium’s FOOF [16] and FDIV bugs [19].

Broadly, the verification techniques can be divided into two categories - static and dynamic. Static verification techniques [7, 12, 55] aim to prove that the implementation is accurate with respect to a specification. Due to the well-known state explosion problem [18] of these techniques, dynamic verification techniques [5, 20, 23, 56, 70, 75] are commonly used as part of the processor verification process. Dynamic verification involves simulating a Design Under Test (DUT) with a test input and analyzing the behavior of the DUT during or after simulation to identify bugs. Recent works [32, 42, 72] demonstrate that Coverage-based Greybox Fuzzing (CGF), a widely-used software testing technique, can be adapted as a dynamic verification technique to identify bugs in a processor design if certain differences between hardware and software are addressed.

Prior works on processor fuzzing mainly focus on addressing two major challenges. First, code coverage metrics used for fuzzing software programs (basic block, branch coverage, etc.) are not well-suited for fuzzing hardware [32, 70]. Second, a bug in a processor design does not result in an observable anomaly (i.e., crash) during testing as opposed to many software programs which
can indicate the presence of bugs by throwing memory violation errors or raising exceptions.

To address the first challenge, researchers have introduced a variety of coverage metrics such as multiplexer toggle coverage, register coverage, etc [32, 42, 44, 54] that are tailored for hardware. In the context of a processor, the processor is effectively a complex Finite State Machine (FSM) that consists of a large number of states. Exploring different states in ‘processor FSM’ is the key to identifying bugs in the processor. Therefore, hardware-specific coverage metrics mainly aim to guide the fuzzer towards different uncovered ‘processor FSM’ states. These metrics take the hardware intrinsic (e.g., wire connections) into account rather than merely the code structure of the hardware. For instance, DIFUZZRTL [32], a state-of-the-art processor fuzzer, introduces register coverage metric where the goal is to monitor value changes in registers that control multiplexer selection signals. The intuition is that a particular value in these registers represents a unique state in the ‘processor FSM’ and guiding the fuzzer based on this feedback explores additional FSM states.

DIFUZZRTL’s register coverage metric improves on prior works [1, 42, 53] in terms of scalability, efficiency, and precision. However, we make a key observation that the register coverage can be a highly misleading metric for a processor fuzzer. Specifically, we find that DIFUZZRTL monitors many datapath registers which have minimal control over the current FSM state of the processor. The coverage increase resulting from the datapath registers does not provide meaningful information related to the current FSM state of the processor. This results in a scenario where inputs that affect datapath register coverage are incorrectly being classified as ‘interesting’ inputs, which in turn leads to wasted fuzzing time.

To address the second challenge, existing processor fuzzers [27, 32, 38, 43] adapt differential testing from the software domain to the hardware domain. Differential testing in software compares outputs of multiple programs that have the same functional behavior and checks for inconsistencies. In the hardware domain, the results of an Register Transfer Level (RTL) simulator are compared with those of an Instruction Set Architecture (ISA) simulator. An RTL simulator is used to simulate the execution of an instruction stream on the detailed microarchitecture implementation of the processor. The ISA simulator is used to simulate the functional behavior of the processor design and used as a reference model. A difference in the execution output of RTL simulation and ISA simulation indicates a potential bug in the processor.

In this work, we present ProcessorFuzz, a processor fuzzer that implements two novel features. First, ProcessorFuzz uses a new coverage metric called CSR-transition coverage to effectively guide processor fuzzing towards exploring unique processor states. Specifically, it monitors transitions in Control and Status Registers (CSRs) that form the core of the architecture specifications. Our intuition is that certain CSRs dictated by ISA readily expose the current ‘processor FSM’ state (e.g., current privilege mode, the event that caused floating mode exception), and thus the transitions in these CSRs signify a new ‘processor FSM’ state.

ProcessorFuzz’s second feature is that it uses ISA simulation to rapidly determine if a test input is interesting. Prior works rely on RTL simulation for the same goal, which is time-consuming. In fact, this problem gets compounded if the coverage guidance is misleading and results in the execution of repetitive test inputs. ISA simulation is significantly faster than RTL simulation\(^1\). Hence, ProcessorFuzz can efficiently eliminate repetitive test inputs and focus on as many qualitatively distinct test input patterns as possible to expose bugs faster. Another benefit of this design feature is that ProcessorFuzz is agnostic to the hardware description language (HDL) used for designing the processor. Unlike prior works [32, 42], ProcessorFuzz does not require any HDL-specific hardware instrumentation because it identifies interesting inputs using ISA simulation. Hence, processors expressed in different HDLs (VHDL, SystemVerilog, etc.) can easily utilize ProcessorFuzz as a verification tool without having to worry about integration issues.

We evaluate ProcessorFuzz using a variety of widely-used open-source RISC-V based processors Rocket Core [3], BOOM [10], and BlackParrot [61]. Here Rocket Core [3] and BOOM [10] have been designed using Chisel HDL, while BlackParrot [61] has been designed using SystemVerilog. In addition, these processors vary in microarchitectural implementations such as their pipeline depths, execution type (i.e., in-order and out-of-order execution), etc. We compare the bug-finding effectiveness of ProcessorFuzz against the state-of-the-art register coverage guided DIFUZZRTL. On average, for the bugs found by DIFUZZRTL, ProcessorFuzz triggers bugs 1.23× faster than DIFUZZRTL. In addition, ProcessorFuzz revealed 8 new bugs in widely-used open-source processors and one new bug in a reference model.

In summary, we make the following contributions:

- We propose ProcessorFuzz, a new processor fuzzing mechanism. ProcessorFuzz uses a novel CSR-transition coverage (CTC) metric, to effectively guide processor fuzzing towards interesting processor states.
- We propose to use the ISA simulator as part of a coverage feedback mechanism to rapidly identify interesting test inputs, thereby accelerating the bug-finding process.
- We demonstrate the practicality of ProcessorFuzz using 3 different open-sourced RISC-V processors and present eight new bugs identified in those three different processor designs and one new bug in a reference model.
- In the spirit of open science and to facilitate reproducibility of our experiments, we will make our source code of ProcessorFuzz publicly available.

2 BACKGROUND AND MOTIVATION

In this section, we first briefly explain coverage-based greybox fuzzing (CGF) for software. Next, we provide a brief background of how CGF is adapted as a hardware fuzzing method (specifically for processor fuzzing).

2.1 Coverage-based Greybox Fuzzing

Fuzzing has gained broad adoption in the software community due to its effectiveness in bug discovery, scalability, and practicality [25, 26, 50]. Fuzzing is the process of repeatedly running a Program Under Test (PUT) with a large number of random inputs to discover bugs in software. One of the widely-used fuzzing variants is CGF which utilizes the coverage feedback collected from

\(^1\)As a reference point, ISA simulation is 79% faster than RTL simulation for an open-source RISC-V based processor (i.e., BOOM [10]).
the PUT at runtime. In each run of the PUT, CGF records coverage (e.g., basic block coverage, edge coverage, etc.) to determine if the input is ‘interesting’, i.e., whether it leads to increased coverage. If so, CGF applies a set of mutations to the ‘interesting’ input to generate new inputs which are then fed to the PUT in the next fuzzing rounds. Here, the intuition is that generating new inputs from coverage increasing ones would cover even more unexplored code. CGF instruments the code of the program (either statically or dynamically) with the necessary book-keeping logic to record coverage during the program execution.

2.2 Adapting CGF for Processor Fuzzing

Recent works [32, 42, 72] show that CGF can be adapted as a dynamic verification method for hardware including processors. In this section, we briefly explain two important aspects when adapting CGF to processor fuzzing.

Hardware Execution.

In the case of CGF for software, the fuzzing target is a software program that can be directly executed on a host machine with a test input after compilation. However, hardware (e.g., a processor) is not directly executable on the host machine. A hardware design is implemented with an RTL abstraction and must be simulated with an RTL simulator to evaluate a test input. RTL describes the hardware design in terms of data transfer between registers and the logical operations between the registers. The RTL design is usually expressed with an HDL (e.g., Verilog, VHDL). The RTL simulator can provide cycle-accurate information regarding the real-time behavior of the RTL design.

Bug Detection. Most software fuzzers focus on bugs that manifest as memory safety violations such as segmentation faults. These types of bugs are relatively easy to detect because they cause an observable anomaly (i.e., crash) in program behavior. However, fuzzing to find semantic bugs (e.g., logic errors) is harder than discovering memory violations because defining semantic violations is a highly domain-specific task. For these types of bugs, researchers proposed differential testing [6, 49, 51, 64]. Differential testing compares the output of multiple programs that have the same functionality and checks for inconsistent behaviors. This approach is used by processor fuzzers [27, 32, 43] as well. In particular, the processor fuzzer provides the same input to both the RTL simulator and the reference model. Here, the reference model is an ISA simulator that mimics the behavior of all the ISA-level operations. The ISA simulator is a software model of the hardware and does not require any low-level microarchitectural details (e.g., the pipeline depth, buffer size). For a given program, it computes the values of architectural registers and memory state after the execution of each instruction. In contrast, RTL simulator is cycle-accurate and realizes the effect of executed instructions in the microarchitectural level such as the available packets in a buffer or branch prediction result of a conditional branch. The hardware fuzzer extracts an execution trace log from both the ISA simulator and the RTL simulator for the same input and cross-checks the traces. Here, the execution trace contains the final memory states and architectural registers. Any mismatch in the traces is considered a potential bug in the processor and is marked for further investigation by the verification engineer.

2.3 DIFUZZRTL’s Register Coverage

DIFUZZRTL [32], the current state-of-the-art hardware fuzzer, uses this CGF approach to identify bugs in processors. DIFUZZRTL proposes a feedback strategy that aims to capture FSM state transitions during RTL simulation. The strategy follows a two-stage approach as depicted in Figure 1. In stage 1, it performs static analysis to identify a small set of registers in each RTL module and instruments the RTL with necessary hardware logic to record register coverage at simulation time. At a high level, DIFUZZRTL monitors a register if its value is directly or indirectly used to control a multiplexer selection signal. DIFUZZRTL creates a circuit graph of the RTL design where nodes and edges of this graph represent circuit elements (e.g., multiplexers, wires, ports, registers) and connections, respectively. Then, it recursively performs a backward data-flow analysis for each multiplexer’s selection signal and identifies any register in the traversed path. In stage 2, DIFUZZRTL monitors value changes in the identified registers during the RTL simulation. For each clock cycle, DIFUZZRTL hashes all the values in the identified registers into a coverage map to represent the current FSM state. If a new hash value is observed, DIFUZZRTL increases register coverage to signify that the current test is interesting for further mutations.

DIFUZZRTL’s register coverage improves prior work [42, 44] in terms of scalability, efficiency, and precision. However, using register coverage metric for hardware fuzzing can be highly misleading. At a high level, we observe that a subset of registers leads to misleading coverage increase, and therefore, misguides the hardware fuzzer. We provide more details using an example (illustrated in Figure 1) from the open-source RISC-V-based Rocket Core [3].

In particular, in the multiplication unit of Rocket Core, there is a 130-bit remainder register in the MulDiv module that indirectly controls 98 mux selection signals. Therefore, DIFUZZRTL identifies this register to monitor during fuzzing. The change in the value of remainder results in an increase in coverage. In Figure 2, we demonstrate the coverage increase resulted from the remainder register during a 24-hour fuzzing session. First, in Figure 2a, we depict the coverage progress of different modules in the Rocket core. Clearly, the MulDiv module (multiplication unit of Rocket core) dominates the module-wise register coverage. 62% of overall register coverage results from the MulDiv module at the end of 24-hours. Figure 2b further shows the contribution of the remainder register to the coverage increase in the MulDiv module. Compared to all other registers in the MulDiv module, remainder register is clearly major factor that causes increase in register coverage. Indeed, our further analysis showed that the multiplication of two different numbers (see code snippet in List 1) increases the register coverage (i.e., explores a new state) even after 2M iterations.

Listing 1: Code snippet for testing multiplication unit.

1 void main() {
2    unsigned int num1, num2, res;
3    for (int i = 0; i < 2000000; i++) {
4        num1 = i; num2 = i + 1;
5        res = num1 * num2;
6    }
7 }

2 DIFUZZRTL applies some optimizations to reduce search space. As one of their optimizations, it is able to track only a subset of bits of a register and therefore, ultimately tracks 98-bit in remainder register.
In this section, we present the design of ProcessorFuzz, a fuzzing mechanism tailored for processors. We first provide a high-level overview of the different stages of ProcessorFuzz. Then, we outline our reasoning for using ISA simulation instead of RTL simulation to evaluate coverage. Finally, we explain the details of our CSR transition coverage metric and how ProcessorFuzz uses this metric to guide the fuzzing procedure.

3 PROCESSORFUZZ

3.1 Design Overview

We illustrate the design overview of ProcessorFuzz in Figure 3. In stage (1), ProcessorFuzz is provided with an empty seed corpus. It populates the seed corpus by generating a set of random test inputs in the form of assembly programs that conforms to the target ISA. Next, ProcessorFuzz chooses a test input from the seed corpus in stage (2) and subsequently applies a set of mutations (such as removing instructions, appending instructions, or replacing instructions) on the chosen input in stage (3). For these three stages, ProcessorFuzz uses the same methods applied by a prior work [32]. In stage (4), ProcessorFuzz runs an ISA simulator with one of the mutated inputs and generates an extended ISA trace log. A typical trace log generated by the ISA simulator contains (for each executed instruction) a program counter, the disassembled instruction, current privilege mode, and a write-back value as detailed in Section 2. The extended ISA trace log additionally includes the value of CSRs for each executed instruction. The Transition Unit (TU) receives the ISA trace log in stage (5). The TU extracts the transitions that occur in the CSRs. Each observed transition is cross-checked against the Transition Map (TM). The TM is initially empty and populated with unique CSR transitions during the fuzzing session. If the observed transition is not present in the TM, it is classified as a unique transition and added to the TM. In case the current test input triggers at least one new transition, the input is deemed interesting and added to the seed corpus for further mutations. If, however, there are no new transitions triggered, the input is discarded. In stage (6), ProcessorFuzz runs the RTL simulation of the target processor with the mutated input only if the input is determined as interesting. The RTL simulation also generates an extended RTL trace log similar to the extended ISA trace log. The extended RTL trace log contains the same information as the extended trace log. The ISA trace log and the RTL trace log are compared in stage (7). Any mismatch between the logs signifies a potential bug that needs to be confirmed by a verification engineer usually by manual inspection.
Figure 3: ProcessorFuzz Design: ProcessorFuzz runs the ISA simulator with an input generated by the mutation engine and outputs an extended ISA trace log that contains CSR values. The transition unit extracts CSR transitions, determines if a transition is new by checking the transition map, and stores new ones in the transition map. ProcessorFuzz runs the RTL simulation only with interesting inputs and creates an RTL trace log to be compared with the ISA log for bug detection.

Figure 4: Extended trace log generated by the ISA simulator. The values (in hexadecimal) of a subset of CSRs in Table 5 in Appendix are included within the square brackets in the given order; mstatus, mcause, scause, medeleg, frm, and fflags. Transitions are color coded; red and blue for mstatus and fflags CSR transitions, respectively.

3.2 Feedback from the ISA Simulation

One design feature of ProcessorFuzz is that it relies on the ISA simulation to determine if a test input is interesting as opposed to prior works that rely on the RTL simulation. Specifically, ProcessorFuzz runs the ISA simulator with each input obtained from the mutation engine and collects necessary feedback (i.e., CSR transitions which we detail in the following subsections) from the simulator. ProcessorFuzz later processes the collected feedback to determine if the input should be ignored or used by the RTL simulator.

We use the ISA simulator to capture the CSR transitions for two main reasons. First, ISA simulators are generally much faster in executing a given program in comparison to executing that program on a processor using the RTL simulation. For instance, we observed that the RISC-V Spike ISA simulator is, on average 79 times faster than the RTL simulation of the RISC-V BOOM processor. This speedup provides a considerable advantage as ProcessorFuzz can then quickly identify if a test input is interesting without performing the slow RTL simulation. Eliminating inputs with similar characteristics help ProcessorFuzz to achieve faster bug discovery times as shown in Section 4. Indeed, ProcessorFuzz discovered all the bugs found by the existing processor fuzzer (i.e., DIFUZZRTL).

Second is the reduced effort needed to instrument the simulator. A simulator needs to be instrumented to generate an extended trace log with the selected CSRs. An ISA simulator can be easily instrumented by extending the already available trace logic with the selected CSRs. The same instrumented ISA simulator can be used to fuzz any processor design as long as it has been designed for the same ISA target. In contrast, instrumenting RTL designs for tracking the coverage metrics requires extensive effort. Moreover, instrumentation in one HDL does not readily translate to other HDLs. Additionally, as shown in Section 4, ProcessorFuzz incurs limited instrumentation overhead during fuzzing (only <1% in ISA simulator) as opposed to prior works [73] that instrument processor RTL and result in higher runtime overheads (e.g., 71% by TheHuzz [73] and 97% by RFUZZ [42]).

3.3 CSR-transition Coverage

3.3.1 Description of the Metric. As described in Section 2.3, DIFUZZRTL’s register coverage technique monitors many datapath registers (e.g., remainder register) to determine the current FSM state, which leads to large state space. Hence, guiding the fuzzing procedure with DIFUZZRTL’s register coverage metric can be highly misleading when fuzzing processors. To test the processor with as many qualitatively distinct input patterns as possible, we propose a novel CSR transition-based coverage metric.

CSRs are system registers in an ISA specification. These registers are used to control (e.g., delegated exceptions) or hold information (e.g., state of the floating-point unit) about the current architectural state of the processor. Our intuition for using CSRs is as follows. A processor is a complex FSM where CSRs have direct control over the current processor state. Architectural state of the processor (held in the register file and status registers) represents the state of a program running in the processor. A value change in a CSR often signifies an architectural state change such as a value change
in a CSR that stores exception code or privilege level. Therefore, ProcessorFuzz aims to realize the current state of the processor by monitoring transitions in CSRs to guide the fuzzer towards interesting processor states.

CSRs are part of both an ISA simulator and the RTL design of a processor. Hence, CSR transitions can be extracted either from the ISA simulation or the RTL simulation. As detailed before, ProcessorFuzz uses the ISA simulator to capture CSR transitions. Specifically, to extract a CSR transition, ProcessorFuzz monitors the CSR values resulting from the execution of the previous and current instructions and checks if they differ. If so, ProcessorFuzz uses the transition to determine if the input is interesting as detailed in the following subsections. Here, we provide a concrete example to illustrate how ProcessorFuzz identifies a CSR transition in the ISA trace log. Consider the extended ISA trace log shown in Figure 4. The CSR value changes after execution of the \texttt{sret} instruction shown in Line 1, which can be seen by comparing the entries in Line 1 and Line 2 of the ‘Privileged’ column. Specifically, we observe a CSR-transition in \texttt{mstatus} CSR from \texttt{0x8000000a00006000} to \texttt{0x8000000a00006020} as highlighted in red in Figure 4. Overall, from Figure 4, we represent the CSR transition caused by \texttt{sret} instruction as $S_0$, \texttt{S}_1) = (8000000a0000600000006020000060000000), where $S_0$ and $S_1$ are defined as the concatenated CSR values before and after the transition, respectively. 

3.3.2 Why Transitions Instead of Values? DIFUZZRTL determines the current processor state based on the register coverage as detailed in Section 2.3. For each newly covered FSM state, DIFUZZRTL’s register coverage only stores the current state of the processor and does not consider the previous state. Unfortunately, this design choice can lead to important test inputs being discarded by the fuzzer and the fuzzer can potentially miss out on the discovery of a bug. We illustrate this in detail below. Figure 5 represents a subset of the abstract states associated with a real-world bug (Bug 2 in Table 2) that we identified in an open-source RISC-V processor.

In the figure, the processor starts out in the N0 state. The bug triggers in the N2 state only if the previous state is N1. It does not trigger when the previous state is N0. During a coverage-guided fuzzing session, if both N1 (through P0 transition) and N2 (through P2 transition) are covered individually, there will not be a coverage increase for the denoted P1 state transition. And so, the unique P1 transition is not particularly driven towards. Thus, the fuzzing session fails to trigger the bug. Contrarily, by monitoring transitions, we can detect P1 as a new transition even though N1 and N2 states are already covered. Overall, we monitor new transitions in CSRs rather than just identifying unique CSR values to improve the sensitivity of the feedback metric. Indeed, our rationale is similar to widely-used software fuzzers [26, 47]’ rationale that monitors edges in a program instead of basic blocks. We provide the details on how ProcessorFuzz extracts CSR transitions in the next subsection.

3.3.3 CSR Selection Criteria. An ISA specification usually specifies a large number of CSRs\footnote{As a reference point, RISC-V ISA defines up to 4096 CSRs}. Monitoring all available CSRs for transitions can mislead the fuzzer (as we show in Section 4) because not all CSRs provide distinctive information regarding the current processor state. As an example, consider \texttt{instret} CSR that holds the total number of retired instructions. Considering this CSR results in a scenario where each committed instruction by the processor results in a CSR transition. Effectively, ProcessorFuzz would identify any test input as interesting since the \texttt{instret} CSR causes a transition after each committed instruction. However, a test would rarely result in a bug because of a change in committed instruction count. To aid ProcessorFuzz in determining qualitatively different inputs, we introduce the following two criteria when selecting the CSRs that ProcessorFuzz monitors transitions. First, we select CSRs that contain status information about the processor (criteria C1). These CSRs are important because they directly reveal the current state of the processor. As an example, we select a CSR that stores the cause for an exception taken by the processor (e.g., \texttt{mstatus}). If a test case results in an exception, ProcessorFuzz analyzes the cause and differentiates it from another test case that has a different exception reason (e.g., misaligned load/store attempt or access faults due to unauthorized privilege mode). Second, we select any CSR that is used to set a certain configuration in the processor (criteria C2). Here, we aim to realize if the processor behaves as expected under different configurations. For instance, the value of \texttt{medeleg} can be changed to determine which traps can be delegated to lower privilege levels (e.g., the load access fault handled in supervisor mode instead of machine mode). This way, ProcessorFuzz aims to realize if processor designs can perform correctly under different configurations (e.g., different exception delegations) for a particular processor status (e.g., an exception). In Table 3 in Appendix, we list all the CSRs in the RISC-V ISA that we used for identifying transitions in the current implementation of ProcessorFuzz based on the aforementioned two criteria C1 and C2. We also provide all the CSRs that we excluded (e.g., \texttt{instret}) along with details why they are not considered as part of ProcessorFuzz’s current design (Table 6 in Appendix).

Apart from these two criteria, CSR selection can be further limited depending on the features supported by the target processor or the desired scope of verification. For example, if the target processor does not support interrupts within the testing framework, any CSRs related to the configuration or status of interrupts can be excluded. Similarly, if we only want to verify the functionality of the floating-point unit in the processor, only floating-point CSRs can be monitored to identify transitions. We quantitatively demonstrate this capability of ProcessorFuzz in Section 4.2.
3.4 Transition Unit

As shown in Figure 3, the TU takes an extended ISA trace log as input and communicates with the TM to output whether the trace log contains any new transitions. We describe the complete workflow of the TU in Figure 6. As a first step, the TU extracts all CSR transitions in the trace log based on the description in Section 3.3. Then, ProcessorFuzz applies a filter to remove unnecessary transitions. Next, the TU groups the transitions to reduce the state space. We describe how the TU filters and groups the transitions in the rest of this subsection.

Filtering Transitions. We note that the number of possible CSR transitions can be large depending on the cumulative width of the selected CSRs. However, not all CSR transitions represent interesting architectural state changes that are relevant for testing processors. For example, a test program running on the target processor can write to a CSR that contains processor status, e.g., mstatus CSR in RISC-V ISA. This could get identified as a new CSR transition. If the write operation is legal, the processor continues the execution of the program and eventually overwrites the CSR with the updated status. Overall, the type of transitions that occur from writes to status CSRs do not affect the architectural state of the processor. Thus, ProcessorFuzz filters out transitions that occur from explicit writes to status CSRs.

Grouping Transitions. ProcessorFuzz provides the flexibility to customize the CSR-transition coverage metric to be suitable for verifying different Architectural Units (AUs) individually. Specifically, ProcessorFuzz allows a designer to group CSR transitions of AUs, thereby considering them as independent events. Grouping transitions improves the exploration of CSR transitions within each group. As a result, the fuzzier is able to generate tests targeted towards individual AUs and verify them thoroughly. This is a useful feature for a verification engineer as AUs in a processor can be individually verified as an initial step of verification. For example, privileged and unprivileged architectures in a RISC-V processor can be verified individually by grouping transitions as shown in Figure 4. Identifying and fixing the bugs in each AU before fuzzing the processor as a whole can reduce the overall verification effort.

Transition Map. ProcessorFuzz maintains a transition map to store CSR-transitions. Each transition is stored in the map as a tuple: \((I_m, S_0, S_1)\) where \(I_m\) is the mnemonic of the instruction whose execution resulted in the CSR transition. \(S_0\) and \(S_1\) are CSR values before and after the transition as defined in subsection 3.3. Revisiting the same example given in subsection 3.3, privileged CSR-transition caused by \texttt{sret} instruction can be represented as \((\texttt{sret}, 8000000a0000060000000000fb1000000, 8000000a0000060200000000fb1000000)\). Similarly, ProcessorFuzz converts the unprivileged CSR-transition in lines 3 and 4 in Figure 4 to \((\texttt{fdiv.s}, 0000, 00003)\).

We include instruction mnemonic in the aforementioned tuple because the same transition can be triggered by different instructions. For example, both floating-point division and floating-point square-root instructions can trigger the same transition in \texttt{fflags} CSR in RISC-V ISA due to invalid operations. Nevertheless, only the invalid operation of floating-point division instruction might contain a bug. Therefore, we tag each transition with the mnemonic of the instruction that triggered it to uniquely identify transitions triggered by different instructions. Only the mnemonic of the instructions is included to ignore repetitive transitions that get triggered by different operands of the same instruction.

Once tuples are created, the map is queried to check whether the detected transition is new or a duplicate. Tuples that are identified to contain new transitions are added to the map while marking the current test input as interesting. The transition map is empty at the beginning of a fuzzing session and maintained throughout the session.

3.5 RTL Simulation and Trace Comparison

If the TU determines that the current input results in a unique CSR transition, ProcessorFuzz launches the RTL simulation and generates the extended RTL trace log. ProcessorFuzz then compares the extended RTL trace log with the extended ISA trace log. Any difference between these logs signifies a potential bug in the processor design and needs to be investigated further by a verification engineer. In case the input does not result in a unique transition, ProcessorFuzz discards the input and proceeds to the next fuzzing iteration.

4 EVALUATION

In this section, we evaluate the effectiveness of ProcessorFuzz using real-world processor designs. First, we provide the details of our evaluation setup. Then, we assess the bug-finding capability of ProcessorFuzz using ground-truth bugs and compare ProcessorFuzz’s performance against DIFUZZRTL. Specifically, we analyze if ProcessorFuzz can expose the same set of bugs reported by DIFUZZRTL in a more efficient way. Finally, we describe the list of new real-world bugs that ProcessorFuzz identified along with the severity of the bugs.

4.1 Evaluation Setup

4.1.1 Implementation Details. ProcessorFuzz has two main implementation steps: generation of an extended trace log using the ISA simulator and building the TU (see Figure 3). For the former, we extended SPIKE [68] open-source ISA simulator to store the values of monitored CSRs (see Table 5 in Appendix) for each executed instruction during the ISA simulation. The instrumentation overhead of SPIKE is 0.4% in terms of lines of C++ code, while the runtime
overhead is 0.15%. The TU is implemented as a Python library. For the RTL simulation of all processors designs, we used Verilator [67], an open-source RTL simulator. We used the same mutation engine (see Figure 3) as provided by DIFUZZRTL’s open-source repository. Using the same engine is important since our goal is to compare two coverage feedback mechanisms (i.e., register coverage and CSR-transition coverage) rather than input generation mechanisms. We separated transitions belonging to $\texttt{f\!r\!m}$ and $\texttt{f\!f\!l\!a\!g}$s to separate floating-point operations from the rest of the CSRs.

4.1.2 Processor Designs. In our evaluation, we use three real-world open-source processors designed using the open-standard RISC-V ISA.

**RISC-V Rocket Core.** Rocket core is an open-source, general-purpose, in-order, RISC-V processor core that can be generated using the Rocket Chip SoC Generator framework [3]. Rocket core is designed in Chisel HDL [4], and is shown to integrate well with custom hardware accelerators. Rocket core has been taped out multiple times [3] and is capable of booting Linux. Essentially, it is well-tested. We used Spike [68] as a reference model to verify the correctness during fuzzing. The commit version of the Rocket core that we used is 148df5d2.

**RISC-V BOOM Core.** BOOM [10] core can also be generated from the same Rocket Chip SoC Generator framework [3] and is also designed in Chisel HDL. BOOM is an out-of-order, superscalar RISC-V processor core and capable of booting Linux. BOOM has also been taped out [11]. We used Spike ISA simulator to verify the correctness during fuzzing. The commit version of the BOOM core that we used is 148df5d2.

**RISC-V BlackParrot Core.** BlackParrot [61] is an open-source 64-bit RISC-V core, designed in the industry-standard SystemVerilog HDL. BlackParrot is an ideal candidate for hosting accelerator fabrics and for hardware research owing to its tiny, modular, and friendly design approach. BlackParrot is silicon-validated and is in active development. We used Dromajo [71] as a reference model to expose the bugs in BlackParrot for the bc3b48b commit version.

4.1.3 Settings. We compared ProcessorFuzz with two different settings of DIFUZZRTL. The first setting is no-cov-difuzzrtl where DIFUZZRTL fuzzing framework is used without any coverage guidance (i.e., as a blackbox fuzzer). For all the cores that we evaluated, we successfully used this setting as a comparison point. The second setting is reg-cov-difuzzrtl where DIFUZZRTL fuzzing framework relies on register coverage as a guidance mechanism. While this setting is applicable to Rocket and BOOM Cores, it is not the case for BlackParrot Core. This is because DIFUZZRTL’s register coverage passes do not support SystemVerilog. They are tailored for FIRRRTL [35], an intermediate representation (IR) used by Chisel HDL, which is used to design Rocket and BOOM cores. We tried to convert SystemVerilog to FIRRRTL using an open-source tool (i.e., Yosys [78]), and apply DIFUZZRTL’s register coverage passes. However, we observed several issues during this conversion due to the limited support for SystemVerilog to FIRRRTL conversion and thus failed to instrument BlackParrot. In our experiments, we used DIFUZZRTL as the sole comparison point since it shows clear benefits over previous processor fuzzing frameworks as well as its open-source nature. Also, for each setting, we reported Time-to-Exposures (TTE) which is defined as the total elapsed time from the starting of the fuzzing session until the bug is exposed.

4.1.4 Infrastructure. All the experiments based on ISA and the RTL simulations were conducted on server nodes with Intel®Xeon® E5-2670 CPUs and CentOS Linux 7 as the operating system. We fuzzed each processor design 10 times for each setting and allocated 48 hours (2 days) of time limit for each fuzzing instance. For each fuzzing instance, we dedicated two cores and 8GB of memory. In total, it took 4320 CPU hours to conduct all the experiments detailed in the following sections.

4.2 Ground-truth Bugs

As discussed by many prior works [39, 48], the bug-finding capability of a fuzzer is the ultimate litmus test for a fuzzer. While there exist several fuzzing benchmarks for software programs [30, 45], this is not the case for processors. Therefore, we relied on a set of bugs (in total six bugs) previously reported by DIFUZZRTL for BOOM processor to evaluate the bug-finding capability of ProcessorFuzz and perform a head-to-head comparison with DIFUZZRTL. Overall, our evaluation aims to demonstrate that ProcessorFuzz can guide the fuzzer efficiently to discover ground-truth bugs thanks to the CSR-transition feedback obtained using the ISA simulation. In summary, ProcessorFuzz was able to discover all the ground truth bugs and achieved lower TTE compared to DIFUZZRTL.

In Table 1, we report the TTE of bugs in seconds for three different settings in 2nd-4th columns; no-cov-difuzzrtl, reg-cov-difuzzrtl, and ProcessorFuzz for the BOOM processor core. We also provide the achieved speedups by ProcessorFuzz over no-cov-difuzzrtl, and reg-cov-difuzzrtl. For ProcessorFuzz, we provide results for three different configurations; selected, fp-csr, and all-csr. These configurations differ in the CSRs that ProcessorFuzz monitors during fuzzing. Specifically, selected configuration of ProcessorFuzz uses the CSRs in Table 5 in Appendix for transition extraction based on the criteria that we detailed in Section 3.3.3. all-csr configuration monitors all implemented CSRs in the BOOM core. Here, by using all-csr configuration, we aim to present that ProcessorFuzz can be effectively guided towards bugs by eliminating certain CSRs that do not assist fuzzing towards exploring bugs (e.g., minstret that repeatedly changes after an instruction retires). Finally, fp-csr configuration uses only the floating-point CSRs (unprivileged CSRs in Table 5 in Appendix). The aim of this experiment is to show that ProcessorFuzz can focus on certain parts of processors by selecting a subset of CSRs (e.g., floating point unit). Overall, ProcessorFuzz selected configuration and DIFUZZRTL discovered five out of six bugs reported in the DIFUZZRTL within the fuzzing time limit in our experiments. Unfortunately, we could not detect #504 with any of the settings. In summary, ProcessorFuzz (selected) achieved, on average, 1.21× (up to 2.1×) and 1.23× (up to 2.32×) speedups over no-cov-difuzzrtl and reg-cov-difuzzrtl, respectively. no-cov-difuzzrtl performed slightly better than reg-cov-difuzzrtl.

We included fp-csr configuration to demonstrate the ProcessorFuzz’s ability to change the scope of verification by changing the CSR selection. fp-csr detected the bugs in the floating-point unit (issues #492, #493 and #503) x2.08 times faster compared to the
selected configuration while showing a slowdown in detecting other bugs.

We also show the effect of CSR selection on TTE of the bugs through all-csr configuration. all-csr configuration failed to detect two of the bugs within the allocated fuzzing time. Moreover, all-csr is significantly slower (i.e., 0.06x on average) than selected in detecting bugs.

To understand the performance of ProcessorFuzz and DIFUZZRTL for different bugs, we further study the relationship among register coverage, CSR-transition coverage, and bug-finding times. Specifically, in Figure 7a, we show the measured register coverage progress for different settings of DIFUZZRTL and ProcessorFuzz. Although ProcessorFuzz covers less number of states (i.e., achieves lower register coverage) during fuzzing, it was still able to discover bugs faster. For instance, ProcessorFuzz triggered the most challenging bug based on the TTE (i.e., #454) after exploring 303K states while no-cov-difuzzrtl and reg-cov-difuzzrtl triggered that bug after exploring 364K and 354K states, respectively. This particular bug shows that higher register state coverage does not necessarily translate to a faster bug discovery. Indeed, an increase in coverage due to value changes in datapath registers can mislead the fuzzers since inputs with similar characteristics (see the multiplicity example in Section 2.3) are repeatedly used by the fuzzers to generate a new set of inputs.

In Figure 7b, we also show the total number of test inputs that lead to a coverage increase, i.e. ‘interesting test inputs’, and the total number of inputs generated by the mutation engine for the two settings of DIFUZZRTL and ProcessorFuzz. For no-cov-difuzzrtl and reg-cov-difuzzrtl, we use the register coverage metric, same as that used in the DIFUZZRTL work, to realize if a test input increases coverage. For ProcessorFuzz, we use the CSR-transition coverage metric to detect inputs that resulted in a coverage increase. The results provide an important takeaway. Although ProcessorFuzz generates significantly more inputs than other approaches, it is very selective when categorizing a test input as an ‘interesting’ input. Consequently, ProcessorFuzz could expose the bugs faster although it used the least number of test inputs for RTL simulation. Note that ProcessorFuzz launched the RTL simulation only with interesting inputs (i.e., curved dotted red line) and discarded any other generated input. Using the fast ISA simulation enabled ProcessorFuzz to quickly eliminate inputs that do not result in a new FSM state and spend more time on inputs that explore new FSM states.

In Figure 8, we show how ProcessorFuzz performs in terms of industry standard RTL coverage metrics (i.e., line, toggle, FSM, and branch coverage) for BOOM core. Here, our goal is to present the effectiveness of ProcessorFuzz based on the widely-used coverage metrics. In particular, we aim to explore how well the CSR-transition coverage metric is able to result in test cases that cover different lines, toggles, FSMs, and branches in the processor RTL. We compare ProcessorFuzz’s overall coverage based on these four metrics against DIFUZZRTL. Line coverage represents the percentage of RTL code lines that got exercised during the simulation. Toggle coverage indicates the percentage of bits in wires and registers that toggled during the simulation. FSM coverage represents the percentage of FSM states reached during the simulation. Branch coverage represents the percentage of different branches that was taken during the simulation against the total branches in the design. In particular, we obtained all the seeds generated by each approach during fuzzing and feed them to the Synopsys VCS tool one by one and reported coverage. Note that Synopsys VCS tool is significantly slower when collecting coverage, and therefore, we could report coverage progress for the first 12 hours of fuzzing although we run VCS tool for a week. The main takeaway from Figure 8 is that, even though ProcessorFuzz uses CSR-transition coverage extracted from ISA simulation, ProcessorFuzz performs as well as DIFUZZRTL in terms of standard RTL coverage metrics and is able to cover different RTL regions based on different metrics.

### 4.3 Newly Discovered Bugs

In Table 2, we document the various new bugs discovered by ProcessorFuzz in the selected processors mentioned earlier and in the ISA simulator used as a reference model. In the following subsections, we describe and highlight the significance of each bug.

#### 4.3.1 Bug Descriptions

**Bug 1.** When multiple floating-point precisions are supported by a floating-point unit in a processor, valid lower precision values are expected to be NaN-boxed (i.e., remaining upper bits set to 1’s). Otherwise, lower precision values are expected to be interpreted as NaNs. BlackParrot does not interpret non-boxed floats as NaNs, which leads to functionally incorrect
Table 1: The speedup achieved by selected ProcessorFuzz configuration over no-cov-difuzzrtl, and reg-cov-difuzzrtl for the ground-truth bugs in the BOOM processor. We also report speedup of fp-csr and all-csr ProcessorFuzz configurations over selected ProcessorFuzz configuration. In the table, we state the maximum allowed runtime of 48 hours (172800 seconds) for bugs that could not be found.

| Issue No | Time (s) | Speedup (over no-cov) | Time (s) | Speedup (over reg-cov) | Time (s) | Speedup (over selected) | Time (s) | Speedup (over selected) |
|----------|----------|-----------------------|----------|-----------------------|----------|------------------------|----------|------------------------|
| #458     | 104.3    | 1.48                  | 54       | 1.93                  | 1.3      | 151324.8               | 0.0      | 172800 NA              |
| #454     | 32883.3  | 0.73                  | 25020    | 1.31                  | 1.81     | 119886.2               | 0.2      | 39523.3 0.63           |
| #492     | 2047.2   | 4258.9                | 1821.2   | 1.12                  | 2.32     | 1221.8                 | 1.49     | 172800 NA              |
| #493     | 585.4    | 494.9                 | 278.7    | 2.1                   | 1.77     | 170.1                  | 1.63     | 526.6 0.52             |
| #503     | 1463.7   | 1011.1                | 2795.9   | 0.52                  | 0.36     | 757.6                  | 3.69     | 62246.8 0.04           |
| #504     | 172800   | 172800                | 172800   | NA                    | NA       | 172800 NA              | NA       | 172800 NA              |
| Geo.     | 3182.9   | 3225.9                | 2636.7   | 1.21                  | 1.23     | 8890.2                 | 0.23     | 43402.2 0.06           |

Table 2: Brief description of bugs discovered by ProcessorFuzz, and their current status, in various processor cores.

| Bug | Core / Simulator | Brief description of the bug | Status |
|-----|----------------|------------------------------|--------|
| 1   | BlackParrot    | Non-boxed single-precision floating point values are not interpreted as NaNs | Confirmed; not fixed |
| 2   | BlackParrot    | Read-after-write dependencies on fcsr. fflags are not satisfied | Fixed |
| 3   | BlackParrot    | When mstatus. FS is not set and the fcsr. fflags is written, FS is unexpectedly updated | Fixed |
| 4   | BlackParrot    | The 2 low-bits of sepc CSR are not write-insensitive | Fixed |
| 5   | BlackParrot    | No exception raised when writing certain read-only CSRs | Fixed |
| 6   | BlackParrot    | Reading zero register, following specific instruction sequences, return unexpected non-zero values | Fixed |
| 7   | BlackParrot    | Unexpected store access-fault on properly aligned, unpaired sc.d instruction. | Reported |
| 8   | Dromajo        | PMP checks are performed, and raise exceptions upon encountering violations, even with no PMP entries set. | Confirmed; not fixed |
| 9   | Rocket & BOOM  | Instruction page fault not raised when accessing non-leaf PTEs with certain unspecified page attributes. | Fixed |
| 10  | BOOM           | mstatus. FS is gratuitously set to dirty. | Confirmed; not fixed |

Figure 8: The progress of industry-standard RTL coverage metrics for ProcessorFuzz and DIFUZZRTL for BOOM core.
the FS field of mstatus CSR. However, BlackParrot wrongly sets the FS field to dirty, instead of keeping it unchanged.

**Bug 4.** The least significant two bits of sepc CSR must be always hardwired to 0 on implementations that only support 32-bit instruction alignment. Any write from software to the least significant two bits of the sepc CSR must be discarded. However, BlackParrot updated the low bits when a test input attempted to modify them. Further analysis showed that this issue exists for mepc CSR as well.

**Bug 5.** Any attempt to modify a read-only register is supposed to trap with an illegal instruction exception. ProcessorFuzz discovered that BlackParrot does not raise an illegal instruction exception if a test input updates a read-only register, specifically mhartid. ProcessorFuzz monitors ncause and scause CSRs that are in charge of exception handling and was, therefore, able to expose this bug.

**Bug 6.** Any write attempt to the zero register (i.e., x0) must be ignored according to the RISC-V ISA. However, in the BlackParrot processor, we detected that the x0 register is read as a non-zero value one of the preceding division instruction writings that writes to x0 is still in the pipeline. Further analysis revealed that this discrepancy is due to bypassing the result of division operation to the following instruction even when the destination register of a division operation is x0. ProcessorFuzz was able to identify this bug because a test input that has this scenario resulted in a CSR transition in fflags due to division by zero.

**Bug 7.** A store-conditional instruction, if properly aligned to the appropriate word boundary, should not raise a store-access fault. However, BlackParrot raises a store access fault when executing an unpaired, but properly aligned sc.d instruction. We reported the issue to the BlackParrot designers and are currently waiting for their response.

**Bug 8.** According to RISC-V privileged specification, the effective privilege mode for implicit page table accesses should be supervisor mode. However, we observed that Dromajo accesses page tables in user mode privilege level when executing user-mode programs. We reported this issue to the BlackParrot designers and are currently waiting for their response.

**Bug 9.** In a multi-level page table implementation, the accessed (A), dirty (D), and user-mode (U) bits of a non-leaf page table entry (PTE) are reserved for future use and should be cleared. If these bits are set in a non-leaf PTE, the processor must raise an instruction page fault when accessing the PTE according to RISC-V ISA. We observed that Rocket and BOOM cores do not raise instruction page fault when software attempts to access a PTE with any of A, D, or U bits set.

**Bug 10.** The FS field in the mstatus CSR in RISC-V ISA is used to check whether save and restore of floating-point registers are required when there is a context switch. ProcessorFuzz detected that BOOM set the FS field to dirty for any write to fcsr register, even when the value of fcsr is zero and unchanged by the write operation. This scenario is not a violation of RISC-V ISA due to the flexibility allowed by the ISA for maintaining FS field. Nevertheless, setting FS field when the floating-point unit state is unchanged degrades the performance as the processor unnecessarily saves and restores floating-point registers.

### 4.3.2 Timing Results
In Table 3, we provide the TTEs for six newly identified and confirmed bugs (Bug 1-6) and one newly identified but currently waiting confirmation bug (Bug 7) in BlackParrot core. We did not include Bug 8-10 since they were easily detected in all the settings that we used in our evaluation. For this evaluation, we were only able to compare ProcessorFuzz with no-cov-difuzzrtl. As detailed in Section 4.1.3, we could not instrument BlackParrot with register coverage since DIFUZZRTL lacks support for SystemVerilog (detailed in Section 4.1.3). ProcessorFuzz does not require any instrumentation on the RTL design, therefore, could successfully guide the fuzzer with CSR-transition coverage to expose bugs. Overall, ProcessorFuzz achieved 1.6× speedup, on average, over no-cov-difuzzrtl. Note that only ProcessorFuzz was able to detect Bug 6 from Table 2. Similar to the experiment that we conducted in the BOOM processor using the ground-truth bugs, all-csr configuration of ProcessorFuzz performed poorly compared to selected configuration (i.e., 0.47× slow-down). Moreover, fp-csr configuration identified floating-point related bugs fairly faster (e.g., Bug 2) compared to other type of bugs (e.g., Bug 4 that focuses on sepc CSR).

### 5 RELATED WORK
We divide the related work into three different categories. First, we present traditional methods in hardware verification such as random instruction generation, coverage-directed test generation, and formal verification. Then, we present fuzzing-based hardware verification approaches and how ProcessorFuzz differs from existing fuzzing works. Finally, we discuss the usage of differential testing in the software domain.

#### 5.1 Traditional Hardware Verification
Random instruction generators [22, 27, 29, 31, 43] have been commonly used in processor verification since they require limited human expertise and are scalable to large RTL designs. These tools produce random assembly programs based on a set of constraints such as the instruction mix, frequencies, etc., to identify functional bugs in processors. The lack of coverage guidance in these tools leads to the generation of the repetitive inputs that test the same processor functionalities, thereby decreasing the chances of finding bugs [32, 42].

A verification engineer can target the uncovered RTL regions by adjusting the constraints that control the random test generator. For instance, if coverage is maximized in the branch prediction unit but not in the load-store unit, the verification engineer can increase the ratio of load and store instructions. However, this method significantly increases engineering effort, and therefore, slows down the verification process. To overcome this problem, researchers proposed several coverage-directed test generation mechanisms [5, 20, 23, 56, 69, 70, 75] that automatically direct the next round of test generation that targets the uncovered parts of RTL. These works use RTL simulators to dynamically monitor the behavior of an RTL design and adjust the test generator constraints towards producing tests inputs that target uncovered RTL regions.

| Bug | Time (s)  | Speedup (over no-cov) | Time (s)  | Speedup (over selected) | Time (s)  | Speedup (over no-cov) | Speedup (over selected) |
|-----|-----------|-----------------------|-----------|-------------------------|-----------|-----------------------|-------------------------|
| 1   | 464.9     | 2.02                  | 430.2     | 1.08                    | 1608.7    | 0.29                  | 0.14                    |
| 2   | 95695.0   | 1.67                  | 100804.9  | 0.95                    | 122076.0  | 0.78                  | 0.47                    |
| 3   | 1520.1    | 1.03                  | 921.8     | 1.65                    | 172800    | 0.01                  | 0.01                    |
| 4   | 583.3     | 1.90                  | 558.8     | 1.05                    | 13560.4   | 0.04                  | 0.02                    |
| 5   | 476.1     | 1.97                  | 239.7     | 1.99                    | 39150.9   | 0.01                  | 0.01                    |
| 6   | 172800    | 1.17                  | 148655.0  | 1.16                    | 172800    | 1.00                  | 0.86                    |
| 7   | 5192.6    | 1.59                  | 172800    | 0.03                    | 172800    | 0.03                  | 0.02                    |
| Geo | 4018.1    | 1.58                  | 5420.9    | 0.74                    | 47404.8   | 0.08                  | 0.05                    |

Unfortunately, these works are generally DUT-specific which hinders their general applicability.

Formal verification methods (e.g., symbolic execution, model checking) are also widely used in hardware verification [7, 12, 55]. These methods use mathematical reasoning to prove that a hardware design conforms to its specification. Unfortunately, formal verification methods have a well-known state explosion problem, and therefore, do not scale well for complex RTL designs such as a processor [18]. Indeed, a prior work [18] clearly presented that many processor bugs cannot be identified with these tools due to the space explosion issues and emphasised the necessity of complementary approaches to existing formal verification tools.

### 5.2 Hardware Fuzzing

Over the past few years, fuzzing has gained traction in RTL verification due to its bug-finding success in the software domain [28]. In Table 4, we provide a high-level overview of all fuzzing-based RTL verification approaches. For each approach, we include the input format, the coverage metric used to guide the fuzzer, and the method to identify bugs.

RFUZZ [42] defines a simple input format (i.e., a series of bits) to increase the portability of hardware fuzzing to a wide range of RTL designs. Unfortunately, this input format is not effective when fuzzing processors since a processor requires instructions defined by an ISA. RFUZZ also proposes a new coverage metric, the multiplexer toggle coverage. RFUZZ monitors all the multiplexers in the RTL design. It retains an input for further mutations if the input toggles a previously uncovered multiplexer selection signal. A follow-up work by Li et al. [44] enhances RFUZZ with symbolic simulation and defines a full multiplexer toggle coverage metric that counts a multiplexer signal as covered for either 0-to-1 or 1-to-0 toggles. Both RFUZZ and Li et al. are highly coupled to Chisel HDL, which limits the applicability of the approach [63]. Additionally, monitoring multiplexers in complex designs introduces excessive performance overhead [32]. ProcessorFuzz is agnostic to HDL and also does not require any instrumentation in the HDL code, which makes it both practical and efficient.

DIFUZZRTL monitors registers that directly or indirectly control multiplexer selection signals. This design choice makes it more efficient than RFUZZ since the total number of bits in the identified registers is significantly less than multiplexers. Moreover, DIFUZZRTL shows that RFUZZ’s coverage metric does not precisely capture the FSM states. To mitigate this issue, DIFUZZRTL monitors value changes in the identified registers for each cycle. Unfortunately, DIFUZZRTL monitors many registers in the datapath as well, thereby misleading the fuzzer as detailed in Section 2.3.

Trippel et al. [72] translate hardware designs to software models and fuzzes those models. This way, available coverage metrics used by software fuzzers (e.g., basic block, edge) can be used for fuzzing hardware as well. However, this method of converting hardware designs to software models introduces additional challenges such as proving the equivalence between hardware design and software model [63].

A recent processor fuzzer, TheHuzz [73], relies on a variety of coverage metrics extracted using industrial-standard tools such as Cadence [8] and ModelSim [65]. TheHuzz proposes an optimization strategy to increase the effectiveness of fuzzing in discovering bugs. Specifically, TheHuzz profiles individual instructions and determines optimum instruction and mutation pairs while generating new sets of inputs. This way, TheHuzz associates individual instructions with relevant mutation strategies and aims to guide fuzzing towards buggy processor states. Unlike DIFUZZRTL or ProcessorFuzz, TheHuzz does not propose a new coverage metric. TheHuzz relies on several coverage metrics used in software testing (i.e., statement, branch, line, expression). As discussed by prior works [32, 70], these metrics are not sufficient metrics to verify a processor. Besides, D-flip flop (DFF) toggle coverage misses certain states as detailed by DIFUZZRTL. Finally, it is not clear how registers that control FSM coverage are identified as the industrial-tools are not open-sourced. Moreover, the runtime overhead of TheHuzz is higher (71%) than ProcessorFuzz due to the instrumentation applied by industrial tools and profiling coverage. We could not quantitatively compare ProcessorFuzz with TheHuzz as TheHuzz is not open sourced.

The common goal of the aforementioned fuzzing works is to maximize coverage of an RTL design, thereby discovering bugs across the entire RTL design. Researchers have also proposed fuzzing frameworks for achieving alternate verification goals. For instance,
Table 4: Existing RTL Fuzzers.

| Input Format       | Coverage Metric     | Evaluated RTL Designs                  | Bug Discovery Method |
|--------------------|---------------------|----------------------------------------|---------------------|
| RFUZZ [42]         | A Series of Bits    | Peripherals,                          | Assertion           |
|                    |                     | RISC-V Processors (Sodor 1-3-5)       |                     |
| Li et. al [44]     | A Series of Bits    | Full Mux Toggle                        | Assertion           |
|                    |                     | Custom RISC-V Processor, OpenCore 1200 |                     |
| DIFUZZRTL [32]     | Assembly            | Register Coverage                      | Golden Model        |
| DirectFuzz [9]     | A Series of Bits    | Mux Toggle                             | Same as RFUZZ       |
| Trippel et. [72]   | Byte Sequence       | Edge Coverage                          | Golden Model        |
| TheHuzz [73]       | Assembly            | Branch, Line, Statement,              | Golden Model        |
|                    |                     | Expression, DFF Toggle, FSM           |                     |
| HYPERFUZZER [54]   | A Series of Bits    | High-Level                             | Custom SoC          |
| Logic Fuzzer [38]  | A Series of Bits,   | N/A                                    | Property Check      |
|                    | Random Data         |                                        |                     |
| ProcessorFuzz (this work) | Assembly    | Control Path Register, ISA-Sim Transition | RISC-V processors (BOOM, BlackParrot, Rocket Chip) | Golden Model |

DirectFuzz [9] adapts the notion of directed greybox fuzzing and applies it to the RTL verification. Contrary to the aforementioned common goal of fuzzing, the goal of DirectFuzz is to cover certain specific RTL regions with a targeted fuzzing approach. Here, the motivation is to dedicate more fuzzing time to the RTL components that need to undergo thorough testing. HYPERFUZZER [54] introduces a new grammar that represents the hardware security properties. During fuzzing, HYPERFUZZER checks if any of the fuzz-generated inputs violates a security property. Defining properties requires human expertise which is error-prone. Logic Fuzzer [38] randomizes control signals and states of a DUT without compromising the functional correctness of the DUT. Logic Fuzzer needs to be provided with fuzzing targets (e.g., congestible points in an RTL design), and therefore requires domain expertise. INTROSPECTRE [24] and Osiris [76] use blackbox fuzzing approach to discover microarchitectural side channels (i.e., Meltdown [46] and Spectre [40]) in processors.

5.3 Differential Testing in Software Domain

Differential testing is commonly used in the software domain to discover inconsistencies (e.g., semantic bugs, side-channels, consensus bugs) across multiple programs with similar functionalities. One use case of differential testing in the software domain is to identify discrepancies between emulators and real hardware. Prior works [49, 59, 64] aim to eliminate the source of discrepancies in emulation environments since adversaries use discrepancies to infer the execution environment and bypass malware analysis. ProcessorFuzz differs from these works in two ways. First, ProcessorFuzz’s test input generation is coverage-guided whereas these works employ blackbox fuzzing. Second, these works aim to identify discrepancies that may or may not necessarily translate to actual bugs. Besides emulators, differential testing has been used to test different types of software including Web application firewalls [2], SSL/TLS libraries [6, 15, 62, 66], compilers [79], cryptocurrency protocols [21, 41, 80], deep learning systems [58, 60], Java Virtual Machines [13, 14], PDF viewers [62], mobile applications [37], file systems [51], and Java programs [57, 58].

6 DISCUSSION AND LIMITATIONS

Other ISAs. In this work, we demonstrated the capability of ProcessorFuzz using the RISC-V ISA. However, CSRs are not only specific to the RISC-V architecture and defined as part of many other ISAs including x86. Therefore, ProcessorFuzz is not limited to the RISC-V-based processors and can be used in processors based on other ISAs.

Unintended RTL Transitions. ProcessorFuzz uses ISA simulation as part of a feedback mechanism since it is faster and agnostic to the HDL. ProcessorFuzz does not use an input for RTL simulation if the input lacks of a unique transition in its ISA simulation trace. One limitation of this design choice is that ProcessorFuzz can potentially miss certain bugs that follow the given scenario. If a test input would result in an unintended transition in RTL simulation but the same test input does not cause any unique transition in ISA simulation, such a test input will be discarded. Hence, the bug will not be identified.

No RTL Coverage. ProcessorFuzz does not collect feedback (i.e., CSR transitions) from the RTL design during fuzzing. However, we can extend its design and collect coverage from the RTL during RTL simulation to further aid fuzzing. Note that ProcessorFuzz is able to discover all bugs found by prior work in its current form without using any feedback from the RTL design during fuzzing.

7 CONCLUSION

This work presents ProcessorFuzz, a processor fuzzer guided by a novel CSR-transition coverage feedback obtained from ISA simulation. ProcessorFuzz demonstrates that monitoring CSR transitions can effectively guide fuzzing towards buggy processor states. Moreover, using ISA simulation instead of RTL simulation can quickly eliminate inputs that result in the same coverage, thereby helping the fuzzer to test as many qualitatively different inputs as possible. Our experimental results discovered eight new bugs in established, real-world, RISC-V processors, and one new bug in a reference model.
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### A SELECTED AND EXCLUDED CSRS

In this section, we provide the reasoning for the CSR selection in the ProcessorFuzz implementation for RISC-V ISA. We used the criteria mentioned in 3.3.3 to select the CSRs. In general, we selected status CSRs under first criteria (C1) and CSRs that change the configuration of the processor under the second criteria (C2). In Table 5, we show the selected CSRs along with the criteria that was used to select them.

We also provide a list of the CSRs that are implemented in the RISC-V cores, but excluded from the selection in Table 6. Exclusion of CSRs is done based on three intuitive reasons. First, we exclude any CSR that holds the same value throughout all tests. For example, we maintain the same physical memory protection (PMP) configuration for all tests. Therefore, we exclude the CSRs that configure PMP (pmpcfg and pmpaddr) because they are not expected to cause CSR transitions. We exclude misa, hartid, mtevc and stvec CSRs with the same reasoning.

Second, we exclude any CSRs that are not supported by the testing infrastructure. For instance, RISC-V ISA vector extension is not supported in our current instruction generator. Intuitively, vector extension CSRs (vstart, vxsat and vxrm) are not expected to cause any transitions when the vector instructions are not present. Hence, we exclude any CSRs from vector extension. Similarly, debug extension CSRs and CSRs related to handling interrupts are excluded.

Third, we exclude CSRs that do not directly represent the architectural state of the processor. These registers contain information to assist designers during analysis of a hardware bug rather than revealing the fundamental issue. For example, hardware performance-monitoring counters (HPCs) provide information for hardware to assist several debugging use cases including performance bottlenecks. Similarly, CSRs that assist in context switching and trap handling (tval, scratch and epc CSRs) are excluded because they similarly do not reveal the origin of a bug. Also, note that we already monitor the trap cause CSRs (cause, scause) and mstatus CSR to capture any changes in the architectural state due to exceptions and context switches.

Four, we exclude CSR that is already a subset of a CSR that we are already monitoring. For example, ssstatus CSR is excluded because it is a subset of mstatus CSR.
Table 5: CSR selection for RISC-V ISA implementation of ProcessorFuzz along with the criteria that was used to select them. Here, C1 and C2 correspond to two criteria that we describe in Section 3.3.3.

| CSR Group | CSR          | Description                                                                 | Criteria |
|-----------|--------------|-----------------------------------------------------------------------------|----------|
| Privileged| mstatus.xIE  | Controls the global interrupt enable bit for privilege x, x = [M, S, U]      | C2       |
|           | mstatus.xPIE | Holds the value of interrupt-enable bit active prior to the trap for privilege mode x | C1       |
|           | mstatus.xPP  | Holds the previous privilege mode active prior to a trap taken to privilege mode x | C1       |
|           | mstatus.XS   | Contains the state of any additional user-mode extensions                    | C1       |
|           | mstatus.FS   | Contains the state of the floating-point unit                                | C1       |
|           | mstatus.MPRV | Controls the privilege mode in which the memory operations are performed      | C2       |
|           | mstatus.SUM  | Controls the permission for accessing user memory from supervisor mode        | C2       |
|           | mstatus.MXR  | Controls the privilege with which loads access virtual memory                | C2       |
|           | mstatus.TYM  | Controls the ability to edit virtual-memory configuration from supervisor mode | C2       |
|           | mstatus.TW   | Controls the privilege modes that wait for interrupt (WFI) is allowed to execute | C2       |
|           | mstatus.TSR  | Provides the ability to trigger a trap when SRET instruction is executed in supervisor mode | C2       |
|           | mstatus.xXL  | Controls the width of an integer register for privilege mode x, x = [S, U]    | C2       |
|           | mstatus.SD   | Indicate the combined state of mstatus.FS and mstatus.XS for context switches | C2       |
|           | mcause       | Contains the trap cause when a trap is taken in to machine mode              | C1       |
|           | scause       | Contains the trap cause when a trap is taken in to supervisor mode           | C1       |
|           | medeleg      | Decides what type of exceptions are delegated to supervisor mode from machine mode | C2       |
|           | mcounteren   | Controls the availability of the hardware performance-monitoring counters for supervisor mode | C2       |
|           | scounteren   | Controls the availability of the hardware performance-monitoring counters for user mode | C2       |
| Unprivileged| frm          | Controls the dynamic rounding mode for floating-point operations            | C2       |
|           | fflags       | Holds the accrued exceptions from the floating-point operations             | C1       |
### Table 6: CSRs not monitored by ProcessorFuzz along with the reason for exclusion.

| Category                  | CSR     | Description                                                                 | Reason for Exclusion                                      |
|---------------------------|---------|-----------------------------------------------------------------------------|------------------------------------------------------------|
| Privileged                | status  | Holds the supervisor mode operating status of the processor                | Subset of mstatus                                         |
|                           | misa    | Reports the CPU capabilities of a hart                                      |                                                            |
|                           | mhartid | Contains the integer ID of the hardware thread running the code            |                                                            |
|                           | mtvec   | Contains the trap handler base address and vector configuration for machine mode |                                                            |
|                           | satp    | Controls supervisor-mode address translation and protection                |                                                            |
|                           | stvec   | Contains the trap handler base address and vector configuration for supervisor mode |                                                            |
| PMP                       | pmpcfg  | Contains the physical memory protection configuration                      |                                                            |
|                           | pmpaddr | Contains the physical memory protection addresses                           |                                                            |
| Interrupt                 | mip     | Reports pending interrupts in machine mode                                 | Not supported by the testing infrastructure                |
|                           | mie     | Control what interrupts are enabled in machine mode                        |                                                            |
|                           | mideleg | Decides what type of interrupts are delegated from machine mode to supervisor mode |                                                            |
|                           | sie     | Reports pending interrupts in supervisor mode                              |                                                            |
|                           | sip     | Control what interrupts are enabled in supervisor mode                     |                                                            |
| Debug Extension           | dcsr    | Contains the configuration and status of debug extension                   |                                                            |
|                           | dpc     | Holds the program counter of the next instruction to be executed before entering debug mode |                                                            |
|                           | dscratch| Optional scratch register that holds temporary values                      |                                                            |
|                           | tselect | Control which trigger is accessible through the other trigger registers     |                                                            |
|                           | tdata1-3| Holds trigger-specific data                                                |                                                            |
| Vector Extension          | vstart  | Holds the index of the first element to be executed by a vector instruction |                                                            |
|                           | vxsat   | Holds the saturation flag for fixed-point operations                       |                                                            |
|                           | vxrm    | Controls the rounding mode used in the vector extension                    |                                                            |
| HPC                       | mcountinhibit | Controls which hardware performance-monitoring counters are allowed to increment | Does not directly reveal the origin of a potential bug |
|                           | cycle   | Holds the elapsed cycle count of the CPU                                   |                                                            |
|                           | instret | Holds the number of retired instruction count                              |                                                            |
|                           | hpmcounter | Performance-monitoring counter of the event selected by hpmevent             |                                                            |
| Privileged (assisting trap handling and context switches) | mtval | Hold the exception-specific information when a trap is taken to machine mode |                                                            |
|                           | mscratch | Holds a pointer to the machine mode context space while the hart executes in lower privilege |                                                            |
|                           | mepc    | Contains the program counter of an instruction that caused an exception in machine mode |                                                            |
|                           | stval   | Hold the exception-specific information when a trap is taken to supervisor mode |                                                            |
|                           | ssscratch | Holds a pointer to the supervisor mode context space while the hart executes in user mode |                                                            |
|                           | sepc    | Contains the program counter of an instruction that caused an exception in supervisor mode |                                                            |