A Feedback Control Method to Maintain the Amplitude of the RF Signal Applied to Ion Traps

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Abstract: For high-fidelity quantum operations in ion traps, it is important to maintain the secular frequency of the trapped ions at a constant value. The radial secular frequency is proportional to the amplitude of the radio frequency (RF) signal applied to ion traps. Owing to the changes in the ambient temperature of a helical resonator and the minute vibration of the optical table, the amplitude can vary. Recently, a method for reducing the fluctuation in the RF signal amplitude, using a commercial universal proportional-plus-integral (PI) controller, has been introduced, which, in turn, reduces the secular frequency drift of the trapped ions. The method improves the capability to maintain the secular frequency at a constant value. However, the structure of the controller is fixed; thus, the control method cannot be changed to suit different experimental conditions, and the different feedback configuration cannot be implemented to increase the resolution. In this paper, we develop a field-programmable gate array (FPGA)-based feedback controller that allows the implementation of various automatic control methods and feedback configurations. In our experiments, the fluctuation in the amplitude of the RF signal was 1.806% using a commercial universal PI controller. The fluctuation was reduced to 0.099% using the developed FPGA-based PI controller, and to 0.102% using the developed FPGA-based lag compensator. By employing the developed FPGA control method, many other automating control methods can be applied to achieve a stable and high-performance control of the secular frequency.

Keywords: helical resonator; feedback controller; FPGA; lag compensator; PI controller

1. Introduction

The development of high-fidelity quantum gates with trapped ions is very important for quantum computing [1–5]. In the realization of ion trap-based quantum computing systems, the motional mode of the trapped ions is applied for quantum computation [6–9]. The frequency of the motional mode must be fixed as the quantum gate fidelity decreases when the frequency drifts. Since the frequency of the motional mode and secular frequency of the trapped ion are directly related, the drift of the secular frequency affects the reliability of the internal state manipulation. The noisy secular frequency excites the motional state and produces heating [10]. In addition, the noisy frequency changes the parameters such as the trap depth and position in the ion shuttling experiment [11,12]. Therefore, the secular frequency must be accurately controlled [13,14]. If the mass of the trapped ion, and the
distance between the trapped ion and the electrodes of the ion trap do not change, the secular frequency $\omega$ can be expressed as follows [13,15–18]:

$$\omega \propto \frac{V}{\Omega},$$  \hspace{1cm} (1)

where $V$ and $\Omega$ denote the amplitude and frequency of the radio frequency (RF) signal applied to the ion trap, respectively. Since the frequency of the RF signal from a signal generator does not drift, the secular frequency of the trapped ion changes only by the amplitude of the RF signal. The amplitude is increased by an RF amplifier and a helical resonator [18], which is vulnerable to the changes in the ambient temperature of the helical resonator and vibration of the optical table. These factors cause a drift in the resonant frequency and eventually change the amplitude of the RF signal. Therefore, the amplitude of the RF signal increased by the helical resonator needs to be maintained at a constant value. The change in the ambient temperature and the vibration of the optical table are less than a few kHz. Resistors, capacitors, and other electrical components may also be slightly affected by these factors. However, those effects are ignored because the bandwidth of the field-programmable gate array (FPGA)-based feedback controller developed in this paper is 133 kHz.

A method for reducing the fluctuation in the amplitude of the RF signal applied to the ion trap, using a commercial universal proportional-plus-integral (PI) controller (LB1005), has been developed [13]. With this method, the control method cannot be changed to suit different experimental conditions, including derivative control or lead–lag compensation. It is also well known that a PI controller can have a long-term drift error. In addition, the feedback configuration cannot be changed to increase the resolution of the controller. The developed method is also unable to increase the bandwidth of the PI controller to more than 1 MHz (LB1005 limited to 1 MHz). We implement the use of a feedback controller that is similar to that developed in the previous work and define it as the baseline method. Subsequently, we compare this method with the field-programmable gate array (FPGA)-based feedback control method under the same conditions. When using the baseline method, the fluctuation in the amplitude of the RF signal is 1.806%. The amplitude is measured by an analog-to-digital converter (ADC). In this paper, we develop a method for reducing the fluctuation in the amplitude of the RF signal using FPGA-based feedback control [19,20]. With this method, the control method can be freely selected, and various feedback configuration for increasing the resolution can be implemented. Furthermore, we design and utilize a PI controller and a lag compensator using Verilog. With the FPGA-based PI controller and lag compensator, the fluctuations in the amplitude of the RF signal are 0.099% and 0.102%, respectively. These values are 94.510% and 94.359% lower, respectively, than that obtained with the baseline method.

2. Experimental Environment

We did not connect the helical resonator to a vacuum chamber equipped with an ion trap. A helical resonator mounted on a vacuum chamber is considerably less vulnerable to the changes in the ambient temperature of the helical resonator and the minute vibration of the optical table compared with the unmounted one. Figure 1 presents the system for the amplification of the RF signal using the helical resonator. We used a 10 pF capacitor instead of a fabricated ion trap. We measured the resonant frequency and resonance width using the helical resonator with the 10 pF capacitor and a voltage divider to find the quality factor of the resonator with the devices [21–23]. The resonant frequency of the helical resonator was 23.342 MHz, and the resonance width was 149 kHz. Therefore, the helical resonator has a quality factor of 156.7. The helical resonator is fastened by an anodized aluminum breadboard and holder, and stainless-steel posts.
Figure 1. An experimental structure amplifying the RF signal applied to ion traps using a helical resonator.

Direct current (DC) voltage, an output of a feedback controller, and an RF signal generated from a signal generator (Tektronix AFG3021C, Beaverton, OR, USA) were applied to a frequency mixer (Mini-Circuits ZX05-1L-S+, New York, NY, USA). The amplitude of the mixed signal was increased 63 times by an RF amplifier (Mini-Circuits ZX60-100VH+, New York, NY, USA). In addition, the peak-to-peak voltage was increased to 312 V through the helical resonator. To measure the amplitude of the RF voltage, we mounted a capacitive voltage divider at the output of the helical resonator. The amplitude of the RF signal was reduced to 1/1000 by the voltage divider. Then, the RF signal was converted by the rectifier to the DC voltage and applied to the feedback controller.

3. FPGA-Based Feedback Control

3.1. Previous Results

It has been shown that the drift of the secular frequency of trapped ions can be reduced using a commercial universal PI controller (LB1005) [13]. The amplitude of the RF signal applied to the ion traps is obtained by mounting a capacitive voltage divider inside a helical resonator. The obtained RF signal was converted to a DC signal by a rectifier. The difference between the DC signal and set-point voltage was used as the error signal of the commercial universal PI controller. Then, the DC voltage, the output of the controller, and the RF signal from the signal generator were applied to the frequency mixer. The amplitude of the mixed signal was increased by the RF amplifier and helical resonator. Using this method, the drift of the secular frequency of the trapped ion was reduced from 0.25% to 0.05% [13].

3.2. Baseline

As the baseline for comparison, we set up a system similar to that developed in a previous study [13], using a commercial universal PI controller (LB1005). Figure 2 presents the block diagram of the system. The output of a digital-to-analog converter (DAC) (Texas Instruments DAC8734, Dallas, TX, USA) was utilized as the set-point voltage. In addition, the helical resonator in the baseline method was not connected to a vacuum chamber. These conditions are different from those of the previous work. The heat capacity of a general vacuum chamber is significantly greater than that of the helical resonator. A substance with a large heat capacity is less sensitive to changes in the ambient temperature compared to a substance with a small heat capacity. Moreover, the substance with large heat capacity is also less sensitive to physical impacts than that with a small heat capacity. Therefore, the helical resonator mounted on a vacuum chamber is less sensitive to the changes in the ambient temperature of the helical resonator and the minute vibration in the optical table than the unmounted one. In this system, the fluctuation in the amplitude of the RF signal...
was 1.806%, which is larger than that in [13]. We will demonstrate in the following sections how a more advanced control architecture can reduce the amplitude fluctuation.

Figure 2. A block diagram of the closed-loop feedback control system for reducing the fluctuation of the amplitude of the RF signal, using a commercial universal proportional-plus-integral (PI) controller.

3.3. FPGA-Based Feedback Controller

To achieve better performance, we developed a control hardware system using an ADC, a DAC, and an FPGA. Figure 3 presents the block diagram of the closed-loop feedback control system for reducing the fluctuation in the amplitude of the RF signal applied to ion traps using this method. The RF signal is converted by the ADC (Texas Instruments ADS8698EVM-PDK, Dallas, TX, USA) to digital data. Then, the closed-loop control input is calculated by the FPGA (Digilent ARTY S7, Pullman, WA, USA). The calculated data are then converted by the DAC (Texas Instruments DAC8734, Dallas, TX, USA) to an analog signal. The FPGA-based system allows changing the control method as well as the feedback configuration. In this paper, we added a voltage adder circuit to the output of the DAC and a subtractor circuit to the input of the ADC, which was very effective in increasing the resolution and hence in regulating the secular frequency. This would not be possible in the commercial servo method.

3.3.1. Finite-State Machine

Figure 4 presents the conceptual diagram of the finite-state machine (FSM) for controlling an ADC, a DAC, and a PI controller (or a lag compensator). The FSM initially starts with WAIT. When we enter the command UPDATE start into an FPGA using the serial communications of a personal computer, the state of the FSM switches from WAIT to UPDATE. Then, we can enter the parameter values, such as the proportional gain and integral gain of a PI controller, the pole and zero of a lag compensator, the sampling period, and the set-point voltage into the FPGA. When we enter the command LOAD start, the FPGA enters the information in the range of the input and the channel to accept the signals into the ADC. When the operation is complete, UPDATE and LOAD are automatically switched to WAIT. When the commands are entered, such as ADC on, Controller on, and DAC on, the state of the FSM switches to the corresponding state. The commands such as ADC off, Controller off, and DAC off return the state to WAIT. In ADC, an analog data entered into the ADC is converted into digital data and stored in the FPGA. In Controller, the output of the feedback controller is calculated to reduce the difference between the
digital data and set-point voltage. In DAC, the calculated data is converted to analog data using the DAC. The output of the DAC changes to a new value every 7.5 μs, and the cycle is repeated. The DAC continues to supply the voltage of the previous cycle until it receives the new value.

![Block diagram of the closed-loop feedback control system](image1)

**Figure 3.** A block diagram of the closed-loop feedback control system for reducing the fluctuation of the amplitude of the RF signal, using the field-programmable gate array (FPGA)-based feedback controller.

![Finite-state machine](image2)

**Figure 4.** A diagram of the finite-state machine of the FPGA-based feedback controller.

3.3.2. Aluminum Enclosure

The magnetic field around the feedback controller can affect the cables connected to the DAC, ADC, FPGA, and printed circuit board (PCB). The devices are mounted inside the aluminum enclosure to shield them from outside electromagnetic fields. We use two linear...
power suppliers to supply power with little noise to the DAC and PCB, including two regulators, a voltage adder, and a voltage subtractor. The resolution of the FPGA-based feedback controller is increased by the voltage subtractor and voltage adder. In the circuits, regulators (STMicroelectronics LM317, Geneva, Switzerland) are used. The op amps (Texas Instruments LM324, Dallas, TX, USA) are used in the circuits, such as the voltage follower, voltage adder, and voltage subtractor.

3.3.3. Design of the Controllers

In Figure 5a, the step response of the unity feedback circuit of a plant is presented. We use a PI controller and lag compensator to implement an FPGA-based closed-loop control. The forms of unity feedback using a PI controller and lag compensator are presented in Figure 5b,c, respectively. To model the helical resonator, which is the plant of the feedback control, we measure the corresponding output signal, thus changing the frequency of the input of the helical resonator. The transfer function $G(s)$ of the model is as follows:

$$
G(s) = \frac{3.117 \times 10^8 s + 7.527 \times 10^{15}}{s^2 + 2.244 \times 10^5 s + 5.373 \times 10^{14}} = \frac{C(s)}{R(s)}, \quad (2)
$$

where $C(s)$ and $R(s)$ denote the output and input of the plant, respectively. The transfer function has two poles, $s = -1.122 \times 10^5 \pm j 2.318 \times 10^7$, and one zero $s = -2.415 \times 10^7$. The overshoot and settling time of the plant was calculated in MATLAB as 135.38% and 34.94 $\mu$s, respectively. By applying the step input to the plant, the steady-state error of the unity feedback can be obtained as follows:

$$
e(\infty) = \lim_{s \to 0} \frac{sR(s)}{1 + G(s)} = \frac{1}{\lim_{s \to 0} \frac{1}{1 + G(s)}} = 0.0666. \quad (3)
$$

![Figure 5. Conceptual diagrams of the unity feedback. (a) Unity feedback without the use of any controller. (b) Unity feedback using a PI controller. (c) Unity feedback using a lag compensator.](image-url)

We designed a PI controller and lag compensator that can reduce the overshoot and maintain the settling time at less than 1 s, which does not have much of an effect on the experiments with the ion traps, while at the same time having the lowest steady-state error.

As previously defined, a PI controller is a proportional-plus-integral controller that feeds an error (proportional) plus the integral of the error (integral) to a plant [24]. It uses a
pure integrator that places the pole of the controller at the origin to reduce the error to zero. Moreover, it can be expressed as follows:

\[ U(s) = \left( K_p + \frac{K_i}{s} \right) E(s), \]  

where \( K_p \), \( K_i \), and \( E(s) \) denote the proportional gain of the controller, integral gain of the controller, and error signal, which is the difference between the set-point voltage and input of an ADC, respectively. Discretization is required to enable the use of the PI controller in Verilog. Using the backward Euler method, we replace \( s \) with \( \frac{1 - z^{-1}}{T} \); the terms of (4) becomes:

\[ U(z) = \left( K_p + \frac{K_i T}{1 - z^{-1}} \right) E(z), \]

where \( T \) denotes the period of the cycle. Equation (4) can be expressed as follows:

\[ U[k] = U[k-1] + K_p E[k] - K_p E[k-1] + E[k] K_i T. \]  

When the PI controller is used, there are no gains to reduce the steady-state error and overshoot together. Further, we found the two gains that reduced the errors the most through trial and error. When the proportional gain and integral gain of the PI controller are \( 2.21 \times 10^{-4} \) and 5.81, respectively, the overshoot and settling time are 135.41% and 34.94 \( \mu s \), respectively, with the least steady-state error.

A lag compensator does not use a pure integrator; it places the pole near the origin [24] and takes the following form:

\[ U(s) = \left( \frac{s + z_c}{s + p_c} \right) E(s), \]  

where \( p_c \) and \( z_c \) denote the pole and zero of the lag compensator, respectively. Again, by applying the backward Euler method for discretization, the following can be obtained:

\[ U[k] = \frac{U[k-1] + (1 + Tz_c)E[k] - E[k-1]}{1 +Tp_c}. \]

\( \left( \frac{s + z_c}{s + p_c} \right) G(s) \) must be greater than 1 to achieve a greater reduction in the steady-state error when a lag compensator is added than when only the plant is used. To reduce the overshoot and maintain the settling time at less than 1 \( s \), with the least steady-state error, we determined the pole and zero. When the pole and zero of the lag compensator are 533 and 293, respectively, no overshoot occurs, and the setting time is 10.2 ms while showing the lowest steady-state error.

4. Experiments and Results

Without the use of any control, the amplitude of the RF signal drifts. In Figure 6, the amplitudes of the RF signals with and without the use of the PI controller for 5 h are presented. When the PI controller is not used, the amplitude of the RF signal drifts; otherwise, it does not drift. This indicates that the FPGA-based controller prevents the secular frequency of trapped ions from drifting. This FPGA-based feedback controller has an error range of approximately 5 mV attributed to the limitations of the resolution of the ADC.
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A lag compensator does not use a pure integrator; it places the pole near the origin \cite{24} and takes the following form:

$$C_s z U_s E_s + \frac{1}{T_p}$$

where $C_p$ and $C_z$ denote the pole and zero of the lag compensator, respectively. Again, by applying the backward Euler method for discretization, the following can be obtained:

$$C_c U_k T_p z E_k E_k U_k - + - = +$$

\(G(s)\) must be greater than 1 to achieve a greater reduction in the steady-state error when a lag compensator is added than when only the plant is used. To reduce the overshoot and maintain the settling time at less than 1 s, with the least steady-state error, we determined the pole and zero. When the pole and zero of the lag compensator are 533 and 293, respectively, no overshoot occurs, and the settling time is 10.2 ms while showing the lowest steady-state error.

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![Figure 6. Results of the amplitude of the RF signal for 18,000 s. (a) The amplitude of the RF signal without the control. The amplitude drifts from 79.50 to 81.34 mV. (b) The amplitude of the RF signal when the FPGA-based PI controller is used. The voltage does not drift. When the FPGA-based feedback controller is used, no overshoot occurs, and the settling time is less than 1 s.](image)

Figure 7 shows fluctuation in the amplitude of the RF voltage with the baseline method and FPGA-based controllers. It represents that the performance of the new method is better than that of the method developed in the previous work. The standard deviations of the amplitude of the RF signal obtained by the ADC are 61.58 $\mu$V with the PI controller and 63.28 $\mu$V with the lag compensator, which are 0.099% and 0.102% of the amplitude, respectively. These results show that there is no drift. If a small drift persists, the lag compensator is more advantageous than the PI controller. Table 1 shows the fluctuation in the amplitude of the RF signal using the three different feedback controllers. This new method can reduce the fluctuation of the 1 MHz secular frequency of the trapped ion to less than 1 kHz. The voltages in Figure 7 and Table 1 are the outputs of the rectifier measured by ADC. When the helical resonator is not mounted on a vacuum chamber, the fluctuation in the amplitude of the RF signal is 1.806% with the use of a commercial universal PI controller, which is much greater than the 0.05% when the helical resonator is mounted on the vacuum chamber \cite{13}. The fluctuation in the amplitude of the RF signal can be reduced more when using the FPGA-based feedback controller with the helical resonator mounted on a vacuum chamber than when employing the baseline method under the same conditions. By using the FPGA-based feedback control, we can also change the control method to suit the experimental conditions. Moreover, researchers can change the gains, set-point voltage, and input and output of a controller using a computer in this system. Remotely changing the conditions of the RF signal applied to the ion trap reduces the possibility of the changes that can be generated by researchers.
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Table 1. The fluctuations in the amplitude of the RF signal using a commercial universal PI controller and the FPGA-based feedback controller.

| Type of data                                      | Commercial Universal PI Controller | FPGA-Based Controller |
|--------------------------------------------------|-----------------------------------|-----------------------|
| Standard deviation ($\mu$V)                      | 1121.7                            | 61.58                 |
| Percentage of the fluctuation in the amplitude of the RF signal (%) | 1.806                            | 0.099                 |

5. Conclusions

In this paper, we developed a method for reducing the fluctuation in the amplitude of the RF signal applied to ion traps using an FPGA-based feedback controller. This controller allows us to freely change the control method and feedback configuration. In particular, the voltage adders and subtractors were very effective in increasing the resolution. When the FPGA-based PI controller and lag compensator were used, the fluctuations in the amplitude of the RF signal were 94.510% and 94.359% lower, respectively, than the fluctuation when the commercial universal PI controller was used. If the helical resonator is mounted on a vacuum chamber, the fluctuation will be further reduced.

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