An Algorithm for Constructing a Smallest Register with Non-Linear Update Generating a Given Binary Sequence

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Abstract—Registers with Non-Linear Update (RNLUs) are a generalization of Non-Linear Feedback Shift Registers (NLFSRs) in which both, feedback and feedforward, connections are allowed and no chain connection between the stages is required. In this paper, a new algorithm for constructing RNLUs generating a given binary sequence is presented. Expected size of RNLUs constructed by the presented algorithm is proved to be \( O(n/\log(n/p)) \), where \( n \) is the sequence length and \( p \) is the degree of parallelization. This is asymptotically smaller than the expected size of RNLUs constructed by previous algorithms and the expected size of LFSRs and NLFSRs generating the same sequence. The presented algorithm can potentially be useful for many applications, including testing, wireless communications, and cryptography.

Index Terms—Binary sequence, LFSR, NLFSR, binary machine, circuit-size complexity, BIST.

1 INTRODUCTION

Binary sequences are important for many areas, including cryptography, wireless communications, and testing.

In cryptography, pseudo-random binary sequences are used in stream cipher-based encryption. A stream cipher produces a keystream by combining a pseudo-random sequence with a message, usually by the bit-wise addition \([1]\). The security of stream ciphers is directly related to statistical properties of pseudo-random sequences. At present, there is no secure method for generating pseudo-random sequences which satisfy the extreme limitations of technologies like RFID. Low-cost RFID tags cannot dedicate more than a few hundreds of gates for security functionality \([2]\). Even the most compact of today’s encryption systems contain over 1000 gates \([3]\). The lack of adequate protection mechanisms gives rise to many security problems and blocks off a variety of potential applications of RFID technology.

In wireless communications, pseudo-random sequences are used for scrambling and spreading of the transmitted signal. Scrambling is performed to give a transmitted signal some useful engineering properties, e.g. to reduce the probability of interference with adjacent channels or to simplify timing recovery at the receiver \([4]\). Spreading increases a bandwidth of the original signal making possible to maintain, or even increase, communication performance when signal power is below the noise floor \([5]\). For both, scrambling and spreading, it is important to select pseudo-random sequences carefully, because their length, bit rate, correlation and other properties determine the capabilities of the resulting systems. Today’s wireless communication systems typically use Linear Feedback Shift Register (LFSR) sequences, or sequences obtained by linearly combining pairs of LFSR sequences, such as Gold codes \([6]\). There are many theoretical results demonstrating the advantages of using nonlinear sequences in wireless communications. For example, complementary sequences can solve the notorious problem of power control in Orthogonal Frequency Division Multiplexing (OFDM) systems by maintaining a tightly bounded peak-to-mean power ratio \([7]\). Popovich \([8]\) has shown that multi-carrier spread spectrum systems using complementary and extended Legendre sequences outperform the best corresponding multi-carrier Code Division Multiple Access (CDMA) system using Gold codes. However, due to the lack of efficient hardware methods for generating nonlinear sequences, their theoretical advantages cannot be utilized at present.

Built-In-Self-Test (BIST) uses the pseudo-random binary vectors usually generated on-chip by a LFSR as test patterns \([9]\). The hardware cost of an LFSR-based BIST is low. However, the test time of BIST may be long due to random-pattern resistant faults. Several methods for coping with these faults have been proposed, including modification of the circuit under test \([10]\), insertion of control and observe points into the circuit \([11]\), modification of the LFSR to generate a sequence with a different distribution of 0s and 1s \([12]\), and generation of top-off test patterns for random-pattern resistant faults using some deterministic algorithm and storing them in a Read-Only Memory (ROM) \([13]\). The latter approach can help detecting not only random-pattern resistant faults, but also delay faults which are not handled efficiently by the pseudo-random patterns. However, the memory required to store the top-off patterns in BIST can exceed 30% of the memory used in a conventional ATPG approach \([14]\). Finding alternative ways of generating top-off patterns is an important open problem.

Any binary sequence can be generated using a Register with Non-Linear Update (RNLU) shown in Figure \([15]\). A \( k \)-stage RNLU consists of \( k \) binary stages, \( k \) updating functions, and a clock. At each clock cycle, the current values of all stages are synchronously updated to the next values computed by the updating functions. RNLUs can be viewed as a more general
type of Non-Linear Feedback Shift Registers (NLFSRs) (see Figure 1b) in which both, feedback and feedforward, connections are allowed and no chain connection between the stages is required. RNLUs are typically smaller and faster than NLFSRs generating the same sequence. For example, consider the 4-stage NLFSR with the updating function

\[ f(x_0, x_1, x_2, x_3) = x_0 \oplus x_3 \oplus x_1 \cdot x_2 \oplus x_2 \cdot x_3, \]

where “\(\oplus\)” is the Boolean exclusive-OR, “\(\cdot\)” is the Boolean AND, and \(x_i\) is the variable representing the value of the stage \(i, i \in \{0, 1, 2, 3\}\). If this NLFSR is initialized to the state \((x_3,x_2,x_1,x_0) = (0001)\), it generates the output sequence

\[(1, 0, 0, 0, 1, 1, 0, 1, 0, 1, 1, 0, 0) \quad (1)\]

with the period 15. The same sequence can be generated by the 4-stage RNU with the updating functions

\[
\begin{align*}
    f_0(x_0, x_3) &= x_0 \oplus x_3 \\
    f_1(x_1, x_2, x_3) &= x_3 \oplus x_1 \cdot x_2 \\
    f_2(x_2) &= x_2 \\
    f_0(x_1) &= x_1.
\end{align*}
\]

We can see that the RNU uses 3 binary operations, while the NLFSR uses 5 binary operations.

While RNLUs can potentially be smaller than NLFSRs, the search space for finding a smallest RNU for a given sequence is considerably larger than the corresponding one for NLFSRs. Algorithms for constructing RNLUs with the minimum number of stages were presented in [15], [16]. However, since, for large \(k\), the size of a circuit implementing a \(k\)-input Boolean function is typically much larger than the size of a single stage of a register, usually these algorithms do not minimize the total size of an RNU.

In this paper, we present an algorithm which minimizes the size of the support set of updating functions, i.e. the number of variables on which the updating functions depend. For most Boolean functions, the size of a circuit computing a function grows exponentially with the number of the variables in their support set [17]. Therefore, by reducing the number of variables of updating functions to the minimum, we can minimize the total size of an RNU. To support this claim, we derive expressions for the expected size of RNLUs constructed by the presented method and previous approaches. Our analysis shows that RNLUs constructed by the presented method are asymptotically smaller. For completeness, we also compare RNLUs to linear and nonlinear feedback shift registers generating the same sequence.

The rest of this paper is organized as follows. Section 2 lists the notation and basic concepts used in the paper. Section 3 discusses the related work. Section 4 gives a general introduction to the presented approach. Section 5 describes the algorithm for constructing RNU. Section 6 compares RNLUs constructed by the presented method to the RNLUs constructed using previous approaches, as well as to linear and nonlinear feedback shift registers. Section 7 presents the experimental results. Section 8 concludes the paper.
2.3 Feedback Shift Registers

A $k$-stage Feedback Shift Register (FSR) can be viewed as a special case of a $k$-stage RNLU satisfying
\[
\begin{align*}
x_0^+ &= x_1 \\
x_1^+ &= x_2 \\
&\vdots \\
x_{k-2}^+ &= x_{k-1} \\
x_{k-1}^+ &= f(x_0, x_1, \ldots, x_{k-1})
\end{align*}
\]
The updating function of the stage $k-1$ is called the feedback function of the FSR.

If all feedback functions of an FSR are linear, then the FSR is called a Linear Feedback Shift Register (LFSR). Otherwise, it is called a Non-Linear Feedback Shift Register (NLFSR).

It is known that the recurrence relation generated by the feedback function of a $k$-stage LFSR has a characteristic polynomial of degree $k$. If this polynomial is primitive, then the LFSR follows a periodic sequence of $2^k - 1$ states which consists of all possible non-zero $k$-bit vectors. This result is very important, because it makes possible the generation of pseudo-random sequences of length $2^k - 1$ with a device of size $O(k)$. No analogous results has been found for the nonlinear case yet.

3 Previous Work

There are many different ways of generating binary sequences. A thorough treatment of this topic is given by Knuth in [21]. In this section, we focus on FSR-based binary sequence generators and their generalizations.

LFSRs are one of the most popular devices for generating pseudo-random binary sequences. They have numerous applications, including error-detection and correction [22], data compression [23], testing [24], and cryptography [25].

The Berlekamp-Massey algorithm can be used to construct a smallest LFSR generating a given binary sequence. It was originally invented by Berlekamp for decoding Bose-Chaudhuri-Hocquenghem (BCH) codes [26]. Massey [27] linked the Berlekamp’s algorithm to LFSR synthesis and simplified it. There were many subsequent extensions and improvements of the algorithm, for example Mandelbaum [28] developed its arithmetic analog, Imamura and Yoshida [29] presented an alternate and easier derivation, Fitzpatrick [30] found a version which is more symmetrical in its treatment of the iterated pairs of polynomials, and Fleischmann [31] modified it to extend the model sequence in both directions around any given data bit. It has also been shown that similar to the Berlekamp-Massey algorithm results can be obtained with the Euclidean algorithm [32] and continued fractions [33].

The Berlekamp-Massey algorithm constructs traditional LFSRs, which generate one output bit per clock cycle. A number of techniques have been developed for constructing LFSRs with the degree of parallelization $p$. Two main approaches are: (1) synthesis of subsequences representing $p$ decimation of some phase shift of the original LFSR sequence [34] and (2) computation of the set of states reachable from any state in $p$ steps. The latter is usually done by computing $p$th power of the connection matrix of the LFSR [25]. LFSRs with a high degree of parallelization are used in applications where high data rate is important, such a Cyclic Redundancy Check (CRC) widely used in data transmission and storage for detecting burst errors [22].

NLFSRs have been much less studied compared to LFSRs [35]. The first algorithm for constructing a smallest NLFSR generating a given binary sequence was presented by Jansen in 1991 [36]. [37]. Alternative algorithms were given by Linardatos et al [38], Rizomiliotis et al [39], and Limniotis et al [40].

Similarly to the LFSR case, an NLFSR can be re-designed to generate $p$ bits of the sequence per clock cycle. This is usually done by duplicating the updating functions of an NLFSR $p$ times, as in [41]–[43]. Such a technique requires that the $p$ left-most stages of the NLFSR are not used as inputs to feedback functions or output functions. More generally, the problem of constructing an NLFSR with the degree of parallelization $p$ can be solved by computing the $p$th power of the transition relation induced by its feedback functions. However, the size of circuits computing the $p$th power of the transition relation may grow substantially larger than a factor of $p$.

An FSR may need up to $n$ stages to generate a binary sequence of length $n$. For example, the smallest LFSR and NLFSR generating the binary sequence
\[
(00 \cdots 01, \underbrace{0 \cdots 0}_{n-1})
\]
have $n$ and $n-1$ stages, respectively [36].

On average, an LFSR needs $n/2$ stages to generate a binary sequence of length $n$ and an NLFSR needs $2\log_2 n$ stages to generate such a sequence [36]. Note that these bounds reflect the size of stages only; they do not take into account the size of circuits computing feedback functions. Since nonlinear feedback function of an NLFSR is typically larger than the linear feedback function of an LFSR, a $k$-stage NLFSR may be considerably larger than a $k$-stage LFSR.

The first algorithm for constructing an RNLU with the minimum number of stages for a given binary sequence was presented in [15]. This algorithm exploits the unique property of RNLUs that any binary $n$-tuple can be the next state of a given current state. The algorithm assigns every 0 of a sequence a unique even integer and every 1 of a sequence a unique odd integer. Integers are assigned in an increasing order starting from 0. For example, if an 8-bit sequence $A = (0,0,1,0,1,1,0,1)$ is given, the sequence of integers $(0,2,1,4,3,5,6,7)$ can be used. This sequence of integers is interpreted as a sequence of states of an RNLU. The largest integer in the sequence of states determines the number of stages. In the example above, $\lfloor \log_2 7 \rfloor = 3$, thus the resulting RNLU has 3 stages.

In [16], the algorithm [15] was extended to RNLUs generating $p$ bits of the output sequence per clock cycle. The main idea is to encode a binary sequence into a $2^p$-ary sequence which can be generated by a smaller RNLU. As an example, suppose that we use the 4-ary encoding $00 = 0, (01) = 1$, $000 = 2, (001) = 3$, $010 = 4, (011) = 5$, $100 = 6, (101) = 7$, $110 = 8, (111) = 9$, and $1000 = 10$. The problem is then reduced to the construction of a 10-stage RNLU.
1, (10) = 2, (11) = 3 to encode the binary sequence \( A \) from the example above, into the quaternary sequence (0,2,3,1). Then, we can construct an RNLU generating the sequence \( A \) 2-bits per clock cycle using a sequence of states (0, 2, 3, 1). Note that \( \lceil \log_2 3 \rceil = 2 \), so the resulting RNLU has one stage less than the RNLU generating one bit per clock cycle in the previous example.

RNLU's have been successfully applied to the storage of cryptographic keys [46] and deterministic test patterns [47]. For example, it was shown in [46] that an RNLU may take less than a quarter of the size of a read-only memory storing the same sequence.

### 4 Intuitive Idea

We can separate each state of a \( k \)-stage RNLU with the degree of parallelization \( p \) into two parts: \( p \) output bits which contain the output sequence and \( k-p \) extra bits which are used for differentiating the states whose output bits are the same. Output bits are defined by the sequence to be generated. For the extra bits, we can use any \( k-p \) bit vector that is not used in another state with the same output bits.

As we mentioned previously, the overall size of an RNLU is typically dominated by the size of circuits computing its updating functions. The size of these circuits greatly depends on the support sets of updating functions. In order to minimize the support sets, we use extra bit vectors which are unique for every specified state. In other words, not only the states with the same output sequence and \( k-p \) extra bits, but also all other specified states are assigned a unique \( (k-p)\)-bit extra bit vector. Such a state encoding allows us to reduce the support sets of updating functions to variables representing extra bits only, as shown in Figure 2.

Suppose we would like to construct an RNLU generating a binary sequence \( A \) of length \( m \times p \) with the degree of parallelization \( p \). In order to distinguish between identical \( p \)-bit vectors in \( A \), we need at least \( \lceil \log_2 m \rceil \) extra bits. Therefore, the number of stages in the resulting RNLU is given by:

\[
k = \lceil \log_2 m \rceil + p.
\]

This number is typically greater than the minimum possible number of stages in an RNLU which can generate \( A \). The minimum number of stages is determined by partitioning \( A \) into \( p \)-bit vectors, computing the decimal representation for each \( p \)-bit vector, and counting the largest number of occurrences among all \( p \)-bit vectors with the same decimal representation, \( N_{max} \). For example, in the 10-bit sequence \( A = (0,1,0,0,0,1,1,0,1) \) the 2-bit vector (0,1) occurs 3 times, so \( N_{max} = 3 \). The minimum number of stages in an RNLU generating \( A \) is given by [16]:

\[
k_{min} = \lceil \log_2 N_{max} \rceil + p.
\]

5 Algorithm

In this section, we present an algorithm for constructing RNLU's which minimizes the support sets of updating functions to \( \lceil \log_2 m \rceil \) variables representing extra bits.

The pseudocode of the algorithm ConstructRNLU\((A,p)\) is shown as Algorithm 1. The input is a binary sequence \( A = (a_0, a_1, \cdots, a_{n-1}) \) and the desired degree of parallelization \( p \). The output is the defining tables of \( p+r \) updating functions of the RNLU generating \( A \) with the degree of parallelization \( p \), where \( r = \lceil \log_2 m \rceil \) and \( m = \lceil n/p \rceil \).

The algorithm begins by selecting an \( r \)-stage extra bits generator \( G \) using the procedure ChooseGenerator\((n,r)\). As we mentioned in the previous section, the size of an RNLU depends on the order of extra bit vectors used for state encoding. In principle, any permutation of \( r \)-bit vectors can be used, however, a good choice of the generator reduces the size of the resulting RNLU. For example, if we use an \( r \)-stage LFSR or a binary counter as generators of extra bit vectors, then the updating functions of extra bits can be computed by a circuit of size \( O(r) \).

The selected generator \( G \) is set to some initial state \( g_0 \in B^r \). For LFSRs, \( g_0 \) must be a non-zero state. For binary counters, \( g_0 \) can be any state. Then, the defining table of updating functions of output bits is constructed as follows. At every step \( i \), \( i \in \{0,1,\cdots, m-1\} \), the input part of the table is assigned to be the current state of the generator \( G \), \( g_i \), and the output part of the table is assigned to be the \( i \)th \( p \)-bit vector of the input sequence \( A \).

All remaining \( 2^r - m \) input assignments are mapped to don’t-care values. This gives us a possibility to specify the functions \( f_0, f_1, \cdots, f_{p-1} \) so that the size of their circuits is minimized.

Since, by construction, the values of functions \( f_0, f_1, \cdots, f_{p-1} \) at step \( i \) correspond to the \( i \)th \( p \)-tuple of \( A \), for \( i \in \{0,1,\cdots, m-1\} \), the resulting RNLU generates \( A \) with the degree of parallelization \( p \).

As an example, let us construct an RNLU which generates the following 40-bit binary sequence with the degree of parallelization 4:
Algorithm 1 ConstructRNLU(A, p) Constructs an RNLU generating a binary sequence \( A = (a_0, a_1, \ldots, a_{n-1}) \) with the degree of parallelization \( p \).

1: \( m = \lceil n/p \rceil \);
2: \( r = \lceil \log_2 m \rceil \);
3: \( G = \text{ChooseGenerator}(m, r) \);
4: Initialize \( G \) to an initial state \( g_0 \in B^r \);
5: for every \( i \) from 0 to \( m-1 \) do
6: for every \( j \) from 0 to \( p-1 \) do
7: \( f_j(g_i) = a_{i+p+j} \);
8: end for
9: \( g_{i+1} = \text{ComputeNextState}(G, g_i) \);
10: end for
11: for every \( i \) from 0 to \( r-1 \) do
12: \( f_{p+i} = \) updating function of the stage \( i \) of \( G \);
13: end for
14: Return \( f_0, f_1, \ldots, f_{p+r-1} \);

\[ A = (1, 0, 0, 1, 0, 0, 1, 0, 0, 0, 1, 0, 1, 0, 1, 1, 0, 1, 0, 1, 0, 0, 1, 0, 1, 0, 1, 1, 0) \]

We need \( r = \lceil \log_2 10 \rceil = 4 \) extra bits to assign to each of the 10 4-bit vector of \( A \) a unique extra bit vector. Suppose that we use the 4-stage LFSR with the primitive generator polynomial \( g(x) = 1 + x + x^4 \) for generating extra bits. If we choose (0001) as the initial state of the LFSR, then extra bit vectors are assigned according to the following sequence of LFSR states:

\[ (1, 8, 4, 2, 9, 12, 6, 11, 5, 10) \]

This gives us the following defining table for the updating functions of output bits:

| \( x_7x_6x_5x_4 \) | \( f_3 \) | \( f_2 \) | \( f_1 \) | \( f_0 \) |
|-------------------|---------|---------|---------|---------|
| 0 0 0 1           | 1 0 0 0 |
| 1 0 0 0           | 0 1 0 0 |
| 0 1 0 0           | 1 1 0 0 |
| 0 0 1 0           | 0 1 0 0 |
| 1 0 0 1           | 0 1 0 1 |
| 1 1 0 0           | 0 1 0 1 |
| 0 1 1 0           | 1 0 0 0 |
| 1 0 1 1           | 0 0 0 1 |
| 0 1 0 1           | 0 1 1 0 |
| 1 0 1 0           | 0 1 1 1 |

These functions can be implemented as follows:

\[ f_3(x_7, x_6, x_5, x_4) = \overline{x}_7(\overline{x}_5 + x_6)(x_4 + x_3 + x_6) \]
\[ f_2(x_7, x_6, x_5, x_4) = (x_7 + (x_5 \oplus x_6))(x_4 + \overline{x}_5 + x_6 + \overline{x}_7) \]
\[ f_1(x_7, x_6, x_5, x_4) = (\overline{x}_4 + \overline{x}_7)(x_6 + x_7)(x_5 \overline{x}_6 + x_4 \overline{x}_3) \]
\[ f_0(x_7, x_6, x_5, x_4) = x_4x_7 + (x_7 \oplus \overline{x}_5 \overline{x}_6) \]

where “+” is the Boolean OR and \( \overline{x} \) denotes the Boolean complement of \( x \).

Algorithm 2 ChooseGenerator\((m, r)\) Chooses an \( r \)-stage generator of extra bits with at least \( m \) states.

1: if \( m < 2^r \) then
2: \( G = \) Any \( r \)-stage LFSR with a primitive generator polynomial of degree \( r \);
3: else
4: \( G = r \)-stage binary counter;
5: end if
6: Return \( G \);

Fig. 3: 8-stage RNLU constructed for the example.

The updating functions of extra bits, \( f_7, f_6, f_5, f_4 \) are defined by the LFSR:

\[ f_7(x_4, x_3) = x_4 \oplus x_3 \]
\[ f_6(x_7) = x_7 \]
\[ f_5(x_6) = x_6 \]
\[ f_4(x_5) = x_5 \]

Figure 3 shows the structure of the resulting RNLU. The block labeled by \( F_{\text{out}} \) computes the updating functions of output bits \( f_3, f_2, f_1, f_0 \).

6 Expected Size Analysis

In this section, we derive expressions for the expected size of RNLU’s constructed using the presented algorithm and the algorithms [15] and [16]. For completeness, we also show results for LFSRs and NLFSRs generating the same sequence.

In 1942, Shannon [17] has proved that there is an (asymptotically) large fraction of Boolean functions of \( k \) variables that remains uncomputable with circuits of size larger than \( 2^k/k \). In 1962, Luponov [48] has shown that, if we allow circuit size to be larger by a small fraction of \( 2^k/k \), namely \( [1 + o(1)]2^k/k \), then we can compute all \( k \)-variable Boolean functions. In both cases, it is assumed that circuits are composed from AND, OR and NOT gates with at most two inputs.

From these two bounds, we can conclude that “most” Boolean function of \( k \) variables require a circuit of size \( \alpha 2^k/k \) to be computed, where \( \alpha \) is a constant such that \( 1 < \alpha < 2 \).

In the analysis below, we assume one storage element counts as \( \beta \) gates. Since the analysis is asymptotic, without the loss of precision we use \( \log_2 n \) instead of \( \lceil \log_2 n \rceil \).

6.1 Degree of Parallelization One

Let \( A \) be a binary sequence of length \( n \) in which every element is selected independently and uniformly at random from \( B \).
Throughout this section, we call such a sequence a random sequence. Suppose that Algorithm 1 is used to construct an RNLU generating A with the degree of parallelization one. Then, the resulting RNLU has:

- one stage for the output bit,
- \( \log_2 n \) stages for extra bits,
- \( \log_2 n \) updating functions of the extra bits,
- one updating function of the output bit.

The updating functions of the extra bits can be computed by a circuit of size \( O(\log_2 n) \). The updating function \( f_0 \) of the output bit is expected to depend on all \( \log_2 n \) state variables of extra bits. This is because the probability that \( f_0 | x_i = 0 = f_0 | x_i = 1 \) for some \( i \in \{1, 2, \ldots, (\log_2 n) - 1\} \) goes to 0 as the sequences length increases. Therefore, \( f_0 \) requires a circuit of size \( \alpha n/\log_2 n \) to be computed. So, the expected size of the RNLU constructed by the presented algorithm is

\[
E[\text{RNLU}(n, 1)] = \beta (1 + \log_2 n) + \alpha n/\log_2 n + O(\log_2 n) = O(n/\log_2 n). \tag{3}
\]

Next, suppose that the algorithm \( \text{Algorithm 15} \) is used to construct an RNLU for the same sequence. This algorithm constructs an RNLU with the minimum number of stages \( k_{min} \) given by (2). For sufficiently large random sequences, this number can be approximated as:

\[
k_{min} \approx 1 + \log_2 (n/2) = \log_2 n s.
\]

In this case, the resulting RNLU has \( k_{min} \) stages and \( k_{min} \) updating functions with the support set of size \( k_{min} \). These functions required \( k_{min} \) circuits of size \( \alpha 2^{k_{min}} / k_{min} \) to be computed, so their expected size is given by:

\[
k_{min} \cdot \alpha 2^{k_{min}} / k_{min} = \alpha 2^{\log_2 n} = \alpha n.
\]

Therefore, the expected size of the RNLU constructed by the algorithm \( \text{Algorithm 15} \) is:

\[
E[\text{RNLU}(n, 1)] = \alpha n + \beta \log_2 n = O(n). \tag{4}
\]

Next, suppose that Berlekamp-Massey algorithm \( \text{Algorithm 27} \) is used to construct an LFSR for the same sequence. Suppose that this LFSR has \( l \) stages. According to \( \text{Algorithm 45} \), for sufficiently large random sequences, \( l \approx n/2 \). The linear feedback function of the LFSR can be computed by a circuit of size \( O(n) \). So, the expected size of the LFSR is

\[
E[\text{LFSR}(n, 1)] = \beta n/2 + O(n) = O(n). \tag{5}
\]

Finally, suppose an \( r \)-stage NLFSR is constructed of the same sequence, e.g. using the algorithm \( \text{Algorithm 38} \). According to \( \text{Algorithm 36} \), for sufficiently large random sequences, \( r \approx 2\log_2 n \). Thus, the feedback function of the NLFSR has the support set of size \( 2\log_2 n \). It requires a circuit of size \( \alpha \cdot 2^{2\log_2 n} / (2\log_2 n) \) to be computed. Therefore, the expected size of the NLFSR is

\[
E[\text{NLFSR}(n, 1)] = 2\beta \log_2 n + \alpha \cdot 2^{2\log_2 n} / (2\log_2 n) = 2\beta \log_2 n + \alpha r^2 / (2\log_2 n) = O(n^2 / \log_2 n). \tag{6}
\]

As we can see from equations \( \text{Algorithm 3, 4, 5, and 6} \), for sufficiently large random sequences, RNLU's with the degree of parallelization one constructed by the presented algorithm are asymptotically smaller than RNLU's constructed by the algorithm \( \text{Algorithm 15} \), LFSRs, and NLFSRs.

### 6.2 Degree of Parallelization \( p \)

In this section, we extend the analysis to the degree of parallelization \( p \).

Let \( A \) be a random binary sequence of length \( n \). Suppose that Algorithm 1 is used to construct an RNLU generating \( A \) with the degree of parallelization \( p \). Let \( m = [n/p] \). Then this RNLU has:

- \( p \) stages for the output bits,
- \( \log_2 m \) stages for extra bits,
- \( \log_2 m \) updating functions of the extra bits,
- \( p \) updating functions of the output bits.

The updating functions of the extra bits can be computed by a circuit of size \( O(\log_2 m) \). Each of the \( p \) updating functions of the output bits is expected to depend on all \( \log_2 m \) state variables of extra bits. This is because, for any \( j \in \{0, 1, \ldots, p - 1\} \), the probability that \( f_j | x_i = 0 = f_j | x_i = 1 \) for some \( i \in \{p, p + 1, \ldots, (p + \log_2 m) - 1\} \) goes to 0 as the sequences length increases. Therefore, the updating functions of output bits require \( p \) circuits of size \( \alpha n/\log_2 m \) to be computed. Thus, the expected size of the RNLU constructed by the presented algorithm is

\[
E[\text{RNLU}(n, p)] = \beta (p + \log_2 m) + p\alpha n/\log_2 m + O(\log_2 m) = O(n/\log_2 m) = O(n/\log_2 (n/p)). \tag{7}
\]

Suppose that the algorithm \( \text{Algorithm 16} \) is used to construct an RNLU for the same sequence. The number of stages \( k_{min} \) is given by \( \text{Algorithm 2} \). Since \( 1 \leq N_{max} \leq m \), we get

\[
p \leq k_{min} \leq p + \log_2 m.
\]

The lower bound is reached when each \( p \)-bit vector occurs in \( A \) exactly once. This is possible only if \( n \leq 2^p \). Therefore

\[
\log_2 n \leq k_{min} \leq p + \log_2 m. \tag{8}
\]

The \( k_{min} \) updating functions require \( k_{min} \) circuits of size \( \alpha 2^{k_{min}} / k_{min} \) to be computed, so their expected size is \( \alpha 2^{k_{min}} \). From \( \text{Algorithm 3} \), we get:

\[
\alpha n \leq \alpha 2^{k_{min}} \leq \alpha n 2^p.
\]

Therefore, the lower bound on expected size of the RNLU constructed by the algorithm \( \text{Algorithm 16} \) is:

\[
E[\text{RNLU}(n, p)] \geq \beta \log_2 n + \alpha n \geq O(n). \tag{9}
\]

An LFSR with the degree of parallelization \( p \) has the same number of stages as the LFSR with the degree of parallelization one, but its feedback function is modified to compute \( p \)th power of the connection matrix. This implies that the expected size of the circuit computing the feedback
function of the LFSR increases \( p \) times. So, the expected size of the LFSR is

\[
E[LFSR(n,p)] = \beta n/2 + O(pn) = O(pn).
\]

Similarly, NLFSRs with the degree of parallelization \( p \) are constructed by modifying its feedback functions to compute \( p \)th power of its transition relation. This may increase in the size of the circuit computing \( p \)th power of its transition relation more than \( p \) times due to multiplication of non-linear terms \([44]\). The expected size of the NLFSR is thus

\[
E[NLFSR(n,p)] \geq 2\beta \log_2 n + \alpha \cdot p \cdot 2^{-2\log_2 n}/(2\log_2 n)
\geq 2\beta \log_2 n + \alpha p n^2/(2\log_2 n)
\geq O(pn^2/\log_2 n).
\]

From equations (7), (9), (10), and (11), we can conclude that, for sufficiently large random sequences, RNLU with the degree of parallelization \( p \) constructed by the presented algorithm are asymptotically smaller than RNLU constructed by the algorithm \([15]\), LFSRs, and NLFSRs.

Note that our analysis does not take into account that two circuits implementing two \( k \)-variable Boolean functions may share some gates, and therefore their cost may be smaller than \( 2\alpha 2^k/k \). However, since the analysis is asymptotic, this factor is not likely to affect the results.

### 7 Experimental Results

To compare the analytical results to the actual size of RNLU, we applied the presented algorithm and algorithms \([15]\), \([16]\), to randomly generated binary sequences of length up to \( 10^8 \) bits.

For all algorithms, circuits for the updating functions were synthesized using the logic synthesis tool ABC \([49]\). The generic library of gates mcnc.genlib was used for technology mapping.

Figures 4a and 4b show the results for the degrees of parallelization 1 and 100, respectively. 2-input AND is used as a unit of gate size. We can see that RNLU constructed by the presented algorithm is considerably smaller than RNLU constructed by the algorithms \([15]\) and \([16]\). The improvement is particularly striking for the degree of parallelization one. For example, for sequences of length \( 10^7 \), RNLU constructed by the algorithm \([15]\) are 6.67 times larger than RNLU constructed by the presented algorithm. For the degree of parallelization 100 and sequences of length \( 10^7 \), RNLU constructed by the algorithm \([16]\) are 65.1\% larger than RNLU constructed by the presented algorithm.

### 8 Conclusion

In this paper, we presented an algorithm for constructing RNLU in which the support set of updating functions is reduced to the minimum. We proved that the expected size of the resulting RNLU is asymptotically smaller than the expected size of RNLU constructed by previous approaches.

The presented method might be useful for applications which require efficient generation of binary sequences, such as testing, wireless communication, and cryptography.

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