Investigation of resistive switching in SiO$_2$ layers with Si nanocrystals

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Abstract. MOS structures with two-layer insulator, SiO$_2$/SiO$_x$, are tested for switching between high and low resistance state. Part of the structures were annealed at 1000 °C for 60 min in N$_2$ in order to form silicon nanocrystals (Si NCs) in a SiO$_x$ matrix. Cross-sectional transmission electron microscopy revealed that after the high temperature annealing phase separation takes place and nanocrystals with size of ~ 4−5 nm are formed. Direct current-voltage measurements showed that bipolar switching occurs only in the annealed c-Si/SiO$_2$/SiO$_x$/Al structures and not in the control samples. A model explaining the resistance change by electric field formation of conductive pathway in the SiO$_x$−Si NCs layer at negative gate voltages and current driven destruction of the conductive filament at positive voltages was verified by high frequency capacitance-voltage ($C$-$V$) measurements. From the $C$-$V$ results the dielectric constant of non-annealed SiO$_x$ films with $x = 1.3$ was calculated to be $\epsilon_{\text{SiO}_x} = 4.6$.

1. Introduction

Continuously increasing interest in efficient, reliable and economic data storage for diverse applications have attracted much research effort in the field. The well-developed flash memory based on floating-gate silicon MOSFET is approaching its physical limit. Among the technologies proposed to develop the next generation of nonvolatile memories resistive random access memories have received significant attention due to their simple structure, high switching speed, low operating voltage and potential scalability beyond 10 nm feature size [1, 2]. These memories are reversibly switched between a high and low resistance state by direct current (DC) voltage or voltage pulses and the resistance changes are used to store information. Though the development of resistive random access memory has achieved remarkable progress in recent years, the understanding of its conduction mechanisms, dynamic processes and stability issues is still limited.

Resistive switching effect has been observed in many oxides including SiO$_x$ [3], which is particularly interesting compared to other oxides because of its complete CMOS compatibility. SiO$_x$ has been studied as switching oxide in various types of electrode-oxide-electrode and metal-oxide-semiconductor (MOS) structures [4, 5]. Poly-Si and different metals have been used as electrodes [6−8]. For SiO$_x$ a switching mechanisms based on voltage-driven formation and modification of silicon nanocrystals (NCs) in the SiO$_x$ matrix, with SiO$_x$ also serving as source for formation of conductive Si pathway has been proposed [6]. Another model is based on formation of filaments on the edges of columns in sputtered SiO$_x$ [8]. In MOS structures having SiO$_x$ with Si NCs as gate insulator formation of conductive pathway of aligned nanocrystals has been observed [5].

In this study we present results for the resistive switching properties of thin SiO$_x$ films deposited on thermally grown SiO$_2$ on n-type Si. The difference in the electron injection properties of the top
(Al/SiOₓ) and bottom (crystalline Si/SiO₂) interfaces favors electric field formation of conductive pathways at negative voltages applied to the top contact and current-driven destruction of the filament at positive voltages.

2. **Experimental details**

Silicon-rich SiOₓ layers with initial composition of \( x = 1.3 \) and thicknesses of 20 and 40 nm were deposited on SiOₓ/crystalline silicon (c-Si) substrates maintained at room temperature. The thermal oxide with thickness of \( \sim 25 \) nm was grown in dry oxygen atmosphere at 1000 °C on (100) n-type c-Si with \( \rho = 4–6 \ \Omega \) cm. The silicon wafers were cleaned chemically prior to oxidation applying a standard procedure for the microelectronics industry. Thermal evaporation of SiO at a vacuum of \( 1 \times 10^{-3} \) Pa was used for the SiOₓ film preparation [9]. The deposition rate and film thickness were monitored by a calibrated quartz microbalance. All as-prepared layers were annealed at 250 °C for 30 min in Ar atmosphere to ensure good film stability at ambient conditions. This annealing does not lead to phase separation and Si nanoparticle formation [9]. To form silicon nanocrystals (Si NCs) in SiOₓ matrix the samples were furnace annealed at 1000 °C in N₂ for 60 min. Part of the samples without high temperature annealing were used as control samples. After the annealing Al metallization was carried out through a mask and top electrodes (referred from now on as gates) of MOS structures with area of \( \sim 2 \times 10^{-3} \) cm² were formed. Aluminum electrodes were deposited on the bottom side of the silicon substrates.

The thicknesses of the deposited SiOₓ layers were determined ellipsometrically using J.A. Woollam M-2000U instrument and values of approximately 27 and 40 nm were obtained for the thin and thick layers, respectively. For the thermal oxide a value of 24.7 nm was found. The effect of high temperature annealing on the structural modification of SiOₓ was studied by cross-sectional Transmission Electron Microscopy (XTEM) using JEOL JEM-2100F microscope. DC current-voltage (I-V) and high frequency (1 MHz) capacitance-voltage characteristics were measured by Semiconductor Characterization System Keithley 4200-SCS with preamplifiers. The hold and delay times of all measurements were 2 and 0.5 s, respectively. The polarity of the applied voltage given below refers to the top electrode.

3. **Results and Discussion**

Figure 1 shows XTEM images of a high temperature annealed c-Si/SiOₓ/SiOₓ structure with 40 nm thick SiOₓ film. In figure 1(a) two regions can be clearly distinguished: an amorphous layer with thickness of \( \sim 25 \) nm, the thermal SiO₂ and a second one, which exhibits Si nanocrystals (SiOₓ-Si NCs) seen as dark spots. It has been shown that SiOₓ films with \( x = 1.3 \) remain amorphous after 250 °C annealing. Figure 1(a) shows cross-sectional micrographs of an annealed c-Si/SiOₓ/SiOₓ structure with 40 nm SiOₓ layer; (b) high resolution XTEM image showing nanocrystals with size of \( \sim 4–5 \) nm formed after the high temperature annealing.

![Figure 1](image-url)
annealing in Ar [10]. Therefore, the formation of NCs can be attributed to the high temperature annealing. The nanocrystals are randomly distributed along the film thickness. A thin region free of Si nanocrystals is seen close to the top surface, most likely because the nanocrystals in this region get transformed into SiO₂ due to oxidation after exposure to air. From the high resolution image in figure 1b the size of the NCs was determined to be about 4–5 nm.

Figure 2 shows I-V characteristic of a control MOS structure with ~27 nm thick SiOₓ layer. Large difference was observed between the current flowing through the sample at positive and negative voltages. For example, at gate voltage of \( V_g = 30 \) V the current was \( \sim 2.1 \times 10^{-8} \) A (curve 1), while at \( V_g = (-30) \) V it was \( \sim 1.2 \times 10^{-11} \) A (curve 2). The current dependence on the voltage polarity can be related to differences in the properties of the injecting interfaces. At positive voltage electrons are injecting from the c-Si in the thermal oxide overcoming the Si/SiO₂ barrier of 3.1 eV and then in the SiOₓ. At negative voltage, holes could be injected from the silicon in the SiO₂ and electrons from the top metal electrode in the SiOₓ layer. The energy barrier for holes at the Si/SiO₂ interface is much larger (~4.7 eV) than the barrier for electrons at the Al/SiO₂ interface (less than 3.2 eV, the Al/SiO₂ barrier). Therefore, the main part of the current at negative voltage is due to electrons injected from the top electrode. Most likely, part of these electrons are trapped close to the Al electrode forming a negatively charge region which opposes further electron injection and leads to smaller current values.

This assumption was confirmed by high frequency C-V measurements on control c-Si/SiO₂/SiOₓ/Al structure (figure 3). The curves in Figure 3 were measured with consecutive voltage sweeps between 2 V and a negative voltage \( V_L \) in both directions; first from positive to negative voltage and then in the opposite direction. \( V_L \) was varied between (-4) and (-14) V with step of (-2) V. The initial curve was measured in the (+2, -3) V range in order to avoid charging of the structure. All curves show hysteresis corresponding to a negative charge trapped in the insulator after a complete voltage cycle. The change of the flat band voltage \( V_{FB} \) increases with the increase of the absolute value of \( V_L \) (the inset in figure 3). Thus, a sweep to (-14) V results in \( \Delta V_{FB} \sim 0.8 \) V corresponding to charge density of approximately \( 4 \times 10^{11} \) cm⁻² if assumption is made that all electrons are trapped at the Al/SiOₓ interface. No such shifts, corresponding to trapped electrons in the gate insulator were observed when the voltage was varied between (-3) V and positive voltages up to 14 V. Thus, the C-V measurements confirmed that electrons are trapped in the SiOₓ only when negative voltages are applied to the Al electrode; this could be a possible explanation of the asymmetry of the I-V dependencies.

The obtained results indicate that the Al/SiO₂/SiOₓ/c-Si structure favors electric field switching from high to low resistance state by formation of conductive pathway at negative gate voltages because large electric fields (\( E_{ox} \sim 8 \) MV cm⁻¹ at \( V_g \sim (-45) \) V) can be achieved at relatively small currents, \( \sim 10^{-10} \) A (figure 2, curves 2, 3). On the other hand, current driven destruction of the conductive filament may be expected at positive voltages because large currents flow at smaller
electric fields, i.e. $\sim 10^{-8}$ A at $E_{\text{ox}} \sim 5.8$ MV cm$^{-1}$ corresponding to $V_g \sim 30$ V. However, no high-low resistance switching of the control sample was observed for negative voltages in the range between 0 and approximately (-50) V ($E_{\text{ox}} \geq 10$ MV cm$^{-1}$) when destructive breakdown occurs (figure 2, curve 3). No switching was also observed at positive voltages. The current through the gate insulator after destructive breakdown shows similar dependence on the voltage polarity (figure 2, curves 4, 5) as before breakdown, faster current increase in the positive direction.

Thickness of 25 nm was calculated for the thermal oxide from the accumulation capacitance of c-Si/SiO$_2$/Al structure, a value in good agreement with the ellipsometry result. Using the measured capacitance in accumulation of the c-Si/SiO$_2$/SiO$_x$/Al structures (161 pF) and the thicknesses of the SiO$_x$ (27 nm) and SiO$_2$ (25 nm) the dielectric constant of the SiO$_x$ layer was calculated to be $\varepsilon_{\text{SiO}_x} = 4.6$.

In contrast to the control samples the structures annealed at 1000 °C showed resistive switching (figure 4). A strong current increase of more than 3 orders of magnitude was obtained at negative voltages between (-20) and (-25) V (curves 1, 4). After switching the structures maintain the low resistance state at voltages varying between (0, -30) V range (curve 2). Transitions from low to high resistance state were observed with ramps in the positive direction at voltages between 25 and 30 V (curves 3, 5). After switching, $I-V$ curves very close to the initial ones (in both high and low resistive states) were measured. Similar result for resistive switching only in SiO$_x$ with Si nanocrystals and not in control samples was reported in [5].

Interestingly, after several switching cycles some structures remained in high resistance state when the voltage was varied in the negative direction until breakdown was reached (curve 6). It may be assumed that in these capacitors the defect density and other structural modifications caused by the high temperature annealing, which facilitate the formation of conductive pathways is very low. After several cycles the defects are probably completely eliminated and no further high-low resistance transition is possible.

From the obtained results it may be concluded that the studied structures show bipolar switching. None of the measured capacitors was switched from high to low resistance state at positive voltage and from low to high resistance state at negative voltage.

Figure 3. C-V characteristics of c-Si/SiO$_2$/SiO$_x$/Al structure with 27 nm thick SiO$_x$ layer annealed at 250 °C in Ar. The inset shows $\Delta V_{\text{FB}}$ as a function of the negative voltage $V_L$ in the ramp scans (+2,$V_L$) V.
4. Conclusion

Resistive bipolar switching was obtained in annealed c-Si/SiO\(_x\)/SiO\(_x\)/Al structures, which contain Si nanocrystals in the SiO\(_x\) layer. The transition from high to low resistance state was accomplished by electric field formation of conductive pathway in the SiO\(_x\)-Si NCs layer at negative gate voltages, while current driven destruction of the conductive filament was observed at positive voltages. No resistive switching was found in the control c-Si/SiO\(_x\)/SiO\(_x\)/Al structures. From C-V measurements at 1 MHz the dielectric constant of non-annealed SiO\(_x\) (\(x = 1.3\)) films was calculated to be \(\varepsilon_{\text{SiO}_x} = 4.6\).

Further optimization of the proposed structure for memory applications may be achieved by the following modifications: first, decrease of the SiO\(_x\) and thermal oxide thicknesses, which will result in lower switching voltages. Second, increase of the defect density in the SiO\(_x\), which could facilitate the formation of conductive pathways in the annealed structures and eventually lead to resistive switching in non-annealed (control) c-Si/SiO\(_x\)/SiO\(_x\)/Al structures.

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