LANA: Latency Aware Network Acceleration

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Abstract

We introduce latency-aware network acceleration (LANA) – an approach that builds on neural architecture search techniques and teacher-student distillation to accelerate neural networks. LANA consists of two phases: in the first phase, it trains many alternative operations for every layer of the teacher network using layer-wise feature map distillation. In the second phase, it solves the combinatorial selection of efficient operations using a novel constrained integer linear optimization (ILP) approach. ILP brings unique properties as it (i) performs NAS within a few seconds to minutes, (ii) easily satisfies budget constraints, (iii) works on the layer-granularity, (iv) supports a huge search space \(O(10^{100})\), surpassing prior search approaches in efficacy and efficiency.

In extensive experiments, we show that LANA yields efficient and accurate models constrained by a target latency budget, while being significantly faster than other techniques. We analyze three popular network architectures: EfficientNetV1, EfficientNetV2 and ResNeST, and achieve up to 3.0% accuracy improvement for all models when compressing larger models to the latency level of smaller models. LANA achieves significant speed-ups (up to 5\times) with minor to no accuracy drop on GPU and CPU. The code will be available soon.

1. Introduction

In many applications, we may have access to a neural network that satisfies desired performance needs in terms of accuracy but is computationally too expensive to deploy. The goal of hardware-aware network acceleration [5, 13, 27, 57, 65, 101] is to accelerate a given neural network such that it meets efficiency criteria on a device without sacrificing accuracy dramatically. Network acceleration plays a key role in reducing the operational cost, power usage, and environmental impact of deploying deep neural networks in real-world applications.

The current network acceleration techniques can be grouped into: (i) pruning that removes inactive neurons [4, 8, 18–20, 22, 24–26, 28, 29, 33, 35, 36, 38, 42–44, 46–48, 50, 52, 92, 95, 96, 102], (ii) compile-time optimization [60] or kernel fusion [14, 15, 79, 98] that combines multiple operations into an equivalent operation, (iii) quantization that reduces the precision in which the network operates at [7, 11, 16, 34, 54, 63, 81, 85, 99], and (iv) knowledge distillation that distills knowledge from a larger teacher network into a smaller student network [1, 31, 45, 51, 89, 93]. The approaches within (i) to (iii) are restricted to the underlying network operations and they do not change the architecture. Knowledge distillation changes the network architecture from teacher to student, however, the student design requires domain knowledge and is done usually manually.

In this paper, we propose latency-aware network transformation (LANA), a network acceleration framework that automatically replaces inefficient operations in a given network with more efficient counterparts. Given a convolutional teacher network, we formulate the problem as searching in a large pool of candidate operations to find efficient operations for different layers of the teacher. The search problem is combinatorial in nature with a space that grows exponentially with the depth of the network. To solve this problem, we can turn to neural architecture search (NAS) [6, 55, 68, 76, 103, 104], which has been proven successful in discovering novel architectures. However, existing NAS solutions are computationally expensive, and usually handle only a small number of candidate operations (ranging from 5 to 15) in each layer and they often struggle with larger candidate pools.

To tackle the search problem with a large number of candidate operations in an efficient and scalable way, we propose a two-phase approach. In the first phase, we define a large candidate pool of operations ranging from classic residual blocks [21] to recent blocks [2, 15, 17, 64], with varying hyperparameters. Candidate operations are pretrained to mimic
the teacher’s operations via a simple layer-wise optimization. Distillation-based pretraining enables a very quick preparation of all candidate operations, offering a much more competitive starting point for subsequent searching.

In the second phase, we search among the pre-trained operations as well as the teacher’s own operations to construct an efficient network. Since our operation selection problem can be considered as searching in the proximity of the teacher network in the architecture space, we assume that the accuracy of a candidate architecture can be approximated by the teacher’s accuracy and a simple linear function that measures changes in the accuracy for individual operations. Our approximation allows us to relax the search problem into a constrained integer linear optimization problem that is solved in a few seconds. As we show extensively in our experiments, such relaxation can drastically cut down on the cost of our search and it can be easily applied to a huge pool of operations (197 operations per layer), while offering improvements in model acceleration by a large margin.

In summary, we make the following contributions: (i) We propose a simple two-phase approach for accelerating a teacher network using NAS-like search. (ii) We propose an effective search algorithm using constrained integer optimization that can find an architecture in seconds tailored to our setting where a fitness measure is available for each operation. (iii) We examine a large pool of operations including the recent vision transformers and new variants of convolutional networks. We provide insights into the operations selected by our framework and into final model architectures.

1.1. Related Work

Since our goal is to discover new efficient architectures, in this section we focus on related NAS-based approaches.

**Hardware-aware NAS:** The goal of hardware-aware NAS is to design efficient and accurate architectures from scratch while targeting a specific hardware platform. This has been the focus of an increasingly large body of work on multiobjective neural architecture search [6,69,76,77,84,86,90,91]. The goal here is to solve an optimization problem maximizing accuracy while meeting performance constraints specified in terms of latency, memory consumption or number of parameters. Given that the optimization problem is set up from scratch for each target hardware platform, these approaches generally require the search to start from scratch for every new deployment target (e.g., GPU/CPU family) or objective, incurring a search cost that increases linearly as the number of constraints and targets increases. [3] circumvents this issue by training a supernetwork containing every possible architecture in the search space, and then applying a progressive shrinking algorithm to produce multiple high-performing architectures. This approach incurs a high pretraining cost, but once training is complete, new architectures are relatively inexpensive to find. On the other hand, the high computational complexity of pretraining limits the number of operations that can be considered. Adding new operations is also costly, since the supernetwork must be pretrained from scratch every time a new operation is added.

**Teacher-based NAS:** Our work is more related to the line of work that focuses on modifying existing architectures. Approaches in this area build on teacher-student knowledge distillation, performing multiobjective NAS on the student to mimic the teacher network. Pioneering works [41], [37] and [49] demonstrated great benefits of teacher-student NAS, however, can be improved.

The AKD approach [41] applies knowledge distillation at the network level, training a reinforcement learning agent to construct an efficient student network given a teacher network and a constraint and then training that student from scratch using knowledge distillation. DNA [37] and DONNA [49] take a more fine-grained approach, dividing the network into a small number of blocks, each of which contain several layers. During knowledge distillation, they both attempt to have student blocks mimic the output of teacher blocks, but [37] samples random paths through a mix of operators in each block, whereas [49] trains several candidate blocks with a repeated single operation for each teacher block. They then both search for an optimal set of blocks, with DNA [37] using a novel ranking algorithm to predict the best set of operations within each block, and then applying a traversal search, while [49] train a linear model that predicts accuracy of a set of blocks and use that to guide an evolutionary search. While both methods deliver
impressive results, they differ from our approach in important ways. DNA [37] ranks each path within a block, and then uses this ranking to search over the blocks, relying on the low number of blocks to accelerate search. DONNA [49] samples and finetunes 30 models to build a linear accuracy predictor, which incurs a significant startup cost for search. In contrast, we formulate the search problem as an integer linear optimization problem that can be solved very quickly for large networks and large pool of operations.

Table 1 compares our work to these works in detail. We increase the granularity of network acceleration, focusing on each layer individually instead of blocks as done in DNA and DONNA. The main advantage of focusing on layers is that it allows us to accelerate the teacher by simply replacing inefficient layers whereas blockwise algorithms such as DNA and DONNA require searching for an efficient subnetwork that mimics the whole block. The blockwise search introduces additional constraints. For example, both DNA and DONNA enumerate over different depth values (multiplying the search space) while we reduce depth simply using an identity operation. Additionally, DONNA assumes that the same layer in each block is repeated whereas we have more expressivity by assigning different operation to different layers. The expressivity can be seen from the design space size in Table 1 in which our search space is orders of magnitude larger. On the other side, this extremely large space necessitate the development of a highly efficient search method based on integer linear optimization (presented in Section 2). As we can see from Table 1, even with significantly larger search space, our total cost is lower than prior work. We additionally introduce zero-shot formation when the teacher cell and the identity operations participate in ILP, reducing the pretraining and the search costs to a minimum.

2. Method

Our goal in this paper is to accelerate a given pre-trained teacher network by replacing its inefficient operations with more efficient alternatives. Our method, visualized in Fig. 1, is composed of two phases: (i) Candidate pretraining phase (Sec. 2.1), in which we use distillation to train a large set of operations to approximate different layers in the original teacher architecture; (ii) Operation selection phase (Sec. 2.2), in which we search for an architecture composed of a combination of the original teacher layers and pretrained efficient operations via linear optimization.

2.1. Candidate Pretraining Phase

We represent the teacher network as the composition of $N$ teacher operations by $T(x) = t_N \circ t_{N-1} \circ \ldots \circ t_1(x)$, where $x$ is the input tensor, $t_i$ is the $i$th operation (i.e., layer) in the network. We then define the set of candidate student operations $\bigcup_{i=1}^{N} \{s_{ij} \}_{j=1}^{M}$, which will be used to approximate the teacher operations. Here, $M$ denotes the number of candidate operations per layer. The student operations can draw from a wide variety of operations – the only requirement is that all candidate operations for a given layer must have the same input and output tensor dimensions as the teacher operation $t_i$. We denote all the parameters (e.g., trainable convolutional filters) of the operations as $W = \{w_{ij} \}_{i,j}^{N,M}$, where $w_{ij}$ denotes the parameters of the student operation $s_{ij}$. We use a set of binary vectors $Z = \{z_i \}_{i=1}^{N}$, where $z_i = \{0, 1\}^M$ is a one-hot vector, to represent operation selection parameters. We denote the candidate network architecture specified by $Z$ using $S(x; Z, W)$.

The problem of optimal selection of operations is often tackled in NAS. This problem is usually formulated as a bi-level optimization that selects operations and optimizes their weights jointly [40, 103]. Finding the optimal architecture in hardware-aware NAS reduces to:

$$\min_{Z} \min_{W} \sum_{(x,y) \in X_{tr}} \mathcal{L}(S(x; Z, W), y), \tag{1}$$

subject to:

$$\sum_{i=1}^{N} b_i^T z_i \leq B; \quad 1^T z_i = 1 \forall i \in [1..N]$$

where $b_i \in \mathbb{R}_+^M$ is a vector of corresponding cost of each student operation (latency, number of parameters, FLOPs, etc.) in layer $i$. The total budget constraint is defined via scalar $B$. The objective is to minimize the loss function $\mathcal{L}$ that estimates the error with respect to the correct output $y$ while meeting a budget constraint. In general, the optimization problem in Eq. 1 is an NP-hard combinatorial problem with an exponentially large state space (i.e., $M^N$). The existing NAS approaches often solve this optimization using evolutionary search [58], reinforcement learning [103] or differentiable search [40].

However, the goal of NAS is to find an architecture in the whole search space from scratch, whereas our goal is to improve efficiency of a given teacher network by replacing operations. Thus, our search can be considered as searching in the architecture space in the proximity of the teacher network. That is why we assume that the functionality of each candidate operation is also similar to the teacher’s operation, and we train each candidate operation to mimic the teacher operation using layer-wise feature map distillation with the mean squared error (MSE) loss:

$$\min_{W} \sum_{x \in X_{tr}} \sum_{i,j} \|t_i(x_{i-1}) - s_{ij}(x_{i-1}; w_{ij})\|^2, \tag{2}$$

where $X_{tr}$ is a set of training samples, and $x_{i-1} = t_{i-1} \circ t_{i-2} \circ \ldots \circ t_1(x)$ is the output of the previous layer of the teacher, fed to both the teacher and student operations.
Our layer-wise pretraining has several advantages. First, the minimization in Eq. 2 can be decomposed into $N \times M$ independent minimization problems as $w_{i,j}$ is specific to one minimization problem per operation and layer. This allows us to train all candidate operations simultaneously in parallel. Second, since each candidate operation is tasked with an easy problem of approximating one layer in the teacher network, we can train the student operation quickly in one epoch. In this paper, instead of solving all $N \times M$ problems in separate processes, we train a single operation for each layer in the same forward pass of the teacher to maximize reusing the output features produced in all the teacher layers. This way the pretraining phase roughly takes $O(M)$ epochs of training a full network.

### 2.2. Operation Selection Phase

Since our goal in search is to discover an efficient network in the proximity of the teacher network, we propose a simple linear relaxation of candidate architecture loss using

$$
\sum_{X_{tr}} \mathcal{L}(S(x; Z), y) \approx \sum_{X_{tr}} \mathcal{L}(T(x), y) + \sum_{i=1}^{N} a_i^T z_i, \tag{3}
$$

where the first term denotes the training loss of teacher which is constant and $a_i$ is a vector of change values in the training loss per operation for layer $i$. Our approximation bears similarity to the first-degree Taylor expansion of the student loss with the teacher as the reference point (since the teacher architecture is a member of the search space). To compute $\{a_i\}_i^{N}$, after pretraining operations in the first stage, we plug each candidate operation one-by-one in the teacher network and we measure the change on training loss on a small labeled set. Our approximation relaxes the non-linear loss to a linear function. Although this is a weak approximation that ignores how different layers influence the final loss together, we empirically observe that it performs well in practice as a proxy for searching the student.

Approximating the architecture loss with a linear function allows us to formulate the search problem as solving an integer linear program (ILP). This has several main advantages: (i) Although solving integer linear programs is generally NP-hard, there exist many off-the-shelf libraries that can obtain a high-quality solutions in a few seconds. (ii) Since integer linear optimization libraries easily scale up to millions of variables, our search also scales up easily to very large number of candidate operations per layer. (iii) We can easily formulate the search problem such that instead of one architecture, we obtain a set of diverse candidate architectures. Formally, we denote the $k$th solution with $\{Z^{(k)}\}_{k=1}^{K}$, which is obtained by solving:

$$\min_{Z^{(k)}} \sum_{i=1}^{N} a_i^T z_i, \quad \text{s.t.} \quad \sum_{i=1}^{N} b_i^T z_i \leq B; \quad 1^T z_i = 1 \quad \forall \ i; \quad \text{one op per layer}$$

$$\sum_{i=1}^{N} z_i^{(k)} \leq 1 \quad \forall k' < k \tag{4}$$

where the overlap constraint

$$\sum_{i=1}^{N} z_i^{(k)} \leq 1$$

which is obtained by solving:

$$\Delta L = \sum_{i=1}^{N} \frac{\Delta a_i^T z_i}{\Delta a_i} \frac{\Delta z_i}{\Delta a_i}$$

where $\Delta a_i$ is a small change in the $i$th element of $a_i$.

### Figure 1. LANA consists of two phases: a candidate pretraining phase (a) and an architecture search phase (b).

(a) Candidate pretraining phase: We minimize the MSE loss between the output of the teacher operation $t_i$ and the output of each student operation on each layer $s_{i,j}$, where the input to each operation is the teacher output from the previous layer.

(b) Operation Selection Phase: We estimate and record in a lookup table the reduction of network accuracy and latency from replacing a teacher operation with one of the student operations. We then apply integer programming to minimize the accuracy reduction while attaining a target latency reduction.
where we minimize the change in the loss while satisfying the budget and overlap constraint. The scalar $\mathcal{O}$ sets the maximum overlap with any previous solution which is set to 0.7$N$ in our case. We obtain $K$ diverse solutions by solving the minimization above $K$ times.

**Solving the integer linear program (ILP).** We use the off-the-shelf PuLP Python package to find feasible candidate solutions. The cost of finding the first solution is very small, often less than 1 CPU-second. As $K$ increases, so does the difficulty of finding a feasible solution. We limit $K$ to $\sim 100$.

**Candidate architecture evaluation.** Solving Eq. 4 provides us with $K$ architectures. The linear proxy used for candidates loss is calculated in an isolated setting for each operation. To reduce the approximation error, we evaluate all $K$ architectures with pretrained weights from phase one on a small part of the training set (6k images on ImageNet) and select the architecture with the lowest loss.

**Candidate architecture fine-tuning.** After selecting the best architecture among the $K$ candidate architectures, we fine-tune it for 100 epochs using the original objective used for training the teacher. Additionally, we add the distillation loss from teacher to student during fine-tuning.

### 3. Experiments

We apply LANA to the family of EfficientNetV1 [71], EfficientNetV2 [73] and ResNeST50 [100]. When naming our models, we use the latency reduction ratio compared to the original model according to latency look-up table (LUT). For example, 0.25×B6 indicates 4× target speedup for the B6 model.

For experiments, ImageNet-1K [59] is used for pretraining (1 epoch), candidate evaluation (6k training images) and finetuning (100 epochs).

We use the NVIDIA V100 GPU and Intel Xeon Silver 4114 CPU as our target hardware. A hardware specific look-up table is precomputed for each candidate operation (vectors $b_i$ in Eq. 4). We measure latency in 2 settings: (i) in Pytorch framework, and (ii) TensorRT [53]. The latter performs kernel fusion for additional model optimization making it even harder to accelerate models. Note that the exact same setup is used for evaluating latency of all competing models, our models, and baselines. Actual latency on the target platform is reported in the tables.

**Candidate operations.** We construct a large pool of diverse candidate operation including $M = 197$ operations for each layer of teacher. Our operations include:

- Teacher operation is used as is in the pretrained model with teacher model accuracy.
- Identity is used to skip teacher’s operation. It changes the depth of the network.
- Inverted residual blocks $efn$ [61] and $efnv2$ [73] with varying expansion factor $e = \{1, 3, 6\}$, squeeze and excitation ratio $se = \{No, 0.04, 0.025\}$, and kernel size $k = \{1, 3, 5\}$.

**Dense convolution blocks** inspired by [22] with (i) two stacked convolution (cb_stack) with CBRCB structure, C-conv, B-batchnorm, R-Relu; (ii) bottleneck architecture (cb_bottle) with CBR-CBR-CB; (ii) CB pair (cb_res); (iii) RepVGG block [15]; (iv) CBR pairs with perturbations as conv_cs. For all models we vary kernel size $k = \{1, 3, 5, 7\}$ and width $w = \{1/16, 1/10, 1/8, 1/5, 1/4, 1/2, 2, 3, 4\}$.

- Transformer variations (i) visual transformer block (vit) [17] with depth $d = \{1, 2\}$, dimension $w = \{2^5, 2^6, 2^7, 2^8, 2^9, 2^{10}\}$ and heads $h = \{4, 8, 16\}$; (ii) bottleneck transformers [64] with 4 heads and expansion factor $e = \{1/4, 1/2, 1, 2, 3, 4\}$; (iii) lambda bottleneck layers [2] with expansion $e = \{1/4, 1/2, 1, 2, 3, 4\}$.

With the pool of 197 operations, distilling from an EfficientNet-B6 model with 46 layers yields a design space of the size $197^{100} \approx 10^{100}$.

#### 3.1. EfficientNet and ResNeST Derivatives

Our experimental results on accelerating EfficientNetV1(B2, B4, B6), EfficientNetV2(B3), and ResNeST50 family for GPUs are shown in Table 2 and Figure 2. Comparison with more models from timm is in the Appendix.

**Results demonstrate that:**

- LANA achieves an **accuracy boost of 0.18 − 3.0%** for all models when compressing larger models to the latency level of smaller models (see EfficientNet models and the corresponding LANA models in the same latency group).
- LANA achieves **significant real speed-ups** with little to no accuracy drop: (i) EfficientNetV1-B6 accelerated by 3.6x and 1.8x times by trading-off 0.34% and 0.11% accuracy, respectively; (ii) B2 variant is accelerated 2.4x and 1.9x times with 0.36% and no accuracy loss, respectively. (iii) ResNeST50 is accelerated 1.5x with 0.84% accuracy drop.

A detailed look on EfficientNets is shown in Figure 2, where we observe that EfficientNetV1 models are accelerated beyond EfficientNetV2. LANA generates models that have better accuracy-throughput trade-off when comparing models under the same accuracy or the same latency. LANA also allows us to optimize models for different hardware at a little cost. Only a new LUT is required to get optimal model for a new hardware without pretraining the candidate operations again. We present models optimized for CPU in Table 3 which are obtained using a different LUT.

#### 3.2. Analysis

Here, we provide detailed ablations to analyze our design choices in LANA for both pretraining and search phases, along with observed insights. Unless otherwise stated, we used EfficientNetV2-B3 as our teacher for the ablation.

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1 can potentially be improved by parallelization
**Table 2. Models optimized with LANA for GPU inference, evaluated on ImageNet-1K.** Latency is computed for a batch of 128 images over 10 runs on the actual hardware. Models are grouped by the latency to demonstrate accuracy improvement over the vanilla EfficientNet models with default model scaling.

| Method          | Variant | Res (px) | Accuracy (%) | Latency (ms) TensorRT | PyTorch |
|-----------------|---------|----------|--------------|-----------------------|---------|
| EfficientNetV1  | 1.00xB0| 224      | 77.70        | 17.9                  | 35.6    |
| LANA            | 0.45xB2| 260      | 79.71 (+2.01) | 16.2                  | 30.2    |
| EfficientNetV1  | 1.00xB1| 240      | 78.83        | 29.3                  | 59.0    |
| LANA            | 0.55xB2| 260      | 80.11 (+1.28) | 20.6                  | 48.7    |
| LANA            | 0.20xB4| 380      | 80.33 (+1.50) | 33.0                  | 52.2    |
| LANA            | 0.25xB4| 380      | 81.33 (+3.00) | 30.4                  | 64.5    |
| EfficientNetV1  | 1.00xB2| 260      | 80.07        | 38.2                  | 77.1    |
| LANA            | 0.3xB4 | 380      | 82.16 (+2.09) | 38.8                  | 81.8    |
| EfficientNetV1  | 1.0xB3 | 300      | 81.67        | 67.2                  | 125.9   |
| LANA            | 0.5xB4 | 380      | 82.66 (+0.99) | 61.4                  | 148.1   |
| EfficientNetV1  | 1.00xB4| 380      | 83.02        | 132.0                 | 262.4   |
| LANA            | 0.25xB6| 528      | 83.77 (+0.75) | 128.8                 | 282.1   |
| EfficientNetV1  | 1.0xB5 | 456      | 83.81        | 265.7                 | 525.6   |
| LANA            | 0.5xB6 | 528      | 83.99 (+0.18) | 266.5                 | 561.2   |
| EfficientNetV1  | 1.0xB6 | 528      | 84.11        | 466.7                 | 895.2   |

**Table 3. EfficientNetV1 accelerated by LANA for CPU inference.**

| Model           | Res. (px) | Accuracy (%) | Latency (PyTorch) (ms) |
|-----------------|-----------|--------------|-----------------------|
| EfficientNetB0  | 224       | 77.70        | 57                    |
| 0.4xB2 (Xeon)   | 260       | 78.11 (+0.97) | 48                    |
| 0.5xB2 (Xeon)   | 260       | 78.87 (+1.17) | 58                    |
| EfficientNetB1  | 240       | 78.83        | 86                    |
| 0.7xB2 (Xeon)   | 260       | 79.89 (+1.06) | 80                    |
| EfficientNetB2  | 260       | 80.07        | 113                   |

**Figure 2.** A visual summary of the EfficientNetV1 and EfficientNetV2 model families accelerated by LANA. Accelerated EfficientNetV1 models outperform EfficientNetV2 models.

**Linear relaxation** in architecture search assumes that a candidate architecture can be scored by a fitness metric measured independently for all operations. Although this relaxation is not accurate, we observe a strong correlation between our linear objective and the training loss of the full architecture. This assumption is verified by sampling 1000 architectures (different budget constraints), optimizing the ILP objective, and measuring the real loss function. Results are shown in Fig. 3(a) using the train accuracy as the loss. We observe that ILP objective ranks models with respect to the measured accuracy correctly under different latency budgets. The Kendall Tau correlation is 0.966.

To evaluate the quality of the solution provided with ILP, we compare it with random sampling. The comparison is shown in Fig. 3(b), where we sample 1000 random architectures for 7 latency budgets. The box plots indicate the poor performance of the randomly sampled architectures. The first ILP solution has significantly higher accuracy than random architecture. Furthermore, finding multiple diverse solutions is possible with ILP using the overlap constraint. If we increase the number of solutions found by ILP from $K=1$ to $K=100$, performance improves further.

**Candidate architecture evaluation** plays an important role in LANA. This step finds the best architecture quickly out of the diverse candidates generated by the ILP solver, by evaluating them on 6k images from the train data. The procedure is built on the assumption that the accuracy of the model on the training data before finetuning (just by plugging all candidate operations) is a reasonable indicator of the relative model performance after finetuning. As shown in Fig. 3(b), when plugging pretrained operations into the teacher, the accuracy is high (it is above 30%, even at an acceleration factor of 2×). For EfficientNetV1, this is above 50% for the same compression factor.

**Comparing with other NAS approaches.** We compare our search algorithm with other popular approaches to solve Eq. (1), including: (i) Random architecture sampling within a latency constrain; (ii) **Differentiable search with Gumbel Softmax** – a popular approach in NAS to relax binary optimization as a continuous variable optimization via learning the sampling distribution [76, 84, 88]. We follow SNAS [88] in this experiment; (iii) **REINFORCE** is a stochastic optimization framework borrowed from reinforcement learning and adopted for architecture search [55, 70, 104]. We follow an E-NAS-like [55] architecture search for (iii) and...
Table 4. Comparing methods for candidate selection (NAS). Our proposed ILP is better (+0.43%) and 821× faster.

| Method                  | Accuracy | Search cost |
|-------------------------|----------|-------------|
| ILP, K=100 (ours)      | 79.28    | 4.5 CPU/m   |
| Random, found 80 arch   | 76.44    | 1.4 CPU/m   |
| SNAS [88]               | 74.20    | 16.3 GPU/h  |
| E-NAS [55]              | 78.85    | 61.6 GPU/h  |

Table 5. Zero-shot LANA with only skip connections.

| Setup          | Top-1 Acc. | Zero-shot | All operations | Latency(ms) | TensorRT |
|----------------|------------|-----------|----------------|-------------|----------|
| 0.45xEfficientNetV1-B2 | 78.68      | 79.71     | 16.2           |             |          |
| 0.55xEfficientNetV1-B2 | 79.40      | 80.11     | 20.6           |             |          |
| EfficientNetV1-B0   | 77.70      | 17.9      |                |             |          |
| EfficientNetV1-B2   | 80.07      |           | 38.8           |             |          |

use weight sharing for (ii) and (iii). Experiments are conducted on EfficientNetV1-B2 accelerated to 0.45× original latency. The final validation top-1 accuracy after finetuning are presented in Table 4. Our proposed ILP achieves higher accuracy (+0.43%) compared to the second best method E-NAS while being 821× faster in search.

Zero-shot LANA. Our method can be applied without pretraining procedure if only teacher cells and Identity (skip) operation are used ($M = 2$ operations per layer). Only the vector for the change in loss for the Identity operator will be required alongside the LUT for the teacher operations. This allows us to do zero-shot network acceleration without any pretraining as reported in Table 5. We observe that LANA efficiently finds residual blocks that can be skipped. This unique property of LANA is enabled because of accelerating layers as apposed to blocks as done in [37,49].

Pretraining insights. To gain more insights into the tradeoff between the accuracy and speed of each operation, we analyze the pretrained candidate operation pool for EffientNetV1B2. A detailed figure is shown in the appendix. Here, we provide general observations.

We observe that no operation outperforms the teacher in terms of accuracy: changing pretraining loss from per-layer MSE to full-student cross-entropy may change this but that comes with an increased costs of pretraining. We also see that it is increasingly difficult to recover the teacher’s accuracy as the depth in the network increases. The speedups achievable are roughly comparable across different depths, however, we note that achieving such speedups earlier in the network is particularly effective towards reducing total latency due to the first third of the layers accounting for 54% of the total inference time.

Looking at individual operations, we observe that inverted residual blocks (efn, efnv2) are the most accurate throughout the network, at the expense of increased computational cost (i.e., lower speedups). Dense convolutions (cb_stack, cb_bottle, conv_cs, cb_res) exhibit a good compromise between accuracy and speed, with stacked convolutions being particularly effective earlier in the network. Visual transformer blocks (ViT) and bottleneck transformer blocks (bot_trans) show neither a speedup advantage nor are able to recover the accuracy of the teacher.

3.2.1 Architecture insights

In the appendices, we visualize the final architectures discovered by LANA. Next, we share the insights observed on these architectures.

EfficientNetV1. Observing final architectures obtained by LANA on the EfficientNetV1 family, particularly the 0.55×B2 version optimized for GPUs, we discover that most of the modifications are done to the first half of the model: (i) squeeze-and-excitation is removed in the early layers; (ii) dense convolutions (like inverted stacked or bottleneck residual blocks) replace depth-wise separable counterparts;
We further verify whether we can achieve a similar high accuracy without any loss in accuracy, yielding a 1.45% performance degradation of 0.65%. This emphasizes the benefit of large model optimizations on latency as ours.

**EfficientNetV2.** LANA accelerates EfficientNetV2-B3 by 2×, leading to the following conclusions: (i) the second conv-bn-act layer is not needed and can be removed; (ii) the second third of the model benefits from reducing the expansion factor from 4 to 1 without squeeze-and-excitation operations. With these simplifications, the accelerated model still outperforms EfficientNetV2-B2 and B1.

**ResNeST50.** LANA on ResNeST50d discovers that cardinality can be reduced from 4 to 1 or 2 for most blocks without any loss in accuracy, yielding a 1.45× speedup.

### 3.2.2 Ablations on finetuning

**Pretrained weights.** We look deeper into the finetuning step. For this experiment, we select our 0.45× EfficientNetV1-B2 with the final accuracy of 79.71%. Reinitializing all weights in the model, as opposed to loading them from the pretrained stage, results in 79.42%. The result indicates the importance of pretraining stage (i) to find a strong architecture and (ii) to boost finetuning.

**Knowledge distillation** plays a key role in student-teacher setups. When it is disabled, we observe an accuracy degradation of 0.65%. This emphasizes the benefit of training a larger model and then distilling to a smaller one. We further verify whether we can achieve a similar high accuracy using knowledge distillation from EfficientNetV1-B2 to vanilla EfficientNetV1-B0 in the same setting. The top-1 accuracy of 78.72% is still 1% less than LANA’s accuracy. When both models are trained from scratch with the distillation loss, LANA 0.45xB2 achieves 79.42% while EfficientNetV1-B0 achieves 78.01%. This verifies that results similar to LANA cannot be obtained simply by distilling knowledge from larger EfficientNets to smaller ones.

**Length of finetuning.** Pretrained operations have already been trained to mimic the teacher layer. Therefore, even before finetuning the student model can be already adept at the task. Next, we evaluate how does the length of finetuning affects the final accuracy in Table 6. Even with only 5 epochs LANA outperforms the vanilla EfficientNet counterparts.

**Search space size.** ILP enables us to perform NAS in a very large space \(O(10^{108})\). To verify the benefit of large search space, we experiment with a restricted search space. For this, we randomly pick 2, 5 and 10 operations per layer to participate in search and finetuning for 50 epochs. We observe clear improvements from increasing the search space, shown Table 7 (results are averaged over 5 runs).

**Comparison to [49].** DONNA has a similar motivation ours and has reported results comparable to our setup. We observe significant improvements over DONNA in the Table 8 with lower latency and higher accuracy.

### 4. Conclusion

In this paper, we proposed LANA, a hardware-aware network transformation framework for accelerating pretrained neural networks. LANA uses a NAS-like search to replace inefficient operations with more efficient alternatives. It tackles this problem in two phases including a candidate pretraining phase and a search phase. The availability of the teacher network allows us to estimate the change in accuracy for each operation at each layer. Using this, we formulate the search problem as solving a linear integer optimization problem, which outperforms the commonly used NAS algorithms while being orders of magnitude faster. We applied our framework to accelerate EfficientNets (V1 and V2) and ResNets with a pool of 197 operations per layer and we observed that LANA accelerates these architectures by several folds with only a small drop in the accuracy. We analyzed the selected operations and we provided new insights for future neural architecture designs.

### Limitations.

The student performance in LANA is bounded by the teacher, and it rarely passes the teacher in terms of accuracy. Additionally, the output dimension of layers in the student can not be changed, and must remain the same as in the original teacher.

**Future work.** We envision that a layer-wise network acceleration framework like LANA can host a wide range of automatically and manually designed network operations,
developed in the community. Users with little knowledge of network architectures can then import their inefficient networks in the framework and use LANA to accelerate them for their target hardware. Our design principals in LANA consisting of extremely large operation pool, efficient layer-wise pretraining, and lightening fast search help us realize this vision. We will release the source code for LANA publicly to facilitate future development in this space.

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Appendix

Distribution of selected operations. In Fig. 4, we provide the histogram of selected operations for three EfficientNetV1t networks and different acceleration ratios. All statistics are calculated for the first 100 architectures found via integer optimization.

Final architectures. Fig. 5 and Fig. 6 visualize the final architectures found by LANA. We observe that teacher ops usually appear towards the end of the networks. Identity connections appear in the first few resolution blocks where the latency is the highest to speed up inference, for example 0.2×B4 has 2, 1, 1 in the first 3 resolution blocks from original 3, 4, 4.

4.1. Additional implementation details

We next provide details on chosen batch size defined as \( bs \) and learning rate \( lr \), joint with other details required to replicate results in the paper.

Pretraining implementation. Pretraining stage was implemented to distill a single operator over all layers in parallel on 4xV100 NVIDIA GPU with 32GB. For EfficientNet-B2 we set \( lr=0.008 \) with \( bs=128 \), for EfficientNet-B4 \( lr=0.0005 \) with \( bs=40 \), and EfficientNet-B6 \( lr=0.0012 \) with \( bs=12 \). We set \( \gamma_{MSE} = 0.001 \). We run optimization with an SGD optimizer with no weight decay for 1 epoch only.

Finetuning implementation. Final model finetuning runs for 100 epochs. We set \( bs=128 \) and \( lr=0.02 \) for EfficientNet-B2 trained on 2x8 V100 NVIDIA GPU; for EfficientNet-B4 derivatives we set \( bs=128 \) and \( lr=0.04 \), for EfficientNet-B6 \( bs=48 \) and \( lr=0.08 \) on 4x8 V100 NVIDIA GPU. Learning rate was set to be 0.02. We set \( \gamma_{CE} \) and \( \gamma_{KL} \) to 1.

Latency look up table creations. We measure the latency on V100 NVIDIA GPU with TensorRT in FP16 mode for batch size of 128 images. For Xeon CPU latency we use a batch size of 1. Input and output stems are not included in latency LUT. This results in a small discrepancy between theoretical and real speed. As a result, we use latency LUT for operator evaluation, and report the final real latency for the unveiled final models.

4.2. Candidate pretraining insights

Latency-accuracy tradeoff for different operations after pretraining is shown in the Figure 8. Observations from these plots are discussed in Section 3.2.

The choice of pretraining loss. To motivate our choice of MSE for pretraining, we investigate the distribution of activations at the output of residual blocks. We observe that for all blocks, activations follow a Gaussian-like distribution. Shapiro-Wilk test for normality averaged over all layers is 0.99 for EfficientNetV1-B2, and 0.988 for EfficientNetV2-B3. Given this observation, MSE error seems a reasonable loss function to minimize.

4.3. Detailed comparison to prior work

For comparison to prior work we look into latest models from the out-of-the-box timm package [83] with Apache-2.0 License. We include detailed individual method names and references as follows:

- efficientnet: Efficientnet [71].
- ca1t: Class-attention in image transformers [75].
- cspnet: Cross-stage partial network [78].
- deit: (Data-efficient) vision transformer [74].
- dlia: Deep layer aggregation [94].
- dpn: Dual-path network [10].
- ecanet: Efficient channel attention network [82].
- hrnet: High-resolution network [80].
- inception: Inception V3 [67] and V4 [66].
- mixnet: MixConv-backed network [72].
- ofa: Once-for-all network [5].
- pilt: Pooling Vision Transforms [30].
- regnetX: Regnet network [56], accuracy is taken from the original paper.
- regnetY: Regnet network [56] with squeeze-and-excitation operations, accuracy is taken from the original paper.
- repvgg: RepVGG [15].
- resnest101_e: Resnest101 (with bag of tricks) [23].
- resnest50_d: Resnest50 (with bag of tricks) [23].
- resnet50_d: Resnet50 (with bag of tricks) [23].
- resnetrs10_1: Resnet rescaled [3].
- resnetrs15_1: Resnet rescaled [3].
- resnet50_0: Resnet rescaled [3].
- resnext50d_32x4d: Resnext network (with average pooling downsampling) [87].
- seresnet5_0: Squeeze Excitement Resnet50 [32].
- skresnext50_32x4d: Selective kernel Resnext50 [39].
- vitt-base: Visual Transformer, base architecture.
- vitt-large_384: Visual Transformer, large architecture, 384 resolution [17].
- wide_resnet50_2: Resnet50 with 2x channel width [97].
- xception6_5: Xception network (original) [12].
- xception7_1: Xception network aligned [9].

A more detailed comparison with other models is shown in the Figure 9. We observe that models resulted from LANA acceleration are performing better than the most of other ap-
Figure 4. The histogram of selected operations for top-100 models of EfficientNetV1 derivatives. Teacher layers are often selected especially in the deeper layers of the network as we visualize in Fig. 5 and Fig. 6. The identity layer is also selected often especially when the target latency is low. Interestingly, simple layers with two stacked convolution (cb_stack) in the CBRCB structure (C-convolution, B-batchnorm, R-ReLU) are selected most frequently after the teacher and identity operations. Additionally, we see a higher chance of selecting inverted residual blocks (efn and efn2) with no squeeze-and-excitation operations se1.00.

proaches. All of the models for LANA used LUTs computed with TensorRT and clearly the speed up in the TensorRT figure is larger when compared with other methods. On the same time if model latency is estimated with Pytorch, we still get top models that outperform many other models.
Figure 5. Final architectures selected by LANA as EfficientNet-B2/B6 derivatives.
Figure 6. Final architectures selected by LANA as EfficientNetV1-B4/V2-B3 derivatives.
Figure 7. Final architectures selected by LANA as 0.7xResNeST50d_1s4x24d

Figure 8. Result of the pretraining stage for EfficientNetB2, showing three layers equally spaced throughout the network: 7, 14 and 21. Speedup is measured as the ratio between the latency of the teacher and the latency of the student operation (higher is better). We measure latency using Pytorch FP16. Accuracy is the ratio of the operation’s accuracy and the teacher’s (higher is better). The dashed black lines correspond to the teacher.
Figure 9. Comparison with other models from TIMM package.