A Closed-Form Mathematical Model and Method for Fast Fault Location on a Low Voltage DC Feeder Using Single-Ended Measurements

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ABSTRACT Fault location on a dc microgrid feeder needs to be extremely fast to protect the circuit breaker and converter-source components. This paper develops a seminal theoretical foundation for fast fault location on a dc feeder that uses only single-ended local measurements in time domain. The theory provides a closed-form deterministic solution for fault location, making the resulting fault location method agnostic to system-topology and immune to fault resistance. The theory is developed with ideal dc voltage sources, and extended to practical converter-sources. The performance of the resulting method is demonstrated by simulating a dc feeder with converters connected at both ends, modeled in PSCAD.

INDEX TERMS DC distribution, microgrid, fault, protection.

I. INTRODUCTION

As penetration of solar-photovoltaic (PV) and storage grows in distribution systems, the concept of dc microgrids is gaining traction due to lower conversion losses and the inherent ease of operation of dc systems [1]. However, for safe operation of any system, a faulted feeder must be quickly and selectively isolated, without having to shut down the whole system. This requires an accurate fault detection and location technique. For dc feeders the speed of fault location becomes critical, typically 10's of microseconds, due to the following reasons.

1) In response to a fault, current in dc circuits rises in a matter of tens of microseconds [2], without having a natural current zero. If the fault current crosses the breaking limit of the controlling circuit breaker, it can not be interrupted.

2) A dc microgrid is fed by dc-dc converters that interface renewable sources and ac-dc converters that connect the microgrid with the ac grid. These converters are made of power electronic devices such as diodes and IGBTs, and have capacitors connected at their dc side, known as dc link capacitors. When a fault occurs in a dc microgrid, current from these capacitors dominates at first. After the capacitor voltage drops to a critical value, a high fault current starts to flow through the power electronic devices [3], [4], exposing them to damage.

Due to the speed constraints a fault location scheme that avoids communication from the other end of the feeder to locate fault could be very useful. However, the biggest hurdle in locating fault on a feeder using only single-ended measurements is the presence of unknown fault resistance. As the literature survey presented now shows, a single-ended fault location method for a dc feeder fed from both ends that is immune to fault resistance has yet to be developed.

In [5], [6], the faulted section is isolated, but the location of fault on that section is not determined. Schemes in [3], [4] use iterative methods for determining fault location, but the
execution time increased with increasing distance to the fault point and increasing value of fault resistance. In [7], a local measurement based fault location method is used for bolted faults only; for any other fault involving a resistance, authors had to use communication. An inductance based fault location method was proposed in [8], [9], but the method can only be applied if the system is radial, and the fault current is being sourced from one end only. However, a dc microgrid will certainly have multiple sources, and therefore a fault will be fed from both ends of the faulted feeder.

Some offline methods were also proposed for fault location to avoid communication, using a power probe unit (PPU) [10], [11] and a portable current injection kit (CIK) [12]. However, these offline techniques can be used only after the faulted section is isolated by some other means. Also, as PPU or CIK are only used in locating the fault, which adds extra cost to the system.

Traveling wave based methods were used in a number of papers for locating faults in HVDC systems [13]. However, a traveling wave based method is not practical for dc microgrids. Due to the complex topology of the distribution system, a large number of reflections take place, compromising the accuracy of the method [14]. Additionally, very short feeder-lengths, characteristic of dc microgrids, hamper the process of isolating traveling waves.

Machine learning (ML) based approaches are also tried for fault location in dc microgrid. For example, two different Artificial Neural Networks (ANNs) were used for fault location and fault detection in a 4 bus ring type dc microgrid in [15]. This method is system dependent, as any change in the network will require a new set of simulations to train the ANN again with new circuit parameters. It is also practically impossible to show the method performs well for every fault at any distance with any fault resistance. Moreover, lack of field data compromises the validity of such ML based approaches.

To overcome these drawbacks this paper develops a deterministic closed-form mathematical formulation that forms the foundation of a single-ended fault location method for a feeder fed from both ends that is immune to fault resistance. It can be implemented in both radial and meshed networks. The only constraint is that the data should be sampled at a high enough frequency for the current derivative to be calculated accurately. By properly adjusting the sampling frequency, high-resistance faults can also be located by this method. The fault is detected and located using only three fault-samples, which means that for a sampling frequency of 1 MHz (assumed in this paper), the time taken is just 3 μs.

Since commercially available relays already use this sampling frequency [16], and oscilloscopes support even higher sampling frequencies [17], this assumption is reasonable. Since the formulation uses the total resistance and inductance of only the protected feeder, the resulting method becomes system-independent, i.e., any change in the operating parameters of the system or any topological change in the network will not impact the detection or location of fault by this method.

The rest of the paper is organized as follows. Section II presents the theoretical proof that forms the foundation of the proposed method with ideal dc voltage sources. Section III validates the theory with simulated data, Section IV shows how the method is applicable to a practical test feeder fed by converter-based sources, Section V shows how the method can be adapted for any value of fault resistance, Section VI includes sensitivity analysis of this method with respect to various parameters, and Section VII concludes the paper and describes future work.

II. DERIVATION OF THEORY FOR THE PROPOSED METHOD WITH IDEAL SOURCES

A. FAULT CURRENTS

Fig. 1(a) shows a two-bus dc system with a dc feeder connected between Bus 1 and Bus 2. Two voltage sources with steady state values $V_1$ and $V_2$ are feeding the line from the two buses. At a distance $x$ from Bus 1, a fault with a fault resistance $R_f$ is assumed. Current $I_0$ is flowing from Bus 1 to Bus 2 before the fault. Due to short lines in dc microgrids, line capacitance is ignored in Fig. 1, and the line is approximated with an inductance and a resistance only. Other circuit parameters used in the development of theory are as follows:

- $R_1, L_1 = $ resistance and inductance, respectively, of line-section from Bus 1 to fault.
- $R_2, L_2 = $ resistance and inductance respectively, of line-section from Bus 2 to fault.
- $R, L = $ total resistance and inductance of line.
- $r, l = $ resistance and inductance per unit length of the line.
- $\tau_L = \frac{L_1}{R_1}, \frac{L_2}{R_2} = $ time constant of the line.
- $i_1 = $ Current from Bus 1 to fault.
- $i_2 = $ Current from Bus 2 to fault.

Fig. 1(b) shows the $s$ domain equivalent of the circuit of Fig. 1(a). $I_1(s)$ and $I_2(s)$ denote the $s$ domain equivalent of currents $i_1$ and $i_2$, respectively, and will be denoted simply as $I_1$ and $I_2$ during derivation. Applying KVL to the circuit in Fig. 1(b), we get

\begin{equation}
(s^2L_1 + s(R_1 + R_f))I_1 + sR_f I_2 = V_1 + sL_1 I_0
\end{equation}

\begin{equation}
sR_f I_1 + (s^2L_2 + s(R_2 + R_f))I_2 = V_2 - sL_2 I_0
\end{equation}

If (1) and (2) are solved for $I_1(s), I_2(s)$ and subsequent inverse Laplace transforms are performed to get $i_1(t)$ and $i_2(t)$, the following expressions are obtained:

\begin{equation}
i_1(t) = K_1 + K_3 e^{-(\lambda_L + \lambda_f)t}
\end{equation}

\begin{equation}
i_2(t) = K'_1 + K'_3 e^{-(\lambda_L + \lambda_f)t}
\end{equation}

where, $\lambda_L = \frac{1}{\tau_L} = \frac{1}{\frac{L_1}{R_1}}, \lambda_f = \frac{R_f}{L_f}, K_1, K_3, K'_1, K'_3$ are constants.

Step-wise derivation is provided in Appendix A submitted with this paper.
Dividing (7) by (6), (8) is obtained.

If \( v_1, i_1, \frac{di_1}{dt} \) can be measured at two different times \( t_1 \) and \( t_2 \), (11) and (12) can be formed.

\[
v_1(t_1) = x[l \cdot \frac{di_1(t_1)}{dt} + ri_1(t_1)] + R_f(m + 1)(i_1(t_1) - I_0) \quad (11)
\]

\[
v_1(t_2) = x[l \cdot \frac{di_1(t_2)}{dt} + ri_1(t_2)] + R_f(m + 1)(i_1(t_2) - I_0) \quad (12)
\]

From (11) and (12), the location of fault, \( x \), can be expressed as:

\[
x = \frac{|v_1(t_1) - i_1(t_1) - I_0|}{|v_1(t_2) - i_1(t_2) - I_0|} \quad (13)
\]

Notice that (13) provides a closed-form solution for fault location that does not include the fault resistance term \( R_f \). Samples of voltage and current at time \( t_1 \) and \( t_2 \) can be measured, and if the sampling rate is high enough (1 MHz assumed in this paper), current derivative \( \frac{di_1}{dt} \) can also be accurately calculated. Thus, (13) can be used to find fault location \( x \), regardless of the unknown fault resistance. This theoretical formulation is claimed to be the seminal contribution of this work. Three consecutive readings are needed, as two samples are needed to calculate \( \frac{di_1}{dt} \). This translates to a solution time of just 3 \( \mu s \).

When the fault current will start to settle down, i.e., \( \frac{di_1}{dt} \bigg|_{t=t_1} = \frac{di_1}{dt} \bigg|_{t=t_2} \approx 0 \) and \( i_1(t_1) \approx i_1(t_2) \). In that case, both equations will have the same information, and the solution will have the zero-determinant problem. So, it is important to use values during the transient state after a fault.

### III. VALIDATION OF THE PROPOSED THEORY

To validate the theory developed in section II, the circuit depicted in Fig. 1(a) is simulated in PSCAD with a sampling frequency of 1 MHz, meaning the sampled values are 1 \( \mu s \) apart. Rated system voltage is chosen to be 400 V, as it has been used in a number of papers for dc microgrids [18]–[21]. A 100 m long Yorkshire conductor [22] is chosen for the feeder. Circuit parameters are: \( r = 1.37 \, m \Omega / m, l = 0.25 \, \mu H / m, V_1 = 400 \, V, V_2 = 395 \, V, I_0 = 36.63 \, A \). Fault resistance is taken as \( R_f = 0.01 \, \Omega \) (low resistance) for this validation. Section V will show how the method can be extended to high-resistance faults.

Two faults are simulated at \( x^{(1)} = 80 \, m \) and \( x^{(2)} = 40 \, m \) distance from Bus 1. The fault inception time was set at \( t_0 = 0.1 \, s \) for both the cases. Currents from Bus 1 to fault (Bus1-fault) for both cases are plotted in Fig. 2.

For \( x^{(1)} = 80 \, m \) case, \( L_1^{(1)} = 20 \, \mu H, L_2^{(1)} = 5 \, \mu H, R_1^{(1)} = 109.6 \, m \Omega, R_2^{(1)} = 27.4 \, m \Omega \). So, \( L_1^{(1)} = L_2^{(1)} = 4 \, \mu H, \lambda_L = \frac{R}{L} = 5480 \, s^{-1} \) and \( \lambda_f = \frac{R_f}{L_0} = \frac{0.01 \, \Omega}{4 \, \mu H} = 2500 \, s^{-1} \).
To get the expression of current in form of (3), values of coefficients $K^{(1)}_1$ and $K^{(1)}_3$ are needed. A detailed calculation of the coefficients is provided in Appendix B. From the calculated values, current $i^{(1)}_1(t)$ is

$$i^{(1)}_1(t) = 2524.2843 - 2487.6497e^{-7980t}.$$

However, since the fault in the circuit was simulated at $t_0 = 0.1$ s, $i^{(1)}_1(t)$ will be

$$i^{(1)}_1(t) = 2524.2843 - 2487.6497e^{-7980(t-0.1)} \quad (14)$$

The calculated current using (14) is plotted in Fig. 2(a) as $i_{Bus1 \text{calc}}$. It is superimposed on the simulated current. Similarly, simulated and calculated currents for fault at $x^{(2)} = 40$ m are plotted in Fig. 2(b), which are also superimposed. This validates the theory of Section II-A.

To validate the method for fault location, measurements of three consecutive samples at three instances during the transient period after the fault initiation were made, and the fault distance was calculated using (11) and (12) for each set of samples. In each case, the current derivative at a specific time-instant (say, $t_2$) was calculated using measurement at that time instant and the previous measurement, i.e.,

$$\frac{di^{(1)}_1(t_2)}{dt} = \frac{i_1(t_2) - i_1(t_1)}{t_2 - t_1}. \quad (15)$$

Table 1 shows measured and calculated values at all three instances, for faults created at 80 m and 40 m from Bus 1. The calculated distance in each case is very close to the actual distance. The other variable being solved through (11) and (12) is $R_f(m + 1)$, which is of no interest to fault location. This result validates the closed-form deterministic theoretical formulation developed in Section II-B.

### IV. PERFORMANCE OF THE METHOD WITH NON-IDEAL SOURCES

When a fault occurs on a feeder-section in a dc microgrid, the current contributions from the dc link capacitors associated with converters dominate the fault current first [6], [23]. As capacitors resist rapid change in voltage, for a short period of time after fault the capacitor will act like a constant voltage dc source. Thus, measurements from this initial period can be used to determine the fault location modeled by (11) and (12). This section describes the converter models, and fault detection and location on a feeder fed by converters.

#### A. LV DC FEEDER DESCRIPTION

Fig. 3 shows a two-bus dc feeder with dc-dc boost converters connected to the end-buses instead of ideal voltage sources. Parameters of this test system are listed in Table 2. Feeder parameters are taken from [24] to match the ampacity of the 100 kW converter. As LVdc feeders are likely to be short in length, feeder capacitance was not considered in Section II-A while developing the theory. But in practical cases, every cable is associated with some capacitance. So the performance of the proposed method was verified with cable capacitance included in the simulation. Equivalent capacitance for the 100 m long cable was divided equally into two parts ($C_{cab}$ in Fig. 3), which were connected on each end of the feeder to form a pi-section. A commonly used unipolar microgrid topology with T(earth)N(neutral) grounding scheme [25] is chosen, where the grid is unipolar and the neutral is solidly grounded [19], [26]. The fault location device based on the proposed theory is placed on the positive pole [19].

The dc-dc boost converter model is taken from [27]. Converter parameters are chosen using typical values for a 100 kW converter, and verified through a number of resources [7], [20]. It is assumed that the converter has an ideal dc voltage source at its low voltage side, representing a PV panel or a battery. This is justified, since the inductor at the input side of the converter ($L_{cin}$) shown in Fig. 3, which
TABLE 2. Parameters of the test system.

| Network component/ parameter | Value       |
|------------------------------|-------------|
| Rated voltage                | 400 V       |
| Converter rating             | 100 kW      |
| Converter low voltage, $V_{in}$ | 200 V   |
| Switching frequency of converter | 20 kHz       |
| DC link capacitor, $C_f$     | 2 mF        |
| Converter inductor, $L_{conv}$ | 1 mH        |
| Cable resistance [33]        | 0.0991 mΩ/m |
| Cable inductance [33]        | 0.2929 μH/m |
| Cable capacitance [33]       | 1.44 nF/m   |
| Cable ampacity [33]          | 260 A       |
| Cable length                 | 100 m       |
| Load at Bus 2                | 100 kW      |

is placed to filter out the ripple in the input dc current [28], [29], will oppose any sudden change in current. Within the time frame of a few microseconds after fault inception when the method is applied, any rapid change in the input current is restricted by this inductor, and the voltage across the input source therefore remains constant. This was tested by replacing the ideal dc input source in Fig. 3 with a practical input source comprising of a battery in parallel with an input capacitor and the hypothesis was validated. The duty cycle is kept fixed, since the initial period after fault is governed by the natural response of an $RLC$ circuit [6], [18], [23], and the converter control would not activate during that time. Load current is 247 A, representing almost the full load in the system.

B. CURRENTS UNDER NORMAL LOADING AND FAULT CONDITIONS IN CONVERTER INTERFACED FEEDERS

Fig. 4 shows currents through diode ($i_{Bus1_{conv}-d}$), through capacitor ($i_{Bus1_{conv}-c}$), the summation of the two (total current $i_{Bus1_{conv}}$), and the output voltage of the converter ($v_{Bus1}$) for the converter connected to Bus 1 in Fig. 3. It can be seen that the output current and voltage are practically constant throughout the time. The capacitor current and the diode current change depending on the switching of the IGBT.

A fault was simulated in the dc feeder of Fig. 3 at 0.1 s with a fault resistance of $R_f = 0.01 \, \Omega$ at a distance $x = 80$ m from Bus 1. The simulation was run for 0.2 s. Fig. 5 shows the currents through different components under this fault condition - current through diode $i_{Bus1_{conv}-d}$, current through capacitor $i_{Bus1_{conv}-c}$, total current from Bus 1 to fault $i_{Bus1_{conv}}$.

The same circuit then was simulated replacing the converters on the two buses with ideal dc sources. The voltages of the dc sources were set at the prefault voltages of Bus 1 and Bus 2 of the dc feeder with converters. The current from Bus 1 to fault from the circuit with the ideal dc source was plotted in Fig. 5 in green ($i_{Bus_{1_{vs}}}$). Notice that total currents from Bus 1 to fault in both cases are practically equal to each other for much longer than 3 μs (equivalent to 3 samples here) after the fault initiation. Thus, (11) and (12) can also be applied to dc feeders fed by converters.

C. FAULT DETECTION AND FAULT LOCATION

Detecting a fault is necessary before applying the proposed method to locate it. This Section shows how (13) can be used for fault detection as well.

If voltage drop per unit length of line is denoted as $v_u(t)$, i.e., $v_u(t) = l * \frac{di_1(t)}{dt} + r * i_1(t)$, so (13) becomes

$$x = \begin{bmatrix} v_1(t_1) & i_1(t_1) - I_0 \\ v_1(t_2) & i_1(t_2) - I_0 \\ v_u(t_1) & i_1(t_1) - I_0 \\ v_u(t_2) & i_1(t_2) - I_0 \end{bmatrix}$$

Under normal loading condition, as seen in Fig. 4, the converter output voltage and current remain practically constant, i.e., $v_1(t_1) \approx v_1(t_2)$. Voltage drop across the unit length of
line can also be assumed constant, i.e., \( v_u(t_1) \approx v_u(t_2) \). So,

\[
x \approx \frac{v_1(t_1) - i_1(t_1) - I_0}{v_u(t_1) - i_1(t_1) - I_0} \Rightarrow x \approx \frac{v_1(t_1) \ast (i_1(t_2) - i_1(t_1))}{v_u(t_1) \ast (i_1(t_2) - i_1(t_1))} \Rightarrow x \approx \frac{v_1(t_1)}{v_u(t_1)}
\]

But \( v_1(t) = L_{line} \ast v_u(t) + v_2(t) \), where \( L_{line} \) is the length of the line. So,

\[
x \approx \frac{L_{line} \ast v_u(t_1) + v_2(t_1)}{v_u(t_1)} \Rightarrow x \approx L_{line} + \frac{v_2(t_1)}{v_u(t_1)}
\]

Equation (17) implies that under normal operation the calculated length of fault point from Bus 1 will be larger than the line length. In case of Bus 2, the current in the line is flowing towards the bus. As a result, from the perspective of Bus 2, both, the measured current \( i_2(t) \) and the voltage drop per unit length of line, \( v_u(t) \), are negative. So, from (16), \( x \) becomes a negative number under normal operating condition. Thus, under un-faulted condition, the distance measured will be either greater than the line length or negative. This can be used to distinguish prefault condition from fault condition, and hence detect a fault. Note that the prefault current has to be used with care in this approach. Since the load current can change over time, the prefault current should be updated with every new sample if no fault is detected. But, once a fault is detected, the prefault current should be fixed at its latest updated value during the fault location process. Fig. 6 shows the flowchart of the proposed fault detection and location.

**D. RESULTS**

To evaluate the performance of the algorithm developed in Section IV-C, data were generated from the fault simulation described in Section IV-B with sampling frequency of 1 MHz. To implement the flowchart of Fig. 6, a moving window consisting of three samples was run through the accumulated data from the simulation to calculate the fault distance before and after the fault initiation. Fig. 7 shows the calculated distance of fault from Bus 1 (\( dist_{Bus1} \)) and Bus 2 (\( dist_{Bus2} \)) from 10 \( \mu s \) before fault inception to 10 \( \mu s \) after fault inception. Clearly, before fault inception the distance from Bus 1 is much larger than the line length, and distance from Bus 2 is negative, as discussed in Section IV-C. Within 3 samples after the fault inception (at \( t_0 = 0.1 \) s), calculated distances become almost equal to the actual distances of the fault point on the line. Thus, both detection and location of fault are correctly and accurately performed simultaneously in 3 \( \mu s \) after inception of fault.

The accumulated data spanned from 40 \( \mu s \) before the fault inception to 80 \( \mu s \) after. From the 3\textsuperscript{rd} sample after the fault inception time to the end of accumulated data, the calculated distances from Bus 1 varied from 79.8 m to 81.4 m. So, the proposed method provides accurate fault location over an extended range of data points after fault.

**E. A SPECIAL CASE**

Clearly, the derivation of theory assumes dc sources present at both ends of the feeder. Since most of the dc loads and all nonideal sources connect through converters, this is a reasonable assumption. A dc bus with only purely resistive load is therefore a rare case. However, it should be mentioned that under this unlikely scenario, one of the sources in Fig. 1 (a), say, \( V_2 \), will be replaced by a load resistance. This will drastically alter the nature of the current \( i_2(t) \) during fault, and the value of \( m \) in (8) will no longer be constant. This means the two foundational equations (11) & (12) that require \( m \) to be a constant will no longer be valid, and the method will therefore fail.

It is important to mention here that the dc feeder analyzed here would typically be a part of a dc microgrid. This special case can occur only if such microgrid is single-sourced and there is no converter based load in the microgrid. This is contrary to the vary nature of microgrids, and therefore this special case would be rare in practice.

**V. USING THE METHOD FOR HIGH RESISTANCE FAULTS**

In order to use the method for high resistance faults, the impact of higher fault resistance on the fault-induced transient needs to be understood. From (3), fault current in a feeder fed by an ideal source is

\[
i_1(t) = K_1 + K_3 \ast e^{-\left(\frac{R_f + R_l}{2}ight)t} \Rightarrow i_1(t) = K_1 + K_3 \ast e^{-\left(\frac{R_f + R_l}{2}ight)t} \Rightarrow i_1(t) = K_1 + K_3 \ast e^{-\left(\frac{R_f + R_l}{2}ight)t}
\]

\[
(18)
\]
where, $\tau_T$ is the equivalent time constant, and

$$\frac{1}{\tau_T} = \frac{1}{\tau_L} + \frac{1}{\tau_f} \quad (19)$$

Also, $\tau_L = L/R =$ time constant of line, and $\tau_f = \frac{L_p}{R_f} =$ time constant of fault.

From (19), $\tau_T$ is smaller than both $\tau_L$ and $\tau_f$. The smaller the value of $\tau_T$, shorter the time the transient will last. Therefore, as the value of $R_f$ increases, the transient period will be shorter. Fig. 8 shows simulated currents from the circuit of Fig. 1(a), with varying fault resistances to verify this argument. In addition, the shorter transient also gets steeper, increasing the chances of erroneous calculation of $\frac{di}{dt}$. Therefore, to accurately determine location with high resistance faults, sampling frequency needs to be increased, so the required samples with adequate sampling rate for accurate calculation of $\frac{di}{dt}$ can be obtained before the transient subsides.

A fault is simulated in the system described in Section IV-A with $R_f = 2 \ \Omega$, at fault inception time $t_0 = 0.1 \ \text{s}$, at a distance of 80 m from Bus 1. From the manufacturer’s data-sheet of the chosen 185 sqmm conductor [24], $\tau_L \approx 2955.6 \ \mu\text{s}$ and $\tau_f \approx 2.3432 \ \mu\text{s}$. According to (19), $\tau_T \approx 2.34 \ \mu\text{s}$. According to [31], the transient will settle down approximately within $5\tau_T \approx 11.71 \ \mu\text{s}$ after the fault inception. Current plot in Fig. 9(a) from the simulation supports the argument.

Observe from the voltage plot of Fig. 9(b) that the change in the capacitor voltage before the current settles to steady state is less than 0.82% of the initial voltage. This phenomenon is characteristic of high resistance faults. Because of low fault currents and fast transients, capacitors do not loose much charge, and voltage remains practically constant. Thus, the proposed theory, developed with ideal voltage sources, can be used to determine fault location for high resistance faults.

Fig. 9(c) shows the plot of the calculated distance to the fault point from Bus 1 for this high resistance fault simulated at 1 MHz sampling rate. With this sampling rate, it is expected that the method will provide fault location for up to approximately 10 samples after fault inception. Fig. 9(c) shows that the method provides rational (though incorrect)
answers for approximately 15 µs after fault inception. Then, the calculations are affected due to the determinant in (13) getting close to zero in steady state. Clearly, there is a significant error in fault location. This is because errors are introduced in the calculation of \( \frac{di}{dt} \) due to the much steeper exponential transient. To minimize this error, a higher sampling frequency is required. Table 4 confirms this rationale. Conversely, it can be argued that lower sampling rates would suffice for faults with low fault resistances. In the fault simulation case with \( R_f = 0.01 \) Ω in Section IV-B, data were sampled at 1 MHz frequency. The same circuit was simulated and sampled at lower frequencies and the proposed algorithm was implemented for the same amount of time to check the performance of this method at lower frequencies. Table 5 shows the results. Data points from lower sampling frequency cases result in higher error, but even with 100 kHz sampling frequency, the error is less than 5%.

To further investigate the performance of the method for high resistance faults, faults with resistances ranging from 0.01 Ω to 100 Ω were simulated. Table 3 lists the sampling frequencies required to get the fault location error within ±1.5%. These results illustrate that as long as the sampling frequency is adequate, the proposed method provides accurate results, regardless of fault resistance. The state-of-the-art oscilloscopes have probes that can sample up to 100 GHz [17], which would enable the method to work for higher fault resistance values as well.

VI. SENSITIVITY ANALYSIS

A. FAULT DISTANCE

As \( \tau_f = \frac{L_p}{R_f} = \frac{L_1}{R_f}||L_2}{R_f} \), the less \( L_1 \) or \( L_2 \) will be, the less \( L_p \) will become, which will eventually result in lower \( \tau_f \). So, if the fault is very close to or very far from the bus, \( \tau_f \) will be smaller, and according to the trend seen in Section V, errors will be higher, potentially requiring higher sampling frequency. To examine the sensitivity of the method to fault-distance, several simulations were performed with varying fault distances and \( R_f = 0.01 \) Ω in the system of Fig. 3. Then sampling frequency was varied to examine the impact on the location error. Results are tabulated in Table 6. The results support the argument. Notice that with 1 MHz sampling frequency the error is quite low for all fault locations, showing low sensitivity to fault distance. So, there may not be any need to change the assumed sampling frequency.

B. DC LINK CAPACITOR SIZE

The proposed fault location method is accurate because the dc link capacitor behaves like an ideal dc source for a short duration after the initiation of a fault. But the time duration for which the response of the capacitor can be treated as the response of an ideal dc source is dependent on the size of the capacitor. Given the fault resistance, line parameters, and fault distance is fixed, this duration gets larger if the capacitor size (in Farad) gets larger. With the advancement in power electronics and high-speed switching devices, the

| \( R_f, \) \( \Omega \) | Sampling Frequency | Percentage error achieved at corresponding sampling frequency |
|-----------------|-----------------|--------------------------------------------------|
| 0.01            | 100 kHz         | -1.29%                                           |
| 0.1             | 1000 kHz (1 MHz)| -1.09%                                           |
| 1               | 10 MHz          | -1.05%                                           |
| 10              | 100 MHz         | -0.9%                                            |
| 100             | 1000 MHz        | 0.93%                                            |

| Sampling frequency | Fault location error |
|--------------------|----------------------|
| 1 MHz              | -20.67%              |
| 2 MHz              | -10.60%              |
| 5 MHz              | -4.27%               |
| 8 MHz              | -2.67%               |
| 10 MHz             | -2.14%               |

| Sampling frequency | Fault location error |
|--------------------|----------------------|
| 1 MHz              | -0.18%               |
| 666.67 kHz         | -0.26%               |
| 500 kHz            | -0.32%               |
| 200 kHz            | -0.71%               |
| 100 kHz            | -1.29%               |

| Fault Distance | % Error with increasing sampling freq. | 1 MHz | 5 MHz | 10 MHz |
|---------------|--------------------------------------|-------|-------|--------|
| 5%            | -0.160%                              | -0.050%| -0.060%|
| 20%           | -0.132%                              | -0.016%| -0.010%|
| 50%           | -0.094%                              | -0.016%| -0.006%|
| 80%           | -0.180%                              | -0.024%| -0.010%|
| 95%           | -0.377%                              | -0.074%| -0.035%|
TABLE 7. Performance of the proposed method with varying dc link capacitor size.

| Capacitor Size ($\mu F$) | Switching Freq. (kHz) | $R_f = 0.1 \Omega$ | $R_f = 0.01 \Omega$ |
|-------------------------|-----------------------|---------------------|---------------------|
| 781.25                  | 20                    | -1.400%             | -0.147%             |
| 156.25                  | 100                   | -0.494%             | -0.243%             |

VIII. POTENTIAL FOR FURTHER RESEARCH

This paper reports the discovery of the mathematical foundations and implementation of a fast fault location method for a dc feeder that is independent of the topology of the system built around the feeder. This opens the doors for a communication-free topology-independent protection scheme for an entire dc microgrid. Such a scheme could use the method as a time-domain distance relay, placed on each side of every feeder of a dc microgrid. However, the backup protection in such a scheme requires further research. Another avenue of research would be investigating and adapting the performance of the method for different grounding schemes in a dc microgrid. Research can be performed to include feeder capacitance in the formulation to adapt the method for HVDC lines fed by voltage source converters (VSCs). An arcing model for HIF faults is another worthy research pursuit.

REFERENCES

[1] H. Kakigano, Y. Miura, and T. Ise, “Low-voltage bipolar-type DC microgrid for super high quality distribution,” IEEE Trans. Power Electron., vol. 25, no. 12, pp. 3066–3075, Dec. 2010.
[2] L. Kong, H. Nian, Q. Huang, Z. Zhang, J. Xu, and K. Dai, “Optimization of current breaker and fault current limiter in DC micro-grid based on faulty transient analysis,” in Proc. 21st Int. Conf. Electr. Mach. Syst. (ICEMS), Oct. 2018, pp. 2017–2022.
[3] A. Meghwani, S. C. Srivastava, and S. Chakrabarti, “Local measurement-based technique for estimating fault location in multi-source DC micro-grids,” IET Gener. Transmiss. Distrib., vol. 12, no. 13, pp. 3305–3313, Jul. 2018.
[4] R. Bhargav, B. R. Bhalja, and C. P. Gupta, “Novel fault detection and localization algorithm for low-voltage DC microgrid,” IEEE Trans. Ind. Informat., vol. 16, no. 7, pp. 4498–4511, Jul. 2020.
[5] A. Meghwani, S. C. Srivastava, and S. Chakrabarti, “A new protection scheme for DC microgrid using line current derivative,” in Proc. IEEE Power Energy Soc. Gen. Meeting, Jul. 2015, pp. 1–5.
[6] A. Meghwani, S. C. Srivastava, and S. Chakrabarti, “A non-unit protection scheme for DC microgrid based on local measurements,” IEEE Trans. Power Del., vol. 32, no. 1, pp. 172–181, Feb. 2017.
[7] A. Meghwani, S. Chakrabarti, and S. C. Srivastava, “An on-line fault location technique for DC microgrid using transient measurements,” in Proc. 7th Int. Conf. Power Syst. (ICPS), Dec. 2017, pp. 386–391.
[8] X. Feng, L. Qi, and J. Pan, “A novel fault location method and algorithm for DC distribution protection,” IEEE Trans. Ind. Appl., vol. 53, no. 3, pp. 1834–1840, May/Jul. 2017.
[9] J. E. Hill, S. D. Fletcher, P. J. Norman, and S. J. Galloway, “Protection system for an electrical power network,” U.S. Patent 8 842 401, Sep. 23, 2014.
[10] R. Mohanty, U. S. M. Balaji, and A. K. Pradhan, “An accurate noniterative fault-location technique for low-voltage DC microgrid,” IEEE Trans. Power Del., vol. 31, no. 2, pp. 475–481, Apr. 2016.
[11] J.-D. Park, “Fault detection, isolation, location and reconnection systems and methods,” U.S. Patent 9 007 735, Apr. 14, 2015.
[12] A. K. Pradhan and R. Mohanty, “Cable fault location in a DC microgrid using current injection technique,” in Proc. Nat. Power Syst. Conf. (NPSC), Dec. 2016, pp. 1–6.
[13] S. Azimi, M. Sanaye-Pasand, M. Abedini, and A. Hasani, “A traveling-wave-based methodology for wide-area fault location in multimodal DC systems,” IEEE Trans. Power Del., vol. 29, no. 6, pp. 2552–2560, Dec. 2014.
[14] S. Beheshtaein, R. M. Cuzner, M. Forouzesh, M. Savaghebi, and J. M. Guerrero, “DC microgrid protection: A comprehensive review,” IEEE J. Emerg. Sel. Topics Power Electron., early access, Mar. 12, 2019, doi: 10.1109/JESTPE.2019.2904588.
[15] Q. Yang, J. Li, S. L. Blond, and C. Wang, “Artificial neural network based fault detection and fault location in the DC microgrid,” Energy Proced., vol. 103, pp. 129–134, Dec. 2016. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1876610216314710
[16] SEL. SEL-T400L Time-Domain Line Protection. Accessed: Feb. 14, 2021. [Online]. Available: https://cms-cdn.selinc.com/assets/Literature/Product%20Literature/Data%20Sheets/T400L_DS_20190430.pdf?v=20190508-132112

[17] Tektronix. Digital and Mixed Signal Oscilloscopes. Accessed: Jan. 28, 2021. [Online]. Available: https://www.tek.com/datasheet/digital-and-mixed-signal-oscilloscopes

[18] S. D. A. Fletcher, P. J. Norman, S. J. Galloway, P. Crolla, and G. M. Burt, “Optimizing the roles of unit and non-unit protection methods within DC microgrids,” IEEE Trans. Smart Grid, vol. 3, no. 4, pp. 2079–2087, Dec. 2012.

[19] M. Mobarrad, D. Fregosi, S. Bhattacharya, and M. A. Bahmani, “Grounding architectures for enabling ground fault ride-through capability in DC microgrids,” in Proc. IEEE 2nd Int. Conf. DC Microgrids (iDCM), Jun. 2017, pp. 81–87.

[20] D. Salomonsson, L. Söder, and A. Sannino, “Protection of low-voltage DC microgrids,” IEEE Trans. Power Del., vol. 24, no. 3, pp. 1045–1053, Jul. 2009.

[21] Y. O. Reddy, S. Chatterjee, and M. A. Bhowmik, “Fault detection and location estimation for LVDC microgrid using self-parametric measurements,” Int. Trans. Electr. Energy Syst., vol. 30, no. 9, Sep. 2020, Art. no. e12499. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/2050-7038.12499

[22] Nexans Energy. Service Cable Products. Accessed: Feb. 3, 2020. [Online]. Available: https://drive.google.com/file/d/1qBrt1anpjklmp73ah1YUGgg5kBVu2_BP/view?usp=sharing

[23] A. Ukil, Y. M. Yeap, and K. Satpathi, Fault Analysis and Protection System Design for DC Grids, 1st ed. Singapore: Springer, 2020.

[24] HAVELLS. LT/HT Power & Control Cables. Accessed: Jun. 5, 2021. [Online]. Available: https://www.havells.com/content/dam/havells/brochures/Industrial%20Cable/Cable%20Catalogue-2016.pdf

[25] S. Augustine, J. E. Quiroz, M. J. Reno, and S. Brahma, “DC microgrid protection: Review and challenges,” Sandia Nat. Lab., Albuquerque, NM, USA, Tech. Rep. SAND2018-8853, Aug. 2018.

[26] T. R. de Oliveira, A. S. Bolzon, and P. F. Donoso-Garcia, “Grounding and safety considerations for residential DC microgrids,” in Proc. 40th Annu. Conf. IEEE Ind. Electron. Soc. (IECON), Oct. 2014, pp. 5526–5532.

[27] G. M. Masters, Renewable and Efficient Electric Power Systems, 2nd ed. Hoboken, NJ, USA: Wiley, 2013, ch. 9, sec. 9.2, p. 217.

[28] B. Hauke. “Basic calculation of a boost converter’s power stage,” Texas Instrum., Dallas, TX, USA, Tech. Rep. SLVA372C, Nov. 2009. [Online]. Available: https://www.ti.com/lit/an/slva372c/slva372c.pdf?ts=1652440495717

[29] R. W. Erickson and D. Maksimovic, Fundamentals of Power Electronics, 3rd ed. Cham, Switzerland: Springer, 2020.

[30] High Impedance Fault Detection Technology, PSRC Working Group D15. Accessed: Aug. 23, 2020. [Online]. Available: https://www.pes-psrc.org/kb/published/reports/High_Impedance_Fault_Detection_Technology.pdf

[31] J. W. Nilsson and S. A. Riedel. Electric Circuits, 9th ed. Upper Saddle River, NJ, USA: Prentice-Hall, 2011, ch. 7, sec. 7.1, p. 217.

[32] S. Gautam and S. M. Brahma, “Detection of high impedance fault in power distribution systems using mathematical morphology,” IEEE Trans. Power Syst., vol. 28, no. 2, pp. 1226–1234, May 2013.

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* * *
APPENDIX A
Detailed Proof of Fault Current Expression in DC Microgrids With Ideal Voltage Sources

Applying KVL in loop 1 of Fig. 1b, the following can be obtained

\[-V_1/s - L_1I_0 + (s \ast L_1 + R_1)I_1 + R_f(I_1 + I_2) = 0\]
\[(sL_1 + R_1 + R_f)I_1 + R_fI_2 = V_1/s + L_1I_0\]
\[(s^2L_1 + s(R_1 + R_f))I_1 + sR_fI_2 = V_1 + sL_1I_0\]  

(1)

Similarly in loop 2,

\[-V_2/s + L_2I_0 + (sL_2 + R_f)I_2 + R_f(I_2 + I_1) = 0\]
\[R_fI_1 + (sL_2 + R_2 + R_f)I_2 = V_2/s - L_2I_0\]
\[sR_fI_1 + (s^2L_2 + s(R_2 + R_f))I_2 = V_2 - sL_2I_0\]  

(2)

From (1) and (2) we can get

\[I_1 = \frac{\Delta_1}{\Delta}; I_2 = \frac{\Delta_2}{\Delta}\]  

(A.1)

where,

\[\Delta = \begin{vmatrix}
V_1 + sL_1I_0 & sR_f \\ V_2 - sL_2I_0 & s^2L_2 + s(R_2 + R_f)
\end{vmatrix}\]
\[\Delta = s^2[(sL_1 + R_1 + R_f)(sL_2 + R_2 + R_f) - R_f^2]
\[\Delta = s^2[s^2L_1L_2 + s \ast (L_1(R_2 + R_f) + L_2(R_1 + R_f)) + (R_1 + R_f)(R_2 + R_f) - R_f^2]
\[\Delta = s^2[s^2L_1L_2 + s \ast (L_1(R_2 + R_f) + L_2(R_1 + R_f) + R_1R_2 + R_1R_f + R_2R_f)]\]  

(A.2)

and,

\[\Delta_1 = \begin{vmatrix}
V_1 + sL_1I_0 & sR_f \\ V_2 - sL_2I_0 & s^2L_2 + s(R_2 + R_f)
\end{vmatrix}\]
\[\Delta_1 = s[(V_1 + sL_1I_0)(sL_2 + (R_2 + R_f)) - R_f(V_2 - sL_2I_0)]\]  

(A.3)

and,

\[\Delta_2 = \begin{vmatrix}
V_1 + sL_1I_0 & sR_f \\ V_2 - sL_2I_0 & s^2L_2 + s(R_2 + R_f)
\end{vmatrix}\]
\[\Delta_2 = s[(V_2 - sL_2I_0)(sL_1 + (R_1 + R_f)) - R_f(V_1 + sL_1I_0)]\]  

(A.4)

Putting the values of \(\Delta_1\) and \(\Delta\) in (A.1), \(I_1\) can be expressed as

\[I_1 = \frac{(V_1 + sL_1I_0)(sL_2 + (R_2 + R_f)) - R_f(V_2 - sL_2I_0)}{(V_1 + sL_1I_0)(sL_2 + (R_2 + R_f)) - R_f(V_2 - sL_2I_0) + (L_1L_2) \ast s\left[\frac{(L_1(R_2 + R_f) + L_2(R_1 + R_f))}{L_1L_2} + R_1R_2 + R_1R_f + R_2R_f\right]}\]  

(A.5)

Let’s say the denominator of (A.5) is \((L_1L_2) \ast s(as^2 + bs + c)\) where

\[a = 1\]
\[b = \frac{L_1(R_2 + R_f) + L_2(R_1 + R_f)}{L_1L_2}\]
\[c = \frac{R_1R_2 + R_1R_f + R_2R_f}{L_1L_2}\]  

(A.6)

Roots of \(as^2 + bs + c = 0\) are

\[r_1, r_2 = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}\]
\[r_1, r_2 = 1/2 \ast (-b/a \pm \sqrt{(b/a)^2 - 4(c/a)})\]  

(A.7)
Now,

\[
\begin{align*}
\frac{b}{a} &= \frac{L_1(R_2 + R_f) + L_2(R_1 + R_f)}{L_1L_2} \\
\frac{b}{a} &= \frac{R_2 + R_f}{L_2} + \frac{R_1 + R_f}{L_1} \\
\frac{b}{a} &= \frac{R_2}{L_2} + \frac{R_f}{L_2} + \frac{R_1}{L_1} + \frac{R_f}{L_1} \\
\frac{b}{a} &= \frac{R_1}{L_1} + \frac{R_2}{L_2} + \frac{R_f}{(\frac{1}{L_1} + \frac{1}{L_2})} \\
\frac{b}{a} &= \frac{R_1}{L_1} + \frac{R_2}{L_2} + \frac{R_f}{L_p}
\end{align*}
\]  

(A.8)

where, \( \frac{1}{L_p} = \frac{1}{L_1} + \frac{1}{L_2} \), parallel equivalent inductance of \( L_1, L_2 \).

But, \( \frac{R_1}{L_1} = \frac{R_2}{L_2} = \frac{1}{\tau_L} = \lambda_L \), where \( \tau_L \) = time constant of line.

Let’s say \( \lambda_f = \frac{1}{\tau_f} = R_f / L_p \)

So, from (A.8),

\[
\frac{b}{a} = \lambda_L + \lambda_L + \lambda_f \\
\frac{b}{a} = 2\lambda_L + \lambda_f
\]  

(A.9)

Now,

\[
\begin{align*}
4\left(\frac{c}{a}\right) &= 4 \ast \left( \frac{R_1R_2 + R_1R_f + R_2R_f}{L_1L_2} \right) \\
4\left(\frac{c}{a}\right) &= 4 \ast \left[ \frac{R_1R_2}{L_1L_2} + \frac{(R_1 + R_2)R_f}{L_1L_2} \right] \\
4\left(\frac{c}{a}\right) &= 4 \ast \left[ \lambda_L^2 + \frac{(R_1 + R_2)R_f}{L_1L_2} \right] \\
4\left(\frac{c}{a}\right) &= 4 \ast \left[ \lambda_L^2 + \frac{R_f}{LL_p} \right] \\
4\left(\frac{c}{a}\right) &= 4 \ast \left[ \lambda_L^2 + \lambda_L \lambda_f \right]
\end{align*}
\]  

(A.10)

Now,

\[
\sqrt{\left(\frac{b}{a}\right)^2 - 4\left(\frac{c}{a}\right)} = \sqrt{(2\lambda_L + \lambda_f)^2 - 4[\lambda_L^2 + \lambda_L \lambda_f]} \\
= \sqrt{4\lambda_L^2 + 4\lambda_L \lambda_f + \lambda_f^2 - 4\lambda_L^2 - 4\lambda_L \lambda_f} \\
= \sqrt{\lambda_f^2} \\
= \lambda_f
\]  

(A.11)

Now, roots from (A.7)

\[
\begin{align*}
r_1, r_2 &= \frac{1}{2} \ast [-(2\lambda_L + \lambda_f) \pm \lambda_f] \\
r_1 &= -\lambda_L; \quad r_2 = -(\lambda_L + \lambda_f)
\end{align*}
\]  

(A.12)

If (A.5) is expanded through partial fraction expansion and subsequent inverse Laplace transform is done on that, the current expressions will get the following forms.

\[
I_1(s) = \frac{K_1}{s - 0} + \frac{K_2}{s - r_1} + \frac{K_3}{s - r_2}
\]  

(A.13)

and,

\[
i_1(t) = K_1 + K_2 \ast e^{-\lambda_L t} + K_3 \ast e^{-(\lambda_L + \lambda_f) t}
\]  

(A.14)
It can be shown that, in (A.14) the coefficient \( K_2 = 0 \). The coefficient \( K_2 \) will be

\[
K_2 = (s + \lambda_L)I_1(s) \bigg|_{s = -\lambda_L} \]

\[
K_2 = (s + \lambda_L) \frac{(V_1 + sL_1 I_0)(sL_2 + (R_2 + R_f)) - R_f(V_2 - sL_2 I_0)}{s(L_1 L_2)s^2 + (L_1(R_2 + R_f) + L_2(R_1 + R_f)s + (R_1 R_2 + R_1 R_f + R_2 R_f))} \bigg|_{s = -\lambda_L}
\]

\[
K_2 = (s + \lambda_L) \frac{(V_1 + sL_1 I_0)(sL_2 + (R_2 + R_f)) - R_f(V_2 - sL_2 I_0)}{(L_1 L_2) * s(s + \lambda_L)(s + \lambda_L + \lambda_f)} \bigg|_{s = -\lambda_L}
\]

(A.15)

Numerator of (A.15) can be reorganized as follows

\[
= (V_1 + sL_1 I_0)(sL_2 + (R_2 + R_f)) - R_f(V_2 - sL_2 I_0)
\]

\[
= sL_2 V_1 + V_1 R_2 + V_1 R_f + s^2 L_1 L_2 I_0 + sL_1 R_2 I_0 + sL_1 R_f I_0 - R_f V_2 + sL_2 R_f I_0
\]

\[
= s^2 L_1 L_2 I_0 + sL_2 V_1 + L_1 R_2 I_0 + L_1 R_f I_0 + L_2 R_f I_0 + V_1 R_2 + R_f(V_1 - V_2)
\]

\[
= s^2 L_1 L_2 I_0 + sL_2 V_1 + sL_1 R_2 I_0 + L_2 R_f I_0 + V_1 R_2 + R_f(V_1 - V_2)
\]

\[
= s^2 L_1 L_2 I_0 + sL_2 V_1 + sL_1 R_2 I_0 + sL_2 R_f I_0 + V_1 R_2 + R_f(V_1 - V_2)
\]

(A.16)

From the prefault circuit \( I_0 = (V_1 - V_2)/R \), so the numerator comes

\[
= s^2 L_1 L_2 \left( \frac{V_1 - V_2}{R} \right) + sL_2 V_1 + sL_1 R_2 \left( \frac{V_1 - V_2}{R} \right) + sL_2 R_f \left( \frac{V_1 - V_2}{R} \right) + V_1 R_2 + R_f(V_1 - V_2)
\]

(A.17)

When evaluated at \( s = -\lambda_L \), the numerator becomes

\[
= (-\lambda_L) L^2 \left( \frac{V_1 - V_2}{R} \right) + (-\lambda_L) L^2 V_1 + (-\lambda_L) L^2 R_2 \left( \frac{V_1 - V_2}{R} \right) + (-\lambda_L) L R_f \left( \frac{V_1 - V_2}{R} \right) + V_1 R_2 + R_f(V_1 - V_2)
\]

\[
= \frac{RL}{L} \left( \frac{V_1 - V_2}{R} \right) - \frac{RL}{L} V_1 - \frac{L_1 R_2}{L} (V_1 - V_2) - R_f(V_1 - V_2) + V_1 R_2 + R_f(V_1 - V_2)
\]

\[
= \frac{RL}{L} \left( \frac{V_1 - V_2}{R} \right) - \frac{L_1 R_2}{L} (V_1 - V_2) + V_1 R_2 - \frac{RL}{L} V_1
\]

But from line parameter, \( R_2/L_2 = R/L \), i.e., \( R_2 = RL_2/L \). So the numerator becomes

\[
= \frac{L_1}{L} \left( \frac{RL}{L} - R_2 \right)(V_1 - V_2) + (R_2 - \frac{RL}{L}) V_1
\]

\[
= \frac{L_1}{L} (R_2 - R_2)(V_1 - V_2) + (R_2 - R_2)V_1
\]

\[
= 0
\]

(A.19)

This means coefficient \( K_2 = 0 \) and eventually current \( i_1(t) \) reduces to

\[
i_1(t) = K_1 + K_3 e^{-(\lambda_L + \lambda_f)t}
\]

(3)

So the current \( i_1(t) \) can be represented through one exponent. In a similar fashion, expression for \( i_2(t) \) can be derived and written as

\[
i_2(t) = K_1' + K_3' e^{-(\lambda_L + \lambda_f)t}
\]

(4)
APPENDIX B
CALCULATION OF COEFFICIENTS

In this section, coefficients $K_1$ and $K_3$ are calculated for section III using the relevant data. From (A.13)

$$K_1 = s \cdot I_1 \bigg|_{s=0}$$

$$K_1 = s \* \frac{(V_1 + sL_1I_0)(sL_2 + (R_2 + R_f)) - R_f(V_2 - sL_2I_0)}{s[(L_1L_2)s^2 + (L_1(R_2 + R_f) + L_2(R_1 + R_f))s + (R_1R_2 + R_1R_f + R_2R_f)]} \bigg|_{s=0}$$

$$K_1 = \frac{V_1(R_2 + R_f) - R_fV_2}{R_1R_2 + R_1R_f + R_2R_f}$$

$$K_1 = 2524.2843$$

Similarly

$$K_3 = (s + \lambda_L + \lambda_f) \* I_1 \bigg|_{s=-(\lambda_L+\lambda_f)}$$

$$K_3 = (s + \lambda_L + \lambda_f) \* \frac{(V_1 + sL_1I_0)(sL_2 + (R_2 + R_f)) - R_f(V_2 - sL_2I_0)}{(L_1L_2) * s(s + \lambda_L)(s + \lambda_L + \lambda_f)} \bigg|_{s=-(\lambda_L+\lambda_f)}$$

$$K_3 = \frac{(V_1 + sL_1I_0)(sL_2 + (R_2 + R_f)) - R_f(V_2 - sL_2I_0)}{(L_1L_2) * s(s + \lambda_L)} \bigg|_{s=-(\lambda_L+\lambda_f)}$$

$$K_3 = -2487.6497$$