Dynamic Write-Voltage Design and Read-Voltage Optimization for MLC NAND Flash Memory

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Abstract: To mitigate the impact of noise and interference on multi-level-cell (MLC) flash memory with the use of low-density parity-check (LDPC) codes, we propose a dynamic write-voltage design scheme considering the asymmetric property of raw bit error rate (RBER), which can obtain the optimal write voltage by minimizing a cost function. In order to further improve the decoding performance of flash memory, we put forward a low-complexity entropy-based read-voltage optimization scheme, which derives the read voltages by searching for the optimal entropy value via a log-likelihood ratio (LLR)-aware cost function. Simulation results demonstrate the superiority of our proposed dynamic write-voltage design scheme and read-voltage optimization scheme with respect to the existing counterparts.

Keywords: error correction coding; multi-level-cell (MLC); NAND flash memory; read voltage; write voltage

I. INTRODUCTION

As a non-volatile memory (NVM) device, NAND flash memory has attracted extensive attention from both academia and industry due to the advantages of high capacity and low power consumption. Solid state disk (SSD) based on NAND flash memory has gradually replaced traditional storage devices and been widely used in various scenarios (e.g., mobile intelligent devices). With the era of Internet of Things (IoT), the generation of a large amount of data has brought great challenges to the capacity and reliability of storage devices. To address the above issue, a great deal of research effort has been devoted to boosting the storage capacity and reliability of flash memory. For single-level-cell (SLC) flash memory, each cell stores one bit. With the emergence of multi-level-cell (MLC), triple-level-cell (TLC), quadruple-level-cell (QLC) and three-dimensional (3D) flash memory [1], the capacity of flash memory has been significantly increased. In MLC flash memory, each cell stores one bit. With the emergence of multi-level-cell (MLC), triple-level-cell (TLC), quadruple-level-cell (QLC) and three-dimensional (3D) flash memory [1], the capacity of flash memory has been significantly increased. In MLC flash memory, each cell stores two bits, which are represented as \{11, 10, 00, 01\}. The bit on the left is called the most significant bit (MSB), while the bit on the right is called the least significant bit (LSB). However, the increase of storage capacity and the decrease of processing size make the flash memory suffer from more serious noises and interferences, mainly including programming noise, random telegraph noise (RTN), data retention noise and cell-to-cell interference (CCI) [2]. These noises and interferences greatly reduce the storage reliability of flash memory.

To enhance the robustness against noise and interference, error-correction-coding (ECC) technology is applied to MLC flash memory. For example, Bose-Chaudhuri-Hocquenghem (BCH) codes have been adopted as the ECC scheme for flash memory in [3].
However, the BCH codes are more suitable for short-codeword-length scenario, which is extremely difficult to meet the error-correction requirements of flash memory. Thereby, low-density parity-check (LDPC) codes [4, 5] have been widely studied in flash memory because of its low implementation complexity and strong error-correction ability, especially in the long-codeword-length scenario. Moreover, due to the influence of channel-asymmetric noise, the probability distribution functions (PDFs) of the four voltages in MLC flash memory continue changing over different program-and-erase (PE) cycles and retention time. Consequently, it is necessary to update the write voltage and optimize the read voltage for adapting to the variation of flash memory channel.

1.1 Literature and Motivation

To attenuate the asymmetric noise errors of flash memory, some techniques have been presented to optimize write voltage and read voltage. In [6], the authors have proposed a write-voltage optimization scheme, which only considers the RTN noise in the flash memory channel. Furthermore, another scheme has been proposed in [7] to optimize the write voltage by modeling the flash memory channel as an additive white Gaussian noise (AWGN) channel. However, these techniques are not precise and suitable for flash memory channel, because the practical NAND flash memory contains various non-stationary noises such as the programming noise, RTN, data retention noise and the CCI. These noises and interferences have different characteristics and vary continuously with the PE cycles and the retention time.

On the other hand, differential evolution algorithm has been utilized to find the optimal write voltage by maximizing the channel capacity (MCC) of flash memory channel in [8]. A write-voltage design scheme has been also proposed in [2] to design the efficient write voltage by minimizing the raw bit error rate (RBER) of flash memory channel. However, the authors have not considered the unbalanced RBERs between MSB and LSB pages. In [9], the authors have considered the unbalanced RBERs and searched the write voltage to minimize the RBER difference (MRD) between MSB and LSB pages. Nonetheless, this write-voltage scheme does not consider the influence of coding on flash memory system. To further improve the reliability of flash memory, more noises and interferences, the unbalanced RBER property as well as LDPC codes are considered in our proposed write-voltage design scheme.

To enable soft-decision decoding of error-correction codes, NAND flash memory systems usually need the fine-grained memory-sensing operations. Nonetheless, high sensing accuracy always lead to severe sensing delay. Therefore, it is very important to balance the decoding performance and delay in the read-voltage design of flash memory.

The conventional read-voltage design scheme has utilized the uniform quantization scheme [10]. This method has read the data by evenly placing the read voltage. However, the log-likelihood-ratio (LLR) information obtained by the uniform quantization scheme is not accurate. In [11], the authors have proposed a “constant ratio (CR)” non-uniform quantization scheme to improve the memory-sensing accuracy.

In [12], the authors have proposed the convolutional neural network (CNN)-based detection scheme to obtain the read voltages and LLR values. Nevertheless, these LLR values are not accurate because the network is used when the channel model is unknown, and it uses training data to obtain the conditional probability distribution of the voltage states corresponding to each threshold voltage, while the probability distribution of the threshold voltage cannot be obtained. The authors of [13] have proposed the adaptive read-voltage (ART) algorithm to use the statistical data for calculating the mean and variance of each voltage-state distribution, and then obtain the read voltages and calculate LLR values. But in practice, this scheme cannot obtain the accurate threshold voltages of the memory cells, and thus leads to inaccurate LLR values.

A read-voltage optimization scheme based on maximum mutual information (MMI) has been also proposed in [11]. However, this scheme obtains the read voltages under the assumption that the codeword length is infinite. The authors in [2] have also proposed to exploit the entropy function to select the read voltage for controlling the width of the erasure area, so as to find the read voltage that minimizes the bit error rate (BER). Nevertheless, in [2], the optimal entropy is obtained through the iterative decoding (i.e., belief-propagation (BP) decoding) operation, which suffers from high computational complexity.
1.2 Our Contributions

The principle idea behind this paper is to improve the decoding performance of LDPC-coded flash memory through optimization of write voltage and read voltage over the PE cycles and retention time. To achieve this goal, we first propose a cost-function-aided method to update the write voltage, called dynamic write-voltage design scheme. Furthermore, motivated by the importance of the LLR for decoding performance, we present a new read-voltage optimization scheme to adjust the position of read voltage to meet the variation of flash memory channel, which enables relatively lower complexity than the existing entropy-based read-voltage design scheme. Simulation results illustrate that the proposed dynamic write-voltage design scheme and the read-voltage optimization scheme can effectively improve the BER performance of flash memory compared with the state-of-the-art schemes.

The rest of the paper is organized as follows. In Sect. II, we depict the channel model of MLC flash memory. In Sect. III, we propose a novel cost-function-aided dynamic write-voltage design scheme for the flash memory system. The read-voltage optimization scheme is conceived in Sect. IV. Simulation results are shown and discussed in Sect. V. Finally, the conclusions are drawn in Sect. VI.

II. CHANNEL MODEL OF FLASH MEMORY

The practical NAND flash memory contains various non-stationary noises such as programming noise, RTN, data retention noise and CCI [2, 14]. These noises and interferences have different characteristics and vary continuously over the PE cycles and retention time. Figure 1 shows the threshold-voltage distribution in an MLC flash memory with Gray mapping. The write voltages for the four threshold-voltage states, i.e., $V_{min}$, $V_1$, $V_2$ and $V_{max}$, represent data symbols of 11, 10, 00, 01, respectively.

2.1 Programming Noise

In an MLC flash memory, the programming noise follows a Gaussian distribution [14]. The PDF of the programming noise is expressed by

$$p_{pi}(x) = \begin{cases} \mathcal{N}(0, \sigma_i^2) & \text{if } i = 11 \\ \mathcal{N}(0, \sigma_{ip}^2) & \text{if } i \neq 11 \end{cases}, \quad (1)$$

where $i \in \{11, 10, 00, 01\}$. In practice, the flash memory utilizes the iterative incremental step pulse programming (ISPP) algorithm for programming operation [15, 16]. Thus, the threshold-voltage distribution of the noise-free programming cell can be modeled as a uniform distribution [14]

$$p_{v_{pp}}(x) = \begin{cases} \frac{1}{v_{pp}}, & \text{for } 0 \leq x \leq v_{pp} \\ 0, & \text{otherwise} \end{cases}, \quad (2)$$

where $v_{pp}$ is the step size of programming voltage.

Afterwards, the programming-noise distribution for the programming cell can be calculated via the convolution operation (i.e., “∗”) of uniform and Gaussian distribution functions, given by [14]

$$p_{ni}(x) = p_{pi}(x) * p_{v_{pp}}(x), \quad (3)$$

where $p_{ni} \in \{p_{n10}, p_{n00}, p_{n01}\}$ for $V_i \in \{V_1, V_2, V_{max}\}$.

2.2 Random Telegraph Noise

In the NAND flash memory, PE cycling causes damage to the tunnel oxide of floating gate transistors, which directly results in threshold-voltage shift and fluctuation. This is referred to as random telegraph noise. In particular, the RTN is a non-stationary noise and the PDF can be defined as a Gaussian distribution [2]:

$$p_{i}(x) = \frac{1}{\sqrt{2\pi}\sigma_i} e^{-\frac{x^2}{2\sigma_i^2}}, \quad (4)$$

where $\sigma_i^2$ is the variance of the PDF for RTN, which is affected by the PE cycles.

2.3 Data Retention Noise

Data retention noise, caused by the leakage of charge from the floating gate over time, is one of the dominant errors in the flash memory. According to [17], the data
retention noise is approximately considered to follow Gaussian distribution whose mean and variance are affected by the data retention time and the number of PE cycle. The PDF is expressed by [2, 17]:

$$p_{r_i}(x) = \frac{1}{\sqrt{2\pi}\sigma_{r_i}} e^{-\frac{(x-\mu_{r_i})^2}{2\sigma_{r_i}^2}},$$

(5)

where $\mu_{r_i}$ and $\sigma_{r_i}^2$ represent the mean and variance of the PDF for data retention noise, and $i \in \{11, 10, 00, 01\}$. Especially, the mean $\mu_{r_i}$ and variance $\sigma_{r_i}^2$ can be calculated as [2]

$$\mu_{r_i} = [A_r \cdot (PE)^{\alpha_i} + B_r \cdot (PE)^{\alpha_0}] \times (V_{r_i} - x_0) \cdot \log(1 + T),$$

(6)

$$\sigma_{r_i} = 0.4 \cdot |\mu_{r_i}|.$$

(7)

### 2.4 Cell-to-Cell Interference

The cell-to-cell interference is caused by the effect of parasitic coupling capacitance between adjacent cells. Hence, the threshold voltage of the victim cell will increase during the programming procedure. According to [10], the voltage-shift value of the victim cell can be expressed as

$$\Delta V_{CCI} = \sum_k \Delta V_k \gamma_k,$$

(8)

where $\Delta V_{CCI}$ is the change of threshold voltage of the victim cell, $\Delta V_k$ is the shift of the threshold voltage in the $k$-th interference cell, and $\gamma_k$ is the capacitive coupling coefficient between the victim cell and the $k$-th interference cell. As the CCI in the readback voltage can be eliminated by employing the post-compensation technique [18], we ignore this interference in this work.

### 2.5 The Overall Threshold Voltage Distribution

According to [2], we can approximately describe the threshold voltages by a Gaussian distribution, i.e.,

$$p_{s_i}(x) = \frac{1}{\sqrt{2\pi}\sigma_{s_i}} e^{-\frac{(x-\mu_{s_i})^2}{2\sigma_{s_i}^2}},$$

(9)

where $i \in \{11, 10, 00, 01\}$, the means and variances of the four voltage states are as follows:

$$\mu_{s11} = V_{min} - \mu_{r11},$$

$$\sigma_{s11} = \sqrt{\sigma_{e}^2 + \sigma_{t}^2 + \sigma_{r11}^2},$$

$$\mu_{s10} = V_1 + \nu_{pp}/2 - \mu_{r10},$$

$$\sigma_{s10} = \sqrt{\sigma_{p}^2 + \sigma_{t}^2 + \sigma_{r10}^2},$$

$$\mu_{s00} = V_2 + \nu_{pp}/2 - \mu_{r00},$$

$$\sigma_{s00} = \sqrt{\sigma_{p}^2 + \sigma_{t}^2 + \sigma_{r00}^2},$$

$$\mu_{s01} = V_{max} + \nu_{pp}/2 - \mu_{r01},$$

$$\sigma_{s01} = \sqrt{\sigma_{p}^2 + \sigma_{t}^2 + \sigma_{r01}^2}.$$

In this paper, we set the channel model parameters as the same in [2]: $V_{min} = 1.4, V_{max} = 3.93, \sigma_{e} = 0.35, \sigma_{p} = 0.05, \nu_{pp} = 0.3, \sigma_{t} = 0.00025(PE)^{0.02}, A_r = 0.000055, B_r = 0.000235, \alpha_1 = 0.62, \alpha_0 = 0.32$ and $x_0 = 1.4$.

## III. PROPOSED DYNAMIC WRITE-VOLTAGE DESIGN SCHEME

To improve the error-rate performance of LDPC-coded flash memory, the write-voltage levels are required to be updated in order to mitigate the noise and interference. In the open literature, there are four main write-voltage design techniques adopted in the flash memory. The first three techniques are the fixed write-voltage design scheme [6], MCC write-voltage design scheme [8] and minimum-RBER write-voltage design scheme [2]. Nevertheless, the above three write-voltage design schemes do not consider the asymmetric property of RBERs [19, 20]. The last one...
is the MRD write-voltage design scheme [9], but it does not consider the influence of LDPC code on flash memory system. To address these issue, a dynamic write-voltage design scheme, which takes the unbalanced RBERs between MSB and LSB pages as well as the LDPC codes into consideration, is proposed in this paper.

According to [21], there is a nonlinear relation between BER and RBER, which means that this relationship can be expressed by a function. However, when using the BP decoding, it is impossible to get the BER from the RBER through theoretical derivation. Because Maximum-likelihood (ML) decoding is an optimal decoding scheme [22], the BER under ML decoding can be treated as the lower bound of the BER under any decoding. Thus, we use the following two formulas based on the ML decoding to estimate the BERs of LSB and MSB pages [20, Eq. (15) and Eq. (16)], i.e.,

\[
P_{\text{LSB}}^{\text{ML}} \approx \int (\alpha_{01} + \alpha_{21}) \omega \left[ \frac{d_{\min}}{2} \right] \times \sum_{d_2 \in \{d_{\min}, 2, \frac{d_{\min} + 1}{2}\}} A_2(d_2) 2^{-\left[ \frac{d_{\min}}{2} \right]}(d_2),
\]

\[
P_{\text{MSB}}^{\text{ML}} \approx \int (\alpha_{12} \omega) \left[ \frac{d_{\min}}{2} \right] \times \sum_{d_1 \in \{d_{\min}, 2, \frac{d_{\min} + 1}{2}\}} A_1(d_1) 4^{-d_1}(d_1),
\]

where \(\alpha_{gh} \omega\) is the transition probability from voltage state \(g\) to \(h\), and \(g, h \in \{0, 1, 2, 3\}\). There is a mapping rule between \(g/h\) and the voltage state, i.e., \(\{0 \rightarrow 11, 1 \rightarrow 10, 2 \rightarrow 00, 3 \rightarrow 01\}\). For the LDPC code employed by page \(z\), \(d_z\) is the code distance and \(A_z(d_z)\) is the Hamming distance spectrum, where \(z = 1\) and \(2\) denote the MSB page and LSB page, respectively.

Because MSB and LSB pages use the same LDPC code, and the corresponding minimum codeword distances \(d_{\min}^2\) on both pages are identical, A simplified function (i.e., cost function (12)) can be formulated by removing the terms involving \(d_z\) (i.e., \(A_z(d_z)\) and \(\left[ d_z / 2 \right] \)) from Eq. (10) and Eq. (11). The above simplification can significantly reduce the computational overhead.

In this cost function, we divide the RBER into two parts, the RBERs of MSB and LSB pages. Finally, the write voltage is determined by the cost-function output. In this work, by considering the asymmetric property of the MSB-page and LSB-page error rates, as well as the minimum Hamming distance of LDPC code, we first define the cost function \(C_{\text{write}}\) for an MLC flash memory channel as follows:

\[
C_{\text{write}} = 2^{-\frac{d_{\min}}{2}} \omega_{\text{lsb}} + 4^{-d_{\min}} \omega_{\text{msb}},
\]

where \(d_{\min}\) is the minimum Hamming distance of the LDPC code that can be estimated by [23]. \(\omega_{\text{lsb}}\) and \(\omega_{\text{msb}}\) are the RBERs of LSB and MSB pages, respectively. Assume that the MLC flash memory exploits three read voltages \(\{t_1^*, t_2^*, t_3^*\}\) to distinguish four threshold-voltage states, and the input probabilities of four data symbols are equal, i.e., \(p_i = 1/4\). Therefore, we can compute the RBERs of MSB and LSB pages as [2]

\[
\omega_{\text{msb}} = \frac{1}{4} \left[ p_{s10}(v > t_2^*) + p_{s00}(v < t_2^*) \right],
\]

\[
\omega_{\text{lsb}} = \frac{1}{4} \left[ p_{s11}(v > t_1^*) + p_{s10}(v < t_1^*) \right] + \frac{1}{4} \left[ p_{s00}(v > t_3^*) + p_{s01}(v < t_3^*) \right],
\]

where \(t_1^*, t_2^*\) and \(t_3^*\) are read-voltage levels at the intersections of adjacent voltage states. For the sake of obtaining \(t_1^*, t_2^*\) and \(t_3^*\), we need to solve three equations:

\[
p_{s11}(v = t_1^*) = p_{s10}(v = t_1^*)
\]
\[
p_{s10}(v = t_2^*) = p_{s00}(v = t_2^*)
\]
\[
p_{s00}(v = t_3^*) = p_{s01}(v = t_3^*)
\]

We get \(t_1^* \in (V_{\min}, V_1)\), \(t_2^* \in (V_1, V_2)\) and \(t_3^* \in (V_2, V_{\max})\). Since Eq. (12) represents the cost of BER, we need to find \(V_1^*\) and \(V_2^*\) that minimize the output of Eq. (12). As a result, the optimal \(V_1^*\) and \(V_2^*\) can be yielded by tackling with the following optimization
Based on the above discussion, we first search for \( V_1^* \) by fixing \( V_2^* \) to minimize the cost function. Since \( V_1 \in (V_{\min}, V_2) \), we can uniformly divide this region into \( M - 1 \) intervals, and thus obtain the boundaries \( V_1 = \{V_1^1, V_1^2, \ldots, V_1^M\} \) of those intervals. To get the optimal \( V_1^* \), we need to obtain all the values of cost function corresponding to \( M \) write voltages. Through such a method, the optimal \( V_1^* \) corresponding to the minimum value of \( C_{\text{write}} \) can be obtained by employing the bisection search method [24]. Likewise, the optimal value \( V_2^* \) can be also obtained by fixing \( V_1^* \), where \( V_2 \in (V_1, V_{\max}) \). These two search operations are repeated in a sequential order until \( V_1^* \) and \( V_2^* \) no longer change or the maximum number \( q \) of iteration is reached. The details of the proposed dynamic write-voltage design scheme are summarized in Algorithm 1.

### IV. PROPOSED COST-FUNCTION-BASED READ-VOLTAGE OPTIMIZATION SCHEME

#### 4.1 Preliminaries

In [2], an entropy-based quantization scheme was proposed to design the read voltage by varying the entropy \( \theta \). Nevertheless, this method obtains the optimal entropy \( \theta^* = 0.35 \) by fixing the retention time as 0. Once the retention time \( T \) varies, the entropy-based quantization scheme needs to use a large number of decoding operations for acquiring the optimal \( \theta^* \), inevitably causing high computational complexity. To address this issue, a novel read-voltage optimization scheme is proposed in this section, which takes the inaccurate LLRs and the unbalanced RBERs of the LDPC-coded flash memory system into consideration. Our objective is to obtain the optimal read voltage while maintaining low computational complexity.

To begin with, we define the entropy function \( H(v) \) as [2]

\[
H(v) = \sum_i \left[ \frac{p_{s_i}(v)}{\sum_j p_{s_j}(v)} \log_2 \left( \frac{\sum_j p_{s_j}(v)}{p_{s_i}(v)} \right) \right],
\]

where \( s_i \in \{s_{11}, s_{10}, s_{00}, s_{01}\} \) and \( p_{s_i} \) is the PDF of the threshold-voltage state \( s_i \).

The main error area usually occurs in the overlapping areas between adjacent threshold-voltage states. Thus, we can optimize the read voltage to determine the main error area by resolving the following function [2]

\[
H(R_n) = \theta, \quad \theta \in [0, 1].
\]

Thus, we can obtain six read voltages, i.e., \( R_1, R_2, \ldots, R_6 \), by changing the value of \( \theta \). The optimization of read voltage can be transformed to the optimization of \( \theta \).

Moreover, as shown in Figure 1, we can calculate

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**Algorithm 1. Proposed write-voltage design algorithm.**

1: **Initialization:** \( V_2^* = 3.3 \).
2: for \( q = 1 \) to 50 do
3: for \( V_1 \in (V_{\min}, V_2) \) do
4: \( \text{Set } V_2 = V_2^*; \)
5: Uniformly divide \( (V_{\min}, V_2) \) into \( M - 1 \) intervals;
6: Calculate the RBERs of MSB and LSB pages by applying Eq. (13) and Eq. (14);
7: Calculate the values of cost function corresponding to \( M \) write voltages by using Eq. (12);
8: **end for**
9: Find \( V_1 \in (V_{\min}, V_2) \) that minimizes \( C_{\text{write}} \);
10: Set \( V_1^* = V_1 \);
11: for \( V_2 \in (V_1, V_{\max}) \) do
12: \( \text{Set } V_1 = V_1^*; \)
13: Uniformly divide \( (V_1, V_{\max}) \) into \( M - 1 \) intervals;
14: Calculate the RBERs of MSB and LSB pages by applying Eq. (13) and Eq. (14);
15: Derives the values of cost function corresponding to \( M \) write voltages by using Eq. (12);
16: **end for**
17: Find \( V_2 \in (V_1, V_{\max}) \) that minimizes \( C_{\text{write}} \);
18: Set \( V_2^* = V_2 \);
19: if \( V_1^* \) and \( V_2^* \) no longer change then\;
20: \( \text{break}; \)
21: **end if**
22: **end for**
the LLR information for each threshold-voltage region, as [2, 12]

\[
L_{msb} = \log \frac{\int_{R_{n-1}}^{R_n} \{ p_{s00}(v) + p_{s01}(v) \}dv}{\int_{R_{n-1}}^{R_n} \{ p_{s10}(v) + p_{s11}(v) \}dv}, \tag{18}
\]

\[
L_{lsb} = \log \frac{\int_{R_{n-1}}^{R_n} \{ p_{s00}(v) + p_{s10}(v) \}dv}{\int_{R_{n-1}}^{R_n} \{ p_{s01}(v) + p_{s11}(v) \}dv}, \tag{19}
\]

where \(R_n(n = 1, 2, \ldots, 6)\) is the \(n\)-th read voltage, \(R_{n-1} < v < R_n\).

\subsection*{4.2 Proposed Optimization Scheme}

Considering the effect of the inaccurate LLR information and the unbalanced RBERs, we propose to optimize the entropy \(\theta\) by minimizing a new cost function.

When three optimal read voltages \(t_1^*, t_2^*, \text{and} t_3^*\) are used for soft-decision BP decoding, two LLR sequences corresponding to LDPC codewords can be obtained, which belong to LSB and MSB pages, respectively. Then, the BER of LDPC codes under ML decoding can be estimated [25], which is similar to Eq. (10) and Eq. (11).

When the entropy-based quantization scheme is used, the read voltages will be set near the intersections (i.e., \(t_1^*, t_2^*, \text{and} t_3^*\)) of adjacent voltage states. If the threshold voltage is in a region including an intersection, its corresponding LLR value is close to 0. Exploiting ML decoding, the LLR value 0 can be decoded as either \(+\zeta\) or \(-\zeta\) with a high probability, where \(\zeta\) is a constant. As can be observed, 0 has the same distance to \(+\zeta\) and \(-\zeta\), which does not affect the result of ML decoding. Thus, we can use the BER of LDPC codes using three-optimal read voltages under ML decoding to find the optimal entropy of the entropy-based quantization scheme.

The read voltages are directly related to BP decoding, because the LLR values of all threshold-voltage regions can be calculated after determining the read voltages. In this sense, the change of LLR value when error occurs can better reflect the noise level as \(\omega_{lsb}\) and \(\omega_{msb}\) in the Eq. (12).

The proposed read-voltage scheme is different from that in [22] because the latter assumes that the RBERs of bit 1 and bit 0 are equal, while the former assumes that they are unequal. In practical flash memory, the RBERs of bit 1 and bit 0 are always unequal. One can measure this inequality level by calculating the expected LLR of error bits.

Therefore, using the equations (13), (14), (18), and (19), we can compute the noise level \(\alpha_{lsb}^P\) and the expected LLR \(\alpha_{lsb}^{llr}\) corresponding to the error bits in the LSB page under BP decoding, given by

\[
\alpha_{lsb}^P = \sum_{i=1}^{7} |L_{lsb}^i| \cdot P_{lsb}^i, \tag{20}
\]

\[
\alpha_{lsb}^{llr} = \sum_{i=1}^{7} L_{lsb}^i \cdot P_{lsb}^i, \tag{21}
\]

where \(L_{lsb}^i\) represents the corresponding LLR value of LSB on the interval \([R_{i-1}, R_i]\), \((i = 1, 2, \ldots, 7)\), as shown in Figure 1. In general, \(R_0\) and \(R_7\) are set as \(-\infty\) and \(+\infty\). \(P_{lsb}^i\) is the RBER of LSB page in the interval \([R_{i-1}, R_i]\). In addition, \(\alpha_{lsb}^P\) and \(\alpha_{lsb}^{llr}\) can be calculated in similar way.

Similar to the cost function (12), the cost functions (22) and (23) can be constructed according to the input variables \(\alpha_{msb}^P\) and \(\alpha_{msb}^{llr}\), respectively, i.e.,

\[
C_{read}^P = 2^{(-\frac{1}{2}d_{min})} \alpha_{lsb}^P + 4^{(-d_{min})} \alpha_{msb}^P, \tag{22}
\]

\[
C_{read}^{llr} = 2^{(-\frac{1}{2}d_{min})} \alpha_{lsb}^{llr} + 4^{(-d_{min})} \alpha_{msb}^{llr}, \tag{23}
\]

where \(d_{min}\) is the minimum Hamming distance of the LDPC code that can be estimated by [23], \(\alpha_{lsb}^P\), \(\alpha_{msb}^P\), \(\alpha_{lsb}^{llr}\), and \(\alpha_{msb}^{llr}\), are given in the Eq. (20) and Eq. (21).

In order to comprehensively consider the impact of the noise level and expected LLR of error bits on the BER, we can obtain the overall cost function, as

\[
C_{read} = c_1 \cdot C_{read}^P + c_2 \cdot C_{read}^{llr}. \tag{24}
\]

In fact, the effect of the noise level and expected LLR on the BER performance of an LDPC-coded flash memory is uncertain. For this reason, two weighted factors \(c_1\) and \(c_2\) need to be included in the Eq. (24) in order to indicate their influence on the BER performance. To estimate the weighted factors \(c_1\) and \(c_2\), we first need to obtain a BER sequence versus the entropy \(\theta\) under the BP decoding. Subsequently, we use the
linear regression technology to couple the cost function and BER [26]. Finally, the two weighted factors are yielded.

With the help of the LLR-aware cost function (24), the optimal entropy $\theta^*$ can be derived by solving the following optimization problem

$$\theta^* = \arg \min_{\theta} C_{oa}^{read}.$$  \hfill (25)

Figure 2a depicts the cost function by varying the value of $\theta$. As shown, the cost function is a concave function, the gradient-descent (GD) algorithm [27] can be used to search for the optimal $\theta^*$ that yields the minimum value of $C_{oa}^{read}$. Then, we can obtain the optimal $\{R_1^*, R_2^*, \ldots, R_6^*\}$ corresponding to the optimal $\theta^*$. To guarantee the desirable BER performance of flash memory, the cost function is required to be re-calculated so as to get the new optimal read voltages when the PE cycles or retention time varies.

### 4.3 Verification of Proposed Optimization Scheme

Figure 2 shows the BER performance and the corresponding cost function value of the proposed read-voltage optimization scheme versus the entropy $\theta$, where the PE cycles is set to 6000 and the retention time $T$ is set to 15000. It can be seen that the minimum BER performance of the proposed read-voltage optimization scheme also can be obtained at the optimal $\theta^* = 0.55$ that yields the minimum value of the cost function. We have also performed verification with the same parameter setting as in [2], and have obtained the same optimal entropy value as $\theta^* = 0.35$. The above phenomenon verifies that the proposed read-voltage optimization scheme can derive the optimal entropy $\theta^*$ achieving the minimum BER performance.

### 4.4 Complexity Analysis

The proposed read-voltage optimization scheme is based on an LLR-aware cost function, while the entropy-based read-voltage optimization scheme in [2] is based on the output of BP decoding. Here, we briefly compare their computational overheads so as to further illustrate the superiority of our design. When comparing the computational overhead, we do not consider the estimation of threshold-voltage distribution and associated LLR values, because these two steps are involved in both schemes. Now, we set $Q$ to be the number of read voltages. For the proposed scheme, the computational overhead mainly comes from the measurement of the variables $\alpha_{lsb}^P$, $\alpha_{llr}^{lsb}$, $\alpha_{msb}^P$, $\alpha_{llr}^{msb}$ and $C_{oa}^{read}$. As such, the computational overhead of the proposed cost function-based quantization scheme is $\mathcal{O}(8(Q + 1))$ for obtaining a single entropy $\theta$.

On the other hand, the computational overhead of the entropy-based quantization scheme mainly comes from the LLR update of variable nodes and check nodes within an LDPC code [29–31]. We set $d_v$ to be the average degree of variable nodes of the protograph LDPC code, $d_c$ to be the average degree of check nodes, $\eta$ to be the number of check nodes, $N$
to be the length of the codeword sequence, \( I \) to be the average decoding-iteration number for each codeword, and \( B \) is the number of codewords generated in BP decoding simulation for calculating a single entropy \( \theta \) (e.g., when the frame error rate is equal to \( 10^{-6} \), the number of codewords should be greater than \( 10^8 \) to obtain a sufficiently reliable simulation result). Therefore, the computational overhead of the entropy-based quantization scheme is \( \mathcal{O}(2(2d_v + 1)IB + 4d_v \eta B + 4d_v \eta B) \approx \mathcal{O}(8d_v \eta B) \) because \( \eta \gg 2 \).

Table 1 summarizes the computational overheads of the proposed cost function-based quantization scheme and the entropy-based quantization scheme required for calculating a single entropy \( \theta \). As observed, the proposed read-voltage optimization scheme benefits from much lower computational complexity with respect to entropy-based quantization scheme. Besides, the proposed read-voltage optimization scheme and the entropy-based quantization scheme [2] should take the same storage space to store the entropy values and their corresponding cost function values and BERs, respectively.

In application, the optimal read voltages at a certain PE cycles and retention time can be calculated off-line, and then stored into a look-up table in the flash memory.

### V. SIMULATION RESULTS

In this section, we present various simulation results of the proposed dynamic write-voltage design scheme and the read-voltage optimization scheme to verify their superiority over the flash memory channel. The simulations are carried out by using MATLAB. We utilize the rate-0.89 protograph LDPC code [28, 32] in the simulations, which is constructed by employing a modified progressive-edge-growth (PEG) algorithm [33]. For decoding of LDPC codes, we use the BP algorithm and assume the maximum number of iterations as 50.

#### Figure 3. BER performance of the fixed write-voltage design scheme, MCC write-voltage design scheme, minimum-RBER write-voltage design scheme, MRD write-voltage design scheme and the proposed dynamic write-voltage design scheme versus the PE cycles.

#### 5.1 BER Performance of Dynamic Write-Voltage Design Scheme

Figure 3 and Figure 4 show the BER performance of the fixed write-voltage design scheme [6], MCC write-voltage design scheme [8], minimum-RBER write-voltage design scheme [2], MRD write-voltage design scheme [9] and the proposed dynamic write-voltage design scheme versus the PE cycles and retention time over an MLC flash memory channel, respectively. It can be seen that the performance of the proposed dynamic write-voltage design scheme is obviously superior to that of the other four write-voltage design schemes. It is because that we substantially consider the unbalanced RBERs between MSB and LSB pages. In particular, at PE = 18000, the proposed dynamic write-voltage design scheme achieves a BER of \( 2.2 \times 10^{-6} \), while the MRD write-voltage design scheme [9], minimum-RBER write-voltage design scheme [2], MCC write-voltage design scheme [8] and the fixed write-voltage design scheme [6] only accomplish the BERs of \( 1.0 \times 10^{-5}, 7.5 \times 10^{-5}, 1.8 \times 10^{-4} \) and \( 2.3 \times 10^{-3} \), respectively.
To improve the reliability of the LDPC-coded MLC flash memory, we have presented a novel dynamic write-voltage design scheme to update the write voltage by considering the asymmetric property of the MSB-page and LSB-page error rates. Besides, we have conceived an LLR-aware cost function to optimize the read voltages, which can further improve the BER performance of flash memory with relatively low computational complexity. Simulation results have shown that our proposed dynamic write-voltage design and read-voltage optimization scheme outperforms the state-of-the-art schemes over MLC flash memory channel. Besides, the proposed schemes can be extended to 3D NAND flash memory after proper modifications.

VI. CONCLUSION

Figure 4. BER performance of the fixed write-voltage design scheme, MCC write-voltage design scheme, minimum-RBER write-voltage design scheme, MRD write-voltage design scheme and the proposed dynamic write-voltage design scheme versus the retention time.

Figure 5. BER performance of the uniform quantization scheme, ART quantization scheme, CNN-based detection scheme, MMI read-voltage scheme, entropy-based quantization scheme ($\theta = 0.35$) and proposed read-voltage optimization scheme versus the PE cycles.

Figure 6. BER performance of the uniform quantization scheme, ART quantization scheme, CNN-based detection scheme, MMI read-voltage scheme, entropy-based quantization scheme ($\theta = 0.35$) and proposed read-voltage optimization scheme versus the retention time.

quantization scheme, the entropy-based quantization scheme and the uniform quantization scheme. For example, at retention time = 2500, the proposed read-voltage optimization scheme obtains a BER of $3.6 \times 10^{-5}$, while the MMI read-voltage optimization scheme, the CNN-based detection scheme, the ART quantization scheme, the entropy-based quantization scheme, and the uniform quantization scheme obtain the BERs of $4.5 \times 10^{-5}$, $1.2 \times 10^{-4}$, $5.0 \times 10^{-4}$, $1.3 \times 10^{-3}$ and $3.5 \times 10^{-2}$, respectively.

5.2 BER Performance of Read-Voltage Optimization Scheme

Figure 5 and Figure 6 show the BER performance of the uniform quantization scheme [10], ART quantization scheme [13], CNN-based detection scheme [12], MMI read-voltage quantization scheme [11], entropy-based quantization scheme [2] and proposed read-voltage optimization scheme versus the PE cycles and retention time over an MLC flash memory channel, respectively. As shown, the proposed read-voltage optimization scheme not only slightly outperforms the MMI quantization scheme, but also is significantly superior to the CNN-based detection scheme, the ART
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