Zero-voltage and zero-current switching phase-shifted full-bridge converter with reduced output filter requirement

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Abstract In this paper, a novel zero-voltage and zero-current switching (ZVZCS) phase-shifted full-bridge (PSFB) converter is proposed to improve the efficiency of traditional PSFB converter. The proposed converter consists of two half-bridge inverters in the primary side and two center-tap rectifiers with one shared output filter in the secondary side. This structure allows the proposed converter to achieve a wide range of ZCS for lagging-leg switches and ZVS for leading-leg switches. The primary energy can be continuously transferred to the secondary side, which is helpful to reduce output filter requirement. The operational principle and design considerations are explained and analyzed in detail. A laboratory prototype with 320-385-V input 50-V/20-A output is built to verify the superior features of the proposed converter.

Keywords: full-bridge converter, output filter requirement, zero-voltage and zero-current switching (ZVZCS)

Classification: Power devices and circuits

1. Introduction

The phase-shifted full-bridge (PSFB) can provide zero-voltage switching (ZVS) for the power switches without the help of any auxiliary components, thus high efficiency and high power density can achieve. Due to these advantages, it has been the most popular candidate in high power applications, such as battery charger and renewable power system [1, 2, 3, 4, 5]. However, the traditional PSFB converter has some serious drawbacks that need to be resolved. First drawback is the severe secondary voltage oscillation, which increases the voltage stress of diodes up to two times [6, 7]. Then, the available ZVS energy is decreased with load current. Both the primary voltage and current are maintained at zero during freewheeling interval. Excessive primary current results in high voltage stress of secondary devices and large ripple of output filter.

Many novel FB dc-dc converters have been proposed to improve the performance of traditional PSFB converter. The secondary voltage oscillation can be well suppressed by the use of snubber or clamping circuits. A resistor-capacitor-diode (RCD) configuration is the most usual circuit [10]. The main disadvantage of RCD circuit is that the power loss in resistor drastically reduce the overall efficiency. In [11, 12, 13, 14], some lossless snubber circuits are implemented. Thus, the power loss of the added circuit is avoided. In [15, 16], two clamp diodes are introduced into the primary side of PSFB converter and the voltage oscillation can be effectively suppressed. However, these converters do not solve the problems of primary circulating current and narrow ZVS range.

Generally, the ZVS range can be easily extended by increasing the leakage inductance of main transformer [17, 18, 19]. However, this method causes serious duty-cycle loss. In [20, 21, 22, 23], the auxiliary circuits with inductors are introduced into the PSFB converter. The available ZVS energy is mainly stored in the auxiliary circuits and it is independent of load current, thus switches can obtain ZVS characteristic under all operating conditions. But the auxiliary circuits increase conduction loss and the efficiency at heavy load is degraded seriously. Moreover, the circulating current still exists and it consumes high energy like the traditional PSFB converter.

In order to remove the primary circulating current, some full-bridge converters with zero-voltage and zero-current switching (ZVZCS) operation are proposed [24, 25, 26, 27, 28]. In these converters, the primary current is reset by the additional auxiliary circuits and the lagging-leg switches are turned off with zero current. Both the primary voltage and current are maintained at zero during freewheeling interval. Thus, the transmission of primary power is discontinuous, which results in high voltage stress of secondary devices and large ripple of output filter.

This paper proposes a novel ZVZCS full-bridge converter, which can solve the aforementioned drawbacks of existing converters. Fig. 1 shows the circuit diagram of proposed converter. As shown in Fig. 1, the proposed converter consists of two half-bridge inverters (HBIs) in the primary side and two center-tap rectifiers with one shared output filter in the secondary side. Q₁, Q₃, T₁ and C₈ form the lagging-HBI. Q₂, Q₄, T₂ and C₉ form the leading-HBI. This structure allows the proposed converter to achieve a wide range of ZCS for lagging-leg switches and ZVS for leading-leg switches. In addition, the primary power can be delivered to the secondary side during the whole switching period. Thus, the circulating current is removed and the requirement of output filter is also significantly reduced.

In order to verify the effectiveness of efficient improve-
iment, a 320-385-V input 50-V/20-A output prototype based on the proposed converter is built and tested. Experimental results show that the proposed converter can achieve higher conversion efficiency than the traditional PSFB converter.

2. Operational principle

To simplify analysis, the output filter inductor $L_n$ is considered as a constant current source and the blocking capacitor $C_b$ is modeled as a constant voltage source of $0.5V_{in}$. In addition, the magnetizing inductance of $T_1$ and the junction capacitances of IGBTs are ignored. The simplified equivalent circuit is shown in Fig. 2. The leakage inductances of $T_1$ and $T_2$ are $L_{k1}$ and $L_{k2}$, respectively. The magnetizing inductance of $T_2$ is $L_m$. The junction capacitances of MOSFETs are $C_{oss}$. $T_1$ and $T_2$ have the same turns ratio of $n = n_s/n_p$.

Fig. 3 shows the key operational waveforms of the proposed converter. $T_s$ means switching period of primary switches, $D$ means duty-cycle of rectified voltage and the phase time is $0.5DT_s$. Each switching period is consisted of twelve modes, which can be divided into two half cycles, $t_0$~$t_6$ and $t_6$~$t_{12}$. Due to the symmetry of the converter, only the first half cycle is described here and the corresponding equivalent circuits are shown in Fig. 4.

Mode 1 [$t_0$~$t_1$]: $Q_1$, $Q_2$ and $D_1$ are ON. The primary voltages of $T_1$ and $T_2$ are $0.5V_{in}$. Thus, the magnetizing current $i_m(t)$ increases linearly and the rectified voltage $v_{rec}(t)$ is $nV_{in}$. This mode is defined as duty-cycle interval.

Mode 2 [$t_1$~$t_2$]: $Q_2$ is turned off at $t_1$. In this mode, the junction capacitances are discharged linearly by the leading-leg current $i_{p2}$. Thus, the leading-leg voltage $v_{leq}(t)$, the voltages of $T_2$, and the rectified voltage $v_{rec}(t)$ decreases linearly at the same time. The voltage across rectified diode $D_2$ is $2v_{leq} + v_{s1}$. $v_{s1}$ is maintained constant $0.5nV_{in}$ and $v_{leq}$ decreases linearly. At $t_2$, $2v_{leq} + v_{s1}$ falls to zero and $D_4$ starts to conduct.

Mode 3 [$t_2$~$t_3$]: During this mode, the resonance of leakage inductances and junction capacitances occurs in the primary side since $D_4$ and $D_3$ conduct simultaneously. The initial value of $v_{leq}(t)$ is $0.25V_{in}$ and it decreases with a sinusoidal shape.

\[ v_{leq}(t) = 0.25V_{in} - (nL_s + I_m)z \sin \omega(t - t_2) \]  

where \( \omega = 1/\sqrt{2C_{oss}L_{eq}} \) $z = \sqrt{L_{eq}/2C_{oss}}$ $L_{eq} = 0.25L_{k1} + L_{k2}$

Mode 4 [$t_3$~$t_4$]: At $t_3$, $v_{leq}(t)$ falls to zero. Then, the parasitic diode of $Q_4$ begins to conduct and $Q_4$ is turned on with ZVS. The voltage across $L_{k1}$ is given by

\[ v_{k1}(t) = -0.125L_{k1}V_{in}/L_{eq} \]  

The leading-leg current decreases linearly and it is

\[ i_{p1}(t) = i_{p1}(t_3) + \frac{v_{k1}(t)}{L_{k1}}(t - t_3) \]  

Mode 5 [$t_4$~$t_5$]: At $t_4$, $i_{p1}(t)$ falls to zero and $D_4$ turns off naturally. The commutation of $D_1$ and $D_3$ finishes. During this mode, the power flowing through the lagging-HBI is
zero and only the leading-HBI transfer the primary energy to the output side.

Mode 6 \([t_5\sim t_6]\): The lagging-HBI current is zero and Q1 is turned off with ZCS at \(t_5\). After a short dead-time, Q3 is turned on and D3 starts to conduct. The voltage across \(L_k\) is 0.5\(V_n\) and \(i_{p1}(t)\) begins to rise linearly in the negative direction. At \(t_6\), \(i_{p1}(t)\) reaches to \(-nI_0\), and D4 turns off. The commutation between D2 and D4 is completed.

3. Performance comparison

3.1 Voltage conversion ratio

The durations of ZVS transitions are very narrow and only Mode 1, Mode 5 are considered. The rectified voltage during duty-cycle interval (Mode 1) is \(nV_n\) while it is 0.5\(nV_n\) during freewheeling interval (Mode 5). For the traditional PSFB converter, the rectified voltage is zero during freewheeling interval. Since the output voltage is equal to the average of rectified voltage, the voltage conversion ratios of these two converters can be calculated as follows, respectively.

\[
G_{pro}(D) = V_o/nV_n = D + 0.5 \quad (4)
\]

\[
G_{ref}(D) = V_o/nV_n = D \quad (5)
\]

It is obvious that \(G_{pro}(D)\) is higher than \(G_{ref}(D)\). Generally, the converter with high voltage gain can be designed with a small turns ratio of transformer, which is helpful for the reductions of secondary voltage stress and primary conduction loss [29, 30]. Therefore, the proposed converter has the performance over the traditional PSFB converter.

3.2 Output filter requirement

The output filter requirement is mainly decided by the waveform of rectified voltage. In the traditional converter, the rectified voltage is zero during freewheeling interval and the output power is maintained constant by the energy stored in the output filter. This is in contrast to the fact that in the proposed converter, the rectified voltage is greater than zero during the whole switching period and the primary power can be continuously transferred to output side. Therefore, the output filter requirement is significantly reduced, which is helpful to improve the power density and conversion efficiency.

The output filter inductor is designed based on the following equation.

\[
L_o = \frac{V\Delta t}{\Delta I_o} \quad (6)
\]

where \(V\) means the voltage applied to the output filter inductor \(L_o\) during the time \(\Delta t\) and \(\Delta I_o\) means the current ripple flowing through \(L_o\).

For the proposed converter

\[
L_{pro} = \frac{T_sV_o}{4\Delta I_o} \times \frac{D(1-D)}{D+1} \quad (7)
\]

For the traditional converter

\[
L_{tra} = \frac{T_sV_o}{4\Delta I_o} \times (1-D) \quad (8)
\]

From (7) and (8), the ratio of \(L_{pro}\) to \(L_{tra}\) is given as

\[
r(D) = \frac{L_{pro}}{L_{tra}} = \frac{D}{D+1} \quad (9)
\]

Fig. 5 shows the curve of \(r(D)\) versus duty-cycle. As shown in Fig. 5, the required value of output filter inductor in the proposed converter is much smaller than that in the traditional converter. The reduced filter requirement is beneficial in terms of size and weight.

3.3 Soft-switching conditions of the proposed converter

The ZVS transition of leading-HBI is divided into two phases, Mode 2 \([t_1\sim t_2]\) and Mode 3 \([t_2\sim t_3]\), as shown in Fig. 6(a). In the first phase, \(v_{ileg}(t)\) decreases linearly. When \(v_{ileg}(t)\) falls to 0.25\(V_n\), at \(t_3\), the resonance between leakage inductances and junction capacitances occurs and \(v_{ileg}(t)\) decreases with a sinusoidal waveform. Based on (1), the ZVS condition of leading-leg switches can be expressed as

\[
\frac{1}{2}(0.25L_k + L_d)(nI_o + I_m)^2 > \frac{4}{3}C_{oxs}(0.25V_n)^2 \quad (10)
\]

The lagging-leg current is reset by a voltage source during Mode 4. The resetting time is derived from (3).

\[
t_{ZCS} = i_{p1}(t_3)(0.25L_k + L_d) = \frac{nI_o(0.25L_k + L_d)}{0.125V_n} \quad (11)
\]

Fig. 6(b) shows the simplified waveforms during the ZCS transition. In order to realize the ZCS operation, the lagging-leg current should have enough time to decay to zero. Thus, the resetting time \(t_{ZCS}\) need to be smaller than 0.5(1 - \(D\))\(T_s\). The ZCS condition of lagging switches is represented as

\[
D_{max} \leq 1 - \frac{16nI_{max}(0.25L_k + L_d)}{V_nT_s} \quad (12)
\]

where \(I_{max}\) means maximum load current and \(D_{max}\) means maximum duty-cycle.

Thus, the lagging switches can easily achieve ZCS operation over the entire input voltage and load range.

3.4 Mechanism analysis of voltage oscillation

The junction capacitances of rectified diodes are ignored to simplify the analysis when the operation principle is intro-
duced in Section II. Actually, the secondary-voltage oscillation is mainly caused by the resonance between junction capacitances and leakage inductance of transformer after the lagging-leg transition [6, 7]. Since \(D_2\) and \(D_4\) have much lower average current values compared to \(D_1\) and \(D_3\), lower current-rated diodes are adopted for \(D_2\) and \(D_4\). In this part, only the junction capacitances of \(D_1\) and \(D_3\) are considered to analyze the oscillation mechanism. The leakage inductances of main transformers and junction capacitances of rectified diodes constitute the resonant circuit after the ZCS transition is finished at \(t_6\), as shown in Fig. 7. \(C_j\) means the junction capacitance of \(D_1\) or \(D_3\).

Based on the equivalent circuit during Mode 6 \([t_5 \sim t_6]\), the initial voltage \(v_{j0}\) of \(C_j\) is \(nV_{in}\). The oscillation voltage \(v_j\) in the proposed converter is calculated based on Fig. 7(b).

\[
v_j(t) = 2nV_{in} + (v_{j0} - 2nV_{in}) \cos \omega_j t \tag{13}
\]

where \(\omega_j = 1/2n\sqrt{C_j(L_{d1} + L_{d2})}\)

The oscillation voltage in the traditional PSFB converter with center-tap rectifier is expressed as

\[
v_j(t) = 2nV_{in}(1 - \cos \omega_j t) \tag{14}
\]

According to (13) and (14), the peak value of oscillation voltage in the proposed converter is \(3nV_{in}\) while it is \(4nV_{in}\) in the traditional PSFB converter. In order to alleviate the voltage oscillation, a RCD snubber circuit is employed. Generally, the loss of RCD circuit is proportional to the peak voltage of oscillation. Thus, the snubber loss in the proposed converter can be reduced compared with the traditional converter.

4. Experimental results

To verify the performance of proposed converter, an experimental prototype is established. The specifications and circuit parameters are illustrated in Table I.

Fig. 8 shows the experimental waveforms of lagging-HBI and leading-HBI at \(V_{in} = 385\) V and \(I_o = 20\) A. As shown in Fig. 8, \(i_{p2}\) and \(v_{p2}\) always have negative or positive values, and \(i_{p3}\) falls to zero after the transition of leading-HBI ends. Therefore, the leading-HBI can continually transfer power to the secondary side while the lagging-HBI only transfers power during duty-cycle. The experimental results coincide well with the theoretical waveforms described in Fig. 3.

Fig. 9 shows the key waveforms of secondary voltages. As shown in Fig. 9, the rectified voltage is always greater than zero, thus there is no problem related to the duty-cycle loss. The conducting time of \(D_4\) is much smaller than that of \(D_3\), which means that the average current value of \(D_4\) is much smaller than that of \(D_3\). In the proposed prototype, \(D_1\) and \(D_3\) are selected as MBR20200CT while \(D_2\) and \(D_4\) can share one MBR20200CT, which is composed of two diodes in one package.

Fig. 10 and Fig. 11 show the ZVS and ZCS waveforms under different load conditions. It can be noted from Fig. 10 and Fig. 11 that the leading switches are turned on with zero

\begin{table}[h]
\centering
\begin{tabular}{|c|c|}
\hline
Parameter & Value \\
\hline
Input voltage \(V_{in}\) & 320–385V \\
Output voltage \(V_o\) & 50 V \\
Maximum output current \(I_{out}\) & 20 A \\
Leading-leg switches \(Q_1\&Q_2\) & FQP12N60 (600, 10.5A) \\
Lagging-leg switches \(Q_3\&Q_4\) & STG5S160 (600V, 16A) \\
Rectified diodes \(D_1\&D_3\) & MBR20200CT (20A, 200V) \\
Main transformer \(T_1\) & Core: PQ3555, \(n=0.17\) \(L_{e1}=1.4\) mH \(L_{e2}=5.6\) \(\mu\)H \\
Main transformer \(T_2\) & Core: PQ3555, \(n=0.17\) \(L_{e1}=0.73\) mH \(L_{e2}=5.8\) \(\mu\)H \\
\hline
\end{tabular}
\end{table}
Fig. 12 Measured efficiency at $V_{in} = 385$ V.

voltage and the lagging switches are turned off with zero current under a wide range of load conditions.

Fig. 12 shows the measured efficiency at $V_{in} = 385$ V. As shown in Fig. 12, the maximum efficiency is about 95.69% at $I_o = 16$ A and the proposed converter can achieve higher conversion efficiency than the traditional PSFB converter under a wide range of load conditions. This is because the proposed converter can achieve wide ZVZCS operation, reduced output filter requirement and low oscillation voltage.

5. Conclusion

In this paper, a novel PSFB converter is proposed to overcome the problems of traditional PSFB converter. From the theoretical analysis results, it is worth noting that the proposed converter has the following advantages:

1) High voltage conversion ratio can be achieved and the oscillation amplitude of secondary voltage is well suppressed, which will contribute to the reductions of secondary voltage stress and primary conduction loss;

2) The leading switches are turned on with ZVS and the lagging switches are turned off with ZCS over a wide load range;

3) The primary power can be transferred to the secondary side during the whole switching period. This feature removes the primary circulating current and reduces the output filter requirement.

Due to these advantages, it is possible for the proposed converter to have higher efficiency than the traditional PSFB converter. An experimental prototype based on the proposed converter is built and the measured results coincide well with the theory analysis.

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