A Competitive Edge: Can FPGAs Beat GPUs at DCNN Inference Acceleration in Resource-Limited Edge Computing Applications?

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Abstract—When trained as generative models, Deep Learning algorithms have shown exceptional performance on tasks involving high dimensional data such as image denoising and super-resolution. In an increasingly connected world dominated by mobile and edge devices, there is surging demand for these algorithms to run locally on embedded platforms. FPGAs, by virtue of their reprogrammability and low-power characteristics, are ideal candidates for these edge computing applications. As such, we design a spatio-temporally parallelized hardware architecture capable of accelerating a deconvolution algorithm optimized for power-efficient inference on a resource-limited FPGA. We propose this FPGA-based accelerator to be used for Deconvolutional Neural Network (DCNN) inference in low-power edge computing applications. To this end, we develop methods that systematically exploit micro-architectural innovations, design space exploration, and statistical analysis. Using a Xilinx PYNQ-Z2 FPGA, we leverage our architecture to accelerate inference for two DCNNs trained on the MNIST and CelebA datasets using the Wasserstein GAN framework. On these networks, our FPGA design achieves a higher throughput to power ratio with lower run-to-run variation when compared to the NVIDIA Jetson TX1 edge computing GPU.

I. INTRODUCTION

Generative models are widely used as a means of parameterizing distributions of high-dimensional signals and structures. Among the various types of generative models, the Generative Adversarial Network (GAN) first proposed by Goodfellow \textit{et al.} \cite{goodfellow2014} yields superior performance on applications such as image generation, super-resolution, and language modeling \cite{ion2013}. The learning strategy of the GAN jointly optimizes a generator \(G\) and a discriminator \(D\). While the generator \(G\) is trained to minimize the distance between the ground truth distribution \(P_g\) and the model-parameterized distribution \(P_\theta\), the discriminator \(D\) is trained to separate \(P_g\) from \(P_\theta\). Although training optimizes both \(G\) and \(D\), only the generator \(G\) is needed for inference when drawing samples from \(P_\theta\).

The typical GAN framework shown in Fig. 1 involves convolution layers, where \(D\) is a Convolutional Neural Network (CNN) and \(G\) is a Deconvolutional Neural Network (DCNN). Traditionally, these networks are deployed on CPUs and GPUs using cloud computing infrastructures. However, the proliferation of applications for mobile and edge computing have created new opportunities to deploy these models on embedded hardware for local inference. In contrast to CPUs and GPUs, FPGAs offer large-scale fine-grained parallelism and provide consistent power-efficient throughput, making them well-suited for these edge computing applications \cite{michelmore2005}.

In this paper, we consider DCNN inference acceleration using a resource-limited Xilinx PYNQ-Z2 FPGA. We benchmark our implementation against the NVIDIA Jetson TX1 GPU, a processor heavily optimized for edge computing applications, and achieve a superior throughput to power ratio. The contributions of this paper are as follows:

- Significant enhancements over the algorithm proposed by \cite{choi2018} that reduce resource utilization, improve dataflow, and exploit memory hierarchy
- A spatio-temporally parallelized hardware architecture specifically designed to exploit these algorithmic innovations for power-efficient acceleration of DCNN inference
- An application of high-dimensional statistical analyses to balance the trade-off between hardware performance and generative quality when exploring network sparsity

II. RELATED RESEARCH

Previous works take architectural and algorithmic approaches to accelerating deconvolution workloads. The authors in \cite{wang2018} and \cite{liu2019} reformulate the deconvolution operation as a sparse convolution and build complex architectures that unify SIMD and MIMD execution models. Wang \textit{et al.} \cite{wang2018} also use the zero-insertion deconvolution algorithm, approaching the problem by parallelizing over a uniform 2D systolic array hardware architecture to accelerate both 2D and 3D DCNNs. Liu \textit{et al.} \cite{liu2019} propose a tiling method with a memory-efficient architecture that limits off-chip memory accesses at the cost of increased resource utilization via on-chip buffering. Chang \textit{et}
proposed an accelerator that transforms the deconvolution operation into a convolution (TDC), requiring \( \text{stride}^2 \) as many filters and potentially zero-padding the input and weight matrices. To improve dataflow, Tu et al. [21] explore the on-chip re-stitching of the disjoint output feature maps resulting from the TDC method. Mao et al. [16] adapt this method in a piecewise manner to handle the load-imbalance resulting from zero-padding at the cost of increased hardware complexity. The algorithm first proposed by Zhang et al. [26] avoids the zero-insertion and zero-padding requirements of the methods outlined above. We adapt this algorithm to a parallel hardware architecture as described in Sections III and IV.

III. DECONVOLUTION ALGORITHM

Standard deconvolution arithmetic traverses the input space, which requires a summation of regions that overlap in the output space [7]. When realized in hardware, accumulating over these overlapping regions can require complex dataflow and increase resource utilization via on-chip buffering [4], [14], [26]. To circumvent this, Zhang et al. [26] redesign the deconvolution algorithm to directly loop over the output space at the cost of the expensive modulo arithmetic required to calculate dependent input pixels. We propose the following three enhancements to adapt this reverse looping algorithm to a spatio-temporally parallelized hardware architecture.

1) Preprocessing modulo arithmetic. Standard deconvolution arithmetic calculates the indices of dependent output pixels \( o_h \) from input index \( i_h \) using weight index \( k_h \), stride \( S \), and padding \( P \), as shown in Eq. 1.

\[
o_h = i_h \times S + k_h - P
\]

To avoid this, Zhang et al. [26] use the mapping in Fig. 2 to loop over the output space and determine \( i_h \) using Eq. 2.

\[
i_h = \frac{a_h + P - k_h}{S}
\]

When \( S > 1 \), Eq. 2 yields fractional values. To ensure functional correctness, Zhang et al. [26] propose a stride hole skipping technique, adding an offset value \( f_h \) given by Eq. 3.

\[
f_h = \text{mod}(S - \text{mod}(P - k_h, S), S)
\]

However, the resulting input pixel calculation given by Eq. 4 relies on modulo arithmetic which increases resource utilization and power consumption when implemented in hardware.

\[
i_h = \frac{a_h + P - k_h + f_h}{S}
\]

Algorithm 1 Deconvolution Kernel. Each kernel loads inputs, weights, and offsets into local memory to compute each output block.

\[
y \leftarrow \text{initializeToBias}()
\]

\[
x \leftarrow \text{loadInputBlock}()
\]

\[
w \leftarrow \text{loadWeightBlock}()
\]

\[
\text{for } k_h = 0, k_h++, \text{ while } k_h < K \text{ do}
\]

\[
\text{for } k_w = 0, k_w++, \text{ while } k_w < K \text{ do}
\]

\[
w = w[k_h, k_w]
\]

\[
f_h = \text{loadOffset}(k_h)
\]

\[
f_w = \text{loadOffset}(k_w)
\]

\[
\text{for } o_h = 0, o_h++, \text{ while } o_h < T_{Oh} \text{ do}
\]

\[
o_h = o_h + f_h
\]

\[
o_w = o_w + f_w
\]

\[
i_h = \frac{(o_h + P - k_h)}{S}
\]

\[
i_w = \frac{(o_w + P - k_w)}{S}
\]

\[
y[o_h, o_w] \leftarrow w \times x[i_h, i_w]
\]

pushOutputBlock\(y\)

Observing that, in Eq. 3 \( f_h \) is only dependent on \( k_h \), we pre-compute and cache these offsets for each value of \( k_h \). This process reduces the number of modulo operations to \( 2K \), where \( K \) is the weight filter size. This minimizes resource utilization and on-chip memory as \( K \) tends to be small.

2) Dataflow Optimization. Loop interchange is an algorithm-level optimization that can be applied to improve the sequential computation order of operations [15]. We reorder the loops of the deconvolution arithmetic in [26] to sequentially traverse the weight space and maximize data reuse. Increasing weight-level data reuse also increases the impact of zero-skipping - a conditional execution paradigm that eliminates redundant operations by only processing non-zero elements.

Additionally, we exploit the opportunities for data-level parallelism exposed by directly looping over the output space. Unlike the standard deconvolution algorithm which suffers from the overlapping sum problem, the output space of the reverse looping deconvolution can be tiled into smaller batches to execute concurrently on a parallelized hardware architecture. When the size of the output feature space increases owing to the upsampling nature of deconvolution operations, the workloads and memory requirements remain constant, simplifying hardware design requirements.

3) Decoupling external memory accesses from compute operations. Reverse looping deconvolution arithmetic using [26] produces a non-sequential external memory access pattern over the input space. To mask any resulting overhead, we decouple all external memory accesses from compute operations to allow for the cascaded execution of these sub-tasks on a pipelined hardware architecture and restrict non-sequential memory access patterns to faster on-chip memory. This is done by first computing the pixel addresses of an input block using Eq. 4 then sequentially reading these addresses from external memory, and finally caching the data on-chip to be distributed. To do this, we determine the tile size \( T_{Oh} \) of the input block needed for each output block from the output space.
As discussed in Section IV, we design a spatio-temporally parallelized hardware architecture customized to accelerate the deconvolution algorithm proposed in Section III for low-power DCNN inference at the edge. Tiling factor $T_{OH}$ and the layer parameters using Eq. 5. The resulting deconvolution kernel given by Algorithm 1 can then continuously compute $T_{OH} \times T_{OW}$ output blocks with a non-sequential access pattern over locally cached $T_{IH} \times T_{IW}$ input blocks using $K \times K$ weight blocks as the next set of inputs are fetched from external memory using sequential reads.

$$T_{IH} = \max(i_h) - \min(i_h) = \left\lceil \frac{T_{OH}}{S} \right\rceil + \left\lceil \frac{K}{S} \right\rceil$$ (5)

IV. FPGA HARDWARE ARCHITECTURE

To accelerate DCNN inference on an FPGA, we design a SIMD (Single Instruction Multiple Data) hardware architecture with replicable compute units (CUs) that exploits the opportunities for both spatial and temporal data-level parallelism that arise from the optimizations discussed in Section III. As depicted in Figure 3, the dataflow of the deconvolution accelerator IP block is split into the three pipelined stages outlined below.

1. **Reading Inputs and Weights.** The limited amount of on-chip memory is a bottleneck when accelerating large networks on a resource-limited FPGA. As such, the input feature maps and network weights are stored in off-chip DDR memory and fetched using AXI interconnects. As described in Section III, decoupling external memory accesses masks the communication overhead when executed in a pipelined architecture. We separate input and weight external memory accesses into dedicated hardware blocks to concurrently read from DDR memory and stream to CUs through on-chip FIFOs. This efficient memory hierarchy is realized by on-chip buffers using BRAMs to store tiled input and weight blocks to be processed by CUs.

2. **Spatially Parallelized Compute Units.** Looping over the output feature map enables partitioning deconvolution arithmetic into tiled batches that can execute concurrently across an array of CUs. The CUs follow a SIMD execution model, where each workload is dependent on blocks of inputs and weights that are sequentially streamed in through FIFOs and accumulated. The CUs each perform the deconvolution arithmetic outlined in Algorithm 1 using on-chip DSP units and the resulting $T_{OH} \times T_{OW}$ output block is streamed out to be written to off-chip memory. To maximize the occupancy of these CUs, we explore the design space as outlined in Section V-A to optimize the output tiling factor.

3. **Writing Output Pixels.** Traversing the output space and avoiding the overlapping sum problem allows for a one-shot write to external memory for each output block computed by a CU. We dedicate a hardware block to stream the outputs from each element in the CU array to be written to external DDR memory. This minimizes communication overhead with DDR and on-chip BRAM memory requirements.

V. EXPERIMENTAL RESULTS

We implement our architecture on a Xilinx PYNQ-Z2 board at 32-bit fixed point precision using the Vivado Design Suite. With the available hardware resources, we synthesize the design with 16 CUs at 125MHz in Vivado HLS using HLSLIB [6] and benchmark performance on the two DCNNs depicted in Figure 4. Each DCNN is trained on the MNIST and CelebA datasets using the WGAN-GP [10] framework.

A. Design Space Exploration

In this work, we explore square tiling factors over the output space such that $T_{O_H} = T_{O_W}$ and use the design space exploration methodology proposed by Zhang et al. [25] to optimize $T_{O_H}$. Because our accelerator multiplexes through the DCNN layers, we optimize $T_{O_H}$ globally across all layers for each network architecture as a unified hardware design parameter as in [25]. Fig. 5 depicts all legal solutions for both the MNIST and CelebA DCNNs. Any solution to the left of the peak sustainable bandwidth slope requires a higher bandwidth than the FPGA can sustain [25]. The optimal $T_{O_H}$ (indicated in green) maximizes attainable throughput while satisfying the hardware constraints. Table I provides the values used in this work and the resulting FPGA resource utilization. Note that the Xilinx PYNQ-Z2 board is extremely resource-constrained,
using only 9% of the DSP blocks used in [23] and 5% of that used in [22] and [3].

B. Performance-per-Watt Comparison with Edge GPU

GPUs are power-hungry processors heavily optimized for large batch processing of on-chip memory [12]. Unlike the FPGA, which has been shown to provide workload-insensitive throughput with better power-efficiency, the time-varying optimizations leveraged by modern GPUs give rise to a non-deterministic execution model that can rarely provide the consistent performance that is required by edge computing applications [1], [13]. Additionally, modern GPUs use hardware throttling (ie. reducing clock frequency) to lower power and cool the chip when it gets hot, further increasing run-to-run variation [19]. This makes FPGAs the more suitable choice for edge computing applications when consistent throughput and power efficiency are key requirements [1].

In our experiments, we compare the throughput to power ratio of our Xilinx PYNQ-Z2 FPGA design against the heavily optimized NVIDIA Jetson TX1 edge computing GPU. As in [18], we evaluate the GPU with Torch using nvpprof to collect performance and power numbers for each layer in each DCNN. We measure FPGA power using a USB Power Meter Voltage Detector and collect performance numbers using hardware counters. We compute total network throughput as the sum of the arithmetic operations of all layers divided by the sum of the execution time of all layers. Our results provided in Table II show that our design yields a higher total network throughput to power ratio with lower run-to-run variation when compared to the GPU for both DCNNs. As noted in [25], unified design parameters such as $T_{Oh}$ simplify implementation cost but may be sub-optimal for some layers. We observe this behavior for the CelebA DCNN as shown in Table II. In future work, we will investigate dynamically reconfiguring tiling factors to optimize dataflow per layer.

C. Sparsity Experiments

Weight pruning is a widely studied technique used to reduce network power consumption and memory footprint on mobile and edge computing platforms [11]. It’s difficult for GPUs to effectively accelerate this form of unstructured sparsity as they are highly sensitive to conditional execution paradigms such as zero-skipping [1], [18]. Alternatively, FPGA performance is stable under such paradigms and can yield significant speed-ups when only executing non-zero valued computations [1]. [5]. Previous works optimizing DCNN dataflow for unstructured sparsity fail to account for this degradation [5].

In our experiments, we systematically prune DCNN weights by their magnitude as done in [11]. To visualize both hardware performance and generative quality, we analyze the rates of change of both system latency and Maximum Mean Discrepancy (MMD) distance, respectively. MMD distance is used to compute the dissimilarity between model-parameterized distribution $P_\theta$ and ground truth distribution $P_\theta$ and, in practice, is empirically estimated by drawing independent samples $\{x_1, \cdots, x_n\} \sim \mu$ and $\{y_1, \cdots, y_n\} \sim \nu$ from distributions $P_\theta$ and $P_\theta$, respectively, where kernel $k$ maps to a reproducing kernel Hilbert space [2], [9]. It follows that the MMD distance given by the equation below is zero if and only if the distributions are identical. Here, we explore the use of MMD with the standard Gaussian kernel $k(x, x') = \exp(\|x - x'|^2)$ using the Euclidean distance, selecting the median euclidean distance between ground truth samples as the bandwidth [9].
Pruning more weights yields higher speed-ups when skipping computations with zero-valued weights, as shown in Fig 6a. However, as shown in Fig 6b, the generative quality decreases with added sparsity. To balance the trade-off between hardware performance and generative quality, we propose an optimization metric given by Eq. 6. Here, $d_0$ and $d_p$ denote the execution time and MMD distance with respect $P_g$ using the full weight matrix $\theta_0$ while $t_p$ and $d_p$ denote that of the sparse matrix $\theta_p$ where $d_1$ is given by $\text{MMD}(P_g, P_{\theta_p})$. Multiplying the rate of change of system latency and MMD distance leads to a concave optimization curve with a peak representing the sparsity level that balances image quality with execution time.

$$\frac{d_0 - t_0}{d_p - t_p}$$  \hspace{1cm} (6)

### VI. Conclusions and Future Work

In this paper, we adapt the deconvolution algorithm first proposed in [26] to a parallelized execution model by reducing resource utilization, improving dataflow, and exploiting memory hierarchy. We design a spatio-temporally parallelized hardware architecture to accelerate this algorithm for DCNN inference on a Xilinx PYNQ-Z2 FPGA. For edge computing applications when consistent throughput and power efficiency are key requirements, we show that this resource-limited FPGA achieves a higher throughput to power ratio with lower run-to-run variation than the NVIDIA Jetson TX1 edge computing GPU. To balance the trade-off between generative quality and hardware performance, we propose a MMD-based optimization metric when exploring unstructured sparsity. In future work, we will adapt this architecture to other GANs and investigate the effect of bitwidth reduction on hardware performance and generative quality.

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