LDPUF: Exploiting DRAM Latency Variations to Generate Robust Device Signatures

B. M. S. BAHAR TALUKDER and BISWAJIT RAY, University of Alabama in Huntsville, USA
MARK TEHRANipoor and DOMENIC FORTE, University of Florida, USA
MD TAUHIDUR RAHMAN, University of Alabama in Huntsville, USA

Physically Unclonable Functions (PUFs) are potential security blocks to generate unique and more secure keys in low-cost cryptographic applications. Memories have been popular candidates for PUFs because of their prevalence in the modern electronic systems. However, the existing techniques of generating device signatures from DRAM is very slow, destructive (destroy the current data), and disruptive to system operation. In this paper, we propose latency-based (precharge) PUF which exploits DRAM precharge latency to generate signatures. Our proposed methodology for key generation is fast, robust, least disruptive, and non-destructive. The silicon results from DDR3 chips show that the proposed key generation technique is at least \( \sim 4,300 \times \) faster than the existing approaches, while reliably reproducing the key in extreme operating conditions.

CCS Concepts: • Security and privacy → Hardware security implementation; • Computer systems organization → Embedded and cyber-physical systems;

Additional Key Words and Phrases: DRAM-PUF, DRAM latency based PUF, robust key generation.

ACM Reference Format:
B. M. S. Bahar Talukder, Biswajit Ray, Mark Tehranipoor, Domenic Forte, and Md Tauhidur Rahman. 999. LDPUF: Exploiting DRAM Latency Variations to Generate Robust Device Signatures. ACM Trans. Web 999, 999, Article 999 (999), 22 pages. https://doi.org/0000001.0000001

1 INTRODUCTION
In recent years, the hardware security community has helped to shift industry’s attention towards the design of hardware-based security primitives to replace the more expensive and vulnerable software-based primitives. Hardware-based security primitives play important roles in protecting and securing the assets of an electronic system. Identification, authentication, secure communication, IC obfuscation to prevent IC piracy in semiconductor supply chain, detection of counterfeit ICs, etc. are common applications of hardware-based security primitives. Physical unclonable functions (PUFs), true random number generator (TRNG), and anti-counterfeiting are three of the most important hardware-based security primitives.

A PUF is a hardware-based security primitive capable of generating a unique identifying key [1]. Uniqueness is derived from physical variations inherent in the electronics manufacturing process such as resistances, capacitances, and transistor dimensions. These variations cannot be controlled during the manufacturing process and as such are considered unclonable [1, 2]. The security of a
PUF is dependent upon two major criteria (1) its inability to be replicated and (2) the inability to predict its secret key. Memory-based PUFs such as DRAM (the variant that will be investigated in this paper), SRAM, and Flash PUFs have the ability to reliably authenticate the system, in which it is embedded, by generating the same unique key upon request. This characteristic eliminates the need for additional circuitry which makes memory based PUFs a more cost-effective solution. This is the advantage that memory PUFs have over others such as the Arbiter and Ring-Oscillator PUF which require additional single-purpose circuits [2]. The purpose of a PUF is to generate the same key upon each access throughout the lifetime of the product as opposed to a True Random Number Generator (TRNG) which, as its name suggests, is meant to generate a purely random bit sequence upon access [2]. In order to create a memory based PUF, the most stable cells (reliably ‘1’ or ‘0’) across all operating conditions (temperature, voltage, and aging) need to be identified and enrolled into the secret key.

Reliability (how often a PUF can generate the same outputs over different environmental conditions through entire chip lifetime), uniqueness (how well a single PUF is differentiated from other PUFs), and randomness (the unpredictability of the PUF/TRNG outputs) are the standard metrics to quantify the quality of security primitives [3]. Like other silicon PUFs, a DRAM-PUF is capable of generating secret responses and/or cryptographic keys by exploiting inherent physical variations from the manufacturing process. As a circuit, however, DRAM-based PUF is impacted by voltage supply variation, temperature variation, and aging/wear-out as well [4–7]. Negative/positive bias temperature instability (BTI) and hot carrier injection (HCI) [8] can increase the delay of a device [9]. The operating temperature affects the delay of a device by changing its mobility and threshold voltage [10]. Consequently, the PUF output varies at different operating conditions and make the applicability of PUF less useful. While some applications can tolerate a certain amount of errors, others such as generation of cryptographic keys cannot. To make the PUF output more stable, (i.e., to obtain the same response for the applied challenge to a PUF) post-processing techniques such as error correcting code (ECC) and different enrollment schemes are often used [11–13]. All these approaches add to the overall footprint required by PUFs which is undesirable. Besides overhead, ECC schemes result in entropy loss and can also be attacked using side channel information [14]. Cell selection algorithm can be used to increase the reliability of a PUF but requires extensive post-processing [15, 16]. Therefore, many of these techniques are not suitable for high-volume production because the robust cells are unique from one memory chip to another. Previous work on DRAM PUFs has focused on using mainly two methods (1) writing all cells to ‘1’ and disabling the refresh then waiting for half the cells to discharge and reading cell values [2] and (2) using the startup values of the cells to generate the secret key as in [17]. Recently Kim et. al. [18] proposed a new DRAM based PUF by reducing activation time during the reading cycle. DRAM-based PUFs are far behind than SRAM and Flash based PUFs because of major limitations listed in Section 2.5. Waste of power cycle, substantial evaluation time, the destructiveness of the memory contents, and disruption of the system are primary reasons that an alternative is needed.

The objective of this paper is to propose a DRAM-PUF that exploits timing latency variations. The method used in this paper greatly reduces the time needed to acquire the PUF response. Our main contributions include:

- We explore the impact of the latency variation on DRAM operation and based on that, we characterize the flipped bits to select the best-suited DRAM cells for PUF operation.
- We propose a cell selection algorithm and a registration technique to generate robust and unique PUF response with reduced DRAM latency.
- We make a comparative analysis of our proposed technique with previously proposed DRAM based PUFs. The findings show that our proposed method outperforms all of them regarding...
robustness against voltage and temperature variation, evaluation time and system level integrity.

The rest of the paper is organized as follows. In Section 2, we present the background of DRAM architecture, read/write operation, existing DRAM-based PUFs and major challenges. We propose the latency-based DRAM PUF in Section 3. The experimental results and discussions are presented in Section 4. We conclude the paper in Section 5.

2 BACKGROUND AND MOTIVATION

In this section, we provide a brief background of the modern memory subsystem and its operation. We also present existing DRAM-based PUFs and the major obstacles to them in real low-cost applications.

2.1 DRAM Organization

For most of the modern computer system, DRAM servers the purpose of main memory. Fig. 1 illustrates the organization of a modern DRAM system. A modern DRAM system maintains a hierarchy of channel, rank, bank, DRAM chips, DRAM cells, and memory controller. Memory commands, address space, data are driven between the memory controller and DRAM modules by a memory channel. The memory requirement can vary from system to system which controls the total number of DRAM modules. A DRAM module is divided into one or multiple ranks. We access a rank in each attempt (reading/writing). Rank consists of several DRAM chips and provides a wide databus together. The same databus is shared among the ranks. A chip select pin is used to choose a particular rank. The width of the databus is usually 64 bits and distributed equally among the chips inside of a rank. Each DRAM chip consists of multiple banks to support the parallelism. In a memory bank, the DRAM cells are arranged in a two-dimensional array. The rows and columns of a DRAM are known as wordline and bitline respectively. The row of a DRAM is also known as the page. The bitlines are connected to the row-buffer (a row of sense-amplifiers). Sense-amplifier acts like a latch. When the DRAM is read, it senses the stored charge of each memory cell and latches the corresponding value. A DRAM cell is the smallest unit and used to store a single bit (‘1’ or ‘0’). The DRAM cell consists of two components- a capacitor to hold the charge and an access transistor to access the capacitor. The charging state of the capacitor determines the state of the value (‘1’ or ‘0’). Fully charged capacitor represents logic ‘1’ and empty capacitor represents logic ‘0’. The access transistor connects the capacitor with a bitline and is controlled by the wordline. The DRAM content (i.e., the state of charge in the capacitor) is read or overwritten by activating a wordline. An applied $V_{dd}$ to the wordline creates a path between the capacitor and bitline in order to perform read or write operation. For most of the modern DRAM, a specific combination of the row address and column address can access 64 bits (most common interface width) of data simultaneously by accessing multiple chips at a time.

2.2 DRAM Operation

2.2.1 READ Operation: Fig. 2i demonstrates the simplified DRAM read operation. In precharge state, the memory controller generates a PRECHARGE command (PRE). PRE command precharges all bitlines to $V_{dd}/2$ (green line) and deactivates previously activated wordline. In the next state (activation state), the ACTIVATE command (ACT) from memory controller activates the target wordline by raising the value of wordline to $V_{dd}$ (violet line). Once the pass-transistor (connected to the wordline) is ON, the charge flows from the capacitor (red line) to the attached bitline if the stored value is ‘1’ and moves from bitline to the capacitor if the stored value is ‘0’. In the final stage, the differential sense-amplifier senses the voltage perturbation on the bitline and amplifies the
bitline voltage to a strong logic ‘1’ (or ‘0’). Then, the sense-amplifier latches the logic value from the bitline. Finally, the appropriate column address decides, which sense-amplifier data should appear in the data bus. Reading operation in a DRAM is destructive. After a successful reading, the initial charged state of the capacitor must be restored to preserve its value.

2.2.2 WRITE Operation: In the DRAM write operation, initially all bitlines are precharged with the PRE command, and then, an ACT command is applied to activate the target wordline. Next, the target column’s sense-amplifier is driven to the desired logic value (high or low). This sense-amplifier with desired logic value enables the corresponding bitline to charge or discharge the connected storage capacitor. During WRITE operation, the activated wordline turns ON all access transistors to overwrite the contents of each associated cell. After each successful READ/WRITE operation, the bitlines must be again precharged to $V_{dd}/2$ to access the new set of memory cells from different wordline.

2.3 DRAM Timing
Timing is critical for reliable DRAM operation. All major timing parameters of a DRAM module are presented in Fig. 2ii. Initially, all bitlines are precharged to $V_{dd}/2$. To access the data from a specific wordline, ACTIVATE (ACT) command is applied to the corresponding wordline. After that, a READ/WRITE command is sent from the memory controller to sense the voltage perturbation on bitlines or to write a data to the memory cells. The minimum required time interval between ACT command and READ/WRITE command is defined as the activation time, $t_{RCD}$. The Column Access Strobe (CAS) latency $t_{CL}$ is the minimum waiting time to get the first data bit on data bus after sending READ/WRITE command. After a successful READ/WRITE operation, precharge command (PRE) is applied to deactivate the previously activated wordline (if any) and precharge the bitlines to its initial precharge state (i.e., to $V_{dd}/2$). If the WRITE command is applied, the PRE command should be further delayed for $t_{WR}$ period (write recovery time) at the end the write data burst. The PRE command is applied for at least $t_{RP}$ (precharge time) duration before sending the next ACT command. The time from activation state to the start of the precharge state is called row active time or restoration latency ($t_{RAS}$). The $t_{RAS} + t_{RP}$ is the total time required to access a single row of a bank and known as row cycle time ($t_{RC}$). Usually, the $t_{RC}$ is on the order of 50ns for most modern DDR3 DRAMs.

Without changing the DRAM architecture, although two rows cannot be activated at the same time, it is possible to read/write multiple columns in a single row cycle (i.e., activating one row and then reading/writing multiple columns of that row). A system can perform such kind of data access in Burst mode. In Burst mode, instead of accessing data only from specified memory address, multiple

Fig. 1. Organization of a modern memory subsystem [19], [20].
consecutive bitlines from the same wordline are accessed (usually 4 or 8 consecutive locations from the address requested by the memory controller).

The DRAM manufacturer provides the minimum required timing latency to perform a reliable read/write operation. We can expect erroneous read/write if the minimum timing latency is not maintained. It has been observed that, during the read operation, the failure to ensure the minimum \( t_{RCD} \), \( t_{RAS} \) and \( t_{RP} \) can lead to:

- **Observation 1**: A reduced \( t_{RCD} \) only affects the first accessed column/cache line.
- **Observation 2**: A reduced \( t_{RP} \) might affect almost all cells of a row.
- **Observation 3**: Almost no bit error is introduced at the reduced \( t_{RAS} \).

(i) Signal waveform at reading cycle. (ii) DRAM Timing at reading cycle.[20].

Fig. 2. DRAM operation and timing.

### 2.4 Existing DRAM-based PUF

#### 2.4.1 Retention-based DPUFs:

DRAM cells need to be refreshed with a periodic interval to ensure the integrity of the memory contents. The maximum allowed retention time is directly linked to the charge leakage across the memory cells of the DRAM module. The probability distribution of the charge leakage rate depends on several factors of the DRAM module such as:

- The manufacturing process variations on the charge storage capacity among the memory cells [5, 21].
- Operating voltage, temperature, and device wear-out. [5].

The DRAM contents need to be refreshed periodically before the cells lose their original value. According to the JEDEC standard, the refresh interval has to be 64ms/32ms [22] to ensure the data integrity against any hostile environment. Failing to refresh within this time interval can alter the memory contents. The increment of refresh interval by a sufficient margin will cause random data failure across the DRAM chips. This error pattern is unique from chip to chip and is used to generate device signatures.

The retention-based device signature is promising but suffers from several drawbacks. First, for most of the DRAM module, the periodic refresh operation is handled internally by a memory controller. There is no efficient way to control this refresh time for an arbitrarily small region of DRAM module as the granularity for such refresh operation is predefined by the vendors. An authentication key of sufficient length can be generated by retention failure from a small portion of a DRAM module, but the whole operation may cause unwanted data corruption of other memory cells under the same granularity [22]. Second, a key of sufficient length requires an adequate number of errors which might need a long waiting time (order of minutes) [18]. Third, the retention time is heavily temperature dependent. Therefore, the key is sensitive to temperature variations [15]. The bit error rate (BER) decreases exponentially with the temperature. i.e., at a lower temperature, the key generation scheme requires a longer time interval between two refresh operations. The required time to generate the key is also a function of the size of the memory segment. A smaller segment requires longer evaluation time than a bigger one [18]. Therefore, the designer must decide
on area vs. time overhead. Several techniques can be used to address above challenges but with limited scope \[4, 15, 21, 23–25\].

2.4.2 **Latency-based DPUFs**: We know from Section 2.3 that the reduction in different DRAM timing parameters introduces erroneous read/write operation. This latency-based failure creates the opportunity to generate faster device signature generation. The latency-based failure is random across the whole DRAM modules because of random process variations. Like other PUFs, the latency-based error pattern is unique from module to module. Recently, Kim et al. \[18\] proposed a DRAM PUF by manipulating the *activation* time \(t_{RCD}\). Like retention-based DPUF, the reduction of \(t_{RCD}\) introduces random errors across the whole chip which can be used to generate device signature. The evaluation time is much faster than the retention-based DPUFs. Their reported result shows that the mean evaluation time is \(\sim 88.2\) ms and outperforms all previously proposed retention-based DRAM PUFs \[15, 26, 27\]. However, the throughput is still low because multiple row cycles are needed to evaluate the PUF response. Furthermore, this type of latency based DPUF still needs a filtering mechanism in each access which adds both hardware and computational overhead.

2.4.3 **Other DPUFs**: In start-up based DPUF\[28\], the device signature is generated from the start-up states of DRAM cells. Initially, the bitlines are charged to \(V_{dd}/2\). But the process variations on the storage capacitor slightly deviates the *bitline* voltage and to \(V_{dd}/2 + \delta\) or \(V_{dd}/2 - \delta\), where \(\delta\) represents a small amount. The sense amplifier senses the voltage difference to ‘1’ or ‘0’ accordingly, which can be effectively used to generate device footprint. Recently, Hashemian et al. \[29\] performed Monte Carlo simulations and showed that a shorter duty cycle of the *write enable* signal might cause write failure randomly in DRAM memory cells and can be used to generate device signature.

2.5 **Motivations**

The major limitations of existing techniques for generating robust key form DRAM chips are summarized below.

- **Waste of DRAM Power Cycle**: Start-up based key generation requires a DRAM power cycle to obtain device signatures \[28\]. Hence, the whole system needs a turn-off and a turn-on to evaluate the PUF operation. Therefore, this type of PUF cannot be evaluated while the system is in operation.
- **Large Evaluation Time**: Retention-based key generation requires a large amount of time to generate a key. Order of minutes is required to generate enough retention failures \[15, 26, 27\]. Latency-based DPUF can be a superior solution, but the existing one still needs multiple row cycles (reading one data burst at each cycle) to evaluate the PUF key \[18\] as the reduction in activation time only affects the first few bits in the cache line (see Section 2.3).
- **Destructive**: Retention based key generation is destructive. The DRAM granularity causes random bit failure throughout the smallest granular region (usually a rank). Note that the DRAM refresh can be disabled only at the granularity of channels \[22\]. A dedicated memory might need to be used to overcome this problem, but it spoils the original no additional hardware advantage of memory PUFs. Like retention-based DPUF, the start-up based DPUF is also destructive.
- **Disruptive**: DRAM granularity keeps entire DRAM rank busy during each access from that rank. As the evaluation time of a retention-based DRAM PUF is the order of a minute, such kind of PUF evaluation blocks the access on the target DRAM region by other applications for a long time. Though the existing latency-based DRAM PUF \[18\] solves the problem of long evaluation time and unwanted data failure due to granularity, it still needs a filtering
mechanism to evaluate PUF in each access which introduces additional computational and hardware cost.

3 LDPUF

3.1 Generating Device Signature

In our proposed technique, we characterize the DRAM cells at the reduced $t_{RP}$ to find the most suitable cells for generating the quality signature. The latency is defined as the time required to move charge during read/write operation. In modern DRAM architecture, multiple DRAM cells are connected to the same bitline through access transistors. To access the memory cell properly, all bitlines should be precharged to $V_{dd}/2$. Like transistor and capacitor of a DRAM, the variations on RC path delay and the capacitance of the bitline follow the Gaussian distribution [30–32]. Due to this distribution, each bitline requires different $t_{RP}$ to be precharge itself properly. At reduced $t_{RP}$, partially precharged bitline may cause wrong logic interpretation in sense amplifier (as explained in section 2.2). Furthermore, a partially precharged bitline may interact differently with the memory cells which are connected to it. This phenomenon can be explained using Fig. 1ii. In the figure, the content of first and last memory cell connected to the bitline $B_1$, travel through the path of different length while sensing by the same sense amplifier. Hence, an insufficiently precharged bitline might impact differently with the memory cells that are connected to it. This bit error in read data due to random characteristics of bitlines can take part to generate the device signature.

In our proposed method, failure bits (i.e. do not consistently obey the original cell content) are generated by reducing $t_{RP}$ during read operation. We reduce the $t_{RP}$ to the smallest possible value to achieve (i) the maximum number of failed memory cells from each memory module and (ii) smallest possible time for PUF evaluation. However, during PUF evaluation, the reduced $t_{RP}$ should be kept sufficiently long enough to deactivate the previously activated wordline to suppress its impact on evaluated PUF.

3.2 Characterization

To obtain the robust and unique signature, we characterize the DRAM errors due to the reduced $t_{RP}$ (i.e., partial precharging). The characterization provides us valuable insight on DRAM cells and their eligibility for key generation. The characterization phase is conducted by observing the outputs with different types of input patterns (e.g., all 1’s, all 0’s or checkerboard pattern). A particular input pattern is applied for several times to study the temporal variation (i.e., measurement variation). Then based on the input pattern dependency (i.e., initially written data) and temporal variation, we categorize the cells into two major types:

- **Noisy Cells**: Error pattern varies from measurement to measurement for these type of cells. Internal/external noise can influence the outputs of these cells. Some of these cells can be useful to generate random number and rest of them can be used to create PUF but require a large ECC [33].

- **Robust Cells**: These cells do not show any temporal variation, i.e., cell outputs are independent of measurements. These cells are tolerant to internal and external noise and ideal for PUF.

The outputs at the reduced $t_{RP}$ might depend on the memory cell contents (i.e., written values) due to the coupling effect of neighborhood cells [34]. Based on the data dependency, we categorize the DRAM cells into two major types as well:

- **Pattern Independent Cells**: These type of cells exhibit the same output (at the reduced $t_{RP}$) regardless the patterns written into the memory. The experimental results show that (details
in Section 4) most of the DRAM cells from the major manufacturers are pattern independent. In this paper, we have only focused on pattern independent for PUF implementation.

- **Pattern Dependent Cells:** Pattern dependent cells respond differently with different input patterns. These cells can be the ideal candidates to create a strong PUF [35].

### 3.3 Cell Selection Algorithm

In this paper, we focus only on the pattern independent cells. Pattern-dependent cells are suitable for strong PUF which is our plan for future. The experimental results show that some of the pattern independent cells are strong ‘1’ and some of them are strong ‘0’. Besides the reproducibility, it is important that the generated key is random and unique as well. Entropy is used to measure the randomness of a bitstream [33, 36]. Entropy measures the number of zeros and ones in a bitstream. We scan each page to find the suitable cells for generating robust and random keys. We observe that the generated outputs using all pattern independent bits of every word (a word is 64 bits wide) suffer from poor entropy. Therefore, all bits of every word are not suitable for key generation. It is observed that some specific bits of every word of a page give a predictable outcome. For example, for a particular memory bank, the first bit of every word of a specific page always read as ‘0’ at reduced t_{RP}. Therefore, the binary string (V_i) from the first bits of the words cannot be used to generate keys. The hamming weight\(^1\) of the binary string V_i is 0%. A 50% of hamming weight, which is ideal for a key, means that the binary string has an equal number of 1’s and 0’s. Similar to V_i, we create a binary string V_2 with the second bit of each word in a page. Similarly, the binary string generated from the i^{th} bit of each word is V_i. The i^{th} bit of the word is considered as the eligible bit if it produces a random binary string V_i with a ~ 50% hamming weight.

To improve the entropy of our proposed LDPUF, we propose Algorithm 1 for selecting the qualified memory cells and their location. In practice, not all binary strings in \(\mathcal{V} = \{V_1, V_2, ..., V_{64}\}\) experiences a 50% of hamming weight. Therefore, we choose only those binary strings which fall into a range of allowable hamming weight (\(H_{\text{min}}\) to \(H_{\text{max}}\)). All eligible bits (of words) from a page \(\mathcal{R}_x\) can be defined as expression 1. If the page \(\mathcal{R}_x\) consists of \(n\) words, then we can create a binary string from each word by only accounting the qualified bits. For example, if we consider the i^{th} word \(W_i\) from page \(\mathcal{R}_x\), then, \(W_i^{\beta_{\mathcal{R}_x}}\) is a binary string by taking bits which are the elements of \(\beta_{\mathcal{R}_x}\). So, all allowable data bits from the \(\mathcal{R}_x\) can be presented as the expression 2. Here, \(\mathcal{M}_{\mathcal{R}_x}\) is a single dimensional binary string containing all eligible data bits from \(\mathcal{R}_x\).

\[
\beta_{\mathcal{R}_x} = \{b \in \{1, 2, 3, ..., 64\} : H_{\text{min}} < \text{hamming weight of } (V_b) < H_{\text{max}}\} \tag{1}
\]

\[
\mathcal{M}_{\mathcal{R}_x} = [W_1^{\beta_{\mathcal{R}_x}}, W_2^{\beta_{\mathcal{R}_x}}, W_3^{\beta_{\mathcal{R}_x}}, ..., W_n^{\beta_{\mathcal{R}_x}}] \tag{2}
\]

However, the length of the key can be larger than the number of qualified memory cells in a binary string \(\mathcal{M}_{\mathcal{R}_x}\). In this case, we will have to use more than one binary string from the multiple pages. Algorithm 1 is designed to select the qualified bits from each page. From now on to the rest of our discussion, the b^{th} bit of the 64 bits data word, accessed from the location (r,c), will be noted as (r,c,b) where, \(r\) is the row number (or page number), \(c\) is the column number (c^{th} word of the page \(r\)). In Algorithm 1, \(R_n\), \(C_n\), and \(B_n\) are the total number of rows, total number of columns, and the word width respectively (constant for a specific memory module). Note that in our experiment, we have used 1GB memory modules, where, \(R_n = 16384\), \(C_n = 1024\), and \(B_n = 64\).

In the proposed Algorithm 1, an one-dimensional array \(\mathcal{R}\) and a two-dimensional array \(\beta\) together hold the memory locations of the qualified DRAM cells. The \(\mathcal{R}\) holds all eligible row (or page) addresses and \(\beta\) holds corresponding qualified bit number of the page. For example, \(\mathcal{R} = 1, 3, 4, 7\)

---

\(^1\)The hamming weight is defined as the total number 1’s (or 0’s) in a bitstream.
represents that $1^{st}$, $3^{rd}$, $4^{th}$, and $7^{th}$ rows (or pages) are marked as the qualified rows (see Fig. 3). 2D array, $\beta$ (on right side) of the fig. 3 represents corresponding locations of the eligible bits. For example, for $R = 1$, the ‘2’, ‘5’ & ‘8’: i.e. $2^{nd}$, $5^{th}$ and $8^{th}$ bit of all words from page 1 can be used to generate key.

ALGORITHM 1: Selecting Qualified memory cells.

**Input:**
- $\text{mem\_data}$: A $R_n \times C_n \times B_n$ matrix, containing pattern independent data. An element of $\text{mem\_data}$ can be empty (if the corresponding memory cell is not pattern independent) or '0' or '1'.
- $H_{\text{min}}$ & $H_{\text{max}}$: Minimum and maximum allowable hamming weight as described in sec 3.3.

**Output:**
- $R$: 1D array, contains the list of qualified pages which holds qualified bits for PUF generation
- $\beta$: 2D array, $i^{th}$ row is associated with the $i^{th}$ page of $R$. Each row of $\beta$ contains all qualified bits from each word of the corresponding page.

1: $\beta = []$; // $\beta$ initialized with empty matrix
2: $R = []$; // $R$ initialized with empty matrix
3: $\text{bit\_count} = 0$;
4: $\text{row\_count} = 0$;
5: $\text{row\_flag} = \text{false}$;
6: for $r = 1$ to $R_n$ do
7:   for $b = 1$ to $B_n$ do
8:      $V_b = []$;
9:      $k = 0$;
10:     for $i = 1$ to $C_n$ do
11:        $\text{current\_mem\_data} = \text{mem\_data}(r, i, b)$;
12:        if $\text{is\_pattern\_independent}(\text{current\_mem\_data}) == \text{true}$ then
13:           $V_b(k) = \text{current\_mem\_data}$;
14:           $k = ++$;
15:        end if
16:     end for
17:     $h = \text{hamming\_weight\_of}(V_b)$;
18:     if $h > H_{\text{min}} \&\& h < H_{\text{max}}$ then
19:        $\text{row\_flag} = \text{true}$;
20:        $\beta(\text{row\_count}, \text{bit\_count}) = b$;
21:        $\text{bit\_count} += 1$;
22:     end if
23: end for
24: if $\text{row\_flag} == \text{true}$ then
25:    $R(\text{row\_count}) = r$;
26:    $\text{row\_count} += 1$;
27:    $\text{bit\_count} = 0$;
28:    $\text{row\_flag} = \text{false}$;
29: end if
30: end for

3.4 Registration

In the registration phase, we generate a golden data set (i.e. challenge-response dataset). The golden dataset can be used to generate the key or can be used to identify whether the DRAM chip is authentic or not. The golden dataset is created in a secure environment and stored in the database.
Using all qualified memory cells produced by the Algorithm 1, the golden data set is generated by the Algorithm 2. In this algorithm, the goldenDataLoc holds the logical locations of eligible memory cells and the goldenData saves the outputs that are accessed from the corresponding location with reduced $t_{RP}$. The goldenDataLoc, goldenData and the reduced value of $t_{RP}$ should be used as a golden data set for future authentication.

**ALGORITHM 2:** Generating Golden Data.

| Input:          |          |
|-----------------|----------|
| mem_data: A $R_n \times C_n \times B_n$ matrix, containing pattern independent data. An element of mem_data can be empty (if the corresponding memory cell is not pattern independent) or '0' or '1'. |          |
| $\beta$ & $\mathcal{R}$: generated from algorithm 1. |          |
| Output:         |          |
| goldenDataLoc: A boolean matrix of size $R_n \times C_n \times B_n$. goldenDataLoc(r,c,b) is true if corresponding memory cell qualified for the PUF application | goldenData: A matrix of size $R_n \times C_n \times B_n$, contains pattern independent output of those memory cells which are marked as true in goldenDataLoc matrix. |
| ALGORITHM 2: Generating Golden Data. |          |

1: goldenDataLoc = matrix_of_all_false ($R_n$, $C_n$, $B_n$) ;
2: goldenData = matrix ($R_n$, $C_n$, $B_n$) ;
3: for $i$ = 1 to length($\mathcal{R}$) do
4:   for $j$ = 1 to length($\beta$($i$, 1 to end)) do
5:     for $k$ = 1 to $C_n$ do
6:       current_mem_data = mem_data ($\mathcal{R}$($i$), $k$, $\beta$($i$, $j$)) ;
7:       if is_pattern_independent(current_mem_data) == true then
8:         goldenDataLoc ($\mathcal{R}$($i$), $k$, $\beta$($i$, $j$)) = true;
9:         goldenData ($\mathcal{R}$($i$), $k$, $\beta$($i$, $j$)) = current_mem_data;
10:    end if
11:   end for
12: end for
13: end for

4 RESULT AND ANALYSIS

Our results are based on experiments conducted with the commercial DDR3 memory modules from two major memory manufacturers (namely $A$ and $B$). We used SoftMC (Soft Memory Controller [37]) along with the Xilinx ML605 Evaluation Kit which is embedded with Virtex-6 FPGA. SoftMC uses Riffa [38] framework to establish communication between a host PC and the evaluation board through x8 PCIe bus. To check the design reliability against voltage variation, we used USB Interface

\[2\text{Manufacturer } A: 	ext{ Micron} \]
\[2\text{Manufacturer } B: 	ext{ Samsung} \]
Adapter Evaluation Module [39]. This Evaluation Module provides precise voltage control of the power rail directly connected to the memory module.

The experiment was performed in two steps. First, an 8-bit pattern was written with nominal timing parameter and then read it back with reduced timing parameter. The reading operation was done in a single row cycle, i.e., we activated one wordline at a time and then, read all bitlines with consecutive burst, where, each data burst was able to capture the data from successive 8 bitlines. This whole process was done at the nominal operating voltage and room temperature. The pattern length was chosen according to the burst length of the memory module. To evaluate the error pattern, we first checked the Hamming Distance between the written pattern (input pattern) and the pattern that was read out (output pattern) with reduced timing parameter. Then, flipped bits were analyzed for additional information (e.g., spatial distribution, pattern dependency, etc.). Four sets of 8-bit input pattern (0xFFFF, 0xAAAA, 0x5555, 0x0000) were used to characterize the DRAM cells. For each set of the input pattern, we repeated our experiment five times to study the temporal variation. Independent analysis is done by choosing random memory banks (three from manufacturer A and two from B; each consists 128MB memory cells).

We conducted our experiment on DRAM memory module by changing the activation time ($t_{RCD}$), restoration time ($t_{RAS}$), and precharge time ($t_{RP}$). However, we did not observe any data error due to reduced $t_{RAS}$ which is consistent with the observation made by [20]. We characterized flipped bits which is the result of the reduced $t_{RP}$.

### 4.1 Reduced Latency: Activation Time vs. Precharge Time

We read a whole memory page in a single row cycle to evaluate the error patterns generated at the reduced $t_{RCD}$. Two 32-byte (double-data rate) memory chunks were read with each burst (with 8-bit burst length, i.e., eight words can be accessed at a time while each word corresponds to 64-bit data). From now on to rest of our discussion we will use the notation $t_{A,x}$ to presents the reduced timing parameter $t_A$, where $t_{A,x} = x \times t_A$. At reduced activation time (e.g., at $t_{RCD,0.38}$), flipped bits were only observed at the first accessed cache line (i.e., in the first 64-byte data). As the DRAM-based PUFs rely on flipped bits at non-standard DRAM operation, to evaluate DRAM based PUF at reduced $t_{RCD}$ needs multiple reading cycles (by accessing 64-byte data in each cycle). All memory banks from both manufacturers exhibited similar characteristics. Such behavior is observed because the target wordline gets enough time to get fully activated before accessing the second content of the cache line (see appendix A). Note that, [20] and [18] also presented similar observation. In our experiment, reduced activation latency-based error was first observed at $t_{RCD,0.57}$.

On the other hand, the experimental results show that excessively reduced $t_{RP}$ flips memory cells and affects uniformly while we read the whole page in a single row cycle. Fig. 4 shows the percentage of flipped bits in two random banks from two manufacturers at reduced $t_{RP}$ and with different input patterns. The bit flipping was first observed when the $t_{RP}$ is reduced to $t_{RP,0.57}$. With the sufficient reduction in $t_{RP}$, the bitlines do not get enough time to settle themselves to $V_{dd}/2$ form their previous states and, therefore, float into an intermediate value [4, 20]. We reduced the $t_{RP}$ to $t_{RP,0.57}$, $t_{RP,0.38}$, and $t_{RP,0.19}$ to observe the behavior of erroneous outputs. The results show that, for manufacturer A, the total number of flipped cells are $\ll 1\%$ at $t_{RP,0.38}$. The number of flipped cells keep increasing as we keep decreasing the $t_{RP}$. The total number of errors increase by a huge margin at $t_{RP,0.19}$. For vendor B, the total number of flipped cells are $\ll 1\%$ at $t_{RP,0.57}$ but increase significantly at $t_{RP,0.38}$. The pattern dependency of flipped bits count is also noticeable in Fig. 4. At $t_{RP,0.19}$, for manufacturer A, the number of flipped cells (flipped to ‘0’) for the input pattern 0xFFFF (all 1’s) is 75.17%. On the other hand, only 25.01% memory cells are flipped (flipped to ‘1’) for input pattern 0x00 (all 0’s). With checker board pattern (i.e., 0xAAAA & 0x5555), the number of flipped cells is $\sim 50\%$. This is because, for vendor A, at $t_{RP,0.19}$, most of the memory cells produce ‘0’,
regardless of the input pattern. We found similar observation for all memory banks from vendor $B$, for which, most of the memory cells produce 1 with the partially precharged bitlines. Fig. 4 also shows that, for vendor $B$, the statistics of the flipped cells are almost similar at $t_{RP,0.19}$ and $t_{RP,0.38}$.

![Fig. 4. $t_{RP}$ vs % of flipped bits- (i) from manufacturer $A$, (ii) from manufacturer $B$, Horizontal axis is shown in logarithmic scale.](image)

We can conclude from the results that reducing precharge time is superior to the reducing activation time for generating quality keys in a single row cycle. The results show that we can have enough errors at $t_{RP,0.19}$ to obtain PUF keys.

4.2 Cell Characterization

We characterize the DRAM cells to improve the quality of the generated device signatures. We read either the right contents or the flipped of the original contents in a DRAM due to the partial precharging. We characterized the DRAM cells based on their response to the partial precharging state. We studied whether the memory cell content read at partial precharge state is dependent on its content and the contents of neighbor cells. We investigated the spatial correlation in the error pattern. It was found that some of the cells are noisy compared to the other cells at the reduced $t_{RP}$. To characterize memory cells based on their output patterns, we collected data at $t_{RP,0.57}$, $t_{RP,0.38}$ and $t_{RP,0.19}$. However, we characterize DRAM cells only at $t_{RP,0.19}$, so that, we can generate the maximum number of flipped bit for the PUF operation. Note that, cell characterization was done at nominal voltage and room temperature.

![Fig. 5. Spatial Location of pattern Independent cells- (i) bit ’0’, (ii) bit ’1’.](image)

![Fig. 6. Pattern Dependent cells, (i) flipped to ’0’, (ii) flipped to ’1’.](image)
(1) **Pattern Independent**: Memory cells from this category always get flipped to a fixed value (either to '0' or to '1') regardless of the input pattern (i.e., originally written value to the DRAM cells). Fig 5 shows the spatial locations of output '0' (left) and '1' (right) across a random DRAM bank from manufacturer A. The results show that pattern independent 1’s and 0’s are uniformly distributed. All memory banks from manufacturer B also showed the similar type of uniform spatial distribution (not shown in the figure). Therefore, the reduction of $t_{RP}$ is very useful to obtain responses for PUF.

(2) **Pattern Dependent**: The outputs of these type of cells depend on the input patterns written to the DRAM cells. The outputs are affected by the cumulative voltage of partially precharged bitline, stored values, and the coupling effect of neighbor cells. We consider a memory cell as pattern dependent if it provides different outputs for different inputs and shows measurement invariance for at least one input pattern. Fig. 6 shows the DRAM cells which are dependent on input patterns 0xAA. Pattern dependent cells can be used for strong PUF with a large challenge-response pair (CRP) space. Furthermore, spatial locality along both row and column are visible in Fig. 6. Darker line in the Fig. 6 (both horizontal and vertical) represents rows and columns with the higher number of pattern dependent cells. The spatial locality might be used to get the physical to logical address mapping [25]. Fig. 6 is captured from a random bank of manufacturer B, a similar type of spatial locality was found in all memory banks from all manufacturer. The third column (from right) in Table 1 shows the percentage of pattern dependent cells from each bank.

(3) **Noisy Cells**: With partially precharged bitlines, outputs of these cells varies from measurement to measurement. Therefore, these noisy cells are not suitable to be used as PUF. The second column (from right) in Table 1 represents the percentage of noisy cells from each bank. Fig. 7 shows the distribution of noisy memory cells for a random bank from the manufacturer B. This figure shows that the noisy cells are not entirely random (in this case, most of the cells are biased to '1'). Similar characteristics are found in other memory banks from both manufacturers (i.e. most of the noisy cells are biased to either '0' or '1'). Large ECC might be required to use these cells as PUF [11], [12]. The locations of noisy cells from a bank to another are random. However, a proper subset of such kind of cells can also be used to generate the random number which is beyond the scope of this paper.

![Fig. 7. Noisy Cell Characteristics. Most of the cells are biased to '1'.](image_url)

![Fig. 8. Cell Distribution among the bitlines.](image_url)

The complete distribution of these three types of DRAM cells is presented in Fig. 8 for a given bank of vendor A. In this figure, we only presented two consecutive data words ($64 \times 2 = 128$ bitlines) from each page. The figure shows that all memory cells from $4n^{th}$ and $(4n + 1)^{th}$ (where, $n = 1, 2, 3, \ldots$) bit of the word generate '0' regardless of the input patterns. One of the possible reasons is that these bitlines are deviated toward '0' (from $V_{dd}/2$) by a huge margin due to the
insufficient $t_{RP}$. Therefore, generation of the key from such memory cells reduces the overall entropy of the key. Our proposed Algorithm 1 is designed to eliminate such memory cells.

Table 1 summarizes the distribution of the cells for two different manufacturers (manufacturer A, and manufacturer B) at $t_{RP,0.19}$. The results show that more than 90% cells from each bank of manufacturer A are pattern independent while it is < 75% for the manufacturer B. For both manufacturers, the number of pattern dependent cells is less than 1%. The rest of them are noisy cells. Note that, a very small number of cells from manufacturer B, presented in the first column (from right, marked as ‘Correct bits’) of the table, were able to retain their actual stored data even at $t_{RP,0.19}$ with all input patterns.

| Manufacturer | Memory Bank ID | Pattern Independent 0 (%) | Pattern Independent 1 (%) | Pattern Dependent (%) | Noisy (%) | Correct bits (%) |
|--------------|----------------|---------------------------|---------------------------|----------------------|-----------|-----------------|
| A            | a              | 85.825                    | 12.631                    | 0.006                | 1.537     | 0               |
|              | b              | 72.663                    | 18.790                    | 0.135                | 8.413     | 0               |
|              | c              | 72.793                    | 17.202                    | 0.133                | 9.872     | 0               |
| B            | a              | 8.226                     | 63.674                    | 0.519                | 27.580    | 0.001           |
|              | b              | 6.339                     | 53.530                    | 0.113                | 40.017    | 0.001           |

Table 1. Distribution of memory cells based on characteristics at partial Precharge state.

4.3 LDPUF Evaluation:

Diffuseness, Uniqueness, and Reliability are three major PUF performance metrics.

- **Diffuseness**: PUF device should be able to generate distinguishable responses with different challenges. For LDPUF, we consider the address as the challenge and corresponding cell content at reduced $t_{RP}$ as the response.
- **Uniqueness**: Response from different device should be unique.
- **Reliability**: Same response (i.e., PUF output) should be generated to its entire lifetime at any operating condition.

Table 1 shows that the pattern-independent cells are dominant across all memory banks for both manufacturers. In this paper, we have focused only on the pattern independent cells. We used the Algorithm 1, presented in Section 3 to obtain the logical locations of the qualified memory cells. In this algorithm, we used $H_{min} = 0.25$ and $H_{max} = 0.75$ as the input parameters. Ideally, the Hamming distance should be 0.5. A Hamming distance of 0 represents that the PUF is not unique. We completed the registration (i.e., creating the golden data set) using our proposed Algorithm 2. We generated at least one 1024-bit key from each qualified page (or row). However, it is possible to generate multiple keys from each page since the number of qualified memory cells from each page was more than 1024. For the simplicity, we obtained only one key from each page to test the PUF performance. The key generated from the golden data set is used as the reference key. We refer the corresponding address for generating a reference key as the key address. To evaluate the performance of our proposed LDPUF, we created four set of test data in four different operating conditions (will be discussed in 4.3.3). Each test set contains the output data with four different input patterns: $0xFF$, $0xAA$, $0x55$, and $0x00$. From now on to the rest of the discussion, all results are shown combinedly for all four inputs patterns otherwise it is specified. The outputs at different operating conditions are compared with the reference key to ensure the robustness of our proposed key generation methodology. We present the major performance metrics below.
4.3.1 **Diffuseness:** To check the diffuseness, we measured inter Hamming Distance (inter HD) among the reference keys from each bank (i.e., intra-bank but inter-reference key). A 50% of inter HD signifies that a single device can generate unique keys from each row (i.e., address). The average Hamming weight of 50% also represents that the keys are random. Table 2 shows the average Hamming weight of each key and average Hamming distance among the different keys generated from each bank. The average hamming weight and hamming distance for the banks from manufacturer A are more close to the ideal value (i.e., 50%). Though the average HD and Hamming weight for manufacturer B deviates from 50%, still we did not find any repetition of keys that are generated from a distant page of the same memory bank.

Table 2. Average Hamming weight and Hamming Distance among the key generated from each Bank.

| Manufacturer | Memory Bank ID | #Qualified page (%) | Average Hamming Distance (%) | Average Hamming Weight(%) |
|---------------|----------------|---------------------|-----------------------------|---------------------------|
| A             | a              | 100.00              | 48.87                       | 54.23                     |
|               | b              | 92.31               | 49.35                       | 53.29                     |
|               | c              | 92.30               | 49.24                       | 49.24                     |
| B             | a              | 74.84               | 42.28                       | 68.19                     |
|               | b              | 63.99               | 38.06                       | 70.31                     |

4.3.2 **Uniqueness:** To quantify the uniqueness, we measured the inter Hamming Distance (inter HD) of the key from different memory banks. i.e. we measured the HD between the two keys of two banks generated from each key address. We have checked inter HD for all possible combination by taking account all five banks. Fig. 9 shows the inter HD from each manufacturer. This figure only represents the worst case (largest deviation from 50% inter HD) scenario of both manufacturers. For the manufacturer A, the average, minimum, and maximum inter HD are 45.78%, 37.05%, and 52.5% respectively. For the manufacturer B, the mean, minimum, and maximum inter HD are 51.91%, 40.92%, and 72.23% respectively. The above results conclude that the key generated from the proposed LDPUF is unique.

![Fig. 9. Inter Hamming distance for the worst case from (i) manufacturer A, (ii) manufacturer B.](image-url)
4.3.3 Reliability: The reproducibility at different operating conditions is presented in Fig. 10. This figure only presented the worst memory bank from each manufacturer (i.e. memory bank with the largest deviation from 0% intra HD). We collected results at four different operating conditions: (i) Nominal Voltage and Room Temperature (NVRT), (ii) Low Voltage and Room Temperature (LVRT), (iii) High Voltage and Room Temperature (HVRT), and (iv) Nominal Voltage and High Temperature (NVHT). These operating conditions were chosen to examine the impact of voltage variation and high temperature. Throughout the experiment, we have only measured the external temperature (environment temperature). The result shows that the memory module from manufacturer A less robust than the manufacturer B in reduced operating voltage. For manufacturer A, we can only change the operating voltage by \(-20\text{mv}\) without causing an excessive error. On the other hand, the DRAM module from manufacturer B can tolerate \(-75\text{mv}\) change in operating voltage. Table 3 presents the intra HD under different operating conditions. Column 4 of Table 3 represents the change in operating voltage from the nominal operating voltage (1.5v), and column 5 represents the change in temperature from room temperature (25°C). The results show that all memory banks from both manufacturers are robust against the temperature variation.

![Fig. 10. Intra HD for the worst case from- (a) manufacturer A, (b) manufacturer B with (i) NVRT, (ii) LVRT, (iii) HVRT, (iv) NVHT.](image)

4.4 Performance Comparison

4.4.1 Evaluation Time: The Evaluation Time is the time between we send the READ command to the system and we receive the required amount of data to generate 1024-bit key from the system. Table 4 shows the required number of data bursts (mean) and time (mean and standard deviation) to generate 1024-bit key. The result shows that in the proposed technique, on average, we need < 2 ms to obtain a 1024-bit key which is much faster than the existing approaches. We observe that the longest time to evaluate LDPUF is \(\sim 3.97\text{ms}\). However, the evaluation time is shown in table 4 also includes the required time to transfer the data in between the host PC and evaluation board. With our proposed technique, the experimental result shows that the average system level evaluation time is \(\sim 6.7\mu\text{s}\) for manufacturer A and \(\sim 20.5\mu\text{s}\) for manufacturer B. Note that, on average it required \(\sim 91.2\mu\text{s}\) to access the whole 8KByte page in a single row cycle.

Note that in our proposed algorithm, we used only the pattern independent cells at reduced \(t_{RP}\). Hence, we don’t need to write any explicit data for PUF evaluation. The average system level evaluation time of reduced \(t_{RCD}\) based DPUF is 88.2ms [18] which is still \(\sim 4,300\times\) worse
Table 3. Intra HD at different operating conditions.

| Manufacturer | Memory Bank ID | Operating Codition | Mean Intra HD (%) | Standard Deviation (%) | % of Key with Intra HD >1% | % of Key with Intra HD >30% |
|--------------|----------------|-------------------|-------------------|------------------------|---------------------------|--------------------------|
| A            | a              | NVRT -20 0        | 0.48              | 0.07                   | 0                         | 0                        |
|              | b              | LVRT +20 0        | 0.07              | 0.09                   | 0                         | 0                        |
|              | c              | HVRT +20 0        | 0.06              | 0.09                   | 0                         | 0                        |

Table 4. Average LDPUF Evaluation time.

| Manufacturer | Memory Bank ID | #Required Data Bursts (mean) | Mean Evaluation time (ms) | Standard Deviation (ms) |
|--------------|----------------|-------------------------------|---------------------------|-------------------------|
| A            | a              | 9.00                          | 0.31                      | 0.12                    |
|              | b              | 6.43                          | 0.25                      | 0.08                    |
|              | c              | 7.19                          | 0.29                      | 0.10                    |
| B            | a              | 28.15                         | 1.16                      | 0.27                    |
|              | b              | 24.18                         | 1.04                      | 0.23                    |

4.4.2 System Level Disruption: For most of the DRAM chips, the granularity of refreshing the DRAM contents is rank. Therefore, we need to increase the refresh interval for entire memory rank during retention-based PUF evaluation. Hence, it causes random data corruption over the whole rank. Also, due to the long evaluation time of the retention based PUF, the particular DRAM rank become unavailable for other applications for a long time. For our proposed LDPUF, the reduced \( t_{RP} \) only affects those cells which are being accessed. Furthermore, we also checked the
interference to the neighborhood pages of the target page that is being accessed for key generation. To do so, we arbitrarily selected consecutive 1000 rows from each memory bank at nominal voltage and room temperature. Then, at first, we read the data from all odd-numbered rows with the reduced $t_{RP}$ and after that checked the impact on the memory cells of the even-numbered row with nominal $t_{RP}$. Our results show that there is no data corruption in the adjacent rows.

However, though the latency based DPUF [18] with reduced $t_{RCD}$ solves the problem of long evaluation time by a significant margin, this type of DPUF evaluation needs a filtering mechanism upon each access which causes both computational and hardware overhead. In our proposed mechanism, determination of eligible PUF cells by cell characterization is required to be done only once on entire DRAM lifetime (see section 3.3). Once the suitable cells for PUF operation are determined, the evaluation of our proposed PUF is straightforward (i.e. request the response by sending an address and then compare only the eligible cells’ content with the golden data). Furthermore, our proposed PUF evaluation has least evaluation time which ensures the smallest stall to the system.

Therefore, our proposed LDPUF can be used in run-time which cannot be performed in many existing memory-based PUFs [2, 15, 26].

4.4.3 Robustness: We compared the robustness between our proposed LDPUF and retention-based DPUF in different operating conditions. To accumulate the retention based failure, we chose a memory segment containing 1000 rows from each bank. At first, we stored logic ‘1’ to all memory cells under the segment and then refresh interval was prolonged till we get at least $\sim 2\%$ failure at NVRT. For a specific bank, same refresh interval was kept for all operating conditions. For the proposed LDPUF, we measured bit failure with four input patterns ($0xFF$, $0xAA$, $0x55$, and $0x00$) at $t_{RP,0.19}$ for the same 1000 rows. The Jaccard Index is used to compare the robustness of our proposed LDPUF with the retention-based PUF. For the retention-based DPUF, the PUF characteristics are evaluated from the location of flip bits. For example, in our case, retention-based failure bits are always flipped from logic ‘1’ to logic ‘0’. But the location of the flipped cells differs from one device to another. For the two set of the measurements ($M_1$, $M_2$), Jaccard Index is measured as $\frac{M_1 \cap M_2}{M_1 \cup M_2}$, where $M_1 \cap M_2$ is the total matched failed bits and $M_1 \cup M_2$ is the total failed bits from two measurements $M_1$ and $M_2$ [18, 40]. For better reproducibility, the intra Jaccard Index should be $\sim 1$. Table 5 shows the comparison between LDPUF and retention-based PUF. The results show that the proposed LDPUF is more robust than retention-based DPUF. The retention-based PUF is more vulnerable to the temperature variation compared to the LDPUF. This is because the retention-based bit failure is mostly emphasized by the charge leakage rate of DRAM cells which has a strong exponential dependence on the temperature [15, 26, 27, 41, 42]. On the other hand, the change in $t_{RP}$ is very negligible as temperature changes. The $t_{RP}$ changes only ($\sim 3\%$) as temperature changes from 27°C to 85°C [43].

Though we did not evaluate the LDPUF with reduced $t_{RCD}$, the result shown in [18] implies that it can tolerate only a small change in temperature (e.g., 5°C). On the other hand, for the LDPUF based on our proposed method, we observed only a negligible difference in robustness after increasing the temperature by 20°C. The result presented in [43] also suggests that the temperature dependency of $t_{RCD}$ is stronger than the temperature dependency of $t_{RP}$.

5 Conclusion

In this paper, we characterized DRAM cells based on data failure due to partially precharged bitlines in reading cycle. Throughout the experimental evaluation, we used total five commercial off-the-shelf 128MB DDR3 memory banks. We showed that most of the data latched at sense-amplifier are independent of the original content of the memory cells when the bitlines are precharged partially.
Based on this pattern independent data, we proposed LDPUF which can be evaluated in much shorter time (at least $\sim 4,300X$ shorter) compared to the fastest DPUF that is available till now. We also provided experimental evidence that showed, our proposed method has less system interference and higher robustness against different operating condition compared to the other DRAM based PUF. We conclude that our proposed partial precharged based DRAM PUF will provided much faster authentication to the run-time application with smaller system overhead. We also believe that, different characterization information that we provided, can be used to generate other security primitives such as Random number, strong PUFs and to expose the internal architecture of DRAM itself.

ACKNOWLEDGMENT
We thank ETH Zürich & CMU for the SoftMC software.

REFERENCES
[1] Charles Herder, Meng-Day Yu, Farinaz Koushanfar, and Srinivas Devadas. 2014. Physical Unclonable Functions and Applications: A Tutorial. Proceedings of the IEEE 102, 8 (2014), 1126–1141. DOI:http://dx.doi.org/10.1109/jproc.2014.2320516
[2] Christoph Keller, Frank Gurkaynak, Hubert Kaeslin, and Norbert Felber. 2014. Dynamic memory-based physically unclonable function for the generation of unique identifiers and true random numbers. 2014 IEEE International Symposium on Circuits and Systems (ISCAS) (2014). DOI:http://dx.doi.org/10.1109/iscas.2014.6865740
[3] Md. Tauhidur Rahman, Domenic Forte, Jim Fahrny, and Mohammad Tehranipoor. 2014. ARO-PUF: An Aging-Resistant Ring Oscillator PUF Design. Design, Automation & Test in Europe Conference & Exhibition (DATE), 2014 (2014). DOI:http://dx.doi.org/10.7873/date2014.082
[4] Kevin K. Chang, A. Giray Yaşlıköç, Saugata Ghose, Aditya Agrawal, Niladrish Chatterjee, Abhijith Kashyap, Donghyuk Lee, Mike O’Connor, Hasan Hassan, and Onur Mutlu. 2017. Understanding Reduced-Voltage Operation in Modern DRAM Devices: Experimental Characterization, Analysis, and Mechanisms. Proc. ACM Meas. Anal. Comput. Syst. 1, 1, Article 10 (June 2017), 42 pages. DOI: https://doi.org/10.1145/3084447
[5] Karthik Chandrasekar, Sven Goossens, Christian Weis, Martijn Koedam, Benny Akesson, Norbert Wehn, Kees Goossens. 2014. Exploiting Expendable Process-Margins in DRAMs for Run-Time Performance Optimization. Design, Automation & Test in Europe Conference & Exhibition (DATE), 2014 (2014). DOI:http://dx.doi.org/10.7873/date.2014.186
[6] Donghyuk Lee, Samira Khan, Lavanya Subramanian, Saugata Ghose, Rachata Ausavarungnirun, Gennady Pekhimenko, Vivek Seshadri, Onur Mutlu. 2017. Design-Induced Latency Variation in Modern DRAM Chips. Proceedings of the 2017 ACM SIGMETRICS / International Conference on Measurement and Modeling of Computer Systems - SIGMETRICS 17 (Abstracts). DOI:http://dx.doi.org/10.1145/3078505.3078533

[7] Fatemeh Tehranipoor, Nima Karimian, Wei Yan, and John A. Chandy. 2017. Investigation of DRAM PUFs Reliability under Device Accelerated Aging Effects. 2017 IEEE International Symposium on Circuits and Systems (ISCAS) (2017). DOI:http://dx.doi.org/10.1109/iscas.2017.8050629

[8] Kangil Kim, Ilsub Chung, Duan Sun, Sangjae Rhee, Igweon Kim, Hongsun Hwang, Kangyong Cho, Gyoyoung Jin. 2016. Study on Off-State Hot Carrier Degradation and Recovery of NOSMFET in SWD Circuits of DRAM. 2016 IEEE International Integrated Reliability Workshop (IRW) (2016). DOI:http://dx.doi.org/10.1109/irw.2016.7904910

[9] Dinesh Ganta and Leyla Nazhandali. 2014. Study of IC Aging on Ring Oscillator Physical Uncloneable Functions. Fifteenth International Symposium on Quality Electronic Design (2014). DOI:http://dx.doi.org/10.1109/isqed.2014.6783360

[10] Md. Hasanuzzaman, Syed K. Islam, and Leon M. Tolbert. 2004. Effects of temperature variation (300–600 K) in MOSFET modeling in 6H–silicon carbide. Solid-State Electronics 48, 1 (2004), 125–132. DOI:http://dx.doi.org/10.1016/s0038-1101(03)00293-4

[11] Matthias Hiller, Dominik Merli, Frederic Stumpf, and Georg Sigl. 2012. Complementary IBS: Application Specific Error Correction for PUFs. 2012 IEEE International Symposium on Hardware-Oriented Security and Trust (2012). DOI:http://dx.doi.org/10.1109/hst.2012.6224310

[12] Srinivas Devadas and Meng-Day Yu. 2015. Secure and Robust Error Correction for Physical Uncloneable Functions. IEEE Design & Test (2015), 1–1. DOI:http://dx.doi.org/10.1109/mdt.2009.163

[13] Jung Rae Kim, Michael Sullivan, Seong-Lyong Gong, and Mattan Erez. 2015. Frugal ECC: Efficient and Versatile Memory Error Protection through Fine-Grained Compression. Proceedings of the International Symposium on High Performance Computing, Networking, Storage and Analysis on - SC 15 (2015). DOI:http://dx.doi.org/10.1109/sc15.2807591

[14] Soubhagya Sutar, Arnab Raha, Devadatta Kulkarni, Rajeev Shorey, Jeffrey Tew, and Vijay Raghunathan. 2017. D-PUF: Error Protection through Fine-Grained Compression. Proceedings of the International Symposium on High Performance Computing, Networking, Storage and Analysis on - SC 15 (2015). DOI:http://dx.doi.org/10.1109/sc15.2807597

[15] Mudit Bhargava and Ken Mai. 2014. An Efficient Reliable PUF-Based Cryptographic Key Generator. Proceedings of the 25th edition on Great Lakes Symposium on VLSI - GLSVLSI 15 (2015). DOI:http://dx.doi.org/10.1109/glsvlsi.2015.80

[16] Jeremie S. Kim, Minesh Patel, Hasan Hassan, and Mohammad Tehranipoor. 2014. Advanced Analysis of Cell Stability for Reliable SRAM PUFs. 2014 IEEE 23rd Asian Test Symposium (2014). DOI:http://dx.doi.org/10.1109/ats.2014.70

[17] Mohammad Tehranipoor, Nima Karimian, Wei Yan, and John A. Chandy. 2017. Investigation of DRAM PUFs Reliability under Device Accelerated Aging Effects. 2017 IEEE International Symposium on Circuits and Systems (ISCAS) (2017). DOI:http://dx.doi.org/10.1109/iscas.2017.8050629

[18] Fatemeh Tehranipoor, Nima Karimian, Wei Yan, and John A. Chandy. 2017. Investigation of DRAM PUFs Reliability under Device Accelerated Aging Effects. 2017 IEEE International Symposium on Circuits and Systems (ISCAS) (2017). DOI:http://dx.doi.org/10.1109/iscas.2017.8050629

[19] Mudit Bhargava and Ken Mai. 2014. An Efficient Reliable PUF-Based Cryptographic Key Generator. Proceedings of the 25th edition on Great Lakes Symposium on VLSI - GLSVLSI 15 (2015). DOI:http://dx.doi.org/10.1109/glsvlsi.2015.80

[20] Jeremie S. Kim, Minesh Patel, Hasan Hassan, and Mohammad Tehranipoor. 2014. Advanced Analysis of Cell Stability for Reliable SRAM PUFs. 2014 IEEE 23rd Asian Test Symposium (2014). DOI:http://dx.doi.org/10.1109/ats.2014.70
(DSN) (2016). DOI:http://dx.doi.org/10.1109/dsn.2016.30

[26] Wenyije Xiong, André Schaller, Nikolaos A. Anagnostopoulos, Muhammad Umair Saleem, Sebastian Gabmeyer, Stefan Katzenbeisser, Jakub Szefer. 2016. Run-Time Accessible DRAM PUFs in Commodity Devices. Lecture Notes in Computer Science Cryptographic Hardware and Embedded Systems – CHES 2016 (2016), 432–453. DOI:http://dx.doi.org/10.1007/978-3-662-53140-2_21

[27] Christoph Keller, Frank Gurkanayak, Hubert Kaeslin, and Norbert Felber. 2014. Dynamic Memory-Based Physically Unclonable Function for the Generation of Unique Identifiers and True Random Numbers. 2014 IEEE International Symposium on Circuits and Systems (ISCAS) (2014). DOI:http://dx.doi.org/10.1109/iscas.2014.6865740

[28] Fatemeh Tehraniipoor, Nima Karimian, Wei Yan, and John A. Chandy. 2017. DRAM-Based Intrinsic Physically Unclonable Functions for System-Level Security and Authentication. IEEE Transactions on Very Large Scale Integration (VLSI) Systems 25, 3 (2017), 1085–ÅŠ1097. DOI:http://dx.doi.org/10.1109/tvlsi.2016.2606658

[29] Maryam S. Hashemian, Bhanu Singh, Francis Wolff, Daniel Weyer, Steve Clay, and Christos Papachristou. 2015. A Robust Authentication Methodology using Physically Unclonable Functions in DRAM Arrays. Design, Automation & Test in Europe Conference & Exhibition (DATE), 2015 (2015). DOI:http://dx.doi.org/10.7873/date.2015.0308

[30] Yao Chen, Andrew B. Kahng, Bao Liu, and Wenjun Wang. 2015. Crosstalk-Aware Signal Probability-Based Dynamic Statistical Timing Analysis. Sixteenth International Symposium on Quality Electronic Design (2015). DOI:http://dx.doi.org/10.1109/issqd.2015.7085463

[31] Smruti R. Sarangi, Brian Greskamp, Radu Teodorescu, Jun Nakano, Abhishek Tiwari, and Josep Torrellas. 2008. VARIUS: A Model of Process Variation and Resulting Timing Errors for Microarchitects. IEEE Transactions on Semiconductor Manufacturing 21, 1 (2008), 3–13. DOI:http://dx.doi.org/10.1109/tsm.2007.913186

[32] Wangyang Zhang, Wenyije Yu, Zeyi Wang, Zhiping Yu, Rong Jiang, and Jinjun Xiong. 2008. An Efficient Method for Chip-Level Statistical Capacitance Extraction Considering Process Variations with Spatial Correlation. 2008 Design, Automation and Test in Europe (2008). DOI:http://dx.doi.org/10.1109/date.2008.4484739

[33] M.Tauhidur Rahman, Alison Hosey, Zimu Guo, Jackson Carroll, Domenic Forte, and Mark Tehraniipoor. 2017. Systematic Correlation and Cell Neighborhood Analysis of SRAM PUF for Robust and Unique Key Generation. Journal of Hardware and Systems Security 1, 2 (2017), 137–155. DOI:http://dx.doi.org/10.1145/31635-017-0012-3

[34] Yan Li, Helmut Schneider, Florian Schnabel, Roland Thewes, and Doris Schmitt-Landsiedel. 2011. DRAM Yield Analysis and Optimization by a Statistical Design Approach. IEEE Transactions on Computers and Systems I: Regular Papers 58, 12 (2011), 2906–2918. DOI:http://dx.doi.org/10.1109/tcisi.2011.2157741

[35] Qianying Tang, Chen Zhou, Woong Choi, Gyuseong Kang, Jongsun Park, Keshab K. Parhi, and Chris. H. Kim. 2017. A DRAM based Physical Unclonable Function Capable of Generating > 1032 Challenge Response Pairs per 1KBit Array for Secure Chip Authentication. 2017 IEEE Custom Integrated Circuits Conference (CICC) (2017). DOI:http://dx.doi.org/10.1109/cicc.2017.7993610

[36] Md. Tauhidur Rahman, Kan Xiao, Domenic Forte, Xuhe Zhang, Jerry Shi, and Mohammad Tehraniipoor. 2014. TI-TRNG: Technology Independent True Random Number Generator. Proceedings of the The 51st Annual Design Automation Conference on Design Automation Conference - DAC 14 (2014). DOI:http://dx.doi.org/10.1145/2593069.2593236

[37] Hasan Hassan, Nandita Vijaykumar, Samira Khan, Saugata Ghose, Kevin Chang, Gennady Pekhimenko, Donghyuk Lee, Oguz Ergin, Onur Mutlu. 2017. SoftMC: A Flexible and Practical Open-Source Infrastructure for Enabling Experimental DRAM Studies. 2017 IEEE International Symposium on High Performance Computer Architecture (HPCA) (2017). DOI:http://dx.doi.org/10.1109/hpca.2017.62

[38] Matthew Jacobsen, Dustin Richmond, Matthew Hogains, and Ryan Kastner. 2015. RIFFA 2.1: A Reusable Integration Framework for FPGA Accelerators. ACM Trans. Reconfigurable Technol. Syst. 8, 4, Article 22 (September 2015), 23 pages. DOI:http://dx.doi.org/10.1145/2815631

[39] http://www.ti.com/tool/usb-to-gpio

[40] André Schaller, Wenyije Xiong, Nikolaos Anagnostopoulos, Muhammad Umair Saleem, Sebastian Gabmeyer, Stefan Katzenbeisser, and Jakub Szefer. 2017. Intrinsic Rowhammer PUFs: Leveraging the Rowhammer Effect for Improved Security. 2017 IEEE International Symposium on Hardware Oriented Security and Trust (HOST) (2017). DOI:http://dx.doi.org/10.1109/hst.2017.7951729

[41] Jamie Liu, Ben Jaiyen, Yoongu Kim, Chris Wilkerson, and Onur Mutlu. 2013. An Experimental Study of Data Retention Behavior in Modern DRAM Devices: Implications for Retention Time Profiling Mechanisms. In Proceedings of the 40th Annual International Symposium on Computer Architecture (ISCA ’13). ACM, New York, NY, USA, 60-71. DOI: http://dx.doi.org/10.1145/2485922.2485928

[42] Yasunao Katayama, Eric J. Stuckey, Sumio Morioka, and Zhao Wu. Fault-Tolerant Refresh Power Reduction of DRAMs for Quasi-Nonvolatile Data Retention. Proceedings 1999 IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (EFT99). DOI:10.1109/2tvs.1999.802898

[43] Karthik Chandrasekar, Sven Goossens, Christian Weis, Martijn Koedam, Benny Akesson, Norbert Wehn, Kees Goossens. 2014. Exploiting Expendable Process-Margins in DRAMs for Run-Time Performance Optimization. Design, Automation
Appendix

A. IMPACT OF REDUCED ACTIVATION TIME

In figure 11, red spots represent the flipped bits at the reduced activation time ($t_{RCD,0.38}$) for a DRAM bank. The results show that the flipped bits are only observed at the first accessed cache line (i.e., just in the first column). A similar observation was concluded in [18] and [20].

![Graph showing flipped bits at $t_{RCD,0.38}$](image)

Fig. 11. Flipped bits at $t_{RCD,0.38}$ with input pattern- (i) 0x00, (ii) 0x55, (iii) 0xAA, (iv) 0xFF.