Hyper-optimized tensor network contraction

Johnnie Gray\textsuperscript{1} and Stefanos Kourtis\textsuperscript{1,2,3}

\textsuperscript{1}Blackett Laboratory, Imperial College London, London SW7 2AZ, United Kingdom
\textsuperscript{2}Department of Physics, Boston University, Boston, MA, 02215, USA
\textsuperscript{3}Institut quantique & Département de physique, Université de Sherbrooke, Québec J1K 2R1, Canada

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Tensor networks represent the state-of-the-art in computational methods across many disciplines, including the classical simulation of quantum many-body systems and quantum circuits. Several applications of current interest give rise to tensor networks with irregular geometries. Finding the best possible contraction path for such networks is a central problem, with an exponential effect on computation time and memory footprint. In this work, we implement new randomized protocols that find very high quality contraction paths for arbitrary and large tensor networks. We test our methods on a variety of benchmarks, including the random quantum circuit instances recently implemented on Google quantum chips. We find that the paths obtained can be very close to optimal, and often many orders or magnitude better than the most established approaches. As different underlying geometries suit different methods, we also introduce a hyper-optimization approach, where both the method applied and its algorithmic parameters are tuned during the path finding. The increase in quality of contraction schemes found has significant practical implications for the simulation of quantum many-body systems and particularly for the benchmarking of new quantum chips.

I. INTRODUCTION

Since the advent of the density-matrix renormalization group algorithm, invented to study one-dimensional lattice systems of quantum degrees of freedom, tensor networks have permeated a plethora of scientific disciplines, finding use in fields such as quantum condensed matter [1–4], classical statistical mechanics [5–7], information science and big-data processing [8, 9], systems engineering [10], quantum computation [11], machine learning and artificial reasoning [12–14] and more. The underlying idea of tensor network methods is to use sparse networks of interconnected low-rank tensors to represent data structures that would otherwise be expressed in (very) high-rank tensor form, which is hard to manipulate. Due to this ubiquity, techniques to perform (multi)linear algebraic operations on tensor networks accurately and efficiently are very useful to a highly interdisciplinary community of researchers and engineers. Of these operations, tensor network contraction, i.e., the evaluation of a scalar quantity that has been expressed as a tensor network, is the most common.

When a system under consideration gives rise to a tensor networks with a regular structure, such as lattices, the renormalization group apparatus is often employed to perform tensor network contractions with controllable accuracy. This approach has been successful in tackling a variety of classical and quantum many-body problems [5–7, 15–20]. Efficient tensor network contraction is also possible in special cases in which network topology (e.g., trees), values of tensor entries, or both are restricted [21–26]. Despite these results, contracting tensor networks with arbitrary structure remains (at least) \#P-hard in the general case [27, 28]. This is true, in particular, for tensor networks that model arbitrary quantum circuits, a fact that has recently inspired proposals for quantum algorithms running on these circuits that aim towards a practically demonstrable quantum computational advantage over classical computers [11, 29–39]. The precise threshold for observing such a quantum advantage is nonuniversal and ultimately depends on the efficiency of the classical simula-

![Sample tensor networks: (a) simplified network for a rectangular 7x7 qubit 1 + 40 + 1 depth random quantum circuit with 742 rank-3 tensors; (b) a random 5-regular network with 100 tensors, arising in, e.g., SAT problems; and (c) random planar network with 184 tensors, arising in, e.g., the statistical-mechanical evaluation of knot invariants.](image)
traction algorithms based on graph partitioning and community structure detection [43], previously theorized [11] and recently implemented [44] algorithms based on the tree decomposition of graphs, as well as new heuristics that we introduce in this work. Furthermore, observing that different graph structures favor different algorithms, we implement a hyper-optimization approach, where both the method applied and its parameters are varied throughout the contraction path search, leading to automatically customized contraction algorithms that often achieve near-optimal performance. Our findings can lead to significant performance gains across the spectrum of tensor network applications.

The remainder of this paper is organized as follows. In Sec. II we formalize the problem of finding the optimal contraction path for arbitrary tensor networks. In Sec. III we introduce and explain the various algorithms employed in our heuristics. In Sec. IV we test our methods on a variety of benchmarks, including the random quantum circuit instances recently implemented on Google Bristelecone and Sycamore quantum chips. We conclude in Sec. V.

II. PROBLEM STATEMENT

We denote an edge-weighted graph by \( G = (V, E) \), where \( V \) is the vertex set and the set of 2-tuples of vertex indices \( E \subset \{(u, v) : u, v \in V\} \) is the edge set, along with a weight function \( w : E \to \mathbb{R}^+ \) that assigns a positive real number to each edge. For each vertex \( v \), define the incidence set \( s_v = \{ e : e \in E \text{ and } v \in e \} \), which is the set of edges incident to vertex \( v \), such that \( |s_v| = d_v \), the degree of vertex \( v \).

To define a tensor network, we augment \( G \) with (i) a discrete variable \( x_e \) for each edge \( e \in E \), whose set of possible values (or Hilbert space) is given by \( D(e) \) with \( |D(e)| = w(e) \), (ii) an ordered tuple \( t_v : \mathbb{N}_{d_v} \to s_v \) for each vertex \( v \in V \), and (iii) a multivariate function or tensor \( T_v : D(t_v(1)) \times \cdots \times D(t_v(d_v)) \to \mathbb{C} \), where \( t_v(i) \) denotes the \( i \)-th element of tuple \( t_v \), for every vertex \( v \in V \). That \( w \) is defined to be a real-valued function even though \( D(e) \in \mathbb{Z}^+ \forall e \in E \) is simply a choice that allows for extra flexibility in the design of contraction algorithms, see, e.g., the Boltzmann greedy algorithm below.

With these definitions, a tensor network contraction can be represented as a sequence of vertex contractions in graph \( G \). Each vertex contraction removes common edges between pairs of tensors, if any, and represents a product operation on the corresponding tensors, in which one takes the inner product over common indices or an outer product if there are no common indices. For simplicity, in what follows we consider only pairwise contractions, which are common practice. Multiway contractions are also possible, but they can always be decomposed to sequences of pairwise contractions. For some applications, only a subset of \( V \) must be contracted, while in others all vertices in \( V \) are contracted into a single vertex. Here we will focus on the latter case, as it underlies the former. We will assume that \( G \) has no loops initially and that multiple edges are always contracted simultaneously, so that no loops occur throughout the contraction.

To represent the sequence of vertex contractions, we define a rooted binary tree \( B = (V_B, E_B) \), with the first \( |V| \) vertices indices denoting leaves, using two touples \( l \) and \( r \) such that \( l(v) \) and \( r(v) \) are the indices of the ‘left’ and ‘right’ children of vertex \( v \in V_B \), respectively, if any. This defines a tree embedding of \( G \) [45]. Finally, we assign an incidence set \( s_v \) to each \( v \in V_B \), starting with leaves, according to

\[
s_v = \begin{cases} \{ e : e \in E \text{ and } v \in e \} & \text{if } v \text{ is a leaf index}, \\ s_{l(v)} \oplus s_{r(v)} & \text{otherwise}, \end{cases}
\]

with \( s_i \oplus s_j = (s_i \cup s_j) \setminus (s_i \cap s_j) \). The composite of \((B, S)\), where \( S = \{ s_v : v \in V_B \} \), defines a contraction tree of \( G \).

For a given tensor network contraction tree, one can quantify the space and time cost of contracting the network. First, the total space required for the contraction of a network is given, up to an \( O(|V|) \) prefactor, by \( 2^W \), for contraction width

\[
W = ec_{max}(B, S),
\]

where \( ec_{max} \) is the maximum edge congestion for this tree embedding of \( G \) [46]. In our notation,

\[
ec_{max}(B, S) = \max_{v \in V_B} \sum_{e \in s_v} \log_2 w(e).
\]
A space-optimal contraction tree for $G$ is then defined by

$$B_{\text{space}}(G) = \arg\min_{B \in B_{|V|}} \mathcal{C}(B, S),$$

where $B_{|V|}$ is the set of all rooted binary trees with $|V|$ leaves. For systems of boolean variables or qubits, $w = 2$ and $\mathcal{C}(B, S) = \max_{v \in V_G} |S_v|$. The contraction width is then equal to the maximum vertex degree in the minors of $G$ obtained throughout the contraction path represented by $B$ [43], as illustrated in the example of Fig. 2. The same logic extends to any constant $w$.

Similarly, the time complexity of the contraction is captured by the contraction cost

$$C(B, S) = \sum_{v \in V_B} 2^{\mathcal{V}(B, S, v)},$$

where $\mathcal{V}$ is the vertex congestion [46]

$$\mathcal{V}(B, S, v) = \sum_{e \in \mathcal{E}(v)} 2^{|S_{e}|}. \quad (6)$$

Again using the case of qubits as an example, the number of operations required to obtain the tensor corresponding to a non-leaf vertex $v$ by contracting its children is proportional to $2^{|S_{e}|}$. More precisely, assuming every contraction is an inner product, for real (complex) tensors, the associated FLOP count will be a factor of two (eight) times more than $C$: one (six) FLOP(s) for the multiplication and one (two) FLOP(s) for the addition. A time-optimal contraction tree for $G$ is then

$$B_{\text{time}}(G) = \arg\min_{B \in B_{|V|}} C(B, S).$$

$B_{\text{time}}(G)$ and $B_{\text{space}}(G)$ are not necessarily the same and hence a strategy that aims to find one is not guaranteed to also find or approximate the other.

III. TENSOR NETWORK CONTRACTION ALGORITHMS

We have shown that the optimization of the contraction path for a given tensor network corresponds to minimization of a vertex or edge congestion measure over the possible tree embeddings of the network. Instead of performing this minimization, here we will use methods that optimize contraction paths based on quantities that are proxies to these congestion measures, as explained below. Our heuristics are based on established algorithms for a variety of common graph theoretic tasks, such as balanced bipartitioning or community detection, some of which, unlike tree embedding, have seen decades of development and improvement. This affords great benefits in performance to our methods.

A. Optimal Contraction Trees

One method for finding contraction trees is to exhaustively search through all of them and return whichever minimizes the desired target $W$ or $C$. Since outer products are rarely ever beneficial, an efficient but virtually optimal way to perform this search is to adopt a dynamic programming approach that builds the tree considering connected subgraphs only [47]. We refer to this optimizer as Optimal and for our results we use the version implemented in opt.einsum [48].

B. Line-Graph Tree Decompositions - QuickBB & FlowCutter

The most common approach to contracting arbitrary tensor networks in recent years, motivated by the results of Markov and Shi [11], has been to find a tree decomposition of the line graph of $G$. From this tree decomposition, an edge elimination ordering can be constructed such that the complexity of the corresponding contraction is upper bounded by the tree-width of the line-graph minus one. Practically speaking, we turn an edge ordering, $(e_1, e_2, e_3, \ldots)$ into a contraction tree as follows. First, find the subgraph of $G$ induced by the next edge in the ordering, $e$. Update $G$ by contracting all of the tensors in this subgraph to form a single vertex (if there are more than 2 tensors use an exhaustive or greedy approach to find a contraction sequence for this small subgraph only). Repeat until all edges in the ordering have been processed.

In the tensor network literature the most commonly used tree decomposition finder is QuickBB [49], which implements a depth-first ‘branch and bound’ search. Broadly speaking this approach emphasizes performance for graphs with modest numbers of edges, where indeed QuickBB has been shown to work well [42]. More recently, the FlowCutter tree decomposition finder [50, 51], has been applied to tensor networks [44]. FlowCutter takes more of a ‘top-down’ approach which emphasizes performance on graphs with large numbers of edges. Both function as ‘any-time’ algorithms, able to yield the best found solution after setting an arbitrary time. On the other hand, neither of these optimizers take edge weights into account, which may be a significant disadvantage in the many-body setting, where, unlike in quantum circuits, bond dimensions can vary significantly.

C. Community detection via edge betweenness - GN

One of the methods for the contraction of tensor networks with arbitrary structure introduced in Ref. [43] is based on detecting communities in the network. Qualitatively, a community is a subset of the vertices in a network that is densely connected internally and sparsely connected with its complement. Detecting communities in networks is a central problem in the study of complex networks [52, 53].

The intuition behind using the community structure to contract an arbitrary tensor network is that it is advantageous to contract all the edges between vertices that belong to a community first. That is because the vertex that results from the contraction of all edges within a community, which we call a community vertex, is sparsely connected with the rest of the network. Thus, when a community structure exists and is de-
ected in the network, the adherence of contractions to this community structure is expected to lead to community vertices with a maximum degree that is lower than that of the same number of vertices reached by an arbitrary sequence of contractions of the original network. This approach hence effectively minimizes the contraction cost, i.e., yields a contraction sequence that approximates the one defined by the space-optimal contraction tree.

A popular community structure detection algorithm is the one of Girvan and Newman [54]. It operates by evaluating a quantity called edge betweenness centrality, defined as

$$g(e) = \sum_{s,t\in V} \sigma_{st}(e) / \sigma_{st},$$  \hspace{1cm} (8)

where $\sigma_{st}$ is the total number of shortest paths between vertices $s$ and $t$, and $\sigma_{st}(e)$ is the number of those paths that pass through edge $e \in E$. The algorithm starts with an empty edge list and repeats two steps:

1. remove $e' = \text{argmax}_e g(e)$ from $E$ and add it to the list, $e \in E$.
2. calculate $g(e) \forall e \in E$.

until exhausting $E$. Multiple edges can be processed simultaneously, since they have the same $g$. The resulting list of edges, sometimes called a dendrogram, defines the detected community structure: if one sequentially removes the list entries from $E$ until $G$ becomes disconnected, then the resulting connected components are the communities of $G$. The algorithm then proceeds by splitting each connected component into smaller communities, and the process repeats all the way down to the individual vertex level.

The output of the Girvan-Newman method is also a contraction path: one simply has to traverse the edge list in reverse, each entry defining a contraction of the endpoints of the corresponding edge. One can incorporate edge weights (and thus bond dimensions) into Eq. (8), possibly randomized with some strength $\tau$, to generate varied paths. We call the optimizer based on repeated sampling of these paths GN.

D. Agglomerative contraction trees - BGreedy

One simple way to construct a contraction tree is greedily from the bottom up. Here, one ignores any overall structure of the graph $G$ and instead heuristically scores each possible pairwise contraction. Based on these scores, a pair of tensors can be chosen and contracted into a new vertex and the list of scores then updated with any new possible contractions. Whilst we know the exact cost and output size of each pairwise contraction, we do not know the effect it might have on the cost and size of later contractions, meaning we must instead carefully choose the heuristic score function.

Given two tensors $T_i$ and $T_j$ whose contraction yields $T_k$, one reasonable choice for the heuristic cost function is

$$\text{cost}(T_i, T_j) = \text{size}(T_k) - \alpha(\text{size}(T_i) + \text{size}(T_j))$$  \hspace{1cm} (9)

with $\alpha$ a tunable constant. If we take $\alpha = 1$ then this cost is directly proportional to the change in memory should we perform the contraction. Whereas instead taking $\alpha = 0$ essentially just prioritizes the rank of the new tensor. Since we will want to sample many greedy paths we also introduce a ‘Boltzmann factor’ weighting of the costs such that the probability of selecting a pairwise contraction is

$$p(T_i, T_j) \propto \exp \left( -\frac{\text{cost}(T_i, T_j)}{\tau} \right),$$  \hspace{1cm} (10)

with $\tau$ an effective temperature governing how ‘adventurous’ the path finding should be. Repeatedly generating contraction trees using this combination of cost and weighting, whilst potentially tuning both $\alpha$ and $\tau$, leads to the $\text{BGreedy}$ optimizer. $\text{BGreedy}$ generally outperforms other greedy approaches and is quick to run, making it a simple but useful reference algorithm.

E. Divisive contraction trees - KaHyPar

The greedy or agglomerative approach is a natural way to think about building contraction trees from the bottom up. However, as introduced in [43] we can also try and build contraction trees from the top down in a divisive manner. The key here is that each node in a contraction tree represents not only an effective tensor but a subgraph of the initial graph describing the full tensor network. As we ascend a contraction tree, merging two nodes corresponds to a pairwise contraction of the two effective tensors. In reverse, as we descend a contraction tree, splitting a node corresponds to a bipartitioning of subgraph associated with that node.

Practically we start with the list of ‘childless’ vertices initially just the root of the tree corresponding to the full graph, $\{V_G\}$. We take the next childless vertex, $V$, and partition it into $V = V_1 \cup V_2$. If $|V_1| > 1$ we append it to the list of childless vertices and similarly if $|V_2| > 1$. This process can be repeated until the full contraction tree is generated. Such a divisive approach is very similar to the community detection scheme introduced earlier, however, whilst the Girvan-Newman algorithm naturally yields the entire contraction tree, here we create single contractions one at a time. This allows one to combine partitioning with other optimizers. For example, we can instead partition a vertex $V$ into $k$ partitions, $V_1, V_2, \ldots, V_k$ and then use the $\text{Optimal}$ or $\text{BGreedy}$ optimizer to ‘fill in’ the contraction tree — essentially find the contraction path for a tensor network composed just of the tensors corresponding to each of these new subgraphs. Similarly, if the size of $V$ drops below some threshold, we can again use either $\text{Optimal}$ or $\text{BGreedy}$ to find the remaining part of the contraction tree corresponding just to the leaf tensors in $V$.

The cost of an individual contraction - a vertex bi-partitioning - is given by the product of the dimensions of the involved indices. These include any outer indices of the subgraph, plus any indices that cross the newly created partition. Since the outer indices are independent of the partition, minimizing the number of indices cut by a partition also minimizes
the cost of the corresponding contraction. This is still essentially a greedy approach - it only considers the cost of a single contraction and strictly minimizing this cost (corresponding to choosing a min-cut) could likely create more expensive contractions down the line. However, one way to heuristically adjust this is to control how balanced to make the partitions, in other words, how much to match the size of each partition. Specifically, we can define the imbalance parameter, $\epsilon$, such that $|V_i| \leq (1+\epsilon)|V|/k$ for $i = 1 \ldots k$, where $k$ is the number of partitions. If $\epsilon$ is close to zero, then the partitions are forced to be very similar in size, whilst if $\epsilon$ is close to $k$ the partitions are allowed to be of any size.

Taking into account the internal structure of the tensors in a problem allows for further flexibility in the recursive bipartitioning process, which in turn can lead to significant performance gains. As an example, consider the case of a COY tensor, whose entries are 1 only when all indices are equal and 0 otherwise. These tensors appear, for example, when modeling circuits of controlled gates (see, e.g., Sec. IV C 1) or satisfiability formulas [26, 43]. Each COPY tensor in a network can be replaced by any connected graph of COPY tensors without changing the result of the contraction [4]. By replacing all COPY tensors in the network with hyperedges, one can perform recursive hypergraph bipartitioning with more freedom in the search for short cuts compared to the original graph. To revert back to a ‘traditional’ tensor network after partitioning, each hyperedge can be replaced by a low-rank COPY tensor subgraph that cuts each separator at most once, as illustrated in Fig. 3. Another important use-case for hyperedges is to efficiently treat batch and output indices, though these are not benchmarked in this work.

We employ the partitioner KaHyPar [55, 56] to generate our contraction trees for a number of reasons. Aside from offering state-of-the-art performance, it also can handle hypergraphs (and thus arbitrary tensor expressions), allows key parameters such as the imbalance to be specified, and takes into account edge weights (and thus arbitrary bond dimensions). Repeatedly sampling contraction trees whilst tuning the parameters $k$, $\epsilon$ and the cut-off to stop partitioning leads us to the optimizer we call KaHyPar. Note that the line graph and greedy methods of Secs. III B and III D, respectively, also support hypergraphs natively.

FIG. 3. (a) Segment of tensor network with six tensors, one of which (black filled circle) is a COY tensor. (b) COY tensor replaced by a hyperedge. Recursive hypergraph bipartitioning yields the separator hierarchy drawn as dashed lines, with thicker lines for higher level in the hierarchy. (c) After a separator hierarchy is found, the hyperedge is replaced by a connected subgraph of COY tensors whose edges intersect each separator at most once. The results of the contraction of networks (a) and (c) are identical.

F. Stochastic Bayesian Optimization

The optimal contraction tree optimizer runs until completion whilst QuickBB and FlowCutter are natively anytime algorithms. For the remaining three optimizers – GN, BGreedy and KaHyPar – we use a combination of randomization and Bayesian optimization [57] to intelligently sample ever better contraction paths. This allows all three of them to run as parallel anytime algorithms.

For the GN and KaHyPar optimizers, randomization can be introduced as a noise of the edge weights of the initial graph $G$. For the BGreedy optimizer the Boltzmann sampling of greedy contractions yields another source of randomization. Due to the high sensitivity of the contraction width $W$ and cost $C$ to the contraction path, simply sampling many paths and keeping the best already offers significant improvements over single shot versions of these same algorithms. However we can further improve the performance if we allow the heuristic parameters of each optimizer to be tuned as the sampling continues. We use the baytune [58] library to perform this optimization, which uses Gaussian processes [59] to model the effect of the parameters on the target score – either $W$ or $C$ – and suggest new combinations which are likely to perform well.

IV. RESULTS

We benchmark our contractors on three classes of tensor networks with complex geometry – random regular graphs, random planar graphs, and random quantum circuits. In each set of results we set a time limit for each of the optimizers to run for, and then target either the contraction width, $W$, or contraction cost $C$. As a reminder, $W$ is essentially the space requirement of the contraction (log$_2$ of the size of the largest intermediate tensor) whilst $C$ is the time requirement (the total number of scalar operations). The optimal algorithm is able to search for either the minimum $W$ or $C$, whilst GN, BGreedy and KaHyPar can target either through the guided Bayesian optimization. Finally, there is no way to specifically bias QuickBB and FlowCutter towards either $W$ or $C$ so in each case the optimizer runs identically. If an optimizer can run in parallel, we allow it 4 cores to do so. An open source implementation of the optimizers, compatible with opt_einsum [48] and quimb [60], is available at [61].

To give some context to the relative scale of $W$ and $C$, a complex, single precision tensor of size $2^{27}$ requires 1GB of memory, and a consumer grade GPU can usually achieve a few teraFLOPs in terms of performance, corresponding to $C \sim 10^{15}$ over an hour. In the final results section we benchmark various contractions and indeed find this real-world performance. At the extreme end of the scale, the most powerful supercomputer in the world currently, Summit, has a few petabytes of memory, corresponding very roughly to $W \sim 47$, though this is obviously distributed among nodes and utilizing it for a single contraction would need, among many other technical considerations, significant inter-node communication. Summit has also achieved sustained performance of a
few hundred petaFLOPs [62], which over an hour might correspond to $C \sim 10^{20}$, but is unlikely to do so if distributed contraction is required (i.e. for high $W$).

A. Random Regular Graphs

We start by benchmarking tensor networks with geometries defined by random regular graphs, as studied in [43, 44]. For such a $k$-regular graph, every vertex is connected randomly to $k$ others, with total number of vertices $|V|$. We treat each of the edges as tensor indices of size 2 and associate a rank-$k$ tensor with each vertex. An example of such a network is shown in Fig. 1(b). For each size $|V|$, degree $k$ and target $\in \{W, C\}$, we generate 100 sample regular graphs uniformly [63], and allow 5 minutes of search time per instance for each optimizer. The reference Optimal path finder we instead run for 24 hours and only show data points where all but one or two of the instances successfully terminated so as not to bias those points towards easy instances.

The results are shown in Figs. 4(a)-(f). First of all we note that for small sizes all optimizers return similar performance, indeed, close to Optimal. As $|V|$ increases however the same ranking emerges in each combination of $k$ and $\{W, C\}$: (from worst to best) QuickBB, BGreedy, FlowCutter, GN, then finally KaHyPar. We attribute the improvement of GN over previous studies [44] to the use of guided stochastic sampling. There are some interesting performance comparisons when it comes to targeting contraction width $W$ or cost $C$. For example, while BGreedy beats QuickBB for width across the board, the results are much closer for contraction cost. On the other hand, the advantage of KaHyPar over GN and FlowCutter is much more pronounced when considering cost rather than width.

B. Random Planar Graphs

A contrasting class of geometries to consider is that of planar graphs, encountered for example in the study of physical systems defined on a 2D lattice or in evaluating knot invariants [64]. To investigate these in a generic fashion, we generate random planar graphs with $|V| \in [20, 200]$ according to the scheme in [65], an instance of which is shown in Fig. 1(c). Whilst these are much more random than square lattices for example, we find nonetheless that the results are broadly representative. Similarly to the random regular graphs, for each vertex with $k$ edges we associate a rank-$k$ tensor with bond dimensions of size 2 and allow each optimizer 5 minutes per instance to explore contraction paths. In [44] it was shown that the optimal contraction path with respect to $W$ for planar graphs can be found in polynomial time. In Fig. 5(a) and
C. Random Quantum Circuits

The final class of tensor networks we study is those corresponding to random quantum circuits executed on a range of quantum chip geometries. In particular, we look at sizes and depths previously explored in the context of so-called ‘quantum supremacy’ [37, 38, 66, 67]. Quantum circuits can be naturally cast as tensor networks and then simulated via contraction, as shown in [11]. In recent years, random quantum circuits have been used both as a test-bed for tensor network contraction schemes as well as setting the benchmark for demonstrating ‘quantum supremacy’ [41, 68–72]. Practically speaking, such simulations can also allow the fidelity of real quantum chips to be benchmarked and calibrated [38, 67, 71].

The simplest quantity to compute here is the ‘transition amplitude’ of one computational basis state to another through a unitary describing the quantum circuit. Assuming we start with the $N$ qubit all-zero bit-string $|0^N\rangle$, the transition amplitude for output bit-string $x$ can be written:

$$c_x = \langle x| U_d U_{d-1} \ldots U_2 U_1 |0^N\rangle,$$

where we have assumed some notion of circuit depth, $d$, such that each unitary $U_i$ contains a ‘layer’ of entangling gates, the exact composition of which depends on the specific circuit definition. The process for computing $c_x$ takes place in several steps: (a) construct the tensor network corresponding to the circuit; (b) perform some purely structure dependent simplifications of the tensor network; (c) find the contraction path for this simplified network; and (d) actually perform the contraction using the found path. Steps (a) and (b) are very cheap, and moreover we can re-use the path found in step (c) to contract any tensor with matching structure but different tensor entries, such as varying $x$.

1. Gate Decompositions

We find that pre-processing the tensor networks before attempting to find contraction paths is an important step, particularly for optimizers such as QuickBB and BGreedy that scale badly with the number of edges and vertices. A tensor network for $c_x$ initially consists of: rank-1 tensors describing each of the input and output qubit states; rank-2 tensors describing single qubit gates; and rank-4 tensors describing two-qubit gates. The first processing step is deciding how to treat the two-qubit gates. A tensor describing such a gate can be written $g_{i_b o_b}^{a_o a_i}$, such that $i_a (i_b)$ is the input index and $o_a (o_b)$ the output index of qubit $a (b)$. Whilst $g_{i_a o_b}^{a_o a_i}$ is unitary with respect to $i_a i_b \rightarrow o_a o_b$, a low rank decomposition can potentially be found by grouping the indices $\{i_a, o_b\}$ or $\{i_b, o_a\}$ and performing an SVD on the resulting matrix. In the first case this yields two rank-3 tensors:

$$g_{i_a o_b}^{a_o a_i} = \sum_{\xi=1}^\chi f_{i_a}^{\xi} f_{o_b}^{\chi} f_{a_i}^{\xi},$$  

where we have dropped any zero singular vectors and absorbed the remaining singular values into either of the left and right tensors $l$ and $r$, each of which is now ‘local’ to either qubit $a$ or $b$, connected by a bond of size $\chi$. The second case yields the same but with an effective SWAP (which can be implemented purely as a relabelling of tensor indices) of the qubit states first:

$$g_{i_a i_b}^{a_o o_b} = \sum_{\xi=1}^\chi \sum_{l=r}^{2} f_{i_a}^{\xi} f_{i_b}^{\xi} f_{o_b}^{\chi} f_{o_a}^{\xi}.$$

The options for a gate are thus to: (a) perform no decomposition; (b) perform a spatial decomposition – Eq. (12); or (c) perform a swapped decomposition – Eq. (13). By default we only perform a decomposition if the bond dimension, $\chi$,
yielded is less than 4; all controlled gates fall into this category for a spatial decomposition, whereas the ISWAP gate for instance has $\chi = 2$ for the swapped decomposition. Another option is to discard small but non-zero singular values which will result in a drop in the fidelity of $c_p$ – unless explicitly noted we do not perform this form ‘compression’.

2. Tensor Network Simplifications

Next we describe a series of simplifications based simply on tensor network structure and sparsity of the tensors that we perform iteratively until no more operations are possible. The first of these is diagonal-reduction of tensor axes, as introduced for quantum circuits in [69]. For a $k$-dimensional tensor, $t_{i_1i_2...i_k}$, with indices $i_1i_2...i_k$, if for any pair $\{i_x, i_y\}$

$$t_{i_xi_y} = 0 \quad \forall \quad i_x \neq i_y$$

(14)

then we can replace $t$ with a $(k-1)$-dimensional tensor, $\hat{t}$ with elements $\hat{t}_{i_1...i_{k-1}} = t_{i_1:i_{k-1}i_k} \delta_{i_k}^{i_y}$, where the $\delta$ copy can be implemented by re-indexing $i_y \to i_x$ everywhere else in the tensor network, thus resulting in $i_x$ becoming a hyperedge. This enables the use of the hypergraph machinery detailed in Sec. III E.

The second pre-processing step we perform is rank-simplification. Here we generate a greedy contraction path that targets rank reduction only (i.e. with respect to Eq. (9) and (10) sets $\alpha = \tau = 0$). We then perform any of the pairwise contractions such that the rank of the output tensor is not larger than the rank of either input tensor. If the tensor network has no hyperedges, this corresponds to absorbing all rank-1 and rank-2 tensors into neighbouring tensors, a process which cannot increase the cut-weight across any partition for example.

The third pre-processing step we perform is antidiagonal-gauging. Here, again assuming we have a $k$-dimensional tensor $t_{i_1i_2...i_k}$, if for any pair of indices $\{i_x, i_y\}$ of matching size $d$ we find

$$t_{i_xi_y} = 0 \quad \forall \quad i_x \neq d - i_y$$

(15)

then we can flip the order of either index $i_x$ or $i_y$ throughout the tensor network. This corresponds to gauging that index with a ‘reflected’ identity, for example if $d = 2$ the Pauli matrix $X$. This simplification does not help on its own but merely produces tensors which can then be diagonally reduced using the prior scheme.

The final simplification we perform is column-reduction. Here, if for any $k$-dimensional tensor $t_{i_1i_2...i_k}$, we find an index $i_x$ and ‘column’ $c$ such that

$$t_{i_xi_1...i_k} = 0 \quad \forall \quad i_x \neq c$$

(16)

then we can replace every tensor, $t_{i_1...i_x}$, featuring that index with the $(k-1)$-dimensional tensor $\tilde{t}$ corresponding to the slice $\tilde{t}_{i_1...i_{x-1}c}$, removing that index from the network entirely.

We apply the above set of simplifications iteratively but deterministically until no method can find any operation to perform. The order they are applied in can produce very different networks – we find cycling through the order $\{\text{diagonal-reduction, rank-simplification, antidiagonal-gauging, column-reduction}\}$ produces good results. Indeed for quantum circuits generally the resulting tensor networks often have almost no sparsity among tensor entries. Note for methods such as GN which cannot handle hyperedges we skip the diagonal-reduction. Finally, if aiming to reuse a contraction path, one needs to maintain the sparsity structure from network to network, possibly excluding any variable tensors from the simplification steps that detect sparsity. For most circuits terminated with a layer of Hadamard gates, if one only changes the sampled bit-string $x$ then even this is not usually necessary.

3. Random Quantum Circuit Geometries

We benchmark the contraction path optimizers against different random quantum circuits executing on three different quantum chip geometries: (i) a rectangular $7 \times 7$ lattice of 49 qubits; (ii) a 70 qubit ‘Bristlecone’ lattice; and (iii) a 53-qubit ‘Sycamore’ lattice.

For the first two we use the updated, harder versions of the random circuit definitions first suggested in [38], which are available at [73]. We adopt the notation $(1+d+1)$ for depth $d$ to emphasize that the technically first and last layer of single qubit gates (which add no real complexity) are not counted. In both cases the entangling gate used is the controlled-$Z$ which has a $\chi = 2$ spatial decomposition.

For the Sycamore architecture, we use the same circuits that were defined and also actually executed in the recent work [67]. Here each two-qubit gate is a separately tuned ‘fermionic simulation’ gate which has no low-rank decomposition if treated exactly. On the other hand, if a swapped decomposition is performed, the two smallest singular values are quite small and on average discarding them leads to a fidelity drop of a fraction of a percentage point – for a single gate. If this approximation is used for every single entangling gate in the circuit, however, the error is compounded. For our main results, labelled ‘Sycamore-53’, we thus perform no gate decomposition and consider perfect fidelity transition amplitude calculations only. Results where the $\chi = 2$ swapped decomposition has been used we label ‘Sycamore-53*’. We also note that the definition of circuit ‘cycles’, $m$, used in [67] is about twice as hard as the rectangular and bristlecone circuit definition of depth, $d$, since per layer almost all qubits are acted on with an entangling gate rather than approximately half respectively.

In the following table we report the number of network vertices and edges for representative depths of each circuit geometry after simplifications. The first two columns, $|V|, |E|$ are for the case where hyperedge introduction is avoided, the last two columns, $|\tilde{V}|, |\tilde{E}|$, are for the case where the full simplification scheme introduced above has been applied.
We note that if the swap decomposition is not applied to the sycamore circuits then no diagonal-reductions can take place and the resulting simplified tensor network is the same in both cases.

4. 2D Circuit Specific Optimizers - qFlex/PEPs

Before presenting results for contraction width and cost for these random circuits, we introduce one final form of contraction path optimizer that has been successfully applied to circuits acting on 2D lattices [71, 72]. Here one performs the spatial decomposition of the entangling gates, regardless of rank, such that every tensor is uniquely localized above a single qubit register. One can then contract every tensor in each of these spatial slices resulting in a planar tensor network representing \( c_x \) with a single tensor per site. Although the two works, [71] and [72], have significant differences in terms of details (and goals beyond the computation of a single perfect fidelity amplitude), the core object treated by each is ultimately this planar tensor network, which is small enough that we can report optimal contraction widths and costs for. We call this optimizer – which flattens the circuit tensor network into the plane before finding the optimal \( W \) or \( C \) from that point onwards – qFlex/PEPs. With regards to a swapped decomposition, in order to maintain the spatial locality of the tensors this method can only benefit in the first and last layer of gates [67].

5. Results

In Fig. 6(a)-(f) we report the mean contraction width, \( W \), and cost, \( C \), for each geometry and optimizer as a function of circuit depth, \( d \), or cycles, \( m \). For these large tensor networks we allow each optimizer one hour to search for a contraction path. While this is not an insignificant amount of time, we note that many optimizers converge to their best contraction paths much quicker, and moreover that contraction paths can be re-used if only changing tensor values from run to run. We show the variance in \( W \) and \( C \) across 10 instances, despite the fact the tensor network structure is the same, since all the optimizers aside from qFlex/PEPs are naturally stochastic.

We first note that across the board, the KaHyPar optimizer again performs best, with little variance from instance to instance. Performance of the remaining optimizers is more difficult to rank. The tensor network simplification scheme employed here results in significant improvement over previous results even when using QuickBB to perform the actual path optimization, particularly when \( |E| \) or \( |E| \) is moderate. As the tensor networks get larger QuickBB is consistently outperformed by the other line-graph based optimizer FlowCutter.

For the Rectangular-7x7 and Bristlecone-70 circuits, which both use a CZ entangling gate, the diagonal reduction of tensors greatly simplifies the tensor networks. The methods that make use of this, aside from Greedy, perform best here, with similar values of \( C \), though interestingly KaHyPar is able to target a lower contraction width. GN and qFlex/PEPs do not use the diagonal simplification and here show similar performance.

In the case of Sycamore-53 the entangling fSim [74] gates are close to but not exactly ISWAP gates. As a result there are no diagonal reductions to be made and the simplified tensor network has no hyper-edges. Whilst FlowCutter, GN and KaHyPar find similar contraction widths, KaHyPar achieves a much lower contraction cost. This is likely due to its ability to search imbalanced partition contraction trees such as ‘Schrödinger style’ (full wavefunction) evolution. Note that for the entangling gates an approximate swapped \( \chi=2 \) decomposition can be made, resulting in a drop in fidelity based on how many of the \( m \) layers of gates this is applied to. The qFlex/PEPs method results in [67] make use of this in the first and last layer of gates for a drop in total fidelity of \(~5\%\) that reduces \( W \) by \(~4\) and \( C \) by \(~2\)^5. We only show the exact results here so as to compare all methods on exactly the same footing. If the swapped decomposition is used for all layers (Sycamore-53*) then at \( m=20 \) the corresponding drop in total fidelity is likely to be at least \(~50\%\). For the best performing optimizers in Fig. 6(c) and (f) we find little gain in doing so. We also emphasize that for the highest values of \( m \), the estimates for classical computation cost in [67] are not based on the qFlex [71] simulator and moreover involve the unbiased sampling of many bit-strings at low fidelity.

D. Practical Performance

In this final results section, we examine how the high quality contraction paths obtained so far transform into practical performance. Whilst the contraction cost estimates the time complexity of contracting a tensor network, this is irrelevant if the contraction width is too large to fit the computation into available memory. One method to bring down the space requirement of any contraction is slicing, also known as ‘variable projection’ [41] or ‘bond cutting’ [71].

1. Slicing

A tensor network can always be thought of as \( |E| \) nested summations of the product of the entries of the \( |V| \) tensors. Such an expression is associative and a contraction tree is equivalent to a re-arrangement of the summations and the insertion of a sequence of \( |V| - 1 \) parentheses defining intermediate tensors to form. However, we can also choose to perform any subset of the summations last, moving them back to the exterior of the expression. We’ll call the corresponding set of indices \( s_{\text{sliced}} \). For each fixed value of this exterior sum, the
remaining expression corresponds to a tensor network of \(|V|\) nodes, but with all the edges in \(s_{\text{sliced}}\) removed. In each network, the fixed value of indices corresponds to taking slices of any tensors with those indices. The total number of such sliced tensor networks is then 
\[
W = \prod_{e \in s_{\text{sliced}}} w(e),
\]
each of which can be contracted independently, optionally using the same tree as the original network.

The advantage of doing this is twofold: (i) the contraction width and thus required memory of each sliced tensor network, \(W_s\), is generally reduced; and (ii) the sum over independent contractions is ‘embarrassingly parallel’ and so can be easily distributed. The disadvantage is that the contraction cost of each sliced tensor network generally increases beyond \(C/d_{\text{sliced}}\) (due to redundantly repeated contractions) meaning the total sliced cost, \(C_s\), rises. Choosing which indices to slice is thus a balancing act between reducing the memory footprint without increasing the cost too much.

We employ a method similar to [41] to choose which indices to slice. Given a contraction tree \(B\), it is simple to compute the new width and cost with any index removed using Eqs. (3) and (6). We greedily choose single indices to slice based on this, repeating the process until the sliced contraction tree width reaches the desired target. Repeating this process a few times with a slight randomization to the cost score allows us to sample a moderate number of combinations for \(s_{\text{sliced}}\) and choose whichever achieves target \(W_s\) whilst minimizing \(C_s\). Crucially, we can slice trial contraction trees and report \(C_s\) within the Bayesian optimization loop, thus explicitly targeting paths which slice well.

In Fig. 7 we demonstrate the effect of different levels of slicing for the deepest Sycamore-53 circuit \((n=20)\), with either no fSim gate decomposition, or the approximate \(\chi=2\) gate decomposition for all layers (Sycamore-53*), which now shows an appreciable benefit. We allow the optimizer an hour to find paths with the lowest \(C_s\) for a given target \(W_s\). If a path targeting a neighbouring \(W_s\) achieves a lower \(C_s\), this is shown instead, and the points connected by a line. One can see that the required memory can be brought down by a factor of \(~ 16,000\) whilst keeping the FLOPs increase \(< 10\). Across this same range performing the swapped decomposition yields no benefit. Beyond that, the increase to \(C_s\) becomes significant, with the swapped decomposition becoming advantageous for heavily sliced contractions. For reference, \(W_S \sim 27\) is required to fit a contraction on a standard consumer GPU. Interestingly, the paths which achieve lowest overall \(C_s\) when targeting a large \(W_s\) (dark purple), are not good candidates for heavy slicing (yellow). Instead, the Bayesian optimizer targets a variety of different paths specific to each level of slicing.

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**FIG. 6.** Mean contraction width (upper row) and cost (lower row) as a function of gate depth (or number of ‘cycles’) for perfectly simulating a single output amplitude of random quantum circuits defined on three different qubit geometries – Rectangular-7x7 (left column), Bristlecone-70 (central column) and Sycamore-53 (right column) – for different contraction path optimizers each allowed an hour to search. The shaded regions show the standard deviation across 10 random circuit instances, non-zero despite the network structure of each being identical, since all optimizers but the qFlex/PEPs approach are naturally stochastic.
FIG. 7. Sliced contraction width vs. cost for computing a single amplitude of an $m = 20$ cycle random Sycamore circuit using the KaHyPar optimizer. The two sets of markers correspond to how the fSim gate is applied: either the tensor is not decomposed and left rank-$4$, or the two qubits are first swapped and then a decomposition is performed with only the two dominant singular values kept – Sycamore-53 and Sycamore-53* respectively. Points joined by a line are sliced from the same original contraction tree, with colour given by what contraction width was being targeted by the Bayesian optimization. Each optimizer targeting a particular $W_s$ was allowed 1 hour to search.

2. Benchmarks

To demonstrate that the contraction paths and calculated costs translate well into real world performance, we here report actual times for contracting a single perfect fidelity amplitude on a single GPU for various circuits. All tensor network manipulations and contractions were performed using quimb [60]. For each run, we allow the path optimizer to search for 1 hour in the space of paths sliced to $W_s = 27$. We then compile the resulting contraction using JAX [75] and run it on a NVIDIA Quadro P2000 which has 5GB of memory and theoretical single precision performance of 3.031 teraFLOPs. Both the path finding and compilation time are one-off costs per circuit and the times we report are only for performing the contraction. All the examples shown require some degree of slicing to fit onto the GPU, so we also show the sliced cost and how this compares to the best non-sliced cost. This slicing overhead is the increase in cost induced by squeezing the contraction into 5GB of memory. Finally we compare the achieved FLOP rate to theoretical maximum for the GPU.

The results are shown in Tab. I. For this specific task, and to the best of our knowledge, these generally represent state-of-the-art performance. For the rectangular and Bristlecone geometries, there is little inefficiency induced by slicing the contractions down to fit into memory. On the other hand, the performance extracted from the GPU via JAX is not great, likely due to the fact that the corresponding tensor networks have hyper-edges resulting in pairwise contractions that do not dispatch to matrix-matrix multiplication. For Sycamore-53, there are no hyper-edges and the realised FLOP rate is close to the theoretical limit of the GPU. On the other hand, there is much greater inefficiency induced by slicing the contractions down to $W_s = 27$. For $m = 20$ this overhead is very significant, representing the far right point of Fig. 7. From that same figure it can be seen that performing the swapped decomposition alleviates the slicing overhead, and indeed we find this to be the case with the Sycamore-53* benchmarks, though the introduction of hyperedges again lowers the FLOPs efficiency. From Fig. 7 it can also be seen that there are steady gains to be made by allowing a higher $W_s$, either through simply more memory or moving to a distributed computing setting. In the latter case, sliced indices might instead be suggestive of how to partition the initial tensors.

V. SUMMARY AND CONCLUSION

We have introduced heuristic algorithms for the contraction of arbitrary tensor networks that show very good performance across a range of benchmarks. Through a stochastic hyperoptimization over the parameters of each of the algorithms, we obtain near-optimal contraction paths that yield exponential speedups over the state-of-the-art contraction algorithms. We find that the contractor based on hypergraph partitioning, in particular, often outperforms all other methods. We demonstrated how this translates to superior performance in the simulation of computing amplitudes on Google quantum chips. New algorithms can be straightforwardly added to the Bayesian tuning approach.

Due to the generality of tensor networks, our results can help advance applications in a variety of fields. The algorithms introduced here can be directly employed in the calibration of ever larger quantum chips, with techniques such as cross-entropy benchmarking. They can also be used to accelerate classical computational tasks related to machine learning and artificial intelligence in general, such as inference and model counting. Finally, incorporating controllable schemes for approximate contractions into the methodology introduced here is a promising domain of future research.

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[1] F. Verstraete, V. Murg, and J. Cirac, Adv. Phys. 57, 143 (2008).
[2] R. Orús, Ann. Phys. (N. Y), 349, 117 (2014).
[3] J. C. Bridgeman and C. T. Chubb, J. Phys. A Math. Theor. 50, 223001 (2017).
[4] J. D. Biamonte and V. Bergholm, arXiv:1708.00006 (2017), arXiv:1708.00006.
TABLE I. Benchmark times and other information for computing a single amplitude of random circuits, in single precision. The time shown is for the contraction only, using a NVIDIA Quadro P2000 for which a target sliced contraction width $W_s = 27$ suffices for its 5GB of memory. Times with an asterisk are estimates extrapolated from computing the first 100 of $d_{sliced}$ contractions. The sliced cost, $C_s$, is always higher than the best cost without slicing, $C_{best}$ (shown in Figs. 6(d), (e) and (f)). As such, the ‘slicing overhead’ indicates the inefficiency induced by squeezing the contraction into 5GB. The FLOPs efficiency compares the theoretical single precision performance of the Quadro P2000, 3.031 teraFLOPs, with $(8C_s$/time).

| Circuit          | time (sec) | $C_s$       | Slicing Overhead ($C_s/C_{best}$) | $d_{sliced}$ | FLOPs Efficiency |
|------------------|------------|-------------|-----------------------------------|--------------|------------------|
| Bristlecone-70 (1+32+1) | $4.18 \times 10^{-1}$ | $4.91 \times 10^{10}$ | $1.24 \times$ | 2 | 31.9% |
| Bristlecone-70 (1+36+1) | $1.74 \times 10^{1}$ | $2.06 \times 10^{12}$ | $1.05 \times$ | 2$^8$ | 31.1% |
| Bristlecone-70 (1+40+1) | $2.77 \times 10^{2}$ | $3.14 \times 10^{13}$ | $1.65 \times$ | 2$^8$ | 29.9% |
| Rectangular-7x7 (1+32+1) | $3.38 \times 10^{-1}$ | $2.84 \times 10^{10}$ | $1.49 \times$ | 2 | 22.2% |
| Rectangular-7x7 (1+40+1) | $4.80 \times 10^{1}$ | $8.12 \times 10^{12}$ | $1.35 \times$ | 2$^7$ | 44.6% |
| Rectangular-7x7 (1+48+1) | $9.40 \times 10^{4}$ | $1.20 \times 10^{16}$ | $1.33 \times$ | 2$^{18}$ | 33.7% |
| Sycamore-53 (m=12) | $5.74 \times 10^{2}$ | $1.80 \times 10^{14}$ | $7.51 \times$ | 2$^9$ | 82.6% |
| Sycamore-53 (m=14) | $4.98 \times 10^{3}$ | $1.37 \times 10^{15}$ | $13.6 \times$ | 2$^{12}$ | 72.8% |
| Sycamore-53 (m=16) | $8.01 \times 10^{6}$ | $2.41 \times 10^{18}$ | $13.0 \times$ | 2$^{22}$ | 79.4% |
| Sycamore-53 (m=18) | $8.18 \times 10^{7}$ | $2.64 \times 10^{19}$ | 42.6 | 2$^{24}$ | 85.2% |
| Sycamore-53 (m=20) | $9.74 \times 10^{10}$ | $3.10 \times 10^{22}$ | 6410 | 2$^{24}$ | 84.1% |
| Sycamore-53* (m=12) | $7.87 \times 10^{2}$ | $2.42 \times 10^{13}$ | $1.67 \times$ | 2$^9$ | 8.16% |
| Sycamore-53* (m=14) | $2.92 \times 10^{3}$ | $2.53 \times 10^{14}$ | $2.63 \times$ | 2$^{12}$ | 22.9% |
| Sycamore-53* (m=16) | $3.01 \times 10^{6}$ | $3.43 \times 10^{17}$ | $7.43 \times$ | 2$^{22}$ | 30.1% |
| Sycamore-53* (m=18) | $2.66 \times 10^{7}$ | $3.62 \times 10^{18}$ | $11.3 \times$ | 2$^{24}$ | 30.6% |
| Sycamore-53* (m=20) | $7.17 \times 10^{9}$ | $1.50 \times 10^{21}$ | 431 | 2$^{24}$ | 55.3% |

[5] M. Levin and C. P. Nave, Phys. Rev. Lett. 99, 120601 (2007).
[6] G. Enevby and G. Vidal, Phys. Rev. Lett. 115, 180405 (2015).
[7] G. Enevby, Phys. Rev. B 95, 045117 (2017).
[8] A. Cichocki, N. Lee, I. Oseledets, A.-H. Phan, Q. Zhao, and D. P. Mandic, Found. Trends Mach. Learn. 9, 249 (2016).
[9] A. Cichocki, N. Lee, I. Oseledets, A.-H. Phan, Q. Zhao, M. Sugiyama, and D. P. Mandic, Found. Trends Mach. Learn. 9, 431 (2017).
[10] L. Dueñas-Osorio, M. Y. Vardi, and J. Rojo, Struct. Saf. 75, 110 (2018).
[11] I. L. Markov and Y. Shi, SIAM J. Comput. 38, 963 (2008).
[12] E. Stoudenmire and D. J. Schwab, in Advances in Neural Information Processing Systems 29, edited by D. D. Lee, M. Sugiyama, U. V. Luxburg, I. Guyon, and R. Garnett (Curran Associates, Inc., 2016) pp. 4799-4807.
[13] E. M. Stoudenmire, Quantum Sci. Technol. 3, 034003 (2018).
[14] C. Roberts, A. Milsted, M. Ganahl, A. Zalcman, B. Fontaine, Y. Zou, J. Hidary, G. Vidal, and S. Leichenauer, arXiv:1905.01330 (2019), arXiv:1905.01330.
[15] H. C. Jiang, Z. Y. Weng, and T. Xiang, Phys. Rev. Lett. 101, 090603 (2008).
[16] Z.-C. Gu and X.-G. Wen, Phys. Rev. B 80, 155131 (2009).
[17] Z. Y. Xie, J. Chen, M. P. Qin, J. W. Zhu, L. P. Yang, and T. Xiang, Phys. Rev. B 86, 045139 (2012).
[18] H.-H. Zhao, Z. Y. Xie, T. Xiang, and M. Imada, Phys. Rev. B 93, 125115 (2016).
[19] M. Bal, M. Mariën, J. Haegeman, and F. Verstraete, Phys. Rev. Lett. 118, 250602 (2017).
[20] S. Yang, Z.-C. Gu, and X.-G. Wen, Phys. Rev. Lett. 118, 110504 (2017).
[21] Y.-Y. Shi, L.-M. Duan, and G. Vidal, Phys. Rev. A 74, 022320 (2006).
