Superconducting-semiconducting voltage-tunable qubits in the third dimension

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We propose superconducting-semiconducting (super-semi) qubit and coupler designs based on high-quality, compact through-silicon vias (TSVs). An interposer “probe” wafer containing TSVs is used to contact a sample wafer with, for example, a superconductor-proximitized, epitaxially-grown, germanium quantum well. By utilizing the capacitance of the probe wafer TSVs, the majority of the electric field in the qubits is pulled away from lossy regions in the semiconducting wafer. Through simulations, we find that the probe wafer can reduce the qubit’s electric field participation in the sample wafer by an order of magnitude for thin substrates and remains small even when the epitaxial layer thickness approaches 100 $\mu$m. We also show how this scheme is extensible to multi-qubit systems which have tunable qubit-qubit couplings without magnetic fields. This approach shrinks the on-chip footprint of voltage-tunable superconducting qubits and promises to accelerate the understanding of super-semi heterostructures in a variety of systems.

INTRODUCTION

Solid-state quantum devices based on superconducting Josephson junctions have formed the basis for a variety of new quantum information technologies. Circuit QED\textsuperscript{[1]}, for example, has inspired the development of both qubits and associated control circuitry, such as readout resonators and parametric amplifiers\textsuperscript{[2–4]}. More recently, these techniques and technologies have been increasingly incorporated into semiconductor-based qubits for control, readout and long-range coupling\textsuperscript{[5–8]}. In parallel, devices with voltage-tunable superconducting-semiconductor (super-semi) junctions\textsuperscript{[9–12]}, known as gatemons, have emerged as an interesting avenue both for developing new kinds of devices and for exploring the fundamental physics associated with highly transmissive channels\textsuperscript{[13, 14]}.

One of the important challenges in this area is identifying and reducing the sources of microwave loss in these new hybrid super-semi devices. An extensive body of research has focused on characterizing and improving dielectric loss at surfaces and in bulk substrates for superconducting qubits\textsuperscript{[15–21]}. Similar work in semiconductor-dot qubits focuses on materials improvements to reduce charge noise\textsuperscript{[22–25]}. The fabrication of gatemon qubits containing super-semi Josephson junctions (JJs), similar to dot-resonator experiments\textsuperscript{[26–28]}, typically involves additional design and process steps to prepare and position the semiconductor element relative to the superconducting components. In particular, maintaining sufficient quality of the superconducting elements while maintaining voltage-tunability of the super-semi JJ requires removal of excess lossy material in the case of 2D electron/hole gas (2DEG/2DHG) based gatemon devices\textsuperscript{[29, 32]}. These complications can lengthen the iterative process between device fabrication and measurement and may also impede progress toward multi-qubit demonstrations.

Flip-chip technology, in which the active components of both a probe wafer and sample wafer are placed facing each other with a small (or zero) separation between wafers, increases the options for materials choices and signal routing while reducing fabrication demands\textsuperscript{[33–35]}. Through-Silicon Via (TSV) technology allows for an additional layer of connectivity and signal routing\textsuperscript{[36]} and has been recently integrated into active components used in superconducting control lines and readout\textsuperscript{[37]}, as well as qubits\textsuperscript{[38]}. In this work, we propose the use of this technology for gatemon qubit and coupler designs with active components on two different wafers.

DEVICE DESCRIPTION

A schematic diagram of the device which consists of “probe” and “sample” wafers in a flip-chip configuration is shown in Fig. 1. The silicon probe wafer incorporates superconducting TSVs, which connect device components on its front and back surfaces. Separation between the two wafers is defined by etched silicon spacers on the edges of the probe wafer\textsuperscript{[39]}, and the chips are connected via superconducting bump bonds\textsuperscript{[33]}. A crucial element of this scheme is that the majority of the qubit electric field energy is confined to the bulk of the (high-quality) probe wafer, and away from both the device wafer and the lossy metal-air interfaces. This distinguishes the present proposal from a recent work\textsuperscript{[40]} that made use of flip-chip technology, in which the pads of a transmon qubit were bump bonded across two wafers.

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Dielectric loss plays a dominant role in limiting the quality factors and lifetimes of superconducting resonators and qubits. The excited-state lifetime, $T_1$, of a transmon qubit [45] with frequency $\omega$ can be approximated as:

$$\frac{1}{T_1} = \frac{\omega}{Q} = \omega \sum_i \frac{P_i}{Q_i} + \Gamma_0,$$  

where the decay rate has been broken into a sum of terms associated with dielectric losses in different materials and interfaces (each with a fractional participation of $P_i$ and quality factor $Q_i$) and a term $\Gamma_0$ which captures the decay rate due to all other mechanisms (such as quasiparticle tunneling across the JJ [46] and damping due to coupling to the measurement circuitry [47, 48]). Each $P_i$ can be calculated via finite-element simulation, by defining voltages on the qubit electrodes, solving for the DC electric field across the device, and integrating the field in each of different dielectric volumes, 

$$P_i = \int_{V_i} \varepsilon_i |E_i|^2/U_{tot},$$  

where $\varepsilon_i$ is the dielectric constant of a region and $U_{tot}$ is the total energy stored in the system. We simulate the electric field distribution over four volumes: the two Si substrates, the SiGe epitaxial layers, a 5 nm thick oxide layer on top of the qubit and ground plane, and the vacuum between the two wafers (here assumed to be separated by 4 $\mu$m). For comparison, we also simulate a traditional planar gatemon design. We approximate the multilayer epitaxial quantum well heterostructure as a uniform block of Si$_{0.8}$Ge$_{0.2}$ with a dielectric constant of $\varepsilon_r = 12.6$ and calculate the $P_{SiGe}$ as a function of the SiGe layer thickness (Fig. 2). To verify that the DC electric field accurately captures the field participation for the planar and 3D geometries, we add a lumped element inductor between the qubit capacitors, find the eigenmodes of the system, and calculate $P_{SiGe}$ near the qubit frequency of 4-5 GHz. The data from the eigenmode solver (green and red stars in Fig. 2) is in good agreement with the DC field solutions, indicating that for these qubit geometries, using the simpler electrostatic

![Figure 1](image-url)
screw is sufficient to accurately model the field participation. For SiGe layers < 10 µm, $P_{\text{SiGe}}$ is an order of magnitude smaller for the 3D TSV-based devices compared to the planar gatemon, and for SiGe thicknesses above 10 µm, $P_{\text{SiGe}}$ saturates at around 5%.

A reduction in $P_{\text{SiGe}}$ is particularly advantageous when the SiGe loss tangent in the epitaxial layers ($\tan \delta_{\text{SiGe}}$) is large compared to that of bulk Si. The loss in bulk SiGe is believed to arise from threading dislocations originating at the interface between the buffer layer and the epitaxial heterostructure grown on the surface; however, its exact origin is a matter of ongoing study [44]. We compare the quality factors of the planar and 3D TSV devices using the calculated participation factors and recently reported value of $\tan \delta_{\text{SiGe}} = 1.6 \times 10^{-5}$ [44]. Fig. 2 shows the ratio of $Q$ for the 3D TSV design ($Q_{\text{TSV}}$) to that of the conventional planar design ($Q_{\text{planar}}$) as a function of $Q_{\text{TSV}}$. Here, simplifying assumptions have been made that $\tan \delta_{\text{SiGe}}$ is uniform as a function of SiGe thickness. In future experimental work, measurements of the loss in these devices will elucidate to what degree this assumption is valid. For thick SiGe layers, the 3D design can yield already significant improvement at the currently-achievable $Q_{\text{TSV}}$ [35].

MULTI-QUBIT DEVICES

While we have so far motivated our 3D TSV design because of its potential for reducing loss and minimizing processing of the sample wafer containing the semiconductor heterostructure, the design also supports a novel two-qubit coupling scheme based on voltage-controlled tunable couplers. Tunable coupling between qubits has the potential for higher on/off ratios of interaction between qubits compared to systems based on fixed two-qubit coupling and microwave-drive-activated gates [50]. This kind of quasistatic controllable coupling between superconducting qubits is typically achieved by modulating the magnetic flux bias applied to a nonlinear coupler circuit (such as a SQUID), thereby changing the effective coupling strength between qubits [51, 52]. To minimize the resulting additional susceptibility to flux noise via the coupler circuits, they are typically designed so that a relatively large difference in coupler flux bias separates their on and off states. However, as the circuit size and the number of qubits and couplers increases, it becomes increasingly challenging to independently control these large flux bias signals, due to the nonlinearity and nonlocality of Meissner screening of these signals by surround-
ing superconducting circuit elements.

These difficulties could in principle be avoided if it were possible to use \textit{voltage-sensitive} coupler circuits, since electrostatic shielding for reduction of parasitic capacitive coupling is much more well-controlled and extensible. In fact, proposals for electrostatically-tunable couplers exist back to the early days of Cooper-pair box qubits \cite{54}. However, these kinds of circuits were quickly found to be impractical experimentally due to the ubiquitous presence of nonstationary, low-frequency electric noise, in the form of slowly drifting offset charges and quasiparticle tunneling events \cite{54,55}. Gatemon qubits present a new opportunity to revisit these schemes, since their voltage tunability is of an entirely different, semiconducting character, and could be dominated by less severe noise processes. The proposed TSV-based 3D design presented here gives a natural platform for realizing such schemes.

We propose constructing the coupler and qubits out of the TSV-based gatemons in the transmon regime. This multi-qubit system can be described by the following Hamiltonian \cite{51,57,58}:

\[ H/h = \sum_{i=1,2} \left( \omega_i a_i^\dagger a_i + \frac{\alpha_i}{2} a_i^\dagger a_i^\dagger a_i a_i \right) + \sum_{i<j} g_{ij}(a_i - a_i^\dagger)(a_j - a_j^\dagger) \]

where \( \omega_i \) and \( \alpha_i \) are the qubit/coupler frequencies and anharmonicities respectively, \( g_{ij} \) are the coupling strength between the qubits and coupler, and \( a_i^\dagger \) (\( a_i \)) are the creation (annihilation) operators for each qubit and coupler. A schematic of the multi-qubit system is shown in Fig. 4. Although this device layout can be used with most types of coupling schemes, we highlight the system similar to \cite{57} in which two differential transmons were coupled via a tunable coupler with a frequency lower than those of the two qubits. We note that an in depth theoretical treatment of coupling strengths and fidelities for several transmon-gatemon systems has been previously reported \cite{59} and that here, we explore the particular transmon gatemon coupler system to understand the coherence impact on the transmons from the reduced gatemon coherence. The qubit-qubit interaction is of the form ZZ with an interaction strength \( \zeta = \omega_{11} - \omega_{10} - \omega_{01} + \omega_{00} \), where \( \omega_{ij} \) are the frequencies of each qubit in the coupled system. The Hamiltonian in Eqn. 3 is numerically diagonalized to find the qubit and coupler frequencies as well as the magnitude of \( \zeta \). In this treatment, the coupler is assumed to remain in its ground state.

A short voltage pulse on the gate TSV adjusts the tunable-coupler frequency \( \omega_c \) and changes the magnitude of \( \zeta \) to perform a controlled-Z gate between the two qubits. As the coupler frequency is adjusted by the change in junction transparency (a local effect on the scale of the junction dimensions) cross-talk from adjacent coupler pulses is expected to be substantially reduced compared to flux-based control schemes which have crosstalk typically on the order of \( \sim 10\% \) \cite{60}. Figure 5 shows \( \zeta \) vs. \( \omega_c \) for three different sets of couplings chosen to have similar idle frequencies.

One potential area of concern of this coupling scheme is the deleterious effects of gate noise, which changes \( \omega_c \) and will shift the dressed qubit frequencies \( \omega_{q1} \) causing a reduction in their \( T_2 \), similar to what has been noted in flux based tunable coupling schemes \cite{61}. In a hybrid system where the coupler is fabricated with a gatemon and the qubits are transmons with Al/AlO \(_x\) JJ’s, we can quantify the impact of this gate voltage coupler noise on qubit coherence by observing the dressed qubit frequencies as a function of the strength of gate noise. For each of the parameter sets shown in Fig. 5 \( \omega_c \) is set such that \( \zeta = 0 \), with an additional offset from the idle point, \( \epsilon \). \( \epsilon \) is chosen from a zero-mean Gaussian distribution of coupler frequencies with a width of \( \sigma_{\omega_c} \). We solve Eqn. 3 for one thousand different values of \( \epsilon \) for a fixed value of \( \sigma_{\omega_c} \) (Fig. 5 c) to obtain the variation in dressed qubit frequencies. As the magnitude of gate voltage noise is not something that is known \text{\textit{a priori}}, we repeat this processes for different \( \sigma_{\omega_c} \) (Fig. 5 d). For gatemon coupler coherence less than 1 \( \mu s \), corresponding to \( \sigma_{\omega_c} \approx 0.3 \text{ MHz} \), the coherence limit via this dephasing mechanism for the qubits is still above 100 \( \mu s \). This is encouraging, as coherence times much greater than 1 \( \mu s \) have already been demonstrated in gatemon devices \cite{10}, indicating that this scheme is compatible with existing devices. We note that as the strength of coupling between the qubits and resonators is increased, there is a reduction in the qubit \( T_2 \) which implies that a balance will have to be made between strong coupling for fast two-qubit gates, but not so strong as to significantly impact the qubit coherence times.

\section*{CONCLUSION}

We have proposed a novel type of super-semi qubit device formed across two wafers. This design allows for minimal processing of the sample wafer as well as an improvement to the qubit coherence for very thick and lossy sample substrates. This scheme is also compatible with a high coherence, magnetic field-free, multi-qubit coupling architecture. Although we considered a particular use case of the TSV probe wafer for qubits, the modular nature of probe makes it compatible as a tool for studying other systems such as layered 2D materials \cite{62} in which processing of the sample wafer could be drastically simplified.
FIG. 4. A schematic for the multi-qubit systems directly coupled (a) or coupled via an intermediate coupler (b). Both schemes are compatible with capacitive (c), inductive (d), or tunable inductive coupling (e). As in the single qubit case, neighboring qubits are shielded with a fence of TSVs (blue rings) to reduce parasitic capacitance between non-nearest neighbor qubits.

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FIG. 5. Simulation of two qubits coupled via a tunable coupler. (a) Effective ZZ coupling strength between the qubits as a function of coupler frequency for three parameter sets, $g_{1c} = g_{2c} = 110$ MHz, $g_{12} = -6$ MHz (set 1), $g_{1c} = g_{2c} = 70$ MHz, $g_{12} = -2.5$ MHz (set 2), and $g_{1c} = g_{2c} = 150$ MHz, $g_{12} = -11$ MHz (set 3), with $\alpha_{1,2,c} = -260$ MHz in all cases. These parameters are chosen such that the coupler idle frequency is similar for the three parameter sets. (b) The dressed qubit frequencies for the two qubits vs. the coupler frequency. The finite derivative of $d\omega_q/d\omega_c$ implies that changes to the coupler frequency, $\sigma_{\omega_c}$ though charge noise or gate voltage fluctuations moves the qubit frequencies. (c) A histogram of the difference between the noise free and noisy dressed qubit frequencies for a thousand different values of $\epsilon$ for a $\sigma_{\omega_c} = 1$ MHz. This can be then converted to a $T_2$ for the qubits based on the strength of noise in the coupler (d).

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