Hardware calibrated learning to compensate heterogeneity in analog RRAM-based Spiking Neural Networks

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Abstract—Spiking Neural Networks (SNNs) can unleash the full power of analog Resistive Random Access Memories (RRAMs) based circuits for low power signal processing. Their inherent computational sparsity naturally results in energy efficiency benefits. The main challenge implementing robust SNNs is the intrinsic variability (heterogeneity) of both analog CMOS circuits and RRAM technology. In this work, we assessed the performance and variability of RRAM-based neuromorphic circuits that were designed and fabricated using a 130 nm technology node. Based on these results, we propose a Neuromorphic Hardware Calibrated (NHC) SNN, where the learning circuits are calibrated on the measured data. We show that by taking into account the measured heterogeneity characteristics in the off-chip learning phase, the NHC SNN self-corrects its hardware non-idealities and learns to solve benchmark tasks with high accuracy. This work demonstrates how to cope with the heterogeneity of neurons and synapses for increasing classification accuracy in temporal tasks.

I. INTRODUCTION

Resistive Random Access Memories (RRAMs) have been shown to have a large potential for locally storing the synaptic weights and enabling “in memory computing” in Artificial Neural Networks (ANNs) [1]. The assembly of resistive memories organized as a crossbar naturally implements the Multiply And Accumulate (MAC) operation in ANNs (Fig. 1). However, one of the major problems of this ANN approach is network scalability. In this approach, the output current at each column, and the overall power budget increase linearly with the number of devices being read (i.e. number of activated rows), thus strongly limiting the array size (Fig. 1). Another limitation is the overhead required by the Digital-to-Analog (DAC) and Analog-to-Digital (ADC) circuits needed for the conversion. To overcome these issues we focus on the hardware implementation of analog Spiking Neural Networks (SNNs). SNNs have typically very sparse activations, so the number of activated rows at any instance of time is very small, significantly reducing the current and power consumption at each column (Fig. 1). Moreover, analog neurons and synapses in SNNs do not require DACs and ADCs, resulting in a further reduction of energy consumption and area [2].

The basic building block of analog SNNs is composed of Leaky Integrate and Fire (LIF) neurons. In SNNs LIF neurons transmit voltage pulses (spikes) to multiple columns of one resistor-one-transistor (1T1R) devices, which encode the network synaptic weights in their conductance. The resulting current is the weighted sum of all the synaptic outputs. In the architecture we propose these currents are then integrated temporally by a shared Differential Pair Integrator (DPI) circuit (Fig. 1), which is a subthreshold log-domain low-pass filter [3], [4]. To realize a multi-layer neural network, such basic blocks can be chained together in a modular way.

However, both analog circuits and RRAMs exhibit device variability. In this work, we compared the performance of SNNs trained to carry out three different tasks, with different degrees of hardware heterogeneity. The CMOS variability affects the neuron’s and synapse’s time constants. The RRAM variability affects the synaptic weights. We propose a Neuromorphic Hardware Calibrated (NHC) SNN, where off-chip training is calibrated on experimentally measured data and hardware non-idealities. This approach allows achieving classification accuracy on three different tasks, comparable to equivalent full-precision (32-bit floating point) software-based simulations. Moreover, we demonstrated that heterogeneity in neuron and synapse time constants originates a richer system temporal dynamics, thus improving the accuracy for tasks with temporal structure. Experiments have been conducted on custom analog LIF neuron and DPI synapse circuits as well as on a 4 kb HfO2 crossbar 1T1R memory array fabricated in a commercial 130 nm technology node.

II. HETEROGENEITY IN NEURONS AND SYNAPSES

We designed, fabricated, and tested analog CMOS-based LIF neuron and synapse circuits (Fig. 2a,b). The design is based on the DPI circuit [3], [4], which implements a low pass filter with time constant controlled by a tunable bias voltage. In arrays of such circuits the same bias voltage produces heterogeneous leak current. To derive the DPI circuit time constant we applied an input voltage pulse at the input (Vin) and measured the voltage at the capacitor. The resulting trace was fitted with an exponential function. By modulating the Vlk bias of the neuron (or Vtau bias of the synapse), we modified the current leak rate, resulting in different time constants (Fig. 2). The measurements have been repeated over 100 samples and the time constant extrapolated from the response of Vmem/Vsyn. Variability in the neuron and synapse time constants is quantified at about 30% in standard deviation over the mean.
III. Variability in the RRAM and Synaptic Weights

To obtain 8 conductance levels per RRAM device in a 4 kb 1T1R array, we used the multilevel smart programming procedure described in [5]. We then measured and characterized the distribution of the conductances in time (see Fig. 3a). As shown, the smart programming procedure yields tightly distributed conductance levels, which broaden with time due to temporal variability of the devices. RRAMs show 3 degrees of temporal variability that take place at different time scales (Fig. 3b). Relaxation takes place just after programming (milliseconds) and broadens all the conductance levels distributions. Data retention causes long term (hours) variation of the conductance, particularly affecting the lower conductance levels, whose mean of the distribution decreases with time (Fig. 3c). Read-to-Read (R2R) noise does not affect the shape of the conductance distribution, although when looking at individual devices there are fast temporal fluctuations of conductance due to reading disturbances and Random Telegraph Noise (RTN). We evaluate the RTN component in R2R via the $\Delta G/G$ figure of merit (Fig. 3d), measuring the conductance jumps $\Delta G$ due to RTN. The result is in line with the literature [6]. Finally, the Power Spectral Density of the 8 conductance levels shows that the amount of noise is inversely proportional to the conductance and is general of the 1/f type (Fig. 3e), as also observed in [7].
VI. IMPACT OF RRAM NON-IDEALITIES ON PERFORMANCE

The RRAMs support up to 8 distinct conductance levels, enough to saturate performance for simple datasets, as demonstrated in [5]. The impact of the RRAM temporal variability approach recovers this loss in performances. Moreover, heterogeneity in time constants surprisingly improves the accuracy on datasets with rich temporal structure (ECG and SHD). This result is in agreement with the theoretical study performed in [11] and could be explained by the richer temporal dynamics of the heterogeneous substrate.

|               | Weights | N-MNIST (%) | ECG (%) | SHD (%) |
|---------------|---------|-------------|---------|---------|
| ANN           | float32 | 97.5        | 95.5    | 89.0    |
| NC SNN        | float32 | 90.2        | 63.7    | 58.4    |
| Hom. SNN      | float32 | 97.4        | 94.5    | 72.5    |
| NHC SNN       | float32 | 97.5        | 94.9    | 74.9    |
| 4bits         | 96.7    | 91.4        | 71.6    |
| RRAM t=0s     | 96.8    | 91.2        | 71.2    |
| RRAM t=5s     | 96.2    | 90.2        | 67.5    |
| RRAM t=1h     | 95.3    | 89.9        | 60.4    |

TABLE I: NHC SNN results and comparison with ANN, Non-Calibrated SNN (NC SNN) and Homogenous SNN (Hom. SNN).

is shown in Fig 4. Relaxation causes an immediate decrease in performance (Fig 4b). The decrease of performance over time due to poor data retention (Fig 4a) is minimal for simpler tasks like MNIST (blue) and ECG (red), while it is more pronounced for SHD (green). R2R noise slightly varies the conductance values at each inference operation (Fig 4c), causing accuracy to fluctuate. Furthermore, the impact of failures in the RRAM-based neuromorphic chip is evaluated. A failure is represented by a device stuck at either low (1 µS ± 0.5 µS) or high (200 µS ± 25 µS) conductance. The accuracy as a function of the RRAM’s Bit Error Rate (BER) is shown in Fig 5a: SNN models are resilient up to BER of $10^{-3}$. In order to mitigate faults, we can retrain the SNN with broken RRAMs (Fig 5b), to recover performance. MNIST is re-learned with just one learning epoch, while ECG and SHD require a few more epochs to recover. Overall, the performance is almost fully restored in all cases.

VII. ENERGY ASSESSMENT

To assess the efficiency of an RRAM based neuromorphic processor we compare their energy per inference sample with a mixed-signal neuromorphic processor, DYNAP [12]. DYNAP uses similar LIF neuron and DPI synapse circuits, but employs an asynchronous digital communication protocol to implement network connectivity. The energy consumption for the RRAM-based system is estimated by means of SPICE simulations and
is more than 1 order of magnitude lower than that of DYNAP (Fig. 6a). Energy is dominated by the RRAMs (that store the synaptic weights and define the network topology) in the reading operation. However, the RRAM associated energy is about 1 order of magnitude less than that of the communication protocol used in DYNAP (Fig. 6b). Furthermore, SNN computation is very sparse, reducing the number of simultaneously activated rows of the RRAM array, yielding small currents on the column lines (Fig. 6c).

VIII. CONCLUSION

We proposed a new approach for training RRAM-based analog SNN that takes into account the hardware details. The results show, that SNNs trained with our approach reach competitive classification accuracy levels, and that the heterogeneity of neurons and synapses improves network performance for temporal tasks. Although the use of RRAMs could result in slightly reduced performance over time, they can reduce the energy cost per inference by one order of magnitude with respect to conventional Mixed-Signal processors.

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