Fabrication of metal nanowires

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This review article discusses and compares various techniques for fabricating metal nanowires. We begin by defining what we mean by a nanowire, and why such nanostructures are of scientific and technological interest. We then present different fabrication methodologies, describing in some detail the advantages of each. "Top-down" techniques discussed include: electron beam lithography; scanned probe lithography; step-edge and molecular beam epitaxy templating; and nanotube templating. "Bottom-up" methodologies covered include: electrodeposition into etched porous media; direct chemical synthesis; step-edge decoration; and strain-mediated self-assembly. We conclude by summarizing our observations and briefly discuss the future of metal nanowire fabrication.

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I. INTRODUCTION

Colloquially, a wire is a metallic structure extended in one (longitudinal) direction and strongly confined in the other two (transverse) directions. A fundamental attribute of such a two-terminal device is electrical continuity, i.e. the ability to transport charge along its length under a longitudinal potential bias. There is much scientific and technological interest in fabricating and understanding metal wires with transverse dimensions approaching the nanometer scale. We call such structures nanowires, and this article reviews a number of techniques for the fabrication of these objects.

For our purposes a metal nanowire has transverse dimensions (w, t) substantially below 100 nm, an aspect ratio significantly greater than one (L >> w, t), and is composed of a material that is metallic in the bulk (e.g. gold, copper, nickel). This definition is deliberately constructed to exclude from discussion some other structures known colloquially as nanowires: e.g., nanoscale metal point contacts; extended semiconductor crystals; and heterostructures (so-called "quantum wires"); and molecules used as two-terminal conductors.

It is useful to compare the sizes of nanowires with some of the physically significant length scales in metals. These comparisons emphasize the difference between nanowires and the other elongated structures mentioned above, and also show why the sub-100 nm transverse scale is interesting.

The Fermi wavelength, λ_F, is one relevant length scale. In typical bulk metals the Fermi wavelength associated with the conduction electron Bloch waves is on the order of 0.1 nm. This short wavelength is due to the high spatial density of electrons. Since λ_F << w, t except for wires of atomic cross-section, most nanowires under discussion have many conducting channels, and are well-described by three dimensional Fermi Liquid Theory. More exotic physics (e.g. Luttinger liquid properties) only becomes relevant in extremely narrow structures, when w, t → λ_F. Note that in contrast, λ_F in doped semiconductor nanowires may be on the order of tens of nanometers.

Another closely related quantity is the screening length, L_sc, the scale over which electrostatic impurities are screened by the conduction electrons. This is on the same order as λ_F. As transverse wire dimensions are reduced, an increasing fraction of the metal atoms are within L_sc of the wire surface.

Other relevant sizes are ℓ, the electronic mean free path for elastic scattering, and ℓ_tot, the mean free path for either inelastic or elastic scattering. A "good" metal has ℓ/λ_F >> 1; that is, electronic partial waves propagate many wavelengths between scattering events. Since metal nanowires are often nanocrystalline, elastic scattering in such structures is strongly influenced by grain boundary scattering. Similarly, if the transverse dimensions of the wire are sufficiently small (ℓ ~ w, t) then boundary scattering can also strongly influence nanowire conduction properties. This limit is certainly achievable at low temperatures for "clean" metals.

Related to the inelastic mean free path is the coherence length, L_φ. Consider introducing an electron in a single-particle eigenstate of the wire, and then allowing the electron to propagate while undergoing interactions with other dynamic degrees of freedom (e.g. phonons, photons, magnetic impurities, other electrons). L_φ is the distance traversed before the phase of the electron partial wave becomes poorly defined through interactions with the environment. Quantum interference corrections to electronic conduction (often referred to as mesoscopic phenomena) are typically relevant on this length scale. Because of the temperature dependence of processes involving those dynamic degrees of freedom, L_φ often varies strongly with T, tending toward larger values at lower temperatures. In a metal like silver at 1 K, L_φ ~ 1 μm.

Once L_φ > w, t, the wire is one-dimensional with respect to quantum phase coherence. One important property of such one-dimensional structures is that the motion of a single impurity or defect will then affect the conduct-
ing properties of the entire wire. Every trajectory that brings an electron from one end of the wire to the other will have to pass through the same coherent volume as the defect in question. Similarly, suppose some charged defect adjacent to the nanowire changes its state. Classically this should only affect electron trajectories passing within $L_{\text{sc}}$ of the nanowire surface; however, because of quantum coherence and mixing of transverse channels, all trajectories passing within $L_{\phi}$ must now be considered.

As wire transverse dimensions are reduced, quantum corrections to conduction become relevant at higher temperatures. In the limit of atomic-scale metal contacts, quantum effects dominate electronic transport even at room temperature. In some of the smallest nanowires considered in this article, conductance fluctuation noise from quantum interference and scatterer motion is clearly detectable at temperatures above that of liquid nitrogen.

Finally, one more useful quantity is the thermal length $L_T = \sqrt{\hbar D/k_B T}$ in diffusive wires and $\hbar v_F/k_B T$ in ballistic wires, where $v_F$ is the Fermi velocity. Consider starting two electrons near the Fermi surface with energies differing by $k_B T$, but beginning on the same trajectory. The length $L_T$ is the distance that the electrons would typically travel before their partial waves are out of step due to their slightly different energies. This scale also determines the thermal smearing of the conductance fluctuation noise described above.

Metal nanowires with transverse dimensions well below 100 nm are of scientific interest because this size range spans the lengths mentioned above. Surface scattering effects, changes in screening, and the increased importance of quantum corrections to the conductance are all topics of research that may be addressed through novel nanowire samples. Moreover, metals with substantial electronic correlation effects such as ferromagnetism and superconductivity possess additional length scales (e.g., domain wall thickness, superconducting coherence length) that further complicate wire properties. Nanowires are ideal tools for the study of such physics.

With the continued trend toward further technological miniaturization, nanowires are likely to be industrially relevant as well. Already the physical gate length for transistors is predicted to be as small as 25 nm by 2007. With the possibility of electronic devices based on individual molecules being seriously explored, fabrication of metal nanostructures on comparable scales is a topic of much interest.

As has been pointed out by other authors, fabrication processes at these length scales fall into three broad categories: lithographic processes (Sec. II) involve pattern definition through a drawing step; while templating approaches (Sec. III) use alternative means to produce a nanodetailed template and replicate some feature of that template in metal; and finally chemical synthesis and self-assembly may be employed without any patterning step at all. We begin by considering lithographic techniques.

## II. LITHOGRAPHIC TECHNIQUES

Lithographic techniques for nanowire fabrication may be divided into two classes: additive and subtractive methods. In many additive techniques some form of resist is applied to the entire substrate; the resist is then modified in a pattern definition step, turning the resist layer into a stencil, with resist material removed to expose the underlying substrate. Metallization then occurs, in which the entire resist layer is coated with a metal film of thickness $t$, usually by evaporation or sputtering. The final step is lift off, in which the remaining resist is removed by chemical means, leaving behind metal on the substrate only where the resist had been patterned. Alternately, resist-free techniques may be employed, in which the metal is “drawn” directly onto the substrate.

Subtractive techniques begin by metallizing the entire substrate with the desired wire material. Some form of resist may then be applied and patterned, with resist remaining where the wire is desired to be formed. Unwanted metal is then removed by physical etching or chemical means. Any remaining resist is then lifted off chemically. Again, there are also resist-free approaches that locally remove the excess metal to form the nanowires. For nanowire fabrication, subtractive lithographic approaches are less common than additive ones.

### A. Photolithography

We only briefly consider photolithography because of its size limitations. For more complete discussions of this extremely wide-spread technique, see Refs. [15, 16]. In this technique chemical changes in a resist material are photoactivated, with some sort of optical mask used to spatially define the regions of photochemical activity. Optics between the mask and the substrate are used to further reduce mask feature sizes when exposing the resist.

An intrinsic limitation of this technique is the diffraction limit of the wavelength of light involved. Current industrial practice typically uses 248 nm light, and through clever mask designs and specially tailored polymeric resists, feature sizes below 100 nm are possible. Further reductions are achievable, but there are enormous engineering challenges involved, since wavelengths in the deep ultraviolet (DUV) and x-ray require significant changes in the optical elements used in patterning. Extensions of projection photolithography to the 10 nm transverse size scale seem unlikely to occur, except perhaps through scanning near-field methods. We do not consider nanowire production by photolithography further.
B. Electron-beam lithography

One of the most flexible and widely used techniques for producing narrow metal nanowires is electron beam lithography (EBL). We consider this method in some detail, and certain steps (e.g. metallization) are of general concern to the other techniques that we discuss.

1. Patterning

In EBL, a resist of some type (often polymeric) is applied to the substrate, and a focused beam of high energy (typically \(> 30 \text{kV}\)) electrons is scanned over the surface, tracing out the desired pattern. The beam hits the resist and locally ionizes the constituent atoms, breaking chemical bonds and producing a cloud of secondary electrons, many of which are also sufficiently energetic to do further damage to the resist.

In “positive” polymer resists, exposed polymers are broken down into smaller units, typically with enhanced solubility in some developer solution when compared to the original material\[15, 16\]. Development removes the exposed resist, with the remaining material comprising a stencil for further processing. “Negative” resists are less common; in these materials the electron beam locally crosslinks the polymer, so that development removes the unexposed resist. Positive resists nearly always have superior resolution for isolated features such as single nanowires, in part because of some techniques described below. Thus we confine the remainder of our EBL discussion to positive resists.

Polymethylmethacrylate (PMMA) is the most commonly employed positive e-beam resist; different molecular weights of polymer (typically 495 kDaltons and 950 kDaltons) and different concentrations of polymer in carrier solvent (typically anisol or chlorobenzene) are used to tailor the resist’s exposure and viscosity properties. The resist is commonly spun onto a planar substrate which is then baked for some time. The bake is at a temperature high enough to drive off the carrier solvent yet low enough to avoid crosslinking or decomposing the polymer (say 160°C for 2 hours).

Nanowire production with a positive resist requires pattern definition in the resist, development that preserves that pattern, and a successful metallization and liftoff step. Each of these steps contains subtleties that determine the size limits of EBL-produced nanowires.

Electron wavelength is usually not an issue, since sub-Angstrom wavelengths are achievable with beam voltages in excess of a few kV. Similarly, electron beam spot size is generally not a limiting factor; electron optics can produce electron beams with atomic resolution\[20\]. The exposed area of resist is primarily limited by the size of the secondary electron cloud, which is usually much larger than the impinging beam size. All other things being equal, higher column voltages tend to produce narrower exposed patterns for two reasons: lower beam transit time to the sample minimizes relative jitter between the gun and the sample; and higher incident electron momentum produces a secondary cloud farther into the substrate, with fewer secondary exposures within the resist. A similar secondary distribution in the resist may be achieved by using extremely thin samples to reduce the total secondary yield\[21\].

Figure 1a illustrates an ideal resist exposure profile for liftoff metallization. When developed, this exposure profile should leave a clean resist overhang for liftoff, as shown. Other approaches for obtaining such a profile include double-layer resist schemes, with the lower layer possessing a higher sensitivity\[22, 23\], and using an extremely thin metal film as a top layer to produce a large downward secondary yield\[24\]. More exotic schemes include inorganic resists such as CaF\(_2\)\[25\] and self-assembled monolayer (SAM) resists\[26\].

It is challenging to convert even an ideal resist exposure profile into a completed nanowire at deep-sub-100 nm scales. Beam jitter must be extremely well-
controlled to avoid edge roughness. The development process also plays a crucial role. Significant complications arise in the development process, including: the transport of developer into and out of the exposed resist; the strong intermolecular forces between development products and unexposed resist at sub-10 nm scales; and resist swelling. These difficulties are enhanced as the aspect ratio of the resist exposure profile is increased, so that thinner resist layers are generally used for higher resolution lithography.

An alternative approach is to make do with larger feature sizes in the original resist pattern, and use subsequent steps to reduce the linewidth. For example, by applying SAM coatings to parallel metal leads, the gap between the leads can be reduced by precise amounts; subsequently evaporated metal can then form nanowires with widths ~12 nm, significantly narrower than the original pattern linewidth.

2. Metallization

Finally, as we shall see again in other fabrication techniques, the detailed choice of metallization material and method can strongly affect final nanowire morphology. Evaporation (thermal or electron beam) and sputtering are common metal deposition methods. The sticking and diffusion properties of the metal on the substrate are crucial to forming uniform and continuous metal films, let alone nanowires. For example, on clean, room-temperature GaAs, pure Au is highly mobile, adhering better to itself than to the substrate. As a result, a Au film nominally a few nm thick tends to break up into discrete grains rather than to form a continuous layer of uniform thickness.

One metallization approach that has been successful in a number of nanowire fabrication methods is to minimize the grain size of the metal. For example, alloys of Au and Pd are known to have reasonably good adhesion qualities and grain sizes on the nm scale. The ultimate limit of small grains is an amorphous metal. Quench condensation by evaporation onto extremely cold substrates can produce continuous and films of a number of metals at few-monolayer coverages. Another approach is to use “naturally” amorphous metals, such as MoGe alloys. Even with atomic lateral definition of a pattern, the narrowest nanowires possible are determined by the surface physics of the metal and any metal-substrate interface.

To summarize: EBL is a very flexible nanofabrication technique capable, under the best circumstances, of sub-10 nm linewidths on a variety of substrates. With more typical conditions, nanowires with widths on the order of 20-40 nm may be produced fairly routinely. Edge roughness is a significant issue, and even with ideal liftoff lateral definition is influenced by the patterning beam itself, the development process, and the morphology of the metal. A major advantage of the technique is that nanowires may be positioned in a variety of configurations and directions on the substrate. Furthermore, EBL requires no exotic contraints on sample treatment (e.g. ultra-high vacuum (UHV) conditions). However, the lack of atomic-level lateral definition in the resist pattern makes extension of EBL well into the sub-10 nm width regime exceedingly challenging.

C. Scanned probe lithography - additive

Lithographic techniques using scanned probes have also been employed to create sub-100 nm wide nanowires, though no scanned probe lithography (SPL) approach has yet attained the wide-spread popularity of EBL. Scanned probes (e.g. atomic force microscopy (AFM) and scanning tunneling microscopy (STM)) are natural candidates for adaptation to fabrication techniques, since the probe tip interacts with the substrate on a very local scale. A number of results have been reported in which AFM and STM have been used to modify a substrate electrochemically (see Refs. and references therein). However, we restrict our discussion to methods that result in nanowires as defined in Section 1.

1. AFM methods

AFM-based lithography techniques used for nanowire creation use three main approaches for pattern definition: direct drawing of metal onto a substrate; mechanical modification of a resist layer followed by evaporation and liftoff; or electrochemical modification of a resist layer followed by evaporation and liftoff.

Using an AFM tip in contact mode to draw various organic molecule “inks” directly onto a substrate is a technique known as “dip-pen nanolithography” 11. This method uses the adsorbed layer of water on the AFM tip under ambient conditions to “wick” ink directly to the contact point between tip and substrate. An approach similar in spirit has been demonstrated to produce Au nanowires 4 nm wide, 1 nm thick with lengths of several microns. The substrate is (111) Si that has been heated in vacuum to remove the native oxide and trigger the 7 × 7 surface reconstruction. At room temperature under UHV, an AFM tip coated by e-beam evaporation with Au is then drawn across the Si surface in contact mode. Gold atoms have sufficient surface diffusivity at room temperature that a gold wire is left behind on the Si surface where the tip had been in contact. While this technique is quite interesting, it must be performed under UHV conditions, and should only work with metals having high atomic diffusivities.

Mechanical deformation of resist by an AFM tip typically leads to a resist profile that is not conducive to liftoff processing (see Fig. 4). With a trough-shaped indentation, subsequently evaporated metal tends to cling strongly to the resist sidewalls, making a clean liftoff
problematic. One approach to dealing with this issue is that of Ref. [42]. Rather than “plowing” through a single layer of resist, the authors employ a bilayer resist scheme, using a lower layer composed of PMMA-MAA (methacrylic acid) copolymer with a considerably higher solubility than the top layer of PMMA. The cantilever tip plows through the upper layer, exposing the more soluble base layer for removal. The result is an undercut resist profile that allows good liftoff. The thick resist bilayer is also useful for producing wires that cross substrate topography. The authors produced 40-50 nm thick and wide nanowires extending over 50 nm-thick predefined contact pads.

Another way to mitigate the resist profile issue is described in Ref. [44]. A 200-300 nm thick layer of PMMA-MAA copolymer is spun onto the substrate, baked, and then coated by thermal evaporation with a 5-15 nm thick germanium layer. This Ge layer will eventually act as a suspended mask. The substrate is then coated with a 15-20 nm thick polymide layer and baked at 60 °C to drive off residual solvent. This polymide is mechanically furrowed by a Si AFM cantilever, exposing the Ge layer under the polymide. By reactive ion etching (RIE), the exposed Ge is removed, revealing the underlying PMMA-MAA: subsequent RIE in an O₂ plasma etches the PMMA-MAA vertically down to the substrate, and laterally to some extent. The suspended Ge layer now acts as a properly undercut mask for metallization and subsequent liftoff. Wires as narrow as 40 nm were made with this process.

A slightly simpler approach is described in Ref. [45]. An ultrathin (3 nm) Ti layer is evaporated on top of a baked PMMA resist layer. The AFM tip mechanically removes the Ti by abrasion as the cantilever is drawn across the surface in the desired pattern. The PMMA exposed by Ti removal is then etched by oxygen RIE to form an undercut resist pattern.

These mechanical-deformation-based AFM methods succeed as flexible approaches, capable of producing nanowires substantially below 100 nm in width on a variety of substrates. In terms of ultimate wire size, however, their capabilities appear to differ insignificantly from those of EBL. While AFMs may have atomic resolution in imaging [46] because of the extremely short-range nature of the hard-core part of the tip-surface interaction, no convenient method currently exists to use that resolution in a patterning mode. Mechanical surface modification tends instead to affect a region at least as large as the radius of curvature of a typical AFM tip, on the order of 10-20 nm.

Both conducting AFM tips and STM tips have been used as local sources of electrons to modify a resist layer chemically, in a proximal probe form of EBL. Examples of conducting AFM or STM to expose a resist layer include Refs. [47, 48, 49, 50]. This approach runs into similar limitations as standard EBL, described in Sec. II B. Despite extremely local tip-resist interactions, the actual wire widths seen in the best liftoff-processed samples remain near 50 nm. The need to sink current from the tip into the substrate at comparatively low voltages means that this method tends to work best on conducting substrates. Furthermore, since tip voltages in this method cannot approach those used in high resolution EBL, achieving a resist profile favorable for liftoff is challenging. Similarly, the thinner resist layers best-suited for this method also tend to be those least suited to metallization and liftoff.

2. STM methods

One additional scanned probe approach that does seem capable of producing nanowires with exceedingly narrow cross-sections uses UHV STM on a conducting silicon substrate. The patterning process begins with a doped (100) Si wafer in UHV that has had its native oxide removed by heating to 1250 °C for 1 minute. The surface is then exposed at 650 °C to atomic hydrogen obtained by cracking a dose of molecular hydrogen with a 1500 °C filament. The hydrogen passivates the silicon surface, forming a uniform monohydride layer that will act as a resist.

The STM tip is then biased negatively with respect to the sample by several volts and current doses on the order of 100-1000 µC/cm are used to strip the hydrogen away through electron-stimulated desorption. The depassivated Si surface is now available for metallization. Metal nanostructures have been produced with this approach using chemical vapor deposition as well as physical vapor deposition. In the former, the chemistry that deposits the metal can only occur on the depassivated Si sites. In the latter case Co was deposited at sub-monolayer coverage, and annealing allowed the Co to migrate to the unpassivated Si sites and possibly form metallic silicides. Cobalt nanowires as narrow as 3 nm were reported, though no...
FIG. 3: An STM image of a cobalt nanowire 3 nm wide on a Si surface, produced by selective depassivation and surface decoration in UHV. Figure reproduced with permission from Ref. [52], copyright 1999, American Institute of Physics.

The STM depassivation technique is the only SPL approach thus far that can approach true atomic resolution in structure definition. The restrictions on the method, however, are quite severe: UHV working conditions, a Si substrate that conducts well enough for STM, and careful control of the metallization process.

D. Scanned probe lithography - subtractive

STM, and conducting AFM, have also been employed in subtractive approaches to nanowire fabrication. The resulting devices often do not meet our definition of “nanowire” due to their small length. We briefly describe the method of Ref. here, since that work specifically addresses devices that satisfy the aspect ratio criterion of Sec. I.

A substrate of interest, in this case an oxidized Si wafer, is coated with a metal layer, 7 nm of Ti, patterned by photolithography. To eventually make a narrow wire, one starts with a wider (micron-scale) structure between larger pads; this allows wire conductance to be monitored in real time as fabrication proceeds. A conducting AFM tip is then brought into contact with the metal surface under ambient conditions (in air, 40% relative humidity, 300 K). When the tip is negatively biased by ~10-12 V with respect to the Ti layer, an electrochemical reaction takes place due to the adsorbed water at the tip-metal junction. The Ti layer immediately in contact with the tip is converted into TiO₂, with a sheet resistance greater than 1 TΩ. Using the computer to sweep out particular paths, a Ti film originally 2 μm wide was selectively oxidized, leaving an unoxidized wire 15 nm wide, 7 nm thick, and 500 nm long with a resistance of approximately 100 kΩ. Wires with nominal widths as narrow as 3 nm are reported in this work. Variations of this approach have been used on chromium and aluminum.

As pointed out in Ref. , inferring wire transverse dimensions produced in this technique from resistance measurements is nontrivial. In the smallest structures actual conducting cross-section does not scale linearly with apparent wire width. Reasons for this include the intrinsic roughness of the wire edges due to granularity of the metal, and swelling of the anodized material because of lattice mismatch between the metal and its oxide. In fact, metallic conduction is observed even in structures so narrow that oxide swelling has eliminated any AFM-image signature of unoxidized material. Feedback control of anodization using the in-situ measured wire conductance allows the electrical properties of resulting devices to be precisely controlled, but geometrical measurements of the wires are not readily performed when widths fall below 10 nm.

E. Lithographic methods: summary

Some general observations are possible. First, the prime advantage of lithographic approaches is the flexibility in nanowire geometry that is then possible. By definition lithographic methods are capable of producing nanowires of nearly any shape that may be “drawn”. Second, resist-based techniques face fundamental limitations due to the development process and the need for a resist profile that will generate clean liftoff. Third, while probes like AFM and STM are capable of extremely local examination of the properties of substrates, employing these generalized tools for precise lateral definition of nanowire structures is nontrivial. SPL often requires special substrates, metals, UHV conditions, or some combination of the three. Finally, even with atomically precise lateral definition of a hole in resist (such as STM-depassivated Si), the ultimate limits of nanowire size are set by the surface science of the constituent metal itself, and of the metal-substrate interface.

III. TEMPLATING

Templating has also proven extremely useful for the fabrication of nanowires. While a lithographic technique employs some kind of drawing to define the pattern, templating instead utilizes nanoscale surface relief to provide definition to the metal structure. The keys to nanoscale wire construction then become finding a suitable tem-
plate and controlling metal morphology. Below we discuss a number of templating approaches.

A. Step-edge lithography

One templating approach that has proven quite successful and innovative is “step-edge lithography” (SEL), as illustrated in Fig. 4. On a suitable substrate such as a glass slide, an initial patterning step is used to define an edge; for example, photolithography and liftoff processing may be used to define a large chromium pad on the substrate. The sample is now placed in an ion mill, and a beam of Ar ions is directed to impinge at normal incidence on the substrate. Because of the differential etch rate between the substrate and the chromium, the area covered by the chromium becomes a mesa, while the exposed substrate surface is sputtered away by the ion beam. The chromium is then removed with a standard wet etch. This has now produced surface relief on the substrate (a crisp step at the edge of the mesa) with a critical dimension (the step height) determined by the ion etch time.

Next, metal is deposited at normal incidence onto the substrate. As with all such metallization steps, to achieve transverse wire dimensions on the few-nm scale requires the metal to have nm-scale grains or be amorphous. A AuPd alloy was first used to demonstrate this technique. Now the metal-coated substrate is placed back in the ion mill, with the ion beam this time incident on the sample at a substantial angle ($\sim 45^\circ$) from the normal. The ion mill then sputters away the exposed metal on top of the mesa as well as that on the remainder of the substrate, with the exception of one place: The step at the mesa edge geometrically protects the metal right next to the step from the etching effects of the ion beam. The ideal end result is a nanowire of triangular cross-section running the length of the mesa edge. The critical wire dimensions have been determined by metal deposition (thickness) and template geometry (width via the etch angle). Contacts to larger pads may then be made via additional lithography steps or other means.

This method has been employed to make 10 nm-scale nanowires from a variety of materials, including normal metals, superconductors, and ferromagnetic metals. Nanowires made with the step-edge approach may be hundreds of microns long. A limitation is that, because of the shadowing involved, the lateral definition of the wire is only as good as the collimation of the incident ion beam. Similarly, by necessity the ion beam damages the exposed wire surface. Furthermore, the edge roughness of the original step is set by the initial lithography and chrome metallization processes. Finally, this technique works best if the ion etch rate of the deposited metal is on the order of or faster than that of the substrate.

A clear advantage of this technique is its ability to reach extremely small lateral length scales while preserving a large aspect ratio. The tradeoff when compared to EBL or SPL is one of flexibility; step-edge lithography is very good for achieving linear nanowires in isolation, rather than for producing multiple nanowires intersecting at arbitrary angles.

B. MBE-defined templates

A recent innovation in nanowire fabrication with a number of similarities to the step-edge technique is described in Refs. 12, 68. However, rather than relying on lithographic and ion etch processes to provide lateral definition to the nanowires, the authors take advantage of the remarkable thickness resolution possible in molecular beam epitaxy (MBE). In the GaAs/AlGaAs system monolayer thickness control of MBE growth is typical. This MBE templating approach is shown in Fig. 5.
This technique begins with a 500 μm thick undoped (100) GaAs substrate, onto which has been grown a layered structure. To produce single wires of width $d$, the layers are: 2 μm thick $Al_{0.3}Ga_{0.7}As$, a GaAs layer of thickness $d$, and an additional 2 μm of $Al_{0.3}Ga_{0.7}As$. All of these layers are undoped. The substrate is then cleaved into a strip approximately 5 mm by 15 mm to expose the (011) surface. The growth layer thickness $d$ is now the width of a GaAs strip on the (011) surface.

The strip is then etched to produce a trough; wire material is deposited, the resist is lifted off, and a directional ion etch removes excess material; a nanowire is left in the trough, ready for further lithography to define multiple leads.

Metal is then deposited by e-beam evaporation or sputtering at normal incidence to the (011) surface, into the trough and onto the surrounding exposed wafer material. After liftoff of the PMMA layer, the assembly is placed in an ion etching system (either an RIE or an ion beam) so that the ions are incident at approximately 60° from normal to the (011) plane. The surface geometry protects the metal in the bottom of the trough, while the excess metal on the (011) surface is sputtered away. Additional EBL and liftoff processing may be used to form leads to monitor wire conductance, or to fabricate nearby gates. At the conclusion of the directional dry etching process, the result is a nanowire in a trough.

A different wet etch may be used to remove some of the surrounding $Al_{0.3}Ga_{0.7}As$, allowing SEM characterization of the nanowire; see Fig. 6. With more complicated layered structures, arrays of nanowires may be fabricated in parallel, shown in the lower portion of Fig. 6.

This technique requires specialized substrates, and, like step-edge lithography, is clearly best suited for producing single or arrays of parallel wires. One key difference between this approach and SEL is that here the wire width is defined by the MBE growth process, rather than the collimation of the directional etch. As a result, the wire cross-section tends to be rectangular rather than triangular, with the ultimate limit of accessible wire size set by the morphology of the deposited metal. Using e-beam evaporated Au$_{0.6}$Pd$_{0.4}$ with a 1 nm Ti adhesion layer, wires as small as 5 nm wide and 7.5 nm thick with lengths well over 1 μm have been studied extensively with multiterminal transport measurements. Some continuous two-terminal devices as narrow as 3 nm have been made, though they were extremely fragile. MBE-grown templates combined with either amorphous or epitaxially deposited metals have the potential to create engineered nanowire structures as narrow as a few atoms.

C. Nanoscale etch-masks

Another subtractive approach to templating is to employ nanoscale etch masks. The idea is to coat an entire substrate with a thin metal layer. One deposits (by spinning from solution) some nanowire-shaped templates onto the surface. The substrate is then placed into a dry etcher, either an ion mill or a RIE, and the templates protect nanowire-shaped patches of the surface from the normally-incident beam. Finally, the templates are removed, ideally leaving behind nanowires where the underlying metal film had been protected.

Multiwalled carbon nanotubes have been used as templates for such a process. Beginning with a (111) Si wafer coated with 200 nm of thermal oxide, a 1 nm Ti adhesion layer and a 9 nm Au film were evaporated onto the substrate. A few drops of multiwalled nanotubes suspended in CHCl$_3$ were spin-coated onto the surface, leav-
FIG. 6: Upper image: a 20 nm wide AuPd wire (indicated by arrows) made with the MBE templating process, spanning several EBL-fabricated Au leads. Surface etching of the GaAs/AlGaAs substrate has been performed to aid in imaging. Lower image: an array of parallel nanowires made with the same technique. The largest wires are 50 nm wide, while the narrowest are 7.5 nm wide. Scale bar = 100 nm.

ning behind isolated nanotubes as the solvent evaporated. The substrate was then placed in the path of a 300 V beam of Ar$^+$ ions at normal incidence for 1 minute, long enough to mill away the metal film and ∼1 nm of SiO$_2$ from uncovered portions of the surface. The nanotubes of various diameters act as etch masks, allowing isolated Ti/Au wires as narrow as 12 nm to be produced. The remaining nanotubes could be removed by AFM manipulation, though one suspects that exposure to an oxygen plasma or ozone environment might be more effective at speedily ridding large areas of any carbon residue.

A variation on this approach addresses two difficulties in the above technique: the dispersity of multiwalled nanotube sizes and the difficulty of removing carbon residue. Rather than carbon nanotubes, the templates are chemically modified V$_2$O$_5$ fibers. Unlike fibers produced in pure water, these are hydrolyzed in a dilute solution of N-methylforamide, resulting in transverse fiber dimensions of 6-10 nm × 15-20 nm, with lengths on the micron scale. These authors use a 1 nm Ti / 6 nm AuPd film for enhanced metal uniformity from the small AuPd grain size, and an Ar ion beam (200 V) to provide the directional etch. The V$_2$O$_5$ fibers consistently lead to fairly monodisperse 15 nm-wide nanowires wherever the fibers protect the film from the etch. Residual V$_2$O$_5$ is removed by soaking the substrate in a dilute acid solution.

A more involved example of this approach interposes an additional step. Starting with a CdTe substrate coated with a Bi film (the desired wire material; the unusual substrate facilitates MBE growth of high quality Bi films), a layer of PMMA is spun on and baked. The masking in this case is provided by chemically self-assembled chains of Ag nanocrystals. The chains are ∼40 nm in diameter, with micron-scale lengths. These structures are transferred from solution as a Langmuir-Schaeffer film onto the PMMA-coated substrates that are then flood-exposed with a dose of 50 µC/cm$^2$ of 700 V electrons. This is sufficiently energetic to expose the PMMA but not to penetrate the Ag nanocrystals. The nanocrystals act as a shadow mask for e-beam exposure rather than as a direct etch mask. After the exposed resist is removed by development in MIBK:IPA solution, the substrate is etched with BCl$_3$ in a RIE etcher. The BCl$_3$ attacks the exposed Bi, leaving Bi nanowires behind. Removal of the remaining PMMA and Ag nanocrystals is not discussed.

A final example of this approach uses biopolymeric materials as etch masks. Microtubules with diameters smaller than 40 nm and lengths of tens of microns were used to shadow regions of Ti/Au film on an oxidized Si wafer. Biopolymer templates open up the possibility of using biologically inspired pattern formation mechanisms to engineer complicated mask structures.

A variation on this approach addresses two difficulties in the above technique: the dispersity of multiwalled nanotube sizes and the difficulty of removing carbon residue. Rather than carbon nanotubes, the templates may be fabricated by chemical means, often with high reliability and uniformity on the nm scale. The fidelity with which this uniformity is transferred to the final structures is then limited by the etching technique and the morphology of the initial metal film. A further complication is the positioning of the templates; the methods described here form wires wherever the templates happen to land, rather than in predetermined locations.

D. Suspended nanotubes

One may also consider templating approaches that are additive rather than subtractive. Here a template is used as a mechanical scaffold upon which wire material is deposited. Using suspended carbon nanotubes in this way has allowed the creation of amorphous MoGe nanowires
with widths from a few nm up to \(\sim 20\) nm \[76\].

For this technique to produce nanowires suited for conductance studies, the nanotube must be suspended over the substrate so that it is electrically isolated, except at end points. One method of achieving this configuration \[77\] begins with a Si wafer coated with 1 \(\mu\)m of SiO\(_2\) and a further 60 nm of Si\(_3\)N\(_4\) film. EBL and RIE are used to open a \(\sim 100\) nm wide slit in the nitride with a narrower constriction where the measuring electrodes will be. An HF treatment etches the exposed SiO\(_2\) and undercuts the Si\(_3\)N\(_4\). The result is a trough with two cantilevered Si\(_3\)N\(_4\) protrusions at the location of the original constriction. Through a shadow mask, metal is deposited to coat these protrusions, forming two measuring electrodes spaced very closely, with the HF etch undercut preventing the two electrodes from shorting together. Electrostatic trapping is then used to “capture” a single nanotube from solution to bridge the electrodes.

**E. Electrodeposition into channels**

Electrochemical approaches have also been used very effectively to produce nanowires using additive templating. To constrain the growth of electrochemically deposited metal, a three-dimensional template \(i.e.\) a channel with transverse dimensions close to the desired final wire size \(i.e.\) is most commonly required.

An ideal template would be a long pore, ideally of uniform cross-section, through an electrochemically inert membrane. A recent review of membrane-based templating of nanoscale materials may be found in Ref. \[81\]. One approach \[82\], borrowing from a nuclear physics technique of particle detection, is to create such pores by chemically etching membranes that have been exposed to an energetic ion flux from a radioactive source \[83\]. The MeV-scale ions pass through thin films of mica or polycarbonate, leaving behind a chemically-altered track. Mica tracks are etched by HF, while polycarbonate membranes may be etched by a mixture of NaOH and methyl alcohol. Pore sizes below 100 nm are routine, and diameters below 10 nm have been reported \[84\]. Polycarbonate membranes may also be purchased commercially \(e.g.\) as small as a few nm \[81\], and alumina’s chemical stability allows great diversity in the types of materials that may be deposited \[81\]. Another template alternative is nanochannel glass \[85, 86\], in which pores are reduced.

An alternative membrane material is anodically etched porous alumina. This may be produced electrochemically from a thin aluminum membrane \[81\]: such membranes may purchased commercially, albeit with a limited range of pore sizes, from, \(e.g.\), Whatman Lab. Division. Pore density is determined by the integrated ion dose and may be as high as \(10^9\) cm\(^{-2}\), while diameter uniformity is set by the details of the etch process \[81\].

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produces a 0.5 µm-thick, hexagonally close-packed array of PMMA rods 14 nm in diameter embedded in a PS matrix. Exposure to DUV radiation degrades the PMMA and crosslinks the PS, so that subsequent development in acetic acid leaves behind a dense array of pores in a PS film for use as a template. Pore density and parallelism are similar to that in alumina films, while not requiring strong acids or bases for processing.

Figure 8 illustrates the steps in the templating process. An initial metal layer is deposited by evaporation or sputtering onto one side of the membrane. The membrane is then placed in an appropriate solution and the desired metal is electrochemically deposited, using the initial metallization as a seed. Note that wires with longitudinally varying chemical composition may be grown by changing the deposition solution during the growth process. Precise multilayers are possible and may be combined with chemical functionalization for self-assembly experiments or diagnostic sensing.

Similarly, by depositing alternating layers of ferromagnetic and normal metals, wires that exhibit longitudinal giant magnetoresistance (GMR) have been made. It should also be noted that templates such as these may be filled by methods other than electrodeposition, such as high pressure injection of molten metal into the pores (see references therein).

Following deposition the membrane may be dissolved with an appropriate solvent, allowing access to individual nanowires. Alternately, for sparse arrays made using low-porosity membranes, lithography on the upper membrane surface may allow two-terminal contacting of small numbers of nanowires.

Attractive features of this templating approach include: the ability to make large numbers of wires in parallel; the ability for those wires to be substantially narrower than 100 nm with a small dispersity in wire diameter; and applicability to a large number of material systems, including noble metals, ferromagnetic materials, semimetals, etc. Wire diameter is limited by the template, particularly the longitudinal uniformity of pore size, and the morphology of the electrodeposited material. It is possible to form single crystal nanowires with appropriate materials and conditions; for example, see Refs. 84-97. A complication of this method is that arranging individual wires in precise configurations for study is quite challenging.

F. Other templated deposition

Cleaved heterostructures can be another example of an unconventional template. A heavily doped well layer in an MBE-grown III-V heterostructure on the edge of a cleaved can be used as the active electrode for deposition wafer. While the quantum well itself is defined with atomic precision, as discussed above in Sec. III B, deposition in this approach is not capable of producing wires with comparable definition. The growth of deposited metal is not constrained laterally, so that the resulting nanowires produced from a 4 nm-wide quantum well are granular and have widths ~20 nm.

Chemically synthesized template structures may also be employed as scaffolds for nanowire deposition. Hong et al. synthesize arrays of organic nanotubes from calix[4]hydroxyquinones (CHQs). The pores in these arrays are 0.6 nm × 0.6 nm and are lined with OH groups and π-conjugated faces. The hydrophilic OH groups allow silver ions in aqueous solution to be intercalated into the pores and reduced out of solution, where they aggregate to form 0.4 nm diameter crystalline Ag nanowires up to microns in length. This approach produces large numbers of extremely narrow, straight nanowires without the need for UHV or high temperature processing. Forming metallic contacts to the resulting structures, however, is extremely challenging.

Individual molecules may also be used as templates for chemical metallization. For example, DNA molecules may be functionalized to form connections between lithographically defined Au electrodes. A chemical pro-
procedure exploiting ion exchange is used to seed silver clusters along the DNA. Chemical reduction of additional Ag from solution then leads to the formation of a granular wire spanning the electrodes. While this method can take advantage of existing tools for manipulating DNA, the quality of the resulting wires is not well-controlled at present.

IV. CHEMISTRY AND SELF-ASSEMBLY

Direct chemical synthesis and other self-assembly techniques have also demonstrated nanowire formation. We have already discussed templated chemical synthesis, which relies on a template to confine the reactants and shape the metallic reaction products. Direct chemical synthesis instead takes advantage of some inherent anisotropy in reaction materials or kinetics to produce extended structures. Other forms of self-assembly utilize anisotropic energetics (e.g. strain energy from lattice mismatch) to guide nanowire formation.

A. Chemical approaches

Direct chemical synthesis of nanowires can be difficult to generalize to large numbers of metals because of the need for precise control of anisotropy in growth, and a lack of suitable reaction chemistries. A full explanation of chemical approaches is beyond the scope of this article. Instead we very briefly state some essential features of the methods and provide some references in this rapidly developing field.

Synthesizing elongated structures in either the solution (for example, [104]) or the gas phase [105] often involves clever use of seed or catalytic particles. Particle size can directly influence the diameter of the resulting nanowire. One example of catalytic growth that has been very successfully applied to semiconductor materials (though not yet to metals) is described in Ref. 105. The growth mechanism is called the vapor-liquid-solid (VLS) technique [106, 107]. A catalytic liquid nanocluster is made from a material that can form a liquid alloy with the desired nanowire material. Such a cluster, which defines the diameter of the nanowire, is then placed in an environment supersaturated with reactant, and serves as a nucleation site for crystallization. One-dimensional growth then occurs, with the liquid nanocluster serving as one end of the resulting nanowire.

An alternative method of chemically producing elongated structures from nanoparticles [104] uses surfactants to coat the seed. By using multiple surfactants, the crystallographic direction of growth of crystalline material from solution onto the seed may be controlled. This method has been used to produce single crystal Co nanorods with diameters below 15 nm, though to date their lengths have been limited to ~100 nm.

Other chemical means may be used to encourage growth anisotropy. For example, by reducing silver out of solution onto 4 nm seed particles in the presence of a micellar template [108], microns-long Ag nanowires ~12 nm in diameter may be formed.

Some metals possess crystallographic structures that naturally tend toward anisotropic growth when synthesized from solution. Examples include selenium [109] and alloys of selenium and tellurium [110]. These substances tend to have helical crystal structures that favor 1d growth. Single crystal selenium nanowires 10 nm in diameter microns in length have been produced from solution.

Chemical methods sometimes succeed in producing nanowire structures even when there is no clear mechanism for growth anisotropy. Silver nanowires produced from solution with AgBr seeds [111] and zinc “nanobelts” [112] from ZnS and graphite powder heated in flowing Ar are two examples.

FIG. 9: SEM image of chemically synthesized Zn “nanobelts”. The growth mechanism that produces these anisotropic nanowire structures is not yet known. Figure reproduced with permission from [112], copyright 2001 Royal Society of Chemistry.

Development of chemical methods for nanowire synthesis are in an early stage, and have already produced some spectacular results. As with templating approaches, for study of electrical transport properties, the nanowires produced chemically must then be separated and manipulated onto leads. If suitable reaction pathways and growth mechanisms may be found and utilized for more materials of interest, chemical synthesis may play a major role in future nanowire studies.

B. Self-assembly

Finally, self-assembly techniques may be employed, particularly to form ordered arrays of nanowires from
certain materials on specific substrates. One might imagine that the large configurational entropy associated with placing adsorbate atoms on a substrate would make spontaneous formation of nanowire structures unlikely. Energetic considerations can make organized patterns favorable, however. This section only touches on the richness of this subject, focusing on recent examples explicitly dealing with metal nanowires.

One common means of ensuring linear structures is “step-edge decoration.” Here one considers a substrate that is a vicinal surface, where the surface normal deviates very slightly from a high symmetry crystalline direction. As a result, for clean surfaces (usually annealed at high temperatures in UHV), the substrate has a series of parallel atomic terrace steps that are roughly linear, with the density of steps increasing with the degree of “mis-cut”. Nanowire material is then deposited at submonolayer coverages. With appropriate choices of substrate, nanowire material, and deposition/annealing conditions, deposited metal migrates via surface diffusion until being trapped up against step edges.

Step edge growth has been employed by a number of investigators (for example, Refs. [113, 114, 115, 116]) in recent years. The resulting wires are often difficult to characterize electronically. The wires are usually only one or two atomic layers thick perpendicular to the substrate; further, when metal wires are formed at steps on the surface of another metal, isolating the conducting properties of the wires from the substrate may not be possible.

One interesting variation that evades these difficulties is that of Zach et al. [117]. Using electrochemistry the authors deposit molybdenum oxide at step edges on a cleaved graphite substrate. By exposing the substrate to hydrogen at 500° C for an hour, the oxide is reduced to form metallic Mo wires. The wire adhesion to the graphite is sufficiently poor that the wires may be transferred to the surface of a polymer film cast on top of the graphite substrate.

An alternative approach to nanowire fabrication that has received much recent attention is self-assembly assisted by differential strain between a deposited metal and the underlying substrate lattice. As in the step decoration method, energetic considerations in certain material systems may be sufficient to overwhelm the entropy gain that would result from non-straight wires. Lattice mismatch strain has been employed extensively in epitaxially grown semiconductor structures in recent years (see Ref. [119]).

Simple lattice mismatch is not sufficient to produce wire structures [120, 121]. Isotropic lattice mismatch results in islands rather than nanowire formation. Substantial growth anisotropy requires the wire material to have minimal lattice mismatch along the wire direction and large mismatch along the transverse direction. This self-assembly technique requires epitaxially smooth and clean substrate surfaces, UHV growth conditions, and careful material selection to achieve the required lattice conditions.

Rare earths have been observed to form long metallic silicide nanowires on Si (001) surfaces [118, 120, 122, 123]. A typical growth process begins with a flat Si (001) substrate in UHV. Submonolayer coverages of Er are then evaporated onto the substrate. Erbium forms a thermodynamically stable silicide, ErSi$_2$, with a hexagonal crystal structure. The silicide grows so that the lowest lattice mismatch (-1.3%) occurs along the [1120] direction of the ErSi$_2$ and the (110) direction of the Si. This direction is the long axis of the wires. The transverse direction (0001) for the ErSi$_2$; (100) for the Si) has a much larger (6.5%) lattice mismatch; as a result wire growth in that direction is strongly disfavored. The result after annealing is a large number of metallic nanowires a few nm in width, one or two atomic layers in thickness, and microns in length. See Fig. 10.

As with direct chemical synthesis, self-assembly techniques for producing nanowires are relatively immature, but show signs of great promise for certain classes of materials. The requirements for UHV conditions and extremely careful surface preparation are stringent, however. Research on more robust, fault-tolerant, and engineerable self-assembly mechanisms is sure to be an active field for some time.
V. CONCLUSIONS

Metal nanowires are important both as components of future technologies and as tools for examining fundamental science in metals at the nm scale. It is clear from the above that tremendous progress has been made in the last twenty years on techniques for fabricating such structures. Nanowires with transverse dimensions below 20 nm present a particular challenge.

The techniques presented here have advantages and disadvantages that make them well-suited to certain tasks. Summarizing the main points:

- Nanowires are only as well-defined as the metal material that constitutes them. For physically deposited metals small grain sizes aid in the formation of narrow structures, and the surface physics of the metal-substrate interface is critical in determining wire morphology.

- Lithographic processes possess tremendous flexibility, but tend to be slow. Lateral definition at extremely small scales is very challenging, and true atomic resolution from scanned probe methods requires UHV conditions and special substrate preparation.

- Templating approaches have been very successful. Subtractive methods produce small numbers of extremely narrow wires at very well-defined locations, given engineered (step-edge, MBE-defined) templates.

- Additive templating using porous membranes to constrain electrochemical metal growth produces very large numbers of nanowires. Addressing individual wires or arraying them on a substrate is nontrivial, however. Other structures for templating (chemical scaffolds, nanotubes) are also promising.

- Direct chemical synthesis of metal nanowires is promising in its infancy. Encouraging results exist in a small number of material systems, and much remains to be learned about growth mechanisms and generalizability of techniques.

- Self-assembly is also a nascent approach. Here, too, the restrictions of particular material systems and processing conditions present challenges that need to be more fully investigated.

Nanowires promise to be a fruitful area of physics, materials science, and chemistry research for the foreseeable future. Advances in nanoscale characterization techniques and computational approaches to materials should ensure much continued progress in this exciting arena.

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