Hybrid Memristor-CMOS (MeMOS) based Logic Gates and Adder Circuits

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Abstract—Practical memristor came into picture just few years back and instantly became the topic of interest for researchers and scientists. Memristor is the fourth basic two-terminal passive circuit element apart from well known resistor, capacitor and inductor. Recently, memristor based architectures has been proposed by many researchers. In this paper, we have designed a hybrid Memristor-CMOS (MeMOS) logic based adder circuit that can be used in numerous logic computational architectures. We have also analysed the transient response of logic gates designed using MeMOS logic circuits. MeMOS use CMOS 180 nm process with memristor to compute boolean logic operations. Various parameters including speed, area, delay and power dissipation are computed and compared with standard CMOS 180 nm logic design. The proposed logic shows better area utilisation and excellent results from existing CMOS logic circuits at standard 1.8 V operating voltage.

Index Terms—Memristor-CMOS (MeMOS) Logic, full adder, logic gates, memristor based boolean logic.

I. INTRODUCTION

MEMRISTOR is the well known device now-a-days, that captured the interest of researchers and scientists when HP Labs realized a practical physical device in 2008. It all started back when L. Chua in 1971 on the basis of symmetry forefront, postulated memristor[1](short of memory resistor) as the fourth basic fundamental circuit element. [11–16] Memristor basically connects electric charge q and magnetic flux ϕ as voltage V and current I is connected by resistor, magnetic flux ϕ and current I by inductor and voltage V and charge q is connected by capacitor. The relation charge q and magnetic flux ϕ was missing as per Chua stated. Chua demonstrated that memristors can be characterised by pinched hysteresis loop as shown in Fig. 1. In theory the memristor term was extended to memristive devices in 1976 by S. Kang. Characterisation of memristors require two equations instead of one. [7–12]

In 2008, HP Labs realized memristor that consists of TiO2 thin film sandwiched between two platinum electrodes on both sides. The response of the linear ion drift memristor is shown in Fig. 1 for frequency ω0, 5ω0 and 10ω0. Now, after few years of research, memristors are considered as one of the best alternative to current generation CMOS technology. Memristors are basically the devices with varying resistance that depends on the previous state of the device. Memristors can be voltage or current driven. Memristors can be used for memory implementation, where the logic bits are stored as resistance states. Various applications has been proposed by researchers recently that includes neuromorphic applications and use in analog circuits.

One major area of interest is the logic computation by using memristors. Researchers has proposed different methods of logic computation. One of the primary methodology that is most regarded is the material implication using memristor. Some has proposed integration with CMOS logic to compute various logical operations. Material implication logic shows promising results but need more computational steps in performing logic. The major constrain with material implication is the designing of read/write circuits as the logic is completely different from boolean logic. Moreover, it is not compatible with current generation CMOS technology. [13–15]

Hybrid Memristor-CMOS logic is a hybrid of both memristors and CMOS. Using this implementation scheme, we can compute logic and the outputs can also be represented by voltage levels. We coined the term ‘MeMOS’ that better suits Memristor-CMOS hybrid integration. In this approach, AND and OR logic can be computed using the memristors only and CMOS inverter is used to get NOT operation as the operation NOT is not possible with memristors only.
Many mathematical models of memristor presented by researchers. We have chosen TeAM (Threshold Adaptive Memristor Model) for our study as, the model has current threshold parameters and provides realistic modeling for logic implementation. Although, there are many proposed models for logic computation but in our study we have kept the voltage level at standard 1.8 V and designed logic gates and thus full adder. We have also simulated the response of logic gates and full adder with CMOS only by keeping the same MOS parameters. This study will give a fair enough idea that by using MeMOS logic, we can save much more area than the current CMOS implementation requires. There are different ways to design adder but we have chosen the most basic one for the comparison sake. [16]–[20] Different advantages and issues with this logic is also discussed in next sections.

The paper is organised as follows: Section II describes the modeling of TeAM memristor model. The schematic of AND and OR logic computation models are described in Section III. Section IV describes the logic gates designing and transient response analysis. Full adder circuit is described in Section V and the comparison of parameters like delay, rise and fall time is given in Section VI followed by Section VII which summarise the paper and future work is given in the same section.

II. Memristor Modelling

The memristor was postulated by L. Chua in 1971 based on the symmetry forefront. The operation of memristor depends on the history or the previous state of the device. The memristor is considered as varying resistor with varying resistance as memristance $M$ of device. The memristance $M$ of the memristor depends on the total current passed through the device. When the voltage or current is removed from the source, the memristor retains its state and by applying lower value of voltage or current the previous state can be read easily. [21]–[24] In 1976 L. Chua and S. Kang generalised the concept of memristor to a broader class of nonlinear dynamical systems. [25] They called these systems as the memristive systems, the current-controlled, time-invariant memristor can be described by the equations as [26]

$$ v = \mathcal{R}(w, i) \ i $$
$$ \frac{dw}{dt} = f(w, i) $$

where $w$ is a set of state variables of the device and $f$ and $\mathcal{R}$ are the explicit functions of time. $v$ and $i$ are voltage and current with respect to time respectively.

The most popular and common memristor model is the Linear ion drift model that is based on the memristor characteristics described by HP Labs in 2008. In linear ion drift model, a device of physical width $D$ is considered that has two regions viz. dopes and undoped as shown in Fig. 2. A region of width $w$ has high dopants concentration. $w$ also acts as the state variable of the device. The dopants are oxygen vacancies that are TiO$_{2-x}$ for the case of TiO$_2$ based memristor. The other region of width $D - w$ is generally an oxide region with the dopant with higher conductance than that of oxide region with mobility of ions is described by $\mu_v$. [27], [28] The device is modelled as two series connected resistors. For the assumption that linear ion drift is in uniform field and ions have similar average ion mobility $\mu_v$, the equations (1) and (2) can be represented by [29]

$$ v(t) = \left( R_{ON} \frac{w(t)}{D} + R_{OFF} \left( 1 - \frac{w(t)}{D} \right) \right) \ i(t) $$
$$ \frac{dw}{dt} = \mu_v \frac{R_{ON}}{D} \ i(t) $$

Equations (3) and (4) yields the following equation for state variable $w(t)$ as

$$ w(t) = \mu_v \frac{R_{ON}}{D} q(t) $$

Plugging the values from equation (5) into equation (3), we can compute the memristance of the system, for the condition $R_{ON} \ll R_{OFF}$ that further reduces to the equation

$$ M(q) = R_{OFF} \left( 1 - \frac{\mu_v R_{ON}}{D^2} q(t) \right) $$

where, $M(q)$ is the memristance of the memristive system.

To describe the physical behavior of the device, various memristor models have been proposed. The models proposed are mostly deterministic and mostly do not consider the stochastic switching behavior. The threshold adaptive memristor model as described in (7) demonstrates that the memristors have a current threshold and have an adaptive nonlinearity. For this model, the equation (2) becomes

$$ \frac{dx(t)}{dt} = \begin{cases} k_{off} \left( \frac{i(t)}{i_{off}} - 1 \right)^{\alpha_{off}} \cdot f_{off}(x) & \text{for } 0 < i(t) < i_{off}, \\ 0 & \text{for } i_{on} < i(t) < i_{off}, \\ k_{on} \left( \frac{i(t)}{i_{on}} - 1 \right)^{\alpha_{on}} \cdot f_{on}(x) & \text{for } i(t) < i_{on}, \end{cases} $$

where the current threshold parameters are defined by $i_{on}$ and $i_{off}$, $\alpha_{on}$ and $\alpha_{off}$ parameters define the adaptive nonlinearity of device, $k_{on}$ and $k_{off}$ are the fitting parameters of memristor, and $f_{on}(x)$ and $f_{off}(x)$ are the window functions. The voltage of the memristor model $v$ described in equation (1) can be defined for the threshold adaptive memristor model as per equation (7) as [30]–[32]

$$ v(t) = \left( R_{ON} + \frac{R_{OFF} - R_{OFF}}{x_{off} - x_{on}} (x - x_{on}) \right) \cdot i(t) $$

Fig. 2. Schematic of linear ion drift memristor as proposed by HP Labs.
where $R_{ON}$ and $R_{OFF}$ are the minimum and maximum resistance of the device respectively, and $x_{on}$ and $x_{off}$ are the internal state variable $x$’s minimum and maximum allowed value for the memristor. The current-voltage characteristics simulated using TeAM model is shown in Fig. 3. We have chosen the TeAM model for its explicit current-voltage relationship and memristance deduction and it shows matching memristive system definition as linear ion drift memristor model shows. This model is more generic and provides accuracy comparing practical memristive devices. The important aspect of TeAM model is the existence of threshold because it not only accurately characterises the Simmons tunnelling aspect of TeAM model is the existence of threshold because it not only accurately characterises the Simmons tunnelling aspect of TeAM model for its explicit current-voltage relationship and computational cum storage element as can be used using material implication logic.

The basic boolean logic operations AND and OR can be analysed using memristors. Although, many researchers have reported the material implication logic using memristor but that is not compatible with current generation standard CMOS process. Material implication works on the state variable, the inputs and outputs are the states of memristors instead of the voltages that are required for signal propagation in CMOS process. So to integrate memristor with CMOS and to work with same voltage levels, there is a need of hybrid Memristor-CMOS (MeMOS) logic.

In this logic, the voltages are used as logic state. Memristors can only be used as computational element rather than computational cum storage element as can be used using material implication logic.

As per the current–voltage characteristics of memristor shown in Fig. 1 and 3 the basic idea of using memristors for logic computation is its property of varying resistance with respect to the direction of current flow through the memristor. Fig. 3 shows that the resistance of memristor varies depending on the direction of current flow. By using this, we can create a voltage divider circuit as reported in [6]. Fig. 4 shows the schematic of two input OR and AND gate circuit designed using memristors. We just need to change the polarity of memristors to get the correct logic value.

Based on the given merits of TeAM model, we have chosen this model for logic design integrated with CMOS technology. From the fabrication point of view, memristors are compatible with current generation standard CMOS technologies. The memristors are relatively smaller in size ($\approx 3$ nm) and thus can be fabricated with the similar techniques used for processing the in-between metal cross-layer via. Memristors are basically thin oxide sandwiched in metal layers, whereas the oxide shows memristive effect between electrodes. Memristors offer higher density of logic elements per unit area and hence can be used to design much more logic functions on same chip area.

III. Logic Using Memristors

From the modeling of memristor, it is clear that the memristors exhibit varying resistance when current flows into the device or out of the device. The change in resistance $\Delta R$ with respect to the direction of current flow $i(t)$ is shown in Fig. 3. The thick black line in memristor symbol represents the polarity of the device.
Fig. 5 describes the computation of AND operation for all input cases of a two input AND gate using memristors only. For case A=1 and B=1, both the inputs are tied to VCC i.e., at logic 1. As described in Fig. 5(a), no current flow through the circuit and the output in this case is logic = VCC or 1. For the case of A=0 and B=0 as shown in Fig. 5(c) it can be considered that the inputs are at logic 0, the output should also be logic 0. Again there is no current flow through the circuit, the same logic appears at output node Y. These two cases are same for OR logic also. Even with the reverse polarity of memristors, the output remains same.

For the case when any of input is at logic 1 and other at logic 0 as shown in Fig. 5(b). In this case, input A=1 and B=0 the current flows through VCC to GND. When current passes from memristor MR0, the resistance of that memristor increases to R_OFF, the resistance of memristor MR1 decreases to R_ON and current leave through GND node. Resistance of memristors are R_OFF ≫ R_ON. By this way, we get two resistors R_OFF and R_ON with different values. Thus as per the voltage divider rule, we get output Y=0 that completes the logic for AND gate as per truth table shown in Fig. 5(d).

The calculation of output voltage at Y for the voltage divider circuit can be determined as

\[ Y = V_{CC} \times \frac{R_{ON}}{R_{ON} + R_{OFF}} \]  

(15)

\( R_{OFF} \) is significantly higher than \( R_{ON} \) we can simplify the equation as

\[ Y = V_{CC} \times \frac{R_{ON}}{R_{OFF}} \ll V_{CC} \approx GND \]  

(16)

When the polarity of the memristors MR0 and MR1 is reversed, the circuit behaves as OR gate. For inputs A=0, B=0 and A=1, B=1 the output Y get the value 0 and 1 as no current flow through the circuit and the behavior remains same as in the case of AND gate. Fig. 5(d) shows the case when any one of the input is at logic 1 and other at logic 0. Current flows through the VCC towards memristor MR0. As the memristor is in reverse polarity arrangement, the resistance of the memristor decreases to R_ON and thus the voltage shows up at output node Y=V_{CC}. The output becomes logic 1 when any of the input is at logic 1. The resistance of other memristor MR1 increases to R_ON and the condition remains same \( R_{OFF} \approx R_{ON} \) because these are the fixed values. The output can be determined for OR gate using the voltage divider rule as

\[ Y = V_{CC} \times \frac{R_{OFF}}{R_{ON} + R_{OFF}} \approx V_{CC} \]  

(17)

AND and OR gates can be implemented using memristors only. By this topology, even ‘n’ input gates can be implemented using memristors. But the primary issue is incomplete logic family. Without NOT operation, it is not possible to implement boolean functions. CMOS inverter can be used to implement NOT operation. The CMOS inverter is designed using 180 nm process technology. The operating voltage for the CMOS inverter is 1.8 V. We kept the same parameter of memristors as used to simulate the current–voltage characteristics shown in Fig. 3. There is an advantage of using hybrid MeMOS logic in terms of level restoration. As per the voltage divider, the output of the memristor based gate depends on the value of R_OFF and R_ON. Even if there is a large difference in these two values then also the output degrades a little bit as in the denominator term of equation (15) and (17), R_ON is added with R_OFF. In the case of different inputs, we get 0.996 V_{CC} at output. Hence, while cascading memristor stages, the output level decreases. PMOS is always tied to V_{DD}, so when signal pass through inverter, the logic level is retrieved. But in certain cases, we need BUFFER to restore the logic level.

Static power dissipation, delay and large area consumption are some of the primary trade-offs of integrating CMOS with memristors. Memristor layer can be fabricated on top of CMOS layer.
IV. LOGIC GATES DESIGNING USING MeMOS LOGIC

As described in previous section, NOT operation is not possible with memristors. So, to get the complete logic family we should add CMOS inverter at the output of AND gate to get NAND operation and similarly NOR operation can also be implemented. The operating voltage is kept at same level of 1.8 V for all the designed gates. The schematic of NAND or NOR gate (reversed memristor in this case) is shown in Fig. 6. Similarly XOR gate can be designed using these approaches as shown in Fig. 7.

The transient response of designed XOR gate is shown in Fig. 8. The delay \( d \), rise time \( t_r \) and fall time \( t_f \) is kept at 1.0 ps. Pulse signal with width of 1.0 ns is given at input. Cadence Virtuoso is used for designing the schematics and Spectre simulator is used to plot the transient response. The output shown for different gates is logically correct except XOR or XNOR gate.

Designing of XOR or XNOR gate leads to logic degradation as shown in Fig. 8. The reason of degradation is explained in the previous section, it is because of the voltage divider circuit. As designing an XOR or XNOR gate needs cascaded stages as shown in the schematic of XOR gate in Fig. 7 in this case a BUFFER can be used to restore the level of output voltages. The output of XOR or XNOR gate with BUFFER at output is shown in Fig. 8. The level after adding BUFFER is restored at \( V_{CC} \approx 1.8 \) V. Although, even in CMOS process, cascading stages need BUFFER for level restoration but with extra area overhead.

By using MeMOS logic gates, any digital logic circuit can be implemented. We have evaluated the transient response of these gates with the CMOS logic and found that the gates designed with MeMOS logic shows improved performance.

A. Adder Circuits

Using the gates designed using MeMOS logic, we can further extend the circuits towards the basic building block of any computation i.e., adder logic. Adders are used in different configurations to perform addition, subtraction, multiplication or division of bits. In this section, we have reported half adder, full adder and 8-bit adder circuit. Fig 9 shows that by adding such a buffer, the output can be levelled to 1.8 V. The output of NAND is taken by using a NOT gate in front of AND gate.

![Fig. 6. Schematic of NAND gate using Hybrid Memristor-CMOS logic. The memristors are in the configuration to provide AND operation and CMOS NOT gate is used at the output to get NAND operation.](image)

![Fig. 7. Transient response of XOR gate till 4 nm using Hybrid Memristor-CMOS logic shows degraded output due to the cascading of stages in XOR implementation. The logic can be levelled by using a buffer.](image)

![Fig. 8. Transient response of XOR gate. The output of XOR gate is levelled using a buffer showing correct logic output. The output of NAND is taken by using a NOT gate in front of AND gate.](image)

![Fig. 9. Half Adder circuit implementation using Hybrid Memristor-CMOS logic. The circuit consumes same areas as of one XOR gate with the inclusion of just two additional memristors.](image)
just two memristors in the circuit of XOR gate, half adder can be implemented.

In Fig. 7, memristor MR0 and MR1 completes an AND gate operation that is same with the memristor MR4 and MR5, while memristor MR2 and MR3 fulfils an OR gate. Thus connecting it in a standard fashion that leads to XOR gate implementation. From the XOR gate, we can add one more AND gate at the end of XOR gate to form half adder as shown in Fig. 9. In this the memristor MR0 and MR7 forms AND gate after the XOR gate to complete the half adder operation. Similarly, A one bit full adder circuit using MemMOS logic is shown in Fig. 10 that is designed using two similar half adders and memristors MR0 and MR11 act as OR gate in the circuit to fulfil the CARRY operation. The transient response of the adder circuit is shown in Fig. 11.

B. Advantages over Implication Logic

Material implication recently get hype when using memristor based IMPLY can perform all logic tasks. [23], [24]. Although, circuits designed using IMPLY gate shows significance advantages like high speed operation, smaller area overhead and lower power consumption but except just the circuits, IMPLY operation works on internal state resistance of memristors. External read/write circuitry is required to implement IMPLY based logic to current generation CMOS logic a circuit is required to convert memristor’s state into voltage levels for further computation. The read/write circuitry consumes much more area because of complete CMOS implementation and then due to extra circuitry, it leads to overall performance degradation of the circuit due to bottlenecks of CMOS technology.

MemMOS logic uses hybrid of both the technologies. The major advantage of using MemMOS logic is to integrate the circuits with different circuits designed by CMOS logic only. Then the input/output signals work on same voltage level that is acceptable by CMOS logic, hence the need of extra circuitry diminishes. Although, it consumes more area than IMPLY logic based circuits but considering external read/write circuitry in IMPLY logic, MemMOS logic still has advantages over CMOS logic and close to IMPLY logic. For Full adder circuit, two half adders are cascaded to get the desired full adder circuit. The performance is analysed for the given circuit.

The critical path can examine all the transitions. In Fig. 9 the circuit is designed that is almost identical to XOR gate. The circuit area is totally similar to XOR gate designed using hybrid memristor-CMOS logic as shown in Fig. 7, but the circuit act like as half-adder. Thus with full adder circuit implementation, by using just 8 MOSFETs the adder circuit works as desired. The degradation problem can be solved by adding BUFFER at the output.

V. Performance Analysis

Transient response of MemMOS based adders are computed and various parameters like rise time, fall time, delay are analysed and compared with current generation CMOS technology. Table I shows the performance analysis of various logic gates using MemMOS logic and Table II shows the performance analysis of gates using CMOS logic.

The performance is analysed for full adder circuit as shown in Fig. 11. Transient analysis is simulated for all the possible combinations of the circuit. The Top three waveform shows signal A, B and Cin and the result is plotted or Sum and Carry Signal as shown in Fig. 11.

The major problem with the linear ion drift model is the non-stabilized output parameters. That is the level degradation
The level degradation can be approximated due to the voltage divider circuit and thus the TEAM model is preferred to raise the output level of the signal.

In full adder transient analysis there are very slight glitches that are due to CMOS technology used. Memristors alone provides near ideal transient response for the circuit.

Delay and Rise time/fall time of the circuits are extracted for the given transient response is $T_r = 43.71$ ps, $T_f = 22.43$ ps. The delay calculated is 98 ps for half adder circuit.

The four bit adder is designed using 4 one bit full adders and then two four bit adders are cascaded to implement the 8 bit adder. The performance parameters for 8 bit Full adder are extracted as $T_r = 114.2$ ps, $T_f = 78.7$ ps, Delay = 371.3 ps for worst case and normalised power = $52.7 \mu W$.

For Hybrid Memristor-CMOS logic, the layout for the circuits designed completely with CMOS logic and for the possible implementation of Hybrid Memristor-CMOS logic.

Fig. 12 shows the implementation using CMOS 180 nm process technology. For the sake of comparison, the AND gate required 6 MOSFETs but in the case of hybrid memristor-CMOS logic, there is no any MOSFET required. Hence, even for n-input AND or OR gate, there is much saving in area as memristors can be implemented over the top of MOSFETs and through interconnects the gates can be connected together.

The layout of CMOS full adder is shown in Fig. 12. In the Fig. 12(a), the full adder circuit is shown. In Fig. 12(b), the reduced number of MOSFETs are only required for the implementation of full adder circuit. Fig. 12(c) shows the possible layout of hybrid memristor-CMOS logic circuit with memristor layer on top of CMOS layer.

Memristors are connected on the poly-silicon layer on top of MOSFET's gate. The connection with the gate can be done with the help of vias. Two memristors are required for the computation of AND and OR function, that is shown in Fig. 12(c), lot of complex functions can be implemented that take the area similar to one MOSFET. Hence, it can further help in the reduction of area and implement more logic functions per unit area of chip.

Hybrid Memristor-CMOS logic based gates and adder architectures are designed using Cadence Virtuoso and the performance parameters are analysed. The results are acquired for...
all logic gates, half adder, full adder and 8-bit full adder. The comparison is done with current generation CMOS technology. The parameters of MOSFETs, Memristors and supply voltages are kept constant for fair comparison in between these two logic families. The advantages and disadvantages of these logic families are discussed in previous sections. The IMPLY logic family is not included in analysis due to the highest number of computational steps required for any boolean functions.

The extracted performance parameters of various gates and adder circuits are given in Table I for Hybrid memristor-CMOS logic and for CMOS logic the parameters are given in Table II. The required number of transistors in both logic families are given in Table III and IV for hybrid memristor-CMOS logic and for CMOS logic respectively. The parameter comparison of adder circuits with CMOS logic is shown in Table V.

### A. Comparison between logic families

1) Speed: In general, the total calculation time for any logic computation is Hybrid memristor-CMOS logic < CMOS logic. From the parameters like rise time, fall time and delay, hybrid memristor-CMOS logic seems prominent than CMOS logic. NOT gate is used for NOT function in both the logic families, the maximum speed limit in hybrid memristor-CMOS logic is due to NOT gate.

#### TABLE I

| Logic Component | Rise Time (Tr) | Fall Time (Tf) | Delay (d) | Power (Dyn+Stat) |
|-----------------|----------------|----------------|-----------|------------------|
| NOT             | 23.3 ps        | 14.1 ps        | 18.70 ps  | 0.5 µw           |
| AND             | 02.2 ps        | 00.8 ps        | 1.50 ps   | 1.50 µw          |
| OR              | 02.1 ps        | 00.8 ps        | 1.45 ps   | 1.51 µw          |
| NAND            | 23.4 ps        | 19.1 ps        | 21.25 ps  | 1.82 µw          |
| NOR             | 28.1 ps        | 14.2 ps        | 21.15 ps  | 1.83 µw          |
| XOR             | 40.4 ps        | 20.8 ps        | 30.60 ps  | 2.08 µw          |
| XNOR            | 40.1 ps        | 22.1 ps        | 31.11 ps  | 2.41 µw          |
| Half Adder      | 43.7 ps        | 22.4 ps        | 98.05 ps  | 8.07 µw          |
| Full Adder      | 82.1 ps        | 34.1 ps        | 212.3 ps  | 17.87 µw         |
| 8-bit FA        | 114.2 ps       | 78.7 ps        | 371.3 ps  | 52.71 µw         |

#### TABLE II

| Logic Component | Rise Time (Tr) | Fall Time (Tf) | Delay (d) | Power (Norm. Power) |
|-----------------|----------------|----------------|-----------|---------------------|
| NOT             | 23.3 ps        | 14.1 ps        | 18.70 ps  | 5.41 µw             |
| AND             | 35.0 ps        | 18.7 ps        | 26.85 ps  | 19.28 µw            |
| OR              | 29.4 ps        | 27.6 ps        | 58.21 ps  | 19.63 µw            |
| NAND            | 47.8 ps        | 20.9 ps        | 34.35 ps  | 10.69 µw            |
| NOR             | 50.7 ps        | 17.2 ps        | 33.90 ps  | 10.88 µw            |
| XOR             | 83.9 ps        | 48.3 ps        | 66.02 ps  | 47.81 µw            |
| XNOR            | 78.8 ps        | 50.4 ps        | 64.61 ps  | 43.61 µw            |
| Half Adder      | 85.2 ps        | 47.8 ps        | 126.2 ps  | 58.32 µw            |
| Full Adder      | 96.4 ps        | 54.2 ps        | 342.7 ps  | 17.87 µw            |
| 8-bit FA        | 183.1 ps       | 106.5 ps       | 586.2 ps  | 0.98 m              |

#### B. Area Utilisation

For the assumption that memristors are smaller than MOSFETs, thus the area utilisation is hybrid memristor-CMOS logic < CMOS logic. This new logic ushers in the area saving because the memristors considered for analysis is of width = 3 nm which is way smaller than width = 180 nm of a MOSFET. Memristors can possibly be implemented on the polysilicon layer of a MOSFET, thus a single MOSFET can be a house for many memristors. Many complex functions can be implemented under the area of a single MOSFET whereas in CMOS logic much more transistors are required for the computation of similar function. The layout of full adder is demonstrated to compare the number of MOSFETs required for both logic families. There is a reduction of around 47% in area if Hybrid Memristor-CMOS logic is used.

#### C. Controller Complexity

The only logic family that required an external read/write controller is the IMPLY logic family. Because, IMPLY logic family requires internal states for read/write operation, there is a need to convert this internal states viz. resistances into its equivalent logic states to implement with CMOS. Hence, controllers are required that takes a lot of area and can further reduce the speed of IMPLY logic.

For Hybrid memristor-CMOS logic and CMOS logic there is no any extra read/write circuit is required. The primary purpose of this hybrid memristor-CMOS logic is to build a new logic family that can be integrated with current generation of CMOS technology.

#### D. Power Dissipation

Generally, current generation CMOS process consumes more power due to the constant connection of supply voltage

#### TABLE III

| Device | Hybrid Memristor-CMOS Logic | CMOS Logic |
|--------|-----------------------------|------------|
| MOSFETs| 2 0 0 2 2 4 4 4 | 0 2 0 2 6 6 1 1 |
| Memristors | 0 2 2 2 2 6 6 0 | 1 1 1 1 1 1 1 1 |

#### TABLE IV

| Device | Half Adder | Full Adder | 8-bit Adder |
|--------|------------|------------|-------------|
| Hybrid Memristor-CMOS Logic | | | |
| MOSFETs | 8 16 | 128 | |
| Memristors | 8 18 | 144 | |
| CMOS to Memristor Layer Transitions | | | |
| VIAs | 5 10 | 80 | |
| CMOS Logic | | | |
| MOSFETs | 14 34 | 272 | |
that induce static leakage. However, in hybrid memristor-CMOS logic, static leakage is there. The case is not same with IMPLY logic, however, controllers will be having MOSFETs that means if seen from a broader viewpoint, complete architecture including read/write circuits, there is a static power dissipation.[7]

Static power dissipation can be further reduced by well known techniques like clock gating or multi threshold CMOS. Static power dissipation is not a major concern for the average power, the maximum power dissipation is the dynamic power, that is due to the transitions. Power is computed for signal that have maximum transitions. The power is normalised for memristors because the computation of power is not the same as of CMOS[43]. [44].

E. Versatility

Till now CMOS logic is the most versatile logic, as it offer many different ways to design the circuit or architecture according to the needs of complete system. But as with the Hybrid memristor-CMOS logic, the versatility increases, because the memristor layer on top of CMOS layer, adds advantage to compute some of the functions of a separate layer and the results can be taken directly from that layer.

In the previous section, the full adder is designed in the same way, the SUM is computed with the help of CMOS and memristor layer, through VIAs the signal gets exchanged but the CARRY is computed entirely on memristor layer, because the AND and OR gates are required for CARRY can be implemented in memristors only.

F. Further Improvements

In Hybrid memristor-CMOS logic, the speed is mostly dependent on the working voltages provided that are mostly determined by the threshold voltages. Hence, memristors with higher current threshold value are faster but consumes more power.

In terms of the area utilisation, if the speed is a primary concern, current threshold should be high, thus there is a requirement of more BUFFERs that affects the area requirement of hybrid memristor-CMOS logic.

Power is usually dominated by the applied voltages, that can be chosen as per the current threshold. One method to reduce power dissipation is to add more BUFFERs with CMOS logic gates, BUFFERs can reduce static power dissipation as well as dynamic power dissipation as BUFFERs eliminated the glitches. But the compromise in terms of area is there. Static power can be completely eliminated by adding BUFFERs after each successive hybrid memristor-CMOS logic state.

### VI. Conclusion

In this work, we have studied the models of memristors and its application in logic circuits. We used TeAM model to implement Hybrid Memristor-CMOS (MeMOS) based logic architectures. The degradation factor using linear ion drift model is also considered and thus by using TeAM model. Logic gates are designed with CMOS 180 nm process technology. Adder circuits are designed and the performance is analysed and compared with current generation CMOS 180 nm technology. Area utilisation using IMPLY logic and proposed logic is also compared. Possible layout configuration of MeMOS logic is also described. This paper opens the possibility of newly developed memristor for logic circuits. Based on the excellent performance of adder circuits, this work can be extended further on complex logic architectures like multipliers and many more.

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