DESCNet: Developing Efficient Scratchpad Memories for Capsule Network Hardware

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Abstract—Deep Neural Networks (DNNs) have been established as the state-of-the-art method for advanced machine learning applications. Recently proposed by the Google Brain’s team, the Capsule Networks (CapsNets) have improved the generalization ability, as compared to DNNs, due to their multi-dimensional capsules and preserving the spatial relationship between different objects. However, they pose significantly high computational and memory requirements, making their energy-efficient inference a challenging task. This paper provides, for the first time, an in-depth analysis to highlight the design- and run-time challenges for the (on-chip scratchpad) memories deployed in hardware accelerators executing fast CapsNets inference. To enable an efficient design, we propose an application-specific memory architecture, called DESCNet, which minimizes the off-chip memory accesses, while efficiently feeding the data to the hardware accelerator executing CapsNets inference. We analyze the corresponding on-chip memory requirement, and leverage it to propose a methodology for exploring different scratchpad memory designs and their energy/area trade-offs. Afterwards, an application-specific power-gating technique for the on-chip scratchpad memory is employed to further reduce its energy consumption, depending upon the mapped dataflow of the CapsNet and the utilization across different operations of its processing.

We integrated our DESCNet memory design, as well as another state-of-the-art memory design \cite{1} for comparison studies, with an open-source DNN accelerator executing Google’s CapsNet model \cite{2} for the MNIST dataset. We also enhanced the design to execute the recent deep CapsNet model \cite{3} for the CIFAR10 dataset. Note: we use the same benchmarks and test conditions for which these CapsNets have been proposed and evaluated by their respective teams. The complete hardware is synthesized for a 32nm CMOS technology using the ASIC-design flow with Synopsys tools and CACTI-P, and detailed area, performance and power/energy estimation is performed using different configurations. Our results for a selected Pareto-optimal solution demonstrate no performance loss and an energy reduction of 79% for the complete accelerator, including computational units and memories, when compared to the state-of-the-art design.

Index Terms—Machine Learning, Capsule Networks, Memory Design, Memory Management, Special-Purpose Hardware, Scratchpad Memory, Energy Efficiency, Performance, Power Gating, Design Space Exploration.

I. INTRODUCTION

Deep Neural Networks (DNNs) have shown state-of-the-art accuracy results for various machine learning (ML)-based applications, e.g., image and video processing, automotive, medicine, and finance. Recently, Sabour and Hinton et al. from Google Brain \cite{2} investigated the Capsule Networks (CapsNets), an enhanced type of DNNs which has multi-dimensional capsules instead of uni-dimensional neurons (as used in traditional DNNs). The ability to encapsulate hierarchical information of different features (position, orientation, scaling) in a single capsule allows to achieve high accuracy in computer vision applications (e.g., MNIST \cite{4} and Fashion-MNIST \cite{5} datasets, as shown by the Google’s team \cite{2}). Recently, Rajasegaran et al. \cite{3} proposed a deeper version of the CapsNets (DeepCaps) that performs well on the image classification task, such as the CIFAR10 dataset \cite{6}. To reduce the energy consumption and latency, many researchers have designed specialized inference accelerators for both DNNs \cite{7,8,9,10,11,12,13} and CapsNets \cite{1}, which are typically based on 2D-arrays of multiply-accumulate (MAC) units. The work in \cite{1} mainly focused on the design of a compute-array along with the optimizations for the dynamic routing algorithm. However, the state-of-the-art have not yet investigated the memory architecture design and management for the CapsNet accelerators, which is a crucial component when considering energy reductions of the overall hardware design. Furthermore, memory optimizations for the traditional DNN accelerators do not work efficiently as they do not account for the distinct processing flow and compute patterns of the CapsNets algorithms. This necessitates investigations for specialized memory architectures for the DNN-accelerators executing CapsNets algorithms, while exploiting their unique processing characteristics and memory access patterns to enable high energy efficiency\textsuperscript{1} as targeted in this paper.

Target Research Problem and Motivational Analysis: Our detailed experimental analysis in Section \textsuperscript{IV} illustrates that the energy consumption for both the on-chip and off-chip memories contributes to 96% of the total energy consumption of the CapsNet hardware architecture. Therefore, it is crucial to investigate the energy-efficient design and management of an on-chip memory hierarchy for CapsNets hardware architectures. The key to achieve high energy efficiency is to exploit the application-specific properties of the CapsNet algorithms, that is, the processing behavior of their unique computational blocks, mapped dataflow, and the corresponding memory access patterns. Note, the operations and memory access patterns of the CapsNet inference are distinct from those of the traditional DNNs, as we discuss in Section \textsuperscript{IV}. Therefore, the existing memory architectures for the DNN accelerators may not be efficient when executing CapsNets inference. Hence, to understand the corresponding design challenges and the optimization potential, we perform a detailed analysis of the memory requirements in terms of size, bandwidth and number of accesses for every stage of the CapsNet inference when mapping it to a dedicated CapsNet accelerator (called CapsAcc) \cite{1} and to a traditional DNN accelerator like TPU \cite{11}.

Fig. \textsuperscript{I} shows the on-chip memory utilization in the two

\textsuperscript{1}Note: assuming a huge on-chip memory is typically not applicable in resource-constrained embedded applications, e.g., deployed in the IoT-Edge devices. Therefore, a memory hierarchy system with on-chip and off-chip memories is preferred in this scenario.

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accelerator architectures. The dashed lines represent their respective maximum values. Note, unique operations (like ClassCaps, Sum, Squash, Update and Softmax) of the Google’s CapsNet [2] inference mapped onto the CapsAcc accelerator of [1] exhibit different memory utilization profile compared to when mapped to a memory architecture designed for the traditional DNNs like TPU [11]. This analysis unleashes the available design and optimization potential for improving the memory energy efficiency when considering a specialized memory architecture for a given CapsNets accelerator.

Our Novel Contributions: Fig. 2 provides an overview of our DESCNet memory architecture design methodology, showing the integration of our novel contributions (blue boxes) with a CapsNet accelerator. In a nutshell, we propose:

1) Memory Analysis of CapsNet Inference (Section IV) to systematically study the design requirements (size, accesses, etc.), performance and energy consumption, for different operations of the CapsNet [2] and DeepCaps [3] inference.

2) DESCNet: A Specialized Multi-Banked Scratchpad Memory Architecture for CapsNet Accelerators (Section V-A), which is designed considering the dataflow mapping and the corresponding memory access patterns of different steps of the CapsNet inference. The SPM is partitioned into multiple sectors to support fine-grained sector-level power-gating, thereby providing a higher potential for energy savings under run-time varying memory usage scenarios. Since our SPM supports standard input/output interfaces, it can be coupled with any DNN accelerator that can execute CapsNet inference.

3) Design Space Exploration (DSE) (Section V-C), which is performed to automatically obtain the Pareto-optimal values of different key parameters of our DESCNet memory architecture. It leverages trade-offs between memory, area and energy consumption, while exploiting the distinct processing behavior of different steps of the CapsNet inference.

4) Application-Driven Memory Power Management (Section V-B): it leverages the processing flow of the CapsNet inference, the architectural parameters of the accelerator, and the interfacing with memory, to devise a sector-level power-gating for reducing the static power.

5) Hardware Implementation and Evaluation (Section VI) of the complete CapsNet architecture with an integrated DESCNet memory in a 32nm CMOS technology using the ASIC-design flow with Synopsys tools and CACTI-P [17]. We perform area and energy evaluations for 15,233 possible configurations of the on-chip memory architectures for the CapsNet and 215,693 for the DeepCaps, and benchmark them against the state-of-the-art memory design of [1].

Before proceeding to the technical sections, we present an overview of the CapsNets algorithm and hardware accelerator in Section II to a level of detail necessary to understand the contributions of this paper. Afterwards, Section III will discuss the required architectural modification towards more practical embedded inference systems, and raise the key research questions to enable efficient memory design and management, that will be addressed by the proposed contributions.

II. OVERVIEW OF CAPSNETS: ALGORITHM AND HARDWARE ACCELERATOR

In [13], Hinton et al. showed the potential of CapsNets, which exploit the novel concepts of the so-called multi-dimensional
capsules and the dynamic routing algorithm \(^2\) to achieve high accuracy compared to traditional DNNs \([19][20]\). However, CapsNets are also significantly more complex compared to the traditional DNNs due to their new operations and processing flow, and thereby require new hardware specializations to realize energy-efficient embedded implementations, as showcased in \([11]\). More details on the applicability of CapsNets are discussed in Section II.C.

A. CapsNets vs. DNNs: Differences w.r.t. the Inference

As compared to traditional DNNs, a CapsNet has:

- **Capsule**: a multi-dimensional neuron, which is able to encapsulate hierarchical information of multiple features (like position, scale, and orientation).

- **Squash Activation Function**: a multi-dimensional non-linear function, which efficiently fits to the prediction vector.

- **Dynamic routing**: an algorithm to learn the connection between two subsequent Capsule layers at run-time during the inference. It is an iterative algorithm, i.e., it loops over a defined number of routing iterations.

The last point is challenging from the hardware design perspective, because, unlike in traditional feed-forward DNN inference, CapsNet inference employs a feedback loop in the ClassCaps layer, as highlighted by the red arrows in Fig. 3. Hence, it is more difficult to parallelize and pipeline these computations in the hardware. A detailed view of the operations performed in the ClassCaps layer, with a focus on the dynamic routing, is depicted in Fig. 4.

![Fig. 3: Architecture of the CapsNet for Inference](image)

Recently, an advanced deep CapsNet model, DeepCaps \([3]\), has been proposed (see Fig. 5). It introduces skip connections, as well as 2-dimensional (2D) and 3D convolutional layers of capsules (ConvCaps). After the first convolutional layer with ReLU activation function, the network features 15 ConvCaps2D layers, with squash activation function. Every three sequential ConvCaps layers have an additional ConvCaps2D layer that operates in parallel. The last parallel ConvCaps layer is 3D and performs the dynamic routing. The output layer of the DeepCaps architecture is a fully-connected capsule layer (ClassCaps) with dynamic routing.

B. The CapsNet Accelerator Architecture under Consideration

Fig. 6a shows the architecture of a state-of-the-art hardware accelerator for CapsNet inference called CapsAcc \([1]\). Although our memory designs support standard input/output interfaces such that they can be integrated with any DNN accelerator that can execute CapsNets, we adopt the CapsAcc in our evaluation studies because it is the only open-source DNN hardware accelerator executing CapsNets. The CapsAcc consists of specialized hardware modules like for the Squash function, a 2D MAC-based neural processing (NP) array \((16 \times 16 \text{ Processing Elements})\) for efficiently parallelizing the capsule computations, and a specialized dataflow policy for CapsNets. The dedicated connections between the accelerator and the memories allow data and weight reuse, properties which are particularly effective for the dynamic routing computation. However, the work of \([1]\) employs a relatively large on-chip memory to simultaneously store all the memory elements on chip, which can immediately become an impractical solution due to its lack of scalability to large-sized CapsNets and non-applicability in resource-constrained embedded systems.

C. Applicability of Capsule Networks

CapsNets represent emerging deep learning algorithms for a wide variety of applications. Initially proposed by the Google Brain’s team \([2][19]\) for image classification, several architectural variants of Capsule Networks have been proposed \([3][21][22][23][24]\), as well as CapsNets for other applications, such as action detection \([25]\), object segmentation \([26]\), and machine translation \([27]\). Moreover, Saqur et al. \([28]\) proposed to use CapsNets as the discriminator for the Generative Adversarial Networks, while Qin et al. \([29]\) proposed to employ CapsNets for detecting adversarial images.

Overall, the key differences between traditional neurons and capsules are summarized in Fig. 6. While traditional neurons directly multiply and accumulate the scalar input values, the capsules first apply a transformation matrix to the input vectors and then multiply and accumulate the obtained vectors. Moreover, the squash operation replaces traditional activation functions. The dynamic routing algorithm, already shown in Fig. 4, iteratively learns the coupling coefficients, in such a way that the higher level entities can be detected, rather than the simple features detected by traditional neurons.

![Fig. 5: The DeepCaps architecture of](image)

\(^3\)MAC-based NP array architectures have also been proposed for other DNN accelerators like \([9]\) and \([11]\), but they differ from the CapsAcc \([1]\) in terms of their dataflow, inter-layer transfer of prediction vectors due to the dynamic routing algorithm, and other connecting hardware modules.

\(^4\)An implementation with 8MiB on-chip memory is shown with a 16x16 NP array.
From the hardware perspective, Marchisio et al. [11] proposed a CMOS-based hardware architecture for accelerating CapsNets, while Zhang et al. [30] designed a Processing-In-Memory architecture for CapsNets. Moreover, the works in [31] and [32] show that CapsNets offer huge potential of energy-efficiency improvements when specialized optimizations such as approximate computing and quantization are applied. However, the key takeaway message from the works in [11] and [30] is that the dynamic routing operations constitute the bottleneck for CapsNet inference, as demonstrated by the analysis of the performance breakdown of the Google’s CapsNet executed on the Nvidia Ge-Force GTX 1070 GPU, shown in Fig. 7.

![Fig. 7: Parameter count vs. execution time of the Google’s CapsNet on the Nvidia Ge-Force GTX 1070 GPU.](image)

III. REQUIRED ARCHITECTURAL MODIFICATION AND KEY RESEARCH QUESTIONS

To overcome the limitation of the base-architecture of [11] and towards real-world embedded implementations, we employ a modified architectural model of CapsNet hardware with a memory hierarchy consisting of an on-chip SPM and an off-chip DRAM, as shown in the blue-colored boxes and green-colored boxes of Fig. 8b respectively.

![Fig. 8: Architecture view of the CapsNet inference accelerator. (a) Baseline architecture of [11] (b) Modified architecture for this work with off-chip and on-chip memory partitioning, which is more practical for embedded implementations.](image)

Such a solution can generalize the problem for different applications and more complex CapsNet architectures. However, given such a memory hierarchy, the challenge then lies in designing and managing the on-chip memory such that (i) the off-chip memory accesses are minimized, (ii) the reuse of weights and intermediate data stored in the on-chip memory is exploited at the maximal, and (iii) the unnecessary parts of the on-chip memory can be power-gated under scenarios of varying memory accesses without affecting the performance of CapsNets processing. These problems have not yet been studied for the CapsNets hardware. Towards this, we aim at investigating the following key questions when determining the memory sizes and the communication between off-chip and on-chip memories.

1) How to minimize the off-chip memory accesses to reduce the access energy? Every data is read from / written to the off-chip memory only once, while it is used once or multiple times in the on-chip memory.
2) How to keep the latency and throughput similar/close to the case of having all the memory on-chip, i.e., hiding the off-chip latency as much as possible?
3) How to minimize the on-chip SPM size to reduce the leakage, while it becomes a contradicting design requirement w.r.t. the above-discussed questions 1) and 2)? Hence, what would be the appropriate design trade-offs?
4) How can we design efficient power-gating for the on-chip SPM to save the leakage power for the unused sectors?
5) Can we exploit the unique processing and data reuse behavior of CapsNets to address the above questions and to optimize the corresponding memory access profiles?

Since the above-discussed questions can pose contradicting requirements and constraints, there is a need for an in-depth analysis of the resource requirement and usage patterns of CapsNets processing before taking appropriate design decisions, which we discuss in the following Section IV.

IV. RESOURCE ANALYSIS OF CAPSNET INERENCE

First we investigate the Google’s CapsNet architecture of [2] that performs MNIST [4] classification, using the architectural organization presented in Fig. 9b. We analyze the performance and the on-chip memory requirements for different operations of the CapsNet inference, showing their on-chip read and write accesses. Afterwards, we analyze the DeepCaps [3] for the CIFAR10 [6] classification, showing that, overall, the accumulators have the major contributions in memory usage and accesses. Moreover, the energy breakdown analysis highlights the respective contributions of the accelerator and the memories. Note that our experiments obtain the same classification accuracies for these CapsNets as they have been proposed by their respective teams, i.e., 99.67% for the CapsNet on the MNIST dataset and 92.74% for the DeepCaps on the CIFAR10 dataset.

A. Performance and Memory Analyses for the Google’s CapsNet [2] on the MNIST Dataset

Memory Usage Analysis: Considering the design options discussed in Section II-B, we analyze the on-chip memory requirements for each operation of the CapsNet inference, as shown in Fig. 1. The dashed lines in Fig. 1 represent the maximum values. The overall size can be determined by the operation that requires the largest amount of memory (i.e., the PrimaryCaps layer). For this configuration, the on-chip SPM is composed of the data, weight and accumulator memories.

Performance Analysis: Fig. 2 presents the execution time (i.e., number of clock cycles) of different operations involved in the CapsNet inference. Note, the dynamic routing operations contribute for more than half of the execution time of the complete CapsNet inference. Overall, the performance is 116 frames-per-second (FPS) for the CapsAcc accelerator, as also reported in the work of [11]. If we combine the results of Figures 1 and 2, we notice that, potentially, a significant amount of leakage energy can be saved by the power-gating part of the on-chip memory, when the utilization is below 100%. We leverage this observation to develop an application-specific power management policy for memories of the CapsNet Accelerators, as discussed in Section V-B.

Memory Access Analysis: Fig. 10b provides a detailed analysis for each memory component (i.e., data memory, weight memory and accumulators), which enables an efficient
In the first two layers, the weight memory usage is quite low (see pointer 1 in Fig. 10), because the architecture can efficiently employ weight reuse for the convolutions. 

Data and weight memory requirements vary significantly across different operations. In the first two layers, the weight memory usage is quite low as compared to the other stages, because the architecture can efficiently employ weight reuse for the convolutions. In the ClassCaps layer the data memory usage is low (see pointer 2 in Fig. 10), because the corresponding data reuse is efficient.

- Weight reuse is relatively more efficient in the last six operations (dynamic routing), as compared to the first three (see pointer 3 in Fig. 10).
- During the dynamic routing, the off-chip memory is not accessed, except for read accesses in the first operation and write accesses in the last one (see pointer 4 in Fig. 27), due to the efficient data and weight reuse in these operations.

**B. Performance and Memory Analyses for the DeepCaps**

Similar analyses have also been carried on for a deeper and more complex capsule network such as the DeepCaps [3]. The performance in terms of clock cycles is shown in Fig. 9, and overall it is 9.7 FPS. Compared to the CapsNet, the DeepCaps shows a more distributed partition. Overall, we can notice that the most time-consuming operations are in the ConvCaps2D layers, which contribute for 73% of the execution time of the complete DeepCaps inference. The on-chip memory usage, reads and writes are shown in Fig. 11. Similar to the case of the CapsNet, the accumulator’s usage is higher than the data and weight memories. Moreover, the usage and accesses for the weight memory are low in the convolutional layers, but higher for the dynamic routing operations.

**C. Energy Breakdown Analysis**

To compute the energy consumption of the complete architecture, we develop the following two different versions. (a) Fig. 8a [1]: an accelerator (composed of NP array, activation unit and control unit), on-chip SPM buffers (data, weight and accumulator’s memory), and an on-chip SPM (for data and weights). The total on-chip memory is of 8MiB.

(b) Fig. 8b an accelerator with the same composition as above, but different architectures of on-chip and off-chip memories. The sizes are derived from the analyses of Section IV-C.

The energy breakdown is shown in Fig. 12. The results are obtained by synthesizing the DNN accelerator of [1], executing the Google’s CapsNet [2] for the MNIST dataset, in a 32nm CMOS technology, while the on-chip and off-chip memory...
values are obtained using the CACTI-P tool \cite{17} with the compatible technology parameters, as it is well-adopted by the memory community.

Our analysis shows that by designing a different memory hierarchy we can already save 73\% of the total energy, as compared to the state-of-the-art architecture in \cite{1}. This can be attributed to the significantly reduced leakage energy due to the lower on-chip memory size. Moreover, the on-chip memory consumes 31\% of the on-chip energy (i.e., accelerator and SPM). Hence, an application-driven memory power management (see Section V-B) can have a significant impact on the overall on-chip energy savings.

Note: the DeepCaps’ execution for the CIFAR10 dataset cannot be supported on the original baseline CapsAcc \cite{1} due to its memory requirements (i.e. DeepCaps does not fit in the 8 MiB memory of \cite{1}). Hence, a comparison similar to the results of Fig. 12 for executing the DeepCaps is not feasible. However, as we will demonstrate later in the paper, our proposed DESCNet memory architecture enables the deployment of DeepCaps with low hardware resources.

D. Summary of the Key Observations from our Analyses

Summarizing our analyses of Sections IV-A and IV-C the following key observations can be leveraged to design an efficient memory sub-system for the CapsNet hardware.

- Most of the energy is consumed by the (on-chip and off-chip) memory, as compared to the computational array.
- An application-driven memory hierarchy, composed of an on-chip SPM and an off-chip DRAM, can save up to 73\% of the energy on the Google’s CapsNet model, without compromising the throughput\cite{9} as compared to having a fully on-chip memory organization.
- The utilization of the on-chip memory is variable, depending upon the operation of the CapsNet inference. Thus, applying power-gating to the non-utilized sectors can further reduce the energy consumption.
- Partitioning the SPM into separate components (for data, weight and accumulator) can be beneficial for storing values and efficiently feeding them to the accelerator.

V. DESCNet: Scratchpad Memory Design

A. DESCNet Memory Architecture

The architecture of our DESCNet is depicted in Fig. 13. It is connected to the CapsNet accelerator and to the off-chip memory through dedicated bus lines. The SPM is partitioned into B banks, where each bank consists of SC number of equally-sized sectors. All the sectors with the same index across different banks are connected through a power-gating circuitry (implemented with sleep transistors\cite{10}) to support an efficient sector-level power-management control, at the cost of some area overhead. Our application-driven memory power management unit determines the appropriate control signals (i.e., ON ↔ OFF\cite{10}) for the sleep transistors. The transitions between sleep modes come at the cost of a certain wakeup energy and latency overhead, that needs to be amortized by the leakage energy savings which depends upon the sleep duration and the number of sectors in the sleep-mode. Note, our memory model can be generalized for different memory organizations supporting different sizes and level of parallelism, including multi-port memories. Towards this, we study the following three different design options.

(a) Fig. 14a - Shared Multi-Port Memory (SMP): a shared on-chip memory with 3 ports for accessing the weights, input data and accumulator’s storage in parallel.
(b) Fig. 14b - Separated Memory (SEP): weights, input data, and the accumulator’s partial sums are stored in separate on-chip memories.
(c) Fig. 14c - Hybrid Memory (HY): a combination of the above two design options, i.e., an SMP coupled with a SEP memory.
B. Application-Driven Memory Power Management

Our application-driven memory PMU determines the sleep signals according to the utilization profile of the memory, as observed in Figures 10a and 11. A simple schematic showing how a sleep transistor is connected to its memory sectors is depicted in Fig. 15. The sleep request is followed by the acknowledge signal, forming a 2-way handshake protocol. The timing diagram of a complete sleep cycle (ON → OFF → ON) is shown in Fig. 16. When exploiting the application-specific knowledge, it is known from the analysis presented in Section IV which sectors need to be activated during the execution of different operations. Hence, the wakeup latency overhead is transparently masked, i.e., the required sectors are pre-activated in advance, in such a way that they are active when needed.

C. Application-Driven Design Space Exploration (DSE) of the DESCNet Memory Designs

Considering the above memory models, we now determine their organization, sizes, the number of banks (B), and the number of sectors-per-bank (SC) systematically through a DSE methodology. We explore different configurations of the memory architecture and evaluate their area and energy consumption. Different levels of abstraction of application-driven knowledge (i.e., architecture and utilization profiles specific to CapsNets) are employed. In the subsequent equations and algorithms, we adopt the following notations:

- \( i \): index of the operations of the CapsNet inference.
- \( D_i, W_i, A_i \): operation-wise memory usage of data memory, weight memory and accumulators, according to the analyses shown in Figures 10 and 11.

- \( S_{Z_{\{S,D,W,A\}}} \), \( SC_{\{S,D,W,A\}} \), \( B_{\{S,D,W,A\}} \): size, number of sectors, number of banks of \( \{ \)shared memory, data memory, weight memory, accumulators\( \} \), respectively.
- \( \sigma(s) \): pool of available numbers of memory sectors for power-gating, given the memory size \( s \), which are all the power of two values in the range \([2^2, 2^{11}]\).

For all the memory designs, without loss of generality, the number of banks is chosen to be \( B_D = B_W = B_A = B_S = 16 \), as it corresponds to the number of rows and columns of the NP array of the CapsAcc architecture. To facilitate efficient data feeding to the accelerator, this parameter is not changed in our DSE.

For the SMP design, the size of the shared memory is derived from the operation-wise maximum memory usage scenario\(^{11}\) as shown in Equation 1:

\[
\text{SMP} : S Z_S = \max_i (D_i + W_i + A_i) \tag{1}
\]

For the SEP design, the sizes of the data memory, weight memory and accumulator are set as in Equation 2 based on the operation-wise maximum memory usage of the separated components.

\[
\text{SEP} : \begin{cases} 
S Z_D = \max_i (D_i) \\
S Z_W = \max_i (W_i) \\
S Z_A = \max_i (A_i)
\end{cases} \tag{2}
\]

For the HY design, sizing the memories becomes a more complicated challenge. Within the range allowed by the Algorithm\(^{11}\) the memory sizes considered in our design space have power-of-two values, with the addition of four randomly selected memory sizes (that are 25 kB, 108 kB, 450 kB, and 460 kB), to have more fine-grained results in the low-sized range. For every possible sizes of data memory, weight memory and accumulators, the size of the shared memory is computed as the operation-wise worst-case that still guarantees the minimum memory usage required by each operation.

After finding the appropriate memory sizes, the power-gating technique can be applied. It directly affects the number of sectors in the memory designs, since a sleep transistor is connected to each sector to switch ON or OFF the whole sector.

\(^{11}\)This value is due to a limitation of the CACTI-P\(^{12}\) tool, which sets the limit for the ratio between memory size and sector size to be at least 128.

\(^{12}\)Since only a finite values of memory sizes are acceptable, when computing the \( \max_i \) function, the memory size becomes the lowest acceptable size that is greater than or equal to the operation-wise maximum, and vice-versa for the \( \min_i \).
Hand, if $SZ$ equal to 0, its resulting $SZ$ and $A$ is: for each design option, the values of memory organization $D$. Our Methodology for the DSE of Scratchpad Memories cannot be achieved for a HY solution, due to the minimum constraints given in Algorithm 1. However, it represents a hypothetical extreme case to discuss.

Hence, for the memory designs where the power-gating is not supported, the number of sectors is 1. When the power-gating is supported, the choice of number of sectors directly influences the trade-off between the reduction in the static power and the overhead of the power-gating circuitry overhead. Towards this, Algorithm 2 describes all the combinations of valid number of sectors allowed by the function $\sigma(s)$ that are explored.

Algorithm 1: Exploration of hybrid memory sizes.

| Inputs: Operation-wise memory usage $D_i, W_i, A_i$ | Outputs: Hybrid memory sizes $SZ_D, SZ_W, SZ_A$. |
|--------------------------------------------------|--------------------------------------------------|
| $ret \leftarrow \{}$; | $ret \leftarrow \{}$; |
| for $sz_d \leftarrow \min(D_i)$ to $\max(D_i)$ do | for $sz_w \leftarrow \min(W_i)$ to $\max(W_i)$ do |
| | |
| for $sz_a \leftarrow \min(A_i)$ to $\max(A_i)$ do | |
| $sz_a \leftarrow \max(0, D_i - sz_d) + \max(0, W_i - sz_w) + \max(0, A_i - sz_a)$; | $ret \leftarrow ret \cup \{(sz_a, sz_d, sz_w, sz_a);$ |
| end | end |
| end | end |
| return $ret$; | return $ret$; |

Algorithm 2: Exploration of number of memory sectors.

| Inputs: Memory sizes $sz_a, sz_d, sz_w, sz_a$ | Outputs: Number of sectors $SC_a, SC_d, SC_W, SC_A$ |
|--------------------------------------------------|--------------------------------------------------|
| $ret \leftarrow \{}$; | $ret \leftarrow \{}$; |
| for $sc_a \in \sigma(sz_a)$ do | for $sc_d \in \sigma(sz_d)$ do |
| | |
| for $sc_w \in \sigma(sz_w)$ do | for $sc_a \in \sigma(sz_a)$ do |
| $ret \leftarrow ret \cup \{(sc_a, sc_d, sc_w, sc_a);$ | $ret \leftarrow ret \cup \{(sc_a, sc_d, sc_w, sc_a);$ |
| end | end |
| end | end |
| return $ret$; | return $ret$; |

Following the above-discussed procedures, we have generated 15,233 configurations of the DESCNet architecture for the CapsNet, and 215,693 configurations for the DeepCaps, with different design options (SMP, SEP, HY), different sizes and number of sectors. Note that the SMP and SEP design options can also be considered as the boundary cases of the HY design option. On one hand, a HY organization where $SZ_D, SZ_W$ and $SZ_A$ are maximum is equivalent to the SEP, because the corresponding $SZ_S$ for the HY results to be null. On the other hand, if $SZ_D, SZ_W$ and $SZ_A$ of a HY organization are all equal to 0, its resulting $SZ_S$ would have the same value as the one for the SMP.

D. Our Methodology for the DSE of Scratchpad Memories

The flow of our methodology is depicted in Fig. 17. Inputs are: CapsNet models and hardware accelerators for CapsNets. Output is: for each design option, the values of memory organization (i.e., size, number of banks and sectors), the energy consumption and area are generated. The key steps of our methodology are:

1) The extraction of the memory usage and memory accesses for each operation of the CapsNet inference. While the usage is needed for defining the design options and sizes, the read and write accesses, along with the operation-wise clock cycles, are used for computing the energy consumption.

2) An analysis of the design options (SMP, SEP, HY), and definition of the memory configurations, such as size and number of banks and sectors for the power-gating.

3) A DSE of the possible memory configurations under analysis, through an exhaustive search, to find and select the non-dominated solutions. The estimation of area and energy consumption, with and without the power-gating option, are conducted through the CACTI-P tool [17]. Note: We have performed an exhaustive search because, due to the practical limitations on the memory sizes and number of sectors, as discussed in Section V-C, the execution time of the search still results relatively low [14]. However, if the search space increases, or more sophisticated memory evaluations require longer computational time, a heuristic search algorithm can easily be integrated into our methodology, in order to find a solution more quickly. Such a solution may be away from the optimal solution as found by the exhaustive search.

VI. EVALUATING OUR DESCNET ARCHITECTURES

A. Results for Google’s CapsNets [2]: Area and Energy of the On-Chip Memory

We evaluate different memory architectural options (as discussed in Section V) for area and energy consumption, using the CACTI-P [17] tool. The results of different DESCNet architectural designs of the scratchpad memory for the CapsNet on the MNIST dataset are discussed below. Design Space Exploration Results and Selected Configurations (Fig. 18): The figure shows the trade-off between energy and area for 15,233 different DESCNet architectural configurations. For each design option (SMP, SEP, HY) and its corresponding version with power-gating (with suffix -PG), the Pareto-optimal solutions with lowest-energy are selected. Note, while SEP, SEP-PG and HY-PG belong to the Pareto-frontier, HY, SMP and SMP-PG are dominated by other configurations. Their size and number of sectors are reported in Table IV.

Area Comparison (Fig. 19): The figure shows the area breakdown of different memory components of the DESCNet. We notice that, while the organization SEP has relatively larger

\[13\]Note that this particular solution, with $SZ_D = SZ_W = SZ_A = 0$, cannot be achieved for a HY solution, due to the minimum constraints given in Algorithm 1. However, it represents a hypothetical extreme case to discuss.

\[14\]We measured the times for executing a complete DSE, including the estimation of energy and area provided by CACTI-P [17], of 1.5 minutes for the Google’s CapsNet and of 22 minutes for the DeepCaps, when running with a single-thread application on an AMD Ryzen 5 CPU with 32GB RAM.
memory sizes, compared to the other architectures, their area is relatively smaller. This effect is due to having single-port memories instead of a shared multi-ported design, where the latter requires more area for the complex interconnections. Indeed the area of the HY organization is lower than the SMP, due to a small-sized shared memory. Moreover, the power-gating circuitry also incurs additional area overhead (on average, 2.75% for equally-sized SPMs) due to the sleep transistors.

**Energy Breakdown at the Component Level (Fig. 19):**

The figure shows that the design option HY-PG is more energy efficient than the others, due to having high flexibility and thus the higher potential of power-gating an heterogeneous combination of sectors, as compared to other designs such as the SEP-PG, whose energy consumption is slightly higher. Note, despite having a smaller size than the weight memory, the shared memory of the HY organization consumes a higher energy, due to the more complex internal architecture of a multi-ported memory.

**Dynamic vs. Static Energy Consumption (Fig. 19):**

When comparing different architectural designs, the figure illustrates that: (1) moving from SMP to SEP and then to HY, the dynamic energy can be reduced progressively; (2) moving from HY to HY-PG, the static energy can be further reduced, due to the benefits of the power-gating, and (3) the dynamic energy remains unchanged between non-PG and -PG organizations.

Besides this, we noticed that the wakeup latency overhead is negligible. Even though it is masked by preloading the necessary values, its value is very low (0.072\(\mu\)s) compared to the average computational time of an operation (614\(\mu\)s) where the sleep transistors driving their corresponding memory sectors are in a steady state, either ON or OFF. This behavior also explains why the contribution of the wakeup energy (on average 1.6\(\mu\)J), which appears during the transitions between OFF and ON, is low.

**Energy Breakdown for the Different Operations of the CapsNet Inference (Fig. 19):**

Though the absolute values vary, the relative proportions of the energy consumption by different operations of the CapsNet inference remain approximately similar across different memory designs. The highest portion of energy comes from the PrimaryCaps (Prim) layer, since it has a high memory utilization and frequent access to it, requiring most of the available memory, and thereby providing limited power-gating potential. On the contrary, the energy consumed by the dynamic routing operations (i.e., Sum+Squash, Update+Softmax) is significantly lower for the -PG organizations (see pointer 3 in Fig. 19).

For the detailed memory breakdown for the selected Pareto-optimal solutions, we refer to Appendix B.1.

### B. Results for DeepCaps [3]: Area and Energy of the On-Chip Memory

Similarly to the above-discussed results for the Google’s CapsNet [2], detailed evaluations are also conducted for the DeepCaps [3]. Fig. 20 shows the solutions in the space area vs. energy, for 215,693 different memory design organizations. The selected solutions with memory size and number of sectors are reported in Table I. Note that the high-energy solutions have only 1 sector (i.e., the power-gating cannot be applied), the high-area solutions have the size of the shared memory equal to 8 MiB, while the solutions with low area and low energy consumption have a shared memory with a size lower than or equal to 256 kib. Compared to the CapsNet, the DeepCaps needs larger memory sizes, to efficiently handle the large-scale and more-complex computations.

### C. DSE for the HY-PG Design Option with Size-Constrained Memory for DeepCaps [3]

Motivated by the observation that the shared memory size has a great impact on the efficiency (see Fig. 20), and to the fact...
that embedded systems might have size-constrained memory, we extend the analysis by exploring the HY-PG architectural organizations with a memory constraint. More specifically, we performed a DSE by constraining the maximum size of the shared memory. Moreover, the memory usage patterns and partitions reported in Appendix B show that the shared memory of the HY and HY-PG design options do not always require having three ports, because for some solutions, the shared memory only needs to store one or two different types of values. 

To this regard, in this analysis we also explored the space of the HY-PG solutions when the number of ports of the shared memory (P_S) is constrained. Fig. 22 shows their tradeoffs between area and energy consumption, for 113,337 different memory configurations. The most efficient solutions have a size of the 1-port shared memory equal to 2 MiB and 4 MiB (see pointer (1)) in Fig. 22a), while the worst results are obtained by the combination of a shared memory of 4 MiB and accumulator memory of 8 MiB (see pointer (2)). Note, despite having a smaller-sized shared memory, the solutions with the 1-port shared memory of size 128 kiB and 256 kiB (see pointer (3)) are relatively less efficient. This implies that such a size of the shared memory can more efficiently couple with the rest of the system, to achieve overall a lower area and energy consumption. Moreover, as clearly visible from Figure 22b), the area and energy efficiency is improved by having a lower P_S. The detailed memory configuration for the HY and HY-PG lowest-energy solutions are shown in the respective lines of Table I.

D. Impact of the Memory on the Complete CapsNet Accelerator Architecture

Based on the evaluations performed in Section VI-A we select two Pareto-optimal DESCNet architectures for the CapsNet, which are SEP and HY-PG. The choice of these organizations is strategic, because they represent the Pareto-optimal solutions with the lowest area and the lowest energy, respectively. Note that there is no performance loss, compared to the CapsNet and DeepCaps executed on the baseline CapsAcc [1]. We synthesize the complete architecture of the DNN accelerator executing CapsNets for the MNIST dataset and DeepCaps on the CIFAR10 dataset in a 32nm CMOS technology library, using the ASIC design flow with the Synopsys Design Compiler.

The detailed area and energy estimations of the complete on-chip architectures for the Google’s CapsNet, comprising the accelerator and the on-chip memories with SEP-PG and HY-PG organizations, are shown in Figures 23 and 24, respectively.

When comparing the initial design as discussed in Section IV-C version (b) with the SEP (Fig. 23), the total on-chip memory energy is reduced by 65% and the on-chip memory area by 91%. Compared to version (a), our SEP DESCNet incurs 78% reduced energy and 47% reduced area for the complete accelerator.

Our proposed DESCNet HY-PG organization reduces the on-chip energy by 82% and the on-chip area by 35%, compared to the version (b), while reducing the total energy and the total area by 79% and 40% compared to the version (a), respectively.

Consequently, compared to version (a), which corresponds to the state-of-the-art design of [1], our proposed approach can provide total energy and area reductions, comprising accelerator, on-chip memory and off-chip memory, of up to 79% and 47%, respectively, without any performance loss.

Energy and area estimations of the complete on-chip architecture executing the DeepCaps, using the SEP-PG organization, are reported in Fig. 25. The graph shows a clear dominance of the accumulator memory on both the on-chip area and the on-chip energy, due to its large size. On the contrary, the HY-PG, P_S=1 organization results reported in Fig. 26 show a relatively more balanced distribution of the energy and area between the accumulator and the shared memory. As previously discussed in Section IV-C since the original baseline architecture of [1] cannot execute the DeepCaps for the CIFAR10 dataset, we cannot compare their work with our DESCNet design deploying the DeepCaps. This also shows that our memory sub-system can indeed successfully support DeepCaps enabling its memory-efficient acceleration, which is not possible for the original baseline CapsAcc [1].

E. Results Summary and Discussion

Table II shows the detailed results of the area and energy consumption for the different DESCNet architectures, obtained by our DSE, for the CapsNet and the DeepCaps. The following key observations can be derived from our analyses.

- Despite many efforts in optimizing the computational arrays of the DNN accelerators, more fruitful area and energy savings are obtained when the optimizations are applied to the memory, as showcased in this paper with the DNN accelerators executing both the Google’s CapsNets and the DeepCaps.
Fig. 21: DeepCaps results for different components of the DESCNet memory configurations: (a) Area breakdown, (b) Energy breakdown, (c) Static vs. dynamic energy consumption, (d) Energy breakdown of the different operations of the DeepCaps inference.

TABLE III: Area and energy consumption results for different DESCNet architectural organizations.

| NN   | Mem    | Shared Mem | Data Memory | Weight Memory | Accumulators | Wakeup Energy |
|------|--------|------------|-------------|---------------|--------------|---------------|
|      |        | Area [mm²] | Energy [mJ] | Energy [mJ]   | Energy [nJ]  |               |
|      |        |            |             |               |              |               |
| CapsNet |       |            |             |               |              |               |
| SEP | — | — | 0.334 | 0.051 | 0.301 | 0.044 |
| SEP-PG | — | — | 0.469 | 0.053 | 0.135 | 0.044 |
| SMP | 2.521 | 1.859 | 1.529 | 0.352 | — | — |
| SMP-PG | 2.958 | 1.875 | 0.668 | 0.348 | — | — |
| HY | 0.519 | 0.068 | 0.348 | 0.125 | 0.044 | 0.238 |
| HY-PG | 1.061 | 0.004 | 0.046 | 0.080 | 0.213 | 0.045 |
| HY-PG, P(embed)=1 | 17.731 | 6.019 | 120.913 | 0.642 | 0.896 | 0.040 |

Fig. 22: Design space exploration results for the HY-PG DESCNet memory configurations for the DeepCaps, having constraints on the size and number of ports of the shared memory.

Fig. 23: (a) Energy and (b) area breakdown of our CapsNet inference architecture using SEP memory.

Fig. 24: (a) Energy and (b) area breakdown of our CapsNet inference architecture using HY-PG memory.

Fig. 25: (a) Energy and (b) area breakdown of our DeepCaps inference architecture using SEP-PG memory.

Fig. 26: (a) Energy and (b) area breakdown of our DeepCaps inference architecture using HY-PG, P(embed)=1 memory.

bad design choice, because of the resource-hungry hardware overhead for handling heterogeneous accesses, which are not necessary if we systematically study the application-driven memory resource requirements. Indeed, as highlighted in Fig. 20 having $S_z \leq 256 \text{ kiB}$ can relatively reduce jointly the energy and the area, compared to other solutions with larger $S_z$.

- For a certain set of solutions belonging to the HY and HY-PG design options, the multi-port shared memory can be replaced by an equivalent single-port, offering further energy and area reductions due to a more balanced memory breakdown between the accumulator and the shared memory.

- Employing efficient on-chip SPM memory organization architectures (e.g., SEP, SEP-PG, and HY-PG) significantly reduces the hardware resource requirements, thereby bearing the development of DNN accelerator executing complex operations such as the Capsule Networks in resource-constrained scenarios, which are typical for IoT-edge devices.
VII. CONCLUSION

Based on an extensive analysis of the CapsNet inference, we identified that a significant amount of energy can be saved by designing a specialized memory hierarchy. To achieve high efficiency, we designed the on-chip SPM in a way to minimize the off-chip memory accesses, while maintaining high throughput. We explored different architectural designs for our DESCNet, i.e., a specialized scratchpad memory architecture for the CapsNet accelerators. It is equipped with an application-driven memory power management unit to further reduce the leakage power. We performed comprehensive evaluations for both the Google’s CapsNet and the DeepCaps, and illustrated significant benefits of our proposed architectures and optimizations. As per our knowledge, this paper proposes the first specialized memory architecture for a DNN inference accelerator executing CapsNets. Our work motivates the need for application-specific design and optimizations towards energy-efficient memory architectures for the next-generation embedded DNN inference hardware.

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APPENDIX A
OFF-CHIP MEMORY ANALYSIS

1. Operation-Wise Off-Chip Analysis for the Google’s CapsNet on the MNIST dataset

The off-chip accesses\textsuperscript{15} reported in Fig. 27, can be computed using the Equations (3) and (4), which are valid for the first three operations, indicated with the index $i$. $RD_{off}$ and $WR_{off}$ indicate the SPM read and write accesses, while the subscripts $D$ and $W$ stand for on-chip data and weight memories, respectively. In the dynamic routing, the off-chip memory is not accessed, except for the first and last operation, because all the values required during the dynamic routing are stored on-chip.

\begin{align*}
(RD_{off})_i &= (WR_D + WR_W)_i \quad (3) \\
(WR_{off})_i &= (RD_D)_{i+1} \quad (4)
\end{align*}

Note, the peak of accesses are measured for the PrimaryCaps (Prim) layer. On the contrary, during the dynamic routing, the off-chip memory is not accessed, except for read accesses in the first operation and write accesses in the last one (see pointer \textsuperscript{4} in Fig. 27), due to the efficient data and weight reuse in these operations.

2. Operation-Wise Off-Chip Analysis for the DeepCaps on the CIFAR10 dataset

The off-chip accesses for the DeepCaps are shown in Fig. 28. While reads and writes proportionally decrease by decreasing the sizes of the convolutional layers, for the dynamic routing the accesses are low, thanks to the efficient reuse. The peak is visible at the beginning of the ClassCaps layer (see pointer \textsuperscript{5} in Fig. 28), which is due to the large number of weights in that operation.

APPENDIX B
SCRATCHPAD MEMORY BREAKDOWN

1. Breakdown for the Selected Pareto-Optimal Solutions of the Google’s CapsNet on the MNIST dataset

Fig. 29 shows, for different design options, which type of memory is used to store the operation-wise information. While for the SEP and SMP designs the picture is clear and relatively simple, this mean of visualization is extremely useful for the hybrid solutions (HY and HY-PG). It shows in a comprehensive way, for each operation, the fraction of the memory usage that is covered by the shared memory (represented with silver-colored filled bars), thereby lowering the sizes of the other memories. The main benefit of having an HY configuration is that the peaks in the operation-wise memory usage can be amortized by the utilization of the shared memory (see pointer \textsuperscript{7} in Fig. 29).

An example showing the power-gating mechanism for the HY-PG organization is reported in Fig. 30. Here, the colored boxes represent the memory sectors. The ON sectors are filled in white, while the OFF sectors in grey. The figure highlights that the shared memory is often powered OFF, except for the ClassCaps (Class) operation, where its sectors are active and contain part of the necessary weights for this operation. (see pointer \textsuperscript{8} in Fig. 30).

2. Breakdown for the Selected Pareto-Optimal Solutions of the DeepCaps on the CIFAR10 dataset

The memory breakdown showing operation-wise which type of memory is used is shown in Fig. 31. Note, the analysis shows that the shared memory of the HY and HY-PG design options do not always require having three ports, because for some solutions, the shared memory only needs to store one or two different types of values. For example, as shown by pointer \textsuperscript{10} in Fig. 31c, the shared memory covers simultaneously part
of the data and part of the accumulator memory usage for the operation CONV2D, while, for all the other operations of the DeepCaps, at most one type of value is covered by the shared memory. Therefore, for this particular solution, a 2-port shared memory is sufficient to guarantee the correct functioning of the system, thus potentially saving area and energy, compared of having an equivalent 3-port memory.

![Fig. 31: Memory breakdown for different design options of the DESCNet for the DeepCaps. The dashed lines show the respective memory sizes.](image)

Therefore, this outcome motivated us to conduct the exploration of the space of the HY-PG solutions with constraints on the number of ports of the shared memory, as discussed in Section VI-C. Fig. 32 shows the memory breakdown for the lowest-energy HY-PG solutions with the given constraints on the shared memory. The 1-port shared memory of sizes 2 MiB and 4 MiB can partially contain accumulator values for some DeepCaps’ operations, while the lowest-energy solutions for the 2-port and 3-port shared memory of size 2 MiB partially contain the weights and data values (see pointer 15 in Fig. 32). Hence, for the latter two solutions, the size of the accumulator memory is not reduced.

![Fig. 32: Memory breakdown for the HY-PG DESCNet design option with different constraints on the shared memory for the DeepCaps. The dashed lines show the respective memory sizes.](image)