Abstract

In this paper, novel Si/SiGe fin on insulator (FOI) structure fabrication on bulk-Si substrate is systematically explored. A notched Si/SiGe fin etching is first achieved by using a novel three-step etching after a high-quality of SiGe layer epitaxially grown is realized on a Si substrate by optimizing the epitaxial process. To fabricate the Si/SiGe FOI structure, isolation of upper Si/SiGe fin above the notch is investigated by a direct rapid thermal anneal (RTA) oxidation scheme, spike anneal post SiGe fin reveal scheme, and SiN spacer protection scheme. It is found that all these three schemes can achieve the upper Si/SiGe isolation at the notch location, but the direct RTA oxidation scheme suffers the issue of serious oxidation of SiGe fin because SiGe is more easily oxidized than Si in O2 ambient. Furthermore, compared with the direct oxidation scheme, the spike anneal post SiGe fin reveal scheme can attain an obvious better SiGe fin profile. However, there is still a minor lateral loss of SiGe fin caused by the oxidation of SiGe fin due to the residual O2 in N2 ambient. The SiN film covering the revealed SiGe fin before spike anneal treatment may be an effective solution to avoid the oxidation of SiGe fin. Meanwhile, SiN spacer protection scheme by employing a SiN spacer post the step-1 etching of the three-step etching can realize the Si/SiGe FOI structure and protect the upper SiGe fin from oxidation during the low-temperature RTA oxidation process. Therefore, using the SiN film or spacer to protect SiGe from oxidation is a necessary way to fabricate the Si/SiGe FOI structure. Meanwhile, the SiN spacer protection scheme with a relative low temperature RTA isolation oxidation is a prefer choice compared with the spike anneal post SiGe fin reveal scheme.

1. Introduction

High mobility SiGe channel p-FinFET device has been demonstrated to be a promising candidate for future generation of high-performance logic application owing to its advantages of higher hole mobility, better negative bias temperature instability (NBTI) reliability than silicon and more compatible with present silicon platform [1–5]. Meanwhile, SiGe-on-insulator (SGOI) substrate demonstrates a great advantage on leakage reduction due to a naturally isolated fin channel and can attain excellent driven current performance and subthreshold swing (SS) characteristics through enhanced 3D Ge condensation and advanced gate stack process [6–8]. However, the SGOI substrate suffers from cost issues and may face serious self-heating effects due to low thermal conductivity of SiO2 buried oxide layer [9]. As a result, the SGOI-liked FinFET, e.g. SiGe or Si/SiGe fin on Insulator (FOI) FinFET, fabricated on bulk Si substrate takes both advantages of these two technologies [10]. At the same time, this FOI structure can omit the ground-plane (GP) implantation, which is required to suppress the leakage current in the sub-fin region for the normal FinFET [11]. Therefore, SiGe or Si/SiGe FOI FinFET may be one of the most promising candidates for further device scaling.

So far, some papers have reported the fabrication process of the advanced FOI structure for the Si fin by the bottom oxidation through STI process [12] or an advanced reactive ion etching combined with a liner oxidation process [10, 13]. However, there are few reports on the fabrication of Si/SiGe FOI structure in detail. At the same time, the above traditional oxidation method may lead to the thermal stability issue of SiGe since the Ge bulk
crystal melting point is only 937 °C. Therefore, the fabrication of Si/SiGe FOI structure is still a very challenge task and needs to be further studied.

In this work, a notched Si/SiGe fin is first demonstrated by a novel three-step etching after a high-quality of SiGe layer epitaxially grown on Si substrate. Then, to fabricate the Si/SiGe FOI structure, isolation of upper Si/SiGe fin above the notch is investigated in detail by a direct rapid thermal anneal (RTA) oxidation (scheme A), spike anneal post SiGe fin reveal (scheme B), and SiN spacer protection scheme (scheme C).

2. Experiment

Three schemes were employed to develop the Si/SiGe FOI structure and their process flow are presented in figure 1. The SiGe film was epitaxially grown on a Si substrate for all schemes by reduced-pressure chemical vapor epitaxial deposition. Then, the novel three-step etching process was applied for the notched Si/SiGe fin patterning through the sidewall image transfer method. Subsequently, the direct oxidation of the notched Si fin from both sides was implemented to isolate upper fin structure and the bottom Si substrate by an RTA treatment in O₂ ambient. After the shallow trench isolation (STI) planarization and densification annealing, SiGe fin reveal was realized by using 1:100 diluted HF solution (scheme A). Compared with scheme A, scheme B employed a spike anneal treatment post SiGe fin reveal instead of low-temperature RTA oxidation post three-step etching to achieve notched Si fin being oxidized. The scheme C employed a SiN spacer post the step-1 etching of the three-step etching to protect the upper fin from oxidation during the low-temperature RTA oxidation process post the notched Si/SiGe fin patterning.

Figure 1. Process flow of Si/SiGe FOI fin structure fabrication under different schemes.
High-resolution x-ray diffraction (HRXRD), scanning electron microscopy (SEM) and scanning transmission electron microscopy (STEM) were used to check the quality, and etching profile of the Si/ SiGe FOI structure. Additionally, the composition of the SiGe film was ascertained through energy-dispersive x-ray spectroscopy (EDX) mapping.

3. Results and discussion

3.1. High-quality SiGe epitaxial grown

The high-quality of SiGe epitaxial growth on Si substrate is realized by optimizing the epitaxial process under the STI-last scheme [14]. A relative low-temperature of H₂ prebaking process at 825 °C for 7 min is employed to achieve an excellent surface of the Si substrate after a standard BOE clean. Afterward, epitaxial growth is carried out at reduced pressure (20 Torr) using H₂ as carrier gas. The precursor gases are SiH₂Cl₂ and GeH₄ for SiGe growth at 650 °C. The crystalline microstructure result of the SiGe film detected by HRXRD in the vicinity of the (004) Bragg peak with a Cu peak radiation is shown in figure 2. Well defined satellite peaks and small-intensity fringes are found and they are the characteristic of high-quality SiGe film [15]. Moreover, the fitting result shows that the thickness SiGe film is of 29.58 nm and the percentage of Ge atom is 31.83%.

3.2. Notched Si/SiGe fin etching

To achieve a notched Si/SiGe fin etching, a novel three-step etching process is employed in the same dry etch chamber. An anisotropic etching process by Cl₂/HBr/O₂ plasma under the ratio of 8:4:1 is firstly performed for the SiGe fin and partial Si fin etch (step-I). Then, the etched fin surface is lightly oxidized by the high-pressure oxygen plasma to form a thin layer of oxide, which can protect the etched SiGe and Si fin from etching during the following etching. Afterward, an isotropic etch by SF₆ plasma is performed to form a pair of notches on the Si fin sidewalls (step-II). Finally, a Cl₂/HBr/O₂ plasma etching process is performed for the following Si fin etch (step-III). Its etching result is presented in figure 3. It is found that a notched Si/SiGe fin etching is realized and the remaining width of the notched Si fin is ~10 nm, which can physically support the upper fin. In addition, the lateral recess depth can be precisely defined by adjusting the etching time, power, flow rate and pressure of SF₆ plasma. At the same time, the notch location can be modulated by adopting the etching time of step I and upper fin above the notch is the stacked Si/SiGe fin in this work.

3.3. Isolation upper fin by a direct oxidation

In previous Si FOI process, the direct isolation oxidation of 1050 °C by a rapid thermal oxidation or furnace tool post three-step etching is employed to isolate the Si fin above the notch [13]. This thermal budget of isolation oxidation will cause the thermal stability issue of SiGe, such oxidation or Ge diffusion, because the Ge bulk crystal melting point is only 937 °C. As a result, RTA treatment at a relative low-temperature in O₂ ambient is implemented for the isolation oxidation of Si/SiGe FOI structure. In addition, SiGe film can keep stable without obvious Ge diffusion when the temperature of RTA treatment in N₂ ambient is no more than 900 °C [16]. Therefore, RTA treatment of 800 and 850 °C for 120 s in O₂ ambient are employed and their results are shown in figure 4. It can be noted that fully isolation the notched fin structure can be achieved under the RTA oxidation at 850 °C for 120 s, but the SiGe fin suffers the issue of unaccepted oxidation at the same time. Furthermore, even the temperature of RTA oxidation is reduced to 800 °C, the oxidation of SiGe fin is still found and the width of
left notched Si fin is \( \sim 5 \) nm. It means that longer treatment time of RTA under 800 \(^\circ\)C will be used to realize the isolation and it also will cause the unaccepted oxidation of SiGe fin.

To achieve an isolation of the notched fin structure without obvious oxidation of SiGe, a tetramethyl ammonium hydroxide (TMAH) solution etching at 20 \(^\circ\)C is first implemented to further reduce the width of
notched Si fin post three-step etching. This is because the TMAH solution can achieve a reasonable etching rate of Si and have a high selectivity to SiGe by optimization its concentration and temperature [17]. It is found that the width of notched Si fin can be decreased from ~10 nm to ~5 nm after TMAH etching and it still can physically support the upper fin well, as shown in figure 5(a). Moreover, the notched Si fin has a typical etching characteristic of alkaline solution since the Si(001) and (110) directions etching much faster compared to the Si (111) crystallographic planes [18]. Based on the SEM result in figure 4(a), RTA treatment with a lower temperature and longer time should be introduced even the width of notched Si fin is reduced ~5 nm. Therefore, RTA treatment of 760 °C for 240 s is introduced to form the isolation of the notched fin structure. Its result is presented in figure 5(b). Compared with figure 4(a), the isolation of the notched fin is achieved, but a slightly weaker oxidation of SiGe fin is still found. The above results show that forming isolation of Si/SiGe FOI structure by using the direct oxidation after the three-step etching is not feasible because SiGe is easily oxidized in O₂ ambient.

### 3.4. Isolation upper fin by a spike anneal post SiGe fin reveal

To avoid obvious oxidation of SiGe fin, a spike anneal under 1050 °C in a N₂ ambient post SiGe fin reveal is proposed. Post SiGe fin reveal, the notched Si fin can be oxidized during the spike anneal due to the surrounding STI oxide. However, SiGe fin can maintain stable during the spike anneal in N₂ ambient. Moreover, STI surrounding fin can act as a mechanical anchor to hold the fin straight during the spike anneal treatment. Figures 6(a) and (b) present the isolation upper fin structure formed on a bulk Si substrate by one time and three times spike anneal post SiGe fin reveal. One time spike anneal treatment cannot attain a full isolation of the notched Si fin and the width of left notched Si fin is ~3.5 nm. This is because the surrounding STI oxide cannot provide the enough oxidation species to oxidize the notched Si fin. However, a Si/SiGe FOI structure is achieved

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**Figure 5.** (a) TMAH etching post three-step etching and (b) RTA treatment in O₂ ambient under 760 °C for 240 s post TMAH etching for the Si/SiGe FOI structure.
after three times spike anneal treatment. In particular, the SiGe fin profile under this new proposal is obviously better than the direct oxidation post three-step etching method.

To further clarify the effect of spike anneal on the SiGe fin, the STEM of sample in figure 6(b), and its Si and Ge elements EDX mapping analysis results are presented in figure 7. No obvious Ge diffusion is found and the distinct interface between SiGe and Si is maintained. However, there is still a minor lateral loss of SiGe fin compared with the below Si fin boundary. The oxidation of SiGe fin during the spike anneal treatment is highly suspected owing to the residual O2 in N2 ambient. The revealed fin covered by a SiN film before spike anneal treatment can be implemented to further protect the SiGe fin from oxidation in the future.

3.5. Isolation upper fin by a SiN spacer protection

Another strategy to form Si/SiGe FOI structure is to introduce a SiN spacer post the step-I etching of the three-step etching and this SiN spacer can protect the upper SiGe fin from oxidation during the low-temperature RTA oxidation process post notched Si/SiGe fin patterning. Finally, the SiN spacer can be removed by hot H3PO4 solution before STI dep because the H3PO4 solution has a high selectivity to SiGe [14]. The SEM image of Si/SiGe FOI structure after RTA oxidation of 850 °C for 120 s under this new proposal is shown in figure 8. It is found that a fully isolation of the notched fin structure can be achieved. Moreover, the SiGe fin can maintain well without oxidation impact owing to the existence of SiN spacer. Based on the above results, introduction of the SiN material as the SiGe protection layer before isolation oxidation is an essential for the fabrication of Si/SiGe FOI structure. Moreover, considering the temperature of RTA anneal in N2 ambient is 1050 °C, the SiN spacer protection scheme with a relative low temperature RTA isolation oxidation is a better choice.

**Figure 6.** Isolation upper fin structure formed on a bulk Si substrate by spike anneal for one time (a) and three times (b) post SiGe fin reveal.
4. Conclusion

In this work, a notched Si/SiGe fin is demonstrated by a novel three-step etching after a high-quality of SiGe layer epitaxially grown on Si substrate. For the isolation of upper Si/SiGe fin, a direct low-temperature RTA oxidation in O$_2$ ambient is not feasible and a spike anneal in N$_2$ ambient post SiGe fin reveal also attains a minor oxidation of SiGe fin. However, employing a SiN spacer after the step-I etching of the three-step etching can realize the Si/SiGe FOI structure without SiGe fin oxidation. Therefore, using the SiN film or spacer to protect SiGe from oxidation is a necessary way to fabricate the Si/SiGe FOI structure. Meanwhile, the SiN spacer protection scheme with a relative low temperature RTA isolation oxidation is a better choice compared with the spike anneal post SiGe fin reveal scheme.
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Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

ORCID iDs

Yongliang Li https://orcid.org/0000-0002-5590-861X
Jun Luo https://orcid.org/0000-0002-5122-6806

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