Design, analysis, and implementation of a new high-gain P-type step-up dc/dc converter with continuous input current and common ground

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Abstract
Step-up converters are increasingly developed for renewable energy and storage systems in order to raise the output voltage of those resources to higher voltage levels. Conventional step-up structures, such as P-type boost converter, provide low voltage gain, and they must be cascaded with the same modules to produce higher boost factors. This conversion method reduces overall efficiency. Affording higher gains with lower duty cycles and single-stage conversion increase efficiency. This paper proposes a new step-up P-type dc/dc converter with high voltage gain even with lower duty ratios. Additionally, it has continuous input current, high efficiency, and common ground between the input and the output. Detailed analysis is presented, and the performance of this new topology is compared with other high-gain step-up converters. Simulations and experiments evaluate the achievements of this topology. Results prove the proposed structure.

1 | INTRODUCTION

Step-up converters are broadly designed and developed for dc microgrid [1, 2], electric vehicles [3, 4], distributed generation [5], and many other applications. There are several methods to design step-up converters [6], which are grouped into six categories, as illustrated in Figure 1. Each method has its pros and cons. The switched-capacitor-based topologies like those presented in [7, 8] provide high voltage gain. However, they need large number of capacitors that affect the lifetime of the converter. A similar problem also exists in switched-inductor-based topologies [9]. Transformer-based step-up converters, such as the conventional flyback, forward [10], push–pull, half-bridge, and full-bridge [11] converters, require a large turns-ratio for ultra step-up applications that increases the volume of the high-frequency transformer, and consequently it increases the cost.

Recently, a new family of boost converters has been developed, which is called impedance-based converters. These converters usually incorporate an impedance network and a switching circuit, including power switches and power diodes that provide high output voltage gain based on a specific switching algorithm. Different derivatives of impedance networks, such as Z-source [12, 13], quasi Z-source [8, 14–17], X-source [18], Y-source [19], Γ-source [19], and transformer-based Z-source [20], have been presented and evaluated. They are also applicable for use with all types of power electronics converters [20, 21]. They provide single-stage conversion feature and high gain, but some of them may be exposed to high voltage and current stresses, low efficiency, and common-mode problem. Some articles especially concentrate on reducing the voltage and current stress of power switches in impedance-based conversion [22–24], fast dynamic response of impedance networks [25], decreasing the output voltage ripple of impedance-based converters [26], and the modular design of these topologies [27, 28]. Recently, the active form of Z-source converters has been reviewed and cited by Nozadian et al. [29], comprising switched-boost networks (SBN) [30] and other derivations, such as embedded SBN [31] and quasi-SBN [32, 33].

The topic of modular boost converters has received considerable interest. In this type, a step-up cell with a specific configuration of components is designed, and the final step-up topology is produced according to that manufactured cell, together with a
FIGURE 1 Category of methods for designing step-up converters

TABLE 1 Summary of voltage and current stresses on semiconductors in CCM

| Parameter Stress | Parameter Stress |
|------------------|------------------|
| $V_{D1}$         | $V_{D4}$         |
| $V_{D2}$         | $V_{D1}$         |
| $V_{D3}$         | $V_{Q2}$ and $V_{D5}$ |
| $I_{D1}$         | $I_{D4}$ + $\Delta I_1$ |
| $I_{D2}$         | $I_{D3}$ and $I_{Q2}$ |
| $I_{D3}$         | $I_{Q1}$ |

particular arrangement [27, 28, 34, 35]. Those are usually extensible that yields a high gain. However, the overall efficiency is reduced if compared with the one step-up cell. As an instance, Mohammadi et al. [36] proposed an efficient P-type step-up cell that although has continuous input current, common ground, and low voltage pressure on its power switch, the resulted gain is lower than some other topologies. However, in order to reach a higher boost factor, several cells must be linked together in a cascade configuration. This method reduces the overall efficiency.

If a topology provided a high boost-factor with low duty ratio and single-stage conversion, the efficiency is increased. This paper uses this rule to design a new step-up P-type dc/dc converter with high voltage gain in lower duty ratios. The continuous input current, high efficiency, and common ground between the input and the output are other features of this topology. This paper is organized as follows. Detailed analysis is described in Section 2, and the performance of this new topology is compared with other high-gain step-up converters. Simulation and experiment evaluate the performance of this topology, which will be presented in Section 3. Results prove the proposed structure. In Section 4, design considerations are presented. Finally, all achievements are summarised in Section 5.

FIGURE 2 Different P-type step-up converters. (a) Proposed topology presented in [36]. (b) P-type cell with a coupled inductor. (c) Extended P-type boost converter

FIGURE 3 The proposed P-type boost converter

FIGURE 4 Switching modes of the proposed converter. (a) Mode 1. (b) Mode 2
TABLE 2 The converter specifications

| Parameters             | In simulation          |
|------------------------|------------------------|
| Input voltage          | 4.8 V                  |
| Output voltage         | 60 V                   |
| Output power           | 60 W                   |
| Switching frequency    | 20 kHz                 |
| The inductance of $L_1$, $L_2$, and $L_4$ | 50 $\mu$H, 50 $\mu$H, 1 mH |
| Capacitance of $C_1$-$C_4$ | 1000 $\mu$F       |
| Turns ratio            | 1.1                    |
| Power diodes           | SB560 and MUR460       |
| Power switches         | IRFP250                |
| Duty cycle             | About 42%              |
| Core size              | EER2834                |

2 | PRINCIPLE OF THE IMPROVED P-TYPE STEP-UP CONVERTER

Figure 2(a) shows a P-type-based step-up converter, which was presented by Mohammadi et al. [36]. The P-type cell has been highlighted in blue. Figure 2(b) shows another P-type cell with a coupled inductor; Figure 2(c) represents the extended version of this P-type converter. The significant difference between these three circuits is the maximum achievable voltage gain and the number of components. Adding a coupled inductor to the basic cell as shown in Figure 2(a) increases the gain value to \( \frac{2 + \pi}{1 - \pi} \), where \( \pi \) and \( D \) denote the turns-ratio of the coupled inductor and the duty cycle of the power switch, respectively.

Figure 3 represents the proposed P-type-based boost converter. A P-type cell with a coupled inductor has been used. This
structure provides high gain. This circuit includes two power switches, five fast diodes, three capacitors, and three inductors. There are two switching events in each switching interval, which are explained in the following sections.

2.1 Mode 1: \( t = [0 \ t_{on}] \)

In this state, \( Q_1 \) and \( Q_2 \) are turned on. Hence, diodes \( D_1, D_2, \) and \( D_3 \) are turned off, and diodes \( D_3 \) and \( D_4 \) are on. Figure 4(a) illustrates the corresponding current paths. The following equations are obtained from Figure 4(a). The voltage drop of diodes and switches and the series resistance of inductors and capacitors can be neglected if components are assumed to be ideal.

\[
\begin{align*}
v_{L1} &= V_i \\
v_{L2} &= V_{C1} - V_{IK2} = V_{C3} - V_{C2} - v_{L3} - V_{IK2} \\
v_{L3} &= n v_{L2} = \frac{n_1}{n_2} v_{L2} \\
v_{LA} &= V_{C3}
\end{align*}
\]
Figure 9 Simulation results. (a) Inductors voltage. (b) The voltage stress on power diodes

\[
i_{C4} = -I_o \tag{8}
\]

\[
i_i = i_{i1} \tag{9}
\]

where \(v_{L1}, v_{L2}, v_{L3}, v_{L4}\), and \(V_{LK2}\) indicate the instantaneous values of inductor voltage and the leakage inductance, \(i_{L1}, i_{L2}, i_{L3}\), and \(i_{LA}\) refer to the values of inductor current, and \(i_{C1}, i_{C2}, i_{C3}\) and \(i_{C4}\) denote the instantaneous values of capacitor current. Besides, \(V_{C1}, V_{C2}, V_{C3}\) and \(V_{C4}\) show the voltages of capacitors. The \(i_i\) is the input current, the “\(n\)” is the turns ratio of the coupled inductor, that is \(\frac{n_1}{n_2}\), \(V_i\) is the input voltage, and \(I_o\) is the load current.

2.2 Mode 2: \(t = [t_{on} T_s]\)

In this mode, \(Q_1\) and \(Q_2\) are turned off. As a result, \(D_1, D_2,\) and \(D_5\) conduct the current, and \(D_3\) and \(D_4\) are turned off, as shown in Figure 4(b). The following equations are obtained:

\[
v_{L3} = V_i - V_{C1} \tag{10}
\]

\[
v_{L2} = V_{C1} - V_{C2} - v_{L3} - V_{LK2} \tag{11}
\]
**FIGURE 11** Part of experimental results. (a) The input voltage, the output voltage, and the duty cycle. (b) The voltage stress on $Q_1$. (c) The voltage stress on $Q_2$. (d) The stress on $D_1$ and $D_3$ (left), the stress on $D_2$ and $D_3$ (mid), and the input current (right).

**FIGURE 12** Part of the experimental results. (a) The voltage of capacitors $C_1$ and $C_3$. (b) The voltage of capacitor $C_2$.

**FIGURE 13** Part of experimental results. (a) The voltage of $L_1$. (b) The voltage of the coupled inductor $L_2$. (c) The voltage of inductor $L_4$. 
### Table 3: Comparative analysis between the proposed power converter and others

| Refs. | Topology | Components | Voltage gain | Efficiency | Max. duty cycle | Input current | Common ground | Power flow modes |
|-------|----------|------------|--------------|------------|----------------|--------------|---------------|-----------------|
| [36]  |          | Two diodes | \( \frac{2-D}{1-D} \) | 90.5%      | 1 CCM          | √            | U1            |                 |
| [14]  |          | Five diodes| \( \frac{2+D}{1-2D} \) | 90.1%      | 0.5 CCM        | ×            | U            |                 |
| [37]  |          | One diode  | \( \frac{1+D}{1-D} \) | 91.7%      | 1 CCM          | ×            | U            |                 |
| [3]   |          | Zero diode | \( \frac{1+D}{1-D} \) | 96%        | 1 CCM          | √            | B1            |                 |
| [35]  |          | Five diodes| \( \frac{u^2-D}{(1-D)^2} \) | 94%        | 1 CCM          | ×            | U            |                 |
| [8]   |          | Six diodes | \( \frac{1+D}{1-3D} \) | 94%        | 0.33 CCM       | ×            | U            |                 |
| [34]  |          | Five diodes| \( \frac{3+2a}{1-D} \) | 95%        | 1 CCM          | √            | U            |                 |
| [18]  |          | Three diodes| \( \frac{3+2a}{1-D} \) | 95%        | 1 CCM          | √            | U            |                 |

(Continues)
TABLE 3 (Continued)

| Refs. | Topology | Components | Voltage gain | Efficiency | Max. duty cycle | Input current | Common ground | Power Flow modes |
|-------|----------|------------|--------------|------------|---------------|--------------|---------------|----------------|
| Proposed | Five diodes Two switches Four capacitors One inductor One coupled inductor | $\frac{2k-D}{(1-D)^2}$ | 94.76% | 1 | CCM | √ | U |

Abbreviations: U = uni-directional; B = bi-directional.

FIGURE 14 Efficiency variations vs output load. (a) The efficiency of the proposed converter. (b) The simulated converter efficiency for $V_i = 72$ V, $V_o = 350$ V, and $P_{nominal} = 600$ W. (c) The simulated converter efficiency for $V_i = 72$ V, $V_o = 350$ V, and $P_{nominal} = 1$ kW.

2.3 Calculating the ideal voltage gain function

Modes 1 and 2 are begun and finished during the intervals $[0, \tau_{on}]$ and $[\tau_{on}, T_s]$, respectively, where $\tau_{on}$ is the power switch on-time, and $T_s$ is the switching period. The effect of these events on the voltage and current of handled components is illustrated in Figure 5.

Equations (18) and (19) represent volt-second and coulomb-second identities. By applying these rules to (1)–(17) and neglecting the leakage inductance due to its small value, the average value of inductor voltage and capacitor current can be deduced. Equation (26) confirms that the input current is continuous, and as a result, this converter operates in continuous current mode (CCM):

\[
\langle v \rangle = \frac{1}{T_s} \int_0^{D T_s} v(t) \, dt + \frac{1}{T_s} \int_{D T_s}^{T_s} v(t) \, dt
\]
\[ \langle \dot{i} \rangle = \frac{1}{T_i} \int_0^{T_i} \dot{i}(t) \, dt + \frac{1}{T_i} \int_0^{T_i} i(t) \, dt \]  

\[ \langle v_{L1} \rangle = V_i - (1 - D) V_{C1} \]  

\[ \langle v_{L2} \rangle = \frac{1 + n D}{1 + n} V_{C1} - \frac{1 - D}{1 + n} V_{C2} \]  

\[ \langle v_{LA} \rangle = V_{C3} - (1 - D) V_o \]  

\[ \langle i_C1 \rangle = \frac{n \cdot (1 + n)}{n} I_{L2} - \frac{1 - D}{n} I_{L2} + (1 - D) I_{L1} \]  

\[ \langle i_C2 \rangle = D I_{L3} - I_{LA} \]  

\[ \langle i_C4 \rangle = D I_{LA} - I_O \]  

\[ \langle i_L \rangle = I_i = I_{L1} \]  

where \( I_{L1}, I_{L2}, I_{L3}, \) and \( I_{LA} \) indicate the average values of inductor current, and \( D \) and \( V_o \) indicate the duty ratio and output voltage, respectively. According to the volt-second balance theory, the average value of the inductor voltage is zero in every switching interval. Therefore, the following identities are determined:

\[ V_{C1} = \frac{V_i}{1 - D} \]  

\[ V_{C2} = \frac{1 + n D}{1 - D} V_{C1} = \frac{(1 + n D)}{(1 - D)^2} V_i \]  

\[ V_{C3} = \frac{2 + n - D}{(1 - D)^2} V_i \]  

Equations (27)–(29) identify the voltage of capacitors. Furthermore, capacitor \( C_4 \) is exposed to the output voltage. Therefore, \( V_{C4} = V_o \). From (30), the value of output voltage gain is obtained. Accordingly, the maximum allowable duty cycle is one.

\[ G(n, D) = \frac{V_o}{V_i} = \frac{2 + n - D}{(1 - D)^2} \]  

Figure 6(a) shows the voltage gain characteristics of the proposed converter. Figure 6(b) and (c) compares the gain of the proposed topology with those presented in Figure 2(a)–(c). Additionally, the discontinuous current mode (DCM) operation has been demonstrated in Figure 5(b). According to the voltage waveforms of inductors and (18), the following expressions can be obtained:

\[ V_{C1} = \frac{D + D_2}{D_2} V_i \]  

\[ V_{C2} = \frac{(1 + n) D + D_2}{D_2} V_{C1} \]  

\[ V_{C3} = \frac{D + 2 D_2}{D} V_{C2} = \frac{D_2}{D} V_{C1} \]  

\[ V_o = \frac{D + D_2}{D_2} V_{C3} \]
Table 4: List of advantages and disadvantages for the proposed topology and others

| Topology | Advantages | Disadvantages |
|----------|------------|---------------|
| [36]     | Low number of required components CCM operation Common ground Unlimited maximum duty cycle | Low efficiency Low output voltage gain Need to operate with higher duty cycles |
| [14]     | CCM operation | High number of required components Low efficiency Low output voltage gain Need to operate with higher duty cycles No common ground Limited maximum duty cycle |
| [37]     | Low number of required components CCM operation Unlimited maximum duty cycle | Low efficiency Low output voltage gain Need to operate with higher duty cycles No common ground |
| [3]      | Low number of required components CCM operation Unlimited maximum duty cycle Common ground High efficiency | Low output voltage gain Need to operate with higher duty cycles |
| [35]     | CCM operation Unlimited maximum duty cycle High efficiency | High number of required components Low output voltage gain Need to operate with higher duty cycles No common ground |
| [8]      | CCM operation High efficiency | High number of required components Low output voltage gain Need to operate with higher duty cycles Limited maximum duty cycle No common ground |
| [34]     | CCM operation Unlimited maximum duty cycle High efficiency Common ground | High number of required components Low output voltage gain Need to operate with higher duty cycles |
| [18]     | CCM operation Unlimited maximum duty cycle High efficiency Common ground | High number of required components Low output voltage gain Need to operate with higher duty cycles |
| Proposed | High voltage gain Need to operate with lower duty cycles CCM operation Unlimited maximum duty cycle High efficiency Common ground | High number of required components |

Also, by calculating the average value of $I_{D_s}$, the relation between $D_s$ and other parameters can be found as follows:

$$D_s = \frac{V_o}{V_{C3}} \left( \frac{2L_s}{R_{L_s} D T_s} \right)$$  \hspace{1cm} (36)

where $D_s$ is the off-time duty ratio. This paper only focuses on the CCM operation due to the need for the continuous input current. In theory, this topology provides better voltage gain even with lower duty ratios. The extended P-type boost converter shown in Figure 2(c) requires more P-type cells to provide a higher gain that needs more components. Therefore, the implementation cost increases significantly. However, in the proposed topology, higher gains are achievable only by increasing the turns ratio of the coupled inductor.

### 2.4 Calculating the current and voltage of components

The coulomb-second balance theory indicates that the average value of the capacitor current is equal to zero in each switching interval. By applying this principle to (23)–(25), the average value of inductors current is calculated as follows:

$$I_{L_2} = \frac{n (1 - D)}{1 + \frac{n}{D}} I_{L_1}$$ \hspace{1cm} (37)

$$I_{L_3} = \frac{I_{L_A}}{D} = \frac{I_o}{D^2}$$ \hspace{1cm} (38)

$$I_{L_A} = D I_{L_3} = \frac{I_o}{D}$$ \hspace{1cm} (39)

On the basis of the basic equations for capacitor voltage ($i_C = C_\frac{\Delta V_C}{\Delta t}$), the voltage ripple values of capacitors are deduced.

$$\Delta V_{C1} = \frac{(1+n) I_{L_2} D T_s}{C_1}$$ \hspace{1cm} (40)

$$\Delta V_{C2} = \frac{I_o T_s}{D C_2}$$ \hspace{1cm} (41)

$$\Delta V_{C3} = \frac{(1-D) I_o T_s}{D C_3}$$ \hspace{1cm} (42)

$$\Delta V_{C4} = \frac{I_o D T_s}{C_4}$$ \hspace{1cm} (43)

Similarly, $V_L = \frac{I L}{\Delta t}$ specifies the relation between inductor voltage and current. Consequently, (44)–(47) are determined.

$$\Delta I_{L_1} = \frac{V_s D T_s}{L_1}$$ \hspace{1cm} (44)
\[ \Delta I_{L2} = \frac{V_i D T_i}{L_2 (1 - D)} \]  
\[ \Delta I_{L3} = \frac{V_i n D T_i}{(1 - D) L_3} \]  
\[ \Delta I_{LA} = \frac{(2 + n - D) V_i D T_i}{L_4 (1 - D)^2} \].

### 2.5 Voltage stresses on semiconductors

During state 1, as displayed in Figure 4(a), diodes $D_1$, $D_2$, and $D_3$ are in reverse bias condition. $D_1$ is exposed to the voltage of $C_1$, $D_2$ must tolerate $V_{C2} + V_{L3}$, and $D_3$ is exposed to the output voltage. During state 2, as shown in Figure 4(b), diodes $D_3$ and $D_4$ and switches $Q_1$ and $Q_2$ are off. $D_3$ must tolerate ($V_{C3} - V_{C1}$) during its off-state, and $D_4$ meets ($V_\phi - V_{C1}$). The voltage stress on these components is listed in Table 1.

### 2.6 Converter model considering the voltage drop of diodes and power switches

In applications where the input voltage is low, neglecting the voltage drop of diodes and power switches is impossible. Consequently, the abovementioned equations are accounted for ideal conditions, and relations must be reformulated, considering the voltage drop of diodes and power switches. This section deals with this case. It is assumed that $V_D$ and $V_{on}$ denote the voltage drop of diodes and power switches, respectively. As a result, (1)–(4) and (10)–(12) change with the following format:

\[ v_{l1} = \begin{cases} 
V_i - V_D - V_{on} & \text{for } [0 \ t_{on}] \\
V_i - V_D - V_{C1} & \text{for } [t_{on} \ T]
\end{cases} \]  
\[ v_{l2} = \begin{cases} 
\frac{V_{C1} - V_{on}}{1 + n} & \text{for } [0 \ t_{on}] \\
\frac{V_{C1} - V_D - V_{C2}}{1 + n} & \text{for } [t_{on} \ T]
\end{cases} \]  
\[ v_{l3} = \begin{cases} 
n V_{l2} & \text{for } [0 \ t_{on}] \\
 V_{l2} & \text{for } [t_{on} \ T]
\end{cases} \]  
\[ v_{LA} = \begin{cases} 
V_{C3} - V_{on} & \text{for } [0 \ t_{on}] \\
V_{C3} - V_D - V_\phi & \text{for } [t_{on} \ T]
\end{cases} \]

By applying (18) and (19) to (48)–(51), the following relations are derived:

\[ V_{C1} = \frac{V_i - V_D - D V_{on}}{1 - D} \]  
\[ V_{C2} = \frac{(1 + nD) V_{C1} - (1 + D) D V_{on} - (1 - D) V_D}{1 - D} \]  
\[ V_{C3} = \frac{V_{C2} - (1 - D) V_{C1} - (2D - 1) V_D}{D} \]  
\[ V_\phi = \frac{V_{C3} - D V_{on} - (1 - D) V_D}{1 - D} \]

Figure 7(a) shows the voltage gain characteristic and the voltage of capacitors for $V_D = 0.6$, $V_{on} = 1$, $n = 1.1$, and $V_i = 4.8$ V with different duty cycles. Also, the voltage gain has been drawn for $V_D = 0.6$, $V_{on} = 1$, $n = 2.25$, and $V_i = 10$ V with different duty cycles. Figure 7(b) shows the voltage of each capacitor for different duty ratios for $V_D = 0.6$, $V_{on} = 1$, $n = 1.1$, and $V_i = 4.8$ V. Figure 7(a) and (b) will be validated by simulation and experiments in Section 3.

### 2.7 Small-signal model

It is possible to use (20)–(26) in order to find the small-signal model of this topology. By adding a small-signal variable to all parameters (e.g. $\hat{x} = x + \delta x$) and linearising the resulting equations, the following relations can be obtained:

\[ L_1 \hat{i}_{L1} = \hat{V}_i - (1 - D) n \hat{v}_{C1} + V_{C1} \hat{d} \]  
\[ L_2 \hat{i}_{L2} = \left( \frac{1 + nD}{1 + n} \right) \hat{v}_{C1} - \left( \frac{1 - D}{1 + n} \right) \hat{v}_{C2} + \left( \frac{n V_{C1} + V_{C2}}{1 + n} \right) \hat{d} \]  
\[ L_3 \hat{i}_{L3} = n \left( \frac{1 + nD}{1 + n} \right) \hat{v}_{C1} - \hat{v}_{C2} + \hat{d} \left( \frac{n V_{C1} + V_{C2}}{1 + n} \right) \]  
\[ L_4 \hat{i}_{LA} = \hat{v}_{C3} - (1 - D) n \hat{v}_{C4} + V_\phi \hat{d} \]  
\[ C_1 \hat{v}_{C1} = (1 - D) \hat{v}_{L1} + \left( \frac{2 - n}{n} \right) \hat{v}_{L2} + \left( \frac{2 - n}{n} I_{L2} - I_{L1} \right) \hat{d} \]  
\[ C_2 \hat{v}_{C2} = \left( \frac{1 - D}{n} \right) \hat{v}_{L2} + D \hat{v}_{L3} + \left( I_{L3} - \frac{I_{L2}}{n} \right) \hat{d} \]
\[ C_3 \mathbf{v}_{C_3} = -D \mathbf{i}_{L_3} - \mathbf{i}_{lA} - i_{L_A d} \]  \hspace{1cm} (62)
\[ C_4 \mathbf{v}_{C_4} = D \mathbf{i}_{lA} + i_{L_A d} - \frac{\mathbf{v}_O}{R_{L}}. \]  \hspace{1cm} (63)

From (56)–(63), the small-signal equations can be formulated in the state-space form, as shown in (64) and (65).

### 3 RESULTS AND ANALYSIS

#### 3.1 Simulation results

Simulations have been done by MATLAB/Simulink software. Table 2 shows the specifications of the proposed converter. Figure 8 displays part of simulation results, including the input and output voltages, the voltage of capacitors, input current, and voltage stress on each power switch. According to Figure 8(a), the output voltage follows the expected value (60 V). As a result, the output voltage gain is 12.5. According to Figure 7(a), if the duty cycle is adjusted to 42%, then the converter reaches a gain of about 12.5. Therefore, the theoretical gain is confirmed by Figure 8(a). Figure 8(b) shows the voltage of each capacitor. This result validates Figure 7(b). Figure 8(c) represents the input current and the voltage stress on power switches.

\[
\begin{bmatrix}
0 & 0 & 0 & 0 & \frac{-1}{1-D} & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & \frac{1}{1-D} & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & \frac{1}{1-D} & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{1-D} & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{1-D}
\end{bmatrix}
\]

\[
\begin{bmatrix}
\frac{1}{L_4} & \frac{V_{C_1} - 1}{L_4} & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & \frac{1}{L_3} & \frac{V_{C_2}}{L_3} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & \frac{1}{L_2} & \frac{V_{C_1}}{L_2} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & \frac{1}{L_1} & \frac{V_{C_2}}{L_1} & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & \frac{1}{L_3} & \frac{V_{C_1}}{L_3} & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & \frac{1}{L_4} & \frac{V_{C_2}}{L_4} & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{L_2} & \frac{V_{C_2}}{L_2} \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 1
\end{bmatrix}
\]

\[
\mathbf{v}_O = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix}
\hat{i}_{L_1} & \hat{i}_{L_2} & \hat{i}_{L_A} & \hat{v}_{C_1} & \hat{v}_{C_2} & \hat{v}_{C_3} & \hat{v}_{C_4}
\end{bmatrix}^T
\]

The input current varies continuously. Therefore, the proposed converter operates in CCM. On the basis of the applied duty cycle and Table 1, the voltage stress on \( V_{Q1} \) and \( V_{Q2} \) are equalised to 14 V and 60 V, respectively; Figure 8(c) affirms these values. Figure 9 presents other relevant waveforms, which are composed of the voltage of inductors and the voltage stress on power diodes. Since the voltage of inductors has never been zero, the inductors current is continuous, as shown in Figure 9(a). The results of voltage stresses on power diodes also authenticate the summary presented in Table 1.

#### 3.2 Experimental results

Figure 10 shows the experimental prototype and its components. This circuit has the same elements and values as simulated topology. Generating pulse width modulated (PWM) signal is essential for driving power switches, which has been done by a simple PWM generator IC TL494. Results are captured by using a GWInstek GDS-2074 oscilloscope.

Figure 11(a) shows the output voltage, the input voltage, and the applied PWM simultaneously. The output voltage is 60 V, when the duty cycle is adjusted to 42%. As a result, the voltage gain is 12.5, which confirms the simulation result and the graph presented in Figure 7(a). Figure 11(b) and (c) represents the amount of voltage stresses on power switches \( Q_1 \) and \( Q_2 \), which are about 13 V and 60 V, respectively, and as can be seen, these values are identical to simulation and theoretical values. Furthermore, Figure 11(d) exhibits the voltage stresses on power diodes. Each diode has a voltage drop of 0.8 V when it is on. Figure 11(d) shows the input current waveform. It confirms that this circuit works in CCM. Figure 12(a) and (b) shows the voltage of capacitors, which are 7 V, 19 V, and 32 V.

Also, these values are identical to the values shown in Figure 8(b). Figure 13 illustrates waveforms of inductors voltage. Since they are changing in CCM, their currents also change continuously. The voltage amplitude of inductors validates values depicted in Figure 9(a). Figure 14(a) shows the converter efficiency curve, respectively. The efficiency curve has been obtained for different output loads. The maximum achievable efficiency for this proposed topology is 94.76%. The proposed efficiency curve is obtained by experimental results. Figure 14(a) includes the overall efficiency, the converter efficiency, and the simulation results for the converter efficiency. The overall loss incorporates the efficiency of the proposed converter plus the control unit, sensors, and gate drivers. The efficiency has been calculated by using \( P_{out}/P_i \) ratio. According to Figure 14(a), at point (1), the converter works under no-load condition. The control loss is equal to 0.1 W, and the converter loss is about 0.159 W. Because the converter operates under no-load condition, the converter loss corresponds only to the switching losses. The converter efficiency is equal to 86.25%. However, due to above-mentioned existing losses, the total efficiency is reduced...
to 79.4%. This efficiency value can be compensated by choosing a lower loss control unit. It should be noted that the main scope of this article is to propose a novel topology. Therefore, the loss of the control unit has not been considered. At point (2), the output power is increased to 10 W. Therefore, the converter loss is also increased to 1.4 W due to adding conduction, core and copper losses to the proposed converter. The control loss is constant (0.15 W). At point (3), as illustrated in Figure 14, the maximum efficiency is occurred, in which the nominal output power is drawn. Figure 14(a) displays simulated efficiency. It confirms the experimental efficiency curve of the presented new topology. According to point (3), the maximum converter loss is 5% of the output power. Figure 14(b) and (c) shows the converter efficiency for different voltage and power ratings.

3.3 | Comparative analysis

Many step-up topologies have been presented, providing high gain, low stresses, continuous input current, bidirectional power flow, common ground etc. Of those structures, some topologies have been compared with the proposed step-up converter. Table 3 compares them in terms of the number of power switches, the number of inductive and capacitive components, the voltage gain, and some other features. Figure 15 compares the proposed converter with other references in terms of voltage gain under the same condition. In the proposed topology, small duty ratios produce medium gains, whereas intermediate duty cycles provide high gain. The best duty cycle for this switching converter is laid between 0.25 and 0.5, which produces higher voltage gains than others. In addition, unlike some topologies, the maximum duty cycle is limited to 1, which makes this converter appropriate for a wide input voltage range.

As an instance, the converter presented in [14] has a higher gain than this converter for \( D > 0.42 \). However, its maximum duty ratio is limited to 0.5, and it does not have a common ground. The converter presented in [18] provides better gain for \( D < 0.25 \), but if \( \eta \) is set to lower values, the gain characteristics will be reduced significantly, as illustrated in Figure 15(c). Table 4 mentions the advantages and disadvantages of each structure.

4 | DESIGN CONSIDERATIONS

In order to design the suggested structure, following stages must be considered.

1. First, a suitable duty cycle for a nominal condition of the input and output voltages must be selected. The best value is between 0.2 and 0.6 for better efficiency. In this prototype, the value of \( D \) is selected to be 0.4 for good efficiency.
2. By using (31), the proper value for \( \eta \) is determined, which in this example is identical to 1.1.
3. By using (37)–(39), the average value of inductors current is obtained.
4. By using (44)–(47) and choosing the right current ripple value for inductors, the value of inductances can be deduced. The right value for the current ripple in CCM operation is between 20% and 40% of the average inductor current.
5. Similar to stage 4, the capacitance value of capacitors can be estimated using (40)–(43). The best ripple value for capacitors is lower than 120 mVpp.

5 | CONCLUSION

This paper proposes a new step-up dc/dc converter based on an improved P-type step-up cell. It comprises five diodes, two switches, four capacitors, two inductors, and one coupled inductor. The proposed structure reaches to high gain with this configuration. In theory, it was demonstrated that this converter performs better gain characteristics than many other boost topologies. Operating principle of the suggested topology was explained in detail. Simulation and experimental results were shown to assess the performance of this novel topology. Results and the comparative analysis validate this step-up topology. As indicated, this converter provides high voltage gain, continuous input current, high efficiency (94.76%), and common ground between the input and the output.

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