Block-Parallel Systolic-Array Architecture for 2-D NTT-based Fragile Watermark Embedding

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Abstract

Number-theoretic transforms (NTTs) have been applied in the fragile watermarking of digital images. A block-parallel systolic-array architecture is proposed for watermarking based on the 2-D special Hartley NTT (HNTT). The proposed core employs two 2-D special HNTT hardware cores, each using digital arithmetic over GF(3), and processes $4 \times 4$ blocks of pixels in parallel every clock cycle. Prototypes are operational on a Xilinx Sx35-10f868 FPGA device. The maximum estimated throughput of the FPGA circuit is 100 million $4 \times 4$ HNTT fragile watermarked blocks per second, when clocked at 100 MHz. Potential applications exist in high-traffic back-end servers dealing with large amounts of protected digital images requiring authentication, in remote-sensing for high-security surveillance applications, in real-time video processing of information of a sensitive nature or matters of national security, in video/photographic content management of corporate clients, in authenticating multimedia for the entertainment industry, in the authentication of electronic evidence material, and in real-time news streaming.

Keywords

Fragile watermarking, number-theoretic transforms

1 Introduction

Fragile watermarking is an authentication technique that can detect and localize all possible types of modifications in images including, but not limited to, nonlinear distortion, linear filtering, intensity/contrast changes, zooming, and lossy compression of digital two-dimensional (2-D) signals. It finds applications in copyright protection, high-security biometric image processing [2,19,21], digital content management, and Internet-based streaming video [25]. These scenarios are subject to electronic attacks, leading to an increasing demand for authentication. Application-specific VLSI hardware for error-free high-speed real-time fragile watermarking of large datasets is an emerging requirement in the information security industry [15].

In [23,24], fragile watermarking techniques were given a number-theoretic transform (NTT) approach. Unlike fixed-point fragile watermarking schemes based on conventional discrete transforms [17], systems derived from NTTs do not introduce round-off or truncation errors, since they are capable of exact computation. This property stems from the fact that all arithmetic computations are performed in a finite field. This is a highly desirable feature for practical applications [16].

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In this work, we propose an architecture for the real-time computation of the $4 \times 4$ special Hartley NTT (HNTT)\cite{9}. The special HNTT is the finite field version of the special discrete Hartley transform (DHT)\cite{5,12,26}.

Furthermore, employing the introduced 2-D special HNTT core, an efficient architecture for the fragile watermarking scheme by Tamori et al.\cite{23} is also proposed.

It is important to note that number-theoretic transforms have no physical meaning, unlike the well-known conventional trigonometric transforms. The lack of a physical meaning and concept of energy make the transform coefficients extremely sensitive to error, thereby making the NTT useful for fragile watermarking schemes. This high sensitivity to error is a highly-desirable property for fragile watermarking as it guarantees complete destruction of the embedded watermark when the watermarked image is tampered-with.

The HNTT uses exact integer arithmetic, whereas usual DHT architectures require floating point arithmetic.

For completeness, we provide a brief review of the available DHT architectures based on systolic-array VLSI circuits that employ conventional DHT transforms. Unlike the HNTT framework, DHT architectures suffer from finite precision effects. Mainly represented by truncation and rounding-off, finite precision issues lead to performance and signal-to-noise ratios that depend on the employed fixed-point precisions of the systolic-array processor.

This paper unfolds as follows. In Section 2, we furnish the necessary number-theoretic results to construct a low-complexity special HNTT. Section 3 offers a detailed account of the implementation issues of the proposed hardware design. The resulting output measurements from the designed circuitry are also reported in several realistic test scenarios. The paper is concluded in Section 4.

2 Review and Mathematical Background

2.1 Conventional DHT Systolic-Array VLSI Architectures

The proposed systolic-array architecture is the first, and the only currently available VLSI architecture for both the 2-D HNTT and the Tamori fragile watermarking scheme\cite{23}. However, we do provide a brief summary of available VLSI architectures so that the reader is familiar with the current state-of-the-art in VLSI DHT architectures based on systolic-arrays although none of the architectures reviewed here are for the HNTT.

The $N$-point conventional DHT relates two discrete signals $v_n$, $n = 0, 1, \ldots, N - 1$, and $V_k$, $k = 0, 1, \ldots, N - 1$, with real components according to

$$V_k = \sum_{n=0}^{N-1} v_n \text{cas} \left( \frac{2\pi kn}{N} \right), \quad k = 0, 1, \ldots, N - 1,$$

where $\text{cas}(x) = \cos(x) + \sin(x)$ is the Hartley function. Real-time high-speed signal and image processing algorithms employing the DHT achieve high-speed computations using massively-parallel VLSI arrays.

A VLSI systolic-array design for the 1-D DHT of any length using cyclic convolution requiring ROM based digital arithmetic is available in\cite{13}. Systolic-arrays are modular, regular, and locally interconnected, making them very suitable for high-throughput fast algorithms. In\cite{4}, a DHT is calculated using a VLSI block for the Fermat number transform and its inverse\cite{1}, at lower multiplier complexity using shift and add operations.
based on the algorithm derived in [3].

In [6], an algorithm for calculating the DFT is extended to a class of discrete trigonometric transforms and a VLSI architecture that is capable of real-time calculation of such transforms is presented. This architecture could provide local interconnections, identical processing elements in the systolic-array architecture and minimal control complexity [6].

An application-specific VLSI architecture for the parallel calculation of the decimation in time and radix-2 fast Hartley transform (FHT) is available in [27], where a modular and regular parallel architecture based on a constant geometry algorithm using butterflies of four data items and permutations is employed. This resulted in the mapping of the algorithm to simplified VLSI circuits and reduced communications among processors [27].

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An efficient design of a VLSI systolic-array for a prime-length type III generalized DHT is available in [7]. The design employs an appropriate decomposition of the generalized DHT into two half-length circular correlation structures having the same length and form. Such structure can be concurrently computed and implemented on a systolic array using hardware sharing. A substantial increase in computational throughput using a simplified control structure and low hardware complexity was achieved, together with low I/O and for low hardware cost [7].

An algorithm for computing the DHT using an algebraic integers encoding scheme for the coefficients is available in [11]. An associate fully pipelined systolic architecture with $O(N)$ throughput is available [11].

A systolic-array processor for the prime-factor DHT is given in [18]. In [10], a systolic-array architecture for the fast computation of the 2-D DHT of size $M \times N$ in $O(M + N)$ time using Givens rotors as processing elements is provided [10]. In critical applications, fault detection of these VLSI circuits is also required. A self-checking array architecture for the radix-2 FHT transform is available in [22] where it is shown that algorithm-based error detection schemes for FHT can be realized with reasonable hardware and time overheads.

### 2.2 1-D and 2-D HNTT

Despite the achievements on DHT implementation, the DHT is inherently a transformation defined over the real numbers. Thus, it is naturally prone to truncation and round-off errors. A truly error-free transform should work on a numerical framework where the concept of error or approximation is inexistent. Galois field theory offers an adequate algebraic formalism for such framework [1].

Let $\text{GF}(p)$ be a Galois field of odd characteristic $p$. An integer $a$ is said to be a quadratic nonresidue of $p$ if the congruence $x^2 \equiv a \mod p$ has no solution [14, p. 68]. If $p \equiv 3 \mod 4$, then the element $-1$ is a quadratic nonresidue. Therefore, the associated Gaussian integer field can be defined as $\text{GI}(p) = \{a + jb : a, b \in \text{GF}(p)\}$, where $j^2 \equiv -1 \mod 4$. An element $a + jb \in \text{GI}(p)$ is said to be unimodular if $a^2 + b^2 \equiv 1 \mod p$. The finite field Hartley function is analogous to its real field counterpart and is given by

$$\text{cas}(i) \triangleq \cos(i) + \sin(i), \quad i = 0, 1, \ldots, N - 1,$$

where the finite field cosine and sine functions are

$$\cos(i) = \frac{\zeta^i + \zeta^{-i}}{2}, \quad \sin(i) = \frac{\zeta^i - \zeta^{-i}}{2j},$$

where $\zeta$ is a primitive $N$-th root of unity.
respectively, and $\zeta \in \text{GI}(p)$ is a fixed element of order $N$. In addition, if $\zeta$ is a unimodular element, then $\text{cas}(i) \in \text{GF}(p)$, $i = 0, 1, \ldots, N - 1$ [9].

If a unimodular $\zeta$ element is selected, then the 1-D HNTT relates input and output vectors, $x = \begin{bmatrix} x_0 & x_1 & \cdots & x_{N-1} \end{bmatrix}^T$ and $X = \begin{bmatrix} X_0 & X_1 & \cdots & X_{N-1} \end{bmatrix}^T$, respectively, according to the following pair of relations:

$$X = H_N \cdot x,$$
$$x = N^{-1} \mod p \cdot H_N \cdot X,$$

where $H_N$ is the transformation matrix, whose elements are given by $[H_N]_{i,k} = \text{cas}(ik)$, $i, k = 0, 1, \ldots, N - 1$. The unimodularity of $\zeta$ ensures that if $x_i \in \text{GF}(p)$, for all $i$, then $X_k \in \text{GF}(p)$, for all $k$ [9]. Quantities $\zeta$, $p$, and $N$ are not independent.

Among several possible choices of $\zeta$, $p$, and $N$, we adopted $\zeta = j$, $p = 3$, which implies $N = 4$. This combination of Galois field characteristic, blocklength size and $\zeta$ element under the HNTT formalism advances the existing techniques in several ways.

Firstly, whereas the method described in [23] employs the standard Fourier-like NTT, our approach employs the HNTT. For this particular transform, the above selected parameters furnishes a particularly interesting transformation matrix:

$$H_4 = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & 2 & 2 \\ 1 & 2 & 1 & 2 \\ 1 & 2 & 2 & 1 \end{bmatrix} \equiv \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & 1 & -1 \\ 1 & -1 & -1 & 1 \end{bmatrix} \mod 3,$$

since $2 \equiv -1 \mod 3$. In comparison, the Fourier-like NTT approach described in [23] requires a transformation matrix filled at best with powers of two. Our design is computationally simpler: it minimally requires only additions and subtractions, being multiplication-free in nature.

Secondly, the HNTT can provide a symmetrical transform operation. This is because the forward transform matrix is identical to the inverse transform matrix. Among the trigonometric based transforms, the Hartley transform is unique in this aspect [5]. This implies that the hardware design for the forward transform can be re-used for the inverse transform.

Thirdly, in our mathematical setup, even the usual scaling factor $N^{-1}$ present in the inverse transformation could be eliminated. This is possible due to the fact that, for the chosen Galois field, we have that $N^{-1}$ is congruent to one: $N^{-1} \equiv 4^{-1} \equiv 1 \mod 3$.

A possible drawback to this approach would be the cumbersome 2-D HNTT framework, inherited from the 2-D DHT formalism [5]. Indeed, given a $4 \times 4$ matrix $A$, its 2-D HNTT transform is furnished by [9]:

$$\frac{1}{2}(B + B^{(c)} + B^{(r)} - B^{(cr)}),$$

where

$$B = H_4 \cdot A \cdot H_4,$$
and $B^{(c)}$, $B^{(r)}$, and $B^{(cr)}$ are built from the temporary matrix $B$. Their elements are respectively given by $t_{i,N-j} \pmod{N}$, $t_{N-i} \pmod{N}$, and $t_{N-i,N-j} \pmod{N}$, where $t_{i,j}$ are the elements of $B$, for $i, j = 0, \ldots, N-1$. Above mathematical description stems from the properties of the csa function [5, p. 21]. It is excessively computationally complex, being unattractive for the goals of this paper.

However, for our purposes, there is no point in calculating the actual 2-D HNTT. In fact, the lack of physical meaning of the NTT spectrum allows us to consider the 2-D special Hartley transform, whose computational complexity is lower. Therefore, we define the 2-D special HNTT of a $4 \times 4$ matrix $A$ as simply equal to $B$.

The expression for $B$ is the core operation of our proposed implementation. It can be understood as multiple applications of the 1-D HNTT to the columns of $A$, and then to the rows of the resulting intermediate calculation. This entire operation can be efficiently performed by means of the fast algorithms as depicted in Fig. 1(a)-(b). By the end we obtained a multiplication-free, totally symmetric, low complexity 2-D NTT.

## 3 Watermarking Implementation and Results

### 3.1 Block-parallel systolic-array fragile watermarking architecture

The proposed architecture employs the 4-point HNTT based on modulo-3 arithmetic. This configuration leads to relatively simple hardware. Our architecture is massively-parallel, fine-grain pipelined, and fully-systolic. It is also modular, regular, and has good local interconnectivity, making it well-suited for application-specific integrated-circuit implementations. We employ fully-parallel building-blocks for implementing the atomic arithmetic operation $c \equiv a + b \pmod{3}$, where $a$, $b$, and $c$ are 2-bits wide, using 4-input look-up tables (LUTs) implemented on random-access memory (RAM).

The watermark embedding step is mathematically detailed in [23]. It consists of the additive blockwise insertion of a given watermark pattern into the NTT domain of the input data blocks. Input $4 \times 4$ 8-bit image
blocks have their pixels \( x_{i,k}, 0 \leq i, k \leq 3 \), decomposed into residue \( r_{i,k} \equiv x_{i,k} \pmod{3} \) and divisible \( d_{i,k} = x_{i,k} - r_{i,k} \) parts. This procedure is achieved by storing precomputed values of \( d_{i,k} \) in a LUT of depth 256. The fully-pipelined architecture computes the 2-D special HNTT (Fig. 1(b)) of incoming residues blocks at each new clock cycle, resulting in number-theoretic transformed residue blocks \( R_{i,k} \).

Then sixteen block-parallel modulo-3 adders are used to insert watermark pixels \( w_{i,k}, 0 \leq i, k \leq 3 \) into NTT domain residue data \( R_{i,k} \). This operation is described according to the following expression:

\[
R'_{i,k} \equiv R_{i,k} + w_{i,k} \pmod{3},
\]

which is submitted to another instantiation of the 2-D special HNTT core. This latter operation is intended to inverse transform \( R'_{i,k} \).

Finally, the resulting inverse transformed data \( r'_{i,k} \) is added to the previously computed divisible part employing 16 parallel 8-bit unsigned binary adders, furnishing the watermarked data

\[
x'_{i,k} = d_{i,k} + r'_{i,k}.
\]

The total throughout of the systolic-array is one \( 4 \times 4 \) block of watermarked samples per clock cycle at a pipelining latency of \( m \) cycles. The design is shown in Fig. 2.

The massively-parallel systolic-array proposed here and shown in Fig. 2 is derived using the NTT-based fragile watermark embedding algorithm detailed in [23]. A direct-form realization is employed, with feed-forward paths subject to fine-grain pipelining for reduced critical path delay and register retiming for lower dynamic power [20]. The systolic-array is a one-to-one mapping of the algorithm.

The IP core was physically implemented on a Xilinx Virtex-4 Sx35-10ff668 FPGA. It consumed 2034 (out of 15360) slices, 3272 (out of 30720) logic fabric LUTs, and 160 (out of 192) FIFO16/RAM16 hardware blocks. Post place-and-route timing analysis indicated a clock speed greater than 100 MHz for \( m = 89 \) stages of internal pipelining. Fig. 3 shows a screen shot of the final FPGA design and physical implementation, which was completed using the bit-true cycle-accurate model-based design and implementation tool called Xilinx System Generator (XSG), which functioned in association to Matlab and Simulink. The XSG could automatically determine the glue-logic required for the connection of the proposed systolic-array watermarking processor to the personal computer memory space via the 32-bit PCI bus.
Figure 3: FPGA circuit design using Xilinx System Generator (XSG) with on-chip physical implementation.
3.2 Simulation

The on-chip digital verification platform based on XSG allowed stepped hardware cosimulation with a parallel software model in MATLAB/Simulink. This facilitated a direct comparison of simulated algorithm outputs with actual measurements from the FPGA implementation under test. An FPGA implementation of the proposed systolic-array for the fragile watermark embedding was successfully verified on-chip using hardware-in-the-loop cosimulation on Xilinx XtremeDSP Development Kit-4 hardware prototyping system.

Streamed 4 × 4 sized test data blocks from the Lena image were submitted to the FPGA chip. The resulting watermarked data from the proposed core was routed back to our computing environment via a PCI slot, for analysis in MATLAB. Fig. 4(a) shows intact and tampered versions of a watermarked subimage of Lena portrait.

The following minimal image perturbations were considered: (i) random changes of the least significant bit of each pixel with probability 10 \(^{-2}\) (top left image); (ii) JPEG compression and decompression with quality factor of 100 (bottom left image); and (iii) JPEG 2000 compression and decompression at 8 bits per pixel (bottom right image). The employed watermark was the same in each case: a regular pattern of pixels.

Watermarks are extracted by taking the modular difference between the special HNTT transformed versions of the original image and the watermarked image. This procedure is detailed in [23]. Obtained watermarks from subimages are shown homologously in Fig. 4(b). Clearly, tampered subimages furnished severely damaged extracted watermarks.

The proposed 2-D fragile watermarking core delivered one 4 × 4 block of watermarked results every clock cycle, implying a video frame rate 95.3 Hz at a resolution of 4096 × 4096, for a clock of 100 MHz.

4 Conclusion

The increasing demand for secure data storage and tamper-free transmission is expected to lead to new applications of high-speed server side hardware algorithms for handling large amounts of data and Internet traffic. In this paper, we proposed, physically implemented, and verified on chip a novel systolic-array processor architecture for high-speed efficient fragile watermarking scheme for images.

The introduced circuitry is based on the number-theoretic algorithm introduced by Tamori et al. in [23]. Our work also introduced the number-theoretic version of the special DHT, which was necessary for the transform-domain watermark embedding. Finite field characteristic and unimodular element selection were tailored to allow a low-complexity implementation without complex arithmetic.

Moreover, the proposed architecture is the only one of its kind available in the current literature and is capable of embedding 100 million 4 × 4 image blocks per second, in real-time, when implemented on a mid-capacity Xilinx Virtex-4 FPGA device.

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Figure 4: (a) Measured watermarked images from physical FPGA circuitry: top right image was not tampered, and remaining images were submitted to minimal perturbations (see text). (b) Extracted watermarks for each case.
References

[1] R. E. Blahut, *Fast Algorithms for Digital Signal Processing*, Addison-Wesley, 1987.

[2] H. Borgen, P. Bours, and S. WoltUSEn, Visible-spectrum biometric retina recognition, in Proceedings of the International Conference on Information Hiding and Multimedia Signal Processing, 2008, pp. 1056–1062.

[3] S. BouSSAKTA, O. H. AlSHIBAMI, and M. Y. Aziz, Radix-2 × 2 algorithm for the 3-D discrete Hartley transform, IEEE Transactions on Signal Processing, 49 (2001), pp. 3145–3156.

[4] S. BouSSAKTA and A. G. J. Holt, Calculation of the discrete Hartley transform via the Fermat number transform using a VLSI chip, IEE Proceedings G Electronic Circuits and Systems, 135 (1988), pp. 101–103.

[5] R. N. BrACEWELL, *The Hartley transform*, Oxford University Press, New York, 1986.

[6] J. Canaris, A VLSI architecture for the real time computation of discrete trigonometric transforms, The Journal of VLSI Signal Processing, 5 (1993), pp. 94–105.

[7] D. F. ChipE, M. N. S. Swamy, and M. O. Ahmad, An efficient design approach for a prime-length generalized Hartley transform systolic array, in DSP2000, 2000.

[8] H. Choi, S. Lee, D. M., Y. C., and S. Pan, Secret distribution for secure fingerprint verification, in Proceedings of the International Conference on Convergence and Hybrid Information Technology, 2008, 2008, pp. 535–540.

[9] R. J. CinTra, V. S. Dimitrov, H. M. OliVeIra, and R. M. CampelIo de Souza, Fragile watermarking using finite field trigonometrical transforms, Signal Processing: Image Communication, 24 (2009), pp. 587–597.

[10] A. S. DhAr and S. BanerJeE, An array architecture for computing two-dimensional discrete Hartley transforms, Computers and Electrical Engineering, 17 (1991), pp. 23–29.

[11] V. Dimitrov and R. BaghaiE, Computing discrete Hartley transform using algebraic integers, in Conference Record of the Thirty-Third Asilomar Conference on Signals, Systems, and Computers, vol. 2, 1999, pp. 1351–1355.

[12] I. DuleBra, Hartley transform in compression of medical ultrasonic images, in Proceedings. International Conference on Image Analysis and Processing, 1999, pp. 722–727.

[13] J.-I. Guo, C.-M. Liu, and C.-W. Jen, A novel VLSI array design for the discrete Hartley transform using cyclic convolution, IEEE International Conference on Acoustics, Speech, and Signal Processing, 3 (1994), pp. 501–504.

[14] G. H. Hardy and E. M. Wright, *An Introduction to the Theory of Numbers*, Oxford at the Clarendon Press, 4 ed., 1975.

[15] G. HuiPing, L. YingJiU, A. LiU, and S. Jajodia, A fragile watermarking scheme for detecting malicious modifications of database relations, Information Sciences, 176 (2006), pp. 1350–1378.

[16] G. A. JullIen and V. S. Dimitrov, Two-dimensional transforms using number theoretic techniques, in Computer Techniques and Algorithms in Digital Signal Processing, C. T. Leondes, ed., vol. 75 of Control and Dynamic Systems, Academic Press, 1996, ch. 4, pp. 155–210.

[17] P. Meenakshidevi, M. Venkatesan, and K. Duraiswamy, A fragile watermarking scheme for image authentication with tamper localization using integer wavelet transform, Journal of Computer Science, 5 (2009), pp. 831–837.

[18] P. K. Meher, J. K. Satapathy, and G. Panda, Efficient systolic solution for a new prime-factor discrete Hartley transform algorithm, IEE Proceedings G on Circuits, Devices & Systems, 140 (1993), pp. 135–139.

[19] A. Mondal, K. Roy, and P. Bhattacharya, Secure biometric system for accessing home appliances via internet, in Proceedings of the International Conference for Internet Technology and Secured Transactions, 2009, 2009, pp. 1–7.

[20] K. K. Parhi, *VLSI Digital Signal Processing Systems: Design and Implementation*, John Wiley and Sons, 1 ed., 1999.

[21] K. Roy, C. SueN, and P. Bhattacharya, Segmentation of unideal iris images using game theory, in Proceedings of the 20th International Conference on Pattern Recognition (ICPR), 2010, pp. 2844–2847.

[22] J. M. Tahir, S. S. Dlay, R. N. G. Naguib, and O. R. Hinton, Self-checking architectures for fast Hartley transform, in Proceedings of the 1995 European conference on Design and Test, Washington, DC, USA, 1995, IEEE Computer Society, p. 363.

[23] H. Tamori, N. Aoki, and T. Yamamoto, A fragile digital watermarking technique by number theoretic transform, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, E85-A (2002), pp. 1902–1904.
[24] H. Tamori and T. Yamamoto, *Asymmetric fragile watermarking using a number theoretic transform*, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 92-A (2009), pp. 836–838.

[25] T. Toivonen and J. Heikkila, *Video filtering with Fermat number theoretic transforms using residue number system*, IEEE Transactions on Circuits and Systems for Video Technology, 16 (2006), pp. 92–101.

[26] A. B. Watson and A. Poirson, *Separable two-dimensional discrete Hartley transform*, Journal of the Optical Society of America A, 53 (1986), pp. 2001–2004.

[27] E. L. Zapata and F. Argüello, *A VLSI constant geometry architecture for the fast Hartley and Fourier transforms*, IEEE Transactions on Parallel and Distributed Systems, 3 (1992), pp. 58–70.