IMAC: In-memory multi-bit Multiplication and ACCumulation in 6T SRAM Array

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Abstract—‘In-memory computing’ is being widely explored as a novel computing paradigm to mitigate the well known memory bottleneck. This emerging paradigm aims at embedding some aspects of computations inside the memory array, thereby avoiding frequent and expensive movement of data between the compute unit and the storage memory. In-memory computing with respect to Silicon memories has been widely explored on various memory bit-cells. Embedding computation inside the 6 transistor (6T) SRAM array is of special interest since it is the most widely used on-chip memory. In this paper, we present a novel in-memory multiplication followed by accumulation operation capable of performing parallel dot products within 6T SRAM without any changes to the standard bitcell. We, further, study the effect of circuit non-idealities and process variations on the accuracy of the LeNet-5 and VGG neural network architectures against the MNIST and CIFAR-10 datasets, respectively. The proposed in-memory dot-product mechanism achieves 88.8% and 99% accuracy for the CIFAR-10 and MNIST, respectively. Compared to the standard von Neumann system, the proposed system is 6.24× better in energy consumption and 9.42× better in delay.

Index Terms—In-memory computing, 6T SRAM Cell, Multiplication, Accumulation, Neural Networks

I. INTRODUCTION

For decades the miniaturization of Silicon field effect transistor has been the major driving factor leading to ever increasing on-chip compute capabilities. However, the classical transistor scaling has slowed down as device dimensions are approaching their physical limits. Unfortunately, this imminent end of transistor scaling comes at a time when massive data compute requirements demanded by machine learning and neural network applications have become more important than ever. With this backdrop, a novel paradigm — in-memory computing, is being actively investigated by the research community. In-memory computing attempts to embed certain aspects of computations within the memory array. This allows to bypass the well-known memory-wall bottleneck that limits both the throughput and energy-efficiency of state-of-the-art processors [1], [2]. In-memory computing is being actively explored in both Silicon and beyond-Silicon emerging technologies.

Out of various memory technologies SRAM based in-memory computing is of particular interest. SRAMs occupy dominant chip area in state-of-the-art processors. Further, SRAMs are highly subanked, therefore, enabling in-memory fine-grained compute operations within each sub-bank allows massive parallelism both due to high internal memory bandwidth and the existence of multiple sub-banks. Various previous works have investigated different forms of in-memory enabled SRAM banks. These can be broadly classified in two categories — those that enable bit-wise Boolean computations and those that focus on analog mixed-signal computations within the SRAM array. Bit-wise Boolean computations by enabling word-lines simultaneously and using modified sensing circuit have been presented in [3], [4], [5]. Additionally, such bit-wise computation can be complemented with additional digital circuits at the periphery to implement more complex operations like addition [3], [6]. On the other hand, analog charge-based compute techniques have been utilized in works like [5], [7], [8]. Additionally, current based analog convolution for multi-bit dot product computations has been presented in [4], [9]. Note, given the complex nature of analog operations, many analog compute proposals in SRAM arrays have either relied on using explicit analog multipliers at the periphery as in [8], [10] for the 6T cells or use less-area efficient 8T or 10T cells for binary and multi-bit dot products. In this paper, we present multi-bit multiplication in 6T SRAM cells through charge sharing principle followed by an analog accumulation operation. We further perform an extensive variation analysis to study the approximations induced in the resulting computations due to the analog nature of processing. Subsequently, based on the obtained approximation we implement a deep neural network and analyze the effect of circuit level approximation on the recognition accuracy for CIFAR10 dataset. The key highlights of this work are as follows:

1) In-SRAM Analog Multiplication: We make use of the SRAM precharge circuit to perform multi-bit analog multiplication by encoding the bit significance in the pulse width of pre-charge pulse.
2) Analog Accumulation: We propose an almost-linear analog accumulator followed by the multiplication operation to further reduce the overall energy consumption as well as increase computing throughput.
3) Variation Analysis: To ascertain the proposed in-memory computing primitive robustness, we perform extensive variations in the SRAM cells.

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The rest of the work is organized as follows. In Section II we elaborate the proposed in-memory multiplication. Section III explains the accumulation scheme. Circuit simulation results are presented in Section IV. In Section V we analyze the effect of variations on the end application performance. System level comparisons are presented in Section VI. Section VII concludes the manuscript.

II. 6T SRAM BASED MULTI-BIT MULTIPLICATION

We use the standard 6T SRAM cell as the basic memory unit as shown in Fig. 1. The conventional read and write operations in a 6T SRAM cell are performed as follows. For reading the data stored in the cell, the bitline terminals, BL and BLB, are precharged to $V_{DD}$, and the wordline (WL) is enabled. When ‘1’ ($Q=V_{DD}$ and $Q_b=0$ V) is stored in the cell BL voltage remains close to $V_{DD}$ while BLB starts discharging. Likewise, when ‘0’ ($Q=0$V and $Q_b=V_{DD}$) is stored BLB would remain close to $V_{DD}$ and BL would discharge from its initial precharged voltage. For writing ‘1’ into the cell, BL is pulled to $V_{DD}$, BLB is pulled to 0V and WL is enabled. Similarly for writing ‘0’ BLB is pulled to $V_{DD}$, BL is pulled to 0V and WL is enabled.

We would now describe the proposed scheme to enable ‘in-memory compute’ mode wherein a read operation is accomplished such that instead of reading the individual data, a resultant product between two multi-bit words can be achieved. Specifically, during the multiplication operation one of the operand is passed as input (a voltage on WL) and other operand is stored in memory. We denote the operand passed as input (a voltage on WL) and other operand is stored in memory as $W$ in the rest of the paper.

A. Multi-bit Single-bit Multiplication in 6T SRAM

Let us first consider the simpler case, wherein $V_{in}$ is a multi-bit word and $W$ is a single bit word. Suppose $W$ is ‘1’ ($Q=V_{DD}$ and $Q_b=0$ V) and stored in the 6T SRAM cell. As mentioned, BL and BLB are precharged to $V_{DD}$ for a read operation. When the world-line is enabled, transistor M5 start conducting but transistor M6 remains in cut-off. Thereby transistor M5 creates a path for BLB (pre-charged to $V_{DD}$) to discharge toward ground (0V). In fact, the rate of discharge of BLB in this case depends on the discharging current through transistor M5. The current flowing through the transistor M5 is proportional to its overdrive voltage. Therefore, changing WL pulse amplitude directly controls the gate voltage of transistor M5, thereby, controlling the discharge rate of BLB. As such, if a multi-bit input is mapped as an analog voltage ranging from the transistor threshold voltage to $V_{DD}$, the discharge on BLB would be proportional to $V_{in}$ provided that $Q_b$ is storing 0V. The resultant discharge voltage on the BLB, within a specified time, effectively represents a one bit multiplication on the data stored in SRAM cell ($W$) with the multi-bit $V_{in}$ applied as an analog voltage on the word-line.

We use a standard SRAM cell in 65 nm TSMC process with BLB discharging rate slowing down drastically at BLB value of $\sim 100$ mV. Thus, we allow BLB to discharge only till 350 mV to maintain the linearity. We refer to the time taken for BLB to discharge from $V_{DD}$ to 350 mV when WL is at $V_{DD}$ to be $8\tau$. We limit the maximum WL pulse width to $8\tau$. Assuming a 4-bit word for $V_{in}$, this corresponds to the case when $V_{in}=15$ ($V_{in}=1111$, maximum value) – the amplitude of WL is $V_{DD}$ and pulse-width of WL is $8\tau$. Fig. 2 (a) shows BLB discharge process versus time. On the other hand, when $V_{in}=0$ ($V_{in}=0000$, minimum value), the amplitude of WL is mapped to 300 mV (close to the value of transistor threshold voltage) while the pulse-width remains $8\tau$. In this case the transistor M5 will no be able to switch ON and BLB will not discharge as shown in Fig. 2 (c). For $V_{in}$ value lying between 0 to 15, say 6, the amplitude of WL lies between the two extreme cases, keeping the pulse width of WL as $8\tau$. Here, the transistor M5 switches ON but as the overdrive voltage is low the discharge rate of BLB will be proportionally low. As the duration of discharge is fixed to be $8\tau$, the BLB would not discharge completely and rather settle to an intermediate value as shown in Fig. 2 (b). Essentially, the discharge rate is proportional to $V_{in}$ and since the duration of discharge is fixed, it can be shown that discharge of BLB after a period of $8\tau$ is proportional to $V_{in}$. Conversely, when $W$ is ‘0’ ($Q=0$V and $Q_b=V_{DD}$) and stored in a 6T SRAM cell as shown in Fig. 2 (b).

Figure 1: 6T-SRAM cell.

Figure 2: Waveform of WL and BLB voltage when (a) $V_{in}=15(1111)$, $W=1$ (b) $V_{in}=6(0110)$, $W=1$ (c) $V_{in}=0(0000)$, $W=1$. 
enables multi-bit multiplication between $V_{in}$ and $W$. The rate of discharge of BLB is made proportional to $V_{in}$ to LSB bit. Inducing such bit significance based discharge in significance, i.e. MSB bit leads to higher discharge as compared to LSB bit. Indicating the MSB stored in the rightmost cell and LSB stored in the leftmost cell. In 6T SRAM cells in a row as shown in Fig. 3 with MSB stored in 8-bit $V_{in}$ by 4-bit $W$. The 4-bit $W$ is stored within 4 adjacent nodes. The waveforms for $W$, $V_{pre3}$, $V_{pre2}$, $V_{pre1}$, $V_{pre0}$, $EN_{ch-sh}$, BLB3, BLB2, BLB1, BLB0, and $V_{ch-sh}$. 8$t$ and $\tau_{ch-sh}$ are the pulse width of wordline and $EN_{ch-sh}$ signals respectively. Fig. 4 shows the waveforms in details.

1. transistor M5 remains in cut off and transistor M6 switches ON. In this case the source voltage of the M5 is $V_{DD}$ and the gate voltage of the M5 is $V_{DD}$. Thus, at any $V_{in}$, M5 will still be in cut off.

To summarize, when W is ‘0’ BLB does not discharge and remains close to its pre-charged voltage. When W is ‘1’ BLB discharges by an amount proportional to the input operand $V_{in}$. The reason for this being the rate of discharge of BLB is made proportional to $V_{in}$ and the duration of discharge is fixed to 8$t$. If the analog voltage obtained after converting $V_{in}$ is $v + 300$ mV (since we map the lowest $V_{in}$ to 300 mV) and $W$ stored in memory is $w$, then the discharge of BLB can be given by following proportionality in equation (1).

$$V_{precharge} = V_{BLB} \propto v \times w$$

(1)

B. Multi-bit Multi-bit Multiplication in 6T SRAM

In this Section we discuss how to perform multiplication of 4-bit $V_{in}$ by 4-bit W. The 4-bit W is stored within 4 adjacent 6T SRAM cells in a row as shown in Fig. 3 with MSB stored in the rightmost cell and LSB stored in the leftmost cell. In order to achieve multi-bit multiplication with respect to stored value W, the BLB discharge rate should depend on bit significance, i.e. MSB bit leads to higher discharge as compared to LSB bit. Inducing such bit significance based discharge in conjunction to the discharge rate being proportional to $V_{in}$ enables multi-bit multiplication between $V_{in}$ and $W$.

This requirement can be fulfilled through the pre-charge circuits that hold the BL and BLB to $V_{DD}$. We can disable the pre-charge circuit by making $V_{pre}$ voltage equal to $V_{DD}$ at different instant of time such that the BLB corresponding to the MSB bit starts discharging before the LSB bit. The ratio of time intervals for which MSB, 2nd bit, 3rd bit and LSB should discharge is 8:4:2:1. Thereby, by appropriately pulsing the pre-charge circuit, while $V_{in}$ is applied on the WL, would make the discharge on the BLBs proportional to their bit significance and to the input voltage $V_{in}$. Interestingly, by enabling the $EN_{ch-sh}$ signal after the BLBs have been given sufficient time to discharge, the four BLBs get connected to each other leading to charge sharing. This in turn ensures that the average discharge obtained from 4 BLBs (BLB3, BLB2, BLB1, and BLB0) is proportional to analog value of W as explained by equation 2. In the proportionality equation (2), $w$ is the analog equivalent of W.

$$V_{precharge} = V_{ch-sh} \propto v \tau_{ch} \times \frac{[2^3w_3 + 2^2w_2 + 2w_1 + w_0]}{4} \propto v \times w$$

(2)

As mentioned in Section II-A, the pulse width of WL is 8$t$ and the amplitude of WL is dependent on $V_{in}$, hence the intervals of discharge for BLB3, BLB2, BLB1 and BLB0 should be 8$t$, 4$t$, 2$t$ and 1$t$ respectively. If WL and $V_{pre3}$ signals are enabled at the instant say t=0, then $V_{pre2}$, $V_{pre1}$ and $V_{pre0}$ are enabled at 4$t$, 6$t$ and 7$t$, respectively. At t=8$t$, $EN_{ch-sh}$ signal is enabled and has a pulse width of $\tau_{ch-sh}$. This enables charge sharing among BLB3, BLB2, BLB1 and BLB0. The voltage obtained after the charge sharing at the node $V_{ch-sh}$ is the analog multiplication result of 4-bit $V_{in}$ and 4-bit W. Timing diagram for various waveforms is shown in Fig. 4. In Fig. 4 we can see that there is a overlap between the WL signal and the precharge signal($V_{pre3}$). This means...
that there will be a static current flowing from the PMOS of the precharge through the access transistor. Next, we explain why static current does not play a significant role in the overall energy of the multiplication operation.

C. Static Current

Multiplication operation in our approach is based on constant current discharge of the bit line as explained in Section II-A (Fig. 2). The bit line corresponding to the end of the latch storing ‘0’ will start discharging the bit line through the access transistor, while the other access transistor will remain switched off. In Section V-A we show that the internal node voltage of the SRAM cell is held close to the initial stored node voltage during the multiplication operation. Hence, the discharge current is mainly governed by the access transistor as the node storing ‘0’ is strongly held close to 0V by the NMOS transistor of the inverter latch. Further, to have a nearly constant current discharge we ensure that $V_{DS}$ of the access transistors is large enough to operate in the constant current region of $I_{DS} - V_{DS}$ characteristics. Therefore, we do not allow the bit line voltage to fall below a minimum voltage ($\approx 350$ mV), as mentioned in Section II-A, to have a high enough $V_{DS}$ across the access transistor. Regarding the case where the WL signal and the precharge circuit have no overlap, BLB will discharge through the access transistors with a constant current. In this case, the charge stored on the bit line capacitance acts as source of power to facilitate constant current, this in effect reduces the voltage of capacitance at a constant rate. Due to channel length modulation effect the current through the access transistor not perfectly constant as the BLB voltage drops from 1200 mV to 350 mV, hence, to tackle this problem we change the pulse width of the precharge circuit to make the discharge at BLB3, BLB2, BLB1, and BLB0 in the ratio 8:4:2:1 respectively. This approach is discussed in detail in IV-B.

The static current discharge path has a PMOS transistor of precharge circuit, NMOS access transistor and the NMOS transistor of the inverter latch. The PMOS transistor of the precharge circuit is strong enough to hold the bit line voltage close to 1.2V, when both the precharge and WL signals are enabled. Hence, the access transistor connected to the internal node storing logic low, has one of the end held to close to ground by the NMOS transistor of the inverter latch circuit, while the other end held close to 1.2V by the PMOS transistor of the precharge circuit. As a result, the current flowing through the access transistor and the NMOS transistor of the inverter latch is still governed by the access transistors. This current is equal to the fixed current that was discussed in the case where there was no overlap between the precharge circuit operation and the WL signal. This is due to the fact that the current through the access transistor is constant for $V_{DS}$ ranging from 350 mV to 1200 mV and in this case $V_{DS}$ is $\approx 1200$ mV. The difference in this case is that the bit line capacitor maintains it’s charge and the constant current in this case is supplied by the power supply through the precharge circuit.

From the above two cases, it is clear that overlap between the operation of precharge circuit and the WL signal does not play a key role in terms of the energy consumption. Both the case dump equal amounts of charge to the ground if we neglect the channel length modulation effect of the access transistor. The difference in both the cases is that the case having the overlap in the operation of precharge and WL signal takes the charge form the power supply directly, while on the other hand the case where there is no overlap between the two operations takes the charge form the bit line capacitance which in turn is replenished by the supply during the next cycle of operation of precharge circuit. Our circuit simulations in spectre show constant and similar currents values for the $I_{DS}$ of the NMOS transistor of the inverter latch for both the aforementioned case and justify the above explanation. In the next Section, we describe the array peripherals required to perform Multiply and Accumulate (MAC) operation.

III. Peripheral Circuits

In this Section we explain the analog accumulator and the SAR-ADC in detail. Further, we provide provide the overall array architecture.

A. Analog Accumulator

The accumulation circuit shown in Fig. 5 consist of a sample and hold circuit formed by a transmission gate (M7 and M8) and a sampling capacitor; a PMOS transistor (M9)
and an accumulation capacitor. It is important to note that we use PMOS transistor instead of transmission gate for accumulating charge on the accumulation capacitor. Transistor $M9$ can only conduct when its overdrive voltage is positive, i.e. if $0V$ is applied at the gate of this transistor, it will only conduct when $V_{\text{sample}}$ is greater than the threshold voltage of transistor $M9(V_{th,M9})$. If we are able to maintain the voltage of the accumulation capacitor less than $V_{th,M9}$ for the entire process of accumulation period, then we can see that charge dumped on the accumulation capacitor would be $C_{\text{sample}} \times (V_{\text{sample}} - V_{th,M9})$. This charge is independent of the capacitor ratios or the initial charge/voltage on the accumulation capacitor. The increase in the voltage of accumulation capacitor would be given by:

$$\Delta V_{\text{acc}} = C_{\text{acc}} \times (V_{\text{sample}} - V_{th,M9})$$

(3)

Here, $C_{\text{acc}}$ and $C_{\text{sample}}$ represent the accumulation capacitor(40 fF) and the sampling capacitor(2.5 fF) respectively. Equation (3) holds true only if the following two conditions are met.

$$V_{\text{sample}} \geq V_{th,M9}$$

(4)

$$V_{\text{acc}}(n \times \Delta V_{\text{acc}}) \leq V_{th,M9}$$

(5)

Here, $n$ is the number of accumulations performed. Equations (4) and (5) are the design constrains which help us decide $n$, $V_{th,M9}$ and the capacitor sizes used in the accumulation circuit. As analog accumulation unit was introduced to skip the ADC operation for every analog product. A high value of $n$ is hence preferred as it leads to less frequent operation of ADC which in turn helps us save energy and improve the overall latency. On the other side, a high value of number of accumulations leads to a higher value accumulation capacitor evident from the above inequalities (4 and 5). A larger accumulation capacitor would occupy more area and would therefore limit the number of accumulations. A high value of number of accumulation also leads to degradation in software accuracy as the error in the analog value accumulated increases with number of accumulations. Further, the time taken for accumulation is 5 times the time taken for multiplication as seen in Table IV. Therefore, for the number of accumulations we explored the multiples of 5 to facilitate the multiplexing of ADC to further reduce the peripheral area if required. Hence, the number of accumulations(10) were chosen to be maximum provided the area and software accuracy are in acceptable limits. We keep the threshold voltage of transistor $M9$ to be high enough($\approx600$ mV) to allow larger values of $n$ to satisfy the constrain equation (5) while not violating constrain equation (4). The sampling capacitor $C_{\text{sample}}$ was kept to be the low (2.5 fF), so that the voltage at the node $V_{\text{sample}}$ is almost equal to the voltage at the node $V_{ch-sh}$ and not a scaled version of $V_{ch-sh}$. This means that the range of voltage at node $V_{\text{sample}}$ is also 750 mV to 1200 mV. Using the value of $C_{\text{sample}}$, $V_{th,M9}$ and $n$ in constrain equation (5) we get $25 \times 10^{-15} \leq C_{\text{acc}}$ when $V_{\text{sample}}$ is kept as 1200 mV (voltage corresponding to maximum value of $\Delta V_{\text{acc}}$, when all parameter apart from $V_{\text{sample}}$ is kept fixed). Hence we chose the accumulation capacitor to be 40 fF.

B. Successive Approximation Register based ADC

The accumulated voltage is then converted to a digital output using a Successive Approximation Register ADC (SAR-ADC) as shown in Fig 6. Three components of this ADC are the sense amplifier, digital logic and the capacitor array based Digital to Analog Converter (DAC). The digital logic initializes the MSB of the ADC output to ‘1’, keeping all other bits ‘0’ and sends the digital code to DAC. The DAC converts this digital code to an analog voltage ($V_x$). Subsequently, $V_x$ is compared against the input analog signal using a comparator. This is equivalent to comparing the input signal ($V_{\text{acc}}$) to $(V_{dd} + V_{ss})/2$. If the input signal is higher than the DAC output (Compout is 0), MSB is kept at ‘1’ otherwise, it is flipped to ‘0’ which concludes 1 cycle of operation for SAR-ADC. In the consecutive cycle, the digital logic makes the next most significant bit ‘1’ keeping all the bits following it to be ‘0’. DAC converts the digital code to the analog signal which is compared against the input signal using the Sense Amplifier. The sense amplifier output is used to fix the bit under evaluation. The same process continues until all bits are evaluated. SAR-ADC takes $n$-cycles to evaluate the digital output, where $n$ is the bit precision of the ADC. We adopt a capacitor array as the DAC and a standard sense amplifier as the comparator to reduce the static energy consumption in the utilized SAR-ADC. The target application of this work inspires the ADC bit-precision to be 4 bits with a conversion delay of 5 ns.

C. Array Overview

The SRAM array for the proposed in-memory computing methodology is shown in Fig. 7. We adopt TSMC 65 nm technology node in our design. Additionally, we consider 50 fF bitline capacitance resulting from metal lines in layout.

The proposed array behaves as a conventional 6T-SRAM memory when $EN_{ch-sh}$ and the analog multiplexer (MUX) are disabled and normal read/write operations are performed. Moreover, the circuit is capable of performing 4-bit×4-bit multiplication and accumulation to provide a 4-bit output. The sign of the analog product is computed as XOR of the signs of both $V_{in}$ and $W$, and the product is accumulated on two different accumulation capacitors depending on the output.

![Figure 6: Successive approximation ADC.](image-url)
Figure 7: 6T-SRAM Array overview.

Figure 8: Analog Output when Pre-charge pulse width ratios 8:4:2:1.

Figure 9: Analog Output when BLB discharge ratio 8:4:2:1.

IV. CIRCUIT SIMULATION RESULTS

In this Section we present circuit simulation results, wherein we analyse the non-linearity in the proposed multiplication circuitry and propose a mechanism to mitigate the non-linearity.

A. Linearity Analysis

The proposed multiplication circuitry, multiplies two scalars, namely, the input $V_{in}$ and the weight $W$ in an analog fashion. For the purpose of the linearity analysis we ignore the signs of both the input and the weight. This is because our approach computes the sign of the result depending on the signs of input and weight using digital gates and is free from any analog non-linearity. On the x-axis in Fig. 8 we have the ‘Expected Product’ or expected multiplication result for the digital multiplication of input and weight, while on y-axis we have the ‘Observed Product at $V_{ch-sh}$ (V)’ which is the analog product obtained at the node $V_{ch-sh}$ corresponding to input $V_{in}$ and the weight $W$. For example, if the input $V_{in}$ is 5 and the weight $W$ is 10, then the x-coordinate for such a pair will be 50 ($=5 \times 10$), while the y-coordinate will be the analog multiplication result obtained at $V_{ch-sh}$ by our proposed approach. We use spectre simulation to obtain the analog multiplication values as proposed in the paper. The SRAM bit cells are initialized to the weight value $W$ and input $V_{in}$ is provided to the input DAC. The DAC converts the input to an analog value according to the equation $6$. To multiply the two scalars $V_{in}$ and $W$, proper signals were applied to precharge circuit ($V_{pre3}$, $V_{pre2}$, $V_{pre1}$ and $V_{pre0}$) and the charge sharing circuit ($E_{NH-ch-sh}$), as shown in Fig. 4.

To multiply the two scalars $V_{in}$ and $W$, proper signals were applied to precharge circuit ($V_{pre3}$, $V_{pre2}$, $V_{pre1}$ and $V_{pre0}$) and the charge sharing circuit ($E_{NH-ch-sh}$), as shown in Fig. 4.

$$V_{WL} = 300 + V_{in} \times \frac{700}{15} \text{ mV} \quad (6)$$

For the plot shown in the Fig. 8, we keep the precharge pulse widths corresponding to $V_{pre3}$, $V_{pre2}$, $V_{pre1}$, and $V_{pre0}$ such that the duration for which the BLB discharges are in the ratio 8:4:2:1 corresponding to BLB3, BLB2, BLB1 and BLB0 respectively (as shown in Fig. 4). However, with this approach we see from the scatter plot that the analog product obtained is non-linear and would require some correction techniques to mitigate the error. The possible options could be to have a non linear mapping for the input $V_{in}$ which would require design of a complicated DAC structure or non linear mapping of the weights which would require storing the non linear weights in the memory. In the next subsection we discuss how we mitigate this non linearity without having to use non-linear mapping.

B. Linearity Enhancement

We saw that the plot in Fig. 8 could be explained with four lines. This systematic non-linearity caused us to examine the analog multiplication even further. The approach followed to obtain results as shown in Fig. 8 is based on the assumption that the discharge of the BLB is the proportional to duration of discharge. However, we know that the access transistors in the SRAM bit cell are non-linear and hence the above assumption would no longer hold true. For equation (2) to hold, the discharge of BLB3, BLB2, BLB1 and BLB0 should be in ratio 8:4:2:1. Therefore, we keep the duration for which BLB3, BLB2, BLB1 and BLB0 discharge such that the discharge on the corresponding BLB is in the ratio 8:4:2:1 respectively.
other words, rather than keeping the duration of discharge in ratio 8:4:2:1, the discharge is kept in the ratio 8:4:2:1. To obtain the pulse width of $V_{\text{pre0}}$, $V_{\text{pre1}}$, and $V_{\text{pre0}}$, we obtain the time taken by the BLB to discharge to 350 mV (minimum voltage for almost linear discharge as explained in Section II), 775 mV, 987.5 mV and 1093.75 mV respectively from 1.2V when the bit stored in bit cell is high which makes the discharge in the ratio $(1200-350):4(1200-775):2(1200-987.5):1(1200-1093.75)$ respectively. For further analysis the ratios of the pre-charge pulse width are kept such that the BLB discharge ratio is 8:4:2:1.

In Fig. 10 (a) we present the analog multiplication output with varying $V_{\text{in}}$ and $W = 0, 5, 10$ and 15, similar trends were observed for other values of $W$. Similarly, in Fig. 10 (b) we observe the analog multiplication output with varying $W$ and $V_{\text{in}}$ fixed to 0, 5, 10 and 15, similar trend observed for other values of $V_{\text{in}}$. Fig. 10 (a) and Fig. 10 (b) show that digital output is directly proportional to the input voltage $V_{\text{in}}$ and the $W$ stored in the memory, respectively, confirming the multiplication operation of the proposed scheme. For Fig. 10 (a) the Integral Non-Linearity(INL) values for the $W = 0, 5, 10$ and 15 are $1.13 \times 10^{-14}$, $1.11 \times 10^{-14}$, $-4.88 \times 10^{-14}$ and $2.55 \times 10^{-14}$ respectively and INL values for $V_{\text{in}} = 0, 5, 10$ and 15 in Fig.10 (b) are $1.09 \times 10^{-14}$, $5.77 \times 10^{-14}$, $-2.36 \times 10^{-14}$ and $3.109 \times 10^{-14}$ respectively.

Note, the accumulation voltage is always less than the threshold voltage of transistor M9 as discussed in section III-A. As a result, the analog accumulator behaves linearly by design. It is worth mentioning that the DAC block in ADC is designed to perform linearly during successive approximation by fine tuning the capacitor ratio. Additionally, the comparator is designed with an offset voltage as low as 5 mV, which is lower than the ADC precision, to ensure linearity.

V. VARIATION ANALYSIS

In this section we analyse the read stability of the SRAM cells to the ‘functional read’ in Subsection A. We study the effect of variations on the proposed circuitry considering random variations of the transistor threshold voltage in Subsection B and develop a framework presented in Subsection C to study the effects of such variations on the end application accuracy.

A. Read Stability

To avoid read disturb we design the cell to have acceptable read noise margin, following a standard approach for SRAM cell design [11]. In our approach we only activate one WL at a time which further decreases the chances of corrupt read. When there is overlap between the WL signal and operation of the precharge, both BL and BLB are held high by the precharge circuit and hence the differential signal applied to the cell is zero which ensure that the data stored in the cell is not corrupted by the multiplication operation. When the precharge circuit is disabled, while the WL signal is still high, the circuit performs normal conventional read and discharges BL or BLB depending on data stored in bit cell. Many in-memory compute primitives [12], [7], [13] have shown similar kind of functional read operations where they connect the internal storage node to the bit line in order to enable analog in-memory compute.

In order to understand the read disturb that could arise due to analog multiplication operation as proposed in our approach, we need to understand the differences in our approach and the conventional memory read operation. In our approach, we have an overlap between the operation of precharge circuit and the WL signal for certain bits of weights, as seen in waveforms shown in Fig. 4. The case where the precharge circuit operation and WL signal have no overlap, as in the case of $V_{\text{pre3}}$, the operation is similar to conventional memory read operation. On the other hand, when the precharge circuit operation and WL signal have maximum overlap as seen in the case of $V_{\text{pre0}}$, it is different from the conventional read case and requires further analysis. We also use analog signal on the WL which is different from the conventional read operation. The worst case WL signal amplitude would be 1V, which is the strongest connection between the internal node and the bit line. Hence, we analyse the case where the amplitude of WL signal is 1V and there is maximum overlap between the operation of the precharge circuit and the WL signal.

To study the read disturb for these conditions, we simulate two SRAM bit cells with the precharge circuit and initialize the two cells to store opposite bits(one storing digital high and other storing digital low). We perform 10000 Monte Carlo runs, on the two SRAM cells, having the WL amplitude 1V and setting the precharge signal to $V_{\text{pre0}}$ and monitor the...
number of times the bit stored in the internal node switches. We find that none of the cells flip there initial stored states. Further, the maximum change in voltage during the functional read operation at node storing digital low (0 V) is 95.56 mV and maximum change in the node storing digital high (1 V) is 51.91 mV. This analysis shows that the proposed SRAM in memory multiplication approach is robust to read disturbs.

B. Variations in Multiplication In-memory

Random variations of access transistor threshold voltage are one of the major causes of performance degradation in circuit design. In the proposed circuit, the mismatch between BLB access transistors of the 4 adjacent SRAM cells, shown in Fig. 3, can cause erroneous output. Such output errors happen because the rate of discharge for BLB1, BLB2, BLB3 and BLB0 are no longer proportional to 8:4:2:1 for the same value of input \( V_{in} \). We perform Monte Carlo runs using the TSMC 65nm PDK to simulate the random variations in the proposed circuitry. The maximum standard deviations for the analog multiplication output in 1000 Monte Carlo runs is seen to be 13.17 mV.

To assess the effect of variations on the digital output we run 1000 samples of Monte Carlo simulation on the entire circuit consisting of SRAM array and the peripheral circuits including the ADC. The simulation results for a chosen set of cases where the digital output is 0,3,6,8,11 and 15 are shown in Fig. 11. Notice that the maximum standard deviation of the Gaussian curve for digital output was 0.6. From Fig. 11 we see that the distributions for digital output 0 and 15 are truncated Gaussian distributions. The reason for that is the ADC being only able to map the input voltage in its predefined range of conversion. Any voltage below the range of conversion is mapped to 0 and any voltage above the range of conversion would be mapped to 15.

C. Functional Accuracy Analysis

We test the proposed multiplication and accumulation engine on a convolutional neural network shown in Table I for classifying Cifar10 dataset. We refer to [14] for the training framework. The network is trained using Adam optimizer with initial learning rate of 0.0001 for 200 epochs. The learning rate is dropped by a factor of 10 at epoch number 100, 150 and 180. The training batch size and testing batch size is 32 and 128 respectively. We perform small data augmentation (Flipping the training dataset and shifting the training dataset by 4 pixels). Cross-entropy loss function is adopted for training, while the test accuracy for such network is 91.50%. Now, in order to assess the effect of hardware non ideal effects we first run the neural network with quantized weights and activation with the weights and activations being quantized separately for each layer of the network. Using linear quantization, the minimum number of bits required to represent activations and weights is 5-bits to get acceptable accuracy of 90.91%. Moreover, we add an effective multiplication error to the output map sampled from a Gaussian distribution of circuit variation sigma equal to 0.6×\( \sqrt{n} \), where n is number of 10 element MAC operations and standard deviation for individual multiplication from the variation analysis was taken to be 0.6 following a pessimistic approach. For inference, we sample the errors from the Gaussian distribution for each output map and keep it constant for that particular inference as the error is dependent on the location where the weight is written and is fixed once the weight is stored in SRAM. We run 1000 inferences adding error to the output map as described above, the test accuracy remains between 88.83%-89.62% (mean=89.25% and sigma=0.1329) with circuit variations.

Most of the recent in-memory work in literature are designed to run neural networks against the MNIST dataset. We use our network model to classify MNIST dataset on a vanilla LeNet network. For this task full precision test accuracy is found to be 99.3%, quantized (4-bit activation and 4-bit weights) test accuracy is 99.24% and test accuracy for our approach remains between 99.05% to 99.32% (mean=99.19% and sigma=0.0398) for 1000 variation-affected inference runs.

VI. SYSTEM LEVEL ANALYSIS

In this section we compare the proposed work with a standard von Neumann architecture which is considered as our baseline. For conventional von Neumann architecture a neural network application can be broken down into Read, Multiply, Accumulate and non-linearity(ReLU in our case) kernels. It is

| Layer       | Input Map | Output Map | Non Linearity |
|-------------|-----------|------------|--------------|
| 64x3xConv1  | 32x32x3   | 32x32x64   | ReLU,dropout(0.3) |
| 64x3xConv2  | 32x32x64  | 32x32x64   | ReLU           |
| 12x2xMaxPool1 | 32x32x64  | 16x16x64   |               |
| 12x2xMaxPool2 | 16x16x64  | 8x8x128    |               |
| 256x3xConv5 | 8x8x128   | 8x8x256    | ReLU,dropout(0.4) |
| 256x3xConv6 | 8x8x256   | 8x8x256    | ReLU,dropout(0.4) |
| 256x3xConv7 | 8x8x256   | 8x8x256    | ReLU           |
| 12x2xMaxPool3 | 8x8x256  | 4x4x256    |               |
| 64x3xConv1  | 1x1x4096  | 1x1x4096   | ReLU,dropout(0.5) |
| 64x3xConv2  | 1x1x4096  | 1x1x4096   | ReLU,dropout(0.5) |
| 4096x10 FC3 | 1x1x10    | 1x1x10     |               |

Figure 11: Histogram showing the effect of process variation on final digital output after the 10 element 4bit x 4bit multiply and accumulate operation.
Table II: Comparison with other related works

| Related Work | Process (nm) | SRAM Array | Cell Area | Computation Nature | Input/Weight Precision | Dataset | Network Architecture | Accuracy | Energy |
|--------------|--------------|------------|-----------|--------------------|------------------------|---------|---------------------|----------|--------|
| IMAC         | 65           | 6T         | 1x        | Analog             | 5/5                    | Cifar10 | VGG                 | >88.83%  | 158.203 nJ (/inference) |
| [12]         | 65           | 6T         | 1x        | Analog             | 6/4                    | MNIST   | LeNet-5             | >99.05%  | 359.288 nJ (/inference) |
| [15]         | 45           | 8T         | 1.68x     | Analog             | /-4                   | MNIST   | MLP                 | >97%     | 98.15%  |
| [16]         | 28           | 8T         | 1.3x      | Analog             | 8/1                   | ImageNet| AlexNet             | <1% drop | 12.8-119.7 TOPS/W |
| [17]         | 65           | 12T        | 2x        | Analog             | ternary/1             | Cifar10 | MNIST              | 85.7%   | 90.42%  |
| [19]         | 55           | Twin-8T    | 1.4x      | Digital           | 4/5                   | Cifar10 | CNN                | 99.52%  | 11.7 pJ (unit-Macro (64×60 bits)) |
| [9]          | 28           | 6T         | 1x        | Digital           | 8/8                   | ImageNet| Inception V3       | -        | 0.236 J (/inference) |

Figure 12: Energy Delay Product comparison for IMAC and von Neumann with varying $B_{IO}$ (bits fetched from SRAM to processor per bank)

Figure 13: Plots showing inference comparison for different layers in Lenet-5 using MNIST dataset (a)Delay (b) Energy (c) Energy-Delay product.

Table III: Notations used in the delay and energy equation

| Notation | Description |
|----------|-------------|
| M        | number of input Feature Maps |
| N        | number of output Feature Maps |
| K        | Kernel size K×K |
| L        | Size of input feature map L×L |
| $A_{move}$ | Size of output feature map $N_{move} \times N_{move}$ (for memory = L × K + 1) |
| $B_{IO}$ | bits fetched from SRAM to processor per bank |
| $B_{SRAM}$ | bit width of the weight stored in SRAM |
| $N_{col}$ | number of columns in SRAM array |
| $N_{SRAM}$ | number of SRAM banks |
| $N_{mult}$ | number of multipliers in processor |
| $T_{read}$ | time required to fetch data from SRAM to processor |
| $T_{mult}$ | time required to perform multiplication in processor |
| $T_{mac}$ | time required for 1 in memory analog multiply and accumulation |
| $T_{adc}$ | time required for ADC operation |
| $E_{read}$ | energy required to fetch data from SRAM to processor |
| $E_{mult}$ | energy required to perform multiplication in processor |
| $E_{mac}$ | energy required for 1 in memory analog multiply and accumulation |
| $E_{adc}$ | energy required for ADC operation |
| $R$ | number of MAC performed in analog domain |
| $P_{leak}$ | Standby power consumption of SRAM memory |

The delay ($T_{in-memory}$) and energy ($E_{in-memory}$) of convolution operation in the conventional von Neumann architecture are given by equation (7) and (8) similar to [12]. The notations used in the equations below are described in Table III. We can obtain the formula for fully connected layer by simply making the input size $(L)$ and kernel size $(K)$ as 1. In the fully connected layer $M$ and $N$ denote the number of input and output neurons respectively.

$$T_{VN} \approx \left[ \frac{MNK^2}{(B_{IO}/B_{W})N_{bank}} \right] T_{read} + \left[ \frac{MNK^2}{N_{mult}} \right] N_{move}T_{mult}$$

(7)

$$E_{VN} \approx MNK^2E_{read} + MNK^2N_{move}E_{mult} + P_{leak}T_{VN}$$

(8)

The delay($T_{in-memory}$) and energy($E_{in-memory}$) for convolution operation involving in-memory multiplication operation as described in this work is given by equation (9) and (10) respectively.

$$T_{Imac} \approx \left[ \frac{MNK^2}{(N_{col}/B_{W})N_{bank}} \right] N_{move}^2[T_{mac} + T_{adc}/R]$$

(9)

$$E_{Imac} \approx MNK^2N_{move}^2E_{mac} + E_{adc}/R + P_{leak}T_{in-memory}$$

(10)

For a fair comparison, all array parameters are kept the same as [12] and delay and energy parameters are obtained from circuit simulations. The parameters used are presented in Table IV. Fig. 13 compares the energy, delay and the Energy delay product of this work against baseline. From Fig. 13, the total improvements in energy, delay and energy-delay product are seen to be 9.42×, 6.24× and 58.79× respectively. Since the array architecture for this work is kept similar to [12], we compare the Energy and Delay of this work and find this work to be 2.27× and 4.83× better than [12]. Table II compares this work with other similar in-memory computing works. The plot show in Fig. 12 compare the EDP improvements of this work against von Neumann for different $B_{IO}$. EDP of this work
Table IV: Parameter Values

| Parameter | Value | Parameter | Value |
|-----------|-------|-----------|-------|
| $B_{1O}$ | 16-256 | $B_W$ | 5 |
| $N_{bias}$ | 4 | $N_{cell}$/m | 256 |
| $N_{mult}$ | 175 | |
| $E_{read}$ | 52.3 pJ | $T_{read}$ | 4 ns |
| $E_{write}$ | 0.9 pJ | $T_{write}$ | 4 ns |
| $E_{DAC}$ | 0.254 pJ | $T_{DAC}$ | 1 ns |
| $P_{peak}$ | 0.253 pJ | $T_{ADC}$ | 5 ns |
| $P_{peak}$ | 2.4 nW | |

Table V: Area estimations

| Component | Total area per array ($\mu$m$^2$) |
|-----------|---------------------------------|
| SRAM cell | 83100 |
| ADC | 40800 |
| Accumulator | 30600 |
| DAC | 400 |
| MUX | 2100 |
| Decoder | 4800 |
| Column circuit | 44000 |

is $22 \times$ better than von Neumann, even when $B_{1O}$ is made 256. The area estimates for individual blocks are presented in the Table V. It can be seen that $\sim$36% of the total array area would be occupied by the peripherals introduced in this work.

VII. CONCLUSION

In this work we present an in-memory dot product computing primitive using standard 6T SRAM arrays. We encode the input ($V_{in}$) signal as an analog voltage on the wordline, while the bit significance of the stored input (W) is encoded using precharge pulse. We perform analog accumulation to reduce the use of energy expensive ADC. We also perform detailed circuit analysis including random transistor variations to study the effects of such non-idealities on application accuracy. We develop a circuit-software co-simulation framework including circuit non-idealities and show an accuracy of 88.83% and 99.05% on CIFAR-10 and MNIST datasets, respectively. Additionally, we evaluate the proposed in-memory compute primitive to compare the system delay/energy with state-of-the-art neural network in-memory accelerators. The proposed system is $58.78 \times$ and $8 \times$ better in EDP than the standard von Neumann system and recent neural network accelerator, respectively.

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