A flexible design platform for Si/SiGe exchange-only qubits with low disorder

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Gated silicon quantum dots are an attractive qubit technology for quantum information processing with respect to coherence time, control, and engineering. Here we present an exchange-only Si qubit device platform that combines the throughput of CMOS-like wafer processing with the versatility of direct-write lithography. The technology, which we coin “SLEDGE,” features dot-shaped gates that are patterned simultaneously on one topographical plane and subsequently connected by vias to interconnect metal lines. The process design enables non-trivial layouts as well as flexibility in gate dimensions, material selection, and additional device features such as for rf qubit control. We show that the SLEDGE process has reduced electrostatic disorder with respect to traditional overlapping gate devices with lift-off metallization, and we present spin coherent exchange oscillations and single qubit blind randomized benchmarking data.

FIG. 1. A) Illustrated render of SLEDGE device. Gate level in tan and BEOL levels in aqua. B) Top-down SEM image after gate etch with gaps evident between gates. Labels are as described in text. C) Top-down SEM image after M1 CMP of dual damascene BEOL. Spans connect each via to bond-level routing (not shown). Scale bars in (B) and (C) are 200 nm. D) Cross-section TEM image through P-gate row, as illustrated by red dashed line in (C), showing BEOL vias contacting uniplanar gates. E) Cross-section TEM image through rightmost P-T gates, as illustrated by blue dashed line in (C), showing M1 trench in ILD connecting to P-gate via.

connect vias to macroscopic routing 10 µm to 50 µm away (not shown). The gate-level design (Fig. 1(b)) is similar to recent work on Si quantum dot devices [7, 14]. Plunger (P) and exchange (X) gates for accumulating and exchange-coupling electron spins are arranged collinearly and are offset from measure dot (M) gates used for charge
sensing and readout of spin-to-charge conversion. Electrons are supplied by bath (B) gates via tunnel gates (T and Z) to P- and M-gates, respectively. Electron baths are supplied from source/drain Ohmics via supply gates (SG, see Fig. 2(a) lower right), which control Ohmic-bath contact resistance independent of B-gate voltage [15]. There are two field gates used for depleting carriers around the active gates: the inner field gate (IFG) for the region between P and M gates, and the outer field gate (OFG) for the periphery. SLEDGE devices are nominally designed for triple-dot exchange-only qubit operation [16], but could be used for a variety of encodings.

The uniplanar gate arrangement is a key feature of SLEDGE and is unlike conventional quantum dot qubit devices that have been demonstrated to date, in which exchange gates (sometimes referred to as barrier gates) are on a separate dielectric plane and may overlap laterally with plunger gates [17]. From a qubit operation perspective, exchange gates on the same topographical plane as plunger gates experience less electric field screening than those on a separate plane and therefore require smaller voltage throws to modulate exchange energy for qubit rotations (see supplement). The absence of an additional dielectric layer between exchange gates and quantum well should also reduce charge noise [18]. In addition to the uniplanar gate design, the quantum dot gates are notably dot-shaped (~zero-dimensional), as opposed to conventional extended line-shaped (~one-dimensional) gates. The major drawback of using one-dimensional gate lines to define a zero-dimensional quantum dot is that device designs are essentially topologically limited to ring-like (i.e., two-row) geometries, whereas SLEDGE designs can be extended to highly-customizable gate arrangements with additional BEOL levels as needed (see supplement).

The process flow to fabricate SLEDGE devices on Si/SiGe quantum well heterostructures is outlined in Fig. 2(a). The heterostructure (“epi wafer”) consists of a tensile-strained Si quantum well epitaxially grown on a strain-relaxed Si$_{1-x}$Ge$_x$ (x = 0.25 − 0.35) buffer, followed by a SiGe capping layer of the same stoichiometry as the buffer. The beginning of the process flow includes optical lithography steps to pattern degenerately doped phosphorus-implanted Ohmics (NWELL) and argon-implanted electrically inactive regions (ISO). After defining implant regions, the gate dielectric (bilayer Al$_2$O$_3$/HfO$_2$) and gate metal (TiN) stack are blanket deposited, and gates are patterned in two steps. First, an optically-defined coarse etch removes gate metal from a majority of the wafer, leaving a block of gate metal for each device from which all active gates will be subtractively patterned. Second, positive tone e-beam lithography is used to write gaps between gates, and a F-based dry-etch of gaps defines gates, as seen in the top-down SEM image of Fig. 1(b). The process flow then enters the BEOL phase, wherein gates are contacted by vias (V01, connects M0 (gate) to M1) through an interlayer dielectric material (ILD, SiO$_2$), and spans (M1) connect vias to macroscopic routing at the bond pad level. A top-down SEM image after M1 patterning is shown in Fig. 1(c).

The SLEDGE gate process is compatible with a variety of BEOL integration schemes due to its topographically flat design. Fig. 1(d-e) shows cross-sectional TEM images along horizontal and vertical cuts from a TiN dual damascene process. (We have also demonstrated a subtractive BEOL process flow, as discussed in the supplement). Here, vias are patterned by e-beam lithography and etched into the ILD, stopping selectively on a HfO$_2$ etch stop dielectric layer deposited on top of the gates prior to ILD deposition. M1 spans are then patterned by e-beam lithography and trenches are etched into the ILD. Following e-beam resist strip, a blanket etch completes the via etch down to gates through the etch stop layer. We fill V01 and M1 with an atomic layer deposition (ALD) TiN process, followed by chemical-
mechanical polishing (CMP) to remove excess TiN and isolate M1 spans (Fig. 1(c)). M1 is subsequently contacted by an optically-defined metallization step to create wide (1 µm to 3 µm) routing lines and bond pads for wirebonding to a chip carrier.

Using direct-write e-beam lithography with separate gate and BEOL contact layers allows for within-wafer flexibility in device design. In one reticle (∼10 mm × 10 mm), of which many are patterned across each wafer, we can fabricate devices with varying parameters to explore a broad design space including, but not limited to, gate pitch, P-M separation, relative P/X ratio, and M1 width. The gate, V01, and M1-level designs can be easily and independently modified in layout. Using appropriate proximity effect correction [19], new designs are fractured and patterned in e-beam lithography without needing substantial development, if any, to optimize exposure or develop conditions. As an example, we show in Fig. 2(b) SEM images of three different devices patterned in one reticle with varying P/X dimensions but fixed pitch and fixed V01/M1-level design. The P-gate diameter (dp) and X-gate length (Lx) are varied from 90/50 nm to 110/30 nm, but the BEOL dimensions are unchanged between devices. This allows for examining relative P- and X-gate capacitances without confounding effects from differences in contact layers. The device design flexibility is additionally independent of the substrate heterostructure design, wherein Si well and SiGe cap can be modified in the epitaxial growth stage prior to fabrication. The ability to explore a broad parameter space is crucial for converging on the optimal device design for spin-based quantum information processing.

Flexibility of the SLEDGE process extends beyond gate-level device design. BEOL materials can be chosen separately from gate metal provided a sufficient Ohmic contact can be engineered. For example, a subtractive BEOL process can be used if sputtered metals (e.g. Nb or Pt) are desired, while dual damascene is conducive to materials deposited by chemical vapor deposition or ALD (e.g. W or TiN). Moreover, the BEOL span fanout can be readily designed to allow space for additional active features in arbitrary locations around the device, such as a micromagnet or a superconducting resonator [4, 20], again independent of the gate-level design (see supplement).

The requirements for e-beam overlay between V01-gate and M1-V01 layers are approximately 5 nm to 15 nm, set by gate pitch and minimum gate dimension. While non-trivial, we readily achieve the alignment requirements within-wafer and across lots with a non-customized, commercially available Raith EBPG5200 e-beam writer. In the supplemental materials, we show that the mean misalignment magnitude across four representative lots (with four wafers per lot) is ≤ 5 nm for both V01-gate and M1-V01 levels. We use the tool with four 3-in wafers (i.e. one lot) mounted onto a 200 mm wafer holder, and therefore the overlay we achieve represents a 200 mm wafer capability for e-beam lithography. We show also that the mean P-gate critical dimension (CD) in lithography varies < 7% between the same four lots. Overall, this demonstrates that e-beam lithography is well capable of wafer-level Si qubit fabrication.

In addition to device design flexibility, the SLEDGE process flow enables aggressive SiGe surface cleaning prior to gate dielectric deposition. With overlapping gate technologies [7, 21], the screening gate (also known as confinement gate) and underlying gate dielectric, which are commonly Al-based, preclude most wet surface cleans prior to plunger gate dielectric deposition. Similar restrictions exist for exchange gate dielectric deposition. This can lead to substantial interface defect densities and associated electrostatic non-uniformity. Pd gates are more etch-resistant than Al [22], but still may be roughened or delaminated in common HCl- or piranha-based (H2SO4:H2O2:H2O) cleaning chemistries. In the SLEDGE process with simultaneously patterned unipolar gates, there is only one dielectric layer for all gates, and the semiconductor surface is free of metal and dielectric materials prior to dielectric deposition. Therefore, wet etchants for trace metal, oxide, and carbon contamination, such as SC1 (NH4OH:H2O2:H2O), SC2 (HCl:H2O2:H2O), HF, and piranha can be used given ratios are chosen to have reasonable selectivity to SiGe.

The improvement in electrostatic uniformity with appropriate surface cleaning can be demonstrated from characteristics of gated Hall bars (HB) fabricated on-wafer alongside quantum dot devices. On our device wafers, gates for HBs (∼400 µm × 20 µm) are fabricated as process control monitors at each planar metallization step (e.g. gate, M1, bond), and Hall parameters are measured to characterize the epitaxial material and device dielectric layers. Such HBs serve to quickly quantify intra- and inter-wafer gate/semiconductor uniformity due to relative ease of fabrication and measurement interpretation. We use low carrier density HB properties to quantify potential disorder [23], which influences charge manipulation at the dot level. In two-dimensional electron systems, potential disorder on relevant length scales can be characterized by the density at which there is a crossover from metallic to insulating behavior. The crossover density has various potential mechanisms, for example strong localization or that of classical percolation theory, which each have several measurement methods [24]. In our Hall measurements, we characterize disorder instead using the sheet density at which the Hall mobility extrapolates to 0 in a linear mobility-density plot, which we denote as nmin. To extract nmin, we perform a line fit using only data in the low-density regime (n ≤ 4 × 1010 cm−2). While not necessarily physical (negative values are possible), the advantage of nmin is that extrapolation is relatively straightforward, in contrast to the percolation density or metal-insulator transition density. The latter may involve temperature sweeps and/or fitting many data points to some functional form, which can be difficult for imperfect gate or epitaxial structures. In addition, we have found in our HBs that nmin typically
scales similarly as the percolation and metal-insulator transition densities.

In Fig. 3(a), we plot \( n_{\text{min}} \) distributions for lift-off plunger gates (from our overlapping gate technology prior to SLEDGE), SLEDGE gates with unoptimized surface cleaning, and SLEDGE gates with optimized surface cleaning. From lift-off gates to unoptimized SLEDGE gates, mean \( n_{\text{min}} \) is reduced from \( 4.5 \times 10^{10} \, \text{cm}^{-2} \) to \( 2.6 \times 10^{10} \, \text{cm}^{-2} \). There is a further reduction in mean \( n_{\text{min}} \) with optimized SLEDGE gates to \( 1.4 \times 10^{10} \, \text{cm}^{-2} \). The means are statistically different with \( > 99\% \) confidence. The data implies a reduction in disorder by switching from overlapping or multi-plane gates, which have multiple dielectric deposits before gate patterning and limited pre-gate clean options, to uniplanar gates, which allow for more aggressive pre-deposition wet cleans.

We can further quantify potential disorder at the device level by analyzing single dot charge stability diagrams across wafers. One metric is to use the differential voltage between P- and neighboring T- or X-gates \( (V_P - V_T) \) at the first electron loading line, as shown in the inset of Fig. 3(b). We have found that the differential voltage scales exponentially with SiGe cap thickness as expected from solving Laplace’s equation for a pinned surface gate potential model [25]. This indicates that 1) across devices, the quantum well is tuned to approximately the same potential at the one-electron loading line, and 2) variations in the voltage difference to load one electron are due to potential disorder. For each wafer, we find the standard deviation (pooled by device) of all \( (V_P - V_T) \) differential biases from the wafer, which we use as a metric for disorder. In Fig. 3(b), we plot distributions of the pooled standard deviations (\( \sigma_p \)) for lift-off gates, SLEDGE gates with unoptimized pre-clean, and SLEDGE gates with optimized pre-clean. Only data from wafers with the same 60 nm SiGe cap thickness are plotted. As with \( n_{\text{min}} \), there is a statistically significant reduction \( (> 99\% \) confidence) in mean \( \sigma_p \) from lift-off gates to unoptimized SLEDGE gates of \( 0.34 \, \text{V} \) to \( 0.13 \, \text{V} \).

The mean for optimized SLEDGE gates is \( 0.12 \, \text{V} \), but it is not statistically different from that of unoptimized SLEDGE gates at the same confidence level, perhaps because of residual disorder in the gate stack itself. Regardless, the HB and charge stability diagram data both show a clear reduction in wafer-level electrostatic disorder for SLEDGE devices as compared to lift-off devices. Moreover, the SLEDGE \( \sigma_p \) means compare favorably to corresponding addition voltages \( \sim 40 \, \text{mV} \), see 3(b) inset).

Beyond the advantages in device design flexibility and disorder with the SLEDGE process, the technology also readily produces qubit devices capable of spin coherent operations. A representative set of charge stability diagrams from a 6-dot SLEDGE device recorded at 1.6 K is shown in Fig. 4(a), with one diagram for each adjacent plunger gate pair. Each diagram exhibits the canonical double dot honeycomb pattern with cells merging at higher electron occupancy due to tunnel barrier lowering [26]. Loading voltages for the most relevant \((0,1), (1,0), \) and \((1,1) \) charge configurations are all \( \leq 1 \, \text{V} \), and, with the exception of the outer dots, which experience enhanced cross-capacitance from the OFG, all loading voltages are similar to each other. This is a critical feature for proposed multiplexed cryogenic control [27].

Representative plots from each X-gate showing exchange \( (J) \) fringes as a function of neighboring P-P detuning \( (\Delta, \text{ordinate}) \) and exchange gate voltage \( (V_x, \text{abscissa}) \) are shown in Fig. 4(b). In these so-called “fingerprint” plots [28], which were measured at dilution refrigerator (DF) temperatures from the same device as in Fig. 4(a), the exchange frequency between inter-dot electrons increases with both tunnel coupling (controlled by \( V_X \)) and \( \Delta \). Fingerprint plots are used to determine the symmetric axis (vector in \( \Delta-V_X \) voltage space where \( J/\Delta \sim 0 \)) for reduced sensitivity to charge noise, and they indicate that a given double dot pair exhibits spin coherent exchange oscillations. Furthermore, single qubit blind randomized benchmarking (RB) data from an exchange-only encoded 3-dot SLEDGE device is shown in Fig. 4(c). In the blind RB sequence, the qubit is initialized in the spin singlet \( (|0\rangle) \), a sequence of \( N \) gates randomly selected from the Clifford group is applied, and a recovery Clifford returns the qubit ideally to the spin singlet or spin triplet \( (|1\rangle) \) [5]. The sum and difference of the \( |0\rangle \) and \( |1\rangle \) return probabilities as a function of \( N \) can be fit to exponential forms to extract per-Clifford error and leakage rates. For this particular device, we find per-Clifford error of \( 0.12 \pm 0.01\% \) and leakage of \( 0.035 \pm 0.011\% \).

In conclusion, we have demonstrated a flexible fabri-
cation process for Si/SiGe exchange-only qubits wherein dot-shaped gates and routing are defined on separate planes and are contacted with interconnect vias. The separation, in combination with electron-beam lithography, enables high customizability in materials and device designs, particularly toward non-conventional layouts. SLEDGE qubit devices have uniplanar gates with low electrostatic disorder compared to overlapping gate devices fabricated with lift-off metallization processes. Future work includes improved rf engineering of M1 and optical layer routing, as well as integration of micromagnets and superconducting resonators.

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FIG. S1. (A) Illustrations of a 2x3 dot device connected with 2 BEOL levels. Top-down is left, and dashed lines denote cut of cross-section on right. In the top-down image, M- and Z-gates are on the left between bath gates, a 3-dot is in the center, and another 3-dot is on the right. T-gates and IFG islands separate 3-dot columns. M1 connects to all perimeter gates and M2 connects to all interior gates. (B) Illustration of a 3-dot device with a micromagnet patterned on top. Top-down is left, and dashed lines denote cut of cross-section on right.

The ability to extend the SLEDGE gate layout and add additional device features is shown in Fig. S1. In Fig. S1(a) we show how a SLEDGE 2x3 quantum dot device, which is 3 rows of dots including the M- and Z-gates, can be connected by adding an additional BEOL level M2. The perimeter gates would be connected with M1 while the interior gates would be connected with M2. The M2 process and pitch could be nominally the same as that of M1, allowing for ease of extending the process flow. Such designs are enabled by the dot-shaped gates and interconnect process of SLEDGE. Similarly, we show in Fig. S1(b) how a micromagnet can be straightforwardly fabricated on a 3-dot device after M1 patterning. The micromagnet is drawn as in [1]. An additional dielectric layer (ILD2) could be deposited after M1 and the micromagnet could be optically patterned directly on top of ILD2 by lift-off or subtractive etch processes.
In Fig. S2 we show that uniplanar SLEDGE gates have greater exchange energy ($J$) dynamic range than overlapping gates as a function of X-gate voltage. The overlapping gates here are patterned by lift-off metallization. Exchange energy is calibrated by measuring exchange oscillation frequency on the symmetric axis [2] with fixed voltage pulse duration as a function of X-gate voltage. It can be seen in the figure that SLEDGE X-gates can achieve higher $J$ than overlapping X-gates for a given voltage throw. For example, at 40 mV offset, the exchange energy with SLEDGE gates is $>10 \times$ larger than with overlapping gates. In addition, the exchange energy in the absence of X-gate throw is lower with SLEDGE as compared to overlapping gates, which minimizes unintentional rotations during idle. The advantages of SLEDGE X-gates arise from reduced electric field screening from neighboring P-gates that do not overlap, as well as reduced dielectric material under X-gates with the uniplanar design.
In Fig. S3, we show the wafer-level reproducibility of e-beam lithography across lots for Si quantum dot fabrication, as measured by an automated critical dimension SEM (CDSEM) tool (Hitachi S9380). As stated in the main text, each lot in this work consists of four 75 mm wafers patterned in one exposure sequence on a single 200 mm wafer holder. Fig. S3(a) shows the measured diameter in e-beam resist of plunger gates from two devices with nominally 80 nm and 100 nm designed dot diameter. Although many devices are patterned on each wafer, we only measure the critical dimension (CD) from a small subset of devices and reticles. It is evident in the chart that the lot-to-lot variation in mean lithography CD is \(<7\%\) from the group mean.

Figs. S3(b-c) show the V01-gate and M1-V01 magnitudes of misalignment \(\sqrt{\Delta x^2 + \Delta y^2}\) across the same four lots. Misalignment was measured at V01 and M1 e-beam lithography steps using box-in-box (BIB) structures wherein an interior rectangle is patterned in the prior etch step and an external rectangle is patterned in the current lithography step. The offset of the interior rectangle from the exact center of the exterior rectangle is the local misalignment. The CDSEM can rapidly extract \(x\) and \(y\) misalignments from \(\sim100s\) of BIBs from each wafer. As seen in the figure, the mean misalignment magnitude for all lots is \(\lesssim5\) nm in both lithography steps. The standard deviations are \(\leq2.5\) nm for V01-gate BIBs and \(\leq3.5\) nm for M1-V01 BIBs. This level of misalignment across wafers and lots is well within the requirements necessary for SLEDGE devices, demonstrating that e-beam lithography is suitable for wafer-scale Si qubit fabrication.

In the main text we discuss how the SLEDGE device platform enables straightforward tuning of P- and X-gate dimensions across devices. Another design parameter that can be easily modified within-reticle is the distance between P- and M-gate rows. This dimension controls the sensitivity of M-gate charge sensors to electrons under corresponding P-gates (i.e. measurement signal-to-noise ratio). If the M-P distance is too narrow, the Coulomb interaction from electrons under either M- or P-gates can adversely affect charge manipulation or sensing by the other, respectively. In Fig. S4, we show top-down SEM images of two devices patterned within one reticle with M-P distance of 140 nm and 200 nm but all other dimensions fixed. The M1 (and V01) pattern is easily adjusted in accordance with the gate-level design change.
FIG. S5. (A) Top-down SEM images of M1 patterned by a subtractive etch process. Scale bar corresponds to 1 µm. (B) Cross-section TEM image of a SLEDGE device with subtractive M1. The dark area on top of vias is W in M1, and the conformal gray layer over M1 is a protective SiNx encapsulation layer.

The SLEDGE gate process can be used with a variety of BEOL integration schemes. In Fig. S5 we show top-down SEM and cross-section TEM images from a subtractive etch process. In this process, immediately after V01 etch, vias are filled by ALD TiN followed by blanket tungsten (W) sputter deposition. Then the bilayer TiN/W stack is patterned by e-beam lithography and subtractively etched to form M1. W serves as a low resistivity normal metal in the case that TiN superconductivity is broken by an applied magnetic field or by narrow linewidth. The subtractive process is advantageous over dual damascene because vias are filled immediately after etch, which avoids contamination in vias leading to poor via-gate connectivity. Via-gate connectivity is discussed further below.

FIG. S6. (A) Charge stability diagram near boundary of (0,0) and (1,1) cells showing charging lines from parasitic metal dots. (B) Gate-level PMD rate as a function of cryoprober mean via resistance. Each data point represents one wafer.

In integrated circuits designed to operate at room temperature, a poor (non-Ohmic) connection between a via and a lower level metal feature may manifest as a high series resistance or open circuit. In cryogenic quantum dot devices, an additional phenomenon may occur wherein a poorly connected gate acts as a floating quantum dot and electrons tunnel into the dot from vias across the non-Ohmic barrier. This can be observed in charge stability diagrams as additional discrete, faint charging lines with slopes incommensurate with P-gate electron loading and with small addition voltages (Fig. S6(a)). We denote this phenomenon “parasitic metal dots” (PMDs), and it is considered a device failure if any gate exhibits PMDs. We have developed a proxy metric for gate-level PMD rate based on via resistance measured by cryogenic on-wafer probing, which can provide more statistically meaningful wafer- and lot-level trends.
In our fab-test workflow, after device fabrication but before 1.6 K electrostatic screening, whole wafers are electrically tested in a \( \sim 40 \) K automated on-wafer probing system (Cascade PAC200 with Celadon Systems probe card). A representative subset of all devices on a wafer are pre-screened for isolation (\( \leq 100 \) pA at 1 V) between all nearest-neighbor gates. Other process control monitors such as Hall bars, capacitors, sheet resistance structures, transfer length method structures, via resistance structures, etc. are also measured. This “cryoprober” test provides a rapid (\( \sim 1 \) d) method for selecting plausibly good devices for further low temperature testing. After die singulation, devices that were fully isolated in cryoprober measurements are packaged and wirebonded for 1.6 K screening.

We can compare the mean via resistance measured per wafer in cryoprober against the gate-level rate of PMD observations in 1.6 K screening per wafer, as shown in Fig. S6(b). The PMD rate is \( \sim 0 \) % at low cryoprober via resistance and it nears \( \sim 90 \) % at high via resistance. Based on the number of nanoscale gates in a 6-dot device (20), the gate-level PMD rate should be as close to 0 % as possible to not substantially impact device yield. Based on the figure, we set a specification for SLEDGE cryoprober via resistance at 3 k\( \Omega \). In this manner, we can easily identify at cryoprober whether a wafer is expected to have a low PMD rate without having to use resources singulating die, packaging die, and measuring only finite number of devices at 1.6 K. While in principle it should be possible to achieve low via resistance with any BEOL integration scheme, with our toolset we have had the greatest success with the subtractive process described above.

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