Hardware Design of Multichannel Video Acquisition System Based on FPGA

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Abstract. A hardware design of multi-channel video acquisition system is designed, we propose system based on FPGA Cyclone V chip, The A/D conversion of analog video signal is accomplished through high-speed parallel AD chip LTC2202 of LINEAR Company. In the process of image data acquisition, SDRAM is used for data caching in image processing. From capacity and reading and writing speed analysis, 2 pieces of MICRON Company’s 32 bit wide MT48LC2M32B2B5 are selected, and the capacity is 64Mb, The Cameralink interface is selected as the interface between FPGA and image data transmission of external system. There is reserved communication with external control signals, sending control signals by TI Company DS90LV047. The system collects the image data from the front end through the A/D, caches the SDRAM and outputs the image through Cameralink to achieve the high speed and high efficiency of the data transmission. The hardware realizes the data acquisition and transmission of the multi-channel target image.

1. Introduction
With the rapid development of digital electronic technology [1-3], high precision and multi-channel image data acquisition system [4, 5] has occupied the main position in the field of measurement and control, and is widely used in various fields such as industrial [6], people's livelihood [7, 8] and so on. The measurement items are mainly compressed image data and image data, remote control and telemetry related parameters [10], and later used for data analysis, system improvement and so on. There are many systems of data measurement and acquisition, but many systems have such problems as single function, few acquisition channels, low sampling rate, complex operation, and higher requirements for the test environment. People need a high-speed data acquisition system with wide application and high cost performance. Multichannel video acquisition based on FPGA will come from the acquisition of analog signals through the A/D converter, processing, caching and transmission by FPGA, realizing multi-channel data acquisition, powerful data processing function, high cost performance and wide application.

2. Overall design of the system
The multi-channel video acquisition card mainly consists of 4 A/D converter module, FPGA signal control module, power management module, data storage module, LVDS communication module and
Cameralink image output module. The hardware composition block diagram of the system hardware is shown in Figure 1. The hardware design of the multi-channel video acquisition system is that the front end 4 ADC can collect the simulated image or video signal of the external input in real time. The SDRAM cache module is used to cache the image data into a complete image information or a complete frame of video information is sent to the upper computer by the Cameralink output module. The FPGA control module is finished. With the control of each module, the control parameters of the image acquisition can be adjusted by the LVDS communication module, and the image parameters can be sent to the upper computer by the LVDS communication module. The power module mainly completes the conversion of external input power to the acquisition card system, requiring various levels.

Figure 1. Block diagram of multi-channel video acquisition system

3. Hardware circuit of data acquisition system

3.1. FPGA control module circuit
On the image processing board, FPGA is selected as the processor. Considering the application requirements, the development cycle, the technology accumulation and the economy, the 5CEFA9 of the cyclone V series of ALTERA company is selected as the control chip of the system. The silicon chip has a lot of system level hard core functions - dual core ARM Cortex-A9 hard core processor system (HPS), embedded peripherals, multi port memory controllers, serial transceivers and PCIe ports, and its main parameters are shown in Table 1.
Table 1. SCEA9 performance parameters

| Core Voltage | LE(k) | ALM | register | M10k memory module | M10k storage (Kb) | MLAB storage (Kb) | Precision adjustable DSP module | 18x18 Multiplier | Global clock network | PLL | Support I/O level voltage (V) | Supported I/O standards | LVDS channel (receiver / transceiver) | Hard core storage controller | Supported storage devices |
|--------------|-------|-----|----------|-------------------|------------------|------------------|-------------------|-------------------|---------------------|-----|--------------------------|------------------------|--------------------------|--------------------------|--------------------------|
| 1.1V         | 301   | 113560 | 454240   | 1220              | 12200            | 1717             | 342               | 684               | 16                  | 8   | 1.1, 1.2, 1.5, 1.8, 2.5, 3.3 | LVTTL, LVCMOS, PCI, LVDS | 120/120                  | 2                        | DDR3, DDR2, LPDDR2 |

3.2. High speed parallel A/D circuit
The ADC conversion module selects LINEAR's high-speed parallel AD chip LTC2202 to complete the A/D conversion of analog video signals. The integrated circuit is mainly used in the imaging system. The LTC2202 are 25Msps/10Msps, sampling 16-bit A/D converters designed for digitizing high frequency, wide dynamic range signals with input frequencies up to 380MHz. The input range of the ADC can be optimized with the PGA front end. The LTC2202 are perfect for demanding applications, with AC performance that includes 81.6dB SNR and 100dB spurious free dynamic range (SFDR). Maximum DC specs include ±4LSB INL, ±1LSB DNL (no missing codes). The typical application is shown in Figure 2.

![LTC2202 typical application](image)

Figure 2. LTC2202 typical application

3.3. SDRAM circuit design
SDRAM is used for data cache in image processing. From the analysis of capacity and read and write speed, 2 MICRON 32 bit wide MT48LC2M32B2B5 with capacity of 64Mb are selected. The 64Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 67,108,864 bits. It is
internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). The SDRAM provides for programmable read or write burst lengths (BL) of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The schematic diagram of the circuit design is shown in Figure 3.

Figure 3. SDRAM schematic diagram

3.4. Cameralink interface circuit

The Cameralink interface is the interface between FPGA and image transmission of the external system, and adopts the DS90CR285 chip of TI Company. The DS90CR285 transmitter converts 28 bits of LVCMOS/LVTTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. The DS90CR286 receiver converts the LVDS data streams back into 28 bits of TTL data. At a transmit clock frequency of 66 MHz, 28 bits of TTL data are transmitted at a rate of 462 Mbps per LVDS data channel. Using a 66 MHz clock, the data throughput is 1.848 Gbit/s (231 Mbytes/s). The schematic diagram of the circuit is shown in Figure 4.
3.5. **Differential amplifier circuit**

The multi-channel video capture system contains 4 channels of LVDS differential signal output, using TI's DS90LV047. The DS90LV047A device is a quad CMOS flowthrough differential line driver designed for applications requiring ultra-low power dissipation and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) using Low Voltage Differential Signaling (LVDS) technology. The DS90LV047A accepts low voltage TTL/CMOS input levels and translates them to low voltage (350 mV) differential output signals. In addition, the driver supports a TRI-STATE function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low idle power state of 13 mW typical. Circuit design figure 3, It is used for output of image data or output of control signal.

![Figure 4. Cameralink interface circuit](image)

![Figure 5. Schematic diagram of differential output DS90L047 circuit](image)
4. Experimental Result
The hardware system of multi-channel video acquisition board is designed as shown in Figure 6, and the A/D conversion of analog video signal is completed by four road high-speed parallel AD chip LTC2202, cyclone V FPGA as the main control core, Cameralink output interface as the system image output interface, Cameralink clock rate is 66MHz. Auxiliary peripheral other interface communication unit to complete the communication function.

![Figure 6. Hardware system of multi-channel video acquisition board](image)

5. Conclusion
This system uses Altera cyclone V series low power, low cost, programmable logic controller to design a multi-channel video acquisition board hardware system. The hardware circuit design has multi-channel video acquisition function, rich peripheral interface and protection function. It has good application prospect.

Acknowledgments
This work was financially supported by the CAS “Light of west China” fund. (No.XAB2015B21).

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