Pre-charge solution for low-power, area-efficient SAR ADC

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Abstract: In this paper, a new method is proposed to reduce the power consumption and occupied area of successive-approximation register analog to digital converters (SAR ADCs). The proposed solution is based on pre-charged capacitor array consisting of identical unit capacitors. According to the new method, switching operations to determine the least significant bits are replaced by adding pre-charged capacitors to the main capacitor array. This method is applicable for binary-weighted capacitor arrays with different switching schemes. With the presented method, switching energy and the number of unit capacitors are reduced by at least 50%.

Keywords: SAR ADC, switching algorithm

Classification: Integrated circuits

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1 Introduction

SAR ADC is the most popular architecture for low-power, medium-resolution applications. However the conventional SAR ADC occupies a large chip area owing to the large number of unit capacitors for its digital to analogue converter (DAC). And also considerable switching energy is consumed during conversion. Recently, several switching schemes have been presented to reduce the switching energy and/or chip area such as [1, 2, 3, 4, 5, 6, 7]. In this letter, a new solution is proposed which reduces drastically the dynamic power consumption and occupied area of the SAR capacitor arrays. The presented method is applicable for binary weighted C-DACs with different switching schemes. Here, for example, it is applied to the DAC with Vcm-based switching which is one of the popular switching algorithms [1]. It is reference of many other proposed schemes such as [3, 4, 5]. The operation of the proposed ADC is described in the following Section.

2 Proposed DAC

In order to clarify the proposed method, the C-DAC array is broken down to two arrays as MSB-array and LSB-array. The resolution of each array depends on applied division by designers. The proposed DAC for a 6-Bit SAR-ADC is illustrated in Fig. 1 which its first three bits are extracted by MSB-array and last 3 bits are detected by adding LSB-array capacitors. For MSB-array, binary-weighted capacitor-array with common-mode based switching algorithm is used and For LSB-array, an identical capacitor-array is proposed which are pre-charged before their operation phase. In addition, a unit capacitor is needed as auxiliary capacitor to help in pre-charging procedure if it is determined more than one LSB to extract by LSB-array.

![Fig. 1. The proposed 6-bit SAR-ADC.](image)

Initially, the input signal is sampled on the capacitors of MSB-array. Simultaneously, two unit capacitors of LSB-array are pre-charged to Vcm and other capacitors are discharged as shown in Fig. 2. Next, a coarse quantization is performed to determine the first 3 bits using only the MSB-DAC which its operation is based on the main switching algorithm which is described in [1] for this case. This conversion time, which MSB array is active, is named as MSB phase.
and the next phase to determine fine quantization is named as LSB phase. As shown in Fig. 3, during the MSB phase, LSB-DAC capacitors are connected together in consecutive cycles to produce required pre-charged capacitors for fine quantization by charge sharing. Thus, it does not need any extra cycles to pre-charge LSB-array. Assuming ‘10’ as the first two bits, MSB-array and LSB-array status at the end of MSB phase is shown in Fig. 4, a.

![Fig. 2. Sampling phase. a) MSB-array. b) LSB-array.](image)

![Fig. 3. Pre-charge of LSB-array during 3 cycles of MSB phase.](image)

For the fine quantization, pre-charged unit capacitors are, consecutively, connected to the MSB-DAC based on the prior extracted bit. The operation of LSB-DAC is shown in Fig. 4, b. for example the 3rd extracted bit is ‘1’ then a unit capacitor pre-charged to the Vcm is connected to the lower side at the 4th conversion cycle and a unit capacitor without charge is connected to the higher side. Assuming ‘00’ as the 4th and 5th bits, unit capacitors pre-charged to Vcm/2 and Vcm/4 are added at 5th and 4th conversion cycles, respectively. DAC array status at these cycles is shown in the Fig. 4, b. Based on proposed scheme, for an N-bit which consists of m-bit MSB-DAC and (N-m)-bit LSB-DAC, the overall DAC output (comparator input) in each conversion cycle ‘i’, which is shown by $V_{out,i}$, can be calculated by following equation.

$$V_{out,i} = -V_{in} + \frac{\sum_{j=1}^{i-1}(2D_j - 1)C_j V_{ref}}{C_0 + \sum_{j=1}^{i-1} C_j}, \quad i = 2, 3, \ldots, m$$  \hspace{1cm} (1)

$$V_{out,i} = \frac{2^{m-1}}{2^{m-1} + (i - m)} \left( -V_{in} + \frac{\sum_{j=1}^{i-1}(2D_j - 1)V_{ref}}{2^j} \right), \quad i = (m + 1), \ldots, N.$$  \hspace{1cm} (2)
As illustrated in Eq. (1), DAC output at MSB phase \((i \leq m)\) is same as conventional Vcm-based switched DAC output. For LSB phase \((i > m)\), there is an attenuation factor which effects on both input voltage and DAC value as shown in Eq. (2). Since this attenuation does not effect on direction of comparator input voltage, it does not cause error in comparator output. However the attenuation factor leads to decrease the LSB value with the same coefficient which means a comparator with higher resolution is needed. Of course the calculated factor in Eq. (1) depends on ‘\(m\)’ value. For example for a 10 bit ADC this factor is 0.998 and 0.761 for \(m = 9\) and \(m = 5\), respectively. Thus the extra resolution required for comparator is less than \(1/2\) LSB even for \(m = 5\).

As explained in the above, the proposal solution leads to decrease the number of unit capacitors. Therefore reduction of switching energy and DAC area resulted from total capacitance reduction. However there is a limiting factor of thermal noise, \(KT/C\), which should be considered in using the proposal solution. Hence, the proposed pre-charge solution is an effective method if the total capacitance is larger than thermal noise limitation.

Fig. 4. a) The status of C-arrays at the end of MSB phase. b) Switching operation during LSB phase.
3 SAR switching energy

The behavioural simulations of Vcm-based switching technique before and after applying the proposed scheme for a fully differential 10-bit SAR ADC were performed in MATLAB and the results of switching energy against the output codes are illustrated in Fig. 5. Due to the large capacitance with large voltage transition steps at the input of the comparator, most of the consumed switching energy in SAR ADCs refers to the first several conversion cycles. In the proposed architecture, the number of unit capacitors involved in the first conversion steps is decreased owing to use lower resolution DAC as MSB-array. Further, using identical capacitors instead of binary weighted capacitors as LSB-array causes considerable reduction in the occupied area.

The efficiency of presented method is summarized in Table I. Only by detecting one bit with the proposed pre-charged unit capacitor without adding any complexity, the switching energy and DAC area are decreased by 49.8%. In compared with conventional SAR ADC, this reduction means 93.74% and 75% energy and area saving, respectively. As more bits are determined by pre-charged capacitors, more energy saving and area reduction is achieved.

Table I. The effect proposed method for different division of MSB and LSB resolution for a 10-bit SAR ADC with Vcm-based switching.

| m | l | Average switching energy (CVref2) | Energy saving | Area reduction |
|---|---|----------------------------------|---------------|---------------|
| 10 | 0 | 170.17                          | ref           | ref           |
| 9  | 1 | 85.33                           | 49.85%        | 49.8%         |
| 8  | 2 | 43.15                           | 74.64%        | 74.6%         |
| 7  | 3 | 22.26                           | 86.91%        | 86.71%        |

Fig. 5. Switching energy versus output codes of a 10-bit ADC with different number of MSB bits (m).
4 Conclusion

A new solution is proposed for SAR ADC to decrease the number of unit capacitors of DAC array which is applicable to binary weighted C-DACs with different switching algorithms. Compared to the main DAC (before applying new solution), the proposed method leads to reduce switching energy and occupied area by at least 50%.