Design, Engineering and Optimization of a Grid-Tie Multicell Inverter for Energy Storage Applications

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Multilevel converters have found many applications within renewable energy systems thanks to their unique capability of generating multiple voltage levels. However, these converters need multiple DC sources and the voltage balancing over capacitors for these systems is cumbersome. In this work, a new grid-tie multicell inverter with high level of safety has been designed, engineered and optimized for integrating energy storage devices to the electric grid. The multilevel converter proposed in this work is capable of maintaining the flying capacitors voltage in the desired value. The solar cells are the primary energy sources for proposed inverter where the maximum power density is obtained. Finally, the performance of the inverter and its control method simulated using PSCAD/EMTDC software package and good agreement achieved with experimental data.

Index Terms—Multicell inverter; Grid-tie multilevel inverter; Maximum Power Point Tracking; Flying capacitor; Energy storage devices.

I. INTRODUCTION

The application of renewable energy sources (i.e. solar wind energy) into an electric grid requires high performance energy storage devices along with various types of power electronics (i.e. rectifiers, converters and inverters). Figure 1 includes the schematic of a hybrid energy storage system in which a renewable energy source (here photovoltaic modules) along with an energy storage device has been implemented to the electric grid via the utilization the multilevel inverters [1], [2], [3].

As shown in Fig. 1, battery-based devices and hydrogen-based energy storage technologies are promising. A good review on the battery- and hydrogen-based energy storage has been provided recently [4]. For hydrogen based energy storage, an electrolyzer along with a polymer electrolyte membrane (PEM) fuel cells are utilized. Although being very promising, the water management for electrolyzers and PEM fuel cells remains a challenging issue to be addressed [5], [6]. Also, the hydrogen gas storage technologies and infrastructure for regenerative hydrogen fuel cell systems is required to be addressed appropriately [7], [8]. Several battery technologies are developed for energy storage technologies that redox flow batteries are among the most promising devices. However, engineering the redox flow batteries for optimum operation requires detailed mathematical models [9], [10], [11] and experimental diagnostics [12], [13].

The application of multilevel converters for the renewable energy systems has been increased recently [14], [15], [16], [17]. This is mostly because of high energy output (in the range of MW), high efficiency and low electromagnetic interference being offered via their application [18], [19], [20].

Three-level converter first proposed by Nabae [21] and the converters with increased number of levels developed later to obtain higher levels of voltage and reduce the harmonic content of the output voltage. However, increasing the number of voltage levels results in increased system complexity and severe voltage balancing problems. Different topologies for these types of converters have been utilized including Neutral Point Clamped (NPC) and variant types of multicell inverters [22], [23], [24]. The NPC topology suffers from diode clamped and capacitor voltage balancing issues where the multicell
TABLE I: Comparison of different inverters components

| Type   | # DC Sources | Magnitude | # Switches | # Capacitors |
|--------|--------------|-----------|------------|--------------|
| CM     | n            | $E/n$     | $4n$       | 0            |
| FCM    | 2            | $E$       | $4n$       | $2n - 1$     |
| SM     | 2            | $E$       | $4n$       | $(2n - 1)$   |
| DFCM   | 1            | $E$       | $2n + 2$   | $n - 1$      |

inverters do not suffer from the same issue. Therefore, multicell inverters are promising candidates to generate increased voltage levels for high power generation applications. The multicell inverters have different types including the Cascaded Multicell (CM), Flying Capacitor Multicell (FCM) and Stacked Multicell (SM) inverters [25], [26], [27]. The FCM inverters along with the SM inverters have many unique advantages for medium voltage applications such as operation without transformer and naturally capacitor voltage balancing ability. A comparison of the different components being used with these different inverters for generating levels had been provided in Table I.

Table I. comparison of different inverters components

The advantages of DFCM compared to conventional structures are eliminating the common point of DC sources, reducing the number of input DC sources, switches and capacitors. However, this structure is an island and in the grid-tie form of this inverter with presented control method, some difficulties arise including the power transfer from grid to input source and the possibility of discharging flying capacitors in case of connecting to the Photovoltaic (PV) cells. In this paper a new topology for grid-tie multicell inverter has been developed. The proposed inverter has been designed based upon the DFCM inverter and accordingly shares the common advantages associated with the DFCMs including the elimination of common point of DC source, reduced number of DC sources and increased number of voltage levels. Also, the new design assures higher level of safety and via its utilization, the common problems related to the DFCMs has been eliminated (while extracting the maximum power from PV cells).

II. PROPOSED MULTILEVEL INVERTER

The proposed inverter is shown in Fig. 2. In this structure independent of the number of inverter cells and generated voltage levels, only the switches $S_n$ and $P_n$ in cell$_n$ are bidirectional. The oscillations of the PV cells voltage is mostly caused by climatic oscillations. In case of low PV cells and because of the cascaded diode of PV cells would not be functional and therefore, the possibility of discharging flying capacitors or grid voltage on the PV cells increases. Discharging the grid in the positive half cycle, the negative half cycle and discharging the flying capacitors are shown in Fig. 3. According to Fig. 3, in the proposed inverter, by using only two bidirectional switches, there would be no chance of discharging the grid and the flying capacitors on the PV cells.

Table II. includes the switching states within the proposed inverter for generating 5-level output voltage. In this table, when the switch is on, the corresponding state number is one and for the off position it is zero. Also X in this table due to modes of charging or discharging of flying capacitor $C_1$, is either one or zero. Based on this table, in the states 2 and 4, charging or discharging of $C_1$ happens naturally, while in the other states, due to value of $X$, $C_1$ can be charged. The voltage balancing algorithm of $C_1$ in positive half cycle is shown in Fig. 3. Based on this figure, if the measured value of voltage of capacitor $C_1$ is lower than its set value ($v_{C1}$), $P_2$ (or $S_2$) will be on in the state 1 (or 3). This can continues until the voltage of $C_1$ reaches its specified value then $P_2$ will be off.

III. PROPOSED CONTROL METHOD

In the control method, it is assumed that the inverter output current tracks the favorite sinusoidal reference current. Also as it is shown in Fig. 5, it is assumed that the proposed inverter (base on IEEE 1547 standard) does not exchange any reactive power with the grid and only active power exchanges, therefore:

$$v_n(t) = V_m \sin (wt) \quad (1)$$

$$i_r(t) = I_m \sin (wt) \quad (2)$$

Fig. 2: (a) Proposed grid-tie multicell inverter and (b) Proposed 5-level grid-tie multicell inverter.

TABLE II: Switching states in the proposed inverter

| States | $S_1$ | $S_2$ | $S_3$ | $P_1$ | $P_2$ | $P_3$ |
|--------|-------|-------|-------|-------|-------|-------|
| 1      | 1     | 1     | 1     | 0     | X     | 0     |
| 2      | 1     | 0     | 1     | 0     | 1     | 0     |
| 3      | 1     | 1     | 0     | 0     | X     | 1     |
| 4      | 0     | 1     | 0     | 1     | 0     | 1     |
| 5      | 0     | X     | 0     | 1     | 1     | 1     |
Fig. 3: (a) Discharging the grid in the positive half cycle, (b) Discharging the grid in the negative half cycle and (c) Discharging the flying capacitors.

Fig. 4: Algorithm of charge and discharge of capacitor in the positive half cycle of output voltage.

Figure 6 shows five output voltage levels that have been considered for the proposed inverter. The proposed control method should be capable of injecting power from inverter to grid at different operating conditions and therefore, the maximum voltage generated through the inverter \( E_1 \) should be greater than the grid’s maximum voltage \( V_m \).

Due to generating output voltage with low Total Harmonic Distortion (THD), the values of output voltages are considered as follows:

\[
E_2 = \frac{E_1}{2}, \quad E_3 = 0, \quad E_4 = -\frac{E_1}{2}, \quad E_5 = -E_1
\]

The grid voltage and reference current is calculated according to (4) and (5) assuming the circuit current in the constant \( t_k \) is \( i_s(t_k) \):

\[
\begin{align*}
v_s(t_k) &= V_m \sin (wt_k) \\
i_r(t_k) &= I_m \sin (wt_k)
\end{align*}
\]

The equivalent circuits of the proposed inverter are shown in Fig. 7.

In Fig. 7, \( R_l \) and \( L_l \) are the line resistance and inductance between inverter and grid and \( V_0 \). According to Fig. 7(a):

\[
L_1 \frac{di_s(t)}{dt} + R_l i_s(t) = V_0 + v_s(t) = V_0 + V_m \sin (wt)
\]
In constant \( t_k \), \( i_s(t_k) \) is measured. Control system using (8), calculates five current for a five-level output voltage of inverter during the next switching period. Therefore, for five output voltage levels, five cost functions can be written as follow:

\[
\Delta I = |i_r(t_k + T_s) - i_s(t_k + T_s)|
\]  

From (12), proper switching state and consequently proper output voltage can be applied. Initially, when the inverter connects to the network, the initial voltage of the capacitor is zero. At this point, no impulse current is drawn until the capacitor voltage reaches the proper value where the grid current is bypassed by \( S_1, S_2 \) and \( P_3 \) and simultaneously input source charged the capacitor by \( S_2 \) and \( P_2 \). When the capacitor voltage reaches its proper value, control method will follow their normal operation. In Fig. 8(a) and (b), upper waveforms are inverter output voltage and the lower waveforms are the inverter output current. Based on Fig. 8(a), if the initial control method does not apply, 60% of the original period (0.012 seconds) would be required for inverter to reach its own stable performance. This situation also results in over-drawn current as high as four times of the maximum nominal current through the circuit, which potentially damages the whole circuit. However, this situation has improved in Fig. 8(b) where the response time has decreased to about 0.0005 seconds. Therefore, the inverter only requires approximately 2.5% of the original period to reach its own stable performance. Also in this case, the drawn current is within the safe range.

**IV. FLYING CAPACITOR VOLTAGE BALANCING METHOD**

In this section, the method of capacitor voltage balancing is investigated. Based on Table II, the capacitor is discharged in the duration that output voltage equals to \( E/2 \) with positive current of circuit and output voltage equal to \( -E/2 \) with negative current of circuit. Based on the equivalent circuit of capacitor discharging states (Fig. 7(b) and (c)):

\[
\begin{align*}
    v_s(t) &= V_m \sin (wt) \\
    i_s(t) &= I_m \sin (wt) \\
    v_s(t) &= V_c(t) + L_i \frac{di_L(t)}{dt} + R_i i_s(t) \\
    v_c(t) &= \sqrt{(V_m - R_i I_m)^2 + (L_i I_m)^2} \sin(\omega t + \arccos(\frac{-L_i I_m}{\sqrt{(V_m - R_i I_m)^2 + (L_i I_m)^2}}))
\end{align*}
\]

Fig. 7: (a) Equivalent circuit of the system, (b) Equivalent circuit of capacitor discharging state, (c) Equivalent circuit of capacitor discharging state and (d) Equivalent circuit of capacitor charging.
$E$ or zero, charging of capacitor is controlled by switch $P_2$ and within the range that output voltage is equal to $-E$ or zero, charging of capacitor is controlled by switch $S_2$. The capacitor charging circuit in all five modes is shown in Fig. 7(d). In this figure, $R_s$ is the resistance of switches per current loop, therefore the following equations for a capacitor charging state can be obtained:

$$E = R_s i_c(t) + v_c(t)$$  \hspace{1cm} \text{(17)}

$$i_c(t) = e \frac{dv_c(t)}{dt}$$  \hspace{1cm} \text{(18)}

$$v_c(t_1) = V_1$$  \hspace{1cm} \text{(19)}

$$v_c(t) = E + \frac{V_1 - E}{e^{\frac{t}{t \cdot \text{max}}}}$$  \hspace{1cm} \text{(20)}

In the (17) and (18), $v_c(t)$ and $i_c(t)$ are the voltage and current of capacitor respectively. The value of $R_s$ is very small, therefore the time of capacitor charging is short and capacitor is charged rapidly. However, capacitor discharging state is a swinging relation. Thus, capacitor voltage can be adjusted to the desired value just by controlling the charging state of capacitor voltage.

V. DETERMINATION OF CAPACITANCE OF FLYING CAPACITOR

The capacitor charging and discharging states is shown in Fig. 7(b)-(d). The value of $R_s$ is very small, therefore the time of capacitor charging is short and capacitors capacitance determination is applied only for discharging state of capacitor.

$$i_c = \frac{\Delta V_c}{\Delta t}$$  \hspace{1cm} \text{(21)}

Here, $\Delta t$ is the time of single switching duty cycle. $\Delta V_c$ is the capacitor rated voltage drop in one switching duty cycle which is assumed five percent of capacitor rated voltage. Consequently:

$$T_s = \Delta t$$  \hspace{1cm} \text{(22)}

$$\Delta v_c = \frac{5E}{2}$$  \hspace{1cm} \text{(23)}

Circuit current in Fig. 7, ($i_s$), is the sine wave that can be formulated as follow:

$$i_s = i_m \sin (wt)$$  \hspace{1cm} \text{(24)}

$i_c$ in (21) is equal to maximum value of current in (24), $I_m$, and therefore (25) is utilized to calculate the capacitors capacitance.

$$c = \frac{i_c \Delta t}{\Delta v_c}$$  \hspace{1cm} \text{(25)}

VI. MPPT IN THE PROPOSED INVERTER

Maximum power of PV cells in any constant is shown by $P_{PV}$. The efficiency of the system is $\eta$, the output is $P_{ac}$. Therefore:

$$P_{ac} = \eta P_{pv}$$  \hspace{1cm} \text{(26)}

And:

$$P_{ac} = V_s I_s$$  \hspace{1cm} \text{(27)}

Here, $V_s$ and $I_s$ are the RMS value of grid voltage and current respectively. Therefore, if one assigns any values for $P_{PV}$ and $V_s$, the appropriate value for $I_{ref}$ capable of tracking $I_s$ determined and this guarantees the maximum output power from solar cells.

VII. VOLTAGE LOSS CALCULATION

In this section, the loss calculation has been done for the proposed topology. The loss calculation contains switches losses and capacitor losses.

A. Switches losses

Mainly conduction and switching losses are calculated for switches. Every power switch contains a transistor (MOSFET) and a diode, and therefore, the instantaneous conduction loss of these elements is calculated using (28) and (29), respectively [21]:

$$P_{c,T} = |RT_i(t)|i(t)$$  \hspace{1cm} \text{(28)}

$$P_{c,D} = |V_D + R_D|i(t)$$  \hspace{1cm} \text{(29)}

Where $V_D$ is considered as forward voltage drop of the diode. $R_T$ and $R_D$ are equivalent resistance of the transistor and diode. At any time $N_T(t)$ transistor and $N_D(t)$ diodes are in current path, so the average conduction power losses can be written as:

$$P_c = \frac{1}{2\pi} \int_0^{2\pi} [N_T(t)P_{c,T}(t) + N_D(t)P_{c,D}(t)]dt$$  \hspace{1cm} \text{(30)}

The switching losses occur during turn on and turn off period of switches. For simplicity, the linear approximation of voltage and current of switches during the switching period is considered. Based on this assumption, the switching loss is calculated as follows:

$$E_{off,J} = \int_0^{t_{off}} (v(t)i(t))dt =$$

$$\int_0^{t_{off}} [(\frac{V_{sw,i}}{t_{off}})(-\frac{I''(t-t_{off})}{t_{off}})]dt = \frac{1}{6} V_{sw,J}I''t_{off}$$  \hspace{1cm} \text{(31)}

$$E_{on,J} = \int_0^{t_{on}} (v(t)i(t))dt =$$

$$\int_0^{t_{on}} [(\frac{V_{sw,i}}{t_{on}})(-\frac{I'(t-t_{on})}{t_{on}})]dt = \frac{1}{6} V_{sw,J}I'_{on}$$  \hspace{1cm} \text{(32)}
$E_{off,J}$ and $E_{on,J}$ are turn off and turn on loss of the switch $J$. $I_J$ is the current through the switch before turning off, $I_J$ is the current through the switches after turning on and $V_{sw,J}$ is the off-state voltage on the switch. The switching power loss is equal to the sum of all turns off and turns on energy losses in the fundamental frequency of the output voltage; as a result, average switching power loss can be calculated as follow:

$$P_{sw} = f \sum_{J=1}^{N_{sw}} (\sum_{k=1}^{N_{on,J}} E_{on,Jk} + \sum_{k=1}^{N_{off,J}} E_{off,Jk})$$

(33)

$f$ is the fundamental frequency, $N_{on,J}$ and $N_{off,J}$ are the number of turning on and off the $J$th switch during fundamental frequency. $E_{on,Jk}$ is the energy loss of the $J$th switch during the $k$th turning on and $E_{off,Jk}$ is the energy loss of the $J$th switch during the $k$th turning off.

B. Capacitor losses

The capacitor losses consist of capacitor voltage ripple losses $P_{rip}$ and conduction losses $P_{cond}$. The voltage ripple of capacitor is calculated as follow:

$$\Delta V_{rip} = \frac{1}{C} \int_{t_-}^{t_+} i_C dt$$

(34)

Where $i_C$, the transient current of the capacitor, equals to the line current. $t_-$ to $t_+$ is the interval that the capacitor is connected in series with DC voltage sources. So, voltage ripple loss is written as follow:

$$P_{rip} = C \Delta V_{rip}^2 f$$

(35)

$f$ is the frequency of the output voltage. The conduction losses can be written as follow:

$$P_{cond} = 2f \int_{t_-}^{t_+} r_C i_C^2 dt$$

(36)

Where $r_c$ is the internal resistance of the capacitor. Total loss of the proposed topology is equal:

$$P_{loss} = P_C + P_{sw} + P_{rip} + P_{cond}$$

(37)

Finally, the efficiency of converter is written as follow:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{in} - P_{loss}}{P_{in}}$$

(38)

Where $P_{out}$ and $P_{in}$ are output power and input power of converter.

VIII. SIMULATION RESULTS AND EXPERIMENTAL VERIFICATION

The simulation has been done by PSCAD / EMTDC. The circuit used in the simulation and the experimental set up and the value of elements used in both of them are shown in Fig. 9 and Table III. Due to the limitation of laboratory components, DC voltage source is used instead of PV cells.

For further analysis of inverters performance, input DC voltage source is changing from 60 V to 65 V in 0.04 s and from 65V to 55 V in 0.06 s, the results are shown in Fig. 10. According to Fig. 10, the proposed inverter with proposed control method produces 5-level voltage and tracks the reference current properly in the variation of DC source. Also, Flying capacitors voltage is balanced in its specified value (half of the input DC source).

In the experimental circuit, inverter output voltage and current for 5-level output voltage is shown in Fig. 11. This figure indicates that the proposed inverter produces an output voltage waveform with 5 levels with maximum output level of 60 V. Also in this inverter, output current of approximately 2 A tracks the reference current properly that is in phase with grid voltage, therefore the proposed inverter can exchange active power with the grid. In the laboratory condition the measured output and input power are about 48 (W) and 52.8 (W), respectively. Therefore, the efficiency is equal 90.91%. Based on the efficiency calculation, it is about 91.13%. Accordingly, the computed efficiency has good accordance with
 Fig. 10: Input DC source (E), grid voltage (Vs), inverter output voltage (Eo) and inverter output current (Io).

 Fig. 11: Grid voltage (50V/div), inverter output voltage (50V/div) and current (4A/div), 10ms/div.

 Fig. 12: Voltage ripples (200mV/div) and voltage of flying capacitor (20V/div), 5ms/div.

TABLE IV: Abbreviations

| DC   | Direct Current       |
|------|----------------------|
| MPPT | Maximum Power Point Tracking |
| NPC  | Neutral Point Clamped |
| CM   | Cascaded Multicell   |
| FCM  | Flying Capacitor Multicell |
| SM   | Stacked Multicell    |
| DFCM | Double Flying Capacitor Multicell |
| PV   | Photovoltaic         |
| THD  | Total Harmonic Distortion |
| MOSFET | MetalOxideSemiconductor Field-Effect Transistor |

IX. Conclusion

In the proposed inverter compared to the structure of DFCM, independent of the inverter cell number and the number of generated voltage levels, by replacing only two unidirectional switches with two bidirectional switches, network connectivity with high safety is provided. Also, this inverter with proposed control method has unique abilities such as capacitor voltage balancing in any desired value and obtaining maximum power from PV cells. Theoretically there is no limitation for the number of flying capacitors for balancing the voltage. The proposed control method tracks maximum power point of PV cells through assuring the equal magnitude for the input and output power. Through this unique controlling methodology, the MPPT is performed just by the inverter itself. Finally, the mathematical analysis and simulation results are used to verify the operation of proposed inverter and control method. The design, engineering and optimization procedure explained in this work provides further insight for designing multilevel inverters to be used in hybrid systems equipped with various energy storage devices (i.e. redox flow batteries and regenerative hydrogen fuel cell systems).
| n  | Number of cells |
| E  | Magnitude of DC voltage source |
| v_a | Grid voltage |
| i_r | Reference current |
| V_m | Grid maximum voltage |
| i_s | Grid current |
| ω | Angular frequency of grid voltage |
| R_s | Resistance of switches per current path loop |
| N_T (t) | Number of Transistor in current path at any time |
| N_D (t) | Number of Diode in current path at any time |
| r_C | Internal resistance of capacitor |
| f_g | Grid frequency |
| f_s | Switching frequency |

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