Modelling and Simulation of 16-bit Vedic Multiplication Using FPGA

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Abstract. As India is becoming digital India, so focusing towards digitization, there is requirement of updating the capacity of the processors becomes essential. Arithmetic is the basic component of any processors, multiplication is one of the principal procedure utilized in a number-crunching activities. To design the multiplication module require more hardware resources in contrast with addition & subtraction module. Therefore the present paper deals with study of multiplier to be operated using low power, less area & complexity and execution done with high speed in less time. Hence the implementation of the multiplier with above all requirements through Vedic Science. Vedic mathematics is primordial method of mathematics, which uses the exclusive techniques founded on sixteen sutras. The proposed paper focused on urdhva tiryakbhyam sutra, which is one of the method in Vedic mathematics dedicated for multiplication as it can be solved easily using vertical and crosswise manner. According, it diminishes the time, power, speed and in terms of area also. This paper discusses the 16-bit Vedic multiplication using verilog coding and simulation mode via software.

Keywords: Vedic multiplier, adder, urdhva tiryakbhyam, multiplication, delay, digital signal processing, conventional multiplier

1. INTRODUCTION

The process of multiplication is often being considered as one of the significant and fundamental process used in arithmetic operations. The multiplication process is mainly implemented in the Digital Signal Processing (DSP) as it takes most of the execution time, which makes a most promising need for developing a high speed multiplier. The multiplication time for any processor is determined by the instruction cycle required by a DSP chip [1]. For real time processors a higher throughput is required to get the desired performance characteristics of any system, which could be achieved by reducing the delay in time and the power consumed by the system. This proposed paper describes the multiplier techniques that are done using Vedic mathematics, which provides us with a very fast and also consumes less power [1]. The minimizations of the power consumption used by the digital systems could be optimized by manipulating all the levels of design. The modification of conventional multiplier so as to use as Vedic multiplier requires the circuit design, the technology through which the digital system are implemented, the basic building block for circuits implementation at the top
levels and the topologies implemented. The digital multipliers are used frequently as a component in digital system hence very fast, reliable and much efficient in any operations. Since there are various kinds of multiplier and particular architecture could be used according to the application. In most of the algorithms used in DSP the multiplier delay could be as much more critical and mainly tells us about the performance characteristics of the algorithm used. The conventional multiplication was generally implemented by the use of add and shift operations. In this way the proposed paper presents calculation to perform augmentation by offering points of interest and giving exchange off in setting of speed, region, unpredictability and force utilization. In this proposed paper the 16 bit Vedic multiplier architecture is showcased that is based upon the “Vertical and Crosswise” algorithm that is one of ancient Indian Vedic Mathematics. The main concept of this proposed paper is to minimize the propagation delay and power consumption.

2. VEDIC MULTIPLICATION

Vedic mathematics which is mainly used in reducing the typical and hard calculations as compare to normal conventional method used in mathematics [2]. This happens due to the fact that the Vedic formulas very much based on the natural principles and it is claimed that human minds easily grasp to Vedic mathematics. Vedic science is characterized as an approach of mathematics rules, it permits all the more quicker speed usage. It tends to be applied to separate fields of building innovation, for example, distributed computing, ascertaining and investigating, along these lines it turns into a proficient calculation.

3. URDHVA TIRYAKBHYAM SUTRA

In Vedic mathematics there are a total of sixteen sutras. The Vedic multiplier that has been proposed in this paper works on the principle of urdhva tiryakbhyam sutra. In ancient times, the main purpose of this sutra is specifically to perform the multiplication of two numbers in decimal form [2]. The decimal numbers uses the same manipulation technique that is used by the binary numbers so that the proposed algorithm remains unchanged and the desired system is compatible with other hardware systems. The normal multiplication formulae are applicable for all forms of multiplication techniques, but urdhva tiryakbhyam uses vertical and crosswise algorithm. Right now incomplete items that is created in ordinary multiplication is produced by simultaneous option of the transversely augmentations resultant and convey produced is then added to the following across increase resultant and the procedure proceeds. This calculation can be additionally reached out for n x n bit augmentations [3]. The Vedic multiplier doesn't rely upon clock frequencies as the halfway items and their summarized qualities are handled in equal structure. The advantages of this framework is that its structure is standard in nature and it very well may be laid in any of the chip by less human exertion and the fashioners can without much of a stretch identify and maintain a strategic distance from numerous gadget disappointments. In order to speed up the multiplier the number information and the yield width of the information transport could be additionally expanded. The fundamental purpose behind utilizing this sort of multiplier is that when the quantity of bits expands then the deferral of the doors and zone of the multiplier gets increment in an a lot lesser extent when contrasted with other typical multiplier.

4. ILLUSTRATION OF THREE DIGIT NUMBER MULTIPLICATION

By considering Urthava Tiryakbhyam sutra the decimal numbers which are shown in the Figure:1 i.e. 252 x 846 are multiplied. The multiplication starts by multiplying the extreme right digits on both rows then in next step the carry is added from the previous step. These outcomes in the generation of one of the bits as the outcome and carry. In the following stage this carry is included and subsequently this procedure is going on. On the off chance that there is more than one column in initial step, at that point all the outcomes are added to the past carry [3]. In the means that are followed, least significant bits (LSB) goes about accordingly bit and every single residual piece goes about as convey for the subsequent stage to follow. At first the pre carry is being taken to be zero.
5. MULTIPLIER ARCHITECTURES

Right now, the equipment structures of 2x2, 4x4, 8x8 and 16x16 Vedic multiplier modules are utilized which is clarified in the portrayals [4]. Here, Urdhva Tiryakbhyam sutra is being utilized to perform such the increase of two double numbers. Vedic multiplier is increasingly main stream in light of the fact that here fractional item age and expansion is done simultaneously. Thus it is very much taken by equal preparing framework. Therefore it is more suitable for binary multiplication. As a result there will be reducing in delay, which is primary goal of this proposed work.

6. 2X2 VEDIC MULTIPLICATION

The two bit vedic multiplier is built using two variable namely a’ and ‘b’ and the corresponding bit pattern as a[0:1] and b[0:1] which shows the two bits that are being used in the multiplication process [4].

By equations 1,2,3, the process of multiplication starts by multiplying the least significant bits (LSB) i.e. a0 and b0. The product of both the bits are taken vertically as s0 , then in the next step the MSB of the 1st input (a) i.e.; a1 is multiply crosswise with b0 and is given as the first input of the first half adder which is being used in the multiplier. The second input to the half adder comes from the product of b1 along with a0. The addition of the first half adder is taken down vertically as s1 and the carry is moved further to the second half adder used in the multiplier. The 2nd input becomes the produce of MSB of a and b i.e; a1 & b1. The sum of the second half adder is taken down vertically as s2 and carries as c0.

\[ s_0 = (a_0)\times(b_0) \]  
\[ (c_1)\times(s_1) = (a_1b_0)+(a_0b_1) \]  
\[ (c_2)\times(s_2) = (c_1)+(a_1b_1) \]  

![Fig. 2. 2-bit Vedic Multiplication Block](image)
Thus, for the implementation of the 2x2 vedic multiplier block as shown in figure requires four AND gates and two half adders[5]. This block diagram is a same as of the conventional multiplier and have much similar multiplication efficiency but provides a base for the implementation of the advanced command multipliers as 4x4, 8x8, 16x16 and so on.

7. 4X4 VEDIC MULTIPLICATION

The four bit vedic multiplier block diagram as shown in Figure:3 is built with the use of four 2x2 vedic multiplier blocks, a four bit adder and two six bit adders arranged in such a way so as to reduce the multiplication delay and increase its efficiency[5]. The inputs to the multiplier are the two 4-bit inputs namely ‘a’ as a0,a1,a2,a3 and ‘b’ as b0,b1,b2,b3. The inputs bits are further grouped in a group of two bits respectively. The input bits to the first 2x2 Vedic multiplier block are a1a0 and b1b0, similarly the inputs to second block are a3a2 and b1b0, the input bits to the third block are a1a0 and b3b2 the to the fourth block are a3a2 and b3b2. The output of the 2x2 Vedic multiplier blocks are provided to the adders i.e. 4 bit and 6 bit accordingly, which gives the final output of eight bits after addition.

Also the proposed architecture provides a way in order to reduce the total propagation delay taking place in the process of multiplication and also in turn provides better efficiency and paves a path for implementing the 8x8 and 16x16 Vedic multiplier architectures[6]. Fig: 3 show the diagram for the 4x4 Vedic multiplier.

8. 8X8 VEDIC MULTIPLICATION

The eight bit Vedic multiplication block diagram as shown in Fig 4 is built with the use of four 4x4 Vedic multiplier blocks which in turn uses 2x2 Vedic multipliers, one eight bit adder and two twelve bit adders arranged in such a way so as to reduce the multiplication delay and increase its efficiency. The inputs to the multiplier are the two 8-bit inputs namely ‘a’ as a0,a1,a2,a3,a4,a5,a6,a7 and ‘b’ as b0,b1,b2,b3,b4,b5,b6,b7. The inputs bits are further grouped in a group of two bits respectively [7]. The input bits to the first 4x4 Vedic multiplier block are a3a2a1a0 and b3b2b1b0, similarly the inputs to second block are a7a6a5a4 and b3a2a1a0, the input bits to the third block are a3a2a1a0 and b7b6b5b4 and to the fourth block are a7a6a5a4 and b7b6b5b4.

The output of the 4x4 Vedic multiplier blocks are provided to the adders i.e.; 8 bit and 12 bit accordingly, which gives the final output of eight bits after addition. Also the proposed architecture provides a way to reduce the total propagation delay taking place in the process of multiplication and also in turn provides better efficiency and paves a path for implementing the 16x16 Vedic multiplier architectures. Figure: 4 show the block diagram for the 8x8 Vedic multiplier.
9. 16 X 16 VEDIC MULTIPLICATIONS

The sixteen bit Vedic multiplier block diagram shown in fig 5 is built with the use of four 8x8 Vedic multiplier blocks which in turn uses 8x8, 4x4 and 2x2 Vedic multipliers, a sixteen bit adder and two twenty four bit adders arranged in such a way so as to reduce the multiplication delay and increase its efficiency [8]. The inputs to the multiplier are the two 16-bit inputs namely ‘a’ as a[15:0] and ‘b’ as b[15:0]. The inputs bits are further grouped in a group of two bits respectively. The input bits to the first 8x8 Vedic multiplier block are a[0:7] and b[0:7], similarly the inputs to second block are a[15:8] and b[7:0], the input bits to the third block are a[7:0] and b[15:8] and to the fourth block are a[15:8] and b[15:8].

The output of the 8x8 Vedic multiplier blocks are provided to the adders i.e. 16 bit and 24 bit accordingly, which gives the final output of eight bits after addition [9]. Also the proposed architecture provides a way in order to diminish the total circulation delay taking place in the process of multiplication and also in turn provides better efficiency and paves a path for implementing further high order Vedic multiplier architectures. Figure: 5 show the block diagram for 16x16 Vedic multiplier.

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**Fig 4. 8-Bit Vedic Multiplier Block**

**Fig 5. 16-Bit Vedic Multiplier Block**
10. RESULT

In this project the performance of Vedic multiplier architecture has been studied by means of XILINX simulation. The comparison is done with the results obtained from the previous work on low-cost block of multiplier implementations. The main requirement is to achieve the minimum cost, because of tool automation tends to minimize LUT count and increase the number of utilized slices. Hence, this results the area cost of an IP-block is the number of utilized slices.

The comparison of previous work with different techniques is as shown in Table 1 that target to a commonly used FPGA; the Vedic multiplier architecture is the smallest implementation that ever had been in the literature.

The area result of Vedic multiplier, it uses 804 slices, whereas our project costs 565 slices. The proposed architecture is also smaller than all other introduced low-cost multiplier.

The synthesis result of 16 x 16 bit Vedic multiplication is fastest than conventional multiplication, the proposed paper of sixteen bit Vedic multiplier of top view design as depicted in fig 6 and RTL view of proposed design as viewed in fig 7.

**TABLE 1. Comparison of 16 x 16 bit Vedic Multiplier (in ns)**

| Vedic Multiplier | Comparison |
|------------------|------------|
|                  | Device     | Conventional Multiplier | Vedic Multiplier |
| Path Delay       | Spartan 3  | 64.010ns                | 12.980ns         |

Device Utilization review:

Selected Device: XC3S100E
Device Family: Spartan3E
Number OF Slices LUT: 565
Number of Bonded IOB: 64 out of 210

**Fig 6.** Top view of sixteen-bit Vedic multiplier
The Design utilization summary for the sixteen bit Vedic multiplier is shown below table 2. It shows the number of transistors used in the designing of the multipliers which is shown in the LUT table. The number of slices used is displaced in the table which tells us about the spaces used by the multiplier and its efficiency.

**Table 2: Sixteen Bit Project Summary**

| Project File | Description | LUT |
|--------------|-------------|-----|
|               |             |     |
|               |             |     |
|               |             |     |
|               |             |     |
|               |             |     |
|               |             |     |
|               |             |     |
|               |             |     |

The Simulation for the sixteen bit Vedic multiplier is shown below fig 8 and the results are analyzed. Simulation is the imitation of the operation of a real-world process or system.

**Fig 7:** RTL View of Sixteen Bit Vedic Multiplier

**Fig 8:** Simulation result of 16 bit Vedic Multiplier.
11. CONCLUSIONS

It tends to be seen that the Vedic multiplier is amazingly honourable in all angles like working pace, engendering postponement, and intricacy. Multipliers are likewise valuable for DSP application like FFT, Convolution, sifting and so forth. It is seen that Vedic Mathematics gives a lot of effective calculations and equations for augmentation, which thusly speeds up the gadget. "URDHVA TRIYAKBHYAM" is general scientific formulae and similarly works the best and material in all the instances of increase.

This design is combination of different explored engineering accessible for increase and expansion, for example, Vedic multiplier, reconfigurable multiplier and compressor. Upon correlation with other existing multiplier it very well may be presumed that proposed multiplier is best in speed. For future work multiplier can be actualized and tried in ALU to build the exhibition of processors.

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