A New Test Device for Characterization of Mechanical Stress Caused by Packaging Processes

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Abstract. This paper reports on a new method for estimation and minimization of mechanical stress on MEMS sensor and actuator structures due to packaging processes based on flip chip technology. For studying mechanical stress a test chip with silicon membranes was fabricated. A network of piezo-resistive solid state resistors created by diffusion was used to measure the surface tension pattern between adjacent membranes. Finite element method simulation was used to calculate the stress profile and to determine the optimum positions for placing the resistive network.

Keywords: Thermo mechanical stress, Micro electromechanical systems (MEMS), Packaging.

1. Introduction
Microsystems technology spreads out rapidly over many other engineering fields, such as chemical and biological process engineering. This constantly draws a need for new, adapted packaging processes according to their application [1]. Otherwise, these customized solutions are generating enormous rising costs, which are defrayed only with difficulty. In order to fulfill the requirements on high quality and reliability negative effects caused by packaging should be analyzed and characterized early during the design phase. Currently, these are reduced afterwards by external circuiting and signal processing, but are not entirely compensated [2]. In this contribution a new method is presented for the estimation and minimization of mechanical stresses caused by packaging processes. Thermo mechanical loads often affect the operability of micro system components. We will concentrate on thermo mechanical aspects of packaging of MEMS starting from the investigations of mechanical deformation by packaging processes. Requirements on related material laws and material data for model based simulation are pointed out. Afterwards, the test chip (Figure 1) is introduced for predicting the influence of packaging processes on the accuracy of a micromechanical pressure sensor with the help of finite element analysis (FEA). With pressure sensors packaging of MEMS over a wide temperature range causes impairments on the long-term and drift behavior. Finally, a procedure for the test chip fabrication is proposed that focuses on the membrane with sensor elements in particular, as well as on related electrical structures.
2. Design and Fabrication

2.1. Theory
Micro electromechanical assemblies are exposed to temperature loads during their production and operation. These cause mechanical tension and dilatation (thermo mechanical stress) due to different thermal expansion coefficients of applied materials or inhomogeneous temperature distribution. Cyclic temperature changes lead to mechanical fatigue of the assembly and thus to their breakdown. The accurate evaluation of the thermo mechanical reliability of micro systems usually encounters considerable difficulties due to the complexity of technological and material related phenomena. They still increase with rising miniaturization that also stands in direct connection to the multiplicity of joint materials and locally strongly varying material properties. A mathematical for the computation of the load can be formulated as:

\[ \varepsilon_{th} = \int (\alpha_p(T) - \alpha_s(T)) dT \]  

Where \( \alpha_p \) represents the thermal expansion coefficient of the packaging materials and \( \alpha_s \) stands for the thermal expansion coefficient for the silicon substrate.

2.2. Simulation
For evaluating the reliability of packaging assemblies reliability tests based on statistic methods are very often used. Those methods are subject to the randomness of the test parameters. An essential utility for the development and optimization of packaging processes is simulation. With modeling of physical processes conclusions can be obtained, which would otherwise require time-consuming fabrication of test structures and their instrumentation. Finite element analysis is a numeric procedure

Figure 1. Silicon test chip structure

Figure 2. FEA model of test structure
for the approximate solution of partial differential equations within boundary conditions. The problem is being put into discrete form by dividing the general structure into plain subsections or elements. The used FEA model with structure related mesh is shown in Figure 2. Especially the complex geometry of packaging assemblies and diverse characteristics of applied materials lead to problems for defining the model. In many cases it is necessary to accompany theoretical investigations by experimental procedures. In order to examine thermo mechanical problems more efficiently, it is important to analyze the packaging assembly the same time, because of different thermal expansion coefficients. A selection of material parameter used in the simulation is presented in Table 1. Figure 3 and Figure 4 show the simulated results of the mechanical power distribution in a quarter models. It can be recognized that a use of different packaging materials leads to a change in the tension profile. There are different approaches for measuring the mechanical stress in silicon structures, e.g. Seebeck effect, Hall effect, photovoltaic effect etc. [3, 4]. A multiplicity of silicon sensors are based on the piezo-resistive effect. The piezo-resistive effect is based on the change of a resistance by applying a mechanical load.

| Material            | CTE (ppm/K) | Young’s Modulus (GPa) | Poisson’s Ratio |
|---------------------|-------------|-----------------------|-----------------|
| Silicon             | 2.59        | 160                   | 0.28            |
| Glass               | 3.27        | 62                    | 0.2             |
| Alumina             | 6.6         | 345                   | 0.23            |
| FR-4                | 16          | 18.2                  | 0.25            |
| Moulding Compound   | 15          | 14.2                  | 0.3             |
| Solder              | 28          | 32                    | 0.4             |

Figure 3. Simulated distribution of stress across the section of a quarter silicon MEMS structure (w=300 μm)

Figure 4. Simulated distribution of stress across the section of a quarter silicon MEMS structure (w=675 μm)
To this change of resistance contribute changes in geometrical form on one hand and on the other hand changes in the conduction mechanism. In order to record the mechanical stress arising in the silicon test chip diffused piezo-resistive semiconductor resistors are used. With the help of the finite elements method the optimal position for the placement of the resistive network was determined. The employment of the resistive network makes it possible to acquire the entire surface tension profile.

2.3. Fabrication
At the beginning when optimizing MEMS devices it is important to ask if permitted material characteristics have been exceeded. For this purpose multiple solutions exist. However, solely using simulation techniques cannot always help to discover the causation due to non-specific load rations and constraints. For studying mechanical stress originated by packaging processes a silicon test chip was produced. The core piece of the silicon test chip is a membrane array, which was fabricated with bulk micro machining. Using wet chemical, anisotropic etching of wells an appropriate membrane thickness has been developed time-controlled. In order to analyze different tension scenarios at the same time, different membrane thicknesses were produced. It has been a process technological challenge to manufacture the different membrane thicknesses in one process step. The detailed fabrication process of the membrane array is shown in Figure 5. Before starting the fabrication process, the 6 inch silicon wafer was cleaned in acetone, isopropanol and Carot’s acid (H₂O₂ : H₂SO₄) and kept on the hotplate at 150°C for 20 minutes. The first fabrication steps are (a) thermal wet and dry oxidation on both sides and (b) opening the front side for the p⁺-diffusion. Then follows (c) backside etching of silicon oxide to open the etching window for the silicon diagram. The under bump metallization thin films are (e) deposited on the front side by sputtering and are patterned by lift-off method to form the contact pads. The solder bump material was fabricated by (f) screen printing. The printing paste was a lead free powder (F620 Heraeus), with 95.5% of tin (Sn), 4% of silver (Ag) and 0.5% copper (Cu). The reflow process was done under inert athmosphere. Finally, (g) bulk silicon anisotropic wet etching with potassium hydroxide (KOH) was used to produce the thin membrane structure. It was necessary to understand the relationship between membrane thicknesses and etching window for the design of application. For controlling the diaphragm thickness not only the etching rate in a certain crystal orientation plays an important role, but also the knowledge of the anisotropy relationship.

For aqueous KOH solutions it was stated that silicon in <100> direction is up to 400-times faster attacked than in <111> direction [5]. In order to better understand the time-dependent etching process for silicon in KOH solution, physical approaches are used. With this approaches exclusively models for the simulation of the etched structures are concerned. The relationship between diaphragm thickness and the ratio of masked and unmasked area was quantitatively determined by combining the mathematical method and practical experiments [6, 7].

![Figure 5. Schematic diagram of the device fabrication process](image-url)
3. Experimental
For researching the influence of membrane stiffness and shape, a test bench of membranes was developed. Figure 6 a shows single membranes, membrane arrays and membranes with MESA structures. With the help of a white light Profilometer (Fries Research & Technology) the height profile as well as the roughness of individual elements was examined. On the surface of the test chip metal electrodes were applied (Figure 6 b, c). The sheet resistance was then measured using a high precision modular resistance meter that has been developed on the institute.

![Figure 6. (a) Membrane array, (b, c) Single piezo resistors](image)

The measurement technique is based on a two-term-calibration method (Figure 7 a). Two very temperature stable reference resistors (TCR < 0.2 ppm·K-1) have been chosen close to top and bottom of the expected measurement range [8]. With each measurement cycle these two references and up to six piezo resistors can be measured. When calibrating the measurement voltages nearly all temperature dependent effects from the electronics are compensated. Figure 7 b shows a noise test for a reference channel. It can be seen there is a maximum noise floor of about ±5 mΩ that was introduced from the electronics. All resistors are measured using the four-point probe method that compensates inlet and contact resistances. In particular the elimination of the contact resistances is important, since their value can also be dependent on mechanical stress.

4. Conclusion
In this contribution a new test chip was introduced for the estimation and minimization of the mechanical stress caused by packaging processes. Piezo-resistive semiconductor resistors have been used to acquire the surface tension profile. The results of the first measurements show a fundamental agreement with the results of the simulation. Thus it was possible to define design guidelines for the packaging process and to verify existing concepts. Linking FEA with the measurements of piezo-resistive resistors allowed both, validation of the used methods as well as of applied load rations and constraints. Further work concentrates on the examination of the developed design guidelines in connection to existing packaging processes.

![Figure 7. (a) Schematic diagram for the resistance measurement circuit; (b) measured noise on a reference resistor](image)
References

[1] A. D. Romig, Jr., P. V. Dressendorfer and D. W. Palmer. “High performance microsystem packaging: A perspective” Microelectronics and Reliability, Volume 37, Issues 10-11, October-November 1997, Pages 1771-1781.

[2] Lau, J.H. “Temperature and Stress Time History for Electrical Packaging”, Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on, Vol.19, Iss.1, Feb 1996, Pages 248-254.

[3] Smith, C.S. “Piezoresistance effect of germanium and silicon”, Phys. Rev., vol. 94, pp. 42-49, 1954.

[4] Kanda, Y. “Piezoresistance effect of silicon”, Sensors and Actuators A, vol. 28, pp. 83-91, 1991.

[5] Seidel, H. “Anisotropic Etching of Crystalline Silicon in Alkaline Solutions”, J. Electrochem. Soc., vol. 137, pp. 3626-3632, 1990.

[6] Chung, Chen-Kuei “Modelling and fabrication of step height control of a multilevel Si (100) structure in KOH solution”, J. Micromech. Microeng, vol. 14, pp. 341-346, 2003.

[7] Kim, Eun Sok, Muller, Richard S., “Front-to-Backside Alignment Using Resist-Patterned Etch Control and One Etching Step”, J. of Microelectromechanical Systems, vol. 1, NO. 2, pp. 95-99, 1992

[8] T. Braun, K.- F. Becker, M. Koch, V. Bader, R. Aschenbrenner, H. Reichl, “High-temperature reliability of Flip Chip assemblies”, J. Microelectronics Reliability, vol.46, pp.144-154, 2006