Effect of CoSi$_2$ Formation Process on CMOS Transistor Electrical Properties for Sub-100-nm Memory Applications

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Effect of various processing conditions on abnormal CoSi$_2$ formation, such as the well-known Co spike and crystal agglomeration. We used Co metal sputtering and subsequent thermal treatment such as rapid thermal processing (RTP). The effect of the ion implantation conditions and Co deposition method were studied. To evaluate the electrical failure of transistors, we checked the chip level leakage current ($I_{CQ}$) and the unit level leakage current ($I_{JC}$) in the test pattern, simultaneously. As the dopant species and concentration were believed to affect the electrical properties of every single transistor, chip level leakage current and unit level leakage current deteriorate or improve simultaneously. When we used a Ti/TiN capping layer and high-temperature physical vapor deposition, abnormal growth was suppressed and the interface became smooth. The chip level leakage current in both cases showed significant improvement; however, the unit level leakage current showed a negligible change in contrast to the chip level one. We concluded that, despite no change in unit level leakage current, the overall level of chip level leakage current improved because of the significantly decreased number of defective sites such as Co spike.

Experimental

We prepared wafers with sub-50-nm technology node structure using a full CMOS process. The short process flow with respect to the cobalt silicide formation is illustrated in Fig. 1. After conventional CMOS transistor formation, source–drain (SD) RTP followed. An interlayer dielectric was deposited, and a metal contact (M0) was formed to connect the SD region with the metal signal line (M0). To reduce the metal contact resistance, we applied extra ion implantation, real sub-100-nm dynamic random-access memory (DRAM) devices. Various electrical failures related to abnormal CoSi$_2$ formation were observed, and their mechanism is proposed. The proposed mechanism was also employed to clarify the relationship between various process conditions and the electrical properties of our DRAM chip.

Figure 1. Overall Process Flow of cobalt silicide formation.
which was followed by post-RTP. After the contact bottom surface was cleaned by a wet chemical such as a sulfuric peroxide mixture (SPM), we deposited Co metal by a physical vapor deposition (PVD) sputter process, where the processing temperature was kept below 100 °C. To form cobalt silicide, RTP was performed using two consecutive processes (first step: 400–500 °C, second step: >700 °C). After RTP, residual Co metal was removed using SC-1 (a NH4OH:H2O2 mixture). Finally, CoSi2 formation was completed, and metal plugging of the M0C was performed. A subsequent conventional DRAM process (such as cell capacitor formation) was performed; thus, an additional post-thermal budget was introduced.

We varied the process conditions related to extra ion implantation and Co metal deposition to obtain ideal cobalt silicide formation.

We investigated the structural properties of the formed CoSi2 metal contact as follows: The cross-sectional view of the metal contact was observed by transmission electron microscopy (TEM). In particular, the zero axis contrast imaging method was employed to visualize the formed CoSi2 phases more clearly. To confirm the composition of the CoSi2, we used electron energy-loss spectroscopy (EELS) (Fig. 2). The Si peak in a single crystal (i.e., a Si wafer) was found to be located at ~17 eV. In the EELS spectra from the sample, we observed a shift in the Si peak position. From the peak shift, we identified the exact crystalline phases of the metal silicide contact area, which will be described in the next section.

To check the electrical properties of the DRAM chip, we estimated the drain leakage current of the chips using two methods (Fig. 3). First, as shown in Fig. 3a, we measured the total current through a metal pad connected to the substrate P-type metal–oxide–semiconductor (PMOS) bulk, gate electrode, and SD junction in the chip standby state. This represents the combined junction leakage current of millions of PMOS transistors in the wordline driver circuit region, which we refer to as $I_{pp}$. Second, in Fig. 3b, the unit junction leakage current (JLC) of an individual PMOS transistor in the test pattern was measured at a gate-bulk voltage $V_{gb}$ of 0 and a drain-bulk voltage $V_{db}$ set to a certain value. We use the terms "$I_{pp}$" and "JLC" to refer to representative parameters for the device electrical performance.

Results and Discussion

Abnormal CoSi2 growth and electrical failure.—Fig. 4 shows typical images of abnormal CoSi2 growth. We can see that some
CoSi₂ grains accumulate locally and form a large agglomeration. It is well-known that with increasing surface energy between two different material phases, crystals of the same phase tend to agglomerate to reduce the total thermodynamic energy of the system. On the basis of this mechanism, we can assume that the interface energy between CoSi₂ and the substrate bulk Si is very high. This means that the surface of the bottom contact area is very unstable before Co deposition. Fig. 4 also shows that some CoSi₂ phases penetrate along a specific direction, which is called a Co spike. This phenomenon suggests that recrystallization with a preferred crystal orientation might occur or that the formed metal silicide penetrates the bulk Si through existing crystal defects.

The EELS spectrum of a Co spike is shown in Fig. 5 for Si atoms in different phases. As we have seen above, the peak located at ~17 eV can be assigned to silicon atoms in bulk Si. On the other hand, there is another peak shifted to a higher value than that of bulk Si. To confirm the specific crystal phase, we identified the peaks in EELS spectra of CoSi and CoSi₂ on an un-patterned wafer (not shown). We found that the Si peaks of CoSi₂ and CoSi are shifted upward by about 3 and about 5 eV, respectively. Hence, we can conclude that the dominant crystalline phase in the Co spike is unquestionably CoSi₂.

Cobalt silicide has two crystalline phases, cobalt mono-silicide (CoSi) and cobalt di-silicide (CoSi₂). When Co and Si react with each other at low temperature, CoSi, which is thermodynamically stable under this condition, is formed preferentially. After the CoSi is subjected to post-thermal treatment, it enters the CoSi₂ phase, which is stable at higher temperatures.

Considering our process flow, CoSi₂ is formed directly through RTP at a relatively high temperature (above 500°C), at which CoSi₂ is the thermodynamically stable crystalline phase. Because the same CoSi₂ phase was maintained at the Co silicide defect, we can conclude that these types of defects should be generated without any phase transformation.

We measured the Iₚp values of all the chips on a wafer having many agglomeration defects. We selected one of the chips with a relatively high Iₚp value and observed its photo-emission. We detected bright spots in the sub-wordline PMOS region; we then measured the I-V characteristics of each transistor and compared the curves in the normal PMOS (dark) and failed PMOS (bright) regions. These comparisons are shown in Fig. 6.

In Fig. 6, with decreasing absolute value of V₉ₕ, the gate bias is lowered, and the transistor shifts into off-state and gate-induced drain leakage (GIDL) condition. At a sufficiently low bias condition in V₉ₕ, a significant degradation in the drain off-state leakage current (on the
order of about $10^2$) is observed for the failed PMOS transistor compared to the normal one. In summary, the increase in $I_{pp}$ is accompanied by junction failure of each PMOS transistor in the sub-wordline area.

The mechanisms of the junction failure are shown in Fig. 7. Type (A) is direct SD-to-bulk tunneling after CoSi$_2$ diffusion into bulk Si. When a Co spike extends beyond the SD junction, the SD and the bulk can be connected to each other. This facilitates free charge carrier flow between the SD and bulk.

Type (B) is trap creation led by the CoSi$_2$ spike and subsequent trap-assisted-tunneling (TAT). Type (B) is different from type (A) in that Co spike is so short in length not enough to extend to SD junction. Hence, this type of Co spike does not cause direct junction leakage. On the other hand, after a Co spike is generated in the bulk Si, the bulk Si experiences a highly compressive stress condition. This would produce many crystal defects that act as bulk traps by the TAT effect.

Type (C) is electric field enhancement due to the small separation between the CoSi$_2$ and the gate. As a Co spike approaches the gate electrode, the electric field between the Co silicide and the gate becomes strong. Then, the increased electric field enhances the GIDL current.

Comparing three types of junction failure, type (C) is thought to be minor, because the increase in $V_{gb}$ (to positive in PMOS) does not cause a significant increase in leakage current. Thus, type (A) and (B) act as dominant mechanism for junction failure. Further, type (A) will be effective to enhance the junction leakage with increased length of Co spike.

As Ti is a very active metal species, it can easily form TiSi$_x$ compounds with Si atoms and TiO$_x$ with ambient air. Unlike the Ti atoms in the compound TiN, single Ti atoms can move freely into bulk Si. Consequently, Ti might play an important role in the Co–Si reaction. Ti is known as an effective inhibitor of CoSi$_2$ radical formation.\textsuperscript{15,16} The Co/Ti stack produced a thinner CoSi$_2$ formation in the film compared to that in the Co/TiN stack film. In fact, with increasing Ti thickness, a thinner CoSi$_2$ layer was observed. Although there are many possible explanations for this phenomenon, the following two arguments are likely to describe the role of Ti atoms in the Co–Si reaction.

First, free Ti atoms can move swiftly through the formed CoSi$_2$ layers and tend to be segregated along the CoSi$_2$ grain boundaries as other researcher such as Tung et al. already reported.\textsuperscript{15} The Ti atoms trapped at grain boundaries hinder motion of the Co atoms toward the Co–Si interface to react with each other. Further, they also block any further movement of CoSi$_2$ grain boundaries that would allow grain growth. Regarding agglomeration, the easy movement of CoSi$_2$ grain boundaries is detrimental to abnormal growth, and we need to...
control their motion effectively. This hindering effect mitigates CoSi₂ agglomeration well.

Second, a CoTi₅ intermediate layer is thought to be generated near the CoSi₂ layer. When Co and Ti are deposited alternately, they can react to form a CoTi₅ phase before the Co–Si reaction. This CoTi₅ phase is believed to be rather unstable because many experiments have failed to detect it explicitly. Nevertheless, if any type of Co–Ti linkage does exist instead of Co–Si, the CoTi₅ layer could retard dramatic CoSi₂ formation by limiting the supply of Co atoms that participate in the Co–Si reaction to form CoSi₂.¹⁶

In conclusion, we need to introduce a Ti cap on the Co metal to produce a smooth interface, which is favorable for obtaining good contact resistance and less junction failure. As excessive Ti decreases the final CoSi₂ thickness by suppressing the Co–Si reaction, the thickness of the Ti capping layer should be optimized to obtain excellent CoSi₂ formation.

Next, the effect of ion implantation on CoSi₂ formation was observed. Before additional SD implantation to lower the contact resistance and less junction failure. As excessive Ti decreases the final CoSi₂ thickness by suppressing the Co–Si reaction, the thickness of the Ti capping layer should be optimized to obtain excellent CoSi₂ formation.

The sample with room temperature Ge implantation has dislocation (dark area) under bottom metal contact. In contrast to this, although the sample with cold Ge implantation has no dislocations, the morphology and amount of abnormal crystal growth are unaffected by the implant condition. As it is generally accepted that crystal defects could enhance material diffusion, this result is rather hard to understand well. However, considering that the sample with cold implantation has the same level of Co agglomeration, the mechanism that governs Co agglomeration is not diffusion via lattice imperfections such as dislocations. On the other hand, morphological evolution in the polycrystalline phase, such as grain boundary movement, is the main driver for Co agglomeration, as described above, when Ti/TiN capping is used.

We also investigated how Co agglomeration was affected by the use of carbon ion implantation to inhibit SD dopant diffusion. The implanted carbon tends to react with the existing SD dopant and form a linkage with it. This linkage effectively hinders the diffusion of the SD dopant and implanted carbon, and the abrupt dopant profile at the SD junction can be maintained. Another study reported that carbon implanted above a certain level (>10¹⁵ cm⁻³) became segregated at the grain boundaries of CoSi₂ and improved the thermal stability of CoSi₂ by suppressing grain boundary movement.¹⁷ In our experiment, however, Co agglomeration was not significantly reduced. This is not clearly understood; however, the low level of carbon dopant (~10¹³) might not inhibit grain boundary movement but rather suppresses dopant diffusion. The electrical properties of the sample with suppressed diffusion of the SD dopant will be shown below in detail.

In this study, Co metal was deposited by PVD, i.e., metal sputtering. Unlike chemical vapor deposition, a standard PVD process is conducted in a cold chamber (<200°C, i.e., cold PVD). We used a higher-temperature PVD process (hot PVD) instead of cold PVD. Fig. 10 shows that the resulting CoSi₂ formation beneath the metal plug is smoother and more uniform than that obtained in cold PVD.

This phenomenon is thought to happen via the following reaction steps. First, the wafer is heated to high temperature, and the Si surface become susceptible to further reaction with Co. Next, the Co target is
sputtered onto the wafer, and Co–Si clustering occurs more easily than in cold PVD. This type of clustering cannot be identified as normal cobalt silicide (CoSi or CoSi2) using X-ray diffraction. However, in Fig. 11, TEM observation clearly shows that a mixed layer exists, indicating that some level of Co–Si clustering occurs. Finally, after RTP, the Co–Si clusters transform completely into the CoSi2 phase.

We also performed Co sputtering under various bias conditions, but the bias had a negligible effect on CoSi2 formation. From this observation, we can conclude that in-situ thermal treatment above a certain level is more effective than other methods for enhancing stable CoSi2 formation.

Electrical failure characteristics: processing parameter dependence.—Here, we investigate the effect of Co agglomeration on the electrical properties of the DRAM chip. Fig. 12 shows the $I_{pp}$ values of DRAM chips with a Ti or TiN layer capping the Co metal. In the case of Ti capping, $I_{pp}$ exhibits stable behavior below 0.5 [A/U], whereas for the TiN cap, $I_{pp}$ reaches 3–4 [A/U], accompanied by overall degradation.

Fig. 13 shows the JLC characteristics of the test pattern for different capping materials. In contrast to the results in Fig. 12, the JLC levels do not differ greatly between the Ti and TiN capping cases, indicating that the behavior related to $I_{pp}$ is quite different from that affecting the JLC of the test pattern. Considering the structural differences such as Co agglomeration associated with the different capping materials, Co agglomeration has a huge effect on $I_{pp}$ but a negligible effect on the JLC in the test pattern. What causes this discrepancy?

As we noted briefly in the Experimental section, $I_{pp}$ is the summation of the leakage current caused by all the PMOS transistors in a chip. A DRAM chip consists of an array of millions of PMOS transistors; hence, it is possible that there are a few abnormal PMOS transistors with exceptionally high junction leakage. We return to Fig. 6, which shows the $I$–$V$ characteristics of a failed PMOS transistor detected using its photoemission. This figure shows that there was a difference on the order of $10^3$ in the magnitude of the leakage current. Thus, even if only a few of the PMOS transistors show such abnormal behavior, they could affect $I_{pp}$ to some degree.

On the other hand, because there are only dozens of test patterns on a wafer and the JLC is measured for these patterns, abnormal transistors can seldom be counted in the measurement of the test pattern. This means that transistor failure occurs very seldom, and the JLC failed to show the anticipated effect of Co agglomeration depending on the capping material. In conclusion, we cannot detect the very rare failure in the JLC measurement of the test pattern; the only way to find this failure is to implement an electrical measurement method that collects data from all the PMOS transistors on a chip.

We investigated the $I$–$V$ characteristics of several fail points showing anomalous leakage current and analyzed the structural properties at those points by TEM observation. We found that transistors with no exception contains a Co spike and has a leakage current 103 times higher than that of normal ones containing Co agglomeration observed throughout the chip. This observation proves that Co agglomeration, which is the typical form of abnormal CoSi2 growth, is not the main cause of the abnormally high leakage current, and that Co spikes are...
mainly responsible for the phenomenon. In other words, Co agglomeration, which can be observed easily on the sample, does not directly cause the abnormal behavior in the JLC of the test pattern and the increased $I_{pp}$. Therefore, it can be postulated that only a small fraction of PMOS transistors having Co agglomeration produce a Co spike, which leads to the increase of $10^3$ times in the leakage current followed by an apparent increase in $I_{pp}$, which degrade the operation of real DRAM chips.

Fig. 14 shows the values of $I_{pp}$ with and without carbon ion implantation. The sample with implanted carbon has a slightly higher $I_{pp}$ than that without carbon implantation. As we already found that the morphology does not change greatly with carbon implantation, it can be assumed that the dramatic increase in $I_{pp}$ under carbon doping indicates a different electrical mechanism from that in the case of Ti capping. The JLC characteristics in the test pattern with carbon implantation are shown in Fig. 15. In contrast to the case of Ti capping, the JLC characteristics exhibited the same behavior as the $I_{pp}$ characteristics. Taking all these observations into account, it is reasonable to postulate as follows: Carbon implanted into the sample inhibits SD dopant out-diffusion by combining with the SD dopant, as we noted above. In PMOS transistors, boron is the SD-type dopant and is well confined to the original SD region by blocking of boron diffusion by boron–carbon linkages. Consequently, the highly doped SD junction causes an increase in the electric field in the region, followed by an enhanced GIDL current. This event is not as rare as Co spikes but is rather common in all of the transistors on the chip and increases the JLC in the test pattern. In addition, all of the transistors having a higher leakage current contribute directly to $I_{pp}$, which is thus increased simultaneously. Comparing the changes in $I_{pp}$ and the JLC, we find that both of them increase in magnitude by a factor of about 10. Therefore, it can be concluded that the increase in $I_{pp}$ is not induced by abnormal CoSi$_2$ growth (in particular, Co spikes), as we found for the case of the capping material. Although abnormal CoSi$_2$ growth does occur at the same level, the increase in the leakage current of the unit PMOS transistor causes the overall increase in $I_{pp}$.

Fig. 16 shows the effect of the deposition temperature on $I_{pp}$. When high-temperature PVD was used, a dramatic decrease in $I_{pp}$ appeared. The effect of the deposition temperature on the JLC in the test pattern is shown in Fig. 17.

From the arguments regarding the capping material and carbon implantation, we found that $I_{pp}$ and the JLC of the test pattern are closely related regardless of whether abnormal CoSi$_2$ growth such as Co spikes occurs. The JLC of the sample deposited by hot PVD is similar to that of the sample deposited by cold PVD. This result resembles the effect of different capping materials more than the effect of carbon implantation. This implies that abnormal CoSi$_2$ growth is responsible for this behavior. We found that a smoother interface between the CoSi$_2$ and the bulk Si can be obtained by using hot PVD. That is, the sample deposited by hot PVD shows no Co agglomeration or Co spikes, which can explain the fact that there is an apparent decrease in the $I_{pp}$ value of DRAM chips fabricated using this sample. In conclusion, both Ti capping and hot PVD are very useful for effectively hindering the formation of Co spikes, which are responsible for the abnormal increase in $I_{pp}$ but do not affect the JLC in the test pattern.

In summary, we attempted to correlate the $I_{pp}$ value at the chip level and the JLC at the test pattern level with various process conditions. $I_{pp}$ is the summation of the leakage current of all the PMOS transistors and is related to the current characteristics of standard transistors and the electrical properties of a few abnormal transistors. On the other hand, the JLC in the test pattern seems to behave quite differently from $I_{pp}$ because the JLC represents only the standard transistor characteristics. Therefore, if CoSi$_2$ formation produces irregularities such
as Co spikes, they affect only the characteristics of $I_{pp}$, not those of the JLC in the test pattern. In contrast, carbon implantation is believed to affect the standard transistor characteristics and changes $I_{pp}$ and the JLC simultaneously. Carbon implantation does not affect abnormal CoSi$_2$ growth such as Co spikes but only degrades the $I_{pp}$ characteristics via overall degradation of the transistors, assuming the same number of Co spikes.

Conclusions

We investigated cobalt silicide formation and its effect on the electrical properties at the full chip level for various process conditions such as the dopant species, concentration, and Co deposition method. The SD junction profile was found to change with the dopant species and content, which affected the junction leakage. Because it changes the electrical properties of normal transistors, $I_{pp}$ and the unit JLC exhibit similar behavior.

The CoSi$_2$ formation behavior varies with the method of Co material deposition. When we used a Ti/TiN capping layer and high-temperature PVD, abnormal growth was suppressed and the interface was smooth, which can prevent agglomeration and Co spikes. The $I_{pp}$ values showed significant improvement under both conditions (hot PVD and a Ti/TiN capping layer). In contrast, the JLC in the test pattern showed no obvious change. This observation indicates that the GIDL current of normal transistors is degraded; however, it can be concluded that the larger effect of a decrease in the number of defective sites improves the overall $I_{pp}$ characteristics.

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