A multi-path switched-capacitor-inductor hybrid DC-DC converter with reduced inductor loss and extended voltage conversion range

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Abstract This work proposes a hybrid DC-DC converter using a multi-path switched-capacitor-inductor (MPSCI) topology. Assisted by switched-capacitor branches, it features voltage-conversion range extension and inductor power loss reduction, and hence improving the conversion efficiency. Implemented in a 180-nm CMOS process, the proposed converter can regulate an output voltage of 1.8–3.3 V from a 5-V input bus voltage using a 4.7 µH inductor (DCR = 240 mΩ) at a switching frequency of 800 kHz. It achieves a peak conversion efficiency of 93.7% when delivering an output current of 1 A. Under a maximum loading of 3 A, this design still attains an efficiency of up to 85.8%. Furthermore, in contrast to the existing dual-path and conventional buck topologies, the proposed converter realizes an inductor loss reduction up to 3.3 and 5.4 times, respectively, at the maximum loading conditions.

key words: DC-DC converter, DCR loss, hybrid topology, multi-path, switched-capacitor, voltage conversion range

Classification: Integrated circuits (analog)

1. Introduction

In recent years, the fast-growing demand for portable intelligent devices powered by low-voltage buses or batteries requires high-efficiency power converters with a small form factor [1 2 3 4 5 6 7 8]. The improvement of the functionality and performance of the loading systems brings more challenges to the DC-DC converter design to suffice the rising loading current requirements. Existing inductor-at-output topologies, such as buck or 3-level topologies [1 2 8 9 10 11 12 13 14 15 16 17 18], suffer from significantly climbed-up conduction loss on the power inductor when delivering a high loading current with a compact system volume. It is mainly due to the loss of inductor parasitic DC resistance (DCR) and can be critical for achieving high power conversion efficiency (PCE). As the tradeoff, a bulky inductor with a smaller DCR can contribute to the efficiency improvement by, however, sacrificing the system compactness [2 3 4 13 16 19]. Within a specific volume, the DCR increases with the inductance and can be as high as hundreds of milliohms, which is dramatically higher than the switch conducting resistance (RDS) and hence introduces considerable influence to the overall PCE. A common issue with the inductor-at-output converters is that the total output current (IOUT) flows through the inductor, leading to a high I²R loss (thermal dissipation) when delivering a large IOUT.

To limit the converter size and simultaneously reduce the power dissipation on the inductor, a practical solution is to reduce the inductor current by adding more current-conducting paths to the output, as demonstrated in [1 20 21 22 23 24 25]. For example, Fig. 1 shows two existing dual-path (DP) switched-capacitor-inductor hybrid topologies proposed in [1 20]. These topologies reduce the inductor current by delivering a part of IOUT through the switched-capacitor (SC) branches. However, these DP topologies suffer from a restricted voltage conversion ratio (VCR) of 1/2 to 1 due to the constraints on inductor charging and discharging voltages, limiting their application of converting a 5-V bus voltage to a 1.8-V load supply. Although this issue can be resolved by adding an extra power switch and one more switching phase, as discussed in [20], the effectiveness of the inductor current reduction degrades with enlarging the step-down VCR, resulting in a

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noticeable PCE drop.

This work proposes a multi-path switched-capacitor-inductor (MPSCI) converter topology, addressing the inductor DCR loss and VCR range limitation in high loading current conversions. It consists of a single inductor and dual flying capacitors to realize a extended step-down ratio of 1/3 to 1, featuring enhanced inductor current reduction in a higher-step-down (closer to 1/3) VCR condition.

2. The proposed MPSCI converter topology

2.1 Steady-State Operations

Regarding the inductor-voltage analysis for the existing DP topologies depicted in Fig. 1, the VCR limitation is determined by the voltage across the inductor in both charging and discharging phases. Based on the inductor current balance in steady state, applying \( V_{IN} - 2V_{OUT} < 0 \) in \( \Phi_2 \) for the inductor discharging indicates that \( V_{OUT} / V_{IN} > 1/2 \) for both topologies shown in Fig. 1. Accordingly, a higher voltage difference across the inductor during its current decaying phase can give a lower VCR boundary and, hence, realize a wider conversion range. An effective way to extend the step-down conversion range is to increase the voltage difference across the inductor from \( (V_{IN} - 2V_{OUT}) \) to \( (V_{IN} - 3V_{OUT}) \) during \( \Phi_2 \) by using two SC cells, coming up with the proposed MPSCI topology as illustrated in Fig. 2. According to the operating states shown in Fig. 2(b), the steady-state capacitor voltages on \( C_1 \) and \( C_2 \) are \( V_{IN} - V_{OUT} \) and \( V_{OUT} \), respectively. Based on the steady-state volt-second-balance relation of the inductor, the corresponding VCR expression is:

\[
M = \frac{V_{OUT}}{V_{IN}} = \frac{1}{3-2D} \quad 0 < D < 1. \quad (1a)
\]

\[
D = \frac{3M-1}{2M} \quad (1b)
\]

As observed, the duty ratio \( D \) varying between 0 and 1 results in a VCR from 1/3 to 1.

During \( \Phi_1 \), the current \( i_L \) ramps up as the inductor voltage \( V_{L,\Phi_1} = V_{IN} - V_{OUT} \). Paralleled with the inductor, \( C_1 \) is charged up to the same voltage as the \( V_{L,\Phi_1} \). At the same time, capacitor \( C_2 \) is discharged by the converter output and, hence, \( V_{C2} = V_{OUT} \) in steady-state. During \( \Phi_2 \), \( L \), \( C_1 \), and \( C_2 \) are connected in series. Thus, by applying a small ripple approximation to the inductor, the total charges flowing to \( C_1 \) and \( C_2 \) are

\[
Q_{C1} = Q_{C2} = (1 - D)I_{L,DC} \quad (2)
\]

where \( I_{L,DC} \) is the DC average of the \( i_L \) and \( T \) is the switching period. \( i_L \) decays as \( V_{L,\Phi_2} = V_{IN} - 3V_{OUT} \) during \( \Phi_2 \), while the charging/discharging states for \( C_1 \) and \( C_2 \) are opposite to \( \Phi_1 \). According to the above operations, three current-conducting branches (through \( L \), \( C_1 \), and \( C_2 \)) are connected to the output during \( \Phi_1 \), realizing a multi-path output-charge delivery. In contrast to single-path structures, the proposed scheme effectively reduces the \( I_{L,DC} \). Based on charge conservation and the expression in (2), the \( I_{L,DC} \) is derived as below:

\[
TI_{L,DC} + Q_{C1} + Q_{C2} = Q_{OUT}
\]

\[

I_{L,DC} = \frac{I_{LOAD}}{3 - 2D} = M I_{LOAD}. \quad (3)
\]

From above, the inductor current can be reduced by a factor of \( M \) when compared with the existing inductor-at-output topologies.

Fig. 3 exhibits the conceptual waveforms for the steady-
state operations of the proposed topology. According to the information of \( V_{T1} - V_{T2} \) in either \( \Phi_1 \) or \( \Phi_2 \), the inductor current ripple \( \Delta I_L \) has the following form:

\[
\Delta I_L = \frac{(V_{IN} - V_{OUT})DT}{L} = TV_{OUT} \frac{3(M-1)(1-M)}{2M^2}.
\]

(4)

From (4), the peak value of the \( \Delta I_L \) occurs at \( M = 0.5 \), and the corresponding maximum inductor current ripple amplitude equals \( 0.5TV_{OUT}/L \). Thus, in the conversion range from 1/3 to 1/2, the proposed topology achieves a lower inductor current for DC and AC components than a buck.

### 2.2 Conduction Loss Analysis

Under heavy load conditions, the conduction losses from inductor DCR and switches \( R_{ON} \) dominate the converter efficiency [26][27]. The corresponding theoretical loss analysis is as below

\[
I_{L,rms} = \frac{1}{\sqrt{2}} \int_0^T I_L^2(t) \, dt = \sqrt{I_{L,DC}^2 + \frac{\Delta I_L^2}{12}}.
\]

(5)

By substituting (3) into (5), we can derive the loss power expression accordingly, i.e.,

\[
P_{loss,L} = I_{L,rms}^2 R_{L,DC}
\]

\[
= R_{L,DC} \left\{ M^2 I_{OUT}^2 + \frac{1}{12} \left[ \frac{V_{OUT}^2 (3M-1)(1-M)^2}{2M^2} \right] \right\}.
\]

(6)

From (6), the DC part of the conduction loss with the MPSCI is \( M^2 \) times smaller than that of the inductor-at-output converters. Besides, the AC part of the conduction loss due to the inductor current ripple decreases with \( M \). From Fig. 3, the charge amount \( Q_{C1,2} \) flowing through the capacitors \( C_{1,2} \) equals to the \( Q_L \) during \( \Phi_2 \), estimated as

\[
Q_{C1,2} = (1 - D)TI_{L,DC}
\]

(7)

According to the steady-state charge conservation with the capacitor, the average current through the \( C_{1,2} \) during \( \Phi_1 \) is

\[
I_{C1,2,\Phi_1} = \frac{Q_{C1,2}}{DT} = \frac{(1-D)}{D} I_{L,DC}
\]

(8)

Based on (8) and the operating states shown in Fig. 2(b), we can estimate the passing current through different switches in each phase, as:

\[
\Phi_1: \begin{cases}
I_{RS1} = \frac{1}{D} I_{L,DC} \\
I_{RS3} = \frac{(1-D)}{D} I_{L,DC} \\
I_{RS4} = \frac{1}{D} I_{L,DC} \\
I_{RS5} = \frac{(1-D)}{D} I_{L,DC}
\end{cases}
\]

\[
\Phi_2: \begin{cases}
I_{RS2} = I_{L,DC} \\
I_{RS6} = I_{L,DC}
\end{cases}
\]

(9)

(10)

where \( I_{RSi} \) represents the passing current through the switch \( S_i \). The overall switch conduction loss expression is:

Table I Topology modeling parameters

| V_
| f_
| L | C_
| C_
| R_
| DCR |
|---|---|---|---|---|---|
| 5V | 500kHz | 2A | 4.7μH | 10μF | 10μF | 10mΩ | 250mΩ |

---

\[ P_{loss,SW} = D \left( I_{RS1}^2 I_{S1} + I_{RS3}^2 I_{S3} + I_{RS4}^2 I_{S4} + I_{RS5}^2 I_{S5} \right) + (1 - D) \left( I_{RS2}^2 I_{S2} + I_{RS6}^2 I_{S6} \right) \]

\[ = I_{L,DC}^2 \left\{ \frac{1}{D} \left( R_{S1} + R_{S4} \right) + \frac{(1-D)^2}{D} \left( R_{S3} + R_{S5} \right) + (1 - D) \left( R_{S2} + R_{S6} \right) \right\} \]

(11)

where \( R_{Si} \) denotes the switch-on resistance of the switch \( S_i \), as shown in Fig. 2. Based on the above theory, we can establish an analytical model of the conduction loss power to evaluate and compare the performance of different topologies. Using the corresponding parameters given in Table I, we can obtain the modeling results, as displayed in Fig. 4, for the proposed MPSCI, existing DP, and the conventional buck topologies. From the highlighted region in the figures, the efficiency and power loss difference between the proposed and the existing topologies become more noticeable as the VCR enlarging.

### 3. Converter design and implementation

The overview implementation of the proposed MPSCI converter system composes of the power stage, gate drivers, and the feedback control loop, as shown in Fig. 5. All the power switches are based on 5-V transistors in a 180-nm CMOS process to ensure operating reliability. Regarding the power passive selection, the capacitance of \( C_1 \) and \( C_2 \) is 10μF, and \( C_{OUT} \) is 20μF with an equivalent series resistance (ESR) of 10mΩ for each. The converter adopts an inductor of 4.7μH with DCR=240mΩ and a dimension of 2.5mm × 2mm × 1mm. It features regulating a \( V_{OUT} \) of 1.8–3.3V from an input of 5V based on voltage-mode PWM control. A typical type-III compensated error amplifier (EA) is adequate for stabilizing the load regulation control loop. For proper switch on/off operations, the gate driving voltage for all the switches is 5V. Except for the input switch \( S_i \), which is implemented by a PMOS transistor to ease the driving...
requirement, all the other switches are implemented by NMOS for better conductance and lower silicon area.

We designed the gate driver circuits in three categories for different power switches according to the individual operating voltage conditions. Specifically, $S_2$ and $S_5$ are GND-connected switches, an inverter-based buffer chain with a stage size increase by a factor of 10 that ensures an effective fan-out is applicable for the gate driving. A starving-resistor-based buffer is used to drive the last stage of the buffer chain to prevent shoot-through current. Due to the fixed-DC-terminal property with the operation of $S_1$ and $S_4$, charge pump-based level shifters (CPLS), as given in Fig. 6, with different types of cross-coupled transistors can be used to fulfill the driving requirements [28 29 30]. Considering $S_1$ as an example, the generated turn-on and -off gate-driving voltage are $V_{IN} - V_{DD}$ and $V_{IN}$, respectively. A similar control principle applies to $S_4$. Since $S_1$ and $S_5$ are floating switches (i.e., with no terminal connected to a DC voltage), bootstrapping driving techniques are necessary to generate floating voltage domains for the individual switches. The junction isolation level shifter (JILS), as shown in Fig. 6, shifts up the clock signal from $0-V_{DD}$ to $V_{SSH}$($V_{SSH}$+$V_{ch}$) domain, $V_{ch}$=$V_{DD}$ according to the node switching voltages of $V_{HH}$ and $V_{BB}$.

![Fig. 5 Implementation overview of the proposed converter system.](image)

![Fig. 6 Circuit implementation of the level shifters adopted in the proposed converter for switch control.](image)

4. Simulation results

The converter design validation is through full-transistor-level simulation at a switching frequency of $f_{SW}$=800kHz. The concerned losses include inductor DCR loss, switch $R_{ON}$ conduction loss, switching loss, switch gate driving loss, and shunt loss from the control building blocks. Considering the line-conduction loss caused by the practical parasitic effect, each power switch is in series with a line impedance of $\sim 10\,$m$\Omega$. A simulated loss-power breakdown is summarized in Fig. 7 for a 5V-to-1.8V conversion with an output current of 3A. It validates that the proposed MPSCI converter achieves improved overall efficiency compared with a buck converter implemented with the same total switch area and power inductor. From the pie chart, in contrast to the buck, the DCR loss reduction in the proposed converter is significant, and hence it attains a higher efficiency under a heavy load condition.

![Fig. 7 Complete loss breakdown comparison between the proposed MPSCI and conventional buck converters under a specific operating condition of $V_{OUT}$=1.8V and $I_{OUT}$=3A.](image)

Fig. 8 shows the simulated efficiency of the proposed MPSCI converter under different loading conditions and VCRs. From Fig. 8(a), this design ensures a PCE above 90% over a conversion range of 5V to 1.8-3.3V under 1A loading current. The peak efficiency can be up to 93.7%. When delivering a current of 2A, the total conduction loss increases, and the converter can still reach a 90% peak efficiency and maintain the overall PCE above 86%. Targeting on a maximum loading of 3A, the simulated result demonstrates a peak efficiency of 85.8%. Fig. 8(b) displays the simulated curves of PCE and DCR loss power together with a comparison between the proposed converter and the existing ones under a continuous loading current range and different $V_{OUT}$ of 1.8 and 2.5V. In contrast to the existing DP and conventional buck converters, the proposed MPSCI realized a DCR loss reduction up to 3.3 and 5.4 times and hence a PCE benefit of 7.1% and 15%, respectively, at a 1.8-V output. As the increase of the $V_{OUT}$ level, the DCR loss power takes less proportion among the total loss. On the other hand, although the relative DCR loss advantage attained by the proposed topology shrinks as the increase of the D, according to (3), it still realize a PCE advantage up to 2.3% and 11%, and a DCR loss reduction up to 1.5 and 3.
times when compared with the existing DP and conventional buck converter, respectively.

Fig. 9 shows the frequency-domain characteristics of the proposed converter. From the Bode plot, the power stage double poles locate around 16kHz, and the loop phase margin is 54° after the compensation. In contrast, the power stage phase margin is only 7° in the open-loop condition. Accordingly, the type-III compensator is adequate for stabilizing the voltage-mode control loop of the implemented converter system.

Fig. 10 depicts the time-domain transient waveforms of the proposed converter under a step response with the loading current from 0.5 to 3A. A ~10% $V_{OUT}$ overshoot/undershoot happens during the step-current transition and the recovery time is about 35μs. As observed, during the dead-time, the body diode of the power MOSFETs in the inductor current path is in forward conducting to provide a freewheeling path for the $I_L$, causing the diode voltage drop observed in the waveform. Besides, the $V_{OUT}$ ripple is about 30mV, which is majorly due to the ESR influence mainly.

The overall performances of the proposed converter are summarized in Table II and compared to the state of the art. From the table, this work achieves high efficiency and a high loading current level using a large-DCR inductor. In addition, the proposed topology achieves a higher inductor current reduction theoretically under a high step-down condition and hence demonstrates an advantage of delivering heavier loading current. It features significance for the efficiency optimization, owing to the improvement of the DCR loss.

### 5. Conclusion

This letter proposes a hybrid DC-DC converter technique that features multi-path output-charge conduction to achieve effective inductor current reduction and, therefore, a lower DCR loss. This property ensures the possibility of adopting a large-DCR power inductor with a shrunk volume in high-output-current delivery scenarios. A systematic analysis, design, and implementation methodology have been...
discussed. Through the simulation validation, in contrast to the existing techniques, the proposed topology demonstrates an extended VCR range down to 1/3 and a significant efficiency advantage when delivering a loading current up to 3A. Furthermore, the converter implementation attains a peak efficiency of 93.7% at 1A and 85.8% at 3A conditions.

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