Bulk-synchronous pseudo-streaming algorithms for many-core accelerators

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Abstract

The bulk-synchronous parallel (BSP) model provides a framework for writing parallel programs with predictable performance. An important class of parallel hardware in modern high-performance systems are many-core coprocessors. These often have limited locally memory, and can not be targeted by classic BSP programs. In this paper we extend the BSP model by introducing the notion of bulk-synchronous pseudo-streaming (BSPS) algorithms that are able to run on many-core coprocessors. We generalize the BSP cost function to these algorithms, so that it is possible to predict the running time for programs targeting many-core accelerators and to identify possible bottlenecks. To illustrate how to apply the novel framework, two simple examples of BSPS algorithms are explored. To ensure the portability of BSPS software, we propose a small number of additional primitives as an extension to the BSPlib standard. We introduce a software library called Epiphany BSP that implements the introduced concepts specifically for the Parallella development board. Finally, experimental results are given for BSPS algorithms on the Parallella board.

Keywords: Bulk-synchronous parallel, Streaming algorithm, Software library, Parallel scientific computing, Many-core coprocessor

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1. Introduction

The bulk-synchronous parallel (BSP) model, proposed by Valiant in 1989 [1], is a bridging model for parallel algorithms. The variant of the model we describe here, and use in the remainder of this article, differs slightly from the original model, and will form the basis of the new model that we propose. The BSP computer consists of \( p \) processors, assumed to be identical, which each have access to their own local memory. There is also assumed to be a communication network available which can be used by the different processor to communicate with each other. There are bulk synchronizations that ensure that all outstanding communication has been resolved. The time of such a synchronization, the latency, is denoted by \( l \). The communication cost per data word is denoted by \( g \). The parameters \( l \) and \( g \) are usually expressed in the number of floating-point operations (FLOPs), and are related to wall time through the computation rate \( r \) of each individual processor which is measured in floating-point operations per second (FLOPS). The four parameters \((p, g, l, r)\) define a BSP computer completely.

A BSP algorithm is structured in a number of supersteps. Each superstep consists of a computation phase and a communication phase. It is assumed that each processor can simultaneously send and receive data, and that there are no congestion effects in the network, so that the cost of communication is dominated by the maximum number of words sent or received by any processor. At the end of each step a bulk synchronization is performed. Each processor runs the same program, but on different data, which means that BSP algorithms adhere to the Single Program Multiple Data (SPMD) paradigm.

Each BSP algorithm has an associated cost, which can be expressed completely using the parameters of a BSP computer. We denote by \( w_i(s) \) the amount of work, measured in FLOPs, performed by processor \( s \) in the \( i \)th superstep. We denote by \( r_i(s) \) the number of data words received, and with \( t_i(s) \) the number of data words transmitted by processor \( s \) in superstep \( i \). Central to the communication cost of a superstep is the concept of an \( h \)-relation, which is defined as the maximum number of words transmitted or received by any processor during the superstep, i.e. \( h_i = \max_{0 \leq s < p} \max\{t_i(s), r_i(s)\} \). This leads naturally to the following cost, the BSP cost, of a BSP algorithm.
consisting of $k$ supersteps:

$$T = \sum_{i=0}^{k-1} \left( \max_{0 \leq s < p} w_i^{(s)} + g h_i + l \right).$$

*Streaming algorithms* are a class of algorithms that can be seen as processing methods for sequential data under typically two constraints:

1. The computer executing the algorithm has limited (local) memory $L$ available – typically much less than the total size $S$ of the input, i.e. $L \ll S$.

2. For each part of the input there is only a very limited amount of processing time available (e.g. it is required that the processing should be done in real-time).

Although the main ideas behind streaming algorithms have been studied since the 1980s, the first formal discussion was given in a 1999 article by Alon, Matias and Szegedy [2]. Many streaming algorithms, in particular because of the second constraint, are massively parallel and often employ randomized methods to provide an approximation (typically called a *sketch*) of the answer. The input of a streaming algorithm takes the form of a *stream* for which we will use the following definition:

**Definition 1.** A stream is an ordered and finite collection of $n$ tokens, which we write as

$$\Sigma = (\sigma_1, \ldots, \sigma_n).$$

Each token is a collection of data that fits in the predetermined local memory size $L$ of the machine processing the stream, i.e. the size satisfies $|\sigma_i| \leq L$.

Many additional constraints can be put on streaming algorithms. For example, they can be enforced to support data streams that can potentially be unbounded in size, or the tokens to be processed are not guaranteed to be presented in any predetermined order, or each token should be discarded or archived after a single pass; see e.g. [3]. In particular, streaming algorithms usually refer to algorithms which only use the input a constant number of times, in many applications even only a single time.

*Many-core coprocessors* are a class of energy-efficient accelerators which focus on massive parallelism. They differ from common multi-core processors
found in most desktop computers and servers, by having a large number of simpler processors that typically run at relatively low clock speeds. They can be found in many modern HPC systems. Because they are energy-efficient, they are also well suited for use in embedded environments. Algorithms that target these processors are closely related to streaming algorithms, since the constraints that have to be put on the programs strongly resemble the general setting of these algorithms. Furthermore, since the performance of a single processor core is limited, they are optimized for explicit parallel code. Examples of these many-core coprocessors include the Intel Xeon Phi family, the Adapteva Epiphany processor, the Movidius Myriad 2, the Kalray MPPA processors, and many others.

We propose a streaming framework within the BSP model which allows BSP algorithms to be generalized so that they can run on these many-core coprocessors with predictable performance.

In the remainder of this article we will discuss this streaming extension to BSP. In Section 2, we give a detailed description of this extension. In particular, we introduce the concept of a BSP accelerator and a bulk-synchronous pseudo-streaming algorithm. In Section 3, we will give a number of examples of algorithms that fit in this framework. In Section 4, we discuss the Parallella, which is a small parallel computer that will serve as a hardware example to which we can apply the theory that we introduce in this article. In Section 5, we discuss the Epiphany processor as a BSP accelerator. Finally, in Section 6 we discuss experimental results for BPS algorithms obtained with the Parallella board.

2. Streaming extension to the BSP model

Compared to common multi-core processors, many-core coprocessors lack coherent caches, and because of this it is very hard to scale to thousands of processors. Instead, software uses the local memory of each core as a partitioned global address space or as scratchpad memory. For explicit parallel programs, the program can only act on the data loaded into the local memory, and therefore an additional layer of software complexity is introduced that

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1In the June 2016 TOP-500 supercomputer ranking, the number two supercomputer TIANHE-2 uses Intel Xeon Phi coprocessors, while the fastest supercomputer in the world, the SUNWAY TAIHULIGHT, uses SW26010 many-core processors consisting of 256 cores each.
is, from the viewpoint of a computer programmer, traditionally handled by the hardware. This layer deals with the data flow between the larger pool of shared memory, and the local memory of each processor core. There is a pressing need for a parallel programming model that can target these systems, while being able to leverage existing algorithms. The approach we take in this article is to use a combination of BSP programs and streaming algorithms to handle this complexity.

**BSP accelerator**

We amend the notion of a BSP computer so that it describes more accurately modern many-core hardware, by defining the **BSP accelerator**. In a BSP accelerator, each processing element (in this context called a core) has limited local memory $L$. In addition, each core has an asynchronous connection to a shared external memory pool of size $E \gg L$. This type of connection is commonly available for the many-core coprocessors that motivate this model. We capture the bandwidth to the external memory pool with an additional parameter $e$, the *inverse bandwidth to external memory*, which is defined in FLOPs per data word similar to $g$. A BSP accelerator is completely defined by the parameter pack $(p, r, g, l, e, L, E)$.

In streaming algorithms, both limited local memory as well as limited processing time per data word are assumed. For a BSP accelerator, the processing time need not be limited, but we assume that the local memory is much less than the total input size. We are interested in streaming algorithms not because we want an approximate answer efficiently, but because the amount of local memory of each core of the coprocessor is only sufficient to act on a small part of the input at once.

The input to the algorithms that run on a BSP accelerator is structured into $n$ streams $\Sigma^{(i)}$, indexed with $1 \leq i \leq n$. These streams reside in external memory, but can be opened by the cores so that they can *stream data down* (read) and *up* (write) from/to a stream. These streams consist of a number of tokens $\sigma^{(i)}_j \in \Sigma^{(i)}$, where $1 \leq j \leq |\Sigma^{(i)}|$, and each token fits in the local memory of a core, i.e. $|\sigma^{(i)}_j| < L$.

The processing of tokens occurs in a *bulk-synchronous manner*, and is explained in more detail in the upcoming sections. The algorithms we describe here will be written in a SPMD manner, and we assert the completion of the current pass over a token for each processing core before moving on to the next.
Contrary to conventional streaming algorithms, where there is usually a strict order in which the tokens are processed, we are allowed to revisit or skip tokens at any given time. In particular we are free to reuse tokens an arbitrary number of times, and furthermore we assume that we have random access to the tokens within the stream, so that they can be processed in any order. This is similar to media streaming where it is possible to seek within a stream, allowing one to skip ahead, or revisit arbitrary parts of the audio or video content. After terminology that is common in that context, we will refer algorithms that run on BSP accelerators, which fit into a model that will be described in detail in the next section, as bulk-synchronous pseudo-streaming (BSPS) algorithms.

Hypersteps

At any given time, the BSP accelerator only has simultaneous access to a limited number of tokens. To cope with this constraint in a systematic manner, we structure the BSPS programs that run on BSP accelerator into a number of hypersteps. A hyperstep consists of two operations; 1) an (ordinary) BSP program that is performed on the tokens that are currently loaded into the cores, and 2) the fetching of tokens that will be used in the next superstep. Although the computations on a core are limited to the tokens that it has available in its local memory, it can communicate with the other cores of the BSP accelerator. After such a step, there is a global bulk-synchronization before every core moves on to the next hyperstep. This ensures that each core has all the tokens required for the next hyperstep available in its local memory. See also Figure 1. The data streams are prepared by an external processing unit which we will call the host, and for our purposes it is considered a black box.

Since we assume that there is an asynchronous communication mechanism with the external memory pool, obtaining the tokens for the next hyperstep (prefetching) can be done concurrently with the BSP program of the current hyperstep. In practice, the next tokens are written to a local buffer so that after a hyperstep the next hyperstep can be initiated as soon as possible. This minimizes the down-time within hypersteps, and is reminiscent of cache prefetching techniques. Note that prefetching data halves the effective local memory size, since storage needs to be reserved for the buffer that holds the next token.
Figure 1: Structure of a hyperstep for $p = 3$ processors and $n = 4$ streams. A hyperstep is a BSP program that is executed on the tokens currently loaded into the cores, together with the concurrent reading of tokens for the next hypersteps. At the end of a hyperstep each core waits until the tokens for the next hyperstep are loaded in for each core, and optionally streams a token containing the results of the hyperstep back up to a stream. Note that the time it takes to fetch the next token may vary between cores. Because the fetching of tokens, and the BSP program executed on the current tokens happens concurrently, the total time taken for a hyperstep is dominated by the slowest of the two operations.
**BSPS cost**

Next we want to generalize the BSP cost, and define the BSPS program consisting of $H$ hypersteps. Each hyperstep $0 \leq h < H$ has an associated BSP program, with a BSP cost $T_h$. In every hyperstep (except for the last, which is a technicality we will ignore) the next tokens are prefetched from the external memory $E$ with inverse bandwidth $e$. In our discussion we will set the size of a data word to be equal to the size of a *floating point number*. We will therefore allow ourselves to write ‘float’ when talking about message sizes and buffers. For simplicity we assume that the tokens of the $i$th stream have constant size $C_i$, and furthermore we assume that the first tokens are available for each core of the accelerator at the start of the program. The set of indices of the *active streams* of core $s$, i.e. the streams from which tokens are being read by the core, we will denote with $O_s$. The BSPS cost of a single hyperstep then corresponds to the maximum between the time spent processing the current tokens, denoted by $T_h$, and the time taken to fetch the next tokens. This leads to a natural definition for the cost function of a BSPS program:

$$\tilde{T} = \sum_{h=0}^{H-1} \max \left( T_h, e \max_{0 \leq s < p} \sum_{i \in O_s} C_i \right).$$  \hspace{1cm} (1)

If fetching the next token takes more time than processing the current token, then the running time of the hyperstep is bound by the memory bandwidth. If this happens, we say that the hyperstep is *bandwidth heavy*. Otherwise we say that the hyperstep is *computation heavy*.

The advantages of this pseudo-streaming paradigm for programming many-core processors include:

- Streams and tokens *guide* algorithm designers and implementers to use predictable and efficient access patterns when dealing with external data.

- The resulting algorithms are amenable to *precise run-time analysis*.

- The model provides a *simple way to describe and implement portable parallel algorithms for many-core accelerators*, and the library implementation we describe minimizes the necessary boilerplate.

We believe these advantages will ultimately lead to performant parallel algorithms and programs that will run across a variety of modern platforms.
Comparison with previous work

The main contribution of this paper is the new pseudo-streaming programming model that provides a convenient and portable way to develop algorithms for many-core accelerators. As we will show, a powerful feature of this paradigm is that existing BSP algorithms can be reused within hypersteps of BSPh algorithms, so that the programmer often only needs to worry about the communication with the shared external memory, for which streaming algorithms and techniques can be employed. This powerful interplay between streaming algorithms and BSP algorithms lead to elegant implementations of algorithms for many-core coprocessors.

The main distinction between the classic BSP performance model and the model we consider here, is the asynchronous fetching from external memory. Extensions to the BSP model that specify parameters for the memory size have already been studied before, see e.g. [9, 10]. In particular, there exists an external memory extension to the BSP model, EM-BSP [11], and many algorithms have been considered in this context [12]. In the EM-BSP model, each core has a synchronous connection to secondary local memories. Instead, we consider a single shared external memory pool, and algorithms optimized for limited local memory. The performance model we describe here is similar to the multi-memory BSP (MBSP) model [13], which supports multiple units of external memory. Compared to MBSP, the BSPh model has a simplified view of the accessible memory; since it only distinguishes between external and local memory, and has the important advantage of providing an explicit programming model that is well adapted to modern many-core accelerators and that can leverage ideas from BSP algorithms as well as from the large body of streaming algorithms that exist.

Another recent development is Multi-BSP [14], introduced as a model for writing portable parallel algorithms for general multi-core systems. The Multi-BSP model uses a tree structure to represent the memory hierarchy of a computer. In our view, this model is overly complicated for the architectures that we target with this work, and the explicit asynchronous prefetching we discuss can not be incorporated within the model.

Finally we note that although here we exclusively use BSP as our on-core model for the parallel programs that run during a hyperstep, there is a lot of flexibility in this choice, other on-core models can easily be incorporated into the BSPh cost function. We mention for example D-BSP [15], which allows for varying parameters between different clusters of cores, and which
may become relevant as the on-core model as the number of cores on a single chip increase.

3. Examples

In this section we will discuss two simple examples of algorithms that fit into the framework we described. First we will discuss BSPS algorithms for computing the inner-product of two vectors, and for performing the matrix multiplication of two dense matrices.

We use the following functions, with their usual semantics, in the descriptions of the algorithms:

| Function          | Description                                      |
|-------------------|--------------------------------------------------|
| \( \sigma \leftarrow \text{READ}(\Sigma) \) | read token \( \sigma \) from its stream          |
| \( \text{WRITE}(\sigma, \Sigma) \)         | write token \( \sigma \) to stream \( \Sigma \)   |
| \( \text{BROADCAST}(a) \)                  | send the value \( a \) to all other cores        |
| \( \text{SYNC} \)                          | perform a bulk-synchronization of all the cores  |
| \( \text{MOVE}(\Sigma, k) \)               | change the next token read off of \( \Sigma \) by \( k \) tokens. |

3.1. Inner-product

As a simple example to illustrate the main BSPS concepts, we will first consider the inner product of two vectors \( \vec{v}, \vec{u} \in \mathbb{R}^N \) of size \( N \), and construct a BSPS algorithm to compute

\[
\alpha = \vec{v} \cdot \vec{u} = \sum_{i=1}^{N} v_i u_i.
\]

Here, we assume that the total number of components \( v_i \) that can be stored at a single core is much smaller than the total size of the vector.

We begin by implicitly distributing the vectors over the processing cores of our BSP accelerator. In this discussion we will use a cyclic distribution of the vector so that \( v_i \) and \( u_i \) are assigned to the processor with index \( s = i \mod p \). Next we partition the resulting data for the \( s \)th core, which we will take as the streams \( \Sigma_s^\vec{v} \) and \( \Sigma_s^\vec{u} \), into a number of tokens, each of which will fit in a designated chunk of local memory with a certain token size \( C \), see also Figure 2.

Every core maintains a partial sum \( \alpha_s \) throughout the algorithm. We consider each pair of tokens (both consisting of \( C \) vector components) and compute locally the inner product of this subvector and add it to \( \alpha_s \). After
Figure 2: Here we depict the construction of the streams used in the inner-product problem. The stream shown here is $\Sigma_0^\vec{v}$, corresponding to the components of $\vec{v}$ assigned to the first processor. We consider $p = 3$ processors in total. Each token consists of $C = 2$ vector components, and the total stream size is $|\Sigma_0^\vec{v}| = 4$.

\begin{algorithm}
\textbf{Input:} $\Sigma_s^\vec{v} = \{\sigma_1^\vec{v}, \sigma_2^\vec{v}, \ldots, \sigma_n^\vec{v}\}$, $\Sigma_s^\vec{u} = \{\sigma_1^\vec{u}, \sigma_2^\vec{u}, \ldots, \sigma_n^\vec{u}\}$
\textbf{Output:} $\alpha = \vec{v} \cdot \vec{u}$

\begin{algorithmic}
\STATE $\alpha_s \leftarrow 0$
\FOR {1 $\leq$ \textit{i} $\leq$ \textit{n}}
\STATE $\sigma_i^\vec{v} \leftarrow \text{READ}(\Sigma_s^\vec{v})$
\STATE $\sigma_i^\vec{u} \leftarrow \text{READ}(\Sigma_s^\vec{u})$
\STATE $\alpha_s \leftarrow \alpha_s + \sigma_i^\vec{v} \cdot \sigma_i^\vec{u}$
\STATE $\text{BROADCAST}(\alpha_s)$
\STATE $\text{SYNC}$
\STATE $\alpha \leftarrow \sum_{t=0}^{p-1} \alpha_t$
\ENDFOR
\end{algorithmic}
\end{algorithm}

Algorithm 1: Summary of the BSPS algorithm for computing the inner product. After the completion of the algorithm every core of the accelerator will have computed the value $\alpha = \vec{v} \cdot \vec{u}$. This value can then be communicated back to the host.
every token has been considered, the combined partial sums of all the cores will be equal to the desired value for the inner product $\alpha$. Note that we can identify a token with a subvector, and we construct the streams for the two vectors in a completely identical manner. We summarize the algorithm in Algorithm 1.

Let us consider the BSPS cost of this algorithm. The total number of hypersteps is equal to $n = \frac{N}{pC}$. The last hyperstep is followed by an ordinary superstep in which the sum of partial sums is computed, where each processor sends and receives $(p - 1)$ data words. In each of these hypersteps we compute an inner product between two vectors of size $C$, taking $2C$ time, and this requires no communication. The total BSPS cost of this algorithm is:

$$T_{\text{inprod}} = n \cdot \max\{2C, 2Ce\} + p + (p - 1)g + l.$$  

We see that if $e > 1$ then the hypersteps are bandwidth heavy, otherwise they are computation heavy.

3.2. Dense matrix-matrix multiplication

The next algorithm we consider in this context is the product of two dense matrices, which are too large to fit completely in the local memory of the accelerator. The resulting algorithm will be an adaptation of Cannon’s algorithm [16] which computes this product on a square grid of accelerator cores.

**Cannon’s algorithm**

We first describe Cannon’s algorithm. We want to compute $AB = C$ for two matrices $A$ and $B$, and assume we have $N \times N$ processors. We index each processor core with a pair $(s, t)$. The matrices $A$, $B$ and $C$ are split into $N \times N$ blocks of equal size (padding with zeros if necessary):

$$A = \begin{pmatrix}
A_{11} & A_{12} & \cdots & A_{1N} \\
A_{21} & A_{22} & \cdots & A_{2N} \\
\vdots & \vdots & \ddots & \vdots \\
A_{N1} & A_{N2} & \cdots & A_{NN}
\end{pmatrix},$$

so that we can write for the resulting blocks of $C$:

$$C_{ij} = \sum_{k=1}^{N} A_{ik}B_{kj} \quad 1 \leq i, j \leq N.$$
We see that the resulting block $C_{ij}$ is the result of adding $N$ terms, in each of which a block of $A$ and a block of $B$ are multiplied. Since there are exactly $N \times N$ blocks $C_{ij}$, and $N \times N$ processors, it would be very natural to let each processor compute exactly one of these sums in $N$ steps. However there is one immediate problem: many blocks of $A$ and $B$ are needed simultaneously in the same step $k$, and we do not want to copy our blocks to every single processor since we assume that there is finite storage, and therefore limited room for duplication. Luckily, the sum above can be rearranged so that in step $k$ the processor requiring a specific block of $A$ or $B$ is unique, so that we never require any data redundancies. After computing a term, the matrix blocks that were used can be moved around to the processor that needs the block next. We let the processor with index $(s,t)$ compute the product:

$$A_{s,1+(t+s+k-3) \mod N} B_{1+(s+t+k-3) \mod N,t}$$

in the $k$th step. Next, we consider which processor needs the blocks of the current step after a processor is done with it. In the $(k+1)$th step, the processor $(s,t)$ needs the $A$ block that was previously owned by processor $(1+(s+t+k-3 \mod N),t)$ in the previous step, while the $B$ block was previously owned by $(s,1+(s+t+k-3 \mod N))$. In summary, we have the following scheme:

1. Perform an initial distribution of the matrix blocks over the $N \times N$ processors, sending $A_{i,j} \mapsto (i,1+((i+j-2) \mod N))$ and $B_{i,j} \mapsto (1+((i+j-2) \mod N),j)$.

2. Let each processor compute the product of the two local matrix blocks of $A$ and $B$, adding the result to $C_{st}$.

3. Next each processor sends the matrix block of $A$ to the right, i.e. to processor $(s,1+(t \mod N))$, and each matrix block of $B$ down to processor $(1+(s \mod N),t)$. We repeat steps 2 and 3 a total number of $N$ times.

The resulting matrix product $C$ will then be available distributed over the processors. We wil refer to this algorithm in the program text as CANNON.

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Note that the indices would be much more straightforward had we used 0-based indices for our matrices, but we will stick with 1-based indices in this discussion for consistency.
Multi-level Cannon’s algorithm

We will now generalize this algorithm to a BSPS variant. The method we discuss here is similar to the one described in e.g. [17]. The distribution scheme that we derived in the previous section will not suffice in general for BSP accelerators, since for reasonably large matrices, dividing them into $N \times N$ blocks will not make them small enough so that they can be stored in the local memory of the cores. Thus, we need to reduce these sub-problems in size even further. We do this by subdividing the matrix in two levels. The first level will no longer consist of $N \times N$ blocks, but of $M \times M$ blocks, where $M$ is taken suitably large. Each of these blocks will be divided further in $N \times N$ blocks, which will be distributed over the cores in the method described above.

For example $A$ will now look like this:

$$\begin{pmatrix}
A_{11} & A_{12} & \ldots & A_{1M} \\
A_{21} & A_{22} & \ldots & A_{2M} \\
\vdots & \vdots & \ddots & \vdots \\
A_{M1} & A_{M2} & \ldots & A_{MM}
\end{pmatrix}$$

where each outer block $A_{ij}$ is divided further as:

$$A_{ij} = \begin{pmatrix}
(A_{ij})_{11} & (A_{ij})_{12} & \ldots & (A_{ij})_{1N} \\
(A_{ij})_{21} & (A_{ij})_{22} & \ldots & (A_{ij})_{2N} \\
\vdots & \vdots & \ddots & \vdots \\
(A_{ij})_{N1} & (A_{ij})_{N2} & \ldots & (A_{ij})_{NN}
\end{pmatrix}.$$  

In total we then have $MN \times MN$ blocks. We can choose our value of $M$ such that the resulting smaller blocks $(A_{ij})_{kl}$ are small enough to fit in the local memory of the cores. Let us now turn our attention to constructing the streams. We will consider the $M^2$ blocks of $A$ in row-major order, and the $M^2$ blocks of $B$ in column-major order. The blocks will form the tokens, and will all be considered $M$ times. In every hyperstep we will compute the product of two blocks using Cannon’s algorithm introduced above. To construct the stream, we will denote with e.g. $(A_{ij})_{st}$ the first inner block that the processor $(s,t)$ receives when computing a product involving the outer block $A_{ij}$. We define $(B_{ij})_{st}$ in a similar manner. We are now ready to
define the streams:

\[
\Sigma^A_{st} = (A_{11})_{st}(A_{12})_{st} \cdots (A_{1M})_{st} (A_{21})_{st}(A_{22})_{st} \cdots (A_{2M})_{st} \\
\cdots (A_{M1})_{st}(A_{M2})_{st} \cdots (A_{MM})_{st},
\]

\( \circ \ M \) times

and

\[
\Sigma^B_{st} = (B_{11})_{st}(B_{21})_{st} \cdots (B_{M1})_{st}(B_{12})_{st}(B_{22})_{st} \\
\cdots (B_{M2})_{st}(B_{13})_{st} \cdots (B_{1M})_{st}(B_{2M})_{st} \cdots (B_{MM})_{st}.
\]

\( \circ \ M \) times

Here, we indicate with \( \circ \) the order in which we consider the tokens, so that \( \circ \ M \) means that we will repeat looping over that particular section of blocks \( M \) times before moving on to the next section of blocks. Note that each block is only stored in the stream once. We will loop over groups of \( M \) blocks of \( A \) a number of \( M \) times before moving to the next, while we simply loop over the \( M^2 \) blocks of \( B \) a total number of \( M \) times. After constructing these streams, from the perspective of an accelerator we have to multiply the two tokens, corresponding to the outer matrix blocks, given to us in each of the \( M^3 \) hypersteps. This is done by computing the product of the two blocks with the general Cannon’s algorithm, which can now be applied since we have chosen the outer blocks to be of small enough size. The result of this product is added to the block \( C_{ij} \) that is currently being computed. After every \( M \) hypersteps we have completely computed one of the \( M^2 \) blocks of \( C \), and we store the result in the external memory \( E \).

Let us consider the BSPS cost of this algorithm. First we will derive the BSP cost of Cannon’s algorithm. There are \( N \) supersteps in which we compute the product of two inner blocks of size \( k \times k \equiv \frac{n}{NM} \times \frac{n}{NM} \), which takes \( 2k^3 \) flops. Next we send and receive such an inner block consisting of \( k^2 \) words. Note that we do not send or receive such a block in the final superstep, but for simplicity we will ignore this. The BSP cost equals:

\[
T_{\text{cannon}} = N(2k^3 + k^2g + l).
\]

The number of values in a token, the token size \( C \), is given by the number of values in an inner block which is equal to \( k^2 \). For simplicity, we will ignore
Algorithm 2: Summary of the BSPS version of Cannon’s algorithm that runs on core \((s, t)\). Here, \(\vec{0}\) denotes an array of zeros.
the costs of storing the resulting blocks. There are $M^3$ hypersteps, so that we can write for the BSPS cost of this algorithm:

$$\tilde{T}_{cannon} = M^3(\max(N(2k^3 + 2k^2g + l), 2k^2c)),$$

(2)

Alternatively, after substituting back $k$, we can write for the total cost:

$$\tilde{T}_{cannon} = \max\left(2\frac{n^3}{N^2} + \frac{2Mn^2}{N}g + NM^3l, 2\frac{Mn^2}{N^2}e\right).$$

4. Streaming extension to BSPlib

In this section we propose a streaming extension to the BSPlib standard [18]. This initial proposal targets simple streaming applications. The BSPlib standard has been extended previously with high-performance primitives [19], which we have adopted. In addition, we introduce a number of new primitives that can be used to write BSPS programs. A BSPS program consists of a host program that runs on the host, and a kernel that runs on the cores of the accelerator. For a more detailed specification of these new primitives we refer to the Epiphany BSP documentation [20], which is a software package that provides implementations for the primitives introduced here.

The host of a BSP accelerator needs to be able to create streams of data. To create a stream we have to specify respectively the total size, the size of the tokens, and optionally it is possible to set the initial data of the stream.

```c
void * bsp_stream_create (int stream_size, int token_size,
const void * initial_data);
```

This is the only new primitive that is called from the host. The return value is a pointer to a buffer for the data in the stream. Streams are given an identifier `stream_id` in order of creation, starting from index 0 and increasing by one each time a stream is created. Inside a kernel program, streams can be opened and closed using the following primitives:

```c
int bsp_stream_open (bsp_stream * stream, int stream_id);
int bsp_stream_close (bsp_stream * stream);
```

Here, `bsp_stream` is a C struct that holds the required information for a stream.

Streams are shared between cores. Streams can only be opened if they are not yet opened by another core. After opening a stream, tokens can be
obtained from it. After closing the stream any core can open it again. The return value is equal to the maximum size of a token in bytes.

Tokens can be moved down from open streams. Furthermore, data can be streamed back up to the streams, i.e. the streams are mutable. For this the following primitives are used:

```c
int bsp_stream_move_down(bsp_stream* stream, void** buffer,
                         int preload);
int bsp_stream_move_up(bsp_stream* stream, const void* data,
                       int data_size, int wait_for_completion);
```

These functions return the size in bytes of the buffer that will hold the next token. The location of this buffer is written to *buffer. The argument preload should be set to either 0 or 1, this respectively disables, or enables prefetching (see Section 2) the next token. The parameters of the second function are self-explanatory.

It is possible to (re)use a token at different stages of your algorithm. A cursor is maintained for each stream which corresponds to the next token that should be obtained or written to. This cursor can be modified using the following primitive:

```c
void bsp_stream_seek(bsp_stream* stream, int delta_tokens);
```

Here delta_tokens denotes the number of tokens the cursor should move, relative to the current position. Note that this mechanism gives us random access inside the streams.

5. The Epiphany processor as a BSP accelerator

The Parallella\(^3\) is a “credit card-sized computer” intended to make parallel programming accessible and open to a large community. It is similar to other small-form computing platforms such as the popular Raspberry Pi\(^4\) and Arduino\(^5\).

The Parallella board has basic network capabilities and support for a number of peripherals. There are two different processors available. The

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\(^3\)Parallella: a supercomputer for everyone. [https://www.kickstarter.com/projects/adapteva/parallella-a-supercomputer-for-everyone](https://www.kickstarter.com/projects/adapteva/parallella-a-supercomputer-for-everyone)

\(^4\)Raspberry Pi: a low cost, credit-card sized computer: [https://www.raspberrypi.org/](https://www.raspberrypi.org/)

\(^5\)Arduino: an open-source electronics platform [https://www.arduino.cc/](https://www.arduino.cc/)
Figure 3: Overview of the Parallella memory. There are three kinds of memory: (A) 32 kB local memory per core, (B) 32 MB of shared DRAM, (C) 1 GB of main DRAM. We also give an indication of the relative speed of the different memory lanes that are available. There is also a slow connection between the host and the local memory of each core which we do not use and will therefore ignore.

host processor, which runs the (Linux) operating system, is a dual-core ARM processor. The coprocessor on the Parallella board is based on the Epiphany architecture which has 16 RISC (Reduced Instruction Set Computer) cores. The Epiphany processor architecture [21] defines a square grid of cores of size $N \times N$. On the processor there is also a network-on-chip (NOC) present. There is support for single-precision floating point operations. The chip supports core-to-core communication on the processor with very low latency (in the order of nanoseconds) and zero start-up costs. Besides the 16 core Epiphany-III processor, there has also been a limited production of Parallella boards with the Epiphany IV processor which has 64 cores. The Epiphany-V coprocessor has recently been announced. Although it is not yet available, it will have 1024 cores and has support for double-precision operations [22]. We distinguish between three layers of memory on the Parallella board. There is 1GB of RAM available, which is split into two parts; The largest part is exclusive to the host processor, and we will simply refer to it as RAM. A relatively small section is shared between the host and the Epiphany, and is called the DRAM (or dynamic memory). Finally, there is 32 kB of local memory present at each core, which we will refer to as the SRAM (or static memory). See Figure 3. An important feature is the availability of two direct memory access (DMA) engines at each Epiphany core. These allow for asynchronous reading and writing between Epiphany cores, and between the (local memory of) Epiphany cores and the dynamic memory, and will play an important role in our implementation of pseudo-streaming algorithms.

5.1. Epiphany BSP

We developed Epiphany BSP [20] (EBSP) as an implementation of the BSPlib standard [18] on top of the Epiphany SDK provided for the Parallella. It is released under the lesser GNU public license (LGPL). Other libraries and technologies that are supported on the Parallella include MPI [17], OpenMP
Table 1: The communication speeds to shared memory that were obtained from measurements done during the development of Epiphany BSP. In the network state column we indicate if a single core is reading/writing (free) or if all cores are reading/writing simultaneously (contested). All the speeds are given per core.

| Actor | Network state | Read      | Write     |
|-------|---------------|-----------|-----------|
| Core  | contested     | 8.3 MB/s  | 14.1 MB/s |
|       | free          | 8.9 MB/s  | 270 MB/s  |
| DMA   | contested     | 11.0 MB/s | 12.1 MB/s |
|       | free          | 80.0 MB/s | 230 MB/s  |

[23], Erlang [24], and OpenCL [25].

A typical Epiphany BSP application consists of two separate programs. The host program configures the application and prepares the data to be processed by the Epiphany coprocessor. The kernel is a program that runs on each of the Epiphany cores in a SPMD manner. All the communication between Epiphany cores, and between the host and the coprocessor can be done using the conventional BSP methods and syntax (e.g. buffered and unbuffered writes or through message passing mechanisms). A major goal of the development of EBSP is to allow current BSP programs to be run on dual-processor hardware such as the Parallella with minimal modifications.

The Epiphany BSP library also provides many utilities to ease the development of BSP applications for the Parallella board, such as timers, dynamic memory management and debugging capabilities. Finally, EBSP also provides an extension to BSP to support streaming algorithms. We will introduce and formalize this extension in the next section.

We will consider the Epiphany-III 16-core Microprocessor (E16G301) chip that is found on the original Parallella board as a concrete example of a BSP accelerator. As we mentioned when we introduced the Parallella in Section 4, the Epiphany chip is connected to a portion of memory called the DRAM which we will take as our external memory E, and each core comes equipped with a DMA engine which gives us an asynchronous connection to this memory pool. There are many possible communication paths between the host, the Epiphany and the various kinds of memory. We are interested in estimating as accurately as possible the inter-core communication speed g, the latency l, and the read/write speed e from an Epiphany core to the external memory using the DMA engine.

We summarize the results of a number of measurements of the memory
Figure 4: Different read and write speeds from a single core to external-memory when the network is free (no other cores are active). The horizontal axis shows the size of the data that was being written or read and the vertical axis shows the speed in MB/s. Because there is a small overhead associated with reading or writing to external memory the speeds are slow for very small sizes. Burst refers to hardware support for faster memory writes that is activated when consecutive 8-byte writes are performed. The non-burst writes are to non-consecutive locations. A possible explanation for the jumps in the blue line (write + burst) is that the burst mode gets interrupted after a specific number of bytes have been written. The non-monotonic behaviour of the green line (write) is due to a buffering effect of the Epiphany network mesh.
speed of the Parallella that we performed in Table 1. In Figure 4 we show the results of one particular such measurement, regarding the reading and writing to external memory in a non-contested network state. From these results we can estimate $e$. Note that there is a significant difference between the read and write speeds when multiple cores are communicating with the external memory at the same time. We will choose to use the most pessimistic number, the read speed using the DMA engine from the external memory with a contested network state, since we expect that all cores will simultaneously be reading from the external memory during a hyperstep. We have found experimentally that a core of the Epiphany-III chip is on average performs the equivalent of one FLOP per 5 clock cycles in representative programs implementing BSPS algorithms that are compiled using GCC 4.8.2. We do note however that with hand-optimized assembly code as many as the equivalent of two FLOPs per clock cycle can be performed when performing multiplications and additions in succession, but we will not make use of this to preserve generality, so that the values we present are valid for real world BSPS algorithms implemented on top of Epiphany BSP. We then find that the external inverse bandwidth for this platform is:

$$e \approx (11 \text{ MB/s})^{-1} \approx 43.4 \text{ FLOP/float},$$

where we used that an Epiphany core runs at a default frequency of 600 MHz. Also we use single-precision floats which have a size of 4 bytes on this platform. Note that from a practical perspective, this value for $e$ is sometimes prohibitively high, which means that we need to perform a large number of FLOPs with every floating point number we obtain or the time of a hyperstep will have the bandwidth as a bottleneck. This is an obvious limitation of the Parallella board, and is specific to this computer. We note that this high value for $e$ is not a general property of the Epiphany chip (nor any other BSP accelerator). For $g$ and $l$ we fit a linear function against the raw measurements that were obtained for core-to-core writes for a varying number of bytes. We note that the Epiphany hardware is such that this specific type of communication does not suffer from the large discrepancies between simultaneous and non-simultaneous communication of multiple cores. After compensating for overhead because of the hardware clock that was used to
perform the measurements\footnote{Starting and stopping the hardware clock takes a specific, fixed number of clock cycles. This offset has been subtracted from our measurements.}, we obtain for the barrier time (the latency):

\[ l \approx 136 \text{ FLOP}, \]

and for the inverse bandwidth of inter-core communication:

\[ g \approx 5.59 \text{ FLOP/float}. \]

We note that this is an upper bound, because one can obtain a value of \( g \) lower than 1 FLOP/float when using only optimized writes instead of reads. Furthermore, the startup cost of inter-core communication is less than one FLOP so the value of \( l \) is almost entirely due to the synchronization mechanism and not due to starting up communication.

6. Experimental results

6.1. Cannon’s algorithm

We have implemented Cannon’s algorithm for dense matrix multiplication as discussed in Section 3 and measured the running time for different parameters on the E16G301 chip found on the Parallella-16 micro-server with the Zynq 7010 SOC. The benchmark, which is part of the Epiphany BSP library, was compiled with GCC 4.8.2 using the Epiphany SDK version 2016.3. The results are shown in Figure 5. The BSPS cost function of the algorithm, Equation 2, shows that the number of FLOPs required for computing the multiplication does not depend on \( M \) (first term) but the communication volume (second and third term) does scale with \( M \). Indeed, we expect a higher value of \( M \), which results in a smaller block size, to give a higher run time and this is in agreement with the results in Figure 5. The block size should always be chosen as large as the limited amount of local memory allows.

Equating the left and right hand side of Equation 2 and solving for \( k \) using the values we have found for the Epiphany processor yields \( k_{\text{equal}} \approx 8 \). Here, \( k_{\text{equal}} \) corresponds to the boundary values for computation heavy and communication heavy hypersteps. As shown by Figure 5 this corresponds to the transition of communication heavy hypersteps to computation heavy
hypersteps, and this is verified by our experiments. This shows that the BSPS cost function is a good way to identify possible bottlenecks for a BSPS algorithm, as well as being able to predict its running time.

7. Future work

There is still a wide range of algorithms in e.g. numerical linear algebra, scientific computing or computational geometry that we have not considered in this context but for which there exist efficient algorithms within the BSP model. We have some preliminary work on sparse matrix vector multiplication and external sorting within the BSPS model.

Furthermore, there are many real-world applications to be explored. As an example, we imagine applying the BSPS cost function to real-time video processing, where a frame is analyzed in each hyperstep. Here we could
require the hypersteps to be bandwidth heavy to ensure that we are able to process the entire video feed in real-time.

While we focus on many-core coprocessors in this article, the same principles hold for any type of hardware that has to process data that is too large to fit in working memory. Therefore, these streaming algorithms may also be applied in Big Data contexts.

Finally, it would be interesting to consider models in which there are different types of processing units, and to develop models that uses the BSP and BSPS costs to distribute the work of a single algorithm in this heterogeneous environment.

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