Titanium Nitride Film on Sapphire Substrate with Low Dielectric Loss for Superconducting Qubits

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Dielectric loss is one of the major decoherence sources of superconducting qubits. Contemporary high-coherence superconducting qubits are formed by material systems mostly consisting of superconducting films on substrate with low dielectric loss, where the loss mainly originates from the surfaces and interfaces. Among the multiple candidates for material systems, a combination of titanium nitride (TiN) film and sapphire substrate has good potential because of its chemical stability against oxidization, and high quality at interfaces. In this work, we report a TiN film deposited onto sapphire substrate achieving low dielectric loss at the material interface. Through the systematic characterizations of a series of transmon qubits fabricated with identical batches of TiN base layers, but different geometries of qubit shunting capacitors with various participation ratios of the material interface, we quantitatively extract the loss tangent value at the substrate-metal interface smaller than $8.9 \times 10^{-4}$ in 1-nm disordered layer. By optimizing the interface participation ratio of the transmon qubit, we reproducibly achieve qubit lifetimes of up to $300 \mu s$ and quality factors approaching 8 million. We demonstrate that TiN film on sapphire substrate is an ideal material system for high-coherence superconducting qubits. Our analyses further suggest that the interface dielectric loss around the Josephson junction part of the circuit could be the dominant limitation of lifetimes for state-of-the-art transmon qubits.

INTRODUCTION

In superconducting quantum computing, sufficiently long qubit coherence times compared to the time scales of operations are the foundation of realizing practical quantum computation. In the past two decades, the coherence times of superconducting qubits have been improved by more than five orders of magnitude through innovations in qubit design as well as the mitigation of decoherence sources [1]. Among the diverse decoherence channels [2], dielectric loss has been indicated to be ubiquitous, and has been the center of a few coherence-time breakthroughs [3, 4] regarding the transmon platform.

The lifetime of a qubit, also known as the energy relaxation time $T_1$, is directly related to the circuit quality factor $Q = \omega_q T_1$, where $\omega_q$ is the qubit frequency. Regarding a transmon qubit, which is weakly anharmonic [5], the dielectric-loss part of $Q$ can be decomposed into contributions from various materials or regions as

$$Q^{-1} = \sum_i P_i \tan \delta_i.$$  \hspace{1cm} (1)

Here, $i$ is the index indicating different spatial regions; $P_i$ is the participation ratio (PR) of the $i$-th region, representing the proportion of the electric energy stored in that part to the total electric energy of the qubit; and $\tan \delta_i$ characterizes the intrinsic dielectric loss of the $i$-th region.

It is intuitive that the region with the largest PR, usually, the bulk of the substrate due to its large volume and dielectric constant, would be the most crucial part of the dielectric loss. However, previous studies show that, the small-volume regions at the interfaces of the qubit structure contribute more significantly to dissipation because of their large $\tan \delta$ values [6–11]. In a superconducting qubit, the typical interface regions are the substrate-metal (SM), substrate-air/vacuum (SA), and metal-air/vacuum (MA) layers illustrated in Fig. 1(d).

To lower the dielectric loss, $P_i$ and $\tan \delta_i$ are two independent variables that can be optimized. However, because of the strong correlation between PR and qubit geometry which will be discussed later, the optimization of $P_i$ incurs potential trade-offs with regard to the device structure, footprint size, and measurement configurations. Therefore, reducing the $\tan \delta$ values of the interfaces with respect to the material and fabrication, is a general and fundamental approach for reducing dielectric loss despite specific qubit designs. In addition to the aluminum (Al) film on silicon substrate which is widely used in the community, people actively explored other material systems and the corresponding fabrication processes for low dielectric loss. For example, titanium nitride (TiN) film on silicon substrate has been explored in various devices [8–12]. Recently, a study of tantalum film on sapphire substrate reported low dielectric loss in a two-dimensional (2D) transmon qubit [4, 13]. Long-lifetime 2D transmon qubits fabricated with niobium film on silicon substrate have been applied as sensitive probes to characterize other dissipation mechanisms [14]. In these previous studies, a qubit quality factor in the 5-
10 million range was achieved by utilizing high-quality material systems and optimizing the corresponding fabrication processes. Further improvements in the qubit lifetime would require a quantitative understanding of the loss mechanism in the circuits and its correspondence to the underlying material properties.

In this work, we report our study on TiN film deposited onto sapphire substrate as a material system providing low dielectric loss at the SM interface. We select TiN as the superconductor because of its chemical stability against oxidation, and ability to form clean interfaces on certain substrates [15–17]. With regard to the substrate, sapphire is selected for its highly passive surface, and extremely low dielectric loss [18]. To characterize quantitatively $\tan \delta_{\text{SM}}$, we systematically measure the $Q$ of 2D and three-dimensional (3D) transmon qubits fabricated with identical batches of TiN base layers depending on the $P_{\text{SM}}$. The value of $P_{\text{SM}}$ covers a range of more than two orders of magnitude by varying the design of the qubit shunting capacitor. The experimental data from all the qubits are consistent with a single model comprising only the interface dielectric loss of the TiN shunt capacitors and that of the Josephson junction part of the circuits. We extract a dielectric loss of the TiN film on sapphire substrate of $\tan \delta_{\text{SM}}$ less than $8.9 \times 10^{-4}$ in a 1-nm-thick disordered layer and a dielectric loss of the interfaces around the Al junctions of $\tan \delta_J 3.5 \times 10^{-3}$. By optimizing the $P_{\text{SM}}$ values of the transmon qubits, we reproducibly achieve qubit lifetimes up to 300 $\mu$s and quality factors approaching 8 million.

**DESIGN AND FABRICATION**

Regarding the interface region, $P_i$ ($i = \text{SM, SA, MA}$) can be described as [6, 9]

$$ P_i = \frac{1}{2} \epsilon_i \int_0^{t_i} dt \int_{S_i} |E|^2 ds / U_{\text{tot}} $$

where $t_i$, $\epsilon_i$, $S_i$, and $E$ are the thickness, dielectric constant, in-plane geometry, and electric field of the $i$-th interface region, and $U_{\text{tot}}$ is the total electric energy of the qubit. Usually, because the thicknesses of the interface layers are much smaller than the dimensions of the qubit’s in-plane geometry, the electric field can be assumed to be uniform across these thicknesses. Among the three regions listed above, the SM interface catches our attention: on the one hand, the SM interface usually has major PR values in the common designs of coplanar waveguide cavities and qubits [7, 8, 19, 20]; moreover, $\tan \delta_{\text{SM}}$ is sensitive to the selection of material and the method of fabrication, and lacks well-tested post process for further improvement, such as those applied on other interfaces [7, 10, 21].

In Eq. 2, $S_{\text{SM}}$, the integral limit of the SM interface, is determined by the geometry of the superconducting metal. In our design of the transmon qubit, we apply varied geometries of the qubit’s shunting capacitor in different regimes of $P_{\text{SM}}$. For the 2D transmon qubits with large $P_{\text{SM}}$ values, we select the interdigital geometry which shows an ability to distribute more energy in the SM interface region [20]. We keep the widths of the gap and finger identical, and vary them together to reduce the number of variables in our design of the interdigital capacitor. The amount and length of fingers are tuned correspondingly to achieve the target values of capacitance. Meanwhile, in the small-$P_{\text{SM}}$ regime, we use the dumbbell geometry of the shunting capacitor for the 2D transmon qubit. The minimal $P_{\text{SM}}$ in our study is achieved by combining the dumbbell geometry with the 3D configuration. The transmon qubits with varied geometries described above are demonstrated in Fig. 1(a)-(c).

For each geometry, we apply an independently developed electrostatic solver to simulate the $P_{\text{SM}}$ values of the varied shunting capacitor designs [22]. The other inputs required in the simulation (i.e., $t_{\text{SM}}$ and $\epsilon_{\text{SM}}$) will be discussed later. Focusing on the SM interface between the TiN film and sapphire substrate, we do not include the contribution from the Josephson junction region. The
simulation result of the interdigital geometry plotted in Fig. 1(e) shows that, by varying the gap and finger widths in a range of 1-20 µm, we can change the $P_{SM}$ from approximately $2.1 \times 10^{-4}$ to $3.3 \times 10^{-3}$. By extending the lower boundary of the $P_{SM}$ with the dumbbell geometry and 3D configuration, we achieve a series of transmon qubits covering a range of $P_{SM}$ values of more than two orders of magnitude, which is beneficial for the fitting and analysis of the experimental data to obtain a reasonable estimation of $\tan \delta_{SM}$.

The transmon qubits in this study are fabricated in two steps, namely the TiN base layer fabrication and the Josephson junction fabrication. We first deposit the 100-nm-thick TiN films on the c-plane sapphire substrates via a magnetron sputtering system. The deposited TiN films are then capped with SiNx layers serving as inorganic hard masks [23]. Patterns including the qubit shunting capacitors, the readout cavities, and the qubit drive lines are first lithographically defined by a direct-write-laser system, and then transferred to the SiNx hard mask layers via dry etching. In the open regions of the hard masks, the TiN films are etched in the SC-1 solution of RCA clean [24]. After the stripping of the SiNx hard mask layers with diluted hydrofluoric acid (HF), the TiN base layers with the desired geometries are released. In the next main step, we fabricate the Al/AIOx/Al Josephson junctions using the “Manhattan” technique [25, 26]. The patterns of the junctions are defined by e-beam lithography, followed by ion milling to remove the possible residuals from the development and to clean the contact regions between the TiN base layers and Al leads. By utilizing the shadowing effects of the e-beam resist patterns, we sequentially deposit the Al leads of the junction in two orthogonal directions, with an in situ oxidation process between the two evaporation steps to form the AIOx insulating barriers.

To obtain the parameters required by the simulation of the $P_{SM}$, we characterize the cross section of the TiN film on the sapphire substrate with transmission electron microscopy (TEM), and demonstrate the results in Fig. 2. The image of the SM interface shows that, there is a thin, disordered layer with a thickness of approximately 1 nm between the TiN film and sapphire substrate, implying that the main component of this layer could be AIOx. Therefore, we use the value of sapphire’s dielectric constant (10.15 $\epsilon_0$, where $\epsilon_0$ is the vacuum permittivity) as the $\epsilon_{SM}$. As a typical value for many metal oxides, an $\epsilon_{SM}$ of approximately 10 $\epsilon_0$ is widely adopted in the simulation of PR [8].

We also check the morphologies of the MA and SA interfaces with TEM, as shown in Fig. 2(b) and (c). The images indicate that, the lattices of the crystalline TiN and sapphire extend to their surfaces without an obvious disordered layer, implying that the MA and SA interfaces are expected to show insignificant contributions to the dielectric loss. The high-quality MA and SA interfaces could benefit from the process designs of TiN wet etching, SiNx layer stripping, and the chemical stability of the TiN-sapphire material system. Briefly, as the wet etchant of TiN is effectively a remover for organics and certain metallic contaminants [27], etching TiN film with SC-1 solution could be accompanied by in situ decontamination. In the subsequent SiNx layer stripping, the HF-based process also provides an effective post cleaning for the material stacks to further reduce the dielectric losses at the MA and SA interfaces [10, 21]. Moreover, the chemical stability of TiN guarantees its compatibility with sufficient HF treatment, and suppresses the regeneration of the lossy dielectric layer from oxidation. Although disordered layers are not observed at the MA and SA interfaces through TEM imaging, their possible contributions to the dielectric loss are discussed later.

RESULTS AND DISCUSSION

We characterize our transmon qubits with the standard $T_1$ measurement [28]. To reduce the potential influence of the temporal fluctuation of qubit performance [29–31], we repeat the measurement approximately 100 times, and use the average $T_1$ as the representative value for data analysis [32]. The typical measurement result is demonstrated in Fig. 3. The relaxation of qubit generally shows an expected, single-exponential decay behavior, and the statistic of $T_1$ has a relatively concentrated distribution. In our systematic measurements, 13 designs of transmon
qubits with different $P_{SM}$ values on 5 kinds of dies are tested. For each kind of die, multiple samples picked out randomly from the identical wafer are measured to check the reproducibility [33]. On our best device, a time-averaged relaxation time $T_1$ of 291.7 ± 68.6 µs is measured. More details of the sample and measurement are available in the Appendix.

Fig. 4(a) summarizes the experimental data of our measurements. As a well-known extrinsic limit on $Q$ of qubits, the dissipation from the Purcell effect induced by the readout cavity is subtracted from each data point presented here [34]. We find that the measured $Q$ values increase monotonically with a decrease in $P_{SM}$, which is qualitatively consistent with the expectation of the dielectric loss at the SM interface. However, there is an obvious deviation between the experimental data and the prediction made by a simple model counting SM interface dielectric loss only. Although the data points in the large-$P_{SM}$ regime generally follow the straight line predicted by the simple model, the $Q$ values in the small-$P_{SM}$ regime are systematically smaller than the expected values, resulting in a variation in $\tan\delta_{SM}$ between $7 \times 10^{-4}$ and $5 \times 10^{-3}$ (gray shaded zone), depending on the choice of data points. This observation implies that, in addition to the readout-cavity-induced Purcell effect, which is removed from each data point, there is other dissipation mechanism independent of the SM interface dielectric loss in the shunting capacitor region. Following Eq. 1, we add a phenomenological parameter $Q_0$ and fit the data with $Q^{-1} = P_{SM} \tan\delta_{SM} + P_3 \tan\delta_1$. The fitting result is plotted in Fig. 4(a) as the black line, which matches the experimental data better than that from the simple model (black dashed line as an example). Based on the patched model, we get a $\tan\delta_{SM} \simeq 8.3 \times 10^{-4}$ and a $Q_0 \simeq 7.1 \times 10^6$.

Regarding the physical origin of the $P_{SM}$-independent $Q_0$, we hypothesize that it is correlated with the dissipation induced by the Josephson junction regions. Since all the qubits share a similar geometry of the junctions not included in the simulation of $P_{SM}$, it is reasonable to expect that the energy loss induced by the junction region is universal for all the transmon qubits in our measurements. To verify this hypothesis, we further simulate the PR of the junction region by assuming that the dissipation there is still dominated by the dielectric losses at the interfaces. Similar to the PR simulation of the shunting capacitor region, the thickness of the potential lossy layer at each interface (i.e., SM, SA, and MA) is characterized by TEM [35]. The characterization shows that, in addition to the approximately 1-nm-thick disordered layer at the SM interface, the amorphous layer at the MA interface has a thickness of approximately 5.5 nm, indicating a nonnegligible $P_{MA}$. Therefore, we count all the PR values in the junction region together as $P_3$, and characterize the intrinsic dielectric losses of the interface regions with an overall $\tan\delta_1$. Then, we fit the data with $Q^{-1} = P_{SM} \tan\delta_{SM} + P_3 \tan\delta_1$, and plot the fitting result in Fig. 4(b) as the black line. To demonstrate the data and fitting result clearly, we plot $Q$ against the normalized PR defined by $P_{SM} + \tan\delta_1 / \tan\delta_{SM} P_3$ [36]. The analysis with the updated model gives a $\tan\delta_{SM} \simeq 8.9 \times 10^{-4}$ and a $\tan\delta_1 \simeq 3.5 \times 10^{-3}$.

After considering the contribution from the junction region, the data in Fig. 4(b) show more consistent behavior with the prediction from the dielectric loss model. This result suggests that: the quality of fabrication is reproducible among multiple samples, and the impact from the temporal fluctuation on $T_1$ is suppressed by the repetition of measurements; moreover, our simulation of the PR values of transmon qubits with varied geometries and the assumption of the dielectric losses in the interface regions, are self-consistent. With these well-controlled experiments, we are able to achieve more direct characterizations on the individual intrinsic dielectric losses of the TiN film for the shunting capacitors and the Al film for the Josephson junctions on the sapphire substrate.

Regarding the fitting result of $\tan\delta_{SM} \simeq 8.9 \times 10^{-4}$, we would like to point out that, this value sets an upper limit for the dielectric loss at the SM interface. Our simulation reveals that, $P_{SA}$ and $P_{MA}$ are approximately proportional to $P_{SM}$ especially in the case of interdigital shunting capacitors, consistent with previous studies [6, 20]. Therefore, the potential dielectric losses of the SA and MA interfaces would be attributed to $\tan\delta_{SM}$ in the fitting, leading to a result larger than its real value. The extracted value of $\tan\delta_{SM}$, although overestimated, indicates that the quality of the SM interface of the TiN film is comparable to those of the best reported material systems with low dielectric losses [4, 8–11].
Although obtained from the data points distributing in a relatively narrow range of $P_J$, the dielectric loss of the junction region, a $\tan \delta_J \approx 3.5 \times 10^{-3}$, is consistent with previous studies on Al devices fabricated with a lift-off process [6, 37]. We note that for long-lifetime devices that have a small $P_{SM}$, approximately 80% of the relaxation can be attributed to the disordered layers at the interfaces of the Al electrodes forming the junction, which leaves considerable space for further improvement of the $Q$ of transmon qubits.

In conclusion, we implement a material system of TiN film deposited on sapphire substrate with low dielectric loss at the SM interface. Through the measurements of a series of transmon qubits with varied shunting capacitor designs and measurement configurations, we systematically characterize the $Q$ values of qubits versus $P_{SM}$, and estimate the loss tangent at the SM interface. The experimental data show that, $\tan \delta_{SM}$ is less than $8.9 \times 10^{-4}$ in a 1-nm-thick disordered layer, accompanied by a dissipation induced by the junction region with a $\tan \delta_J \approx 3.5 \times 10^{-3}$. On the basis of the low dielectric loss of the material, we achieve transmon qubits with $T_1$ values of up to the 300 $\mu$s level and $Q$ values of approximately 8 million with reproducibility. Our work indicates that, the TiN film deposited by magneto sputtering on sapphire substrate is an ideal material system for superconducting quantum computing, which provides a low-loss platform for the implementation of high-coherence qubits and in-depth studies on other dissipation mechanisms in superconducting circuits. Our analyses further suggest that the interface dielectric loss around the Josephson junction part of the circuit could be the dominant limitation of lifetimes for state-of-the-art transmon qubits.

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**APPENDIX**

**Fabrication**

The 100-nm-thick TiN films were deposited by using a high-throughput sputter system equipped with a 4-inch radio-frequency (RF) sputter gun (CS-200, ULVAC Inc.) using a 99.999% purity titanium target. The deposition
power was set at 600 W and the Ar-N\textsubscript{2} (ratio 4:1) gas mixture used for the reactive sputtering was held at a pressure of 0.5 Pa. The substrates used for this study were 2-inch, single-side polished, c-plan sapphire (Suzhou RDMicro Co. Ltd.).

The 100-nm-thick Si\textsubscript{N}x hard mask layers were deposited via a plasma-enhanced chemical vapor deposition (PECVD) system (Haasrode C200A, LEUVEN Instruments Inc.). The deposition was performed at 200°C in a gas mixture of N\textsubscript{2}, SiH\textsubscript{4}, and NH\textsubscript{3}. The deposition pressure was maintained at 500 mTorr, and the RF power was set at 100 W.

The lithography was implemented by a DWL 2000 direct-write-laser lithography system (Heidelberg Instrument GmbH). S1813 photoresists (Advanced Materials Inc.) were first spin-coated and soft-baked at 115°C for 60 s. After exposure, the coated wafers were developed in an MIF319 developer (Kayaku Advanced Materials Inc.) for 60 s, and cleaned in the running DI water for 120 s.

The lithography pattern was subsequently transferred to the Si\textsubscript{N}x hard mask layers using an inductively coupled plasma (ICP) system (PlasmaPro100, Oxford Instruments). The dry-etch process was performed at 20°C in a gas mixture of SF\textsubscript{6} and CHF\textsubscript{3}. The ICP power was set at 800 W and the bias power was set at 20 W.

The wet etch of the TiN films was performed in SC-1 solution [i.e., a mixture of deionized (DI) water, ammonium hydroxide (29% NH\textsubscript{3} by weight), and hydrogen peroxide (30%) at a volumetric ratio of 6:1:1]. The process was performed at 60°C with added stirring. After the completion of the wet-etch process, the wafers were cleaned in DI water heated to 60°C, followed by cleaning with running DI water for 2 min. The Si\textsubscript{N}x hard mask layers were then stripped off in diluted hydrofluoric solution (5%).

The fabrication of the Al/AlO\textsubscript{2}/Al Josephson junctions was performed using a conventional “Manhattan” technique. First, the lithography of the mask structures was implemented by a high-resolution e-beam lithography system (JBX 8100FS, JOEL Inc.). The e-beam resist stack was composed of 950-nm PMMA (MicroChem Inc.) on 200-nm MMA (Advanced Materials Inc.). The exposure current was 2 nA and the beam dosages were 1750 and 1550 uC/cm\textsuperscript{2} at the junction-area and the connection pad regions, respectively. The deposition of the junctions was performed using an e-beam evaporator (MEB-600, CSWN). Before the deposition, a gentle ion mill was applied for 30 s to remove the residual resists in the mask openings. The first 40-nm-thick Al layer was deposited at 6 Å/s. After 10 min of cooling, O\textsubscript{2} was injected and maintained at 160 Pa for 6 min to form the AlO\textsubscript{2} insulating barrier. The second 80-nm-thick Al layer was then deposited at a rate of 6.8 Å/s rate after a rotation of the sample stage in an orthogonal direction. After junction fabrication, lift-off was implemented by 2 h of soaking in acetone, and another 2 rounds of acetone cleaning and one isopropanol cleaning in a sonication bath.

**Interfaces at the Al/AlO\textsubscript{2}/Al Junction Region**

Similar to the characterizations on the interfaces of the TiN film on the sapphire substrate in the shunting capacitor region, we perform TEM imaging on the cross section of the Al film in the junction region, and demonstrate the result in Fig. 5. The images of the interfaces show that, on average, there are approximately 1-nm- and 5.5-nm-thick disordered layers at the SM and MA interfaces, respectively, which are adopted in the $P_1$ simulation. The dielectric constant applied in the simulation is kept the same as the one assumed at the SM interface of the shunting capacitor.

**Measurement**

We use the standard heterodyne measurement setups shown in Fig. 6 to characterize the $T_1$ values of our qubits.

We apply a HDAWG (Zurich Instruments Ltd.) and a UHFQA (Zurich Instruments Ltd.) to generate qubit driving (XY) and readout signals, respectively, at approximately 100 MHz intermediate frequencies. Then, these signals are modulated with carrier waves generated by a microwave source, a SLFS 0211D signal generator (Sinolink Inc.), through SIQM 0408 mixers (Sinolink Inc.). On the signal input channels inside the dilution refrigerator, cryogenic attenuators (XMA Inc.), F-30-8000-R low-pass filters (RLC Inc.) and in-house developed infrared (IR) filters are applied at different temperature stages, to achieve thermal anchoring and noise suppression.
On the signal output channel, F-30-8000-R low-pass filters (RLC Inc.) and LNF-ISISC4_8A 2-stage isolators (Low Noise Factory Inc.) are applied to reduce the possible noise and back reactions from the upper stages at higher temperatures. The output signal is amplified by LNC4_8C high-mobility electron transistor (HEMT) amplifiers (Low Noise Factory Inc.) at 4 K, followed by additional amplification at 300 K with LNR4_8C RF amplifiers (Low Noise Factory Inc.). After the demodulation by a mixer with the identical carrier wave divided from the one used in readout signal generation, the output signal is sampled by the analog-digital converter (ADC) of UHFQA (Zurich Instruments Ltd.).

To approach an ideal electromagnetic environment for our measurements, we apply multiple-stage shields to isolate the samples from possible noise sources. Copper (Cu), aluminum, and μ-metal shields are applied from the inside out. The channel feedthroughs on the shields are light-tight to eliminate the influence of spray radiation from high-temperature parts of the dilution refrigerator. Moreover, we optimize the package of 2D transmon qubit samples by hollowing the bottom stage under the die, which has been indicated to be helpful in suppressing the coupling between the package and the qubits [38, 39].

Regarding the measurements of the dumbbell 3D transmon qubits, we load our samples in rectangular Al cavities. The setups are almost identical to those shown in Fig. 6, except that the XY and readout channels are merged by a power splitter at 300 K, and share one signal input channel inside the dilution refrigerator.

**Qubit Parameters and Data Processing**

In Table I, we list the relevant parameters and experimental data of the transmon qubits reported in this work.

Following Ref. [5], the Purcell limit induced by the readout cavity on the transmon qubit ($T_{\text{Purcell}}^{-1}$) is estimated by $T_{\text{Purcell}}^{-1} \approx (g/\Delta)^2 \kappa$, where $g$ and $\Delta$ are the coupling strength and frequency difference between the qubit and readout cavity, respectively, and $\kappa$ is the line width of the readout-cavity spectrum. $g$ is deduced from the dispersive shift of the readout cavity $\chi \simeq g^2/\Delta$ in the dispersive regime. We directly measure $\Delta$, $\kappa$, and $\chi$ in the experiments. After estimating $T_{\text{Purcell}}$, we first subtract the contribution of the Purcell limit from each measured $T_1$, then covert the result to $Q$, and finally apply statistics to obtain the average value and standard deviation shown in Fig. 4 and Table I.

The experimental data demonstrated in Fig. 3 come from device DT-1 in Table I. Regarding the two data points of the dumbbell 3D transmon qubits in Fig. 4 and Fig. 7, the average $Q$ and standard deviation come from the statistics of the single-round measurement results of multiple devices fabricated in an identical batch, listed as series D8 and D9 in Table I.

In Fig. 7, we show the original fitting result of the
TABLE I. Relevant parameters and experimental data of transmon qubits showed in Fig. 4. \(\omega_q\), \(\omega_c\), and \(g\) are the qubit frequency, readout cavity frequency, and the coupling strength between qubit and readout cavity. \(T_{\text{Purcell}}\) is the Purcell limit of qubit induced by the readout cavity. The standard deviations of \(T_1\) and \(Q\) are listed in parentheses. The experimental data of the dumbbell 3D transmon qubits (D8 and D9 series) are stable values from single-round measurements.

model including the contributions from both \(\tan \delta_{\text{SM}}\) and \(\tan \delta_J\). The relative fitting errors are approximately 8% and 5%, respectively. The expected \(Q\) from the model with the fitted loss tangent values is plotted as the semi-transparent blue surface in the figure.

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