Thermocompression Bonding Technology for Multilayer Superconducting Quantum Circuits

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Extensible quantum computing architectures require a large array of quantum devices operating with low error rates. A quantum processor based on superconducting quantum bits can be scaled up by stacking microchips that each perform different computational functions. In this article, we experimentally demonstrate a thermocompression bonding technology that utilizes indium films as a welding agent to attach pairs of lithographically-patterned chips. We perform chip-to-chip indium bonding in vacuum at 190 °C with indium film thicknesses of 150 nm. We characterize the dc and microwave performance of bonded devices at room and cryogenic temperatures. At 10 mK, we find a dc bond resistance of 515 nΩ mm$^{-1}$. Additionally, we show minimal microwave reflections and good transmission up to 6.8 GHz in a tunnel-capped, bonded device as compared to a similar uncapped device. As a proof of concept, we fabricate and measure a set of tunnel-capped superconducting resonators, demonstrating that our bonding technology can be used in quantum computing applications.

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The field of quantum computing1 is experiencing major growth thanks to the development of architectures with ten or more quantum bits (qubits).6 The biggest challenge in the realization of a universal quantum computer is the implementation of extensible architectures where qubit operations can be performed with low error rates. Among many promising qubit architectures,7 those based on superconducting quantum circuits8 are rapidly reaching a level of maturity sufficient to demonstrate supremacy of a digital quantum computer over the state-of-the-art classical supercomputer.9 Elements of quantum-error correcting codes10 have already been demonstrated in a variety of experiments using superconducting qubits,11,12 and a quantum memory has been realized with quantum states of microwave fields.13

In order to build an extensible quantum computer, however, many technological advances must first be demonstrated. Among these, three-dimensional integration and packaging of superconducting quantum circuits is emerging as a critical area of study for the realization of larger and denser qubit architectures. This approach allows the departure from the two-dimensional confinement of a single microchip to a richer configuration where multiple chips are overlaid. Three-dimensional integration, thus, provides a flexible platform for more advanced classical manipulation of qubits and qubit protection from the environment. In this framework, an architecture based on multilayer microwave integrated quantum circuits has been proposed16 and some of its basic elements realized, showing that high-quality micromachined cavities17 can be used to implement three-dimensional superconducting qubits.18 Leveraging the extensive body of work developed in the context of classical integrated circuits, flip chip technology has been adopted to bond pairs of microchips containing superconducting circuits.19–21 Microfabricated air bridges have been utilized to reduce on-chip electromagnetic interference22. High-frequency through-silicon vias23 and a quantum socket based on three-dimensional wires24 have been developed to attain dense connectivity on a two-dimensional array of qubits.

In this article, we demonstrate the experimental implementation of a two-layer integrated superconducting circuit where two microchips are attached by means of thermocompression bonding in vacuum. The structures on the surface of the bottom chip (or base chip) and on the underside of the top chip (or cap) are fabricated using standard photolithography techniques. Instead of a discrete set of indium bump bonds, a continuous thin film of molten indium serves as bonding medium between the chips. We perform a detailed electrical characterization of a variety of bonded devices from room temperature to 10 mK at both dc and microwave frequencies, showing that the bonding technology can be used in quantum computing applications.

Figure 1(a) illustrates the geometric characteristics of a capped device. The base chip consists of an intrinsic silicon substrate of thickness 500 μm coated by an alu-

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The CPW transmission line features a center conductor of aluminum and indium films. The bonding procedure is realized in a custom-made vacuum chamber with the aid of an aligning and compressing fixture (see details in the supplementary material). The base chip and cap are aligned with a horizontal accuracy of less than 10 µm, significantly smaller than the device’s maximum allowed tolerances. The chips are subsequently compressed by applying vertical pressure with the fixture lid. At a system pressure of approximately 10⁻² mbar, the chamber is placed for 100 min on a hot plate at 190 °C, above the indium melting temperature (∼157 °C). Heating in vacuum prevents the formation of thick indium oxide and results in a strong mechanical bond without chemical or physical cleaning of the indium films prior to bonding. In fact, we found that bonded samples can withstand several minutes of high-power sonication and multiple cooling cycles to 77 K and 10 mK. Images of a bonded device are shown in Figs. 1(b), 1(c), and 1(d).

The dc electrical behavior of a bonded device is characterized using the base chip and cap layouts shown in the inset of Fig. 2(a). By applying a dc current through ports 1 and 4 and measuring the voltage across ports 2 and 3, we find a room temperature dc resistance $R \simeq 2.785 \Omega$. This resistance is due to the room temperature resistance of the aluminum-indium films on both the base chip and cap as well as the bond resistance between the two chips. We realize detailed numerical simulations of the device under test (DUT) by means of ANSYS Q3D Extractor and find a theoretical $R \simeq 1.323 \Omega$. The discrepancy between the measured and simulated resistance is likely due to the bond resistance (not included in the Q3D model), bond inhomogeneity, or both; possible contributors to these effects are the presence of native indium oxide before bonding, inter-diffusion of aluminum and indium, or a tilt between base chip and cap.

Bond inhomogeneity can be understood by modeling the five metallic layers of a bonded device – aluminum, indium, bond region, indium, and aluminum – as a large set of flux tubes directed from the base chip to the cap. At room temperature, each tube has a resistance $R_{\text{tube}}$; the total resistance $R$ is approximately the parallel resistance of all flux tubes. Flux tubes in an unbonded region are open circuits with resistance $R_{\text{tube}} \sim \infty$ and cause $R$ to increase. Following this model, the ratio between measured and simulated resistance indicates that approximately 50 % of the DUT is bonded. This result is verified by breaking apart bonded devices and inspecting optically the surfaces of the bond region (see supplementary material).

Figure 2(a) shows a four-point measurement of $R$ as a function of temperature $T$ for the bonded device shown in the inset. Below the superconducting transition temperature of aluminum, $T \simeq 1.2 K$, $R$ is approximately the bond resistance. The data points in the figure are obtained by measuring the device’s current-voltage (I-V) characteristic curves at various temperatures and fitting their slope. Figure 2(b) shows the I-V curve measured at $T \simeq 10 mK$. We find a critical current intensity for the aluminum-indium films, $I_c \simeq 7 mA$. An ensemble of measurements well below $I_c$ is reported in the inset of Fig. 2(b). From the least-squares best fit, we obtain a
Figure 2. Bond characterization at dc. (a) Resistance $R$ as a function of temperature $T$ for the capped device depicted in the inset. Inset: Base chip with two aluminum-indium islands separated by a dielectric gap. The fully metallized cap includes a tunnel which, when the chips are bonded, spans the gap on the base chip. (b) I-V characteristic curve at $T \approx 10 \text{ mK}$ for the capped device in (a). Inset: Data and fit [magenta (middle gray)] below $I_c$.

The bond resistance $R \approx 50 \pm 2 \mu \Omega$, which is less than approximately 515 nΩ mm$^{-2}$ assuming a 50% bond area. This resistance is likely due to the native indium oxide film initially present on the chips, preventing the bond region from becoming superconductive at low temperatures.

Figure 3 displays the microwave characterization of three capped and uncapped devices with layouts shown in the insets. The measurements are realized by means of a vector network analyzer (VNA) from Keysight Technologies Inc., model PNA-X N5242A; details on the measurement setups can be found in Béjanin et al.$^4$

The measurements in Fig. 3 (a) demonstrate that the bonding process and the addition of the cap – including the tunnel mouth – do not noticeably increase reflections, which are instead dominated by the three-dimensional wires.$^4$

Figure 3 (b) shows a measurement of the isolation coefficient between two adjacent transmission lines (see inset). At microwave frequencies a signal injected at port 1 or 2 can leak to ports 3 and 4, generating signal crosstalk. Due to the three-dimensional wires, signal crosstalk for the uncapped device is already very low.$^4$ The cap further reduces crosstalk by more than 10 dB across the entire measurement bandwidth. These results may have important implications to quantum computing, where crosstalk has been identified as a major source of error.$^{29}$

Reflection and isolation measurements are performed at room temperature in order to maintain the DUT reference planes as close as possible to the VNA ports. However, the line shown in the inset of Fig. 3 (c) is characterized by a room-temperature loss sufficiently large to mask any abnormalities in transmission measurements at microwave frequencies. We therefore measure this line at $\sim 10 \text{ mK}$, where both the indium and aluminum films are in the superconducting state.

Figure 3 (c) shows clean transmission for both uncapped and capped devices up to $f \approx 6.8 \text{ GHz}$. At higher frequencies, we observe a series of pronounced resonances in the transmission coefficient of the capped device. The simulations in Fig. S3 of the supplementary material and the results in Fig. 3 (a) indicate that these resonances are not due to the presence of the tunnel. We believe they are caused by bond inhomogeneity, shown in Fig. S2 of the supplementary material, resulting in unwanted resonances similar to the slotline modes observed by Wenner et al.$^{30}$

As a proof of concept for quantum computing applications, we fabricate and measure a set of capped superconducting CPW resonators. The device layout is sketched in the inset of Fig. 3 (b), which shows nine $\lambda/4$-wave resonators coupled to line 1−2 in a multiplexed design.$^4$

The resonators are characterized by measuring their internal quality factor at $\sim 10 \text{ mK}$ and for a mean photon occupation number $\langle n_{ph} \rangle \approx 1$, similar to the excitation power used in quantum computing operations. The main resonator parameters are reported in Table I.$^{31}$ The measured data and fits for the second pair of resonators in Table I are shown in Fig. S4 of the supplementary material. Note that the resonance frequency of an uncapped resonator shifts with the addition of the cap.

In the supplementary material, we determine that the internal quality factor of a capped resonator is approx-
FIG. 3. Characterization at microwave frequencies of the uncapped and capped CPW transmission lines shown in insets; black lines refer to structures on the base chip and light green (light gray) shades indicate metallized tunnels and through holes in the cap. Data for uncapped devices is plotted in light green (light gray) and for capped devices in dark blue (dark gray). (a) Magnitude of the room temperature reflection coefficient at port 1, $|S_{11}|$, as a function of frequency $f$. (b) Magnitude of the room temperature isolation coefficient between ports 1 and 4, $|S_{14}|$, vs. $f$. (c) Magnitude of the transmission coefficient $|S_{21}|$ measured at 10 mK.

approximately 1% larger than that of an uncapped resonator due to the vacuum participation. However, this effect is significantly smaller than the quality factor fluctuations over time and, thus, it cannot be resolved in our measurements. In fact, accounting for time fluctuations, the quality factors for capped and uncapped resonators in Table I are approximately equal.

In conclusion, we have developed and characterized a hot thermocompression bonding technology in vacuum using indium thin films as bonding agent. Our results show that this technology can be readily used to implement an integrated multilayer architecture, combining the fabrication advantages of two-dimensional superconducting qubits and the long coherence of micromachined three-dimensional cavities. This bonding technology is compatible with the quantum socket design, paving the way toward the implementation of extensible quantum computing architectures as proposed by Béjanin et al.

In future implementations, we will improve the bonding procedure by including a cleaning step with an acid buff to remove native indium oxide prior to bonding. Additionally, we will use slightly thicker indium films ($\sim 1 \mu m$), a lower bonding pressure ($\sim 10^{-6}$ mbar), in vacuo chip alignment and compression, as well as a higher and more homogeneous compression by means of an hydraulic press. Finally, we will add an inter-diffusion barrier between the aluminum and indium films.

See supplementary materials for details on the thermocompression bonding setup, bond inhomogeneity, transmission simulations, resonator data and fits, and vacuum participation.

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Table I. Resonance frequencies and internal quality factors $f_{0}^{uc}$, $Q_{1}^{uc}$, $f_{0}^{c}$, and $Q_{i}^{c}$, respectively, for a set of four uncapped and capped resonators.

| $f_{0}^{uc}$ (GHz) | $Q_{1}^{uc}$ | $f_{0}^{c}$ (GHz) | $Q_{i}^{c}$ |
|------------------|-----------|----------------|----------|
| 4.252            | 37700     | 4.033          | 20230    |
| 4.448            | 52100     | 4.982          | 22510    |
| 4.722            | 41830     | ...            | ...      |
| 4.913            | 44840     | ...            | ...      |

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Supplementary Materials for “Thermocompression Bonding Technology for Multilayer Superconducting Quantum Circuits”

In this supplementary materials, we provide further details on the thermocompression bonding setup. We characterize bond inhomogeneity with optical imaging. We present numerical simulations of the transmission coefficient at microwave frequencies for various configurations of capped and uncapped coplanar waveguide (CPW) transmission lines. We show the measured data and fits for a capped and uncapped superconducting resonator at 10 mK. Finally, we calculate the ratio of the internal quality factor for a capped and uncapped resonator, thus estimating the effect of vacuum participation.

S1: THERMOCOMPRESSION BONDING SETUP AND PROCEDURE

Figure S1 shows a computer-aided design of the custom-made vacuum chamber and aligning-compressing fixture used for the thermocompression bonding. The bottom of the chamber is made from a 10 mm thick copper plate, ensuring a high thermal conductivity and heat capacity. The bottom surface of the plate is mirror polished each time before placing the chamber on the hot plate. The top surface features a set of threaded screw holes, where aligning-compressing fixtures with different dimensions can be fixed; the chamber is designed to process up to 3-in. wafers. The chamber’s wall is a 30 cm high, 3 mm thick hollow cylinder made from stainless steel, the low thermal conductivity of which ensures little or no heating of the top part of the chamber. The top edge of the cylindrical wall is welded to a 6-in. ConFlat (CF) flange made from 304L stainless steel.

The CF flange features a knife-edge seal mechanism; the sealing element is a fully annealed copper gasket. The gasket is made from 1/4 hard, high purity, oxygen-free (OFHC) copper, which allows for system pressures as low as 10^{-12} mbar at operating temperatures up to 450°C. A ultra-high vacuum, temperature-resistant valve is used to connect the CF flange to a pump. A CF flanged Kodial glass viewport (sealed with a silver plated copper gasket) permits the observation of the chamber’s interior during processing.

The aligning-compressing fixture is a square washer with inner dimensions 16.5 mm × 16.5 mm made from stainless steel and featuring an adjustable edge corner. This corner can be moved along a groove at the bottom of the washer, allowing alignment between the base chip and cap. In this work, we use square chips with dimensions 15 mm × 15 mm. Note that the base chip is in direct contact with the copper plate, guaranteeing good thermalization. The aligning procedure comprises three steps: First, the base chip is placed inside the washer at the bottom of the chamber and pushed against the washer’s corner opposite to the adjustable corner; second, the cap is manually dropped on the base chip, pre-aligning the chips as accurately as possible; third, the two chips are aligned with the adjustable corner, which is finally fixed to the chamber with a screw. The manual pre-alignment in step two is sufficient to prevent damage of the on-chip structures due to relative dragging of the chips during step three. The lid shown in Fig. S1 (b) is used to apply pressure on the aligned chips by means of four screws. We find that little pressure is required to obtain a mechanically strong bond.

After closing the chamber, we evacuate it with a molecular pump from Pfeiffer Vacuum GmbH for 30 min to reach a system pressure of 1.5 × 10^{-2} mbar. While pumping we monitor the chamber leak rate, which is typically on the order of 10^{-10} mbar Ls^{-1}. Once the chamber is placed on the hot plate, the temperature initially fluctuates reaching a steady state in approximately 10 min; at that time we start counting 100 min. Pumping is continued during the entire heating process, as well as during a cooling period when the chamber is placed to rest on a thick aluminum plate.

Our bonding procedure is simple and highly reproducible, with a yield of 80% for a total of 15 bonded samples.

When performing thermocompression bonding of devices with superconducting qubits, the Josephson tunnel junctions that make the qubits will be heated at high temperature. In order to verify whether this process damages the Josephson junctions, we fabricate a set of aluminum-aluminum oxide-aluminum junctions using e-beam lithography and evaporation. The junctions’ area is 350 nm × 350 nm and their room temperature resistance ∼5 kΩ. We perform a preliminary test by heating the junctions to 190°C for 5 min at atmospheric pressure, finding that most of the junctions survive the process. In addition, we find that the post-heat room temperature resistance decreases to approximately 4 kΩ. A complete study of heating effects on submicron sized Josephson junctions was performed by Koppinen et al[2].

S2: BOND INHOMOGENEITY

Bond inhomogeneity can be characterized by breaking apart a bonded device and imaging the base chip and cap bond surfaces optically, as shown in Fig. S2. The images refer to the device outlined in the inset of Fig. 3 (c) in the main text and are taken by means of a handheld digital microscope.

The indium film within the boundary of the through holes on the base chip [see Fig. S2 (a)] is heated during
FIG. 4. Thermocompression bonding setup. (a) Vacuum chamber. (b) Aligning-compressing fixture comprising a square washer, an adjustable edge corner, and a lid. The channels used to evacuate the interior of the washer when tightened to the chamber’s bottom are visible.

the bonding process, but not bonded to the cap. We can thus use the color of the indium film in this region as a reference to discern bonded from not bonded regions. We determine that the region near the center of the base chip and cap was bonded well, whereas the area around the edges of the two chips was not bonded. In this case, approximately 50% of the chips’ area was bonded well. We find similar results in other devices. This effect is likely due to the compressing fixture lid that was designed to be smaller than the chips’ area, thus applying pressure only to the center of the chips. In the conclusions of the main text we propose a remedy to this issue.

S3: TUNNEL MOUTH MICROWAVE SIMULATIONS

The edge of a through hole where the cap tunnel begins (the tunnel mouth) represents a boundary condition for the electromagnetic field associated with a capped transmission line. The line shown in the inset of Fig. 3 (c) in the main text is characterized by two of such boundary conditions. In order to determine whether these conditions generate unwanted resonance modes, we simulate the transmission coefficient $S_{21}$ for this line and compare it to that of an uncapped line and of a capped line without tunnel mouths (i.e., covered by an infinitely long tunnel). The numerical simulations are performed with ANSYS HFSS,$^7$ assuming perfect conductors and lossless CPW transmission lines with equal geometric characteristics.

The graphs displayed in Fig. S3 reveal almost perfect transmission for the three simulated configurations, with less than 0.1 dB of loss due to slight impedance mismatch. We can safely conclude that the unwanted resonances shown in Fig. 3 (c) of the main text are not due to the presence of the tunnel mouths.

S4: CAPPED SUPERCONDUCTING CPW RESONATORS

Figure S4 shows data and fits for the second pair of uncapped and capped superconducting resonators reported in Table 1 of the main text. The displayed data for the capped resonator is the ensemble average of 2 measured traces, whereas only one trace is measured for the uncapped resonator. In both cases, each data point is obtained setting the vector network analyzer (VNA) to an intermediate frequency bandwidth $\Delta f_{IF} = 1$ Hz.

S5: VACUUM CONTRIBUTION TO CAPPED RESONATORS QUALITY FACTOR

In this section, we estimate the effect of a metallized cap on the internal quality factor $Q_i$ of a superconducting CPW transmission line resonator. The addition of a grounded cap above a CPW resonator forces some of the electric field lines to be distributed from the base chip
to the cap, away from the base chip substrate. This increases the contribution of vacuum to the mode volume of a capped resonator compared to the case of an uncapped resonator. Assuming all metallic structures to be perfect conductors, the internal quality factor is solely due to dielectric losses and, thus, it can be found by inverting the loss tangent as:

\[
Q_i = \frac{\varepsilon_e'}{\varepsilon_e''},
\]

where \(\varepsilon_e = \varepsilon_e' - j\varepsilon_e''\) is the effective electric complex permittivity of the CPW transmission line with real and imaginary parts \(\varepsilon_e'\) and \(\varepsilon_e''\), respectively (\(j^2 = -1\)).

The effective electric permittivity of a capped CPW transmission line can be calculated using Eq. (2.39) in Simons:

\[
\varepsilon_c = 1 + q_3 (\varepsilon_{1r} - 1),
\]

where \(q_3\) is the partial filling factor dependent on the device geometry [see Eq. (2.40) in Simons and \(\varepsilon_{1r} = \varepsilon_{1r}' - j\varepsilon_{1r}''\) is the relative electric complex permittivity of the base chip substrate (in our case silicon) with thickness \(h_1\). Hereafter, we assume \(h_1 \to \infty\) (a reasonable approximation as the silicon substrates are 500 µm thick, much thicker than any of the other structures; see main text for all relevant dimensions). Note that Eq. (2) is applicable as the tunnel sidewalls are much farther away from the conductor than the in-plane ground planes, \(T \gg H\) (see Fig. 1 in the main text).

Inserting Eq. (2) into Eq. (1), we obtain the capped internal quality factor

\[
Q_i^c = \frac{1 + q_3 (\varepsilon_{1r}' - 1)}{q_3 \varepsilon_{1r}''}. \tag{3}
\]

In the case of an uncapped CPW transmission line, the effective electric permittivity is given by:

\[
\varepsilon_{uc}^e = \frac{1 + \varepsilon_{1r}}{2}. \tag{4}
\]
FIG. 7. Uncapped (left panels) and capped (right panels) resonator measurements (dots) at low power [i.e., \(\langle n_{\text{ph}} \rangle \simeq 1\) (cf. main text)]. The resonator transmission magnitude \(|S_{21}|\) (above) and phase angle \(\angle S_{21}\) (below) are fitted as in Béjanin et al.\textsuperscript{[S4]} (light gray).

and the internal quality factor is given by

\[
Q_i^{\text{uc}} = \frac{1 + \varepsilon'_r}{\varepsilon'_r}. \tag{5}
\]

The ratio between the uncapped and capped internal quality factors is thus

\[
\frac{Q_i^{\text{uc}}}{Q_i^{\text{c}}} = \frac{(1 + \varepsilon'_r) q_3}{(\varepsilon'_r - 1) q_3 + 1}. \tag{6}
\]

Using the dimensions \(S, W,\) and \(h_4 = H\) reported in the main text and assuming \(\varepsilon'_r = 11\) for silicon, we find \(q_3 \simeq 0.4722\) and, thus, \(Q_i^{\text{uc}}/Q_i^{\text{c}} \simeq 0.99\). As a consequence, the increase in vacuum participation due to the addition of the cap increases the internal quality factor by approximately 1%. This is a very small effect for the devices presented in this work, where other loss mechanisms such as the presence of native indium oxide on both the base chip and cap, the low quality thin-film sputter deposition, and possibly the bonding procedure itself outweigh the benefits of a higher vacuum participation. However, a careful design and a suitable fabrication and cleaning process may be used to take advantage of this effect to make capped devices (e.g., qubits) with lower error rates than similar uncapped devices.

\[S1\]A new chamber is being designed made from 316LN stainless
steel with low magnetic permeability $\mu \leq 1.005$, reducing magnetic contamination of the samples.

[S2] P. J. Koppinen, L. M. Väistö, and I. J. Maasilta, “Effects of annealing to tunnel junction stability,” AIP Conference Proceedings 850, 1639–1640 (2006).

[S3] http://www.ansys.com/products/electronics/ansys-hfss

[S4] J. Béjanin, T. McConkey, J. Rinehart, C. Earnest, C. McRae, D. Shiri, J. Bateman, Y. Rohanizadeh, B. Penava, P. Breul, S. Royak, M. Zapatka, A. Fowler, and M. Mariantoni, “Three-dimensional wiring for extensible quantum computing: The quantum socket,” Physical Review Applied 6 (2016), 10.1103/PhysRevApplied.6.044010.

[S5] R. N. Simons, Coplanar Waveguide Circuits, Components, and Systems (John Wiley & Sons, Inc., Hoboken, NJ, USA, 2001).