PEV BASED FILTER BANK FOR DIGITAL HEARING AID APPLICATION: PEVFB

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Abstract

Designing an electronic circuit with low power and small area are two important concerns for signal processing designers. Though fast emergence of the new technologies and several reviews over signal and speech processing, the difficulty cannot be fulfilled for the hearing impaired people. Many filter bank algorithms have been discussed on the hearing aid design to extend the efficiency. The conventional design of cascaded Direct Truncation (DT) data path is mainly based on the design of Full Precision Static Floating Point. In this paper, we introduce Static Floating Point Sample Rate Converter (SFP-SRC) with Linear Phase Finite Impulse Response (LPFIR) for hearing aid applications. The Sampling Rate Conversion is done before or after the LPFIR filter with upsampling and downsampling factors. In order to increase efficiency of DSP systems, filter bank algorithms need more than one sampling rate. The proposed method provides minimum delay and excellent Signal to Noise Ratio (SNR) performance when compared to Post Truncation (PT) data path. In order to obtain better performance, many experiments have been conducted. The proposed SFP-SRC is suitable for hearing assistance applications. Hence, it is implemented on 1/3 octave analysis filter bank with umc-90nm CMOS technology at 24 KHz.

Keywords : Finite Impulse Response, Filter bank algorithms, Digital hearing aid, DSP algorithms

I. Introduction

In recent years, novel techniques of Digital Signal Processing (DSP) algorithms like Noise reduction, Auditory Compensation, Sub-band calculation, Echo Cancellation, and Speech Enhancement are applied repetitively [XVI]. DSP
algorithms are used for implementing hearing aid devices to enhance speech precision in availability of noise [XXI]. Auditory compensation provides the solutions to the person who are severely affected from the hearing illness. Figure.1 describes the block diagram of a typical hearing aid design [XIII].

Hearing aid includes a filter bank which has a several bands and at the output a compressor to balance the loss of audibility. Several low power algorithms are implemented such as Co-efficient Decimation, Frequency Response Masking and ANSI filter. For the hearing impaired people hearing thresholds normally high for high frequency sounds is advanced when compared to the reference speech intensities. Hearing aid does the capability of enhancing the input sounds to equivalent audiogram values. For different frequency levels, sound inputs are adjusted at to achieve the exact sounds. Various algorithms have been discussed about Non-uniform, Uniform, Interpolated FIR, ANSI S1.11 and Quasi 10 ms and Octave ([III], [VII], [XI], [XXVI], [XXVII], [XXIX] and [XVIII]) for digital hearing aids. Each design has its distinct architecture with corresponding merits and demerits. Variable filter banks are discussed in [XXIX], [XXVIII] and [XII]. The Frequency Response Masking (FRM) filter banks are described in [XXV] and [XVIII] for reducing the filter complexity and group delay.

Rapid increase of emerging methods, more multifaceted algorithms may be incorporated in the hearing aid applications to enhance performances of the DSP circuits. Though the implementation of the DSP algorithms, to modify the complexity restricts signal processing algorithms. The fundamental blocks of filter are adder, multiplier, shifter and accumulator. Some of the DSP algorithms such as Fast Fourier Transform (FFT), Direct Cosine Transform (DCT) and the Data path of the DSP are

**Fig 1. Block diagram of a Typical Hearing Aid [XIII]**

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used in many applications. The synthesis of high level and fixed point circuits verification for analyzing the range and precision are discussed in [I], [II], [XIV], [XV], [V] and [XIX]. In the Floating Point Arithmetic (FPA) design, high precision is implemented with a large dynamic range exponents and Mantissa. Hence the floating point arithmetic is helpful for the algorithms which are dealt with unsolvable issues due its high precision.

The parallel and cascaded data path are important in the filter design. The cascaded adder-multiplier-accumulator data path is used in Linear Phase FIR filter. The cascaded data path maintains comparable operations per cycle with limited access of hardware accordingly when compared to the parallel datapath. When compared to Post Truncation (PT) method or Full Precision (FP), Direct Truncation (DT) which is cascaded is expensive and Speedy. In a digital hearing aid must consume low power usage than processor with other applications. The complicated data path has a cycle dual Multiply and Accumulator (MAC) with 24-bit for reasonable accuracy Audio signal processing. The Static Floating Point arithmetic is used to provide optimal SQNR performance.

A High precision LPFIR filter is used in [XX]. It comprises of embedded shifter with one-bit, DT adder, 16-bit DT multiplier, shifter and accumulator. The two interval 1-bit shifters are used for better hardware utilization and parallel structure of the filter data path. This filter is implemented on 18-band quasi ANSI S1.11 1/3 octave analysis filter bank. The Silicon area is diminished to 8.3%. The rest of the paper is organized as follows. Section II discusses the PEV analysis. Section III provides the proposed SFP-SRC filter bank to digital hearing aids. Section IV discusses about the results. Section V concludes the paper.

II. Experimental Study

A compact DSP for multi core systems which is fully programmable is described in [VI]. It performs light weight arithmetic-static floating point Arithmetic. Various software techniques have been extensively discussed to diminish computation complexity in the algorithm and round off noise is encountered in the proposed design. A power efficient computing platform is proposed in [XXII] for hearing aids. It consists of four processing elements. Those elements have RISC processor with various power competent accelerators. Those hardwired accelerators include truncated multiplier and static floating point for improving the SNR and diminish the hardware difficulty. This method reduces the data path, area and improves SNR reasonably than Post truncation method. In FPA, every data manipulation normalizes its value before obtaining the results. DSP designers generally choose the fixed point arithmetic. Though, this method does not suitable for the FIR filter due to its high attenuation parameter constraints. The stop band attenuation of ANSI filter bank (for Example) is 60 dB at least. Therefore the optimal design is a combination of the floating point arithmetic and integer arithmetic [XX].
Fig 2. PEV Analysis (a)Addition and (b) Multiplication

The DSP algorithms are represented by Data Flow Graph (DFG), in VLSI signal processing, nodes includes inputs & outputs, adders, multipliers and the data dependency occurs at in between nodes. In order to achieve high precision word length, the Static floating point arithmetic is suitable [XX].

Peak Estimation Vector (PEV) [VI] : \([M, r]\) of each node is evaluated in the DFG. M denotes the maximum value that cause change in the output and r is a radix point and a non-negative integer shown in Fig 2. (a) and (b).

\[
\begin{align*}
M \times 2^{-r} &= \frac{M}{2} \\
\lfloor M, r \rfloor &= \lfloor \frac{M}{2}, r-1 \rfloor
\end{align*}
\]

The PEV analysis of nodes in DFG is estimated by the following rules [VI]:

a. Addition rule:
‘r’ should be identical before performing the addition or subtraction operation and the equation becomes

\[
\lfloor M1, r \rfloor + \lfloor M2, r \rfloor = \lfloor M1 + M2, r \rfloor; \text{ Add } M1 \text{ and } M2 \text{ by keeping } r \text{ as such.}
\]

b. Multiplication rule:

The equation becomes,

\[
\lfloor M1, r1 \rfloor \times \lfloor M2, r2 \rfloor = \lfloor M1 \times M2, r1 + r2 \rfloor; \text{ Multiply } M1 \text{ and } M2 \text{ by adding } r1 \text{ and } r2.
\]

c. Normalization rule:
M associated with radix point ‘r’ should be sustained as a fractional value among 0.5 to 1. If the M is divided by 0.5 then the r is added with (-1). If the M is multiplied by 0.5 the n r is added with (+1).

In Fig2., the adder has input different M values and different r values. But in the PEV analysis the added output should be the r value. hence it is normalized with 0.5 to 1. The first input ([1,0]) of the adder is normalised i.e M is multiplied by 0.5 and adding -1 with the r. The normalized values becomes [0.5, -1]. The output of the adder is also normalised by 0.5. In the multiplier, there is no need to normalize the input because the multiplier output is the added combination of r1 and r2. Hence, directly we can get the output by multiplying M1 and M2 and simply adding the r1 and r2.

Fig 3. PEV Analysis for FIR Filter

The output of the multiplier is then normalized by 0.5. the final values are: [0.96,0]. Figure. 3 shows the PEV analysis of DFG of LPFIR filter. Assume that all input values are normalized to [1, 0]. Two co-efficient values h1 and h2 are considered as 0.125 and 0.0625 respectively. Initially, the coefficients are normalized as [0.5, 2] and [0.5, 3] by normalized rule. After the computation of addition node by its addition rule, the output values are normalized. Hence, [2, 0] is normalized as [1, -1]; Then using multiplication rule, the multiplication values are evaluated as [0.5, 1] and [0.5, 2]. The multiplication output [0.5, 2] is normalized to [0.25, 1]. Finally, the values [0.5, 1] and [0.25, 1] are added and hence the filter output is calculated by PEV analysis. This proposed method provides more effective bits which are stored instead of zeros in the limited word length. This shows that the coefficient value of SFP has better accuracy than fixed point arithmetic. Fig 3. shows the Direct Truncation data path for 16-bit LPFIR filter. It includes two adders and one multiplier for the data path. After applying the PEV analysis the output becomes same for all the nodes of operation.

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III. Proposed PEB Based Filter Bank

In DSP algorithms, several sub-blocks with individual sample clock rates are necessary for interfacing each block together. Sampling rate converters are utilized in many applications such as digital audio resampling, biomedical applications, CORDIC, Software Defined Radio, etc. If the design needs $m$ operations per cycle, then the reduction of sample rate with respect to the input signal by a factor $X$. 

![Diagram of Proposed PEVFB](image-url)

Fig 5. Block Diagram of Proposed PEVFB
The arithmetic bandwidth is reduced from its \( mf_s \) to \( mf_s / X \) operations per second. However, the sample rate converter is obtained when resampling a signal at a lower rate, in order to permit the signal to pass through a channel with limited bandwidth. Sample rate converter is connected to the LPFIR filter to improve the efficiency and consume less power consumption. This SFP-SRC filter bank is suitable for hearing aid applications. The input and output of the LPFIR filter are connected with sample rate converter. The block diagram for the SFP-SRC is shown in Fig. 4.

In the proposed filter design three shifters such as two one bit shifters for normalization and one N-bit shifter are inserted by the application of PEV analysis into filter design. Along with the two adders and one multiplier, two (2:1) multiplexers are also used for the selection of the accumulator values. Multiplexer selects the input according to input select \( Mux\_sel \). \( S_1, S_2 \) are two operands of the filter. The value of the accumulator is denoted as \( acc \). Coefficient represents filter coefficients which are predefined. The sample rate Converter produces the output value according to the input sample frequency \( f_{input} \) and output sample frequency \( f_{output} \). The ratio is estimated using the formula \( f_{input} / f_{output} \). Then the output value is multiplied by the

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every output of the LPFIR filter design. Then, the next output of the filter is divided by factor X then multiplied by the sample rate converter. Hence, the sample rate is reduced by half and the number of computation is also decreased due to sample rate converter. To noise ratio. The SFP-SRC technique is less complex when compared to traditional techniques. PEV analysis provides more effective bits which are stored instead of zeros in the limited word length. The sample rate is minimized using sample rate converter. The structure is designed in the MATLAB tool and it is implemented in Vertex 5. The results are compared with other filter bank methods. Comparison Table. 2 shows that this proposed method is well suitable for hearing aid applications.

IV. Implementation Results

The results are implemented in the Matlab Simulink Tool and the outputs are verified in the Xilinx ISE 14.1. Table. 1 states that the proposed filter bank provides better results compared to the other filter banks. By observing the results, the area can be reduced 12% in proposed method when compared to direct truncation method. The proposed method achieved 5% of less power than direct truncation. Signal to noise ratio also provides better results by using the proposed method. Table. 2 shows performance comparison with different arithmetic. F1, F2 and F3 are the filters of ANSI filter bank. The SNR performance of the 16 bit Floating point integer data path, only the SNR performance of filters F1,F2 and F3 was best. However, worst performance in the gate count and the energy. The proposed filter bank provides better SNR performance and energy. The simulation and implementation results validate the achievement of the proposed minimum area, delay and high-precision 16-bit direct truncation SFP A–M–S–Accdatapath. Fig 5. shows the performance comparison of various filters with the proposed filter. Fig 6. shows the simulation results of 16-bit linear phase FIR Filter with PEV Analysis.

V. Conclusion

An efficient architecture Static Floating Point Sample Rate Converter (SFP-SRC) with Linear Phase Finite Impulse Response (LPFIR) for audio and speech signal processing is proposed in this paper. The basic idea behind the design of filter bank to reduce the complexity and low power consumption. This paper provides better performance in signal. This technique evaluates many combinations by conducting many experiments which results in better performance. From the results, it shows that 12% reduction in area and 5% power savings compared to the traditional methods. The proposed PEVF is suitable for hearing assistance applications. Hence, it is implemented on 1/3 octave analysis filter bank with umc-90nm CMOS technology at 24 KHz. In this paper, various filter bank techniques are reviewed based on the following aspects: Algorithms used for design, Number of sub-
bands, Various Performance metrics such as area, power, delay and noise, Simulation tools used to implement the filter bank design.

**Table 1. LPFIR Data path**

| ANSI S1.11                  | SNR (dB) | Area (Gate Count) | Power (µW) |
|-----------------------------|----------|-------------------|------------|
| Parallel Integer Arithmetic | 0        | 39267             | 142.234    |
| Direct Truncation, LPFIR    | -1.2     | 34218             | 86.571     |
| Direct Truncation SFP-SRC (Proposed) | -2.6     | 32611             | 82.323     |

**Table 2. Performance Comparison with Different Arithmetic (implemented in Quasi ANSI S1.11 Filter bank)**

| Performance                                   | Delay (ns) | Area (gate count in %) | SNR (dB) | Energy |
|------------------------------------------------|------------|------------------------|----------|--------|
|                                                 |            |                        | F1      | F2      | F3 |
| Floating Point, A-M-Acc with integer arithmetic| 11.7       | 77.1                   | 28.1    | 34.2    | 35.4 |
| Post Truncation, A-M-Acc, with integer arithmetic | 13.9       | 57.4                   | 15.9    | 16.3    | 16.9 |
| Direct Truncation, A-M-Acc, with integer arithmetic | 52.7       | 11.1                   | 13.9    | 18.2    | 19.8 |
| Direct Truncation, A-M-Acc, with SFP arithmetic with SRC | 58.5       | 13.2                   | 12.1    | 15.1    | 17.2 |

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Fig 7. Performance Comparison with Different Arithmetic

Fig 8. Simulation Results of 16-Bit Linear Phase FIR Filter with PEV Analysis

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