3-D Hetero-Integration Technologies for Multifunctional Convergence Systems

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Abstract: Since CMOS device scaling has stalled, three-dimensional (3-D) integration allows extending Moore’s law to ever higher density, higher functionality, higher performance, and more diversified materials and devices to be integrated with lower cost. 3-D integration has many benefits such as increased multi-functionality, increased performance, increased data bandwidth, reduced power, small form factor, reduced packaging volume, because it vertically stacks multiple materials, technologies, and functional components such as processor, memory, sensors, logic, analog, and power ICs into one stacked chip. Anticipated applications start with memory, handheld devices, and high-performance computers and especially extend to multifunctional convergence systems such as cloud networking for internet of things, exascale computing for big data server, electrical vehicle system for future automotive, radioactivity safety system, energy harvesting system and, wireless implantable medical system by flexible heterogeneous integrations involving CMOS, MEMS, sensors and photonic circuits. However, heterogeneous integration of different functional devices has many technical challenges owing to various types of size, thickness, and substrate of different functional devices, because they were fabricated by different technologies. This paper describes new 3-D heterogeneous integration technologies of chip self-assembling stacking and 3-D heterogeneous opto-electronics integration, backside TSV fabrication developed by Tohoku University for multifunctional convergence systems. The paper introduce a high speed sensing, highly parallel processing image sensor system comprising a 3-D stacked image sensor with extremely fast signal sensing and processing speed and a 3-D stacked microprocessor with a self-test and self-repair function for autonomous driving assist fabricated by 3-D heterogeneous integration technologies.

Keywords: 3-D heterogeneous integration, chip self-assembly, electrostatic bonding, TSV

1. Introduction

In high-density and high-performance large-scale integration (LSI), various concerns such as higher off-state and subthreshold leakage, threshold voltage variability, and large signal delay by wiring have become more serious as metal-oxide semiconductor field-effect transistors (MOSFETs) continue on the path to scaling down toward 10 nm or less. High off-state leakage current at zero input voltage and subthreshold leakage current at very low input voltage in MOSFETs results in high static power consumption of LSIs. The total wiring length significantly increases, and hence the signal delay due to wiring increases as the number of transistors in LSI increases by device scaling. To overcome these concerns, three-dimensional (3-D) integration technology has attracted attention, because it vertically stacks multiple CMOS LSI chips such as processor, memory, logic, analogue, and power integrated circuits (ICs) into one stacked chip. It can provide many benefits; increased performance, increased data bandwidth, reduced power, a small form factor, reduced packaging volume, increased yield, and reduced overall costs.1,8)

Moreover, tremendous demands for high-performance, multifunctionality integrated systems require heterogeneous integrations of various functional blocks involving CMOS, MEMS, and photonic circuits owing to its multi-functionality, high-speed communication, and low power consumption.9-16)

3-D heterogeneous integration can create new multifunctional convergence systems beyond electrical products such as mobile & consumer, networking, and computing. One of innovative potential applications is Internet of Things (IoT). IoT is expected to tremendously increase connectedness, allowing for the transfer of a huge amount of data to interconnect all things with trillions sensors (Fig. 1). Then, it requires the convergence of semiconductor,
microelectromechanical systems (MEMS), sensor, wireless, and the Internet technologies for high speed sensing, highly parallel processing, and high performance networking. Low power consumption, small form factor, and multifunctionality are required for embedded devices in IoT. To realize IoT, it is indispensable to introduce a new concept of heterogeneous integration in which various materials, devices, and technologies are integrated on a Si substrate, which different kinds of chips such as compound semiconductor device, photonic device, spintronic device, and sensor device are integrated complementary metal oxide semiconductor (CMOS) Si chips (Fig. 2). We call a heterogeneous 3-D super-chip.\(^{17}\) However, hetero-integration of different functional devices has many technical challenges owing to various types of size, thickness, and substrate of different functional devices, because they were fabricated by different technologies. This paper overviews new 3-D heterogeneous integration technologies of chip self-assembled stacking and 3-D heterogeneous optoelectronics integration, backside TSV fabrication technologies developed by Tohoku University for 3-D super chip. A 3-D stacked image sensor chip with an extremely fast processing speed and a 3-D microprocessor with a self-test and self-repair function for an advanced driving assistant system demonstrated by 3-D heterogeneous integration technology as typical examples of a super-chip.

### 2. Heterogeneous 3-D Integration Technology for Super-chip

#### 2.1. Chip self-assembly and electrostatic (SAE) bonding technologies

A new heterogeneous 3D integration technology to fabricate a super-chip using SAE temporary bonding has been developed, which can provide high production throughput. This technology has been named reconfigured wafer-to-wafer (RW2W) 3D integration technology.\(^{18,19}\) First, more than several hundred known good dies (KGDs) are sorted from several device wafers and then simultaneously bonded in a batch, with a high alignment accuracy of 1 µm, onto a carrier wafer using SAE temporary bonding. High alignment accuracy in SAE bonding is indispensable for forming a high density of electrical connections between the upper and lower chips. This carrier wafer, which consists of many KGDs, is called a reconfigured wafer, and it exhibits very high production yield because of
the KGDs. Next, another reconfigured wafer is fabricated by simultaneously bonding many KGDs onto another carrier wafer. We can produce many reconfigured wafers by repeating this procedure. These reconfigured wafers are stacked onto a target interposer wafer at the wafer level. Several hundred super-chips with different configurations can be simultaneously fabricated on a 12-inch wafer with high production throughput and low cost by using the RW2W integration technology. The surface tension of a liquid is utilized in self-assembly to simultaneously align many dies in parallel. Hydrophilic areas and hydrophobic areas are formed on the surface of a wafer or chip to obtain high alignment accuracy. Hydrophilicity and hydrophobicity are evaluated by measuring the contact angle of a water droplet on the surface. The contact angle of the hydrophilic area is smaller than 30°, whereas that of the hydrophobic area is larger than 110°. Liquid droplets are simultaneously formed on the hydrophilic areas that are the bonding areas, and then many chips are simultaneously supplied onto the hydrophilic areas in the self-assembly process. We have succeeded in simultaneously aligning five hundred chips with an average alignment accuracy of 0.5 µm within 0.1 s, which gives rise to a high bonding speed of 5000 chips/s. In contrast, conventional chip bonding machines provide low bonding speeds of 0.1 to 1 chip/s, depending on the alignment accuracy of 1 to 10 µm.

In the RW2W integration technology, it is necessary to temporarily bond many chips onto a carrier wafer after simultaneously aligning them by self-assembly. After debonding, these chips are simultaneously transferred to a support wafer. Therefore, temporarily bonding and debonding are very important steps in RW2W integration technology. An electrostatic temporary bonding and debonding method has been developed for the RW2W integration technology. Many chips are simultaneously bonded onto the electrostatic carrier (e-carrier) wafer by electrostatic force after simultaneous alignment by self-assembly, as shown in Fig. 3. The electrostatic force for temporary bonding is generated by applying a high voltage of 200 V to the electrodes embedded in the e-carrier. A high voltage with opposite polarity is applied to the electrodes for debonding chips. Chips with the support wafer are then debonded from the e-carrier by applying a voltage with opposite polarity. Thus, many chips are simultaneously transferred from the e-carrier to the support wafer. Transferred chips are thinned from the backside to form TSVs and metal microbumps, and then the target interposer wafer is bonded on the thinned chips with TSVs and metal microbumps. The support wafer is then removed from thinned chips/target interposer wafer for further stacking of chips. Super-chips can be fabricated by repeating this sequence.

2.2. 3-D heterogeneous opto-electronics integration technology.

A very attractive feature in 3-D LSI is the capability of heterogeneous integration. Especially, heterogeneous integration involving CMOS, MEMS, and photonic circuits...
has attracted much attention owing to its multi-functionality, high-speed communication, and low power consumption. Such heterogeneous 3D integration provides the possibility to achieve new functional LSIs.\(^{22}\) Typical examples of heterogeneous 3-D integration are the 3-D heterogeneous opto-electronic integrated module using 2.5-D Si interposer with embedded sensor chips, TSVs and micro-fluidic channels and organic substrate with optical waveguides (Fig. 4),\(^2\)\(^{23,24}\) the integration of MEMS chip on CMOS chip by chip self-assembly and sidewall interconnection technologies (Fig. 5),\(^2\)\(^{25,26}\) and the integration of an optoelectronic chip on a CMOS chip (Fig. 6).\(^{27}\) Figure 4 shows a 3-D heterogeneous opto-electronic integrated module using 2.5-D Si interposer. Image sensor stacked on ADC chip is for high-performance image-processing. An accelerometer MEMS sensor, optical sensor, and radio-frequency integrated circuits (RF ICs) are for high-sensitive sensing of the high moving speed. 3-D memory and 3-D processor are for high-performance data computing. Optical interconnection facilitates high-speed data transmission networking. Micro-fluidic channels assist in heat sinking from high-power LSIs. Figure 5 shows a 3-D stacked MEMS-LSI module where a CMOS chip is stacked on an LSI wafer and a pressure sensor MEMS chip is integrated onto the CMOS chip by chip self-assembly technique. Figure 6 shows a 3-D optoelectronic LSI where an optoelectronic integrated circuit chip with Si photonic devices is stacked on CMOS chips. The respective chip layers are
vertically connected by both optical interconnections (TSPV, through-Si photonic vias) and electrical interconnections (TSV, through-Si vias). A Si optical waveguide with an oxide cladding layer is used as a TSPV. In order to fabricate TSV and TSPV, a cylindrical deep trench and a ring-type deep trench are simultaneously formed by RIE. Then the Cu-TSV is formed by the process described earlier, whereas the Si-TSPV is formed by filling the ring-type deep trench with silicon oxide or organic material. Thus, the Si-TSPV and Cu-TSV are simultaneously fabricated. We confirmed that an optical signal is effectively guided by the TSPV. An optical grating coupler with a mirror was used to change the propagation direction of the optical signal. A high coupling efficiency of more than 80% in this optical grating coupler was obtained, which is sufficient for high speed optical data transfer. Continuous propagation of the optical signal from the vertical TSPV to the horizontal Si waveguide through the optical grating coupler has been confirmed.

2.3. Via-last backside TSV fabrication technology

Via-last backside TSV approach attracted attention as a better solution to heterogeneously integrate different devices, size, and materials, because of high flexibility to apply commercial chip/wafer, better reliability, and low cost process.\(^{28,29}\)

Figure 7 shows the via-last backside TSV fabrication process. First, a LSI device wafer with metal microbumps is temporarily bonded onto a support wafer then the Si substrate is thinned from the backside by gringing and CMP process. After via patterning on the grinded surface, the deep Si trench is formed from the backside by reactive-ion-etching (RIE) process until to expose the first level metallization layer (M1). The oxide liner is deposited into via holes and the bottom oxide liner in via hole is selectively etched by dry etching to expose again M1 layer. Next, the deep trench is filled with Cu by electroplating after the formation of a barrier metal layer, such as a Ta layer and a Cu seed layer. Re-distribution layer (RDL) is formed on the backside of the Cu-TSV by CMP or wet etching process depending on the required RDL width. Then metal microbumps are formed on the RDL by electroplating process. Finally, the support wafer is debonded from the thinned LSI wafer with backside TSVs. Figure 8 show SEM cross-sectional images of backside TSV formed after the process optimization. The fine backside Cu TSVs with 10 µm dia./50 µm depth are successfully fabricated without Si notch, liner under-etching, electroplating fail, and well contacted to M1 layer.

3. 3-D Stacked Image Sensor System for Autonomous Driving Assist

A stereo vision 3-D stacked image sensor module for an advanced driving assistant system is shown in Fig. 9, where a pair of 3-D stacked CIS chips and several 3-D...
stacked multicore processors are integrated on a Si interposer. High performance image processing using stereo vision for image recognition and obstacle detection is indispensable to guarantee safety while driving using the driving assistant system in an automobile. A pair of 3-D stacked CIS chips are used to provide stereo vision images with a high data rate of 10,000 frames/s. CIS chips have already been used to capture rear views in automobiles. However, a conventional 2-D CIS chip cannot provide stereo vision images at such a high data rate. 3-D stacked multicore processors are used to process the very large amount of data provided from a pair of 3-D stacked CIS chips with high speed and low power.\(^{30,31}\) Parallel processing is indispensable to achieve high speed and low power operation in multicore processors. The 3-D stacked structure is necessary for the high performance parallel processing. Figure 10 shows the photographs of 2-D core processor chip with self-test and self-repair functions fabricated by 90-nm CMOS technology (a) and 2-D cache memory chip fabricated by 130-nm CMOS technology, respectively. The processor chip has totally 1,920 TSVs and the cache memory has totally 1,200 TSVs, respectively. Figure 11(a) shows top view and SEM cross-sectional images of the fabricated 4-layer stacked 3-D multicore processor chip (Cu RDLs and bumps are not seen at the same line of Cu TSVs) and Fig. 11(b) shows top view and SEM cross-sectional image of the fabricated 2-
layer stacked 3-D cache memory chip (Cu RDLs and Cu/Sn bumps are seen), by using the RW2W integration technology with SAE bonding and backside TSV technologies.\cite{29,32,33} It is clearly observed in the figures that the backside Cu TSVs with a diameter of 10 µm and a length of 50 µm have good contact to the M1 layer with high alignment accuracy and without any notching and Cu voids.

Figure 12 show X-ray CT scanning images of a TSV array in 4-layer stacked multicore processor chip (a) and in 4-layer stacked cache memory chip (b), respectively. A number of Cu TSVs with 10 µm dia. and 50 µm length, RDLs, metal micro-bumps, and BEOL interconnects are clearly seen. This 3-D multicore processor has a new self-test and self-repair function to achieve high dependability. New built-in self-test circuits and self-repair circuits are embedded in each processor core. Processor chips are self-tested and self-repaired on-time using these circuits. It was estimated that a high dependability of 80 Fits can be achieved using such a new on-time self-test and self-repair function. Figure 13 show SEM cross-sectional view of TSV and 3-D X-ray CT scanning image (right) obtained from the fabricated 3-D stacked image sensor (CIS) chip.\cite{34} It is obvious in the image that the fabricated 3D stacked CIS chip has a layered structure with four layers where TSVs with 5 µm diameter and 50 µm lengths are clearly observed. Excellent block parallel-operation performance with high frame rate of 10,000 frames/s was confirmed in the fabricated 3-D stacked CIS chip.

However, 3-D heterogeneous integrated systems have many potential reliability challenges such as packaging materials, packaging methods, heat dissipation, and thermal

![Fig. 12. 3-D X-ray CT scanning images measured from TSV array of 10µm diameter and 50 µm length obtained in the 4-layer stacked 3-D multicore processor chip (a) and the 2-layer stacked 3-D cache memory chip (b), respectively.](image1)

![Fig. 13. (a) SEM cross-sectional image and (b) 3-D X-ray CT scanning image obtained from the 3-D stacked CIS image sensor chip with four-layer structure.](image2)
managements for automotive applications.\textsuperscript{35,36}

4. Summary

Various applications are expected for 3-D LSIs in the IoT era since 3-D LSI has many advantages, such as high performance, low power, multifunctionality, and small form factor. Heterogeneous 3D integration is expected to further expand the application area of 3D LSIs. Several types of LSI chips with different sizes, devices, and materials can be heterogeneously integrated to fabricate a super-chip. A new RW2W 3-D integration technology using SAE temporary bonding, 2.5-D interposer, and backside TSV has been developed to fabricate super-chips with high production throughput and yield. The stereo vision 3-D stacked image sensor module composed of pair of 3-D stacked CIS chips and several 3-D stacked multicore processors are fabricated using our SAE bonding and backside TSV technologies.

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