Testing of Front-End Readout Prototype ASICs Designed for WCDA in LHAASO

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Abstract—The water Cherenkov detector array (WCDA) is one of the key detectors in the large high altitude air shower observatory (LHAASO), which is proposed for very high gamma ray source survey. In WCDA, there are more than 3000 photomultiplier tubes (PMTs) scattered under water in an area of 80000 m². As for the WCDA readout electronics, both high precision time and charge measurement is required over a large dynamic range from 1 photon electron (P.E.) to 4000 P.E. To reduce the electronics complexity and improve the system reliability, a readout scheme based on application specific integrated circuits (ASICs) is proposed. Two prototype ASICs were designed and tested. The first ASIC integrates amplification and shaping circuits for charge measurement and discrimination circuits used for time measurement. The shaped signal is further fed to the second ADC ASIC, while the output signal from the discriminator is digitized by the FPGA-based time-to-digital converter (TDC). Test results indicate that time resolution is better than 250 ps RMS, and the charge resolution is better than 10% at 1 P.E., and 1% at 4000 P.E. which meets the requirements of the LHAASO WCDA.

Index Terms—ASIC, charge measurement, time measurement, LHAASO, WCDA

I. INTRODUCTION

The large high altitude air shower observatory (LHAASO) aims to discover the cosmic ray origin and perform the advanced scientific research in the field of high-energy physics and astronomy. The water Cherenkov detector array (WCDA) is one of the key detectors in the LHAASO, and it is composed of three water ponds with more than 3000 photomultiplier tubes (PMTs). Due to the research demands, both high precision time and charge measurements are required over a large dynamic range from 1 Photon Electron (P.E.) to 4000 P.E. The detectors in the LHAASO are shown in Fig. 1, including electromagnetic particle detector (ED), muon detector (MD), wide field of view Cherenkov telescopes array (WFCTA) and WCDA [1-7].

The rest of the paper is organized as follows. In Section II, ASIC-based front-end readout electronics is introduced and the amplification and shaping ASIC is presented in Section III. In Section IV, the SAR ADC ASIC is explained in detail. The results of the combined tests of two ASICs are provided in Section V. Lastly, a brief conclusion is given in Section VI.

II. ASIC-BASED FRONT-END READOUT ELECTRONICS

The readout system of the LHAASO WCDA is shown in Fig. 2. The output PMT signals are fed to the front-end electronics, and then the digitalized data are sent to the data acquisition system (DAQ) through switches. One front-end electronics module can deal with up to nine PMT output signals [1, 2, 8].

To simplify the circuit structure of the readout electronics, a readout scheme based on application specific integrated circuit (ASIC) is proposed. After the investigation of different ASICs used in large-scale physics experiments all over the world, including switched capacitor array (SCA) ASIC [9-11], time-over-threshold (TOT) ASIC [12-14] and the amplification and shaping ASIC [15-17], one technical route based on...
amplification and shaping, analog-to-digital conversion combined with digital peak detection is proposed [2]. The architecture of the ASIC-based PMT front-end readout electronics is shown in Fig. 3. Two prototype ASICs that integrate the amplification and shaping circuits and analog-to-digital converter (ADC) circuits are designed respectively. Charge measurement is performed by using the combination of the anode and dynode channels to cover the dynamic range from 1 to 4000 P.E. in the amplification and shaping ASIC. The shaper output signals are then digitized by the second ASIC, which is a successive approximation (SAR) ADC [18]. The digitized amplitude information is transformed to the field programmable gate array (FPGA) for peak detection. As for the time measurement, the PMT anode signal is fed to the discrimination circuits inside the amplification and shaping ASIC, and then digitized by the FPGA-based time-to-digital converter (TDC).

III. AMPLIFICATION AND SHAPING ASIC

A. Structure of Amplification and Shaping ASIC

The amplification and shaping ASIC is designed with three anode channels and three dynode channels based on the Global Foundry 350-nm CMOS dual gate technology.

The structure of the amplification and shaping ASIC is shown in Fig. 4, wherein it can be seen that it contains the preamplifiers, RC⁴ shaping circuits, output buffers, and discriminators. In the charge measurement, two channels are used to read out the signals from the anode and dynode of one PMT to achieve a large dynamic range. On the other hand in the time measurement, both low and high thresholds are used, whereas the latter is used to avoid the deterioration of time resolution around the baseline of a large input signal [8].

The structure of the anode channel is shown in Fig. 5. The preamplifier is a voltage amplifier because this kind of amplifiers has the high input impedance and wide bandwidth, which enables achievement of a high-precision time measurement. In the filter circuit, RC⁴ shaping circuit is used because the signal-to-noise ratio (SNR) of the output signal is higher than the SNR of the Sallen Key shaping circuit. Also, the time constant can be adjusted to 20 ns, 30 ns, 40 ns and 50 ns. Considering the large power consumption caused by the large load, the output buffer uses the class-AB structure to reduce the static power consumption. The output signal from the preamplifier is also fanned out for the discriminators of high threshold and low threshold [18].

The output signals of the RC⁴ shaping circuit nodes on cadence spectre platform are presented in Fig. 6. In Fig. 6, the signal changing trend of the RC output nodes can be observed, which meets the design requirements.
C. Amplification and Shaping ASIC Testing

The block diagram of the test system used to test the amplification and shaping ASIC is presented in Fig. 7. In the test system, the PMT output signals from the signal source are fed to the attenuator to simulate the dynamic range 1-4000 P.E. Then, the signals are fed to the ASIC via the 30-m cable for time and charge measurements. The output time and charge signals are transmitted to the ADC and data transmission board, and then to the computer for further analysis.

As shown in Fig. 7, the output signals from the discriminators are digitized by the FPGA TDC, and the output signals from the shapers are digitized by the AD9222, which is a 12-bit commercial ADC with a sampling rate of 62.5 Mega samples per second.

A total of 12 channels were tested. The results of the charge resolution, time resolution, and time delay of the amplification and shaping ASIC are presented in Fig. 8, Fig. 9, and Fig. 10, respectively. The charge measurement resolution is the ratio of the RMS value of the ADC code to the average value of the ADC code. The line delay method is used to calculate the time resolution because, in that way, the signal source jitter can be eliminated.

Test results indicate that the charge resolution is better than 10% at 1 P.E. and 1% at 4000 P.E., while the time resolution is better than 250 ps using the low threshold and better than 150 ps using the high threshold. Also, time walk is less than 15 ns in the full dynamic range.
D. Temperature Tests

Additional tests were conducted to evaluate the performance of the ASIC under different temperatures. Test results of the charge resolution, time resolution, and time delay of the amplification and shaping ASIC under different temperatures, which are 0°C, 25°C and 45°C, are shown in Fig. 11, Fig. 12, and Fig. 13, respectively.

![Fig. 11. Charge resolution of the amplification and shaping ASIC under different temperatures.](image1)

![Fig. 12. Time resolution of the amplification and shaping ASIC under different temperatures.](image2)

![Fig. 13. Time delay of the amplification and shaping ASIC under different temperatures.](image3)

In Figs. 11-13, it can be noticed that the amplification and shaping ASIC has a good temperature drift performance. And as presented before, the charge measurement resolution is better than 10% at 1 P.E. and 1% at 4000 P.E. and the time resolution is better than 250 ps while the time walk is less than 15 ns in the full dynamic range under different temperatures.

IV. SAR ADC ASIC

A. Structure of SAR ADC ASIC

According to the features of the shaper output signal, as well as the charge resolution requirement, an ADC ASIC was designed with a 12-bit resolution and a sampling rate of about 30 Msps based on the global foundry 1P6M 180-nm CMOS technology. The structure of the designed ADC including the sampling and holding circuits, capacitive DAC, dynamic comparator, asynchronous SAR logic, reference voltage buffer, and clock generator [19-22] is shown in Fig. 14.

![Fig. 14. Structure of the SAR ADC ASIC.](image4)

B. Capacitive DAC

The capacitive DAC of the designed SAR ADC ASIC is...
presented in Fig. 15. Considering the total number of capacitor and its power consumption, it is more reasonable to adopt two-level weight capacitor DAC structure with integral bridging capacitor.

and power module. The Balun (balanced to unbalanced) is used to convert a single-ended output signal of the signal source to a differential signal, and then the voltage of a differential signal is changed by AC coupling to 1 V which is required by the ADC.

The dynamic performance is tested by the Fast Fourier Transformation method. Test results are shown in Fig. 18, Fig. 19 and Fig. 20. The sampling rate was set to 31.25 Msps. The input signals were sine signals with the frequency of 2.4 MHz, 5 MHz, 8 MHz, 10 MHz, and 15.5 MHz. In order to avoid the coherent sampling, the frequency of an input signal was adjusted slightly.

C. SAR ADC ASIC Testing

The block diagram of the system for SAR ADC ASIC testing is presented in Fig. 17. The sine waves are generated by the SMA 100A signal source and then fed to the SAR ADC ASIC through the passive LC bandpass filter for digitization. The quantization codes are sent to the data transmission board for data processing and then transferred to the computer via the USB.

The peripheral circuits of the ADC ASIC evaluation board mainly include the input module, output module, clock module,
Fig. 20. ENOB dependence on the input signal frequency.

The typical frequency spectrums at the input signal frequencies of 8 MHz and 15.5 MHz are presented in Fig. 18 and Fig. 19, respectively. Fig. 20 shows that the ENOBs of all 12 ADC channels under test are between 8.92 and 9.65 bit.

V. COMBINED TEST OF TWO ASICs

The combined tests of two ASIC prototypes were conducted to evaluate the overall charge measurement performance. The test bench used in the tests is presented in Fig. 21.

The sampling rate was set to 31.25 Msps, and the time constant of the amplification and shaping ASIC was set to 40 ns. Only the charge measurement was conducted because the time measurement was accomplished by the discriminator in the amplification and shaping ASIC and FPGA TDC, which was achieved in the data transmission board.

Fig. 21. Test bench of the combined tests.

The charge resolution of the tests is presented in Fig. 22, where it can be seen that the charge resolution is better than 10% at 1 P.E. and 1% at 4000 P.E., which meets the requirements of the readout electronics for WCDA.

VI. CONCLUSION

Due to the requirements for high precision during the time and charge measurements over a large dynamic range of the LHAASO WCDA, the analysis and design of ASICs are carried out based on the amplification, shaping, and A/D conversion, along with the digital peak detection method. Two prototype ASICs are designed and tested. Tests results indicate that the SAR ADC ASIC can function well at 31.25 MSPS, and its ENOB is between 8.92 bit and 9.65 bit; the time resolution is better than 250 ps RMS, and the overall charge resolution is better than 10% at 1 P.E. and 1% at 4000 P.E., which meets the requirements of the readout electronics for LHAASO WCDA.

REFERENCES

[1] Ma, Cong, et al. “Analog front-end prototype electronics for the LHAASO WCDA.” Chinese Physics C 40.1 (2016): 016101.
[2] Lei, Zhao, Liu Shu-Bin, and An Qi. “Proposal of the readout electronics for the WCDA in the LHAASO experiment.” Chinese Physics C 38.1 (2014): 016101.
[3] He, H. H. "LHAASO Project: detector design and prototype." Proc 31st ICRC, LORZ, Poland (2009).
[4] Zhen, Cao. "A future project at tibet: the large high altitude air shower observatory (LHAASO)." Chinese Physics C 34.2 (2010): 249.
[5] Di Sciascio, G., & LHAASO Collaboration. (2016). The LHAASO experiment: From gamma-ray astronomy to cosmic rays. Nuclear and Particle Physics Proceedings, 279, 166-173.
[6] He, H. H. (2009). LHAASO Project: detector design and prototype. Proc 31st ICRC, LORZ, Poland.
[7] Li, H. C., Yao, Z. G., Yu, C. X., Chen, M. J., Wu, H. R., Zha, M., ... & Liao, W. Y. (2016). A way to measure the water quality of the LHAASO-WCDA with cosmic muon signals. arXiv preprint arXiv:1607.06687.
[8] Zhao, L., et al. "Prototype of a front-end readout ASIC designed for the water cherenkov detector array in LHAASO." Journal of Instrumentation 10.03 (2015): P03015.
[9] Kleinfelder, S. (2003). Gigahertz waveform sampling and digitization circuit design and implementation. IEEE Transactions on Nuclear Science, 50(4), 955-962.
References:

[10] Ritt, S., Dinapoli, R., & Hartmann, U. (2010). Application of the DRS chip for fast waveform digitizing. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 623(1), 486-488.

[11] Bechtol, K., Funk, S., Okumura, A., Ruckman, L. L., Simons, A., Tajima, H., ... & Varner, G. S. (2012). TARGET: A multi-channel digitizer chip for very-high-energy gamma-ray telescopes. *Astroparticle Physics*, 36(1), 156-165.

[12] Anghinolfi, F., Jarron, P., Martemiyanov, A. N., Usenko, E., Wenninger, H., Williams, M. C. S., & Zichichi, A. (2004). NINO: an ultra-fast and low-power front-end amplifier/discriminator ASIC designed for the multigap resistive plate chamber. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 533(1-2), 183-187.

[13] Delagnes, E., Abbon, P., Bedfer, Y., Faivre, J. C., Kunne, F., Magnon, A., ... & Thers, D. (2000). SFE16, a low noise front-end integrated circuit dedicated to the read-out of large Micromegas detectors. *IEEE Transactions on Nuclear Science*, 47(4), 1447-1453.

[14] Nishino, H., Awai, K., Hayato, Y., Nakayama, S., Okumura, K., Shozawa, M., ... & Arai, Y. (2009). High-speed charge-to-time converter ASIC for the Super-Kamiokande detector. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 610(3), 710-717.

[15] Bouchel, M., Dulucq, F., Fleury, J., de La Taille, C., Martin-Chassard, G., & Raux, L. (2007, October). SPIROC (SiPM Integrated Read-Out Chip): Dedicated very front-end electronics for an ILC prototype hadronic calorimeter with SiPM read-out. In *Nuclear Science Symposium Conference Record, 2007. NSS'07. IEEE* (Vol. 3, pp. 1857-1860). IEEE.

[16] Raux, L., Callier, S., Di Lorenzo, S. C., Dulucq, F., de La Taille, C., Martin-Chassard, G., & Seguin-Moreau, N. (2012, October). SPIROC: Design and performance of a dedicated very front-end for an ILC prototype Hadronic Calorimeter with SiPM. In *Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2012 IEEE* (pp. 557-561). IEEE.

[17] Barrillon, P., Blin, S., Bouchel, M., Caceres, T., de La Taille, C., Martin, G., ... & Seguin-Moreau, N. (2006, October). MAROC: Multi-anode readout chip for MaPMTs. In *Nuclear Science Symposium Conference Record, 2006. IEEE* (Vol. 2, pp. 809-814). IEEE.

[18] Jianfeng, Liu, et al. "Evaluation of a front-end ASIC prototype for the readout of PMTs in Water Cherenkov Detector Array." *Electronic Measurement & Instruments (ICEMI), 2015 12th IEEE International Conference on*. Vol. 1. IEEE, 2015.

[19] Liu, Jian-Feng, et al. "Design and simulation of a 12-bit, 40 MSPS asynchronous SAR ADC for the readout of PMT signals." *Chinese Physics C* 40.11 (2016): 116103.

[20] Liu, Wenbo, Pingli Huang, and Yun Chiu. "A 12-bit, 45-MS/s, 3-mW redundant successive-approximation-register analog-to-digital converter with digital calibration." *IEEE Journal of Solid-State Circuits* 46.11 (2011): 2661-2672.

[21] Chan, Chi-Hang, et al. "A voltage-controlled capacitance offset calibration technique for high resolution dynamic comparator." *SoC Design Conference (ISOCC), 2009 International*. IEEE, 2009.

[22] Murmann, Boris. "Digitally assisted data converter design." *ESSCIRC (ESSCIR), 2013 Proceedings of the IEEE*, 20