Helper Without Threads: Customized Prefetching for Delinquent Irregular Loads

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Abstract—The growing memory footprints of cloud and big data applications mean that data center CPUs can spend significant time waiting for memory. An attractive approach to improving performance in such centralized compute settings is to employ prefetchers that are customized per application, where gains can be easily scaled across thousands of machines. Helper thread prefetching is such a technique but has yet to achieve wide adoption since it requires spare thread contexts or special hardware/ firmware support. In this paper, we propose an inline software prefetching technique that overcomes these restrictions by inserting the helper code into the main thread itself. Our approach is complementary to and does not interfere with existing hardware prefetchers since we target only delinquent irregular load instructions (those with no constant or striding address patterns). For each chosen load instruction, we generate and insert a customized software prefetcher extracted from and mimicking the application's dataflow, all without access to the application source code. For a set of irregular workloads that are memory-bound, we demonstrate up to 2X single-thread performance improvement on recent high-end hardware (Intel Skylake) and up to 83% speedup over a helper thread implementation on the same hardware, due to the absence of thread spawning overhead.

1 INTRODUCTION

The rise of the cloud and big data has caused the memory footprint of applications to grow faster than the pace of technology scaling (i.e., memory capacity and core counts). Moreover, as data parallel workloads increasingly move away from the CPU into GPUs, FPGAs and accelerators, the CPU is faced with a rise of irregular memory applications. As a result, data center CPUs can spend a significant fraction of execution cycles waiting for the caches [33]. Yet, despite the large core counts available, Amdahl’s Law means that mitigating such single-thread performance bottlenecks remains crucial to achieving improved overall performance [26], [74]. Interestingly, the centralization of compute in the data center can be seen as an opportunity to be exploited. By customizing performance optimizations per application, gains can be scaled across many thousands of machines. This approach relies on obtaining intimate knowledge of an application’s behavior through profiling and hardware performance counters [71], and using such information to extract optimal performance from the hardware for the target application.

Speculative precomputation [12], [13], [15], [16], [20], [21], [43], [59], [67], [75], otherwise known as helper threading [31], [32], [34], [35], [41], [42], [68] is such a technique. It reduces the single-thread latency of an application by using idle thread contexts in the hardware to spawn special-purpose, speculative threads called helper threads. Helper threads contain computation extracted from the main thread and consume the latency of execution on behalf of it. They encounter cache misses and branch mispredictions ahead of the main thread, and act as execution-driven prefetchers or branch predictors for the main application, thereby improving its latency significantly. Their benefit accrues from the fact that they are tailored to the specific application they are extracted from, and therefore orchestrate the hardware precisely to suit its needs.

However, helper threads can be tricky to implement efficiently. Although the original ideas appeared over two decades ago, we are not aware of any commercial processors with hardware support for helper threads today. Note that industry-strength compiler support is available for code generation of helper threads on multicore CPUs [1], [3]. However, the corresponding hardware support for generating low-overhead micro/nano threads (for e.g., as in [12]) is absent. Hence, the dynamic thread spawn overhead is still significant in current operating systems. In the absence of such specialized hardware support, helper threads have two disadvantages today: (1) the need for spare thread contexts; and (2) the difficulty in synchronizing and match the rates of the main application and the helper threads. In this work, we overcome both these limitations with an inline prefetching technique inspired by software pipelining [37], [56], yet our method retains an important benefit of helper threads: it works without access or modification to the application source code. This makes our technique attractive to cloud service providers who run third-party applications at scale.

1.1 Delinquent Irregular Loads

Load instructions in a program can fall into three categories: (a) constant address, (b) striding, and (c) irregular. Constant address loads are loads whose virtual address does not change over multiple dynamic instances of the load (for e.g., global variables and stack accesses). Striding loads are those with successive virtual addresses following an arithmetic progression (for e.g., array accesses). Irregular loads are those which do not fall into either of the above two categories (for e.g., indirect and pointer references). Furthermore, loads that frequently miss in the cache are said to be delinquent. While current hardware mechanisms are effective at prefetching regular address patterns [22], delinquent irregular loads (DILs) remain a challenge.

For a set of 165 traces from commercial applications identified by our framework as containing prefetchable DILs (see Section 4 for a formal definition), Figure 1 shows the fraction of CPU cycles...
spent stalled waiting for data at the time of retirement of the specific DILs. The traces are from several client applications (productivity, games, content creation), server applications (cloud, database, enterprise, HPC) and CPU benchmarks (cloud, database, enterprise, HPC) and CPU benchmarks simulated on a cycle-accurate simulator modeling the Intel Skylake [18] microarchitecture. On average, each trace has about three prefetchable DILs that are memory-bound. Should all that stall time be reduced to zero, the potential geometric mean speedup possible in these traces is 15%, which is significant headroom. However, these opportunities were identified from a universe of over 2000 traces and building a prefetcher in hardware for such a narrow focus is not a profitable microarchitectural trade-off since such a prefetcher will be unused most of the time. On the other hand, large silicon and software companies currently employ significant software resources for manually optimizing select applications (e.g., Figure 5a is from a search engine). The scale of these high-value applications justifies the extra effort spent in optimizing them ( [9], [65]). As long as these applications fall into the right side of figure 1, targeting the DILs from them through software is a better strategy than implementing a specialized prefetcher in hardware. Hence, we propose an inline software prefetching technique that selectively targets DILs that are memory-bound for prefetching.

1.2 Contributions
This paper makes the following contributions:

- We overcome the limitations of helper threads with an inline prefetching scheme that does not require spare thread contexts or special hardware support;
- We eliminate the need for thread synchronization in helper prefetching by employing a statically-controlled prefetch distance and a prefetcher generation process inspired from software pipelining;
- For a set of irregular memory workloads, we demonstrate up to 2X end-to-end execution time speed-up on current high-end hardware and up to 83% gain over helper threads.

2 RELATED WORK
A full discussion of the literature on prefetching is beyond the scope of this paper; the interested reader is referred to Falsafi and Wenisch [22] and Lee et. al. [38] for thorough treatments of the hardware and software approaches to prefetching and the various challenges involved. Limiting our focus to irregular load prefetching, prior work can be classified into three main categories:

Microarchitectural techniques use on-chip storage to record patterns in the addresses of the irregular load and predict a future address to prefetch if the current address is from one of the recorded patterns [27], [30], [47], [49], [54], [57], [70], [72]. These approaches require large on-chip storage, the cost of which continues to preclude their commercial viability. The Indirect Memory Prefetcher (IMP) [72] is an exception—it uses very little on-chip storage by targeting specific indirect memory patterns of the form $a[b[i]]$, where the array $a$ is addressed by a striding feeder load $b[i]$. At runtime, IMP records in a hardware table the relationship between the striding load and the irregular load address and uses this to predict future addresses. The goals of our present work are to minimize prefetcher implementation complexity, as well as improve performance on current hardware. Hence, we...
choose the software implementation route. Moreover, as described in Section 3, our dataflow analysis framework is generic enough to handle more complex patterns such as $a[f(b[i])]$ where $f$ is any arbitrary function.

**Computation-based techniques** typically execute program instructions ahead of time to prefetch delinquent loads. While computation-based prefetching [25], [34], [48], [55] can be accurate, large runahead buffers or spare thread contexts for running helper threads are resource-intensive, especially considering their energy costs. Since regular loads are the overwhelming majority in general purpose applications, dedicating special hardware resources to handle comparatively rare events such as irregular loads may not represent a good microarchitectural trade-off. In contrast, a software implementation is more flexible and can be invoked to incur the cost only when the benefit is known to be greater.

There are other limitations to computation-based methods beyond just the cost of implementation. For example, runahead [48] is a technique that ignores a branch misprediction and continues execution to extract prefetching benefit from control independent instructions. However, it is not designed to handle dependent misses (i.e., misses whose addresses are data-dependent on previous misses). Our approach handles dependent misses by prefetching the entire dependency chain through to the missing leaf instruction (see Section 3).

Helper threads [12], [13], [15], [16], [20], [21], [31], [32], [34], [35], [41], [42], [43], [59], [67], [68], [75] extract the backward slice of a delinquent load and run it on a spare thread context. When the latency of the backward slice is less than that of the original loop, the helper thread runs ahead of the main thread and prefetches memory accessed by the main thread into the cache. This technique has the advantage of being flexible enough to be implemented in hardware [12], [13], [15], [16], [20], [21], [23], [43], [59], [67], [75], or software [31], [32], [34], [35], [41], [42], [68]. It can also work in the absence of high-level source code and has been demonstrated in a compiler [35], binary tool [41], or a dynamic optimizer [42]. However, all prior work in this area has either required spare thread contexts or special hardware/firmware support. Virtual Multithreading (VMT) [68] overcomes the need for spare thread contexts by partitioning the registers available to the compiler between the main and the helper computation. However, it still requires special *yield* instructions to orchestrate the transfer of control between the virtual threads and corresponding modifications to the processor firmware. In our work, by choosing an inline implementation, we (1) avoid the need for any extra hardware or firmware support; (2) sidestep thread spawning overheads and synchronization bugs since there are no threads to run; and (3) make straightforward the rate matching between the main computation and the prefetcher by statically setting the prefetch distance.

Similar to our approach, recent work [8] has proposed inserting prefetch hints based upon binary analysis. However, due to the absence of control flow analysis, it requires specialized hardware support in the form of speculative loads. Moreover, the benefits demonstrated are on top of a simulated microarchitecture without state-of-the-art hardware prefetchers such as [63], [72]. In contrast, we show benefit on existing hardware (not requiring special hardware support) and in comparison with state-of-the-art hardware prefetchers.

**High level language software techniques.** Broadly speaking, software-based prefetchers are typically concerned with inserting prefetch hints [4] into a program or modifying its data structures. Most [6], [14], [38], [45], [58] rely on access to the program's source code. For instance, Roth and Sohi [58] augment the data layout of linked data structures with a jump pointer that acts as a prefetch pointer. Others [5], [6] have demonstrated significant speedup with programmable prefetching. However, many real-world situations preclude access to program source code, e.g., while using third party libraries or when serving third-party applications in the cloud. In such situations, the ability to improve performance in the absence of source code is attractive. This work retains such capability from its lineage in helper threads. Finally, while our prefetcher generation is inspired from software pipelining [37], [56], [61], it is not a static instruction scheduling technique. Our target is performance improvement over dynamically scheduled out-of-order processors that hold multiple iterations of loops in their instruction window. The performance improvement is exclusively due to the duplication of code that stays a constant number of iterations ahead.

### 3 A Motivating Example

Let us now consider an example scenario where memory-bound DILs occur frequently. Hash tables are widely used because of their algorithmic efficiency in converting expected linear and logarithmic time operations into expected constant time operations [17]. For instance, they are used to implement associative arrays in popular scripting languages such as Python and R, and in relational databases for indexing. However, the underlying hash functions generate hash table keys are designed specifically to disrupt data locality, *i.e.*, they are designed to enforce irregular access. Thus, when a given hash table has too many unique keys to be held in on-chip caches, loading hash table entries can become a performance bottleneck.

```cpp
#include <unordered_map>
typedef unsigned long UINT64;
typedef unordered_map<UINT64, UINT64> Histo;
void gen_histo(UINT64 *array, UINT64 size, Histo histo) {
    for(UINT64 i=0; i < size; i++)
        if (histo.find(array[i]) != histo.end())
            histo[array[i]]++;
        else
            histo[array[i]] = 1;
}
```

Listing 1: Example Histogram Calculation using C++ STL unordered_map, illustrating memory-bound DILs.

Listing 1 shows a sample frequency histogram computation over an integer array that uses C++ STL unordered_map, the standard implementation of a hash table, to store the frequency counts. The code assigns a frequency of 1 to a key encountered for the first time and increments the frequency every time the same key is subsequently encountered. Assuming each key is encountered several times, the hot path around the loop is through the frequency increment shown in Line 10. Figure 3a shows the x86_64 disassembly for this short, hot path around the loop when compiled with gcc 6.1 using the -O3 -march=native flags. Please note that this disassembly is part of the implementation of unordered_map and that longer, cold paths around the loop are not shown for clarity. It highlights the load instructions in the loop with different colors: constant address loads are shown in blue, striding loads in green, and irregular loads in yellow or red. Microarchitectural simulation of this loop shows that the average cycles per instruction (CPI) measured at retirement (as the number of cycles between the retirement of the current dynamic
When the number of unique keys in the hash table is too large, we make two design decisions: (1) we exit the helper thread at all times, and (2) we observe that as part of the hashing function, the value from the striding load feeds all the DILs in this loop. In Listing 1, this striding load causes the helper thread to run ahead of the main loop, even though it is only 3-30 µs delayed. The helper thread can cause segmentation faults for the main thread when it runs ahead despite the 3-30 µs delay. Therefore, we choose the clone method to spawn the backward slice of the critical DIL as a separate thread at hundreds-of-thousands of CPU cycles in our test system. Next, we measure the overhead of spawning a thread using this approach to be approximately 3-30 µs.

To explicitly contrast runnable and chasing DILs, we provide examples from real applications in Figure 5. To see why it is difficult for the microarchitecture to execute this loop, Figure 3b shows the backward slice of the critical DIL. An edge from a lower IP to a higher IP indicates the dataflow within an iteration while an edge from a higher IP to a lower IP indicates the dataflow from a previous iteration of the loop. A cycle in this graph indicates a loop-carried dependence. We can see that a single striding load at address 0x6bc feeds all the DILs in this loop. In Listing 1, this striding load corresponds to the variable array. Hardware prefetchers prefetch this striding load successfully. Looking at the path from the striding load to the critical DIL (green to red path) in the backward slice, we can observe that as part of the hashing function, the value from the striding load is divided by a constant and the remainder is used to calculate the address of the DIL in successive iterations. These indications occurring after the non-linearity (due to the div instruction) are beyond the capability of hardware prefetchers today. When the number of unique keys in the hash table is too large to fit in the on-chip caches, each of these indications becomes DRAM-bound. Even with large out-of-order instruction windows, the latency of three consecutive round-trips to DRAM becomes impossible to hide.

Neither IMP [72] nor runahead [48] improves the performance of this loop. The non-linear relationship between the value of the striding feeder load and the consumer DIL is outside the purview of IMP, which only captures linear relationships of the form $ax + b$. Runahead, on the other hand, can alleviate branch mis-speculations, but the chain of dependent cache misses will ultimately cause the runahead engine to stall for data.

### 3.1 Helper Thread Implementation

Before delving into our approach, we discuss the challenges in implementing a prefetcher using traditional helper threads. Prior work has studied several design choices including hardware support for extremely lightweight threads [20] and a variety of trigger mechanisms, including one helper thread spawning another in series [16]. However, our requirement is that the prefetcher must be able to run on existing CPUs without any additional hardware or firmware support. Hence, we choose the clone system call in Linux [69] to create helper threads. As a first step, we measure the overhead of spawning a thread using this approach to be approximately 3-30 µs, which is equivalent to several tens-to-hundreds-of-thousands of CPU cycles in our test system. Next, we spawn the backward slice of the critical DIL as a separate thread at each entry into the loop. Since the backward slice is much smaller than the main loop, it runs ahead despite the 3-30 µs delay.

Note that the loop has calls to functions that allocate memory on-demand for the hash table. Thus, if the helper thread runs arbitrarily ahead, it can cause segmentation faults for the main program by accessing memory that has not yet been allocated. Here, we make two design decisions: (1) we exit the helper thread at all paths other than the hot path through the loop; and, (2) to balance the overhead of thread spawning against the performance benefit due to prefetching, we skip a tunable fraction of the loop before starting the helper thread. This allows time for most memory allocation to complete before we begin prefetching.

We run the application with the helper threads for two different inputs and examine the speedup over the baseline implementation without prefetching. We run the helper version in two different modes: first, we allow the helper thread to run only on the same core as the main thread. In this case (2T), the main and helper threads use the two SMT contexts of the same core. In the second mode (All), we allow the threads to be scheduled in any of the cores available on the machine. The speedup is shown in Figure 4 for different settings of the tunable thread start delay (skip).

When the tunable skip thresholds are low, the helper threads are created and destroyed too often alongside the frequent memory allocation. When there is no restriction on the number of parallel thread contexts available, this does not cause too much slowdown (right, “All”), but with only two SMT contexts on the same core, the spawning penalty is prohibitive (left, “2T”). On the other hand, high skip thresholds result in lost opportunity. Moreover, the maximum speedups on the right are low, due to cache interference caused by threads hopping to different cores. Furthermore, the optimal skip threshold for the 2T case varies across inputs (it is 87.5% for Input 1 and 37.5-50% for Input 2). This serves to illustrate how tricky it can be to tune the helper thread implementation.

### 4 Method

In the previous section, we explained the problem of memory-bound DILs through a hash table example and outlined the challenges in implementing a prefetcher with helper threads. Here, we will outline our approach to a solution, with a reminder that we want to create a prefetcher implementation without threads.

Observing the backward slice shown in Figure 3a, we see that the one cycle in the graph is comprised of a single instruction 0x6cf, i.e., the stride address increment, and that it is the only loop-carried dependence in this backward slice. Note that a cycle in the backward slice captures the essential relationship between the addresses produced by a DIL in successive iterations. If the instructions in the cycle can be executed efficiently by the hardware, then it becomes possible to overcome the bottlenecks outside the cycle through software prefetching. Conversely, if the cycle cannot be executed efficiently by the hardware due to true data dependencies, then the performance of such a DIL cannot be improved with software prefetching.

Specifically, if the backward slice of a DIL has no cycles with any irregular memory operations, then such a cycle can be executed efficiently by the hardware. Such a cycle can be run multiple iterations ahead of the main computation by a software prefetcher and we describe DILs with such a backward slice as runnable. On the other hand, if the cycles in the backward slice have delinquent irregular memory operations, then running a few iterations ahead gives no advantage; the performance bottleneck would simply shift from the main computation to the prefetcher computation instead. This is the classic situation of pointer chasing and we refer to such DILs as chasing DILs. Short of moving the whole cycle of chasing computation closer to memory (through techniques such as processing in memory), not much can be done to improve such loads.

To explicitly contrast runnable and chasing DILs, we provide respective examples extracted from real applications in Figure 5.
After the entry into the loop, the carrot locks steps with the horse. We call this phase of dynamic execution the "stay ahead" dynamic execution-phase. During the last $k$ iterations ahead of the horse.

We call this phase in the dynamic execution the "stay ahead" phase. Once a prefetchable DIL has been identified, inspired by software pipelining [37, 56], we take a carrot and the horse approach to prefetching it. We duplicate the backward slice code and assign new registers to it. By analogy, this code is the "carrot" and the main computation is the "horse". Prior to the entry into the loop, the carrot is first extended $k$ iterations ahead of the horse. We call this phase in the dynamic execution the head start phase. After the entry into the loop, the carrot locks steps with the horse and stays a constant $k$ iterations ahead. We call this phase in the dynamic execution the stay ahead phase. During the last $k$ iterations of the loop, the carrot ceases to stay ahead and merges with the horse. We call this phase of dynamic execution the join phase. Finally, since the carrot overwrites the architectural registers, we also need to save them onto the stack at loop entry and restore them at loop exit.

This process is more formally described in Figure 6. The figure contrasts the dynamic instruction streams and the memory addresses accessed before and after the insertion of the software prefetcher code. At the top, each iteration in the original instruction stream has a DIL (marked DIL$_{\text{a}}$) that demands a particular memory access. The coloring scheme remains the same as in Figure 3. The backward slice of the runnable DIL shown in Figure 5a has three total cycles, but none have irregular memory operations. In contrast, the backward slice of the chasing DIL shown in Figure 5b has two cycles, one of which has an irregular memory operation at 0x1000 (yellow).

Through dataflow analysis, we can determine if a DIL is runnable. However, merely being runnable does not guarantee that a DIL is also prefetchable. We must also examine the control flow within the loop. If the backward slice of a DIL varies along the different control flow paths through the loop, then the backward slice is control dependent on the branches within the loop. A popular example of such a situation occurs in an array-based implementation of a binary search tree. If the current search node is at index $x$, the next node to be searched can either be the left child (at index $2x+1$) or the right child (at index $2x+2$), dependent on the result of the comparison at the current node. We exclude such scenarios by design for two reasons: first, such situations are rare and second, prefetcher complexity increases tremendously in such cases. To see why, let us consider the example of the binary tree where both the paths are equally likely. If we want to prefetch $k$ iterations ahead, then there are $2^k$ possible addresses to prefetch. We have the option of either prefetching all of those addresses or implementing a software-based branch predictor to select one of the addresses to prefetch. Both of these options are unrealistic and hence we deliberately exclude such situations by considering only DILs that have backward slices that remain control independent of all the branches within the loop. Finally, when a DIL is runnable as well as control independent, we call it prefetchable. These two criteria comprise our DIL screen; our software prefetcher framework only targets DILs that pass this screen for custom prefetching code generation.

Once a prefetchable DIL has been identified, inspired by software pipelining [37, 56], we take a carrot and the horse approach to prefetching it. We duplicate the backward slice code and assign new registers to it. By analogy, this code is the “carrot” and the main computation is the “horse”. Prior to the entry into the loop, the carrot is first extended $k$ iterations ahead of the horse. We call this phase in the dynamic execution the head start phase. After the entry into the loop, the carrot locks steps with the horse and stays a constant $k$ iterations ahead. We call this phase in the dynamic execution the stay ahead phase. During the last $k$ iterations of the loop, the carrot ceases to stay ahead and merges with the horse. We call this phase of dynamic execution the join phase. Finally, since the carrot overwrites the architectural registers, we also need to save them onto the stack at loop entry and restore them at loop exit.

Through dataflow analysis, we can determine if a DIL is prefetchable. The two plots on the left are from when the main and helper threads are restricted to SMT contexts in the same core. The two plots on the right are obtained by allowing the threads to be scheduled on any of the available cores.
address. At the bottom, customized prefetching code (yellow) is inserted into the instruction stream. These are given a head start to run iterations ahead such that the addresses they prefetch mitigate all the DILs within stay ahead and join phases. Please note that although the carrot and horse approach sounds similar in principle to software pipelining, it is not an instruction scheduling technique and the speedups are exclusively because of the duplication of code that stays a constant number of iterations ahead.

With this overall picture in mind, we provide the details of our method next.

4.1 Analysis and Screening

The first step is the identification of DRAM-bound load instructions. For this purpose, we employ detailed profiling and dataflow analysis of the application of interest. Our analysis infrastructure uses a pintool [44] to generate the basic block vector profiles of the application at a 10M instruction granularity and the SimPoint [62] methodology to identify representative regions for microarchitectural simulation. We implement K-means clustering and augment it with silhouette analysis [60] to ensure clusters of good quality. We then use PinPlay [53] to generate two traces for each SimPoint, a short trace for functional simulation and dataflow analysis and a long trace for cycle-accurate microarchitectural analysis. The short functional simulation traces are 10M instructions long. The long microarchitectural traces are 310M instructions long in order to accommodate in simulation a cache warmup period of 295M instructions, microarchitectural warmup period of 5M instructions, and a detailed cycle-accurate simulation of 10M instructions.

Next, we perform cycle-accurate simulations of a microarchitecture resembling Intel’s Skylake [18] CPU on an in-house x86_64 performance simulator. The cycle simulations produce a list of DRAM-bound load instructions, defined as those with an average CPI higher than the latency of the last level cache. This output list is sorted by the fraction of the total L1 data cache misses produced by each load instruction. We then select the delinquent load instructions covering the top 99% of all the L1 data cache misses for further dataflow analysis. It is worth noting that we chose this route of implementation through trace-level, cycle-accurate microarchitectural simulation, but there are other ways to identify DRAM-bound load instructions, e.g., with assistance from hardware performance counters [19], functional cache simulation [28], profiling DRAM accesses [10], [66] or even statically [52].

The next step in our analysis is to identify the irregular loads from the list of DRAM-bound loads. We achieve this through the calculation of address deltas, defined as the numerical difference between the addresses produced by successive executions of a load instruction. We compute the address delta histograms for all the DRAM-bound loads in the short traces. An n-dimensional regular array accessed inside a loop can produce n different address deltas. Hence, in order to filter out high dimensional regular arrays common in numerical code, we choose a threshold of 10 deltas, i.e., we select only those load instructions with at least 10 distinct address deltas covering the top 90% of the executions. This is our DIL candidate list.

We then build the dynamic control flow graph [7] using the short traces and determine the loop immediately encompassing each DIL. After that, we enumerate all the different control flow paths within the loop. For each such path, we perform dynamic dataflow analysis [36] to compute the backward slice graph and enumerate all the simple cycles in it [29]. With the information from the aforementioned address delta analysis, we find the cycles that do not involve any irregular memory operations and determine whether the DIL is runnable. When a runnable DIL has the same backward slice along all the control flow paths within its encompassing loop, we flag it as control independent and hence prefetchable. For
these graph computations, we utilize the networkx [24] package in Python.

Once all the prefetchable DILs and their encompassing loops are identified, we group the DILs into loops and determine which among them inside the same loop produce addresses that are at a small constant offset from one another. We drop all such DILs from our list except the DIL with the largest average CPI (the critical DIL) since such addresses either fall within the same cache line as the critical DIL or regular hardware prefetchers will handle these properly. The load instruction at address $0x6d8$ in Figure 3 is an example of such a case. Moreover, to avoid alias analysis, we restrict ourselves to situations where the addresses of the stores in the backslice can be inferred statically. Through these successive screens, we are ultimately left with only those prefetchable DILs that are most challenging for the hardware to prefetch.

### 4.2 Prefetcher Generation

We now illustrate the generation of the customized prefetching code for the phases shown in Figure 6, using the hash table example from Figure 3. Keep in mind that we do not operate on the source code and hence begin with the loop shown in Figure 3a. We insert the prefetcher assembly into the application’s assembly directly.

As a first step, we attempt to find unused architectural registers inside the loop. When there are no unused registers available, we create new local variables on the stack and select registers to spill onto them in the following order for minimal performance impact:

1. Registers only written to but never read from inside the loop (only the last write to these registers need to be made visible outside the loop);
2. Registers only read from but never written to inside the loop (all references to these registers will be replaced by their corresponding stack loads).

For our example in Figure 3a, it turns out that registers $r_{11}$, $r_{14}$ and $r_{15}$ are unused inside the loop. Among these, $r_{11}$ is caller-saved and there is a function call inside the loop, meaning it could potentially be used inside the function call. Thus, we choose $r_{14}$ and $r_{15}$ as the registers to use for our carrot computation i.e., inside the customized prefetching code. As discussed before and shown in Figure 6, the first step is to save these registers onto the stack:

```assembly
# save unused registers at loop entry
pushq $r_{14}$
pushq $r_{15}$
```

Listing 2: The save phase.

Next is the head start phase, also performed at loop entry, where the prefetch computation gets a $k$-iteration head start. In our example, $rbp$ is the only register written inside the cycle in the backward slice graph. Hence, we duplicate it onto $r_{14}$. We also use $r_{15}$ as scratchpad to perform the loop boundary check by comparing it with the loop limit in $rbx$, as follows:

```assembly
# duplicate line 4
movq $rbp, $r_{14}$
movq $rbx, $r_{15}$
# duplicate lines 11-13, write output to $r_{15}$
xorq $rbx, rbx$
divq $8$
movq $rbx, $r_{15}$
```

Listing 3: The head start phase.

The next two phases are the (1) stay ahead phase, where the prefetcher (carrot) computation stays ahead of and in lock step with the main (horse) computation, and (2) the join phase, where the prefetcher computation no longer stays ahead and ultimately merges with the main computation. Both of these phases are inserted into the loop body and are shown in Listing 4. For clarity, we distinguish the inserted code from the existing code by highlighting the inserted code in yellow.

```assembly
# add $8 to loop limit in $rbx
addq $0x8, $rbx
```

Listing 4: The stay ahead and join phases.

The last step is to restore the saved registers at all exit points of the loop.

```assembly
# restore saved registers at all loop exits
```

Listing 5: The restore phase.
for those outputs dependent on operating system behavior such as timing measurement, random number generation, signal handling, etc.

5 EXPERIMENTAL EVALUATION

Recall from figure 1 that while DIL prefetching may not benefit all applications, some irregular applications can benefit a lot (right side of figure 1). For instance, several high value cloud applications fall into this category. Hence, we evaluate our proposal on a set of irregular memory workloads similar to the work by Ainsworth and Jones [6] (we do not use the applications from figure 1 since we don’t have access to their binaries).

We study three applications from their work that are bottlenecked by DRAM-bound DILs and add two more to the evaluation including the hash table example we discussed in Sections 3 and 4. Since our focus is on single thread performance, we utilize the serial versions of the benchmarks for experimentation. We compile all benchmarks with gcc 6.1.0 using the flags -O3 -march=native on an Intel Xeon E5 server CPU. We run all the analysis tools for prefetchable DIL identification and generate the customized prefetching code on the same server as well.

5.1 Benchmarks

We now provide a brief overview of the applications studied.

- **STLHistogram** is the example we discussed in Sections 3 and 4. It generates a random array of integers and computes the frequency histogram of the array using C++ STL unordered_map. It takes the size of the array and the number of unique elements in it as arguments. Microarchitectural performance of this application suffers when neither the input array, nor the frequency histogram fits inside the on-chip caches. We choose this benchmark due to the popularity of hash tables in programs and the potential for customized prefetching to improve performance. Please note that since open address hash tables are popular, we also studied a policy based implementation of STLHistogram. While the baseline performance of this new version was 7X better than the unordered_map version, the performance improvement opportunity was very similar to the unordered_map version with a single prefetchable memory bound DIL causing most of the stalls. Hence, we report results only for the unordered_map version.

- **PageRank** is an implementation of the popular web-page relevance ranking algorithm [50] using the C++ Boost Graph Library [2] (BGL). It is a graph algorithm that ranks a website based upon the ranks of the websites that link to it.

- **HashJoin** [11] from the University of Wisconsin implements the join operation of a relational database [64] in main memory using hash tables. The join operation is very common in Structured Query Language (SQL) queries.

- **Graph500CSR** is part of the Graph500 [46] benchmark suite designed to rate supercomputer systems on their data-intensive performance. It performs Breadth-First Search (BFS) on a large graph implemented using a compressed sparse rows (CSR) data structure.

- **Cuckoo** [73] is an application modeling packet processing in the context of Network Function Virtualization (NFV) using the cuckoo hashing algorithm [51].

We run the sequential versions of these applications on the inputs shown in Table 1 and generate traces as discussed in Section 4.1. An automatic tool analyzes the traces to produce the list of prefetchable DILs, the loops they belong to, and a list of available registers for code generation. The customized prefetching code is then generated semi-automatically with manual intervention. Specifically, our scripts generate a skeletal prefetcher code with the duplicated backslice and a list of candidate registers. However, register fills/spills, null-pointer skips and handling slices across function calls are done manually. Another automatic tool then statically rewrites the original function in the binary with a dynamic version that allocates the optimized code in the heap and calls it through a function pointer. We then run the optimized binary to ensure that its output matches the original. For performance measurement, we employ an Intel Core i9-7900X Skylake CPU with all the hardware prefetchers enabled, running at 3.3 GHz and frequency scaling disabled in the BIOS. We choose an evaluation system that is different from the one used for compilation to simulate a binary-only scenario. We run the applications five times each and record the median wall clock time before and after optimization. We also measure the dynamic instruction overhead of the optimized versions using a pintool [44]. The last column of Table 1 shows the dynamic instruction counts of the main computation in the original applications.

| Benchmark          | Input                                | Dynamic Instruction Count |
|--------------------|--------------------------------------|----------------------------|
| STLHistogram       | 100M array, 10M unique elements       | 7.9                        |
| PageRank           | web-Google.txt                       | 1.1                        |
| HashJoin           | 016M_build.tbl, 256M_probe.tbl        | 55.8                       |
| Graph500CSR        | -s 18 -e 10                          | 11.2                       |
| Cuckoo             | 8M flows                             | 10.2                       |

TABLE 1: Benchmarks and inputs (Input 1).

5.2 Results and Discussion

5.2.1 Results of Profiling and Analysis

First, we present the results of the control and dataflow analyses for the applications.

| Benchmark          | DILs | Prefetchable DILs | Loops | Function Name          |
|--------------------|------|-------------------|-------|------------------------|
| STLHistogram       | 4    | 3                 | 1     | gen_histo              |
| PageRank           | 4    | 4                 | 2     | pagerank               |
| HashJoin           | 2    | 2                 | 1     | realprobeCursor        |
| Graph500CSR        | 6    | 6                 | 2     | make_bfs_tree          |
| Cuckoo             | 3    | 2                 | 1     | rte_hash_lookup        |

TABLE 2: Results of control and dataflow analyses.

The data in Table 2 shows that of the 19 total DILs, 17 are prefetchable. We proceed with the performance evaluation of the prefetchers for these DILs.

5.2.2 Prefetcher Performance

For the five applications, we vary the prefetch distance from two iterations to 256 iterations in powers of two. Note that we
choose powers of two for only a minor convenience in code generation since multiplication can be replaced with shifts; it is not a fundamental restriction in our approach and can easily be changed to accommodate any arbitrary lookahead. We then verify that the outputs of the optimized binaries match with the original ones and then measure the performance of the optimized versions. The speedup from the performance optimization is shown in Figure 7a. The corresponding dynamic instruction overhead is shown in Figure 7b. The x-axis on both the figures is the prefetch distance, which is the number of iterations of lookahead available for the prefetcher. On the y-axis in Figure 7a is the ratio of the median wall clock time before optimization to that after. Figure 7b plots on its y-axis the ratio of the total dynamic instructions of the baseline to that of the the optimized executions. Note that the speedups reported include dynamic instruction overhead since we measure wall clock time.

For the applications and inputs described in Table 1, there is a significant speedup of 21-94% due to our software prefetchers. This speedup is in spite of significant dynamic instruction overhead in some cases. Hence, this result clearly demonstrates that we are successful in accurately prefetching the critical load addresses in a manner that does not interfere with the memory bandwidth or with any hardware prefetchers.

A pattern to observe in the data is that even with only a few iterations of the prefetch distance lookahead, the performance increases significantly. In fact, except for PageRank and Cuckoo, the performance improvement is stable across the entire range of prefetch distances. This is because the loop sizes are such that only a few iterations fit in the dynamic instruction window of the CPU. Hence, even with a small lookahead, the prefetcher reaches outside the instruction window to be effective. However, the behavior of PageRank and Cuckoo deserve further explanation.

PageRank operates on the Web-Google graph dataset [40], which has an average degree of less than six. The inner loop encompassing the prefetchable DIL iterates over all the neighbors of a graph node. Hence, the trip count of this loop is equal to the average number of a node’s neighbor or its average degree. Therefore, prefetch distances longer than six skip the loop fully and do not help much. This behavior can also be seen in Figure 7b in the dynamic instruction overhead data. A similar behavior occurs in Cuckoo as well, where the prefetchable DILs are from an inner loop with a fixed iteration count of 32. The lost opportunity cost due to small iteration counts is the reason for the reduction in performance with increasing lookahead.

Note that the performance gains for STLHistogram and HashJoin are much higher than those for the remaining three. In the former two, the critical DIL is fed by a strided load after passing through a hash function and multiple indirections. However, in the latter three, the strided load feeds the DIL directly through fewer indirections (and a hash function in Cuckoo). Thus, as discussed in Sections 3 and 4, the bottleneck of the chain of dependent cache misses is much larger for the former applications than the latter. Consequently, the performance boost obtained by mitigating them is also higher.

5.2.2.1 Impact of Inputs: Next, we select a set of larger inputs for our applications and run the optimized binaries on this set to study sensitivity to different application inputs. Table 3 lists the new inputs used for this experiment.

| Benchmark   | Input                        | Dynamic Instr (B) |
|-------------|------------------------------|------------------|
| STLHistogram| 200M array, 10M unique elements | 12.7             |
| PageRank    | cit-Patents.txt [39]         | 4.2              |
| HashJoin    | 032M_build.tbl, 512M_probe.tbl | 148.2            |
| Graph500CSR | -s 21 -e 10                  | 90.7             |
| Cuckoo      | 16M flows                    | 20.5             |

TABLE 3: Alternative inputs for the optimized benchmarks (Input 2).

Figure 8 displays the speedup and the dynamic instruction overhead for the optimized binaries running on these new inputs. We can see that the speedup has improved for STLHistogram, stayed about the same for HashJoin/Cuckoo and decreased for PageRank and Graph500CSR. Overall, the speedups range from 10%-100% and are still significant over the baselines. For PageRank, the cit-Patents dataset [39] has an average degree of 4.4 which is less than
the previous Web-Google dataset. Thus, as discussed earlier, the drop in its speedup can be attributed to the reduced trip count of its inner loop. As for Graph500CSR, the new input has a higher number of vertices but the same average degree as before and the performance contribution of the DILs is lower than before. Hence, the corresponding speedup by prefetching them is also lower.

5.2.2.2 Impact of Microarchitecture: The results shown so far were for a single microarchitecture. To study the impact of a different microarchitecture, we generate traces from the unoptimized and optimized binaries and perform cycle accurate simulations on them for an aggressive hypothetical microarchitecture that is 2X wider and 3.5X deeper than Skylake. We also model two aggressive hardware prefetchers similar to VLDP [63] and IMP [72] since they were published after the release of the Skylake microarchitecture. Figure 9 shows the result of the experiment. Unlike Skylake, the dynamic instruction window of the hypothetical microarchitecture can hold many more iterations of the loops. Hence, short prefetch distances do not go beyond the instruction window. This is why the speedups are lower for shorter lookaheads (for the benchmarks without small loop iteration counts). However, once the prefetch distances are sufficient to look beyond the instruction window, the speedups stabilize afterwards. The extra latency hiding offered by the 3X increase in out-of-order depth causes the DILs from Pagerank to not be the bottlenecks of performance anymore. Hence, the instruction overhead for the benchmark shows up as a slowdown in the chart. Nevertheless, the speedups continue to be significant overall (the bar for STLHistogram is missing for the prefetch distance of 128 due to simulation failure).

The stability of speedups across prefetch distances beyond a particular threshold is helpful in case of variable DRAM latencies. Setting the lookahead for the worst-case memory latency can provide speedups that are robust to the variability. Moreover, the fact that the speedups remain significant even under contemporary aggressive hardware prefetchers, emphasizes that our approach is complementary to hardware and minimizes interference.

5.2.2.3 Comparison with Helper Threads: We now compare the inline prefetcher to traditional helper threads. To provide the techniques with equal hardware, we restrict the helper thread implementations to one additional SMT context from the same core as the main thread. We also select the best tuning parameters (prefetch distance for the inline prefetcher and launch trigger/frequency for helper threads) for both the schemes. Figure 10 shows the results of the experiment.

Our inline prefetcher outperforms helper threads due to the latter’s thread spawning overhead. Dropping the outlier (Cuckoo), the speedups range from 13-83%, which is significant. For Cuckoo, the number of thread spawns is prohibitive for helper threading to be competitive. From the results of these experiments, we conclude that the proposed prefetcher scheme is accurate in targeting the critical load instructions and improves single thread performance of the targeted applications significantly. It does so without the requirements of traditional helper threading such as idle thread contexts and special support from hardware or firmware.

5.2.3 Limitations and Future Work
As a binary modification technique, debuggability can be affected due to optimization. Hence, it is a good idea to restrict optimization
only to performance critical code.

As a prefetching scheme running on the CPU, we drop all the pointer chasing loads from the purview of our optimization. Such a restriction is not essential. The backward slices and cycles with chasing loads are ideal for offload into Processing-In-Memory (PIM). Future work could explore means of implementing such offloading. Also, we have restricted ourselves to software implementation on existing hardware, which is not mandatory. The profile-based, offline dataflow analysis could advice hardware-software co-design and prefetchers could be implemented in custom hardware instead. With the advent of Field Programmable Gate Arrays (FPGA), custom hardware prefachers closely coupled with a processors pipeline are another potential direction of investigation.

6 Conclusion

In this paper, we have described an inline software prefetcher for DRAM-bound Delinquent Irregular Loads (DILs). In order to avoid interfering with the hardware prefachers for regular loads and to keep the bandwidth impact and cache pollution to a minimum, we have designed the scheme to be highly selective in targeting only the DILs most difficult for the hardware to prefetch. In spite of being selective, our approach has a significant potential for performance enhancement as demonstrated by four applications from different domains: a C++ hash table implementation, the PageRank website ranking algorithm, a database join algorithm and the Graph500 breadth-first search of a large graph. Across all inputs to the test applications, speedup due to our inline prefachers ranged from 10% to 100% on a high-end Intel Skylake system.

Our approach performs better than a traditional implementation of helper threads due to the latter’s thread spawning overhead. It does so while still not requiring separate thread contexts or special hardware/firmware support. It makes the implementation and debugging of the helper easier since it avoids explicit synchronization and stays a constant number of iterations ahead of the main computation. As a software approach that does not require high level source code, it can be attractive for third party cloud applications.

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