Multi-chip assemblies combining wire bond and flip-chip package technologies

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Abstract. The paper considers technological solutions for the production of multi-chip package-on-package assemblies. To evaluate the capabilities of the manufacturer product line the PoP prototype samples were produced. The results of qualification tests of PoP prototype samples are presented. Conclusions have been drawn on the applicability of systems in package, combining the installation technologies of Wire Bond and Flip-Chip crystals.

1. Introduction

The ongoing development of portable communication devices, cell phones and the Internet of Things has required the electronics industry to encapsulate microcircuits in compact packages. At the same time, the growth of technology requires complicating and increasing the productivity of microelectronic components. This logically led to development of multi-chip integration technologies and production of microassemblies that contain several heterogeneous chips in a common package. These chips can act together as a full-fledged computing module or graphic processor [1].

One of these technologies is a system on a chip (system-on-chip, SOC) – an electronic integrated circuit that performs the functions of an entire device. SOC consume less energy, are cheaper, and operate more reliably than chipsets with the same functionality. The reduced number of chips simplify further manufacturing processes. However, designing and debugging one large and complex system on a chip is more expensive than a series of small ones.

An alternative packing technology is the System-in-Package (SiP). There are four main categories of SiP, representing two-dimensional (2D) and three-dimensional (3D) packaging of semiconductor components:

- stacking of two or more functional dies on top of each other with a base in the form of a leadframe or printed circuit board. This type of packaging is used in the production of semiconductor memory devices [2];
- stacking of pre-packaged integrated circuits on the top of each other – the “package-on-package” technology (PoP) [3]. If chip contains other packaged integrated circuits, then such a method is called Package-in-Package (PiP);
- modules based on Low Temperature Cofired Ceramic (LTCC) and printed circuit boards combining one or more dies and integrated and/or discrete passive components in BGA or LGA package. This technology is widely used for high-frequency electronics, such as wireless signal transceivers, amplifiers and antenna modules [4];
• multi-chip 3D modules (Multi-Chip Modules - MCM 3D), containing several dies and optionally passive components located on the same substrate, as well as microcircuits mounted on top of each other. Typical application includes various modern sensors combining a sensitive element with a data processing unit, or processors for portable devices [5].

Among the technologies used in SiP for mounting dies and creating electrical connections both Flip-Chip and Wire Bond technologies are generally accepted. In case of Wire bond the crystal is attached to a substrate using glue or film adhesive (Die Attach Film, DAF) and connected to the contact pads on the substrate using microwelding. In case of Flip Chip the crystal is flipped over so that its top side faces down. The ball contacts (bumps) on top side of the crystal are soldered to the contact pads of the substrate.

The use of SiP technology allows [6] increasing the number of functional elements in a volume unit and reducing energy consumption of devices. In terms of production, the use of SiP reduces time to market and the cost of projects. Modern computer-aided design systems such as Cadence® make it possible to carry out unified design of the system-in-package, as the CAD packaging tools support both Flip-Chip and Wire Bond technologies.

The paper considers technological solutions applied for the production of PoP multi-chip microcircuits. To evaluate the capabilities of the manufacturer product line the PoP experimental samples were produced and tested.

2. Experimental samples
The experimental samples were produced with the aim of evaluating the current SiP assembly technological process for the capability of PoP multi-chip packaging with both Flip Chip and Wire Bond crystals in one package. The PoP experimental samples made in the form of complete devices suitable for electrical and functional testing.

The reference design of PoP experimental samples was developed using Cadence SIP Layout computer-aided design system. This system allows tracing substrates with a large (over 16) number of metallization layers. The design documentation was developed in accordance with ESKD standards.

The PoP experimental sample consist of two stacked substrates and contains two W25Q128JVWI NOR Flash memory crystals and one FC150JY dummy chip. The substrates are interconnected by soldering the ball leads on the lower side of the upper substrate to the corresponding contact pads on the upper side of the lower substrate.

Flash memory crystals are mounted on the upper substrate using Wire Bond technology and electrically connected to the ball leads on the lower side of the lower substrate. The FC150JY chip is mounted on the lower substrate using Flip Chip technology. Bridges located on the lower substrate and in the dummy chip are connected into daisy chains. These daisy chains are used to perform electrical testing and solder joint reliability verification.

3. Technological manufacturing cycle
The technological cycle of manufacturing PoP experimental samples is of interest due to its complexity. The raw materials for the manufacture of samples are substrates, crystals, solder balls, gold wire, adhesives, compounds, and other auxiliary materials.

Chip substrates are made in the form of strips. One strip contains 36 upper substrates (12 rows of 3 modules) or 20 lower substrates (10 rows of 2 modules). To prevent oxidation and electrostatic damage the substrates are transported in hermetically sealed antistatic bags and stored in nitrogen cabinets. At the pre-assembly stage the substrates are dried for 8 hours at a temperature of 120° C. Then visual inspection and warpage measurement of substrates are carried out.

The crystals come to pre-assembly in the form of wafers with a diameter of 200 and 300 mm. To achieve the required overall height of the product, grinding of the wafers on the non-working side is performed. Then the wafers are cut into dies. A wafers with cut dies remaining on the film is mounted in a metal frame for further operations.
The dies are mounted on substrates using the Besi Datacon 2200 evo. Before mounting the dies, the substrates are cleaned with hydrogen and oxygen plasma. For these purposes, the Nordson March AP1000 system is used.

NOR flash dies are mounted on the upper substrate. Installation is carried out in two stages. First, using a dispenser the die mounting seat is coated with the adhesive, and then the die is transferred from the wafer to the substrate. The adhesive is cured in an oven, and then the substrates are cleaned with plasma.

The electrical connections between flash memory dies and the upper substrate are performed by a 20 μm gold wire using ultrasonic thermocompression bonding on a Shinkawa UTC-2000 wire bonder. One strip of the upper substrates with memory crystals mounted is presented in figure 1-a. An enlarged photograph of memory crystals with completed wire bonding is presented in figure 1-b.

![Figure 1. A strip with the upper substrates of the PoP experimental samples (a) and an enlarged snapshot of one unit with two memory crystals mounted and connected to substrate (b).](image)

At the next stage the upper substrates are sealed by filling it with a mold compound using the Fico AMS i306 molding system. The encapsulated strips are baked at 185°C for 5 hours. Then the strips are divided into separate upper units using the DFD6340 dicing saw. The split units are shown in figure 2-a.

Using a solder paste and a stencil the solder balls are attached to their contact pads on the lower side of upper microcircuit units. Then the reflow process in Rehm V8 nitrogen oven is performed.

![Figure 2. Left: lower side of the upper substrates (a), strip of the lower substrates with the crystals installed (b) and with the upper microcircuits installed (c). Right: developed chip testing device (d).](image)
Nordson Dage XD7500VR X-ray inspection system. The reflow process is carried out in a Rehm V8 nitrogen oven with the recommended thermal profile. After that an X-ray inspection of the position of the crystals is repeated. Then flux residues are washed from the surface of the substrate.

Due to the presence of ball leads there are cavities between the Flip-chip and the substrate. To increase the reliability and achieve better distribution of the mechanical load, these cavities are filled with a special underfill compound. To do this, on the Besi Datacon 2200 evo setup, the underfill is dispensed along two adjacent sides of each crystal. Because of capillary effect, the underfill distributes itself under the crystal and fills all cavities. Then the underfill is baked at 185°C for 10 minutes. The cavity filling is examined using the Sonoscan CSAM D9500 digital scanning acoustic microscope. After that, the lower substrates are ready for mounting the upper package (figure 2-b).

Before assembling the upper and lower microcircuits into the PoP samples, functional testing of the memory chips of the upper package is performed. For this purpose, a developed testing device for hybrid multi-chip integrated circuits [7], shown in Figure 2-d, is used. This device has a socket for the 17x17 mm BGA package and allows electrical and functional testing of various microcircuits due to the flexible configuration of the socket input/output map.

The upper packages passed the testing are mounted on the lower substrate using the Besi Datacon 2200 evo system. The mounting procedure is similar to Flip Chip die attach process, followed by next operations: (1) ball leads reflow soldering, (2) X-ray control of interconnections between the ball leads of the upper microcircuit and the contact pads of the lower microcircuit, (3) filling the space between the upper and the lower substrates with underfill. The result of the above operations is shown in figure 2-c. After connecting the microcircuits, the strip with lower substrates is divided into separate units, and the ball leads are soldered to each unit.

The experimental samples pass electrical and functional testing. For this, a corresponding input/output map and test scenario for the testing device are used. Then the samples passed the testing are marked and packed in antistatic trays.

4. Results and discussion
One of the problems when creating systems in package using the PoP method is the warpage of the upper substrate during the ball reflow. The curvature of the contact plane of the substrates can interfere with the normal reflow soldering of contacts between them. Therefore, achieving a low level of warpage was one of the important parameters [8]. To achieve the necessary rigidity and stability for the upper integrated circuit, a substrate with a core of 150 μm made of HL832NX-A composite material with high heat resistance and a low coefficient of thermal expansion was used.

![Figure 3](image_url) A defects-free sealed upper substrate strip after the molding process: a general view (a), a fragment of an X-ray (b), the result of ultrasonic inspection of cavities in the mold (c).

In addition to warpage and the absence of cosmetic defects on the cured molding compound surface (figure 3-a), the integrity of the wire connections of the Wire Bond crystals inside the compound was controlled by X-ray inspection (figure 3-b). Also the homogeneity of the structure and the absence of
cavities in the mold compound were analyzed using scanning acoustic microscopy. Figure 3c shows the result of such an ultrasound study of an upper microcircuit strip. There are no cavities in the compound. In the lower part in the middle visible light traces of the flows that are permissible by the process, corresponding. The visible traces in the middle of the image correspond to the flows of the compound during molding process and are permissible by the process.

To avoid cavities in the compound and to prevent breaks of the wired connections of the memory crystals, the profile of the feed rate of the compound was modified. The experimentally obtained dependence of the feed rate of the compound on the position of the molding machine plunger is shown in figure 4. Due to the faster supply of the compound at the beginning and at the end of the process, the overall molding time is reduced. Due to the slower supply of the compound in the middle of the process, the load on the wire connections is reduced during the passage of the free boundary of the mold compound through the crystals.

For research trials 100 experimental samples, shown in figure 5, were manufactured using PoP technology. Then the electrical testing for open-circuit and short-circuit faults of signal lines and functional testing of memory chips were performed for all experimental samples. The open-circuit and short-circuit faults detected in 12 samples, and 8 samples did not pass functional testing. The total number of successfully tests passed samples was 82 out of 100 (82%).

5. Conclusion

As a result of the work, the production process of multi-chip integrated circuits using PoP method, combining Flip-Chip and Wire Bond package technologies was implemented, and 100 experimental samples were made and tested.

Based on the experience gained, the following conclusions can be drawn.

The advantages of PoP technology are a proven technological process and high assembly reliability due to the use of substrates that are simpler than the substrates used in the case of a planar SiP. The type of surface material of substrates can be selected specifically for mounting Flip-Chip or Wire Bond crystals. However, PoP technology has disadvantages such as a height of the chip. The heat dissipation
of crystals placed on the lower substrate is also limited in comparison with the planar SiP, and the crystals on the upper substrate have additional heating. Using larger diameter solder balls to connect the substrates results in a large pitch of the contact pads and occupies a large area on the substrate. This drawback is eliminated in a later package-on-package technology with the formation of through mold vias (PoP-TMV).

The use of crystals manufactured abroad as components for the production of SiP developed and manufactured in Russia increases the safety from the point of view of the product consumer. Dependence on foreign suppliers is reduced due to the possibility of acquiring crystals from different manufacturers, including domestic ones.

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References
[1] Yoon S W, Petrov B and Liu K 2015 Advanced wafer level technology: Enabling innovations in mobile, IoT and wearable electronics IEEE 17th Electronics Packaging and Technology Conf. (Orlando:IEEE) pp 1-5
[2] Yoon J H and Tressler G A 2012 Advanced flash technology status, scaling trends and implications to enterprise SSD technology enablement Flash Memory Summit 3(3.1) 4
[3] Lau J H 2019 Heterogeneous integration of PoP Heterogeneous Integrations pp 205-19
[4] Shamim A and Zhang H 2020 Antenna-in-package designs in multilayered low-temperature co-fired ceramic platforms Antenna-in-Package Technology and Applications pp 147-78
[5] OSD335x-SM smallest footprint, quickest design Retrieved from: https://octavosystems.com/octavo_products/osd335x-sm/
[6] Leung L L W, Sham M L, Ma W, Chen Y C, Lin J R and Chung T 2006 System-in-package (SiP) design: issues, approaches and solutions 2006 Int. Conf. on Electronic Materials and Packaging (IEEE) pp 1-5
[7] Kirienko D A, Ershova N Yu, Putrolaynen V V, Lunkov P V and Marcinkevich K R 2020 Electrical testing of small-series multi-chip microcircuit samples combining Wire Bond and Flip Chip technologies Int. Conf. Metrological Support of Innovative Technologies (Saint Petersburg, Krasnoyarsk) ICMSIT-1077
[8] Appelt B K 2017 Advanced substrates: a Materials and Processing Perspective Materials for Advanced Packaging pp 287-29