Layout-aware Soft Error Rate Estimation Technique for Integrated Circuits under the Environment with Energetic Charged Particles

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Abstract. Single Event Transient (SET) is a current and voltage disturbance in an integrated circuit (IC), caused by charged particle impact. In modern IC technologies single charged particle can cause multiple SETs on multiple electrical nodes, this can lead to faults. There are several mitigation techniques with their drawbacks affecting circuit performance. This work presents a comparison of experimental data with simulation results acquired by the means of our technique and tools. Our technique is able to simulate sub-100 nm IC performance under multiple SET using industry standard SPICE simulator, without incorporation of a T-CAD or physical measurements, and taking into account layout of the device.

1. Introduction
Space radiation coming from the sun and other galactic sources consists of charged particles of various types. A charged particle hits an integral circuit (IC) produce the electrical disturbance called single event transient (SET). SET is able to transform to a single event upset (SEU). In sub -100 technologies, single particle can hit multiple devices simultaneously, producing multiple SETs and multiple SEUs. The effects of multiple SETs are hard to predict, there are some works about more than 10 simultaneous upsets in sub-100 nm memory units [1], [2]. There are some tools that help designers of the space electronics to develop mitigation techniques. Most of them incorporate T-CAD data from physical measurements. Monte-Carlo simulations with wide use of T-CAD data are implemented in MUSCA SEP [3] and MRED [4] software. This software needs the appropriate competence from designer and additional data from T-CAD or physical measurements of the device. In [5] we presented the simulation technique that uses device layout information to perform SPICE simulations of multiple SET. The developed technique uses only foundry technology documentation and models files.
2. Technique description

The idea of the technique is to perform SPICE simulation of the circuit with instances of Verilog-A SET model. SET model is connected to the devices affected by a charged particle impact. SET model is a well known “double exponential current source” [6] written in Verilog-A hardware description language. SET model input parameters are deposited charge, start time, technology specific rise and fall time constants.

The first thing is to extract the SPICE netlist from the layout, then compare and equate nets and instances of the original and extracted netlists. As coordinates of the extracted devices and symmetric source devices are known, it is possible to apply charged particle impact to the circuit and detect affected devices and calculate their portions of deposited charge. This is a full set of required data to perform a simulation of the circuit SET performance and detect the upset. Detailed description of the developed technique can be found in [5].

It is possible to plot simulated upsets cross-section (CS) distribution and to compare it with experimental CS data. To calculate simulated CS distribution it is essential to gather for each LET point the following set of data: number of simulations, number of upsets and area of the device. Equation for simulated CS for each LET and energy point is (1), where \( N \) – a number of the conducted simulations, \( S \) – area of the device and \( N_{ci} \) – number of the detected upsets.

\[
\sigma_i = \frac{N_{ci}}{N / S}
\]

A sequence of the \( \sigma_i \) distributed over LET values can be directly compared to the similar experimental distribution.

3. Experiment and simulation description

The experiment was concerned in majority voters [7] SET immunity. 5 voter types were tested. Test system is displayed in Figure 1, it consists of an array of the certain type of majority voters, SET detector and output circuit. Set detector is a D-Flip-Flop with reset, "D" input is tied to "1" and the majority voter connected to the "C" input. Before the irradiation, a "Reset" signal was applied to the SET Detector, forcing its output "Q" to "0". If any of the voters suffered enough impact by the ion, it produced SET to the "C" input of the DFFR, turning its output to the "1" state, this meant SET detection. Test system was designed for 65 nm TSMC bulk CMOS technology and irradiated by ions of different energies. Ions parameters are described in Table 1, SET effects studied at room temperature; the fluence was varied from \( 8.5 \times 10^5 \) cm\(^{-2}\) to \( 1.6 \times 10^7 \) cm\(^{-2}\). The detailed description of the experiment can be found in [8].
Table 1. Heavy ion beams parameters.

| Ion  | Energy (MeV) | Effective LET (MeV·cm²/mg) |
|------|--------------|-----------------------------|
| $^{22}$Ne | 81           | 7                           |
| $^{40}$Ar   | 146          | 18                          |
| $^{84}$Kr   | 269          | 41                          |
| $^{136}$Xe  | 435          | 60                          |

Simulation system directly repeats the test system and consists of a majority voter and DFFR based SET detector. Simulation procedure repeats experimental procedure: reset detector, apply impact, detect upset, gather and process data.

4. Results and discussion
The results of the simulations are sensitivity maps and the cross-section plots. Cross-section values are plotted against LET values on the Figure 2. simulated cross-section plots are combined with experimental cross-section plots. Five types of voters were tested: ACOMP, 12TI, MUX, AWB and NAND, detailed description of the voters is in [8]. Simulation results for the ACOMP voter are on the Figure 2 (a), 12TI on the Figure 2 (b), MUX on the Figure 2 (c). Figures 2 (a) – 2 (c) show a good agreement with the experimental data. The diversion on the figure 2 (c) at 40 LET point is due to lack of experimental statistics.

AWB voter on the figure 2 (d) shows relatively poor agreement. There is the type of SET the effect that cannot be simulated by the developed tools at current point. Simulation of AWB voter shows immunity for transistors, situated in n-well (p-MOS) and deep n-well (n-MOS). The only vulnerable parts are the output buffers. At the layout point of view, n-well and deep n-well regions are surrounded by guard rings to tie them and prevent latch-up effect. The guard ring (n/p- doped area) surrounding well and substrate regions (p/n-doped areas) forms parasitic bipolar transistor with base tied to keep the parasitic transistor in “close” state. There are some works about danger of different parasitic bipolar transistor structures [1], [9], [10]. If particle hits the vicinity of the guard ring it overcomes guard ring potential and opens parasitic bipolar transistor, which injects charges directly to the nodes thought to be immune. The technique only does the distribution of charges among affected devices, this effect cannot be simulated.
Figure 2. Comparison of the simulation and the experiential cross-sections. Round markers are for simulation data, triangle markers are for experiential data, red markers for "0" inputs, blue markers are for "1" inputs. Corresponding types of the majority voters: a – ACOMP, b – 12TI, c – MUX, d – AWB, e – NAND [8].

Figure 2 (e) shows good agreement for the “0” inputs and moderate agreement for the “1” inputs. The reason is the simulation procedure and the structure of the voter output. NAND voter includes 3 stacked n-MOS transistors in the output NAND device. This n-MOS are closely situated: most of impacts affect all 3 transistors simultaneously. Simulation tool shares charge between the output n-MOS transistors. Two of three transistors in stack produces SET signal to the nodes in high-Z state and only one transistor produces SET to the output (1/3 of whole charge goes to the output). This is not accurate because whole charge should flow to the output through the topmost stacked n-MOS transistor via charge sharing through substrate. As p-MOS transistors in output NAND device are connected in parallel they simultaneously produce their portions of SET to the output.

5. SPICE SET model
As it was shown on Figure 2 (d) and (e), simulation approach with direct distribution of the deposited charge and SET simulation via current sources does not consider all effects that leads to the SEU. The new approach is in development. The idea is to simulate whole amount of deposited charge as capacitor charged to certain voltage. To simulate charge collection the charge should be delivered to the sensitive nodes through chain of resistors. The resistors represent substrate resistance. Additionally, the different types of the parasitic devices should be detected. This SET model can be
constructed from standard SPICE building blocks and simulated by standard SPICE simulation. Approximate values for SPICE parameters of parasitic devices can be found in technology documentation or through simulation of foundry elementary devices. Example of the SPICE SET model is displayed on the Figure 3.

![Figure 3](image)

**Figure 3.** The example of device connected with SPICE SET model.

Simulation of the AWB voter with the SPICE SET model shows a possibility to upset it with an impact of the charge equivalent to the charge deposited by a 40 MeV·cm²/mg LET particle.

6. **Conclusion**

The technique was tested on sub-100 nm designs and proved to be suited for estimation. The technique goal is to use only PDK data and documentation without incorporating T-CAD and physical measurements. Verilog-A model module can be modified to any model and to account additional parameters. Technique provides graphical representation: sensitivity maps that presents simulation data in illustrative form. Technique need revision in SET model part, proposed SPICE SET model will be suited for this purpose.

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