Novel High-Throughput Decoding Algorithms for Product and Staircase Codes based on Error-and-Erasure Decoding

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Abstract—Product codes (PCs) and staircase codes (SCCs) are conventionally decoded based on bounded distance decoding (BDD) of the component codes and iterating between row and column decoders. The performance of iterative BDD (iBDD) can be improved using soft-aided (hybrid) algorithms. Among these, iBDD with combined reliability (iBDD-CR) has been recently proposed for PCs, yielding sizeable performance gains at the expense of a minor increase in complexity compared to iBDD. In this paper, we first extend iBDD-CR to SCCs. We then propose two novel decoding algorithms for PCs and SCCs which improve upon iBDD-CR. The new algorithms use an extra decoding attempt based on error and erasure decoding of the component codes. The proposed algorithms require only the exchange of hard messages between component decoders, making them an attractive solution for ultra high-throughput fiber-optic systems. Simulation results show that our algorithms based on two decoding attempts achieve gains of up to 0.88 dB for both PCs and SCCs. This corresponds to a 33% optical reach enhancement over iBDD with bit-interleaved coded modulation using 256 quadrature amplitude modulation.

Index Terms—Bounded distance decoding, coded modulation, error and erasure decoding, forward error correction, hard-decision decoding, high-throughput fiber-optic communications, low-density parity-check codes, product codes, staircase codes.

I. INTRODUCTION

The transmission rate of a single optical fiber has increased by a factor of 8000 over the past 30 years [1]. Recently, a chipset with the capacity of 800 Gbit/s/λ has become commercially available [2]. To cope with the growth of applications such as cloud computing, internet-of-things, video-on-demand, etc., next-generation optical line cards target data rates of 1 Tbps/λ and beyond. Reliable transmission at such high data rates can not be achieved using off-the-shelf digital signal processing (DSP) nor by exclusively relying on the improvement of integrated circuits (due to the end of Moore’s law [3]). Forward error correction (FEC) is an essential component of the receiver DSP and must be adapted accordingly to cope with the current trends on data rate. Designing high-performance FEC decoders for ultra high-speeds is very challenging due to the strict latency and power constraints.

Product codes (PCs) [4] and staircase codes (SCCs) [5] are popular FECs for high-throughput applications such as fiber-optic systems and have been included in several recommendations (e.g., ITU-T G.709.2/Y.1331.2 [6] and 400ZR [7]). Soft-decision decoding (SDD) of PCs—also known as turbo product decoding (TPD)—was proposed already more than 20 years ago in [8]. TPD provides excellent performance at the cost of a high internal decoder data flow due to the iterative exchange of soft messages, which significantly limits the achievable throughput [9]. Further, such soft message passing entails high power consumption, e.g., 10 W for 128 Gbps line rate [10]. An alternative to TPD is to employ iterative hard-decision decoding (HDD). HDD requires much lower decoding complexity (e.g., 0.62 W for 317 Gbps information rate [11]), however, it entails large performance losses (1–2 dB depending on the code rate) compared to SDD.

Recently, several hybrid soft-decision decoding (SDD) and hard-decision decoding (HDD) architectures have been proposed for both PCs and SCCs, which provide a suitable performance-complexity tradeoff between SDD and HDD [12]–[17]. The unifying idea of these schemes is to employ HDD as the decoding core, while exploiting some level of soft information to improve the overall decoder performance. In [12] and [13], two decoding algorithms for PCs were proposed based on error-and-erasure decoding (EDD) [25]. In [14], a low-complexity decoding algorithm called iBDD with scaled reliability (SABM-SR) was presented for both PC and SCCs. SR models the reliability of the hard decisions of the BDD of the component codes by combining the hard decisions properly scaled by a scaling factor and the channel LLRs. In [15], the soft-aided bit-marking (SABM) decoder was proposed for PCs and SCCs based on flipping the least reliable bits and a heuristic miscorrection detection procedure. The performance of SABM was further improved for PCs based by combining SABM with the SR principle [16].

The employed code rate is not specified, hence, the corresponding information rate is unknown to the authors.

Other proposals for high-throughput coding schemes comprise the concatenation of an inner code with SDD and an outer code with HDD [18], LDPC codes with binary, ternary, and quaternary message passing [19]–[21], anchor decoding (AD) of PCs and SCCs based on tracking the conflicts between component decoders [22], and two-stage decoding based on multi-stage decoding and exploiting both SDD and HDD [23], [24].
The latest algorithm in the class of hybrid decoding architectures was introduced in [17], where iBDD with combined reliability (iBDD-CR) was presented. iBDD-CR improves iBDD-SC by performing the optimal combining (optimal for large block lengths and extrinsic iBDD) of the hard decisions and channel LLRs. This combining is found based on density evolution (DE) analysis of the generalized low-density parity-check (GLDPC) code ensemble encompassing PCs. Employing the iBDD-CR decoder for SCCs demands finding an accurate estimate of the reliability of the HDD outputs for SCCs, which is not necessarily the same as for PCs.

This paper extends [17] in two different directions. First, we extend iBDD-CR to SCCs. In particular, we perform a DE analysis for iBDD-CR based on the spatially-coupled GLDPC (SC-GLDPC) code ensemble that contains SCCs as particular instances. The derived DE provides an accurate estimate of the reliability of the hard decisions of the BDD of the SCC component codes, which is exploited in iBDD-CR. Second, we propose two novel decoding algorithms for PCs and SCCs that enhance the iBDD-CR architecture with EDD of the component codes. The proposed decoders can be efficiently implemented by only exchanging hard messages between component decoders. We perform an algorithmic-level complexity comparison between our proposed schemes and the decoders of [12]–[17], [22]. We show via simulations that the proposed schemes for both PCs and SCCs provide up to 0.88 dB gain compared to standard HDD based on iBDD of the component codes for a bit-interleaved coded modulation (BICM) scheme using 256 quadrature amplitude modulation (QAM). Such gains are predicted to yield up to 33% optical reach improvement compared to the original optical reach of iBDD for BICM with 256-QAM.

The remainder of the paper is organized as follows. In Section II, some preliminaries and the system model are explained, and the iBDD-CR algorithm is reviewed. The new hybrid decoding algorithm for PCs and SCCs is introduced in Sections III and IV, respectively. In Section V we explain the heuristics behind the proposed hybrid decoders and analyze their complexity. Conclusions are drawn in Section VI.

II. PRELIMINARIES

Product-like codes are a family of codes described by a two-dimensional array. In this paper, we consider binary PCs and SCCs. In the following, we briefly review the structure of PCs and SCCs and also explain the channel model considered in this paper. The last part of this section describes the recently introduced iBDD-CR algorithm.

Notation: Boldface letters stand for vectors and matrices, e.g., \(x\) and \(X = [x_{i,j}]\), with \(x_{i,j}\) representing the element corresponding to the \(i\)-th row and \(j\)-th column of \(X\). \(X_{i,:}\) denotes the \(i\)-th row of \(X\). A Gaussian distribution with mean \(\mu\) and variance \(\sigma^2\) is denoted by \(\mathcal{N}(\mu, \sigma^2)\). Functions and subscript texts are shown with serif font. \(T\) is the matrix transpose operation. \(|x|\) and \(|x|\) stand for the absolute value of \(x\) and the vector with components equal to the absolute value of the component of \(x\), resp.

While higher-dimensional product-like codes exist, the most conventional ones are two-dimensional.

A. Product and Staircase Codes

Let \(C\) be a Bose-Chaudhuri-Hocquenghem (BCH) code constructed over the Galois field \(GF(2^s)\) with error correction capability \(t\) and shortening parameter \(s\). The codeword length of \(C\) is \(n = 2^s - 1 - s\) and the number of its information bits is \(k = 2^s - vt - 1 - s\). A PC with \((n,k)\) component codes is defined as the set of all \(n \times n\) arrays \(C = [c_{i,j}]\) such that each row and column of \(C\) is a valid codeword of \(C\). The rate of such PC is \(R = k/n^2\). Fig. 1(a) shows the code array of a PC code with component code length \(n = 6\). The code bit corresponding to the second row and second column component codes, \(c_{2,2}\), is highlighted. PCs are conventionally decoded based on BDD of the component codes. BDD corrects all error patterns of Hamming weight up to \(t\). If the weight of the error pattern is larger than \(t\) and there exists another codeword with Hamming distance less than \(t\) to the received codeword, BDD introduces miscorrections. Otherwise, BDD fails, where conventionally it is considered that BDD outputs its input. We refer to iteratively applying BDD on row and column codes as iBDD.

A SCC comprises the set of all matrices \(B_i\) of size \(n/2 \times n/2\), \(i = 1, 2, \ldots\), such that each row of the matrix \([B_{i-1}, B_i]\) is a valid codeword in \(C\). Each matrix \(B_i\) contains \((n/2) \cdot (n-k)\) parity bits out of \(n^2/4\) code bits, hence, the corresponding code rate is \(R = 1 - 2(n-k)/n\). Fig. 1(b) shows an schematic of the SCC comprising the blocks \(B_{i-1}, B_i, B_{i+1}\), and \(c_{2,2}\) as a code bit corresponding to the second row and second column of \(B_i\). Note that \(B_0\) is an all-zero matrix which initializes the decoding procedure of the SCC. SCCs are decoded in a windowed-decoding fashion, i.e., each row of \([B_{i-1}, B_i]\) for staircase blocks within a decoding window is decoded based on BDD [5]. We also refer to iteratively applying BDD on the component codes of an SCC within the decoding window as iBDD.

B. System Model

We consider bit-interleaved coded modulation (BICM) based on M\(^2\)-QAM. In BICM, the code bits are interleaved and then mapped to the constellation points using the binary reflected Gray code (BRGC) mapping. The real and imaginary
part of an $M^2$-QAM symbol with $M = 2^m$ are both selected from the set $X \triangleq \{((-2^m+1)\Delta, \ldots, -\Delta, \Delta, \ldots, (2^m-1)\Delta)\}$, where $\Delta = \sqrt{3/2(M^2-1)}$ normalizes the constellation energy to unity. Due to the symmetry of the $M^2$-QAM constellation, we only consider transmission of the real part of the $M^2$-QAM symbol.

The AWGN channel output at time instant $i$ corresponding to transmitted symbol $x_i \in X$ is given by

$$y_i = x_i + n_i, \quad i = 1, 2, \ldots, n_{\text{ch}},$$

where $n_{\text{ch}}$ is the number of channel uses corresponding to a PC or SCC block, and $n_i \sim N(0, \sigma^2)$. The log likelihood ratio (LLR) of the $q$th bit level of $y_i$ is given as

$$l_{i,q}^q = \sum_{b \in \{0,1\}} (-1)^b \ln \sum_{a \in S_{i,q}^a} e^{-\frac{(y_i-a)^2}{2\sigma^2}}, \quad q = 1, 2, \ldots, m,$$

where $S_{i,q}^0 \subset X$ and $S_{i,q}^1 \subset X$ are sets of size $2^m$ symbols with 0 and 1 as the $q$th bit of the corresponding BRGC label, respectively. For the special case of the binary input AWGN (bi-AWGN) channel, $m = 1$, $\Delta = 1$, and $l_i = 2y_i/\sigma^2$.

C. iBDD with Combined Reliability

We briefly review the architecture of iBDD-CR [17], which is shown in Fig. 2.

Let us denote by $\Psi_i^{\ell}(\ell-1) = [\psi_{i,j}^{\ell}(\ell-1)]$ the decoding output of the $n$ column codes at iteration $\ell - 1$, i.e., $\psi_{i,j}^{\ell}(\ell-1)$ corresponds to the hard decision on code bit $c_{i,j}$. The input of the row decoder at iteration $\ell$ is $\Psi_i^{\ell}(\ell-1)$. In the following, we explain the decoding of the $i$th row code at iteration $\ell$, using the input $\Psi_i^{\ell}(\ell-1)$. We denote by $\tilde{\mu}_{i,j}^{\ell}$ the output of BDD of the $i$th row code corresponding to code bit $c_{i,j}$. In case of correct decoding or miscorrection, BDD outputs a codeword. This case $\tilde{\mu}_{i,j}^{\ell} = 0$.  \cite{footnote2}

The LLR on code bit $c_{i,j}$ after BDD at iteration $\ell$ is given as [17, Eq. (9)]

$$\hat{l}_{i,j}^{\ell} = \tilde{\mu}_{i,j}^{\ell} + l_{i,j},$$

where $l_{i,j}$ is the channel LLR and $\tilde{\mu}_{i,j}^{\ell}$ can be computed using a look-up table (LUT) based on $\mu_{i,j}^{\ell}$ (see [17, Theorem 1]). Then, a hard decision is made on $\hat{l}_{i,j}^{\ell}$,

$$\psi_{i,j}^{\ell}(\ell) = B \left( \hat{l}_{i,j}^{\ell} \right),$$

where $B(\cdot)$ is the mapping $-1 \mapsto +1$ and $+1 \mapsto -1$. After applying this procedure to all row codes, the matrix $\Psi_i^{\ell}(\ell) = [\psi_{i,j}^{\ell}(\ell)]$ is formed and used as the input for the $n$ column decoders. Column decoding is similar to the row counterpart. The decoding continues by iterating between row and column decoding for a given number of iterations. The additional component of iBDD-CR compared to iBDD is shown as “iBDD-CR core” in Fig. 2. As can be seen, the operations in the iBDD-CR core are based on soft values; however, only (binary) hard messages are exchanged between component decoders. Therefore, the contribution of the messages exchange between component decoders to the overall internal decoder data flow of iBDD-CR is the same as that of iBDD [17].

III. HYBRID DECODING OF PCs

In this section, we introduce a novel hybrid decoding algorithm for PCs, which we call binary message passing based on EDD (BEE), as an improved variant of our recently introduced iBDD-CR algorithm. BEE is then extended to SCCs in Section IV. We will refer to BEE for PCs and SCCs as BEE-PC and BEE-SCC, respectively.

A. Generalized Distance Metric

BEE exploits the so-called generalized distance (GD) metric, originally introduced in [25], in order to improve the performance of iBDD-CR. GD is defined as follows. Let $a = (a_1, a_2, \ldots, a_n)$ be a binary vector with reliability $l = (l_1, l_2, \ldots, l_n)$. The GD between $a$ and the binary vector $b = (b_1, b_2, \ldots, b_n)$ is

$$d_{\text{GD}}(a, b) \triangleq \sum_{i=1}^{n} (1 - \alpha_i) + \sum_{i=1}^{n} (1 + \alpha_i),$$

where $\alpha = (\alpha_1, \alpha_2, \ldots, \alpha_n)$ is the vector of normalized reliabilities, i.e., $\alpha_i \overset{\Delta}{=} |l_i|/ \max_{1 \leq j \leq n} |l_j|$. One can interpret the GD as a soft version of the Hamming distance. Indeed, assuming $\alpha_i = 1$ for $a_i = b_i$ and $\alpha_i = 0$ for $a_i \neq b_i$, $d_{\text{GD}}(a, b)$ corresponds to the Hamming distance between $a$ and $b$.

B. BEE-PC Algorithm

Fig. 3 shows the block diagram of the proposed BEE algorithm for PCs. Without loss of generality, we explain the BEE-PC decision corresponding to the decoding of the $i$th row of the PC at iteration $\ell$. BEE-PC encompasses two decoding attempts, each corresponding to a branch in Fig. 3. First, we explain the upper branch of Fig. 3. Let $\bar{M}_i^{\ell}(\ell-1)$ contain the BDD outcome of the $n$ column decoders at iteration $\ell - 1$ corresponding to the $i$th row of the PC codeword, with elements in $\{\pm 1, 0\}$. Similar to the iBDD-CR decoder (see (3)), using $\bar{M}_i^{\ell}(\ell-1)$, the channel LLRs $L_{i,:}$, and the iBDD-CR LUT, the LLLR $L_{i,j}^{\ell}(\ell-1)$ can be computed, on which a hard decision is made according to $\Psi_i^{\ell}(\ell-1) = B(L_{i,j}^{\ell}(\ell-1))$. Then, BDD is performed with input $\Psi_i^{\ell}(\ell-1)$, which yields $\bar{M}_i^{\ell}(\ell)$, with elements in $\{\pm 1, 0\}$. Using $\bar{M}_i^{\ell}(\ell)$, $L_{i,:}$, and
the iBDD-CR LUT, the LLR $\bar{L}^r_{i;\ell}$ is then computed and the candidate decision $\Psi^r_{i;\ell}$ is formed as $\Psi^r_{i;\ell} = \mathcal{B}(\bar{L}^r_{i;\ell})$. Finally, a score of the candidate decision $\Psi^r_{i;\ell}$, denoted by $\bar{d}$ is obtained as

$$
\bar{d} = \begin{cases} 
2n, & \text{if BDD fails} \\
\lfloor d_{\text{GD}} \left( \Psi^c_{i;\ell}, \Psi^c_{i;\ell-1} \right) \rfloor, & \text{otherwise}
\end{cases},
$$

(6)

where $2n$ is a constant discussed in Section V-A.

The second branch of Fig. 3 serves as another decoding attempt based on EED. The two least reliable bits of $\Psi^c_{i;\ell}$ are found based on $|L^c_{i;\ell-1}|$ and then erased. Then, algebraic EED [26, Sec. 6.6] is performed on $\Psi^c_{i;\ell-1}$. Let $\bar{M}^r_{i;\ell}$ be the outcome of EED with three possible values for its elements, i.e., $\{\pm 1\}$ in case of successful (but potentially erroneous) decoding with the mapping according to $0 \mapsto +1$ and $1 \mapsto -1$, and $0$ if EED fails. Similar to what explained for the first branch, a candidate decision is formed as $\bar{M}^r_{i;\ell} = \mathcal{B}(\bar{L}^r_{i;\ell})$, where the LLR vector $\bar{L}^r_{i;\ell}$ is computed using $\bar{M}^r_{i;\ell}$, $L_{i;\ell}$, and the iBDD-CR LUT. Finally, the score of candidate decision $\bar{M}^r_{i;\ell}$ is computed as

$$
\bar{d} = \begin{cases} 
2n, & \text{if EED fails} \\
\lfloor d_{\text{GD}} \left( \bar{M}^r_{i;\ell}, \Psi^c_{i;\ell-1} \right) \rfloor, & \text{otherwise}
\end{cases}.
$$

(7)

Finally, comparing $\bar{d}$ and $\hat{d}$, the candidate codeword with the minimum score is chosen as the BEE-PC decision and the corresponding BDD outcome is as the input for column decoding in the next iteration, i.e.,

$$
M^r_{i;\ell} = \begin{cases} 
\bar{M}^r_{i;\ell}, & \text{if } \bar{d} \leq \hat{d} \\
\hat{M}^r_{i;\ell}, & \text{if } \bar{d} > \hat{d}
\end{cases}.
$$

(8)

After decoding of all rows of the PC at iteration $\ell$, $M^r_{i;\ell}$ is utilized as the input to the column decoders. To initialize the algorithm, the channel LLRs are employed as the input LLRs of both BDD and EED blocks, i.e., $L^c(0) = L$. In the last iteration ($\ell_{\text{max}}$), the BEE-PC decoding output corresponds to the branch with lowest score, i.e., the decoding output is $\Psi^r_{i;\ell_{\text{max}}}$ if $\bar{d} \leq \hat{d}$ and $\Psi^r_{i;\ell_{\text{max}}}$ if $\bar{d} > \hat{d}$.

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**C. Numerical Results**

We evaluate the performance of BEE-PC. Throughout this paper, we consider an extended BCH (eBCH) code, $C_1$, and BCH codes $C_2$ and $C_3$ as component codes. The corresponding parameters, PC and SCC rates, and hard decision (HD) and soft decision (SD) Shannon limits are given in Table I.\(^6\) We consider 10 iterations of BEE-PC appended with 2 iBDD iterations. The decision rule (4) is unable to correct errors with high reliability (code bits in error with high $|l_{i,j}|$). This is because $\mathcal{B}(\hat{r}_{i,j}) = \mathcal{B}(l_{i,j})$, i.e., the decision on a code bit is overridden by the channel error. Therefore, the appended iBDD iterations (which disregard reliabilities in the decision rule) help the decoder to correct errors with high reliability (see [14, Sec. VII]). For the sake of fairness, we evaluate all other algorithms with a total of 12 iterations.

In Fig. 4, we show the bit error rate (BER) performance of BEE-PC for a PC with component code $C_1$ and transmission over the bi-AWGN channel. For the sake of comparison, we also depict the performance of iBDD, AD [22], iBDD-SR [14], SABM-SR [16], and BEE-PC with TPD.\(^6\)

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\(^6\)These component codes are also considered for performance evaluation of the hybrid decoding schemes in [12]–[17], [22].
Table I

| Component code | Component parameters | PC code rate | HD Shannon limit at PC code rate | SD Shannon limit at PC code rate | SCC code rate | HD Shannon limit at SCC code rate | SD Shannon limit at SCC code rate |
|----------------|----------------------|--------------|----------------------------------|----------------------------------|--------------|----------------------------------|----------------------------------|
| $C_1$          | (256, 239, 2)        | 0.933        | 4.05 (dB)                        | 2.64 (dB)                        | 0.867        | 3.99 (dB)                        | 2.74 (dB)                        |
| $C_2$          | (255, 231, 3)        | 0.905        | 3.54 (dB)                        | 2.23 (dB)                        | 0.811        | 3.46 (dB)                        | 2.14 (dB)                        |
| $C_3$          | (511, 484, 3)        | 0.947        | 4.36 (dB)                        | 3.15 (dB)                        | 0.894        | 4.32 (dB)                        | 3.11 (dB)                        |

Fig. 5. Performance of iBDD, ideal iBDD, iBDD-SR, iBDD-CR, and BEE-PC for PC with component code $C_2$ in the BICM with (a) 4-QAM, (b) 16-QAM, (c) 64-QAM, and (d) 256-QAM modulation. (e) The optical reach improvement of BEE-PC over iBDD as well as the original optical reach of iBDD, corresponding to (a)-(d).

SABM [15], iBDD-CR [17], iGMDD-SR [12], and SABM-SR [16]. We also plot the performance of ideal iBDD which disregards miscorrections using a genie approach, TPD based on the Chase-Pyndiah algorithm [8], and the HD and SD Shannon limits. We highlight that iBDD and AD should be compared to the HD capacity. However, all other algorithms should be compared to the SD capacity, as they all exploit channel LLRs in the decoding rule. As it can be seen, BEE-PC outperforms all other algorithms. The performance gain of BEE-PC over conventional iBDD is 0.68 dB. Remarably, the gap between BEE-PC and TPD is only 0.43 dB. Therefore, BEE-PC can close 62% of the gap between (full hard) iBDD and (full soft) TPD. We highlight that the performance of iGMDD-SR, SABM-SR, and BMP-GMDD is close to that of BEE-PC. However, BMP-GMDD requires up to 30% more message exchanging between component decoders than BEE-PC, and both iGMDD-SR and SABM-SR require exchanging soft messages between component decoders, which yields significantly higher decoder data flow than BEE-PC (see Section V-B for a high level complexity discussion of the different algorithms).

In Figs. 5(a)-(d), the performance of iBDD, ideal iBDD, iBDD-SR, iBDD-CR, and BEE-PC for a PC with component code $C_2$ are shown for a BICM system (employing random interleaver) with 4-QAM, 16-QAM, 64-QAM, and 256-QAM, respectively. As can be seen, BEE-PC outperforms all other
The channel spacing used in computing the optical reach is:

| Symbol rate: 32 Gbaud | Channel spacing: 32 GHz |
|------------------------|-------------------------|
| No. of Channels: 5     | Roll-off-factor: 0      |
| \( \gamma = 1.3 \) W/km | \( D = 17 \) ps/nm/km  |
| \( \alpha = 0.2 \) dB/km | \( \lambda = 1550 \) nm |
| EDFA noise figure: 4.5 dB | Span length: 80 km |

### IV. Hybrid Decoding of SCCs

In this section, we extend iBDD-CR to SCCs by analyzing the decoding behavior using DE for the SC-GLDPC code ensemble, as the ensemble encompassing SCCs. Then, we propose a novel decoding algorithm for SCCs, similar in spirit to BEE-PC, which improves upon iBDD-CR.

#### A. iBDD-CR decoding of SCCs

Without loss of generality, we assume that \( B_{i-1} \) and \( B_i \) are within the decoding window and we explain the decision of iBDD-CR at iteration \( \ell \) corresponding to \( c^{(i)}_{j,p} \), which is located in \( B_i \), and also in the \( j \)-th row of \( [B_{i-1}^T, B_i] \). Let us assume that \( \Psi^{(i), \ell} = [\psi^{(i), \ell}_{j,p}], j = 1, 2, \ldots, \pi, p = 1, 2, \ldots, n \) contains the hard decision inputs of iBDD-CR corresponding to \( [B_{i-1}^T, B_i] \), and \( l^{(i), \ell} = [l^{(i), \ell}_{j,p}] \) is the corresponding channel LLRs.

We denote by \( \hat{r}^{(i), \ell}_{j,p} \in \{ \pm 1, 0 \} \) the output of BDD on the \( j \)-th row of \( \Psi^{(i), \ell} \), i.e., \( \hat{r}^{(i), \ell}_{j,p} \), corresponding to code bit \( c^{(i)}_{j,p} \). Furthermore, let \( \tilde{l}^{(i), \ell}_{j,p} \) be the LLR of code bit \( c^{(i)}_{j,p} \) after BDD at decoding iteration \( \ell \). The hard decision on code bit \( c^{(i)}_{j,p} \) produced by the \( j \)-th row decoder is formed as

\[
\psi^{(i), \ell}_{j,p} = B \left( \tilde{l}^{(i), \ell}_{j,p} \right).
\]

After updating \( \Psi^{(i), \ell} \), \( \Psi^{(i+1), \ell} \) is used as the input to the iBDD-CR decoder, which decodes each row of \( [B_i^T, B_{i+1}] \).

This procedure continues until all blocks within the decoding window are decoded for a given number of iterations.

In Fig. 6, a schematic of the iBDD-CR decision for the code bit \( c^{(i)}_{j,p} \) corresponding to the decoding iteration \( \ell \) is shown. As can be seen from the figure, the core of iBDD-CR is to compute \( \hat{r}^{(i), \ell}_{j,p} \). As explained in Section II-C, \( \hat{r}^{(i), \ell}_{j,p} = \tilde{l}^{(i), \ell}_{j,p} + l^{(i), \ell}_{j,p} \), where \( \hat{r}^{(i), \ell}_{j,p} \) can be computed using a LUT (see [17, Table I & II]). In [17] the entries of the LUT are optimized via DE for the GLDPC code ensemble encompassing PCs, and used for implementing the iBDD-CR for PCs. In the following, we extend this DE analysis to the SC-GLDPC code ensemble, which allows to find the LUT for SCCs and implement iBDD-CR.

#### B. DE analysis of iBDD-CR for SC-GLDPC Ensembles

Fig. 7 shows the Tanner graph of a SC-GLDPC ensemble with \( n^2/4 \) degree-2 variable nodes (VNs) and \( n/2 \) constraint nodes (CNs) of degree \( n \) at each spatial position.

The coupling memory of this SC-GLDPC ensemble is \( 2 \). Therefore, the VNs at spatial position \( i \) are randomly connected to CNs at spatial position \( i \) and \( i+1 \). This randomness is represented in Fig. 7 by the edge interleavers \( \pi_i \). Furthermore, CNs at spatial position \( i \) are randomly connected (via the edge interleavers \( \pi'_i \) in Fig. 7) to VNs at spatial position \( i-1 \) and \( i \). Comparing Fig. 1(b) with Fig. 7, one can infer that SCCs can be constructed as a particular instance of a SC-GLDPC ensemble, where \( n/2 \) BCH component codes correspond to CNs and the \( n^2/4 \) code bits of \( B_i \) correspond to VNs at spatial position \( i \). We highlight that SCCs are deterministic codes (see [28]), i.e., the connections between VNs and CNs are determined by the SCC structure, which is not random. The
reason for analyzing the SC-GLDPC code ensemble instead of the Tanner graph of SCCs is that the randomization in the SC-GLDPC ensemble significantly simplifies the DE analysis. Assuming extrinsic message passing [29, Sec. II–B], BICM channel mixing [30, Sec. IV–A], and employing channel adapters in BICM [31], in what follows we generalize the DE analysis of iBDD-CR originally derived for the GLDPC code ensemble in [17, Sec. IV], to the SC-GLDPC code ensemble.

Let us assume BCH codes as the CNs. In the DE analysis of iBDD-CR for the GLDPC code ensemble [17, Sec. IV], it is shown that for a one-dimensional modulation of order \( M \) and noise standard deviation \( \sigma \), the output message error probability of the iBDD-CR at CNs and iteration \( \ell \) is given by

\[
x_{\text{out}}^{(\ell)} = \mathcal{g} \left( x_{\text{in}}^{(\ell)}, \sigma, M \right),
\]

where \( \mathcal{g}(\cdot) \) is defined by [17, Eq. (13)] and \( x_{\text{in}}^{(\ell)} \) denotes the input message error probability of CNs. Note that \( x_{\text{in}}^{(0)} = \rho_{\text{ch}} \) initializes the DE, with \( \rho_{\text{ch}} \) defined as the channel output error probability yielded by applying hard detection on the channel LLRs. The main difference between the Tanner graph of GLDPC code ensembles and SC-GLDPC code ensembles is the existence of coupling memory in the Tanner graph of the latter. To incorporate the effect of coupling in the DE analysis, we need to track the message error probability corresponding to each spatial position. As we are interested in iBDD-CR for SCCs, in what follows we consider SC-GLDPC code ensembles with coupling memory 2 (see Fig. 7).

We denote by \( \hat{x}_{\text{CN}}^{(i), (\ell)} \) the average bit error probability from CNs at spatial position \( i \) to connected VNs at positions \( i \) and \( i - 1 \). Furthermore, we denote by \( x_{\text{CN}}^{(i), (\ell)} \) the average bit error probability from CNs at spatial position \( i \) to the connected CNs at spatial positions \( i \) and \( i + 1 \). \( x_{\text{CN}}^{(i), (\ell)} \) and \( x_{\text{CN}}^{(i), (\ell)} \) can be calculated as

\[
x_{\text{CN}}^{(i), (\ell)} = \frac{x_{\text{CN}}^{(i-1), (\ell)} + x_{\text{CN}}^{(i), (\ell)}}{2},
\]

\[
x_{\text{CN}}^{(i), (\ell+1)} = \mathcal{g} \left( x_{\text{CN}}^{(i), (\ell)}, \sigma, M \right) + \mathcal{g} \left( x_{\text{CN}}^{(i+1), (\ell)}, \sigma, M \right),
\]

where (10) is employed to compute (12).

Recall that window decoding is usually employed for decoding of SCCs. To account for the effect of window decoding in the DE analysis, we assume that messages are only exchanged between VNs and CNs within the decoding window. Concretely, let \( \mathcal{W} \) be the set of spatial positions within the decoding window and \( x_{\text{CN}}^{(i), (\ell)} \) the average bit error probability from CNs at spatial position \( i \) within the decoding window. Then, \( x_{\text{CN}}^{(i), (\ell)} = x_{\text{in}}^{(i), (\ell)} \) if \( i \in \mathcal{W} \), otherwise \( x_{\text{CN}}^{(i), (\ell)} = 0 \).

Employing \( \hat{x}_{\text{CN}}^{(i), (\ell)} \) in (11)–(12) yields the DE recursion for the SC-GLDPC code ensemble at position \( i \) and iteration \( \ell + 1 \), which is given as

\[
x_{\text{CN}}^{(i), (\ell+1)} = \mathcal{g} \left( \frac{x_{\text{CN}}^{(i), (\ell)} + x_{\text{CN}}^{(i), (\ell-1)}}{2}, \sigma, M \right) + \mathcal{g} \left( \frac{x_{\text{CN}}^{(i), (\ell)} + x_{\text{CN}}^{(i+1), (\ell)}}{2}, \sigma, M \right) \tag{13}
\]

As shown in [17], the computation of \( \mathcal{g}(\cdot) \) for a GLDPC code ensemble results in a LUT for the values of \( x_{\text{CN}}^{(i), (\ell)} \) (see Fig. 2). Similarly, the computation of (13) for a SC-GLDPC code ensemble yields a LUT for the values of \( \hat{x}_{\text{CN}}^{(i), (\ell)} \) corresponding to spatial position \( i \) (see Fig. 6). Due to this similarity and for the sake of compactness of the paper, we refer to employ (13) in [17, Proposition 1] for computing the entries of the LUTs.

### C. BEE-SCC Algorithm

In this section, a novel decoding algorithm is developed for SCCs. We refer to this new algorithm as BEE-SCC. Similar to BEE-PC, BEE-SCC is inspired by iBDD-CR and utilizes the GD metric (5). Fig. 8 shows the schematic of BEE-SCC in making a decision for the \( j \)th row of \( [B_j^1, \ldots, B_j^{T}] \). Similar to Section IV, we denote by \( \hat{\Psi}_{j, :}^{(i), (\ell)} \) the hard decision input of BEE-SCC corresponding to \( [B_j^1, \ldots, B_j^{T}] \).

We start by explaining the upper branch of Fig. 8, which has some similarities to iBDD-CR. Following the iBDD-CR algorithm with input \( \hat{\Psi}_{j, :}^{(i), (\ell)} \), the candidate decision \( \hat{\Psi}_{j, :}^{(i), (\ell)} \) is computed as

\[
\hat{\Psi}_{j, :}^{(i), (\ell)} = \mathcal{B}(L_{j, :}^{(i), (\ell)}), \quad \text{if BDD fails}
\]

\[
\hat{\Psi}_{j, :}^{(i), (\ell)} = \mathcal{d}(\hat{\Psi}_{j, :}^{(i), (\ell)}, \hat{\Psi}_{j, :}^{(i), (\ell)}), \quad \text{if EED fails}
\]

\[
\hat{\Psi}_{j, :}^{(i), (\ell)} = \mathcal{d}(\hat{\Psi}_{j, :}^{(i), (\ell)}, \hat{\Psi}_{j, :}^{(i), (\ell)}), \quad \text{otherwise}
\]

The lower branch of Fig. 8 serves as a second decoding attempt. In particular, the 2 least reliable bits of \( \hat{\Psi}_{j, :}^{(i), (\ell)} \) according to reliability vector \( [L_{j, :}^{(i), (\ell)}] \) are erased and passed to the algebraic EED [26, Sec. 6.6]. We denote by \( \hat{M}_{j, :}^{(i), (\ell)} \) the output of EED with three possible values for the components. Using the same LUT iBDD-CR utilizes, the LLR \( L_{j, :}^{(i), (\ell)} \) is computed. Then, the candidate decision \( \hat{\Psi}_{j, :}^{(i), (\ell)} \) is formed as

\[
\hat{\Psi}_{j, :}^{(i), (\ell)} = \mathcal{B}(\hat{L}_{j, :}^{(i), (\ell)}), \quad \text{if BDD fails}
\]

\[
\hat{\Psi}_{j, :}^{(i), (\ell)} = \mathcal{d}(\hat{\Psi}_{j, :}^{(i), (\ell)}, \hat{\Psi}_{j, :}^{(i), (\ell)}), \quad \text{if EED fails}
\]

\[
\hat{\Psi}_{j, :}^{(i), (\ell)} = \mathcal{d}(\hat{\Psi}_{j, :}^{(i), (\ell)}, \hat{\Psi}_{j, :}^{(i), (\ell)}), \quad \text{otherwise}
\]

These assumptions are only considered for the sake of DE analysis, yielding the LUT required for implementing the iBDD-CR for SCCs. The LUT obtained via DE is then used for the simulation of SCCs. However, for the simulation results in Section IV-D, we consider standard BICM with intrinsic message passing decoding of SCC. No channel mixing and no channel adapters are used in the numerical simulations.
**D. Numerical Results**

In this section, we evaluate the performance of iBDD-CR and BEE-SCC. We consider a window decoder with a size of 7 staircase blocks and a maximum of 10 iterations, appended with 2 iBDD iterations (see Section III-C for discussion of appended iBDD iterations). Also, we consider SCCs with even length component codes, hence, when necessary, one bit shortening is performed to have even component code length.

In order to evaluate the derived DE of iBDD-CR for the SC-GLDPC code ensemble (see Section IV-B), in Fig. 9, we compare the DE results with the performance of SCCs with component codes \( C_2 \) and \( C_3 \) for transmission over the bi-AWGN channel. For the sake of comparison, we also show the performance of PCs with the same component codes and the DE evolution curves for the corresponding GLDPC code ensemble [17, Fig. 4]. As it can be seen, DE can predict the performance of SCCs with good accuracy and the gap between simulation results and DE is reduced by increasing the code block length (c.f. the gap between dotted curves with solid curves of Fig. 9(a) and Fig. 9(b)). Furthermore, the spatial-coupling gain of SCCs over the corresponding PCs is also well-predicted by the DE analysis. Therefore, the derived DE for iBDD-CR in Section IV-B can also be used for the parameter optimization of SCCs, similar to the approach taken in [32] for the parameter optimization of PCs.

In Figs. 10 and 11, the performance of iBDD-CR and BEE-SCC are compared with that of iBDD, ideal iBDD, AD, and iBDD-SR for SCCs with component codes \( C_2 \) and \( C_3 \) and transmission over the bi-AWGN channel. One can see that BEE-SCC and iBDD-CR outperform all other algorithms. In particular the gain of iBDD-CR and BEE-SCC over iBDD is 0.41 dB and 0.55 dB, respectively, for \( C_2 \), and 0.33 dB and 0.44 dB for \( C_3 \).

In Fig. 12, we consider a BICM system (employing random interleaver) with 256-QAM and \( C_2 \) as component code, and compare the performance of iBDD, ideal iBDD, iBDD-CR, and BEE-SCC. For a BER of \( 10^{-7} \), the performance gain of iBDD-CR and BEE-SCC over iBDD is 0.61 dB and 0.88 dB, respectively. Comparing Fig. 12 with Fig. 10 reveals that the performance improvement of the proposed schemes over iBDD increases by employing higher order modulations.

Finally, by employing the GN model and fiber parameters given in Table II, the gain for BEE-SCC compared to iBDD translates into 80 km reach enhancement of BEE-SCC compared to iBDD, corresponding to \( \eta = 33\% \).

Comparing Figs. 4, 5, 10, and 11, one can see that the performance gain of BEE-PC and BEE-SCC over iBDD depends on the component codes. In particular, for a given component code length \( n \), reducing \( t \) yields higher gains. Furthermore, for a given component code error correcting capability \( t \), reducing \( n \) also increases the performance gain. This is due to fact that the probability of component decoding miscorrections and failures increases in such cases, hence, BEE-PC and BEE-SCC (which deal with recovering miscorrections and failures) can improve more the performance of (standard) iBDD.

V. BEE-PC AND BEE-SCC: HEURISTICS AND COMPLEXITY

In this section, our goal is to shed some light on the insights and heuristics at the basis of BEE-PC and BEE-SCC algorithms as well as to discuss the algorithmic complexity of the proposed algorithms.
Fig. 10. Performance comparison of iBDD, AD, iBDD-SR, iBDD-CR, and BEE-SCC for staircase code with component code $C_2$.

Fig. 11. Performance comparison of iBDD, AD, iBDD-SR, iBDD-CR, and BEE-SCC for SCC with component code $C_3$.

A. Heuristics

We first explain the similarities of BEE-PC and BEE-SCC. Both algorithms employ an erasure attempt to improve the performance of iBDD-CR. For a component code containing $e$ errors and $s$ erasures, the EED is successful if $2e + s \leq d_{\text{min}} - 1$, where $d_{\text{min}}$ is the minimum Hamming distance of the component code [26, Sec. 6]. The first attempt of BEE-SCC (corresponding to the upper branches in Fig. 6 and Fig. 8) considers $s = 0$, therefore it is capable of correcting up to $\lceil d_{\text{min}} - 1/2 \rceil$ errors, i.e., $t$ errors. However, the second attempt (corresponding to the lower branch in Fig. 6 and Fig. 8) considers $s = 2$, hence it is capable of correcting $\lceil d_{\text{min}} - 3/2 \rceil$ errors and 2 erasures. One can easily check that $\lceil d_{\text{min}} - 3/2 \rceil < \lceil d_{\text{min}} - 1/2 \rceil$ and $\lceil d_{\text{min}} - 3/2 \rceil + 2 \geq \lceil d_{\text{min}} - 1/2 \rceil$, therefore, the second attempt can correct more errors if the least reliable bits corresponds to error bits.

For a component code of length $n$, one can show that (5) is upper bounded by $2n$, hence the definition of $\bar{d}$ and $\tilde{d}$ for both BEE-PC and BEE-SCC (see (6), (7), (15), and (17)) ensures that the candidate codeword is selected from the branch without a decoding failure.

We also highlight that both BEE-PC and BEE-SCC employ the same LUT for both decoding attempts. As shown in [17, Appendix A], the entries of the LUT are derived based on analyzing the behavior of BDD. Following the DE steps in [17], we found that employing EED should in principle yield a new LUT compared to that of iBDD-CR. Unfortunately, finding the entries of the optimal LUTs for BEE-PC and BEE-SCC requires the computation of some probabilities which seems to be intractable. Therefore, we pragmatically resorted to the same LUT as given by the DE analysis for iBDD-CR.

In this sense, the mapping given by the LUTs for the second branch of BEE-PC and BEE-SCC is heuristic.

The main difference between BEE-PC and BEE-SCC is that each algorithm exploits different soft information values for the erasure attempt. In order to efficiently perform the erasure attempt one needs a reliability measure. In BEE-PC, $|L_{i,\ell}^c(\ell-1)|$ is used to find the two least reliable bits of $\Psi_{k,i}^c(\ell-1)$. (see Fig. 3). If we use the architecture of iBDD-CR to implement BEE-PC, we have to exchange soft values $L_{i,\ell}^c(\ell-1)$ between component decoders, yielding a significantly higher internal decoder data flow compared to iBDD-CR. To avoid this, BEE-PC modifies the iBDD-CR architecture such that the BDD/EED decisions, i.e., $M_{i,\ell}^c(\ell-1)$ are exchanged (cf. Fig. 2 and the first branch of Fig. 3). With this modification, both (hard) decisions $\Psi_{i}^c(\ell-1)$ and LLRs $L_{i,\ell}^c(\ell-1)$ used in BEE-PC can be computed locally in the row and column decoders using $M_{i,\ell}^c(\ell-1)$ (or $M_{i,\ell}^c(\ell-1)$), the channel LLRs, and the iBDD-CR LUT.

On the other hand, in BEE-SCC $|\bar{L}_{i,\ell}^c|$, is used to find the two least reliable bits of $\Psi_{j,\ell}^c(\ell)$. Note that according to the derived DE in Section IV-B, $|\bar{L}_{i,\ell}^c|$ is the reliability of the iBDD-CR output $\Psi_{j,\ell}^c(\ell)$ (see Fig. 8). However, in BEE-
Table III
ALGORITHMIC-LEVEL COMPLEXITY COMPARISON BETWEEN DIFFERENT HYBRID DECODING SCHEMES FOR PCs AND SCCs [12]–[17], [22] AND THE PROPOSED BEE-PC AND BEE-SCC. THE MEMORY REQUIREMENTS SPECIFY THE MAIN TYPE OF MEMORY REQUIRED AND A BRIEF EXPLANATION.

| Decoding Algorithm | Computing LLRs | Required sorting Alg. | Code/System type | Contribution of message exchanges to the decoder data flow | Memory requirements |
|---------------------|----------------|-----------------------|-----------------|----------------------------------------------------------|---------------------|
| AD [22]             | no             | no                    | PC, SCC, bi-AWGN | hard messages similar to iBDD                             | Dynamic: Storing the location of decoding conflicts and realizing the proposed backtracking algorithm |
| iGMDD-SR [12]       | yes            | yes                   | PC, bi-AWGN     | soft messages                                            | Static: Storing channel LLRs                                    |
| BMP-GMDD [13]       | yes            | yes                   | PC, bi-AWGN     | hard messages with 8%-33% higher data flow than iBDD     | Static: Storing channel LLRs                                    |
| iBDD-SR [14]        | yes            | no                    | PC, SCC, CM     | hard messages similar to iBDD                            | Static: Storing channel LLRs                                    |
| SABM [15]           | yes            | yes                   | PC, SCC, CM     | hard messages similar to iBDD                            | Static: Storing channel LLRs                                    |
| SABM-SR [16]        | yes            | yes                   | PC, CM          | soft messages                                            | Static: Storing channel LLRs                                    |
| iBDD-CR [17]        | yes            | no                    | PC, SCC, CM     | hard messages similar to iBDD                            | Static: Storing channel LLRs                                    |
| BEE-PC              | yes            | yes                   | PC, CM          | hard messages with 0.2%-0.5% higher data flow than iBDD  | Static: Storing channel LLRs                                    |
| BEE-SCC             | yes            | yes                   | SCC, CM         | hard messages similar to iBDD                            | Static: Storing channel LLRs                                    |

SCC we pragmatically employ it as the reliability measure for $\Psi_{j; i}(t))$. The motivation is that BDD reveals also some information about its input, e.g., in the case of decoding failure it shows that the input is not within distance $t$ of any codeword. Using $[\bar{L}]_{j; i}$ as the reliability measure for the error-and-erasure attempt has also a practical implication. $[\bar{L}]_{j; i}^{(i)}(t)$ is computed inside the decoder by the first decoding attempt (see first branch of Fig. 8), hence, there is no need to exchange any soft value between component decoders in order to erase the two least reliable bits for the second decoding attempt. We remark that, in principle, one can employ the BEE-PC architecture for SCCs as well. However, we found that such scheme yields minor performance improvement compared to iBDD-CR.

### B. Complexity

A detailed complexity comparison between BEE-PC, BEE-SCC, the hybrid decoding algorithms in [12]–[17], and AD [22] would require a hardware implementation of each decoder, and comparing the resulting overall throughput and energy consumption. This implementation is beyond the scope of this paper, and thus, here we provide an algorithmic-level comparison. In the following, we first evaluate the contribution of the message exchange between component decoders of BEE-PC and BEE-SCC to the overall internal decoder data flow, as an essential metric for high-throughput systems [5]. We then compare this and other implementation requirements of BEE-PC and BEE-SCC with those of the algorithms in [12]–[17], [22] from an algorithmic-level perspective.

As explained in Section II-C, for the $i$th row decoding of a PC, BEE-PC outputs $M_{i; i}^{(i)}(t)$ with elements in $\{0, \pm 1\}$, and sends it to the column decoders. Therefore, it may seem at a first glance that the contribution of the message exchange of BEE-PC to the decoder data flow is higher than that of iBDD-CR and iBDD—both exchange only binary messages. However, in what follows, we show BEE-PC can be implemented more efficiently than a plain ternary message passing between component decoders. Recall that the elements of $M_{i; i}^{(i)}$ are ternary because BDD or EDD may fail. In such case, all elements of $M_{i; i}^{(i)}$ are zero. If the row decoders can somehow indicate the failure to the column decoders (and vice versa), then the components of $M_{i; i}^{(i)}$ become binary. For the efficient implementation of BEE-PC, we propose to extend $M_{i; i}^{(i)}$ by one bit, i.e., $M_{i; i}^{(i)}$ is extended from a length-$n$ vector to a vector of length $n + 1$, in which the extra bit is $1$ if $M_{i; i}$ corresponds to BDD/EDD decoding. In this case, the other $n$ bits of $M_{i; i}^{(i)}$ take value in $\{0, 1\}$ using the mapping $+1 \rightarrow 0$ and $-1 \rightarrow 1$. The extra bit is $0$ if $M_{i; i}^{(i)}$ corresponds to BDD/EDD failure. In this case, the other $n$ bits of $M_{i; i}^{(i)}$ are $0$. With this simple bit extension and mapping, $M_{i; i}^{(i)}$ becomes binary, at the cost of sending only a single extra bit per component code. As the component code of a PC is typically long to reduce the error floor, the contribution of exchanging an extra bit to the decoder data flow is negligible. For instance, BEE-PC decoding of a PC with BCH component code of length 255 and 511, entails an increase in message exchange of only 0.4% and 0.2%, respectively, compared to iBDD-CR and conventional iBDD.

As shown in Section IV-C, BEE-SCC only exchanges (binary) hard decisions between component decoders (see (18) and Fig. 8), hence, the contribution of message exchange of BEE-SCC to the decoder data flow is the same as that of iBDD-CR and conventional iBDD.

Two other implementation aspects we consider here are the complexity entailed by EDD and the LLR calculations. BDD is usually implemented based on the Berlekamp-Massey algorithm [33]. EED can also be implemented by modifying
the Berlekamp-Massey algorithm, hence, the complexity of EED and BDD are roughly similar [34]. Both BEE-PC and BEE-SCC require to compute and store the channel LLRs for the code bits, and an algorithm to find the two least reliable bits per component code. It is important to remark that the memory required to store the channel LLRs static, as they are not updated during the decoding process. It is known that static memory is significantly less costly than dynamic memory in hardware implementation [11].

In Table III, we compare different features of AD [22], iBDD-SR [14], SABM [15], iBDD-CR [17], SABM-SR [16], iGMDD-SR [12], and BMP-GMDD [13] with those of BEE-PC and BEE-SCC. As can be seen from the table, some of the proposed algorithms are evaluated for PCs or for transmission over the bi-AWGN channel, however, the others are investigated for both PCs and SCCs and CM scheme. Furthermore, one can see that each algorithm requires different memory types and message passing. We highlight that the contribution of message passing to the decoder data flow is estimated based on BCH component code parameters \( n = 255, n = 511, \) and \( t = \{2, 3, 4\} \), which are typically considered in the literature [12]–[17], [22].

VI. CONCLUSIONS

We extended the recently introduced iBDD-CR algorithm for PCs to SCCs via a DE analysis of the SC-GLDPC code ensemble encompassing SCCs as particular instances. We further proposed two novel decoding algorithms for PCs and SCCs which augment iBDD-CR by introducing a second decoding attempt based on EED of the component codes. Both BEE-PC and BEE-SCC offer sizeable performance gains compared to standard iBDD, up to 0.88 dB for a BICM system using 256-QAM. These translate into an enhancement of the optical reach of up to 33%. Moreover, the internal decoder data flow of BEE-PC and BEE-SCC resulting from the exchange of messages between component decoders is roughly the same of that of (standard) iBDD, which makes the proposed algorithms excellent candidates for next generation ultra high-throughput systems.

Future work includes hardware implementation of BEE-PC and BEE-SCC and measuring the corresponding energy consumption per information bit at high throughputs.

ACKNOWLEDGMENT

The authors would like to thank Dr. Christian Häger for providing the simulation results of AD in Figs. 4, 10, and 11.

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8 Table III briefly compares the implementation requirements of different decoders. We refer the reader to [12]–[17], [22], for more extensive description of each decoding algorithm.

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