Performance of the new Amplifier-Shaper-Discriminator chip for the ATLAS MDT chambers at the HL-LHC

M. De Matteis, a, 1 F. Resta, a R. Richter, b H. Kroha, b M. Fras, b Y. Zhao, b V. Danielyan, b S. Abovyan b and A. Baschirotto a

a Physics Department, Piazza della Scienza 3, Milano, Italy
b Max-Planck-Institute for Physics, Munich, Germany

E-mail: marcello.dematteis@unimib.it

Abstract: The Phase-II Upgrade of the ATLAS Muon Detector requires new electronics for the readout of the MDT drift tubes. The first processing stage, the Amplifier-Shaper-Discriminator (ASD), determines the performance of the readout for crucial parameters like time resolution, gain uniformity, efficiency and noise rejection. An 8-channel ASD chip, using the IBM 130 nm CMOS 8RF-DM technology, has been designed, produced and tested. The area of the chip is $2.2 \times 2.9 \text{ mm}^2$ size. We present results of detailed measurements as well as a comparison with simulation results of the chip behavior at three different levels of detail.

Keywords: Front-end electronics for detector readout; Analogue electronic circuits; Radiation-hard electronics

1 Corresponding author.

doi:10.1088/1748-0221/11/02/C02087
1 Introduction

In the last years, integrated circuits (ICs) solutions have been widely used in high-energy physics experiments (HEP), with the main aim to replace the common service electronics (based on very old CMOS processes and/or off-the-shelf components [1, 2]), with more efficient scaled-down ICs, able to improve sensitivity, noise and power performance.

The analog front-end, named ASD, includes Amplifier, Shaping and Discriminator stages. The ASD [1], presently used for the read-out of Monitored-Drift-Tube (MDT) chambers of the ATLAS experiment at the Large Hadron Collider (LHC) at CERN, is a 0.5 µm CMOS design. It is biased at 3.3 V and provided reliable operation and low failure rate. It performs a front-end charge-to-voltage conversion (by a proper Charge-Sensitive-Preamplifier) followed by the analog signal conditioning (amplification and shaping) and A/D conversion. It features a sensitivity (i.e. voltage vs. charge conversion ratio) of 8.9 mV/fC [1], 15 ns nominal Peaking Time Delay (i.e. PTD, the front-end capability to quickly detect charge arrival time) and low-noise enabling 5 fC minimum detected charge at 10 dB (3.2× factor) Signal-to-Noise-Ratio (i.e. SNR).

The LHC collider at CERN is presently in an upgrade process ([2]) to be implemented after the year 2025, called Phase-II, to enable higher luminosities of a factor 5–7.5 beyond the nominal value of $10^{34}$ cm$^{-2}$s$^{-1}$. This high luminosity is challenging for the MDT read-out system for two aspects. Higher hit rates, mainly due to increased cavern background, drive data transmission to the rear end electronics to the limit of available bandwidth. In addition, the new L1 trigger operating parameters — latency up to 60 µs and trigger rates up to 400 kHz — call for a replacement of the entire readout chain.

In this scenario, the ASD performance of the MDT system has to be improved, while maintaining the present, well established system architecture (including the parasitic capacitance of the detector of about 60 pF).
This paper presents the 8-channels MDT-ASD (8xASD) in CMOS 0.13 μm technological node, where improvements are performed in terms of:

- lower peaking time delay (PTD) to achieve the required time resolution;
- larger sensitivity and higher SNR at 5 fC minimum charge.

The large swing required to adopt a single 3.3 V supply voltage that can be sustained only by the 0.35 μm High-Voltage (HV) devices. The 8xASD performs 11 ns PTD (w.r.t. the original 15 ns), 13.8 mV/fC sensitivity (w.r.t. the original 8.9 mV/fC) and 15 dB (5.6× factor) SNR (w.r.t. the original 10 dB). These improved results have been obtained without increasing the power consumption that is strongly fixed by the input noise specifications. This means that the technology scaling has been exploited for performance improvement and area reduction (about a factor 2× with 6 mm² die size w.r.t. the original 11.9 mm²).

This paper is organized as follows. Section 2 introduces the ATLAS experiment key points for electronics development. Section 3 presents the CMOS 8xASD circuital/design choices, while section 4 is focused on the preliminary experimental results. At the end conclusions will be drawn.

2 The ATLAS experiment

The ATLAS experiment at the CERN LHC collider is designed to record collisions from protons on protons (p-p collisions) at center-of-mass energies of up to 14 TeV. In order to determine energy and direction of the secondary particles, emerging from the p-p collisions, a sequence of specialized detectors is used for the detection of charged and neutral particles through a shell-like structure.

The muons emerging from the primary collision, being the most penetrating charge particle component, are able to transverse the Calorimeters and to reach the Muon spectrometer, the outermost shell of the ATLAS detector. Electrons generated by muons in the gas-filled pressurized MDT tubes are drifting to the central wire of the tube, where their time-of-arrival is used to determine the distance of the track from the wire. As the muon usually passes through a large number of drift tubes, the position of the muon track can be reconstructed from a combination of measurements in the tubes along the muon trajectory. Details about the MDT ATLAS readout electronics are given in [4]. Figure 1 shows a simplified MDT readout simplified scheme. The small charge signals coming from the wires are sent to the ‘mezzanine’ board where the 8xASD is placed (see figure 2 for the single-channel system generic block scheme).

This monolithic 8xASD senses, shapes and converts the signal coming from the tubes, providing time-domain voltage pulses, whose duty cycle is proportional to the amount of charge at the 8xASD input. The output signal of the discriminator, triggered when the voltage pulse crosses a predefined, adjustable threshold is subsequently sent to an off-chip Time-to-Digital Converter (TDC), which forwards the signal arrival times down the data acquisition chain for recording and track reconstruction.

3 MDT-ASD circuital implementation

The device includes eight identical channels and it has been realized in IBM 0.13 μm CMOS technology. The architecture of a single-channel 8xASD is shown in figure 2 [3]. Each channel input signal is a current pulse signal coming from the detector. It is converted into a voltage signal
3.1 Charge-Sensitive-Preamplifier

The system behavior is strongly dependent on the performance of the CSPreamp that must manage the large detector capacitance of about 60 pF.

The CSPreamp is composed by two identical symmetrical paths. A dummy preamp has been used for differential signal processing, and as a consequence the input charge is read from one single path (CSP in figure 2). The transistor-level scheme of the CSPreamp is shown in figure 3.
The CSPreamp structure is the same of the previous design. However the design strategy and parameters have been completely re-designed to improve the performance in terms of the input impedance (< 120Ω), noise, and speed of response. Regarding the input impedance, the CSPreamp is based on a cascode common source amplifier, which guarantees large loop-gain for closed-loop operation, and as consequence a better virtual ground at the input node (required by the large CD). The input impedance is maintained almost constant for all in-band frequencies, since at low frequency, it is fixed by RL (=16 kΩ) and RF (=16 kΩ), while, at higher frequency, it is regulated by the Feedback Capacitance (CF = 680 fF) and by the detector capacitance (CD = 60 pF). The output signal is read at the M2 drain. The M3 – RS – M4 source-follower is used to increase and optimize the output node common-mode voltage, for the following DA1 stage, which has NMOS input transistors (for noise minimization). Vb2 and Vb3 nodes are connected to diode transistors of cascode mirrors.

Regarding CSPreamp noise and time-response, both are optimized by suitable input device transconductance (g_m1). In this direction, transistor M1 operates in moderate inversion region (V_ov ≈ 100 mV) with a nominal current of 1.6 mA in order to have large g_m1 (25 mA/V), much larger than in previous design. This improves both noise and speed. Nonetheless, thanks to a better redistribution of the power among the different stages, the overall power consumption is not increased. In fact, larger power is allocated to the CSPreamp input stage, saving power where it was not necessary (mainly in the DAx chain, and in the bias circuit). Such large g_m1 value improves the speed-of-response as follows. The CSPreamp transfer function is approximately given by:

\[
T(s) \approx -R_F \cdot \frac{1 - s \cdot \frac{C_F}{g_m1}}{\left(1 + s \cdot C_F \cdot R_F \left(1 + \frac{C_D}{C_F} \cdot \frac{1}{1 + g_m1 \cdot R_L}\right)\right) \cdot \left(1 + s \cdot \frac{C_D}{g_m1}\right)}.
\]  

(3.1)

Since g_m1 = 25 mA/V and CF ≪ CD, the zero is at much higher frequency and can be neglected. Assuming infinite g_m1, the dominant pole is given by (CF • RF), and the output pulse voltage peak value should be approximately given by (Q_IN/CF) ≈ 7 mV_0–PEAK. In this design g_m1 has been fixed at 25 mA/V, as trade-off between noise and power, resulting in a CSPreamp sensitivity of 1.4 mV/fC. These considerations are validated by figure 4, where the simulated CSPreamp time response is shown (NO-NOISE curve) and compared with the single-pole ideal system (No-Noise, No-CD curve). The main effects of the CD capacitance increase are lower sensitivity (4 mV_0–PEAK vs. 6 mV_0–PEAK for minimum Q_IN = 5 fC), and slightly slower time response (7 ns vs. 4 ns).
The large $g_{m1}$ value avoids significant sensitivity degradation due to the large parasitic detector capacitance and mitigates the second pole effect, pushing it up to much higher frequency. This improves the CSPreamp transient performance (the second pole time constant is inversely proportional to $g_{m1}$, as stated in eq. (3.1)). Moreover, such large $g_{m1}$ value enforces virtual ground and lowers CSPreamp equivalent input impedance down to $\approx 60\,\Omega$ (nominal, in order to be $< 120\,\Omega$ in nominal condition and in presence of CMOS process, supply voltage and temperature variations) acceptable for the peaking time delay, and noise. Two transient-noise iterations have been run, to highlight the thermal noise contribution, resulting in $0.55\,\text{mV RMS}$-in-band output noise power. The SNR at the CSPreamp output is $19\,\text{dB}$ ($8.9 \times$ factor) in case of minimum input charge of $5\,\text{fC}$, and it rises up to $45\,\text{dB}$ ($178 \times$ factor) at $100\,\text{fC}$.

3.2 DA$_1$-DA$_2$-DA$_3$

The CSPreamp output signal is amplified & filtered by the DA$_1$-DA$_2$-DA$_3$ stages, which convert the signal into a bipolar pulse and define the fall-down time. In this DA$_1$-DA$_2$-DA$_3$ chain, the scaled $0.35\,\mu\text{m}$ devices have been exploited in the reduction of the parasitic capacitance, and in increasing the speed while reducing power consumption. The frequency response at the output of each stage is plotted in figure 5. The full chain exhibits a pass-band characteristic with a $5\,\text{MHz}$ center frequency. The high-pass part, mainly imposed by DA$_3$, shows a $30\,\text{kHz}$ corner frequency and a slope of $+6\,\text{dB/octave}$ ($1^{\text{st}}$-order high-pass filter). The band-pass section is the superposition of all four amplifier low-pass characteristics.

3.3 Wilkinson A/D

The DA$_3$ output signal feeds to the Discriminator and the Wilkinson ADC (W-ADC) stage, to provide information regarding the arrival time and the total amount of input charge at the CSPreamp input node. The Discriminator is a comparator, which detects the presence of a specific minimum charge at the CSPreamp input nodes and provides the charge arrival time, and the Start-of-Conversion signal for the W-ADC. The W-ADC, instead, performs a Voltage-to-Time conversion, as shown in figure 6. The sampling capacitor ($C_H$) is charged for a given time range $T_{GW}$ (programmable between $8\,\text{ns}$ and $32\,\text{ns}$) and the capacitance $C_H$ is then discharged down to the time of zero-crossing.
Charge and discharge phases depend on $\Phi_1$ and $\Phi_2$, such as on ON-OFF switches phases. $\Phi_1$ and $\Phi_2$ signals are complementary MOS switches. The time to discharge $C_H$ will be proportional to the analog input voltage and, as a consequence, to the equivalent amount of charge at the CSPreamp input nodes. For a given integration time $T_{GW}$, the analog voltage peak value (i.e. the input charge $Q_{IN}$) is proportional to the time to cross the horizontal axis (figure 6). The transconductor stages design had to face the lower output impedance of the 0.35 $\mu$m devices w.r.t. the 0.5 $\mu$m devices. Specific arrangements have then been adopted to guarantee the same impedance level. On the other hand, the power here is unchanged since it is fixed by the value of $C_H$, maintained to be equal to 3 pF, to make parasitic effects negligible.

4 Preliminary measurements result

The presented 8xASD chip has been integrated in CMOS 0.13 $\mu$m (figure 7 shows the chip photo). The electrical characterization has been carried out mounting the 8xASD on the mezzanine board, working in the same boundary conditions w.r.t. the ATLAS experiment environments. The 8 channels are placed and routed in order to guarantee symmetrical paths w.r.t. the bias and setting circuits (located in the center region of the layout top-view, and used to program and regulate the discriminators thresholds, gain, etc). Each channel occupies 0.4 mm$^2$. The total area (including additional pads, JTAG, etc.) is about 6.38 mm$^2$. All measurements have been performed using input charge ($Q_{IN}$) in the range 5 fC – 100 fC.
4.1 8xASD electrical characterization

The analog section of the 8xASD composed by the cascade of the CSPreamp and the DA1-DA2-DA3 stages is here presented. Figure 8 shows the output signal vs. time at DA3 output buffers test pins (see figure 2), hence some voltage peak drop (i.e. about 3 dB (1.4× factor) and 2 ns additional time delay) and an additional peaking time delay is expected w.r.t. the effective on-chip DA3 signal. The DA3 output voltage ranges from 90 mV$_{0-\text{PEAK}}$ up to 1.2 V$_{0-\text{PEAK}}$. Figure 9 shows the V$_{\text{OUT,DA3/QIN}}$ trans-characteristic, justifying the 14.2 mV/fC of sensitivity for minimum Q$_{\text{IN}}$. Moreover, the sensitivity is quite constant over the input charge range, so no voltage swing saturation is presented over the 5 fC – 100 fC range, resulting in a sufficiently linear behaviour. Finally, figure 10 shows Peaking Time Delay that is lower than 9 ns for minimum Q$_{\text{IN}}$ (5 fC), and raises up to 12 ns at 100 fC. For sake of completeness, the figures 9–11 are shown with and without the amplitude and time effects of the test points output buffers.\footnote{Note that there are not measurements without buffer. The curves, indicated as ‘without buffer’, have been extrapolated from simulations.} The Wilkinson ADC has bee also tested for four different equivalent input charge values (in the 20 fC – 100 fC range). The output pulse width is proportional to the equivalent amount of charge at the 8xASD input, resulting in the sufficiently linear characteristic in figure 12.

5 Conclusions

An 8-channels read-out front-end for the MDT ATLAS detectors at CERN LHC has been presented. The design has been carried out in IBM 0.13 µm technology, targeting area and noise reduction at the same power budget of the state-of-the-art for ATLAS MDT detectors. Table 1 summarizes the most important performance of the presented 8xASD for the MDT-ATLAS-read-out, compared with the previous implementation.

The device exhibits a factor 2 area reduction (lower than the CMOS scaling-down factor due to 0.35 µm High-Voltage devices). For the same detector capacitance, the single channel power consumption is approximately the same than in [3], whereas input charge signal quality improves (higher SNR, given by better CSPreamp ENC noise performance). The peaking time delay is 12 ns, i.e. 3 ns lower than the state-of-the-art, resulting in faster response and reduced probability to muons data loss.
Table 1. State-of-the-art comparison.

| Parameter                        | This Work      | [3]            |
|----------------------------------|----------------|----------------|
| CMOS Technology                  | 0.13 µm@3.3 V  | 0.5 µm@3.3 V   |
| Total Die Area                   | 6.38 mm²       | 11.9 mm²       |
| Channel Current Consumption      | 10 mA          | 11 mA          |
| Detector Parasitic Cap.          | 60 pF          | 60 pF          |
| Input Charge                     | 5 fC – 100 fC  | 5 fC – 100 fC  |
| Front-End Delay at 100 fC@Q_{IN} | 12 ns          | ~ 15 ns        |
| Front-End Sensitivity            | 14 mV/fC       | 8.9 mV/fC      |
| ENC                              | 0.6 fC         | 1 fC           |
| SNR                              | 15 dB          | 10.9 dB        |

Figure 7. Chip Layout Photo.

Figure 8. DA₃ Test Point Buffers Output Signal vs. Input Charge (5 fC-100 fC).

Figure 9. Analog Chain (CSPreamp-DA₃) V_{OUT,DA₃}/Q_{IN} vs. Input Charge.
Figure 10. Analog Chain Peaking Time Delay vs. Input Charge.

Figure 11. Wilkinson ADC Output Pulse/DA3 output Signal vs. Input Charge.

Figure 12. Wilkinson ADC Output Pulse Time Width vs. Input Charge.
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