Recent progress in the technology linking sensors and digital circuits

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Abstract: Sensing systems perform digital-signal processing after converting analog input to digital output. These systems are used for various applications. This paper addresses the link between sensors and digital circuits. In particular, I address two areas: analog-to-digital converter (ADC) architecture and signal processing for sensing systems, and then describe their demands. Each circuit and system processing method was investigated and their basic outlines are illustrated. Finally, recent trends in specific hardware implementations of these algorithms are discussed.

Keywords: sensor network, low power, image sensor, image processing, hardware implementation

Classification: Integrated circuits

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1 Introduction

Sensing systems consisting of sensor outputs and signal processing have been used in various applications. A sensor outputs analog values, which, after
analog-to-digital conversion (ADC), are digitally processed. Sensing, as listed below, is undertaken, and the obtained information is handled differently depending on the intended use.

- Environmental sensing (temperature, air flow, water volume, luminance, etc.)
- Condition sensing (position, velocity, acceleration, strain, etc.)
- Substance identification (chemical substance, gas, radioactivity, etc.)

Figure 1 shows the block diagram of a sensor system [1, 2]. For example, in a digital temperature sensor, outputs of the band-gap-reference and temperature sensor are transmitted to the delta-sigma ADC, the ADC output is counted, and the obtained digital data is transferred externally. In the other hand, novel temperature sensing, which is based on temperature-dependent delays of inverters (in Fig. 2) [3, 4] and heat diffusion in Si and SiO$_2$ [5, 6], has been proposed. In an acceleration sensor, micro-electro-mechanical systems (MEMS) devices extract capacitance change as mass displacement, and

![Fig. 1. Circuit diagram of example digital temperature sensor](image1)

![Fig. 2. Operation scheme of delay line based temperature sensor](image2)
digital filtering is performed on the ADC outputs [7]. Since the applications of sensing systems cover very different areas, this paper addresses the linkage between sensors and digital circuits and focuses on two main areas: ADC architecture and digital signal processing. Especially in image sensing systems, the sensing information at each pixel is needed to process as 2-dimensional meaningful data. Since the output information quantity of the imaging device is much larger than the other sensing devices, the post processing with specific processors (e.g. Digital signal processor (DSP), etc.) is strongly demanded. Therefore, I also note the effective processing algorithm for hardware implementation.

2 Circuits for sensing systems

In a sensing system, while accurate sensing is an obvious necessity, it is important to develop cheap, small, and low-power sensors. Particularly in sensor-network applications, low-power communication and power generation are also required. With this in mind, the circuit technologies listed below have been researched.

- Efficient power generation
- Low-power ADC and/or robust A/D conversion in harsh environments
- Low-power communication protocols

2.1 Circuitry for efficient power generation

Passive sensor units need to generate their power from the environment. When generating power from environmental conditions such as temperature differentials, oscillation, pressure, and the electromagnetic waves of wireless communication, an efficient DC converter (such as a rectifier) is a key component. Since the threshold voltage of a MOSFET degrades the efficiency of the MOSFET rectifier, threshold-voltage $V_{th}$ cancelling techniques have been proposed. For this canceling, Umeda et al. gives external bias voltage to nodes between the gate and source terminals in 2005 [8]; Nakamoto et al. uses nonvolatile-memory architecture which stores the boosted voltage in 2006 [9]; Kotani et al. proposed a rectifier can automatically control $V_{th}$ of diode-connected MOS transistors in forward/reverse bias conditions in 2009 [10].

2.2 ADC architecture for sensing

Conventionally, delta-sigma type, dual-slope integrating type, flash type, and successive-approximation-register (SAR) type ADCs have been used for digitizing sensing values. In low-power ADCs, improvements in the efficiency of SAR ADCs have progressed rapidly. The SAR ADC charges/discharges the capacitor bank n-times for comparator operations at n-bits resolution, the process for which various low-power techniques have been proposed. This paper does not describe these techniques in detail as this paper is not a review
of ADCs alone. Watanabe et al., proposed a fully digital ADC architecture for sensing which is called “time A/D converter” (TAD) [11]. Figure 3 shows circuitry of the TAD. It has been proposed as a robust sensing circuit for harsh environments such as in vehicles. It consists of a voltage-controlled ring delay line and a counter. The delay line has an even number of delay cells and a duty controller. Velocity of the pulse in the delay line depends on the input voltage. At each sampling period, the internal state of the delay line and the frequency of pulse counting are output. In the TAD, the quantization error is transferred to the next conversion, so the TAD performs a first-order noise-shaping function. Moreover, use of an analog pre-filter can be removed by due to the nature of the TAD’s continuous operation. The integral non-linearity (INL) depends on the nonlinear response of the delay line. The good differential non-linearity (DNL) of the TAD is theoretically guaranteed and the INL is continuous, so it is easy to compensate for the INL.

![Block diagram of time A/D converter (TAD) and delay unit](image)

**Fig. 3.** Block diagram of time A/D converter (TAD) and delay unit

### 2.3 Low-power communication circuit

Although RF circuits are important in achieving low-power sensor network circuits, this paper leaves a detailed description to other papers. The digital part of these circuits operates a low-power medium access control (MAC) layer protocol. This protocol is related to high efficiency packet control on the sensor network. The MAC layer is based on synchronized preamble sampling. There is the trade-off between power consumption and sleep period, therefore various MAC protocols, which controlled periods of wake-up and sleep and synchronization at each node, have been proposed [13, 14, 15, 16].

### 3 Image sensing and processing

In image sensing systems, since the output information quantity of the imaging device is much larger than the other sensing devices, the image processing
with specific processors becomes key technique. Therefore, I explain not only ADC architecture for imagers but also the effective image-processing algorithm for hardware implementation in this section.

3.1 Column ADC architecture for image sensors
After the 4-transistor-type pixel with buried photodiode was developed, CMOS imager overcame issues about thermal noise and dark current noise; the image quality of the imagers approached that of charge-coupled devices (CCDs). Figure 4 shows a block diagram of a CMOS imager. Almost all imagers use column-parallel ADC architecture for high-speed A/D conversion. Conventionally, a single-slope ADC (SS-ADC) has been used as a small ADC and a simple-column ADC (in Fig. 5). The SS-ADC converts analog signal to a pulse-width modulated (PWM) signal and digitizes the pulse width by using the clock-signal period. However, the SS-ADC requires a $2^n$ conversion time at $n$-bit resolution. Therefore, various methods to speed up the process

![Fig. 4. Block diagram of CMOS imager](image)

![Fig. 5. Circuit configuration of single-slope ADC and working principle](image)
have been proposed. Carried in a phase locked loop (PLL), the generated high-speed clock signal quickly drives SS-ADCs without changes in the circuit structure. Using this scheme, digital correlated double sampling (CDS) was also proposed (in Fig. 6). To obtain the digitized pixel value, the digital CDS performs subtraction reset- and signal-readout conditions with the up-down counter. When used in combination of analog CDS with a column amplifier, noise components of the pixel and the column amplifier can be removed simultaneously. The 1.77 megapixel imager with the PLL, which generates a 2.4 GHz clock signal, achieved a frame rate of 120 fps and data transfer rate of 34.8 Gbps in 2011 [17, 18]. Cyclic ADCs (which repeatedly use one unit of a pipelined ADC) and SAR ADCs have also been used in high-speed column ADCs. The 3.3 megapixel imager with the cyclic ADCs achieved 120 fps and 51.2 Gbps in 2012 [19]. The 1.42 megapixel imager with the SAR ADCs achieved 80 fps in 2013 [20].

3.2 Useful image processing in image sensing

Image-sensing systems perform preprocessing that includes demosaicing, noise reduction, and white balancing, etc. Demosaicing involves reconstructing the RGB values of a pixel from Bayer color space. Recently, local adaptive tone mapping has been used as it is a versatile processing method (in Fig. 7). Local tone mapping is widely applied to high-quality/high-dynamic-range compression, under/overexposure image correction, and local contrast enhancement in vehicle/security camera systems and medical images. In the local tone mapping, individual tone curve function, which is derived from local patch, is applied to each target pixel. Local adaptive tone mapping and associated techniques are explained in detail in Section 3.3 and 3.4. These processes are separated into two groups: multi-layer methods (including Retinex theory) [21, 22] and local histogram equalization (LHE).
3.3 Image correction using multiple layers

In the multi-layer method, the low frequency components of the image, called the base layer, are handled as illuminance; the high frequency components, which approximately correspond to the texture, are separated by filtering (in Fig. 8). As each component is adequately corrected, under/overexposed images are compensated while preserving good contrast. When obtaining the base layer using an isotropic low pass filter (LPF), some artifacts, called the “halo effect”, are generated at the boundary of objects in the corrected images. Thus, an edge-preserving blur filter is used with the multi-layer method. The most popular filter is a bilateral filter which Tomasi et al. proposed in 1998 (in Fig. 9 (a)) [23]. Using spatial weight and range weight, this filter only smoothes groups of pixels which have close luminance values. However, since the filter excessively enhances the edges of objects, exact gradients of
the edges cannot be preserved. Therefore, edge-preserving filters have been rapidly improved in the last few years. He et al. proposed guided filtering in 2010 (in Fig. 9 (b)) [24, 25]. This filter works based on the variance of the image; when the variance of local image is large, the filter recognizes that there is an edge part in the local image and preserves the initial pixel value. Gastol et al. proposed domain-transform filtering in 2011 (in Fig. 9 (c)) [26]. In this filtering technique, distances for gradients of edge and color difference are transformed to the distance in the image space; simple blur filtering is applied to the transformed image space. These filtering techniques preserve the exact gradients of object edges. Moreover, since these are based on 1- or 2-dimensional box filtering, high speed processing without filter-kernel-size dependency can be achieved. Edge preserving filters are useful for various applications such as soft matting, so hardware implementations of these filters are expected.

### 3.4 Local histogram equalization (LHE) based algorithm

Local histogram equalization based local tone mapping converts target pixels by using tone curves constructed from local cumulative histograms. Apical Iridix® [27], which is based on LHE, has achieved a dominant share of local tone mapping; the SW/HW-IP cores are licensed to many companies. In Apical Iridix®, local processing is performed after global tone mapping
(such as by logarithmic conversion). Pixel values are multiplied by Legendre basis functions of luminance domain, and LPF is applied to the multiplied data (in Fig. 10). This processing is the frequency spectrum analysis of the local histogram shape. Then, the local cumulative histogram is directly reconstructed by using the products-sum of the integral form of the Legendre basis functions. By controlling the number of the basis functions, smoothed local cumulated histogram can be obtained without high frequency components of the histogram shape. These cumulative histograms have some ripples, so alpha blending between the smoothed LHE images of the Iridix® and the initial image is used. In short, the Apical Iridix® generates images with enhanced local contrast and globally controlled features (in Fig. 11). When the above process is used for a still image, a frame buffer is required. However, for the movie processing, correlation among frames is strong, so the

![Diagram of processing scheme](image)

**Fig. 10.** Processing scheme of Apical Iridix®

![Input and output images](image)

**Fig. 11.** Processing example of Apical Iridix® (Number of basis = 6, α blending ratio = 50%)
information from previous frames can be used for current frame correction. Therefore, a low-resolution image of the previous frame is stored; the local histogram calculations within the Iridix® are performed on the low-resolution image. Using interpolation, the obtained low-resolution local histograms are adjusted to the resolution of the input/output images and a significant memory use reduction can be achieved in hardware implementation. The LPF in Iridix® hardware is calculated with a 2-D FFT core.

3.5 Other remarkable processing

Depth extraction within image sensing has attracted attention for many years. It is used for domain segmentation, object recognition, 3-D analysis, and refocusing. As for pixel structure, a time of flight (TOF) pixel, which extracts phase information of reflected periodical infrared radiation, dual pixels for phase-contrast auto focusing [28] and stereo matching [29], and light field cameras which store information on multiple directions of light [30], have been developed.

4 Circuit implementation of sensing system

As exact sensing, low power consumption, and network connection are important, circuit design for a sensor network must consider all elements. However, for the combination of imager and image processing, the two parts are fully separated except for simple preprocessing. Therefore, at first, state of the art algorithms that use high-capacity GPU processing are developed. Then, an analysis of the algorithms and research of suitable circuit implementation is conducted. Examples of actual research and development are:

- Computational photography processor [31] using joint bilateral filtering [32]
- Dehazing processor [33] with dark channel prior [34]
- Field-programmable gate array (FPGA) implementation of stereo matching algorithms with AD census [35, 36], etc.

Rithe et al. proposed the processor using joint bilateral filtering (in Fig. 12). This filter uses a guidance image as range weight. For example, using flash images with low noise as the guidance, noisy images of low-light environments can be cleared by effects of low-noise range weight. The processor applied bilateral grid structure, which is approximated algorithm with down sampling and enables fast bilateral filtering. And, it can perform High-Dynamic Range (HDR) imaging, Low-Light Enhanced (LLE) imaging, tone management and glare reduction. For high quality image processing, filtering with a large kernel and/or solving energy optimization problems with iteration processing are used. Therefore, as necessary, the algorithms are approximated; evaluating applicable parallel processing, estimating the number of iteration processes, and memory use reduction become important for circuit implementation.
5 Conclusions

The applications of sensing systems cover very different areas, so this paper followed the linkage between sensors and digital circuits and described two main areas: ADC architecture and digital signal processing. Conventionally, various type ADCs have been used for digitizing sensing values. In low-power ADCs, improvements in the efficiency of SAR ADCs have progressed rapidly. As a robust sensing circuit for harsh environments such as in vehicles, a fully digital ADC architecture “time A/D converter” (TAD) has been proposed. Since the quantization error is transferred to the next conversion in the delay line, so the TAD performs a first-order noise-shaping function. In image sensors, high-speed column ADC architecture with effective CDS scheme works so well. For the combination of imager and image processing, the two parts are fully separated except for simple preprocessing. Particularly, edge preserving filter is useful for various applications such as local tone mapping and soft matting etc., so hardware implementations of these filters are expected.
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