GHOST: Building Blocks for High Performance Sparse Linear Algebra on Heterogeneous Systems

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Abstract While many of the architectural details of future exascale-class high performance computer systems are still a matter of intense research, there appears to be a general consensus that they will be strongly heterogeneous, featuring “standard”
as well as “accelerated” resources. Today, such resources are available as multicore processors, graphics processing units (GPUs), and other accelerators such as the Intel Xeon Phi. Any software infrastructure that claims usefulness for such environments must be able to meet their inherent challenges: massive multi-level parallelism, topology, asynchronicity, and abstraction. The “General, Hybrid, and Optimized Sparse Toolkit” (GHOST) is a collection of building blocks that targets algorithms dealing with sparse matrix representations on current and future large-scale systems. It implements the “MPI+X” paradigm, has a pure C interface, and provides hybrid-parallel numerical kernels, intelligent resource management, and truly heterogeneous parallelism for multicore CPUs, Nvidia GPUs, and the Intel Xeon Phi. We describe the details of its design with respect to the challenges posed by modern heterogeneous supercomputers and recent algorithmic developments. Implementation details which are indispensable for achieving high efficiency are pointed out and their necessity is justified by performance measurements or predictions based on performance models. We also provide instructions on how to make use of GHOST in existing software packages, together with a case study which demonstrates the applicability and performance of GHOST as a component within a larger software stack. The library code and several applications are available as open source.

Keywords Sparse linear algebra · Heterogeneous computing · Software library · Task parallelism · Large scale computing · Data parallelism

1 Introduction and Related Work

1.1 Sparse Solvers on Heterogeneous Hardware

Users of modern supercomputers are facing several obstacles on their way to highly efficient software. Out of those, probably the most prominent is the ever increasing level of parallelism in hardware architectures. Increasing the parallelism on the chips—both in terms of the number of cores as well as inside the core itself—is currently the only way to increase the maximum performance while keeping the energy consumption at a reasonable level. The parallelization of hardware architectures peaks in the use of accelerators, coprocessors, or graphics processing units (GPUs) for general purpose computations. Those devices trade off core sophistication against a very high core count, achieving an extremely high level of parallelism with unmatched peak floating point performance per Watt. As of June 2016, approximately 20 % of all TOP500 [51] systems are heterogeneous and the accelerators in those installations account for almost quarter of the entire aggregated TOP500 performance. This evolution has led to the emergence of a large scientific community dealing with various aspects of accelerator programming and a considerable amount of accelerator-enabled software packages.
However, a fact which is frequently not being considered is that also the CPU part of a heterogeneous system can contribute significantly to a program’s performance. On the other hand, even in simpler CPU-only machines, properties like memory hierarchy, ccNUMA effects and thread affinity play an important role in high performance code development. The addition of accelerators further increases the level of complexity in the system topology. At the same time, the world’s largest compute clusters exhibit a steady growth in terms of cores and nodes as a result of continuously increasing requirements from application users. This poses challenges to algorithms and software in terms of scalability.

There is a wide range of applications which require computation with very large sparse matrices. The development of sparse linear and eigenvalue solvers that achieve extreme parallelism therefore remains an important field of research. One example is the analysis of novel materials like graphene [37] and topological insulators [45] in the field of solid state physics, which is a driving force in the GHOST development within the ESSEX project [1]. These eigenvalue problems require the computational power of full petascale systems for many hours, so it is crucial to achieve optimal performance at all levels.

Recent work in the area of sparse matrix algorithms can roughly be subdivided into three categories. Methods that increase computational intensity (i.e. reduce/avoid communication), methods that hide communication by overlapping it with computation, and fully asynchronous algorithms. To the first category belong, among others, block Krylov methods and the communication avoiding GMRES (CA-GMRES [13]) method, which require optimized block vector kernels. The second category includes the pipelined CG and GMRES methods [19]. An example for the third category is the asynchronous ILU preconditioner by Chow and Patel [11]. Methods from the latter two categories benefit from an easy-to-use tasking model that delivers high performance. The novel implementation of ILU methods in [11] replaces the poorly scaling forward/backward substitution by a matrix polynomial, increasing the performance requirements of the sparse matrix-vector multiplication in preconditioned Krylov methods.

1.2 Related Work

There is a large interest in efficient heterogeneous software driven by the developments in modern supercomputer architectures described above. Many efforts follow a task-parallel approach, which strives to map a heterogeneous workload to heterogeneous hardware in an efficient way. A prominent software package implementing task-parallel heterogeneous execution is MAGMA [28]. A major drawback of MAGMA is the absence of built-in MPI support, i.e., users have to implement MPI parallelism around MAGMA on their own. Under the hood, MAGMA uses the StarPU runtime system as proposed by Augonett et al. [3] for automatic task-based work scheduling on heterogeneous systems. Another significant attempt towards heterogeneous software is ViennaCL [42]. Being based on CUDA, OpenCL or OpenMP, this software package can execute the same code on a wide range of compute architectures. However, as in MAGMA, concurrent use of different architectures for a single operation is
not supported. Besides, ViennaCL has limited support for complex numbers, which is problematic for many applications. The same applies to the C++ framework LAMA [26], a library based on MPI+OpenMP/CUDA with special focus on large sparse matrices. PETSc [6] is an MPI-parallel library for the scalable solution of scientific applications modeled by partial differential equations. Its intended programming model is pure MPI, with MPI+X support for GPUs (‘X’ being CUDA or OpenCL) and some limited support for threading. It also lacks support of heterogeneous computation of single operations. Another library containing sparse iterative solvers and preconditioners is PARALUTION [35]. However, the multi-node and complex number support is restricted to the non-free version of this software. The Trilinos packages Kokkos and Tpetra [4] implement an MPI+X approach similar to the one used in GHOST. Being implemented in C++, they clearly separate the MPI level (Tpetra package) from the node level (Kokkos package), whereas GHOST can benefit from tighter integration for, e.g., improved asynchronous MPI communication (cf. Sect. 4.2). In Sect. 6 we will provide a performance comparison of GHOST vs. Trilinos for an eigenvalue solver.

While all of these libraries certainly improve the accessibility of heterogeneous hardware to a wide range of applications, they do not fit our purpose of extreme scale eigenvalue computations in an optimal way. In particular, we believe that a single library for building blocks integrating well-tuned kernels, communication on all levels and good performance on heterogeneous systems ‘out of the box’ is key to satisfying the needs of scientists who are trying to tackle problems at the edge of ‘what can be done’.

1.3 Contribution

In this work, we present the software package GHOST (General, Hybrid and Optimized Sparse Toolkit). As summarized in Sect. 1.2, there is a range of efforts towards efficient sparse linear algebra on heterogeneous hardware driven by modern hardware architectural developments. GHOST can be classified as an approach towards a highly scalable, and truly heterogeneous sparse linear algebra toolkit with a key target in the development process being optimal performance on all parts of heterogeneous systems. In close collaboration with experts from the application side we focus on a few key operations often needed in sparse eigenvalue solvers and provide highly optimized and performance-engineered implementations for those. We show that disruptive changes of data structures may be necessary to achieve efficiency on modern CPUs and accelerators featuring wide single instruction multiple data (SIMD) units and multiple cores.

One may argue about whether performance should be the primary goal in a computational science and engineering (CS&E) software library and whether it is worth the effort to optimize a few core operations for a two-digit percentage gain in performance. Our efforts are targeted at large-scale supercomputers in the petaflop range and beyond, and computing time is a valuable resource there. Even a performance gain below an order of magnitude can become significant in terms of time, energy, and money spent on the large scale. Needless to say, the kernels we provide can be used on smaller clusters or single workstations as well. GHOST does not give up generality or
extensibility for this purpose, rather we aim to provide performance-optimized (guided by performance models) kernels for some commonly used algorithms (e.g., the kernel polynomial method [25], the block Jacobi-Davidson method [41] or Chebyshev filter diagonalization [38]). The successful implementations of these methods (which are very popular in fields like material physics and quantum chemistry) will serve as blueprints for other techniques such as advanced preconditioners needed in other CS&E disciplines. In the application areas we consider right now, methods such as incomplete factorization or multigrid can usually not be applied straightforwardly. The matrices that appear may not have an interpretation as physical quantities discretized on a mesh, they may be completely indefinite, and they may have relatively small diagonal entries and/or random elements [16].

A key feature of GHOST is the transparency to the user when it comes to heterogeneous execution. In contrast to other heterogeneous software packages (cf. Sect. 1.2), GHOST uses a data-parallel approach for work distribution among compute devices. While a task-parallel approach is well-suited for workloads with complex dependency graphs, the data-parallel approach used by GHOST may be favorable for uniform workloads (i.e., algorithms where all parts have similar resource requirements) or algorithms where an efficient task-parallel implementation is unfeasible. On the process level, GHOST’s tasking mechanism still allows for flexible work distribution beyond pure data parallelism.

GHOST unifies optimized low-level kernels whose development process is being guided by performance modelling into a high-level toolkit which allows resource-efficient execution on modern heterogeneous hardware. Note that for uniform workloads, performance models like the roofline model [54] are a suitable tool to check an implementation’s efficiency. In recent work, GHOST has proven to scale up to the petaflop level, extending the scaling studies presented in [25]. A list of challenges we are addressing specifically and the corresponding sections in this paper can be given as follows:

(i) Emerging asynchronous sparse solver algorithms are in need of a light-weight, affinity-aware and threading-friendly task-based execution model. In this context, the high relevance of OpenMP should be noted, which requires the tasking model to be compatible to OpenMP-parallel codes. See Sect. 4.2.

(ii) Existing software rarely uses all components of heterogeneous systems in an efficient manner. See Sects. 4.1 and 5.1.

(iii) The potential performance of compute libraries is often limited by the requirement of high generality, leading to a lack of application-specific kernels. See Sect. 5.3.

(iv) The possibilities for application developers to feed their knowledge into compute libraries for higher performance are often limited. See Sect. 5.4.

(v) The applicability of optimization techniques like vector blocking is often limited due to restrictions in existing data structures. Fundamental changes to data structures are often hard to integrate in existing software packages. See Sects. 5.2 and 5.1.

GHOST is available as a BSD-licensed open source download [18]. Along with it, a list of sample application based on GHOST (e.g., a Conjugate Gradient solver...
Table 1  Relevant properties of all architectures used in this paper

| Alias | Model | Clock (MHz) | SIMD (bytes) | Cores/ SMX | b (GB/s) | p^{\text{peak}} (Gflop/s) |
|-------|-------|-------------|--------------|------------|----------|--------------------------|
| CPU   | Intel Xeon E5-2660 v2 | 2200 | 32 | 10 | 50 | 176 |
| GPU   | Nvidia Tesla K20m | 706 | 128…512* | 13 | 150 | 1174 |
| PHI   | Intel Xeon Phi 5110P | 1050 | 64 | 60 | 150 | 1008 |

The maximum attainable memory bandwidth as measured with any of the STREAM [30] benchmarks is denoted by $b$ and $p^{\text{peak}}$ is the theoretical peak floating point performance. Turbo mode was activated on the CPU and the GPU was configured with ECC enabled.

* SIMD processing is done by 32 threads. Hence, the SIMD width in bytes depends on the data type in use: 128 bytes is valid for 4-byte (single precision floating point) data while 512 bytes corresponds to complex double precision data.

and a Lanczos eigensolver) can be downloaded. On top of that, the iterative solver package and sister project of GHOST named PHIST [36] can use GHOST to execute more sophisticated algorithms like, e.g., the block Jacobi-Davidson eigensolver as described in [41], and blocked versions of the MinRes and GMRES linear solvers.

1.4 Testbed

All experiments in this paper have been conducted on the Emmy cluster located at the Erlangen Regional Computing Center. Table 1 summarizes the hardware components used in this cluster. They are connected with a QDR InfiniBand network. The Intel C/C++ compiler version 14, Intel MPI 4.1, and CUDA version 6.5 have been used for compilation. Intel MKL 11.1 was used as the BLAS library on the CPU. Test matrices are denoted by the name under which they can be found in the University of Florida sparse matrix collection [12] unless noted otherwise.

2 Design Principles

2.1 Supported Architectures and Programming Models

Many modern compute clusters comprise heterogeneous nodes. Usually, such nodes consist of one or more multi-core CPUs and one or more accelerator cards. In the TOP500 [51] systems of June 2016, 95 % of all accelerator performance stems from NVIDIA Fermi/Kepler GPUs or Intel Xeon Phi (to be called “PHI”) coprocessors. Hence, we decided to limit the accelerator support in GHOST to modern NVIDIA GPUs and Intel coprocessors. Instead of implementing support for any kind of hardware architecture, our primary goal is to stick to the dominant platforms and to develop properly performance-engineered code for those.

Although GPUs and PHIs share the name accelerators, there are significant differences in how those devices are operated. GPUs can only be driven in accelerator mode, i.e., data transfers and compute kernels must be launched explicitly from a main program running on a host CPU. The PHI can be operated in accelerator mode, too.
However, in addition to this, the PHI can also be driven in *native mode*, i.e., in the same way as a multicore CPU would be used. In GHOST only native execution on the PHI is supported, i.e., the PHI hosts its own process. Hence, the PHI can be considered as a CPU node on its own. With regard to the PHI as a multi-(many-)core CPU, it has to be taken into account that serial code may run at very low performance due to its very simple core architecture.

### 2.2 Parallelism in GHOST

For illustration of the principles, we consider a heterogeneous node as shown in Fig. 1. This node contains two multicore CPU sockets with ten cores and two-way hyper-threading each. In total, there are 20 hardware threads or processing units (PUs) available per socket. In addition to that, one GPU and one PHI are attached to the node as accelerators. Note that a node with two different accelerator architectures is unlikely to be installed in a production system.

In terms of parallelization, GHOST implements the “MPI+X” paradigm, i.e., coarse-grained parallelism is done by means of MPI accompanied with fine-grained and device-specific parallelization mechanisms (“X”). One may certainly omit the “X” part and go with plain MPI altogether if the hardware can be efficiently utilized in this way; the plain fact that modern hardware exhibits complex topologies does not mean that a hybrid programming model is required in all cases, and it may sometimes even be counterproductive. However, interesting opportunities in terms of load balancing, additional levels of parallelism, communication hiding, etc., arise from combining MPI with a threading model [40]. This is why GHOST supports OpenMP for the “X” component on CPUs. Further down the hardware hierarchy, implicit vectorization by compiler-friendly code and pragmas as well as explicit vectorization using Single Instruction Multiple Data (SIMD) intrinsics provide efficient single-threaded code. On Nvidia GPUs, CUDA is used as the “X” parallelization layer.

In general, parallelism in compute applications can be categorized into data and task parallelism. The term data parallelism describes a number of workers operating on the same data set, each having assigned a certain amount of work. The term task
parallelism describes workers working on independent tasks at the same time. GHOST implements both data (between processes) as described in Sect. 4.1 and task parallelism (inside a process) as analyzed in Sect. 4.2.

In many cases, algorithms from sparse linear algebra are centered around a single and potentially large sparse system matrix. Hence, the distribution of work in GHOST is done in a matrix-centered way. More precisely, the system matrix and corresponding vectors are distributed row-wise across the MPI processes. The amount of work per process can either be expressed by the number of rows or the number of nonzero elements. Details on the implementation are given in Sect. 4.1.

3 Available Data Structures

3.1 Sparse Matrices

GHOST supports the SELL-C-σ sparse matrix storage format as introduced in [25]. More details on sparse matrix storage are given in Sect. 5.1. As mentioned in Sect. 2.2, the sparse system matrix is the central data structure in GHOST.

A significant performance bottleneck for highly scalable sparse solvers may be the generation of the system matrix. In GHOST this matrix can be stored in a file, either in the Matrix Market [29] format or a binary format which resembles the CRS data format. However, the scalability of this approach is intrinsically limited. The preferred method of matrix construction in GHOST is via a callback function provided by the user, which allows to construct a matrix row by row. The function must have the following signature:

```c
int mat(ghost_gidx row, ghost_lidx *len, ghost_gidx *col, void *val, void *arg);
```

GHOST passes the global matrix row to the function. The user should then store the number of non-zeros of this row in the argument rowlen and the column indices and values of the non-zeros in col and val. Any further arguments can be passed in arg. The maximum number of non-zeros must be set in advance such that GHOST can reserve enough space for the col and val arrays.

There are several reasons which make it necessary to permute rows of the sparse system matrix. A global (inter-process) permutation of matrix rows can be applied in order to minimize the communication volume of, e.g., the sparse matrix vector multiplication (SpMV) kernel. Currently, GHOST can be linked against PT-SCOTCH [10] or Zoltan [15] for this purpose. Row length information and column indices are passed to the third-party library which results in a permutation vector on each process containing global indices. Afterwards, the matrix is assembled on each process according to the global permutation. In addition to the global permutation, a local (intra-process) permutation can be applied, e.g., to minimize the storage overhead of the SELL-C-σ sparse matrix format (cf. Sect. 5.1). Further local permutations can be applied based on matrix bandwidth reduction for better cache utilization (using the parallel bandwidth reduction algorithms of SpMP [47]) or row coloring to enable parallelization of, e.g., the Kaczmarz [23] algorithm or a Gauß-Seidel smoother as present in the HPCG benchmark (using ColPack [17]). Note that an application-based
permutation, e.g., by optimizing the numbering of nodes in a mesh-based problem, usually leads to better overall performance and should be preferred over an a posteriori permutation. In GHOST the former can be achieved by a sensible implementation of the matrix construction via the callback interface on the user side.

### 3.2 Dense Matrices

GHOST is a framework for sparse linear algebra. Dense matrices are mainly occurring as dense vectors (dense matrices with a single column) or blocks of dense vectors (to be referred to as block vectors). Section 5.2 will cover the aspect of block vectors in more detail. Block vectors can be considered as tall and skinny dense matrices, i.e., dense matrices with a large row count (in the dimension of the sparse system matrix) but relatively few (at most a few hundred) columns. Furthermore, a dense matrix can be used to represent small local or replicated matrices, e.g. the result of an inner product of two (distributed) block vectors.

Dense matrices can be chosen to be stored in a (locally) row- or column-major manner. In many cases, row-major storage (i.e., interleaved storage of block vectors) yields better performance and should be preferred (cf. Sect. 5.2). On the other hand, column-major storage may be required for easy integration of GHOST into existing software. GHOST offers mechanisms to change the storage layout either in-place or out-of-place, while copying a block vector.

Instead of allocating its own memory, a dense matrix can also be created as a view of another dense matrix or a view of arbitrary data in memory. This makes it easily possible to let a function work on a sub-matrix or a subset of vectors in a larger block vector without having to copy any data. Additionally, by viewing “raw” data in memory it is possible to integrate GHOST into existing codes (cf. Sect. 6). A potential disadvantage of using non-GHOST data structures is the violation of data alignment which may result in a performance loss. GHOST implements different kinds of views. In general, compact views allow vectorized computation with the matrix data. This is not the case for scattered views due to “gaps” in the memory layout in the leading dimension, e.g. caused by columns not included in a row-major view. In this case, it may be favorable to create a compact clone of the scattered view before executing the computation.

### 4 Runtime Features

In this section we describe runtime features which are deeply woven into the software architecture and constitute GHOST’s unique feature set. In contrast to the so-called performance features which will be introduced in Sect. 5, they are fundamentally built into the library and hard to apply to other approaches.

#### 4.1 Transparent and Data-Parallel Heterogeneous Execution

The distribution of work among the heterogeneous components is done on a per-process basis where each process (MPI rank) is bound to a fixed set of PUs. This allows flexible scaling and adaption to various kinds of heterogeneous systems. The
sets of PUs on a single node are disjoint, i.e., the compute resources are exclusively available to a process. For the example node shown in Fig. 1, the minimum amount of processes for heterogeneous execution on the full node is three.

Application developers are frequently confused by the ccNUMA memory structure of modern compute nodes and how to handle it to avoid performance penalties. Although the required programming strategies are textbook knowledge today, establishing perfect local memory access may be tricky if a multithreaded process spans multiple ccNUMA domains even if proper thread-core affinity is in place and parallel first-touch initialization is performed [21]. A simple way to avoid ccNUMA problems is to create one process per multicore CPU socket, which would result in a process count of four as illustrated for the example node in Fig. 1. Processes 0 and 2 cover one CPU socket each. Process 1 drives the GPU. As this has to be done in accelerator mode, this process also occupies one core of the host system. Note that this core is located on the socket whose PCI Express bus the GPU is attached to and thus has to be subtracted from Process 0’s CPU set. Process 3 is used for the PHI. The process can directly be located on the accelerator which is used in native mode, i.e., no host resources are used for driving the PHI.

An intrinsic property of heterogeneous systems is that the components differ in terms of performance. For efficient heterogeneous execution it is important that the performance differences get reflected in the work distribution. In GHOST the underlying sparse system matrix gets divided on a row-wise basis among all processes. For example, if component A is expected to have twice the performance of component B, process A will get assigned a twice as large chunk (either in terms of rows or in terms of nonzero elements) of the system matrix as process B.

Figure 2 illustrates the row-wise distribution of a sparse matrix among the example processes shown in Fig. 1. As the performance of sparse solvers is often bound by main memory bandwidth, the device-specific maximum attainable bandwidth, as given in Table 1, has been chosen as the work distribution criterion in this example. Note that an arbitrary work share for each process/architecture can easily be specified at runtime.

For each numerical function in the GHOST library, implementations for the different architectures are present. However, the choice of the specific implementation of a

![Fig. 2](https://example.com/figure2.png)

**Fig. 2** Heterogeneous row-wise distribution of a sparse matrix. Step (1) is the determination of process weights according to the device’s peak memory bandwidths. In step (2), a partial sparse matrix is created on each process. In order to avoid integer overflows and storage overhead in the communication buffers, the column indices of elements in the remote matrix part (pale colors) are compressed in step (3) (Color figure online)
kernel does not have to be made by the user. Consequently, in almost all usage cases, no changes to the code are necessary when switching between different hardware architectures. An exception of this rule is, e.g., the creation of a dense matrix view from plain data: If the dense matrix is located on a GPU, the plain data must be valid GPU memory. Internally, each process gets assigned a type which allows to define the compute platform used by an executable. Valid types are CPU and GPU. The type can be set explicitly at runtime either via API calls or by specifying an environment variable. If multiple processes are launched on a node containing CPUs and GPUs, the type gets selected automatically if not explicitly specified. In this case, Process 0 is always of type CPU, initially covering all CPUs in the node. Processes 1 to N are of type GPU where N is equal to the number of GPUs attached to the node. For each GPU process getting added to a node, a small CPU set (usually a single core) gets subtracted from Process 0’s resources. The addition of any more than \((1 + \text{“Number of GPUs”})\) processes to a node causes a division of Process 0’s CPU set into equally sized smaller CPU sets. A good number of processes to put on a node is \(\text{“Number of CPUs”} + \text{“Number of GPUs”}\), which is an easy way to avoid NUMA locality problems by having one process per CPU socket.

In the following we demonstrate the heterogeneous execution capabilities on our example node using a simple benchmark program which measures the SpMV performance for a given matrix and storage format (downloadable from the GHOST website [18]). In this case, we used the Janna/ML_Geer matrix (dimension \(n = 1,504,002\), number of non-zeros \(n_{nz} = 110,686,677\)) stored in SELL-32-1. The program performs 100 SpMV operations and reports the average performance. Performance will be reported in Gflop/s, with 1 Gflop/s corresponding to a minimum memory bandwidth of 6 GByte/s. This relation is founded on the minimum code balance of the SpMV kernel. If we want to perform computations on one device only and use one process per CPU socket, the type has to be set explicitly and a suitable number of processes has to be launched on the host using the \(-np\) flag. Automatic process binding by the MPI startup script should be suppressed with \(-nopin\) to avoid conflicts with GHOST’s resource management.

\[
\text{> GHOST\_TYPE=CPU mpirun -nopin -np 2 ./spmvbench -m ML\_Geer.mtx -f SELL-32-1}
\]

\[
\text{[GHOST] PERFWARNING: The number of MPI ranks (2) on this node is not optimal!}
\]

\[
\text{Suggested number: 3 (2 NUMA domains + 1 CUDA device)}
\]

\[
\text{[GHOST] PERFWARNING: There is 1 Xeon Phi in the set of active nodes but only 0 are used!}
\]

\[
15.26 \text{ Gflop/s}
\]

\[
\text{> GHOST\_TYPE=GPU ./spmvbench -m ML\_Geer.mtx -f SELL-32-1}
\]

\[
22.64 \text{ Gflop/s}
\]

The performance warnings (omitted on subsequent occurrences) issued by GHOST indicate that the node is not used to its full extent. The suggested process count of three is in accordance with the knowledge about the node architecture; each node contains two CPU sockets and one GPU. The Intel PHI attached to this node has to be considered as a node on its own. The achieved performance matches the prediction of a simple roofline model for SpMV on the respective architecture. GHOST can determine process weights in heterogeneous runs automatically based on micro-benchmarks. Due to the bandwidth-bounded nature of sparse matrix algorithms, the STREAM [30] copy
benchmark is a natural choice which is also used in GHOST. Starting the program with the suggested number of three processes on the node yields the following:

```bash
> mpirun -nopin -np 3 ./spmvbench -v -m ML_Geer.mtx -f SELL-32-1
[HOST] PE0 INFO: Setting GHOST type to CPU.
[HOST] PE1 INFO: Setting GHOST type to GPU.
[HOST] PE2 INFO: Setting GHOST type to CPU.
[HOST] PE0 INFO: Setting weight to 41.6 according to STREAM copy bandwidth!
[HOST] PE1 INFO: Setting weight to 148.5 according to STREAM copy bandwidth!
[HOST] PE2 INFO: Setting weight to 39.9 according to STREAM copy bandwidth!
26.81 Gflop/s
```

The information log messages indicate that the process types and weights have automatically been set as described above. The achieved performance is less than the accumulated single-device performances. This is due to the MPI and CUDA communication of input vector data which is done in each SpMV iteration and non-optimal load balancing. The latter factor can be alleviated by assigning process weights according to the actual single-device SpMV performance (instead of automatic weights based on the copy bandwidth) with the `-w` flag. For testing purposes, it is furthermore possible to suppress the communication by selecting an appropriate “pseudo SpMV” routine with the `-s nocomm` flag. Note that this does not give the correct result for the SpMV operation on multiple processes. Without communication, the heterogeneous performance approximately sums up to the accumulated single-device performances. In order to include the node’s PHI in the computation, the library and executable have to be compiled for the MIC architecture separately. A machine file or environment settings must be prepared for starting the correct executable on each process. Using all parts of the heterogeneous node now yields the following:

```bash
> mpirun -nopin -np 4 ./spmvbench -m ML_Geer.mtx -f SELL-32-1 -s nocomm
[HOST] PE0 INFO: Setting weight to 41.6 according to STREAM copy bandwidth!
[HOST] PE1 INFO: Setting weight to 148.5 according to STREAM copy bandwidth!
[HOST] PE2 INFO: Setting weight to 39.9 according to STREAM copy bandwidth!
[HOST] PE3 INFO: Setting weight to 143.9 according to STREAM copy bandwidth!
54.79 Gflop/s
```

The total node performance without communication of almost 55 Gflop/s indicates a good use of the aggregated memory bandwidth of all resources. Note that the inclusion of the PHI barely leads to a performance benefit over the CPU+GPU run for the real SpMV operation and manual weights. This is due to the small amount of work on each device and an increasing dominance of communication over the slow PCI express bus as a result of this (i.e., strong scaling). The impact of communication may be reduced by matrix re-ordering (cf. Sect. 3.1) or more sophisticated communication mechanisms (using GPUdirect, pipelined communication, etc.).

### 4.2 Affinity-Aware Resource Management

Although GHOST follows a data-parallel approach across processes for heterogeneous execution, work is organized in tasks on the process level. The increasing asynchronic-
ity of algorithms together with the necessity for sensible hardware affinity and the avoidance of resource conflicts constitute the need for a unit of work which is aware of the underlying hardware has to be used: a GHOST task. Affinity and resource management is implemented by means of the \texttt{hwloc} library \cite{9} which is, besides a BLAS library, the only build dependency of GHOST.

There are existing solutions for task parallelism. Apart from the ones named in Sect. 1.2, OpenMP tasks or Intel’s Threading Building Blocks can be mentioned here. However, a crucial requirement in the design phase of GHOST was to support affinity-aware OpenMP parallelism in user-defined tasks. As we could not find a lightweight existing solution which meets our requirements, we decided to implement an appropriate tasking model from scratch. For example, both Intel TBB and Cilk Plus warn about using those frameworks together with OpenMP in their user manuals. This is due to potential performance issues caused by core over-subscription. As OpenMP is in widespread use in scientific codes, this limitation disqualifies the integration of TBB and Cilk Plus tasks for many existing applications. Note that GHOST tasks lack a list of features compared to existing solutions, such as intelligent resolution of dependencies in complex scenarios. Yet, for most of our usage scenarios they work well enough. In our opinion, a holistic performance engineering approach is a key to optimal performance for complex scenarios. Thus, we decided to make the resource management a part of the GHOST library.

Figure 3 visualizes the lifetime of an application using a GHOST task to perform some work asynchronously. Generally speaking, a task’s work can be an arbitrary user-defined function in which OpenMP can be used without having to worry about thread affinity or resource conflicts. The threads of a task are pinned to exclusive compute resources, if not specified otherwise. GHOST tasks are used in the library itself, e.g., for explicitly overlapping communication and computation in a parallel SpMV (see below). However, the mechanism is designed in a way that allows easy integration of the tasking capabilities also into user code. The user-defined callback function containing the task’s work, its arguments, the number of threads to execute this task and the preferred NUMA node for execution have to be provided to GHOST. The specification of the NUMA node is important for situations where different tasks work with the same data in main memory in a process which spans several NUMA nodes. In this situation, and assuming a NUMA first touch policy, one can enforce a task which works on specific data to run on the same NUMA node as the task which initialized this data. Due to physical persistence of OpenMP threads, a parallel region in the task function will be executed by the same threads as those which have been pinned by GHOST. Note that this persistence is not required by any standard. However, our experiments have shown that the most relevant OpenMP implementations GOMP and Intel OpenMP work like this, which makes the assumption of persistent OpenMP threads realistic in practice. Assuming that this assumption is invalid, one could still confine the children of a shepherd thread to, e.g., a specific NUMA domain, by setting the shepherd thread’s affinity. This is possible since children created via \texttt{fork()} inherit their parent’s CPU affinity mask. Note that this fallback mechanism involves a coarser level of affinity than the original approach and might be inappropriate for scenarios where a task spans several physical affinity (e.g., NUMA) domains.
In the initialization phase GHOST creates a number of shepherd threads which will immediately wait on a condition. As a task gets enqueued, this condition gets signalled which causes an arbitrary shepherd thread to be woken up. The `enqueue()` function returns immediately. A decision whether this task can be executed is now made by the shepherd thread based on the task’s resource requirements. In case the task can be executed, an initial OpenMP parallel region is opened in which all threads of the task get pinned to their exclusive PU and each PU is marked as busy. The task’s work function now is called by the shepherd thread and is executed in parallel to the user code which followed the call to `enqueue()`. After completion of the task’s work, the PUs are freed, the threads are unpinned and it is checked whether another task can be executed using the newly freed resources. At finalization time, the shepherd threads are terminated.
It is possible to create nested tasks, i.e., tasks running inside other tasks. A parent task can be configured such that none of its children steals resources of it. Otherwise, it is expected that parents wait for their child tasks and thus, the children can occupy the parent’s resources. In the simplest case, there is only a single task which includes all the work done in the entire application. This “main task” should be created for all GHOST applications for controlled thread placement and the avoidance of resource conflicts. Moreover, while conducting performance analyses using hardware performance counters, controlled placement of threads is inevitable for making sense of the measurements. On top of this, tasks can be used to implement task-level parallelism by having several tasks running concurrently. Due to the fact that starting a task is a non-blocking operation, asynchronous execution of work is inherently supported by GHOST tasks. Normally, each task uses its own set of resources (= PUs) which is not shared with other tasks. However, a task can also be requested to not reserve any compute resources. The PUs available to GHOST can be set by the user. This feature can be used, e.g., for integration with third-party resource managers that deliver a CPU set to be used.

A realistic usage scenario for task level parallelism is communication hiding via explicit overlap of communication and computation. This can be done, e.g., in a parallel SpMV routine, which will be called task-mode SpMV. In this, a main task is being split up into two child tasks. Communication and local computation are being overlapped explicitly. In principle, this could also be done via non-blocking MPI calls. However, experience has shown that even nowadays some MPI implementations do not fulfill non-blocking communication requests in an asynchronous way. This has been discussed in various publications where also several attempts to solving this problem have been proposed by, among others, Wittmann et al. [55] and Denis [14]. Thus, in order to create an assured overlap, independent of the MPI library, GHOST’s tasking mechanism could be used. Note that in many application scenarios based on GHOST tasks, an MPI implementation supporting the \texttt{MPI\_THREAD\_MULTIPLE} compatibility level is required.

Figure 4 depicts the potential performance gain by using GHOST tasks. In this example, 100 parallel SpMV operations on 4 CPU-only compute nodes using the \texttt{vanHeukelum/cage15} test case ($n=5,154,859, n_{nz}=99,199,551$) stored in SELL-
32-1024 have been performed. Note that both overlapped variants require a splitting of the process-local matrix into a local and a remote part, where the remote part contains entries with column indices who require communication of input vector data. It can be observed that overlapping communication and computation pays off in this case. The runtime for the two overlapped variants is significantly lower than for the non-overlapped variant. Note that this may not always be the case: The overlapped versions require the result vector to be written twice and the cost of this may be higher than the benefit from communication hiding. The MPI library apparently features asynchronous point-to-point communication routines for this problem. The execution time for overlapped local computation and communication indicates that those operations are really overlapping. Note that this may not be the case in general, even for this MPI library. It is as well possible that the communication volume is below the “eager limit” and larger messages would not be transferred asynchronously. Although one would not expect the “GHOST overlap” variant to perform any better than the MPI-overlapped variant, the execution time for local computation and communication is lower for the version using GHOST tasks. This performance benefit of GHOST can be explained by its explicit thread placement.

5 Performance Features

In this section we present several features of GHOST that constitute a unique feature set leading to high performance for a wide range of applications. The goal of GHOST is neither to provide a “Swiss army knife” for sparse matrix computations nor to re-invent the wheel. Instead, existing implementations are used and integrated into the GHOST interface whenever possible and feasible. In contrast to the runtime features presented in Sect. 4, the described performance features may be available in other libraries as well. In order to justify their implementation in GHOST, short benchmarks or performance models will be shown to demonstrate the potential or measurable benefit over standard solutions.

5.1 Sparse Matrix Storage

For the SpMV operation, the choice of a proper sparse matrix storage format is a crucial ingredient for high performance. In order to account for the heterogeneous design of GHOST and simplify heterogeneous programming, SELL-C-\(\sigma\) is chosen to be the only storage format implemented in GHOST. This is no severe restriction, since SELL-C-\(\sigma\) can “interpolate” between several popular formats (see below). We briefly review the format here. A detailed and model-guided performance analysis of the SpMV kernel using the SELL-C-\(\sigma\) format can be found in [24].

SELL-C-\(\sigma\) features the hardware-specific tuning parameter \(C\) and the matrix-specific tuning parameter \(\sigma\). The sparse matrix is cut into chunks, each containing \(C\) rows where \(C\) should be a multiple of the hardware’s SIMD width. In a heterogeneous environment, the relevant SIMD width should be the maximum SIMD width over all architectures. For instance, considering our example node’s properties as given in Table 1 and using 4-byte values (single precision) and indices, the minimum value of
C should be $C_{\text{min}} = \left[ \max(32; 64; 128) \right]/4 = 32$. The rows in a chunk are padded with trailing zeros to the length of the chunk’s longest row. The chunk entries are stored column-/diagonal-wise. Additionally, in order to avoid excessive storage overhead for matrices with strongly varying row lengths, $\sigma$ rows are sorted according to their nonzero count before chunk assembly. As this is a local operation, it can be trivially parallelized (which is also done in GHOST). Note that, due to its general formulation, a range of further storage formats can be represented by SELL-$C-\sigma$: SELL-1-1 is similar to CSR/CRS, SELL-$n$-1 matches ITPACK/ELLPACK [34], and SELL-C-1 with $C < n$ corresponds to Sliced ELLPACK [31]. Thus, a considerable selection of known sparse matrix storage formats is supported by GHOST. A single storage format for all architectures greatly facilitates truly heterogeneous programming and enables quick (matrix) data migration without conversion overhead. In [24] we demonstrate that the performance of the SELL-$C-\sigma$ SpMV is on par with or better then the vendor-supplied libraries Intel MKL and NVIDIA cuSPARSE using their device-specific sparse matrix storage formats (CRS in MKL and HYB in cuSPARSE) for most test matrices.

For easy integration in existing software stacks, GHOST allows to construct a SELL-$C-\sigma$ matrix from raw CRS data, i.e., row pointers, column indices, and values. A common case in CS&E applications is the subsequent appearance of multiple sparse matrices with the same sparsity pattern but different values. Let us assume that we want to use GHOST and SELL-$C-\sigma$ for computations with a CRS matrix obtained from another source. Obviously, gathering row lengths and column indices as well as the assembly of communication data structures and permutation vectors only has to be done for the first read-in in this case. Given the ML_Geer matrix (cf. Sect. 4.1) present in CRS, we want to perform SpMV using GHOST with SELL-32-128 on two CPU sockets with one MPI rank each. We find that an initial complete construction of this matrix in GHOST (including communication buffer setup and SELL permutation) costs as much as 48 SpMV operations. Note that the communication buffer setup, which has to be done independently of the library or the sparse matrix format, accounts for 78% of the construction time. Each subsequent matrix construction only needs to update the matrix values. Hence, all values need to be read from the CRS data and written to the SELL-$C-\sigma$ matrix. Taking into account the additional read operation due to the write-allocate of the SELL-$C-\sigma$ matrix, we have at least $3 \times n_{nz}$ matrix elements to transfer. The relative cost depends on the matrix data type. Considering double precision data (and 32-bit indices), subsequent CRS-to-SELL-$C-\sigma$ conversions should cost as much as two SpMV operations. This performance can also be observed in GHOST. A possible future feature may be sparse matrix views. Using a view, a SELL-1-1 matrix could just point to existing CRS data and GHOST could be used for computation with existing matrices at no conversion cost.

GHOST differentiates between local and global indices. Even for sparse system matrices of moderately large size, it may be necessary to have 64-bit integer numbers for global indices. However, for the process-local part, 32-bit integers may still be sufficient. As data movement should be minimized, especially for (often bandwidth-bound) sparse solvers, it is possible to configure GHOST with 64-bit indices for global quantities (ghost_gidx) and with 32-bit indices for local quantities (ghost_lidx). Thus, the column and row indices of the entire process-local sparse matrix can be
stored using 32-bit integers. Compression of the remote column indices as shown in Fig. 2 is inevitable in this case. Considering the minimum amount of data transfers for the SpMV operation, using 32-bit instead of 64-bit column indices for the sparse matrix results in a reduction of data transfers between 16% (complex double precision data) and 33% (single precision data).

5.2 Block Vectors

The architectural performance bottleneck for many sparse linear algebra algorithms is the main memory bandwidth. Hence, reducing the movement of data through the memory interface often improves performance. One well-known way to achieve this is to process multiple vectors at once in a SpMV operation if allowed by the algorithm. Classic block algorithms are, e.g., the block Conjugate Gradient (CG) method proposed by O’Leary et al. [33] and the block GMRES method introduced by Vital [52]. The continued relevance of this optimization technique is seen in recent publications, e.g., by Röhrig-Zöllner et al. [41] in which the authors present a block Jacobi-Davidson method. Vector blocking is also very relevant in the field of eigenvalue solvers for many inner eigenpairs. For example, the FEAST algorithm [39] and Chebyshev filter diagonalization [44] profit from using block vector operations. Basic work on potential performance benefits from using block vectors has been conducted by Gropp et al. [20], where a performance model for the Sparse Matrix Multiple Vector Multiplication algorithm (SpMMV) has been established. In SpMMV, row-major (i.e., interleaved) storage of block vectors is often preferred over column-major storage as it brings a more favorable memory access pattern and higher performance (see, e.g., [41] for benchmark results on this topic.) Support for block vectors has been implemented for many mathematical operations in GHOST.

Generally speaking, block vectors resemble tall and skinny dense matrices, i.e., matrices with many rows and few columns. Although they are represented by general dense matrices, it has turned out that existing BLAS implementations tend to deliver poor performance in numerical kernels using tall and skinny dense matrices. This is the reason why selected tall and skinny matrix kernels have been implemented directly in GHOST. One may assume that a mature library like the Intel MKL yields optimal performance for a widely-used kernel like general dense matrix matrix multiplication (GEMM) for matrices of any shape. However, this is not the case as we demonstrate in Fig. 5. Similar observations concerning the performance drawback of MKL in the context of tall and skinny dense matrices have been made by Anderson et al. [2]. The GEMM kernel with (not too small) square matrices can reach a modern processor’s peak floating point performance if properly optimized. However, this does not hold for tall and skinny matrices where the arithmetic intensity is lower and possibilities for blocking are limited due to the small matrix dimensions. This results in a GEMM kernel which should ideally be memory-bound (as long as the dimension \( n \) is sufficiently large). In Fig. 5 it can be observed that the GHOST versions of both kernels are at least on par with the MKL performance for relatively small dimensions. The potential speedup can be up to \( 30 \times \) for some matrix sizes. Vectorized and fully unrolled versions of those kernels are automatically generated at compile time for predefined small
Fig. 5  Speedup of custom tall and skinny matrix kernels over Intel MKL on a single CPU socket. V is \( n \times m \), W is \( n \times k \) and X is \( m \times k \), where \( m, k \ll n \). a \( W \leftarrow VX \), b \( X \leftarrow V^T W \)

dimensions. See Sect. 5.4 for details on code generation and its impact on performance. If GHOST’s GEMM function is called, it first checks whether a suitable specialized function is applicable before calling the BLAS library.

In order to achieve a transparent support of block vectors in GHOST we implemented several BLAS level 1 routines and equipped them with block vector support. Obviously, as block vectors are also represented as dense matrices, those operations could be realized using existing BLAS level 3 routines. For example, the \texttt{vscal} kernel, which scales a block of vectors with a separate factor for each of them, could be replaced by a multiplication of the block vector with a diagonal matrix containing the scaling factors on its diagonal. However, this would come at additional cost by transferring zeros, which we want to avoid. Additionally, the concerns about the efficiency of BLAS level 3 operations for tall and skinny dense matrices apply here as well.

5.3 Kernel Fusion

Many sparse iterative solvers consist of a central SpM(M)V routine accompanied by several BLAS level 1/2 functions. It is thus useful to augment the SpM(M)V with more operations according to our needs. The general, shifted SpM(M)V operation \( y = \alpha (A - \gamma I)x + \beta y \) encompasses many of the practical use cases. In GHOST this operation can be chained with the computation of the dot products of \( \langle y, y \rangle \), \( \langle x, y \rangle \), and \( \langle x, x \rangle \) as well as the BLAS level 1 operation \( z = \delta z + \eta y \). This approach is similar to the well-known optimization technique of \textit{kernel fusion}. Similar thoughts led to the addition of the so-called BLAS 1.5/2.5 operators \texttt{AXPY\_DOT}, \texttt{GE\_SUM\_MV}, \texttt{GEMVT}, \texttt{TRMVT}, and \texttt{GEMVER} to the updated BLAS standard [7]. Siek et al. [46] observed the application specificity of these BLAS x.5 operators and made an attempt towards a domain-specific compiler to generate arbitrarily fused kernels consisting of different BLAS calls. This work has been continued by Nelson et al. [32], who plan to adapt their framework towards sparse matrices in future work. Recently, the idea of kernel fusion has gained new attention in the GPU programming community [43,50,53].

Note that each augmentation on top of the standard SpM(M)V can be enabled separately. Both, the use of block vectors and kernel fusion, have large potential regarding
performance, depending on the algorithm. For example, for the Kernel Polynomial Method, a method for computing the eigenvalue density of quantum systems as analyzed in [25], a 2.5-fold performance gain for the overall solver could be achieved by using block vectors and augmenting the SpMMV. Fused kernels are likely to be more cumbersome from an implementation point of view than fine-grained kernels. For instance, fusing the SpMMV operation with block vector dot products on a GPU leads to complex data access patterns which make an efficient implementation hard to achieve (see [25] for details). Due to the potentially high complexity of fused kernels and fundamental architectural differences, hand-optimized implementations for each target architecture can hardly be avoided if the focus is on high efficiency in heterogeneous settings.

A significant design decision for scientific computing libraries is whether and how to use task and data parallelism. A task-parallel approach for work distribution between heterogeneous devices, as implemented in MAGMA [28], may conflict with the presented optimization technique of kernel fusion and leave some optimization potential unused. In cases where the potential benefits of task parallelism are limited, such as the sparse matrix algorithms targeted by GHOST, data parallelism with kernel fusion may thus be favored over task parallelism.

5.4 Low-Level Implementation and Code Generation

GHOST is implemented with the goal of efficient execution from a single core to the petaflop level. Modern CPUs feature SIMD units which cause code vectorization to be a crucial ingredient for efficient core-level code. For kernels with sufficient simplicity, automatic vectorization is likely to be done by the compiler. If this is not the case, GHOST addresses this issue by using compiler pragmas, or SSE, AVX or MIC compiler intrinsics for explicit vectorization. Benchmarks on one CPU showing the impact of vectorization on SpMV performance can be seen in Fig. 6a. Here, we used the Sinclair/3Dspectralwave matrix \((n = 680,943, n_{nz} = 30,290,827)\) in complex double precision. A first observation is that all three variants reach the same maximum performance when using the full socket. Due to the the bandwidth-bound nature of the SpMV kernel this limit corresponds to the CPU’s maximum memory bandwidth. However, the faster saturation of the explicitly vectorized SELL kernel allows to use less cores to reach the same performance. The spare cores can be used for working on independent tasks (cf. Sect. 4.2) or they can be switched off in order to save energy. Hence, good vectorization should always be a goal, even for bandwidth-bound kernels. Note that this is especially true on accelerator hardware, where the width of vector units is typically comparatively large (cf. Table 1).

An obstacle towards efficient code often observed by application developers is lacking performance of existing program libraries due to their inherent and indispensable requirement of generality. Often, better performance could be achieved if performance-critical components were tailored to the application. Obviously, this goal is opposing the original goal of program libraries, namely general applicability. An important feature of GHOST for achieving high performance is code generation. At compile time, the user can specify common dimensions of data structures for which versions
of highly-optimized kernels will be compiled. A prominent example is the width of block vectors, i.e., the number of vectors in the block. This number typically is rather small, potentially leading to overhead due to short loops in numerical kernels. The positive impact of hard-coded loop lengths on the performance of SpMMV with increasing block vector width is demonstrated in Fig. 6b. The hardware and problem setting is the same as described above for Fig. 6a, i.e., the performance for one vector is the same as the saturated performance of Fig. 6a. If block vector widths 1, . . . , 8 are configured at compile time a significant performance benefit can be achieved compared to the case where none of them is configured. This is due to more optimization possibilities for the compiler thanks to simpler code and a lower impact of loop overheads.

Highly general fallback implementations exist for all compute kernels. This guarantees general applicability of GHOST functions. The degree of specialization gets diminished until a suitable implementation is found, which probably implies a performance loss.

6 Case Study: An Eigensolver with Trilinos and GHOST

In this section we want to briefly discuss how GHOST can be used with existing sparse solver libraries. A characteristic feature of typical iterative solvers for sparse linear systems or eigenvalue problems is that they require only the application of the matrix to a given vector. It is therefore good practice to separate the implementation of such methods from the data structure and details of the SpMV.

One approach that originated in the days of Fortran 77 is the ‘Reverse Communication Interface’ (RCI). The control flow passes back and forth between the solver routine and the calling program unit, which receives instructions about which operations are to be performed on which data in memory. While this programming model is still widely used in, e.g., ARPACK [27] and even in modern libraries such as Intel MKL [22], it is awkward and error-prone by today’s standards. Another idea is to use callback functions for selected operations. For example, the eigensolver package PRIMME [48] requires the user to provide the SpMMVM and a reduction operation on given data. Neither RCI nor simple callbacks can make optimal use of GHOST.
Obviously such software could only make use of accelerators by means of offload-
ing inside a function scope. If no special attention is paid to data placement, this is
typically inefficient due to the slow PCI express bus between CPU and device. Even
on the CPU, GHOST preferably would control memory allocation itself to achieve
alignment and NUMA-aware placement of data. Another drawback is the restriction
to data structures as prescribed by such solvers. For instance, the required storage
order of block vectors is typically column-major, which may be also inefficient (cf.
Sect. 5.2). The Trilinos package Anasazi [5] takes a different approach. It requires
the user to implement what we call a ‘kernel interface’, an extended set of callback
functions that are the only way the solver can work with matrices and vectors. New
(block) vectors are created by cloning an existing one via the kernel interface. Thus,
memory allocation stays on the user side and can be done, e.g., on a GPU, with a
custom data layout, or applying further optimizations.

In the iterative solver package PHIST [36] we use a similar kernel interface which
is written in plain C. It does not require a very general vector view concept and has
some functionality for executing (parts of) kernels asynchronously as GHOST tasks.
PHIST also provides GHOST adapters for Anasazi and the linear solver library Belos
from Trilinos, with the restriction that views of permuted columns of a block vector do
not work with row-major storage. This is not a grave restriction as the feature is—to
our knowledge—hardly used in the packages. For a performance study of the block
Jacobi-Davidson method implemented in PHIST (using GHOST), see [41].

We have demonstrated the applicability and performance of GHOST in a number
of publications. In [41], we have presented and implemented a block Jacobi-Davidson
method using PHIST & GHOST on up to 512 dual-socket CPU nodes. A fully hetero-
geneous GHOST implementation of the kernel polynomial method which we scaled
up to 1024 CPU+GPU nodes has been demonstrated in [25]. In the meantime, we
have continued our scaling studies of this application to 4096 heterogeneous nodes.
Recent work includes the implementation of Chebyshev filter diagonalization, for
which we show performance data on up to 512 dual-socket CPU nodes in [38]. While
all of the presented work has been conducted within activities closely related to the
GHOST project, we see that it is of special interest for a broader potential user base
how GHOST could integrate in existing CS&E software stacks.

In the following we want to demonstrate the applicability and performance of
GHOST using the Krylov-Schur method [49] for finding a few eigenvalues of large
sparse matrices. An implementation of this method is available in the Anasazi package
[5] of Trilinos. As mentioned in the previous section, PHIST can serve as an interface
layer between algorithmic packages like Anasazi and kernel libraries like GHOST or
Tpetra (+Kokkos). Developers can thus work at a high level of abstraction and have
the option to switch between kernel implementations. For this study, we are using
version 11.12.1 of Trilinos and an MPI+X approach with OpenMP parallelization on
the socket level. The test case is the non-symmetric MATPDE problem from the Matrix
Market [8]. It represents a five-point central finite difference discretization of a two-
dimensional variable-coefficient linear elliptic equation on an $n \times n$ grid with Dirichlet
boundary conditions. The ten eigenvalues with largest real part are sought using a
search space of twenty vectors. The convergence criterion is a residual tolerance of
Fig. 7  Scaling behavior of GHOST and Tpetra on up to 64 dual-socket CPU nodes for Anasazi’s implementation of the Krylov-Schur method. The annotations show the number of iterations until convergence. The computed parallel efficiencies consider changed iteration counts. a Strong scaling, $n = 2^{12}$. b Weak scaling, $n = 2^{12} \ldots 15$

10^{-6}. We set the random number seed in GHOST in a way which guarantees consistent iteration counts between successive runs.

GHOST integrates well with Anasazi and is straightforward to use on this level. Moreover we show in Fig. 7 that GHOST surpasses Tpetra both in terms of performance and scalability. On a single node one can save about 16% of runtime for the entire solver. Figure 7a reveals a higher parallel efficiency of GHOST. Consequently, the better node-level performance gets amplified on larger node counts, resulting in a 42% runtime saving on 64 nodes. For weak scaling, similar conclusions can be drawn from Fig. 7b. At the largest node count, the parallel efficiency of GHOST is ten percentage points above Tpetra. Relevant GHOST features used in the presented runs are resource management (thread pinning), SpMV with SELL-C-$\sigma$ and auto-generated kernels for tall & skinny dense matrix multiplications. Finding out the exact cause of the performance difference would require a deep analysis of the Tpetra implementation. This would go beyond the scope of this work and is therefore omitted. Note that even higher performance could possibly be obtained by exploiting advanced algorithmic optimizations available with GHOST, such as kernel fusion, block operations and communication hiding. However, those would potentially require a re-formulation of the algorithm which is not what we wanted to demonstrate here.

7 Conclusions and Outlook

GHOST is a novel and promising attempt towards highly scalable heterogeneous sparse linear algebra software. It should not be considered a comprehensive library but rather a toolbox featuring approaches to the solution of several problems which we have identified as relevant on modern hardware in the context of sparse solvers. A crucial component of highly efficient software, especially in the complex environment of heterogeneous systems, is sensible resource management. Our flexible, transparent, process-based and data-parallel approach for heterogeneous execution is accompanied by a lightweight and affinity-aware tasking mechanism, which reflects the requirements posed by modern algorithms and hardware architectures. During the ongoing development, we have observed that high performance is the result of a
mixture of ingredients. First, algorithmic choices and optimizations have to be made considering the relevant hardware bottlenecks. In the context of sparse solvers, where minimizing data movement is often the key to higher efficiency, this includes, e.g., vector blocking and kernel fusion. Second, while implementing those algorithms, it is crucial to have an idea of upper performance bounds. This can be accomplished by means of performance models, which form a substantial element of our development process. An optimal implementation may come at the cost of fundamental changes to data structures, e.g., storing dense matrices row- instead of column-major or changing the sparse matrix storage format from CRS to SELL-C-σ. During the ongoing development it has turned out that often the generality of the interface has to be traded in for high performance. There are several ways to relax this well-known dilemma, one of which is a close collaboration between library and application developers with the possibility for the latter to feed their application-specific knowledge into the library. In GHOST this idea is implemented by automatic code generation.

In its current state, GHOST has no provision for exploiting matrix symmetry. Obviously, there is large potential for increased of performance if symmetric (or Hermitian) matrices were treated as such. The implementation is challenging, but cannot be avoided in the long run. The optimization of heterogeneous MPI communication, e.g., using GPUdirect which bypasses the host memory in GPU-GPU communication, should be investigated in order to improve the communication performance. Future architectural developments, like deeper memory hierarchies and a tighter integration of “standard” and “accelerated” resources require rethinking existing performance models and possibly new implementations. On top of the currently implemented static load balancing for heterogeneous runs by means of micro-benchmarks, another important goal for future development is dynamic and automatic load balancing during an iterative solver’s runtime. Currently, the sparse matrix portion for each process is fixed during the entire runtime. By using the SELL-C-σ storage format, it will be straightforward to communicate matrix data at runtime between heterogeneous devices to overcome load imbalances.

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References
1. Alvermann, A., Basermann, A., Fehske, H., Galgon, M., Hager, G., Kreutzer, M., Krämer, L., Lang, B., Pieper, A., Röhrig-Zöllner, M., Shahzad, F., Thies, J., Wellein, G.: ESSEX: Equipping Sparse Solvers for Exascale, pp. 577–588. Springer International Publishing, Cham (2014). doi:10.1007/978-3-319-14313-2_49
2. Anderson, M., Ballard, G., Demmel, J., Keutzer, K.: Communication-avoiding QR decomposition for GPUs. In: IEEE International on Parallel Distributed Processing Symposium (IPDPS), 2011, pp. 48–58 (2011). doi:10.1109/IPDPS.2011.15
3. Augonnet, C., Thibault, S., Namyst, R., Wacrenier, P.A.: StarPU: a unified platform for task scheduling on heterogeneous multicore architectures. Concurr. Comput.: Pract. Exp. 23(2), 187–198 (2011). doi:10.1002/cpe.1631
4. Baker, C.G., Heroux, M.A.: Tpetra, and the use of generic programming in scientific computing. Sci. Program. 20(2), 115–128 (2012). doi:10.1159/2012/693861
5. Baker, C.G., Hetmaniuk, U.L., Lehoucq, R.B., Thornquist, H.K.: Anasazi software for the numerical solution of large-scale eigenvalue problems. ACM Trans. Math. Softw. 36(3), 13:1–13:23 (2009). doi:10.1145/1527286.1527287
6. Balay, S., Abhyankar, S., Adams, M.F., Brown, J., Brune, P., Buschelman, K., Dalcin, L., Eijkhout, V., Gropp, W.D., Kaushik, D., Knepley, M.G., McInnes, L.C., Rupp, K., Smith, B.F., Zampini, S., Zhang, H.: PETSc Web page (2016). http://www.mcs.anl.gov/petsc
7. Blackford, L.S., Demmel, J., Dongarra, J., Duff, I., Hammarling, S., Henry, G., Heroux, M., Kaufman, L., Lumsdaine, A., Petitet, A., Pozo, R., Remington, K., Whaley, R.C.: An updated set of basic linear algebra subprograms (BLAS). ACM Trans. Math. Softw. 28, 135–151 (2001). doi:10.1145/567806.567807
8. Boisvert, R.F., Pozo, R., Remington, K., Barrett, R.F., Dongarra, J.J.: Matrix market: A web resource for test matrix collections. In: Proceedings of the IFIP TC2/WG2.5 Working Conference on Quality of Numerical Software: Assessment and Enhancement, pp. 125–137. Chapman & Hall, Ltd., London, UK (1997)
9. Broquedis, F., Clet-Ortega, J., Moreaud, S., Furmento, N., Goglin, B., Mercier, G., Thibault, S., Namyst, R.: Hwloc: A generic framework for managing hardware affinities in HPC applications. In: Proceedings of the 2010 18th Euromicro Conference on Parallel, Distributed and Network-Based Processing, PDP ’10, pp. 180–186. IEEE Computer Society, Washington, DC, USA (2010). doi:10.1109/PDP.2010.67
10. Chevalier, C., Pellegrini, F.: PT-Scotch: a tool for efficient parallel graph ordering. Parallel Comput. 34(6–8), 318–331 (2008). doi:10.1016/j.parco.2007.12.001
11. Chow, E., Patel, A.: Fine-grained parallel incomplete factorization. SIAM J. Sci. Comput. 37(2), 169–193 (2015). doi:10.1137/140968896
12. Davis, T.A., Hu, Y.: The university of florida sparse matrix collection. ACM Trans. Math. Softw. 38(1), Art. No. 1 (2011). doi:10.1145/2049662.2049663
13. Demmel, J., Hoemmen, M., Mohiyuddin, M., Yelick, K.: Avoiding communication in sparse matrix computations. In: IEEE International Symposium on Parallel and Distributed Processing, 2008. IPDPS 2008, pp. 1–12 (2008). doi:10.1109/IPDPS.2008.4536305
14. Denis, A.: POSTER: a generic framework for asynchronous progression and multithreaded communications. In: IEEE International Conference on Cluster Computing (CLUSTER), 2014, pp. 276–277 (2014). doi:10.1109/CLUSTER.2014.6968752
15. Devine, K., Boman, E., Heaphy, R., Bisseling, R., Catalyurek, U.: Parallel hypergraph partitioning for scientific computing. In: Parallel and Distributed Processing Symposium, 2006. IPDPS 2006, 20th International, p. 10 (2006). doi:10.1109/IPDPS.2006.1639359
16. Galgon, M., Krämer, L., Thies, J., Basermann, A., Lang, B.: On the parallel iterative solution of linear systems arising in the FEAST algorithm for computing inner eigenvalues. Parallel Comput. 49, 153–163 (2015). doi:10.1016/j.parco.2015.06.005
17. Gebremedhin, A.H., Nguyen, D., Patwary, M.M.A., Pothen, A.: Colpack: software for graph coloring and related problems in scientific computing. ACM Trans. Math. Softw. 40(1), 1:1–1:31 (2013). doi:10.1145/2513109.2513110
18. GHOST: General, Hybrid, and Optimized Sparse Toolkit. https://bitbucket.org/essex/ghost. Accessed July 2016
19. Ghysels, P., Ashby, T.J., Meerbergen, K., Vanroose, W.: Hiding global communication latency in the GMRES algorithm on massively parallel machines. SIAM J. Sci. Comput. 35(1), C48–C71 (2013). doi:10.1137/12086563X
20. Gropp, W.D., Kaushik, D.K., Keyes, D.E., Smith, B.F.: Towards realistic performance bounds for implicit CFD codes. In: Proceedings of Parallel CFD99, pp. 233–240. Elsevier (1999)
21. Hager, G., Wellein, G.: Introduction to High Performance Computing for Scientists and Engineers, 1st edn. CRC Press Inc, Boca Raton, FL (2010)
22. Intel Math Kernel Library. https://software.intel.com/en-us/intel-mkl. Accessed July 2016
23. Kaczmarz, S.: Angenäherte auflösung von systemen linearer gleichungen. Bull. Int. Acad. Pol. Sci. Lett. 35, 355–357 (1937)
24. Kreutzer, M., Hager, G., Wellein, G., Fehske, H., Bishop, A.R.: A unified sparse matrix data format for efficient general sparse matrix-vector multiplication on modern processors with wide SIMD units. SIAM J. Sci. Comput. 36(5), C401–C423 (2014). doi:10.1137/130930352
25. Kreutzer, M., Pieper, A., Hager, G., Wellein, G., Alvermann, A., Fehske, H.: Performance engineering of the kernel polynomial method on large-scale cpu-gpu systems. In: Parallel and Distributed Processing Symposium (IPDPS), 2015 IEEE International, pp. 417–426 (2015). doi: 10.1109/IPDPS.2015.76
26. LAMA: Library for accelerated mathematical applications. http://www.libama.org. Accessed July 2016
27. Lehoucq, R., Sorensen, D., Yang, C.: ARPACK users’ guide. Soc. Ind. Appl. Math. (1998). doi: 10.1137/1.9780898719628
28. MAGMA: Matrix algebra on GPU and multicore architectures. http://icl.cs.utk.edu/magma/. Accessed July 2016
29. Matrix Market Exchange Format. http://math.nist.gov/MatrixMarket/formats.html#MMformat. Accessed July 2016
30. McCalpin, J.D.: Memory bandwidth and machine balance in current high performance computers. IEEE Computer Society Technical Committee on Computer Architecture (TCCA) Newsletter pp. 19–25 (1995)
31. Monakov, A., Lokhmotov, A., Avetisyan, A.: Automatically tuning sparse matrix-vector multiplication for GPU architectures. In: Y. Patt, P. Foglia, E. Duesterwald, P. Faraboschi, X. Martorell (eds.) High Performance Embedded Architectures and Compilers, Lecture Notes in Computer Science, vol. 5952, pp. 111–125. Springer, Berlin (2010). doi: 10.1007/978-3-642-11515-8_10
32. Nelson, T., Beller, G., Siek, J.G., Jessup, E., Norris, B.: Reliable generation of high-performance matrix algebra. ACM Trans. Math. Softw. 41(3), 18:1–18:27 (2015). doi: 10.1145/2629698
33. O’Leary, D.P.: The block conjugate gradient algorithm and related methods. Linear Algebra Appl. 29, 293–322 (1980). doi: 10.1016/0024-3795(80)90247-5. (Special Volume Dedicated to Alson S. Householder)
34. Oppe, T.C., Kincaid, D.R.: The performance of ITPACK on vector computers for solving large sparse linear systems arising in sample oil reservoir simulation problems. Commun. Appl. Numer. Methods 3(1), 23–29 (1987). doi: 10.1002/cnm.1630030106
35. PARALUTION. http://www.paralution.com. Accessed July 2016
36. PHIST: Pipelined Hybrid-parallel Iterative Solver Toolkit. https://bitbucket.org/essex/phist. Accessed July 2016
37. Pieper, A., Heinisch, R.L., Wellein, G., Fehske, H.: Dot-bound and dispersive states in graphene quantum dot superlattices. Phys. Rev. B 89, 165121 (2014). doi: 10.1103/PhysRevB.89.165121
38. Pieper, A., Kreutzer, M., Alvermann, A., Galgon, M., Fehske, H., Hager, G., Lang, B., Wellein, G.: High-performance implementation of Chebyshev filter diagonalization for interior eigenvalue computations. J. Comput. Phys. 325, 226–243 (2016). doi: 10.1016/j.jcp.2016.08.027
39. Polizzi, E.: Density-matrix-based algorithm for solving eigenvalue problems. Phys. Rev. B 79, 115112 (2009). doi: 10.1103/PhysRevB.79.115112
40. Rabenseifner, R., Hager, G., Jost, G.: Hybrid mpi/openmp parallel programming on clusters of multicore smp nodes. In: 17th Euromicro International Conference Parallel, Distributed and Network-based Processing, 2009, pp. 427–436 (2009). doi: 10.1109/PDP.2009.43
41. Röhrig-Zöllner, M., Thies, J., Kreutzer, M., Alvermann, A., Pieper, A., Basermann, A., Hager, G., Wellein, G., Fehske, H.: Increasing the performance of the Jacobi–Davidson method by blocking. SIAM J. Sci. Comput. 37(6), C697–C722 (2015). doi: 10.1137/140976017
42. Rupp, K., Rudolf, F., Weinbub, J.: ViennaCL—A High Level Linear Algebra Library for GPUs and Multi-Core CPUs. In: International Workshop on GPUs and Scientific Applications, pp. 51–56 (2010)
43. Rupp, K., Weinbub, J., Jüngel, A., Grassner, T.: Pipelined iterative solvers with kernel fusion for graphics processing units. ACM Trans. Math. Softw. 43(2), 11:1–11:27 (2016). doi: 10.1145/2907944
44. Schofield, G., Chelikowsky, J.R., Saad, Y.: A spectrum slicing method for the Kohn–Sham problem. Comput. Phys. Commun. 183(3), 497–505 (2012). doi: 10.1016/j.cpc.2011.11.005
45. Schubert, G., Fehske, H., Fritz, L., Vojta, M.: Fate of topological-insulator surface states under strong disorder. Phys. Rev. B 85, 201105 (2012). doi: 10.1103/PhysRevB.85.201105
46. Siek, J., Karlin, I., Jessup, E.: Build to order linear algebra kernels. In: IEEE International Symposium on Parallel and Distributed Processing, 2008. IPDPS 2008, pp. 1–8 (2008). doi: 10.1109/IPDPS.2008.4536183
47. SpMP: Sparse matrix pre-processing library. https://github.com/IntelLabs/SpMP. Accessed July 2016
48. Stathopoulos, A., McCombs, J.R.: PRIMME: preconditioned iterative multimethod eigensolver-methods and software description. ACM Trans. Math. Softw. 37(2), 1–30 (2010). doi: 10.1145/1731022. 1731031
49. Stewart, G.W.: A Krylov-Schur algorithm for large eigenproblems. SIAM J. Matrix Anal. Appl. 23(3), 601–614 (2002). doi:10.1137/S0895479800371529

50. Tabik, S., Ortega, G., Garzn, E.: Performance evaluation of kernel fusion BLAS routines on the GPU: iterative solvers as case study. J. Supercomput. 70(2), 577–587 (2014). doi:10.1007/s11227-014-1102-4

51. TOP500 Supercomputer Sites as of June 2016. http://www.top500.org. Accessed July 2016

52. Vital, B.: Etude de quelques méthodes de résolution de problèmes linéaires de grande taille sur multiprocesseur. Ph.D. thesis, Université de Rennes, Rennes (1990)

53. Wahib, M., Maruyama, N.: Scalable kernel fusion for memory-bound GPU applications. In: Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis, SC ’14, pp. 191–202. IEEE Press, Piscataway, NJ, USA (2014). doi:10.1109/SC.2014.21

54. Williams, S., Waterman, A., Patterson, D.: Roofline: an insightful visual performance model for multicore architectures. Commun. ACM 52(4), 65–76 (2009). doi:10.1145/1498765.1498785

55. Wittmann, M., Hager, G., Zeiser, T., Wellein, G.: Asynchronous MPI for the masses (2013). http://arxiv.org/abs/1302.4280. Preprint