Boda-RTC: Productive Generation of Portable, Efficient Code for Convolutional Neural Networks on Mobile Computing Platforms

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Abstract—The popularity of neural networks (NNs) spans academia [1], industry [2], and popular culture [3]. In particular, convolutional neural networks (CNNs) have been applied to many image based machine learning tasks and have yielded strong results [4]. The availability of hardware/software systems for efficient training and deployment of large and/or deep CNN models is critical for the continued success of the field [5] [1]. Early systems for NN computation focused on leveraging existing dense linear algebra techniques and libraries [6] [7]. Current approaches use low-level machine specific programming [8] and/or closed-source, purpose-built vendor libraries [9]. In this work, we present an open source system that, compared to existing approaches, achieves competitive computational speed while achieving significantly greater portability. We achieve this by targeting the vendor-neutral OpenCL platform [10] using a code-generation approach. We argue that our approach allows for both: (1) the rapid development of new computational kernels for existing hardware targets, and (2) the rapid tuning of existing computational kernels for new hardware targets. Results are presented for a case study of targeting the Qualcomm Snapdragon 820 mobile computing platform [11] for CNN deployment.

Index Terms—computer vision; code generation; neural networks; mobile computing; convolution

I. INTRODUCTION AND MOTIVATION

Convolutional neural network (CNN) based approaches have become dominant in a broad variety of computer vision applications, including object detection [12], video classification [13], and human action recognition [14]. On a mobile phone or wearable device, energy-efficient computer vision is necessary to put these and other applications into production in order to enable novel functionality and achieve the promises of augmented reality. More critically, the safety of autonomous vehicles hinges on their ability to understand their surroundings in real-time under tight energy, power, and price constraints. To support ongoing research, development, and deployment of systems that include NNs, it is desirable to nurture a diverse enabling ecosystem of tools and approaches. In particular, we feel it is desirable to support many hardware and software platforms to enable new applications across many areas, including mobile, IoT, transportation, medical, and others. Imagine that, for a given task, high-performance vendor libraries exist for at least one platform. Currently, for CNNs, the vendor is Nvidia, the platform is Maxwell, and the library is cuDNN [9]. Why not simply use that vendor’s platform and libraries for the task and be satisfied? One issue is quite simple: in industrial use cases, choice of platform may be dictated by business concerns. Further, those same business concerns may preclude dependence on any single vendor. For example, the flagship Samsung Galaxy S7 mobile phone ships in two versions: one using a Samsung-proprietary Exynos 8890 System-on-Chip (SoC), the other using the Qualcomm Snapdragon 820 [11] SoC. Neither of these SoCs contains Nvidia GPUs or are otherwise capable of running cuDNN. Further, Nvidia, Qualcomm, and Samsung have engaged in a long running patent dispute over GPU technologies. Based on the uncertainties associated with such litigation, SoC and/or GPU alternatives are subject to constant change. Further, even once a hardware platform is chosen, business needs may dictate the specific software tasks that must be supported. For example, in an effort to provide differentiation, vendors have a strong desire to implement novel functionality not present in existing publicly available libraries. Together, these uncertainties about both target hardware and particular use-case create a strong pressure for portability: the ability to quickly achieve reasonably performance for a variety of tasks across a variety of platforms.

This work focuses on the challenges associated with achieving portable, efficient computation of the key primitive operations needed by convolutional neural networks. We frame the problem as follows:

Consider a use-case consisting of a specific combination of:

- a target computational device (i.e. a hardware architecture), and
- a set of convolutional neural network primitives and an input size (i.e. a CNN architecture and task).

For such a use-case, achieving good computational efficiency
and/or meeting particular performance requirements is, in general, difficult. Building systems based on existing computational libraries (e.g. BLAS) generally achieves only limited efficiencies \[15\]. Improving on such approaches requires tuning multiple computational kernels for the particular use-case at hand. This generally requires months of effort by a very specialized programmer. This programmer must be one that is both capable of producing high-efficiency code for a target platform as well as being familiar with the details of CNN computations. Such programmers are not common and thus their time is a very limited resource.

In this work, we present an open-source vertically-integrated framework for developing and deploying CNN computations. The framework combines parts of the functionality of CNN middleware frameworks such as Caffe \[7\] or TensorFlow \[10\] with the functionality of CNN computation libraries such as Nvidia’s cuDNN \[9\] or Nervana System’s NervanaGPU/neon \[17\] \[18\]. “Out-of-the-box,” our framework does not attempt to have the breadth or depth of features of a typical general-use middleware such as Caffe or TensorFlow. Also, it does not attempt to achieve the same efficiency as a highly-target-specific computational library such as cuDNN. Instead, we aim to allow for the rapid development and deployment of new use-cases/flows of the form described above. In particular, the framework enables productive, flexible, modular code generation of the full set of needed CNN operations for any given use case.

This allows for both:

- the rapid development of new computational kernels for existing hardware targets, and
- the rapid tuning of existing computational kernels for new hardware targets.

To provide support for these claims, we present a case study of using the framework to target the Qualcomm Snapdragon 820 mobile computing platform \[11\] for CNN deployment (see Figure \[1\]). We show that the framework enabled a quick path to initial functional correctness, and from there helped navigate a smooth path to reasonably efficient computational performance.

The rest of the paper is organized as follows. In Section \[II\] we review the semantics of the key computational operations needed to support CNNs, focusing particularly on convolution. Then, in Section \[III\] we discuss performing CNN calculations on modern computational hardware, focusing particularly on the issue of data reuse. We take a historical approach to this explanation, citing related work along the way. In Section \[IV\] we consider the general topic of programming GPUs and performance portability. In Section \[V\] we introduce our framework using the example kernel of single-precision matrix-matrix multiply (SGEMM). The use of such a relatively simple, existing computational kernel allows us to:

- illustrate in general what our framework does and how to apply it,
- to show in particular how we approach a new hardware target, and
- to provide a good baseline for general performance evaluation.

Then, we present our core contribution of productive, portable, efficient, code generation for CNN operations (via case study) in Sections \[VI\] and \[VII\]. Finally, we conclude in Section \[VIII\].

II. INTRODUCTION TO CNN COMPUTATIONS

Different CNN architectures can contain a wide variety of computational primitives. For completeness, it is important that any CNN computation system supports a reasonably broad set of such primitives. Further, it is desirable that support for new operations, particularly those that are simple, can be easily added. The most common operations needed for deployment (also known as testing or inference, and as opposed to training) include convolution, pooling and softmax. However, across many common networks, such as AlexNet \[6\], GoogLeNetV1 \[19\], and the VGG networks \[20\], convolution operations dominate the overall computation. Thus, in this section, we focus on the convolution operation. In particular, we consider the commonly occurring forms of convolutions from the above (and similar) CNNs. Given the nature of this work, we will focus on practical, operational definitions of the relevant computations and the data on which those computations act. Although various types of data are used in CNNs, the most common are 32-bit (and, increasingly, 16-bit) floating point numbers. Regardless of exact type or precision, the numeric values used by CNNs are grouped into named ND-Arrays (i.e. collections of numbers with N indexes, sometimes also called N-D Matrices or tensors). Thus, we define convolution operationally as the function \( out = \text{conv}(in, \text{filts}) \) where \( out, in, \) and \( \text{filts} \) are all N-D arrays. For simplicity, we omit discussion of the common practice of special-case handling of biases here. Further, we will restrict the discussion to convolution over 2D images, which is the only type used in the above example networks. Thus, for a single 2D multi-channel image, both \( in \) and \( out \) are 3D arrays, with their dimensions being the image height, the image width, and the number of image channels. For example, the overall input to a network might be an RGB (3 channel) image with a size of \( 205 \times 205 \) pixels. Thus the dimensions of the 3D array storing this image (\( \text{dims}(in) \)) could be written compactly as \( Y \times X \times C = 205 \times 205 \times 3 \), where the \( H, W, \) and \( C \) name the dimensions, and the 200, 200, and 3 are the concrete sizes of those dimensions. Often, particularly for training, it is desirable to process a \textit{batch} of multiple images. In this case, an additional \( B \) dimension is added to \( in \) and \( out \). For the example of a 32 image batch, \( \text{dims}(in) \) becomes \( B \times Y \times X \times C = 32 \times 205 \times 205 \times 3 \). The results of the convolution are fully independent across input/output image pairs. Thus, for simplicity, we assume a single image for the remainder of this discussion. The semantics of convolutions are determined by several architecturally specified values: the number of output channels, the kernel size, and the stride. While in general the kernel size and stride can be different in each spatial dimension (i.e. \( X \) and \( Y \) in the 2D case), for simplicity, here we consider only the case where kernel size...
and stride are the same for all dimensions (i.e. are scalars). The kernel size and number of output channels, combined with the number of channels in \( in \), determine \( \text{dims}(\text{filts}) \). In our running example, recall that the number of input channels \( IC = 3 \). If the number of output channels \( OC = 96 \), and the kernel size \( KSZ = 7 \), then \( \text{dims}(\text{filts}) \) will be \( OC \times KSZ \times KSZ \times IC = 96\times7\times7\times3 \). Finally, the width of the output will be given by \( out_X = 1 + (in_X - KSZ) / \text{stride} \) (and similarly for the height). Thus, if the stride for this example is 2, then we have \( out_X = 1 + (205 - 7) / 2 = 100 \), and \( \text{dims}(\text{out}) \) will be \( Y \times X \times C = 100 \times 100 \times 96 \). Note that \( in \) is often padded by \( \lfloor KSZ / 2 \rfloor \) elements (usually zeros) in each spatial dimension. When such padding is applied (assuming \( stride = 1 \)), \( out \) will have the same spatial dimensions (height and width) as \( in \). We can calculate each output channel \( oc \) using \( in \) and the 3D slice of \( \text{filts} \) where \( OC = oc \). That is, we use each slice \( \text{filts}[OC = oc] \) (\( \text{dims} KSZ \times KSZ \times IC = 7 \times 7 \times 3 \)) to compute each slice \( out[OC = oc] \) (\( \text{dims} Y \times X = 100 \times 100 \)). Then, for each output point \( out[OC = oc, Y = oy, X = ox] \), we extract a \( KSZ \times KSZ \) window of \( in \) (sometimes called an input patch or patch) starting at \( Y = oy \times \text{stride}, X = ox \times \text{stride}, \) across all input channels, to yield the slice \( in[Y = oy \times \text{stride}, oy \times \text{stride} + KSZ], X = [ox \times \text{stride}, ox \times \text{stride} + KSZ] \) (\( \text{dims} Y \times X \times C = 7 \times 7 \times 3 \)). The final value of each output point is the sum of all elements of the element-wise product of the per-output-channel slice of \( \text{filts} \) and the per-output-x-y-point slice of \( in \). Typically some activation function, such as ReLU (\( \text{max}(0, x) \)) \( \text{[21]} \), is next applied to each output value, and this operation is often fused into the convolution operation itself for efficiency. For later reference, note here that each \( in \) slice is reused across all output channels, and each \( \text{filts} \) slice is reused across all output x-y points. Similarly, note that if multiple images are processed in a batch, the number of input-patches/output-x-y-points is multiplied by \( B \).

III. CNN COMPUTATIONS ON MODERN HARDWARE AND RELATED WORK

In the prior section, the final computation of each (scalar) output value in a convolution consisted of an element-wise product of two ND-Arrays (one a slice of the input, one a slice of the filters, with exactly equal dimensions), followed by a sum over all the elements of the product. If we were to conceptually reshape or view the two 3D slices as 1D arrays (i.e. vectors, with size equal to the product of the 3 3D-Array dimension sizes), we can see that this operation is simply a vector dot-product. Thus, the core computational operation of a large class of NNs (including CNNs) is to perform many dot-product operations between a large set of input vectors and model parameter vectors (also known as filter weights, filters, or weights). In NNs with multiple layers, the outputs of one operation may become inputs to another. In CNNs, the slices that form the inputs to each dot-product may spatially overlap and thus share data with each other. Recall that in our running example, the we have \( \text{dims}(\text{out}) \) of \( Y \times X \times C = 100 \times 100 \times 96 \), yielding \( 100 \times 100 \times 96 = 960000 \) output points, each requiring one dot-product to compute. If we consider the set of all input-slice/filter-slice pairs to these 960000 dot-products, we see that it is formed from the cross product of \( 100 \times 100 = 10000 \) input slices and 96 (per-output channel) filter slices. Thus, each dot-product input is reused across many dot-products: 96 dot-products for each input-slice, and 10000 dot-products for each filter-slice.

At least as early as 2004, work using GPUs to accelerate NNs made the key observation that this data reuse pattern of NNs makes then well suited for calculation using GPUs \( \text{[5]} \). Based on the amount of calculation hardware available, and the rate at which it can perform calculations, each computational system has a peak computational rate. Computations which can achieve this peak rate on a given system are termed compute limited. But, on modern computational systems (CPUs and GPUs), computations such as batches of independent dot-product operations are instead limited by the time taken to transfer operands between different storage locations in the system. This is termed a bandwidth limited computation. Depending on the ratio of communication resources to compute resources in a system, it is necessary to reuse data to varying degrees at different levels of the storage hierarchy of the system to avoid becoming bandwidth limited \( \text{[22]} \). Over time, the relative cost of communication has increased compared to that of computation, so systems that have high absolute peak computational rates (for a given power level) require increasing amounts of data reuse to achieve those rates \( \text{[23]} \). The terms Arithmetic Intensity (or sometimes more generally Operational Intensity), abbreviated AI in this work, is used to refer ratios between an amount of computation and an amount of communication. The most common units for AI are FLOPS/byte \( (F/B) \), and care must be taken to properly convert any quantities of communication from elements (e.g. 32-bit or 16-bit floats) into bytes (e.g. 4 bytes per 32-bit float, 2 bytes per 16-bit float). For a given flow, there are two key top-level AI values of interest: the AI required by the hardware to achieve peak compute rate (the knee AI), and the best-case AI available in the computation to be performed. To find the top-level knee AI for a given hardware device, we simply divide the peak compute rate of the device by the peak off-chip bandwidth of the device. However, note that since most hardware systems have multiple levels of memory hierarchy and have many quirks that complicate issues, this top-level knee AI provides only (perhaps unachievable) upper bounds on performance with respect to any given computation’s AI. To calculate the best-case available AI for a given computation, we take the number of FLOPS to be performed divided by the (minimal) total number of bytes to transfer.

Returning to our working example, recall that the size of each input-slice is \( 7 \times 7 \times 3 \), or 147 elements. If we form a 2D matrix using all 10000 input slices as rows, we will have a \( 10000 \times 147 \) matrix \( \text{inmat} \). Similarly, we can form 2D matrix using all 96 filter slices as columns, yielding a \( 147 \times 96 \) matrix \( \text{filtsmat} \). We can now express the entire convolution operation as a single matrix-matrix multiply operation: \( \text{outmat} = \text{inmat} \cdot \text{filtsmat} \). Note that \( \text{outmat} \) has \( 10000 \times 96 = 960000 \) elements, so we can reshape it to the desired \( \text{dims}(\text{out}) \) of \( Y \times X \times C = \)}
100×100×96. Due to the dot-product-input reuse discussed earlier, such matrix-matrix multiplies are generally amenable to high-efficiency GPU implementations [24]. Quantitatively, this is seen by the fact that such computations have high AI.

In Figure 2 we show the calculation of the AI for the matrix-multiplication of our running example. Early CNN frameworks such as cuda-convnet [6] and Caffe [7] originally performed CNN convolutions in exactly this fashion, leveraging Nvidia’s cuBLAS [25] matrix library. However, there are several limitations of this BLAS-based approach:

- When $in_X, in_Y >> KSZ$, $inmat$ is roughly $(KSZ/\text{stride})^2$ larger than $in$; thus explicitly creating the matrix $inmat$ may require significant intermediate memory, and to a lesser extent, non-negligible time.
- It does not allow for data reuse between spatially overlapping input slices.
- The underlying matrix-matrix multiply library may not be well optimized for the problem sizes required.
- It is not possible to fuse an activation function with the convolution operation.
- It is not possible to use various other optimizations, such as Winograd convolution [26].

Regardless of the exact reasons, it became clear to the community of researchers working on high-performance implementations of CNNs that BLAS-based approaches were often falling far short of peak compute. Overall community efforts then turned to purpose-built libraries for convolution, so it remains an open research question what the limits of BLAS-based approaches are in various cases.

In particular, Nvidia soon released the cuDNN [9] library, which exposes an API for directly performing convolutions using a variety of approaches. Due to the closed-source nature of the library, and the fact that it has evolved rapidly, it is difficult to analyze in detail. However, from community benchmarking it is clear that it achieves much higher efficiency than BLAS-based approaches [15]. Concurrently, a family of libraries based on an assembly-language-level programming flow appeared [81] [17] [18], offering similar performance to cuDNN. Historically, the assembly language level approach has offered the best performance at any given time, with cuDNN catching up in its next release. Since the above mentioned assembly-language kernels are open source, one could speculate that Nvidia is copying or reimplementing them internally. If true, it would imply that the entire high-performance CNN computation ecosystem is anchored by only a few high-performance programmers at Nervana Systems and Nvidia. One result of this state of affairs is that there is effectively only one usable hardware platform for high efficiency CNN computations: Nvidia Maxwell GPUs. For completeness, we briefly consider the state of the art for performing convolution on CPUs. Recently, Intel has made significant advances in supporting convolutions, and is competitive with GPUs at large scale [27]. However, in practice, most use cases are still single socket, or at most single node, and current CPUs cannot offer competitive performance at this scale, particularly using consumer (as opposed to server) parts. Also, it is unclear that CPUs are currently competitive with GPUs on a power or cost basis for CNN computation. Note that a detailed comparison of CPUs vs. GPUs is outside the scope of this paper. While in this work we focus on targeting GPUs, extending our results to CPUs is a reasonable topic for future work.

IV. Programming GPUs and Performance Portability

GPUs are generally considered more difficult to program than CPUs. This is not an issue for an end-user of a library like cuDNN, since all interactions with the GPU are hidden behind a C library interface. However, if one wishes to write such a library, one must face the complexity and issues of GPU programming and portability. For Nvidia hardware, the proprietary CUDA language is the officially blessed programming language. Alternately, the OpenCL [10] standard is the only portable option for targeting a variety of GPUs (including Nvidia GPUs). In terms of low-level features, memory model, and threading model, CUDA and OpenCL are quite similar. For example, many GPUs allow explicit loads and stores to the L2 cache memory as an alternative or adjunct to traditional caching and prefetching. OpenCL and CUDA both expose this; OpenCL calls it local memory whereas CUDA calls it shared memory. For the program itself, both languages are based on defining a single function (termed a kernel in both languages) that is run by many threads in parallel. Kernels are compiled to sequences of machine code and cached in instruction caches on GPUs similarly to on CPUs. In practice, when running the same program on different GPUs, OpenCL provides only functional portability. That is, a given (correct) OpenCL program will produce consistent results on all supported OpenCL platforms. However, an OpenCL program that is tuned for high efficiency on one platform (e.g. an Nvidia Maxwell GPU) will not necessarily deliver high efficiency when run on a different platform (e.g. a Qualcomm Snapdragon SoC’s GPU). Perhaps due to this issue, no OpenCL library comparable to cuDNN or NervanaGPU exists. Thus, OpenCL support for CNN operations on AMD or any other GPU platforms is generally lacking. Currently, in the caffe framework, support for OpenCL uses only the BLAS-based approach, and even that support is marginalized and fragmented across various forks and pull requests. In this paper, we aim to bridge the performance-portability gap for CNN operations, and bring such operations to a more even footing across various hardware platforms when compared with existing high efficiency approaches.

For the two platforms we consider in this work, Figure 3 shows the basic roofline curves formed by considering peak compute rate and off-chip memory bandwidth. The knee Arithmetic Intensity (AI) for each platform is marked; note that although the two platforms have very different absolute performance, their knee AIs are similar. Peak values are taken from documentation in the case of the Nvidia hardware, but (due to lack of documentation) are approximated using a microbenchmark (clpeak [29]) for the Qualcomm hardware.
inmat batches of images, the size of inmat is typically simply a reshape of the matrix-of-input-slices naming convention, an auxiliary function implements the core computation. Also, following the Caffe metaprogramming, and all offer similar key benefits: C++ templates, and ad-hoc code generation are all examples of metaprogramming, and all offer similar key benefits: 

- In general, values that are known ahead of time can be constant in the final code without (potentially repeatedly) hard-coding them at the source level.
- Loops with static bounds are easier to unroll and/or require less instructions or registers to implement.
- Offsets, strides, scales, and other values can often be statically combined and/or used as immediates to reduce register usage and instruction count.
- Conditionals depending on known-constant values can be

exceed GPU memory. To avoid this, batches may be handled with separate per-image calls to im2col() and SGEMM(). SGEMM is a simple and well studied function across many hardware architectures. The main required tasks for achieving an efficient SGEMM implementation for a given hardware target are as follows:

1) Arranging accesses to storage to make best use of system’s communication potential.
2) Achieving sufficient data reuse at each level of the system’s storage hierarchy to avoid being bandwidth limited.
3) Ensuring computational units are continually active; (2) is necessary but not sufficient for this.
4) Repeating (1), (2), and (3) for all interesting input sizes.

Unfortunately, these goals are often both interrelated and in conflict with each other. For example, it is often the case that accessing storage contiguously, or in certain patterns, achieves higher bandwidth than others. Thus, there may be a tradeoff between achieving good communication bandwidth and reading the best set of data for reuse at the next level. In general, (1) and (2) directly balance each other. So, if a factor of N additional reuse can be achieved at anything less than a factor of N cost in bandwidth, it is favorable to do so. The primary goal is (3); if the maximum compute rate can be achieved, other concerns are secondary. The input sizes for SGEMM are expressed as $M, K,$ and $N$, all scalars, where if $c = SGEMM(a, b)$, then $c$ is an $M \times N$ matrix, $a$ is $M \times K$, and $b$ is $K \times N$. The general-case AI calculation for SGEMM is $AI = \frac{\text{FLOPS}}{\text{BW}}$. Typically, it is difficult to achieve good efficiency across a range of sizes and hardware targets without some form of metaprogramming. We define metaprogramming as the collection of techniques where, instead of directly writing code, some higher level facility is used to create the desired final code. C Macros, C++ templates, and ad-hoc code generation are all examples of metaprogramming, and all offer similar key benefits:

- In general, values that are known ahead of time can be constant in the final code without (potentially repeatedly) hard-coding them at the source level.
- Loops with static bounds are easier to unroll and/or require less instructions or registers to implement.
- Offsets, strides, scales, and other values can often be statically combined and/or used as immediates to reduce register usage and instruction count.
- Conditionals depending on known-constant values can be
eliminated.
- Many variants of a single version of an algorithm can be generated simply by varying parameters at the meta level.
- Repetitive sections of code can be generated, rather than manually written. This is particularly important when simpler techniques such as compiler-driven loop unrolling are insufficient or cumbersome.

The usage of metaprogramming for SGEMM for GPUs seems to be commonplace; as far as the authors are aware, it is used to varying degrees by all modern, efficient GPU BLAS libraries including cuBLAS [25], MAGMA [30], and clBLAS [31].

Our framework uses a combination of string-replacement templates, specific support for known-size ND-Array access, and ad-hoc unrestricted programmatic code generation. This places it toward the more flexible/extreme end of the space of metaprogramming techniques. Although metaprogramming is inherently complex, we nonetheless attempt to achieve a good balance between flexibility, power, simplicity, and ease of use. To implement SGEMM in OpenCL for GPU targets, we employ the following standard techniques:
- Register Tiling [32]
- Explicit Local Memory Blocking
- Inner Loop Unrolling

Listing 1 shows pseudocode for our SGEMM template.

Listing 1. SGEMM code template

```c
void SGEMM( nda M:K a, nda N:K bt, nda M:N c ) {
    // dims work Mg:Ng:Mb:Nb:Kb:Mt:Nt // blocking values
    local a_lm (%(work_Kb_dim)) (%(work_Nb_dim)) (%(work_Mt_dim))
    // per-thread tile of output to compute, stored in registers
    float c_t (%(work_Mt_dim)) (%(work_Nt_dim)) = 0;
    float a_r (%(work_Mt_dim));
    float b_r (%(work_Mt_dim));
    for( int32_t k = 0; k < %(a_K_dim); k += %(work_Kb_dim) ) {
        BARRIER_SYNC;
        // workgroup-wide load of local memory for this iteration
        %lm_loads;
        BARRIER_SYNC;
        for( int32_t k = 0; k < %(a_K_dim); k += %(work_Kb_dim) ) {
            BARRIER_SYNC;
            for( uint32_t m = 0; m < %(work_Mt_dim); ++m ) {
                BARRIER_SYNC;
                %transposes_c_t_row; // transpose row of c_t into b_r
                a_r += b_r[%(store_c_t_row)]; // store transposed row of c_t to c
            }
        }
    }
}
```

For a given input size and hardware platform, the first main task of the code generation is to determine a good blocking strategy. This can be accomplished with a combination of heuristic calculations, manual parameter tuning, or automated tuning. In this work, we use only the first two approaches; use of automated tuning is a good subject for future work. The general flow from operation (SGEMM or convolution) to blocking constants is illustrated in Figure 5. The main blocking parameters we must choose are:
- $Mt, Nt$: The number of output elements computed per thread in the M and N dimensions. Typically in the range $[1, 8]$. Note that the kernel will require at least $Mt \times Nt$ registers per thread.
- $Kb$: The inner loop unrolling factor. Typically in the range $[1, 8]$. If too small, loop overhead becomes excessive. If too large, Instruction or Local memory will be insufficient, as both scale linearly with $Kb$.
- $Mb, Nb$: Determines the total number of output elements computed per workgroup. Valid and/or desirable values vary by hardware architecture, but often $Mb \times Nb \equiv \text{threads per workgroup}$ should be in the range $[32, 256]$. When $Mb \approx Nb$, both Local memory usage and the Global/Local memory reuse factor scale linearly as $Mb$ (or $Nb$).
- $Mg, Ng$: Based on $M, N$ and the prior choices of $Mt, Nt, Mb, Nb$, we have $Mg = \lfloor M/Mb/Mt \rfloor$ and $Ng = \lfloor N/Nb/Nt \rfloor$. $Mg \times Ng$ workgroups will be needed to compute the final result. For many targets, the total number of workgroups must be above a threshold to saturate all computational elements in the device. Small values may be subject to performance limitations if they are not a multiple of some particular constant.

After determining the blocking constants, the code generator must emit code for various blocks:
- %lm_loads: workgroup-wide cooperative global memory load
- %loads: $Mt \times Nt$ per-thread local memory load
- %fmas: $Mt \times Nt$ in-register multiply-adds
- %store_c_t_row: transpose and write per-thread outputs into $c$

The general challenges when emitting these blocks are to minimize conditionals and choose particular constructs that can execute efficiently. Careful data layout at the global, local, and register levels may be required, potentially with additional code to reorganize, shuffle, or transpose data at each level. With a few days of effort, reasonable SGEMM performance on an Nvidia Titan-X GPU was achieved. See Table IV for a comparison of this template’s performance with that of the SGEMM from Nvidia’s highly-tuned cuBLAS library. In short, with moderate effort our framework achieved $\approx 80\%$ of the performance of the vendor library, albeit only for a few simple cases.

Next, we turn our attention to our main focus: our new hardware target, the Snapdragon 820 (SD820). The first key thing we learned about this platform is that manual vectorization
of load and stores yields an improvement of 2x or more in load/store bandwidth. Further, at least for SGEMM on the SD820 platform, we find that it is not generally profitable to explicitly move data from global to local memory. Instead, we apply our usual work-blocking strategy, but simply omit input (load) and output (store) code running on the CPU portion of the SD820 SoC. Currently, it is not clear if any other OpenCL BLAS libraries can target the SD820 platform without some significant additional efforts. Thus, research of, profiling of, and comparison against other OpenCL-based BLAS libraries is a good topic for future work.

VI. CODE GENERATION FOR CNN CONVOLUTIONS

As discussed earlier, the BLAS-based or \texttt{im2col()}/\texttt{SGEMM()} approach to performing convolutions has various limitations. Now, we turn our attention to using our framework to generate functions that directly perform convolutions. The first variant we will discuss is a simple fusion of \texttt{im2col()} and \texttt{SGEMM()}. We apply the same basic techniques as in the \texttt{SGEMM()} discussion above, but we fold the behavior of \texttt{im2col()} into the \texttt{KNN()} code block. Or, in other words, we only \texttt{implicitly} create the matrix \texttt{inmat}; we just read the correct elements from \texttt{in} as needed. While this approach is simple, and avoids the memory overhead of creating \texttt{inmat} explicitly, it makes task (1) much more difficult. In particular, both the overhead of additional indexing logic and the resultant poor access patterns reading global memory can make this variant less efficient than \texttt{im2col()+SGEMM()}. However, it provides a starting place for further explorations, and can function as a fallback method for convolutions not handled by more specialized variants, especially for cases with large kernel sizes where the overhead of \texttt{im2col()} is larger. We term this the \texttt{implicit-SGEMM} or \texttt{conv} variant. The next variant we consider exploits the common case where the convolution kernel size \texttt{KSZ} is 1. In this case, various simplifications are possible, and it is relatively easy to use a transformation function over \texttt{in} to ensure a good global memory access pattern. Note that, for \texttt{KSZ = 1} convolutions, per-image \texttt{im2col()} is the

| Size | Communication/Compute | cubLAS Performance | Boda Performance |
|------|------------------------|-------------------|-----------------|
| MKN  | Bytes                  | FLOPs             | Runtime         | GF/s | Speedup |
| 128  | 197KB                  | 4.19MF            | 21.3            | 49.3us | 85.0GF/s |
|      |                        |                   |                 |      |         |
|      |                        |                   |                 | 54.2us | 681GF/s |
| 384  | 1.77MB                 | 113MF             | 64.0            | 63.3us | 1.79TF/s |
|      |                        |                   |                 |      |         |
|      |                        |                   |                 | 80.1us | 1.41TF/s |
| 512  | 3.15MB                 | 268MF             | 85.3            | 107us  | 2.51TF/s |
|      |                        |                   |                 |      |         |
|      |                        |                   |                 | 120us  | 2.24TF/s |
| 768  | 7.08MB                 | 906MF             | 128             | 202us  | 4.94TF/s |
|      |                        |                   |                 |      |         |
|      |                        |                   |                 | 255us  | 3.55TF/s |
| 1024 | 12.6MB                 | 2.15GF            | 171             | 541us  | 3.97TF/s |
|      |                        |                   |                 |      |         |
|      |                        |                   |                 | 602us  | 3.57TF/s |
| 1536 | 28.3MB                 | 7.25GF            | 256             | 1.39ms | 5.22TF/s |
|      |                        |                   |                 |      |         |
|      |                        |                   |                 | 1.63ms | 4.44TF/s |
| 2048 | 50.3MB                 | 17.2GF            | 341             | 3.56ms | 4.83TF/s |
|      |                        |                   |                 |      |         |
|      |                        |                   |                 | 4.08ms | 4.21TF/s |

| Size | Communication/Compute | QBLAS Performance | Boda Performance |
|------|------------------------|-------------------|-----------------|
| MKN  | Bytes                  | FLOPs             | Runtime         | GF/s | Speedup |
| 128  | 197KB                  | 4.19MF            | 21.3            | 500us | 7.5GF/s |
|      |                        |                   |                 |      |         |
|      |                        |                   |                 | 507us | 66GF/s  |
| 256  | 786KB                  | 33.6MF            | 42.7            | 1.7ms  | 20GF/s  |
|      |                        |                   |                 |      |         |
|      |                        |                   |                 | 2.1ms  | 54GF/s  |
| 384  | 1.77MB                 | 113MF             | 64.0            | 3.8ms  | 30GF/s  |
|      |                        |                   |                 |      |         |
|      |                        |                   |                 | 3.6ms  | 74GF/s  |
| 512  | 3.15MB                 | 268MF             | 85.3            | 8.0ms  | 34GF/s  |
|      |                        |                   |                 |      |         |
|      |                        |                   |                 | 11ms   | 78GF/s  |
| 768  | 7.08MB                 | 906MF             | 128             | 23ms   | 39GF/s  |
|      |                        |                   |                 |      |         |
|      |                        |                   |                 | 27ms   | 80GF/s  |
| 1024 | 12.6MB                 | 2.15GF            | 171             | 544ms  | 40GF/s  |
|      |                        |                   |                 |      |         |
|      |                        |                   |                 | 89ms   | 81GF/s  |
| 1536 | 28.3MB                 | 7.25GF            | 256             | 175ms  | 41GF/s  |
|      |                        |                   |                 |      |         |
|      |                        |                   |                 | 223ms  | 77GF/s  |
| 2048 | 50.3MB                 | 17.2GF            | 341             | 401ms  | 42GF/s  |
|      |                        |                   |                 |      |         |
|      |                        |                   |                 | 501ms  | 41GF/s  |

TABLE I

SGEMM OPERATION SPEED AND EFFICIENCY: cubLAS VS. Boda

TABLE II

SGEMM OPERATION SPEED AND EFFICIENCY: QBLAS VS. Boda
identity function; thus the k1conv variant is quite similar to SGEMM. The final variant we consider, termed tconv (tiled convolution), is targeted at the commonly occurring cases of kernel sizes in the range $[2, \sim 11]$, with reasonable widths for $in$ (perhaps in the range $[KSZ \times 5, KSZ \times 50]$). In this case, we can perform some additional optimizations:

- We can fully unroll over the $X$ dimension of the kernel. This uses significant extra local memory and registers, but allows sharing of $in$ row data in registers across unrollings of the inner loop.
- We can load entire $X/Y$ tiles of $in$ at the workgroup level. Even for kernels as small as $2 \times 2$, this vastly reduces the amount of data that must be loaded from global memory for $in$. The reduction is a factor of $(KSZ/stride)^2$; this is naturally the same factor by which im2col() is expansive.

Again, an input transformation must be applied to $in$ to help simplify indexing logic and improve memory access patterns.

For benchmarking, we consider a range of convolutions drawn from three common CNNs: AlexNet [6], NiN [33], and GoogLeNetV1 [19]. For each network, we consider batch sizes $B$ of 1, 5, and 20. We then gather all the unique convolution operations, of which there are $\sim 180$. While some operations are duplicated within some networks, and the mixing together of operations from different batch sizes is perhaps not ideal, this set of operations represents a reasonable set over which low total runtime (summed over all operations) is desired. That is, absolute efficiency is generally less important than absolute runtime, and total runtime tends to be dominated by the larger convolutions. That said, high efficiency across a broad range of problems sizes is still desirable. Each particular network, batch size, and overall use case requires some particular subset of convolutions. As with SGEMM, we initially compare our convolutions against Nvidia’s cuDNN library on an Nvidia Titan-X. Due to space limitations, we do not present the full results of that experiment here, but only summarize them. In brief, as with SGEMM, we achieve reasonable performance, albeit with a few weeks of effort rather than a few days. Compared to SGEMM, tuning convolutions took more time for various reasons. This was the both the author’s first experience at implementing high efficiency code on Maxwell GPUs as well as the author’s first attempt at implementing convolutions; both of these incurred a substantial learning curve penalty. Beyond that, the design space for convolution seems to be more complex and varied than that of SGEMM; while this does offer more potential for optimization, it certainly also increases development time to the degree one attempts to explore and exploit the space. Note that of the $\sim 180$ convolutions, almost all are handled by either the k1conv or tconv variant. Only a few cases fall though to the conv variant. Both k1conv and tconv provide a 2x or more speedup over conv. Now, we turn to our main focus in this work of targeting the SD820 platform. As with the SGEMM case, our main task is to manually vectorize loads and stores. Additionally, as with SGEMM, we avoid the explicit use of local memory, and instead rely on cache for global memory bandwidth amplification. So far, we have only implemented two new variants for the SD820 platform: conv_simd and k1conv_simd, which are manually load/store vectorized versions of their non-simd counterparts. As with the Nvidia case, the k1conv_simd variant provides significant speedup over the fallback conv_simd variant. Detailed speed results are presented for the SD820 platform in the next section. Given the knowledge gained from implementing SGEMM on the SD820, it took only a few days to create these new variants. As with SGEMM, progress was hindered due to lack of documentation and tools. Such things are undoubtedly available inside of corporations, and we hope the potential for higher performance CNN implementations will encourage vendors to make them available to programmers.

VII. Results

![Fig. 6. Speedup of k1conv_simd over conv_simd on SD820 platform.](image)

Here, for the SD820 platform, we show the speed of the OpenCL code generated by our framework for our benchmark set of convolutions. In Figure 6, we show the benefit of the k1conv_simd variant for the convolutions to which it can be applied: those with size 1 kernels. In Figures 7 and 8, we show the absolute performance of our framework’s generated code for each benchmark convolution. As per the graph legend, for each convolution, we indicate which variant was selected. Inspecting the results, it can be seen that there are many convolutions with high arithmetic intensity (AI) that perform worse than those with lower AI. This is due to the fact that the higher performing cases are using the higher-efficiency k1conv_simd variant. Based on our experience with the Nvidia platform, we predict that implementing a tconv_simd variant for the SD820 platform will greatly improve the performance of most of the cases currently using the fallback conv_simd variant. Given the lack of a vendor CNN library or other libraries to
Convolutional Neural Nets are of growing importance in a broad range of applications, and particularly in computer vision systems used in self-driving cars, medical imaging, and a variety of consumer-facing applications such as face identification in social media. As both the research and development communities continue to grow, interest in productive deployment of CNNs across many platforms and application domains will only increase; however, the number of programmers capable of efficiently implementing CNN operations is very limited, and the keys for efficient implementations are not widely known. As a result, support for high efficiency CNN calculation is currently limited to only a few hardware platforms. In the Boda framework described in this paper we have aspired to bridge the performance-portability gap for the key CNN operations and to bring such operations to a more even footing across various hardware platforms when compared with existing high efficiency approaches. We have demonstrated our approach with a case study of tuning CNN deployment computations for the Snapdragon 820 mobile computing platform. By offering competitive performance and superior portability, we feel this work will positively impact the ability of the research and development communities to experiment with the deployment of CNNs across a wide range of platforms for an ever-broadening range of applications.

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VIII. CONCLUSIONS

directly compare against, it is difficult to know how close our performance is to optimal. From the SD820 roofline curve in Figure 2 we know there is significant headroom over our results in terms of peak compute performance. While our limited knowledge of the SD820’s on-chip memory subsystems makes a determination difficult, in many cases it seems likely we are limited by cache and/or global memory bandwidth. Thus, usage of smaller data types for storage (e.g. half-precision floats) and/or using hardware support for texture access are natural candidates to achieve additional improvements.
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