Design Of Two Stage CMOS Operational Amplifier in 180nm Technology

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Abstract—In this paper a CMOS two stage operational amplifier has been presented which operates at 1.8 V power supply at 0.18 micron (i.e., 180 nm) technology and whose input is depended on Bias Current. The op-amp provides a gain of 63dB and a bandwidth of 140 kHz for a load of 1 pF. This op-amp has a Common Mode gain of -25 dB, an output slew rate of 32 \( \text{V}/\mu\text{s} \), and a output voltage swing. The power consumption for the op-amp is 300\(\mu\text{W}\).

Index Terms—Phase Margin, Gain Bandwidth Product, CMRR, ICMR, CMOS Analog circuit.

I. INTRODUCTION

The trend towards low voltage low power silicon chip systems has been growing due to the increasing demand of smaller size and longer battery life for portable applications in all marketing segments including telecommunications, medical, computers and consumer electronics. The operational amplifier is undoubtedly one of the most useful devices in analog electronic circuitry. Op-amps are built with different levels of complexity to be used to realize functions ranging from a simple dc bias generation to high speed amplifications or filtering. With only a handful of external components, it can perform a wide variety of analog signal processing tasks. Op-amps are among the most widely used electronic devices today, being used in a vast array of consumer, industrial, and scientific devices. Operational Amplifiers, more commonly known as Op-amps, are among the most widely used building blocks in Analog Electronic Circuits.

Op-amps are linear devices which has nearly all the properties required for not only ideal DC amplification but is used extensively for signal conditioning, filtering and for performing mathematical operations such as addition, subtraction, integration, differentiation etc. Generally an Operational Amplifier is a 3-terminal device. It consists mainly of an Inverting input denoted by a negative sign, ("-"), and the other a Non-inverting input denoted by a positive sign ("+") in the symbol for op-amp. Both these inputs are very high impedance. The output signal of an Operational Amplifier is the amplified difference between the two input signals or in other words the amplified differential input. Generally the input stage of an Operational Amplifier is often a differential amplifier.

An operational amplifier is a DC-coupled differential input voltage amplifier with an rather high gain. In most general purpose op-amps there is a single ended output. Usually an op-amp produces an output voltage a million times larger than the voltage difference across its two input terminals. For most general applications of an opamp a negative feedback is used to control the large voltage gain. The negative feedback also largely determines the magnitude of its output (“closed-loop”) voltage gain in numerous amplifier applications, or the transfer function required. The op-amp acts as a comparator when used without negative feedback, and even in certain applications with positive feedback for regeneration. An ideal Opamp is characterized by a very high input impedance (ideally infinite) and low output impedance at the output terminal(s) (ideally zero), to put it simply the op-amp is one type of differential amplifier. This section briefly discusses the basic concept of op-amp. An amplifier with the general characteristics of very high voltage gain, very high input resistance, and very low output resistance generally is referred to as an op-amp. Most analog applications use an Op-Amp that has some amount of negative feedback. The Negative feedback is used to tell the Op-Amp how much to amplify a signal. And since op-amps are so extensively used to implement a feedback system, the required precision of the closed loop circuit determines the open loop gain of the system.

For this design process, we will first demonstrate the formula of main properties of an operational amplifier in Section II than we will introduce how we find the proper parameters for our design in Section III the simulation result of out design will be presented in Section IV.

II. THEORETICAL ANALYSIS

A. MOSFET ans Two Stage amp

For MOSFET we have several basic parameters including

\[
i_D = \frac{1}{2} k_n \left( \frac{W}{L} \right) (V_{GS} - V_{TN})^2
\]

and

\[
g_m = \sqrt{2k_n \left( \frac{W}{L} \right) \cdot \sqrt{T_D}}
\]

for calculation, we have parameters \( k_n = 170\mu\text{A/V}^2 \) and \( k_p = 36\mu\text{A/V}^2 \). 
B. Gain, Pole and Zeros

We define the input $V_{in}$, the output voltage of the first stage, i.e., the input voltage of the second stage $V_1$, and the output voltage of the whole circuit $V_{out}$, so we can get that for two stage operational amplifier we have

$$\frac{V_{out}}{V_{in}} = \frac{V_{out}}{V_1} \times \frac{V_1}{V_{in}}$$

so we can calculate the voltage gain of two stage separately and then combine together.

We set the output resistance of the first stage $R_{o2} \parallel R_{o4}$ as $R_1$ and the output resistance of the second stage $R_{o6} \parallel R_{o7}$ as $R_2$. We also see the output capacitance of the first stage as $C_1$ and second stage as $C_2 \approx C_L$ for the second stage. So we finally get that

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1} R_1 \times g_{m2} R_2 \times (1 - \frac{sC_2}{g_{m2}})}{as^2 + bs + 1}$$

with

$$a = R_1 R_2 (C_1 C_2 + C_1 C_L + C_2 C_L)$$

$$b = R_2 (C_c + C_2) + R_1 (C_c + C_1) + C_c g_{m2} R_1 R_2$$

and

$$g_{m1} = \sqrt{2K_p (\frac{W}{L})} I_{D1}$$

$$g_{m2} = \sqrt{2K_n (\frac{W}{L})} I_{D6}$$

to find the poles and zeros, we must transform the equation into form like

$$\frac{V_{out}}{V_{in}} = \frac{A_{dc} (1 - \frac{s}{Z_1})}{(1 + \frac{s}{p_1})(1 + \frac{s}{p_2})}$$

here for this two stage amplifier we have the DC gain of the amplifier

$$A_{dc} = g_{m1} R_1 \times g_{m2} R_2$$

the zero point of the circuit

$$Z_1 = \frac{g_{m2}}{C_2}$$

, and with a external resistor,

$$Z_1 = \frac{1}{C_c \left( \frac{1}{g_{m2}} - R_z \right)}$$

so we could set

$$R_z = \frac{1}{g_{m2}}$$

When it comes to the poles of the circuit, approximately we have

$$P_1 \approx \frac{1}{b}$$

we can simply it to

$$P_1 \approx \frac{1}{C_c g_{m2} R_1 R_2}$$

for another pole $P_2$ we have

$$P_2 \approx \frac{g_{m2} C_c}{C_1 C_2 + C_1 C_L + C_2 C_L}$$

$C_1$ is very small so we can simply it into

$$P_2 \approx \frac{g_{m2}}{C_1 + C_2}$$

C. Phase Margin

The gain band with GBW is equal to $DC_{gain} \times P_1 = \frac{g_{m1}}{C_c}$

For phase margin, we have

$$\angle \frac{V_{out}}{V_{in}} = - \arctan(\frac{\omega}{z}) - \arctan(\frac{\omega}{p_1}) - \arctan(\frac{\omega}{p_2})$$

and we have

$$z = 10 \times GBW$$

by substituting

$$\angle \frac{V_{out}}{V_{in}} = - \arctan(\frac{GBW}{z}) - \arctan(\frac{GBW}{p_1}) - \arctan(\frac{GBW}{p_2})$$

so

$$\angle \frac{V_{out}}{V_{in}} = - \arctan(\frac{1}{10}) - \arctan(A_{DC}) - \arctan(\frac{GBW}{p_2})$$

then we need

$$p_2 \geq 2.2 \text{GBW}$$

and finally

$$C_c > 0.22 C_L$$

to get more than 60° phase margin. Thus we also have

$$\frac{g_{m1}}{g_{m2}} \leq 0.22$$

D. Slew Rate

In our design, the slew rate is just equal to

$$\text{slewrate} = \frac{I_5}{C_c}$$

we already have $I_5 = 100 \mu A$ so $C_c$ must be under 10C, with is certain to full-fill. Here we need to obtain $10MV/s$ slew rate under $100MHZ$, so we need the voltage change more than $0.05V$ in one pulse, which is 5ns in width.

E. Power

The power of the op-amp can be calculated by

$$I_{total} \times V_{dd}$$

III. DESIGN PROCEDURE

A. Design Goal

**Bonus:** Design your opamp such that the specifications are met under a ±10% variation of the supply voltage.
### TABLE I  
**The Design Goal of the Operational Amplifier**

| Parameters                                | Design Goal   |
|-------------------------------------------|---------------|
| Process                                   | 0.18µm CMOS   |
| $V_{DD}$                                  | 1.8V          |
| $V_{SS}$                                  | 0V            |
| Load                                      | 1pF           |
| Phase margin                              | $\geq 60^\circ$ |
| $A_{DM0}$                                 | $\geq 1000V/V$ (60dB) |
| $A_{CM0}$                                 | $\leq 0.1V/V$ (-20dB) |
| Unity gain frequency                      | $\geq 100MHz$ |
| Slew rate                                 | $\geq 10V/\mu s$ |
| Output voltage swing (differential peak to peak) | $\geq 800mVpp$ |
| Power                                     | Minimum       |

#### B. Design Principle

The minimum size of the MOSFET we can use is 180nm in length and 400nm in width, but normally we don’t use the minimum channel length due to the increase of the $L$. $L > 2L_{\text{min}}$ is recommended, in this design, we use $L = 1\mu m$. And after initially designed, to optimise the performance of the op-amp, we will adjust the length of some MOSFET while keep the $(W/L)$ unchanged.

To control the systematic offset we set

\[
\frac{(W/L)_3}{(W/L)_6} = \frac{(W/L)_4}{(W/L)_9} = \frac{(W/L)_5}{2 \times (W/L)_7}
\]

We also have

\[
\frac{(W/L)_8}{(W/L)_5} = \frac{I_{\text{ref}}}{I_5}
\]

and

\[
\frac{(W/L)_8}{(W/L)_7} = \frac{I_{\text{ref}}}{I_7}
\]

During the procedure of the design, we first calculate the proper value of the compensate capacitance and resistance, then we will design the first stage, finally the second stage will be designed.

#### C. Parameter Optimization

1) **Design of $C_c$**: To satisfy the phase margin of $60^\circ$ we need $C_c \geq 0.22C_L$, since we have $C_L = 1pF$ so we can use $C_c \geq 2200fF$. To achieve slew rate $10V/\mu s$ we need $C_e = 10pF$, to meet a balance between two requirement, and we choose $C_e = 3pF$

2) **Design of $M1$ and $M2$**: We have

\[
g_{m1} = GBW \times C_c \times 2\pi
\]

and GBW is also called unity gain frequency, which is listed in the design goal with value of 100MHZ. So we need to apply that

\[
g_{m1} = 100MHz \times 5pF \times 2\pi = 302\mu
\]

and for convince we choose a litter larger value 510µ. Since

\[
\frac{W}{L} = \frac{g_m^2}{\mu_n C_{ox} \times 2I_D}
\]

and $2I_D = I_5 = 100\mu A$, fianly we get

\[
\frac{W}{L} = 14.8
\]

so we use 20 as the final value of the ratio.

3) **Design of $M3$ and $M4$**: To get more than 800mV of the output range, we need to at least 800mV input common mode voltage range before the zero point, where the gain is 1. This characteristic parameter can also be used to determine the size of the MOSFET M1 and M2. We have

\[
\frac{W}{L} = \frac{2I_{D3}}{\mu_n C_{OX} (V_{DD} - ICMR(+) - V_{TH1} + V_{TH3})^2}
\]

we choose ICMR(+) at 1.6V and we get $(\frac{W}{L})_{3,4} \approx 50$.

4) **Design of $M5$ and $M8$**: In the mean while, we also need to fit the proper value of ICMR(-) to determine the size of MOSFET M5. We have

\[
\frac{W}{L} = \frac{2U_{D5}}{\mu_n C_{OX} (V_{DSat})^2} = \frac{2I_{D5}}{\mu_n C_{OX} (V_{DSat})^2}
\]

with

\[
V_{DSat} = ICMR(-) - \sqrt{\frac{2I_{D1}}{\beta_1}} - V_{TH1}
\]

Approximately we can choose $(\frac{W}{L})_5 = 30$ and $(\frac{W}{L})_8 = 10$.

5) **Design of $M6$**: And also we need $g_{m2} \geq \frac{g_{m1} - I_{D4}}{\mu_n}$, so we need $g_{m2} \geq 2318\mu$, we want

\[
V_{DS3} = V_{DS4} = V_{DS6}
\]

and

\[
V_{GS3} = V_{GS4} = V_{GS6}
\]

So we need

\[
\frac{W}{L} = \frac{I_6}{I_4} = \frac{g_{m2}}{g_{m4}}
\]

so here we get

\[
I_6 = 2.5 \times I_4
\]

\[
(\frac{W}{L})_6 = 150
\]

6) **Design of $M7$**:

\[
\frac{W}{L} = \frac{I_7}{I_5} = \frac{g_{m7}}{g_{m5}}
\]

\[
(\frac{W}{L})_7 = (\frac{W}{L})_5 = 10
\]

7) **Design of $R_z$**:

\[
R_z = \frac{1}{g_{m2}} = 5k
\]

8) **Common and differential mode gain**: After initially determining the parameters of the MOSFETs, we need to check output voltage gain, than we may need to adjust the parameters to meet the requirements of common and differential mode voltage gain.
TABLE II
THE PARAMETERS OF MOSFETS

| Device | Length (L) | Width (W) | W/L |
|--------|------------|-----------|-----|
| M1     | 1µ       | 20µ       | 20  |
| M2     | 1µ       | 20µ       | 20  |
| M3     | 1µ       | 50µ       | 50  |
| M4     | 1µ       | 50µ       | 50  |
| M5     | 50µ      | 39µ       | 39  |
| M6     | 100µ     | 20µ       | 111 |
| M7     | 1µ       | 30µ       | 30  |
| M8     | 1µ       | 10µ       | 10  |

Parameter | Design |
---|---|
$c_c$ | 2pF |
$R_c$ | 7kΩ |
$T$ | 10mA |

TABLE III
THE DESIGN RESULT

| Parameter | Target | Achieved | Plot |
|-----------|--------|----------|------|
| Phase margin | $\geq 60^\circ$ | 61.8° | Fig 6 |
| $A_{DAM}$ | $\geq 1000V/V$ (60dB) | 67.5dB | Fig 4 |
| $A_{CAM}$ | $\leq 0.1V/V$ (-20dB) | -20.5dB | Fig 5 |
| Unity gain frequency | $\geq 100MHz$ | 131.9MHz | Fig 8 |
| Slew rate (Rise) | $\geq 10V/\mu s$ | 20.7V/\mu s | Fig 6 |
| Slew rate (Fall) | $\geq 10V/\mu s$ | 12.6V/\mu s | Fig 7 |
| Output voltage swing | $\geq 800mVpp$ | 936mV | Fig 6 |
| Power | Minimum | 204µW | Fig 2 |

IV. OUR DESIGN

After we initially determine the parameters, we use Parameter Analysis in Cadence Virtuoso to optimize our design and finally we get the design as shown in Table II and the simulation results are in Table III.

The final design schematic is named project-final.

V. CONCLUSION

In this design, we have satisfied all the parameters in the requirement and specially we achieved high $A_{dm}$, slew rate and wide unity gain phase margin. By comparison we found that the simulation result is a little different from out theoretical design due to some omitting during our calculation. But after all, our calculation has represent the real situation and offered great help in the design of the device.

VI. APPENDIX
Fig. 6. Simulation result of raise slew rate

Fig. 7. The output voltage swing and fall slew rate

Fig. 8. Phase margin and unity gain frequency

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