Abstract

Recently, pattern recognition technologies such as character recognition and finger print recognition are used in various fields. Accordingly, the retrieval technology is becoming important to retrieve the most similar data from a huge database. However, the real-time search is difficult for a software approach, because a digital computer must compare the called data sequentially. To solve this problem, an associative memory has been studied in order to retrieve the reference data which is the most similar to an input data. The associative memory is one of functional memories which is capable of high-speed retrieving for the most similar data by operating parallel. Human brain can retrieve the most similar data to the input data instantly, because it processes information parallel. Accordingly we have focused a neuron CMOS inverter which has characteristics of the brain neuron. In the associative memory, the Hamming distance search circuit is one of the most important circuit to achieve real-time search. In this paper, we propose a wide range Hamming distance search circuit by utilizing neuron CMOS inverters. Unlike conventional circuits, the proposed circuit can retrieve all reference data within a specified Hamming distance.

Keywords: Associative Memory, Hamming Distance, Neuron CMOS Inverter, Time domain

1. Introduction

According to the development of information technologies, pattern recognition technologies such as character recognition and fingerprint recognition are used in various fields. In the pattern recognition technology, high-speed searching is a basic and important process to retrieve the most similar data from a huge database. Also, this process is often used in data compression and network control. For these reasons, the improvement of its performance is strongly desired. However, the search technique implemented into a software program takes a long processing time to retrieve the most similar data, because a digital computer must compare the called data sequentially. Therefore, the real-time search is difficult for a software approach. On the other hand, in the case of traditional hardware approaches, it also takes a long time, because the basic operation of the traditional hardware approach is the same as that of the software approach. In order to solve these problems, the study has been conducted on an associative memory in recent years\(^{1-4}\). The associative memory with a traditional memory function can retrieve not only perfect matched data but also the most similar data at a high-speed in addition to the functions of a conventional memory.

In the case of a human being, we can instantly retrieve the most similar data from a huge number of memory data, because the memory system of human is operated in parallel unlike the storage memory of a digital computer. In previous studies, we have focused on a neuron CMOS inverter which has characteristics similar to a brain neuron\(^{5}\). By utilizing the neuron CMOS inverters, the authors proposed a minimum Hamming distance search associative memory which can achieve parallel high-speed operation\(^{6}\). The neuron CMOS inverter has multiple input terminals and one floating gate, where the input terminals...
are coupled capacitively with the floating gate. Depending on the threshold voltage of neuron CMOS inverter and the floating gate voltage, the neuron CMOS inverter performs the switching operation, where the floating gate voltage is determined by the weighted average of input voltages and capacitances. In our associative memory suggested in\(^6\), the reference data which is the most similar to an input data is retrieved from a huge database, where the Hamming distance search circuit is one of the most important circuits to achieve real-time search. However, the associative memory can retrieve only the most similar data and matching data.

In this paper, we propose a wide range Hamming distance search circuit by utilizing the neuron CMOS inverters. When the Hamming distance is specified from outside, the proposed circuit can retrieve all reference data within the Hamming distance. Also, the proposed circuit can remove the influence caused by the initial charge of a floating gates and the variation of a threshold voltage, because the voltage of the floating gate is equal to the threshold voltage by connecting the output of the neuron CMOS inverter to the floating gate before search operation. To clarify the characteristics of the proposed circuit, SPICE simulations are performed concerning the proposed circuit designed by the Rohm 0.18\(\mu\)m CMOS process.

2. Circuit Configuration

2.1 Data Coincidence Detector

First, we describe a data coincidence detector using the neuron CMOS inverter which is the most important building block of the proposed circuit. Figure 1 illustrates the circuit configuration of the data coincidence detector. The equivalent circuit of Figure 1 can be expressed as shown in Figure 2. In these figures, \(A = (a_1, \ldots, a_i, \ldots, a_N)\) \((i = 1, 2, \ldots, N)\) and \(B = (b_1, \ldots, b_i, \ldots, b_N)\) denote the input data and the reference data, respectively. The \(V_{DD}\) is the supply voltage, \(F\) is the control signal to start the operation of retrieving for matching data, and \(G\) is the control signal for the most similar data search. Each switch is constituted by MOS transistors, where \(SW_1\) is the switch for setting up the floating gate voltage \(V_F\) of the neuron CMOS inverter \(\nu\)CMOS to the threshold voltage \(V_{TH}\) and \(SW_2\) is the switch to enable the coincidence detection.

The neuron CMOS inverter \(\nu\)CMOS of Figure 1 is equivalent to an inverter constituted by capacitors \(C\) and MOS transistors \(M_1\) and \(M_2\), where all the capacitors \(C\)

![Figure 1. Circuit configuration of the data coincidence detector using neuron CMOS inverter.](image1)

![Figure 2. Equivalent circuit of Figure 1.](image2)

have the same value. The Hamming distance \(D_{\text{Hamm}}\) is the number of different bits between the input data \(A\) and the reference data \(B\) and is defined as follows:

\[
D_{\text{Hamm}} = \sum_{i=1}^{N} (a_i \oplus b_i)
\]

Where \(\oplus\) is an exclusive-OR operator.

The operation principle of the data coincidence detector using the neuron CMOS inverter is described as follows: First, the control signal \(F\) is prepared to a low level, \(G\) is prepared to a high level, the switch \(SW_1\) is turned “ON,” and \(SW_2\) is connected to the floating gate.
Under these conditions, the floating gate voltage $V_f$ of neuron CMOS inverter vCMOS would be as follows:

$$V_f = V_{TH}$$  \hspace{1cm} (2)

Here, since $F$ is at a low level, all the outputs of NAND become a high level and the output $OUT$ becomes a low level.

Second, after $SW_i$ is changed to “OFF”, $SW_i$ is switched to the upper side. At this timing, the behavior of the floating gate voltage $V_f$ is as follows. When the voltage of one input terminal is changed, the variation of the floating gate voltage $V_f$, $\Delta V_f$, is expressed as

$$\Delta V_f = \frac{C}{C_T} \Delta V$$  \hspace{1cm} (3)

Where, $C_T$ is the total of the capacitance between the input terminals and the floating gate and the capacitance $C_p$ between the floating gate and the substrate, and is shown as:

$$C_T = (N + 1)C + C_p$$  \hspace{1cm} (4)

The voltage of the lowest input terminal $V_{N+1}$ becomes $V_{DD}$ from $V_{TH}$ when $SW_i$ is connected to the upper side. In this case, from Equation (2) and Equation (3), the floating gate voltage $V_f$ is expressed as:

$$V_f = V_{TH} + \frac{C}{C_T} (V_{DD} - V_{TH})$$  \hspace{1cm} (5)

As you can see from Equation (5), $V_f$ exceeds the threshold voltage $V_{TH}$, because the supply voltage $V_{DD}$ exceeds the threshold voltage $V_{TH}$. Therefore, the output $V'_{OUT}$ of vCMOS becomes a low level.

Next, when the control signal $F$ is set to a high level, the output $V_f$ of NAND changes from a high level to a low level if the $i$-th bit of the input data, $a_i$, and the $i$-th bit of the reference data, $b_i$, are not equal. In other words, the outputs $V_f$ become $0V$ from $V_{DD}$ according to the number of the Hamming distance $D_{Hamm}$ between the input data $A=(a_1, \ldots, a_i, \ldots, a_n)$ and the reference data $B=(b_1, \ldots, b_i, \ldots, b_n)$. By combining Equation (3) and Equation (5), the floating gate $V_f$ can be defined as

$$V_f' = V_{TH} + \frac{C}{C_T} (V_{DD} - V_{TH}) - D_{Hamm} \frac{C}{C_T} V_{DD}$$  \hspace{1cm} (6)

From Equation (6), the output $V'_{OUT}$ of vCMOS becomes a high level. On the other hand, the output $OUT$ does not change from a low level, because $V_f$ is lower than the threshold voltage $V_{TH}$.

When the input data $A=(a_1, \ldots, a_i, \ldots, a_n)$ is fully equal to the reference data $B=(b_1, \ldots, b_i, \ldots, b_n)$, the floating gate voltage $V_f$ does not change from Equation (5) because all the outputs $V_f$ of NAND remain a high level. Therefore, the output $V'_{OUT}$ of vCMOS remains a low level and the output $OUT$ becomes a high level. Owing to this operation, the data coincidence detector can retrieve the matching data at the time when the control signal $F$ becomes a high level.

As Equation (6) shows, the floating gate voltage $V_f'$ decreases in proportion to the Hamming distance $D_{Hamm}$ if the input data $A=(a_1, \ldots, a_i, \ldots, a_n)$ is not equal to the reference data $B=(b_1, \ldots, b_i, \ldots, b_n)$. When the control signal $G$ is changed to a low level, the MOS transistor $M_1$ is switched to “ON” and the constant current flows from the current mirror circuit which is constituted by $M_1$, $M_2$, and resistor $R$. Therefore, the floating gate voltage $V_f$ starts to increase linearly from $V_f'$. When $V_f$ exceeds the threshold voltage $V_{TH}$ of vCMOS, the output $V'_{OUT}$ of vCMOS becomes a low level and the output $OUT$ becomes a high level. When the current that flows through the MOS transistor $M_1$ is defined as $I$, the time taken from the control signal $G$ becomes a low level to the output $OUT$ becomes a high level is shown as:

$$T = \frac{C_T (V_{TH} - V_f')}{I}$$  \hspace{1cm} (7)

By substituting Equation (6) for Equation (7), the time $T$ is expressed as

$$T = \frac{C_T \left\{ \frac{C}{C_T} (V_{DD} - V_{TH}) + D_{Hamm} \frac{C}{C_T} V_{DD} \right\}}{I}$$  \hspace{1cm} (8)

The time $T$ of Equation (8) can be rewritten as

$$T = D_{Hamm} \frac{C}{I} V_{DD} - \frac{C}{I} (V_{DD} - V_{TH})$$  \hspace{1cm} (9)

As you can see from Equation (9), the time $T$ is not affected by the parasitic capacitance and the initial charge. From Equation (9), the time lag $\Delta T$ in the case of the difference of one Hamming distance is expressed as

$$\Delta T = \frac{C}{I} V_{DD}$$  \hspace{1cm} (10)

From this Equation, the time lag for the difference of the Hamming distance is invariant to the variation of the threshold voltage caused by the variation of temperature and manufacturing process.
3.2 Wide Range Hamming Distance Search Circuit

Figure 3 shows the circuit configuration of the proposed wide range Hamming distance search circuit using neuron CMOS inverters. The proposed circuit consists of \( M + 1 \) data coincidence detectors, where \( M \) corresponds to the number of the reference data and “+1” corresponds to the detector in order to specify the range of the Hamming distance. The output of OR is connected to the gate terminal of MOS transistor \( M_3 \) of the data coincidence detectors.

Figure 3. Circuit configuration of a wide range Hamming distance search circuit using neuron CMOS inverters.

In Figure 3, \( A = (a_1, \ldots, a_i, \ldots, a_N) \) is the input data, \( B_j = (b_{1,j}, \ldots, b_{i,j}, \ldots, b_{N,j}) \) \((j = 1, 2, \ldots, M)\) is the reference data, \( D = (d_1, \ldots, d_i, \ldots, d_N) \) is the control signal for specifying the search range of the Hamming distance. The control signal \( D \) is set to a high level as many as the number of the Hamming distance corresponding to the search range.

We describe the operation principle of the proposed circuit. After the proposed circuit performs the above operations, if the control signal \( F \) is set to a high level, all the MOS transistors \( M_3 \) of the data coincidence detectors become “ON”. Therefore, the constant current from the current mirror circuit which is constituted by the MOS transistor \( M_1, M_2 \) and the resister \( R \) flows. Then charging to all floating gates is started. The voltage of the floating gate increases linearly. When the output of the data coincidence detector for the specifying the range becomes “ON,” all the MOS transistor \( M_j \) is turned “OFF”. Then charging to the floating gate is stopped. The data coincidence detector converts the Hamming distance into the time. In other words, the time taken to the output of the data coincidence detector for specifying the range becomes a high level is in proportion to the number of high level in \( D \). Therefore, the \( OUT \) of points that have the reference data within the specified Hamming distance becomes a high level. By the above operation, the proposed circuit can retrieve all the reference data within the specified Hamming distance in plurality reference data.

4. Simulation

Using the Rohm 0.18 \( \mu \)m CMOS process as a transistor model, the HSPICE simulation of the proposed circuit with 64-bits and 64-words was performed. In this simulation, the supply voltage \( V_{DD} \) is applied 1.8V and the threshold voltage \( V_{TH} \) of the neuron CMOS inverters is set to 0.9V that is a half of the supply voltage \( V_{DD} \). Table 1 shows specifications used in the simulation of the proposed circuit, and Table 2 shows performance specifications of the proposed circuit. Table 2 shows the search time of the simulation until 32 Hamming distance that is half of 64-bits. Because, the proposed circuit can retrieve only the reference data within the half of the number of bits by setting the floating gate to the half of the threshold voltage. In the simulation of the proposed circuit, four inputs signals at high level are given as the control signal \( D \) for specifying the search range. In other words,
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Indian Journal of Science and Technology
Vol 9 (28) | July 2016 | www.indjst.org

The four Hamming distance reaches to the threshold voltage before the floating gate voltage of the data coincidence detector for specifying the range reaches the threshold voltage and the charging is stopped.

5. Conclusion

In this paper, we proposed a wide range Hamming distance search circuit using neuron CMOS inverters. First, the proposed circuit converts the Hamming distance to the voltage of the floating gate. Then, the voltage is converted into the time until the floating gate voltage reaches to the threshold voltage and the output is inverted by charging to the floating gate. By comparing the time, the proposed circuit retrieves for the reference data within the range. The proposed circuit can achieve a high-speed operation, because the neuron CMOS inverter can compare input data with reference data in parallel manner.

Furthermore, the proposed circuit can eliminate the influence of the initial charge and the variation of the threshold voltage by connecting the output of the neuron CMOS inverter to the floating gate before the retrieving operation.

In the future, we are going to integrate the proposed circuit. Furthermore, we would like to verify the specification of the proposed circuit by the experiment using the IC chip.

6. References

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Table 1. An example of the I/O data in SPICE simulations

| Input data | Reference data | Hamming distance | Range specification | Output |
|------------|----------------|------------------|---------------------|--------|
| A (11…111111) | B(11…111110000) | 2 | OUT<sub>1</sub> | ...
| B(11…111110000) | B(11…111110000) | 3 | OUT<sub>2</sub> | ...
| B(11…111110000) | B(11…111110000) | 4 | OUT<sub>3</sub> | ...
| B(11…111100000) | B(11…111100000) | 5 | OUT<sub>4</sub> | ...
| B(11…110000000) | B(11…110000000) | 6 | OUT<sub>5</sub> | ...
| B(11…100000000) | B(11…100000000) | 7 | OUT<sub>6</sub> | ...
| B(11…000000000) | B(11…000000000) | 8 | OUT<sub>7</sub> | ...
| B(11…000000000) | B(11…000000000) | 9 | OUT<sub>8</sub> | ...
| B(11…000000000) | B(11…000000000) | 10 | OUT<sub>9</sub> | ...

Table 2. Performance specifications of the proposed circuit

| Process | Rohm 0.18μmCMOS |
|---------|-----------------|
| Organization | 64-bit, 64-word |
| Supply voltage | 1.8V |
| Search time | 4ns-74ns(32bit) |

Figure 4. Simulated results of the proposed circuit.