Research on MMC Voltage Equalization Control Strategy Based on Optimal Sorting Algorithm

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Abstract. The voltage sharing control strategy based on sorting algorithm is widely used in modular multilevel converter Converter (MMC) in practical engineering, aiming at the problems of frequent switching states, high switching frequency and large loss caused by traditional scheduling algorithm, a voltage sharing control strategy based on optimal sequencing is proposed by introducing the average value of capacitor voltage and the maximum deviation threshold under the premise of considering the switching state of sub-modules at the last moment. Finally, the simulation system of modular multilevel converter is built in PSCAD / EMTDC for verification. The simulation results show that the proposed optimal sequence voltage sharing control strategy significantly reduces the switching frequency of the devices and improves the operation performance of the system.

Keywords: Modular multilevel converter, voltage balancing, average value, maximum deviation threshold, switching frequency.

1. Introduction
With the development of power electronics technology, converters based on fully-controlled devices can effectively control active and reactive power without requiring additional reactive power compensation devices, and the output waveform is better. The modular multilevel converter (MMC) is easy to realize a large number of levels, can provide a common DC side, and is easy to realize back-to-back connection, which is very suitable for flexible DC transmission applications. In actual projects, we can meet the voltage and required power requirements by adjusting the number of sub-modules in series with the bridge arms. However, due to the characteristics of the modular structure, MMC also has many problems. Due to the large number of modular multi-level cascaded sub-modules, the IGBT contained in a single sub-module will inevitably have differences in switching losses and trigger pulses during operation, which will cause the sub-module capacitor voltage to be difficult to control, and it is impossible to Support the DC side voltage, causing equipment damage. Therefore, an appropriate control strategy must not only ensure the continuous balance of the capacitor voltage, but also achieve the optimal utilization of capacitor energy storage and the uniform distribution of valve losses. With the continuous increase of the number of sub-modules, the calculation amount of the sorting method becomes complicated, occupies a lot of resources, and seriously affects the stability of system operation. Therefore, many scholars have optimized and improved the traditional sorting algorithm. Literature [3] puts forward the concept of virtual sub-module and mapping based on the
carrier-stacked pulse-width modulation strategy, introduces the balance strategy of transposition margin, and reduces the switching frequency of the sub-module. Literature [4] is a low-complexity balancing algorithm, which is relatively simple to implement, without any conditional execution requirements, and reduces the switching frequency of power devices, but the algorithm has a poorer voltage equalization effect under the recent level approximation modulation strategy. Literature [5] takes the median value of the capacitor voltage of the sorting sub-module as the reference value, and determines the input and removal of the sub-module by comparing the recursive method, but this method obviously increases the fluctuation rate of the capacitor voltage. Literature [6] proposed a method that combines the model predictive control of the MMC-HVDC system with an improved sub-module voltage balance control strategy, which has a good voltage equalization effect, but the control strategy is more complicated. Therefore, choosing an appropriate voltage equalization control strategy plays a great role in reducing the MMC switching frequency, reducing control complexity, and improving operating performance.

This paper analyzes the basic topological structure and working principle of MMC. Taking into account the switching status of the sub-modules at the previous moment, the average value of the sub-modules is used as the benchmark, and the switching frequency is reduced through an optimized sorting algorithm.

2. Basic structure and working principle of MMC

As shown in Figure 1, the MMC system consists of 3 bridge arms, each bridge arm contains an upper bridge arm and a lower bridge arm, and each individual bridge arm has N series-connected sub-modules (SM) and one Inductance (L).

![Figure 1. Diagram of MMC topology structure.](image)

The sub-module is an important part of the MMC system. The sub-module in this article contains a half-bridge structure and a sub-module capacitor. The half-bridge unit is composed of two switches as a complement to each other, as shown in Figure 2:
During normal operation, each sub-module has 4 operating modes, as shown in Figure 3. In figure (a) and figure (b), VT1 is in the on state and VT2 is in the off state. If the current flows into the sub-module, it will charge the capacitor; if the current flows out of the sub-module, it will also pass through the capacitor. Therefore, no matter which direction the current flows from, the terminal voltage of the sub-module is equal to the capacitor voltage; in Figure (c) and Figure (d), VT1 is in the off state and VT2 is in the on state. If the current flows into the sub-module, it will flow through VT2, If the current flows out of the sub-module, it will flow through VD2, regardless of the current flow direction, the terminal voltage of the sub-module is equal to 0.

Define the switch state as shown in formula 1. When the upper switch is opened and the lower switch is closed, the sub-module capacitor is put into the bridge arm to run, and the output voltage is the sub-module capacitor voltage; when the upper switch is closed and the lower switch is opened, the sub-module capacitor in the bypass state, the output voltage is 0. Therefore, to synthesize (N+1) level waveforms according to the state of the switch, 2N sub-modules are required.

$$\begin{cases} 
S_j = 1, \text{when } VT_1 = 1, & VT_2 = 0 \\
S_j = 0, \text{when } VT_1 = 0, & VT_2 = 1
\end{cases}$$ (1)

Then the port voltage of the sub-module can be expressed as:
3. Capacitor voltage balance control strategy
For modular multi-level converters, each sub-module can be equivalent to an ideal DC voltage source, so that the converter can generate various voltage levels appropriately to generate AC voltage on the AC side. However, since the capacitor voltage of the sub-module will fluctuate, the three parallel phase units may have different voltages. This will cause the rms value of the circulating current flowing through the bridge arm and the converter loss to increase. Therefore, the sub-module capacitor voltage balance control is also a necessary condition for the stable operation of MMC. Generally, there are the following requirements for capacitor voltage control: 1) Balance control should be simple and easy to implement, which can be applied to the situation of a large number of sub-modules in the bridge arm. 2) The number of sub-modules that need to be changed in the switching state of the bridge arm each time a control action is triggered as few as possible, and the more the number of sub-modules that need to be changed in the switching state, the more severe the fluctuation of the DC side voltage. 3) Capacitor voltage balance control should be coordinated with trigger control.

4. MMC capacitor voltage optimization sorting algorithm

4.1. Traditional sorting algorithm
The most widely used capacitor voltage balance control in MMC is based on the sequencing method. That is to say, in each switching cycle, the capacitance voltage of each leg of the MMC is classified according to the measured voltage. In each control range, if the bridge arm current is positive (or negative), the sub-module is the lowest (or highest) input. The traditional sorting method is simple, intuitive and easy to implement. However, because this method ignores the switching situation of the sub-modules at the previous moment, when the number of sub-modules is large, the amount of calculation will increase, and it will also cause the frequent turn-on and turn-off of the same IGBT, which improves the device performance. The switching frequency causes a large converter switching loss.

4.2. Optimize sorting algorithm
The traditional sorting algorithm can well control the capacitor voltage of the sub-module within a small fluctuation range, but it ignores the switching situation of the sub-module at the previous moment, which will cause excessive turn-on and turn-off loss. In order to solve the shortcomings of traditional pressure equalization sorting, this paper proposes an optimized sorting algorithm on the basis of literature [7]. In order to reduce the switching frequency of the device, fully consider the switching state of the sub-module at the previous moment; in order to better reduce the fluctuation rate of the sub-module capacitor voltage, the average value of the sub-module capacitor voltage is introduced as a reference value. Define the maximum deviation threshold of the sub-module capacitor voltage from the average value at any time as $U_{\text{max}}$.

$$U_c - U_{\text{ave}} = \Delta U_{\text{dif}}$$

In the formula: $U_c$ is the sub-module capacitor voltage at any time; $U_{\text{ave}}$ is the average value of the sub-module capacitor voltage; $\Delta U_{\text{dif}}$ is the difference between the two.

(1) When $N_{\text{need}} > 0$, a certain number of sub-modules need to be invested. At this time, the direction of the bridge arm current needs to be judged. When the bridge arm current is greater than 0, in order to reduce the additional switching frequency, consider investing in the sub-module that has been removed. The sub-module with the highest/lowest voltage of the $|N_{\text{need}}|$ sub-modules depends on the direction of the bridge arm current.
(2) When $N_{\text{need}}=0$, the number of input sub-modules is appropriate at this time, and unnecessary sub-module input and removal actions are not required. In order to fully ensure a high degree of coincidence of the sub-module capacitor voltage and reduce the sub-module capacitor voltage fluctuation rate, the average value of the sub-module voltage is introduced as the reference value, because the average value is easier to better reflect the fluctuation of the sub-module capacitor voltage. First calculate the average value of the sub-module capacitor voltage and formula (3). Secondly, compare the difference between the instantaneous value and the average value of the capacitor voltage at each moment with the set maximum deviation threshold. When the deviation is within the controllable range, keep the existing trigger pulse unchanged; when the deviation exceeds the set threshold, judge the current flow direction of the bridge arm. When the bridge arm current is positive, replace the sub-modules exceeding the voltage deviation threshold with the same number of sub-modules with $\Delta U_{\text{dif}} < 0$; when the bridge arm current is negative, replace the sub-modules exceeding the voltage deviation threshold with the same number of sub-modules $\Delta U_{\text{dif}} > 0$ sub-module.

(3) When $N_{\text{need}} < 0$, a certain number of sub-modules need to be removed. At this time, the direction of the bridge arm current needs to be judged. When the bridge arm current is greater than 0, in order to reduce the extra switching frequency, consider cutting off in the sub-module that has been put into use. Removal $|N_{\text{need}}|$ the sub-module with the highest/lowest voltage of each sub-module depends on the direction of the bridge arm current.

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**Figure 4.** Optimized sorting and equalization voltage algorithm.
5. Simulation analysis
In order to verify the effectiveness of the proposed voltage equalization control strategy, this paper builds a PSCAD/EMTDC MMC simulation system at both ends. The simulation parameter design of the system is shown in Table 1.

| Items                          | Values   |
|-------------------------------|----------|
| Active power (MW)             | 120      |
| Reactive power (Mvar)         | 0        |
| AC side bus volt (KV)         | 60       |
| Transformer ratio             | 110/60KV |
| Number of bridge arm sub-module | 20     |
| DC side bus volt (KV)         | 120      |
| Sub-module capacitance (mF)   | 2.5      |
| Bridge arm inductance (mH)    | 10       |

The first sub-module of the upper bridge arm of phase A is selected as the research object, and its trigger pulse is shown in Figure 5 and Figure 6. From the figure, we can easily see that after the optimized trigger pulse is adopted, the sub-module switch trigger pulse frequency is significantly reduced, which greatly reduces the switching loss.

![Figure 5](image_url)

**Figure 5.** Switch trigger frequency of traditional sequencing method.

![Figure 6](image_url)

**Figure 6.** Optimized sequence method switch trigger pulse frequency.

Figure 7 adopts the traditional sequencing method, and the total number of switching times between 0.8 and 1.8s reaches 1091; Figure 8 adopts the optimized sequence method, and the total number of switching times is 428 between 0.8 and 1.8s. Obviously, after adopting the optimized
sorting method, the number of switching times is obviously reduced, which well verifies the feasibility of the proposed method.

![Switch times of traditional sorting method.](image)

**Figure 7.** Switch times of traditional sorting method.

![Optimal sorting method switch times.](image)

**Figure 8.** Optimal sorting method switch times.

From Figure 9 and Figure 10, it can be seen that after the optimized sequence voltage equalization control strategy is adopted, compared with the traditional voltage equalization control strategy, the volatility and imbalance of the sub-module capacitor voltage waveform are reduced, but can still be well restrained within the set threshold. After the optimized sequencing control strategy is adopted, the capacitor voltage fluctuates greatly because the optimized sequencing control strategy is adopted under the nearest level approach modulation strategy. In the voltage equalization process, once the number of input sub-modules is determined, the sub-modules in the input state will always be in the long-term input state, the capacitor voltage will fluctuate greatly in the end.

![Traditional sorting method capacitor voltage waveform.](image)

**Figure 9.** Traditional sorting method capacitor voltage waveform.
6. Conclusions
This paper proposes an optimized sequencing voltage equalization control strategy based on the problems of high switching frequency and large operating loss caused by the traditional sequencing voltage equalization algorithm. Under the premise of setting the maximum capacitance voltage deviation threshold, the algorithm considers the switching situation of the sub-module at the previous moment, and tries to keep the original switching state unchanged, which greatly reduces the number of repeated switching of the sub-module. Unnecessary switching losses. The simulation results show that the optimized sequencing voltage equalization control strategy adopted in this paper is basically the same as the traditional sequencing method, the output sub-module capacitor voltage waveform is basically the same, the switching frequency is effectively reduced, the circulating current suppression effect is better, and the MMC operating performance is greatly improved. The method has certain feasibility.

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