A Method of Camera Link Image Data Processing Based on FPGA

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Abstract. Camera Link is based on the development of Channel Link Technology. The data is transmitted using low voltage differential signal (LVDS). It has some advantages, such as fast speed, strong anti-interference ability and so on. Camera Link is widely used in the field of robot vision applications. FPGA integrates rich gate circuit resources and has the advantages of high speed, which makes it suitable for processing parallel data. In this paper, a Camera Link image data processing method based on FPGA is proposed, which is verified by simulation and has been successfully applied to practical projects.

Introduction

Camera Link is a serial communication protocol in the field of machine vision application. It is based on the development of Channel Link technology and uses low voltage differential signal LVDS transmission. There are four kinds of camera signals: power signals, video data signals, camera control signals and serial communication signals. The video data signals are the core of Camera Link, including 1 pairs of differential clock and 4 pairs of serial differential data. The Camera Link conversion chip converts 4 pairs of differential data into parallel data, and parallel data includes 24 bit data, frame synchronization, row synchronization, data synchronization and image pixel clock. There are three modes of video transmission: Base, Medium and Full. The conversion chips, interfaces and data bits for each pixel clock transmission under the three modes are shown in the following table.

| Mode | Frame conversion chips | Mechanical interface | Transmit bit per pixel clock |
|------|------------------------|----------------------|-----------------------------|
| Base | Basic                  | 1                    | 1                           | 28                          |
| Medium | Midile                | 2                    | 2                           | 40                          |
| Full  | Complete              | 3                    | 3                           | 68                          |

FPGA (Field Programmable Gate Array) is a chip that can change the internal routing and logic by programming. It integrates logic block, layout and routing resources, configurable IO port, clock management unit, RAM memory, DSP module and other resources. It is widely used in video image preprocessing because of its fast processing speed and high capability of data processing in parallel.

The data output of Camera Link is in parallel, and FPGA stores the data in the FIFO, the processor reads the data out by detecting the state of FIFO, and then processes, displays, or compares the data.

System Structure

The system consists of peripherals, Camera Link adapter, FPGA and DSP processor. The constitution of the system is shown below.
Chip Selection

We choose the DS90CR286A of National Semiconductor as the Camera Link convert chip. The chip can convert 4 serial LVDS signals to 28 bit parallel TTL data output, and the pixel clock can reach 66MHz.

We choose the XC7A200T-1FBG676I of Xilinx as the FPGA, which has 215k logic unit, 13Mb RAM block and 500 programmable IO ports. It has the advantages of low power consumption and fast speed, and can realize serial and parallel conversion of video signals.

Besides, we use DSP of TI as processor. The capacity of FIFO is small, so the DSP will read the data out when the data in the FIFO reaches a specified number. The DSP will receive a interrupt signal and calculate and display a frame of data according to the number of rows and columns when a frame of data is transmit.

Signal Connections

The signal of the system peripheral to the converter chip is 4 pairs of LVDS data plus 1 LVDS clocks. The rate range of the data line is 140~462Mbps, the clock frequency range is 20~66MHz. In this design, the pixel clock is 30MHz.

The DS90CR286A chip converts serial data to parallel data to FPGA, and the output data includes 24 bit data, FVAL (frame synchronization signal), LVAL (line synchronization signal), DVAL (data effective signal), and CLK_OUT (pixel clock). The correspondence of 4 LVDS serial data converting to parallel data are shown in the following figure.

The data transmission between DSP and FPGA are through EMIF bus, including control bus, address bus and data bus.

FPGA Design

Timing

The output data of Camera Link convert chip is in parallel. The size of each frame is 640 * 480 pixels in this design. FVAL is the frame synchronization signal, LVAL is the row synchronization signal,
and the CLK_OUT is the pixel clock signal. The convert chip outputs data on the falling edge of the clock, and FPGA locks data on the data bus on the rising edge of the clock. It contains 640 clock cycles each row, and 480 rows each frame.

**Figure 3. Timing of the Camera Link convert chip.**

**FPGA Code**

The signals of Camera Link interface module are shown in table 2.

| Name          | I/O | Bit width | Meaning            | others  |
|---------------|-----|-----------|--------------------|---------|
| clk_100m      | I   | 1         | Clock              | 100MHz  |
| reset_n       | I   | 1         | Reset              | Active low |
| FVAL          | I   | 1         | frame synchronzation | Active high |
| LVAL          | I   | 1         | line synchronzation  | Active high |
| CLK_OUT       | I   | 1         | pixel clock        | 30MHz   |
| A             | I   | 8         | parallel data in   |         |
| cl_frame_int  | O   | 1         | frame finish int   |         |
| cl_frame_count| O   | 32        | frame count        |         |
| cl_line_count | O   | 10        | line count         |         |
| cl_fifo_rd_en | I   | 1         | fifo read enable   | Active high |
| cl_fifo_dout  | O   | 64        | fifo data output   |         |
| cl_fifo_empty | O   | 1         | fifo empty         | Active high |
| cl_fifo_full  | O   | 1         | fifo full          | Active high |
| cl_rd_data_count | O   | 10        | fifo read time count |         |
| cl_wr_data_count | O   | 13        | fifo write time count |         |

FVAL, LVAL, CLK_OUT and A[7..0] are the output signals of the conversion chip, and the timing is show in figure 3. Other signals are connected to other modules inside the FPGA.

**Figure 4. The block diagram inside the FPGA.**

The interface program consists of two subroutine modules, the count_int module and the FIFO.
The module generates the interrupt signal, the reset signal and the counting signals. The input signals are clock of 100MHz, reset signal, frame synchronization signal, the row synchronization signal. There are four output signals. The cl_frame_int signal is interrupt signal after the completion of transmission of one frame. It is low in usual state, when the falling edge of FVAL is detected, the cl_frame_int signal goes high for 8 clock as the interrupt for DSP. The DSP reads the data out and processes the data when the DSP receives the interrupt signal. The signal cl_frame_count is count for frame, it increases for one when the falling edge of FVAL is detected. The signal cl_line_count is the count for line, it increases for one when the falling edge of FVAL is detected. The signal cl_fifo_rst is the reset signal of the FIFO, which is active high. The signal goes high for one clock to reset the FIFO in order to clear the old data when the falling edge of FVAL is detected.

The FIFO solves the problem of the clock domain crossing. The data goes into FIFO with the pixel clock first, and then the data is read in the clock domain of 100MHz. The signal rst is the reset signal of the FIFO, which is generated by the module count_int, and it reset the FIFO at the beginning of every frame. The signal wr_en is the result of the AND operation of FVAL and LVAL. The signal wr_clk is the pixel clock. The signal din[7..0] is the output data A[7..0] of the conversion chip. The signal rd_clk is the main clock of FPGA, which is 100MHz. The others signals, including rd_en, dout[63..0], empty, full, rd_data_count[9..0], wr_data_count[9..0], are connected to the other modules in FPGA.

Simulation and Application

Simulation

The simulation of the program is done to verify the function. The waveform of the signals cl_fifo_rst, cl_line_count[9..0], cl_frame_int, cl_frame_count[31..0] are shown in the following figures.

![Figure 5. The waveform of signal cl_fifo_rst.](image)

![Figure 6. The waveform of signal cl_line_count[9..0].](image)

![Figure 7. The waveform of signal cl_frame_int.](image)
Application

The method is used in the project. The infrared camera of 640*480 pixel is used as peripheral, and the cup full of hot water as the observed object. The output signals are divided into two, and one goes to the standard test instrument, and the other goes to the system. The connection diagram of the instruments is shown in figure 9 and the result is shown in figure 10.

Summary

A method of data processing of Camera Link based on FPGA is put forward in this article. The image data is converted from serial to parallel and stored in FIFO of FPGA, the DSP read the data out and process the data. The method has a certain application value in engineering practice.

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