Impact of Process-Induced Variations on Negative Capacitance Junctionless Nanowire FET

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Abstract: In this study, the impact of the negative capacitance (NC) effect on process-induced variations, such as work function variation (WFV), random dopant fluctuation (RDF), and line edge roughness (LER), was investigated and compared to those of the baseline junctionless nanowire FET (JL-NWFET) in both linear ($V_{ds} = 0.05$ V) and saturation ($V_{ds} = 0.5$ V) modes. Sentaurus TCAD and MATLAB were used for the simulation of the baseline JL-NWFET and negative capacitance JL-NWFET (NC-JL-NWFET). Owing to the NC effect, the NC-JL-NWFET showed less variation in terms of device performance, such as $\sigma[V_{th}], \sigma[SS], \sigma[I_{on}/I_{off}], \sigma[V_{th}]/\mu[V_{th}], \sigma[SS]/\mu[SS]$, and $\sigma[I_{on}/I_{off}]/\mu[I_{on}/I_{off}]$, and enhanced device performance, which implies that the NC effect can successfully control the variation-induced degradation.

Keywords: random variation; line edge roughness (LER); random dopant fluctuation (RDF); work function variation (WFV); negative capacitance (NC)

1. Introduction

In the past a few decades, the downsizing of metal oxide semiconductor field effect transistors (MOSFETs) has not only increased the number of transistors in integrated circuits (ICs), but also improved their performance such as high-frequency performance [1]. To address these scaling-down issues of MOSFETs, MOSFET structures were evolved over the years, and different types of Multi-Gate FETS (MuGFETs) have been proposed [2]. However, the downsizing of transistors has caused an ever-increasing power density in ICs. In addition, process-induced random variation (RV) reduced yield efficiency. Therefore, the effective control on the RV has become a major issue when designing and integrating transistors in ICs. Based on previous studies, it is known that there are three root-causes in process-induced RV, namely, line edge roughness (LER) [3], random dopant fluctuation (RDF) [4], and work function variation (WFV) [5].

As a promising device solution, negative capacitance FETs (NCFETs) have been proposed as one of the next-generation low-power devices. Compared to the baseline FET, the ferroelectric-gated NCFET shows an enhanced output drain current at the same supply voltage, because of the amplified internal voltage (which primarily originates from the polarization switching in ferroelectric material) [6–8]. In addition, using NC, i.e., using ferroelectric layer in a gate stack, allows for the subthreshold slope of FET to be reduced to lower than the theoretical limit of 60 mV/decade [4]. Various dopants that are doped in hafnium-based ferroelectric materials, such as Al (HAO), Zr (HZO), and Si (HSO), are studied for NCFETs. Particularly, HAO shows stable ferroelectricity in a wide range of thermal processes (e.g., 500–1000 °C) [9].

Moreover, the junctionless (JL) doping profile, which is a constant doping profile along the source-channel-drain direction in MOSFET, is a promising fabrication scheme, in terms of scaling issues because of its various advantages. In recent years, the channel length has been scaled down less than 20 nm, requiring very high doping concentrations. However, by the statistical characteristics of the distribution of dopants and the law of
diffusion, this has become a very difficult challenge for the semiconductor manufacturing process. The JL doping profile is not only less sensitive to the thermal budget, but it can also simplify the ion implantation process, compared to conventional MOSFETs with different doping profiles. In addition, JL-nanowire FETs (JW-NWFETs) is known to have extremely low leakage current and close-to-ideal subthreshold slope, and the degradation of mobility is less than that of nanowire with junction [10].

In this study, the impact of negative capacitance on junctionless nanowire FETs (NC-JL-NWFETs) has been studied with various process-induced variations, such as work function variation (WFV), random dopant fluctuation (RDF), and line edge roughness (LER). The impact of each variation type on baseline JL-NWFETs and NC-JL-NWFETs are compared and discussed. The impact from all the variation sources (i.e., integrated types (WFV, RDF, and LER combined)) are also investigated. The MATLAB and Sentaurus TCAD tools were used together for the simulation in this study. This combined simulation method/approach (vs. TCAD-only simulation method) significantly saved on the simulation running time.

2. Simulation of the NC-JL-NWFET and Process-Induced Variations

Figure 1a,b show the bird’s-eye view and equivalent capacitive model of the metal-ferroelectric-insulator-silicon (MFIS)-structured NC-JL-NWFET used in this study. The device was designed according to the International Roadmap for Devices and Systems (IRDS) [11]. Table 1 lists the device parameters.

![Figure 1. (a) Bird’s-eye view and (b) equivalent capacitive model of MFIS-structured NF-JL-NWFETs. (c) Experimentally measured polarization versus coercive field of 10 nm-thick Al:HfO2 (HAO) capacitor.](image)

For the simulation of ferroelectric behavior in the NC-JL-NWFET, the Landau–Khalatnikov (LK) model is adopted to determine the voltage drop across the ferroelectric layer. The ferroelectric parameters for LK model are extracted from experimentally fabricated HAO-based MFM (Metal–Ferroelectric–Metal) capacitor. The LK parameters are determined as follows from Polarization–Electric field curve, shown in Figure 1c:

\[
\alpha = -\frac{3\sqrt{3}E_c}{4P_r}, \quad \beta = \frac{3\sqrt{3}E_c}{8P_r^3}, \quad \gamma = 0
\]  

(1)

The LK parameters are calculated from the remnant polarization \(P_r\) and coercive field \(E_c\) of the Aluminum-doped Hafnium (HAO)-based ferroelectric, where \(\alpha = -1.226 \times 10^{11} \text{ cm/F}\) and \(\beta = 2.394 \times 10^{20} \text{ cm}^2/\text{C}^2\) are defined for \(P_r = 16 \mu\text{C/cm}^2\) and \(E_c = 1.51 \text{ MV/cm}\). In this study, \(\gamma\) is assumed to be zero because the last term in Equation (1) is negligible [12].

The voltage drop \(V_{fe}\) in terms of the charge density \(Q_g\) is calculated as follows:

\[
V_{fe} = 2\alpha T_{fe} Q_g + 4\beta T_{fe} Q_g^3 + 6\gamma T_{fe} Q_g^5
\]  

(2)

where \(T_{fe}\) is 4 nm, and \(Q_g\) is extracted from TCAD simulation of the baseline JL-NWFET. Following the derivation of \(V_{fe}\), the internal voltage \(V_{int}\) is derived from MATLAB as follows:
The TCAD values of $V_g$ and MATLAB-extracted values of $V_{int}$ are simulated, and the drain current ($I_d$) of the NC-JL-NWFET is derived from TCAD. This simulation process is described in the flow chart shown in Figure 2.

![Figure 2. Simulation flow chart of NC-JL-NWFET using Sentaurus TCAD and MATLAB tools.](image)

### Table 1. Device Design Parameters for NC-JL-NWFET.

| Parameters                              | Value         |
|-----------------------------------------|---------------|
| Doping concentration (N) in channel/source/drain | $10^{19}$/cm$^3$ |
| Channel length                          | 20 nm         |
| Channel radius                          | 5 nm          |
| Ferroelectric thickness ($T_{fe}$)       | 4 nm          |
| Ferroelectric (Al: HfO$_2$) remnant polarization ($P_r$) | 16 µC/cm$^2$ |
| Ferroelectric (Al: HfO$_2$) coercive voltage ($E_c$) | 1.51 MV/cm |
| Equivalent oxide thickness ($T_{ox}$)    | 1 nm          |

The process-induced variations, i.e., WFV, RDF, and LER, were simulated using the TCAD tool. The variation parameters were set in the TCAD simulation and implemented for the baseline JL-NWFET simulation. To analyze the fluctuation induced by WFV and RDF, a simulation was conducted with a function embedded in TCAD [13]. TiN was used as the metal gate and the grain orientation was considered as the corresponding probability (i.e., orientation <100>: workfunction = 4.6 eV as probability = 60%, orientation <111>: workfunction = 4.4 eV as probability = 40%). The average metal grain size was 4 nm. To investigate the LER-induced variation, the roughness patterns on the channel were generated based on the quasi-atomistic model with the 2D autocorrelation function (ACF) method using TCAD (Sentaurus) and MATLAB [14]. The RMS amplitude $\sigma = 0.5$ nm, $X$-axis correlation length $\xi_x = 20$ nm, $Y$-axis correlation length $\xi_y = 50$ nm, and roughness exponent $\alpha = 1$ [15] were the design parameters used in this study. The extent of fluctuations induced by WFV, RDF, and LER were investigated in terms of the variation parameters. The RDF values implemented and integrated were controlled by applying the NC.

### 3. Results and Discussion

#### 3.1. Work Function Variation (WFV)

The overall performance of the device with WFV is improved when the NC was applied. Figure 3 shows the $I_d-V_{gs}$ curves for the n-/p-type JL-NWFET and NC-JL-NWFET in both linear and saturation modes. Table 2 summarizes the device performance of the JL-NWFET implemented with WFV and with/without NC in the two modes (linear and saturation).
Figure 3. Simulated $I_{DS}$-$V_{GS}$ curves (a) for n-type JL-NWFET (JL) and (b) for n-type NC-JL-NWFET (NC-JL) with WFV. $I_{DS}$-$V_{GS}$ curves (c) for p-type JL-NWFET (JL) and for (d) p-type NC-JL-NWFET (NC-JL) with WFV. The dotted line indicates the nominal $I_{DS}$-$V_{GS}$ for JL-NWFET and NC-JL-NWFET.

Table 2. Variation parameters of n-/p-type JL-NWFET and NC-JL-NWFET in linear and saturation mode with work function variation.

| Mode       | N-baseline | N-NC        |
|------------|------------|-------------|
| Linear     |            |             |
|            | $V_t$      | $I_{on}/I_{off}$ | $SS_{avg}$ | $V_t$ | $I_{on}/I_{off}$ | $SS_{avg}$ |
| Std        | 0.017154   | 0.268854    | 0.223317  | 0.01672 | 0.269738 | 0.290196 |
| Mean       | 0.043405   | 8.005784    | 63.68198 | 0.09334 | 9.054849 | 61.24335 |
| Std/Mean   | 0.395215   | 0.033582    | 0.003507 | 0.01972 | 0.029789 | 0.004738 |
| Saturation |            |             |
|            | $V_t$      | $I_{on}/I_{off}$ | $SS_{avg}$ | $V_t$ | $I_{on}/I_{off}$ | $SS_{avg}$ |
| Std        | 0.01688    | 0.222199    | 0.181642  | 0.016566 | 0.198823 | 0.218464 |
| Mean       | -0.27324   | 11.03523    | 63.8211  | -0.31917 | 12.01489 | 61.5753 |
| Std/Mean   | -0.06178   | 0.020135    | 0.00285  | -0.0519 | 0.016548 | 0.00355 |

First, in the linear mode, the mean of the log scaled-on/off ratio for the n-type is increased from 8.01 without NC to 9.05 with NC. The p-type also experienced an increase from 11.03 without NC to 12.01 with NC. The mean of SS is decreased from 63.68 without NC to 61.58 with NC for the n-type and p-type, respectively. The increase in the on/off ratio and decrease in SS indicates that the device performance of the JL-NWFET is improved by the NC effect. Although the device performance is improved, not all variations were improved. $V_t$ and the on/off ratio show the decreased CV (that is, $V_t$: from 0.395 to 0.179 (n-type), from 0.062 to 0.052 (p-type); on/off ratio: from 0.0335 to 0.0298 (n-type), from 0.0201 to 0.0165 (p-type)). However, the mean of SS is reduced, but the standard deviation (Std) of SS is increased, indicating that the coefficient of variation is increased.

The overall performance was improved when NC was applied in the saturation mode (that is, the mean of on/off: from 8.413 to 9.510 (n-type), from 11.234 to 12.176 (p-type); the mean of SS: from 62.983 to 61.026 (n-type), from 63.184 to 61.360 (p-type), and the variation caused by WFV was reduced (that is, the CV of $V_t$: from 0.586 to 0.195 (n-type), from 0.067 to 0.053 (p-type); the CV of the on/off ratio: from 0.0305 to 0.0265 (n-type), from 0.018 to 0.015 (p-type)).
3.2. Random Dopant Fluctuation (RDF)

Figure 4 shows the n-/p-type $I_{DS} - V_{GS}$ of the JL-NWFET and NC-JL-NWFET in both linear and saturation modes; Table 3 shows the device performance of the RDF-implanted JL-NWFET with/without NC in the linear/saturation mode. The mean on/off ratio (log scale) is increased from 7.814 without NC to 8.852 with NC and from 10.86 without NC to 11.828 with NC for n-type and p-type, respectively. The mean of SS is decreased from 61.042 without NC to 61.668 with NC (n-type) and from 63.99 without NC to 61.84 with NC (p-type) in the linear mode. In the saturation mode, the mean on/off ratio and SS is increased when NC was applied. This change indicates that the performance of the NC-JL-NWFET was enhanced compared to that of the baseline JL-NWFET.

![Figure 4](image-url)

**Figure 4.** Simulated $I_{DS}-V_{GS}$ curves (a) for n-type JL-NWFET (JL) and (b) for n-type NC-JL-NWFET (NC-JL) with RDF. $I_{DS}V_{GS}$ curves (c) for p-type JL-NWFET (JL) and for (d) p-type NC-JL-NWFET (NC-JL) with RDF. The dotted line indicates the nominal $I_{DS}V_{GS}$ for JL-NWFET and NC-JL-NWFET.

|            | Linear   | N-baseline | N-NC          | N-NC          | N-NC          |
|------------|----------|------------|---------------|---------------|---------------|
|            |          | $V_t$      | $I_{on}/I_{off}$ | SS$_{avg}$    | $V_t$         | $I_{on}/I_{off}$ | SS$_{avg}$ |
| Std        |          | 0.044637   | 0.725784      | 0.612073      | 0.035404      | 0.595695      | 0.461292   |
| Mean       |          | 0.033385   | 7.814381      | 64.04266      | 0.084205      | 8.852136      | 61.66757   |
| Std/Mean   |          | 1.337033   | 0.092878      | 0.009557      | 0.420455      | 0.067294      | 0.00748    |
| Linear     |          | $V_t$      | $I_{on}/I_{off}$ | SS$_{avg}$    | $V_t$         | $I_{on}/I_{off}$ | SS$_{avg}$ |
| Std        |          | 0.044614   | 0.652677      | 0.466485      | 0.035189      | 0.498014      | 0.342692   |
| Mean       |          | −0.26427   | 10.86005      | 63.9898       | −0.3111       | 11.82838      | 61.838     |
| Std/Mean   |          | −0.16882   | 0.060099      | 0.00729       | −0.11311      | 0.042103      | 0.00554    |
| Saturation |          | $V_t$      | $I_{on}/I_{off}$ | SS$_{avg}$    | $V_t$         | $I_{on}/I_{off}$ | SS$_{avg}$ |
| Std        |          | 0.04631    | 0.718698      | 0.60987       | 0.037003      | 0.588964      | 0.557013   |
| Mean       |          | 0.017349   | 8.180337      | 63.22915      | 0.07581       | 9.277599      | 61.22045   |
| Std/Mean   |          | 2.669281   | 0.087857      | 0.009645      | 0.488101      | 0.063482      | 0.009098   |

In terms of variation, NC effectively controlled the fluctuation induced by the RDF in the JL-NWFET. The coefficient of $V_t$ variation, on/off ratio, and SS is decreased with NC. In the case of n-type device, the coefficient of $V_t$ variation, on/off ratio, and SS is decreased by approximately 69%, 28%, and 22% in linear mode and 81%, 28%, and 7% in saturation mode, respectively. For the p-type device, the coefficients of variation in the three profiles are decreased by 33%, 30%, and 24% in linear mode and by 35%, 32%, and 20% in saturation mode, respectively.
3.3. Line Edge Roughness (LER)

Figure 5 shows the n-/p-type $I_{ds}-V_{gs}$ of the JL-NWFET and NC-JL-NWFET in both the linear and saturation modes. Notably, the average values of both $V_{th}$ and $V_{on}$ are increased for the NC-JL-NWFET (see Table 4). This is because the capacitance-boost effect of NC is the strongest when the applied electric field is near 0 [16], which acts in a way that suppresses the leakage current in the subthreshold region. The on-state current is also improved (increased) but not as much as the leakage current improvement (decreased). In other words, the on/off ratio is improved. For the linear mode operation, values 8.032 to 9.131, and from 11.108 to 12.107, were yielded for n-type and p-type, respectively; for the saturation mode, these values were from 8.456 to 9.608 and from 11.298 to 12.265 for n-type and p-type, respectively. SS is also improved from 63.553 to 61.046 and from 63.627 to 61.377 for n-type and p-type, respectively.

![Figure 5.](image)

**Figure 5.** Simulated $I_{DS}-V_{GS}$ curves (a) for n-type JL-NWFET (JL) and (b) for n-type NC-JL-NWFET (NC-JL) with LER. $I_{DS}-V_{GS}$ curves (c) for p-type JL-NWFET (JL) and for (d) p-type NC-JL-NWFET (NC-JL) with LER. The dotted line indicates the nominal $I_{DS-}V_{GS}$ for JL-NWFET and NC-JL-NWFET.

| Linear | N-baseline | N-NC | N-NC | N-NC |
|--------|------------|------|------|------|
| Vt     | $I_{on}/I_{off}$ | $SS_{avg}$ | $V_{t}$ | $I_{on}/I_{off}$ | $SS_{avg}$ |
| Std    | 0.024123   | 0.416495 | 0.475774 | 0.019775 | 0.37503 | 0.375156 |
| Mean   | 0.043285   | 8.032002 | 63.55298 | 0.096085 | 9.130583 | 61.4604 |
| Std/Mean | 0.552699 | 0.051854 | 0.007486 | 0.205812 | 0.038881 | 0.006145 |

| Linear | P-baseline | P-NC | P-NC | P-NC |
|--------|------------|------|------|------|
| Vt     | $I_{on}/I_{off}$ | $SS_{avg}$ | $V_{t}$ | $I_{on}/I_{off}$ | $SS_{avg}$ |
| Std    | 0.02632    | 0.40593 | 0.506412 | 0.021023 | 0.321489 | 0.46072 |
| Mean   | −0.276944  | 11.10786 | 63.627 | −0.324944 | 12.10733 | 61.3765 |
| Std/Mean | −0.09504 | 0.036545 | 0.00796 | −0.0647 | 0.026553 | 0.00751 |

| Saturation | N-baseline | N-NC | N-NC | N-NC |
|------------|------------|------|------|------|
| Vt         | $I_{on}/I_{off}$ | $SS_{avg}$ | $V_{t}$ | $I_{on}/I_{off}$ | $SS_{avg}$ |
| Std        | 0.039171   | 0.563022 | 0.62611 | 0.027999 | 0.479479 | 0.537083 |
| Mean       | 0.030968   | 8.456462 | 62.86968 | 0.091937 | 9.607924 | 60.80284 |
| Std/Mean   | 1.030429   | 0.066579 | 0.009959 | 0.302373 | 0.049905 | 0.008833 |

| Saturation | P-baseline | P-NC | P-NC | P-NC |
|------------|------------|------|------|------|
| Vt         | $I_{on}/I_{off}$ | $SS_{avg}$ | $V_{t}$ | $I_{on}/I_{off}$ | $SS_{avg}$ |
| Std        | 0.030426   | 0.427816 | 0.531366 | 0.024346 | 0.32841 | 0.490825 |
| Mean       | −0.26217   | 11.29754 | 63.023 | −0.31865 | 12.26493 | 61.1525 |
| Std/Mean   | −0.11605   | 0.037868 | 0.00843 | −0.0764 | 0.026776 | 0.00803 |

With respect to variation, it can be denoted that NC can successfully suppress the impact of LER-induced variation in nanowire FETs. For $V_{th}$, $\sigma/\mu$ (coefficient of variation (CV)) is decreased dramatically from 1.0304 to 0.3023 and from 0.1161 to 0.0764 for n-type and p-type nanowire FETs, respectively. A similar tendency was observed for $V_{on}$. The value of $\sigma/\mu$ is decreased from 0.5573 to 0.2058 and from 0.095 to 0.064, respectively. The improvement was more pronounced in n-type FETs than in p-type FETs. Regarding other parameters, such as the on/off ratio and SS, their improvements are summarized in Table 4.
3.4. Integrated Process Induced Variation

We were able to confirm that the mean threshold voltage in two modes (i.e., \( V_{\text{tlin}} \) and \( V_{\text{tsat}} \)) would increase when NC was applied, which we identified in the previous process. The on/off ratio and SS are also exhibiting the improved performance when NC was applied.

Figure 6 shows the n-/p-type \( I_{\text{ds}}-V_{\text{gs}} \) curves of the JL-NWFET and NC-JL-NWFET in both the linear and saturation modes. Table 5 shows the three performance profiles of the JL-NWFET when NC was applied and not applied in both the linear and saturation modes. The NC-applied JL-NWFET shows a more successfully controlled process-induced random variation than the baseline JL-NWFET without NC. In particular, for \( V_{t} \) in n-type, the coefficient of variation (CV) is decreased by 65% (from 1.321 to 0.452) in the linear mode, and 80% (from 2.780 to 0.563) in the saturation mode. Also, Figures 7 and 8 show how much improved the RDF-induced variation was controlled by NC, compared to the other process-induced LER/WFV. In addition, although the variation in SS was induced only by WFV, it was not properly controlled, and the variation in the on/off ratio and SS, induced by process-induced random variation, was successfully controlled by NC.

![Figure 6. Simulated \( I_{\text{ds}}-V_{\text{gs}} \) curves for n-type JL-NWFET (JL) and for (b) n-type NC-JL-NWFET (NC-JL) with three random variations (WFV, RDF, and LER).](image)

Table 5. Variation parameters of n-/p-type JL-NWFET and NC-JL-NWFET in linear and saturation mode with combined random variations.

| Linear | N-baseline | N-NC |
|--------|------------|------|
| Std    | \( V_{t} \) | \( I_{\text{on}}/I_{\text{off}} \) | \( SS_{\text{avg}} \) | \( V_{t} \) | \( I_{\text{on}}/I_{\text{off}} \) | \( SS_{\text{avg}} \) |
| Mean   | \( V_{t} \) | \( I_{\text{on}}/I_{\text{off}} \) | \( SS_{\text{avg}} \) | \( V_{t} \) | \( I_{\text{on}}/I_{\text{off}} \) | \( SS_{\text{avg}} \) |

| Linear | P-baseline | P-NC |
|--------|------------|------|
| Std    | \( V_{t} \) | \( I_{\text{on}}/I_{\text{off}} \) | \( SS_{\text{avg}} \) | \( V_{t} \) | \( I_{\text{on}}/I_{\text{off}} \) | \( SS_{\text{avg}} \) |
| Mean   | \( V_{t} \) | \( I_{\text{on}}/I_{\text{off}} \) | \( SS_{\text{avg}} \) | \( V_{t} \) | \( I_{\text{on}}/I_{\text{off}} \) | \( SS_{\text{avg}} \) |

| Saturation | N-baseline | N-NC |
|------------|------------|------|
| Std        | \( V_{t} \) | \( I_{\text{on}}/I_{\text{off}} \) | \( SS_{\text{avg}} \) | \( V_{t} \) | \( I_{\text{on}}/I_{\text{off}} \) | \( SS_{\text{avg}} \) |
| Mean       | \( V_{t} \) | \( I_{\text{on}}/I_{\text{off}} \) | \( SS_{\text{avg}} \) | \( V_{t} \) | \( I_{\text{on}}/I_{\text{off}} \) | \( SS_{\text{avg}} \) |

| Saturation | P-baseline | P-NC |
|------------|------------|------|
| Std        | \( V_{t} \) | \( I_{\text{on}}/I_{\text{off}} \) | \( SS_{\text{avg}} \) | \( V_{t} \) | \( I_{\text{on}}/I_{\text{off}} \) | \( SS_{\text{avg}} \) |
| Mean       | \( V_{t} \) | \( I_{\text{on}}/I_{\text{off}} \) | \( SS_{\text{avg}} \) | \( V_{t} \) | \( I_{\text{on}}/I_{\text{off}} \) | \( SS_{\text{avg}} \) |
When the negative capacitance effect was applied, it was possible to reduce the process-induced variation in both the linear and saturation modes, as shown in Table 6. Overall, the process-induced variation showed, on average, the improvements of 25.17% and 27.46% in the linear and saturation modes, respectively. The better resistance to variation is due to the larger gate capacitance of the NC-JL-NWFET, which allows the device to be more tolerant to variation, resulting in a decreased variation in the surface potential of the device. This makes the NC-JL-NWFET exhibit improved performance with respect to process-induced random variations, compared to the baseline of JL-NWFET.

Table 6. Percentage of difference in value of $\sigma/\mu$ for NC-JL-NWFET compared to the JL-NWFET in linear and saturation modes.

| Mode   | $V_t$  | $I_{on}/I_{off}$ | $SS_{avg}$ | $I_{on}/I_{off}$ | $SS_{avg}$ |
|--------|--------|------------------|------------|------------------|------------|
| Linear | LER    | 63.070%          | 25.020%    | 17.910%          | 31.922%    |
|        | RDF    | 68.552%          | 27.546%    | 21.732%          | 32.999%    |
|        | WVF    | 54.676%          | 11.295%    | −35.123%         | 15.985%    |
|        | RV     | 65.819%          | 25.809%    | 17.722%          | 31.753%    |
| Saturation | LER   | 70.656%          | 25.045%    | 11.303%          | 34.164%    |
|        | RDF    | 81.714%          | 27.743%    | 5.670%           | 34.889%    |
|        | WVF    | 66.676%          | 13.004%    | −17.497%         | 20.461%    |
|        | RV     | 79.740%          | 25.897%    | 4.923%           | 33.857%    |

Figure 7. (a) On/off ratio variation $[\sigma(I_{on}/I_{off})]$ and $[\sigma(I_{on}/I_{off})/\mu(I_{on}/I_{off})]$ comparison, (b) SS variation $[\sigma(SS)]$ and $[\sigma(SS)/\mu(SS)]$ comparison and (c) $V_t$ variation $[\sigma(V_t)]$ and $[\sigma(V_t)/\mu(V_t)]$ comparison between n-type JL-NWFET and n-type NC-JL-NWFET in linear mode. (d) On/off ratio variation $[\sigma(I_{on}/I_{off})]$ and $[\sigma(I_{on}/I_{off})/\mu(I_{on}/I_{off})]$ comparison, (e) SS variation $[\sigma(SS)]$ and $[\sigma(SS)/\mu(SS)]$ comparison and (f) $V_t$ variation $[\sigma(V_t)]$ and $[\sigma(V_t)/\mu(V_t)]$ comparison between p-type JL-NWFET and p-type NC-JL-NWFET in linear mode.
In this study, we investigated the impact of process-induced variations on the JL-NWFET and NC-JL-NWFET for each n-/p-type and lin/sat mode. The results show that the voltage amplification of the NC effect enhanced the overall device performance (i.e., SS, on/off ratio, and $V_T$) in both the linear and saturation modes. In addition, the decreased coefficient values imply that the ferroelectric layer-made devices are more resistant to process-induced variations. This improvement in device performance is described in terms of variation parameters, such as the mean, standard deviation, and mean/deviation.

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References

1. Crupi, G.; Schreurs, D.M.M.-P.; Caddemi, A. Effects of Gate-Length Scaling on Microwave MOSFET Performance. *Electronics* 2017, *6*, 62. [CrossRef]
2. Groeseneken, G.; Crupi, F.; Shickova, A.; Thijs, S.; Linten, D.; Kaczer, B.; Collaert, N.; Jurczak, M. Reliability issues in MuGFET nanodevices. In Proceedings of the 2008 IEEE International Reliability Physics Symposium, Phoenix, AZ, USA, 27 April–1 May 2008; pp. 52–60.
3. Asenov, A.; Kaya, S.; Brown, A.R. Intrinsic parameter fluctuations in decananometer MOSFETs introduced by gate line edge roughness. *IEEE Trans. Electron Devices* 2003, *50*, 1254–1260. [CrossRef]
4. Asenov, A. Random dopant induced threshold voltage lowering and fluctuations in sub-0.1/spl mu/m MOSFET’s: A 3-D “atomistic” simulation study. *IEEE Trans. Electron Devices* 1998, *45*, 2505–2513. [CrossRef]
5. Brown, A. R.; Roy, G.; Asenov, A. Poly-Si-gate-related variability in decananometer MOSFETs with conventional architecture. *IEEE Trans. Electron Devices* 2007, *54*, 3056–3063. [CrossRef]
6. Kwon, D.; Cheema, S.; Lin, Y.-K.; Liao, Y.-H.; Chatterjee, K.; Tan, A.J.; Hu, C.; Salahuddin, S. Near Threshold Capacitance Matching in a Negative Capacitance FET With 1 nm Effective Oxide Thickness Gate Stack. *IEEE Electron Device Lett.* 2019, *41*, 179–182. [CrossRef]
7. Khan, A.I.; Chatterjee, K.; Wang, B.; Drapcho, S.; You, L.; Serrao, C.; Bakaul, S.R.; Ramesh, R.; Salahuddin, S. Negative capacitance in a ferroelectric capacitor. *Nat. Mater.* 2015, *14*, 182–186. [CrossRef] [PubMed]
8. Salahuddin, S.; Datta, S. Use of negative capacitance to provide voltage amplification for low power nanoscale devices. *Nano Lett.* 2008, *8*, 405–410. [CrossRef] [PubMed]
9. Zhou, J.; Zhou, Z.; Wang, X.; Wang, H.; Sun, C.; Han, K.; Kang, Y.; Gong, X. Temperature Dependence of Ferroelectricity in Al-Doped HfO$_2$ Featuring a High P r of 23.7 µC/cm$^2$. *IEEE Trans. Electron Devices* 2020, *67*, 5633–5638. [CrossRef]
10. Colinge, J.-P.; Lee, C.-W.; Afzalian, A.; Akhavan, N.D.; Yan, R.; Ferain, I.; Razavi, P.; O’neill, B.; Blake, A.; White, M.; et al. Nanowire transistors without junctions. *Nat. Nanotechnol.* 2010, *5*, 225–229. [CrossRef] [PubMed]
11. Moore, M. *International Roadmap for Devices and Systems*; Institute of Electrical and Electronics Engineers: Piscataway, NJ, USA, 2017.
12. Hoffmann, M.; Max, B.; Mittmann, T.; Schroeder, U.; Slesazeck, S.; Mikolajick, T. Demonstration of High-Speed Hysteresis-Free Negative Capacitance in Ferroelectric Hf$_{0.5}$Zr$_{0.5}$O$_2$. In Proceedings of the 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 1–5 December 2018. [CrossRef]
13. Synopsys, T. *Sentaurus Device User Guide*; Version P-2019.03; Synopsys Inc.: Mountain View, CA, USA, 2019.
14. Oh, S.; Shin, C. 3-D quasi-atomistic model for line edge roughness in nonplanar MOSFETs. *IEEE Trans. Electron Devices* 2016, *63*, 4617–4623. [CrossRef]
15. Min, J.; Shin, C. Study of line edge roughness on various types of gate-all-around field effect transistor. *Semicond. Sci. Technol.* 2019, *35*, 015004. [CrossRef]
16. Park, H.W.; Roh, J.; Lee, Y.B.; Hwang, C.S. Modeling of negative capacitance in ferroelectric thin films. *Adv. Mater.* 2019, *31*, 1805266. [CrossRef] [PubMed]