Communication—The Role of the Metal-Semiconductor Junction in Pt-Assisted Photochemical Etching of Silicon Carbide

Markus Leitgeb, Andreas Backes, Christopher Zellner, Michael Schneider, and Ulrich Schmid

Institute of Sensor and Actuator Systems, TU Wien, 1040 Vienna, Austria

Porous 4H-SiC layers were fabricated by photochemical etching of n-type 4H-SiC samples with varying resistivity. An etching solution of Na2S2O8 and HF was used while Pt deposited at the 4H-SiC surface served as catalyst for the reduction of Na2S2O8.

The contact resistance at the Pt/4H-SiC junction was decreased by annealing and surface near phosphorous doping. This enabled the porosification of 4H-SiC with photochemical etching.

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Results and Discussion

The first samples obtained from pure MAPCE experiments showed non-uniform etching characteristics. The samples having lower resistivity showed etching depths ranging from 0.5 μm to just surface roughening at the same sample. The samples having higher resistivity showed mostly surface roughening, locally parts with etching depths up to 1.3 μm could be observed, featuring a sharp border to the not porous regions. Both samples were etched in the regions not covered with Pt unlike metal assisted etching of Si where etching is mainly enhanced underneath a noble metal catalyst deposited at the surface. For etching to occur, oxidation and reduction reactions are necessary. This means that electrons need to flow from the anode (i.e. 4H-SiC) to the cathode (i.e. Pt). Because the electrical current has to pass the Pt/4H-SiC interface, a low contact resistance should increase the etching rate and the uniformity of the porous layers. Annealing metal layers deposited on silicon carbide is a standard approach to form low ohmic contacts.

The MAPCE experiment was carried out again with the difference that after Pt deposition the samples were annealed for 5 minutes in Argon atmosphere at 1100 °C with a prior temperature ramp starting at 800 °C that lasted for 30 minutes. After 2 hours of MAPCE a porous layer with a more uniform depth of (1.11 ± 0.14) μm was observed at the samples with a resistivity of ρ = 0.02 Ω · cm. A cross-sectional view of the obtained porous structure is shown in Figure 1, demonstrating that a porous layer has formed. Figure 2a shows the current voltage characteristics of a sample having a resistivity of ρ = 0.02 Ω · cm before and after annealing. It demonstrates that the contact resistance at the Pt/4H-SiC junction had decreased due to the annealing. This has enhanced the formation of a porous layer during the MAPCE process.

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E-mail: markus.leitgeb@tuwien.ac.at
The same experiments were not successful using the samples with higher resistivity of $\rho = 0.106 \ \Omega \cdot \text{cm}$. This means that just surface roughening or occasional formation of a thin porous layer was observed. At higher resistivity and thus lower dopant concentration the contact resistance is increased at the metal-semiconductor junction. This explains why for the samples with higher resistivity no reproducible porous layer formation was observed even when the samples were annealed. To decrease the contact resistance further a sample with $\rho = 0.106 \ \Omega \cdot \text{cm}$ was doped with phosphorous near the surface according to a method developed by Mendis et al.\textsuperscript{12} Therefore, 0.1 mL of a solution consisting of 50 mL absolute ethanol and 20 mL phosphoric acid (85%) were placed on the sample surface. Next, the sample was annealed in air at 650°C for 30 minutes and in a second step in air at 1100°C for 2 hours. Finally, the sample was cleaned in buffered oxide etch to remove oxidation products, Pt was sputter deposited and annealed like in the previous experiments. These samples showed the formation of a porous layer with uniform depth of (0.78 ± 0.07) μm homogeneously across the sample after 2 hours of MAPCE. A cross-sectional micrograph of the obtained porous layer is shown in Figure 3. Due to the increased dopant concentration near the surface the resistance at the Pt/4H-SiC contact decreased substantially, thus initiating the MAPCE process. This is verified by current voltage measurements of differently processed samples (see Figure 2b), demonstrating the expected impact of annealing and additional doping on contact resistance.

The observed etching depth for the surface near doped sample with $\rho = 0.106 \ \Omega \cdot \text{cm}$ is large compared to the reported diffusion depth of phosphorous atoms in SiC (about 0.1 μm) during annealing.\textsuperscript{13} This means that also not additionally doped 4H-SiC was etched. These observations show that there are three interfaces of interest in Pt assisted photochemical etching of 4H-SiC which determine the performance of the etching process. One is the Pt/4H-SiC junction for which a low contact resistance is needed. Next, at the Pt/etching solution interface persulfate is reduced. Lastly, at the 4H-SiC/etching solution interface holes in the valence band of 4H-SiC are generated by UV light which are needed to increase the etching rate.

Summary

In this letter the metal assisted photochemical etching (MAPCE) of n-type 4H-SiC in a solution of HF/Na$_2$S$_2$O$_8$ with Pt as catalytic metal was investigated. It was shown that the Pt/4H-SiC interface plays a crucial role in this process. Decreasing the contact resistance at the Pt/4H-SiC junction by annealing the samples was sufficient to allow photochemical etching of specimens with low resistivity, while additional surface near doping with phosphorous was necessary for samples having high resistivity to initiate the porosification process. Furthermore, UV light illumination is necessary to generate electron-hole pairs in the space charge layer of the etching solution/4H-SiC interface.

There is hardly any literature available regarding MAPCE of 4H-SiC. The presented findings allow the further investigation of 4H-SiC MAPCE with respect to experimental parameters such as the type of the catalytic metal, the spectral distribution properties of the light source or the composition of the etching solution.

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