Proposal For Neuromorphic Hardware Using Spin Devices

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Abstract: We present a design-scheme for ultra-low power neuromorphic hardware using emerging spin-devices. We propose device models for ‘neuron’, based on lateral spin valves and domain wall magnets that can operate at ultra-low terminal voltage of ~20 mV, resulting in small computation energy. Magnetic tunnel junctions are employed for interfacing the spin-neurons with charge-based devices like CMOS, for large-scale networks. Device-circuit co-simulation-framework is used for simulating such hybrid designs, in order to evaluate system-level performance. We present the design of different classes of neuromorphic architectures using the proposed scheme that can be suitable for different applications like, analog-data-sensing, data-conversion, cognitive-computing, associative memory, programmable-logic and analog and digital signal processing. We show that the spin-based neuromorphic designs can achieve 15X-300X lower computation energy for these applications; as compared to state of art CMOS designs.

Keywords : Neuromorphic computation, spin device, non-Boolean, threshold logic, nano-magnets, domain wall magnet, neuron

I. INTRODUCTION

Neural-networks (NN) constitute a powerful computation paradigm that can algorithmically outperform Von-Neumann schemes in numerous data-processing applications [1]-[8]. However, CMOS based hardware implementations of neuromorphic architectures prove inefficient in terms of power consumption and area-complexity. On one hand, digital designs consume large amount of area, whereas, on the other hand, analog designs, although compact, lead to power hungry solutions. This has limited the scope of neural networks to algorithms and software.

In order to tap the potential of neuromorphic computation at the hardware level, the device-circuit models for the neuron and the synapse, apart from being compact, should also achieve low power consumption. In this work we propose the application of spin-devices in NN hardware design that can help achieve these goals.

Ultra low voltage, current-mode operation of magneto-metallic devices like LSV’s and DWM’s can be used to realize analog summation/integration and thresholding operations, and, can be used to model energy efficient “neurons” [1]-[8]. Such compact, low-resistance, magneto-metallic devices can perform analog-mode-computation, while operating at ultra-low magnitude, pulsed voltage-supply, thereby simultaneously achieving low power consumption as well as small area. We use magnetic-tunnel-junctions (MTJ) to interface the proposed device models for neuron with CMOS, in order to realize different classes of neuromorphic architectures, dedicated to different applications.

In brief, we propose an entirely novel hardware-design scheme which exploits specific spin-device characteristics to perform ultra low energy neuromorphic computation. The presented work involves innovation in device-modeling as well as in the associated circuit-design. It also addresses the architecture level issues related to such a heterogeneous integration, in order to arrive at a comprehensive design solution.

Rest of the paper is organized as follows. A brief introduction to spin torque devices and their application in logic design, proposed in literature, is provided in section 2. Section 3 describes the spin-based device models for neurons, proposed in this work. Neuromorphic circuit design scheme using the proposed devices is described in section 4. Section 5 presents some examples of neuromorphic architectures based on the proposed scheme. The performance and prospects of the proposed design scheme is discussed in section 6. Finally section 7 concludes the paper.

II. COMPUTING WITH SPIN DEVICES

Recent experiments on spin torque in device structures like lateral spin valve (LSV) [9], [10], domain wall magnets (DWM) [11], [12], and magnetic tunnel junctions, have opened new avenues for spin based computation. Several logic schemes have been proposed using such devices. Hybrid design schemes using MTJ have been explored that aim to club memory with logic and can possibly benefit from reduced memory-data traffic [18]. Use of spin-torque in LSV’s facilitated higher degree of spin current manipulation for logic. All spin logic (ASL) proposed in [13], employs cascaded LSV’s interacting through spin torque, to realize logic gates and larger blocks like compact full adders [14], based on spin majority evaluation. A number of logic schemes have been proposed based on current driven domain wall motion in magnetic nano-strips [15], [16]. Recently it has been shown that domain wall motion can be achieved with relatively small current density ($10^7$ A/cm²) in magnetic nano-strips with perpendicular magnetic anisotropy [20]. This phenomenon was exploited in a recent proposal on DWM based logic scheme that employed short magnetic nano-wires to model logic gates [15].

Most of the spin based computation schemes proposed so far have been centered on modeling digital logic gates using these devices. A wider perspective on application of spin torque devices however, would involve, not only exploring possible combination of spin and charge devices but, searching for computation models which can
derive maximum benefits from such heterogeneous integration.

We noted that ultra low voltage, current-mode operation of magneto-metallic devices like LSV’s and DWM’s can be used to realize analog summation/integration and thresholding operations with the help of appropriate circuits, and, can be used to model energy efficient “neurons” [1]-[8]. Such device-circuit co-design can lead to ultra low power neuromorphic computation architectures, suitable for different data processing applications. The proposed hybrid design scheme can open a new frontier for spin torque based analog and digital computing.

III. SPIN BASED DEVICE MODELS FOR NEURON

In this section we present different models for neurons based on spin-devices. Device-models for ‘summing – neurons’ are discussed in detail. In such a neuron, all input signals are clock synchronized and concurrent. Hence the ‘integration’ operation in the ‘integrate and fire’ functionality of a neuron can be simply replaced by summation. A brief description of DWM based ‘integrating-neuron’ is presented towards the end.

A. Neuron Models Based on LSV

1. Bipolar Spin Neuron

Fig. 1 shows the device structure for bipolar spin neuron [2], [4], [5], [7]. It constitutes of an output magnet $m_1$ with MTJ based read-port (using a reference magnet $m_5$), and two anti-parallel input magnets $m_2$ and $m_3$, with their ‘easy-axis’ parallel to that of $m_1$. A preset-magnet $m_4$, with an orthogonal easy-axis, is used to implement current-mode Bennett-clocking (BC) [13].

A current pulse input through $m_4$ presets the output magnet, $m_1$, along its hard-axis. The preset pulse is overlapped with the synchronous input current pulses received through the magnets $m_2$ and $m_3$. After removal of the preset pulse, $m_1$ switches back to its easy-axis. The final spin-polarity of $m_1$ depends upon the sign of the difference $\Delta I$, between the current inputs through $m_2$ and $m_3$. The lower limit on the magnitude of $\Delta I$ (hence, on current per-input for the neuron), for deterministic switching, is imposed by the thermal-noise in the output magnet, and, imprecision in Bennett-Clocking (BC). The effects of these non-idealities have been included in device simulation (fig. 2).

Transfer-function of an artificial neuron can be expressed as the sign-function of weighted sum of inputs, where the individual weights can be either positive or negative. In the proposed device, the neuron functionality is realized by connecting all the positive-weight inputs (excitatory inputs) to its right-spin input-magnet and vice-versa. The output magnet, in effect, evaluates the sign function with the help of Bennett-clocking, where the right-spin state can be regarded as the ‘firing state’

2. Unipolar Spin Neuron

Fig. 3 shows a slightly different device structure for neuron based on LSV that has a single input magnet. In this case the input magnet receives the difference of current from positive and negative weights magnets, i.e., the subtraction between the two current components is carried out in charge mode, outside the neuron device. As this device receives only the difference $\Delta I$ between the two current components, it can handle larger number of inputs thereby allowing larger scale network. This however comes at the cost of additional circuit design complexity that is discussed later.
3. Multi-input spin neuron with DWM synapse

The device operation explained above can be extended to a multi-input lateral spin valve (LSV) with programmable inputs in the form of DWM (fig. 4a), to realize a compact neuron-synapse unit [1]-[3] (fig. 5).

A DWM constitutes of opposite spin-polarity domains separated by a non-magnetic transition region, termed as the domain wall (DW). The DW can be moved along the nano-magnetic strip by current injection. Hence, a DWM interfaced with the metal channel of an LSV acts as a programmable spin-injector or a spin-mode synapse [1]. The spin-potential in the central region of the channel (around the ground lead below the output magnet) depends upon the sum of spin currents injected by all the DWM synapses and in turn determines the firing or non-firing state of the neuron, post-Bennett clocking. Fig. 6 depicts the plot for spin-potential in the central region of the channel, surrounding the output magnet of a 16-input neuron, under input conditions corresponding to firing and non-firing conditions. It shows that, in case of a firing event, the entire channel is dominantly at a positive spin potential and vice-versa.

Fig. 3 Unipolar spin neuron.

Fig. 4 (a) Domain wall synapse with channel interface (b) Spin polarization strength current injected through DWM as a function of DW location

In [18] we showed that both local as well as non-local spin torque can be used to realize the neuron models based on LSV described above.

Fig. 5 Spin-based neuron model with three inputs (DWMsynapses). The free layer of the neuron MTJ is in contact with the channel and its polarity, after preset, is determined by spin polarity of combined input current in the channel region (ground terminal) just below it.

B. Neuron Models based on Domain Wall magnet

1. Unipolar Summing Neuron

Low current threshold for domain wall motion in Perpendicular Magnetic Anisotropy (PMA) nano-magnet strips [20], can be exploited to model a ‘unipolar’ neuron shown in fig 7 [6]. It constitutes of a thin and short (20x60x2 nm³) DWM nano-strip connecting two antiparallel magnets of fixed polarity, \( m_1 \) and \( m_2 \). The magnet \( m_1 \) forms the input port, whereas, \( m_2 \) is grounded. Spin-polarity of the DWM layer can be written parallel to \( m_1 \) or \( m_2 \) by injecting a small current (~3µA) along
it, depending upon the direction current flow [15]. MTJ based detection port is used for reading the spin polarity of the DWM stripe (fig. 7).

![Fig. 7 Unipolar spin neuron using domain wall magnet.](image)

Note that, application of such a structure in memory [20] and digital logic design [15] has been proposed earlier. We exploit this structure to model a neuron using appropriate circuit scheme [6]. The input port of the DWM neuron receives the difference of the positive and the negative synapse currents, ΔI. In addition to this, a bias current can be supplied which effectively shifts the DWM threshold closer to the origin. As a result, a small positive or negative ΔI (~1µA) can determine evaluation to one of the spin states, thereby realizing the sign function of a neuron. We employ dynamic CMOS latch for reading the MTJ, which results in only a small transient current drawn from the ground terminal (G) of the DWM neuron, which can be kept below its switching threshold. Additionally, the time domain threshold for domain wall motion also helps in preventing read disturb from the small transient current [15].

2. Integrating Neuron Using Domain Wall Magnets

Spiking neural network is the most recent and evolving topology of neural networks. Among different NN classes, it is regarded as the closest analogue to the biological neural network.

![Fig. 8 Integrating neuron using DWM stripe: periodic restoration spikes are used to model ‘leaky integration’ in the neuron.](image)

It employs asynchronous communication between neurons using spikes. This necessitates time-domain integration of input-signals. Conventionally, dedicated capacitors have been employed for low speed SNN, while analog integrators have been used for getting higher performance. This once again presents the similar bottle neck of area and power consumption as described in the introduction. We propose the use of DWM stripe to realize time domain integration of input spikes. Step-wise motion of domain wall in longer nano-magnet stripes can be used to perform ultra-low voltage current mode integration. Firing state of the neuron can be detected using an MTJ (fig. 8). A DWM based integrating neuron allows spike transmission across ultra low terminal voltage and also mitigates the area overhead of capacitor. Hence it can lead to low power and compact SNN design.

IV. CIRCUIT INTEGRATION SCHEME

In this section, we describe the circuit integration scheme used in this work that exploits the ultra low voltage operation of the proposed spin neurons for energy efficient, analog-mode neuromorphic computation.

A dynamic CMOS latch senses the state of the neuron MTJ while injecting only a small transient current into the detection terminal [1]. The latch drives transistors operating in deep triode region, which transmit synapse current to all the fan-out neurons (fig. 9). The inter-connection scheme is different for unipolar and bipolar neuron models described in the previous section. For the bipolar neurons, two voltage levels differing by ΔV are used, i.e., V and V+ΔV (fig. 9a). Here V is a DC level close to 1V, whereas, ΔV can be around ~20mV. The source terminal of the output transistors are biased a V+ΔV, whereas as the ground terminals of the receiving neurons are connected to V. Hence, the synapse currents, involved in computation, flow across a small terminal voltage ΔV, thereby, reducing the static power consumption resulting from large number of analog-mode synaptic communications in a neural network.

![Fig. 9 Circuit integration scheme for (a) bipolar neurons and (b) unipolar neurons. (DTCS: deep triode current source transistors)](image)
For the unipolar neurons, the currents received from negative and positive synapses need to be subtracted in charge mode, outside the device. This necessitates the use of three different voltage levels (fig. 9b). The transistors corresponding to positive weights, effectively source current to the receiving neurons (I_{out}^+), whereas the transistors corresponding to the negative weights act as drains (I_{out}^-). In this scheme, most of the current flows between the two extreme levels, V+ΔV and V-ΔV, whereas, only a small net current flows to and from the mid DC level V, through the neuron devices. Hence, routing the additional mid DC level may not be a significant design overhead. However, as the synapse currents in this case flow across 2ΔV, for a given strengths of the current source transistors, this scheme leads to 2X higher computation energy as compared to the case of bipolar neuron. Note that, we have chosen two relatively high DC levels differing by ΔV (/2ΔV), rather than small absolute levels +/-ΔV (+/-2ΔV), in order to ensure stable supply voltages [1].

V. DESIGN EXAMPLE

The circuit integration scheme described above can be employed for realizing different classes of neuromorphic architectures. Weights or connection strength between neurons can be realized in different ways. For the multi-input neuron proposed in [1], the DWM inputs act as compact spin-mode synapses (fig. 10).
In the on-sensor image processing architecture presented in [5], A and B-type synapse weights were realized using weighted triode source transistors, as described above. Note that, in this scheme, the B-synapse transistors receive analog-mode photo-sensor voltage at their gate, and, in turn, provide proportional currents to the neurons. On the other hand the A-synapse transistors receive binary voltage levels at their gates, corresponding to the source neurons’ output state.

Simulation results for some common image processing applications like edge extraction, motion detection, half-toning and digitization (fig. 13), using the spin based CNN, showed ~100x lower computation energy, as compared to state of art mixed-signal CMOS designs. As mentioned earlier, the main advantage comes from ultra low voltage, pulsed operation of spin neurons that are applied to analog computation.

![Fig. 12. 3x3 neighborhood architecture of CNN and equation for neuron’s state: Current from each photosensor \( u_{ii} \) is transmitted to 3x3 neighbors through type-B synapses implemented using weighted transistors, whereas, inter-neuron connection is determined by type-A synapses.](image)

The cell state equation for Discrete-Time CNN is:

\[ x_i(n) = \sum_{(i,j) \in S^2} A(i,j, l) y_j(n) + \sum_{(i,j) \in S^2} B(i,j, l) u_n(n) + Z(i,j) \]

where \( y_i(n) = f(x_i(n-1)) = \begin{cases} 1 & \text{if } x_i(n-1) > 0 \\ 0 & \text{if } x_i(n-1) \leq 0 \end{cases} \)

X(n): cell state at \( T=n \), A: 3x3 inter-neuron weight, B: 3x3 input weight, Z: cell bias, u(n): 3x3 neighborhood input, y(n): cell output at \( T=n \).

![Fig. 13 Simulation results for different image processing applications: edge extraction, motion detection, halftoning and digitization: Table 1, 2 compares the energy per computation frame, per pixel, of the proposed CNN design with some recent CMOS designs for edge extraction and ADC.](image)

Programmable and self-adaptive weights can be realized using programmable conductive elements, like TiO\(_2\) memristor or phase change memory (PCM) [2]. Fig. 14 shows a cross-bar neural network architecture using memristor (/PCM) synapses and bipolar spin neurons. Depending upon the polarity of the connectivity between an input line and a neuron, one of the two memristive junctions between them is driven to the off state, while the other is programmed to match the required weight magnitude.

![Fig. 14 Cross-bar network design using (a) unipolar spin neuron, (b) using bipolar spin neuron](image)

The spin-neurons facilitate ultra-low voltage, pulsed synaptic communication across the cross-bar metal interconnects, thereby reducing the static-power consumption resulting from large number of inter-neuron signals per-cycle in a large-scale array. Such a design can provide ultra low power solution to several interesting applications, like, logic in memory, associative memory, programmable logic and pattern matching. Spiking neural networks based on memristive cross-bar arrays can realize self-learning networks for cognitive computing. Such a design employs some additional control circuits in each neuron to implement synaptic weight modification according to specific learning rules, as most of the power consumption in all such networks results from synaptic communication, which can be reduced using DWM based integrating-neurons.

### VI. DESIGN PERFORMANCE

Fig. 15 pictorially depicts the device-circuit co-simulation framework employed in this work to assess the system level performance for different neuromorphic architectures. The device models for neurons have been benchmarked with experimental data on LSVs’ and DWM [1]-[7]. The corresponding behavioural models are used for circuit and system level simulation.

![Fig. 15 Pictorially depicts the device-circuit co-simulation framework for assessing the system level performance for different neuromorphic architectures.](image)
different applications. The large benefits for analog applications (2-3 orders of magnitude) comes from the fact that ultra low voltage pulsed operation of spin-based neurons greatly reduce the static power consumption resulting from conventional analog circuits. For applications involving binary signal processing more than 15X-30X lower computation energy has been estimated.

Fig. 15. Device circuit co-simulation framework employed in this work

Fig. 16. Energy benefits of the proposed design scheme over CMOS for different applications.

VII. CONCLUSION

We proposed spin-based device models for neurons that can facilitate the design of ultra-low power neuromorphic-computation hardware. We developed device-circuit co-simulation framework to assess the performance of heterogeneous neuromorphic designs that employ the proposed neurons. We obtained highly promising estimates for common data processing applications that show 20X-300X improvement in computation energy as compared to state of art CMOS design. The research presented in this work involves device-circuit-architecture co-design and can lead to a comprehensive design solution for neuromorphic hardware.

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