StreamBrain: An HPC Framework for Brain-like Neural Networks on CPUs, GPUs and FPGAs

Artur Podobas¹, Martin Svedin¹, Steven W. D. Chien¹, Ivy B. Peng², Naresh Balaji Ravichandran¹, Pawel Herman¹, Anders Lansner¹,², and Stefano Markidis¹
¹ KTH Royal Institute of Technology, Stockholm, Sweden
² Stockholm University, Stockholm, Sweden
3 Lawrence Livermore National Laboratory, CA, USA

Abstract
The modern deep learning method based on backpropagation has surged in popularity and has been used in multiple domains and application areas. At the same time, there are other - less-known - machine learning algorithms with a mature and solid theoretical foundation whose performance remains unexplored. One such example is the brain-like Bayesian Confidence Propagation Neural Network (BCPNN). In this paper, we introduce StreamBrain—a framework that allows neural networks based on BCPNN to be practically deployed in High-Performance Computing systems. StreamBrain is a domain-specific language (DSL), similar in concept to existing machine learning (ML) frameworks, and supports backends for CPUs, GPUs, and even FPGAs. We empirically demonstrate that StreamBrain can train the well-known ML benchmark dataset MNIST within seconds, and we are the first to demonstrate BCPNN on STL-10 size networks. We also show how StreamBrain can be used to train with custom floating-point formats and illustrate the impact of using different bfloat variations on BCPNN using FPGAs.

Keywords
HPC, Unsupervised learning, Representation learning, Neural networks, AI, Emerging Machine Learning, BCPNN, GPU, FPGA

1 Introduction
The recent surge in popularity of Artificial Neural Networks (ANNs) is attributed to how they effectively map to existing high-performance hardware. Most deep learning [18] frameworks (e.g., Keras [12]) are implemented as (or transformed into) a series of dense matrix multiplications (GEMM). Dense matrix multiplication, coincidentally, has been the prime computation that has driven the assessment of High-Performance Computing (HPC) for the past decades through the TOP500 (https://top500.org/) performance assessment project. The famed neural network AlexNET [17] was realized by using Graphics Processing Units (GPUs) optimized for dense matrix multiplications, ultimately sparking the renewed interest in many-layer ANNs that we enjoy today. At the same time, there are a large number of alternative neural network models that host a sound and solid theoretical base, but which, to this day, remains empirically untested on a large scale. One such model is the Bayesian Confidence Propagation Neural Network (BCPNN) [15, 26].

BCPNN is a brain-like neural network, that builds on a Hebbian-like learning principle derived from Bayes theorem. The main building blocks are so-called hypercolumns units (HCUs) (considered to be the building block of the human cortex [21]), which account for computations in local receptive fields (e.g., share input pixels of an image). BCPNN can be used to implement unsupervised, semi-supervised, and supervised learning. It also features runtime-adaptable structural plasticity, which facilitates remapping of cortical components such as the connectivity of HCUs to maximize information entropy of the system, which can lead to better features [26]. BCPNN has recently been used for synaptic plasticity in large scale spiking cortex models of working memory function [9, 10] and temporal sequence learning and generation, implemented on SpiNNaker [16]. BCPNN was further shown to reach 98.58% accuracy [25] on the famed MNIST [19] classification benchmark. This is lower than reached by supervised gradient descent methods, but comparable to other methods using the unsupervised generation of hidden representation [25]. BCPNN has also been considered for ASIC acceleration [27]. Unfortunately, despite the solid theory that BCPNN holds, it still remains non-trivial for non-experts to adapt and explore the system.

In this work, we propose a high-level domain-specific language (DSL)/API to interface and use BCPNN for practical deployment in future supercomputers or data-centers. Contrary to prior BCPNN work (which focuses on its theory), the present paper focuses on how to map BCPNN in order to leverage modern state-of-the-art supercomputing resources and accelerators. We create a domain-specific language — conceptually similar to that of Keras [12] — that hosts functionality for creating, training, and inferring BCPNN-based neural networks. Our implementation, called StreamBrain, supports device heterogeneity, including (i) an OpenMP- or MPI-based [3], hand-vectorized general-purpose version, (ii) a highly-parallel GPU version based on the Compute Unified Device Architecture (CUDA), and (iii) a prototype for a Field-Programmable Gate Arrays (FPGA) version based on OpenCL [5] and High-Level Synthesis (HLS) on Intel devices, capable of using variable-precision numerical formats.

We claim the following three contributions: (i) StreamBrain, a Keras-inspired [12] DSL for implementation, evaluation, and deployment of BCPNN for use in future high-performance computers and data-centers, (ii) Analysis, implementation, validation, and empirical evaluation of three different BCPNN backends for CPUs, GPUs, and FPGAs, on the MNIST and STL-10 benchmarks and on two modern supercomputers, (iii) Empirical evaluation on both batching and variable-precision arithmetic on the BCPNN model.

2 The BCPNN Model
BCPNN is a brain-like neural network model that has both an abstract rate-based formulation and detailed spiking neuron-based formulation. In this paper, we focus on the rate-based formulation. We model the neural network problem with a collection of random variables \(x_1, x_2, ..., x_n, y_1, ..., y_m, z_1, ..., z_l\) as joint distribution \(p(x_1, x_2, ..., x_n, y_1, ..., y_m, z_1, ..., z_l)\). Each node of the graph represents a
random variable, while edges represent the conditional dependence or correlation between the variables. In particular, we determine the weights ($w_i$) and biases ($b_j$) characterizing the connection during a training phase, and then we use them for prediction in an inference phase. Internally, BCPNN is built up using hypercolumns (HCUs), which correspond to a particular variable. For example, if trying to identify numbers, a particular HCU might learn how to capture the number ‘5’. Inside HCUs are minicolumn units (MCUs), which capture a particular instance of the variable. For example, inside an HCU that captures the number of ‘5’, each MCU might learn a different version of the number ‘5’ (one rotated, one skewed, etc.). The BCPNN network capacity is thus a function of both how many HCUs the network has as well as how many MCUs are inside each HCU.

Unlike traditional DL, which relies on backpropagation for training the network, we use a localized (and unsupervised) brain-like rule to determine the neural network’s weights and biases. In our approach, the learning of the graph connection weights complies with Hebb’s postulate: learning only depends on the available local connections during a training phase, and then we use them for prediction in an inference phase. Internally, BCPNN is built up using hypercolumns (HCUs), which correspond to a particular variable. For example, if trying to identify numbers, a particular HCU might learn how to capture the number ‘5’. Inside HCUs are minicolumn units (MCUs), which capture a particular instance of the variable. For example, inside an HCU that captures the number of ‘5’, each MCU might learn a different version of the number ‘5’ (one rotated, one skewed, etc.). The BCPNN network capacity is thus a function of both how many HCUs the network has as well as how many MCUs are inside each HCU.

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![Figure 1: Array and matrix sizes for different quantities associated to the BCPNN graphical model.](image-url)

| Description | Size |
|-------------|------|
| $a_i$ | Activity in the input layer $A_i × Y_i$ |
| $b_j$ | Activity in the output layer $A_j × Y_j$ |
| $w_{ij}$ | Support in the hidden layer $A_i × A_j$ |
| $a_k$ | Support in the output layer $A_k × Y_k$ |
| $c_{ih}$ | Marginal probability in input layer $A_i$ |
| $c_{oh}$ | Marginal probability in output layer $A_o$ |
| $c_{oh}$ | Marginal probability in hidden layer $A_o$ |
| $c_{oh}$ | Marginal probability in output layer $A_o$ |
| $v_i$ | Connection weight $A_i × Y_i$ |
| $v_j$ | Connection weight $Y_j × A_j$ |
| $a_i$ | Connection bias $A_i × Y_i$ |
| $a_j$ | Connection bias $Y_j × A_j$ |

Algorithm 1: Unsupervised training of hidden layers

Result: Calculate $w_0$ and $b_0$

```plaintext
for 1 to $n_{epochs}$ do
    Shuffle input data;
    for $i_B$ ← 1 to $N_B$ do
        if $i_B / N_{HCU} == 0$ then
            Update plasticity mask;
        end
        $a_i$ ← batch of input data;
        $s_j$ ← $a_i w_0 + b_0$;
        $a_j$ ← softmax($s_j$) over the HCU;
        for 1 to $n_{cycles}$ do
            $C_i ← (1 - \lambda)C_i + \lambda(a_i)$;
            $C_j ← (1 - \lambda)C_j + \lambda(a_j)$;
            $C_{ij} ← (1 - \lambda)C_{ij} + \lambda(a_i ⊗ a_j)$;
            $w_0 ← \log(C_{ij}/C_i × C_j)$;
            $b_0 ← k_B \log(C_j)$;
            Apply mask to $w_0$;
        end
    end
end
```

2.1 BCPNN Performance Model

The main computational kernel used in the training and inference step of the BCPNN network is the batched outer product of arrays. The outer product of the two arrays is calculated as dense
which would cater to different needs for different users. These two
operations are: (i) Streaming, which allows a third party (e.g., a network card or camera) to deliver input data to the application at variable (and unpredictable) latencies, which are used to either train or infer using a network. (ii) Batched, which is similar to existing DL frameworks (but also incorporates the notion of time), for both training and inference. This paper focuses exclusively on exploring and investigating the batched execution mode. StreamBrain as a framework is implemented in Python, albeit core parts – particularly those that are computationally heavy – have been factored out and optimized with OpenMP, CUDA, or FPGA backends. A prototype version of StreamBrain has been made available at 1.

StreamBrain DSL: To facilitate an easy, portable, and familiar interface for using BCPNN, we created a Keras-like interface for StreamBrain. In this paper, we focus primarily on three-layer BCPNN use-cases that combine unsupervised (hidden layer) and supervised (output layer) training, which is implemented in our DSL using few lines of code (see Listing 1). StreamBrain is described in Python, allowing using it standalone or integration into existing ML pipelines. We also support multiple HPC backends.

StreamBrain Backends: The StreamBrain implementation is based on using the Python Numpy module and expressing the operation in Algorithm 1 as arrays and tensor operations. We implemented a series of backends to support accelerators targeting CPU, GPU, FPGA, and MPI. The backends can be switched easily through an environment variable and they are interfaced with the StreamBrain framework through Python bindings.

Python Implementation: StreamBrain is implemented in Python, leveraging NumPy where applicable for performance reasons. We have structured the implementation according to the function they perform, according to Algorithm 1. The first group of methods is responsible for computing activations inside the network (1:L7-9).

The second group of methods is responsible for learning and updating weights (Algorithm 1:L10-16). The final group is responsible for updating the receptive fields on layers with structural plasticity (Algorithm 1:L4-6). Out of all the methods implementing, perhaps the most important ones are the updateMarginals() (L11-L15 in Algorithm 1), the updateWeights() and updateBias() (L14 and L15 in Algorithm 1). These are the most computationally expensive, relying on an optimized BLAS library for performance; they are also the most salient candidates for accelerators. The structural plasticity (Algorithm 1:L4-6) follows the description in [26], and computes a score for each position in the receptive field and silencing active connections with the lowest score while activating connections with the highest score.

CPU Backend: Our CPU-backend use OpenMP primitives to parallelize those kernels that are the main computational bottlenecks (obtained through profiling) in the BCPNN model. These computational bottlenecks are mainly associated with the Python functions updateMarginals() as well as the updateWeights(). We merged the updates on $C_i$ and $CI_f$ to maximize temporal locality, and used OpenMP data-parallelism (#pragma omp parallel for) to distribute work across worker threads. Inside threads, we manually inserted vector operations to further increase performance. For matrix multiplications (such as the inference step, Algorithm 1:L8), we called Intel MKL’s SGEMM function.

GPU Backend: Our GPU backend was designed to fully run BCPNN on the GPU with little interaction with the orchestrating host CPU. We implemented it using CUDA and leveraged cuBLAS, adapting multiple techniques, including local prefetching, blocking, and preprocessing. Each CUDA warp operates on a single HCU, which allows us to use the warp shuffle functionality to finding sums of all elements inside an HCU in an efficient manner (for the softmax and structural plasticity). We have found this solution to work well, albeit for a much smaller (or larger) number of MCUs, a different implementation might make better use of the hardware. The structural plasticity mask is updated by a single warp, which will score the connections and activate/silence new connections; the infrequent updating of the structural plasticity makes it not the primary candidate for performance optimization. See our open-source implementation for more details.

FPGA Backend: To support emerging HPC and data-center infrastructure, we explicitly added support to offload parts of the computation to Field-Programmable Gate Arrays (FPGAs), currently targeting the Stratix V DE5-Net board. Rather than describing the hardware using low-level (and less portable) Hardware Description Languages (HDLs) such as Verilog or VHDL, we use High-Level Synthesis (HLS). We used Intel OpenCL SDK for FPGA [5], which was primarily driven by choice of hardware, our prior experiences [8, 23] and to accommodate support for the upcoming Intel OneAPI.

For the FPGA implementation, we focused on the partial acceleration of the two most heavy components of the BCPNN models: updateMarginals() and updateWeights(), both of which we merged into a single FPGA kernel in order to preserve space, encourage the sharing of resources and increase temporal data locality. Several components make up our FPGA accelerator. An address-generator is responsible for prefetching most of the data from external DDR memory and storing the fetched data in local blockRAM (a memory resource unique to FPGAs). A custom matrix engine

Listing 1: Describing a BCPNN Network in StreamBrain

```
# 1. Create empty network
def model = BCPNN.Network()

# 2. Add layers
model.add(BCPNN.StructuralPlasticityLayer())
model.add(BCPNN.DenseLayer())

# 3. train and evaluate
model.fit(dataset=().
model.evaluate(dataset=().
```

1 https://github.com/KTH-HPC/StreamBrain
will perform the necessary BLAS-3 matrix-matrix operation on the fetched data, before streaming the result to the network probability unit, which finalizes the update and streams the data back to external DDR memory. In this paper, we consider most of the data to be stored in external (DDR) memory, which can (in future work) trivially be extended to handle a stream of data (e.g., from a camera) for use with external devices. Unlike CPUs and GPUs, which work with a predetermined fixed floating-point precision format, our StreamBrain accelerator can vary the type of floating-point representation that is used. More specifically, all additions, subtractions, multiplications, division, and logarithm floating-point functions can be varied, which is a property we exploit to study the resilience to numerical precision that BCPNN has (not only multiply-accumulate as in NVIDIA Tensorcore or Google TPU). Such studies are also imperative to later guide a BCPNN ASIC accelerator. We implemented variable precision through custom Register Transfer Level (RTL) VHDL code generated by FloPoCo [7], and created a custom OpenCL library with these variable-precision operators inside, allowing said operators to be invoked through regular C-like function calls. We investigate variations of the IEEE-754 single-precision, but with reduced mantissa, and can call them BF28 down-to BF14– our BF16 representation is identical to the one in, e.g., Google TPU.

MPI Backend: To support training with large-scale datasets across multiple nodes on HPC systems, we extend the CPU Backends to use data-parallelism through a hybrid MPI-OpenMP approach. In each step, a batch is further divided by the number of processes where each process is responsible for a sub-batch. Weight updates are performed using MPI_Allreduce() to derive a global mean operation over all the batches (for L11-13 in Algorithm 1) before updating the marginal probabilities (C) and weights (w) locally. For all other CPU Backends, we distribute work using block distribution and finalize using MPI_Allgatherv(). Inside each process, OpenMP is used to further parallelize the computation.

4 Results

We evaluated StreamBrain on a broad and diverse set of architectures, including GPUs and FPGAs. The systems were as follows:

1) Beskow is a supercomputer at KTHi on the Cray XC40, where each node has two Xeon E5-2698V3 Haswell 2.3 GHz, 64 GB RAM, running Python 3.7 and MKL+IntelMPI-ICC 19.0.1.144.

2) Kebnekaise is a supercomputer at HPC2N, containing either two Intel Xeon E5-2690v4 or Gold 6132 processors per node, which also contains NVIDIA Volta-100 GPUs (Pcie), running OpenMPI 3.1.3, GCC 8.2.0, Python 3.7.2, MKL 2019.1.144, and CUDA 10.1.243.

3) A100-system is local KTH node with an AMD Epyc 7302P (16-Core) processor, a NVIDIA Ampere-100 GPU (Pcie), running GCC 8.3.1, CUDA 11.1, Intel MKL, and Python 3.8.

4) FPGA-system is a local KTH node with an Intel Core i5-8400 with an Intel DE5-Net board (Stratix V 5SGXEA7N2F45C2).

All evaluations applied aggressive optimizations (~0.3). All GPU experiments were done with a single GPU (NVidia A100 or V100). For the FPGA evaluation we disabled caching (~nocaching), relaxed floating-point ordering (~fp-relaxed), and created custom IEEE-754 derived FPUs (for addition/subtraction/multiplication/logarithm) using FloPoCo [7] and manually assembled them into an OpenCL library. We enabled the OMP_PROC_BIND=true environment variables for those platforms that gained from using it. NumPy was recompiled with support for Intel MKL. For the evaluation, we used MNIST [19] and STL-10 [4], both well-known and well-used image recognition benchmarks. For both the MNIST and STL-10 experiments, we use a 3-layer network (input, hidden, output) where the hidden layer is composed of 3000 MCUs and the number of HCUs a hyperparameter. The batch-size varies depending on the experiment. We optimize hyperparameters by doing 1000 runs as follows: (i) 250 quasi-random samples using the AX platform (https://ax.dev), (ii) one worker selects a hyperparameter using the GPEI algorithm from the AX platform, and (iii) all other workers select hyperparameters using TBPSA algorithm from Nevergrad.

4.1 StreamBrain CPU and GPU performance

We start by quantitatively evaluating StreamBrain on both general-purpose processings (CPUs) and Graphics Processor Units (GPUs) using the well-known MNIST [19] handwritten digit recognition benchmark. We use MNIST (instead of, e.g., the larger ImageNET or STL-10) because the performance (in terms of accuracy) of MNIST using BCPNN is well-understood and documented, allowing us to examine compute performance of StreamBrain and correctness.

Fig. 2.a shows the performance of StreamBrain as a function of batch-size on MNIST for both CPUs and GPUs, using both IEEE 754 single- and double-precision (named f32 and f64 respectively). Overall, we notice that the performance increases as a function of batch-size; a larger batch-sized encourage more data-parallelism [2] and locality, turning multiple expensive BLAS2 operations into a single BLAS3 operation. We also notice that the difference between the CPU and GPU StreamBrain is rather large, ranging between 7.75x-65x in favor of the GPUs; this difference is larger with double- compared to single-precision, is also because more code remains in Python for the CPU (contra GPU) version. We also see an (expected) near two times increase in performance of decreasing the width of the numerical representation and going from double- to single-precision increase the performance of ~ 2x on the CPUs and between 1.7x and 1.26x (on average) on the GPUs. Training the entire MNIST dataset using StreamBrain can be as fast as ~ 10 seconds using the NVIDIA A100 GPU or ~ 4 minutes on a server-class Xeon CPU. The (seemingly) large difference between AMD Epyc and Intel Xeon processors is because our code has dual-socket Intel Xeons (while we only used a single AMD Epyc processor). Fig. 2.b shows inference (or prediction) performance of the StreamBrain framework. Here, the difference between the CPU and GPU is lower and can be as low as 3x difference (Xeon vs V100 in some cases), albeit on average the CPUs are between 5x-8x slower. As with training, the performance scales with the batch-size: single-image inference (or "streaming") reach between 28k to 87k images/second, while a larger batch-size allows up to 350k images/second to be achieved by the GPUs. Fig. 2.c shows the inference accuracy, here averaged across all batch-sizes. Overall, all implementations yield an average that is above 95%, which is roughly 1% away from the boosted learning in [26]. There are some discrepancies both between using single- and double-precision, as well as between the GPU and CPU versions. The difference in architecture is likely because of the different random generators used to initialize the network at the start. Finally, 97.5% of accuracy can be reached by using a
hybrid solution: using StreamBrain to derive hidden layer representations using unsupervised learning and use a stochastic gradient descent (SDG) training only for the output layer, demonstrating correctness with the hybrid approach as reported in [25] (average of 97.77%). We end by noting that training a network to reach 95.5% with StreamBrain on MNIST is faster (10.5 seconds) than training an MLP of similar capacity with PyTorch (33.94 ± 1.04 seconds) to reach the same 95.5% accuracy on the modern Nvidia A100, showing a benefit in performance over PyTorch (albeit, given longer time, the PyTorch version will reach a better accuracy).

4.2 StreamBrain FPGA Exploration

In the previous section(s), we evaluated our high-performance BCPNN implementation in StreamBrain on the MNIST benchmark to verify correctness with prior work. We also observed that the testing accuracy degradation between IEEE-754 single- and double-precision was negligible, yielding the follow-up question: how tolerant (or resilient) is BCPNN to reductions in the number representation? A smaller representation can significantly increase performance (more data per unit bandwidth) and reduce the silicon FPU footprint. In this section, we leverage our FPGA implementation to explore number representations that (for performance reasons) are hard to explore in CPUs (simulating different representations is slow). More specifically, we create custom hardware that uses (the today well-known) brain-float 16 (BF16) representation, as well as create alternative versions that we call BF14, BF15, BF20, BF24, and BF28 (that have between 5- and 19-bit mantissa), and accelerate the most compute-intensive functions of StreamBrain on the FPGA. Despite using a rather old FPGA (from 2010), the performance of our FPGA accelerator is faster than the original code in Python/NumPy, and is comparable to that of the CPU versions. Fig. 3 shows the training accuracy (blue diamonds) as a function of numerical representation, and we see that the BCPNN model is resilient enough to tolerate down-to BF16 with minor (∼ 4%) accuracy degradation; BF20 and higher experience no accuracy degradation compared to single-precision. BF14, however, drops down to mere chance (∼ 10%) for the MNIST dataset, while BF15 is between (67.5%). While the operating frequency(red squares) of using a different representation tends to stay roughly the same (between 198 and 252 MHz), the resource utilization tends to decrease as a function of reduced numerical representation. While all types of resources decrease with smaller representation, interestingly, the DSP utilization drop significantly (from ∼ 70%+ to 10% when using BF16 and below). We cannot fully understand this jump in reduction, but it is likely that smaller representations are synthesized to logic (rather than DSPs). In short, our experiments show that BCPNN would be a good candidate to accelerate on BF16-capable devices, such as Google’s TPU or the upcoming Power10 or Intel Sapphire Rapids. In future work, we would use the FPGA to explore alternative representations (e.g., Posit [13, 24]).

4.3 Higher-Dimensional Problems

In the previous section (and also in prior work), applying BCPNN was limited to MNIST-sized data-sets primarily due to the lack of a high-performance framework. With StreamBrain, for the first time, BCPNN can now be scaled to more complex high-dimensional problems. We trained the STL-10 dataset (∼ 30+ times larger than MNIST) using BCPNN for 100 (hidden) and 20 (output) epochs using StreamBrain’s GPU backend on the NVIDIA A100 on a network with 3000 MCUs (20 HCUs). To contrast our performance, we also trained an MLP network with similar capacity using PyTorch (AdamW optimizer, cross-entropy loss function, ReLu activations) also for 100 epochs. The time to train the BCPNN network was 178.2±0.1 seconds and yielded a test accuracy of 34.8±4.9%. The
(deep learning type) PyTorch trained network took 100.2±0.43 seconds and yielded a test accuracy of 42.2±0.12%. Ignoring the better accuracy (+7.4%) that the backpropagation-type network gave, both performances are comparable, where our StreamBrain is ~77% slower – a respectable number given the difference in the number of manhours spent in StreamBrain versus PyTorch.

4.4 Strong scaling

We end the result section by measuring the strong scaling properties of StreamBrain (MPI-backend) when given between one and eight nodes of computing capacity on the Kebnekaise and Beskow supercomputers. The problem to solve is to train on the STL-10 benchmark under a batch-size of 512. Fig. 2d shows the speed-up (relative to single-node performance). We see that the speed-up on the Kebnekaise machine is very stable, and both the single- and double-precision version reaches (near) identical performance, albeit capping out at 2.7x. For the Beskow computer, there is one anomaly when using four nodes between the single- and double-precision version, which we still do not fully understand. At eight nodes, the Beskow supercomputer yields a peak of 5.25x speed-up. Note how the test accuracy, even with a batch-size of 512, remains comparable to that with lower batch-sizes (previous section).

5 Related Work

Our contribution, StreamBrain, has been primarily inspired by the many different DSLs and libraries that exist for use in deep learning. We name Keras [12] as our primary source of inspiration, but equally intuitive interface also exists in PyTorch [22]. Outside of DL, the literature and availability of such frameworks are sparse. For the neuroscience community, domain-specific mark-up languages and libraries such as Neuron [14] and NEST [11] provide an interface to simulating highly accurate and exact spiking neural networks. Despite the relatively large user base that these tools have, they are not a good match for applying emerging brain-like networks. Despite the relatively large user base that these tools have, they are not a good match for applying emerging brain-like models in practice, as they are often too detailed (and hence slow to simulate) and aimed at simulating the biological brain; using these tools requires significant expertise and effort. Moving an abstraction layer up, simulation frameworks such as PyNN [6] offers a DSL for describing populations of spiking neurons and multiple simulation backends. At this level, it is possible to undertake experiments and evaluations for practical tasks such as the image recognition we do here. However, many of these frameworks still incur a steep learning curve. There is, however, one framework that provides an interface similar to the one of StreamBrain: Nengo [1]. Nengo’s Brain Maker allows the simple creation of brain-like neural network models, both spiking and non-spiking, for use in ML, with examples showing, for example, MNIST. Nengo supports the same backends as StreamBrain, including CPU, GPU, and FPGA [20] implementation. Unlike Nengo, StreamBrain focuses on BCPNN.

6 Conclusion

We have introduced StreamBrain – a high-performance DSL targeting the BCPNN model. We presented and evaluated four different backends on GPUs, FPGAs, and CPUs. We show how to train MNIST as fast as 10 seconds, and showed results (for the first time) on higher dimension problems such as STL-10. We also introduced batching into BCPNN and showed that BCPNN could work with low-precision arithmetic. Our contribution enables future exploration of BCPNN in HPC Computing.

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