Design of Vedic multiplier-based FIR filter for signal processing applications

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Abstract: Digital Signal Processing (DSP) devices are becoming increasingly important with the introduction of multiple signal processing techniques. Vedic Multiplier is one of the most common applications for high-speed DSP deployment. This paper constitutes a significant development in the design of the FIR filter architecture based on the modified Nikhalam Sutra Vedic multiplier. In addition, the Kongestone adder is used to increase speed performance. Using Xilinx FPGA Spartan 6 with Xilinx ISE, the modified architecture of FIR filter has been simulated and synthesized for achieving optimized results. The simulation results of the proposed FIR filter architecture illustrate that it operates at least 20 percent faster than traditional multiplier-based FIR filters.

Keywords: Finite Impulse Response filter, Vedic algorithm, Signal processing, Xilinx FPGA

1. INTRODUCTION

Digital Finite Impulse Response (FIR) filtering is an all-powerful mechanism that takes place on DSP systems[1, 2]. Multiplication operations that result in unnecessary power consumption, area and delay have dominated FIR filter problems since the last decades. Various filter architectures and algorithms[3] have been developed more efficiently to circumvent FIR filters. Multiplier blocks present in FIR filters, multiplier-less or alternative multiplier blocks are used to minimize power consumption and area. Many multipliers-less architectures have been developed to increase the performance of FIR filters. These are referred to as conversion-based designs [4,5] and memory-based designs [6-9].

Distributed arithmetic method is one of the most efficient architectures, with fewer multiplier being used to implement a memory-based FIR filter[10-12]. Comparable input data and coefficients for DA filters are typically bi-directional. In the DA algorithm, the time of propagation is proportional to the length of the input data bit[13]. If not, the design performance will be reduced because the length of the input data is short. The generation of the filter is adapted to the optical high-speed signal processing using the RNS number system.

Alam& Gustafson [14] uses time-multiplexed output to implement filter masking technology. This approach is developed using frequency response masking techniques to minimize the complexity of FIR filters in the restricted transition band. Both methods are used to simplify periodic modeling and filter masking. Sailaja[15] carried out experiments on various multipliers using the Wallace multiplier, multipliers based on the CLA adder, the CSA adder and the Vedic multiplier which are
being checked for modern FIR design integration. Over several decades, several designs have been built over low-complicity FIR operation. Using different transformation methods, the construction of Filter design may be carried out. The FIR filter's hardware architecture consists of adders, multipliers and delay elements. Through designing strategies that provide an efficient algorithm to minimise the number of operations involved in the various components, the architecture of the FIR filter can be simplified.

The literature survey shows that the latest approaches for the design of the FIR filter are based on either architectural changes or technical developments. In addition, the configuration of the multiplier plays a crucial role in the FIR filter. The use of the FIR filter is better applicable to Vedic multipliers as opposed to other empirical methods. Thanks to its simple architecture, the Vedic multipliers result in less hardware resources and faster operating speed, this FIR filter design using Vedic math is a success. This research focuses on designing and modifying high-performance FIR filters that have not been studied using Vedic approaches. The introduction to Vedic mathematics is discussed in Section 2. The methodology adopted in this work is discussed in Section 3. The proposed modified design of FIR filter and its corresponding simulation results are discussed.

2. OVERVIEW OF VEDIC MATHEMATICS

Indispensable developments in accelerated production have been on the rise as a result of all growing signal processing systems. Advanced multiplication method is known to have completed the maximum cycle of various FIR filtering systems. Filter is the primary signal processing tool used in a variety of applications. The center of each processing unit depends on its inclusion and multiplication scheme, the quality of which determines the precision of operation and the efficiency of the FIR filter. In addition, the size of the filter increases multiplication and slows down the entire process. Optimizing rate and area is therefore a major constraint and a contradictory concern regarding speeding up. Like the traditional model, multiplier takes a certain amount of time to measure each resource. Experimental work also depends on improving the estimation of multipliers and adders.

Ancient Vedic techniques include a broad variety of methods to solve math operations. Due to this reason, this work explores and analyzes various current multiplier methods with Vedic methods and quick adders. From the analysis, progress has been made towards the realization of an efficient FIR filter.

With the process of easy cross-checking Vedic mathematics derived from Veda performs a very fast solution to any mathematical problem. The word Veda was derived from the Sanskrit word root vid, which means knowledge without limits. The word Veda is also meant to be a repository of knowledge and information. Sri reintroduced the concept of the Vedic mathematics. Bharati Krsna Tirthaji. With his extensive study of Atharva Veda, he built 16 mathematical sutras and 13 up-sutras. The sutras are powerful and simple, covering the whole branch of mathematics. All arithmetic operations such as addition, subtraction, division and multiplication required for the operation of any processor may be carried out effectively using these 16 sutras[16]. This paper offers an overview of and use of the high-speed square and multiplier architectures concept. A lot of research has been done in Nikhilam and Urdhava sutra on multiplier principle [17-18].

The multiplier principle is based on the Urdhva-Tiryakbhyam(UT) algorithm of ancient Indian-Vedic mathematics. In either case, Urdhva-Tiryakbhyam Sutra is a broad variety of multiplication formulas. This basically means 'vertical and cross-sectional.' It is founded on the idea that all partial products can be generated simultaneously by adding other partial products. The parallelism of the development and summation of the partial product is described in Figure 1, using Urdhva-Tiryakbhyam. The algorithm can be generalized to a bit size of n x n. Because the device properties are calculated in addition to their quantity, the multiplier is independent of the clock frequency of the processor. The multiplier then carries the output variable independently and is thus independent of the clock
In addition, Nikhilam Sutra means 'all 9 and last 10.' Although this is true for all multiplication circumstances where the numbers involved are the, it is more efficient. Because it controls the addition of a large number to perform a multiplication operation from its adjacent base, the initial number is simpler, the multiplication complexity is smaller than seen in Figure 2. Keeping in mind the multiplication of two decimal numbers (96 * 93), we first explain this Sutra, where the chosen base is 100, which is stronger and greater than the two. Nikhalam sutra is shown in Figure 2.

3. PROPOSED FIR FILTER DESIGN METHODOLOGY

The systematic method adopted in this study is a step-by-step methodology for applying the problem under consideration. Next, the FIR filter and vedic multiplier requirements are to be defined on the basis of the literature survey. Two types of solutions are identified from the literature survey. One is a technological solution and the other is an architectural solution. Existing architectures are built with lower technical nodes in the technological solution. Numerous modifications are made to the current architectures in the architectural solution and the corresponding FIR filter is introduced.

The architectural solution is chosen to implement the FIR filter in this work. The Vedic multiplier is chosen to replace the current traditional multipliers due to its low power and high speed properties. Then the HDL Verilog coding is written for the desired topology. Figure 3 shows that, on the basis of a literature survey, the configuration of the FIR filter with a Vedic multiplier and adder is specified first. Later, the appropriate equipment technology must be chosen on the basis of the requirements. Then the simulation is performed and the correct parameter values are obtained. These values are compared with the specifications to check whether or not the specifications are met. If the requirements are not met, the suggested circuit will be implemented using optimization techniques to reach the correct specifications; otherwise the circuit may be implemented without any optimization.
4. PROPOSED ARCHITECTURE AND DESIGN OF FIR FILTER USING MODIFIED NIKHALAM SUTRA

The FIR order simplifies the creation of FIR filters for add-on and modification operations and the primary objective of this strategy is to reduce the sum of additional and subtraction transactions [19]. The downside of this approach is that the coefficient cannot be modified until the filter design has been defined. Due to this, difficulties in FIR filter programming this method is not acceptable. Though the abovementioned difficulties can be solved by the use of Vedic Mathematics with previous techniques.
In FIR filter design, the Vedic multipliers used are simple and very powerful. Such simple methods for improving process parameters are groundbreaking, efficient multipliers. In this method, the FIR filter is indicated by the use of the Vedic multiplier algorithm to replace the conventional multipliers used in it as shown in Figure 4.

Using linear convolution, the direct form structure of the FIR filter can be determined. All sequences \( k(n) \) and \( j(n) \) are finite in the FIR filter, and thus linear convolution is finite. The convolution will give the output sequence \( y(n) \) with an input \( x \) of length \( P \) with a filter of length \( Q \). Figure 4 represents the FIR filter's direct form structure. Vedic Mathematics contains several multiplication algorithms from which Nikhalam Sutra has been selected. Through using this Sutra, a modified Nikhalam Sutra is proposed to be used for the implementation of FIR filters. This approach further improves the Vedic multiplier by using strong adders. The approximate 8-Tap FIR filter is generated using a multiplier and adders for a similar sample of inputs.

To get the following specifications, a low-pass FIR filter must be constructed:
- **Type of filter:** low pass filter
- **Sampling Frequency(s):** 2000 HZ
- **transition/Cut-off Frequency:** 460 HZ
- **Length of filter (M):** 8

\[ F_t = \text{Cut off or transition frequency} / \text{ sampling Frequency Hz.} \quad (1) \]

The frequency of transformation \( (f_t) \) is calculated based on Equation (1).

\[ F_t = 460/2001 = 0.23 \text{ Hz} \]

The rectangular frame truncates the normalized frequency response. Unless the generic transfer method weights the range, the coefficients inside the length of the window will be maintained and the period will be omitted. There are several windows, including a rectangular one, a barlet, a hanging one, a hamming one, a black maan, and a kaiser with a rectangular frame. You can measure the right window feature using a rectangular window system. As seen in Equation (2), the optimal impulse response of the low-pass filter can then be rewritten using a rectangular plane.

\[ J_P(n) = \begin{cases} \frac{\sin[2\pi f_t(n - \frac{M}{2})]}{n(n - \frac{M}{2})} & \text{if } n \neq \frac{M}{2} \\ 2f_t, & \text{if } n = \frac{M}{2} \end{cases} \quad (2) \]
The respective coefficient values of the filters \( jD(n) \) are determined for the filter length \( M=8 \). The equation (3) shows the difference between the filters of the FIR.

\[
g(n) = \sum_{n=0}^{M-1} b_u k(n - u) \tag{3}
\]

The equation above indicates the length of the device \( M \) as the time limit is 0 to \( M-1 \). This cycle is a causal sequence, ranging from 0 to \( M-1 \). With the aid of Z-Transform, we shall obtain equation (4) from equation (3).

\[
G(Z) = \sum_{u=0}^{M-1} b_u K(Z) Z^{-u} \tag{4}
\]

Equation (5) includes the conversion function of the FIR method.

\[
J(k) = \frac{G(Z)}{K(Z)} = \sum_{u=0}^{M-1} b_u Z^{-u} \tag{5}
\]

5. PROPOSED MODIFIED NIKHALAM MULTIPLIER

Among the different operations used in the design of the FIR filter, multiplication operation is very important because it needs additional resources to work perfectly. The efficiency of the multiplier depends more on the adders used in the design to measure the final number. On this basis, a new multiplication unit using KSA and Nikhalam Vedic sutra multiplier is proposed to resolve the drawbacks mentioned above. This multiplication has the advantages that it requires less power, less delay and less area.

Two binary numbers are used using the Nikhalam Vedic multiplier. In this method, the CSA is replaced by a KSA high-speed adder. This approach enables successful execution by multiplying from one bit to another and evaluating the partial product sum and generating output[20]. The block diagram for the proposed Vedic multiplier is shown in Figure 5 using the KSA adder rather than the RCA or CLA. KSA offers more advantages than CSA, which enables high-speed processing and reduces delays in propagation. As a consequence, the output of the Nikhalam multiplier can be obtained in a shorter time using KSA[21].

![Fig 5: Modified Nikhalam Vedic multiplier](image-url)
6. DESIGN OF FIR FILTER USING MODIFIED VEDIC MULTIPLIER

The proposed modified Vedic multiplier is used for the design of a digital low-power FIR filter. This method is similar to the design of the FIR filters with the Nikhalam sutra, but simplifies the adder functionality by integrating new techniques into the multiplier process. The new filter series outperforms previous methods by integrating the CSA and the KSA. The use of the modified Vedic multiplier is an easy and efficient process for any complexity of the filter configuration. The revised Nikhalam Multipliers used the FIR filter design method as shown in Figure 6. Using the proposed multiplication process, the input value k(n) is multiplied by the vector coefficient j(n) and summed for the right resulting number. The proposed FIR Filter architecture based on the 8-Tap Direct Form-I can be easily adapted to FPGA applications using the modified Nikhalam as shown in Figure 6. The vector k(n) is the set number of inputs. The j(n) function represents the nth FIR filter coefficient for KSA, the two numbers to be used for this modern multiplication of the Vedic, i.e. Modified version of the Nikhalam Vedic multiplier. On this basis, the modified Nikhalam multiplier can be used to calculate the filter coefficient j(n) and the input variable k(n) to minimize the operation of the FIR filter. Rather than simply multiplying the larger inputs, the filter performs multiplication operations by adding the specified amount obtained from W.B, thereby increasing the operating speed. In addition, KSA makes use of partial goods to boost speed. Finally, the multiplication and addition of units perform a bitwise addition with the necessary modifications.

Fig 6. The suggested FIR Filter design uses modified Multiplier based on Nikhalam Sutra

7. RESULTS & ANALYSIS

In this work the different multiplier architectures are being implemented and synthesized with Spartan 6 FPGA by Xilinx ISE. Here simulation is carried out for multipliers with length taken as 8-bit.

Fig 7. Transient Simulation of 8X8 Array Multiplier
The Figure 7 shows the multiplication carried out Array multiplier with 8 bits each for the inputs X and Y. The resultant of the multiplication is shown by the output vector P.

Fig 8. Transient Simulation of 8X8 Bough-wooley Multiplier

The Figure 8 shows the 8-bit Bough–Wooley Multiplier with inputs x and y and the corresponding result is assigned to vector P.

Fig 9: Transient Simulation of 8X8 Wallace Tree Multiplier

The Figure 9 shows the multiplication carried out Wallace tree multiplier with 8 bits each for the inputs x and y. The resultant of the multiplication is shown by the output vector P.

Fig 10: Transient Simulation of 8X8 Booth Multiplier

The Figure 10 shows the 8-bit Booth Multiplier with inputs x and y and the corresponding result is assigned to vector P.

Fig 11: Transient Simulation of 8X8 UT based Vedic Multiplier

The Figure 11 shows the multiplication carried out UT sutra based Vedic Multiplier with 8 bits each for the inputs a and b. The resultant of the multiplication is shown by the output vector named as result.
The Figure 12 shows the 8-bit modified Nikhalam sutra where inputs are x and y and the corresponding result is assigned to vector r.

Also for the multipliers architectures are synthesized in Xilinx ISE and their corresponding delay and area parameters are tabulated in the Table 1.

| Name of the Multiplier                  | Delay(ns) | Area(4-bit LUTs) |
|-----------------------------------------|-----------|------------------|
| Baugh Wooley Multiplier                 | 25.011    | 121              |
| Array Multiplier                        | 31.132    | 126              |
| Booth Multiplier                        | 26.608    | 144              |
| Wallace Tree Multiplier                 | 27.814    | 139              |
| UT Sutra Vedic Multiplier               | 21.542    | 121              |
| Modified Nikhalam Sutra Vedic Multiplier| 18.412    | 75               |

From the Table 1, it is clearly seen that the delay and area occupied by modified Nikhalam sutra Vedic Multiplier are better when compared with the other architectures. With the approach of using high speed Koggestone adder instead of other adders like RCA or CLA reduced the delay and area occupied due to the multiplication process. As a consequence, the output of the Nikhalam multiplier can be obtained in a shorter time using KSA.

From the Table 2 and it is crystal clear that Comparative Analysis of various multipliers like array and Urdhva Thiryakbhyam sutra based multipliers used for FIR filter Implementation is explained in terms of delay, area and power dissipation.

Figure 13 shows the simulation result using the Nikhalam Vedic multiplier for the FIR filter. There are several different multiplier modules in the FIR filter but this module provides improved results by using the Nikhalam Vedic multiplier.
Table 2. Comparative Analysis of various multipliers used for FIR filter Implementation

| FIR Implementation with a Multiplier | Delay(ns) | Area(4-bit LUTs) | Power (mW) |
|--------------------------------------|-----------|-----------------|------------|
| Array Multiplier                     | 34.323    | 236             | 28         |
| UT Sutra Vedic Multiplier            | 24.322    | 211             | 17         |
| Modified Nikhalam Sutra Vedic Multiplier | 19.873  | 168             | 14         |

With this Vedic Multiplier, architectural defects due to structural irregularity may be reduced. Since the configuration of the Vedic multiplier is periodic, the design of the silicon chip is simple. Among the multipliers tested, KSA used the Nikhalam Vedic multiplier to produce a modified Nikhalam multiplier with less delay and higher speed performance. This method takes much less time to achieve 16-bit results. As a result, improved performance reduces delays by using KSA in the effects of the Nikhalam multiplier, and the area improves efficiency. Nikhalam modified filter is used for the implementation of the FIR filter. The proposed design was simulated and synthesized for real-time testing using Xilinx FPGA Spartan 6 and Xilinx ISE. The simulation results show that the suggested architecture has a very good processing speed with a cumulative delay of just 20 ns, which is 20% faster than the designs with other multipliers.

Table 3. Comparative Analysis of various Proposed FIR filter with existing architectures

| Proposed architecture | [22] | [23] | [24] | [24] | [24] |
|------------------------|------|------|------|------|------|
| FIR Filter Topology Used | Complex Multiplier using CBL Adder | High speed FIR filter based on vedic Mathematics | Parallel FIR Filter Using Wallace Multipliers |Parallel FIR Filter Using Vedic Multipliers | FIR filter based on Modified Nikhalam Sutra Vedic Multiplier |
| Delay(ns)              | 65.89 | 38.19 | 19.8 | 18   | 19.8 |
| Area(number of Luts)   | 43095 | 307   | 687  | 1097 | 168  |

From the table 3, it is evident that the proposed architecture occupies very less area when compared with the existing FIR filter architectures. The proposed architecture also exhibits better speed when compared with the other FIR architectures.

8. CONCLUSION

This paper presents a FIR 8-tap filter based on the modified Nikhalam sutra multiplier. In addition, the modified Nikhalam Vedic Multiplier is used to reduce the delay and improve the efficiency of the FIR filter compared to the current FIR filter multipliers. It makes for more powerful DSP systems due to the ability of the vedic multiplier to perform fast computing operations. Simulation results show that the processing speed of the current architecture is 20% higher than the existing FIR filter. The vedic multiplier-based FIR filter also consumes approximately 50 percent less power than the standard traditional array multiplier-based FIR filter. Also the proposed FIR filter utilizes 30% of less area when compared with conventional array multiplier based FIR filter.

In future with the response to the rapid growth of technology, new engineering solutions and new architectures may be developed to meet the demand for technology size. In addition, with ongoing technological developments, researchers may focus on new IC architecture approaches for wireless medical and health care applications with low power consumption. There may be a scope for developing design strategies at both the device level and the circuit block level on the basis of recent technological advancements.
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