Effects of Interface Roughness Scattering on Radio Frequency Performance of Silicon Nanowire Transistors

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The effects of an atomistic interface roughness in n-type silicon nanowire transistors (SiNWT) on the radio frequency performance are analyzed. Interface roughness scattering (IRS) is statistically investigated through a three dimensional full–band quantum transport simulation based on the sp3d5s∗ tight–binding model. As the diameter of the SiNWT is scaled down below 3 nm, IRS causes a significant reduction of the cut-off frequency. The fluctuations of the conduction band edge due to the rough surface lead to a reflection of electrons through mode-mismatch. This effect reduces the velocity of electrons and hence the transconductance considerably causing a cut-off frequency reduction.

Keywords: interface roughness scattering, silicon nanowire transistor, RF, cut-off frequency

Since the lengths of silicon (Si) metal-oxide-semiconductor field effect transistor (MOSFET) have been scaled down to the sub-100 nm regime, the cut-off frequency has increased significantly to reach hundreds of gigahertz (GHz)1–3. Even though the cut-off frequency is not the only important parameter in radio frequency (RF) MOSFETs, a high cut-off frequency certainly represents a good criterion for Si MOSFETs to catch up with III-V transistors if other shortcomings are overcome. Power losses due to a long skin depth of the Si substrate, a poor noise figure and a high gate resistance4 are the examples of such obstacles. Recently there have been tremendous efforts to improve the RF performance of the Si MOSFET and it is becoming competitive to III-V high electron mobility transistor (HEMT)/heterojunction bipolar transistor (HBT) or silicon germanium (SiGe) HBT2,3,5.

Silicon-on-insulator (SOI) multi-gate (MG) structures also have been found to be capable of achieving the cut-off frequency predicted by the international technology roadmap for semiconductors (ITRS)6 for RF applications while reducing substrate losses and noise figures5. Gate-all-around (GAA) silicon nanowire transistors (SiNWTs) have attracted attention since it was found that their cut-off frequency can be much larger than that of planar Si MOSFET8.

Traditionally, interface roughness scattering (IRS) has been considered as one of the most important scattering mechanisms. At a high effective electric field, IRS dominates the universal mobility trend10,11. In SiNWTs, IRS is still an important scattering mechanism reducing the on-current and the mobility significantly from the ballistic values11.

This paper focuses on the effects of interface roughness scattering on the RF performance of SiNWTs, especially on the cut-off frequency (fT). For that purpose, a three dimensional full-band quantum transport simulator based on the sp3d5s∗ tight-binding (TB) model12,13 is used. As the maximum oscillation frequency (fmax) – another important figure of merit of the RF MOSFETs is directly related to the cut-off frequency, the effects of IRS on the theoretical limit of the SiNWT’s RF performance can be estimated through this study.

The structure of the SiNWT studied in this paper is depicted in Fig. 1 where the oxide layer is described in the cross-sectional view. The model of the interface roughness is included in the figure.

FIG. 1. The simulated silicon nanowire with rough surface in the channel: the root-mean-square roughness height ∆rms and the correlation length Lm are adopted from Ref. 9. The crystal orientation (110) is selected for the electron transport direction. The source/drain doping density Ns/Nd is set to 5 × 1020 cm−3. The diameter of the nanowire dSi varies from 2, 2.5, 3 to 4 nm. The length of the source/drain extension region Ls/Ld, the gate length Lg, and the oxide thickness tox are shown in the figure. The channel of the nanowire is undoped.

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FIG. 2. (a) The cut-off frequency \( f_T \), (b) the transconductance \( g_{m,on} \), (c) the total gate capacitance \( C_{g,tot} \) vs diameter \( d_\text{Si} \) at the on-state with the gate bias \( V_{\text{gs}} \sim V_{\text{th}} + 0.4 \text{V} \) with the oxide capacitance \( C_{\text{ox}} = 2\pi e_{\text{ox}}/\ln[2(t_{\text{ox}} + d_\text{Si}/2)/d_\text{Si}] \) where \( e_{\text{ox}} \) is the dielectric constant of the oxide, and (d) the transconductance \( g_{m,on} \) vs gate overdrive for 100 rough nanowire samples (errorbar: standard deviation). All the values except \( f_T \) are normalized with the perimeter of the NW.

This is to first order a consequence of the improvement of the injection velocity in a \((110)\) silicon nanowire (SiNW) with smaller diameter\(^2\).

As shown in Fig. 2(b), the transconductance \( g_{m,on} \) is reduced significantly by the IRS while \( C_{g,tot} \) is not affected much (Fig. 2(c)). The reduction of \( g_{m,on} \) is due to reflections caused by the rough interface. A small dip in \( g_m \) marked by an arrow in Fig. 2(d) is an indication that the second subband starts to carry the current\(^6\). In rough NWs, this dip is smoothed out due to subband mixing.

Mismatch of the subbands throughout the channel of the rough nanowire also can be observed in Fig. 3(b). This causes reflections of electrons causing reduction of the electron velocity which, in turn, reduces the transconductance. Fig. 3(b) shows the electron velocity throughout the smooth NW and the rough NWs with the diameter 2 nm. The electron velocity is significantly reduced by interface roughness scattering.

One thing noticeable in Fig. 3(b) is that the IRS causes a reduction of the electron velocity at the beginning of the channel, but not much at the end of the channel. Electrons gain a relatively large kinetic energy due to a large electric field at the end of the channel. As a result, the fluctuation of the conduction band edge at the end of the channel does not affect the electron velocity significantly.

The cut-off frequency relationship (Eq. 1) can also be expressed as

\[
f_T = \frac{v_{\text{on}}}{2\pi L_g}.
\]

Therefore, the average electron velocity \( v_{\text{on}} \) can be calculated from the cut-off frequency. The transit time under the gate \( \tau_T \) is determined from \( v_{\text{on}}/L_g \), such that the average velocity is an effective velocity with which electrons flow in the channel when a small signal is applied to the gate. As shown in Fig. 3(a), it turns out that \( v_{\text{on}} \) is higher than the ballistic injection velocity (\( \sim 1.5 \times 10^7 \text{cm/s} \) from
It is found that the rough surface causes back-
tance due to volume inversion of carriers in a nanowire.

The total gate capacitance is reduced from the oxide capaci-
ter in the SiNW. Experimentally it is found that the
is close to the velocity in the middle of the channel.

Interface roughness causes mode mixing and additional
reflections in the current. It does, however, not mod-
ify the total density of states (DOS), and therefore the
capacitance of the nanowire. Therefore, the total gate
capacitance is relatively unaffected by rough interfaces.

In conclusion, the cut-off frequency of SiNWTs is sta-
tistically studied through quantum transport simulation
using a realistic modeling of the rough Si/SiO₂ inter-
face. It is found that the rough surface causes back-
scattering and reduces the velocity of electrons via modify-
ing the DOS in the channel. Mode-mismatch due to in-
terface roughness scattering reduces the overall transcon-
ductance, but does not significantly affect the total gate
capacitance. In addition to the cut-off frequency degra-
dation, its variability is another issue that should be ad-
dressed in RF SiNWTs.

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tional resources.

FIG. 4. (a) The average electron velocity at the on-state for
NWs with a different diameter and (b) the electron velocity
along the channel at the on-state for rough NWs with diam-
eter 2 nm (errorbar: standard deviation).

FIG. 5. The electron density from source to drain for (top) the
smooth NW and (bottom) the rough NW (the same sample
selected for Fig. 3) at the on-state with \( V_{gs} \sim V_{th} + 0.4V \).

Ref. 17) because electron velocity is not saturated in the
beginning of the channel as in a long channel transistors.
It can be observed that the average electron velocity \( v_{on} \)
is close to the velocity in the middle of the channel.

The total gate capacitance is also an important param-
eter in the SiNWT. Experimentally it is found that the
total gate capacitance is reduced from the oxide capaci-
tance due to volume inversion of carriers in a nanowire.\textsuperscript{22}

In the simulated NW, the total gate capacitance is found
using a realistic modeling of the rough Si/SiO₂ inter-
face. It can be observed that the electron density is fluctuating
throughout the channel as compared to the smooth NW.

FIG. 5(c) shows the electron density along the NW where
it can be observed that the electron density is fluctuating
throughout the channel as compared to the smooth NW.

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