Thermal analysis of interior defects in 3D-TSV based on thermoelectric coupling method

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Abstract. In order to understand the thermal effect of the defects in 3D-TSV interconnection structure, corresponding finite element models were established and thermal-electronic analysis was conducted. The temperature distributions of different layers of TSV structure with defects were investigated and the distribution variations due to the three common types of interior defects, which were filling missing, axial cavity and end cavity, were analysed respectively. The simulation results of defect-free TSV were also given for the sake of comparison. From the results, it was clear that all kinds of defects caused obvious variations of temperature distribution. And TSV with the filling missing problem had the most recognisable temperature distribution difference among those three typical defects. The defect of end cavity, followed by axial cavity, had less effect. Based on these conclusion, the temperature distribution supported important defect information by which the interior defect inspection and recognition could be realized.

1. Introduction
TSV (Through Silicon Via) was a promising technology by making vertical channel between wafers or chips to achieve interconnect [1]. It raised the device integration, reduced the interconnect delay and improved the operation speed. However, the interior defects in TSV could be hardly found by traditional method. If defective TSVs were integrated in device packaging, the failure risk of chip and device were raised sharply. Therefore, it was necessary to analyze the defect effect in the 3D-TSV package interconnect structure.

At present, the research of TSV with defects mainly focused on the thermodynamics, analysis of parasitic parameters and the electrical performance, etc. In 2017, Wang Shi Wei analyzed the diameter, height, spacing and the thickness of the BCB on thermal stress by variable parameters, reducing the thickness and height of BCB was an effective method to reduce the thermal stress of low resistance silicon and the possibility of defects generation [2]. In 2017, Pan Y. studied the influence of size parameters and defects on the thermal behavior of TSV package, and obtained the corresponding location, shape and size of defects on the temperature field [3]. In 2016, Shang Yu Ling established circuit models of TSV with defects by variable parameters, and recognized the corresponding TSV fault modes [4].

These researchers investigated the causes of interior defects in TSV and some of them discussed the relevant adverse effects on the packaging reliability and lifetime. However, the research of working state of TSV with defects was seldom found. Therefore, the relationship between external appearance and internal effect of TSV defect was still veiled. Since the temperature was almost the most obvious external appearance of TSV working state, the thermal-electric coupling finite element analysis was conducted to reveal the internal state of TSV with different defects.
In this regard, the finite element models of different TSVs (with and without defects) were established and corresponding thermal-electronic coupling analysis was conducted. The temperature field distribution was obtained and compared with the distribution of the temperature field of TSV without defects.

2. Modeling

2.1. Establishment and parameter design of TSV finite element model

According to the structure principle of 3D-TSV packaging, the model was simplified to facilitate the thermal analysis. The schematic diagram of this model of stacked TSV packaging was shown in Fig.1. The model structure, which consisted of chip layer, solder layer, TSV layer, TSV pillars, substrate layer, was shown in Fig.2. The feature size parameters of each part were as follows: chip layer and the TSV layer was $4 \text{ mm} \times 4 \text{ mm} \times 300 \mu \text{m}$, two solder layers was $4 \text{ mm} \times 4 \text{ mm} \times 100 \mu \text{m}$, the substrate was $7 \text{ mm} \times 7 \text{ mm} \times 300 \mu \text{m}$ and the radius of the copper pillar was $100 \mu \text{m}$. The material properties used in the finite element analysis were shown in Table1.

![Figure 1: Schematic diagram of TSV chip structure](image1.png)

![Figure 2: Each part of the module structure](image2.png)

Table1. Property parameters.

|                | Thermal conductivity [W/(m·K)] | Electrical resistivity (Ω·m) | Modulus of elasticity (E/GPa) | Poisson ratio | Specific heat capacity [J/(kg·℃)] | Density (kg/m³) |
|----------------|--------------------------------|------------------------------|-------------------------------|--------------|-----------------------------------|-----------------|
| **Copper cylinder** | 390                            | 1.75e-8                      | 117                           | 0.32         | 385                               | 8950            |
| **Silicon chip**   | 124                            | 1                            | 191                           | 0.28         | 700                               | 2330            |
| **Substrate**      | 0.3                            | 0.1                          | ---                           | ---          | ---                               | ---             |
| **Solder**         | 0.1                            | ---                          | ---                           | ---          | 700                               | 8740            |
| **TSV layer**      | 124                            | 0.1                          | ---                           | ---          | 700                               | 2330            |

2.2. Common defect types of TSV interconnection structure

In the process of TSV manufacturing, three types of defects usually arose, which were shown in Fig.3 as (a) filling missing (radius 100μm), (b) axial cavity (radius 80μm) and (c) end cavity (radius 80μm, height 100μm). All the defects located in the same pillar as indicated in Fig. 9. In order to uncover the influence of different defects and copper self-heating on the whole temperature field distribution. The working voltage of the 1.5V was applied to the upper surface of the chip layer. The boundary conditions of all models were following: the ambient temperature was $20^\circ \text{C}$, convective heat transfer coefficient was $15 \text{ W/m}^2\cdot^\circ\text{C}$.
3. Results and discussion

3.1. The temperature distribution of the chip layer and TSV layer under various defects

Figure 3. Common defect profiles of TSV interconnect structure

(a) Temperature distribution of the chip layer with defect-free TSV

(b) Temperature distribution of the chip layers with filling pillars missing

(c) The temperature distribution of the chip layer under the axial cavity

(d) Temperature distribution of chip layer under the end cavity

Figure 4. The temperature distribution of the chip layer under various defects
The simulation results of chip and TSV layer was shown in Fig. 4 and Fig. 5 respectively. It is obvious the temperature distribution of each layer was transferred from the center to the periphery, and the lowest temperature was located at the upper right corner of the chip layer. However, under the same working voltage load, the highest temperature 113.091℃ was found in Fig.4(b) which was the result of filling missing defect. In contrast, the chip layer temperature of the end cavity defect was lowest (97.109℃) as shown in Fig.4(d). From Fig.5, it was easily found that the temperature of the TSV layer with filling missing defect was the highest, 113.082℃ in Fig.5(b). The lowest temperature was 97.105℃ in Fig.5(d) which presented the result of end cavity defect.

3.2. Selecting the path and observing the change of the temperature under each defect

The simulation results of chip and TSV layer was shown in Fig. 4 and Fig. 5 respectively. It is obvious the temperature distribution of each layer was transferred from the center to the periphery, and the lowest temperature was located at the upper right corner of the chip layer. However, under the same working voltage load, the highest temperature 113.091℃ was found in Fig.4(b) which was the result of filling missing defect. In contrast, the chip layer temperature of the end cavity defect was lowest (97.109℃) as shown in Fig.4(d). From Fig.5, it was easily found that the temperature of the TSV layer with filling missing defect was the highest, 113.082℃ in Fig.5(b). The lowest temperature was 97.105℃ in Fig.5(d) which presented the result of end cavity defect.
As seen from Fig. 6, an observation path was defined from point A to point B on the TSV layer. It was clear that the temperature profile of various defects was different from that of TSV without defects (Fig. 7). Furthermore, the highest peak temperature 112.937°C was found caused by pillars missing defect and the lowest temperature was 97.101°C which presented the result of the end cavity defect as shown in Fig. 7(b) and Fig. 7(d) respectively.

4. Result discussion
Based on the thermoelectric coupling analysis of the three typical TSV defects, it could be concluded that:

1. The TSV with the filling missing problem had the most recognizable temperature distribution difference among those three typical defects. And the defect of end cavity, followed by axial cavity, had less effect.
2. Since the influence of the TSV pillar heating was considered, under the same voltage load, heating power of different types of defects induced various temperature distribution.
3. The temperature profile difference in TSV layer was very significant, which could provide theoretical guidance for subsequent TSV defect recognition and detection.

5. Conclusion
According to the common defect types of TSV interconnect structure, the working state finite element models were established and thermal-electronic analysis was conducted. The analysis results were compared with that of defect-free TSV. From the result, it was undoubted that the TSV with filling missing defect showed the most obvious temperature distribution difference among all kinds of defects. In other word, this kind defect applied very severe influence on TSV working state. The effects of other two kinds of defect were weaker relatively. Therefore, the monitoring of temperature distribution in TSV packaging was a reasonable method to realize TSV interior defect inspection and recognition.
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