Three-Phase Interleaved LLC Asymmetric Resonant Converter With Capacitive Current Balancing and Reduced Switch Voltage Stress

YOSHIYA TADA¹, (Student Member, IEEE), MASATOSHI UNO², (Member, IEEE), AND YUSUKE SATO²

¹Graduate School of Science and Engineering, Ibaraki University, Hitachi 316-8511, Japan
²Panasonic Corporation, Yokohama 224-8520, Japan

Corresponding author: Masatoshi Uno (masatoshi.uno.ee@vc.ibaraki.ac.jp)

ABSTRACT Interleaved converters are a typical solution to enhance a current capacity and to reduce current ripples of an input or output port. Conventional interleaved LLC resonant converters need additional switches and passive components with a feedback control loop for active current balancing, increasing the circuit complexity and cost. This paper proposes a novel three-phase interleaved LLC resonant converter with an automatic capacitive current balancing capability. Two flying capacitors are added to a conventional interleaved LLC resonant converter in order to realize not only the automatic capacitive current balancing but also the reduced switch voltage stresses and asymmetric resonant operations that contribute to reducing rms currents as well as copper losses of transformers. The detailed operation analysis, including the capacitive current balancing mechanism and gain characteristics derivation, are performed. The experimental verification using a 1-kW prototype demonstrated that the automatic capacitive current balancing could be achieved despite the significant mismatch in transformers’ parameters.

INDEX TERMS Asymmetric resonance, current balancing, flying capacitor, interleaved converter, LLC resonant converter.

I. INTRODUCTION

Interleaved converters consisting of parallel-connected multiple converters operating out of phase at the same frequency are widely used to enhance a current capacity and to reduce current ripples of an input or output port. Gain characteristics of parallel-connected phases are naturally mismatched to a certain degree due to component tolerance. Currents flowing through each phase (hereafter call ‘phase currents’) are imbalanced due to the gain characteristic mismatch, causing a current concentration and increased current stresses. To balance phase currents in the interleaved PWM converters, all phase currents are measured, and a duty cycle of each phase is individually adjusted so that the gain characteristics of parallel-connected phases are matched [1]. This active current balancing technique, however, requires not only multiple current sensors but also an additional current balancing feedback control loops, resulting in increased circuit complexity and cost.

A previous work [2] has proposed an automatic current balancing technique based on a magnetic coupling. Topologies employing a magnetic coupling for the current balancing are prone to be bulky due to a large number of magnetic components. An interleaved PWM buck and boost converters presented in [3], [4] realize an automatic capacitive current balancing thanks to the charge conservation of dc blocking capacitors. In this interleaved buck converter, the number of phases can be extended without impairing the automatic current balancing capability.

Meanwhile, LLC resonant converters offer prominent features of galvanic isolation, high efficiency, high-power density, and reduced switching loss and EMI thanks to zero voltage switching (ZVS) operations. In general, gain characteristics of LLC resonant converters are dependent on their frequency-dependent impedance characteristics, suggesting that switching frequencies of parallel-connected LLC resonant converters need to be individually adjusted...
to balance phase currents. Alternatively phrased, parallel-connected LLC resonant converters eventually operate at different switching frequencies [5], [6], and therefore, interleaving operations cannot be simply applied to LLC resonant converters.

Several interleaved LLC resonant converters with active current balancing techniques have been proposed [7]–[9]. The interleaved LLC resonant converter presented in [7] adds variable inductors in order to compensate gain characteristic mismatches. Topologies proposed in [8] and [9] adjust parasitic capacitances of MOSFETs by controlling their switching frequencies, but the slight mismatch in a resonant capacitor (e.g., 5%) reportedly results in the existence of phases no longer contributing to power conversion. In general, interleaved LLC resonant converters with an active current balancing are prone to be complex and costly due to additional feedback control loops and current sensors for the active current balancing.

The multi-phase LLC resonant converters presented in [10]–[13], on the other hand, achieve a passive current balancing without additional feedback control loops nor current sensors, but there are still challenges to be addressed. Topology reported in [10] cannot achieve adequate current balancing if the transformers’ parameters are mismatched. The interleaved LLC resonant converter employing common inductors tends to suffer from a current imbalance under light load conditions [11]. The three-phase interleaved LLC resonant converter developed in [12] automatically balances three-phase currents by utilizing an integrated transformer and current balancing transformer. However, the existence of the integrated transformer not only increases its design difficulty but also impairs the LLC resonant converters’ advantage of the simple structure. Meanwhile, the two-phase interleaved LLC resonant converter [13] achieves an automatic capacitive current balancing thanks to the charge conservation of a capacitor even under light load conditions, but output current ripples cannot be reduced even with the interleaving structure. In addition, a three-phase LLC resonant converter topology with capacitive current balancing has not been proposed yet.

This paper proposes a novel three-phase interleaved LLC resonant converter with an automatic capacitive current balancing capability. Two flying capacitors are added to a conventional three-phase LLC resonant converter to realize not only the automatic capacitive current balancing but also reduced switch voltage stresses. In addition, the added flying capacitors achieve asymmetric resonant operations, by which rms currents of resonant tanks in the case of asymmetric duty cycles $d \neq 0.5$ can be reduced.

This paper is organized as follows. Section II introduces the proposed three-phase interleaved LLC asymmetric resonant converter and its major features. Section III explains the mechanisms of the automatic capacitive current balancing and asymmetric resonant operation. The operation analysis, switch voltage stress, and gain characteristics will be discussed in detail in Section IV. The experimental verification using a 1-kW prototype will be presented in Section V.
The proposed interleaved LLC converter adopts the asymmetric resonant operation by employing $C_1$ and $C_2$ for resonance. The asymmetric resonant operation reduces rms current as well as Joule losses of components and copper losses of the transformers compared with those in the conventional interleaved LLC converter operating with the symmetric resonance.

The number of phases in the proposed interleaved converter can be extended to increase the current capacity of the converter. However, capacitances of flying capacitors need to be properly designed to achieve the asymmetric resonant operations, resulting in increased design difficulty of the resonant tanks compared with the ordinary LLC resonant converters, as will be detailed in Section III-B. Given the design difficulty of the asymmetric resonant tanks in extended topologies, three- or four-phase topologies would be the practical implementation of the proposed interleaved LLC converter.

Similar to the ordinary LLC resonant converters, the output voltage of the proposed converter is regulated by pulse frequency modulation (PFM) control. All switches in the proposed converter achieve ZVS turn-on and -off by utilizing magnetizing inductances of transformers, $L_{mgi}$, and parasitic capacitances of MOSFETs, $C_{OSS}$. All the diodes on the transformers’ secondary side achieve zero current switching (ZCS) turn-on and -off.

Since the proposed converter operates with the asymmetric duty cycle of $d \neq 0.5$, dc blocking capacitors of $C_{bj}$ are necessary to prevent magnetic saturation of the transformer.

\[ \text{FIGURE 2. Concept of extension for multi-phase interleaved LLC resonant converter.} \]

C. EXTENSION TO MULTIPLE PHASE

The concept of the proposed interleaved LLC converter can be extended to arbitrary numbers of phases. The generalized concept of the proposed multi-phase interleaved converter is shown in Fig. 2. The transformers’ secondary sides are not illustrated for the sake of clarity. The number of phases can be arbitrarily increased by adding the circuit consisting of a resonant tank, two switches, and a flying capacitor. Extended topologies of the multi-phase interleaved LLC converter also achieves an automatic current balancing, reduced switches’ voltage stresses, and asymmetric resonant operations thanks to the flying capacitors.

Resonant frequencies need to be properly designed with considering asymmetric duty cycles, as will be explained in the next section. Let $n$ be the number of phases, duty cycles $d$ of high-side switches are $1/n$. Therefore, the larger the number of phases, the smaller will be the duty cycles, resulting in increased design difficulties of asymmetric resonant frequencies. Accordingly, three- or four-phase topologies would be practical from the viewpoint of design difficulty.

\[ \text{FIGURE 3. Current flows in (a) Phase A, (b) Phase B, and (c) Phase C.} \]

III. AUTOMATIC CAPACITIVE CURRENT BALANCING AND ASYMMETRIC RESONANT OPERATION

A. AUTOMATIC CAPACITIVE CURRENT BALANCING

The proposed converter offers an automatic current balancing owing to the charge conservation of flying capacitors of $C_1$ and $C_2$. The current flows in each phase are highlighted in Fig. 3. As shown in Fig. 3(a), during the period when $i_A$ is positive, $C_1$ and $C_{A1}$ in the resonant tank of Phase A are charged in series. In the period when $C_1$ is discharging, $C_2$ and $C_{B1}$ in the resonant tank of Phase B are charged in series by $C_1$, as shown in Fig. 3(b). In summary, $C_1$ is charged together with $C_{A1}$ of Phase A, and $C_1$ discharges to $C_2$ and $C_{B1}$ of Phase B. Therefore, the phase currents of $i_A$ and $i_B$ are automatically balanced by the charge conservation of $C_1$. After $C_2$ is charged with $C_{B1}$ in the resonant tank of Phase B, $C_2$ discharges to $C_{C1}$ in the resonant tank of Phase C, as illustrated in Fig. 3(c). Hence, the phase currents of $i_B$ and $i_C$ are naturally balanced by $C_2$. Consequently, all phase currents are automatically balanced thanks to $C_1$ and $C_2$ even if component parameters are mismatched.

B. ASYMMETRIC RESONANT OPERATION

In general, to improve the power conversion efficiency of traditional LLC converters operating with a symmetric duty cycle of $d = 0.5$, rms currents at a given output power need to be minimized with ensuring ZVS operations. To this end, the resonant period $1/f_r$ is set to be slightly shorter than the switching period $T_S$. The proposed interleaved LLC converter, on the other hand, operates with an asymmetric
duty cycle of \( d = 0.33 \) for high-side switches, and hence, positive and negative half resonant periods, \( 1/2f_P \) and \( 1/2f_N \), must be shorter than \( T_S/3 \) and \( 2T_S/3 \), respectively.

\[
f_{rAP} = \frac{1}{2\pi \sqrt{L_{kgA} C_{rA}}} \quad (1)
\]

\[
f_{rBP} = \frac{1}{2\pi \sqrt{L_{kgB} C_{rB}}} \quad (2)
\]

\[
f_{rBN} = \frac{1}{2\pi \sqrt{L_{kgC} C_{rB}}} \quad (3)
\]

\[
f_{rCP} = \frac{1}{2\pi \sqrt{L_{kgC} C_{rC}}} \quad (4)
\]

\[
f_{rCN} = \frac{1}{2\pi \sqrt{L_{kgC} C_{rC}}} \quad (5)
\]

\[
f_{rAN} - f_{rCN} \quad (6)
\]

FIGURE 4. Current waveforms of symmetric and asymmetric LLC resonances.

Figure 4 compares the current waveforms of the symmetric and asymmetric resonant operations with \( d = 0.33 \). The resonant frequencies of the positive half cycle are identical. In the negative half cycle, the negative peak current of the asymmetric resonance is reduced compared with that of the symmetric resonance. Thus, the asymmetric resonant operations can lower negative peak currents, reducing rms currents as well as conduction losses.

As shown in Fig. 3, in the positive half cycle of resonance, not only the resonant tanks but also the flying capacitors of \( C_1 \) and \( C_2 \) take part in the resonant operations. The resonant frequencies of positive and negative half cycles of Phases A–C, \( f_{rAP} - f_{rCP} \) and \( f_{rAN} - f_{rCN} \), are expressed as

\[
f_{rAP} = \frac{1}{2\pi \sqrt{L_{kgA} C_{rA}}} \quad (1)
\]

\[
f_{rBP} = \frac{1}{2\pi \sqrt{L_{kgB} C_{rB}}} \quad (2)
\]

\[
f_{rBN} = \frac{1}{2\pi \sqrt{L_{kgC} C_{rB}}} \quad (3)
\]

\[
f_{rCP} = \frac{1}{2\pi \sqrt{L_{kgC} C_{rC}}} \quad (4)
\]

\[
f_{rCN} = \frac{1}{2\pi \sqrt{L_{kgC} C_{rC}}} \quad (5)
\]

\[
f_{rAN} - f_{rCN} \quad (6)
\]

\[
f_{rAN} - f_{rCN} \quad (6)
\]

\[
f_{rAN} - f_{rCN} \quad (6)
\]

\[
f_{rAN} - f_{rCN} \quad (6)
\]

\[
f_{rAN} - f_{rCN} \quad (6)
\]
tank of Phase A are charged in series with \( C_{tA} \). The charge stored in \( C_1 \) and \( C_A \) in this mode is designated as \( q_A \) (see Fig. 5). The voltages across \( Q_{AL} \), \( Q_{BH} \), and \( Q_{CH} \) are yielded as

\[
\begin{align*}
v_{QAL} &= V_{in} - V_{C1} \quad (10) \\
v_{QBH} &= V_{in} - V_{C2} \quad (11) \\
v_{QCH} &= V_{C2}. \quad (12)
\end{align*}
\]

Mode 2 [Fig. 6(b)]: Phases A and C operate in negative half cycles, while Phase B in the positive half cycles. In Phase B, both \( C_1 \) and \( C_2 \) take part in the resonant operation. The amount of charge stored in \( C_2 \) and \( C_{B} \) designated as \( q_B \) (see Fig. 5) must be equal to \( q_A \) because of the charge conservation of \( C_1 \). Consequently, currents of Phases A and B, \( i_A \) and \( i_N \), are automatically balanced. The voltage stresses of \( Q_{AH} \), \( Q_{BL} \), and \( Q_{CH} \) are expressed as

\[
\begin{align*}
v_{QAH} &= V_{in} - V_{C1} \quad (13) \\
v_{QBL} &= V_{C1} - V_{C2} \quad (14) \\
v_{QCH} &= V_{C1}. \quad (15)
\end{align*}
\]

Mode 3 [Fig. 6(c)]: Phases A and B are in negative half cycles, while Phase C is in a positive half cycle. \( C_2 \) participates in the resonant operation of Phase C. The released charge amount of \( C_2 \), \( q_C \), must be equal to \( q_B \), resulting in an automatic current balancing between Phases B and C. The voltages across \( Q_{AH} \), \( Q_{BH} \), and \( Q_{CL} \) can be expressed as

\[
\begin{align*}
v_{QAH} &= V_{in} - V_{C1} \quad (16) \\
v_{QBH} &= V_{C1} - V_{C2} \quad (17) \\
v_{QCL} &= V_{C2}. \quad (18)
\end{align*}
\]

The resonant tanks of Phases A–C are assumed identical, and they operate with the same duty cycles of \( d = 0.33 \). The voltages applied to resonant tanks of Phases A–C are equivalent to the low-side switch voltages obtained in (10), (14), and (18), respectively. Hence, average voltages of the resonant tank (or resonant capacitor) of each phase, \( V_{rA} \) to \( V_{rC} \), are expressed as

\[
\begin{align*}
V_{rA} &= (V_{in} - V_{C1})/3 \quad (19) \\
V_{rB} &= (V_{C1} - V_{C2})/3 \quad (20) \\
V_{rC} &= V_{C2}/3. \quad (21)
\end{align*}
\]

Switch voltage stresses in the proposed interleaved LLC resonant converter are one-third or two-third of \( V_{in} \), whereas those in traditional LLC resonant converters are \( V_{in} \). The reduced voltage stresses translate to lowered on-resistances of MOSFETs as well as reduced conduction losses.

C. GAIN CHARACTERISTICS

First harmonic approximation (FHA) is a widely used method to briefly analyze the gain characteristics of LLC resonant converters [14, 15]. However, FHA cannot be applied to the proposed interleaved LLC converter due to asymmetric duty cycles and asymmetric resonant operations. This section reveals the gain characteristics of the proposed converter by applying the time-domain analysis [16, 17]. As discussed in Section III-B, \( f_P \) and \( f_N \) are preferably designed to be \( f_P : f_N = 2 : 1 \) because the proposed converter operates with the asymmetric duty cycle \( d = 0.33 \). However, to derive the universal gain characteristics, the time-domain analysis under the condition of \( f_{AP} : f_{AN} \neq 2 : 1 \) is performed in this section.

The time-domain analysis is performed based on the following premises in order to simplify the analysis. All the circuit elements are ideal. \( V_{C1} \) and \( V_{C2} \), and voltages across the dc blocking capacitors on the transformers’ secondary sides, \( V_{CB} \) and \( V_{CNC} \), are constant. In this paper, the time-domain analysis for Phase A only is performed to save the page length, but Phases B and C can be analyzed in the same manner.

The voltage of \( C_{tA} \), \( V_{CtA} \), and \( I_{LmgA} \), and the current flowing through the secondary winding, \( i_{SA} \), are highlighted in Fig. 7.
The characteristic impedance, \( Z_r \), is defined as

\[
Z_r = \sqrt{\frac{L_{kgA}}{C_{RA}}}. \tag{27}
\]

**Period 1** (\( T \leq t \leq T_1 \)) [Fig. 8(a)]: \( C_1, \ C_{tA}, \) and \( L_{kgA} \) resonate. \( i_A \) sinusoidally changes, whereas \( i_{LmgA} \) linearly increases. \( v_{CRA}, \ i_A, \) and \( i_{LmgA} \) are yielded as

\[
v_{CRA} (t) = \{v_{CRA} (T_0) - V_{in} + V_{C1} + n_A (V_{CBA} + V_{out})\}
\cdot \cos(\omega_{rAP} (t - T_0)) + i_A (T_0) Z_r \sin(\omega_{rAP} (t - T_0)) + V_{in} - V_{C1} - n_A (V_{CBA} + V_{out}) \tag{28}
\]

\[
i_A (t) = i_A (T_0) \cos(\omega_{rAP} (t - T_0)) - \frac{v_{CRA} (T_0) - V_{in} + V_{C1} + n_A (V_{CBA} + V_{out})}{Z_r} \sin(\omega_{rAP} (t - T_0)) \tag{29}
\]

\[
i_{LmgA} (t) = \frac{n_A (V_{CBA} + V_{out}) - (t - T_0) + i_A (T_0)}{L_{mgA}} \tag{30}
\]

where \( \omega_{rAP} = 2\pi f_{rAP} \).

**Period 2** (\( T_1 \leq t \leq T_2 \)) [Fig. 8(b)]: \( L_{mgA} \) takes part in the resonance. \( i_A \) increases together with \( i_{LmgA} \). \( v_{CRA}, \ i_A, \) and \( i_{LmgA} \) are expressed as

\[
v_{CRA} (t) = \{v_{CRA} (T_1) - V_{in} + V_{C1}\} \cos(\omega_{mAP} (t - T_1)) + i_A (T_1) Z_r \sin(\omega_{mAP} (t - T_1)) + V_{in} - V_{C1} \tag{31}
\]

\[
i_A (t) = i_A (T_1) \cos(\omega_{mAP} (t - T_1)) - \frac{v_{CRA} (T_1) - V_{in} + V_{C1}}{Z_r} \sin(\omega_{mAP} (t - T_1)) \tag{32}
\]

\[
i_{LmgA} (t) = i_A (t) \tag{33}
\]

where \( m = L_{mgA}/L_{kgA} \), and \( \omega_{mAP} = \omega_{rAP}/\sqrt{1 + m} \).

**Period 3** (\( T_2 \leq t \leq T_3 \)) [Fig. 8(c)]: \( C_{tA} \) and \( L_{kgA} \) are resonating. \( i_A \) sinusoidally changes, and \( i_{LmgA} \) linearly decreases. \( v_{CRA}, \ i_A, \) and \( i_{LmgA} \) are expressed as

\[
v_{CRA} (t) = \{v_{CRA} (T_2) + n_A (V_{CBA} - V_{out})\} \cos(\omega_{rAN} (t - T_2)) + i_A (T_2) Z_r \sin(\omega_{rAN} (t - T_2)) \tag{34}
\]

\[
i_A (t) = i_A (T_2) \cos(\omega_{rAN} (t - T_2)) - n_A (V_{CBA} - V_{out}) \tag{35}
\]

\[
i_{LmgA} (t) = \frac{n_A (V_{CBA} - V_{out})}{L_{mgA}} (t - T_2) + i_A (T_2) \tag{36}
\]

where \( \omega_{rAN} = 2\pi f_{rAN} \).

One switching cycle is subdivided into four periods, and equivalent circuits of Phase A in each period are illustrated in Fig. 8. Before detailing the gain characteristic analysis, \( V_{CBA} \) is derived. The voltage across \( L_{mgA} \) in Periods 1–4 is yielded as

\[
v_{Lmg} = \begin{cases} n_A (V_{CBA} + V_{out}) & \text{(Period 1)} \\ V_{in} - V_{C1} - V_{CRA,ave2} & \text{(Period 2)} \\ n_A (V_{CBA} - V_{out}) & \text{(Period 3)} \\ V_{CRA,ave4} & \text{(Period 4)} \end{cases} \tag{24}
\]

where \( V_{CRA,ave2} \) and \( V_{CRA,ave4} \) are the average voltages of \( C_{RA} \) in Periods 2 and 4, respectively. Equation (25), as shown at the bottom of this page, is derived from the volt-second balance on \( L_{mgA} \), and \( V_{CBA} \) can be obtained as (26), as shown at the bottom of this page.
TABLE 1. Component values used for gain characteristics analysis.

| Components          | Value |
|---------------------|-------|
| $C_1$ and $C_2$     | 1.0 µF |
| $C_{CA} - C_{GC}$   | 680 nF |
| $L_{mgA} - L_{mgC}$ | 2.0 µH |
| $r_{r-c}$           | 30 µH  |
| $f_{CP}$            | $f_{AP} = 177$ kHz, $f_{AP} = 210$ kHz, $f_{CP} = 177$ kHz |
| $f_{AN}$            | $f_{AN} = 136$ kHz, $f_{AN} = 136$ kHz, $f_{AN} = 136$ kHz |

Period 4 ($T_3 \leq t \leq T_4$) [Fig. 8(d)]: $L_{mgA}$ participates in the resonance. Similar to Period 2, $i_A$ sinusoidally changes together with $i_{mgA}$, $v_{CA}$, $i_A$, and $i_{mgA}$ are given by

$$v_{CA}(t) = v_{CA}(T_3) + i_A(T_3)Z_r\sqrt{1 + m}\sin{\omega_{mAN}(t - T_3)}$$

$$i_A(t) = i_A(T_3)\cos{\omega_{mAN}(t - T_3)} - \frac{v_{CA}(T_3)}{Z_r\sqrt{1 + m}}\sin{\omega_{mAN}(t - T_3)}$$

$$i_{mgA}(t) = i_A(t)$$

where $\omega_{mAN} = \omega_{mAN}/\sqrt{1 + m}$.

As discussed in Section III-B, the resonant frequency of the positive half cycle of Phase B (i.e., $f_{RP}$) differs from those of Phases A and C ($f_{AP} = f_{AP} = f_{CP}$). The time-domain equations for Phase B can be obtained and expressed in a similar way as (24)–(39).

Assuming Phases A and C have the identical characteristics, the gain $G$ of the proposed three-phase interleaved LLC converter is derived as

$$G = \frac{n_AV_{out}}{V_{in}} = \frac{n^2_AR_{out}}{V_{in}T_S} \left(2\int_0^{T_3} |i_A - i_{mgA}| dt + \int_0^{T_3} |i_B - i_{mgB}| dt \right)$$

where $R_{out}$ is the load resistance, and $T_S (= 1/f_S)$ is the switching period.

Theoretical and simulated characteristics of $G$ are compared in Fig. 9, and component values used for the analysis are listed in Table 1. The normalized frequency $F$ and quality factor $Q$ are defined as

$$F = \frac{f_S}{f_{AN}}$$

$$Q = \frac{\pi^2 \cdot Z_r}{8n^2_A \cdot R_{out}}$$

In general, $G$ of conventional half-bridge LLC converters converges to 0.5 at normalized frequency $F = 1.0$. Meanwhile, $G$ of the proposed interleaved converter ideally converges to 0.167 when $C_1$ and $C_2$ are designed to be $f_{AP} : f_{AN} = 2 : 1$ because $V_{C1}$ is $2V_{in}/3$, as discussed in Section IV-B. However, $G$ in Fig. 9 converged to 0.17 at $F = 0.9$ because $C_1$ and $C_2$ were chosen so that $f_{AP}/f_{AN} < 2$ in this analysis.

Theoretical and simulated characteristics agreed satisfactorily, but there were slight mismatches observed in the low-frequency region. These mismatches were due to the discrepancy between the ideal analysis and reality. The analysis was performed assuming that $V_{C1}$ and $V_{C2}$ are constant. In reality, however, $V_{C1}$ and $V_{C2}$ fluctuate to some extent due to the resonant operations. Thus, the theoretical gain characteristics slightly differed from the simulated ones. Hence, the simulation-based analysis is recommended to reinforce the theoretical analysis if precise gain characteristics in the entire frequency region are required.

The resonant tanks must be designed to ensure the gain requirement even if the input voltage fluctuates. An ordinary PFM feedback control system, similar to that for ordinary LLC converters, can regulate the output voltage.

V. EXPERIMENTAL RESULTS

A. PROTOTYPE

A 1-kW prototype was designed and built for $V_{in} = 400$ V and $V_{out} = 48$ V, as shown in Fig. 10, and its component values are listed in Table 2. The resistances of primary and secondary windings, $r_{primary,j}$ and $r_{secondary,j}$, were measured by the frequency response analyzer (FRA5087, NF Corporation, Japan), and measured resistances at 106 kHz are shown in Table 2. As discussed in Section III-B, the three transformers $Tr_{A \rightarrow TC}$ are preferably designed so that their parameters are matched to equalize peak currents of Phases A–C and to achieve high efficiency power conversion. In this paper, however, to verify the automatic capacitive current balancing capability, $Tr_{A \rightarrow TC}$ were designed so that their key parameters of $L_{mgj}, L_{kgj}$, and $n_j$ were intentionally severely mismatched.

Experiments with symmetric resonant operations were also performed to demonstrate the reduced conduction losses by the asymmetric resonant operations. $C_1$ and $C_2$ were replaced with ceramic capacitors with a capacitance of 4.4 µF so that these capacitors did not take part in resonant operations.

B. MEASURED WAVEFORMS

Measured currents of the primary windings, secondary windings, and an output port under the asymmetric resonant
A three-phase interleaved LLC asymmetric resonant converter is described. Table 2 lists the component values. Figure 10 shows the photographs of a 1-kW prototype: (a) front side and (b) rear side. Operations at 1 kW and \( f_S = 106 \) kHz are shown in Figs. 11(a), (b), and (c), respectively. Despite the severely mismatched transformer parameters, the primary phase currents were automatically balanced, as shown in Fig. 11(a). The secondary phase currents, on the other hand, were slightly imbalanced due to the mismatch of each transformer’s turn ratio, as shown in Fig. 11(b).

Figure 12 shows the measured current waveforms under the symmetric resonant operations at 1 kW and \( f_S = 145 \) kHz. The peak currents of the positive and negative half cycles of resonant tanks were nearly identical in the symmetric resonance, as shown in Figs. 12(a) and (b). With the asymmetric resonance [see Figs. 11(a) and (b)], on the other hand, the peak currents of the negative half-cycles were lower than those of the positive half cycles, reducing rms currents at a given output power.
Measured voltage waveforms of the high- and low-sides switches at a full load of 1 kW under the asymmetric resonant operations are shown in Figs. 13(a) and (b), respectively. $v_{QBH}$ and $v_{QCH}$ were suppressed to around two-third of the input voltage, thanks to $C_1$ and $C_2$, as discussed in Section IV-B. Peak values of $v_{QAH}$, $v_{QAL}$, $v_{QBL}$, and $v_{QCL}$ were suppressed to approximately one-third of $V_{in}$, though they slightly exceeded the theoretical values due to the resonances of $C_1$ and $C_2$.

Drain-source and gate-source voltages of the switches, $v_{ds}$ and $v_{gs}$, at a full load of 1 kW under the asymmetric resonant operations are shown in Fig. 14. $v_{gs}$ was applied after $v_{ds}$ declined to zero, verifying ZVS turn-on for all switches. ZVS turn-off operations for all switches were also confirmed as $v_{ds}$ rose with moderate $dv/dt$ slope after $v_{gs}$ dropped to zero.

C. AUTOMATIC CAPACITIVE CURRENT BALANCING

From the measured phase currents of the primary windings $i_A–i_C$, the averaged phase currents $I_A–I_C$ were calculated from the following equation

$$I_j = \frac{1}{T_S} \int_0^{T_S} |i_j(t)| dt \quad (43)$$

where $j$ is A, B, or C.

The calculated $I_A–I_C$ are shown in Fig. 15. Despite the severe mismatch in the transformers’ parameters, $I_A–I_C$ were automatically balanced with errors less than 2% over the entire output power range.

D. POWER CONVERSION EFFICIENCY

The measured and calculated power conversion efficiencies of the asymmetric and symmetric resonance are compared in Fig. 16. The peak efficiency of the symmetric resonance was as high as 92.4% at 700 W, and the full-load efficiency at 1 kW was 91.6%. With the asymmetric resonance, the efficiencies increased because of the lower rms values of $i_A–i_C$ as well as reduced Joule losses. The full-load efficiency at 1 kW increased to as high as 93.1%, and the peak efficiency was 94.0% at 600 W.

The calculated power conversion efficiencies agreed very well with the measured ones, verifying the estimated loss breakdowns that will be shown in the next subsection.

E. LOSS ANALYSIS

Detailed loss breakdowns of the proposed interleaved LLC converter with the asymmetric or symmetric resonant operations were theoretically calculated. Figures 17(a) and (b) compare the estimated loss breakdowns at 500 W and 1 kW, respectively. Switching losses were assumed to be negligibly small due to ZVS operations over the entire output power range. Gate driving losses were excluded from these loss
breakdowns since an auxiliary power supply drove the gate drivers. Iron losses of the transformers were experimentally measured and were obtained from no-load losses of the prototype.

It should be noted that there were slight differences in iron losses of the asymmetric and symmetric resonance because the switching frequency \( f_S \) slightly differed even at the same output power. To be specific, \( f_S \) of asymmetric resonant operations at 500 W and 1 kW were 123 and 106 kHz, respectively, whereas that of the symmetric resonant operations were 165 and 145 kHz.

The asymmetric resonant operation significantly reduced the Joule losses, especially the primary and secondary windings of the transformers (i.e., copper losses). Under both resonant operations, power losses in \( C_1 \) and \( C_2 \) were negligibly small—the total loss in \( C_1 \) and \( C_2 \) was merely around 0.1 W at 1 kW.

Diode conduction losses were the dominant factors in both conditions of 500 W and 1 kW. Therefore, reducing the diode count by employing center-tapped transformers or synchronous rectifiers would effectively improve the efficiencies over the entire power range.

VI. CONCLUSION

This paper has proposed the three-phase interleaved LLC resonant converter with an automatic capacitive current balancing capability. Phase currents are automatically balanced by the flying capacitors without using current sensors nor feedback control loops, achieving the reduced circuit complexity and cost. The flying capacitors also contribute to lowering switches’ voltage stresses. Furthermore, the proposed asymmetric resonant operations utilizing flying capacitors can reduce Joule losses of circuit components and copper losses of transformers.

The experimental verification using the 1-kW prototype demonstrated the automatic capacitive current balancing capability even with the severe mismatch in the transformers’ parameters. The power conversion efficiency was improved thanks to the proposed asymmetric resonant operations compared to that of the symmetric ones.

REFERENCES

[1] H.-C. Chen, C.-Y. Lu, and U. S. Rout, “Decoupled master–slave current balancing control for three–phase interleaved boost converters,” IEEE Trans. Power Electron., vol. 33, no. 5, pp. 3683–3687, May 2018.
[2] K. I. Hwu and Y. H. Chen, “Applying differential–mode transformer to current sharing with current ripple considered,” IEEE Trans. Ind. Electron., vol. 58, no. 7, pp. 2755–2771, Jul. 2011.
[3] K. I. Hwu, W. Z. Jiang, and P. Y. Wu, “An expandable four–phase interleaved high step–down converter with low switch voltage stress and automatic uniform current sharing,” IEEE Trans. Ind. Electron., vol. 63, no. 10, pp. 6064–6072, Oct. 2016.
[4] M. Uno, M. Inoue, Y. Sato, and H. Nagata, “Bidirectional interleaved PWM converter with high voltage–conversion ratio and automatic current balancing capability for single–cell battery power system in small scientific satellites,” Energies, vol. 11, no. 10, p. 2702, Oct. 2018.
[5] G. Yang, P. Dubus, and D. Sadaranc, “Double–phase high–efficiency, wide load range high– voltage/low–voltage LLC DC/DC converter for electric/hybrid vehicles,” IEEE Trans. Power Electron., vol. 30, no. 4, pp. 1876–1886, Apr. 2015.
[6] M. Noah, S. Kimura, J. Imaoka, W. Martinez, S. Endo, M. Yamamoto, and K. Umetsu, “Magnetic design and experimental evaluation of a commercially available single integrated transformer in three–phase llc resonant converter,” IEEE Trans. Ind. Applicat., vol. 54, no. 6, pp. 6190–6204, Nov. 2018.
[7] E. Orietti, P. Mattavelli, G. Spiazzi, C. Adragna, and G. Gattavari, “Two–phase interleaved LLC resonant converter with current–controlled inductor,” in Proc. Brazilian Power Electron. Conf., Sep. 2009, pp. 298–304.
[8] Z. Hu, Y. Qiu, L. Wang, and Y.-F. Liu, “An interleaved LLC resonant converter operating at constant switching frequency,” IEEE Trans. Power Electron., vol. 29, no. 6, pp. 2951–2943, Jun. 2014.
[9] Z. Hu, Y. Qiu, Y.-F. Liu, and P. C. Sen, “A control strategy and design method for interleaved LLC converters operating at variable switching frequency,” IEEE Trans. Power Electron., vol. 29, no. 8, pp. 4426–4437, Aug. 2014.
[10] H. Wang, Y. Chen, Y. Qiu, P. Fang, Y. Zhang, L. Wang, Y.-F. Liu, J. Asifahian, and Z. Yang, “Common capacitor multiphase LLC converter with passive current sharing ability,” IEEE Trans. Power Electron., vol. 33, no. 1, pp. 370–387, Jan. 2018.
[11] H. Wang, Y. Chen, Y.-F. Liu, J. Afsharian, and Z. Yang, “A passive current sharing method with common inductor multiphase LLC resonant converter,” *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6994–7010, Sep. 2017.

[12] M. Noah, S. Endo, H. Ishibashi, K. Nanamori, J. Imaoka, K. Umetani, and M. Yamamoto, “A current sharing method utilizing single balancing transformer for a multiphase LLC resonant converter with integrated magnetics,” *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 2, pp. 977–992, Jun. 2018.

[13] O. Kirshenboim and M. M. Peretz, “Combined multilevel and two–phase interleaved LLC converter with enhanced power processing characteristics and natural current sharing,” *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5613–5620, Jul. 2018.

[14] X. Fang, H. Hu, Z. J. Shen, and I. Batarseh, “Operation mode analysis and peak gain approximation of the LLC resonant converter,” *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1985–1995, Apr. 2012.

[15] G. Ivensky, S. Bronstein, and A. Abramovitz, “Approximate analysis of resonant LLC DC–DC converter,” *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3274–3284, Nov. 2011.

[16] X. Sun, Y. Shen, Y. Zhu, and X. Guo, “Interleaved boost–integrated LLC resonant converter with fixed–frequency PWM control for renewable energy generation applications,” *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4312–4326, Aug. 2015.

[17] X. Sun, Y. Shen, W. Li, and H. Wu, “A PWM and PFM hybrid modulated three–port converter for a standalone PV/battery power system,” *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 4, pp. 984–1000, Dec. 2015.

**YOSHIYA TADA** was born in 1994. He received the B.E. degree in electrical and electronics engineering from Ibaraki University, Hitachi, Japan, where he is currently pursuing the M.E. degree in electrical and electronics engineering with the Graduate School of Science and Engineering. His research interest includes resonant converters.

**MASATOSHI UNO** (Member, IEEE) was born in Japan, in 1979. He received the B.E. degree in electronics engineering and the M.E. degree in electrical engineering from Doshisha University, Kyoto, Japan, in 2002 and 2004, respectively, and the Ph.D. degree in space and astronautical science from the Graduate University for Advanced Studies, Hayama, Japan, in 2012.

In 2004, he joined the Japan Aerospace Exploration Agency, Sagamihara, Japan, where he developed spacecraft power systems including battery, photovoltaic, and fuel cell systems. In 2014, he joined the Department of Electrical and Electronics Engineering, Ibaraki University, Ibaraki, Japan, where he is currently an Associate Professor of electrical engineering. His research interests include switching power converters for renewable energy systems, life evaluation for EDLCs and lithium-ion batteries, and the development of spacecraft power systems. He received the Isao Takahashi Power Electronics Award, in 2018.

**YUSUKE SATO** was born in 1995. He received the B.E. and M.S. degrees in electrical and electronics engineering from Ibaraki University, Ibaraki, Japan, in 2017 and 2019, respectively. He is currently with Panasonic Corporation. His research interest includes dc–dc converters for automotive applications.

---

**YOSHIYA TADA**

**MASATOSHI UNO**

**YUSUKE SATO**