Erase-Hidden and Drivability-Improved Magnetic Non-Volatile Flip-Flops With NAND-SPIN Devices

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Abstract—Non-volatile flip-flops (NVFFs) using power gating techniques promise to overcome the soaring leakage power consumption issue with the scaling of CMOS technology. Magnetic tunnel junction (MTJ) is a good candidate for constructing the NVFF thanks to its low power, high speed, good CMOS compatibility, etc. In this article, we propose a novel magnetic NVFF based on an emerging memory device called NAND-SPIN. The data writing of NAND-SPIN is achieved by successively applying two unidirectional currents, which respectively generate the spin orbit torque (SOT) and spin transfer torque (STT) for erase and programming operations. This characteristic allows us to design an erase-hidden and drivability-improved magnetic NVFF. Furthermore, more design flexibility could be obtained since the backup operation of the proposed NVFF is not limited by the inherent slave latch. Simulation results show that our proposed NVFF achieves performance improvement in terms of power, delay and area, compared with conventional slave-latch-driven SOT-NVFF designs.

Index Terms—Non-volatile flip-flop, NAND-SPIN, spin orbit torque (SOT), spin transfer torque (STT), magnetic tunnel junction (MTJ).

I. INTRODUCTION

A S KEY units in digital systems, flip-flops (FFs) store computing data for the central processing unit (CPU), micro controller unit (MCU), and so on. However, with CMOS technology scaling down, leakage power of the conventional flip-flops is becoming more and more significant [1], [2]. In a microprocessor, the leakage power may exceed 40% of the total system power below 65 nm technology node [3]. Power gating (PG) technology, which makes the inactive circuits disconnected from the power supply in the standby mode, is a popular solution to eliminate the leakage power [4], [5]. Nevertheless, the conventional CMOS FFs cannot retain the data during the power off, thus the data have to be backup into the main memory or disk drivers before triggering the PG, which results in additional speed and energy overhead. These bottlenecks can be overcome by designing a non-volatile flip-flop (NVFF) [6]–[11], which is a hybrid architecture combining the conventional CMOS FF with the emerging non-volatile memories (NVMs). While the PG is activated in a NVFF, the data can be backup into the local NVMs rather than be moved to the other modules. Thus, additional cost in the speed and energy could be avoided.

Amongst the NVFFs, magnetic NVFFs employing magnetic tunnel junction (MTJ) have been paid much attention due to high speed, low power, unlimited endurance and good CMOS compatibility [11]–[26]. Spin transfer torque (STT) is most widely used for the write operation of the MTJ [27]–[30], and hence for the backup operation of the magnetic NVFF. However, the performance of the STT-NVFFs is deteriorated by the asymmetry of backup operation between two write directions, which is attributed to the asymmetrical STT switching efficiency. In addition, the backup operation requires a pair of opposite currents to write ‘0’ and ‘1’, respectively, thus the source degeneration effect degrades the drivability of the related transistors, due to the different gate-source biases while writing ‘0’ and ‘1’ [31]. As a result, the transistors have to be large enough to tolerate the worst case of two switching events. However, it would induce large current for the other case, which incurs larger energy dissipation and threatens the reliability of the devices. Although spin orbit torque (SOT) have been recently explored as an alternative to the STT [32]–[34], the source degeneration effect remains unresolved in the SOT-NVFF since the SOT switching current is still bi-directional.

In the most of the area-efficient magnetic NVFFs, the MTJs are directly switched by a pair of coupled CMOS inverters in the slave latch during the backup operation [21], [23], [25], [30]. Large-size transistors are required to ensure the drivability of the slave latch, which may degrade the performance of the CMOS part (i.e. volatile flip-flop structure). Moreover, most of the SOT-NVFFs employ two complementary SOT-MTJs to store 1-bit non-volatile data. The current channels (i.e. the heavy metal below the MTJ) have to be oppositely placed so that the MTJs are always written into the complementary states [11], [19], [23], [25], [26]. This type of layout will lead to difficulty in the practical fabrication process.

To overcome the aforementioned drawbacks of both STT-NVFFs and SOT-NVFFs, in this paper we propose an erase-hidden and drivability-improved magnetic NVFF based on a high-performance magnetic memory structure called NAND-SPIN [35]. Generally, the data is written into the NAND-SPIN by applying two unidirectional currents, which perform a SOT-induced erasing and a STT-driven programing, respectively. The erase operation is hidden into the active mode to reduce the...
backup delay. Furthermore, the source degeneration effect is eliminated thanks to the use of unidirectional switching currents. More importantly, the proposed NVFF relaxes the requirement on the drivability of the inherent slave latch, and therefore allows a more flexible design. Two embodiments of the proposed NVFF, which uses perpendicular- and in-plane-anisotropy MTJs, are designed and simulated with an electrical model of the SOT-MTJ and CMOS 40 nm design kit. Comparison among various NVFFs is shown based on the simulation results.

The remainder of this paper is organized as follows. Section II introduces the fundamentals of NAND-SPIN devices. In Section III, we elaborate the circuit structure and operation of the proposed NVFF. The simulation results are discussed and evaluated in Section IV. An extension work is described in Section V. Finally, Section VI concludes this paper.

II. FUNDAMENTAL OF NAND-SPIN DEVICE

The NAND-SPIN device used in this work is composed of two MTJs and a heavy-metal strip, as shown in Fig. 1. An MTJ comprises of two ferromagnetic layers, called free layer (FL) and pinned layer (PL), separated by a tunneling oxide barrier. The magnetization of the PL is fixed whereas the FL magnetization can be switched between parallel and antiparallel (P and AP) to that of the PL, corresponding to low and high tunnel resistances, respectively. Two MTJs of the NAND-SPIN device are always switched to complementary resistance states, which represents 1-bit non-volatile data.

Here the MTJs are switched by a SOT-induced erasing and a STT-driven programming. The detailed operation is described as follows [35]. First, a current is applied to the heavy metal and induces the SOT, which switches both the MTJs to AP states. Thus, this step is called erase operation. Then the programming operation is performed. The SOT current is turned off, and another current flowing through one MTJ will switch it to P state by the STT. The other MTJ remains at AP state. As a result, two MTJs are switched to P and AP states, respectively. Depending on the relative states between two MTJs, the data ‘0’ or ‘1’ is stored.

Compared with the conventional STT- or SOT-MTJs, NAND-SPIN shows extraordinary properties in energy efficiency and area efficiency for three reasons. First, AP and P states are respectively written by the SOT and STT. Therefore, the write currents are unidirectional, which allows more compact circuit structure and avoids the source degeneration of the transistors [31]. Second, the asymmetry of the STT is alleviated since the STT is only used for the easier AP-to-P switching. Third, NAND-SPIN device could be fabricated as a whole by self-aligned process [36], which simplifies the procedure and improves the integration density.

An electrical model of NAND-SPIN is developed for the simulation and evaluation in this paper. The resistance of the MTJ is modeled by Brinkman model, bias-dependent tunneling magnetoresistance effect, Slonczewski model, etc. More details could be found in [37]. The magnetization switching is described by a Landau-Lifshitz-Gilbert (LLG) equation, which considers both the STT and SOT, as

\[ \frac{\partial m}{\partial t} = -\gamma \mu_0 m \times H_{\text{eff}} + \alpha m \times \frac{\partial m}{\partial t} - \xi \mathcal{P} J_{\text{STT}} m \times (m \times m_p) - \xi \eta J_{\text{SHE}} m \times \sigma_{\text{SHE}} \]  

where \( m \) and \( m_p \) are the unit vectors along the magnetization orientation of the FL and PL, respectively. \( \sigma_{\text{SHE}} \) is the polarization direction of the SOT-induced spin accumulation. \( J_{\text{STT}} \) and \( J_{\text{SHE}} \) are the STT and SHE write current densities, respectively. \( H_{\text{eff}} \) is the effective magnetic field. \( \gamma \) is the gyromagnetic ratio, \( \mu_0 \) is the vacuum permeability, \( \xi = \gamma h/2e t_F M_s \) with \( h \) the reduced Planck constant, \( e \) the elementary charge, and \( t_F \) the thickness of the FL. Other parameters are exhibited in Table I.

The asymmetry of the STT is reflected by \( \mathcal{P} \), as

\[ \mathcal{P} = \frac{2P_A^2}{(\Lambda^2 + 1) + (\Lambda^2 - 1)(m \cdot m_p)} \]  

where \( \Lambda \) is a factor [40]. The larger \( \Lambda \) induces more asymmetrical STT efficiency between two switching directions. \( \Lambda = 1 \) will eliminate the asymmetry of the STT.

**Table I** SIMULATION PARAMETERS

| Parameters                      | iMTJ device [19][21][23][38] | pMTJ device [19][35][38][39] |
|---------------------------------|------------------------------|-------------------------------|
| Free layer volume               | \( \pi/4 \times 120 \text{nm} \times 40 \text{nm} \) | \( 40 \text{nm} \times 40 \text{nm} \) |
| Dimensions of W strip (w x l x d) | \( 180 \text{nm} \times 60 \text{nm} \times 5 \text{nm} \) | \( 80 \text{nm} \times 60 \text{nm} \times 5 \text{nm} \) |
| Damping constant (a)           | 0.0122                       | 0.035                         |
| Resistance-area product (RA)   | 50 \( \mu \text{m}^2 \)      | 50 \( \mu \text{m}^2 \)       |
| Saturation magnetization (M_s) | 1000 A/m                     | 1000 A/m                      |
| Spin Hall angle (\( \gamma \)) | 0.3                           | 0.3                           |
| Tunneling spin polarization (P) | 0.62                          | 0.62                          |
| TMR ratio                      | 120%                         | 120%                          |
| Heavy metal resistivity (\( \rho_{\text{HM}} \)) | 200 \( \mu \Omega \cdot \text{cm} \) | 200 \( \mu \Omega \cdot \text{cm} \) |
| Thermal stability barrier (E)  | 92 \( k_B T \)               | 32 \( k_B T \)                |
| Asymmetrical STT efficiency (\( \Lambda \)) | 1.3                           | 1.3                           |
| Bias magnetic field (\( B_{\text{bias}} \)) | -                              | -0.005/\( \mu_0 \) |
III. PROPOSED NVFF DESIGN WITH NAND-SPIN

This section presents the schematic and operation of the proposed NAND-SPIN based NVFF using both perpendicular- and in-plane-anisotropy MTJs (named as p-NAND-SPIN and i-NAND-SPIN). NVFFs targeting PG architectures could work in four modes: active, backup, standby, and restore modes. In the active mode, the NVFF operates as a normal volatile flip-flop (VFF). Before triggering the PG, the volatile data need to be written into the non-volatile NAND-SPIN in the backup mode. Then the power supply could be turned off in the standby mode to avoid the leakage power. Once the power supply is restarted, the non-volatile data inside the NAND-SPIN need to be written back to the volatile flip-flop in the restore mode. As mentioned in Section II, the data is written into the NAND-SPIN through an erase operation and a programming operation. It is worth noting that the polarity of the written data is determined by the programming operation rather than the erase operation. Therefore, we intentionally hide the erase operation inside the active mode so that only programming operation occurs in the backup mode. With this erase-hidden design, the backup latency is reduced, meanwhile the size of driving transistors could be tuned more flexibly.

A. Circuit Operation

The schematic of the p-NAND-SPIN NVFF is illustrated in Fig. 2(a), including a CMOS-based VFF part (outside the dashed region) and a NAND-SPIN based non-volatile part (inside the dashed region). A slave latch is combined with one NAND-SPIN and six additional transistors (P1-2 and N1-4) for data retention during the standby mode. This non-volatile slave latch is connected with a clocked CMOS master latch to form the NVFF. The i-NAND-SPIN NVFF is not shown here for the simplicity, because it can be designed with the same structure as Fig. 2(a) except for the anisotropy direction of the MTJ.

During the active mode, as shown in Fig. 2(b), EQ = ‘1’, Ctrl = ‘0’ and REN = ‘0’, thus P1, N1 and N3–4 are deactivated. As a result, the NVFF acts as a CMOS-based VFF which is isolated from the NAND-SPIN. Once the NVFF just enters the active mode, the PSL signal holds low and the EEN signal is set high (meanwhile, the BEN signal is also high) to turn on transistors...
P2 and N2 for a short time to initialize the NAND-SPIN to state ‘1’, which means that two MTJs are initialized to AP states (i.e. the erase operation mentioned above). This erase operation of the NAND-SPIN does not interfere with the normal operation of CMOS-based VFF due to the disconnected structure. As a result, the erase operation is hidden inside the active mode without additional latency.

Before the system enters the standby mode through the PG technology, the runtime data in the NVFF need to be backup into the NAND-SPIN.

To perform a backup, the CTRL signal is asserted high, the PSL signal and the CLK signal hold low for storing data into the slave latch. At this time, the EEN signal is relevant to the backup operation and holds low. As mentioned above, both MTJ1 and MTJ2 have been erased to AP states during the active mode. Thus, one of two MTJs needs to be switched to P state for completing the backup. Assume QT = ‘1’ and QC = ‘0’, as shown in Fig. 2(d), transistors P2 and P6 work together as the current source, while transistor N5 acts as the current sink. Two currents (Iw1 and Iw2) driven by P2 and P6 are applied to the NAND-SPIN. As a result, MTJ2 is switched to P state through the NAND-SPIN. The output signal Q of the NVFF follows the input signal QT.

The restore operation is illustrated in Fig. 2(c). Once the power supply is restarted, EQ is kept at low level so that transistor P1 shorts QT and QC, and thus the power supply charge QT and QC to VDD/2. Meanwhile the signal REN is pulled down and transistor N1 is open. Thus, QT and QC start discharging to form two read currents (Ir1 and Ir2) passing through MTJ1 and MTJ2, respectively. At this time the signal EQ is pulled up again to isolate QT from QC. As MTJ1 and MTJ2 have been written into complementary states during the backup mode, the discharging in the low MTJ resistance branch is faster than that in the other branch. As a result, the node on the low MTJ resistance branch drops to ground and the other node is pulled up to VDD. In this way, the complementary states in the NAND-SPIN are restored to the slave latch of VFF.

B. Advantages of the Proposed NVFFs

Generally, most of the SOT-NVFF architectures rely on the inherent slave latch to achieve the backup operation. However, these architectures exhibit poor performance in backup delay and energy consumption. Below we will demonstrate how our proposed NVFF improves the speed and energy efficiency.

For the existing SOT-NVFFs, the polarity of the written data is dependent on the direction of the applied current. Therefore, bi-directional current need to be generated by the driving circuits. A common solution is to construct an independent write driver with additional four transistors [19], [20], but it leads to large area overhead. To achieve an area-efficient design, this bi-directional current is mostly provided by an inherent slave latch (e.g. transistors P5-6 and N5-6 in Fig. 2). To ensure sufficient write current, the transistors of the slave latch have to be large, which may degrade the performance of CMOS-based VFF part, such as large area overhead and strong parasitic effects. In contrast, our proposed NVFF employs unidirectional current to achieve the backup operation. Thus, the write current could be mainly provided by the power supply rather than the slave latch. Only two access transistors (P2 and N2 in Fig. 2) are added for the efficient controlling. Furthermore, transistor P2 shows the largest drivability since it is directly connected to the power supply to maximize its source-gate bias (i.e. the source degeneration effect is eliminated). The same benefit is obtained by transistor N2 during the erase operation, as the unidirectional current is directly injected to ground. Thanks to this novel design, the current for the backup operation could be tuned by adjusting transistors P2 and N2, not limited by the size of the slave latch.

In addition, some SOT-NVFFs employ a pair of oppositely-placed SOT-MTJs to store complementary states [11], [19], [23], [25], [26]. Although oppositely-placed SOT-MTJs could be independently fabricated, they require specific routing at transistor level to ensure the storage of complementary states. In contrast, in our proposed NAND-SPIN based NVFF, two MTJs share the same heavy metal strip which could be easily fabricated by self-aligned etching process [36]. As a whole device, NAND-SPIN could store complementary states through well-designed operation method without the additional hardware routing.

IV. RESULTS AND DISCUSSION

In this section the proposed NVFFs are simulated with a CMOS 40 nm design kit and a SOT-MTJ model mentioned in Section II. The comparison of performance among various NVFFs is shown based on the simulation results. The optimization strategy of the proposed NVFF is discussed by investigating the roles of key parameters.

A. Evaluation of Different SOT-Based NVFF Architectures

Fig. 3 shows the transient simulation results of the proposed p-NAND-SPIN NVFF. The signal waveforms reproduce the behaviors of the four operation modes described in Section III-A. During the active mode, the EQ signals are kept low to separate the NVM part from the VFF part, and the EEN signal is asserted high for a short time to enable an erase operation of NAND-SPIN. The output signal Q of the NVFF follows the input signal D at the positive edge of the CLK signal. During the backup mode, the CRTL, EQ, and VDD signals are pulled high, and other signals are kept low. During the sleep mode, all signals are reduced to low, and the MTJs store the data of the VFF part in complementary states. The restore mode is activated by pulling VDD, CRTL, REN and BEN high while the EQ signal is kept low for 450 ps and then switched to high. The P1 transistor controlled by the EQ signal short the inverters at first to charge the nodes QT and QC to half supply voltage, and then releases the voltage of the nodes to sense the difference of the NAND-SPIN. The timing diagram of i-NAND-SPIN NVFF can be obtained
Fig. 3. Timing diagram of the proposed p-NAND-SPIN NVFF. The MTJ1 and MTJ2 signals are normalized z-component magnetization of the free layer. Others are voltage signals.

TABLE II

| Parameter | p-y type | i-y type | [23] | [25] | p-x type | i-x type |
|-----------|---------|---------|------|------|---------|---------|
| Delay (ns) | Backup | 1.04 | 1.87 | 4.95 | 4.32 | 0.99 | 1.868 |
|           | Restore | 0.66 | 0.66 | 0.66 | 0.66 | 0.66 | 0.66 |
| Energy (J) | Backup | 84.3 | 216.5 | 281.7 | 239.5 | 84.1 | 216.4 |
|           | Erase   | 84.1 | 119.9 | - | - | 196.0 | 229.2 |
|           | Restore | 56.0 | 54.0 | 67.6 | 53.0 | 58.4 | 64.4 |

The transistor sizes of PFET and NFET in VFF part of all NVFFs above are set to 400/40 and 290/40, respectively. In the proposed NVFFs (p-y type, i-y type, i-x type), the driving transistor P2 is set to 1000/40; in the proposed p-x type NVFF, the driving transistor P2 is set to 2000/40 to ensure a successful erase. The definitions of x-type and y-type will be described in Section V.

Two NVFFs presented in [23] and [25] are chosen as the baseline for comparison, because they showed more excellent performance than the existing other proposals. For a fair comparison, the same MTJ parameters and VFF part are used among the various NVFFs. The other transistor parameters are configured so that each NVFF obtains its optimal performance under the given MTJ and VFF settings. The detailed comparison results are listed in Table II.

The proposed i-NAND-SPIN NVFF design offers 10% lower backup energy with nearly 43% reduction of the backup delay compared to [25]. This improvement is mainly attributed to two reasons: first, in the i-NAND-SPIN NVFF the magnitude of the write current is not limited by the slave latch. Instead larger write current could be driven by the transistor P2. For instance, the backup write currents of p- and i-NAND-SPIN NVFFs are respectively ∼80 μA and ∼105 μA. However, the backup write currents of [23] and [25] are only 48 μA and 50 μA under the given parameter settings. Second, only AP-to-P STT switching is performed in the backup mode, which costs smaller energy and shorter delay than the P-to-AP case due to the asymmetrical
STT efficiency. But in the conventional STT-MTJ, the switching delay has to be dominated by the worse P-to-AP case [41], [42]. For instance, P-to-AP STT switching delay of the proposed p-NAND-SPIN NVFF is as large as ∼2.7 ns under the above parameter settings. Thus, in our proposed NAND-SPIN NVFF the AP state is written by the SOT-induced erase operation rather than the STT for avoiding the excessive cost in the speed and energy. As a result, although the proposed NAND-SPIN NVFFs use larger write currents than [23] and [25], their backup energy could be smaller thanks to the shorter switching delay. The proposed i-NAND-SPIN offers 23% lower energy and 2.6× faster backup speed compared with [23], using the same operation mechanism.

As for the proposed p-NAND-SPIN NVFF, 65% lower backup energy and 4.2× faster backup speed can be achieved compared with [25]. The improvement is more significant than the case of i-NAND-SPIN NVFF, which is attributed to the fact that the perpendicular-anisotropy optimizes the STT efficiency. Furthermore, the design freedom is enhanced in the proposed NVFF since the backup circuit is almost decoupled from the CMOS-based slave latch. Nevertheless, it is important to mention that the designs in [23] and [25] may show better performance under the other scenarios.

It should be pointed out that concealment of erase operation also largely reduces delay and energy during the period of backup. The influence of erase energy on the active mode is weakened as the duration of the active mode increases.

All the NVFFs mentioned above perform a restore operation in the same way, thus fewer differences can be seen from the comparison shown in Table II.

### B. Drivability Analysis on the Proposed NVFF

As mentioned above, the currents for the backup operation mainly arise from the driving transistor P2 rather than the inherent slave latch. Therefore, more design flexibility could be obtained. Here we study the backup performance as a function of P2 transistor size, as shown in Fig. 4.

Given a fixed VFF area, we observe the change of backup performance by sweeping the width of the driving transistor P2 in both p- and i-NAND-SPIN NVFFs. As shown in Fig. 4(b), when the width of P2 varies from 500 nm to 2000 nm, the backup delay and energy of i-NAND-SPIN NVFF are reduced by 12.4%
and 5\%, respectively. Similarly, as shown in Fig. 4(a), they decrease by 10.2\% and 5\% when the width of P2 changes from 1000 nm to 2000 nm in the p-NAND-SPIN NVFF. This tendency could be easily understood since P2 acts as a current source offering the backup current. From the results, a trade-off could be obtained between the backup performance and P2 size: faster and more energy-efficient backup operation of NAND-SPIN NVFFs require a larger P2.

C. Performance of the Proposed NVFFs With CMOS-Based VFF Scaling

In addition to the driving transistor P2, the CMOS-based VFF part also has a non-negligible influence on the backup performance. In particular, the CMOS-based slave latch can provide a portion of backup current for the MTJs, and hence influences the backup speed and backup energy of the NVFF. Figs. 5–6 shows the backup performance as a function of the various VFF area. At each VFF area, a range of performance variation is obtained by adjusting the size of P2. It is seen that the backup performance is degraded with the scaling of the VFF, because the current source or current sink transistors are shrunk to limit the total backup current. The degradation could be compensated by adjusting appropriately the P2 size, which is consistent with the conclusion of Fig. 4. For the p-NAND-SPIN NVFF, the ranges of variation at different VFF areas are not uniform, due to the non-linear dependence of the switching speed on the current.

Although the backup performance is dependent on the VFF area, we argue that our NAND-SPIN NVFF has a more relaxed requirement on the VFF area, compared with previously proposed NVFFs. In Fig. 6, we show the detailed comparison between our proposal and previous slave-latch-driven NVFFs. Clearly, the NVFF in [23] fails to perform a backup operation when the width of PFET/NFET in VFF is scaled down to 320/240 and 240/180, due to the inadequate driving current. The similar phenomenon could be observed from the NVFF in [25]. However, in our proposal, the unique characteristic of NAND-SPIN allows the use of P2 to provide additional drivability. Therefore, the backup operation is not easily blocked by the scaling VFF. In other words, our proposed NAND-SPIN NVFFs could achieve efficient backup operation in a wide range of VFF area. For instance, in Fig. 5(c) and (d), when the PFET and NFET of VFF are respectively scaled from 400/40 to 240/40 and 180/40, the increment of backup delay and energy of i-NAND-SPIN NVFF are less than 1 ns and 50 fJ, respectively. These results mean that our proposed NVFF could be more area-efficient thanks to the fact that the size of VFF part is allowed to be smaller.

V. EXTENSION AND DISCUSSION

As an extension of the proposed NVFF, here we design a new type of NAND-SPIN device with another geometry, and evaluate its application in the NVFF. Furthermore, we perform Monte-Carlo simulations to evaluate the robustness of the proposed NVFFs.

A. X-Type NAND-SPIN

In Fig. 1, the erase current is applied to NAND-SPIN along y-axis. Actually, it is also feasible to apply it along x-axis, as shown in Fig. 7(a). Thus, we named them as y-type and x-type NAND-SPINs, respectively. It is worth noting that the exchange bias direction of x-type p-NAND-SPIN needs to be changed to x-axis for the deterministic switching. Similarly, the magnetization direction of x-type i-NAND-SPIN should be changed to y-axis.

The working mechanisms of x-type and y-type NAND-SPINs are identical, except for the direction of the applied current, as
TABLE III
MEANS AND STANDARD DEVIATIONS (STD DEV) OF QT, QC AND IW
(IW1 + IW2) DURING THE BACKUP MODE

|                | p-y backup 0 | p-y backup 1 |                | i-y backup 0 | i-y backup 1 |                | i-x backup 0 | i-x backup 1 |
|----------------|--------------|--------------|----------------|--------------|--------------|----------------|--------------|--------------|
| QT (V)         | 124.1m       | 122.3m       | QC (V)         | 11.29m       | 178.6m       | Iw (A)         | 8.667u       | 104.5u       |
| Std dev        | 1.1          | 1.1          | 5.183u         | 1.1          | 1.1          | 95.46u         | 10.88m       | 178.6m       |
| Mean           | 124.1m       | 122.3m       | QC (V)         | 11.29m       | 178.6m       | Iw (A)         | 8.667u       | 104.5u       |
| Std dev        | 1.1          | 1.1          | 5.183u         | 1.1          | 1.1          | 95.46u         | 10.88m       | 178.6m       |

shown in Fig. 7(a). It is important to mention that the number of terminals of x-type NAND-SPIN is less than y-type NAND-SPIN, which means a smaller area overhead.

B. X-Type NAND-SPIN NVFF

The schematic of x-type NAND-SPIN NVFF is shown in Fig. 7(b). Compared to y-type NAND-SPIN NVFF, the programming currents for ‘0’ and ‘1’ are more symmetrical thanks to the altered geometry. The detailed performance metrics is listed in Table I. The erase operation of x-type NAND-SPIN NVFF requires longer delay, since the current is applied to a larger lateral area of the heavy metal for driving two MTJs in parallel. Nevertheless, the performance of NVFF is not deteriorated since the erase operation is hidden into the active mode. For the backup and restore performances, all the conclusions obtained from y-type NAND-SPIN NVFFs remain correct in the case of x-type NAND-SPIN NVFFs, due to the same operation mechanism.

C. Robustness Evaluation of the Proposed NVFFs

To validate the robustness of the proposed NVFFs, we run Monte Carlo simulations 200 times which consider CMOS variation and mismatch, as shown in Fig. 8. The results demonstrate that all the proposed NVFFs can complete backup successfully within 200 times, which validates the robustness of our NVFF design. Besides, the means and standard deviations of QT, QC and Iw of the proposed NVFFs during the backup mode are listed in Table III, which shows the stability of the backup operation on the proposed NVFFs.

VI. CONCLUSION

We have proposed a novel NVFF by utilizing the advantages of the NAND-SPIN devices. The erase operation is hidden into the active mode for improving the operation speed. The unidirectional programming current of the NAND-SPIN devices allows to use an additional current source transistor to enhance the drivability, meanwhile relaxes the requirement on the VFF parts. Simulation results show the advantages of our proposed NVFF over the previous solutions, moreover, more considerable tolerance to the VFF scaling is obtained in the proposed NAND-SPIN NVFF.

In this work we suppose that the programming operation of NAND-SPIN device is achieved by the sole STT mechanism. Actually, recent experiments have demonstrated that the STT current in the NAND-SPIN device inevitably passes the partial heavy metal and induces additional SOT effect, which further assists the magnetization switching [43], [44]. In addition, the current is non-uniformly distributed at the heavy-metal/MJ interface, which assists the domain nucleation and reduce the switching current [44]. Also many progresses have been made in the community of SOT-MTJs [45]. Therefore, all the above simulated results of the NAND-SPIN NVFF promise to be improved in the practical realization.

REFERENCES

[1] M. Horowitz, E. Alon, D. Patil, S. Naffziger, R. Kumar, and K. Bernstein, “Scaling, power, and the future of CMOS,” in IEEE Int. Electron Devices Meet. IEDM Tech. Digest, 2005, pp. 7–15.
[2] N. S. Kim et al., “Leakage current: Moore’s law meets static power,” Computer, vol. 36, no. 12, pp. 68–75, Dec. 2003.
[3] H. Kim, J. H. Ahn, and J. Kim, “Exploiting replicated cache blocks to reduce l2 cache leakage in CMPs,” IEEE Trans. Very Large Scale Integr. Syst., vol. 21, no. 10, pp. 1863–1877, Oct. 2013.
[4] Z. Hu, A. Buyuktosunoglu, V. Srinivasan, V. Zyuban, H. Jacobson, and P. Bose, “Microarchitectural techniques for power gating of execution units,” in Proc. Int. Symp. Low Power Electron. Design, 2004, pp. 32–37.
[5] S. Shigematsu, S. Mutoh, Y. Matsuya, Y. Tanabe, and J. Yamada, “A 1-V high-speed MTCMOS circuit scheme for power-down application circuits,” IEEE J. Solid-State Circuits, vol. 32, no. 6, pp. 861–869, Jun. 1997.
[6] I. Kazi et al., “Energy/reliability trade-offs in low-voltage ReRAM-based non-volatile flip-flop design,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 61, no. 11, pp. 3155–3164, Nov. 2014.
[7] A. Lee et al., “A ReRAM-based nonvolatile flip-flop with self-write-termination scheme for frequent-off fast-wake-up nonvolatile processors,” IEEE J. Solid-State Circuits, vol. 52, no. 8, pp. 2194–2207, Aug. 2017.
[8] Y. Ye, Y. Du, D. Gao, Y. Kang, Z. Song, and B. Chen, “A non-volatile flip-flop based on diode-selected PCM for ultra-low power systems,” in Proc. Int. Work. Inf. Data Storage Tenth Int. Symp. Opt. Storage, 2016, pp. 981803-1-981803-6.
[9] C. M. Jung, K. H. Jo, E. S. Lee, H. M. Vo, and K. S. Min, “Zero-sleep-leakage flip-flop circuit with conditional-storing memristor retention latch,” IEEE Trans. Nanotechnol., vol. 11, no. 2, pp. 360–366, Mar. 2012.
[10] M. Qazi, A. Amerasekera, and A. P. Chandrakasan, “A 3.4-\textmu A feram-enabled d flip-flop in 0.13-\textmu CMOS for nonvolatile processing in digital systems,” IEEE J. Solid-State Circuits, vol. 49, no. 1, pp. 202–211, Jan. 2014.
[11] N. Sakimura, T. Sugibayashi, R. Nebashi, and N. Kasai, “Nonvolatile magnetic flip-flop for standby-power-free SoCs,” IEEE J. Solid-State Circuits, vol. 44, no. 8, pp. 2240–2250, Aug. 2009.
[12] D. Chabi et al., “Ultra low power magnetic flip-flop based on checking-pointing/power gating and self-enable mechanisms,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 61, no. 6, pp. 1755–1765, Jun. 2014.
[13] D. Suzuki and T. Hanyu, “Magnetic-tunnel-junction based low-energy nonvolatile flip-flop using an area-efficient self-terminated write driver,” J. Appl. Phys., vol. 117, no. 17, Jan. 2015, Art. no. 17B504.
[14] R. Bishnoi, F. Oboril, and M. B. Tahoori, “Design of defect and fault-tolerant nonvolatile spintronic flip-flops,” *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 25, no. 4, pp. 1421–1432, Apr. 2017.

[15] K. Ryu, J. Kim, J. Jung, J. P. Kim, S. H. Kang, and S. O. Jung, “A magnetic tunnel junction based zero standby leakage current retention flip-flop,” *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 20, no. 11, pp. 2044–2053, Nov. 2012.

[16] M. Kazemi, E. Ipek, and E. G. Friedman, “Energy-efficient nonvolatile flip-flop with subnanosecond data backup time for fine-grain power gating,” *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 12, pp. 1154–1158, Dec. 2015.

[17] H. Cai, Y. Wang, W. Zhao, and L. A. De Barros Naviner, “Multiplexing sense-amplifier-based magnetic flip-flop in a 28-nm FDSOI technology,” *IEEE Trans. Nanotechnol.*, vol. 14, no. 4, pp. 761–767, Jul. 2015.

[18] A. S. Iyengar, S. Ghosh, and J. W. Jang, “MTJ-Based state retentive flip-flop with enhanced-scan capability to sustain sudden power failure,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 8, pp. 2062–2068, Aug. 2015.

[19] K. Jabeur, G. Di Pendina, F. Bernard-Granger, and G. Prenat, “Spin orbit torque non-volatile flip-flop for high speed and low energy applications,” *IEEE Electron Device Lett.*, vol. 35, no. 3, pp. 408–410, Mar. 2014.

[20] Z. Wang, W. Zhao, D. Deng, Y. Zhang, and J. O. Klein, “Magnetic non-volatile flip-flop with spin-Hall assistance,” *Phys. Status Solidi - Rapid Res. Lett.*, vol. 9, no. 6, pp. 375–378, May 2015.

[21] K. W. Kwon, S. H. Choday, Y. Kim, X. Fong, S. P. Park, and K. Roy, “SHE-NVFF: Spin hall effect-based nonvolatile flip-flop for power gating architecture,” *IEEE Electron Device Lett.*, vol. 35, no. 4, pp. 488–490, Apr. 2014.

[22] W. Kang, Y. Ran, W. Lv, Y. Zhang, and W. Zhao, “High-speed, low-power, magnetic non-volatile flip-flop with voltage-controlled, magnetic anisotropy assistance,” *IEEE Magn. Lett.*, vol. 7, No. 2016, Art. no. 3106205.

[23] K. Ali, F. Li, S. Y. H. Lua, C. Heng, and S. Member, “Energy- and area-efficient spin-orbit torque nonvolatile flip-flop for power gating architecture,” *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 26, no. 4, pp. 630–638, Apr. 2018.

[24] A. Jaiswal, R. Andrawis, and K. Roy, “Area-efficient nonvolatile flip-flop based on spin hall effect,” *IEEE Magn. Lett.*, vol. 9, May 2018, Art. no. 430304.

[25] W. Kang, W. Lv, Y. Zhang, and W. Zhao, “Low store power high-speed high-density nonvolatile SRAM design with spin hall effect-driven magnetic tunnel junctions,” *IEEE Trans. Nanotechnol.*, vol. 16, no. 1, pp. 148–154, Jan. 2017.

[26] R. Bishnoi, F. Oboril, and M. B. Tahoori, “Non-volatile non-shadow flip-flop using Spin Orbit Torque for efficient normally-off computing,” in *Proc. ASP-Digital Analog Converter*, 2016, pp. 769–774.

[27] J. C. Slonczewski, “Current-driven excitation of magnetic multilayers,” *J. Magn. Magn. Mater.*, vol. 159, no. 1, pp. L1–L7, 1996.

[28] L. Berger, “Emission of spin waves by a magnetic multilayer traversed by a current,” *Phys. Rev. B, Condens. Matter Mater. Phys.*, vol. 54, no. 13, pp. 9353–9358, Oct. 1996.

[29] X. Fong, Y. Kim, R. Venkatesan, S. H. Choday, A. Raghunathan, and K. Roy, “Spin-transfer torque memories: Devices, circuits, and systems,” *Proc. IEEE*, vol. 104, no. 7, pp. 1449–1488, Jul. 2016.

[30] S. Yamamoto, Y. Shuto, and S. Sugahara, “Nonvolatile flip-flop using pseudo-spin-transistor architecture and its power-gating applications,” in *ISCDG*, 2012, pp. 17–20.

[31] C. J. Lin et al., “45 nm low power CMOS logic compatible embedded STT MRAM utilizing a reverse-connection 1T/1MTJ cell,” in *Proc. IEDM*, 2009, pp. 1–4.

[32] I. M. Miron et al., “Perpendicular switching of a single ferromagnetic layer induced by in-plane current injection,” *Nature*, vol. 476, pp. 189–193, Aug. 2011.

[33] L. Liu, C. F. Pai, Y. Li, H. W. Tseng, D. C. Ralph, and R. A. Buhrman, “Spin-torque switching with the giant spin hall effect of tantalum,” *Science*, vol. 336, no. 6081, pp. 555–558, May 2012.

[34] M. Cubukcu et al., “Spin-orbit torque magnetization switching of a three-terminal perpendicular magnetic tunnel junction,” *Appl. Phys. Lett.*, vol. 104, no. 4, Jan. 2014, Art. no. 042406.

[35] Z. Wang et al., “High-density NAND-like spin transfer torque memory with spin orbit torque erase operation,” *IEEE Electron Device Lett.*, vol. 39, no. 3, pp. 334–346, Mar. 2018.

[36] S. Shiratori et al., “Voltage-control spintronics memory with a self-aligned heavy-metal electrode,” *IEEE Trans. Magn.*, vol. 51, no. 11, Nov. 2017, Art. no. 3401104.

[37] Z. Wang, W. Zhao, and E. Deng, “Perpendicular-anisotropy magnetic tunnel junction switched by spin-Hall-assisted spin-transfer torque,” *J. Phys. D Appl. Phys.*, vol. 48, no. 6, Jan. 2015, Art. no. 65001.

[38] D. Apalkov, S. Watts, A. Driskill-Smith, E. Chen, Z. Diao, and V. Nikitin, “Comparison of scaling of in-plane and perpendicular spin-transfer switching technologies by micromagnetic simulation,” *IEEE Trans. Magn.*, vol. 46, no. 6, pp. 2240–2243, Jun. 2010.

[39] K. Garello et al., “Spin-Orbit Torque MRAM for ultrafast embedded memories from fundamentals to large scale technology integration,” in *Proc. IEEE 11th Int. Memory Workshop*, 2019, pp. 1–4.

[40] J. Xiao, A. Zangwill, and M. D. Stiles, “Boltzmann test of Slonczewski’s theory of spin-transfer torque,” *Phys. Rev. B, Condens. Matter Mater. Phys.*, vol. 70, no. 17, Nov. 2004, Art. no. 172405.

[41] S.-W. Chung et al., “Gbit density STT-MRAM using perpendicular MTJ realized with compact cell structure,” in *Proc. IEEE Int. Electron Dev. Meet.*, Dec. 2016, pp. 27.1.1–27.1.4.

[42] S. H. Choday, S. K. Gupta, and K. Roy, “Write-optimized STT-MRAM bit-cells using asymmetrically doped transistors,” *IEEE Electron Device Lett.*, vol. 35, no. 11, pp. 1100–1102, 2014.

[43] N. Sato, F. Xue, R. M. White, C. Bi, and S. X. Wang, “Two-terminal spin-orbit torque magnetoresistive random access memory,” *Nat. Electron.*, vol. 1, no. 9, pp. 508–511, Sep. 2018.

[44] M. Wang et al., “Field-free switching of a perpendicular magnetic tunnel junction through the interplay of spin-orbit and spin-transfer torques,” *Nat. Electron.*, vol. 1, no. 11, pp. 582–588, Nov. 2018.

[45] S. Shi, Y. Ou, S. V. Aradhy, D. C. Ralph, and R. A. Buhrman, “Fast low-current spin-orbit-torque switching of magnetic tunnel junctions through atomic modifications of the free-layer interfaces,” *Phys. Rev. Appl.*, vol. 9, 2018, Art. no. 011002.