Search for Optimal Systolic Arrays: A Comprehensive Automated Exploration Framework and Lessons Learned

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ABSTRACT
Systolic arrays have been widely used for accelerating HPC and deep learning applications. There is a plethora of previous works on the performance tuning of systolic arrays, but usually based on a number of oversimplified assumptions (e.g., only considering divisors for loop tiling, pruning based on off-chip data communication) to reduce the design space.

In this paper, we present a comprehensive design space exploration tool named Odyssey for systolic array optimization. Odyssey does not rely on artificial assumptions to limit the design space, and yet it is highly efficient and scalable with a hybrid optimization technique. For example, for a 1024x1024x1024 matrix multiplication, it finds designs that reach 90% of the optimal performance in 5 seconds with a single CPU thread. Moreover, using Odyssey, we unveil and quantify the suboptimality introduced by multiple commonly used oversimplifications in prior studies for systolic array design space exploration. For example, Odyssey results show that limiting to divisors for loop tiling leads to a 39% performance loss, and pruning based on off-chip data movement results in a 45% performance loss. We applied Odyssey to explore the architecture trade-offs for matrix multiplication and convolutional neural network, providing inspiration into possible optimizations for these two applications.

1 INTRODUCTION
Performance optimization for a given class of microarchitectures, also called performance tuning, has long been an important topic given the complexity of hardware systems and applications. This issue is intensified on domain-specific architectures (DSA), which grant designers explicit control over the software stack and hardware architecture, opening up a vast design space to explore.

This paper focuses on the performance tuning of systolic arrays. A complete design space of systolic arrays contains multiple dimensions, such as the selection of dataflows\(^1\), loop permutation and tiling. These factors impact the final design performance in an intertwined manner and compose a vast design space which is intractable to handle manually.

Many previous works have attempted this challenging task by looking into different dimensions of the design space and proposing various auto-tuning methods [4, 9, 17, 19, 21, 28, 31, 41]. However, after a thorough examination of the previous works, we identified several limitations that need to be addressed.

**Limitation 1: Incomplete coverage of the design space.** When selecting the tiling factors, many previous works only considered divisors to reduce the design space [4, 9, 17, 41]. In Figure 1, we compare the throughput and DSP usage of best systolic arrays found when limiting tiling factors to 1) divisors only (Design 1) and 2) both divisors and non-divisors (Design 4) for a 1024 x 1024 x 1024 matrix multiplication (MM)\(^2\). Limiting to divisors leads to a 39% performance loss. With the limited design space, the divisor-only design fails to fully exploit the on-chip resource, with only 60% DSP usage.

**Limitation 2: Inaccurate performance modeling.** An inaccurate performance model could also hurt the quality of search results. For example, the previous work TENET [28] estimated the design latency as the maximum of compute and communication latency. This model overlooks the prologue/epilogue phases when loading the first tile of data and writing out the final results. Figure 1 shows the performance of the best design found when using the maximum-based model (Design 2) for the same MM problem. We observe a 9% performance loss compared to the optimal design.

**Limitation 3: Inefficient search methods and imperfect pruning heuristics.** When searching the design space, many previous works adopted pruning-based exhaustive search which may not scale to large-sized problems [4, 9, 28, 41]. To make matters worse, several works chose imperfect pruning heuristics, failing to cover optimal designs. For example, the previous work Marvel [4] pruned the design space based on the off-chip data communication and applied an exhaustive search in the pruned sub space. However, an optimal design needs to balance both the data communication and computation and does not necessarily minimize the off-chip memory accesses. As a result, the best design found which minimizes the off-chip data communication (Design 3) in Figure 1 introduces a 45% performance loss compared to the optimal design.

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\(^1\)Given a target loop program to map to systolic arrays, designers could select different loops to be mapped to spatial dimensions of systolic arrays, leading to different array topologies and execution models. We define each of such choices as a unique dataflow.

\(^2\)Please refer to Section 4.1 for more details.
All of these limitations affect the quality of search results and further impact the architecture decisions that designers derive based on these results. To overcome this challenge, in this paper, we propose a new automatic design space exploration framework for systolic arrays. Odyssey \(^3\), Figure 2 depicts the proposed tuning flow.

Odyssey leverages AutoSA \([37]\), an open-source FPGA-based systolic array compiler, to construct the design space automatically. AutoSA takes in a C program that describes the target algorithm to Xilinx HLS C \([40]\). We extend the AutoSA framework to generate a design description file that covers the full details of the generated hardware. Odyssey uses this file to create hardware performance models as symbolic expressions of the tuning parameters that can be used by the auto-tuner. Inside the auto-tuner, Odyssey implements a two-stage flow that starts with a mathematical programming (MP)-based optimizer that leverages optimization solvers with a simplified objective function to produce an initial high-quality design, followed by the evolutionary search with the accurate performance models. Odyssey surpasses the previous works in multiple dimensions.

**Contribution 1: A comprehensive design space and accurate performance modeling.** Odyssey covers a comprehensive design space including the selection of dataflows, loop permutation and tiling. Furthermore, Odyssey derives the performance models directly from the compiler-generated hardware with high estimation accuracy. For example, we are able to produce latency models by traversing the ASTs of the generated HLS designs, which achieved a low estimation error of 1.99% compared to the real hardware execution.

**Contribution 2: Efficient auto-tuning methods.** The proposed auto-tuning algorithm does not rely on any artificial assumptions (e.g., divisors tiling factors, pruning based on off-chip data communication) to limit the design space, and yet it is highly efficient with a hybrid optimization technique that combines the MP-based optimization and evolutionary search. We propose a hybrid mutation operation in evolutionary search that takes non-divisor tiling factors into consideration. In addition, we implement a pruning algorithm for loop permutation that trims away inferior designs without omitting the optimal designs. As a result, our search framework can locate designs with high performance in a short amount of time. For example, for the 1024 \(\times\) 1024 \(\times\) 1024 MM, the proposed auto-tuner finds a design that achieves 90% of the optimal performance in 5 seconds with a single CPU thread.

**Contribution 3: A fully automated and open-source framework.** The entire flow is fully automated and open-sourced\(^4\). Odyssey is the first work that is built directly on an open-source systolic array compiler to construct the design space and generate performance models based on real hardware implementations. This guarantees the comprehensiveness and accuracy of the design space modeling, and validity and reproducibility of the search results. In this paper, we show two architecture studies on MM and convolutional neural network (CNN).

The rest of this paper is organized as follows: Section 2 discusses the previous works and covers the basics of AutoSA. Section 3 explains how we construct the design space. In Section 4, we introduce the search methods to explore this design space. Section 5 presents the evaluation results. Section 6 discusses lessons learned from this work and Section 7 states the limitations of this work. Section 8 concludes the paper.

2 BACKGROUND AND RELATED WORK

## 2.1 Design Space

**Design space coverage.** We consider three dimensions of the design space: dataflows, loop permutation and loop tiling. In addition, in this work, we cover non-divisor tiling factors in loop tiling. Many previous works only used divisors for simplicity \([4, 9, 17, 31, 41]\). However, this choice could lead to significant performance loss, as discussed in Section 1.

**Performance model.** The accuracy of performance models plays an important role in performance tuning. In Section 1, we discussed

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\(^3\) Odyssey is abbreviated from **A**utomatic **D**esign space exploration for **S**ystolic arrays.

\(^4\) https://github.com/UCLA-VAST/AutoSA/tree/master/autosa_scripts/odyssey
the issue of using a simplified performance model that overlooks the epilogue and prologue phases of the hardware execution. Table 1 highlights several previous works with a similar issue [9, 28, 31]. In addition, such performance models are usually derived manually which is time-consuming and inaccurate. Odyssey distinguishes itself from the prior works in that it automatically creates performance models by leveraging the AutoSA compiler.

2.2 Search Methods

We classify the search methods into three categories.

**Brute-force methods.** Such methods include random search [5, 31] and exhaustive search with pruning [4, 9, 28, 37, 39, 41]. Brute-force methods face scalability issues with large-scale problems. For pruning-based exhaustive search, imperfect pruning heuristics could lead to inferior designs. In Section 1, we mentioned using off-chip data communication as the pruning heuristic leads to inferior performance. Previous works like [4, 6] used this heuristic.

**Mathematical programming-based methods.** These methods formulate the search task as a mathematical optimization problem and resolve it with optimization solvers [4, 17, 26, 27]. The recent work CoSA [17] modeled the design space as a mixed integer programming (MIP) problem. To accommodate for the formulation requirements of MIP, CoSA set the objective function as a linear combination of several high-order factors such as resource utilization and data communication. The simplified models employed in such approaches will lead to inferior designs. We conducted an experiment in which we model the tuning task for AutoSA-generated designs as a non-linear optimization problem and used the off-the-shelf solver (AMPL [10] with Ipopt [8]) to generate the solutions. The best design obtained from this approach is 1.5× slower than the optimal design obtained by Odyssey (see Section 4.2).

**Iterative methods.** Examples include simulated annealing [5], evolutionary search [43], Bayesian optimization [32], and reinforcement learning [19]. In this work, we examined several iterative search methods and chose evolutionary search given its high sample efficiency and search quality.

An ideal performance tuning framework should achieve: 1) a comprehensive coverage and accurate modeling of the design space, and 2) efficient search methods to explore the design space. The failure in either of the two targets will impact the quality of search results, as well as the architecture conclusions derived from these results. Unfortunately, regardless of the plethora of past studies, we observe no prior work that reached a balance between these two goals. This situation has motivated us to tackle this challenge.

2.3 Review of Automatic Systolic Array Generation

Automatic systolic array generation is an important research topic given the high performance of the systolic array architecture and the complexities of the designing process [3, 11, 12, 25, 29]. The recent work, AutoSA [37], reported the best performance results in this field. AutoSA takes in a C program as the input and applies a sequence of program transformations on this program to build and optimize systolic arrays. The first step space-time mapping assigns space and time semantics to different loops to create a systolic array. The left column in Figure 3 shows two examples for MM. The first example assigns loop i as space loops, leading to a 1D systolic array with I PEs. We assign all the loops below the space loops as time loops that describe the computation inside PEs. The second example maps loops i and j to spatial dimensions, producing a 2D systolic array with a size of I × J. AutoSA identifies all the legal space loops and generates different space-time mapping candidates.

The next step, array partitioning, employs loop tiling on the outermost permutable loops to reduce the array size. The middle column in Figure 3 presents two examples of MM in which the original loops i, j, k are tiled with factors of [2, 2, 2] that leads to a smaller array with a size of 2 × 2. The original computation task is partitioned and executed on this array in sequence. The tiled loops, named as array partitioning loops, can be further permuted which could lead to different array architectures. The first array keeps the original loop ordering < i, 0, j, k, 0 >. Data of matrix C is accumulated along the loop k.0. Consequently, intermediate results are updated on-chip and only written out off-chip on the last iteration of loop k.0. In comparison, the second array uses the loop ordering < i, 0, k, 0, j, 0 >. As different tiles of matrix C are updated at each iteration of loop j.0, we add additional hardware modules in the on-chip I/O network (marked as C(in)) to load in the intermediate results. The third step, latency hiding, tiles parallel loops and permutes them to the innermost to hide the computation latency. And the last step, SIMD vectorization, vectorizes one loop to improve the compute-over-control ratio to amortize the control overheads inside PEs.

With a comprehensive coverage of hardware optimization techniques, AutoSA generates high-performance systolic arrays with comparable or better performance than previous works [37]. However, such a vast design also poses significant challenges to performance tuning. As an example, considering all the available tiling options, the size of design space blows to O(2^49) for a 1024×1024×1024 MM. This challenge has motivated us to develop Odyssey which provides efficient auto-tuning support to explore such a design space.

The subfigure at the bottom-right of Figure 3 summarizes the design space covered by Odyssey. Odyssey explores different dataflows in the space-time transformation and the loop tiling factors in array partitioning, latency hiding, and SIMD vectorization. Odyssey also explores non-divisor tiling factors and loop permutation in the step of array partitioning. When a non-divisor tiling factor is chosen, the original problem dimension is zero padded to be a multiple of the tiling factor. Tiling factors of latency hiding and SIMD vectorization are still required to be divisors as the array dimension is fixed after array partitioning and non-divisor tiling factors at later steps introduce prologue/epilogue phases and costly max/min operations that hurt the design performance.

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Footnote: Previous works [7, 23, 41] used the term dataflow to identify different array topologies and execution patterns, which are equivalent to different space-time mappings within the scope of systolic arrays. In the rest of the paper, we use dataflow to refer to different space-time mappings. We annotate each dataflow in the format of [i, j] that marks the selected space loops for this array.
3 CONSTRUCTING THE DESIGN SPACE

In this section, we discuss how we construct the design space. The current design space considers loop permutation. We can prune the loop permutation orderings without filtering out the optimal designs. The second part of this section covers the details of the pruning heuristics.

3.1 Enhancement to AutoSA

We have extended AutoSA to generate a design descriptor that contains all the necessary information for estimating the design performance. This descriptor contains the following components:

- **Abstract syntax tree (AST):** ASTs of all the hardware modules for latency estimation.
- **Memory information:** Properties of on-chip buffers including buffer size, data type, and memory banking.
- **Compute information:** Information about the PE computation logic, such as the SIMD lanes and computation statements.
- **Array Topology:** Information about the topology of the systolic array, such as the array dimension and the number of different hardware modules. We use this information, along with the memory and compute information for resource estimation.
- **Tuning parameters:** Loop tiling factors to be tuned.

The auto-tuner utilizes this description file to create a Python file containing functions for estimating the design performance. All the performance models are symbolic expressions of the tuning parameters. During the search, the auto-tuner samples the design space and plugs in different tuning parameters into the performance models for assessing the design performance.

3.2 Loop Permutation Pruning

Odyssey explores different loop permutation orderings in the array partitioning. As shown in Section 2.3, different loop orderings may lead to various architecture designs. AutoSA enumerates all the loop permutation orderings. For MM, there are 3! = 6 different orderings to consider. The number grows larger for a more complicated application like CNN.

```plaintext
for (int i = 0; i < I; i++)
for (int j = 0; j < J; j++)
for (int k = 0; k < K; k++)
... // Reduce dead time
... // Reduces off-chip communication
... // Reduces latency hiding
```

Listing 1: Example code of a CNN layer. Batch size and stride are set to 1 here for simplicity.

Listing 1 shows the example code of one CNN layer. The six-level nested loop leads to 6! = 720 different loop orderings. However, as pointed out by previous works [9, 26, 27], among all the loop orderings, many of them are dominated by a few orderings in performance, thus can be safely pruned without leaving out the optimal points. Next, we show that with proper pruning, we can reduce the number of loop orderings to consider for both MM and CNN to only 3.

We consider resource usage and latency when assessing the design performance. Different loop orderings will impact the structure of the I/O network, resulting in different resource usage. In Figure 3, we showed that after hoisting the loop k 0 from the innermost position of the array partitioning loop band, additional I/O modules for transferring the intermediate results of matrix C are added, increasing the total resource usage. The key takeaway is: By placing loops that carry the flow dependences innermost in the array partitioning:

![Figure 3: Example of using AutoSA to generate systolic arrays for MM.](image-url)
loop band, intermediate data are accumulated on-chip, eliminating the resource overheads brought by the additional I/O modules.

Latency-wise, different loop orderings will affect off-chip data communication. We compute the off-chip data movement for the two example designs in Figure 3. For the first ordering \( < i.0, j.0, k.0 > \), final results of matrix \( C \) are only drained out at the last iteration of loop \( k.0 \), leading to a total amount of data movement as:

\[
DM(C) = \left\lceil \frac{I}{T_{J1}} \right\rceil \left\lceil \frac{J}{T_{J1}} \right\rceil T_{J1} \cdot T_{J1}
\]

As for the second ordering \( < i.0, k.0, j.0 > \), the intermediate results of matrix \( C \) are swapped off-chip at each loop iteration of \( j.0 \). We compute the total data movement of matrix \( C \) as:

\[
DM(C) = 2\left\lceil \frac{I}{T_{J1}} \right\rceil \left\lceil \frac{K}{T_{K1}} \right\rceil \left\lceil \frac{J}{T_{J1}} \right\rceil T_{J1} \cdot T_{J1}
\]

To take into account both the inbound and outbound traffic of matrix \( C \), we multiply the factor 2. Compared to the first ordering, the second ordering introduces a higher amount of data movement for matrix \( C \). For communication-bound designs, this could lead to a longer latency. In addition to the loops that carry the flow dependence, loops that carry the read dependence will impact the data communication as well. We use matrix \( A \) as an example. As shown in Figure 3, with the loop ordering \( < i.0, j.0, k.0 > \), at each array partition, we load new array tiles with a size of \( T_{J1} \times T_{K1} \) from array \( A \). In comparison, with the loop ordering \( < i.0, k.0, j.0 > \), data of matrix \( A \) are reused along the loop \( j.0 \). New data tiles are only loaded at each new loop iteration of loop \( k.0 \), reducing the data communication for matrix \( A \) compared to the first ordering. Detailed equations of data movement for matrix \( A \) can be found in Figure 3. The key takeaway is: By placing array partitioning loops that carry the flow/read dependences innermost, data are reused on-chip, reducing the off-chip data communication and design latency.

Putting it all together, we have a complete picture of the pruning strategy.

**Theorem 3.1.** Given a program that can be mapped to systolic arrays, let \( RL(r) \) be the set of array partitioning loops that carry the read/flow dependences associated with the array reference \( r \), and \( NRL(r) \) be the rest of the loops in the loop partitioning loop band, the set of unique loop orderings \( O \) can be obtained as the union of loop orderings in the form of \( < NRL(r), RL(r) > \) for each array reference \( r \). All the other loop orderings are dominated by \( O \) in terms of resource usage and latency. Note that \( RL(r) \) could be an empty set if there is no read/flow dependence associated with \( r \). For this case, the loop ordering is in the form of \( < NRL(r) > \), and is added into \( O \) for consideration.

**Proof Sketch.** Assume the above statement is false, i.e., there is a loop ordering \( o' \) out of the set \( O \) that achieves better performance than loop orderings in \( O \). Then, there exists at least one loop \( I_{j1} \) in \( o' \) that carries the read/flow dependences for a certain array reference \( r \), and is placed above a certain loop \( I_{o1} \) that belongs to \( NRL(r) \). We group all such loops \( I_{j1} \) into a set \( RL'(r) \) and permute them to the innermost of the array partitioning loop band to generate a new loop ordering \( o \) that belongs to \( O \). If \( r \) is associated with flow dependences, \( o' \) introduces additional I/O modules for loading in the intermediate results, increasing the resource usage compared to \( o \). If \( r \) is associated with read/flow dependences, \( o' \) increases off-chip data communication, and could lead to a longer latency than \( o \) if the design is bound with data communication of \( r \). Overall, this loop ordering \( o' \) is dominated by \( o \) in both resource usage and design latency, which contradicts to the initial assumption that \( o' \) dominates loop orderings from \( O \) in performance. \( \square \)

For the MM example, loop \( i.0 \) carries the read dependence for array \( B \), loop \( j.0 \) carries the read dependence for array \( A \), and loop \( k.0 \) carries the flow dependence for array \( C \). In total, there are three loop ordering candidates which lead to systolic arrays with potentially different performance. Note that as long as the innermost loop is fixed, the ordering of other loops will not impact the performance. In the rest of this paper, we use the annotation \( < i.0, j.0, k.0 > \) to identify the set of loop orderings. All the loops in the same brackets can be permuted freely with equivalent performance. We will choose one ordering randomly in practice. Table 2 shows all the unique loop orderings for MM and CNN.

To summarize, given an input program, we use AutoSA to generate different dataflows and loop permutation orderings of the array partitioning loops, and leave the tiling factors as tunable parameters to be handled by the auto-tuner. The next section will discuss the details of the auto-tuner.

**4 SEARCHING THE DESIGN SPACE**

4.1 Evolutionary Search

In the Odyssey framework, we select evolutionary search as the backbone search method. Evolutionary search [16] is a generic meta-heuristic algorithm inspired by biological evolution, in which individuals of a population gradually improve themselves through a series of biological mechanisms such as mutation, crossover, and selection. In the context of hardware design space exploration, each design point is termed as an individual in the population. The feature vector that describes a design point is coined as the genome of the individual. Each design point is assigned a fitness score by its performance assessed by the real hardware measurement or the performance model. At each iteration, we select a group of individuals with the highest fitness scores in the population as the parents to produce the children in the next iteration (selection). These parents will breed new individuals with mutation and crossover operations. In the next iteration, we filter out the low-fitted individuals and repeat the same reproduction process until finding the satisfactory solutions.

**Encoding scheme.** Each individual is encoded by the tiling factors used in AutoSA compilation passes.

**Mutation.** Figure 4 shows one example for MM. We first compute the updated loop bounds with the current tiling factors. The mutation process operates on the values of the loop bounds. We

| Application | MM | CNN |
|-------------|----|-----|
| Dataflows   | \([i.0, j.0, k.0] \) | \([i.0, k.0, j.0] \) |
| Loop Permutation | \(<i.0, j.0, k.0>\) | \(<i.0, k.0, j.0>\) |
| #Designs    | 18 | 30  |

Table 2: Unique systolic arrays generated by AutoSA for MM and CNN.
implement two mutation methods: factorization-based mutation and random mutation.

1) Factorization-based mutation: We randomly choose one loop \( l_1 \), divide it by a random divisor \( \alpha \) (\( \alpha \) is an integer), and multiply \( \alpha \) to another loop \( l_2 \) that is derived from the same loop as \( l_1 \). For example, in Figure 4, we select the loop \( l_2 \) and divide it by 2, then we choose the other loop \( l_1 \) and multiply its current value with 2. The factorization-based mutation keeps the product of the tiled loop sizes unchanged, guaranteeing the mutated program is always valid.

The factorization-based mutation always chooses the divisors of the loop bounds. While such an implementation is common in many previous works [9, 17, 31, 41], it could result in a reduced design space with inferior performance. Table 3 compares the best systolic array designs, it is usually hard to have a close-formed performance model suitable for the solvers as the objective function. Instead, previous works chose different high-order functions that impact the performance as the objective functions [4, 17, 27]. We conducted an experiment on evaluating the effectiveness of several objective functions.

2) Random mutation: We randomly select one loop \( l_1 \) and mutate this loop by changing the loop bound to a random value \( s \in [1, l_1] \). Next, we select another corresponding loop \( l_2 \) and change its loop bound to a new value \( s' \) computed by \( s' = \text{ceil}(l_2 \times s) \).

We show one example of random mutation in Figure 4. In the right example, we select the loop \( j \times 2 \) and change its original loop size from 8 to 6. Then we choose the other loop \( j \) to mutate. We compute the new loop bound for \( j \) as \( \text{ceil}(4 \times 8/6) = 6 \). As a result, the tiling factor \( T_{j1} \) is changed from 32 to 36, which is a non-divisor of the problem size \( f = 64 \). The random mutation method adjusts two loops at the same time as an effort to keep the product of these two loops with minimal changes. The use of \( \text{ceil}() \) function guarantees the new product is no less than the original product so that the mutated program is always legal.

When performing the mutation, we assign a probability \( \alpha \) to execute the factorization-based mutation and the probability \( 1 - \alpha \) to the random mutation. Based on a grid search, we set \( \alpha \) to 0.4 by default.

Crossover. The crossover operation exchanges the genomes of two individuals. To guarantee the validity of the offspring, we exchange the tiling factors associated with the same original loop together.

### 4.2 Mathematical Programming

Although the mathematical programming (MP)-based method fails to identify the optimal design, the design it finds achieves relatively good performance and could be used as the initial population of evolutionary search. Odyssey implements a MP-based optimizer to produce high-quality seeds to evolutionary search. We formulate the optimization problem as follows.

#### 4.2.1 Constraints

A valid hardware design should not overuse the available memory and computation resource. For FPGA designs, we consider the BRAM and DSP usage.

\[
U_{\text{mem}} \leq M_{\text{available}}, U_{\text{DSP}} \leq D_{\text{available}} \tag{3}
\]

**Memory resource.** We model the memory usage as:

\[
U_{\text{mem}} = \sum_{m \in \text{Modules}} U_{\text{mem}}(m) \times N_m \tag{4}
\]

which is a sum of the memory usage of each type of hardware module \( m \), computed by multiplying the memory usage of module \( m (U_{\text{mem}}(m)) \) with the total number of such modules \( N_m \).

**Computation resource.** We compute the DSP usage as:

\[
U_{\text{DSP}} = \sum_{m \in \text{Modules}} U_{\text{DSP}}(m) \times N_m \tag{5}
\]

\[
U_{\text{DSP}}(m) = \sum_{op \in \text{ComputeOps}} \text{SIMD}(op) \times U_{\text{DSP}}(op) \tag{6}
\]

We calculate the total amount of DSPs as a sum of the DSPs consumed by all the hardware modules and the per module DSP usage \( U_{\text{DSP}}(m) \) is computed as a sum of the products of SIMD factor \( \text{SIMD}(op) \) of each computation operator \( op \) and the number of DSPs consumed by each single SIMD lane \( U_{\text{DSP}}(op) \). We maintain an internal database for the per operator DSP usage \( U_{\text{DSP}}(op) \).

#### 4.2.2 Objective Function

Given the high complexity of the hardware designs, it is usually hard to have a close-formed performance model suitable for the solvers as the objective function. Instead, previous works chose different high-order functions that impact the performance as the objective functions [4, 17, 27]. We conducted an experiment on evaluating the effectiveness of several objective functions.

**Objective 1: Computation resource.** We use the total DSP usage \( U_{\text{DSP}} \) as the optimization target. The heuristic is that a design with higher performance should utilize more DSPs.

\[
\text{Obj1} : \min(-U_{\text{DSP}}) \tag{7}
\]
Objective 2: Off-chip communication. We aggregate the off-chip data movement of all the arrays in the program.

\[
\text{Obj2} : \min \sum_{a \in \text{Arrays}} DM(a) \tag{8}
\]

Objective 3: Off-chip communication - computation resource. This objective function takes both computation and communication into consideration. Ideally, we would like to maximize the computation resource and reduce the off-chip communication.

\[
\text{Obj3} : \min \left( \sum_{a \in \text{Arrays}} DM(a) - U_{\text{DSP}} \right) \tag{9}
\]

We use the off-the-shelf solver (AMPL [10] with Ipopt [8]) to implement the optimization problem. All the metrics have been normalized. The best solution obtained from the solver is then fed to the evolutionary search as the initial population. Figure 5 shows the search traces of evolutionary search with different optimization targets. Table 4 compares the performance of designs found by solvers.

As seen in the figure, all three objective functions help reduce the convergence time and yield better results compared to the evolutionary search-only method (annotated as No Solver). Specifically, Obj3 helps significantly reduce the convergence time. With Obj3, the auto-tuner locates a better design than the baseline (No Solver) within 2000 epochs. In Odyssey, we use the Obj3 as the optimization target of the solver. The implications from this experiment are multi-fold.

First, MP-based methods are insufficient to find optimal designs. As demonstrated in Table 4, the best design identified by the MP-based approach is 1.5x slower than the design discovered by Odyssey with a hybrid search method that combines both mathematical programming and evolutionary search.

Second, the optimal design does not necessarily minimize the off-chip data communication. In Table 4, the best design found by Odyssey introduces 4.9x more off-chip data communication than designs identified by Obj2 and Obj3.

In this section, we evaluate the performance of the Odyssey framework. We first validate the performance models from Odyssey against the real hardware. Then, we compare the proposed auto-tuning method with several other search methods to assess its efficiency. Lastly, we use Odyssey to investigate the architecture trade-offs of systolic arrays on MM and CNN.

5.1 Performance Model Validation

5.1.1 Approaches.

Workloads. We evaluate the accuracy of the hardware models derived from Odyssey on two important workloads in HPC and deep learning, MM and CNN. Table 5 details the parameters for the chosen workloads. We choose a relatively small problem size in consideration of the long RTL simulation time. All the experiments in this paper target Xilinx Alveo U250 FPGA.

Baselines. We measure the design latency by RTL simulation. We use the reported resource numbers from the HLS synthesis reports as the baseline for resource models.

Designs. We validate all 18 and 30 different designs generated for MM and CNN by AutoSA, as listed in Table 2. To select the tiling factors, we randomly sample the design space. We compare the performance numbers estimated by the models derived from Odyssey against the numbers measured by RTL simulation and HLS synthesis.

5.1.2 Validation Results. Figure 6 compares the model-predicted performance numbers against the measured numbers for all the designs. The performance models generated by Odyssey are highly accurate, with estimation error rates of 1.99%, 0%, and 0% for latency, BRAM, and DSP, respectively.

5.2 Auto-Tuning Evaluation

5.2.1 Approaches.
Workloads. We evaluate the performance of the proposed auto-tuning method using a $1024 \times 1024 \times 1024$ MM.

Baselines. We use the following methods as baselines.

- **Random search.** We randomly sample the design space and update the best solutions.
- **Exhaustive search with pruning.** We extend the random search by pruning the design samples based on the DSP utilization. As the smallest design among the 18 designs uses 30% of DSPs, we set the DSP pruning threshold to 25%.
- **Simulated annealing.** We use the Python package [33] as the baseline. Based on a grid search, we designate the hyperparameter temperature $T$ to be 200. We implement a customized step-taking function using the proposed hybrid mutation method for evolutionary search.
- **Bayesian optimization.** We use the Python package [30] as the baseline.
- **OpenTuner [1].** OpenTuner is an auto-tuning framework built on an ensemble of several efficient search techniques. It has been demonstrated effective in cases such as searching the GCC compilation flags and optimal schedules for Halide programs [1]. We use the latest release of OpenTuner from its Github repository [2].
- **Reinforcement learning (RL).** RL is a machine learning algorithm that can be used for hardware optimization. The previous work ConfuciuX [19] implemented a two-step search algorithm for tuning the dataflow architectures which employs RL as the first step to locate a good sub design space and utilizes evolutionary search to perform a more fine-grained search later to find the best design. We use the open-source implementation from ConfuciuX as the RL baseline [20]. ConfuciuX applied a 3-layer multi-layer perceptron (MLP) neural network for the policy network.

Designs. We compare our tuning methods against the baselines on all 18 different designs generated for MM by AutoSA.

Evaluation method. For each systolic array design, we run the search method for 5 minutes and repeat it 3 times. The final results are averaged from the 3 runs. All the search methods are executed with a single CPU thread. RL baseline uses Pytorch which implements multi-threading during the training of MLP. All experiments are executed on a workstation with Intel Xeon E5-2680 v4 CPU.

5.2.2 Results.

Search results quality. Figure 7 compares the best throughput (1/latency) achieved by each tuning method on the 18 systolic array designs. The throughput is normalized against the optimal performance found by exhaustive search. Odyssey found designs that achieve more than 95% of the optimal performance for 13 designs out of the total 18 designs. For the remaining 5 designs, the performance gap is within 1% of the best performance identified by other baselines (OpenTuner and simulated annealing). Overall, Odyssey locates designs that achieve more than 95% of the optimal performance.

Sample efficiency. In addition to the high-quality search results, Odyssey achieves high sample efficiency. Figure 8 compares the convergence traces of all the tuning methods on the design with the highest optimal throughput. As shown by the figure, Odyssey finds a good design configuration resulting in 93% of the optimal performance after evaluating 3000 design samples. Simulated annealing earns the second-best performance, locating a design that reaches 66% of the optimal performance.

Search time. Lastly, Figure 9 shows the performance of the best designs located by Odyssey in 5 seconds. Odyssey finds designs achieving over 90% of the optimal performance for all the designs in 5 seconds with a single CPU thread.

5.3 Application 1: MM

In this section, we perform a detailed architecture comparison of different systolic arrays for matrix multiplication. Figure 10 displays the normalized throughput and design usage of different systolic arrays for MM. We draw the following conclusions from this figure.

**Loop permutation.** The loop permutation ordering $\langle i, j, k \rangle \rangle$ dominates the performance across different dataflows. The major reason for such a performance gap is the extra memory consumed
by the two other loop orderings. As discussed earlier in Section 3.2, the loop orderings < [j, k], i > and < [i, k], j > introduce additional I/O modules for loading in the intermediate results, leading to a higher memory usage than the loop ordering < [i, j], k >. Table 6 illustrates the resource usage breakdown for three designs with the same dataflow [i] and different loop permutation orderings. As shown in the table, designs with loop orderings < [j, k], i > and < [i, k], j > allocate more BRAMs to I/O modules for matrix C, which limits the size of array (#PE), leading to a poorer performance than the ordering < [i, j], k >.

Dataflow. Among the designs with the same loop ordering, the dataflow [i, j] achieves the best performance because the dataflow [i, j] exploits the most degrees of parallelism from the application. For MM, we vectorize the loop k for all the designs which serve as the first degree of parallelism. The space dimensions of the systolic array exploit the rest of the degrees of parallelism. 1D systolic arrays can exploit at most one more degree of parallelism. In comparison, the dataflow [i, j] exploits two more degrees of parallelism (i and j). Other 2D systolic arrays ([i, k] and [j, k]) include k in the space dimensions such that they could extract at most one more degree of parallelism as similar as 1D parallelism. More dimensions of parallelism help cover more profitable designs that fully utilize the on-chip resource. As seen in Figure 10b, the dataflow [i, j] utilizes the most DSPs, achieving the highest throughput among all the designs.

5.4 Application 2: CNN

In the previous section, we perform a detailed performance analysis of different systolic array designs for MM. This section applies the same mythology and compares the performance of different systolic arrays for CNN.

As shown in Table 2, Odyssey produces 30 different designs for CNN. We evaluate these designs on the VGG16 network [35]. The VGG16 network includes 13 convolutional (CONV) layers and 3 fully-connected layers. We only examine the mapping of CONV layers in this work. We annotate the 13 CONV layers as CONV[1-13] following their order in the network. Figure 11 presents the detailed evaluation results of the first 2 CONV layers of VGG16. We make the following conclusions from this figure.

Loop permutation. Consistent with the observation from the MM case study, designs with the loop ordering < [o, h, w], [i, p, q] >, which eliminates the additional I/O modules for transferring the intermediate results of output feature maps, result in the best performance across all the dataflows.

Dataflow. The performance of different dataflows varies across CONV layers. On CONV1, we observe that dataflow [h, i] delivers the best performance. However, on CONV2, dataflows [o, h] and [o, w] dominate other designs. Below, we examine the best designs on these two CONV layers in detail.

Figure 12 depicts the detailed architectures of these two designs. AutoSA implements a multi-level I/O network for transferring the data (e.g., L1, L2, L3). To increase the I/O throughput, we pack multiple data elements between the I/O modules. A larger I/O bus width introduces more hardware resources. As a consequence, the bus width gradually increases at higher levels as a trade-off between the data transfer throughput and hardware resource.
Table 7 summarizes the performance details of two designs with dataflows \([h, i]\) and \([o, h]\) on first two CONV layers. On CONV1, the design latency of dataflow \([o, h]\) is bound by the data transfer latency of the L1 I/O modules that drain out the output feature maps \(f_o\). In comparison, in dataflow \([h, i]\), data of \(f_o\) are accumulated across PEs and drained out by L2 I/O modules. As more data are packed between the L2 I/O modules than L1 I/O modules (32 Bytes vs. 8 Bytes), the I/O network is no longer the performance bottleneck for dataflow \([h, i]\). Instead, the performance loss comes from the zero padding on the input channel dimension \(i\). The best first-level tiling factor \(T_{L1}\) for both dataflows is 4. As a consequence, the input dimension \(i\) is padded from 3 to 4 for both dataflows, introducing 25% computation overheads.

On CONV2, the I/O network is no longer the performance bottleneck for the dataflow \([o, h]\). The design is compute-bound as the input dimension \(i\) increases from 3 to 64 on this layer and there is more computation inside the PEs on accumulating the intermediate results along the \(i\) dimension. We see from Table 7 that PE latency now dominates the design. On this layer, dataflow \([h, i]\) delivers a slightly lower performance than the \([o, h]\) due to the fewer degrees of parallelism to explore. Both dataflows vectorizes the loop \(i\). The dataflow \([o, h]\) explores two more levels of parallelism by mapping the loops \(o\) and \(h\) to space dimensions. In comparison, dataflow \([h, i]\) only exploits one more level of parallelism on the loop \(h\). With more degrees of freedom to use in the design space, we are able to find a design which utilizes more DSPs and achieves a higher performance.

Finally, Figure 13 presents the best throughput attained by systolic arrays with different dataflows on VGG16. We fix the loop ordering to \(<[o, h, w], [i, p, q]>\) for all dataflows. Figure 14a computes the geometric mean of the best throughput of each dataflow over the entire network.

Overall, we observe that 2D systolic arrays achieve a higher performance than 1D arrays with more degrees of parallelism to exploit. Dataflows \([o, h]\) and \([o, w]\) deliver the best performance among all the dataflows, followed by \([o, i]\), \([h, i]\), and \([w, i]\). The best average throughput of a single dataflow on VGG16 is 77% of the peak layer-wise throughput obtained on the entire network. This is due to the divergent problem sizes of each CONV layer that limit the performance of a single systolic array. We applied the same methodology on another CNN, ResNet50 [14], and summarized the results in Figure 14b. ResNet50 is more compact than VGG16, with less parallelism and data locality to exploit. This results in a reduction of the best average throughput of a single array to 57% of the peak layer-wise throughput on ResNet50.

Ideally, we would like to achieve 100% average throughput such that computation resource is fully utilized for each CONV layer. However, in reality, we ended with only 77% and 57% for VGG16 and ResNet50, respectively. This indicates that mapping CNNs to a single systolic array will face the issue of resource underutilization. Several previous works also identified this issue [18, 24, 38, 42]. In terms of solutions, TPU chose to increase the batch size to improve the overall throughput [18]. On FPGAs, previous works like DNNExplorer [42] implemented a multi-array architecture that customizes each smaller array to different CONV layers to improve the overall throughput.

6 LESSONS LEARNED FROM THIS WORK

This section summarizes four major lessons we learned from this work.

Lesson 1: Incomplete and inaccurate design space modeling could lead to inferior search results and skewed architecture conclusions. We have demonstrated that considering only divisor tiling factors or overlooking the prologue and epilogue phases could lead to inferior designs. This could further hurt the validity of the architecture conclusions derived from these results. For example, Figure 15 illustrates the search results for MM with only divisor tiling factors. With the limited design space, the best systolic array design only uses 60% of the DSP. Furthermore, architects may draw skewed conclusions from these results such as all three 2D array dataflows achieve the equivalent performance, which contradicts to the findings as seen in Figure 10.

Lesson 2: A high-performance design needs to balance computation and communication. We show that the latency-optimal design does not necessarily minimize the off-chip data communication and both computation and communication need to be considered. Several previous works [4, 6] that used the off-chip communication to prune the design space may leave out the optimal designs, leading to inferior performance.

Lesson 3: Iterative search methods can be enhanced with mathematical programming solvers. Iterative methods achieve high sample efficiency and are portable to different search problems. It can be further enhanced with mathematical programming solvers. We have...
demonstrated that a MP-based optimizer which uses a simplified objective function that considers data communication and computation resource can effectively boost the convergence of evolutionary search. Although this work only focuses on systolic arrays, the methodology is general, and designers can apply it to performance tuning tasks for other applications and hardware architectures.

Lesson 4: Compiler-assisted design space construction improves productivity and performance. To the best of our knowledge, Odyssey is the first work that constructs the design space of systolic arrays with an open-source compiler that generates real hardware designs. This approach guarantees the validity and accuracy of search results and improves the productivity. In the recent years, we have seen an emergence of domain-specific language compilers for DSAs [11, 13, 22, 36]. We believe the methodology in this work could provide valuable insights to further enhance the performance tuning of these works and enable a wider adoption of DSAs in the post Moore’s law era.

7 LIMITATIONS

The current framework limits the input programs to ones with rectangular iteration domains. For programs with non-rectangular iteration domains, such as LU decomposition, programmers need to implement the design performance models in Python manually and supply it to the auto-tuner. We will address this limitation in the future work.

8 CONCLUSION

This paper presents Odyssey, an automatic design space exploration framework for systolic arrays. Odyssey covers a comprehensive and accurate design space of systolic arrays and incorporates a hybrid search method consisting of the MP-based optimizer and evolutionary search. Furthermore, it implements an effective loop permutation pruning algorithm that helps reduce the design space without leaving out the optimal designs. With Odyssey, we unveil the limitations of several commonly used assumptions by previous works in the performance optimization of systolic arrays. We have also conducted an architecture analysis of systolic arrays on two applications, MM and CNN. Although this work focuses on the systolic array architecture, the methodology and insights can be applied to other hardware and architectures as well. Future work includes extending the Odyssey framework to support applications with non-rectangular iteration domains.

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