Charge Pump and Loop Filter for Low Power PLL Using 130nm CMOS Technology

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Abstract. A tri-state charge pump circuit and second order low pass filter circuit were designed to be used in Phase Lock Loop (PLL) system. The proposed design reduces the non-ideal effects such as a current mismatch and charge sharing. Therefore, it can be minimized by providing an equal value for the two switches UP and DOWN. While the charge pump output determines the output condition of the low pass filter. The proposed design have been simulated by using 130nm Complementary Metal Oxide Semiconductor (CMOS) technology in Cadence Tools. The simulation also includes the parameters for tri-state charge pump and second order low pass filter using voltage supply of 1.2 V. The power consumption of the design is 2.07 mW with the output voltage swing from 288 mV to 413.8 mV. The frequency achieved from the proposed design is 4.7 GHz. The total area of the layout that have been measured is 31.4 µm x 22.6 µm (0.7096 mm²). Thus, the proposed design able to achieve the scope of low power consumption and high frequency in smaller technology.

1. Introduction

Phase Lock Loop (PLL) is a system that consists of three major parts; Phase Frequency Detector (PFD), Charge Pump and Loop Filter, and Voltage Controlled Oscillator (VCO). A PLL is highly preferred because it is a feedback system that compares the output frequency from the input frequency and can survive in a single chip. A PLL is normally used in well-timed clock generator, recovery of signal from noisy communication channel and high performance wireless with additional application in PLL’s parts [1]. Figure 1 shows the basic block diagram for a PLL system.

The charge pump circuit is connected with loop filter and located within PFD and VCO. Charge pump is functioning as a converter for the logic states of the PFD into an analog signal in order to control the VCO. The frequency of the VCO is controlled by the output signal of the charge pump circuit. The output voltage of the charge pump circuit must be held at a constant voltage, when PLL locks in some frequency. The charge pump consists of two switched current source that pump charge in or out of the loop filter according to two logical inputs.

Loop Filter circuit is also important to the performance of the PLL because it removes high frequency noise of the detector, influences the hold and captures ranges, and influences the switching speed of the loop in lock [2]. Loop filter convert the output signal of phase frequency detector to control voltage and reduce the ripple from the charge pump. A charge pump circuit along with low pass filter is used to minimize the disturbances at the input of current-starved voltage controlled oscillator (CS-VCO) and to get a sharper and smoother signal at the CS-VCO output.
2. Charge Pump Circuit

A charge pump circuit consists of two symmetrical current sources that are controlled by the PFD output, and it will convert the sequential logic state of PFD into analog signals that are suitable to control VCO [5]. It also carries the phase error between the reference and the divided signal into analog quantities or current pulses. There are several types of charge pump, for example, conventional charge pump, current steering, different input with single-ended output and high voltage charge pump.

From previous studies, most of the charge pump circuit that have been used are basic charge pump with two switches, ideal charge pump, Dickson charge pump and so on. Figure 2 shows an ideal charge pump that gives the output frequency of 1.5 GHz and input voltage of 90 mV. Table 1 shows the operation of ideal charge pump.

| UP Signal | DN Signal | Condition     | Note                      |
|-----------|-----------|---------------|---------------------------|
| 1         | 0         | Charging      | \(I_{op}\) flows into filter |
| 0         | 1         | Discharging   | \(I_{op}\) flows out from filter |
| 0         | 0         | Vout constant | \(I_{op} = 0\)             |
| 1         | 1         | Vout constant | \(I_{op} = \text{not} 0\)  |
Charge pump circuit used in [6] is a Dickson charge pump that causes the output voltage to be higher than the input voltage as shown in Figure 3. It is consists of capacitors and MOS switches. The two-stage charge pump is used as a step-up converter to prevent problems at the threshold voltage. By using 3.3 V input voltage, this charge pump produces 6.3 V of output voltage and more than 100 mA of load current.

![Dickson Charge Pump Diagram](image)

Figure 3. Dickson Charge Pump [6]

Tri-state charge pump also have been used in PLL system. There are a few architectures for charge pump. For example, a conventional tri-state that consist of three topologies of switch in source, gate and drain. This type of charge pump consumes lower current depending on the frequency of the PFD. Figure 4 shows the transistor level for conventional tri-state charge pump with the three topologies. After one of the topologies have been properly biasing, the output voltage gained in the range of 0.5 V to 2.5 V with 3 V supply.

![Tri-state Charge Pump Diagram](image)

Figure 4. Conventional tri-state charge pump with different topologies. (a) Switch in drain (b) Switch in Gate (c) Switch in Source.

### 3. Loop Filter Circuit

Loop filter needs to be chosen properly with the correct value to prevent inappropriate values that may either lead the loop to oscillate for long without reaching the locked state or small variations in the input data may cause the loop to unlock. From the previous studied, there are several types of loop filters have been designed. For example, passive and active low pass filter [1], inductor-capacitor (LC) filter [10], first order passive lag filter [4], simple resistor and capacitor (RC) low pass filter [6]. Figure 5 shows the second order loop filter while Figure 6 shows the lag filter from the previous studies.
4. Proposed Design Architecture

The Charge Pump in a PLL design is constructed in an integrated circuit technology consisting of pull-up and pull-down transistor and on-chip capacitor. The output from the PFD provides UP and DOWN gating signals that work as switches so that when UP is ON then DOWN is OFF. It only works on either way. Low Pass Filter is a filter that builds with a resistor and capacitor that pass through the low-frequency signals and also blocking high frequency signals. The capacitor is a reactive device that offers very high resistance to low frequency signal and vice versa. Since the current always takes the path with lowest resistance, the capacitor that represents a low resistance in a circuit for high frequency signal will build its path. Figure 7 shows the block diagram for charge pump and loop filter.

4.1 Tri-state Charge Pump Circuit

Tri-state charge pump are commonly known as the low current consumption depends on the frequency of the PFD. This tri-state charge pump consists of one inverter, one amplifier and a total of five transistors. When the input is low, the current pump into filter also low. Thus, an amplifier was added as shown in Figure 8 where the amplifier was placed in between switch UP and the inverter to increase the amplitude of the voltage and the current signal of the circuit. The equal values for switch UP and DOWN are provided to prevent the current mismatch for the proposed charge pump circuit. For this 130 nm CMOS technology, this circuit is using 1.2 V supply voltage. The delay given to switch UP and DOWN is 100 ps and 500 ps respectively as shown in Table 2.
Table 2. Properties for Switch UP and DOWN

|                   | UP  | DOWN |
|-------------------|-----|------|
| DC Voltage (V)    | 1.0 | 1.0  |
| Voltage 1 (V)     | 200m| 200m |
| Voltage 2 (V)     | 1.0 | 1.0  |
| Delay (s)         | 150p| 150p |
| Rise Time (s)     | 10p | 10p  |
| Fall Time (s)     | 10p | 10p  |
| Pulse Width (s)   | 5n  | 5n   |
| Period (s)        | 1n  | 1n   |

4.2 Second Order Low Pass Filter Circuit

Loop Filter for a PLL system needs to be chosen wisely to prevent the locked loop to be unlocks due to the inappropriate value and small variations in the data input [5]. The main function of the loop filter used, second order low pass filter, which converts the current generate from the charge pump into a controlled voltage signal for controlling the VCO after it filters out the noise. Loop filter is used to overcome the noise and high frequency signal component from the charge pump and stabilize the loop. Figure 9 shows the schematic circuit for second order low pass filter.

By referring to the method introduced by Ken Holladay [9], the parameter values for the loop filter must be defined in order to design the basic requirement. For this PLL design, the frequency range is 3.1 GHz to 5.1 GHz and the VCO sensitivity, \( K_{VCO} \) are assumed at 10 kHz. The charge pump current, \( I_{CP} \) is at 5 \( \mu \)A while the PLL loop bandwidth, \( BP_{PLL} \) is 100 kHz.

\[
F_{step} = F_{osc\ max} - F_{osc\ min}
\]

\[
N = \frac{F_{osc\ max}}{F_{step}}
\]

The frequency step, \( F_{step} \), is obtained by subtracting the maximum oscillator frequency and minimum oscillator frequency and the value of \( N \) is obtained when the \( F_{osc\ max} \) is divided by \( F_{step} \). The \( F_{step} \) obtained from the calculation is 2 GHz and the value of \( N \) is 2.55. Considering the damping factor, \( \xi \), is typically at 0.707 therefore equation (3) will calculate the natural frequency, \( F_N \), that is equal to 30.01 kHz.
From Equation (4), (5) and (6), the value of the capacitor, $C_1$ is defined by calculating the value of $C_2$ and $R_1$. Thus, the value of $C_2$ and $R_1$ is 551.49 fF and 19.35 kΩ respectively. The value of $C_1$ is equal to 55.1 fF.

$$C_2 = \frac{I_{CP} \times K_{VCO}}{N \times (2\pi \times F_N)^2}$$

(4)

$$R_1 = 2 \times \xi \times \sqrt{\frac{N}{I_{CP} \times K_{VCO} \times C_2}}$$

(5)

$$C_1 = \frac{C_2}{10}$$

(6)

Equation (7) is the equation to calculate, $T_s$, the time desired for the filter to step to the new frequency. The frequency of the carrier within the desired time after a step, $F_a$, is normally in 1000 Hz. Thus, the value of $T_s$ is equal to 54.42 µs or 50 µs.

$$T_s = \frac{-1 \times \left( \ln \frac{F_a}{F_{step}} \right)}{F_N \times 2\pi \times 2\xi}$$

(7)

From the value of $R_1$, $C_1$ and $C_2$ calculated above, the frequency cutoff, $f_c$, for this proposed design are calculated by using Equation (8). Thus, frequency cutoff is 6.53 GHz.

$$f_c = \frac{1}{2\pi \sqrt{R_1 C_1 C_2}}$$

(8)

5. Results and Discussion

This proposed design of charge pump and loop filter was designed in CMOS 130 nm technology and operates at 1.2V power supply. Figure 10 shows the combined circuit of the tri-state charge pump and second order low pass filter. The charge pump output determined the condition of the capacitor in low pass filter is charged or discharged.

![Combined Circuit of Charge Pump and Loop Filter](image)

The result gained from the tri-state charge pump and second order low pass filter has been plotted as shown in Figure 11. The waveform plotted is almost in ideal behavior with a glitch or noise in it. From the waveform, by using the Result Browser in WaveView in Cadence Tool, the power consumption was
plotted at 2.07mW with voltage supply of 1.2V as shown in Figure 12. The power consumption gained is within the range of the scope wanted.

![Figure 11. The output waveform for the proposed design.](image1)

![Figure 12. The power consumption of the proposed design is 2.07 mW.](image2)

This circuit also has been tested in different voltage supply which is 1.0 V, 1.2 V, and 1.8 V. The different usage of power supply can produce different power consumption as shown in Table 3. By using voltage supply of 1.0 V, smaller power consumption was consumed compared to 1.2 V, where the power consumption is 2.07 mW. Meanwhile, Figure 13 shows the plotted frequency that is measured at 4.7 GHz by using Calculator in the Analog Design Environment. Figure 14 shows the layout for tri-state charge pump and low pass filter that have been arranged. From the figure, the charge pump area is smaller than loop filter area. This is because the loop filter is using analog components, which is a resistor and capacitor. The total area of the layout that have been measured is 31.4 µm x 22.6 µm (709.6 µm²). The impairment that Figure 15 is the comparison of power consumption and frequency that have been plotted.

![Figure 13. The output waveform for the proposed design.](image3)

![Figure 14. The power consumption of the proposed design is 2.07 mW.](image4)

![Figure 15. The output waveform for the proposed design.](image5)

### Table 3. Comparison of Different Values of Voltage Supply.

| Voltage Supply (V) | Average Power (µW) | Power Consumption (mW) |
|--------------------|--------------------|------------------------|
| 1.0                |                    |                        |
| 1.2                |                    |                        |
| 1.8                |                    |                        |
| Value  | Frequency (GHz) |
|--------|----------------|
| 1.0    | 1.72           |
| 1.2    | 1.956          |
| 1.8    | 4.0            |

**Figure 13.** The plotted frequency of the proposed design.

**Figure 14.** Layout of Tri-State Charge Pump and Low Pass Filter
There is a lot of technique used by charge pump and loop filter whether in PLL system or not. But, most of the techniques used 180nm CMOS technology and above. Power consumption of the proposed design is improved about 58.6% compared to ideal charge pump and low pass filter. Basic charge pump and high pass filter improved about 69.38% when compared to the proposed design and also compared to other. Last but not least, bipolar switched charge pump and loop filter only focus on the power consumption of the whole system. The difference is about 69.05% compared to the proposed design.

6. Conclusion

A tri-state charge pump and second order low pass filter has been designed by using Cadence Tools in 130nm CMOS technology. For the proposed designed, the aim of the power consumption and frequency required are achieved. The power consumption achieved is 2.07 mW with the range of frequency is from 3.1 GHz to 5.1 GHz and frequency achieved is 4.7 GHz. From the final design, the area measured for the whole tri-state charge pump and low pass filter is 31.4 µm x 22.6 µm (709.6 µm²).

Acknowledgement

This work was financial supported by FRGS Grant Vot Number 1538.

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