A Design for Testability of Open Defects at Interconnects in 3D Stacked ICs

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SUMMARY A design-for-testability method and an electrical interconnect test method are proposed to detect open defects occurring at interconnects among dies and input/output pins in 3D stacked ICs. As part of the design method, an nMOS and a diode are added to each input interconnect. The test method is based on measuring the quiescent current that is made to flow through an interconnect to be tested. The testability is examined both by SPICE simulation and by experimentation. The test method enabled the detection of open defects occurring at the newly designed interconnects of dies at experiments test speed of 1 MHz. The simulation results reveal that an open defect generating additional delay of 279 psec is detectable by the test method at a test speed of 200 MHz beside of open defects that generate no logical errors.

key words: 3D stacked IC, open defects, design-for-testability, through-silicon via, electrical interconnect test

1. Introduction

Much attention has been paid to 3D stacked ICs, due to both their high speed operation and their low power dissipation\([1]\). The ICs are fabricated by stacking dies that are connected with Through Silicon Vias (TSVs) and micro solder bumps\([2]\).

The IC dies are fully tested prior to stacking. Only dies that had been judged as known good dies (KGDs) are stacked in such fabrications. However, open defects may occur at interconnects between KGDs during the TSV forming process as well as during the stacking process\([1, 3]\).

The open defects are classified into hard open defects and soft open ones. A soft interconnect open defect is modeled as a finite resistance path, since logic signals propagate through the defective interconnect with an additional propagation delay time\([3]\). The soft open defect is referred to in this paper as a “hard open defect”. If the gap is short, the two parts are modeled as two resistors connected via a capacitor. In such a case, a high speed logic signal does propagate through the capacitor\([4]\). The defect is called in this paper a “capacitive open defect”.

This paper discusses how to detect the above three types of open defects occurring at interconnects among dies and input/output pins of 3D stacked ICs: hard, resistive and capacitive open defects.

Open defects at interconnects in a 3D stacked IC are caused by a void or a crack in a TSV and a micro bump\([3]\). A test method based on X-ray computed tomography has been proposed in order to detect such defects\([5]\). Such detection is time consuming and prone to false alarms resulting in a significant yield loss.

Interconnects in a 3D stacked IC can also be tested by a boundary scan test method\([1]\) like in tests of interconnects between an IC and a printed circuit board (PCB). Thus, an IEEE 1149.1 test architecture may be implemented within dies located inside many kinds of 3D stacked ICs. Since there are many TSVs inside a 3D stacked IC, it takes a long test time when the IC is tested by such test method. Thus, various kinds of design-for-testability (DfT) methods and built-in test circuits have been proposed so as to shorten the test time\([6–11]\).

Resistive and capacitive open defects that generate timing errors may not be detected by the above test methods. Defects that may cause timing errors may instead be detected by a variety of electrical test methods as proposed in\([12–18]\). A test method proposed in\([12]\) is based on the principle of oscillation testing in analog circuits. An electrical test method that uses an on-chip sensing amplifier has been proposed\([13]\). A test method is proposed by which an open defect at an interconnect is detected by examining whether a short pulse signal is capable of propagating\([16]\).

Electrical test methods proposed in\([14]\) and\([15]\) are based on a quiescent current that is made to flow through an interconnect under test, called a “targeted interconnect” in this paper. Dies are typically designed so that no quiescent current can normally flow. Dies however should be designed so that a quiescent current can be made to flow in interconnects tests. Area overhead of circuits added for the tests may be significant, since there is a large number of interconnects between dies in 3D stacked ICs.

Boundary scan flip flops and input protection circuits embedded in dies are utilized in the electrical test method.
proposed in [14]. Thus, there are no extra circuits added by the DfT method and the area overhead is smaller compared to the ones proposed in [15].

The input protection circuits can be modified so that currents, supplied from boundary scan flip-flops, flow during the tests only [14]. However, modification of input protection circuits may not be acceptable in real designs. Thus, another DfT method was proposed by which input protection circuits were not modified [17], [18]. Since only an nMOS is added to each input interconnect by the DfT method, the area overhead is smaller than that for the method proposed in [15].

The test method proposed in [17] is based on measuring a quiescent supply current of an IC under test. Generally speaking, current measurements typically result in a higher test cost than measurements based on voltages, since a relatively expensive equipment is needed to measure currents. Thus, an electrical test method based on measuring voltages caused by the supply current has been proposed [18].

Whenever an IC designed by the DfT method proposed in [17], [18] is tested, some part of the quiescent supply current may flow through interconnects other than the targeted one. This additional current reduces the sensitivity of open defect detection and it also necessitates the preparation of many threshold values for the tests prior to testing, since such thresholds depend on the number of the interconnects through which the supply current flows. It is a difficult preparation task. Hence, this paper discussing how that DfT method is revised. It was examined by SPICE simulations and by some experimentation whether open defects were detected by the new test method.

The DfT method and an electrical test method are proposed in Sect. 2. The results of the testability analysis are described in Sect. 3.

2. DfT Method for Electrical Interconnect Tests

An IEEE 1149.1 test circuit is implemented in each of the dies residing inside the 3D ICs so that interconnects between KGDs can be tested easily. Thus, 3D ICs made of dies embedding the test circuit are devices under tests (DUTs) in this paper. The control signals for the test method, $T_D I$, $T C K$, $T M S$ and $T R S T$, are provided to a DUT from an external tester as shown in Fig. 1. Two kinds of source voltages, $V_{D D C}$ and $V_{D D H O}$, are nowadays provided to an IC. One belongs to the core circuit and the other belongs to the input/output interface circuits in the IC, respectively. This paper discusses to test ICs to which $V_{D D C}$ and $V_{D D H O}$ are supplied.

It is assumed that dies in a DUT are KGDs. A three-die example of DUTs is illustrated in Fig. 1. The tests aim only at open defects that occur at interconnects made of TSVs and/or micro-bumps of the dies and input/output pins.

The principle of the electrical interconnect test method proposed in [18] for interconnects that lie between $D i e #1$ and $D i e #2$ is shown in Fig. 2. An nMOS switch is added to the output terminal of any protection circuit of each input interconnect in the dies in order to make them testable by the proposed test method as shown in a circuit block $C B a$ in Fig. 2. The source terminals of all the nMOS switches are connected to the $T_{S O P}$ terminal of the IC whereas the $T_{S T}$ terminal that is added to each die in the DUT is connected to the gate terminals of the added nMOSs.

Whenever an IC is tested, a test circuit made of a switch $S w t$ that toggles between a resistor $R_s$ at side $s b$ and a high level ($H$) signal at side $s a$, is connected to the $T_{S O P}$ terminal. In addition, an $H$ signal is provided by the IEEE 1149.1 test circuit only to a targeted interconnect (for example, interconnect $b$ as shown in Fig. 2) whereas low level ($L$) signals are provided to interconnects other than the targeted one. The test input signal application creates a potential quiescent supply current $I_D t$ that may flow along the current path $P a t h # 1$ from $V_{D D H O}$, when an $H$ signal is provided to a $T_{S T}$ terminal of $D i e #2$. If either a hard open defect or a capacitive one occurs at a targeted interconnect $b$ (as shown in Fig. 2), $I_D t$ will not flow. If a resistive open defect occurs there, a smaller $I_D t$ than that of the defect-free IC will flow. Thus, if (1) is satisfied, it is deemed that an open defect occurs at the targeted interconnect.

$$I_{D t} \leq I_{th}$$  \hspace{1cm} (1)

where $I_{th}$ is a threshold value that is specified from variation of $I_{D t}$ from the defect-free ICs.

In order to avoid any expensive measurement equipment necessary to measure $I_{D t}$, the quiescent voltage across $R_s$, $V_{R s}$, is measured in place of $I_{D t}$ [18]. The voltage is
defined by (2) below.

\[ V_{Rc} = R_c \cdot I_{Dt} \quad (2) \]

If (3) is satisfied, it is deemed that an open defect occurs at the targeted interconnect.

\[ V_{Rc} \leq V_{th} \quad (3) \]

where \( V_{th} \) is a threshold value specified from the deviation of \( V_{Rc} \) from the respective voltage of defect-free ICs.

Some part of \( I_{Dt} \) may flow into interconnects other than the targeted one (as shown in Fig. 2 as \( I_{Dt2} \)), since an \( L \) signal is provided to interconnects other than the targeted one. Thus, \( I_{Dt} \) is expressed by (4).

\[ I_{Dt} = I_{Dt1} + I_{Dt2} \quad (4) \]

\( I_{Dt2} \) depends on the number of interconnects between dies that are connected to the targeted interconnect. As such number becomes large, a large reverse \( I_{Dt2} \) may flow and the changes in \( I_{Dt} \) caused by an open defect may become small. Thus, a resistive open defect of a small resistance may not be detected by the test method proposed in [18].

The DfT method of [18] has therefore been revised so that currents of the type \( I_{Dt2} \) cannot flow. As shown in Fig. 3(a), a diode is added to the source terminals of the nMOSs to prevent reverse \( I_{Dt2} \) currents from flowing in tests. Whenever a defect-free IC is tested, \( I_{Dt} \) will flow only along the current path, \( \text{Path#2} \), shown in Fig. 3(a), since only the diode that is in \( \text{Path#2} \) is turned on. Whenever either a hard open defect or a capacitive open defect occurs at the targeted interconnect, the current will not flow. When a resistive open defect occurs at the targeted interconnect, a smaller \( I_{Dt} \) than that of the defect-free ICs will flow. Thus, such currents are detected by thresholding tests shown in (3). Since the current flows through only one interconnect, a defective interconnect is located whenever the condition of (3) is satisfied.

Two dies are connected with TSVs and/or micro bumps. The connection is modeled as Fig. 3(a). More than two dies are able to be connected with them by stacking the dies. The connection is modeled as an interconnection with fan-out branch which is shown in Fig. 3(b). Whenever interconnects connecting to more than two dies are tested, an \( H \) signal is provided to a \( Tst \) terminal of only one of the dies to which fan-out branches of the targeted interconnect are connected. For example, when an input interconnect of \( \text{Die#3}, b2 \), is tested as shown in Fig. 3(b), \( L \) and \( H \) signals are provided to \( Tst2 \) and \( Tst3 \), respectively. Hence, \( I_{Dt} \) flows along \( \text{Path#3} \) as shown in Fig. 3(b). When an open defect occurs at \( b2 \) or the stem of the fan-out branch \( b \), it is detected by the condition given in (3), since \( I_{Dt} \) is altered.

A defective interconnect can be located by the test method equally well for both interconnects with fan-out branches as well as for interconnects that do not fan-out, since an \( H \) signal is output to only one interconnect and is provided to a \( Tst \) terminal of only one die. For example, if (3) is satisfied only in the cases of \( Tst2 = H \) and \( Tst3 = L \) as shown in Fig. 3(b), it is concluded that an open defect occurs at an input interconnect of \( \text{Die#2}, b1 \). If the condition is satisfied only in the cases of \( Tst2 = L \) and \( Tst3 = H \), it is concluded that the defect occurs at \( b2 \). If the condition is satisfied in both of the cases, it is concluded that the defect occurs at \( b \).

Interconnects between dies that are inside a DUT and primary output pins of the IC are tested in the same manner as in Fig. 3 by measuring \( V_{Rc} \). Such interconnects are tested by being connected to ICs embedding a circuit block \( CBb \) as shown in Fig. 3(a), and providing the previously described test input signals.

Even if open defects occur at more than one interconnect simultaneously, all of them will be detected by the test method since only one interconnect is tested at a time. Also,
the number of test input vectors of the test method is the total number of input terminals of the core circuits in a DUT and the primary output pins.

ICs designed by the DfT method can be tested by a boundary scan test method and work in the normal mode with $V_{DDIO}$ provided to a $T_{SOP}$ terminal of a DUT.

Only dies determined as KGDs in pre-bond tests that are performed prior to stacking are stacked in a stacking process. Our testable designed circuit block $CBa$ in a die is tested easily in the pre-bond tests by measuring $V_{Rc}$ after connecting the test circuit to it and providing $V_{DDIO}$ to only one input interconnect and no signal to the others with test probes attached to the die, respectively.

3. Testability of The Interconnect Test Method

A layout of a die is designed by incorporating the proposed DfT method in 0.18 $\mu$m CMOS technology process of Rohm Co. Ltd. A core circuit in the die is taken as a 16 stage inverter chain circuit. Input and output protection circuits used in the die design were initially adopted from the CMOS cell library distributed by VDEC in the University of Tokyo, Japan. However, prior to the ICs prototyping by Rohm Co. Ltd, the input and output protection circuits in the designed die were replaced by the protection circuits of the IC foundry.

It was examined via SPICE simulations and experimentation whether open defects occurring at interconnects of the dies could be detected by the test method described above. It is apparent from [18] that interconnects connecting to more than two dies shown in Fig. 3(b) are able to be tested by means of $I_{Dt}$ by providing an $H$ level signal provided only to a $T_{st}$ terminal of one of them. Thus, we discuss only detectability of open defects between two dies in Fig. 3(a). The two source voltages that are provided to the dies are specified by the CMOS process: $V_{DDIO} = 3.3V$, $V_{DDC} = 1.8V$.

3.1 Evaluation by SPICE Simulations

A SPICE netlist is extracted from the layout of the designed die with an extraction tool Virtuoso by Cadence. The SPICE netlist code of the simulation circuit shown in Fig. 4 was merged with the die netlist by adding the parasitic resistance $R_p = 0.01\Omega$ and capacitance $C_p = 3pF$ extracted from a TSV interposer to interconnects that lie between the two dies. A resistor $R_c$ of 300 $\Omega$ is used in the test circuit. The selection of $R_c$ is discussed in 3.3.

A resistive open defect is inserted to an interconnect $S1$ by adding a resistor $R_f$ of $1T\Omega$ to the coded netlist in order to examine whether a hard open defect is detectable. In addition, a resistive open defect and a capacitive open one are inserted to $S1$ by adding a resistor $R_f$ and a capacitor $C_f$ to the netlist, respectively.

Input signals to $IN0$, $IN1$, $IN2$ and $IN3$ in the evaluations are shown in Fig. 5. The test vectors are applied to the circuit every $T_s$. An IEEE 1149.1 test circuit is not included in the simulation circuit. However, by providing the test vectors to $IN0$, $IN1$, $IN2$ and $IN3$, an equivalent operation can be realized as that of a circuit made of dies in which an IEEE 1149.1 test circuit is implemented.

The simulation results are shown in Fig. 6. $I_{Dt}$ stops flowing whenever a $L$ signal is provided to a targeted interconnect following an $H$ signal that had been provided to it. As a next step, an $H$ signal is provided to another interconnect and $I_{Dt}$ resume flowing. Thus, after $V_{Rc}$ decreases
at the beginning of each test input application, the quiescent \( V_{Rc} \) appears as shown in Fig. 6.

When a resistive open defect of \( R_f = 400\Omega \) occurs at \( S_1 \), almost the same quiescent \( V_{Rc} \) appears as the defect-free circuit. Thus, such a defect may not be detected by the test method. On the other hand, the hard open defect and the resistive one of \( R_f = 750\Omega \) at \( S_1 \) are capable of being detected by the test method, since a significantly smaller quiescent \( V_{Rc} \) appears than that of the defect-free circuit. In addition, both can be detected at an ordinary digital oscilloscope test speed of 200MHz, since \( T_s = 5\) nsec.

Simulation results for \( T_s = 1\) nsec are shown in Fig. 7. An \( H \) signal is provided to \( S_2 \) prior to the appearance of a quiescent \( V_{Rc} \) that does appear when \( S_1 = H \) as shown in Figs. 7(b) and (c). Thus, it is impossible to test the IC by means of quiescent \( V_{Rc} \)'s at a certain high enough test speeds such as 1GHz.

\( V_{Rc} \) waveforms that appear whenever capacitive open defects of 0.47pF and 2pF occurs at \( S_1 \) are shown in Figs. 8 and 9. A supply current from \( V_{DDIO} \) begins to flow through \( S_1 \) so as to charge \( C_f \) when an \( H \) signal is an output to \( S_1 \) after providing an \( L \) signal to \( S_0 \). As \( C_f \) is charged, the supply current becomes small and \( V_{Rc} \) decreases as shown in Fig. 8(a). When \( C_f \) is charged fully, the current stops flowing and \( V_{Rc} \) becomes zero. On the other hand, an \( H \) signal is provided to \( S_2 \) before the appearance of the quiescent \( V_{Rc} \) that is created when \( S_1 = H \) as shown in Fig. 8(b), since \( C_f \) cannot be charged quickly.

Similarly, in case of a capacitive open defect of large \( C_f \), it takes a long time to charge the capacitance fully as shown in Fig. 9. The capacitive open defects are not detectable by measuring a quiescent \( V_{Rc} \) at a test speed of 1GHz. The capacitors however will be charged fully and \( V_{Rc} \) will become zero for a larger value of \( T_s \). Thus, such will be detected by reducing the test speed. On the other hand, capacitive open defects of \( C_f \leq 0.47\) pF are detected at a test speed of 200MHz, since \( C_f \) is charged fully in a short time.

Voltage waveforms at \( S_{1x} \) and \( S_{1y} \) in the simulation circuit with \( T_{st2} = L \) are shown in Figs. 10 and 11. It is observed from Fig. 10 that the resistive open defect of \( R_f = 750\Omega \) and the capacitive open one of \( C_f = 0.47\) pF at \( S_1 \) generate additional propagation delay times of 279psec and 71psec, respectively. These are detected by the test method at a test speed of 200MHz as shown in Fig. 6(c) and Fig. 8(a).

An \( H \) signal does not propagated to \( S_{1y} \) in case of a capacitive open defect of \( C_f = 0.2\) pF as shown in Fig. 11. Thus, it will be detected by measuring the logical error. However, an \( H \) signal propagates to \( S_{1y} \) in case of a capacitive open of \( C_f \geq 0.47\) pF. It means that it is impossible to detect capacitive open defects of \( C_f \geq 0.47\) pF by measuring logic values, since no logical errors will appear. The defect of \( C_f = 0.47\) pF is detected by the test method at a test speed of 200MHz as shown in Fig. 8(a). Thus, capacitive open defects that cannot be detected by measuring logic values are detected by our test method.

3.2 Evaluation by Experiments on PCB Circuits

An IC which was made of the designed die was prototyped. A PCB circuit made of the IC was built in order to examine testability of the test method. The circuit is shown in
Fig. 11 Faulty effects of capacitive open defects.

Fig. 12 Experimental circuit.

Fig. 13 Tests for resistive open defects at $T_s = 1\mu\text{sec}$.

(a) Defect-free circuit
(b) Resistive open defect of $R_f = 5.1k\Omega$
(c) Resistive open defect of $R_f = 7.5k\Omega$
(d) Hard open defect

Fig. 14 Tests for capacitive open defects at $T_s = 1\mu\text{sec}$.

(a) $C_f = 47pF$
(b) $C_f = 100pF$

As shown in Figs. 13(c) and (d), the 7.5kΩ resistive ones and the hard open defect at $S1$ are capable of being detected by our test method, since a smaller $V_{Rc}$ results when $S1 = H$ compared to the defect-free circuit. On the other hand, a quiescent $V_{Rc}$ that is almost similar to the one in the defect-free circuit appears at $S1 = H$ as shown in Fig. 13(b). Thus, the resistive open defect of $R_f = 5.1k\Omega$ may not be detected by the test method.

Capacitive open defects of $C_f = 47pF$ and $C_f = 100pF$ are both detected by the test method as shown in Fig. 14. As the capacitance becomes large, it takes a longer time for $C_f$ and $C_p$ to be charged fully. It is found from Fig. 14 that such defects represented by larger capacitance values are detected by increasing $T_s$, that is, at a lower test speed. $V_{Rc}$’s in the measured waveforms are smaller than the corresponding ones obtained in the simulation results implying that the actual models of circuit blocks $CBi$ and $CBo$ in the prototype IC differ from the ones assumed in the simulation circuits. The reason for the discrepancy is the users’ inability to access the explicit model blocks of the prototype IC provided by the IC foundry.

In order to validate the experimental results denoted above, SPICE netlists of the circuit in Fig. 12 were coded along with a netlist of 74HC04 distributed by NXP Co. Ltd and the one of our designed die. The sizes of MOSs in output buffer gates inside 74HC04 were adjusted so that almost the same $V_{Rc}$ could appear as in Fig. 13(a). In addition, a resistive open defect of $R_f = 7.5k\Omega$ and a capacitive open one...
of $C_f=100\text{pF}$ were inserted to the netlist. The simulation results are shown in Fig. 15. As shown in Fig. 15, almost the same simulation results are obtained as in the experimental results of Fig. 13(c) and Fig. 14(b). The small difference is caused by the difference of $CB_i$’s between our designed IC and the prototyping IC. Hence, it is validated by SPICE simulation that the defects inserted to the experimental circuit are detected by the test method.

4. Discussions

4.1 Testability of Open Defects

In case of dies designed by the DfT method proposed in [17], [18], $I_{Df}$ is divided into $I_{Df1}$ and $I_{Df2}$. As $I_{Df2}$ increases, the change in $V_{Re}$ caused by an open defect decreases. $I_{Df2}$ depends on the number of interconnects between dies that are connected to a targeted interconnect. Thus, one should prepare for many threshold voltages $V_{ih}$’s prior to testing. In addition, it is difficult to estimate testability of the test method owing to $I_{Df2}$. On the other hand, $I_{Df}$ flows into only a targeted interconnect in case of dies designed by the DfT method proposed in this paper. Furthermore $V_{ih}$ is independent of the number of interconnects. Hence, a further discussion of the testability of defects using the test method is discussed in this paper.

An equivalent circuit of the current path of $I_{Df}$ is shown in Fig. 16(a). In the figure, $R_i$ is a resistor in the input protection circuit depicted in Fig. 4. A pMOS, $Mp1$, existing in the output buffer gate in $CBo$ outputs an $H$ signal to $b$. An $L$ and an $H$ signals are provided to the gate terminals of $Mp1$ and $Mn1$ in the test of $b$, respectively. When $Mp1$ and $Mn1$ operate in the triode mode, drain currents of less than 115mA and 6.8mA flow, respectively. In Figs. 7 and 8, $I_{Df}$ of 2.5mA flows when a defect-free interconnect is tested, since $V_{Re}$ becomes about 750mV across $R_e$ of 300Ω. It means that $Mp1$ and $Mn1$ indeed operate in the triode mode. Thus, $Mp1$ and $Mn1$ are each modeled as a resistor and the equivalent circuit is simplified to a circuit made of an equivalent resistor and a diode.

$I_{Df}$ is found from the intersection of the Ohm’s law characteristics defined by (5) and an $I_{Df} – V_{AK}$ characteristic curve of the diode defined by (6).

$$I_{Df} = \frac{(V_{DDIO} – V_{AK})}{(R_e + R_p + R_i + R_{Mp1} + R_{Mn1})}$$

(5)

$$I_{Df} = I_S \cdot (e^{V_{AK}/V_T} – 1)$$

(6)

where $I_S$ is the saturation current of the diode. $R_{Mp1}$ and $R_{Mn1}$ are the ON-resistances of $Mp1$ and $Mn1$. $V_T$ is the thermal voltage as defined by (7).

$$V_T = kT/q$$

(7)

where $k$, $T$ and $q$ are the Boltzmann’s constant, absolute temperature and the charge of an electron, respectively.

Whenever a hard open defect or a capacitive one occurs, $I_{Df}$ does not flow and $V_{Re}$ becomes zero independently of $R_e$. However, $V_{Re}$ depends on $R_e$ for resistive open defects. In case of $R_e$, whose resistance is $R_{c1}$, $I_{Df}$ specified by $P1$ in Fig. 16(b) flows. $R_{M}$ in the figure is the sum of $R_p$, $R_{c1}$, $R_{Mp1}$ and $R_{Mn1}$. If a resistive open defect whose resistance is $R_f$ occurs at $b$, $I_{Df}$ flows whose value is defined as an intersection $P2$ of the $I_{Df} – V_{AK}$ characteristic curve and the line defined by (8).

$$I_{Df} = \frac{(V_{DDIO} – V_{AK})}{(R_e + R_p + R_i + R_{Mp1} + R_{Mn1} + R_f)}$$

(8)

Thus, $I_{Df}$ specified by $P2$ flows.

The difference of $I_{Df}$ between the defect-free IC and the defective one, $\Delta I_{Df}$, depends on $R_e$. When a resistor of $R_{c2}$ larger than $R_{c1}$ is used, $I_{Df}$ specified by $P3$ flows in the defect-free IC. If a resistive open defect of $R_f$ occurs at $b$, $I_{Df}$ specified by $P4$ in Fig. 16(b) flows. As shown in Fig. 16(b), $\Delta I_{Df}$ in $R_{c2}$ is smaller than in $R_{c1}$.

Resistive open defects are detected by means of $V_{Re}$. Since $V_{Re}$ is defined by (2), it is found from Fig. 16(b) that as $R_e$ becomes smaller, $\Delta V_{Re}$, which is defined as the difference from $V_{Re}$ in the defect-free ICs, becomes larger. Thus, $R_e$ should be taken as small as possible in order to detect
resistive open defects of small resistance. However, as \( R_c \) becomes smaller, \( V_{Re} \) becomes smaller which may need amplification for detectability of the defect. This may lead to higher test cost. Hence, there is a tradeoff in specifying \( R_c \).

\( I_{Df} \) of a defect-free IC varies due to process variations. The variation is defined as the range from \( I_{Df/\text{min}} \) to \( I_{Df/\text{max}} \) in Fig. 17. When a hard open defect occurs, \( V_{Re} \) becomes zero regardless of the process variation. When a capacitive open defect occurs, \( V_{Re} \) becomes zero regardless of process variation by reducing the test speed. Thus, these are detected by this test method regardless of process variations.

On the other hand, a dependency on both process variations and the test speed happens in tests attempting to detect resistive open defects. A resistive open defect of large resistance generates long propagation delay. The defect is easy to be detected by measuring logic values. Resistive open defects of small resistance cannot be detected by measuring logic values. These should be detected by the test method advocated by this paper. A quiescent \( V_{Re} \) appears momentarily whenever the open defects occur. Thus, it depends only on process variations whether or not a resistive open defect can be detected. The minimum resistance \( R_{f/\text{min}} \) of resistive open defects that can be detected by our test method is derived under known process variations.

\( I_{Df} \) of a defective IC varies like in \( I_{Df} \) of defect-free ICs. \( I_{Df} \) of a defective IC that includes a resistive open defect of \( \text{defect1} \) varies in a range from \( I_{Df/\text{min}} \) to \( I_{Df/\text{max}} \) that is defined in Fig. 17. The defect is not detected by the test method, since \( I_{Df} \) of the defective IC can be greater than \( I_{Df/\text{min}} \) due to the process variations. A resistive open defect of \( \text{defect2} \) will be detected by our test method, since the maximum \( I_{Df} \), \( I_{Df/\text{max}} \), is smaller than \( I_{Df/\text{min}} \).

Process variations of MOS transistors are modeled as the following four worst-case design corners [19]: (Fast Fast), (Fast Slow), (Slow Fast) and (Slow Slow) for a pair of nMOS and pMOS. Thus, the range of \( I_{Df} \) of the defective circuit in which \( R_f \) is inserted to \( S \) in Fig. 4 is derived under the process variations by SPICE simulation. \( R_f \) from the simulation results is derived so that the maximum \( I_{Df} \) can be smaller than \( I_{Df/\text{min}} \). Since testability of resistive open defects may depend on \( R_c \), the resistance, \( R_{f/\text{min}} \), for \( R_c = 0\Omega \), 100\Omega, 300\Omega and 600\Omega was examined.

As shown in Table 1, \( R_{f/\text{min}} \) depends on \( R_c \). It is apparent from Fig. 16. It is also shown in the table that resistive open defects whose resistance is 750\Omega or more are detected by the test method under the known process variations when \( R_c = 300\Omega \). The resistive open defect of \( R_f = 750\Omega \) generates additional propagation delay of 279psec as shown in Fig. 10. Thus, open defects causing longer propagation delay time of 279psec or more are detected by our test method under the assumed process variations.

Since parasitic oscillation is sometimes imposed on the waveforms of \( V_{Re} \) as shown in Figs. 13 and 14, ICs should be tested by the average value of measured \( V_{Re} \) values. Test speed of the method is specified as the time until quiescent supply current \( I_{Df} \) appears. It depends on \( R_c \), \( R_f \) of a resistive open defect and \( C_f \) of a capacitive open defect to be detected. Also, it depends on parasitic resistance and capacitance in \( CBi, CBo \) and a targeted interconnect besides drivability of output buffer gates in \( CBo \). Simulation results presented in 3.1 revealed that open defects can be detected at a test speed of 200MHz. In the PCB circuit experiments, open defects are detected at the test speed of 1MHz. In case of 3D ICs, a faster test speed can be realized, since parasitic resistance of an interconnect is smaller so that logic signals can be transferred at a high speed with output buffer gates. Thus, it is expected that open defects can be detected at a test speed faster than 1MHz in real 3D stacked ICs.

We have discussed detectability of open defects in 3D ICs dies of 0.18\mu m CMOS process. \( V_{DDIO} \) for dies of an ultra deep submicron CMOS process is smaller. Since the source voltage reduction makes \( V_{Re} \) smaller than 3.3V, an amplifier should be used to amplify \( V_{Re} \) in our test. However, we think that open defects are detected by means of the amplified \( V_{Re} \), since \( I_{Df} \) change will be caused in such ICs by the defects.

4.2 Comparison to [18]

The DfT method proposed in this paper is revised from [18]. We compare the DfT method and the test method to the ones in [18].

Pin overhead of the DfT method is the same as [18], since only one \( T_{st} \) terminal should be added to each die like in [18].

A couple of an nMOS switch and a diode are added to each input terminal of a die. The diode is made of a MOS. Thus, area overhead of the DfT method is 2\( N_i \), where \( N_i \) is the number of input interconnects of the die. We think that the area overhead will be accepted since it is extremely smaller than the number of MOSs in core circuits implemented inside dies.

\( \Delta I_{Df} \), caused by a resistive open defect is higher than [18]. When an interconnect \( b \) is tested by the test method proposed in [18], \( I_{Df2} \) does not flow through \( R_c \) as shown in Fig. 2, so that \( \Delta V_{Re} \) can become small nevertheless \( I_{Df} \) changes owing to a resistive open defect. The equiva-
As shown in Fig. 19, the resistance \( R \) of the interconnects between them increases. When the number of interconnects between them is small, the number of interconnects shown in Fig. 3(a). When the number of interconnects in case of our testable designed dies shown in Fig. 19. However, there are a huge number of interconnects between dies in 3D ICs. In this case, the number of interconnects between dies is greater than 8 in 3D ICs. Thus, sensitivity of resistive open defects in our new DfT method is higher than [18]. In case of capacitive open defects and hard open defects, \( I_{\text{Dt}} \) will not flow in the defect-free circuits. Thus, the sensitivity of the DfT method in [18] is independent of the number of interconnects between dies and is the same as the one proposed in this paper.

Operating speed of 3D ICs made of dies designed by this DfT method is the same as the ones in [18], since an \( L \) level signal is provided to \( T_{\text{st}} \) terminals of all dies in them. Both of the test methods are based on quiescent \( I_{\text{Dt}} \). Time for quiescent \( I_{\text{Dt}} \) to appear after providing a test input vector depends on \( C_p \)'s and \( R_p \)'s of interconnects to which \( I_{\text{Dt}} \) flows besides \( R_c \). The \( R_c \) and drivability of output buffer gates in dies. All of the \( C_p \)'s should be charged through \( R_c \) and \( I_{\text{Dt}} \). In case of the DfT method in [18], the total capacitance made of \( C_p \)'s depends on the number of interconnects through which \( I_{\text{Dt}} \) flows. Since there are many interconnects between dies, it takes longer time for quiescent \( I_{\text{Dt}} \) to appear than our new DfT method. The number of test input vectors is the same as [18], since only one input interconnect of a die is tested at a time like in [18]. Thus, test time is able to be shortened by the DfT method proposed in this paper.

\( I_{\text{Dt}} \) flowing in tests of ICs designed by the DfT method.

![Fig. 18](image1) Equivalent circuit in a test of \( b \) in Fig. 2.

![Fig. 19](image2) \( \Delta I_{\text{Dt}} \) caused by a resistive open defect.

### Table 2

| \( n \)  | \( \Delta I_{\text{Dt}} \) [mA] | \( \Delta V_{\text{Re}} \) [mV] | \( \Delta I_{\text{Dt}} \) [mA] | \( \Delta V_{\text{Re}} \) [mV] |
|-------|----------------|----------------|----------------|----------------|
| 4     | 0.725          | 217.3          | 4.240          | 633.4          |
| 8     | 0.527          | 158.4          | 8.480          | 1266.8         |
| 16    | 0.146          | 33.96          | 16.00          | 2061.0         |

In order to examine it, we examined whether sensitivity of resistive open defects in our testable designed dies was greater than [18] by SPICE simulation. We designed layouts of \( \text{Die#2} \) in Fig. 4 whose number of input interconnects were 4, 8 and 16, and replaced the diodes in \( C B b \) to metal lines. We converted them to SPICE netlists with \textit{Virtuoso}. We coded SPICE netlists of the simulation circuits in Fig. 4 that were made of the designed dies and inserted a resistive open defect by adding \( R_f \) of 750\( \Omega \) to \( S_1 \). \( \Delta I_{\text{Dt}} \) and \( \Delta V_{\text{Re}} \) were derived with \( R_c = 300\Omega \) when \( T_{\text{st}} = H \) by SPICE simulation. The results are summarized in Table 2.
is smaller than the one in [18] as shown in Fig. 19. Thus, ICs will be tested with a lower test power consumption than [18].

\( I_{Dh} \) in the DfT method of [18] depends on the number of interconnects between dies. Thus, \( V_{th} \) should be prepared for each die before testing by considering process variation. It is a hard task. On the other hand, it is specified for the DfT method proposed in this paper only by considering process variation of MOSs. Hence, \( V_{th} \) preparation is simpler than [18].

Area overhead is only a disadvantage of our new DfT method and is small as denoted above. Therefore, it is concluded that the new DfT method is more effective than [18].

5. Conclusions

A DfT method and an electrical interconnect test method for open defects in 3D stacked ICs were proposed. The circuits were evaluated by SPICE simulation and by some experiments in a PCB circuit made of a prototype IC designed by the DfT method. The simulation results show that an open defect that is modeled as a delay fault generating additional delay time of 279psec and an open defect that generates no logical errors at a test speed of 200MHz. Also, open defects inserted to the PCB circuit are detected by the test method in the experiments at a test speed of 1MHz. It remains as a future work to examine the testability in real 3D stacked ICs.

Acknowledgments

This work was supported by JSPS KAKENHI Grant 17H0175. Also, it is supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Synopsys, Inc., Cadence Design Systems, Inc., and Mentor Graphics, Inc. The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Rohm Corporation and Toppan Printing Corporation. We would like to thank Mr. Shoichi Umezu and Mr. Akihiro Odoriba, Tokushima University, for their IC design. We are also grateful to Universiti Teknikal Malaysia Melaka (UTeM) and Yayasan Pelajaran Mara (YPM) for the scholarship and financial support.

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