A Survey on Hardware Implementations of Elliptic Curve Cryptosystems

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Abstract

In the past two decades, Elliptic Curve Cryptography (ECC) have become increasingly advanced. ECC, with much smaller key sizes, offers equivalent security when compared to other asymmetric cryptosystems. In this survey, an comprehensive overview of hardware implementations of ECC is provided. We first discuss different elliptic curves, point multiplication algorithms and underlying finite field operations over binary fields $F_{2^m}$ and prime fields $F_p$ which are used in the literature for hardware implementation. Then methods, steps and considerations of ECC implementation are presented. The implementations of the ECC are categorized in two main groups based on implementation technologies consist of field programmable gate array (FPGA) based implementations and application specific integrated circuit (ASIC) implementations. Therefore, in these categories to have a better presentation and comparison, the implementations are presented and distinguished based on type of finite fields. The best and newest structures in the literature are described in more details for overall presentation of architectures and approaches in each group of implementations. High-speed implementation is an important factor in the ECC applications such as network servers. Also in smart cards, Wireless Sensor Networks (WSN) and Radio Frequency Identification (RFID) tags require to low-cost and lightweight implementations. Therefore, implementation methods related to these applications are explored. In addition, a classification of the previous works in terms of scalability, flexibility, performance and cost effectiveness is provided. Finally, some words and techniques about future works that should be considered are provided.

keywords: Elliptic Curve Cryptography, FPGA, ASIC, Finite fields, point multiplication.

1 Introduction

Elliptic Curve Cryptography (ECC) was proposed independently by Victor Miller [1] and Neal Koblitz [2] in the mid 1980’s. It is a public key cryptography, which is based on the Elliptic Curve Discrete Logarithm Problem (ECDLP) of the elliptic curve over a finite fields [3]. ECC provides various security applications such as key exchange, digital signatures, data encryption and authentication. The main advantages of ECC, when compared to other public key cryptosystems such as RSA is smaller key size and better performance with equivalent security level. In the two last decades, the application of the elliptic curves in cryptography has been considered and is attractive for many scientists. ECC has different applications in public key cryptography, e.g., banking transactions, mobile security, digital right management, Wireless Sensor Networks (WSN) and other security applications. Also it is applicable in many internet protocols and network applications such as SSL (Secure Sockets Layer), TLS (Transport Layer Security) [4], WAP WTLS (Wireless Transport Layer Security) [5] (for elliptic curves over prime) and IPsec which are commonly used today in over-the-web transactions and secure document transfers. The ECC has been adopted by many standards such as ANSI [6], IEEE [7], ISO [8] and NIST [9]. In December 2010, Chinese State Cryptography Administration (SCA) published the national public key cryptographic algorithm based
on ECC in [10], known as SM2. The industry has taken extreme interest in the ECC for internet protocols, smart cards, Radio Frequency Identification (RFID) tags and cell phones. Manufacturing companies related to ECC are consist of Sun Microsystems, Certicom, MasterCard, Fujitsu, MIPS Technologies, Digital Signature Trust Co and DataKey. The small key size, low area consumption and fast implementation make ECC one of the best choices for hardware implementation. The hardware-based implementations can provide significant security improvements by protecting secret keys and other parameters compared to software solutions. There is a growing need for hardware implementation of the ECC. Hardware implementations have better performance and better power efficiency than that of software implementations based on a microcontrollers. In the ECC, main and backbone operation is point multiplication (scalar multiplication) which is based on field operations. The efficiency of the ECC implementation depends on point multiplication. Efficient hardware implementation of field operations have direct impact on speed and performance of the ECC applications. In computation of elliptic curve point multiplication, the main operations are field multiplication and field inversion. Therefore, for implementation of the ECC these two field operations have more complexity. Some of the time critical applications, such as network servers where millions of heterogeneous client devices need to be connected. Therefore, high-speed hardware implementation of the ECC is an important factor. It could be only feasible and acceptable solution to reach a performance. Also in low-cost and low-area applications such as smart cards, WSN and RFID tags low-power and lightweight hardware implementations are only solutions for realization of these applications.

Implementation of an elliptic curve cryptosystem, like many other systems, follows a hierarchical approach, in which the performance of the top implemented layers is greatly influenced by the performance of the underlying layers. Therefore, it is important to have efficient implementations of the finite field operations in the underlying layer. To that end, three main steps have been performed. The first step is related to design and implementation of finite field operations such as field multiplication, field addition and field inversion. In the second step, design and implementation of point addition and point doubling operations are performed. In the third step, based on point multiplication algorithm, implementation are performed. Different option for ECC implementation are shown in Fig.1. In the first step of the figure type of the elliptic curve is selected. In the second step, the point multiplication algorithm based on elliptic curve can be selected. Also in the third step, the type of finite field, size and other properties are selected. Two applicable fields are binary field $\mathbb{F}_{2^m}$ and prime field $\mathbb{F}_p$. In addition, different works for flexibility are implemented based on two fields that are called dual-field implementations. The binary finite field operations are suitable for hardware implementations due to these structures are carry free. Therefore, the field addition is implemented by a simple bit-wise XOR operation without carry bit. Moreover, the efficiency of the field multiplication depends on representation of elements in $\mathbb{F}_{2^m}$. There are two main practical bases called polynomial basis (PB) and normal basis (NB). In PB by using irreducible Trinomials and Pentanomials the field multiplication and squaring can be implemented efficiently. Also special types of NB representation called Gaussian normal basis representation (GNB) where the field multiplication is implemented efficiently. On the other hand, for prime fields, special primes are highly suited for efficient reduction techniques and implementation, the most simple form of such primes being the Mersenne primes and other are Generalizations Mersenne primes and pseudo-Mersenne primes. In next sections, we explain these options in more details.
This paper focuses on survey of techniques for implementing ECC at a high-speed and low-area and the existing hardware implementations of the ECC. The presentation is organized based on implementation technologies of the ECC such as field programmable gate array (FPGA) and application specific integrated circuit (ASIC). The survey starts by defining different elliptic curves, point multiplication algorithms and finite field arithmetics and also discussing their impact on implementations. Also, methods, steps and considerations in the implementation of the ECC are discussed. Then, the implementations of the ECC found in the literature are presented in related sections also a categorized and comprehensive comparison of the existing works is performed. For fair comparison and better analysis, the works are categorized and presented based on used finite field, type of elliptic curves, representation basis, implementation technology and platforms. We study implementations in terms of (1) hardware consumption (area) which is important for any cost-sensitive application, (2) execution time which is important for many applications especially in high-speed application and is related to speed processing of implementation, (3) maximum operation frequency that has a direct impact on the computation time, power consumption which is important for low-power, low-energy and low-area ASIC implementations.

The rest of the paper is organized as follows. Section 2 describes the mathematical background. The point multiplication algorithms are discussed in Section 3. Section 4 presents finite field arithmetics. In Section 5 methods, steps and considerations of ECC implementation are presented. Elliptic curve implementations are presented in Section 6. Finally, the paper is concluded in Section 7.
2 Mathematical background

In this section, we will briefly introduce the mathematical background relevant to the present survey. We start with a short review of defining different elliptic curves, point multiplication algorithms and finite field arithmetics and also discussing their effect on implementations. The elliptic curves can be defined over any field such as field of rational numbers, real numbers and complex numbers. For cryptographic application, elliptic curves are defined over finite fields. Two important finite fields for hardware implementation are binary fields and prime fields. Elliptic curves are traditional represented by the so called Weierstrass equations. For cryptographic applications, many other forms of elliptic curves have been proposed and investigated to improve high-speed and efficient implementations. In following, we briefly recall elliptic curves used in implementations.

2.1 Elliptic curves over $\mathbb{F}_{2^n}$

Various binary elliptic curves over $\mathbb{F}_{2^n}$ and their properties are discussed and reviewed in this subsection.

2.1.1 Binary Weierstrass curves

An elliptic curve over a field $\mathbb{F}$ can be defined by

$$E : y^2 + a_1 xy + a_3 y = x^3 + a_2 x^2 + a_4 x + a_6$$

This equation is called long Weierstrass equation, where $a_1, a_2, a_3, a_4$ and $a_6$ are in $\mathbb{F}$. The discriminant of the field is given by

$$\Delta = -d_2^2 d_4 - 8d_1^3 - 27d_6^2 + 9d_2 d_4 d_6$$

where $d_2 = a_1^2 + 4a_2, d_4 = 2a_4 + a_1a_3, d_6 = a_3^2 + 4a_6$, and $d_8 = a_1^2 a_6 + 4a_2 a_6 - a_1 a_3 a_4 + a_2 a_3^2 - a_1^2$. $\Delta \neq 0$, since the elliptic curve is nonsingular. The set of affine points $(x, y)$ satisfying the curve equation with the point at infinity denoted by $\mathcal{O}$ construct a group [3]. The set of $\mathbb{F}$-rational points on $E$ is defined as follows:

$$E(\mathbb{F}) = \{(x, y) \in \mathbb{F} \times \mathbb{F} : y^2 + a_1 xy + a_3 y - x^3 - a_2 x^2 - a_4 x - a_6 = 0\} \cup \{\mathcal{O}\}$$

Based on a group of points defined over an elliptic curve, group law operation for two points $P_1, P_2$, where $P_1 \neq P_2$, defines the point addition (PA) $P_3 = P_1 + P_2$ using the tangent and chord rule as the primary group operation. For $P_1 = P_2$ we have point doubling (PD) $P_3 = 2P_1$. Basically a point $P$ over the curve can generate all the other point by PA.

The binary elliptic curves defined over a binary field $\mathbb{F}_{2^n}$. Binary Weierstrass curves (BWCs) is defined by following equation

$$W : y^2 + xy = x^3 + ax^2 + b$$

where $a, b \in \mathbb{F}_{2^n}$ and $b \neq 0$. This equation is called non-super singular which is suitable for cryptographic applications. For this family of curves, NIST recommended standard elliptic curves over $\mathbb{F}_{2^n}$ fields consist of {B-163, B-233, B-283, B-409 and B-571}.

In following point addition and point doubling on BWCs in affine coordinate are presented. Let $P_1 = (x_1, y_1)$ and $P_2 = (x_2, y_2)$ be two points on the BWCs with $P_1 \neq \pm P_2$ where $-P_2 = (x_2, x_2 + y_2)$. Then the addition of points $P_1, P_2$ is the point $P_3$ denoted by $P_3 = P_1 + P_2 = (x_3, y_3)$, where $x_3 = \lambda^2 + \lambda + x_1 + x_2 + a$, and $y_3 = \lambda(x_1 + x_3) + x_3 + y_1$, where, $\lambda = \frac{y_1 + y_2}{x_1 + x_2}$. Also for the point doubling we have $P_3 = 2P_1 = (x_3, y_3)$, where $x_3 = \lambda^2 + \lambda + a$, and $y_3 = \lambda(x_1 + x_3) + x_3 + y_1$, where, $\lambda = x_1 + \frac{y_1}{x_1}$. In this case, point addition and point doubling are computed by $1I+2M+1S$, where $I, M$ and $S$ are cost of computation field inversion, field multiplication and field squaring respectively. Inversion is the most time-consuming operation in among other field
operations. Therefore, the projective coordinate system (each point is represented by three coordinates \((X, Y, Z)\)) is used to reduce the complexity of the point addition and point doubling computation. The more details of the projective coordinates are presented in point multiplication subsection.

2.1.2 Koblitz Curves

In the binary Weierstrass curves if \(a \in \{0, 1\}\) and \(b = 1\), it is called Koblitz curves or anomalous binary curves [1]. Therefore, the Koblitz curves are defined over \(F_{2^m}\) by following equation:

\[
K : y^2 + xy = x^3 + ax^2 + 1
\]

Koblitz curves offer considerable computational advantages compared to the binary Weierstrass curves, because can be used to computation of the point multiplication without the need for point doubling [3]. NIST recommended standard Koblitz curves over \(F_{2^m}\) consist of \{K-163, K-233, K-283, K-409 and K-571\}.

2.1.3 Binary Edwards curves

Binary Edwards curves (BECs) are the first family of the binary elliptic curves with complete group law operation [12]. Let \(d_1, d_2\) be elements of \(F_{2^m}\) such that \(d_1 \neq 0\) and \(d_2 \neq d_1(d_1 + 1)\). The binary Edwards curve with parameters \(d_1\) and \(d_2\) is given by the equation

\[
E : d_1(x + y) + d_2(x + y)^2 = xy(x + 1)(y + 1).
\]

The equation of the binary Edwards curve \(E\) is symmetric in \(x, y\) and the negation of the point \((x, y)\) is \((y, x)\). The point \(O = (0, 0)\) is the neutral element of the addition law and the point \((1, 1)\) has order 2. The addition, doubling and differential addition formulas for the binary Edwards curves are presented in [12]. The addition group law is complete if \(Tr(d_2) = 1\), where \(Tr\) is the trace function from \(F_{2^m}\) to \(F_2\).

2.1.4 Generalized Hessian curves

The Hessian curve is a symmetric curve shape representing an elliptic curve [13]. The arithmetic in this curve is faster than that of Weierstrass form. Therefore, use of Hessian curve in cryptography has been studied. The family of generalized Hessian curves over a finite field covers more isomorphism classes of elliptic curves and it is equivalent to the family of all elliptic curves with a point of order 3 [13]. Generalized Hessian curves provide efficient unified addition formulas which is resist against side-channel attacks. They also have complete addition formulas with suitably chosen parameters. A generalized Hessian curve (GHC) over \(F_{2^m}\) is defined by

\[
H : x^3 + y^3 + c = dxy
\]

where \(c, d\) are elements of \(F_{2^m}\), \(c \neq 0\) and \(d^3 \neq 27c\). This equation a symmetric cubic equation. The Hessian addition formulas, called the Sylvester formulas. In [13] a suitable modification of the Sylvester formulas for fast and efficient unified addition formulas on generalized Hessian curves is presented. For the point \(P = (x, y)\) on \(H\) the additive inverse is given by \(-P = (y, x)\).

2.1.5 Binary Huff curves

The affine model of binary Huff curve (BHC) [14] given by

\[
Huff : ax(y^2 + y + 1) = by(x^2 + x + 1)
\]

where \(a, b \in F_{2^m}\) and \(a \neq b\). Also this curve is birationally equivalent to the Weierstrass elliptic curve [14]

\[
v(v + (a + b)u) = u(u + a^2)(u + b^2)
\]

5
under the inverse maps

\[(x, y) \leftarrow \left( \frac{b(u + a^2)}{v}, \frac{a(u + b^2)}{v + (a + b)u} \right) \quad \text{and} \quad (u, v) \leftarrow \left( \frac{ab(axy + b)}{xy^2}, \frac{ab}{x^2y} \right) \]  

(10)

The set of points on a BHC forms a group. The identity element is \(O = (0, 0)\). While the above maps are not line-preserving, the group law on a BHC satisfies the tangent and chord rule [14]. Binary Huff curves are curves with unified point addition and point doubling formula with resistance against power attacks.

### 2.2 Elliptic curves over \(\mathbb{F}_p\)

Let \(p\) be a prime with \(p > 3\), an elliptic curve over \(\mathbb{F}_p\) is defined the so-called short Weierstrass equation as:

\[y^2 = x^3 + ax^2 + b\]  

(11)

where \(a, b, x, y \in \mathbb{F}_p\) and \(4a^3 + 27b^2 \neq 0\). In this curves the characteristic is not equal 2 and 3 or \(p > 3\). Also group operations on elliptic curves over \(\mathbb{F}_p\) is defined. NIST recommended standard elliptic curves over prime fields consist of \(\{p-192, p-224, p-256, p-384, p-521\}\).

In recent years in [15] a special elliptic curve called Curve25519 over \(\mathbb{F}_p\) is defined, where \(p = 2^{255}-19\). The curve Curve25519 is defined as follows:

\[y^2 = x^3 + 486662x^2 + x\]  

(12)

Other traditional elliptic curve over prime fields \(\mathbb{F}_p\) with \(p \geq 5\) is called Montgomery curve [16] and defined by following equation:

\[M : By^2 = x^3 + Ax^2 + x\]  

(13)

where \(A, B\) are elements in \(\mathbb{F}_p\) and \(B(A^2 - 4) \neq 0\).

Also, the so-called Gallant-Lambert-Vanstone curves for simply GLV curves, are elliptic curves over \(\mathbb{F}_p\) which possess an efficiently computable endomorphism \(\varphi\) whose characteristic polynomial has small coefficients. The three family of GLV curves that can be defined, over a prime field \(\mathbb{F}_p\), by a Weierstrass equation based on [17] are as follows:

In the first case we have

\[GLV_1 : y^2 = x^3 + ax\]  

(14)

In this equation, let \(\alpha \in \mathbb{F}_p\) be an element of order 4. Then the map \(\varphi : GLV_1 \rightarrow GLV_1\) defined by \((x, y) \rightarrow (x, \alpha y)\) and \(O \rightarrow O\) is an endomorphism defined over \(\mathbb{F}_p\). The second family is

\[GLV_2 : y^2 = x^3 + b\]  

(15)

where \(p \equiv 1 \mod 3\). Let \(\beta \in \mathbb{F}_p\) be an element of order 3. Then the map \(\varphi : GLV_2 \rightarrow GLV_2\) defined by \((x, y) \rightarrow (\beta x, y)\) and \(O \rightarrow O\) is an endomorphism defined over \(\mathbb{F}_p\). Let \(p > 3\) be a prime such that 7 is a perfect square in \(\mathbb{F}_p\), and let \(\omega = (1 + \sqrt{-7})/2\), and let \(a = (\omega - 3)/4\). And also for third family of the elliptic curve defined over \(\mathbb{F}_p\) we have

\[GLV_3 : y^2 = x^3 - 3/4x^2 - 2x - 1\]  

(16)

Then the map \(\varphi : GLV_3 \rightarrow GLV_3\) defined by \((x, y) \rightarrow (\omega^{-2}x^2 - \omega, \omega^{-3}y - 2ax + \omega)\) and \(O \rightarrow O\) is an endomorphism defined over \(\mathbb{F}_p\). Computing the endomorphism is a little harder than doubling a point. Galbraith,
Lin, and Scott (GLS) \[18\] generalized the GLV technique to a broader class of elliptic curves defined over $\mathbb{F}_{p^2}$.

The GLS curves were generalized for binary curves over $\mathbb{F}_{2^{2m}}$ in \[19\].

Also Jacobian curve \[20\] can be used in cryptography instead of the Weierstrass form because it can provide a robustness against simple and differential power analysis attacks. In addition, this curve has faster arithmetic compared to the Weierstrass curve.

### 3 Point multiplication algorithms

The most important operation and dominates the execution time of elliptic curve cryptography is called point multiplication or scalar multiplication. In this operation we have, $kP = P + P + ... + P$, where $k$ is a positive integer and $P$ is a point on the curve. Therefore, in a straightforward way the point multiplication can be computed by $k$ times addition of point $P$ by self using PA and PD operations. Here, we presented different point multiplication methods. There are several ways to implement point multiplication \[3\]: Right to left double-and-add, Left to right double-and-add, Non-adjacent-form (NAF) method, window NAF method (width-$w$ NAF), Sliding window method, $\tau$-adic NAF ($\tau$NAF) method and Montgomery ladder method. Possible coordinates are affine and projective. In the projective coordinate, projective point $(X, Y, Z)$, $Z \neq 0$ corresponds to the affine point $(X/Z, Y/Z)$. Applicable and the most popular projective coordinates are consist of Standard $(c = 1, d = 1)$, Jacobians $(c = 2, d = 3)$ and Lopez-Dahab $(c = 1, d = 2)$. For example, in Lopez-Dahab (LD) coordinate \[21\] projective version of the BWCs in Eq.(2) is obtained by replacing $x$ and $y$ with $X/Z$ and $Y/Z$ as:

$$E: Y^2 + XYZ = X^3Z + aX^2Z^2 + bZ^4 (17)$$

In the point multiplication algorithm, for use with most cryptographic protocols, it is required to convert the output result with projective coordinates to affine coordinates. A point multiplication is performed in three main steps. In the first step, the point multiplication algorithm must be selected. In the second step, the coordinates to represent elliptic curve points must be defined. Finally in the last step, the field operations algorithms, representation of the field elements (type of basis for the binary fields and structure of the prime number $p$ in the prime fields) are defined and selected. Fig.2 shows three main steps for compute of the point multiplication.

| First step        | Select the point multiplication method |
|-------------------|----------------------------------------|
| Second step       | Select the coordinates to represent elliptic curve points |
| Third step        | 1- The field operations algorithms,  
|                   | 2- Representation of the field elements:  
|                   | - Type of basis for the binary fields  
|                   | - Structure of the prime number $p$ in the prime fields  
|                   | 3- and ... |
to left and Algorithm\textsuperscript{2} processes the bits from left to right. In these algorithms every bit of scalar \(k\) is scanned, then based on value of each bit, ‘0’ or ‘1’, a PD or both PD and PA operations are performed. In the right to left algorithm, the PD and PA operations can be performed in parallel form.

\begin{center}
\textbf{Algorithm 1} Right-to-left point multiplication algorithm
\begin{algorithmic}
\State \textbf{Input:} \(k = (k_{l-1}, k_{l-2}, \ldots, k_2, k_1, k_0), P \in \mathbb{F}_q\)
\State \textbf{Output:} \(kP\)
\State 1. \(Q \leftarrow O\)
\For\(i\) from 0 \textbf{downto} \(l-1\) \Do
\If\(k_i = 1\) \Then \(Q \leftarrow P + Q\) \EndIf
\EndFor
\Return \(Q\)
\end{algorithmic}
\end{center}

\begin{center}
\textbf{Algorithm 2} Left-to-right point multiplication algorithm
\begin{algorithmic}
\State \textbf{Input:} \(k = (k_{l-1}, k_{l-2}, \ldots, k_2, k_1, k_0), P \in \mathbb{F}_q\)
\State \textbf{Output:} \(kP\)
\State 1. \(Q \leftarrow O\)
\For\(i\) from \(l-1\) \textbf{downto} 0 \Do
\If\(k_i = 1\) \Then \(Q \leftarrow P + Q\) \EndIf
\EndFor
\Return \(Q\)
\end{algorithmic}
\end{center}

The Hamming weight (HW) of \(k\), i.e., \(H(k)\), is the number of nonzero terms in the representation of \(k\). The PA is required in the algorithm only when \(k_i = 1\). When a signed-bit representation in NAF, i.e., \(k_i \in \{0, \pm 1\}\) so that \(k_i k_{i+1} = 0\), for all \(i\), is used, \(H(k) = m/3\) on average. Therefore, it is of interest to reduce \(H(k)\). Hamming weight of \(k\) can be further reduced with windowing methods, but then certain points need to be precomputed\textsuperscript{22}. In Koblitz curves, PD operation can be replaced efficiently by Frobenius endomorphism\textsuperscript{11}. An algorithm similar to Algorithm\textsuperscript{1} and Algorithm\textsuperscript{2} can be devised so that PDs are replaced by Frobenius endomorphisms. Frobenius map \(\varphi\) is an endomorphism that raises every element to its power of two, i.e., \(\varphi : x \rightarrow x^2\). Koblitz curves have the appealing feature that if the point \(P = (x, y)\) is on curve, so is the point \((x^2, y^2)\). Frobenius map for a point \(P = (x, y)\) can be defined as \(\varphi : (x, y) \rightarrow (x^2, y^2)\). Frobenius endomorphism can be carried out efficiently if the field elements are represented in normal basis.

Algorithm\textsuperscript{3} shows point multiplication algorithm by using NAF\((k)\) instead of the binary representation of \(k\). In this algorithm, if processes \(w\) digits of \(k\) at a time by using a window method we have Algorithm\textsuperscript{4}.

\begin{center}
\textbf{Algorithm 3} Binary NAF method for point multiplication
\begin{algorithmic}
\State \textbf{Input:} \(k = (k_{l-1}, k_{l-2}, \ldots, k_2, k_1, k_0), P \in \mathbb{F}_q\)
\State \textbf{Output:} \(kP\)
\State 1. Compute NAF\((k)\) = \(\sum_{i=0}^{l-1} k_i 2^i\)
\State 2. \(Q \leftarrow O\)
\For\(i\) from \(l-1\) \textbf{downto} 0 \Do
\If\(k_i = 1\) \Then \(Q \leftarrow Q + P\) \EndIf
\EndFor
\Return \(Q\)
\end{algorithmic}
\end{center}

\begin{center}
\textbf{Algorithm 4} Window NAF method for point multiplication
\begin{algorithmic}
\State \textbf{Input:} \(k = (k_{l-1}, k_{l-2}, \ldots, k_2, k_1, k_0), P \in \mathbb{F}_q\)
\State \textbf{Output:} \(kP\)
\State 1. Compute NAF\(_w\)(\(k\)) = \(\sum_{i=0}^{l-1} k_i 2^i\)
\State 2. Compute \(P_i = iP\) for \(i \in \{1, 3, 5, \ldots, 2^{w-1} - 1\}\)
\State 3. \(Q \leftarrow O\)
\For\(i\) from \(l-1\) \textbf{downto} 0 \Do
\If\(k_i \neq 0\) \Then \(Q \leftarrow Q + P_{k_i}\) \EndIf
\EndFor
\Return \(Q\)
\end{algorithmic}
\end{center}

In order to utilize fast Frobenius endomorphisms, \(k\) must be converted into an optimize NAF representation such as \(\tau\)NAF. In\textsuperscript{23} efficient algorithms for finding \(\tau\)NAF are presented. \(\tau\)NAF is analogous with the binary NAF as it has on average the same length and HW. In the Koblitz curves, the point multiplication can be further improved
by converting the scalar $k$ into $\tau$-adic nonadjacent form $\tau$NAF which rewrites $k$ into the form $\sum_{i=0}^{l-1} u_i \tau^i$, where $u_i \in \{0, \pm 1\}$ and $\tau = ((-1)^{1/2} + \sqrt{-1})/2$. $\tau$NAF point multiplication algorithm is shown in Algorithm 5. In the point multiplication based on NAF representation of the scalar $k$, it is needs to be converted in NAF expansion. Therefore, this conversion is one of the important steps in the hardware implementation of the point multiplication. One popular point multiplication algorithm is Montgomery ladder [23] which is shown in Algorithm 6. In this algorithm point multiplication computes based on the $x$ and $z$ and the $y$-coordinate is recovered in the end. Both PD and PA operations are computed very efficiently for every $k_i$, where $k_i$ is $i^{th}$ bit of scalar $k$. The point multiplication is computed recursively by projective PA and PD operations without using the $Y$ coordinate. Therefore, the numbers of the field multiplications are reduced. This is an important property of Algorithm 6. In the final step of the algorithm, the projective coordinate is converted to the affine coordinate. In Montgomery ladder algorithm, both PA and PD are done simultaneously for each bit of scalar $k$, so the power trace has regular and unified form.

**Algorithm 5 $\tau$NAF method for point multiplication**

Input: $k = (k_{l-1}, k_{l-2}, \ldots, k_2, k_1, k_0), P \in \mathbb{F}_q$

Output: $kP$

1. Compute $\tau$NAF($k$) $= \sum_{i=0}^{l-1} u_i \tau^i$
2. if $u_{l-1} = 1$ then $Q \leftarrow P$ else $Q \leftarrow -P$
3. end if
4. for $i$ from $l-2$ downto $0$ do
5. $Q \leftarrow \varphi(Q)$
6. if $u_i = 1$ then $Q \leftarrow Q + P$
7. end if
8. if $u_i = -1$ then $Q \leftarrow Q - P$
9. end if
10. end for
11. Return $Q$

**Algorithm 6 Montgomery ladder algorithm for point multiplication**

Input: $k = (k_{l-1}, k_{l-2}, \ldots, k_2, k_1, k_0), k_{l-1} = 1, P \in \mathbb{F}_q$

Output: $kP$

1. $Q_1 \leftarrow P, Q_2 \leftarrow 2P$
2. for $i$ from $l-2$ downto $0$ do
3. if $k_i = 1$ then
4. $Q_1 \leftarrow Q_1 + Q_2, Q_2 \leftarrow 2Q_2$
5. else
6. $Q_2 \leftarrow Q_1 + Q_2, Q_1 \leftarrow 2Q_1$
7. end if
8. end for
9. Return $Q_1$

For GLV curves, the cost for the computation of a point multiplication can be significantly reduced by efficiently-computable endomorphism. This endomorphism allows one to accomplish an $m$-bit point multiplication $kP$ by a computation of the form $k_1P + k_2Q$, where $k_1, k_2$ have only half the length of $k$ [17]. The two half-length point multiplications can be carried out simultaneously via Shamir’s trick, which takes $m/2$ point doubling and roughly $m/4$ additions when $k_1, k_2$ are represented in Joint Sparse Form (JSF). Therefore, $k_1P + k_2Q$ can be computed by a *Simultaneous multiple point multiplication* type algorithms.

Comparisons between the implementations of point multiplication in Montgomery ladder by Lopez and Dahab coordinate system and binary Edwards curves shows the traditional Weierstrass curves perform faster than the recently proposed binary Edwards. But, the main advantage of using binary Edwards curves compared to other forms of elliptic curves is their complete formulas, that is providing hardware implementation which works for any inputs.

4 Finite field arithmetics

Elliptic curves can be defined over any field such as field of rational numbers, real numbers, and complex numbers. For cryptographic application, elliptic curve is defined over finite fields. There are different finite fields and representations for use in ECC. Two important finite fields for hardware implementation are binary fields $\mathbb{F}_{2^m}$ and prime fields $\mathbb{F}_p$ [25]. The field operations required to implement the elliptic curve point multiplication are field multiplication, field addition, field squaring and field inversion.
4.1 Field arithmetic over $\mathbb{F}_{2^m}$

Binary finite fields $\mathbb{F}_{2^m}$ are defined as a vector space with dimension equal $m$ over $\mathbb{F}_2$ rather a basis. A basis can be represented by set of elements $\{e_0, e_1, \ldots, e_{m-1}\}$ in $\mathbb{F}_{2^m}$. In this case, each element in the field, i.e. $A \in \mathbb{F}_{2^m}$ can be represented as $A = \sum_{i=0}^{m-1} a_i e_i$, where $a_i \in \mathbb{F}_2$. There are different basis for $\mathbb{F}_{2^m}$, polynomial basis (PB) and normal basis (NB) are the most used basis in cryptographic applications over binary finite fields. In the normal basis representation field squaring is cost free, it is implemented by a simple cyclic shift, but in polynomial basis it is based on an array of XOR gates if irreducible polynomial of the field is an irreducible pentanomial or trinomial. In the literature polynomial basis is the most used, due to the field multiplier in this basis is more efficient than that of the normal basis. In following polynomial basis and normal basis representation are explained briefly.

4.1.1 Polynomial basis representation

The irreducible polynomial $P(x) = x^m + p_{m-1}x^{m-1} + \ldots + p_1x + p_0$ with degree $m$ and $p_i \in \mathbb{F}_2$ is called reduction polynomial. If $\alpha$ be one roots of the $P(x)$, i.e. $P(\alpha) = 0$, therefore, set $\{\alpha^{m-1}, \alpha^{m-2}, \ldots, \alpha^2, \alpha, 1\}$ is a polynomial basis (or canonical basis). In this case, elements of the field $\mathbb{F}_{2^m}$ are presented based on set of the polynomials with degrees $0 \leq d \leq m - 1$ such as $A(x) = a_{m-1}x^{m-1} + a_{m-2}x^{m-2} + \ldots + a_1x + a_0$, where $a_i \in \mathbb{F}_2$. Also, the polynomial $A(x)$ is simply given by its coefficients in $\mathbb{F}_2$ as the $m$-bit number $(a_{m-1}, a_{m-2}, \ldots, a_1, a_0)$, that is the binary representation of the corresponding element in $\mathbb{F}_{2^m}$. In the polynomial basis, numbers 0 and 1 are represented by $0 = (0, 0, \ldots, 0, 0)$ and $1 = (0, 0, \ldots, 0, 1)$ respectively. As know, the number of nonzero terms in the irreducible polynomial $P(x)$ must be an odd number. On the other hand, complexity of the field arithmetics is depends on the number of nonzero terms in the irreducible polynomial, so that lower number of nonzero terms is better for an efficient implementation because sparse polynomials offer considerable computational advantages. Therefore, first candidate for $P(x)$ is irreducible trinomials (three nonzero terms) and other candidate is irreducible pentanomials (five nonzero terms). In practice, these two irreducible polynomials have the most widely used in the implementations.

- Trinomial basis representation

For binary finite fields which are generated by irreducible trinomials, the reduction polynomial is defined as $T_{m,k}(x) = x^m + x^k + 1$, where $0 \leq k \leq m - 1$. A trinomial is irreducible if only if it’s Reciprocal polynomial, i.e. $T_{m,m-k}(x) = x^mT_{m,k}\left(\frac{1}{x}\right) = x^m + x^{m-k} + 1$ be irreducible. Hence, we should be interested in trinomials of the form only $T_{m,k}(x) = x^m + x^k + 1$, where $1 \leq k \leq m/2$ [26]. Such trinomials exist for certain values of $m$ only. If they exist, we should choose the reduction polynomial with the smallest $k$. Such a trinomial are the most efficient for the point multiplication implementation.

- Pentanomial basis representation

The reduction polynomial in this case is an irreducible pentanomial as follows:

$$P(x) = x^m + x^{k_3} + x^{k_2} + x^{k_1} + 1, \quad 1 \leq k_1 \leq k_2 \leq k_3 \leq m - 1$$

Irreducible pentanomials $P(x)$ always exist for $m \geq 4$. In practice, it is recommended to use pentanomials whose coefficient triples $k_1, k_2, k_3$ or $k_3, k_2, k_1$ will have the first coefficient as small as possible and next coefficients are kept as small as possible after fixing the previous one or ones in the triple order [26]. These irreducible pentanomials are efficient for computations of the field operations and reduce hardware and time complexity.
4.1.2 Normal basis representation

Normal basis representation can be defined for any finite field $\mathbb{F}_q$, where $q$ is a power of a prime number. A normal basis for $\mathbb{F}_{2^m}$ over $\mathbb{F}_2$ is shown as follows:

$$B = \{\beta^{2^{m-1}}, \beta^{2^{m-2}}, ..., \beta^{2^2}, \beta^2, \beta^0\}$$

where $\beta \in \mathbb{F}_{2^m}$ and it is called generator of base $B$. For any binary field, always exists a normal basis $B$. Each normal element such as $A$ is represented as follows:

$$A = \sum_{i=0}^{m-1} a_i \beta^i = a_{m-1}\beta^{2^{m-1}} + a_{m-2}\beta^{2^{m-2}} + ... + a_2\beta^2 + a_1\beta + a_0\beta$$

where $a_i \in \mathbb{F}_2$. In the vector representation, similar to polynomial basis, for the element $A$ we have the $m$-bit number $(a_{m-1}, a_{m-2}, ..., a_1, a_0)$. In this basis, zero element and multiplicative identity can be represented by $(0, 0, ..., 0, 0)$ and $(1, 1, ..., 1, 1)$ respectively.

- Gaussian normal basis

The Gaussian normal basis (GNB), is a special class of normal basis. The field multiplication is performed simpler and more efficient in GNB [27] and [7]. The complexity of the GNB multiplication is measured by its type, which is a positive integer related to the number of nonzero entries of the multiplication matrix. Therefore, a more efficient multiplier has a smaller type. The GNB is considered in several standards such as IEEE P1363 [7] and NIST [9]. For example these two standards recommended even types $T$, which is a positive integer related to the number of nonzero entries of the multiplication matrix. Therefore, a GNB of type $1$ or $2$ exists. In more details, for the given positive integers $m$ and $T$, if $p = mT + 1$ be a prime number such that $gcd(h, m) = 1$, where $h = \frac{mT}{k}$ and $k$ is the multiplicative order of $2$ modulo $p$, then a GNB over $\mathbb{F}_{2^m}$ of type $T$ exists. The GNBs with odd values of $m$ are applicable for cryptography, that implies $T$ is an even number.

- Optimal normal basis

The optimal normal basis (ONB) is a GNB of type $1$ or $2$ that provide the most efficient multiplication algorithm among all other normal bases [28]. For ONB the number of nonzero entries of the multiplication matrices is minimum and is equal $2m-1$. The ONB of type $1$ or $2$ are defined as follows [28]:

1. ONB of type-1 exists if $m + 1$ is a prime number and ‘2’ is a primitive element of the prime field $\mathbb{F}_{m+1}$.
2. In $\mathbb{F}_{2^m}$ ONB of type-2 exists if $m + 1$ is a prime number and either ‘2’ is a primitive element in $\mathbb{F}_{2m+1}$ or $2m + 1 \equiv 3 (mod 4)$ and the order of ‘2’ in $\mathbb{F}_{m+1}$ is $m$.

- Addition in $\mathbb{F}_{2^m}$

Addition is the simplest field operation in among other field operations over $\mathbb{F}_{2^m}$. It is a bit-wise addition in $\mathbb{F}_2$ which is implemented by XOR gates in hardware. For example, for addition of two field elements $A, B$ in binary fields we have:

$$A(x) + B(x) = \sum_{i=0}^{m-1} ((a_i + b_i \mod 2)) x^i = \sum_{i=0}^{m-1} (a_i \oplus b_i) x^i = (a_{m-1} \oplus b_{m-1}, a_{m-2} \oplus b_{m-2}, ..., a_1 \oplus b_1, a_0 \oplus b_0)$$
**Squaring in \( \mathbb{F}_{2^m} \)**

Squaring of the element \( A(x) = a_{m-1}x^{m-1} + a_{m-2}x^{m-2} + \ldots + a_1x + a_0 \) in polynomial basis is a linear operation, such that

\[
C(x) = \sum_{i=0}^{m-1} c_i x^i = A^2(x) = \sum_{i=0}^{m-1} a_i x^{2i} = a_{m-1}x^{2(m-1)} + a_{m-2}x^{2(m-2)} + \ldots + a_0
\]

The vector representation of \( A^2(x) \) is obtained by inserting a '0' bit between consecutive bits of the vector representation of \( A(x) \), i.e.

\[
\begin{pmatrix}
(a_{m-1}, a_{m-2}, \ldots, a_1, a_0) \\
\end{pmatrix}
\]

(as an array of XOR gates [30], [31]). Fig 3 shows the squaring in polynomial basis.
Also in normal basis the squaring of element \( A \) is expressed as:

\[
A^2 = \left( \sum_{i=0}^{m-1} a_i \beta^{2i} \right)^2 = \sum_{i=0}^{m-1} a_i \beta^{2i+1} = a_{m-1} \beta + \sum_{i=1}^{m-1} a_{i-1} \beta^{2i}
\]

This means \( A^2 \) is represented by \( (a_{m-2}, a_{m-3}, \ldots, a_2, a_1, a_0, a_{m-1}) \). So, one important property of the normal basis representation is that the squaring is performed very efficiently by a simple one-bit cyclic shift.

- **Multiplication in \( \mathbb{F}_{2^m} \)**

There are three main architectures for implementation of finite field multipliers consist of bit-serial, digit-serial (or word-level) and bit-parallel. The bit-serial structures need very low hardware resources but on the other hand, the complete output bits are computed after \( m \) clock cycles because one bit of the output is processed at each clock cycle. These architectures are suitable for lightweight cryptosystems. In digit-serial architectures, there is a trade-off between number of clock cycles and area; therefore digit-serial architecture can be a better choice for hardware implementation of the elliptic curves point multiplication. The third architectures are bit-parallel multipliers in which the output is computed in one clock cycle. However, the critical path delay and area are increased. The area consumption in the digit-serial architectures is higher than that of the bit-serial, but it is much lower than the bit-parallel architectures.

If finite field \( \mathbb{F}_{2^m} \) is generated by irreducible polynomial \( P(x) = x^m + \sum_{i=0}^{m-1} p_i x^i \) for multiplication of two elements \( A(x) = \sum_{i=0}^{m-1} a_i x^i \) and \( B(x) = \sum_{i=0}^{m-1} b_i x^i \) we have following steps [29]:

\[
S(x) = A(x) \times B(x) = \sum_{k=0}^{2m-2} s_k x^k
\]

where for coefficients of \( s_k \) we have

\[
s_k = \sum_{i+j=k \leq i, j \leq m-1} a_i b_j \quad k = 0, 1, 2, \ldots, 2m - 2
\]

The \( S(x) \) must be reduced with module \( P(x) \)

\[
C(x) = S(x) \mod P(x) \Rightarrow C(x) = \sum_{i=0}^{m-1} c_i x^i, \quad c_i \in \mathbb{F}_2
\]

There are different methods for polynomial basis multiplication such as Mastrovito method, Karatsuba-Ofman algorithm, bit-serial MSB method, bit-serial LSB method, Least Significant Digit-serial (LSD) method, Interleaving method, Two-Step method, Matrix-Vector method and Montgomery method for more details see [32], [33], [34], [35], [36] and [37].

Also for multiplication two normal elements \( A = \sum_{i=0}^{m-1} a_i \beta^{2i} \) and \( B = \sum_{j=0}^{m-1} b_j \beta^{2j} \)

\[
C = A \times B = \sum_{i=0}^{m-1} a_i \beta^{2i} \times \sum_{j=0}^{m-1} b_j \beta^{2j} = \sum_{i=0}^{m-1} \sum_{j=0}^{m-1} a_i b_j \beta^{2i} \beta^{2j} = \sum_{k=0}^{m-1} c_k \beta^{2k}
\]

for \( \beta^{2i} \beta^{2j} \) we have

\[
\beta^{2i} \beta^{2j} = \sum_{k=0}^{m-1} c_k \lambda^{(k)}_{i,j} \beta^{2k}, \quad \lambda^{(k)}_{i,j} = 0 \text{ or } 1
\]

which \( \lambda^{(k)} \) is \( m \) dimensional matrix called multiplication matrix with entries \( \lambda^{(k)}_{i,j} \). So, coordinates of \( C \), i.e., \( c_k \) are as follows:
\[ c_k = \sum_{i=0}^{m-1} \sum_{j=0}^{m-1} a_i b_j \lambda_{i,j}^{(k)} \]

More details for computation of \( \lambda_{i,j}^{(k)} \) and normal basis multiplication is presented in [38] and [39].

The GNB multiplication of \( C = A \times B \) can also be computed by the following approach [7]. Let \( \mathbb{F}_{2^m} \) has a GNB of type \( T \). Also let \( u \) be an integer of order \( T \text{ mod } p \), where \( p = mT + 1 \) is a prime number. Then, the set

\[ Z = \{ z_{i,j} : z_{i,j} = 2^i u^j | i \in \{0, 1, ..., m-1\}, j \in \{0, 1, ..., T-1\} \} \]

is a reduced residue system modulo \( p \). Therefore, each positive integer \( x \) less than \( p \) can be uniquely represented as \( x = z_{i,j} \text{ mod } p \). Let \( F \) be a function given by:

\[ F(x) = i, \ x = z_{i,j} \text{ mod } p, \quad \text{and} \quad F : \{1, 2, ..., p-1\} \rightarrow \{0, 1, ..., m-1\} \]

for an even type \( T \), the first coordinate \( c_0 \) of product \( C \) is computed by:

\[ c_0 = \sum_{k=1}^{p-2} a_{F(k+1)} b_{F(p-k)} \]

Also, other coordinates \( c_i, 1 \leq i \leq m-1 \), are computed similarly by one bit right cyclic shift of inputs [40]-[41]. Normal basis multiplication approaches and comprehensive comparisons for GNB and ONB multiplier structures can be found in [39]-[41].

- **Inversion in \( \mathbb{F}_{2^m} \)**

There are mainly two ways of computing field inversion. The first is to use the extended Euclidean algorithm. The second method is to use the Fermat’s little theorem in the multiplicative group of the finite field. If \( A \) be a nonzero element in \( \mathbb{F}_{2^m} \), then one element such as \( C \) exist which satisfies in following equation:

\[ A \times C = 1 \]

here the \( C \) element is called invert of \( A \).

In general, for computation of inversion in any finite field one can use the multiplicative structure of the group of the nonzero elements with Lagrange’s theorem. In particular, for the binary field \( \mathbb{F}_{2^m} \) and for any nonzero element \( A \) we have:

\[ A^{2^m-1} = A.A^{2^m-2} = 1 \]

Therefore, for binary fields the computation of the inversion of \( A \) can be performed by the modular exponentiation \( A^{2^m-2} \). This computation can be done using the basic Square-Multiplication algorithm [42]. In this algorithm inversion is computed with \( m-1 \) squaring and \( m-2 \) multiplication operations. An efficient method to compute the inversion in \( \mathbb{F}_{2^m} \) based on the Fermat’s little theorem is proposed by Itoh and Tsuji in [43]. In their algorithm the number of multiplication is reduced to \( \log_2^{m-1} + HW(m-1) - 1 \). The hardware implementations of the inversion operation in the literature often use the Itoh-Tsuji algorithm (ITA) for the point multiplication. In [30], [44] and [45] recent hardware implementations of ITA on polynomial basis and normal basis are presented. Also Euclidean-based inversion algorithms which are presented in [46] are consist of Extended Euclidean Algorithm (EEA), Almost Inverse Algorithm (AIA), Modified Almost Inverse Algorithm (MAIA).
4.2 Field arithmetic in $\mathbb{F}_p$

One of the popular fields which are choice for ECC are prime fields with large prime characteristic. To hardware implementation of the ECC over $\mathbb{F}_p$ we have various choices for prime number $p$. In following, we present these choices based on [47].

- **General Primes**

  In general prime fields the number $p$ has not a special pattern. Therefore, implementation of modular field arithmetics are not very efficient. The most hardware implementations for these prime numbers are based on Montgomery method [48]. In this method uses a special representation to perform efficient arithmetic, the division and remaindering are essentially implemented by shift operation.

- **Generalized Mersenne Primes**

  Special primes are highly suited for efficient reduction techniques, the most simple form of such primes being the Mersenne primes, which are primes of the form $p = 2^k - 1$. Generalization on the Mersenne primes is considered in literature because in practice the number of Mersenne primes of the correct size for cryptography is limited. In [49] the use of primes of the form $p = 2^k - c$, where $c$ is a small integer is proposed. Primes of the form $p = 2^k \pm c$ for a small value of $c$ are called pseudo-Mersenne primes. NIST recommended five efficient prime fields, with prime numbers: $p_{192} = 2^{192} - 2^{64} - 1$, $p_{224} = 2^{224} - 2^{96} + 1$, $p_{256} = 2^{256} - 2^{244} + 2^{192} + 2^{96} - 1$, $p_{384} = 2^{384} - 2^{128} - 2^{96} + 2^{32} - 1$ and $p_{521} = 2^{521} - 1$.

- **Addition and Subtraction in $\mathbb{F}_p$**

  Addition in $\mathbb{F}_p$ has carry bit which is propagates in the structure. This leads to long critical path delay and reduce operating frequency for fields with a large prime $p$ in a hardware implementation. The modular addition is defined as the computation of $S = A + B \pmod{p}$ given the integers $A$, $B$ and $p$, where $A = \sum_{i=0}^{m-1} a_i 2^i$ and $B = \sum_{i=0}^{m-1} b_i 2^i$ are $m$-bit positive integers with $0 < A, B < p$. One of the efficient method for computation of the modular addition and subtraction is Omura’s method [50]. The modular addition is computed as follows:

  $$S = A + B \pmod{p} = \begin{cases} 
  A + B - p, & A + B \geq 2^m \text{ or } A + B - p \geq 0 \\
  A + B & \text{otherwise}
  \end{cases}$$

  and for modular subtraction we have

  $$S = A - B \pmod{p} = \begin{cases} 
  A - B + p, & \text{if } A - B < 0 \\
  A - B & \text{otherwise}
  \end{cases}$$

  Fig.4 shows circuits for modular addition and subtraction.
A modular addition over $\mathbb{F}_p$ is implemented by using two adders. The two elements $A$ and $B$ are added together by the first adder. Then, the second one subtracts the modulus $p$ based on carry bit of the first adder. To reduce the critical path delay, the implemented adders for $\mathbb{F}_p$ are based on carry propagate adders such as carry skip adder, carry select adder, carry lookahead adder, carry delayed adder and carry save adder. See [32]-[34] for algorithms, structures and more details.

- **Multiplication in $\mathbb{F}_p$**

  The modular multiplication of two elements $A$ and $B$ in $\mathbb{F}_p$ is defined as product of these two field elements modulo $p$

  \[ C = A \times B \pmod{p} \]

  where $A, B, C, p \in \mathbb{F}_p$ and $A, B < p$. There are many different methods for computation of the modular multiplication consist of multiply and then divide, Interleaved modular multiplication, Brickell’s method, Montgomery modular multiplication, Bipartite modular multiplication and Tripartite modular multiplication [52], [54] and [51]-[52]. The Montgomery multiplication is the most used in between other modular multiplication methods. Montgomery multiplication of $A$ and $B \pmod{p}$, is defined as $A \times B \times 2^k \pmod{p}$ for some fixed integer $k$. Algorithm 7 shows the Montgomery modular multiplication.

---

**Algorithm 7** Montgomery Modular Multiplication

**Input:** $A, B < p < 2^k$, with $2^{k-1} < p < 2^k$ and $p = 2t + 1$, with $t \in \mathbb{N}$

**Output:** $u = A \times B \times 2^k \pmod{p}$.

1. $u = 0$
2. for $i$ from 0 to $k-1$
3.   $u = u + a_i.B$
4.   **if** $u_0 = 1$ **then**
5.     $u = u + p$
6.   **end if**
7. $u = u \div 2$
8. **end for**
9. **if** $u \geq p$ **then**
10.   $u = u - p$
11. **end if**

In Montgomery method, the operations are computed based on shift (division by 2) and addition which leads to efficient implementation. Therefore, this is the most important property of the algorithm.
• **Inversion in \( \mathbb{F}_p \)**

If for nonzero element \( A \in \mathbb{F}_p \) we have \( A \times B = 1 \mod p \) or \( B = A^{-1} \mod p \), where \( B \in \mathbb{F}_p \), then \( B \) is inverse of \( A \) in \( \mathbb{F}_p \). There are two general approaches, similar to binary fields, for find \( B \). The first is based on Fermat’s little theorem which can be implemented by modular exponentiation and the second is based on the extended Euclidean \( (\text{GCD}) \) algorithm.

The Fermat’s little theorem states that for the prime number \( p \) and for any integer \( A \) not divisible by \( p \), we have,

\[
A^{p-1} \equiv 1 \pmod{p}
\]

We write \( A \times A^{p-2} \equiv 1 \pmod{p} \), that means, \( A^{-1} \equiv A^{p-2} \pmod{p} \). So, the inversion of \( A \) can be performed by the modular exponentiation \( A^{p-2} \). The disadvantage of this approach is high execution time \([34]\). In another approach to inversion is implemented based on extended Euclidean algorithm. The more efficient methods in this type of approaches are **Kaliski Inversion for Montgomery Domain** and **Almost Montgomery Inverse \((AMI)\)** \([34]\). In \([34]\) and \([38]\) more detailed information about modular inversion in \( \mathbb{F}_p \) are presented.

### 5 Implementation of the elliptic curve cryptography: Methods, Steps and Considerations

The hardware implementation of ECC has two important stages that both have direct impact on the efficiency of the implementation. In the first stage, type of elliptic curve, finite field, point multiplication algorithm and structures related to field operations are selected. And in the second stage, the hardware architecture of the circuit in two levels of time scheduling of field operations, based on available resources and design of microarchitecture of field operations is implemented. Overall architecture for computation of the elliptic curve point multiplication is shown in Fig. 5.

![Figure 5: Overall architecture for computation of the elliptic curve point multiplication.](image)

Fig. 6 shows more details of the hardware implementation of the elliptic curve point multiplication with aims and related works in each step. As seen from this figure, implementation is split into four steps: (1) Mathematical review (study) of elliptic curves and finite fields. (2) Implementation of the field operations. (3) Implementation of the point multiplication algorithm. (4) Verification of the circuit performance and report the hardware resources and timing characteristics. Main details of the first step, second step, third step and fourth step of the hardware implementation of the elliptic curve point multiplication are shown in Figs. 7(a), (b), (c) and (c) respectively.
Figure 6: Steps of the hardware implementation of the elliptic curve point multiplication with aims and related works in each step.

Figure 7: Main details of the first step (a), second step (b), third step (c) and fourth step (d) of the hardware implementation of the elliptic curve point multiplication
5.1 Design Considerations for the hardware implementation of the elliptic curve cryptography

Different hardware implementation of the elliptic curve point multiplication are proposed. In the following main design considerations for the hardware implementation of the ECC in the different level of speed, efficiency, reconfigurability and hardware consumption are present.

- **Flexibility**

Flexibility and reconfigurability of ECC implementations make them one of the best choice for high-performance applications. It allows designing ECC implementations that are optimized for support several parameters such as arbitrary elliptic curve, different standards, fields, algorithms and coordinate choices can be achieved through re-configuration. In this case, implementation of the cryptographic algorithms in hardware are preformed without losing flexibility. But in specific structures, ECC implementation are optimized based on only specific parameters such as one field size, one irreducible polynomial in binary field, one prime number as modulo in prime fields. The flexible ECC implementation are usually based on hardware-software codesign approach. The structure is implemented by a parameterized module generator, which can accommodate arbitrary parameters. The control part of the processor is microcoded, enabling curve operations to be incorporated into the processor. The microcoded approach also has a shorter development time, algorithmic optimization and is more flexible. Fig.8 shows overall block diagram of flexible processor.

![Overall block diagram of flexible processor.](image)

Dual-field ECC processor are traditional flexible implementation. General block diagram of Dual field ECC processor is shown in Fig[8]. In this structure, arithmetic unit support both field operations on $\mathbb{F}_p$ and $\mathbb{F}_{2^m}$. It is consists of a control unit, dual-field ALU, ROM memory, register file and standard advanced microcontroller bus architecture (AMBA) advanced high-performance bus (AHB) interface. By initializing memory with curve parameters and instruction codes, the processor can flexibly perform arbitrary elliptic curve operations over dual-field and different point multiplication algorithms.
Scalability

One of the important subject when designing crypto-processor is scalability. It is the ability to perform cryptographic operations with support various field sizes (for various level of security) and irreducible polynomials (or modulo in prime field) without reconfiguration. In this case, the performance and power consumption of crypto-processor can be controllable. There are two primary approaches for realization of scalable crypto-processor. The first approach is over-designing. It is based on consideration of require hardware for performing the full field operation but the total clock cycles are decreased when performing cryptographic operations with minimum level of security. The second approach is the hardware-software codesign method. In this method the minimum bit size for operations (proper to minimum level of security) implements in hardware and uses software to perform the extension to maximum bit size.

Security

The security is one of the most issues in the ECC implementation. Countermeasures to attacks consist of power, timing and electromagnetic radiation must be considered until leaks no information about the bit pattern of the secret key. In a side-channel attack the implementation is under attack by power consumption and execution time of operations. Bit pattern of the scalar $k$ in the point multiplication can be approximated based on power consumption and picks on power trace in a simple power attack (SPA). Montgomery ladder algorithm is highly regular for each bit of scalar $k$. In other words, for any bit of $k$ the point addition and point doubling are computed simultaneously. Therefore, the power trace has a unified and bit pattern of $k$ is not visible from the power trace. In timing analysis attack which is a side-channel attack, the time taken to execute cryptographic algorithms is analyzed for compromise a cryptosystem. To resistant against this attack, the implementation must be reduces data dependent timing information. So, in the implementation of the point multiplication execution time for each point multiplication must be fixed and independent from inputs and scalar number $k$.

Implementation platforms

The the most of the hardware implementations of ECC are realized based on FPGA design and ASIC design. FPGAs are reconfigurable platforms, so the functionality of the implementation can be modified through reconfiguration. For ASIC implementations, the circuit is specialized forever. It should be noted that low number of papers about full-custom implementation of the point multiplication in chip-level have been found.
5.2 Different used techniques and the proposed ideas for hardware implementations of the elliptic curve cryptography

- Pipelining and Fine-Grain pipelining

In pipelining technique we use registers between field operations in the data path to reduce critical path delay. Therefore, pipelining of data path of the point multiplication can increase operation frequency and processing speed. Besides using pipelining of data path, to further increase speed and throughput in implementations the Fine-Grain pipelining technique is employed. In this case, in addition data path, field operations are pipelined. Fig. 10 shows implementation of the Fine-Grain pipelining technique for field multipliers. In this figure 2 field multipliers shown at left are broken into 4 smaller and faster parts in right. Breaking and replacing slower parts with some faster units in pipeline architecture will increase clock frequency and throughput of the circuit. As shown in the figure for desired operation frequency, the multiplier is broken into two smaller units with lower critical path delay than that of original structure.

![Figure 10: (a) Pipelined structure and (b) implementation of the Fine-Grain pipelining technique for field multipliers.](image)

In Figs. 11 (a) and (b) show the scheduling of Fig. 10 (a) (pipelined) and Fig. 10 (b) (Fine-Grain pipelined) respectively. It can be seen that the number of field operations processed in the structure with Fine-Grain pipelined is more than that of in pipelined structure.

![Figure 11: (a) The scheduling of Fig. 10 (a) and (b) the scheduling of Fig. 10 (b).](image)

- Retiming: minimize the clock period and the number of registers in the circuit

Retiming is a technique for optimizing sequential digital circuits. It repositions the registers between the combinational parts of digital circuits. The main aim of retiming is to find a digital circuit with the minimum
number of registers for a specified clock period. There are two general approaches; minimizing the clock period of the circuit without regard to the number of registers and minimizing the number of registers in the circuit with no constraints on the clock period [53]. For explain the concept of retiming, consider a simple circuit in Fig.12(a), where delay of each gate is shown inside it. The typical clock period for this circuit is given by the maximum delay of critical path of gates. So, in Fig.12(a) the clock period is 6ns. In Fig.12(b) an equivalent circuit with three D flip-flops and clock period of 4ns can be obtained by repositioning D flip-flops. This circuit has the minimum number of D flip-flops. On the other hand, the minimum clock period achievable by moving D flip-flops is 2ns at a cost of 4 D flip-flops as shown in Fig.12(c).

Therefore, a simple reconfiguration of D flip-flops product designs with differing area costs (number of D flip-flops) and performance (clock period). The retiming handles a trade-off between area and performance to provide solutions for varying clock periods. This technique can be proposed as an efficient method for hardware implementation of ECC.

• **Scheduling of the underling field arithmetics:** Parallel processing and Resource sharing

To efficient implementation of the point addition and point doubling based on selected coordinate and also management of hardware consumption and computation time, we can use proper scheduling. The scheduling of point multiplication operations must be carefully performed. A suitable parallelization of the operations can be employed based on the scheduling of the underling field arithmetics in the point addition and point doubling computation. It can be implemented by performing point addition and point doubling, in each loop iteration of the point multiplication, concurrently. The limitations of the parallel processing method is hardware resources. In the ECC processors, computation time is one of the most important factor that is considered in all previous works (specially in FPGA-based implementations). In the binary Weierstrass curves, the point addition and point doubling formulas are performed in parallel by using two levels of multiplications. In more details, for example computation of PA and PD in LD coordinate requires 6 field multipliers as follows:

---

Figure 12: A simple circuit (a), retiming for minimum registers (b) and retiming for minimum period (c).
The point addition \((Z_a, X_a) = Add(X_1, Z_1, X_2, Z_2, x)\) is given by:

\[
Z_a = (X_1 \times Z_2 + X_2 \times Z_1)^2, \quad X_a = xZ_a + (X_1 \times Z_2) \times (X_2 \times Z_1)
\]

and for point doubling \((X_d, Z_d) = Double(X_1, Z_1, b)\), we have:

\[
Z_d = X_d^2 \times Z_1^2, \quad X_d = X_1^4 + bZ_1^4.
\]

The parallel point addition and point doubling operations are computed in at least three steps due to the data dependency of the formulas. And, in each step at most three field multiplier are used. In the first step the three multiplications \(A = X_1 \times Z_2, B = X_2 \times Z_1\) and \(X_1^2 \times Z_1^2\) are computed in parallel by multipliers \(M_1, M_2\) and \(M_3\) respectively. In the second step \(A \times B, x \times Z_a\) and \(b \times Z_1^4\) are performed similarly. Now if we have restriction on hardware resources these computation based on two field multipliers can be implemented in three steps.

\[
\text{Step } - 1 = \begin{cases} 
  t_1 = X_1 \times Z_2 \xrightarrow{by} M_1, \\
  t_2 = X_2 \times Z_1 \xrightarrow{by} M_2 
\end{cases}
\]

\[
\text{Step } - 2 = \begin{cases} 
  x \times Z_a \xrightarrow{by} M_1, \\
  t_1 \times t_2 \xrightarrow{by} M_2 
\end{cases}
\]

\[
\text{Step } - 3 = \begin{cases} 
  X_1^2 \times Z_1^2 \xrightarrow{by} M_1, \\
  b \times Z_1^4 \xrightarrow{by} M_2 
\end{cases}
\]

The scheduling of parallel computation of the point addition and point doubling of binary Weierstrass curves is shown in Fig[13](a). In Fig[13](b) the scheduling of the resources is performed to reduce the number of clock cycles. In Fig[13](b) six field multiplication operations for the point addition and point doubling are implemented by three and two multipliers by resource sharing in separate steps.

![Figure 13](image.png)

Figure 13: Scheduling with restriction on hardware resources based on two field multipliers (a), the resource allocation to reduce the number of clock cycles based on three field multipliers (b).

There are two different application scenarios: resource constrained and fast execution time. For resource constrained architectures, reduce area and power has more priority than execution time parameter. The fast execution
time scenario is specifically for servers that involve key exchange and signatures. In this application scenario there will be thousands of point multiplication requests simultaneously, and hence the server should be fast enough to satisfy the requests. Therefore, an accurate scheduling of the field operations in the point multiplication algorithm could be an efficient solution for high speed and resource constrained design. Category of the scheduling algorithms for hardware implementations is shown in Fig. 14. Future implementations could be done based on advantages of these algorithms. In [54] there are more details about scheduling algorithms.

![Figure 14: Scheduling algorithms.](image)

- **Analysis of mathematical topics related to elliptic curves:** Finite field operations and Group law operations

  Analysis of point addition and point doubling formulates, coordinate and optimization of related mathematics and algorithms of the field operations are one of the methods for efficient implementation of the ECC. In this case aim is reduce the number of field operation especially field multiplier. Also, new and modified hardware structures of the field multiplier in polynomial basis, normal basis and and prime field are introduced. This mathematical optimization can be useful for point addition and point doubling in differential addition coordinate in binary Edwards and generalized Hessian curves. One of the contributions in analysis of mathematical topics is the modify finite field operations for efficient implementation. For example, in [55] a hybrid-double multiplier is proposed. This structure performs double multiplications with a latency of $\lceil \frac{m}{d} \rceil + 1$ (where $m$ is field size and $d$ is digit size) clock cycles assuming that one clock cycle is required to load the output of the first multiplier to the input of the second multiplier. A hybrid-double multiplier is composed based on a digit-serial parallel-input serial-output (PISO) GNB multiplier, a LSD-first digit-serial serial-input parallel-output (SIPO) multiplier and a register for loading and saving intermediate results. The structure of the hybrid-double multiplier is shown in Fig. 15.

![Figure 15: Structure of the hybrid-double GNB multiplier over $\mathbb{F}_{2^m}$.](image)

- **Logical effort**

  The logical effort technique is a method for achieving the least delay for a given load in a logic circuit [56]. In the design of the field multiplier in the ECC structure, to balance the delay among the stages and to obtain a
minimum over all delay, the logical effort technique can be applied. A hardware implementation of the logical effort in the cryptographic applications can be found in [39] and [57]. This technique is suitable for high-speed hardware implementation of the ECC. We can design an algorithmic and automatics approach based on logical effort for compute size of transistors in the critical path delay for different loads. Also, in this case the best trade-offs between area and speed can be achieved.

6 Elliptic curve cryptography implementations

During the last decade, many papers about hardware implementation of ECC have been published in the literature. The most previous works have similar selection in the implementation, i.e., in selecting type of finite field, elliptic curve, point multiplication algorithm, and algorithm of field operations. For example, the Montgomery ladder and the Itoh-Tsujii algorithm are widely used for point multiplication and field inversion respectively. The aim of this section is review of the these implementations and architectures. In this survey, hardware structures of the ECC are categorized based on implementation technologies as follows:

1. Hardware implementations of the elliptic curve cryptosystems on FPGAs
2. ASIC Hardware Implementations of the elliptic curve cryptosystems

6.1 Hardware implementations of the elliptic curve cryptosystems on FPGAs

In this subsection, we review hardware architectures for ECC on FPGA. FPGA implementation leads to faster architectures which have more parallelism in performing field operations. The main parts of cryptographic applications are increasingly implemented in FPGA platforms according to the recent advancements in these applications [58]. In particular, parallel and pipelined architectures and also low-power and low-cost designs are implemented on FPGAs, such that can operate at very high data rates. Therefore, these properties and the reconfigurability of the FPGAs make them one of the best devices for high-performance and low-power reconfigurable implementation. To implement cryptographic algorithms in hardware without losing flexibility the FPGA platforms are the best choice. Reconfigurability advantage of FPGAs, allows designing ECC implementations that are optimized for specific parameters, because support for other parameters such as different fields, algorithm and coordinate choices can be achieved through reconfiguration. Here, the FPGA-based implementations are categorized based on type of finite fields into three groups. The first and second groups are implementations on binary fields and prime fields respectively. Also the third group is the FPGA-based implementations with dual-field property. The elliptic curve point multiplication with field operations over dual-fields, required for the ECC schemes such as signature, authentication and key exchange.

6.1.1 FPGA implementations of the point multiplication on binary fields

In this subsection, FPGA implementations of the point multiplication on binary fields are presented. These works are consist of [22], [25], [59]-[107] and [109]-[114]. Two works [59]-[60] are based on GLS curves. To better comparison, the implementations are categorized based on type of the curve. The efficient and popular curves are include binary Weierstrass curves, Koblitz curves, binary Edwards curves, generalized Hessian curves and binary Huff curves.

- FPGA implementations of the binary Weierstrass curves:

FPGA-based implementations of the point multiplication on binary Weierstrass curves are presented in [22], [25] and [61]-[94]. The most of these implementations are implemented by using polynomial basis representation. The main special techniques, which are used in this category of implementations are summarized as follows:
1. In [22] tools for evaluating the use of parallelism and shows where it should be used in order to maximize efficiency are provided.

2. In [25] a clock switch circuit is used to manage the clock signal so that the circuit operates at its maximum clock frequency at different steps of the Montgomery ladder algorithm.

3. In [61] a parallel version of the half-and-add method using the mixed-coordinate representation for PA, PD and point halving are implemented.

4. In [63] a parameterized generator, which can produce field multipliers with different speed and area trade-offs. The curve operations to be incorporated into the processor based on microcoded control unit.

5. In [93] three finite field RISC cores and a main controller to achieve instruction-level parallelism (ILP) for elliptic curve point multiplication based on the analysis of both data dependency and critical path is proposed.

In following, we present recent works in this category in more details. In [25] a hardware structure of the point multiplication based on Montgomery ladder algorithm for binary Weierstrass curves is presented. In this work, the PA and PD are performed concurrently in parallel by three pipelined digit-serial multipliers in polynomial basis. The field multiplier is based on a parallel and independent computation of multiplication by power of the variable polynomial. An efficient architecture of the Itoh-Tsujii inversion algorithm is implemented for field inversion more details of this architecture is presented in [30]. A clock switch circuit is used to manage the clock signal so that the circuit operates at its maximum clock frequency at different steps of the Montgomery ladder algorithm. The proposed structure for implementation of the Montgomery ladder loop iterations in [25] is shown in Fig.16. As seen in this figure the point addition and point doubling are computed independently in parallel by three multipliers.

![Figure 16: Structure for implementation of loop iterations in the Montgomery ladder algorithm proposed in [25].](image)

As known in the point multiplication algorithm, computations of coordinate conversion from projective to affine is start at the end of loop iterations. In [25] the critical path delay of the proposed circuit in loop iterations mode is
less than that of in coordinate conversion mode. Therefore, to increase the speed processing, multi-frequency clock
 technique is used. In this way, the structure can switch between two different fast and slow clock frequencies, that
determined by the different critical path delays of loop iterations part and coordinate conversion part. The structure
of the clock switch circuit and its performance is explained in [25].

In [74] two high-speed ECC implementations for point multiplication is proposed. A pipelined full-precision
field multiplier is used to reduce the latency, and the Lopez-Dahab Montgomery ladder algorithm is modified for
accurate scheduling to avoid data dependency. It the first proposed high-performance architecture includes a 2-
stage pipelined full-precision \( m \) bit field multiplier, one field squaring, one quad-squaring, and two field addition
units in order to perform point operations within 6 clock cycles. To performing operations in 6 clock cycles, squarer
block or quad-square block or both blocks in parallel along with the multiplication is applied. In this structure one
of the adders is placed in the common data path. The second adder is used to add the two outputs of the multiplier.
In addition, the circuit can save some intermediate results of the operations in the registers (accumulator) to avoid
loading/unloading to the main memory.

The second ECC implementation for point multiplication in [74] is based on three full-precision field multipli-
cers called \( Mul_1, Mul_2 \) and \( Mul_3 \) to achieve the lowest latency high-speed ECC. The one field multiplication is
pipelined by one stage so output is ready in one clock cycle. Also, the field square and field adder are performed
in the same clock cycle based on combinational logic. The field operation circuits are cascaded, therefore different
operations in the same clock cycle can achieve by tapping the results.

In [76] an efficient pipelined architecture of the point multiplication over \( \mathbb{F}_{2^m} \) is proposed. The architecture
uses a multiplier accumulator (MAC) by bit-parallel field multiplier based on the Karatsuba-Ofman algorithm. In
this work, for better sharing of execution paths the Montgomery ladder algorithm is modified. The data path in
the architecture is well designed, so that the critical path contains few extra logic primitives apart from the MAC.
To find the optimal number of pipeline stages, placement of pipeline registers is analyzed. Therefore, scheduling
schemes with different pipeline stages are proposed. The data path of implemented ECC using a three stages
pipelined MAC is shown in Fig.17 The proposed architecture consists of one bit-parallel MAC, one field squarer,
a register file, a finite state machine (FSM) and a \( 6 \times 18 \) control ROM. The inputs to field squarer and MAC are all
registered. For data caching, 4 registers \( T_1 \) to \( T_4 \) are used in the data path. A multiplexer is before each register.
The control signals \( T_1 \text{sel}, T_2 \text{sel}, T_3 \text{sel} \) and \( T_4 \text{sel} \) are given at each clock cycle to select different operations
in the point multiplication implementation. Therefore, the input delay for registers is only the delay of a 4 to 1
multiplexer. In the Fig.17 the critical path of the 3-stage pipelined architecture is shown by the bold dashed line.
The critical path is consists of a pipelined MAC, a field adder and one 4 to 1 multiplexer.
Figure 17: Data-path of elliptic curve scalar multiplication using a three stages pipelined MAC in [76].

Other recent work is presented in [80]. In this work, a theoretical model to approximate the delay of different field operations used in a point multiplication structure is implemented on \( k \) input lookup table (LUT) based FPGAs. Also a suitable scheduling for performing PA and PD in a pipelined data path of the point multiplication is implemented.

The point multiplication architecture presented in [80] uses the left to right double-and-add algorithm with binary signed digit representation. The used coordinate in the processor is Lopez-Dahab projective coordinate. The inputs of the arithmetic unit are provided by the register bank, at each clock cycle, through six buses. At the end of the clock cycle, the results of the computation are stored in the registers through buses. Control signals are generated at every clock based on the state of the FSM and key digit.

In [86] a high-speed elliptic curve point multiplication using FPGA is presented. To find out an optimal digit size different levels of digit-serial computation are applied to the data-path of field multipliers and dividers. Results for the five NIST recommended curves are provided in [86].

The point multiplication architecture presented in [86] is constructed based on three field multipliers, three field squarers, nine field adders and one field divider. In this structure, for increase speed processing the multipliers are parallel. The four output registers are used for storing of the output parameters in the point multiplication algorithm, in addition, they are employed for loading of initial values in the start of the algorithm. Table 1 shows the results of the FPGA implementations of the point multiplication on binary Weierstrass curves.
Table 1: Results of the FPGA implementations of the point multiplication on binary Weierstrass curves.

| Works(Year) | Field          | Device            | Area               | $F_{max}$ (MHz) | Time(µs) |
|-------------|----------------|-------------------|--------------------|----------------|----------|
| ![image](image.png) | VE (XC2V2000E) | 167                | 1769 Slices        | 76.7           | 210      |
| ![image](image.png) | VE (XC2V6000E) | 163                | 15527 LUTs + 3994 FFs | 98.3           | 31.17    |

The recent works [74], [76], [25] and [80] are the best time efficient implementations of the point multiplication on binary Weierstrass curves. High-throughput design presented in [91] is the best reported work in terms of area×time metric. Work presented in [74] over $\mathbb{F}_{2^{163}}$ on Virtex-7 achieves a better metric value. Also it is the fastest FPGA design to date on Virtex-7. Execution time in work [25] over $\mathbb{F}_{2^{233}}$ is 4.913µs, which is outperforms compared to other works. For Virtex-4 over $\mathbb{F}_{2^{163}}$, the previous highest speed 3-stage pipelined implementation is presented in [76] and consumed 7354 slices to achieve 6.1µs. For Virtex-4 over $\mathbb{F}_{2^{233}}$, the highest speed work is [25] with 7.84µs. For Virtex-5, the best reported performance result over $\mathbb{F}_{2^{163}}$ and $\mathbb{F}_{2^{233}}$ are 4.6µs and 6.84µs presented in [74] and [25] respectively. Point multiplication implemented in [74] consumes only 4393 slices to compute a point multiplication in 4.913µs, which is 10% and 29% better in both speed and area than that recent work [80]. The HPEC architecture in [74] over $\mathbb{F}_{2^{257}}$ is the first reported implementation based on full-precision multiplier and sets a new time record equal 37.5µs for the point multiplication on Virtex-7.
structures respectively. To have a better comparison, in these graphs the results are distinguished based on field size and type of FPGA platform. As seen in Fig.18 and Fig.19 the works [74], [76], [25] and [86] have acceptable performance in terms of speed and hardware resources.

Figure 18: Graphical representation of the execution time in the some previous FPGA-based works for binary Weierstrass curves.

Figure 19: Graphical representation of the number of Slices in the some previous FPGA-based works for binary Weierstrass curves.

- **FPGA implementations of the Koblitz Curves:**

  The first FPGA-based implementation of the point multiplication for NIST Koblitz curve K-163 is presented in [92] with computation time of 45.6\(\text{ms}\) on Altera Flex 10K FPGA. Other previous FPGA-based implementations of the Koblitz curves are presented in [95]–[107]. The main special contributions in this category of implementations are summarized as follows:

  1. In [96] a parallelization method utilizing point operation interleaving is provided.

  2. In [100] algorithms for point multiplication on Koblitz curves using multiple-base expansions of the form 
     \[ k = \sum \pm \tau^a (\tau - 1)^b \] and 
     \[ k = \sum \pm \tau^a (\tau - 1)^b (\tau^2 - \tau - 1)^c \] are described. Also, the first rigorously-proven sub-linear point multiplication using complex bases is presented.
3. In [103] presents parallelization of scalable point multiplication that can support all 5 NIST Koblitz curves without reconfiguring structure.

In following these works are discussed. The focus of the works are reducing the computation time of the point multiplication and flexibility for support all five NIST Koblitz curves. With the increase in hardware resources in recent FPGAs, designers are enabled for maximum parallelism of the several field operations in the ECC hardware implementation. For example, in [96] discuss implementation of the point multiplication on Koblitz curves with parallel field multipliers. In this work, a novel parallelization method by using interleaving of point operation is presented. The effects of field basis selection is studied in [96] and conclude that polynomial basis has faster results than normal basis.

In [97] a scalable ECC processor is presented. This ECC processor supports all five NIST Koblitz curves K-163, K-233, K-283, K-491 and K-571 without the need to reconfigure the FPGA. A finite field arithmetic unit (FFAU) that reduces the number of clock cycles is proposed. Also an improved PA algorithm to take advantage of the FFAU structure is presented. The structure computes the point multiplication after the $\tau$NAF($k$) computation, therefore it gets as inputs the point $P$ with two affine coordinates $x_1$ and $y_1$ and $\tau$NAF converted value of $k$. The outputs of the scalable structure are the two affine coordinates, $x_3$ and $y_3$, of the output point $Q = kP$.

A very high-speed FPGA-based ECC for Koblitz curves is described in [98]. It is based on a preliminary version that was presented in [95]. The implementation is optimized for both increased the performance and decreased the hardware resources for Koblitz curve K-163. In more details, the structure in [98] consists of four main components. The top level view of the structure is given in Fig.20. The converter, converts the integer $k$ into width-4 $\tau$NAF and encodes it. The preprocessor computes the precomputed points, $P_1, ..., P_N$ for algorithm right to left point multiplication algorithm on Koblitz curves with precomputations [98]. These precomputations can be performed in parallel in the preprocessor concurrently with the converter. The loop iterations of the point multiplication algorithm is performed in the main processor after two previous computations. Finally, the result point $Q = (x, y)$ is maps from Lopez-Dahab coordinate to affine coordinate by the postprocessor.

![Figure 20: Structure of the ECC processor in [98].](image)

The design of the ECC processors using two field multipliers over $F_{2^{163}}$ with digit-serial processing is presented in [102]. The field operations are implemented using GNB representation over binary field. Also the point multiplication is computed using window-$\tau$NAF algorithm with $w=2, 4, 8$ and 16. In [104] a highly parallel structure to speed up the point multiplication for high-speed FPGA implementation on Koblitz curves is presented. The PA formulas are modified in order to employ 4 parallel field multipliers in the data-flow. Therefore, the number of the clock cycles of performing PA is reduced and speed of the point multiplication is increased.

In [106] the scalar conversion process in [108] is improved based on division by $\tau^2$. Two levels of optimizations are applied in the scalar conversion structure. First, the number of long integer subtractions during the scalar
conversion is reduced. This optimization reduces the computation complexity and also simplifies the critical paths in the conversion structure. Then the architecture is pipelined.

Implementation results of the FPGA-based point multiplication on Koblitz curves are presented in Table 2. The fastest implementations on K-163 in table compute point multiplication in 4.9 $\mu$s [96] ($D=55$), 5.05 $\mu$s [102], 5.1 $\mu$s [103] ($D=41$), 5.1 $\mu$s [103] ($D=55$) and 5.2 $\mu$s [103] ($D=41$). Also on K-233 computation times are 6.8 $\mu$s ($D=78$) and 7.7 $\mu$s ($D=59$) in [103]. The fastest implementation [96] require large amounts of ALMs on Stratix-II FPGA. The work [97] has the number 2431 Slices which is the lowest area in among of the K-163 curves. Fig. 21 and Fig. 22 show graphical representation of the execution time and the number of Slices, respectively, based on type of FPGA and field size for different structures on Koblitz curves. In these figures implementation conditions for presented works are equal.

Table 2: Results of the FPGA-based point multiplication on Koblitz curves.

| Work (Year) | Field | Device | Area | $F_{max}$ (MHz) | Time ($\mu$s) |
|-------------|-------|--------|------|----------------|--------------|
| [95], PB, (2008) | 163 | SII (EP2S180F1020C3) | 16930 ALMs+21 M4Ks | 185 | 16.36 |
| [96], $D=41$, PB, (2009) | 163 | SII (EP2S180F1020C3) | 20525 ALMs | 203.87 | 5.1 |
| [96], $D=55$, PB, (2009) | 163 | SII (EP2S180F1020C3) | 26148 ALMs | 187.48 | 4.91 |
| [102], $D=59$, NB, (2009) | 163 | SII (EP2S180F1020C3) | 23806 ALMs | 182.42 | 9.48 |
| [96], $D=59$, PB, (2009) | 233 | SII (EP2S180F1020C3) | 26148 ALMs | 181.56 | 8.09 |
| [103], PB, (2013) | 163 | V4 (XC4VFX12) | 2431 Slices | 155.376 | 275 |
| [95], PB, (2011) | 163 | SII (EP2S180F1020C3) | 14280 ALMs+25 M4Ks | 187.9 | — |
| [100], PB, (2013) | 163 | SII (EP2S180F1020C3) | 14280 ALMs+25 M4Ks | 11.71 | 8.6 |
| [97], GNB, (2013) | 163 | V4 (XC4VFX12) | 2431 Slices | 155.376 | 604 |
| [22], PB, (2008) | 163 | SII (EP2S180F1020C3) | 13472 ALMs | 187.9 | — |
| [98], PB, (2011) | 163 | SII (EP2S180F1020C3) | 18236 ALMs | 187.9 | 11.71 |
| [101], PB, (2016) | 163 | SII (EP2S180F1020C3) | 13472 ALMs | 187.9 | 11.71 |
| [102], GNB, (2014) | 163 | SIV (EP4SGX180HF35C2) | 24220 ALUTs | 177.1 | 5.05 |
| [22], PB, (2008) | 163 | SII (EP2S180F1020C3) | 13472 ALMs | 155.5 | 26 |
| [103], $D=41$, GNB, (2015) | 163 | SV (SSGXMA3E2H129C2) | 12942 ALMs | 259.2 | 5.2 |
| [103], $D=55$, GNB, (2015) | 163 | SV (SSGXMA3E2H129C2) | 13472 ALMs | 234.5 | 5.1 |
| [103], $D=59$, GNB, (2015) | 233 | SV (SSGXMA3E2H129C2) | 20988 ALMs | 245.7 | 7.7 |
| [103], $D=78$, GNB, (2015) | 233 | SV (SSGXMA3E2H129C2) | 16421 ALMs | 246.1 | 6.8 |
| [104], $D=41$, GNB, (2013) | 163 | SII (EP2S180F1020C3) | 23084 ALMs | 188.71 | 9.15 |
| [105], PB, (2016) | 163 | V5 (XC5LX110T) | 2708 Slices+5 BRAMs | 222.67 | 55 |
| [107], ALU single, PB, (2008) | 233 | V2 (XC2V4000) | 14091 Slices | 51.7 | 8.72 |
| [107], ALU parallel, PB, (2008) | 233 | V2 (XC2V4000) | 15916 Slices | 51.7 | 7.22 |

$D$: Digit Size; PB: Polynomial basis; GNB: Gaussian normal basis; SII: Stratix II; SV: Stratix V; SIV: Stratix IV; V5: Virtex-5; V7: Virtex-7.

Figure 21: Graphical representation of the execution time for point multiplication on Koblitz curves.
FPGA implementations of the binary Edwards, Generalized Hessian and Huff curves:

The hardware implementations of the point multiplication presented in [109]–[114] are based on binary Edwards and general Hessian curves. In [109] a design and implementation of the binary Edwards curves processor is explained. This work is the first FPGA-based unified processor in the literature. Furthermore, the structure is explored in terms of power analysis to make the design simple power attack preventive. In [110] parallelization in higher levels by full resource utilization of computing PA and PD formulas for both binary Edwards and general Hessian curves is performed. For computing of the point multiplication, \( w \)-coordinate differential formulations are used. The authors evaluate the LUT complexity and time-area tradeoffs of the processor on an FPGA by using a LUT-based pipelined and efficient digit-level GNB multiplier.

To reduce the number of clock cycle in the point multiplication computation, an analysis of data-flow and maximum number of parallel field multipliers is used in [111]. Also the PA and PD formulas are modified. A digit-serial hybrid-double GNB multiplier is employed to reduce the data dependencies and the latency of the point multiplication. The architectures of the processors in [111] are shown in Fig. 23. The point multiplication processors are composed of four main parts including field arithmetic part (FAU), register file, control part and conversion part to obtain the final affine coordinates. In FAU part of crypto-processors for binary Edwards curves, three single digit-level parallel-in parallel-out (DL-PIPO) GNB multipliers and two hybrid-double multipliers are employed. Also for Generalized Hessian curves, in FAU part two single DL-PIPO multipliers and a hybrid-double multiplier are employed.
In [112] a high-speed binary Edwards curves point multiplication implementation is proposed based on a parallel design strategy. In this work, two field multipliers are employed and also power analysis attack resistance against a variety of attacks is provided. The hardware structure is implemented based on the parallelism layer concept. A parallelism unit (PU) realizes a single parallelism layer of the point multiplication computations. It is consists of two bit-parallel field multipliers, two field squarers and three field adders. These components operate in parallel form and output result of each component is ready with one clock cycle. Outputs of the PU components are stored in the register file (constructed by 23 registers) in order to be reused in future clock cycles. Generator irreducible polynomials of the field $\mathbb{F}_{2^m}$ are specific irreducible polynomial such as trinomial or pentanomial.

A high-speed hardware structures of the point multiplication based on Montgomery ladder algorithm for binary Edwards and generalized Hessian curves in GNB are presented in [114]. Computations of the PA and PD in the structure are simultaneously performed by pipelined digit-serial field multipliers. The field multipliers in parallel form are scheduled for reduce latency. The structure of digit-serial GNB multiplier is constructed based on regular and low-cost components of exponentiation by powers of 2 and multiplication by normal elements [40]. Therefore, the structures are area efficient and have low critical path delay. In these architectures, the point multiplication is implemented by using four and three field multipliers for $d_1 \neq d_2$. More details of the structure are presented in [114].

In [115] the first hardware design of binary Huff curves is proposed, which also lead to unified point multiplication. To a faster circuit and better utilization of the FPGA resources, several optimized architectural features have been developed. In [116] provide an efficient hardware implementation of the unified Huff formula in projective coordinates on FPGA. Also side channel vulnerability is studied with simple power analysis. It is claimed that the formula is unified and there is not power consumption difference when computing PA and PD operations. The architecture of the point multiplication on Huff curve based on left-to-right binary algorithm is shown in Fig. 24. The $Q$ registers are initialized with coordinates of input point $P$. There is a counter $i$ with counting range 0 to $m - 2$. At each loop iteration the counter helps to select the corresponding bit of the scalar $d$. Two intermediate signals $flag_1$ and $flag_2$ are for detect the on-going point operation of either PA ($P + Q$) or PD ($Q + Q$). If PA operation is going on, $flag_2$ will be enabled and $flag_1$ will be disabled. Also if PD operation is going on, $flag_1$ will be enabled and $flag_2$ will be disabled. The PA and PD operations are computed using the same block implemented using unified addition formula. After the completion of one point operation, the addition done signal will be enabled for one clock cycle during which the $Q$ registers are updated by the new intermediate result coming out from the unified point addition block. Finally, the done signal will be enabled once the point multiplication is complete.

The results of the FPGA implementations of the point multiplication on BECs, GHCs and BHCs are shown in
Table 3: Results of the FPGA implementations of the point multiplication on BECs, GHCs and BHCs.

| Works/Year | Field | Device | Area | \( f_{max} \) (MHz) | Time (\( \mu s \)) | Area x Time |
|------------|-------|--------|------|-------------------|-----------------|------------|
| [112] | BECs, \((d_1 \neq d_2)\), PB, (2012) | 233 | V4 (XC4VLX140) | 21816 Slices | 47.384 | 190 | 4.145 |
| [110] | BECs, \((d_1 \neq d_2)\), D=41, GNB, (2012) | 163 | V5 (XC5VLX110) | 5788 Slices | 264.5 | 25.3 | 0.14844 |
| [110] | BECs, \((d_1 = d_2)\), D=41, GNB, (2012) | 163 | V5 (XC5VLX110) | 5788 Slices | 264.5 | 19.8 | 0.11446 |
| [110] | GHCs, D=41, GNB, (2012) | 163 | V5 (XC5VLX110) | 5788 Slices | 267.1 | 17.7 | 0.10245 |
| [111] | BECs, \((d_1 = d_2)\), D=33, GNB, (2014) | 163 | V4 (XC4VLX110) | 27778 Slices | 217.2 | 17.5 | 0.48612 |
| [111] | BECs, \((d_1 = d_2)\), D=26, GNB, (2014) | 233 | V4 (XC4VLX110) | 29252 Slices | 198.4 | 36.3 | 1.06185 |
| [111] | BHCS, D=33, GNB, (2014) | 163 | V5 (XC5VLX110) | 15992 Slices | 218.2 | 15.9 | 0.2543 |
| [111] | BHCS, D=26, GNB, (2014) | 233 | V4 (XC4VLX140) | 10940 Slices | 205.1 | 33.1 | 0.5509 |
| [123] | BECs, \((d_1 = d_2)\), PB, (2016) | 233 | V4 (XC4VLX140) | 40793 LUTs | 67 | 49 | 1.9989 |
| [123] | BECs, \((d_1 = d_2)\), PB, (2016) | 233 | V5 (XC5VLX110) | 32874 LUTs | 132 | 25 | 4.33937 |
| [123] | BECs, \((d_1 = d_2)\), D=41, GNB, (2016) | 163 | V4 (XC4VLX110) | 27636 Slices | 247.396 | 10.52 | 0.28788 |
| [123] | BECs, \((d_1 = d_2)\), D=41, GNB, (2016) | 163 | V4 (XC4VLX110) | 20853 Slices | 247.750 | 10.49 | 0.21734 |
| [123] | BHCS, D=41, GNB, (2016) | 163 | V5 (XC5VLX110) | 29752 Slices | 247.397 | 10.54 | 0.21873 |
| [123] | BECs, \((d_1 = d_2)\), D=41, GNB, (2016) | 163 | V5 (XC5VLX110) | 11397 Slices | 302.081 | 8.62 | 0.09824 |
| [123] | BHCS, D=41, GNB, (2016) | 163 | V5 (XC5VLX110) | 8645 Slices | 302.093 | 8.6 | 0.04347 |
| [123] | BHCS, D=26, GNB, (2016) | 163 | V5 (XC5VLX110) | 8645 Slices | 302.093 | 8.62 | 0.07452 |
| [144] | BECs, \((d_1 = d_2)\), D=26, GNB, (2016) | 233 | V4 (XC4VLX110) | 13786 Slices | 333.970 | 21.6 | 0.39480 |
| [144] | BECs, \((d_1 = d_2)\), D=26, GNB, (2016) | 233 | V4 (XC4VLX110) | 333.970 | 21.6 | 0.29364 |
| [144] | BECs, \((d_1 = d_2)\), D=59, GNB, (2016) | 233 | V5 (XC5VLX110) | 14343 Slices | 337.603 | 11.03 | 0.1582 |
| [144] | BHCS, D=59, GNB, (2016) | 233 | V5 (XC5VLX110) | 8675 Slices | 337.603 | 11.03 | 0.097891 |
| [145] | BHCS, PB, (2012) | 233 | V4 (XC4VLX140) | 20437 Slices | 81 | 73 | 1.4919 |
| [146] | BHCS, PB, (2013) | 233 | V5 (XC5VLX110) | 19352 Slices | 118 | 55 | 1.06436 |
| [146] | BHCS, PB, (2013) | 233 | V6 | 7150 Slices | 172 | 43 | 0.30745 |
| [146] | BHCS, PB, (2013) | 233 | V7 | 6032 Slices | 183 | 40 | 0.24128 |

D: Digit Size; PB: Polynomial basis; GNB: Gaussian normal basis; V4: Virtex-4; V5: Virtex-5; V6: Virtex-6; V7: Virtex-7.

6.1.2 FPGA implementations of the point multiplication on prime fields

The ECC processors on prime fields utilize more hardware resources and are relatively slower than binary fields. The point multiplication implementation on prime fields can be categorized based on the modular reduction methods and modulus primes. Therefore, the prime field ECC hardware implementations can be split into three groups as follows:

- **Arbitrary prime field and curve parameters**
- **Special curves or special modulus primes such as Mersenne and pseudo Mersenne prime numbers**
- **Residue number systems (RNS) and redundant signed digits (RSD) based prime field ECC processors**

The special cases of implementations are efficient for the point multiplications, but for further applications such as digital signature generation cannot be applicable. For example, order of the base point in the ECDSA is not a special prime. Therefore, arbitrary prime fields are better for supporting the ECC such as curve transition, key...
agreement and signature generation which require the operations over another prime field. Modular multiplication is the most important operation in the elliptic curve point multiplication over \( \mathbb{F}_p \). Two main methods are employed for implementation of modular multiplication. The first method is based on Montgomery method. It is widely used in implementations of arbitrary curves. The second method is multiply-then-reduce. It is used, with efficient modular reduction, for implementation of special curves over \( \mathbb{F}_p \) where \( p \) is the generalized/pseudo-Mersenne prime. The FPGA-based implementations of the point multiplication on prime fields are presented in [117]-[155]. In this category, many of works are implemented based on the DSP blocks and embedded multipliers in FPGA. The works [117], [119], [121], [126], [131], [138]-[146], [148]-[149] and [151] utilized the inherent DSP blocks in FPGAs to optimize the area and performance. Scalable and flexible FPGA-based point multiplication implementations are proposed in [142] and [151] respectively. The hardware structure in these works support all five prime field elliptic curves recommended by NIST. The main special techniques for FPGA implementations of the point multiplication on prime fields are summarized as follows:

1. in [124] the balanced ternary representation of the point multiplication based on multiple point tripling and point addition is presented.
2. In [142] a single instruction based ultra-light ECC processor coupled with dedicated hard-IPs of the FPGAs is proposed.
3. In [152] point multiplication algorithm is based on efficient co-Z arithmetics, where addition of projective points share the same Z-coordinate. The algorithm is fast and secure against different attacks.

In [122] an application-specific instruction-set ECC processor based on redundant signed digit representation is proposed. The processor uses pipelining techniques for Karatsuba-Ofman multiplication algorithm. Also, an efficient modular adder without comparison and a high-throughput modular divider are implemented. The structure supports the NIST curve P-256. A hardware implementation of fast point multiplication using the balanced ternary representation is presented in [124]. In this implementation, uses multiple point tripling and point addition. Here, 3P, 9P, 27P, etc. are precomputed by using fast tripling and use them in preforming of the final product over \( \mathbb{F}_p \). This work is the first implementation of balanced ternary representation and pre-computation over \( \mathbb{F}_p \) on FPGA platform. In [125] a high-performance structure for the point multiplication over general prime field using Jacobian coordinates is presented. The structure is implemented based on a parallel field arithmetic unit. The field adder and subtractor are in parallel to four field multipliers. The field multiplier is optimized by radix-4 Booth encoding technique, while adder and subtractor are implemented by using available fast carry chains on FPGA. It is constructed based on the parallel arithmetic unit (PAU) unit, a register file, input/output multiplexing logic and a control unit. The PAU consists of 5 field arithmetic units. Add/Sub unit compute a single addition or subtraction operation in one clock cycle, also four multiplications can be computed in parallel by the four multipliers. The control signals are generated for execution of the respective field operation based on fetch and decode instructions.

In this architecture, a division block is used for the final conversion from Jacobian to affine coordinates.

In [141] a flexible hardware processor over five standard NIST prime fields P-192, P-224, P-256, P-384 and P-521 is proposed. The flexibility of the implementation is achieved through the software-controlled hardware programmability, which allows for different scenarios of computing atomic block sequences. A single instruction based lightweight ECC processor coupled with dedicated hard-IPs of the FPGAs is proposed in [141]. This hardware structure is the first implementation of the point multiplication which requires less than 100 Slices on Virtex-5 and Spartan-6 FPGA. A secure and efficient implementation of a special ECC processor using the Curve25519 [15] on FPGA is presented in [144]. In the structure, the DSP blocks of FPGAs are used for field operations. Also, basic multi-core DSP-based architectures achieves a high-performance of more than 32000 point multiplications per second on a Xilinx Zynq 7020 FPGA. Architecture of the Curve25519 core in [144] is shown in Fig [25]. In this structure, two dual-ported BRAMs in butterfly configuration are used. In more details, the first BRAM only receives the results of the addition or subtraction unit and provides the input to the multiplication while the second BRAM stores the multiplication result and feeds the addition unit. Therefore, parallel operation is enabled and pipeline stalls through loading and write back can be avoided with only little overhead.
The field multiplier in the arithmetic unit is consists of 18 DSP blocks, 15 DSP blocks are used to compute partial products, one for a pre-reduction and two for the final modular reduction. Computation of partial products in the field multiplier can be interleaved with the reduction step in pipeline manner. In this work, the single core design with a dedicated inverter circuit and share it among several cores are augmented for an optimal area and performance trade-off.

In [147] a high-performance scalable elliptic curve processor is presented (Fig. ??). The double-and-add algorithm is selected using mixed affine and Jacobian coordinates for PAs and Jacobian coordinates for PDs. The processor is able to support all five NIST prime field elliptic curves. To achieve high speed and low hardware resource the structure takes advantage of the DSP48E blocks available in Virtex-5 FPGA. The parallelizes of the field operations reduce the number of clock cycle of the point multiplication. To better fit the structure of the addition/subtraction/reduction (AR) block into the reduction algorithms of the five NIST primes, the internal operation of the AR block uses a 32-bit data-path.

A detailed comparison for FPGA-based implementations of the elliptic curve point multiplication on prime fields are shown in Table 4 and Table 5. Table 4 shows results of works which are implemented for arbitrary prime field or are scalable for support all NIST prime fields. Presented works in Table 5 are implemented over a special NIST prime field or are implemented on special curve.
Table 4: Results of the FPGA implementations of the elliptic curve point multiplication on arbitrary prime field and scalable works.

| Works(Year) | Prime Field | Device | Area | $F_{max}$(MHz) | Time($\mu$s) |
|-------------|-------------|--------|------|---------------|--------------|
| [117], (2016) | Arbitrary 256 | Spartan-6 | 105 Slices + 2 DSPs + 2 BRAMs | 200.4 | 9200 |
| [120], (2012) | Arbitrary 256 | V5 (XC5VLX110) | 3657 Slices + 10 DSPs | 263 | 860 |
| [123], (2012) | Arbitrary 256 | V4 (XC4VFX112) | 2901 Slices + 14 DSPs | 227 | 1090 |
| [125], (2012) | Arbitrary 256 | V4 (XC4VFX110) | 3421 Slices + 14 18*18-bit MULs | 172 | 2240 |
| [123], (2016) | Arbitrary 256 | V6 (XC6VLX110) | 32.4K LUTs | 144 | 1430 |
| [123], (2016) | Arbitrary 256 | V4 (XC4VFX140) | 35.7K Slices | 70 | 2960 |
| [125], (2016) | Arbitrary 256 | V6 | 22131 LUTs | 95 | 2010 |
| [125], (2016) | Arbitrary 256 | V5 | 31431 LUTs | 73 | 2620 |
| [125], (2016) | Arbitrary 256 | V4 | 20579 Slices | 49 | 3910 |
| [125], (2011) | Arbitrary 256 | V2 pro | 12K Slices | 36 | 9380 |
| [125], (2004) | Arbitrary 256 | V2 (XC6VLX200)-0 | 3109 Slices | 44.42 | |
| [121], (2010) | Arbitrary 256 | SIH (EP4S80I-4F1443) | 9177 ALMs + 96 DSPs | 157.2 | 680 |
| [123], (2005) | Arbitrary 256 | V2 (XC4VFX100) | 3729 LUTs + 1134 FFs + 2 BRAMs | 50 | 6000 |
| [125], (2006) | Arbitrary 256 | V2 (XC2VFX100) | 15755 Slices + 256 18*18-bit MULs | 40 | 3860 |
| [123], (2010) | Arbitrary 256 | V2 pro | 1832 Slices + 2 DSPs + 9 BRAMs | 108.2 | 29830 |
| [125], (2009) | Arbitrary 256 | V5 (XC5VLX110) | 2025 Slices | 100 | 9700 |
| [123], (2014) | NIST P-192, P-224, P-256, P-384 and P-521 | V6 (XC6VLX760) | 32.9K LUTs + 289 DSPs + 128 BRAMs | 100 | 360 to 3910 |
| [125], (2004) | Arbitrary 256 | V2 pro | 15755 Slices + 256 DSPs | 39.3 | 3840 |
| [125], (2006) | Arbitrary 256 | Zynq-7020 | 15755 Slices + 20 DSPs + 2 BRAMs | 39.46 | 3860 |
| [125], (2010) | Arbitrary 256 | V4 (XC5VLX30) | 20809 Slices | 200 | 1680 |
| [123], (2014) | NIST P-192, P-224, P-256, P-384 and P-521 | V5 (XC5VLX110) | 1980 Slices + 7 DSPs | 251.3 | 1709 to 2040 |
| [123], (2014) | NIST P-192, P-224, P-256, P-384 and P-521 | V4 (XC4VFX100) | 7020 Slices + 8 DSPs | 182 | 2361 to 3870 |
| [125], (2016) | Arbitrary 192, 224, 256, 384 and 521 | V7 (XC7U440) | 6816 LUTs + 20 DSPs | 225 | 690 to 9700 |
| [125], (2015) | Arbitrary 192 | V5 (XC5VLX330) | 615 Slices | 191.42 | 675 |
| [125], (2013) | Arbitrary 256 | V5 | 1725 Slices + 37 DSPs + 10 BRAMs | 291 | 380 |
| [125], (2010) | NIST P-192, P-224, P-256, P-384 and P-521 | V4 (XC4VFX100) | 20793 Slices + 32 DSPs | 43 | 6100 |
| [125], (2012) | Arbitrary 256 | V5 (XC5VLX110) | 41.6K Slices | 94.7 | 2600 |
| [125], (2009) | Arbitrary 256 | V4 (XC4VLX200) | 13661 Slices | 43 | 9200 |

Table 5: Results of the FPGA implementations of the elliptic curve point multiplication on special NIST prime field and works on special curve.

| Works(Year) | Prime Field | Device | Area | $F_{max}$(MHz) | Time($\mu$s) |
|-------------|-------------|--------|------|---------------|--------------|
| [121], (2015) | NIST P-384 | V4 (XC4VLX40) | 11883 Slices + 26 DSPs | 276 | 1030 |
| [121], (2015) | NIST P-256 | V4 (XC4VLX40) | 30589 LUTs | 139 | 2600 |
| [121], (2015) | NIST P-256 | V3 (XC5VLX110) | 34812 LUTs | 160 | 2250 |
| [121], (2015) | NIST P-192 | V5 (XC5VLX110) | 2657 Slices | 48.147 | 11.05 |
| [121], (2015) | FourQ, Mont 256 | Zynq-7020 | 565 LSs + 16 DSPs + 7 BRAMs | 175 | 310 |
| [121], (2016) | FourQ, End 256 | Zynq-7020 | 1691 LSs + 27DSPs + 10 BRAMs | 175 | 157 |
| [121], (2001) | NIST P-384 | VE1 (XC5VLX100) | 11416 LUTs + 7333 FFs + 35 BRAMs | 40 | |
| [121], (2007) | 160 | V2 pro | 1806 Slices + 3 BRAMs | 103 | 12716 |
| [121], (2011) | NIST P-256 | V2 pro | 1158 Slices + 3 BRAMs | 210 | 4520 |
| [121], (2008) | NIST P-256 | V4 (XC4VFX12) | 1715 Slices + 32DSPs + 11 BRAMs | 490 | 450 |
| [121], (2011) | NIST P-256 | V2 pro | 773 Slices + 1 DSPs + 9 BRAMs | 210 | 10020 |
| [121], (2010) | NIST P-256 | V2 pro | 81 Slices + 6 DSPs + 22 BRAMs | 171.5 | 11100 |
| [121], (2016) | NIST P-256 | Spartan-6 | 73 Slices + 8 DSPs + 24 BRAMs | 156.25 | 12200 |
| [121], (2015) | Curve25519 | Zynq-7020 | 1029 LSs + 20DSPs + 2 BRAMs | 100 | 397 |
| [121], (2008) | NIST P-256 | V2 Pro (XC4VFX30) | 2107 Slices + 1618*18-bit MULs + 6 BRAMs | 93 | 9900 |
| [121], (2017) | NIST P-256 | V5 (XC5VLX330) | 12300 Slices | 75.43 | 5260 |

The works [117], [124], [134] and [139] focused on low-cost and compact implementations and other works [122], [123], [126], [131], [138], [141], [143], [146], [149] and [154] [155] on high-speed implementations. Hardware resources in [117] are 350 Slices with 2 MULTs and 2 BRAMs, for arbitrary prime field with 256-bit, which are the lowest in the comparison with other implementations. Therefore, [117] achieves a good trade-off in the consumed slices and hardcores. The work [142] for NIST P-256 only occupies 72 Slices, but the consumed 8
DSP blocks and 24 BRAMs on Spartan-6 FPGA. The work [128] is the fastest FPGA-based implementation to date. It runs at 291 MHz on a Virtex-2 Pro FPGA and takes 380 $\mu$s per point multiplication. The designs [126], [144] and [145] are implemented on same FPGA Zynq-7020. The structure presented in [126] has the lowest hardware consumption compared to [144] and [145]. The best computation time for performing of one point multiplication is 157 $\mu$s for FourQ, End 256 structure in [126]. Also FourQ, End 256 structure in [126] is 2.54 times faster in computation time than that of [144]. The number of DSP blocks in [126] is 27 and for [144] is 20. Therefore, work [126] has about 1.88 times better speed-area ratio than [144]. The implementations [141], [147], [148] and [151] are scalable FPGA-Based architectures and support five prime fields P-192, P-224, P-256, P-384 and P-521. The best computation time for performing of one point multiplication is 157 $\mu$s for FourQ, End 256 structure in [126]. Also FourQ, End 256 structure in [126] is 2.54 times faster in computation time than that of [144]. The number of DSP blocks in [126] is 27 and for [144] is 20. Therefore, work [126] has about 1.88 times better speed-area ratio than [144]. The implementations [141], [147], [148] and [151] are scalable FPGA-Based architectures and support five prime fields P-192, P-224, P-256, P-384 and P-521. The proposed ECC processor implemented on Virtex-7 in [151] computes the point multiplication with size 192, 224, 256, 384 and 521 in 690 $\mu$s, 1080 $\mu$s, 1490 $\mu$s, 4080 $\mu$s and 9700 $\mu$s respectively. The FPGA implementation of this work consumed 6818 LUTs and 20 DSP48E slices. It runs at a maximum clock frequency of 225 MHz. It also supports arbitrary curves in short Weierstrass form up to 1024-bit without the need to reconfigure the hardware. In this category of the implementations work [141] has the best timing performance but hardware consumption in this work is 32.9K LUTs, 289 DSPs and 128 BRAMs.

6.1.3 FPGA implementations of the point multiplication on dual-field

General purpose ECC crypto-processors are implemented for both fields $\mathbb{F}_p$ and $\mathbb{F}_m$. These hardware implementations work in $\mathbb{F}_m$ as well as $\mathbb{F}_p$ which are categorized in dual-field implementations. They are usually slower than the two previous ECC hardware implementations. Important and desired factor in this group are flexibility and compatibility for support different standards, curve parameters, algorithms and security applications.

In [156] an efficient and flexible hardware implementation of dual-field ECC processor using the hardware-software approach is presented. The structure can support arbitrary elliptic curve based on Modular arithmetic logic unit (MALU). It can compute basic field operations and achieve high efficiency. The processor can be programmed by instruction set to compute different point operations and algorithms. The presented ECC processor in [156] is shown in Fig.26. It is consists of a control unit, MALU, ROM memory, register file and AMBA-AHB interface. By initializing memory with curve parameters and instruction codes, the processor can flexibly perform arbitrary elliptic curve operations over dual-field and different point multiplication algorithms.

![Figure 26: Architecture of the dual-field ECC processor in [156].](image)

To achieve the flexibility and applicability for different elliptic curves in dual-field, in [156], authors have integrated the multiple field operations into an MALU. In this circuit, adders are based on carry propagation adder and carry save adder. Modified Radix-4 Interleaved multiplication is used for field multiplier. Also, the plus-minus
version of the Radix-4 binary GCD algorithm is used for field inversion and division operations.

In [157] to speed up point multiplication a processor based on parallel processing technique is presented. The processor consists of a controller that checks instruction-level parallelism (ILP) and multiple sets of modular arithmetic units accelerating field operations. The FPGA results of two dual-field works [156] and [157] are shown in Table 6.

| Works (Year) | Field size \( \mathbb{F}_p/\mathbb{F}_{2^m} \) | Device | Area | \( f_{max} \) (MHz) | Time(\( \mu s \)) |
|--------------|---------------------------------|-------|------|-----------------|--------------|
| [156], (2016) | 256/256 | V2 | 12425 LUTs | 55.7 | 8250 |
| [156], (2016) | 256/256 | V4 | 24003 LUTs | 36.5 | 12600 |
| [157], (2006) | 160/163 | V2 pro | 8954 Slices+6 BRAMs | 100 | 1040/840 |

6.2 ASIC Hardware Implementations of the Elliptic Curve Cryptosystems

In this section, we present a review of different ASIC hardware implementations for the ECC processor. In general, three different types of the ASIC implementations in elliptic curve cryptosystems are over binary fields, prime fields and dual-fields. Many of the works in the ASIC implementations have been focused on the applications which have limited hardware resources with low-power such as smart cards, Wireless Sensor Networks (WSN) and Radio Frequency Identification (RFID) tags. Therefore, in recent years much of the efforts have been confined to designing the lightweight ECC processors. The ASIC hardware implementations of the ECC are reported in [57], [92], [93], [154], [155], [156], [158]-[160], [162], [164]-[167], [169]-[170], [172], [174], [176], [178]-[180], [183]-[187], [191], [193], [195]-[196], [201]-[206], and [209]. In this category, are only synthesized by the Synopsis Design Compiler (Design Vision tool) with CMOS technology. These works are not implemented in layout level. The works [57], [163], [166], [168], [171], [173], [175], [177], [181], [183]-[187], [191], [194] and [206]-[207] are implemented in layout level. In following subsections we present three different types of the ASIC implementations in elliptic curve cryptosystems in more details.

6.2.1 ASIC implementations of the ECC on binary fields

The works [57], [92], [93], [158], [161], [154], [163]-[167], [169]-[170], [172], [174], [176], [177]-[180], [181], [183]-[187], [191], [194] and [206]-[207] are ASIC implementation of the ECC on binary fields \( \mathbb{F}_{2^m} \).

The main special techniques for FPGA implementations of the point multiplication on prime fields are summarized as follows:

1. In [57] by using the **logical effort technique** the delay is optimally decreased and the drive ability of the structure in the point multiplication is increased.

2. In [161] the ECC processor is designed based on **programmable cellular automata**.

3. In [183] an **optimized RAM-macro block** is used and the design allows reduces the complexity by sharing different resources of the controller and the data-path.

4. In [186] a **new technique to compute point additions in affine coordinates** on Koblitz curves is proposed. This technique is based on applying a efficient inversion algorithm, which is implemented by fewer registers than the traditional schemes.

In [57] an efficient ASIC implementation of point multiplication on binary Edwards curves with GNB representation. The implementation is a low-cost structure constructed by one digit-serial field multiplier. The field multiplier is busy during PA and PD computations. In this work, by using the logical effort technique the delay is optimally decreased and the drive ability of the structure in the point multiplication is increased.
In [93] a ECC processor over $\mathbb{F}_{2^{163}}$ for the cryptographic applications that require high-performance is proposed. It has three 5-stage pipelined field RISC cores and a control unit to achieve instruction-level parallelism for the point multiplication. To decrease the latency customized instructions are proposed. The internal connections among three finite field cores and the main controller is obtained based on the analysis of both data dependency and critical path. The structure is illustrated in Fig.27. This structure is called pseudo-multi-core because this implementation achieves parallelism in instruction-level, not process level.

![Figure 27: Structure of pseudo-multi-core ECC processor in [93].](image)

The instruction set, $AB, A + B, (A + B)^2$ and $A^4$, for the parallelized Lopez-Dahab algorithm, in each core is obtained by analyzing the algorithm level and the hardware level.

In [158] a highly area optimized ECC processor for binary field is designed. The fast squarer circuit is used to construct an addition chain for efficient hardware implementation of the inversion. Therefore, an ASIC implementation of the processor using a modified Montgomery ladder point multiplication based on affine coordinate is presented. The design is for binary elliptic curves ranging from 113 to 193 bits. Area consumed is between 10k and 18k gates on a 0.35$\mu$m CMOS process for the different curves. Fig.28 shows ECC processor presented in [158]. The three units: field addition (ADD), field multiplication (MUL) and field squaring (SQR) are connected inside a single arithmetic unit sharing the common input data-bus $A$. The output results of the three previous units are selected at the output data-bus $C$ by the control signal $C_{sel}$ and one 3 to 1 multiplexer. The field adder needs an additional data-bus $B$ for the second input operand and the field multiplier requires a serial bit $b_i$ for the multiplicand. The operands are stored in the registers with the output being selected for $A$, $B$ and $b_i$ using multiplexers with control signals $A_{sel}$, $B_{sel}$ and $b_{i,sel}$. All registers are connected in parallel to the data-bus $C$ based on load signal $C_{ld_reg}$. 
An architecture of an elliptic curve processor for RFID tags over $\mathbb{F}_{2^{163}}$ is proposed in [165]. The processor is able to perform the point multiplications as well as general field operation such as additions and multiplications which are required for the different cryptographic protocols. By applying several techniques, the number of registers in register file are reduced from 9 to 6. A redundant field operation is introduced to obtain an efficient field arithmetic. Furthermore, the structure can support several cryptographic protocols. Elliptic curve PA and PD circuit (EC Add/Doubler) consists of control unit-1 (Control1), the modular arithmetic logic unit (MALU) and a register file. Control unit-1 receives the curve parameters and gives the result of the point multiplication via control unit-2 (Control2). Also control unit-2 reads in bytes a scalar (key) via the bus manager and controls the elliptic curve Add/Doubler based on the Montgomery ladder algorithm.

In [184] a lightweight coprocessor based on 283-bit Koblitz curve that implements high security ECC is presented. For the fast point multiplication the scalars are given as specific $\tau$-adic expansions. This work is the first lightweight different of the conversion algorithm from integers to $\tau$-adic. Therefore, the first lightweight implementation of Koblitz curves that includes the scalar conversion is introduced in [184]. Also the structure is the first lightweight ASIC multiplication for Koblitz curves that includes a set of countermeasures against simple power analysis, differential power analysis, timing attacks and safe error fault attacks. The processor consists of an ALU, an address generation unit, a shared memory and a control unit based on FSM. The ALU is connected with the memory block using an input register pair and an 2 to 1 multiplexer at output. The central part of the ALU consists of a 16 bits integer adder/subtractor circuit, a 16 bits binary field multiplier and two binary field adders. The some constant parameters are stored in a small ROM called Reduction-ROM which are used during modular reductions and multiplications.

In [186] an efficient implementation of the point multiplication on Koblitz curves for extremely-constrained applications in term of area is proposed. The field multiplication is designed by an efficient bit-serial multiplier with GNB representation. The addition and accumulation of this GNB multiplier is shared with other field additions.

A processor for ECC over $\mathbb{F}_{2^{163}}$ in [192] is presented. It is flexible enough to support several cryptographic protocols. The chip for hardware realization processor is fabricated using UMC 130nm 1P8M process, resulting in a core area of 0.54 mm$^2$. The energy consumption to perform one point multiplication is 5.1µJ.

In Table 7 we present the timing characteristics, area and power consumption of the previous ASIC hardware implementations of the ECC on $\mathbb{F}_{2^m}$. The works [93], [158], [161], [163], [167], [169], [170], [172], [174], [177]-[181], [183]-[184], [194], [205] and [208] are implemented based on binary Weierstrass curves. The fastest design in this category is presented work [93] with execution time for one point multiplication equal 5.4µs in 180nm CMOS technology. Hardware resources in this work is equivalent 217.9K gates. The fully programmable processor
In [206] can handle various curve parameters and an arbitrary irreducible polynomial. In addition, a wide range of the field size can be supported by changing the program and reconfiguring the data-path in the MALU cores. The type of the elliptic curve in the works [184], [186], [191] and [192] is Koblitz curves. For Koblitz curves the proposed structure in [184] has minimum area consumption compared to other works, it is equal to 4323 gates and also work [191] has minimum computation time with hardware resources equal to 108K gates. The work [186] is aimed at the low-area constrained application, such as RFID. So it consumed 11571 logic gates with power consumption 0.66 µW at 106 KHz. Fig 29 shows the number of gates for works which are implemented over $F_{2^{163}}$.

Table 7: Results of the timing characteristics, area and power consumption of the previous ASIC implementations of the ECC on $F_{2^{m}}$

| Works/Year | Field size | Technology | Area | $F_{\text{max}}$(MHz) | Time(µs) | Power consumption (µW) |
|------------|------------|------------|------|----------------------|---------|------------------------|
| 158, BWCs, PB, (2013) | 163 | 350nm AMI | 16.206K gates | 13.56 | 27900 | — |
| 164, BWCs, PB, (2011) | 256 | 120nm | 1.29 m²m $^2$ | 312 | 830 | 23100 |
| 164, BWCs, PB, (2007) | 163 | 180nm TSMC | 30K gates+1K RAM | 125 | 62 | — |
| 164, BWCs, PB, (2007) | 163 | 180nm | 13.182K gates | — | — | — |
| 166, BWCs, PB, (2004) | 191 | 130nm | 0.16 m²m $^2$ | 10 | 34143 | — |
| 167, BWCs, PB, (2003) | 178 | 500nm | 112K gates | 20.83 | — | 150000 @ 20MHz |
| 169, BWCs, PB, (2009) | 163 | 180nm TSMC | 1.92m²m$^2$, 69K gates | 181 | 1200 | 136000 |
| 170, BWCs, PB, (2005) | 191 | 350nm | 68K gates | 125 | 590 | — |
| 172, BWCs, PB, (2009) | 163 | 130nm IBM | 9.613K gates | — | — | — |
| 174, BWCs, PB, (2010) | 163 | 130nm | 267.7K gates | 199 | 111 | — |
| 173, BWCs, PB, (2010) | 163 | 180nm TSMC | 217.9K gates | 263 | 5.4 | — |
| 176, BWCs, PB, (2007) | 283 | 250nm | 1.91m²m $^2$ | — | 175 | 50.6 |
| 178, BWCs, PB, (2003) | 251 | 350nm | 2.75m²m $^2$ | 100 | 5500 | 13600 |
| 179, BWCs, PB, (2002) | 192 | 350nm | 16.847K gates | 10 | 126 | — |
| 180, BWCs, PB, (2009) | 163 | 180nm TSMC | 13.25K gates | 46 | 2792000 | 8.57 @ 106KHz |
| 181, BWCs, PB, (2006) | 131 | 130nm | 6.718K gates | — | 115000 | 30 @ 500KHz |
| 183, BWCs, PB, (2011) | 163 | 130nm UMC | 8.958K gates | — | — | 32.34 @ 1MHz |
| 184, BWCs, PB, (2015) | 163 | 130nm UMC | 5.773K gates | — | 30310 | 6.11 @ 1MHz |
| 184, BCKs, PB, (2015) | 163 | 130nm UMC | 4.332K gates | — | 26300 | 6.11 @ 1MHz |
| 184, BCKs, GNB, (2014) | 163 | 65nm | 11.521K gates | — | 1006600 | 0.66 @ 106KHz |
| 184, BCKs, PB, (2010) | 163 | 130nm | 11.72K gates | — | 547870 | 7.27 @ 400KHz |
| 185, BCKs, PB, (2007) | 165 | 130nm | 108K gates | 555.6 | 27 | — |
| 185, BCKs, PB, (2016) | 163 | 180nm TSMC | 73.81pm² | 535.6 | 102000 | 50.4 @ 847.5KHz |
| 189, BCKs, PB, (2015) | 163 | 65nm TSMC | 10.945K gates | — | — | — |
| 191, BWCs, PB, (2014) | 160 | 130nm | 12.348K gates | — | — | 42.42 @ 1MHz |
| 200, CONFIG-I, BWCs, PB, (2007) | 163, 193, 283 and 571 | 130nm | 393K gates | 292 | 54 to 1349 | — |
| 206, CONFIG-II, BWCs, PB, (2007) | 163, 193, 283 and 571 | 130nm | 244K gates | 292 | 54 to 1349 | — |
| 207, BCKs, GNB, (2017) | 223 | 180nm | 29.324K gates+10*233 Regs | 1070.66 | 118.6 | — |
6.2.2 ASIC implementations of the ECC on prime fields

The works [154], [155], [159], [160], [162], [168], [182], [195], [196], [205] and [209] are ASIC implementations of the ECC on prime fields. In [154] two different parallelization techniques to accelerate the point multiplication over $\mathbb{F}_p$ in affine coordinates are presented. The proposed implementations are resist against different side channel attacks based on power and time analysis. The both architectures are synthesized for 160, 192, 224 and 256 bits on FPGA and also ASIC implementation in 130nm CMOS technology is performed. In [155] to achieve a high-speed and low-area hardware structure of elliptic curve point multiplication over a prime field, a combined PA and PD architecture is presented by using efficient modular arithmetic in Jacobian coordinates. In [162] a high-performance ECC processor for general prime curves is presented. By using a unified systolic array the field addition, field subtraction, field multiplication and field division are efficiently implemented. The structure is pipelined and pipeline stall problems are successfully solved by using two optimization methods. The processor, is synthesized in 130nm standard cell technology, it takes 1.01ms to compute a 256 bits point multiplication for general curves. The proposed ASIC implementation in [168] is includes a 3-stage pipelined full-word modular Montgomery multiplier which needs a few clock cycles. The precomputation steps of field multiplication based on Montgomery method are implemented by hardware. The ECC field arithmetic unit has programmable data-path, so, arbitrary field lengths are supported for implementation.

A high-performance implementation of ECC over SCA-256 prime field by considering an all-new isochronous architecture is proposed in [195]. It is resist against simple power analysis and double attack with minimum time cost. Also random cycles are inserted in the structure to differential power analysis. By modifying Montgomery ladder point multiplication algorithm the PA and PD can operate synchronously. The processor achieves 211$\mu$s and 8.5$\mu$J for one point multiplication with 208k gates using CMOS standard cell library of 130nm.

The timing characteristics, area and power consumption of the previous ASIC hardware implementations of the ECC on $\mathbb{F}_p$ are illustrated in Table 8. Compared to other related designs, the work [196] outperforms other implementations in terms of execution time and area/time product. Hardware consumed in [182] is equal to 30.3K gates in 130nm CMOS technology which is the lowest compared to other designs.
Table 8: Results of the timing characteristics, area and power consumption of the previous ASIC Implementations of the ECC on $\mathbb{F}_p$.

| Works            | Field size | Technology | Area       | $F_{\text{max}}$(MHz) | Time (µs) | Power consumption (µW) |
|------------------|------------|------------|------------|------------------------|-----------|------------------------|
| [160], (2010)    | 256        | 180nm      | 132K gates | 671                    | 850       | —                      |
| [162], (2007)    | 256        | 130nm      | 122K gates | 556                    | 1010      | —                      |
| [168], (2012)    | 256        | 90nm       | 540K gates, 2.72mm$^2$ | 185        | 120       | —                      |
| [156], Design 1, (2009) | 256        | 130nm      | 106.7K gates | 137.7     | 2680      | —                      |
| [156], Design 2, (2009) | 256        | 130nm      | 102.2K gates | 110        | 3610      | —                      |
| [162], (2004)    | 167        | 130nm      | 30.3K gates | —          | 34143     | 990 @ 20MHz            |
| [165], (2015)    | 256        | 130nm      | 208K gates | 215        | 251       | —                      |
| [196], (2016)    | 256        | 90nm       | 447K gates, 0.93mm$^2$ | 546.5      | 730       | —                      |

6.2.3 ASIC implementations of the ECC on dual-fields

Flexibility and scalability for ASIC implementation of elliptic curve applications is important and interesting subject in literature. The works [156], [173], [175], [188]-[190] and [197]-[204] are ASIC implementations of the ECC over both prime fields $\mathbb{F}_p$ and binary fields $\mathbb{F}_{2^m}$ to support a wide range of elliptic curves and applications. In [173] a unified division algorithm and a free precomputation structure are proposed to speedup the $\mathbb{F}_p/\mathbb{F}_{2^n}$ elliptic curve arithmetic operations. The structure is optimized by a very compact field arithmetic unit with the fully pipelined technique. Also, a key-blinded technique with regular computation is implemented against the power analysis attacks without time cost. After fabricated in 90nm CMOS 1P9M process, area of ECC processor is 0.55mm$^2$. It can perform the point multiplication in 19.2ms over $\mathbb{F}_{p251}$ and 8.2ms over $\mathbb{F}_{2^{409}}$, respectively. Fig.30 shows the ECC architecture with a standard AMBA AHB bus interface. The inputs are consist of user public/private-key, elliptic curve coordinates, elliptic curve parameters and protocol instructions. The instruction decoder and pre-/post-process are combined in the processor. After the instruction decoding, the pre-process stage is to convert the coordinates and parameters into the Montgomery domain and blind the key value to avoid power analysis attacks. All dual-field modular and Montgomery operations are integrated into the pipelined Galois field arithmetic unit with circuit sharing.

Figure 30: Architecture of the dual-field ECC processor in [173].

In [173] presents a parallel, scalable and high-throughput dual-field ECC architecture. This processor has features all ECC functions with the programmable field and curve parameters over both the prime and binary fields. Using 130nm CMOS technology, the core size of the processor is 1.44mm$^2$. The results show that the
ECC processor can perform one 160-bit point multiplication with coordinate conversion over \( \mathbb{F}_p \) in 608\( \mu \text{s} \) at 121MHz with only 70mW and the field \( \mathbb{F}_{2^m} \) in 372\( \mu \text{s} \) at 146MHz with 82.1mW. The ECC instructions and data are fed into the input buffer through the AMBA AHB interface. The main controller decodes the instructions that support comprehensive cryptographic functions, including the coordinate conversion, PA, PD, point multiplication, Montgomery pre-/post-processing, modular exponentiation and common field operations. The ECC processor has been fabricated using TSMC 130nm 1.2-V 1P8M CMOS technology. The size of the ECC processor chip is 5.1mm\(^2\), where the core size is only 1.44mm\(^2\) (1.2 \times 1.2 mm). Table 9 summarizes the previously published results of the ASIC implementations of the dual-field ECC.

Table 9: Results of the previously published ASIC implementations of the dual-field ECC.

| Work(Year) | Field size \( \mathbb{F}_p/\mathbb{F}_{2^m} \) | Technology | Area | \( F_{\text{max}} \) (MHz) | \( \text{Time(\mu s)} \) \( \mathbb{F}_p/\mathbb{F}_{2^m} \) | Power consumption \( (\mu W) \) \( \mathbb{F}_p/\mathbb{F}_{2^m} \) |
|------------|---------------------------------|------------|------|-------------------|-------------------|---------------------|
| [171], (2010) | 256/256 130nm TSMC | 184K gates, 1.30mm\(^2\) | 75/114 | 368/252 | 68400/58200 |
| [172], (2010) | 256/256 90nm | 119K gates, 0.55mm\(^2\) | 147/188 | 4400/1150 | 67600/72500 |
| [173], (2009) | 160/160 130nm TSMC | 169K gates, 1.44mm\(^2\) | 121/146 | 608/372 | 70000/82000 |
| [181], (2008) | 160/160 130nm | 150.1K gates, 1.04mm\(^2\) | 217/350 | 340/155 | --/-- |
| [189], (2010) | 163/163 130nm | 331.7K gates, 2.34mm\(^2\) | 415/415 | 440/440 | --/-- |
| [190], (2011) | 160/160 130nm | 179K gates, 1.35mm\(^2\) | 141.3/158.1 | 385/272 | 32300/46200 |
| [177], (2012) | 163/256 65nm | 179K gates, 1.10mm\(^2\) | 500/500 | 320/80 | 120000/25000 |
| [188], (2008) | 160/160 180nm | 17.81mm\(^2\) | 233/233 | --/-- | 10000 @ 1MHz |
| [199], (2011) | 256/256 90nm | 122K gates, 0.45mm\(^2\) | 250/250 | 770/590 | 31000/35600 |
| [189], (2014) | 160/160 90nm UMC | 90K gates, 0.41mm\(^2\) | 256/256 | 250/250 | --/-- |
| [156], (2016) | 256/256 55nm | 189K gates, 0.35mm\(^2\) | 316/316 | 1450/450 | --/-- |
| [204], (2003) | 192/160 130nm | 17.5K gates | 137.9/102.2 | 144/990 | --/-- |
| [202], (2003) | 160/160 90nm | 61.3K gates, 0.21mm\(^2\) | 277/277 | 710/610 | --/-- |
| [203], (2012) | 160/160 90nm | 83.2K gates, 0.29mm\(^2\) | 250/250 | 800/4850 | --/-- |
| [203], (2012) | 521/699 90nm | 168K gates, 0.38mm\(^2\) | 250/250 | 800/4850 | --/-- |
| [203], (2012) | 521/699 90nm | 265K gates, 0.93mm\(^2\) | 232/232 | 4570/2770 | --/-- |

The present work in [200] needs a preprocessing to convert the operands into the Montgomery domain. But in recent work [156] no domain conversion is needed, it is implemented in the ordinary prime/binary finite fields. Overall, ECC processor in [156] achieves high efficiency and flexibility due to the elaborate MALU structure and soft-hardware approach respectively. It can be used for different ECC standards, different elliptic curves and different point multiplication algorithms. In [175] for design-for-testability (DFT), six scan chains were inserted with a fault coverage of 99.77%. The best work in term of computation time is [197] for 163-bit binary field and 256-bit for prime field.

### 7 Conclusion

In this paper, a comprehensive study of hardware implementations of elliptic curve cryptography is presented. For fair comparison and better analysis, the implementations are categorized and presented based on used finite field, type of elliptic curves, representation basis and implementation platforms. In the survey, different elliptic curves, point multiplication algorithms and finite field arithmetics and also their effect on implementations are defined and discussed. The implementations are compared in terms of hardware consumption which is important for any cost-sensitive application and execution time which is important for many applications especially in high-speed application. The study shows that FPGAs are suitable for reconfigurable applications and ASIC implementations are suitable for Lightweight implementations of the ECC which is one of the attractive fields in ECC implementation. The most previous works have similar selection in the implementation, i.e., in selecting type of finite field, elliptic curve, point multiplication algorithm and algorithm of field operations. For example, the Montgomery ladder and the Itoh-Tsujii algorithm are widely used for point multiplication and field inversion respectively. Several proposed solutions and important issues that can be helpful in hardware implementation of the ECC are as follows:

- The number of researches concerning the implementation of ECC in low-cost microcontroller-based de-
sives is increasing. It is important and feasible to implement cryptographic applications in constrained environments and be able to achieve acceptable performance. Therefore, implementation of the ECC on microcontrollers and microprocessors is attractive subject.

- Binary Edwards curves (BECs) are complete and without exception points, the point addition law which makes them attractive for implementation and intrinsically resistant to Simple power analysis. The design and implementation of the hardware structures for the point multiplication on binary Edwards curves can be a popular research topic and more work could be done to take the best advantage of these curves.

- The logical effort technique is a procedure for achieving the least delay for a given load in a logic circuit. In the design of the field multiplier in the ECC structure, to balance the delay among the stages and to obtain a minimum over all delay, the logical effort technique can be applied. This technique is suitable for high-speed hardware implementation of the ECC. We can design an algorithmic and automatics approach based on logical effort for compute size of transistors in the critical path delay for different loads. Also, in this case the best trade-offs between area and speed can be achieved.

- Lightweight hardware implementation of the ECC for FPGAs and ASIC design has been a popular research topic due to the development low-cost hardware embedded applications.

- The field addition and multiplication operations in $F_{3^m}$ are comparable in performance to a space equivalent characteristic two alternative. So, implementation of the ECC on $F_{3^m}$ can be an important issue in future.

- To design ECC processor based on large field multipliers for high-level security application in a significant speedup, the Fine-Grain pipelining and retiming technique (minimize the clock period and the number of registers in the circuit) should be applied.

- For flexible and scalable ECC processors, more work could be done to take the best advantage of full size hardware for different applications and concurrent multi-point multiplication algorithms.

- For high-speed and low-area ECC processors, more work could be done to take the best advantage of different scheduling algorithms, for example, List scheduling, Force directed and Iterative refinement. The aim of the high-speed implementation is reduce the number of field operation especially field multiplier. Therefore, the new scheduling methods can be useful for computation of the point addition and point doubling, in differential addition coordinate, in binary Edwards and generalized Hessian curves.

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