Integrated CMOS edge voltage quantizer for detection of low-frequency simple waveforms

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Abstract: A novel edge voltage (EV) quantizer with digital-intensive implementation is proposed to detect DC voltage, peak-to-peak magnitude, and frequency of low-frequency simple waveforms (e.g. sinusoidal). The proposed EV quantizer does not need the area-consuming low pass filter. It can be implemented using digital-intensive circuits with little computing complexity, thanks to the simple detection algorithm. A successive approximation register (SAR) version of the EV quantizer was integrated in a monolithic satellite low noise block (LNB) IC in a 65 nm CMOS process to detect low-frequency control signals. And the measurement results validate that the EV quantizer enables low-cost operation for detection of low-frequency simple waveforms.

Keywords: 22-KHz tone detection, low-noise block (LNB), polarization switch

Classification: Integrated circuits

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1 Introduction

Television broadcast under DVB-S regulations has been in use for many years. The block diagram of a satellite system for DVB-S is shown in Fig. 1. Satellites transmit both horizontal (H) and vertical (V) polarized RF signals in the Ku-band, which is divided into two parts, low band (LB: 10.7–11.7 GHz) and high band (HB: 11.7–12.75 GHz). The parabolic dish on roofs or outside windows is used to concentrate the weak satellite signals. And low noise block (LNB), which is set up at the focus of the dish, picks up and translates the signals to IF, ranging within the L-band (0.95–2.15 GHz). Then the L-band signals are transmitted through a coaxial cable to the integrated receiver decoder (IRD), which is more familiarly known as set-top box inside the room. IRD is in charge of the final signal processing before we can watch the TV programs on the TV set.

Actually, the coaxial cable is also used for transmission of power supply and low-frequency control signals from IRD to LNB. Fig. 2 shows the block diagram of LNB and IRD. In IRD, digital control bits $D_{\text{Voltage}}$ and $D_{\text{Tone}}$ are set according to the television viewer’s operations. Thus, the supply voltage for LNB is 13 or 18 V, with or without a 22-KHz tone [1]. The Voltage/Tone detector in LNB integrated

Fig. 1. Common receiver equipment for DVB-S.
circuit (IC) is in charge of detecting this compound low-frequency control signal. The detected $D_{\text{Voltage}}$ and $D_{\text{Tone}}$ are respectively used to control the bias of off-chip amplifiers and division ratio in PLL. Therefore, the signal of the wanted polarization (H/V) in the wanted band (LB/HB) is picked up and translated to L-band.

Fig. 2. Block diagram of LNB and IRD.

The nominal DC voltage of the power supply $V_{\text{DC}}$ is 13/18 V. And the nominal peak-to-peak magnitude $V_{\text{PP}}$ and frequency $f_{\text{IN}}$ of the tone is 0/650 mV and 22 KHz respectively. Due to the unavoidable variances of the circuit devices, the current driven from the supply from LNB and the leakage of the tone, the actual $V_{\text{DC}}$ is $13 \pm 2/18 \pm 2$ V. And the actual $V_{\text{PP}}$ is $0 \sim 0.1/0.22 \sim 1$ V. Even the frequency $f_{\text{IN}}$ is $22 \pm 2$ KHz. The detector in LNB has to be able to tolerate these signal variances to detect the correct $D_{\text{Voltage}}$ and $D_{\text{Tone}}$.

References [2, 3, 4, 5] list several products dedicated to the voltage/tone detection. Fig. 3 shows one of those traditional analog detection schemes. $V_{\text{DC}}$ can be extracted through a simple one-order RC low-pass filter. $D_{\text{Voltage}}$ can be detected by comparing the extracted $V_{\text{DC}}$ with a reference voltage. $V_{\text{PP}}$ can be extracted through a simple one-order RC high-pass filter and a peak detector. $D_{\text{Tone}}$ can be detected by comparing the extracted $V_{\text{PP}}$ with another reference voltage. For low-frequency applications, an obvious shortcoming of the analog detection
scheme is the large silicon area occupied by low-pass filters and/or AC coupling capacitors. Moreover, analog circuitry usually suffers from low supply voltages in more advanced CMOS technologies and is not as power-efficient as digital circuits and comparators (CMP) in low-frequency applications due to the huge difference in static power consumption.

Traditional electronics has to develop and update using new technology such as integrated circuits on silicon. In early years, LNB is constructed almost all by discrete components [6, 7]. With the rapid development of semiconductor, more and more parts can be integrated in the same die [8, 9, 10]. In recent years the circuits for voltage/tone detection have also been integrated in a monolithic LNB IC [11, 12] further cutting the cost. Moreover, only one pin is allocated to input the combined control signal for low package cost.

This paper presents an area/power-efficient digital-intensive detection scheme for low-frequency simple waveforms based on a novel edge voltage (EV) quantizer, which greatly reduces the circuit design complexity compared to the analog scheme. The rest of this paper is organized as follows. Section 2 discusses the idea of digital-intensive detector, including the proposed novel EV quantizer. Circuit implementation of the proposed EV quantizer based on successive approximation register (SAR) architecture is presented in Section 3. Section 4 summarizes the measurement results of the proposed digital-intensive detector using EV quantizer. Finally a brief conclusion is drawn in Section 5.

2 Digital-intensive detection scheme

As is shown in Fig. 4, a simple waveform $S_{IN}$ can be parted into three regions, i.e., high region (H), middle region (M), and low region (L). Two voltage levels, $V_{HE}$ and $V_{LE}$, separate these three regions, where $V_{HE}$ is the high side edge voltage and $V_{LE}$ is the low side edge voltage of the input waveform $S_{IN}$. In observing this, a novel edge voltage (EV) quantizer using “analog” comparators, along with simple digital signal processing, is proposed to extract $V_{DC}$, $f_{IN}$ and $V_{PP}$ from simple waveforms, completely avoiding traditional sampling and also reducing digital computing complexity without the need for FFT computing.

2.1 EV quantizer

Without loss of generality, we elaborate on EV quantizer by means of a flash version. Fig. 5 shows the block diagram of an N-bit flash EV quantizer and its corresponding coding table. As is expected in a typical flash quantizer, the flash EV quantizer also compares the input with a set of reference voltages simultaneously,
indicated by a joint name $V_{DAC}$ in Fig. 5. The comparison output $V_{CMP}$ is fed to a
digital square waveform indicator (DSWI), which output $V_{DSWI}$ indicates whether
$V_{CMP}$ is a square waveform with a certain frequency.

In a traditional quantizer, a discrete or sampled voltage value from input $S_{IN}$ is
used for comparison with a digitized output (either “1” or “0”) during one
conversion period. In contrast, the proposed EV quantizer compares input $S_{IN}$
continuously with reference voltages using “analog” comparators, i.e., all signals
(input, output, and reference) can be treated as continuous analog signals and the
comparator behaves more like a limiting amplifier. No sampling is required in the
EV quantizer. The comparison result is either continuous DC voltages or a
continuous square waveform, which is digitized in the digital square waveform
indicator (DSWI).

As can be seen from the coding table in Fig. 5, the quantization codes can be
easily obtained by combining the comparator output $V_{CMP}$ and DSWI output $V_{DSWI}$
with simple coding logic. The resulting quantization codes can be further divided
into three sections, depending on the values of $V_{CMP}$ and $V_{DSWI}$. Codes $D_{HE}$ and
$D_{LE}$, separating these three sections, correspond to the quantized results of those
two edge voltages $V_{HE}$ and $V_{LE}$ and the quantized code of $V_{PP}$ is obtained by:

$$V_{PP} = V_{HE} - V_{LE} \quad (1a)$$

$$Q(V_{PP}) = D_{HE} - D_{LE} \quad (1b)$$

where $Q(\cdot)$ stands for the operation of quantization. For an input waveform with a
$V_{PP}$ less than a quantization step, $D_{HE}$ and $D_{LE}$, or $V_{HE}$ and $V_{LE}$, are identical and
the input waveform would be detected as a DC signal with a voltage equal to $V_{HE}$
or $V_{LE}$.

### 2.2 Digital square waveform indicator (DSWI)

The digital square waveform indicator DSWI is actually a digital synchronous
sequential counter driven by a clock ($CLK_F$), whose frequency $f_{CLK_F}$ is much
higher than $f_{IN}$. Assume that $V_{PP}$ is larger than a quantization step, which is
required for EV quantizer to detect any non-DC signal. When the reference voltage lies between two edge voltages $V_{HE}$ and $V_{LE}$, “analog” comparator output $V_{CMP}$ becomes a continuous square waveform with the same frequency as $f_{IN}$.

Fig. 6 shows the timing diagram of DSWI. Two counters CNT1 and CNT2 begin to count from 0 when a rising edge of $V_{CMP}$ arrives. When a falling edge of $V_{CMP}$ arrives, CNT1 stops counting with the equivalent counted duration being $\tau$ ($\tau_{HE}$ for $D_{HE}$ and $\tau_{LE}$ for $D_{LE}$). When another rising edge of $V_{CMP}$ arrives, CNT2 restarts to count from 0 with the equivalent counted duration being $T$ (same for $D_{HE}$ and $D_{LE}$). $f_{IN}$ is estimated as:

$$f_{IN} = \frac{1}{T}. \quad (2)$$

Fig. 7 shows how to detect the rising and falling edges in the comparator’s output $V_{CMP}$ using digital synchronous sequential circuits. At every rising edge of $CLK_F$, the real-time value of $V_{CMP}$ is registered by register REG1 and the old value in REG1 is used to update another register REG2. In other words, REG1 and REG2 are detecting two closely-spaced values of $V_{CMP}$ in time domain. As a consequence, the event of “$\text{REG}_1 = 1$ & $\text{REG}_2 = 0$” represents that a rising edge of $V_{CMP}$ is detected. In a similar way, the arrival moment of the falling edge of $V_{CMP}$ can be detected and represented by the event of “$\text{REG}_1 = 0$ & $\text{REG}_2 = 1$”. The latency of
this edge detection scheme is about 1–2 periods of CLKF, which is the exact reason why the counters do not start/stop counting immediately upon the arrival of rising/falling edges, as shown in Fig. 6.

After confirming a continuous square waveforms at the comparator output VCMP by counting one or more periods defined by the rising and falling edges, DSWI updates VDSWI to “1”, otherwise VDSWI remains to be “0”. Value change from “1” to “0” in VDSWI, along with VCMP can be used to determine codes DHE and DLE, and thus the peak-to-peak magnitude VPP.

Fig. 8 shows the comparator’s input and output waveforms corresponding to codes DHE and DLE.

Fig. 8 shows the comparator’s input and output waveforms corresponding to codes DHE and DLE. It is obvious that DC voltage VDC of the input waveform SIN can be approximated by averaging the area of the shown trapezoid Atrap over the period T:

$$A_{\text{trapezoid}} = \frac{(T - \tau_{\text{HE}} + T - \tau_{\text{LE}}) \times (D_{\text{HE}} - D_{\text{LE}})}{2}$$

$$Q(V_{\text{DC}}) = \frac{A_{\text{trapezoid}}}{T} + D_{\text{LE}} = D_{\text{HE}} - \frac{\tau_{\text{HE}} + \tau_{\text{LE}}}{2T} \times (D_{\text{HE}} - D_{\text{LE}}).$$

For sinusoidal or square waveforms with a 50% duty cycle, equation (4) can be further simplified to:

$$Q(V_{\text{DC}}) \approx \frac{D_{\text{HE}} + D_{\text{LE}}}{2}.$$
DC voltage for LNB IC switches between two ranges of 1.2~1.63 V and 1.74~2.17 V. However, the input $V_{PP}$ is unchanged due to the 100-nF bypass capacitor.

![Block diagram of the SAR EV quantizer inside LNB IC.](image)

The SAR EV quantizer consists of a comparator CMP, a resistor array $R_X$, and digital circuits including a digital square waveform indicator DSWI, a SAR Logic, a DSP block, and a clock divider. A reference current $I_{DAC}$ flowing through $R_X$ generates the $V_{DAC}$. The clock divider divides the on-chip available 25-MHz reference clock signal to generate another two clock signals $CLK_F$ and $CLK_S$ for the DSWI and the SAR logic respectively. The SAR logic with binary search algorithm adjusts $D_{SAR}$ according to the 2-bit signals $V_{CMP}$ and $V_{DSWI}$. Within several binary searching iterations, code $D_{HE}$ or $D_{LE}$, along with their corresponding high side edge voltage $V_{HE}$ or low side edge voltage $V_{LE}$, can usually be obtained. Equations (1)–(5), which are implemented in the DSP block, can then be used to obtain the input waveform’s DC voltage ($V_{DC}$), peak-to-peak magnitude ($V_{PP}$), and frequency ($f_{IN}$). One can get the detected $D_{Voltage}$ and $D_{Tone}$ by comparing the digital $V_{DC}$ and $V_{PP}$ with preset threshold values in digital domain.

### 3.1 Circuits design

The proposed SAR EV quantizer was implemented in a 65 nm CMOS technology. The $V_{DAC}$ generation circuit shown in Fig. 9 is developed based on a bandgap reference circuit (BGR) [13]. The bandgap current source $I_{DAC}$ coming from bandgap core circuit is used to set the values of reference voltages for the comparator. A 6-bit setting is realized with reference voltages ranging from 1.05 V to 2.35 V with 1 LSB of roughly 20 mV. With a typical $I_{DAC} \approx 30 \mu A$, $R_X$ is chosen to be linearly programmable from 35 to 77.5 KΩ. The equivalent internal preset threshold values for $V_{DC}$ and $V_{PP}$ are designed as $V_{DC_{TH}} = 15.5 V$ and $V_{PP_{TH}} = 150 mV$, respectively. The comparator CMP is a static comparator to simplify the design as much as possible. Fig. 10 shows the schematic of the
comparator CMP. A 3.3 V supply voltage is used to accommodate the input DC voltage range and thus thick-oxide transistors in 65 nm CMOS are adopted to operate under high supply voltage. The input offset of the comparator is estimated below 10 mV by simulations.

![Schematic of the comparator (CMP).](image)

The detection accuracy is also affected by the frequency of CLKF. To avoid detection errors caused by CLKF, its frequency $f_{CLK_F}$ is set high enough, about 780 KHz. And the DSWI is designed to recognize the frequency range of about $22 \pm 10$ KHz. The SAR logic clock (CLKS) should have a frequency $f_{CLK_S}$ lower than $f_{IN}$ in order to give more time to DSWI for stable $V_{DSWI}$, which might need more than one-period counting. In this design, $f_{CLK_S}$ is set to about 6 KHz. Based on 6-KHz $f_{CLK_S}$ and 6-bit DAC setting, it takes about 2.4 ms ($1 \div 6000 \times 2 \times (6 + 1)$) to obtain the final detection results or track any changes of the control signals. This is fast enough for the detection in LNB. As to the specifications in Digital Satellite Equipment Control (DiSEqC) [14], a design with a flash version EV quantizer and a faster CLKS could achieve a detection time of shorter than 100 $\mu$s.

### 4 Measurement results

![Die photo.](image)

Fig. 11 shows the die photo of the SAR EV quantizer based low-frequency simple waveform detector, which was integrated in a low-cost LNB IC. It was fabricated in
a 65 nm CMOS process with a total active area of only 0.0084 mm². The total current consumption is from 120 to 250 µA, depending on the input signal DC voltage and $V_{PP}$ magnitude.

To demonstrate the detection of $V_{DC}$ and $V_{PP}$ in the situation that no extra pins are allocated for testing, the input sinusoidal waveform was adjusted continuously until the biasing state or the LO frequency in LNB changes. Statistical measurement results of 8 samples of the proposed EV quantizer are plotted in Fig. 12. The results prove that the proposed detector is able to distinguish whether the input $V_{DC} < 15 \text{ V}$ or $> 16 \text{ V}$, and whether the $V_{PP} < 0.1 \text{ V}$ or $> 0.22 \text{ V}$ with a better-than-enough accuracy for satellite television applications. If needed, the accuracy could be improved using a bandgap reference with less variations since reference voltages are the main source of the detection errors. Performance from previous work [2, 3, 11, 12] is summarized and compared with that of our work in Table I. No details about integrated voltage/tone detector are presented in [6, 7, 8, 9, 10] and the reason could be that the discrete voltage/tone detector is utilized as in many cases. To the best of the authors’ knowledge, this work presents the first low-cost integrated voltage/tone detector for LNB IC, with smallest silicon area, lowest current consumption, and best detection resolution.

![Graphs showing input $V_{DC}$ versus $V_{PP}$ and input $V_{PP}$ versus $V_{DC}$](image)

(a) Input $V_{DC}$ versus $V_{PP}$, when $V_{DC,TH} = 15.5 \text{ V}$. (b) Input $V_{PP}$ versus $V_{DC}$, when $V_{PP,TH} = 150 \text{ mV}$.

**Fig. 12.** Measurement results from 8 samples.

| Reference | [2] | [3] | [11] | [12] | This work |
|-----------|-----|-----|------|------|-----------|
| Integrated | No  | No  | Yes  | Yes  | Yes       |
| Number of allocated pins | 2   | 2   | 1    | 1    | 1         |
| Detection offset* | $V_{DC}$ (±V) | 0.75 | 0.5  | —    | 0.6       | 0.5      |
| Detection offset* | $V_{PP}$ (±mV) | 125  | 125  | 60   | 250       | 20       |
| Current (mA) | 8   | 5   | —    | —    | <0.25     |
| Active area (mm²) | —   | —   | CMOS | —    | 0.0084    |
| Technology | —   | —   | CMOS | 65 nm CMOS |

*The maximal deviation from the nominal threshold ($V_{DC,TH}$ and $V_{PP,TH}$).
5 Conclusions

This paper presents a novel digital-intensive edge voltage (EV) quantizer, which can be utilized to detect the DC voltage, peak-to-peak magnitude, and frequency of low-frequency simple waveforms (e.g., sinusoidal). Quantizer based detection scheme avoids using low pass filtering and thus saves silicon area. Moreover, the proposed EV quantizer can be implemented using almost all-digital circuits with little computing complexity, thanks to its simple algorithm for detection results. As a result, the proposed EV quantizer enables low-cost operation for detection of low-frequency simple waveforms.

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