Designing of RF Single Balanced Mixer with a 65 nm CMOS Technology Dedicated to Low Power Consumption Wireless Applications

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Abstract
The present work consists of designing a Single Balanced Mixer (SBM) with the 65 nm CMOS technology, this for a 1.9 GHz RF channel, dedicated to wireless applications. This paper shows; the polarization chosen for this structure, models of evaluating parameters of the mixer, then simulation of the circuit in 65nm CMOS technology and comparison with previously treated.

Keywords: SBM Mixer, Radio Frequency, 65 nm CMOS Technology, Non-Linearity, Power Consumption.

I. Introduction
With the multimedia’s advent, the aspect of embedded systems, of RF architecture of transmission / reception channel; require a reduction in size and energy consumption with equal performances. In this stage, advanced CMOS technologies are therefore a new way now increasingly studied for the design of RF functions, the transition frequency of CMOS transistors is inversely proportional to the length of the channel, and has, as such, steady progress of lithography.

In a radio-frequency wireless, especially in a superheterodyne architecture, the frequency mixer is an indispensable module which the impact is critical on the performance of all functions [1].

II. Modeling of evaluating mixer ‘Parameters

2.1 Architecture of the SBM Mixer

The architecture of the mixer design, shown in Fig.2, is of the type single balanced (SBM).

This structure requires that transistors CMOS M2 and M3 must be identical. The CMOS M1 receives the RF signal and acts as the voltage / current converter. The current trail Is is shared equally among the coupled sources M2 and M3. Thus, the $V_{RF}$ signal varies the drain-source current of M1, and the switching operation of M2 and M3 multiplies this variation by the $V_{LO}$ signal coming from a local oscillator. Finally, the output signal $V_{out}$ is represented by the voltage between the drains of CMOS M2 and M3 [2].

We have chosen sizing for CMOS 65 nm technology (M1, M2, M3, M4) [3].
**Fig. 2 Polarization Diagram of a SBM**

$V_{RF}$ and $V_{LO}$ frequencies are respectively 1.9 GHz and 1.8 GHz which provides an intermediate frequency of 100 MHz. The choice of these values gives an IF frequency as agreed to meet most of the wireless networks deployed today, and operating frequency around 1 GHz, such as GSM [4].

### 2.2 Conversion Gain

The chosen architecture is an architecture single balanced with the two CMOS M2 and M3 of the differential pair are on commutation mode (Fig. 2), so the output current is controlled by the state of the VCO signal generated by the local oscillator which allows write:

$$I_{out}(t) = I_s(t) \cdot \text{sign}[V_{LO}(t)]$$

(1)

With $\text{sign}[V_{LO}(t)]$ is the Fourier transform of the VCO signal:

$$\text{sign}[V_{LO}(t)] = \frac{4}{\pi} \left\{ \cos(\omega_{LO}t) - \frac{1}{3} \cos(3\omega_{LO}t) + \frac{1}{5} \cos(5\omega_{LO}t) + \ldots \right\}$$

(2)

According to the circuit and the internal structure of CMOS M1 we have:

$$I_s(t) = g_m V_{GS1} + g_m V_{RF} \cos(\omega_{RF}t)$$

(3)

$g_m$ is the Transductance of the CMOS M1

$V_{GS1}$ is the bias voltage of the M1 CMOS gate, and is the DC component of the $V_{RF}$ signal

Then we obtain:

$$I_{out}(t) = \left\{ g_m V_{GS1} + g_m V_{RF} \cos(\omega_{RF}) \right\} \frac{4}{\pi} \left\{ \cos(\omega_{LO}t) - \frac{1}{3} \cos(3\omega_{LO}t) + \frac{1}{5} \cos(5\omega_{LO}t) + \ldots \right\}$$

(4)

And as $V_{out}(t) = R_d I_{out}(t)$ we can write:

$$V_{out}(t) = \left\{ \frac{4g_m V_{GS1}}{\pi} R_d \cos(\omega_{LO}t) + \frac{2}{\pi} R_d g_m V_{RF} \left[ \cos((\omega_{RF} - \omega_{LO})t) - \cos((\omega_{RF} + \omega_{LO})t) \right] + \ldots \right\}$$

(5)

The conversion gain is [5]:

$$G_{conv} = \frac{V_{out}(t)_{out-\omega_{LO}}}{V_{RF} \cdot \text{d}^{(\omega_{RF})}} = \frac{2}{\pi} R_d g_m$$

(6)

On the ADS2009 tool we have chosen a model for CMOS 65nm technology [7]. According to a simplified modeling of the internal structure of the transistor M1, we found $g_m$, which is in the range of 34mA / V; this gives a theoretical conversion gain equal to 13.55dB.

### 2.3 Non-linearity

- **1 dB Compression Point**

Like any electronic device with nonlinear active components, the mixer has an output power curve based on that of the entry and presenting a saturation zone. It is characterized by the 1 dB compression point, defined as the RF input power for which the conversion gain is reduced by 1 dB [6] (Fig.3).

- **Order 3 Interception Point (IIP3)**

Also called the intermodulation level of order 3, characterizes the distortion of the system, in effect: we can notice that around two useful rays $f_1$ and $f_2$, can be superimposed two other very close rays $(2 \cdot f_1 - f_2)$ and $(2 \cdot f_2 - f_1)$ that can’t be easily filtered out (Fig.4) [6].
IIP3 is given by the relation:

$$\text{IIP3} = \frac{\Delta}{2} + \text{PowerRF}$$  \hspace{1cm} (7)

or \text{PowerRF} is the input power.

- **Isolation**

Isolation is translated by the power coupled from one port to another. In general for a mixer, whatever its type, isolation is the most critical between RF and LO ports because of their closest frequencies and therefore difficult to filter [5].

$$I_{\text{OL,RF}} = \frac{P_{\text{OL,RF}}}{P_{\text{OL,LO}}}$$  \hspace{1cm} (8)

- **Noise Figure**

The noise figure \text{NF} of a mixer is defined conventionally as the degradation of signal to noise ratio between the input and the output [5]:

$$F = \frac{N_{\text{RF}}}{N_{\text{NF}}} \text{ so } F = \frac{N_{\text{NF}}}{N_{\text{RF}}R_{\text{con}}},$$  \hspace{1cm} (9)

### III. Simulation results

$V_{\text{RF}}$ and $V_{\text{LO}}$ frequencies are respectively 1.9 GHz and 1.8 GHz which provides to an intermediate frequency IF of 100 MHz.

#### 3.1 Transient signals

The Figure 5 show the shape of the IF output signal whose frequency is 100 MHz.

Such a chronogram represents in fact the RF carrier and the useful signal IF that we will have to restore it after an adequate filter. The following figure shows $V(t)$, it’s the output signal $V_{\text{out}}(t)$ after inserting a filter.

#### 3.2 Power Consumption

DC simulation, allowed us to measure the power consumption of the mixer circuit which is 2 mW, with Vdd = 1.8V.

#### 3.3 Harmonic responses

The Figures 7 and 8 show the harmonics response of order 5 of $V_{\text{RF}}$ and $V_{\text{out}}$ signals whose basic rays are represented respectively by 1.9 GHz and 100 MHz frequencies.
Harmonic simulation of mixer circuit results in a conversion gain (equation 6) equal to \((-18.033\text{dB})-(-30.458\text{dB}) = 12.425\text{dB}\) (figures 7 and 8). This reveals the importance of taking into consideration all the internal CMOS parameters which are liable to affect the results.

3.4 dBm Gain

We obtain the function shown in Fig.9, which represents a linear zone (horizontal) where the output is directly proportional to the input, and an area decreasing from -11.5dBm resulted by the non-linearity of the mixer circuit.

3.5 1 dB Compression Point

As shown in Figure 10, it’s the gain value for which the output power (Vout_dBm1) does not follow its right line (Line1) with a difference of 1 dB. It corresponds well to an RF power equal to -11.5 dB.

3.6 Interception Point Order 3 (IIP3)

The simulation result shown in Fig.11, and (equation 7) lead to an IIP3 value in the order of 6 dBm.

3.7 Measure of Isolation between ports
Isolation report (equation 8) is represented in Fig.12; it is equal to -37.704dB for 1.9 GHz RF frequency.

From the curves we obtain: $NIF=4.266nV$ and $NRF=0.383nV$ and knowing $G_{conv} = 12.425dB$, by the relation (9) the noise figure is 8.92dB.

IV. Comparison of performance obtained with recent mixers

According to the simulation results found, choosing the 65nm CMOS technology with the design of other parameters (Rd, Z, .. etc.) of the SBM circuit, allowed us to achieve a very stable gain and linearity over a wide range of input power.

The performances of this mixer (SBM) are compared in the table below with that of some recent mixers:

| Ref | Technology (μm) | RF (GHz) | $GF$ (dB) | $NF$ (dB) | $P_{1}$ (dBm) | $IP_{3}$ (dBm) | $P_{con}$ (mW) |
|-----|-----------------|----------|-----------|-----------|---------------|---------------|---------------|
| [8] | 0.55            | 0.9      | 1.1       | 13.4      | -5.3          | 12.51         | 2.3           |
| [9] | 0.25            | 2.44     | -2.6      | 12.67     | 5.07          | 12.51         | 12.3          |
| [10]| 0.18            | 2.4      | 3.3       | 14.3      | -8.98         | 5.46          | 5.6           |
| [1] | 0.18            | 1.8      | 1         | 8         | -10           | 5             | 2             |

We note that the CMOS 65 nm technology SBM design witch we proposed is performing well in terms of Conversion Gain, Power Consumption, levels of IIP3 point and 1 dB compression point, noise figure still acceptable.

V. Conclusion

The research work presented in this paper is part of the overall objective; to study the feasibility of a Single Balanced Mixer (SBM) in a RF chain, dedicated to wireless applications; by 65nm CMOS technology, also to see from the simulation results, the performance of this choice compared to recent technologies, and finally to proceed to the implementation of this choice.

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