Intel MPX Explained

An Empirical Study of Intel MPX and Software-based Bounds Checking Approaches

https://Intel-MPX.github.io

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Abstract

Memory-safety violations are a prevalent cause of both reliability and security vulnerabilities in systems software written in unsafe languages like C/C++. Unfortunately, all the existing software-based solutions to this problem exhibit high performance overheads preventing them from wide adoption in production runs. To address this issue, Intel recently released a new ISA extension—Memory Protection Extensions (Intel MPX), a hardware-assisted full-stack solution to protect against memory safety violations.

In this work, we perform an exhaustive study of the Intel MPX architecture to understand its advantages and caveats. We base our study along three dimensions: (a) performance overheads, (b) security guarantees, and (c) usability issues. To put our results in perspective, we compare Intel MPX with three prominent software-based approaches: (1) trip-wire—AddressSanitizer, (2) object-based—SAFECode, and (3) pointer-based—SoftBound.

Our main conclusion is that Intel MPX is a promising technique that is not yet practical for widespread adoption. Intel MPX’s performance overheads are still high (~50% on average), and the supporting infrastructure has bugs which may cause compilation or runtime errors. Moreover, we showcase the design limitations of Intel MPX: it cannot detect temporal errors, may have false positives and false negatives in multithreaded code, and its restrictions on memory layout require substantial code changes for some programs.

1 Introduction

The majority of systems software is written in low-level languages such as C or C++. These languages allow complete control over memory layout, which is especially important for systems development. Unfortunately, the ability to directly control memory often leads to violations of memory safety, i.e., illegal accesses to unintended memory regions [50].

In particular, memory-safety violations emerge in the form of spatial and temporal errors. Spatial errors—also called buffer overflows and out-of-bounds accesses—occur when a program reads from or writes to a different memory region than the one expected by the developer. Temporal errors—wild and dangling pointers—appear when trying to use an object before it was created or after it was deleted.

These memory-safety violations may result in sudden crashes, data losses, and other nasty bugs [50]. Moreover, these vulnerabilities can also be exploited to build a memory attack—a scenario when an adversary gets access to an illegal region of memory and can hi-jack the system or steal confidential data. This attack vector is prevailing among low-level languages, with almost 1,200 memory vulnerabilities published only in 2016 according to the US National Vulnerability Database [40].

Given the importance of the problem, there are numerous solutions for enforcing memory safety in unsafe languages, ranging from static analysis to language extensions [8, 12, 13, 18, 24, 31, 32, 35, 38, 41, 42, 47, 55]. In this work, we concentrate on deterministic dynamic bounds-checking since it is widely regarded as the only way of defending against all memory attacks [37, 49]. Bounds-checking techniques augment the original unmodified program with metadata (bounds of live objects or allowed memory regions) and insert checks against this metadata before each memory access. Whenever a bounds check fails, the program is aborted and thus

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This paper presents only the general discussion and aggregated data; for the complete evaluation, please see the supporting website: https://Intel-MPX.github.io/. Evaluation plots and section headings have hyperlinks to the complete experimental description and results.
the attack is prevented. Unfortunately, state-of-the-art bounds-checking techniques exhibit high performance overhead (50–150%) which limits their usage to development stages only.

To lower runtime overheads, Intel recently released a new ISA extension—Memory Protection Extensions (Intel MPX). Its underlying idea is to provide hardware assistance, in the form of new instructions and registers, to software-based bounds checking, making it more efficient.

Yet, to our knowledge, there is no comprehensive evaluation of Intel MPX, neither from the academic community nor from Intel itself. Therefore, the goal of this work was to analyze Intel MPX in three dimensions: performance, security, and usability. Performance is important because only solutions with low (up to 10–20%) runtime overhead have a chance to be adopted in practice [49]. It was also crucial to investigate the root causes of the overheads to pave the way for future improvements. Security assessment on a set of real-world vulnerabilities was required to verify advertised security guarantees. Usability evaluation gave us insights on Intel MPX production quality and—more importantly—on application-specific issues that arise under Intel MPX and need to be manually fixed.

To fully explore Intel MPX’s pros and cons, we put the results into perspective by comparing with existing software-based solutions. In particular, we compared Intel MPX with three prominent techniques that showcase main classes of memory safety: trip-wire AddressSanitizer [47], object-based SAFEC ode [18], and pointer-based SoftBound [38] (see §2 for details).

Our investigation reveals that Intel MPX has high potential, but is not yet ready for widespread use. Some of the lessons we learned are:

- New Intel MPX instructions are not as fast as expected and cause up to 4× slowdown in the worst case, although compiler optimizations amortize it and lead to runtime overheads of ~50% on average.
- The supporting infrastructure (compiler passes and runtime libraries) is not mature enough and has bugs, such that 3–10% programs cannot compile/run.
- In contrast to other solutions, Intel MPX provides no protection against temporal errors.
- Intel MPX may have false positives and false negatives in multithreaded code.
- By default, Intel MPX imposes restrictions on allowed memory layout, such that 8–13% programs do not run correctly without substantial code changes. In addition, we had to apply (non-intrusive) manual fixes to 18% programs.

Though the first three issues can be fixed in future versions, the last two can be considered fundamental design limits. We project that adding support for multithreading would inevitably hamper performance, and relaxing restrictions on memory layout would go against Intel MPX philosophy.

2 Background

All spatial and temporal bugs, as well as memory attacks built on such vulnerabilities, are caused by an access to a prohibited memory region. To prevent such bugs, memory safety must be imposed on the program, i.e., the following invariant must be enforced: memory accesses must always stay within the originally intended (referent) objects.

Memory safety can be achieved by various methods, including pure static analysis [19, 55], hardware-based checking [32, 36, 51, 54], probabilistic methods [13, 33, 43], and extensions of the C/C++ languages [30, 35, 41]. In this work, we concentrate on deterministic runtime bounds-checking techniques that transparently instrument legacy programs (Intel MPX is but one of them). These techniques provide the highest security guarantees while requiring little to no manual effort to adapt the program. For a broader discussion, please refer to [49].

Existing runtime techniques can be broadly classified as trip-wire, object-based, and pointer-based [37]. In a nutshell, all three classes create, track, and check against some bounds metadata kept alongside original data of the program. Trip-wire approaches create “shadow memory” metadata for the whole available program memory, pointer-based approaches create bounds metadata per each pointer, and object-based approaches create bounds metadata per each object.

For comparison with Intel MPX, we chose a prominent example from each of the aforementioned classes: AddressSanitizer, SAFEC ode, and SoftBound. Figure 1 highlights the differences between them.

**Trip-wire approach:** AddressSanitizer [47]. This class surrounds all objects with regions of marked (poisoned) memory called redzones, so that any overflow will change
values in this—otherwise invariable—region and will be consequently detected. In particular, AddressSanitizer reserves 1/8 of all virtual memory for the shadow memory which is accessed only by the instrumentation and not the original program. AddressSanitizer updates data in shadow memory whenever a new object is created and freed, and inserts checks on shadow memory before memory accesses to objects. The check itself looks like this:

```c
shadowAddr = MemToShadow(ptr)
if (ShadowIsPoisoned(shadowAddr))
    ReportError()
```

In addition, AddressSanitizer provides means to detect temporal errors via a quarantine zone: if a memory region has been freed, it is kept in the quarantine for some time before it becomes allowed for reuse.

AddressSanitizer was built for debugging purposes and is not targeted for security (though it could be used in this context [15, 37, 52]). For example, it may not detect non-contiguous out-of-bounds violations. Nevertheless, it detects many spatial bugs and significantly raises the bar for the attacker. It is also the most widely-used technique in its class, comparing favorably to other trip-wire techniques such as Light-weight Bounds Checking [24], Purify [25], and Valgrind [42].

**Object-based approach: SAFECode** [17, 18]. This class’s main idea is enforcing the intended referent, i.e., making sure that pointer manipulations do not change the pointer’s referent object. In SAFECode, this rule is relaxed: each object is allocated in one of several fine-grained partitions—pools—determined at compile-time using pointer analysis; the pointer must always land into the predefined pool. This technique allows powerful optimizations and simple runtime checks against the pool bounds:

```c
poolAddr = MaskLowBits(ptr)
if (poolAddr not in predefinedPoolAddrs)
    ReportError()
```

On the downside, SAFECode provides worse guarantees than AddressSanitizer—buffer overflow to an object in the same pool will go undetected.

We also inspected and discarded other object-based approaches. CRED [46] has huge performance overheads, mudflap [20] is deprecated in newer versions of GCC, and Baggy Bounds Checking [12] is not open sourced.

**Pointer-based approach: SoftBound** [38, 39]. Such approaches keep track of pointer bounds (the lowest and the highest address the pointer is allowed to access) and check each memory write and read against them. Note how SoftBound associates metadata not with an object but rather with a pointer to the object. This allows pointer-based techniques to detect intra-object overflows (one field overflowing into another field of the same struct) by narrowing bounds associated with the particular pointer.

Intel MPX closely resembles SoftBound; indeed, a hardware-assisted enhancement of SoftBound called WatchdogLite shares many similarities with Intel MPX [36]. For our comparison, we used the SoftBound+CETS version which keeps pointer metadata in a two-level trie—similar to MPX’s bounds tables—and introduces a scheme to protect against temporal errors [39]. The checks in this version are as follows:

```c
LoBound, UpBound, key, lock = TrieLookup(ptr)
if (ptr < LoBound or ptr > UpBound or key != +lock)
    ReportError()
```

As for other pointer-based approaches, MemSafe [48] is not open sourced, and CCured [41] and Cyclone [30] require manual changes in programs.

## 3 Intel Memory Protection Extensions

Intel Memory Protection Extensions (Intel MPX) was first announced in 2013 [28] and introduced as part of the Skylake microarchitecture in late 2015 [27]. The sole purpose of Intel MPX is to transparently add bounds checking to legacy C/C++ programs. Consider a code snippet in Figure 2a. The original program allocates an array `a[10]` with 10 pointers to some buffer objects of type `obj` (Line 1). Next, it iterates through the first `M` items of the array to calculate the sum of objects’ length values (Lines 3–8). In C, this loop would look like this:

```c
for (i=0; i<M; i++) total += a[i]−>len;
```

Since `M` is a variable, a bug or a malicious activity may set `M` to a value that is larger than `obj` size and an overflow will happen. Also, note how the array item access `a[i]` decays into a pointer `ai` on Line 4, and how the subfield access decays to `lenptr` on Line 6.

Figure 2b shows the resulting code with Intel MPX protection applied. First, the bounds for the array `a[10]` are created on Line 3 (the array contains 10 pointers each 8 bytes wide, hence the upper-bound offset of 79). Then in the loop, before the array item access on Line 8, two MPX bounds checks are inserted to detect if `a[i]` overflows (Lines 6–7). Note that since the protected load reads an 8-byte pointer from memory, it is important to check `ai+7` against the upper bound (Line 7).

Now that the pointer to the object is loaded in `objptr`, the program wants to load the `obj` `len` subfield. By design, Intel MPX must protect this second load by checking the bounds of the `objptr` pointer. Where does it get these bounds from? In Intel MPX, every pointer stored in memory has its associated bounds also stored in a special memory region accessed via `bdNSTx` and `bd1dx` MPX instructions (see next subsection for details). Thus, when
it is inadvisable to use Intel MPX at all.)

In the following, we detail how Intel MPX support is implemented at each level of the hardware-software stack.

3.1 Hardware

At its core, Intel MPX provides 7 new instructions and a set of 128-bit bounds registers. The current Intel Skylake architecture provides four registers named bnd0–bnd3. Each of them stores a lower 64-bit bound in bits 0–63 and an upper 64-bit bound in bits 64–127.

Instruction set. The new MPX instructions are: bndmk to create new bounds, bndcl and bndcu/bndcn to compare the pointer value against the lower and upper bounds in bnd respectively, bndmov to move bounds from one bnd register to another and to spill them to stack, and bndldx and bndstx to load and store pointer bounds in special Bounds Tables respectively. Note that bndcu has a one’s complement version bndcn which has exactly the same characteristics, thus we mention only bndcu in the following. The example in Figure 2b shows how most of these instructions are used. The instruction not shown is bndmov which serves mainly for internal rearrangements in registers and on stack.

Intel MPX additionally changes the x86-64 calling convention. In a nutshell, the bounds for corresponding pointer arguments are put in registers bnd0–bnd3 before a function call and the bounds for the pointer return value are put in bnd0 before return from the function.

It is interesting to compare the benefits of hardware implementation of bounds-checking against the software-only counterpart—SoftBound in our case [38, 39]. First, Intel MPX introduces separate bounds registers to lower register pressure on the general-purpose register (GPR) file, something that software-only approaches suffer from. Second, software-based approaches cannot modify the calling convention and resort to function cloning, when a set of function arguments is extended to include pointer bounds. This leads to more cumbersome caller/callee code and problems with interoperability with legacy uninstrumented libraries. Finally, dedicated bndcl1 and bndcu instructions substitute the software-based “compare and branch” instruction sequence, saving one cycle and exerting no pressure on branch predictor.

The prominent feature of Intel MPX is its backwards-compatibility and interoperability with legacy code. On the one hand, MPX-instrumented code can run on legacy hardware because Intel MPX instructions are interpreted as NOPs on older architectures. This is done to ease the distribution of binaries—the same MPX-enabled program/library can be distributed to all clients. On the other hand, Intel MPX has a comprehensive support to interop-

1Note that narrowing of bounds is not shown for simplicity, see §3.3.
2Henceforth, we focus on 64-bit Linux-based support of Intel MPX.
erate with unmodified legacy code: (1) a BNDPRESAVE configuration bit allows to pass pointers without bounds information created by legacy code, and (2) when legacy code changes a pointer in memory, the later bndldx of this pointer notices the change and assigns always-true (INIT) bounds to it. In both cases, the pointer created/modified in legacy code is considered “boundless”: this allows for interoperability but also creates holes in Intel MPX defense³ [1].

**Storing bounds in memory.** The current version of Intel MPX has only 4 bounds registers, which is clearly not enough for real-world programs—we will run out of registers even if we have only 5 distinct pointers. Accordingly, all additional bounds have to be stored (spilled) in memory, similar to spilling data out of general-purpose registers. A simple and relatively fast option is to copy them directly into a compiler-defined memory location (on stack) with bndmov. However, it works only inside a single stack frame: if a pointer is later reused in another function, its bounds will be lost. To solve this issue, two instructions were introduced—bndstx and bndldx. They store/load bounds to/from a memory location derived from the address of the pointer itself (see Figure 2b, Line 9), thus making it easy to find pointer bounds without any additional information, though at a price of higher complexity.

When bndstx and bndldx are used, bounds are stored in a memory location calculated with two-level address translation scheme, similar to virtual address translation (paging). In particular, each pointer has an entry in a Bounds Table (BT), which is allocated dynamically and

³x264 from PARSEC highlights this issue: its x264_malloc function internally calls memalign which has no corresponding wrapper. Thus, the pointer returned by this function is “boundless”. Since all dynamic objects are created through this function, the whole program operates on “boundless” pointers, rendering Intel MPX protection utterly useless.

![Figure 3: Loading of pointer bounds using two-level address translation.](image1)

![Figure 4: The procedure of Bounds Table creation.](image2)

is comparable to a page table. Addresses of BTs are stored in a Bounds Directory (BD), which corresponds to a page directory in our analogy. For a specific pointer, its entries in the BD and the BT are derived from the memory address in which the pointer is stored.

Note that our comparison to paging is only conceptual; the implementation side differs significantly. Firstly, the MMU is not involved in the translation and all operations are performed by the CPU itself. Secondly and most importantly, Intel MPX does not have a dedicated cache (such as a TLB cache), thus it has to share normal caches with application data. In some cases, it may lead to severe performance degradation caused by cache thrashing.

The address translation is a multistage process. Consider loading of pointer bounds (Figure 3). In the first stage, the corresponding BD entry has to be loaded. For that, the CPU: (1) extracts the offset of BD entry from bits 20–47 of the pointer address and shifts it by 3 bits (since all BD entries are 2³ bits long), (2) loads the base address of BD from the BNDCFGx register, and (3) sums the base and the offset and loads the BD entry from the resulting address.

In the second stage, the CPU: (4) extracts the offset of BT entry from bits 3–19 of the pointer address and shifts it by 5 bits (since all BT entries are 2⁵ bits long), (5) shifts the loaded entry—which corresponds to the base of BT—by 3 to remove the metadata contained in the first 3 bits, and (6) sums the base and the offset and (7) finally loads the BT entry from the resulting address. Note that a BT entry has an additional “pointer” field—if the actual pointer value and the value in this field mismatch, Intel MPX will mark the bounds as always-true (INIT). This is required for interoperability with legacy code and only happens when this code modifies the pointer.

This operation is expensive—it requires approximately 3 register-to-register moves, 3 shifts, and 2 memory loads. On top of it, since these 2 loads are non-contiguous, the protected application has worse cache locality.

**Interaction with other ISA extensions.** Intel MPX can cause issues when used together with other ISA extensions, e.g., Intel TSX and Intel SGX. Intel MPX may cause transactional aborts in some corner cases when

⁴In particular, BNDCFGU in user space and BNDCFGS in kernel mode.
we are not aware of any side-channel attacks that could make it easier for the protected memory access (which proved wrong).

expected that Intel MPX would take advantage of underutilized CPU resources for programs with low original IPC. This was surprising: we expected the protection does not increase the IPC (instructions/cycle) of programs, which is usually the case for memory-safety techniques (see Figure 11). This was surprising: we expected that Intel MPX would take advantage of underutilized CPU resources for programs with low original IPC. To understand what causes this bottleneck, we measured the throughput of typical MPX check sequences.\(^5\)

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\(^5\)We originally blamed an unjustified data dependency between `bndcl/u` and the protected memory access (which proved wrong).

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![Figure 5: Distribution of Intel MPX instructions among execution ports (Intel Skylake).](image-url)

Our measurements pointed to a bottleneck of “bndcl/u b,m” instructions due to contention on port 1. Without checks (Figure 6 a), our original benchmark could execute two loads in parallel, achieving a throughput of 2 IPC (note that the loaded data is always in a Memory Ordering Buffer). After adding “bndcl/u b,r” checks (Figure 6 b), IPC increased to three instructions per cycle (3 IPC): one load, one lower-, and one upper-bound check per cycle. For “bndcl/u b,m” checks (Figure 6 c), however, IPC became less than original: two loads and four checks were scheduled in four cycles, thus IPC of 1.5. In summary, the final IPC was ~1.5–3 (compare to original IPC of 2), proving that the MPX-protected program typically has approximately the same IPC as the original.

As Figures 9 and 10 show, it causes major performance degradation. It can be fixed, however; if the next generations of CPUs will provide the relative memory address calculation on other ports, the checks could be parallelized and performance will improve. We speculate that GCC-MPX could perform on par with AddressSanitizer in this case, because the instruction overheads are similar. Accordingly, ICC version would be even better and the slowdowns might drop lower than 20%. But we must note that we do not have any hard proof for this speculation.

### 3.2 Operating System

The operating system has two main responsibilities in the context of Intel MPX: it handles bounds violations and manages BTs, i.e., creates and deletes them. Both these actions are hooked to a new class of exceptions, #BR, which has been introduced solely for Intel MPX and is similar to a page fault, although with extended functionality.

**Bounds exception handling.** If an MPX-enabled CPU detects a bounds violation, i.e., if a referenced pointer appears to be outside of the checked bounds, #BR is raised and the processor traps into the kernel (in case of Linux). The kernel decodes the instruction to get the violating address and the violated bounds, and stores them in the

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**Table 1: Latency (cycles/instr) and Tput (instr/cycle) of Intel MPX instructions; b—MPX bounds register; m—memory operand; r—general-purpose register.**

| Instruction     | Description | Lat | Tput |
|-----------------|-------------|-----|------|
| bndmk b,m       | create pointer bounds | 1   | 2    |
| bndcl b,m       | check mem-operand addr against lower | 1   | 1    |
| bndcl b,r       | check reg-operand addr against lower | 1   | 2    |
| bndcu b,m       | check mem-operand addr against upper | 1   | 1    |
| bndcu b,r       | check reg-operand addr against upper | 1   | 2    |
| bndmov b,m      | move pointer bounds from mem | 1   | 1    |
| bndmov b,b      | move pointer bounds to other reg | 1   | 2    |
| bndmov m,b      | move pointer bounds to mem | 2   | 0.5  |
| bndldx b,m      | load pointer bounds from BT | 4-6 | 0.4  |
| bndstx m,b      | store pointer bounds in BT | 4-6 | 0.3  |
siginfo structure. Afterwards, it delivers the SIGSEGV signal to the application together with information about the violation in siginfo. At this point the application developer has a choice: she can either provide an ad-hoc signal handler to recover or choose one of the default policies: crash, print an error and continue, or silently ignore it.

**Bounds tables management.** Two levels of bounds address translation are managed differently: BD is allocated only once by a runtime library (at application startup) and BTs have to be created dynamically on-demand. The later is a task of OS. The procedure is presented in Figure 4. Each time an application tries to store pointer bounds ①, the CPU loads the corresponding entry from the BD and checks if it is a valid entry ②. If the check fails, the CPU raises #BR and traps into the kernel ③. The kernel allocates a new BT ④, stores its address in the BD entry ⑤ and returns in the user space ⑥. Then, the CPU stores bounds in the newly created BT and continues executing the application in the normal mode of operation ⑦.

Since the application is oblivious of BT allocation, the OS also has to free these tables. In Linux, this “garbage collection” is performed whenever a memory object is freed or, more precisely, unmapped. OS goes through the elements of the object and removes all the corresponding BT entries. If one of the tables becomes completely unused, OS will free the BT and remove its entry in the BD.

**Microbenchmark.** To illustrate the additional overhead of allocating and de-allocating BTs, we manufactured two microbenchmarks that showcase the worst case scenarios. The first one stores a large set of pointers in such memory locations that each of them will have a separate BT, i.e., this benchmark indirectly creates a large number of bounds tables. The second one does the same, but in addition, it frees all the memory right after it has been assigned, thus triggering BT de-allocation. Our measurement results are shown in Table 2 (note that we disabled all compiler optimizations to showcase the influence of OS alone). In both cases, most of the runtime parameters (cache locality, branch misses, etc.) of the MPX-protected version are equivalent to the native one. However, the slowdown is noticeable—more than 2 times. It is caused by a single parameter that varies—the number of instructions executed in the kernel space. It means that the overhead is caused purely by the BT management in the kernel. From this, we can conclude that OS itself can make an MPX-protected application up to 2.3× slower, although this scenario is quite rare.

In this section, we discussed only Linux implementation. However, all the same mechanisms can also be found in Windows. The only significant difference is that Intel MPX support on Windows is done by a daemon, while on Linux the functionality is implemented in the kernel itself [7].

### 3.3 Compiler and Runtime Library

Hardware Intel MPX support in the form of new instructions and registers significantly lowers performance overhead of each separate bounds-checking operation. However, the main burden of efficient, correct, and complete bounds checking of whole programs lies on the compiler and its associated runtime.

**Compiler support.** As of the date of this writing, only GCC 5.0+ and ICC 15.0+ compilers have support for Intel MPX [7, 21]. To enable Intel MPX protection of applications, both GCC and ICC introduce the new compiler pass called Pointer(s) Checker. Enabling Intel MPX is intentionally as simple as adding a couple of flags to the usual compilation process:

```bash
>> gcc -fcheck-pointer-bounds -mmmpx test.c
>> icc -check-pointers -mpx=rw test.c
```

In a glance, the Pointer Checker pass instruments the original program as follows. (1) It allocates static bounds for global variables and inserts bndmk instructions for stack-allocated ones. (2) It inserts bndcl and bndcu
When the compiler can statically prove safety of memory writes protection can already provide sufficiently high security guarantees. The user can instruct the compiler to instrument only writes and reads: this ensures protection from buffer over-reads. Otherwise, optimization (2) can kick in and move these bounds-check instructions before each load or store from/to memory.

One of the advantages of Intel MPX—in comparison to AddressSanitizer and SAFECode—is that it supports narrowing of struct bounds by design. Consider struct obj from Figure 2. It contains two fields: a 100B buffer buf and an integer len right after it. It is easy to see that an off-by-one overflow in obj.buf will spillover and corrupt the adjacent obj.len. AddressSanitizer and SAFECode by design cannot detect such intra-object overflows (though AddressSanitizer can be used to detect a subset of such errors [44]). In contrast, Intel MPX can be instructed to narrow bounds when code accesses a specific field of a struct, e.g., on Line 10 in Figure 2b. Here, instead of checking against the bounds of the full object, the compiler would shrink obj.ptr_.b to only four bytes and compare against these narrowed bounds on Lines 11–12. Narrowing of bounds may require (sometimes intrusive) changes in the source code, and is enabled by default.

By default, the MPX pass instruments both memory writes and reads: this ensures protection from buffer over-writes and buffer over-reads. The user can instruct the MPX pass to instrument only writes. The motivation is twofold. First, instrumenting only writes significantly reduces performance overhead of Intel MPX (from 2.5× to 1.3× for GCC). Second, the most dangerous bugs are those that overwrite memory (classic overflows to gain privileged access to the remote machine), and the only-writes protection can already provide sufficiently high security guarantees.

At least in GCC implementation, the pass can be fine-tuned via additional compilation flags. In our experience, these flags provide no additional benefit in terms of performance, security, or usability. For a full list of supported flags, refer to the official documentation of Intel MPX [7].

For performance, compilers must try their best to optimize away redundant MPX code. There are two common optimizations used by GCC and ICC (also used, for example, in Baggy Bounds [12]). (1) Removing bounds-checks when the compiler can statically prove safety of memory access, e.g., access inside an array with a known offset. (2) Moving (hoisting) bounds-checks out of simple loops. Consider Figure 2b. If it is known that k<10, then optimization (1) can remove always-true checks on Lines 6–7. Otherwise, optimization (2) can kick in and move these checks before the loop body, saving two instructions on each iteration.

| Compiler & runtime issues | GCC | ICC |
|---------------------------|-----|-----|
| Poor MPX pass optimizations | 22/38 | 3/38 |
| Bugs in MPX compiler pass: | | |
|ira correct bounds during function calls | – | 2/38 |
| – conflicts with auto-vectorization passes | – | 3/38 |
| – corrupted stack due to C99 VLA arrays | – | 3/38 |
| – unknown internal compiler error | 1/38 | – |
| Bugs and issues in runtime libraries: | | |
| – Missing wrappers for libc functions | all | all |
| – Nullified bounds in memcpy wrapper | all | – |
| – Performance bug in memcpy wrapper | all | – |

*One compiler has >10% worse results than the other.

Runtime library. As a final step of the MPX-enabled build process, the application must be linked against two MPX-specific libraries: libmpx and libmpxwrappers (libchkp for ICC).

The libmpx library is responsible for MPX initialization at program startup: it enables hardware and OS support and configures MPX runtime options (passed through environment variables). Most of these options concern debugging and logging, but two of them define security guarantees. First, CHKP_RT_MODE must be set to “stop” in production use to stop the program immediately when a bounds violation is detected; set it to “count” only for debugging purposes. Second, CHKP_RT_BNDPRESERVE defines whether application can call legacy, uninstrumented functions in external libraries; it must be enabled if the whole program is MPX-protected.

By default, libmpx registers a signal handler that either halts execution or writes a debug message (depending on runtime options). However, this default handler can be overwritten by the user’s custom handler. This can be useful if the program must shutdown gracefully or checkpoint its state.

Another interesting feature is that the user can instruct libmpx to disallow creation of BTs by the OS (see §3.2). In this case, the #BR exception will be forwarded directly to the program which can allocate BTs itself. One scenario where this can come handy is when the user completely distrusts the OS, e.g., when using SGX enclaves [31].

The libmpxwrappers library in GCC (and its analogue libchkp in ICC) contain wrappers for functions from C standard library (libc). Similar to AddressSanitizer, Intel MPX implementations do not instrument libc and instead wrap all its functions with a bounds-checking counterparts.

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All bugs were acknowledged by developers. Bug reports:

https://software.intel.com/en-us/forums/intel-c-compiler/topic/701764
https://software.intel.com/en-us/forums/intel-c-compiler/topic/700675
https://software.intel.com/en-us/forums/intel-c-compiler/topic/700550
**Issues.** For both GCC and ICC, the compiler and runtime support have a number of issues summarized in Table 3.

Concerning performance, current implementations of GCC and ICC take different stances when it comes to optimizing MPX code. GCC is conservative and prefers stability of original programs over performance gains. On many occasions, we noticed that the GCC MPX pass disables other optimizations, e.g., loop unrolling and autovectorization. It also hoists bounds-checks out of loops less often than ICC does. ICC, on the other hand, is more aggressive in its MPX-related optimizations and does not prevent other aggressive optimizations from being applied. Unfortunately, this intrusive behavior renders ICC’s pass less stable: we detected three kinds of compiler bugs due to incorrect optimizations.

We also observed issues with the runtime wrapper libraries. First, only a handful of most widely-used libc functions are covered, e.g., malloc, memcpy, strlen, etc. This leads to undetected bugs when other functions are called, e.g., the bug with recv in §5.2. For use in production, these libraries must be expanded to cover all of libc. Second, while most wrappers follow a simple pattern of “check bounds and call real function”, there exist more complicated cases. For example, memcpy must be implemented so that it copies not only the contents of one memory area to another, but also all associated pointer bounds in BTs. GCC library uses a fast algorithm to achieve this, but ICC’s l1bchkp has a performance bottleneck (see also §4).

**Microbenchmarks.** To understand the impact of different compiler flags and optimizations, we wrote four microbenchmarks, each highlighting a separate MPX feature. Two benchmarks—arraywrite and arrayread—perform writes to/reads from memory and stress bndcl and bndcu accordingly. The struct benchmark writes in an inner array inside a struct and stresses the bounds-narrowing feature via bndmk and bndmov. Finally, the ptrcreation benchmark constantly assigns new values to pointers and stresses bounds propagation via bndstx. Figure 7 shows the performance overheads over native versions.

We can notice several interesting details. First, arraywrite and arrayread represent bare overhead of bounds-checking instructions (all in registers), 50% in this case. struct has a higher overhead of $2.1 - 2.8 \times$ due to the more expensive making and moving of bounds to and from the stack. The $5 \times$ overhead of ptrcreation is due to storing of bounds—the most expensive MPX operation (see §3.1). Such high overhead is alarming because pointer-intensive applications require many loads and stores of bounds.

Second, there is a 25% difference between GCC and ICC in arraywrite. This is the effect of optimizations: GCC’s MPX pass blocks loop unrolling while ICC’s implementation takes advantage of it. (Interestingly, the same happened in case of arrayread but the native ICC version was optimized even better, which led to a relatively poor performance of ICC’s MPX.)

Third, the overhead of arrayread becomes negligible with the only-writes MPX version: the only memory accesses in this benchmark are reads which are left uninstrumented. Finally, the same logic applies to struct—disabling narrowing of bounds effectively removes expensive bndmk and bndmov instructions and lowers performance overhead to a bare minimum.

3.4 Application

At the application level, we observed two main issues of Intel MPX. First, Intel MPX cannot support several widely-used C programming idioms (some by design, some due to implementation choices) and thus can break programs. Second and more importantly, there is no support for multithreaded programs.

**Not supported C idioms.** As discussed previously, one of the main features of Intel MPX—narrowing of bounds—can increase security because the code that explicitly works with one field of a complex object will not be able corrupt other fields. Unfortunately, our evaluation reveals that narrowing of bounds breaks many programs (see Table 4). The general problem is that C/C++ programs frequently deviate from the standard memory model [16, 34].

A common C idiom (before C99) is flexible array fields with array size of one, e.g., arr[1]. In practice, objects with such array fields have a dynamic size of more than one item, but there is no way of MPX knowing this at compile-time. Thus, Intel MPX attempts to nar-

---

Table 4: Applications may violate memory-model assumptions of Intel MPX. Columns 2 and 3 show number of misbehaving programs (out of total 38).

| Application-level issues | GCC | ICC |
|--------------------------|-----|-----|
| Flexible or variable-sized array (arr[1]) | 7/38 | 7/38 |
| Accessing struct through struct field | 1/38 | 3/38 |
| Custom memory management | 2/38 | 2/38 |

* GCC affects less programs due to milder rules w.r.t. first field of struct


```c
char* arr[1000];  ; ; Array with MPX data race
char obj1         ; ; Two adjacent objects 
char obj2

while (true):
    ;; Background thread
    for (i=0; i<1000; i++) arr[i] = &obj1

for (i=0; i<1000; i++) arr[i] = &obj2

while (true):
    ;; Main thread
    for (i=0; i<1000; i++) *(arr[i] + offset)
```

**Figure 8:** This program breaks Intel MPX. If `offset=0` then MPX has false alarms, else — undetected bugs.

row bounds to one-item size whenever `arr` is accessed, which leads to false positives. A similar idiom is variable-sized arrays also not supported by Intel MPX, e.g., `arr[]`. These idioms are frequently seen in modern programs, see Table 4, row 1. Note that the C99-standard `arr[0]` is acceptable and does not break programs.

Another common idiom is using a struct field (usually the first field of struct) to access other fields of the struct. Again, this breaks the assumptions of Intel MPX and leads to runtime #BR exceptions (see Table 4, row 2). GCC makes an exception for this case since it is such a popular practice, but ICC is strict and does not have this special rule.

Finally, some programs introduce “memory hacks” for performance, ignoring restrictions of the C memory model completely. The SPEC2006 suite has two such examples: `gcc` has its own complicated memory management with arbitrary type casts and in-pointer bit twiddling, and `soplex` features a scheme that moves objects from one memory region to another by adding an offset to each affected pointer (Table 4, row 3). Both these cases lead to false positives.

Ultimately, all such non-compliant cases must be fixed (indeed, we patched flexible/variable-length array issues to work under Intel MPX). However, sometimes the user may have strong incentives against modifying the original code. In this case, she can opt for slightly worse security guarantees and disable narrowing of bounds via a `fno-chkp-narrow-bounds` flag. Another non-intrusive alternative is to mark objects that must *not* be narrowed (e.g., flexible arrays) with a special compiler attribute.

**Multithreading issues.** Current Intel MPX implementations may introduce false positives and negatives in multithreaded programs [16]. The problem arises because of the way Intel MPX loads and stores pointer bounds via its `bndldx` and `bndstx` instructions. Recall from §3 that whenever a pointer is loaded from main memory, its bounds must also be loaded from the corresponding bounds table (Figure 2b, Lines 8-9).

Ideally, the load of the pointer and its bounds must be performed *atomically* (same for stores). However, nor

the current hardware implementation neither GCC/ICC compilers enforce this atomicity. This lack of proper multithreading support in Intel MPX can lead to (1) correct programs crashing due to false alarms, or (2) buggy programs being exploited *even if* protected by Intel MPX.

Consider an example in Figure 8. A “pointer bounds” data race happens on the `arr` array of pointers. The background thread fills this array with all pointers to the first or to the second object alternately. Meanwhile, the main thread accesses a whatever object is currently pointed-to by the array items. Note that depending on the value of the constant `offset`, the original program is either always-correct or always-buggy: if `offset` is zero, then the main thread always accesses the correct object, otherwise it accesses an incorrect, adjacent object. The second case, if found in a real code, introduces a vulnerability which could be exploited by an adversary.

With Intel MPX, additional `bndstx` instruction is inserted in Line 2 to store the bound corresponding to the first object (same for Line 3 and second object). Also, a `bndldx` instruction is inserted in Line 5 to retrieve the bound for an object referenced by `arr[1]`. Bound checks `bndcl` and `bndceu` are also added at Line 5, before the actual access to the object. Now, the following race can occur. The main thread loads the pointer-to-first-object from the array and—right before loading the corresponding bound—is preempted by the background thread. The background thread overwrites all array items such that they point to the second object, and also overwrites the corresponding bounds. Finally, the main thread is scheduled back and loads the bound, however, the bound now corresponds to the second object. The main thread is left with the pointer to the first object but with the bounds of the second one.

We implemented this test case in C and compiled it with both GCC and ICC. As expected, the MPX-enabled program had both false positives and false negatives.

In case of a correct original program (i.e., with `offset=0`), such discrepancy leads to a *false positive* when actually accessing the object at Line 5. Indeed, the pointer to the object is correct but the bounds were overwritten by the background thread, so MPX triggers a false-alarm exception. Debugging the root cause of such non-deterministic pseudo-bugs would be a frustrating experience for end users.

The case of an originally buggy program (with `offset=1`) is more disconcerting. After all, Intel MPX is supposed to detect all out-of-bounds accesses, but in this example Intel MPX introduces *false negatives!* Here, the pointer to the first object plus `offset` incorrectly lends into the second object. But since the main thread checks against the bounds of the second object, this bug is not caught by Intel MPX. We believe that this implement-
tation flaw—that out-of-bounds bugs can sometimes go unnoticed—can scare off users of multithreaded applications. We also believe that a resourceful hacker would be able to construct an exploit that, based on these findings, could overcome Intel MPX defense with a high probability [56].

We must note however that we did not observe incorrect behavior in Phoenix and PARSEC multithreaded benchmark suites—we were lucky not to encounter programs that break Intel MPX.

For safe use in multithreaded programs, MPX instrumentation must enforce atomicity of loading/storing pointers and their bounds. At the software (compiler) level, this dictates the use of some synchronization primitive around each pair of mov-bndldx/bndstx, being it fine-grained locks, hardware transactional memory, or atoms. Whatever primitive is chosen, we conjecture a significant drop in performance of Intel MPX.

A solution at a microarchitectural level would be to merge the pairs mov-bndldx/bndstx and assure their atomic execution. The instruction decoder could detect a bndldx, find the corresponding pointer mov in the instruction queue, and instruct the rest of execution to handle these instructions atomically. However, we believe this solution could require intrusive changes to the CPU front-end. Moreover, it would significantly limit compiler optimization capabilities.

4 Measurement Study

In this section we answer the following questions:

• What is the performance penalty of Intel MPX?
  – How much slower does a program become?
  – How does memory consumption change?
  – How does protection affect scalability of multithreaded programs?
• What level of security does Intel MPX provide?
• What usability issues arise when Intel MPX is applied?

4.1 Experimental Setup

All the experimental infrastructure was build using Fex [5] benchmarking framework with corresponding changes for the required build types, measurement tools, and for certain experimental procedures.

Testbed. All the experiments were performed on the following setup:

1. Hardware:
   • Intel(R) Xeon(R) CPU E3-1230 v5 @ 3.40GHz
   • 1 socket, 8 hyper-threads, 4 physical cores
   • CPU caches: L1d = 32KB, L1i = 32KB, L2 = 256KB, shared L3 = 8MB
   • 64 GB of memory

2. Network. For experiments on case studies, we used two machines with the network bandwidth between them equal to 938 Mbits/sec as measured by iperf.

3. Software infrastructure:
   • Kernel: 4.4.0
   • GLibC: 2.21
   • Binutils: 2.26.1

4. Compilers:
   • GCC 6.1.0. Configured with:
     

Measurement tools. We used the following tools for measurements:

• perf stat. Our main tool used to measure all CPU-related parameters. The full list includes:

  

Not to introduce additional measurement error, we measured these parameters in parts, 8 parameters at a time.

• time. Since perf does not provide capabilities for measuring physical memory consumption of a process, we used time -v -v -v -v and collected maximum resident set size.

• Intel Pin. To gather Intel MPX instruction statistics, we developed a Pin tool. Full code of our instrumentation can be found in the repository.

Benchmarks. We used three benchmark suits in our eval-
uation: PARSEC 3.0 [14], Phoenix 2.0 [45], and SPEC CPU 2006 [26]. To remove some of the previously found bugs, we applied a patch to SPEC suite. Also, during our work, we found and fixed a set of bugs in them.

All the benchmarks were compiled together with the libraries they depend upon (except raytrace from PARSEC which requires X11 libraries).

### Build types.

- **GCC implementation of MPX.**
  - Compiler flags:
    - `-fcheck-pointer-bounds -mmmpx`
  - Linker flags:
    - `-lmmpx -lmmpxwrappers`
  - Environment variables:
    - `CHKP_RT_BNDPRESERVE="0"`
    - `CHKP_RT_MODE="stop"`
    - `CHKP_RT_VERBOSE="0"`
    - `CHKP_RT_PRINT_SUMMARY="0"`
  - Subtypes:
    - * Disabled bounds narrowing:
      - `-fno-chkp-narrow -bounds`
    - * Protecting only memory writes, not reads:
      - `-fno-chkp-check -read`

- **ICC implementation of MPX.**
  - Compiler flags:
    - `-check-pointers -mpx=rw`
  - Linker flags:
    - `-lm`
  - Environment variables:
    - `CHKP_RT_BNDPRESERVE="0"`
    - `CHKP_RT_MODE="stop"`
    - `CHKP_RT_VERBOSE="0"`
    - `CHKP_RT_PRINT_SUMMARY="0"`
  - Subtypes:
    - * Disabled bounds narrowing:
      - `-noinstrument -param asan`
    - * Protecting only memory writes, not reads:
      - `-check_pointers -mpx=write`
      // instead of
      `-check_pointers -mpx=rw`

- **AddressSanitizer (both GCC and Clang).**
  - Compiler flags:
    - `-fsanitize=address`
  - Environment variables:
    - `ASAN_OPTIONS="verbosity=0:`
    - `detect_leaks=false;`
    - `print_summary=true;`
    - `halt_on_error=true;`
    - `poison_heap=true;`
    - `alloc_dealloc_mismatch=0;`
    - `new_delete_type_mismatch=0;`

---

### Table 5: Variation of results in our experiments.

| Experiment | Average CV, % | Maximum CV, % |
|------------|---------------|---------------|
| Phoenix    | 0.34          | 3.87          |
| PARSEC     | 0.28          | 3.75          |
| SPEC       | 0.41          | 3.96          |
| All        | 0.35          | 3.96          |

Experiments. Each program was executed 10 times, and the results were averaged using arithmetic mean (note, we made sure that variance is very low and it is safe to use arithmetic mean). The mean across different programs in the benchmark suite was calculated using geometric mean. Geometric mean was also used to calculate the “final” mean across three benchmark suites.

We performed the following types of experiments:

- **normal:** experiments on a single thread (serialized) and with fixed input
- **multithreaded:** experiments on 2, 4, and 8 threads
- **variable inputs:** experiments with increasing input size (5 runs, each next one with an input twice bigger than the previous)

The results were checked to fulfill the following criteria:

- application compiled successfully
- application run successfully (with zero exit code)
- the output is equal to the output of non-protected application (if it is deterministic)

Values of coefficient of variation (CV) are presented in Table 5.

### 4.2 Performance

To evaluate overheads incurred by Intel MPX, we tested it on three benchmark suites: Phoenix 2.0 [45], PARSEC 3.0 [14], and SPEC CPU2006 [26]. To put the results into context, we measured not only the ICC and GCC implementations of Intel MPX, but also AddressSanitizer, SAFECode, and SoftBound (see §2 for details).

**Runtime overhead.** We start with the single most impor-
tant parameter: runtime overhead (see Figure 9).

First, we note that ICC-MPX performs significantly better than GCC-MPX. At the same time, ICC is less usable: only 30 programs out of total 38 (79%) build and run correctly, whereas 33 programs out of 38 (87%) work under GCC (see also §4.4).

AddressSanitizer, despite being a software-only approach, performs on par with ICC-MPX and better than GCC-MPX. This unexpected result testifies that the hardware-assisted performance improvements of Intel MPX are offset by its complicated design and suboptimal instructions. Although, AddressSanitizer provides worse security guarantees than Intel MPX (§4.3).

SAFECode and SoftBound show good results on Phoenix programs, but behave much worse—both in terms of performance and usability—on PARSEC and SPEC. First, consider SAFECode on Phoenix: due to the almost-pointerless design and simplicity of Phoenix programs, SAFECode achieves a low overhead of 5%. However, it could run only 18 programs out of 31 (58%) on PARSEC and SPEC and exhibited the highest overall overheads. SoftBound executed only 7 programs on PARSEC and SPEC (23%). Moreover, both SAFECode and SoftBound showed unstable behavior: some programs had overheads of more than 20×.

**Instruction overhead.** In most cases, performance overheads are dominated by a single factor: the increase in number of instructions executed in a protected application. It can be seen if we compare Figures 9 and 10; there is a strong correlation between them.

As expected, the optimized MPX (i.e., ICC version) has low instruction overhead due to its HW assistance (≈70% lower than AddressSanitizer). Thus, one could expect sufficiently low performance overheads of Intel MPX once the throughput and latencies of Intel MPX instructions improve (see §3.1).

Instruction overhead of Intel MPX may also come from the management of Bounds Tables (see §3.2). Our microbenchmarks show that it can cause a slowdown of more than 100% in the worst case. However, we did not observe a noticeable impact in real-world applications. Even those applications that create hundreds of BTs exhibit a minor slowdown in comparison to other factors.

**IPC.** Many programs do not utilize the CPU execution-unit resources fully. For example, the theoretical IPC (instructions/cycle) of our machine is ∼5, but many programs achieve only 1–2 IPC in native executions (see Figure 11). Thus, memory-safety techniques benefit from underutilized CPU and partially mask their performance overhead.

The most important observation here is that Intel MPX does not increase IPC. Our microbenchmarks (§3.1) indicate that this is caused by contention of MPX bounds-checking instructions on one execution port. If this functionality would be available on more ports, Intel MPX would be able to use instruction parallelism to a higher extent and the overheads would be lower.

At the same time, software-only approaches—especially AddressSanitizer and SoftBound—significantly increase IPC, partially hiding their performance overheads.

**Cache utilization.** Some programs are memory-intensive and stress the CPU cache system. If a native program has many L1 or LLC cache misses, then the memory subsystem becomes the bottleneck. In these cases, memory-safety techniques can partially hide their performance overhead.

It can be illustrated with the wordcnt example compiled with ICC-MPX (Figure 12). It has a huge instruction overhead of 4×, IPC close to native, and (as we will see next) many expensive bndldx and bndstdx operations. And still its performance overhead is only 3×. Why? It appears the native version of wordcnt has a significant number of cache misses. They have high performance cost and therefore can partially mask the overhead of ICC-MPX.

**Intel MPX instructions.** In the case of Intel MPX, one of the most important performance factors is the type of instructions that are used in instrumentation. In particular, storing (bndstx) and loading (bndldx) bounds require two-level address translation—a very expensive operation that can break cache locality (see §3.1). To prove it, we measured the shares of MPX instructions in the total number of instructions of each program (Figure 13).

As expected, a lion share of all MPX instructions are bounds-checking bndc1 and bndcu. Additionally, many programs need bndmov to move bounds from one register to another (bndmovreg) or spill bounds on stack (bndmovmem). Finally, pointer-intensive programs require the use of expensive bndstx and bndldx to store/load bounds in Bounds Tables.

There is a strong correlation between the share of bndstx and bndldx instructions and performance overheads. For example, matrixmul under ICC-MPX almost exclusively contains bounds checks: accordingly, there is a direct mapping between instruction and performance overheads. However, the GCC-MPX version is less optimized and inserts many bndldx, which leads to a significantly higher performance overhead.

The ICC-MPX version of wordcnt has a ridiculous share of bndldx/bndstx instructions. This is due to a performance bug in libchkp library of ICC that uses a naive algorithm for the memcpy wrapper (see §3.3).
Memory consumption. In some scenarios, memory overheads (more specifically, resident set size overheads) can be a limiting factor, e.g., for servers in data centers which co-locate programs and perform frequent migrations. Thus, Figure 14 shows memory overhead measurements.

On average, Intel MPX has a 2.1× memory overhead under ICC version and 1.9× under GCC. It is a significant improvement over AddressSanitizer (2.8×). There are three main reasons for that. First, AddressSanitizer changes memory layout of allocated objects by adding “redzones” around each object. Second, it maintains a “shadow zone” that is directly mapped to main memory and grows linearly with the program’s working set size. Third, AddressSanitizer has a “quarantine” feature that restricts the reuse of freed memory. On the contrary, Intel MPX allocates space only for pointer-bounds metadata and has an intermediary Bounds Directory that trades lower memory consumption for longer access time. Interestingly, SAFECode exhibits even lower memory overheads because of its pool-allocation technique. Unfortunately, low memory consumption does not imply good performance.

Influence of additional Intel MPX features. Intel MPX has two main features that influence both performance and security guaranties (§3.3). Bounds narrowing increases security level but may harm performance. Only-write protection, on the other side, improves performance by disabling checks on memory reads.

The comparison of these features is presented in Figure 14. On average, Intel MPX has a 2.1× memory overhead under ICC version and 1.9× under GCC. It is a significant improvement over AddressSanitizer (2.8×). There are three main reasons for that. First, AddressSanitizer changes memory layout of allocated objects by adding “redzones” around each object. Second, it maintains a “shadow zone” that is directly mapped to main memory and grows linearly with the program’s working set size. Third, AddressSanitizer has a “quarantine” feature that restricts the reuse of freed memory. On the contrary, Intel MPX allocates space only for pointer-bounds metadata and has an intermediary Bounds Directory that trades lower memory consumption for longer access time. Interestingly, SAFECode exhibits even lower memory overheads because of its pool-allocation technique. Unfortunately, low memory consumption does not imply good performance.

Influence of additional Intel MPX features. Intel MPX has two main features that influence both performance and security guaranties (§3.3). Bounds narrowing increases security level but may harm performance. Only-write protection, on the other side, improves performance by disabling checks on memory reads.

The comparison of these features is presented in Figure 14.
ures 15 and 16. As we can see, bounds narrowing has a low impact on performance because it does not change the number of checks. At the same time, it may slightly increase memory consumption because it has to keep more bounds. Only-write checking has the opposite effect—having to instrument less code reduces the slowdown but barely has any impact on memory consumption.

**Multithreading.** To evaluate the influence of multithreading, we measured execution times of all benchmarks on 2 and 8 threads (see Figure 17). Note that only Phoenix and PARSEC are multithreaded (SPEC is not). Also, both SoftBound and SAFECode are not thread-safe and therefore were excluded from measurements.

As we can see from Figure 17, the difference in scalability is minimal. For Intel MPX, it is caused by the absence of multithreading support, which means that no additional code is executed in multithreaded versions. For AddressSanitizer, there is no need for explicit synchronization—the approach is thread-safe by design.

Peculiarly, GCC-MPX experiences no speedups but slowdowns on `linearreg` and `wordcnt`. Upon examining these cases, we found out that this anomaly is due to detrimental cache line sharing of BT entries.

For `swaptions`, AddressSanitizer and Intel MPX scale significantly worse than native. It turns out that these techniques do not have enough spare IPC resources to fully utilize 8 threads in comparison to the native version (the problem of hyperthreading). Similarly, for `streamcluster`, Intel MPX performs worse than AddressSanitizer and native versions. This is again an issue with hyperthreading: Intel MPX instructions saturate IPC resources on 8 threads and thus cannot scale as good as native.

**Varying inputs sizes.** Different input sizes (working sets) may cause different cache behaviors, which in turn causes changes in overheads. To investigate the extent of such effects, we ran several benchmarks with three inputs—small, medium, and large. The results do not provide any unexpected insights and thus omitted from the paper (but can be found on the website). The general trend is that the input size has very little impact on performance overhead.

### 4.3 Security

**RIPE testbed.** We evaluated all approaches against the RIPE security testbed [53]. RIPE is a synthesized C program that tries to attack itself in a number of ways, by overflowing a buffer allocated on the stack, heap, or in data or BSS segments. RIPE can imitate up to 850 attacks, including shellcode, return-into-libc, and return-oriented programming. In our evaluation, even under relaxed security flags—we disabled Linux ASLR, stack canaries, and fortify-source and enabled executable stack—modern compilers were susceptible only to a small number of attacks. Under native GCC, only 64 attacks survived, under ICC—34, and under Clang—38.

The results for all approaches are presented in Table 6. Surprisingly, a default GCC-MPX version showed very poor results, with 41 attacks (or 64% of all possible attacks) succeeding. As it turned out, the default GCC-MPX flags are sub-optimal. First, we found a bug in the `memcpy` wrapper which forced bounds registers to be nullified, so the bounds checks on `memcpy` were rendered useless (see Table 3). This bug disappears if the `BIDPRESERVE` environment variable is manually set to one. Second, the MPX pass in GCC does not narrow bounds for the first field of a struct by default, in contrast to ICC which is more strict. To catch intra-object overflows happening in the

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8 RIPE is specifically tailored to GCC, thus more attacks are possible under this compiler.
Phoenix PARSEC SPEC smatch matrixmul wordcnt blackscholes facesim swaptions bz2 mcf perlbmk
1
2
4
8
Normalized runtime (w.r.t. native)
Full (ICC) No narrow bounds (ICC) Only write (ICC) Full (GCC) No narrow bounds (GCC) Only write (GCC)

Figure 15: Impact of MPX features—narrowing and only-write protection—on performance. (Lower is better.)

Figure 16: Impact of MPX features—narrowing and only-write protection—on memory. (Lower is better.)

| Approach                | Working attacks                                                                 |
|-------------------------|---------------------------------------------------------------------------------|
| MPX (GCC) default *     | 41/64 (all memcpy and intra-object of.)                                         |
| MPX (GCC)               | 0/64 (none)                                                                     |
| MPX (GCC) no narrow     | 14/64 (all intra-object overflows)                                              |
| MPX (ICC)               | 0/34 (none)                                                                     |
| MPX (ICC) no narrow     | 14/34 (all intra-object overflows)                                              |
| AddressSanitizer (GCC)  | 12/64 (all intra-object overflows)                                              |
| SoftBound (Clang)       | 14/38 (all intra-object overflows)                                              |
| SAFECode (Clang)        | 14/38 (all intra-object overflows)                                              |

*Without -fchkp-first-field-has-own-bounds and with BNDPRESERVE=0

Table 6: Results of RIPE security benchmark. In Col. 2, “41/64” means that 64 attacks were successful in native GCC version, and 41 attacks remained in MPX version.

first field of structs—the case of RIPE code—one needs to pass the -fchkp-first-field-has-own-bounds flag to GCC. When we enabled these two flags, all attacks were prevented; all next rows in the table were tested with these flags.

Other results are expected. Intel MPX versions without narrowing of bounds overlook 14 intra-object overflow attacks, where a vulnerable buffer and a victim object live in the same struct. The same attacks are overlooked by AddressSanitizer, SoftBound, and SAFECode. Interestingly, AddressSanitizer has 12 working attacks, i.e., two attacks less than other approaches. Though we did not inspect this in detail, AddressSanitizer was able to prevent two shellcode intra-object attacks on the heap.

We performed the same experiment with only-writes versions of these approaches, and the results were exactly the same. This is explained by the fact that RIPE constructs only control-flow hijacking attacks and not information leaks (which could escape only-writes protection).

Other detected bugs. During our experiments, we found 6 real out-of-bounds bugs (true positives). Five of these bugs were already known, and one was detected by GCC-MPX and was not previously reported.

The bugs found are: (1) incorrect black-and-white input pictures leading to classic buffer overflow in ferret, (2) wrong preincrement statement leading to classic off-by-one bug in h264ref, (3) out-of-bounds write in perlbench, (4) benign intra-object buffer overwrite in x264, (5) benign intra-object buffer read in h264ref, and (6) intra-object buffer overwrite in perlbench.

All of these bugs were detected by GCC-MPX with narrowing of bounds. Predictably, three intra-object bugs and one read-only bug could not be detected by the no-narrowing and only-writes versions of Intel MPX respectively. ICC-MPX detected only three bugs in total: in other cases programs failed due to MPX-related issues (see §3.3 and §3.4). An interesting correlation emerged: the programs that contain real bugs are also the ones that break most often under Intel MPX.

As expected, AddressSanitizer found only three of these bugs—it checks bounds at the level of whole objects and cannot detect intra-object overflows. SAFECode found bugs (2) and (3), the others either could not be detected due to coarse-grained granularity of bounds-checking or SAFECode could not compile the programs. Unfortunately, SoftBound left bug (2) undetected and broke on other three programs with bugs: ferret and x264 are multithreaded and thus not supported by SoftBound, and perlbench would not run correctly.

4.4 Usability

As we showed in §3.4, some programs break under Intel MPX because they use unsupported C idioms or outright violate the C standard. Moreover, as shown in §3.3, other
programs even fail to compile or run due to internal bugs in the compiler MPX passes (one case for GCC and 8 for ICC).

Figure 18 highlights the usability of Intel MPX, i.e., the number of MPX-protected programs that fail to compile correctly and/or need significant code modifications. Note that many programs can be easily fixed (see Table 4); we do not count them as broken. MPX security levels are based on our own classification and correspond to the stricter protection rules, where level 0 means unprotected native version and 6—the most secure MPX configuration (see §6). In total, our evaluation covers 38 programs from the Phoenix, PARSEC, and SPEC benchmark suites.

As can be seen, around 10% of programs break already at the weakest level 1 of Intel MPX protection (without narrowing of bounds and protecting only writes). At the highest security level 6 (with enabled BNDPRESERVE), most of the programs fail.

As for other approaches, no programs broke under AddressSanitizer. For SAFECoder, around 70% programs executed correctly (all Phoenix, half of PARSEC, and 3/4 of SPEC). SoftBound—being a prototype implementation—showed poor results, with only simple programs surviving (all Phoenix, one PARSEC, and 6 SPEC). These results roughly correspond to the ones in the original papers [18, 38].

Encountered issues. Figure 19 presents an overview of the issues we encountered during our experiments.

AddressSanitizer has no usability issues—by design it makes no assumptions on the C standard with respect to the memory model. Also, it is the most stable tested product, fixed and updated with each new version of GCC and Clang.

On the contrary, SoftBound and SAFECoder are research prototypes. They work perfectly with very simple programs from Phoenix, but are not able to compile/run correctly the more complicated benchmarks from PARSEC and SPEC. Moreover, SoftBound does not support multithreading, and any multithreaded program immediately fails under it.

Both GCC-MPX and ICC-MPX break most programs on Level 6 (with BNDPRESERVE=1). This is because BNDPRESERVE does not clear bounds on pointers transferred from/to unprotected legacy libraries. This means that any pointer returned from or modified by any legacy library (including C standard library) will almost certainly contain wrong bounds. Because of this, 89% of GCC-MPX and 76% of ICC-MPX programs break. These cases are represented as gray boxes.

Note that for Phoenix, GCC-MPX fails in most cases while ICC-MPX works correctly. This is because of a slight difference in libc wrappers: all the failing programs use mmap64 function which is correctly wrapped by ICC-MPX but ignored by GCC-MPX. Thus, in the GCC case, the newly allocated pointer contains no bounds which (under BNDPRESERVE=1) is treated as an out-of-bounds violation.

One can wonder why some programs still work even if interoperability with C standard library is broken. The reason is that programs like kmeans, pca, and lbm require literally no external functions except malloc, memset, free, etc.—which are provided by the wrapper MPX libraries.

Some programs break due to memory model violation:

- ferret and raytrace both have structs with the first field used to access other fields in the struct (a common practice that is actually disallowed by the C standard). ICC-MPX disallows this behavior when bounds narrowing is enabled. GCC-MPX allows such behavior by default and has a special switch to tighten it (-fno-chkp-first-field-has-own-bounds) which we classify as Level 5.
- gcc has its own complex memory model with bit-twiddling, type-casting, and other practices depre-
In some cases, real bugs were detected (see also §4.3):

- Three bugs in ferret, h264ref, and perlbench were detected and fixed by us. These fixes are represented as blue background.
- Three bugs in x264, h264ref, and perlbench were detected only by GCC-MPX versions. These bugs are represented as red boxes. Note that ICC-MPX missed bugs in h264ref and perlbench. Upon debugging, we noticed that ICC-MPX narrowed bounds less strictly than GCC-MPX and thus missed the bugs. We were not able to hunt out the root cause, but presume it is due to different memory layouts generated by GCC and ICC compilers.

In rare cases, we hit compiler bugs in GCC and ICC:

- GCC-MPX had only one bug, an obscure “fatal internal GCC compiler error” on only-write versions of xalancbmk.
- ICC-MPX has an autovectorization bug triggered on some versions of vips, gobmk, h264ref, and milc.
- ICC-MPX has a “wrong-bounds through indirect call” bug triggered on some versions of x264 and xalancbmk.
- ICC-MPX has a bug we could not identify triggered on dealII.
- We also manually fixed all manifestations of the C99 VLA bug in ICC-MPX. These bugs are represented as pink background.
5 Case Studies

To understand how Intel MPX affects complex real-world applications, we experimented with three case studies: Apache and Nginx web servers and Memcached memory caching system. Similar to the previous section, we evaluated these programs along three dimensions: performance and memory overheads, security guarantees, and usability.

We compare default Intel MPX implementations of both GCC and ICC against the native version, as well as AddressSanitizer. We were not able to compile any of the case studies under SoftBound and SAFECode: in most cases, the Configure scripts complained about an “unsupported compiler”, and in one case (Apache under SoftBound) the compilation crashed due to an internal compiler error. The native version we chose to show is GCC: native ICC and Clang versions have almost identical results, with an exception of Nginx explained later. For the same reasons, we show only the GCC implementation of AddressSanitizer.

All experiments were performed on the same machines as in the previous section (§4). One machine served as a server and a second one as clients, connected with a 1GB Ethernet cable and an actual bandwidth of 938 Mbits/sec. We configured all case studies to utilize all 8 cores of the server (details below). For other configuration parameters, we kept their default values.

All three programs were linked against their dependent libraries statically. We opted for static linking to investigate the complete overhead of all components constituting each program.

5.1 Apache Web Server

For evaluation, we used Apache version 2.4.18 linked against OpenSSL 1.0.1f [4]. This OpenSSL version is vulnerable to the infamous Heartbleed bug which allows the attacker to leak confidential information such as secret keys and user passwords in plain-text [11]. Since both AddressSanitizer and Intel MPX do not support inline assembly, we disabled it for all builds of Apache. To fully utilize the server, we used the default configuration of Apache’s MPM event model.

The classic ab benchmark was run on a client machine to generate workload, constantly fetching a static 2.3K web-page via HTTP, with a KeepAlive feature enabled. To adapt the load, we increased the number of simultaneous requests at a time.

Unfortunately, while testing against Heartbleed, we discovered that ICC-MPX suffers from a run-time Intel compiler bug9 in the x509_cbc OpenSSL function, leading to a crash of Apache. This bug triggered only on HTTPS connections, thus allowing us to still run performance experiments on ICC-MPX.

Performance. As Figure 20a shows, GCC-MPX, ICC-MPX, and AddressSanitizer all show minimal overheads, achieving 95.3%, 95.7%, and 97.5% of native throughput. Overhead in latency did not exceed 5%. Such good performance is explained by the fact that our experiment was limited by the network and not CPU or memory. (We observed around 480 – 520% CPU utilization in all cases.)

In terms of memory usage (Table 7), AddressSanitizer exhibits an expected 3.5× overhead. In contrast, Intel MPX variants have dramatic 12.8× increase in memory consumption. This is explained by the fact that Apache allocates an additional 1MB of pointer-heavy data per each client, which in turn leads to the allocation of many Bounds Tables.

Security. For security evaluation, we exploited the infamous Heartbleed bug [3, 11]. In a nutshell, Heartbleed is triggered when a maliciously crafted TLS heartbeat message is received by the server. The server does not sanity-check the length-of-payload parameter in the message header, thus allowing memcpy to copy the process memory’s contents in the reply message. In this way, the attacker can read confidential memory contents.

AddressSanitizer and GCC-MPX detect Heartbleed10.

5.2 Nginx Web Server

We tested Nginx version 1.4.0—the last version with a stack buffer overflow vulnerability [10]. Nginx was configured with the “autodetected” number of worker processes to load all cores and was benchmarked against the same ab benchmark as Apache. ab was also used as a client.

To successfully run Nginx under GCC-MPX with narrowing of bounds, we had to manually fix a variable-

|                | Apache | Nginx | Memcached |
|----------------|--------|-------|-----------|
| Native         | 9.4    | 4.3   | 73        |
| MPX            | 120    | 18    | 352       |
| ASan           | 33     | 380   | 95        |

Table 7: Memory usage (MB) for peak throughput. (GCC-MPX and ICC-MPX showed identical results.)

9https://software.intel.com/en-us/forums/intel-c-compiler/topic/700550

10The actual situation with Heartbleed is more contrived. OpenSSL uses its own memory manager which partially bypasses the wrappers around malloc and mmap. Thus, in reality memory-safety approaches find Heartbleed only if the length parameter is greater than 32KB (the granularity at which OpenSSL allocates chunks of memory for its internal allocator) [6].
length array name[1] in the ngx_hash_elt_t struct to name[0]. However, ICC-MPX with narrowing of bounds still refused to run correctly, crashing with a false positive in ngx_http_merge_locations function. In a nutshell, the reason for this bug was a cast from a smaller type, which rendered the bounds too narrow for the new, larger type. Note that GCC-MPX did not experience the same problem because it enforces the first struct’s field to inherit the bounds of the whole object by default—in contrast to ICC-MPX which takes a more rigorous stance. For the following evaluation, we used the version of ICC-MPX with narrowing of bounds disabled.

**Performance.** With regards to performance (Figure 20b), Nginx has a similar behavior to Apache. AddressSanitizer reaches 95% of native throughput, while GCC-MPX and ICC-MPX lag behind with 86% and 89.5% respectively. Similar to Apache, this experiment was network-bound, with CPU usage of 225% for native, 265% for Intel MPX, and 300% for AddressSanitizer. (CPU usage numbers prove that HW-assisted approaches impose less CPU overheads.)

As a side note, Nginx has predictable behavior only under GCC. Native ICC version reaches only 85% of the GCC’s throughput, and native Clang only 90%. Even more surprising, the ICC-MPX version performed 5% better than native ICC; similarly, the AddressSanitizer-Clang version was 10% better than native Clang. We are still investigating the reasons for this unexpected behavior.

As for memory consumption (Table 7), the situation is opposite as with Apache: Intel MPX variants have a reasonable $4.2 \times$ memory overhead, but AddressSanitizer eats up $88 \times$ more memory (it also has $625 \times$ more page faults and $13\%$ more LLC cache misses). But then why Intel MPX is slower than AddressSanitizer if their memory characteristics indicate otherwise? The reason for the horrifying AddressSanitizer numbers is its “quarantine” feature—AddressSanitizer employs a special memory management system which avoids re-allocating the same memory region for new objects, thus decreasing the probability of temporal bugs such as use-after-free. Instead, AddressSanitizer marks the used memory as “poisoned” and requests new memory chunks from the OS (this explains huge number of page faults). Since native Nginx recycles the same memory over and over again for the incoming requests, AddressSanitizer experiences huge memory blow-up. When we disabled the quarantine feature, AddressSanitizer used only 24MB of memory.

Note that this quarantine problem does not affect performance. Firstly, Nginx is network-bound and has enough spare resources to hide this issue. Secondly, the rather large overhead of allocating new memory hides the overhead of requesting new chunks from the OS.

**Security.** To evaluate security, the bug under test was a stack buffer overflow CVE-2013-2028 that can be used to launch a ROP attack [2]. Here, a maliciously crafted HTTP request forces Nginx to erroneously recognize a signed integer as unsigned. Later, a recv function is called with the overflown size argument and the bug is triggered.

Perhaps surprisingly, AddressSanitizer detects this bug, but both versions of Intel MPX do not. The root cause is the run-time wrapper library: AddressSanitizer wraps all C library functions including recv, and the wrapper—not the Nginx instrumented code—detects the overflow. In case of both GCC-MPX and ICC-MPX, only the most widely used functions, such as memcpy and strlen, are wrapped and bounds-checked. That is why when recv is called, the overflow happens in the unprotected C library function and goes undetected by Intel MPX.

This highlights the importance of full protection—not only protecting the program’s own code, but also writing wrappers around all unprotected libraries used by the program. Another interesting aspect is that this overflow bug is read-only and cannot be caught by write-only protection. No matter how tempting it may sound to protect only writes, one must remember that buffer-overread vulnera-
abilities will slip away from such low-overhead bounds checking.

5.3 Memcached Caching System

Lastly, we experimented with Memcached version 1.4.15 [22]. This is the last version susceptible to a simple DDoS attack [9]. In all experiments, Memcached was run with 8 threads to fully utilize the server. For the client we used a memaslap benchmark from libmemcached with a default configuration (90% reads of average size 1700B, 10% writes of average size 400B). We increased the load by adapting the concurrency number.

After some vexing debugging experiences with Nginx and Apache, we were pleased to experience no issues instrumenting Memcached with GCC-MPX and ICC-MPX.

Performance. Performance-wise, Memcached turned out to be the worst case for Intel MPX (see Figure 20c). While AddressSanitizer performs on par with the native version, both GCC-MPX and ICC-MPX achieved only 48 – 50% of maximum native throughput.

In case of native and AddressSanitizer, performance of Memcached was limited by network. But it was not the case for Intel MPX: Memcached exercised only 70% of the network bandwidth. The memory usage numbers in Table 7 help understand the bottleneck of Intel MPX. While AddressSanitizer imposed only 30% memory overhead, both Intel MPX variants used 350MB of memory (4.8× more than native). This huge memory overhead broke cache locality and resulted in 5.4× more page faults and 10 – 15% LLC misses, making Intel MPX versions essentially memory-bound. (Indeed, the CPU utilization never exceeded 320%.)

Security. For security evaluation, we used a CVE-2011-4971 vulnerability [9]. In this denial-of-service attack, a specially crafted packet is received by the server and passed to the handler (conn_nread) which tries to copy all packet’s contents into another buffer via the memmove function. However, due to the integer signedness error in the size argument, memmove tries to copy gigabytes of data and quickly segfaults. All approaches—AddressSanitizer, GCC-MPX, and ICC-MPX—detected buffer overflow in the affected function’s arguments and stopped the execution.

6 Lessons Learned

Table 8 summarizes the results of our work. For convenience, we introduce six Intel MPX security levels to highlight the trade-offs between security, usability, and performance.

In general, Intel MPX is a promising technology: it provides the strongest possible security guarantees against spatial errors, it instruments most programs transparently and correctly, its ICC incarnation has moderate overheads of ~50%, it can interoperate with unprotected legacy libraries, and its protection level is easily configurable. However, our evaluation indicates that it is not yet ready for widespread use because of the following issues:

Lesson 1: New instructions are not as fast as expected. First, current Skylake processors perform bounds checking mostly sequentially. Our microbenchmarks indicate this is caused by contention of bounds-checking instructions on one execution port.11 Secondly, loading/storing bounds registers from/to memory involves costly two-level address translation, which can contribute a significant share to the overhead. Together, these two issues lead to tangible runtime overheads of ~50% even with all optimizations applied (in the ICC case).

Lesson 2: The supporting infrastructure is not mature enough. Intel MPX support is available for GCC and ICC compilers. At the compiler level, GCC-MPX has severe performance issues (~150%) whereas ICC-MPX has a number of compiler bugs (such that 10% of programs broke in our evaluation). At the runtime-support level, both GCC and ICC provide only a small subset of function wrappers for the C standard library, thus not detecting bugs in many libc functions.

Lesson 3: Intel MPX provides no temporal protection. Currently, Intel MPX protects only against spatial (out-of-bounds accesses) but not temporal (dangling pointers) errors. All other tested approaches—AddressSanitizer, SoftBound, and SAFECode—guarantee some form of temporal safety. We believe Intel MPX can be enhanced for temporal safety without harming performance, similar to SoftBound.

Lesson 4: Intel MPX does not support multithreading. An MPX-protected multithreaded program can have both false positives (false alarms) and false negatives (missed bugs and undetected attacks). Until this issue is fixed—either at the software or at the hardware level—Intel MPX cannot be considered safe in multithreaded environments. Unfortunately, we do not see a simple fix to this problem that would not affect performance adversely.

Lesson 5: Intel MPX is not compatible with some C idioms. Intel MPX imposes restrictions on allowed memory layout which conflict with several widespread C programming practices, such as intra-structure memory accesses and custom implementation of memory management. This can result in unexpected program crashes and

11We project that, if this functionality would be available on more ports, Intel MPX would be able to use instruction parallelism to a higher extent and the overheads would be lower.
is hard to fix; we were not able to run correctly 8–13% programs (this would require substantial code changes).

In conclusion, we believe that Intel MPX has a potential for becoming the memory protection tool of choice, but currently, AddressSanitizer is the only production-ready option. Even though it provides weaker security guarantees than the other techniques, its current implementation is better in terms of performance and usability. SoftBound and SAFECode are research prototypes and they have issues that restrict their usage in real-world applications (although SoftBound provides higher level of security).

We expect that most identified issues with Intel MPX will be fixed in future versions. Still, support for multithreading and restrictions on memory layout are inherent design limitations of Intel MPX which would require sophisticated solutions, which would in turn negatively affect performance. We hope our work will help practitioners to better understand the benefits and caveats of Intel MPX, and researchers—to concentrate their efforts on those issues still waiting to be solved.

All sources of our experiments can be found in the public repository

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| Level | Description | Detects | RIPE attacks | Unfound bugs | Broken | Perf (×) |
|-------|-------------|---------|--------------|--------------|--------|--------|
| 0     | native program (no protection) | —       | GCC 64 | ICC 34 | GCC 6 | ICC 3 | GCC 0 | ICC 0 | Perf 1.00 |
| 1     | MPX only-writes and no narrowing of bounds | inter-object overwrites | 14 | 14 | 3 | 0 | 0 | Perf 1.29 |
| 2     | MPX no narrowing of bounds | + inter-object overreads | 14 | 14 | 3 | 0 | 2 | 8 | Perf 2.39 |
| 3     | MPX only-writes and narrowing of bounds | all overwrites* | 14 | 0 | 2 | 0 | 4 | 7 | Perf 1.30 |
| 4     | MPX narrowing of bounds (default) | + all overreads* | 14 | 0 | 0 | 0 | 4 | 9 | Perf 2.52 |
| 5     | + fchkp-first-field-has-own-bounds* | + all overreads | 0 | – | 0 | – | 6 | – | Perf 2.52 |
| 6     | + BNDPRESERVE=1 (protect all code) | all overflows | 0 | 0 | 0 | 34 | 29 | – | – | – |
| AddressSanitizer [47] | inter-object overflows | 12 | – | 3 | – | 0 | 1.55 | – | – | – |

* except intra-object overflows through the first field of struct, level 5 removes this limitation (only relevant for GCC version)

Table 8: The summary table with our classification of Intel MPX security levels—from lowest L1 to highest L6—highlights the trade-off between security (number of unprevented RIPE attacks and other Unfound bugs in benchmarks), usability (number of MPX-Broken programs), and performance overhead (average Perf overhead w.r.t. native executions). AddressSanitizer is shown for comparison in the last row.

References

[1] AddressSanitizerIntelMemoryProtectionExtensions. [https://github.com/google/sanitizers/wiki/AddressSanitizerIntelMemoryProtectionExtensions](https://github.com/google/sanitizers/wiki/AddressSanitizerIntelMemoryProtectionExtensions) Accessed: January, 2017.

[2] Analysis of nginx 1.3.9/1.4.0 stack buffer overflow and x64 exploitation (CVE-2013-2028). [http://www.vnsecurity.net/research/2013/05/21/analysis-of-nginx-cve-2013-2028.html](http://www.vnsecurity.net/research/2013/05/21/analysis-of-nginx-cve-2013-2028.html) Accessed: January, 2017.

[3] Anatomy of OpenSSL’s Heartbleed: Just four bytes trigger horror bug. [http://www.theregister.co.uk/2014/04/09/heartbleed_explained/](http://www.theregister.co.uk/2014/04/09/heartbleed_explained/) Accessed: January, 2017.

[4] Apache HTTP server project. [http://httpd.apache.org/](http://httpd.apache.org/) Accessed: January, 2017.

[5] Fex: A Software Systems Evaluator. [https://github.com/tudinfse/fex](https://github.com/tudinfse/fex) Accessed: January, 2017.

[6] Heartbleed vs malloc.conf. [http://www.tedunangst.com/flak/post/heartbleed-vs-mallocconf](http://www.tedunangst.com/flak/post/heartbleed-vs-mallocconf) Accessed: January, 2017.

[7] Intel(R) Memory Protection Extensions Enabling Guide. [https://software.intel.com/en-us/articles/intel-memory-protection-extensions-enabling-guide](https://software.intel.com/en-us/articles/intel-memory-protection-extensions-enabling-guide) Accessed: January, 2017.

[8] Introduction to SPARC M7 and Silicon Secured Memory (SSM). [https://swisdev.oracle.com/_files/What-Is-SSM.html](https://swisdev.oracle.com/_files/What-Is-SSM.html) Accessed: January, 2017.

[9] Memcached bug: CVE-2011-4971. [http://www.cvedetails.com/cve/cve-2011-4971](http://www.cvedetails.com/cve/cve-2011-4971) Accessed: January, 2017.

[10] nginx: The Architecture of Open Source Applications. [http://www.aosabook.org/en/nginx.html](http://www.aosabook.org/en/nginx.html) Accessed: January, 2017.

[11] The Heartbleed Bug. [http://heartbleed.com/](http://heartbleed.com/) Accessed: January, 2017.

[12] AKRITIDIS, P., COSTA, M., CASTRO, M., AND HAND, S. Baggy Bounds Checking: An efficient and backwards-compatible defense against out-of-bounds errors. In Proceedings of the 18th Conference on USENIX Security Symposium (Sec) (2009).

[13] BERGER, E. D., AND ZORN, B. G. DieHard: Probabilistic memory safety for unsafe languages. In Proceedings of the 27th Conference on Programming Language Design and Implementation (PLDI) (2006).

[14] BIENIA, C., AND LI, K. PARSEC 2.0: A new benchmark suite for chip-multiprocessors. In Proceedings of the 5th Annual Workshop on Modeling, Benchmarking and Simulation (MoBS) (2009).

[15] BLOG, T. T. Tor browser 5.5a4-hardened is released. [https://blog.torproject.org/blog/tor-browser-55a4-hardened-released](https://blog.torproject.org/blog/tor-browser-55a4-hardened-released) Accessed: January, 2017.

[16] CHISNALL, D., ROTHWELL, C., WATSON, R. N., WOODRUFF,
[52] WAGNER, J., KUZNETSOV, V., CANDEA, G., AND KINDER, J. High system-code security with low overhead. In Proceedings of the 2015 Symposium on Security and Privacy (SP) (2015).

[53] WILANDER, J., NIKIFORAKIS, N., YOUNAN, Y., KAMKAR, M., AND JOOSEN, W. RIPE: Runtime intrusion prevention evaluator. In Proceedings of the 27th Annual Computer Security Applications Conference (ACSAC) (2011).

[54] WOODRUFF, J., WATSON, R. N., CHISNALL, D., MOORE, S. W., ANDERSON, J., DAVIS, B., LAURIE, B., NEUMANN, P. G., NORTON, R., AND ROE, M. The CHERI capability model: Revisiting RISC in an age of risk. In Proceeding of the 41st Annual International Symposium on Computer Architecture (ISCA) (2014).

[55] XIE, Y., CHOU, A., AND ENGLER, D. ARCHER: Using Symbolic, Path-sensitive Analysis to Detect Memory Access Errors. ACM SIGSOFT Software Engineering Notes (2003).

[56] YANG, J., CUI, A., STOLFO, S., AND SETHUMADHAVAN, S. Concurrency attacks. In Proceedings of the 4th Conference on Hot Topics in Parallelism (HotPar) (2012).