Scaling Theory of Electrically Doped 2D Transistors

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Abstract—Due to channel thicknesses of atomic dimensions, 2D material transistors exhibit outstanding gate control, and can potentially reach the Boltzmann limit of ln(10) KT/q and also sub-ln(10) KT/q in field-effect transistors (FETs) and tunnel FETs (TFETs) respectively at temperature T. The lack of adequate knowledge of chemical species and doping methods have led to the use of electrical doping by gates as the predominant method for modulating the band profiles in these materials. Electrical doping methods are also preferred in TFETs as chemical doping introduces states in the bandgap which degrade the off-current. It is shown here that the existing scaling theories for chemically doped 3D transistors cannot be applied to the novel class of electrically doped 2D transistors. Hence, a novel scaling theory is developed to aid device design and performance optimization of 2D transistors. Full band atomic quantum transport simulations help to benchmark the theory and to show that the critical design parameters are the physical oxide thickness and spacing between the gates.

Index Terms—2D FETs, electrical doping, scaling theory.

I. INTRODUCTION

Ultra-thin channels are desired in aggressively scaled field-effect transistors (FETs) and in tunnel FETs (TFETs) for better gate control and higher performance [1]–[3]. The emergence of a novel class of 2D semiconducting materials has enabled the possibility of atomically thin channels in transistors. In addition to achieving almost ideal 2D electrostatics, these materials have high mobility [4], weak interaction with the environment [5], and a technologically relevant bandgap spanning from 0.5 to 2 eV [6], all of which add to their potential as transistors. However, to operate as TFETs, these materials need to be doped appropriately to realize pn junction-like regions with high internal electric fields [7]. TFETs, which are promising low power devices capable of achieving in principle a sub-60 mV/dec sub-threshold swing (SS) at room temperature [8], are specially prone to deleterious effects of chemical doping, as the dopant states in the bandgap increase the off-currents [9]. Hence, electrical doping methods which realizes a pn junction by appropriate gate biases are both promising and the currently dominant doping method in 2D material transistors [10]. Although conventional scaling length theory in chemically doped transistors has been widely successful in elucidating the effect of device design parameters on performance, it is shown here that such a theory fails to explain the behavior of electrically doped 2D material transistors correctly. Consequently, a new scaling theory is developed here backed by atomic transport simulations.

The well-known scaling length theory [10] can be used in conventional transistors to quantify the effect of gate control on the electric field at the junctions [11]. This theory provides a simple analytic way to understand how various device parameters affect the spatial variation of the potential along the channel described by a modified 1D Poisson equation, \( \frac{d^2U}{dx^2} - \frac{U}{\lambda} = 0 \), where U and \( \lambda \) are the electrostatic potential and the natural scaling length of the potential, respectively. The expression for \( \lambda \) depends on the structure of the device [10]. \( \lambda \) has a generic form of \( \sqrt{\frac{\varepsilon_{ch}}{\varepsilon_{ox}} t_{ch} t_{ox}} \), where \( \varepsilon_{ch} \) and \( \varepsilon_{ox} \) are the dielectric constants of channel and oxide respectively, whereas \( t_{ch} \) and \( t_{ox} \) are their thicknesses. \( \beta \) is a factor that depends on the device structure; e.g. in single gated structures \( \beta \) is 1 whereas in gate-all-around structures \( \beta \) equals 1/2 [10].

First, full-band quantum transport simulations are performed on a monolayer 2D transition metal dichalcogenide WSe\(_2\) homojunction TFET in Section III to show the critical design parameters involved in electrical doping. Based on the simulation results, the inadequacies of the original scaling theory are then highlighted, and a new analytical theory is developed in Section IV.

II. SIMULATION DETAILS

The atomistic quantum transport simulations use a sp\(^3\)d\(^5\) 2nd nearest neighbor tight-binding model and a self-consistent Poisson-NEGF (Non-equilibrium Green’s Function) method. The details of the models and the methods can be found in [7]. The simulated monolayer WSe\(_2\) TFET assumes a structure shown in Fig. 1a. Each gate has a length of 13nm, with the gate spacing \( S \) assumed to be zero unless otherwise stated. An electrically doped pn junction can be created in this structure by applying biases of opposite polarity in the two gates. A source-drain voltage \( V_{DS} \) of 1V is used throughout, and the relative dielectric constant and physical oxide thickness are set to 20 and 1.66nm respectively unless mentioned otherwise. The total thickness of the device (the distance between the top and bottom gates shown as \( T_{tot} \) in Fig. 1b) equals 4nm by default, including the body thickness of monolayer WSe\(_2\) (\( \approx 0.67 \text{nm} \)). All of the transport simulations have been performed with the simulation tool NEMO5 [14].

III. SIMULATION RESULTS

Fig. 1d shows the transfer characteristics of an electrically doped TFET. The I-V curve labeled as reference has \( T_{tot} \) of 4nm and \( \epsilon \) of 20. There are two ways to increase equivalent oxide thickness (EOT): 1) reduce \( \epsilon \) or 2) increase the thickness of the oxide. According to the previous scaling theory, these two methods should lead to similar results since they result in the same EOT (substituting \( t_{ox}/\epsilon_{ox} \) with \( EOT/3.9 \)) gives \( \lambda = \sqrt{\varepsilon_{ch} t_{ch} EOT}/3.9 \). However, the numerical results show...
Fig. 1: a) Physical structure of an electrically doped monolayer WSe$_2$ TFET with left and right oxide lengths of 13nm. b) Transfer characteristics of the TFET with $T_{\text{tot}} = 4\text{nm}$ and $\epsilon = 20$ as reference (black line), with $T_{\text{tot}} = 6.7\text{nm}$ and $\epsilon = 20$ (blue triangles), and with $\epsilon = 11$ and $T_{\text{tot}} = 4\text{nm}$ (red circles). c) On-current of the TFET with gate spacing $S$.

It is significant to observe that changing the dielectric constant does not affect the I-V significantly, while increasing the physical thickness of oxide does. This is a critical finding of the new scaling theory that the main scaling parameter is the physical thickness of the oxide. This implies that to obtain better performance in an electrically doped 2D TFET, the physical thickness of the oxide should be reduced, not just EOT.

Fig. 1: shows the effect of gate spacing on the on-current of the WSe$_2$ TFET. Increasing the spacing reduces the on-current significantly, however, this effect is not as large as the effect of increasing the oxide thickness. Numerical simulations therefore identify the physical oxide thickness and the gate spacing as two critical parameters for electrical doping. This is essentially due to the presence of fringing fields from the gates. As long as these fringing fields are strong, the physical thickness of the oxide matters more than the EOT.

**IV. Analytic Modeling**

To find an analytic solution of the device potential due to electrical doping, few assumptions have been made here: 1) there is no spacing distance ($S = 0$) between the gates but the gates are electrically isolated, 2) the thickness of the 2D material is neglected compared to the oxide thickness (or the dielectric constant of the 2D material is close to that of oxide), 3) the length of the device is much larger than its thickness ($L_{C_h} \gg T_{\text{tot}}$), 4) the mobile charge within the tunnel junction is small enough to be neglected in the Poisson equation such that the Laplace equation can be solved instead. Later on, assumption 1) is relaxed by introducing an empirical parameter $\alpha$ in the analytic model that captures the effect of spacing on the scaling length $\lambda$. Assumptions 2) and 3) are justified from the physical structure of 2D material FETs and their sub-nm thicknesses. Assumption 4) is valid if the magnitude of the mobile charge $n$ is much smaller than a critical charge $n_0$, which depends on the magnitude of the second derivatives of the potential close to the tunnel junction, $n_0 \approx \frac{eV_1 - V_2}{q \epsilon^2}$. In a typical case, for $\lambda$ of 1nm, oxide relative dielectric constant $\epsilon$ of 10, and the potential difference between the gates ($V_1 - V_2$) of 1V, $n_0$ is about $5e20\text{cm}^{-3}$. The high value of $n_0$ makes assumption 4 valid for most practical situations including graphene. It is to be noted that the numerical simulations do not make any of these assumptions. Hence, a comparison between the two will justify the analytic model. Considering the above assumptions, the 2D Laplace equation can be solved with the boundary conditions shown in Fig. 2a to obtain the potential profile inside the device.

\[
V(x, y) = \sum_{k=0}^{\infty} A_k \sin \left(\frac{(2k+1)\pi x}{T_{\text{tot}}} \right) e^{\exp \left(-\frac{(2k+1)\pi y}{T_{\text{tot}}} \right)} + C
\]

Since the first term of the series ($k = 0$) in (1) has the largest magnitude and the smallest slope, it is the limiting factor for the magnitude of the electric field. Hence, considering this term only in (1), the potential along the channel ($y = T_{\text{tot}}/2$) is given as,

\[
V(x, T_{\text{tot}}/2) \approx \left\{ \begin{array}{ll}
(V_M - V_1) e^{\exp \left(-\frac{\pi}{T_{\text{tot}}} (x - x_M) \right)} + V_1 & x < x_M \\
(V_M - V_2) e^{\exp \left(-\frac{\pi}{T_{\text{tot}}} (x - x_M) \right)} + V_2 & x > x_M 
\end{array} \right.
\]

where $V_M$ and $x_M$ are the potential and the position of the interface between the gates respectively. Using continuity of the displacement field at $(x, y) = (0, T_{\text{tot}}/2)$, $V_M \approx \frac{eV_1 + eV_2}{\epsilon_1 + \epsilon_2}$, for the general asymmetric gating case shown in Fig. 2b with two different dielectric constants $\epsilon_1$ and $\epsilon_2$ for the p and n junctions. For the case of symmetric gating with $\epsilon_1 = \epsilon_2$, $V_M = (V_1 + V_2)/2$. Comparing the above solution with a conventional scaling theory solution $\exp(-x/\lambda)$, the natural scaling length can be extracted as $\lambda \approx T_{\text{tot}}/\pi$, which shows again that the scaling length depends on the physical oxide thickness, and not on EOT.

Fig. 2b depicts the potential profile along the channel obtained from NEGF simulations and the approximate solution using (2). The analytical potential profile matches the numerical results very well for different physical oxide thicknesses which supports the validity of the new scaling length. Fig. 4: shows the conduction band profile of the pn junction with different asymmetric gating ratios $\epsilon_1/\epsilon_2 = 4, 1$, and 1/4 showing excellent agreement again between the analytic results and NEGF. Notice that reducing or increasing $\epsilon$ of the right gate oxide ($\epsilon_2$) compared to the left ($\epsilon_1$) does not change the electric field significantly.

An empirical factor $\alpha$ can be used to capture the effect of spacing $S$ on the scaling length, as given by

\[
\lambda \approx \frac{T_{\text{tot}} + \alpha S}{\pi}
\]

From atomistic simulation results, $\alpha$ is found to be about 1/4, which implies that $T_{\text{tot}}$ has more impact on the performance of the device if compared to the spacing $S$ (since $\alpha < 1$).

**V. Conclusion**

In this work, a new scaling theory is developed for electrically doped 2D transistors. The predictions of the new theory differ significantly from those of the old scaling theory, and
Fig. 2: a) Domain and boundary conditions of the simplified problem for the purpose of finding an analytic solution, b) The potential profile along the channel obtained from atomistic simulation (red lines) and analytic expressions (blue circles) for different total physical thicknesses of the device and c) various $\epsilon_1/\epsilon_2$ values.

are justified by full band atomistic NEGF simulations. The major players in the performance of electrically doped 2D transistors are found to be the physical thickness of the oxides and the spacing distance between the gates. Among the two, the spacing has less impact by a factor of about 1/4. As a result, it is critical for electrically doped 2D TFETs to reduce the physical thickness of oxide and fabricate the gates as close as possible for high performance applications.

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