A Transformer using two RDL metal layers based on Fan-Out Panel Level Package Technology

Zixu Wang¹, Xulei Niu², Shaopan Lin³, Tingyu Lin⁴ and Guochi Huang¹*

¹College of Photo and Electronic Engineering, Fujian Normal University, Fuzhou City, Fujian Province, 350007, China
²College of Photo and Electronic Engineering, Fujian Normal University, Fuzhou City, Fujian Province, 350007, China
³College of Photo and Electronic Engineering, Fujian Normal University, Fuzhou City, Fujian Province, 350007, China
⁴Guangdong Xinhua Microelectronics Co., Ltd. 2/F Block A Buddha High-tech Think Tank Center Nanhai High-tech Zone, Foshan City, Guangdong Province, 528000, China
¹*Corresponding author’s e-mail: guochi.huang@fjnu.edu.cn

Abstract. Under the background that electronic products have been developing in the direction of being smaller, lighter and cheaper, the packaging of chip components has also been continuously improved. Fan-out panel-level package (FOPLP) is one of the latest development trends in microelectronics package, which can achieve higher productivity and lower costs. A planar toroidal spiral transformer is designed based on Fan-Out Panel Level Package technology. The transformer is constructed by two RDL layers provided by the packaging process. The size of the proposed transformer is 434μm×434μm. The simulated primary and secondary inductance is 2.5nH and 2.5nH respectively. The coupling factor of the transformer is 0.845. The quality factor of the transformer is higher than 800 during the entire working frequency range. The self-resonant frequency of the present transformer is 20 GHz. Compared to the on-chip counterpart, the transformer designed based on Fan-Out Panel Level Package technology can achieve higher coupling factor and quality factor. Therefore, the proposed transformer can save chip size and reduce the cost through avoiding using area hungry passive on chip transformer.

1. Introduction
In the context of the development of electronic products in the direction of smaller, lighter and cheaper, to achieve higher productivity and lower costs, this requires continuous improvement in the package technology of chip components. Flip chip technology is an interconnection method based on small size chips, high I/O density, excellent electrical and thermal performance. The early package technology can only use expensive ceramic substrate package technology. Due to the vast commercial application requirement, a reliable and low-cost flip-chip package technology is needed. This resulted in the redistribution layer (RDL) technology, which was implemented using polymer film materials and AL/Cu metalized wiring. Today,
this kind of RDL technology has been widely used in many advanced package technologies, such as Mini Ball Grid Array (BGA) package and Ultra Chip Scale Package (Ultra CSP). Recently, in order to further increase the packaging efficiency and reduce the cost, Fan-Out Panel Level Package (FOPLP) was developed.

FOPLP package technology is the fastest growing advanced package technology. It has higher annual growth rate and can save costs by increasing the size of package. The package size has always been the concern of the industry and academia. Enlarging the package size can further reduce the cost through increasing the packaging die number [1]. Therefore, the FOPLP can reduce the cost of a single package by increasing the number of packages produced in parallel [2]. Currently, FOPLP is mainly used in mobile terminal products. However, with the development of applications such as 5G, artificial intelligence (AI) and autonomous driving, FOPLP will expand to heterogeneous integration with a size of more than 15*15 mm² [3] by around 2020, and the demand for modularity and high-speed data processing will increase sharply. One of the key points of FOPLP technology is the integration of homogeneous and heterogeneous multi-chips. These chips are integrated in a single package by means of micro-copper redistribution layer connections to achieve higher density redistribution layer and more fine line width/line spacing. The RDL technology used in FOPLP can not only provide high quality inter-chip connection for high frequency signals, but also provide a new method for constructing passive components to replace the lossy passive component on silicon chips.

In this paper, a transformer is designed using RDL metal layers in FOPLP technology. The transformer is designed to work in a frequency band of 10 GHz. In order to further analyze the advantages of off-chip package, this paper designs the same form of on-chip transformer as a comparison. This paper discusses the advantages of FOPLP technology by separately studying off-chip package transformers and on-chip transformers, and studying their physical properties, and provides the necessary basis for the practical application of FOPLP transformers and the application of FOPLP technology to other device package in the future.

2. Methods and Materials
FOPLP technology is still in the developing stage, and there have many solutions available in the commercial area. The FOPLP technology adopted in the design is one of the most popular solutions.

2.1. Methods
The development of fan-out technology from wafer level to panel level is a trend of embedded chip technology. Two redistributed copper layer (RDL) interconnects are used in the FOPLP technology to provide low-cost package solution and high quality inter-chip connection. The FOPLP package solution is shown in Figure 1. The silicon chip faces down and is embeded in the mold compound. Two RDL metal layers are used for interconnection and embedded into modified polyimide (MPI). Vias are also provided for connecting the silicon chips and the two metal layers.

Figure 1. illustration of Fan-Out Panel Level Package solution of transformer
2.2. Materials
As shown in Figure 1, the medium used in fan-out panel-level package is a modified polyimide (MPI) material. As shown in Table 1, the thickness of the MPI and RDL layer materials is 100um and 15um respectively, and their thickness could be well controlled to be accurate enough.

Table 1. The material and thickness of the Fan-Out Panel Level Package technology used in this design

| Material         | Thickness |
|------------------|-----------|
| MPI              | 100um     |
| RDL1             | 15um      |
| RDL2             | 15um      |
| Mold Compound    | 600um     |

3. Spiral Structure Transformer
Transformers are often used for power conversion, voltage and current conversion, and DC isolation. In radio frequency circuits, transformers are mainly used for impedance conversion to complete the impedance matching of the circuit and effectively transmit the maximum gain or power. In some circuit systems, conversion between single-ended and differential signals is required, where a balun (balance to unbalance) is needed. An external balun requires additional cost, and sacrifices from higher signal transmission loss especially at microwave or millimeter-wave frequency. The balun formed by a transformer can be easily integrated into the chip. The use of transformer coupling to reduce the use of transistor stacks to achieve the characteristics of low-voltage operation.

Figure 2 shows the design structure and parameters of the transformer proposed by RDL in the FOPLP technology. In order to better reflect the function of the transformer, the design of this paper adopts a fully differential structure, so the symmetry of the differential port layout is very necessary [4].

3.1. A planar toroidal spiral transformer
The transformer in this paper adopts the structure of interweaving and mutual winding, two identical coils are used for interweaving and mutual winding, as to ensure that the performance is exactly the same when the number of turns of the primary coil and the secondary coil are equal, and can provide perfect 1:1 symmetrical spiral transformer, and this interwoven structure has a medium coupling strength.

3.2. Inductor
The transformer consists of a primary coil and a secondary coil. Each coil is equivalent to an inductance, which is realized with a flat toroidal spiral. Each coil is equivalent to an inductance, which is realized by a toroidal spiral. \( L_p \) and \( L_s \) represent the inductance values of the primary and secondary windings of the transformer respectively. The calculation methods of the inductance and resistance of the spiral structure have been described in [5] and [6]. The most important thing about a spiral inductor is its quality factor (Q). Many useful variants can be obtained through [7], which can potentially increase the Q value, and can also reduce the parasitic capacitance or reduce the lateral size of the inductor. For this reason, this paper adopts the form of staggered coupling to complete this design. The coupling coefficient expression is:

\[
K = \frac{M}{\sqrt{L_p L_s}}
\]  

Where: \( M \) is the mutual inductance between the primary coil and the secondary coil, \( L_p \) is the primary inductance value, \( L_s \) is the secondary inductance value. Generally, in the design of transformers, it is required that the larger \( K \) is the better.
3.3. Transformer structure parameter design

The area of the transformer is directly related to the cost. In order to make the size as small as possible without reducing the performance, and the inner diameter, line distance and line width of the transformer are limited by parameters, it is difficult to directly determine the structural parameters of the transformer, so the simulation method is adopted to determine the parameters.

The inner diameter of the transformer is 60um, the line distance is 1.5um, and the line width is 8um, as shown in Figure 2.

![Figure 2. The structure of the transformer](image)

4. Simulation results

In order to better illustrate the advantages of transformer based on off-chip fan-out panel-level package, the off-chip and on-chip transformers are simulated and analyzed separately.

Figure 3 shows the off-chip transformer model in HFSS. Planar structure spiral transformer, the size of the transformer is 434um×434um. Export the sp file and send it to ADS for simulation. The target operating frequency is 8GHz ~ 12GHz. Figure 4 shows the model of the on-chip transformer in Cadence. The layout adopts the SMIC 0.13um process, which is the same size as the model in HFSS, and the operating frequency is the same. The sp file is also exported and sent to ADS for simulation.

![Figure 3. Transformer model in HFSS](image)
4.1. Quality factor (Q)

Figure 5 shows that the quality factors of the two inductors of the off-chip package transformer are basically the same, and both are above 800, showing a very good quality factor. Figure 6 shows the two inductance quality factors of the on-chip transformer, and the two Q values are basically the same, but far lower than the inductance Q value of the off-chip package.

4.2. Self-inductor (L)

Figure 7 shows the inductance values of the two transformers. It can be seen that the primary and secondary inductance values of the off-chip package and on-chip are basically the same, both are about 2.5nH.

4.3. Coupling coefficient (K)

Figure 8 shows the coupling coefficient (K) of the two transformers. It can be seen that the coupling coefficient of the off-chip package is about 0.845 in the frequency range, and the coupling coefficient of the on-chip is about 0.83.
5. Conclusion
The proposed transformer occupies 434um×434um area in the package, and achieve 2.5nH inductance, 0.845 Q-factor and 800 coupling factor.

Compared to the on-chip transformer with the same size, the transformer designed using Fan-Out Panel Level Package technology can achieve higher coupling factor and quality factor. The proposed transformer can save chip size, thus it can reduce the chip cost. The focus of this paper shows that the use of FOPLP technology can not only reduce the size and cost, but also effectively improve the performance of the transformer. The proposed FOPLP transformer can be widely used in many RF front-end systems, for example, it can be used in series to the output of power amplifier in microwave radar system and serving as a differential to singled-ended signal convertor. This paper only introduces the advantages of transformers under FOPLP technology. In order to further study the advantages of FOPLP technology, the proposed FOPLP technology can be used in the package research of other passive components and compared with on-chip devices.

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