Low-Power Differential SRAM design for SOC Based on the 25-um Technology

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Abstract: In recent, the SOC styles area unit the vast complicated styles in VLSI these SOC styles having important low-power operations problems, to comprehend this we tend to enforced low-power SRAM. However these SRAM Architectures critically affects the entire power of SOC and competitive space. To beat the higher than disadvantages, during this paper, a low-power differential SRAM design is planned. The differential SRAM design stores multiple bits within the same cell, operates at minimum in operation low-tension and space per bit. The differential SRAM design designed supported the 25-um technology using Tanner-EDA Tool.

Index terms: Differential SRAM, Low-power, static random access memory (SRAM).

Introduction
In VLSI Technology SOC styles having vast complexity and in operation on battery power. The SOC application having giant bit sizes with reference to the memory needed to store these bits with low power and high speed/faster access. For this purpose most developer developing steady SRAM Technology related to SOC applications. But this SRAM technology having competitive space and value. The low in operation voltages affects the brink voltage (Vth) of SRAM cell. Within the case of a traditional 6T SRAM cell, a trade-off exists between the scan stability and therefore the write ability, attributable to that, it's terribly difficult to at the same time succeed adequate scan stability and write ability in an exceedingly low-tension region. Several SRAM cell alternatives with a scan port are planned for a low-tension operation. The 10T SRAM\textsuperscript{[3]} cell includes vertical and horizontal WLs, each of which require to be designated to access the storage nodes. Throughout the write operation, each the WLs area unit designated solely within the designated cell. The most disadvantage of the 10T SRAM is that it suffers from an outsized space overhead to accommodate the extra transistors in its design. To beat this drawback average 8T-SRAM [1], [4],[9] introduced however, a difficulty with no write-back theme and it exhibits a competitive space. However, a downside of this 8T SRAM is that it’s scan delay will increase significantly with an outsized variation in Vth, as a result of a trade-off between the scan stability and therefore the scan delay exists.
Differential SRAM design
Fig. 1. shows the design of the differential SRAM style in one block. The differential SRAM[1],[2] stores multiple bits in one block, the minimum in operation voltage and space per little bit of the planned SRAM depend upon the quantity of bits in one block. SRAM includes four cross-coupled electrical converter pairs, pass gate transistors (PGL1~4 and PGR1~4), block mask transistors (MASK1 and MASK2), write access transistors (WR1 and WR2), scan buffers (RD1 and RD2), a head switch (P1), and cross-coupled PMOS’s (P2 and P3).WLs (WL1~4), the block choose signal (BLK), and therefore the scan WL (RWLB) area unit row-based signals, whereas the write WL (WWL), write BLs (WBL and WBLB), and browse BLs (RBL and RBLB) area unit column-based signals. The differential SRAM design operates at full swing native bit line with low-tension operations.

![Diagram of differential SRAM design](image)

Fig. 1. The design of the differential SRAM style in one block.

The differential SRAM Having 3 forms of operation modes. These are

**Hold operation:**
During the hold state BLK forced to VDD the write bit line and native bit lines area unit discharged and browse buffers area unit in off state. The RWLB conjointly control at 0v, to eliminate the RBL outpouring current.
The below table 1 shows the operation modes of differential SRAM block with four bit.

| Signal Name | Hold Operation | Read Operation | Write Operation |
|-------------|----------------|----------------|-----------------|
|             |                | Phase 1        | Phase 2         | Selected | Row selected | Column selected |
| WL1         | 0              | 1              | 1               | 1        | 0            | 0               |
| WL2         | 0              | 1              | 1               | 1        | 0            | 0               |
| WL3         | 0              | 1              | 1               | 1        | 0            | 0               |
| WL4         | 0              | 1              | 1               | 1        | 0            | 0               |
| BLK         | 1              | 0              | 0               | 0        | 0            | 1               |
| RWLB        | 1              | 1              | 0               | 1        | 1            | 1               |
| WBL         | 0              | 0              | 0               | 1        | 0            | 1               |
| WBLB        | 0              | 0              | 0               | 0        | 0            | 0               |
| RBL         | 0              | 1              | 1               | 1        | 1            | 1               |
| RLBL        | 0              | 1              | 0               | 1        | 1            | 1               |
| WWL         | 0              | 0              | 0               | 1        | 0            | 1               |

Table.1. Operation modes of differential SRAM block with four bit.

**Read operation:**
The read operation having once more 2 phases of operation, in section one scan operation is comparable to 8T-SARM scan operation except RWLB. If RWLB is high then scan buffer line isn’t discharged.
The second section starts with the falling of the RWLB. The RWLB permits not solely the discharge of the RBL however conjointly the feedback of cross-coupled PMOS’s. Conjointly BLK control at 0V, and write lines area unit control at VDD. One among the scan buffer line remains at VDD. Regeneration of the cross-coupled PMOS’s will increase the LBL to the worth of the complete VDD then LBL achieved fully swing and gate of RBL is at VDD no would like of boosted WL’s.

**Write operation:** The write operation more divided into 3 types, these are selected block write operation, row selected block write operation and column selected block operation.

**Selected Block:** In selected write operation BLK is at 0V, and WWL is control at VDD then write access transistors area unit ON. Write lines area unit enabled. The write operation is differential.

**Row Selected Block:** This operation is comparable to scan operation except RWLB control at VDD.

**Column Selected Block:** The write lines area unit control at 0V and BLK and WWL area unit high, leading to the consumption of an outsized quantity of static power throughout the write operation. The dc current path within the column half-selected block is eliminated by connecting the sources of the block mask transistors to the WBLs.

**Data flip:** If each the WL and therefore the BLK area unit high, at the same time then knowledge flipping condition is happens.

The fig.2. Shows the various bit sizes of differential SRAM Architectures with 25-um technology with Tanner EDA S-edit Tool.
Bit-Interleaved SRAM style

Many SRAM cell alternatives with a decoupled scan port are planned for a low-tension operation. The advantage of adding a decoupled scan port is that it eliminates the trade-off between the scan stability and therefore the write ability within the SRAM array to that the bit-interleaving[2] isn't applied; therefore, the scan stability and write ability may be optimized severally, facilitating a low-tension operation.
Fig. 3. Selected, half-selected, and unselected cells in an exceedingly bit-interleaved SRAM array.

Fig. 3. shows a bit-interleaved SRAM array design. In an exceedingly bit-interleaved SRAM array, the chosen cells area unit the SRAM cells targeted for the scan or write operation. The row half-selected cells area unit the SRAM cells set on the chosen row and therefore the unselected column, whereas the column half-selected cells area unit the SRAM cells set on the unselected row and therefore the designated column. throughout the write operation, the row half-selected cells area unit disturbed attributable to the choice of the wordline (WL) of the row half-selected cells. Thus, the soundness of the row half-selected cells ought to even be thought of within the SRAM style.

In the bit-interleaved style we have a tendency to exploitation the various bit sized SRAM cells. Looking on the memory size, the bit-interleaved style is enforced. Essentially this system is employed in NXN SRAM array styles to lowering the forward soft errors. Therefore these single bit errors are simply rectify exploitation the error correction codes.

**Simulation results**
Simulation results are performed exploitation Tanner EDA tool in 25-um technology with provide voltage 5v. The differential size SRAM styles are having minimum operative voltages, the cross coupled PMOS at most voltage and RWLB is enabled, once BLK are command at VDD.
then the native bit line is charged with VDD and WL’s are boosting from VSS to VDD then the minimum voltage write operation is going on. The vice versa condition, the cross coupled PMOS charging with low voltages and RWLB is disabled, once BLK is command at VDD forthwith the native bit line is discharged WL’s are discharged then the minimum scan operation is going on. The below results shows the differential SRAM S-Edit style simulation in T-Spice.

![Fig.5. Differential SRAM S-Edit simulation results in T-Spice.](image)

The area of the layout is calculated exploitation the L-Editor, the Layout of the differential SRAM design supported the 25-um technology.

![Fig.6. Layout of the differential SRAM design supported the 25-um technology.](image)
Performance analysis
Comparison table depicts the transistors over a spread of Power provide. It's shown that the planned technique has minimum power, delay and area.

| PARAMETERS | Power | Delay | Area |
|------------|-------|-------|------|
|            | 5Vdd  | 3.3Vdd| 2.5Vdd| 5Vdd | 3.3Vdd| 2.5Vdd|      |
| AVERAGE 8T| 102   | 4.38  | 2.07  | 0.58 | 0.52  | 0.5   | 19x19 |
| SRAM       | nW    | pW    | pW    | ns   | ns    | ns    | um    |
| DIFFERENTIAL SRAM DESIGNS |
| 2BIT CELL  | 0.24  | 0.41  | 64.9  | 0.69 | 0.49  | 0.69  | 15x14.5|
|           | pW    | nW    | pW    | ns   | ns    | ns    | um    |
| 4BIT CELL  | 3.7   | 0.46  | 45.8  | 0.57 | 0.50  | 0.49  | 15x22.5|
|           | pW    | nW    | pW    | ns   | ns    | ns    | um    |
| 8BIT CELL  | 0.25  | 0.21  | 0.21  | 0.53 | 0.49  | 0.45  | 15x43  |
|           | pW    | nW    | nW    | ns   | ns    | ns    | um    |

Conclusion
In the differential SRAM, the tradeoff between the read stability and the read delay is eliminated. A full-swing LBL is achieved using cross-coupled PMOS’s, thus, the gate of the read buffer is driven by a full VDD, while a suppressed WL read assist circuit is applied to enhance read stability.
Consequently, it can be concluded that the differential SRAM based on the 25-um technology exhibits a considerably smaller read delay and consumes less energy with a slightly smaller area than the average-8T SRAM.
Feature scope of this project we will develop the differential SRAM design in to NxN SRAM array with bit-interleaving.

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