3-D Stacking of SiC Integrated Circuit Chips With Gold Wire Bonded Interconnects for Long-Duration High-Temperature Applications

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Abstract—Silicon carbide integrated circuits (SiC ICs) have been demonstrated to operate at high temperatures, such as ~460 °C at the Venus' surface, for two months, and for over a year at 500 °C. At these high temperatures, the SiC integrated circuits and sensors need to be packaged in quite different ways than those below 300 °C. In addition, to integrate more devices into the limited footprint of the high-temperature circuit board, three-dimensional (3-D) packaging is a notable advantage. In this work, 3-D stacking of SiC chips using a gold wirebonding interconnect is investigated. The gold bonding wire is used due to its mechanical robustness and chemical inertness at high temperatures. Triple-stacked SiC chips are bonded to each other and to the gold conduction pads on the alumina substrate with screen-printed gold pastes. The mechanical die shear test, wire pull tests, and interconnect electrical resistance tests are executed and analyzed before and after the 3-D SiC chip packages are subjected to a 600 °C thermal aging process in the air for up to 10 days. This 3-D SiC chip packaging has promise for long-duration high-temperatures (up to 600 °C) applications and may be potential for use for applications such as Venus's surface sensing and telemetry.

Index Terms—3-D packaging, die attach, high temperature, interconnect, integrated circuit bonding, integrated circuit packaging.

I. INTRODUCTION

THE surface of Venus has a high temperature of about 460 °C and high air pressure of around 9.4 megapascal (MPa). The common silicon (Si) based integrated circuits (ICs) are designed to work below 125 °C. To equip Venus’s landers with electronics for sensing, data acquisition, and transmission with a nearby Venus’s relay satellite, silicon carbide (SiC), and gallium nitride (GaN) integrated circuits are currently the most promising ones for working on Venus’ surface, as the devices such as diodes and transistors based on these materials can continue to work at 500 °C [1]. The National Aeronautics and Space Administration (NASA) Glenn Research Center has demonstrated that bare junction-gate field-effect transistor (JFET)-based SiC IC chips with hundreds to a thousand transistors withstood the simulated Venus surface extreme environment for days to months [2], [3]. For SiC ICs to be integrated into Venus’s lander subsystems, they must be packaged to provide electrical interconnection and mechanical/chemical protection from the corrosive sulfuric acid environment. Furthermore, current SiC ICs only have hundreds of up to a thousand transistors, which is far less than the modern Si IC chips with millions to billions of transistors.

To accomplish data collection, storage, computation, and communication tasks on Venus’ surface, a lot of SiC ICs need to be integrated into a ceramic printed circuit board (PCB). To save the precious ceramic PCB footprint, multilayers of SiC ICs can be packaged using 3-D packaging.

The current advanced 3-D packaging is mainly developed for Si and gallium arsenide (GaAs) ICs at temperatures below 300 °C. Its structure and materials are not feasible for high-temperature Venus’s surface applications. Traditional polymer materials heavily used in conventional packaging technologies will be burned to ashes, while traditional solders or adhesives for die attach can either melt or fail at temperatures above 400 °C. High-temperature electronic packaging is maturing. Some high-temperature two-dimensional (2-D) electronics packaging has been under investigation in recent years [4], [5], [6], [7], [8], [9]. The author’s research group at the University of Idaho has done some preliminary wirebonding-based 3-D SiC IC stacking for high-temperature applications such as Venus’s exploration, which was presented at the 2022 IEEE 72nd Electronic Components and Technology Conference (ECTC) [10]. The 3-D packaging materials used for Venus’s surface exploration must withstand high-temperature applications of about 460 °C, high pressure of 9.4 MPa, and the sulfuric acid atmospheric environment.
II. EXPERIMENT PROCESS

This section discusses the process for the triple-layer 3-D SiC IC staking on an alumina ceramic substrate, including ceramic substrate preparation, first-layer SiC die attach, second- and third-layer SiC die attach, and gold wire bonding.

A conceptual schematic of this wirebonding-based 3-D SiC IC packaging is shown in Fig. 1(a). The gold conductor paste is screen printed onto the ceramic substrate. The first layer of SiC IC is die attached to the substrate gold conductors through another layer of gold conductor paste material, followed by a second layer of SiC ICs. More chip layers can be added for a higher density of ICs. Fig. 1(b) and (c) show the material layers at the interface of the chips with Ti/Pt/Au metallization, (c) Material layers at the interface of chips with Ti/Pt metallization. (Not to scale.)

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610M rapid thermal processing (RTP) system. Wafer B2 was annealed at 600 °C for 5 min using the same AccuThermo AW 610M RTP system. The rapid thermal annealing (RTA) process improves the adhesion of Au to Pt and the possible Ohmic contact formation to the SiC substrate. Ohmic contact itself to the SiC was not verified in this work. While Au still was visibly present on B1 after low-temperature RTP annealing, the Au color paled out on B2 after high-temperature annealing, indicating significant intermetal diffusion between Au and Pt because of the high-temperature RTP.

The wafers were then diced into dummy SiC IC chips of three different-sized squares: 0.2 × 0.2, 0.15 × 0.15, and 0.1 × 0.1 using Disco DAD 321 Dicing Saw.

C. Die Attach

Ferro ESL gold cermet conductor 8835 (520C) was screen printed on top of the gold conductor pads, which had been printed on the alumina ceramic substrate as described in Section II-A. This die attach layer was then leveled at room temperature for 8 min. Then, 0.2 × 0.2 (5 × 5 mm) square SiC dummy chips were picked and placed onto the 8835 die attach material. A 4-bar pressure was then applied to the dies to enhance the die attachment.

Following a similar process to that of the first layer, the second layer of dummy chips of 0.15 × 0.15 square was attached to the first layer of dummy chips. The third layer dummy chips of 0.1 × 0.1 square was attached to the second layer.

D. Co-Firing Multilayer Chips

After the die attach process, the 8835 conductors were dried at 125 °C for 12 min, followed by a firing process at 520 °C for 12 min. Some fabricated triple-layer dummy SiC chip stacks are shown in Fig. 3. The chips were diced from Wafer A, Wafer B1, and Wafer B2, respectively. The color difference of the top metals can be clearly seen, with Pt shining white or silver in Fig. 3 (top), interdiffused Pt/Au paled silver (bottom left), and low-temperature RTA Au shining yellow (bottom right).

E. Au Wirebonding

Au bond wire of 1 mil (25 μm) diameter was used as a wirebonding interconnect due to its mechanical and chemical robustness at high temperatures. The wire bonding process was carried out with a K&S 4524AD Multiprocess Auto Step Back Ball Bonder. Fig. 4 shows a 3-D chip stack before and after the wirebonding process. Note that the dark chip color was mainly because of the lab light reflections when the image was taken.

This phenomenon also appears in the other micrographs of the dummy chips in this article.

It is worth noting that the stacked chips from Wafer B2 subject to 600 °C RTP annealing for 5 min showed very poor wirebondability for unknown reasons. Therefore, such chip stacks were not included in the discussion in Section III.

F. Thermal Aging Process

After the preliminary bond wire pull test, electrical resistance test, and die shear test, to be discussed in Section III, the chips were stored in a Fisher Isotemp 750 Programmable Muffle Furnace at 600 °C for 2, 4, 6, 8, and 10 days to evaluate durability at high temperatures. During the thermal aging process, the furnace was filled with lab air. Fig. 5 shows a chip stack with wirebonding after two days (48 h) of the thermal aging process at 600 °C. Scanning electron microscopy (SEM) images are shown in Fig. 6 for a ball (a) and a wedge (b) taken from an FEI/Thermo Scios® dual-beam system, showing the excellent wire bonding quality after 10 days of the thermal aging process at 600 °C.

III. TEST RESULT AND DISCUSSIONS

A. Electric Resistance Test

Daisy chains were formed by interconnecting the SiC IC chips of the four adjacent stacks to evaluate the electrical integrity of the wirebonding after the thermal aging process. Fig. 7 shows the schematics and images of two daisy chains based on Ti/Pt (Wafer A) front surface metallization and Ti/Pt/Au front surface metallization (Wafer B1).

Four-wire electric resistance measurements were carried out using a Siglent SMD 3055 Digital Multimeter before and after the 600 °C thermal aging process for 2, 4, 6, 8, and 10 days. The interconnect includes the gold bonding wires, the surface metallization, and the contact between them. The electric
Fig. 4. Micrographs of 3-D SiC IC chip stacks (a) before and (b) after wirebonding process.

Fig. 5. Micrograph of wirebonded 3-D SiC IC stack with Pt Ohmic contact after 48 h of the thermal aging process at 600 °C.

Fig. 6. (a) SEM images of a bond ball and (b) wedge after 10 days of thermal aging process at 600 °C.

Fig. 8 shows the daisy chain resistance change for Ti/Pt/Au and Ti/Pt based interconnect, respectively. TI/Pt 1 and TI/Pt 2 represents the test result from two slightly different Ti/Pt based interconnects. It can be seen that there is a significant increase in the resistance after two days of the thermal aging process at 600 °C, especially for Ti/Pt/Au metallization, followed by a steady slow decrease, approaching a constant resistance value in the following days. The reduction in the resistance can be attributed to the metal thermal annealing effect [11], [12]. While both types of metallization showed excellent gold wire bondability, Pt-based Ohmic contact offers higher resistance than Au based before the thermal aging process. Still, Pt-based Ohmic contact offers less resistance than Au-based, indicating that the Ti/Pt metallization has a better electrical performance than Ti/Pt/Au for such high-temperature applications, because Au and Pt form an alloy with a higher specific resistance than Pt, e.g., about 35 μΩ-cm for 75Au-25Pt [13] versus 21 μΩ-cm for the sputtered Pt thin film.

B. Au Bond Wire Pull Test

An XYZTEC Condor 70 Wire Pull and Die Shear Tester was used for the destructive bond wire pull test and die shear test. Unlike the nondestructive electrical test, which can be done

resistance test results are shown in Fig. 8. These measurements do not interrogate the SiC devices themselves but only the surface layers that are part of the packaging structures.
as many times as we can, the die shear and wire pull tests are destructive, so the number of tests is limited by the number of samples. In this experiment, 10 days of thermal aging and six electrical tests were done, while six days of thermal aging and four die shear and wire bond pull tests were done based on the available samples.

Both Ti/Pt and Ti/Pt/Au metallization-based 3-D SiC IC chip stacks were wirebonded between the top chip, center (medium) chip, bottom chip, and the gold conduction pads.
on the alumina substrate surface, as illustrated in Fig. 1(a). Using the test condition C: wire pull (single bond) of MIL-STD-883 method 2011.9, the bond wires were destructively pull-tested before the thermal aging process, and after two, four, and six days of the thermal aging process at 600 °C in air. The results are shown in Tables III–X. In these tables, “Bottom-substrate” means the gold bond wire interconnect between the contact pads of the bottom chip and the conduction pads on the ceramic substrate, and “Top-medium” stands for the bond wire interconnect between the contact pads of the top chip and the center (medium) chip, and so on. In general, the bond wires for different types of chips at different stack positions met the MIL-STD-883 2011.9 destructive bond pull test standard, which defines the minimum bond strength of 3 gram force (gF) for gold wires of 25 mil diameter [14]. In this experiment, the most common failure mode is mid-span break, as can be seen in Fig. 9. The average bonding strengths in the pull test are shown in Fig. 10. On average, the gold bond wire shows better bondability to Au metallization than Pt before the thermal aging process (7.0 gF versus 5.3 gF). After two days of the thermal aging process at 600 °C, the destructive pull test forces stabilized at around 4.5 gF, indicating that Pt and Au metallization have a very similar bond quality to gold bond wires for long-duration high-temperature applications.
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Fig. 9. Micrograph for the destructive wire pull test for Ti/Pt metallization-based 3-D SiC IC stacks six days after the thermal aging process.

Fig. 10. Average destructive wire pull test results for Ti/Pt and Ti/Pt/Au metallization-based SiC IC stacks before and after thermal aging process.

Fig. 11. Die shear test after six days of thermal aging at 600 °C, showing the shear tool (top), bottom chip (center), medium chip (left), and top chip (bottom).

C. Die Shear Test

The destructive die shear test was also implemented using the XYZTEC Condor 70 Wire Pull and Die Shear Tester. The die shear test results for Ti/Pt/Au metallization-based SiC IC stacks are listed in Table XI for chips before and after two, four, and six days of the thermal aging process at 600 °C.

For the package before the thermal aging process, as can be seen from Table XI, all layers of the chips meet the minimum destructive force requirement of 2.5 kilogram force (kgF) for chip areas greater than $64 \times 10^{-4}$ inch$^2$ defined by the MIL-STD-833 2019.9 [15]. Many factors affect the destructive shear force, including the thickness and quality of the screen-printed gold paste; the shear test may not be that uniform from sample to sample of the chips and chip stacks. With the limited samples for the destructive die shear test, the trend in the destructive shear force with the thermal aging time in Table XI may not be as apparent as the wire pull tests do, or six days may not be enough to see a steady trend as the wire pull test. Nevertheless, from the table, the excellent reliability of the die attach for the 3-D SiC chip stacks is apparent after six days of the thermal aging process to meet the requirement set by the MIL-STD-833 2011.9, with the most frequent failure mode of “separation of the die from the die attach material” as shown in Fig. 11.

For the 3-D stacks based on the Ti/Pt top metallization, there were some challenges in doing the shear test for the top-medium and medium-bottom chip interfaces, thus only the bottom-substrate interface die shear tests were implemented, and the results are shown in Table XII.

IV. CONCLUSION

In this work, 3-D SiC IC die stacks based on Au wirebonding interconnections were successfully developed and subject to the thermal aging process at 600 °C in air for two, four, six, eight, and 10 days. Two types of metallization were used for possible Ohmic contact metallization: Ti/Pt and Ti/Pt/Au. Daisy chain electrical resistance test shows that the gold bond wire interconnect resistance across the various surface layers
increased after two days of the thermal aging process, but then decreased and flattened in the following days, thanks to the thermal annealing and metal interdiffusion process. It also shows that the surface of the Ti/Pt metallization has better electrical performance than the surface of the Ti/Pt/Au metallization after two days of the thermal aging process, even though it is the opposite before the thermal aging process.

The destructive wire pull test shows Ti/Pt/Au has better wire bondability to the gold wires with higher destructive pull force than Ti/Pt before the thermal aging process. However, the gold wire bondings to Ti/Pt/Au and Ti/Pt metallization both show decreased, stabilized, and similar destructive force after two days of the thermal aging process at 600 °C. The wire pull and die shear tests for the 3-D SiC IC stacks met the MIL-STD-883 2011.9 and 2019.9 standard, respectively. In general, Ti/Pt metallization on the SiC substrate performs better than Ti/Pt/Au for this high-temperature wirebonding-based 3-D SiC IC packaging. This 3-D SiC IC stacking process is promising for long-duration high-temperature (up to 600 °C) applications such as the sensing and telemetry mission of Venus surface exploration.

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REFERENCES

[1] J. Holmes, A. M. Francis, J. Getreu, M. Barlow, A. Abbasi, and H. A. Mantooth, “Extended high-temperature operation of silicon carbide CMOS circuits for Venus surface application,” J. Microelectron. Electron. Packag., vol. 13, no. 4, pp. 143–154, 2016, doi: 10.4071/maps.527.

[2] P. G. Neudeck, R. D. Meredith, L. Chen, D. J. Spry, L. M. Nakley, and G. W. Hunter, “Prolonged silicon carbide integrated circuit operation in Venus surface atmospheric conditions,” AIP Adv., vol. 6, no. 12, Dec. 2016, Art. no. 125119, doi: 10.1063/1.4973429.

[3] P. G. Neudeck et al., “Operational testing of 4H-SiC JFET ICs for 60 days directly exposed to Venus surface atmospheric conditions,” IEEE J. Electron Devices Soc., vol. 7, pp. 100–110, 2019, doi: 10.1109/JEDS.2018.2882693.

[4] A. Nasiri and S. Ang, “Application of alumina-based ceramic paste for high-temperature electronics packaging,” J. Electron. Packag., vol. 143, no. 2, Jun. 2021, doi: 10.1115/1.4049292.

[5] A. Nasiri et al., “High-temperature electronics packaging for simulated Venus condition,” J. Microelectron. Electron. Packag., vol. 17, no. 2, pp. 59–66, Apr. 2020, doi: 10.4071/imaps.115241.

[6] L. Chen et al., “Sixty earth-day test of a prototype Pt/HTCC alumina package in a simulated Venus environment,” J. Microelectron. Electron. Packag., vol. 16, no. 2, pp. 78–83, Apr. 2019, doi: 10.4071/imaps.873073.

[7] L. Chen, P. G. Neudeck, J. Spry, G. M. Beheim, and G. Hunter, “A 96% alumina based packaging system for 500°C tet of SiC integrated circuits,” in Proc. Additional Conf., Device Packag. HITEC CICMT (HITEC), Apr. 2021, pp. 69–75, doi: 10.4071/2380-4491.2021.HITEC.00069.

[8] L. Chen, P. G. Neudeck, D. J. Spry, G. M. Beheim, and G. W. Hunter, “Electrical performance of a high temperature 32-I/O HTCC alumina package,” in Proc. Additional Conf., Device Packag. HITEC CICMT (HITEC), 2016, pp. 66–72, doi: 10.4071/2016-HITEC-66.

[9] L.-Y. Chen, P. G. Neudeck, D. J. Spry, G. M. Beheim, and G. W. Hunter, “Electrical performance of a 32-I/O HTCC alumina package for high-temperature microelectronics,” J. Microelectron. Electron. Packag., vol. 14, no. 1, pp. 11–16, Jan. 2017, doi: 10.4071/imaps.529.

[10] F. Li and S. Raveendran, “Wirebonding based 3-D SiC IC stacks for high temperature applications,” in Proc. IEEE 72nd Electron. Comp. Technol. Conf. (ECTC), May 2022, pp. 2023–2027, doi: 10.1109/ECTC51906.2022.00319.

[11] U. Schmid and H. Seidel, “Effect of high temperature annealing on the electrical performance of titanium/platinum thin films,” Thin Solid Films, vol. 516, no. 6, pp. 898–906, Jan. 2008.

[12] P. Wilfmann and H.-U. Finzel, “The effect of annealing on the electrical resistivity of thin gold films,” Springer Tracts Mod. Phys., vol. 223, pp. 35–52, Apr. 2013, doi: 10.1007/3-540-48490-6.

[13] A. S. Darling, “Gold-platinum alloys,” Platinum Met. Rev., vol. 6, no. 3, pp. 106–111, 1962, doi: 10.1016/j.plm.2007.04.128.

[14] Xyztec. MIL-STD-883 Method 2011.9—Bond Strength (Destructive Bond Pull Test). Accessed: Feb. 19, 2022. [Online]. Available: https://www.xyztec.com/knowledgecenter/guidelines/mil-std-883-method-2011-9-bond-strength-destructive-bond-pull-test/

[15] Xyztec. MIL-STD-883 Method 2019.9—Die Shear Strength. Accessed: Aug. 8, 2022. [Online]. Available: https://www.xyztec.com/knowledgecenter/guidelines/mil-std-883-method-2019-9-die-shear-strength/