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Fan Zhao, Yidian Wang, Weilian Guo, Jia Cong, Clarence Augustine T. H. Tee, Le Song, and Yelong Zheng

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Analysis of the eight parameter variation of the resonant tunneling diode (RTD) in the rapid thermal annealing process with resistance compensation effect

Fan Zhao,1,a) Yidian Wang,2,b) Weilian Guo,2,c) Jia Cong,1,d) Clarence Augustine T. H. Tee,3,e) Le Song,4,f) and Yelong Zheng4,g)

AFFILIATIONS
1 Department of Microelectronics and Solid-State Electronics, School of Electrical and Information Engineering, Tianjin University, Tianjin 300072, China
2 Department of Microelectronics and Solid-State Electronics, School of Microelectronics, Tianjin University, Tianjin 300072, China
3 Department of Electrical Engineering, Faculty of Engineering, University of Malaya, Kuala Lumpur 50603, Malaysia
4 State Key Laboratory of Precision Measuring Technology and Instruments, Tianjin University, Tianjin 300072, China

a)fanhere@tju.edu.cn
b)wangyidian123@126.com
c)wg886688@163.com
d)congj2012@163.com
e)catht@um.edu.my
f)songle@tju.edu.cn
g)Author to whom correspondence should be addressed: zhengyelongby@tju.edu.cn. Tel: +86-1822-233-3873

ABSTRACT
The rapid thermal annealing process is a key technology to control the parameters of the resonant tunneling diode (RTD) and to achieve high performance for the device. In this paper, the rapid thermal annealing process on the planar RTD has been investigated experimentally. In the experiment, the annealing sample chips of different annealed times have been recorded from the annealing equipment and their I–V characteristics have been measured accordingly. From the I–V characteristics, the negative resistance and the series resistance of the RTD can be obtained. Thus, the relationship between these parameters and annealing time can be established. Finally, by analyzing the concept of the resistance compensation effect, this study explains fully and in detail the dependency of the RTD parameter variation on the annealing time.

V_P and V_i are significantly reduced, greatly lowering R_S, which in return also reduces the heat loss of the circuit and the power consumption of the RTD digital circuits as well as the RTD terahertz oscillator. As V_P decreases, negative resistance R_N is increased, and thus, the output power of the RTD terahertz oscillator is increased. These results are very useful in the study of RTD devices and fabrication technology.

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I. INTRODUCTION
The resonant tunneling diode (RTD) is a high speed negative resistance-type nano-device.1–6 Terahertz (THz) electromagnetic radiation is generally composed of electromagnetic waves with frequencies of 100 GHz–10 THz. The wavelengths of THz waves fall between those of light waves and millimeter waves. They are characterized by strong penetration, high security, and good
orientation and can be used extensively in medical and exploration applications. However, a coherent and high-power source operating at room temperature is indispensable in these applications. Terahertz wave sources are classified into optical wave sources and electrical wave sources. Optical THz products are available commercially, but they are expensive and bulky. Resonant tunneling diode (RTD) oscillators are electrical wave sources, which are coherent, solid-state, compact, and high-power sources operating at room temperature. Resonant tunneling diodes (RTDs) are good candidates for electronic THz wave sources from the angle of RTD oscillator fabrication. Kanaya et al. reported a 1.42 THz oscillation with a reduction in the RTD intrinsic delay. The same team reported a 1.55 THz oscillation through optimization of the antenna length. A 1.98 THz RTD oscillator was fabricated with the optimum electrode thickness of 2 μm. In Ref. 10, the authors used a conventional lumped-element equivalent circuit to analyze a RTD oscillator. However, the theoretical analysis showed that the oscillator frequency and RTD size were correlated negatively. By contrast, the device output power and RTD size were correlated positively. Thus, the fabrication of high frequency RTD oscillators remains a challenge.

In addition to the fabrication of resonant tunneling diode terahertz oscillators, the RTD has other applications as a negative resistance device. Artificial intelligence (AI) is currently a research hotspot. In Ref. 19, the proposed systems of differential equations with the piecewise linear approximation of the S-type I–V characteristics could be utilized in analytical and numerical research and development of neural networks, one of the core components of artificial intelligence. The development of neurodynamic models in circuit design is an important task of modern neuroelectronics, in particular, in the field of brain–machine interface. For example, it is applied as an electrical switching (ES), which gives an abrupt, significant, and reversible change in the conductivity of an electric element under the applied electric field or a flowing current, in addition, in current–voltage (I–V) characteristics of the element, which contains areas with negative differential resistance (NDR), created by the positive feedback of current (S-type I–V) or voltage (N-type I–V).

Although the fabrication techniques of the RTD have been researched for a long time, some fabrication technologies, inclusive of very critical ones related to the RTD, have not been researched in depth or systematically. For example, there are some published papers on the RTD, which shows a near vertical straight line representation in the negative region of I–V characteristics. The series resistance $R_S$ of the RTD is very large and its DC negative resistance $R_N$ would approach zero, which would affect the output power of the RTD in the circuits. The purpose of rapid thermal annealing processing for the RTD is to ensure the contact electrode layer AuGeNi and heavily doping layer n'-GaAs in realizing the alloy process in forming an ohmic contact structure with an extremely low resistance, hence the RTD series resistance ($R_S$) can achieve a very low value. However, so far in our literature review, there are neither any convenient or quick methods for measuring the RTD series resistance nor monitoring the annealing process, and thus, the annealed RTD still holds a high value of $R_S$. The structure of the PRTD used in this study and the annealing process detailed will be discussed in Sec. II. The annealing results will be presented in Sec. III. Section IV will investigate the measurement results accordingly.

II. EXPERIMENT

RTD devices include mesa RTD (MRTD) and planar RTD (PRTD). The MRTD is a traditional RTD, which is grown by using Molecular Beam Epitaxy (MBE) or Metal–Organic Chemical Vapor Deposition (MOCVD) processes. The MRTD is a vertical device, and emitter region (E), well, and collector region (C) are located at different levels of the vertical direction. Comparing with the PRTD, the advantage of the MRTD is that it is easier to obtain a larger Peak-to-Valley Current Ratio (PVCR), which translates into better circuit design, while the disadvantage is the difficulty of controlling the actual active area. Furthermore, the difficulty of the reproducibility process hinders its integration on a larger scale. The limitations of the lithography precision and lateral corrosion processes constrain further refinement and miniaturization of the active area. There are other technical issues, such as preparation of side leakage and ohmic contact wiring. In order to solve the shortcomings of the MRTD, the n'-GaAs grown by MBE technology is used as the substrate for the material structure, and self-aligned Boron ion implantation is used as the device isolation for producing the PRTD.

The PRTD chips and the material structure of the PRTD used in this experiment are shown in Fig. 1 and Table I. Boron ion implantation creates electrical isolation. The emitter is located on the top of the device, which is easy to integrate with other devices. The PRTD produced facilitates the hybrid integration of the RTD.
where $R_i$ (valley current) parameters directly from the I–V curve and calculating $R_{ex}$, $R_N$, and $PVCR$ can be done using the following equations:

$$R_s = \frac{V_p - V_i}{I_p} - R_{ex},$$

$$R_N = \frac{V_p - V_v}{I_p - I_v},$$

and CMOS. This integration can be improved via transferring and bonding of electronic and optoelectronic devices to the host substrates, which greatly simplifies the whole process. The sub-well structure is used in the well structure to reduce the effective threshold voltage ($V_t$). The emitter sub-well structure and the collector sub-well structure are used to form a two-dimensional resonant tunneling with the well structure, thus improving the negative resistance $I$–$V$ characteristics and $PVCR$. Spacer and Barrier structures are indicated in the diagram also. The key structures are shown in Table I.

The emitter AuGeNi metal is used to mask the Boron ion implantation. $n^+$-GaAs is used as the substrate for the RTD to avoid the longitudinal current. In addition, the Boron ion injection is terminated to the $n^+$-GaAs substrate. After the back of the substrate is thinned, AuGeNi is sputtered on the back of the substrate as the collector electrode, and on the front of the PRTD as the emitter electrode.

In our experimental study, the annealing temperature is fixed at 380 °C (a constant), while the annealing time changes from zero to 90 s. The measurement of $I$–$V$ characteristics for different annealing times would extract $V_p$ (peak voltage), $V_v$ (valley voltage), $V_t$ (effective threshold voltage), $I_p$ (peak current), and $I_v$ (valley current) parameters directly from the I–V curve and calculating $R_s$, $R_N$, and $PVCR$ can be done using the following equations:

$$PVCR = \frac{I_p}{I_v}. \tag{3}$$

This study has deduced the relationship of the above parameters with the time-varying annealing process. By analyzing these relationships with the concept of the resistance compensation effect of the RTD, we can explain fully the variation of RTD parameters with the time-varying annealing process in detail.

The equipment used for the annealing process is a RTD-500 rapid annealing oven. The equipment has the tungsten halide lamp as a light thermal source with annealing temperature changed rapidly using a designed program. The temperature ($T$)–time ($t$) characteristics of the temperature rising section, constant temperature section, and temperature falling section can be designed by setting the program controller of the annealing equipment. In this study, two chips of $6 \mu m \times 6 \mu m$ PRTD with the GaAs substrate labeled by sample A and sample B, respectively, are taken as sample chips. The annealing condition of 380 °C, 30 s in nitrogen has been chosen for every annealing stage followed by 15 s cooling until reaching the room temperature. In the actual annealing experiment, the cooling time is about 90 s. The $T$–$t$ characteristics are shown in Fig. 2, in which the blue line shows the setting annealing by program and the red line shows the practical operating annealing process. The full experiment is taken per following sequence: After the first annealing stage is finished, while waiting for the chip temperature to fall near room temperature, the annealed chip is taken out from the annealing equipment, using probe to contact with the electrode of the chip, and so on for a total of three times. The $T$–$t$ characteristics are shown in Fig. 2, in which the blue line shows the setting annealing by program and the red line shows the practical operating annealing process. After cleaning with deionized water by supersonic wave and drying by blowing nitrogen, the chip is taken into the annealing equipment, using probe to contact with the electrode and the red line shows the practical operating annealing process.

### Table I. Material structure of the PRTD.

| Layer         | Material       | Thickness (nm) | Doping density ($cm^{-3}$) |
|---------------|----------------|----------------|----------------------------|
| Emitter electrode | AuGeNi         |                |                            |
| Cap           | $n^+$-GaAs   | 500            | $3 \times 10^{18}$        |
| Emitter       | $n^+$-GaAs   | 10             | $1 \times 10^{17}$        |
| Spacer        | GaAs          | 5              | Un-doped                   |
| Sub-well      | In$_{0.1}$Ga$_{0.9}$As | 5              | Un-doped                   |
| Spacer        | GaAs          | 0.5            | Un-doped                   |
| Barrier       | AlAs          | 1.7            | Un-doped                   |
| Well          | In$_{0.1}$Ga$_{0.9}$As | 4              | Un-doped                   |
| Barier        | AlAs          | 1.7            | Un-doped                   |
| Sub-well      | In$_{0.1}$Ga$_{0.9}$As | 5              | Un-doped                   |
| Spacer        | GaAs          | 5              | Un-doped                   |
| Collector     | $n^+$-GaAs   | 10             | $1 \times 10^{17}$        |
| Substrate     | $n^+$-GaAs   | 1000           | $3 \times 10^{18}$        |
| Collector electrode | AuGeNi       |                |                            |
III. EXPERIMENTAL RESULTS

Figure 3 shows I–V characteristics of sample A of the annealed chips. Table II shows the parameters of the sample A chip extracted from Fig. 3. \( R_S \) is calculated by Eq. (1) as \( R_{ex} = 0 \).

The first annealing is a non-pulsed standard annealing. When the number of pulses is reasonable, the experimental results show that the pulsed T-profile annealing is more beneficial to the performance optimization of the device than the non-pulsed standard annealing.

Figure 4 shows the I–V characteristics of the annealed sample B chip. Table III shows the parameters of the sample B chip extracted from Fig. 4.

IV. DISCUSSION

Taking the eight parameters of the PRTD listed in Tables II and III as the Y-axis and taking the annealed times as the X-axis, we can draw the curves of eight parameters as functions of annealing times of the stage or the total annealing time, as shown in Figs. 5 and 6.

From Tables II and III and Figs. 5 and 6, we can summarize the following results for discussion.

A. \( I_P, I_V, \) and \( PVCR \) are near constant in all of the annealing processes

Besides the slight increase of \( I_P \) in the first annealing, \( I_P, I_V, \) and \( PVCR \) are near constant in all of the annealing processes. From Refs. 46 and 48, \( I_P \) and \( I_V \) are determined by intrinsic negative resistance characteristics due to the resonant tunneling effect. In addition, from Ref. 44, we also find that \( I_P \) and \( I_V \) hold as a constant when \( R_S \) changes. \( I_P \) and \( I_V \) are near constant as the energy band or the material structure of the RTD (including the width of the potential barrier and well, and the doping density of the emitter and collector layer) is not changed. In our experiment, the annealing temperature of 380 °C cannot make any changes on the material structure of the PRTD, so \( I_P \) and \( I_V \) are near constant. Since \( PVCR = I_P/I_V, PVCR \) is also a constant.

B. Over-annealing, \( R_S \) decreases and \( |R_N| \) increases as annealing time increases

For a different chip, the situation of decreasing \( R_S \) is different. For the sample A chip, \( R_S \) maintains a decreasing trend until over-annealing to present an apparent positive resistance (APR) phenomenon and until reaching positive resistance \( R_{APP} \). However, for the sample B chip, \( R_S \) falls to the saturated value of 141 Ω for the first annealing, and still holds this saturated value near a constant until over-annealing, then \( R_S \) starts to increase. The explanation of decreasing \( R_S \) with annealing time is that at 380 °C, the Ge atom of AuGeNi will diffuse into the n⁺-GaAs layer more deeply with increasing annealing time, this effect will increase the donor impurity density in the n⁺-GaAs layer, so the ohmic contact resistance and \( R_S \) will decrease.

In Figs. 5 or 6, \( |R_N| \) increases with increasing annealing time and shows a change in an opposite trend with \( R_S \). Since from Ref. 44, for

| TABLE II. RTD parameters from the annealing experimental results of the sample A chip. |
|-----------------------------------------------|
| **Annealing stage** | **\( V_P \) (V)** | **\( V_V \) (V)** | **\( V_1 \) (V)** | **\( I_P \) (mA)** | **\( I_V \) (mA)** | **PVCR** | **\( R_S \) (Ω)** | **\( R_N \) (Ω)** |
| Not annealing | 1.75 | 1.77 | 0.90 | 3.70 | 1.40 | 2.64 | −8.69 | 230 |
| First annealing stage | 1.08 | 1.10 | 0.30 | 3.90 | 1.40 | 2.78 | −8.1 | 200 |
| Second annealing stage | 0.96 | 1.10 | 0.25 | 3.90 | 1.40 | 2.78 | −56.0 | 182 |
| Third annealing stage | 0.80 | 1.05 | 0.25 | 3.90 | 1.40 | 2.78 | −100 | 141 |
| Over-annealing | 1.20 | 1.13 | 0.20 | 4.00 | 1.40 | 2.86 | 26.9 | 250 |
TABLE III. RTD parameters from annealing experimental results of the sample B chip.

| Annealing stage     | $V_P$ (V) | $V_V$ (V) | $I_V$ (mA) | $I_P$ (mA) | PVCR | $R_N$ (Ω) | $R_S$ (Ω) |
|---------------------|-----------|-----------|------------|------------|------|----------|----------|
| Not annealing       | 2.10      | 2.15      | 1.25       | 3.10       | 1.10 | 2.82     | −25      | 274      |
| First annealing stage | 0.95      | 1.10      | 0.50       | 3.20       | 1.20 | 2.82     | −75      | 141      |
| Second annealing stage | 0.75      | 1.00      | 0.30       | 3.20       | 1.20 | 2.82     | −125     | 141      |
| Third annealing stage | 0.75      | 1.00      | 0.30       | 3.20       | 1.20 | 2.82     | −125     | 140      |
| Over-annealing      | 0.80      | 1.00      | 0.24       | 3.20       | 1.20 | 2.82     | −100     | 175      |

As PRTD chips are annealed and contact resistance $R_C$ decreases with annealing time, from Eq. (6), $V_i$ will surely decrease.

D. Over-annealing phenomenon

The so-called over-annealing means that under more severe annealing conditions (such as over-high annealing temperature or over-long annealing time), the performances of annealed chips are deteriorated by the annealing process.

After over-annealing, $R_S$ of the sample B chip increases in the medium level from 140 Ω to 175 Ω, $V_P$ also increases a little from 0.78 V to 0.80 V, and $|R_N|$ decreases from 125 Ω to 100 Ω.
This is a phenomenon of primary over-annealing. It indicates that the effect of annealing begins to run toward the opposite direction. \( R_s \) of sample A increased obviously from 141 \( \Omega \) to 250 \( \Omega \). From Ref. 50, when \( R_s \) increases as large as to make \( R_{\text{NNRT}} < R_s \), the remainder of \( R_s \) compensation with \( R_{\text{NNRT}} \) is positive resistance \( R_{\text{APP}} \). The APR\(^{19} \) effect will happen. The experimental results on the over-annealing effect on both chips completely demonstrate the process of generation of APR by the fact of \( R_s \) from \(-100 \Omega\) hanging to \( R_{\text{APP}} = 26.9 \Omega \) (for sample A) as well as presenting the I–V characteristics of \( V_P > V_V \) [see Fig. 3(e)]. At present, the concrete physical mechanism of over-annealing is yet to be determined and further work would be carried out. It may be related to non-uniform over-heating or slight oxidation of contact metal (could be due to the introduction of impurity to the nitrogen used). We yet to set up a gas monitoring equipment for measuring the oxygen content and distribution in the annealing equipment. Further study is required at a later stage for this work. Figure 7 shows the PRTD surface after over-annealing with some impurities and craze.

V. CONCLUSIONS

In this paper, based on the measurement of negative resistance parameters from the I–V curve of the PRTD with different annealing times, the variations of eight parameters as a function of annealing time have been studied and analyzed in detail with full explanations using the variation of eight parameters with annealing time and using the concept of the resistance compensation effect of the RTD device. \( I_P, I_V, \) and \( PVCR \) are near constant in all of the annealing processes. \( V_P \) and \( V_V \) are significantly reduced, greatly reducing \( R_s \), which will reduce the heat loss of the circuit and the power consumption of the RTD digital circuits and RTD terahertz oscillator. As \( V_V \) decreases, negative resistance \( R_N \) increases, increasing the output power of the RTD terahertz oscillator. The annealing condition for the PRTD is more severe than that of the MRTD. In actual fact, the experimental results of the rapid thermal annealing process that takes on the PRTD are very similar to those of the MRTD, i.e., the work is suitable for both types of RTD devices. The work done here is of great significance and novelty to the study and further understanding of the RTD fabrication technology.

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REFERENCES

1. R. Izumi, S. Suzuki, and M. Asada, “1.98 THz resonant-tunneling-diode oscillator with reduced conduction loss by thick antenna electrode,” in IEEE 2017 42nd International Conference on Infrared, Millimeter, and Terahertz Waves (IRMMW-THz) (IEEE, 2017), pp. 1–2.
2. H. Kanaya, R. Sogabe, T. Maekawa, S. Suzuki, and M. Asada, “Fundamental oscillation up to 1.42 THz in resonant tunneling diodes by optimized collector spacer thickness,” J. Infrared, Millimeter, Terahertz Waves 35(5), 425–431 (2014).
3. E. Bagci, M. McGrath, C. Barthelmes, S. Dean, and U. Roedig, “Resonant-tunneling diodes as PUF building blocks,” IEEE Trans. Emerging Top. Comput. (published online 2019).
4. E. Wasige, K. H. Alharbi, A. Alkaladi, J. Wang, A. Khalid, G. C. Rodrigues, and J. Figueiredo, “Resonant tunneling diode terahertz sources for broadband wireless communications,” Proc SPIE 10103, 101031J (2017).
5. D. Pandey, L. Bellentani, M. Villani, G. Albareda, P. Bordone, A. Bertoni, and X. Oriols, “A proposal for evading the measurement uncertainty in classical and quantum computing: Application to a resonant tunneling diode and a mach-zehnder interferometer,” Appl. Sci. 9(11), 2300 (2019).
6. F. Zhao, C. Zhu, W. Guo, J. Cong, C. A. T. H. Tee, L. Song, and Y. Zheng, “Resonant tunneling diode (RTD) terahertz active transmission line oscillator with graphene-plasma wave and two graphene antennas,” Electronics 8, 1164 (2019).
7. N. Oshima, K. Hashimoto, D. Horikawa, S. Suzuki, and M. Asada, “Wireless data transmission of 30 Gbps at a 500-GHz range using resonant-tunneling-diode terahertz oscillator,” in 2016 IEEE MTTS-S International Microwave Symposium (IMS) (IEEE, 2016).
8. C. Zhu, L. Mao, F. Zhao, X. Mao, and W. Guo, “Photo-Controlled Terahertz Amplified Modulator via Plasma Wave Excitation in ORTD-Gated HEMTs,” IEEE Photonics J. 9(5), 1–8 (2017).
9. T. Maekawa, H. Kanaya, S. Suzuki, and M. Asada, “Frequency increase in terahertz oscillation of resonant tunnel junction diode up to 1.55 THz by reduced slot-antenna length,” Electron. Lett. 50(17), 1214–1216 (2014).
10. N. Orihashi, S. Hattori, S. Suzuki, and M. Asada, “Experimental and theoretical characteristics of sub-terahertz and terahertz oscillations of resonant tunneling diodes integrated with slot antennas,” Jpn. J. Appl. Phys., Part 1 44(11), 7809–7815 (2005).
11. C. C. Yang, “Influence of parasitic effects in negative differential resistance characteristics of resonant tunneling,” Electronics 8, 673 (2019).
12. V. Ulansky, A. Raza, and H. Oun, “Electronic circuit with controllable negative differential resistance and its applications,” Electronics 8(4), 409 (2019).
13. J. Cong, L. Mao, S. Xie, F. Zhao, D. Yan, and W. Guo, “Photoelectric dual control negative differential resistance device fabricated by standard CMOS process,” IEEE Photonics 1 113(1), 1 (2019).
14. A. Elmishali, R. Stern, and M. Kalech, “An artificial intelligence paradigm for troubleshooting software bugs,” Eng. Appl. Artif. Intell. 69, 147–156 (2018).
15. D. Sayfuddin, “Control of fixed-wing UAV at levelling phase using artificial intelligence,” IOP Conf. Ser.: Mater. Sci. Eng. 327(2), 022092 (2019).
16. S. Gielen, “Natural intelligence and artificial intelligence: Bridging the gap between neurons and neuro-imaging to understand intelligent behaviour,” in Challenges for Computational Intelligence (Springer-Verlag, Berlin, Heidelberg, 2007), pp. 145–161.
17. S. Hu, Y. Liu, H. Li, T. Chen, Q. Yu, and L. Deng, “A MoS\(_2\)-based coplanar neuron transistor for logic applications,” Nanotechnology 28(21), 214001 (2017).
18. A. P. Alivisatos, M. Chun, G. M. Church, R. J. Greenspan, M. L. Roukes, and R. Yuste, “The brain activity map project and the challenge of functional connectomics,” Neuron 74(6), 970–974 (2012).
19. A. V. Petr Boriskov, “Switch elements with S-shaped current-voltage characteristic in models of neural oscillators,” Electronics 8, 922 (2019).
20. P. Bachiller-Burgos, L. J. Manso, and P. Bustos, “A spiking neural model of HT3D for corner detection,” Front. Comput. Neurosci. 12, 37 (2018).
21. A. Velichko, M. Belyaev, and P. Boriskov, “A model of an oscillatory neural network with multilevel neurons for pattern recognition and computing,” Electronics 8(1), 75 (2019).
22. M. Itoh and L. O. Chua, “Star cellular neural networks for associative and dynamic memories,” Int. J. Bifurcation Chaos 14(5), 1725–1772 (2004).
23. T. Roska and L. O. Chua, “The CNN universal machine: An analogic array computer,” IEEE Trans. Circuits Syst. II: Analog Digital Signal Process. 40(3), 163–173 (1993).
24. A. Velichko, “A method for evaluating chimeric synchronization of coupled oscillators and its application for creating a neural network information converter,” Electronics 8, 756 (2019).
25. D. S. Liang, K. J. Gan, and K. Y. Chun, “Frequency divider design using the A-type negative differential-resistance circuit,” in IEEE International Midwest Symposium on Circuits and Systems (IEEE, 2010).
26. N. A. Bogoslovsky, “Physics of switching and memory effects in chalcogenide glasy semiconductors,” semiconductors 46(5), 559–590 (2012).
27. G. Wehner, T. Yabuki, C. Monachon, J. Wu, and C. Dames, “Thermal diodes, regulators, and switches: Physical mechanisms and potential applications,” Appl. Phys. Rev. 4(4), 041304 (2017).
28. J. Alibart and D. B. Strukov, “Utilizing NDR effect to reduce switching threshold variations in memristive devices,” Appl. Phys. A 111(1), 199–202 (2013).
29. M. Asada, S. Suzuki, and N. Kishimoto, “Resonant tunneling diodes for subterahertz and terahertz oscillators,” Jpn. J. Appl. Phys. Part 1 47(6), 4375 (2008).
30. M. Feiginov, C. Sydlo, O. Cojocari, and P. Meissner, “Resonant-tunnelling-diode oscillators operating at frequencies above 1.1 THz,” Appl. Phys. Lett. 99(23), 233506 (2011).
31. W. D. Zhang, E. R. Brown, T. A. Growden, P. R. Berger, and R. Droopad, “A nonlinear circuit simulation of switching process in resonant-tunneling diodes,” IEEE Trans. Electron Devices 63(12), 4993–4997 (2016).
32. A. G. Deppe, N. Holonyak, D. W. Nam, C. K. Haieh, G. S. Jackson, R. J. Matyi, H. Shichijo, J. E. Epler, and H. F. Chung, “Room-temperature continuous operation of p-n Al,Ga,As–GaAs quantum well heterostructure lasers grown on Si,” Appl. Phys. Lett. 51(9), 637–639 (1987).
33. J. Ortega-Gallegos, L. E. Guevara-Macias, A. D. Ariza-Flores, R. Castro-Garcia, L. F. Lastras-Martinez, R. E. Balderas-Navarro, R. E. Lopez-Estopier, and A. Lastras-Martinez, “On the origin of reflectance-anisotropy oscillations during GaAs (001) homoepitaxy,” Appl. Surf. Sci. 439, 963–967 (2018).
34. J. Benyahia, L. Kubiszyn, K. Michalczewski, I. Bogusiak, A. Keblovski, P. Martyniuk, J. Piotrowski, and A. Rogalski, “Electrical properties of midwave and longwave InAs/GaSb superlattices grown on GaAs substrates by molecular beam epitaxy,” Nanoscale Res. Lett. 13, 196 (2018).
35. S. Kotzea, W. Witte, B.-J. Godejohann, M. Marx, M. Heukten, H. Kalisch, R. Aidam, and V. Koros, “Comparison of MOCVD and MBE regrowth for CAVET fabrication,” Electronics 8(4), 377 (2019).
36. H. Shichijo, J. E. Epler, and H. F. Chung, “Room-temperature continuous operation of p-n Al,Ga,As–GaAs quantum well heterostructure lasers grown on Si,” Appl. Phys. Lett. 51(9), 637–639 (1987).
37. J. Ortega-Gallegos, L. E. Guevara-Macias, A. D. Ariza-Flores, R. Castro-Garcia, L. F. Lastras-Martinez, R. E. Balderas-Navarro, R. E. Lopez-Estopier, and A. Lastras-Martinez, “On the origin of reflectance-anisotropy oscillations during GaAs (001) homoepitaxy,” Appl. Surf. Sci. 439, 963–967 (2018).
38. J. V. Dhawan, J. E. Kim, H. Y. Park, K. S. Park, K. Y. Lim, and H. J. Lee, “Clustering effect and residual stress in As/GaAs strained layer grown by metal-organic chemical-vapor deposition,” Phys. Rev. B 51(12), 7894–7897 (1995).
39. K. N. Kuznia, J. W. Yang, Q. C. Chen, S. Krishnankutty, M. A. Khan, T. George, and J. Frietas, Jr., “Low pressure metalorganic chemical-vapor deposition of cubic GaN over (100) GaAs substrates,” Appl. Phys. Lett. 65(19), 2407–2409 (1994).
40. P. V. Seredin, A. S. Lenshin, A. V. Fedyukin, I. N. Arsentyev, A. V. Zhabotinsky, D. N. Nikolaev, L. Leiste, and M. Rinke, “Influence of substrate misorientation on the composition and the structural and photoluminescence properties of epilayer layers grown on GaAs(100),” semiconductors 52(1), 112–117 (2018).
41. S. Hoang Huynh, M. T. H. Ha, H. Binh Do, T. A. Nguyen, H. W. Yu, Q. H. Luc, and E. Y. Chang, “Growth of high-quality In0.13Ga0.87As/AlSb/GaSb/GaAs heterostructure by metalorganic chemical vapor deposition for single-channel Sb-based complementary metal-oxide-semiconductor applications,” Appl. Phys. Express 10(7), 075505 (2017).
42. J. Guo, G. Li, F. Faria, Y. Gao, R. Wang, J. Verma, X. Gao, S. Guo, E. Beam, A. Ketterson, M. Schuette, P. Saunier, M. Wisstey, D. Jena, and H. Xing, “MBE-regrown ohmics in InAlN HEMTs with a regrowth interface resistance of 0.05 Ω mm,” IEEE Electron Device Lett. 33(4), 525–527 (2012).
43. J. I. Bergman, J. Chang, Y. Joo, and B. Matinpour, “RTD/CMOS nanoelectronic circuits: Thin-film InP-based resonant tunneling diodes integrated with CMOS circuits,” IEEE Electron Device Lett. 32(3), 119–122 (2009).
44. Y. Zheng and C. Huang, “Reconfigurable RTD-based circuit elements of complete logic functionality,” in Asia and South Pacific Design Automation Conference, 2008.
45. M. Egard, M. Arlelid, L. Ohlsson, B. M. Borg, E. Lind, and L. E. Wernersson, “In0.53Ga0.47As/Al0.53Ga0.47As RTD-MOSFET multistage wavelet generator,” IEEE Electron Device Lett. 34(7), 970–972 (2012).
46. M. J. Deen, “Simple method to determine series resistance and its temperature dependence in AlAs/GaAs/AlGaAs double barrier resonant tunneling diodes,” Electron. Lett. 28(13), 1195–1197 (1992).
47. L. A. Yang, L. Yue, W. Ying, S. Xu, and H. Yue, “Asymmetric quantum-well structures for AlGaN/AlGaN/GaN resonant tunneling diodes,” J. Appl. Phys. 119(16), 164501 (2016).
48. X. Li, J. Jin, W. L. Guo, L. H. Mao, H. T. Li, and F. Zhao, “Study of relationship between resistance parameters in resonant tunneling diode,” J. Nanoelectron. Optoelectron. 11(4), 430–434 (2016).
49. H. J. Ueng, V. R. Kolagunta, D. B. Janes, K. J. Webb, and M. R. Melloch, “Annealing stability and device application of nonalloyed ohmic contacts using a low temperature grown GaAs cap on thin n+ GaAs layers,” Appl. Phys. Lett. 71(17), 2496–2498 (1997).
50. W. Guo, H. Liang, R. Song, S. Zhang, L. Mao, L. Hu, J. Li, H. Qi, Z. Feng, and G. Tian, “Design and fabrication of gate-type resonant tunneling transistors,” Chin. J. Semiconductors 33(2), 227–233 (2006).
51. C. Miao, W. Guo, P. J. Niu, H. Liu, H. Q. Li, Q. Dan, and X. Zhe, “Apparent positive resistance and temperature effect on I-V characteristics of RTD,” Proc. SPIE 5276, 1–6 (2004).
52. S. Suzuki, M. Asada, A. Teranishi, H. Sugiyama, and H. Yokoyama, “Fundamental oscillation of resonant tunneling diodes above 1 THz at room temperature,” Appl. Phys. Lett. 97(24), 242102 (2010).