An Efficient Methodology to Identify Missing Tags in Large-Scale RFID Systems

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Abstract—Radio frequency identification (RFID) has been widely used with broad applications. One such application is to use RFID to track inventory in warehouses and retail stores. In this application, timely identifying the missing items is an ongoing engineering problem. A feasible solution to this problem is to map each tag to a time slot and verify the presence of a tag by comparing the status of the predicted time slot and the actual time slot. However, existing works are time inefficient because they only verify tags one by one in singleton slots but ignore the collision slots mapped by multiple tags. To accelerate the identification process, we use bit tracking to verify tags in collision slots and design two protocols accordingly. We first propose the Sequential String based Missing Tag Identification (SSMTI) protocol, which converts all time slots to collision slots and enables tags in each slot to reply to a designated string simultaneously. By using bit tracking to decode the combined string, the reader can verify multiple tags together. To improve the performance of SSMTI when most tags are missing, we further propose the Interactive String based Missing Tag Identification (ISMTI) protocol. ISMTI improves the strategies of designing strings for each collided tag so that the reader can verify more tags using shorter strings than SSMTI. Besides, ISMTI can dynamically adjust the verification mechanism according to the proportion of missing tags to maintain time efficiency. We also provide theoretical analysis for proposed protocols to minimize execution time and evaluate their performance through extensive simulations. Compared with state-of-the-art solutions, the proposed SSMTI and ISMTI can reduce the time cost by as much as 39.74% and 68.87%.

Index Terms—RFID, missing tag identification, bit tracking, time efficiency.

I. INTRODUCTION

Radio frequency identification (RFID), as a compelling technology in the Internet of Things, is widely used in various applications, such as supply chain management [1], [2], inventory control [3], [4], and localization [5], [6]. In these applications, RFID can realize automated inventory management with its significant advantages of fast identification, high reliability, and long distance. Specifically, an RFID system consists of at least one reader and multiple tags. Each tag in the system has a unique ID and is attached to a physical object. The RFID reader can collect information such as IDs from tags through wireless communication. Further, by tracking responded tags, the RFID reader can know the presence of corresponding objects.

Fast identification of missing objects is a critical task in RFID-enabled applications. According to statistics [7], employee theft, vendor fraud, and management errors have become the main causes of inventory shrinkage in warehouses, retail stores, and supermarkets. In these scenarios, increasing delays in discovering and tracking the missing objects may cause substantial economic losses. Intuitively, to identify the missing objects, the RFID reader has to identify the missing tags. Therefore, this paper studies the challenging problem of missing tag identification, which can be formulated as follows: given a candidate tag set $S_{all}$, whose IDs are known by the reader, design a protocol that is capable of completely pinpointing the missing tags in $S_{all}$ using the minimum execution time, which we define as time efficiency.

Although many approaches based on RFID have been proposed to identify the missing tags [8]–[13], these approaches have the following limitations. First, the ID collection protocols are time-consuming [8], [9], [14]. In these protocols, each tag has to transmit its 96-bit ID that has been pre-stored in the reader. In addition, serious tag collisions cause many tags to transmit their IDs multiple times. Second, most existing missing tag identification protocols only verify tags one by one and therefore cannot meet the real-time requirements [11]–[13], [15]–[17]. Specifically, existing works use the stored tags’ ID and hash method to predict the slot selection of each tag in the frame and verify the presence of tags by comparing the status of expected singleton slots with actual singleton slots. As shown in Fig. 1, the reader in existing works check whether slot 1 and slot 4 are empty or not during actual execution, so that only two tags $t_1$ and $t_3$ can be identified by the reader. Although many efforts aim at increasing the proportion of singleton slots in the frame [11], [15], [16], they still waste many empty slots and collision slots. Moreover, most protocols ignore the impact of the missing rate, which is the proportion of missing tags to all candidate tags, on the execution time [11], [12], [15]–[17]. Therefore, the performance of such protocols deteriorates sharply at high missing rates.

In this paper, we reduce the empty slots and extract the information hidden in the collision slots for tag verification.
Specifically, we set a shorter frame length to map multiple tags in each slot. Then we separate the collided tags into different bits in a $w$-bit sequence, which we define as a string. These tags are expected to simultaneously transmit a string to the reader, and each tag sets one bit in its string to “1” and the other bits to “0” through Manchester encoding.

Accordingly, we first propose the Sequential String based Missing Tag Identification (SSMTI) protocol. SSMTI converts all slots to collision slots and performs hash calculations to arrange each collided tag to a position of bit “1” in the string. After that, the reader enables tags to transmit their respective strings simultaneously in each collision slot. As shown in Fig. 1, tags $t_1$, $t_2$, and $t_4$ are respectively arranged to the first, second, and third bit in the string. These three tags simultaneously transmit the strings, whose combination is expected to be “XXX”. Here “X” is the collided bit. Since the reader only receives “X0X”, it identifies that $t_1$ is missing and $t_2$, as well as $t_4$, are present. Furthermore, we propose the Interactive String based Missing Tag Identification (ISMTI) protocol to accelerate the identification process under high missing rates. ISMTI arranges multiple tags to the same bit in the string so that the reader can identify more missing tags using a shorter string length. As shown in Fig. 1, by checking the first bit of the string “0X”, the reader identifies that $t_1$ and $t_2$ are missing. We provide theoretical analysis for optimizing the parameters in our proposed protocols and conduct extensive simulation analysis to evaluate their performance under different working scenarios. Numerical results, which match the analytical results well, demonstrate that the proposed protocols can significantly reduce execution time by 39.74% and 68.87% when comparing with state-of-the-art solutions.

The rest of the paper is organized as follows: Section II reviews the related works. Section III introduces the system models and formulates the main problem. The detailed process of our proposed protocols is illustrated in Section IV, Section V, and Section VI. Some discussions of the proposed protocols are described in Section VII. The simulation results and analyzes are presented in Section VIII. Section IX concludes the paper.

II. RELATED WORKS

Fast identifying the missing tags is critical to avoid substantial economic losses. The solutions to missing tag identification can be classified into two categories: ID collection protocol [9], [10], [14], [18]–[20] and missing tag identification protocol [3], [11]–[13], [15], [16], [21].

Collecting the ID of all the tags under the reader’s coverage is a direct way to identify the missing tags. Existing ID collection protocols can be divided into two categories: Tree-based protocols [9], [10] and Aloha-based protocols [14], [19], [20]. In Tree-based protocols, the reader broadcasts a query command containing a string “0”, and tags whose IDs start with “0” will respond. When the reader detects a collision, it appends a “0” or “1” to the previous string and queries the unidentified tags using this new string. When the reader successfully receives a reply, it identifies the involved tag. After the reader has identified all tags, the identification process in Tree-based protocols is terminated. On the other hand, Aloha-based protocols divide the frame into multiple time slots and enable each tag to select a time slot randomly to reply to its ID. When two or more tags respond in the same time slot, the reader detects a collision and requires involved tags to reply again. When the reader successfully receives the tag ID in a time slot, it can identify the involved tag. The identification process in Aloha-based protocols consists of multiple frames until all the tags are identified by the reader. In summary, ID collection protocols suffer from server tag collisions. Moreover, it is time-consuming for each tag to transmit the 96-bit ID that the reader already knows.

The missing tag identification protocols can be classified into two categories: probabilistic detection and deterministic identification. Probabilistic detection protocols [22]–[24] aim at detecting whether or not any tags are missing under the reader’s coverage with a predefined probability. However, these protocols are unable to completely identify the missing tags and therefore cannot solve the problem in this paper. On the other hand, deterministic identification protocols [3], [11]–[13], [15], [16], [21] aim at determining the IDs of all the missing tags. The basic idea of these protocols is to precompute the expected status of each slot using the stored tag IDs and compare the status of the expected time slots with actual time slots. By checking the difference between the expected slots and actual slots, the reader can determine the involved missing tags.

The Iterative ID-free Protocol (IIP) [15] was the early work to identify missing tags. In IIP, the reader checks the expected singleton slots to verify the presence of tags and increases the proportion of expected singleton slots using an additional hash function. However, about half of the slots in the frame cannot be used by IIP. To improve the slot utilization of IIP, the Multi-hashing based Missing Tag Identification (MMTI) protocol [16] was proposed to turn most expected collision and empty slots into singleton slots for tag verification. However,
to achieve this goal, the reader in MMTI has to spend much time broadcasting a long-bit indicator vector. Similar to MMTI, the Slot Filter-based Missing Tag Identification (SFMTI) protocol [11] was proposed to turn a part of the expected two-collision slots and three-collision slots into singleton slots. Compared with IIP, SFMTI can achieve better time efficiency. Considering that the SFMTI protocol can only verify tags one by one, the Pair-Wise Collision-Resolving Missing Tag Identification (PCMTI) protocol [12]. Coarse-grained inventory list Stocktaking (CLS) protocol [13], and Collision Resolving based Missing Tag Identification (CR-MTI) protocol [17] were proposed. In PCMTI, the reader uses Manchester coding to verify two tags simultaneously in each expected two-collision slot that are mapped by two tags. On the other hand, the reader in CR-MTI verifies tags in expected singleton slots and part of the collision slots. However, many collision slots are still ignored by PCMTI and CR-MTI, thus limiting the performance of these protocols. Moreover, the above-mentioned identification protocols do not consider the impact of the missing rate on the execution time and become time-consuming as the missing rate increases. The CLS protocol is designed to identify missing tags under high missing rates. Specifically, the reader checks each expected collision slot for tag verification. When an expected collision slot becomes empty during execution, the reader can identify multiple missing tags together. However, it is time-consuming for the reader to check all collision slots when most tags are present. In summary, existing works cannot effectively explore the expected collision slots for tag verification, which has motivated us to design new protocols.

III. SYSTEM MODEL AND PROBLEM DESCRIPTION

A. System Model

A large-scale RFID system consists of a back-end server, an RFID reader, and N RFID tags. The back-end server has powerful capabilities of data processing and communicates with the reader via high-speed links. The RFID reader can communicate with tags within a certain range, which we define as the interrogation region. Each candidate tag has a unique 96-bit ID and is equipped with a hash function \( H(\cdot) \). Note that the hash based protocols assume that both the reader and tags share the common hash function, which is thoroughly studied [11]–[13], [15]. We use \( S_{\text{all}} = \{t_1, t_2 \ldots t_N\} \) to denote the set of candidate tags to be monitored in the RFID system. The set of tags that move out of the reader’s interrogation region is called missing tags and is referred to as \( S_m \). Accordingly, the remaining tag set is called present tags and is represented by \( S_p \). We use \( N, M, \) and \( P \) to denote \( |S_{\text{all}}|, |S_m|, \) and \( |S_p| \), where \(|\cdot|\) stands for the cardinality of a set. By accessing the back-end server, the reader can generate an inventory list that records the IDs of all candidate tags.

B. Communication Model

The communications between the reader and tags are assumed to be reliable and use the frame slotted Aloha protocol [25]. Specifically, the reader divides time into multiple frames, and each frame includes multiple time slots. At the beginning of a frame, the reader initiates the communication by broadcasting the Query command containing frame size \( f \) and random seeds \( r \). Upon receiving the reader’s command, each tag calculates \( H(id, r) \mod f + 1 \) as the slot index to reply. According to tags’ replies, the reader can divide the time slots into three types: empty slots with no tag reply, singleton slots with only one tag reply, and collision slots with multiple tag replies. Besides, the reader can also pre-compute the status of each slot using the stored IDs of \( N \) tags. We refer to the time slots calculated by the reader as expected slots and the time slots during execution as actual slots. The process of executing all the expected slots in a frame is called a round of identification, and the reader usually needs multiple rounds to identify all candidate tags.

C. Problem Statement

Existing works only identify missing tags under a fixed missing rate in the system. However, the missing rate may vary in different application scenarios [13]. For example, when we use a reader to perform high-frequency scans for the same region, candidate tags recorded in the inventory list can be updated periodically by the reader and therefore are usually close to the present tags. On the other hand, when we use the reader to scan the tags for the first time, the present tags might be much smaller than the candidate tags in the inventory list. Therefore, we concentrate on quickly identifying all the missing tags under various missing rates. Similar to previous works [11], [13], [16], the execution time is taken as the most critical performance metric. Generally, the problem can be summarized as follows: given the candidate set \( S_{\text{all}} \) whose IDs are known by the reader, identify all missing tags \( S_m \) in \( S_{\text{all}} \) using the minimum execution time.

D. Bit Tracking

Bit tracking is based on Manchester encoding, which defines a one-bit value as a voltage conversion within a fixed time. In RFID systems, the bit tracking technology can detect the positions of collided bits in a string and therefore has been widely used in information collection protocols, anti-collision protocols, and unknown tag identification protocols [9], [26]–[28]. In these protocols, bit tracking requires tags to respond to the reader synchronously. Note that RFID systems usually operate at low rates and the transfer rate of a tag to the reader is 25 us [16], [17]. Since the synchronization offset for commercial RFID tags is no more than 1 us [29], a bit duration offset of 4% does not have much negative on bit tracking [30] and the clocks of the tags can be well synchronized via the signal received from the reader [9], [26]. Moreover, the practical experiment of bit synchronization with USRP and WISP also verified that the bit tracking in the UHF RFID system is feasible [30]. Therefore, we assert that the signals from each tag can be well synchronized on bit-level [9], [26]–[28] and introduce bit tracking technology in this paper to accelerate tag identification and the proposed method.

Different from most missing tag identification protocols that only verify each tag in the expected singleton slot, we use bit tracking to explore the information hidden in collision slots
for tag verification. As shown in Fig. 2, we assume that an expected collision slot is mapped by Tag 1, Tag 2, and Tag 3. The reader separates these tags into different bits in a five-bit string, which is represented by W. Since Tag 1 is arranged to the first bit, this tag sets the value of this bit to “1” and the value of the other bits to “0”. Similarly, Tag 2 and Tag 3 are arranged to the third and fifth bit. These three tags are expected to transmit their strings to the reader simultaneously. By decoding the first, third, and fifth bits of the combined string, the reader can determine whether or not any tags are missing. Specifically, When the reader detects a collided bit or a bit value of “1”, the tag arranged to this bit can be identified as the present tag. On the other hand, when the reader detects a bit value of “0” or receives no signal, it can identify the tag as the missing tag. Following this idea, we design three protocols to identify the missing tags quickly.

IV. SEQUENTIAL STRING BASED MISSING TAG IDENTIFICATION PROTOCOL

In the most related CR-MTI protocol [17], multiple tags can be identified by the reader in the expected collision slots only when each tag obtains a unique value in the string. However, due to the probabilistic nature of the hash function, many expected collision slots cannot be resolved. Moreover, to resolve the collision slots, the string length \( w \) has to be larger than the involved tags, resulting in multiple bits in the string are not arranged by any tags. To address this problem, we propose the Sequential String-based Missing Tag Identification (SSMTI) protocol. SSMTI converts all the expected slots into resolvable collision slots and uses short indicator vectors to make each bit in the string corresponding to a tag. SSMTI consists of four stages: main filter vector construction stage, collided tags reconciling stage, candidate tags sequencing stage, and present tag verification stage. The reader executes the first three stages round by round until each candidate tag has been arranged a unique value. After that, the reader begins the fourth stage and checks the response of each slot. In what follows, we will describe the SSMTI protocol.

A. Protocol Description of SSMTI

1) Main Vector Construction Stage: In this stage, the reader maps each tag to a bit and constructs a main vector accordingly. Specifically, the reader constructs the main vector \( F_2 \) with \( f_2 \) elements as follows: if a bit is selected by one tag, the reader sets the corresponding elements in \( F_2 \)

2) Collided Tags Reconciling Stage: For each bit that is selected by two tags, the reader generates another seed \( r_2 \) and calculates \( H(id_i, r_2) \mod 2 \) using the involved tags’ IDs. If each tag obtains a unique value of 0 or 1, we say this bit is reconcilable. After that, the reader updates the value of the corresponding elements in \( F_2 \): if a bit is reconcilable, the reader updates the corresponding element in \( F_2 \) to “3”; if a bit is unreconcilable, the reader updates the corresponding element in \( F_2 \) to “4”. An example of the reconciling stage is shown in Fig. 5. Since \( H(id_{a_4}, r_2) \mod 2 = 0 \) and \( H(id_{a_6}, r_2) \mod 2 = 1 \), the first bit is reconcilable. On the other hand, \( t_7 \) and \( t_9 \) obtain the same value of 0. Therefore, the sixth bit is unreconcilable.

After that, the reader constructs an append filter vector \( A \) with \( a \) elements based on the following rules:

(i) If \( F_2[i] = 1 \), which means that the \( i \)-th bit is selected by one tag, the reader will set the \( a_i + 1 \)-th element of vector \( A \) to “0”, where \( a_i \) is the number of elements “1” and “4” proceeding the \( F_2[i] \).

(ii) If \( F_2[i] = 4 \), which means that the \( i \)-th bit is selected by two tags and is reconcilable, the reader will set the \( a_i + 1 \)-th element of vector \( A \) to “1”.

As illustrated in Fig. 5, since \( F_2[1] = 4 \) and \( a_1 = 0 \), the reader sets \( A[1] = 1 \). On the other hand, since \( F_2[4] = 1 \) and \( a_4 = 1 \), the reader sets \( A[2] = 0 \).

3) Candidate Tags Sequencing Stage: In this stage, the reader combines the main vector \( F_2 \) and the append vector \( A \) to construct the indicator vector \( V_2 \). Specifically, if \( F_2[i] = 1 \) and \( A[a_i + 1] = 1 \), the reader will set the \( i \)-th element of \( V_2 \) to “11”; if \( F_2[i] = 1 \) and \( A[a_i + 1] = 0 \), the reader will set the \( i \)-th element of \( V_2 \) to “10”; otherwise, the reader sets the \( i \)-th element of \( V_2 \) to “0”. As shown in Fig. 5, since \( F_2[1] = 1 \) and \( A[0 + 1] = 1 \), the reader sets \( V_2[1] = 11 \). Similarly, the reader sets \( V_2[4] = 10 \) because \( F_2[4] = 1 \) and \( A[1 + 1] = 0 \). In our construction method, only the elements corresponding to reconcile 2-collision slot and singleton slot are encoded by 2 bits in \( V_2 \). In the simulation, we will evaluate that this constructed method can reduce the number of bits transmitted by the reader.

After constructing the indicator vector, the reader broadcasts
V_2 and parameters, including f_2, a, r_1, r_2, w, and \( \mu \) to all tags. Here \( \mu \) is the number of tags that have received a unique number before the current execution round.

Upon receiving the indicator vector and parameters, each present tag, say \( t_c \), obtains an index \( i \) by calculating \( H(id_i, r_1) \mod f_2 + 1 \). Then \( t_c \) checks the indicator vector \( V_2 \). Let \( \chi_{10} \) and \( \chi_{11} \) be the number of “10” and “11” before the \( i \)th element in \( V_2 \). \( t_c \) will store \( \chi_{10} \) and \( \chi_{11} \), and determine where and how to reply to the reader based on the following rules:

(iii) If \( V_2[i] = 0 \), which means that the \( i \)th bit is unreconcilable, \( t_c \) will wait for the indicator vector in the next round.

(iv) If \( V_2[i] = 1 \), which means that the \( i \)th bit is selected by one tag, \( t_c \) will calculate \( \chi = \mu + \chi_{10} + 2 \times \chi_{11} + 1 \) as its unique value and wait for the beginning of the fourth stage.

(v) If \( V_2[i] = 11 \), which means that the \( i \)th bit is reconcilable, \( t_c \) will perform \( H(id, r_2) \mod 2 \). If the hashing result is “0”, \( t_c \) will calculate \( \chi = \mu + \chi_{10} + 2 \times \chi_{11} + 1 \) as its unique value. If the hashing result is “1”, \( t_c \) will calculate \( \chi = \mu + \chi_{10} + 2 \times \chi_{11} + 2 \) as its unique value. After that, \( t_c \) will wait for the beginning of the fourth stage.

As illustrated in Fig. 5, since \( V_2(2) = V_2(3) = V_2(5) = V_2(6) = 0 \), \( t_1 \), \( t_2 \), \( t_3 \), \( t_6 \), \( t_7 \), \( t_9 \), and \( t_{10} \) wait for the indicator vector in the next round. On the other hand, since \( V_2(1) = 11 \), \( t_4 \) and \( t_8 \) perform \( H(id, r_2) \mod 2 \). Then \( t_4 \) calculates \( \chi = 0 + 0 + 2 \times 0 + 1 \) and \( t_8 \) calculates \( \chi = 0 + 0 + 2 \times 0 + 2 \). Note that in the example of Fig. 5, we assume no tag has been arranged a unique number before the current round. Therefore, \( \mu = 0 \). Since \( V_2(4) = 10 \) and the number of \( \chi_{11} \) before the fourth element of \( V_2 \) is 1, \( t_5 \) calculates \( \chi = 0 + 0 + 2 \times 1 + 1 \). Both \( t_4 \), \( t_5 \), and \( t_8 \) keep silent and wait for the beginning of the fourth stage.

4) Present Tag Verification Stage: After each tag has obtained a unique value \( \chi \), the reader begins the fourth stage. In this stage, each present tag \( t_c \) will calculate \( \lceil \frac{\chi}{w} \rceil \) as its actual slot to reply. Meanwhile, the tag will calculate \( j = \chi \mod w \) to sets the \( j \)th bit to “1” and all other \( w - 1 \) bits to “0” in its string. In Fig. 5, \( t_5 \) calculates \( i = \lceil \frac{\chi}{6} \rceil = 1 \) and \( j = 3 \mod 6 = 3 \). Therefore, \( t_5 \) transmits a 6-bit string “001000” in slot 1.

After replying, \( t_c \) will keep silent and not participate in the subsequent identification process.

On the reader side, the reader checks each receiving string, whose bits are all expected to “1”. If the reader detects a difference, the corresponding tags are identified as missing. As illustrated in Fig. 5, since the reader detects “XXX0X00” in slot 1 and “X0X000” in slot 2, the reader identifies that \( t_1 \), \( t_3 \), \( t_2 \), \( t_7 \), and \( t_9 \) are missing. Meanwhile, the other tags are identified as present.

B. Parameter Optimization

We first determine the optimal main vector length \( f_2 \) for the first three stages. The tag that has obtained a unique value is called the arranged tag. Let \( P_{SS} \) denote the probability that a candidate tag can be successfully arranged to a unique value. Then we have

\[
P_{SS} = P_{SS}^1 + P_{SS}^2
\]  

where \( P_{SS}^1 \) is the probability that a bit is mapped by only one tag and \( P_{SS}^2 \) is the probability that a bit is mapped by two tags and is reconcilable. Here we calculate \( P_{SS}^1 \) as

\[
P_{SS}^1 = \left( \frac{N^*}{2} \right) \left( \frac{1}{f_2} \right) \left( 1 - \frac{1}{f_2} \right)^{N^* - 1}
\]  

\[
\approx \frac{N^*}{f_2} e^{-\frac{N^*}{2}}
\]  

(2)

For a bit that is mapped by two tags, the probability that it can be reconciled is \( \frac{2!}{2^2} \). Hence, we calculate \( P_{SS}^2 \) as

\[
P_{SS}^2 = \left( \frac{N^*}{2} \right) \left( \frac{1}{f_2} \right)^2 \left( 1 - \frac{1}{f_2} \right)^{N^* - 2} \times \frac{2!}{2^2} 
\]  

\[
\approx \frac{N^* (N^* - 1)}{4f_2^2} e^{-\frac{N^* - 2}{2}}
\]

(3)

Let \( \phi_{SS} \) denote the expected number of bits that can be used for unique value arrangement in each round of the first three stages, and let \( \phi_{SS}^k \) denote the number of bits selected by \( k \) tags. We can calculate \( \phi_{SS} \) as

\[
\phi_{SS} = \phi_{SS}^1 + \phi_{SS}^2
\]

\[
= f_2 \times P_{SS}^1 + f_2 \times P_{SS}^2
\]

\[
= f_2 f_2 e^{-p_2} + \frac{1}{4} f_2 f_2 e^{-p_2}
\]

(3)

where \( \frac{N^*}{f_2} = p_2 \). Let \( N_{SS} \) denote the number of arranged tags in each round of the first three stages and \( N_{SS}^k \) denote the number of arranged tags in the bits that are selected by \( k \) tags. We can calculate \( N_{SS} \) as

\[
N_{SS} = N_{SS}^1 + N_{SS}^2
\]

\[
= f_2 \times P_{SS}^1 + f_2 \times f_2 \times P_{SS}^2
\]

\[
= f_2 f_2 e^{-p_2} + \frac{1}{2} f_2 f_2 e^{-p_2}
\]

(4)
Let $T_{SS1}$ denote the execution time of each round in the first three stages. Note that the length of the indicator vector $V_2$ is $f_2 + a$. Hence, we can calculate $T_{SS1}$ as

$$T_{SS1} = \left[ \frac{(f_2 + a)}{96} \right] \times t_{tag}$$
$$= \left[ \frac{(f_2 + \phi_1 + \phi_2) + 1}{96} \right] \times t_{tag}. \quad (5)$$

Combing (13), (14), and (15), we can calculate the efficiency of identifying each tag in the fourth stage as

$$\epsilon \approx w = \frac{(f_2 + \phi_1 + \phi_2) + 1}{96} \times t_{tag}. \quad (6)$$

The objective of the first three stages is to maximize the efficiency. Hence we calculate the derivative of the efficiency with respect to $p_2$ as

$$\left( \frac{\epsilon}{T_{SS1}} \right)' = \frac{\left( 1 - \frac{1}{2^{p_2}} \right) \times \left[ \left( \frac{3}{2^{p_2}} - 1 \right) \times \frac{e^{-p_2}}{p_2} + 1 \right] \times e^{-p_2}}{\left( \frac{p_2 e^{-p_2} + \frac{1}{2^{p_2}} e^{-p_2}}{p_2 e^{-p_2} + \frac{1}{2^{p_2}} e^{-p_2} + 1} \right)^2 \times t_{tag}}. \quad (7)$$

We can obtain an optimal $p_{opt}$ to satisfy $\left( \frac{\epsilon}{T_{SS1}} \right)' = 0$. When $p_{opt} \approx 1.50$, $\frac{\epsilon}{T_{SS1}}$ is maximized. Therefore we obtain the optimal size of the main vector $f_{opt} = N^*/1.5$ and the execution time of the first three stages is $NT/8 = N/16.0448 \approx 0.0623N$, where $N$ is the number of total candidate tags.

Let $T_{SS2}$ denote the execution time in the present tag verification stage. $T_{SS2}$ includes the time to reply to the $w$-bit strings. Since each tag is arranged to a unique value, the total number of strings is equal to $\left[ \frac{N}{w} \right]$. Recall that the time to transmit one string is $t_w = 0.4 + (w - 1) \times 0.025$, we can calculate $T_{SS2}$ as

$$T_{SS2} = \left[ \frac{N}{w} \right] \times t_w$$
$$= \left[ \frac{N}{w} \right] \times (0.4 + (w - 1) \times 0.025). \quad (8)$$

where $\left[ \right]$ is the ceiling function. Therefore, we can calculate the efficiency of identifying each tag in the fourth stage as

$$N \times T_{SS2} \approx \frac{w}{(0.4 + (w - 1) \times 0.025)}. \quad (9)$$

Since $w > 0$, $N/T_{SS2}$ is a monotonically increasing function with respect to $w$. Intuitively, the larger the $w$ value, the more tags can be identified in each string. In this paper, we set $w = 96$ as the length of each string in SSMMI because the maximum length of the vector should not be greater than 96 bits [15, 16, 27, 30]. Therefore, the execution time of SSMMI is approximately $(0.0623N + \left[ \frac{N}{96} \right] \times 2.375)$ ms.

V. INTERACTIVE STRING BASED MISSING TAG IDENTIFICATION PROTOCOL

In the proposed SSMMF protocol, each bit in the string corresponds to a tag to be verified. However, when the missing rate is high, we can arrange multiple tags to the same bit value in a string to further improve the time efficiency of SSMMI. Following this idea, we propose the Interactive String-based Missing Tag Identification (ISMFI) protocol, which consists of two stages: the present tag response stage and the missing tag verification stage. ISMMF executes two stages round by round until all the tags are identified. The detailed operations of these two phases are presented below.

A. Present Tag Response Stage

In this stage, the reader broadcasts the parameters $f_3$, $r$, and $w$ to all the tags. Subsequently, the reader predicts the slot and bit mapping of each tag using tags’ IDs. Accordingly, the reader constructs an expected vector EV consisting of $f_3$ elements. Specifically, the element’s value of EV is encoded by “0” if the corresponding bit is not mapped by any tags in the string; “1” if the corresponding bit is mapped by one tag in the string; “2” if the corresponding bit is mapped by multiple tags in the string. As depicted in Fig. 6, the reader constructs the expected frame vector $EV = [022222]$.

Once receiving the parameters, each tag $t_i$ will calculate $i = \left[ (H(id_i, r) \mod f + 1)/w \right]$ as the actual slot to reply. Meanwhile, $t_i$ will calculate $j = \left[ H(id_i, r) \mod f \right]$ as the actual slot to transmit. As shown in Fig. 6, the reader constructs the expected frame vector $EV = [022222]$. The reader constructs the vector $EV = [022222]$.

B. Missing Tag Verification Stage

After receiving the strings from all the present tags, the reader can generate an actual vector AV consisting of $f_3$ elements. Specifically, for each bit of strings received by the reader, if the reader detects “1” or “X”, the reader will set the corresponding element in AV to “1”; otherwise, the reader will set the corresponding element in AV to “0”. As some tags are missing, some elements in EV with a value of “1” or “2” will become “0” in AV. Therefore, the reader can identify the missing tags by comparing EV and AV. As shown in Fig. 6, since the reader detects “0” or no signal in the fourth, fifth, sixth bit of AV, the reader identifies that $t_3$, $t_5$, $t_7$, $t_9$, $t_{10}$, and $t_{11}$ are missing.

Then, the reader constructs the indicator vector $V_3$ according to the following rules:

(i) If $EV[i] = 0$, $V_3[i] = 0$.
(ii) If $EV[i] = 1$ or $2$, and $AV[i] = 0$, $V_3[i] = 1$.
(iii) If $EV[i] = 1$ and $AV[i] = 1$, $V_3[i] = 1$.
(iv) If $EV[i] = 2$ and $AV[i] = 1$, $V_3[i] = 0$.

After that, the reader broadcasts $V_3$ to all the tags. Each tag $t_i$ checks the value of its corresponding bits in $V_3$. If the value happens to be “1”, $t_i$ will keep silent and not participate in
the subsequent identification process; otherwise, \( t_c \) will wait for the beginning of the next round. As shown in Fig. 6, \( t_1 \), \( t_2 \), \( t_5 \), and \( t_8 \) are expected to participate in the next round.

\[ EV = T^\ast \left[ f_3 \left( \frac{q}{f_3} - q \right)^{k-1} \left( 1 - \frac{1}{f_3} \right)^{N^* - k} \right] \times \frac{N^* q}{f_3} - f_3 P_{1IS}^1 q. \]  

\[ \sum_{k=2}^{N^*} N_{1IS}^k = f_3 \sum_{k=2}^{N^*} \left( \frac{N^* q}{f_3} - q \right)^{k-1} \left( 1 - \frac{1}{f_3} \right)^{N^* - k} \times \frac{N^* q}{f_3} - f_3 P_{1IS}^1 q. \]  

(11)

According to the binomial theorem, we rewrite (21) as

\[ \sum_{k=2}^{N^*} N_{1IS}^k = f_3 \left( \frac{N^* q}{f_3} + 1 - \frac{1}{f_3} \right)^{N^* - 1} - P_{1IS}^1 q. \]  

(12)

where \( p_3 = \frac{N^*}{f_3} \). Hence we can obtain \( N_{1IS} \) as

\[ N_{1IS} = N_{1IS}^1 + \sum_{k=2}^{N^*} N_{1IS}^k = f_3 \times \left( p_3 q e^{-p_3} + p_3 q e^{-p_3(1-q)} - p_3 q e^{-p_3} \right). \]  

(13)

Let \( T_{IS} \) denote the execution time in each round of ISMTI. \( T_{IS} \) includes the transmission time of the \( f_3 \)-bit string and the \( f_3 \)-bit indicator vector \( V_3 \). Hence, we calculate \( T_{IS} \) as

\[ T_{IS} = \left[ \frac{f_3}{96} \right] \times t_w + \left[ \frac{f_3}{96} \right] \times t_{tag}. \]  

(14)

Combing (23) and (24), we can obtain the efficiency as

\[ \frac{N_{IS}}{T_{IS}} = \frac{N_{1IS} + \sum_{k=2}^{N^*} N_{1IS}^k}{f_3 \times t_{tag} + f_3 \times t_w} \approx 96 \left( p_3 q e^{-p_3} + p_3 q e^{-p_3(1-q)} - p_3 q e^{-p_3} \right) t_{tag} + t_w. \]  

(15)

To maximize the efficiency, we can calculate the derivative of the efficiency with respect to \( p_3 \). Here we set the length of \( w \) to 96 to verify more tags in a slot. Owing to the existence of \( q \), which is unknown by the reader in advance, we should first estimate the number of missing tags. Although we can use some existing methods to estimate the cardinality of tags before executing the ISMTI, the time overhead and protocol complexity will increase accordingly. Therefore, we propose a cardinality estimation method based on the replies of all the tags in each round of ISMTI. Recall that the reader can obtain the expected vector \( EV \) by using its stored IDs and the actual vector \( AV \) based on the replies from tags. Hence, we have:

\[ \exists i \in [1...f_3], EV[i] \neq AV[i]. \]  

Let \( P_{11} \) denote the probability
that the current bit of a string is arranged to one present tag, we have
\[
P_{11} = \left(\frac{N^* - M^*}{1}\right) \left(\frac{1}{f_3}\right) \left(1 - \frac{1}{f_3}\right)^{N-1} \approx \frac{N^* - M^*}{f_3} e^{-\frac{N^*}{f_3}}, \tag{16}
\]
where \(M^*\) is the number of unidentified missing tags in the current round. Let \(N_{11}\) denote the number of bits mapped by one present tag in each round, which follows the distribution of Bernoulli \((f_3, P_{11})\). Then we can calculate the expectation of \(N_{11}\) as
\[
E_{N_{11}} = f_3 \times P_{11} = (N^* - M^*) \times e^{-\frac{N^*}{f_3}}. \tag{17}
\]
Let \(N_I\) denote the number of bits arranged to one tag in each round. According to \((12)\), we can calculate the expectation of the \(N_I\) as
\[
E_{N_I} = f_3 \times P_{11}^\ast = N^* \times e^{-\frac{N^*}{f_3}}. \tag{18}
\]
Combining \((27)\) and \((28)\), we can obtain the expressions of \(M^*\) as
\[
M^* = N^* - \frac{E_{N_{11}}}{E_{N_I}} \times N^*. \tag{19}
\]
Substituting \(N_I\) for \(E_{N_I}\) and \(N_{11}\) for \(E_{N_{11}}\) we can calculate the estimators \(\hat{M}^*\) as
\[
\hat{M}^* = N^* - \frac{N_{11}}{N_I} \times N^*. \tag{20}
\]
Therefore, we can obtain the missing rate \(q\) of each round as
\[
q = \frac{\hat{M}^*}{N^*}. \tag{21}
\]
Note that we cannot directly provide a closed-form expression of \(f_3\) because \(q\) is different in different scenarios. However, when \(q\) is estimated, we can equate the derivative of \(\theta\) to 0 and calculate the optimal value of \(p_{opt}\). Then, we can obtain the optimal value of \(f_3\) as \(f_{opt} = N^*/p_{opt}\).

VI. DISCUSSION

A. Practical Implementation Issues

To implement the proposed protocols on commercial RFID devices, we need to make the following modifications to the reader and tags. First, the tags need to execute hash calculations based on their ID and the random seed broadcast by the reader. Recently, such on-tag hashing has been implemented on commercial RFID devices using the fundamental and mandatory functionalities in the EPC C1G2 standard \[31\]. Second, the tags need to add a counter to store the slot index. Compared with the overall circuit scale of modern tags \[32\], the added counter is negligible. Moreover, the functionality of recording the slot index is also used in previous protocols \[3\], \[11\]–\[13\]. Third, the tags need to perform simple arithmetic operations. Compared with the EPC C1G2 protocol, the additional operation of our protocol is only the addition operations, and each passive tag is equipped with about 4000-5000 NAND gates. Therefore, it is feasible to deploy our protocol on passive tags \[33\]. On the other hand, to achieve the functionality of transmitting the indicator vector and the parameters in each round, the RFID reader needs to add extra custom commands supported by the EPC C1G2 protocol \[29\]. However, this operation does not need to change the original hardware circuit of the reader. Therefore, the proposed protocols have the potential to be implemented on commercial RFID systems.

B. Multiple-Reader RFID Systems

Due to the limited interrogation range, which is normally less than 10 meters \[34\], it is challenging for a single RFID reader to cover a large-scale identification area. Although handheld readers are available to scan a specific area of a large system periodically, multiple readers are also required in many scenarios. However, if two or more adjacent readers simultaneously interrogate the tags in a multiple-reader RFID system, the readers’ signals will collide. In this case, the overlapping tags cannot receive correct commands. To avoid the collision of readers, some advanced reader-scheduling algorithms \[35\], \[36\] were proposed to determine the query order of each reader. Since reader scheduling strategy is not the key point of this paper, we consider using the Colorwave scheme \[37\] to illustrate the extension of our protocols in multiple-reader RFID systems. Specifically, we use one color to mark readers without collision as many as possible. Then, we mark the readers without collision among the remaining uncolored readers using a different color. This coloring process is executed continuously until all readers are marked. Finally, we active all readers of the same color to execute the proposed protocols in parallel.

In multiple-reader RFID systems, the back-end server stores the IDs of all the tags, but each reader does not have the tag IDs in its interrogation range. Therefore, we use the whole tag set as input to calculate the same parameters and indicator vectors for the first batch of scheduled readers. When receiving the replies from tags, each reader sends the information to the back-end server for data aggregation. After all the readers having completed the missing tag identification, we activate readers of another color to restart the protocol. To save execution time, the back-end server deletes the identified present tags from the inventory list and then uses IDs of the remaining tags to calculate the parameters and vectors for the next batch of scheduled readers. The scheduled process is continuously executed until all readers have completed the missing tag identification.

VII. PERFORMANCE EVALUATION

In this section, we evaluate the performance of the proposed SSMTI and ISMTI protocols. For a fair comparison, we use the same wireless communication settings for each protocol based on the specification of the Philips I-Code system \[38\]. Specifically, after including the required waiting times between two transmissions, the time for the reader or tags to transmit a 1-bit message is \(t_s = 0.4\) ms, and the time to transmit a 96-bit tag ID is \(t_{tag} = 2.4\) ms. In other words, the data rate is about 96/2.4 = 40 kbps \[12\], \[16\]. Therefore, it takes \(0.4 + (w - 1) \times 0.025\) ms to transmit a \(w\)-bit string for each
tag. In addition, the communication channels between the reader and tags are considered as error-free as in the literature [12], [13], [15], [16]. For reliability, we carry out five hundred experiments for each parameter group and report the averaged results.

A. Comparative Works

To verify the efficiency of the proposed protocols, we consider two types of tag identification protocols as benchmarks. The first type is anti-collision protocol, which consists of a well-known Aloha-based protocol, namely Enhanced Dynamic Framed Slotted Aloha (EDFSA) [14], and an advanced tree-based scheme, which is M-ary Query Tree scheme (MQT) [39]. On the other hand, the second type is advanced missing tag identification protocols, including IIP [15], MMTI [16], SFMTI [11], CLS [13], PCMTI [12], and CR-MTI [17].

We set the frame length of EDFSA, IIP, MMTI, SFMTI, PCMTI to $N^*/14$, $N^*/1.516$ [15], $N^*/1.68$ [11], $0.8735N^*$ [12], and $N^*/34$ [17], where $N^*$ is the number of tags not verified by the reader at the beginning of each round. For CLS, its frame length is set according to the missing rate of each round [13].

B. Impact of Frame Length and String Length

In this section, we simulate the proposed SSMTI and ISMTI under different parameters and compare the average execution time to identify a candidate tag. Here we set the number of candidate tags $N$ as 10,000. Based on the analysis in Section IV, the optimal frame length of SSMTI is $f_{SS} = N^*/1.5$. Besides, the string length of SSMTI is $w_{SS} = 96$. On the other hand, the string length of ISMTI is $w_{IS} = 96$, and the optimal frame length $f_{IS}$ is set based on the missing rate. In Fig. 5(a), we vary the parameter $w$ of SSMTI. Similarly, to verify the setting of $f$, we also vary the parameter $p = \frac{N^*}{N}$ of SSMTI and ISMTI in Fig. 5. We can observe that the identification time of THSMTI and SSMTI are minimized when $w_{SS} = 38$ and $f_{SS} = N^*/1.5$. We can also observe in Fig. 5(c) that there is an optimal value of $p$ in ISMTI under different missing rates. Therefore, the simulation results match our theoretical analysis.

C. Impact of Number of Candidate Tags

Execution time: According to existing works [11]-[13], [16], [40], [41], the execution time is one of the most critical performance metrics in missing tag identification. The execution
time can be obtained by calculating the time required by the reader to transmit the indicator vectors and the time required by tags to reply. Note that the construction of indicator vectors and most of the calculation tasks are done on the reader side, which has powerful calculation and storage capabilities. Moreover, these tasks can be performed by the reader offline. Therefore, the execution time on the reader side is ignored like other protocols [11], [13], [15], [16].

In Fig. 6(a), we compare the execution time of the proposed protocols with existing works. Here we set the missing rate q as 0.1 and vary the number of candidate tags N from 1,000 to 10,000. We can observe that the execution time of all the protocols increases as the number of candidate tags grows. The reason is that more time slots are required by the reader to verify more candidate tags. The performance of the proposed SSMTI and ISMTI are better than other protocols. For example, when the number of candidate tags N = 10,000, the total execution time of EDFSA, MQT, IIP, SFMTI, PCMTI, CLS, and CR-MTI is approximately 58.75 s, 37.61 s, 8.66 s, 4.73 s, 3.05 s, 7.72 s, and 1.51 s. However, the execution time of ISMTI and SSMTI is 1.45 s, and 0.91 s. Compared with the state-of-the-art CR-MTI protocol, the proposed SSMTI protocol reduce the execution time by 39.74%. The underlying reasons are as follows. First, although EDFSA and MQT can reduce tag collisions, these protocols require each tag to transmit ID multiple times. Therefore, it is time-consuming to use anti-collision protocols to solve the problem of missing tag identification. On the other hand, most tag identification protocols, such as IIP, MMTI, and SFMTI, can only identify one tag in each time slot. The proposed protocols use bit tracking technology to verify multiple tags together in each collision slot, thus accelerating the identification process. Moreover, different from PCMTI and CR-MTI, which can only use part collision slots for tag verification and suffer from serious bit waste in each string, SSMTI exploits all collision slots and makes each bit of string correspond to an unverified tag, thus fundamentally improving the identification efficiency.

Number of bits transmitted: The number of bits transmitted by the reader and tags can reflect the complexity of the communication and implies the energy consumption of the communication process [9]. Under the same settings of Fig. 6(a), we compare the number of bits transmitted by the reader and tags in Fig. 6(b). We can observe that CR-MTI has to transmit more bits than SSMTI when the missing rate is low. The reason is that CR-MTI uses the hash method to arrange the bit positions in the string for each tag, resulting in some bits of the string may not be arranged to any tags. On the other hand, SSMTI transmits the fewest bits. The underlying reasons are as follows. First, the coding method of the indicator vectors in SSMTI reduces the bit transmitted by the reader. Second, SSMTI arranges each tag a unique bit in the string to reply, thus avoiding the waste of bits in CR-MTI.

Number of slots transmitted: Fig. 6(c) shows the number of actual response slots required by the reader to verify all tags. Compared with IIP, MMTI, and SFMTI, PCMTI can verify two tags simultaneously in a slot, thus requiring a smaller number of response slots. Based on the bit tracking technology, the proposed protocols can verify more than two tags in a slot. Therefore, SSMTI, and ISMTI require fewer response slots than PCMTI. Moreover, among the proposed protocols, SSMTI and ISMTI map more tags in each slot than CR-MTI, so they require fewer response slots than the CR-MTI protocol.

D. Impact of Missing Rate

In Fig. 7, we set N = 1,000, and vary the missing rate to evaluate the proposed protocols. We can observe in
Fig. 7(a) that the execution time of IIP, MMTI, SSFMTI, and PCMTI is stable. The reason for this result is that these protocols only verify one or two tags in a slot. Moreover, the execution time of CR-MTI, SSMTI is also stable because each tag is arranged to one bit in the string. Therefore, the execution time of the above protocols is only affected by the number of candidate tags. On the other hand, the execution time of CLS gradually decreases as the missing rate increases. The reason for this result is that CLS checks the expected collision slots for tag verification. When the missing rate is high, most expected collision slots will turn out to be empty during actual execution. However, when the missing rate is low, the performance of CLS is worse than SSMFTI because CLS cannot verify the collided tags in a slot. The proposed protocols run faster than existing approaches when the missing rate is less than 0.95. Moreover, as the missing rate increases, the execution time of the ISMTI protocol decreases quickly, so that ISMTI gradually becomes the fastest. For example, when the missing rate is 0.9, the execution time of CLS is approximately 3.05 s. ISMTI consumes 0.47 s, which reduce the execution time by 84.59%, 68.87%, and 48.96% compared with CLS, CR-MTI, and SSMFTI. Unlike CR-MTI and SSMTI that do not consider the impact of missing rate on execution time, ISMTI arranges multiple tags to the same bit in the string at high missing rates. In this way, the reader in ISMTI can verify more tags in each string than SSMTI, thereby further reducing the execution time. Besides, ISMTI can adaptively adjust the string design strategy according to the changing missing rate, thus avoiding the performance degradation of CLS.

In Fig. 7(b), we vary the missing rate from 0.999 to 0.999. We can observe that the execution time of EDFSA and MQT is also reduced because the number of present tags in the reader’s interrogation region is small. Moreover, the performance of EDFSA and MQT is better than that of CLS when most tags are missing. However, EDFSA and MQT are time-consuming in most scenarios and not suitable for identifying some valuable items because tag IDs are directly transmitted by tags in the air [3].

E. Impact of Estimation Error

When the reader does not know the missing rate, the ISMTI protocol can use the method in Section VI to estimate the number of missing tags. In Fig. 8, we compare the execution time of ISMTI using the proposed estimation method with ISMTI that is given the missing rate. Here we set the initial estimation of the missing rate \( p \) to 0.5 in the first round of ISMTI (estimate the missing rate). We can observe in Fig. 8 that the execution time of ISMTI (estimate the missing rate) is close to ISMTI (given the missing rate) when the missing rate ranges from 0 to 0.9. Therefore, when the missing rate is not given, ISMTI can achieve the expected performance. Besides, ISMTI does not need to add additional estimation protocols.

F. Impact of Channel Error

In the above analysis, the communication channel is considered to be error-free as in existing works [11], [13], [17]. However, channel errors may happen in many realistic scenarios. Similar to existing works that adopt bit-tracking technology [42], [43], the performance of SSMTI and ISMTI are mainly influenced by detection errors and capture effect. Specifically, detection errors are caused by the weak backscattering signal from some passive tags. In this case, the reader cannot tag signal and therefore misidentify these tags as missing. On the other hand, the difference in the distance between tags and the reader causes the signal strength of each tag to be different. When the signal strength of a tag is significantly stronger than other tags in a time slot, the reader can only detect this tag, thus causing the capture effect. Note that we do not consider bit errors like other RFID identification protocols [42], [43]. The reason is that in most indoor scenes where the distance between the reader and the tag is often less than 10 m, the probability of bit errors is less than 10^{-6} [44], which has a negligible impact on tag identification [42], [43].

In Fig. 9, we set the missing rate to 0.1 in Fig. 9(a) and 0.9 in Fig. 9(b) to evaluate the proposed protocols. Here the number of candidate tags \( N \) is 10,000. We can observe that the identification accuracy of the proposed protocols decreases when the capture effect and detection errors occur. This is because multiple existing tags in SSMTI and ISMTI transmit strings in the same time slot. When the capture effect happens, the reader can only identify one present tag and treat other tags as missing. Besides, the detection errors can also cause some present tags to be not detected by the reader. To improve identification accuracy, the reader can reduce the string length.
in each slot. Moreover, it is worth noting that the reader usually executes the identification protocol periodically. Therefore, these undiscovered tags have a high probability of being detected by the reader in the subsequent cycle. We can also observe that the identification accuracy of SSMTI and ISMTI becomes higher when the missing rate is high. This is because most actual time slots are empty slots, which are not affected by capture effects and detection errors. By using the proposed protocol in this scenario, the reader can identify multiple missing tags at once to significantly improve the identification efficiency and ensure high identification accuracy.

VIII. CONCLUSION

We investigated a critical problem of missing tag identification under different missing rates. Unlike most protocols that verify tags one by one in singleton slots, we exploit collision slots for tag verification and proposed three efficient missing tag identification protocols based on bit tracking technology. We first proposed the Sequential String based Missing Tag Identification (SSMTI) protocol, which converts all time slots to collision slots and enables multiple tags in each slot to simultaneously reply to a designed string. By adopting the bit tracking technology to decode the combined string, the reader can verify multiple tags together. To further accelerate the identification process under high missing rates, we proposed the Interactive String based Missing Tag Identification (ISMTI) protocol. Unlike SSMTI that arranges each tag to a unique bit of the string, multiple tags in ISMTI can be arranged to the same bit in the string so that the reader can identify more tags using a shorter string than SSMTI. Besides, the verification mechanism in ISMTI can be dynamically adjusted according to the missing rates. We also analyzed the parameter configuration of the proposed protocols to minimize the execution time. Numerical results show that the proposed protocols outperform state-of-the-art solutions in terms of communication complexity and time efficiency. In future work, we intend to investigate the rapid identification of some important tags using commercial RFID systems.

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