**OpSparse: A Highly Optimized Framework for Sparse General Matrix Multiplication on GPUs**

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**ABSTRACT**

Sparse general matrix multiplication (SpGEMM) is an important and expensive computation primitive in many real-world applications. Due to SpGEMM’s inherent irregularity and the vast diversity of its input matrices, developing high-performance SpGEMM implementation on modern processors such as GPUs is challenging. The state-of-the-art SpGEMM libraries (i.e., *nsparse* and *spECK*) adopt several algorithms to tackle the challenges of global load balance, local load balance, and allocation of the result matrix. While these libraries focus on the high-level algorithm design for SpGEMM, they neglect several low-level architecture-specific optimizations, which causes inefficient implementations in their libraries. In this paper, we classify their inefficient implementations into seven categories. Based on our observations, we propose a highly optimized SpGEMM library called *OpSparse*. The optimizations in *OpSparse* include 1) optimizing the binning method by improving the utilization of the shared memory, 2) optimizing the hashing method by reducing the access to the hash table, 3) improving the trade-off between hash collision rate and hardware utilization in the hashing method by setting appropriate binning ranges, 4) reducing the overheads of global memory utilization by minimizing the global memory usage of the metadata, and 5) improving the execution parallelism by overlapping global memory allocation with kernel execution. Performance evaluations with 26 commonly used matrices on an Nvidia Tesla V100 GPU show that *OpSparse* achieves up to 27.8×, 1.81×, and 2.04× performance speedup over three state-of-the-art libraries: *cuSPARSE*, *nsparse*, and *spECK*, respectively.

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# 1 Introduction

Sparse general matrix multiplication (SpGEMM) is widely used in many real-world applications such as algebraic multigrid solvers [1, 2], Markov clustering [3], multi-source breadth first search [4], molecular dynamics simulations [5], and finite element simulations based on domain decomposition [6].

The extensive use of SpGEMM in real-world applications has led to the development of several SpGEMM libraries on CPUs [8, 9, 10, 11], GPUs [12, 13, 14, 15], and accelerators [16, 17, 18, 19], targeting high-performance computing. This paper focuses on developing a high-performance SpGEMM library on GPUs.

The inherent irregularity and the vast diversity of the input matrices cause many challenges that hinder the performance of SpGEMM on GPUs. Irregularity is introduced by the condensed storage format used by the input and output matrices of SpGEMM, which causes challenges including dataflow selection, accumulator algorithm design, and load imbalance among sub-tasks. In addition, the hard-to-predict sparse structure of the output matrix makes its memory allocation in condensed storage format challenging, which further affects the performance of SpGEMM.

The state-of-the-art SpGEMM libraries (i.e., *nsparse* [14] and *spECK* [15]) adopt several algorithms to tackle the challenges of global load balance, local load balance, and memory allocation of the result matrix. While these libraries focus on the high-level algorithm design for SpGEMM, they neglect several low-level architecture-specific optimizations, which cause inefficient implementations in their libraries. For example, the excessive global memory accesses in the binning method, the excessive accesses to the hash tables in the hashing method, and the excessive global memory allocation for the metadata are inefficient implementations in their libraries. Moreover, the parallelism of global memory allocation and kernel execution, which can improve the performance of SpGEMM, is not utilized in these SpGEMM libraries.

In this paper, we identify seven kinds of inefficient implementations of two state-of-the-art SpGEMM libraries, i.e., *nsparse* and *spECK*. Then we propose optimizations for each of the inefficient implementations and integrate them into the proposed framework named *OpSparse*. According to our experiments on diverse sparse matrices, *OpSparse* achieves significant performance improvement over the libraries *nsparse* and *spECK*. We also conduct additional experiments to show the performance improvements of several individual optimizations to provide insights of the low-level architecture-specific optimizations of SpGEMM.

The key technical contributions of this work are as follows:

- We identify seven kinds of inefficient architectural implementations of two state-of-the-art SpGEMM libraries.
- We optimize all the identified inefficient implementations and propose a library named *OpSparse*, integrating all the optimizations we developed.
- We evaluate the performance of the proposed *OpSparse* framework on 26 commonly used benchmarks. The results show that the proposed *OpSparse* achieves on average $7.35 \times$ (up to $27.8 \times$), $1.43 \times$ (up to $1.81 \times$), and $1.52 \times$ (up to $2.04 \times$) speedups over three SpGEMM libraries *cuSPARSE*, *nsparse*, and *spECK*, respectively.

The rest of the paper is organized as follows. Section 2 and section 3 provide background and related work, respectively. Section 4 describes the inefficient implementations in the existing libraries. Section 5 describes the proposed SpGEMM framework (*OpSparse*) and the corresponding optimizations. Section 6 first shows the overall performance compared to three state-of-the-art libraries; then, it shows the performance improvements of several individual optimizations as compared to the baseline. Section 7 concludes this paper.

## 2 Background

In this section, we provide the background of SpGEMM algorithm on GPUs.

### 2.1 Row-wise SpGEMM

In SpGEMM, given two sparse input matrices $A$ and $B$, each element of the output matrix $C$ is computed as:

$$C_{ij} = \sum_k A_{ik} \cdot B_{kj},$$  (1)
where \( i \) and \( j \) are the row and column indices of the nonzero elements of \( A \) and \( B \), respectively, and \( k \) is the set of the colliding indices.

One variation of the above computation pattern of SpGEMM is:

\[
C_{i*} = \sum_k A_{ik} \cdot B_{k*},
\]

(2)

where \( C_{i*} \) and \( A_{i*} \) represent all the nonzero elements in the \( i_{th} \) row of \( C \) and \( A \), respectively, \( k \) belongs to the set of column indices of the nonzero elements in the \( i \)th row of \( A \), and \( B_{k*} \) represents all the nonzero elements in the \( k_{th} \) row of \( B \).

Equation (2) describes the row-wise dataflow to perform SpGEMM. The row-wise dataflow is commonly adopted in the state-of-the-art SpGEMM libraries [12, 13, 14, 15]. There are three key benefits of the row-wise dataflow: 1) zero elements are completely avoided in both computation and memory access, 2) the computation of each output row is independent of each other; therefore, the row-wise SpGEMM can be easily parallelized, and 3) accumulating the intermediate products of each output row has good temporal locality.

2.1.1 CSR storage format

The compressed sparse row (CSR) storage format is one of the most commonly used sparse storage formats for SpGEMM, which is adopted by state-of-the-art SpGEMM libraries such as cuSPARSE [12], nsparse [14], and spECK [15]. In this paper, we also choose CSR as the storage format of the input and output matrices in the proposed SpGEMM framework.

Fig. 1 illustrates the CSR storage format. The CSR consists of three arrays to record the nonzero elements and their corresponding indices. The \( \text{val} \) and \( \text{col} \) array record the nonzero elements and their corresponding column indices in a sorted row-major and column-major order. The lengths of \( \text{val} \) and \( \text{col} \) arrays are both the number of nonzero elements \( (n_{nz}) \) of the sparse matrix. The \( \text{rpt} \) array records the start and end positions for each row’s values and column indices in the \( \text{val} \) and \( \text{col} \) arrays. Since the \( i_{th} \) row’s end positions can be encoded the same as the \( (i + 1)_{th} \) row’s start positions in the \( \text{rpt} \) array, the \( \text{rpt} \) array is further compressed to \( M + 1 \) entries, where \( M \) is the number of rows of the matrix.

One of the key performance benefits of using CSR is that it is easy to access the elements of an entire row.

![Figure 1: Illustration of the CSR storage format. Left: matrix A in the dense storage format. Right: matrix A in the CSR storage format](image-url)

2.1.2 Compression ratio (CR)

In row-wise SpGEMM, each output row is computed by accumulating multiple intermediate products. The compression ratio represents the average number of intermediate products for one nonzero element in the result matrix. Therefore, the compression ratio can be calculated by dividing the total number of intermediate products \( (n_{prod}) \) in performing row-wise SpGEMM by the result matrix’s total number of nonzero elements \( (n_{nz}) \) (Equation (3)).

\[
\text{Compression ratio} = \frac{\text{Total } n_{prod} \text{ to compute } C}{\text{Total } n_{nz} \text{ of } C}.
\]

(3)

2.2 One-phase SpGEMM and two-phase SpGEMM

One of the critical issues in row-wise SpGEMM design is that the number of nonzero elements of the result matrix is not known before calculating the result matrix. To tackle such an issue, both one-phase [13] and two-phase [12, 10, 14, 15] methods are used.

To avoid ambiguity, we only discuss the one-phase and two-phase methods when applying the row-wise dataflow and the CSR storage format in SpGEMM. The two-phase method consists of the symbolic and numeric phases, in which
the numeric phase depends upon the result from the symbolic phase. In the symbolic phase, the row size (number of nonzero elements of a row) of each output row is computed with the indices information of the two input matrices. Multiplication operation is avoided in the symbolic phase. After the symbolic phase, the total number of nonzero elements of the result matrix is computed based on the row sizes. Then the memory for the column indices and values of the result matrix is allocated. In the numeric phase, each output row’s column indices and values are calculated and stored in the allocated memory space.

In contrast, the one-phase method computes the row sizes, column indices, and values of the result matrix simultaneously. However, due to the unknown memory size of the result matrix, the memory space for storing the column indices and values of the result matrix cannot be precisely allocated in advance. As a result, temporary memory space is required in the one-phase method. The size of the temporary memory space is defined by either estimating the upper-bound row sizes of the result matrix [13] or using dynamic allocation when needed [8]. The former may result in over-allocation, and the latter is not feasible for GPUs [10] (due to the high cost-to-benefit ratio of allocating small-footprint memory in GPUs). Moreover, the one-phase method additionally requires two time-consuming operations: 1) allocating the temporary memory space to store the result matrix, and 2) copying the result matrix from the temporary memory space to the standard CSR memory space.

3 Related work

Researchers have proposed many approaches to improve the performance of SpGEMM on GPUs. We introduce several approaches that use the row-wise and two-phase methods to perform SpGEMM on GPUs.

Demouth proposed the cuSPARSE [12] library, which uses the two-phase method to implement SpGEMM. The memory usage for the C matrix is efficient. However, cuSPARSE use the naive load balance method for the computation. They compute all the output rows in the same way (one kernel for the symbolic phase and one kernel for the numeric phase) despite the varying \( n_{\text{prod}} \) (or \( n_{\text{nz}} \)) per output row. Consequently, their implementation may suffer from severe load imbalance issues. cuSPARSE uses hashing method to compute the result row. However, the implementation of their hashing method is inefficient. Specifically, because cuSPARSE computes all the output rows with the same kernel, the kernel implements both shared memory and global memory hash tables to compute the rows with varying \( n_{\text{prod}} \) (or \( n_{\text{nz}} \)). Therefore, the keys can first be inserted into the shared memory hash table for fast access speed. However, when insertion to the shared memory hash table fails, it switches to the global memory hash table and recomputes the failed row. This implementation causes recomputations of several rows and potentially inefficient utilization of the hardware resources for the shared memory hash tables.

Nagasaka et al. proposed nsparse [14], which improves the global load balance issue by using multiple kernels to compute the output rows with varying \( n_{\text{prod}} \) (or \( n_{\text{nz}} \)). Specifically, nsparse first groups rows into multiple bins by their \( n_{\text{prod}} \) (or \( n_{\text{nz}} \)), then it computes the rows in each bin with a more appropriate kernel. For better thread utilization, combines two thread assignment methods. When computing tiny rows, nsparse uses a sub-warp instead of a whole thread block to compute each row and extracts an entire row in B by one thread. When computing other rows, nsparse uses a thread block to compute each row and extracts an entire row in B by a warp (32 threads). In general, nsparse achieved high performance on many commonly used benchmarks and showed an efficient framework for SpGEMM on GPUs. However, there are still several inefficient implementations in nsparse’s library, limiting its performance. We identify and optimize them in section 4 to section 5.

Parger et al. proposed spECK [15] to improve the performance of the two-phase SpGEMM. In addition to the hashing accumulator, spECK also uses the dense accumulator and the single-row accumulator to improve the performance when computing particular rows. For example, it uses the dense accumulator to compute rows with extremely large \( n_{\text{nz}} \). Moreover, spECK introduces the local load balance method by which the number of threads to extract the rows in B is dynamically determined. To guide their global and local load balance and selection of accumulator methods, spECK introduces an additional lightweight row analysis on the two input matrices. In this paper, we do not adopt the local load balance method and the multiple accumulator methods. The performance improvement of our optimizations is orthogonal to the performance improvement of adopting these two methods.

4 Inefficient implementations in the existing libraries

There are multiple inefficient implementations in the state-of-the-art SpGEMM libraries, limiting their performance nontrivially. We classify these inefficient implementations into seven categories and describe them in detail.
4.1 Binning method

The binning method implements the global load balance for the symbolic and the numeric phases [14][15]. The primary function of the binning method is to classify rows into different bins/groups. One important task of the binning method is to count the bin size by the atomic operation. However, existing libraries perform massive atomic operations directly on the global memory, which is inefficient. Considering the cost of the binning steps, our performance profiling shows that the execution time of the binning method in nsparse and spECK takes more than 10% of the overall execution time in many benchmarks (shown in Fig. 7 in section 6.3.1). Note that the complexity of the binning method is only $O(M)$, where $M$ is the number of rows.

4.2 Hashing method

The hashing method efficiently implements the accumulator in SpGEMM due to its good parallelism on GPUs [14][15]. Therefore, the hashing method is massively used in both nsparse and spECK. Nevertheless, the hashing operation is one of the most time-consuming operations [14] in SpGEMM.

One performance-critical operation in the hashing method is accessing the hash table with an inherently random access pattern. The inefficient implementation of the hashing method in nsparse and spECK is that they access the hash table too often, which may cause too many bank conflicts in the shared memory due to the random access.

4.3 Binning range selection

The state-of-the-art SpGEMM libraries adopt row-wise and hashing methods to implement SpGEMM. One of the most important tasks in their implementation is choosing an appropriate hash table size to compute each output row. To make this choice appropriately, the trade-off between hash collision rate and hardware resource utilization needs to be carefully considered. Specifically, the computing kernels are configured with a pre-defined hash table size. If the pre-defined hash table size in a kernel equals the largest $n_{\text{prod}}$ (or $n_{\text{nz}}$) of the rows computed by that kernel (potentially full occupancy of the hash table), the hash collision rate can be very high. However, the implementation can achieve high hardware resource utilization. In contrast, if the hash table size is kept unchanged, when computing rows with smaller $n_{\text{prod}}$ (or $n_{\text{nz}}$), it is observed that the hash collision rate decreases significantly. However, the hardware resource utilization also decreases.

Analytical models for choosing the appropriate hash table size to $n_{\text{prod}}$ (or $n_{\text{nz}}$) ratio could be difficult due to the entangled effects of hardware parameters and sparse matrix properties. However, to the best of our knowledge, the experimental exploration of this design choice was also missed in existing libraries. nsparse computes the rows with potentially full occupancy of their hash table, yielding a huge hash collision rate. spECK noticed the hash collision issue and used a larger hash table size for the numeric phase such that the largest occupancy of the hash table is 2/3. However, spECK did not demonstrate if this configuration is experimentally best. This paper experimentally explores the design choice of the binning range selection and finds a general best configuration in section 6.3.3.

4.4 Global memory usage for metadata

To perform SpGEMM efficiently on GPUs, recording some metadata in the global memory is necessary. For example, rows are classified into multiple bins/groups for good global load balance [14][15]. The classified row ids should be stored in the global memory as metadata to be used in the following computation steps.

Our micro-benchmarking shows that the global memory allocation is much more expensive than memory access in execution time. For example, the bandwidth of allocating 4MB of global memory is roughly 13.7GB/s, whereas accessing global memory with the same size achieves 124GB/s on the NVIDIA Tesla V100 GPUs. Therefore, minimizing the global memory usage should be considered and even prioritized when designing the SpGEMM algorithm. However, the existing SpGEMM libraries [14][15] allocated too much global memory for the metadata in their implementations, which affect their performance.

In nsparse, the majority of metadata is used to store 1) the classified row ids in the binning method and 2) the $n_{\text{prod}}$ and $n_{\text{nz}}$ information. nsparse allocates two arrays of size $M$ to store them. We observe that the array to store the $n_{\text{prod}}$ and $n_{\text{nz}}$ information can be reduced by sharing the $C.rpt$ array. In spECK, the majority of metadata is used to store the classified row ids in the binning method. Unlike nsparse, spECK uses a two-dimensioned array of size $M \times \text{NUM\_BIN}$ to store the classified row ids, where $\text{NUM\_BIN}$ is the number of the classified bins. spECK allocates much more metadata than nsparse.
4.5 Overlapping of global memory allocation and kernel execution

By using NVIDIA’s profiling tool Nsight Systems [25] in our GPU program profiling, we observe that when the host executes `cudaMalloc` [28] to allocate global memory, the already launched kernels can execute normally on the device without performance loss. In other words, the global memory allocation executed on the host machine can be parallelized (overlapped) with the kernel execution on the device machine. We denote this feature as the memory allocation and kernel execution parallelism. Note that executing `cudaMalloc` on the host usually takes much longer time than launching a kernel.

Existing SpGEMM libraries [14, 15], however, did not utilize this parallelism feature to improve the performance of SpGEMM. For example, in the symbolic and numeric phases, both nsparse and spECK first allocate the global memory for hash tables and then launch other computing kernels. In typical benchmarks, the performance overhead of allocating the global memory is significant. Therefore, lack of memory allocation and kernel execution overlapping can waste a large amount of GPU resources.

4.6 Load imbalance of the streaming multiprocessors

NVIDIA’s GPUs usually have a few dozens of streaming multiprocessors (SMs) that can accommodate hundreds to thousands of thread blocks simultaneously. Therefore, either the insufficient number of thread blocks or varying execution durations of the thread blocks in SpGEMM may cause the load imbalance of the SMs, which limits the performance of SpGEMM.

In the row-wise SpGEMM, each output row can be computed independently. Therefore, the execution order of the multiple kernels in the symbolic and numeric phases does not affect the accuracy of SpGEMM. nsparse reported that they launched the kernels concurrently with multiple CUDA streams to tackle the possible insufficient number of thread blocks when computing small matrices [14].

However, when nsparse launched the kernel that computes the largest rows with global memory hash tables, it immediately called the `cudaFree` [28] to release the global memory before launching other kernels. Since `cudaFree` implicitly invokes `cudaDeviceSynchronize` [28], when the kernel that computes the largest rows is executing on a few SMs, many other kernels are not yet launched for execution, causing a significant load imbalance among the SMs. spECK optimized this problem in their source code [23] by calling the `cudaFree` in the last phase. However, details of this optimization are missing in their paper [15].

4.7 Full occupancy of the kernels

When executing a GPU program, the high device memory access latency is hidden by switching warp execution within one streaming multiprocessor (SM). A kernel can have more opportunities to hide its memory access latency by having more warps located on one SM. The theoretical full occupancy of a kernel is achieved when the maximum number of threads are resident on one SM, which is 2048 in current NVIDIA GPUs [27].

Although up to 2048 threads can be executed on one SM in theory, the number of computing resources (e.g., FP64 cores [24]) is much less than 2048. Therefore, for a computation-bounded [20] kernel where few memory accesses are needed, a relatively low occupancy may achieve similar performance as compared to the full occupancy counterpart. However, since SpGEMM is a typical memory-bounded application with an irregular memory access pattern, occupancy is critical for its performance.

Moreover, when profiling the occupancy of the existing SpGEMM libraries [14, 15] by using NVIDIA’s profiling tool Nsight Compute [26], we find that the achieved occupancy of the kernels in the symbolic and numeric phases is nearly always larger than 90% when the kernel is configured with theoretical full occupancy. This practically shows that occupancy is playing a vital role in performing SpGEMM.

However, although nsparse and spECK mentioned the occupancy issue, they did not prioritize achieving theoretical full occupancy in the design goals of their kernels. As a result, many kernels in nsparse and spECK did not achieve the theoretical full occupancy [22, 23], limiting their performance.

5 OpSparse

To cope with the inefficient implementations of the existing SpGEMM libraries, we propose our optimized SpGEMM framework OpSparse in this section. We first describe the overall computation flow of OpSparse and then describe multiple optimizations.
The overall computation flow is illustrated in Fig. 2 with mainly six steps. Our computation flow is similar to nsparse in that it adopts the row-wise, and two-phase methods to perform SpGEMM on GPUs. Two main computation steps are the symbolic and numeric steps (step3 and step5), which compute the \( n_{nz} \), and the result column indices and values per output row, respectively. We only use hashing method to calculate the \( n_{nz} \) and the result matrix in the two main computation steps. To achieve good global load balance, the two main computation steps are each equipped with a binning step (i.e., the symbolic binning step and the numeric binning step). Before the numeric step, we compute the total \( n_{nz} \) and allocate the \( C.col \) and \( C.val \) arrays for the result matrix. We also compute the \( C.rpt \) array by the exclusive-sum operation on the computed \( n_{nz} \) information. In the setup step, we allocate the \( C.rpt \) array, allocate the necessary device and host memory for the metadata used in SpGEMM, and compute the \( n_{prod} \) per output row used in the symbolic binning step. Moreover, we create multiple CUDA streams \([28]\) in the setup phase used for the concurrent kernel execution \([27]\) in step3 and step5. In the final cleanup step, we release the allocated memory for the metadata and destroy the created CUDA streams.

Note that, in the symbolic and numeric steps, there are multiple kernels to compute rows with different \( n_{prod} \) (or \( n_{nz} \)). We use multiple CUDA streams to launch these kernels concurrently.

5.1 Efficiently utilizing the shared memory for the binning method

The binning method is used in the two binning steps, which classify the rows into different bins for good global load balance. The binning method requires metadata to record its result, such as the classified row ids. Fig. 3 illustrates our implementation of the binning methods that minimizes the memory usage for the metadata.
Our implementations of the symbolic binning and numeric binning steps are the same, only with a difference in the input data. The symbolic binning step takes the $n_{\text{prod}}$ information as input, whereas the numeric binning step takes the $n_{nz}$ information. Therefore, the metadata used for the two binning steps is also shared to minimize the metadata usage further.

Since we aim to store the classified row ids in one array of length $M$ and we do not know each bin’s size and offset (Fig. 2), we need a two-pass computation method to implement the binning method. In the first pass (Algorithm 1), the bin sizes are counted. And then, the bin offsets are computed by exclusive-sum operation on the bin sizes. In the second pass (Algorithm 2), the offset position for each bin is known, and the classified row ids are written to their appropriate positions in the $bins$ array.

Algorithm 1 Binning method (first pass)

1: // Set $d_{bin\_size}$ to all zeroes before this kernel execution
2: $i = tid + blockIdx \cdot blockDim$
3: Initialize $r\_range[NUM\_BIN]$ in registers
4: Initialize $s_{bin\_size[NUM\_BIN]}$ to zeros in shared memory
5: Initialize $s_{max\_row\_nnz[0]}$ to zero
6: atomicMax($s_{max\_row\_nnz, nnz[i]}$)
7: for $j = 0$ to $NUM\_BIN - 1$
8: \hspace{1em} if $nnz[i] \leq r\_range[j]$
9: \hspace{2em} atomicAdd($s_{bin\_size} + j, 1$)
10: \hspace{1em} goto Label
11: end if
12: end for
13: Label:
14: syncthreads
15: if $tid < NUM\_BIN$
16: \hspace{1em} atomicAdd($d_{bin\_size} + tid, s_{bin\_size[tid]}$
17: end if
18: if $tid == 0$
19: \hspace{1em} atomicMax($d_{max\_row\_nnz, s_{max\_row\_nnz[0]}$)
20: end if

Atomic operations should be used when computing the bin size and bin offset in the two binning kernels (Algorithm 1 and Algorithm 2) since the bin size (Line 9 in Algorithm 1, Line 8 in Algorithm 2) and bin offset (Line 24 in Algorithm 2) are processed by multiple threads. Our algorithms fully utilize the shared memory to process the bin sizes and the bin offsets by atomic operations to improve the performance.

Furthermore, we also utilize shared memory to monitor the max $n_{\text{prod}}$ (or $n_{nz}$) information in the first pass (Line 6 in Algorithm 1). If all the $n_{\text{prod}}$ (or $n_{nz}$) can be classified into the smallest bin (bin0), we save the comparison operations in the second pass by directly setting the $bins$ array as increasing row ids with another kernel (Algorithm 3). The overall computation flow of our binning method is shown in Fig. 3.

5.2 Reducing the accesses to the hash table for the hashing method

In the row-wise and hashing SpGEMM, each output row is computed with one hash table. The hash table is initialized to all 0 representing unoccupied status since the column indices (key) will be no less than 0. To determine the address to insert the key into the hash table, the key is multiplied with a constant integer $HASH\_SCALE$, and then the result is mod-ed with the hash table size as the initial address (hash). However, the hash of different keys can be the same, referred to as the hash collision issue. When the hash collision occurs, we increment the hash by one until an unoccupied place in the hash table is found. Another situation is that there may be multiple duplicated keys when computing one result element. When duplicated keys are detected in the symbolic step, the $n_{nz}$ should only be incremented in the first occurrence of the duplicated keys. In contrast, when duplicated keys are detected in the numeric step, the values with the same duplicated keys should be accumulated together to generate one final element.

Algorithm 4 and Algorithm 5 show our proposed hashing method in the symbolic and numeric steps, respectively. We introduce one optimization in our hashing method. In each iteration in the while loop, we access the hash table only once to minimize the access to shared memory hash tables, reducing the bank conflicts of the shared memory. We use atomic compare and swap (atomicCAS) to access the hash table and store the swapped result in a register, which is reused in the following computation.
Algorithm 2 Binning method (second pass)

1: // Set d_bin_size to all zeroes before this kernel execution
2: // d_bin_offset is already computed
3: i = tid + blockIdx * blockDim
4: Initialize r_range[NUM_BIN] in registers
5: Initialize s_bin_size[NUM_BIN] to zeros
6: for j = 0 to NUM_BIN - 1 do
7:   if nnz[i] ≤ r_range[j] then
8:     atomicAdd(s_bin_size + j, 1)
9:   goto Label
10: end if
11: end for
12: Label:
13: syncthreads
14: // Compute s_bin_offset
15: if tid < NUM_BIN then
16:   s_shared_offset[tid] = atomicAdd(d_bin_size + tid, s_bin_size[tid])
17:   s_bin_offset[tid] += d_bin_offset[tid]
18: end if
19: Reset s_bin_size[NUM_BIN] to zeros
20: syncthreads
21: // Write row ids to d_bins
22: for j = 0 to NUM_BIN - 1 do
23:   if nnz[i] ≤ r_range[j] then
24:     r_index = atomicAdd(s_bin_offset + j, 1)
25:     d_bins[r_index] = i
26:   return
27: end if
28: end for

Algorithm 3 Binning method (small)

1: i = tid + blockIdx * blockDim
2: d_bins[i] = i

Figure 4: Overall computation flow of our binning method
### Algorithm 4 Hashing method in the symbolic step

1: Initialize `shared_table` to $-1$
2: Initialize `shared_nnz[0]` to 0
3: Obtain the `key` the same way as `nsparse`
4: $hash = key \times HASH\_SCALE \mod (t\_size - 1)$
5: while `true` do
6:   $old = \text{atomicCAS}(shared\_table + hash, -1, key)$
7:   if $old == -1$ then
8:     \text{atomicAdd}(shared\_nnz, 1)
9:     break
10:   else if $old == key$ then
11:     break
12:   else
13:     $hash = (hash + 1) \& (t\_size - 1)$
14:   end if
15: end while

### Algorithm 5 Hashing method in the numeric step

1: Initialize `shared\_col` to $-1$
2: Initialize `shared\_val` to 0
3: Obtain the `key`, `aval`, and `bval` the same way as `nsparse`
4: $hash = key \times HASH\_SCALE \mod t\_size$
5: while `true` do
6:   $old = \text{atomicCAS}(shared\_col + hash, -1, key)$
7:   if $old == -1$ || $old == key$ then
8:     \text{atomicAdd}(shared\_val + hash, aval \times bval)
9:     break
10:   else
11:     $hash = hash + 1 < t\_size ? hash + 1 : 0$
12:   end if
13: end while

When the hash table size ($t\_size$) in hashing method is a power-of-two number, the mod operation can be mathematically replaced with the logic-and operation \[12\] (Line 4 and Line 13 in Algorithm 4). We utilize the logic-and operation since it is executed faster than the mod operation on GPUs. In the symbolic step, we keep most of the $t\_size$s as power-of-two numbers and use the logic-and operation to improve performance. However, in the numeric step, we do not set the $t\_size$ as power-of-two numbers for performance gains by full occupancy, detailed in section 5.6.2. Consequently, we use mod operation in the numeric step (Line 4 in Algorithm 5).

### 5.3 Minimizing global memory usage for the metadata

The metadata usage in our implementation only comes from the two binning steps and the exclusive-sum task in step5. How we minimize the metadata usage for the binning method has been described in section 5.1 when introducing the binning method. For the exclusive-sum task, we use the highly optimized `cub :: DeviceScan :: ExclusiveSum` API \[29\] to implement it. The CUB library defines the required global memory usage to store its intermediate result. Our profiling shows that the size of the memory usage in the CUB library `cub :: DeviceScan :: ExclusiveSum` can be computed with low cost ($\sim 1.2us$) before computing the real results of the exclusive-sum operation \[29\].

Although the computed $n\_prod$ in the setup step and the computed $n\_nz$ in the symbolic step also need memory to store their results, we save the memory usage of the $n\_prod$ and $n\_nz$ information by reusing the `C.rpt` array. The reasons are four-fold. 1) The size of the `C.rpt` array is easily obtained as $M + 1$, where $M$ is the number of rows of the $A$ matrix; therefore, the `C.rpt` array can be allocated before computing the $n\_prod$ and $n\_nz$. 2) The $n\_prod$ and $n\_nz$ information are computed in different steps; therefore, they can be shared with the same memory space. 3) The memory size for $n\_prod$ or $n\_nz$ is $M$, which is smaller than the memory size of the `C.rpt` array. 4) The `C.rpt` array can be used by $n\_prod$ or $n\_nz$ since the `C.rpt` array is not used for its original purpose until step4. Note that when computing the `C.rpt` array in step4, the `cub :: DeviceScan :: ExclusiveSum` library can compute the exclusive-sum operation in-place.
Furthermore, since the required size of all the metadata is known in our implementation before performing SpGEMM, we sum them up and allocate them together with one `cudaMalloc` call to further reduce the overheads of global memory allocation. As a result, our memory usage for the metadata is self-managed.

5.4 Overlapping memory allocation with kernel execution

There are multiple computation steps where we can overlap the kernel execution with global memory allocation. In the setup step, we need to allocate global memory for metadata and compute the \( n_{prod} \) information. The two tasks do not have a logical dependency. Therefore, we first launch the kernel to compute \( n_{prod} \) and then allocate the global memory for the metadata without waiting for the kernel computation to finish. This execution sequence is shown in Fig. 2.

In step 5, we first compute the total \( n_{nz} \) within the first pass of the numeric binning method. Then we launch the second pass of the binning method and the exclusive sum interleaved with the two memory allocations for the \( C.col \) and \( C.val \) array (Fig. 2). Note that we make sure the exclusive-sum operation is computed after the two passes of the numeric binning step because we reuse the \( C.rpt \) array to record the \( n_{nz} \) information.

In the symbolic and numeric steps, there may be global memory allocation for the hash table to compute extremely large rows. Since the kernels that use shared memory hash tables do not depend on the global memory allocation, we first launch one kernel that uses a shared memory hash table and then allocate the global memory immediately. As a result, part or all of the execution time of the memory allocation is parallelized with the pre-launched kernel execution.

5.5 Load balance of the streaming multiprocessors

The load imbalance of SMs in our implementation may occur in the symbolic and numeric steps since rows are computed on different SMs with varying execution time.

One attribute of the concurrently-launched kernels is that the thread blocks in the earlier launched kernel still execute earlier than or concurrently with the thread blocks in the later launched kernels. Therefore, to achieve a good load balance of the SMs, our implementation launches kernels that compute large rows relatively earlier and launch kernels with the smallest thread block size in the last phase. Moreover, we do not call `cudaFree`, which implicitly invokes `cudaDeviceSynchronize` until all kernels have been launched with multiple CUDA streams.

5.6 Kernel configuration

This section describes how we configure the kernel’s parameters to achieve theoretical full occupancy for the symbolic and numeric steps. Nevertheless, some kernels are configured with theoretically 50% occupancy for maximum shared memory usage.

Our implementation targets the NVIDIA Tesla V100 GPUs, which implement several dozens of SMs on one GPU. Each SM has maximumly 96KB shared memory, and the maximum thread block size for a kernel is 1024. For NVIDIA’s GPU, the theoretical occupancy is affected by register usage, thread block size, and shared memory usage. We use the `__launch_bounds__` compiler directive to force the register usage of the kernels to meet the requirement of theoretical full occupancy. We describe how we set each kernel’s shared memory usage and thread block size as follows.

5.6.1 Kernel configuration in the symbolic step

We divide the rows with different \( n_{prod} \) into 8 bins for computation by 9 kernels in the symbolic step. Table 1 shows the kernels’ parameter settings and the \( n_{prod} \) range in the symbolic step on NVIDIA Tesla V100 GPU. The rows in bin0–bin6 are computed by the corresponding kernel0–kernel6, and each bin is computed by one kernel. The rows in bin7 are firstly computed by kernel7. When the computed \( n_{nz} \) of any row exceeds a threshold value, the row id is recorded, and the row is recomputed by kernel8. We set the threshold value as 0.8 times the kernel7’s hash table size. Kernel0–kernel7 implements shared memory hash tables, and kernel 8 implements global memory hash tables.

Kernel0 computes multiple rows in one thread block, which means there are multiple hash tables in one thread block. In contrast, kernel1–kernel8 compute one row in each thread block. We first describe the shared memory usage and thread block size configuration in kernel1. The kernel1’s thread block size is the minimum thread block size, which is 64. Therefore, one SM can contain 2048/64 = 32 thread blocks, which requires 32 hash tables. Since each column index needs 4 bytes, the largest hash table size \( t_{size} \) can be set as 96KB/32/4KB = 768. We set the \( t_{size} \) as 512 to utilize the lightweight logic-and operation in the hashing method (Algorithm 1). We also use an additional 4 bytes of shared memory as `shared_rows` to count the \( n_{nz} \) per row. With the above configuration, kernel1 achieves theoretical full occupancy. Then we double the \( t_{size} \) and thread block size in the following kernel2–kernel5 so that they all achieve theoretical full occupancy.
Table 1: Parameter setting and binning ranges for the symbolic step on NVIDIA’s Tesla V100 GPU

| Bins | Kernels | Table size | TB size    | Ranges (Sym_1.2x) |
|------|---------|------------|------------|-------------------|
| Bin0 | Kernel0 | 32         | 4 \cdot 256 = 1024 | 0 – 26            |
| Bin1 | Kernel1 | 512        | 64         | 27 – 426          |
| Bin2 | Kernel2 | 1024       | 128        | 427 – 853         |
| Bin3 | Kernel3 | 2048       | 256        | 854 – 1706        |
| Bin4 | Kernel4 | 4196       | 512        | 1707 – 3413       |
| Bin5 | Kernel5 | 8192       | 1024       | 3414 – 6826       |
| Bin6 | Kernel6 | 12287      | 1024       | 6827 – 10240      |
| Bin7 | Kernel7 | 24575      | 1024       | 10241 – ∞         |

Kernel6 is configured with the maximum thread block size, which is 1024. It uses (48K-4) bytes and 4 bytes of shared memory to implement the hash table and \( \text{shared\_nnz} \). Therefore, two thread blocks of 2048 threads can reside on one SM, achieving theoretical full occupancy.

Kernel7 uses the maximum shared memory (96KB) to implement the hash table and \( \text{shared\_nnz} \), while the thread block size stays the maximum 1024. Therefore, kernel7 achieves theoretically 50% occupancy. Note that kernel7 computes the group of rows with the largest \( n_{prod} \). If the actual \( n_{nnz} \) for a particular row exceeds a threshold size, that row will be recorded and recomputed in kernel8. We configure kernel7 with maximum hash table size to compute more large rows so that they are not computed by a much more expensive global memory hash table in kernel8.

Kernel8 only uses 4 bytes of shared memory to implement \( \text{shared\_nnz} \), and the thread block size is set as 1024. Therefore, kernel8 achieves theoretical full occupancy.

Kernel0 computes multiple rows in one thread block. We use 4 threads to compute one row. Therefore, 2048/4 = 512 rows can be computed in one SM, which requires 512 hash tables on one SM. The largest \( t_{size} \) is 96KB/512/4B = 48. Similar to the configuration in kernel1–kernel5, we set the \( t_{size} \) as 32 and use an additional 4 bytes of shared memory to store the \( \text{shared\_nnz} \) information.

Kernel1–kernel6 implement shared memory hash tables, and kernel7 implements global memory hash tables.

5.6.2 Kernel configuration in the numeric step

In the numeric step, we divide the rows with different \( n_{nnz} \) into 8 bins for computation by 8 kernels. Table 2 shows the kernels’ parameter settings and the \( n_{nnz} \) range on NVIDIA Tesla V100 GPU. The rows in bin0–bin7 are computed by the corresponding kernel0–kernel7, and each bin is computed by one kernel. kernel0–kernel6 implements shared memory hash tables, and kernel7 implements global memory hash tables.

Table 2: Parameter setting and binning ranges for the numeric step on NVIDIA’s Tesla V100 GPU

| Bins | Kernels | Table size | TB size    | Ranges (Num_2x) |
|------|---------|------------|------------|----------------|
| Bin0 | Kernel0 | 31         | 8 \cdot 128 = 1024 | 0 – 16         |
| Bin1 | Kernel1 | 255        | 64         | 17 – 128       |
| Bin2 | Kernel2 | 511        | 128        | 129 – 256      |
| Bin3 | Kernel3 | 1023       | 256        | 257 – 512      |
| Bin4 | Kernel4 | 2047       | 512        | 513 – 1024     |
| Bin5 | Kernel5 | 4095       | 1024       | 1025 – 2048    |
| Bin6 | Kernel6 | 8191       | 1024       | 2049 – 4096    |
| Bin7 | Kernel7 | -          | 1024       | 4097 – ∞       |

The kernels in the numeric phase consist of three computing phases: hashing, condensing, and sorting. The hashing phase computes the values and column indices of the output matrix by utilizing the hash table. In double-precision, each value and column index pair requires 12 bytes of memory. After the hashing phase, the values and column indices are stored sparsely in the hash table being unsorted. The condensing phase gathers the sparsely stored values and column indices with multiple threads. When a thread carries valid data, it atomically increments an offset variable and then stores the valid data to the position pointed by the offset variable. We use 4 bytes of shared memory to implement this offset variable named \( \text{shared\_offset} \). The last sorting phase sorts the nonzero values in the condensed hash map and stores them in global memory.

Kernel0 computes multiple rows in one thread block, which means it implements multiple hash tables in one thread block. In contrast, kernel1–kernel7 computes one row in each thread block. We first describe the shared memory usage.
and thread block size configuration in kernel1. The kernel1’s thread block size is set as the minimum thread block size, which is 64. Therefore, one SM can contain 2048/64 = 32 thread blocks, which requires 32 hash tables. Since each value and column index pair requires 12 bytes in double precision. The largest table size $t_{size}$ is 96KB/64/12B = 256. Our algorithm sets the $t_{size}$ in kernel1 as 255, so that additional 4 bytes of shared memory can be used to implement the shared_offset. With the above configuration, kernel1 achieves theoretical full occupancy. The kernel2–kernel5 are configured similarly to kernel1 with doubled $t_{size}$ and thread block size. Therefore, kernel2–kernel5 all achieve theoretical full occupancy.

Kernel6 uses the maximum shared memory (96K bytes) to implement the hash table and shared_offset, while the thread block size is the maximum 1024. Therefore kernel6 achieves theoretical 50% occupancy. We sacrifice half occupancy in kernel6 so that more rows can be computed by kernel6 with the shared memory hash table rather than kernel7 with the global memory hash table.

Kernel7 only uses 4 bytes of shared memory to implement shared_offset, and the thread block size is set as 1024. Therefore, Kernel7 achieves theoretical full occupancy.

Kernel0 computes multiple rows in one thread block. Our algorithm sets 8 threads to compute each row. Therefore, maximum 2048/8 = 256 rows are computed in one SM, which requires 256 hash tables. The largest $t_{size}$ is 96KB/256/12B = 32. Similar to kernel1–kernel5, we set the $t_{size}$ as 31 and use the additional 4 bytes of shared memory to implement the shared_offset information. Kernel0 achieves theoretical full occupancy.

5.7 Binning range selection

We have implemented the binning method and determined the hash table size and thread block size for all the computation kernels. This section describes the binning range selection with which each row with varying $n_{prod}$ (or $n_{nz}$) is assigned to the appropriate kernel.

In the symbolic step, we keep the hash table size of each kernel at least $1.2 \times$ larger than the largest $n_{prod}$ in the corresponding group. In the numeric step, we keep the hash table size of each kernel at least $2 \times$ larger than the largest $n_{nz}$ in the corresponding group. Our binning ranges for symbolic and numeric steps are given in Table 1 and Table 2, respectively. These binning ranges are demonstrated with generally better performance than other binning ranges through our experiments which will be shown in section 6.3.3.

6 Performance evaluation

We compare the overall performance with three state-of-the-art SpGEMM libraries cuSPARSE, nsparse, and spECK. We also provide individual performance analysis of our multiple optimizations and mainly compare them with ourselves in different implementation versions. The evaluation is based on the FLOPS performance of the matrix square benchmarks [13, 14, 15], which is twice the number of the intermediate products divided by the execution time. The execution time is obtained by first executing the program once for warmup, then executing the program ten times to obtain an average execution time. In all benchmarks, we measure the execution time of the approaches in double precision.

6.1 Evaluation environments

We select 26 square matrices from the SuiteSparse Matrix Collection [21], which are commonly used for the performance evaluation of SpGEMM on GPUs [13, 15]. The detailed information of these matrices are summarized in Table 5. Due to limited device memory capacity, cuSPARSE cannot compute 7 matrices at the bottom in Table 5. Therefore, we denote the top 19 matrices in Table 5 as normal matrices and the bottom 7 matrices in Table 5 as large matrices.

For a fair comparison, we evaluate the performance of both our approach and others with the same hardware and software settings. NVIDIA Tesla V100 PCI-e GPU is used for the evaluation, which has 16GB device memory, and up to 900GB/s memory bandwidth. The code is compiled by nvcc with version 11.2, and the optimization level is O3. The code runs on the ubuntu 18.04.5 LTS operating system on a Intel Xeon Platinum 8163 CPU.

6.2 Performance of SpGEMM

Since spECK does not include the overheads of allocating the $C$ matrix in their benchmarking [15], we slightly modify their source code to include the overheads of allocating $C$. Note that the overheads of allocating $C$ is included in all the other SpGEMM libraries, including ours. The nsparse’s source code [22] provides a Volta version of their SpGEMM implementation. We use their Volta version for the performance evaluation. The source code of our
| Id  | Name          | Rows       | Nnz   | Nnz/row | Max nnz/row | Nprod of $A^2$ | Nnz of $A^2$ | Compression ratio of $A^2$ |
|-----|---------------|------------|-------|---------|-------------|----------------|--------------|-----------------------------|
| 1   | m133-b3       | 200,200    | 800,800 | 4.0     | 4           | 3,205,200      | 3,182,751    | 1.01                        |
| 2   | mac_econ_fwd500 | 206,500    | 1,273,389 | 6.2  | 44          | 7,556,897      | 6,704,899    | 1.13                        |
| 3   | patents_main  | 240,547    | 560,943 | 2.3     | 206         | 2,604,790      | 2,281,308    | 1.14                        |
| 4   | webbase-1M    | 1,000,005  | 3,105,536 | 3.1 | 4700        | 69,524,195     | 51,111,996   | 1.36                        |
| 5   | mc2depi       | 525,825    | 2,100,225 | 4.0  | 4           | 8,391,680      | 5,245,952    | 1.60                        |
| 6   | secrscuit     | 170,998    | 958,936  | 5.6     | 353         | 8,676,313      | 5,222,525    | 1.66                        |
| 7   | mario002      | 389,874    | 2,101,242 | 5.4  | 7           | 12,829,364     | 6,449,598    | 1.99                        |
| 8   | cage12        | 130,228    | 2,032,536 | 15.6   | 33         | 34,610,826     | 15,231,874   | 2.27                        |
| 9   | majorbasis    | 160,000    | 1,750,416 | 10.9 | 11         | 19,178,064     | 8,243,392    | 2.33                        |
| 10  | offshore      | 259,789    | 4,242,673 | 16.3  | 31         | 71,342,515     | 23,356,245   | 3.05                        |
| 11  | 2cubes_sphere | 101,492    | 1,647,264 | 16.2  | 31         | 27,450,606     | 8,974,526    | 3.06                        |
| 12  | poison3Da     | 13,514     | 352,762  | 26.1    | 110        | 11,768,678     | 2,957,530    | 3.98                        |
| 13  | filter3D      | 106,437    | 2,707,179 | 25.4  | 112        | 85,957,185     | 20,161,619   | 4.26                        |
| 14  | mono_500Hz    | 169,410    | 5,036,288 | 29.7  | 719        | 204,030,968    | 41,377,964   | 4.93                        |
| 15  | conf5_4-8x8-05 | 49,152     | 1,916,928 | 39.0  | 39         | 74,760,192     | 10,911,744   | 6.85                        |
| 16  | cant          | 62,451     | 4,007,383 | 64.2  | 78         | 269,486,473    | 17,440,029   | 15.45                       |
| 17  | consph        | 83,334     | 6,010,480 | 72.1  | 81         | 463,845,030    | 26,539,736   | 17.48                       |
| 18  | shipsec1     | 140,874    | 7,813,404 | 55.5  | 102        | 450,639,288    | 24,086,412   | 18.71                       |
| 19  | rna10        | 46,835     | 2,374,001 | 50.7  | 145        | 156,480,259    | 7,900,917    | 19.81                       |
| 20  | delannay_n24 | 16,777,216 | 100,663,202 | 6.0  | 26        | 633,914,372    | 347,322,258  | 1.83                        |
| 21  | cage15       | 5,154,859  | 99,199,551 | 19.2  | 47        | 2,078,631,615  | 929,023,247  | 2.24                        |
| 22  | wb-edu       | 9,845,725  | 57,156,537 | 5.8  | 3841      | 1,559,579,990  | 630,077,764  | 2.48                        |
| 23  | cop20k_A      | 121,192    | 2,624,331 | 21.7  | 81        | 79,883,385     | 18,705,069   | 4.27                        |
| 24  | hood         | 220,542    | 10,768,436 | 48.8  | 77        | 562,028,138    | 34,242,180   | 16.41                       |
| 25  | pwk          | 217,918    | 11,634,424 | 53.4  | 180       | 626,054,402    | 32,772,236   | 19.10                       |
| 26  | pdb1HYS      | 36,417     | 4,344,765 | 119.3 | 204       | 555,322,659    | 19,594,581   | 28.34                       |

Table 3: Detailed information of the 26 matrices. The top 19 matrices are denoted as normal matrices, whereas the bottom 7 matrices are denoted as large matrices.

The SpGEMM library and the SpGEMM libraries of *spECK*, *nsparse*, and *cuSPARSE* will be provided in a github repo after the acceptance by IEEE Access.

Fig. 5 shows the overall performance of SpGEMM for the normal matrices. We can see that *OpSparse* clearly outperforms other state-of-the-art SpGEMM libraries on all the normal matrices. Specifically, *OpSparse* performs on average 7.35×, 1.43×, and 1.52× better than *cuSPARSE*, *nsparse*, and *spECK*, respectively. *cuSPARSE* achieves relatively stable performance with varying input matrices. However, *cuSPARSE*’s performance is the lowest. *nsparse* and *spECK* achieve similar performance on all the normal matrices.

Fig. 6 shows the overall performance of SpGEMM for the 7 large matrices. The performance of *cuSPARSE* is omitted since it cannot compute the large matrices. *OpSparse*’s performance is the best among other libraries on all the 7 large matrices.

### 6.3 Performance analysis of the multiple optimizations

Our proposed framework provides multiple optimizations for SpGEMM. To better show the performance contribution of the optimizations, we analyze their performance improvements individually in this section.

#### 6.3.1 Binning method

We compare the performance of the binning method with *nsparse* and *spECK*. Fig 7 shows the execution time of the two binning steps compared to the overall execution time of SpGEMM. *OpSparse* clearly outperforms *nsparse* and *spECK*. For *nsparse*, the two binning steps take up to 29.2% of the total execution time in the worst case and 10.1% of the total execution time on average for the 26 matrices. For *spECK*, the two binning steps take up to 27.1% of the total execution time in the worst case and 10.6% of the total execution time on average for the 26 matrices. In
Figure 5: Performance comparison of SpGEMM on 19 normal matrices

Figure 6: Performance comparison of SpGEMM on 7 large matrices

Opsparse, the two binning methods only take 4.7% of the total execution time in the worst case and 1.5% on average. The overhead of the two binning steps in nsparse and spECK is nontrivial since the binning steps are only a low complexity and auxiliary task for SpGEMM. By fully utilizing shared memory, our binning methods only take a little computation time in computing the overall SpGEMM.

Figure 8 shows the execution time of the two binning steps. The performance of the two binning steps in Opsparse achieves on average 12× and 10× performance speedup compared to nsparse and spECK, respectively. We attribute this impressive performance speedup to our better utilization of the shared memory.

6.3.2 Hashing method

Our hashing method is shown in Algorithm 4 and Algorithm 5. We optimise the access pattern to the hash tables compared to the traditional implementation in nsparse and spECK. We access the hash table once in each while loop, whereas nsparse and spECK access the hash table multiple times in each while loop. To compare the performance difference between the two hashing versions, we implement the two hashing versions in our framework such that all other implementations are kept the same except for the access pattern. Fig. 9 shows the performance of the two versions of hashing methods in symbolic and numeric steps. Compared to the multiple access version of the hashing method, the single access version achieves on average 1.09× and 1.10× performance speedup in the symbolic step and numeric step, respectively. In Opsparse, we adopt the single access version of hashing method.

6.3.3 Binning range selection

Each kernel’s hash table size is fixed in the symbolic and numeric steps in Opsparse. However, assigning rows with different $n_{prod}$ (or $n_{nz}$) to the kernels is a relatively free choice controlled by the binning ranges. As mentioned in section 4.3, selecting different binning ranges is a trade-off between hardware utilization efficiency and hash collision rate.

To explore which kinds of binning ranges yield the best performance for the symbolic and numeric steps, we test three kinds of binning ranges (shown in Table 4) in the symbolic step and four kinds of binning ranges (shown in Table 5) in the numeric step.
Figure 7: Execution time of the two binning steps compared to the overall execution time of SpGEMM

Figure 8: Execution time of the two binning steps

Figure 9: Performance of the symbolic and numeric steps with the two versions of the hashing method. The prefix sym and num denote the symbolic and numeric steps. The suffix single and multi denote the single access and multiple access versions of the hashing method.

Fig. 10 shows the performance of the symbolic step with the three kinds of binning ranges. The implementations with the sym_1.2× and sym_1.5× binning ranges achieve on average 1.02× and 0.99× performance speedup, respectively, compared to the sym_1× binning range. This means the average performance improvement when scaling down the binning range in the symbolic step is not significant and even negative. The reason is that, by using the n_prod in the classification, the hash collision rate is usually low since the n_prod is usually larger than the actual n_nz.

However, scaling down the binning ranges may improve the performance nontrivially for benchmarks with a small compression ratio. For the matrix webbase-1M and patents_main, the performance speedup of sym_1.2× and sym_1.5× binning range is significant compared to the sym_1× binning range. We attribute the significant performance improvement to the lowered hash collision rate since the compression ratios of the webbase-1M and patents_main benchmarks are only 1.36 and 1.15, respectively. For other tested benchmarks, the performance of the sym_1.2×
Table 4: The hash table size and three kinds of binning ranges for the symbolic step. The three binning ranges are obtained by keeping the hash table size of each kernel $1\times$, $1.5\times$, and $2\times$ larger than the largest $n_{\text{prod}}$ in the corresponding group. We denote the four binning ranges for the symbolic step as $\text{sym}_1\times$, $\text{sym}_1.2\times$, and $\text{sym}_1.5\times$, respectively.

| Kernels | Table size | Sym_1x   | Sym_1.2x  | Sym_1.5x  |
|---------|------------|----------|-----------|-----------|
| Kernel0 | 31         | 0 – 31   | 0 – 21    | 0 – 10    |
| Kernel1 | 255        | 32 – 255 | 22 – 192  | 17 – 128  | 11 – 85 |
| Kernel2 | 511        | 256 – 511| 193 – 384 | 129 – 256 | 86 – 170 |
| Kernel3 | 1023       | 512 – 1023| 385 – 768 | 257 – 512 | 171 – 341 |
| Kernel4 | 2047       | 1024 – 2047| 769 – 1536| 513 – 1024| 342 – 682 |
| Kernel5 | 4095       | 2048 – 4095| 1537 – 3072| 1025 – 2048| 683 – 1365 |
| Kernel6 | 8191       | 4196 – 8191| 3073 – 5460| 2049 – 4096| 1366 – 2730 |
| Kernel7 | 24575      | 12288 – $\infty$ | 5461 – $\infty$ | 4097 – $\infty$ | 2731 – $\infty$ |

Table 5: The hash table size and four kinds of binning ranges for the numeric computation. The four binning ranges are obtained by keeping the hash table size of each kernel $1\times$, $1.5\times$, $2\times$, and $3\times$ larger than the largest $n_{\text{nz}}$ in the corresponding group. We denote the four binning ranges for the numeric step as $\text{num}_1\times$, $\text{num}_1.5\times$, $\text{num}_2\times$, and $\text{num}_3\times$, respectively.

| Kernels | Table size | Num_1x   | Num_1.5x  | Num_2x   | Num_3x   |
|---------|------------|----------|-----------|----------|----------|
| Kernel0 | 31         | 0 – 31   | 0 – 21    | 0 – 16   | 0 – 10   |
| Kernel1 | 255        | 32 – 255 | 22 – 192  | 17 – 128 | 11 – 85 |
| Kernel2 | 511        | 256 – 511| 193 – 384 | 129 – 256| 86 – 170 |
| Kernel3 | 1023       | 512 – 1023| 385 – 768 | 257 – 512| 171 – 341|
| Kernel4 | 2047       | 1024 – 2047| 769 – 1536| 513 – 1024| 342 – 682 |
| Kernel5 | 4095       | 2048 – 4095| 1537 – 3072| 1025 – 2048| 683 – 1365 |
| Kernel6 | 8191       | 4196 – 8191| 3073 – 5460| 2049 – 4096| 1366 – 2730 |
| Kernel7 | 24575      | 12288 – $\infty$ | 5461 – $\infty$ | 4097 – $\infty$ | 2731 – $\infty$ |

is similar to the $\text{sym}_1\times$ binning range, whereas the performance of the $\text{sym}_1.5\times$ is considerably lower than the $\text{sym}_1\times$ binning range. Therefore, $\text{OpSparse}$ adopts the $\text{sym}_1.2\times$ binning range for the symbolic step.

![Normalized performance](image)

Figure 10: Normalized performance of the symbolic step with different binning ranges. The performance is normalized to the performance with $\text{sym}_1\times$ binning range, $\text{sym}_1\times$, $\text{sym}_1.2\times$, and $\text{sym}_1.5\times$ denote the performance of the symbolic step with the $\text{sym}_1\times$, $\text{sym}_1.2\times$, and $\text{sym}_1.5\times$ binning ranges (shown in Table 4), respectively.

Fig. 11 shows the performance of the numeric step with the four kinds of binning ranges. The implementations with the $\text{num}_1.5\times$, $\text{num}_2\times$, and $\text{num}_3\times$ binning ranges achieve on average $1.14\times$, $1.23\times$, and $1.20\times$ performance speedup, respectively, compared to the $\text{num}_1\times$ binning range. We can see that the performance is considerably improved when scaling down the binning ranges in the numeric step. We attribute the performance improvement to the lowered hash collision rate.

Since the implementation with the $\text{num}_2\times$ binning range achieves the average best performance than other binning ranges, our framework adopts the implementation of the $\text{num}_2\times$ binning range for the numeric step.
6.3.4 Load balance of the streaming multiprocessors

When computing the *webbase-1M* benchmark in our framework, one extremely large row is computed with the global memory hash table in the numeric phase, which takes one SM for execution. The computation time for the largest row is 7.6ms, whereas the computation time for all the other rows is only 20ms. This feature of the *webbase-1M* benchmark shows that considering the load balance of the SMs is important. Our framework ensures that when the kernel computing the largest rows is executing, other kernels are also available for execution. As a result, the total execution time of the numeric step on *webbase-1M* benchmark in our optimized framework was reduced to 21.5ms.

6.3.5 Overlapping memory allocation with kernel execution

When computing the *webbase-1M* benchmark in our framework, allocating the global hash table is required in the numeric phase, which takes 1ms. Since our framework launches one kernel in the numeric phase before the memory allocation, and the execution time of the launched kernel takes more than 1ms, the execution time of the global memory allocation in our numeric step is completely hidden for the *webbase-1M* benchmark.

7 Conclusion

Efficiently performing SpGEMM on GPUs is a challenging task. We found that both high-level algorithm design and low-level architecture-specific optimizations are critical for the overall performance of SpGEMM. In this paper, we identify seven kinds of inefficient implementations in two state-of-the-art SpGEMM libraries (i.e., *nsparse* and *spECK*). Then we propose corresponding optimizations and integrate them into a highly optimized framework *OpSparse*. The optimizations include 1) optimizing the binning method by improving the utilization of the shared memory, 2) optimizing the hashing method by reducing the access to the hash table, 3) improving the trade-off between hash collision rate and hardware utilization in the hashing method by setting appropriate binning ranges, 4) reducing the overheads of global memory utilization by minimizing the global memory usage of the metadata and using combined memory allocation instead of multiple separate memory allocations, 5) improving the execution parallelism by overlapping global memory allocation with kernel execution, 6) improving the load balance of the SMs in the GPU by manipulating the kernel launch orders, and 7) optimizing the kernel configuration for full occupancy. As a result, *OpSparse* achieves on average 7.35× (up to 27.8×), 1.43× (up to 1.81×), and 1.52× (up to 2.04×) speedups over three SpGEMM libraries *cuSPARSE*, *nsparse*, and *spECK*, respectively.

Moreover, We conduct comprehensive experiments to demonstrate the performance improvements of several individual optimizations. These experiments numerically show the performance improvements of our proposed optimizations as compared to the inefficient implementations in the state-of-the-art SpGEMM libraries.

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