Reservoir Computing on Atomic Switch Arrays with High Precision and Excellent Memory Characteristics

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Abstract

Reservoir computing (RC) refers to an artificial neural network framework that exhibits temporal dynamic behavior, and its computational structure can be implemented in physical systems. However, the network performance of conventional RC is limited in terms of power scale, readability, spatial and temporal scalabilities, mass producibility, and precision. Therefore, we propose an RC with atomic switches. An atomic switch is a new type of nanodevice that exhibits superior power scale, readability, spatial and temporal scalabilities, and mass producibility. In the proposed RC architecture, we arranged atomic switches sequentially in a ring formation and used time-division multiplexing. The resistance of the atomic switches in the proposed architecture changes nonlinearly with a change in input and memorizes the input; therefore, this RC architecture is expected to have high precision and a large memory capacity (MC). In this study, we simulated this architecture and compared it with the conventional architecture in terms of precision and MC. The results showed that the proposed RC architecture had higher precision and greater MC.

1. Introduction

Reservoir computing (RC) is a type of recurrent neural network (RNN) architecture comprising an artificial network that exhibits temporal dynamic behavior [1, 2, 3]. Unlike in conventional RNNs, the weights between nodes in RC do not change, thus simplifying training, and its computational structure can be implemented in physical systems with non-linear behavior [4]. To date, various physical RC (PRC) architectures have been proposed, including optical [5], spintronics [6], soft and elastic materials [7], molecular [8], and FPGA [9]. However, no PRC architecture satisfies all aspects of the power scale, readability, spatial and temporal scalabilities, mass producibility, and high network performance. In this study, we propose RC using atomic switches [10]. The atomic switch can be controlled by simply applying a bias to the device, and the bias is recorded in the form of the device resistance. Atomic switches work as fast as conventional electronic devices and have a simple structure [11, 12]. They exhibit superior power scale, readability, spatial and temporal scalabilities, and mass producibility. Because the resistance of an atomic switch changes non-linearly with the bias, the proposed RC architecture is expected to have a high precision [13]. Moreover, because the atomic switch can record the input for a long time, the proposed architecture is also expected to have a large memory capacity (MC) [14]. In the proposed RC architecture, we arranged atomic switches and moved the read/write header of each device to create a loop structure. This can perform calculations with delay feedback and time-multiplexed inputs. We simulated this architecture using Python and evaluated it in terms of MC and precision.

2. Construction of the Atomic Switch Reservoir

In the proposed architecture, the atomic switches were arranged as virtual nodes (VNs). The data delaying structure in existing RC systems with a single dynamical node [15] (a delay feedback reservoir) was replaced by moving data read/write headers, creating a loop structure, and short-term memory and nonlinear operations were performed in all VNs.
2.1 Atomic switch

An atomic switch has an atomic filament between its electrodes (Figure 1) [16]. Changing the bias input changes the resistance exponentially. When a positive bias is applied, atoms are deposited, and the resistance decreases. When a negative bias or zero bias is applied, the atoms are ionized and dissolved, and the resistance increases. When the device is applied with a bias greater than the threshold bias for a certain time, it maintains a lower resistance (switch) [12]. In the proposed architecture, the device did not switch, and we used it with a small bias because an over-threshold bias is extremely large and not suitable for the proposed architecture.

2.2 Delay feedback reservoir

A delayed feedback reservoir (DFR) refers to a reservoir implemented by replacing the RC network of multiple connected nodes with a dynamic system with nonlinear performance nodes that receive delayed feedback [15]. The input data are time-divided by the number of reservoir nodes and multiplied by the input mask. The value is written into the delayed loop structure through the nonlinear calculation module (Figure 2 (a)). In this DFR, the read/write interface has a nonlinear computing ability, and the loop structure only has the function of delaying data. Conversely, in the proposed architecture (Figure 2 (b)), each node has a short-term memory characteristic and nonlinear computing capability, and the read/write header forms a loop structure. This architecture is expected to have a high RC performance because all nodes have the characteristics needed for RC calculation. For the actual structure of the proposed architecture, we assume that atomic switches are arranged in an array and scanned by electrical switching with a sub-threshold current mirror circuit as a header (Figure 2 (c)).

3. Simulation and Results

We simulated the proposed architecture using Python with our atomic switch model [17].

3.1 Structure of the header

Figure 3 shows the sub-threshold current mirror circuit that was used in our simulation. We set the supply voltage as $V_{dd} = 1.8$ V and connected it to the read atomic switch. The current flowing through the write atomic switch refers to the current in the read atomic switch added to the input current source. The current value from the input current source is $J(t) \times 10^{-8}$ A, where $J(t)$ represents the input data.

3.2 Simulation parameters

The simulation parameters were the number of VN's ($N_V$), the number of nodes ($N$), and the speed of moving the header for each atomic switch ($v_s$). We prepared the step function using 3000 random input data $u(t)$ $(-0.5 \leq u(t) \leq 0.5)$ and the random matrix $M$ $(-0.1 \leq M \leq 0.1)$ for time-division multiplexing. The input data given to the current mirror circuit (Figure 3) were generated by a step function $J(t) = M \times u(t) + 0.5$ with a duration of $1/v_s$ s (Figure 4 (a)). We evaluated the MC and the normalized root mean square error (NRMSE) [4] with batch learning for the NARMA-10 [18] task using random input data from 0 to 1000 for RC initialization, from 1000 to 2000 for training,
and from 2000 to 3000 for evaluation.

To determine the values of \( N \) and \( N_V \), we ran the following simulations. When \( N = 395 \) and \( N_V \) were varied from 400 to 440 (\( v_s = 10^{-4} \) s) (Figure 4 (b)), we obtained a large MC when the numbers of VNs and nodes were co-prime. Therefore, we simulated our architecture with several configurations in which these numbers were co-prime.

### 3.3 Simulation with scan period

Figure 4 (d) shows the relationship between the MC and scan period (SP: \( N_V/v_s \)) with \( N_V = 101, 201, 301, 401, 501, \) and 601 in the proposed architecture and \( N_V = 401 \) in a conventional DFR, where \( N = V_N - 6 \). The MC does not exceed \( N \) [14], and in the proposed DFR, the maximum MC obtained is close to \( N \). When the SP is short, the MC increases because the nonlinearity of the atomic switch decreases.

Figure 4 (c) shows the linear relationship between \( V_N \) and \( v_s \) when the MC is maximized. This can be used as an index to determine \( v_s \).

Figure 4 (e) shows the relationship between the NRMSE in the NARMA-10 task and the SP under the same conditions as those for Figure 4 (d). When \( V_N \geq 201 \), the NRMSE obtained is less than 0.06. When the SP is long, the NRMSE decreases because the input integration time increases, resulting in the atomic switch being strongly nonlinear.

We compared the proposed architecture with a conventional DFR (Figure. 2 (a)) with \( V_N = 401 \) and the same data input. The calculation module in the conventional DFR used the Mackey–Glass function [15]

\[
\dot{X}(t) = -X(t) + \frac{\eta \cdot [X(t-1) + \gamma \cdot J(t)]}{1 + [X(t-1) + \gamma \cdot J(t)]^p}
\]

where \( X \) is the value of the calculation module; \( \eta (= 0.5), \gamma (= 0.05), \) and \( p (= 1.0) \) are constants.

#### Table 1: Performance comparison when the NRMSE between the proposed and conventional DFRs is the same

|                | Proposed DFR | Conventional DFR |
|----------------|--------------|------------------|
| NRMSE          | 0.12         | 0.12             |
| MC             | 75           | 27               |

Figure 4: (a) Step function given as the input data, (b) MC vs. \( N_V \) (with \( N = 395 \) and \( v_s = 10^{-4} \) s), (c) \( N_V \) vs. \( v_s \) when the MC is maximized, (d) MC vs. scan period, (e) NRMSE vs. scan period with \( N_V = 101, 201, 301, 401, 501, \) and 601 and a conventional DFR with \( N_V = 401 \).
Table 2: Performance comparison when the MC between the proposed and conventional DFRs is the same

|          | Proposed DFR | Conventional DFR |
|----------|--------------|------------------|
| NRMSE    | 0.06         | 0.12             |
| MC       | 27           | 27               |

Table 1 shows that when the NRMSE of the proposed DFR is the same as that of the conventional DFR (SP = 0.2 s), the MC of the former is larger than that of the latter. Table 2 shows that when the MC of the proposed DFR is the same as that of the conventional DFR (SP = 0.8 s), the NRMSE of the former is less than that of the latter.

4. Conclusions

We have shown that the proposed RC architecture with atomic switches can attain a large capacity and high precision. The scan speed affects the performance of the RC architecture, and its characteristics can be selected according to specific requirements. In addition, this architecture is superior in terms of the power scale, readability, spatial and temporal scalabilities, and mass producibility, which will contribute to the development of new RC devices.

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