Reduced Complexity Belief Propagation Decoders for Polar Codes

Jun Lin, Chenrong Xiong and Zhiyuan Yan
Department of Electrical and Computer Engineering, Lehigh University, PA, USA
Email: {jul311, chx310, yan}@lehigh.edu

Abstract—Polar codes are newly discovered capacity-achieving codes, which have attracted lots of research efforts. Polar codes can be efficiently decoded by the low-complexity successive cancelation (SC) algorithm and the SC list (SCL) decoding algorithm. The belief propagation (BP) decoding algorithm not only is an alternative to the SC and SCL decoders, but also provides soft outputs that are necessary for joint detection and decoding. Both the BP decoder and the soft cancelation (SCAN) decoder were proposed for polar codes to output soft information about the coded bits. In this paper, first a belief propagation decoding algorithm, called reduced complexity soft cancelation (RCSC) decoding algorithm, is proposed. Let \( N \) denote the block length. Our RCSC decoding algorithm needs to store only \( 5N - 3 \log_2 N \) and \( N(\log_2 N + 1) \) LLRs needed by the BP and SCAN decoders, respectively, when \( N \geq 64 \). Besides, compared to the SCAN decoding algorithm, our RCSC decoding algorithm eliminates unnecessary additions over the real field. Then the simplified SC (SSC) principle is applied to our RCSC decoding algorithm, and the resulting SSC-aided RCSC (S-RCSC) decoding algorithm further reduces the computational complexity. Finally, based on the S-RCSC decoding algorithm, we propose a corresponding memory efficient decoder architecture, which has better error performance than existing architectures. Besides, our decoder architecture consumes less energy compared to updating LLRs.

I. INTRODUCTION

Polar codes [1] are a significant breakthrough in coding theory, since polar codes can achieve the channel capacity of binary-input symmetric memoryless channels [1] and arbitrary discrete memoryless channels [2]. Polar codes of block length \( N \) can be efficiently decoded by a successive cancelation (SC) algorithm [1] with a complexity of \( O(N \log N) \), where \( N \) is the block length. In spite of the low-complexity nature of the SC algorithm, the error performance of the SC algorithm is worse than Turbo or LDPC codes for short or moderate polar codes.

The belief propagation (BP) decoding of polar codes over factor graph [3] was proposed in [1]. The message passing schedules and error performances under finite lengths were further discussed in [4], [5]. A low complexity soft-output version of the SC decoder called soft cancelation (SCAN) decoder was proposed in [6]. Compared to the BP decoders in [4], [5], the SCAN decoder has much lower computational complexity and requires less memory to store the soft messages. The SCAN decoding algorithm employs a serial message updating schedule, which is similar to the SC decoding of polar codes. In contrast, the BP decoding algorithms in [1], [4], [5] employ a parallel message updating schedule. It was shown in [6] that the SCAN decoding algorithm converges faster than the BP decoding algorithm due to the better dissemination of information. Compared to the SC decoding algorithm, both the BP and SCAN decoding algorithms have higher computational complexity and require more memory. However, these belief propagation decoding algorithms not only offer an alternative to the SC and SCL list (SCL) decoders, but also are necessary for the application of polar codes in receivers that employ the joint detection and decoding technique.

Even though the decoder architectures of the SC and SCL decoding algorithms have been well studied, the architectures of the soft-output decoders for polar codes have not been sufficiently investigated in literature. Under a 65nm CMOS technology, for a (1024, 512) polar code, the BP polar decoder chip in [7] achieves a coded throughput of 4.68Gbps when the signal to noise ratio (SNR) equals 4.0dB by occupying 1.48mm\(^2\) silicon area. Several early stopping criterions for the BP decoding of polar codes were proposed in [8] to improve the decoder throughput and energy efficiency. The (1024, 512) polar BP decoder in [8] achieves a net information throughput of 4.5 Gbps using 1.96 million gates under a 45nm CMOS technology. The BP decoder architectures in [7], [8] achieve multi Gbps throughput due to the parallel message updating schedule. However, these architectures in [7], [8] are not suitable for larger block lengths, since the number of basic processing elements (PE) is \( N \) and \( \frac{N}{2} \log_2 N \), respectively. For larger \( N \), the resulting BP decoders will suffer from excessive area and power. For the SCAN decoding algorithm, its efficient hardware implementations have not been discussed in open literature to the best of our knowledge.

In this paper, we focus on the soft-output decoding of polar codes. Our main contributions are:

1) A reduced complexity soft-output version of SC decoder, called reduced complexity soft cancellation (RCSC) decoder, is proposed. Compared to the BP and SCAN decoding algorithms, our RCSC decoding algorithm has lower computational complexity and stores less LLRs. Our RCSC decoding algorithm needs to store only \( 5N - 3 \) LLRs, significantly less than \( 4N - 2 + \frac{N \log_2 N}{2} \) and \( N(\log_2 N + 1) \) LLRs needed by the BP and SCAN decoder, respectively, when \( N \geq 64 \). Besides, our RCSC decoding algorithm converges almost as fast as the SCAN decoding algorithm.

2) The simplified SC [9] (SSC) principle is applied to our RCSC decoding algorithm, resulting in the SSC-aided RCSC (S-RCSC) decoding algorithm with even less computational complexity.
complexity.

(3) Based on our S-RSCSC algorithm, a corresponding scalable decoder architecture for polar codes is proposed. Compared to BP decoders in [7], [8], our decoder architecture has better error performance. Besides, our decoder architecture consumes less energy on updating LLRs.

II. PRELIMINARIES

A. Polar codes

Under the Arıkan’s construction method [1], the generation matrix of a polar code is an $N \times N$ matrix $G = B_N F^{\otimes n}$, where $N = 2^n$, $B_N$ is the bit reversal permutation matrix [1], and $F = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}$. Here $\otimes n$ denotes the $n$th Kronecker power and $F^{\otimes n} = F \otimes F^{\otimes (n-1)}$. Let $u_0^{N-1} = (u_0, u_1, \ldots, u_{N-1})$ denote the data bit sequence and $x_0^{N-1} = (x_0, x_1, \ldots, x_{N-1})$ the coded bit sequence, then $u_0^{N-1} = u_0^{N-1} G$. An $(N, K)$ polar code is defined by setting $x_0^{N-1}$ denoted as frozen bits. The information is conveyed by the rest $K$ bits, denoted as information bits.

B. BP and SCAN Decoding Algorithms for Polar Codes

The BP and SCAN decoding algorithms are performed over the factor graph of a polar code, which is derived from the encoding equations. Take $N = 8$ as an example, the corresponding factor graph is shown in Fig. 1(a). For $i = 0, 1, 2$ and $j = 0, 1, \cdots, 7$, node $(i, j)$ in Fig. 1(a) has two associated LLR messages $L_{i,j}$ and $R_{i,j}$, which are passed to the left and right directions of the factor graph. $L_{i,j}$ and $R_{i,j}$ are called left and right LLR messages, respectively. As shown in Fig. 1(a), the factor graph of a polar code of length $N = 2^n$ consists of $\frac{N}{2}$ homogenous unit factor graphs and $n + 1$ columns of nodes.

![Fig. 1. (a) Factor graph for a polar code with $N = 8$ (b) Message passing on an unit graph](image)

The message passing on a unit graph is shown in Fig. 1(b), where $L_{i,j}$, $L_{i,j}$, $R_{i,j}$, $R_{i,j}$, $R_{i,j}$ are LLR messages sending to the unit graph. $R_{i,j}$, $R_{i,j}$, $L_{i,j}$, $L_{i,j}$, $L_{i,j}$ are LLR messages sending from the unit factor graph and can be computed as follows:

$$L_{i+1,j_2} = f(R_{i+1,j_2} + L_{i,j_1}, L_{i,j_0}),$$  
$$L_{i+1,j_3} = f(R_{i+1,j_3}, L_{i,j_0} + L_{i,j_1}),$$  
$$R_{i,j_0} = f(R_{i+1,j_2}, R_{i+1,j_3} + L_{i,j_1}),$$  
$$R_{i,j_2} = R_{i+1,j_3} + f(R_{i+1,j_2}, L_{i,j_0}),$$

where $f(a, b)$ is approximated as

$$f(a, b) \approx \text{sign}(a) \times \text{sign}(b) \times \min(|a|, |b|).$$

For $i = 0, 1, \cdots, n$, let $L_i = (L_{i,0}, L_{i,1}, \cdots, L_{i,N-1})$ and $R_i = (R_{i,0}, R_{i,1}, \cdots, R_{i,N-1})$ denote all the left and right LLRs associated with the nodes in column $i$, respectively. Each iteration of the BP decoding algorithm consists of the left-direction message updating and the following right-direction message updating. During the left-direction message updating, $L_1, L_2, \cdots, L_n$ are updated in serial using Eqs. (1) and (2), where all the left LLRs associated with the same column are updated in parallel. During the right-direction message updating, $R_{n-1}, R_{n-2}, \cdots, R_0$ are updated in serial using Eqs. (3) and (4), where all the right LLRs associated with the same column are computed in parallel. Note that $L_0$ is the received channel LLR vector and $R_n$ has $N$ constant LLRs, where $R_n, j = 0$ if $u_j$ is an information bit and $R_n, j = +\infty$ otherwise. As shown in [7], a BP decoder needs to store $N (\log_2 N + 1)$ LLRs. In terms of the computational complexity, each iteration of the BP decoding algorithm is dominated by $2N \log_2 N$ additions and $2N \log_2 N$ comparisons over the real field.

Based on Eqs. (1) to (4), the SCAN decoding algorithm applies a different message updating schedule, which follows the SC decoding schedule. For each $L_i$ and $R_i$, instead of updating all the LLRs in parallel, the SCAN decoding algorithm divides $N$ LLRs into $2^i$ groups, which are updated in serial. However, the $\frac{N}{2}$ LLRs within each group are updated in parallel. Compared to the BP decoding algorithm, the SCAN decoding algorithm converges faster and needs to store fewer LLRs due to the fact that certain LLRs will never be used in the following iterations. As shown in [6], the SCAN decoding algorithm needs to store $2N - 1$ left LLRs. In [6], the right LLRs are divided into two groups: $R_{i,j}$’s with $j$ being an odd and even number, which are denoted as $R^o$ and $R^e$, respectively. The SCAN decoding algorithm in [6] needs to store $\frac{N}{2} \log_2 N$ and $2N - 1$ LLRs for $R^o$ and $R^e$, respectively. Note that, the SCAN decoding algorithm has the same computational complexity per iteration as the BP decoding algorithm.

III. THE PROPOSED RCSC DECODING ALGORITHM

A. Modified Message Passing on the Unit Graph

Both the BP and SCAN decoding algorithms are based on the message passing schedules shown in Eqs. (1) to (4). In this section, we first propose a modified message passing schedule to compute $L^o$, which are $L_{i,j}$’s with $j$ being an even integer.
For each unit graph, the left LLR
\[ L_{i+1,j_2} = \begin{cases} f(R_{i+1,j_3} + L_{i,j_3}, L_{i,j_0}) & \text{if } i = 0, \\ f(L_{i,j_1}, L_{i,j_0}) & \text{if } i > 0, \end{cases} \tag{6} \]
where \( j_2 \) is an even integer and \( j_3 = j_2 + 1 \). The modified message passing schedule for \( i = 0 \) and \( i > 0 \) is shown in Figs. 2(a) and 2(b), respectively. As shown in Figs. 2(a) and 2(b), the right LLR \( R_{i+1,j_3} \) is considered only when \( i = 0 \). For the computation of \( L_{i+1,j_3} \) and other right LLRs, Eqs. (2) to (4) are still used.

Fig. 2. (a) Message passing for the computing of \( L_{i+1,j_2} \) when \( i = 0 \) (b) Message passing for the computing of \( L_{i+1,j_2} \) when \( i > 0 \)

Compared to the message passing schedule shown in Fig. 1(b), the benefits of our modified message passing schedule are as follows.

1) When \( i > 1 \), an summation over the real field is saved when computing \( L_{i,j} \) with \( j \) being an even integer.

2) When \( j \) is an even integer, the data dependency between \( R_{i,j+1} \) and \( L_{i,j} \) is removed when \( i > 1 \). As a result, it is unnecessary to store all LLRs in \( \mathbb{R}^e \) for the following iterations.

When \( i = 0 \), the modified message passing schedule still considers the right LLR as \( R_{i+1,j_3} \) as shown in Fig. 2(a). The reason is that we want to find a way to feed \( \mathbb{R}^o \) back to the next iteration.

B. The Proposed RCSC Decoding Algorithm

Based on our modified message passing schedule, an RCSC decoding algorithm is proposed in Alg. 1 for polar codes. Like the SCAN decoding algorithm, our RCSC algorithm also employs the SC decoding schedule when updating all soft messages. As shown in Alg. 1, \( \mathbb{L} \) is a set of \( n + 1 \) LLR arrays \( \mathbb{L}_0, \mathbb{L}_1, \ldots, \mathbb{L}_n \), where \( \mathbb{L}_i \) stores \( 2^{n-i} \) LLRs for \( i = 0, 1, \ldots, n \). \( \mathbb{R}^o \) is a set of \( n \) LLR arrays \( \mathbb{R}^o_1, \mathbb{R}^o_2, \ldots, \mathbb{R}^o_n \), where \( \mathbb{R}^o_i \) stores \( 2^{n-i} \) LLRs for \( i = 1, 2, \ldots, n \). \( \mathbb{R}^e \) is a set of \( n + 1 \) LLR arrays \( \mathbb{R}^e_0, \mathbb{R}^e_1, \ldots, \mathbb{R}^e_n \), where \( \mathbb{R}^e_i \) stores \( 2^{n-i} \) LLRs for \( i = 0, 1, \ldots, n \). For our RCSC algorithm, \( \mathbb{L}_i, \mathbb{R}^o_i, \mathbb{R}^e_i \) are the memory locations used to store left LLRs, \( \mathbb{R}^o \) and \( \mathbb{R}^e \), respectively.

As shown in Alg. 1 each iteration of our RCSC decoding algorithm is divided into \( N \) serial steps. For \( i = 0, 1, \ldots, N-1 \), during step \( i \), part of left LLRs are first updated in the way shown in Alg. 2. If \( i \) is an odd integer, part of the right LLRs are also updated in the way shown in Alg. 2. \( s_j \) and \( e_j \) in Alg. 2 and 3, respectively, are variable integer indices depending on \( j \). Let \((b_{n-1}, b_{n-2}, \ldots, b_0)\) be the binary representation of the integer index \( j \), where \( b_0 \) is the least significant bit (LSB). When \( j \) is a non-zero even number, \( s_j = n - (k + 1) \) such that \( b_{k+1} = 1 \) and \( b_{r=0} = 0 \) for \( r \leq k \).

**Algorithm 1**: The Proposed RCSC Decoding algorithm

**input**: \( n \), the received channel message \( y_0^{N-1} \)

**output**: \( \hat{x}_0^{N-1} \)

1. for \( \text{iter} = 1 \) to \( M \) do
2. for \( j = 0 \) to \( N-1 \) do
3. \( \text{LComp}(j, \mathbb{L}, \mathbb{R}^o, \mathbb{R}^e) \)
4. if \( j \mod 2 = 0 \) then
5. if \( u_j \) is a frozen bit then \( \mathbb{R}^o_0[0] = \infty \) else
6. \( \mathbb{R}^o_0[0] = 0 \)
7. else
8. if \( u_j \) is a frozen bit then \( \mathbb{R}^o_0[0] = \infty \) else
9. \( \mathbb{R}^o_0[0] = 0 \)

10. RCComp(j, L, \mathbb{R}^o, \mathbb{R}^e)
11. if \( \langle L_0[j] + \mathbb{R}^o_0[j] \rangle \geq 0 \) then \( \hat{x}_j = 0 \) else \( \hat{x}_j = 1 \)
12. if \( \hat{x}_0^{N-1} \) is a valid codeword then return \( \hat{x}_0^{N-1} \)

**Algorithm 2**: LComp(j, L, \mathbb{R}^o, \mathbb{R}^e)

**input**: \( j, \mathbb{L}, \mathbb{R}^o, \mathbb{R}^e \)

1. \( i = s_j \)
2. for \( k = 0 \) to \( 2^{n-i} - 1 \) do
3. if \( j = 0 \) then
4. \[ \mathbb{L}_i[k] = f(\mathbb{L}_{i-1}[2k], \mathbb{L}_{i-1}[2k+1] + \mathbb{R}^o_i[k]) \]
5. else \[ \mathbb{L}_i[k] = \mathbb{L}_{i-1}[2k+1] + f(\mathbb{L}_{i-1}[2k], \mathbb{R}^o_i[k]) \]
6. for \( i = s_j + 1 \) to \( n \) do
7. for \( k = 0 \) to \( 2^{n-i} - 1 \) do
8. \[ \mathbb{L}_i[k] = f(\mathbb{L}_{i-1}[2k], \mathbb{L}_{i-1}[2k+1]) \]

**Algorithm 3**: RCComp(j, L, \mathbb{R}^o, \mathbb{R}^e)

**input**: \( j, \mathbb{L}, \mathbb{R}^o, \mathbb{R}^e \)

1. for \( i = n-1 \) to \( e_j + 1 \) do
2. for \( k = 0 \) to \( 2^{n-i} - 1 \) do
3. \[ \mathbb{R}^o_i[2k] = f(\mathbb{R}^o_{i+1}[k], \mathbb{R}^o_{i+1}[k] + \mathbb{L}_i[2k+1]) \]
4. \[ \mathbb{R}^o_i[2k+1] = \mathbb{R}^o_{i+1}[k] + f(\mathbb{R}^o_{i+1}[k], \mathbb{L}_i[2k]) \]
5. \( i = e_j \)
6. for \( k = 0 \) to \( 2^{n-i} - 1 \) do
7. \[ \mathbb{R}^e_i[2k] = f(\mathbb{R}^e_{i+1}[k], \mathbb{R}^e_{i+1}[k] + \mathbb{L}_i[2k+1]) \]
8. \[ \mathbb{R}^e_i[2k+1] = \mathbb{R}^e_{i+1}[k] + f(\mathbb{R}^e_{i+1}[k], \mathbb{L}_i[2k]) \]
When \( j = 0, s_j = 1 \). When \( b_0 = 1, s_j = n \), \( e_j = n - k \), where \( k \) is the smallest integer such that \( bk = 0 \). If \( bk = 1 \) for \( k = 0, 1, \ldots, n-1 \), then \( e_j = 0 \).

### Table I

Comparisons with the BP and SCAN Decoding Algorithms

|                  | BP       | SCAN     | RCSC    |
|------------------|----------|----------|---------|
| \# of stored LLRs| \( N(n+1) \) | \( 4N-2+N^2/2 \) | \( 5N-3 \) |
| \# of additions  | \( 2Nn \) | \( 2Nn \) | \( 4Nn+N^2/2 \) |
| \# of comparisons| \( 2Nn \) | \( 2Nn \) | \( 2Nn \) |

In Table I we compare our RCSC decoding algorithm with the BP and SCAN decoding algorithms in terms of memory and computational complexities. The block length \( N = 2^n \).

As shown in Table I when \( n \geq 6 (N \geq 64) \), the number of stored LLRs by our RCSC algorithm is the smallest among all three algorithms. When the block lengths are larger, our RCSC algorithm achieves more significant memory saving compared to the BP and SCAN decoding algorithms. Besides, as shown in Table I, our RCSC algorithm saves \( \frac{(n-1)N}{2} \) additions per iteration compared to the BP and SCAN algorithm.

Compared to the SCAN decoding algorithm, the major improvements of our RCSC decoding algorithm are as follows.

1) As shown in Alg. 2 when updating left LLRs, our RCSC algorithm employs the modified message passing schedule shown in Section III-A, which changes the data dependency between left LLRs and \( \mathbb{R}^v \).

2) The modified data dependency results in efficient storage of \( \mathbb{R}^v \) and reduced number of additions.

### C. SSC-aid RCSC Decoding Algorithm

In [9], [10], a polar code of length \( N \) can be represented by a binary tree of depth \( n \), where each node represents a constituent code. Fig. 3 shows the tree representation of an \((8, 3)\) polar code, where the black and white leaf nodes correspond to information and frozen bits, respectively. Among all the nodes of a tree, a node is called a rate-1 and rate-0 node if all of its leaves are associated with information and frozen bits, respectively. The SC decoding algorithm was performed on a binary tree in [9], [10], where each node behaves as a decoder for the corresponding constituent code. In this section, we formulate the proposed RCSC decoding algorithm on a binary tree.

![Fig. 3. Message passing on a binary tree](image)

As shown in Fig. 3, a node \( v \) with layer index \( i \) and a constituent code of length \( N_v = 2^{n-v} \) receives a soft message vector, \( \alpha_v \), containing \( N_v \) LLRs, from its parent node \( v_p \). Node \( v \) then calculates the soft message vector to its left child, \( \alpha_l \), containing \( N_v/2 \) LLRs, via

\[
\alpha_i[k] = \begin{cases} 
  f(\beta_r[k] + \alpha_v[2k+1], \alpha_v[2k]) & \text{if } i = 0, \\
  f(\alpha_v[2k], \alpha_v[2k+1]) & \text{if } i > 0,
\end{cases}
\]

for \( k = 0, 1, \cdots, N_v/2 - 1 \), where \( \beta_r \) (containing \( N_v/2 \) LLRs) is the soft message vector sent from the right child in the previous iteration. Node \( v \) then waits until an updated soft LLR vector, \( \beta_r \) (containing \( N_v/2 \) LLRs), is sent from its left child. In the following step, Node \( v \) calculates the soft message vector to its right child, \( \alpha_r \), where \( \alpha_r[k] = \alpha_v[2k+1] + f(\alpha_v[2k], \beta_r[k]) \) for \( k = 0, 1, \cdots, N_v/2 - 1 \). Once both \( \beta_l \) and \( \beta_r \) are updated, the soft message sent from node \( v \), \( \beta_v \), is calculated using \( \beta_v[2k] = f(\beta_l[k], \beta_r[k] + \alpha_v[2k+1]) \) and \( \beta_v[2k+1] = \beta_r[k] + f(\beta_l[k], \alpha_v[2k]) \) for \( k = 0, 1, \cdots, N_v/2 - 1 \). If node \( v \) is a leaf node, \( \beta_v = 0 \) if node \( v \) corresponds to an information bit and \( \beta_v = +\infty \) otherwise.

For our SSC-aid RCSC (S-RCSC) decoding algorithm, if node \( v \) is a rate-0 node, \( \beta_v = (+\infty, +\infty, \cdots, +\infty) \) is returned immediately without traversing its child nodes. If node \( v \) is a rate-1 node, \( \beta_v = (0, 0, \cdots, 0) \) is returned immediately. In this way, both the decoding latency and computational complexity can be reduced further. The S-RCSC algorithm has the same memory architecture as that of RCSC. \( \beta_v \) is stored in \( \mathbb{R}^v \) and \( \mathbb{R}^v \) if node \( v \) is the left and right child of its parent node \( v_p \), respectively. For each node \( v \), \( \alpha_v \) can be stored in \( \mathbb{L} \). Take the \((8, 3)\) polar code in Fig. 3 as an example, during each iteration, the RCSC decoding algorithm needs to visit all 15 nodes. In contrast, our S-RCSC decoding algorithm visits only 7 nodes (nodes 0, 1, 2, 5, 6, 11, 12) in each iteration. Hence, the S-RCSC decoding algorithm has lower computational complexity that the RCSC decoding algorithm since the number of LLRs that need to be updated is reduced due to the SSC principle.

### D. Numerical Results

For both a \((1024, 512)\) and a \((32768, 29504)\) polar codes, the frame error rate (FER) performance of our S-RCSC decoding algorithm is shown in Figs. 4 and 5, respectively, where S-RCSC\( k \) denotes our S-RCSC algorithm with the maximum number of iterations \( I_M = i \). SCAN2 denotes the SCAN decoding algorithm with the maximum number of iterations being 2. The error performances of the BP decoding algorithm under 100 maximum iterations are also shown in Figs. 4 and 5. As shown in Figs. 4 and 5, the error performance of the S-RCSC is slightly better than SCAN decoding algorithm. For both polar codes, our S-RCSC decoding algorithm has better error performance than the BP decoding algorithm when the signal to noise ratio (SNR) is higher. Note that the error performances of the RCSC and S-RCSC decoding algorithm are the same. As a result, we did not show the error performances of the RCSC decoding algorithm in Figs. 4 and 5. Let \( I_{av} \) and \( I_{bav} \) denote the average numbers of iterations for the S-RCSC and SCAN decoding algorithms, respectively, when the maximum number of iterations is set to two. As
shown in Table II, the S-RCSC algorithm and converges almost as fast as the SCAN algorithm.

**Table II**

| code          | 1.6  | 2.0  | 2.4  | 2.8  | 4.0  | 4.4  |
|---------------|------|------|------|------|------|------|
| SNR           | 1.62 | 1.25 | 1.06 | 1.007| 1.000002| 1    |
| \(I_{w,u}\)   | 1.36 | 1.12 | 1.02 | 1.003| 1.000002| 1    |

**IV. AN EFFICIENT SOFT-OUTPUT DECODER ARCHITECTURE FOR POLAR CODES**

A. Top Architecture

Based on our S-RCSC decoding algorithm, a corresponding memory efficient decoder architecture is proposed in Fig. 6(a), where LMEM, RMEMo, RMEMe, CMEM, SMEM are five LLR memories. LMEM stores the left LLRs in \(L_1, L_2, \ldots, L_n\), RMEMo stores the right LLRs in \(\mathbb{R}^c\), while RMEMe stores the right LLRs in \(R^n_1, R^n_2, \ldots, R^n_n\). The channel LLR memory, CMEM, stores \(L_0\). The soft-output memory, SMEM, stores LLRs in \(R^n_0\). Our architecture in Fig. 6(a) has one processing element array (PEA), which has \(P (P \ll N)\) identical processing elements (PEs). With the concatenation and split method in [11], LMEM, RMEMo and RMEMe can be implemented with area efficient memories such as register files or SRAMs. Note that each LLR memory in Fig. 6(a) is a dual port memory, where each word stores at most 2\(P\) LLRs. Take the LMEM as an example, the LLRs are stored in this memory in the way shown in Fig. 6(b), where \(L_i\) is stored in \(\lceil \frac{2^{n-i}}{2P} \rceil\) words and each word stores 2\(P\) LLRs. LMEM has a total of \(W = \sum_{i=1}^{n} \lceil \frac{2^{n-i}}{2P} \rceil\) words. The read and write datapaths between LLR memories and the PEA are shown in Fig. 6. The read and write address signals and enable signals of each memory are not shown for simplicity. Besides, each memory needs a bypass buffer [12] to avoid read-write conflict. Suppose each internal LLR (except the channel LLRs) is quantized with \(Q\) bits, the width of each read or write data bus of LMEM, RMEMo, RMEMe and SMEM is \(2PQ\).

Suppose each channel LLR is quantized with \(Q_c\) bits, then \(T_c = 2PQ_c\), where \(T_c\) is width of the data busses of the CMEM. For \(k = 0, 1, \ldots, P - 1\), the micro architecture of PE\(j\) is shown in Fig. 7 where the SUM unit outputs the sum of its two input LLRs and the compare-and-select (CAS) unit implements the \(f\) function in Eq. (5). The write buffer (\(wB\)) in Fig. 7 is a \(Q\)-bit register. During each iteration of our S-RCSC decoding algorithm, the left and right LLRs are updated in an interleaved way.

When updating the left LLRs, the computation type control signal, CTC, is set to 0 and the updated left LLRs are written into LMEM. For example, when \(L_i\) needs to be updated, the PEA may need to fetch \(L_{i-1}, R^n_i\) and \(R^n_i\) as shown in Alg. 2. When \(R^n_i\) is employed in the updating of \(L_i\), the left LLR selection signal, LLS, is set to 1. Otherwise, LLS = 0. When \(R^n_i\) is needed in order to compute the updated \(L_i\), the control
signal, zset, is set to 1. When no right LLRs are needed for the update of $L_i$, zset = 0. Since the PEA generates at most $P$ updated left LLRs and each word in LMEM stores $2P$ LLRs, $P$ wbs are used to buffer the first $P$ left LLRs, which are written back to LMEM once the next $P$ left LLRs are computed. If $L_i$ has less than $2P$ LLRs, the left LLL output control signal, LOC, is set to 1.

When updating the right LLRs, CTC = 1, zset = 1 and the updated right LLRs could be written into RMEMo, RMEMe and SMEM. In this case, each PE computes two updated right LLRs in one clock cycle. For our PE architecture in Fig. [7] at most $P$ right LLRs are needed during each clock cycle. However, $2P$ LLRs are read out in parallel for each right LLL memory. In Fig. [7], the segment selection signal, SS, is used to select out $P$ right LLRs from $2P$ inputs.

B. Implementation Results and Comparisons

The proposed soft-output decoder architecture has been implemented for the (1024, 512) and (32768, 29504) polar codes simulated in this paper. Each channel LLL is quantization with 5 bits, and each of the rest LLL is quantized with 7 bits. The fixed point FER performance of these two decoders are shown in Fig. [8]. For our implemented decoders, a maximum of two iterations are allowed. As shown in Fig. [8], our quantization scheme causes negligible error performance degradation. $I_{av}$'s for the two implemented decoders under various SNR are shown in Table III.

For both of our decoders, $I_{av}$ = 1 when FER is below $10^{-5}$.

![Fig. 8. Fixed point error performances](image)

Table III

| code          | (1024, 512) | (32768, 29504) |
|---------------|-------------|----------------|
| SNR           | 1.5, 2, 2.5, 3, 3.5, 4, 4.5 | 1.5, 2, 2.5, 3, 3.5, 4, 4.5 |
| $I_{av}$      | 1.68, 1.25, 1.07, 1.007, 1.000003 | 1.93, 1.47, 1.007, 1.00013, 1.00001 |

Both decoders are synthesized with the Cadence RTL compiler under the TSMC 90nm CMOS technology. The implementation results are shown in Table IV where $N_c$ and CT denote the number of clock cycles per iteration and coded throughput, respectively. Hence, $CT = \frac{N_f}{N_c}$, where $f$ is the achieved frequency. For our decoders with $N = 2^{10}$ and $2^{15}$, $P = 64$ and 128, respectively. Area efficiency (AE) in Table IV denotes the coded throughput normalized by the corresponding area. The implementation results in [7] are from the chip fabrication, while the other results are from synthesis. For fair comparisons, our implementation results under 90nm CMOS technology have been scaled to those under 65nm and 45nm.

As shown in Table IV for the (1024, 512) polar code, the area of our decoder is about 34% and 17% of that of the decoder in [7] and [8], respectively. The coded throughput of our decoder is about 28% and 21% of that of the decoder in [7] and [8], respectively. The area efficiency of our decoder is about 82% and 122% of that of the decoder in [7] and [8], respectively. For the (32768, 29504) polar code, our decoder achieves a coded throughput of 2208Mbp/s with an area of 4.734mm$^2$ under the TSMC 90nm CMOS technology. Implementation results for such a long code were not shown in [7], [8]. Compared to the decoder architectures in [7], [8], our decoder architecture has advantages in the following aspects.

(a) Compared to the BP decoders [7], [8], our decoder has much better error performances when the FER is below $10^{-7}$ as shown in Figs. [4] and [5] as well as [7] Fig. 6.

(b) Our decoder architecture is expected to consume less energy on computing updated LLRs compared to the BP decoder. In this paper, we demonstrate this advantage of our decoder architecture based on an analytical approach. When the supply voltage is $V$, let $e_a$ and $e_b$ denote the energy used for an addition and a comparison, respectively. Let $E_r$ and $E_b$ denote the average energy used for the decoding of a codeword for the S-RSC and BP decoders, respectively, where $E_r = I_{av}(N_a e_a + N_r e_b)$ and $E_b = 2Nn(e_a + e_b)I_{av}^{BP}$. Here, $I_{av}^{BP}$ is the average number of iterations for a BP decoder. $N_a$ and $N_r$ denote the number of iterations, respectively. The corresponding SNR is 3.5dB. *Scaled results under the 65nm technology. †Scaled results under the 45nm technology. ‡Estimated area under the CMOS technology scaling. *The corresponding SNR is 3.5dB. $I_{av}$ will be even smaller for larger SNR. †The corresponding SNR is 4.0dB. ²The corresponding SNR is 3.5dB.
and $N_c$ are the numbers of additions and comparisons per iteration for our S-RCSC decoder, respectively. In this paper, we consider only the energy used for computations over the real field. When the FER is low, $I_{av} \ll I_{av}^{BP}$ and $I_{av} \approx 1$.

Besides, due to our modified message passing schedule and the application of the SSC principle, $N_a < 2Nn$ and $N_c < 2Nn$.

For example, for our (1024, 512) polar code, $N_a = 11261$ and $N_c = 14332$ while $2Nn = 20480$. When SNR is 4.0 dB, $I_{av} = 1.000003$ while $I_{av}^{BP} = 6.57$ for the decoder in [7] as shown in Table [IV]. As a result, $\frac{E_b}{E_r} \approx 8.8$ compared to the BP decoder in [7].

V. CONCLUSION

In this paper, we present a more efficient belief propagation decoding algorithm and its hardware architecture. Our decoder architecture shows advantages in terms of error performance and energy efficiency.

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