A Fitting Model for Asymmetric I-V Characteristics of Graphene Field-Effect Transistors for Extraction of Intrinsic Mobilities

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Abstract—A fitting model is developed for accounting the asymmetric ambipolarities in the I-V characteristics of graphene field-effect transistors (G-FETs) with doped channels, originating from the thermionic emission and interband tunneling at the junctions between the gated and access regions. Using the model, the gate-voltage-dependent intrinsic mobility as well as other intrinsic and extrinsic device parameters can be extracted. We apply it to a top-gated G-FET with a graphene channel grown on a SiC substrate and with SiN gate dielectric that we reported previously, and we demonstrate that it can excellently fit its asymmetric I-V characteristic.

Index Terms—graphene field-effect transistor, fitting of I-V characteristic, interband tunneling, thermionic emission, intrinsic mobility.

I. INTRODUCTION

GRAPHENE field-effect transistors (G-FETs) have been vastly investigated for ultrahigh speed electronics [1] since the discovery of graphene [2,3]. The demonstration of intrinsic carrier mobility higher than 200,000 cm²/Vs of peeling graphene at room temperature [4], which was extracted by excluding all the scattering mechanisms other than acoustic-phonon scattering, stimulated the development of fabrication technologies of G-FETs that maintain the ultimately high mobilities and realize large-scale integration of them at the same time. So far, an intrinsic cutoff frequency above 300 GHz has been demonstrated [5] by G-FETs based on either epitaxial graphene grown on silicon carbide (SiC) or on graphene grown by chemical vapor deposition (CVD).

Up to now, techniques such as utilization of C-face of 4H- or 6H-SiC [6] and epitaxial CVD growth on hetero-epitaxial metal substrates [7] have been developed to realize high-quality, large-area graphene, while techniques such as hydrogen intercalation between graphene and SiC substrates [8,9], encapsulation of graphene by hexagonal boron nitride layers for CVD or peeling graphene [10], and low-damage deposition of silicon nitride (SiN) as gate dielectrics [11] have been introduced to suppress interfacial effects of substrates and gate dielectrics. Deposition of metal contacts to reduce contact resistances as well as control of doping to graphene are of equal importance on the device performances.

For evaluation of growth and gate-stack technologies of G-FETs on their performances, the most important figure of merit is the intrinsic mobility, i.e., the mobility in the gated region of a G-FET. It is directly influenced by carrier scattering mechanisms originated from scatterers in graphene, substrates, and gate dielectrics. There exist several models [12-15] which can be used for fitting the I-V characteristics of G-FETs and extracting the intrinsic mobilities. However, they assume gate-voltage-independent mobilities and, more importantly, do not take into account the asymmetric ambipolarities in the I-V characteristics of G-FETs with doped channels, which arises due to the thermionic emission and interband tunneling between the gated and access regions [16, 17]. To fully evaluate and understand the device performance from the I-V characteristics, the gate-voltage-dependent intrinsic mobilities and the asymmetry must be taken into account. Especially, the latter is important to extract the hole mobility correctly; otherwise, it causes an unphysically large discrepancy in the electron and hole mobilities (see, for example, [11]).

The purpose of this paper is to develop a fitting model to correctly extract the gate-voltage-dependent intrinsic mobilities in G-FETs and other intrinsic and extrinsic device parameters, taking into account the asymmetric ambipolarities in the I-V characteristics of doped channels, and to demonstrate its applicability to real devices. The model includes the following factors: (i) energy-dependent momentum relaxation time, which results in the gate-voltage-dependent Drude conductivity and, hence, the gate-voltage-dependent mobility, and (ii) the thermionic emission and interband tunneling at n/i/i-n or n-p/p-n junctions formed at the edges of the gated region, which results in the asymmetric ambipolarities in the I-V characteristics. We verify the model by applying it to a top-gated G-FET with a graphene channel grown on a SiC substrate and with SiN gate dielectric. We demonstrate that our model can fit the measured asymmetric I-V characteristic excellently and can extract the gate-voltage-dependent intrinsic mobility and other intrinsic and extrinsic device parameters. At the same time, it is turned out that there is a fundamental...
difficulty of unique extraction of the intrinsic mobility of a G-FET from a single I-V characteristic only, because of the inseparability of the extrinsic resistance (the sum of access and contact resistances) to the gate-voltage-independent part of the resistance of the gated region. Instead, we introduce a method to find the upper and lower bounds of the mobility. Also, it is revealed that the Dirac voltage does not correspond to the dip of the I-V characteristic because of the thermionic emission and interband tunneling at the junctions.

II. FITTING MODEL

In the model developed below, we restrict ourselves in the case (i) where the graphene channel with zero gate voltage is uniformly doped (either n or p), (ii) where the G-FET operates in the linear regime, i.e., where the drain voltage is sufficiently small so that the drain current is proportional to the drain voltage, (iii) where the gated region of the channel is sufficiently long so that the potential distribution around the gated region is applicable, and (iv) where the access regions are sufficiently long so that the potential distribution around n-i/i-n or p-p/p-n junctions does not change by the presence of contacts. In addition, we neglect the variation of the concentration in the gated region by the voltage drop across it when applying the drain voltage, which was indicated in [18]. This together with the assumption (iii) make the calculation of the conductance in the gated region somewhat inaccurate in the proximity of the Dirac voltage, where the concentration variation is large and even charge polarity might change. Away from the Dirac voltage, however, this effect should be negligibly small as long as the source-drain voltage is small, which is guaranteed by the assumption (ii), and it should not affect the fitting of an entire I-V characteristic. Here, we consider the n-doped channel; the model can be easily extended to the case of the p-doped channel by exploiting the symmetry of the electron and hole transports. We also focus on a top-gated G-FET, as the extension to a top- and/or back-gated G-FET is straightforward, except that we need to take care of variation of the contact resistance by the back gate [19, 20].

A schematic view of a top-gated G-FET under consideration is depicted in Fig. 1(a). The following geometrical parameters are assumed to be known from the device design: the gate length \( L_g \), thickness \( t_g \) and relative permittivity \( \varepsilon_r \) of the gate dielectric, the channel width \( W_{ch} \), relative permittivity of the substrate \( \varepsilon_{\text{sub}} \), and length of the access regions \( L_a \). The doping concentration, which is represented through the Fermi level, \( \varepsilon_{\text{dope}} \), is to be determined by the fitting. Figures 1(b)-(e) show band diagrams in the channel at zero drain voltage with different gate voltages. Depending on the value of the gate voltage, the carrier type of the gated region becomes either n (Figs. 1(b) and (c)), or (Fig. 1(d)), and p (Fig. 1(e)).

In this model, we take into account the electron thermionic emission and interband tunneling either at n-i/i-n or p-p/p-n junctions formed at the edges of the gated region (see Fig. 1(f)). As shown in Fig. 1(g), the channel resistance can be represented as the sum of the resistance of the gated region, \( R_g \), the resistance due to the thermionic emission and interband tunneling at the junctions, \( R_i \), and the sum of the contact resistances and access resistances, \( R_c = 2(R_{e} + R_{c}) \), which do not depend on the gate voltage:

\[
R = R_g(V_g) + R_i(V_g) + R_c = \frac{1}{G_g} + \left( \frac{1}{G_{\text{thermal}}} + \frac{1}{G_{\text{tunnel}}} \right) + R_c, \tag{1}
\]

where \( G_g \) is the conductance of the gated region, and \( G_{\text{thermal}} \) and \( G_{\text{tunnel}} \) are the conductances associated with the thermionic emission and interband tunneling at the two junctions, respectively. Expressions of \( G_g \), \( G_{\text{thermal}} \), and \( G_{\text{tunnel}} \) shall be derived and discussed in details in the following subsections.

A. Conductance of Gated Region

The conductance of the gated region can be expressed as

\[
G_g = \frac{W_{ch}}{L_g} \left( \sigma_e + \sigma_h \right), \tag{2}
\]

where \( W_{ch} \) is the width of the channel, \( L_g \) is the gate length, and \( \sigma_e \) and \( \sigma_h \) are the Drude conductivities of electrons and holes, respectively, which can be derived from the Boltzmann equation:

\[
\sigma_i = \frac{e^2}{\pi \hbar^2} \int_0^\infty \text{d}E \tau(E) \left( \frac{df_i}{dE} \right) \tag{3}
\]

In (3), \( e \) is the elementary charge, \( \hbar \) is the reduced Planck constant, \( f_i = f(E, E_i, T) = \{1 + \exp[(E-E_i)/k_B T]\}^{-1} \).
+1, and $s_h = -1$) is the Fermi distribution function, which contains the Fermi level of the gated region, $\varepsilon_g$, and the carrier temperature, $T$, $k_B$ is the Boltzmann constant, and $\tau_i = \tau(\varepsilon)$ is the momentum relaxation time. Here, it is important to account for the energy-dependent relaxation time in order to accomplish a good fitting. This is because the Fermi level in graphene widely varies by the gate voltage, unlike usual semiconductors where the averaged relaxation time is reasonable.

The Fermi level of the gated region $\varepsilon_g$ is determined by the gate voltage, $V_g$, as well as the Fermi level by the doping (i.e., $\varepsilon_g$ at zero gate voltage), $\varepsilon_{dope}$. First, the Fermi level by doping $\varepsilon_{dope}$ can be obtained from the relation of the electron concentration and the gate voltage at the Dirac voltage (see Fig. 1 (d)), $V_{dirc, g}$,

$$c_g \left( V_{dirc, g} + \varepsilon_{dope} / e \right) + e \left( -n_{dope} + p_{dope} \right) = 0.$$  \hspace{1cm} (4)

Here, $c_g = e^2/\varepsilon_0 t_g$, where $\varepsilon_0$ is the vacuum permittivity, is the static capacitance per unit area between the gate and the channel, and $n_{dope} = n(\varepsilon_{dope}, T)$ and $p_{dope} = p(\varepsilon_{dope}, T)$ are the electron and hole concentrations by doping, which are given by

$$\left[ n(\varepsilon_e, T) \right] / \left[ p(\varepsilon_e, T) \right] = \frac{2}{\pi \hbar^2 v_F^2} e^{\varepsilon_e / k_B T} \int_{-\infty}^{\infty} \frac{f(\varepsilon_1, \varepsilon_e, T)}{f(\varepsilon_2, \varepsilon_e, T)} d\varepsilon_1$$  \hspace{1cm} (5)

where $v_F$ is the Fermi velocity of graphene. Then, the Fermi level of the gated region $\varepsilon_g$ can be calculated for an arbitrary gate voltage from the relation [21]:

$$c_g \left[ V_g + (\varepsilon_{dope} - \varepsilon_g) / e \right] + e \left( -n_{dope} + p_{dope} \right) = e \left( n(\varepsilon_{dope} - \varepsilon_g, T) - p(\varepsilon_{dope} - \varepsilon_g, T) \right).$$  \hspace{1cm} (6)

Equations (4)-(6) account for the quantum capacitance of graphene, so that the Fermi level $\varepsilon_g$ around the Dirac voltage is calculated more accurately than accounting only for the static capacitance. The only unknown quantity here is the Dirac voltage, and it should be calculated as a fitting parameter.

In general, the energy-dependent momentum relaxation time $\tau_i$ should include contributions from possible scatterers: acoustic/optical phonons in graphene, disorders (short-range point defects and long-range inhomogeneities), charged impurities, grain boundaries, surface optical phonons and surface roughnesses in the substrate and the gate dielectric. To demonstrate the importance of including the energy-dependent momentum relaxation time for extraction of the intrinsic mobility, however, we focus only on two contributions in this paper and represent the momentum relaxation time as follows:

$$\frac{1}{\tau_i(\varepsilon)} = \frac{1}{\tau_{inh}(\varepsilon)} + \frac{1}{\tau_{inh}(\varepsilon)}.$$  \hspace{1cm} (7)

The first term in (7) is the contribution from scatterers whose scattering rates are linear in energy (e.g., acoustic phonons at not too low temperatures [22] and point defects [23]):

$$\frac{1}{\tau_{inh}(\varepsilon)} = \frac{1}{\tau_{inh}(\varepsilon)} + \frac{1}{\tau_{inh}(\varepsilon)}.$$  \hspace{1cm} (8)

where $\tau_{inh}$ is a dimensionless fitting parameter; its minimum value at room temperature is bounded by the acoustic phonon scattering and is $6.58 \times 10^{-4}$. The second term is the contribution from long-range inhomogeneities [23] with nonlinear scattering rate. To be specific, it includes ripples, surface roughnesses in the substrate and the gate dielectric, and, in some sense, grain boundaries if they are sufficiently dense. It is expressed as

$$\frac{1}{\tau_{inh}(\varepsilon)} = \frac{1}{\tau_{inh}(\varepsilon)} + \frac{1}{\tau_{inh}(\varepsilon)}.$$  \hspace{1cm} (9)

where $\tau_{inh}$ and $U_{inh}$ are the correlation length and the characteristic potential of inhomogeneities, $\rho(z) = \exp(-z^2/2)I_1(z^2/2)/z^2$, and $I_1$ is the first-order modified Bessel function of the first kind.

The inclusion of the second term, which is nonlinear in energy, is crucial to describe the gate-voltage dependence of the conductance and, hence, of the resistance because the conductivity becomes independent of the gate voltage if the nonlinear term is absent. This behavior was already pointed out in [4, 21]. Conversely, the second term is sufficient to qualitatively describe the usual gate-voltage dependence of the conductivity, i.e., the ambipolar curve with minimum conductivity. This is clearly illustrated in Figure 2, which show gate-voltage dependences of total conductivities, $\sigma_{+\sigma}$, in Fig. 2, we used the following parameters: $\tau_{inh}$ and $U_{inh}$ for the inhomogeneity scattering, $\alpha_{inh} = 6.58 \times 10^{-4}$ for the acoustic-phonon scattering, the Dirac voltage $V_{dirc, g}$, the thickness of the gate dielectric $t_g = 45$ nm, and the relative permittivity of the gate dielectric $\varepsilon_i = \varepsilon_2$ (a measured value of SiN for our device, see Sec. III for the detail). As expected, the conductivity is constant in the case where $U_{inh}$ is equal to zero. Also, it is seen from Fig. 2 that the sharpness of the minimum changes with $l_{inh}$. 

![Graph showing gate-voltage dependence of total conductivity](image-url)

Fig. 2. Gate-voltage dependence of total conductivity, $\sigma_{+\sigma}$, with different values of $U_{inh}$ and $U_{inh}$ for the inhomogeneity scattering, $\alpha_{inh} = 6.58 \times 10^{-4}$ for the acoustic-phonon scattering, the Dirac voltage $V_{dirc, g} = 0$, the thickness and relative permittivity of the gate dielectric $t_g = 45$ nm and $\varepsilon_i = 42$, respectively.

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B. Thermionic-Emission and Interband Tunneling Conductance

The conductances associated with the thermionic emission, \( G_{\text{thermal}} \), and with the interband tunneling, \( G_{\text{tunnel}} \), at the \( n-i/n \) or \( n-p/p-n \) junctions can be approximated analytically as follows [16,17]:

\[
G_{\text{thermal}} = \alpha_{\text{thermal}} \frac{2e^2W_{\text{th}}}{\pi^2 h} v_F T \log \left( 1 + e^{\gamma/k_BT} \right),
\]

(9)

\[
G_{\text{tunnel}} = \begin{cases} 
\alpha_{\text{tunnel}} \frac{2e^2W_{\text{th}}}{\pi^2 h} \sqrt{\frac{eE_{\text{tunnel}}}{h v_F}} & (\epsilon_g < 0), \\
0 & (\epsilon_g \geq 0).
\end{cases}
\]

(10)

Here, \( E_{\text{tunnel}} = E_{\text{tunnel}}(V_g, V_{\text{dirac}}) \) is the in-plane electric field at the "tunneling point" between the gated and access regions, where the Fermi level is equal to zero, and \( \alpha_{\text{thermal}} \) and \( \alpha_{\text{tunnel}} \) are dimensionless fitting parameters. If the analytical expressions work perfectly, then \( \alpha_{\text{thermal}} = \alpha_{\text{tunnel}} = 1 \). Equation (10) is slightly different from that derived in [17]; it reflects the fact that the doping concentrations in both source and drain sides of the access regions in top-gated G-FETs do not depend on the drain voltage. The fitting parameters \( \alpha_{\text{thermal}} \) and \( \alpha_{\text{tunnel}} \) are introduced to compensate to some extent for cases where the analytical expressions above do not provide good approximations. Those especially include the case of a low doping concentration and/or the case close to the Dirac voltage, where the thermal spread of the distribution functions should be taken into account for the interband-tunneling conductance, and the case where voltage drops at the junctions and the gated region change the barrier height from \( \epsilon_g \) in the thermionic-emission conductance (9).

Rather than searching for an analytical approximation of \( E_{\text{tunnel}} \) for top-gated G-FETs similar to that derived in [16] for top- and back-gated G-FETs, we numerically solve the two-dimensional self-consistent Poisson equation to calculate \( E_{\text{tunnel}} \). This allows us to obtain \( E_{\text{tunnel}} \) in wide ranges of \( V_g \) and \( V_{\text{dirac}} \), as well as with different values of \( \epsilon_b \) and \( \epsilon_i \). Figure 3(a) shows \( E_{\text{tunnel}} \) vs the gate voltage with different Dirac voltages (other parameters same as in Fig. 2). As the gate voltage sweeps negatively, it increases rapidly below the Dirac voltage. After that, \( E_{\text{tunnel}} \) gradually decreases. This is associated with the gate fringe effect that gradually extends the \( p \)-region under the gate with a gradual decrease in the slope of the \( n-p \) junction, i.e., the electric field. The decrease is less pronounced for higher Dirac voltage because the higher electron concentration in the \( n \)-regions screens the fringe electric field of the gate more effectively and prevents the extension of the \( p \)-region.

Figure 3(b) shows the gate-voltage dependence of the resistance \( R_n \), which is a parallel connection of \( 1/G_{\text{thermal}} \) and \( 1/G_{\text{tunnel}} \). As can be understood from Fig. 3(b) as well as (9) and (10) and Figs. 1(b)-(e), it exhibits an abrupt increase as the gate voltage sweeps negatively across the Dirac voltage. For \( V_g > V_{\text{dirac}} \), \( G_{\text{thermal}} \) is large and the resistance is fairly small (corresponding to Figs. 1(b) and (c)). After \( V_g \) passes through \( V_{\text{dirac}} \), \( G_{\text{thermal}} \) exhibits exponentially decrease, so that the total resistance rises abruptly. Meanwhile, for \( V_g < V_{\text{dirac}} \), \( G_{\text{tunnel}} \) starts to increase (Figs. 1(d) and (e)). In a range of \( V_g \) where \(-\epsilon_b T \leq \epsilon_g < 0\), \( G_{\text{thermal}} \) is comparable to \( G_{\text{tunnel}} \), so that the non-monotonic decrease in the total resistance can be seen for lower values of \( V_{\text{dirac}} \) in Fig. 3(b).

C. Extraction of Intrinsic Mobility in Gated Region

Fitting of measured I-V characteristics given as resistances, \( R_n \), at gate voltages \( V_g \) \((n = 1, 2, \ldots, N)\) is done by finding the least squares of the function

\[
f = \sum_{n=1}^{N} \left[ 1 - \frac{R(V_g)}{R_n} \right]^2,
\]

(11)

where \( R(V_g) \) is calculated as (1), with fitting parameters \( V_{\text{dirac}}, \alpha_{\text{th}}, U_{\text{th}}, \alpha_{\text{thermal}}, \alpha_{\text{tunnel}}, \) and \( R_n \). In the fitting demonstrated in the next section, the simulated annealing method was adapted to find the optimal set of the fitting parameters. To reduce the computational cost of the optimization search, we prepared a table of \( E_{\text{tunnel}} \) at wide ranges of the gate voltage and Dirac voltage and interpolated it during the search.

Then, the intrinsic mobilities of electrons and holes, \( \mu_{\text{int}}^{(e)} \) and \( \mu_{\text{int}}^{(h)} \), respectively, in the gated region can be extracted by

\[
\mu_{\text{int}}^{(e)} = \sigma_e / eN, \quad \mu_{\text{int}}^{(h)} = \sigma_h / eN.
\]

(12)

Since we assume the symmetry of the electron and hole transports in our model, gate-voltage dependences of the electron and hole mobilities are symmetric with respect to the Dirac voltage. Therefore, we use a term “intrinsic mobility” to refer both of them.

As discussed in subsection III.A, if the nonlinear term in (9) is absent, the total conductivity in (2) is independent of the gate voltage. Similarly, even when the nonlinear term is not too large compared with the linear term, contributions from those terms to the total conductivity and, hence, the resistance can be approximately separable. In other words, the resistance of the
gated region is approximately represented as \( R_g(V_g) = R_{lin} + R_{inh}(V_g) \), where \( R_{lin} \) is the contribution from the linear term and is constant, \( R_{inh} \) is that from the nonlinear term. In such a situation, the resistance \( R_{lin} \) and the sum of contact resistances and access resistances, \( R_s \), cannot be well separated from each other. In turn, the intrinsic mobility cannot be uniquely extracted from an I-V characteristic only, and another complementary measurement is necessary to do so; for example, a direct measurement of \( R_s \), or temperature-dependent I-V characteristics. This is not specific to the model developed in this paper but is a fundamental issue for any extraction methods of gate-voltage-dependent intrinsic mobilities of G-FETs, especially those with high-quality graphene channels in which the acoustic-phonon scattering becomes one of major scattering mechanisms.

However, it is possible to extract the range of intrinsic mobility from a single I-V characteristic. First, the lowest value of \( \alpha_{lin} \) is equal to \( 6.58 \times 10^{-3} \) for room-temperature acoustic-phonon scattering. Second, the lowest value of \( R_s \) can be roughly estimated from a contact resistivity already reported in literatures (for instance, see [19, 20, 24]) corresponding to the contact materials and the processing techniques that a G-FET under consideration is fabricated with. Those determine the lower and upper bounds of the mobility, respectively. In this case, we first find all the fitting parameters from the fitting, and then we replace either \( \alpha_{lin} \) or \( R_s \) with its lowest value and find another to give a minimum value of (11).

### III. FITTING OF I-V CHARACTERISTIC OF G-FET WITH SiC SUBSTRATE AND SiN GATE DIELECTRIC

Here, we apply the fitting model developed above to a G-FET fabricated and measured in our previous work [11]. It has a graphene channel grown on a C-face 4H-SiC substrate and a SiN gate dielectric deposited by the plasma-enhanced CVD. The geometrical parameters of the G-FET are as follows: the gate length \( L_g = 4.4 \) µm, thickness \( t_g = 45 \) nm and relative permittivity \( \varepsilon_r = 4.2 \) of the gate dielectric, the channel width \( W_{ch} = 11 \) µm, relative permittivity of the substrate \( \varepsilon_b = 9.7 \), and the length of access regions \( L_a = 100 \) nm. The measured relative permittivity of SiN is lower than the known value of SiN in literatures (around 7.5) because deposition conditions were identical with those for growth of large-area, thick SiN passivation layers and not optimized for deposition of thin gate dielectrics. Also, the short access regions were prepared to reduce the access resistance. As the lowest value of the extrinsic resistance, we set it to \( R_s = 40 \) Ω estimated by \( R_s = \frac{2\rho_c}{W_{ch}} \) with the contact resistivity taken from [24].

The assumption (i) of the model mentioned in Sec. II was confirmed by observing a large negative shift of the peak of the I-V characteristic, meaning the channel is highly \( n \)-doped, while (ii) was checked by applying the source-drain voltage up to \( V_{ds} = 100 \) mV. The assumption (iii) is evidently valid, although the short access regions slightly violate (iv). A possible effect of this violation on fitting results shall be discussed later.

Figure 4(a) shows the total resistance of the G-FET in [11] measured at the drain voltage \( V_{ds} = 50 \) mV and at room temperature, \( T = 300 \) K (circles), a fitting curve for it calculated with the lowest value of \( R_s = 40 \) Ω (solid line), and the decomposition into the gate-voltage dependent portions, \( R_g \) and \( R_{tt} \) (inset). (b) The same as (a) but for the fitting with the lowest value of \( \alpha_{lin} = 6.58 \times 10^{-3} \).

Figure 5. Carrier-energy dependences of scattering rates \( 1/\tau_{lin} \) with \( \alpha_{lin} = 9.42 \times 10^{-3} \) and \( \alpha_{lin} = 6.58 \times 10^{-3} \) (solid and dashed lines, respectively) and \( 1/\tau_{inh} \) with \( U_{imh} = 24.9 \) meV and \( l_{imh} = 4.59 \) nm (dashed-dotted line).
\( \alpha_{\text{lin}} = 6.58 \times 10^{-3} \) is shown in Fig. 4(b). The extracted extrinsic resistance was \( R_s = 56.2 \, \Omega \). As seen in Figs. 4(a) and (b), the fitting curves do not have visible differences. It illustrates the difficulty of unique extraction of \( \alpha_{\text{lin}} \) and \( R_s \) from a single I-V characteristic and the necessity of finding their ranges (and the intrinsic mobility).

From the extracted Dirac voltage, the doping concentration is obtained as \( 3.91 \times 10^{12} \, \text{cm}^{-2} \). It can be seen in Fig. 4(a) that the Dirac voltage does not correspond to the peak of the total resistance, at \( V_g = -8.75 \, \text{V} \). This shift takes place because the resistance of the gated region, \( R_{gn} \), has a peak at the Dirac voltage but the resistance due to the thermionic emission and interband tunneling, \( R_{th} \), has an abrupt increase there (see the inset in Fig. 4(a)). In general, with an n-doped channel, the latter resistance shifts the peak of the total resistance to the “left”, and the “left” part of the total resistance shifts up; vice versa with a p-doped channel.

Figure 5 shows scattering rates \( 1/\tau_{\alpha_{\text{lin}}} \) and \( 1/\tau_{\alpha_{\text{inh}}} \) with extracted parameters as functions of carrier energy. Compared to the acoustic-phonon-limited scattering rate, \( 1/\tau_{\alpha_{\text{lin}}} \) with \( \alpha_{\text{lin}} = 6.58 \times 10^{-3} \), the scattering rates \( 1/\tau_{\alpha_{\text{inh}}} \) with \( \alpha_{\text{inh}} = 9.42 \times 10^{-3} \) and \( 1/\tau_{\alpha_{\text{inh}}} \) are of the same order (the latter is even lower than that). This indicates that in the G-FET under consideration the external scattering sources other than acoustic phonons are remarkably suppressed and the scattering rate is comparable to that by acoustic-phonon scattering.

Values of the extracted fitting parameters for the thermionic emission and interband tunneling, \( \alpha_{\text{therm}} = 5.33 \) and \( \alpha_{\text{tunnel}} = 3.11 \), which are higher than expected, mean that the analytical expressions (9) and (10) and/or the numerical calculation of \( E_{\text{tunnel}} \) underestimate those in the real G-FET. For the interband tunneling, neglect of thermal spread of distribution functions when the gated region become i-region (i.e., \( V_g \sim V_{\text{Dirac}} \)), invalidation of an assumption of smooth n-p junctions required for the analytical expression of the tunneling probability [25] to derive (10), and/or inaccuracy of \( E_{\text{tunnel}} \) due to the neglect of contacts in the numerical calculation can be possible reasons. The last one can be caused by the short access regions in our G-FET. For the thermionic emission, the change in the barrier height by voltage drops at the junctions and the gated region and/or the local heating of electrons at the junctions can cause the increase in the conductance. Although identification of reasons for these discrepancies, as well as correction to the model while keeping computational costs of finding optimal fitting parameters reasonably low, necessitate further investigation, it is out of scope of the paper.

Figures 6(a) and (b) show the gate-voltage-dependent intrinsic mobility (\( V_g > V_{\text{Dirac}} \) for electrons and \( V_g < V_{\text{Dirac}} \) for holes) and the intrinsic conductance with the voltage drop of 50 mV in the gated region. For the mobility, total concentration (n-p) corresponding to each gate voltage is also shown. Here, we define the intrinsic transconductance as

\[
\sigma_{\text{int}} = \frac{\partial G}{\partial V_g}|_{V_{ds},}
\]

which is the transconductance in the gated region as if all the source-drain voltage is applied to there. As seen in Fig. 6(a), the intrinsic mobility exhibits the maximum of 194,000-239,000 cm²/Vs at the Dirac voltage and of 50,600-63,300 cm²/Vs at the maximum of the intrinsic conductance. This together with the low extrinsic resistance, 40-56.2 Ω, indicate an excellent performance of the G-FET in [11]. The extracted value of the constant mobility in [11], 101,000 cm²/Vs, is only at the middle between the maximum mobility and the mobility at the maximum intrinsic transconductance, and is insufficient to represent either of the latter values. The gate-voltage-dependent mobility provides more useful information about G-FETs, depending on operating points of the gate voltage in question; e.g., as amplifiers the mobility at maximum transconductance is important. For other applications such as terahertz lasers [26] or plasmonic terahertz devices [27], the concentration-dependent momentum relaxation time is more important to determine the device performances. In either case, the fitting model developed here is a powerful tool to correctly extract intrinsic and extrinsic device parameters of G-FETs, especially the gate-voltage-dependent intrinsic mobility, for evaluation of growth and gate-stack technologies of G-FETs on their performances.
IV. Conclusion

A fitting model for asymmetric I-V characteristics of G-FETs was developed in order to correctly extract the gate-voltage-dependent intrinsic mobility in the gated region and other intrinsic and extrinsic device parameters. It took into account (i) the energy-dependent momentum relaxation time to describe the gate-voltage-dependent Drude conductivity and, hence, the gate-voltage-dependent mobility; and (ii) the thermionic emission and interband tunneling at n-i-i-n or n-p-p-n junctions formed at the edges of the gated region to describe the asymmetric ambipolarities in I-V characteristics. The following assumptions for device operation and geometry were made: (i) the graphene channel is uniformly doped, (ii) the gated region is sufficiently long, and (iv) the access regions are sufficiently long. Based on these assumptions, the total resistance calculated from the I-V characteristic of the G-FET can be represented as the sum of the resistance of the gated regions, $R_g$, the resistance due to the thermionic emission and interband tunneling at the junctions, $R_{th}$, and the sum of contact and access resistances, $R_c$. To describe the gate-voltage-dependent $R_g$, it is crucial to include both scattering rates linear and nonlinear in carrier energy, as the absence of the latter causes $R_g$ independent of the gate voltage. Conversely, it was turned out that the former causes a fundamental difficulty in separating the gate-voltage-independent part of $R_g$ from $R_c$. Thus, the intrinsic mobility cannot be uniquely extracted from an I-V characteristic only, and another complementary measurement is necessary. Instead, upper bounds of the mobility was found by assuming only the acoustic phonon scattering for the gate-voltage-independent part of $R_g$, while lower bounds was found by estimating $R_c$ from a lowest value of the contact resistivity already reported in literatures. The model was applied to a top-gated G-FET with a graphene channel grown on a SiC substrate and with SiN gate dielectric we reported previously. We demonstrated that the model can excellently fit the I-V characteristic and can extract its high intrinsic mobility as well as its low extrinsic resistance. It was shown that the Dirac voltage does not correspond to the peak of the total resistance because of an abrupt increase in $R_c$ near the Dirac voltage. These results verified that the model is a powerful tool to correctly extract intrinsic and extrinsic device parameters of G-FETs, especially the gate-voltage-dependent intrinsic mobility, for evaluation of growth and gate-stack technologies of G-FETs on their performances.

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