A Compact Model for SiC Power MOSFETs for Large Current and High Voltage Operation Conditions

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Abstract—This work presents a physics based compact model for SiC power MOSFETs that accurately describes the I-V characteristics up to large voltages and currents. Charge-based formulations accounting for the different physics of SiC power MOSFETs are presented. The formulations account for the effect of the large SiC/SiO2 interface traps density characteristic of SiC MOSFETs and its dependence with temperature. The modeling of interface charge density is found to be necessary to describe the electrostatics of SiC power MOSFETs when operating at simultaneous high current and high voltage regions. The proposed compact model accurately fits the measurement data extracted of a 160 milli ohms, 1200V SiC power MOSFET in the complete IV plane from drain-voltage $V_d = 5$mV up to 800 V and current ranges from few mA to 30 A.

I. INTRODUCTION

Silicon Carbide (SiC) is gradually penetrating the power electronics market [1], [2]. The fast switching speeds, low on-resistance and superior temperature handling of SiC power MOSFETs presents this technology as a good candidate to replace Silicon in the medium voltage range of hundreds to thousands of volts. The switching speeds and threshold voltage instability of SiC power MOSFETs bring however new challenges for circuit designers and hinders the process of unlocking the full potential of this promising technology [4], [5]. To exploit full potential of SiC technology accurate circuit simulations are a necessity. Simulations save iterative design costs and speed up the overall design process. To achieve accurate circuit simulations, it is essential to provide circuit designers with accurate and convergence-robust transistor models. The development of transistor models that can reproduce the static and dynamic behavior of SiC power MOSFETs play a crucial role in the path to achieve reliable and accurate circuit simulations.

SiC modeling research has progressed from previous empirical models [6], [7] to physics-based surface-potential-based models [8], [9]. Silicon Carbide power MOSFETs suffer from a reduced charge carrier mobility in the inversion charge functioning as channel due to a high density of charge traps in the SiC/SiO2 interface. The temperature dependence of the traps density in the SiC/SiO2 interface incurs a reduction of the threshold voltage of the device at high temperatures. Such phenomena combined with the self-heating of the transistor affect the $dV/dt$ and the $di/dt$ of the power switch, key parameters that define the switching losses of power transistors. Some efforts have been put in improving the accuracy of SiC transistor models by accounting for these effects. However, so far no models have been reported on the modeling of SiC power MOSFETs in the high voltage high current operation region. In this work, we propose a physics-based model for SiC MOSFETs which is valid in all regions of device operations. We have developed new formulations based on the silicon MOSFET compact models [10], [11] which account for the SiC MOSFET specific physics. With the developed model we report for the first time, how the behavior of interface traps w.r.t local temperature is critical to model the high current high voltage regions of I-V plane.

II. CHARACTERIZATION OF SiC MOSFET

We have selected a 160 milli Ohms/1200V commercially available SiC power MOSFET as device under test (DUT) to develop and the transistor model. Our goal is to develop a model valid for the full I-V plane. One of the challenges is that data-sheet typically do not include characterization plots covering both low and high current regions. Typically a very limited I-V graphs are given. For example to fit the trans-conductance of the power MOSFET in the extreme high voltage region, no information is given in the datasheet. Measurement equipment manufacturers also currently do not have commercial instruments capable of measuring the high current region. Therefore, in-house electrical characterization of the device to model is performed to characterize the SiC MOSFET specific physics. With the developed model we report for the first time, how the behavior of interface traps w.r.t local temperature is critical to model the high current high voltage regions of I-V plane.
High current IV characteristics are helpful to extract information of the DUT in the linear and saturation region such as drain and source terminals resistances, on-resistance of the channel of the MOSFET and its transconductance. Those are extracted through pulsed measurements to reduce self-heating and maintain the DUT inside its safe operating area (SOA) during the characterization process. Power MOSFETs however operate at bias conditions far beyond the power limits a curve tracer can measure. While hard-switching an inductive load, for example, a power MOSFET withstands high voltage and high current instantaneously. However, the static IV characteristics of a power MOSFET under such biasing conditions are often unknown and transistor models either extrapolate or flattened them. This leads to inaccurate modeling of the transconductance of the power switch at large drain-source voltages and hence non-precise dynamic behavior reproduction. A double pulse test (DPT) permits the study of a power switch at switching conditions close to the application [12]. The power MOSFET in a DPT experiences for short time simultaneous high current and high voltage operation conditions. From the current and voltage transient waveforms read in an oscilloscope, the intrinsic instantaneous voltages of the power switch can be inferred to extend the characterization of the high current IV plane of a power MOSFET up to very large voltages. For that, different techniques have been proposed. To minimize the effect of self-heating in the measurements and to achieve high accuracy in the high voltage and high current IV characteristics of the DUT, we use the technique and considerations explained in. From the I-V characteristics of the power MOSFET at high current and high voltages, we can extract useful information for modeling the transconductance at large drain-source voltages and short channel effects typical in SiC power MOSFETs.

III. MODEL DEVELOPMENT

We have developed a physics-based compact model for SiC power MOSFETs. This model accounts for the interface charge in SiC FETs, and the effect of drift region in these devices. This modifies the device electrostatics and is accounted in our model in the following manner. The starting point for charge-based compact model is the calculation of the pinch-off potential. We modify the basic formulation of the pinch-off potential to account for the interface traps charge present in the SiC MOSFETs as well as its temperature dependence. The pinch-off potential formulation for SiC power MOSFETs is,

$$V_g - V_{FB} - \frac{\alpha \psi_s}{1 + \alpha \cdot \psi_s} - \psi_p - \gamma \sqrt{\psi_p^2 + \psi_p} - 1$$  \hspace{1cm} (1)

where $V_g$ is the gate voltage, $V_{FB}$ is the flat-band voltage, $\psi_s$ is the surface-potential, $\alpha$ is a fitting parameter to capture the variation of filled interface charges $\psi_{s}$, $\gamma$ is the body-effect coefficient and $N_{it}$ is the density of traps in the SiC/ SiO2 interface in SiC power MOSFETs which is a function of local temperature $T$. Next, the inversion charge at the source and the drain is calculated using the following formulation.

$$\ln(q) + \ln\left(\frac{2n}{\gamma} \left(\frac{2n}{q} + 2\sqrt{\psi_p - 2q}\right)\right) + 2q = \psi_p - v_c$$ \hspace{1cm} (2)

where $n$ is slope factor, $q$ is the normalized charge at any location $x$ in the channel, and $v_c$ is the normalized channel potential at a location in the channel. $v_c$ will represent the intrinsic drain potential at the drain end in the calculations, and will be equal to source potential for calculation of the charge at the source side. Eq. [2] is used to calculate the charge at the source, and at the intrinsic drain of the device. Intrinsic drain is the defined to be the location at the start of the drift region in the device. The above analytical calculation of charge at the source and the intrinsic drain enables the development of drain-to-source current model for the transistor regions of the SiC device. Applying the drift diffusion carrier transport the current is obtained to be [10].

$$I_{ds} = 2n \frac{W}{L} C_{ox} (q_s - q_d) (q_s + q_d + 1) V_i^2$$ \hspace{1cm} (3)

where $q_s$ and $q_d$ are the charges at the source and drain end of the channel, $W$ is the channel width, $L$ is the channel length, $C_{ox}$ is the dielectric capacitance per unit area, and $V_i$ is the thermal voltage. In addition to the model formulation above, the drift region of the SiC FET should be modeled properly for accurate I-V model. The drift region resistance can be obtained as,

$$R_{drift,lin} = \frac{L_d}{\mu_d \cdot q \cdot N_d \cdot A_d}$$ \hspace{1cm} (4)

where $L_d$ is the length of the drift region, $A_d$ is the area of the drift region, $\mu_d$ is the mobility in this region, and $N_d$ is the doping per unit volume of this region. We found that the above formulation is not sufficient for large voltage and current regions. In such a case, carrier velocity can saturate in the drift region leading to a non-linear behavior of the drift.
In-fact, depending on the doping and the saturation velocity drift region of the SiC FETs can only behave linearly when the current in the device is well below the maximum current $I_{\text{max}}$ given by,

$$I_{\text{max}} = v_{\text{sat}} \cdot q \cdot N_d \cdot A_d$$  

where $v_{\text{sat}}$ is the saturation velocity of the carrier in the drift region. As the drain-current $I_d$ in the device approaches the $I_{\text{max}}$ drift region resistance can behave non-linearly and increase dramatically. This is similar effect as observes in the access regions of the GaN HEMTs [13]. To account for this effect, we modify the formulation of the drift resistance as shown below.

$$R_{\text{drift}} = \frac{R_{\text{drift,lin}}}{1 + \left( \frac{I_d}{I_{\text{max}}} \right)^\beta}$$  

where $\beta$ is a model parameter which models the transition from the linear to the non-linear region resistance. Using the developed formulations we modeled the SiC FET device we characterized. The results are discussed in the next section.

**IV. RESULTS**

The linear $I_D-V_{GS}$ characteristics of the power MOSFET at low $V_{DS}$ voltages is shown in Fig. 1 for six different $V_{DS}$ voltages. We found that with the new inversion charge model calculated from Eq. 2 an accurate model can be obtained. In Fig. 2 we show the model results for output characteristics for relatively low $V_{DS}$ voltages (up-to 10 V) for several different $V_{GS}$ voltages. The accuracy of the linear region is achieved thanks to the drain resistance modification which includes the drift region typical of vertical devices. Fig. 2 is a typical output characteristics curve given in data-sheets of power MOSFETs. A reasonable model result in Fig. 2 demonstrates accurate modeling of the on-resistance and the saturation current.

In Fig. 3 we show the transfer characteristics for different drain voltages, also showing a good agreement with the measured data. In Fig. 4 we also show the modeling of the trans-conductance of the device demonstrating a good correlation with the measurements. Fig. 3 and Fig. 4 show the model results up-to 800 V an a logarithmic and linear X-axis to clearly highlight both the low and high voltage different regions. A good agreement with the measured data is observed. An accurate accounting for the temperature dependent effects is found to be very important to achieve the shown results, especially in the high power dissipation region. At the high $V_{DS}$ and $I_D$ conditions, the power dissipated in the device is quite large resulting in significant heating even in the pulsed measurements. The significant increase in current with drain-voltage $V_{DS}$ is seen in the measurements is unlike a long-channel transistor characteristic. We found that this unusual behavior can not be explained fully by the drain side electric field influence on the channel charge. The drain-side electric field can reduce the barrier and increase the charge, however, this effect alone was not sufficient to model the data accurately. We found that for SiC power MOSFETs the threshold voltage...
is strongly influenced by the temperature due to the change in interface states with the temperature. This has been reported earlier in [14]. The threshold voltage is found to decrease with temperature and this effect is found to be stronger than the mobility change with temperature. This in-turn results in an overall increase in current with temperature for the high Id regions. Similar trends have been observed in other SiC MOSFETs too. This effect is accurately modeled in the developed model.

V. CONCLUSION

The characterization of a commercially available Silicon Carbide power MOSFET in the extended I-V plane up to high current and high voltage reveals information about the current-voltage characteristics of the power switch at operation points similar to the application. SiC power MOSFETs is their large SiC/SiO2 interface trap density that hinders the carrier mobility in the channel and whose temperature dependence leads to a reduction in the threshold voltage of SiC power MOSFETs at high temperatures. This phenomena affect the trans-conductance of the SiC-based power switch at high drain-source voltages and changes its dynamic behavior. We propose formulations which account for this and the drift resistance in these devices to accurately model the drain-current in SiC vertical power MOSFETs. The effect of temperature in the traps density of the SiC/SiO2 is included and is proven to be necessary to extend the model accuracy to the high voltage and high current I-V plane, where the power SiC MOSFET is subject to high power dissipation. Simulations of the proposed drain-current model accurately resemble the measurements of the SiC power MOSFET in the complete I-V plane from $V_{DS} \approx 5$ mV to 800 V.

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