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Receiver Analog Front-End Cascading Transimpedance Amplifier and Continuous-Time Linear Equalizer for Signals of 5 to 30 Gb/s

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Abstract: A 5–30 Gb/s receiver analog front-end (AFE) cascading transimpedance amplifier (TIA) and continuous-time linear equalizer (CTLE) were implemented using a Taiwan Semiconductor 180 nm process. The system comprises a two-stage differential input pair CTLE, TIA, and a differential termination resistor \( R_m \). A source-degenerated transconductance stage was adopted in the CTLE, and source follower and shunt feedback resistor stages were adopted in the TIA. The proposed CTLE could achieve high frequencies by altering the tail current with fixed degenerate capacitance \( C_S \) and resistance \( R_S \). The proposed AFE achieved high bandwidth, and the use of a feedback resistor \( R_f \) and inductor \( L_f \) improved its high-frequency performance. Simulation results revealed that the CTLE can compensate for 16 dB of channel loss at a 3 GHz Nyquist frequency and can open closed eyes in a 6 Gb/s non-return-to-zero signal with a bit error rate of \( 0.16 \times 10^{-12} \) for a \( 2^{31} – 1 \) pseudorandom binary sequence input. The AFE could compensate for 12 dB of channel loss at a 15 GHz Nyquist frequency and can open closed eyes in a 30 Gb/s PAM4 signal from a pseudorandom binary sequence input; it consumed 27 mW of power at 1.8 V.

Keywords: continuous-time linear equalizer; transimpedance amplifier; pulse amplitude modulation; no-return-to-zero; analog front-end; source follower

1. Introduction

As data rates have increased by 1.5 times every year since 2000, high-speed data communications are required in modern broadband applications to address bandwidth demand. Initially, in 2000, radio frequency applications required a bandwidth of 1–2 GHz for optical time-domain reflectometer applications. To meet modern broadband demand, data rates have increased to 25–30 Gbps, which is more than 75% of previous data communications. Increasing bandwidth must meet multiple challenges including channel loss, high-speed operation, area, equalization, and robustness. For data communication power, in particular, consumption is a very important factor in maintaining high performance. There are several previous studies of 28 Gbps or higher data rates [1–5]. Those use unrolled decision feedback equalizers to meet critical timing margins, but the unrolled CTLE structure increases the power and die’s area. To achieve these challenges, one of the key designs is an analog front-end (AFE) cascading transimpedance amplifier with a continuous-time linear equalizer.

Historically, TIAs have been mostly developed for the front-ends of the optical receivers (for example, the families of 2.5, 10, 40, … GB/s). However, their usage is not limited to optical applications, although they have been for a long time the major driving force beyond development towards both lower noise and higher speeds. Nevertheless, in recent decades, advanced TIA designs have become increasingly popular for a variety of applications such as physics and radiation detectors of particles, miniaturized magnetic resonance spectroscopy [2], and vision and biological sensors. Different applications have
their own requirements for the main parameters of TIA design. For example, high-speed optical communication circuits have pushed the bandwidth of TIAs in multiple GHz ranges from novel designs with lower power consumption to reduced chip area and minimized noise while operating at significant frequency [6]. Obviously, the front-end TIA is the most critical component of the channel influencing both noise sensitivity and the speed of the overall system. At the output of the linear channel, voltage is provided that can be later used by decision circuits.

The second most critical component of the analog front-end block is the decision circuit or equalization circuit as shown in Figure 1. Equalization is typically implemented in both the transmitter and the receiver [7]. Before the channel, it is desirable to “peak” the transmitted high-frequency content instead of performing all the high-frequency peaking at the receiver side. On the receiver side, high-frequency peaking degrades the receiver input signal-to-noise ratio (SNR), whereas the transmit side does not. Therefore, within the transmitter, equalization is implemented to supply pre-emphasis of the high-frequency vanguard of bit transitions. In the receiver, equalization is implemented to revive the combined transmitter and channel characteristics towards a reference channel that has no or reduced ISI. Obviously, CTLE in a receiver is intended to equalize the combined characteristics of the transmitter and channel and remove the ISI at the received signal sampling points. The RX CTLE is similar to TX FFE CTLE except the input is an analog signal. The RX CTLE is often called a discrete-time linear equalizer [3,8]. As an FIR filter, designed to subtract ISI effects from adjacent bits. The output of RX CTLE is further sampled to point per data time interval for data detection. The RX CTLE will only cancel ISI at the data detection sample points.

Channel losses or insufficient bandwidth are obstacles to achieving higher data rates in data communications. One solution is changing the signal transformation scheme from two-level pulse amplitude modulation (PAM2), also known as non-return-to-zero (NRZ), to four-level pulse amplitude modulation (PAM4), to double the data rate without increasing the bandwidth [9,10]. However, PAM4 requires greater system linearity. Increasing system bandwidth or using a continuous-time linear equalizer (CTLE) to compensate for channel losses are other potential solutions [11–13].

Receivers with equalization can overcome problems caused by channel loss, such as intersymbol interference. Effective high-performance receivers must meet numerous requirements, including those for power consumption, area, bit error rate (BER), and equalization. In receiver analog front-ends (AFEs), equalizers such as CTLE are commonly used (Figure 1). CTLE has lower power consumption than other equalizers in high-speed applications. Moreover, as the data rate increases, the proposed CTLE can achieve different
equalization for different cable lengths by tuning the tail current with a fixed capacitor and resistor. The architecture presented in [1] is generally used in high-speed AFEs.

Typically, transimpedance amplifiers (TIAs) are used to limit receiver noise. Common-gate stages are effective amplifiers for high frequencies but have poor noise characteristics [14,15]. The TIAs based on the shunt–feedback architecture have a low-noise topology that is advantageous for high-data-rate applications. However, a trade-off exists between the performance of the circuit and the suitability of the DC operating point in conventional linear transconductance (Gm)-TIA systems. To achieve a suitable DC operating point, the size of the transistors must be increased, resulting in a large parasitic capacitance at the output nodes and reducing the bandwidth of the circuit. To overcome this problem, source follower (SF) stages were used to design the proposed AFE. This paper is organized as follows: Section 2 details the design considerations, Section 3 presents the simulation results, and Section 4 concludes the research.

2. Design Consideration

2.1. CTLE

The equalization value of conventional CTLEs can be increased or decreased by varying the capacitor ($C_S$) and resistor ($R_S$), illustrated in the schematic in Figure 2. The peaking frequency is directly correlated with this equalization value and affects the bandwidth ($f_w$). Consequently, disassociating the equalization value and $f_w$ in the circuit is key. The source-degenerated Gm-cell is chosen such that the gain is degenerated through $R_S$, ensuring sufficient linearity in the system (Figure 2). A zero can also be introduced by combining $C_S$ and $R_S$ [8,16].

![Figure 2. Schematic of Conventional CTLE.](image)

Equation (1) presents the transfer function of the single-ended CTLE.

$$H(S) = \frac{G_M R_L}{1 + \frac{G_M R_S}{2}} \times \frac{1 + \frac{S}{\omega_z}}{(1 + \frac{S}{\omega_p})(1 + \frac{S}{\omega_z})}$$

(1)

where $\omega_z = \frac{1}{R_S C_S}$, $\omega_p = \frac{1 + G_M R_S}{R_L C_L}$, and $\omega_p = \frac{1}{R_L C_L}$ are the zero and two poles of the CTLE, respectively (Figure 3).
Figure 3. Single-ended Bode Plot of the CTLE.

To attain the peak gain at a higher frequency, the CTLE must be designed such that the pole frequency is higher than the zero frequency [17–19]. The peaking gain also depends on the dominant pole and zero. The frequencies depend on $G_M$ of the differential pair and of the degeneration $C_S$ and $R_S$, as presented in Equation (2).

$$\text{Maximum boost peaking} = \frac{\omega_p^1}{\omega_z} = 1 + G_M R_s. \quad (2)$$

In the low-frequency range, CTLE operates similarly to a differential amplifier with source degeneration, and their gains are therefore equal in this range:

$$\text{DC gain} = \frac{g_m R_L}{1 + \frac{G_M R_s}{2}} \quad (3)$$

In the high-frequency range, $C_S$ shorts the pins of the CTLE, and the circuit operates similarly to a differential amplifier without source degeneration. Therefore, the peak gain of the CTLE is as follows:

$$\text{peak gain} = g_m R_L \quad (4)$$

Figure 2 reveals that if $V_{bias}$ varies, the current flow through transistors $M_1$ and $M_2$ varies. However, the output current at nodes $V_{out1}$ and $V_{out2}$ changes drastically, and the dominant poles and zero also change slightly. To achieve constant current flow at nodes $V_{out1}$ and $V_{out2}$ while enabling variation in $V_{bias}$, a two-stage differential input pair CTLE with fixed degeneration $C_S$ and $R_S$ is proposed.

### 2.2. Proposed Continuous-Time Linear Equalizer

Figure 4 presents a schematic of the proposed CTLE comprising two differential pairs, $M_1$ with $M_2$ and $M_3$ with $M_4$. The differential pair comprising $M_3$ and $M_4$ is degenerated by the parallel resistor $R_S$ and the capacitor $C_S$. $M_5$, $M_6$, and $M_7$ are the current sinks and are controlled $V_{bias1}$ and $V_{bias2}$. 
where $V_{biasn}$ is the common-mode voltage, and $V_{adjust}$ is the adjusting voltage for varying the bias currents of the differential pairs of the CTLE. If $V_{biasp} > V_{biasn}$, the current $I_2 = 2I_1$ flows through $M_6$, passes to $M_7$, and the current $I_1$ flowing through $M_6$ and $M_7$ passes to $M_3$ and $M_4$, as presented in Figure 4. The output current at nodes $V_{out1}$ and $V_{out2}$ is $I_{tot} = 2I_1$. Similarly, $V_{biasp} < V_{biasn}$, the output current at nodes $V_{out1}$ and $V_{out2}$ is $I_{tot} = 2I_1$. This design also boosts the DC gain at high frequency and slightly shifts the zero ($\omega_z$) and poles ($\omega_{p1}$ and $\omega_{p2}$). The zero $\omega_z$ of the proposed CTLE is dependent on $g_{m1}$ and $g_{m3}$ and on $R_S$ and $C_S$. The transfer function of the single-ended proposed CTLE is presented in Equation (8).

$$H(S) = \frac{(G_{M1} + G_{M3})R_L}{1 + \frac{(G_{M1}G_{M3})R_S}{2}} \times \frac{1 + \frac{s}{\omega_z}}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})}$$

where $\omega_z = \frac{1}{R_L C_L}$, $\omega_{p1} = \frac{1}{\frac{R_L}{R_S} C_s}$, and $\omega_{p2} = \frac{1}{R_S C_L}$ are the zero and poles of the proposed CTLE.

The maximum boost gain at higher frequencies and the DC gain are determined using Equations (8) and (9).

$$\frac{\omega_{p1}}{\omega_z} = 1 + (G_{M1}G_{M3})R_s$$

$$\text{DC gain} = \frac{(g_{m1} \times g_{m3})R_{L1}}{1 + \frac{(G_{M1}G_{M3})R_s}{2}}$$

**Figure 4.** Schematic of Proposed CTLE.
The Bode plot of the single-ended proposed CTLE with zeroes $\omega_Z$ and $\omega_{Z1}$ that shift due to variations in the DC gain is presented in Figure 5.

![Bode Plot](image)

**Figure 5.** Single-ended Bode Plot of the Proposed CTLE.

### 2.3. TIA

A trade-off exists between the suitability of the DC operating point and performance at low frequency in this conventional $g_m$ transimpedance structure. The bandwidth $f_w$ and transimpedance $g_m$ in TIAs are decoupled. High-feedback resistance is necessary for good noise performance. Figure 6 presents a schematic of a TIA topology with a feedback resistor $R_f$. The input impedance is extended by a factor of $A+1$, where $A$ is the amplifier gain, and the transimpedance is approximately $R_f$ [1,14,15].

![TIA Schematic](image)

**Figure 6.** Simple TIA Topology with feedback resistor $R_f$.

For a fixed-bandwidth amplifier, the equivalent transfer function $T(s)$ is as shown in Equation (10):

$$
T(S) = \frac{V_{out}}{I_{in}} = -\frac{A}{1 + A} \frac{R_f}{1 + \frac{R_f C}{1 + A}} = -\frac{A}{1 + A} R_f
$$

(10)

To achieve the desired DC operating point, transistor size ($W/L$) must be increased. However, bandwidth decreases, and large parasitic capacitances occur at the output nodes [15,17]. To overcome this problem, the SF state is introduced along with a shunt feedback resistor in the TIA as preferred in [14]. To increase the frequency bandwidth, a differential out-phase circuit is included in the TIA as shown in Figure 7.
Figure 7. Schematic of Single-ended TIA.

A two-input differential TIA with resistor feedback along the inductor in series is implemented. The TIA can facilitate data transfer at all speeds tolerated by the interface. The architecture has three parts that each corresponds to a stage. The first part is a shunted feedback resistor, the second part is a simple buffer, and the third part is an entirely differential output phase. A single-ended schematic is presented in Figure 7 [14,17]. Specifically, the shunt feedback resistor in the first stage converts a current to a voltage. The second-stage $M_{B1}$ acts as a buffer and inverter with two SFs enabling isolation between the input and output of the amplifier. The third stage, $M_{O1}$, is the output phase, which increases the phase and increases the amplifier gain in which $M_{O2}$ is the tail current.

Figure 8 shows a single-ended TIA circuit with a common source stage and SF. The SF isolates $R_D$ from the loading effect of both $R_f$ and $L_f$. The output impedance of the SF is less than the resistor feedback [17,20,21].

Figure 8. Single end of the TIA.
The open-loop gain of the amplifier is as follows:

$$T(S) = -\frac{A}{1 + \frac{G_{M}R_{D}}{1 + G_{M}R_{D}Z}}$$  \quad (11)$$

where $Z$ is the impedance, which is the total resistance to current flow in a circuit containing both resistance $R_{f}$ and inductor reactance $X_{L}$. $Z$ is defined as $\sqrt{R_{f}^2 + X_{L}^2}$.

The input and output impedances of the resistor feedback at low frequencies are as follows.

$$R_{Zin} = \frac{Z}{1 + G_{M}R_{D}}$$  \quad (12)$$

$$R_{Zout} = \frac{1}{G_{MB}(1 + G_{M}R_{D})}$$  \quad (13)$$

The inductor and resistor in series, gives second order frequency 3 dB bandwidth as follows.

$$\omega_{-3db} = \frac{\sqrt{2}(1 + A)}{R_{D}}$$  \quad (14)$$

2.4. Receiver AFE Architecture

The AFE architecture presented in Figure 9 includes a differential $R_{m}$ (100 Ω) termination, a two-stage CTLE and TIA, and a feedback resistor ($R_{f}$) and inductance reactance ($L_{f}$). The 100 Ω resistor was adopted to match the differential input of the circuit with that of the equipment. The AFE topology along the $g_{m}$ TIA with the CTLE compensates for the channel loss at a 15 GHz Nyquist frequency and adjusts the output amplitude without bandwidth deterioration [1,4,7]. The transfer function of the AFE circuit is as follows:

$$A_{V,DC} = -\frac{g_{m}R_{D}}{1 + g_{m}R_{f}} \frac{1 - g_{mTIA}R_{f}}{1 + g_{mTIA}R_{D}f_{s}}$$  \quad (15)$$

$$A_{V,AC} = A_{V,DC} \frac{\left(1 + \frac{S}{\omega_{p1}}\right)\left(1 + \frac{S}{\omega_{p2}}\right)}{\left(1 + \frac{S}{\omega_{n1}}\right)\left(1 + \frac{S}{\omega_{n2}}\right)\left(\frac{S}{\omega_{n1}}\right)^2 + \frac{2\pi}{\omega_{n1}} + 1}$$  \quad (16)$$

where $\omega_{p1} = \frac{1}{R_{m}C_{L1}}$, $\omega_{p2} = \frac{1 + \frac{g_{m}R_{f}}{g_{m}C_{L1}}}{1 + \frac{g_{m}R_{f}}{g_{m}C_{L1}}}$, $\omega_{n} = \sqrt{1 + \frac{g_{mTIA}R_{D}\omega_{p1}}{(C_{L2}L_{f})}}$, $\omega_{p2} = \sqrt{1 + \frac{g_{mTIA}R_{D}}{(C_{L2}L_{f})}}$, $\omega_{n1}$, and $\omega_{n2}$ are poles. To increase the bandwidth, $R_{f}$ should be larger. However, the RC constant can be increased by simply increasing $R_{f}$, unexpectedly decreasing the bandwidth [22,23]. Thus, inductance reactance is used to increase bandwidth without changing the pole $\omega_{p2}$.

![Figure 9. Receiver AFE Architecture.](image-url)
3. Results

The proposed AFE cascading TIA and CTLE was designed and simulated in a 180 nm complementary metal–oxide–semiconductor (CMOS) process. The performance of the CTLE, TIA, and the resulting eye diagram was simulated with Virtuoso 6.1.8–64 b software.

A high-frequency through-silicon scalable electrical model using a field solver was used as a transmission line (channel) [24,25]. Figure 10 reveals that the simulated channel can achieve 10 dB decay isolation loss at a 1.5 GHz Nyquist frequency for different cable lengths (2–8 m).

Figure 10. Variations in Channel Characteristics for Lengths of 2 m–8 m at 1.5 GHz.

Figure 11 reveals that the simulated CTLE can achieve a DC gain of −2 to 9 dB at a 3 GHz Nyquist frequency by tuning bias voltage $V_{biasn}$ and $V_{biasp}$ and adjusting the voltage $V_{adjust}$ (represented by X in Figure 11) from +360 to −360 mV for a channel length of 3 m. Figure 12 presents the characteristics of CTLE with and without a 3 m channel at a 3 GHz Nyquist frequency.

Figure 11. Simulated Frequency Response for the CTLE.
Figure 11 reveals that the simulated CTLE can achieve a DC gain of $-2$ to 9 dB at a 3 GHz Nyquist frequency by tuning bias voltage $V_{biasn}$ and $V_{biasp}$ and adjusting the voltage $V_{adjust}$ (represented by X in Figure 11) from +360 to −360 mV for a channel length of 3 m.

Figure 12 presents the characteristics of CTLE with and without a 3 m channel at a 3 GHz Nyquist frequency.

Figure 13 presents the simulated single-ended 6 Gb/s NRZ eye diagrams with the two different lossy channels. Figure 13b reveals that the output eye is closed at the decay stage in which the CTLE is disabled. By contrast, Figure 13a reveals that the 6 Gb/s NRZ eyes are open if the CTLE is enabled.
In this case, the input signal was a simulated NRZ pseudorandom bit sequence $2^{31} - 1$ with a peak-to-peak amplitude of 189.914 mV; the root-mean square jitter was 8.86 picosecond. An input and output impedance of 50 Ω and a 50 pf capacitor were used in this case. Figure 14 presents all measured parameters of the simulated eye diagram.

Figure 14. Simulated Eye Diagram. (1) 0 level at 1.33 V; (2) 1 level at 1.52 V; (3) and (4) rise and fall time of 102.2 and 95.1151 ps, respectively; (5) and (6) eye height and width of 118.882 mV and 196.79 ps, respectively.

Figure 15 presents the simulated histogram plots used to calculate the eye width and height. Figure 15a presents a horizontal histogram used to measure the eye width at each time point and to sum up the number of traces across vertical bins. Figure 15b is a vertical histogram of eye height measurements for every amplitude point; these points were summed across the time axis.

Simulated BER bathtub curves for NRZ input data rates of 6 Gb/s are presented in Figure 16. The BER variations for different positions of the sampling point for both time delay and the voltage–power relationship are presented in Figure 16. In this case, BER(t) was $0.16 \times 10^{-12}$. Table 1 summarizes the key performance metrics of the proposed CTLE and other recently published CTLEs. The proposed CTLE achieved a peaking frequency with constant current for tuning its equalization competence.

Figure 17 presents the simulated frequency response of the AFE cascading the CTLE and the TIA. Subsequently, the bandwidth must recover from 6 GHz (approximately 18/3 GHz) to 15 GHz; thus, the equalizer is tuned to its maximum peaking. To reach this required bandwidth, the TIA is designed to boost the equalizer by introducing a feedback resistor $R_s$ and inductor $L_t$. The frequency response for AFE reached 15 GHz at various bias voltages ($-80, 0, \text{ and } 80 \text{ mV}$) with 12 dB channel losses at a 15 GHz Nyquist frequency with a 3 m channel (Figure 17a). Similarly, Figure 17b reveals that the DC gain varies as $V_{adjust}$ varied from $-80$ to 160 mV at a 15 GHz Nyquist frequency.
Figure 14. Simulated Eye Diagram. (1) 0 level at 1.33 V; (2) 1 level at 1.52 V; (3) and (4) rise and fall time of 102.2 and 95.1151 ps, respectively; (5) and (6) eye height and width of 118.882 mV and 196.79 ps, respectively.

Figure 15 presents the simulated histogram plots used to calculate the eye width and height. Figure 15a presents a horizontal histogram used to measure the eye width at each time point and to sum up the number of traces across vertical bins. Figure 15b is a vertical histogram of eye height measurements for every amplitude point; these points were summed across the time axis.

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Figure 17 presents the simulated frequency response of the AFE cascading the CTLE and the TIA. Subsequently, the bandwidth must recover from 6 GHz (approximately 18/3 GHz) to 15 GHz; thus, the equalizer is tuned to its maximum peaking. To reach this required bandwidth, the TIA is designed to boost the equalizer by introducing a feedback resistor $R_s$ and inductor $L_f$. The frequency response for AFE reached 15 GHz at various bias voltages ($-80, 0, \text{ and } 80 \text{ mV}$) with 12 dB channel losses at a 15 GHz Nyquist frequency (Figure 17a). Similarly, Figure 17b reveals that the DC gain varies as $V_{\text{adjust}}$ varied from $-80$ to $160 \text{ mV}$ at a 15 GHz Nyquist frequency.

Table 1. Performance comparison.

| Equalization | [9] | [10] | [12] | [13] | This Work |
|--------------|-----|-----|-----|-----|-----------|
| Data rate (Gbps) | 10 | 16 | 16 | 20 | 5–15 |
| Channel loss (dB) | Nyquist | NA | 27.6 | 20.5 | 12 | 16 |
| Eye width@BER < $10^{-12}$ | 0.62 | 0.18 | 0.16 | NA | 0.16 |
| Supply (V) | 1 | 1.2 | 1.2 | 1.5 | 1.8 |
| Power (mW) | 72 | 173.17 | 173.17 | 100 | 14 |
| Technology | 65 nm | 65 nm | 65 nm | 90 nm | 180 nm |

Figure 16. Simulated BER(t) bathtub curves for the 6 Gb/s NRZ signal.
Table 1. Performance comparison.

| Equalization                          | [9] | [10] | [12] | [13] | This Work |
|---------------------------------------|-----|------|------|------|-----------|
| Data rate (Gbps)                      | 10  | 16   | 16   | 20   | 5–15      |
| Channel loss (dB)/Nyquist             | NA  | 27.6 | 20.5 | 12   | 16        |
| Eye width@BER < $10^{-12}$            | 0.62| 0.18 | 0.16 | NA   | 0.16      |
| Supply (V)                            | 1   | 1.2  | 1.2  | 1.5  | 1.8       |
| Power (mW)                            | 72  | 173.17| 173.17| 100  | 14        |
| Technology                            | 65 nm | 65 nm | 65 nm | 90 nm | 180 nm    |

Figure 17. Simulated frequency response for the AFE. (a) 12 dB by tuning $V_{\text{bias}}$ from $-80$, 0, and 80 mV and (b) from $-80$ to 160 mV.
Figure 18 reveals that the simulated single-ended 30 Gb/s PAM4 eyes are open for 12 dB of channel loss at a 15 GHz Nyquist frequency. The PAM4 eyes parameters are indicated as (1)–(4) in the figure. The simulated 0-level (1), 1-level (2), 2-level (3), and 3-level (4) voltages were 1.325, 1.392, 1.463, and 1.544 V, respectively. The eye width of levels 0/1, 1/2, and 2/3 were all 375 ps. Figure 19a presents the width of a simulated level-4 eye using the histograms for the other levels. Similarly, Figure 19b presents the bit periods for level 0/1, 1/2, and 2/3 through threshold histograms.

Figure 18. Eye diagram AFE for PAM4 signal.

Figure 19. Cont.
Figure 19. (a) Histogram of the eye diagram reveals eye widths for levels 0, 1, 2, and 3. (b) Threshold histogram of the eye diagram reveals the bit period of levels 0/1, 1/2, and 2/3.

Table 2 presents the key performance metrics of the proposed AFE and other recently proposed AFEs.

| Reference | [1] | [4] | [15] | [23] | This Work |
|-----------|-----|-----|------|------|-----------|
| Technology CMOS | 28 nm | 28 nm | 40 nm | 40 nm | 180 nm |
| Power supply | 1.5 V | 0.9 V | 1 V | 1.2 V | 1.8 V |
| Equalization | 14-tap CTLE | CTLE+DFE | CTLE | CTLE | CTLE |
| Data rate range (Gbps) | 1.25–28.5 | 32 | 8–10 | 20 | 5–30 |
| Power (mW) | 560 | 240 | 10 | 12.8 | 27 |
| Channel loss (@GHz) | 34 dB@14 | 37 dB@16 | 17 dB@4 | 18 dB@10 | 28 dB@15 |

4. Conclusions

The simulated two-stage differential input pair CTLE can successfully compensate for 16 dB of channel loss at a 3 GHz Nyquist frequency and can open the closed-eye 6 Gb/s NRZ signal with an energy efficiency of 8 pJ/bit and a BER of $0.16 \times 10^{-12}$ from a $2^{31} - 1$ pseudorandom binary sequence input. The TIA topology can achieve higher bandwidth, ameliorating the trade-off between bandwidth and DC gain. The AFE compensated for 12 dB of channel loss at a 15 GHz Nyquist frequency and opened closed eyes for a 30 Gb/s PAM4 signal from a pseudorandom binary sequence input; it consumed 27 mW of power from a 1.8 V supply.

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References

1. Kimura, H.; Aziz, P.; Jing, P.; Sinha, A.; Narayan, R.; Gao, H.; Jing, P.; Hom, G.; Liang, A.; Zhang, E.; et al. A 28 Gb/s 560 mW Multi-Standard SerDes with Single-Stage Analog Front-End and 14-Tap Decision Feedback Equalizer in 28 nm CMOS. In Proceedings of the 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, CA, USA, 9–13 February 2014; Volume 49, pp. 3091–3103.

2. Takemoto, T.; Yamashita, H.; Yazaki, T.; Chujo, N.; Lee, Y.; Matsuoka, Y. A 4 25-to-28 Gb/s 4.9 mW/Gb/s 9.7 dBm high-sensitivity optical receiver based on 65 nm CMOS for board-to-board interconnects. In Proceedings of the 2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers, San Francisco, CA, USA, 17–21 February 2013; pp. 118–119.

3. Kim, M.; Bae, J.; Ha, U.; Yoo, H.J. A 24-mW 28-Gb/s wireline receiver with low-frequency equalizing CTLE and 2-tap speculative DFE. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), Lisbon, Portugal, 24–27 May 2015; pp. 1610–1613.

4. Parikh, S.; Kao, T.; Hidaka, Y.; Jiang, J.; Toda, A.; Mcleod, S.; Walker, W.; Koyanagi, Y.; Shibuya, T.; Yamada, J. A 32 Gb/s wireline receiver with a low-frequency equalizer, CTLE and 2-Tap DFE in 28 nm CMOS. In Proceedings of the 2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers, San Francisco, CA, USA, 17–21 February 2013; pp. 28–29.

5. Kim, J.; Buckwalter, J.F. A 40-Gb/s optical transceiver front-end in 45 nm SOI CMOS. IEEE J. Solid-State Circuits 2012, 47, 615–626. [CrossRef]

6. Säckinger, E. Broadband Circuits for Optical Fiber Communication; Wiley: New York, NY, USA, 2005.

7. Lee, J. A 20-Gb/s Adaptive Equalizer in 0.13-um CMOS Technology. IEEE J. Solid-State Circuits 2006, 41, 2058–2066. [CrossRef]

8. Zheng, K.; Frans, Y.; Chang, K.; Murmann, B. A 56 Gb/s 6 mW 300 mm2 inverter-based CTLE for short-reach PAM2 applications in 16 nm CMOS. In Proceedings of the 2018 IEEE Custom Integrated Circuits Conference (CICC), San Diego, CA, USA, 8–11 April 2018; pp. 1–4.

9. Hyun, C.; Ko, H.; Chae, J.; Park, H.; Kim, S. A 20 Gb/s Dual-Mode PAM4/NRZ Single-Ended Transmitter with RLM Compensation. In Proceedings of the 2019 IEEE International Symposium on Circuits and Systems (ISCAS), Sapporo, Japan, 26–29 May 2019; pp. 1–4.

10. Roshan-Zamir, A.; Elhadidy, O.; Yang, H.; Palermo, S. A Reconfigurable 16/32 Gb/s Dual-Mode NRZ/PAM4 SerDes in 65-nm CMOS. IEEE J. Solid-State Circuits 2017, 52, 2430–2447. [CrossRef]

11. Komatsu, Y.; Shinmyo, A.; Kato, S.; Funabashi, M.; Hatooka, K.; Fujita, M.; Tanaka, K.; Yamasaki, A.; Fukuda, K. A 0.25–27-Gb/s PAM4/NRZ Transceiver with Adaptive Power CDR and Jitter Analysis. IEEE J. Solid-State Circuits 2019, 54, 2802–2811. [CrossRef]

12. Lee, J.; Chiang, P.; Peng, P.; Chen, L.; Weng, C. Design of 56 Gb/s NRZ and PAM4 SerDes Transceivers in CMOS Technologies. IEEE J. Solid-State Circuits 2015, 50, 2061–2073. [CrossRef]

13. Lee, J.; Chen, M.; Wang, H. Design and Comparison of Three 20 Gb/s Backplane Transceivers for Duobinary, PAM4, and NRZ Data. IEEE J. Solid-State Circuits 2008, 43, 2120–2133. [CrossRef]

14. Razavi, B. The Transimpedance Amplifier [A Circuit for All Seasons]. IEEE Solid-State Circuits Mag. 2019, 11, 10–97. [CrossRef]

15. Wang, J.; Pan, Q.; Qin, Y.; Chen, X.; Hu, S.; Bai, R. A fully-integrated 25 Gb/s low-noise TIA+CDR optical receiver designed in 40nm-CMOS. In Proceedings of the 2011 Transactions on Circuits and Systems II: Express Briefs, Tainan, Taiwan, 27 June 2019; pp. 67–68.

16. Lee, J.; Lee, K.; Kim, H.; Kim, B.; Park, K.; Jeong, D. A 0.1-pJ/b/dB 1.62-to-10.8-Gb/s Video Interface Receiver with Jointly Adaptive CTLE and DFE Using Biased Data-Level Reference. IEEE J. Solid-State Circuits 2020, 55, 2186–2195. [CrossRef]

17. Lin, Y.T.; Chen, H.C.; Wang, T.; Lin, Y.S.; Lu, S.S.S. 3–10-GHz ultra-wideband low-noise amplifier utilizing miller effect and inductive shunt-shunt feedback technique. IEEE Trans. Microw. Theory Techn. 2007, 55, 1832–1843. [CrossRef]

18. Choi, J.-S.; Hwang, M.-S.; Jeong, D.-K. A 0.18-um CMOS 3.5-Gb/s continuous-time adaptive cable equalizer using enhanced low-frequency gain control method. IEEE J. Solid-State Circuits 2004, 39, 419–425. [CrossRef]

19. Li, D.; Minoa, G.; Repossi, M.; Baldi, D.; Temporiti, E.; Mazzanti, A. A low-noise design technique for high-speed CMOS optical receivers. IEEE J. Solid-State Circuits 2014, 49, 1437–1447. [CrossRef]

20. Li, C.; Palermo, S. A low-power 26-GHz transformer-based regulated cascode SiGe BiCMOS transimpedance amplifier. IEEE J. Solid-State Circuits 2013, 48, 1264–1275. [CrossRef]

21. Galal, S.; Razavi, B. 10-Gb/s limiting amplifier and laser/modulator driver in 0.18-m CMOS technology. IEEE J. Solid-State Circuits 2003, 38, 2138–2146. [CrossRef]

22. Hsiao, J.; Jhou, D.; Lee, T. A 10-Gb/s equalizer with digital adaptation. In Proceedings of the 2017 International SoC Design Conference (ISOCC), Seoul, Korea, 5–8 November 2017; pp. 38–39.

23. Chen, K.-Y.; Chen, W.-Y.; Liu, S.-I. A 0.035-pJ/bit/dB 20-Gb/s adaptive linear equalizer with an adaptation time of 2.68 µs. IEEE Trans. Circuits Syst. II Exp. Briefs 2017, 64, 645–649. [CrossRef]

24. Raj, M.; Monge, M.; Emami, A. A modeling and nonlinear equalization technique for a 20 Gb/s 0.77 pJ/b VCSEL transmitter in 32 nm SOI CMOS. IEEE J. Solid-State Circuits 2016, 51, 1734–1743. [CrossRef]

25. Kim, J.; Pak, J.S.; Cho, J.; Song, E.; Cho, J.; Kim, H.; Song, T.; Lee, J.; Lee, H.; Park, K.; et al. High-Frequency Scalable Electrical Model and Analysis of a Through Silicon Via (TSV). IEEE Trans. Compon. Packag. Manuf. Technol. 2011, 1, 181–195. [CrossRef]