Improved DSVPWM strategy for transformerless three-level grid-connected inverter

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Abstract. Aiming at the leakage current problem in the transformerless three-level grid-connected inverter, an equivalent model of the common-mode circuit is established, and the analysis shows that in addition to the common-mode voltage, the fluctuation of the neutral point voltage is also an important reason for the leakage current. Therefore, an improved DSVPWM strategy is proposed, which introduces a non-basic vector in the same sector as the synthesized reference vector. This not only makes up for the shortcomings of the traditional DSVPWM strategy that cannot balance the neutral point voltage due to the lack of redundant vectors, but also retains the advantage of halving the common-mode voltage amplitude in the traditional strategy, because this introduced vector is the basis vector for other sectors. In order to prevent the total vector action durations from overflowing and reasonably allocate the duration of each vector action, a corresponding neutral point voltage balance algorithm is designed, so that the neutral point voltage is effectively controlled, and the leakage current is greatly attenuated. Simulation results verify the effectiveness of the proposed improved modulation strategy.

1. Introduction
The elimination of the output transformer from the three-level grid-connected inverter reduces the cost, size, and weight of the conversion stage, and is widely used in photovoltaic power generation systems [1,2]. But at the same time, it causes leakage current generation, which leads to an increase in the harmonic content of the grid-connected current, reduces the system's operating efficiency, and brings hidden dangers to equipment and personnel safety [3]. Therefore, it is of great significance to study the leakage current suppression method of transformerless three-phase three-level inverters.

At present, the leakage current suppression methods are mainly divided into two types: changing circuit topology and improving modulation methods. The method of changing the circuit topology includes bypassing the parasitic capacitors by connecting the negative pole of the DC bus to the neutral point of the grid [4], using an improved LCL filter to remove the high-frequency components of the common mode voltage [5], and adding a symmetric switch on the DC side to keep the common-mode voltage constant, etc [6]. This type of method generally requires the addition of devices or exists difficulties in engineering applications that will lead to increased costs, and it is difficult to effectively control the neutral point voltage at the same time. The most commonly used modulation methods are virtual space vector pulse width modulation (VSPWM) [7] and discontinuous space vector pulse width modulation (DSVPWM) [8]. VSPWM itself has a neutral point voltage balance capability, and leakage current can be suppressed by improving the modulation process, but it will cause the complication in vector transformation, the switching frequency and calculation volume will also
increase accordingly [9]. DSVPWM has a low switching frequency and can reduce the amplitude of the common-mode voltage. However, the abandonment of redundant vectors with a large common-mode voltage will cause the neutral point voltage fluctuation [10].

This paper studies the common-mode characteristics of transformerless three-phase three-level photovoltaic inverters and analyzes the generation process of leakage current. The Discontinuous Space Vector Pulse Width Modulation (DSVPWM) strategy is used to suppress the amplitude of the common-mode voltage. Based on this, an improved modulation strategy is proposed to solve the problem that traditional DSVPWM strategy is unable to balance the neutral point voltage due to the lack of redundant vectors and further reduce the leakage current amplitude. Finally, through simulation, this paper verifies the suppression effect of the improved modulation strategy on the common mode current amplitude and midpoint potential fluctuation.

2. Equivalent common-mode model of transformerless grid-connected inverter

Figure 1 shows the circuit topology of a transformerless three-level grid-connected inverter. Among them, \(C_1\) and \(C_2\) are two capacitors on the bus-side, \(u_{dc1}\) and \(u_{dc2}\) are the voltage values of the two capacitors. \(C_{PV}\) is the distributed capacitance of the solar panel to the ground, and it depends on factors such as panel area, soil properties, air humidity, and installation method [11]. The grid is represented by ideal voltage sources \(u_{ga}\), \(u_{gb}\) and \(u_{gc}\).

The parasitic capacitor, filter elements and grid impedance between the photovoltaic cells and ground can form a loop, thus forming a leakage current \(i_{cm}\). From Kirchhoff’s voltage law

\[
\begin{align*}
\frac{du_{AO}}{dt} &= L \frac{di_a}{dt} + e_a + u_{nO} \\
\frac{du_{BO}}{dt} &= L \frac{di_b}{dt} + e_b + u_{nO} \\
\frac{du_{CO}}{dt} &= L \frac{di_c}{dt} + e_c + u_{nO}
\end{align*}
\]

(1)

The common-mode voltage \(u_{cm}\) is the average of the three-phase voltage sum of the inverter output, which can be written as

\[
u_{cm} = \frac{u_{AO} + u_{BO} + u_{CO}}{3}
\]

(2)

The leakage current \(i_{cm}\) is the average value of the three-phase current sum of the inverter output, which can be written as

\[
i_{cm} = \frac{i_a + i_b + i_c}{3}
\]

(3)

Considering the three-phase voltage balance of the power grid, equation (1) could be expressed as equation (4).
\[ u_{cm} = L \frac{di_{cm}}{dt} + u_{nO} \]  

Since the common-mode voltage and leakage current are both AC quantities, the photovoltaic cells could be regarded as a short circuit when modeling.

\[
\begin{align*}
    u_{nO} &= u_{PV} + u_{dc1} \\
    u_{nO} &= u_{PV} - u_{dc2}
\end{align*}
\]  

Introducing the offset factor \( k \) \((-1 < k < 1)\), the capacitor values on the bus-side can be expressed as

\[
\begin{align*}
    u_{dc1} &= \frac{(1+k)U_{dc}}{2} \\
    u_{dc2} &= \frac{(1-k)U_{dc}}{2}
\end{align*}
\]  

Operating with equations (6), the parasitic capacitor voltage is represented by the leakage current, equation (5) can be expressed as equation (7)

\[ u_{nO} = \frac{1}{C_{PV}} \int i_{cm} dt + \frac{k}{2} U_{dc} \]  

Using the equations (4) and (7), the equivalent common-mode model can be shown that

\[ u_{cm} = L \frac{di_{cm}}{dt} + \frac{1}{C_{PV}} \int i_{cm} dt + \frac{k}{2} U_{dc} \]  

Figure 2 is an equivalent common-mode circuit model obtained by equation (8). It can be seen that there are two excitation sources in the model: the bus-side capacitor voltage differential-mode component and the output voltage common-mode component. By reducing the two excitation sources in the model, the leakage current amplitude can be reduced. The common-mode component can be suppressed by the DSVPWM strategy. In order to reduce the differential-mode component, the original modulation method should be improved to ensure that the neutral point voltage does not shift and there is no fluctuate greatly.

### 3. Improved DSVPWM strategy

#### 3.1. Select the introduced voltage vector

By introducing a non-base voltage vector to participate in the synthesis of the reference voltage vector, the improved DSVPWM strategy can balance the neutral point voltage and suppress the leakage current. Figure 3 is a basic vector diagram of the first major sector, each sector contains four minor sectors. Taking minor sector B as an example, it is discussed in two cases:

When the voltage of the bus-side capacitor C1 is greater \((u_{dc1} > u_{dc2})\), the neutral point voltage is negative. The large vector PPN in the same major sector is selected as the introduced vector, and the duration of the negative small vector OON is reduced to improve the offset of the neutral point voltage. And the introduction of PPN also helps reduce the switching times and the switching losses of the inverter. In the modulation process, introducing small vectors in other major sectors can also achieve the balance effect. However, it will increase the total small vector's duration, which will contribute to the fluctuation of the midpoint voltage, affecting the grid connection.

The improved modulation strategy follows the following three principles to modify the duration of each voltage vector: first, the synthesized reference voltage vector does not change in amplitude or direction; second, the sum of the duration is maintained as a switching period \( T_s \); Third, the condition of the neutral point voltage shift can be improved after modulation. The increase of the duration of vector OON, PON, POO and PPN is \(-t, t, -t\) and \(t\). The vector action effect is the production of the vector and its duration. Figure 4 is each vector action effect addition diagram. The total additions that can be calculated is zero, which indicates that the vector introduction has no effect on the final synthesized reference voltage.
Figure 3. The basic vector diagram of No. Ⅰ major sector.

Figure 4. Vector action effect addition diagram.

2) When the voltage of the bus-side capacitor $C_1$ is less ($u_{dc1} < u_{dc2}$), the neutral point voltage is positive. For minor sectors C and D, there is also a problem that the total duration overflows, and the duration needs to be approximated. The processing of the large vector, the medium vector and the small vector is shown in Equation (9).

$$
\begin{align*}
T_{max}^* &= T_S \cdot \frac{T_{max} + T_{mid} + T_{min}}{T_{max} + T_{mid} + T_{min}} \\
T_{mid}^* &= T_S \cdot \frac{T_{mid} + T_{max} + T_{min}}{T_{max} + T_{mid} + T_{min}} \\
T_{min}^* &= T_S \cdot \frac{T_{min} + T_{mid} + T_{max}}{T_{max} + T_{mid} + T_{min}}
\end{align*}
$$

Because the duration of introduced vector is much shorter than the switching period, the effect of this approximation on the final synthesized reference voltage can be ignored.

3.2. Calculate the duration of the introduced vector

In order to reduce the impact on the original vector sequence to minimize the switching times, the introduced vector is placed in the middle of the sequence. Taking the minor sector B as an example, when the neutral point voltage is negative, the sequence and the duration of each vector are shown in Table 1.

| Vector sequence | Duration (S) | Nutrual point current (A) |
|-----------------|--------------|--------------------------|
| OON             | $t_1 - t$    | $-i_c$                   |
| PON             | $t_2 - t$    | $i_b$                    |
| POO             | $t_3 + t$    | $-i_a$                   |
| PPN             | $t$          | 0                         |

In Table 1, $t_1$, $t_2$, and $t_3$ are the original duration of the vector. Based on the principle of charge conservation, the amount of charge flowing out from the midpoint should be exactly equal to the amount of charge difference carried by the two capacitors on the bus-side.

$$
(t_1 - t)(-i_c) + (t_2 - t)i_b + (t_3 + t)(-i_a) = -0.5CU_{dm}
$$

$U_{dm}$ is the difference between the bus-side capacitor voltage and the capacitance $C1 = C2 = C$. After finishing, the duration of the introduced vector is shown as equation (11).

$$
t = -0.5CU_{dm} + i_c t_1 - i_b t_2 + i_a t_3 \\
2i_c
$$
The vector sequence and the calculation method of the duration $t$ in other sectors are the same as those of this sector and will not be enumerated. Compared with other balance algorithms, this paper proposes an improved algorithm by collecting the inverter output current and bringing it into the equation (11) to obtain the required time parameter $t$. It is not necessary to judge the direction of the midpoint current in the algorithm, which can simplify the control process.

4. Results and analysis

Comprehensive simulation study was performed in SIMULINK. Set grid line voltage $380V$, the bus voltage to $700V$, the peak value of the grid-connected phase current to $50A$, and the switching frequency to $6kHz$. The filter inductance $L$ is $10mH$. Set the parasitic capacitance to $100nF$.

Figure 5. The capacitor $C_1$ voltage and leakage current under the traditional DSVPWM strategy.

Figure 6. The capacitor $C_1$ voltage and leakage current under the improved DSVPWM strategy.

Figure 5 and figure 6 respectively show the voltage on capacitor $C_1$ and leakage current waveforms under traditional DSVPWM and improved DSVPWM. It can be seen from Figure 5 that the system tends to stabilize after $0.02s$, the amplitude of the DC-side capacitor voltage fluctuation is $3V$, and there is a significant third-frequency harmonic component. The maximum leakage current reaches $1.5A$, and the amplitude of the leakage current is $1A$ after the system is stable.

As can be seen from Figure 6, the system stabilizes after $0.02s$, and the amplitude of the DC-side capacitor voltage fluctuation drops to $1V$. At the same time, the maximum leakage current is $300mA$, and after the system runs stably, the leakage current fluctuation drops to $200mA$. The results show that compared with the traditional DSVPWM strategy, the improved strategy proposed in this paper is also compatible with the balance control of the midpoint potential. And due to the reduction of the neutral point voltage fluctuation, the magnitude of the leakage current has been further reduced.

5. Conclusions

Based on the transformerless three-level grid-connected inverter, an equivalent model of a common-mode circuit is established, and the leakage current excitation source is composed of a common-mode
voltage component and a neutral point voltage difference-mode component. In order to solve the problem that the traditional DSVPWM strategy cannot balance the neutral point voltage, an improved modulation strategy is proposed. The non-base vector with the same sector as the synthesized reference vector is selected to reduce the number of switching times and neutral point voltage fluctuations as much as possible. Based on the principles of not changing the reference voltage vector, not changing the total vector durations, and reducing the neutral point voltage shift, an improved balance algorithm is designed to rationally distribute the vector durations and simplify the modulation process. The results show that the proposed improved modulation strategy achieves neutral point voltage balance on the premise that the amplitude of the common-mode voltage can be reduced by half, thereby fully suppressed the leakage current and improved the overall performance of the inverter.

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