Topical Review

Atomic level deposition to extend Moore’s law and beyond

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Abstract
In the past decades, Moore’s law drives the semiconductor industry to continuously shrink the critical size of transistors down to 7 nm. As transistors further downscaling to smaller sizes, the law reaches its limitation, and the increase of transistors density on the chip decelerates. Up to now, extreme ultraviolet lithography has been used in some key steps, and it is facing alignment precision and high costs for high-volume manufacturing. Meanwhile, the introduction of new materials and 3D complex structures brings serious challenges for top-down methods. Thus, bottom-up schemes are believed to be necessary methods combined with the top-down processes. In this article, atomic level deposition methods are reviewed and categorized to extend Moore’s law and beyond. Firstly, the deposition brings lateral angstrom resolution to the vertical direction as well as top-down etching, such as double patterning, transfer of nanowires, deposition of nanotubes, and so on. Secondly, various template-assisted selective deposition methods including dielectric templates, inhibitors and correction steps have been utilized for the alignment of 3D complex structures. Higher resolution can be achieved by inherently selective deposition, and the underlying selective mechanism is discussed. Finally, the requirements for higher precision and efficiency manufacturing are also discussed, including the equipment, integration processes, scale-up issues, etc. The article reviews low dimensional manufacturing and integration of 3D complex structures for the extension of Moore’s law in semiconductor fields, and emerging fields including but not limited to energy, catalysis, sensor and biomedicals.

Keywords: Moore’s law, atomic level deposition, high resolution, selective deposition, alignment

(Some figures may appear in colour only in the online journal)
1. Introduction

The continuous development of the semiconductor industry is mainly driven by reducing the sizes of microelectronic devices [1]. Notably, the number of transistors doubled at per unit area every two years with the sizes decreasing, as described by Moore’s law in 1965 [2]. After that, the law predicted the development of semiconductor manufacturing until the beginning of this century, which was known as the traditional scaling era in figure 1(a). Then, it is no longer feasible to reduce the size of transistors in equal proportion due to the limitation of photolithography. During the next equivalent scaling era, strained Si-Ge [3, 4], high K-metal gate [5] and non-planar FinFET [6] are successfully adopted into the VLSI industry, which continue to extend Moore’s law until now. The non-planar FinFET needs higher precision nanopatterning and alignment methods. EUV lithography can be used for some steps with higher resolution, but still very expensive for mass production [7, 8]. Meanwhile, the introduction of new materials and the alignment of 3D structures are quite challenging. Novel micro-nano manufacturing techniques are much needed for nanopatterning on 3D nanostructures as well as for micro-nano devices or systems with high precision and resolution. Top-down subtractive manufacturing technologies are still the mainstream of current micro-nano manufacturing for microelectronics, optical devices and other applications. However, bottom-up additive manufacturing technologies are much required because of the considerations of device geometry, density, performance and cost [9–13].

It is a long-standing dream for human beings to make atoms as building blocks for bottom-up manufacturing [14–17]. As early as 1959, Feynman speculated, ‘there’s plenty of room at the bottom’ [18]. This talk inspired the vigorous development of bottom-up manufacturing, including injection molding, 3D printing, direct self-assembly, atomic manipulation, etc. Injection molding can be used for mass production, but the machining accuracy is usually limited to the micron scale [19]. 3D printing can balance the contradiction between personalized manufacturing and high-throughput processing, which is still difficult to be applied in the processing of nanomaterials and nanostructures [20]. Direct self-assembly has machining accuracy at the atomic or molecular level, but it is only applicable to a small number of organic materials [21]. Although atomic manipulation can reach the atomic level control, it has limited methods and complex operations [22]. So, the challenges of bottom-up approaches include efficiency and precision, and they are difficult to achieve at the same time.

Atomic and close-to-atomic scale manufacturing have become the main development trend in manufacturing [23, 24]. In the booming period, various subtractive, additive and transformative nanomanufacturing methods are developed. Among them, the deposition at atomic scale is widely researched because of the characteristics of thickness control and area-selective deposition. Atomic level deposition is a kind of versatile deposition technologies towards atomic or close-to-atomic scale manufacturing of nanomaterials, nanostructures, nanodevices and nanosystems. It is important to improve resolution and alignment precision, which can relax the complexity of fabrication processes. Up to now, many deposition methods are adopted in state-of-the-art chip manufacturing, including PVD, CVD, ALD and so on. PVD is a deposition method by vaporizing the target solid materials onto various substrates through physical methods (such as evaporation, sputtering, etc), which is suitable for metals, compounds, polymers and so on [25]. CVD is a chemical process for thin films by the reaction and/or decomposition of precursors on the substrate [26, 27]. Unlike traditional CVD, ALD achieves cyclic layer-by-layer deposition which relies on saturated surface chemisorption and self-limiting chemical reactions of alternating precursors. Therefore, ALD shows controllable film thickness and excellent shape retention [28–31]. Generally, the deposition rate decreases in the order of PVD, CVD and ALD, while the step coverage is the opposite [32]. With the miniaturization of devices, deposition technologies face the challenges of ultra-high precision and high-volume manufacturing. Advanced deposition processes at the atomic level will promote the solution to these problems.

In this article, atomic level deposition is discussed. Through embedding atomic level deposition into patterned substrates, vertical angstrom resolution can be achieved as well as lateral resolution (see figure 1(b)(I)). For example, double patterning starts with the deposition of spacer layers around vertical sidewall spacers; then anisotropic etching is carried out to remove hard sacrificial masks; finally, the sidewalls leave. It can improve vertical resolution and integrate into existing lithography-etch production lines [35]. Through bringing lateral angstrom resolution to the vertical direction, atomic level deposition can also be used for patterning of low dimensional structures, such as nanowires, nanotubes, nanopores and so on. On the other hand, the downscaling of transistors drives the selective deposition of semiconductors and metals [36–38]. In figure 1(b)(II), template-assisted selective deposition methods are developed to solve the challenge of alignments, including inorganic templates, patterned polymers, SAMs and so on. There are two main challenges for selective deposition: ‘mushroom’ growth and defects in the non-growth regions [10]. To achieve high selectivity and alignment precision, integrating corrected deposition with other technologies needs a lot of exploration. To achieve sub-angstrom resolution, non-template deposition with high selectivity is discussed (see figure 1(b)(III)). Those methods are suitable for hyper-scaling structures, including nanowires, nanoparticles, single site, etc. Finally, the review gives summaries and perspectives. Atomic
level deposition is important for manufacturing of nanostructures, nanodevices, etc, it will extend Moore’s law and beyond.

2. Lateral resolution to the vertical direction

The atomic level deposition methods are characterized by the conformality and uniformity of thin films. They can bring lateral resolution to the vertical direction for diversified structures with high aspect-ratios, including sidewalls, nanowires, nanotubes and so on. Especially, the methods reduce the vertical resolution to the sub-nanometer scale. The improved resolution at vertical direction is helpful for the fabrication of nanodevices with higher precision. On the other hand, the control of vertical thickness can also be used to improve the performance of materials for applications in electronics, magnetism, acoustics, photonics, etc. Atomic level deposition can improve the accuracy of nanopatterning and obtain some special structures, which can further reduce the feature size and increase the density of transistors, thereby promoting the continuation of Moore’s law in the short term.

2.1. Sidewall resolution

The sidewall resolution is usually obtained by depositing thin films on the sidewalls of the pre-patterned substrate with a high
aspect ratio. After deposition, nanoscale sidewall films can be used to improve the resolution of processing as well as the performance of devices.

An example of sidewall resolution is double patterning. It is an important manufacturing process for VLSI production to deal with resolution limitations and overlay requirements. Current double patterning strategies mainly include LELE and SADP [39]. In LELE, the process is characterized by two sequential exposure steps, and then the feature size reduces to half of the single photolithography. As to SADP, it holds the intrinsic self-aligned characteristics and robust tolerance against overlay. In particular, the process firstly deposited thin films around vertical sidewall spacers by plasma-enhanced CVD or ALD; then etching was taken to remove hard sacrificial mask; finally, the sidewalls left with reduced half-pitch [40]. The details are presented in figure 2. In this process, obtaining a conformal and uniform thin film on prepatterned mask is the key step that determines the resolution. To get the final pattern, its difficulty lies in removing hard sacrificial masks without any residue and maintaining the integrity of the free-standing sidewalls. Double patterning came into use at the beginning of the century, which can further improve the resolution of photolithography.

As the minimum size of transistors further decreased with the increasing density, multi-patterning methods were developed based on repeating of double patterning processes. These techniques work as an effective way to reach a higher resolution. Up till now, many multi-patterning methods, including SATP, SAQP and SAOP, are developed as effective scenarios for chip manufacturing [41]. Yaegashi et al [42] realized 22 nm, 11 nm and 5.5 nm half-pitch based on above multi-patterning methods, respectively. Theoretically, the resolution can be further improved by repeating the deposition-etching steps. However, due to the difficulty of process coupling and mechanical instability of free-standing sidewalls, the current ultimate resolution is ~5 nm. Generally, these patterning methods utilize accurate control in the vertical direction to obtain increased patterning density, and will continue to play important roles in the future.

The atomic-scale sidewall resolution can be applied in other areas through atomic level deposition. For example, sidewall barriers have been used for the isolation of contact or interconnect metals and dielectrics in FETs [43–46]. Chen et al [44] deposited 7 nm Ta and 3 nm TaN barriers between Cu and low-K dielectric by PVD. It was found that Ta barrier layers showed higher step coverage and better uniformity than that of TaN layers, and the former had lower line-to-line leakage current and improved electrical field. As discussed above, only an ultra-thin layer is required to significantly improve the device performance.

Other studies were investigated for optics and magnetism applications. Shkondin et al [47] utilized sidewall deposition to fabricate nano-gratings with a high aspect ratio larger than 20:1. Silicon trenches were fabricated by deep reactive ion etching; then e-beam deposition was applied to achieve 6 nm gold layers; finally, Al2O3 and TiO2 were grown uniformly by ALD. The above applications took advantage of the conformability and uniformity of atomic level deposition on the sidewalls of 3D structures. Ozatay et al [48] deposited 1.5 nm AlOx as sidewall barriers to protect thin-film nanomagnets. Firstly, Al coatings were uniformly performed at high Ar partial pressure by ion-beam deposition, and then the layers were oxidized under oxygen atmosphere to achieve ultra-thin antiferromagnetic oxide layers. The in-situ oxidation induced high thermal stability and low magnetic damping.

As for vertical resolution down to 1 nm, nanogap structures based on sidewall deposition was potential to improve the resolution further [49–52]. Chen et al [49] created vertically oriented nanogaps in thin metal films by ALD, and the structures were packaged on a 4 inch wafer. The resolution of gap widths reached as small as 9.9 Å, which can be used for electromagnetic nanodevices with high throughput. The above methods show the advantages of reducing steps such as photolithography and etching, and results in improved performance with sidewall thickness less than 10 nm. These deposition methods have accurate thickness control in the vertical direction to realize a series of applications, including electronics, magnetics, optics, etc.
Ni nanowires were electrochemically deposited in controlled nanowire, as shown in figureography method with controllable face-to-face gaps on a single lithography. Qin deserves further exploration. preparation of nanowires through laminated structures, which aminated films \[\text{laminated structures, such as block copolymers \[\text{other methods of electronic products, and showed applications for fabrication methods as follows. Nanowires have attracted people’s attention for their applications in microelectronics [53–56], energy devices [57, 58], sensors [59, 60] and so on. Fabrication of nanowires with the vertical resolution is usually achieved by templates. As shown in figure 3(a), Heath et al developed parallel nanowire arrays with the spacings as small as 13 nm and the widths of 7 nm. This process was called superlattice nanowire pattern transfer [61, 62]. Generally, a custom-grown laminated superlattice template (GaAs/AlGaAs) with controlled spacings was achieved via molecular beam epitaxy. AlGaAs layers were selectively etched to form comb-like structures. After etching, the desired metal nanowires were deposited only on the raised GaAs layers by electron beam evaporation. Finally, the metal nanowires were transferred on a silicon substrate. This method was compatible with classical manufacturing methods of electronic products, and showed applications for one-dimensional electronics. In addition to superlattices, other laminated structures, such as block copolymers [63] and laminated films [64], can be used as templates for the preparation of nanowires. There are relatively few studies on the preparation of nanowires through laminated structures, which deserves further exploration. Another example of the template-based process is on-wire lithography. Qin et al [65, 66] reported an on-wire lithography method with controllable face-to-face gaps on a single nanowire, as shown in figure 3(b). Segmented Au–Ag and Au–Ni nanowires were electrochemically deposited in controlled porous alumina masks. Each segment of nanowires can be controlled by tailing the charge during electrochemical deposition. The bridging substrates were deposited by plasma-enhanced CVD. Finally, nanowires were released, and Ni was selectively etched with gap size down to \(~2\) nm. Nanowires with control gap size can be applied for electronics and biological sensing. The process is a high-throughput manufacturing method compared with other nanolithography techniques, such as e-beam lithography, ion-beam lithography, dip-pen lithography, etc.

The checkerboard structure with vertical resolution was also called vertically aligned nanocomposite thin films, which could indirectly achieve vertical thickness control with the regulation of temperature [67–69]. MacManus–Driscoll et al [69] got two mixed phases at high temperature by pulsed laser deposition. After low-temperature annealing, the two mixed phases were decomposed separately to form a nanocheckerboard structure with a vertical thickness of less than 10 nm. This structure is achieved by the differences between the thermodynamical stability and minimum interfacial energy of the two phases. It is interesting that the structures are free from substrate clamping, and strain manipulation in the vertical direction can be achieved through lattice mismatch between two phases with different elastic modulus. Many similar works fabricate the checkerboard structures in perovskite-spinel, perovskite-rocksalt, and perovskite-fluorite systems, which is suitable for the applications of ferroelectric or ferromagnetic devices [70]. However, the decomposition process is affected by many important factors, including film composition, substrate crystallinity and growth conditions. It requires careful selection of materials and regulation of microstructures. The checkerboard structures are hard to produce with conventional deposition methods. It opens novel ways for vertical resolution with enhanced functionalities.

2.2. Template-based resolution

In this section, the indirect processes using vertical resolution are introduced for special structures, such as nanowires patterning, on-wire nanogaps, checkerboard structures, etc. Since nanowires are low-dimensional structures, the resolution cannot be obtained by directly depositing on the sidewalls of the 3D structure. The resolution typically requires prefabricated templates and additional transfer steps. Therefore, the difficulty lies in obtaining a high-resolution template and controlling the transfer process. Moreover, the post-treatment of the external field can also obtain the vertical resolution in checkerboard structures that cannot be obtained by direct deposition. A lot of researches have been done to study the fabrication methods as follows.

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Figure 3. (a) Nanowire pattern transfer [61] and (b) on-wire lithography [66]. (a) Reprinted with permission from [61]. Copyright (2008) American Chemical Society. (b) Reprinted with permission from [66]. Copyright (2008) American Chemical Society.
precise size control of nanotubes and nanopores by deposition is a typical example for the vertical thickness control, which can be used as photoelectric devices, FETs, energy storage devices, catalysis, etc [71–74].

The shape of nanotubes can be tuned by the vertical film thickness control during atomic level deposition. For example, we [75] fabricated Co$_3$O$_4$/TiO$_2$ nanotube arrays with an aspect ratio of more than 100:1 by ALD for visible-light photoelectrochemical devices, as shown in figure 4(a). By tuning the number of ALD cycles, the Co$_3$O$_4$ layer with a controlled thickness from sub-nanometer to over 10 nm was coated onto the inner wall of TiO$_2$ nanotubes. The growth rate of Co$_3$O$_4$ was ∼0.4 nm cycle$^{-1}$. As a result, the nanopores’ diameter could be controlled by the Co$_3$O$_4$ cycles, and the photoelectrochemical properties can be feasible tuned.

When the number of cycles increases, the above method can shrink nanopores until they are completely filled. Nam et al [76] fabricated ALD modified nano-pores on Si$_3$N$_4$/TiN/Si$_3$N$_4$ membrane, as shown in figure 4(b). Before the ALD process, the initial nanopores were manufactured through e-beam lithography. After 1000 cycles of TiO$_2$ deposition, the pore size scaled down from 70 ~ 80 nm to only ∼1 nm, which was suitable for ionic FETs. Similarly, Sainiemi et al [77] tuned the perforation on silicon membranes by controlling the ALD cycles. This type of through-silicon via technology has attracted much attention for 3D integration of chips [78].

Beyond vertical resolution, free-standing nanotubes are fabricated by shrinkage of nanopores and removing the sacrificial template subsequently. The nanotubes show the same diameter as the porous sacrificial template. The thickness of nanotubes can be tuned by optimizing the deposition process. Sander et al [79] fabricated TiO$_2$ nanotubes on the porous alumina template by ALD, and then the nanotubes were released by etching of the alumina mask. In this situation, the inner diameter was fixed, and the tube wall thickness can be precisely controlled below 3 nm. Similarly, Ras et al [80] applied polymer nanorods as internal sacrificial templates to get nanotubes. After the ALD process, the polymer nanorods were decomposed at 300 °C. Then, outside nanotubes remained with controllable wall thickness down to sub-10 nm. Nanotubes have high surface-to-volume ratio, and their properties can be controlled by adjusting the size. The tailorable nanoscale building blocks are expected to be used in future nanoscale engineering.

In addition to ceramic materials, carbon materials can also be integrated into the fabrication method. Choi et al [81] deposited vertically aligned carbon nanotubes by CVD for FETs. The anodized aluminum oxide templates were used as sacrificial patterned substrates. The nanotubes fabricated by such a method showed a diameter of 20 nm and 50 nm. Generally, this method requires the prefabrication of
an easily removable template without compromising nanotube integrity. These deposition methods exhibited controllable vertical thickness below 10 nm, which is suitable for FETs, sensing, photovoltaics and photocatalysis. Other low dimensional structures beyond vertical resolution will be presented in section 4.

3. Template-assisted alignment

With the devices become more complex, the aligned growth of thin films has been considered as an essential aspect during nanomanufacturing. If alignment cannot be achieved, the problem of EPEs will be so difficult that the insulation performance of the devices will be deteriorated, and then the yield and stability of the devices will be reduced. To achieve alignment with high precision, it is a challenge to avoid or remove deposition nucleation on undesired areas. There are currently two methods to achieve alignment: self-aligned selective deposition and conventional patterning (including film deposition, lithography, and etching, etc) [10]. Selective deposition is an efficient and promising method to achieve alignment, which can reduce steps such as photolithography and etching. Also, alignment is an important application of selective deposition in the field of micro-nano manufacturing. Selective deposition is characterized by deposition only on designated areas, which is usually assisted by templates. The purpose of the templates is to limit the growth direction and/or block the deposition regions. The deposition happens on the growth areas uncovered by the template, while it is suppressed on the non-growth areas where the template is covered. The selectivity can be obtained or maximized through a template for materials that are even not sensitive to substrate differences. It is an effective solution to achieve alignment of 3D stacking structures for relaxing downstream processing steps of microelectronics. However, the loss of selectivity needs to be noticed, like ‘mushroom’ growth, defects on the non-growth areas, and so on [10]. Thus, selective removal, especially selective etching, is required to improve alignment accuracy and edge orientation.

Normally, it is effective to achieve deposition with high selectivity by using special templates. Table 1 summarizes different types of template-assisted selective deposition processes, including dielectric templates, patterned polymers, SAMs and so on. It is worth noting that the deposition techniques are CVD and ALD in table 1. Currently, the main deposition technology used in the semiconductor industry is CVD. With the help of templates, rapid selective CVD can be achieved, and the film thickness can reach more than 100 nm. MOCVD, also called MOVPE, is a branch of CVD. It uses organic compounds of the main group III–V elements and hydrides of the sub-group II–VI elements as the sources of crystal growth [82–84]. The vapor phase epitaxy is performed on the substrate by thermal decomposition to grow single crystal films for compound semiconductors and their multiple solid solutions. ALD precursors are very sensitive to the surface species of the substrate because of the characteristics of self-limiting reactions. It is usually suitable for the preparation of ultra-fine structures within 10 nm. It can even achieve high selectivity without a template (as shown in the section 4). By the way, the selectivity of PVD is less reported because it is difficult to inhibit the nucleation of gaseous particles with kinetic energy on the non-growth areas.

How to choose the appropriate templates depends on materials, manufacturing accuracy, technical maturity, etc. Dielectric templates are mainly used to achieve selective deposition in the semiconductor industry due to mechanical stiffness. Typical examples are STI, vias, holes and others. Through physical isolation, channel semiconductors of FETs are selectively grown on desired surfaces by MOCVD or MOVPE as well as contact or interconnect metals. For some materials that are hard to be etched, polymer templates patterned by lithography are needed. After deposition, lift-off steps are taken to remove polymers. In some situations, the deposition takes place on the sidewalls and the top surface of polymers, which makes lift-off steps challenging. A possible solution to the above issues is SAMs, which has been widely used in surface modification due to area-selective assembly. The adsorption and reaction rate of precursors on the SAMs and a clean substrate usually show large differences, and the selective deposition of targeted thin films can be achieved. However, SAMs modification is time-consuming during liquid immersion or printing, and it is not suitable for plasma-assisted processes and high temperature deposition. To achieve large scale production, vapor-based advanced processes are presented. In the future, area-selective deposition will show excellent prospects for versatile applications. With the help of the templates, chip makers can not only superimpose transistors directly in three dimensions, but also integrate multi-functionality, such as sensing, energy storage, etc., to obtain super chips.

3.1. Dielectric-based alignment

To achieve alignment, various structures of dielectric templates were researched, such as shallow trenches, vias, holes, nanotubes and so on. Dielectric templates have great mechanical stiffness and thermal stability. Thus, they exhibit great edge orientation and alignment accuracy. Unlike conformal deposition, this method is beneficial for the whole filling of target spaces. Typically, the preparation of these templates requires various sophisticated lithography techniques. Therefore, the accuracy of alignment is limited by the shape of templates. When the filling exceeds the height of the template, the restraint of selective deposition is released. Then, the selectivity is lost and ‘mushroom’ occurs, which requires additional post-treatment, such as etching or polishing. This strategy can achieve rapid space-selective filling, and the film thickness of selective deposition depends on the shape of templates.

Selective epitaxy by STI is a well-known example for alignments, which is widely used in high volume manufacturing of integrated circuits (ICs) [82–84, 115–122]. During IC fabrication, STI was created before the deposition of high mobility materials. As shown in figure 5(a), STI-oxide acted as a blocking template, and the Ge/LnP species exhibited epitaxial growth only in channel regions [84]. The Ge epitaxial growth
| Type                        | Process            | Materials                       | Process | Materials                         | Reference |
|-----------------------------|--------------------|--------------------------------|---------|-----------------------------------|-----------|
| Dielectric templates        | STI                | SiO\(_2\)/Si pattern          | MOCVD   | SiGe, strained Ge channels        | [82]      |
|                             | SiO\(_2\)/Si pattern | MOVPE                          |         | Ge, InP                           | [83, 84]  |
| SiO\(_2\) nanotube templates | Si substrate       | Selective area epitaxy         |         | III–V semiconductors               | [85, 86]  |
| Holes                       | SiO\(_2\)/Si pattern | Low-pressure CVD              | CVD     | Al                                 | [87]      |
|                             | SiN\(_2\)/Cu pattern |                                |         | Cu                                 | [88]      |
| Patterned substrate         | SiN\(_2\) layer on C-plane sapphire |                                |         |                                    |           |
| Patterned polymers          | Photolithography   | Photoresist                    | ALD     | Rh                                 | [90]      |
|                             | PS                 |                                 | ALD     | BaTiO\(_3\)                        | [91]      |
|                             | PMMA               |                                 | ALD     | TiO\(_2\)                          | [92]      |
|                             | PS, PVC, PTFE-AF   |                                 | ALD     | Al\(_2\)O\(_3\) and TiO\(_2\)     | [93]      |
|                             | PS                 |                                 | ALD     | CoO                                | [94]      |
|                             | PVP                |                                 | ALD     | Ir, Pt, Ru, Al\(_2\)O\(_3\), ZrO\(_2\) | [95]      |
|                             | PMMA               |                                 | ALD     | Pt                                 | [96]      |
| Microcontact printing       | PDMS               |                                 | ALD     | TiO\(_2\)                          | [97]      |
|                             | PMAM               |                                 | ALD     | Pt                                 | [98]      |
| Nanoimprint lithography     | PMMA               |                                 | ALD     | ZnO                                | [99]      |
|                             | E-beam lithography | PMMA, PVP, C\(_4\)F\(_8\)      | ALD     | TiO\(_2\)                          | [100]     |
| AFM lithography             | PMMA               |                                 | ALD     | TiO\(_2\)                          | [101]     |
| SAMs                        | Solution immersion | ODPA on CuO\(_2\)/SiO\(_2\) substrates | ALD     | ZnO                               | [102]     |
|                             | ODPA on CuO\(_2\)/SiO\(_2\) patterned substrates | ALD     | Al\(_2\)O\(_3\)                   | [103]     |
|                             | ODPA on copper/silicon pattern | MLD     | Polyurea                          | [104, 105]|
|                             | ODT on CuO\(_2\) substrate | ALD     | Al\(_2\)O\(_3\)                   | [106]     |
| Others                      | Vacuum-based processes | Si precursors on MoO\(_2\)/SiO\(_2\) pattern | ALD     | Ru                                 | [110]     |
|                             | H\(_2\) plasma     | a-C:H/SiCN                      | ALD     | Ru                                 | [111]     |
|                             | Hacac dosing       | Acetylacetone on GeO\(_2\), SiN\(_2\), SiO\(_2\), WO\(_1\), Al\(_2\)O\(_3\), TiO\(_2\), and HFO\(_2\) surfaces | ALD     |                                    |           |
|                             | Joule heating      | n+/n−/n+/n− polysilicon nanobelts | Plasma-enhanced CVD | Pt and ZnO                           | [113]     |
|                             | Ion implantation   | Si fin array nanostructures     | ALD     | Pt                                 | [114]     |

*PS: polystyrene; PMMA: poly(methyl methacrylate); PVC: poly(vinyl chloride); PTFE-AF: poly [difluoro-bis(trifluoromethyl)-dioxole-co-tetrafluorethylene]; PVA: poly(vinyl pyrrolidone); PDMS: poly(dimethylsiloxane); PMAM: polymethacrylamide; ODPA: octadecylphosphonic acid; ODT: octadecylthiol; DDT: dodecanethiol.*
was performed to deal with thermal budgets and lattice mismatch between LnP layers and the substrate. LnP layers were deposited on top of [110]-oriented trenches by MOVPE. After polishing and selective etching of ‘mushroom’ bulges, channel materials continuously grew on shallow trenches. The channel quality of selective epitaxy growth depended on many different factors, like STI structures, growth conditions and post-treatment processes. For example, Wang and coworkers [123] found that STI wider than 50 nm showed better channel filling ability than that of less than 20 nm. Merckling et al [83] studied three different deposition temperatures of LnP: 500 °C, 550 °C, and 625 °C, respectively. LnP grown on low temperature (500 °C) had higher defect density, while at high deposition temperature (625 °C) bad uniformity occurred as well as voids and pits. The above methods can achieve versatility by integrating different materials on one substrate.

The self-aligned growth can also be realized by nanotube templates. Compared with STI, this method removes the templates for free-standing nanowires. As shown in figure 5(b), Riel and coworkers [86] reported the preparation of aligned III–V nanowires in vertical direction by SiO₂ nanotube templates. 5 ~ 6 nm etch-stop layer and 500 ~ 800 nm sacrificial amorphous Si (α-Si) were deposited on Si wafers by CVD and sputter deposition, respectively. Electron-beam lithography and plasma reactive-ion etching were performed to get vertical α-Si nanowires. Then SiO₂ conformally deposited on patterned Si wafers. The top of nanowires was etched while SiO₂ template sidewalls remained. After selective etching of inner α-Si nanowires, the SiO₂ nanotube templates were fabricated. Finally, III–V semiconductors selectively initiated growth under the guiding of nanotube templates. Similarly, other inorganic isolation strategies were used to get aligned nanowires [124, 125]. Hertenberger et al [124] patterned SiO₂/Si substrates by lithography with 18 nm deep holes and a diameter of 80 nm. Then, vertical InAs nanowire arrays were fabricated within SiO₂ nanoholes by molecular beam epitaxy. It can be used to prepare nanowires with high processing accuracy and arbitrary shape. The scalable approach provides a feasible way for large-scale integration of electronic and optoelectronic devices.

Except for selective deposition of channel semiconductors in FETs, contact or interconnect metals of ICs also utilize sidewall isolation to achieve selectivity [87, 88, 126–130]. For example, Zheng et al [127] selectively filled Co on the bottom Cu surface of small vias by CVD. With the decreasing of vias’ critical dimension to sub-10 nm, the normalized resistance of conventional Cu vias increased greatly. After pre-filling the vias with Co, the resistance reduced by 30% at

![Figure 5. Aligned epitaxy growth by (a) STI templates [84] and (b) SiO₂ nanotube templates [86]. (a) Reproduced from [84]. © 2010 The Electrochemical Society. All rights reserved. (b) Reprinted with permission from [86]. Copyright (2014) American Chemical Society.](image-url)
Figure 6. (a) Selective deposition with polymers [97]; (b) passive and negative patterning by SAMs [139]; (c) nano-trap structure by SAMs [142]; (d) topographically selective deposition by ion implantation [114]. (a) Reprinted with permission from [97]. Copyright (2006) American Chemical Society. (b) [139] John Wiley & Sons. Copyright © 2006 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim. (c) [142] John Wiley & Sons. Copyright © 2017 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim. (d) Reprinted with permission from [114]. Copyright (2016) American Chemical Society.

7 nm node. The conductivity and selectivity of filler metals strongly depended on holes opening shape and deposition processes. The dielectric isolation technique is of great significance to improve selectivity as well as alignment. With the help of super vias, area-selective deposition will deal with process challenges on scaling boosters in the semiconductor industry. For complex structures, alignment can be realized through exploring the proper shapes of dielectric templates.

3.2. Inhibitor-based alignment

Surface modification by organic groups is a widely investigated method for alignment, including polymers, SAMs and other inhibitor molecules [131]. After modification, the chemical properties of the surface will be changed, thus selective deposition appears. Compared with dielectric templates, the inhibitors are easier to remove, but the edge orientation needs to be improved.

Patterned polymers are intensively investigated in recent years [132, 133]. For example, photoresist is wildly used as mask layers for area-selective deposition. Photoresist-based selective deposition has been applied to chips’ manufacturing. The polymers need to be patterned to expose growth areas by lithography. After deposition, the post lift-off or etching steps are necessary to acquire target patterns. Suresh et al [99] fabricated the nano-porous PMMA template on Si substrate by spin-coating and nanoimprint lithography, then followed by ZnO deposition. After removing PMMA films, the ZnO nanoarray with feature size down to sub-100 nm was demonstrated. Up until now, many lithography strategies have been researched to achieve patterned polymer templates. Park et al [97] prepared patterned PDMS films by microcontact printing, then TiO$_2$ thin films were deposited on Si substrate instead of PDMS thin films, as shown in figure 6(a). These methods combining lithography and polymer-assisted selective deposition will continue to play an important role in micro-nano manufacturing.

However, avoiding undesired nucleation on polymer templates is challenging. Thus, researchers developed alternative methods for selective deposition with high resolution. SAMs are extensively reported in the literature for selective adsorption and surface passivation [102, 134–138]. Moreover, SAMs can be easily removed through heating compared with polymer thin films. Usually, SAMs are organic ultra-thin films consisting of close-packed monomers synthesized by wet chemistry methods. Typically, the monomers contain three parts: head group, carbon chain, and tail group. The head group is chemisorbed on the substrate through covalent or ionic bonding. The carbon chain mutually repulses by van der Waals forces, which leads to an orderly arrangement. The tail group is
characterized by reduced surface energy for area-deactivation. SAMs are mostly used to deactivate substrates by solution immersion before deposition.

Through selectively attaching OTDS to SiO$_2$ surface by liquid method, Chen and Bent [139] selectively deposited HfO$_2$ on Si surface rather than on SiO$_2$, as illustrated in figure 6(b). When changing OTDS to 1-octadecene, hydride-terminated Si regions were blocked; thus, Pt nucleation only happened in SiO$_2$ regions during ALD. This area-deactivation strategy can be used in many patterned metal/dielectric nanostructures. It was reported that the Cu areas were selectively blocked prior to SiO$_2$ areas by different kinds of SAMs, and then deposition only happened in SiO$_2$ regions [104, 106, 108, 140]. Due to selective adsorption, other nanostructures were reported based on SAMs [141]. Liu et al [142] selectively grown ODT on Pt nanoparticles, then the Al$_2$O$_3$ substrate was coated by Co$_3$O$_4$. After removing SAMs by calcination, nano-trap structures were fabricated (see figure 6(c)). Through selective self-assembly, the two-step selectivity greatly expands the material boundary of selective deposition, and can be applied to the manufacturing of various nanostructures.

Like the polymers, SAMs can be combined with lithography for nanopatterning on the surface of the same material, such as the EUV technique [136], electron beam direct writing [143], dip-pen lithography [144] and nanoimprint technology [99]. Through lithography, the growth areas can be exposed to chemical adsorption, while the non-growth areas would still be blocked by SAMs. Although it faces the challenges of long processing time and arduous process coupling, it is able to achieve the area-selective growth of thin films less than 100 nm, which has enticing prospects in applications of electronics.

Except for SAMs, advanced vapor-based methods are also studied to achieve area-deactivation. For example, Khan et al [110] reported that Si precursors could be used as inhibitors to realize selective deposition on SiO$_2$ instead of Si. This vapor-based process can be integrated into the production lines for high volume manufacturing. Kim et al [114] selectively passivated horizontal areas of patterned Si substrate by ion implantation; then Pt films only occurred on vertical areas. This type of ALD was also named as topographically selective ALD, as shown in figure 6(d). This type of inhibitor is relatively small and needs a lot of excavation to meet future nanomanufacturing trends.

3.3. Correction steps of deposition for alignment

The inhibitor molecules for selective deposition face challenges for blocking the non-growth areas [145–149]. For example, the quality of SAMs is affected by temperature and substrate conditions during deposition. Thus, the defects are inevitable during ALD cycles. Low defect levels and corresponding metrology are necessary for high-volume production. In this section, advanced deposition with correction steps is discussed to improve selectivity and alignment performance.

The selectivity decreased because of pinholes, which is shown in figure 7(a) [147]. Avila et al [149] used the unsaturated models of SAMs during ALD cycles to analyze nucleation initiation and island growth. In the first stage, SAMs provided a good blocking effect. During this incubation period, the quantity of the deposition materials did not increase. Then, with the increasing of defect sites, the quantity of deposition materials increased exponentially in every subsequent cycle. Finally, when the nucleation islands converged and the sidewall areas decreased, the linear growth occurred. The defects of the SAMs need to be solved, and corresponding nanoscale features will become more important with further scaling of nanodevices. By the way, the pinholes of SAMs can also be utilized reversely to grow core–shell nanoparticles, and the pinholes density can be regulated with immersion time [150, 151]. For example, we [150] deposited Pd nanoparticles on pinholes of SAMs. Then, Pt ALD only occurred on Pd cores prior to densely blocked SAMs regions (see figure 7(b)). SAMs are versatile inhibitors, and the properties and applications deserve further investigation.

Due to the above problems, advanced selective deposition combining correction steps is investigated. Kalanyan et al [152] discovered that the selectivity of W ALD on patterned SiO$_2$/Si substrate usually decreased only after a few cycles. Through adding H$_2$ into W precursor dose, the SiO$_2$ regions were passivated for at least additional 10 cycles. The researchers attributed the passivation effect to HF formation, which passivated or removed surface species on SiO$_2$ regions. This diluted WF$_6$ delivery method expanded selectivity windows for sub-10 nm nanodevices. Recently, H$_2$ and H$_2$ plasma were reported to be an effective way to inhibit amorphous carbon on nanopatterning structures [111, 153, 154]. These methods have been proved to reduce impurities on the non-growth regions and undesired edge effects.

Except for corrected AB-type strategies, advanced ABC-type deposition methods are also researched. Through repeating surface modification steps after certain numbers of AB-type ALD cycles, ultrahigh selectivity for nanopatterning can be achieved. For example, Hashemi and Bent [108] developed a process by dosing the vapor molecules into the ALD process every 100 cycles. This strategy improved the selectivity by a factor of three. In order to improve the weak selectivity, it is necessary to shorten the time interval of functionalization. Mameli et al [112] found that SiO$_2$ deposited linearly on SiO$_2$ substrate in the initial stage, while there were only 10 ~ 15 cycles delay for nucleation on TiO$_2$, HfO$_2$, CoO$_x$, and MoO$_x$. The weak selectivity was improved by adding acetylacetone as inhibitors after less than 10 cycles. Furthermore, Yanguas-Gil et al [155] functioned the surface per ALD cycles to improve selectivity as shown in figure 7(c). Through repeating corrected steps, also called ABC-type cycles, selectivity can be significantly enhanced. This method overcomes the denaturation of inhibitors during deposition, and can obtain the high selectivity required.

Another method is to integrate selective etching into the selective deposition process. Selective etching, especially atomic layer etching, is an effective approach to remove materials on the non-growth areas. To maintain and improve selectivity between the growth and non-growth areas, adding selective etching into ALD cycles is suitable for the
nanopatterning. George and Lee [156] used HF and metal precursors as the reactants, and the substrate is exposed to the HF atmosphere to fluorinate a layer of atoms, followed by metal precursors to exchange ligands. Thus, thin films were etched layer by layer. It should be noted that metal oxides only reacted with specific metal precursors. For example, Al(CH$_3$)$_3$ only reacted with the fluorinated matrix of Al$_2$O$_3$ instead of SiO$_2$, ZrO$_2$, Si$_3$N$_4$ and TiN (see figure 7(d)). ALD cycles and ALD + ALE supercycles were compared by Song et al [157], the selectivity of supercycles is 10 times higher than that of traditional cycles. The thickness of TiO$_2$ on the non-growth Si areas decreased from 8.0 nm to zero after adopting supercycles. Moreover, Vos et al [158] added selective etching every 100 cycles to achieve area-selective deposition of ruthenium on Pt rather than SiO$_2$. After 800 cycles, 8 nm Ru was deposited on Pt regions, while SiO$_2$ regions were clean. ALE has attracted much attention because of its isotropy and selectivity. It is particularly suitable for complex 3D structures that cannot be achieved by traditional anisotropic etching. Coupling atomic level deposition and top-down etching will be research focus, and industrial applications seem to be approaching soon.

4. Non-template selective deposition

In the previous part, we introduce the selective deposition for alignment based on the assistance of various templates. However, the above methods have limitations for low dimensional materials and complex 3D structures, since it is challenging to prepare appropriate templates for selective deposition. Non-template selective deposition has been investigated. Because there are no templates and the emergence of low-dimensional materials, the film thickness is usually less than 10 nm, in some cases it is even only a single atomic scale in this section. Non-template selective deposition is of high interest since it is truly free of any resist films, inhibitors, etchants or lift-off chemicals. To realize high selectivity, inhibiting nucleation on the non-growth areas is desired. Recently, non-template selective deposition methods are exploited to deposit ultra-thin films on the specific materials while keeping the non-growth areas clean without additional treatments. To quantify selectivity, the generally accepted equation as follows [130]:

\[
\text{Selectivity} = \frac{\theta_{GA} - \theta_{NGA}}{\theta_{GA} + \theta_{NGA}},
\]

where $\theta_{GA}$ and $\theta_{NGA}$ are the numbers of nuclei or amount of materials deposited on the growth and the non-growth regions, respectively. In some conditions, the $\theta$ value is simplified as film thickness. If $S = 1$, there is perfect selective growth, and no target products appear on the non-growth surface. If $S = 0$, then there’s no selectivity at all. About selective deposition, it is worth considering what the desired selectivity for applications should be.

In this section, inherent selectivity, hyper-scaling selective deposition and single-site deposition will be discussed. So far, researchers find that some specific selective deposition reactions appear between metal (or metalloid) and dielectric, since
| Structure                  | Type                                        | Substrate materials     | Deposition materials | Deposition process | Reference |
|----------------------------|---------------------------------------------|-------------------------|----------------------|--------------------|-----------|
| Patterned substrate        | Inherently selective deposition             | SiO$_2$/Si substrate    | Ru                   | ALD                | [159]     |
|                            | Cu/Si substrate                            | HfO$_2$                 | ALD                  |                    | [160]     |
|                            | Pt/SiO$_2$ substrate                        | Fe$_2$O$_3$             | ALD                  |                    | [161]     |
|                            | TiN/SiO$_2$ pattern                        | Ru                      | ALD                  |                    | [162]     |
|                            | Direct-write deposition                     | Pt seed layer on Al$_2$O$_3$ covered Si | Pt | Direct-write ALD | [163] |
|                            |                                             | SiO$_2$ seed layer on Si | ZnO                  | ALD                | [164]     |
| Phase-selective deposition | ZnO/V/Zn substrate                         | Cu, Cu$_2$O             | ALD                  |                    | [165]     |
| Nanowires                  | 1D defects                                  | CVD graphene            | Pt                   | ALD                | [166]     |
|                            |                                             | Graphene                | Ru                   | ALD                | [167]     |
|                            |                                             | Graphene                | Ni                   | ALD                | [168]     |
|                            |                                             | Si                      | Ge                   | CVD                | [169]     |
|                            | Facet-selective deposition                  | Ti$_3$Si$_2$ nanosheets | Ru                   | ALD                | [170]     |
| Nanoparticles              | Core/shell                                  | Pt on nitrogen-doped carbon nanotube | ZrO$_2$ | ALD | [171] |
|                            |                                             | Pd on Al$_2$O$_3$-covered Si$_3$N$_4$ support | Pt | ALD | [172] |
|                            | Liquid-phased method                        | CdSe quantum dots       | CdS                  | Facet-selective epitaxy | [173] |
|                            |                                             | Pt nanocubes            | Au                   | Solution precipitation | [174] |
|                            |                                             | Hexoctahedral gold nanoparticles | Pt | Solution precipitation | [175] |
|                            | Vapor-phased method                         | Pt on Al$_2$O$_3$ support | CeO$_3$ | ALD | [176] |
| Single-site                | An atom                                     | Graphene                | Pd                   | ALD                | [177, 178] |
|                            |                                             | Si                      | P                    | Chemical doping    | [179, 180] |
|                            | A vacancy                                   | P-type NiO              | Al                   | Site-selective deposition | [181] |
two types of substrates present different surface chemical states. This type of selective deposition is classified as inherently selective deposition, then direct-write deposition and phase-selective deposition are also discussed. As for hyper-scaling selective deposition, low dimensional materials are the focus of the discussion, including 2D materials, nanowires, nanoparticles, etc. For example, line defects in 2D materials are eliminated by selective deposition. Another selective deposition occurs in different crystal faces of nanowires or nanoparticles, which is called facet-selective deposition or site-selective deposition. At the end, single-site selective deposition is a similar expansion, including an atomic vacancy and a single atom. Table 2 shows a lot of non-template selective deposition strategies. For the post-Si era, atomic level deposition can prepare many alternative nanomaterials, such as 2D materials, carbon materials, ferroelectric materials, phase transition materials, and so on, which can overcome the constraints of the physical limits of silicon materials and broaden the boundaries of Moore’s law.

4.1. Inherently selective deposition

Inherently selective deposition utilizes nucleation delay of thin films on different materials without the assistance of templates. Usually, the selectivity is easily lost once the nuclei appear on the non-growth areas. Thus, it is suitable for ultrafine structures. In this section, various patterned substrates for inherently selective deposition are presented, such as Si/SiO$_2$, metal/oxide, oxide/oxide, etc.

The development of transistors drives the inherently selective deposition of semiconductors and metals on Si/SiO$_2$ substrates. As early as 1962, Joyce and Baldrey [37] reported the selective deposition of Si on the Si substrate prior to silicon dioxide surface. The rate of nucleation on oxide layers has been minimized because of competition between nucleation and reduction in a hydrogen atmosphere at high temperature. Similarly, Minjauw et al. [159] found nucleation delay on SiO$_2$ for Ru deposition, and 60 cycles were the thresholds to start its growth on SiO$_2$ through in situ spectroscopic ellipsometry (see figure 8(a)). It was worth noting that hydroxyl groups on SiO$_2$ surfaces provided more active reaction sites for HfO$_2$ and ZnO ALD, which was different from the above works.

Roozeboom and coworkers [164, 182] patterned SiO$_2$ seed layer on Si substrate by EBID, the ALD cycles for nucleation delay on Si increased from 80 to 120 by increasing temperature from 100 °C to 250 °C, respectively. Similarly, McDonnell et al. [183] used dip-pen nanolithography to acquire SiO$_2$/Si nanopatterns, and the TiO$_2$ nucleation only occurred on SiO$_2$ areas (see figure 8(b)). The reason comes from the comprehensive effect of ALD nucleation reaction and surface catalysis between precursors (or co-reactants) and surface groups. Inherent selectivity usually exists only in specific material systems, and the regulation of selective window needs to be more refined for multi-functional applications. It is vital to develop more materials and obtain high selectivity without additional treatments.

Up to now, the inherently selective deposition based on surface differences has expanded its applications in many other fields. In this part, metal/oxide substrates are the most studied. Selective deposition on noble metals instead of oxide substrates is motivated by core–shell catalysts. Lu and coworkers [184] successfully deposited bimetallic core–shell nanoparticles while avoiding growth on oxide surfaces. The active sites on the surface are H$^+$ and O$^+$ for Pd ALD and Pt ALD, respectively. The introduction of ALD shows excellent thickness control at the atomic level and improvement of catalytic properties. Weber et al. [185] found that the Pt shells only occurred when the Pd cores were larger than 1 nm, and the selectivity mainly comes from different surface energy between metal and oxide substrates. They [163, 186] reported Pt nanopatterning structures through preparing EBID seed layers and selective ALD. The lateral resolution of Pt nanowires was only ~10 nm. EBID can pre-pattern the substrate in any planar shape, so some researchers named these processes as direct-write ALD [182, 187, 188]. The contact resistance of metals deposited by direct-write ALD is lower because there is no etchant residue. This approach is alternative to lithography and is more compatible with sensitive nanomaterials.

Except for metal on metal, the selectivity ofoxide on metal prior to oxide is investigated. Bent and coworkers [161] found that Fe$_2$O$_3$ ALD exhibited excellent selectivity on Pt versus SiO$_2$ up to 2000:1 by elemental counts of auger electron spectroscopy. Also, the Fe$_2$O$_3$ and NiO ALD on SiO$_2$ substrates with patterned iridium showed selectivity of 900:1
and 200:1, respectively. The selectivity existed not only in patterned bilayer films, but also in core/shell nanoparticles. The oxide substrates cannot catalyze co-reactant O$_2$. Thus, there is no activated O$_2$ that can participate in the ALD precursor decomposition. The selectivity comes from lower chemisorption energy and activation energy on metal regions. It is worth noting that the difference in surface activity between metal and oxide always exists, whether it is 3D structures, 2D planes or nanoparticles. For the above reasons, the inherent selectivity between the two different materials always exists once the appropriate target materials appear.

Different from the above area-selective deposition, the phase-selective deposition methods allow different phases to grow synchronously on different surfaces [189]. De Melo et al [165] prepared patterned ZnO/Al-doped ZnO films by e-beam lithography. After 10 000 ALD cycles, Cu selectively deposited on the Al-doped ZnO regions, and Cu$_2$O selectively grown on ZnO areas. The authors attributed it to substrate conductivity. Cu was grown on high conductive regions, while Cu$_2$O was deposited on low conductive areas. This selectivity is difficult to exist, so it has rarely been reported. It is believed that phase-selective deposition will significantly expand the applications of selective deposition.

4.2. Hyper-scaling selective deposition

Now, the semiconductor industry enters the hyper-scaling era, and the applications of low-dimensional materials are in the ascendant, like 2D materials, 1D nanowires, nanoparticles, etc. Since the surface species are identical on the same materials, it is very challenging to achieve selective deposition. In this situation, a slight difference in free energy is a possible way to achieve selectivity. In this part, the hyper-scaling selective deposition will be discussed. It is widely researched for applications of electronics, catalysis, displays, energy storage, etc.

To extend Moore’s law and beyond, 2D materials are reported as promising candidates of FET channel materials [190–193]. Huang and Liu [194] synthesized 2D MoS$_2$ by ALD with only a few atomic monolayers. It is easy to break the weak interlayer combination depending on van der Waals force. The number of layers can be controlled from 1 to 10. Similarly, semiconductor materials can also be processed to obtain layered structures. Wang et al [195] synthesized 2D semiconductor nanocrystals with uniform monolayer thickness. Although the thickness of 2D materials is only nanoscale or sub-nanoscale, they do not have short channel effects compared with bulk Si materials. Also, excellent mobility makes them promising candidates for post-silicon electronics. 2D materials can only be deposited on some specific substrates. How to selectively deposit them into specific shapes and integrate them into semiconductor production lines are difficult.

For the manufacturing of 2D materials, many methods are being explored. One-dimensional defects in 2D graphene will deteriorate the electrical properties, selective deposition of metal on defects is developed [166–168, 196, 197]. Bao and coworkers [166] found that Pt was selectively deposited on CVD graphene’s line defects after 500 ALD cycles. After 1000 cycles, isolated Pt exited at point defects. During 300 cycles, the authors calculated that Pt nucleation density at grain boundaries was 440 times higher than that of graphene grains. The researchers contributed it to different reaction energies. Moreover, EBID and EBIS have become important ways to manufacture them with high resolution down to the angstrom level [198]. These methods are not only conducive to the development of electronics, but also applied in the emerging fields of sensing, catalysis, energy, etc.

Selective deposition happens during two types of materials raising from different active sites. But for the homogeneous low-dimensional materials, the only difference comes from different crystal faces with different surface activity. Recently, many attempts of vapor-based selectivity on low-dimensional structures are investigated to expand Moore’s law. Kempa et al [169] synthesis Si nanowires by CVD. Then three types of Ge shells were grown on Si templates. Through revealing GeH$_4$ at 380 °C, Ge deposited isotopically on nanowires’ surface with an estimated growth rate of 10 nm min$^{-1}$. After adding PH$_3$ and Ar at the same temperature, the growth rate increased in the order of (111), (011) and (113). During accessing H$_2$ at 330 °C, high selectivity achieved. Ge only showed growth on (111) (2 nm min$^{-1}$) and (011) (1 nm min$^{-1}$) surfaces instead of (113) surfaces. Moreover, they found that Si was only selectively grew on (111) surface of Si nanowires at 650 °C with Si precursors and H$_2$. It is crucial to control the process window during deposition, including temperature, pressure, gas type and flow rate, etc. This selective regulation method has a bright future in nanowire transistors.

As for zero-dimensional structures, many researchers found that selective deposition can be obtained at Au [175], TiO$_2$ [199, 200], Ag [201] and quantum dot [173] nanoparticles through the liquid-phase deposition. The vapor-based selectivity on nanoparticles is mostly driven by the field of catalysis. We [176] fabricated nano-fence CeO$_x$/Pt structure catalysis through facet-selective ALD. CeO$_x$ was selectively deposited on Pt (111) facets to prevent sintering, while Pt (100) facets with higher catalytic activity were exposed (see figure 9(a)). Also, Wang et al [202] found that the TiO$_2$ firstly coated low-coordination sites of Au (see figure 9(b)). Before 5 ALD cycles, the catalysis activity was improved remarkably due to the exiting of Au-TiO$_2$ interfaces. After 20 ALD cycles, active sites were gradually covered. Thus, the catalytic performance was greatly influenced by the oxide thickness. Up to now, several selective ALD methods in the catalysis field are reported, including embedded structures, discontinuous coating structures and core–shell structures, etc [203].

The deep understanding of selectivity is also studied based on the theoretical investigation. Edge-selective ALD (see figure 9(c)) is brought up by McCp$_2$ (M = Fe, Co, and Ni) precursors on Pt nanoparticles, the preferential growth was in the order of edge >(100) > (111), which was verified by first-principles calculations [204, 206]. Also, Hu et al [205] found FeO$_x$ firstly decorated (221) sites, then followed with (211) and (111). The adsorption energy decreased in order of (221) > (211) > (111), which contributed selective deposition (see figure 9(d)). It can be further optimized by thermodynamics and dynamics to obtain high selectivity, like precursor activity, cavity pressure, reaction temperature, etc.
4.3. Single-site deposition

Site-selective deposition comes into people’s eyes due to the applications of displays and energy. For example, perovskite quantum dots are stabilized by coating nanoscale alumina via ALD (see figure 10(a)) [207]. During ALD, regions with long chain protection were absent of alumina, while non-protected sites were selectively passivated. There was no significant deterioration in performance after 100 min, while the performance without treatment dropped to zero within 1 min. As for P-type semiconductors, vacancy defects deteriorate properties of the materials [208]. Flynn et al [181] selectively passivated vacancy defects by ALD. Due to the existence of reactive oxygen bonds, site-selective deposition happened only on vacancies. After that, the performance of solar cells improved by a factor of 3. The above improvement of performance is the synergistic effects of many isolated single-site selective deposition.

Except for nanoparticles, a single-atom also shows its potential applications on semiconductor nanodevices. Single-atom transistors are proposed as a promising route for the hyper-scaling era [179]. Fuechsle et al and Petta [180, 209] doped a single P atom into the epitaxy Si surface by chemical doping with atomic precision (see figure 10(b)). Saturation dosing induced dissociation of three PH$_3$ molecules at three dimer sites. After heating to 350 °C, PH$_2$ underwent two steps of dissociation to a single P atom. At last, the Pt atom incorporated into the top surface of Si lattice accompanied by the spray of silicon atoms. Except for chemical methods, there are physical manipulation approaches of a single-atom, including AFM [210], STM [211] and STEM [212]. In the future, the development of commercial single-atom manipulation technology will be the commanding point of atomic or close-to-atomic scale manufacturing.

5. Summary and perspectives

In this review, we summarize the development of atomic level deposition approaches for nanomaterials and nanostructures, which will extend Moore’s law and beyond. To improve the density of transistors, double patterning and multi-patterning approaches are developed. These processes are characterized by bringing the lateral sub angstrom resolution to vertical. Similar approaches are also investigated to fabricate nanostructures, such as nanowires, nanopores, nanotubes and so on. On the other hand, alignment with high precision has become a major challenge for the fabricating of complex 3D structures. Selective deposition can achieve self-alignment with a smooth surface and streamline the manufacturing process. For depositing aligned stacking structures, two types of selective deposition methods are developed, including template-assisted deposition and inherently selective deposition. To further decrease the size of devices, atomic
level deposition methods have also been studied to fabricate nanostructures, like nanosheets, nanowires, nanoparticles and single-atom.

To achieve nanomanufacturing with high precision, the mechanism of atomic level deposition needs in-depth study. First, the growth behavior in the primary stage of deposition is critical as it determines the nucleation and quality of films. For example, the surface roughness can be reduced by promoting lamellar growth and inhibiting island nucleation. Then, to obtain high-quality thin films, it is necessary to explore the process window to reduce the defects formation and byproducts reaction. Finally, the issue calls for the development of in-situ characterization methods for the manufacturing processes. In situ studies of the reaction mechanisms can provide more information that is needed for further improving deposition approaches.

Although the characterization technologies are booming, the single-atom characterization and manipulation technology still have vast room for improvement. In the future, micro-nano manufacturing will develop with the trend of ultrahigh accuracy, especially in the semiconductor industry. At the atomic and close-to-atomic scale, methods are needed to achieve direct manipulation and characterization, like AFM, STM and STEM. AFM has the advantage of strong adaptability without surface treatment and vacuum environment. Moreover, it has strong expansibility for almost all types of materials. However, non-real-time topography is the biggest obstacle to AFM. For STM, it is only suitable for conducting materials and sensitive to materials’ surface and mechanical vibration. Up to now, it is flexible for very low temperature detection, ultrafast scanning, liquid phase testing, etc. As for STEM, it can only test ultrathin nanomaterials without 3D topography, but the resolution can be as small as 0.05 nm. Although the above techniques are powerful tools for atomic physics and chemistry, they are still in their infancy for atomic manipulation with rapidity and stability.

To achieve complex nanostructures fabrication, multiple processes coupling is indispensable for various materials. The conventional processing is widely exploited with patterning, lithography, etching and strip processes. However, only a few selective deposition schemes are adopted in the semiconductor industry, which is mainly because that only a few materials obtain high selectivity. It is of great significance to obtain selective deposition of new materials by optimizing the deposition processes. To balance deposition rate and step coverage, it is very effective to use different deposition methods, like PVD, CVD, ALD and so on. Newly developed spatial ALD is expected to be used to improve the efficiency for large-area
production [213]. Due to the trade-off between accuracy and efficiency, combining atomic level deposition and top-down processing could be attractive for multi-dimensional structures with exponential complexity. Thus, subtractive manufacturing like atomic layer etching and topological etching are needed to remove impurities on the non-growth areas during selective deposition.

In addition, the integration of the atomic level deposition methods also has great advantages for cross-scale processing during chip manufacturing. The versatile applications will promote cross-scale nanofabrication from atom manipulation to atom/molecule self-assembly to nanoparticle synergy to multi-dimensional structures, which increase the complexity and coupling difficulty of the process. In cross-scale manufacturing, other issues need to be considered, such as interface effects, alignments and thermal management. 3D integration and package are promising architectures to overcome the size limitation and increase device performances, like chip-to-chip, chip-to-wafer and wafer-to-wafer strategies. Edge flatness and smooth interface control will be important considerations for atomic scale deposition in 3D integration, which needs precise control of pressure, temperature, flow rate, etc. Moreover, many innovative schemes are needed to deal with the challenges of defect tolerance and thermal densities. Offering heterogeneous integration and monolithic 3D integration, the methods will help to extend Moore’s law by high density and multi-functionality. Moreover, the multi-dimensional manufacturing technologies have great potential for both ‘more Moore’ and ‘more than Moore’ applications [214].

Besides fabricating thin films and nanostructures with high precision, accuracy and processing efficiency are inter-inhibitive factors. The development of manufacturing equipment to achieve high throughput production is desired. On the other hand, the complexity of packaging devices requires the back-end equipment to support heterogeneous integration and assembly. In order to meet the needs of high-value heterogeneous system integration, it is necessary to integrate the front-end equipment and the back-end equipment soon.

Atomic level deposition is developed to extend Moore’s law and expand more versatile applications. For microelectronics, the deposition will continue to play an important role with the critical size down to sub-7 nm. It is gratifying to see that optimized deposition methods can improve both the performance and stability of nanodevices. Atomic level deposition methods also have full potentials for emerging applications, include energy, environment, biomedical, flexible electronic, etc. Therefore, the applications of Moore’s law are not limited to microelectronics manufacturing, it will become a platform to support optics, magnetism, acoustics and biotechnology, etc to realize the transformation beyond the integration of Si-based electronic technology. In these areas, atomic level deposition still plays an important role beyond Moore’s law.

In summary, atomic level deposition provides a technological driving force for the development of micro-nano manufacturing, especially in the semiconductor industry. Firstly, the processing accuracy ranges from micron to nanoscale, even to atomic scale; secondly, the deposition materials expand from traditional semiconductors and metals to emerging 2D materials, carbon materials, ferroelectric, etc; finally, the manufactured structures include high aspect-ratio structures, nanotubes, nanowires, nanoparticles, and so on. Moreover, 3D integration allows high-density placement and functional diversification. Thus, atomic level deposition enables integrated manufacturing of nanomaterials, nanostructures, nanodevices and nanosystems with high accuracy to extend Moore’s Law and beyond.

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