Research on SCESS-DFIG DC Bus Voltage Fluctuation Suppression Strategy for Frequency Inertia Regulation of Power Grid

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\textbf{ABSTRACT} The doubly fed induction generator with super capacitor is helpful to enhance the system inertia. At the same time, its structural characteristics are more suitable for the power grid topology without communication lines. However, the change of its topology also brings some problems. In this article, when SCESS-DFIG is participating in frequency regulation, DC bus voltage fluctuation caused by power imbalance of multiple converters is studied. The dynamic power response of super capacitor with DC-DC converter is a step load for grid side converter. The load of DC bus is nonlinear and random, so the balance and stability of the original system will change accordingly. Because of the complex topology and system composition of the doubly fed induction generator with super capacitor, the conventional feed-forward compensation control strategy can not be used to improve its dynamic response speed. Therefore, this article designs a control strategy which is applied for DC bus voltage fluctuation of the doubly fed induction generator with super capacitor. The theory proposed in this article is verified by simulation model and experiment.

\textbf{INDEX TERMS} SCESS-DFIG, frequency regulation, DC BVF, power balance, ADRC.

\section{I. INTRODUCTION}

With the increase of the penetration of wind power, its operation characteristics make it lack the inertia response, primary frequency regulation and other functions of conventional synchronous generator set. This weakens the stability of the grid [1], [2].

Therefore, as shown in [3], the doubly fed induction generator (DFIG) with super capacitance (SCCESS-DFIG) is proposed. The SCESS-DFIG has the inertial response capability through control. In [4]–[7], it is proposed that SCESS-DFIG can suppress the influence of wind speed change on its output power. Reference [8] is proposed that SCESS-DFIG can improve its low voltage ride through performance. However, these studies mainly focus on the power level control strategy, without considering the impact of increasing DC-DC converter on DFIG operation. It should be noted that the essential difference between DFIG and SCESS-DFIG is the addition of DC-DC converter. In order to simplify the process of transforming DFIG into SCESS-DFIG, the capacity of DC bus support capacitance is not changed. RSC and GSC in SCESS-DFIG keep the original control target. The DC-DC converter provides damping power when the grid frequency changes, and its control command is power signal. The control mode is power outer loop and current inner loop. This will effect operation stability of SCESS-DFIG. This is due to the addition of super capacitor energy storage device, DC bus has multiple converters. It includes DC-DC converter, GSC and RSC. DC-DC converter and super capacitor are step load for GSC. The power imbalance among multiple converters will cause DC bus voltage fluctuations (DC BVF). It has an adverse effect on the life of DC capacitors and power devices of converters, and even damage the devices, bringing down the system [9].
Therefore, it is necessary to improve the response speed of GSC by changing its control strategy to reduce DC BVF.

In [10], DC BVF is divided into disturbance fluctuation [11]–[17] and oscillation fluctuation [18]. In this article, the voltage fluctuation of support capacitor of SCESS-DFIG belongs to disturbance fluctuation.

The ways to control the DC BVF can be divided into hardware design and software design.

Hardware design. Wang H aims at the problem of DC bus power imbalance and voltage fluctuation of Back-to-Back (BTB) PWM converter, the most direct and simple method is to increase the capacitance of capacitor [9]. Zhong Q C adopts a new topology of converter, and adds auxiliary capacitance can also stabilize the power imbalance of DC bus [19]. But this method will reduce the power density of converter, increase the volume and cost, and slow the dynamic response speed.

Software design, in [11], the control effect of the current feed-forward method is verified, which proves that the method can reduce DC BVF. In [12], [20], a first-order differential is added to compensate the current control loop delay based on the steady-state full compensation, which is introduced into the DC BVF control application of the AC-DC hybrid microgrid to improve the robustness and disturbance control effect of the system. In [13], DC BVF power feed-forward control method based on BTB converter is proposed. The complementary sliding mode control (CSMC) is used to improve the DC BVF of PWM converter in [14]. According to the DC power balance relationship, [15] proposes a GSC output current compensation control strategy to ensure the stability of the DC bus voltage. Reference [16] proposes that on the basis of power compensation, the dynamic energy required should be compensated in stages with several switching cycles. However, the energy flow relationship in [15], [16] can still be attributed to one-way grid connection, which is essentially different from the two terminal power supply. In the two terminal power supply architecture, two converters adopt the control strategy that one end controls the DC bus voltage and the other end controls the active power. At this time, the DC BVF is no longer only caused by the disturbance of single terminal network side and DC load, and the jump of active power command of power control at the other end will also cause the DC BVF.

In [17], a scheme of BTB converter low voltage DC distribution equipment is proposed. The device integrates two converters and has high power density. Aiming at the core problem of DC voltage stability of converter, the mechanism of DC voltage fluctuation is analyzed by small signal modeling method from the point of view of DC bus power and energy balance. This article proposes a DC voltage stability control strategy with multi-disturbance momentum introduced into current loop to realize DC voltage stability control of low-voltage DC distribution equipment.

For the multi converter coordinated control of SCESS-DFIG structure, the existing researches is very few. How to optimize the control strategy to improve the response speed of GSC has a certain value. At the same time, the load characteristics of RSC and DC-DC are non-linear, so ADRC is used to enhance the dynamic response speed and anti disturbance ability of GSC.

In addition, in software design, ADRC is a practical new digital control technology that draws on the achievements of modern control theory [21]. In [22], ADRC is used in PWM converter grid frequency control. Based on the linear active disturbance rejection control (LADRC) strategy proposed by Gao [23], an observer based controller is proposed to regulate the DC-link voltage of the AC/DC converters against capacitance parameter variation [24]. In [25], considering the bandwidth of the closed-loop current dynamic, this article presents a novel DC-link voltage control strategy of PWM rectifiers based on the reduced-order linear extended state observer (RLESO). Using a RLESO to observe and even compensate the model variations caused by grid voltage and DC BVF or load disturbance, the proposed method can effectively improve the dynamic performance against grid and load disturbances, as well as for sudden changes in DC-link reference voltage.

This article designs a GSC control strategy for SCESS-DFIG. The purpose is to reduce DC BVF in the process of SCESS-DFIG output power regulation. For the voltage loop of GSC, the easily realized discrete LADRC control was adopted. For the current loop of GSC, the current feed-forward compensation was carried out by the mathematical model of the whole system. Due to the structure characteristics and sampling point distribution of SCESS-DFIG, compensation power needs to be calculated according to DFIG speed and grid state. The control strategy was verified by building simulation models and physical experiments.

II. ANALYSIS OF SYSTEM OPERATION CHARACTERISTICS OF SCCESS-DFIG

A. SCCESS-DFIG TOPOLOGY AND POWER FLOW ANALYSIS UNDER DIFFERENT CONDITIONS

As shown in Fig.1, SCESS-DFIG is an integrated power generation system composed of the super capacitor and DFIG. The first is to change the power of DFIG by controlling the RSC, and the second is to absorb or release energy by super capacitor. Therefore, as shown in Fig. 2 and Fig. 3,
the instantaneous power of SCESS-DFIG is adjustable. This makes the new energy generation system have inertia response and primary frequency regulation.

There are many variables in (1)∼(4), the meaning of the variables is explained in the appendix. The power of DFIG capturing mechanical power caused by wind speed change is shown in (1).

\[
\begin{align*}
P_{\text{mech}} &= 0.5\rho \pi R^2 V_w^3 C_p(\lambda, \beta) \\
C_p &= 0.73\left(\frac{151}{\lambda_i} - 0.58\beta_i - 0.002\beta_i^2 1.4 - 13.2\right)e^{-18.4/\lambda_i} \\
\lambda &= \frac{R \Omega_m}{V_w} \\
1 &= \frac{1}{\lambda + 0.02\beta_i} - 0.003 \beta_i^2 + 1
\end{align*}
\]

Fig.2 shows the power flow diagrams of DFIG and SCESS-DFIG at different speed conditions (sub-synchronous speed and super-synchronous speed). RSC is the load and GSC is the power supply in traditional DFIG. Therefore, instantaneous power balance is easier to control. SCESS-DFIG has not only dual PWM converters, but also DC-DC converters. This is equivalent to two loads and one power supply. It is special that the DC-DC converter is not a voltage regulation control, but a power control in the application of SCESS-DFIG.

In SCESS-DFIG, the power of RSC \((P_{\text{SD,RSC}})\) and the power of GSC \((P_{\text{SD,GSC}})\) are no longer the same. The power relations among the multi-converters (RSC, GSC, DC-DC) are shown in (2). \(P_{\text{SC}}\) is the power of super capacitor.

\[
P_{\text{SD,GSC}} - P_{\text{SD,RSC}} = P_{\text{SC}}
\]

As shown in Fig.3, the instantaneous power of SCESS-DFIG can be adjusted in a wide range under most operating conditions. This is different from DFIG. Therefore, it has the ability to participate in the power grid frequency regulation.

The load characteristics of RSC and DC-DC are different. The following is a simulation analysis of them.

1) LOAD CHARACTERISTICS OF RSC
When DFIG operates under MPPT condition, \(P_{\text{SD,rsc}}\) is shown as follows (3).

\[
\begin{align*}
k_\lambda &= 0.5\rho \pi R^5 \lambda_{opt}^3 N^3 C_{p_{max}} \\
P_{\text{DFIG}} &= k_\lambda \Omega_m^3 = k_\lambda (\frac{\Omega_m}{pN})^3 \\
P_{\text{SD,rsc}} &= s P_{\text{DFIG}}
\end{align*}
\]

As shown in Fig.4, the DFIG with variable wind speed is simulated. Fig.4 (a) is the wind speed curve. Fig.4 (b) is capture mechanical power for the fan. Fig.4 (c) is the rotor speed of DFIG. Fig.4 (d) is output power of RSC. The characteristics of wind make the instantaneous power of RSC random and nonlinear.

\[\text{FIGURE 2. The power flow diagrams of DFIG and SCESS-DFIG at different speed conditions.}\]

\[\text{FIGURE 3. Operation characteristics of DFIG and SCESS-DFIG at different wind speeds.}\]

\[\text{FIGURE 4. Load characteristic analysis of RSC.}\]
2) LOAD CHARACTERISTICS OF SCESS
The calculation of frequency regulation power is shown in (4):

\[ P^*_{F} = H \frac{f}{f_N} \frac{dL}{dt} \]  

As shown in Fig.5, when the grid frequency drops, the super capacitor provides inertia response power by sampling the grid frequency. The characteristic of inertia response power is step and nonlinear.

![FIGURE 5. Load characteristic analysis of the DC-DC converter.](image)

Based on Fig.4 and Fig.5, the DC bus voltage comparison between DFIG and SCESS-DFIG is shown in Fig.6. DFIG does not have the ability of frequency inertia response. At 1s, the wind speed decreases gradually, RSC power decreases, and the load decreases for GSC. The voltage of DC bus is maintained at 2000V. Due to the inertia response capability of SCESS-DFIG, when the grid frequency drops, DC-DC output power participates in the grid frequency regulation. The load of the GSC suddenly increases. As shown in Figure 6, the maximum DC BVF of SCESS-DFIG is 132V. But this is not the worst. If the wind speed suddenly increases in 1s, the load change rate of GSC will be greater, and DC BVF will be more than 10%. Therefore, if the GSC of SCESS-DFIG keeps the original control strategy, the voltage of the supporting capacitor is likely to be too high or too low. The high voltage will cause the damage of the supporting capacitor and even cause the whole wind turbine to be destroyed.

![FIGURE 6. Comparison of DC bus voltage between SCESS-DFIG and DFIG.](image)

B. THE MATHEMATICAL MODEL OF GSC
The GSC topology is shown in Fig. 7. The meaning of the variables in the (6) is explained in the appendix.

Suppose two IGBT switching functions \( S_k (k = a, b, c) \) on an independent bridge arm are turned on, while the lower arm is turned on at 1, and turned off at 0. According to Kirchhoff’s law of voltage, the mathematical model in three-phase stationary coordinate system can be obtained as shown in (5):

\[
\begin{align*}
L \frac{di_{g_d}}{dt} + R_i i_{g_d} &= (u_{gsc,a} + u_{NO}) - u_{ga} \\
L \frac{di_{g_b}}{dt} + R_i i_{g_b} &= (u_{gsc,b} + u_{NO}) - u_{gb} \\
L \frac{di_{g_c}}{dt} + R_i i_{g_c} &= (u_{gsc,c} + u_{NO}) - u_{gc} \\
C \frac{dU_{dc}}{dt} &= i_{load} - i_{dc}
\end{align*}
\]  

In this article, power grid voltage orientation is adopted. After Clark and Park transformation, the mathematical model of GSC in \( d \) and \( q \) coordinates can be obtained as follows:

\[
\begin{align*}
u_{gd} &= Ri_{gd} + L \frac{di_{gd}}{dt} - \omega_1 i_{liq} + v_{gd} \\
u_{gq} &= Ri_{gq} + L \frac{di_{gq}}{dt} + \omega_1 i_{liq} + v_{gq} \\
C \frac{dU_{dc}}{dt} &= \frac{3}{2} (S_d i_{gd} + S_q i_{gq}) - i_{load}
\end{align*}
\]  

Among them, the meaning of the variables in the (6) is explained in the appendix.

As shown in Fig.8 below, two groups of simulation are rectifier controller backend connected with non-linear load. One group of curves are simulation results of independent control without feed-forward power compensation, and the other group are simulation results with power feed-forward. As shown in Fig.8(a), the instantaneous power response speed of PWM rectifier with feed-forward compensation is faster. As shown in Fig.8(b), its voltage fluctuation of the supporting capacitor is smaller and the recovery speed is fast.

![FIGURE 8. The effect of power feed-forward control on PWM control.](image)

Due to the SCESS-DFIG topology, the voltage and current measurement points are fixed, and the power of the “load” is
not convenient for direct measurement. The general capacity of wind turbines is MW level. The addition of new sensors increases the complexity of the system and the extra cost.

III. GSC CURRENT LOOP CONTROL STRATEGY BASED ON POWER-ENERGY BALANCE

A. EFFECT OF SAMPLING POINTS ON POWER FEEDFORWARD CONTROL

According to the power flow analysis under different conditions in Fig. 2, SCESS-DFIG can be divided into six operating conditions. The description for each case is shown in Fig. 9 and Table 1.

![Power diagram of SCESS-DFIG under different operating conditions](image)

**FIGURE 9.** Power diagram of SCESS-DFIG under different operating conditions.

**TABLE 1.** The Power flow direction of different operating conditions.

| Operating conditions | The Speed of DFIG | \( \frac{df}{dt} \) | The power of RSC | The power of DC-DC converter | The power of GSC power |
|----------------------|------------------|-----------------|-----------------|-----------------------------|-----------------------|
| I                    | Sub-synchronous  | > 0             | < 0             | < 0                     | < 0                   |
| II                   | Sub-synchronous  | > 0             | < 0             | > 0                     | < 0                   |
| III                  | Super-synchronous| > 0             | > 0             | < 0                     | < 0                   |
| IV                   | Super-synchronous| > 0             | > 0             | > 0                     | < 0                   |
| V                    | Sub-synchronous  | > 0             | > 0             | > 0                     | > 0                   |
| VI                   | Sub-synchronous  | > 0             | > 0             | > 0                     | > 0                   |

As shown in Table 1, the operation of SCESS-DFIG is divided into six working conditions according to rotor speed, frequency change rate of power grid, power flow direction of RSC, DC-DC converter and GSC. As shown in Fig. 9, the power flow direction of each converter, rotor speed state and the change rate of grid frequency under each working condition of SCESS-DFIG are described.

For example, when DFIG operates at sub-synchronous speed, the rate of grid frequency change increases. The current of RSC converter flows from supporting capacitor to motor, super capacitor absorbs power, and the current in GSC converter flows from grid to supporting capacitor. At this time, SCESS-DFIG operates under condition I. When DFIG operates at super synchronous speed, the frequency change rate of power grid decreases. At this time, the current of RSC flows from the motor to the supporting capacitor, the super capacitor releases the power, and the current of GSC flows from the supporting capacitor to the grid. At this time, SCESS-DFIG operates under condition IV. When SCESS-DFIG transitions between operating conditions I and IV, due to the instantaneous power imbalance, the DC bus voltage fluctuates the most.

The following will analyze the effect of RSC and DC-DC converter on GSC feed-forward compensation control strategy when SCESS-DFIG participates in grid frequency regulation.

1) POWER AND ENERGY ANALYSIS OF RSC

As shown in Fig. 10, the topology diagram of DFIG and RSC is given. The sampling point of the RSC is at the stator side of DFIG, which has voltage sensor and current sensor. The relationship between \( P_{SD_{es}} \) and \( P_{SD_{rsc}} \) is shown in (7).

![Topological topology and sampling points of DFIG and RSC](image)

**FIGURE 10.** Topological topology and sampling points of DFIG and RSC.

The relationship between \( P_{SD_{rsc}} \) and \( P_{SD_{es}} \) is as follows:

\[
P_{SD_{rsc}} = s \left( P_{SD_{es}} + 1.5 R_s i_{sd}^2 + \frac{dE_{L_{es}}}{dt} \right) \quad (7)
\]

Among them, \( E_{L_{es}} \) is the variation of inductance energy due to current change in stator winding.

From the initial time of dynamic response to the steady time, the energy on the winding has a changing process. As shown in Fig. 11 (a), the stator current increases from 1pu to 1.2pu (where pu represents only one unit, not the rated current, but only the scalar of the research conditions). As shown in Fig. 11 (b), the energy stored in the inductor is a periodic variable. But as shown in Fig. 11 (c), the sum of the energy of the instantaneous three-phase winding is a scalar.

For three-phase windings, the total instantaneous energy is as follow:

\[
E_{L_{es}} = \frac{1}{2} L_s \left( i_{sd}^2 \sin^2(\omega t) + i_{sb}^2 \sin^2(\omega t - 120^\circ) + i_{sc}^2 \sin^2(\omega t + 120^\circ) \right) \quad (8)
\]
Therefore, $E_{L_{es}}$ in (7) can be expressed as:

$$
\Delta E_{L_{es}} = E_{L_{s2}} - E_{L_{s1}} = \frac{1}{2} L_s \left( i_{s2}^2 - i_{s1}^2 \right) \sin^2(\omega t - 120^\circ)
$$

In combination with (2) and (9), rewrite (9) to:

$$
\Delta E_{L_{es}} = \frac{2}{9} L_s \left( \frac{P_{es2}^2 - P_{es1}^2}{U_s^2} \right)
$$

Resistance loss power $P_{RDFIG}$ of DFIG rotor windings:

$$
P_{RDFIG} = \frac{3}{2} R_{DFIG}^2 i_{sc_d}^2
$$

The total variation of stored energy in rotor windings of DFIG is $E_{L_{r}}$:

$$
\Delta E_{L_{r}} = E_{L_{r2}} - E_{L_{r1}} = \frac{1}{2} L_r \left( i_{rd2}^2 - i_{rd1}^2 \right)
$$

3) POWER AND ENERGY ANALYSIS OF GSC

The topology of GSC is shown in Fig. 7, and its instantaneous power is shown in (16).

$$
P_{gsc} = \frac{3}{2} u_{gd} i_{gsc_d}
$$

The energy variation of GSC inductance ($E_{L_{g}}$) can be expressed as follows:

$$
\Delta E_{L_{g}} = \frac{1}{2} L_g \left( i_{gsc_d2}^2 - i_{gsc_d1}^2 \right)
$$

The resistance loss power $P_{Rg}$ of GSC input terminal can be expressed as:

$$
P_{Rg} = \frac{3}{2} R_{g} i_{gsc_d}^2
$$

In the above three sections, the power and energy relations of each converter consisting of SCCESS-DFIG are analyzed, and the formulas for calculating power and energy are given. On the basis of the above research, the current loop of the GSC is compensated by feedforward.

B. FEED-FORWARD COMPENSATION CONTROL STRATEGY OF CURRENT LOOP BASED ON POWER BALANCE

When the SCCESS-DFIG rotor side has multiple converters, DC BVF is the smallest, the instantaneous power of GSC is (19), as shown at the bottom of the next page.

In (19), the $K$ coefficient is -1 or 1, which is due to the different instantaneous current directions of SCCESS-DFIG converters. This article defines that current flows from DFIG to power grid as positive and current flows from power grid to DFIG as negative.
to DFIG as negative. Therefore, the relationship between the value of \( K \) and the direction of power flow is arranged into Table 2 (in appendix), and the working conditions I~VI correspond to Fig. 9.

The change of storage energy of DC bus capacitor \( E_{DC} \) can be expressed as:

\[
\Delta E_{DC} = \frac{1}{2} C_{dc} \left( U_{dc2}^2 - U_{dc1}^2 \right) \tag{20}
\]

If the power response speed of GSC approximates the load change speed, the voltage of DC bus capacitor can be stabilized as fast as possible in theory. However, the full energy of the compensation capacitor voltage fluctuation in an ultra-short time (one switching cycle) may cause disturbance to the closed-loop control of the grid-side converter. The compensation can become disturbance, so the compensation needs to be divided into two parts. As shown in (19), the first part of the compensation is the compensation for instantaneous power, which is expressed as follows:

\[
P_{gsc,1}^* = K_{Rg}P_{Rg} + K_{RDC}P_{RDC} + K_{RDFIG}P_{RDFIG} + P_{SD\_rsc} + P_{sc} \tag{21}
\]

The relationship of (22) can be obtained from (20):

\[
\frac{3}{2} u_{gsc}i_{gsc,1}^2 = K_{Rg}P_{Rg} + K_{RDC}P_{RDC} + K_{RDFIG}P_{RDFIG} + P_{SD\_rsc} + P_{sc} \tag{22}
\]

By substituting (11), (13), (17) into (22), the expression of the partial compensation current is obtained in (23), as shown at the bottom of the next page.

The resistance values of GSC filter inductor and DC-DC converter inductor are very small, \( R_{Rg} \) and \( R_{DCI} \) are close to zero, so the two roots in (23) are real roots. One of the roots is nearly infinite, which is not in line with the actual situation. The other root is consistent with the actual situation. This current is the active current amplitude of GSC after the system is stabilized.

The second part of compensation is energy compensation, which is related to the initial and final states of energy storage devices in the GSC response process. Its physical essence is to compensate the energy changes of energy storage components in the response process. The total energy required to compensate \( E_{x,com} \) is shown in (24):

\[
E_{x,com} = \frac{3}{2} K_{Lg} L_g i_{gsc,d2}^2 - i_{gsc,d1}^2)
+ \frac{3}{2} K_{LDFIG} L_{DFIG} (i_{rsc,d2}^2 - i_{rsc,d1}^2)
\]

\[
+ \frac{1}{2} K_{LDC} \sum_{h=1}^{n} \left( L_{DCH2}^2 - L_{DCH1}^2 \right)
+ \frac{1}{2} C_{dc} \left( U_{dc2}^2 - U_{dc1}^2 \right) \tag{24}
\]

Among them, \( i_{gsc,d1} \) and \( i_{gsc,d2} \) are the d-axis currents of the GSC at the start and end of the dynamic response, respectively. \( U_{dc1} \) and \( U_{dc2} \) are the voltages of the supporting capacitors at the beginning and end of the dynamic response, respectively. \( i_{DCH1} \) and \( i_{DCH2} \) are the currents of the DC-DC converter inductance \( L_{DCH} \) at the start and end of the dynamic response, respectively. \( i_{rsc,d1} \) and \( i_{rsc,d2} \) are the d-axis currents of the RSC at the beginning and end of the dynamic response, respectively.

If the energy value calculated in (24) is compensated in a short time, it will cause fluctuations in the stability of the system and even cause the system to collapse. Therefore, the energy can be compensated for in several cycles. Assuming that the number of compensation cycles is \( n \), \( T_{gsc} \) is the power module switching period of the GSC, which can be obtained from the above analysis (25):

\[
nT_{gsc}P_{gsc,2}^* = \frac{3}{2} K_{Lg} L_g \left( i_{gsc,d2}^2 - i_{gsc,d1}^2 \right)
+ \frac{1}{2} C_{dc} \left( U_{dc2}^2 - U_{dc1}^2 \right)
+ \frac{1}{2} K_{LDC} \sum_{h=1}^{n} \left( L_{DCH2}^2 - L_{DCH1}^2 \right)
+ \frac{3}{2} K_{LDFIG} L_{DFIG} \left( i_{rsc,d2}^2 - i_{rsc,d1}^2 \right) \tag{25}
\]

The grid voltage is instantaneous constant, the compensation in the inner current loop can be calculated by (25). Then the total current of feed-forward compensation in power-energy compensation control strategy can be obtained in (26), as shown at the bottom of the next page.

**IV. RESEARCH ON GSC CONTROL STRATEGY BASED ON SCCESS-DFIG FOR MINIMUM VOLTAGE FLUCTUATION OF SUPPORTING CAPACITOR**

**A. DESIGN OF GSC VOLTAGE LOOP BASED ON ADRC**

Because of the topology and operation characteristics of SCCESS-DFIG, the rotor-side multi-converter is a highly nonlinear, time-varying, coupled and uncertain system. Based on the traditional linearized PI controller, it will be difficult to obtain satisfactory control effect. Active disturbance rejection control (ADRC) is a kind of non-linear robust control technology which does not depend on accurate model. It has the advantages of fast tracking speed, small overshoot, high
precision and strong anti-interference ability. Therefore, this article applies ADRC technology to GSC control to reduce DC bus voltage fluctuation caused by unbalanced power on both sides of the supporting capacitor.

When GSC is operating at unit power factor $i_{eg}$ is 0, the third equation in (5) can be written as:

$$\frac{dU_{dc}}{dr} = \frac{1}{2} \left( S_1 t_{gd} - h_{load} \right)$$  \hspace{1cm} (27)

Assuming $S_1 t_{gd} = t_{eg}$, then,

$$\frac{dU_{dc}}{dr} = \frac{1}{2} \left( S_1 t_{gd} - \frac{1}{C} h_{load} \right)$$  \hspace{1cm} (28)

1) DESIGN OF TRACKING DIFFERENTIATOR

According to the experience of [23] in ADRC research, tracking differentiator may cause phase lag. Therefore, the ADRC is applied in the voltage loop of GSC. Because the response speed of outer ring is slower than that of inner ring, it is not sensitive to phase lag. In steady state, the tracking differentiator has no phase delay. It has advantages in tracking dynamic step signals.

$$\begin{aligned} x_1 (k+1) &= x_1 (k) + T \cdot x_2 (k) \\ x_2 (k+1) &= x_2 (k) + T \cdot f_{han} (x_1 (k), x_2 (k), r, h) \end{aligned}$$  \hspace{1cm} (29)

Among them, $T$ is the sampling period, $r$ is the velocity factor, $h$ is the filtering factor, and $f_{han} (x_1 (k), x_2 (k), r, h)$ is the synthesized function of the fastest control. When $h$ is fixed, the tracking speed becomes faster and faster with the increase of velocity factor $r$. However, too large $r$ value will make $x_1 (k)$ have a larger peak. When the $r$ value is fixed, the smaller $h$ will weaken the filtering ability, while the larger $h$ value will slow down the response speed of $x_1 (k)$.

The expression of $f_{han} (x_1 (k), x_2 (k), r, h)$ is (30):

$$\begin{aligned} d &= rh \\ d_0 &= hd \\ y &= x_1 + hx_2 \\ a_0 &= \sqrt{d^2 + 8R \cdot |y|} \\ a &= \begin{cases} x_2 + \frac{a_0 - d}{2} \cdot \text{sign}(y) & |y| > d_0 \\ x_2 + \frac{y}{h}, & |y| \leq d_0 \end{cases} \\ f_{han} &= \begin{cases} r \cdot \text{sign}(a) & |a| > d \\ r \cdot \frac{a}{h}, & |a| \leq d \end{cases} \end{aligned}$$  \hspace{1cm} (30)

where: $d$, $d_0$ control the length of the linear segment of the $f_{han}$; $y$, $a$, $a_0$ are internal variables.

Fig. 13 shows the output contrast of the TD under different parameters $h$. The smaller the sampling step size $T$, the more accurate the simulation, and the closer the tracking signal and the differential signal are to the actual value. However, considering the performance of the controller, the smaller the step-size controller, the greater the computational burden, so it take 0.1ms.

In Fig. 13, when the sampling step size is fixed, the filter factor $h$ is also fixed. If the filter factor is equal to the sampling step size ($h = 0.0001$), there is no filtering effect, and the tracking signal will have an overshoot phenomenon. At the same time, when the input signal is polluted, this overshoot phenomenon will aggravate the noise amplification effect on the differential signal. If the filter factor is too large ($h = 0.01$), the response speed of the tracking signal will be slowed down. In contrast, the filter factor $h$ is usually five to ten times of the sampling step size. When $h = 0.001$, the system has no overshoot and has a fast dynamic response.

As shown in Fig.14(a) and Fig.14(b), when the sampling step length $T$ and the filtering factor $h$ are fixed, as the speed factor $r$ increases (5000 to 500000), the response speed of...
the tracking signal increases. However, an excessive speed factor \( r = 500000 \) will cause the output differential signal to generate excessive spikes, which is not conducive to system control, and the speed increase is not obvious. Compared with the simulation results, \( r = 50000 \) achieves a better compromise effect.

2) DISCRETE LESO DESIGN

Taking the first-order controlled object as an example, the equation of state is as follows:

\[
\begin{align*}
\dot{x}_1 &= f(x_1, w(t), t) + bu \\
y &= x_1
\end{align*}
\]  

(31)

where: \( x \) is the state variable of the controlled object; \( w(t) \) is the unknown external disturbance; \( u \) is the control input; \( b \) is the control input coefficient, the internal disturbance of the system is \( f(x_1, w(t), t) \), and \( y \) is the output.

The extended state can be obtained from (31) as shown in (32), \( x_2 \) is the extended state variable:

\[
\begin{align*}
\dot{x}_1 &= x_2 + bu \\
\dot{x}_2 &= \dot{f}(x_1, w(t), t) \\
y &= x_1
\end{align*}
\]  

(32)

The extended equation of state of (28) can be obtained by (33):

\[
\begin{align*}
\dot{U}_{dc} &= \left(-\frac{i_{load}}{C}\right) + \frac{3}{2C}i_{egd} \\
\dot{x}_2 &= -\left(\frac{i_{load}}{C}\right) \\
y &= U_{dc}
\end{align*}
\]  

(33)

The discrete LESO of the equation of state can be expressed as:

\[
\begin{align*}
e &= z_1 - x_1 \\
z_1 &= z_1 + T(z_2 - \beta_{01}e + bu) \\
z_2 &= z_2 + T(-\beta_{02}e)
\end{align*}
\]  

(34)

where: \( z_1 \) and \( z_2 \) are estimates of \( x_1 \) and \( x_2 \) through ESO, \( T \) is the sampling period, \( \beta_{01}, \beta_{02} \) are the gain coefficients.

LESO can simplify parameter selection into closed-loop poles [23]. When \( \dot{e} = x_i - z_i \), \( i = 1, 2, \) \[
\begin{align*}
\dot{e}_1 &= -\beta_{01}e_1 + e_2 \\
\dot{e}_2 &= -\beta_{02}e_1 + h
\end{align*}
\]  

(35)

When \( \dot{e} = A_e + Eh \), (34) be rewritten as:

\[
A_e = \begin{bmatrix}
-\beta_{01} & 1 \\
-\beta_{02} & 0
\end{bmatrix}
\]  

(36)

Obviously, if LESO is expected to be bounded input bounded output (BIBO) stable, then there are (37):

\[
\lambda(s) = s^2 + \beta_{01}s + \beta_{02}
\]  

(37)

The root of matrix \( A_e \) characteristic polynomial should be in the negative half plane, so when all poles are \( \sim \omega_0 \), \( \beta_{01} = 2\omega_0, \beta_{02} = \omega_0^2 \), where \( \omega_0 = (3 \sim 5)\omega_C \), \( \omega_C \) is determined by the expected transient response speed of the system.

3) DISTURBANCE ESTIMATION COMPENSATION AND LINEAR STATE ERROR FEEDBACK CONTROL LAW

According to the step load and disturbance estimated by LESO, the output control quantity is as follows:

\[
i_{egd}^* = u_0 - \frac{z_2}{b}
\]  

(38)

where \( u_0 \) is designed as follows:

\[
u_0 = k_pe
\]  

(39)
$k_p$ is proportional gain and it can be selected as the desired bandwidth of the speed loop, which is determined on account of the dynamic response requirements.

Ignoring the observational error of the state observer, the controlled system is simplified to a first-order pure integral system.

$$\ddot{y} = (f_0 - z_2) + u_0 \approx u_0$$  \hspace{1cm} (40)

So the closed-loop transfer function is:

$$G_{cl} = \frac{k_p}{s + k_p}$$  \hspace{1cm} (41)

From the form of the closed-loop transfer function, it can be seen that the control method can quickly track the given order without overshoot, and has simple topology and easier parameter adjustment.

**B. CONTROL BLOCK DIAGRAM ANALYSIS OF SCCESS-DFIG SYSTEM BASED ON ADRC AND FEEDFORWARD COMPENSATION CONTROL**

Fig. 15 is a system control block diagram of SCCESS-DFIG topology. The variable marked red in the figure is the fixed parameter or instantaneous variable needed in the improved control strategy of GSC. The known integrally fixed electrical parameters include $L_{DCS}, R_{DCS}, L_{DFIG}, R_{DG}, L_{DG}$ and $R_{BG}$. The control strategy improvement of GSC is divided into voltage loop and current loop. Calculation methods have been described in detail in the section III and section IV.

The input of GSC voltage loop is $u_{dc1}$, the sampling feedback is $u_{dc2}$, and the output variable obtained by LADRC is current $i_{gsc, d}$.

As shown in Fig.15, in the improvement of current loop control of GSC, the added control amount includes power
balance compensation and energy balance compensation. First, according to the operating conditions of the SCESS-DFIG, the power directions of the RSC, GSC, and DC-DC converters are determined. According to the working conditions, the values of $K_{Rg}$, $K_{Lg}$, $K_{RDC}$, $K_{LDC}$, $K_{RDFIG}$ and $K_{LDFIG}$ are obtained. According to the power commands of (11), (15), (18), the compensated current calculated by power balance is obtained. The sign of resistance loss in the figure is negative because the direction of power flow defined in this article is positive from the motor to the grid, so its value is negative.

For the compensation current of energy balance, the operation condition is also determined according to the direction of power flow. The values of $K_{Rg}$, $K_{Lg}$, $K_{RDC}$, $K_{LDC}$, $K_{RDFIG}$ and $K_{LDFIG}$ are obtained. In the process of energy balance compensation, the required parameters mainly include the current setting of each DC-DC converter, and the power setting of RSC and the output of LADRC of GSC.

According to the (24), the variation of energy on the inductive energy storage element from the beginning to the end of the dynamic response is calculated, and the instantaneous compensation power is obtained by dividing the energy by the compensation time. The calculated power is multiplied by $2/3U_{gsc}$ to obtain the converted compensation current $i_{gsc\_com}$, which is used as feed-forward compensation for current loop control of GSC.

V. SIMULATION AND EXPERIMENTAL VERIFICATION

This part is mainly divided into two parts. The first part is the simulation verification of the research content, and the second part is the experimental verification of the research content.

A. SIMULATION OF SUDDEN DISTURBANCE UNDER GRID FREQUENCY STABILITY

Fig.16 is the wind speed curve given to DFIG in the simulation process. Wind speed changes constantly in the simulation process. Fig.17 shows the speed curve of DFIG in the simulation process. Because of the inertia of DFIG blade, the speed change of DFIG is smoother. As shown in the figure, in the process of simulation, the operating condition of DFIG decreases from super synchronous speed to sub-synchronous speed. The parameters of the simulation model are shown in Table 4 and Table 5 in the appendix.

![Figure 16. Simulation wind speed curve.](image)

Fig.18 (a) shows optimal power curve of DFIG through the MPPT. As the speed decreases, the maximum output power curve of the DFIG also shows a downward trend. Fig.18 (b) is the output power curve of DFIG stator side. Combining this with Fig.19, it can be seen that the operation condition of SCESS-DFIG can be divided into two stages in the whole simulation process. In the first stage, the generator is in super synchronous speed, RSC power flows from rotor to DC bus, DC-DC converter absorbs power, GSC is in rectification state, and SCESS-DFIG runs in condition III of Fig. 9. In the second stage, the generator is in sub-synchronous speed, DC-DC
output power and GSC is in inverted state. SCESS-DFIG works in working condition VI of Fig. 9.

Fig. 18(c) shows the instantaneous power curve of the super capacitor. With the change of wind speed and given power instruction, the output power of SCCESS-DFIG system can be adjusted to achieve the target power. Fig. 18(d) shows the output power curve of SCESS-DFIG.

Fig. 19 shows the output power curve of SCESS-DFIG system. As shown in the figure, the wind speed changes, the output power of DFIG changes. But the super capacitor compensation makes the output power of SCESS-DFIG adjustable. It enables SCESS-DFIG to track target power accurately.

Fig. 20 is the feed-forward compensation current curve in the current loop. Fig. 20(a) is the compensating current curve based on power balance calculation. Fig. 20(b) is the compensating current curve based on energy balance calculation. In the initial stage, the DC bus voltage is stabilized by GSC at 2000V. At first second, the output power of SCESS-DFIG increases sharply and the super capacitor releases power. This is equivalent to the decrease of GSC load and the increase of support capacitor voltage. When the output power of SCESS-DFIG drops suddenly at 2.5s, the DC bus voltage of super capacitor will also drop suddenly. By comparing the two sets of waveforms in Fig. 22, it is not difficult to find that the proposed control strategy can stabilize the DC bus voltage better than the traditional control strategy when the power of the GSC changes abruptly.

**B. EXPERIMENTAL VERIFICATION**

As shown in Fig. 23, it is the experimental platform topology used in this article. The experimental platform mainly consists of seven parts: 1. Upper computer control system, which is used to simulate the real wind turbine; 2. Supporting platform of induction motor and doubly fed induction motor; 3. RSC; 4. GSC; 5. DC-DC converter; 6. Super capacitor energy storage device; 7. Supporting platform of synchronous generator. Because of the low moment of inertia of the experimental platform, the upper computer and inverter are used to control the induction motor, through the power closed-loop control its speed simulation moment of inertia. The control chip of RSC, GSC and DC-DC converter is DSP28335 of TI company. The DC-DC converter adopts triple phase shifting control to reduce the current ripple. The super capacitor energy storage system is equipped with a pre charging system. Synchronous generator set to support platform simulation grid. Through the grid connected control of doubly fed induction generator, the whole operation of microgrid system is realized.
Fig. 24 shows the wind speed curve given during the experiment. The wind speed curve is random. Fig. 25 shows the wind turbine speed curve obtained by upper computer simulation during the experiment.

In this process, the total power target of SCESS-DFIG is changed. Super capacitor energy storage device releases the total output of power lifting system. At this time, the lower arm of the super capacitor DC-DC converter is opened and the upper arm is closed. The voltage, current and switch state of super capacitor are shown in Fig. 26.

Fig. 27 shows the stator voltage and current of the synchronous generator and the stator current of SCESS-DFIG. The peak value of synchronous generator stator voltage is...
The power direction of the GSC is positive when the converter flows from the DC bus to the grid, so in the sub synchronous state, the phase difference between the current and the voltage is 180 degrees. By comparing Fig. 28 (a) and Fig. 28 (b), the current compensation control strategy proposed in this article has a fast instantaneous current response.

Fig. 29 shows the DC bus voltage comparison under the two control strategies. When the super capacitor energy storage device releases power, the DC bus voltage increases. The DC bus voltage under the conventional PI control strategy changes from 210V to 243V. After 210ms, the DC bus voltage recovered smoothly. As shown in Fig. 29 (b), the DC bus voltage fluctuates to 232V and the recovery time is about 103ms. No matter from the angle of voltage fluctuation amplitude or the angle of voltage recovery time, the control strategy designed in this article has advantages over the former. It is proved that the control strategy optimizes the control of GSC, reduces the fluctuation amplitude of DC bus voltage and accelerates the speed of voltage recovery.

VI. CONCLUSION

This article analyzes the influence of multi converter on DC bus voltage in the topology of SCESS-DFIG. The research results are summarized as follows:

1. A current feed-forward control strategy based on power balance and energy conservation is proposed for the voltage fluctuation of DC bus caused by instantaneous power imbalance. According to the topology of SCESS-DFIG, the mathematical expression of power compensation current is derived by mathematical model.

2. Through the analysis of energy conservation, the energy changes of inductance and capacitor in the system are calculated, and the energy is compensated by several periods.

3. The voltage loop control strategy of GSC is designed by using ADRC, which optimizes the nonlinear performance of GSC to DC load.

4. The overall control strategy of SCESS-DFIG is designed, and the simulation model and experimental platform are built. The simulation and experimental results show that the control strategy designed in this article can reduce the fluctuation amplitude of DC bus voltage and accelerate the speed of voltage recovery.

APPENDIX

Among them:

- $P_{\text{mech}}$ is the capture power of the fan,
- $\lambda$ is the tip speed ratio,
- $R$ is the blade radius,
- $V_w$ is the wind speed,
- $C_p$ is the utilization ratio of wind energy,
- $\omega_m$ is the angular velocity of the blade,
- $\beta_f$ is the pitch angle, $\lambda_{\text{opt}}$ is the optimal tip speed ratio,
- $N$ is the speed ratio, $\rho$ is the air density,
- $s$ is the slip rate,
- $\omega_m$ is the mechanical angular velocity of the rotor,
- $P_F^*$ is the per-unit value of inertia response power,
### TABLE 2. The relationship between k and the power flow direction of SCESS-DFIG.

| Condition             | Power direction                  | K                        |
|-----------------------|----------------------------------|--------------------------|
| Condition 1           | $P_{sccs rsc}<0$, $P_{sec}<0$, $P_{gscc gsc}<0$ | $K_{dc1}=1$, $K_{dc2}=1$, $K_{dc3}=1$, $K_{dc4}=1$, $K_{dc5}=1$, $K_{dc6}=1$ |
| Condition 2           | $P_{sccs rsc}=0$, $P_{sec}<0$, $P_{gscc gsc}<0$ | $K_{dc1}=1$, $K_{dc2}=1$, $K_{dc3}=1$, $K_{dc4}=1$, $K_{dc5}=1$, $K_{dc6}=1$ |
| Condition 3           | $P_{sccs rsc}=0$, $P_{sec}<0$, $P_{gscc gsc}=0$ | $K_{dc1}=1$, $K_{dc2}=1$, $K_{dc3}=1$, $K_{dc4}=1$, $K_{dc5}=1$, $K_{dc6}=1$ |
| Condition 4           | $P_{sccs rsc}=0$, $P_{sec}<0$, $P_{gscc gsc}=0$ | $K_{dc1}=1$, $K_{dc2}=1$, $K_{dc3}=1$, $K_{dc4}=1$, $K_{dc5}=1$, $K_{dc6}=1$ |
| Condition 5           | $P_{sccs rsc}<0$, $P_{sec}<0$, $P_{gscc gsc}<0$ | $K_{dc1}=1$, $K_{dc2}=1$, $K_{dc3}=1$, $K_{dc4}=1$, $K_{dc5}=1$, $K_{dc6}=1$ |
| Condition 6           | $P_{sccs rsc}<0$, $P_{sec}<0$, $P_{gscc gsc}<0$ | $K_{dc1}=1$, $K_{dc2}=1$, $K_{dc3}=1$, $K_{dc4}=1$, $K_{dc5}=1$, $K_{dc6}=1$ |

### TABLE 3. Parameters of the DFIG model in the simulation.

| Parameter          | Value     | Parameter          | Value     |
|--------------------|-----------|--------------------|-----------|
| Rated power        | 2.5MW     | Number of pole-pairs $p$ | 2         |
| Stator voltage     | 690V      | Moment of inertia $J$ | 5.0x10³ kg m² |
| Rated speed        | 1500rpm   | Speed change       | ±50%      |
| Rated frequency    | 50Hz      | $U_b$              | 2000V     |
| $R_s$              | 3.0ΩmH    | $L_d$              | 0.03mH    |
| $L_m$              | 0.053mH   | $L_s$              | 5.892mH   |
| $R_t$              | 2.3ΩmH    | $C$                | 500μF     |
| $L_{in}$           | 0.19mH    |                    |           |

### TABLE 4. Parameters of the DC-DC converter model in the simulation.

| Parameter          | Value     | Parameter          | Value     |
|--------------------|-----------|--------------------|-----------|
| DC bus voltage     | 2000V     | Super Capacitor voltage | 800V   |
| $L_1$              | 5mH       | $K_{dc1}$          | 5.35mH    |
| $L_2$              | 5.58mH    | $K_{dc2}$          | 10.4      |
| $K_{dc1}$          | 5.05      | $K_{dc3}$          | 10.2      |
| $K_{dc2}$          | 5.02      | $K_{dc4}$          | 10        |
| $K_{dc3}$          | 5         | $K_{dc5}$          | 9.7       |
| $K_{dc4}$          | 5.1       | $K_{dc6}$          | 9.85      |
| $K_{dc5}$          | 5.25      | $K_{dc7}$          | 10        |
| $K_{dc6}$          | 5.38      | Switching frequency | 6kHz      |

$H$ is the time constant of inertia response, $f$ is the grid frequency, $f_N$ is the rated frequency of power grid, $u_{gsc\_d}$, $u_{gsc\_q}$ are three-phase grid voltages, $u_{gsc\_a}$, $u_{gsc\_b}$ and $u_{gsc\_c}$ are three-phase voltages on the AC bridge arm side of the converter. $i_{gd}$, $i_{gq}$ are $d$ and $q$ axis components of input current, $u_{gsc\_d}$, $u_{gsc\_q}$ are $d$ and $q$ axis components of output voltage of AC bridge arm of converter, $S_d$ and $S_q$ are the switching function of $d$ and $q$ axis components, $\omega_1$ is angular velocity of grid voltage, $P_{SD\_es}$ is the stator side power of the DFIG, $P_{SD\_RSC}$ is the power of RSC.

### TABLE 5. Parameters of doubly-fed wind turbine in experimental platform.

| Parameter          | Value     | Parameter          | Value     |
|--------------------|-----------|--------------------|-----------|
| Rated power        | 1.562kW   | Number of pole-pairs $p$ | 3         |
| Rated speed        | 1000rpm   | Shrinkage ratio coefficient $\Delta$ | 40        |
| Rated frequency    | 50Hz      | Speed change       | ±30%      |
| The length of the blade | 1.878m | $L_{blade}$ | 1.95kg m² |
| $R_{pa}$           | 0.06      | $U_{DC}$           | 200V      |
| $L_{pa}$           | 0.08      | $L_{in}$           | 3.52      |
| $R_{pa}$           | 0.046     | $C$                | 5000μF    |
| $L_{in}$           | 0.046     | $H_{DC}$           | 10s       |

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