Power Relay Based Multiple Device Cryogenic Characterization Method and Results

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ABSTRACT Cryogenic power electronics is a promising technology due to their high efficiency and high power density characteristics. As the key element of power electronic systems, semiconductor performance should be evaluated under cryogenic temperatures. Liquid nitrogen or liquid helium are usually adopted to achieve cryogenic temperatures. Traditionally, only one semiconductor can be evaluated at one time under different temperatures, which is time-consuming and not energy-friendly. To enable multiple-device characterization at one time under different temperatures, a novel power relay based characterization circuit and corresponding control strategy are described. With the aid of the proposed circuit, multiple devices can be characterized by controlling the power relays. The introduced parasitics by the power relays are minimized through paralleling, which has negligible influence on the device under test (DUT). Cryogenic characterization results of the gate driver, power relay, and semiconductors are presented. Both silicon (Si) metal–oxide–semiconductor field-effect transistor (MOSFET) and silicon carbide (SiC) MOSFETs are characterized and their performances are discussed.

INDEX TERMS Cryogenic power electronics, multiple device characterization, power relay, Si MOSFET, SiC MOSFET.

I. INTRODUCTION

There are primarily two motivations for the application of cryogenic power electronics [2]. First, for some applications, the superconducting cables, motors, and generators are operating in a cryogenic environment, while a heater is used to keep the electronics warm, which increases the system cost, weight, and volume. A straightforward approach to overcome these issues is operating electronic circuits under the same cryogenic temperatures as the other elements. Second, it has been reported that some semiconductors have improved performance under cryogenic temperatures when compared with room temperature operation. Cryogenic power electronics is an emerging technology for high-efficient all electric aircraft [2],[3].

Research into cryogenic power electronics have been mainly conducted from the following perspectives: 1) component performance evaluations [2]–[12]; and 2) converter or system level design and evaluation [13]–[15]. In [2], the authors reviewed the applications of cryogenic power electronics and some key component performances. In [3], an overall review regarding the performances of key components under cryogenic temperatures in power electronic systems was presented. The characterization results demonstrate that different semiconductors have different performances.

Generally, silicon (Si) and gallium nitride (GaN) devices have reduced on-state resistance under low temperatures and improved switching speed, which are suitable for cryogenic applications. On the other hand, the silicon carbide (SiC) semiconductors have increased on-state resistance and reduced switching speed under cryogenic temperatures, which make them less attractive for these applications.
Traditionally, the double pulse test (DPT), or clamped inductive load (CIL) test, is performed to evaluate semiconductor device dynamic performance. The typical circuit for DPT/CIL is shown in Fig. 1(a). Fig. 1(b) shows the typical waveform for the DPT test.

Semiconductor is the key element for power electronics system. To investigate cryogenic power electronics, cryogenic characterizations of massive semiconductors are required. For cryogenic semiconductors characterizations, the cryogenic chamber and liquid nitrogen/liquid helium are normally adopted. Typically, only one DPT board with one device under test (DUT) can be characterized at one time due to the limited space of cryogenic chamber and the electromagnetic interference issues. To evaluate another device, the cryogenic chamber needs to be heated up to room temperature first, and then replace the DUT and cool down the cryogenic chamber to initiate another test, which takes more than half hour to setup and achieve cryogenic temperature again. Clearly, the traditional test method is both time-consuming and not energy-friendly since more liquid nitrogen/liquid helium are consumed. Therefore, the main purpose of this paper is to propose a power relay based test method to characterize multiple devices at the same time so that there is no necessary to start again the process in order to test other devices.

Please note that placing multiple DPT boards with different DUTs is impractical due to the following reasons: 1) the space of the cryogenic chamber is limited; 2) multiple sets of equipment are required, including load inductors, DC power supply, auxiliary power supply, voltage and current probes; 3) to avoid leakage of liquid nitrogen/liquid helium, only a small hole exists for the cryogenic chamber to achieve connections from oscilloscope, DC power supply, auxiliary power supply, and pulse generation equipment. If multiple setups are used, which makes the layout of the cables complicate and even unable to place the required number of cables due to the interference issues. Moreover, the electromagnetic interference (EMI) would also be degraded due to the crowded placement of the cables. Thanks to the proposed power relay based multiple device characterization method, the above-mentioned issues can be effectively resolved by using only one DPT board. The main contributions of this paper lie into the following aspects: 1) a novel power relay based multiple device characterization method is proposed for cryogenic applications; 2) cryogenic characterizations of power relay, gate driver, and semiconductors, including Si MOSFET and SiC MOSFETs are presented.

To enable multiple device characterization capability, a novel power relay based characterization circuit is proposed. Different devices under test can be selected by controlling the power relays. A control method is proposed to ensure that the power relays are switched at zero current so that it can block the high DC voltage, which is different from the normal operation of power relay. To minimize the introduced circuit parasitics, paralleling operations of power relays are adopted to reduce the parasitic inductance and increase the current capability. Performance evaluations of the gate driver, power relay, and semiconductors are presented.

II. OPERATIONAL PRINCIPLES OF THE PROPOSED POWER RELAY BASED MULTIPLE DEVICE CHARACTERIZATION CIRCUIT

Fig. 2(a) shows the proposed power relay based characterization circuit and Fig. 2(b) shows the corresponding control strategy. Please note that if no relays are adopted, when one DUT is characterized, the output capacitance of another DUT will affect the operation of the evaluated DUT. There are four important stages to consider. For simplicity, only two devices
are described, but the concept is extensible to multiple devices in parallel. From \( t_0 \) to \( t_1 \), one of the power relays is ON, while all others are OFF. Since the semiconductor device switches much faster (several ns) than the power relay (several ms), a certain amount of time \((t_1-t_0)\) is required before performing characterizations. From \( t_1 \) to \( t_2 \), a traditional double pulse test is performed for DUT1. From \( t_2 \) to \( t_3 \), the load inductor current decreases to zero through the freewheeling diode. The most important timing for the control strategy is \( t_3 \) since the power relay blocking voltage is reduced significantly if there is current flowing through it. Take the power relay (ALQ3F18 from Panasonic) adopted in this article for an example, the maximum switching capacity is only 30 V DC with a switching current of 5 A. Therefore, innovatively, to maximize the blocking voltage capability of the power relay, the power relay is switched at zero current, which is different from the traditional application of power relays, where the power relays are required to switch at a specific current and voltage. When switching at zero current, the maximum blocking voltage capability is determined by the airgap between two contacts and the media between the contacts, which can be increased significantly. Moreover, to leave some safety margin, the relay transition occurs at \( t_4 \). Then, the same process of DUT1 is applied for DUT2.

By adopting the proposed power relay based characterization circuit and control strategy, multiple devices can be evaluated at the same temperature values. Otherwise, the cryogenic chamber is required to heat up first and replace the DUT, and cool down the environment temperature again to perform characterizations for another DUT. The significant improvements of the proposed method including: 1) test time is reduced significantly since multiple devices can be characterized at the same time; 2) liquid nitrogen/liquid helium can be saved significantly since it is unnecessary to heat up cryogenic chamber and re-cool down the chamber to perform other tests.

The airgap for the power relay is approximately 0.5 mm. The voltage blocking capability can be estimated based on the following equation, where \( k \) is the dielectric strength of the insulation material, conventionally, air is the insulation material with a dielectric strength of 3 kV/mm, and \( t \) is the thickness of the insulation material. From (1), the estimated blocking voltage is around 1.5 kV, which satisfies the requirement for many applications (the typical DC bus voltage for 1.7 kV device is 1 kV). Fig. 3 shows the simplified electric field simulation result for the power relay with ANSYS MAXWELL 3D, 1 kV voltage difference is applied to the two contacts. The results demonstrate that the maximum electric field is around 2 kV/mm, which is lower than the breakdown strength of air (3 kV/mm). In addition, the simulated parasitic capacitance between two contacts is only around 464 fF, which has negligible influence to the circuit.

\[
V_{\text{breakdown}} = k \times t \tag{1}
\]

However, the voltage blocking capability actually determines by the test conditions. If the test is conducted in non-vacuum condition, the icing and other gases will degrade the power relay voltage blocking capability. If the test is conducted in vacuum condition, the voltage blocking capability can be improved. Therefore, the selection of power relays should be based on the test condition and the required voltage blocking capability. By using the cryogenic chamber, a near vacuum condition can be created and no icing is observed during the test.

The parasitic capacitance for the power relay in open circuit condition can be estimated by using the model of two parallel metal plates.

\[
C = \frac{k \varepsilon_0 A}{d} \tag{2}
\]

where \( k \) is the relative permittivity of the dielectric material between the plates. In this case, the medium is air so that \( k \approx 1 \) can be obtained. \( \varepsilon_0 \) is the permittivity of free space, \( \varepsilon_0 = 8.854 \times 10^{-12} \text{F/m} \). \( d \) is the distance between two contacts, and \( A \) is the overlap area between two contacts.

By substitution \( d = 0.5 \text{ mm} \) and \( A = (5 \text{ mm})^2 \) into (2), the estimated parasitic capacitance is only 442 fF, which is negligible. Since the power relay is in series with the DUT, the total parasitic capacitance can be further reduced, which has negligible influence on any other DUTs. To validate the theoretical analysis, the parasitic capacitance of power relay in open circuit is measured by impedance analyzer. The E4990A impedance analyzer with a frequency range of 20 Hz to 30 MHz, industry best 0.045% (typical) basic accuracy over wide impedance range, with 40 V built-in DC bias source, for component, semiconductor and materials measurement [16]. It can provide high accuracy measurement for very low parasitics. Fig. 4 illustrates the measurement result. Clearly, the introduced parasitic capacitance is only around 600 fF.
Another important parasitic introduced by the power relay is the inductance. The following two steps are taken to minimize the introduced parasitic inductance: 1) a small-sized or low-current power relay is used so that the parasitic inductance is small; 2) several power relays are connected in parallel to reduce the parasitic inductance. In this work, three 10 A relays are used in each branch to achieve a parasitic inductance less than 3 nH. Fig. 5 shows the parasitic inductance measurement result for a single power relay. It can be seen that the parasitic inductance for a single power relay is around 10 nH, by paralleling three power relays, a total parasitic inductance around 3.3 nH can be achieved. Meanwhile, the parasitic capacitance caused by the paralleling operation of three power relays is around 100 pF. For the branch in open circuit condition, the parasitic capacitance of power relays and the parasitic capacitance of semiconductors (greater than 100 pF) are in series connection, and the total equivalent parasitic capacitance on the branch in open circuit condition is slightly less than 1.8 pF.

Moreover, to further demonstrate the influence of the introduced parasitic capacitance and inductance on the DUT, simulation results comparisons between the traditional DPT and the power relay based DPT are made and the results are shown in Fig. 6. As can be seen from the comparison results, only a slight influence is observed due to the parasitics caused by power relays. Thus, it is effective to use power relay to achieve multiple device characterizations. Please note the simulation is performed at room temperature instead of cryogenic temperature since the SPICE model from the manufacturer is not developed for cryogenic applications. The main purpose of the simulation is to demonstrate the influences of introduced parasitics on the performances of semiconductors.

III. COMPARISONS BETWEEN THE PROPOSED POWER RELAY BASED METHOD AND TRADITIONAL METHOD

A. COST COMPARISONS

To demonstrate the advantages of the proposed power relay based multiple device characterization circuit, cost
comparisons between the proposed method and traditional DPT are made and the results are summarized in Table 1. There are two major reasons for the selection of device current measurement method: 1) cryogenic temperature operation: the current shunt can operate properly under cryogenic temperature since it is a high-accurate resistor, while other current measurement equipment cannot work properly due to the additional circuitries inside the equipment; 2) signal bandwidth requirement: to achieve accurate measurement results, a high bandwidth is required for the current measurement equipment due to the fast switching speed of semiconductors. Compared with all other current measurement equipment, the current shunt has the highest bandwidth performance, which is sufficient for semiconductor characterization application. Take the selected current shunt SSDN-015 in this paper for an example, the bandwidth is up to 1200 MHz.

Please note that two DPTs are required for the traditional method, the unit cost from Digikey is used for comparison. Clearly, with the proposed power relay based characterization method, the system cost can be reduced almost by half. Please note that two current shunts are required for traditional test method, while for the proposed method, two device currents can be measured with the same current shunt as shown in Fig. 2(a). Moreover, the additional cost introduced by the power relay is only 18.77 $. Therefore, the proposed power relay based characterization method is also cost-friendly when compared with traditional method.

### B. SIZE COMPARISONS

The proposed power relay based DPT board and the size dimensions are shown in Fig. 7(a), and the traditional single DPT board and size dimensions are shown in Fig. 7(b). Clearly, due to the power relays, the size for the proposed power relay based DPT board is increased. However, in order to test multiple devices, two single DPT boards are required and the size for the traditional method, which gives a size dimension around 230 mm × 81 mm or 115 mm × 162 mm if two DPT boards are closed placed. Thus, the proposed method can even achieve a size reduction around 35%, which is critical for the cryogenic chamber since the space is limited.

### C. MEASUREMENT EQUIPMENT COMPARISONS

For the traditional DPT board, three signals, gate voltage, device voltage, and device current, are required. Thus, the total required signals are six in order to test two DPT boards. On the contrary, as shown in Fig. 2(a), four signals, two gate voltages, device voltage, and device current, are required. A four-channel oscilloscope can be used for the proposed method, while either six-channel oscilloscope or two four-channel oscilloscopes are required.

Please note that although the control signals for power relays are critical, the purpose of the proposed test method is to achieve cryogenic characterizations of semiconductors. The gate voltage, device voltage and device current are enough for the characterizations of semiconductors. Therefore, the control signals for power relays are unnecessary and not required for the characterizations.

### D. LAYOUT COMPARISONS

For the connections from outside to inside of the chamber, a small hole on side of chamber is used. In order to avoid leakage of liquid nitrogen, the size of the hole is limited. Fig. 8 shows a picture of the cryogenic chamber in this work and the cryogenic chamber in [6]. Clearly, the size of the hole is limited, while there are various connections from outside to
Inside, which including the pulse signal, auxiliary power supply for gate driver, DC high voltage power supply to the bus capacitor, and measurement probes. To avoid electromagnetic interference (EMI) issues, the placement of these connections should be designed carefully so that the signals will not be affected. If two DPT boards are placed inside of the chamber, the placement of these connections would be difficult and even impossible since more connections and measurement probes are required. Therefore, the proposed power relay based characterization method can help mitigate the stress on the layout.

Instead of using two separate DPTs, a modified DPT circuit by sharing the bus capacitor and current shunt as shown in Fig. 9 can be used. Compared with this test method, the proposed method has the following advantages and is preferred for cryogenic characterization: 1) less signals are required. For the proposed test method, the device voltages for different DUTs are measured with one voltage probe at the same position. While for this test method, separate device voltage measurement is required for all DUTs. An oscilloscope with more channels and voltage probes are required, especially when the number of DUTs is large; 2) The semiconductor cryogenic characterizations are normally conducted inside the cryogenic chamber, which has very limited space for inside and outside connections. Since the load inductor is placed outside, it requires connections from outside to inside, this test method requires additional two cables for the load inductor connection. Thus, compared with this method, the proposed test method reduces the number of connections.

Generally, although the proposed method introduced some parasitics to the circuit, it still has the following advantages when compared with two traditional DPT boards: 1) cost reduction; 2) size reduction; 3) reduction of measurement signals; 4) easy layout. When compared with single DPT board, it enables multiple device characterization capability, which is time-consuming and energy-friendly. Meanwhile, the introduced parasitics are minimized.

IV. RESULTS AND DISCUSSIONS

In this section, the performance evaluations for the power relay, gate driver, and semiconductor devices are described.

A. POWER RELAY

To evaluate the performance of a power relay under cryogenic temperatures, the test setup shown in Fig. 10 is used. Please note that the highlighted area is the space for cryogenic chamber. The power relay from Panasonic (ALQ3F18) is controlled by a DC voltage supply that is located outside of the cryogenic chamber. The power relay and a load resistor are placed inside the chamber. By measuring the voltage across the load resistor $V_R$, both the actuation voltage and release voltage of the power relay can be investigated over temperature through the regulation of a control voltage $V_{\text{control}}$. $V_R$ equals the input voltage $V_i$ when power relay is ON, while $V_R$ is zero when the power relay is OFF. Fig. 11 shows the power relay performance over temperature. The power relay operates properly down to $-180^\circ\text{C}$, so that it can be applied in cryogenic applications to achieve multiple device characterization.
characterization. Both actuation and release voltages increase initially with the decrease of temperature. When the temperature is below −50°C, both actuation and release voltages decrease with the decrease in temperature. These changes are caused by the change of copper wire resistance under different temperature. The variations of actuation and release voltages do not affect the operation of the power relay since the relay driver provides a sufficiently wide drive voltage of 15 V and 0 V for turn on and turn off, respectively.

B. GATE DRIVER

In this work, the gate driver from Silicon Lab (Si8271) is selected, which can provide a peak current of 4 A and 200 kV/µs common-mode transient immunity [23]. A power supply from Murata (MGJ2D052005SC) with a 5 V input and 20 V and −5 V outputs is selected, which can be used for most Si MOSFET and SiC MOSFET applications. Fig. 12 shows the output of the gate driver at different temperatures. It can be seen that the gate driver works properly when the temperature is above −130°C. The faulty component is the gate driver chip Si8271, which does not operate properly when temperature is below −130°C. This conclusion is obtained by performing an additional test, where the auxiliary gate driver power supply is placed outside of the chamber so that it can work properly.
Under this test, we found out the output of the gate driver chip becomes abnormal when temperature is below \(-130^\circ \text{C}\) as shown in Fig. 12(c). Thus, the dynamic characterizations are only performed down to \(-130^\circ \text{C}\) in this paper. Although the dynamic test has been performed to around \(-180^\circ \text{C}\) in the literatures for Si IGBT [7], [24], SiC MOSFET [7], and GaN HEMT [8], the adopted gate drivers are not reported [7]. In [17], although the gate driver was located inside the chamber, the gate driver is not directly in contact with the cold head, thus, the temperature of the gate driver is only around 200 K. In [8], the gate driver from Texas Instrument LM5113 is adopted, but this gate driver can only work for 100 V GaN devices, which cannot be applied for other applications. Meanwhile, gate driver Si8271 has been used in the literatures and the same conclusion can be obtained [6]. In a nutshell, it is challenging to find a combination of gate driver power supply, gate driver chip, and signal isolator that operating properly under cryogenic temperature. Our group is currently investigating on the designing and testing of the cryo-friendly gate driver power supply.

**C. CAPACITOR**

Aluminum electrolytic capacitor and film capacitor are normally used to serve as the bus capacitor in the DPT circuit [25]. However, the aluminum electrolytic capacitor has degraded performance under low temperatures, where the capacitance reduces significantly, and the dissipation factor increases sharply [2]. Thus, the film capacitor with polypropene is used as the bus capacitor.

**D. SEMICONDUCTORS**

In this research, a Si MOSFET IXFH26N50P (500 V/26 A) from IXYS and a SiC MOSFET SCT3120AL (650 V/21 A) from ROHM are selected. The B1505 curve tracer from Keysight is used to perform the static characterization. The test setup is shown in Fig. 13, where the liquid nitrogen is used to achieve cryogenic temperature. As discussed in [6], to mitigate the measurement errors caused by the long connection cables from the test fixture to the cryogenic chamber, the Kelvin connection as illustrated in Fig. 13(b) is adopted. Another advantage of the designed PCB board is that it can enable multiple device characterizations by simply modifying the connections on the front panel, which saves great amount of time and energy.

Fig. 14 shows the on-state resistance performance of the two devices, and the data at a drain current of 10 A are selected. For the Si MOSFET, the on-state resistance decreases significantly with the decrease of temperature due to the...
increased carrier mobility [2]. The resistance at $-178^\circ$C (36.8 m$\Omega$) is about five times lower than that of room temperature (212 m$\Omega$). On the contrary, the on-state resistance for the SiC MOSFET increases significantly with the decrease of temperature. It was explained in [5] that there are two parts that contribute to the on-state resistance: 1) channel resistance; and 2) residual resistance. Although the residual resistance decreases with the decrease of temperature like a Si MOSFET due to the increased carrier mobility, the channel resistance has a negative temperature coefficient and dominates the device on-state resistance at low temperatures.

Fig. 15 shows the threshold voltage performance of the two devices over temperature. The threshold voltage for both devices increase with the decreasing temperature. The bulk potential for the nMOS can be expressed as (3). With decreasing temperature, the intrinsic carrier concentration ($n_i$) decreases, and the bulk potential increases. The threshold voltage directly proportional to the bulk potential. Thus, the device threshold voltage increases with the decrease of temperature.

$$\phi_B = \frac{kT}{q} \ln \left( \frac{N_A}{n_i} \right)$$  

E. OTHERS

A SiC Schottky diode is used as the freewheeling diode, which itself has an increasing on-state resistance similar to the SiC MOSFET [2]. The relay driver (ULN2803A from Texas Instruments) and the load inductor are placed outside of the chamber. The selected relay driver have eight outputs, which is sufficient for this application. It is noteworthy to mention that the magnetic core based load inductor is not suitable for cryogenic characterizations since the magnetic material characteristic varies significantly at low temperatures.
F. CIRCUIT IMPLEMENTATION AND RESULTS DISCUSSIONS

Fig. 16 shows the system setup and designed multiple device characterization board. The signals of interest are demonstrated in Fig. 2(a), which are device current (measured by a current shunt with part number SSDN-015 from T&M research produces and 1200 MHz bandwidth), gate voltages (measured by passive voltage probes P2220 from Tektronix with 200 MHz bandwidth), and drain-to-source voltage (measured by passive voltage probe P5120 from Tektronix with 200 MHz bandwidth). To reduce the parasitics introduced by measurements, BNC tip adaptors are used. Since two devices are in parallel operation, the drain-to-source voltage is measured at the same point, which includes the voltage across the power relays. Based on the available channels of the oscilloscope, the load inductor current and separate drain-to-source voltages can be measured.

Fig. 17 shows the turn-on and turn-off comparisons for the Si MOSFET at room temperature and $-130 \degree C$ with a bus voltage of 300 V and load current of 20 A. Both the turn-off and turn-on switching performances are increased at low temperature when compared with room temperature. The significant improvement during turn-off process is observed as shown in Fig. 17(b), the turn-off switching speed is improved by 26 ns and the turn-off $dv/dt$ is increased from 5.79 V/ns at room temperature to 11.77 V/ns at $-130 \degree C$. Fig. 18 shows the experimental results for 650 V SiC MOSFET. It can be seen that there is no obvious change in the switching speed during the switching processes.

The explanations for the dynamic switching performance for Si and SiC MOSFET can be summarized as follows: 1) the dynamic switching performance of a MOSFET is determined by three factors: threshold voltage ($V_{th}$), inversion carrier mobility ($\mu_{ni}$), and gate drain capacitance ($C_{gd}$) [26]; 2) the device threshold voltage is increased for both the evaluated Si MOSFET and SiC MOSFET, which slows down the turn-on switching speed, but improves the turn-off switching speed; 2) for the SiC MOSFET, the inversion carrier mobility decreases with the decrease of temperature, which makes it difficult to form (or eliminate) the current, thus increasing both the turn-on and turn-off switching times [26]. While for Si MOSFET, the inversion carrier mobility is improved under low temperatures [24], which improves its turn-on and turn-off switching performances; 3) the gate drain capacitance is decreased due to the reduction of ionized doping concentration, which improves the switching performance [28]. However, dopant ionization would be low in the absence of field at low temperature. When combined with sufficient electric field, the temperature dependence of ionization would be very weak. As reported in [24], the gate drain capacitance is very slightly reduced at cryogenic temperature.

Thus, the turn-on switching performance for Si MOSFET is less affected by the increase of threshold voltage as shown in Fig. 17(a) due to the increase of inversion carrier mobility and slight reduction of gate drain capacitance, while the turn-off switching performance is improved significantly since all three factors lead to fast turn-off switching speed. On the other hand, for the evaluated 650 V SiC MOSFET, both the turn-on process and turn-off process remain almost unchanged. Although the turn-on speed is improved initially as shown in Fig. 18(b), it actually takes longer time at low
temperature to achieve fully turn-on (zero voltage) when compared with room temperature. For the turn-off switching process, although the threshold voltage is increased, the reduction of inversion carrier mobility slows down the turn-off switching process. Therefore, the overall switching performance for the evaluated 650 V SiC MOSFET is stable.

Tables 2 and 3 summarize the turn-on time, turn-off time, turn-on loss, and turn-off loss for the two devices over the tested temperature range. Please note that the turn-on switching loss is calculated when the device voltage drops to 5% of the bus voltage. As shown in Fig. 18(b), if a lower voltage is selected, the turn-on switching loss at low temperature will increase since it takes longer to reach the fully turn-on device voltage. The following conclusions can be drawn for these two devices: 1) the rising time reduces slightly for the Si MOSFET over temperature, while the turn-off speed/falling time is improved significantly. Around 44% falling time reduction is achieved; 2) for the SiC MOSFET, both turn-on speed and turn-off speed remain largely unchanged over temperature; 3) both the turn-on and turn-off switching losses for the Si MOSFET reduces at low temperature operations. More than 65% turn-off switching loss reduction is achieved.

In addition to the 650 V SiC MOSFET, we also investigated two 1200 V SiC MOSFETs (1.2 kV 20 A SiC MOSFET MSA12N080A from Monolith and 1.2 kV 40 A SiC MOSFET SCH2080KE from Rohm) with the proposed multiple device characterization circuit. Fig. 19 shows the dynamic switching performances comparisons at room temperature and $-130^\circ$C. Compared with the turn-on experimental waveform of 650 V SiC MOSFET (Fig. 18(b)), the turn-on switching speed of 1200 V SiC MOSFETs at $-130^\circ$C is decreased significantly. A “long tail turn-on voltage” is observed during the turn-on process, which increases the turn-on switching loss significantly. The “long tail turn-on voltage” for 1200 V SiC MOSFETs might be caused by the differences between device structures.

Fig. 20 and Fig. 21 show the turn-on and turn-off switching losses comparisons under different testing conditions. Based on the characterization results, the following conclusions can be drawn: 1) conventional Si MOSFET is
advantageous at cryogenic temperature, both the conduction loss and switching loss can be reduced at low temperatures; 2) low voltage SiC MOSFET has stable switching performance at low temperatures; 3) high voltage SiC MOSFET has degraded switching performance at low temperatures, which increases the switching loss significantly. Generally, Si MOSFET is advantageous for cryogenic applications, while SiC MOSFET is not preferred.

V. CONCLUSION

There are three main contributions of this paper. First, a novel power relay based multiple device characterization circuit and corresponding control strategy are proposed for cryogenic applications. With the aid of the proposed circuit, multiple devices can be characterized at the same time, which can save both time and energy. Meanwhile, the introduced parasitics are minimized by paralleling relays. Second, components and system cryogenic characterization methods are introduced that can serve as guidelines. Third, power electronic component performances are evaluated under cryogenic temperatures, especially the semiconductors, the Si MOSFET, 650 V SiC MOSFET, and 1200 V SiC MOSFETs are characterized. In the future, more components and devices will be evaluated, especially the gate driver, which is critical for cryogenic circuit operation.

REFERENCES

[1] Y. Wei, M. M. Hossain, and H. Alan Mantooth, “Power relays based novel circuit with multiple device characterization capability for cryogenic applications,” in Proc. IEEE Trans. Electrific. Conf. Expo. 2022, pp. 137–142.

[2] H. Gui et al., “Review of power electronics components at cryogenic temperatures,” IEEE Trans. Power Electron., vol. 35, no. 5, pp. 5144–5156, May 2020.

[3] K. Rajashekara and B. Akin, “Cryogenic power conversion systems: The next step in the evolution of power electronics technology,” IEEE Electrific. Mag., vol. 1, no. 2, pp. 64–73, Dec. 2013.

[4] H. Mhiesan, M. M. Hossain, A. U. Rashid, Y. Wei, and A. Mantooth, “Survey of cryogenic power electronic systems for hybrid electric aircraft applications,” in Proc. IEEE Aerosp. Conf., 2020, pp. 1–7.

[5] S. Chen, C. Cai, T. Wang, Q. Guo, and K. Sheng, “Cryogenic and high temperature performance of 4H-SiC power MOSFETs,” in Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo., 2013, pp. 207–210.

[6] Z. Zhang et al., “Characterization of wide bandgap semiconductor devices for cryogenically-cooled power electronics in aircraft applications,” in Proc. AIAA/IEEE Electric Airr. Technol. Symp., 2018, pp. 1–8.

[7] J. Qi et al., “Dynamic performance of 4H-SiC power MOSFETs and Si IGBTs over wide temperature range,” in Proc. IEEE Appl. Power Electron. Conf. Expo., 2018, pp. 2712–2716.

[8] J. Colmenares, T. Foulkes, C. Barth, T. Modeert, and R. C. N. Pilawa-Podgurski, “Experimental characterization of enhancement mode gallium-nitride power field-effect transistors at cryogenic temperatures,” in Proc. IEEE 4th Workshop Wide Bandgap Power Devices Appl., 2016, pp. 129–134.

[9] Min Chen et al., “The magnetic properties of the ferromagnetic materials used for HTS transformers at 77 K,” IEEE Trans. Appl. Supercond., vol. 13, no. 2, pp. 2313–2316, Jun. 2003.

[10] S. S. Gerber, “Performance of high-frequency high-flux magnetic cores at cryogenic temperatures,” in Proc. 37th Intersociety Energy Convex, Eng. Conf., 2002, pp. 249–254.

[11] M.-J. Pan, “Performance of capacitors under DC bias at liquid nitrogen temperature,” Cryogenics, vol. 45, no. 6, pp. 463–467, 2005.

[12] A. Hammoud, S. Gerber, R. L. Patterson, and T. L. MacDonald, “Performance of surface-mount ceramic and solid tantalum capacitor for cryogenic applications,” in Proc. Annu. Rep. Conf. Electr. Insul. Dielectric Phenomena, 1998, vol. 2, pp. 572–576.

[13] H. Gui et al., “Development of high-power high switching frequency cryogenically cooled inverter for aircraft applications,” IEEE Trans. Power Electron., vol. 35, no. 6, pp. 5670–5682, Jun. 2020.

[14] C. B. Barth et al., “Design, operation, and loss characterization of a 1-kW GaN-based three-level converter at cryogenic temperatures,” IEEE Trans. Power Electron., vol. 35, no. 11, pp. 12040–12052, Nov. 2020.

[15] R. Chen et al., “A cryogenically-cooled MW inverter for electric aircraft propulsion,” in Proc. AIAA/IEEE Electric Airr. Technol. Symp., 2020, pp. 1–10.

[16] Keysight Ltd., “E4990A impedance analyzer,” E4990A datasheet, Aug. 2022.

[17] [Online]: Available: https://www.digikey.com/en/products/detail/ecpos+tdkelectronics/B32928C3360M00/4915318?s=N4lgTCBcDalEIGY-WE4wADCCEAYBAsjsALoC%2BQA

[18] [Online]: Available: http://www.tandresearch.com/index.php?mact=ListI2Products,cntnt01,detail0&cntnt01item=series-sdn_2&cntnt01template_summary=Side&cntnt01returnid=19

[19] [Online]: Available: https://www.digikey.com/en/products/detail/element.com/E3D20065D135606068?s=N4lgTCBcDalKIGYAJAqMBB6WJC6AvK&A

[20] [Online]: Available: https://www.digikey.com/en/products/detail/texas-instruments/ULN2803ADW/1912658

[21] [Online]: Available: https://www.digikey.com/en/products/detail/texas-instruments/ALQ3F18/1063904

[22] [Online]: Available: https://www.digikey.com/en/products/detail/panasonic-electric-works/ALQ3F18/1063904

[23] Skyworks Ltd., “Si827x,” Si827x datasheet, Jul. 2022.

[24] S. Yang, “Cryogenic characteristics of IGBTs,” Ph.D. dissertation, Birmingham, U.K.: Univ. Birmingham, 2005.

[25] Z. Zhang, B. Guo, F. F. Wang, A. E. Jones, L. M. Tolbert, and B. J. Blalock, “Methodology for wide band-gap device dynamic characterization,” IEEE Trans. Power Electron., vol. 32, no. 12, pp. 9307–9318, Dec. 2017.

[26] K. Tian et al., “Comprehensive characterization of the 4H-SiC planar and trench gate MOSFETs from cryogenic to high temperature,” IEEE Trans. Electron Devices, vol. 66, no. 10, pp. 4279–4286, Oct. 2019.

[27] B. J. Baliga, Fundamentals of Power Semiconductor Devices. New York, NY, USA: Springer, 2008.

[28] I. G. Ivanov, A. Henry, and E. Janzen, “Injection energies of phosphorus and nitrogen donors and aluminum acceptors in 4H silicon carbide from the donor-acceptor pair emission,” Phys. Rev. B, Condens. Matter, vol. 71, no. 24, 2005, Art. no. 241201(R).
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