Structure and properties of dislocations in interfaces of bonded silicon wafers

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Abstract. The realization of defined dislocation networks by hydrophobic wafer bonding allows the characterization of electrical properties of individual dislocations. The present paper describes the fabrication and characterization of SOI MOFSETs with various dislocations densities in the Si channel. The aim was to investigate the electrical properties in samples containing only 6 dislocations. A drain current of \( I_D > 1 \times 10^{-2} \) A induced by a single dislocation was determined by data extrapolation from current measurements in combination with previously analyzed samples containing a varying dislocation density.

1. Introduction

Dislocations in silicon have been extensively studied for more than 50 years. For instance, electron microscopy was applied to investigate the structure of individual dislocations, interactions, and the dynamic behavior of dislocations. The weak-beam method of electron microscopy evolved in the early 1970s [1, 2] demonstrated the dissociation of perfect dislocation into partial dislocations [3]. Modern high-resolution electron microscopy (HREM) and high-angle annular dark field (HAADF) imaging allow a new insight into the atomic structure of individual dislocations and grain boundaries [4-6]. The strain field around individual defects was recently analyzed by using special techniques such as geometric phase analysis (GPA) or peak-pairs analysis (PPA) of high-resolution structure images [7-9], or nano-beam electron diffraction (NBD) [10].

The electronic and optical properties of dislocations were studied by numerous analytical techniques such as the Hall effect, electron paramagnetic resonance (EPR), deep level transient spectroscopy (DLTS), photoluminescence, and electron beam induced current (EBIC) [4, 11-14]. Most of these studies used plastically deformed silicon in order to achieve defined dislocation arrangements and a high density of dislocations to attain the detection limit. Plastic deformation, however, result also in a large number of point defects and defect reactions making it sometimes difficult to interpret experimental data [11]. In order to avoid interactions between dislocations or between dislocations and other defects, methods are required allowing the realization and analyses of only a few dislocations or, in the ideal case, of an individual dislocation. A method to realize defined dislocation arrangements in a reproducible way is semiconductor wafer direct bonding (SWDB) originally developed to produce silicon on insulator (SOI) substrates and three-dimensional micro-electromechanical systems (MEMS) [15]. If two wafers are joined together without any interface layers, a two-dimensional dislocation network is obtained analogous to early experiments on bicrystals [16]. For bicrystals a Czochralski growth process is required allowing only the formation of specific grain boundaries such as \( \Sigma = 9 \) (rotation 38°56’17”, boundary plane (122), common [011] axis), \( \Sigma = 13 \) (rotation 26°37’12’”,

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boundary plane (510), common [001] axis), and $\Sigma = 25$ large angle grain boundaries (rotation $16^\circ 15^\prime 36^\prime\prime$, boundary plane (710), common [001] axis) [17]. Semiconductor wafer direct bonding, on the other hand, uses commercially available wafers making it possible to realize any grain boundary. Especially small angle grain boundaries having rotational angles $\alpha \ll 1^\circ$ are of interest allowing dislocation distances of a few hundred nanometers. Applying state of the art techniques for preparation and analyses individual or a small number of dislocations can be characterized.

2. **Semiconductor wafer direct bonding**

Semiconductor wafer direct bonding (SWDB), or fusion bonding, describes a method to join mirror-polished semiconductor wafers at room temperature without the addition of any glue or external forces. The bonding of silicon wafers was first reported 1985/86. Lasky [18] described the bonding of two oxidized silicon wafers to form silicon on insulator (SOI) substrates. In the same time, Shimbo et al. [19] analyzed the bonding behavior of non-oxidized silicon wafers forming an epitaxial substrate for power devices.

SWDB requires wafers with a high degree of flatness, parallelism and smoothness. Also clean surfaces are necessary which are free of particulate, organic and metallic contaminations. This is important because the surface cleanliness has a direct effect on both the structural and electrical properties of the bonding interface as well as on the resulting electrical properties of the bonded material. After cleaning an activation of the surfaces is required prior to bonding. Then the two mating wafers are brought together face to face in air at room temperature. The top wafer is floating on the other due to the presence of a thin cushion of air between both wafers. When an external pressure is applied onto a small part of the pair to push out the intermediate air, a bond is allowed to be formed by surface attraction forces between the wafers at this location. Depending on the surface conditions, two bonding mechanisms are distinguished:

(i.) **Wafer bonding using hydrophilic surfaces** is the most common technique [15]. Silicon surfaces are covered with an oxide layer under room temperature conditions. If oxidized surfaces are bonded, an oxide layer results in the interface. A model for hydrophilic wafer bonding was first described by Stengl et al. [20] using the analogy of surface chemistry of silica and oxidized silicon. Based on results of infrared spectroscopy, a three-dimensional hydrogen bonded network of water molecules was assumed. The water is primarily bonded via Si–OH groups on the silica surface. During heating above $180^\circ\text{C}$ the adsorbed water molecules desorb under atmospheric pressure leaving a hydroxylated silica surface, on which most of the SiO groups are linked via hydrogen atoms. OH groups are bonded more stably with increasing temperature. Annealing above $800^\circ\text{C}$ results in the formation of strong Si-O bonds via the interface.

(ii.) **When the oxide layer from a crystalline silicon substrate is removed with HF**, a hydrophobic surface with unique properties is obtained, i.e. having a good resistance to chemical attack and a low surface recombination velocity, which means a surface with a very low density of surface states. Bonded hydrophobic wafers are characterized by completely different interfaces. The removing of the oxide results in two silicon lattices that are in contact, and Si-Si bonds are formed via the interface. Crystal defects (dislocations) are generated forming a two-dimensional network in order to match both crystal lattices. The structure of the dislocation network depends on the surface orientation of both wafers. Figure 1 shows transmission electron microscope (TEM) images of dislocation networks formed by bonding of (100)/(100)-, (110)/(110)-, and (111)/(111)- wafer pairs. Bonding of Si(100) wafers, for instance, cause a $\Sigma = 1$ (100) small angle grain boundary characterized by a square-like mesh of screw dislocations expected from theory [21]. These dislocations are formed by the rotational misfit (twist) between both crystal lattices. There is, however, an additional tilt component caused by the deviation on the [001] axis of real wafers (cut-off). The tilt component is compensated by a periodic array of $60^\circ$ dislocations. The spacing between dislocations, $S$, in both networks are indirectly proportional to the misalignment angle and are given by
for the screw dislocation network. On the other hand, the relation between dislocation distance and tilt angle of the network formed by 60°-dislocations follows as

\[ S_{\text{tilt}} = \frac{a}{2 \cdot \tan \alpha_{\text{tilt}}} \]

In both equations, \( a \) represents the lattice constant (\( a = 0.543 \) nm for Si) and \( \alpha_{\text{twist}} \) and \( \alpha_{\text{tilt}} \) are the angles of misorientation of the twist and tilt components, respectively.

Both dislocation fractions were investigated for hydrophobic wafers bonded under environmental conditions [22-25] and under ultra-high vacuum (UHV) conditions [26, 27]. There are different observations for wafer pairs bonded under UHV conditions. Some reports present dislocation networks already after bonding at room temperature [28], while dislocation networks are observed by other authors only after a subsequent annealing above 800°C [27]. The reason probably is that the boundary is unrelaxed after bonding at room temperature, while relaxation occurs for energetic reasons only at higher temperatures [29].

Figure 1. TEM images of the dislocation structure in the interfaces of hydrophobic bonded wafer pairs.

a) (100)/(100) bonded pair
b) (110)/(110) bonded pair
c) (111)/(111) bonded pair

Annealing at 1000°C for 4 hours was applied after the initial bond process. Plan-view images (25° beveled samples).

Numerous investigations on (100)/(100) bonded wafer pairs showed that there are no differences in the structure of the interfacial dislocation networks produced by bonding under UHV and environmental conditions. Differences are only obtained in the dislocation spacing (caused by the different twist angles) and in the types of interaction between screw dislocations and 60°-dislocations.
(caused by different twist and tilt angles as well as different annealing processes). An almost undisturbed mesh of the screw dislocations exists on {100}-terraces while at steps on the surface (characterized by the 60°-dislocations) interactions between both dislocations portions are found. Different interactions were discussed for hydrophobic bonded wafers [30] and grain boundaries in sintered silicon [31].

Dislocation reactions modify the existing dislocation network especially at very low twist and tilt angles ($\alpha_{\text{tilt}} \equiv \alpha_{\text{twist}} < 0.1°$) where the mesh size of the screw dislocation network reaches the same values as the distance of the 60°-dislocations. At $\alpha_{\text{tilt}} \equiv \alpha_{\text{twist}} \equiv 0.07°$ dislocation networks with hexagonal meshes appear [25]. Twist and tilt angles below 0.1° can be realized experimentally only by aligned wafer bonding allowing the control of the twist angle down to $\alpha_{\text{twist}} = \pm 0.005°$ [24, 32]. At $\alpha_{\text{twist}} \leq 0.001°$ dislocation networks were not observed. Instead, segments of individual dislocations of different geometries were found. Straight segments of screw dislocations are observed first, while – probably at lower angles – loops of various geometries are dominant [24].

3. Properties of dislocations in bonded interfaces

Dislocations in the interface of bonded wafers possess numerous remarkable properties which may be used for different applications [33, 34]. The electrical properties of bonded hydrophobic silicon wafers were studied for the first time by Bengtsson et al. [35]. The measurement of the capacitance-voltage (CV) characteristics on bonded unipolar wafers were interpreted on the assumption of two distributions of interface states, one of acceptors and one of donors, causing a potential barrier at the bonded interface. The origin of the interface states was assumed to be impurities and crystal defects. More recent analyses by EBIC proved barrier heights generally smaller than 100 meV for different types of bonded hydrophobic wafers [36]. The concentration of deep levels along the interface was determined to be a few $10^5$ per cm. Low concentrations of deep levels at the interface are also the reason for low dark currents, an improved CV-characteristics, and fast rise times of pin-diodes prepared on bonded hydrophobic wafers [37].

The luminescence properties of dislocation networks were also studied. Figure 2 shows the luminescence spectra of different bonded samples. The spectra are obtained from samples having different misorientation. Detailed photoluminescence and cathodoluminescence measurements provide direct evidence that the wavelength of light emitted from the dislocation network could be tailored to some extent by misorientation of the wafers during the bonding procedure. D1 or D3 lines have the largest intensity in the spectra due to the variation of the twist angle from 8.2° to 9°. Thus the luminescence spectrum can be tailored by the misorientation angles in a controlled manner and the dominance of either D1 or D3 radiation can be attained. Furthermore, in some special cases the D1 emission could completely dominate the spectrum, even at room temperature (RT) [33].

An external bias voltage applied across the bonded interface can significantly enhance the luminescence intensity from the bonded interface. The reason for this effect can be that, on the one hand, the external bias could reduce the potential barrier at one side of the bonded interface and therefore increase the occupancy of dislocation related states responsible for the D-lines; on the other hand, the bias could change the distribution of minority carriers close to the bonded interface. This results in the variation of carrier recombination velocity at the bonded interface and in relevant variation of luminescence. The application of the proper external bias voltage enhances the total luminescence at any excitation level, but the enhancement is more pronounced for lower excitation conditions. A maximum enhancement factor of 130 was achieved.

4. Analyses of individual dislocations

The study of individual dislocations or only of a small number of dislocations is an important issue because all of the interactions between defects can be eliminated. This results in more precise data
about the electronic structure of dislocations and, combining these investigations with microscopic observations, conclusions about the correlation between the structure and properties of dislocations can be derived. A combination of bonded wafer pairs with preparation methods to separate individual dislocations or a small number of dislocations allow such experiments. Twist angles between two bonded Si wafers below 0.1° results in dislocation distances of more than 100 nm (equation 1). Using photolithography and etching techniques, individual dislocations can be separated and measured.

Diodes and metal-oxide-semiconductor field-effect transistors (MOSFETs) were prepared on such bonded wafers. In order to avoid the effect of the bulk material, dislocation networks were realized in SOI wafers having only a thin device layer. The substrates were prepared by hydrophobic wafer bonding of commercially available SOI wafers having the following specification of the silicon device layer: CZ-grown silicon, 150 mm diameter, p-type, resistivity $\rho = 13.5 - 22.5$ $\Omega$cm, <100>-orientation, thickness of the buried oxide (BOX) layer was 60nm or 1000 nm. The final device layer thicknesses of 15 nm and 40 nm were obtained by thinning down the initially 260 nm or 600 nm thick layers, respectively, by thermal oxidation. After dipping in diluted HF the wafers were immediately bonded under hydrophobic conditions in an atmospheric environment. Various twist angles between $0.01° < \alpha_{\text{twist}} < 0.65°$ were realized. The bonded wafer pairs were annealed at 1050°C for 4 hours in nitrogen. Finally one of the handle wafers was removed by a combination of mechanical grinding and chemical etching (spin etching) followed by chemical etching of the oxide layer. This process results in SOI wafers having 2-dimensional dislocation networks in their thin device layers (figure 3).

SOI MOSFETs were prepared on such substrates using lithographic techniques and dry reactive ion etching (RIE). The channel region was defined first. Because dislocations are parallel to <110>-directions in Si, they are parallel to the channel. In order to study the effect of the dislocation density, channel width and length, respectively, are varied between 1 $\mu$m and 10 $\mu$m. Source and drain contacts were formed by As$^+$ implantation (5 kkeV, $1\cdot10^{15}$cm$^{-2}$) combined with a RTA step (950°C, 60 sec.). A thin gate oxide of about 6 nm was formed by thermal oxidation. The device gates were prepared by low-pressure chemical vapour deposition (LP-CVD) of polycrystalline silicon (100 nm thick) followed

Figure 2. The impact of the misorientation/dislocation structure on the luminescence spectra of dislocation networks. The misorientation (tilt and twist components) are indicated in the figure. Cathodoluminescence spectra recorded at 77K.
by As⁺ implantation (30 keV, 1·10¹⁵ cm⁻²) and a RTA step (950°C, 60 sec). Finally, contacts were formed by Al deposition and annealing at 420°C for 30 minutes in hydrogen.

Figure 3. TEM cross-section image of a SOI substrate with a dislocation network in the device layer. The dislocation distance is about 15 nm corresponding to a twist angle of about 0.7°.

Figure 4. I-V characteristics of SOI-MOSFETs with and without dislocations (V_G = 0V). The distance between contacts is 1 μm, while widths of 1, 5, and 10μm are used. Because the dislocation spacing is about 34 nm, 30, 150, and 300 dislocations, respectively, are present in the channel. The reference is an SOI wafer having the same device layer thickness but without dislocations.

Figure 4 shows the conductance of dislocation layers by measuring MOSFETs at gate voltages V_G = 0V. A characteristic increase of the current I is obtained for devices containing dislocations compared to a reference sample prepared on a SOI wafer with the same device layer thickness (40 nm). The current increase depends on the dislocation density and probably on the type of the dislocation. The reason is that dislocations form channels of higher conductance in the silicon layer resulting in a higher carrier concentration in the channel [38] but increase also the effective carrier mobility which is consistent with quasi-ballistic transport along dislocations [39]. From figure 4, we can see that the carriers transported through dislocations are electrons [40]. Furthermore, it can be also seen from the figure that the current increases as the number of dislocations decreases. The highest current is obtained if only 30 dislocations are present.
The I-V characteristics of nMOSFETs with and without a dislocation network in the channel are shown in figure 5. The thickness of the device layer was about 80 nm. The channel length was 1 µm. Typical output and transfer characteristics are obtained for the reference sample without a dislocation network in the device layer (figure 5 a,b). The devices are characterized by a sub-threshold slope \( S = 100 \text{ mV/dec} \) and a threshold voltage \( V_T = -150 \text{ mV} \). The output and transfer characteristics of a device with a dislocation network in the channel are shown in figures 5c and 5d. It can be seen that higher drain currents \( (I_D) \) are measured at the same gate \((V_G)\) and drain \((V_D)\) voltages, compared to the devices without a dislocation network. The increase of the drain current even at very low gate voltages is about one order of magnitude. Similar results were also obtained by other authors [38] and are ascribed to the presence of dislocations. The relatively high source-drain current even at \( V_G = 0 \text{V} \), in contrast to the reference sample, indicates the presence of charged carriers on the dislocations.

The analysis of the device data clearly proved that the number of dislocations in the channel characteristically affects the device parameter. Indications are found by measurements on devices prepared on wafers having dislocation networks with different dislocation density. As described above, such networks are realized by varying the twist angle during the wafer bonding process. Besides devices prepared on a dislocation network with \( \alpha_{\text{twist}} = 0.31^\circ \) (resulting in a dislocation

Figure 5. Output and transfer characteristics of nMOSFETS without dislocations (a,b) and with a dislocation network (c,d). The insets represent the transfer characteristic \((I_D = f(V_G))\) in linear scale for a better current comparison. The device layer thickness was 80 nm. The channel length and width, respectively, for both devices are 1 µm. The sub-threshold slope of the dislocation MOSFET is in this example 550 mV/dec.

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**Figure 5.** Output and transfer characteristics of nMOSFETS without dislocations (a,b) and with a dislocation network (c,d). The insets represent the transfer characteristic \((I_D = f(V_G))\) in linear scale for a better current comparison. The device layer thickness was 80 nm. The channel length and width, respectively, for both devices are 1 µm. The sub-threshold slope of the dislocation MOSFET is in this example 550 mV/dec.
spacing of about 35 nm) analogous samples were prepared on a wafer having a dislocation network characterized by \( \alpha_{\text{twist}} = 0.035^\circ \). Here, the dislocation spacing is about 150 nm. Using channel widths, \( W \), between 1 \( \mu \)m and 10 \( \mu \)m, devices having about 660 dislocations (at a dislocation spacing of 15 nm and \( W = 10 \mu \)m) up to 6 dislocations per channel at a dislocation spacing of 150 nm and \( W = 1 \mu \)m were prepared. The \( I_D - V_D \) curves of these devices show that the drain current depends on the number of dislocations in the channel. At \( V_D = 2 \) V, a drain current of \( 3 \times 10^{-3} \) A is obtained if there are only 6 dislocations in the channel. On the other hand, a value of \( I_D = 2 \times 10^{-6} \) A is measured under the same conditions if the channel includes about 660 dislocations.

![Figure 6. Source-drain current \( I_D \) as a function of the number of dislocations in the channel. Measurements at \( V_D = 2 \) V and \( V_G = 0 \) V. Different symbols characterize measurements on various wafers having different dislocation densities.](image)

Besides \( I_D \) also the threshold voltage (\( V_T \)) and the sub-threshold swing of the MOSFETs dependent on the dislocation density. Increasing the number of dislocations by a factor of 10, by increasing the channel width from 1 \( \mu \)m to 10 \( \mu \)m, results in a decrease of \( V_T \) from about -400 mV down to -150 mV. An explanation could be the dependence of \( V_T \) and the sub-threshold voltage shift (\( \Delta V_T \)) on the effective channel length for MOSFETs [41]. Decreasing the effective channel length results in an increase of \( \Delta V_T \). If dislocations are present in the channel, the effective channel length is defined by the number of dislocations as the effective transport channels. Therefore, reducing the number of dislocations in the channel results in an increase of \( V_T \) and \( \Delta V_T \).

On the other hand, the sub-threshold slope increases as the dislocation density increases. An analogous increase of the sub-threshold swing is generally interpreted as a thickness effect of the device layer for short channel SOI-MOSFETs and is caused by an inhomogeneous electron concentration in the layer [42].

Measurements on MOSFETs prepared on wafers with different dislocation networks proved a dependence of the drain current on the dislocation density (figure 6). The figure clearly shows that the current depends only on the number of dislocations where the current increases as the number of dislocations decreases. Because the data were measured on different wafers prepared in different experimental runs, impurities on the dislocations would modify the results. Fitting the data allows to extrapolate the current given by one dislocation of more than \( 10^{-2} \) A. This corresponds to a current density of more than 100 A/cm. Further measurements are required to confirm this result.

5. Conclusions
The analysis of the structure and properties of dislocations is a fundamental issue in materials science. Most of the hitherto existing investigations used dislocation arrangements having a high density of dislocations. In order to avoid interactions between dislocations or between dislocations and other defects, methods are required allowing the realization and analyses of only a few dislocations or, in the ideal case, of an individual dislocation.

A method to realize defined arrangements in a reproducible way is hydrophobic wafer bonding. Two-dimensional dislocation networks are produced if two wafers are bonded. The length and distance of the dislocations in a network is defined by the mesh size and can be up to several micrometers. Combining wafer bonding with pattern formation techniques (photolithography and dry etching), devices were realized allowing the measurement of the electrical characteristic of only a few dislocations.

The presented data clearly show an indirect behaviour of the drain current on the number of dislocations in the channel. The fact that the highest current is obtained if only a few dislocations are present allows the conclusion that electrically active centres in the dislocation core of the straight dislocation segments are responsible for the electron transport while dislocation nodes and dislocation segments oriented orthogonal to the channel direction act as “scattering centres” and reduce the carrier transport.

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