The effect of interface roughness scattering on Si SOI FinFET with Ando’s and extended Prange and Nee model

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Abstract. A new multi-subband interface roughness scattering (IRS) model is incorporated into a 3D Finite Element Monte Carlo simulator with 2D Schrödinger equation based quantum corrections. The model takes advantage of wavefunctions and energy levels obtained in solutions of Schrödinger equation on slices across the channel to calculate the respective form factors. The new 3D code is then used to forecast the performance of 10.7 nm gate length SOI Si FinFETs with rectangular cross-section and rounded corners. We found that the multi-subband IRS is much stronger at large electron kinetic energies resulting in a drive current of 600 mA/µm² that is 25% reduction when compared to 3D Ando model.

1. Introduction
Non-planar multi-gate transistors [1] are the leading solutions for sub-16 nm digital CMOS technology [2] scaled to ultimate limit thanks to superior electrostatic integrity and delivering a large ON-current. In this scaled process, interface roughness scattering (IRS) is considered to be one of the key limiting factors to carrier transport [3][4] because fabrication of the interface between semiconductor and channel in multi-gate nanoscaled devices is harder to control [5]. In this work, we have implemented a new multi-subband IRS model which uses wavefunctions and energy levels from our 3D finite element (FE) Monte Carlo (MC) toolbox [6] with 2D FE Schrödinger equation quantum corrections (SEQC) [7]. The wavefunctions and energy levels are used to calculate form factors entering the multi-subband scattering rate adapted to the FE mesh. The new multi-subband IRS model within the 3D FE MC is then applied to 10.7 nm gate length SOI FinFETs with rectangular cross-section (see Fig. 1), designed according to the ITRS guidelines [8], by the FE method and compared with a basic 3D Ando model.

2. Monte Carlo Code
In the past, a 3D FE ensemble MC simulation toolbox with density gradient (DG) [6] demonstrated an excellent agreement with experimental I_D-V_G characteristics of the 25 nm gate length SOI FinFET [9]. Later, the DG quantum corrections in MC toolbox has been replaced by SEQC [7] to predict transistor performance when in deep nanoscaled region [10]. A 3D FE mesh of the device in the 3D MC toolbox accommodates 2D FE planes perpendicular to the transport direction (see Fig. 2) [7]. The extracted 2D potential V(y, z) from the 3D
electrostatic potential $V(r)$ is used to solve the 2D Schrödinger equation:

$$\frac{-\hbar^2}{2} \nabla_\perp \cdot \left[ (m^*)^{-1} \cdot \nabla_\perp \psi(y,z) \right] + U(y,z)\psi(y,z) = E\psi(y,z),$$

(1)

where $E$ is the energy, $(m^*)^{-1}$ is the inverse effective mass tensor, $\psi(y,z)$ is the wavefunction penetrating the oxide, and $U(y,z) = -[qV(y,z) + \chi(y,z)]$ is the potential energy with $\chi(y,z)$ being the electron affinity. The eigenstates of the Schrödinger equation are used to calculate the 2D quantum density $n_q$. The quantum density is then interpolated onto the 3D simulation domain to obtain the quantum corrected potential which, in turn, is used to move particles. More details on the 3D FE MC toolbox can be found in Refs. [6] [7] [11].

**Figure 1.** Schematic of the simulated Si SOI FinFET. The device has a Gaussian doping profile with $\sigma$ of 3.45 nm in the transport direction and an effective oxide thickness (EOT) of 0.62 nm.

**Figure 2.** The interface slices along the transport direction (x-axis) that are also the position of the 2D FE slices used by the 2D Schrödinger solver.

### 3. Interface Roughness Scattering Model

Many IRS models require a power spectrum of the interface roughness commonly described by Gaussian and exponential forms [12]. We have chosen the latter as suggested in Ref. [13] given by:

$$C(q) = \frac{\pi \Delta_{RMS}^2 \Lambda^2}{\sqrt{1 + \frac{q^2 \Lambda^2}{2}}}$$

where $\Delta_{RMS}$ is the RMS height of the interface roughness, the $\Lambda$ is the correlation length and the $q$ is the wavevector. The value of $\Delta_{RMS}$ is 0.57 nm, taken from experimental data [14] and $\Lambda$ is 1.7 nm [13].

**3.1. Ando Model**

The matrix element for Ando model is given by [15]:

$$\Gamma(k) = \frac{m^*e^4 \Delta_{RMS}^2 \Lambda^2 E_\perp^2}{\hbar^3 c^2 S \sqrt{1 + k^2 \Lambda^2}} \mathcal{E} \left( \frac{k \Lambda}{\sqrt{1 + k^2 \Lambda^2}} \right)$$

(3)

where $E_\perp$ is the transverse electric field and $\mathcal{E}$ is the complete elliptic integral of the first kind. Fig. 4 shows the calculated maximum scattering rate for the IRS model using a rejection technique which takes into account the local electric field at the scattering event [16].

**3.2. Extended Prange & Nee Model**

The multi-subband EPN model is based on a 2D formulation of Prange & Nee scattering model for arbitrary paths [5]. Wavefunctions at each eigenstate are extracted along the interface for all the 21 slices (see Fig. 2), then the form factors are calculated by:
\begin{equation}
\psi_{n,k}^* \psi_{n',k'} \Delta V (4)
\end{equation}

where \( n, n' \) are the initial and final energy levels, respectively, \( \Delta V \) is the potential barrier between the Si channel and the high-\( \kappa \) dielectric. Finally the scattering rate is calculated by:

\begin{equation}
\frac{1}{\tau_{n,n'}(E)} = \frac{1}{2\hbar} \int_R |F_{n,n'}(q_\perp)|^2 C(q) dq_\perp g_{1D,n'}(E) A (5)
\end{equation}

where the \( F_{n,n'}(q_\perp) \) is a fast Fourier transform (FFT) of the form factors, \( C(q) \) is the exponential power spectrum of the interface roughness, \( g_{1D,n'} \) is the 1D density of states (DOS) and \( A \) is the area of the channel.

Fig. 3 shows the time-line of the simulation. A drift-diffusion (DD) simulation is run beforehand to acquire results for the subthreshold slope and also to provide an initial solution for the MC. To speed up the MC simulation, we run a pre-simulation using 3D Ando model followed by another pre-simulation using the multi-subband EPN model setting a maximum IRS rate for each energy. This rate is calculated as the maximum rate over all slices for the given energy. During the MC simulation itself, the instantaneous IRS rate, depending on the actual potential distribution in the device, is calculated to perform a rejection technique. The instantaneous IRS rate is interpolated from the nearest slice and assumes an exponential decay of the roughness potential strength as a function of distance from the interface [3]. Fig. 4 compares the maximum average scattering rates for both models. In case of the Ando model, the scattering rate reduces with increasing energy. For the multi-subband EPN model, the scattering has a maximum at the subband positions as expected. Note that the Ando model gives a higher probability of scattering below 0.15 eV while at a larger energy the trend is opposite.

![Figure 3. Time scale for the 3D FE MC with 2D Schrödinger QC toolbox.](image)

![Figure 4. The maximum scattering rate from 3D (Ando) compared to multi-subband (EPN) model. The EPN is for the 20 lowest electron subbands at \( V_D = 0.05 \) V and \( V_G = 0.0 \) V showed only up to 0.77 eV but calculated up to 3 eV.](image)

4. Effect of the Interface Roughness

The new IRS model incorporated into the 3D SEQC FE MC toolbox and then applied to investigate \( n \)-channel SOI FinFET with a gate length of 10.7 nm and a \( \langle 100 \rangle \) channel orientation designed following the ITRS guidelines [8]. We study a rectangular-like cross-section with rounded corners to demonstrate realistic nanoscale device geometry. Fig. 5 shows \( I_D-V_G \) characteristics, with the current normalized-to-area, comparing the IRS models at both low (\( V_D = 0.05 \) V) and high (\( V_D = 0.7 \) V) drain biases. At low drain bias, the current is slightly overestimated by the Ando model as the gate voltage increases above 0.4 V by about 8%. At high drain bias, the difference in overestimation of the current between the two IRS models largely increases to 25%. Table 1 lists the current at \( V_G-V_T = 0.7 \) V and subthreshold slope (SS) from drift-diffusion (DD) simulations. Note that drain induced barrier lowering (DIBL) obtained from MC is larger than DD since it accounts for quantum capacitance [10].
5. Conclusions

A new multi-subband EPN model has been incorporated into the 3D FE SEQC ensemble MC simulation toolbox for physically based modelling of nanoscale multi-gate transistors. The new 3D tool has been employed to study the effect of the IRS on I-V characteristics at low and high drain biases in the 10.7 nm gate length Si SOI FinFETs for a rectangular-like realistic cross-section. We have found that the multi-subband EPN IRS has a much stronger impact on non-planar devices for large electron kinetic energy (from above 0.18 eV) than the 3D Ando IRS. The 3D MC simulations that use the multi-subband EPN model predict a drive current of 161 mA/µm² at a low drain bias of 0.05 V. This is about 8% smaller when compared to the results obtained using the 3D Ando model, which is negligible difference. However, at a high drain bias of 0.7 V, the predicted drive current is 600 mA/µm², smaller by about 25%, which is noticeable reduction in the drain current. The IRS is thus essential for meaningful modelling of carrier transport in nanoscale multi-gate transistors.

References

[1] Huang X and et al 1999 Electron Devices Meeting, 1999. IEDM ’99. Technical Digest. International pp 67–70
[2] Hook T 2012 Custom Integrated Circuits Conference (CICC), 2012 IEEE pp 1–7
[3] Jin S, Fischetti M V and Tang T w 2007 J. Appl. Phys. 102 083715
[4] Wang J and et al 2005 Appl. Phys. Lett. 87 043101
[5] Stanojevic Z and Kosina H 2013 Simulation of Semiconductor Processes and Devices (SISPAD), 2013 International Conference on pp 352–355
[6] Aldegunde M, Garcia-Loureiro A and Kalna K 2013 IEEE T. Electron. Dev. 60 1561–1567
[7] Lindberg J and et al 2014 IEEE T. Electron. Dev. 61 423–429
[8] ITRS(2012) International technology roadmap for semiconductors http://www.itrs.net/Links/2012ITRS/Home2012.htm
[9] Basker V and et al 2010 VLSI Technology (VLSIT), 2010 Symposium on pp 19–20
[10] Nagy D and et al 2015 IEEE T. Nanotechnol. 14 93–100
[11] Aldegunde M, Scoane N, Garca-Loureiro A and Kalna K 2010 Comput. Phys. Commun. 181 24 – 34
[12] Esseni D, Palestri P and Selmi L 2011 Nanoscale MOS Transistors: Semi-Classical Transport and Applications (Cambridge University Press)
[13] Goodnick S M and et al 1985 Phys. Rev. B 32(12) 8171–8186
[14] Tang X and et al 2009 IEEE T. Nanotechnol. 8 611–616
[15] Ferry D 2000 Semiconductor Transport (Taylor & Francis)
[16] Kalna K, Yang L and Asenov A 2005 Solid-State Device Research Conference, 2005. ESSDERC Proceedings of 35th European pp 169–172