A Ka-Band Radar Frequency Synthesizer Design Based on DDS Technology

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ABSTRACT

This paper puts forward a design of frequency synthesizer based on DDS for Ka-band radar signal simulation. RF signal is generated through the AD9854 DDS chip driving the PLL and VCO. The testing results showed that this Ka-band frequency synthesizer has low phase noise and wider bandwidth, and can generate Ka-band continuous wave signal, LFM signal for radar signal simulation.

INTRODUCTION

The frequency source is the core of modern radar system, in order to meet the need of all-phase reference, the radar signal generator must have the higher performance in wider band. In recent years, the development of DDS and PLL technique, provides a better method to design the higher performance frequency synthesizers. This paper puts forward a design of frequency synthesizer based on DDS for Ka-band radar signal simulation. The output of VCO is phase locked by DDS. By the DDS driving PLL, we can obtain the higher performance Ka-band continuous wave signal and LFM signal.

In the Paragraph II, this paper provides the Structure of DDS driving PLL frequency synthesizer and designs the schematic circuit diagram. In the Paragraph III, the phase noise and frequency capture time are analyzed. Paragraph IV summarizes the experiments and measurements results.

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ENGINEERING IMPLEMENTATION

The Structure of Frequency Synthesizer

The Structure diagram of DDS-driving PLL for Ka-band frequency synthesizer is shown in Fig.1. The crystal oscillator produces the reference frequency of DDS, $f_{ref}$, $f_{DDS}$ is the output frequency of DDS and is controlled by the frequency tuning word $K$. The reference frequency of PLL is driven by the $f_{DDS}$. The Charge Pump (CP) controls the output of VCO. We can obtain the output signal of this frequency synthesizer by multiplying $f_{VCO}$. $f_{diejia}$ is the LFM signal and the additional Doppler frequency signal. While The PLL is locked, the output frequency of frequency synthesizer and the VCO is

\[
 f_{\text{out}} = 4 \times f_{\text{vco}} \tag{1}
\]

\[
 f_{\text{vco}} = (BP + A) \times \frac{f_{\text{DDS}}}{R} \tag{2}
\]

$f_{\text{DDS}}$ is controlled by the frequency tuning word $K$, and

\[
 f_{\text{DDS}} = \frac{K}{2^M} \cdot f_{\text{CLK}} \tag{3}
\]

Where $M$ is the phase accumulator word length of DDS and $f_{\text{CLK}}$ is the internal clock of DDS. Then equation (2) can be expressed as

\[
 f_{\text{vco}} = \frac{BP + A}{R} \cdot \frac{K}{2^M} \cdot f_{\text{CLK}} \tag{4}
\]

In the Structure shown in Figure.1, since DDS chip has good frequency resolution ratio, from (4) we can find that the output signal has a better frequency resolution ratio than traditional Structure. LFM signal and Doppler frequency signal can be easily acquired using DDS. While the DDS works on the LFM mode, the output of DDS can be expressed as

\[
 f_{\text{diejia}} = \frac{(K + \Delta K \times l)}{2^M} \times f_{\text{CLK}} \tag{5}
\]
Where $\Delta K$ is the change rate of frequency tuning word $K$. $t$ is the time of duration of pulse of LFM signal. From the equation (5), the Doppler frequency $f_d$ is

$$f_d = \frac{K}{2^M} \times f_{CLK}$$

(6)

The band $B$ of LFM signal is

$$B = \frac{\Delta K \times t}{2^M} \times f_{CLK}$$

(7)

The Circuit Design

This design implements the low phase noise level signal generating, the center frequency is required 35GHz, the band is 3 GHz, the frequency resolution ratio is 100KHz, the phase noise level is less than $-85$dBc/Hz@1KHz. From the equation (1), the $f_{VCO}$ is required 8.375GHz $\sim$ 9.125GHz, the band $B$ of LFM signal is 150MHz. According to the design requirement, we use the AD9854 DDS module and ADF4106 PLL device to design the circuit[1]-[2]. The Single chip can receive the data which come from the ISA bus and write the FTW to the AD9854, which make AD9854 produce the frequency signal.
We use the Single Chip of µPSD3251 to provide the write time diagram. The internal clock of AD9854 can be 300MHz by doubling the external reference clock. It can easily generate low frequency LFM signals with better dynamic performance. The ADF4106 has a wide band, which consists of a digital phase frequency detector (PFD), a precision charge pump, a programmable reference divider, programmable dual-modulus prescaler. It has fast settling time and low phase noise performance. The loop filter design can remove the high frequency component and ensure the loop stability. We use AD820 amplifier to design the loop filter[3]-[5].

ANALYSIS AND SIMULATION

In order to analyze and evaluate the performance of the frequency synthesizer we designed, we use the ADI SimPLL software to calculate the phase noise curve and the capture time.

Phase Noise

The output phase noise is simulated at the central frequency 35GHz. The result of simulation is shown in Figure.3. We find that the phase noise level at $-87$dBc/Hz@1KHz and at $-140$dBc/Hz@1MHz, which verifies the frequency synthesizer has a good phase noise performance and meet the designing need.

Capture Time

The capture time is the time of the frequency synthesizer change the frequency from one frequency point to another frequency point. The capture time is decided by the PLL, which will be faster locked when the PD works on the higher frequency. We make the simulation when the locked frequency is 35GHz.

![Figure 3. The phase noise curve.](image-url)
EXPERIMENTS AND MEASUREMENTS

In order to test the performance of the Ka-band frequency synthesizer given in this paper, we use the frequency synthesizer to produce the single frequency continuous wave signal, the modulated frequency signal and LFM pulse signal.

The Continuous Wave Signal

A continuous wave signal of VCO at 8.75GHz is produced using the frequency synthesizer. The output signal is the four frequency multiplication of the $f_{\text{VCO}}$, the $f_{\text{out}}$ is shown in the Fig. 4. The $f_{\text{out}}$ can be changed from 33.5GHz to 36.5GHz, the phase noise level is less than $-85$dBc/Hz@1KHz.

The Modulated Frequency Signal

A pulse modulated frequency signal is produced and measured. The frequency spectrum is shown in Fig. 5.
LFM Pulse Signal

A linear FM pulse signal is produced and measured. The frequency spectrum is shown in Fig.6. The linear FM pulse width is from 10µs to 50µs, the linear FM bandwidth is from 10 MHz to 150 MHz.

CONCLUSIONS

This paper provides using the AD9854 DDS module and ADF4106 PLL device to design a Ka-band frequency synthesizer. The circuit diagram is given and its performance is analyzed. Experiments results shown that the Ka-band frequency synthesizer has wider bandwidth and better performance and can be used to produce multiple radar signals for simulation, such as continuous wave signal, the modulated frequency signal and LFM pulse signal. It meets the demand of Ka-band radar signal simulation.

REFERENCES

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