Hardware design and implementation of digital payload data receiver of LAPAN-A2 satellite

R Hartono*, D E Amin, R Permala, and R Yatim

Satellite Technology Centre, National Institute of Aeronautics and Space (LAPAN), Bogor 16310, Indonesia
*rommy.hartono@lapan.go.id / rommyhartono@ymail.com

Abstract. LAPAN A2 is the second-generation Indonesian micro satellite which designed and developed in Indonesia. This satellite was launched in September 2015 in India as piggy-back. Orbit of this satellite is circular and near equatorial with altitude approximately 650 km. This satellite carries digital payloads such as digital space camera, Automatic Identification System (AIS) for vessel traffic, and upgrade S-Band transmitter 3 Mbps. The digital payloads of LAPAN-A2 satellite data is downloaded in Rancabungur Ground Station, which is equipped with 11 meters antenna using S-Band frequency. The data generated from the satellite is in raw format. For ensuring this missions, it needs some hardware for receiving digital payload data of LAPAN-A2 satellite. This paper describes result of design, implementation and test from the hardware for receiving digital payload data of LAPAN-A2 Satellite. The hardware uses Morph-IC FPGA using software Quartus and microcontroller ATMega128 embedded using Basic compiler-AVR, then the design and layout of printed circuit board uses Eagle Software. From the result of the hardware functionality test of hardware payload data receiver system, the hardware is capable to pass the signal from transmitter S-band around 3Mbps and forwarded to PC by using communication serial with speed 6Mbps, and is able to download digital payload of LAPAN-A2 satellite either digital space camera or AIS data. The amount of received data depends on the height of elevation and attitude of the satellite.

1. Introduction

The objective of LAPAN-A2 satellite project is to achieve the design, integration and operation of micro satellite in Indonesia. LAPAN-A2 main mission is Earth Observation using digital RGB camera (5 m resolution). In addition, the satellite carries AIS (Automatic Identification System) receiver to monitor maritime traffic, a reaction wheel made by LAPAN for space proofing, and an amateur radio Automatic Packet Reporting System (APRS), as well as an amateur radio voice repeater for Indonesian Amateur Radio Organization (ORARI). Due to this cooperation, LAPAN-A2 is called LAPAN-ORARI [1].

The digital payloads of LAPAN-A2 are digital camera and AIS. The first is digital camera system. It is a Complementary Metal–Oxide–Semiconductor Image Sensor (CMOS-IS) 4000 model provided by Theta System Elektronik, Germany [2]. With a focal length of 60 centimeters, the camera system can delivers frames of 12 by 12 kilometers at a ground resolution of 6 meters from 650 kilometers in altitude. The RGB format camera can tolerates large variations in illumination and supports different operational modes. The camera employs a CMOS detector of 2048 by 2048 pixels with a standard 5.5-micrometer pixel size and a 12 bits digital data quantization. After downloaded from satellite, the RAW data will be processed to be implemented some radiometric correction and enhancement [3].

The second of digital payloads is Automatic Identification System (AIS). AIS Systems is a developed technology to detect and monitor the activities of cruise ships in certain areas [4]. AIS is
used by sea vessels that sends and receives VHF messages containing identification, position, course and speed information to allow the monitoring of vessel movements and collision avoidance as well as alerting in the event of sudden speed changes. On LAPAN-A2, this device will monitor ships along near equatorial orbit since it orbiting the earth. Since AIS receiver was mounted into spaceborne or satellite, it would give an advantage of broad coverage area.

Those of the digital payloads data will be transmitted using 3 Mbps via S band transmitter [5]. All Payload system of LAPAN-A2 satellite is described in figure 1. Therefore, to handling this mission of payload data LAPAN A2 satellite needs some hardware for receiving digital payload data of LAPAN-A2 Satellite.

Figure 1. Payload system of LAPAN-A2 satellite [6].

This research aims to describe hardware design and implementation of digital payload data receiver of LAPAN-A2 satellite. The hardware uses development module of Morph-IC Field Programmable Gate Array (FPGA), and microcontroller AVR ATmega 128 IC, both IC will be combined with another module such as bit synchronize, sub carrier, and demodulator.

FPGA is suitable for fast implementation controller and can be programmed to do any type of digital functions. A FPGA has an ability to operate faster than a microprocessor chip. Because of the flexibility of the FPGA, the additional functionality and user interface control can be incorporated into the FPGA minimizing the requirement for additional external components [7]. FPGAs are programmed using Very High Speed Integrated Circuit Hardware Description Language (VHDL) and a download cable which is connected to a host computer. Once they are programmed, they can be disconnected from the computer, and it will be running as stand-alone device. The FPGAs can be programmed while they run, because they can be reprogrammed in the order of microseconds. This short time means that the system will not even sense that the chip was reprogrammed [8]. Applications of FPGA’s include industrial motor drivers, real time systems, digital signal processing, aerospace and defense systems, medical imaging, computer vision, speech recognition, cryptography, computer hardware emulation and a growing range of other areas.

The Atmel AVR ATMega128 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATMega128 achieves throughputs approaching 1MIPS per MHz allowing the system designer to optimize power consumption versus processing speed. The ATMega128 device is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits [9].

2. Methodology

Methods used in this paper to achieve hardware design and implementation of digital payload data receiver of LAPAN-A2 satellite are described as flowchart in figure 2. First step is observation, the observation collects information about output of transmitter S-band formatter, and it is done in laboratory. The next step is design, the design assigns main component which used for digital payload data receiver based result of observation. The next step is implementation, the realization of a design digital payload data receiver using Quartus for programmable FPGA, and Basic Compiler language for
microcontroller ATmega 128 IC, and manufacture PCB (Printed Circuit Board) using Eagle software. Last step is testing and analysis, it is used for checking every system whether is done.

![Methodology flowchart](image)

**Figure 2.** Methodology flowchart.

3. Result and discussion

3.1. Observation
The purpose of this observation is to know characteristics of the data format sent from the transmitter to assist in the design of module ingest data of LAPAN-A2 satellite. First step of observation is preparing spacecam module which is integrated with S-Band transmitter module, S-band antenna, PDH, PCDH and power supply. Second step, sets up a LAPAN-A2 payload receiver module includes S-band receiver module, bit sync module and S-band antenna. Last step is setting up ingest data 3Mbps module. In the observation, there are several alternative steps to find the first sequence of bits. Characteristics of Spacecam data transmitted as follows:
- The first sequence of bits sent from a byte of data is bit 0 continue to bit 1 until bit 7,
- Keyword or header for one package of space camera data is 00-11-22-33 (example),
- Footer for one space camera packet data is 00-11 (example),
- If there is no data from payload, Payload Data Handling will send the dummy data package consisting of 4 byte,
- The number of data in one packet transmitted is inconsistent at 4098 bytes, and
- In one data packet there can be some dummy byte packets whose positions are random.

3.2. Hardware design
The detail of hardware design and implementation process of digital payload data receiver of LAPAN-A2 satellite is shown in figure 3 below.

![System of digital payload data receiver](image)

**Figure 3.** System of digital payload data receiver of LAPAN-A2 satellite.
All systems in hardware digital payload data receiver of LAPAN-A2 satellite is connected with other hardware. The hardware is used for S-Band receiver consists of S-band antenna, video analogue receiver, radio frequency system (RF System), sub carrier demodulator, bit synch is used to make sure that the signals sent from one transmitter of the communication of LAPAN-A2 Satellite could be rightly decoded by the receiver, and the last ingest data using FPGA and microcontroller. FPGA module should be able produce clock and speed is around 3Mbps, and microcontroller should be give the command to select digital payload data between space camera and AIS by serial communication with personal computer (PC).

3.2.1. Morph ıc FPGA
The implementation of this project uses FPGA morph IC. It is needed for high speed application. We proposed three main schematics in Quartus software. First, we make schematic using FIFO. Most FIFO designs require free-running clocks, which the write or read operation is controlled by the respective clock enable. A typical FIFO has a DATA IN bus, a DATA OUT bus, a free-running write clock with its Enable control, and a free-running read clock with its Enable control. The data width of the FIFO must accommodate the application but the exact depth is irrelevant, as long as it is deep enough. The user never sees the unused locations. A FIFO is very easy to use, since it hides all functional and timing complexity from the user. The FIFO block has function as a bridge different speed, the data before using FIFO is synchronous with speed 3Mbps, and the data out from FIFO is asynchronous with speed 6Mbps. Figure 4 below shows schematic FIFO using Quartus software Altera.

![Figure 4](image)

**Figure 4.** Implementation of FIFO schematic Morph-IC.

Next step is making comparator schematic. This schematic is using a phase-locked loop (PLL). PLL is a closed loop frequency control system based on the phase difference between the input clock signal and the feedback clock signal of a controlled oscillator, also using the frequency divider. It is a simple component which objective is to reduce the input frequency. The component is implemented through the using of the scaling factor and a counter. The scaling factor is the relation between the input frequency and the desired output frequency. Overall, figure 5 shows comparator schematic which has functions to search keyword patterns per bit between dummy data and real data, give input to the frame synch schematic to specify the initial bit entry, and give signing via led if there is a dummy or keyword detected.

![Figure 5](image)

**Figure 5.** Implementation of comparator schematic.
The last schematic is controller of the microcontroller ATMega 128. This schematic is used for sending or setting keyword and dummy keyword data in parallel 8 bit and some bits control to manage data traffic, also to input keywords or read keywords and to read clock frequency which has been received. Figure 6 shows the detail of schematic control of the microcontroller.

**Figure 6.** Implementation of control of the microcontroller.

Between pin of the morphic FPGA must be connected with pin microcontroller ATMega 128. The pins of the FPGA module with microcontroller is presented in table 1.

| No | ATmega128 | Morph-IC | No | ATmega128 | Morph-IC | No | ATmega128 | Morph-IC | No | ATmega128 | Morph-IC |
|----|-----------|----------|----|-----------|----------|----|-----------|----------|----|-----------|----------|
| 1  | Yellow LED| F16      | 6  | PC1       | P16      | 11 | PC6       | L12      | 16 | PA3       | T14      |
| 2  | Green LED | L15      | 7  | PC2       | R14      | 12 | PC7       | N11      | 17 | PA4       | T13      |
| 3  | Input Data| L16      | 8  | PC3       | R13      | 13 | PA0       | M14      | 18 | PA5       | T10      |
| 4  | Input Clock| K16     | 9  | PC4       | R11      | 14 | PA1       | P15      | 19 | PA6       | T9       |
| 5  | PC0       | N16      | 10 | PC5       | R9       | 15 | PA2       | N14      | 20 | PA7       | P13      |

3.2.2. **ATMega 128 development board**

This report uses of ATMega128, which is one of AVR (Advanced Virtual RISC) series of ATmel co. Ltd.. ATMega128 has a processing speed from 16 MHz on average by applying RISC (Reduced Instruction Set Computer) technique which is based on pipeline architecture processing and applying Harvard architecture which independently accesses to program memory and internal data memory with high speed 8 bits Micro-controller [9]. It also has an advantage of convenient development environment coming from ISP (In System Programming) method which combines program cord use flash memory with a chip where user programs are downloaded [10]. ATMega128 is well known to be suitable for manufacturing small and midsize industrial controllers. In particular, it is able to transmit and receive monitoring or control instruction because it has USART (Universal Synchronous and Asynchronous serial Receiver and Transmitter) serial communication port which retains following functions; 8 channel 10 bits A/D converter, a couple of 8 bits timer/counter, 16 bits timer/counter, a couple of Full Duplex[11]. The microcontroller embedded is done by Basic Compiler (BASCOM-AVR) language. Figure 7 shows the final design PCB schematic and board layout diagram that we need to implement in hardware, the final design we use EAGLE (Easily Applicable Graphical Layout Editor) software [12][13][14].
3.3. Hardware Implementation

After finishing the design, the next step is integration session. As was described in the first part, we must combine the hardware of digital payload data receiver with another hardware such as, power supply, demodulator, receiver S-band, and bit synch. All hardwares are putting in the one enclosure as shown in figure 8 below. The detailing of figure 8 are:

- Number 1, indicates Ingest module, which consist of microcontroller and morph-IC FPGA module. This hardware is the key of hardware digital payload receiver. This hardware receives trigger such as clock from bit synch then looking the pattern for the keyword of spacecam data or AIS with 3 Mbps speed. Moreover, it can be set and forwarded to serial communication (UART) with speed 6 Mbps so it can communicates with PC and the data can be saved in PC.
- Number 2, indicates the Bit Synch. This is used for decoding analog signal become bits, giving trigger data and clock signal to FPGA module [15]. It must reconstruct its input data stream and recover the clock with the highest fidelity to allow the processing system to produce meaningful information.
- Number 3, indicates S-band receiver. It is used for receptioning in the S-band frequency band, with frequency 2220 MHz and receiving analog video data from satellite.
- Number 4, indicates Sub-Carrier Demodulator. It operates at a subcarrier frequency of 6.2 MHz. The demodulator accepts the composite baseband output from the video receiver.
- Number 5, power supply. In this project, we used the switching power supply to minimize the noise does come with some drawback, slower responses and more sensitive to reverse from the load. Almost the hardware of digital payload data receiver of LAPAN-A2 is using 12V.

Figure 7. Implementation of board and schematic.

Figure 8. Implementation of digital payload receiver of LAPAN-A2.
3.4. Testing And Analysis The Hardware of Digital Payload Data Receiver

There are several tests to verify the functionality and performance of hardware digital payload data receiver. First test was module functionality test using electronic instrumentation ie. oscilloscope. The second was testing the hardware of digital payload data receiver between simulator transmitter S-band satellite, and download data digital payload via LAPAN-A2 satellite.

3.4.1. Testing Using Instrumentation

The test was done using oscilloscope. It is used to display and analyze the waveform of electronic signals. The result shows a signal from simulator S-band transmitter capability to pass by the frequency clock 2.9070 Mhz and speed rate around 3.030 Mbps. So that, the hardware was implemented using morphic-IC and microcontroller ATmega128 can be applied because the test results show the value among observation that was first conducted in this research. Figure 9 shows the test result using the oscilloscope from left side (a) is clock and right side (b) is speed rate.

![Oscilloscope Results](image)

**(a)**

**(b)**

**Figure 9.** The test result using the oscilloscope: (a) clock testing 3 Mbps, (b) speed testing 3 Mbps.

3.4.2. Test via LAPAN-A2 satellite

After testing by oscilloscope. Next test is direct test between simulator transmitter S-band with hardware of digital payload data receiver. The test is done in ground segment Satellite Technology Centre LAPAN. The hardware will upload the program in format RBF file. After that, the microcontroller will give a trigger a keyword in by Docklight software via FTDI-RS 232 communication. During the end to end test, the selected key parameters are the device is Morph-IC, baud rate speed is 6Mbps and select com port for communication. The result of this test is output data from simulator S-band is raw data in Hex. We can see in figure 10, the output data is sequence byte data from 00 01 02 03 until FF.
After finishing direct test using simulator S-band, the last test is by utilizing LAPAN-A2 satellite. This test was done in 24 March 2018 in Rancabungur Bogor ground station. LAPAN-A2 satellite will sends the digital data payload to the ground station via S-band transmitter satellite, and then the person who was in charge / satellite operators at acquisition of LAPAN-A2 satellite will prepare everything such as software and hardware that was implemented of digital payload data receiver. The next, satellite operator must select the data to be derived from LAPAN-A2 satellite as digital camera or AIS data. After that, turn on the S-band transmitter satellite, the signal will be received by antenna and RF next the hardware will be locked the signal, the incoming data first is dummy and if the keyword match continue with space camera or AIS data. The process of download data of LAPAN-A2 to the ground station is estimated 10 minutes, and the amount of data received is depends on the height of elevation and attitude of satellite. The total data was downloaded in Rancabungur Bogor ground station can be seen in figure 11 below, for this case AIS data is arround 293 MB and space camera is around 102 MB.
4. Conclusion
The hardware design and implementation of digital payload data receiver of LAPAN-A2 Satellite is made for supporting acquisition of digital payload data of LAPAN-A2 satellite. From the results and discussion chapter seen functionally test of hardware payload data receiver system getting enough results. The hardware using Morph-IC and microcontroller ATMega128 has been successfully designed and implemented to be digital payload data receiver of LAPAN-A2 satellite. From design and implementation, we get the hardware is capable to pass the clock and speed signal around 3Mbps from S-band transmitter of LAPAN-A2 satellite, and forwarded through serial communication to PC with 6 Mbps. The hardware was tested to download of digital payload, for AIS data is around 200 MB and space camera data is around 100-150 MB. The total of downloaded data from LAPAN-A2 satellite to Ground Station depends on the height of altitude and the attitude of the satellite. The hardware was installed in Rancabungur ground station to facilitate download data digital from LAPAN-A2 satellite.

Future works of this project is the software acquisition of digital payload data will be automatically downloaded, because the process will be planned 24 hours continuously, and also to reduce noise interference in S-band frequency (2220Mhz) will be made Band Pass Filter (BPF).

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