Design and implementation of multi-channel moving target radar signal simulator

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Abstract: The development of radar signal simulator in specific environment can effectively accelerate the debugging process of radar system and reduce the consumption of human, material, and financial resources. This study analyses the mathematical model of the IF radar signal in aerial distributed semi-active radar system and deduces the parameters of radar signals based on direct digital synthesiser (DDS) technology. After solving the problem of multi-channel synchronisation, delay precision control, and envelope delay compensation, an IF radar signal simulator system was designed and implemented, which can generate three direct-path-wave signals and three echo signals.

1 Introduction
It can effectively accelerate the debugging process of radar system by developing the radar signal simulator.

The simulation scenario in this paper is the aerial distributed semi-active radar system. In aerial distributed semi-active radar systems, the signals emitted by ground wide-beam radar are simultaneously illuminated to targets and multiple distributed radar receivers in the air. The radar receiver receives the direct-path-wave directly irradiated by the radar transmitter and the reflected wave (also called echo) reflected by the target. The signal processing unit completes the Doppler frequency tracking and distance information extraction by performing down-conversion, analogue-to-digital conversion, and matched filter processing on the received signal, and searches and tracks the moving target. Multiple receivers work on the same principle and work together, one serves as master and others serve as slaves, so as to achieve accurate search and tracking of moving targets. The simulator designed in this paper takes three receivers as an example to simulate the generation of three-channel intermediate frequency (IF) direct-path-wave and three-channel IF echo.

For the generation of radar signal, this paper adopts the scheme to implement DDS technology in FPGA. FPGA transmits the phase data of waveform to the high-speed DA chip, and the DA chip outputs analogue waveforms.

In this paper, a multi-channel moving target radar signal simulator is designed and implemented. In the second section, the mathematical model of IF direct-path-wave and IF echo in airborne semi-active radar system is analysed in detail and the waveform generation parameters based on DDS technology are deduced. In the third section, the design scheme of radar signal simulator system is introduced. The multi-channel synchronisation, delay precision control, and phase compensation of envelope delay are discussed, and the feasible solution is put forward. Finally, both the implemented hardware of simulator and the waveform generation results of this simulator are displayed.

2 Radar system and signal model
The ground radar in this system is a pulsed Doppler (PD) radar. PD radar transmits pulse-modulated signal and uses the Doppler effect generated by the relative motion between the target and the radar to extract and process the target information [1,2]. PD radar that adopts the linear frequency modulation (LFM) signal can not only conduct the process of moving target identification (MTI), but also be featured with long detection range and high resolution of range and velocity.

PD radar that equipped with LFM signal transmits coherent LFM pulse train. The signal discussed in this paper is narrow-band signal.

2.1 Radar transmit signal
Let \( t_m \) represent the slow time and \( \dot{t} \) represent the fast time. The slow time indicates the moment of emitting and can be expressed as \( t_m = (m-1)T_p \), \( (m = 1, 2, \ldots) \), where \( T_p \) is the pulse repetition interval. The relationship between \( t_m, t \) and the full time \( t \) is \( t = t - t_m \).

The \( n^{th} \) LFM pulse signal transmitted by the radar can be expressed as:

\[
S(\dot{t}, t_m) = \text{rect}\left(\frac{\dot{t}}{T}\right) \exp\left(j2\pi f_c t + j\pi \mu t^2\right)
\]  

where

\[
\text{rect}(t) = \begin{cases} 1 & \frac{-1}{2} \leq t \leq \frac{1}{2} \\ 0 & \text{otherwise} \end{cases}
\]

is rectangle function, \( T \) is the pulse width, \( f_c \) is the carrier frequency, and \( \mu \) is the LFM modulation index.

2.2 Direct-Path-Wave channel signal
It is assumed that the radar receiver is moving at a uniform speed and the relative velocity with the ground radar is \( V_m \) (Set away from the ground radar to positive direction). The initial radial distance between the radar receiver and the ground radar is \( R_{0M} \). At the moment \( t \), the distance between ground radar and radar receiver is \( R_{0M}(t) = R_{0M} + V_m t \). Then, the received direct-path-wave is:

\[
S_{\text{dp}}(\dot{t}, t_m) = \text{rect}\left(\frac{\dot{t} - R_{0M}(t)}{T_p}\right) \times \exp\left[j2\pi f_c (\dot{t} - R_{0M}(t))/C\right]
\]  

where \( \tau_d(t) = R_{0M}(t)/C \) is the delay of direct-path-wave and \( f_m = f_c V_m/C \) indicates the Doppler frequency caused by the motion of the radar receiver.
where $K_0$ is the initial frequency control word, $K_i$ is the frequency control word step (frequency modulation slope control word), and $P_0$ is the initial phase word.

Taking the IF direct-path-wave as an example. The starting point of each direct-path-wave is $\tau_d(t_0) = (m-1)\tau_p$. After performing coordinate transformation according to $i = t - t_0$ (3) can be expressed as:

$$S_d(i, t_0) = \text{rect}(\frac{i - \tau_d(t_0)}{\tau_p}) \times \exp[j \pi f_i(i - \tau_d(t_0))^2] \times \exp[j 2\pi f_c f_s(i - t_0)]$$

Then the echo phase decomposition model is:

$$\Phi(i) = 2\pi f_c [H_d^2 + H_s^2 + H_j]$$

3 Design of radar signal simulator

To implement the multi-channel moving target radar signal simulator, some key factors should be considered, such as the multi-channel synchronisation, delay precision control, and phase compensation of envelope delay.

3.1 Multi-Channel synchronous design

In the aerial distributed semi-active radar system, distributed radar receivers work together to improve the accuracy of distance measurement and speed measurement. Synchronisation between receivers is required, that is, the synchronisation between the direct-path-wave and the echo. Therefore, signal synchronisation between channels is an important part in the design of the multi-channel signal simulator.

In order to meet the needs of multi-channel signal synchronisation, DA chip selected ADI's AD9739. AD9739 is a 14-bit, 2.5GSPS high-performance RF DAC and supports multi-chip synchronisation operation [4]. Setting the chip in master mode or slave mode by configuring internal registers, and synchronising data among multiple AD9739 chips through synchronous output interface and synchronous input interface can realise the synchronous function.

In addition, the AD9739 work clock also needs to meet the high-frequency stability requirements. Therefore, the system selects the constant temperature crystal oscillator (10 MHz) with the frequency stability of 0.01 ppm and the clock multiplier chip selects the HMC832A. The HMC832A is a high-performance, wideband, divide-by-N, integrated VCO phase-locked loop chip that generates continuous frequencies from 25 MHz to 3000 MHz [5]. Industry leading phase noise and spurious performance, across all frequencies, enable the HMC832A to minimise blocker effects, and to improve receiver sensitivity and transmitter spectral purity.

The final multi-channel synchronous design is shown in Fig. 1. The detailed requirements to achieve multi-chip AD9739 chip synchronisation are as follows: in the hardware design to achieve the following equal length: clock buffer supply 6 AD9739 clock lines to all equal length; FPGA and AD9739 between the clock synchronisation pin DCO and DCl need to be equal length; clock buffer supply AD9739 synchronous clock lines need to all the same length.

$\Phi(n) = \frac{2\pi}{N} \left[ K_i n^2 + \left( K_n - \frac{K_i}{2} \right) n + P_0 \right]$
3.2 Delay precision control and Multiplex parallel processing method

The accuracy of the generated waveform data and the stability of the output signal are the key factors that affect the actual performance of the radar processor. In the design, the main considerations are the initial phase precision of the direct-path-wave and the echo, the envelope delay, as well as the additional Doppler modulation frequency requirements.

In practice, due to the limitation of FPGA devices, it is necessary to adopt the method of multiplex parallel processing to obtain high precision delay and phase requirements (Fig. 2).

Specific operations are as follows: First, get the waveform data, whose sampling rate is 1.6 GHz, then split it into eight channels, each channel down to 200 MHz data stream. Second, make these eight channels data divided into even channels and odd channels according to section 2.4 derivation of the phase-parameters of the mathematical relationship. Third, make the four odd channels data synthesised to one channel data by parallel-serial conversion, so as to the four even channels data. The data rate of the two synthesised channel is 800 MHz. Finally, output the two synthesised channels data to the DA chip which generates waveform with 1.6 GHz data rate.

For the data precision of signal, the time interval resolution of 1.6 GHz sampled data is 0.625 ns, so the precision delay of signal and the control of initial phase of signal can be realised.

\[
\Phi_n(n) = \Phi(8m + i) = \frac{2\pi}{2N} K_0 (8m + i)^2 + \left( K_0 - \frac{K_1}{2} \right) (8m + i) + P_0,
\]

where

\[
K_0 = 8K_0 + (81 + 28)K_1,
\]

\[
P_0 = P_0 + iK_0 + (i - 1)K_1/2
\]

3.3 Phase compensation analysis of envelope delay

Taking the direct-path-wave as an example, the envelope delay control is rect \( \frac{t - R(t)/C}{T_p} \) [7, 8]. Suppose the clock frequency of the FPGA is \( F_s \), and sampling period is \( T_s \). The number of delay clocks per pulse implemented in the FPGA is:

\[
N_m = \left( R_m + V_m (m - 1) \right) T_p / T_s (m = 1, 2, \ldots)
\]

where symbol \([ * ]\) represents a roundness operation. The number of delay clocks is the whole relation of FPGA working clock cycle. If \( F_s \) is 200 MHz, the sampling period is 5 ns. In order to improve the precision of envelope delay and eliminate the phase problem caused by the pulse delay control unit, the delay control unit can be kept unchanged and compensated in the initial phase of the output signal. As shown in Fig. 3, the working clock \( F_s \) is used to drive the output signal. The output signal is behind the initial phase of the actual sampled signal. In order to compensate for this defect, the initial phase is adjusted according to the output starting time. As shown in Fig. 3, the compensated sampling signal is desired.

4 Hardware and experiment results

Based on the scheme design of the simulator mentioned above, the hardware board has been made as shown in the figure below (Fig. 4).

After the FPGA program design completed, different waveforms can be generated by setting different waveform parameters. One example is show in Fig. 5. As per the limit to the number of oscilloscope channels, there are four waves displayed. The first two waves represent direct-path-wave and the others represent echo. From the diagram, the delay control between these channels is demonstrated.

5 Conclusion

In this paper, the mathematical model of the radar signal in aerial distributed semi-active radar system is analysed and a multi-channel moving target radar signal simulator is designed and
implemented. This simulator could be capable of generating three-channel direct-path-wave signals and three-channel echo signals. The delay between these channels could be changed by setting waveform parameters, which meet the requirement of the radar signal simulator.

6 References

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Fig. 5 Waveform generated by simulator