NxTF: An API and Compiler for Deep Spiking Neural Networks on Intel Loihi

BODO RUECKAUER, Institute of Neuroinformatics, University of Zurich and ETH Zurich, Switzerland
CONNOR BYBEE, Redwood Center for Theoretical Neuroscience, University of California, Berkeley, USA
RALF GOETTSCHE, Intel Corporation, Germany
YASHWARDHAN SINGH, JOYESH MISHRA, and ANDREAS WILD, Intel Corporation, USA

Spiking Neural Networks (SNNs) are a promising paradigm for efficient event-driven processing of spatio-temporally sparse data streams. SNNs have inspired the design and can take advantage of the emerging class of neuromorphic processors like Intel Loihi. These novel hardware architectures expose a variety of constraints that affect firmware, compiler and algorithm development alike. To enable rapid and flexible development of SNN algorithms on Loihi, we developed NxTF: a programming interface derived from Keras and compiler optimized for mapping deep convolutional SNNs to the multi-core Intel Loihi architecture. We evaluate NxTF on Deep Neural Networks (DNNs) trained directly on spikes as well as models converted from traditional DNNs, processing both sparse event-based and dense frame-based data sets. Further, we assess the effectiveness of the compiler to distribute models across a large number of cores and to compress models by exploiting Loihi’s weight sharing features. Finally, we evaluate model accuracy, energy and time to solution compared to other architectures. The compiler achieves near optimal resource utilization of 80% across 16 Loihi chips for a 28-layer, 4M parameter MobileNet model with input size 128 × 128. In addition, we report the lowest error rate of 8.52% for the CIFAR-10 dataset on neuromorphic hardware, using an off-the-shelf MobileNet.

CCS Concepts:
• Hardware → Neural systems; Analysis and design of emerging devices and systems;
• Computer systems organization → Multicore architectures; Neural networks;
• Theory of computation → Machine learning theory;
• Computing methodologies → Neural networks.

Additional Key Words and Phrases: spiking neural network, deep neural network, neuromorphic, compiler

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1 INTRODUCTION

The widespread success of Deep Learning (DL) has been accompanied by the development of user-friendly frameworks like Keras [7] and PyTorch [27] that ease the development and mapping of large scale machine learning models to state of the art DL hardware. Still, training and running DNNs on conventional hardware is often costly in terms of time and...
energy consumption. This realization has driven research to develop more efficient algorithms (e.g. [4]) and dedicated hardware (e.g. [30]).

SNNs form a particular class of such algorithms that draw inspiration from the brain by transmitting information asynchronously in form of discrete spikes. Neuromorphic platforms like SpiNNaker [17], TrueNorth [23], and Loihi [10] are optimized for this kind of event-based computation and have demonstrated the potential to run neural networks at much lower latency and energy consumption [11, 15, 38] than traditional Central Processing Units (CPUs) or Graphics Processing Units (GPUs) based computer architectures.

However, none of the current mainstream DL software frameworks support these neuromorphic architectures for the purposes of DL applications. Instead, the available neuromorphic software frameworks often expose the user to some of the complexities and constraints of these novel hardware architectures, therefore rendering them less accessible to end-users not familiar with neuromorphic technologies. There are several software frameworks for programming neuromorphic systems today. For instance, Nengo [3] is a cross-platform tool suite to train, simulate and map SNNs to different neuromorphic hardware platforms. PyNN [8] is a simulator-independent programming language for neural networks that supports running the models on SpiNNaker and BrainScaleS [35]. In addition, each neuromorphic platform usually comes with its own set of programming abstractions, compiler, and firmware like Spynnaker [31], SpiNNTools [32], TrueNorth Corelets [1] or Intel’s NxSDK for the Loihi architecture.

Intel’s NxSDK (see Fig. 1) supports different high-level Application Programming Interfaces (APIs), each intended for different use cases, including the third-party API Nengo and Intel’s own APIs NxNet as well as the new NxTF framework introduced here. All interfaces provide their own compiler to map a neural network definition to the lower-level NxCore API that allows to configure a system of Loihi chips at the register level. NxNet provides full access to all computational features offered by Loihi. It allows to define neural networks at a structural level of individual cells or populations of neurons connected via axons and synapses that might be subject to synaptic learning rules. In contrast, NxTF trades generality for an application focus towards deep SNNs. This objective is achieved by inheriting from the Keras Model and Layer interface and providing a specialized DNN compiler. To compress large DNNs on Loihi, this compiler exploits the regular structure of typical DNN topologies like Convolutional Neural Networks (CNNs) in combination with Loihi’s ability to share connectivity state. The NxTF source code is publicly available online\(^1\).

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\(^1\)https://github.com/intel-nrc-ecosystem/models/tree/master/nxsdk_modules_ncl/dnn

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Fig. 1. NxSDK software stack and workflow to configure a deep SNN on Loihi. Starting from a trained or converted SNN, the user defines a model in Python using the Keras-derived NxTF interface. The network is then partitioned and mapped onto Loihi by the DNN compiler via the register-level NxCore API. The NxDriver and NxRuntime components are responsible for interaction and execution of the SNN on Loihi.

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We begin this paper by outlining the typical workflow of using the proposed NxTF framework to deploy a DNN on Loihi in Sec. 2.1. After reviewing the necessary background about the Loihi architecture in Sec. 2.2, we explain the network compilation procedure in Sec. 2.3. To evaluate the effectiveness of the compiler, we measure the memory utilization when deploying architectures of different structure and size on Loihi (Sec. 3.1.1). Low memory utilization is essential on a non-Von-Neumann architecture like Loihi, where multiple smaller blocks of memory are distributed locally close to the computation. We also study how well NxTF is able to exploit Loihi’s ability to share synapses and axons when compiling convolution layers in order to compress redundant connectivity information (Sec. 3.1.2). In terms of applications, we present two common use cases of NxTF in Sec. 3.2: Deploying an SNN on Loihi that a) has been trained directly on a spike-based dataset using SLAYER [36], and b) that has been converted from an Artificial Neural Network (ANN) trained on frames. Finally, we benchmark the performance of these networks and compare their energy consumption and execution time against results on other neuromorphic hardware.

2 METHODS

As our core contribution, we present here a user interface and compiler for DNNs on Loihi, called NxTF. In the design of this compiler, we followed two objectives: (1) To provide an easy-to-use tool that adopts Keras’ level of abstraction. (2) To optimize the allocation of resources on the neurocores and exploit Loihi’s connection sharing features for efficient deployment of large-scale CNNs. With regard to the first objective, we will first provide a high-level overview of the tool chain in Sec. 2.1. We then introduce basic concepts of the Loihi hardware architecture to understand resource constraints and opportunities for resource sharing taken into account by the compiler. With this background we can then dive more deeply into the compilation method in Sec. 2.3 to show how we solve the second objective.

2.1 Overview of Workflow

The two-step workflow to deploy a DNN on Loihi using the NxTF interface is outlined in Fig. 1. In the first step, the user trains or converts an SNN, for instance using a third-party tool like Nengo [3], SLAYER [36], or the SNN toolbox (SNN TB) [34]. The expected output of this step is a set of learned weights for each layer, the layer specifications defining e.g. the padding and stride of convolutions, and the desired neuron properties (like voltage decay and threshold value).

Given this information, the user can then define a network in Python using the NxTF interface (red box in Fig. 1). This interface is derived from Keras and follows the same syntax for setting up a Keras model, except that additional arguments are required for Loihi-specific settings.
Loihi arguments (for threshold, time constants etc.) are supported. See Fig. 2 for a minimal code sample. The result at this stage is an instance of NxModel, which inherits all functionality of its Keras base class.

To prepare the NxModel for deployment on Loihi, the user then calls the compile method, which consists of two parts: A partitioner and a mapper. The objective of the partitioner is to find the optimal distribution of the network across neurocores, whereas the mapper is responsible for bit-level configuration of Loihi registers.

Once the mapping is complete, the user is able to run the model and retrieve the output for evaluation. A detailed tutorial covering these steps is provided within the Intel Neuromorphic Research Community (INRC) framework. In Sec. 3, we apply this pipeline on models trained directly on spike-based datasets as well as on models converted from frame-based ANNs. But before going to the results we will take a closer look at the Loihi hardware and NxTF compiler.

2.2 Loihi

2.2.1 Architecture Overview. Intel’s Loihi research chip is an asynchronous, compute-in-memory neuromorphic processor optimized for the execution of Spiking Neural Networks. Fabricated in Intel’s standard 14 nm CMOS process, Loihi consists of 128 neurocores, each of which supports up to 1024 neurons. Three embedded x86 processors per chip enable off-chip data encoding and interaction with the neurocores. Loihi’s asynchronous network-on-chip communication infrastructure allows it to be seamlessly scaled up to various form factors, ranging from 2-chip USB device Kapoho Bay to the 768-chip rack Pohoi Springs.

Spiking neurons on Loihi are stateful dynamical systems that support a wide range of features. These include synaptic plasticity, variable numeric precision of synaptic weights up to 9 bits, multi-compartment models, threshold adaptation for homeostasis, and configurable synaptic, axon and refractory time constants. To support hierarchical and repeated connectivity as in CNNs, Loihi provides a connection-sharing mechanism (described in more detail in Sec. 2.3).

The dynamical equations that underlie the Loihi neuron model are approximated in discrete time. Unlike in conventional synchronous architectures, the transition between algorithmic time steps is not driven by a fixed global clock but mediated through a barrier synchronization protocol between all participating neurocores. As part of this protocol, neurocores signal the completion of the workload for the current time step to their neighbors, resulting in a workload-dependent duration of each time step. Neuron updates contribute on the order of microseconds to the duration of each time step. Spike traffic typically dominates the overall time step duration. Hence, spatially and temporally sparsely communicating SNNs promise the greatest level of efficiency on such architectures.

2.2.2 Information Flow in Loihi Cores. In order to understand how the compiler utilizes Loihi’s resource sharing features to efficiently compress CNNs, we will briefly review the logical entities within a neurocore (c.f. left column of Fig. 3). The central building blocks are compartments, which may form single- or multi-compartment neurons. For simplicity we will use the term “neuron” in this section to denote a single compartment. A neuron accumulates spikes and eventually generates a spike itself once its membrane voltage exceeds a threshold. Spikes are routed from a neuron to their destination via axons. In our compiler, we distinguish between output and input axons. An output axon is responsible for core-to-core connectivity; it routes spikes to a corresponding input axon on the same or another core. The input axon references a list of synapses, which connect the axon to its destination neurons. Spikes travelling through the axon are weighted by the respective synaptic strength before accumulation on the neuron’s membrane.

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2 https://github.com/intel-nrc-ecosystem/models, accessed January 13, 2021
3 A two-compartment neuron will be introduced in Sec. 2.3.6.
potential. While this level of abstraction is sufficient for the purpose of the present work, a more detailed description can be found in [21].

Table 1. Rough estimate of resource constraints on a Loihi chip.

| Resource      | Availability | Assumptions                  |
|---------------|--------------|------------------------------|
| Cores         | 128 / chip   | -                            |
| Neurons       | 1024 / core  | Single compartment           |
| Input axons   | 4096 / core  | No off-chip axons            |
| Output axons  | 4096 / core  | No off-chip axons            |
| Synapses      | 128k / core  | 8 bit weights; depends on compression |

The quantity of these entities (neurons, axons, synapses) on a given neurocore is limited by the SRAM memory resources in each neurocore (c.f. Table 1). Fortunately, Loihi provides a way to share axonal and synaptic resources to efficiently compress highly redundant convolutional connectivity patterns (Fig. 3 right).

In particular, all neurons in a source population of neurons (dashed box in Fig. 3) may share one output axon to connect to a shared input axon instead of consuming discrete axonal resources for every neuron in the population. Similarly, these special shared input axons, may reference a shared set of synapses (A, B, C, D) rather than redundant copies of those synapses. Exploiting this resource sharing while adhering to core constraints is the aim of the NxTF compiler, which we address next.

2.3 Compilation Method

Given a network with certain topology, the purpose of the compiler is to find a distribution of neurons across multiple neurocores that makes optimal use of the available chip resources. Due to the layer-to-layer connectivity, the resource requirements of a layer depend on the way the subsequent layer is distributed across neurocores. Therefore layers...
cannot be partitioned independently of each other. On the other hand, partitioning all layers simultaneously is unfeasible because the combinatorial space of possible partitions is large.

Instead, we opt for a greedy two-layer-wise optimization, which will be explained in Sec. 2.3.3. To quantify the degree of optimality, we define a cost function (Sec. 2.3.4) that takes into account hard constraints (e.g., number of available neurons per core) as well as soft constraints (e.g., the total number of cores used). To understand the terms contributing to the total cost, we need to compare opportunities for resource sharing in DNNs and on Loihi (Sections 2.3.1 and 2.3.2).

2.3.1 Connection Sharing. Deep Neural Networks are characterized by a regular connectivity and repeated architectural patterns. This fact can be exploited to develop a compiler optimized specifically for DL applications. Commonly seen convolution layers are particularly advantageous because of their efficient use of trainable parameters. For a given layer, a single set of weight kernels is re-used at every spatial location of the feature map. Fig. 4 illustrates this connectivity pattern within a CNN and defines basic terminology used throughout this section.

NXTF flattens all layers to a 1D topology on Loihi, so we introduce another way of inspecting the CNN structure in Fig. 5. For clarity we consider only the spatial ($x, y$) dimensions of a feature map, neglecting the channel ($z$) dimension. The graphic illustrates the implied connectivity matrix resulting from the convolutional connection from the input layer (yellow) to the output layer (blue) with the layers flattened to 1D. This Toeplitz matrix is well known in the context of unrolling convolutions as matrix-vector product [6]. Layers and kernels are color-coded by neuron and weight index, respectively. The two green boxes (labeled A, B) show two applications of the kernel at different locations of the feature map.

With this perspective of the connectivity matrix at hand, we can compare weight sharing in a CNN on general-purpose hardware against weight sharing on Loihi (Fig. 6). Panel 6a shows that, in a CNN, we would ideally store the kernel only once, and re-use it when iterating over the output neurons (rows). However, in Loihi, weight look-up can only be triggered by the arrival of input spikes resulting in a column-major representation of the connectivity matrix. Hence, as described in Fig. 3, the synapses referenced by input axons form the non-zero entries in each column of Fig. 6b. Such a column vector does not appear with the same regularity as a row vector.

Although Loihi does not support the minimal row-major representation of a convolutional kernel, the axon and synapse sharing mechanism described in Fig. 3 still allows to exploit regularities in the column-major representation to efficiently compress large-scale DNNs such as MobileNet architectures as will be shown in Sec. 3.1. The basic principle is illustrated in Fig. 6c. A population of input neurons shares a group of synapses (solid red rectangle), which is stored...
Fig. 5. Unrolled connectivity matrix from an input layer (yellow) to an output layer (blue), via a convolution kernel (green). Boxes labeled A and B illustrate the application of the convolution kernel at two different locations of the feature map.

Fig. 6. Optimal connection sharing in CNNs (6a), without weight re-use (6b), and with NxTF exploiting Loihi’s resource sharing features (6c).

The degree to which we can exploit this connection sharing depends on the particular way that the layer is partitioned across neurocores. Connection sharing is factored into the partitioner’s cost function and thus is subject to the optimization procedure discussed below.

2.3.2 Axon Sharing. Aside from neuron count and synaptic memory, another limited resource per neurocore is the number of core-to-core routing slots, the axons. In Fig. 3 (right panel) we have shown how a population of source neurons (dashed blue box) shares the same axon. Likewise, we can define a population of input neurons in Fig. 6 (right panel), to contain all neurons of the input layer that utilize a particular synapse group (red box). This neuron population may use a single shared axon to send spikes to the output layer, where the spikes will be fanned out according to the synapse group. Without the ability to share axons, the layer would possibly have to be distributed across more cores to satisfy the axon constraint (Table 1).
Axons in NxTF may be shared, except when targeting multiple cores, as in the example on the left. Following the notation of Fig. 5, the green boxes labeled A and B indicate the consecutive application of a convolution kernel. A spike originating from the shaded region of kernel overlap is sent to neurons on different cores in the output layer. Such connections require unique rather than shared axons (right panel).

However, such axon sharing is possible only when spikes are being routed from one core to a single other core. If multiple cores are targeted, a discrete axon for each core is required. Fig. 7 illustrates this case in a convolution layer. The subsequent application of a convolution kernel in two neighboring locations of the input layer defines a region of kernel overlap (shaded box). Neurons within this region send their spikes to two neighboring neurons (A, B) in the output layer. If the layer happens to be partitioned such that neuron A lives in core 0 but neuron B in core 1, the input neurons within the shaded region each need two discrete axons to reach A and B on their separate cores. The input neurons outside the kernel overlap may share their axons as indicated on the right side of Fig. 7. As with connection sharing, the amount of shared axons is included in the cost function and optimization algorithm.

The way layer $L + 1$ is partitioned (blue line denotes core border) effects a duplication of axons in layer $L$ for neurons connecting to multiple cores in layer $L + 1$ (thick yellow line), thus determining the reverse optimization direction.

2.3.3 Optimization procedure. We saw in Fig. 7 that a given partitioning of layer $L$ influences the resource allocation in the next lower (“pre-”) layer $L - 1$, namely the axon count in the depicted case. This circumstance implies that our optimization algorithm needs to traverse the network graph from top to bottom: A given layer can only be partitioned once we know the resource duplication imposed by its post-layer (Fig. 8).

To optimize the distribution of a layer $L$, the partitioner proposes $M$ different partition candidates and computes their cost according to Eq. (1) (Sec. 2.3.4). But since layers cannot be optimized in isolation, the partitioner moves on to layer
Each layer selects $M$ possible partitions (blue) among $M^2$ candidates according to cost function (1).
becomes active only when the soma crosses threshold and issues a spike. The second compartment then inhibits the soma via the recurrent connection with an amount of charge equal to the threshold.

The optional use of this soft reset implementation improves error rate and reduces runtime, at the cost of doubling the number of compartments allocated for the network.

2.3.7 Parameter Normalization. When porting floating-point weights from an ANN to Loihi, two issues need to be considered. First, Loihi expects fixed-point weight, bias and threshold values. Second, previous work has shown that the limited dynamic range of SNNs can lead to saturating or vanishing firing rates unless the network parameters are properly rescaled [13, 34]. The latter only concerns models converted from ANNs, not directly trained SNNs. To address these two points, we briefly summarize a normalization algorithm that ensures that parameters satisfy the hardware requirements, and that neuron activity spans the full dynamic range.

**Integer conversion.** For the weights $W$ of each layer we apply the following steps:

1. Determine the maximum or some high percentile of the weight distribution: $\sigma = \max(W)$.
2. Normalize values in $W$ by $\sigma$.
3. Scale by the highest value allowed for weights, i.e. $\max(-W_{\text{lim}}^-, W_{\text{lim}}^+)$. The weight limits $W_{\text{lim}}^\pm$ depend on the number of bits allocated for the weights.
4. Truncate values to the nearest integer.
5. Clip the resulting weight values to the allowed range $[W_{\text{lim}}^-, W_{\text{lim}}^+]$. Clipping is only necessary if $\sigma$ was computed based on a percentile rather than the max.

Biases can in principle be converted in the same way. A subtle difference arises from the fact that the allowed bit precision differs for weights and biases. If one wishes to fully exploit their individual bit precision, determining the normalization and scaling factors is more involved; details can be found in the implementation.

**Dynamic range.** To obtain the scaling factor for the dynamic range, we iterate over each layer in turn and estimate the expected distribution of net voltage change $\frac{d\nu}{dt} = Wx + b$ to neurons in the layer, using a subset of the training data. To estimate the expected input distribution without having to run the SNN, we build an SNN emulation from a modified copy of the ANN. In this model we perform the same changes to the weights as we would do to the SNN (i.e. integer quantization as outlined above), and mimick the SNN activation function by dividing by the threshold $\tau$, which converts the membrane potential change into a spike rate.

If the maximum (or some high percentile) $\lambda = \max(\frac{d\nu}{dt})$ of the input distribution lies near the voltage threshold $\tau$, then this layer is utilizing the full dynamic range, and no change is required. Conversely, a supra-threshold value $\lambda > \tau$ indicates saturation, because neurons cannot fire more than one spike per time step. Small net inputs $\lambda < \tau$ predict that a large fraction of neurons will have low or possibly vanishing firing rates.

To prevent vanishing or saturating spike rates, the measured scaling factor $\lambda$ is used to scale the weights and biases as described in [34]. Then, the layer parameters are transformed to integers as described above. Finally, these values are decomposed into mantissa and exponent parts as expected by Loihi.

3 RESULTS

Our experimental results focus on two areas: The evaluation of the compiler, and the demonstration of NxTF on standard use cases. To address the first, we characterize the NxTF compiler by comparing the resource utilization on neurocores when mapping different convolutional architectures. Further, we perform a scaling analysis on a 28-layer MobileNet [18]

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to determine the execution time, energy consumption, and the number of cores required to fit networks of increasing size on the hardware. This analysis also reveals how effective the compiler is at exploiting Loihi’s support for weight sharing.

For the second area, we apply the NxTF framework in two common use cases: A) Frame-based ANNs are trained on standard image datasets, converted to SNNs [34], and then evaluated on Loihi. B) SNNs are trained on event-based datasets using SLAYER [36], and are then deployed on Loihi. In addition to reporting the classification error for the tested models, we perform a profiling of power consumption and execution time, and compare against results published for other neuromorphic platforms.

![Utilization of available neurons, synapses, and axons on neurocores in a standard CNN (grey), and in a MobileNet architecture of equivalent size (blue).](image)

Fig. 10. Utilization of available neurons, synapses, and axons on neurocores in a standard CNN (grey), and in a MobileNet architecture of equivalent size (blue).

### 3.1 NxTF Compiler Efficiency

3.1.1 Depthwise Convolutions Maximize Core Utilization. We begin by showing a limitation with the current CNN support on Loihi, and how to avert it. As discussed in Sec. 2.3.2, axons can only be shared when targeting neurons within one core; if the synaptic fan-out spans across core borders (c.f. Fig. 7), neurons use a discrete axon for each destination core. A particularly adverse condition occurs when the target layer is split along the channel dimension: In that case, each neuron in the source layer sends its spikes to at least two separate cores, and axon sharing for that layer is no longer possible. This situation is suboptimal because a core will run out of available axons while using up only few of the other (in particular neuron) resources, resulting in an overall larger number of cores. We illustrate this case in Fig. 10 for a CNN of comparable size to MobileNet. The utilization of core resources is dominated by axons and synapses, while only a small fraction of available neurons are in use.

Depthwise-separable convolutions provide a remedy to this imbalanced core utilization. Because depthwise convolutions operate on each channel separately rather than combining all channels, they reduce the overall synaptic fan-out. In addition, axons do not need to be duplicated even if the layer is split along the channel dimension, because the fan-out does not span the core borders. Such separable convolutions occur in MobileNet architectures [18]. By replacing the convolutions of the vanilla CNN in Fig. 10 with depthwise-separable convolutions, we obtain a core utilization where most of the layers fully exploit the available neurons, in addition to maintaining a high level of axon and synapse.
utilization. Even though the number of neurons in MobileNet is 1.6× larger than in the vanilla CNN, the total number of cores needed for MobileNet is 12.6× smaller because of the efficient resource utilization.

3.1.2 NxTF Approaches CNN-like Weight Sharing on Loihi. In this section we investigate to what extent the NxTF compiler is able to exploit Loihi’s axon and synapse sharing features to implement convolutional architectures efficiently. As real-world workload we take an off-the-shelf MobileNet [18], a common image classification architecture consisting of 28 layers. In a scaling analysis, we increase the input size from $32 \times 32$ to $176 \times 176$, thereby increasing the spatial dimensions of the feature maps and thus the overall model size. Each member of this model family is compiled and mapped to Loihi. With this experiment we address three questions: 1) How does the number of required neurocores scale with the model size? 2) To what extent are the resources on these cores used up? 3) How effectively does the compiler optimize weight re-use – ranging between the worst case (storing all copies of a convolution kernel) and the best case (storing the kernel only once).

![Fig. 11. Scaling behavior of MobileNet. Each triplet of bars represents the compilation result for a given size of MobileNet, when weight sharing is turned off (right), turned on as supported by Loihi (center), and in the hypothetical best case of full weight sharing (left). Bar height denotes the number of cores required to fit each compiled model. Bar shading indicates the amount of resource utilization per core (darker is better). The horizontal lines represent system form factors, ranging from a single Loihi chip to a 32 chip Nahuku board. The models use single-compartment neurons.](image)

Fig. 11 shows the number of cores used by MobileNet while increasing the model size. For a given model size, three bars are shown, corresponding to three repetitions of the compilation phase. The left bar of each triplet corresponds to the hypothetical best case scenario, in which the compiler computes the number of cores needed if each kernel had to be stored only once (Fig. 6a). The right bar of each triplet indicates the worst case, where weight sharing in NxTF is turned off and all kernel duplicates are stored (Fig. 6b). The middle bar shows the amount of resources allocated when weight sharing is turned on, i.e. the NxTF compiler optimizes the layer partitions such as to maximize the amount of synapse re-use in Fig. 6c.

From this comparison, we observe that the optimization for weight sharing as applied by NxTF reduces the number of cores by about 2× on average, compared to when weight sharing is disabled. Furthermore, the partition solution found by the compiler comes close to the best case scenario, using only 13% more cores on average.
Another metric of interest is the core utilization, which we define as the average fraction of neurons used on the neurocores that are allocated by the compiler (gray shading in Fig. 11). This number should be as high as possible to minimize the overall number of cores, which impacts static power and to some degree active energy consumption. With weight sharing enabled, the solution found by the compiler deviates on average only 15% from the hypothetical best case. This analysis demonstrates that despite the lack of dedicated support for convolutional compression, Loihi is able to encode such topologies close to the optimal encoding.

With this use of synapse sharing on Loihi, the compiler is able to fit a MobileNet of input size $152 \times 152$ onto the 32 chip Nahuku32 board at 60% core utilization. The model with $128 \times 128$ input size fits on 16 chips at 80% core utilization. This network consists of 28 layers, 5 M neurons, and 4 M parameters, thus representing a real-world workload for image classification on neuromorphic hardware.

### 3.2 SNN Performance Analysis

In this section, we use the NxTF framework to map directly trained SNNs as well as converted SNNs to Loihi and benchmark these networks on sparse event-based and dense frame-based datasets. Before presenting the results, we describe the methodology used to analyze SNN performance on Loihi.

#### 3.2.1 Methodology

NxSDK allows for the measurement of both execution time per algorithmic time step and power consumption. These metrics allow us to compute the energy and time to solution per inference sample.

Algorithmic time steps in Loihi are further subdivided into sequential spiking, learning, and management phases, which are partially required for deadlock avoidance of the asynchronous mesh [10]. For inference-only DNN workloads, only the spiking and management phase are of interest. During the spiking phase, neurons are updated and spikes are communicated between neurocores. During the management phase, the embedded CPUs may inject new data or read out the current SNN state. When comparing our results to those of other groups, we compute the total execution time per algorithmic time step from the sum of all phases, and multiply by the number of time steps that each sample is run.

The total power consumption can be broken down into static and dynamic components. Static power mainly results from leakage while dynamic power results from active computations performed inside neurocores and embedded CPUs. Active neurocore power arises from memory access and logic operations for updating neurons and transmitting spikes. Active CPU power arises from the clock of the synchronous x86 processors as well as the execution of user code. The power measurement utilities provided by NxSDK always measures the power and energy of the entire system but automatically excludes the part of unused neuro and CPU cores.

A common metric to combine both time and energy to solution is the Energy Delay Product (EDP) [9]. It is computed from the product of energy and execution time. In our experiments, the energy per inference sample (frame) is computed from the product of execution time per sample and the total dynamic and static power of neurocores and x86 processors.

#### 3.2.2 Models Trained with SLAYER on Event-Based Datasets

Our first use case for NxTF consists of deploying a model trained directly on spikes. We take as example the SLAYER method [36]. This spike-based training method uses a form of backpropagation that updates synaptic weights by taking into account the timing of spikes in the past. After constructing the model using the NxTF interface (c. f. Fig. 2), we transfer the publicly available SLAYER weights

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All measurements reported here are obtained using NxSDK version 0.9.5 on Nahuku32 board ncl-ghrd-04. CPU results use an Intel Core i7-9700K processor with 32 GB RAM. GPU results use an Nvidia RTX 2070 card with 8 GB of memory. The operating system is Ubuntu 16.04.6 LTS running Python 3.5.5 and TensorFlow 1.13.1. Performance results are based on testing as of 1 Sep 2020 and may not reflect all publicly available security updates. Results may vary.

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and neuronal configuration from the original implementation\textsuperscript{5} into our model, and invoke the NxTF compilation function. Neurons in SLAYER models use a hard reset and thus require only a single compartment (c. f. Sec. 2.3.6). The resulting network is then run on Loihi while measuring power consumption and execution time. A tutorial for porting a SLAYER-trained model to Loihi using NxTF is included in the NxTF software package.

**N-MNIST.** The N-MNIST dataset \cite{1} is an event-based version of the classic MNIST handwritten digit dataset \cite{2}. The neuromorphic variant is obtained by recording the MNIST digits using a Dynamic Vision Sensor (DVS), while performing saccades to elicit motion-induced events. The SLAYER model for this dataset is a fully-connected network with a 1156-neuron input layer, a 512-neuron hidden layer, and a 10-neuron output layer.

The network fits on 30 neurocores (about 25\% of a Loihi chip). Even though the number of neurons in this network is small, the all-to-all connectivity between layers leads to a large number of synapses in the hidden layer. Hence, the partitioner distributes this particular layer across 18 cores that are only partially occupied by neurons but whose synaptic memory is exploited to the limit. Similarly, the input layer is distributed across 11 cores, which do not exhaust the neuron capacity but rather the limit of available output axons (to accommodate the large fan-out to the hidden layer). The final layer (consisting of 10 neurons) fits on a single core, where it consumes less than 15\% of available neuron-, synapse- and axon-resources.

As in the original SLAYER work, each of the 10 000 N-MNIST test samples is run for 350 algorithmic time steps, resulting in a total classification error of 1.49\% on Loihi. Table \ref{tab:results} compares the error rate against a model trained on spikes using spatio-temporal backpropagation \cite{28} and deployed on the SpiNNaker platform (unfortunately, power and execution time measurements were not available). With this SLAYER-trained model, inference on N-MNIST can be done at 141 samples per second and with an energy consumption of 0.62 mJ per sample.

As comparison, we trained the same architecture with standard backpropagation, using frames that were synthesized by binning 5 ms time slices from the DVS event data. The resulting ANN was then converted to an SNN using the method by \cite{34}. Interestingly, the energy and time to solution is lower compared to the directly trained model. The reason is that with a denser frame input, the converted SNN can be run for fewer algorithmic time steps to reach the desired classification error.

**DVS Gestures.** To demonstrate that NxTF can also be applied to SLAYER-trained convolutional architectures, we repeated the procedure of N-MNIST with the DVS Gestures dataset, using the SLAYER model from \cite{36}. This task consists of recognizing 11 human gestures like clapping and waving, recorded with a DVS. The dataset was originally evaluated on TrueNorth \cite{2}, to which we compare in Table \ref{tab:results}. For consistency with their methodology, we adopt in this experiment their definition of “delay” or “time to solution”, which is measured as the time it takes the correct neuron in the classification layer to fire its first spike after a new gesture is presented. For our model, this point is reached on average after 65 algorithmic time steps, resulting in an average delay of 4.35 ms per sample. Using instead a fix number of 300 time steps for measuring the delay, we obtain an execution time of 22 ms. The SLAYER model consists of 6 layers, which the compiler fits on 59 neurocores - 14 cores less than a prior version implemented with NxNet \cite{11}.

Another Loihi implementation of this task was reported recently by \cite{22}, who trained a model on synthesized frames, converted it using the method by \cite{34}, and applied NxTF to deploy the model on Loihi. The authors measure the delay based on 300 time steps per sample, which results in a 161 ms delay.

\textsuperscript{5}\url{https://github.com/bamsumit/slayerPytorch}, accessed Aug 2020

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Table 2. Summary and comparison of profiling results. "Energy" and "Delay" refer to energy and execution time per sample (c. f. Sec. 3.2.1). The delay values denoted with a * in the DVS Gestures section use the definition of delay from [2], i. e. the time it takes the correct neuron in the classification layer to become active. As for the Method column, "Train." denotes direct spike-based learning; "Conv." indicates a conversion approach; "ANN" denotes running the original non-spiking model. Our work using NxTF is highlighted in bold. Remarks on other methods: [19] is an FPGA implementation, [35] used 5 out of 10 classes and a subset of 1200 samples with resolution reduced to $10 \times 10$.

| Task          | Platform     | Method       | Num Neurons | Num Params | Error [%] | Energy [mJ] | Delay [ms] | EDP [μJs] |
|---------------|--------------|--------------|-------------|------------|-----------|-------------|------------|----------|
| N-MNIST       | SpiNNaker    | Train. (STBP) [28] | 810         | 792k       | 2.08      | -           | -          | -        |
|               | Loihi        | Train. (SLAYER) | 522         | 597k       | 1.49      | 0.62        | 7.07       | 4.38     |
|               | Loihi        | Conv. (SNN TB) | 522         | 597k       | 1.57      | 0.29        | 6.46       | 1.87     |
| DVS Gestures  | TrueNorth    | Conv. (Corelets) [15] | 262k       | 2M         | 8.23      | 19          | 105*       | 1971     |
|               | Loihi        | Conv. (SNN TB) [22] | 82k         | 83k        | 10.36     | -           | 161        | -        |
|               | Loihi        | Train. (SLAYER) | 31k         | 1M         | 3.79      | 0.54        | 4.35*      | 2.34     |
| MNIST         | Minitaur     | Conv. (Matlab) [19] | 1k          | 648k       | 8         | -           | 136        | -        |
|               | SpiNNaker    | Conv. (Matlab) [38] | 1k          | 648k       | 4.99      | 3.3         | 11         | 36.26    |
|               | TrueNorth    | Conv. [14]    | 4k          | -          | 0.60      | -           | -          | -        |
|               | BrainScales  | Conv. (PyNN) [35] | 55          | 2k         | 5         | -           | -          | -        |
|               | SpiNNaker    | Conv. (SNN TB) [28] | 8k          | 213k       | 1.80      | -           | -          | -        |
|               | Loihi        | Conv. (SNN TB) [22] | 58k         | 60k        | 1.30      | -           | 8          | -        |
|               | Loihi        | Conv. (SNN TB) | 4k          | 7k         | 0.79      | 0.66        | 6.65       | 4.38     |
|               | CPU³         | ANN (Tensorflow) | 4k          | 7k         | 0.74      | 19          | 0.4        | 7.55     |
|               | GPU³         | ANN (Tensorflow) | 4k          | 7k         | 0.74      | 111         | 2          | 222      |
| CIFAR-10      | TrueNorth    | Conv. (Corelets) [15] | 1M          | -          | 17.50     | -           | -          | -        |
|               | Loihi        | Conv. (SNN TB) [22] | 82k         | 83k        | 22.90     | -           | 21         | -        |
|               | Loihi        | Conv. (SNN TB) | 413k        | 3M         | 8.52      | 102         | 340        | 34926    |
|               | CPU³         | ANN (Tensorflow) | 413k        | 3M         | 8.07      | 157         | 3          | 508      |
|               | GPU³         | ANN (Tensorflow) | 413k        | 3M         | 8.07      | 1035        | 18         | 18924    |

3.2.3 Converted Models on Frame-Based Datasets. Our second use case for the NxTF framework covers the conversion of pre-trained ANNs to SNNs. For convenience we developed an interface⁶ between NxTF and a common conversion software, the SNN toolbox (SNN TB) [34]. This open-source framework automates most stages in the conversion and deployment pipeline. A user provides the pre-trained ANN in one of the supported DL libraries (Tensorflow / Keras, Pytorch, Caffe, Lasagne). The toolbox parses the provided network and constructs an equivalent model using the NxTF layer classes. If desired, SNN TB performs a parameter normalization step as outlined in Sec. 2.3.7. Subsequently, the network is compiled and run on Loihi. The toolbox includes methods for performance benchmarking and visualization of network activity.

MNIST. For MNIST we trained a 4-layer CNN with Keras [7] to achieve an error rate of 0.74%. After conversion to an SNN using the rate-based encoding method by [34], the SNN was mapped to 14 neurocores on Loihi. Even though the model contains about 8x more neurons than the N-MNIST model in Sec. 3.2.2, the core count is halved because the convolutional architecture requires about 88x fewer parameters than the fully-connected one. Thus, the utilization of resources on neurocores is dominated by the neuron count in case of the CNN, rather than synapse / axon count as in the fully-connected network. The reduced core count also highlights the benefit of the basic connection sharing capabilities of Loihi as described in Sec. 2.3.1. If no connections could be shared, the CNN would require 341k discrete rather than 6746 shared weights, and the core count would likely approach that of the fully-connected model.

⁶https://github.com/intel-nrc-ecosystem/models/tree/master/nxsdk_modules_ncl/snntoolbox
After mapping the model onto Loihi, we ran it for 100 algorithmic time steps per sample. Table 2 lists our profiling result together with related MNIST results published on other hardware platforms using different network architectures. Unfortunately, energy and execution time were not always reported or could not be compared directly. For instance, the TrueNorth work reports a throughput of 1000 frames per second while consuming 0.1 mJ per frame. This throughput however is achieved by pipelining the processing of consecutive frames on individual layers of the network. Also, the first convolution layer is computed offline. Models on TrueNorth employ a customized convolution connectivity, are stateless and binarized, and neuron activations are encoded by single spikes rather than firing rates, which impedes a direct comparison.

A useful property of SNNs is their ability to trade off accuracy against computational cost. As the classification result is obtained by accumulating evidence in form of spikes at the output layer across a certain time period, one may shorten the run time of the network to reduce the inference delay and energy cost at the potential risk of misclassifying some samples. Fig. 12 displays the resulting trade-off curve for the MNIST model tested here. We observe a high error at the beginning of a simulation, where spikes have not yet reached the output layer. As spikes begin to accumulate at the output, the error drops and converges to the error rate achieved by the original ANN, with an overall reduced Energy Delay Product. Note that the relatively low performance of the GPU can be attributed to the fact that we target an online setting (i.e. using a batch size of 1), which reduces the amount of parallelism that can be exploited.

CIFAR-10. Based on the high core utilization observed in Sec. 3.1.1 with this architecture, we choose MobileNet [18] for our experiments with CIFAR-10. The model consists of 28 layers and fits on 861 cores when compiled by NxTF. We trained the network in Tensorflow to a classification error of 8.07%, before converting it with SNN TB and compiling it with NxTF. The model was then benchmarked while running for 400 time steps per frame. We also profiled the performance of the original ANN on general-purpose hardware (Table 2) in online mode (batch size 1).

While the model runs more energy-efficiently on Loihi than on the CPU or GPU, the execution time per frame is significantly larger than on those platforms. A different CIFAR-10 model implemented with NxTF on Loihi by [22] runs 16x faster than our MobileNet. This smaller model fits on only 37 cores, i.e. 29% of a single Loihi chip, compared to the 7 chips required by MobileNet. To investigate the dependence of the execution time on the model size, we performed a
scaling analysis of the MobileNet architecture. MobileNet comes with a scale factor to reduce the number of channels in each feature map. By sweeping this scale factor from 1 to 1/16 in steps of 2, we reduced the overall model size by the same factor. Each of the resulting models was mapped to Loihi and profiled for energy consumption and execution time per frame. Figure 13 shows that the energy consumption increases supralinearly with the number of chips, while the execution time scales approximately linearly in this example. This delay scaling is in line with the observed increased run time of our larger MobileNet compared to the CNN of [22].

The observed slowdown compared to CPU or GPU platforms for increasingly larger models can be attributed to three causes. 1) Previous work on ANN-to-SNN conversion [34] has shown that approximation errors in the converted model increase with the network depth. These errors can be reduced by increasing the number of algorithmic time steps, at the cost of an increased delay. 2) The models evaluated here employ firing rates to represent and transmit information. The large number of spike events needed for an accurate encoding is reflected in a large number of synaptic operations, which slows down the execution duration of an algorithmic time step (Sec. 3.2.1). Promising approaches to reduce the spike count include temporal codes [24, 33], spike frequency adaptation [41], sigma-delta modulation [39, 40], and constrained training methods [28, 29, 37]. 3) The large number of spikes present in a rate code have the added side effect of increasing the likelihood of spike congestion at Loihi’s off-chip mesh links as discussed in Davies et al. [11]. In our current implementation of the NxTF compiler, a neuron connected to multiple cores on another chip will send individual spikes to each off-chip destination. Especially in the case of increasing neuron fanout of large networks, this redundant spike traffic easily congests off-chip links and slows down execution significantly. To mitigate this congestion problem, the number of redundant spikes can be reduced either at the compiler or hardware level by sending only a single spike per neuron to each destination chip and then fanning out to all destination cores from there. At the compiler level, this solution can be achieved by adding additional relay cores on the destination chip. At the hardware level, this multi-cast behavior could be integrated into the off-chip links. Preliminary experiments at the compiler level (not shown here) suggest a potential speed-up of 15× using relay cores.
4 DISCUSSION

In this work we introduced NxTF, a programming interface and compiler embedded in Intel’s NxSDK, for deploying DNNs on the neuromorphic Intel Loihi system. In this task we were guided by two objectives: reducing the entry barrier for users familiar with standard DL software frameworks to access neuromorphic hardware, and optimal usage of the limited on-chip memory resources. The first objective was achieved by deriving the user-interface from Keras. The second objective was approached using a greedy layer-wise optimization algorithm that minimizes a cost metric as a function of neuron, synapse and axon requirements per Loihi core. Further, we exploited Loihi’s support for connection sharing to minimize duplication of weight kernels in convolutional topologies.

The present work targets a particular neuromorphic platform, Loihi. Some aspects of NxTF are specifically tailored to this architecture, for instance the dissection of the connectivity matrix (Fig. 6c) and the synapse encoding (Sec. 2.3.5). However, several aspects of NxTF are general enough to be adopted in other SNN hardware, such as the Keras-derived API (Fig. 2), or the partition optimization strategy (Sec. 2.3.3).

A direct comparison against the compilation methods of other frameworks such as SpiNNTools [32] or TrueNorth Corelets [1] is difficult because NxTF specializes in mapping DNNs rather than arbitrary network topologies. Perhaps most closely related is the Nengo tool chain [3] from Applied Brain Research, which provides a training and conversion framework for Deep Learning models (NengoDL) as well as a backend for deployment on Loihi. This framework has lead to promising results on a variety of tasks, including keyword spotting [5] and robotic control [12]. Unlike NxTF however, NengoDL currently does not optimize for synapse sharing in convolution layers and provides no automated partitioning scheme. To fit a large network onto Loihi, users must determine core shapes for a suitable layer dissection heuristically.

The NxTF framework was applied in two typical use cases: Models obtained via direct spike-based training and models converted from ANNs applied to sparse spike-based and dense frame-based inputs respectively. For the first use case we considered the neuromorphic datasets N-MNIST and DVS Gestures, for the second we converted a CNN for MNIST and a MobileNet for CIFAR-10. The models achieve a throughput between 3 and 230 inference samples per second, consuming between 102 and 0.29 mJ per sample (for CIFAR-10 and N-MNIST, respectively). In terms of classification accuracy, our models are on par with other state-of-the-art models; with an error rate of 8.52% on CIFAR-10 we significantly advance the best result reported for this dataset on neuromorphic hardware.

Our results suggest several improvements for future neuromorphic architecture designs: Although the NxTF compiler achieves high resource utilization for many DNN topologies as shown in Sec. 3.1, higher degrees of memory utilization would be possible via a shared-memory architecture that allowed to trade on-chip neuron, synapse or axon resources off against each other to ensure near 100% memory utilization on every neurocore. This mechanism would avoid scenarios as shown in Fig. 10 in which only a small fraction of neurons in a neurocore are occupied because the synaptic memory limits are exceeded. Support for dedicated CNN compression would further allow to save on-chip memory resources. Furthermore, a built-in soft reset as opposed to a hard reset mechanism would eliminate the need to duplicate neuron compartments as in our current multi-compartment implementation (Sec. 2.3.6). Finally, an execution slow-down due to spike congestion at off-chip mesh links could be mitigated by multi-cast links.

The present work also highlights the need for more efficient spike codes than the rate codes employed here. This need has long been recognized and a variety of alternatives have been proposed. Direct training of SNNs that tap into the temporal coding domain, explicit temporal coding schemes, hybrid training / conversion methods, or sigma-delta coding approaches are all promising steps in this direction [24, 29, 33, 37, 39–41].
Finally, performance results in the form of energy and execution time are scarce in the literature, even for well-explored datasets like MNIST. We hope that the SNN API and compilation framework developed here will enable a more rapid and straightforward evaluation of novel SNN models on neuromorphic hardware.

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