Abstract

In this work, we present a family of operational semantics that gradually approximates the realistic program behaviors in the C/C++11 memory model. Each semantics in our framework is built by elaborating and combining two simple ingredients: viewfronts and operation buffers. Viewfronts allow us to express the spatial aspect of thread interaction, i.e., which values a thread can read, while operation buffers enable manipulation with the temporal execution aspect, i.e., determining the order in which the results of certain operations can be observed by concurrently running threads.

Starting from a simple abstract state machine, through a series of gradual refinements of the abstract state, we capture such language aspects and synchronization primitives as release/acquire atomics, sequentially-consistent and non-atomic memory accesses, also providing a semantics for relaxed atomics, while avoiding the Out-of-Thin-Air problem. To the best of our knowledge, this is the first formal and executable operational semantics of C11 capable of expressing all essential concurrent aspects of the standard.

We illustrate our approach via a number of characteristic examples, relating the observed behaviors to those of standard litmus test programs from the literature. We provide an executable implementation of the semantics in PLT Redex, along with a number of implemented litmus tests and examples, and showcase our prototype on a large case study: randomized testing and debugging of a realistic Read-Copy-Update data structure.

1. Introduction

Memory models describe the behavior of multithreaded programs, which might concurrently access shared memory locations. The best studied memory model is sequential consistency (SC) [28], which assumes a total order on all memory accesses (i.e., read and write operations) in a single run of a concurrent program, therefore, ensuring that the result of each read from a location is a value that was stored by the last preceding write to the very same location.

However, sequential consistency falls short when describing the phenomena, observed in concurrent programs running on modern processor architectures, such x86, ARM, and PowerPC, and resulting from store buffering [50] and CPU- and compiler-level optimizations, e.g., rearranging independent reads and writes [21]. Relaxed memory models aim to capture the semantics of such programs and provide suitable abstractions for the developers to reason about their code, written in a higher-level language, independently from the hardware architecture it is going to be executed on.

The most prominent example of a relaxed memory model is the C11 model, introduced by the C/C++ 2011 standards [2, 3] and describing the behavior of concurrent C/C++ programs. It defines a number of memory accesses, implementing different synchronization policies and having corresponding performance costs. For instance, SC-atomics provide the SC-style total ordering between reads and writes to the corresponding memory locations, while release/acquire (RA) accesses implement only partial one-way synchronization, but are cheaper to implement. Finally, relaxed accesses are the cheapest in terms of performance, but provide the weakest synchronization guarantees.

Existing formalizations of the full C11 memory model adopt an axiomatic style, representing programs by sets of consistent executions [5–7]. Each execution can be thought of as a graph, whose nodes are read/write-accesses to memory locations. The edges of the graph represent various orders between operations (e.g., total orders between SC-atomics and operations in a single thread), some of which might be partial. Defined this way, the executions help one to answer questions of the following kind: “Can the value X be read from the memory location L at the point R of the program P?”

This axiomatic whole-program representation makes it difficult to think of C11 programs in terms of step-by-step executions of a program on some abstract machine, making it non-trivial to employ these semantic approaches for the purposes of testing, debugging and compositional symbolic reasoning about programs, e.g., by means of type systems and program logics. Recently, several attempts have been made to provide a more operational semantics for C/C++ concurrency, however, all the approaches existing to date focus on a specific subset of C11, e.g., release/acquire/SC synchronization [26,45] or relaxed atomics [38], without providing a uniform framework accommodating all features of the standard.

In this work, we make a step towards providing a simple, yet uniform foundations for accommodating all of the essential aspects of the C11 concurrency, and describe a framework for defining operational semantics capturing the expected behaviors of concurrent executions observed in realistic C/C++ programs, while prohibiting unwelcome outcomes, such as Thin-Air executions. The paramount idea of our constructions is maintaining a rich program state, which is a subject of manipulation by concurrent threads, and is represented by a combination of the following two ingredients.

Ingredient 1: Viewfronts for threads synchronization. We observe that, assuming a total ordering of writes to each particular shared memory location, we can consider a state to be a collection of per-location histories, representing totally-ordered updates—an idea adopted from the recent works on logics for SC concurrency [41]. We introduce the notion of viewfronts as a way to account for the phenomenon of particular threads having specific, yet consistent, views to the global history of each shared location, similarly to the way vector clocks are used for synchronization in distributed systems [30]. We then consider various flavors of C11 atomicity as ways to “partially align” viewfronts of several threads.
Ingredient 2: Operation buffers for speculative executions  The mechanism of relaxed atomic accesses in C11 allows for speculative reordering or removing of operations, involving them, in particular threads. In order to formally define the resulting temporal phenomena, observed by concurrently running threads (which can see some values appearing “out-of-order”), we need to capture a speculative nature of such computations. As an additional challenge, the semantics has to prohibit so-called Out-of-Thin-Air executions, in which results appear out of nowhere. We solve both problems by adopting the notion of operation buffers from earlier works on relaxed memory models [10, 11, 16], and enhancing it with nesting structure as a way to account for conditional speculations.

While simple conceptually, the two described ingredients, when combined, allow us to capture precisely the behavior of standard C11 synchronization primitives (including consume-reads), desired semantics of relaxed atoms, as well as multiple aspects of their interaction, by elaborating the treatment of viewfronts and buffers. The C11 standard is intentionally designed to be very general and allow for multiple behaviors. However, particular compilation schemes into different target architectures might focus only on specific subsets of the enumerated features. To account for this diversity, our framework comes in an aspect-oriented flavor: it allows one to “switch on and off” specific aspects of C11 standard and to deal only with particular sets of allowed concurrent behaviors.

1.1 Contributions and outline  We start by outlining the basic intuition and illustrating a way of handling C11’s RA-synchronization and speculative executions, introducing the idea of thread-specific viewfronts and operation buffers in Section 2. Section 3 demonstrates more advanced aspects of C11 concurrency expressed in our framework. Section 4 gives a formal definition of the operational model for C11, which is our central theoretical contribution. Section 5 describes evaluation of our semantics implemented in the PLT Redex framework [17, 25]. We argue for the adequacy of our constructions with respect to the actual aspects of C11 using a large corpus of litmus test programs, adopted from the earlier works on formalizing C11 concurrency. To do so, we summarize the described operational aspects of concurrent program behavior in C11, relating them to outputs of litmus tests. In Section 6, we showcase our operational model by tackling a large realistic example: testing and debugging several instances of a concurrently used Read-Copy-Update data structure [31, 34], implemented under relaxed memory assumptions. Our approach successfully detects bugs in the cases when the employed synchronization primitives are not sufficient to enforce the atomicity requirements, providing an execution trace, allowing the programmer to reproduce the problem. We compare to the related approaches to formalizing operational semantics for relaxed memory in general and for C11 in particular in Section 7, and conclude with a discussion of the future work in Section 8.

2. Overview and Intuition  We start by building the intuition for the program behaviors one can observe in the C11 relaxed memory model.

The code below implements the message passing pattern, where one of the two parallel threads waits for the notification from another one, and upon receiving it proceeds further with execution.

```plaintext
[f] := 0; [d] := 0;
repeat [f] end;
[r] = [d]
```

The identifiers in square parentheses (e.g., [f]) denote accesses (i.e., reads and writes) to shared mutable memory locations, subject to concurrent manipulation, whereas plain identifiers (e.g., r) stand for thread-local variables. In a sequentially consistent setting, assuming that reads and writes to shared locations happen atomically, the right thread will not reach the last assignment to r until the left thread sets the flag f to be 1. This corresponds to the “message passing” idiom, and, hence, by the moment [f] becomes 1, d will be pointing to 5, so by the end of the execution, r must be 5.

In a more realistic setting of C/C++ concurrent programming, it is not sufficient to declare all accesses to [f] and [d] as atomic: depending on particular ordering annotations on read/write accesses (e.g., relaxed, SC, release/acquire etc) the outcome of the program might be different and, in fact, contradictory to the “natural” expectations. For instance, annotating all reads and writes to [f] and [d] as relaxed might lead to r being 0 at the end, due to the compiler and CPU-level optimizations, rearranging instructions of the left thread with no explicit dataflow dependency or, alternatively, assigning the value of [d] to r in the right thread speculatively.

One way to avoid these spurious results is to enforce stronger synchronization guarantees between specific reads and writes in a program using release/acquire order annotations. For instance, to ensure the “natural” behavior of the message-passing idiom, the program from above can be annotated as in Figure 1.

In the modified program, all accesses to the location d are now annotated as non-atomic, which means racy concurrent manipulations with them are considered run-time errors. What is more important, the write to f in the left thread is now annotated with rel modifier, which “publishes” the effects of the previous operations, making them observable by concurrently running threads after the assigned to f value 1 is read by them. Furthermore, the read from f in the right thread is now annotated with acq, preventing the operations following it in the same thread from taking effect before the read itself takes place. Together, the release/acquire modifiers in Figure 1 create a synchronization order we are seeking for and ensure that the second assignment to r will only take place after the repeat-loop terminates, hence the observed value of f is 1, which implies that the observed value of d is 5, thanks to the release-write, so the final value of r is also 5. Notice that there is also no race between the two concurrent non-atomic accesses to d, as those are clearly separated in time, thanks to the synchronization between release/acquire accesses to f.

Axiomatic semantics and execution orders  The state-of-the-art formalization [7] of C11 defines semantics for program execution as a set of graphs, where nodes denote memory accesses (i.e., reads and writes) with particular input/result values, and edges indicate ordering relations between them.1

One instance of an execution graph for MP_rel+acq-na is shown in Figure 2. The edges labelled by sb indicate a natural program order, reconstructed from the program’s syntax. The green edge marked sw indicates the synchronizes-with relation, which arises dynamically between a release-write and acquire-read of the same value from the same location. The transitive closure of the union of the sb and sw relations is called happens-before relation (hb) and is central for defining the observed behaviors. In particular, a value X, written at a point R0 of a program, can be only read at a point R1 if there is no hb-ordering between the corresponding read event in R2 and write event in R1. That, the read-from order (rf) must not contradict the hb order.

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1For illustrative purposes, here we employ a version of execution graphs [49] with additional explicit nodes for spawning and joining threads.
The C11 standard defines a number of additional axioms, specifying the consistent execution graphs. In particular, all write actions on an atomic location (i.e., such that it is not accessed non-atomically) must be totally ordered via modification ordering relation (mo), which is consistent with hb, restricted to this location: if a write operation \( W_1 \) to a location \( \ell \) has a greater timestamp than \( W_1 \), also writing to \( \ell \), then \( W_1 \) cannot be hb-ordered after \( W_2 \). The mo relation is shown in Figure 2 via per-location timestamps \( \tau \), incremented as new values are stored. Moreover, a read event \( R_\ell \) cannot read from \( W_1 \), if \( R_\ell \) is hb-ordered after \( W_2 \), i.e., it’s aware of the later write \( W_2 \), as illustrated by \( rf \)-edges in Figure 2, preventing the case of reading of \( 0 \) from \( d \).

2.1 Synchronizing threads’ knowledge via viewfronts

The read-from relation determines the results of reads in specific program locations depending on preceding or concurrent writes by relying on the global \( sb \) and \( sw \) orderings, and restricting them according to the C11 axioms. To avoid the construction of global partial orders and provide an incremental operational formalism for executing concurrent C11 programs, we focus on the mo relation for specific locations, making it an inherent component of the program state. We call this state component a history: it contains totally ordered “logs” of updates to every shared memory location, indexed by timestamps (natural numbers). The history is objective (i.e., global): it contains information about all updates to shared locations, as they took place during the execution.

However, the way threads “see” the history with respect to particular locations is subjective (i.e., thread-local): each thread has its own knowledge of what is the “latest” written value to each location. Thus, the value a thread actually reads can be written no earlier than what the thread considers to be the location’s latest value. To formalize this intuition, we define the notion of viewfronts.

A viewfront is a partial function from memory locations to natural numbers, representing timestamps in the corresponding location’s part of the history. A thread’s viewfront represents its knowledge of what were the timestamps of last written values to the relevant locations that it is aware of. When being a subject of a release-write, a location will store the viewfront of a writing thread, which we will refer to as synchronization front, in addition to the actual value being written. Symmetrically, another thread performing a synchronized load (e.g., acquire-read) from the location will update its viewfront via the one “stored” in the location. Viewfronts, when used for expressing release/acquire synchronization, are reminiscent to vector time frames [39], but are used differently to express more advanced aspects of C11 atomicity (see Section 3 for details).

The following table represents the history and the threads' viewfronts for the example from Figure 1 at the moment the left thread has already written 1 and 5 to \( f \) and \( d \), but the right thread has not yet exited the repeat-loop.

| \( \tau \) | \( f \) | \( d \) |
|---|---|---|
| 0 | \( [x]_{1,6} := 0 \) | \( [y]_{1,6} := 0 \) |
| 1 | \( r_1 = [y]_{1,6} ; \) | \( r_2 = [x]_{1,6} ; \) |

Figure 3. An example with early reads (LB_rfx).

The values in the first column (0, 1) are timestamps, ascribing total order mo to the values written to a certain location (\( f \) and \( d \) correspondingly). The remaining columns capture the sequence of updates of the locations, each update represented as a pair of a value and a stored synchronization front. Viewfronts form a lattice, as partial maps from locations to timestamps, with \( \perp = 0 \). The \( \perp \) fronts are used for location updates corresponding to non-atomic stores. The front (\( f \mapsto 1, d \mapsto 1 \)) was stored to \( f \) upon executing the corresponding release-write, capturing the actual viewfront \( \perp \) of the left thread. The right thread’s viewfront \( R \) indicates that it still considers \( f \) and \( d \) to be at least at timestamp 0, and, hence, can observe their values at timestamps larger or equal than 0.

Let us explore a complete execution trace of the program from Figure 1. The initial state looks as follows:

| \( \tau \) | \( f \) | \( d \) |
|---|---|---|
| 0 | \( 0, \perp \) | \( 0, \perp \) |

and after the parent thread executes ‘\( f \mapsto 0 \)’ and ‘\( d \mapsto 0 \)’, it becomes:

| \( \tau \) | \( f \) | \( d \) |
|---|---|---|
| 0 | \( 0, \perp \) | \( 0, \perp \) |

Two subthreads are spawned, inheriting the parent’s viewfront:

| \( \tau \) | \( f \) | \( d \) |
|---|---|---|
| 0 | \( 0, \perp \) | \( 0, \perp \) |

The left subthread performs ‘\( [d]_{1,6} := 5 \)’, incrementing the timestamp \( \tau \) of \( d \) and updating its own viewfront \( L \):

| \( \tau \) | \( f \) | \( d \) |
|---|---|---|
| 0 | \( 0, \perp \) | \( 0, \perp \) |

Next, the left thread executes ‘\( f \mapsto 1 \)’, updating its viewfront and simultaneously storing it to the 1-entry \( f \):

| \( \tau \) | \( f \) | \( d \) |
|---|---|---|
| 0 | \( 0, \perp \) | \( 0, \perp \) |

The right thread can read the values of \( f \), stored no later than its viewfront \( R \) indicates, thus, eventually it will perform the acquire-read from \( f \) with \( \tau_f = 1 \), updating its \( R \) correspondingly:

| \( \tau \) | \( f \) | \( d \) |
|---|---|---|
| 0 | \( 0, \perp \) | \( 0, \perp \) |

Now the right thread’s viewfront is updated with respect to the latest store to \( d \), it reads 5 from it, and the threads join:

| \( \tau \) | \( f \) | \( d \) |
|---|---|---|
| 0 | \( 0, \perp \) | \( 0, \perp \) |

2.2 Speculating with operation buffers

Relaxed atomics in C11 allow for speculative program optimizations, which might result in out-of-order behaviors, observed during concurrent executions under weak memory assumptions.

As a characteristic example of such a phenomenon, consider the program in Figure 3. The C11 standard [3], as well as its axiomatic...
formal models [5,7,49], allow for the outcome \( r_1 = 1 \land r_2 = 1 \) by the end of its execution, as a result of rearranging instructions. Alas, our viewfront-based semantics cannot account for such a behavior: in order to be read from a location, a value should have been first stored into the history by some thread! However, in the example, it is either \( x \) or \( y \) that stores 1 (but not both) at the moments \( r_1 \) and \( r_2 \) were assigned. That is, while viewfront manipulation enables fine-grained control of what can be observed by threads, it does not provide enough flexibility to specify when effects of a particular thread’s operations should become visible to concurrent threads.

To account for such anomalies of relaxed behaviors, we introduce per-thread operation buffers, which allow a thread to postpone an execution of an operation, “resolving” it later. An operation buffer itself is a queue of records, each of which contains essential information for performing the corresponding postponed operation. For instance, for a postponed read action, a thread allocates a fresh symbolic value to substitute for a not-yet-resolved read result, and adds a tuple, containing the location and the symbolic value, to the buffer. For a write action the thread puts another tuple, the location and the value to store to it, to the buffer. As it proceeds with the execution, the thread can non-deterministically resolve an operation from the buffer if there is no operation before it, which may affect its result, e.g., a write to the same location, or an acquire-read changing the local viewfront. For instance, in Figure 3, buffering the effects of the two relaxed reads, \([y]_{r_1} \) and \([x]_{r_2} \), postpones their effects beyond the subsequent writes, enabling the desired outcome, as by the moment the reads are resolved, the corresponding 1’s will be already stored to the history.

**Nested buffers and speculative conditionals** The idea of buffering operations for postponing their effects in a relaxed concurrency settings is not novel and has previously appeared in a number of related weak memory frameworks [10, 11, 13, 16]. However, in our case it comes with a twist, making it particularly well suited for modelling C11 behaviors, while avoiding “bad” executions.

To illustrate this point, let us consider an example of a speculative optimization involving a conditional statements. Such optimizations are known to be difficult for modelling in relaxed concurrency [5, 38]. For instance, in the program in Figure 4, the assignment \([y]_{r_1} := 1 \) can be “pulled out” from both branches of the left thread’s conditional statement, as it will be executed anyway, and, furthermore, it does not bear a data dependency with the possible preceding assignment \([y]_{r_2} := 1 \).

Such an optimization will, however, lead to interesting consequences: in the right thread, the conditional statement might succeed assigning 1 to \( x \), therefore leading to the overall result \( r_{ef} = 1 \). This outcome relies on the fact that the optimization, which made \([y]_{r_2} := 1 \) uncontrollably visible to the right thread, was done speculatively, yet it has been justified later, since the same assignment would have been performed no matter which branch has been executed.

Luckily, to be able to express such a behavior, our buffer machinery requires only a small enhancement: nesting. In the semantics, upon reaching an if-then-else statement, whose condition’s expression is a result of some preceding relaxed read, which is not yet resolved, we create a tuple, containing the symbolic representation of the condition as well as two empty buffers, to be filled with postponed operations of the left and the right branches, correspondingly. The tuple is then added to the thread’s main operation buffer.

More specifically, in the program SE_simple, the history after the three initial relaxed writes is as follows:

\[
\begin{array}{c|c|c|c}
\text{r} & x & y & z \\
\hline
0 & 0, (x \mapsto 0) & 0, (y \mapsto 0) & 0, (z \mapsto 0) \\
1 & - & 1, (y \mapsto 1) & - \\
\end{array}
\]

The left thread then postpones reading from \( x \) and start the executing the if statement speculatively, with the following buffer:

\[
(a = [x]_{r_1} : \text{if } a \not\equiv 0) \}
\]

Proceeding to execute the two branches of the if-statement with focusing on the corresponding nested buffers, the left thread eventually fills them with the postponed commands:

\[
(a = [x]_{r_1} : \text{if } a \not\equiv 0) \}
\]

At this point the two sub-buffers contain the postponed write \([y]_{r_1} := 1\) and \([y]_{r_2} := 1\), and no other postponed operations in the same buffer are in conflict with them. This allows the semantics to promote this write to the upper-level buffer (i.e., the main buffer of the thread):

\[
(a = [x]_{r_1} : [y]_{r_1} := 1) \}
\]

Next, the write is resolved, so its effect is visible to the right thread:

\[
(a = [x]_{r_1} : [y]_{r_1} := 1) \}
\]

At that moment, the overall history looks as follows:

\[
\begin{array}{c|c|c|c}
\text{r} & x & y & z \\
\hline
0 & 0, (x \mapsto 0) & 0, (y \mapsto 0) & 0, (z \mapsto 0) \\
1 & - & 1, (y \mapsto 1) & - \\
\end{array}
\]

Hence, the right thread can read 1 from the location \( y \), take the then branch of the if statement, and perform the write to \( x \):

\[
(1 \not\equiv 0) \}
\]

Now the left thread can resolve the postponed read \( a = [x]_{r_1} \) obtaining 1 as its result and reducing the operation buffer:

\[
(1 \not\equiv 0) \}
\]

By evaluating the buffered if and resolving the write \([x]_{r_2} := 1\):

\[
\begin{array}{c|c|c|c}
\text{r} & x & y & z \\
\hline
0 & 0, (x \mapsto 0) & 0, (y \mapsto 0) & 0, (z \mapsto 0) \\
1 & 1, (x \mapsto 1) & 1, (y \mapsto 1) & 1, (z \mapsto 1) \\
\end{array}
\]

Reading from the latest record for \( z \) results in \( r_{es} = 1 \). The idea of nested buffers with promoting duplicating records from a lower to an upper level (under some dependency conditions) naturally scales for the case of nested if-statements.

**On the Out-of-Thin-Air problem** So what are the “bad” executions that should be prohibited by a meaningful semantics?

The C11 standard [2, 3] and the axiomatic semantics [7] allow for so-called Out-of-Thin-Air (OTA_if) behaviors, witnessed by self-satisfying conditionals, such as the one represented by the program in Figure 5, which, according to the standard is allowed to end up with \( r_1 = r_2 = 1 \). Such behavior is, however, not observable on any of the major modern architectures (x86, ARM, and POWER), and considered as a flaw of the model [5, 8], with researchers developing alternative semantics for relaxed atomics that avoid OTA [38].

![Figure 4](image-url) A program allowing if-speculations (SE_simple).

![Figure 5](image-url) Program with C11-allowed Thin-Air behavior (OTA_if).
Notice the only essential difference between the programs in Figure 4 and 5 is that in the former the write performed speculatively will always take place, whereas in the latter one the speculative writes in the then-branch might end up unjustified.

As we have previously demonstrated, our semantics supports the weak behavior of the program in Figure 4, and outlaws it for the program in Figure 5, as the conditions for promoting buffered operations in the if-branches will not be met in the latter case.

3. Advanced Aspects of C11 Concurrency

In this section, we elaborate and employ the ideas of viewfronts and operation buffers to adequately capture the remaining aspects of C11 concurrency. In particular, we (i) show how to extend the viewfront mechanism to support sequentially-consistent (SC) and non-atomic (NA) memory accesses, as well as consume-reads, (§§3.1–3.3); (ii) employ operation buffers to account for specific phenomena caused by sequentialization optimization (§3.4), and (iii) demonstrate the interplay between relaxed atomics and RA-synchronization (§3.5).

3.1 Sequentially-consistent memory accesses

To see the difference between SC-style and release/acquire-synchronization in C11, consider the program in Figure 6. All SC-operations are totally ordered with respect to each other, and the last of them is either read from x, or from y. Thus, the overall outcome $r_1 = 0 \land r_2 = 0$ is impossible. Replacing any of the $sc$ modifiers by release or acquire in the corresponding writes and reads, makes $r_1 = 0 \land r_2 = 0$ a valid outcome, because there is no more the total order on all operations. In particular, the left subthread (with RA modifiers instead of SC) could still read 0 from y, as by its viewfront, which at that moment is $(x \mapsto 1, y \mapsto 0)$.

In the axiomatic model [7,49], the restricted set of SC behaviors is captured by introducing an additional order $sc$ and several axioms, requiring, in particular, consistency of $sc$ with respect to $rh$ and $ro$. In our operational setting, it means that an SC-read cannot read from a write with a smaller timestamp than the greatest timestamp of SC-writes to this location. To capture this requirement, we instrument the program state with an additional component—a global viewfront of sequentially consistent memory operations $(\sigma_{\text{sc}})$, which is being updated at each SC-write.

3.2 Non-atomic memory accesses and data races

Following the C11 standard [2,3], our semantics does not draw a distinction between non-atomic and atomic locations (in contrast with the axiomatic model [7]). However, data races involving non-atomic memory operations (whose purpose is data manipulation, not thread synchronization) might result in an undefined behavior.

Consider the following two code fragments with data races on non-atomics. In the first case, a thread performs a na-read concurrently with a write to the same location.

$[d]_{\text{na}} := 0; \quad [d]_{\text{val}} := 1 \quad \sigma = [d]_{\text{val}}$

We can detect the data race, when the right subthread is executed after the left one, so it performs the na-read, while not being “aware” of the latest write to the same location. As our semantics constructs the whole state-space for all possible program executions, we will identify this data race on some execution path.

The second case is an opposite one: na-write and atomic read:

$[p]_{\text{na}} := \text{null}; \quad [d]_{\text{na}} := 0; \quad [x]_{\text{na}} := 0; \quad [x]_{\text{acl}} := 1; \quad [d]_{\text{acl}} := 0; \quad [x]_{\text{acl}} := 1;\quad r_1 = [p]_{\text{con}}; \quad \sigma = r_1 \lor [r]_{\text{na}}; \quad r_2 = [r]_{\text{na}}; \quad r_3 = [x]_{\text{acl}}; \quad \text{if } r_1 \lor [r]_{\text{na}}; \quad \text{then } r_2 = [r]_{\text{na}}; \quad r_3 = [x]_{\text{acl}}; \quad \text{else } r_2 = 0; \quad r_3 = 0 \quad \text{fi}$

Figure 7. An example with a consume read ($MP_{\text{con}+na_2}$).

It still has a data race involving a non-atomic access, which, however, we cannot detect by comparing threads’ viewfronts. To identify data races of this kind, we extend the state with a global na-front, storing a timestamp of the last na-write to a location. Now, if the left thread executes its na-write first, the atomic read in the right one will not be aware of it, which will be manifested as a data race, thanks to the na-front.

3.3 Consume-reads

Unlike acquire-reads, consume-reads [33] do not update a thread’s viewfront, but provide a synchronization front only for subsequent reads that are dereferencing their result.

Consider the code fragment in Figure 7. Here, we have message-passing of data stored in d via location p. The right thread employs a consume-read from p. In the case when it gets a non-null value (representing a pointer to d), it reads from it to r2, and after that from location x to r3. There might be three possible outcomes: $r_1 = \text{null} \land r_2 = 0 \land r_3 = 0$, $r_1 = d \land r_2 = 1 \land r_3 = 1$, and $r_1 = d \land r_2 = 1 \land r_3 = 0$. Changing the consume-read to an acquire one makes the last triple forbidden, as the right thread’s viewfront would become up to date with both $[x]_{\text{acl}} := 1$ and $[d]_{\text{val}} := 1$ after acquire-reading a non-null pointer value from p. At the same time, consume-read $r_1 = [p]_{\text{con}}$ provides synchronization only for $r_2 = [x]_{\text{acl}}$, which explicitly dereferences its result, but not for r3, which has no data-dependency with it.

Adding consume-reads to the semantics requires us to change the program syntax to allow run-time annotations on reads, which might be affected by consume ones. When a consume-read is executed, it retrieves some value/first-entry $(v, \sigma)$ from the history, as any other read. Unlike an acquire-read, it does not update the thread’s viewfront by the retrieved $\sigma$. Instead, it annotates all subsequent data-dependent reads by the front $\sigma$. Later, when these reads will be executed, they will join the front $\sigma$ from the annotation with the thread’s viewfront for computing the lower boundary on the relevant location’s timestamp. The same process is applied to annotate data-dependent postponed reads in buffers, which might refer to the symbolic result of a consume-read.

3.4 Threads joining and synchronization

Once two threads join, it is natural to expect that all their postponed memory operations are resolved, i.e., they have empty operation buffers. This is reflected in the axiomatic semantics [7] by an additional-synchronizes-with relation, which is a part of the happens-before relation. Thus, every memory action of joined threads happens-before actions which are syntactically after the
between the writes of thread axiomatic model [7], which defines a notion of release sequence $T$. However, when an acquire-read in thread $1$ would imply synchronization between $y_{rel} = 1$ and $r_1 = [y]_{acq}$, thus the former happens before the latter one! Following the rules of RA-synchronization, $r_2 = [x]_{rlx}$ should happen before $[x]_{rlx} = 1$ as well, making it impossible to read $1$ into $r_2$. The problem is clear now: we need to prevent from happening the situations, when a read, postponed beyond a release-write $W$, is resolved after some concurrent acquire-read gets synchronized with $W$, as it might damage RA-synchronization sequences.

To achieve this, we instrument the state with a global list $y$ of triples that consist of: (i) a location $\ell$, (ii) a timestamp $\tau$ of some executed write, and (iii) a symbolic value $x$ of a read postponed beyond this write. When executing a release-write $W$, which stores a value to a location $\ell$ with a timestamp $\tau$, for each thread-local postponed read, we globally record a tripel $\langle \ell, \tau, x \rangle$, where $x$ is the symbolic value of the read. An acquire-read of the $(\ell, \tau)$ history entry by another thread succeeds only if there are no $\langle \ell, \tau, x \rangle$ left in $y$ for any symbolic value $x$. Resolving a postponed read with a symbolic value $x$ removes all $x$-related entries from $y$.

The program in Figure 11 is more problematic, as it has release/acquire modifiers on accesses to $y$, and postponing the read $[x]_{rlx}$ in the right thread might lead to $r_1 = r_2 = 1$. Notice that such an outcome is in conflict with the semantics of RA, as assigning $1$ to $r_1$ would imply synchronization between $y_{rel} = 1$ and $r_1 = [y]_{acq}$, thus the former happens before the latter one! Following the rules of RA-synchronization, $r_2 = [x]_{rlx}$ should happen before $[x]_{rlx} = 1$ as well, making it impossible to read $1$ into $r_2$.

The problem is clear now: we need to prevent from happening the situations, when a read, postponed beyond a release-write $W$, is resolved after some concurrent acquire-read gets synchronized with $W$, as it might damage RA-synchronization sequences.

3.5 Relaxed atomics and synchronization

Interaction between relaxed atomics and RA-synchronization is particularly subtle, due to a number of ways they might affect the outcomes of each other. We identify these points of interaction and describe several design decisions, elaborating the structure of the state, so the requirements imposed by the C11 standard are met.

3.5.1 Relaxed writes and release sequences

Since a relaxed read cannot be used for synchronization, in our semantics it does not update the viewfront of the thread with a synchronization front from the history (as an acquire read does). However, when an acquire-read in thread $T_1$ reads a result of a relaxed write performed by thread $T_2$, it should be synchronized with a preceding release-write to the same location performed by thread $T_1$, if there is one. This observation follows the spirit of the axiomatic model [7], which defines a notion of release sequence between the writes of thread $T_1$.

For an example, let us take a look at Figure 9 presenting a modified version of the message-passing program. The only possible outcome for $r_1$ is $5$, because when $[y]_{acq}$ gets $2$, it also becomes synchronized with $[x]_{rel} := 1$, which precedes $[y]_{rel} := 2$ in the left thread. At the same time $r_2$ can be either $0$ or $1: 0$ is a possible outcome for $r_2$, because $[y]_{acq}$ synchronizes with $[y]_{rel} := 1$, which precedes the $[x]_{rel} := 1$ write, which therefore might be missed.

To express this synchronization pattern in our model, we instrument the state with per-thread write-fronts, containing information about last release writes to locations performed by the thread. Upon a relaxed write, this information is used to retrieve a synchronization front from the history record with a timestamp equal to the write-front value, contributed by a preceding release-write.

3.5.2 Postponed relaxed operations and synchronization

Consider the program in Figure 10, which is similar to the example from Figure 3, but writes have release-modifiers. Since a release write does not impose any restriction without a related acquire read, it is still possible to get the result $r_1 = r_2 = 1$. Therefore, our semantics allows to perform a release-write even if there are postponed reads from other locations in the thread’s buffer.

Figure 9. Example of release sequence (MP_rel+acq+na+rlx_2).

\[
[f]_{na} := 0; \quad [d]_{na} := 0; \quad [x]_{na} := 0; \\
[d]_{na} := 5; \quad \{f\}_{rel} := 1; \quad \{x\}_{rel} := 1; \quad \{y\}_{rel} := 2 \\
\text{repeat}\; \{f\}_{acq} = 2\; \text{end}; \\
r_1 = [d]_{na}; \quad r_2 := [x]_{rels}; \\
\]

Figure 10. Postponed relaxed reads and release-writes (LB_rel+rlx).

\[
[x]_{rlx} := 0; \quad [y]_{rlx} := 0; \\
r_1 = [y]_{rlx}; \quad r_2 = [x]_{rlx}; \\
[x]_{rel} := 1; \quad [y]_{rel} := 1; \\
\]

Figure 11. Postponed relaxed reads and RA (LB_rel+acq+rlx).

\[
[x]_{rlx} := 0; \quad [y]_{rlx} := 0; \\
[x]_{rel} := 1; \quad [y]_{rel} := 2 \\
r_1 = [x]_{rlx}; \quad r_2 = [y]_{rlx}; \\
\]

Figure 12. Postponed writes and release-writes (WR_rlx+rel).

The problem in Figure 11 is more problematic, as it has release/acquire modifiers on accesses to $y$, and postponing the read $[x]_{rlx}$ in the right thread might lead to $r_1 = r_2 = 1$. Notice that such an outcome is in conflict with the semantics of RA, as assigning $1$ to $r_1$ would imply synchronization between $y_{rel} = 1$ and $r_1 = [y]_{acq}$, thus the former happens before the latter one! Following the rules of RA-synchronization, $r_2 = [x]_{rlx}$ should happen before $[x]_{rlx} = 1$ as well, making it impossible to read $1$ into $r_2$.

To achieve this, we instrument the state with a global list $y$ of triples that consist of: (i) a location $\ell$, (ii) a timestamp $\tau$ of some executed write, and (iii) a symbolic value $x$ of a read postponed beyond this write. When executing a release-write $W$, which stores a value to a location $\ell$ with a timestamp $\tau$, for each thread-local postponed read, we globally record a tripel $\langle \ell, \tau, x \rangle$, where $x$ is the symbolic value of the read. An acquire-read of the $(\ell, \tau)$ history entry by another thread succeeds only if there are no $\langle \ell, \tau, x \rangle$ left in $y$ for any symbolic value $x$. Resolving a postponed read with a symbolic value $x$ removes all $x$-related entries from $y$.

3.6 Putting it all together

As one can notice, almost every aspect of the C11 standard, outlined in Sections 3.1–3.5 requires us to enhance our semantics in one way or another. The good news are that almost all of these enhancements are orthogonal: they can be added to the operational model independently. For instance, one can consider a subset of C11 with RA-synchronization, relaxed and non-atomic accesses, but without accounting for release-sequences or SC-accesses.
4. Operational Semantics, Formally

In this section, we formally describe main components of our operational semantics for C11, starting from the definition of the language, histories and viewfronts, followed by the advanced aspects. The semantics of consume-reads is described in Appendix ??.

4.1 Language syntax and basic reduction rules

The syntax of the core language is presented in Figure ?? The meta-variable \( e \) ranges over expressions, which might be integer numbers \( z \), location identifiers \( \ell \), (immutable) local variables \( x \), pairs, selectors and binary operations. The random choice operator, which non-deterministically returns one of its arguments. At the moment, arrays or pointer arithmetics are not supported.

Programs are statements, represented by terms \( s \), most of which are standard. As customary in operational semantics, the result of a fully evaluated program is either a value \( v \) or the run-time stuck statement, which denotes the result of a program that "went wrong". For instance, it is used to indicate all kinds of undefined behavior, \( e.g. \), data races on non-atomic operations or reading from non-initialized locations. The \( \text{sw} \) \( s_1 \), \( s_2 \), when reduced, spawns two threads with subprograms \( s_1 \) and \( s_2 \) respectively, emitting the run-time statement \( \text{par} \) \( s_1 \), \( s_2 \), which is necessary for implementing dynamic viewfront allocation for the newly forked threads, as will be described below. In our examples, we will use the parallel composition operator \( | \) for both \( \text{sw} \) and \( \text{par} \) statements.

A binding statement \( x = s_1 ; s_2 \), implements sequential composition by means of substituting \( s_1 \) in \( s_2 \) for all occurrences of \( x \). Location-manipulating statements include reading from a location \( ([l]_{\text{inv}}) \), writing \( ([l]_{\text{inv}} := e) \), and compare-and-set on a location \( (\text{cas}_{\text{inv}}(l, e_1, e_2)) \). These statements are annotated with order modifiers. We will sometimes abbreviate \( r_1 = [x]_{\text{inv}} ; [y]_{\text{inv}} := r_2 \) as \( [y]_{\text{inv}} := [x]_{\text{inv}} \) and \( r_1 = s ; r_1 = r_1 = s \).

Meta-variable \( \xi \) ranges over dynamic environments, defined further. Evaluation of a program \( s \) in the semantics starts with the initial state \( s, \xi_{\text{init}} \), where \( \xi_{\text{init}} \) contains an empty history, and an empty viewfront for the only initial thread. The semantics is defined in reduction style [18], with most of its rules of the form

\[
E \Rightarrow E'[\xi']
\]

where \( E \) is a reduction context, defined as follows:

\[
E ::= | | x = E ; s | \text{par} \ E | s | \text{par} \ s \ E
\]

If there is more than one thread currently forked, \( i.e. \), the program expression contains a \( \text{par} \) node, its statement might be matched against \( E[s] \) in multiple possible ways non-deterministically.

\[
\xi' = \text{spawn}(E, \xi) \quad \text{SPAWN}
\]

\[
(E[\text{sw} s_1 s_2], \xi) \Rightarrow (E[\text{par} s_1 s_2], \xi')
\]

\[
\xi' = \text{join}(E, \xi) \quad \text{JOIN}
\]

\[
(E[\text{par} v_1 v_2], \xi) \Rightarrow (E[v_1, v_2], \xi')
\]

Figure 14. Generic rules for spawning and joining threads

The core rules of our semantics, involving non-memory operations, are standard and are presented in Appendix B. The only interesting rules are for spawning and joining threads (Figure 14), as they alter the thread-related information in the environment \( e.g. \), the viewfronts). The exact shape of these rules depends on the involved concurrency aspects, which define the meta-functions spawn and join.

4.2 Histories and Viewfronts

In its simplest representation, the program environment \( \xi \) is a pair, whose components are a history \( H \) and per-thread viewfront function \( \phi^\xi \), defined in Figure 15.

A history \( H \) is a partial function from location identifiers \( \ell \) and timestamps \( \tau \) to pairs of a stored value \( v \) and a synchronization front \( \sigma \). Further aspects of our semantics feature different kinds of fronts, but all of them have the same shape, mapping memory locations to timestamps. Per-thread viewfront function \( \phi^\xi \) maps thread paths \( \pi \) to viewfronts. A thread path is a list of directions \( (1 \mid \tau) \), which shows how to get to the thread subexpression inside a program statement tree through the \( \text{par} \) nodes: it uniquely identifies a thread in a program statement. We use an auxiliary function path in the rules to calculate a path from an evaluation context \( E \).

Once threads are spawned, they inherit a viewfront of their parent thread, hence the simplest spawn function is defined as follows:

\[
\text{spawn}(E, (s, \phi^\xi)) = (s, \phi^\xi(l \mapsto \sigma_{\text{rd}}, \tau \mapsto \sigma_{\text{rd}}))
\]

where \( \pi = \text{path}(E) \), and \( \sigma_{\text{rd}} = \phi^\xi(\pi) \). When threads join, their parent thread gets a viewfront, which is the least upper bound \( (\text{join}) \) of subthread viewfronts:

\[
\text{join}(E, (s, \phi^\xi)) = (s, \phi^\xi(l \mapsto \sigma_{\text{rd}} \cup \sigma_{\text{rd}}))
\]

where \( \pi = \text{path}(E) \), \( \sigma_{\text{rd}} = \phi^\xi(l) \), and \( \sigma_{\text{rd}} = \phi^\xi(\pi, \tau) \), thus, synchronizing the children threads’ views.

We can now define the first class of “wrong” behaviors, corresponding to reading from non-initialized locations (Figure 16). The rules are applicable in the case when a thread tries to read from a location, which it knows nothing about, \( i.e. \), its viewfront is not yet defined for the location, making it uninitialized from the thread’s point of view. This condition is also satisfied if the location is not initialized at all, \( i.e. \), it has no corresponding records in the history.

4.3 Release/Acquire synchronization

The reduction rules for release-write and acquire-read are given in Figure 17. A release-write augments the history with a new entry \( (\ell, \tau) \mapsto (v, \sigma) \), where \( v \) is a value argument of the write, and \( \sigma \) is a synchronization front, which now might be retrieved by the threads reading from the new history entry. The stored front \( \sigma \) is the same
\( \xi = (H, \psi^{rd}) \) \Rightarrow \begin{align*}
\pi &= \text{path}(E) \\
\sigma^{rd} &= \psi^{rd}(\pi) \\
\sigma^{rd}(\ell) &= \bot \quad \text{READ-UNINIT}
\end{align*}
\( \langle \xi[\text{last}] = \ell \rangle \Rightarrow (\text{stuck}, \xi_{\text{init}}) \)
\( \xi = (H, \psi^{rd}) \) \Rightarrow \begin{align*}
\pi &= \text{path}(E) \\
\sigma^{rd} &= \psi^{rd}(\pi) \\
\sigma^{rd}(\ell) &= \bot \quad \text{CAS-UNINIT}
\end{align*}
\( \langle \xi[\text{cas}_{\text{stuck}}(e_1, e_2)] = \ell \rangle \Rightarrow (\text{stuck}, \xi_{\text{init}}) \)

**Figure 16.** Rules for reading from an uninitialized location.

\( \xi = (H, \psi^{rd}) \) \Rightarrow \begin{align*}
\pi &= \text{path}(E) \\
\sigma^{rd} &= \psi^{rd}(\pi) \\
\sigma^{rd}(\ell) &= \bot \\
\xi &= (H, \psi^{rd}) \quad \text{READACQ}
\end{align*}
\( \langle \xi[\text{last}] = \ell \rangle \Rightarrow \langle \xi[v], \xi' \rangle \)

**Figure 17.** Reduction rules for release/acquire atomics.

\( \xi = (H, \psi^{rd}) \) \Rightarrow \begin{align*}
\pi &= \text{path}(E) \\
\tau &= \text{next}(H, \ell) \\
\sigma^{rd} &= \psi^{rd}(\pi) \\
\sigma^{rd}(\ell) &= \tau \\
\xi' &= (H[\ell, \tau] \rightarrow (v, \sigma)) \\
\xi &= (H, \psi^{rd}) \quad \text{WRITEREL}
\end{align*}
\( \langle \xi[\text{last}] = \ell \rangle \Rightarrow \langle \xi[v], \xi' \rangle \)

**Figure 18.** Reduction rules for SC atomics.

as the viewfront of the writer thread after having stored the value, 
i.e., featuring updated \( \ell \)-entry with the new timestamp \( \tau \).

An acquire-read is more interesting. It is non-deterministically 
chooses, from the global history, an entry \( (\ell, \tau) \rightarrow (v, \sigma) \), 
with a timestamp \( \tau \) which is at least a new as the timestamp \( \tau' \) 
for the corresponding location \( \ell \) in the thread’s viewfront \( \sigma^{rd} \) (i.e., 
\( \tau' \leq \tau \)). The value \( v \) replaces the read expression inside the context \( E \), 
and the thread’s local viewfront \( \sigma^{rd} \) is updated via the retrieved 
synchronization front \( \sigma \). The RA-CAS operations (rules omitted 
for brevity) behave similarly with only difference: a successful 
CAS reads from the latest entry in the history.

### 4.4 SC operations

To account for SC operations, we augment \( \xi \) with sc-front:

\[ \xi := (\ldots, \sigma^{sc}) \]

that maps each location to a timestamp of the latest entry in the location history, which has been added by a SC-write.

The SC operations update the history and local/stored fronts similarly to RA atoms. In addition, an SC-write updates sc-front, 
and an SC-read introduces an additional check for the timestamp \( \tau \), 
taking max of two viewfronts, as defined in Figure 18.\(^2\) That is, the 
rule \( \text{READSC} \) ensures that an SC-read gets a history entry, which is 
not older than the one added by the last SC write to the location.

### 4.5 Non-atomic operations

For non-atomic accesses we augment \( \xi \) with na-front:

\[ \xi := (\ldots, \sigma^{na}) \]

Similarly to sc-front, it maps a location to the latest corresponding 
na-entry in the history, and it is updated by NA-writes.

\(^2\)Read and write rules only depict difference with the release/acquire ones.

The real purpose of na-front is to detect data races involving 
NA-operations as defined in Figure 19. When a thread performs 
NA-write or NA-read (see \( \text{WRITNA, READNA rules} \)), it must be 
aware of the latest stored record of the location (i.e., it should match 
the timestamp in its local front \( \sigma^{rd} \)). Violating this side condition 
is condemned to be a data race and leads to undefined behavior 
(\( \text{READNA-stuck1} \)). In addition, if a thread performs \( \text{any} \) write 
or read from a location, it should be aware of the latest NA-record 
to the location (see the side condition \( \sigma^{rd}(\ell) < \alpha^{na}(\ell) \) in the rule 
\( \text{READNA-stuck2} \)). The stuck-cases reflect the cases when a write 
or a read is in data race with the last NA-write to the location.

Unlike release or SC-writes, NA-writes do not store a front to 
the history entry, as they cannot be used for synchronization. A similar 
fact holds for NA-reads: they do not get a stored front from the 
history entry, upon reading from it.

### 4.6 Release-sequences and write-fronts

Relaxed reads do not update their thread’s viewfront with a syn-
chronization front from the history (see \( \text{READLX} \) rule in Figure 20). 
At this stage, their support does not require augmenting the state. 
An additional instrumentation is required, though, to encode 
release sequences. As discussed in Section 3.5, an acquire-read, 
when reading the result of a relaxed write, might get synchronized 
with a release-write to the same location performed earlier by the 
same writer thread. To account for this, we introduce pre-thread

\(^3\)Rules \( \text{WRITENA-stuck1} \) and \( \text{WRITENA-stuck2} \) are similar and can be 
found in Appendix B.
write-front function $\psi^{WR}$ as an environment component:

$$\xi := \langle \ldots, \psi^{WR} \rangle$$

It is similar to the viewfront function $\psi^{VD}$, but it stores a timestamp of the last release-write to a location by the thread. Specifically, when a thread performs a relaxed write $W$ (see rule $\text{Write-Relaxed}$ in Figure 20), it checks if there was a release-write $W'$ performed by it earlier, takes a synchronization front $\sigma_{sync}$ from the history entry, added by $W'$, and stores it as the synchronization front in the new history entry.\footnote{If $H(\ell, \tau_{col}) = \bot$ then $\sigma_{sync} = \bot$.} Additionally, we need to modify the old rules $\text{WriteRel}$, $\text{WriteSet}$, CAS-Rel, etc., so they update $\psi^{WR}$ correspondingly (e.g., see rule $\text{WriteRel'}$ in Figure 20).

We also need to change our meta-functions, in order to account for the $\psi^{WR}$ component of the state environment:

$$\text{spawn}(E, \langle \ldots, \psi^{WR} \rangle) = \langle \ldots, \psi^{WR}[\pi \mapsto \downarrow, \pi \mapsto \downarrow] \rangle$$

$$\text{join}(E, \langle \ldots, \psi^{WR} \rangle) = \langle \ldots, \psi^{WR}[\pi \mapsto \downarrow] \rangle$$

Sub-threads do not inherit write-fronts upon spawning, and a parent thread does not inherit the joined one, since the described synchronization effects via relaxed writes and release sequences do not propagate through spawn/join points according to the model [7].

4.7 Postponed operations and specifications

To support postponed operations (or, equivalently, speculative executions) we instrument the state with two additional components:

$$\xi := \langle \ldots, \psi, \gamma \rangle$$

The main one, $\psi$, is a function that maps a thread path $\pi$ to a per-thread hierarchical buffer $\alpha$ of postponed operations $\beta$:

$$\psi := \pi \mapsto \alpha$$

$$\alpha := \beta^*$$

$$\beta := \text{read}(x, \ell, RM) \mid \text{write}(x, \ell, WM, e) \mid \text{bind}(x, e) \mid \text{if}(x, e, \alpha, a, a')$$

Each operation $\beta$ is uniquely identified by its symbolic value $x$. Read entries contain a (possibly unresolved) location $\ell$ to read from as well as a read modifier $RM$. Write entries additionally contain an expression $e$ to be stored to the location. Bind entries are used to postpone calculation of an expression depending on a symbolic value, making it possible to postpone the reads as follows:

$$r_1 = [x]_{rel}; r_2 = r_1 + 1; \ldots$$

Both reads $r_1$ and bind $r_2$ might be postponed, so the second statement will not "trigger" evaluation of the first one. If-entries have a conditional expression $e$ and two subbuffers $a$ and $a'$ representing operations speculatively put to the buffer under $\text{then}$ and $\text{else}$ branches. To represent speculation under (possibly nested) if statements we define an if-specified reduction context $\text{Env}$ as follows:

$$\text{Env} ::= \text{if } e \text{ then Env else } f\downarrow \mid \text{Env}$$

where the symbolic value $x$ in the condition is the same as in the corresponding buffer entry $e(x, a_1, a_2)$. The list of symbolic values from conditions of the context can be used to uniquely identify an operation buffer inside an hierarchical per-thread buffer $\alpha$.

The list $\gamma$ encodes Acquire-Read Restrictions by containing triples ($\ell, \tau, x$), forbidding to acquire-read from ($\ell, \tau$) until $x$ is not resolved.

During a thread execution, any read, write, or bind operation (including those under not fully reduced if-branches) can be postponed by the semantics by adding a corresponding record into the matching subbuffer of the thread buffer $\alpha$. For the sake of brevity we discuss only write rules here; other rules can be found in the appendix and in our implementation.

The postpone-rules append operation records into the corresponding buffer $\psi$. An operation to be postponed can be nested under a not fully reduced if statement.
with various C11 concurrency aspects (Sections 4.3–4.7) implemented on top of them, in 1310 LOC. Implementation of litmus tests (Section 5) and case studies (Section 6) took 3130 LOC.

**Evaluation via Litmus Tests** To ensure the adequacy of our semantics with respect to the C++11 standard [2] and gain confidence in its implementation, we evaluated it on a number of litmus test programs from the literature. For each test, we encoded the set of expected results and checked, via extensive state-space enumeration, provided by PLT Redex, that these are the only outcomes produced.

Figure 21 provides a table, relating specific litmus tests from the literature [7, 9, 26, 29, 45] to the relevant aspects of our semantics from Section 4, required in order to support their desired behavior. All tests mentioned before in the paper are presented in the table. Since there is no common naming conventions for litmus tests in a high-level language, making consistent appearance in related papers, we supplied ours with meaningful names, grouping them according to the behavioral pattern they exercise (e.g., message-passing, store buffering, etc.). Exact definitions of the test program and descriptions of their behaviors can be found in Appendix A.

All tests within the same group have a similar structure but differ in memory access modifiers. The columns Hst–JN in Figure 21 show which semantic aspects a test requires for its complete and correct execution. The last column indicates, whether the test’s behavior in our semantics matches fully its outcome according to the C11 standard or not. Below, we discuss the tests that behave differently in the C11 standard and in our semantics.

**Discrepancies with the C11 standard** The combining relaxed and acquire-writes, LB_{acq+rlx,acq+rlx+join}, in order to adhere to the “canonical” C11 behavior, require an ability to do an acquire-read and a subsequent relaxed write out-of-order. Even though the relaxed behavior of this kind is not supported by our semantics, it is not observable under sound compilation schemes of acquire-read to the major architectures [1]: (i) load buffering is not observable on x86 in general [42], (ii) all barriers (sync, bsync, ctrl+isync) forbid reorderings of read and write on Power [4], (iii) as well as barriers (dmby, dmb ld, ctrl+isb) on ARM [19].

Our semantics rules out OTA behaviors (tests OTA_{lb, if}), which are considered to be an issue of the standard [5, 8, 38].

## 6. Case Study: Read-Copy-Update

We showcase our implementation by testing and debugging a Read-Copy-Update structure (RCU) [31, 34] and its client programs.

### 6.1 RCU: background and implementation

Read-Copy-Update is a standard way to implement non-blocking sharing of a linked data structure (e.g., list or a tree) between single writer and multiple readers, running concurrently. For our purposes, we focus on RCU for a singly linked list, implemented via Quiescent State Based Reclamation (QSBR) technique [14]. The central idea of RCU is the way the writer treats nodes of the linked structure. Specifically, instead of in-place modification of a list node, the writer creates a copy of it, modifies the copy, updates the link to the node, making the older version inaccessible, and then waits until all readers stop using the older version, so it could be reclaimed. The crux of the algorithm’s correctness is a fine-grained synchronization between the writer and the readers: the writer updates the link via release-write, and the readers must traverse the list using an acquire-read for dereferencing its nodes, ensuring that readers will not observe partially modified nodes.

A QSBR RCU implementation and its client program are shown in Figure 22. The first line in the top of the figure initializes thread counters, which are used by the reader threads to signal if they use the list or not (i.e., they are in a quiescent state), and a pointer to the list (lhead), which is going to be shared between the threads. Next, three threads are spawned: a writer and two readers. The writer thread on the left appends 1, 10, and 100 to the list. A call to append creates a new node and adds a link from the current last node to the new one via relaxed write to ltail. The updating write to the last node [rt] is a release one, guaranteeing that a reader thread, which might be observing the added node pointer via an acquire-read in concurrent traverse call, will become aware of the value and

| Test name |VF |WF |SCF |NAF |PO |ARR |CR |JN |C11 |
|-----------|----|----|-----|-----|----|-----|----|----|----|
| rel+acq   | ✓  |    |     |     |     |     |    |    |    |
| sc         | ✓  | ✓  | ✓   |     |     |     |    |    |    |
| sc+rel     | ✓  | ✓  | ✓   |     |     |     |    |    |    |
| sc+acq     | ✓  | ✓  | ✓   |     |     |     |    |    |    |
| rlx        | ✓  | ✓  | ✓   | ✓   | ✓  | ✓   | ✓  | ✓  | ✓  |
| rel+rlx    | ✓  | ✓  | ✓   | ✓   | ✓  | ✓   | ✓  | ✓  | ✓  |
| acq+rlx    | ✓  | ✓  | ✓   | ✓   | ✓  | ✓   | ✓  | ✓  | ✓  |
| rel+acq+rlx| ✓  | ✓  | ✓   | ✓   | ✓  | ✓   | ✓  | ✓  | ✓  |
| rlx+use    | ✓  | ✓  | ✓   | ✓   | ✓  | ✓   | ✓  | ✓  | ✓  |
| rlx+let    | ✓  | ✓  | ✓   | ✓   | ✓  | ✓   | ✓  | ✓  | ✓  |
| rlx+join   | ✓  | ✓  | ✓   | ✓   | ✓  | ✓   | ✓  | ✓  | ✓  |
| rel+rlx+join| ✓ | ✓  | ✓   | ✓   | ✓  | ✓   | ✓  | ✓  | ✓  |
| acq+rlx+join| ✓ | ✓  | ✓   | ✓   | ✓  | ✓   | ✓  | ✓  | ✓  |

**Figure 21.** Litmus tests (Appendix A) and corresponding semantic aspects of our framework: viewfronts (VF, §2.1), write-fronts (WF, §4.6), SC-fronts (SCF, §3.1), non-atomic fronts (NAF, §3.2), postponed operations (PO, §4.7), acquire read restrictions (γ) (ARR, §4.7), consume-reads (CR), joining threads with non-empty operation buffers (JN, §3.4). The column C11 indicates whether the behavior is coherent with the C11 standard.

In the absence of implemented allocation, the example uses the fixed locations a, b, and c for storing nodes of the list.
link data, stored to the node. This release/acquire synchronization eliminates a potential data race.

At the end, the writer thread changes the second value in the list, 10, to 1000. In the corresponding updateSecondNode routine, first five commands get pointers to first, second, and third list nodes. The next two commands create a new node with value stored in it, and update the corresponding link in the previous node (i.e., the first one). By executing sync(cw, cr1, cr2), the writer checks that the reader threads no longer use an older version of the list (with 10), so, once the check succeeds, the old node can be reclaimed.

The reader threads calculate two times the sum of the list’s elements by traversing the list. Before and after each traversal they call rcuOnline and rcuOffline routines respectively to signal to the writer about their state.

6.2 Additional infrastructure for testing RCU

Having an executable operational semantics gives us a possibility to run a dynamic analysis of the RCU and its client, exercising all possible executions. Realistically, running such an analysis would take forever, because of the size of the program state-space. The state-space explosion is because of the following three reasons:

1. Non-determinism due to concurrent thread scheduling;
2. Resolution of postponed operations;
3. Loading any value, which is newer than the one in the thread’s viewfront representation of the reading location.

Indeed, our semantics accounts for all combinations of the factors above, exploring all possible execution traces.

Randomized semantics In order to make dynamic analysis practically feasible, we implemented a semantics, which non-deterministically chooses a random path in the program state space of the original semantics. It does so by applying semantic rules to the current state getting a set of new states, checks if there is a stuck state, and randomly chooses the next state from the set. The presence of the randomized semantics makes possible to implement property-based testing of executions [22].

Deallocation As an additional aspect, we added delete operator to the language for reclaiming retired nodes in RCU, and extended the state by a global list of reclaimed locations. That is, if a location is added to the “retired” list, any read or write on it will lead to the stuck state, indicating accessing a deallocated pointer.

6.3 Testing and debugging the RCU implementation

We can now run some random tests on our RCU implementation and see whether it meets the basic safety requirements. In particular, we can check that no matter what path is being exercised by the randomized semantics, the execution of the program does not get stuck. In our experience, this correctness condition held for the implementation in Figure 22 for all test runs.

Next, we intentionally introduced a synchronization bug into our implementation. In particular, we removed from the implementation syncWithReader loops (see grayed code fragments), which were used to synchronize the writer with the readers. Additionally, we considered the following correctness criteria: (i) the values of r11, r12, r21, and r22 must be in [0, 1, 11, 111, 1101]; this guarantees that the list is read correctly, and, (ii) it should be the case that by the end r11 ≤ r12 ∧ r21 ≤ r22, i.e., second list traversals see the list at least as up to date as the first ones.

We ran the test twenty times on Core i7 2.5GHz Linux machine with 8 GB RAM. Despite the large number of states to visit, all runs terminated in less than 27 seconds, and did not violate the desired criteria of correctness with respect to r+ invariants.\(^7\) In the

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\(^7\)The table with run results is in appendix, Figure 27.
absence of intentionally removed active wait loops, non-guarded deallocation has lead to stuck state in four out of twenty runs.

Can one implement the RCU with weaker order modifiers? To check this hypothesis, we changed release write $[r_{\text{t}}]_{\text{loc}} := \langle \text{fst} \text{ etc.} \text{ loc} \rangle$ in append to a relaxed one, which resulted in 8 out of 10 test runs getting stuck, even without deallocation after update in the writer. We then changed only $[\text{head}]_{\text{loc}} := \text{a in the writer to a relaxed version, which led to 10 out of 10 test runs ending up in the stuck state, as these changes break synchronization between the writer and the reader threads. The same results are observed when changing acquire-reads to relaxed ones in traverse. Without the enforced RA-synchronization, the reader threads do not get their viewfronts updated with writes to locations a-d, so attempts to read from them result in stuck state, according to Read-Uninit rule.

As our semantics is implemented in PLT Redex, these synchronization bugs are easy reproduce: if a program gets stuck or delivers unexpected results, one can retrieve the corresponding execution trace via standard Redex machinery.

**RCU via consume-reads** The original implementation of the RCU used consume-reads instead of acquire-reads. Our version of RCU employs release/acquire synchronization for the following reason. Currently, our semantics does not support mutable local variables, as we did not need them for running litmus tests. In their absence, the only possible way to transfer a pointer’s value to the next iteration of a loop is to store it in some location, as it is currently done in the repeat-loop of traverse. The downside of using a proper memory location instead of a local variable is that this breaks data-dependency chain, which is required by consume-reads for synchronization. There are no fundamental problems preventing us from adding mutable variables to make proper use of consume-reads, and we plan to do it in the future.

7. Related Work

**Existing semantics for C11 and their variations** The axiomatic C11 semantics by Batty et al. [7] has been adapted for establishing soundness of several program logics for relaxed memory [15,27,45,49]. While some of these adaptations bear a lot of similarity with operational approach [45], all of them are still based on the notion of partial orders between reads and writes. The recent operational semantics for C11 took steps to incrementallyize Batty et al.’s model, constructing the partial orders in a step-wise manner, checking the consistency axioms at every execution step [36]. This model does not follow the program execution order and allows OTA behaviors.

The semantics for Strong Release-Acquire (SRA) model by Lahav et al. [26] does not use graphs and consistency axioms, relying instead on message buffers, reminiscent to our viewfronts in the way they are used for thread synchronization in our approach. However, Lahav et al.’s semantics only targets a (strengthened) subset of C11, restricted to release/acquire-synchronization, thus, sidestepping the intricacies of encoding the meaning of relaxed atomics.

**Operational semantics for relaxed memory models** A low-level operational model for the total store order (TSO) memory model, which is stronger than C11, has been defined by Owens et al., targeting x86-64-TSO processors [37]. A more complex model is tackled by Sarkar et al., who provided an operational semantics for the POWER architecture [40]. Finally, the most recent work by Flur et al. provides an operational model for the ARMv8 architecture [19]. While in this work we are concerned with semantics of a high-level language (i.e., C/C++), investigating compilation schemes to those low-level models with respect to our semantics is our immediate future work.

Related proposals with respect to operational semantics for relaxed memory, inspired by the TSO model, are based on the idea of write-buffers [10, 11, 16, 23], reminiscent to the buffers we use to define postponed operations in our approach. The idea of write buffers and buffer pools fits operational intuition naturally and was used to prove soundness of a program logic [43], but it is not trivial to adapt for C11-style synchronization, especially for reconciling RA-synchronization and relaxed atomics, as we demonstrated in Sections 3 and 4. An alternative approach to define relaxed behavior is to allow the programmer to manipulate with synchronization orders explicitly via program-level annotations [13]. This approach provides a highly generic way of modelling custom synchronization patterns at atomic accesses, although, it does not correspond to any specific standard and is not executable. Due to the intentional possibility to use it for modelling very “relaxed” behaviors via arbitrary speculations, the approach allows OTA behaviors. In contrast, our semantics, tailored to allow for modelling all essential concurrent features of C11, prevents OTA by careful treatment of operation buffers, and is executable.

**Semantics for relaxed atomics via event structures** The OTA executions are considered a serious issue with the C++ standard [5, 8, 32], in particular, because there is no well-stated and uniform definition of this phenomenon, which is only characterized in the folklore as “values appearing out of nowhere”.

At the moment, several proposals provide treatment for relaxed atomics, avoiding the OTA behavior by presenting models for relaxed-synchronization and relaxed-atomic event structures [24, 38]. These models allow aggressive optimizations including value-range speculations, without introducing classic out-of-thin-air behaviors. Our semantics does not support all of these compiler transformations yet, (e.g., speculative calculation of an arithmetic expression with symbolic values), but they can be added as additional rules without changing the underlying program state. In contrast with our semantics, the model of Pichon-Parabod and Sewell [38] is not realistically executable, as it requires for every read operation in a program execution to consider $N$ events, where $N$ is a size of the value domain. That is, for instance, for reading a 32-bit integer it is $2^{32}$. Furthermore, at the moment the model [38] does not account for release/acquire-synchronization.

The model by Jeffrey and Riely [24] does not allow for reorderings of independent reads, which makes it too strong to be efficiently implemented on such architectures Power and ARM. The authors suggest a fix for it, which, however, invalidates some other guarantees their initial proposal provides.

**Reasoning about Read-Copy-Update** RCU structures have been used recently to showcase program logics [27, 44], semantic frameworks [26], and program repair/synthesis methods [35] in the context of C11 concurrency. To the best of our knowledge, no other existing approach provides a way of efficiently debugging them by means of re-tracing executions, exhibiting synchronization issues, as we demonstrated in Section 6.3.

8. Conclusion and Future Work

In this work, we presented a family of operational semantics for modelling C/C++ concurrency features. The encoding of C11-style semantics in our framework is based on the two main ideas: viewfronts and operation buffers, with their various combinations and elaborations allowing to express specific synchronization mechanisms and language aspects from the C11 standard. Our C11 semantics is executable, which we demonstrated by implementing it in PLT Redex and showcasing with a number of examples.

As our future work, we plan to extend the defined formalism for C11 fences [15] and establish formal results relating executions in our semantics to executions in low-level languages via standard compilation schemes [19, 40, 42], thus, proving that our semantics is weak enough to accommodate them. Next, we are going to employ it as a basis for developing a higher-order program logic
for establishing Hoare specifications and program refinement in the C11 model [47], proving the logic’s soundness with respect to our semantics, lifted to sets of traces [12] or logical relations [46]. Finally, we plan to use our operational framework for exploring the ideas of efficiently synthesizing synchronization primitives via bounded model checking [35] and partial order reduction [20].

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### A. The Catalogue of Litmus Tests

#### A.1 Store Buffering (SB)

| SB_rel+acq | Possible outcomes: | Requires: Postponed Reads + History + Viewfronts |
|------------|-------------------|-----------------------------------------------|
| Fully Supported: ✓ | $r_1 = 0 \land r_2 = 0$ | $x_{rel} := 0; \; y_{rel} := 0; \; y_{acq} := 0$ |
| Requires: History | $r_1 = 0 \land r_2 = 1$ | $y_{rel} := 1; \; r_1 = [y_{acq)]; \; r_2 = [x_{acq}]$ |
| Viewfronts | $r_1 = 1 \land r_2 = 0$ |                                         |
|            | $r_1 = 1 \land r_2 = 1$ |                                         |

| SB_sc     | Forbidden outcomes: | Requires: SC + History + Viewfronts |
|-----------|-------------------|-----------------------------------------------|
| Fully Supported: ✓ | $x_{sc} := 0; \; y_{sc} := 0$ | $x_{sc} := 1; \; y_{sc} := 1$ |
| Requires: SC + History | $r_1 = [y_{acq}]; \; r_2 = [x_{acq}]$ |                                         |
| Viewfronts | $r_1 = 0 \land r_2 = 0$ |                                         |
|            | $r_1 = 0 \land r_2 = 1$ |                                         |

| SB_sc+rel | Possible outcomes: | Requires: SC + History + Viewfronts |
|-----------|-------------------|-----------------------------------------------|
| Fully Supported: ✓ | $x_{sc} := 0; \; y_{sc} := 0$ | $x_{sc} := 1; \; y_{sc} := 1$ |
| Requires: SC + History | $r_1 = [y_{acq}]; \; r_2 = [x_{acq}]$ |                                         |
| Viewfronts | $r_1 = 0 \land r_2 = 0$ |                                         |
|            | $r_1 = 0 \land r_2 = 1$ |                                         |

| SB_sc+acq | Possible outcomes: | Requires: SC + History + Viewfronts |
|-----------|-------------------|-----------------------------------------------|
| Fully Supported: ✓ | $x_{sc} := 0; \; y_{sc} := 0$ | $x_{sc} := 1; \; y_{sc} := 1$ |
| Requires: SC + History | $r_1 = [y_{acq}]; \; r_2 = [x_{acq}]$ |                                         |
| Viewfronts | $r_1 = 0 \land r_2 = 0$ |                                         |
|            | $r_1 = 0 \land r_2 = 1$ |                                         |

#### A.2 Load Buffering (LB)

| LB_rlx | Possible outcomes: | Requires: Postponed Reads + History + Viewfronts |
|--------|-------------------|-----------------------------------------------|
| Fully Supported: ✓ | $x_{rlx} := 0; \; y_{rlx} := 0;$ | $x_{rlx} := 1; \; y_{rlx} := 1$ |
| Requires: History | $r_1 = [y_{rlx}]; \; r_2 = [x_{rlx}]$ |                                         |
| Viewfronts | $r_1 = 0 \land r_2 = 0$ |                                         |
|            | $r_1 = 0 \land r_2 = 1$ |                                         |

| LB_rel+rlx | Possible outcomes: | Requires: Postponed Reads + History + Viewfronts |
|------------|-------------------|-----------------------------------------------|
| Fully Supported: ✓ | $x_{rlx} := 0; \; y_{rlx} := 0;$ | $x_{rlx} := 1; \; y_{rlx} := 1$ |
| Requires: History | $r_1 = [y_{rlx}]; \; r_2 = [x_{rlx}]$ |                                         |
| Viewfronts | $r_1 = 0 \land r_2 = 0$ |                                         |
|            | $r_1 = 0 \land r_2 = 1$ |                                         |

| LB_rel+rlx | Possible outcomes: | Requires: Postponed Reads + History + Viewfronts |
|------------|-------------------|-----------------------------------------------|
| Fully Supported: ✓ | $x_{rlx} := 0; \; y_{rlx} := 0;$ | $x_{rlx} := 1; \; y_{rlx} := 1$ |
| Requires: History | $r_1 = [y_{rlx}]; \; r_2 = [x_{rlx}]$ |                                         |
| Viewfronts | $r_1 = 0 \land r_2 = 0$ |                                         |
|            | $r_1 = 0 \land r_2 = 1$ |                                         |

| LB_acq+rlx | Possible outcomes: | Requires: Postponed Reads + History + Viewfronts |
|------------|-------------------|-----------------------------------------------|
| Fully Supported: ✓ | $x_{rlx} := 0; \; y_{rlx} := 0;$ | $x_{rlx} := 1; \; y_{rlx} := 1$ |
| Requires: History | $r_1 = [y_{rlx}]; \; r_2 = [x_{rlx}]$ |                                         |
| Viewfronts | $r_1 = 0 \land r_2 = 0$ |                                         |
|            | $r_1 = 0 \land r_2 = 1$ |                                         |

Our semantics doesn’t allow the $r_1 = 1 \land r_2 = 1$ outcome for the program. It doesn’t allow reordering of an acquire read with a subsequent write. The known sound compilation schemes of acquire read to major platforms (x86, ARM, Power) don’t allow the behavior either.

| LB_rel+acq+rlx | Forbidden outcomes: | Requires: Postponed Reads + History + Viewfronts |
|---------------|-------------------|-----------------------------------------------|
| Fully Supported: ✓ | $x_{rlx} := 0; \; y_{rlx} := 0;$ | $x_{rlx} := 1; \; y_{rlx} := 1$ |
| Requires: History | $r_1 = [y_{rlx}]; \; r_2 = [x_{rlx}]$ |                                         |
| Viewfronts | $r_1 = 1 \land r_2 = 1$ |                                         |

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| **LB_rel+use** | Allowed outcome: |
|---------------|----------------|
| Fully Supported: ✓ | \( r_1 = 1 \land r_2 = 1 \) |
| Requires: Postponed Reads + History + Viewfronts |
| \([x]_{rel} := 0; \) | \([y]_{rel} := 0; \) |
| \( r_1 = [y]_{rel}; \) | \( r_2 = [x]_{rel}; \) |
| \([z1]_{rel} := r_1; \) | \([z2]_{rel} := r_2; \) |
| \([x]_{rel} := 1 \) | \([y]_{rel} := 1 \) |

| **LB_rel+let** | Allowed outcome: |
|---------------|----------------|
| Fully Supported: ✓ | \( r_1 = 1 \land r'1 = 2 \land r_2 = 1 \land r'2 = 2 \) |
| Requires: Postponed Reads + History + Viewfronts + IN |
| \([x]_{rel} := 0; \) | \([y]_{rel} := 0; \) |
| \( r_1 = [y]_{rel}; \) | \( r_2 = [x]_{rel}; \) |
| \([z1]_{rel} := r_1 \) | \([z2]_{rel} := r_2 \) |
| \([x]_{rel} := 1 \) | \([y]_{rel} := 1 \) |

| **LB_acq+rel+join** | Allowed outcomes: |
|---------------------|------------------|
| Fully Supported: ✓ | \( r_1 = 1 \land r_2 = 1 \) |
| Requires: Postponed Reads + History + Viewfronts + IN |
| \([x]_{rel} := 0; \) | \([y]_{rel} := 0; \) |
| \( r_1 = [y]_{acq}; \) | \( r_2 = [x]_{rel}; \) |
| \([z1]_{rel} := r_1 \) | \([z2]_{rel} := r_2 \) |
| \([x]_{rel} := 1 \) | \([y]_{rel} := 1 \) |

### A.3 Message Passing (MP)

#### MP_rel+na

| Possible outcomes: |
|---------------------|
| Fully Supported: ✓ | \( r_1 = 0 \) |
| Requires: NA + History + Viewfronts + stuck |
| \([f]_{rel} := 0; \) | \([d]_{na} := 0; \) |
| \([d]_{na} := 5; \) | \( \text{repeat } [f]_{rel}; \) |
| \([f]_{rel} := 1 \) | \( r_1 = [d]_{na} \) |

#### MP_rel+na+acq

| Possible outcomes: |
|---------------------|
| Fully Supported: ✓ | \( r_1 = 0 \) |
| Requires: NA + History + Viewfronts + stuck |
| \([f]_{rel} := 0; \) | \([d]_{na} := 0; \) |
| \([d]_{na} := 5; \) | \( \text{repeat } [f]_{acq}; \) |
| \([f]_{rel} := 1 \) | \( r_1 = [d]_{na} \) |

#### MP_rel+acq+na

| Possible outcomes: |
|---------------------|
| Fully Supported: ✓ | \( r_1 = 0 \) |
| Requires: NA + History + Viewfronts + stuck |
| \([f]_{rel} := 0; \) | \([d]_{na} := 0; \) |
| \([d]_{na} := 5; \) | \( \text{repeat } [f]_{acq}; \) |
| \([f]_{rel} := 1 \) | \( r_1 = [d]_{na} \) |

#### MP_rel+acq+na+rlx

| Possible outcomes: |
|---------------------|
| Fully Supported: ✓ | \( r_1 = 5 \) |
| Requires: NA + History + Viewfronts + Write-fronts |
| \([f]_{rel} := 0; \) | \([d]_{na} := 0; \) |
| \([d]_{na} := 5; \) | \( \text{repeat } [f]_{acq}; \) |
| \([f]_{rel} := 1; \) | \( r_1 = [d]_{na} \) |
| \([f]_{rel} := 2 \) | \( r_1 = [d]_{na} \) |
A.4 Coherence of Read-Read (CoRR)

**CoRR_rlx**

Impossible outcomes:

| r1 = 1 \land r2 = 2 \land r3 = 2 \land r4 = 1 | [x]_{rlx} := 0; | [y]_{rlx} := 0; | r2 \rightarrow [x]_{rlx}; | r2 \rightarrow [y]_{rlx}; | r3 \rightarrow [x]_{rlx}; | r4 \rightarrow [y]_{rlx} |
|---|---|---|---|---|---|---|

**CoRR_rel+acq**

Impossible outcomes:

| r1 = 1 \land r2 = 2 \land r3 = 2 \land r4 = 1 | [x]_{rel} := 1; | [y]_{rel} := 1; | r1 \rightarrow [x]_{acq}; | r2 \rightarrow [y]_{acq}; | r3 \rightarrow [x]_{acq}; | r4 \rightarrow [y]_{acq} |

A.5 Independent Reads of Independent Writes (IRI\-W)

**IRI\_rlx**

Possible outcomes:

| r1 = <0, 1>; r2 = <0, 1>; | [x]_{rlx} := 0; | [y]_{rlx} := 0; | r2 \rightarrow [x]_{rlx}; | r2 \rightarrow [y]_{rlx}; | r3 \rightarrow [x]_{rlx}; | r4 \rightarrow [y]_{rlx} |

Comment: It is possible to get r1 = 1; r2 = 0; r3 = 1; r4 = 0

**IRI\_rel+acq**

Possible outcomes:

| r1 = <0, 1>; r2 = <0, 1>; | [x]_{rel} := 1; | [y]_{rel} := 1; | r1 \rightarrow [x]_{acq}; | r2 \rightarrow [y]_{acq}; | r3 \rightarrow [x]_{acq}; | r4 \rightarrow [y]_{acq} |

Comment: It is possible to get r1 = 1; r2 = 0; r3 = 1; r4 = 0
A.6 Write-to-Read Causality (WRC)

### WRC_rel+acq

| Forbidden outcomes: | \( x_{rel} := 0; \quad y_{rel} := 0; \) |
|---------------------|-----------------------------------------|
| \( r2 = 1 \land r3 = 0 \) | \( x_{rel} := 1; \quad y_{rel} := r1 \) |

### WRC_rlx

| Possible outcomes: | \( x_{rlx} := 0; \quad y_{rlx} := 0; \) |
|--------------------|-----------------------------------------|
| \( r2 = 0 \land r3 = 0 \) | \( x_{rlx} := 1; \quad r2 = [x_{rlx}] \) |

### WRC_cas+rel

| Impossible outcomes: | \( x_{cas} := 0; \quad y_{cas} := 0; \) |
|----------------------|-----------------------------------------|
| \( r2 = 0 \land r3 = 0 \) | \( x_{cas} := 1; \quad r2 = [x_{cas}] \) |

### WRC_cas+rlx

| Impossible outcomes: | \( x_{cas} := 0; \quad y_{cas} := 0; \) |
|----------------------|-----------------------------------------|
| \( r2 = 0 \land r3 = 0 \) | \( x_{cas} := 1; \quad r2 = [x_{cas}] \) |

A.7 Out-of-Thin-Air reads

In our semantics it is not possible to get out-of-thin-air results, unlike the C11 standard. But such reads are considered to be an undesirable behavior by most of the standard’s clients [5].

### OTA_if

| Possible outcomes: | \( x_{if} := 0; \quad y_{if} := 0; \) |
|--------------------|-----------------------------------------|
| \( r1 = 0 \land r2 = 0 \) | \( x_{if} := r1; \quad y_{if} := r2 \) |

Comment: According to the C11 standard [2, 3], \( r1 \) and \( r2 \) can get arbitrary values.

### OTA_if

| Possible outcomes: | \( x_{if} := 0; \quad y_{if} := 0; \) |
|--------------------|-----------------------------------------|
| \( r1 = 0 \land r2 = 0 \) | \( x_{if} := r1; \quad y_{if} := r2 \) |

Comment: According to the C11 standard [2, 3], \( r1 \) and \( r2 \) can be 1s at the end of execution.

A.8 Write Reorder (WR), or 2+2W from [26]

### WR_rlx

| Possible outcomes: | \( x_{rlx} := 0; \quad y_{rlx} := 0; \) |
|--------------------|-----------------------------------------|
| \( r1 = 1 \land r2 = 2 \) | \( x_{rlx} := 1; \quad y_{rlx} := 1; \) |

Comment: According to the C11 standard [2, 3], \( r1 \) and \( r2 \) can be 1s at the end of execution.
WR_rlx+rel  Possible outcomes:
Fully Supported: ✓ r₁ = 1 ∧ r₂ = 2
Requires: History + r₁ = 2 ∧ r₂ = 1
Viewfronts + Operational Buffers r₁ = 2 ∧ r₂ = 2
[x]_{rel} := 0; [y]_{rel} := 0;
[y]_{rlx} := 0;
r₁ = [x]_{rlx}; r₂ = [y]_{rlx}

WR_rel  Possible outcomes:
Fully Supported: ✓ r₁ = 1 ∧ r₂ = 2
Requires: History + r₁ = 2 ∧ r₂ = 1
Viewfronts + Operational Buffers r₁ = 2 ∧ r₂ = 2
[x]_{rel} := 0; [y]_{rel} := 0;
[y]_{rel} := 1; [x]_{rel} := 1;
[y]_{rel} := 2; [x]_{rel} := 2
r₁ = [x]_{acq}; r₂ = [y]_{acq}

A.9 Speculative Execution

SE_simple  Possible outcomes:
Fully Supported: ✓ r₀ = 0
Requires: r₀ = 1
[x]_{rel} := 0; [y]_{rel} := 0; [z]_{rel} := 0;
[x]_{rlx} := 0; [y]_{rlx} := 0; [z]_{rlx} := 0;
r₁ = [x]_{rlx};
if r₁ then [z]_{rlx} := 1;
  if r₂ then [x]_{rlx} := 1
else [y]_{rlx} := 1
fi
r₀ = [z]_{rlx}

SE_prop  Possible outcomes:
Fully Supported: ✓ r₀ = 0
Requires: r₀ = 1
[x]_{rel} := 0; [y]_{rel} := 0; [z]_{rel} := 0;
[x]_{rlx} := 0; [y]_{rlx} := 0; [z]_{rlx} := 0;
r₁ = [x]_{rlx};
if r₁ then [z]_{rlx} := 1;
  if r₂ then [x]_{rlx} := 1
else [y]_{rlx} := 1
fi
r₀ = [z]_{rlx}

SE_nested  Possible outcomes:
Fully Supported: ✓ r₀ = 0
Requires: r₀ = 1
[x]_{rel} := 0; [y]_{rel} := 0; [z]_{rel} := 0; [f]_{rlx} := 0;
[x]_{rlx} := 0; [y]_{rlx} := 0; [z]_{rlx} := 0;
r₁ = [x]_{rlx};
if r₁ then r₂ = [f]_{rlx};
  if r₂ then [z]_{rlx} := 1;
    if r₃ then [x]_{rlx} := 1
    else [y]_{rlx} := 1
fi
else [y]_{rlx} := 1
fi
r₀ = [z]_{rlx}

A.10 Locks

Dekker's lock
stuck
Possible outcomes:
[x]_{rel} := 1;
[y]_{rel} := 1;
[r]_{acq} := 1; [y]_{acq} := 1;
[r]_{rlx} := 0 if r₁ = 0
[r]_{rlx} := 0 if r₂ = 0
then [d]_{na} := 5
else 0
fi
then [d]_{na} := 6
else 0
fi

2016/7/12
Cohen’s lock

Impossible outcomes (according to [45]):

stuck

Requires: RA + na

Fully Supported: ✓

\[ x_{rel} := 0 ; \ y_{rel} := 0 ; \ d_{na} := 0 ; \]
\[ x_{rel} := \text{choice} \ 1 \ 2 ; \]
\[ \text{repeat} \ y_{acq} \ \text{end} ; \]
\[ r = [x_{acq} ; \]
\[ r2 = [y_{acq} ; \]
\[ \text{if} \ r1 == r2 \]
\[ \text{then} \ d_{na} := 5 \]
\[ \text{else} \ 0 \]
\[ \text{fi} \]
\[ y_{rel} := \text{choice} \ 1 \ 2 ; \]
\[ \text{repeat} \ x_{acq} \ \text{end} ; \]
\[ r3 = [x_{acq} ; \]
\[ r4 = [y_{acq} ; \]
\[ \text{if} \ r3 != r4 \]
\[ \text{then} \ d_{na} := 6 \]
\[ \text{else} \ 0 \]
\[ \text{fi} \]

B. Additional Semantic Rules

\[
\begin{align*}
E & ::= [ ] | x = E ; s \\
    & | \text{par} \ E \ s \ | \text{par} \ s \ E \\
EU & ::= [ ] | (EU) | EU \ \text{op} \ e | e \ \text{op} \ EU \\
    & | (\mu, EU) | EU, \mu \\
    & | \text{fst} \ EU | \text{smd} \ EU \\
    & | \text{choice} \ EU \ e | \text{choice} \ e \ EU \\
    & | x = EU ; s \\
    & | \text{if} \ EU \ \text{then} \ s1 \ \text{else} \ s2 \ \text{fi} \\
    & | [r]_{\text{hom}} := EU \\
    & | \text{cas}_{SM,FM}(t, EU, \mu) | \text{cas}_{SM,FM}(t, \mu, EU)
\end{align*}
\]

Figure 23. Syntax of evaluation contexts.

\[
\begin{align*}
&\text{If-True} \quad \langle E[\text{if} \ n \ \text{then} \ s1 \ \text{else} \ s2 \ \text{fi}], \xi \rangle \Rightarrow \langle E[s1], \xi \rangle \\
&\text{If-False} \quad \langle E[\text{if} \ 0 \ \text{then} \ s1 \ \text{else} \ s2 \ \text{fi}], \xi \rangle \Rightarrow \langle E[s2], \xi \rangle \\
&\text{Repeat-Unroll} \quad \langle E[\text{repeat} \ s \ \text{end}], \xi \rangle \Rightarrow \langle E[s \ \text{if} \ x \ \text{then} \ x \ \text{repeat} \ s \ \text{end} \ \text{fi}], \xi \rangle \\
&\text{Spawn} \quad \langle E[\text{spw} \ s1 \ s2], \xi \rangle \Rightarrow \langle E[\text{par} \ s1 \ s2], \xi' \rangle \\
&\text{Join} \quad \langle E[\text{par} \ v1 \ v2], \xi \rangle \Rightarrow \langle E[(v1, v2)], \xi' \rangle \\
&\text{Choice-Fst} \quad \langle E[\text{EU}[\text{choice} \ e1 \ e2]], \xi \rangle \Rightarrow \langle E[\text{EU}[e1]], \xi \rangle \\
&\text{Choice-Snd} \quad \langle E[\text{EU}[\text{choice} \ e1 \ e2]], \xi \rangle \Rightarrow \langle E[\text{EU}[e2]], \xi \rangle
\end{align*}
\]

Figure 24. The core rules of the semantics.
\( \xi = (H, \psi^r, \ldots, \sigma^na) \ldots \)
\( \sigma_{rd}(\ell) \equiv \text{LastTS}(H, \ell) \quad \sigma = \sigma_{rd}(\ell \mapsto \tau) \)
\( \xi' = (H[(\ell, \tau) \mapsto (v, \ell)], \psi_{rd}[\pi \mapsto \sigma], \ldots, \sigma_{na}[\ell \mapsto \tau]) \)

\[ \langle E[l']na := v], \xi \rangle \Rightarrow \langle E[v], \xi' \rangle \quad \text{WRITE-N\_NA} \]
\[ \xi = (H, \psi^r, \ldots, \sigma^na) \ldots \]
\[ \tau = \text{LastTS}(H, \ell) \quad \tau \equiv \sigma_{rd}(\ell) \quad H(\ell, \tau) = (v, \sigma) \]
\[ \langle E[l']na].\ell \rangle \Rightarrow \langle E[v], \xi \rangle \quad \text{READ-N\_NA} \]
\[ \xi = (H, \psi^r, \ldots, \sigma^na) \ldots \]
\[ \sigma_{rd}(\ell) \neq \text{LastTS}(H, \ell) \]
\[ \langle E[l']na := v], \xi \rangle \Rightarrow \langle \text{stuck}, \xi \rangle \quad \text{WRITE-N\_STuck1} \]
\[ \xi = (H, \psi^r, \ldots, \sigma^na) \ldots \]
\[ \sigma_{rd}(\ell) \neq \text{LastTS}(H, \ell) \]
\[ \langle E[l']na].\ell \rangle \Rightarrow \langle \text{stuck}, \xi \rangle \quad \text{READ-N\_STuck1} \]
\[ \xi = (H, \psi^r, \ldots, \sigma^na) \ldots \]
\[ \sigma_{rd}(\ell) < \sigma_{na}(\ell) \]
\[ \langle E[l']na := v], \xi \rangle \Rightarrow \langle \text{stuck}, \xi \rangle \quad \text{WRITE-N\_STuck2} \]
\[ \xi = (H, \psi^r, \ldots, \sigma^na) \ldots \]
\[ \sigma_{rd}(\ell) < \sigma_{na}(\ell) \]
\[ \langle E[l']na].\ell \rangle \Rightarrow \langle \text{stuck}, \xi \rangle \quad \text{READ-N\_STuck2} \]

**Figure 25.** Reduction rules for non-atomics.

\[ \xi = (\ldots, \psi, \gamma) \ldots \]
\[ \times \equiv \text{fresh symbolic variable} \quad \alpha = \psi(\pi) \]
\[ \xi' = (\ldots, \psi[\pi \mapsto \text{append}(\alpha, E, \text{read}(x, \ell, \text{WM})), \gamma]) \quad \text{READ-POSTPONE} \]
\[ \langle E[E[x]l'm := e]], \xi \rangle \Rightarrow \langle E[\bar{E}[x]], \xi' \rangle \]
\[ \xi = (\ldots, \psi, \gamma) \ldots \]
\[ \times \equiv \text{fresh symbolic variable} \quad \alpha = \psi(\pi) \]
\[ \xi' = (\ldots, \psi[\pi \mapsto \text{append}(\alpha, E, \text{write}(x, \ell, \text{WM})), \gamma]) \quad \text{WRITE-POSTPONE} \]
\[ \langle E[E[x]l'm := e]], \xi \rangle \Rightarrow \langle E[\bar{E}[x]], \xi' \rangle \]
\[ \xi = (\ldots, \psi, \gamma) \ldots \]
\[ \times \equiv \text{fresh symbolic variable} \quad \alpha = \psi(\pi) \]
\[ \xi' = (\ldots, \psi[\pi \mapsto \text{append}(\alpha, E, \text{let}(x, \ell, \phi)), \gamma]) \quad \text{LET-POSTPONE} \]
\[ \langle E[E[x]l'm := e]], \xi \rangle \Rightarrow \langle E[\bar{E}[x]], \xi' \rangle \]
\[ \xi = (H, \psi^r, \ldots, \psi, \gamma) \ldots \]
\[ \text{read}(x, \ell, \text{RM}) \] is inside \( \psi(\pi) \)
\[ \text{and there is no conflicting operation before} \]
\[ \phi' = \text{remove}(\psi, \pi, \text{read}(x, \ell, \text{RM})) \]
\[ \gamma' = \gamma \setminus \{x\} \quad \xi' = (\ldots, \psi'[\psi/x], \gamma') \quad \text{READ-RESOLVE} \]
\[ \langle s, \xi \rangle \Rightarrow \langle s[v/x], \xi' \rangle \]

**Figure 26.** Rules for work with postponing of operations.

### C. RCU testing
Figure 27. Test results and runtimes for modified RCU.