Accelerating Framework of Transformer by Hardware Design and Model Compression Co-Optimization

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Abstract—State-of-the-art Transformer-based models, with gigantic parameters, are difficult to be accommodated on resource constrained embedded devices. Moreover, with the development of technology, more and more devices are available to run a Transformer model. For a Transformer model with different constraints (tight or loose), it can be deployed onto devices with different computing power. However, in previous work, designers did not choose the best device among multiple devices. Instead, they just used an existing device to deploy model, which was not necessarily the best fit and may lead to underutilization of resources. To address the deployment challenge of Transformer and the problem to select the best device, we propose an algorithm \(\Rightarrow\) hardware closed-loop acceleration framework. Given a dataset, a model, latency constraint \(LC\) and accuracy constraint \(AC\), our framework can provide a best device satisfying both constraints. In order to generate a compressed model with high sparsity ratio, we propose a novel pruning technique, hierarchical pruning (HP). We optimize the sparse matrix storage format for HP matrix to further reduce memory usage for FPGA implementation. We design a accelerator that takes advantage of HP to solve the problem of concurrent random access. Experiments on Transformer and TinyBert model show that our framework can find different devices for various \(LC\) and \(AC\), covering from low-end devices to high-end devices. Our HP can achieve higher sparsity ratio and is more flexible than other sparsity pattern. Our framework can achieve \(37\times, 1.9\times, 1.7\times\) speedup compared to CPU, GPU and FPGA, respectively.

Index Terms—component, formatting, style, styling, insert

I. INTRODUCTION

Recently, Transformer \cite{1} has gained popularity and achieved record-breaking results on major natural language processing (NLP) tasks, including question answering, sentiment analysis and language inference \cite{2, 3}. Although state-of-the-art Transformer models offer great prediction accuracy, they have a large number of parameters. For example, the BERT\_LARGE model has 340M parameters \cite{3} and the DistilBERT, a compact model, has 67M parameters \cite{4}. Moreover, with the ongoing democratization of machine learning \cite{7}, there are increasing needs to execute such giant models on embedded devices \cite{8, 9}, e.g., field-programmable gate array (FPGA) or application-specific integrated circuit (ASIC). Using these devices as an acceleration platform for Transformer is challenging as they offer a limited on-chip memory and often possess limited off-chip bandwidth, both of which are critical for high performance. This restriction is particularly limiting for FPGA due to its extremely small on-chip memory, approximately 5MB for low-end FPGA (e.g., ZCU104) and 35MB for high-end FPGA (e.g., Alveo U200). Therefore, when Transformer comes to embedded devices, the primary challenge is in accommodating giant models onto these devices, along with the requirement of low inference latency. Three research trends have attracted enormous interests to improve the performance of Transformer, as Table I shows. The first trend is hardware acceleration on ASIC, e.g., A\textsuperscript{3} \cite{13}, where researchers mainly focus on hardware acceleration. The second trend is algorithm optimization on CPU and GPU, such as neural architecture search (NAS) and model compression algorithms, e.g., block structured pruning \cite{14}, lottery ticket hypothesis \cite{12, 15, 16}. The third trend is the algorithm \(\Rightarrow\) hardware sequential design flow \cite{10, 11}, which compress the model first and then implement compressed model to a existing device. This sequential design flow has no hardware performance feedback to software optimization. In this paper, we propose an algorithm \(\Rightarrow\) hardware closed-loop framework, which can trade off between the sparsity ratio and hardware resources to achieve co-exploration of model compression and hardware acceleration. Our framework simultaneously considers hardware type, resource utilization, model compression, and \(LC\) and \(AC\).

Moreover, with the development of technology, more and more hardware devices are available to run a Transformer model, such as various types of mobile device (e.g., Apple Bionic, Qualcomm Snapdragon, HiSilicon Kirin, Samsung Exynos, ...), FPGAs (e.g., ZCU102, VC707, Alveo U200, Versal, ...), ASICs and son on. These devices have different

\begin{table}[h]
\centering
\begin{tabular}{|c|c|c|c|c|c|}
\hline
Methods & Algorithm & Hardware & NAS & Hardware & Ours \\
\hline
AC & & & & & \\
\hline
Hardware Type & & & & & \\
\hline
Resource Uti. & & & & & \\
\hline
Compression & & & & & \\
\hline
\end{tabular}
\caption{Comparisons of acceleration framework for Transformer models. Our framework distinguishes from other works by considering both AC and LC.}
\end{table}
computing power and storage capacities, which are critical to the performance of Transformer. Moreover, for a Transformer model with different constraint requirements (tight or loose), it can be deployed onto devices with different computing power. However, in previous work, designers did not choose the best one among multiple devices. Instead, they just used an existing device to deploy the model, which was not necessarily the best fit and may lead to underutilization of resources. Therefore, with the surging of various types of devices and constraint requirements for models, it is becoming increasingly difficult for designers to select the best device for their application.

To address the deployment challenge of Transformer and the problem to select the best device, as the first attempt, we propose an algorithm toward hardware closed-loop framework, which can provide a best device under different constraints. Our framework makes a tradeoff between the sparsity ratio of model and hardware resources to achieve co-exploration to accelerate Transformer inference. We use FPGA to illustrate our design, and it can also be applied to other hardware devices, such as mobile devices, ASICs.

The main contributions of this paper are: (1) An Algorithm=⇒ hardware closed-loop framework. We provide a co-exploration framework from constraints \((LC, AC)\) to device. User can input some constraints, \(LC, AC\), backbone model and dataset, our framework can output the best device to deploy this model meanwhile satisfying both constraints. (2) A Hardware-friendly Hierarchical Pruning (HP) Technique. We propose HP, a novel sparsity pattern, which is a two-level pruning technique and takes advantage of two existing pruning techniques, block structured pruning (BP) and vector-wise pruning (VW). HP is hardware-friendly and can achieve high sparsity ratio. (3) A Sparse Matrix Storage Format Optimization. We optimize a sparse weight format for our HP matrix on FPGA implementation. Our format can significantly reduce memory usage and perform better than commonly used formats. (4) Sparsity-aware Accelerator. We design a FPGA-based accelerator for HP and abstract a performance predictor to build a bridge between the software and hardware for efficient clock cycles and resource usage estimation.

II. RELATED WORK

Transformer. Transformer has been highly optimized at the software level for CPU and GPU. A research trend is to modify the architecture of Transformer to improve the performance on CPU and GPU [12], [17]. These work exploit Neural Architecture Search (NAS) to search a best model architecture. However, the cost is usually high in the search process, since massive computations and neural network samples are required for an optimized network architecture. However, little work has been published related to custom hardware acceleration for transformer-based model, particularly on FPGAs. [15] has been proposed to accelerate different parts of transformer model, attention and fully-connected layers, to achieve efficient processing on ASIC. [10] is the only currently published FPGA accelerator, which proposes a acceleration framework to enable compression on FPGA. This work sequentially first compress model and then deploy the compressed model on FPGA. This sequential design flow has no hardware performance feedback to software optimization and is not the optimal. In this paper, we trade off between the sparsity ratio and hardware resources to achieve co-exploration of model compression and hardware acceleration.

Model Compression. [15], [16] applied Lottery ticket hypothesis on model compression on BERT, based on an observation that a subnetwork of randomly-initialized network can replace the original network with the same performance. However, the non-structure pruning is not hardware-friendly. For hardware-friendly weight pruning, [18] proposes a hardware-friendly block structured pruning technique for transformer. However this technique will result in a significant accuracy loss when pruning ratio increases or block size is larger. [19] proposes pattern pruning to make a better balance between accuracy and pruning ratio. But this pruning technique cannot directly apply to hardware due to parallelism limit.

Sparse Matrix Compression Formats. A variety of sparse matrix representation formats have been proposed to compress the sparse matrix. Prior works take two major approaches to design such compression scheme. The first approach is to devise general compression formats, such as Compressed Sparse Row (CSR) [20], Coordinate (COO) [21]. They both record the row/column indices of each non-zero elements, which cause excessive memory usage. The second approach is to leverage a certain known structure in a given type of sparse matrix. For example, the DIA format [22] is highly efficient in matrices where the non-zero elements are centered along the diagonals of the matrix. The CSB format [23] is devised for the proposed CSB sparsity pattern. Though these compression schemes are specific to certain types of matrices, they are the most efficient in both computation and storage. In our work, in order to be the most efficient in storage, we optimize a sparse matrix compression scheme for our sparsity pattern HP.

III. THE ALGORITHM=⇒ HARDWARE CLOSED-LOOP ACCELERATION FRAMEWORK

To address the deployment challenge of Transformer and the problem to select the best device, as the first attempt, we propose an algorithm=⇒ hardware closed-loop framework, which can provide a best device under different constraints. Our framework makes a tradeoff between the sparsity ratio and hardware resources to achieve co-exploration of model compression and hardware acceleration. Next, we use FPGA to illustrate our design, and it can also be applied to other devices, such as mobile devices, ASICs.

A. Problem Definition and Overview

In this paper, we aim to develop an algorithm=⇒ hardware closed-loop acceleration framework to select the best device under different \(AC\) and \(LC\) for Transformer. We define the problem as follows: Given a specific data set \(D\), a backbone model \(bM\), a hardware pool \(H\), latency constraint \(LC\), accuracy constraint \(AC\), the objective is to determine: (i) \(cM\) : a compressed model including sparsity of each layer; (ii) \(tH\) :
the target hardware device; such that the compressed model \( cM \) can be deployed onto the target device \( tH \) meanwhile satisfying both constraints \( LC \) and \( AC \).

Figure 1 shows the overview of our framework and Algorithm 1 illustrates the whole process. Firstly, we design a pruning technique and conduct sparsity-aware accelerator design (components 1, 2) and abstract a performance predictor to estimate hardware resource requirements (components 3). Then we use the RNN-based RL controller to guide the search process: (i) the controller predicts a sample; (ii) the performance predictor roughly estimates resource requirements of the sample (components 3); (iii) select the target device from hardware pool to meet resource requirements (components 4); (iii) fine tune the resource allocation exactly and optimize the latency under the target device constraint (components 5); (iv) fine tune the model and get accuracy (components 6). At last, the controller is updated based the feedback (reward) from 4 5 6 and then predicts better samples. In the following text, we will introduce these components one-by-one.

**Algorithm 1** Acceleration Framework.

**Input:** \( bM \): backbone model; \( D \): a specific data set

**Output:** \( cM \): a compressed model

1. for each \( i \) in range(1, \text{iterMax}) do
2. RL controller predicts a sample (\( sw, hw \))
3. Performance predictor to roughly predict clock cycles \( E_{cycle}, \) the number of block RAMs (BRAMs) \( E_{bram} \) and DSPs \( E_{dsp} \) based on the sample.
4. Choose device from \( H \) based on \( E_{cycle}, E_{bram}, E_{dsp} \).
5. Estimate the maximum latency \( ML \)
6. if find proper device and \( ML < LC \) then
7. calculate the \( RU \) and choose the best \( tH \).
8. fine tune resource allocation to get mini latency \( L \)
9. \( A, cM = \text{Prune}_\text{Train}(bM,D) \)
10. else
11. assign negative values to \( A, L, RU \)
12. Reward = \( A + \text{norm}(L_f) + RU \)
13. Monte Carlo algorithm to update controller
14. end if

**B. Network Compression**

In order to accommodate Transformer models with enormous parameters onto the on-chip memory of FPGA, a pruning technique that can achieve a high sparsity ratio with a small accuracy loss and hardware-friendly is necessary. In this paper, we propose HP, which is a two-level pruning technique. It combines the advantages of existing two pruning techniques, BP [14] and VW [24]. Firstly, to keep hardware-friendly, we adopt BP to prune model. However, it is coarse-grained and can’t achieve high sparsity ratio with a small accuracy loss. But how to achieve higher sparsity ratio? Next, based on BP, we adopt VW, a fine-grained pruning, to prune further. In this way, we can maintain hardware-friendly and achieve high sparsity.

As Figure 2 shows, our HP is a combination of BP and VW. First, we adopt BP as the first level pruning and we divide the weight matrix into blocks and prune some unimportant columns in each block. We regard this BP model as the backbone model BP, and denote its sparsity ratio by \( S_{bm} \). The value of \( S_{bm} \) determines the starting sparsity rate of HP weight, which can be adjusted flexibly. Then, based on the backbone model BP, we adopt VW as the second level to remove unimportant elements in each unpruned column of blocks. To keep balanced, we remove the same number of elements in each column of blocks. Our HP combines coarse-grained (BP) and fine-grained pruning (VW) to achieve a higher sparsity ratio and ensure a small accuracy loss. We make a comparison among BP, VW and HP. As Table II shows, our HP combines the best of both BP and VW and is

| Pruning Techniques Comparison among BP, VW and Our HP. Our HP Combines Coarse-grained and Fine-grained Pruning and Can Achieve Higher Sparsity Ratio Than BP and VW. |
|-----------------|-----|-----|-----|
| Fine-grained    | BP  | VW  | HP(ours) |
| Coarse-grained  | ✓   | ✓   | ✓   |
| Flexibility     | ✓   | ✓   | ✓   |
| Hardware-friendly | ✓   | ✓   | ✓   |
| High spar.& acc. | ✓   | ✓   | ✓   |

![Fig. 2. The Proposed Pruning Technique, Hierarchical Pruning (HP).](image-url)
more flexible and effective than them. As for VW, it keeps all vectors (columns), which is unnecessary because some vectors are important and some are not. As for HP, we can first prune some unimportant columns, which can increase the sparsity ratio than VW to some extent. Moreover, we can also flexibly adjust the value of $S_{bm}$ to achieve different sparsity ranges and accuracy.

C. Sparsity-aware Accelerator Design

In this section, first, we introduce the optimized sparse weight matrix storage format when implementing on FPGA. Then we introduce the accelerator design.

The Storage Format Optimization. In sparse matrices, the number of non-zero elements (NZ) is much smaller than the number of zero elements. In order to avoid unnecessarily 1) storing zero elements and 2) performing computations on them, we need an efficient scheme to compress the sparse matrix. Various sparse matrix storage formats have been proposed, e.g., COO [21], CSR [20], BCSR [25], Tile-Bitmap [26], MBR [27]. In our work, we use a bitmap format similar to MBR and optimize this format based on our sparsity pattern HP to reduce memory usage further.

Figure 3 shows our format, WMark. We design two formats according to the sparsity ratio of backbone model $S_{bm}$. When $S_{bm}$ is not equal to 0%, the weight is pruned by BP and VW and we use SF1. When $S_{bm}$ is equal to 0%, the weight is only pruned by VW and we use SF2. There are three arrays in SF1: (i) the three-dimensional array $w$ records all non-zero elements (NZ). The first dimension record the number of blocks and the NZ in successive blocks are concatenated (column-major order) and stored continuously in the last two dimension; (ii) array $\text{colIdx}$ stores the indices of unpruned columns in each block; (iii) In order to track which elements are NZ in each unpruned column, we use a bitmap array $\text{WBit}$. If the a slot contains a NZ we set the it to "1", otherwise to "0". As for SF2, the $\text{colIdx}$ array is not needed and there are only two array. There are four arrays in MBR [27]: value, row_idx, col_idx, Bitmap. The difference between our WMark and MBR [27] format is that: 1) row_idx array is not needed. Because it is easy to calculate the row indices due to the balanced property of HP sparsity pattern. 2) The Bitmap array WBit in our WMark only records the unpruned column not all columns, which can save memory storage. We set a $800 \times 800$ weight matrix with 50% sparsity ratio and compare the memory usage of the five formats with ours. As Table III shows, our format performs better than all.

Accelerator Design. Different from other FPGA accelerator design [24], [28]–[30], we fit all weights on on-chip memory of FPGA and don’t move data between on-chip and off-chip memory by weight pruning and quantization. And to realize a low inference latency with parallel FPGA, there are multiple challenges to design an architecture that can exploit the benefits of HP. In previous work, [24] and [23] implement accelerators with sparsity but they are designed for RNN model (matrix-vector multiplication, MV) and can’t be applied to Transformer (matrix/vector-matrix multiplication, MM / VM). As Figure 4 show, with generalized VM as in [31], there are two concurrent irregular memory accesses challenges, one for random read to input vector and the other for random write to result matrix, which can install the parallel execution. To solve these challenges, we change the memory access pattern. To avoid the random write to result matrix, we multiply multiple rows of the input matrix by one column of the weight matrix, which can achieve sequential writing. To solve the challenge of random read to input, we assign a input matrix row buffer IRB and use register to implement it which can be randomly accessed.

Figure 5 shows our computation engine. It consists of $T$ parallel processing elements (PEs) that compute dot products of distinct input matrix rows and one column of the weight matrix (one block) concurrently to exploit inter-row parallelism, while each PE is designed to exploit intra-row parallelism in a single dot product operation. Each PE contains a input matrix row buffer IRB to buffer each row of the being multiplied input matrix and this buffer is implemented by register which can be randomly accessed. This computation includes 5 steps: (1) The PE reads $C$ elements from the weight matrix memory and $C$ elements based on the WBit array from the input row buffer IRB. (2) C multipliers operate simultaneously to obtain $C$ scalar products. (3) an adder tree sums $C$ scalar products to calculate the dot product. (4) PE reads col_idx from the weight matrix. (5) The dot product result is written back to the result memory based on the col_idx. PEs are fully pipelined so that one operation can be processed per clock cycle.

D. Performance Predictor

We develop a FPGA performance predictor to roughly analyze resource requirements $E_{cycles}$, $E_{bram}$, $E_{dsp}$ based on software and hardware parameters predicted by RL controller.

1. We model the Block RAMs (on-chip SRAM units, called BRAMs) usage $E_{bram}$ using the formula in [32]. According to on-chip buffer allocation, we can calculate the BRAMs for
the denseresult matrix memory
input row buffer
××++××+valueWBit(registers)
PE-T
thesparse weight memory …input row buffer
××++××+valueWBit(registers)
PE-1
C
col_Idx
Computation Engine the dense multiplied matrix memory (input)
random writeto result only write a column
input weight result
input resultT C (a)
(b) input row buffer (register)
1 2 5 3
1 2 5
1 2 5
1 2 5
1 2 5
1 2 5
1 2 5
1 2 5
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1 2 5
(a) generalized VM and parallelism. (b) our MM design with HP. We exploit the multi-row of input matrix to avoid random write to result matrix.

Fig. 4. The sparse MM parallelism scheme. (a) generalized VM and parallelism. (b) our MM design with HP. We exploit the multi-row of input matrix to avoid random write to result matrix.

Fig. 5. Computation Engine.

i-th buffer \( B_i = \left\lceil \frac{\text{bits}}{\text{width}} \right\rceil \times \left\lceil \frac{\text{elements}}{\text{depth}} \right\rceil \times \text{factor} \). Among them, \( \text{bits} \) represents the quantization bits of weight and \( \text{elements} \) represents the number of NZ of weight. The \( \text{width} \) and \( \text{depth} \) represent the configuration of BRAM. Then we can get the total BRAMs by adding up all buffers \( E_{\text{bram}} = \sum B_i \).

The DSP usage \( E_{\text{dsp}} \) is related to multiply-accumulate and data type. According to the computation engine in Figure 5, it can execute \( C \times T \) MAC operations in parallel. For the 16-bit fixed point, it requires \( 2 \times C \times T \) DSPs, where each multiplication and add operation requires 1 DSP. For 32-bit floating point, it requires \( 5 \times C \times T \) DSPs, where 5 is the sum of 3 DSPs for one multiplication and 2 DSPs for one add operation. Suppose that the total number of layers are \( n \) and the PEs size of i-th layer is \( C_i \times T_i \), then the total DSP is :  \( E_{\text{dsp}} = \sum_{i=1}^{n} 5 \times C_i \times T_i \).

The clock cycles \( E_{\text{cycles}} \) are related to the size of PEs. After implementing PEs in Vivado HLS, we try to make the pipeline interval become 1, indicating that PEs can output one result in 1 clock cycles. Therefore, clock cycles of one layer equal the number of times that PEs is invoked. The sparse matrix multiplication of \( K \times M \) and \( M \times N \) with sparsity ration \( s \) can support \( K \times M \times N \times (1-s) \) MAC. With the PEs size \( C \times T \), we can calculate the clock cycles: \( l = \frac{K \times M \times N(1-s)}{T \times C} \). Therefore, for \( n \) layers in total, the total clock cycles is: \( E_{\text{clock}} = \sum_{i=1}^{n} l_i \).

E. Choose Device

Next, we introduce how to choose the best device from hardware pool based on \( E_{\text{cycles}}, E_{\text{bram}}, E_{\text{dsp}} \). Figure 6 show the process of selecting a best device. Table IV show our hardware pool. The process is as follows: (1) First, we sort devices in hardware pool according to the number of BRAMs provided by each device. (2) we perform binary search to find the device whose BRAMs are larger than \( E_{\text{bram}} \). That might be more than one device thus we use a set \( F \) to denote the alternative devices. (3) we calculate the latency \( L_i \) for device \( i \) in set \( F \) based on the formula \( L_i = E_{\text{cycles}}/\text{freq} \), where \( \text{freq} \) is the running frequency of device \( i \) and meanwhile we also compute the resource utilization \( R_i \) for each device. (4) we choose the device whose \( L_i \) is small than \( LC \). Specifically, When there are more than two device to choose from, we choose the device with largest \( R_i \), meaning that we can select the device with lower price and higher resource utilization.

F. Optimization

The optimization step is to exactly fine tune the resource allocation sheme under the resource constraint of the target device to achieve the least clock cycles and fill up the gap between the actual and estimated value. In this step, we specifically consider the parallelism of the Dot-Attention layer, which defaults to 1 in the performance predictor step. The target FPGA offers a certain number of resource including DSP slices (ALUs) and BRAMs. And our goal is to leverage these resources to exploiting the compute capabilities of the FPGA and achieving reasonably high performance. This problem can be expressed as the following optimization objective:

\[
\min \quad \text{exeCyc} = g(T, C, h) = \sum_{i=0}^{n} f(T_i, C_i) + \frac{n\text{Head}}{h} \times C\text{yc}_h
\]

s.t. \( 0 \leq \sum_{i=0}^{n} C_i \times T_i + h \times R_h \leq R_{total} \)

Here, the parameters \( T_i, C_i \) are the PE size of i-th layer and \( h \) is the parallelism of Dot-Attention layers. The \( C\text{yc}_h \) and \( R_h \) are the clock cycles and computation resource needed by one Dot-Attention layer. \( R_{total} \) is the available computation resource of the target device. \( n\text{Head} \) is the number of heads of Transformer-based models. Algorithm 2 illustrates our fine-tuned resource allocation scheme and solves the optimization objective. The algorithm takes in as input the Transformer model architecture \( A \) and the target device constraints \( F \). And
it finally outputs the parallelism factor $C, T, h$ and the least latency $execCycle$.

**Algorithm 2 Fine-tuned Resource Allocation Scheme**

**Input:** $F$: the target device constraints  
$A$: the Transformer model architecture  
s: the sparsity ratio for all layers  

**Output:** $execCyc$, the optimized cycles $C, T, h$: parallelism factor

1. Initialize the $exec$ // execution cycles
2. Set available computation resource: $R_{total}$ //total DSPs
3. Compute the computation complexity of $i$-th layer: $Com_i = MAC_{of}Layer_i \times s_i$ and the total computation complexity of all layers: $Com_{total} = \sum_{i=0}^{n} Com_i$
4. for each $i$ in range(0, A.numHead) do
5. $tempR = R_{total} - i \times R_b$
6. for each $j$ in range(0, $n$) do
7. $R_j = \frac{Com_{total}}{Com_{total} - R_{total}} \times tempR$
8. adjust the parallelism factor ($C_j \times T_j$) based on $R_j$
9. end for
10. calculate cycles = $g(C, T, h)$
11. if cycles < $exec$ then
12. $execcycles$
13. record $C, T, i$
14. end if
15. end for

**G. Reinforcement Learning (RL)**

In our design, the search space is very big, therefore we exploit the RL to carry out guided search. The RL controller is implemented based on an RNN [34]. In each episode, the controller first predicts a sample, and gets its $Reward$ based on the evaluation results from the environment (components 3 4 5 6 in Figure 1). Then, we employ the Monte Carlo policy gradient algorithm [35], [36] to update the controller:

$$\nabla J(\theta_c) = \frac{1}{m} \sum_{k=1}^{m} \sum_{t=1}^{T} \gamma^{T-t} \nabla_{\theta_c} \log(a_t|a_{t-1}; \theta_c) (R_b - b)$$

where $m$ is the batch size and $T$ is the number of steps in each episode. The exponential factor $\gamma$ are used to adjust the reward at every step and the baseline $b$ is the average exponential moving of rewards.

Our framework specifically takes hardware performance ($L, RU$) into consideration rather than just model accuracy $A$. As Figure 7 shows, we integrate the software parameters (# sparsity ratio) and accelerator design parameters (# parallelism factors) into the action space to realize a co-exploration of sparsity ratio and hardware resource. Therefore, we employ a reward function to calculate $Reward$, which takes the accuracy $A$, latency $L$, the resource utilization $RU$ and latency constraint $LC$ to calculate reward. The function is defined as follows:

$$Reward = \begin{cases} 
A + \frac{LC - L}{LC} + RU & L < LC, A > AC \\
-\frac{pen_A}{pen_L} & L > LC, A < AC \\
\end{cases}$$

In the above function, there are two cases. First, if $L < LC$ and $A > AC$, it indicates that the performance of the sample can satisfy the constraints, we sum up the reward of hardware performance and accuracy. Otherwise, in any other case, it indicates that the sample can’t satisfy constraints and we directly return negative values to the controller, which can save the search time. Note that we return different negative reward to guide the search. We return $\text{pen}_A$ for $L < LC&A < AC$ and return $\text{pen}_L$ for $L > LC&A > AC$.

**IV. EXPERIMENTS**

**A. Experimental Settings**

**Baseline Models and Datasets.** We test our method on Transformer model using WikiText-2 dataset [37] and on TinyBERT model using GLUE benchmark [38]. For Transformer model, there are 2 encoder and 1 decoder layers (the hidden size is 800, the feed-forward size is 200 and the head number is 4). And we use the accuracy of word prediction as our evaluation metrics. For TinyBERT, there are 4 encoder layers and 1 pooler layer and 1 classifier layer.

**Evaluation Platforms.** We conduct the reinforcement learning framework with the training of Transformer model on an 8× NVIDIA Quadro RTX 6000 GPU server (24 GB GPU memory). Experiments environment are performed on Python 3.6.10, GCC 7.3.0, PyTorch 1.4.0, and CUDA 10.1. The hardware accelerator design is implemented with Vivado HLS, which is the commonly used high level synthesis tool. This tool enables implementing the accelerator with C languages and exports the RTL as a Vivado’s IP core. The C code of our accelerator is parallelized by adding HLS-defined pragma. Pre-synthesis resource report are used for performance estimation.

**B. Experimental Results**

1) Pruning Strategy: We set the sparsity ratio of backbone model $S_{bm}$ to different values for different models. For TinyBert model, its model size is relatively small and is sensitive to pruning. Therefore in order to maintain high accuracy, we set $S_{bm}$ to 0%. For Transformer model, through experiments we set $S_{bm}$ to 50%, which can ensure high sparsity ratio and maintain acceptable accuracy loss. As Table IV shows, Transformer model pruned by HP can reduce model size by 90% with 2.37% accuracy loss. And the TinyBert model can achieve 0.7% and 2.23% accuracy loss for MRPC task and SST-2 task.

**Accuracy.** To evaluate benefit of our HP, we compare it with BP [14], VW [24], block-wise pruning (BW) [39], and irregular pruning on Transformer model. The block size of BW and BP is $12 \times 12, 10 \times 800$, respectively. And the
vector size for VW is $10 \times 1$. As Figure 9 shows, the HP, VW and the irregular pruning can achieve the same model accuracy when the sparsity is smaller than 70%. The HP can achieve better accuracy than irregular pruning at around 82% sparsity. When the sparsity is larger than 92% (the intersection of HP and irregular), HP performs worse than irregular due to large sparsity of the backbone model. VW can only achieve the limited 90% sparsity when the vector size is $10 \times 1$ and our HP can achieve 99% sparsity. These experimental results demonstrate that HP has almost the same effectiveness as irregular sparsity and outperforms BW, BP and VW sparsity in terms of achievable accuracy or sparsity during pruning.

**Visualization.** We visualize the weight matrices after HP, VW and irregular pruning on Transformer model. Figure 8 visualizes the three sparse weight matrices of a $20 \times 20$ sub-matrix which is randomly selected from the whole $200 \times 800$ weight matrix. Pink grids indicate non-zero parameters and the pink level indicates the magnitude of the absolute value. Figure 8(a) shows the two steps of HP. In our HP matrices, there are two blocks (the top and bottom of the dashed line) and each vector (column) of $10 \times 1$ in blocks has 7 NZ. We can see that the heat map of HP weight can prune some unimportant columns and maintain most important weights as irregular pruning. Although irregular sparsity retains some weights in a column while our HP removes the whole column, these weights are relatively small (this can be seen from the pink level in Figure 8) and the removal has no significant impact on accuracy. Instead, most of the important weights can be retained by our HP to ensure accuracy.

2) **Overhead Comparison of Sparse Weight Format:** We compare overhead among CSR [20], Tile-Bitmap [26], MBR [27] and our WMark format. We use the memory usage as the metric. Figure 10 shows the results, it is clear that our optimized format WMark needs the least memory than all of them. And the WMark can achieve 1.5 $\times$ $2.5 \times$ reduction in memory usage than MBR [27]. The reason is that our WMark has the balanced property and we don’t need the row_start array to calculate the start index of each row. Besides, our WBit array only mask the non-zero columns not all columns. Therefore, our WMark can use less memory than MBR [27].

3) **Validation On FPGA:** We use FPGA devices to validate our approach. Table VI show our results. Our approach can find different devices under different sets of LC and AC. For Transformer, we set two sets of constraints to choose device: (40ms,92%) for loose constraints and (20ms,96%) for tight constraints. For (40ms,92%), its latency and accuracy restrictions are loose, so it is possible to achieve a higher sparsity ratio and deploy to a mid-end FPGA VC709. For (20ms,96%), its latency and accuracy restrictions are relatively tight, therefore the sparsity ratio is relatively small to ensure accuracy and it will be deployed to a device with strong computing power, Alveo U200, to achieve very low latency.

For MRPC task of TinyBERT model, first we set up three sets of constraints which have the same AC but different LC. The experimental results show that constraints with smaller LC can be deployed on FPGAs with greater computing power, such as (180ms, 85%) to ZCU102, (45ms, 85%) to VC709. Then we set constraint with lower AC (50ms, 80%), the searched result of sparsity ratio is 25% and the target device is ZCU102. This constraint can also be mapped to low-end FPGA (ZCU102), the same device as (180ms, 85%), due to compression and can achieve 3.7 $\times$ latency reduction. Therefore, the same device can satisfy different sets of constraints.
TABLE VI
VALIDATION ON FPGA

| Models | (LC, AC) | sparsity | accuracy | est. latency | BRMA / Util | DSP / Util | LUT / Util | FF / Util | Target device |
|--------|----------|----------|----------|--------------|-------------|------------|------------|------------|---------------|
| Transformer | (40ms, 92%) | 92.00% | 94.45% | 35.70ms | 2492 / 85% | 1644 / 46% | 303579 / 77% | 268065 / 30% | VC709 |
| TinyBERT (MRPC) | (180ms, 85%) | 0% | 86.45% | 17.5ms | 1602 / 87% | 1027 / 40% | 262248 / 95% | 131542 / 23% | ZCU102 |
| TinyBERT (SST-2) | (45ms, 90%) | 25.00% | 90.83% | 40ms | 1674 / 91% | 1056 / 42% | 264443 / 96% | 189035 / 34% | ZCU102 |
| TinyBERT (SST-2) | (50ms, 90%) | 25.00% | 90.37% | 25.1ms | 2504 / 85% | 2028 / 56% | 316028 / 73% | 235177 / 27% | VC709 |

TABLE VII
COMPARISON AMONG CPU, GPU AND FPGA

| Operations(G) | Latency(s) | FLOPS(G) | Impro. |
|---------------|------------|----------|--------|
| CPU | 1.5 | 2.9 | 1.1 |
| GPU | 1.1 | 0.284 | 0.09 | 2 |
| FPGA | 0.64 | 0.38 | 0.52 | 0.0146 | 0.00645 | 0.0158 |

by compression and can be applied to different application scenarios. For SST-2 task of TinyBERT model, it shows similar experimental results as Transformer and MRPC task.

4) Cross-platform Comparison: The research on Transformer models mainly focus on at the software level for CPU and GPU, such as Trans [1], Evolved Transformer [40], and HAT [12], but little work has been published related to custom hardware acceleration on FPGAs, in addition to FTRANS [10]. We compare the efficiency of ours with these work. Since these work exploit different models and data set, in order to provide a fair comparison, we use the floating-point operations per second (FLOPS) as the metric. As Table VII shows, our FPGA implementation can achieve $31 \times 37 \times 21$ speedup compared to Trans [1], Evolved Transformer [40] and HAT [12] on CPU respectively. And it can achieve $1.9 \times 1.7$ speedup compared to HAT [12] on GPU and FTRANS [10] on FPGA.

5) Search Space Exploration: We collect the explored results from RL to form the search space exploration results of Transformer in Figure [11]. In this figure, the x-axis and y-axis stand for the latency and accuracy. We show the search result of constraint (26ms, 96%). We can see that these points are mainly concentrated in the vicinity of (26ms, 96%). This is due to the guided search of RL, which makes the search samples closer to the solution. There are two points A and B satisfying the constraints in Figure [11]. It may represent there are two devices to choose from. In this case, we use the third metric, resource utilization, to select the best solution. The device with the largest resource utilization is the one that is more suitable, and at the same time it will be the cheaper one. Therefore, with our approach we can choose the best device.

6) Ablation Study: In this section, we investigate the influence of the sparsity of backbone model $S_{bm}$ in our HP. We set the row of block size as 10 in our experiment. The first feature of HP is that it can achieve different sparsity range when combined with different backbone models. For example, when $S_{bm}$ is equal to 40%, it can achieve sparsity range from 46% to 94%. When $S_{bm}$ is equal to 80%, the sparsity range is from 82% to 98%. VW has the limited sparsity of 90% and it can’t achieve sparsity larger than 90%. For accuracy, as Figure 11. The RL Search Results for Transformer under constraint (26ms, 96%). We select the device with the largest RU from A and B.

Fig. 11. The RL Search Results for Transformer under constraint (26ms, 96%). We select the device with the largest RU from A and B.

Fig. 12. The accuracy comparison of HP with different backbone models.

V. CONCLUSION

In this paper, we propose an algorithm=hardware closed-loop acceleration framework to solve the challenge of efficient deployments and device selection problem. Our framework can achieve from constraints (LC, AC) to device. To achieve high sparsity ratio, we propose HP to reduce model size. To further reduce memory usage, we optimized the sparse matrix storage format based HP sparsity pattern. Experiments show that our framework can find different devices for various LC and AC, covering from low-end devices to high-end devices.

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