Design and Implementation of a Single-Stage PFC Active-Clamp Flyback Converter with Dual Transformers

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Abstract: This paper proposes an AC/DC single-stage structure by integrating a boost topology and an active clamp flyback (ACF) circuit with power-factor-correction (PFC) function. The PFC function can be achieved by controlling a boost PFC topology operated in the discontinuous conduction mode. With the coordination of active clamping components, a resonant technique is obtained and zero-voltage-switching (ZVS) can be achieved. The proposed converter is combined with the advantages of: (1) compared with two-stage circuit, a single stage circuit decreases the component of the main circuit and reduces the complexity of the control circuit; (2) a boost topology with PFC function operated in discontinuous conduction mode can be accomplished without adding any current detecting technique or detecting input signal; (3) by using the inductor from the PFC stage, ZVS function can be achieved without any additional inductor; (4) the increment of switching frequency facilitates the optimization of power density; (5) the conducting loss at the secondary side can be reduced by adding the synchronous rectification; (6) in this proposed scheme, the dual transformers with series-parallel connection are utilized, the current at the secondary side can be shared for lowering the conduction loss of the synchronous transistors. Finally, a prototype converter with AC 110 V input and DC 19 V/6.32 A (120 W) output under 300 kHz switching frequency is implemented. The efficiency of the proposed converter reaches 88.20% and 0.984 power factor in full load condition.

Keywords: active clamp flyback; power-factor-correction; soft-switching

1. Introduction

The development of civilization and the rapid advancement of science and technology have led to a shortage of our energy. The optimization of efficiency has become one of the main goals in power electronic industries; thus, many countries have begun to establish different kinds of standards for energies gradually. In addition to that, the dimension, the efficiency, and the power density of power supplies are much more a matter of concern today. Therefore, various topologies and control methods are proposed to improve the aforementioned issues widely.

Flyback converters [1–3] are the most commonly used in low power electronics applications and consumer products, such as smart phone chargers, adaptors for laptops, and electric scooter battery chargers. The active-clamp techniques [4–7] have improved several drawbacks of the conventional flyback converter topology. The additional clamping capacitor can absorb the energy which is stored in the leakage inductor [8]. This helps to reduce voltage spikes during switching conditions [9,10]. By designing the parameters of the leakage inductor and the clamping capacitor to resonate appropriately, ZVS can be achieved easily [11]. This technique not only releases the energy of leakage inductance efficiently, but also makes good use of it by achieving soft switching to reduce switching loss. To pursue higher power density, increasing switching frequency can reduce the size of the transformer and magnetic component. Thus, the soft switching technique is one of
the common ways to increase the switching frequency and the efficiency to a higher level. The synchronous rectification (SR) technique is also a trend to improve the efficiency of converters currently. The SR switch can be controlled by detecting the voltage across the SR switch at the secondary side. The switching period can be controlled appropriately. However, if the SR technique works perfectly and precisely, proper layout of the schematic and the good driving signal are necessary.

In addition to the better performance of converters’ efficiency, the power factor (PF) is also a key index to describe the ratio of real power and apparent power. Different output load characteristics will cause the phase shift and deformation of the input current waveform. The increment of the reactive power from the AC main will increase the losses of power line during the energy delivering process. Thus, the PFC technique [12,13] is widely used to maintain the level of power factor and to fulfill the electrical specifications of power supplies. It can be classified into passive and active [14–16] methods. The passive method is mainly realized by passive components which has a low cost but large size. The effect of power factor correction is also limited; active methods use the additional switch and circuit to make the input current and voltage waveform in phase to improve power factor. By using this technique, PF can approach 1 with low harmonic. The effect of the active method is much better than that of the passive one, but this method requires one independent circuit with control stage to achieve. That requires more components and the cost will also increase.

In general, the structure of AC-DC converter with PFC function is a two-stage topology. It can be divided by two independent circuits [17,18]. Both of the independent circuits need to be operated by their own control systems. Hence, the number of components will definitely be increased. In order to simplify the structure of the two-stage circuit [19,20], the single-stage architecture was proposed.

In reference [21], a boost converter and a flyback converter with valley switching were combined. With the valley switching technique, switching loss is reduced by detecting auxiliary winding. The secondary side synchronous rectification is achieved through the self-made detection mechanism for increasing overall efficiency. However, it is difficult for the power factor to exceed 0.9, and the voltage spike problem of \( V_{DS} \) is the obstacle for developing toward a higher frequency level. Reference [22] combined a boost converter with a low-side ACF converter. Soft switching can be used to increase the switching frequency and efficiency. P-channel MOSFET can be utilized to solve the isolation issue for high-side switch in ACF topology. However, it is not common for P-channel MOSFET to have a high withstand voltage in practical. An external inductor is also needed to achieve ZVS which increases the elements of the circuit. In reference [23], an interleaved PFC boost converter is proposed and the efficiency goes to 95% under 110 V AC input. Reference [24] proposed an ACF converter with 93% of efficiency under 120 W output condition. The overall efficiency reached about 88.35% if the ACF and PFC stages were connected. Reference [25] proposed integrating a bridgeless boost and a LLC converter. ZVS and ZCS are achieved under different conditions, but several diodes are required to prevent the wrong current direction. Thus, an external inductor is also needed in the LLC resonant tank of the circuit. It also increases the total component of the circuit. In [26], a novel high-gain DC-DC boost converter with lower component count was implemented. This novel boost converter has higher power density characteristics which is suitable for the smaller size of electronic product with PFC function to boost the voltage for 400 Vdc applications. Lower component counts also bring lower cost and loss.

To compare with previous studies, several papers have proposed a single-stage PFC converter with soft-switching technique. From [26–29], they provided different kinds of single-stage structures, and they have different benefits and features individually. In reference [27], the number of switches is one, thus the switching loss is low. In reference [28,29], the number of switches is two. The switching losses are still low, but the performances of THD for these three references are moderate or even higher. For the proposed circuit, two of the switches are used for PFC and ACF functions, the other two switchers are used for synchronous
rectification for decreasing the conduction loss, and THD performs well among these studies. Table 1 shows a comparison of the related studies.

Table 1. Comparison of the related single-stage converter with soft-switching function.

| Item and No.   | Proposed | Ref. [26] | Ref. [27] | Ref. [28] | Ref. [29] |
|---------------|----------|-----------|-----------|-----------|-----------|
| Switch        | 4        | 1         | 1         | 2         | 2         |
| Inductor      | 2        | 2         | 1         | 3         | 1         |
| Diode         | 4        | 3         | 3         | 4         | 5         |
| Capacitor     | 4        | 2         | 3         | 4         | 5         |
| Windings      | 2        | n/a       | 3         | 4         | 2         |
| THD           | Low      | n/a       | Moderate  | High      | Moderate  |
| Switching loss| Moderate  | Low       | Low       | Low       | Low       |
| Efficiency(%) | 88.2     | 92.0      | 91.5      | 91.3      | 91.0      |

To combine with the PFC stage and the DC-DC converter into one simple circuit is the main concept of this paper. It not only reduces the number of components, but also delivers the energy to the output load directly. The proposed paper is to combine the PFC technique and ACF converter into the single-stage structure. The goal of this paper is to simplify the structure and also to implement the single-stage PFC and ACF converter with dual transformer. In this proposed circuit, the dual transformers with series input and parallel output connection were selected. The benefit of this connection is that each of the transformers only needs to deliver half of the power from input to the output load. The larger inductance causes smaller current variation on $L_m$. This situation can reduce the peak value and effective value of the primary side current. To compare with the volume of a single winding transformer, the dual transformers are indeed larger than the single one. However, the diameter of copper wire and the size of magnetic core can be smaller for dual transformer topology. In addition, the synchronous mechanism can reduce the conduction loss effectively. To sum up the characteristics and the functions above, the proposed topology is suitable for higher power demand adaptor applications, such as gaming laptops and mini-computers.

2. Proposed AC-DC Converter

2.1. The Proposed Circuit Structure

In this paper, a single-stage circuit with AC input and DC output was developed as shown in Figure 1. The proposed design utilizes a PFC boost topology to combine with the active clamp flyback converter without any external resonant inductor [9]. The clamping capacitor $C_{Clamp}$ can be shared as the common current path for both stages to reduce the number of main circuit components. The PFC stage is operated under discontinuous conduction mode for full range to lower the complexity of the PFC control method. Due to the characteristics of active clamping technique, ZVS can be easily achieved on both switches $S_1$ and $S_2$ at the primary side. In addition to that, the dual transformer connection and the synchronous rectification technique at the secondary side can reduce the conduction loss effectively.

2.2. Principle of Operation

Since the AC input voltage passes through a full-bridge rectifier, no matter whether the input voltage is positive or negative, the output voltage of the rectifier is still positive. Therefore, the following description will only focus on the positive waveform duration. As shown in Figure 2, due to the topology of the circuit, the sinusoidal waveform changes as the value of $|v_{in}(t)|$ changes. The waveform can be divided into the valley, the middle, and the peak point. The valley point means that the rectified voltage drops to 0 V and this valley point is operated as a conventional active clamp flyback converter. The peak points are influenced by the value of $|v_{in}(t)|$ the most. For the time axis, $\frac{\pi}{2}$ and $\frac{3\pi}{2}$ are the peak
points of the rectified voltage. The middle points are located between the valley and the peak points which are at $\frac{\pi}{4}$ and $\frac{3\pi}{4}$ of the time axis.

![Figure 1. Topology of the proposed circuit.](image)

![Figure 2. Output voltage from the rectifier circuit.](image)

After the definition of these critical points, the operation modes of the circuit will be discussed in this section. The current path of the primary side and the secondary side will be illustrated in different colors. The blue shows the power factor correction path. The red shows the active clamp current path. The green shows the current at the secondary side. These current paths help to simplify the following explanation, and the theoretical paths are shown in Figure 3.

2.2.1. Mode 1—($t_0 < t < t_1$)

As shown in Figure 4, due to the previous mode, the high side switch’s parasitic capacitor $C_{OSS1}$ is discharged to zero and then $S_1$ turns on in this mode. ZVS of $S_1$ can be achieved. At the beginning of this mode, the total leakage inductor $L_r$, the magnetic inductors $L_{m1}$ and $L_{m2}$ keep the same current direction and charge to $C_{Bus}$ as the previous state. The energy stored in the power factor correction inductor $L_{PFC}$ also charges to the capacitor $C_{Bus}$ at the same time. When the energy stored in $L_r$, $L_{m1}$, and $L_{m2}$ are released, the current direction of these inductors turns to be positive and starts to be charged. When the charging process of $C_{Bus}$ ends, the coming operation mode will be carried out. In this mode, there is no energy delivered to the secondary side. The switches $S_3$ and $S_4$ at the secondary side are turned off; hence, the energy of the output load $R_O$ is provided by the output capacitor $C_o$. Through the analysis above, Equations (1) and (2) can be obtained below. $\omega_1$ is the angular frequency of the AC input voltage. In this mode, the angular frequency $\omega$ and the impedance $Z$ are also shown in Equation (3).
\[ i_{LPFC}(t) = i_{LPFC}(t_0) \cdot \cos \omega(t - t_0) + \frac{[V_m \cdot \sin \omega_1(t - t_0) - V_{Bus} - v_{Clamp}(t_0)] \cdot \sin \omega(t - t_0)}{Z} \]  

(1)

\[ v_{Clamp}(t) = \left[ |V_m \cdot \sin \omega(t - t_0)| - V_{Bus} - v_{Clamp}(t_0) \right] \cdot (1 - \cos \omega(t - t_0)) + Z \cdot i_{LPFC}(t_0) \cdot \sin \omega(t - t_0) \]  

(2)

\[ \omega = \frac{1}{\sqrt{L_{PFC} \cdot C_{Clamp}}} ; \quad Z = \sqrt{\frac{L_{PFC}}{C_{Clamp}}} \]  

(3)

Figure 3. The related key waveforms of the proposed circuit.

2.2.2. Mode 2—(t_1 < t < t_2)

As shown in Figure 5, in this mode, \( S_1 \) still turns on. \( L_{PFC} \) continues releasing the energy and charging to the clamping capacitor \( C_{Clamp} \) from mode 1. \( L_{PFC} \) also charges to \( L_r, L_{m1}, \) and \( L_{m2} \). In the meantime, \( C_{Bus} \) also charges to \( L_r, L_{m1}, \) and \( L_{m2} \) through \( S_1 \). When the energy of \( L_{PFC} \) is exhausted, \( i_{LPFC} \) drops to 0 A. Thus, \( V_{Clamp} \) starts to be clamped at a constant voltage temporarily. This mode ends when \( S_1 \) is turned off.
2.2.3. Mode 3—($t_2 < t < t_3$)

As shown in Figure 6, during the dead time, $C_{OSS1}$ is charged by the path of $C_{Bus}$. The charging path will be open when $C_{OSS1}$ is charged to the sum of $V_{Bus}$ and $V_{Clamp}$. Since $L_{r}$, $L_{m1}$, and $L_{m2}$ maintain the same current direction from the previous step, the energy on $C_{OSS2}$ will be taken away while the current goes through $S_2$. After $C_{OSS2}$’s energy releases to zero, $S_2$’s body diode $D_{S2}$ will be turned on to maintain the negative current path. This mode ends when dead time is finished. In this step, no energy is transmitted to the output load. The secondary side switches $S_3$ and $S_4$ are turned off, the energy of the output load $R_O$ is provided by the output capacitor $C_o$. Equation (4) can be analyzed through this step; $\omega$ and Z’s equation are shown in (5).

\[
i_{Lr}(t) = i_{Lr}(t_2) \cdot \cos(\omega(t-t_2)) + \frac{V_{Bus} \cdot \sin(\omega(t-t_2))}{Z} \quad (4)
\]

\[
\omega = \frac{1}{\sqrt{(L_r+2L_m) \cdot (C_{OSS1}+C_{OSS2})}} ; \quad Z = \sqrt{\frac{L_r+2L_m}{C_{OSS1}+C_{OSS2}}} \quad (5)
\]
Figure 6. Current route of Mode 3.

2.2.4. Mode 4—($t_3 < t < t_4$)

As shown in Figure 7, due to the previous mode, the low side switch’s capacitor $C_{OSS2}$ is released to zero during the switching of $S_2$ in this mode. $S_2$’s ZVS can be achieved. $L_{PFC}$ will be charged by input AC power. $L_r$ and $C_{Clamp}$ start to resonate with each other, the next mode begins when $L_r$ releases its energy to zero. The magnetizing inductors $L_m1$ and $L_m2$ transfer energy to secondary side, $v_{GS3}$ and $v_{GS4}$ turn high to achieve synchronous rectification function to reduce losses of $S_3$ and $S_4$. Equations (6) and (7) can be analyzed through this step; $\omega$ and $Z$’s equation are shown in (8).

$$i_{Lr}(t) = i_{Lr}(t_3) \cdot \cos[\omega(t - t_3)] + \frac{[2 \cdot n \cdot V_O - v_{Clamp}(t_3)] \cdot \sin[\omega(t - t_3)]}{Z}$$

(6)

$$v_{Clamp}(t) = \left[2 \cdot n \cdot V_O - v_{Clamp}(t_3) \right] \cdot (1 - \cos[\omega(t - t_3)]) + Z \cdot i_{Lr}(t_3) \cdot \sin[\omega(t - t_3)]$$

(7)

$$\omega = \frac{1}{\sqrt{L_r \cdot C_{Clamp}}}; \quad Z = \sqrt{\frac{L_r}{C_{Clamp}}}$$

(8)

Figure 7. Current route of Mode 4.

2.2.5. Mode 5—($t_4 < t < t_5$)

As shown in Figure 8, due to the exhaustion of $L_r$, $C_{Clamp}$ releases its energy to $L_r$. Both components keep resonating with the opposite current direction as shown in mode 4. $L_m1$ and $L_m2$ release their energy to secondary side at the beginning of this step. When both of the magnetizing inductors release to zero, $C_{Clamp}$ will transfer its energy to $L_m1$, $L_m2$, and the secondary side. The current direction of $i_{Lm1}$ and $i_{Lm2}$ will be opposite to the beginning of this step. $L_m1$ and $L_m2$ transfer energy to secondary at the beginning of this step, $C_{Clamp}$ will keep transferring when the magnetizing inductors are out of energy. $v_{GS3}$ and $v_{GS4}$ remain high to
achieve synchronous rectification function for reducing losses of \( S_3 \) and \( S_4 \). Equations (9) and (10) can be analyzed through this step; \( \omega \) and \( Z \)’s equation are shown in (11).

\[
    i_{Lr}(t) = -i_{Lr}(t_4) \cdot \cos \omega(t - t_4) + \frac{2 \cdot n \cdot V_O - v_{Clamp}(t_4)}{Z} \cdot \sin \omega(t - t_4) \tag{9}
\]

\[
    v_{Clamp}(t) = \left[ 2 \cdot n \cdot V_O - v_{Clamp}(t_4) \right] \cdot (1 - \cos \omega(t - t_4)) + Z \cdot i_{Lr}(t) \cdot \sin \omega(t - t_4) \tag{10}
\]

\[
    \frac{1}{\sqrt{L_r \cdot C_{Clamp}}}; \quad Z = \sqrt{\frac{L_r}{C_{Clamp}}} \tag{11}
\]

![Figure 8. Current route of Mode 5.](image)

2.2.6. Mode 6—(\( t_5 < t < t_6 \))

As shown in Figure 9, during the dead time, \( C_{OSS2} \) starts to be charged. The charging path is open when \( C_{OSS2} \) is charged to the sum of \( V_{Bus} \) and \( v_{Clamp} \). Since \( L_r, L_m1, \) and \( L_m2 \) maintain the same current direction from the previous step, the energy on \( C_{OSS1} \) will be taken away during the current went through \( S_1 \). After \( C_{OSS1} \)’s energy releases to zero, \( S_2 \)’s body diode \( D_{S2} \) is turned on to maintain the negative current path. In this mode, \( L_{PFC} \) starts to discharge and to release energy to \( C_{Clamp}, \) \( V_{Bus} \), and \( C_{OSS2} \). \( C_{OSS1} \) also discharges at the same time. This mode ends when dead time is finished. \( C_{Clamp} \) keeps transferring energy to secondary side. \( v_{GS3} \) and \( v_{GS4} \) remain high to achieve synchronous rectification function. Equation (12) can be analyzed through this step; \( \omega \) and \( Z \)’s equation are shown in Equation (13).

\[
    i_{Lr}(t) = \frac{2 \cdot n \cdot V_O - v_{Clamp}(t_5)}{Z} \cdot \sin \omega(t - t_5) - i_{Lr}(t_5) \cdot \cos \omega(t - t_5) \tag{12}
\]

\[
    \omega = \sqrt{\frac{L_r}{(C_{OSS1} + C_{OSS2})}} \quad Z = \frac{L_r}{\sqrt{C_{OSS1} + C_{OSS2}}} \tag{13}
\]

2.3. Design Consideration

In order to simplify the design of single-stage architecture, the power factor correction inductor is designed to operate under discontinuous conduction mode [10,11]. The extra input voltage or current signal detection mechanism for continuous conduction mode or boundary conduction mode [12,13] can be removed. In the case of discontinuous conduction mode, Figure 10 can be drawn. The relationship of \( i_{L_{PFC}} \) during the on and off time of the power switch can be obtained through the operation process, where \( v_{total}(t') \) represents \( V_{Bus} + v_{Clamp}(t') \).
In the case of discontinuous conduction mode, Figure 10 can be drawn. The relationship of $i_{\text{LPFC}}$ during the on and off period is open when $D_1$ starts to be charged. The charging period can be obtained through the operation process, where $V_m$ represents the input peak voltage, $D_{\text{on}}$ is the duty cycle of $S_2$, $T_S$ is the switching period, and $x$ is the voltage ratio, as shown in Equation (15). After combining Equations (14) and (15), Figure 11 can be derived from Figure 10 and references [14,15]. Where $v_{\text{total}}(t')$ is the voltage ratio, as shown in Equation (15). After combining Equations (14) and (15), Figure 11 can be drawn. The waveform of $i_{\text{LPFC}}$ and switches.

Equation (14) can be derived from Figure 10 and references [14,15]. Where $V_m$ represents the input peak voltage, $D_{\text{on}}$ is the duty cycle of $S_2$, $T_S$ is the switching period, and $x$ is the voltage ratio, as shown in Equation (15). After combining Equations (14) and (15), Figure 11 can be obtained. The x-axis represents $D_{\text{on}}$, and y-axis represents voltage ratio $x$. Through a single curve, it can be noticed that the range of $x$ will increase during the increment of $D_{\text{on}}$. In order to avoid excessive variation of the output voltage, $D_{\text{on}}$ is set under 40%. Different curves can be compared under the same variation range of $D_{\text{on}}$. Take the range of $D_{\text{on}}$ varying from 30% to 40% as an example, $x$ increases to 0.304 with $L_{\text{PFC}}$ of 60 $\mu$H, but $x$ increases to 0.833 with $L_{\text{PFC}}$ of 40 $\mu$H. It can be seen that the smaller inductance causes a higher voltage variation range. Larger variation of $x$ also causes a higher voltage spike to increase the switching loss during the transient time. To avoid the higher voltage variation, the inductance of $L_{\text{PFC}}$ should be higher. However, if $L_{\text{PFC}}$ is high, $i_{\text{LPFC}}$ still has to be in discontinuous conduction mode at the same time to avoid the decrement of power factor. If the converter operates in heavy load condition or the peak value of $i_{\text{LPFC}}$ goes to continuous conduction mode, these impacts will decrease the power factor. Therefore, the trade-off between loss and the power factor for the inductance of $L_{\text{PFC}}$ should be designed carefully.

$$L_{\text{PFC}} = \frac{V_m^2 D_{\text{on}}^2 T_S}{2 P_m} \times \left( \frac{x^3}{\sqrt{x^2 - 1}} \right)^{-1} \left( 1 + \frac{2}{\pi} \tan^{-1} \left( \frac{x}{\sqrt{x^2 - 1}} \right) \right) - x^2 - \frac{2}{\pi} x$$

$$x = \frac{v_{\text{total}}(t')}{V_m} = \frac{V_{\text{Bus}} + v_{\text{Clamp}}(t')}{V_m}$$

Figure 9. Current route of Mode 6.

Figure 10. The waveform of $i_{\text{LPFC}}$ and switches.
To compare with the conventional boost topology for single stage structure [16], the power factor correction stage includes $C_{\text{Clamp}}$ in the proposed topology. Figure 12 can be obtained through Equation (2) under different $v_{\text{in}}$. Noticing $v_{\text{Clamp}}$ is influenced by $v_{\text{in}}$, the value of $v_{\text{DS1}}$ and $v_{\text{DS2}}$ will be influenced as well. Therefore, the value of $C_{\text{Clamp}}$ is related to the switching loss of the primary switches. In Figure 12, the x-axis represents the time and the y-axis represents $v_{\text{Clamp}}$.

**Figure 12.** Relationship between $v_{\text{Clamp}}$ and $v_{\text{in}}$.

$C_{\text{Clamp}}$ and $L_r$ are the main resonant components when $S_2$ turns on. The resonant period $T_r$ between the two elements is about twice of the turn-on time when $S_2$ is on as shown in Equation (16). $C_{\text{Clamp}}$ will affect the switching loss and the capacitance of $C_{\text{Clamp}}$ can be further optimized by SIMetrix software. As shown in Figure 13a, the smaller capacitance can reduce the switching loss of $S_2$. In the meanwhile, from Figure 13b, this will also increase the conduction loss of the synchronous rectifier switch at the secondary side. That is, the smaller capacitance causes higher current at the secondary side. Therefore, the capacitance selection of $C_{\text{Clamp}}$ should be considered carefully.

$$C_{\text{Clamp}} = \frac{D_{\text{out}}^2 \cdot T_r^2}{\pi^2 \cdot L_r}$$  (16)
Since $S_2$ needs to withstand the current stress from $L_{PFC}$ and $C_{Clamp}$ in mode 4 and 5, the switching loss of $S_2$ has a great impact for the efficiency. In order to reduce the switching loss caused by $S_2$, the value of $L_m$ is designed to be larger than $L_{m(min)}$ to reduce the peak current at the primary side. By using the voltage-second balancing law, Equation (17) can be obtained. Where $L_{m(min)}$ represents the minimum inductance of the continuous conduction mode. In this proposed topology, $L_{m(min)}$ is twice that of the conventional single transformer connection under this condition. This design consideration makes $S_1$ have no ZVS function without $L_m$, which causes the failure of ZVS at the valley part. However, the overall efficiency still can be improved by reducing the switching loss of $S_2$.

$$L_{m(min)} = \frac{D_{on}^2 R_{O} n^2 \eta}{f}$$  \hspace{1cm} (17)

A step-by-step design flow chart of proposed converter is shown in Figure 14. The parameters of the converter can be acquired step by step. At first, the input and the output specifications have to be determined. Then, the following parameters of key components can be calculated by using Equations (14), (16) and (17). After all the key components are obtained, the optimization with Matlab is verified to avoid $L_{PFC}$ entering into CCM or ZVS failure. Finally, the circuit can be implemented efficiently.

### 2.4. Switch Utilization Ratio

The definition of switch utilization ratio ($U$) is the output power of the converter circuit derived per unit of switch stress. For this study, the proposed ACF converter of $D_{on}$ is set for 0.35 in practical design consideration. Therefore, the peak of $U$ is 0.385 from the figure. The curve of $U$ is plotted as shown in Figure 15.

### 2.5. Steady-State Voltage Gain with Varying Duty

In Figure 16, the steady-state voltage gain is depicted with varying duty-cycle. It shows a curve of the steady-state voltage gain response of the proposed converter for the duty-cycle changing from 10% to 100%.
2.4. Switch Utilization Ratio

The definition of switch utilization ratio (U) is the output power of the converter circuit derived per unit of switch stress. For this study, the proposed ACF converter of D is set for 0.35 in practical design consideration. Therefore, the peak of U is 0.385 from the figure. The curve of U is plotted as shown in Figure 15.

Figure 14. Design flow chart of proposed converter.

Figure 15. Switch utilization ratio with different $D_{on}$. 
Output current time, which is much shorter than the middle point and the valley point during the resonant full load condition. In order to reduce the switching loss without detecting input signals.

In discontinuous conduction mode, the power factor correction function can be achieved.

Figure 16 shows the simulation waveforms during the valley point to verify the experimental results. As shown in Figure 22, Table 2 will achieve ZVS through the current of \( i_{\text{Lm}} \).

Table 3. Component parameters.

| Parameters          | Value   |
|---------------------|---------|
| \( L_{\text{PFC}} \) | 55 \( \mu \)H |
| \( L_r \)           | 5.4 \( \mu \)H |
| \( L_{m1}, L_{m2} \) | 31 \( \mu \)H |
| \( N_{p1}:N_{s1} \) | 3.33:1 |
| \( N_{p2}:N_{s2} \) | 3.33:1 |
| \( C_{\text{Bus}} \) | 820 \( \mu \)F |
| \( C_{\text{Clamp}} \) | 30 nF |

Figure 17 shows the waveforms of input voltage \( v_{\text{in}} \), current \( i_{\text{in}} \), and \( i_{L_{\text{PFC}}} \) under light load 30 W. Figure 18 shows the waveform of full load 120 W. Since \( i_{L_{\text{PFC}}} \) is designed for discontinuous conduction mode, the power factor correction function can be achieved without detecting input signals.

Figure 17 shows the waveforms of input voltage \( v_{\text{in}} \), current \( i_{\text{in}} \), and \( i_{L_{\text{PFC}}} \) under light load condition \( v_{\text{in}} \): 100 V/div, \( i_{L_{\text{PFC}}} \): 2 A/div, \( i_{\text{in}} \): 1 A/div, Time: 5 ms/div.

3. Experimental and Simulation Result

The specification of the proposed circuit is shown in Table 2, and Table 3 shows the parameters of the proposed circuit. \( L_r \) is the total leakage inductance of the dual transformers.

Table 2. Circuit specification.

| Parameters       | Value                     |
|------------------|---------------------------|
| Input voltage \( V_{\text{in}} \) | 110 V, 60 Hz 19 V         |
| Output voltage \( V_o \)   | 6.32 A                    |
| Output current \( I_o \)   | 300 kHz                   |
| Switching frequency \( f_s \) |                          |

Figure 16. Steady-state voltage gain with different duty.
The waveforms are measured at valley, middle, and peak points individually under full load condition. In order to reduce the switching loss on full load condition, \( L_m \) is designed to be larger than \( L_{m\text{min}} \) for lowering the peak current. This situation causes \( i_{Lm} \) to be positive during valley point. ZVS of \( S_1 \) will fail without \( L_m \) in mode 6 shown Figure 19. On the other hand, \( S_2 \) will achieve ZVS through the current of \( L_r, L_{m1}, \) and \( L_{m2} \) shown in Figure 20. Figure 21 shows the simulation waveforms during the valley point to verify the experimental results. As shown in Figure 22, \( L_r \) and \( C_{\text{Clamp}} \) only resonate during the turn off time of \( S_1 \), which is much shorter than the middle point and the valley point during the resonant time.

![Figure 18. Input and \( i_{\text{LPFC}} \) waveforms under full load condition \( v_{\text{in}}: 100 \text{ V/div}, i_{\text{LPFC}}: 5 \text{ A/div}, i_{\text{in}}: 5 \text{ A/div}, \text{Time: 5 ms/div.} \)](image)

At the middle point under the full load condition, \( i_{\text{LPFC}} \) helps the negative current to flow through \( S_1 \) for achieving ZVS in mode 1 as shown in Figure 23. From Figure 24, they show the period resonated by \( L_{\text{PFC}} \) and \( C_{\text{Clamp}} \). In this situation, the extension of resonant time for \( v_{\text{Clamp}} \) will also influence \( S_1 \) and \( S_2 \)’s switching loss. \( S_2 \) achieves ZVS through the current from \( L_r, L_{m1}, \) and \( L_{m2} \) in mode 2 as shown in Figure 25. In Figure 26, it shows the simulation waveforms to verify the experimental results. Because the current of \( S_2 \) is the summation of \( i_{Lr} \) and \( i_{\text{LPFC}} \), the peak of \( i_{DS2} \) will increase when \( i_{\text{LPFC}} \) increases.

![Figure 19. \( S_1 \)’s waveform during valley point \( i_{DS1}: 2 \text{ A/div}, v_{DS1}: 100 \text{ V/div}, v_{GS1}: 20 \text{ V/div, Time: 2 \mu s/div.} \)](image)

![Figure 20. \( S_2 \)’s waveform during valley point \( i_{DS2}: 5 \text{ A/div}, v_{DS2}: 100 \text{ V/div}, v_{GS2}: 20 \text{ V/div, Time: 2 \mu s/div.} \)](image)
show the period resonated by the point as shown in Figure 27. This is most severe at the peak point, which reduces the switching loss caused by the simulation waveforms to verify the experimental results. Because the current of $i_{DS}$ as shown in Figure 29, it can be seen that the charging and discharging behavior of $i_{DS}$ helps the negative current to flow through $L_r$, $S_1$, and $S_2$ to achieve ZVS in mode 1 as shown in Figure 23. From Figure 24, they will also influence $i_{Lr}$, $S_1$, and $S_2$ to achieve ZVS by the total current of $i_{Lr}$, $i_{DS}$, and $i_{LPFC}$, the peak of $L_m$ in mode 2 as shown in Figure 25. In Figure 26, it shows the related waveform during middle point, Time: 2 $\mu$s/div.

Due to the negative current of $i_{LPFC}$, $v_{Clamp}$, and $v_{GS1}$, $S_1$ turns off momentarily. On the other hand, the higher $i_{LPFC}$, $S_2$ will increase when $v_{Clamp}$ helps the negative current to flow through $L_r$, $S_1$, and $S_2$ to achieve ZVS through the related waveform during valley point, Time: 2 $\mu$s/div.

In Figure 30, the simulation waveform during the peak point is shown to verify the experimental results.

Figure 21. Simulation of $S_1$ and $S_2$ related waveform during valley point, Time: 2 $\mu$s/div.

Figure 22. $C_{Clamp}$ related waveforms during valley point $i_{LPFC}$: 5 A/div, $v_{Clamp}$: 50 V/div, $v_{GS1}$: 10 V/div, Time: 2 $\mu$s/div.

Figure 23. $S_1$’s waveform during middle point $i_{DS1}$: 2 A/div, $v_{DS1}$: 100 V/div, $v_{GS1}$: 20 V/div, Time: 2 $\mu$s/div.

Figure 24. $C_{Clamp}$ relation waveforms during middle point $i_{LPFC}$: 5 A/div, $v_{Clamp}$: 50 V/div, $v_{GS1}$: 10 V/div, Time: 2 $\mu$s/div.
Due to the negative current of $i_{\text{PFC}}$, $S_1$ can easily achieve ZVS function at the peak point as shown in Figure 27. $S_2$ also achieves ZVS by the total current of $L_r$, $L_{m1}$, and $L_{m2}$ as shown in Figure 28. Under the influence of $v_{\text{Clamp}}$’s variation, the higher $v_{DS1}$ with the lower $i_{DS1}$ occurs at the moment when $S_1$ turns off momentarily. On the other hand, the higher $i_{DS2}$ with the lower $v_{DS2}$ occurs at the moment when $S_2$ turns off instantaneously. This complementary situation is achieved by the appropriate selection of the clamping capacitance. As shown in Figure 29, it can be seen that the charging and discharging behavior of $v_{\text{Clamp}}$ is most severe at the peak point, which reduces the switching loss caused by $S_2$ indirectly. In Figure 30, the simulation waveform during the peak point is shown to verify the experimental results.

**Figure 25.** $S_2$’s waveform during middle point $i_{DS2}$: 5 A/div, $v_{DS2}$: 100 V/div, $v_{GS2}$: 20 V/div, Time: 2 $\mu$s/div.

**Figure 26.** Simulation of $S_1$ and $S_2$ related waveform during middle point, Time: 2 $\mu$s/div.

**Figure 27.** $S_1$’s waveform during peak point $i_{DS1}$: 2 A/div, $v_{DS1}$: 100 V/div, $v_{GS1}$: 20 V/div, Time: 2 $\mu$s/div.
Because of the extension of $L_r$ and $C_{Clamp}$’s resonant time, the waveform of $i_{DS2}$ will be affected. The difference of $i_{DS2}$ between Figures 20 and 28 can clearly be seen. This situation will further affect the waveforms of $i_{DS3}$ and $i_{DS4}$. From Figure 31, the current of $i_{DS3}$ and $i_{DS4}$ are smaller at the secondary side for reducing the switching loss of $S_3$ and $S_4$ effectively.

In Figure 32, the efficiency of the proposed converter is measured and summarized. At light load condition, the efficiency starts from 85.8%. When the output goes to full load, the efficiency reaches 88.20%.

**Figure 28.** $S_2$’s waveform during peak point $i_{DS2}$: 2 A/div, $v_{DS2}$: 100 V/div, $v_{GS2}$: 20 V/div, Time: 2 μs/div.

**Figure 29.** $C_{Clamp}$ related waveforms during peak point $i_{LPFC}$: 5 A/div, $v_{Clamp}$: 50 V/div, $v_{GS1}$: 10 V/div, Time: 2 μs/div.

**Figure 30.** Simulation of $S_1$ and $S_2$ related waveform during peak point, Time: 2 μs/div.
Due to the single-stage structure, the two switches at the primary side should withstand the current stress from both side of PFC and ACF stage as shown in mode 1 and mode 5. This will cause switching loss and conduction loss on these two switches to dominate a major part of the total loss for this circuit, especially for higher switching frequency. To compare with CCM PFC converters for detecting AC input signal, the proposed topology has a slightly higher THD causing PF to drop slightly. The reason is that the designed $L_{PFC}$

In addition, harmonic current is also a key factor to verify the PFC function. In Figure 29, the harmonic current of the proposed converter is measured which is shown in green bars. Moreover, the standard of IEC-61000-3-2 is compared which is shown in blue bars. Based on Figure 33, the current of odd-harmonic is lower than the standard.

Due to the single-stage structure, the two switches at the primary side should withstand the current stress from both side of PFC and ACF stage as shown in mode 1 and mode 5. This will cause switching loss and conduction loss on these two switches to dominate a major part of the total loss for this circuit, especially for higher switching frequency. To compare with CCM PFC converters for detecting AC input signal, the proposed topology has a slightly higher THD causing PF to drop slightly. The reason is that the designed $L_{PFC}$
needs to keep the PFC current operating in DCM for low power applications, and there is no need to detect any input signal.

As shown in Table 4, after the measurements, the power factor and the efficiency reached 0.977 and 85.84% under light load. At full load condition, the power factor reached 0.984 and the efficiency goes to 88.20%. Table 5 also shows a calculation for power loss of these switches under full load condition.

Table 4. Experimental measurement.

| Loading Level | 25%    | 50%    | 75%    | 100%   |
|---------------|--------|--------|--------|--------|
| \( v_{in} \)  | 109.89 V | 109.92 V | 109.89 V | 109.92 V |
| \( i_{in} \)  | 326.6 mA  | 638.1 mA  | 955.8 mA  | 1.26 A |
| \( V_{O} \)   | 19.05 V   | 19.01 V   | 19.02 V   | 19.02 V |
| \( I_{O} \)   | 1.58 A    | 3.16 A    | 4.74 A    | 6.32 A |
| PF            | 0.977     | 0.979     | 0.978     | 0.984     |
| Eff%          | 85.84%    | 87.48%    | 87.78%    | 88.20%    |

Table 5. Power losses calculation on the switches at primary and secondary sides [30].

| Item.       | Model No. | \( R_{DS(ON)}/C_{iss} \) | Conduction Loss \((I_{DS,RMS}^2 \times R_{DS(ON)}) \times 2\) | Switching Loss \(\frac{1}{2} \times (C_{iss} \times V_{GS}^2 \times f \times 2)\) |
|-------------|-----------|---------------------------|-------------------------------------------------|---------------------------------------------------------------------|
| Pri. \((S_1, S_2)\) | C3M0065090D | 65 mΩ/660 pF               | 0.206 W (for 2 pcs)                                  | 0.045 W (for 2 pcs)                                                  |
| Sec. \((S_3, S_4)\) | BSC160N15NS  | 16 mΩ/1370 pF             | 1.278 W (for 2 pcs)                                  | 0.093 W (for 2 pcs)                                                  |

The prototype of the proposed single-stage PFC active-clamp flyback converter with dual transformers is shown in Figure 34. The output power is 120 W (19 V, 6.32 A) which is suitable for laptop adaptor application. The dimension is measured in centimeters (12.5 cm × 15 cm).

Figure 34. Prototype of the proposed single-stage PFC ACF with dual transformers.

4. Conclusions

This paper proposes a single-stage active clamp flyback converter with dual transformers in series and parallel connection which is implemented. Through the proposed design, the PFC inductor assists the negative current path of the high-side power switch \( S_1 \) for achieving ZVS without any additional inductors except the rectified voltage drops to the valley point. The proposed design can not only decrease the switching loss but also
lower the number of the components. $S_2$ can also achieve ZVS by the magnetizing current from the dual transformers.

By connecting the dual transformers in series connection at primary side and parallel connection at secondary side, the copper loss and the conduction loss can be saved effectively. The efficiency of 88.20% with power factor 0.984 under full load condition has been achieved.

**Author Contributions:** S.-T.W. conceptualized and supervised the experiments of the research. S.-T.W. revised and modified the research data into paper format. Y.-T.C. Cheng was in charge of environment building up. Y.-T.C. Cheng was in charge of measurement and data recording. All authors have read and agreed to the published version of the manuscript.

**Funding:** This research is supported by Ministry of Science and Technology. The project number of the foundation: MOST 110-2221-E-150-017.

**Institutional Review Board Statement:** Not applicable.

**Informed Consent Statement:** Not applicable.

**Data Availability Statement:** Data sharing not applicable.

**Conflicts of Interest:** The authors declare no conflict of interest.

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