Research Article

Spiking Neural P Systems with Polarizations and Rules on Synapses

Suxia Jiang,¹ Jihui Fan,¹ Yijun Liu,¹ Yanfeng Wang,¹ and Fei Xu,²

¹Henan Key Lab of Information Based Electrical Appliances, School of Electrical and Information Engineering, Zhengzhou University of Light Industry, Zhengzhou 450002, Henan, China
²Key Laboratory of Image Information Processing and Intelligent Control of Education Ministry of China, School of Artificial Intelligence and Automation, Huazhong University of Science and Technology, Wuhan 430074, Hubei, China

Correspondence should be addressed to Suxia Jiang; jiangsx913@126.com and Fei Xu; fei_xu@hust.edu.cn

Received 23 December 2019; Revised 27 May 2020; Accepted 16 June 2020; Published 9 July 2020

Academic Editor: Dimitri Volchenkov

Copyright © 2020 Suxia Jiang et al. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

Spiking neural P systems are a class of computation models inspired by the biological neural systems, where spikes and spiking rules are in neurons. In this work, we propose a variant of spiking neural P systems, called spiking neural P systems with polarizations and rules on synapses (PSNRS P systems), where spiking rules are placed on synapses and neurons are associated with polarizations used to control the application of such spiking rules. The computation power of PSNRS P systems is investigated. It is proven that PSNRS P systems are Turing universal, both as number generating and accepting devices. Furthermore, a universal PSNRS P system with 151 neurons for computing any Turing computable function is given. Compared with the case of SNP systems with polarizations but without spiking rules in neurons, less number of neurons are used to construct a universal PSNRS P system.

1. Introduction

Membrane computing is a burgeoning branch of natural computing that develops new computation models based on the structure and functioning of living cells [1, 2]. Membrane systems (also called P systems) are distributed parallel computation models in membrane computing. There are three main classes of P systems, based on the structure of membranes inside living cells: cell-like P systems [3], tissue-like P systems [4], and neural-like P systems [5]. In the field of mathematical and theoretical computer science, P systems are used to investigate numerous types of problems, such as the Turing universality of the system [6, 7], complexity classes [8], numerical problems [9, 10], NP-complete problems [11–13], and P systems simulation [14, 15]. The reader can consult [16] for more comprehensive information about membrane computing. Up-to-date research results and open problems can be found on the membrane computing website http://ppage.psystems.eu.

Spiking neural P systems (SN P systems) are a class of neural-like P systems, inspired by the biological phenomenon of neurons conveying information by communicating with each other via identical electric impulses (spikes) [17]. In this type of systems, only one type of spike exists, and the information is encoded by the timing and number of spikes. SN P systems are a class of computation models that use spiking/forgetting rules, which is applied by matching the number of spikes with the regular expression. Many variants of SN P systems have been proposed based on various biological characteristics, such as scheduled synapses [18], structural plasticity [19, 20], thresholds [21, 22], and multiple channels [23]. Meanwhile, there are also extensive studies in the view of the mechanism of information communication between neurons, such as white hole neurons [24], request rules [25], inhibitory rules [26], and communication on request [27]. Most of these systems have been proven to have the equivalent computation power with Turing machine.

In addition, SN P systems have been widely investigated in the field of computer science, which can be used to produce binary and string languages [28–31] and simulate the registration machine [32, 33]. With the development of
the research, the SN P systems as small universal computing devices are studied [34, 35]. Moreover, SN P systems and their variants have been successfully implemented in real-life applications, for instance, logic gate design [36], image processing [37], fault diagnosis of electric power systems [38–40], optimization algorithm design for combinatorial optimization problems [41, 42], and robot control [43–46].

Recently, a variant of SN P systems called SN P systems with polarizations (PSNP systems) was proposed in [47], where the rules are controlled by three electrical charges (−, 0, +) associated with each neuron, not by the regular expression; it is closer to biological reality. In PSNP systems, the use of rules is more limited compared with SN P systems, because only three electrical charges can be selected, but SN P systems as number devices proved to be Turing universal. As universal computing devices, the computing process of PSNP P systems is complicated, and a total of 164 neurons (computational resources) are consumed. It is an open problem whether to find such systems that consume less computational resources, such as using extended spiking rules and delay functions and so on. Herein, we are inspired by the functioning of reflex arcs; the brain sends different signals to different cells to elicit responses. We investigate the computation power of SN P systems with rules on synapses? what about the computation power of SN P systems with rules on synapses? Hence, it is also interesting to construct a variant of SN P systems with rules on synapses, where the rules are not controlled by the regular expression.

In this work, inspired by the open problems raised in [47], we put the rules on synapses, proposing SN P systems with polarizations and rules on synapses (PSNRS P systems, for short). In PSNRS P systems, the rules associated with each neuron are placed on synapses, and when the polarity of a neuron meets some rules of its synapses, the rules are activated, and the neuron sends different number of spikes and the same electrical charge to its neighboring neurons. Compared with neurons in PSNP P systems that can only send the same number of spikes at some point to its neighboring neurons, the rules on synapses in PSNRS P systems will be more flexible. We investigate the computation power of PSNRS P systems working in the maximally parallel mode. The main contributions of the present work are summarized as follows:

(i) Rules on synapses and polarizations are considered in SN P systems; we construct a variant of SN P systems, called SN P systems with polarizations and rules on synapses (PSNRS P systems). In PSNRS P systems, polarization is used to control the application of spiking/forgetting rules associated with each synapse of the neurons.

(ii) The computation power of PSNRS P systems is investigated. Specifically, we prove that PSNRS P systems as accepting devices and generating devices achieve universality. Furthermore, a universal PSNRS P system with 151 neurons for computable functions is presented. Compared to the PSNP P system, 13 neurons were reduced in computational resources.

The rest of this paper is organized as follows. The formal definition of PSNRS P systems is introduced in the next section. The computation power of PSNRS P systems as number generators and acceptors is investigated in Section 3. In Section 4, a small universal PSNRS P system for computable functions is given. Finally, conclusions and suggestions for further work are presented in Section 5.

2. Spiking Neural P Systems with Polarizations and Rules on Synapses

In this section, we first review some prerequisites. For details on the basic elements of membrane computing and automata theory, the reader can refer to [16, 49]. $V^*$ is the set of all words over the alphabet, including the empty string $\lambda$. $V^* - \{\lambda\}$ corresponds to the set of nonempty words over $V$ and is denoted by $V^+$. The family of sets of natural numbers computed by Turing machines is denoted by NRE.

In the following definition, the notions of polarity and rules on synapses will be used. Only a brief introduction is provided here; please refer to [47, 48, 50] for details.

A PSNRS P system of degree $m \geq 1$ is a construction as follows:

$$\Pi = (O, \sigma_1, \sigma_2, \sigma_3, \ldots, \sigma_m, \text{syn}, \text{in}, \text{out}),$$

where

(i) $O = \{a\}$ is an alphabet and $a$ denotes the spike

(ii) $\sigma_1, \sigma_2, \sigma_3, \ldots, \sigma_m$ are neurons of the form $\sigma_i = (\alpha_i, n_i), 1 \leq i \leq m$ ($m$ is the number of neurons), where

(a) $\alpha_i \in \{-, 0, +\}$ is the initial polarity of neuron $\sigma_i$

(b) $n_i$ is the number of spikes initially located in $\sigma_i$

(iii) $\text{syn} \in \{1, 2, 3, \ldots, m\} \times \{1, 2, 3, \ldots, m\}$; syn is the sets of synapses; each element is a pair of the form $(i, j, R_{(i,j)})$, where $(i, j)$ indicates that there is a synapse connecting neurons $\sigma_i$ and $\sigma_j$, with $i, j \in \{1, 2, 3, \ldots, m\}, i \neq j$, and $R_{(i,j)}$ is a finite set of rules of the following two forms:

(a) $a/\alpha^c \rightarrow a/\beta; \text{for } \alpha, \beta \in \{-, 0, +\}, c \geq 1$ (spiking rules)

(b) $a/\alpha^c \rightarrow \lambda/\beta; \text{for } \alpha, \beta \in \{-, 0, +\}, c \geq 1$ (forgetting rules)

(iv) in, out $\in \{1, 2, \ldots, m\}$ indicates the input and output neurons, respectively

The spiking rules are applied as follows. If neuron $\sigma_i$ contains $k$ spikes and has $\alpha$ charge ($\alpha^k \in L(E)$, $k \geq c$), then the spiking rule $a/\alpha^c \rightarrow a/\beta$ is enabled. Meanwhile, $c$ spikes from neuron $\sigma_i$ are consumed, and a spike and $\beta$ charge are sent to neuron $\sigma_j$ via a synapse $(i, j)$. Note that
each synapse can have rules, and they do not affect each other, indicating that neuron \( \sigma_i \) sends a difference charge to adjacent neurons.

A forgetting rule \( a / a^c \rightarrow \lambda ; \beta \) is used when neuron \( \sigma_i \) maintains a charge and at least \( c \) spikes, so that all \( c \) spikes are removed from neuron \( \sigma_j \) and the \( \beta \) charge is sent to neuron \( \sigma_j \) by synapse \((i, j)\).

At some point, if a rule from \( R_{i,j} \) can be used by a synapse \((i, j)\), the rule must be used. If several rules from \( R_{i,j} \) can be used by a synapse, these rules are chosen nondeterministically. For example, there are two firing rules, \( a_i / a^c \rightarrow a_i / a^c \rightarrow a_i / a^c \), and the \( \beta \) charge is sent to neuron \( \sigma_i \) by synapse \((i, j)\).

In addition, system \( \Pi \) can work in an accepting mode, can be constructed by the Church–Turing thesis. For this, a specific PSNRS P system \( \Pi \) is constructed to simulate a register machine \( M \), and the register machine \( M = (\alpha, \Pi, \Sigma, \delta, \Gamma, \zeta, \zeta) \) is considered as a number generator. Usually, the time interval between the first two spikes output by the output neuron is used as the result of a computation. The number \( t_2 - t_1 \) is said to be computed by systems \( \Pi \), denoted by \( N_2(\Pi) \).

In this work, system \( \Pi \) is considered as a number generator. Usually, the time interval between the first two spikes output by the output neuron is used as the result of a computation. The number \( t_2 - t_1 \) is said to be computed by systems \( \Pi \), denoted by \( N_2(\Pi) \).

In addition, system \( \Pi \) can work in an accepting mode, where the output neuron is removed. A number \( n \) is introduced in the system, by introducing a sequence \( 10^{n-1} \) in neuron \( \sigma_{\text{out}} \). This number \( n \) is said to be accepted by system \( \Pi \) if the computation eventually halts. The set of numbers accepted by \( \Pi \) is denoted by \( N_{\text{acc}}^{\Pi}(\Pi) \).

We denote the family of all sets of numbers generated or accepted by PSNRS P systems by \( N_{\text{acc}}^{\Pi} \), where the symbol \( \alpha \in \{2, \text{acc}\} \) indicates the generating or accepting mode, \( \alpha \) represents rules on synapses, there are up to \( m \) neurons, and each neuron has up to \( n \) rules on its synapses. As usual, the indices \( m \) and \( n \) are replaced with \( * \) when no bound is imposed on the corresponding parameter.

### 3. Computation Power of PSNRS P Systems

In this section, we mainly investigate the computation power of PSNRS P systems and prove that PSNRS P systems can generate all recursively enumerable sets of numbers.

We first briefly review the definition of register machines. The construction of a register machine is \( M = (m, H, l_0, l_1, I) \), where \( m \) indicates the number of registers, \( H \) indicates the set of instruction labels, \( l_0 \) is the start label, \( l_1 \) is the halt label (assigned to instruction \( \text{HALT} \)), and \( I \) indicates the set of instructions (each of which is precisely labeled by an individual label from \( H \)). Each instruction is one of the following forms: ADD instruction \( l_i \): \( (\text{ADD}(r), l_j, l_k) \) indicates that the register \( r \) is added 1, and then the present instruction labeled with \( l_i \) passes to the next instruction \( l_j \) or \( l_k \) (being chosen nondeterministically); SUB instruction \( l_i \): \( (\text{SUB}(r), l_j, l_k) \) shows that the register \( r \) is subtracted 1 (if the register \( r \) is nonzero), and the present instruction labeled with \( l_i \) passes to the instruction \( l_j \), or else (if the register \( r \) is zero) the present instruction labeled with \( l_i \) passes to the instruction \( l_k \).

It is known that register machines with three registers can precisely generate a family of sets of recursively enumerable natural numbers; in other words, it can characterize NRE [34].

**Theorem 1.** \( N_{\text{acc}}^{\Pi} = N_{\text{acc}}^{\Pi} \).

**Proof.** We prove only the inclusion \( \text{NRE} \subseteq N_{\text{acc}}^{\Pi} \); the reverse inclusion can be invoked from the Church–Turing thesis. For this, a specific PSNRS P system \( \Pi \) is constructed to simulate a register machine \( M \), and the register machine \( M = (m, H, l_0, l_1, I) \) is considered. Each register of \( M \) is associated with a neuron of \( \Pi \); we represent the number \( n \) contained in register \( r \) by \( n \) spikes located in neuron \( \sigma_r \), and the instruction \( l \) of \( H \) corresponds to a neuron \( \sigma_l \). Initially, all neurons are empty; when neuron \( \sigma_r \) is active, the instruction labeled with \( l \) starts. When two spikes are received by neuron \( \sigma_{l_1} \), system \( \Pi \) starts to simulate instruction \( l_i \): \( \text{OP}(r), l_j, l_k \) (\( \text{OP} \) denotes one of the operations ADD and SUB), and either neuron \( \sigma_r \) or \( \sigma_{l_k} \) receives two spikes and a neutral charge, one of which is activated. Then, the system starts to simulate the corresponding instruction. During the simulation of \( M \), when neuron \( \sigma_{l_k} \), which is associated with the halting label \( l_k \) of \( M \), is activated, the computation halts. Without any loss of generality, all registers other than register \( l_1 \) are empty in the halting configuration, and register \( l_1 \) is never decremented during the computation. The time interval between the first two spikes output by the output neuron \( \sigma_{\text{out}} \) is used as the computation result.

The PSNRS P system \( \Pi \) consists of the following three components: ADD, SUB, and FIN modules, shown in Figures 1–3, respectively.

In the following sections, we explain how these modules work.

**ADD module:** simulating an ADD instruction \( l_i \): \( (\text{ADD}(r), l_j, l_k) \).
As shown in Figure 1, suppose that an ADD instruction $I_i$: (ADD $(r, l_j, l_k)$) is simulated in step $t$, and neuron $\sigma_i$ has a neutral charge and receives two spikes.

At step $t$, neuron $\sigma_i$ receives two spikes, rule $0/a^2 \rightarrow a; 0$ on synapses $(l_j, C_1)$ and $(l_k, C_2)$ is applied, and then neuron $\sigma_i$ sends one spike and a neutral charge to auxiliary neurons $\sigma_1$ and $\sigma_2$, respectively. At step $t + 1$, auxiliary neurons $\sigma_1$ and $\sigma_2$ both receive one spike and a neutral charge, the polarity of which remain the same. Rule $0/a \rightarrow a; 0$ is used on synapses $(C_1, r)$ and $(C_2, r)$, and each of the neurons sends a spike to neuron $\sigma_i$. When the two spikes are received, the number of spikes in neuron $\sigma_i$ is increased by two, simulating an increase in the number stored in register $r$ by one. At the same time, neuron $\sigma_3$ receives a spike from each of neurons $\sigma_1$ and $\sigma_2$. Rule $0/a \rightarrow a; 0$ is applied on synapse $(C_2, C_3)$, and neuron $\sigma_3$ sends a spike and a neutral charge to neuron $\sigma_i$. Then, one of the rules $0/a \rightarrow a; +$ and $0/a \rightarrow a; -$ on synapse $(C_3, C_3)$ is nondeterministically chosen and applied, and neuron $\sigma_i$ sends a spike to neuron $\sigma_{c_i}$. There are two possible cases depending on the polarity received by neuron $\sigma_{c_i}$.

**Case 1.** At step $t + 1$, if rule $0/a \rightarrow a; +$ is used on synapse $(C_3, C_3)$, then neuron $\sigma_{c_i}$ receives a spike and positive charge from neuron $\sigma_{c_i}$, and the polarization of the neuron is changed from a neutral charge to a positive charge. At step $t + 2$, neuron $\sigma_{c_i}$ receives a spike to neuron $\sigma_{c_i}$ via rule $+a^2 \rightarrow a; 0$ on synapse $(C_3, C_3)$, and a spike is maintained in neuron $\sigma_{c_i}$. At the same time, rule $+a^2 \rightarrow a; +$ is applied on synapse $(C_3, C_3)$, and neuron $\sigma_{c_i}$ receives a spike and a positive charge. In this way, neuron $\sigma_{c_i}$ accumulates a spike and changes to a neutral charge. At step $t + 3$, neuron $\sigma_i$ receives two spikes from neurons $\sigma_{c_i}$ and $\sigma_{c_i}$, which both have a neutral charge. Meanwhile, by means of rule $-a \rightarrow \lambda; -$, neuron $\sigma_{c_i}$ sends a negative charge to neurons $\sigma_{c_i}$ and $\sigma_{c_i}$, so the polarizations of neurons $\sigma_{c_i}$ and $\sigma_{c_i}$ are changed back to their original state. At the same step, rule is used via synapse $(C_3, l_j)$, and neuron $\sigma_{c_i}$ sends a spike to neuron $\sigma_{c_i}$. In this way, two spikes are present in neuron $\sigma_{c_i}$, and system II starts to simulate instruction $I_j$ of $M$. 

**Figure 1: ADD module (simulating $I_i$: (ADD $(r, l_j, l_k)$)).**

**Figure 2: SUB module (simulating $I_j$: (SUB $(r, l_j, l_k)$)).**

**Figure 3: FIN module (ending the computation).**
Case II. At step $t + 1$, if rule $0/a → a$: can be enabled on synapse $(C_1, C_3)$, a spike and a negative charge are sent to neuron $σ_c$. At step $t + 2$, neuron $σ_c$ receives a spike via synapse $(C_2, C_3)$ via rule $−a/0 → a:0$. At the same step, neuron $σ_c$ sends a spike and a negative charge to neuron $σ_r$ along synapse $(C_3, C_2)$ by rule $−a/2 → a:−$; afterwards, neuron $σ_c$ has a neutral charge. At step $t + 3$, rule $+a/− → λ:+$ is applied on synapse $(C_3, C_3)$, and neuron $σ_r$ sends a positive charge and receives the return state. Similarly, neuron $σ_r$ executes the same rule for neuron $σ_c$ via synapse $(C_3, C_2)$. Otherwise, neuron $σ_r$ receives two spikes from neurons $σ_c$ and $σ_c$ by rules $0/a → a:0$ and $+a/− → a:0$ via synapses $(C_3, C_1)$ and $(C_2, C_1)$. In this way, the system II starts to simulate instruction $l_i$ of $M$.

Therefore, the ADD module can correctly simulate ADD instructions: in neuron $σ_r$, the number of spikes is increased by two; meanwhile, one of two neurons $σ_l$ and $σ_h$ nondeterministically receives two spikes.

**SUB module**: simulating a SUB instruction $l_i$: $(SUB(r), l_i, l_k)$.

In this section, we will describe the SUB module, as shown in Figure 2. Suppose that a SUB instruction $l_i$: $(SUB(r), l_i, l_k)$ is simulated and neuron $σ_r$ receives two spikes at step $t$. Initially, neuron $σ_l$ fires, sending spikes to neuron $σ_c$, and neuron $σ_r$ using rule $0/a^2 → a:+$ on synapses $(l_i, C_3)$ and $(l_i, r)$. However, neuron $σ_r$ maintains a positive charge, and neuron $σ_l$ is changed to a positive charge. At the same step, rule $0/a^2 → a:−$ is applied on synapse $(l_i, C_3)$, and neuron $σ_r$ receives a spike from neuron $σ_l$. According to the number of spikes in neuron $σ_r$, the following two cases are considered.

**Case I.** At step $t + 1$, neuron $σ_r$ has $2n + 1(n ≥ 0)$ spikes (corresponding to the number stored in register $r$, being $n$). In this way, neuron $σ_r$ has a positive charge, rule $+a/λ → λ:+$ is applied on synapse $(r, C_3)$, and neuron $σ_c$, which has a positive charge, sends a spike and a negative charge to neuron $σ_c$. Note that neuron $σ_c$ maintains a neutral charge when a positive charge meets a negative charge, resulting in a spike in neuron $σ_c$. Simultaneously, neuron $σ_l$ fires, sending a spike to neuron $σ_c$ via rule $+a/λ → a:+$ on synapse $(l_i, C_3)$. At the same step, neuron $σ_c$ sends a negative charge to neuron $σ_l$, and the initial state of neuron $σ_l$ is recovered to avoid inaccurate operation. At step $t + 2$, neuron $σ_c$ is activated by rule $+a/a → a:0$ on synapse $(C_3, l_i)$, sending a spike to neuron $σ_i$; meanwhile, neuron $σ_r$ sends a spike to neuron $σ_l$ via rule $0/a → a:0$ on synapse $(C_3, l_i)$. Neuron $σ_r$ receives two spikes, which indicates that system II simulates the instruction $l_i$ of $M$.

**Case II.** At step $t + 1$, neuron $σ_r$ has a spike (corresponding to the number stored in register $r$ being $0$). Then, a negative charge is sent to neuron $σ_l$ via rule $−a/λ → λ:−$ on synapse $(C_1, r)$, and neuron $σ_l$ returns to the initial state when a positive charge meets a negative charge. At the same step, neuron $σ_c$ is activated by rule $+a/a → a:−$ on synapse $(C_2, C_3)$, sending a spike and a negative charge to neuron $σ_c$. At step $t + 2$, rule $−a/a → a:−$ is enabled on synapse $(C_3, C_3)$, and neuron $σ_c$ sends a spike and a negative charge to neuron $σ_c$. At step $t + 3$, neuron $σ_c$ fires, sending a spike to neurons $σ_l$ and $σ_l$ by rules $−a/a → a:−$ and $−a/a → a:+$ on synapses $(C_3, r)$ and $(C_3, C_3)$. Then, there are two spikes in neuron $σ_r$ with a neutral charge and a spike in neuron $σ_c$. At step $t + 4$, rule $−a/2 → a:−$ is applied via synapse $(r, C_3)$, and a spike is sent to neuron $σ_r$ from neuron $σ_l$. Simultaneously, neuron $σ_r$ receives a spike from neuron $σ_l$ by rule $+a/a → a:0$ on synapse $(C_3, C_3)$. Meanwhile, neuron $σ_r$ sends a positive charge to neurons $σ_l$ and $σ_l$, restoring their initial states. At step $t + 5$, neuron $σ_r$ receives two spikes from neurons $σ_c$ and $σ_c$ via rule $−a/a → a:0$ on synapses $(C_3, l_i)$ and $(C_3, l_i)$. In this way, system II simulates the instruction $l_i$.

The simulation of the SUB instruction $l_i$: $(SUB(r), l_i, l_k)$ is correct: system II starts with neuron $σ_l$ having two spikes inside and sends with sending two spikes and a neutral charge to neuron $σ_l$ (if the number located in register $r$ is greater than $0$, the register $r$ is decreased by one) or sending two spikes and a neutral charge to neuron $σ_l$ (if the number located in register $r$ is $0$).

Obviously, there is no interference between the ADD and SUB modules, but interferences exist between two SUB modules. If there are two SUB instructions $l_i$ acting on register $r$, neurons $σ_c$ and $σ_c$ associated with register $r$ send synapses to neurons $σ_c$ and $σ_c$, respectively. In the SUB module associated with $l_i$ ($l_i ≠ l_k$), when we simulate a SUB instruction $l_i$: $(SUB(r), l_i, l_k)$, all neurons except neurons $σ_c$ and $σ_c$ receive no spikes and charges.

It is important to note that the synapses and their rules associated with neurons $σ_c$ and $σ_c$ are not shown in Figure 2; for example, neurons $σ_c$ and $σ_c$ exist between any two subtraction modules, and the rule $+a/λ → λ:0$ is present on the synapse of such two neurons, respectively. Neurons $σ_c$ and $σ_c$ only consume spikes and restore neutral charge, not affecting other neurons’ states. Moreover, the synapses of neurons $σ_c$ and $σ_c$ may be connected to any neuron in the environment or neurons related to SUB instruction $l_i$; that is to say, the synaptic connections between neuron $σ_c$ (or $σ_c$) and other neurons cannot be described in Figure 2.

When $n > 0$ spikes are present in neuron $r$, neuron $σ_c$ sends a spike and a neutral charge to neuron $σ_c$; therefore, neuron $σ_c$ fires, rule $+a/λ → λ:0$ (not shown in Figure 2) is enabled, then one spike $a$ is forgotten, and neuron $σ_c$ returns to the initial state. If no spike exists in neuron $r$, neuron $σ_c$ receives a spike and a neutral charge from neuron $σ_c$, rule $+a/λ → λ:0$ is enabled, and one spike $a$ is forgotten. Next, neurons $σ_c$ and $σ_c$ return to their initial state with respect to the initial number of spikes. Consequently, there is no interference between the SUB modules.

**FIN module**: outputting the result of the computation.

As shown in Figure 3, the FIN module is constructed. Assume that the computation halts; in other words, the halt instruction $l_k$ is reached and the result of the computation is stored in register $r$ (register $r$ contains $n$ spikes). Neuron $σ_l$ receives two spikes and a neutral charge at step $t$, rule $0/a^2 → a:0$ on synapse $(l_k, C_3)$ is activated, and neuron $σ_l$ sends a spike and a neutral charge to neuron $σ_l$. At that...
moment, neuron $\sigma_1$ fires, sending a positive charge to neuron $\sigma_2$ via rule $0/a^2 \rightarrow \lambda; +$ on synapse $(l_0, 1)$. Meanwhile, neuron $\sigma_3$ receives a spike and a positive charge from neuron $\sigma_1$ by rule $0/a^2 \rightarrow a; +$ via synapse $(l_0, C_1)$. At step $t + 1$, neuron $\sigma_2$ sends a spike and a neutral charge to neuron $\sigma_3$ via synapse $(C_2, C_3)$ by rule $0/a \rightarrow a; 0$. Simultaneously, neuron $\sigma_1$ sends a spike and a positive charge to neurons $\sigma_2$ and $\sigma_3$ via rule $+/a^2 \rightarrow a; +$. Meanwhile, rule $+/a \rightarrow a; −$ on synapse $(C_1, C_4)$ is enabled, and neuron $\sigma_2$ receives a spike and a negative charge from neuron $\sigma_1$.

At that moment, a positive charge and a negative charge meet in neuron $\sigma_1$, which therefore has a neutral charge and two spikes. At step $t + 2$, rule $0/a \rightarrow a; 0$ on synapse $(C_3, \text{out})$ is applied, and a spike is sent from neuron $\sigma_4$. Meanwhile, neuron $\sigma_5$ fires, sending no spike and a neutral charge to neuron $\sigma_6$ via rule $0/a^2 \rightarrow \lambda; 0$ on synapse $(C_4, C_5)$. At step $t + 3$, rule $0/a \rightarrow a; 0$ is applied, and neuron $\sigma_6$ sends the first spike to the environment. At the same time, neuron $\sigma_6$ receives two spikes from neurons $\sigma_1$ and $\sigma_5$.

From step $t + 3$ to step $t + n + 1$, the spike of neuron $\sigma_1$ is exhausted by rule $0/a^2 \rightarrow \lambda; 0$ on synapse $(C_4, C_5)$. At step $t + n + 1$, neuron $\sigma_4$ receives a spike and a negative charge from neuron $\sigma_5$. Then, neuron $\sigma_7$, which now has a negative charge, sends a spike and a neutral charge to neurons $\sigma_8$ and $\sigma_9$ by rule $−/a \rightarrow a; 0$ on synapses $(C_7, \text{out})$ and $(C_8, C_9)$ at step $t + n + 2$. At step $t + n + 3$, neuron $\sigma_4$ fires, sending a negative charge via synapses $(C_7, 1)$ and $(C_8, C_9)$ and restoring the initial state of charge. Meanwhile, neuron $\sigma_4$ sends the second spike to the environment by rule $0/a \rightarrow a; 0$. Hence, the interval at which two spikes are sent to the environment by the system $\Pi$ is $(t + n + 3) − (t + 3) = n$, where $n$ is exactly the number stored in register $1$, i.e., corresponding to the result computed by system. Therefore, the register machine $M$ is correctly simulated by the system $\Pi$, $N(M) = N_2(\Pi)$.

**Theorem 2.** $N_{PSNRS}^{\text{acc}} \Pi = N_{RE}$. Proof. A PSNRS P system $\Pi$, working in the accepting mode, is constructed to simulate a deterministic register machine $M = (m, H, l_0, l_1, 1)$. The system $\Pi$ contains an INPUT module, a deterministic ADD module, and a SUB module. The INPUT module is shown in Figure 4. Spike train $10^{n+1}$ is introduced into $\Pi$ by means of neuron $\sigma_{in}$. In this system, the time interval of the first two spikes introduced by the INPUT module is used as the computing result.

At step $t$, we suppose that neuron $\sigma_{in}$ receives the first spike from the environment. Neuron $\sigma_{in}$ fires, sending a spike and neutral charge to neuron $\sigma_1$ via rule $0/a \rightarrow a; 0$ on synapse $(in, in_1)$. At the same time, neuron $\sigma_{in}$ sends a spike and $−$ is applied on synapses $(in, in_2)$ and $(in, in_3)$. A spike is sent to neurons $\sigma_2$ and $\sigma_3$, and their polarity is changed to a negative charge. Similarly, neurons $\sigma_{in}$ and $\sigma_{in}$ receive one spike and a neutral charge from neuron $\sigma_{in}$ via rules $0/a \rightarrow a; 0$ (corresponding to synapses $(in, in_1)$ and $(in, in_2)$). At step $t + 1$, neurons $\sigma_{in}$ and $\sigma_{in}$ receive a spike and neutral charge from neuron $\sigma_{in}$, respectively. Meanwhile, neuron $\sigma_{in}$, fires, rule $+/a^2 \rightarrow a; 0$ is applied on synapses $(in_2, in_3)$ and $(in_1, 1)$, and neurons $\sigma_{in}$ and $\sigma_1$ receive a spike and a neutral charge from neuron $\sigma_{in}$, respectively. Similarly, neurons $\sigma_{in}$ and $\sigma_1$ receive a spike and a neutral charge by rule $−/a \rightarrow a; 0$ on synapses $(in_2, in_3)$ and $(in_1, 1)$. At step $t + 2$ on, neurons $\sigma_{in}$ and $\sigma_{in}$ exchange one spike with each other, and neuron $\sigma_1$ receives two spikes in each step. In this case, at step $t + n + 1$, neuron $\sigma_{in}$ receives the second spike from the environment. Then, neurons $\sigma_{in}$, $\sigma_{in}$, $\sigma_{in}$, and $\sigma_{in}$ receive the second spike and accumulate two spikes. Note that neuron $\sigma_1$ still receives spikes at step $t + n$, and there are two spikes in neuron $\sigma_1$, which represents the number stored in register $1$ of $M$.

At the same step, neurons $\sigma_{in}$ and $\sigma_{in}$ send a positive charge to neurons $\sigma_{in}$ and $\sigma_{in}$, respectively, restoring their original states of charge. Meanwhile, neurons $\sigma_{in}$ and $\sigma_{in}$ have spikes according to rule $0/a \rightarrow a; 0$ on synapses $(in_2, in_3)$ and $(in_1, in_3)$. At step $t + n + 1$, the spikes in neurons $\sigma_{in}$ and $\sigma_{in}$ are depleted by rule $0/a^2 \rightarrow \lambda; 0$ on synapses $(in_1, 1)$ and $(in_1, 1)$.

At the same step, neuron $\sigma_1$ receives two spikes and a neutral charge from neurons $\sigma_{in}$ and $\sigma_{in}$, by rule $0/a^2 \rightarrow a; 0$. In this way, neuron $\sigma_1$ receives two spikes and the system simulates the initial instruction $l_0$ of $M$.

For a deterministic ADD instruction of the form $l_r$: (ADD $(r, l_i)$), the corresponding ADD module shown in Figure 5 is simpler than that shown in Figure 1. Hence, we do not consider the details here.

In system $\Pi$, the SUB module remains unchanged as shown in Figure 2, and neuron $\sigma_{in}$ remains in the system; however, the FIN module is removed. There is no rule in neuron $\sigma_{in}$. When neuron $\sigma_1$ receives two neurons and no rules are available, the computation stops. The computing result introduced is $(t + n + 1) − (t + 1) = n$, which means that the number accepted by system $\Pi$ is $n$. The operation process of INPUT module is shown in Table 1.

According to the above description, the register machine $M$ working in accepting mode can be correctly simulated by PSNRS P systems. Hence, the Theorem holds.
4. A Small Universal PSNR P System

In this section, a small universal PSNR P system of computing device is constructed. Generally, a register machine $M$ is used to compute a Turing computable function $f: \mathbb{N}^k \rightarrow \mathbb{N}$ in the following way: arguments $n_1, n_2, \ldots, n_k$ are introduced by the specified registers $r_1, r_2, \ldots, r_k$ (representing the first $k$ registers). We begin with the first instruction with label $l_0$ and stop with the halt instruction with label $l_h$ (if we stop), and then the value of the function is stored in a specific register $r_i$; beyond that, all other registers are empty. For further information about universal register machines for computable functions, readers can refer to [34].

In the following proof of the universal result, we use a specific universal register machine mentioned in [34], as shown in Figure 6. The universal register machine is of the construct $M_u = (8, H, l_0, l_h, l_r)$, where there are 8 registers, numbered from 0 to 7, and 23 instructions; the last instruction is the halting one. As defined in [34], the input numbers are introduced in registers 1 and 2, and the result is stored in register 0 when the machine $M_u$ halts.

According to the previous description, subtraction instructions are not allowed on the registers where the results are stored, but register 0 of $M_u$ is subject to SUB instructions. Therefore, register machine $M_u$ is modified into $M_u'$: a register with label 8 is added, and the halting instruction $l_h$ of $M_u$ is replaced by the following instructions:

$$
\begin{align*}
l_h : & (\text{SUB}(0), l_{22}, l_h'), \\
l_{22} : & (\text{ADD}(8), l_h), \\
l_h' : & \text{HALT}.
\end{align*}
$$

In this way, the universal register machine $M_u'$ has 9 registers, 24 ADD and SUB instructions, and 25 labels. The result of the computation is stored in register 8, which is never decremented during the computation. Furthermore, the register machine $M_u'$ can be considered deterministic, and, without losing Turing completeness, the ADD instructions $l_i : (\text{ADD}(r), l_j, l_k)$ having $l_j = l_k$ is denoted by the form $l_i : (\text{ADD}(r); l_j)$.

![Figure 5: ADD module of $\Pi'$.](image)

![Figure 6: The universal register machine $M_u$.](image)

**Table 1: Simulation for the INPUT module.**

| Step | Neurons active | Rules executed | Synapses |
|------|----------------|----------------|----------|
| $t$  | in,0,a         | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |
|      |                 | 0/a → a;0      | (in,in)  |

**Note:** The table illustrates the simulation of the INPUT module, where $t$ represents the current step, and the columns describe the active neurons, the rules executed, and the synapses involved, respectively.
Theorem 3. There is a universal PSNRS P system with 151 neurons for computable functions.

Proof. A PSNRS P system Π’ is constructed to simulate the universal register machine $M'_u$, as shown in Figure 7. The system Π’ consists of seven modules: ADD, ADD-ADD, SUB, ADD-SUB, SUB-ADD, INPUT, and OUTPUT. The ADD module (resp., SUB module) is applied to simulate the ADD instruction (resp., SUB instruction) of $M'_u$; in a similar way, each module is applied to simulate its corresponding instruction. However, the INPUT module is used to introduce a spike train from the environment, and the OUTPUT module is used to output the computation result.

In system Π’, each register $r$ corresponds to a neuron $\sigma_r$, and the number saved in register $r$ is encoded by the number of spikes stored in neuron $\sigma_r$. Specifically, register $r$ having the number $n$ ($n \geq 0$) is equivalent to neuron $\sigma_r$ containing $2n$ spikes. Moreover, a neuron $\sigma_i$ in system Π’ is associated with each instruction $l_i$ in $M'_u$. When neuron $\sigma_r$ holds two spikes, the rules on synapses are enabled, which means system Π’ simulates the instruction $l_i$. Until two spikes and a neutral charge are received by neuron $\sigma_r$, the computation in $M'_u$ is simulated by system Π’. The number of spikes emitted from system Π’ into the environment is exactly the result computed by $M'_u$.

All modules are presented in graphical form, indicating the neurons and synapses with the associated sets of rules. In the initial configuration, there is no spike in each neuron.

The INPUT module, shown in Figure 8, introduces $2g(x)$ and $2y$ spikes into neurons $\sigma_1$ and $\sigma_2$ by reading the spike train $10^{g(x)-3}10^{-2}$, respectively. The module works as follows.

Initially, neuron $\sigma_{in}$ receives one spike from the environment. Neuron $\sigma_{in}$ fires, rule $0/a \rightarrow a: 0$ is applied, and a spike and a neutral charge are sent to neurons $\sigma_{c_1}, \sigma_{c_2}, \sigma_{c_3}, \sigma_{c_4}, \sigma_{c_5}, \sigma_{c_6}$. Afterwards, neuron $\sigma_{c_1}$ fires, sending a spike and a negative charge to neurons $\sigma_{c_2}$ and $\sigma_{c_3}$ by using rules $0/a \rightarrow a: -$ via synapses $(C_3, C_5)$ and $(C_4, C_6)$. The neuron $\sigma_{c_1}$ holds a spike, and no rule is enabled. Then, neurons $\sigma_{c_2}$ and $\sigma_{c_3}$ have neutral charge, and the rules $0/a \rightarrow a: 0$ on synapses $(C_4, C_5)$ and $(C_6, C_7)$ can be enabled. From that moment on, neurons $\sigma_{c_2}$ and $\sigma_{c_3}$ exchange a spike and a neutral charge with each other until the neuron $\sigma_{c_1}$ receives the second spikes. After $g(x)-2$ step, neuron $\sigma_{c_1}$ receives second spike. One step later, the neuron $\sigma_{c_1}$ receives a spike and a neutral charge. Subsequently, rules $+/a^2 \rightarrow \lambda: -$ on synapses $(C_4, C_5)$ and $(C_6, C_7)$ are applied, and neurons $\sigma_{c_2}$ and $\sigma_{c_3}$ are changed to positive charge. Rules $+/a^2 \rightarrow \lambda: 0$ can be enabled, removing two spikes in each of the neurons $\sigma_{c_2}$ and $\sigma_{c_3}$. At that moment, all neurons associated with neuron $\sigma_1$ can be used. In this way, $2g(x)$ spikes are introduced in neuron $\sigma_1$.

When the second spike arrives in neurons $\sigma_1$ and $\sigma_3$, rules $+/a^2 \rightarrow a: -$ on synapses $(C_4, C_5)$ and $(C_6, C_7)$ are applied, and then each one receives one spike and one negative charge; hence, they become neutral and contain one spike. From the next moment on, rules $0/a \rightarrow a: 0$ are used, and neurons $\sigma_{c_2}$ and $\sigma_{c_3}$ emit a spike and a neutral charge to each other, in each step, until the third spike arrives in neurons $\sigma_{c_1}$. After $g(x)$ step, neuron $\sigma_{c_1}$ gets the third spike, and rules $+/a^2 \rightarrow \lambda: -$ on synapses $(C_7, C_8)$ and $(C_7, C_9)$ can be applied. The neurons $\sigma_{c_2}$ and $\sigma_{c_3}$ have negative charge, and no rules are applied. At the same time, rules $+/a^2 \rightarrow \lambda: +$ via synapses $(C_4, C_9)$, $(C_5, C_8)$, and $(C_6, C_7)$ are applied; neurons $\sigma_{c_2}$, $\sigma_{c_3}$, and $\sigma_{c_4}$ still keep positive charge; and the extra spikes will be consumed by rules $+/a^2 \rightarrow \lambda: +$ on synapse $(C_4, C_9)$ and $+/a^2 \rightarrow \lambda: 0$ via synapses $(C_7, C_8)$, $(C_6, C_7)$. In this way, $2y$ spikes have been loaded in neuron $\sigma_2$. With a third spike into neurons $\sigma_1$ and $\sigma_3$, this two neurons fire, rules $0/a^3 \rightarrow a: 0$ on synapses $(C_1, l_0)$ and $(C_2, l_0)$ can be enabled, the neuron $l_0$ receives two spikes and a neutral charge, and the system starts to simulate the initial instruction $l_0$ of $M'_u$.

For ADD and SUB modules, we will follow the ADD module in accepting mode as shown in Figure 5 and the SUB module in generating mode as shown in Figure 2.

When neuron $\sigma_{c_1}$ receives two spikes, that is, the instruction $l_0$ is reached, the result of computation is store in register 8. The tasks of outputting the result is carried out by the OUTPUT module shown in Figure 9.
Assume that, at step $t$, the neuron $\sigma'_c$ gets two spikes, rule $0/a^2 \rightarrow a; 0$ on synapse $(l'_0, 8)$ is used, and neuron $\sigma_c$ receives a spike and a neutral charge. Then, there are $2n + 1$ spikes in neuron $\sigma_c$, it fires, using rules $0/a^3 \rightarrow a; 0$ on synapses $(8, \text{out})$ and $(8, C_1)$, and a spike and one neutral charge are sent to neurons $\sigma_{\text{out}}$ and $\sigma_c$. Then, neuron $\sigma_c$ sends a spike and neutral charge to neurons $\sigma_g$ and $\sigma_{\text{out}}$, so neuron $\sigma_{\text{out}}$ emits a spike and neutral charge out by rule $0/a^2 \rightarrow a; 0$, until $n$ spikes are sent out. Note that neuron $\sigma_g$ and neuron $\sigma_c$ exchange a spike and neutral charge with each other, ensuring that neuron $\sigma_{\text{out}}$ can emit all the results of computation for system $M_u'$.

Therefore, according to the above INPUT module, deterministic ADD module, SUB module, and OUTPUT module, we have used the following:

(i) 9 neurons for 9 registers
(ii) 25 neurons for 25 labels
(iii) $8 \times 14$ neurons for 14 SUB instructions
(iv) $2 \times 10$ neurons for 10 ADD instructions
(v) 10 neurons in the OUTPUT module
(vi) 2 neurons in the OUTPUT module

All these come to a total of 178 neurons.

This number can be slightly decreased by some code optimization, exploring some particularities of the register machine $M_u'$.

For instance, the sequence of ADD instructions

$$l_{17}: (\text{ADD}(2), l_2),$$
$$l_{21}: (\text{ADD}(3), l_{18})$$

(3)

without any other instruction addressing the label $l_{21}$, can be simulated by the module shown in Figure 10. Then, three neurons associated with label $l_{21}$ can be saved.

There are also two pairs of ADD-SUB instructions:

$$l_5: (\text{ADD}(5), l_6),$$
$$l_6: (\text{SUB}(7), l_7, l_8),$$
$$l_9: (\text{ADD}(6), l_{10}),$$
$$l_{10}: (\text{SUB}(4), l_9, l_{11}).$$

(4)

Each sequence of ADD-SUB instructions,

$$l_i: (\text{ADD}(r'), l_g),$$
$$l_{g'}: (\text{SUB}(r'), l_j, l_k),$$

(5)

can be simulated by the ADD-SUB module shown in Figure 11.

In this way, we save the 6 neurons associated with labels $l_6$ and $l_{10}$.

A similar operation is possible for the following six sequences of SUB-ADD instructions:

$$l_6: (\text{SUB}(1), l_1, l_2),$$
$$l_1: (\text{ADD}(7), l_6),$$
$$l_5: (\text{SUB}(6), l_5, l_3),$$
$$l_3: (\text{ADD}(5), l_6),$$
$$l_8: (\text{ADD}(6), l_9),$$
$$l_9: (\text{SUB}(5), l_{10}, l_{16})$$

(6)

$$l_{10}: (\text{ADD}(4), l_{11}),$$
$$l_{11}: (\text{SUB}(1), l_{22}, l_{25}),$$
$$l_{22}: (\text{ADD}(8), l_{18}).$$
Each sequence of ADD-SUB instructions, 

$$l_g: (\text{SUB}(r^g), l_1, l_k),$$

$$l_i: (\text{ADD}(r^i), l_g),$$

can be simulated by the SUB-ADD module given in Figure 12. In this way, we save 18 neurons associated with labels $l_1, l_5, l_7, l_9, l_{16}, l_{22}$.

Therefore, by using the ADD-ADD module, ADD-SUB module, and SUB-ADD module, we can totally save 27 neurons ($3(\text{ADD-ADD}) + 6(\text{ADD-SUB}) + 18(\text{SUB-ADD})$). Then, the number of neurons can be decreased from 178 to 151.

5. Conclusions and Remarks

A variant of SN P systems, called SN P systems with polarizations and rules on synapses (PSNRS P systems), is proposed. We prove that as number generating devices and accepting devices, SN P systems with polarizations and rules on synapses are Turing universal. Moreover, a small universal system with 151 neurons as computing function device is given. Compared with the small universal SN P systems with polarizations proposed in [47], by moving rules to synapses, 13 neurons were reduced.

In the proof of Theorems 1 and 2, only standard spiking rules are used. It is interesting to use extended rules to construct universal systems with fewer neurons. In this work, PSNRS P systems are used as number generating or accepting devices. It is of interest to investigate the computation power of PSNRS P systems as language generators or to control language generators.

In general, some open problems about PSNRS P systems may be considered based on the results obtained in this work; for instance, it remains open whether the results about the universality of PSNRS P systems still hold with fewer neurons. The PSNRS P systems proved to be universal when using both spiking rules and forgetting rules; it is challenging to investigate whether PSNRS P systems are still universal when using only one type of rules. In this work, the systems work in the synchronous mode. It is of interest to study the...
computation power of PSNRS P systems working in asynchronous mode [51] or local synchronous mode [52].

Data Availability
No data were used to support this study.

Conflicts of Interest
The authors declare that they have no conflicts of interest.

Acknowledgments
The work of S. Jiang was supported by the National Natural Science Foundation of China (61902360 and 61772214) and the Foundation of Young Key Teachers from University of Henan Province (2019GGJS131). The work of Y. Wang was supported by the National Key R&D Program of China for International S&T Cooperation Projects (2017YFE0103900), the Joint Funds of the National Natural Science Foundation of China (U1804262), and the State Key Program of National Natural Science Foundation of China (61632002). The work of F. Xu was supported by the National Natural Science Foundation of China (61502186), China Postdoctoral Science Foundation (2016M592335), and the Fundamental Research Funds for the Central Universities (HUST: 2019kyfYXMBZ056).

References
[1] G. Păun, "Computing with membranes," Journal of Computer and System Sciences, vol. 61, no. 1, pp. 108–143, 2000.
[2] A. Leporati, L. Manzoni, G. Mauri, A. E. Porreca, and C. Zandron, "Monodirectional P systems," Natural Computing, vol. 15, no. 4, pp. 551–564, 2016.
[3] G. Zhang, M. J. Pérez-Jiménez, and M. Gheorghe, Real-Life Applications with Membrane Computing. Springer-Verlag, Berlin, Germany, 2017.
[4] C. Martín-Vide, G. Păun, J. Pazos, and A. Rodríguez-Patón, "Tissue P systems," Theoretical Computer Science, vol. 296, no. 2, pp. 295–326, 2003.
[5] M. Ionescu, G. Păun, and T. Yokomori, "Spiking neural P systems," Fundamenta Informaticae, vol. 71, no. 2-3, pp. 279–308, 2006.
[6] X. Zhang, L. Pan, and A. Paun, "On the Universality of Axon P systems," IEEE Transactions on Neural Networks and Learning Systems, vol. 26, no. 11, pp. 2816–2829, 2015.
[7] S. Jiang, Y. Wang, J. Xu, and F. Xu, "The computational power of cell-like P systems with Sympor/Antiport rules and promoters," Fundamenta Informaticae, vol. 164, no. 2-3, pp. 207–225, 2019.
[8] G. Ciobanu and A. Resios, "Computational complexity of simple P systems," Fundamenta Informaticae, vol. 87, no. 1, pp. 49–59, 2008.
[9] G. Păun and R. Păun, "Membrane computing and economics: numerical P systems," Fundamenta Informaticae, vol. 73, no. 1-2, pp. 213–227, 2006.
[10] A. Leporati, A. E. Porreca, C. Zandron, and G. Mauri, "Improved Universality results for parallel enzymatic numerical P systems," International Journal of Unconventional Computing, vol. 9, no. 5-6, pp. 385–404, 2013.
[11] G. Zhang, M. Gheorghe, and C. Wu, "A quantum-inspired evolutionary algorithm based on P systems for Knapsack problem," Fundamenta Informaticae, vol. 87, no. 1, pp. 93–116, 2008.
[12] Y. Rogozhin, A. Alhazov, L. Burtseva, S. Cojocaru, A. Colesnicov, and L. Malahov, "Solving problems in various domains by hybrid models of high performance computations," Computer Science Journal of Moldova, vol. 22, no. 1, pp. 3–20, 2014.
[13] A. Leporati, L. Manzoni, G. Mauri, A. E. Porreca, and C. Zandron, "Characterizing PSPACE with shallow non-confluent P systems," Journal of Membrane Computing, vol. 1, no. 2, pp. 75–84, 2019.
[14] R. A. B. Juayong and H. N. Adorna, "On simulating cooperative transition P systems in evolution-communication P systems with energy," Natural Computing, vol. 17, no. 2, pp. 333–343, 2018.
[15] K. Chen, J. Wang, Z. Sun, J. Luo, and T. Liu, "Programmable logic controller stage programming Using spiking neural P systems," Journal of Computational and Theoretical Nanoscience, vol. 12, no. 7, pp. 1292–1299, 2015.
[16] G. Păun, The Oxford Handbook of Membrane Computing. Oxford University Press, New York, NY, USA, 2010.
[17] M. Minsky, Computation: Finite and Infinite Machines, Prentice-Hall, Englewood Cliffs, NJ, USA, 1967.
[18] F. G. C. Cabarle, H. N. Adorna, M. Jiang, and X. Zeng, "Spiking neural P systems with scheduled synapses," IEEE Transactions on Nanobioscience, vol. 16, no. 8, pp. 792–801, 2017.
[19] F. G. C. Cabarle, H. N. Adorna, M. J. Pérez-Jiménez, and T. Song, "Spiking neural P systems with structural plasticity," Neural Computing and Applications, vol. 26, no. 8, pp. 1905–1917, 2015.
[20] F. G. C. Cabarle, H. N. Adorna, and M. J. Pérez-Jiménez, "Sequential spiking neural P systems with structural plasticity based on max/min spike number," Neural Computing and Applications, vol. 27, no. 5, pp. 1337–1347, 2016.
[21] H. Peng, J. Wang, M. J. Pérez-Jiménez, and A. Riscos-Núñez, "Dynamic threshold neural P systems," Knowledge-Based Systems, vol. 163, pp. 875–884, 2019.
[22] H. Peng and J. Wang, "Coupled neural P systems," IEEE Transactions on Neural Networks and Learning Systems, vol. 30, no. 6, pp. 1672–1682, 2019.
[23] H. Peng, J. Yang, J. Wang et al., "Spiking neural P systems with multiple channels," Neural Networks, vol. 95, pp. 66–71, 2017.
[24] T. Song, F. Gong, X. Liu, Y. Zhao, and X. Zhang, "Spiking neural P systems with white hole neurons," IEEE Transactions on Nanobioscience, vol. 15, no. 7, pp. 666–673, 2016.
[25] T. Song and L. Pan, "Spiking neural P systems with request rules," Neurocomputing, vol. 193, pp. 193–200, 2016.
[26] H. Peng, B. Li, J. Wang et al., "Spiking neural P systems with inhibitory rules," Knowledge-Based Systems, vol. 188, Article ID 105064, pp. 1–10, 2020.
[27] L. Pan, G. Păun, and G. Zhang, "Spiking neural P systems with communication on request," International Journal of Neural Systems, vol. 2, pp. 168–179, 2016.
[28] H. Chen, R. Freund, M. Ionescu, G. Păun, and M. J. Pérez-Jiménez, "On string languages generated by spiking neural P systems," Fundamenta Informaticae, vol. 75, no. 1–4, pp. 141–162, 2007.
[29] X. Zeng, L. Xu, X. Liu, and L. Pan, "On languages generated by spiking neural P systems with weights," Information Sciences, vol. 278, pp. 423–433, 2014.
[30] T. Wu, Z. Zhang, and L. Pan, "On languages generated by cell-like spiking neural P systems," IEEE Transactions on Nanobioscience, vol. 15, no. 5, pp. 455–467, 2016.
[31] R. T. A. de la Cruz, F. G. Cabarle, and H. N. Adorna, “Generating context-free languages using spiking neural P systems with structural plasticity,” *Journal of Membrane Computing*, vol. 1, no. 3, pp. 161–177, 2019.

[32] X. Zeng, X. Zhang, T. Song, and L. Pan, “Spiking neural P systems with thresholds,” *Neural Computation*, vol. 26, no. 7, pp. 1340–1361, 2014.

[33] X. Song, J. Wang, H. Peng et al., “Spiking neural P systems with multiple channels and anti-spikes,” *Biosystems*, vol. 169-170, pp. 13–19, 2018.

[34] I. Korec, “Small universal register machines,” *Theoretical Computer Science*, vol. 168, no. 2, pp. 267–301, 1996.

[35] Y. Rogozhin, “Small universal turing machines,” *Theoretical Computer Science*, vol. 168, no. 2, pp. 215–240, 1996.

[36] T. Song, P. Zheng, M. L. Dennis Wong, and X. Wang, “Design of logic gates using spiking neural P systems with homogeneous neurons and astrocytes-like control,” *Information Sciences*, vol. 372, pp. 380–391, 2016.

[37] D. Díaz-Pernil, F. Peña-Cantillana, and M. A. Gutiérrez-Naranjo, “A parallel algorithm for skeletonizing images by using spiking neural P systems,” *Neurocomputing*, vol. 115, pp. 81–91, 2013.

[38] H. Peng, J. Wang, M. J. Pérez-Jiménez, H. Wang, J. Shao, and T. Wang, “Fuzzy reasoning spiking neural P system for fault diagnosis,” *Information Sciences*, vol. 235, pp. 106–116, 2013.

[39] T. Wang, G. Zhang, J. Zhao, Z. He, J. Wang, and M. J. Pérez-Jiménez, “Fault diagnosis of electric power systems based on fuzzy reasoning spiking neural P systems,” *IEEE Transactions on Power Systems*, vol. 30, no. 3, pp. 1182–1194, 2015.

[40] H. Rong, K. Yi, G. Zhang, J. Dong, P. Paul, and Z. Huang, “Automatic implementation of fuzzy reasoning spiking neural P systems for diagnosing faults in complex power systems,” *Complexity*, vol. 2019, Article ID 2635714, 16 pages, 2019.

[41] G. Zhang, H. Rong, F. Neri, and M. J. Pérez-Jiménez, “An optimization spiking neural P system for approximately solving combinatorial optimization problems,” *International Journal of Neural Systems*, vol. 24, no. 5, pp. 1–16, 2014.

[42] G. Zhang, M. Gheorghe, L. Pan, and M. J. Pérez-Jiménez, “Evolutionary membrane computing: a comprehensive survey and new results,” *Information Sciences*, vol. 279, pp. 528–551, 2014.

[43] A. B. Pavel and C. Buiu, “Using enzymatic numerical P systems for modeling mobile robot controllers,” *Natural Computing*, vol. 11, no. 3, pp. 387–393, 2012.

[44] C. Buiu, C. Vasile, and O. Arsene, “Development of membrane controllers for mobile robots,” *Information Sciences*, vol. 187, pp. 33–51, 2012.

[45] X. Wang, G. Zhang, F. Neri et al., “Design and implementation of membrane controllers for trajectory tracking of nonholonomic wheeled mobile robots,” *Integrated Computer-Aided Engineering*, vol. 23, no. 1, pp. 15–30, 2016.

[46] C. Buiu and A. G. Florea, “Membrane computing models and robot controller design, current results and challenges,” *Journal of Membrane Computing*, vol. 1, no. 4, pp. 262–269, 2019.

[47] T. Wu, A. Păun, Z. Zhang, and L. Pan, “Spiking neural P systems with polarizations,” *IEEE Transactions on Neural Networks & Learning Systems*, vol. 29, no. 8, pp. 3349–3360, 2018.

[48] T. Song, L. Pan, and G. Păun, “Spiking neural P systems with rules on synapses,” *Theoretical Computer Science*, vol. 529, pp. 82–95, 2014.

[49] G. Rozenberg and A. Salomaa, *Handbook of Formal Languages*, Springer, Berlin, Germany, 1997.