Field effect transistor sensors for liquid media

Water micropollutants: from detection to removal

November 26-28, 2018
Orléans
• Some liquid sensors
• Dual Gate FET
  • Examples
  • Process of Dual Gate TFT
  • Theory
• Characterization
• Tests for PH measurement
• Prospects
Water sensors

• Some measure parameter
  • Temperature
  • pH
  • conductivity
  • dissolved oxygen
  • turbidity

• Sensor principle
  • Thermistor
  • Redox sensor
  • Metallic electrodes
  • Electrochemical or optical
  • Optical measurement of diffuse light
PH sensors

- Equation:
  - Ox1 + Réd2 <-> Réd1 + Ox2
  
  \[ E = E^0 + \frac{RT}{nF} \ln \left( \frac{a_{ox}}{a_{red}} \right) \]  
  (Nernst equation)

- PdO + 2H\(^+\) + 2e\(^-\) <-> Pd + H\(_2\)O.

\[
E = E^{0} + 0.059 \cdot \log([H^+])
\]

\[
E = E^{0} + 0.059 \cdot pH
\]

Y. Qin et al. / Sensors and Actuators B 255 (2018) 781–790
Sensors objective

• Developing high sensitive sensors from:
  • Electronic device
  • Compatible technologies
  • Easy to functionalize

• Field effect transistors:
  • Detection of charges linked to the surface
  • Easy measurement
  • Numerous possibilities for the technology
  • Low cost and high number of devices

• Specialized in silicon based technologies:
  • Thin film devices
  • Low temperature process
  • Good electrical properties

• TFT as chemical sensors:
  • Different technologies
  • Compatibility with chemical and biological functionalization
  • Possibility to integrate microfluidic
  • Usable in liquid media
  • Highly sensitive devices
Main principle silicon based sensors

- **ISFET**: Ions Sensitive Field Effect Transistors

  ![ISFET Diagram](image)

  pH sensor

  

  pH variation: shift of the transfer characteristic and of the threshold voltage

  \[
  S = \frac{d\psi}{dpH_s} = -2,3 \frac{kT}{q} \alpha 
  \]

Sensitivity: \( S = 59 \text{ mV/pH} \) (Nernst equation)

Well-known device with main advantages

- Limitation of the sensitivity
Main principle silicon based sensors

• SGFET : Suspended Gate Field effect Transistor

MOS or TFT structure
With suspended gate

Compatible with measurements in liquid media
→ pH sensor (Si₃N₄ layer)

Sensitivity : \( \Delta V_{gs} / pH = 255 \text{ mV / pH} \)

Biosensors
• Chemical and biological functionalization
• Antigens/Antibodies
Microfluidics integration

With PDMS microchannels

- Control of the volume
- Continuous flow
- Same sensitivity

With integrated microchannels (front or rear face)

![Microchannel diagram]

- Sensitivity 290mV/pH

![Graph showing pH sensitivity]

- With PDMS microchannels
- Doped area
- Aluminum
- Photoresist
- SiNx

![Inlet/Outlet and Gate diagram]
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Improved sensing characteristics of dual-gate transistor sensor using silicon nanowire arrays defined by nanoimprint lithography
Lim et al., Science and Technology of Advanced Materials, 2017 VOL. 18, NO. 1, 17–25

- nanoimprinted SiNW for the active layer
- Silicon dioxide
- Extended gate

High sensitivity
PTAA stands for the organic semiconductor polytriarylamine.

- The top dielectric consists of a stack of poly-isobutylmethacrylate (PIBMA) and the Teflon derivative AF-1600.

Sensitivity to pH versus coupling capacitance
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Dual Gate TFT with polysilicon

- **SiO$_2$ deposition**
  - **Process:** APCVD
  - **Gas:** Silane/Oxygene
  - **Temperature:** 420°C
  - **Deposition rate:** 29 nm/min
  - **Thickness:** 800 nm

- **Wafer insulation (silicon oxide)**
- **Silicon Wafer**
Dual Gate TFT with polysilicon

**Dry etching**
- **Process**: Plasma
- **Power**: 30w
- **Flow rate**: 30sccm
- **Pressure**: 4 Pa
- **Etching rate**: ~150nm/min

**Doped polysilicon deposition**
- **Process**: LPCVD
- **Gas**: Silane, phosphore
- **Pressure**: 90 Pa
- **Deposition rate**: 5 nm/min
- **Thickness**: 300 nm

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Highly doped polysilicon

Wafer insulation (silicon oxide)

Silicon Wafer
Doped polysilicon deposition
Process: LPCVD
Gas: Silane, phosphore
Pressure: 90 Pa
Deposition rate: 5 nm/min
thickness: 300 nm

Dry etching
Process: Plasma
power: 30w
Flow rate: 30sccm
Pressure: 4 Pa
Etching rate: environ 150nm/min

Highly doped polysilicon
Wafer insulation (silicon oxide)
Silicon Wafer
Dual Gate TFT with polysilicon

Insulator layer ($\text{Si}_3\text{N}_4$)

Highly doped polysilicon

Wafer insulation (silicon oxide)

Silicon Wafer

$\text{Si}_3\text{N}_4$ Deposition

Process: LPCVD
Gaz: Silane/Ammoniac
Pressure: 60 Pa
Temperature: 725°C
Deposition rate: 4 nm/min
Thickness: Variable
Dual Gate TFT with polysilicon

 Deposition of Si₃N₄
Process: LPCVD
Gas: Silane/NH₃
Pressure: 60 Pa
Temperature: 725°C
Deposition rate: 4 nm/min
thickness: Variable

 Deposition of SiO₂
Process: APCVD
Gas: Silane/Oxygène
Temperature: 420°C
Deposition rate: 29 nm/min
thickness: Variable
Dual Gate TFT with polysilicon

Wet etching of SiO₂
Process: BHF
Etching rate: environ 15nm/min

Dry etching
Process: Plasma
Power: 30 W
Flow rate: 10 sccm
Pressure: 1 Pa

Layers:
- Insulator layer (SiO₂)
- Insulator layer (Si₃N₄)
- Highly doped polysilicon
- Wafer insulation (silicon oxide)
- Silicon Wafer
Dual Gate TFT with polysilicon

- Insulator layer ($\text{SiO}_2$)
- Insulator layer ($\text{Si}_3\text{N}_4$)
- Highly doped polysilicon
- Wafer insulation (silicon oxide)
- Silicon Wafer
Doped silicon deposition

Process: LPCVD
Gas: Silane, phosphore
Pressure: 90 Pa
Deposition rate: 5 nm/min
Thickness: 300 nm

Dual Gate TFT with polysilicon

- Insulator layer (SiO$_2$)
- Insulator layer (Si$_3$N$_4$)
- Highly doped polysilicon
- Wafer insulation (silicon oxide)
- Silicon Wafer
Dual Gate TFT with polysilicon

Poly-silicon deposition

Process: LPCVD
Gas: Silane
Pressure: 90 Pa
Deposition rate: 5 nm/min
thickness: 100 nm
First electrical measurement

![Graph showing the relationship between drain current ($I_D$) and gate-source voltage ($V_{GS}$) before encapsulation.](image)

- **Before encapsulation**

**Axes:**
- $I_D$ (A) on the y-axis
- $V_{GS}$ (V) on the x-axis

**Legend:**
- Solid line: Before encapsulation
Dual Gate TFT with polysilicon

Si₃N₄ deposition
Process: LPCVD
Gas: Silane/Amonia
Pressure: 60 Pa
Temperature: 725°C
Deposition rate: 4 nm/min
thickness: Variable

SiO₂ deposition
Process: APCVD
Gas: Silane/Oxygène
Temperature: 420°C
Deposition rate: 29 nm/min
thickness: Variable

Poly-silicon
Insulator layer (SiO₂)
Insulator layer (Si₃N₄)
Highly doped polysilicon
Wafer insulation (silicon oxide)
Silicon Wafer
Wet etching of SiO₂

**Process:** Solution de BHF

Dry etching

**Process:** Plasma
**Power:** 30 W
**Flow rate:** 10 sccm
**Pressure:** 1 Pa
**Etching rate:** environ 15nm/min
1\textsuperscript{st} Goal: decrease of the threshold voltage for bottom gate structure.

Test with several bottom gate insulators → Thicknesses

**Best result**
- Low threshold voltage
- Low dispersion in data point
Final transfer characteristic

- Before encapsulation
- After encapsulation
- After Forming Gas

$I_D (A)$ vs. $V_{GS} (V)$

$I_D$ ranges from 5,0µ to 20,0µ
$V_{GS}$ ranges from -10 to 30
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Modeling

\[ V_{DS} = 1V \]

\[ V_{G,Bottom} = 10V \quad V_{G,top} = 0V \]

\[ V_{G,Bottom} = 0V \quad V_{G,top} = 0V \]
Theoretical amplification calculated from capacitance amplification: \[ \frac{C_{Top}}{C_{Bottom}} \]

Real amplification (for TFT):

\[
I_D = \frac{W}{L} V_{DS} \left[ \mu_{Bottom} \cdot C_{Bottom} \left( V_{G,Bottom} - V_{th,Bottom} \right) + \mu_{Top} \cdot C_{Top} \left( V_{G,Top} - V_{th,Top} \right) \right]
\]

\[
I_D = \frac{W}{L} V_{DS} \left[ \mu_{Bottom} \cdot C_{Bottom} \left( V_{G,Bottom} - V_{th,Total} \right) \right]
\]

\[
V_{th,Total} = V_{th,Bottom} - \frac{\mu_{Top} \cdot C_{Top}}{\mu_{Bottom} \cdot C_{Bottom}} \left( V_{G,Top} - V_{th,Top} \right)
\]

\[
\Delta V_{th,Total} = \frac{\mu_{Top} \cdot C_{Top}}{\mu_{Bottom} \cdot C_{Bottom}} \left( \Delta V_{th,Top} \right)
\]

Sensitivity
Modeling

\[ V_{DS} = 1V \]

\[ V_{G,\text{top}} = 2V \]

\[ V_{G,\text{bottom}} = 0V, \ V_{G,\text{top}} = 2V \]

\[ V_{G,\text{bottom}} = 0V, \ V_{G,\text{top}} = 0V \]
Dual gate operation

Active layer: undoped polysilicon 100 nm

Gate layers: highly doped polysilicon

Top gate insulator
- $\text{Si}_3\text{N}_4$, 25 nm
- $\text{SiO}_2$, 25 nm
- $\text{SiO}_2$, 5.5 nm (native oxide) $C_{\text{Top}} = 6.2 \times 10^{-7} \text{ F/cm}^2$

Theoretical amplification:
\[
\frac{C_{\text{Top}}}{C_{\text{Bottom}}} = 2
\]
\[
\frac{C_{\text{Top}}}{C_{\text{Bottom}}} = 14
\]

| Material   | $\varepsilon_r$ | Thickness (nm) |
|------------|----------------|----------------|
| $\text{SiO}_2$ | 3.90          | 50             |
| $\text{Si}_3\text{N}_4$ | 6.90          | 50             |
| $\text{SiO}_2$ | 3.90          | 5.5            |

\[\epsilon_{eq} = \frac{d_1 + d_2}{\varepsilon_1 + \frac{d_2}{\varepsilon_2}}\]

$C_{\text{Bottom}} = 4.4 \times 10^{-8} \text{ F/cm}^2$
Water measurement

Droplet Polarization

- $V_{\text{top}}=0\,\text{V}$
- $V_{\text{top}}=0.1\,\text{V}$
- $V_{\text{top}}=0.2\,\text{V}$
- $V_{\text{top}}=0.3\,\text{V}$
- $V_{\text{top}}=0.4\,\text{V}$

Drain Current (A) vs Bottom gate voltage (V)

- $0 \times 10^{-7}$
- $1 \times 10^{-7}$
- $2 \times 10^{-7}$
- $3 \times 10^{-7}$
- $4 \times 10^{-7}$
- $5 \times 10^{-7}$
- $6 \times 10^{-7}$
- $7 \times 10^{-7}$
- $8 \times 10^{-7}$
- $9 \times 10^{-7}$
- $1 \times 10^{-6}$
- $2 \times 10^{-6}$
- $3 \times 10^{-6}$
- $4 \times 10^{-6}$
- $5 \times 10^{-6}$
- $6 \times 10^{-6}$
- $7 \times 10^{-6}$
- $8 \times 10^{-6}$
- $9 \times 10^{-6}$
- $1 \times 10^{-5}$
- $2 \times 10^{-5}$
- $3 \times 10^{-5}$
- $4 \times 10^{-5}$
- $5 \times 10^{-5}$
- $6 \times 10^{-5}$
- $7 \times 10^{-5}$
- $8 \times 10^{-5}$
- $9 \times 10^{-5}$
- $1 \times 10^{-4}$
- $2 \times 10^{-4}$
- $3 \times 10^{-4}$
- $4 \times 10^{-4}$
- $5 \times 10^{-4}$
- $6 \times 10^{-4}$
- $7 \times 10^{-4}$
- $8 \times 10^{-4}$
- $9 \times 10^{-4}$
- $1 \times 10^{-3}$
- $2 \times 10^{-3}$
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- $4 \times 10^{-3}$
- $5 \times 10^{-3}$
- $6 \times 10^{-3}$
- $7 \times 10^{-3}$
- $8 \times 10^{-3}$
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- $1 \times 10^{-2}$
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- $1 \times 10^{-1}$
- $2 \times 10^{-1}$
- $3 \times 10^{-1}$
- $4 \times 10^{-1}$
- $5 \times 10^{-1}$
- $6 \times 10^{-1}$
- $7 \times 10^{-1}$
- $8 \times 10^{-1}$
- $9 \times 10^{-1}$
- $1 \times 10$
PH measurement \((C_{\text{top}} \rightarrow 5.5\text{nm})\)

Amplification factor > 14

- Amplification factor: 1098 mV/pH
- 853 mV/pH
Possibilities to decrease the top gate threshold voltage

Decrease the top insulator thickness
→ Limitations due to electrical insulation

Increase of the quality of the interface between silicon dioxide and polysilicon
→ Optimization already done

Increase of the quality of polysilicon layer
→ Optimization already done (low temperature process)
→ Many traps at grain boundaries and between interfaces
→ High threshold voltage

Increase the doping level of polysilicon
→ Modification of the transfer characteristic
→ Increase the conductance
TFT with low doped polysilicon

Active layer:
- Polysilicon deposited from silane by LPCVD
- In-situ doping with phosphine (control of the ratio of gases)

Characterization versus Bottom gate

Field effect → Channel conductance
Low On/off ratio → Not important for sensing

Comparison Top gate versus Bottom gate transfer characteristics

$V_{G \text{Top}}$ compatible with tests in liquid
Dual Gate TFT with low doped polysilicon

Transfer characteristics versus $V_{GBottom}$
With different values of $V_{GTop}$

$V_{GTop}$ from 0 to 2V

Large increase of the current due to the top channel

Voltage shift with fixed $I_{DS}$

The slope gives the amplification ratio

$I_D = 325$ nA

$I_D = 225$ nA
Measurements in liquids

Top Gate with polarized droplet  ➔  Metallic electrode (Ti/Au) for Top gate

Comparison of transfer characteristics
• With metallic Gate (Al)
• With liquid Gate

Good correlation showing the good functioning in liquid media
The amplification value increases with $V_{G\text{Top}}$ 

Top channel formation

The amplification value is higher at low $V_{G\text{Bottom}}$ 

Top channel more influent than Bottom channel

Measured amplification >> Calculated amplification ($C_{\text{Top}}/C_{\text{Bottom}}$)
Comparison of Amplification values

Theoretical values

Amplification range consistent with theory

Increase of the amplification with polysilicon layers

Measured values

Amplification range consistent with theory

Increase of the amplification with polysilicon layers
Several tests with solutions with various pH values

- Sensitivity above the Nernst value > 59 mV/pH
- Highly dependent on polarization
- The sensitivity is higher for low bottom gate voltage (under 4V) and increases with the top gate voltage.
  consistent with previous calculated and measured amplification values in dual gate configuration

Examples:

Amplification factor with :
- $V_{G_{Bottom}}$ around 3
- $V_{G_{Top}} = 0.75V$
  $\Rightarrow$ 3.5
  $\Rightarrow$ pH sensitivity around 200 mV/pH

Amplification with :
- $V_{G_{Bottom}}$ around 3
- $V_{G_{Top}} = 0.5 V$
  $\Rightarrow$ 2.6
  $\Rightarrow$ around 150 mV/pH
Prospects: Applications to biodetection

- Very promising results with pH
- Application to bio elements
- Integration of nanomaterials on the top surface
  - Nanowires, nanotubes, nanocarbons (porous)
- Create a structure based on Extended gate TFT

Increase the surface and interactions with biomolecules
Sensor for biodetection

- Easy measurement
- Integrated
- Highly sensitive
- High selectivity

Electronic detection

Sensor sensitivity
- Surface
- Nanomaterials

Functionalization:
- Chemical
- Biological

Acknowledgment: ANR PlasBioSens
Thank you for your attention
A self-amplified transistor immunosensor under dual gate operation: highly sensitive detection of hepatitis B surface antigen
Lee et al, Nanoscale 7(40):16789, 2015

- SOI (Silicon on Insulator) for the active layer
- Silicon dioxide as insulator
- Extended gate

Application to biosensing
Antigen / Antibody links
Dual Gate TFT with polysilicon

Final structure

External top gate contact

Deposition of a top gate contact (aluminum) ➔ Top gate Bottom gate Dual gate Characterization

Capacitive amplification

Characterization with liquid (pH sensor) : with deported electrode (Au/Ti)
Characterization: Bottom gate

Transfer characteristic

| Mobility $\mu_{FE}$ (cm²/V.s) | Threshold voltage $V_{th}$ (V) |
|-------------------------------|-------------------------------|
| 12.5                          | 10                            |

Dual Gate Characteristics

$I_{DS}$ with $V_{GTop}$

$V_{DS} = 1V$

$V_{GTop} = 0$ to $2V$

$V_{DS} = 1V$

$V_{GTop} = 0$ to $2V$
I\textsubscript{DS} fixed to 2 µA or 3 µA

For each V\textsubscript{GTop}:

\begin{align*}
V_1 &= V_{G\text{Bottom}} (I_{DS} = 2 \, \mu\text{A}) \\
V_2 &= V_{G\text{Bottom}} (I_{DS} = 3 \, \mu\text{A})
\end{align*}

Effect for V\textsubscript{GTop} > 1V

\[ \Delta V = \Delta V_{G\text{Top}} \]

No capacitance amplification

Potential shift

Top Gate threshold voltage to high