Design of an Online Brain-Computer Interface System Based on Field Programmable Gate Array

Zhengquan Feng¹, Lin Zeng¹, Haijing Wu², Fengchun Tian² and Qinghua He¹,*

¹ State Key Laboratory of Trauma, Burns and Combined Injury, Daping Hospital, Army Medical University, Chongqing, China
² College of Communication Engineering, Chongqing University, Chongqing, China

*Corresponding author email: qinghuahe@126.com

Abstract. In the article, an online brain-computer interface (BCI) demo system based on Field Programmable Gate Array (FPGA) was designed. A colour visual stimulator based on a Video Graphics Array (VGA) monitor controlled by FPGA is designed to produce transient visual stimulations. An electroencephalography (EEG) acquisition module including active electrodes and driven-right-leg circuit is used to acquire the visual evoked potential (VEP) signal; Finite impulse response (FIR) filtering combined with an averaging method allows for extraction of the weak VEP signals. The template matching method is used in target identification. The FPGA is successfully used in the BCI system to complete multiple tasks such as the VGA controller, analog to digital (AD) converter controller, VEP signal processor and electronic device controller. Experiments show that the subjects’ transient VEP can successfully activate the electronic devices by the online BCI system which has relatively high identification accuracy. All these results show that the real time BCI demo system based on FPGA is feasible and effective.

1. Introduction
A BCI (brain-computer interface) is a communication system connecting the brain to a computer or other electronic device. Current interests in BCI development mainly come from the hope that this technology could become a valuable new enhanced communication option for those with severe motor disabilities such that use of conventional augmentative technologies is impossible. In EEG-based BCIs, event-related potentials, event-related synchronization and desynchronization, mu and beta rhythms, visual evoked potentials (VEP), and slow cortical potentials are commonly used signals [1]–[4]. VEP have been commonly used as neural signals to transmit user intention to BCI systems, these VEP are derived from the brain’s response to visual stimulation. According to the stimulus rates, VEP corresponding to rapidly repetitive stimulations are categorized as steady-state VEP (SSVEP), and those corresponding to low stimulus rates are categorized as transient VEP (TVEP). So far, both SSVEP and TVEP have already been applied in BCI research [5]-[16]. Among them, Professor Gao’s team of Tsinghua University mainly utilized SSVEP as the input signal of BCI system [6-9,11-12,16]. In the article, TVEP is used as the input signal.

Vidal was probably the first person to report the real-time detection of TVEP for BCI in 1970s. Vidal used the spatial distributions of TVEPs evoked to identify visual fixation by a stimulus located in different visual fields [17]. In 1992, Sutter developed a TVEP-based BCI called the brain response interface (BRI) [18]. A subject with implanted electrodes reached the communication rates of 10 to 12 words per minute. Guo et al proposed a novel BCI based on motion-onset visual evoked potentials (mVEPs) and the result of off-line experiments verified the feasibility of an mVEP-based BCI.
paradigm [19]. Motion-onset VEP elicited by the motion behaviour of the visual object, that is a new kind of TVEP for BCI. The technology causes less visual discomfort and fatigue for the BCI user. Using motion-onset VEPs Liu et al implemented an online BCI system, and the BCI system attained a mean information transfer rats (ITR) of 42.1 bits per min [20].

In recent years, some researchers have been developing practical BCI based on SSVEP. SSVEP BCI has the following advantages, including simple system configuration, little or no user training, and a high ITR (30–60 bits per min). Shyu et al. developed a low-cost multimedia control system of SSVEP BCI based on Field Programmable Gate Array (FPGA) [21]. The SSVEP signal processing algorithm of BCI system is implemented with FPGA. Wang et al. developed a wearable and wireless online SSVEP BCI [22]. The system integrated a wireless and mobile EEG system and a signal-processing platform based on mobile phone platform.

In our previous studies, we have developed an off-line BCI based on TVEP [23]. EEG data acquisition used Active One bio-potential measurement system of Biosemi Inc. One computer was used for visual stimulation; another computer was used for data acquisition and signal analysis. This BCI experiment system was expensive and bulky and the algorithm was implemented off-line.

We wish to design a real time BCI system that could help the seriously disabled to control electrical devices. In this work, an online TVEP based BCI demo system was designed to turn on or turn off the light and the fan. VEP acquisition module was designed instead of using expensive commercial EEG system. FPGA has large amounts of embedded memory and reconfigurable gate arrays, which allows for parallel architectures and thus increases system performance; therefore FPGA was used to design the on-line BCI system.

2. Methods and Materials
The design of an on-line BCI system includes two parts. The first part is the system design and the second part is algorithm implementation.

2.1. System Design
In Fig. 1, the block diagram of the FPGA based BCI system using TVEP is shown. The designed system includes: 1) a visual stimulator, 2) a VEP acquisition module, 3) FPGA board, 4) a BCI control module. The Altera Cyclone II EP2C35 DSP development board is adopted to realize the on line BCI system. In this system, FPGA development board plays a core role, which serves as the VGA controller, AD converter controller, VEP signal processor and device controller.

The visual stimulator was developed using a VGA monitor. Both LCD and CRT monitor can be used as the stimulator. A computer LCD monitor is used for stimulus display. The visual stimulator consists of 4 flickering targets in the form of reversing checkerboard. Fig. 2. is a picture of the stimulus display. 4 different icon represent switching the light and the fan. The black/white checkerboard is reversing in designed sequence to induce transient visual stimulation. The VGA display is controlled by FPGA.

The stimulation pattern and VGA time sequences is produced through Very-High-Speed Circuit Hardware Description Language (VHDL) program in FPGA. R, G and B signals are transformed into analog signals through the triple video D/A converter FMS3818. In this work, the resolution of the LCD monitor is 640×480. The horizontal scanning frequency is 31.469 kHz and the vertical scanning frequency is 59.94Hz.

The flickering cycle of each visual stimuli is 300ms. The four stimuli are flickering in the same frequency but in different phase. The time delay between the neighbouring stimuli is 75ms. The image description of four targets is also realized by VHDL programming.

A VEP acquisition module was designed for the BCI system. In Fig. 3, the block diagram of the VEP acquisition module was indicated. Three EEG electrodes collect the VEP signal from the scalp, those were installed according to the International EEG 10–20 system. The first electrode (VEP_POS) was located at the occipital region Oz, the second electrode (VEP_NEG) was located at the central region Cz, and the third electrode (VEP_DRL) was located at the left mastoid. To reduce large noise, the first and the second electrode were designed as active electrodes. To eliminate loading effects, the active electrode used a pre-amplifier as a voltage follower (Unity Buffer Amplifier). The preamplifier used an instrumentation amplifier AD620 (Gain: 20), to amplify the bipolar EEG signal at first. AD620 has
high input impedance and high gain along with a good common-mode rejection ratio (CMRR) (CMRR=100 dB). Therefore, the current research used the AD620 as pre-amplifier. Firstly, the pre-amplified VEP signal was filtered by a high pass filter (cut-off frequency: 1.06 Hz). And then the low-pass filter used by an active second-order Butterworth filter (cutoff frequency: 26 Hz). Finally, the signal was post-amplified (Gain: 800). Next, for adjust the output voltage level to the desired range, a DC bias adjustment circuit was used (peak-to-peak voltage range: 0–5 V). A driven-right-leg (DRL) circuit was also designed to reduce common-mode interference. The analog signal was converted into a digital signal by the 16-bit ADC chip AD7683. The Ad7683 is a high speed, low power ADC chip, contains 16-bit sampling ADC with no missing codes, a serial SPI-compatible interface port and an internal conversion clock. The ADC controller was realized by VHDL programming of FPGA with a sampling frequency of 200 Hz.

Figure 1. Block diagram of TVEP BCI system based on FPGA

Figure 2. VGA visual stimulator

Figure 3. Block diagram of the VEP acquisition module

High-speed transistor opto-couplers 6N136 were used to design the photoelectric coupled isolate circuit between the VEP acquisition circuit and the FPGA development board to ensure the electrical safety of EEG detection. At the same time, it also prevents noise from the digital circuits which can
disturb the VEP signal acquisition. The VEP acquisition circuits were integrated onto a printed-circuit board (PCB).

2.2. Algorithm Implementation

The subject was asked to stare on one of four on screen stimulus targets for several seconds to have a BCI choice. The signal processor was used to determine which target the subject is looking at. Averaging method is commonly used to improve the signal-noise ratio (SNR) in electrophysiological measurements. FIR filter can be combined with the averaging method for the purpose of reducing the number of accumulation. Almost 20 trials of averaging are needed for VEP recognition. The developed signal processing algorithms were used to extract the weak VEP signals from strong noise. The acquired EEG signal from the ADC was first segmented and averaged according to different stimulus. The averaged data was subtracted by the mean to finish the DC offset removing. Then the DC offset removed data was filtered by a 15 order FIR filter. The 15 order low pass FIR filter (Fc=10Hz) filter was designed using the MATLAB FDATool (Filter Design and Analysis Tool), then converted to HDL code and implemented in FPGA. Fig. 4 illustrated the magnitude response of the low pass FIR filter.

![Figure 4. Magnitude response of the low pass FIR filter (order=15; window: Hamming; Fs=200Hz; Fc=10Hz)](image)

A template matching method was applied to target identification. A training stage was implemented to obtain the VEP template. The steps of target identification are as follows:

- In the training stage, the subject is instructed to fixate on one of four targets. During N stimulation cycles, EEG data is collected, recorded as Xn, n=1, 2, ..., N.
- The average value of EEG data in N cycles is used as a VEP template M, DC offset removing and filtering by a low pass FIR filter.
- Between a segment of EEG data X and the template M, the correlation coefficient is calculated as:

\[
\rho_{X,M} = \frac{\text{cov}(X,M)}{\sqrt{D(x)} \sqrt{D(M)}}
\]  

(1)

- Identify the fixation target by selecting the target which maximizes the correlation coefficient. If the correlation coefficient is close to 1, it is that the EEG data has stood a good chance of being the VEP signal. If all of the correlation coefficients are below the threshold, it means that the subject hasn’t gazed at any target. The output of the BCI is 0 and there is no control on the light or the fan. Otherwise, the output of the BCI is the sequence number of corresponding target with the max correlation coefficient.

The VEP signal processing algorithm was implemented in the Altera Cyclone II EP2C35 FPGA through VHDL programming.

3. Experiments

After giving informed consent, eight healthy (2 females, 6 males) subjects participated in this experiment, that aged from 22 to 33, with normal or corrected to normal vision. The experiments were carried out in an ordinary office room without any electromagnetic shielding. Subjects were seated at a distance of about 50 cm from the screen. Fig.5 is a picture of BCI experiment.
EEG signals were acquired through three electrodes placed on the scalp. The first electrode (POS) was placed at the occipital region Oz, the second electrode (NEG) was placed at the central region Cz, and the third electrode (DRL) was placed at the left mastoid. After placement of the electrodes, the subject was asked to close their eyes for about 1 minute to check if there is alpha EEG signal. Alpha waves are one type of brain wave originating from the occipital lobe during wakeful relaxation with closed eyes. The FPGA would do FFT analysis of the EEG signal to check if the dominant frequency is in 8-13Hz domain. Fig. 6 is the waveform of alpha wave collected by the designed system. If there are alpha waves, the system will turn on an LED indicating the connection of electrodes and the scalp is good and the EEG acquisition circuit works well. Experiments had been carried on in order to test the function of active electrode and DRL circuit. When the first electrode was not used as the active electrode, that is the electrodes were directly connected to the pre-amplifier without using the voltage follower, the acquired signals were embedded with high levels of 50 Hz noise. When not using DRL electrode, the acquired EEG signals were also embedded with high levels of 50Hz noise. Without using the active electrodes and DRL circuit, the VEP acquisition circuit could not detect alpha wave when the subject closed his eyes.

![Figure 5. Picture of BCI experiment](image)

**Figure 5.** Picture of BCI experiment

**Figure 6.** Waveform of alpha waves

![Figure 7. Waveform of VEP; (a) 20 trials averaged VEP; (b) averaged and FIR filtered VEP](image)

**Figure 7.** Waveform of VEP; (a) 20 trials averaged VEP; (b) averaged and FIR filtered VEP

Before BCI experiments, the subject was asked to stare on one flickering stimuli on the screen for 1 minute to acquire his VEP template. The VEP template was then saved in FPGA used for further signal processing. Fig.7 is the waveform of VEP acquired by the BCI system. Figure (a) is the 20 trials averaged VEP, the envelope of the VEP can be seen from the figure. Figure (b) is the averaged and FIR filtered VEP, the waveform of VEP is smoother after filtering. Table I is the results of BCI testing experiments. In the testing experiments, the subject was asked to stare on the four flickering
stimuli representing different electronic device control. Each subject was asked to finish 16 trials of BCI testing experiments. During the BCI testing experiment, the subject was asked to stare at one of the four flickering stimuli for several seconds in one trial to control the light or the fan. The statistics of correct trials and false trials of each subject in the testing experiment is in Table 1.

Table 1. Results of BCI testing experiments.

| Subject | Correct trials | False trials | Accuracy |
|---------|----------------|--------------|----------|
| MJW     | 13             | 3            | 81.25%   |
| FZB     | 14             | 2            | 87.50%   |
| LP      | 15             | 1            | 93.75%   |
| XZQ     | 14             | 2            | 87.50%   |
| YH      | 14             | 2            | 87.50%   |
| WSC     | 15             | 1            | 93.75%   |
| FS      | 16             | 0            | 93.75%   |
| GYS     | 16             | 0            | 100%     |

4. Discussion and Conclusion

The ITR of the proposed BCI system is below 20 bits/min. That is because TVEP BCIs have a lower ITR compared with SSVEP BCIs. SSVEP BCI systems usually have a high ITR of 30-60 bits/min. In our previous experiments, we found a few subjects whose TVEP is quite good, but with very poor SSVEP. Some feel the higher frequency visual stimulation visual fatigue more easily than the lower frequency stimulation. SSVEPs contain more frequency information of stimulation, while TVEPs contain more subtle waveform information. Besides SSVEP, TVEP may also be a choice of EEG signal for some BCI users. That is still poses severe challenges, Moving a BCI system from a laboratory demonstration to real-life applications, for the BCI community. Research on the development of practical TVEP is also worthwhile.

In the article, an online FPGA based BCI demo system was designed for controlling electronic devices. Experiments showed the designed VEP acquisition module including active electrodes and driven-right-leg circuit is helpful to improve SNR. The acquired VEP EEG signal can satisfy the need for BCI application. The operation of EEG collecting is simple and noninvasive with only three electrodes. The designed VEP acquisition module is much cheaper and miniature than commercial EEG system, which is beneficial to design practical BCI system. The visual stimulator was implemented on VGA monitor controlled by FPGA. The stimulation pattern and VGA time sequences were produced through VHDL program in FPGA. Experiments showed that the FPGA based visual stimulator can produce effective transient visual stimulation. FIR filtering combined with averaging method was used to improve SNR. A template matching method is used for target identification. Through computing the correlation coefficient, the algorithm could finish target identification. All the algorithms were implemented by VHDL programming in FPGA.

Experiments showed that the subjects’ TVEP can successfully switch the light and the fan through the online BCI system with relatively high identification accuracy. FPGA was successfully used in BCI system to finish multiple tasks as the VGA controller, AD converter controller, VEP signal processor and electronic device controller.

The experimental results have a certain reference value for the design of a wearable and portable BCI system. The research in future will focus on improving the accuracy, ITC and low power design. It has important application value in rehabilitation engineering and other fields.

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