A CMOS-Thyristor Based Temperature Sensor with +0.37 °C/−0.32 °C Inaccuracy

Jing Li *, Yuyu Lin, Siyuan Ye, Kejun Wu, Ning Ning and Qi Yu

University of Electronic Science and Technology of China, Chengdu 610054, China; linyuyuchn@163.com (Y.L.); 18215521294@163.com (S.Y.); kjwu@uestc.edu.cn (K.W.); ning_ning@uestc.edu.cn (N.N.); qiyu@uestc.edu.cn (Q.Y.)

* Correspondence: lijing686@uestc.edu.cn

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Abstract: This paper describes a voltage controlled oscillator (VCO) based temperature sensor. The VCOs are composed of complementary metal–oxide–semiconductor (CMOS) thyristor with the advantage of low power consumption. The period of the VCO is temperature dependent and is function of the transistors’ threshold voltage and bias current. To obtain linear temperature characteristics, this paper constructed the period ratio between two different-type VCOs. The period ratio is independent of the temperature characteristics from current source, which makes the bias current generator simplified. The temperature sensor was designed in 130 nm CMOS process and it occupies an active area of 0.06 mm². Based on the post-layout simulation results, after a first-order fit, the sensor achieves an inaccuracy of +0.37/−0.32 °C from 0 °C to 80 °C, while the average power consumption of the sensor at room temperature is 156 nW.

Keywords: temperature sensor; CMOS thyristor; VCO

1. Introduction

Temperature sensors are desirable for temperature sensing and compensation in modern applications, such as medical, environmental monitoring, thermal monitoring and wireless Internet-of-Things (IoT) platforms [1–3]. Most of such applications are battery powered for portability, durability or deployment flexibility [4,5], and put a strict power budget on temperature sensor which drives the power consumption to sub-µW and even to near-zero.

Prior works have demonstrated low-power-consumption temperature sensors based on bipolar junction transistors (BJT) [6–8], resistors [9,10], and complementary metal–oxide–semiconductor (CMOS) [11–16]. BJT-based temperature sensors converse the temperature by comparing a temperature-dependent voltage to a temperature-insensitive voltage or inversely temperature-dependent voltage. The voltage difference between these two voltages is quantized by a ΣΔ-ADC (Analog-to-Digital Converter), which achieves high resolution up to 0.002 °C and inaccuracy less than ±0.2 °C [6–8]. Resistor-based temperature sensors can achieve higher resolution and energy efficiency than BJT-based sensors. As discussed in Ref. [9], the authors use a temperature-dependent RC (Resistor and Capacitor) filter to extract the temperature information. In Ref. [10], the authors build a resistor based Wheatstone bridge whose voltage difference is proportional to the temperature. Both the temperature-dependent phase shift and voltage difference are sequentially digitized by ΣΔ-ADCs. ΣΔ-ADCs achieve high resolution at the cost of high power consumption and hardware cost from the decimation filter which normally are not mentioned in papers. Thus, the sacrifice of power consumption and hardware make BJT and resistor based temperature sensors not an optimal choice for battery powered applications. CMOS based temperature sensors are normally composed of digital delay cells. They are much more area efficient and easier to scale down with process. The authors in Ref. [13] demonstrate a VCO based temperature
sensor. The temperature information is extracted by two VCOs with different temperature-dependent frequency. The temperature sensor is fully composed of digital circuit and thus achieves an attractive area. On the other hand, the authors in Ref. [12] firstly create a temperature-dependent current and then transfer the current to frequency by VCOs. It provides better linearity and accuracy.

This paper proposes a VCO based temperature sensor and the VCO is composed of two-stage CMOS thyristor to simplify the circuit and achieve low power consumption.

2. Proposed CMOS Thyristor Based VCO

The proposed VCO is composed of multi-stage delay cells circled together. The desired oscillation frequency is inversely proportional to the number of stages and delay time of delay cell. Increasing the stages or delay time is necessary to reduce the oscillation frequency for low power consumption. Commonly, CMOS inverter is adopted as delay cell for its simplicity and scalability [12–16]. Its delay time is process dependent and ranges from ps to ns in sub-μm CMOS process. It may achieve μs delay by using the current-starved architecture but at the cost of large capacitors [14–16].

2.1. Basics of CMOS Thyristor Based Delay Cell

CMOS thyristor was proposed to increase the delay [17,18]. As shown in Figure 1, M2 and M4 work as a thyristor. M3 and M5 receive the input signal VIp and VIN, respectively, while VIN is the complementary signal of VIp. Current source IBN is used to sink current from VON via switch M1 according to the status of VIp. C0 is the total capacitance on node VON. When VIp is low, M5/M3 are conducted and M1 is non-conducted, VON and VOP are reset to VDD and GND, respectively. When VIp is changing to high, M5/M3 switch off and M1 switches on. Current source IBN starts sinking current from VON which results in node voltage decreasing from VDD. Approximately, M4 conducts when VIp reaches VDD-Vthp, where Vthp is the threshold voltage of M4. After that, VOP is charged from power supply VDD via M4 and increased rapidly. Sequentially, M2 conducts when VOP reaches Vthn and discharges current from VON together with IBN, where Vthn is the threshold voltage of M2. It accelerates the node voltage decrease on VON and constitutes a positive feedback loop between M2 and M4. Once the positive feedback is built, VON and VOP toggle to the opposite state in a short time. The corresponding delay value is calculated as [17]

\[
\tau_d = \frac{C_0 V_{thp}}{I_{BN}} + \sqrt{\frac{6C_1C_0^2}{kI_{BN}^2}} V_{thn} + \delta t
\]

where the first term on the right is the delay contributed by discharging C0, the second term is the delay contributed by charging C1, and \(\delta t\) is the regeneration time of the CMOS thyristor. C1 is the parasitic capacitance of VOP. In reality, because of the subthreshold effect, M4 charges the C1 simultaneously with M2 discharging C0. The second term can be neglected. Comparing to the first term, the regeneration time \(\delta t\) is small and can be omitted. The delay value can be approximated as

\[
\tau_d \approx \frac{C_0 V_{thp}}{I_{BN}}
\]

Both adopting a larger capacitor C0 and reducing sink current IBN are effective to increase the delay value. Since C0 generally adopts metal capacitor which is mostly temperature independent, the temperature coefficients are decided by the ratio of Vthp/IBN.
2.2. Proposed CMOS Thyristor Based VCO

VCO is generally constituted by multiple stages (beyond three stages) to satisfy the desired frequency. The more stages it has, the more devices are required, which would consume more power and also deteriorate the wave performance. To simplify the circuit and reduce device counts, a two-stage ring VCO is proposed and shown in Figure 2. The delay cell is composed of the CMOS thyristor based delay cell aforementioned. In the proposed architecture, the negative output \( V_{ON1} \) of the first stage is connected to the negative input \( V_{IN} \) of the second stage and \( V_{OP1} \) is connected to \( V_{IP} \). In this way, four-stage inversion is produced in the closed loop and thus makes it easy to satisfy the oscillation requirement of 360° phase shift.

![Figure 1. Complementary metal–oxide–semiconductor (CMOS) thyristor based delay cell.](image1)

![Figure 2. Proposed CMOS thyristor based voltage controlled oscillator (VCO).](image2)

Referred to the delay value of CMOS thyristor based delay cell in Equation (1), the oscillation period of the proposed VCO is given by

\[
T_{VCO,P} = \frac{2C_0V_{thp}}{I_{BN}}
\]

(3)

3. Temperature Sensor Architecture

As shown in Figure 3, two types of VCO are adopted to constitute the proposed temperature sensor. At the top, P-type VCO is composed of Delay_Cell_Ps. The delay value of Delay_Cell_P is approximately the discharging time on \( V_{ON} \) via \( I_{REFN} \) according to aforementioned analysis. Referring to Equation (3), the period of P-type VCO is given as

\[
T_{VCO,P} = \frac{2C_0V_{thp}}{I_{REFN}}
\]

(4)
Similarly, N-type VCO is composed of Delay_Cell_Ns. The delay value of Delay_Cell_N is approximately the charging time on \( V_{OP} \) via \( I_{REFP} \) according to aforementioned analysis. Referring to Equation (3), the period of N-type VCO is given as

\[
T_{VCO,N} = \frac{2C_3V_{thn}}{I_{REFP}} \tag{5}
\]

Based on Equations (4) and (5), the ratio between \( T_{VCO,P} \) and \( T_{VCO,N} \) is calculated

\[
ratio_T = \frac{T_{VCO,P}}{T_{VCO,N}} = \frac{C_0I_{REFP}}{C_3I_{REFN}} \frac{V_{thp}}{V_{thn}} \tag{6}
\]

\( C_0 \) and \( C_3 \) are composed of metal capacitors, which are temperature independent. \( I_{REFP} \) and \( I_{REFN} \) come from the same current source and they will have the same temperature characteristics and value. Thus, the ratio can be updated as

\[
ratio_T \propto \frac{V_{thp}}{V_{thn}} \tag{7}
\]

Because \( V_{thp} \) is temperature dependent to the first order [19], \( ratio_T \) is proportional to the temperature [13]. Thus, the ratio of the two-type VCO is used to detect temperature.

The complete block diagram of the proposed temperature sensor is shown in Figure 4. The left block is temperature sensor core which is composed of a P-type and a N-type VCO aforementioned. Bias current generator is used to provide the charging/discharging current \( I_{REFN}/I_{REFP} \).
The right block calculates the ratio between periods and transfers temperature to digital codes via two counters. The working principle of the Temperature to Digital is as follows. After RST switches to low, both counters start counting simultaneously. Counter1 counts CLKP to a constant value $M$ and generates a flag signal STOP. When receiving STOP signal, Counter2 ends counting CLKN with a value of $P$. The counting time of both counters are equal and it can be expressed as

$$M \cdot T_{VCO,P} = P \cdot T_{VCO,N}$$

(8)

The ratio between periods can be obtained

$$ratio_T = \frac{T_{VCO,P}}{T_{VCO,N}} = \frac{P}{M}$$

(9)

Since $M$ is a constant value, $P$ represents the $ratio_T$ and thus is proportional to the temperature. Eventually, $P$ is converted to digital code of $T_{code}$ and output for measurement.

4. Circuit Implementation

4.1. Delay Cell

The detail of delay cell is shown in Figure 5. The bias current $I_{REFP}$ and $I_{REFN}$ are composed of NMOS and PMOS working in saturation region separately. The switches $M_1$ in both delay cells adopt thin-gate MOSFET to achieve fast switching and low conductive resistance. Considering the charging/discharging current of $I_{REFP}/I_{REFN}$ on the magnitude of nA, all the others are thick-gate MOSFET to reduce influence of leakage current. Instead of just using $C_0$ and $C_3$ as what is shown in Figure 3, $C_1$ and $C_2$ are added to keep the load balance between Delay_Cell_P and Delay_Cell_N. MIM (Metal-Insulator-Metal) capacitors are adopted for $C_0$-$C_3$ to maintain process and temperature independence.

![Diagram of Delay Cell](a) (b)

**Figure 5.** Detail of delay cell (a) Delay_Cell_P (b) Delay_Cell_N.

4.2. Bias Current Generator

Bias current could be designed with any kind of temperature characteristics, such as proportional, exponential, or independent [12,20]. It is hard to obtain a temperature dependent or independent current with outstanding linearity even at the cost of power or hardware. Instead of designing a high-linearity and temperature-dependent current generator, this paper adopted a simple current generator since the proposed temperature sensor is independent of $I_{BN}$. Figure 6 shows the architecture of the bias current generator.
As described in Equation (6), $I_{REFP}$ and $I_{REFN}$ can be removed as long as they have the same temperature characteristics and magnitude. Thus, the bias current generator is simply composed of $M_1$-$M_4$. $M_1$ and $M_3$ work in sub-threshold region and provide the source current $I_{ref}$.

$$I_{ref} = \mu \mu_n C_{ox} \frac{W_p W_n}{L_p} (m - 1)V_T^2 \exp\left(\frac{V_{DD} - V_{thn} - V_{thp}}{2mV_T}\right)$$

(10)

where $\mu$ is mobility, $C_{ox}$ is oxide capacitance, $W$ is transistor width, $L$ is transistor length, $m$ is subthreshold slope factor, $V_T$ is thermal voltage ($kT/q$), $V_{th}$ is transistor threshold voltage and $V_{DD}$ is the power supply voltage. The source current is mirrored to Delay_Cell_P and Delay_Cell_N for $I_{REFN}$ and $I_{REFP}$ respectively. According to Equation (6) and Equation (7), $I_{REFP}$ and $I_{REFN}$ should be of equal magnitude. Current mismatch between $I_{REFP}$ and $I_{REFN}$ will deteriorate the temperature linearity. To maintain the same magnitude of $I_{REFP}$ and $I_{REFN}$, the optimal matching among current mirrors ($M_1/M_2/M_6$ and $M_4/M_5$) is required. Thus, the maximum length of 20 $\mu$m is adopted for the current-mirror MOSFETs. The current generator is of simple structure but suffers from the influence of the power supply. Thus, a stable and clean power supply is required.

4.3. Quasi-Static D-Flip Flop

The counters consist of two cascaded dividers (divide by two) which are composed of quasi-static D-Flip Flop for low power consumption (shown in Figure 7). Note that no risk presents in the glitches. The D-Flip Flop adopts dual-feedback loop to remove the impact from leakage. When the counting value of Counter1 reaches $M$, the input clock is blocked, and all dividers in Counter1 and Counter2 stop working and hold the states. Counting value $P$ in Counter2 is output as $T_{code}$ for measurement.

5. Simulation Results

The proposed temperature sensor was designed in 130 nm CMOS process. It does not need external voltage, current and frequency reference. The layout is shown in Figure 8 and the active area
is 0.065 mm². The power supply voltage is 1 V to achieve low power consumption while keeping the
bias current generator working properly under all corners and temperatures. The bias current was set
to 6 nA with oscillation periods about 240 µs under typical corner and room temperature. The average
power is 156 nW at 27 °C while VCO consumes 89%, as shown in Figure 9.

![Figure 8. Layout.](image)

**Figure 8.** Layout.

![Figure 9. Power breakdown.](image)

**Figure 9.** Power breakdown.

### 5.1. VCO Simulation

The proposed VCOs were designed and simulated. Figure 10 shows the simulated results. Since the bias generator works in sub-threshold region, the bias current has exponential relation to
temperature. Accordingly, both VCO periods have exponential relation to temperature as shown in
Figure 10a. Because of the threshold voltage difference between PMOS and NMOS, $T_{VCO,P}$ is larger
than $T_{VCO,N}$. $ratio_T$ is shown in Figure 10b. It is inversely proportional to the temperature with an
outstanding linearity which is in good accordance with the analysis in Equation (7).

![Figure 10. Simulated temperature performance of VCO (a) periods vs. temperature (b) ratio_T vs. temperature.](image)
5.2. Temperature Sensor Simulation

As shown in Figure 10b, \( \text{ratio}_T \) changes slightly over the temperature range of 0 °C to 80 °C. To maintain a 10-bit level resolution, Counter1 is designed to be 14 bits. According to the Monte Carlo simulations, \( \text{ratio}_T \) is always greater than 1 but less than 2, so Counter2 is set to be 15 bits. The proposed temperature sensor is simulated from 0 °C to 80 °C. Both MOSFET mismatches and MIM capacitor mismatch are taken into account and verified with 20 Monte Carlo runs. The standard deviation of the transistors’ mismatch and MIM capacitors’ mismatch are 0.3% and 0.03%, respectively, which are provided by the foundry. Figure 11a shows a temperature error of +1.65 °C /−1.84 °C after 1st order polyfit. Figure 11b shows a temperature error of +0.57 °C /−0.44 °C after 2nd order polyfit.

![Figure 11. Simulated temperature error (a) after 1st order polyfit, (b) after 2nd order polyfit.](image)

The proposed temperature sensor exhibits a systematic error profile dominated by the nonlinearity of \( \text{ratio}_T \) across the temperature range which is in good accordance with the analysis in Equation (7). After 1st order polyfit and the nonlinearity removal (Figure 12a), a maximum temperature error of +0.37 °C /−0.32 °C was observed across a 0 °C to 80 °C temperature range. After 2nd order polyfit and the nonlinearity removal (Figure 12b), a maximum temperature error of +0.17 °C /−0.19 °C was observed.

![Figure 12. Simulated temperature error (a) after 1st order polyfit and systematic nonlinearity removal (b) after 2nd order polyfit and systematic nonlinearity removal.](image)

The proposed temperature sensor was verified under corners. The results are shown in Figure 13. The SS corner shows the best performance while the worst performance can be observed in the FF (Fast-Fast) corner. This is because in the FF corner, the MOSFETs have the lowest threshold voltage. When we increase the reference current, the oscillation period reduces. That results in a worse approximation in Equation (2) and poor linearity.
A CMOS thyristor based temperature sensor was proposed in this paper. Two VCOs composed of CMOS thyristor with different threshold voltage were exploited. The period ratio between two VCOs extracts the temperature information. The ratio calculation is simply realized by two counters where a constant-value counter stops another free running counter. Therefore, the external clock reference was avoided. A diode-connected bias current generator was exploited for its simplicity and little impact on the temperature extraction. The prototype was designed in 130 nm CMOS process and occupies an active area of 0.06 mm². According to the post-layout simulation, it achieves an accuracy of +0.37/−0.32 °C from 0 °C to 80 °C after 1st order polyfit and nonlinearity removal with a power consumption of 156 nW.

### Table 1. Summarizes the performance of the proposed sensor.

|                | [13]  | [12]  | [11]  | [21]  | This Work * |
|----------------|-------|-------|-------|-------|-------------|
| Technology [nm]| 65    | 180   | 180   | 65    | 130         |
| Area [mm²]     | 0.004 | 0.09  | 0.22  | 0.06  | 0.06        |
| Supply Voltage [V]| 0.85–1.05| 1.2  | 1.2   | 1     | 1           |
| External Clock | NO    | NO    | NO    | YES   | NO          |
| Temperature Range [°C]| 0–100 | 0–100 | −20–80| 0–100 | 0 to 80    |
| Resolution [°C]| 0.3   | 0.3   | 0.09  | 0.61  | 0.09        |
| Conversion Time [s]| 22 × 10⁻⁶ | 30 × 10⁻³| 8 × 10⁻³| 10 × 10⁻⁶−1| 3.9         |
| Power [nW]     | 154,000| 71    | 570   | 488.3–0.17| 156        |
| Calibration    | 2-point| 2-point| 2-point| 1-point| 2-point     |
| Inaccuracy [°C]| ±0.9  | +1.5/−1.4| ±0.76 | +1.5/−1.1| +0.37/−0.32 |

* Post layout simulation.

### 6. Conclusions

A CMOS thyristor based temperature sensor was proposed in this paper. Two VCOs composed of CMOS thyristor with different threshold voltage were exploited. The period ratio between two VCOs extracts the temperature information. The ratio calculation is simply realized by two counters where a constant-value counter stops another free running counter. Therefore, the external clock reference was avoided. A diode-connected bias current generator was exploited for its simplicity and little impact on the temperature extraction. The prototype was designed in 130 nm CMOS process and occupies an active area of 0.06 mm². According to the post-layout simulation, it achieves an accuracy of +0.37/−0.32 °C from 0 °C to 80 °C after 1st order polyfit and nonlinearity removal with a power consumption of 156 nW.
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