An amplifier-doubler chain with conversion gain improvement techniques

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Abstract: This paper presents an amplifier-doupler chain to double the signal frequency from 21GHz to 42GHz with about 10GHz bandwidth of output frequency. For the improvement of conversion gain, the doubler adopts the fully differential Gilbert structure which provides large bandwidth and high conversion gain. Meanwhile, an inductive series LC network is used to form resonant tank with the parasitic capacitor to suppress the second harmonic of input frequency, hence the conversion gain of doubler is improved. Once again, the RLC parallel resonant network is employed as load of doubler and power amplifier, and it can improve bandwidth and conversion gain, too. What’s more, transformer matching networks (TMN) are adopted to optimize the bandwidth and conversion gain of amplifier-doupler chain. Finally, the amplifier-doupler chain which fabricated by IBM SiGe 0.13μm BiCMOS technology shows 6.1dB conversion gain and -4.1dBm saturation output power with 26.5mA operating current and 2.8V supply voltage, and the fundamental and 3rd harmonic rejection at 42GHz are 17.5dB and 38.6dB, respectively.

Keywords: Gilbert structure doubler, RLC parallel resonant network.
Classification: Integrated circuits

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1 Introduction

In recent years, millimeter wave (mm-wave) circuits and systems provide excellent opportunity to satisfy the continual increase of demands for higher data rate in wireless communication system. However, it’s difficult to get a low phase noise, high stability, and high power signal source at millimeter-waves frequencies. In general, Nth harmonic oscillators [1-2] and Amplifier Multiplier Chains (AMC) [3-4] are the two most commonly used methods. In AMC, a power amplifier is employed to amplify the signal generated by a low and stable frequency signal source, then the amplified signal is multiplied to high frequency by multiplier. Finally, a stable and high power signal is obtained. Amplifier-doubler chain is one of the main structures of AMC, and the doubler has several kinds of structures. Distributed topology doubler [5] has large bandwidth at expense of low conversion gain and large chip area. Doublers based on passive devices such as diodes [6] and varactors also has low conversion gain, and it is essential to design a high performance power amplifier which provides high power gain and output power. The differential pair of common emitter bipolar structure doubler can get larger output power, but its conversion gain and bandwidth are limited [7]. In this letter, the amplifier-doubler chain with double balanced fully differential Gilbert structure doubler is adopted for its advantage on high gain, high output power and large bandwidth. Furthermore, inductive series LC network and RLC parallel resonant network are employed in the circuit to improve the power gain and output power, and TMNs are adopted to optimize the bandwidth and insertion loss of both the input and output matching network of amplifier-doubler chain.

2 Analysis and design of amplifier-doubler chain
2.1 Analysis and design of power amplifier
As shown in Fig.1, a single stage power amplifier is applied to amplify the 21GHz signal before doubler. The power amplifier employs cascode structure to provide high power gain. Since the amplifier-doubler chain is designed with IBM 0.13μm SiGe BiCMOS technology, all the transistors in the cascode structure adopt the high performance npn transistor with 5μm emitter length, and emitter width of all transistors used in Fig.1 is 0.12μm. It is worth noting that an RLC parallel resonant network is placed between the supply voltage VCC and the collector of Q3/Q4 (in Fig.1). The RLC parallel resonant network not only provides infinite impedance for radio frequency (RF) signal, but also offers direct current (DC) supply voltage with nearly zero DC resistance value by the inductor in the resonant network. As there is almost no RF signal leaked to the power supply from the RLC parallel resonant network, the power gain will be improved. Meanwhile, zero DC resistance can leave larger voltage headroom for the output voltage swing, so the power amplifier exhibits larger output power. Besides, the parasitic capacitances of Q3 and Q4 in Fig.1 are also absorbed into the RLC parallel resonant network, then the bandwidth and power gain of power amplifier are both optimized. A common mode resistor is utilized at the tail of the power amplifier to reject common mode noise. Since the input signal of the amplifier-doubler chain is a single-ended signal, a transformer is adopted to convert single-ended signal to differential signal at the input of the doubler. Besides, the transformer also provides DC bias voltage through its center tap for the amplifier. What’s more, the transformer is employed to make the transformer matching network. By carefully selecting reasonable component values and suitable topology with compact layout, the parasitic components in matching network can be minimized and the loss of transformer matching networks is reduced, so the performance parameters such as power gain, bandwidth of the power amplifier are all optimized.

2.2 Analysis and design of fully differential Gilbert Doubler
Fig.1 shows the adopted fully differential doubler. The frequency doubler is based on Gilbert structure, and the 21GHz output signal of power amplifier is split and fed to the input of switch transistor (Q7-Q10 in Fig.1) as well as to the lower differential pair (Q5-Q6) via DC decoupling MIM capacitors, then the output
signal of the Gilbert structure is doubled to 42GHz. The values of decoupling MIM capacitors C1 and C2 (in Fig.1) which are connected to switch transistors are both 300fF, and the values of decoupling MIM capacitors C3 and C4 in Fig.1 are both 57.9fF. Emitter length of differential pair transistors Q5 and Q6 are 4μm, and emitter length of Q7-Q10 is 2.6μm. What’s worth noting is that the mismatch of transistors and resistors will introduce DC offsets, and mismatch of capacitor and inductor caused by the parasitic of layout will degrade frequency and power performance. So layout of the Gilbert doubler should be strictly symmetrical structure. Meanwhile, an inductive series LC network is employed at the Node A and B of doubler in Fig. 2. The equivalent total parasitic capacitances at common emitter node A and B of the switch transistors are shown in Fig.2. As the frequency

**Fig. 2.** The equivalent parasitic capacitors of the Gilbert doubler which resonate with inductive LC network.

 increases, the common mode impedance at nodes A and B become so small that the second order harmonic of input frequency will not be suppressed; in addition, the parasitic capacitances at nodes A and B will generate a negative resistance at the switch transistor, the negative resistance can cause oscillation either in common mode or differential mode, so the inductive series LC network is necessary to suppress the second harmonic of input frequency and improve the stability of the Gilbert structure doubler. It is assumed that only one transistor is turned on in the switch transistors connected to node A, and the total parasitic capacitance $C_A=C_{be7}+C_{ce5}+C_{bc5}$. Then the $L_{S1}$ is paralleled with $C_A$, in order to isolate the DC current to the ground via $L_{S1}$, a capacitor $C_{S1}$ is connected in series with $L_{S1}$, and the value of capacitor should be a little larger to keep the series connected $L_{S1}$ and $C_{S1}$ to be an inductive network. Then the inductive LC network and $C_A$ forms a parallel LC tank ideally resonating at second harmonic of input frequency. With the application of parallel LC tank, conversion gain is improved by the suppression of second harmonic frequency, and bandwidth is optimized by absorbing the parasitic capacitances into the resonant network. Similar to previous subsection, the RLC parallel resonant network is also adopted in the Gilbert structure doubler. In additional to the aforementioned advantages, the resistor in the resonant network will reduce the output impedance of doubler to make it much easier to match to 50Ω load and improve the bandwidth of output matching
network. With the same consideration as the input TMN of power amplifier, the transformer matching network is employed at the output of doubler, and it adopts a two turns 1:1 stacked transformer for its high coupling efficient. The stacked transformer utilizes the topmost two metal AM and LY to construct the two windings, and the stacked transformer has $65 \mu$m diameter and $6 \mu$m winding width. Besides, as it shown in Fig.1, the inductor and capacitors in the output TMN are used to optimize the matching performance of TMN.

3 Measurement of amplifier-doubler chain

![Fig. 3. (a) Microphotograph of fabricated chip of amplifier-doubler chain. (b) Measured S11 and S22 of the amplifier-doubler chain.](image)

![Fig. 4. (a) Measured conversion gain and output power of amplifier-doubler chain. (b) Measured fundamental and third harmonic rejection of amplifier-doubler chain.](image)

The amplifier-doubler chain is fabricated by IBM 0.13$\mu$m SiGe BiCMOS technology. The microphotograph of amplifier-doubler chain is shown in Fig.3 (a), and the die area of the chip is $1137 \mu$m*1067$\mu$m. Due to the restriction of chip area, the layout has to make a turn to reduce the length of chip. The chip is mounted on printed circuit board, to which supply and bias signals are wire bonded. ZVA40 vector network analyzer and ZVA-Z110E frequency extension module are used to measure the frequency performance and power performance of this work. The measured operating current of amplifier-doubler chain is 26.5mA with 2.8V supply voltage. Fig.3 (b) shows the measured S-parameters, the bandwidths of S11 and S22 defined as being smaller than -10dB are 7.6GHz and 9.4GHz, respectively.
It’s inferred from Fig.4 (a) that the maximum conversion gain is 6.1dB, and the measured saturated output power is -4.1dBm. The fundamental and third harmonic rejection are shown in Fig.4 (b). It is inferred that the fundamental and third harmonic rejection are better than 16.3dB and 29.1dB from output frequency of 36GHz to 48GHz, respectively. At output frequency of 42GHz, the fundamental and third harmonic rejection are 17.5dB and 38.6dB. It is worth noting that the measured power performance in Fig.4 (a) and (b) has been calibrated off the loss of microprobes and cables. The comparison of recently published articles and this work is shown in Table I. It’s inferred that this amplifier-doubler chain shows competitive performance on conversion gain, bandwidth and power consumption when compared with other works.

### Table I. Comparison of published doublers with this work.

| Ref. | [8] | [9] | [10] | [11] | This work |
|------|-----|-----|------|------|-----------|
| Tech. | 90nm CMOS | 0.4μm SiGe HBT | 0.5μm SiGe HBT | 0.8μm SiGe HBT | 0.13μm SiGe BiCMOS |
| Topology | Single-ended | Differential Gilbert structure | Single-ended Gilbert structure | Differential pair of bipolar | Differential Gilbert structure |
| Output Frequency (GHz) | 26.5-28.5 | 18-42 | 14 | 34.6-37.6 | 37-47 |
| Peak Conversion Gain (dB) | 1.5 | 5.6 | 17 | 4.5 | 6.1 |
| Fundamental Rejection (dB) | >11.2 | 22 | 30 | 35 | >16.3 |
| 3rd harmonic rejection (dB) | NA | NA | NA | NA | >29 |
| P_{sat} (dBm) | -1.5 | 0 | -1 | 10.5 | -4.1 |
| Power (mW) | 10 | 185 | 130 | 114 | 74.2 |

### 4 Conclusions

This letter exhibits the design of amplifier-doubler chain with several conversion gain improvement techniques. In the amplifier-doubler chain, power amplifier adopts the RLC resonant network and cascode structure to improve its power gain and output power. For further improvement on conversion gain, the doubler utilizes fully differential Gilbert structure which utilizes inductive LC network to suppress the second harmonic of input signal. Meanwhile, TMNs are employed at the input and output of amplifier-doubler chain to optimize the bandwidth and minimize the insertion loss of passive components. Finally, the amplifier-doubler chain which fabricated by IBM 0.13μm SiGe BiCMOS technology shows 6.1dB conversion gain and -4.1dBm saturated output power. At the same time, the input and output matching networks exhibit 7.6GHz and 9.4GHz bandwidth, and the fundamental and third harmonic rejection are better than 16dB and 29dB, respectively.

### Acknowledgments

Thanks to the test engineers of Rohde&Schwarz Company for their warmly assistances and constructive ideas during the measurement of this work.