INTERLEAVING TECHNIQUES FOR HIGH-THROUGHPUT CHAOTIC NOISE GENERATION IN CMOS

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ABSTRACT: An interleaving technique is proposed to enhance the throughput of current-mode CMOS discrete time chaotic sources based on the iteration of unidimensional maps. A discussion of the reasons and the advantages offered by the approach is provided, together with analytical results about the conservation of some major statistical features. As an example, application to an FM-DCSK communication system is proposed. To conclude, a sample circuit capable of 20 Msample/s is presented.

INTRODUCTION

Interest in the hardware implementation of chaotic systems has recently been boosted by the expectations in fields such as communication systems [8], biologically-inspired computation [4], noise generation, EMI reduction [12], etc. Many applications depend on the existence of pseudo-random data streams of given statistical properties and can directly benefit from chaos-based generators. In fact, the collocation of chaos at the borderline between randomness and causality can be deployed for building extremely simple analog CMOS noise-like sources characterized by small areas and power requirements [3,5]. These are commonly based on discrete time models like the one in Figure 1 [5,6]. Note that for the implementation of the individual building blocks, the current mode approach is currently the best established one. Regrettably, the systems proposed so far exhibit a limited data rate which hinders their applicability. Even with unconventional design optimizations [1], it is difficult to rise data rates over a few MHz.

Herein we propose the addressing of throughput issues by means of hardware resources replication and parallel operation. Particularly, we propose a technique for order-2 concurrency which allows two identical independent chaotic sources to share a large amount of their hardware. The approach is validated by: i. analytical results about major output statistical properties; ii. an application example to an FM-DCSK communication system [8] and iii. the simulation of a sample circuit designed over a conventional 0.8 µm CMOS technology and capable of 20 Msample/s.

ANALOG REGISTER OPTIONS

With reference to the model in Figure 1 and to operating frequencies, one of the most critical sections is the memory which is required for keeping \( x_n \) stable while the map circuit evaluates \( x_{n+1} \). Analog operation is a prerequisite for truly chaotic behaviour, yet this introduces errors in the in-loop signal path which must be kept extremely low as they have an immediate impact on the output statistics of the chaotic source [2]. As expectable, speed-accuracy trade-off do normally exist.

Since the analog memory synchronizes the circuit to an external clock and is never allowed to provide a transparent connection from input to output, its operation is actually as the analog counterpart of a digital register. Just as a digital register, it can be built up of more elementary latching elements, in this case sample-and-hold (SH) or track-and-hold (TH) units. Hence, three main degrees of freedom are allowed to the designer: choice of the reg-
ister architecture, the choice in between TH or SH elements, and the choice of the particular circuit for the SHs or THs. Obviously, the three choices are interrelated.

For what concerns the register architecture and the preference to SHs or THs, it can be noticed that correct operation can be obtained either by cascading TH elements (as shown in Figures 1 and 2), by cascading SH elements (Figure 3), or by having two SH elements operating in anti-parallel (Figure 4). Note that in the current mode operation, one writes:

$$I_{out} = I_{in} + f(I_{in}) + \sigma$$  \hspace{1cm} (1)

where the three addends on the righthandside represent the ideal behaviour, the signal dependent and the signal independent error respectively. Discrete time chaotic circuit are known to be more sensitive to signal dependent errors [2].

In current mode operation, the cascade of two SH (or TH) stages has the property of allowing the cancellation of signal independent errors, as long as the matching among the two stages is sufficiently good. For instance, one can easily arrange things in the spirit of the sample circuit of Figure 5, where:

$$\begin{align*}
I_{out1} &= I_{in} + f(I_{in}) + \sigma \\
I_{in2} &= I_{REF} - I_{out1} \\
I_{out2} &= I_{in2} + f(I_{in2}) + \sigma \\
I_{out} &= I_{REF} - I_{out2}
\end{align*}$$  \hspace{1cm} (2)

Note $I_{REF}$ is a suitably large current, and that the time-indexes $n$, $n-1$ etc. have been omitted for simplicity. The output current is thus

$$I_{out} = I_{in} + g(I_{in})$$  \hspace{1cm} (3)

where $g(I_{in})$ is the overall signal dependent error.

Hence there is an opportunity of selecting SH circuits specially optimized for reducing signal dependent errors, then relying on SH cascading for the reduction of signal independent ones. In this way the signal dependent

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**Figure 2:** Timings of an analog register designed by cascading two TH elements (“T” = track phase, “H” = hold phase).

**Figure 3:** Timings of an analog register designed by cascading two SH elements (keys as in the previous figure, “N/A” = not available).

**Figure 4:** Timings of an analog register designed by operating two SH elements in anti-parallel (keys as in the previous figures).

**Figure 5:** A sample analog register which cancels signal dependent errors exploiting SH cascading.
errors to which chaotic circuits are most sensitive can be addressed at their best, within each SH unit, while less critical signal independent errors can be dealt with at the register level exploiting the SH matching properties. For instance, in [1] it is proposed the adoption of S^21 SHs [7] which have the property of dealing extremely well with signal dependent errors regardless of matching, while leaving a relatively large residual signal independent error.

Because of the signal independent error cancellation property, the cascaded SH analog register architecture is often preferable to the anti-parallel one. Unfortunately, this does normally mean sacrificing the operating speed of the anti-parallel topology. In the following, an interleaving technique is proposed which allows retaining the advantages of both worlds.

**INTERLEAVING**

If two cascaded-SH analog registers are *themselves* connected in anti-parallel, then the topology and the timing diagrams shown in Figure 6 are obtained.

![Figure 6: Timings of an analog register designed by op- diagrams shown in Figure 6 are obtained.](image)

Figure 6: Timings of an analog register designed by operating two whole cascaded-SH analog registers in anti-parallel (keys as in the previous figures).

Note that this architecture provides cancellation of SH signal independent errors. Furthermore, it has the same throughput as the architecture in Figure 4, i.e. a new sample every half clock cycle. The only difference is the associated delay: in the topology of Figure 4 the output is delayed half a clock cycle with regard to input, while in the topology of Figure 6 the delay is a whole clock cycle. This means that if the architecture shown in Figure 6 is substituted for the analog memory in the discrete time system given in Figure 1, still one cannot obtain a chaotic circuit providing a new chaotic sample every half clock cycle. However, **two independent identical** chaotic sources showing interleaved operation can be obtained, as it will be illustrated shortly.

Let us accept that these two systems exist, and name them ‘(A)’ and ‘(B)’. Suppose that the sample \( x_0 \) in Figure 6 corresponds to the initial condition \( x_0^{(A)} \) of system ‘(A)’ and that \( x_1 \) corresponds to the initial condition \( x_0^{(B)} \) of system ‘(B)’. If the clock period is \( T \) and at \( t = 0 \) the analog register outputs \( x_0 \), then from \( t = 0 \) to \( t = T/2 \) the map circuit operates on \( x_0^{(A)} = x_0 \) producing \( x_1^{(A)} = f(x_0^{(A)}) \). At the same time, the analog register samples \( x_2 \), hence \( x_2 = x_1^{(A)} \). From \( t = T/2 \) to \( t = T \) the analog register provides \( x_1 \), causing the map circuit to operate on \( x_0^{(B)} = x_1 \). Thus the map provides \( x_1^{(B)} \) and the register samples \( x_3 = x_1^{(B)} \). From \( t = T \) to \( t = 3/2T \), the register outputs \( x_2 \), i.e. \( x_1^{(A)} \), the map computes \( x_2^{(A)} \), which is in turn sampled as \( x_4 \). From \( t = 3/2T \) to \( t = 2T \), the register outputs \( x_3 \), i.e. \( x_1^{(B)} \) and the map computes \( x_2^{(B)} \) which is sampled as \( x_5 \) and so on.

It is self-evident how two different chaotic trajectories emerging from the same map are kept separated in a time-division fashion. In general terms, the information stored on the interleaved analog register can be related to the state of the chaotic systems as:

\[
x_n = \begin{cases} 
  x_{n/2}^{(A)} & \text{if } n \text{ is even} \\
  x_{(n-1)/2}^{(B)} & \text{if } n \text{ is odd}
\end{cases}
\]

In other words, the SHs marked ‘A’ in Figure 6 store and transfer the state of system ‘A’, while those marked ‘B’ store the state of system ‘B’.

The two systems are obviously independent, since there is no exchange of information among the two. What remains to be seen is if the sequences \( x_n^{(A)} \) and \( x_n^{(B)} \) are themselves independent in a *cross-correlation* sense. What if at startup the initial conditions \( x_0 \) and \( x_1 \) are identical? Being the dynamic chaotic, there is actually no worry about synchronization. In fact, *sensitivity to initial conditions* assures that the trajectories of system ‘(A)’ and ‘(B)’ cannot help rapidly diverging because of the unavoidable mismatch in the initial conditions and the effects of noise. Note that this would be true of any two independent chaotic sources based on the same map, yet this arrangement is particularly convenient, as it allows to realize two identical chaotic sources while sharing a large part of their hardware (the whole map circuit) and to obtain an output sample every half clock cycle.

At this point, it is interesting to consider the statistical properties of the interleaved sequence at the output of the analog register, and to verify whether they can be useful to some applications.

If we consider the sequence \( x_n \), its probability density function (PDF) is of course the same as that of \( x_n^{(A)} \) or \( x_n^{(B)} \). Hence, interleaving does not influence the first order statistics. On the contrary, the autocorrelation is obviously affected. In fact we have:

\[
\Phi_{x,x}(n) = \begin{cases} 
  \Phi_{x^{(A)},x^{(A)}}(n/2) & \text{if } n \text{ is even} \\
  \mu^2 & \text{if } n \text{ is odd}
\end{cases}
\]

where \( \mu \) is the average (or DC component) of the sequences \( x_n^{(A)} \) and \( x_n^{(B)} \), that we shall assume to be zero for simplicity. If we take the Fourier transform of the autocorrelation we obtain the power density spectrum, resulting in:

\[
X(j\omega) = \sum_{n=-\infty}^{\infty} \Phi_{x,x}(n)e^{-j\omega Tn}
\]
which can be rewritten as
\[
X(j\omega) = \sum_{n=-\infty}^{\infty} \Phi_{x,t}(n) e^{-j\omega T_n} + \\
+ \sum_{n=-\infty}^{\infty} \Phi_{x,t}(n) e^{-j\omega T_n} = \\
= \sum_{m=-\infty}^{\infty} \Phi_{x,t}(2m) e^{-j\omega T_{2m}} \\
= \sum_{m=-\infty}^{\infty} \Phi_{x,t}(2m) e^{-j\omega T_{2m}} = X(A)(j\omega)
\]

where \( T \) is the clock period. Hence, being a periodic function, the power density spectrum is not affected. Higher order moments, which are harder but not impossible to compute, are generally all affected, but they have a lower impact on typical applications.

**APPLICATION EXAMPLE**

In order to show an example in which an interleaved chaotic source is adopted instead of a traditional one, we shall consider an FM-DCSK communication system [9, 10]. In an FM-DCSK modulator, a discrete time uniform PDF random/chaotic source is used as the input to an FM modulator. In this way a spread-spectrum band-pass carrier is obtained to be fed to a further DCSK modulator, as shown in Figure 7. Ideally the spread spectrum carrier should be characterized by a bandwidth limited to an interval and by a uniform power density spectrum over that interval.

In practice, it is common to use chaotic models where particular strategies are adopted to enhance the implementation robustness. An example is offered by tailored tent map (TTM) systems [3], such as:

\[
x_{n+1} = 1 - 2|x - (1 - \theta)/2| + \max(x - 1 + \theta, 0) \quad (8)
\]

where \( \theta \) is a control parameter in \((0, 1/2)\) usually taken very close to zero. By adopting a TTM chaos generator \((\theta = 0.05)\) the FM-DCSK signal spectrum is modified as shown by the bottom left plot in Figure 8.

Finally, the bottom right plot shows the spectral properties of a DCSK signal generated using an interleaved TTM based chaotic source. In this case not only the applicability of the interleaving technique is verified: a slightly better behaviour is also obtained. This improvement is due to the effects of the interleaving technique on the higher order moments of the chaotic process. However note that the impact on the overall behaviour of a complete FM-DCSK system is almost negligible. However, the possibility of using an interleaved source is extremely interesting, since it allows to design chaotic sources capable of reaching the data rate requirements of FM-DCSK modulators. As a reference value, consider that typical systems designed so far require 20 Msample/s.

**SAMPLE CIRCUIT**

In order to show the effectiveness of the proposed technique, a sample circuit has been designed and simulated.
For this testing a well established 0.8 µm CMOS technology has been adopted. The circuit has been designed to reach an output data rate sufficient for the FM-DCSK application illustrated above.

The schematic that we illustrate is based on [1], where $S^2I$ dynamic mirrors [7] are used for enhanced speed and accuracy. The TTM is chosen as the system nonlinear function.

The map circuit is shown in Figure 9. Note that it requires two identical input currents to perform concurrently the comparisons necessary to evaluate the relative position of the input and the breakpoints. For this evaluation active circuits are used, so that the main feature of the circuit is that the voltage at the inputs can be kept almost constant. In [1], a convenient way is suggested to make this voltage $V_R$ generally available by means of a dummy rectifier. This allows to use $V_R$ in other parts of the circuit, for instance to connect the wells of M5 and M10, cancelling the body effect and improving performance.

Reference currents $I_{R1}$ and $I_{R2}$ are set respectively to $-2.5$ and $45$ µA and set the breakpoint positions ($\theta = 1/20$). Currents $I_{B1}$ and $I_{B2}$ (2.5 µA) speed up signal processing by never allowing mirrors to operate on null currents. Finally, $I_{ADJ}$ (57.5 µA) fixes the output offset and sets the system invariant set to $[-50, +50]$ µA. Current mirrors are all high swing cascode and gate areas of transistors that could introduce matching errors are always non-minimal (typically > 40 µm²).

The analog delay is shown in Figure 10. This already comprises two interleaved memory units, each of them built up of two $S^2I$ dynamic current mirrors [7]. The clocking scheme is as for a typical $S^2I$ system and the unit embeds mirroring to provide currents to both the map circuit inputs and the chaotic system output. For convenience in Figure 10 the two interleaved analog memories are distinguished by the postfixes “a” or “b” applied to all the relevant devices, while the many switches are named Sxxx.

Note that (as pointed out in [1]) for correct interfacing to the map circuit, the voltage $V_R$ mentioned above must be used as the reference voltage for the $S^2I$ dynamic mirrors in order to exploit the low input impedance of the map unit (in the figure, $V_R$ is simply a buffered version of $V$). This circuit ideally propagates the state variables without introducing signal dependent errors, which is an important condition for the accurate operation of the chaotic system. Only the output variable is subject to a non-negligible sampling error, which is an offset and thus easy to deal with.

Figure 11 shows the evolution of the output variable when the system is simulated using SPICE with accurate analog device models (BSIM 3). The output data rate is 20 Msample/s.

The observation of longer sequences has shown that the unavoidable coupling among the two interleaved chaotic systems due to circuit parasitic does not produce perceivable effects such as synchronization. Direct estimation of statistical properties from spice data has proven hard, due to the inefficiency of SPICE time-step algorithms when dealing with $S^2I$ circuits. In practice, it has not been possible to obtain long enough sequences for reliable statistics estimation. Nonetheless, a mix of Spice and behavioural simulations has allowed to obtain the plots in Figures 12 and 13. The first refers to the probability density function and the second to the power density spectrum of the state variable which is propagated through the analog register.

**Figure 11: The system output current as simulated by SPICE.**

**Figure 12: Estimation of the analog register variable $x_n$ PDF for the presented circuit.**

**CONCLUSIONS**

In this paper, the use of an interleaving technique applied to discrete time chaotic sources has been proposed. Its feasibility has been analytically shown and the usability of the so obtained chaotic sources for a sample application (FM-DCSK communication) has been verified by simulations at the model level.

To validate the possibility of exploiting the proposed technique at the hardware level, a CMOS circuit has been
designed using a conventional 0.8 \mu m technology. As far as simulations have been ran, the circuit has shown operation in accordance with the expected behaviour. Some data is still lacking about the estimation of the spectral properties of the hardware interleaved chaotic generator. Currently work is in progress, both in order to obtain good estimation of the statistical properties of the system directly from circuit simulation and to evaluate the usability of interleaved chaotic sources to other application fields.

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