Miniaturized high-frequency sine wave gating InGaAs/InP single-photon detector

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High-frequency gating InGaAs/InP single-photon detectors (SPDs) are widely used for applications requiring single-photon detection in the near-infrared region such as quantum key distribution. Reducing SPD size is highly desired for practical use, which is favorable to the implementation of further system integration. Here we present, to the best of our knowledge, the most compact high-frequency sine wave gating (SWG) InGaAs/InP SPD. We design and fabricate an InGaAs/InP single-photon avalanche diode (SPAD) with optimized semiconductor structure, and then encapsulate the SPAD chip and a mini-thermoelectric cooler inside a butterfly package with a size of 12.5 mm × 22 mm × 10 mm. Moreover, we implement a monolithic readout circuit for the SWG SPD in order to replace the quenching electronics that is previously designed with board-level integration. Finally, the components of SPAD, monolithic readout circuit and the affiliated circuits are integrated into a single module with a size of 13 cm × 8 cm × 4 cm. Compared with the 1.25 GHz SWG InGaAs/InP SPD module (25 cm × 10 cm × 33 cm) designed in 2012, the volume of our miniaturized SPD is reduced by 95%. After the characterization, the SPD exhibits excellent performance with a photon detection efficiency of 30%, a dark count rate of 2.0 kcps and an afterpulse probability of 8.8% under the conditions of 1.25 GHz gating rate, 100 ns hold-off time and 243 K. Also, we perform the stability test over one week, and the results show the high reliability of the miniaturized SPD module.

I. INTRODUCTION

Single-photon detectors (SPDs) have the ultimate sensitivity for weak light detection, and thus are widely used in numerous applications such as quantum key distribution (QKD), lidar and photoluminescence. Currently, the primary SPD technologies in the near-infrared region include superconducting nanowire single-photon detector (SNSPD)¹, up-conversion single-photon detector² and InGaAs/InP single-photon avalanche diode (SPAD)³, among which InGaAs/InP SPAD is preferred in practical applications due to the advantages of small size and low cost. In InGaAs/InP SPDs, SPADs are operated either in free-running mode or gating mode. Free-running mode is a natural method for single-photon detection, and particularly suitable for the applications with unknown photon arrival times. So far, diverse techniques have been reported to implement free-running InGaAs/InP SPDs.⁴,⁵,⁶ However, the SPD count rates in these schemes are considerably limited, due to the fact that long hold-off time has to be applied to suppress the afterpulsing effect.

High-frequency gating technique, including sine wave gating (SWG)⁷,⁸ and self-differencing⁹, provides a practical approach to significantly increase SPD count rate, which is highly desired in applications requiring high detection rate. For instance, in QKD applications secure key rate is roughly proportional to system clock rate, so that using high-frequency gating InGaAs/InP SPD can substantially improve QKD performance. In the high-frequency gating scheme, gating rate usually reaches a gigahertz level and the avalanche duration time is limited to a few hundred picoseconds, which effectively suppresses the charge carrier quantity of avalanche and thus, the afterpulse probability. As a consequence of ultra-short gating time, the avalanche signals become pretty weak, i.e., at the level of mV. Therefore, the key challenge in high-frequency gating scheme is to extract weak avalanche signals from the large capacitive response signal.¹⁰

Concretely, in the SWG scheme, sine waves with large amplitude are gated on an InGaAs/InP SPAD. Due to the pure and simple frequency spectrum of sine waves, the capacitive response signals from the SPAD only include the fundamental frequency and higher-order harmonics of sine waves, which can be easily eliminated by filters. After filtering, the weak avalanche signals are amplified and then discriminated. So far, many groups have reported the implementations of SWG schemes with InGaAs/InP SPAD¹¹,¹²,¹³ and even silicon SPAD.¹⁴,¹⁵ For practical applications, integration implementation of SPD is crucial. For instance, in 2012 Liang et al. reported a board-level integrated SWG InGaAs/InP SPD with a gating rate of 1.25 GHz and a size of 25 cm × 10 cm.
II. MINIATURIZED SPD DESIGN

A. Design and fabrication of InGaAs/InP SPAD

We follow the method to design an InGaAs/InP SPAD with separate absorption, grading, charge, and multiplication (SAGCM) structure as illustrated in Fig. 1. Further, we combine the semiconductor structure optimization, particularly for InGaAs absorption layer, InP electric field control layer and InP multiplication layer, and fabrication process control to improve the performance of key SPAD parameters including PDE, DCR, afterpulse probability and timing jitter. By tuning the doping concentration in the electric field control layer, the electric field distributions in the InGaAs absorption layer and the InP multiplication layer are well controlled, which can also reduce the timing jitter of the SPAD chip.

In the absorption layer, on one hand the electric field strength should be as low as to avoid avalanche breakdown, and on the other hand the electric field strength should be as high as to maintain the saturation avalanche drift rate of the photogenerated hole carriers. Then, the electric field strength in this layer is compromised at the range of $1 \sim 1.4 \times 10^5$ V/cm. In the multiplication layer, properly decreasing the thickness can reduce the transit time of carriers and thus the timing jitter whilst maintain the enough electric field strength for avalanche breakdown. The multiplication layer thickness is controlled at the range of $1 \sim 1.5$ µm. In the PN junction, a ladder structure is designed, which can be formed using double-diffusion process technology. Such structure has several advantages, i.e., reshaping the electric field distribution of the junction, suppressing the marginal effect of electric field due to curvature, creating uniform electric field in the central zone of the PN junction, and reducing the high electric field regions at the edge of the PN junction and thus the afterpulse probability. Moreover, a floating guard ring is designed to absorb carriers outside the active region, which can help reduce DCR and improve the response time of SPAD chip.

The SPAD chip is fabricated using the standard epitaxial process of metal-organic chemical vapour deposition (MOCVD). During the process, the background impurity concentration of the epitaxial material reaches as low as $2 \times 10^{14}$/cm$^3$, whilst the error of surface charge density in the electric field control layer is controlled at 5%. After the diffusion with a Zn source, the error of depth difference between the first and the second P-doping processes is controlled at 50 nm, and finally a central PN junction with a diameter of 25 µm is formed in the multiplication layer.

We then characterize the chip before packaging at room temperature, as shown in Fig. 2. Fig. 2(a) plots the current-voltage (I-V) curves with and without light illumination, from which one can observe that the punch-through and breakdown ($V_{br}$) voltages of SPAD chip are 38.6 V and 65.9 V, respectively. With a reverse bias voltage of $V_{br} - 1$ V, the total dark current of SPAD chip is as low as 0.2 nA, which is primarily contributed by the surface dark current. Fig. 2(b) plots the capacitance-voltage (C-V) curve, in which the capacitance of SPAD chip decreases rapidly with bias voltage less than $\sim 5$ V and then decreases slowly as bias voltage increases. When the SPAD is operated in Geiger mode, the capacitance of SPAD chip is $\sim 0.13$ pF.

In order to further calibrate the light response of SPAD chip, we perform a full two-dimensional photocurrent-position scan using a point light source of 5 µm spot size with a position step of 2 µm and a bias voltage of $V_{br} - 1$ V, as shown in Fig. 2(c). When the light source is located to the center of active region, the photocurrent generated by the SPAD chip is largest. As the light source moves towards the edge of active region, the photocurrent drastically decreases. When the light source
illuminates on the N-contact metal layer outside the active region, the photocurrent approximates to zero. This indicates that the double-diffusion process successfully realizes high electric field in the central region of the PN junction whilst effectively suppresses the electric field of the marginal region in the multiplication layer.

After the calibration, the SPAD chip is encapsulated inside a butterfly package (12.5 mm × 22 mm × 10 mm) along with a mini-thermoelectric cooler (TEC). The SPAD chip is fixed on the cold side of TEC and then fiber pigtailed. The hot side of TEC is soldered on the bottom of the metal box for heat dissipation. The operation temperature of SPAD chip is monitored via a negative temperature coefficient thermistor very close to the chip.

B. MIRC

In the readout circuit of SWG scheme, either band-stop filters (BPFs) or low-pass filters (LPFs) are used to eliminate the capacitive response signals, and a low-noise amplifier (LNA) is used to amplify the avalanche signals. Here we implement a monolithic read-out circuit with a size of 15 mm × 15 mm, and the details of the MIRC can be found in Ref. 23. Two LPFs and a two-stage LNA are integrated inside the MIRC chip, which is fabricated using the technology of low temperature co-fired ceramics (LTCC).

LTCC is a standard integration and fabrication technique for radio frequency miniaturized components. During the LTCC process, via holes are punched into ceramic tapes and filled with silver paste for electrical connections between layers, and the circuits are printed onto the tapes. Then the tapes are stacked, laminated and cut in a sequential order, to form a desired shape. Finally, the silver paste and ceramic tapes are co-fired together at 900 °C.

The MIRC chip is then tested using a network analyzer, and exhibits excellent ratio frequency performance with a gain of ~40 dB below 1 GHz and a rejection ratio of ~80 dB at 1.25 GHz. This result indicates that the MIRC chip can effectively filter out the capacitive response signals in the SWG scheme with a gating frequency of 1.25 GHz and extract weak avalanche signals.

C. SPD Module

We then integrate the SPAD component, MIRC and the affiliated circuits together to implement a miniaturized 1.25 GHz InGaAs/InP SWG SPD. In Fig. 3(b), we show the design diagram of the miniaturized 1.25 GHz InGaAs/InP SWG SPD. (c) Typical avalanche signal at the output of MIRC captured by an oscilloscope with 8 GHz bandwidth.

FIG. 3. The design diagram (a) and photo (b) of the miniaturized 1.25 GHz InGaAs/InP SWG SPD. (c) Typical avalanche signal at the output of MIRC captured by an oscilloscope with 8 GHz bandwidth.
Apart from DCR, the afterpulse probability is another noise source of SPD that is related to other parameters and readout circuits. During the characterization, with the pulsed laser illumination the detection event distribution is first recorded by the TDC. Fig. 5(a) illustrates a typical histogram of detection event distribution under the conditions of 20% PDE, 243 K and 100 ns hold-off time. The main peak corresponds to the photon detection counts, and the subsequent decay of detection events is attributed to afterpulse counts. The sudden increase of detection events at 120 ns in Fig. 5(a) is due to the effect of hold-off time. From the detection event distribution $P_{ap}$ is calculated after subtracting the DCR contribution.

Fig. 5(b) plots $P_{ap}$ as a function of PDE. At 243 K and 30% PDE, $P_{ap}$ is 8.8%. As temperature increases to 253 K and 263 K, with the same PDE $P_{ap}$ decreases to 7.1% and 6.4%, respectively. One can further normalize the $P_{ap}$ values for comparison. For instance, at 243 K and 30% PDE, $P_{ap}/ns$ is 8.8% / (5.3 $\mu$s × 176 ps/800 ps) $\sim$ 7.5 × 10$^{-5}$/ns, where 5.3 $\mu$s is the average time interval between photon detection events and 176 ps is the measured effective gating width. Such normalized value is around 8 times higher than the normalized DCR parameter, i.e., 2.0 kcps / (176 ps/800 ps) $\sim$ 9.1 × 10$^{-6}$/ns.

Finally, we perform the stability test over one week for the miniaturized SWG SPD module by monitoring two key parameters including PDE and temperature. Fig. 6 depicts the test results. During the test, the SPD module is connected with a computer via RS-232 serial port. PDE is initially set to $\sim$ 20%. The values of detection count and temperature are recorded every second. Every 5 minutes, the SPD runs a full scan for the PS during 30 seconds to optimize the relative delay between sine wave gates and laser pulses. The two straight lines in Fig. 6 clearly indicate the stability of the miniaturized SWG SPD module, which can be ready for practical use.

**III. SPD CHARACTERIZATION**

The miniaturized SWG SPD module is characterized using the standard calibration method$^4$. A signal generator outputs synchronized signals, including 10 MHz signal for the reference clock of SPD and 625 kHz signal for triggering the pulsed laser and the time-to-digital converter (TDC). The laser pulses with a width of $\sim$ 100 ps are divided by a 99:1 beam splitter. The 99% port is monitored by a power meter in real-time, and the pulses from the 1% port enter into an optical variable attenuator to further attenuate the intensity down to a level of mean photon number per pulse of 1. The detection outputs of SPD are used as “stop” signals of TDC, from which the key parameters of PDE, DCR and $P_{ap}$ can be measured.

PDE and DCR are intrinsic parameters of SPAD, which are independent from the readout circuits. Fig. 4(a) plots DCR as a function of PDE at 243 K, 253 K and 263 K, respectively. For a Poissonian light source, PDE is calculated by\[ PDE = \frac{1}{\mu} \ln \frac{1 - DCR/f_g}{1 - R_{ph}/f_l}, \] where $\mu$ is the mean photon number per laser pulse, DCR is the measured count rate without laser illumination, $f_g$ is the gating frequency, $f_l$ is the frequency of laser pulses, and $R_{ph}$ is the photon detection count rate with laser illumination, i.e., the coincidence rate between detections and laser pulses with the subtraction of DCR contribution. As plotted in Fig. 4(a), the SPD exhibits excellent performance, e.g., at PDE of 30% DCR reaches as low as 2.0 kcps.

Effective gating width is an important parameter related to charge carrier quantity of avalanche, which is measured by scanning the relative delay between laser pulses and sine wave gates. For instance, as fitted in Fig. 4(b), the effective gating width is 138 ps full width at half maximum (FWHM) at 20% PDE and 243 K. Such low value can significantly suppress the afterpulsing effect.$^4$

**IV. CONCLUSION**

In conclusion, we have reported, to the best of our knowledge, the most compact SWG InGaAs/InP SPD with 1.25 GHz gating frequency. We have designed and fabricated a high-performance InGaAs/InP SPAD component integrated with a mini-thermoelectric cooler.
Further, we have implemented a monolithic readout circuit for the SWG scheme. With the help of the miniaturized SPAD component and the monolithic readout circuit, the SPD module has been integrated within a size of 13 cm × 8 cm × 4 cm. Compared with the board-level integrated SPD designed in 2012, such size has been reduced by 95%. The SPD exhibits excellent performance with 30% PDE, 2.0 kcps DCR and 8.8% afterpulse probability at 243 K and 100 ns hold-off time, and stability test results show that the miniaturized SPD module can be used in practical applications. Our work paves the way to implement the miniaturization of high clock rate QKD system in the future.

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