A Novel Modeling and Control Design of the Current-Fed Dual Active Bridge Converter under DPDPS Modulation

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Abstract—This paper proposes a novel control design for a Current-Fed Dual Active Bridge (CFDAB) converter in boost mode. The Double PWM plus Double Phase Shifted (DPDPS) modulation is applied to the converter due to its considerable merits. A small-signal model is developed to control the output voltage stably in boost mode. Simulations of the control design for the CFDAB converter were conducted to verify the proposed model. The results show that the system can achieve high performance, not only in the dynamic response but also in the steady-state.

Keywords—Current-Fed Dual Active Bridge (CFDAB) converter; small-signal model; Double PWM plus Double Phase Shifted (DPDPS) modulation

I. INTRODUCTION

Nowadays, the growth in renewable power systems urges researchers and engineers to solve the problems of managing integrated storages and exchange powers to enhance overall system efficiency. In order to connect the battery at low voltage to the DC link at high voltage in a storage system, the utilized DC/DC converter needs to have a high gain voltage factor and an ability of bidirectional transferring power. The DC/DC converters can be classified as isolated and non-isolated. Between these two, the isolated DC/DC converter is highly recommended for its high reliability. It is able to eliminate current leakage in the system. This undesired current is the cause of EMI, additional loss, and unsafe installation and operation [1]. Another advantage of the isolated DC/DC converter is that the flexible gain ratio can be obtained by using a high frequency transformer [2, 3]. The Dual Active Bridge (DAB) converter belongs to the isolated DC/DC type and is well-known for its advantages of high frequency operating ability, inherit zero voltage switching, and bidirectional power flow [4-6]. The structure of the DAB can have modified flexibly with different power sources [7-8]. The DAB converter is divided into two categories: Voltage-Fed (VFDAB) and Current-Fed (CFDAB). When using the VFDAB structure in a variety of applications [9-11], the voltage source is directly supplied to the converter, which produces high current ripple and becomes large and costly. Besides, the VFDAB needs a bulky capacitor in series-connection with the primary coil to avoid the flux saturation of the transformer [11]. Therefore, the CFDAB structure is used to deal with these problems, the input interleave boost inductors in CFDAB help to decrease the current ripple significantly, and ZVS can be achieved for all switches over a wide range of load [9-12].

On the other hand, a small-signal model needs to be built for the accurately controlling problem. Naturally clamped CFDAB modeling structure has been introduced in [13, 14]. Besides, a state-space model under SPSPWM modulation for interleaved boost CFDAB structure is mentioned in [15]. In the current research, DPDPS modulation technique in comparison with SPSPWM modulation [9] is applied, and a small-signal model to regulate the output voltage is built up in boost mode. The simulation results show the effectiveness of the proposed method.

II. RESEARCH METHOD

A. Operation Principles and Control Structure

1) Operation Principles

The applied structure of CFDAB converter in this research is presented in Figure 1, which consists of 2 main parts: the interleaved boost part and the dual active full-bridge part. In the interleaved boost part, two DC inductors are considered as two current research, DPDPS modulation technique in comparison with SPSPWM modulation [9] is applied, and a small-signal model to regulate the output voltage is built up in boost mode. The simulation results show the effectiveness of the proposed method.
The voltages of the clamp capacitor and the output capacitor are assumed as the Low-Voltage Side (LVS) and High-Voltage Side (HVS). The bidirectional transfer power between the LVS, the HVS, and the power flow are determined by the phase shifted angle. The AC inductor $L_r$, which is the sum of the primary-referred transformer leakage inductor, which can be considered as a power link between the two sides of the converter.

2) Modulation Strategy

Due to the high amount of switch devices and inductors, the modulation strategy for the converter needs to be considered before designing the control loop. To handle the voltage ratio variation problems and to minimize the conduction loss in power transfer stages, the PWM plus Phase Shifted (PPS) is introduced while the duty cycle for HVS switches is equal to 50% and the duty ratio for the main LVS switches $Q_1, Q_2$ is a variable $D$. However, in the non-power transfer stage of PPS, the circulation loss is significant with high leak current spike. An additional phase shifted in Double PWM plus Double Phase Shifted (DPDPS) method [9], which equals to $(2D-1)\times T_s / 2$, is applied to eliminate the leak current spike. Figure 2 illustrates the modulation rule of the CFDAB converter, where the phase shifted between $Q_1 - Q_2, Q_2 - S_1$ and $S_1 - S_4$ are 180˚, $\varphi_1$ and $\varphi_2$ respectively. The value of $\varphi_e$ determines the power flow and direction, where $\varphi_e > 0$ represents the operation boost mode with power flow from LVS to HVS and vice versa. By utilizing DPDPS modulation, 8 operation modes in one switching period along with leakage current waveforms, the switching LVS voltage and the transformer voltage waveform $v_{cd}$ are displayed in Figure 3 [9].

3) Control Structure

For CFDAB converter structure, the transfer power is related to the clamp voltage $V_c$ and the phase shifted $\varphi_e$ between the two H-bridges. Therefore, the control structure in boost mode has to control the voltage of the clamp capacitor and the output capacitor simultaneously. There are two pairs of control variables: $V_c$ and $\varphi$, as presented in Figure 4.

B. Small Signal Modeling

It is required to determine the transfer functions of the two pairs of control variables mentioned above so that the control scheme in Figure 4 can be implemented. The transfer function perturbations between clamp voltage $\hat{v}_c$ and duty ratio $\hat{d}$ is depicted in (1) [9]:

$$
\frac{\hat{d}}{\hat{v}_c} = \frac{K_{d/c}}{1 + \lambda s}.
$$
\[ G_{\text{c.e}} = \frac{\dot{\psi}}{d} = \frac{2V_o \varphi - oL_c (I_{d1} + I_{d2})}{\omega L_c s + 2\varphi (1 - D)} + \frac{\varphi}{2\pi} \] (1)

In this paper, the small signal model along with the closed loop controller is proposed to regulate the output voltage of the converter under DPDPS modulation. In the secondary side, the output capacitor is charged and discharged in power transfer and non-power transfer stage respectively. From the switching sequence in Figure 3, the time interval of each switching mode is given by:

\[
\begin{align*}
  d_1 &= d_1 = d_2 = d_3 = d_4 = \frac{\varphi}{2\pi} \\
  d_4 &= d_5 = 1 - d_6 \\
  d_6 &= \frac{2d_1 - 1 - \varphi}{2\pi}
\end{align*}
\] (2)

The relationship between small signals of variables is presented in Table I for 8 modes in one DPDPS switching period. The inductors and capacitors are considered as ideal, i.e. the internal resistors are neglected. The continuous-time equation of output voltage is defined as:

\[
C_0 \frac{dV_o}{dt} = N (d_4 - d_1) \left( \frac{V_c}{\omega L_r} \right) \varphi
\]  
\[+ (-d_1 + d_3 + d_4 - d_4 + d_6 + d_7 - d_7) \frac{V_o}{R}
\]
\[+ Nd_5 \left( \frac{V_c}{\omega L_r} \right) (\pi - \theta_1 + \phi) - Nd_5 \left( \frac{V_c}{\omega L_r} \right) (\theta_1 - \phi)
\] (3)

Using the average model:

\[
\theta_1 = 2d_1 + \frac{\varphi}{2}, \theta_5 = (2d_1 - 1)\pi + \frac{\varphi}{2}
\]

we can obtain:

\[
C_0 \frac{dV_o}{dt} = N \left( d_4 - d_1 \right) \left( \frac{V_c}{\omega L_r} \right) \varphi + N \left( d_2 + d_3 \right) \left( \frac{V_c}{\omega L_r} \right) \varphi
\]
\[+ (-d_1 + d_3 + d_4 - d_4 + d_6 + d_7 - d_7) \frac{V_o}{R}
\] (4)

Replacing (2) to (4) we get:

\[
C_0 \frac{dV_o}{dt} = \left( 4d_4 - 3 \right) \frac{V_o}{R} + N \left( \frac{-\varphi^2}{2\pi} + 2\varphi (1 - D) \right) \frac{V_c}{\omega L_r}
\] (5)

Using the perturbations of duty ratio, phase-shifted angle output voltage, and clamp voltage we have:

\[
C_0 \frac{d(V_o + \hat{V})}{dt} = \left( 4D + \hat{d} - 3 \right) \left( V_o + \hat{V} \right) +
\]
\[+ N \left( \frac{-\Phi + \hat{\phi}}{2\pi} + 2\Phi + \hat{\phi} (1 - D + \hat{d}) \right) \frac{V_o + \hat{V}}{\omega L_r}
\]

Discarding the steady-state value and the second order perturbations and assuming that \( \dot{\hat{d}} = \hat{V}_c = 0 \) we get:

\[ C_0 \frac{dV_o}{dt} = (4d - 3) \frac{V_o}{R} + N \left( \frac{-\varphi^2}{2\pi} + 2\varphi (1 - D) \right) \frac{V_c}{\omega L_r} \] (7)

By Laplace transformation, the transfer function from \( \hat{v}_c \) to \( \hat{\phi} \) in the frequency domain can be expressed as:

\[ \frac{G_{c.e}}{R} = \frac{N R V_D (2 - 2D \frac{\Phi}{\pi})}{\omega R L_c s^2 - \omega R L_c (4D - 3)} \frac{A}{B s + C} \] (8)

### Table I: Small Signal Model in Each Switching Mode

| Mode | Continuous-time equations |
|------|---------------------------|
| Mode I | \( C_0 \frac{dV_o}{dt} = -\frac{V_o}{R} - N_{d1}, i_o = \left( \frac{V_c}{\omega L_r} \right) (\theta - \phi) \) |
| Mode II | \( C_0 \frac{dV_o}{dt} = -\frac{V_o}{R} - N_{d1}, i_o = 0 \) |
| Mode III | \( C_0 \frac{dV_o}{dt} = \frac{V_o}{R} - N_{d2}, i_o = \frac{V_c}{\omega L_r} (\theta - (2d - 1)\pi) \) |
| Mode IV | \( C_0 \frac{dV_o}{dt} = \frac{V_o}{R} - N_{d3}, i_o = \frac{V_c}{\omega L_r} (\pi - \phi) \) |
| Mode V | \( C_0 \frac{dV_o}{dt} = \frac{V_o}{R} - N_{d4}, i_o = \frac{V_c}{\omega L_r} (\pi - \phi) \) |
| Mode VI | \( C_0 \frac{dV_o}{dt} = \frac{V_o}{R} - N_{d5}, i_o = 0 \) |
| Mode VII | \( C_0 \frac{dV_o}{dt} = \frac{V_o}{R} - N_{d6}, i_o = -\frac{V_c}{\omega L_r} (\theta - 2\pi) \) |
| Mode VIII | \( C_0 \frac{dV_o}{dt} = \frac{V_o}{R} - N_{d7}, i_o = -\frac{V_c}{\omega L_r} (\theta - \phi) \) |

### C. Simulation Verification

The control design with the proposed method is firstly verified by simulation in Matlab/Simulink (Figure 5). The specifications of the converter are given in Table II and the transfer function in frequency domain between \( \hat{V}_c \) and \( \hat{\phi} \) is turned into:

\[ G_{c.e} = \frac{\hat{V}_c}{\hat{\phi}} = \frac{A}{B s + C} = \frac{1.643 \times 10^4}{0.3213 s + 4.7} \] (9)

A PI controller is applied to regulate the output voltage:

\[ G_c = K_r (1 + \frac{1}{Tis}) \] (10)

where \( T_i \) is equal to the pole of \( G_{c.e} \): \( T_i = \frac{B}{C} = 0.068 \).

The output voltage close loop transfer can be written as:

\[ G_i = \frac{1}{T_is + 1} \] (11)
with $T_i = \frac{B}{A*K_p}$. By choosing $T_i = 5*10^{-4}$, $K_p = 0.276$.

The simulation scenario consists of 4 steps: the clamp capacitor is charged from 0 to 0.2s, at 0.2s the $V_c$ controller starts and the LVS switches are enabled, at 0.25s the $V_o$ controller starts and in the final step, the load changes suddenly to the nominal value. Figures 6, 7 show the simulation results of clamp and output voltage respectively. As can be observed, in the start-up period, the voltages of the two capacitors are charged and controlled to increase gradually as well as track the reference values with negligible error and no over-shoot.

Furthermore, the currents through the boost inductor and the leakage inductor with little spike in the start interval which ensure the feasibility of the control design in the experiment, are shown in Figures 8 and 9. The clamp voltage and the out voltage decrease slightly, about 3V, at 0.45s when the nominal load is changed. After that, they quickly return to the reference value within 0.01s and 0.03s. In steady-state operation, the voltages on both the LVS and HVS side of the transformer along with leakage current are shown in Figure 9. Due to the
small difference between the reference of clamp voltage and the output voltage, the bias current in the leakage current helps HVS switches achieve the ZVS easier [16]. In addition, the switches voltage and current are presented for $S_1$ and $Q_2$ in Figures 10 and 11.

III. CONCLUSION

The current paper presents the control structure along with the modeling of the CFDAB converter in boost mode. A small signal model is built up with the chosen modulation technique to control the output voltage of the converter. Simulations were carried out to verify both the proposed model and the control design. The simulation results prove the good performance of the control design not only in the steady-state but also in the dynamic responses.

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