Improvement of chip design to reduce resonances in subgap regime of Josephson junctions

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Abstract. Excess current peaks in the IV curves of SIS Josephson junctions have been observed by some groups [1–3]. These peaks have the shape of a resonance as a function of voltage. The resonances appear in the subgap regime of the junctions and the subgap current (leakage current) is concealed. The positions of the resonances do not change as a magnetic field is applied to the junctions, but their amplitude decreases when the supercurrent is suppressed. We have measured the subgap current of Al/AlO_x/Al junctions and we show that these resonances are due to resonant modes in the chip design which are excited by the ac-Josephson effect. We present a chip design that decreases the amplitude of the resonances to a such degree that the subgap current is quantifiable.

1. Introduction
When a Josephson junction with a critical current $I_c$ is biased with a voltage $V$, the phase will vary linearly with time across the junction, corresponding to an AC current with amplitude of the order of $I_c$ and frequency $(2e/h)V$. This is referred to as the ac-Josephson effect. The ac-Josephson effect may excite resonant modes in the surrounding circuit and result in excess current peaks in the IV curves of the Josephson junctions. These modes have been observed by several groups [1–3] in the subgap regimes of the Josephson junctions, thus concealing the subgap current of the junctions. The position of the excess current peaks does not change as a magnetic field is applied to the junctions, but their amplitude decreases as $I_c$ is suppressed.

We have performed simple simulations of different chip contact layouts and experimentally studied the resonance peaks in the IV curves of Al/AlO_x/Al junctions. A remarkable decrease of the resonance amplitudes by altering the contact layout of our chips has been observed.

2. Simulations
A chip contact layout is equal to a distributed LC-circuit, the leads having an self-inductance and a capacitive coupling to ground through the substrate, onto which the structure has been fabricated. The resonant behaviour of the LC-circuit coupled to a Josephson junction gives rise to current peaks in IV curve of the junctions [4], the nature of which could be easily calculated in case the leads were perfect transmission lines. As our standard chip contact layout is far from perfect transmission lines, we have simulated the impedance of a chip contact layout using Microwave Office ®. A standard contact pattern is represented by tapered leads with lengths of 5.2 mm and widths, W, from 900 to 6 µm, see figure 1. The leads couple to the Josephson
junction, represented by a capacitor and resistor coupled in parallel, of 1.8 fF (corresponding to an Al/AlO$_x$/Al junction area of $\sim 0.04 \mu$m$^2$ [5]) and 2000 Ω respectively. The contact layout and junction is simulated on a dielectric with a thickness, $T$, of 120 µm with a dielectric constant of 6. Microwave Office® assumes a quasi-TEM mode of propagation and thus has restrictions on $W$ and $T$ of the layout; in this layout, 120 µm is the maximum limit of the dielectric thickness. The impedance between port 1 and 2 of this layout is shown in figure 2 (△); the impedance is oscillating, and the distance between maxima is $\sim 13$ GHz. The distance between maxima depends on the length of the leads; by reducing the length of the leads to 180 µm, the distance between maxima increases to $\sim 130$ GHz. The amplitude depends distinctly on the width of the leads, the thickness of the dielectric and the dielectric constant and very little on the resistance and capacitance of the junction.

In order to get rid of the oscillating behaviour of the impedance, the tapered leads can be substituted by on-chip low-pass filters, simulation of which is shown in figure 2 (■). The low-pass filter is a 6-element stepped impedance filter with a cutoff frequency of 10 GHz, formed by six narrow contact lines of alternating widths (1 and 15 µm) corresponding to alternating microstrip impedances of 15 and 150 Ω patterned on 800 nm thick dielectric (minimum limit in the simulation) with a dielectric constant of 6 [6]. The total length of the filter is 5.2 mm just as the tapered lines. The impedance of this design has a vague oscillating behaviour, which intensifies as the thickness of the dielectric increases. A spectrally flatter impedance is obtained by substituting the 6-element filter leads with single narrow leads with widths of 1 µm and lengths of 5.2 mm, shown in figure 2 (○).

The amplitudes of the impedance resonances thus decreases when the width of the leads are decreased, suggesting that a high microstrip loss attenuates the resonances. Also, a larger capacitive coupling between the microstrip and the groundplane, i.e., a thinner dielectric layer or a higher dielectric constant, decreases the amplitudes of the impedance resonances due to an increase of the loss of the microstrip.

3. Sample fabrication
We have fabricated Josephson junctions contacted by chip layouts somewhat similar to the designs simulated above. The samples used in this study are all fabricated on oxidized Si wafers. The chip size is 7 by 7 mm in size and has 16 contact pads which fits to a sample holder equipped with spring probes. The chip is thus not bonded but pressed against the probes of the sample holder. Our standard chip contact layout to this holder has tapered leads, 900 to 6 µm in width and 2-3 mm long, connecting the contact pads to each side of the junction. This standard chip layout is illustrated figure 3(a).
Figure 2. Three different chip design simulated in Microwave office ®; standard chip contact layout △, 6-element stepped impedance low-pass filter ■, narrow leads ○.

The modified chip design has narrow contact leads of different widths and 2-3 mm long. The design has an embedded groundplane consisting of 30/600/30 nm Ti/Au/Ti covered by a ~ 300 nm PECVD-grown SiNx grown at a substrate temperature of ~ 300° and a 2 % SiH4 and NH3 flow of 2000 and 40 sccm respectively. The growth rate was around 10 nm/min. The design is shown in figure 3(b). The chip size is slightly larger (7.5 by 7.5 mm) in order to make room for a 6 element stepped impedance low-pass filter on each side of the junctions. The top right and bottom left contact pad is directly coupled to the groundplane by etching through the SiNx via a ~ 3 min CF4 plasma etch at 50 W. Both design has e-gun evaporated contact leads and pads consisting of 30/600/70 nm Ti/Au/Pd.

Figure 3. (a) Standard chip contact layout fabricated on oxidized Si wafer, (b) Modified chip contact layout fabricated on embedded Ti/Au/Ti groundplane.

The Al/AlOx/Al junctions have an area ~ 0.04 µm² and are positioned in a SQUID configuration of area ~ 10 µm² in order to be able to suppress the supercurrent in the junctions by a magnetic field perpendicular to the chip. The junctions themselves are fabricated by using the double-angle evaporation technique with a two-layer resist. The resistance of the junctions varied from 3 -11 kΩ.

4. Experimental Results
The curve in figure 4(a) shows an IV curve of a Josephson junction measured on the standard chip layout. The layout is fabricated on oxidized Si wafers without a groundplane.

The curves in figure 4(b) shows IV curves of junctions connected with a 6 element low-pass filter (■) and junctions connected with single narrow leads with width of 1.45 µm (——), both chip contact layouts grown on a groundplane embedded with ~ 300 nm SiNx. The curves were recorded while the groundplane was not grounded; in this case the groundplane works only to increase the microstrip loss of the leads, as discussed earlier. When the groundplane was
grounded to the chassis of the refrigerator, the resonance at 150 µV disappeared in the IV curves on some junctions but not all, depending on the location of the junction on the chip.

Figure 4(c) plots the current amplitude of the resonances marked with arrows on figure 4(a) and (b) at ∼45 µV and ∼150 µV and is seen to increase linearly with $I_c$ of the junction at high $I_c$.

5. Conclusions
Resonant modes in a chip contact layout can be attenuated by increasing the microstrip loss of the contacts. This increase can be implemented by introducing an embedded groundplane and narrow chip contact leads.

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