On the Performance of Dual-Gate Reconfigurable Nanowire Transistors

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Abstract—We investigate the operation of dual-gate reconfigurable field-effect transistor (RFET) in the program-gate at drain (PGAD) and program-gate at source (PGAS) configurations. To this end, dual-gate silicon nanowire (SiNW) FETs are fabricated based on anisotropic wet chemical silicon etching and nickel silicidation yielding silicide-SiNW Schottky junctions at source and drain. Whereas in PGAD-configuration ambipolar operation is suppressed, switching is deteriorated due to the injection through a Schottky-barrier. Operating the RFET in PGAS-configuration yields a switching behavior close to a conventional MOSFET. This, however, needs to be traded off against strongly non-linear output characteristics for small bias.

Index Terms—Electrostatic doping, lift-off, MOSFET, nanowire, PGAS, PGAD, reconfigurable field-effect transistor, silicidation, silicon-on-insulator, TMAH

I. INTRODUCTION

In recent years, device scaling close to the physical limit has spurred the move from geometrical to equivalent scaling [1] of conventional MOSFETs utilizing new device architectures, materials and integration schemes to continue delivering integrated circuits with higher density and improved performance (power, speed). In addition, fabrication techniques such as ion implantation, yielding n- as well as p-type conduction of an intrinsic semiconductor, gradually become less suitable as device structures are being aggressively miniaturized into the deep nanoscale. The finite solid solubility of dopants and their increased ionization energy in nanoscale dimensions [2] could lead to increased parasitic resistances and capacitances in the source/drain regions. Furthermore, the statistical nature of ion implantation and dopant diffusion during the activation anneal make it hard to implement well-defined potential profiles with abrupt interface transitions within a small volume of semiconductor material, leading to a variability in threshold voltage \( V_{th} \) from device to device due to random dopant distribution effects. Moreover, the potential landscape created by physical doping stays fixed after the implantation/activation process which only allows either n- or p-type unipolar operation mode.

The aforementioned issues are best addressed if doping in source/drain and channel can be avoided altogether. Recently, reconfigurable FETs (RFETs) have attracted an increasing attention because they utilize electrostatic doping to create virtual n-/p-regions avoiding dopant related issues. Moreover, they can be tuned to operate as n-/p-transistors with unipolar device operation similar to conventional MOSFETs [3]–[7]. Previous work using tri-gates [3], [7], i.e. two for creating virtual source/drain regions and the third for on/off switching, has demonstrated reconfigurable devices with high \( I_{on}/I_{off} \) ratio and steep switching behavior. The adoption of three gates will certainly need more area and might become a key limiting factor for down-scaling. Hence, devices using only a dual-gate architecture have been investigated [4]–[6]. In these devices, the gate at the drain contact is used to ‘program’ the device either to n- or p-type operation while the gate at the source is used as the switching or control gate. However, while unipolar device operation is obtained with this program-gate at drain configuration (PGAD), the inverse subthreshold slope is significantly larger than 60 mV/dec. This is obvious since the RFET in PGAD configuration is simply a Schottky-barrier MOSFET with suppressed ambipolar operation [8]. In this work, we investigate the device configuration with the program-gate at source (PGAS) and compare it with the PGAD. As it turns out, the PGAS configuration yields a switching behavior similar to a conventional MOSFET with the drawback of a larger off-state leakage. Furthermore, PGAD and PGAS show a distinctly different non-linearity in the output characteristics with a stronger effect in the PGAS configuration.

II. DEVICE FABRICATION

Reconfigurable silicon nanowire FETs are fabricated using a top-down approach with a two-step wet chemical etching as described in [9]. Tetramethylammonium hydroxide (TMAH) instead of potassium hydroxide (KOH) is chosen as the wet chemical etchant of silicon to ensure a fully CMOS-compatible fabrication process. A \{111\} facet inclined at 54.74° with respect to the \{100\} facet is formed due to the distinct etch-rate anisotropy of different crystallographic planes [10] in an
alkaline solution (i.e. TMAH) when a silicon nitride hardmask is defined in a line-pattern along the [110] direction of a (100)-oriented silicon substrate. Exploiting the ability of SiN to act as effective diffusion barrier enables a local oxidation of the etched {111} facet. After selective removal of the SiN a triangle bounded by two {111} facets is formed in a second TMAH etching since the {111} facet fabricated with the first TMAH etch step is protected by the grown, local oxide (cf. Fig. 1(a), step 1). Atomic force microscopy is used to probe the surface roughness of the wet-etched {111} facet formed on a step structure (step height ～800 nm) in a bulk silicon substrate, the measured root-mean-square (RMS) value = 0.3992 nm from a rectangular scanning area (800 nm × 250 nm) is well within the range of a commercial prime-grade silicon wafer (RMS = 0.2–0.8 nm) [11]. If such a process is carried out on a (100)-oriented silicon-on-insulator substrate (p-type boron doped, 10^{15} \text{cm}^{-3}, \text{top-Si} ～80 \text{nm}, \text{buried oxide} ～145 \text{nm}), the buried-oxide acts as an etch stop layer. Hence the size of the triangle mainly depends on the thickness of the top silicon layer. Subsequently, a dry oxidation step is carried out to reduce the size of the SiNW and form a gate oxide at the same time. The dry oxidation is carried out for 3 min at a temperature of 1100 °C, i.e. higher than the viscous flow point. Although such a high temperature prevents a self-limiting oxidation [12] it allows transforming the cross-section of the SiNW from triangular to a circular shape while minimizing the degradation of the Si/SiO_{2} interface due to roughness induced by the oxidation process [13]. Next, etch windows are patterned in the source/drain contact areas to remove the oxide shell with buffered oxide etch (BOE). Subsequently, nickel contacts and gates are fabricated with electron beam lithography using a bilayer PMMA resist, electron beam evaporation and lift-off. Finally, the sample is annealed in forming gas (mixture of 90% N_{2} and 10% H_{2}) at 450 °C to silicide the SiNW and drive the silicide-SiNW junction underneath the two gate electrodes to avoid a gate retardation and achieve a good electrostatic control of the silicide-SiNW junctions; Fig. 1(c) shows this Ni intrusion into a SiNW surrounded by an oxide shell after the selective removal of the unreacted Ni in source/drain regions (which also removes the two gates). Fig. 1(b) shows a scanning electron micrograph of a readily fabricated reconfigurable dual-gate FET.

III. DEVICE CHARACTERIZATION

I-V characteristics of the reconfigurable field-effect transistors are measured in PGAD- and PGAS-configurations and compared with each other. In both (PGAS and PGAD) configurations, a constant voltage applied to the PG generates a virtual p- or n-type doping section whereas the other gate - called control gate (CG) - is used to switch the transistor. Figure 2 shows transfer curves of a RFET in PGAS (red curves in the right panels) and PGAD configurations (blue curves in the left panels) for both n- and p-type operation modes with increasing V_{PG} values and their corresponding band diagrams. In the case of PGAS, a virtual n-doped source contact is created at the source side if a positive voltage is applied to the program gate, and the behavior of the device is similar to a conventional n-type MOSFET in terms of a steep inverse subthreshold slope. The on-state current increases with a larger V_{PG} due to the increased carrier injection at the
source Schottky junction. In PGAD configuration, a virtual n-type drain contact is created if a positive voltage is applied to the program gate. In this case, the carrier injection through the source-side Schottky-barrier is modulated by different gate voltages in PGAD configuration for both n-type and p-type operation modes. In PGAS configuration, a non-linear current increase in the triode regime is observed, typical of a Schottky-barrier MOSFET. In the PGAS configuration, a non-linear current increase for small bias is also observed. However, in contrast to PGAD, an exponential increase is obtained that is almost the same for all CG voltages displayed in Fig. 4 (b) and (d); a saturation of the current at different levels occurs only for \( V_{ds} \) larger than \( \sim 1 \) V. Both non-linearities, i.e. in PGAD and PGAS, deteriorate the functionality of logic inverters built from those devices. However, the PGAS configuration is particularly detrimental leading to a complete loss of noise margin.

The different behavior of the output characteristics of the two device configurations may at first be surprising since it is generally argued that the non-linearity of the \( I_d - V_{ds} \) curves stems from the forward biased drain Schottky junction. As will become clear below, this is not the case: while the non-linearity of the PGAS configuration is indeed due to a forward-biased drain Schottky junction, the non-linearity of the PGAD configuration is due to an increased tunneling through the source-side Schottky-barrier.

**IV. DEVICE SIMULATIONS**

In order to elaborate further on the behavior of RFETs and in particular to understand the difference in the non-linear behavior of the PGAS and PGAD configurations, self-consistent device simulations using the non-equilibrium Green’s function approach on a finite difference grid have been carried out [14]. An effective mass approximation with symmetric conduction and valence band is assumed; the complex band structure within the band gap is taken into account with Flietner’s dispersion relation [15]. To reduce the computational burden, a nanowire FET with one-dimensional electronic transport is considered. Furthermore, the electrostatics is described by a 1D modified Poisson equation where the device architecture and valence band is assumed; the complex band structure is accounted for with a proper choice of a natural lengths scale \( \lambda \) which represents the characteristic length on which potential variations are being screened [16], [17]. This simulation approach has been used successfully to reproduce and explain the device behavior of conventional as well as Schottky-barrier field-effect transistors (see e.g. [18], [19]).

An important ingredient here is the inclusion of Büttiker probes (cf. Fig 5 (a)), i.e. virtual contacts attached to the
channel of the RFET that mimic inelastic scattering [20]; the Fermi levels of all Buettiker probes are determined to ensure a net zero current from/into each Buettiker probe thus representing the quasi Fermi level within the device. Fermi level pinning with a midgap position of the source/drain Fermi level yielding a Schottky-barrier of $\Phi_{SB} = E_F/2$ is assumed at the interface between source/drain and the channel; all other device parameters are stated in Fig. 5.

Figure 5 depicts simulated output characteristics in PGAD (b) and PGAS (c) configuration, qualitatively reproducing the experimental results displayed in Fig. 4. In particular, the strong non-linear current increase for small bias in the PGAS configuration compared to PGAD is observed. Figure 6 shows a single $I_d-V_{ds}$ curve for PGAD=1.7 V, CGAD=0.8 V (a) and PGAS=1.7 V, CGAD=0.8 V (b) showing clearly the different behavior of the two device configurations: while PGAD exhibits an almost linear behavior in the region of small bias\(^1\), PGAS shows a strong non-linearity. The reason for this different behavior becomes obvious when comparing Fig. 6 (c) and (d): in PGAD, the quasi Fermi level (green dashed lines) at the drain end, i.e. underneath gate 2, drops substantially with increasing bias. This is due to a loss of carrier injection from drain such that the conduction/valence bands are moved to lower energies because of the large $V_{FG}$ at gate 2. As a result, the device does not behave like a forward biased Schottky junction. Instead, the small non-linearity observed in (a) stems from an increased tunneling through the source-side Schottky diode with increasing $V_{ds}$ due to a significant reduction of the carrier density underneath the control gate (cf. Fig. 6 (c)). Note that the same is true in conventional, single-gate Schottky-barrier MOSFETs [21]. In contrast, in the case of PGAS (Fig. 6 (b) and (d)) the quasi Fermi level remains rather fixed by the source contact and increasing the bias yields a forward biased Schottky-junction with an exponential increase of the current. This rather undesirable behavior strongly deteriorates, e.g., the performance of inverters made of RFETs configured in PGAS.

In conclusion, with only two individually controllable gates, the PGAS configuration yields an almost ideal switching behavior while its output characteristics are deteriorated when compared to PGAD which exhibits improved output but deteriorated transfer characteristics.

V. Conclusion

Reconfigurable FETs with wet chemically etched SiNWs and Ni silicidation are fabricated and characterized for both PGAS and PGAD configurations. The top-down fabrication approach yields localized SiNWs with atomically flat surfaces and minimal plasma damage manufacturable with conventional h-line contact lithography. The one-step silicidation process at $450^\circ$C creates a silicide composition that has a Fermi level close to the valance band of silicon. In PGAS configuration, the RFET demonstrates a steep inverse subthreshold slope comparable to a state-of-the-art conventional MOSFET. However, $V_{ds}$ should be kept low to prevent leakage current increase induced by the other carrier type. In PGAD configuration, the RFET is a Schottky-barrier MOSFET with suppressed ambipolar behavior. The price paid for a lower off-state leakage current and more unipolar device behavior is a deteriorated switching behavior. The quasi Fermi level through the device simulated with Buettiker probes to mimic scattering explains the difference in output characteristics for both PGAS and PGAD configurations.

\(^1\)Note, that this is the case due to the large difference in $V_{FG}$ and $V_{CC}$. For larger CG voltages as displayed in Fig. 5 (b), the output characteristics also become non-linear in the PGAD configuration.
ACKNOWLEDGMENT

Bin Sun is grateful for financial support from the China Scholarship Council. The authors thank M. Liebmann (2nd Institute of Physics B, RWTH Aachen University) for carrying out AFM measurements.

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