RNM Calculation of 6T SRAM Cell in 32nm Process Node based on Current and Voltage Information

K. S. Sreekala* and S. Krishnakumar

Department of Electronics, School of Technology and Applied Sciences, Mahatma Gandhi University, Edappally, Kochi – 682024, Kerala, India; sreekalasyam@gmail.com

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Abstract

Objectives: This work aims to analyze the dependency of \( V_{DD} \), T and CR (Cell Ratio) on cell stability in terms of Read Noise Margin (RNM) in 32nm technology by the N-curve and butterfly graphical methods. The advantages of considering both voltage and current information for SRAM cell stability measurement have been reported. Methods/Statistical Analysis: The cell stability calculation of SRAM is a central concern in submicron CMOS process nodes, as they reason for increase in dies variability and voltage scaling. The cell Stability of the SRAM is typically calculated by Static Noise Margin (SNM). As it varies with different operating modes of a cell, a detailed analysis is required. In this article, the RNM of SRAM cell is computed by N curve, which compares with the SNM by bufferfly method. SRAM with PMOS access transistor for improved read stability and low voltage application is also presented. Findings: Results show that proposed SRAM gives 50% cell stability in read mode of operation over conventional SRAM cell for CR=3. Application/Improvements: The typical SRAM bit cell with PMOS access transistor shows improved read stability at low voltage application than standard SRAM cell.

1. Introduction

SRAM remains to be principal components over system-on-chip and high speed VLSI design circuits. Low Power (LP) SRAMs have evolve in to a critical part of many microprocessor chips. Unlike DRAM, which requires the periodical refreshment of the cell in order to preserve the stored content, SRAM does not want to be refreshed to keep the stored data. The necessity of further circuitry and timing generate some obstacle that makes DRAM memory slow and less interesting than SRAM. SRAM modules are much simpler compared to DRAM, which makes it more easy to create an interface for accessing the memory. The most prominent use of SRAM is in the cache memory of processors where speed is very essential, and the power consumption convert to less heat to be dissipated. The minimum operational voltage \( V_{DD} \) for SRAM memories is limited by either write ability or read stability. The scaling of SRAM memory makes it difficult to guarantee the cell stability. It is determined by the Static Noise Margin (SNM) which is the essential criteria for designing the memory cell. SNM is the nominal static noise voltage that causes the cell to flip and a static method to quantify the cell stability of SRAM. The Cell Ratio (CR) and Pull-up Ratio (PR) are the two main parameters that determine the read and write noise margin of the cell. The value of CR and PR equalizes the cell stability and performance. This article present a thorough analysis of RNM of 6T SRAM based on N-curve and butterfly curve methods. Conventional 6T SRAM is chosen as it grant long regime, even in the 15nm technology node. In this paper, 32nm PTM model card (Predictive Technology Model) is selected to explore the performance characterization in different modes of the cell. It provides accurate and compatible model files with a wide range of process variations. All net list simulations are carried out using Eldo spice circuit simulator. The remaining work is presented as follows. Section 2 describes about work-
ing and failure mechanism of conventional 6T SRAM cell. Section 3 provides various graphical approaches to estimate the NM stability of SRAM bit cell. 6T SRAM with PMOS access transistor is introduced in Section 4. Section 5 gives simulation results and discussion of conventional SRAM and proposed technique, which explore the impact of CR, supply voltage and temperature on cell stability. Finally Section 6 provides the conclusion.

2. 6T SRAM and Read Failure Mechanism

SRAM semiconductor memory uses two back-to-back latching circuitry to preserve each data bit. A typical CMOS SRAM is depicted in Figure 1. The cell composed of two cross coupled CMOS inverters (M1, M2, M3 & M4) that can keep one bit of data at a time, and other two NMOS pass transistor (M5 & M6) act as an access transistors to connect storage nodes (Q&QB) of cell to the bit lines (bl & blb). The cell operates in three modes, read, write and hold. In read mode, the bit lines together with word line (wl) are pulsed to a logic high level. Two complementary bit-lines (bl & blb) are attached to a sense amplifier that identify if a logic data ‘1’ or ‘0’ is stored in the preferred elementary cell. In write mode, one of the bit lines is pulsed to $V_{DD}$ and the other bit line is connected to gnd, whereas in hold mode, wl is connected to gnd to turn off the access transistors and the feedback path will preserve the stored data. The hold and read margin determine how well a memory cell keeps its data, while write margin determines how well data can be recorded to a memory cell. Conventionally, SRAM yield is predicted either by read margin or a write margin. 

In order to maintain the data stability and performance of the typical 6T SRAM cell, strict constraints on the dimensions of transistors is required. To retain the stability in write operation, the current carrying capacity of M5 & M6 must be higher than M2 and M4 respectively. The read margin is much more important than hold margin, since in read operational mode the Q & QB are connected to the precharged bit lines (bl &blb). To attain a high read stability, the current capacity of M1 and M3 must be higher as compared to the M5 and M6. However this decline the stability in write operational mode of the cell. Hence, there is a read and write edge trade-off between them. During read cycle, the sense amplifier changes the differential signal from bit lines to a logic output level. Again, at the read cycle extreme, the blb returns to the supply rail value. Each bit in a typical SRAM cell is stored by the driver and load transistors which form two cross-coupled CMOS inverter latch. The access transistors M5 & M6 helps to control the memory access operation of the storage nodes Q and QB. Figure 2 illustrates the stability failure in read mode which results in unexpected flipping of stored data. Here the cell is most sensitive towards noise and the cell stability is badly affected. At the time of read cycle (assume QB=1 & Q=0), the internal storage node Q characterizing a low (‘0’) voltage level gets pulled to $V_{DD}$ by M5 due to the voltage divider effect of M1 and M5. This in turn reduces the read noise margin. When the voltage at Q reaches the $V_n$ of M3, the voltage at node QB begins to decrease and this regenerative action flips the stored data in the cell. To prevent the read failure the driver M1 should be more powerful so that voltage at node Q does not increases more than $V_{th}$. Accordingly for read stability given by Equation (1)

$$I_{M1} \geq I_{M5}$$ (1)
Hence Cell Ratio (CR) is given by

\[
CR = \frac{W_{M1}}{W_{M5}}
\]

During write mode (wl=blb=V_{DD}, bl=0) say going to write '0' at node Q while initially Q=V_{DD}, hence the storage voltage at node Q reaches a low voltage so that the load transistor M4 gets 'on' and the voltage at QB starts to rise and the regenerative action of the cross-coupled inverters causes the Q=0. To prevent write failure, the transistor M5 (access transistor) should be strong enough so that voltage at node Q does not go below \( V_{th4} \). For write ability, PR is derived by (2)

\[
I_{M5} \geq I_{M2}
\]

i.e,

\[
(I_{M5})_{sat} \geq (I_{M2})_{lin}
\]

Pull-Up ratio is

\[
PR = \frac{W_{M2}}{W_{M5}}
\]

Since Q and QB are connected to bl and blb respectively in read mode, thus it is more important than hold margin.

### 3. Graphical Methods of Measuring the Cell Stability of SRAM - N Curve and Butterfly Curve

In this article, the cell stability of the SRAM is characterized by the SNM. It is directly connected to the threshold voltages (\( V_{th} \)) of the drivers and load transistors in the SRAM memory. The presence of cell noise value higher than SNM, alter the condition of the cell and which causes the stored data to lose. Butterfly curve is one of the familiar graphical method to calculate the stability of the cell. It is achieved by drawing and flipping the Voltage Transfer Curve (VTC) of the inverter and obtaining the least square among the biggest eyes of the butterfly curve as in Figure 3. The two back-to-back coupled inverters with infinite ideal gain decide the boundaries of a biggest square side of highest \( \frac{V_{DD}}{2} \).

![Figure 3. Butterfly curve for SNM analysis.](image)

Another read stability calculation by graphical method situated on the N-curve is illustrated in Figure 4. This method providing the united information of voltage and current, which is Static Current Noise Margin (SINM) and Static Voltage Noise Margin (SVNM) to overcome the limitation of scaling the supply voltage. To extract the stability information from N-curve in read mode, it is necessary to precharge both bit and word lines to supply voltage \( V_{DD} \). For obtaining N-curve, a voltage source \( V_s \) is inserted at ‘0’ storage node QB and sweep from ‘0’ to ‘\( V_{DD} \)’. The point corresponding, two stable states and one meta-stable state obtained after simulation are P, Q and R respectively. When point representing stable states coincides, a degraded read operation can arise easily. The difference in voltage between the point P and Q choose the highest acceptable static noise voltage which is SVNM at QB, before its content flips. The highest value of current in middle of P and Q namely SINM, determine the read margin of the cell. The above noticed metrics combined with SNM can be used to estimate cell stability in...
read mode. Furthermore, to calculate the write ability the Write Trip Point (WTV) and Write Trip Current (WTI) are the two extracted information from N-curve, which helps to more accurate prediction of the cell stability. The difference in voltage between the point Q and R represent the Write Trip Voltage (WTV) and the negative peak value of current within a point Q and R denote the Write Trip Current (WTI). Higher value of WTV or WTI point out a smaller write margin.

Table 1. Noise margin for two different width

| Width(W) | SNM(mV) | SVNM(mV) | SINM(uA) |
|----------|---------|----------|----------|
| W        | 300     | 140      | 110      |
| 2*W      | 300     | 140      | 210      |

In order to verify the above statement, a comparison between the stability information extracted from the butterfly curve and N-curve methods are necessary. Table 1 list out the simulation results of noise margin stability information from the above mentioned two graphical methods with varying width. It can be noticed that when the width is doubled, the voltage information given by SNM and SVNM for both designs are same. But there is an increase in SINM for the second design (2*W). This verifies that current information is also valuable for read stability computation.

4. Modified SRAM Cell for Improved Noise Margin

The standard SRAM cell with NMOS access transistors results the threshold voltage degradation during the transition of logic ‘1’ voltage at the storage node. The PMOS access transistors M5 and M6 in Figure 5 provides full logic ‘1’ voltage level due to the ability to pass ‘1’ without voltage degradation. With the new SRAM circuit, the degradation in storage data in read mode is decreased by inserting PMOS access transistor. Figure 5 shows the input of PXR and PXL access transistors are connected to the raw selection line (\( w \)) to perform read and write action over the column lines (bl & blb). During the read and write time the \( w \) is held low to accomplish the cell access. The read operation of new SRAM is identical to the typical SRAM. It uses the back-to-back inverters which analogous to the exiting 6T SRAM topology. A comparative SNM simulation result of modified and conventional SRAM cell using butterfly curve is shown in Figure 6.

![Figure 5. 6T SRAM with PMOS Access Transistor (PXR and PXL).](image)

![Figure 6. Butterfly curve for Conventional 6T SRAM and Proposed SRAM.](image)

It can be noticed that modified SRAM cell exhibit improved read stability as compared with the typical 6T SRAM. In addition, new SRAM exhibit less leakage current than typical SRAM cell with equal size. The new cell does not require any extra circuitry for normal operation, accordingly it does not induce extra area and power requirement. Therefore, to prevent read and write deterioration, CR = 3 and PR = 0.6 are maintained in the simulation result shown in Figure 6.

5. Results and Discussion

The impact of scaling on \( V_{dd} \), CR, and T on read stability is simulated using 32nm PTM process model card is presented. Continues scaling of CMOS technology has results into variability in performance that is attributed to process variation. This work given more important to read stability, so that read SNM is measured based on both butterfly and N-curve method. The read SNM
The cell stability of 6T SRAM depends on supply voltage, temperature and Cell Ratio. Three different CR (CR=1, 2 and 3), three different temperatures (T= 50°C, 150°C and 250°C), and three different supply voltages ($V_{DD}$ = 0.8V, 0.5V, and 0.3V), are selected for the comparison purpose as in Table 2. The cells are designed with minimum length for all transistors and minimum width for pull-up transistors. The size of the driver transistors changes with the Cell Ratio. Both N-curve (SVNM, SINM) and butterfly curves (SNM) are used to compare the static read stability. Table 2a illustrates, proposed 6T SRAM cell shows enhanced read margin for a given CR. It is clear that as CR increases the cell stability also increases. With CR=3 the proposed SRAM achieves 50% read stability over the base case. For a proposed 6T SRAM, it is shown that, SNM and SVNM are same for CR =2 and 3. But there is 57% improvement in SINM for CR=3 than CR=2. This confirms that CR=3 provide improved read stability than CR=2. Figure 7 shows that modified SRAM cell achieves 46% SVNM, 6.6% SINM over typical SRAM with Cell Ratio of 3. In Table 2b, we can observe that the read stability decreases with increase in temperature. We selected the value of CR and PR as 3 and 0.6 respectively for the temperature and supply voltage evaluation. With
proposed SRAM, when the temperature varies from 50°C to 250°C, there is a reduction of SNM by 25% and the same is 57% for conventional circuit. This ensures that, the modified cell shows high noise margin for read operation even at elevated temperature. Figure 8 shows the impact of temperature on read stability. Let us focus on T =250°C, the proposed cell results 2 x SVM, 25% SVNM, and 2.5 x SINM over new 6T SRAM cell. Table 2c display the influence of V_DD degradation in read mode of operation. The RM in read mode of typical SRAM cell is deteriorated with V_DD < 0.8V. When V_DD = 0.8V, the new SRAM circuit bring about 53% SVNM, 61% SINM over new SRAM topology is illustrated in Figure 9. The proposed design shows read stability even at low supply voltage (Table 2c. V_DD =0.3V).

The main observations derive from table and graph is that SNM is higher for higher cell ratio and higher power supply. The increases in CR, positively affect the current, which in turn speed up the memory operations of the cell. The effect of supply voltage variation on read margin creates it more preferable to retain full V_DD value in read mode. Moreover, the threshold voltage of MOSFET is crucially affected by the temperature variation, which results degradation of the noise margin.

6. Conclusion

A read efficient six transistor SRAM circuit with PMOS as access transistors for low voltage application is presented. The impact of CR, V_DD, and T on cell stability is analyzed using N-curve and butterfly graphical methods. The simulation results show that proposed SRAM achieves 1.5 x SNM for CR=3 & 3x SNM for T=250°C, also 2x SNM for V_DD=0.8V than typical SRAM with equal size.

7. References

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