Online Health Monitoring of DC-Link Capacitors in Modular Multilevel Converters for FACTS and HVDC Applications

Mohsen Asoodar, Student Member, IEEE, Mehrdad Nahalparvari, Student Member, IEEE, Christer Danielsson, Rasmus Söderström, and Hans-Peter Nee, Fellow, IEEE

Abstract—This article presents an online health monitoring scheme for dc capacitors in modular multilevel converters (MMCs). The health monitoring algorithm is based on detecting changes in the dc capacitance value over time. The proposed algorithm only utilizes measurements that are typically available in flexible alternating current transmission systems and high-voltage direct current applications. Hence, in the proposed estimation method, no additional sensors are used. The estimation scheme considers the presence of noise in voltage and current measurements, and utilizes a recursive least square estimator in conjunction with a special low-pass filter to minimize the estimation errors. Simulation results of a hardware replica, as well as experimental results on a low-power MMC prototype show that the proposed scheme can identify the dc-link capacitance value with a maximum error of 1%.

Index Terms—DC capacitor, flexible alternating current transmission systems (FACTS), health estimation, modular multilevel converter (MMC), online monitoring, reliability.

I. INTRODUCTION

DC CAPACITORS act as energy buffers in modular multilevel converters (MMCs). In flexible alternating current transmission systems (FACTS) and high-voltage direct current (HVdc) applications, MMCs are typically operated at low switching frequencies in order to minimize switching losses [1]. Consequently, the dc-link capacitors in FACTS and HVdc applications are subject to low-frequency current pulses that are in the order of one or a few multiples of the network frequency [1], [2]. Due to this low-frequency current of dc-link capacitors, in MMCs, large capacitor units are opted to minimize the low-frequency voltage ripple on each dc-link capacitor. Although large dc capacitors in MMCs can reduce the low frequency voltage ripple on each MMC module, they are inevitably bulky and hold a significant amount of energy [3]. Therefore, it is important to predict or avoid any component failure that can lead to a sudden discharge of the energy in dc capacitors. If left unprotected, undesirable short-circuit failures can lead to high surge currents within the submodules [4], [5]. Unprotected failures can potentially damage adjacent components in the circuit and halt the operation of the converter. Since component failure is inevitable in power electronic circuits operating over extended periods of time, protective measures must be taken to avoid stoppage of operation as a result of component failure. These protective measures are realized through additional protective hardware [6], or via health estimation of vulnerable components [7]. The focus of this article is on creating a reliable protective measure for dc-link capacitors in MMCs through online estimation of their health state.

In [8] and [9], two methods for online monitoring of dc capacitors in MMCs are presented. However, in both methods, the value of a charge/discharge resistor must be known with great accuracy in order to assure accurate capacitance estimations. Moreover, in [9], normal operation of each submodule must first be altered before its capacitance can be measured. Also, this solution has the disadvantage of creating extra losses in the system only to simplify the capacitance estimation. In [10], a quasi-online impedance monitoring scheme is presented for condition monitoring of dc capacitors. This solution requires injection of certain harmonics in the converter arms, which inevitably increases the losses in the converter. Yu et al. use additional current sensors to identify the health state of components in an MMC submodule [11]. However, this solution requires accurate current sensors for every submodule. Online capacitor estimation techniques have also been conducted for MMCs assuming a relatively high switching frequency [7], [12], [13]. However, in practical high-power MMC applications, lower switching frequencies are used to reduce the switching losses. Hence, the proposed algorithms using high switching frequencies cannot be immediately used for practical MMCs in FACTS and HVdc applications.

The research conducted in [14] provides a major contribution to the study of online health monitoring of dc capacitors in MMCs, where practical limitations such as the low switching frequency of high-power MMCs are considered. Despite their promising algorithm, no explanation is given for the choice of the
recursive least square (RLS) estimator in comparison to simpler filters. Moreover, that solution cannot be immediately used in MMC-based static synchronous compensator (STATCOM) applications due to its negative effect on the signal to noise ratio (SNR) of the voltage measurement. Another suitable candidate for online capacitor estimation in MMCs is presented in [15], where a novel algorithm for reducing the effect of measurement noise through integration of the fundamental components of capacitor voltage and current is presented. One downside of this method is the sensitivity of the estimator to systems with very low switching frequencies and dynamic load variations. The solutions presented in [14] and [15] are nevertheless the most suitable state-of-the-art candidates for online dc capacitance estimation in MMCs. Hence, a comparison of these solutions with the proposed method is provided in this article.

The aim of this article is to present a solution for online dc capacitor monitoring in practical MMCs with low switching frequencies that has all the advantages of state-of-the-art methods, while exhibiting none of their shortcomings. That is, the proposed solution fulfills the following ten practical requirements of a real setup:

1) operation at low switching frequencies of MMC devices;
2) operation at a wide range of load currents;
3) uninterrupted operation of the converter for the purpose of measurements and estimations;
4) minimization of the effect of measurement noise in the estimated capacitances;
5) accurate estimation of submodule capacitance;
6) utilization of only the existing measurement devices in MMCs for the purpose of capacitance estimation;
7) self-correction of data skewing that might exist between voltage and current measurements;
8) minimization of required memory for postprocessing estimated values;
9) Suitability for a wide range of MMCs used for FACTS and HVdc applications.
10) Suitability for MMC applications with frequently varying output loads.

This article is organized as follows. Section II presents the converter topology on which the online capacitor estimation technique is studied. Section III presents the estimation algorithm, as well as the practical considerations for minimizing the estimation errors. In Section IV, a comparison study between the proposed solution and state-of-the-art solutions is provided. Section V presents the effectiveness of the proposed solution via simulation results in a hardware replica, and experimental results in a low-power prototype. Finally, Section VI concludes the article.

II. CONVERTER TOPOLOGY AND CONTROL HARDWARE

Among the different STATCOM topologies, MMC-based STATCOMs are the preferred solution in the industry for achieving high-efficiency power conversion while providing high power quality at their point of connection (PoC) [16]. Therefore, the proposed capacitor monitoring algorithm is mainly developed for MMC-based STATCOMs. The most popular topologies for these solutions are the Y-STATCOM [17], the D-STATCOM [18], and the double-Y-STATCOM [19]. Although the proposed capacitor monitoring algorithm presented in this article can be used in all three topologies, the illustrations in this article are based on the D-STATCOM and the double-Y-STATCOM topologies. The structure of an MMC-based D-STATCOM is depicted in Fig. 1. This converter consists of three chain-links in delta connection, where each chain-link is composed of a series-connection of full-bridge submodules. The full-bridge submodule shown in Fig. 2 can operate in all four quadrants of voltage and current, i.e., the output voltage, \( v_{\text{out}} \), of each full-bridge submodule can be positive, zero, or negative for any sign of the arm current, \( i_{\text{arm}} \). In Fig. 2, the parameters \( s_i \), \( i \in \{1, 2, 3, 4\} \) represent the gate signals, where \( s_i = 1 \) and \( s_i = 0 \) correspond to the ON-state and OFF-state of the switch \( s_i \), respectively. Each submodule can provide a three-level voltage output. Hence, for a chain-link of \( N \) series-connected submodules, \( 2N + 1 \) voltage levels are achieved. This multilevel voltage structure significantly improves the voltage quality at the PoC of the converter compared to conventional converters that
only provide two-level or three-level output voltages \[20\]. In this article, only full-bridge submodules are considered. However, similar algorithms can be applied to MMCs with half-bridge submodules as well.

In many grid-connected applications, STATCOMs are designed to act as a current source via an internal current controller. Therefore, in normal operation, a sinusoidal current at fundamental frequency is passed through each arm of a D-STATCOM \[21\], \[22\]. Moreover, the converter arms of an MMC are series-connected to an inductor, \( L_{\text{arm}} \), which acts as a passive filter. This arm inductor, together with the current controller, is used to transform the inherent voltage-source behavior of converters into a current-source mode. In MMCs, the direct voltage of submodule capacitors are controlled to a reference voltage through voltage balancing techniques. However, each capacitor submodule faces a certain voltage ripple depending on its capacitance value and the current pulse passing through each capacitor \[3\]. In literature, the preferred solutions for submodule capacitor voltage balancing utilize the direct voltage measurement of each submodule capacitor \[23\]. Therefore, each submodule capacitor is usually equipped with a voltage measurement unit. For the current measurement, typically one current sensor is employed in each arm of the converter. These sensors are depicted in Fig. 1. The intention of this article is to utilize these existing measurements in order to identify the health state of all dc capacitors in MMCs. In the topologies studied in this article, the voltage and current measurements are converted to digital values with a 12-bit analog-to-digital converter (ADC). Clearly, ADCs with high resolutions are more suitable for online estimation purposes. The choice of ADCs with higher resolution does not have a significant impact on cost, but must be considered in the early stages of product development. In this study, it is shown that a 12-bit ADC provides sufficiently accurate measurement data for the purpose of online capacitor estimation. The ADC outputs are read by the field-programmable gate array (FPGA)-based control hardware. Consequently, measurements of all capacitor voltages and arm currents are available in the FPGA controller. The control hardware also utilizes a system-on-chip processor, in which the capacitor voltage balancing as well as the current control is carried out. The system parameters and the control system used for studying the D-STATCOM topology are presented in Table I and Fig. 3, respectively.

### III. Capacitor Estimation Algorithm

In this section, the proposed idea for submodule capacitance estimation is presented. Moreover, the effect of measurement noise on estimation accuracy, as well as various solutions for reducing this effect are discussed.

#### A. Overall Estimation Algorithm

A correlation exists between the health state of dc capacitors used in MMCs and their equivalent series resistance (ESR) and capacitance values \[24\], \[25\]. In high-power MMC applications, large dc capacitor units are used. These capacitors have inherently small ESR values. Consequently, monitoring the ESR of dc capacitors in high-power MMC applications requires voltage and current measurements with accuracies higher than what is needed for the normal operation of the converter. Therefore, in this study, the health estimation algorithm for dc capacitors solely relies on the value of capacitance and its variation over time. In MMC applications, metallized polypropylene film capacitors are typically used. For such capacitors, a 5% reduction in capacitance is reported as their end-of-life \[25\]. Consequently, estimation errors must be significantly lower than 5% in order to achieve meaningful estimation values.

An MMC submodule is inherently a nonlinear system due to the hard-switching of its semiconductors. However, the dc
capacitor itself is a linear system, which is slowly degrading. This degradation is seen as a slow variation in the ESR and the capacitance. In order to estimate the value of the capacitance, both the current passing through the capacitor and its voltage are needed. Then, the capacitance value can be extracted via

\[ C = \frac{\int_{t_1}^{t_2} i_C \, dt}{\Delta v_C} = \frac{\int_{t_1}^{t_2} v_{C,t} \, dt}{v_{C,t_2} - v_{C,t_1}}. \]  

(1)

Since measuring the capacitor current directly requires placing an additional current sensor in every submodule, it is more favorable to extract the capacitor current using the existing arm current measurement. This can be carried out using the gate signals of the semiconductors in each submodule to identify whether the arm current is passing through a capacitor or not. As depicted in Fig. 2, a submodule capacitor’s current is only nonzero when \((s_1 = 1, s_2 = 0, s_3 = 0, s_4 = 1)\) or when \((s_1 = 0, s_2 = 1, s_3 = 1, s_4 = 0)\). In a simpler form, the capacitor current in each submodule can be calculated by multiplying the arm current with \(s_1 s_4 - s_2 s_3\) as

\[ i_C = i_{arm}(s_1 s_4 - s_2 s_3). \]  

(2)

Substituting \(i_C\) in (1) with (2) gives

\[ C = \frac{\int_{t_1}^{t_2} i_{arm}(s_1 s_4 - s_2 s_3) \, dt}{v_{C,t_2} - v_{C,t_1}}. \]  

(3)

During normal operation of the converter, (3) can be repeated to identify any changes in the capacitance of every submodule. The identified capacitance value can be stored in a memory at arbitrary time intervals. Since the dc capacitor degradation is a slow process, it is not necessary to store all estimated capacitance values, nor is it mandatory to store the estimated values at a high rate. The rate of storing estimated capacitances is dependent on the available free memory, and the speed at which an accurate estimation is needed.

In this study, the pulse number (PN) is defined as half the number of switching instances during one period of fundamental frequency of the network. Hence, a pulse number of \(PN = 2\) corresponds to four switching instances during a fundamental period of 0.02 s. The switching signal corresponding to \(PN = 2\) is depicted in Fig. 4. For simplicity, the concepts in this study are illustrated for one of the submodules rather than the entire converter. All the solutions presented in this study can be directly applied to all submodules of MMCs.

For each capacitor submodule, after detecting the transition of the dc capacitor current from zero to a nonzero value using (2), the initial capacitor voltage \(v_{C,t_1}\) is recorded. This time is named \(t_1\) in Fig. 5, which is a close-up of one of the switching transitions shown in Fig. 4. At \(t = t_1\), the integration of current passing through the capacitor is initiated. At an arbitrary time \(t = t_2 > t_1\) within the same conduction phase of the submodule capacitor, the second capacitor voltage \(v_{C,t_2}\) is recorded and the capacitor current integration is stopped. For this conduction phase, the capacitance value can be estimated by substituting \(v_{C,t_2} - v_{C,t_1}\), and \(\int_{t_1}^{t_2} i_C \, dt\) in (2) with measured values. This process is repeated over time in order to identify variations in the capacitance value of each submodule. The equations shown so far are designed to extract the capacitance of dc capacitors in full-bridge modules. In order to apply these equations—and the algorithms in the following chapters—to half-bridge submodules, it is sufficient to set \(s_4 = 0\) and \(s_3 = 1\) in (2) and (3), respectively. With this change, all other algorithms can be used directly for half-bridge modules as well.

**B. Effect of Measurement Noise on Estimated Capacitance Values**

Voltage and current measurements are subject to measurement noise. Noise can significantly distort the estimated capacitance.
value. In this article, what is referred to as measurement noise is the amalgamation of all noises present in the system that appear on the measured voltages and currents. That is, the measurement noise consists of the noises within the measurement system, as well as the coupling noises from the surrounding environment. The source of these external noises may for example be switching transients in adjacent modules. The noise levels used in this article are deducted from MMCs during operation in order to incorporate the effect of all noise sources in the system. In this article, a Gaussian white noise is considered for both current and voltage measurements. The choice of Gaussian white noise is based on observations made on recorded voltage and current measurements over a long window of time. For the voltage and current measurements, the maximum noise level observed is 0.5% and 1% of their nominal value, respectively. These values are extracted from voltage and current measurements of a high-power MMC-based D-STATCOM in operation. The method used for extracting the noise content is presented in Section V-D, where the measurement noise of the low-power prototype is calculated. These two modifications are illustrated in Fig. 7.

C. Practical Considerations for Reduction of Error Caused by Measurement Noise

From (3), it is clear that minimizing the error in the estimated capacitance of submodules requires maximizing the SNR of both $\Delta V_C$ and $\int i_C dt$. To maximize the SNR of $\Delta V_C$, the time $t_2$ in Fig. 5 is chosen to be at the zero-crossing of the arm current. This is due to the fact that the current zero-crossing coincides with the capacitor voltage extrema in MMC-based D-STATCOMs. If the switching signals change before the current zero-crossing is achieved, the last measured current passing through the capacitor is used for the estimation.

To further reduce the effect of noise, the estimation algorithm is designed only to keep estimated capacitance values when the current measurement is at least 20% of its nominal value. Furthermore, a time margin has been defined before initiating the data acquisition, i.e., before $t_1$. This time margin assures that the data acquisition starts after switching transients have damped out. In this study, the time margin is defined to be 100$\mu$s. These two modifications are illustrated in Fig. 7.

D. Practical Considerations for Reduction of Error Caused by Data Skewing

Data skewing is the effect of a relative time delay between two sets of measured data. This time difference is caused by different delays in the paths of various measurement data. The skewing in different measurements can be another source of erroneous capacitor estimation, as the skewed voltage and current data are not a linear function of one another. In low-frequency MMC applications, this error can be identified and compensated for by...
Despite all practical considerations for noise reduction, it is still not possible to rely on a single estimated value. This is because of the high spread of data, and the presence of outliers in the estimated capacitance values. Consequently, postprocessing of the estimated capacitance values is necessary. In this study, four postprocessing methods, namely, moving-average, moving-median, RLS, and low-pass filtering are studied and compared. The moving-average and moving-median methods require a large amount of memory, while the RLS algorithm requires more processing power. It is also possible to utilize modified low-pass filters (MLPFs), which have the advantage of low memory requirement and low processing power, but show lower accuracy in the presence of nonuniform outliers. The four methods are described as follows:

1) Moving-Average and Moving-Median Filters: In the moving-average and moving-median methods, the individually estimated values are initially transmitted to and stored in a memory. Every time a new estimated data point is available, the memory array is shifted by one element, eliminating the earliest data point in the array and updating the last element of the array with the most recent measurement. This process creates a moving window containing the last 100 estimated values. In the moving-average method, the array of estimated data are averaged every time a new value is inserted in the moving window. This average value represents the estimated capacitance at each time. This method can provide good filtering if the estimated values are closely grouped, and are located uniformly around the actual capacitance value. Otherwise, low-probability outliers can strongly affect the outcome of a moving-average filter resulting in low estimation accuracies. Alternatively, the median of the elements in a moving window can be used as a filter for estimated capacitance values. This method is less susceptible to outliers among the estimated values. However, it is more computationally intensive than the moving-average method. Simulation studies show that, under the operational conditions presented in Fig. 9, a maximum estimation error of approximately 2.5% is observed for both the moving-median and moving-average filters. For smaller windows of moving-average or moving-median filters, lower estimation accuracies are achieved.

2) Special Low-Pass Filter: The individually estimated capacitance values can also be filtered via a special low-pass filter. Since the estimated capacitance values are not necessarily updated with a constant frequency, an enabling signal is utilized such that the low-pass filter is only triggered when a new data point is available. As a result, the filter manipulates the data to appear as if they are updated with a constant frequency. The virtual updating rate of the estimated data is realized by an arbitrary digital time step of $t_s$. The arbitrary time step $t_s$ used for creating the digital filter will only have the effect of compressing or expanding the estimated capacitance dataset in a virtual time frame. Since the dc and low-frequency content of the estimated dataset are required, the choice of the arbitrary $t_s$ will only result in smoother filtered data for small values of $t_s$ and vice versa. In this section, a first-order low-pass filter with two virtual time constants of $\tau = 200$ s, and $\tau = 2000$ s is considered. Moreover, an arbitrary digitization time of $t_s = 1$ s is opted. This filter is discretized via the Tustin transformation method as follows:

$$H(s) = \frac{1}{1 + 8\tau}$$

$$H(z^{-1}) = \frac{1 + z^{-1}}{(1 + \frac{2\tau}{t_s}) + (1 - \frac{2\tau}{t_s})z^{-1}}$$  \(4\)
where \( z \approx \frac{1 + s \frac{\tau}{2}}{1 - s \frac{\tau}{2}} \).

The ratio \( \tau / \tau_s \) defines the smoothing factor of this filter. Fig. 9 illustrates the filtering effect of the proposed low-pass filter. Clearly, for higher values of \( \tau \), a lower estimation error can be expected. However, a higher \( \tau \) results in a longer settling time of the filter’s output. Similar to the moving-average filtering method, a nonuniform spread of data, or existence of a significant number of outliers can adversely affect the output of the proposed low-pass filter. On the other hand, unlike the moving-window algorithms, the MLPF does not require additional memory in order to create a smoother output. In fact, the MLPF only utilizes two memory slots, regardless of the chosen virtual time constant \( \tau \). In the simulation study described in Fig. 9, an estimation error of 1.7% and 1.24% is observed for the virtual time constants of \( \tau = 200 \) s and \( \tau = 2000 \) s, respectively.

3) RLS Estimation for Error Reduction: The RLS estimation algorithm is adopted as the fourth method for reducing the effect of noise on the estimated capacitance values. This method has a higher computational intensity than the moving average method. However, it has the advantage of utilizing less memory resources compared to the moving window algorithms, and can provide optimal adaptation of the estimated value to the actual capacitance. A general diagram of the RLS estimator is presented in Fig. 10. The RLS estimator aims to find the best linear time-independent model that mimics the behavior of a physical system. In this article, the RLS estimator aims to estimate a capacitance value that best represents the relationship between the capacitor current integration, \( \int i_C dt \), and the capacitor voltage variation, \( \Delta v_C \), in a sequence of measurement intervals. This is done by continuously updating the estimated capacitance value based on the error between the measured capacitor current integration, \( \int i_C dt \), and the estimated capacitor current integration, \( \int \hat{i}_C dt \).

The general algorithm of the RLS estimator shown in Fig. 10 is described in Algorithm 1. The RLS estimator only utilizes two additional memories, namely \( K[n] \) and \( P[n] \). The forgetting factor, \( \lambda \leq 1 \), defines the filtering strength of the RLS output. For larger values of \( \lambda \), a smoother output is achieved, while the settling time of the output is increased. In this study, three forgetting factors of \( \lambda = 0.99 \), 0.997, and 0.999 are considered. Similar to the proposed low-pass filter, the RLS estimator is only updated when a new estimated data point is available. Estimated values using the proposed RLS estimator are presented in Fig. 9, where an estimation error of 0.86% is observed for when \( \lambda = 0.999 \). An RLS-based approach for capacitor estimation has also been proposed in [13]. However, that solution is not suitable for MMC-based STATCOMs, which typically operate at low switching frequencies. The reason is that the data acquisition period in that study is considered to be the entire conduction period of a submodule. As shown in Fig. 5, using the entire conduction period for low switching frequencies may result in voltage variations close to zero, i.e., \( \Delta v_C \approx 0 \). Consequently, a very low SNR will be achieved for \( \Delta v_C \). Moreover, the effect of measurement noise is not studied in [13]. For the high switching
frequencies presented in that study, low SNRs are expected for both \( \Delta V_C \) and \( \int i_C \, dt \) in a practical setup.

4) Combined Filtering: In order to increase the capacitance estimation accuracy, the output of the moving-median, moving-average, and RLS estimators can be further filtered with the proposed MLPF. Combining these filters allows for utilizing the advantages of different methods. Specifically, the lower susceptibility of the moving-median and RLS filters to outliers can be combined with the smoothing effect of the MLPF. The effect of the combined filtering is summarized in Table II. It can be concluded from Table II that the combined filtering strategy provides much better estimations for the moving-window approaches compared to when only a single filter was used. Since the RLS estimator has a filtering effect incorporated in its design, the addition of the MLPF has a similar effect to changing \( \lambda \) in the RLS algorithm. Therefore, it is more efficient to manipulate \( \lambda \) in the RLS algorithm than to add a MLPF to its output.

5) Overall Estimation Algorithm: The RLS estimation algorithm is chosen as the best estimation method due to providing the lowest estimation error, requiring the lowest number of memory slots, and being less sensitive to outliers. The combination of RLS estimation together with the MLPF (RLS-MLPF) is also a suitable option for further reducing the fluctuations of the RLS estimator’s output. However, as the value of \( \lambda \) gets closer to 1, the combined MLPF becomes less effective and can be omitted.

In this article, all the individually estimated capacitances are recorded and processed. However, not all the estimated values need to be recorded. That is, the rate at which the estimated values are recorded can be significantly lower than that of the estimation rate. This option can alleviate harsh requirements on the allocated memory for such recordings.

IV. COMPARISON WITH STATE-OF-THE-ART SOLUTIONS

Previous studies conducted on dc capacitor estimation for MMC applications are summarized in Table III. State-of-the-art methods utilize measurement sensors in order to directly or indirectly identify the health state of the capacitors. Clearly, degradation of the sensors themselves can create faulty estimations of the capacitor’s health state. However, if estimated values are affected as a result of sensor degradation, and it is determined during the maintenance session that the corresponding capacitor is actually healthy, degradation of the sensors can be identified. Considering the design constraints of MMCs used in FACTS and HVdc applications, the most suitable state-of-the-art solution for dc capacitor estimation is the one proposed in [15]. Hence this solution is chosen for a more detailed comparison study. Liu et al. [15] utilizes a unique method for extracting the amplitude of the fundamental-frequency component of the capacitor voltage, and capacitor current. This is achieved by first multiplying the measured signals by a sine and cosine waveform of fundamental frequency. Then, in order to reduce the effect of noise, the outputs of the multiplications are integrated over a number of fundamental periods. Finally, a division of the extracted fundamental voltage and current values identifies the capacitance of each

| Method | Computational intensity | Noise immunity | Low switching frequencies | High switching frequencies | Special operation |
|--------|-------------------------|----------------|--------------------------|--------------------------|------------------|
| Ref [9] | Low \(^a\) | No | No | Yes | Yes |
| Ref [26] | Low | No | No | Yes | No |
| Ref [7] | Low | No | No | Yes | No |
| Ref [27] | Low | No | No | Yes | Yes |
| Ref [14] | Medium \(^b\) | Yes | Yes | * | * |
| Ref [18] | Medium \(^b\) | Yes | Yes | Yes | No |
| Proposed solution | Medium | Yes | Yes | Yes | No |

(a) Colors represent the strength of the decision. Green and red strongly support the selected decision, while orange states a relative or conditional strength. (b) The computational intensity is only slightly higher. (c) Under certain conditions presented in Section IV-B. (d) Not thoroughly assessed in [14]. (e) Up to practical switching frequencies described in Section V-C.
Fig. 11. Noise sensitivity of estimation algorithms when a carrier frequency of 87.37 Hz is opted. (a) Noise sensitivity of the RLS estimation method at a fixed load of 30%. (b) Noise sensitivity of the method in [15] at a fixed load of 30%, and \( N_{per} = 100 \). (c) Noise sensitivity of the method in [15] at a fixed load of 30%, and \( N_{per} = 200 \). (d) Noise sensitivity of the RLS estimation method at a variable load of 30% ± 30%. (e) Noise sensitivity of the method in [15] at a variable load of 30% ± 30%, and \( N_{per} = 100 \). (f) Noise sensitivity of the method in [15] at a variable load of 30% ± 30%, and \( N_{per} = 200 \).

submodule. This method is summarized as follows:

\[
A_{vc} = \int_0^{N_{per}T_0} v_c(t) \cdot \cos(\omega_0 t) dt \\
B_{vc} = \int_0^{N_{per}T_0} v_c(t) \cdot \sin(\omega_0 t) dt \\
A_{ic} = \int_0^{N_{per}T_0} i_c(t) \cdot \cos(\omega_0 t) dt \\
B_{ic} = \int_0^{N_{per}T_0} i_c(t) \cdot \sin(\omega_0 t) dt \\
C = \sqrt{A_{vc}^2 + B_{vc}^2} \\
\omega_0 \sqrt{A_{ic}^2 + B_{ic}^2}.
\]

(5)

From the perspective of computational intensity, the proposed solution, and that in [15] have a comparable number of arithmetic commands. Both solutions require divisions, which is computationally intensive if they are performed in an FPGA, and they both require a similar number of multiplications and additions. The method in [15] requires two square root functions, while the proposed method has one additional division. The most apparent computational difference between the proposed solution and that of [15] is that the proposed solution uses the switching function in order to identify the times at which the current passes through each submodule capacitor. However, this is just a logical command, and does not require intensive computation, neither in FPGAs, nor in DSPs. Hence the computational intensity of the proposed solution and that of [15] are similar. The computational intensity of both the proposed solution and that of [15] are higher than the methods proposed in [7], [9], [14], [15], [26], [27], simply due to the higher number of mathematical operations. However, conducting such elementary arithmetics in state-of-the-art control hardware is uncomplicated.

With similar computational complexities, it is important to compare the efficacy of state-of-the-art solutions under different conditions. In this study, different switching frequencies, and different measurement noise levels are considered for the comparison study. In [15], it is suggested that integrating over \( N_{per} = 100 \) periods provides sufficient damping of measurement noise in the system. Therefore, \( N_{per} = 100 \) is chosen for the comparison study conducted in this section. Two study cases are considered: 1) different measurement noise—in capacitor voltage and currents—while the converter is operating at a fixed load, and 2) different measurement noise—in capacitor voltage and currents—while the converter’s load is varying. In order to have a fair comparison, similar to [15], a phase-shifted carrier modulation is used. In this study, a carrier frequency of 87.37 Hz per phase leg is considered to reflect the low switching frequency of MMCs. Moreover, a forgetting factor of \( \lambda = 1 - 1e^{-5} \) is considered for the RLS algorithm.

A. Comparison of Measurement Noise Effect at Constant Load

For this study, the converter is set to operate at 30% load while the voltage and current noise levels are varied as shown in Fig. 11(a)–(c). In the proposed solution, the estimation error is affected more by the voltage measurement noise than the current measurement noise. This is apparent from (3) as well, since the current is integrated in the time frame between \( t_1 \) and \( t_2 \), while only two points of voltage at \( t_1 \) and \( t_2 \) are used for the estimation. Nevertheless, the estimation errors of both the proposed solution and that presented in [15] are acceptable for reasonable levels of noise presented in Fig. 11(a)–(c).
B. Comparison of Measurement Noise Effect at Varying Load

In this scenario, the converter is set to operate at a 30% fixed load in addition to a 30% fluctuating load. The fluctuating load is a 30% load that is switched in and out every 1 s of operation. The voltage and current noise levels are varied similar to the previous scenario, and the estimation errors using the two methods are summarized in Fig. 11(d)–(f). It is apparent that the solution proposed in [15] shows slightly larger errors; albeit, still within an acceptable range. The reason for this slight increase in estimation error is that load fluctuations in combination with the low switching frequency create low frequency harmonic content on the capacitor voltages. Low frequency voltage fluctuations as a result of low switching frequencies are explained in [1] and [28]. These low frequency contents temporarily affect the extracted fundamental components in (5). Theoretically, (6) should have zero error for an infinitely large number of integration periods, i.e., $N_{\text{per}} \to \infty$. It is observed that increasing the integration window to $N_{\text{per}} = 200$ cycles reduces the error to the values presented in Fig. 11(f). The best relation between the type of load fluctuation and the minimum value of $N_{\text{per}}$ is not investigated in this study. As shown in Fig. 11(d), for the same simulation scenario, the estimation errors of the proposed method in this article are slightly improved due to the higher average load current provided by the variable load. The proposed solution is intended for MMCs with low switching frequencies. In high switching frequencies, the time period between each two switching actions, i.e., $t_2 - t_1$ becomes small. Theoretically, for an infinitely high switching frequency, the estimator will not record any estimation results. In Section V, the proposed solution has shown to be effective for pulse numbers up to $PN = 12$ for the conditions considered in this article.

V. SIMULATION AND EXPERIMENTAL RESULTS

In this section, simulation and experimental studies of the proposed dc capacitor estimation algorithm are presented. The simulation studies are conducted under various load conditions, and at two different switching frequencies. Furthermore, the efficacy of the proposed solution is studied on a double-Y converter topology. The parameters of the double-Y MMC are chosen to match that of the low-power prototype described in [29].

A. Simulation Results of the D-STATCOM Topology at Low Switching Frequency of $PN = 2$ Under Varying Conditions

It is vital that the capacitance estimation accuracy is not deteriorated under various load currents of the converter. In this section, the proposed capacitor estimation algorithm is studied for when the converter is operating at different loads while maintaining a fixed pulse number of $PN = 2$. The load is varied from 20% to 100% at 20% intervals. Simulation results for this study are presented in Fig. 12. It is evident that for higher current levels, better grouping of the estimated capacitance values is achieved. This is due to the higher SNR of capacitor voltage and current measurements at higher load currents. Furthermore, simulation results prove that the proposed algorithm of the RLS estimator can successfully identify the dc capacitance value with less than 1% over a wide range of loads. In the RLS estimation method, the highest fluctuation in estimated values corresponds to low-current operation modes.

In a second study, the submodule capacitance of one cell is virtually manipulated to first 98% and then to 95% of its initial value, in order to represent capacitor degradation. As depicted in Fig. 13, the proposed RLS algorithm correctly identifies these changes with less than 1% error, while the converter is operating at 20% load capacity.
B. Simulation Results of the D-STATCOM Topology at High Switching Frequency of $PN = 6$ Under Varying Conditions

Although the proposed algorithm has proven to be effective for low switching frequencies, it is also suitable for when higher switching frequencies are opted. In this section, a pulse number of $PN = 6$ is considered for the proposed MMC-based D-STATCOM. Compared to the case when a $PN = 2$ was used, the pulses are relatively shorter. Also, there are fewer pulses in which the current zero-crossing occurs when the arm current is passing through the submodule capacitor. Consequently, for higher switching frequencies, the SNR becomes worse than that in low switching frequency operations. As a result, lower estimation accuracies are expected, especially when the converter is operating at low currents. On the other hand, compared to when low switching frequencies are used, the number of estimated capacitance values is higher. Hence, during high current operation, the combined effect of a relatively higher SNR ratio, and a high number of estimated values leads to similarly accurate estimations compared to when low pulse numbers are used. As illustrated in Fig. 14, despite the relatively higher switching frequency, the proposed RLS algorithm accurately estimates the submodule capacitance for a wide range of load currents.

C. Simulation Results of the D-STATCOM Topology at Fixed Load and Varied Switching Frequency

A simulation study is conducted to identify the capacitance estimation errors at different switching frequencies. The results are summarized in Fig. 15. For pulse numbers higher than 12—and the conditions presented in Fig. 15—the RLS-based approach is not a suitable candidate for dc capacitance estimation. For higher switching frequency operations, the solution proposed in [15] is preferred. Although, requirements on switching losses make switching frequencies higher than $PN = 6$ impractical for high-power MMCs. The estimation accuracy of the proposed method and that of [15] are stated to be similar in Table III for most regions of operation. However, as illustrated in Fig. 11, depending on the switching frequency and load conditions, one method can take precedence over the other.

D. Simulation Results on the Double-Y Topology

The proposed estimation algorithm can be incorporated in various MMC-based topologies. In this section, the estimation algorithm is studied on a double-Y converter topology shown in Fig. 16. This topology—with the parameters stated in Table IV—is used for experimental validation. The control system used for this study is thoroughly explained in [30]. The measurement noise in this setup is extracted from the ADC measurements recorded in the control hardware. For the voltage noise, the times during which the submodule is bypassed is studied. When a submodule is bypassed, the capacitor voltage is stable and can only discharge with a large time constant (approximately 100 s in this setup). Hence, the variations of measured voltage during the bypass time of the converter is attributed to measurement noise. This is shown Fig. 17. In the prototype used for this study, it was observed that the maximum voltage noise is $\pm 0.2$ V regardless of the dc voltage level of the submodule capacitor. This corresponds to the least significant bit (LSB) of the ADC module. Therefore, a measurement noise of $\pm 0.2$ V is considered in the simulations.
Considering that each cell is charged to approximately 40 V, the voltage measurement noise level is at 0.5%. The reason for such low levels of voltage measurement noise is that the ADC is typically placed very close to the capacitor module. Since the dc capacitor itself acts as a voltage filter, in the short distance between the ADC and the capacitor, an insignificant amount of noise is coupled with the measurement circuit.

In order to identify the level of noise in the current measurement, the recorded current in the control hardware is compared to a reference value. Similar to the voltage measurement noise, the noise levels in the current measurements were not affected by the current magnitude. Current measurement noise is identified to be less than 0.4 A, corresponding to 0.8% of the full-load current in the MMC prototype. Two simulation studies are conducted on the double-Y topology considering the identified levels of measurement noise in the setup. One at a low pulse number of PN ≈ 3 and one at PN ≈ 6. In both cases, the load is varied from 1.5 to 3 kVAR at steps of 500 VAR. The estimation results for one cell is presented in Fig. 18. The estimation error in both cases is less than 1%. The number of estimated samples is clearly less when PN ≈ 3 due to the lower number of switching events.

E. Experimental Results

The proposed estimation algorithm is applied to a low-power double-Y-STATCOM prototype shown in Fig. 19. The prototype consists of five full-bridge submodules per arm, and is controlled using a Xilinx Zynq 7000 evaluation board. The design and operation of this prototype is thoroughly explained in [29]. As shown in Fig. 20, the submodule capacitors of this prototype consist of 10 parallel connected capacitor units of 270 μF ± 20% each. Three scenarios are considered for the experimental results on the double-Y prototype. In the first scenario, under fixed load conditions a submodule capacitor is manually reduced. This reduction in capacitance is then estimated by the proposed algorithm. In the second and third scenario, the estimation algorithm is tested at two different switching frequencies while the MMC is subject to a variable load.

1) Manual Capacitor Variation: In order to test the efficacy of the proposed algorithm in identifying variations in the dc
capacitance, estimated capacitance values were extracted once when all capacitor units of the submodule were in place, and once when one of the units was removed. For each scenario, the prototype was operating for 200 s at 30% nominal current, and with a pulse number of PN ≈ 5 per submodule. The upper arm voltage and current waveforms for these operational points of the converter are shown in Fig. 22. Even though the proposed estimation algorithm works better at lower pulse numbers, PN ≈ 5 was chosen due to the low number of submodules in each phase of the prototype. These experimental results are depicted in Fig. 21. It can be seen that the algorithm estimates a value of 2349 μF for all ten units, and 2105 μF for when one unit is removed. This results in a difference of 230 μF, or 9.79%. Offline measurements of the submodule capacitor were conducted using an RLC meter, and summarized in Table V. It is observed that the deviation of capacitance is estimated with an error of 0.13%.

2) Various Operational Conditions: The submodule capacitance is estimated at two different pulse numbers of PN ≈ 3 and PN ≈ 6 while the converter load is varying. In the case where PN ≈ 6 is used, the load varies from 1.5 to 3.5 kVAR in steps of 500 VAR. In the case of PN ≈ 3, the load is switched more frequently between 1.8 and 3 kVAR. The results of these two
### Table V

| Capacitor     | Offline measurement [μF] | Online estimation [μF] | Online estimation% | Estimation error [%] |
|---------------|--------------------------|------------------------|--------------------|---------------------|
| 10-unit submodule | 2349                     | 2335                   | 99.40              | 0.60                |
| 9-unit submodule  | 2116                     | 2105                   | 98.61              | 0.47                |
| Removed unit   | 233                      | 230                    | 97.79              | 0.13                |

* The base value for perunitizing the estimations is 2349 μF.

---

**VI. CONCLUSION**

In this article, a health estimation algorithm for dc capacitors in MMCs is proposed. The proposed algorithm does not require additional sensors and is able to reduce the effect of measurement noise on the estimated capacitance values. Moreover, the proposed algorithm can operate independently without interfering with the normal operation of the converter. Simulation and experimental results show that the capacitance—and therefore, the health state—of all submodule capacitors can be estimated with a maximum error of 1% when respecting the estimation conditions presented in this study. The proposed solution is also compared with suitable state-of-the-art methods, showing comparable estimation errors. The proposed solution is especially deemed suitable for FACTS applications, where low switching frequencies are opted and frequent load variations are expected.

---

**ACKNOWLEDGMENT**

The authors would like to thank Hitachi-ABB Power Grids, Västerås, Sweden, for their technical and financial support.

---

**REFERENCES**

[1] K. Ilves, A. Antonopoulos, S. Norrga, and H.-P. Nee, “A new modulation method for the modular multilevel converter allowing fundamental switching frequency,” *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3482–3494, Aug. 2012.

[2] J. Qin and M. Saedifard, “Reduced switching-frequency voltage-balancing strategies for modular multilevel HVDC converters,” *IEEE Trans. Power Del.*, vol. 28, no. 4, pp. 2403–2410, Oct. 2013.

[3] K. Ilves, S. Norrga, L. Harnefors, and H.-P. Nee, “On energy storage requirements in modular multilevel converters,” *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 77–88, Jan. 2014.

[4] D. Li et al., “Explosion mechanism investigation of high power IGBT module,” in *Proc. 19th Int. Conf. Thermal, Mech. Multi-Phys. Simul. Experiments Microelect. Microsyst.*, 2018, pp. 1–5.

[5] M. Billmann, D. Malipaard, and H. Gambach, “Explosion proof housings for IGBT module based high power inverters in HVDC transmission application,” in *Proc. PCIM Eur. Conf.*, Nuremberg, 2009, pp. 352–257.

[6] B. Ødegård, D. Weiss, T. Wikström, and R. Baumann, “Rugged MMC converter cell for high power applications,” in *Proc. 18th Eur. Conf. Power Electron. Appl.*, 2016, pp. 1–10.

[7] D. Ronanki and S. S. Williamson, “Failure prediction of submodule capacitors in modular multilevel converter by monitoring the intrinsic capacitor voltage fluctuations,” *IEEE Trans. Ind. Electron.*, vol. 67, no. 4, pp. 2585–2594, Apr. 2020.

[8] Z. Wang, Y. Zhang, H. Wang, and F. Blaabjerg, “Capacitor condition monitoring based on the dc-side start-up of modular multilevel converters,” *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5589–5593, Jun. 2020.

[9] H. Wang, H. Wang, Y. Zhang, Z. Wang, X. Pei, and Y. Kang, “Condition monitoring method for submodule capacitor in modular multilevel converter,” in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2019, pp. 344–348.

[10] N. Agarwal, M. W. Ahmad, and S. Anand, “Quasi-online technique for health monitoring of capacitor in single-phase solar inverter,” *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5283–5291, Jun. 2018.

[11] N. Yu, S. Shao, X. Wu, J. Zhang, and H. Chen, “Application of tunnel magnetoresistance to health monitoring of modular multilevel converter submodules,” in *Proc. IEEE Int. Power Electron. Appl. Conf. Expo.*, 2018, pp. 1–5.

[12] Q. Pu, L. Qin, Q. Wang, J. Le, and K. Liu, “Online monitoring and balancing for MMC capacitor aging,” in *Proc. 4th IEEE Workshop Electron. Grid*, 2019, pp. 1–6.
[13] O. Abushafta, S. Gadoue, M. Dahidah, and D. Atkinson, “A new scheme for monitoring submodule capacitance in modular multilevel converter,” in Proc. 8th IET Int. Conf. Power Electron., Mach. Drives, 2016, pp. 1–6.

[14] K. Wang, L. Jin, G. Li, Y. Deng, and X. He, “Online capacitance estimation of submodule capacitors for modular multilevel converter with nearest level modulation,” IEEE Trans. Power Electron., vol. 35, no. 7, pp. 6678–6681, Jul. 2020.

[15] C. Liu, F. Deng, Q. Yu, Y. Wang, F. Blaabjerg, and X. Cai, “Submodule capacitance monitoring strategy for phase-shifted carrier pulse-width modulation based modular multilevel converters,” IEEE Trans. Ind. Electron., vol. 68, no. 9, pp. 8753–8767, Sep. 2021.

[16] S. Sinsel, I. Ramsay, W. Hörger, A. Janke, and M. A. Alegría, “Multilevel STATCOMs—a new converter topology that opens up the market,” in Proc. IEEE PES T&D Conf. Expo., 2014, pp. 1–5.

[17] S. Chou et al., “Average power balancing control of a STATCOM based on the cascaded h-bridge PWM converter with star configuration,” in Proc. IEEE Energy Convers. Congr. Expo., 2013, pp. 970–977.

[18] F. Z. Peng and J. Wang, “A universal STATCOM with delta-connected cascade multilevel inverter,” in Proc. IEEE 35th Annu. Power Electron. Specialists Conf., vol. 5, 2004, pp. 3529–3533.

[19] N. Thitichaiworakorn, M. Hagiwara, and H. Akagi, “Experimental verification of a modular multilevel cascade inverter based on double-star bridge cells,” IEEE Trans. Ind. App., vol. 50, no. 1, pp. 509–519, Jan./Feb. 2014.

[20] A. Hassanpoor, S. Norrga, H.-P. Nee, and L. Ångquist, “Evaluation of different carrier-based PWM methods for modular multilevel converters for HVDC application,” in Proc. IEEE IECON 38th Annu. Conf. Ind. Electron. Soc., 2012, pp. 388–393.

[21] S. Sirisukprasert, A. Q. Huang, and J. Lai, “Modeling, analysis and control of cascaded-multilevel converter-based STATCOM,” in Proc. IEEE Power Eng. Soc. Gen. Meeting, vol. 4, 2003, pp. 2561–2568.

[22] M. Hagiwara, R. Maeda, and H. Akagi, “Negative-sequence reactive-power control by a PWM STATCOM based on a modular multilevel cascade converter (MMCC-SDBC),” IEEE Trans. Ind. App., vol. 48, no. 2, pp. 720–729, Mar./Apr. 2012.

[23] H. Saad, X. Guillaud, J. Mahsereedian, S. Denetrière, and S. Nguenue, “MMC capacitor voltage decoupling and balancing controls,” IEEE Trans. Power Deliv., vol. 30, no. 2, pp. 704–712, Apr. 2015.

[24] M. Makdessi, A. Sari, and P. Venet, “Health monitoring of dc link capacitors,” Chem. Eng. Trans., vol. 33, pp. 1105–1110, 2013.

[25] H. Soliman, H. Wang, and F. Blaabjerg, “A review of the condition monitoring of capacitors in power electronic converters,” IEEE Trans. Ind. App., vol. 52, no. 6, pp. 4976–4989, Nov./Dec. 2016.

[26] F. Deng, Q. Wang, D. Liu, Y. Wang, M. Cheng, and Z. Chen, “Reference submodule based capacitor monitoring strategy for modular multilevel converters,” IEEE Trans. Power Electron., vol. 34, no. 5, pp. 4711–4721, May 2019.

[27] Y. Jo, T. H. Nguyen, and D. Lee, “Condition monitoring of submodule capacitors in modular multilevel converters,” in Proc. IEEE Energy Convers. Congr. Expo., 2014, pp. 2121–2126.

[28] K. Ilves, A. Antonopoulos, L. Harnefors, S. Norrga, and H.-P. Nee, “Circulating current control in modular multilevel converters with fundamental switching frequency,” in Proc. 7th Int. Power Electron. Motion Control Conf., vol. 1, 2012, pp. 249–256.

[29] L. Bessegato, A. Nairula, P. Bakas, and S. Norrga, “Design of a modular multilevel converter prototype for research purposes,” in Proc. 20th Eur. Conf. Power Electron. Appl., 2018, pp. 1–10.

[30] M. Nahalparvari, M. Asoodar, L. Bessegato, S. Norrga, and H.-P. Nee, “Modeling and shaping of the dc-side admittance of a modular multilevel converter under closed-loop voltage control,” IEEE Trans. Power Electron., vol. 36, no. 6, pp. 7294–7306, Jun. 2021.

Mohsen Asoodar

Mehrdad Nahalparvari

Mehrdad Nahalparvari (Student Member, IEEE) received the M.Sc. degree in power electronics from Tampere University, Tampere, Finland, in 2019. He is currently working toward the Ph.D. degree in electrical engineering with KTH Royal Institute of Technology, Stockholm, Sweden.

His research interests include modeling and control of power electronic converters.

Rasmus Söderström received the M.Sc. degree from Uppsala University, Uppsala, Sweden, in 2020.

He conducted his M.Sc. thesis work in collaboration with the FACTS unit of Hitachi-ABB Power Grids, Sweden, on predictive maintenance of high-power STATCOMs. He is currently working at SAAB AB, as a System Developer. His main interests include digital signal processing and FPGA development.

Hans-Peter Nee (Fellow, IEEE) was born in Västerås, Sweden, in 1963. He received the M.Sc., Licentiate, and Ph.D. degrees in electrical engineering from the Royal Institute of Technology (KTH), Stockholm, Sweden, in 1987, 1992, and 1996, respectively.

Since 1999, he has been a Professor of power electronics with the Department of Electrical Engineering, KTH. His research interests include power electronic converters, semiconductor components, and control aspects of utility applications, such as flexible ac transmission systems and high-voltage direct-current transmission, and variable-speed drives.

Dr. Nee was a member of the Board of the IEEE Sweden Section for many years and was the Chair of the Board from 2002 to 2003. He is also a member of the European Power Electronics and Drives Association and is involved with its Executive Council and International Scientific Committee.