A Non-Inverting High Gain DC-DC Converter With Continuous Input Current

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ABSTRACT High gain DC-DC converters are increasingly being used in solar PV and other renewable generation systems. Satisfactory steady-state and dynamic performance, along with higher efficiency, is a pre-requisite for selecting the converter for these applications. In this paper, a non-inverting high gain DC-DC boost converter has been proposed. The proposed converter has only one switch with continuous input current and reduced voltage stress across switching devices. The operating range of the duty cycle is wider, and it obtains a higher gain at a lower value of the duty cycle. Moreover, the converter has higher efficiency at a lower duty cycle while drawing a continuous input current. The continuous input current is a desirable feature of the dc-dc converter making it suitable for solar photovoltaic applications. The converter’s operation has been discussed in detail and extended to include the real circuit parameters for a practical performance evaluation. The proposed converter has been compared with other similar recently proposed converters on various performance parameters. The loss analysis for the proposed converter has also been carried out. Finally, the simulation has been validated with results from the experimental prototype.

INDEX TERMS Continuous conduction mode, duty cycle, high gain, DC-DC boost converter, voltage stress.

I. INTRODUCTION

For sustainable development, renewable energy is going to play a significant role in energy generation. The generation of electricity by solar PV system for grid-connected and off-grid application has already proven to be the game-changer in the energy market scenario [1]–[3]. While the transportation system is also seeing a shift, with electric vehicles promising to be the future’s commutation system. Fuel cells are increasingly being used for electric transportation system [4]. However, both solar PV and fuel cells produce low voltage which is required to be boosted up for practical applications [5]. Therefore, a high voltage gain DC-DC converter is an integral part of the solar PV generation and electric vehicle system. Boost DC-DC converters are also used high-intensity headlamps in automobiles, uninterruptible power supply, motor drives, and many others [6]–[9]. Power converters are used for applications ranging from few watts in a smart battery charging system to hundreds of kilowatts in a converter station in an HVDC transmission system.

The conventional boost converter is not suitable for a very high voltage gain as it achieves high voltage gain at a high value of the duty cycle. A higher value of duty cycles mounts the problems for transient response [10], [11]. And Another demerit of the converter’s operation at extreme duty cycle is that enough time is not provided to transfer the stored energy of inductor and capacitor for a diode with reverse recovery time [12]. The conventional boost converter (CBC) is reduced significantly at higher duty ratios because of voltage drops across diodes, switches, and equivalent series resistance of capacitors and inductors [13]. The converter’s efficiency depends on the number of the components present in the circuit, their conduction time as well as on switching frequency [14].
Several topologies of DC-DC converter with isolation using high-frequency transformer are proposed in the literature. High voltage gain is achieved by raising the transformer’s turn ratio but due to the transformer the cost, size, and weight of the converter increases. Moreover, transformers also introduce non-idealities in the system. Sometimes the leakage inductance of coupled inductor can also create a problem of current transients through the switch [15], [16]. High voltage gain could be achieved using coupled inductors, but a clamp circuit needs to be designed [17], [18]. The converter efficiency can decrease in the two-stage operation of the converters with coupled inductor because of reverse recovery issues and leakage inductance if the energy stored in the leakage inductance is not properly utilized [19].

Two or more converters can be connected in series to achieve a high voltage gain, but this increases the number of passive components in the circuit. The converter’s operation with a large number of components at an extreme duty ratio increases the power loss, which is not appreciable [10], [20], [22]. In [22] switched inductors and capacitors are used to synthesize new hybrid converters. Switched capacitors topologies although draws higher current in charging the capacitors are more popular than switched inductor topologies owing to small size and better voltage gain. In [23], two converters are cascaded which has a quadratic gain slightly greater than that of the conventional quadratic boost. The converter proposed by Fardoun and Ismail [24] has a single switch with two inductors, and that has extended from the relief circuit [25]. The converter has a high voltage gain but also has high voltage stress on the switches. In [26], authors have proposed a single switch quadratic voltage gain converter is proposed, but inductor counts are more, and voltage stress on the switch is the same as output voltage. A schematic diagram that shows the application of DC-DC converter in DC Microgrid is shown in Figure 1.

This paper analyzes a converter topology with high gain using a single switch and comparatively low voltage stresses across the switch and other power components. The key features of the proposed converter are

(i) Voltage gain is more than twice as compared with a conventional quadratic boost converter and twice quadratic boost converter presented in [26]

(ii) Coupled inductor is not used to increase the gain hence the problems caused due to leakage inductance are not there.

(iii) Only one switch is used and hence control is easy.

(iv) Input current is continuous with low ripple that reduces the cost of input filter.

The converter can be operated with a wide range of duty ratios avoiding operation at extreme duty ratio, and hence there is no problem related to reverse recovery time for diodes in the proposed converter. This converter has comparatively more components, but its voltage gain is high and input current is continuous. The circuits of the conventional boost converter and twice the quadratic boost converter [26] are shown in Figure 2(a) and 2(b) respectively. It can be seen that these converters utilize two and three inductors respectively but still their voltage gain is less than the proposed topology. The schematic of the proposed converter topology is shown in Figure 2(c). The absence of common ground is one of the disadvantages of the converter. However, the proposed converter can be interfaced with solar PV by removing the voltage multiplier circuit used in the converter as shown in Figure 2(c) or by adding other existing multipliers with common ground. This paper is outlined as follows:
In section II, circuit description, working, and mode of operation for the proposed converter are detailed in CCM. Further, in section II itself, design parameters like the value of inductances and capacitances are also calculated. Section III has a comparison of this converter among similar converters. Section IV describes the power loss analysis of the converter. Section V shows the simulation and experimental results. The conclusion is discussed in section VI.

II. PROPOSED CONVERTER

A. CIRCUIT DETAILS

The conventional quadratic boost is shown in Figure 2(a) with two inductors. Proposed converter [26] in Figure 2(b) uses a voltage multiplier to boost the voltage to achieve voltage gain of twice the quadratic boost converter with three inductors. The proposed converter consists of two inductors but with an advantage greater than the aforementioned converters. The presented converter in Figure 2(c) includes single switch S1, two inductors L1 and L2, five capacitors named C1, C2, C3, C4 and C0 and six diodes specified as D1, D2, D3, D4, D5, and D6 and load R. All capacitances and inductances are taken as large for analysis so that voltage across capacitors and current through inductors are constant. The converter has two operating states within one switching Period Ts. All analysis is done in CCM mode; therefore, a continuous input current is assumed. The considerations taken to analyze the circuit operations in equilibrium are as follows:

- All components are ideal; therefore, no loss takes place.
- The switching period is constant.

B. MODES OF OPERATION

The circuit is analyzed in two modes: the first one has been analyzed during switch ON, and the second one is during switch off. Both modes of the circuit are shown in Figure 4. And some graphs related to converter such as diode voltage switch off. Both modes of the circuit are shown in Figure 4. In the graph, the interval t0-t1 is the ON period, and t1-t2 is the OFF period.

D. MODE I: WHEN SWITCH IS OFF(t1 < t < t2)

As shown in Figure 4(b), D1, D2, and D3 are forward biased while D4, D5, and D6 are reversed biased during switch OFF. In this interval, inductor currents I1 and I2 decrease simultaneously, and they transfer their energy to capacitor C1, C3, and C4. Capacitor C0 discharges and feeds the load.

\[
\begin{align*}
V_{L1} &= L_1 \frac{dI_{L1}}{dt} = V_{in} \\
V_{L2} &= L_2 \frac{dI_{L2}}{dt} = V_{C1} \\
C_1 \frac{dV_{C1}}{dt} &= I_{C1} = I_{C2} - I_{L2} \\
C_2 \frac{dV_{C2}}{dt} &= I_{C2} \\
C_3 \frac{dV_{C3}}{dt} &= C_4 \frac{dV_{C4}}{dt} = I_{C3} = I_{C4} \\
C_0 \frac{dV_{C0}}{dt} &= I_{C0} = I_{C3} - I_{o} \\
V_0 &= V_{C3} + V_{C4} \\
V_{C1} &= -V_{C2}
\end{align*}
\]

FIGURE 4. Modes of operations for the proposed converter (a) when the switch is ON (b) when the switch is OFF.
Derived voltages and currents are as follows:

\[
\begin{align*}
V_{L1} &= L_1 \frac{dL_1}{dt} = V_{in} - V_{C1} \\
V_{L2} &= L_2 \frac{dL_2}{dt} = V_{C1} - V_{C2} - V_{C3} \\
C_1 \frac{dV_{C1}}{dt} &= I_{C1} = I_{L1} - I_{L2} \\
C_2 \frac{dV_{C2}}{dt} &= I_{C2} = I_{L2} \\
C_3 \frac{dV_{C3}}{dt} + C_4 \frac{dV_{C4}}{dt} &= I_{C3} + I_{C4} = I_{L2} \\
C_0 \frac{dV_{C0}}{dt} &= I_{C0} = -I_o \\
V_{C4} &= V_{C5}
\end{align*}
\]

\section*{E. VOLTAGE GAIN(M) CALCULATION}
At the steady-state, the average voltage across an inductor is zero. Applying the volt-sec balance principle on L1 and L2 using results from (1) and (2) and get results as follows:

\[
DV_{in} + (1-D)(V_{in} - V_{C1}) = 0 \tag{3}
\]

\[
DV_{C1} + (1-D)(V_{C1} - V_{C2} - V_{C3}) = 0 \tag{4}
\]

Using (1), (2), (3), and (4), the following results come out:

\[
\begin{align*}
V_{C1} &= \frac{V_{in}}{1-D} \\
V_{C1} &= \frac{(1-D)V_o}{2(2-D)} \tag{5}
\end{align*}
\]

And finally, using (5) voltage gain for converter comes out as follows:

\[
M = \frac{V_o}{V_{in}} = \frac{2(2-D)}{(1-D)^2} \tag{6}
\]

\section*{F. VOLTAGE AND CURRENT STRESSES OF POWER DEVICES}
The switch and other components’ voltage stress means that the voltage appeared on the switch and the other components when that particular components are OFF. The voltage stresses across switch S1 and all diodes D1, D2, D3, D4, and D5 are mentioned below:

\[
\begin{align*}
V_{S1} &= \frac{(2-D)V_{in}}{(1-D)^2} = \frac{V_o}{2} \quad V_{D1} = \frac{V_o}{2(2-D)} \\
V_{D2} &= \frac{(1-D)V_o}{2(2-D)} \quad V_{D3} = \frac{(1-D)V_o}{2(2-D)} \\
V_{D4} &= V_{D5} = V_{D6} = \frac{V_o}{2}
\end{align*} \tag{7}
\]

Assuming a lossless circuit, ideally, input power is delivered to the load entirely. Hence,

\[
\begin{align*}
P_{in} &= P_{out} \\
V_{in}I_{in} &= V_oI_o \\
\frac{I_{in}}{I_o} &= \frac{V_o}{V_{in}} = M = \frac{2(2-D)}{(1-D)^2}
\end{align*} \tag{8}
\]

It is clear from Figure 3 that

\[
I_{L1} = I_{in}
\]

Hence, from (8)

\[
I_{L1} = \frac{2(2-D)}{(1-D)^2}I_o \tag{9}
\]

Applying ampere-sec balance on C1 and C2 to get average current through inductor L2:

\[
I_{C1,av}D + I_{C1,off} (1-D) = 0
\]

\[
\text{And }
I_{C2,av}D + I_{C2,off} (1-D) = 0
\]

Using current equations from (1) and (2), \(I_{L2}\) can be extracted as shown in Equation (10).

\[
I_{L2} = \frac{2I_o}{(1-D)} \tag{10}
\]

Similarly, applying ampere-sec balance on C1 and C4 to get current through inductor I5:

\[
I_5 = \frac{(3-D^2)I_o}{(1-D)^2} \tag{11}
\]

Similarly, the current through all diodes can be drawn out as follows:

\[
\begin{align*}
I_{D1} &= \frac{2I_o}{(1-D)^2} \\
I_{D2} &= \frac{2I_o}{(1-D)} \quad I_{D3} = \frac{2I_o}{(1-D)} \\
I_{D4} &= I_{D5} = I_{D6} = I_o
\end{align*} \tag{12}
\]

\section*{G. DESIGN PARAMETERS}

1) DUTY CYCLE CALCULATION

To obtain the desired output voltage at the given input voltage, duty cycle D can be calculated. From (6), the duty cycle is:

\[
D = \frac{V_o - V_{in} + \sqrt{V_{in}(V_{in} + 2V_o)}}{V_o} \tag{13}
\]

2) COMPONENT DESIGN

For a given suitable value of ripple of inductor currents \(\Delta I_{L1}\) and \(\Delta I_{L2}\) at a fixed value of switching frequency \(f_s\) for this converter, inductances can be extracted from (1) as:

\[
\begin{align*}
L_1 &= \frac{V_{in}D}{\Delta I_{L1}} = \frac{V_{in}D}{\Delta I_{L1}f_s} \\
L_2 &= \frac{V_{in}DT_s}{(1-D)\Delta I_{L2}} = \frac{V_{in}D}{(1-D)\Delta I_{L2}f_s}
\end{align*} \tag{14}
\]

Moreover, within the valid range of voltage ripple value of capacitances can be calculated from (2) as:

\[
\begin{align*}
C_1 &= \frac{2V_{in}D}{(1-D)R\Delta V_{C1f_s}} \\
C_2 &= \frac{2V_{in}D}{(1-D)R\Delta V_{C2f_s}} \tag{15}
\end{align*}
\]

\[
\begin{align*}
C_3 &= \frac{DV_o}{R\Delta V_{C3f_s}} \\
C_4 &= \frac{DV_o}{R\Delta V_{C4f_s}} \\
C_5 &= \frac{DV_o}{R\Delta V_{C5f_s}} \\
C_6 &= \frac{DV_o}{R\Delta V_{C6f_s}}
\end{align*}
\]
For a specific value of $D$, $f_s$, $V_o$, $V_{in}$, $R$ and suitable current and voltage ripples, convenient inductors and capacitors can be chosen.

**H. BOUNDARY CONDITION**

For continuous conduction mode of operation, the minimum current in each inductor should be greater than zero. And therefore, the minimum inductance required for both the inductors are calculated as follows:

$$I_{L1} = \frac{2(2 - D)}{(1 - D)^2} I_o$$
$$\Delta I_{L1} = \frac{V_{in} D}{L_{1f_s}}$$
$$I_{L1\text{min}} = I_{L1} - \frac{\Delta I_{L1}}{2}$$
$$L_1 \geq \frac{D(1 - D)^2 R}{8(2 - D)^2 f_s}$$

$$I_{L2} = \frac{2I_o}{(1 - D) V_{in} D_L f_s}$$
$$\Delta I_{L2} = \frac{V_{in} D}{L_{2f_s}}$$
$$I_{L2\text{min}} = I_{L2} - \frac{\Delta I_{L2}}{2}$$
$$L_2 \geq \frac{D(1 - D)^2 R}{8(2 - D)^2 f_s}$$

Defining normalized inductor time constant for inductor $L_2$

$$\tau = \frac{8L_{2f_s}}{R}$$

Using (17) the boundary normalized inductor time constant $\tau_B$ can be expressed as

$$\tau_B = \frac{D(1 - D)^2}{(2 - D)}$$

To operate in continuous conduction mode $\tau$ must be greater than $\tau_B$ otherwise, it operates in a discontinuous conduction mode of operation. In other words,

$$\begin{cases} 
\tau > \tau_B; \text{ Continuous conduction mode (CCM)} \\
\tau < \tau_B; \text{ Discontinuous conduction mode (DCM)} \\
\tau = \tau_B; \text{ Boundary mode}
\end{cases}$$

The converter may operate in different region depending upon the condition as shown in Figure 5. It should be noted that switching frequency is constant for both CCM and BCM.

**TABLE 1.** Comparison among other high gain DC-DC converters.

| TOPOLOGY | Number of Switch | Number of Inductors | Number of Diodes | Number of Capacitors | The voltage stress on the switch ($V_{n_o}$) | Voltage Gain ($V_M$) | Voltage gain at $D = 0.5$ |
|----------|-----------------|---------------------|-----------------|----------------------|---------------------------------------------|---------------------|--------------------------|
| Proposed | 1               | 2                   | 6               | 5                    | $\frac{(2 - D)}{(1 - D)^2}$                 | 12                  | 12                      |
| [17]     | 1               | 1 coupled inductor  | 5               | 3                    | $\frac{3}{1 - D}$                           | 10                  | 10                      |
| [23]     | 1               | 2                   | 4               | 5                    | $\frac{1}{(1 - D)^2}$                       | 6                   | 6                       |
| [24]     | 1               | 2                   | 5               | 4                    | $\frac{4}{1 - D}$                           | 7                   | 7                       |
| [26]     | 1               | 3                   | 5               | 3                    | $\frac{2}{(1 - D)^2}$                       | 8                   | 8                       |
| [27]     | 1               | 2                   | 5               | 4                    | $\frac{1}{(1 - D)^2}$                       | 6                   | 6                       |
| [28]     | 6               | 6                   | 14              | 8                    | $\frac{1}{1 - D}$                           | 7                   | 7                       |
| [29]     | 2               | 4                   | 9               | 1                    | $S_1 = \frac{1}{1 - D}$, $S_2 = \frac{2D}{1 - D}$ | 5                   | 5                       |
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FIGURE 6. Comparison (a) Voltage gain vs duty ratio (b) Voltage stress vs Voltage Gain (c) Output diode voltage stress ($V_D/V_0$) vs duty ratio.

Fardoun [27] utilize the same number of inductor and switch as proposed one but voltage gains of the converters are low and voltage stress on the switches are higher than the proposed converter. The converter analyzed in Javed et al. [26] provides a voltage gain of 2 times of CQBC that is lower than the proposed converter and in this converter stress across the switch is the same as that of CQBC. Although this converter brings into service three inductors which makes it heavier. The converters in Maalandish et al. [28] and Gupta et al. [29] provides very low gain compared to the proposed converter utilizing six inductors, six switches and four inductors, two switches respectively. The voltage stress on the switches across the power devices, the proposed converter can utilize the low rating devices which is helpful to gain high efficiency.

IV. POWER LOSS ANALYSIS OF THE CONVERTER

An equivalent circuit with parasitic resistances of the converter is shown in Figure 7. Where $r_{S1}$ is the MOSFET on-resistance, $r_{D1}$, $r_{D2}$, $r_{D3}$, $r_{D4}$, $r_{D5}$ and $r_{D6}$ are the diode on-resistance, $V_F$ is the diode threshold voltage, $r_{L1}$ and $r_{L2}$ are the ESRs of inductors $L_1$, and $L_2$ and $r_{C1}$, $r_{C2}$, $r_{C3}$, $r_{C4}$, and $r_{C0}$ are the ESRs of capacitors respectively. Conduction losses have calculated assuming that inductors currents are ripple-free, and switching losses are not included.

Since, $P_0 = V_0I_0 = I_{S1}^2R$

1) MOSFET CONDUCTION LOSS

$$I_{S1, rms} = \frac{V_0}{\sqrt{2Dr(1-D)t}} I_0$$

$$P_{rS1} = I_{S1, rms}^2 r_{S1} = \left(\frac{3-D^2}{Dr(1-D)t}\right) I_0^2 r_{S1} = \left(\frac{3-D^2}{Dr(1-D)t}\right) \frac{r_{S1}}{R} P_0$$ (20)

2) POWER LOSSES IN DIODES DUE TO ON-RESISTANCE AND FORWARD-VOLTAGE DROPS

$I_{D1, rms}$ and $I_D$ are the rms currents and average currents passing through diodes respectively. $P_{rD}$ is the power loss in

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Since it has assumed that inductor currents are ripple-free, forward-voltage drops can be drawn out using (21), (22), (23), hence, total diode losses due to on-resistance and determined as follows.

\[
\begin{align*}
I_{D1,\text{rms}} &= \frac{2I_0}{\sqrt{D(1-D)^2}} I_D = \frac{2I_0}{(1-D)^2} P_D \\
Pr_{D1} &= I_{D1,\text{rms}}^2 r_{D1} = \frac{4I_0^2}{(1-D)^3} r_{D1} = \frac{4}{(1-D)^4} r_{D1} P_0 \\
PV_{F1} &= V_{F1} I_{D1} = \frac{2I_0}{(1-D)^2} V_{F1} = \frac{2}{(1-D)^2} V_{F0} P_0
\end{align*}
\]

(21)

\[
\begin{align*}
I_{D2,\text{rms}} &= \frac{2I_0}{\sqrt{D(1-D)^3}} I_D = \frac{2I_0}{(1-D)^2} P_D \\
Pr_{D2} &= I_{D2,\text{rms}}^2 r_{D2} = \frac{4I_0^2}{(1-D)^4} r_{D2} = \frac{4}{(1-D)^5} r_{D2} P_0 \\
PV_{F2} &= V_{F2} I_{D2} = \frac{2I_0}{(1-D)^2} V_{F2} = \frac{2}{(1-D)^2} V_{F0} P_0
\end{align*}
\]

(22)

\[
\begin{align*}
I_{D3,\text{rms}} &= \frac{2I_0}{\sqrt{D(1-D)^4}} I_D = \frac{2I_0}{(1-D)^2} P_D \\
Pr_{D3} &= I_{D3,\text{rms}}^2 r_{D3} = \frac{4I_0^2}{(1-D)^5} r_{D3} = \frac{4}{(1-D)^6} r_{D3} P_0 \\
PV_{F3} &= V_{F3} I_{D3} = \frac{2I_0}{(1-D)^2} V_{F3} = \frac{2}{(1-D)^2} V_{F0} P_0
\end{align*}
\]

(23)

\[
\begin{align*}
I_{D4,\text{rms}} &= I_{D6,\text{rms}} = \frac{I_0}{\sqrt{D}} \\
I_{D4} &= I_{D6} = I_0 \\
Pr_{D4} &= I_{D4,\text{rms}}^2 r_{D4} = \frac{I_0^2}{(1-D)^2} r_{D4} = \frac{1}{(1-D)^2} r_{D4} P_0 \\
Pr_{D6} &= I_{D6,\text{rms}}^2 r_{D6} = \frac{I_0^2}{(1-D)^2} r_{D6} = \frac{1}{(1-D)^3} r_{D6} P_0 \\
PV_{F4} &= V_{F4} I_{D4} = V_{F4} I_0 = V_{F0} P_0 \\
PV_{F6} &= V_{F6} I_{D6} = V_{F6} I_0 = V_{F0} P_0
\end{align*}
\]

(24)

\[
\begin{align*}
I_{D5,\text{rms}} &= \frac{I_0}{\sqrt{D}} I_{D5} = I_0 \\
Pr_{D5} &= I_{D5,\text{rms}}^2 r_{D5} = \frac{I_0^2}{(1-D)^2} r_{D5} = \frac{1}{(1-D)^4} r_{D5} P_0 \\
PV_{F5} &= V_{F5} I_{D5} = V_{F5} I_0 = V_{F0} P_0
\end{align*}
\]

(25)

Following assumptions can be taken:

\[
\begin{align*}
r_{D1} &= r_{D2} = r_{D3} = r_{D4} = r_{D5} = r_{D6} = r_D \\
V_{F1} &= V_{F2} = V_{F3} = V_{F4} = V_{F5} = V_{F6} = V_F
\end{align*}
\]

(26)

Hence, total diode losses due to on-resistance and forward-voltage drops can be drawn out using (21), (22), (23), (24), (25), and (26) as follows:

\[
\begin{align*}
Pr_D &= \left(\frac{3-D^2}{D} \right) \frac{(D^2-2D+3)}{(1-D)^4} r_D P_0 \\
PV_F &= \left(\frac{3D^2-10D+9}{(1-D)^2} \right) r_F V_F P_0
\end{align*}
\]

(27)

3) LOSSES IN INDUCTORS DUE TO ESRs
Since it has assumed that inductor currents are ripple-free. Hence, their rms values and average values are equal in magnitude. In equation (28), \(I_L\) is the average current through the inductor and \(Pr_L\) is the power dissipation by inductor due to its equivalent series resistance (ESR) as follows:

\[
\begin{align*}
I_{L1,\text{rms}} &= I_{L1} = \frac{2(2-D)I_0}{(1-D)^2} \\
I_{L2,\text{rms}} &= I_{L2} = \frac{2I_0}{(1-D)^2} \\
Pr_{L1} &= I_{L1,\text{rms}}^2 r_{L1} = \frac{4(2-D)^2}{(1-D)^4} r_{L1} = \frac{4(2-D)^2}{(1-D)^5} r_{L1} P_0 \\
Pr_{L2} &= I_{L2,\text{rms}}^2 r_{L2} = \frac{4}{(1-D)^5} I_{L2}^2 r_{L2} = \frac{4}{(1-D)^6} r_{L2} P_0
\end{align*}
\]

(28)

It can be assumed that,

\[
r_{L1} = r_{L2} = r_L
\]

Hence, total inductor loss from (28),

\[
Pr_L = \left(\frac{4(2D^2-6D+5)}{(1-D)^4} \right) r_L P_0
\]

(29)

4) LOSSES IN CAPACITORS DUE TO ESRs
\(I_{C,\text{rms}}\) is the rms current flowing through capacitor and \(Pr_C\) is the power loss due to equivalent series resistance (ESR) of the capacitor.

\[
\begin{align*}
I_{C1,\text{rms}} &= \frac{2}{\sqrt{D(1-D)}} I_0 \\
Pr_{C1} &= I_{C1,\text{rms}}^2 r_{C1} = \frac{4}{D(1-D)^3} I_0^2 r_{C1} = \frac{4}{(1-D)^4} r_{C1} P_0 \\
I_{C2,\text{rms}} &= \frac{2}{\sqrt{D(1-D)}} I_0 \\
Pr_{C2} &= I_{C2,\text{rms}}^2 r_{C2} = \frac{2}{D(1-D)^3} I_0^2 r_{C2} = \frac{2}{(1-D)^4} r_{C2} P_0 \\
I_{C3,\text{rms}} &= \frac{1}{\sqrt{D(1-D)}} I_0 \\
Pr_{C3} &= I_{C3,\text{rms}}^2 r_{C3} = \frac{1}{D(1-D)^3} I_0^2 r_{C3} = \frac{1}{(1-D)^4} r_{C3} P_0 \\
I_{C4,\text{rms}} &= \frac{1}{\sqrt{D(1-D)}} I_0 \\
Pr_{C4} &= I_{C4,\text{rms}}^2 r_{C4} = \frac{1}{D(1-D)^3} I_0^2 r_{C4} = \frac{1}{(1-D)^4} r_{C4} P_0 \\
I_{C0,\text{rms}} &= \left(\frac{1}{\sqrt{D}} \right) I_0 \\
Pr_{C0} &= I_{C0,\text{rms}}^2 r_{C0} = \frac{(1-D)}{D} I_0^2 r_{C0} = \frac{(1-D)}{D} r_{C0} P_0
\end{align*}
\]

(30)

(31)

(32)

(33)

And it is assuming that,

\[
r_{C1} = r_{C2} = r_{C3} = r_{C4} = r_{C0} = r_C
\]

From (30), (31), (32) and (33), total capacitor losses due to ESRs can be shown as follows:

\[
Pr_C = \frac{(D^2-2D+3)^2}{D(1-D)^3} r_C P_0
\]

(34)

From (20), (27), (29) and (34), total losses in the converter can be calculated as follows:

\[
Pr_{\text{loss, total}} = Pr_S + Pr_D + PV_F + Pr_L + Pr_C
\]

Hence,

\[
Pr_{\text{loss, total}} = \left[4e_r \frac{r_L}{R} + b \left(\frac{r_D}{R} + \frac{r_S}{R} \right) + d \frac{V_F}{V_0} + e \frac{r_C}{R} \right] P_0
\]

(35)
where,
\[
\begin{align*}
a &= \frac{(2D^2 - 6D + 5)}{(1 - D)^4}, \\
b &= \frac{(3 - D^2)^2}{D(1 - D)^4}, \\
c &= \frac{(D^2 - 2D + 3)}{(3 - D^2)}, \\
d &= \frac{\left(3D^2 - 10D + 9\right)}{(1 - D)^2}, \\
e &= \frac{(D^2 - 2D + 3)^2}{D(1 - D)^3}
\end{align*}
\]
And efficiency,
\[
\eta = \frac{1}{1 + \frac{P_{\text{loss, total}}}{P_0}}
\]
Hence, the efficiency of the converter can be determined using (35) as follows:
\[
\eta = \frac{1}{1 + 4a\frac{V_o}{R} + b\left(c\frac{V_o}{R} + \frac{\alpha}{R}\right) + d\frac{V_o}{V_0} + e\frac{V_o}{R}}
\]

V. SIMULATION AND EXPERIMENTAL RESULTS

A. SIMULATION RESULTS

The parameters used to extract the simulation results using PLECS software are shown in Table 2. From (1) and (2), it has been drawn out theoretically that \(V_{C3} = V_o/2\). For input voltage of 24V with 0.3 duty cycle, output voltage \(V_o\) is found to be 166V and \(V_{C3}\) to 83V. Figure 8 shows the value of inductor currents \(I_{L1}\) and \(I_{L2}\) along with a gate pulse at a duty cycle of 0.3. It can be seen that inductor currents are continuous and the average values are found to be 5.8A and 2.6A respectively. The ideal output voltage \(V_o\) is found to be 166V for a duty ratio of 30% at \(V_{\text{in}} = 24\) V as shown in Figure 9. It can be inferred that approximately a voltage gain of more than 6.8 times can be achieved at a small duty ratio of 0.3. Practically the voltage gain will be reduced owing to the voltage drop across switch, diodes, capacitors and inductors.

It can be observed in Figure 10 that the converter draws a continuous current with low ripple that increases its adaptability into PV systems and fuel cells and that is why this converter reduces the cost of input filter. Figure 11 presents the very low variation in voltage across \(C_1, C_3\), and \(C_4\) having values of 34V, 83V, and 83V respectively. Figure 12 shows the stress on switch \(S_1\) with the value of 83V at \(V_o\) of 166V which is far less than \(V_o\). Because of low voltage stress across switch \(S_1\), the proposed converter utilizes a low power rating switch which reduces the loss contribution and increases the efficiency.

Figure 12 presents the voltage across output diode \(D_5\), \(V_{D5}\) also having the value of 83V. Voltage appeared across the output diode is half than output voltage \(V_0\) that is advantageous for the converter that it can be operated with low rating power semiconductor devices. Simulation results have drawn out at duty ratio of 30% with source voltage \(V_{\text{in}} = 24\) V having fed to a resistive load of 200 \(\Omega\).

B. EXPERIMENTAL RESULTS

A 200W prototype has been developed to evaluate and verify the operation of the converter practically. Design parameters and components are listed in Table 2. The hardware prototype
is depicted in Figure 13. The proposed converter can be operated with a wide range of duty ratio but since the converter has a quadratic gain, a high voltage gain of more than 15 times can be achieved for D less than 0.5. All experimental results have been provided at a duty ratio of 30%. This duty cycle is just for illustration to validate the theoretical results of the proposed converter, correctly and any other duty cycle can be employed. In Figure 14, inductor currents $I_{L1}$ and $I_{L2}$ are shown having small ripples with an average value of 5.2A and 2.2A, respectively.

As shown in Figure 15 the for the input voltage of 24 V the output voltage $V_o$ is found to be 160 V at a duty cycle of $D = 0.3$. The practical output voltage is reduced due to voltage drop across $R_{DSOn}$ of MOSFET, parasitic resistances of inductors capacitors and switch. As depicted in Figure 16 the value of capacitor voltages $V_{C1}$, $V_{C3}$, and are found to be 30V, 80V and 80V respectively. It can be observed that the voltage stress across capacitors is less than $V_0$. Figure 17 shows the waveform of stress $V_{S1}$ on switch $S_1$ with a value of 80V. All values of experimental waveforms closely agree with simulation results. The proposed converter has operated at $D = 0.3$ only for the verification of the simulation and theoretical results. It can be operated at a higher duty ratio to get a high voltage level which is required by the inverter.

To quantify the losses in the converter and the efficiency of the converter, a complete analysis is performed. The simulated efficiency of the proposed converter versus output power $P_o$ is plotted in Figure 18 at different value of source voltage $V_{in}$. It can be observed in Figure 18 that an increment
in input voltage improves the efficiency of the converter. The converter can be used in renewable energy applications up to 300 W with high efficiency. The proposed converter’s peak efficiency is found to be greater than 95% when the input is 40 V and \( P_o = 75 \) W. Figure 19 illustrates the losses per group of the same components used in the proposed converter for \( V_{in} = 24 \) V and \( D = 0.3 \). It can be noticed in Figure 19 that a 36% loss of total loss is due to diodes, and the contribution of switch \( S \) in loss is 14%. The losses in the converter can be further reduced by choosing fast recovery diodes with low internal resistance and cut-in voltage. Further, inductor resistance should also be kept low to increase the efficiency of the converter. It should be noted that steady-state equations of losses derived in this paper are used for calculation.

VI. CONCLUSION

A new non-inverting DC-DC boost converter is proposed in this paper. The proposed converter has high gain and utilizes only one switch to operate the converter, and therefore, control is easy. The voltage stress on the switch and diodes is low, and therefore low voltage-rated switch can be chosen which increases the efficiency and reduces the cost. The converter has draws continuous input current and thus the need for an input filter does not arise. Hence, it can be used in microgrid applications as the voltage of the converter at a low duty ratio is high compared to the conventional boost converter and other high gain converters. To verify the analysis practically, a 200W hardware prototype has been prepared for the converter. The peak of the efficiency of the proposed converter is observed to be greater than 95% but the efficiency decreases at high output power on account of losses. Thus, the proposed converter is suitable for medium power range suitably up to 300W. The merits of the converter make it suitable to be used in solar PV applications, automobiles, fuel cells and electric vehicles.

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