Single stage high-frequency non-isolated step-up sinusoidal inverter with three ground-side power switches

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Abstract: Conventional high-frequency non-isolated inverter is generally composed of two stages, the step-up stage and the voltage inversion stage, and independent control strategy must exert on each stage. In order to solve the shortcoming, a topological solution (L3 topology) is proposed in this letter, combining the structure of the boost topology and the improved Watkins-Johnson topology to a single stage, realizing voltage step-up and inversion with only three ground-side power switches and single control signal. Theoretical analysis and experimental results validate the feasibility. The merits include ease of driving, small port current ripple, high efficiency, simple control strategy and so forth.

Keywords: ground-side switch, non-isolated inverter, single-stage, voltage step-up

Classification: Power devices and circuits

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## 1 Introduction

Compared with the high-frequency isolated inverter, the non-isolated inverter possesses advantages of high efficiency, small size, low cost and so on [1]. All existing conventional non-isolated step-up sinusoidal inverters are composed of at least two stages, the voltage step-up stage and the voltage inversion stage [2, 3, 4, 5, 6]. The former steps up the low input dc voltage to a high level, the latter transforms the high-line voltage to a desired sinusoidal output. The structure and keypoint waveforms are illustrated in Fig. 1.

The voltage step-up stage generally adopts topologies including the boost [7] and the Z-source circuit [8, 9]. The voltage inversion stage adopts the half-bridge [10], the full-bridge [11] and its derivative circuits such as H5, H6 [12, 13, 14], multi-level H-bridge [15] and HERIC [16].
The voltage step-up and down procedure brings about extra loss of efficiency, and the separate control strategy on each stage increases the control complexity. In order to solve these inherent shortcomings, a topological approach is proposed, by cascading and optimizing the structure of the conventional boost and the improved Watkins-Johnson (WJ) topology [17, 18]. The merits include: only one control signal is able to realize voltage step-up as well as sinusoidal inversion; three ground-connected power switches render the inverter ease of driving.

2 Proposed L3 topology

Fig. 2 illustrates the proposed L3 topology, which is named because of three low-side (ground-side) power switches denoted as $Q_1$, $Q_2$ and $Q_3$, respectively. The input voltage and the voltage across the resistive load $R$ are denoted as $V_g$ and $v$. Noting that all lowercase letters represent time-varying variables and the uppercase stands for constant. Inductors are marked as $L_1$ and $L_2$ wherein the latter is a coupled inductor with winding turns $N_1$ to $N_2$, which are equally distributed generally. Intermediate capacitor and output filtering capacitor are denoted as $C_1$ and $C_2$, respectively. The freewheeling diode is written as $D_1$. Electrical quantities $v_{L1}$, $i_{L1}$, $v_{L2}$, $i_{L2}$, $v_{C1}$, $i_{C1}$, $v_{C2}$ and $i_{C2}$ are also annotated in the figure. Only one PWM signal $d(t)$ is needed to drive the power switches, and its complementary signal is denoted as $d'(t)$.

Essentially, the L3 topology is the cascade of conventional boost topology and improved WJ topology with floating power switch low-side-ized. The two topologies are deeply merged together, forming a inseparable single-stage inverter. In general, the number of stages of converter is judged by the number of independent control signal (together with its complementary signal can be considered as a whole). Therefore, the L3 topology should be categorized into the single stage.

The intermediate capacitor $C_1$ behaves as a “pulse-link” capacitor rather than a dc-link capacitor, which relays the pulsating voltage to accomplish step-up-and-up procedure. The voltage across $C_1$ drastically changes along with the switching frequency. Therefore, a high-frequency capacitor with small capacitance is needed.

Furthermore, unlike the conventional WJ topology, the L3 topology provides a floating output. The output waveform tends to purer compared with that of ground-
connected, for the reason that the floating output isolates the voltage output from interfere due to ground loops.

2.1 Steady-state analysis

During subinterval 1 ($0 < t < DT_s$), $Q_1$ and $Q_3$ are switched on and $Q_2$ is cut off. The equivalent circuit is derived in Fig. 3.

Electrical quantities related to the inductor and capacitor are expressed in (1) in matrix form. Upon using small-ripple approximation, the time-variant quantities is substituted by their dc terms.

$$\begin{bmatrix} v_{L1} & i_{C1} \\ v_{L2} & i_{C2} \end{bmatrix} = \begin{bmatrix} V_g & i_{L2} \\ v - v_{C1} & -i_{L2} - \frac{v}{R} \end{bmatrix} \approx \begin{bmatrix} V_g & I_{L2} \\ V - V_{C1} & -I_{L2} - \frac{V}{R} \end{bmatrix}$$ (1)

During subinterval 2 ($DT_s < t < T_s$), the switch states are complementary to the former. Consequently, the equivalent circuit is illustrated in Fig. 4.

Again the voltage and current relationships are derived in (2).
Upon invoking principles of inductor volt-second balance and capacitor charge balance and eliminating intermediate variables, one obtains the voltage conversion ratio $M(D)$ shown in (3). Where, $D' = 1 - D.$

$$M(D) = \frac{V}{V_g} = \frac{2D - 1}{D'} = M_{\text{boost}}(D) \cdot M_{\text{WJ}}(D)$$ (3)

Actually, the conversion ratio is the synthesize of the boost ($M_{\text{boost}}(D) = \frac{1}{D'}$) and the WJ topology ($M_{\text{WJ}}(D) = \frac{2D-1}{D}$). The inductor currents related to the load current $I_{\text{load}}$ are also obtained in (4) and (5), respectively.

$$I_{L1} = \frac{2D - 1}{D'} I_{\text{load}}$$ (4)

$$I_{L2} = -\frac{1}{D} I_{\text{load}}$$ (5)

The curves sketched in Fig. 5 illustrate $M(D)$, $I_{L1}$ and $I_{L2}$ with $I_{\text{load}}$ normalized. It can be concluded from the figure that the range of $M(D)$ covers the entire vertical axis, which means the L3 topology can step up, step down, as well as invert the polarity of the input voltage with $D$ sliding between 0 and 1. Furthermore, the inductors should withstand the current larger than the load current.

![Fig. 5. Curves of $M(D)$, $I_{L1}$ and $I_{L2}$ with respect to $D$.](image)

### 2.2 Control strategy

In order to output a pure sinusoidal waveform with angular frequency of $\omega$ and phase of $\phi$, the control signal $d(t)$ should vary with time in the manner shown in (6). Where, the scale factor between the output amplitude $V_m$ and the input voltage $V_g$ is defined as $\alpha_v$, and the entire right term is written as $R_t$ for convenience.

$$M(d(t)) = \frac{2d(t) - 1}{d'(t)d(t)} = \frac{V_m}{V_g} \sin(\omega t + \phi) \triangleq \alpha_v \sin(\omega t + \phi) \triangleq R_t$$ (6)

By unfolding (6), the roots $d_1(t)$ and $d_2(t)$ of the quadratic equation is derived in (7) and (8), respectively.
The range of $R_t$ covers from $-\infty$ to $+\infty$, for the reason that the inverter should output sinusoidal waveform of any amplitude theoretically. Fig. 6 illustrates the distribution of the two roots.

From the figure, $d_2(t)$ should be eliminated, because its value is higher than 1 and lower than 0. The root $d_1(t)$ is selected as the control signal, for its range locates between 0 and 1. Noting that the undefined point $(0, 0.5)$ making the denominator equals to zero belongs to a removable discontinuity point, which has negligible influence on the final waveform. The $R_t$ will not exactly locate on zero in practical.

Consequently, control signals with different $\alpha_v$ is sketched in Fig. 7.

### 2.3 Non-ideal case

Non-ideal parameters restrict and change the performance of the L3 topology. For instance, the series resistor $R_{L1}$ of $L_1$ is taken into account. Then the conversion ratio expressed in (3) is modified into (9).
\[ M_{\text{nonideal}}(D) = \frac{V}{V_g} = \frac{2D - 1}{D - \beta(2D - 1)^2} \]

(9)

Where, the non-ideal factor \( \beta \) is defined as \( R_{L1}/R \). Then the range of operative voltage conversion ratio narrows down as is shown in Fig. 8 with \( \beta \) equals to 0 (ideal), 0.05 and 0.1, respectively. The vertical asymptotes on both sides squeeze together along with \( \beta \) increases.

Next, the unequal distributed winding turns of the coupled inductor is considered. Define a proportionality factor \( K = N_1/(N_1 + N_2) \) for convenience, then the voltage conversion ratio is modified into (10), which is defined as \( M_K(D) \) and sketched in Fig. 9.

\[ M_K(D) = \frac{D - K}{D(1 - K)} \]

(10)

Fig. 8. Non-ideal case.

Fig. 9. Conversion ratio with different \( K \) value.

It can be seen that the point intersects with the horizontal axis (marked as \( \times \circ \Delta \)) moves left to \((0.3, 0)\) when \( K = 0.3 \), and moves right to \((0.7, 0)\) when \( K = 0.7 \). The curve turns to asymmetric when \( K \) deviates 0.5, which will cause problems include: the control strategy becomes more complicated; increasing the
wrapping difficulty; unpredictable non-ideal parameters; the magnetic biasing decreases core utilization. Therefore, \( K = 0.5 \) is the optimum value for L3 topology-based inverter.

3 Experimental results
An experimental prototype of L3 topology-based inverter is designed and photographed in Fig. 10.

![Prototype circuit](image)

**Fig. 10.** Prototype circuit.

3.1 Drive signal
The drive signal and its complementary signal are shown in Fig. 11. The duty cycle is altering accord with the control law expressed in (7).

![Drive signal](image)

**Fig. 11.** Drive signal.

3.2 Output waveforms
The output waveforms are acquired and shown in Fig. 12.

Fig. 12(a) is configured as \( V_s = 12 \text{ V}, \alpha_v = 2 \), and with 100 W power of load. On the other hand, Fig. 12(b) shows the case of \( \alpha_v = 5 \) with other parameters the same as before. The non-ideal parameters lead to waveform distortion and voltage gain inconformity. Therefore, a feedback control is needed in future.
3.3 Total harmonic distortion

In order to evaluate the output waveforms quantitatively, the total harmonic distortion (THD) distributions are calculated and shown in Fig. 13(a) and Fig. 13(b), corresponding the output waveforms of Fig. 12(a) and Fig. 12(b), respectively.

![THD distributions](image)

Fig. 12. Output waveforms.

Fig. 13. THD distributions.

It can be concluded from the figure that the L3 topology is especially suitable for not-too-high voltage step-up ratio, light load and off-grid applications. The L3 topology-based inverter has been applied to stand-by power supply for explosion-proof roadway light in a coal mine for test, with 36VDC input, 127VAC output, and nominal power of 36 W.
4 Conclusion

A single stage topology named L3 topology for high-frequency non-isolated step-up sinusoidal inverter use is proposed in this letter, in order to solve the shortcomings exist in the conventional two-stage inverter, realizing the functionalities of voltage step-up and voltage inversion with only one control signal and three ground-connected power switches. The merits include ease of driving, small port current ripple, high efficiency, simple control strategy and so forth. The application scope of the L3 topology-based inverter includes low to medium voltage step-up ratio, low power and off-grid such as vehicle inverter and household appliances.