Effect of Oxide Thickness Variation in Sub-micron NMOS Transistor

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Abstract. Aggressive scaling of metal oxide semiconductor (MOS) devices have resulted in the use of ultrathin gate oxides, which in turn enhanced the device performance. This work examines different components of tunnelling electron in scaled n-type MOS (NMOS) with ultrathin gate oxides (1.2-2.0 nm). Direct tunnelling currents are focused on the currents between the gate and the channel region in the substrates. The gate direct tunnelling currents are investigated by theoretical modelling and simulation experiments and their effects on the leakage current from those two approaches are compared. The simulation of this project was carried out using Sentaurus TCAD software. A 90 nm NMOS transistor is simulated to investigate the electron tunnelling phenomenon and its effect on the device performance. The 90 nm NMOS device was designed and characterized using Sentaurus TCAD software. In this project, there are two major simulations done using Sentaurus Process and Sentaurus Device. There are four parameters being investigated, which are is oxide thickness (\(T_{ox}\)), threshold voltage (\(V_{TH}\)), drain voltage (\(V_D\)) and gate voltage (\(V_G\)), to obtained result of drain current (\(I_D\)) and leakage current (\(I_{OFF}\)). The simulations data results are listed in the Inspect tools and used to plot graphs to compare between simulation and calculation results. The electrons start tunnelling at the \(T_{ox}\) of 1.4 nm with resulting in large \(I_{OFF}\) of 2.45x10⁻⁹ A at \(V_D\) of 0.5V. The simulation results are found to be almost identical with the theoretical modelling.

1. Introduction
Gate oxide thickness (\(T_{OX}\)) is the insulator layer between gate and substrate in metal oxide semiconductor field effect transistor (MOSFET). This gate oxide thickness can be used to modify the threshold voltage of a transistor [1, 2]. Lower oxide thickness and hence lower threshold voltage in critical paths can maintain the performance. Higher oxide thickness not only reduces gate oxide but also the leakage current decrease exponentially with an increase in the oxide thickness [3, 4]. The increases current not only adversely affect the MOS device performance but also greatly increase the standby power consumption of a highly integrated chip [5, 6].

\(SiO_2\) is a very good insulator, but at very small thickness levels electrons can move across the very thin insulation. The probability drops off exponentially with oxide thickness [7, 8]. The probability of electrons moves through the insulating gate oxide barrier increases with the increasing electric field across it. As complementary metal oxide semiconductor (CMOS) devices shrink in size, their gate oxide...
thickness reduces which reduces the gate voltage. Reducing the gate oxide below 3 nm appears to be difficult because current leaks through the thin oxide layer \[4, 9\].

There are some factors that caused the gate leakage flow through the dielectric to the substrate. The power dissipation due to leakage through a thin SiO\(_2\) gate oxide increase energy consumption \[10, 11\]. First is the oxide thickness layer. The thinner oxide, the larger gate induced drain leakage current. Various leakage current at a given oxide thickness are independent of the channel length. The thinner oxide layer the more dominant on the drain leakage current at lower drain voltage biases \[12, 13\]. The drain leakage current such as band to band and gate induced drain leakage currents have always been a concern for MOSFET scaling. When combining with ultrathin oxides, these effects are significant compared to the gate direct leakage current. Second is the permittivity of oxide layer material. High permittivity (high-k) materials are introduces in scaled transistor to further decrease the electrical thickness while maintaining a reliable physical thickness and low gate leakage \[14-16\]. Third is drain punch through. When the drain voltage is high enough, the depletion region around the drain may extend to source. Thus, causing current to flow irrespective of the gate voltage. When the source-drain electric field is too large, the electron speed will be high enough to break the electron-hole pair. Moreover, the electrons will penetrate the gate oxide, causing a gate current \[17, 18\].

The threshold voltage (\(V_{TH}\)) for transistor MOSFET is the voltage that was generated between the gate and source at MOS device where current drain source drop until zero \[12\]. \(V_{TH}\) is the minimum voltage to turn on the MOS transistor. It is also defined as the applied gate voltage achieving the required threshold inversion point. In this paper, the relationship between parameters that affect the \(V_{TH}\) is being investigated. These changing trend of threshold voltage will be visualised to see whether the targeted parameters are improving or withholding the device performance.

2. Modelling of Oxide Thickness Variation

The modelling was specific to the drain current on the NMOS transistor. The value of oxide thickness, \(V_{TH}\) and gate voltage was varied to study the effect of these parameters on drain current. The determination of drain current is depending on the three conditions in I-V characteristic. They are transition point, non-bias saturation point, and saturation point and described by (1), (2) and (3) respectively.

\[
V_{D \ (sat)} = V_G - V_{TH} \tag{1}
\]

\[
I_D = \frac{K_n}{2} (V_G - V_{TH})^2 \tag{2}
\]

\[
I_D = K_n \left[ 2(V_G - V_{TH})V_D - V_D^2 \right] \tag{3}
\]

where \(\varepsilon_{ox} = \varepsilon_r \varepsilon_0\). \(V_0\) is the threshold voltage, \(V_G\) is the gate voltage and \(K_n = \frac{W \mu_n C_{ox}}{L}\). Next, the oxide capacitance and threshold voltage are calculated using (4), (5) and (6).

\[
C_{ox} = \frac{\varepsilon_{ox} \varepsilon_0}{T_{ox}} = \frac{\varepsilon (\varepsilon_r)}{T_{ox}} \tag{4}
\]

\[
\phi_{FN} = V_T \ln \left( \frac{N_D}{n_i} \right) = \left( \frac{KT}{q} \right) \ln \left( \frac{N_D}{n_i} \right) \tag{5}
\]
\[ V_{TH} = V_{FB} + 2|\phi_{Fn}| + \frac{2\varepsilon_r q N_A (2\phi_{Fn})}{C_{ox}} \]  

where \( V_{TH} \) is the threshold voltage, \( L \) is the length of gate, \( C_{ox} \) is the oxide capacitance, \( W \) is the width, \( \varepsilon_r \) is the dielectric constant of SiO\(_2\), \( \varepsilon_0 \) is the vacuum permittivity, \( T_{OX} \) is oxide thickness, \( N_A \) and \( N_D \) is the doping concentration, \( n_i \) is the intrinsic carrier concentration, \( k \) is Boltzmann’s constant, \( T \) is room temperature and \( q \) is the electron charge. The following parameters are fixed as follows: \( N_A=4.7\times10^{17} \text{ cm}^{-3}, N_D=1\times10^{18} \text{ cm}^{-3}, L=90 \text{ nm and } W=0.2 \mu\text{m}. \)

2.1. Determination of \( V_{TH} \) with varying \( T_{OX} \)

Firstly, the \( V_{TH} \) was determined for different value of \( T_{OX} \). In this case, \( V_{TH} \) is calculated against \( T_{OX} \) with varying value of \( T_{OX} \) from 1.2 nm to 2.8 nm.

2.2. Determination of \( I_D \) with varying \( V_D \) for different \( V_G \) at \( T_{OX}=1.2 \text{ nm} \)

Next, \( I_D \) was determined by varying the value of \( V_D \) with different value of \( V_G \). \( I_D \) is calculated against \( V_D \) for \( V_G=1.0 \text{V}, 1.5 \text{V}, 2.0 \text{V}, 2.5 \text{V} \text{ and } 3.0 \text{V} \) at \( T_{OX}=1.2 \text{ nm} \).

2.3. Determination of \( I_D \) with varying \( V_D \) for different \( V_{TH} \)

Lastly, the calculation was done by varying the value of \( V_D \) with different value of \( V_{TH} \). \( I_D \) is calculated against \( V_D \) for \( V_{TH}=0.38 \text{V}, 0.44 \text{V}, 0.50 \text{V} \text{ and } 0.57 \text{V} \) at \( T_{OX}=1.4 \text{ nm}, 1.8 \text{ nm}, 2.0 \text{ nm}, 2.2 \text{ nm} \text{ and } 2.8 \text{ nm} \).

2.4. Simulation in Sentaurus TCAD

The oxide thickness variation at 90 nm NMOS transistor was simulated by using NMOS Procem window shown in Figure 1. The parameters that used for the simulation were gate length, doping concentration, oxide thickness, drain voltage, gate voltage and threshold voltage to find the value of drain current and leakage current. There are four graph obtained from this simulation, which are \( V_{TH} \) against \( T_{OX} \), \( I_D \) against \( V_D \) with varying \( V_G \), \( I_D \) against \( V_D \) with varying \( V_{TH} \) and \( I_{OFF} \) against \( V_D \) with varying \( T_{OX} \).

![Figure 1. NMOS_procem window in Sentaurus Workbench (SWB)](image)

3. Results and discussion

In this section, the variation of oxide thickness at 90 nm NMOS transistor was obtained by three factors which affect the drain current \( I_D \) and leakage current \( I_{OFF} \). The factors are threshold voltage \( V_{TH} \), gate voltage \( V_G \) and oxide thickness \( T_{OX} \). A total of four graphs were plotted to see the effect of \( I_D \) against
these factors. The first graphs were plotted $V_{TH}$ against $T_{OX}$. The other three graphs were plotted by varying the value of $V_G$, $V_{TH}$ and $T_{OX}$ in Sentaurus Workbench tool to obtain $I_D$ and $I_{OFF}$. All of the graphs were plotted based on result obtained in Sentaurus TCAD simulation.

3.1. $V_{TH}$ against $T_{OX}$
In this simulation, it is assumed that gate length $L$ is 90nm, doping concentration, $N_A$ is $4.7\times10^{17} \text{cm}^{-3}$, $N_D$ is $1\times10^{18} \text{cm}^{-3}$ and varies value of $T_{OX}$ from 1.2 nm to 2.8 nm to obtained values of $V_{TH}$. The values of $T_{OX}$ that used for simulation were recorded in Table 1 the associated graph is shown in Figure 2.

| $T_{OX}$ (nm) | $V_{TH}$ (V) |
|--------------|--------------|
| 1.2          | 0.36         |
| 1.4          | 0.36         |
| 1.8          | 0.37         |
| 2.2          | 0.38         |
| 2.8          | 0.39         |

Figure 2. Changing of $V_{TH}$ against $T_{OX}$

From Figure 2, it is observed that the $V_{TH}$ is directly proportional with $T_{OX}$. As the $T_{OX}$ increase, the $V_{TH}$ increase in proportion to the $T_{OX}$.

3.2. $I_D$ against $V_D$ with varying $V_G$
In this simulation, $T_{OX}$ is 1.2 nm, with both $V_D$ and $V_G$ are varied. The simulated $I_D$ were recorded in Table 2 and the graph is shown in Figure 3.
Table 2. Values of $I_D$ against $V_D$ with several $V_G$

| $V_D$ (V) | $V_G$ = 1.0 V | $V_G$ = 1.5 V | $V_G$ = 2.0 V | $V_G$ = 2.5 V | $V_G$ = 3.0 V |
|-----------|--------------|--------------|--------------|--------------|--------------|
| 0.5       | 0.019        | 0.036        | 0.044        | 0.049        | 0.053        |
| 1.0       | 0.020        | 0.044        | 0.064        | 0.076        | 0.083        |
| 1.5       | 0.021        | 0.045        | 0.068        | 0.088        | 0.101        |
| 2.0       | 0.021        | 0.046        | 0.070        | 0.091        | 0.109        |
| 2.5       | 0.022        | 0.046        | 0.070        | 0.092        | 0.112        |
| 3.0       | 0.022        | 0.047        | 0.071        | 0.093        | 0.113        |
| 3.5       | 0.022        | 0.047        | 0.071        | 0.094        | 0.114        |
| 4.0       | 0.022        | 0.047        | 0.072        | 0.094        | 0.115        |
| 4.5       | 0.023        | 0.048        | 0.072        | 0.095        | 0.115        |
| 5.0       | 0.023        | 0.048        | 0.072        | 0.095        | 0.116        |

Figure 3. Changing of $I_D$ against $V_D$ with several $V_G$

Referring to Figure 3, the $I_D$ changes linearly with $V_D$ before reaching its saturation value. For small large value $V_D$, the values of $I_D$ increase until $V_D = 2$V. The only difference for these graphs is the changes in $V_G$. It is observed that the $I_D$ increases with the increasing of $V_D$ and $V_G$. After the saturation point is achieved, the value of $I_D$ will remain constant.

3.3. $I_D$ against $V_D$ with varying $V_{TH}$

The values of each parameter that used for simulation were recorded in Table 3 and the associated graph is shown in Figure 4.
Table 3. Values of V_th for different N_a and L

| V_D (V) | I_D (mA) | V_th = 0.38 V | V_th = 0.44 V | V_th = 0.50 V | V_th = 0.57 V |
|---------|----------|----------------|----------------|----------------|----------------|
| 0.5     | 0.062    | 0.059          | 0.057          | 0.055          |
| 1.0     | 0.097    | 0.094          | 0.091          | 0.088          |
| 1.5     | 0.119    | 0.114          | 0.120          | 0.107          |
| 2.0     | 0.131    | 0.125          | 0.121          | 0.116          |
| 2.5     | 0.137    | 0.130          | 0.125          | 0.120          |
| 3.0     | 0.141    | 0.133          | 0.127          | 0.121          |
| 3.5     | 0.143    | 0.134          | 0.128          | 0.122          |
| 4.0     | 0.144    | 0.135          | 0.129          | 0.123          |
| 4.5     | 0.145    | 0.136          | 0.130          | 0.124          |
| 5.0     | 0.146    | 0.137          | 0.130          | 0.125          |

Figure 4. Changing of V_th for different N_a and L

In Figure 4, it is observed that the increment of I_D is linear as V_D is increased for small V_D. I_D is linearly increased in non-saturation region and start to saturate when achieved the saturation bias point. After the saturation bias point the drain current will remain constant. When V_D increases, I_D also increases with various value of threshold voltage.

3.4. I_off against V_D with varying T_OX

The values of each parameter that used for simulation were recorded in Table 4 and the associated graph is shown in Figure 5.
Table 4. Values of $I_{OFF}$ against $V_D$ with varies of $T_{OX}$

| $V_D$ (V) | $T_{OX} = 1.4$ nm | $T_{OX} = 1.8$ nm | $T_{OX} = 2.2$ nm | $T_{OX} = 2.8$ nm |
|-----------|------------------|------------------|------------------|------------------|
| 0.5       | 2.45E-09         | 9.66E-11         | 1.59E-11         | 4.67E-12         |
| 1.0       | 8.06E-09         | 1.96E-10         | 2.50E-11         | 6.22E-12         |
| 1.5       | 2.05E-08         | 3.50E-10         | 3.62E-11         | 7.79E-12         |
| 2.0       | 4.40E-08         | 5.73E-10         | 4.84E-11         | 9.47E-12         |
| 2.5       | 8.28E-08         | 8.37E-10         | 6.37E-11         | 1.14E-11         |
| 3.0       | 1.39E-07         | 1.21E-09         | 8.31E-11         | 1.32E-11         |
| 3.5       | 2.08E-07         | 1.73E-09         | 1.06E-10         | 1.49E-11         |
| 4.0       | 2.98E-07         | 2.42E-09         | 1.29E-10         | 1.68E-11         |
| 4.5       | 4.14E-07         | 3.24E-09         | 1.56E-10         | 1.90E-11         |
| 5.0       | 5.57E-07         | 4.30E-09         | 1.88E-10         | 2.16E-11         |

Figure 5. Changing of $I_{OFF}$ against $V_D$ with varies of $T_{OX}$

Figure 5 illustrates the $I_{OFF}$ against $V_D$ with varying $T_{OX}$ at $V_G=3.0$V. The graph shows various values of $T_{OX}$ to see the effect of $T_{OX}$ instead of $I_{OFF}$. The $I_{OFF}$ decreases as the $T_{OX}$ increase due to increment in $T_{OX}$ that causes the $I_{OFF}$ to decrease. It shows that when oxide thickness increase than the gate leakage current decrease. This observation suggests that as the oxide thickness becomes thicker, there is a low leakage current and when the oxide thickness is low there are high leakage currents present.
4. Conclusion
In this work, modelling of $T_{ox}$ variation has been carried out and investigation of its effect over the transistor performance is presented. The simulation results show that the $V_{th}$ is directly proportional to $T_{ox}$ whereas $I_D$ is directly proportional to $V_D$ for various $V_G$ and $V_{th}$ up to the boundary of its saturation level. In addition, the simulation results also illustrates that the $I_{OFF}$ is increased as $T_{ox}$ becomes thinner. A trade off exists to achieve improvement in device performance as suggested by the simulation results. Thinner $T_{ox}$ contributes to higher $I_D$ since $V_{th}$ is suppressed. However, thinner $T_{ox}$ also leads to higher $I_{OFF}$, which is undesirable in transistor operation. Therefore, the $T_{ox}$ need to be optimised in such a way that both $I_D$ and $I_{OFF}$ tuned the desired level.

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