TOPICAL REVIEW

Electric-double-layer-gated transistors based on two-dimensional crystals: recent approaches and advances

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Abstract

Electric-double-layer (EDL) gated transistors use ions in an electrolyte to induce charge in the channel of the transistor by field-effect. Because a sub-nanometer gap capacitor is created at the electrolyte/channel interface, large capacitance densities (~µF cm⁻²) corresponding to high sheet carrier densities (10¹⁴ cm⁻²) can be induced, exceeding conventional gate dielectrics by about one order of magnitude. Because it is an interfacial technique, EDL gating is especially effective on two-dimensional (2D) crystals, which—at the monolayer limit—are basically interfaces themselves. Both solid polymer electrolytes and ionic liquids are routinely used as ion-conducting gate dielectrics, and they have provided access to regimes of transport in 2D materials that would be inaccessible otherwise. The technique, now widely used, has enabled the 2D crystal community to study superconductivity, spin- and valleytronics, investigate electrical and structural phase transitions, and create abrupt p-n junctions to generate tunneling, among others. In addition to using EDL gating as a tool to investigate properties of the 2D crystals, more recent efforts have emerged to engineer the electrolyte to add new functionality and device features, such as synaptic plasticity, bistability and non-volatility. Example of potential applications include neuromorphic computing and non-volatile memory. This review focuses on using ions for electrostatic control of 2D crystal transistors both to uncover basic properties of 2D crystals, and also to add new device functionalities.

1. Introduction

Electrical double layer (EDL) gating is a technique in which ions in an electrolyte are used to control charge transport in an electronic material by field-effect. The electrolyte is electrically insulating—similar to a metal oxide gate dielectric—but ionically conductive, and therefore mobile ions undergo drift diffusion in response to an applied gate voltage. The primary advantage of EDL gating is the high fields (~10 MV cm⁻¹) and therefore large charge densities (~10¹³ to 10¹⁴ cm⁻²) that can be induced in organic [1] and inorganic materials, including metal oxides [2] and 2D crystals [3]. The high doping levels at the interface between the electrolyte and the contacts provides another benefit: Schottky-barrier thinning that makes tunneling a more favorable conduction mechanism than thermal-mediated injection over the barrier [4–6]. Such strong gate control and decreased contact resistance enables the exploration of new regimes of transport that cannot be accessed with traditional gate dielectrics.

A secondary advantage to EDL gating is that the technique is straightforward compared to, for example, atomic or molecular deposition of an inorganic dielectric on a surface that is free of dangling bonds. Instead, solid polymer electrolytes based on polyethylene oxide (PEO), and ionic liquids such as DEME-TFSI ¹ are commonly deposited by simple drop-casting or spin-coating from solution. Either a side gate or a top gate can be used to control the location of the ions (figure 1) with side-gating as a particularly attractive layout.

¹N,N-diethyl-N-methyl-N-(2-methoxyethyl) ammonium bis(trifluoromethanesulfonyl) imide.
Figure 1. EDL-gating mechanisms on 2D FETs in various configurations. (a) Top gated EDLT geometry and corresponding ion distributions under (b) zero gate bias ($V_G = 0$), (c) positive and (d) negative gate biases. When $V_G > 0$ or $< 0$, n- and p-type doping are achieved, respectively. (e) Side-gated EDLT geometry and (f) the corresponding ion distribution under positive side gate (SG) bias inducing n-type doping. (g) One example of using ions to induce a p-n junction by setting $V_S = -V_D$.

because the gate can be lithographically defined. In either geometry, a major advantage to EDL gating is that the strength of the gating depends weakly on the distance from the channel to the gate—permitting flexibility in the gate electrode location. One specific advantage to the side gate geometry is that it does not block the area above the channel as a top gate would, thereby allowing easier integration in optoelectronic devices such as photodetectors or photoemitters [7]. While the technique is uncomplicated, two important aspects need to be considered: (1) maintaining the gate voltage within the electrochemical window of the electrolyte to avoid electrochemical reactions that may be irreversible, and (2) avoiding water exposure which will screen the field and compromise the effectiveness of the gate (note that electrolytes are typically hygroscopic [8, 9]).

In the 2D materials community, EDL gating has been used both as a tool to explore transport and uncover exciting new physics such as spin polarization [10], photogalvanic current [11], current-induced circularly polarized electroluminescence [12] and superconductivity [13, 14], and also as the active material responsible for introducing new functionality such as synaptic plasticity for neuromorphic computing [15, 16], and non-volatility for memory [17, 18]. The basics of EDL gating on a 2D crystal are illustrated in figure 1, where the gate dielectric has been replaced with an electrolyte—a material with mobile anions and cations. When the gate voltage ($V_G$) equals zero, the ions are homogeneously distributed throughout the electrolyte (figure 1(b)). However, when the bias is set to a non-zero voltage, the ions respond to the applied field, forming two EDLs—one at the gate/electrolyte interface, and one at the channel electrolyte interface. At the channel interface, the EDLs are formed by cations (anions) in the electrolyte, and electrons (holes) in the channel when $V_G > 0$ ($V_G < 0$), figures 1(c), (d). A side-gated geometry is shown in figure 1(e) and the corresponding n-type doping in figure 1(f). EDL gating can also be used to create p-n junctions, and one approach is shown in figure 2(f) were $V_S = -V_D$.

The EDL formed by the ions and the induced charge in the channel can be regarded as a capacitor with thickness, $t_{EDL}$, and the capacitance can be estimated as

$$C_{EDL} = \frac{\varepsilon_r \varepsilon_0 A}{t_{EDL}}$$

where $\varepsilon_r$ is the relative permittivity (i.e. dielectric constant) and $\varepsilon_0$ is vacuum permittivity, and $A$ is the channel area. Because the thickness is very small—around 1 nm—the capacitance density is large (1–4 µF cm$^{-2}$) [3, 20]. One way to think about the EDL gate is that it is similar to physically moving a metal gate electrode to within ~1 nm of the channel. Approximately one-half of the gate voltage drops across each EDL of ~1 nm thickness, providing exceptionally strong gate control.

Because EDL gating is an interfacial technique, it is especially effective on molecularly thin 2D materials because they are essentially interface themselves. Thus, a large fraction of the literature investigating the
electronic properties of 2D crystals—mainly graphene and transition metal dichalcogenides (TMDs)—have employed EDL gating to explore transport. Several examples of 2D crystal EDLTs for which the hole and electron sheet carrier densities were measured directly using Hall effect are highlighted in Table 1.

While several excellent reviews covering EDL gating of organic semiconductors exist [29–31], and EDL gating for ‘iontronic applications’ in general [31, 32], this review focuses on EDLTs where the ions induce image charge in the 2D channel but do not exchange charge as they would in electrochemical gating where ions undergo reduction and oxidation reactions—such as those involved with intercalation [33]. We first summarize how EDL gating has moved the field of 2D electronic materials forward by its use as a tool to explore fundamental transport properties and to uncover exciting new physics (section 2), and then we highlight a more recent focus on the electrolyte itself, including custom-synthesized electrolytes that achieve novel functionalities (section 3).

2. EDL gating as a tool to explore transport in 2D crystals

The primary use of EDL gating by the 2D materials community has been to screen 2D material quality by measuring transport properties such as charge carrier density and mobility [5, 22, 24, 34–37]. Non-electrolyte based methods for characterizing transport in 2D materials often require either (1) the transfer of as-grown material to a dielectric substrate, which invariably changes the material’s properties because of interfacial interactions between the 2D material and the supporting substrate [38]; or (2) the deposition of a dielectric directly on the 2D material, which is challenging on a surface that is free of dangling bonds [39]. In contrast, EDL gating is far more straightforward than the approaches mentioned above, and has been applied to a wide range of 2D crystals. Because of the high fields and large capacitance densities that can be induced, EDL-gating has been particularly effective at uncovering new physics and materials properties, some of which are highlighted below.

### 2.1. Spintronics/valleytronics

2D crystals, especially TMDs, provide a promising platform for the study of novel physical properties and functionalities (e.g. spintronics and valleytronics), and EDL-gating provides a straightforward way to modulate the carrier densities of these materials. For example, while a variety of TMDs show ambipolar operation, MoS$_2$ is known to show mostly unipolar $n$-type conduction due to sulphur vacancies and fermi-level pinning [40–42]. However, large spin splitting occurs only in the valence band, and therefore hole conduction must be achieved for spintronic applications. While hole conduction has not been accessible using conventional gate dielectrics, including HfO$_2$ [19, 41], EDL gating can induce carrier densities that overcome the unintentional doping from sulphur vacancies to achieve $p$-type conduction in MoS$_2$. Zhang et al were one of the first to report EDLTs based on MoS$_2$ with on/off ratios greater than $10^5$ for both hole and electron transport [24]. The carrier densities they reported were in the range of $10^{14}$ cm$^{-2}$ for both the $p$ and $n$ branches, which is at least an order of magnitude larger than conventional FETs with solid dielectrics (e.g. $10^{13}$ cm$^{-2}$ on graphene FET with 300 nm SiO$_2$ oxide) [43].

While a previous review by Zhang et al in 2015 discussed the utilization of EDL gating and EDLTs in spintronics and valleytronics [31], here we will mention a few studies that have appeared since 2015. Wang

### Table 1. Electron and hole sheet carrier densities measured by Hall effect for 2D EDLTs.

| 2D crystal     | Thickness | Electrolyte | Max. electron density (cm$^{-2}$) | Max. hole density (cm$^{-2}$) | Ref. |
|----------------|-----------|-------------|-----------------------------------|-------------------------------|-----|
| Graphene       | 1 layer   | PEO:LiClO$_4$ | $4 \times 10^{14}$               | $4 \times 10^{14}$           | [3] |
| Graphene       | 1, 2, 3 layers | DEME-TFSI | $2 \times 10^{14}$               | $2 \times 10^{13}$           | [21] |
| Graphene       | 2 layers  | PEO:LiClO$_4$ | $1 \times 10^{14}$               | $5 \times 10^{13}$           | [22] |
| Graphene       | 2 layers  | PVA:LiClO$_4$ | $6 \times 10^{13}$               | $1 \times 10^{14}$           | [23] |
| MoS$_2$        | 15 nm     | DEME-TFSI | $1 \times 10^{14}$               | $0.75 \times 10^{14}$        | [24] |
| MoS$_2$        | 20 nm     | DEME-TFSI | $1.2 \times 10^{14}$             | —                             | [19] |
| MoS$_2$        | 1–6 layers | DEME-TFSI | $1 \times 10^{14}$               | —                             | [14] |
| MoS$_2$        | 4–10 layers | BMPPD-TFSI* | $1 \times 10^{14}$               | —                             | [25] |
| MoS$_2$        | 60 nm     | DEME-TFSI | $1.7 \times 10^{14}$             | $1.6 \times 10^{14}$         | [13] |
| MoTe$_2$       | 20–100 nm | BMIM-BF$_4$ | $0.45 \times 10^{14}$            | $0.7 \times 10^{14}$         | [13] |
| MoTe$_2$       | 1 layer   | DEME-TFSI | $2.2 \times 10^{14}$             | —                             | [26] |
| WS$_2$         | 20 nm     | DEME-TFSI | $1 \times 10^{14}$               | —                             | [27] |
| Tellurene      | $\sim 15$ nm | PEO:LiClO$_4$ | —                                 | $1.6 \times 10^{13}$         | [28] |

* 1-butyl-1-methylpiperidinium bis(trifluoromethanesulfonyl)imide

* 1-Butyl-3-methylimidazolium tetrafluoroborate
shown in figure 2(a) outperforms the ionic liquid, with electron accumulation occurring at a significantly reduced gate voltage, superconductivity in the TMD metal, NBSe$_2$ and oxidation does not occur). For example, DEME-TFSI was used to demonstrate the reversible tuning of Cr$_{17}$Ge$_2$Te$_6$ measured by Hall effect.

Accessing superconductivity in 2D crystals requires achieving sheet carrier densities on the order of $10^{14}$ cm$^{-2}$, thereby motivating the use of EDL gating. Multiple groups have shown that even $6 \times 10^{13}$ cm$^{-2}$ is too low to induce superconductivity in MoS$_2$ [14, 19], MoSe$_2$ [13], and WS$_2$ [27]. This is illustrated in figure 2(a) for MoS$_2$ specifically, where $T_c$ (i.e. the temperature at which the four-terminal sheet resistance reaches 90% of its normal state value) versus sheet carrier density is shown for EDL gating, along with the larger doping densities that would be required to achieve superconductivity via electrochemical doping [19]. Costanzo et al showed that the total charge induced by the EDL gate is the important figure of merit and not the amount of charge per layer (at least for MoS$_2$). Specifically, both single and bilayer MoS$_2$ require at least $1 \times 10^{14}$ cm$^{-2}$ to induce superconductivity, making the charge density per layer twice as large in the monolayer as the bilayer [14]. This is noteworthy because the bilayer thickness is still within the electrostatic screening length of the EDL gate, but it seems to have no effect on the total density required.

Ionic liquids are the most common electrolyte used to induce superconductivity in 2D crystals, and one reason for the preference is the large electrochemical window (i.e. the voltage window over which reduction and oxidation does not occur). For example, DEME-TFSI was used to demonstrate the reversible tuning of superconductivity in the TMD metal, NBSe$_2$ [46]. DEME-TFSI [19] and BMPPD-TFSI [25] have been used to demonstrate superconductivity in MoS$_2$, where the gate voltage was pushed to 6 V in both studies. However, in the case of DEME-TFSI, a subsequent report by the same group showed that (PEO)$_2$KClO$_4$ outperforms the ionic liquid, with electron accumulation occurring at a significantly reduced gate voltage, shown in figure 2(b) [13]. Moreover, difficulty maintaining interfacial contact between the ionic liquid and the semiconducting channel at low temperature has been cited as a problem by the Morpurgo group [27, 14].

In addition to superior gate control and mechanical properties, PEO:KClO$_4$ provided access to the electrochemical modulation of charge transport in WS$_2$ by enabling operation at $V_G > 6$ V. The resulting ion intercalation increased the capacitance density to 200 $\mu$F/cm$^2$ corresponding to $n_i = 5 \times 10^{15}$ cm$^{-2}$ [13] as measured by Hall effect.
2.3. Metal-insulator transitions

Accessing multiple electronic states within a single 2D material could be useful for various electronic and optoelectronic applications. For example, if the bandgap of a semiconducting 2D crystal could be reversibly collapsed by field effect over sufficiently short timescales, this approach could be useful as a switch. Ion intercalation into 2D crystal FETs can induce various electrical phase transitions (e.g. Li intercalation into 1 T-TaS$_2$ [47]) or structural phase transitions (e.g. Li intercalation into MoS$_2$ [33]) via charge transfer from the metal atom to the 2D crystal. However, we have restricted our review to electrostatic control of phase transitions for which demonstrations are just emerging. One example is a recent demonstration by Ren et al [28], in which PEO:LiClO$_4$ was used to induce the insulator-to-metal transition in Tellurene FETs at hole densities $>1 \times 10^{13}$ cm$^{-2}$. Based on nA gate-to-source leakage currents, the phase change was induced without the aid of electrochemistry.

Specific to TMDs, the 2 H–1 T semiconducting to metallic structural phase transition has received much attention, as highlighted in a recent review [48]. The energetic barriers to transition from one polymorph to another was modeled using density functional theory (DFT) by Duerloo et al for a variety of TMDs including MoS$_2$, MoSe$_2$, WS$_2$, WSe$_2$, MoTe$_2$ and WTe$_2$ [49]. In a follow-up publication by the same group, Li et al used new DFT methods to predict that electrostatic gating is sufficient to induce the semiconductor-to-metal phase transition in TMDs [50]. Specifically, MoTe$_2$ was identified as the leading candidate due to the relatively low (2–4 V) gate voltages predicted to induce the transition.

With focus now on MoTe$_2$, Hwang and co-workers modeled the impact of lithium gating, also using DFT [51]. In their model, they push Li to the surface of MoTe$_2$ and, through charge transfer, allow the Li to provide the compensating charge to reflect the double layer at the interface. One key finding is that the presence of Li$^+$ next to the MoTe$_2$ at doping densities $>2 \times 10^{14}$ cm$^{-2}$ lowers the energy barrier to the phase transition from 0.84 to 0.3 eV, as shown in figure 3. Based on attempt frequency analysis, this energy barrier corresponds to a switching rate of 10–100 MHz between the two phases.

Theory suggests that the 2 H to 1 T' phase transition can be accessed electrostatically, but to do so, a delicate balance must be struck between achieving sufficient charge density to electrostatically induce the phase transition (~$10^{14}$ cm$^{-2}$), but without applying too much voltage to induce intercalation electrochemistry. Such a balance was reported for monolayer MoTe$_2$ FETs gated by DEME-TFSI, where a structural phase transition was induced at side gate voltages >2.8 V [26]. The authors suggest that electrochemistry is not expected because the experiments were conducted at 220 K and the gate voltage was held below 4.5 V. The 2 H–1 T' phase transition was confirmed via well-defined shifts in Raman peak locations while sweeping the gate voltage, along with a large (~1.8 V) hysteresis in the relative Raman scattering intensity. However, a recent report [52] describes a more complicated scenario where electrochemistry between the electrolyte and the MoTe$_2$ drives the formation of Te vacancies which favor the transition from 2 H to 1 T. While no such insulator-to-metal transition was observed in a prior report using PEO:CsClO$_4$ to gate MoTe$_2$ FETs, the MoTe$_2$ was multi-layer and the maximum doping density was only $1.6 \times 10^{15}$ cm$^{-2}$ at an electrolyte gate voltage of only 1 V—well within the electrochemical window [53]. As
advances in wide-area, defect-free 2D materials growth continue along with the refinement of EDL-gating techniques, we predict increased efforts to demonstrate EDL-controlled modulation of TMD polymorphs with distinct electrical properties.

2.4. P-n Junctions

Another unique feature of EDL gating is the ability to create p-n junctions in 2D crystals, and to reconfigurably adjust the doping density in both the n and p regions. Zhang et al [54] were among the first to
electronically control and locate $p$–$n$ junctions in EDL-gated MoS$_2$ transistors. The device geometry is shown in figure 4(a). A $p$–$n$ junction can be created through ion accumulation by controlling the potential difference between the source, drain, and gate electrode. For example, when the source and drain electrodes are negatively and positively biased, respectively, while the gate electrode is grounded, cations accumulate near the source electrode and create electron doping in the adjacent region, while a hole doped region exist near the drain terminal. At the center of the channel where these two regions meet, a $n$–$p$ junction is formed, with a position that can be tuned depending on the bias conditions. The junctions displayed rectifying $I$–$V$ characteristics between source and drain. Using two additional probe electrodes (i.e. a total of four-terminal (4 T) configuration, figure 4(b)), the voltage drops are measured across the two inner probes ($V_{4\;g}$) to detect the location of the $p$–$n$ junction (figure 4(d)). When a junction is formed between the two sensing probes, the $V_{4\;g}$ is non-zero.

A $p$–$n$ junction can be created with EDL gating even without a gate electrode. Xu et al demonstrated that an in-plane electric field can be used to establish a cation/anion transition region, forming a $p$–$n$ junction in the 2 H–MoTe$_2$ channel [53]. Using a 4-terminal geometry, both unipolar doping and $p$–$n$ junction doping can be simultaneously achieved in separate regions of the device by the selection of terminal biases (figure 4(e)). This junction is locked in place by decreasing the temperature of the device below the glass transition temperature ($T_g$) of the electrolyte (figure 4(f)). $I$–$V$ characteristics show rectifying behavior between the two inner terminals (2 and 3 as shown in figure 4(h)) and outer terminals (1 and 4), indicating a $p$–$n$ junction in the channel between terminals 2 and 3. However, between terminals 1–2, and 3–4 the output characteristics are ohmic, indicating that unipolar doing exists between these pairs of electrodes, and the ion doping increases the tunneling transparency of the Schottky contacts (figure 4(g)). The ideality factor of the $p$–$n$ junction is 2.3, suggesting that the junction is recombination dominated.

In addition to using thermal quenching (i.e. operating temperature $<$ $T_g$ of the electrolyte [23]) to lock the $p$–$n$ junctions, room temperature operation is also possible. Liang et al demonstrated a gateless lateral $p$–$n$ junction with reconfigurability on graphene using a custom-synthesized electrolyte [55]. Specifically, a doubly-polymerizable ionic liquid (DPIL) was locked by thermally triggered polymerization that enabled room temperature operation, and it was directly compared to a thermally locked $p$–$n$ junction formed by a (PEO)-based electrolyte. Both approaches show two current minima in the backgated transfer measurements, which is a signature of a graphene $p$–$n$ junction.

In previous examples, the spacing between the two electrodes used to create lateral $p$–$n$ junctions is on the order of micrometers. When this distance is reduced to tens-of-nanometers, and if the $n$- and $p$-type regions adjacent to the $p$–$n$ junction are degenerately doped by the EDL, quantum mechanical band-to-band tunneling (BTBT) can be observed. Paletti et al reported the experimental demonstration of an EDL Esaki junction in synthetic WSe$_2$ thin films [56]. Negative differential resistance (NDR) was detected in the $I$–$V$ measurements. Their device exhibits repeatable, gate-tunable band-to-band tunneling with NDR at temperatures up to 140 K. Numerical simulations were used to determine the bias dependence of the equilibrium ion and carrier density profiles, which showed that degenerate and abrupt doping profiles are achievable, and additional backgate voltage can control the junction location, allowing the NDR to be gate-tunable.

3. EDL gating to add new functionality

Although the majority of EDLTs use ions to uncover transport properties or new physics in 2D crystals, more recent efforts have focused on engineering the electrolyte to add new functionalities. In these cases, the electrolyte is not simply a tool to investigate basic properties of the 2D crystals, but the electrolyte itself adds some feature to the device that cannot be achieved without ions. Below we highlight three such areas in which the electrolyte is the active layer responsible for new functionalities.

3.1. EDL gating using dual-ion conductors for neuromorphic computing

Synaptic devices and neuromorphic systems have the potential to break away from the conventional von Neumann paradigm and deliver distinctive properties such as parallelism and ultra-low power consumption [57]. However, the implementation of synapses in today’s artificial neural networks are based on the conventional digital complementary metal-oxide-semiconductor (CMOS) devices, which still require a large number of transistors (e.g. 5.4 billion) [58] and significantly larger power consumption than the human brain (e.g. 26 pJ [58] vs 20 fJ [59] per synaptic event). In recent years there has been a growing interest in artificial synaptic devices that can truly mimic the functionality of brain, and one of the promising candidate is EDLT with dual-ion conductors.

For the concept of using EDLTs to mimic synaptic functions, 2D materials were not an initial focus. Short-term synaptic plasticity was demonstrated on materials such as carbon nanotubes (CNT) [60, 61] and
conducting polymers [62]. Kim et al reported an EDL-gated CNT transistor using PEG for mimicking excitatory post-synaptic current (EPSC) [60]. Pre- and post-synaptic spikes are applied on the gate and drain electrodes, respectively. A pre-synaptic voltage spike (5 V, 1 ms) at the gate triggers EDL formation at the CNT channel and changes the EPSC, which decays back to its original value in tens of ms—the same timescale of EPSC in biological excitatory synapses. The average energy consumption, calculated by integrating the power consumption of the CNT synapses during the time of an EPSC, is 7.5 pJ spike$^{-1}$, which is 100x lower than the energy consumption by conventional CMOS circuits (900 pJ spike$^{-1}$) [63].

In addition to ionically conductive polymer electrolytes such as PEG, several groups utilized a proton-conducting phosphorus SiO$_2$ electrolyte for creating synaptic pulses [64–66]. Wang et al [65] demonstrated a two-synapse network using two, solid-state SiO$_2$ electrolyte-gated transistors. Gate voltage moves the protons within the SiO$_2$ electrolyte to form EDLs at indium-zinc oxide channel interface. Utilizing the short-term synaptic plasticity of the EDLTs, the device can be used as a high-frequency filter where the excitatory post synaptic current (EPSC) increases with frequency. Their study also utilized the dependence of the current gain of EPSCs on input presynaptic spike frequencies to achieve logic ‘ADD’ function, which shown the potential of EDLTs for synaptic computation.

More recently, EDLT-based synaptic devices were demonstrated on 2D materials. In addition to offering better mobility and conductivity than oxide thin films, one unique advantage of using 2D crystals as the channel is the possibility of integrating photonic components in the system to provide an additional range of modulation. For example, Jiang et al reported a photoelectronic hybrid synaptic device based on EDL gated MoS$_2$ transistors (figure 5) [15]. Electrically, the synaptic potentiation can be realized using an EDL formed between the interface of a sodium alginate electrolyte and MoS$_2$. Optically, both the synaptic potentiation and depression can be achieved by high and low frequency light stimuli, respectively. The authors attribute the depression to the charge-trapping of photoelectrons that leads to decreased channel conductance.

Combining the two types of stimuli, spiking time dependent plasticity (STDP) behavior was demonstrated...
with the electrical and optical stimuli serving as the pre- and post-synaptic neurons, respectively. While the electric and optic pulse widths utilized in their study are on the order of tens of ms for triggering a response, Xu et al has reported the tuning of EDL formation speed on 2D crystals with electric field by more than five orders of magnitude [67], suggesting the potential to substantively reduce the pre-synaptic pulse width.

In addition to pure electrostatic gating using EDLs, researchers are also looking into synaptic device concepts that combine EDL gating with electrochemical reactions to achieve short-term and long-term plasticity, respectively. For example, Zhu et al [16] demonstrated synaptic transistors based on WSe2 (figure 5(d)), NiPS3, and FePSe5, with minimal energy consumption down to ∼30 fJ spike·1. When a single pulse was applied to the gate electrode, an EDL forms at surface of the 2D materials but diffuses back into the ion gel after removing the gate bias, leading to short-term plasticity (STP, figure 5(e)). In contrast, when a train of voltage pulses were applied to the gate, Li+ is intercalated into the 2D materials (an electrochemical process) and cannot be liberated spontaneously after removing the gate bias. The device conductance cannot fully recover to the initial state, instead, a residual current (Ires) is observed, implying a transition to long-term potentiation (LTP, figure 5(f)). Similar coexistence of STP and LTP was demonstrated on graphene FETs by Sharbati et al [68] using a single programing pulse (figure 5(g)). They used lithium-ion phosphate as both the working electrode (i.e. gate) and reference electrode, and attributed the easier intercalation to the large ion diffusivity in graphene.

3.2. Monolayer electrolyte and custom device design for EDL-gated nonvolatile memory (NVM)

High charge carrier densities at low operating voltage make EDLTs attractive, and the same attributes would also be useful for memory, for example, to create a large On/Off ratio at reduced power consumption. However, EDL gating is naturally volatile: EDLs dissipate on the timescale of microseconds to seconds [22, 67] after removing the applied bias. However, researchers have made different attempts to induce bistability in EDL-gated devices. One of the first reports in this direction was from Tsuchiya et al [69], who demonstrated non-volatile bandgap tuning of graphene oxide (GO) in an EDLT. There are two types of conductivity modulation that occurs: (1) a volatile conductivity modulation due to the electrostatic modulation of the carrier induced by the EDL at the GO/electrolyte interface, and (2) a non-volatile conductivity modulation caused by redox reactions between GO and reduced GO (rGO) that leads to a bandgap change and a five order of magnitude change in conductivity. In their design, an electrochemical reaction (i.e. GO to rGO) is required to achieve nonvolatility, and the response speed is limited to below 10 Hz. However, other groups have reported non-electrochemical approaches by stacking the electrolyte where the EDL forms with a nonvolatile or a charge trapping material. Fabiano et al [70] used a polyelectrolyte to translate the polarization of dipoles along the surface of a ferroelectric thin film to the EDLs formed at the ferroelectric/electrolyte and electrolyte/semiconductor interfaces. The memory effect originates from the ferroelectric layer, while the EDLT enables low power and non-destructive reading of the memory. They reported a response time of ∼0.2 ms and a retention time of >10^8 s, but the Vg required to switch the devices is rather high (>7 V) due to the relatively high coercive field of ferroelectric material. Koo et al [71] inserted a layer of Au Nanoparticles (NPs) between the electrolyte and the channel layer, which served as trapping sites to the changes induced in the EDL and therefore store the electrical input signals. The organic ligands attached onto the colloidal gold NPs prevented the escape of the trapped charges from the particles and enhanced the retention. They used 1 ms pulses to program/erase their device and observed a retention as long as 10^5 s.

Other than utilizing additional material to create bistability, another approach is to engineer the electrolyte directly to create an energy barrier for switching between two different configurations that have distinct electrostatic doping effect. Xu et al [17] first reported the nonvolatile electrostatic gating of graphene FETs using a ‘monolayer electrolyte’ consisting of cobalt crown ether phthalocyanine (CoCrPc) and LiClO4. The crown ethers (CEs) on the CoCrPc solvate lithium ions which induce image charges and dope the graphene channel. The CEs provide two stable states for the Li+: one near the graphene channel (i.e. low-resistance state) and one ∼5 Å away from the channel (i.e. high-resistance state), and the switching between the states can be modulated by a gate bias. The retention of the two states is observed for longer than 2 × 10^4 s, but the memory window and On/Off ratio the device is limited due to the lack of a bandgap in graphene. To enlarge the memory window, Liang et al [18] applied the molecularly thin electrolyte on WSe2 FETs (figure 6) and encapsulated the devices with few layers of h-BN to further improve the bistability—consistent with predictions by density functional theory (DFT). An On/Off ratio of 10^4 ∼ 10^5 was observed while reading at VBG = 0 V, which is repeatable for more than 1000 cycles and the retention time for each state exceeds 6 h (max cycles and time measured). The minimal pulse width tested is 1 ms, which is similar to existing flash memory, while the On/Off ratio remains >10^5. DFT calculations predicted that a vertical electric field of 0.15 V Å−1 will lower the energy barrier to Li+ diffusion from 0.29 eV to 0.20 eV, suggesting the potential for lower operating voltage and faster response time (e.g. nanoseconds) [72].
3.3. **EDL gating using single-ion conductors**

The electrolytes highlighted above are dual-ion conductors (i.e. both the cations and anions are mobile and free to respond to an applied field). There also exists a well-studied class of ‘single-ion’ conductors where either the anions or the cations are immobilized, leaving only one type of ion free to respond to the electric field. The polyelectrolyte, Nafion, is one well-known example of a single-ion conductor which is used for, among other applications, actuation. In the case of Nafion, the actuation mechanism involves the inhomogeneous redistribution of solvent molecules on one side of the membrane that leads to bending via electrostatic forces and osmotic pressure differentials \[73\]. Although single-ion conductors have been the subject of much research in the polymers community, their use as an EDL gate for transistors has been infrequent and limited to organic semiconductors. By matching \(p\)- and \(n\)-type electrolytes (i.e. polyanions and polycations) with \(p\)- and \(n\)-type semiconducting channels, free ions only accumulate at the electrolyte/gate interface. Because the other ion is immobilized on the polymer backbone, ion diffusion into the channel, and electrochemistry with the semiconductor, is avoided \[74–76\].

Recently, Xu et al demonstrated the use of a custom-synthesized polyester single-ion conductor (PE400-Li) to EDL gate both graphene and MoTe\(_2\) transistors, and directly compared the performance to the dual-ion conductor, PEO:LiClO\(_4\), on the same devices \[77\]. For both the dual and single-ion conductors, the mobile cations provide similar enhancements to the \(n\)-branches of the transfer characteristics in both graphene and MoTe\(_2\), with an estimated sheet carrier density of \(\sim 10^{14} \text{ cm}^{-2}\). However, because the anion in the single-ion conductor is covalently tethered to the polymer backbone, and because the gate is much larger than the channel, \(p\)-branch conduction is suppressed. Modeling shows that the cationic depletion layer provides some degree of electrostatic gating, but the strength is significantly diminished compared to the anionic double layer present in the dual-ion conductor. In addition to suppressing \(p\)-type conduction, EDL gating using single-ion conductors is also a possible way to induce strain in a 2D crystal via field effect. As described above in section 2.3, some TMDs can undergo a 2 H–1 T\(’\) semiconducting to metallic phase transition, and MoTe\(_2\) is predicted to require the smallest amount of strain to undergo the transition \[49\]. Considering the strong electrostatic imbalance that can be provided by single-ion conductors, they may provide a pathway for field-controlled, low-voltage phase transitions in 2D crystals.
4. Conclusions and outlook

EDL gating of 2D crystals has proven to be an effective tool for uncovering fundamental properties of layered van der Waals crystals. From ultra-high doping densities and mobilities to superconductivity and spintronics, the community has benefited from this straightforward technique. Looking ahead, it is likely that EDL-gated 2D optoelectronic devices will gain more attention—especially because the side-gate geometry allows access to the channel. Another potential advantage is the analog nature of EDL formation and dissipation in response to a voltage spike, which makes it more ideal for neuromorphic computing—especially for spiking neural networks (SNN). In addition, by making use of the large interfacial electric fields, EDL gating is likely to become a key tool for uncovering quantum physical properties. For example, it has been shown that the topological phase and quantum spin hall (QSH) effect can be modulated by an applied electric field; however, the required critical field is difficult to achieve with conventional dielectrics (e.g. >5 V nm$^{-1}$ for 3 layer phosphorene [78]). Opportunities abound for tailoring the electrolyte—from tuning the Tg to immobilizing one type of ion to scaling the electrolyte to its ultimate limit—ion-conductive macromolecules represent a virtual playground for adjusting chemical, mechanical and electrical properties to impart new device functionalities in EDLTs.

Despite all of the progress, EDL gating is not without its challenges. To induce only electrostatic effects—which do not disturb the band structure of the 2D crystal as substitutional doping does—ions in the electrolyte can only interact with charge in the channel through Coulomb interactions. If reduction and oxidation reactions that change the chemistry of the 2D crystal are to be avoided, then care must be taken not to exceed the electrochemical window of the electrolyte. However, this voltage window is not abrupt and depends on both the channel material and the electrolyte, and thus care must be taken to monitor and report current from all terminals to provide a more complete picture of the doping mechanisms involved.

As the community of 2D crystal researchers refine our EDL gating procedures, and remain diligent to report important experimental details, we can expect EDL gating to transition from a tool that is almost exclusively used to explore the basics of electrical transport in 2D crystals, to an integral part of 2D devices with unique electrical and optical characteristics. As device researchers partner with polymer- bio- and electro-chemists to customize electrolytes and work to replicate the biochemistry and electrical signaling found in nature, we can anticipate important discoveries at the boundary between 2D layered materials and ion-conductors.

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