Design of implantable cardioverter defibrillator using low power subthreshold digital circuit

T Vasudeva Reddy 1, B Nareshkumar 2, R Anirudh Reddy 3, P Kavitha Reddy 4

1 Associate Professor, ECE Department, B V Raju Institute of Technology, Narsapur, Telangana, India
2,3,4 Asst. Professor ECE Department, B V Raju Institute of Technology, Narsapur, Telangana, India

vasu.tatiparthi@bvrit.ac.in, nareshkumar.b@bvrit.ac.in, anirudhreddy.r@bvrit.ac.in, kavithareddy.p@bvrit.ac.in

Abstract. Due to tremendous Technological advancements researchers and scientists have proposed designs operating under subthreshold and near threshold regions. With recently, growing the need for low power consumption of devices, the low power circuits have become more eye-catching to the design engineers. But the act of subthreshold design has become more profound to the PVT variations due to exponential relationship of current in Subthreshold region depends on supply voltage(Vgs) and threshold voltage(Vth). The motivation for low power electronics has been derived from the subthreshold operation & its driving forces. In this paper the subthreshold design of source coupled logic circuit is described with its functionality under subthreshold region and performance in static and dynamic mode of operation and used as Implantable cardioverter defibrillator under 28nm technology.

1. Introduction

Now a day’s human life span is reduced by many factors mainly due food, social life and other factors that leads to unhealthy. Most common problem of heart attack and failure. So to improve the life span of person and protect from heart attack, pacemakers are introduced to control heart rhythms. The functionality of pacemaker is used to speed up slow heart rates and sometimes they used to slowdown fast heart rates. Pacemakers standardize functionality of bouncing, de-bouncing also to regulate heart rates. When pacemakers are inserted in body it cannot be replaced every time, operating normally life span of 5 year’s maximum. Here in this paper we discuss the circuit that takes mininum power there by extend the lifetime of battery for portable pacemaker electronic circuit. This is the most encouraging motivation to design a memory with low power functioning in subthreshold operation and power consumption and dissipation [1-3]. Functionality is at the cost of performance depends on technology. Circuits that are modelled under subthreshold withdraw the limitation by modelling devices with sizing and alternative techniques. In this paper, we have described the SRAM implementation using GDI based technique takes the feedback signal boosted and compared by internal circuit that leads to low power consumptions of the design and thereby increasing the life span of battery that is used for functioning life time [4].
1.1. Design & Simulation of Traditional Subthreshold SRAM

Implementation of traditional 8T SRAM using CMOS design to improve the SNM (static noise margin). The SNM and stability can be improved directly between bit cell and the storage node cell to improve the leakage, dynamic and static power, this can be obtained by charging and discharging of the single bit line represented in Figure 1.

![Figure 1](image1.png)

**Figure 1.** 8T SRAM used as memory in Defibrillator

In order to address functionality read and write operations are separated by stacking of transistor that are applied to the 6T SRAM. A memory circuit with the Cmos technology transistor under 32nm is showed shown in Figure 2.

![Figure 2](image2.png)

**Figure 2.** Improved 8T SRAM schematic diagram

1.1.1. Write state functionality

The performance and stability of SRAM is improved by providing isolation between read, write bit line. An 8T model is useful to write operation and for reading operation. Set of stack transistors are used to control read and write operation by Write Word Line (WWL) & Read Word Line(RWL). During a read operation, read bit line (RBL) is pre-charged and WWL maintain as high logical state and that depends on value stored in cross coupled inverters and the operation is charges & discharging [5].

1.1.2. Read state functionality

The read state functionality defines the RBL discharges, treated as bit as '1' else it is treated as 0. In this case storage nodes are completely isolated from write bit lines. Therefore, the stability of SRAM is enhanced. But during a write operation, the WBL & WBLB lines are precharged to predetermined value. Then asserting write word line and nodes attain the corresponding values. During write operation, WBL and WBLB lines are precharged to predetermined voltages. Then, declaring the write
word line WWL and nodes inserts the values from the bit lines. Therefore, the stability is increased and the metal density, dynamic and leakage powers are greatly reduced [6].

1.1.3. Transient model analysis
The transients’ analysis is represented as below from Figure 3, with the supply voltage as 0.4v. either of the transistors will be on, as the CMOS is operating under subthreshold region.

![Figure 3. 8T SRAM Transient analysis](image)

1.1.4. Dc Model Analysis
The operating point of the dc analysis is analyzed from DC characteristics, when a DC load line crosses the middle of dc characteristics and is represented by the below Figure 4.

![Figure 4. 8T SRAM DC analysis](image)

Dynamic power is marked in read and write operation and non-functionality of the memory is also treated static characteristics. Dynamic power is major, when the circuit is operating in the threshold region of operation, where the technology is degrading and reduction in the supply voltage leads to static power or leakage power, which will dominate the dynamic power at when the technology is enhancing [7].

1.2. SRAM power analysis under Subthreshold
In generally, the power consumptions are idle. But in stand by mode, the static power and the leakage power is dominating. Therefore we need Subthreshold design SRAM power and its and the performance is estimated in 32nm.
1.2.1 ANALYSIS OF STATIC POWER DISSIPATION

In digital design static power dissipation is an important parameter. As the complexity of the circuit is keep on increasing nowadays, a SRAM is used in most of the cache memory design indicated by in Figure 5.

1.2.2 Total Power (Tpd) Dissipation

From Figure 6 the total power of the circuit is estimated by considering the static, leakage and dynamic power at different mode of operation like cut off, active and saturation. Normally the dynamic power is maximum, when the supply voltage of above threshold (Vgs>Vth)[8]. When in sub-threshold region, leakage power dominates as the supply voltage reduced than the threshold (Vgs<Vth) voltage and leakage power are dominating. Therefore, there will maximum power dissipation across the circuit.

1.3. SRAM delay analysis

In Subthreshold design SRAM delay is estimated in 32nm and the performance of delay is showed below

1.3.1 Rise time analysis

The rising time of the SRAM is estimated by considering the 2 % to 90 % of the output response, where the 2% is the minimum value and 90 % of the maximum value of the output. The difference in
the VoH to the VoL, Where the VoH is the maximum voltage in the total output and the VoL is the lowest voltage in the output voltage and vice versa in fall time denoted in the Figure 7 & Figure 8.

![Figure 7. Rise state of 205 Ps](image1)

1.3.2 Fall time

![Figure 8. fall time of 42 Ps](image2)

2. Subthreshold GDI Inverter Design

GDI Operation
To understand the analogy of the basic GDI cell, for the low swing issues based on the F1, and that will be improved and advanced for another GDI functions.
A below table 1 represents the full set of logical functions of GDI, when the values of A=0, B=0, the value of the output F1=Vtp instead of 0v. Because of reduced characteristics of high to where the low swing of operation of PMOS Transistors.

When A=0 and B=1, the demand that transition occurs only about 50%, The GDI cell is acts as a inverter when A=1 and B=0, which is largely used for the logic level restoration and finally when A=1 and B=1 GDI Cell is acts as CMOS inverter by producing 0 as an output voltage, [88,90].In some of the cases when the value VDD=1, without swing drop, GDI cell is acting like the inverter and recovering the voltage wings, and also it allows self-restoration in many cases. SRAM is design with only two transistors' [11] and low power dissipation & less delay by reducing the complexity of the circuit and the static noise margin can be greatly reduced.
2.1. DESIGN OF GDI MODEL

The Basic GDI function shows the simple GDI Based cell to realize the basic logic functions with a simple Boolean equation that is represented by circuit diagram Figure 9 and Figure 10 is denoted by schematic model.

![Figure 9. GDI design](image)

![Figure 10. Schematic diagram of GDI Cell inverter](image)

Implementation of all the logic functions is not possible with traditional P-well CMOS, but it can be implemented using SOI Technology. Table 1 CMOS logic will take only two transistors per function. GDI cell has a variation in of low swing voltage, low static power dissipation, less in complexity, less no of transistors [7-9].

### Table 1 Truth table of GDI Inverter

| G | P | N | OUT               | Output |
|---|---|---|-------------------|--------|
| 1 | 0 | 0 | pMOS Transmission gate | F0     |
| 1 | 0 | 1 | CMOS Inverter     | 1      |
| 1 | 1 | 0 | nMOS Transmission gate | 0      |
| 1 | 1 | 1 | CMOS Inverter     | 0      |
2.2. Operation

Operation of SRAM defines by considering read and write operation by applying the supply under subthreshold operation.

2.2.1 Write state operation

Write operation 0 into the SRAM, the word line should make to 1 and Bit line has to apply '0' VDD is applied to bitline Bar (BL) & Write Word Line (WWL) is inserted to make M1, M4 off. Hence value of Bit Line stores value of '0', stores the value at Q as showed in Figure 12.

2.2.2 Read state operation

Read Word Line (RWL) drives the access transistor M2 makes on. When the value stored at Q is equal to 0, then transistor M1 is off, as RBL is directly connect to ground and discharges through M5, M6. Finally, value stored in Q is 0 and QBAR is 1 indicated in Figure 13.
2.3. Modelling of SRAM using GDI technique

The GDI based SRAM indicates the Figure 14 indicate the schematic diagram of SRAM GDI. Both VDD and Vss are treated as input pins and reduces the dissipation of power. The SRAM cell using GDI techniques, is designed by considering four transistors are cross coupled to form inverters and another two transistors acts as access transistors [9]. To separate read and write operation.

2.3.1 GDI based SRAM design.

8T SRAM Cell view of Subthreshold GDI Based SRAM Library Cell using 32nm under subthreshold SRAM Cell diagram represented in Figure 14.

2.3.2 Write state Operation

The write state defines the value stored in cell earlier. When GDI logic acts as Inverter & buffer circuit, GDI CMOS takes the value and restores it. Also treats other two inputs are also 1 and 0. At this point of inputs 0,0[8-9]. A small amount of low voltage swing occurs with BL & WWL values are 0,0which are effected by low swing voltages represented by Figure 15.
2.3.3 Read Functionality

During the read, BL & WWL is 0,1 & 1,1 respectively. when values WWL and RBL are 1,1 GDI circuit is acts as an inverter. Considering BL and VDD are low, a high vtp is values is on state ie 1v instead of off state ie 0. is represented instead of 0v. The reason being here is poor value of 1 to 0 swing represented by Figure 16.

2.4. GDI characteristics
GDI based subthreshold SRAM is designed & analyzed the functionality with transient and dc analysis in 32nm and described below.

2.4.1 Transient Analysis
The analysis of transient characteristics is obtained by considering the pulse as input and the amount of voltage s are treated as 0.4 for a duration & some other duration will be treated as 0, with a subthreshold region of operation. considering the voltage drop at the input & current across that input node will parameters to estimate the functionality of transient analysis described in Figure 17.
Figure 17. GDI Transient Analysis

Figure 18. DC Analysis

Figure 18 denotes the DC analysis of SRAM cell using GDI. The above diagram indicating the dc analysis of GDI SRAM, where the dc load line is the middle point of the characteristics. This results can be obtained by considering the input values of dc with minimum current across it. Another variation is the technology based on the width and length of the transistor. A PMOS Transistors are designed in such a way that width is changed to 32nm, as it has less mobility of electrons and majority of holes. Therefore, the width dimensions are reduced by maintaining the length value are constant. As NMOS Transistors has the higher mobility of charge carriers of electron those are maintained at width value is 32nm.

2.5. **GDI Power Analysis**

GDI power analysis is estimated by Static, dynamic, total power and that has to need to consider under subthreshold operation of GDI SRAM.

2.5.1 **Static Power Dissipation**

Static power dissipation is the power due direct path between supply voltage that directly connects to ground. In GDI when the transistor is under subthreshold operation, the diode under reverse biased current that leads to parasitic capacitance that leads to leakage current. The leakage current forms between drain and source diffusion and also in the bulk of MOS regions. The of leakage current occurs when Supply voltage between gate and substrate is less than the threshold value Vgs <Vth. ie
transistor operating under subthreshold region of operation. Figure 19 showed below represents static power dissipation

![Figure 19. Power Dissipation in Static mode 0.6686µw](image)

2.5.2 Total Power (TPd) Dissipation
Switching activity of the transistor resulting to dynamic power. Normally the power across the transistor during switching mode is high. But in the subthreshold design of operation, leakage power is dominating the dynamic power. The amount of current across the transistor of load capacitance is changing the state from High to low & low to high. The power in total (TPd) of the circuit is given by Total Power is evaluated as sum of the static power and dynamic Power. Figure 20. power dissipation in Total is 0.46692 µA.

![Figure 20. Total power (Tpd) dissipation of 0.46692 µw](image)

From Figure 20 clearly states that there is more dynamic power & the amount of static is reduced drastically in the total power of SRAM cell. Because of power reduction techniques are applied, in GDI technique.

2.6. Delay Analysis
Dynamic response is the time taken change the state from 2% to 90% treated as rising Time (tr), and Fall Time (tf) is time taken to fall from 90% to 2%, average rate of rising and fall time (trf) \((tr + tf)/2\) is called edge Rate. Delay is the delay is an average of \((tpHL + tpLH)/2\), Contamination Delay (tcd) is the delay of Min time of the input crossing 50%.

2.6.1 Rise Time (Tr)
Time taken to raise the output signal from 2% to 90% of the max value is treated as rising time period and represented by Tr denoted by Figure 21
2.6.2 Fall Time($T_f$) Analysis

![Figure 22](image). Fall time of 0.015ns

The times to fall the output change the state from 90% to 2% of the max value that represented as fall time and indicated by $t_f$. denoted by Figure 22

3. Results

| Analysis               | SCL    | GDI   |
|------------------------|--------|-------|
| Total power $nw$       | 13.77  | 4.6606|
| Delay $\mu s$         | 0.615  | 0.122 |
| Power delay product    | 8.4685 | 0.5685|

Table 2 represents the analysis and comparison of Source coupled logic design vs Gate diffused Input SRAM design with their performance parameters of Total power in nano watts, Delay micro watts and Power delay product.
Comparison of Power, delay and power delay product is analyzed leakage power is gradually reduced by a 34%, Delay is decreased by 20% and finally power delay product reduced by 7% indicated in Figure 23.

4. Conclusion

Subthreshold GDI SRAM of power(Pd), delay(Td), power delay product(PDP) is analyzed in 32nm and described. Design & analysis of single bit SRAM and GDI SRAM under subthreshold operation with same length of the transistors at 32nm technology. The characteristics, the threshold voltage of the transistor, considering the threshold(0.49v), applying Vss<Vth (0.4). Hence this leads to operates the SRAM under Subthreshold Operation & also changing width of the transistor to 32nm technology. The performance and functionalities are obtained on the basis of static, dynamic power and also rise,fall time. From the parameters mentioned, power & delays can be analyzed. These power and delay values are greatly reduced in GDI SRAM comparing with SRAM. So low power SRAM based GDI model can be used in cardioverter defibrillator of pacemakers as the power hungry of the circuit is less, GDI SRAM can be used as internal circuit in pacemaker.

References

[1] T Vasudeva Reddy, Designing Of Schmitt Trigger-Based Architecture 8T SRAM Of 256 bit cells under 45nm technology for low power applications, 2016 International Conference on Engineering and Technology (ICET), IEEE
[2] T Vasudeva Reddy, Design strategy & analysis of Subthreshold SRAM in power & delay for wearable applications, 2017 2nd International Conference on Communication and Electronics Systems (ICCES),IEEE
[3] T. Vasudeva Reddy, Performance & functionality of novel Subthreshold SRAM’s using low power techniques for SoC designs, 2018 3rd International Conference on Communication and Electronics Systems (ICCES),IEEE
[4] T. Vasudeva Reddy, Design and estimation of power and delay using high Vth nmos under subthreshold logic operation of SRAM onebit model, DOI: 10.1109/SCOPES.2016.7955750
[5] T. Vasudeva Reddy, Analysis & design of robust ultra-low power subthreshold SRAM models, IEEE, 2016 International Conference on Control, Instrumentation, Communication and Computational Technologies (ICCICCT), IEEE,DOI: 10.1109/ICCICCT.2016.7987945
[6] T Vasudeva Reddy, Sub-threshold SRAM bit cell topologies for ultra-low power applications, International Journal of Scientific & Engineering Research, Volume 5, Issue 8, August-2014 957 ISSN 2229-5518.
[7] K. Amalraj et al presented a paper on " Low Voltage Low Power SRAM design based on
Schmitt Trigger technique Nano Scaled Low Power Leakage 10. ST-based SRAM " in 2012 International Conference on Emerging Trends in Electrical Engineering and Energy Management (ICETEEEM), 978-1-4673-4634-4/12, IEEE.

[8] Single-ended Schmitt-trigger-based robust low-power SRAM cell by Sayeed Ahmad, et al., Journal, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Volume 24, Issue 8, Pages 2634-2642, Publisher, IEEE.

[9] Design of Low Power 6T-SRAM Cell and Analysis for High-Speed Application by G. Shivaprakash1, Vol 9 (46), December 2016.