A combinational full adder based on memristors

A A Kulakova and E B Lukyanenko

Southern Federal University, Institute of Nanotechnology, Engineering center for instrumentation, radio- and microelectronics, 347922, Shevchenko street, 2, Taganrog, Rostov region, Russia

E-mail: anastasya.staryh@mail.ru

Abstract. A combinational full adder based on hybrid memristor – CMOS logic is considered. Physical and mathematical models of memristors based on hybrid memristor – CMOS logic are proposed for studying the adder. It is shown that these models can be used for modeling in very large-scale integrated circuits design tools, such as the OrCAD. Unlike physical models, mathematical models of elements do not reflect physical properties, but the parameters of their work correspond to physical models. The work contains textual descriptions of the models. As a result of modeling (computational experiment), flow diagrams of the operation of the adder built on these elements are shown, parameters are given (signal propagation time, power dissipation, number of elements, energy efficiency). The developed models can be used to speed up the process of modeling digital integrated circuits using memristors.

1. Introduction

The use of memristors in adders leads to an improvement in their parameters: speed, occupied area, power dissipation [1]. As a circuit for a complete adder, we choose a circuit made on homogeneous elements 2NAND [2]. The 2NAND circuits use a hybrid memristor-CMOS logic (MeMOS logic), which combines CMOS-transistors and memristors [3, 4]. For memristor elements 2NAND, two models are proposed: physical and mathematical. The creation of models of digital elements based on hybrid MeMOS logic is an urgent task, since memristors are compatible with CMOS technology, have small dimensions in comparison with transistors, are characterized by non-volatility and unlimited information storage time.

For the proposed models, flow diagrams of the adder operation and the following parameters are given: signal propagation time, power dissipation, number of elements, energy efficiency. The purpose of this research is to develop mathematical models of digital memristor elements 2NAND, allowing to accelerate the simulation of digital circuits on memristors.

2. The physical model of digital memristor’s elements 2NAND

A memristor is a metal-dielectric-metal structure in which a thin film of titanium dioxide (TiO2) is usually used as the dielectric [5, 6].

The circuit of the element 2NAND on the hybrid MeMOS logic is given in the article [7]. It is represented by two cascade-connected memristors connected by positive leads.

The physical model, taking into account the features of the functioning of the 2NAND element on the MeMOS logic, is shown in figure 1.
Both memristors are presented in the form of keys S1, S2, the resistances of which change in opposite directions under the influence of voltage X taken from the output of the integrator. The block H1 converts the value and direction of the current through the memristors into voltage. The integrator is formed by the current source of the G1 unit and the capacitor C1. Due to the peculiarities of the function \( f(X) \), it is necessary to limit the voltage on the capacitor C1 within the limits of less than 1 and more than 0, which is achieved by introducing a negative feedback formed by block I.

The logic element NOT is not implemented on only memristors, therefore an inverter on CMOS transistors is used.

**Spice text model of a physical memristor’s element 2NAND:**

```spice
.mod

.SUBCKT 2I_KL a b nOut

Params: D=10n uv=10f P=4 K=1k Ron=5k Roff=500k

S1 a y x 0 S1mod
S2 b f x 0 S2mod

.Model S1mod VSWITCH (Von=0 Voff=1 Ron=5k Roff=500k)
.Model S2mod VSWITCH (Von=1 Voff=0 Ron=5k Roff=500k)

V1 y f 0v

G1 0 x value=\{[I(V1)]*uv*[(Roff/D^2)*f(v(x),p) - (v(x) - 0.99)*K*stp(v(x) - 0.99) - (v(x) - 10m)*K*stp(10m-v(x))]\}
Raux x 0 1 g
C1 x 0 0.05n IC=0.1

.func f(x,p)=\{1-(2*x-1)^p\}
R1 y d 20k
C2 d 0 1f
E1 nOut 0 value=\{1.8-V(d)\}
.ends
```

3. **The mathematical model of a digital memristor’s element 2NAND**

The authors propose a mathematical model reflecting the physical properties of the memristor (figure 2).

In this model, memristors are modeled with keys S1, S2. The diff block defines the ratio of the input signals: \( a=b \), \( a<b \) and \( a>b \). When \( a=b \), the signal at the output of the diff block is equal to zero and the model must remember the previous state of the 2NAND element. Store occurs using a trigger formed by the Glimit block and resistors R1, R2, which form a positive feedback. The trigger controls the state of the keys S1, S2.

The time delay is formed by the input capacitance of the inverter and the resistance of the switch.
Such a model is much simpler than a physical model, due to which the simulation time of a full adder is reduced by tens of times.

![Figure 2](image_url)  
Figure 2. The mathematical model of a digital memristor’s element 2NAND.

Spice text model of a mathematical memristor’s element 2NAND:
```
.mod
.subckt 2I_math a b nOut
Params: R1=10k R2=10k
S1 a y x 0 S1mod
S2 b y x 0 S2mod
.Model S1mod VSWITCH(Von=-1 Voff=1 Ron=10k Roff=1meg)
.Model S2mod VSWITCH(Von=1 Voff=-1 Ron=10k Roff=1meg)
E1 1 0 value={5*(V(a)-V(b))}
E2 2 0 value={(V(X)-V(1))*R1/(R1+R2)+V(1)}
E3 3 0 value={10*v(2)}
EX X 0 value={(stp(V(3))-0.5)*2}
.ends
```

4. Simulation results
The following parameters of the S1 key are selected: key closing voltage Von=-1 V; key opening voltage Voff=1 V; closed key resistance Ron = 10 kΩ; open key resistance Roff=1000 kΩ. S2 key has Von and Voff inverted. Key resistances correspond to resistances of memristors in low-resistance or high-resistance states.

The analysis of the adder’s parameters is shown in table 1.

| Type of adder | Propagation time, (ps) | Power dissipation, (uW) | Amount of elements, (pcs) | Energy efficiency, (pJ·pcs) |
|---------------|------------------------|-------------------------|---------------------------|-----------------------------|
| On standard elements | 390 | 28 | 36 | 0.39 |
| On memristors | 120 | 20 | 36 | 0.086 |

Figure 3 shows flow diagrams demonstrating the correct operation of the developed mathematical model of the digital memristor’s element 2NAND.
Figure 3. Results of modeling the developed mathematical model of the digital memristor’s element 2NAND.

In figure 4 shows flow diagrams showing the correct operation of the developed adder.

Figure 4. Results of modeling a full adder on memristors.

5. Conclusion
Physical and mathematical models of the 2NAND memristor’s element have been developed. Due to its simplicity, the mathematical model can significantly increase the speed of modeling memristor’s circuits. The study of the adder parameters showed that the energy efficiency of the adder based on memristors is 5 times higher than the energy efficiency of the adder on standard elements.

References
[1] Tejinder S 2015 Hybrid memristor-CMOS (MeMOS) based logic gates and adder circuits CoRR 1-11
[2] Starykh A A 2015 The method for the synthesis of functional blocks of combinational circuits with the use minterms and maxterms Electronic engineering Series 2 Semiconductor devices 2-3(236-7) 63-9
[3] Cho K, Lee S and Eshraghian K 2015 Memristor-CMOS logic and digital computational components Microelectronics Journal 3(46) 214-20
[4] Konoplev B G, Kovalev A V, Kalskov V V, Lukyanenko E B, Kalskov A V and Komarov I A 2012 Schematic model of memristor for Cadence system Fundamental research 11(2) 412-5
[5] Strukov D B, Snider G S, Stewart D R and Williams R S 2008 The missing memristor found Nature 453 80-3
[6] Biolek Z, Biolek D and Biolkova V 2009 SPICE model of memristor with nonlinear dopant drift Radioengineering 18(2) 210-4
[7] Kulakova A A and Lukyanenko E B 2020 Memristor functional units digital circuitry Proc. Univ. Electronics 25(4) 330-8