The Quantum Socket: Three-Dimensional Wiring for Extensible Quantum Computing

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Quantum computing architectures are on the verge of scalability, a key requirement for the implementation of a universal quantum computer. The next stage in this quest is the realization of quantum error correction codes, which will mitigate the impact of fault quantum information on a quantum computer. Architectures with ten or more quantum bits (qubits) have been realized using trapped ions and superconducting circuits. While these implementations are potentially scalable, true scalability will require systems engineering to combine quantum and classical hardware. One technology demanding imminent efforts is the realization of a suitable wiring method for the control and measurement of a large number of qubits. In this work, we introduce an interconnect solution for solid-state qubits: The quantum socket. The quantum socket fully exploits the third dimension to connect classical electronics to qubits with higher density and better performance than two-dimensional methods based on wire bonding. The quantum socket is based on spring-mounted micro wires – the three-dimensional wires – that push directly on a micro-fabricated chip, making electrical contact. A small wire cross section (~1 mm), nearly non-magnetic components, and functionality at low temperatures make the quantum socket ideal to operate solid-state qubits. The wires have a coaxial geometry and operate over a frequency range from DC to 8 GHz, with a contact resistance of ~150 mΩ, an impedance mismatch of ~10Ω, and minimal crosstalk. As a proof of principle, we fabricated and used a quantum socket to measure superconducting resonators at a temperature of ~10 mK. Quantum error correction codes such as the surface code will largely benefit from the quantum socket, which will make it possible to address qubits located on a two-dimensional lattice. The present implementation of the socket can be readily extended to accommodate a quantum processor with a 10 × 10 qubit lattice, which would allow the realization of a simple quantum memory.

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I. INTRODUCTION

The work to be presented in this article lies at the boundary between physics and electrical engineering and aims at the experimental implementation of practical hardware technology for quantum computation [1]. At this point in time, one of the main objectives in the quantum computing community is to build and prototype tools for scalable architectures that may lead to the realization of a universal quantum computer [2]. In this project, we undertake the task of implementing an extensible wiring method for the operation of a quantum processor based on solid-state devices, e.g., superconducting qubits [3–5]. Possible experimental solutions based on wafer bonding techniques [6–9] or coaxial through-silicon vias [10] as well as theoretical proposals [11] have recently addressed the wiring issue, highlighting it as a priority for quantum computing.

Building a universal quantum computer [12–17] will make it possible to execute quantum algorithms [18], which would have profound implications on scientific research and society. For a quantum computer to be competitive with the most advanced classical computer, it is widely believed that the qubit operations will require error rates on the order of 10^{-15} or less. Achieving such error rates is only possible by means of quantum error correction (QEC) algorithms [13,14,19], which allow for
the implementation of fault tolerant operations between logical qubits. A logical qubit is realized as an ensemble of a large number of physical qubits (on the order 10^9 or larger), where each physical qubit behaves as an effective quantum-mechanical two-level system.

Among various QEC algorithms, the most practical at present is the surface code algorithm [3, 20]. The surface code requires only nearest-neighbor interactions between physical qubits on a two-dimensional lattice, one- and two-qubit physical gates, and qubit measurement with error rates below approximately 10^{-2} [3]. Both fast gates and measurements are indispensable to run quantum algorithms efficiently; execution times on the order of tens of nanoseconds for physical operations (e.g., a gate or measurement operation) are highly desirable and represent the state-of-the-art in qubit technology today. Under these conditions, to factorize a 2000-bit number using Shor’s algorithm [22] requires more than 220 million physical qubits (i.e., approximately 4000 logical qubits storing meaningful data; note that these logical qubits occupy less than 10% of the quantum computer, the remainder of which is used to generate special states facilitating computation), with an overall computation time of ~1 d [3].

Quantum computing architectures can be implemented using photons [23, 24], trapped ions [25], spins in molecules [26] and quantum dots [27–31], spins in silicon [30, 32], and superconducting quantum circuits [3–5]. The last are leading the way for the realization of the first surface code logical qubit, which is one of the priorities in the quantum computing community at present. Recently, several experiments based on superconducting quantum circuits have demonstrated the principles underlying the surface code. These works have shown a complete set of physical gates with fidelities beyond the surface code threshold [33], the parity measurements necessary to detect quantum errors [34, 35], and have realized a classical version of the surface code on a one-dimensional array of nine physical qubits [36]. Notably, the planar design inherent to the superconducting qubit platform will make it possible to implement large two-dimensional qubit arrays, as required by the surface code.

Despite all these accomplishments, a truly scalable qubit architecture has yet to be demonstrated. Wiring is one of the most basic unsolved scalability issues common to most solid-state qubit implementations, where qubit arrays are fabricated on a chip. The conventional wiring method based on wire bonding suffers from fundamental scaling limitations as well as mechanical and electrical restrictions. Wire bonding relies on bonding pads located at the edges of the chip. Given a two-dimensional lattice of \( N \times N \) physical qubits on a square chip, the number of wire bonds that can be placed scales approximately as \( 4N \) (\( N \) bonds for each chip side). Wire bonding will thus never be able to reach the required \( N^2 \) law according to which physical qubits scale on a two-dimensional lattice. Furthermore, for large \( N \), wire bonding precludes the possibility of accessing physical qubits in the center region of the chip, which is unacceptable for a physical implementation of the surface code. In the case of superconducting qubits, for example, qubit control and measurement are typically realized by means of microwave pulses or, in general, pulses requiring large frequency bandwidths. By their nature, these pulses cannot be reliably transmitted through long sections of quasi-filiform wire bonds. In fact, stray capacitances and inductances associated with wire bonds as well as the self-inductance of the bond itself limit the available frequency bandwidth, thus compromising the integrity of the control and measurement signals [37]. Additionally, the placement of wire bonds is prone to errors and inconsistency in spacing [38].

In this work, we set out to solve the wiring bottleneck common to almost all solid-state qubit implementations. Our solution is based on suitably packaged three-dimensional micro wires that can reach any area on a given chip from above. We define this wiring system as the quantum socket. The wires are coaxial structures consisting of a spring-loaded inner and outer conductor with diameters of 380 \( \mu m \) and 1290 \( \mu m \), respectively, at the smallest point and with a maximum outer diameter of 2.5 mm. The movable section of the wire is characterized by a maximum stroke of approximately 2.5 mm, allowing for a wide range of on-chip mechanical compression. All wire components are non magnetic, thereby minimizing any interference with the qubits. The three-dimensional wires work both at room temperature and at cryogenic temperatures as low as \( \sim 10 \) mK. The wires’ test-retest reliability is excellent, with marginal variability over hundreds of measurements. Their electrical performance is good from DC to at least 8 GHz, with a contact resistance smaller than 150 m\( \Omega \) and an instantaneous impedance mismatch of approximately 10\( \Omega \). Notably, the coaxial design of the wires strongly reduces unwanted crosstalk, which we measured to be at most \( \sim -45 \) dB for a realistic quantum computing application.

In a recent work [4], seven sequential stages necessary to the development of a quantum computer were introduced. At this time, the next stage to be reached is the implementation of a single logical qubit characterized by an error rate that is at least one order of magnitude lower than that of the underlying physical qubits. In order to achieve this task, a two-dimensional lattice of \( 10 \times 10 \) physical qubits with an error rate of at least \( 10^{-3} \) is required [3]. In the case of superconducting qubits such a lattice can be realized on a chip area of 72 mm \( \times \) 72 mm (the largest square that can be diced from a standard 4 inch wafer) and wired by means of a quantum socket. It is feasible to further miniaturize the three-dimensional wires so as to achieve a wire density of \( 2.5 \times 10^5 \) m\(^{-2} \). This would allow the manipulation of \( \sim 10^5 \) physical qubits and, possibly, the realization of simple fault tolerant operations [4]. Furthermore, the wires could serve as interconnect between a quantum hardware layer fabricated on one chip and a classical hardware layer realized on a separate chip, just
The implications of our cryogenic micro-wiring method go beyond quantum computing applications, providing a useful addition to the packaging industry for research applications at low temperatures. With this work, we demonstrate that the laborious and error-prone wire bonding technique can be substituted by the simple procedure of inserting the chip into a sample box equipped with three-dimensional wires. Our concept will expedite sample packaging and, thus, experiment turn over even for research not directly related to quantum information.

This research article is organized as follows. In Sec. II we introduce the quantum socket design, with special focus on the three-dimensional wires (cf. Subsec. II A), the microwave package (cf. Subsec. II B), and the package holder (cf. Subsec. II C). In the same section, we show microwave simulations of a bare three-dimensional wire, of a wire connected to a pad on a chip, and of an entire microwave package (cf. Subsec. II D). In Sec. III we show the physical implementation of all components described in Sec. II. In this section, we describe the materials used in the quantum socket and show how the socket is assembled. In particular, we describe the magnetic and thermal properties of the quantum socket components (cf. Subsec. III A and Subsec. III B respectively) as well as the spring characterization (cf. Subsec. III C). Moreover, we discuss in detail the quantum socket alignment procedure (cf. Subsec. III D). In Sec. IV we present a variety of measurements used to characterize the quantum socket operation. We first focus on a four-port measurement used to estimate a wire contact resistance (cf. Subsec. IV A). We then show a series of microwave measurements on samples with different geometries and materials, both at room temperature and at 77 K. These measurements comprise two-port scattering parameter (S-parameter) experiments (cf. Subsec. IV B), time-domain reflectometry (TDR) analysis (cf. Subsec. IV C), and signal crosstalk tests (cf. Subsec. IV D). In Sec. V we show an application of the quantum socket relevant to superconducting quantum computing, where the socket is used to measure aluminum (Al) superconducting resonators at a temperature of approximately 10 mK. Finally, in Sec. VI we envision an extensible quantum computing architecture where a quantum socket is used to connect to a 10 × 10 lattice of superconducting qubits and comment on the possibility to use the socket in conjunction with RSFQ electronics.

II. THE QUANTUM SOCKET DESIGN

The development of the quantum socket required a stage of meticulous micro-mechanical and microwave design and simulations. It was determined that a spring-loaded interconnect – the three-dimensional wire – was the optimal method to electrically access devices lithographically fabricated on a chip and operated in a cryogenic environment. An on-chip contact pad geometrically and electrically matched to the bottom interface of the wire can be placed easily at any desired location on the chip as part of the fabrication process, thus making it possible to reach any point on a two-dimensional lattice of qubits. The contact pad is realized as a thin metallic film deposited on a dielectric substrate; arbitrary film thicknesses can be deposited. The rest of the sample is fabricated on chip following a similar process. The coaxial design of the wire provides a wide operating frequency bandwidth, while the springs allow for mechanical stress relief during the cooling process. The three-dimensional wires used in this work take advantage of the knowledge in the existing field of microwave circuit testing [11]. However, reducing the wire dimensions to a few hundred micrometers and using it to connect to quantum-mechanical micro-fabricated circuits at low temperatures resulted in a significant extension of existing implementations and applications.

In this section, we will describe the design of the three-dimensional wires, of the microwave package used to house the wires, and of the microwave package holder. Additionally, we will show a set of microwave simulations of the main components of the quantum socket.

A. Three-dimensional wires

Figure 1 shows the design of the quantum socket components. Figure 1 (a) displays a model of a three-dimensional wire. The coaxial design of the wire is visible from the image, which features a wire 30.5 mm long when uncompressed. The wire is characterized by an inner cylindrical pin of diameter 380 µm and an outer cylindrical body (the electrical ground) of diameter 1290 µm at its narrowest region; this region is the bottommost section of the wire and, hereafter, will be referred to as the wire contact head (cf. the inset of Fig. 1 (a), as well as the dashed box on the left of Fig. 1 (a)). The contact head terminates at the wire bottom interface; this interface is designed to mate with a pad on a chip (cf. Fig. 1 (b) and (c)). The outer body includes a rectangular aperture, the tunnel, to prevent shorting the inner conductor of an on-chip coplanar waveguide (CPW) transmission line [12,13]; the transmission line can connect the pad with any other structure on the chip. Two different tunnel dimensions were designed, with the largest one reducing potential alignment errors. These errors can result in undesired short-circuit connections to ground. The tunnel height was 300 µm in both cases, with a width of 500 µm or 650 µm. The internal spring mechanisms of the wire allow the contact head to be compressed; the maximum stroke was designed to be 2.5 mm, corresponding to a working stroke of 2.0 mm.

The outer body of the three-dimensional wire is an M2.5 male thread used to fix the wire to the lid of the
FIG. 1. Computer-aided designs of the three-dimensional wire, microwave package, and package holder. (a) A wire of length $\ell = 30.5\,\text{mm}$ along with a detail of the contact head (inset). (b) Assembled microwave package including six three-dimensional wires, washer, washer springs, and chip (shown in green). The arrow indicates the screw-in micro connector on the back end of the wire. Forward hatching indicates the washer cutaway, whereas backward hatching indicates both lid and sample holder cutaways. (c) Cross section of the microwave package showing the height of the upper cavity, which coincides with the minimum compression distance $\ell_c$ of the three-dimensional wires (cf. Appendix A). (d) Microwave package mounted to the package holder, connected, in turn, to the mounting plate of a DR with SMP connectors.

The thread is split into two segments of length 3.75 mm and 11.75 mm that are separated by a constriction with outer diameter 1.90 mm. The constriction is necessary to assemble and maintain in place the inner components of the three-dimensional wire. A laser-printed marker is engraved into the top of the outer body. The marker is aligned with the center of the tunnel, making it possible to mate the wire bottom interface with a pad on the underlying chip with a high degree of angular precision. The grooves partially visible on the bottom of Fig. 1(a) are used to torque the wire into a 2.5 mm thread in the package’s lid.
Figure 2 (a) shows a lateral two-dimensional cut view of the three-dimensional wire. Two of the main wire components are the inner and outer barrel, which compose part of the inner and outer conductor. The inner conductor barrel is a hollow cylinder with outer and inner diameters of 380 µm and 290 µm (indicated as part iv in Fig. 2(a)), respectively. This barrel encapsulates the inner conductor spring. The outer conductor barrel is a hollow cylinder as well, in this case with an inner diameter of 870 µm (parts ii and vii). Three polytetrafluoroethylene (PTFE) disks serve as spacers between the inner and outer conductor; such disks contribute marginally to the wire dielectric volume, the majority of which is air or vacuum. The outer spring is housed within the outer barrel towards its back end, just before the last PTFE disk on the right-hand side of the wire. The back end of the wire is a region comprising a female thread on the outer conductor and an inner conductor barrel (cf. dashed box on the right-hand side of Fig. 2(a)).

The inner conductor tip is characterized by a conical geometry with an opening angle of 30°. Such a sharp design was chosen to ensure that the tip would pierce through any possible oxide layer forming on the contact pad metallic surface, thus allowing for a good electrical contact.

Figure 2 (c) shows the design of a typical on-chip pad used to make contact with the bottom interface of a three-dimensional wire. The pad comprises an inner and outer conductor, with the outer conductor being grounded. The pad in the figure was designed for a silver (Ag) film of thickness 3 µm. A variety of similar pads were designed for gold (Au) and Al films with thickness ranging between approximately 100 nm and 200 nm. The pad inner conductor is a circle with diameter 320 µm that narrows to a linear trace (i.e., the inner conductor of a CPW transmission line) by means of a raised-cosine taper. The raised cosine makes it possible to maximize the pad area, while minimizing impedance mismatch. As designed, the wire and pad allow for lateral and rotational misalignment of ±140 µm and ±28°, respectively. The substrate underneath the pad is assumed to be silicon (Si) with a relative permittivity εs ≃ 11. The dielectric gap between the inner and outer conductor is 180 µm in the circular region of the pad; the outer edge of the dielectric gap then follows a similar raised-cosine taper as the inner conductor. The pad characteristic impedance is designed to be Zc = 50 Ω.
B. Microwave package

The microwave package comprises three main parts: The lid; the sample holder; the grounding washer. The package is a parallelepiped with a height of 30 mm and with a square base of side length 50 mm. The chip is housed inside the sample holder. All these components mate as shown in Fig. 2(b) and (c).

In order to connect a three-dimensional wire to a device on a chip, the wire is screwed into an M2.5 female thread that is tapped into the lid of the microwave package, as depicted in Fig. 1(b). The pressure applied by the wire to the chip is set by the depth of the wire in the package. The wire stroke, thread pitch, and alignment constraints impose discrete pressure settings (cf. Appendix A). In the present implementation of the quantum socket, the lid is designed to hold a set of six three-dimensional wires, which are arranged in two parallel rows. In each row, the wires are spaced by 5.75 mm from center to center, with the two rows being separated by a distance of 11.5 mm.

A square chip of lateral dimensions 15 mm × 15 mm is mounted in the sample holder in a similar fashion as in Ref. [44]. The outer edges of the chip rest on four protruding lips, which are 1 mm wide. Hereafter, those lips will be referred to as the chip recess. For design purposes, a chip thickness of 550 µm is assumed. Correspondingly, the chip recess is designed so that the top of the chip is 100 µm above the adjacent surface of the chip holder, i.e., the depth of the recess is 450 µm (cf. Fig. 1(c)). The outer edges of the chip are pushed on by a spring-loaded grounding washer. The 100 µm chip protrusion ensures a good electrical connection between chip and washer, as shown in Fig. 2(c).

The grounding washer was designed to substitute the large number of lateral bonding wires that would otherwise be required to provide a good ground to the chip (as shown, for example, in Fig. 6 of Ref. [44]). The washer springs are visible in Fig. 1(b), which also shows a cut view of the washer. The washer itself is electrically grounded by means of the springs as well as through galvanic connection to the surface of the lid. The four feet of the washer, which can be seen in the cut view of Fig. 1(b), can be designed to be shorter or longer. This makes it possible to choose different pressure settings for the washer.

After assembling the package, there exist two electrical cavities (cf. Fig. 1(d)): One above the chip, formed by the lid, washer, and metallic surface of the sample (upper cavity), and one below the chip, formed by the sample holder and metallic surface of the sample (lower cavity). The hollow cavity above the sample surface has dimensions 14 mm × 14 mm × 3.05 mm. The dimensions of the cavity below the sample are 13 mm × 13 mm × 2 mm. The lower cavity helps mitigate any parasitic capacitance between the chip and the box (ground). Additionally, it serves to lower the effective permittivity, increasing the frequency of the substrate modes (cf. Subsec. II D).

A pillar of square cross section with side length of 1 mm is placed right below the chip at its center; the pillar touches the bottom of the chip, thus providing mechanical support [45]. The impact of such a pillar on the microwave performance of the package will be described in Subsec. II D. A channel with a cross-sectional area of 800 µm × 800 µm connects the inner cavities of the package to the outside, thus making it possible to evacuate the inner compartments of the package. This channel meanders to prevent external electromagnetic radiation from interfering with the sample.

C. Package holder

The three-dimensional wires, which are screwed into the microwave package, must be connected to the qubit control and measurement electronics. In addition, for cryogenic applications, the package must be thermally anchored to a refrigeration system in order to be cooled to the desired temperature. Figure 2(d) shows the mechanical module we designed to perform both electrical and thermal connections. In this design, each three-dimensional wire is connected to a screw-in micro connector, which is indicated by an arrow in Fig. 1(b) and is shown in detail in Fig. 2(d). One end of the micro connector comprises a male thread and an inner conductor pin that mate with the back end of the three-dimensional wire. The other end of the micro connector is soldered to a coaxial cable. The micro connector is necessary because the high temperatures generated by soldering a coaxial cable directly to the wire back end would damage some of the inner wire components [40].

The end of each coaxial cable opposite to the three-dimensional wire is soldered to a sub-miniature push-on (SMP) connector. The SMP connectors are bolted to a horizontal plate attached to the microwave package by means of two vertical fixtures, as shown in Fig. 2(d). The vertical fixtures and the horizontal plate constitute the package holder. The package holder and microwave package form an independent assembly. A horizontal mounting plate, designed to interface with the package holder, houses a set of matching SMP connectors. The mounting plate is mechanically and, thus, thermally anchored to the mixing chamber (MC) stage of a dilution refrigerator (DR). This design significantly simplifies the typical mounting procedure of a sample box to a cryostat, since the package holder and microwave package can be conveniently assembled remotely from the DR and attached to it just prior to commencing an experiment.

D. Microwave simulations

The three-dimensional wires, the 90° transition between the wire and the on-chip pad as well as the inner cavities of the fully-assembled microwave package were extensively simulated by means of the high frequency three-dimensional full-wave electromagnetic field simu-
Figure 3. Numerical simulations of the electric field distribution. (a) Field for a three-dimensional wire at 6 GHz. (b) Field in proximity of the 90° transition region at 6 GHz. (c) Field for the first box mode at 6.3 GHz. Color bar scales are indicated in their respective panels. The x, y, and z directions of a Cartesian coordinate system are also indicated. In (b), the cross section of the transition region is shown. Note the large volume occupied by the electric field beneath the contact pad. In (c), an offset cross section of the first box mode is shown. The field confinement due to the pillar is clearly visible. Additionally, the simulation shows a slight field confinement in the region surrounding the chip recess. Time-domain animations of the simulated electric field can be found in the Supplemental Material at [http://www.Supplemental-Material-Bejanin](http://www.Supplemental-Material-Bejanin).

Simulation software (HFSS) by Ansys, Inc. The results for the electromagnetic field distribution at a frequency of approximately 6 GHz, which is a typical operation frequency for superconducting qubits, are shown in Fig. 3. Figure 3 (a) shows the field behavior for a bare three-dimensional wire. The field distribution resembles that of a coaxial transmission line except for noticeable perturbations at the dielectric PTFE spacers. Figure 3 (b) shows the 90° transition region. This is a critical region for signal integrity since abrupt changes in physical geometry cause electrical reflections [41, 47]. In order to minimize such reflections, an impedance-matched pad was designed. However, this leads to a large electromagnetic volume in proximity of the pad, as seen in Fig. 3 (b), possibly resulting in parasitic capacitance and crosstalk.

In addition to considering the wire and the transition region, the electrical behavior of the inner cavities of the package was studied analytically and simulated numerically. As described in Subsec. II B, the metallic surface of the chip effectively divides the cavity of the sample holder into two regions: A vacuum cavity above the metal surface and a cavity partially filled with dielectric below the metal surface. The latter is of greatest concern as the dielectric acts as a perturbation to the cavity vacuum [48], thus lowering the box modes. For a simple rectangular cavity, the frequency $f$ of the first mode due to this perturbation can be found as [43],

$$f = f_0 - f_0 \left( \frac{\epsilon_r - 1}{2b} \right),$$

where $f_0$ is the frequency of the unperturbed mode, $\epsilon_r$ the relative permittivity of the dielectric, $d_s$ the substrate thickness.

| TABLE I. Simulation results for the first three box modes of the lower cavity inside the assembled microwave package shown in Fig. 1 (b). The dielectric used for these simulations was Si at room temperature with relative permittivity $\epsilon_r = 11.68$. “Vacuum” indicates that no Si is present in the simulation. “with pillar” indicates that the 1.0 mm × 1.0 mm × 2.0 mm support pillar is present. TE$_{xyz}$ indicates the number of half-wavelengths spanned by the electric field in the x, y, and z directions, respectively (cf. Fig 3 (c)). Note that the frequency of the first mode of the upper cavity is $\sim 17.2$ GHz. |
|-----------------|-----------------|-----------------|
|                | TE$_{110}$      | TE$_{120}$      | TE$_{210}$      |
| Vacuum         | 15.7            | 24.2            | 24.2            |
| Vacuum with pillar | 13.1          | 23.6            | 23.6            |
| Si             | 13.5            | 16.8            | 16.8            |
| Si with pillar  | 6.3             | 16.2            | 16.9            |
thickness, and \( b \) the cavity height. From Eq. (1), we estimated this box mode to be 12.8 GHz. However, considering the presence of the pillar, the three-dimensional wires, etc., we had to use numerical simulations to obtain a more accurate estimate of the lowest box modes. The results for the first three modes are reported in Table IV. Discounting the pillar, the analytical and simulated values are in good agreement with each other. The addition of the support pillar significantly lowers the frequency of the modes. In fact, it increases the relative filling factor of the cavity by confining more of the electromagnetic field to the dielectric than to vacuum. Given the dimensions of this design, the pillar leads to a first mode which could interfere with typical qubit frequencies. In spite of this, the pillar was included in the final design in order provide a degree of mechanical support. Note that the pillar can alternatively be realized as a dielectric material, e.g., PTFE; a dielectric pillar would no longer cause field confinement between the top surface of the pillar and the metallic surface of the chip.

III. THE QUANTUM SOCKET IMPLEMENTATION

The physical implementation of the main components of the quantum socket is displayed in Fig. 3. In particular, Fig. 3 (a) shows a macro photograph of a three-dimensional wire. The inset shows a scanning electron microscope (SEM) image of the wire contact head, featuring the 500 \( \mu \)m version of the tunnel. This wire was cycled approximately ten times; as a consequence, the center conductor of the contact head, which had a conical, sharp shape originally, flattened at the top. The metallic components of the wire were made from bronze and brass (cf. Subsec. III A), and all springs from hardened beryllium copper (BeCu). Except for the springs, all components were gold plated without any nickel (Ni) adhesion underlayer. The estimated mean number of cycles before failure for these wires is approximately 100000.

Figure 3 (b) displays the entire microwave package in the process of locking the package lid and sample holder together, with a chip and grounding washer already installed. As shown in the figure, two rows of three-dimensional wires, for a total number of six wires, are screwed into the lid with pressure settings as described in Appendix A; each wire is associated with one on-chip CPW pad. The four springs that mate with the grounding washer feet are embedded in corresponding recesses in the lid; the springs are glued in these recesses by way of Vibra-Tite 12110 (from ND Industries, Inc.), a medium-strength thread locker that works well at low temperatures. All package components were made from high-purity Al.

Figure 3 (c) shows a picture of the assembled microwave package attached to the package holder; the entire structure is attached to the MC stage of a DR. All parts of the assembly were made from high thermal conductivity C10100 oxygen-free electrolytic (OFE) copper alloy [49]. The parts were polished to a mirror finish before being gold plated [50]. The coaxial cables between the screw-in micro connectors and the SMP connectors are from the EZ Form Cable Corporation, model EZ 47-CU-TP (EZ 47). The SMP connectors, also from EZ Form, are models SMP bulkhead jack for 0.084 inch coaxial cables (SMP 047; installed in the package holder horizontal plate) and SMP bulkhead plug with limited detent for 0.086 inch cables (SMP 086; installed in the mounting plate attached to the MC stage of the DR). All SMP connectors were custom-made non-magnetic connectors.

In the remainder of this section, we will discuss the magnetic and thermal properties of the materials used to implement the quantum socket as well as the spring characterization and the alignment procedure.

A. Magnetic properties

An important stage in the physical implementation of the quantum socket was the choice of materials to be used for the three-dimensional wires, the microwave package, and the package holder. In fact, it has been shown that non-magnetic components in proximities of superconducting qubits are critical to preserve long qubit coherence [1, 2, 52, 53].

The three-dimensional wires are the closest devices to the qubits. For this reason, all their components should be made using non-magnetic materials. Due to machining constraints, however, alloys containing ferromagnetic impurities (iron (Fe), cobalt (Co), and Ni) had to be used. For the outer conductor components we used brass, which is easy to thread; the chosen grade was ISO CuZn21Si3P (EN CW724R) [55]. For the inner conductor components, brass CW724R did not meet the machining requirements. Consequently, we decided to use copper alloy (phosphor bronze) grade DIN 2.1030 - CuSn8 (EN CW453K) [56]. The chemical composition for these two materials is reported in Table 1V of Appendix B. The dielectric spacers were made from PTFE and the rest of the components from hardened BeCu; both materials are non-magnetic. The weight percentage of ferromagnetic materials is non-negligible for both CW453K and CW724R. Thus, we performed a series of tests using a zero Gauss chamber (ZGC) in order to ensure both materials were sufficiently non-magnetic. The results are given in Appendix B and show that the magnetic impurities should be small enough not to disturb the operation of superconducting quantum devices.

The microwave package and grounding washer were made from high-purity Al alloy 5N5 (99.9999% purity) provided by Laurand Associates, Inc. The very low level of impurities in this alloy assures minimal stray magnetic fields generated by the package itself, as confirmed by the magnetic tests discussed in Appendix B.
B. Thermal properties

The thermal conductance of the three-dimensional wires is a critical parameter to be analyzed for the interconnection with devices at cryogenic temperatures. Low thermal conductivity would result in poor cooling of the devices, which, in the case of qubits, may lead to an incoherent thermal mixture of the qubit ground state $|g\rangle$ and excited state $|e\rangle$ [57]. Even a slightly mixed state would significantly deteriorate the fidelity of the operations required for QEC [58]. It has been estimated that some of the qubits in the experiment of Ref. [36], which relies solely on Al wire bonds as a means of thermalization, were characterized by an excited state population $P_e \simeq 0.04$. Among other possible factors, it is believed that this population was due to the poor thermal conductance of the Al wire bonds. In fact, these bonds become superconductive at the desired qubit operation temperature of $\sim 10\, \text{mK}$, preventing the qubits from thermalizing and, thus, from being initialized in $|g\rangle$ with high fidelity.

In order to compare the thermal performance of an Al wire bond with that of a three-dimensional wire, we estimated the heat transfer rate per kelvin of a wire, $\Pi_t$, using a simplified coaxial geometry. At a temperature of $25\, \text{mK}$, we calculated $\Pi_t \simeq 6 \times 10^{-7}\, \text{W K}^{-1}$. At the same temperature, the heat transfer rate per kelvin of a typical Al wire bound was estimated to be $\Pi_b \simeq...
$4 \times 10^{-12}\text{W K}^{-1}$ (cf. Appendix C for more details). A very large number of Al wire bonds would thus be required to obtain a thermal performance comparable to that of a single three-dimensional wire.

C. Spring characterization

Another critical step in the physical implementation of the quantum socket was to select springs that work at cryogenic temperatures. In fact, the force that a wire applies to a chip depends on these springs. This force, in turn, determines the wire-chip contact resistance, which impacts the socket’s DC and microwave performance. Among various options, we chose custom springs made from hardened BeCu.

To characterize the springs, their compression was assessed at room temperature, in liquid nitrogen (i.e., at a temperature $T \approx 77\text{K}$), and in liquid helium ($T \approx 4.2\text{K}$). Note that a spring working at 4.2K is expected to perform similarly at a temperature of 10 mK. A summary of the thermo-mechanical tests is reported in Appendix D. The main conclusion of the tests is that the springs do not break (even after numerous temperature cycles) and have similar spring constants at all measured temperatures.

D. Alignment

In order to implement a quantum socket with excellent interconnectivity properties, it was imperative to minimize machining errors and mitigate the effects of any residual errors. These errors are mainly due to: Dicing tolerances; tapping tolerances of the M2.5-threaded holes of the lid; tolerances of the mating parts for the inner cavities of the lid and sample holder; tolerances of the chip recess. These errors can cause both lateral and rotational misalignment and become likely worse when cooling the quantum socket to low temperatures. More details on alignment errors can be found in Appendix E.

The procedure to obtain an ideal and repeatable alignment comprises three main steps: Optimization of the contact pad and tunnel geometry; accurate and precise chip dicing; accurate and precise package machining. For the quantum socket described in this work, the optimal tunnel width was found to be 650 µm. This maintained reasonable impedance matching, while allowing greater CPW contact pad and tapering dimensions. The contact pad width $W_p$ and taper length $T_p$ were chosen to be $W_p = 320\mu \text{m}$ and $T_p = 360\mu \text{m}$. These are the maximum dimensions allowable that accommodate the geometry of the wire bottom interface for a nominal lateral and rotational misalignment of $\pm 140\mu \text{m}$ and $\pm 28^\circ$, respectively. In order to select the given pad dimensions, we had to resort to a 50 $\Omega$ matched raised-cosine tapering.

The majority of the chips used in the experiments presented here was diced with a dicing saw from the DISCO Corporation, model DAD3240. To obtain a desired die length, both the precision of the saw stage movement and the blade’s kerf had to be considered. For the DAD3240 saw, the former is $\approx 4\mu \text{m}$, whereas the latter changes with usage and materials. For the highest accuracy cut, we measured the kerf on the same type of wafer just prior to cutting the actual die. In order to achieve maximum benefit from the saw, rotational and lateral alignment dicing markers were incorporated on the wafer. Such a meticulous chip dicing procedure is only effective in conjunction with a correspondingly high level of machining accuracy and precision. We used standard computer numerical control (CNC) machining with a tolerance of...
1 thou (25.4 µm), although electrical discharge machining can be pursued if more stringent tolerances are required.

Following the aforementioned procedures we were able to achieve the desired wire-pad matching accuracy and precision, which resulted in a test-retest reliability (repeatability) of 100% over 94 instances. These figures of merit were tested in two steps: First, by micro imaging several pads that were mated to a three-dimensional wire (cf. III D 1); second, by means of DC resistance tests (cf. III D 2).

1. On-chip pad micro imaging

Micro imaging was performed on a variety of different samples, four of which are exemplified in Fig. 5. The figure shows a set of micro images for Ag and Al pads (details regarding the fabrication of these samples are available in Appendix F). Figure 5 (a) and (b) show two Ag pads that were mated with the three-dimensional wires at room temperature. Panel (a) shows a mating instance where the wire bottom interface perfectly matched the on chip pad. Panel (b) shows two mating instances that, even though not perfectly matched, remained within the designed tolerances. Notably, simulations of imperfect mating instances revealed that an off-centered wire does not significantly affect the microwave performance of the quantum socket. Finally, panels (c) and (d) display two Al pads which were both mated with a wire one time. While the pad in (c) was operated only at room temperature, the pad in (d) was part of an assembly that was cooled to ∼10 mK for approximately three months. The image was taken after the assembly was cycled back to room temperature and shows dragging of the wire by a few tens of micrometers. Such a displacement can likely be attributed to the difference in the thermal expansion of Si and Al (cf. Appendix E).

As a diagnostic tool, micro images of a sample already mounted in the sample holder after a mating cycle can be obtained readily by means of a handheld digital microscope.

2. DC resistance tests

In contrast to the micro imaging tests, which require the removal of the microwave package’s lid, DC resistance tests can be performed in situ at room temperature after the package and package holder have been fully assembled. These tests were performed on all devices presented in this work, including Au, Ag, and Al samples.

The typical test setup comprises a microwave package with two three-dimensional wires each mating with an on-chip pad. The two pads are connected by means of a CPW transmission line with series resistance $R^c$. The back end of the wires is connected to a coaxial cable ending in a microwave connector, similar to the setup in Figs. 4 (d) and 4 (c). The DC equivalent circuit of this setup can be represented by way of a four-terminal Pi network. The circuit comprises an input “i” and output “o” terminal, two terminals connected to a common ground “g,” an input-output resistor with resistance $R_{io}$, and two resistors to ground with resistance $R_{ig}$ and $R_{og}$. The i and o terminals correspond to the inner conductor of the two microwave connectors. The outer conductor of both connectors is grounded.

The resistance $R_{io}$ is that of the center conductor of the CPW transmission line, including the contact resistance $R^c$ for each wire-pad interface and the series resistance $R^{cc}$ of the wire’s and coaxial cable’s inner conductor, $R_{io} = R^c + 2(R^c + R^{cc})$. The resistances $R_{ig}$ and $R_{og}$ are those of the path between each center conductor and ground and include the resistance of the inner and outer conductor of the various coaxial cables and wires as well as any wire-pad contact resistance. Ideally, these ground resistances should be open circuits. In reality, they are expected to have a finite but large value because of the intrinsic resistance of the Si wafers used as a substrate.

The design parameters, electrical properties, measurement conditions as well as the measured values of $R_{io}$, $R_{ig}$, and $R_{og}$ for various Au, Ag, and Al samples are reported in Table II. The resistances were probed by means of a multimeter from the Fluke Corporation, model 289 [30]. Measuring resistances significantly different from the expected values means that either a lateral or rotational misalignment occurred.

The resistances for some Au samples were also measured at 77 K to verify whether a good room temperature alignment persisted in cryogenic conditions. The cold measurements were realized by dunking the package holder into liquid nitrogen.

The measured value of $R_{io}$ for the Ag samples is larger than the estimated trace resistance by ∼650 mΩ. This simple result makes it possible to find an upper bound value for the contact resistance, $R^c \lesssim 325$ mΩ. A more accurate estimate of the contact resistance based on four-point measurements will be described in Subsec [IV A].

The DC resistance testing procedure presented here will be useful in integrated-circuit quantum information processing, where, for example, CPW transmission lines can serve as qubit readout lines [34-36]. These tests can be expanded to encompass different circuit structures such as the qubit control lines utilized in Ref. [36].

IV. CHARACTERIZATION

The three-dimensional wires are multipurpose interconnects that can be used to transmit signals over a wide frequency range, from DC to 10 GHz. These signals can be: The current bias used to tune the transition frequency of a superconducting qubit; the Gaussian-modulated sinusoidal or the rectangular pulses that, respectively, make it possible to perform XY and Z control on a qubit; the continuous monochromatic microwave tones used to read out a qubit state or to populate and
TABLE II. DC resistance tests. Multiple Au samples were measured. For all samples the length from the center of one pad to that of the opposite pad of the CPW center conductor is \( L_{\text{pp}} = 11.5 \text{ mm} \). In the table are reported: The width \( W \) of each CPW transmission line; the thickness \( d \) of the metal; the metal volume resistivity \( \rho \) at room temperature or at 77 K; the input and output wire pressure settings \( \ell_{\text{p}} \) and \( \ell_{\text{op}} \), respectively; the operating temperature \( T \); the number of measurements \( N \); the estimated trace resistance \( R^\ell \) (for the Au samples, the very large parallel resistance \( \sim 46 \text{k}\Omega \) at room temperature due to the titanium (Ti) adhesion layer was neglected); the measured resistances \( R_{\text{io}}, R_{\text{ig}}, \) and \( R_{\text{og}} \). For a given chip, each resistance was measured independently \( N \) times under similar measurement conditions. The mean values and standard deviations of \( R_{\text{io}} \) are provided; the minimum values of \( R_{\text{og}} \) and \( R_{\text{ig}} \) are given. Note that because \( R^\ell + R_{\text{con}} \ll R^\ell \), we expect \( R_{\text{io}} \approx R^\ell \). The discrepancy between the estimated and measured values \( (R^\ell \text{ and } R_{\text{io}}) \) for the Au and Al samples is mainly due to uncertainties associated with the metal thickness \( d \). The inaccuracies are smaller for thicker films, as in the case of the 3 \( \mu \text{m} \) Ag samples.

| Metal | \( W \) (\( \mu \text{m} \)) | \( d \) (\( \text{nm} \)) | \( \rho \) \((1 \times 10^{-9} \text{\Omega m})\) | \( \ell_{\text{p}} \) (\( \text{mm} \)) | \( \ell_{\text{op}} \) (\( \text{mm} \)) | \( T \) (K) | \( N \) | \( R^\ell \) (\( \Omega \)) | \( R_{\text{io}} \) (\( \Omega \)) | \( R_{\text{ig}} \) (\( \text{M}\Omega \)) | \( R_{\text{og}} \) (\( \text{M}\Omega \)) |
|-------|----------------|----------------|----------------|----------------|----------------|-------|------|--------|--------|--------|--------|
| Au    | 10             | 100            | 22             | 4.52           | 4.44           | 300   | 30   | 253    | 218(3) | 31     | 31     |
| Au    | 10             | 100            | 22             | 4.97           | 4.89           | 300   | 2    | 253    | 223(0) | 38     | 38     |
| Au    | 10             | 100            | 22             | 4.18           | 4.11           | 300   | 2    | 253    | 217(0) | 39     | 39     |
| Au    | 10             | 100            | 22             | 4.57           | 4.45           | 300   | 2    | 253    | 229(0) | 28.8   | 28.6   |
| Au    | 10             | 200            | 22             | 4.60           | 4.70           | 300   | 10   | 126.5  | 98.0(7) | 50     | 50     |
| Au    | 10             | 200            | 4.55           | 4.60\(^{[2]}\) | 4.70\(^{[3]}\) | 77    | 6    | 2.04   | 2.71(4) | 0.0043 | 0.0043 |
| Ag    | 30             | 3000           | 16             | 4.60           | 4.70           | 300   | 6    | 2.04   | 36.02(2)| 77.3   | 81.8   |
| Al    | 15             | 120            | 26             | 4.25           | 4.07           | 300   | 24   | 166.1  | 171(1) | 0.0042 | 0.0042 |

\(^{[a]}\) At 300 K.

measure a superconducting resonator \[2, 3, 34, 36\]. In general, the wires can be used to transmit any bandpass modulated carrier signal within the specified frequency spectrum, at room and cryogenic temperatures.

In this section, we report experimental results for a series of measurements aiming at a complete electrical characterization of the quantum socket at room temperature and at approximately 77 K (i.e., in liquid nitrogen). First, we performed four-point measurements to estimate the contact resistance of a three-dimensional wire. Second, we measured the S-parameters of a wire at room temperature. Third, we measured the S-parameters of the quantum socket with an Au sample at room temperature and at 77 K and an Ag sample at room temperature. Fourth, we realized time-domain measurements of the quantum socket. Last, we performed four-port S-parameter measurements in order to assess the socket crosstalk properties.

A. Four-point measurements

The wire-pad contact resistance \( R^c \) is an important property of the quantum socket. In fact, a large \( R^c \) would result in significant heating when applying DC bias signals and rectangular pulses, thus deteriorating qubit performance.

In order to assess \( R^c \) for the inner and outer conductor of a three-dimensional wire, we performed four-point measurements using the setup shown in the inset of Fig. 6. Using this setup, we were able to measure both the series resistance of the wire \( R^w \) and the contact resistance \( R^c \). This allows us to estimate the overall heating that could be generated during a qubit experiment.

The setup comprises a microwave package with a chip entirely coated with a 120 nm thick Al film; no grounding washer was used. The package featured three three-dimensional wires, of which two were actually measured; the third wire was included to provide mechanical stability. The package was attached to the MC stage of a DR and connected to a set of phosphor bronze twisted pairs. The twisted pairs were thermally anchored at all DR stages and connected at room temperature to a precision source-measure unit (SMU) from Keysight Technologies Inc., model B2911A.

We measured the resistance between the inner conductor of a wire and ground, \( R_{\text{ig}} \). This resistance comprises the inner conductor wire resistance \( R^w_{\text{i}} \) in series with the inner conductor contact resistance \( R^c_{\text{i}} \) and any resistance to ground, \( R_g \). Note that, at the operation temperature of the experiment (\( \sim 10 \text{ mK} \)), Al is superconducting and, thus, the metal resistance can be neglected.

Figure 6 shows the current-voltage (I-V) characteristic curve for \( R_{\text{ig}} \). With increasing bias currents, the contact resistance results in hot-spot generation leading to a local breakdown of superconductivity. For sufficiently high bias currents, superconductivity breaks down completely. At such currents, the observed hysteretic behavior indicates the thermal limitations of our setup. Note, however, that these currents are at least one order of magnitude larger than the largest bias current required in typical superconducting qubit experiments [60].

In order to estimate \( R_{\text{ig}} \) from the I-V characteristic curve, we selected the bias current region from \(-1.5 \text{ mA} \) to \(+1.5 \text{ mA} \) and fitted the corresponding slope. We obtained \( R_{\text{ig}} \approx 148 \text{ m}\Omega \). This value, which represents an
upper bound for the wire resistance and the wire-pad contact resistance, \((R_w^+ + R_g^+))\), is significantly larger than that associated with Al wire bonds \([61]\). In future versions of the three-dimensional wires we will attempt to reduce the wire-pad contact resistance by rounding the tip of the center conductor, stiffening the wire springs, using a thicker metal film for the pads, and plating the contact pads with Au or titanium nitride. We note, however, that even a large value of the wire and/or wire-pad contact resistance will not significantly impair the quantum socket microwave performance.

### B. Two-port scattering parameters

The S-parameter measurements of a bare three-dimensional wire were realized by means of the setup shown in the inset of Fig. 7 (a). The device under test (DUT) comprises a cable assembly attached to a three-dimensional wire by means of a screw-in micro connector. The cable assembly is made of an approximately 230 mm long semi-rigid coaxial cable EZ 47, which is soldered to an EZ Form custom-made Sub-miniature type A (SMA) male connector, model 705538-347. The other end of the coaxial cable is soldered to the screw-in micro connector. The SMA connector of the DUT is connected to one port of a vector network analyzer (VNA) from Keysight, model PNA-L N5230A by means of a flexible coaxial cable. The bottom interface of the wire is connected to a 2.92 mm end launch connector from Southwest Microwave, Inc., model 1092-01A-5, which then connects to the other port of the VNA through a second flexible coaxial cable. The 2.92 mm adapter is characterized by a flush coaxial back plane, which mates with the wire bottom interface well enough to allow for S-parameter measurements up to 10 GHz.

In order to measure the S-parameters of the DUT, a two-tier calibration was performed. First, a two-port electronic calibration module (ECal) from Keysight, model N4691B, with 2.92 mm male connectors was used to set the measurement planes to the end of the flexible cables closer to the DUT. Second, a port-extension routine was performed to correct for the insertion loss, phase, and delay of the 2.92 mm adapter. This made it possible to set the measurement planes to the ports of the DUT.

The magnitudes of the measured reflection and transmission S-parameters are displayed in Fig. 7 (a). We performed microwave simulations of a three-dimensional wire for the same S-parameters (cf. Subsec. III D) for the electric field distribution), the results of which are plotted in Fig. 7 (b). The S-parameters were measured and simulated between 10 MHz and 10 GHz. The S-parameters \(|S_{21}| \) and \(|S_{12}| \) show a featureless microwave response, similar to that of a coaxial transmission line. The attenuation at 6 GHz is \(|S_{21}| \approx -0.58 \text{ dB} \) and the magnitude of the reflection coefficients at the same frequency is \(|S_{11}| \approx -13.8 \text{ dB} \) and \(|S_{22}| \approx -14.0 \text{ dB} \). The phase of the various S-parameters (not shown) behaves as expected for a coaxial transmission line. All measurements were performed at room temperature.

The S-parameter measurements of a three-dimensional wire indicate a very good microwave performance. However, these measurements alone are insufficient to fully characterize the quantum socket operation. A critical feature that deserves special attention is the 90° transition region between the wire bottom interface and the on-chip CPW pad. It is well-known that 90° transitions can cause significant impedance mismatch and, thus, signal reflection \([47]\). In quantum computing applications, these reflections could degrade both the qubit control and readout fidelity.

Figure 8 shows a typical setup for the characterization of a wiring configuration analogous to that used for qubit operations. The setup comprises a VNA from Keysight, model PNA-X N5242A, with ports 1 and 2 connected to a pair of flexible coaxial cables from Huber+Suhner AG, model SucoFlex 104-PE (with SMA male connectors). In order to calibrate the measurement, the flexible cables were first connected to a two-port ECal module.
FIG. 7. S-parameter measurements and simulations of a three-dimensional wire at room temperature. (a) Magnitude of the measured S-parameters $|S_{mn}|$, with $m,n = \{1,2\}$. Inset: Image of the measurement setup. From left to right: Segment of flexible coaxial cable (grey); SMA female connector (red); after plane i, SMA male connector (orange); segment of EZ 47 cable (grey); screw-in micro connector (green); three-dimensional wire (purple); after plane ii, 2.92 mm end launch connector (white and black); SMA female connector (red); segment of flexible coaxial cable (grey). (b) S-parameter simulations. The lower attenuation is due to idealized material properties and connections.

We performed a two-port S-parameter measurement of the DUT from 10 MHz to 10 GHz. We selected an intermediate frequency (IF) bandwidth $\Delta f_{IF} = 500$ Hz, a constant excitation power $P_{RF} = 0$ dB-milliwatts (dBm), and $N_{RF} = 12001$ or $N_{RF} = 100001$ measurement points for the Au and Ag samples, respectively. The measurement results at room temperature for the Au and Ag samples are shown in Figs. 9 (a) and 10 (a), respectively [63]. The results for the Au sample at 77 K are shown in Fig. 9 (b).

The S-parameter measurements of the Au sample show that the quantum socket functions well at microwave frequencies, both at room temperature and at 77 K. Since most of the mechanical shifts have already occurred when cooling to 77 K [64], this measurement allows us to deduce that the socket will continue functioning even at lower temperatures, e.g., $\sim 10$ mK. The Au sample, however, is characterized by a large value of $R_{io}$, which may conceal unwanted features both in the transmission and reflection measurements. Therefore, we prepared an Ag sample that exhibits a much lower resistance even at room temperature. The behavior of the Ag S-parameters is similar to that of a transmission line or coaxial connector. For example, $|S_{11}|$ is approximately $-15$ dB; as a reference, for a high-precision SMA connector at the same frequency $|S_{11}| \approx -30$ dB.

The presence of the screw-in micro connector can occasionally deteriorate the microwave performance of the quantum socket. In fact, if the micro connector is not firmly tightened, a dip in the microwave transmission is observed. At room temperature, it is straightforward to remove the dip by simply re-tightening the connector when required. On the contrary, for the measure-
FIG. 8. Microwave characterization setup. The vertical black dashed lines indicate main reflection planes. The yellow terminations correspond to SMA male connectors at the end of each cable. The input/output flexible cable corresponds to the region in between planes i and ii(xii and xiii), in gray; the blue blocks correspond to SMA female bulkhead adapters; the plane ii(xii) correspond to the input/output port of the DUT; the orange block corresponds to an SMA male to SMA female adapter; the EZ 47 input/output cable corresponds to the region in between planes iv and v(x and xi), in gray; the plane v(x) corresponds to the solder connection on the three-dimensional wire; the plane vi(ix) is associated with the screw-in micro connector; the plane vii(viii) corresponds to the 90° interface connecting each three-dimensional wire to the input/output of the CPW transmission line (pale blue). The three-dimensional wires are indicated in purple.

FIG. 9. S-parameter measurements for the Au sample. (a) $|S_{mn}|$ at room temperature. (b) $|S_{mn}|$ at 77 K. The transmission coefficients show that the DUT is a reciprocal device (i.e., $S_{21} \approx S_{12}$), as expected for a passive structure. The inset in (b) shows the unwrapped phase angle $\angle S_{21}$; the black dashed lines delimit the frequency region between 1 GHz and 3 GHz. Note that the reflection coefficients $S_{11}$ and $S_{22}$ are relatively large at very low frequency. This is expected for a very lossy transmission line. In fact, the center conductor for the Au sample is characterized by a series resistance (cf. Table II) $R_{io} \approx 98 \Omega$ at room temperature, which corresponds to $S_{11} \approx S_{22} \approx -6 \text{ dB}$ at 10 MHz, and $R_{io} \approx 36 \Omega$ at 77 K, which corresponds to $S_{11} \approx S_{22} \approx -12 \text{ dB}$ at 10 MHz. These findings are consistent with the TDR results to be shown in Fig. 11 where the large impedance steps are also due to the large series resistance (cf. Subsec. IV C). The low-loss Ag sample shows much lower reflection coefficients at low frequency (cf. Fig. 10), whereas the lossy Al sample shows high reflections at low frequency and room temperature (cf. Fig. 15 (a) in Sec. V).

Note that the dip is far from the typical operation frequencies for superconducting qubits. Additionally, as briefly described in Sec. VI, we will remove the screw-in micro connector from future generations of the three-dimensional wires.
the latter capture well some of the characteristic features of the microwave response of the DUT. In particular, the measured and simulated reflection coefficients display a similar frequency dependence. It is worth mentioning that we also simulated the case where the wire bottom interface is not perfectly aligned with the on-chip pad (results not shown). We considered lateral misalignments of 100 µm and rotational misalignments of ~ 20°. This allowed us to study more realistic scenarios, such as those shown in Fig. 5. We found that the departure between the misaligned and the perfectly aligned simulations was marginal. For example, the transmission S-parameters varied only by approximately ± 0.5 dB.

In Appendix [65], we show a set of microwave parameters obtained from the measured S-parameters for the Au sample at room temperature and at 77 K and for the Ag sample at room temperature. These parameters make it possible to characterize the input and output impedance as well as the dispersion properties of the quantum socket.

C. Time-domain reflectometry

In TDR measurements, a rectangular pulse with fast rise time and fixed length is applied to a DUT; the reflections (and all re-reflections) due to all reflection planes in the system (i.e., connectors, geometrical changes, etc.) are then measured by way of a fast electrical sampling module. The reflections are, in turn, related to the impedances of all of the system components. Thus, TDR makes it possible to estimate any impedance mismatch and its approximate spatial location in the system.

TDR measurements were performed on the DUT shown in Fig. 8, with the same Au or Ag sample as for the measurements in Subsec. [65] As always, the Au sample was measured both at room temperature and at 77 K, whereas the Ag sample was measured only at room temperature. The TDR setup is analogous to that used for the S-parameter measurements, with the following differences: The DUT input and output reference planes were extended to include the SucoFlex flexible coaxial cables (i.e., these cables were not calibrated out); when testing the DUT input port, the output port was terminated in a load with impedance $Z_L = Z_c$ and vice versa when testing the DUT output port. The TDR measurements were realized by means of a sampling oscilloscope from Teledyne LeCroy, model WaveExpert 100H; the oscilloscope features an electrical sampling module with 20 GHz bandwidth and a TDR step generator, model ST-20. The generated signal is a voltage square wave characterized by a nominal pulse rise time of 20 ps, amplitude of 250 mV, pulse width of 300 ns, and pulse repetition rate of 1 MHz. The voltage reflected by the DUT, $V^-$, is acquired as a function of time $t$ by means of the sampling module. This time is the round-trip interval necessary for the voltage pulse to reach a DUT reflection plane and return back to the sampling module. The measured quantity is given by

$$V_{\text{meas}}(t) = V^+(t) + V^-(t)$$

where $V^+$ is the amplitude of the incident voltage square wave. From Eq. (2), we can obtain the first-order instan-
aneous impedance as \[ Z(t) = Z_c \frac{1 + \xi(t)}{1 - \xi(t)} , \tag{3} \]

where \( \xi(t) = (V_{\text{meas}}(t) - V^+)/V^+ \).

Figure 11 shows \( Z(t) \) for the DUT with the Au sample at room temperature and at 77 K; the measurement refers to the input port of the DUT, including a 2.0 m flexible cable. The figure inset shows the room temperature data for a shorter time interval. This corresponds to a space interval beginning at a point between planes iv and v and ending at a point between planes vii and viii (cf. Fig. 8).

Figure 12 (a) shows \( Z(t) \) for the Ag sample at room temperature. Figure 12 (b) displays the data in (a) for a time interval corresponding to a space interval beginning at a point between planes iv and v and ending at a point between planes x and xi; as a reference, the Au data are overlaid with the Ag data.

For the Au sample, the first main reflection plane (plane ii) is encountered at \( t \approx 18 \) ns. The second main reflection plane (plane v) appears after \( \sim 2.5 \) ns relative to the first plane, at \( t \approx 20.5 \) ns. From that time instant and for a span of approximately 250 ps, the TDR measurement corresponds to \( Z(t) \) of the three-dimensional wire itself. The maximum impedance mismatch between the EZ Form cable and the three-dimensional wire is approximately 10 \( \Omega \). The third main reflection plane (plane vii) corresponds to the 90° transition region; for the Au sample, it is impossible to identify features beyond this plane owing to the large series resistance of the on-chip CPW transmission line. From empirical evidence, the impedance \( Z(t) \) of a lossy line with series resistivity \( \rho \) increases linearly with the length of the line \( L \) as \( \rho L/(Wd) \). In fact, for the Au sample we measured an impedance step across the CPW transmission line of approximately 100 \( \Omega \) at room temperature and 40 \( \Omega \) at 77 K. These steps are approximately the \( R_{\text{in}} \) values reported in Table II.

In order to obtain a detailed measurement of the impedance mismatch beyond the 90° transition region, we resorted to the TDR measurements of the DUT with the much less resistive Ag sample. First, we confirmed that \( Z(t) \) of the input three-dimensional wire for the Ag sample is consistent with the TDR measurements of the Au sample; this is readily verified by inspecting Fig. 12 (b). The three-dimensional wire is the structure ending at the onset of the large impedance step shown by the Au overlaid data. The structure spanning the time interval from \( t \approx 20.5 \) ns to \( t \approx 21 \) ns is associated with the input transition region, the CPW transmission line, and the output transition region. The output three-dimensional wire starts at \( t \approx 21 \) ns, followed by the EZ Form coaxial cable, which finally ends at the SMA bulk-
head adapter at \( t \simeq 23.5 \) ns. The maximum impedance mismatch associated with the transition regions and the CPW transmission line is \( \sim 5 \) \( \Omega \). Notably, this mismatch is smaller than the mismatch between the three-dimensional wire and the coaxial cable. This is an important result. In fact, while it would be hard to diminish the impedance mismatch due to the transition region, it is feasible to further minimize the wire mismatch by creating accurate lumped-element models of the wire and use them to minimize stray capacitances and/or inductances \[67\].

It is worth comparing \( Z(t) \) of the quantum socket with that of a standard package for superconducting qubits, where wire bonds are used to make interconnections between a printed circuit board and the control and measurement lines of a qubit on a chip. A detailed study of the impedance mismatch associated with wire bonds is found in Ref. \[37\], where the authors have shown that a long wire bond (of length between \( \sim 1 \) mm and \( 1.5 \) mm; typical length in most applications) can lead to an impedance mismatch larger than \( 15 \) \( \Omega \) (cf. Fig. S3 in the supplementary information of Ref. \[37\]); on the contrary, a short wire bond (between \( \sim 0.3 \) mm and \( 0.5 \) mm; less typical) results in a much smaller mismatch, approximately \( 2 \) \( \Omega \). In terms of impedance mismatch the current implementation of the quantum socket, which is limited by the mismatch of the three-dimensional wires, lies in between these two extreme scenarios.

D. Signal crosstalk

Crosstalk is a phenomenon where a signal being transmitted through a channel generates an undesired signal in a different channel. Inter-channel isolation is the figure of merit that quantifies signal crosstalk and that has to be maximized to improve signal integrity. Crosstalk can be particularly large in systems operating at microwave frequencies, where, if not properly designed, physically adjacent channels can be significantly affected by coupling capacitances and/or inductances. In quantum computing implementations based on superconducting quantum circuits, signal crosstalk due to wire bonds has been identified to be an important source of errors and methods to mitigate it have been developed \[44, 68, 69\]. However, crosstalk remains an open challenge and isolations (opposite of crosstalk) lower than 20 dB are routinely observed when using wire bonds \[70\]. The coaxial design of the three-dimensional wires represents an advantage over wire bonds. The latter, being open structures, radiate more electromagnetic energy that is transferred to adjacent circuits. The former, being enclosed by the outer conductor, limit crosstalk due to electromagnetic radiation.

In realistic applications of the quantum socket, the three-dimensional wires must land in close proximity of several on-chip transmission lines. In order to study inter-channel isolation in such scenarios, we designed a special device comprising a pair of CPW transmission lines, as shown in the inset of Fig. 13(a). One transmission line connects two three-dimensional wires (ports 1 and 2), exactly as for the devices studied in Subsecs. IV.B

![FIG. 13. Signal crosstalk. (a) Transmission and crosstalk coefficients for the Ag sample shown in the inset. The numbers adjacent to the pads in the inset correspond to the device ports. Reciprocal and reflection S-parameters are not shown. (b) Microwave simulation of the same device. The origin of the peaks at approximately 7 GHz is explained in the main text.](image)
and [IVC] the other line, which also connects two three-dimensional wires (ports 3 and 4), circumvents the wire at port 1 by means of a CPW semicircle. The distance between the semicircle and the wire outer conductor is designed to be as short as possible, $\sim 100$ $\mu$m.

The chip employed for the crosstalk tests is similar to the Ag sample used for the socket microwave characterization and was part of a DUT analogous to that shown in Fig. [9]. The DC resistances of the center trace of the 1–2 and 3–4 transmission lines were measured and found to be $\sim 2.8$ $\Omega$ and $\sim 4.5$ $\Omega$, respectively (note that the 3–4 transmission line is $\sim 18.0$ $\mu$m long). All DC resistances to ground and between the two transmission lines were found to be on the order of a few kilohms, demonstrating the absence of undesired short circuit paths. A four-port calibration and measurement of the DUT were conducted by means of the ECal module and PNA-X. We selected a frequency range from 10 MHz to 10 GHz, $\Delta f_{IF} = 1$ kHz, $P_{RF} = 0$ dBm, and $N_{RF} = 64001$. Among the 16 S-parameters, Fig. [13] (a) shows the magnitude of the transmission coefficients $S_{21}$ and $S_{43}$, along with the magnitude of the crosstalk coefficients $S_{31}$, $S_{41}$, $S_{32}$, and $S_{42}$.

The results show that the isolation in the typical qubit operation bandwidth, between 4 GHz and 8 GHz, is larger than $\sim 45$ dB. Note that the crosstalk coefficients shown in Fig. [13] (a) include attenuation owing to the series resistance of the Ag transmission lines. The actual isolation, due only to spurious coupling, would thus be smaller by a few decibels.

Figure [13] (b) shows the microwave simulations of the crosstalk coefficients, which agree reasonably well with the experimental results. These simulations are based on the models explained in Subsec. [V]. From simulations, we believe the isolation is limited by the crosstalk between the CPW transmission lines, instead of the three-dimensional wires. Note that the peaks at approximately 7 GHz correspond to an enhanced crosstalk due to a box mode in the microwave package. The peaks appear in the simulations, which are made for a highly conductive package, and may appear in measurements performed below $\sim 1$ $K$, when the Al package becomes superconductive. For the room temperature measurements shown in Fig. [13] (a), these peaks are smeared out due to the highly lossy Al package.

V. APPLICATIONS TO SUPERCONDUCTING RESONATORS

Thus far, we have shown a detailed characterization of the quantum socket in DC and at microwave frequencies, both at room temperature and at 77 $K$. In order to demonstrate the quantum socket operation in a realistic quantum computing scenario, we used a socket to wire a set of superconducting CPW resonators cooled to approximately 10 mK in a DR. We were able to show an excellent performance in the frequency range from 4 GHz to 8 GHz, which is the bandwidth of our measurement apparatus.

The experimental setup is described in Appendix [H] and shown in Fig. [19]. Figure [14] shows a macro photograph of a 15 mm x 15 mm chip housed in the sample holder; the chip is the Al sample described in Subsec. [III], with geometrical and DC electrical parameters reported in Table [III]. The sample comprises a set of three CPW transmission lines, each connecting a pair of three-dimensional wire pads; multiple shunted CPW resonators are coupled to each transmission line. In this section, we will focus only on transmission line three and its five resonators. The transmission line has a center conductor width of 15 $\mu$m and gap width of 9 $\mu$m, resulting in a characteristic impedance of approximately 50 $\Omega$. The resonators are $\lambda/4$-wave resonators, each characterized by a center conductor of width $W$ and a dielectric gap of width $G$. The open end of the resonators runs parallel to the transmission line for a length $\ell_c$, providing a capacitive coupling; a 5 $\mu$m ground section separates the gaps of the transmission line and resonators (cf. Fig. S2 of the Supplemental Material at [http://www.Supplemental-Material-Bejanin]). The nominal resonance frequency $f_0$ as well as all the other resonator parameters are reported in Table [III].

A typical DR experiment employing the quantum

![FIG. 14. Macro photograph of an Al sample mounted in a sample holder with grounding washer. The image shows three CPW transmission lines each coupled to a set of $\lambda/4$-wave resonators. The grounding washer, with its four protruding feet, is placed above the chip covering the chip edges. The marks imprinted by the bottom interface of the three-dimensional wires on the Al pads are noticeable. More detailed images of these marks are shown in Fig. [5].](http://www.Supplemental-Material-Bejanin)
socket consists of the following steps. First, the sample is mounted in the microwave package, which has already been attached to the package holder (cf. Subsec. II C and Sec. III). Second, a series of DC tests is performed at room temperature. The results for a few Al samples are reported in Table II. Third, the package holder assembly is characterized at room temperature by measuring its S-parameters. The results of such a measurement are shown in Fig. 15 (a). Fourth, the package is mounted by means of the SMP connectors to the MC stage of the DR and an $S_{21}$ measurement is performed. The results (magnitude only) are shown in Fig. 15 (b) in the frequency range between 10 MHz and 10 GHz. Fifth, the various magnetic and radiation shields of the DR are closed and the DR is cooled down. Sixth, during cooldown the $S_{21}$ measurement is repeated first at $\sim$ 3 K and, then, at the DR base temperature of approximately 10 mK. The results are shown in Figs. 15 (b) and (c), respectively. At $\sim$ 3 K we note the appearance of a shallow dip at approximately 5.7 GHz, probably due to a screw-in micro connector becoming slightly loose while cooling (cf. Subsec. IV B). It is important to
TABLE III. Resonator parameters. The measured resonance frequency is $f_0$. The rescaled coupling and internal quality factors $Q^*_\text{c}$ and $Q_i$, respectively, are obtained from the fits of the measured transmission coefficients (cf. main text for details).

| $i$ | $f_0$ (MHz) | $\ell_c$ (µm) | $G$ (µm) | $Q^*_\text{c}$ (-) | $Q_i$ (-) |
|-----|-------------|--------------|---------|------------------|---------|
| 1   | 4600.0      | 8            | 5       | 400              | 5012    |
| 2   | 5000.0      | 15           | 9       | 300              | 14567   |
| 3   | 5800.0      | 25           | 15      | 400              | 10269   |
| 4   | 7000.0      | 15           | 9       | 300              | 6230    |
| 5   | 7400.0      | 8            | 5       | 400              | 4173    |

VI. CONCLUSIONS

Figure 16 shows an extensible quantum computing architecture where a two-dimensional square lattice of superconducting qubits is wired by means of a quantum socket analogous to that introduced in this work. The architecture comprises three main layers: The quantum hardware; the shielding interlayer; the three-dimensional wiring mesh.

As shown in Fig. 16 (a), the quantum hardware is realized as a two-dimensional lattice of superconducting qubits with nearest neighbor interactions. The qubits are a modified version of the Xmon presented in Ref. [60]. Each qubit is characterized by seven arms that make it possible to connect it to one XY and one Z control line as well as one measurement resonator and four inter-qubit coupling resonators. We name this type of qubit the heptaton. The inter-qubit coupling is mediated by means of superconducting CPW resonators that allow the implementation of control Z (CZ) gates between two neighboring qubits [71][72]. A set of four heptatons can be readout by way of a single CPW transmission line connected to four CPW resonators, each with a different resonant frequency. Figure 16 also shows the on-chip pads associated with each three-dimensional wire. In the Supplemental Material at [http://www.Supplemental-Material-Bejanin](http://www.Supplemental-Material-Bejanin), we propose a more general surface code architecture where each qubit can be measured by means of two different resonators, one with frequency above and the other with frequency below all coupling resonator frequencies.

Assuming a pitch between two adjacent three-dimensional wires of 1 mm, the lateral dimension of one square cell having four heptatons at its edges is 8 mm. The three distances $A$, $B$, and $C$ between wire pads and resonators leading to this quantity are indicated in Fig. 16 (b). It is thus possible to construct a two-dimensional lattice of $10 \times 10$ heptatons on a square chip with lateral dimension $9 \times 8 \text{mm} = 72 \text{mm}$. A $72 \text{mm} \times 72 \text{mm}$ square chip is the largest chip that can be diced from a standard 4 inch wafer. This will allow the implementation of a logical qubit based on the surface code, with at least distance five [9]. In this architecture, the coupling resonators act as a coherent spacer between pairs of qubits, i.e., they allow a sufficient separation to accommodate the three-dimensional wires, while maintaining qubit coherence during the CZ gates. Additionally, these resonators will help mitigate qubit crosstalk compared to architectures based on direct capacitive coupling between adjacent qubits (cf. Ref. [36]). In fact, they will suppress qubit-mediated coupling between neighboring control lines [73]. It is worth noting that adjacent coupling resonators can be suitably designed to be at different frequencies, thus further diminishing qubit-mediated crosstalk.

Implementing a large qubit chip with a lateral dimension of 72 mm presents significant challenges to the qubit operation at microwave frequencies. A large chip must be housed in a large microwave package, causing the appearance of box modes that can interfere with the qubit control and measurement sequences [44]. Moreover, a large chip will inevitably lead to floating ground planes that can generate unwanted slotline modes [44]. All these parasitic effects can be suppressed by means of the shielding interlayer, as shown in Fig. 16 (a). This layer can be wafer bonded [39] to the quantum layer. Through holes and cavities on the bottom part of the layer can be readily fabricated using standard Si etching techniques. The holes will house the three-dimensional wires whereas the
FIG. 16. Extensible quantum computing architecture. (a) Architecture main three layers: The quantum hardware (bottom); the shielding interlayer (middle); the three-dimensional wiring mesh (top). The vertical magenta dashed lines with double arrows show the mounting procedure to be used to prepare the assembly. The middle layer (thinner) will be metalized on the bottom and wafer bonded to the quantum layer beneath. The back end of the wires (top) will be connected to SMPS connectors (not shown). (b) Two-dimensional view of the quantum hardware. The distances between coupling resonators and wire pads are $A = C = 2.25\text{ mm}$ and $B = 3.5\text{ mm}$. Note that the Z control lines are represented as galvanically connected to the heptatons, similar to Ref. [60]. The measurement can be multiplexed so that four qubits are readout by one line only.

cavities will accommodate the qubit and resonator structures on the quantum hardware. Large substrates also generate chip modes that, however, can be mitigated using buried metal layers and through vias [68].

The three-dimensional wires to be used for the $10 \times 10$ qubit architecture will be an upgraded version of the wires used in this work. In particular, the M2.5 thread will be removed and the wires will be inserted in a dedicated substrate (cf. Fig. 16(a)); additionally, the screw-in micro connector will be substituted by a direct connection to a subminiature push-on sub-micro (SMPS) connector (not shown in the figure).

In future applications of the quantum socket, we envision an architecture where the three-dimensional wires will be used as interconnect between the quantum layer and a classical control/measurement layer. The classical layer could be realized using RSFQ digital circuitry [39, 40]. For example, high-sensitivity digital down-converters (DDCs) have been fabricated based on RSFQ electronics [74]. Such circuitry is operated at very low temperatures and can substitute the room temperature electronics used for qubit readout. Note that cryogenic DDC chips with dimensions of less than $5\text{ mm} \times 5\text{ mm}$ can perform the same operations presently carried out by room temperature microwave equipment with an overall footprint of $\sim 50\text{ cm} \times 50\text{ cm}$. Recent interest in reducing dissipation in RSFQ electronics [76] will possibly enable the operation of the classical electronics in close proximity to the quantum hardware. We also believe it is feasible to further miniaturize the three-dimensional wires so that the wire outer diameter would be on the order of $500\mu\text{m}$. Assuming a wire-wire pitch also of $500\mu\text{m}$, it will therefore be possible to realize a lattice of $250000$ wires connecting to $\sim 10^5$ qubits arranged on a $315 \times 315$ two-dimensional qubit grid with dimensions of $1\text{ m} \times 1\text{ m}$. This will allow the implementation of simple fault tolerant operations between a few tens of logical qubits.

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Appendix A: WIRE COMPRESSION

In this appendix, we discuss the pressure settings of the three-dimensional wires. In the current implementation of the quantum socket, the pressure exerted by the three-dimensional wires on the chip is controlled by the installation depth of the wire in the lid. This depth depends on the number of rotations used to screw the wire into the M2.5-threaded hole of the lid. Since the wire's tunnel has to be aligned with the corresponding chip pad, a discrete number of wire pressure settings is allowed. For the package shown in Fig. 1(b) and Fig. 1(c), the minimum length an unloaded wire has to protrude from the ceiling of the lid's internal cavity to touch the chip surface is \( \ell_c = 3.05 \) mm (cf. Fig. 1(c)). For a maximum wire stroke \( \Delta L = 2.5 \) mm, the maximum length an unloaded wire can protrude from the cavity ceiling without breaking when loaded is \( \ell_c + \Delta L = 5.55 \) mm. The first allowed pressure setting, with wire and pad perfectly aligned, is for \( \ell_p = 3.10 \) mm. The pitch for an M2.5 screw is 0.45 mm. Hence, five pressure settings are nominally possible, for \( \ell_p = 3.10 + 0.45 \) k mm, with \( k = 1, 2, \ldots, 5 \). We found the ideal pressure setting to be for \( k = 3 \), corresponding to a nominal \( \ell_p = 4.45 \) mm; the actual average setting for 12 wires was measured to be \( \ell_p = 4.48 \) mm \( \pm \) 0.28 mm, with standard deviation due to the machining tolerances. For greater depths we experienced occasional wire damage; lesser depths were not investigated. Possible effects on the electrical properties of the three-dimensional wires due to different pressure settings will be studied in a future work.

Appendix B: THE QUANTUM SOCKET

In this appendix, we describe the measurement setup used to characterize the magnetic properties of the materials used in the quantum socket and present the main results. Additionally, we give an estimate of the strength of the magnetic field caused by one three-dimensional wire inside the microwave package.

The ZGC used in our tests comprises three nested cylinders, each with a lid with a central circular hole; the hole in the outermost lid is extended into a chimney that provides further magnetic shielding. The walls of the ZGC are made of an alloy of Ni and Fe (or mumetal alloy) with a high relative permeability \( \mu \). The alloy used for the chamber is a CO-NETIC® AA alloy and is characterized by a DC magnetic permeability at 40 G, \( \mu_{\text{DC}}^{40} = 80000 \), and an AC magnetic permeability at 60 Hz and at 40 G, \( \mu_{\text{AC}}^{40} = 65000 \). As a consequence, the nominal magnetic field attenuation lies between 1000 and 1500. The ZGC used in our tests was manufactured by the Magnetic Shield Corporation, model ZG-209.

The flux gate magnetometer used to measure the magnetic field \( \vec{B} \) is a three-axis DC milligauss meter from AlphaLab, Inc., model MGM3AXIS. Its sensor is a 38 mm \( \times \) 25 mm \( \times \) 25 mm parallelepiped at the end of a \( \sim 1.2 \) m long cable; the orientation of the sensor is calibrated to within 0.1° and has a resolution of 0.01 mG (i.e., 1 nT) over a range of \( \pm \) 2000 mG (i.e., \( \pm \) 200 \( \mu \)T).

The actual attenuation of the chamber was tested by measuring the value of the Earth’s magnetic field with and without the chamber in two positions, vertical and horizontal; inside the chamber the measurements were performed a few centimeters from the chamber base, approximately on the axis of the inner cylinder. In these and all subsequent tests, the magnetic sensor was kept in the same orientation and position. The results are reported in Table VI, which shows the type of measurement performed, the magnitude of the measured magnetic field \( |\vec{B}| \), and the attenuation ratio \( \alpha \). The maximum measured attenuation was \( \alpha \approx 917 \) in the horizontal position.

The ZGC characterization of Table VII also serves as a calibration for the measurements on the materials used for the quantum socket. In these measurements, each test sample was positioned approximately 1 cm away from the magnetic sensor. The results, which are reported in Table VII, were obtained by taking the magnitude of the calibrated field of each sample. The calibrated field itself was calculated by subtracting the background field from the sample field, component by component. Note that the background and sample fields were on the same order of magnitude (between 0.10 mG and 0.80 mG), with background fluctuations on the order of 0.10 mG. Thus, we recorded the maximum value of each \( x \), \( y \), and \( z \) component. Considering that the volume of the measured samples is significantly larger than that of the actual quantum socket components, we are confident that the measured magnetic fields of the materials should be small enough not to significantly disturb the operation of superconducting quantum devices. As part of our magnetism tests, we measured a block of approximately 200 g of 5N5 Al in the ZGC; as shown in Table VII, the magnitude of the magnetic field was found to be within the noise floor of the measurement apparatus [76].

A simple geometric argument allows us to estimate the actual magnetic field due to one three-dimensional wire, without taking into account effects due to superconductivity (most of the wire is embedded in an Al package, which is superconducting at qubit operation temperatures). We assume that one wire generates a magnetic field of 0.25 mG (i.e., the maximum field value in Table VII); this is a large overestimate considering the tested samples had volumes much larger than any component.
in the wires) and is a magnetic dipole positioned 15 mm away from a qubit. The field generated by the wire at the qubit will then be \( B_q \simeq 0.25 r_0^3/0.015^3 \) mG, where \( r_0 \simeq 10 \) mm is the distance at which the field was measured in the ZGC; thus, \( B_q \simeq 0.075 \) mG. Assuming an Xmon qubit [60] with a superconducting quantum interference device (SQUID) of dimensions 40 \( \mu \)m \( \times \) 10 \( \mu \)m, the estimated magnetic flux due to the wire threading the SQUID is \( \Phi_q \simeq 4 \times 10^{-18} \) Wb. This is approximately three orders of magnitude smaller than a flux quantum \( \Phi_0 \simeq 2.07 \times 10^{-15} \) Wb; typical flux values for the Xmon operation are on the order of 0.5\( \Phi_0 \).

**Appendix C: THERMAL CONDUCTANCE OF A THREE-DIMENSIONAL WIRE**

In this appendix, we describe the method used to estimate the thermal performance of a three-dimensional wire and compare it to that of an Al wire bond. Note that at very low temperature, thermal conductivities can vary by orders of magnitude between two different alloys of the same material. The following estimate can thus only be considered correct to within approximately one order of magnitude. Thermal conductivity is a property intrinsic to a material. To characterize the cooling performance of a three-dimensional wire, we instead use the heat transfer rate (power) per kelvin difference, which depends on the conductivity.

The power transferred across an object with its two extremities at different temperatures depends on the cross-sectional area of the object, its length, and the temperature difference between the extremities. Since the cross section of a three-dimensional wire is not uniform, we assume the wire is made of two concentric hollow cylinders. The cross-sectional area of the two cylinders is calculated by using dimensions consistent with those of a three-dimensional wire. The inner and outer hollow cylinders are assumed to be made of phosphor bronze and brass alloys, respectively. The thermal conductivities of these materials at low temperatures are determined by extrapolating measured data to 25 mK [77].

The Al wire bonds are assumed to be solid cylinders with diameter 50 \( \mu \)m. In the superconducting state, the thermal conductivity of Al can be estimated by extrapolating literature values [78].

The heat transfer rate per kelvin difference is calculated by multiplying the thermal conductivity \( k \) with the cross-sectional area \( A \) and dividing by the length of the thermal conductor \( \ell \). The heat transfer rate per kelvin difference of a three-dimensional wire is calculated by summing the heat transfer rate per kelvin difference of the inner conductor to that of the outer conductor and is found to be \( \Pi_t \simeq 6 \times 10^{-7} \) W K\(^{-1}\) at 25 mK. At the same temperature, the heat transfer rate per kelvin of a typical Al wire bond is estimated to be \( \Pi_t \simeq 4 \times 10^{-12} \) W K\(^{-1}\) (cf. Table [VII], much lower than for a single three-dimensional wire. Note that, instead of Al wire bonds, gold wire bonds can be used. These are characterized by a higher thermal conductivity because they remain normal conductive also at very low temperatures. However,

**TABLE VI. Magnetic field measurements of the materials used for the main components of the quantum socket.** The tested samples are significantly larger than any component used in the actual implementation of the three-dimensional wires and microwave package. The margins of error indicated in parentheses were estimated from the fluctuation of the magnetic sensor.

| Material  | \( ||\vec{B}|| \) (mG) |
|-----------|-------------------------|
| CW724R    | 0.21(5)                 |
| CW453K    | 0.25(5)                 |
| Al 5N5    | 0.02(5)                 |

**TABLE V. ZGC calibration.** The margins of error indicated in parentheses were estimated from the fluctuation of the magnetic sensor.

| Measurement                        | \( ||\vec{B}|| \) (mG) | \( \alpha \) (-) |
|-----------------------------------|------------------------|-----------------|
| Vertical position, background field | 554(20)                | -               |
| Vertical position, with ZGC       | 0.66(5)                | 842(34)         |
| Horizontal position, background field | 539(20)                | -               |
| Horizontal position, with ZGC     | 0.59(5)                | 917(44)         |
TABLE VII. Parameters used in the estimate of the heat transfer rate per kelvin difference for a three-dimensional wire and Al wire bond. In the table are reported: The hollow cylinder inner diameter \(d_i\); the hollow cylinder outer diameter and wire bond diameter \(d_o\); the hollow cylinder and wire bond cross-sectional area \(A\); the thermal conductivity \(k_i\); Conductor: Cond.; phosphor: Phos.

|                  | \(d_i\) (µm) | \(d_o\) (µm) | \(A\) (m²) | \(k_i\) (mW K⁻¹ m⁻¹) |
|------------------|-------------|-------------|-----------|---------------------|
| Inner cond.      | 290         | 380         | 4.74 × 10⁻⁸ | 3.7                 |
| (Phos bronze)    |             |             |           |                     |
| Outer cond.      | 870         | 1290        | 7.13 × 10⁻⁷ | 24.1                |
| (brass)          |             |             |           |                     |
| Wire bond        | -           | 50          | 1.96 × 10⁻⁹ | 0.01                |
| (Al)             |             |             |           |                     |

Al wire bonds remain the most common choice because easier to use.

Appendix D: THERMO-MECHANICAL TESTS

In this appendix, we discuss the performance of the springs used in three-dimensional wires at various temperatures. The three types of tested springs are called FE-113 225, FE-112 157, and FE-50 15 and their geometric characteristics are reported in Table VIII. We ran temperature cycle tests by dunking the springs repeatedly in liquid nitrogen and then in liquid helium without any load. At the end of each cycle, we attempted to compress them at room temperature. We found no noticeable changes in mechanical performance after many cooling cycles. Subsequently, the springs were tested mechanically by compressing them while submerged in liquid nitrogen or helium. The setup used for the compressive loading test of the springs is shown in Movie 4 of the Supplemental Material at [http://www.Supplemental-Material-Bejanin](http://www.Supplemental-Material-Bejanin), which also shows a properly functioning spring immediately after being cooled in liquid helium. In these tests, we only studied compression forces because in the actual experiments the three-dimensional wires are compressed and not elongated.

The compression force was assessed by means of loading the springs with a mass. The weight of the mass that fully compressed the spring determined the spring compression force \(F_c\). The compression force of each spring is reported in Table VIII. We observed through these tests that the compression force is nearly independent of the spring temperature, increasing only slightly when submerged in liquid helium. Assuming an operating compression \(\Delta L = 2.0\) mm, we expect a force between 0.5 N and 2.0 N for the inner conductor and between 2.0 N and 4.0 N for the outer conductor of a three-dimensional wire at a temperature of 10 mK. Note that we chose spring model FE-113 225 for use with the grounding washer.

Appendix E: ALIGNMENT ERRORS

In this appendix, we provide more details about alignment errors. Figure 14 shows a set of micro images for Au and Ag samples. The Au pads in panels (a) and (b) were mated two times at room temperature; the three-dimensional wires used to mate these pads featured the smaller tunnel (500 µm width). The pad dimensions were \(W_p = 230\) µm and \(T_p = 1000\) µm. Noticeably, in panel (a) the wire bottom interface matched the contact pad in both mating instances, even though the matching was affected by a rotational misalignment of approximately 15° with respect to the transmission line longitudinal axis. In panel (b) the inner conductor landed on the dielectric gap in the second mating instance.

In our initial design, a perfect match required that the die dimensions should be at most 1 thou smaller than the dimensions of the chip recess, as machined. In the case of the sample holder used to house the Au samples, the chip recess side lengths were 15.028(5) mm, 15.030(5) mm, 15.013(5) mm, and 15.026(5) mm. The Au samples were diced from a Si wafer using a dicing saw from DISCO, model DAD-2H/6, set to obtain a 15 mm × 15 mm die. Due to the saw inaccuracies, the actual die dimensions were 14.96(1) mm × 14.96(1) mm, significantly smaller than the chip recess dimensions. This caused the die to shift randomly between different mating instances, causing alignment errors.

As described in the main text, in order to minimize such errors a superior DISCO saw was used, in combination with a DISCO electroformed bond hub diamond blade model ZH05-SD 2000-N1-50-F E; this blade corresponds to a nominal kerf between 35 µm and 40 µm. Additionally, we used lateral markers spaced with increments of 10 µm that allowed us to cut dies with dimen-

TABLE VIII. Thermo-mechanical tests on hardened BeCu springs. In the table are reported: The outer diameter \(D\) of the coil forming the helix structure of the spring; the diameter \(d\) of the circular cross section of the spring (note that the smallest wire diameter is 150 µm); the spring free length \(L_f\), i.e., the spring length at its relaxed position; the number of coils \(N_c\); the spring force \(F_c\) (estimated at all operating temperatures).

| Spring type   | \(D\) (mm) | \(d\) (mm) | \(L_f\) (mm) | \(N_c\) | \(F_c\) (N) |
|---------------|-----------|-----------|-------------|--------|-------------|
| FE-113 225    | 2.30      | 0.26      | 11.55       | 11.25  | \(\sim 1.0\) |
| FE-112 157    | 1.30      | 0.22      | 18.00       | 42.00  | \(\sim 1.0\) |
| FE-50 15      | 0.60      | 0.15      | 31.75       | 150.00 | \(\sim 0.5\) |
In conclusion, it is worth commenting some of the features in Fig. 5 (d) in the main text. The figure clearly shows dragging of a three-dimensional wire due to cooling contractions. In fact, for the Al chip recess an estimate of the lateral contraction length from room temperature to \( \sim 4 \) K can be obtained as 
\[
\Delta L_{\text{Al}} = \alpha(4)L_{\text{Al}} \approx (4.15 \times 10^{-3})(15 \times 10^{-3} \text{ m}) \approx 62 \mu\text{m}, \]
where \( \alpha(4) \) is the integrated linear thermal expansion coefficient for Al 6061-T6 [79] at 4 K from Refs. [64] and \( L_{\text{Al}} \) is the room temperature length of the recess side [80]. Note that the sample holder is actually made from Al alloy 5N5; however, different Al alloys contract by approximately the same quantity. For the Si sample substrate, the lateral contraction length from room temperature to \( \sim 4 \) K is approximately given by 
\[
\Delta L_{\text{Si}} \approx 3.2 \mu\text{m}, \]
where the integrated linear thermal expansion coefficient at 4 K was found in Table 2 of Ref. [81]. Below 4 K, the thermal expansion of both materials is negligible for our purposes and, thus, the 4 K estimate can also be considered to be valid at \( \sim 10 \mathrm{mK} \).

Appendix F: SAMPLE FABRICATION

In this appendix, we outline the fabrication processes for the samples used to test the quantum socket. A set of samples was made by liftoff of a \( \sim 3 \mu\text{m} \) Ag film, which was grown by means of electron beam physical vapor deposition (EBPVD; from Intlvac Canada Inc., model Nanochrome II) on a 3 inch float-zone (FZ) Si (100) wafer of thickness 500 \( \mu\text{m} \). The superconducting samples were made by etching a \( \sim 120 \) nm Al film that was deposited by EBPVD on a 500 \( \mu\text{m} \) FZ Si wafer. Last, two sets of test samples were made by etching Au films of thickness 100 \( \mu\text{m} \) and 200 \( \mu\text{m} \) with a 10 \( \mu\text{m} \) Ti adhesion layer in both sets. The films were grown by EBPVD on a 3 inch Czochralski (CZ) undoped Si (100) wafer of thickness 500 \( \mu\text{m} \).

The 3 \( \mu\text{m} \) Ag samples were required to reduce the series resistance of the CPW transmission lines (cf. Subsecs. IV B, IV C, and IV D). Fabricating such a relatively thick film necessitated a more complex process as compared to that used for the Au and Al samples. The Ag samples were fabricated with a thick resist tone reversal process. The wafer was spun with an AZ P4620 positive tone resist to create a resist thickness of \( \sim 14 \mu\text{m} \), then soft baked for 4 min at 110 \( \circ\text{C} \). Because the resist layer is so thick, a rehydration step of 30 min was necessary before exposure. Optical exposure was performed for 30 s in a mask aligner from SUSS MicroTec AG, model MA6, in soft contact with a photomask. After exposure the sample was left resting for at least 3 h so that any nitrogen created by the exposure could dissipate. The tone reversal bake was done for 45 min in an oven set to 90 \( \circ\text{C} \), filled with ammonia gas. The sample then underwent a flood exposure for 60 s and was developed in AZ® 400K for 15 min. Subsequently, 3 \( \mu\text{m} \) of Ag was deposited and liftoff of the resist was performed in acetone for 5 min.

![Micro images showing three-dimensional wire alignment errors.](image-url)

**FIG. 17.** Micro images showing three-dimensional wire alignment errors. (a)-(b) Au pads. The pad displayed in (a) is connected to that in (b) by way of a CPW transmission line approximately 11.5 mm long. The die shifted upward between the first (green arrow (1)) and second (green arrow (2)) mating instance, resulting in a lateral misalignment for the bottom pad. The rotational misalignment for the pad in (a) is indicated by a dashed green line. (c) Successful alignment for six Ag pads on the same chip. (d) Peripheral area of an Ag sample (ground plane). The marks are due to contact with the grounding washer.
FIG. 18. Quantum socket microwave parameters. (a) Input impedance magnitude $|Z_{\text{in}}|$. (b) Input VSWR, $VSWR_{\text{in}}$. (c) Phase delay $\tau_\phi$. (d) Group delay $\tau_g$. Blue corresponds to the Au sample at room temperature (RT), red to the Au sample at 77 K, and orange to the Ag sample at room temperature.

with ultrasounds.

Appendix G: MICROWAVE PARAMETERS

In this appendix, we present a set of microwave parameters that help further analyze the performance of the quantum socket. These parameters were obtained from the measured S-parameter data of Figs. 9 and 10 (a) and are shown in Fig. 18. The complex input impedance can be obtained from the frequency dependent impedance matrix $Z = [Z_{mn}]$ as

$$Z_{\text{in}} = Z_{11} - \frac{Z_{12}Z_{21}}{Z_{22} - Z_L}, \quad \text{(G1)}$$

where $Z_L = Z_c = 50 \, \Omega$ is the load impedance. The impedance matrix was obtained using the measured complex $S$-parameter matrix $S = [S_{mn}]$ from

$$Z = \sqrt{Z_c} \left( \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} + S \right) \left( \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} - S \right)^{-1} \sqrt{Z_c}. \quad \text{(G2)}$$

The magnitude of $Z_{\text{in}}$ is shown in Fig. 18 (a).

The input voltage standing wave ratio (VSWR) was obtained from

$$VSWR_{\text{in}} = \frac{1 + |S_{11}|}{1 - |S_{11}|} \quad \text{(G3)}$$

and is displayed in Fig. 18 (b).

The phase delay was calculated as

$$\tau_\phi = -\frac{1}{2\pi} \angle S_{21} \quad \text{(G4)}$$

and is displayed Fig. 18 (c).

Finally, the group delay was obtained from

$$\tau_g = -\frac{1}{2\pi} \frac{\partial}{\partial f} (\angle S_{21}) \quad \text{(G5)}$$

and is displayed in Fig. 18 (d). The derivative in Eq. (G5) was evaluated numerically by means of central finite differences with 6th order accuracy. The data in Fig. 18 (d) were post-processed using 1% smoothing. Note that the output impedance and VSWR were also evaluated and resembled the corresponding input parameters.

The input and output impedances as well as the VSWRs indicate a good impedance matching up to approximately 8 GHz. The phase and group delays, which are directly related to the frequency dispersion associated with the quantum socket, indicate minimal dispersion. This is expected for a combination of coaxial structures (the three-dimensional wires) and a CPW transmission line. Thus, we expect wideband control pulses to be transmitted without significant distortion in applications with superconducting qubits (cf. Supplemental Material at http://www.Supplemental-Material-Bejanin for further details about microwave pulse transmission).
Appendix H: DILUTION REFRIGERATOR SETUP

The experimental setup used to measure the superconducting CPW resonators is shown in Fig. 19. The low-temperature system is a cryogen-free DR from BlueFors Cryogenics Ltd., model BF-LD250. The DR comprises five main temperature stages, where microwave components and samples can be thermally anchored: The RT, 50K, 3K, still (\sim 800 mK), cold plate (CP; \sim 50 mK), and MC stage. We will describe the setup following the input signal through the various temperature stages, from port 1 to the input port of the microwave package (where the resonator sample is mounted) and from the output port of the package to port 2. The two ports are connected to the PNA-X, which serves as both the microwave source and readout apparatus. Port 1 is connected to the RT stage of the DR with SucoFlex flexible cables followed by a series of two semi-rigid coaxial cables from EZ Form, model EZ 86-Cu-TP/M17 (each approximately 1.2 m long, with silver-coated copper center conductor, solid PTFE dielectric, and tin-plated seamless copper outer conductor). Except for the PNA-X ports, which feature 3.5 mm connectors, all the connectors and bulkhead adapters are SMA type. In particular, the RT stage of the DR features a set of hermetic SMA bulkhead adapters from Huber+Suhner, model 34_SMA-50-0-3/111_N, with a tested leak rate for helium-4 lower than 1 \times 10^{-9} mbar ls^{-1}.

The DR stages, all the way to the MC stage, are connected by the series of five semi-rigid coaxial cables from Coax Co., Ltd., model SC-219/50-SS-SS (with stainless steel (SUS304) center and outer conductor and solid PTFE dielectric; the cable lengths from RT to MC are: 39.6 cm, 48.0 cm, 39.9 cm, 27.4 cm, and 20.0 cm, respectively). The cables are thermalized to the DR stages by way of cryogenic attenuators from the XMA Corporation-Omni Spectra\textsuperscript{®}, model 2082-6418-XX-CRYO, where XX is the attenuation level in dB; for each stage between RT and MC, we chose XX = 03, 06, 06, 20, and 20, respectively. The input signals are filtered by means of a low-pass filter from Marki Microwave, Inc., model FLP-0960-2S, with bandpass from DC to 9.6 GHz. The filter is heat sunk at the MC stage by anchoring it to a hardware module, which is bolted to the MC stage. The filter module, and similarly all the other modules used to heat sink microwave components in the DR, are made from C10100 OFE copper alloy.

A non-magnetic semi-rigid coaxial cable EZ 86-Cu-TP/M17 connects the output port of the Marki filter to an SMP 086 connector on the mounting plate: the cable is 18 cm long and enters the A4K shield through one of the chimneys on the shield lid. The shield, which is thermalized to the MC stage, is characterized by a DC relative permeability close to 80000 at 4 K. The SMP 086 connector is mated to the input port of the DUT shown schematically in Fig. 18. The DUT used in the DR features SMP 047 connectors in lieu of SMA connectors.

The DUT when connected to the mounting plate is shown in Fig. 18(d) and Fig. 18(c).

The output port of the DUT is then connected to a series of two cryogenic circulators from Raditek Inc., model RADC-4.0-8.0-Cryo-4-77K-S3-1WR-b (with CryoPerm magnetic shielding) by means of a semi-rigid superconducting coaxial cable from Coax Co., model SC-219/50-Nb-Nb, of length 17.3 cm. The circulators are thermalized to the MC stage and are connected to each other by means of a semi-rigid superconducting coaxial cable from Coax Co., model SC-219/50-Nb-Nb, of length 20.7 cm; the spare port of each circulator is terminated with an XMA cryogenic 50 \Omega load, model 2001-7010-02-CRYO, which is thermalized to the MC stage. The output port of the second circulator is connected by way of a 51.9 cm long SC-219/50-Nb-Nb cable to a third circulator at the still stage (the spare port is terminated with a 50 \Omega load thermalized to the still). A 42.7 cm long SC-219/50-Nb-Nb cable connects the output port of the
third circulator to a cryogenic microwave amplifier from Low Noise Factory AB, model LNF-LNC1_12A. The amplifier, which is thermalized to the 3K stage, is characterized by a nominal gain of approximately 39 dB and a noise temperature of 5 K at an operating temperature of 12 K in the 4 GHz to 8 GHz frequency range. Finally, the amplifier output port is connected to the 50 K and RF stages by a series of two SC-219/50-SS-SS cables of length 38.6 cm and 31.2 cm, respectively; the cables are thermalized to the 50 K stage by means of a 1 dB XMA attenuator. Two EZ Form copper cables in series, followed by SucoFlex flexible cables, complete the network to port 2.

The input channel described here is one of three equivalent channels dedicated to resonator measurements. The three channels share the output line; this is possible thanks to a microwave switch from Radiall, model R573.423.605, which is operated at the MC stage. The switch is located after the DUT but before the two MC circulators (two of the three input channels and the switch are not shown in Fig. 19). The switch has six inputs and one output, making it possible to further extend the number of input microwave channels.

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Even though state-of-the-art bonding machines can significantly mitigate these issues. [51]

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S1: INTRODUCTION

This Supplemental Material is organized as follows. In Sec. [H] we show a set of simulated electric field animations. In Sec. [H] we characterize the microwave anomaly due to the screw-in micro connector. In Sec. [H] we discuss in detail the geometry of the coupling region between a CPW transmission line and a superconducting resonator; additionally, we show the fit required to extract the internal quality factor of the resonators. In Sec. [H] we present a movie of the cryogenic spring tests. In Sec. [H] we propose a surface code architecture that makes use of two readout resonators per qubit. Finally, in Sec. [H] we present the quantum socket behavior when fast microwave pulses are applied.

S2: ANIMATED ELECTRIC FIELD SIMULATIONS

The electric fields discussed in Subsec. II D of the main text were generated for multiple phases, enabling a time-domain analysis. This made it possible to better determine the behavior of the simulated fields associated with the various components of the quantum socket. The time-domain animations of the simulated electric field for the three-dimensional wire, the 90° transition between the wire and the on-chip pad, and the first box mode are shown in Movies 1, 2, and 3, respectively.

The simulation of the three-dimensional wire shows a clear impact to the electric field at the dielectric spacers, giving an indication of where potential future improvements of the wire should focus.

The simulation of the 90° transition reveals a surprisingly clean transmission, with no immediately apparent regions of poor performance. The broad field distribution below the contact pad does suggest the appearance of a stray capacitance to the cavity below. However, the TDR results in Subsec. IV C indicate that such a capacitance must be small because of a very good impedance matching at the transition region.

The box mode animation shows the “pinching” effect to the electric field caused by the metallic pillar, leading to a significantly higher relative permittivity and, in turn, a much lower frequency of the first box mode (~ 6.3 GHz). Some other regions of interest in Movie 3 are the outer edges of the chip recess, where the field becomes fully confined within the substrate. As the magnitude of the field in this region is quite low, this effect should have only a marginal impact on the performance of the quantum socket. The animation also reveals some field interaction between the box mode and the contact pads (which are characterized by a relatively large area), suggesting these as the main reason for any spurious coupling between on-chip structures and box modes.

S3: SCREW-IN MICRO CONNECTOR ANOMALY

In order to gain further insight into the electrical behavior of the screw-in micro connector, we report here a set of room temperature measurements showing the appearance of a microwave anomaly associated with the micro connector. These measurements complement the discussion associated with Fig. 9 (b) in Subsec. IV B of the main text.

Figure [S1] shows the magnitude and unwrapped phase angle of the S-parameters as a function of frequency for an Au sample in the case of a slightly loose screw-in micro connector; the measurement was performed at room temperature (cf. Subsec. IV B of the main text for details on the DUT used for the measurements). The microwave dip is centered at approximately 6 GHz and has a 3 dB bandwidth of approximately 400 MHz. The dip is likely not a Lorentzian-type feature due to a resonance mode in the package. This is clearly demonstrated by the phase angle of the coefficients $S_{21}$ and $S_{12}$, which has the characteristic frequency dependence of a transmission line (i.e., no phase shift associated with a resonance). Note that a similar behavior is encountered when performing a microwave measurement with, e.g., a not
well torqued SMA connector. As expected from energy conservation, the dip in $S_{21}$ corresponds to a peak in $S_{11}$; however, the absence of a peak in $S_{22}$ indicates that only the micro connector at the DUT input line was loose in this instance. As explained in the main text, curing the dip at room temperature is rather straightforward. However, it is much harder at low temperatures. Hence, we decided to cool down a DUT without curing the dip that appeared at room temperature. A set of data at 77 K was taken immediately after the room temperature data, as shown in Fig. 9 (b) in Subsec. IV B of the main text. We monitored the S-parameters throughout the cooldown, observing how the dip shifted from approximately 6 GHz to 2 GHz while cooling. It is reasonable to assume that, when cooling down, the micro connector became slightly more loose due to thermal contractions, thus giving rise to a microwave transmission dip at lower frequency.

**S4: SUPERCONDUCTING RESONATORS COUPLING AND FIT**

Figure S2 shows a detail of the coupling region between one of the CPW transmission lines and a $\lambda/4$-wave resonator shown in Fig. 14 of the main text. The width and gap of the CPW transmission line are indicated. The resonator center conductor width $W$ and dielectric gap $G$ are also indicated, as well as the coupling length $\ell_k$ and the line-resonator ground separation (5 μm). The length $\ell_k$ determines how strongly the resonator is coupled to the transmission line and, thus, the resonator external quality factor $Q_e$.

Figure S3 shows a polar plot of the real and imaginary part of the normalized inverse transmission coefficient $\tilde{S}^{-1}_{21}$ of the data shown in Fig. 15 (d) of the main text, along with the fit. The equation used for the fit is

$$\tilde{S}^{-1}_{21} = 1 + \frac{Q_i}{Q_e^*} \frac{1}{1 + i2Q_i \delta x} ,$$

where $\phi$ is an offset angle, $\delta x = (f - f_0)/f_0$, and $i = \sqrt{-1}$.

A normalization is applied before the fit to set the off-resonance transmission magnitude and phase to 0 dB and 0 rad, respectively. The fit parameters for the resonator in Fig. 15 (d) of the main text were found to be $f_0 = 5064513933(6)$ Hz, $Q_i = 165790(60)$, $Q_e^* = 16002(4)$, and $\phi = -0.0347(3)$.

**S5: SPRING TESTS**

As discussed in Appendix D of the main text, Movie 4 shows the setup used to test the springs at low temperature. In the movie, two springs mounted in series are compressed, after having been submerged in liquid helium. This process was repeated multiple times, without any damage occurring to the spring or any measurable change in the spring constant. The same setup also made it possible to perform compression measurements while the springs were submerged in a cryogenic liquid (nitrogen or helium); the compressive force was applied at the top of the rod, which always remained at room temperature.

**S6: QUANTUM SOCKET SURFACE CODE**

Figure S4 shows a more general version of the surface code architecture in Fig. 16 of the main text. In panel (a), numbers from 0 to 5 represent arbitrary frequencies from low to high (0 means a lower frequency than the others). Every qubit is coupled to two measurement resonators; note that label 0 is associated with a CPW transmission line that is coupled to a set of four measurement resonators, all at slightly different frequencies (to allow multiplexing) centered around frequency 0. Similarly, label 5 is associated with a CPW transmission line that is
FIG. S4. Generalized surface code architecture compatible with the quantum socket. (a) The main difference compared to the architecture presented in the main text is the addition of an extra measurement resonator for each qubit. In this case, the qubits are named \textit{octaton} due to their eight arms. The various frequencies from low to high are indicated by the numbers 0, 1, 2, 3, 4, and 5. The CZ gates follow the same numeration \cite{S3}. Measurement qubits are indicated in red and blue and data qubits in black. (b) Extended two-dimensional lattice.

coupled to a set of four measurement resonators, all at slightly different frequencies centered around frequency 5. In this architecture, all qubits start at a low frequency then increase in frequency in unison to perform CZ gates through the coupling resonators in the correct sequence; in the figure, this sequence is indicated by the labels (coupling frequencies) 1, 2, 3, and 4. Finally, the measurement qubits (red and blue) are read out at frequency 5. This is one surface code cycle \cite{S3}. The process is then reversed and during the downward uniform frequency sweep again an appropriate sequence of CZ interactions is executed, followed by readout at frequency 0, implementing the next cycle. This process avoids sweeping either measurement or data qubits past resonators during the cycles. Panel (b) shows an extended portion of the surface code lattice.

S7: MICROWAVE PULSE TRANSMISSION

In Appendix G of the main text, we have shown that the quantum socket is characterized by a small frequency dispersion. In this section, we describe a set of experiments where actual fast microwave pulses were applied to the quantum socket as well as a reference cable. This makes it possible to assess the effects of dispersion directly on pulses similar to those that will be used for the manipulation of superconducting qubits.

Figure S5 shows the magnitude of the Fourier transform of a pulse transmitted through the reference cable (panel (a)) and the quantum socket (panel (b)), both at room temperature. The pulse was generated by mixing a sinusoidal carrier signal at 4.5 GHz with a Gaussian-modulated sinusoidal pulse at 200 MHz. The time length of the Gaussian envelope was 15 ns (full width at half maximum (FWHM)). The carrier signal was generated by means of a microwave source from Keysight, model E8257D PSG; the mixer was an in-phase and quadrature (IQ) mixer from Marki, model IQ-0307LXP; the modulated Gaussian was generated by means of a customized arbitrary waveform generator (AWG) from Tabor Electronics Ltd., model WX2184C+; all instruments were synchronized by way of a rubidium atomic timebase embedded within a digital delay generator from Stanford Research Systems, Inc., model DG645/15, which was also used to trigger the AWG through an SRD1 module from Stanford Research Systems. The generated signal was split with a microwave power divider from Krytar, Inc., model 6005180, with one output sent through a reference SucoFlex flexible coaxial cable from Huber+Suhner of length 1.5 m and the other output through the quantum socket (DUT of Fig. 8 of the main text). The output of each path was acquired and digitized using a real-time oscilloscope from Keysight, model DSO91204A, also synchronized with the rubidium timebase. The pulse going through the quantum socket is attenuated due to the resistance of the Ag CPW transmission line, hence, the magnitude of the Fourier transform is lower than of the reference signal. However, the overall shape of the two pulses is very similar, with marginal distortions.
FIG. S5. Magnitude of a Fourier-transformed signal. (a) Pulse transmitted through a reference flexible coaxial cable. (b) Pulse transmitted through the quantum socket.

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