A TOCTOU Attack on DICE Attestation

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ABSTRACT

A major security challenge for modern Internet of Things (IoT) deployments is to ensure that the devices run legitimate firmware free from malware. This challenge can be addressed through a security primitive called attestation which allows a remote backend to verify the firmware integrity of the devices it manages. In order to accelerate broad attestation adoption in the IoT domain the Trusted Computing Group (TCG) has introduced the Device Identifier Composition Engine (DICE) series of specifications. DICE is a hardware-software architecture for constrained, e.g., microcontroller-based IoT devices where the firmware is divided into successively executed layers.

In this paper, we demonstrate a remote Time-Of-Check Time-Of-Use (TOCTOU) attack on DICE-based attestation. We demonstrate that it is possible to install persistent malware in the flash memory of a constrained microcontroller that cannot be detected through DICE-based attestation. The main idea of our attack is to install malware during runtime of application logic in the top firmware layer. The malware reads the valid attestation key and stores it on the device's flash memory. After reboot, the malware uses the previously stored key for all subsequent attestations to the backend. We conduct the installation of malware and copying of the key through Return-Oriented Programming (ROP). As a platform for our demonstration we use the Cortex-M-based nRF52840 microcontroller. We provide a discussion of several possible countermeasures which can mitigate the shortcomings of the DICE specifications.

CCS CONCEPTS

• Security and privacy → Embedded systems security.

KEYWORDS

Attestation, DICE, TOCTOU, IoT, Trusted computing, TCG, ROP, Malware

1 INTRODUCTION

IoT deployments often incorporate many physically distributed, constrained (e.g., microcontroller-based) devices having minimal or even no security features due to cost reasons. At the same time, the devices have identical software stacks and configurations which allows scalable attacks to be developed once a vulnerability is discovered by an attacker. These properties make IoT deployments an attractive target for remote software attacks such as malware infections as demonstrated in [43, 52, 66]. Once malware is installed on an IoT device it may serve a variety of an attacker’s goals such as to provide wrong application data to the IoT backend or to use the device as a bot in Distributed Denial of Service (DDoS) attacks, e.g., as in the Mirai attack [43].

Malware can be detected through a security primitive called remote attestation, which has been excessively studied in the IoT domain (see [17, 30, 57] for an overview), and standardized by the TCG in the DICE series of specifications [60, 61, 63, 64]. In a nutshell, attestation consists of 1) a method to securely calculate a fingerprint of a device’s software stack and 2) a secure protocol conveying the fingerprint to a remote verifier that can evaluate the fingerprint. If the expected and the received fingerprints differ, the verifier may assume the device is running untrusted, potentially malicious firmware.

In contrast to TCG’s series of attestation specifications using a dedicated security chip called Trusted Platform Module (TPM) [62], DICE is mainly intended to be used in so-called deeply embedded systems. Deeply embedded systems are embedded systems relying on constrained 8-, 16- or 32-bit microcontrollers running application software on top of a simple Real-Time Operating System (RTOS) or bare metal (without an Operating System (OS)). Due to its low hardware requirements, DICE is more suitable than a TPM for this class of devices. In this paper, we concentrate on microcontroller-based deeply embedded systems. More powerful devices, e.g., running Linux or Windows are out of scope.

DICE is a hardware-software architecture supplementing the boot process of a microcontroller. The firmware a DICE-based device is separated into successively executed layers. DICE provides measured boot through all firmware layers where in the top layer an attestation key depending on the measurements of all layers and a Unique Device Secret (UDS) is used in an attestation protocol with a backend. If malware exists in some of the firmware layers the attestation key will be different and the protocol will fail. In this way, DICE can detect malware that is present on the device when the device boots.

In this paper, we demonstrate a TOCTOU attack on DICE-based attestation. We show that, DICE cannot detect malware installed at runtime which is capable of storing the valid attestation key in the flash memory of the microcontroller and reuse it across boot cycles for attestation instead of the newly derived key. We consider
such malware capabilities as realistic and therefore we believe that attacks of this type are likely to happen in real IoT deployments.

Previous work in the area of TOCTOU attacks on attestation has either considered high-end TPM-based Linux devices [21] or discuss TOCTOU countermeasures [46]. To the best of our knowledge we present the first attack on the standardized DICE attestation architecture for deeply embedded systems.

Our attack is conducted through ROP which is a control hijacking attack. Therefore, the requirements for our attack are the same as the requirements for ROP namely: 1) a memory corruption vulnerability and 2) attacker’s knowledge of the devices’ binary image.

Memory corruption vulnerabilities are found often in embedded software as recently demonstrated in [4, 42]. Such attacks are common for software written in system languages lacking memory safety such as C and C++ [58]. Recent research [15] has shown that even well-known protections such as Address-Space Layout Randomization (ASLR), Data Execution Prevention (DEP), and Stack Smashing Protection (SSP) are almost completely absent in deeply embedded systems.

An attacker can gain a copy of the firmware binary running on a fleet of IoT devices with the same software stack, e.g., by capturing or buying a single device and conducting a physical attack on its debug interfaces as shown, e.g., in [40]. The firmware is required for identifying ROP gadgets, as well as for acquiring knowledge about the stack frame and the location of the attestation key in memory. Once the attacker has access to the binary she can develop the remote ROP attack described in this paper and use it against all devices belonging to a given fleet running the same software stack.

For our proof of concept implementation, we selected the Cortex-M architecture since Cortex-M is the de facto standard architecture used by all major semiconductor vendors for low-cost IoT System on Chips (SoCs) and microcontrollers. The differences between the various Cortex-M variants are insignificant for the described attack since we use a subset of instructions available on all of them. In summary, our contributions are:

- We show a remote attack procedure abstracted from any specific IoT end-device capable to undermine DICE-based attestation. Once DICE is circumvented the attacker can reuse the same technique to install useful for him malware, e.g., using the device for DDoS attacks.
- We provide a detailed proof of concept implementation of the attack on a Cortex-M4 based nRF52840 Bluetooth Low Energy (BLE) microcontroller using an artificial memory corruption bug (a buffer overflow). We demonstrate the remote nature of the attack by conducting it in a realistic IPv6 over BLE IoT network [45].
- We propose practical countermeasures such as firmware updates, secure boot, and introducing additional inputs in the attestation key derivation.

2 BACKGROUND

This section provides background information required for understanding the rest of the paper. Additionally, we provide discussion of the related work regarding IoT attestation and TOCTOU attacks in Section 7.

2.1 Control Hijacking Attacks and Countermeasures for Deeply Embedded Systems

In this paper, we use ROP for conducting our attack which is a form of a control hijacking attack. In the following, we review the state of the art of control hijacking attacks and the most common countermeasures against them with a focus on deeply embedded systems. Our goal is to show that these attacks are and will remain a serious threat for deeply embedded systems.

Control hijacking attacks on deeply embedded systems were shown for a variety of microcontroller architectures. One of the earliest works in this area is [29] where a ROP attack is used to install persistent malware in the memory of an Atmel’s AVR microcontroller. In [49] the same architecture was attacked again with ROP. However, here the authors consider the attack in a broader context demonstrating a worm capable to propagate to neighbor nodes in the network. The installation of persistent malware through ROP was demonstrated as well on Cortex-M devices [66]. ROP attacks were presented as well on the currently gaining momentum in the microcontroller market RISC-V architecture [31, 37].

Deeply embedded systems run most often software written in C and C++ either without an OS (bare metal) or on top of RTOS. Such setups almost always lack virtual memory as well as memory separation between tasks and separation between user- and kernel space, as shown in a recent survey conducted with 42 embedded OSs [15]. The lack of those features allows memory corruption bugs to become a root for exploitable vulnerabilities.

Many countermeasures were developed against exploits permitted by memory corruption bugs. Some of the most known are, e.g., Control-Flow Integrity (CFI) [14], shadow stack [23], ASLR [8], DEP [3] and SSP [12].

CFI seeks to restrict control-flow transitions in a program to the set of strictly required transitions for the program’s correct execution. Unfortunately, CFI relies on process isolation and fine-grained memory protection. Without these features, CFI cannot provide any security guarantees [65]. Even if recent research efforts [22, 39, 47, 65] aim to provide CFI for deeply embedded systems CFI is not yet broadly adopted.

Shadow stack techniques compare a protected copy of subroutines’ return address against the return addresses on the stack [23]. In this way manipulations of the return addresses, e.g., as used by ROP are detected. However, shadow stacks require some form of memory protection.

ASLR is a technique that prevents attackers to use the same gadgets on different instantiation of the same program containing the same bug. This is achieved by randomizing the offsets of program segments (e.g. code and data). ASLR is not suitable for microcontrollers because it requires virtual memory and an Memory Management Unit (MMU) [15].

DEP counters code injection attacks by making data memory not executable and code memory not writable by using a Memory Protection Unit (MPU) or an MMU. However, DEP cannot stop control flow attacks such as ROP. Moreover, DEP is infeasible for many microcontrollers lacking even a simple MPU.

SSP detects buffer overflows by placing a random value (called cookie or canary) between the return address and local buffers.
on the stack. Before a function returns the value of the cookies is checked in order to determine if a buffer has overflowed and change it. SSP provides relatively weak protection since it only can detect a small subset of special errors namely return address pointers valuations [58] and therefore cannot stop code reuse attacks such as ROP.

A recent survey [15] presents an evolution of the adoption of ASLR, DEP, and SSP in 42 embedded OSs, where 20 of the OSs are specially intended for deeply embedded systems. The authors conclude that those features are broadly available only on high-end OSs. From all 20 deeply embedded OSs three support DEP, one supports SSP, and none supports ASLR.

2.2 ARM Cortex-M Processors

In this section, we introduce some details of the Cortex-M architecture that are relevant for our attack. Cortex-M CPUs have 13 general-purpose registers (r0 – r12), a stack pointer register (sp), a link register (lr) and the program counter register (pc) [68]. Further, every Cortex-M processor also has special registers, which contain information about the processor status and define operation states and interrupt/exception masking. A special register in all Cortex-M variants is the PRIMASK register. It is used for exception and interrupt masking. It is 1-bit wide and blocks all exceptions and interrupts, when set. Special registers are not memory mapped and can only be accessed with certain special register access instructions. Instructions to modify the PRIMASK value are cpsie i (sets PRIMASK) for enabling exceptions and interrupts and cpsid i (clears PRIMASK) for disabling them [68].

A key memory section for the processor to operate is the stack memory. It is used for temporary storage of register data, local variables, and function parameters. To store and retrieve data from the stack, ARM processors provide the push and pop instruction. The current stack pointer is incremented (push) and decremented (pop) automatically after each execution of these instructions. This non-intuitive increment and decrement of the stack pointer is done because the stack grows from a high memory address (usually the top of the SRAM region) to a lower address [68].

2.3 Return Oriented Programming

ROP attacks use short code snippets that are already present in the code and link them in an order allowing arbitrary programs to be executed. These short code snippets are called gadgets. Gadgets consist of a small instruction sequence ending with a return instruction. The return instruction is used to chain multiple gadgets together. Each gadget performs a specific computation task (load, store, arithmetic operations, etc.), so that the combination of gadgets creates arbitrary programs which the attacker can execute. To perform ROP, the attacker exploits a buffer overflow in order to place addresses and other values on the stack memory. These addresses point to certain gadgets, which can use other stack-placed values as parameters for computation [66].

In general, ARM Cortex-M systems use push, pop, and branch instructions for control flow mechanisms. The push instruction is used by subroutines to store register values on the stack, including the return address held in the link register. When returning, either a branch instruction, e.g., bx or a pop instruction is executed. A push instruction is usually called at the end of subroutines to restore previously pushed registers including the return address from the stack. Figure 1 shows this procedure. In Figure 1 the return address is popped into the program counter register, which causes the processor to continue with the program code specified by the return address. This mechanism allows an attacker to exploit pop instructions to return to the address of a certain gadget, which ideally also includes a pop instruction in order to return to the next gadget. This assumes that, by buffer overflow, the attacker has previously placed appropriate address values on the stack [66].

2.4 Implicit Identity Based Device Attestation with DICE

Several variants of DICE attestation exist [61, 63, 64], where the differences are mainly in the number of software layers, the key derivations, and attestation protocols. Our attack is conducted on the top firmware layer and therefore it is applicable to all of them. In the top firmware layer commonly resides the application logic of the device. We base the following descriptions on the specification Implicit Identity Based Device Attestation [61]. This architecture consists of three layers — the boot layer placed in ROM, the RIOT layer responsible for attestation key and certificate derivation, and the application layer. The RIOT layer receives a secret depending on its measurement and UDS. From this secret, it derives deterministically two asymmetric key pairs, one that is exclusive to the RIOT layer and depends only on the secret called DeviceID and one depending on the secret and the measurement of the application layer called alias key. The alias public key is certified with the DeviceID. Only the alias key and certificate are provided to the application layer for use in an attestation protocol with the backend.

3 ASSUMPTIONS

For our attack we make the following assumptions:

_The attacker can gain access to the firmware image_. We assume that the attacker can gain access to the firmware image, e.g., by conducting a physical attack on a captured (e.g., bought) device. For
this, an image saved in external flash can be dumped or the readback protection of the microcontroller can be circumvented. Attacks of the latter type are feasible since they were often demonstrated in the past, e.g., through glitching the debug interfaces [5, 13] or using UV-light [48]. A comprehensive summary of attacks targeting debug interfaces is given in [40].

A fleet of IoT devices runs the same firmware. We consider a typical IoT scenario where many physically distributed DICE-enabled devices run the same firmware stack. Once the attacker has developed and tested the attack on one captured device he can remotely conduct the attack on all devices of the fleet that run the same firmware. The goal of the attacker is to infect all devices running the same firmware and not the captured device.

The firmware contains an exploitable memory corruption bug. The firmware needs to provide an exploitable memory corruption bug, e.g., a buffer overflow vulnerability, which can be detected, e.g., by using techniques outlined in [4, 51]. Note that such vulnerabilities are common for embedded firmware written in system languages such as C/C++ [58], and were also often demonstrated in the past, e.g., [4, 42].

The firmware contains the necessary gadgets. The firmware has to contain suitable gadgets for the ROP attack. However, this is not a limiting requirement since our attack requires only two very simple gadgets.

The attacker can gain knowledge of the stack frame structure. For conducting a ROP attack the attacker needs to gain knowledge about the stack frames. This information can be retrieved by flashing a captured device with the dumped image and using a debugger to examine the stack when a memory corruption is triggered.

The attacker can gain knowledge of the credentials’ locations in memory. The memory locations of the attestation key and certificate need to be determined. This can be done by dumping the RAM when the top firmware layer is executed and finding the areas with high entropy.

Some functionality of the original firmware are still useful for the attacker. We assume also that parts of the original firmware, e.g., the network stack, the attestation protocol, etc. are still useful for the attacker.

4 ATTACK METHOD

The goal of an attacker is to persist code on the devices’ flash memory that serves his purposes, e.g., code that will turn the devices of a given fleet into bots executing DDoS attacks. This code, henceforth called useful malware, should stay undetected by DICE attestation. In order to circumvent DICE we additionally install a small utility malware. Both the useful and the utility malware are installed by exploiting a memory corruption bug through ROP. The main idea is that the utility malware saves ones persistently the valid attestation credentials and then causes at every new reboot that they are used for attestation with the backend.

We install the utility malware first before installing the useful malware. It consists of two routines ram2flash_copy() and flash2ram_copy(). ram2flash_copy() is executed only one single time just after installing the utility malware. It copies the valid alias private key and alias certificate from RAM to flash. After that, ram2flash_copy() modifies the original firmware, e.g., some initialization function in the original firmware in order to cause an execution jump to flash2ram_copy() every time the system boots. Then, at every subsequent boot, the flash2ram_copy() overwrites the freshly calculated alias key and alias certificate with the previously saved old ones and jumps back to the regular firmware execution. This hides the modification of the device’s firmware to any future attestation requests by the DICE backend. After that, the attacker exploits the same vulnerability for the second time in order to install the useful malware.

We divide our attack into five consecutive steps: 1) disabling interrupts, 2) installing utility malware to flash memory, 3) ram2flash_copy() execution, 4) flash2ram_copy() execution, and 5) installing useful malware to flash memory. These steps are explained in the following considering ideal gadgets. In Section 5 we demonstrate how the same functionality is achieved with real gadgets easily found in firmware images.

Step 1: Disabling interrupts. As the attack is performed on a real-time microcontroller, first all interrupts need to be disabled. This prevents the ROP procedure and afterward the utility malware execution from being interrupted and experiencing unexpected behavior. To disable interrupts a gadget is used. This gadget needs to globally disable interrupts by means of a cpsid i instruction and afterward pop a new address value from the stack into the program counter to jump to the next gadget. An ideal gadget of this type is shown in Listing 1. To execute this gadget at the beginning of the ROP attack, the attacker has to replace the return address of the original stack frame with the 32-bit address of the gadget, followed by the address of the next gadget.

```assembly
cpsid i
pop (pc)
```

Listing 1: Ideal gadget to disable global interrupts (interrupt gadget)

Step 2: Installing utility malware to flash memory. To write to memory (and registers) with ROP, one single store gadget is sufficient. An ideal gadget of this type is shown in Listing 2. The first line stores a 32-bit value contained in register rA to a memory address contained in register rB. The second line gets new values for registers rA, rB and pc from the stack for the next execution of the store operation. Before the first execution of this gadget, execution of only the second gadget line is necessary to load the first values into the registers.

```assembly
str rA, [rB, #0]
pop (rA, rB, pc)
```

Listing 2: Ideal gadget to write values to memory (store gadget)

To install the utility malware to flash memory the malware binary has to be split up into pieces of 32 bits. A 32-bit malware piece, a flash destination address, and the address of the first gadget line build an exploit data block of 96 bits, which is placed on the stack
through a buffer overflow. The second gadget line pops the 32-bit malware pieces into register rA, the flash memory address into register rB, and the gadget address into the program counter register. This causes the next gadget call to store the malware pieces to the specified flash memory address.

After writing the utility malware to the flash memory, it is necessary to jump to ram2flash_copy() to start executing it. Therefore, as the last part of the binary exploit, two 32-bit dummy values (pop into rA and rB) and the address of ram2flash_copy() (pop into pc) have to be appended.

Figure 2 shows the stack content required for installing the utility malware when the ideal gadgets from Listing 1 and Listing 2 are used. The left column shows which elements in the stack are overwritten by the exploit data through the buffer overflow. The middle column shows the exploit data. The right column shows in which registers the exploit data is popped during the ROP procedure.

Note that usually, flash memory of a microcontroller needs to be configured before being able to write to it. As this is a device-specific task, this is not considered here. It will be explained in Section 5.

Step 3: ram2flash_copy() execution. The function ram2flash_copy() first needs to copy the private alias key and the alias certificate from RAM to flash memory. This procedure preserves the current values in order to be used for future attestations. Listing 3 shows an example for that part of ram2flash_copy() where key and certificate are assumed to be adjacent for simplicity. ram2flash_copy() loads the RAM start address of the memory block holding key and certificate into register rA and the flash destination address into register rB. Then, it loads the word from the RAM address in register rA into register rC. Afterwards, it stores the word to the flash address in register rB. To get the next addresses, it increments both addresses in registers rA and rB by four bytes. These steps are repeated until the combined length of the private key and certificate is reached and both key and certificate have been completely copied.

Once key and certificate are copied ram2flash_copy() modifies the original firmware such that it jumps to flash2ram_copy() at every system boot. It is important that the modified original firmware calls flash2ram_copy() after the generation of the new attestation key and certificate, thus they get overwritten. A suitable firmware function to modify can be some initialization function, which is called on every application start. When modifying such a function, it is required that the modified function’s functionality remains unchanged. Otherwise, arbitrary unexpected behavior might occur.

After modifying the original firmware the device needs to be reset or reinitialized. This is required because due to the buffer overflow the stack memory is corrupted and the regular operation of the device cannot continue. A reset can be triggered on many microcontroller architectures by writing into a special soft-reset register. For example, the Cortex-M devices provide Interrupt and Reset Control Register (AIRCR) for that purpose. Alternatively, a jump to the RAM initialization routine in the startup code can reinitialize the device.

Step 4: flash2ram_copy() execution. After reset/re-initialization, the modified original firmware jumps to flash2ram_copy(). flash2ram_copy() takes the saved values for alias private key and alias certificate from flash memory and overwrites the freshly calculated values in RAM. For this, the routine from Listing 3 can be used again. It is only necessary to swap the address values of registers rA and rB in the beginning. Additionally, flash2ram_copy() has to jump back to the original program flow of the firmware. For this, it has to be made sure that potential return values of the original function are returned. To jump back, the flash2ram_copy() can for example use a bx lr instruction, as the link register, which contains the return address, does not get changed during overwriting the key and certificate. Another possibility would be, in case the link register was pushed to the stack by the modified initialization function, to use a pop pc instruction.

Step 5: Installing useful malware. Now that the DICE attestation mechanism is bypassed, the attacker can again load malware to the device’s flash memory undetected by the attestation process. For this, the attacker exploits the same buffer overflow as before. He again uses ROP to disable interrupts, writes the malware to the flash, modifies the original firmware at a suitable location to be able to jump to the useful malware, and resets the device. If the malware needs a large amount of memory which may not fit in the stack memory, the attacker can split up the malware and repeat this procedure multiple times.
5 PROOF OF CONCEPT IMPLEMENTATION

In this section, we describe how we implemented the attack on our target device.

5.1 Target Device - nRF52840

We used the nRF52840 BLE microcontroller as a target for the attack. It is based on a 64 MHz ARM Cortex-M4 processor. It has 1 MB of flash memory and 256 KB RAM. The flash memory is divided in 256 pages of 4 KB each.

To protect the flash memory from non-authorized access nRF52840 features an Access Control List (ACL). The ACL assigns and enforces access permissions to different regions of the on-chip flash memory map. The ACL protection can be activated at runtime and remains active until the next reboot. In our DICE implementation we use the ACL to protect the UDS from writes and reads after it was used by the boot layer. This is done by configuring the ACL configuration registers during the boot layer execution.

Further, the nRF52840 features a Non-Volatile Memory Controller (NVMC). The NVMC is used for writing and erasing the internal flash memory. Before writing to a flash page it has to be erased in advance, or it has to be empty. Also, flash erases can only be done for a whole page of 4 KB at once. To erase a flash page the NVMC configuration register has to be set to "erase enable". Afterward, the starting address of the page has to be written to the NVMC erase-page register, which starts the erase operation. To write values to addresses within the erased page the NVMC configuration register has to be set to "write enable". After this, values can be written to the flash page with a normal store instruction [6].

The radio software for the nRF52840 is provided within the Software Development Kit (SDK) [11] as a pre-built software stack called softdevice [10]. We used the softdevice as a source for gadgets.

5.2 Experimental Setup

Our experimental setup consists of a nRF52840 evaluation board communicating with a laptop using IPv6 over BLE [45]. The nRF52840 runs a UDP server application on top of an underlying DICE implementation. The UDP server application is taken from the nRF5 SDK and uses the softdevice stack as BLE driver. On the laptop, a simple Python UDP client is implemented.

We implemented DICE as explained in Section 2.4. We placed the UDS into a flash page at address 0x0000FC00 and protected it with the described ACL. Additionally, we use the ACL as well to protect the boot layer from overwriting.

To be able to perform the attack, a memory corruption vulnerability is required. In our proof of concept implementation, we use an artificial buffer overflow which was implemented inside a callback function that handles incoming UDP data. For this, we use a memcpy() function that copies incoming data into a buffer on the stack without checking data length and buffer size.

5.3 Identification of Gadgets

We used the open-source tool ROPgadget [9] to identify the required ROP gadgets within the softdevice BLE stack. For disabling interrupts a suitable gadget was found at memory address 0x000015EEE, see Listing 4. It is almost identical to the ideal gadget in Listing 1. The only difference is an additional register r4 used as a parameter in the pop instruction. Fortunately, this additional register does not alter the function of the gadget, so it can be considered redundant. This means that an arbitrary dummy value can be put on the stack and popped into register r4 when the gadget is used.

5.4 Assembling the Exploit

Due to the slightly different gadgets, adaptions are necessary for the ROP procedure described in Section 4. To fill the additional registers of each pop instruction with dummy values, such values have to be inserted into the exploit data. More precisely, the dummy values have to be inserted in front of every gadget address. This is because the redundant registers, as shown in Listing 4 and Listing 5, are right before the program counter in the register order of the pop instructions.

To be able to write to a certain flash memory address the attacker has to configure the NVMC as explained in Section 5.1. In our case, the flash memory is much larger than the firmware size of the regular application, so it is sufficient to just enable flash writing and store the malware to the empty flash sections. If this is not the case, the attacker needs to choose a certain flash page that is not critical for his intentions and erase it first. The NVMC configuration value (write enable), the NVMC configuration register’s address, and the store gadget address have to be inserted into the exploit in front of the first malware piece. This configures the NVMC before the first write to flash.

Figure 3 shows how the flash configuration and the non-ideal gadgets affect the exploit data for our implementation compared to the ideal exploit.

The utility malware has to modify a function in the original firmware so that it jumps to flash2ram_copy(), which copies the alias key and certificate from flash to RAM. As it is not possible to modify a flash memory that is not empty, the utility malware copies the whole flash page, containing the function to modify, into RAM, then modifies it, erases the original flash page, and writes...
Figure 3: Comparison of ideal and actual exploit structure

Listing 6: Instructions that replaced firmware code to jump to malware

back the modified page from RAM into flash. For this, a similar routine as shown in Listing 3 is used. The binary encodings of the new instructions are stored in flash as constant 32-bit words as part of the utility malware. The utility malware takes these words and replaces the original instructions at the right position inside the copied flash page in RAM. Afterward, after erasing the original flash page, again a slightly adapted routine as in Listing 3 is used to write back the modified flash page.

The two routines of the utility malware flash2ram_copy() and ram2flash_copy() are written in two distinct flash pages for simplicity of implementation. ram2flash_copy() is written to the flash page starting at memory address 0x000FC000. flash2ram_copy() is written to the flash page at 0x000FE000. The flash page at the address 0x000FE000 is used for storing the alias key and certificate.

We modified the original firmware function app_sched_init() in order to jump to flash2ram_copy() at every boot. This function is part of the UDP server application and is located in the flash page starting at 0x00034000. The function initializes an event scheduler and is executed at every system start after DICE key derivation. We replaced the last 10 bytes of binary code in the function with the binary encoding of the instructions shown in Listing 6, which also equals 10 bytes. This does not do any harm to the function’s intended functionality. The first two instructions write the address of flash2ram_copy() into register r4. Afterward, the CPU jumps to this address with a bx instruction.

5.5 Analysis

To evaluate our attack we implemented a DICE backend in Python on top of the Python UDP client. This backend executes a challenge-response protocol with the device, where the device signs a nonce with the alias private key. The signature and the alias certificate are sent to the backend. The backend verifies the signature of the nonce and the certificate.

After sending the exploit data the device resets itself as intended. After reconnecting and sending an attestation request the attestation is still successful, even though we could clearly see, through inspecting the memory with a debugger, that the firmware was altered and that formerly empty flash pages are now filled with the utility malware, alias private key and alias certificate. This now allows the attacker to install useful malware without getting detected.

Table 1 gives an overview of the size of the ROP exploit and malware. The size of the ROP exploit is approximately four times the size of both utility malware routines combined. This is because, for every 32-bit malware piece, three additional 32-bit values are needed to build the exploit data and perform the ROP procedure. If an attacker wants to install complex useful malware that requires, e.g., about 100 KB of memory, the ROP exploit would be about 400 KB of size. Depending on how much stack memory is available or how much data the IPv6/UDP server implementation can handle at once, an attacker might need to split the useful malware into smaller parts. In our case, the limitation was the Maximum Transmission Unit (MTU) size of the IPv6 standard, which is 1,280 bytes. This means that in our case we would need to split a exploit of 400 KB into approximately 375 to 400 parts.

| Utility malware routine / ROP exploit data | Size       |
|------------------------------------------|------------|
| ram2flash_copy()                         | 233        |
| flash2ram_copy()                         | 52         |
| ROP exploit                              | 1140       |

Table 1: Sizes of utility malware routines and ROP exploit in bytes

6 COUNTERMEASURES

In this section, we discuss several approaches for mitigating the TOCTOU attack on DICE attestation and discuss their advantages and disadvantages. Additionally, we express our recommendation about the use cases in which a given countermeasure is a good/bad fit.

Firmware Updates. If the vulnerability, allowing our attack becomes known to the device manufacturer, a firmware update can be provided. After this update, a new attestation key will be created and since the bug is removed our attack will not be possible. If the device refuses to attest with the new key, the device is still running malware. This means that DICE can detect malware with absolute certainty only if the bug allowing the malware becomes known and a patch is installed fixing it. Note that providing updates that do not fix the vulnerability is insufficient since the attacker may compromise the newly installed firmware and get the new key by simply repeating the attack after each firmware update. A drawback of this approach is that the bug may stay undetected for a long time. Moreover, even if the bug becomes known, patching the vulnerability may not be possible because of diverse economic and technical reasons. This countermeasure can be preferred in use cases where the device manufacturer provides bug-fixing support for the devices over their lifetime and where it is acceptable that the devices run malware for the time needed to provide the patch. For use cases where this does not apply firmware updates are not a practical countermeasure.
Secure Boot with Secure Reset Trigger. One possible countermeasure against the described attack is to implement secure boot in parallel to DICE attestation. In contrast to DICE where the execution always jumps to the next layer regardless if the layer is compromised or not in the secure boot approach the jump in the next layer is accomplished only if the signature of the next layer is correct. Secure boot can restrict the effect of malware infection up to the time when the device resets. However, if the device runs malware the malware may ensure that the device never resets. In order to overcome this problem, an additional mechanism is required allowing the backend to enforce a device reset as proposed in [33, 67]. In these papers, the authors propose the usage of an Authenticated Watchdog Timer (AWDT) which causes the device to reset if the backend stops issuing authenticated tokens. However, this approach has higher hardware requirements – either an additional coprocessor [67] or a Trusted Execution Environment (TEE), e.g., TrustZone-M [33]. Additionally, a reset may be disturbing in real applications. This countermeasure can be preferred in applications which can be safely reset. This countermeasure is especially not suitable for safety-critical applications, e.g., automotive control units where a reset of the CPU may cause dangerous situations.

Additional Inputs in the Key Derivation Process. The key derivation process for the first mutable layer may use an additional input unique for the boot cycle. This input can be a nonce received from the backend before the last reset or a counter. Doing so will ensure that the attestation key is unique after each reboot. Note that this is a stronger approach than the secure boot approach (without reset trigger) since the backend can request attestation with a new nonce/counter which can only be provided if the device resets. In this way, a device running malware will not be capable to attest at any point in time. This countermeasure can be preferred in the same use cases as the countermeasure using secure boot with secure reset trigger. However, its advantage is that it does not require an additional chip or TEE and that the time of reset can be chosen by the application.

No Alias Key Exposure. Another possible countermeasure against our attack is to run the attestation protocol with the backend as the very first operation of the top firmware layer. Then the alias key must be deleted. This way the device does not expose any networking services and eventual vulnerabilities while the sensitive alias key is available. Additionally, the attestation protocol must be initiated by the device and must not require the receiving of any information from the backend such as a nonce. For replay protection of the protocol in this case a counter can be used, which however requires non-volatile storage. An additional disadvantage is that for a new attestation, a reboot is required and this may be problematic for some real-world applications. This countermeasure is equivalent to the countermeasure using additional inputs in the derivation process regarding the use case for which it is most suited.

Improving Memory Safety. The memory safety of the embedded software can be improved which will make it possible to avoid vulnerabilities such as buffer overflows. This can be achieved by using memory save languages such as Rust. In contrast to other memory save languages which may have too high requirements for the majority of microcontrollers, Rust is a compiled language that makes it comparable regarding speed of execution and executable size to C and C++. A disadvantage of this approach is that a large body of embedded C/C++ code already exists which needs to be rewritten. Using Rust can be beneficial in projects where the dependencies on existing code written in C and C++ are small.

The advantages and disadvantages of the different techniques are summarized in Table 2. To use additional inputs in the key derivation process or reducing the key exposure appears to offer good level of security and have acceptable disadvantages for the majority of use cases.

7 RELATED WORK

Attestation. Attestation techniques are typically classified into three groups regarding their hardware requirements – hardware-based, software-based and hybrid. Hardware-based techniques, e.g., [18, 38, 50, 62] use either a dedicated security chip (TPM [62]) or on-chip trusted execution environment such as TrustZone [2] or SGX [44]. Hardware-based techniques are considered to cumbersome for deeply embedded systems. Software-based techniques, e.g., [19, 54, 55] do not have any specific hardware requirements. They leverage information about the required time for certain computations such as the calculation of checksums. Those techniques are applicable only when the communication channel between prover and verifier has constant delays, therefore they are not suitable for devices communicating over the Internet. Hybrid techniques, e.g., [20, 27, 32, 41, 56] have lower hardware cost than the hardware techniques and at the same time does not impose timing requirements on the communication as the software-based techniques which makes them the preferred choice for constrained IoT devices. These techniques usually use some form of deeply integrated hardware extensions of the Central Processing Unit (CPU). Further, regarding the time at which the attestation evidence is generated the attestation techniques can be classified in attestation with boot time evidence generation [28, 53, 60], attestation with on-request evidence generation [20, 27, 32, 41, 56] and attestation with self-initiated evidence generation [25, 26, 34].

TOCTOU Attacks on Attestation. A discussion of the TOCTOU problem in the context of on-request hybrid attestation for constrained devices is provided in [46]. As a solution, the authors propose a method that uses secure logging of the time of memory modification. Alternatively, the methods presented in [25, 26, 34] propose self-initiated measurements with periodic or unpredictable schedule. Another possible approach to mitigate the TOCTOU attack is presented in [16], where the control flow path of the software is attested. An investigation of the problem of memory consistency during an attestation measurement is provided in [24]. The lack of memory consistency may allow TOCTOU attacks. As a solution, the authors propose different memory locking approaches. A TOCTOU attack on TPM attestation is demonstrated in [21]. The authors show that attestation can succeed when loaded critical code and data are modified after they are measured with a TPM. For this attack a Linux kernel vulnerability that allows the attacker to manipulate the page table is required. For demonstration purposes, the authors developed a malicious kernel module that executes the attack. As a solution, a method is proposed using the MMU and
The DICE series of specifications [60, 61, 63, 64] allows a variety of implementations. Implementations using standard microcontrollers [32, 36], as well as, hardware implementations [35] were demonstrated by previous research. Moreover, DICE is available in commercial products such as the Microchip’s CEC1702 [1] and the NXP’s LPC5500 [7]. An architecture combining DICE and secure boot was recently formally verified in [59].

8 CONCLUSION

The DICE series of specifications provide a standardized mechanism for detecting malware running on constrained IoT devices. However, DICE does not protect from malware capable of copying valid attestation keys and reusing them while the device is compromised. This is, however, a very common malware capability, therefore such attack vectors are realistic. Our attack requires an exploitable memory corruption bug, e.g., a buffer overflow and knowledge of the firmware running on the device. While the former is a valid assumption on embedded systems written in C/C++, the latter information can be obtained by capturing a single device and dumping its software. Then our attack can be conducted on all IoT devices belonging to a given fleet running the same firmware, therefore our attack is scalable. Through our proof of concept implementation we demonstrated the feasibility of the attack in realistic IoT deployments, for instance, where devices communicate over IPv6. We proposed several countermeasures to mitigate the shortcomings of the DICE series of specifications.

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