An Analytical Estimation of Spiking Neural Networks Energy Efficiency

Edgar Lemaire  
LEAT, Univ. Côte d’Azur, CNRS  
edgar.lemaire@univ-cotedazur.fr

Loïc Cordone  
Renault Software Factory  
LEAT, Univ. Côte d’Azur, CNRS  
loic.cordone@univ-cotedazur.fr

Andrea Castagnetti  
LEAT, Univ. Côte d’Azur, CNRS  
andrea.castagnetti@univ-cotedazur.fr

Pierre-Emmanuel Novac  
LEAT, Univ. Côte d’Azur, CNRS  
pierre-emmanuel.novac@univ-cotedazur.fr

Jonathan Courtois  
LEAT, Univ. Côte d’Azur, CNRS  
jonathan.courtois@univ-cotedazur.fr

Benoît Miramond  
LEAT, Univ. Côte d’Azur, CNRS  
benoit.miramond@univ-cotedazur.fr

Abstract—Spiking Neural Networks are a type of neural networks where neurons communicate using only spikes. They are often presented as a low-power alternative to classical neural networks, but few works have proven these claims to be true. In this work, we present a metric to estimate the energy consumption of SNNs independently of a specific hardware. We then apply this metric on SNNs processing three different data types (static, dynamic and event-based) representative of real-world applications. As a result, all of our SNNs are 6 to 8 times more efficient than their FNN counterparts.

Index Terms—Spiking neural networks, Energy metrics, Computational metrics, Event-based processing, Low-power artificial intelligence

I. INTRODUCTION

Neuromorphic computing has been studied for many years as a game changer to address low-power embedded AI, assuming that the inspiration from the brain will natively come with a reduction in energy consumption. Neuromorphic computing mainly focuses on the encoding and the processing of the information with spikes. If this property takes an obvious place in the biological functioning, it is far from obvious that it is the only one to explain the efficiency of the brain. It is therefore necessary to ask the question whether considering this characteristic in isolation brings a gain compared to the classical neural networks used in deep learning. This is the question that this paper seeks to answer by restricting the study to standard machine learning tasks on three different types of data: static, dynamic and event-based data.

There already exist comparisons between Spiking Neural Networks (SNNs) and Formal Neural Networks (FNNs, i.e. non-spiking Artificial Neural Networks) in the literature. However, such comparisons are hardly generalizable since they focus on specific applications or hardware targets [1], [2]. Moreover, the considered applications are often toy examples not representative of real-world AI tasks. Another approach consists in producing metrics in order to evaluate the relative energy consumption between the two coding domains, based on their respective synaptic operations and activity. We thus propose a novel metric for energy consumption estimation taking synaptic operations, memory accesses and element addressing into account. Moreover, our metric is mostly independent from low-level implementation or hardware target to ensure its generality.

The proposed metric is described and applied to three datasets representative of the aforementioned data types: CIFAR-10 for the static case, Google Speech Commands V2 for the dynamic case, and Prophesee NCARS for the event-based case. Moreover, those datasets are closer to real-world applications than usual benchmarks of the neuromorphic community. The metric is used in conjunction with accuracy measurements to provide an in-depth evaluation of those three application cases and their relevance for spiking acceleration. We use the advanced Surrogate Gradient Learning technique and Direct Encoding spike conversion method, since they offer the best trade-off between prediction accuracy and synaptic activity [3].

Our code and trained SNN models are available upon request.

II. STATE OF THE ART

1) Data Encoding: In order to process data in SNNs, it must be encoded into spikes. Rate, Time and Direct encoding are three methods used to convert conventional data towards spiking domain. Rate coding [4] is the most notorious, since it provides state-of-the-art accuracy on most AI tasks. However, it generates a lot of spikes over a large number of timesteps, drastically impacting computational and energy efficiency. Time coding [5] intends to cope with this issue by encoding information in latency rather than rate, thus generating much fewer spikes. Yet, the temporal sparsity of latency-coded spikes causes long processing times, resulting in an energy overhead.

To cope with those limitations, we address a novel encoding scheme: Direct Encoding [6]. It should be noted that this term is a proposition of ours. In Direct Encoding, the first processing layer is made of hybrid neurons with analog inputs...

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and spiking behaviour (IF, LIF...). The weights of this layer are learned during training, thus encoding can be tuned to reduce spiking activity in the network [7]. In the present work, we evaluate Direct Encoding on CIFAR-10 and GSC datasets. Additionally, we evaluate native spike encoding using event cameras [8]. In this method, each pixel of the sensor generates a spike whenever it detects a brightness variation, thus encoding movement into spikes. With such sensor, the input spiking activity is very low, since only the information of interest (i.e. moving objects) are returned by the camera. This property helps improving the computational and energy efficiency of SNNs. We evaluate native encoding using the Prophesee NCARS dataset.

2) Training of SNN in the literature: Spiking neural networks cannot use the classical backpropagation training algorithm to learn their weights because its activations (spikes) are binary and thus non-differentiable. Encoding static data such as images using rate coding enables the conversion of an already trained FNN to a SNN. The most common way is to replace the ReLU neurons of the FNN by IF neurons [9]. However, the prediction accuracy obtained through conversion is systematically inferior to their FNN counterpart, while generating a lot of spikes over a large number of timesteps. Numerous works have studied how to train SNNs directly in spiking domain. The best results were obtained using backpropagation-based learning rules, such as the surrogate gradient [10]. To circumvent the non-differentiability of spikes in SNNs, the main idea of surrogate gradient learning is to use two distinct functions in the forward and backward passes: an Heaviside step function for the first, and a differentiable approximation of the Heaviside in the latter, such as a sigmoid function. Using surrogate gradient learning requires a fixed number of timesteps. As the number of computations performed by SNNs increases with the number of timesteps, being able to fix it beforehand and to tune it during the training is vital to increase the computational efficiency of SNNs.

3) Comparisons based on measurements: In the literature, a few comparisons of SNNs and FNNs have been produced based on hardware measurements. Some papers show competitive results for SNNs: in [11], the authors highlighted the influence of the spike encoding method on the accuracy and computational efficiency of the SNN. They compared the spiking and formal networks through a Resnet-18 like architecture on two classification datasets. They found that SNNs reached higher or equivalent accuracy and energy efficiency. In [11], the authors showed that an SNN could reach twice the power and resource efficiency of an FNN, with an MLP on MNIST dataset targeting ASIC. However, those encouraging results are still very specific and thus hardly generalizable.

A more holistic approach, the authors of [1] performed a design space exploration (including encoding, training method, level of parallelism...) and showed that the advantage of the SNN depended on the considered case, making it difficult to draw general rules. In [2], researchers showed that SNNs on dedicated hardware (Loihi) demonstrated better energy efficiency than equivalent FNNs on generic hardware (CPU and GPU) for small topologies, but observed the opposite using larger CNNs. Once more, the conclusions depended on the studied case and could not be generalized. Albeit encouraging, those results are not sufficient to draw general conclusions regarding the savings offered by event-based processing, since they depend on the selected application, network hyper-parameters and hardware targets. Therefore, another approach consists in comparing both coding domains through estimation metrics, taking a step back to produce more general conclusions.

4) Comparisons based on metrics: Most energy consumption metrics are based on the number of synaptic operations: accumulations (ACC) in the SNN and multiplication-accumulations (MAC) in the FNN. Those models have limitations: energy consumption is assimilated to the energy consumption of synaptic operations [12], thus other factors (such as neuron addressing in multiplexed architecture or memory accesses) are often neglected. Moreover, the models usually do not take into account some specific mechanisms, like membrane potential leakage, reset and biases integration. In [11], the authors proposed a metric based on synaptic operations only, and found great energy consumption savings for the SNN (up to 126× more efficient than the FNN baseline). In [4] the authors demonstrated that such simplistic metrics were not always coherent with actual energy consumption of circuits on FPGA. When taking memory into account, another team [13] found equivalent energy consumptions for SNNs and FNNs using various topologies on CIFAR10. Additionally, reference [14] measured a theoretical maximum spike rate of 1.72 to guarantee energy savings in the SNN based on a detailed metric, accounting for synaptic operations, memory accesses and activation broadcast. Those energy consumption models are enlightening, but still fail to settle whether event-based processing is sufficient to increase energy efficiency. That is mostly because those metrics are too hardware specific, or do not take all significant sources of energy consumption into account.

In the present work, we propose a metric intended to be independent from low-level implementation choices, based on three main operations: neuron addressing, synaptic operations and memory accesses.

III. METRICS

A. Operational cost

In this section we define a metric to compute the number of ACC and MAC due to synaptic operations in SNNs and FNNs.

1) Convolutional layers: For a convolution layer, the number of filters is defined by \( C_{\text{out}} \) and their size are noted \( C_{\text{in}} \times H_{\text{kernel}} \times W_{\text{kernel}} \), where \( C \), \( H \) and \( W \) stands for channel, height and width. The input and output of the layer are composed of a set of feature maps, with shapes \( (C_{\text{in}} \times H_{\text{in}} \times W_{\text{in}}) \) and \( (C_{\text{out}} \times H_{\text{out}} \times W_{\text{out}}) \) respectively. In the following we consider the padding mode “same” and a stride \( S \). The number of timesteps is noted \( T \). The equations describing the number of MAC and ACC operations in FNNs and SNNs, for convolution layers, are summarized in Eq. [1]
In FNNs, the integration of dense input matrices requires a MAC operation for each element of the convolution kernels. That is described in the first row of Eq. \(1\). Additionally, the integration of synaptic biases as ACC operations, since it does not require multiplication with input activation. There is one bias per output neuron as shown in the second row of Eq. \(1\).

On the other hand, for an SNN the input activations are sparse binary matrices. The number of operations of the layer, depends on the number of input and output spikes of that layer, noted \(T_{l-1}\) and \(T_l\). Since spikes are binary and, they are integrated via ACC operations in contrast with FNNs. Each input spike causes one ACC operation per element of each filter, as shown in the first term of the fourth row (ACC\(_{SNN}\)) of Eq. \(1\). The second term accounts for the bias added to each membrane potential at each timestep. The third term accounts for the membrane potential reset whenever an output spike is generated. Additionally, SNNs may involve a membrane potential leakage (i.e. LIF neurons), which is modeled by an additional MAC operations for each output neuron, which is repeated at each timestep. This is depicted in the last two rows of Eq. \(1\).

2) Fully-connected layers: The same reasoning is applied to FC layers. For a given layer \(l\) the number of input and output neurons is noted \(N_{in}\) and \(N_{out}\) respectively. The equations for the number of MAC and ACC operations attributable to synaptic operations in FC layers are summarized in Eq. \(2\).

\[
\begin{align*}
\text{MAC}_{\text{FC-1}} &= N_{in} \times N_{out} \\
\text{ACC}_{\text{FC-1}} &= N_{out} \\
\text{MAC}_{\text{SNN-FC-1}} &= N_{out} \times T \\
\text{ACC}_{\text{SNN-FC-1}} &= T_{l-1} \times N_{in} \times N_{out} + T \times N_{out}
\end{align*}
\]

B. Memory cost

In order to evaluate the amount of energy used by both the FNN and the SNN, multiple assumptions have to be made. Without these assumptions, results could vastly vary between different unconstrained hardware implementations. Each layer of the FNN is assumed to have its own local (non-shared) memory. As a result, activations need to be kept in memory (i.e. I/O buffers) for all layers. The data flow between layers of the SNN is assumed to be sparse and asynchronous. Therefore, messages of incoming spikes must be buffered in a FIFO queue for each layer. Additionally, the SNN must keep the membrane potentials for all layers between timesteps. In both cases, we assume that all the memory is akin to local SRAM, including weights in order to support a reconfigurable architecture. Additionally, there is no local caching in a register bank. Only registers for the operands and a local accumulator are present and are excluded from this evaluation. All data is assumed to be represented with the same number of bits, including the messages describing a spike.

1) Memory accesses: Data flowing from and to the memory is an important sink of energy. We attempt to describe each read or write operation of both the FNN and the SNN for each layer in order to evaluate the possible energy savings from using an SNN, which is mainly a result of its sparsity. Equations are provided for a single input for the FNN and a single timestep for the SNN.

a) Read operations to inputs: For a formal Conv layer, each output position matches with read operations from all input channels and all positions for which the kernel applies. For a formal FC layer, the number of read operations for the input data is equal to the number of inputs \(N_{in}\).

\[
RdIn_{\text{Conv}} = C_{in} \times C_{out} \times H_{out} \times W_{out} \times W_{kernel} \times H_{kernel}
\]

(3)

\[
RdIn_{\text{FC}} = N_{in}
\]

(4)

For the SNN, the read operations in the queue directly depends on the number of incoming spikes \(T_{l-1}\) and must be measured during inference:

\[
RdIn_{\text{SNN}} = T_{l-1}
\]

(5)

b) Read operations to parameters: In a formal Conv layer, each output position matches with read operations for all the weights in all filters associated to all input channels. The biases generate additional reads for all output positions and all filters. For an FC layer, every weight corresponding to all output neurons \(N_{out}\) and all inputs \(N_{in}\). The biases cause additional read for all output neurons.

\[
RdParam_{\text{Conv}} = (C_{in} \times W_{kernel} \times H_{kernel} + 1) \times C_{out} \times W_{out} \times H_{out}
\]

(6)

\[
RdParam_{\text{FC}} = (N_{in} + 1) \times N_{out}
\]

In an spiking Conv layer, all received spikes \(T_{l-1}\) will trigger a read for all output filters and all associated output positions (i.e. of the dimensions of the kernel). Biases for all output positions and filters must still be read. For an FC layer, the number of read operations for parameters is similar to an SNN except that weights are only read for all input spikes \(T_{l-1}\). Biases must still be read for all output neurons \(N_{out}\).

\[
RdParam_{\text{Conv}} = T_{l-1} \times C_{out} \times W_{kernel} \times H_{kernel} + C_{out} \times W_{out} \times H_{out}
\]

(7)

\[
RdParam_{\text{FC}} = T_{l-1} \times N_{out} + N_{out}
\]

(8)

c) Read operations to potentials: There is no membrane potential to update in an FNN so there is no associated read operation.
In a spiking Conv layer, the membrane potentials corresponding to all output positions affected by each input (i.e. of the dimensions of the kernel) in all filters must be read in order to update them. Biases need to be applied separately and therefore generate an additional read operation at each timestep for all output positions and all filters. For FC layers, the potentials of all output neurons are read for each input. Biases are applied separately and therefore generate an additional read operation at each timestep for all output neurons.

\[
RdPot_{\text{Conv}} = \theta_1 \times C_{\text{out}} \times W_{\text{kernel}} \times H_{\text{kernel}} + C_{\text{out}} \times H_{\text{out}} \times W_{\text{out}} \tag{9}
\]

\[
RdPot_{\text{FC}} = (\theta_1 + 1) \times N_{\text{out}} \tag{10}
\]

d) Write operations to outputs: In an formal Conv layer, each output position in all filters requires a write operation. For an FC layer, each output neuron require a write operation. In both cases, the output is assumed to be fully computed in the local accumulator, including bias, before being written to RAM.

\[
WrOut_{\text{Conv}} = C_{\text{in}} \times H_{\text{in}} \times W_{\text{in}} \tag{11}
\]

\[
WrOut_{\text{FC}} = N_{\text{out}} \tag{12}
\]

For the SNN, the write operations to the queue directly depends on the number of generated spikes \(N_{\text{output}}\) and must be measured during inference:

\[
WrOut = N_{\text{output}} \tag{13}
\]

e) Write operations to potentials: There is no membrane potential to update in an FNN so there is no associated write operation.

In an spiking Conv layer, the membrane potentials corresponding to all output positions affected by each input (i.e. of the dimensions of the kernel) in all filters must be written to in order to update them. Additionally, the biases must also be written separately to the potentials for all output positions and all filters at each new timestep. For an FC layer, the potentials of all output neurons must be written to for each input. Additionally, the biases must also be written to the potentials for all output neurons separately at each new timestep.

\[
WrPot_{\text{Conv}} = \theta_1 \times C_{\text{out}} \times W_{\text{kernel}} \times H_{\text{kernel}} + C_{\text{out}} \times H_{\text{out}} \times W_{\text{out}} \tag{14}
\]

\[
WrPot_{\text{FC}} = \theta_1 \times N_{\text{out}} + N_{\text{out}} \tag{15}
\]

C. Addressing in Sparse vs. Dense Convolutions

In this subsection, we evaluate the cost of addressing in FNNs and SNNs. The first uses dense processing, in which all input synapses are stimulated at the same time. On the other hand, the second uses sparse processing, in which synapses are sparsely stimulated across time. Let us begin with convolution layers. In order to simplify the following matter, we consider convolutions with a “same” padding (input and output feature maps of same sizes) and a stride of \(S\). In FNNs, a kernel scans all its possible positions (depending on padding, stride...) on the input sample and generates a dense output feature-map. In such dense convolutions, computation is performed sequentially and addresses can be computed by incrementing only an index (by 1 or \(S\) assuming the memory is contiguous and ordered the same way it is processed. Thus, one index runs through the input, one index runs through the output and one index runs through the weights. In SNNs, sparse convolutions are performed asynchronously upon reception of input spikes, thus the kernel positions (i.e. output neuron addresses) must be calculated each time a spike is received. In a sparse representation, computation is performed non-sequentially with no prior knowledge of which output position is affected by an incoming spike. Computing the initial output position requires two multiplications. Thereafter, the computation of the remaining positions are computed by incrementing an index assuming the memory is contiguous and ordered as for FNNs. There is only one index running through the kernel weights. The cost of addressing in number ACC and MAC operations in spiking and formal convolution layer are summarized in Equation 16.

\[
\begin{align*}
\text{MAC}_{\text{Addr-Conv-l}} &= \theta_1 \times 2 \\
\text{ACC}_{\text{Addr-Conv-l}} &= \theta_1 \times C_{\text{in}} \times H_{\text{in}} \times W_{\text{in}} + C_{\text{out}} \times H_{\text{out}} \times W_{\text{out}} + C_{\text{out}} \times H_{\text{kernel}} \times W_{\text{kernel}} \\
\end{align*}
\]

\[
\text{MAC}_{\text{Addr-Conv-l}} = \theta_1 \times C_{\text{out}} \times H_{\text{kernel}} \times W_{\text{kernel}} \times W_{\text{out}} \times H_{\text{out}} \times C_{\text{out}} \tag{16}
\]

Where \(C\) are the numbers of channels, \(W\) the widths and \(H\) the heights, of respectively the inputs when the index is in, outputs when it is out and kernels when it is kernel. \(\theta_1\) is the number of input spikes.

The same reasoning is applied to fully-connected layers. In FNNs, one index runs through the input, and another index runs through both the output. In SNNs, one single index runs through the output upon receiving an input spikes. This yields Eq. 17.

\[
\begin{align*}
\text{MAC}_{\text{Addr-FC-l}} &= \theta_1 \times N_{\text{in}} + N_{\text{out}} \\
\text{ACC}_{\text{Addr-FC-l}} &= \theta_1 \times C_{\text{in}} \times H_{\text{in}} \times W_{\text{in}} \times C_{\text{out}} \times H_{\text{out}} \times W_{\text{out}} \times C_{\text{out}} \times H_{\text{kernel}} \times W_{\text{kernel}} \\
\end{align*}
\]

\[
\text{MAC}_{\text{Addr-FC-l}} = \theta_1 \times N_{\text{in}} + N_{\text{out}} \tag{17}
\]

Where \(N_{\text{in}}\) and \(N_{\text{out}}\) are respectively the number of input and output neurons.

d) Write operations to outputs: In a formal Conv layer, each output position in all filters require a write operation. For an FC layer, each output neuron require a write operation. In both cases, the output is assumed to be fully computed in the local accumulator, including bias, before being written to RAM.

\[
\begin{align*}
\text{MAC}_{\text{Addr-Conv-l}} &= \theta_1 \times 2 \\
\text{ACC}_{\text{Addr-Conv-l}} &= \theta_1 \times C_{\text{out}} \times H_{\text{out}} \times W_{\text{out}} + C_{\text{out}} \times H_{\text{out}} \times W_{\text{out}} + C_{\text{out}} \times H_{\text{kernel}} \times W_{\text{kernel}} \\
\end{align*}
\]

\[\text{MAC}_{\text{Addr-Conv-l}} = \theta_1 \times C_{\text{out}} \times H_{\text{kernel}} \times W_{\text{kernel}} \times W_{\text{out}} \times H_{\text{out}} \times C_{\text{out}} \tag{16}\]

Where \(C\) are the numbers of channels, \(W\) the widths and \(H\) the heights, of respectively the inputs when the index is in, outputs when it is out and kernels when it is kernel. \(\theta_1\) is the number of input spikes.

The same reasoning is applied to fully-connected layers. In FNNs, one index runs through the input, and another index runs through both the output. In SNNs, one single index runs through the output upon receiving an input spikes. This yields Eq. 17.

\[
\begin{align*}
\text{MAC}_{\text{Addr-FC-l}} &= \theta_1 \times N_{\text{in}} + N_{\text{out}} \\
\text{ACC}_{\text{Addr-FC-l}} &= \theta_1 \times C_{\text{in}} \times H_{\text{in}} \times W_{\text{in}} \times C_{\text{out}} \times H_{\text{out}} \times W_{\text{out}} \times C_{\text{out}} \times H_{\text{kernel}} \times W_{\text{kernel}} \\
\end{align*}
\]

\[\text{MAC}_{\text{Addr-FC-l}} = \theta_1 \times N_{\text{in}} + N_{\text{out}} \tag{17}\]

Where \(N_{\text{in}}\) and \(N_{\text{out}}\) are respectively the number of input and output neurons.

D. Energy consumption metric

In this section, we combine the equations obtained for computation, memory accesses and addressing in a global Energy evaluation metric. For this purpose, we multiply the energy cost of each operation by its number of occurrences, according to the metrics computed in subsections III-A, III-B and III-C. Our model can be summarized as shown in Eq. 18:

\[
E = E_{\text{mem}} + E_{\text{ops+addr}} \tag{18}
\]
Where \( E_{\text{mem}} \) is the energy consumption of memory accesses, \( E_{\text{ops}} \) that of synaptic operations, and \( E_{\text{addr}} \) that of addressing mechanisms.

Those elements are computed based on the metrics proposed in the above subsections, as shown in Eq. (19) for memory accesses, and Eq. (20) for addressing and synaptic operations. Equations are not repeated for those two last elements since they are identical.

\[
E_{\text{mem}}^{\text{FNN}} = (RdIn^{\text{FNN}} + RdParam^{\text{FNN}}) \times E_{\text{RdRAM}}
+ WrOut^{\text{FNN}} \times E_{\text{WWRAM}}
E_{\text{mem}}^{\text{SNN}} = (RdIn^{\text{SNN}} + RdParam^{\text{SNN}} + RdPot) \times E_{\text{RdRAM}}
+ (WrOut^{\text{SNN}} + WrPot) \times E_{\text{WWRAM}}
\]

With \( E_{\text{RdRAM}} \) and \( E_{\text{WWRAM}} \) the energy for a single read and a single write operation in RAM, respectively. In our computation, we assume that \( E_{\text{RdRAM}} = E_{\text{WWRAM}} \) for simplicity purpose.

\[
E_{\text{ops+addr}}^{\text{FNN}} = (E_{\text{ADD}} + E_{\text{MUL}}) \times MAC_{\text{ops+addr}}^{\text{FNN}}
+ E_{\text{ADD}} \times ACC_{\text{ops+addr}}^{\text{FNN}}
E_{\text{ops+addr}}^{\text{SNN}} = (E_{\text{ADD}} + E_{\text{MUL}}) \times MAC_{\text{ops+addr}}^{\text{SNN}}
+ E_{\text{ADD}} \times ACC_{\text{ops+addr}}^{\text{SNN}}
\]

Where \( E_{\text{ADD}} \) and \( E_{\text{MUL}} \) are the energy cost of single additions and multiplications respectively.

The energy consumption of single operations (addition, multiplication and memory accesses) are drawn from the literature [15] for 45nm CMOS technology. For addition and multiplication with 32-bit integers, we use respectively 0.1pJ and 3.1pJ. For SRAM memory accesses, we compute a linear interpolation function based on 3 particular values: 8 kB (10pJ), 32 kB (20pJ) and 1 MB (100pJ). This function enables to compute the energy cost of a memory access knowing the memory size (i.e. knowing the network hyper-parameters).

IV. METHODS

A. Spike coding

The role of spike coding is to convert input pixels into spikes, which are in turn transmitted to an SNN for information processing. In the Direct encoding scheme, a spiking neuron (e.g. LIF or IF) located in the first layer (encoding) of the network is fed with a constant or dynamic input through \( T \) timesteps. The first layer thus converts the analog input into spike trains. In this paper, we propose three different uses of such encoding which are detailed below.

1) Static Frame-based data encoding: The first method is Static Frame-based data encoding, in which the raw input data is directly broadcast to the first layer. The network input size is thus identical to that of the input sample, each of which is presented repeatedly during \( T \) timesteps. This method is adapted to every type of conventional data. The major drawback of this method is that the whole processing must be repeated over several timesteps (bias integration, membrane leakage...).

2) Dynamic Frame-based data encoding: The second method is Dynamic Frame-based data encoding, adapted to temporal signals. The input data is split into several chunks along the temporal dimension. The network input size is the same as the size of a chunk, which are presented successively at the input, one per timestep. This approach has two main benefits: reducing the input size and no longer considering timesteps mechanisms as an additional cost.

3) Event-based data: Event-based data does not require a specific encoding since events can be interpreted as spikes. However, in order to process event-based data in modern deep learning models, we need to convert them into a dense representation. To process events with FNNs, we simply sum all events occurring during the sample duration \( d \) to reconstruct a single frame, containing integer values. On the other hand, when using SNNs, we accumulate events over \( T \) time windows (i.e. timesteps) lasting \( \Delta t = \frac{d}{T} \) to reconstruct frames. This type of representation is called a voxel grid [16], where each voxel represents a pixel and a time interval. We added the constraint that the accumulation is a simple OR operation: if at least one event is present during the time window then its value will be 1 [17]. This way, all of our event frames stays binary in order to leverage the efficiency of spiking neural networks running on specialized hardware [18].

B. Organization of the output layer

Both our FNN and SNN for static frame-based data use a traditional final fully-connected layer. On the other hand, our models for dynamic frame-based and event-based data use a specific final classification layer as the feature maps are not sufficiently reduced to be flattened before the final fully-connected layer.

We followed the approach used in [17]. The output layer of our SNNs is simply composed of a batch normalization layer, a \( 1 \times 1 \) convolution outputting \( \text{num\_classes} \) channels and a final layer of LIF neurons. The final predictions are then obtained by summing all output spikes first in the spatial dimension and time dimension. We therefore obtain a tensor with a spatial size of \( 1 \times 1 \) with \( \text{num\_classes} \) channels, which is equivalent to the output of conventional fully-connected layers. The 1D convolution in the final layer enables to avoid the use of e.g. average pooling to reduce the spatial dimension as it would be incompatible with spikes computations. We used the same approach for the equivalent FNNs but without summation along the time axis since it does not exist.
V. Experiments and Results

A. Datasets and Models

1) Static frame-based data: The CIFAR-10 dataset is made up of 60000 32x32 RGB images representing 10 classes. For the SNN, CIFAR-10 samples are repeated as input over $T = 4$ timesteps, following the static frame-based data encoding described in Section IV-A. For this task, we use a VGG-16 architecture described in [19]. We dropped the max pooling layers by using a stride of 2 in their preceding convolution and we added batch normalization layers after each convolution.

2) Dynamic frame-based data: The Google Speech Commands V2 dataset is a dataset of audio signals sampled at 16 kHz composed of 1-second recordings of 35 spoken keywords. We performed data augmentation by randomly changing the speed of the raw audio signals. The raw data are preprocessed to obtain images that can be fed to CNNs. We used 10 MFC Coefficients, FFT of size 1024, a window size of 640 with a hop of 320, and a padding of 320 on both sides. This results in a 48x10 image interpreted as 1D data truncated to 48 samples with 10 channels. For the SNN, we divided this temporal data in $T = 2$ timesteps, each of size 24. To tackle this classification task, we designed a 4-layers CNN with the following topology: 48c3 - 48c3 - 96c3 - 35c1. Each convolutional layer has a stride of 1 and was followed by a batch normalization layer.

3) Event-based data: The Propheese NCARS dataset is a classification dataset composed of 24k samples of length 100ms captured with a Propheese GEN1 event camera mounted behind the windshield of a moving car. The samples represent either a car or background. We resized all the samples to a size of $64 \times 64$ pixels using nearest neighbor interpolation to keep our inputs binary. For SNNs, we divided each sample in $T = 5$ timesteps, while all the events were summed into a single frame for the CNN. We proposed a variant of the classical Tiny VGG-11 architecture [19] that uses 4 times fewer channels in each convolution layers, reducing the number of parameters and calculations. Once again, we dropped the max pooling layers by using a stride of 2 in their preceding convolution and we added batch normalization layers after each convolution. Finally, we replaced the final 3 fully-connected layers by our output layer described in Section IV-B.

B. Results

We trained our FNNs using PyTorch, and our SNNs using SpikingJelly [21] with surrogate gradient learning. The models were trained over 50 epochs for GSC and NCARS, and 300 for CIFAR-10. All presented results represent the average over 5 runs. The performance of our networks were measured by their classification accuracy. We also measured the spike rate of our SNNs, corresponding to the average number of spikes per synapse in the network. Since computations are only performed when there is a spike, this has a direct impact on the SNN energy consumption within our metric. These results are summarized in Table I.

|         | Dataset   | Network   | #Params | Activation | Acc.  | Spike Rate |
|---------|-----------|-----------|---------|------------|-------|------------|
| CIFAR-10| VGG-16    | 15.2M     | ReLU    | 0.951      | –     |
|         | GSC       | 4-layers CNN | 29k    | ReLU       | 0.936 | –          |
|         | NCARS     | Tiny VGG-11 | 356k   | ReLU       | 0.934 | –          |

For dynamic and event data, SNNs are able to reach equivalent or close accuracies to their FNN counterparts, a result never shown experimentally before on these datasets. On the CIFAR-10 dataset, our SNN reaches lower accuracy than the FNN. This is coherent with state of the art results, but should be improved in further works. Still, all of our SNNs reach these performance while having a very low spike rate, on average each neuron of a model spikes less than 0.14 times per inference for the three datasets.

Using the metrics proposed in Section III-B, we were able to precisely estimate the energy consumption of our models. In our model, I/O buffers between SNN layers are FIFOs able to store 1000 32-bit elements. This assumption has been validated through hardware simulation using SPLEAT architecture [18]. On the other hand, the full feature maps are stored in SRAMs between FNN layers. The results are illustrated in Fig.1 and detailed in Table II.

The total energy consumption is dominated by the cost of memory accesses, which is yet unduly neglected in most metrics of the literature. While SNNs have additional memory accesses for updating the neuron potentials, it also requires fewer memory accesses for the weights and the I/O. Moreover, the size of I/O buffers are often much smaller in SNNs than in FNNs, since the first only requires FIFOs of 1000 elements whereas the second requires storing the full feature maps. The lower number of spikes combined with the absence of multiplication result in an energy consumption of synaptic operations two order of magnitude lower for SNNs than for FNNs. In the end, the total energy consumption of our SNNs is between 6.25 and 8.02 times lower than their FNN counterparts, a promising result for the implementation of SNNs on specialized hardware.

VI. Conclusion

Neuromorphic Engineering is based on the assumption that event-based processing is the key to mimic the unparalleled energy efficiency of the biological brain. However, this assumption remains to be proven. The goal of this work was to settle this question through a generic and accurate energy estimation metric, independent from low-level implementation choices and hardware targets. Our proposed analytical model is based on three types of operations occurring in hardware neural network implementations: synaptic operations, memory accesses and addressing mechanisms. This metric was applied.
to three datasets representative of three characteristic data types. In all three cases, spiking implementation could bring major energy savings compared to formal ones as our SNNs are respectively 8.19x, 6.22x and 8.17x more efficient on CIFAR-10, GSC and NCARS, while producing near state-of-the-art accuracy for the last two.

Future works will include a confrontation of those results with actual energy consumption measurements, using our own SNN hardware architecture (SPLEAT [18]) and other state-of-the-art deep learning accelerators. Moreover, further work is required on our CIFAR-10 model, in order to reach state-of-the-art accuracy and thus increase the fairness of the comparison. Additionally, we will study the impact of various quantization schemes on energy consumption.

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