Ternary and Quaternary CNTFET Full Adders are less efficient than the Binary ones for Carry-Propagate Adders

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Abstract—In Carry Propagate Adders, carry propagation is the critical delay. The most efficient scheme is to generate \( C_{\text{out}0} (C_{\text{in}}=0) \) and \( C_{\text{out}1} (C_{\text{in}}=1) \) and multiplex the correct output according to \( C_{\text{in}} \). For any radix, the carry output is always 0/1.

We present two versions of ternary adders with \( C_{\text{in}}=(0V, V_{\text{dd}}/2) \) and \( C_{\text{in}}=(0V, V_{\text{dd}}) \) and two versions of quaternary adders with \( C_{\text{in}}=(0V, V_{\text{dd}}/3) \) and \( C_{\text{in}}=(0V, V_{\text{dd}}) \). Using full swing \( V_{\text{dd}} \) for \( C_{\text{in}} \) reduces the propagation delays for ternary and quaternary adders. 6-bit, 4-trit and 3-quit CPAs are then compared.

Index Terms—Ternary adders, Quaternary adders, Binary adders, Carry-Propagate Adders, CNTFET, propagation delays, power dissipation, chip area.

I. INTRODUCTION

Carry Propagate Adders (CPAs) are the most simple N-digit adders. Figure 1 presents a 4-digit CPA. Whatever digit radix is used (2,3,4...), the carries are always 0/1. In this paper, we consider both binary, ternary and quaternary CPAs. From Figure 1, it results that the performance of a CPA is a direct function of the used 1-digit full adder. More precisely, the critical delay path of a CPA is related to the carry propagation.

With this approach, all proposed designs use \( V_{\text{dd}}/2 \) as the voltage when carry=1 for ternary circuits and \( V_{\text{dd}}/3 \) for quaternary ones. This raises one question: must the binary carries mandatory use 0 and \( V_{\text{dd}}/2 \) ternary/quaternary values or can they use 0/2 ternary values or 0/3 quaternary values? In other words, 0 and \( V_{\text{dd}}/2 \) or 0 and \( V_{\text{dd}} \) in the ternary case and 0 and \( V_{\text{dd}}/3 \) or 0 and \( V_{\text{dd}} \) when the ternary/quaternary adders have a \( V_{\text{dd}} \) power supply. In this paper, we consider ternary and quaternary circuits using the two different approaches for carry levels and we compare them with binary adders. The comparison is extended to CPAs computing approximately the same amount of information: 6-bit (Binary Digit) CPAs, 4-trit (Ternary Digit) CPAs and 3-quit (Quaternary Digit) CPAs. The paper is organized as follow:

- we present the methodology
- we present the different ternary adders and their performance
- we present the different quaternary adders and their performance
- We present the different binary adders that are used for comparison with their performance
- we compare the performance of the quaternary, ternary and binary CPAs computing the same amount of information
- we finally conclude.

A. Carry values in a \( m \)-valued adder

The truth table of the ternary full adder is shown in Table I. The truth table of the quaternary full adder is shown in Table II. In both cases, the input and output carries are binary (0,1). This property is valid for any radix. So, ternary 1-trit full adders have ternary inputs and output (0,1,2) and binary carries (0,1). Quaternary 1-digit adders have quaternary inputs and outputs (0,1,2,3) and binary carries (0,1). There are two techniques to get the different levels:

- Using two power supplies \( V_{\text{dd}} \) and \( V_{\text{dd}}/2 \) for ternary circuits and three power supplies \( V_{\text{dd}}, 2V_{\text{dd}}/3 \) and \( V_{\text{dd}}/3 \) for quaternary circuits.
- Using only one power supply \( V_{\text{dd}} \) and get the intermediate values through transistor connected as resistors. In that case, there is a large static power dissipation resulting from the direct current flow through the voltage divider for intermediate levels. This is why we only consider the option with two or three power supplies.

Fig. 1: 4-digit Carry Propagate Adder
TABLE I: Truth table of a ternary full adder

| A | B | C_{in} | S_{0} | C_{out0} | A | B | C_{in} | S_{0} | C_{out1} |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 2 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 2 | 0 | 1 |
| 1 | 1 | 2 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |

TABLE II: Truth table of a quaternary adder

| A | B | C_{in} | S_{0} | C_{out0} | A | B | C_{in} | S_{0} | C_{out1} |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 2 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 2 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 3 | 0 |
| 2 | 0 | 0 | 0 | 0 | 2 | 0 | 2 | 1 | 0 |
| 2 | 1 | 1 | 1 | 1 | 2 | 1 | 1 | 3 | 0 |
| 3 | 0 | 0 | 0 | 0 | 3 | 0 | 3 | 0 | 1 |
| 3 | 1 | 1 | 1 | 1 | 3 | 1 | 1 | 3 | 1 |

TABLE III: TFAs Comparison

| TFA / Year | CNTFETs Count | Technique |
|---|---|---|
| In [1] 2011 | 412 | Decoders-Binary-Encoder |
| In [2] 2017 | 105 | Two custom algorithm + TMUXes |
| In [3] 2017 | 74 | TMUXes |
| In [4] 2018 | 89 | TMUXes |
| In [5] 2018 | 98 | TBDD algorithm |
| In [6] 2019 | 142 | Unary ops +MUXes+Encoder |
| In [7] 2020 | 74 | Pass transistors + MUXes |
| In [8] 2020 | 106 | Modified Quine-McCluskey algorithm |
| In [9] 2021 | 54 | Unary ops + Decoders + Transmission gates |

B. Related works

A lot of ternary full adders have been published in the last decade [1]–[9]. They use different techniques. Transistor count is not a sufficient criteria to determine the best TFAs. However, considering Table III and a similar Table comparing Ternary Half Adders in [10], we may consider that the technique using unary operators and MUXes is the most efficient one. Several quaternary full adders with CNTFET simulations have been published in the last decade [11]–[13]. In a preprint paper without simulations, several possible implementations based on the transistor count have been evaluated [14]. This paper considers CPAs.

C. Contributions

This paper compares efficient implementations of CNTFET binary, ternary and quaternary adders. The main contributions of this paper are

- For ternary and quaternary adders, we use both the carry swing corresponding to 0 and 1 usual carry swing and the full $V_{dd}$ carry swing. Using full carry swing reduces the carry propagation delays.
- While ternary and quaternary adders use a $V_{dd}$ power supply, we consider binary adders with both $V_{dd}$ and $V_{dd}/2$ power supplies. Reduced voltage swings for binary adders drastically reduce power dissipation and the Power Delay Product (PdP).
- We compare the performance of 6-bit CPAs, 4-trit CPAs and 3-quit CPA that computes the same or approximately the same amount of information.

## II. Methodology

The significant figures to compare circuit designs include switching times, power dissipation, chip area, etc. The comparison is realized by using HSpice simulations and evaluating the chip area according to transistor sizes.

A. CNTFET technology

All simulations are done with the 32nm CNTFET parameters of Stanford library [15]. We use CNTFET technology for two main reasons:

- Simulations parameters for the most recent FinFET technologies are not available.
- Most of papers presenting designs of ternary or quaternary circuits in the last period use simulations with this 32 nm CNTFET technology. This allows our results to be compared with all published results on ternary or quaternary circuits.

One advantage of CNTFET technology is that the threshold levels of gates only depend on the diameter of individual transistors, which facilitates the design of $m$-valued circuits.

B. Propagation delays

Generally, propagation delays are presented as an average of the delays corresponding to all combinations of input transitions. This presentation could be confusing. For the CPA presented in Figure 1, $A_{i}$, $B_{i}$ and $C_{0}$ inputs are simultaneously available. The important information is the propagation delay corresponding to the critical paths, i.e. from $C_{0}$ (or $A_{0}/B_{0}$) to $C_{4}$ and $S_{3}$. When the 4-digit CPA is used to build larger CPAs, the critical path is from $C_{0}$ to $C_{4}$. We will only present the propagation delays corresponding to the critical paths.

C. Power and Energy dissipation

Power and PDP (Power Delay Product) directly depends on the duration of the input signals. It is important to use the same input signal for all designs. For all simulations, we use the input waveforms shown in Fig. 2. We have verified that the delays for 0-2 or 2-0 ternary transitions are always less than ternary transitions 0-1, 1-2, 2-1 or 1-0. The situation is similar for quaternary transitions. We use these waveforms to compute the worst-case delays from Input (A or B) to Sum/C_{outt} and from C_{in} to Sum/C_{out}.
D. Chip area

Without drawing the layout of the circuits, there is no technique to evaluate the chip area. We use a rough evaluation of the chip area by summing the diameters of all the used transistors by each circuit. This rough evaluation is a little bit better than the transistor count. In this paper, we use the diameter values presented in Table IV.

E. Circuit styles

Many techniques have been proposed to design full adders. We only consider techniques with the following properties:

- No static power dissipation
- The circuit outputs have full swing. Reduced swings degrade noise margins and can degrade the operation of cascaded circuits, such as CPAs
- The circuits should have a sufficient driving capability. This point is outlined in subsection II-G

F. Temperature

All the simulations are done with a 25°C temperature. The ternary adders (section IV), the quaternary one (section IV) and one of the three binary ones (section V) use the same circuit style. The same CNTFET parameters are used. There are very few opportunities that different temperatures would change the results of the comparisons between the different adders.

G. Carry propagation in Carry Propagate Adders (CPAs)

As previously mentioned, carry propagation delay is the critical one in CPAs. This delay must be minimized, either for quaternary FAs or for ternary FAs or for binary FAs. One technique is illustrated in Figure 3: \( C_{\text{out}} = C_{\text{out}0} \) when \( C_{\text{in}} = 0 \) and \( C_{\text{out}} = C_{\text{out}1} \) when \( C_{\text{in}} = 1 \). The correct \( C_{\text{out}} \) is obtained via a multiplexer implemented with transmission gates. This technique is used in many published binary full adders, such as Transmission Gate Adders (TGAs) and other ones quoted in [16]. This approach has a major drawback for CPAs. When there is a direct propagation from the first to the last full adders, there is a RC line effect (Figure 4) associated to the capacitive loads that significantly degrade the carry delays. To get a minimal delay without degrading the switching times, the \( C_{\text{out}} \) signal must be restored by an inverter gate, as shown in Figure 5. It means that \( \overline{C_{\text{out}0}} \) and \( \overline{C_{\text{out}1}} \) should be computed, transmitted to \( \overline{C_{\text{out}}} \) through the multiplexer and the final inverter generates \( C_{\text{out}} \). This technique will be used in most circuits that we present.
Fig. 6: 1-trit Full Adder (Mux approach)

TABLE V: Functions $A^1$ and $A^2$

|   | $A^1$ | $A^2$ |
|---|---|---|
| 0 | 1 | 0 |
| 1 | 2 | 0 |
| 2 | 0 | 1 |

A. The MUX approach

According to Table I, When $C_{in} = 0$

- When $B=0$ then Sum=$A$
- When $B=1$ then Sum = $(A+1) \mod(3)$ quoted as $A^1$
- When $B=2$ then Sum = $(A+2) \mod(3)$ quoted as $A^2$
- When $B=0$ then Carry=0
- When $B=1$ then Carry=1 when $A = 2$ else 0
- When $B=2$ then Carry=1 when $A > 0$ else 0

When $C_{in} = 1$

- When $B=0$ then Sum=$A^1$
- When $B=1$ then Sum=$A^2$
- When $B=2$ then Sum= $A$
- When $B=0$ then Carry=1 when $A = 2$ else 0
- When $B=1$ then Carry=1 when $A > 0$ else 0
- When $B=2$ then Carry=1

Functions $A^1$ and $A^2$ are presented in Table V.

B. The ternary full adders

TFA1 and TFA2 use the same threshold detectors (Fig. 7). They implement the NI (Negative Inverter) and PI (Positive Inverter) functions presented in Table VI. The operators $A^1$ and $A^2$ are derived from the threshold detectors as shown in Fig. 8. $A_n$ is the output of a negative inverter, $A_p$ is the output of a positive inverter. $A_{nb}$ and $A_{pb}$ are the outputs of binary inverters with inputs $A_n$ and $A_p$.

TFA1 and TFA2 differ by the implementation of the MUX operators. TFA1 has a specific implementation of sum MUX and carry MUX [17] in the ternary adder (Fig. 9). TFA2 uses the MUX3 operators shown in Fig. [10]. TFA1 and TFA2 use the same MUX2 implementation.

There are few differences between 0.45V and 0.9V carry versions. TFA1 uses a NTI inverter to get $C_{in}$ and the final carry inverter has a 0.45V power supply. For TFA2, $C_{in}$ and $C_{out}$ use 0.9V inverters. TFA1 $\Sigma(D_i) = 72$ nm (for carry swing $= V_{dd}/2 = 0.45V$) and $\Sigma(D_i) = 73$ nm (for carry swing $= V_{dd} = 0.9V$). TFA2 $\Sigma(D_i) = 111$ nm for carry swing $= 0.45V$ and $\Sigma(D_i) = 112$ nm for carry swing $= 0.9V$.

C. Performance with a 2 fF capacitive load

Fig. 11 presents the Input to $C_{out}/Sum$ performance with a $C_L = 2$ fF capacitive load. Fig. 12 presents the $C_{in}$ to $C_{out}/Sum$ performance with the same load.

The following remarks can be made

- TFA2 has a larger $\Sigma(D_i)$ (x1.5).
- There is a huge difference for Input to $C_{out}/Sum$. The only difference comes from the implementation of ternary MUXes. MUX3 implementation of TFA2 is more efficient.
- There is little difference in $C_{in}$ to $C_{out}$ delay for TFA1 and TFA2. This is not surprising as both uses similar MUX2 + Inverter designs for this propagation.
- TFA1 and TFA2 with 0.9V carry swing have $C_{in}$ to $C_{out}$ delay roughly two times faster than TFA1 and TFA2 with 0.45V carry swing. The 0.9V inverters have more driving capability than the 0.45V inverters.

While TFA2 has 50% more $\Sigma(D_i)$, the huge difference in Input to Sum delay for the last stage of a CPA makes TFA2 the best ternary adder either with 0.45V or 0.9V carry swing.

D. Delays and power according to capacitive load

With a log-log scale (except for $C_L = 0$ fF), Fig. 13 presents the input to outputs delays according to $C_L$. Fig. 14 presents
the same information for $C_{in}$ to outputs delay while Fig. [15] present the evolution of power according to $C_L$. Considering the different curves between $C_L = 0.25fF$ and $C_L = 4fF$, we may observe that the delay evolution are close to a linear one, with different slopes. Power increases more than linearly according to $C_L$.

$C_{in}$ to $C_{out}$ path is through a multiplexer and an inverter while $C_{in}$ to Sum is just through a multiplexer. The inverter restores the signal and has more driving capability than the multiplexer. It explains why the sum delay is more sensitive to capacitive load. Input to $C_{out}$ and Sum paths include the whole circuit. The final inverter delay for $C_{out}$ has a limited impact on the overall delay compared to Sum delay, which explain why these large delays don’t increase much when $C_L$ is multiplied by 16. Power increases from x2 to x3.

Fig. [16] presents the ratio delays($C_L = 4fF$)/delays(0.25fF) when $C_L$ is multiplied by 16. It is a figure of the slope of the quasi-linear evolution of delays($C_L$). For $C_{in}$ to output delays, the sum output is more sensitive to $C_L$ than $C_{out}$. It comes from the Sum MUX output that has less driving capability than the $C_{out}$ inverter. Due to the large delays from input to outputs, the impact of $C_L$ is limited for these delays. Fig.[17] presents the power evolution when $C_L$ is multiplied by 16. The impact is slightly more important for $C_{in}$ to Outputs than for Input to Outputs as it concerns only MUXes and the final inverter. The $V_{dd}$ inverter consumes more than the $V_{dd}/2$ inverter.

IV. QUATERNARY FULL ADDERS

The common scheme is presented in Fig. [18] The two QFAs only differ by the carry swing. Carry input values are $V_{dd}/3$ (QFA1) and $V_{dd}$ (QFA2). The control of the two MUX2 is shown is Fig. [18]. The carry output is obtained by inverters with $V_{dd}/3$ supply (QFA1) or $V_{dd}$ (QFA2)

A. Multiplexer Implementation

The common functional scheme is shown in Fig. [18]. The threshold detectors (Fig. [19], the circuits $A^1$, $A^2$, $A^3$ (Fig. [20]
and the MUX4 (Fig. 21) are similar to those of [3]. The two final multiplexers are typical binary multiplexers. \( C_{out} \) is computed from \( C_{out0} \) and \( C_{out1} \). A final inverter delivers \( C_{out} \). 4-input multiplexers with quaternary control are used.
Fig. 15: TFA-Power dissipation according to $C_L$

Fig. 16: TFA-Delay ratio when $C_L$ is multiplied by 16

(Fig. 21). The three inverters with outputs $B_{nbb}$, $B_{ibb}$ and $B_{pbb}$ operate as buffers because inverters $B_n$ and $B_p$ have poor driving capability. Paper [3] first uses a quaternary half adder (sum and carry circuits). A second stage computes the final result by adding +1 mod(4) to sum when $C_{in}=1$ and computing $C_{out}$ according to $C_{in}$. We directly computes Sum and $C_{out}$ within a single stage. $C_{in}$ to $C_{out}$ propagation delay is reduced to a MUX2 and final inverter path.

Fig. 17: TFA-Power ratio when $C_L$ is multiplied by 16

Fig. 18: Quaternary Full Adder (MUX approach)

Fig. 19: Threshold detectors

Fig. 20: $A^1$, $A^2$ and $A^3$ circuits

Fig. 21: 4-input MUX with quaternary control
B. Performance with a 2 fF capacitive load

For all simulations, the same input waveforms are used. Extensive simulations have determined that 0 → 1 → 2 → 3 → 2 → 1 → 0 for input A with $C_{in} = 0$ lead to the input to $C_{out}/$Sum worst case delays. Similarly, 0 → 1 (QFA1)/3 (QFA2) → 0 with $A = 2$ and $B = 1$ lead to the $C_{in}$ to $C_{out}/$Sum worst case delays. These configurations are used to evaluate the performance of QFA1 and QFA2. The only difference is the amplitude of the carry swing. The performance results are presented in Fig. 22 and 23. These figures provide the data and allows a direct comparison for each feature. The significant information is Input to $C_{out}$ (first adder of a CPA), $C_{in}$ to $C_{out}$ (following adders) and $C_{in}$ to Sum (last adder of a CPA).

QFA1 and QFA2 have similar $\Sigma D_i$. QFA1 has a small advantage in term of power. However, it is outperformed by QFA2 for $C_{in}$ to $C_{out}$ delay, which is the critical delay for a CPA. The situation is the same for PDP. This big advantage comes from the last carry inverter that performs better with a $V_{dd}$ supply than with a $V_{dd}/3$ supply.

C. Delays and power according to capacitive load

We now present the performance of QFA1 (0.3V carry swing) and QFA2 (0.9V carry swing). 

With a log-log scale, Fig. 24 presents the input to outputs delays according to $C_{L}$. Fig. 25 presents the same information for $C_{in}$ to outputs delays while Fig. 26 presents the evolution of power according to $C_{L}$. Fig. 27 presents the ratio delays($C_{L} = 4fF)/$delays($0.25fF$) when $C_{L}$ is multiplied by 16. It is a figure of the slope of the quasi-linear evolution of delays($C_{L}$). Fig. 17 presents the power evolution when $C_{L}$ is multiplied by 16. The ternary adder and the quaternary adder having the same basic circuit structure, it is not surprising that the conclusions detailed in III-D are also valid for the quaternary adder.
V. THE BINARY FULL ADDERS

A. Presentation

For the comparison with ternary and quaternary full adders, we consider three different binary adders:

- The first one is a 14T Full Adder (Fig. 31).
- The second one is the typical 28T full adder (Fig. 29).
- The third one is a MUX-based full adder (Fig. 30) that uses the same circuit style than the ternary and quaternary adders. Using the same circuit style allows a fair comparison.

The three binary full adders operate with the same $V_{dd} = 0.9$V as the quaternary adder. They can also operate with a 0.45V supply, which roughly divide by 4 the dynamic power dissipation. $V_{dd} = 0.45$V is a too small power supply value to operate with the three levels of a ternary adder or four levels of a quaternary adder.
Fig. 30: Binary Full Adder-MUX approach (BFA3)

Fig. 31: 14T Binary Full Adder - BFA1

B. Performance with a 2 fF capacitive load

Fig. 32 presents the Input to \( C_{out}/Sum \) performance with \( C_L = 2 \) fF. Fig. 33 presents the \( C_{in} \) to \( C_{out}/Sum \) performance with the same capacitive load. While the MUX-approach (BFA3) is the best approach for ternary and quaternary adders, it is the worst one for binary adder in terms of delays, power and \( \Sigma Di \). All powers for 0.45 \( V_{dd} \) are roughly 1/4 of the powers of 0.9 \( V_{dd} \) versions, leading to PDD slightly smaller or equivalent for both \( V_{dd} \). For input to \( C_{out} \) performance corresponding to the worst case of the first BFA in a CPA, BFA2 is better than BFA1. However \( C_{in} \) to \( C_{out} \) BFA1 delay, which is the critical delay in a CPA, is about 3x smaller than BFA2 delay both for 0.9V and 0.45V \( V_{dd} \). The \( C_{in} \) to \( C_{out} \) delays, which is critical for the last stage of a CPA, are close for BFA1 and BFA2 (\( V_{dd} = 9V \)) and x2.25 greater for BFA1 (\( V_{dd} = 0.45V \)), but this is counterbalanced by the x3 smaller \( C_{in} \) to \( C_{out} \) delay for TFA1.

BFA1 is globally the most efficient binary adder in terms of delays, PDP and \( \Sigma Di \) for the two different power supplies.

C. Delays and power according to capacitive load

We now present the performance of BFA1 according to capacitive loads and temperature. With a log-log scale, Fig. 34 presents the input to outputs delays according to \( C_L \). Fig. 35 presents the same information for \( C_{in} \) to outputs delays while Fig. 36 presents the evolution of power according to \( C_L \). Fig. 37 presents the ratio delays(\( C_L = 4fF \))/delays(0.25fF) when \( C_L \) is multiplied by 16. It is a figure of the slope of the quasi-linear evolution of delays(\( C_L \)). Fig. 38 presents the power evolution when \( C_L \) is multiplied by 16. We still have a quasi linear evolution of delay and power according to \( C_L \). However, the binary adder structure is different of the m-valued adder structures: there is one MUX for \( C_{out} \), but not a series of MUXes as in the Sum output of ternary and quaternary adders. Globally, the binary adder is more sensitive to capacitive loads than the ternary and quaternary ones.

VI. COMPARING 6-BIT, 4-TRIT AND 3-QDIGIT CPAS

Results provided in III-D, IV-C and V-C allow a detailed comparison of the performance of the different adders to
be used in a Carry-Propagate Adder. The most significant information is to compare CPAs computing the same amount of information. It is strictly the case for 6-bit and 3 quit CPAs. 4-trit input corresponds to 6.34 bits, which corresponds about to 6% more information than 6-bit or 3 quit.

Several 4-trit CPAs have been presented in the literature [3], [10], [2] and [17].

Fig. 39 compares the performance of these three CPAs with two variants: the ternary one uses 0-V_{dd}/2 and 0-V_{dd} carry swing, the quaternary one uses 0-V_{dd}/3 and 0-V_{dd} carry swing and the binary one uses V_{dd} and V_{dd}/2 power supplies. The simulation have been done with a C_L = 2 fF capacitive load and T = 25°C temperature. Other loads or temperatures would not change the results of the comparisons. From Fig. 39, the following conclusions can be deduced:

- While the binary CPA uses more full adders, its estimated chip area is half the chip area of the ternary and quaternary CPAs.
- The ternary and quaternary CPAs have less propagation delays when using full carry swing than when using V_{dd}/2 or V_{dd}/3 carry swing.
- The 0.45 V_{dd} binary CPAs has the smallest power dissipation, from 1/2 to 1/4 power dissipation of the other CPAs. While its input to sum delay is the worst one, this CPA has the lowest PDP both for sum and carry outputs.
- The quaternary CPA has a small advantage for delays with full carry swing, but the values are closed.

While ternary and quaternary CPAs have less full adders, they suffer from the large chip area and don’t provide significant advantages in term of delays. The best CPA is the binary one with V_{dd} = 0.45V supply. Reducing power supply is possible with binary circuits, but is not possible with ternary and quaternary circuits as they need a larger V_{dd} to handle the different voltage levels.

VII. CONCLUDING REMARKS

We have detailed the performance of binary, ternary and quaternary full adders that are probably close to the most performant ones. We have shown that two options are possible for these adders.

- For ternary and quaternary adders, we used two carry swings. The first one correspond to 0-1 logical values, i.e. 0-V_{dd}/2 for the ternary adder and 0-V_{dd}/3 for the quaternary adder. The second one uses the 0-V_{dd} carry swing for both adders, as carry values are always 0-1 logical values for any radix used for addition. It turns out that full carry swing reduces significantly carry propagation delays with a small power increase.
- For binary adders, we use both 0.9V and 0.45V power supplies. The smallest V_{dd} value reduces significantly
power (/4 factor), which leads to reduced PDP with a small increase in delays

The different adders are used in CPAs computing the same amount of information. In CPAs, carry propagation is the critical delay. The critical delay paths are similar for the ternary and quaternary adders. For the binary adder, it consists in a NOR gate and a MUX. With 6, 4 and 3 adders in the binary, ternary and quaternary cases, the ternary and quaternary adders should benefit from the reduced number of carry paths. It turns out that this is not the case as input to carry delays are close (they are not in the ratio 6/4/3). Input to Sum delays are also close with 0.9V $V_{dd}$ (binary) and 0.9V swing (ternary and quaternary).

The only figure for which 3-quit CPAs shows a small advantage is input to output delays with 0.9V carry swing. The ternary and quaternary CPAs are outperformed by the binary CPA with 0.45V supply in terms of power and PDP.

CPAs are circuits for which moving from binary to ternary or quaternary N-digit CPAs is simple: just replace the binary full adders by ternary or quaternary full adders. Moving from a N*N digit binary multiplier to a N*N digit ternary or quaternary multiplier is not so simple. Combination multipliers using Wallace tree reduction circuits (or equivalent ones) uses both 1-digit multipliers and adders. Ternary and quaternary multiplications generates both product and carry values while binary multiplication (AND gate) only generates 1 bit product.

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