Small-signal parameters extraction and noise analysis of CNTFETs

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Abstract
The use of carbon nanotube (CNT) field-effect transistors (FETs) in microwave circuit design requires an appropriate, immediate and efficient description of their performance. This work describes a technique to extract the parameters of an electrical equivalent circuit for CNTFETs. The equivalent circuit is used to model the dynamic and noise performance at low- and high-frequency of different CNTFET technologies, considering extrinsic and intrinsic device parameters as well as the contact resistance. The estimation of the contact resistance at the metal/ CNTs interfaces is obtained from a Y-function based extraction method. The noise model includes four noise sources: thermal noise, thermal channel noise, shot channel noise and flicker noise. The proposed model is compared with a compact model calibrated to hysteresis-free experimental data from a high-frequency multi-tube (MT)-CNTFET technology. Additionally, it has been applied to experimental data from another fabricated MT-CNTFET technology. The comparison in both cases shows a good agreement between reference data (simulation and experimental) and results from the proposed model. Low- and high-frequency noise projections of the fabricated reference device are further studied. Noise results from both studied technologies show that shot noise mainly contributes to the total noise due to the presence of Schottky barriers at contacts and along the channel.

Keywords: CNTFET, small-signal, noise, modeling

(Some figures may appear in colour only in the online journal)

1. Introduction
Nowadays, silicon (Si) based technologies dominate the high-frequency electronic market. However, these components are reaching their performance limits, causing the search for new suitable solutions for high-performance applications, such as transistor technologies based on nanostructured materials. During the last years, carbon nanotube (CNT) field-effect transistors (FETs) have been studied in order to exploit their extraordinary inherent features, e.g. high-linearity [1–4], low high-frequency noise [5, 6], quasi-ballistic transport and an outstanding gate control. Moreover, some projections refers to operation frequencies in the order of THz [7, 8], as the technological process improve and the limitations due to the fabrication are minimized (e.g. parasitics, growth methods and alignment of CNTs).

Fabricated CNTFET technologies with an extrinsic operation frequency of around 100 GHz have been reported in the literature [9–11]. These improvements have caused research efforts to develop radio-frequency (RF) applications using CNTFETs [12–15]. The design of RF circuits based on CNTFET technologies requires a reliable compact model capable to reproduce the novel and unique behavior of the devices when these are used at circuit level computer-aided
design. This compact model may help to understand and quantify the effect of parasitic elements on dynamic and noise performance. Also, this knowledge may highlight limitations in the fabrication process of the device, project ideal device performance at different bias conditions and can be useful to benchmark the device versus other technologies in specific scenarios.

The main problem related to the small-signal representation of an emergent transistor technology, such as CNTFETs, is the correct extraction of the parameters for the equivalent circuit, including the non-negligible contact resistances at metal/channel interfaces. As the development of a complete physics-based model for analog applications is challenging due to the presence of physical phenomena, such as potential barriers [13, 16] produced on the metal/CNT interface, as well as the nonlinear behavior of the charge on the tubes [3, 16], CNTFET compact modeling is usually done by a semi-physical [17, 18] or by a semi-empirical approach [19–21]19-21], the latter is the approach followed here.

In this work, the equivalent circuit and the parameters extraction procedure, including the contact resistance extraction, are described in section 2. The low- and high-frequency noise model as well as the description of the noise sources are presented in section 3. The validation of the proposed model using a reference compact model is presented in section 4. In section 5 the proposed approach is applied to experimental data from a fabricated top-gated MT-CNTFET technology. Finally some conclusions are provided in section 6.

2. Small-signal equivalent circuit and parameters extraction

2.1. Electrical equivalent circuit description

Figure 1 introduces the equivalent circuit considered in this work, which is divided into three sections. The first one is the extrinsic part, which contains the parasitic parameters of the CNTFET, caused mainly by fabrication process issues, the second one is the intrinsic part, which represents the physical transport phenomena that occur inside the device through electrical parameters and the last one includes the contact resistances, related to the interfaces between CNTs in the channel and the metallic contacts, which are specially large in CNTFETs and can not be neglected due to their large impact in device performance [22, 23]. Rgs, Rds, Lgs, Lds, and Lsd are the extrinsic resistances and inductances associated to the access metallizations of the device for the gate, drain and source, respectively. Cgd1 and Cgd2 are the parasitic capacitances between gate and drain Cds1 and Cds2 between drain and source and Cgd1 and Cgd2 between gate and source. Rgs, Rds, and Rsd are the contact resistances at the drain and source, respectively. In contrast to the parasitic parameters, contact resistances can not be de-embedded using standard procedures and are one of the most important CNTFETs fabrication issues, associated to Schottky barriers at the contacts [16], hence, in order to model accurately, the effect of contact resistances must be taken into account. The parameters related to the intrinsic part of the device are described as follows: gds is the channel or output conductance and gms is the transconductance, Cds, Cgs and Cgd represent the intrinsic capacitances between the gate, drain and source and Vgs is the intrinsic voltage between gate and source.

In figure 2, each parameter of the equivalent circuit is associated to the components of the cross-section schematic view for a top-gated CNTFET.

2.2. Extraction of the extrinsic parameters

A small output signal of a CNTFET used as an amplifier, an immediate analog application, can be easily affected by the parasitic elements. Thus, it is important to know appropriately the contribution of the extrinsic parameters and separate their contribution from that produced by the intrinsic parameters.

In order to extract correctly the extrinsic parameters of the device, it is necessary to use an accurate de-embedding procedure. The three-step parasitic de-embedding method is
synthesized as in [24, 25] by equations (1)–(4)

\[
Y_{\text{Dem}} = ((Y_{\text{Raw}} - Y_{E})^{-1} - Z_{S})^{-1} - Y_{I},
\]

(1)

\[
Y_{\text{Open}} = ((Y_{E})^{-1} + Z_{S})^{-1} + Y_{E},
\]

(2)

\[
Y_{\text{Short}} = (Z_{S}^{-1}) + Y_{E},
\]

(3)

\[
Y_{\text{Pad}} = Y_{E},
\]

(4)

where \(Y_{\text{Open}}, Y_{\text{Short}}\) and \(Y_{\text{Pad}}\) are the \(Y\)-parameters of an open, short and thru test structure, respectively. \(Y_{E}, Y_{I}\) and \(Z_{S}\) are the admittance outer-parasitics matrix, the admittance inner-parasitics matrix and the series-impedance parasitics matrix, respectively, (see figure 2 and equations (17)–(19) in [24]). \(Y_{\text{Dem}}\) represents the de-embedded \(Y\)-parameters. The three-step parasitic de-embedding method has been considered suitable to be applied to CNTFET characterization due to the high operation frequency expected in this technology [7–11] where an appropriate de-embedding method can improve accuracy of the device experimental data [24, 26].

Notice that the extracted extrinsic parameters do not consider the contribution of the contact resistances at the source and drain sides since these resistances are produced on the interface between CNTs and contact metallizations. Therefore, in order to have an accurate model for CNTFETs, the contribution of contact resistances is required to be removed by an additional process.

### 2.3. Contact resistance extraction

The total contact resistance \((R_{C} = R_{sc} + R_{ds})\) is an electrical representation of the physical phenomena at the junction metal/CNT at both drain and source contacts. This is one of the main issues that limits CNTFETs performance, thus it has to be considered in an accurate model. Also, an appropriate extraction can provide information about the contact quality to improve fabrication process and to project the performance of an optimized technology.

In order to perform an accurate extraction of the contact resistance of CNTFETs, a \(Y\)-function based method, labeled as YFM2 in [27], has been considered. In contrast to the transfer length method (TLM), YFM2 does not require long CNT test structure [22] and only standard transfer characteristics in the linear region and at low drain bias of the device are required to extract \(R_{C}\). Also, a physics-based validation has been provided for this method in [27]. Despite the extracted resistance is not bias dependent, it can be considered as a reference value for near bias points as well as an upper limit value of \(R_{C}\) for the device working in the active region.

As is stated in [27], in YFM2 the \(R_{C}\) is extracted from the slope of \(\theta = \theta_{0} + R_{C}\beta\) once \(\beta, \theta\) and \(\theta_{0}\) the degradation factor of low-field carrier mobility and the extrinsic and intrinsic reduction mobility carrier coefficient, respectively, are extracted from the \(Y\)-function obtained from the drain current equation described in [27] (see equations (3) and 9 in [27]).

\(^{5}\) Notice that the \(Y\)-function is defined as \(Y = \frac{I_{D}}{V_{G}}\) and has no relation with the admittance parameters discussed along this manuscript.

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### 2.4. Intrinsic parameters extraction

By considering the \(\Pi\)-like topology of the intrinsic part of the equivalent circuit shown in figure 1, the admittance \(Y\)-parameters have been used to characterize the two port network representation of the CNTFET as follows:

\[
Y_{I}(\omega) = \begin{bmatrix}
    y_{11,i} & y_{12,i} \\
y_{21,i} & y_{22,i}
\end{bmatrix}
\]

(5)

From which the intrinsic parameters can be obtained:

\[
g_{m} = \text{Re}(y_{21,i}),
\]

(6)

\[
g_{d} = \text{Re}(y_{22,i}),
\]

(7)

\[
C_{d} = \frac{\text{Im}(y_{22,i})}{\omega} - C_{gs},
\]

(8)

\[
C_{gd} = C_{gs} = -\frac{\text{Im}(y_{12,i})}{\omega}.\]

(9)

Notice that the device electrostatics is considered symmetrical, i.e. \(C_{gd}\) is identical to \(C_{gs}\).

In contrast to previous works [19–21], the approach used here is based on linear matrices in order to remove the contribution of the contact resistances from the de-embedded parameters. As figure 3 shows, \([Z_{R_a}]\) is connected in series with the intrinsic part \([Y]\), while \([ABCD_{R_a}]\) is connected in a cascade topology.

Then, using the following equations, where the operator \(\Rightarrow\) implies a matrix transformation, intrinsic admittance parameters can be obtained from de-embedded parameters

\[
[Z_{I,R_a}] = [Z_{\text{Dem}}] - [Z_{R_a}],
\]

(10)

\[
[Z_{I,R_a}] \Rightarrow [ABCD_{I,R_a}],
\]

(11)

\[
[ABCD_{I}] = \frac{[ABCD_{I,R_a}]}{[ABCD_{R_a}]}.
\]

(12)

\[
[ABCD_{I}] \Rightarrow [Y].
\]

(13)
3. Low- and high-frequency noise model for CNTFETs

Four different noise sources have been considered in this work: thermal noise associated to resistive elements, shot channel noise due to the Schottky junctions, thermal channel noise associated to an equivalent noise temperature and flicker noise ($1/f$), mostly present at low frequencies. Details related to each noise source are presented below.

3.1. Thermal noise in resistive elements

The thermal noise in resistive elements of the equivalent circuit, as a result of the movement of the free carriers inside the conductive material [28], can be described by its power spectral density as:

$$S_T = \frac{I^2_R}{\Delta f} = \frac{4k_B T}{R},$$

where $k_B$ is the Boltzmann constant, $R$ is the resistance, $\Delta f$ is the noise bandwidth, which is considered equal to one for all cases in this work and $T$ is the absolute temperature. Each resistance present in the equivalent circuit has a characteristic power spectral density to describe its produced thermal noise.

3.2. Shot channel noise

The carrier injection in CNTFETs will be affected as a consequence of the potential barriers in the channel [5, 29, 30]. The carrier injection through the potential barrier, when a low carrier density is present in the channel, follows a Poisson’s probability distribution. The result is a power spectral density associated to the shot noise represented in equation (15) where $q$ is the electron charge, $I_D$ is the drain current and $F$ the Fano factor, which represents the compression of the shot noise as a result of the correlation between successive carrier injections in the potential barriers [31]. When no correlation exists $F$ is equal to one, as it has been considered in this work

$$S_{\text{shot}} = \frac{I^2_{\text{shot}}}{\Delta f} = 2qI_D F.$$  

3.3. Thermal channel noise

The relaxed channel length (e.g. $L_{ch} > 300$ nm) [1, 9, 32] and the large density of tubes in high-frequency CNTFETs, as well as the bias near saturation required for the dynamic performance of these devices, induce the activation of scattering mechanisms of acoustic and optical phonons, hence, non-ideal ballistic transport exists in these devices and the channel resistance cannot be neglected [27]. As a result of this channel resistance, thermal channel noise spectral power density is considered as in the Pospieszalski model [33]. The corresponding expression, based on drift-diffusion theory and applied here to CNTFETs due to the transport conditions described above, is shown in equation (16)

$$S_{\text{ThCh}} = \frac{I^2_{\text{ThCh}}}{\Delta f} = 4k_B T_d g_{ds}.$$  

An equivalent noise temperature ($T_d$), associated to the output conductance, is needed to describe the thermal channel noise. Equation (17) describes the equivalent noise temperature $T_d$ [34], as it can be noticed, $T_d$ is independent to the frequency and only depends on the room temperature and the relation between $g_m$ and $g_{ds}$

$$T_d = \left(1 + \frac{g_m}{g_{ds}}\right) T_{\text{amb}}.$$  

Considering a model for thermal noise in the channel explicitly for CNTFETs in this study contrasts with other approaches where such phenomenon is not considered [5, 6] or is implicit in the description of the transport through a transmission probability [17, 18].

3.4. Flicker noise ($1/f$)

Flicker noise presents an inversely proportional power spectral density as a function of the frequency. Previous studies refer that flicker noise is specially large in CNTFETs [30, 35–37] and it is related to the total number of charge carriers [35].

The power spectral density of the flicker noise is described in equation (18). In this equation $A_H$ represents the noise amplitude which scales the noise contribution and is equal to the relation between the Hooge’s constant ($\alpha_H$), dependent on the scattering channel mechanisms, and the number of charge carriers in the channel ($n$) [38]. On the other hand, $A_H$ is an empirical parameter which is commonly in the order between $10^{-4}$ and $10^{-3}$ for non-optimized materials [39] as is the CNTFETs case. For this work the chosen value was $A_H = 2 \times 10^{-4}$. Notice that a dominant mobility variation mechanism has been considered here to describe the flicker noise

$$S_{1/f} = \frac{I^2_{1/f}}{\Delta f} = A_H \frac{I_D^2}{f} = \frac{\alpha_H I_D^2}{n} f.$$  

Once that all proposed noise sources are known these can be added to the electrical equivalent circuit as shown figure 4. As it can be noticed, the considered noise model is related to the small-signal model presented before and as a result of that, accurate projections for dynamic and noise CNTFETs performance are only possible if all parameters are extracted appropriately. Thus, a correct extraction of contact resistance is mandatory in order to achieve a good approximation to CNTFETs performance.
4. Validation of the proposed model using a reference compact model

4.1. Initial reference data

The compact model used as a reference in this work [17, 18], which is called CCAM, has been originally calibrated to hysteresis-free experimental data from a CNTFET technology presented elsewhere [32]. Specifically, the top-gated device used as a reference for this work has a device channel length ($L_{ch}$) of around 700 nm and a gate length ($L_{g}$) of around 250 nm. The device has eight gate fingers of 50 μm each one forming a total device width ($w_{g}$) of approximately 400 μm. The semiconducting-to-metallic (s:m) CNT ratio is 3:1 with around 3000 CNTs randomly distributed in channel and grown via chemical vapor deposition (CVD) on SiO₂. Metallic contacts of the device are made from Pd/Ti. Details on the fabrication process can be found in [32].

In order to perform the extraction of the associated equivalent circuit parameters, results obtained from the reference compact model have been used. The contribution of metallic tubes has been turned-off for this study in order to work with the best-case scenario. The bias point has been chosen at $V_{GS} = 1$ V and $V_{DS} = 3$ V since an optimal high-frequency performance has been found out for this technology under such conditions [12]. The transit frequency ($f_t$) and maximum oscillation frequency ($f_{max}$) obtained with the reference model for the considered DC bias point are 9.8 GHz and 27.9 GHz, respectively. By using CCAM, the S-parameters of the device have been simulated from 1 to 30 GHz as shown in figure 5. These results have been used as the starting point to extract the parameters of the equivalent circuit (see figure 1) for this device by using the methodology presented in section 2.

4.2. Parameters extraction results

In this case, the extrinsic parameters have been obtained directly from CCAM, where access resistances and inductances have been neglected, since pad-de-embedding data is used for the original calibration [17]. The extrinsic parameters are summarized in table 1.

Regarding to the contact resistance extraction, figure 6 shows the transfer characteristics of the device simulated with the reference compact model. Red lines in figure 6 represent the drain current calculated with a drift-diffusion approach (see equation (3) in [27]) considering $R_C \sim 39 \Omega$, extracted using YFM2.

The device exhibit an n-type behavior, i.e. carriers are injected from the source to the channel, which causes a larger impact of the potential barrier at the source on the device performance. Considering the latter, a distribution of the total contact resistance is proposed as follows: $R_k = 12 \Omega$ and $R_{sc} = 27 \Omega$. These values are confirmed by a fitting procedure involving the noise performance developed in section 4.3.
Then intrinsic parameters have been extracted following the proposed procedure (see section 2.4). Parameters of the extracted equivalent circuit are summarized in table 1.

In order to demonstrate the feasibility of the extracted transconductance and output conductance, these have been described properly different FET technologies, regardless the channel length, in saturation and linear regimes [40]

\[
g_m' = \frac{g_m'}{1 - g_m'R_s - g_m'R_d(R_s + R_d)}, \quad (19)
\]

\[
g_{ds} = \frac{g_{ds}'}{1 - g_m'R_s - g_m'R_d(R_s + R_d)}. \quad (20)
\]

\(g_m'\) and \(g_{ds}'\) can be obtained from de-embedded data (\(\text{Y}_{\text{Dem}}\), see equation (1)) using equations (6) and (7), respectively. In this case, as a result of the hysterisis-free data, \(g_m'\) and \(g_{ds}'\) can also be obtained from DC curves. A comparison between extracted and calculated results of \(g_m\) and \(g_{ds}\) shows that both results are equal, therefore both approaches to obtain these intrinsic parameters are valid.

Notice that the charge and current transport are described in this work by relations based on the admittance device parameters (see equations (6)–(9)) in contrast to CCAM where such phenomena have been described by semi-empirical expressions. Hence, the approach presented here is expected to be more efficient for immediate characterization purposes.

### 4.3. Results and discussion

The corresponding simulation of the electrical equivalent circuit has been implemented using Keysight Advanced Design System (ADS) from the extracted values of the table 1. The considered bias point is \(V_{\text{GS}} = 1\) V and \(V_{\text{DS}} = 3\) V resulting in \(I_D = 0.015\) A.

At frequencies up to \(f_i\), which is around 9.8 GHz, the performance of \(S\)-parameters is similar for both CCAM and the extracted equivalent circuit. However, at frequencies higher than \(f_i\), the difference between results from CCAM and from the equivalent circuit increases (not shown here). Due to this difference, mainly caused by extrinsic parameters, an optimization has been performed in order to find a good agreement. The optimization procedure consists in minimizing the difference between dynamic and noise results from the proposed model and reference data by fitting only intrinsic parameters, this has been done using the optimization tools of ADS based on a least-squares error-function [41, 42]. Extracted and optimized parameters for the electrical equivalent circuit are compared in table 1.

Table 1 shows that only two extrinsic parameters have changed as a result of the optimization process. A good agreement has been found for results from CCAM and from the proposed equivalent circuit for \(S\)-parameters as well as for noise parameters (only \(NF\) and \(NF_{\text{min}}\) are shown here) when optimized values are considered as shown in figures 7(a) and (b). A correct distribution of the total contact resistance allows a good agreement of \(S\)-parameters and noise results from equivalent circuit and from CCAM. From figure 7(b) it can be observed that a good agreement between equivalent circuit and CCAM has been found for frequencies commonly used for circuit design @2.4/5 GHz: for the proposed model \(NF = 8.58/8.59\) dB and \(NF_{\text{min}} = 1.46/2.67\) dB while for CCAM \(NF = 8.84/8.47\) dB and \(NF_{\text{min}} = 1.29/2.29\) dB.

From noise results depicted in figure 8 it has been shown that shot noise mainly contributes to the total noise over all frequency range. This trend has been reported in [6, 30, 43], while flicker noise does at low frequencies, the same trend has been found in [30, 35–37].

### 5. Characterization of a fabricated device

The proposed methodology and model have been also applied to experimental data from a fabricated top-gated MT-CNTFET which is detailed in [19]. Extrinsic transit frequency \(f_{\text{t,i}}\) and extrinsic maximum oscillation frequency \(f_{\text{max,e}}\) obtained from measured \(S\)-parameters are \(\sim 5\) GHz and \(\sim 9\) GHz, respectively. An intrinsic \(f_{\text{t,i}} \sim 30\) GHz has been
calculated for the device in [19]. The device has a gate length of 700 nm and channel width of 100 μm, its channel incorporates a large number of aligned SW-CNTs grown by CVD with a nanotube density of 5 CNTs/μm and a s:m ratio of 3:1. Metallic contacts were made from Ti/Au by a photolithography process in a ground-signal-ground (GSG) configuration. The transistor has a p-like behavior and the chosen bias point was $V_{DS} = -1$ V and $V_{GS} = 0$ V. Measurements on test ‘open’ structures have been reported in [19].

Contact resistances have been extracted from transfer characteristics obtained using reported measured output characteristics [19]. It is important to notice that the value of contact resistance has not been reported and hysteresis has been neglected in [19]. Figure 9 shows transfer characteristics of the device and the $I_D$ calculated with the YFM2 method [27]. The extracted value of contact resistance was $R_C \approx 74.9 \, \Omega$ and the contribution of each contact has been considered as identical, i.e., $R_{dc} = R_C = R_C/2$.

A comparison between the $S$-parameters obtained from the proposed model and experimental data from [19] is shown in figure 10. A good agreement has been achieved using the proposed methodology and the optimizing process in which only four extrinsic parameters have been fitted. In contrast with the equivalent circuit in [19], whose parameters have been extracted only by fitting the data and no extrinsic parameters have been treated, in this work an extraction procedure for both the intrinsic and the extrinsic parameters along contact resistances, has been considered. Table 2 shows extracted values and a comparison with the equivalent circuit values in [19].

Moreover, the noise model provides the projection of the device noise performance as shown in figure 11. Experimental noise data reported in [6] for a device from the

![Figure 8](image_url)

**Figure 8.** (a) $NF$ and (b) $NF_{\text{min}}$ for: CCAM (solid black lines), equivalent circuit with the four noise sources (dotted red lines in the electronic version), without $1/f$ noise (cut blue lines in the electronic version), without $1/f$ nor thermal channel noise (cut-dotted green lines in the electronic version) and without $1/f$ noise nor thermal channel noise nor shot noise (dotted gray lines).

![Figure 9](image_url)

**Figure 9.** Transfer characteristics extracted from output measured characteristics of a MT-CNTFET reported in [19] (black markers) and $I_D$ calculated using the extracted values from YFM2 considering $R_C \approx 74.9 \, \Omega$ (solid red lines).

![Figure 10](image_url)

**Figure 10.** Comparison of the $S$-parameters from measurements in [19] and obtained with the optimized equivalent circuit. The bias point is $V_{DS} = -1$ V and $V_{GS} = 0$ V.

![Figure 11](image_url)

**Figure 11.** (a) $NF$ and $NF_{\text{min}}$ of the device reported in [19] obtained with the proposed noise model and (b) comparison of the $h_{21}$ between experimental data from [19] and the equivalent circuit and equivalent circuit without extrinsic parameters. The bias point is $V_{DS} = -1$ V and $V_{GS} = 0$ V.
An equivalent circuit to model the low- and high-frequency parameters for the reference fabricated device [19].

| Parameter | Extracted value | Optimized value | Reported value [19] |
|-----------|-----------------|-----------------|---------------------|
| \( g_{m} \) (mS) | 5.32 | 5.32 | 3.8 |
| \( g_{d} \) (mS) | 2.69 | 2.69 | 1.92 |
| \( C_{gd1} \) (fF) | 11.90 | 11.90 | 52 |
| \( C_{gd2} \) (fF) | 11.90 | 11.90 | 65 |
| \( C_{ds} \) (fF) | 17.75 | 17.75 | 15 |

Contact resistance

| Parameter | Value (Ω) |
|-----------|-----------|
| \( R_{sc} \) | 37.45 |
| \( R_{dc} \) | 37.45 |

Extrinsic part

| Parameter | Value (Ω) |
|-----------|-----------|
| \( R_{gs} \) | 16 |
| \( R_{ua} \) | 0 |
| \( R_{da} \) | 24 |
| \( C_{gd11} \) (fF) | — |
| \( C_{gd21} \) (fF) | 68 |
| \( C_{gd12} \) (fF) | 12 |
| \( C_{gd22} \) (fF) | — |
| \( L_{gd1} \) (pH) | 50 |
| \( L_{gd2} \) (pH) | 50 |

Moreover, noise performance has been simulated giving insights about the expected performance of the device. The intrinsic part of the proposed equivalent circuit for this technology is also able to reproduce closely the expected performance of the device if parasitics were not considered.

Finally, the proposed methodology can be applied to other emergent technologies with large contact resistance because this approach properly considers the effect of the contact resistance in device performance. Moreover a procedure to obtain and remove its contribution in order to extract accurately the intrinsic part of the equivalent circuit has been provided.

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