Electrostatic characteristics of a high-\(k\) stacked gate-all-around heterojunction tunnel field-effect transistor using the superposition principle

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Abstract

We use the superposition method to model the electrostatic characteristics of a high-\(k\) stacked gate-all-around heterojunction tunneling field-effect transistor (TFET). The heterojunction is formed from Ge/Si material in the source/channel, respectively. The modeling is accomplished by considering the space-charge regions at the source–channel and drain–channel junctions and in the channel region. The surface potential in the channel region is obtained by applying the superposition principle derived in the source/drain region by solving the two-dimensional (2D) or one-dimensional (1D) Poisson’s equation, respectively. Furthermore, the electric field and the drain current are modeled by using the surface potential and the Kane model, respectively. The results are confirmed using ATLAS technology computer-aided design (TCAD) simulations.

Keywords

Gate-all-around tunnel field-effect transistor · Heterojunction · Superposition principle · Surface potential · Electric field · Drain current · TCAD

1 Introduction

Following years of continuous downscaling, transistors based on complementary metal–oxide–semiconductor (CMOS) have suffered from deterioration of the subthreshold swing (SS), the leakage current, and the threshold voltage (VT) [1–3]. In addition, the power crisis faced by device engineers led to the emergence of multigate/gate-all-around FETs, group III–V-based FETs, super-steep subthreshold slope FETs, and graphene/Carbon-nanotube-based FETs. The tunnel FET is one such device which has attracted attention from researchers because of its low subthreshold swing (<60 mV/decade) and reduced short-channel effects [4, 5]. A three-terminal \(p-i-n\) device, where the source and drain are oppositely doped while the channel is either intrinsically or lightly doped, is called a TFET. Such a device has two junctions, namely the drain–channel junction (JDC) and source–channel (JSC). The carrier transport in a TFET is controlled by band-to-band tunneling (BTBT) rather than thermionic emission as in metal–oxide–semiconductor FETs (MOSFETs). Although such devices exhibit low SS and \(I_{OFF}\) values, they also suffer from low \(I_{ON}\) and ambipolar conduction [6, 7]. In this regard, alternative approaches such as gate engineering (i.e., employing multigate/gate-all-around structures) [8–10], gate dielectric engineering (i.e., making use of high-\(k\) material for the gate dielectric) [11], work function engineering (i.e., employing asymmetric instead of symmetric gate work functions) [12], tunnel engineering (i.e., introducing a heavily doped source pocket at the JSC such that its completely depleted) [13], and materials engineering (i.e., using lower-bandgap materials such as InAs, GaAs, InGaAs, SiGe, or Ge as an alternative to Si) [14] have been proposed to mitigate the shortcomings of TFETs.

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Over the decades, various analytical models have been reported for the electrical parameters, in particular the surface potential, electric field, threshold voltage, and drain current, of single/double-gate and GAA TFETs [15–17] with single/dual-material gate (SMG/DMG) electrodes. The electrical results for such devices were examined by Verhulst et al. [15]. The 2D electrostatic response of DG and GAA TFETs was reported by Pan et al. [16]. Vishnoi et al. [17] proposed the BTBT current model for DG-GAA-TFETs, irrespective of the depletion regions at the JSC and JDC, by using pseudo-2D analytical modeling. The DMG in a DG-TFET exhibits better drive current and SS than its SMG counterpart according to Kumar et al. [12] and Jain et al. [18]. Kumar et al. [19] and Prabhat et al. [20] reported modeling of the drive current and surface potential of the DMG for SG/DG TFET structures, respectively. The device performance can be enhanced by replacing SiO$_2$ with pile-up SiO$_2$ and a high-$k$ dielectric in DG TFETs, as reported by Kumar et al. [21]. The proposed Ge-Si–Si hetero stacked gate dielectric GAA-TFET device provides better $I_{ON}$ per unit area than counterpart planar devices. Hence, developing an accurate model for the surface potential, electric field, and drain current becomes important.

The model is validated against previously published reports [31] and three-dimensional (3D) numerical simulations [22]. The remainder of this manuscript is presented as follows: Sect. 2 and 3 discuss the device architecture and results, followed by the conclusions.

## 2 The device structure

Figures 1 and 2 show 3D and 2D views of the proposed Gate All Around Heterojunction Tunnel Field Effect Transistor (GAA HJTFET), where the high-$k$ dielectric is deposited on top of the low-$k$ dielectric. The device specifications are presented in Table 1. Three depletion regions are considered in the modeling, namely regions I, II, and III, corresponding to the source–channel, channel, and drain–channel, respectively. The lengths of these regions are considered to be $L_1$, $L_2$, and $L_3$. The potentials across the corresponding regions are $\psi_0$, $\psi_1$, $\psi_2$, and $\psi_3$.

Figure 3 depicts the band profile of the proposed device. When $V_{GS} = 0$ V (OFF-state) the interband tunneling is inhibited, so no electrons tunnel through the depletion region at $J_{SC}$. When $V_{GS} = 1$ V (ON-state) the energy bandgap reduces and interband tunneling is permitted, which allows electrons to tunnel from the source to the channel. The tunneling rate of electrons is high in hetero- compared with homojunction devices due to the narrow-bandgap materials at the source.

### Table 1: The parameter values used for the high-$k$ stacked GAA-HJTFET

| S. no. | Symbol | Description | Value |
|---|---|---|---|
| 1 | $N_S$ | Source doping concentration ($P^+$) | $1 \times 10^{20}$ cm$^{-3}$ |
| 2 | $N_C$ | Channel concentration ($N^-$) | $1 \times 10^{16}$ cm$^{-3}$ |
| 3 | $N_D$ | Drain concentration ($N^+$) | $5 \times 10^{18}$ cm$^{-3}$ |
| 4 | $L_2$ | Channel length | 50 nm |
| 5 | $\phi_{mA}$ | Work function of gate | 4.3 eV |
| 6 | $\varepsilon_{ox}$ | Thickness of SiO$_2$ | 1 nm |
| 7 | $\varepsilon_{k}$ | Thickness of HfO$_2$ | 2 nm |
| 8 | $\varepsilon_{Si}$ | Thickness of Si | 13 nm |
| 9 | $\varepsilon_{a}$ | Permittivity of air | $8.854 \times 10^{-14}$ F/cm |
| 10 | $\varepsilon_{SiO_{2}}$ | Permittivity of Si | 11.9$\varepsilon_0$ |
| 11 | $\varepsilon_{SiO_{2}}$ | Permittivity of SiO$_2$ | 3.9$\varepsilon_0$ |
3 The derivation of the model

Figure 2 shows a 2D view of the device considered in the modeling. The coordinates of the device are denoted by the z- and r-axes, and the junction potentials are given by $\psi_0$, $\psi_1$, $\psi_2$, and $\psi_3$ at $z = 0$, $z_1 = L_1$, $z_2 = L_1 + L_2$ and $z_3 = L_1 + L_2 + L_3$.

3.1 The modeling of the potential in the channel

The distribution of the potential in the gate-all-around device is the same as that in the double-gate device structure. The tubular symmetry of the proposed device means that the surface potential is independent of the angular coordinate. Thus, the 2D Poisson equation in cylindrical coordinates is considered for the modeling, being given in the channel region by

$$\frac{1}{r} \frac{\partial}{\partial r} \left( r \frac{\partial \psi_{ch}(z, r)}{\partial r} \right) + \frac{\partial^2 \psi_{ch}(z, r)}{\partial r^2} = \frac{q}{\varepsilon_{Si}} \eta, \quad (1)$$

where $\psi_{ch}(z, r)$ is the potential across the channel and $\varepsilon_{Si}$ is the permittivity of silicon. The charge density of mobile carriers across the channel is expressed as

$$\eta = \eta_i \exp \left( \frac{\psi_{ch}(z, r) - V_{T}}{U_T} \right), \quad (2)$$

where $\eta_i$ is the intrinsic carrier concentration, $U_T = \frac{kT}{q}$ is the thermal voltage at 300 K, and $V$ is the nonequilibrium quasi-Fermi level with respect to the Fermi level of the source region, with the boundaries given by [23].

Thus, the 2D Poisson equation in cylindrical coordinates is

$$V(0, r) = 0 \quad (3)$$

$$V(L_2, r) = V_{DS}. \quad (4)$$

The quasi-Fermi level is almost constant in the radial direction [24]. $V_{DS}$ is approximated by be drain–source voltage along the channel, except at the left end of the channel. At the channel, the electrostatic potential boundary conditions are

$$C_{ox} [V_{GS} - \varphi_{ms1,i} - \psi_{ch}(z, r = r_0)] = \varepsilon_{Si} \left. \frac{\partial \psi_{ch}(z, r)}{\partial r} \right|_{r=r_0} \quad (5)$$

$$\psi_{ch}(0, r) = \varphi_{0s} \quad (6)$$

$$\psi_{ch}(L, r) = \varphi_{0d} \quad (7)$$

where $C_{ox}$ is the capacitance of the dielectric per unit area.

$$C_{ox} = \frac{\varepsilon_{ox}}{r_0 \ln \left( 1 + \frac{r_o}{r_0} \right)}, \quad (8)$$

where $r_0 = \frac{L_3}{2}$, $\varphi_{ms1,i}$ is the work function of the gate with respect to the silicon material

$$\varphi_{ms1,i} = \varphi_m - \left( \chi_{Si} + \frac{E_{gSi}}{2q} \right), \quad (9)$$

$\varphi_m$, $\chi_{Si}$, $E_{gSi}$, $\varphi_{0s}$, and $\varphi_{0d}$ are the work function of the gate, the electron affinity of Si, the energy bandgap of Si, and the potentials at the left and right end, respectively.

$$\psi_{ch}(z, r) = \phi_1(r) + \phi_2(z, r) \quad (10)$$

where $\phi_1(r)$ is the solution of the 1D Poisson’s equation obtained as shown below:

$$\frac{1}{r} \frac{\partial}{\partial r} \left( r \frac{\partial \phi_1(r)}{\partial r} \right) = \frac{q}{\varepsilon_{Si}} \eta_i \exp \left( \frac{\phi_1(r) - V}{V_T} \right). \quad (11)$$

The boundary condition at the silicon–dielectric interface is

$$C_{ox} [V_{GS} - \varphi_{ms} - \phi_1(r = r_0)] = \varepsilon_{Si} \left. \frac{df_1(r)}{dr} \right|_{r=r_0} \quad (12)$$

where $f_1(r)$ is the solution of the 1D Poisson’s equation obtained as shown below:

$$\frac{df_1(r)}{dr} \bigg|_{r=0} = 0 \quad (13)$$

Using Eqs. (12) and (13), the 1D potential is obtained as

Fig. 3 The energy band profile of the proposed GAA-HJTFET
\[ \phi_1(r) = V + U_T \ln \left( \frac{8B \varepsilon_{Si}}{qn_i (Br^2 + 1)} \right). \tag{14} \]

Substituting Eq. (14) into Eq. (12) yields

\[ B \frac{V_{GS} - \varphi_{mx}}{U_T} - \ln \left( \frac{8B \varepsilon_{Si}}{qn_i (Br^2 + 1)} \right) = - \frac{4BU_T r}{C_{ox} (Br^2 + 1)}. \tag{15} \]

From Eq. (10), the solution \( \phi_2(z, r) \) to the 2D potential equation is obtained from the residual 2D equation

\[ V^2 \phi_2(z, r) = \frac{q}{\varepsilon_{Si}} \times n_i \exp \left( \frac{\phi_1(r) - V}{U_T} \right) \times \left[ \exp \left( \frac{\phi_2(z, r)}{U_T} \right) - 1 \right]. \tag{16} \]

The boundary conditions to be satisfied by \( \phi_2(z, r) \) are [23]

\[ \phi_2(0, r) = \varphi_{os} - \phi_1(r) \tag{17} \]

\[ \phi_2(L, r) = \varphi_{OD} - \phi_1(r) \tag{18} \]

\[ C_{ox} \left[ -\phi_2(z, r = r_0) \right] = \varepsilon_{Si} \left. \frac{\partial \phi_2(z, r)}{\partial r} \right|_{r=r_0}. \tag{19} \]

Assuming \( \phi_2/U_T \) is small, Eq. (16) reduces to the 2D Laplace equation. This approximation is valid for TFETs [25]. The separation-of-variables method is used to derive \( \phi_2(z, r) \), yielding the expression

\[ \phi_2(z, r) = \left[ C_0 e^{\frac{z}{2}} + C_1 e^{-\frac{z}{2}} \right] J_0(\lambda, r), \tag{20} \]

where \( J_0(\lambda) \) is the Bessel function of the first kind of the order \( i \). Using Eq. (20) in Eq. (18) gives the relation for the separation factor \( \lambda \) (which should be a positive value)

\[ \frac{r_0}{\varepsilon_{Si}} = \lambda \frac{J_1(\lambda)}{J_0(\lambda)}. \tag{21} \]

Consider \( C_s = C_{ox} \frac{r_0}{\varepsilon_{Si}} \). Applying the boundary conditions in Eqs. (17) and (18) to Eq. (20) yields the expression for the coefficient in Eq. (20) (a detailed derivation is given in the Appendix).

\[ C_0 = \left( \frac{1}{2N \sinh \left( \frac{\mu c}{r_0} \right)} \left[ \frac{J_1(\lambda)}{\lambda} (\varphi_{OD} - \varphi_{OS}) \exp \left( - \frac{L \lambda}{r_0} \right) \right] + S V_a \right). \tag{22} \]

\[ C_1 = \frac{1}{2N \sinh \left( \frac{\mu c}{r_0} \right)} \left[ \frac{J_1(\lambda)}{\lambda} \left( \varphi_{OS} \exp \left( \frac{L \lambda}{r_0} \right) - \varphi_{OD} \right) \right] + S V_a. \tag{23} \]

Based on the device dimensions, \( S_1, S_2 \), and \( N \) are given by

\[ S_1 = \exp \left( - \frac{L \lambda}{r_0} \right) - 1 \tag{24} \]

\[ S_2 = 1 - \exp \left( \frac{L \lambda}{r_0} \right) \tag{25} \]

\[ N = \frac{J_1^2(\lambda)}{2} \left[ \left( \frac{C_s}{\lambda} \right)^2 + 1 \right] \tag{26} \]

The total potential across the channel of the proposed device is obtained by adding the potential terms given by Eqs. (14) and (20).

### 3.2 The modeling of the potential in the depletion region of the source

The depletion region across the source cannot be neglected for higher voltages, so the voltage drop across this region must be considered. The 2D Poisson’s equation in region R1 is given by

\[ \frac{1}{r} \frac{\partial}{\partial r} \left( r \frac{\partial \phi_1(z, r)}{\partial r} \right) + \frac{\partial^2 \phi_1(z, r)}{\partial z^2} = \frac{qN_A}{\varepsilon_{Si}} - L_1 \leq z \leq 0 \tag{27} \]

where \( \phi_1(z, r) \) is the electrostatic potential with respect to the Fermi level in the source region and \( N_A \) is the doping concentration in the source. The electrostatic potential along the \( r \) direction can be approximated by a parabolic equation [26].

\[ \phi_1(z, r) = \phi_0(z) + \frac{1}{2} A_1 (z) r + A_2(z) r^2. \tag{28} \]

The boundary conditions used to obtain the coefficient of the parabolic approximation equation are

\[ \phi_1(z, r) = \phi(z) \tag{29} \]

\[ \left. \frac{\partial \phi_0(z, r)}{\partial r} \right|_{r=0} = 0 \tag{30} \]

\[ C_f \left[ V_{GS} - \varphi_{mx,i} - \varphi(z) \right] = \varepsilon_{Si} \left. \frac{\partial \phi_1(z, r)}{\partial r} \right|_{r=r_0} \tag{31} \]
where $C_r = \frac{2}{3} C_{ox}$ is the fringing field effect considered by conformal mapping techniques as in Ref. [27]. Applying the boundary conditions to Eq. (28), we obtain the coefficient as

$$A_0(z) = -\frac{r_0 C_{ox}}{\pi \varepsilon_{Si}} (V_{GS} - \varphi_{ms}) + \left(1 + \frac{r_0 C_{ox}}{\pi \varepsilon_{Si}}\right) \phi_1(z)$$

(32)

$$A_1(z) = 0$$

(33)

$$A_2(z) = \frac{C_{ox}}{\pi r_0 \varepsilon_{Si}} (V_{GS} - \varphi_{ms} - \varphi_s(z))$$

(34)

Substituting $A_0(x)$, $A_1(x)$, and $A_2(x)$ into the parabolic approximation in Eq. (28) gives

$$\frac{\partial^2 \varphi_s(z)}{\partial z^2} - \frac{4C_{ox}}{\pi r_0 \varepsilon_{Si}} \varphi_s(z) = \eta,$$

(35)

where $\eta = \frac{q N_s}{\varepsilon_{Si}} - \frac{1}{K_d} (V_{GS} - \varphi_{ms}), K_d = \sqrt{\frac{\varepsilon_{Si} C_{ox}}{4C_{ox}}}.$

The general solution of Eq. (35) is

$$\varphi_s(z) = B_0 \exp \left(\frac{z + L_1}{K_d}\right) + B_1 \exp \left(-\frac{z + L_1}{K_d}\right) + \eta.$$  

(36)

The expression for $\phi_s$ must satisfy the following boundary conditions:

$$\varphi_s(0) = \phi_{0s}$$

(37)

$$\varphi_s(-L_1) = -U_T \ln \left(\frac{N_A}{n_i}\right)$$

(38)

$$\left.\frac{d\varphi_s(z)}{dz}\right|_{z=-L_1} = 0$$

(39)

On applying the above boundary conditions from Eq. (37) to Eq. (39) in Eq. (36), the expression is obtained as

$$\varphi_s(z) = \eta - \left(\frac{\eta + U_T \ln \left(\frac{N_A}{n_i}\right)}{\cosh \left(\frac{z + L_1}{K_d}\right)}\right)$$

(40)

The length of the depletion region at the source is obtained from the potential model when $z = 0$ in Eq. (36):

$$L_1 = K_d \cosh^{-1} \left(\frac{\eta - \phi_{0s}}{\eta - V_{F,s}}\right)$$

(41)

where $V_{F,s} = -U_T \ln \left(\frac{N_A}{n_i}\right).$  Eq. (40) represents the depletion length $L_1$ which depends on the gate-to-source voltage and through $\eta$ and $\phi_{0s}$.

### 3.3 The modeling of the potential in the depletion region of the drain

For lower gate voltages, the drain length cannot be neglected. Thus, modeling of the potential in the drain depletion region is carried out, neglecting the radial direction. The 1D Poisson’s equation in region $R_3$ is expressed as

$$\frac{\partial^2 \phi_{DS}(z)}{\partial z^2} = -\frac{q N_D}{\varepsilon_{Si}} \quad L_2 \leq z \leq L_2 + L_3$$

(42)

where $\phi_{DS}$ is the electrostatic potential with respect to the Fermi level in the drain region and $N_D$ is the doping concentration in the drain region. The fringing field is ignored in this modeling. The boundary conditions are:

$$\phi_D(L_2) = \phi_{0D}$$

(43)

$$\phi_D(L_2 + L_3) = V_{DS} + U_T \ln \left(\frac{N_D}{n_i}\right)$$

(44)

On integrating Eq. (41) twice and applying the boundary condition, the following expression is obtained:

$$\phi_D(z) = -\frac{q N_D}{2 \varepsilon_{Si}} (z - L_1 - L_3)^2$$

$$+ \left(\frac{V_{F,D} - \phi_{0D}}{L_3} - \frac{q N_D L_3}{2 \varepsilon_{Si}}\right) (z - L_2 - L_3) + V_{F,D}$$

(45)

where $V_{F,D} = V_{DS} + U_T \ln \left(\frac{N_D}{n_i}\right).$ The electric field in the lateral direction approaches zero at the right edge of the drain depletion region.

$$\left.\frac{d\phi_D(z)}{dz}\right|_{z=L_2+L_3} = 0$$

(46)

The depletion length at the drain region is obtained from the potential model

$$L_3 = \pm \sqrt{\frac{2 \varepsilon_{Si}}{q N_D} (V_{F,D} - \phi_{0D})}$$

(47)

### 3.4 The modeling of the drain current

The drain current modeling is carried out using Kane’s model. The minimum tunneling path length is considered when calculating the tunneling current. The tunneling path is defined as the path between the conduction-band energy point and the valance-band energy point at the tunneling
junction where the interband tunneling mechanism takes place. This length shows a discrepancy from the shortest tunneling path ($l_{\text{short}}$) to the longest tunneling path ($l_{\text{long}}$).

In Kane’s model, the BTBT generation rate ($G_{\text{BTBT}}$) of carriers per unit volume and per unit time is given as \[30-32\]

$$G_{\text{BTBT}} = \frac{A_{\text{Kane}}}{E_g} |E_{r,z}|^a \exp \left( -B_{\text{Kane}} \frac{E_z^2}{E_{r,z}} \right)$$ \hspace{1cm} (48)

where $|E_{r,z}|$ is the magnitude of the electric field, expressed as $|E_{r,z}| = \sqrt{E_{r}^2 + E_{z}^2}$; $a$ is 2 for direct- and 2.5 for indirect-bandgap tunneling, $A_{\text{Kane}}$ and $B_{\text{Kane}}$ are Kane’s constants with values of $A_{\text{Kane}} = 3.5 \times 10^{21} \text{eV}^{0.5} / \text{cm s V}^2$ and $B_{\text{Kane}} = 2.25 \times 10^7 \text{V/cm eV}^{1.5}$ [28, 29].

The drain current is derived by integrating $G_{\text{BTBT}}$ over the tunneling volume [30-32]:

$$I_{\text{BTBT}} = \int_{V} \frac{qA_{\text{Kane}}}{E_g} E_{r,z}^{a-1} \exp \left( -B_{\text{Kane}} \frac{E_z^2}{E_{r,z}} \right) \mathrm{d}V$$ \hspace{1cm} (49)

$$\times \exp \left( -B_{\text{Kane}} \frac{E_z^2}{E_{r,z}} \right) \mathrm{d}V$$

Since Eq. (47) represents an exponential function of the electric field, the radial term in $G_{\text{BTBT}}$ can be neglected. The lateral electrical field in the channel is obtained from the derivative of Eq. (20), expressed as:

$$E_z(\lambda, r) = \frac{1}{r_0} C_0 \exp \left( \frac{\lambda z}{r_0} \right) - C_1 \exp \left( -\frac{\lambda z}{r_0} \right) \bigg|_0^{l_{\text{avg}}}$$

$$\times J_0(\lambda r)$$

$E_{\text{avg}}$ is the average electric field in the $z$-direction over the tunneling path and can be expressed as [30]

$$E_{\text{avg}} = \frac{E_g}{qL_T}$$ \hspace{1cm} (51)

where $L_T$ is the tunneling path length.

Substituting the average and lateral electric fields into Eq. (49) yields

$$I_{\text{BTBT}} = \frac{2\pi \lambda qA_{\text{Kane}}}{r_0 \sqrt{E_g}} \int_0^{l_{\text{avg}}} \left[ C_0 \exp \left( \frac{\lambda z}{r_0} \right) - C_1 \exp \left( -\frac{\lambda z}{r_0} \right) \right] J_0(\lambda r) \mathrm{d}r$$

$$\times \exp \left( -qB_{\text{Kane}} E_{g}^{2} z \right) \frac{E_g}{qz} \frac{1}{\sqrt{E_z}}$$ \hspace{1cm} (52)

$I_{\text{BTBT}}$ is calculated by integrating Eq. (52) over the exponential terms due to the much faster change of the exponential compared with the polynomial term ($1/z$):

$$I_{\text{BTBT}} = 2\pi \lambda qA_{\text{Kane}} \left( \frac{E_g}{r_0 \sqrt{E_g}} \right) \frac{1}{\sqrt{E_z}}$$

$$\times \left[ H(l_{\text{short}}) - H(l_{\text{long}}) \right] \times \left( \frac{r_0}{\lambda} \right) \mathrm{d}r$$

where $H(z)$ is defined as

$$H(z) = \frac{1}{z^{\alpha-1}} \left( A_0 \exp \left( \frac{C_0 - z}{A_0} \right) + B_0 \exp \left( -\frac{C_0 - z}{B_0} \right) \right)$$ \hspace{1cm} (54)

where $A_0 = \frac{C_0}{\alpha \sqrt{E_g}}$ and $B_0 = \frac{C_1}{\alpha + qB_{\text{Kane}} E_{g}^{2} z}$.  

### 3.4.1 The modeling of the transconductance

The transconductance is derived from the drain current as

$$g_m = \frac{\partial I_{\text{BTBT}}}{\partial V_{GS}}$$ \hspace{1cm} (55)

### 4 Results and discussion

In this section, the results are plotted for the analytical modeling and validated using the ATLAS TCAD simulation tool. The channel length of the proposed model is 50 nm with a source and drain length of 20 nm. The concentration-dependent, Lombardi, Boltzmann, Shockley–Read–Hall,
Auger, and band-to-band models are used in the simulations of the device.

Figure 4 shows the surface potential profile along the channel length for a gate-to-source voltage of 0 V and 1 V. It is observed that the electron density across the channel increases with an increase in the gate voltage, especially near the drain region. The extension of the drain/source depletion regions is observed at low/high gate voltages. The surface potential profile of the model is close to the simulation results. Figure 5 shows the surface potential profile along the channel length for different silicon thicknesses of 13 nm, 14 nm, and 15 nm. It is observed from this plot that, the thicker the silicon, the higher the value of the surface potential. When the thickness of the silicon is large, the electron density increases, leading to an increase of the conductivity along the channel, which further increases the value of the surface potential.

Figure 6 shows the surface potential profile along the channel for different drain voltages of 0 V and 1 V. The plot shows the variation of the potential across the drain region, while it is constant over the source and channel regions. As the drain voltage is varied, the potential profile changes across the drain region due to an increase in the carrier density.

Figure 7 shows a comparison plot of the lateral electric field profile for GAA-HJTFETs with and without high-\(k\) material. It is observed that the high-\(k\) stacked GAA-HJTFET exhibits a higher electric field profile than the GAA TFET. The peak across the source and channel region is due to the variation of the potential. The peak is low at the drain to channel region of the high-\(k\) GAA-HJTFET compared with the GAA TFET. Figure 8 shows a comparison of the
drain current variation versus the gate voltage, revealing that the high-\(k\) stacked GAA-HJTFET exhibits a higher drain current than the GAA-HJTFET due to the higher tunneling rate.

Figure 9 shows the variation of the drain current versus the gate voltage for different work functions of 4.2 and 4.3 eV. It is observed that the OFF-state current is low while the ON-state current is high, thus the \(I_{\text{ON}}/I_{\text{OFF}}\) ratio is high at \(10^{15}\). Figures 10 and 11 show the drain current variation with the drain voltage for different gate voltages of 0.5 V and 1 V. This plot shows that, the higher the gate-to-source voltage, the higher the drain current.

Figure 12 shows the variation of the transconductance with the gate voltage. The transconductance is high for the high-\(k\) stacked GAA-HJTFET, which in turn increases the sensitivity of the device operation.

5 Conclusions

Analytical modeling of a high-\(k\) stacked GAA-HJTFET is presented. First the electrostatic potential modeling of the high-\(k\) GAA-HJTFET is considered. To enhance the
Appendix A

Using the continuity of the lateral electric field across the source–channel interface, the potential \( \phi_{0S} \) can be expressed as

\[
\frac{\partial \phi_c(z)}{\partial z} \bigg|_{z=0} = \frac{\partial \phi_c(z, r = r_0)}{\partial x} \bigg|_{z=0} \tag{56}
\]

From Eq. (56), we obtain

\[
-\frac{1}{k_d} \left( \phi_0 + V_T \ln \left( \frac{N_A}{n_i} \right) \right) \sinh \left( \frac{L_1}{k_d} \right) = \frac{\lambda}{r_0} \left( C_0 - C_1 \right) J_0(\lambda r_0) \tag{57}
\]

Using the continuity of the lateral electric field across the drain–channel interface, the potential \( \phi_{0D} \) is expressed as

\[
\frac{\partial \phi_c(z, r = r_0)}{\partial z} \bigg|_{z=L_2} = \frac{\partial \phi_d(z)}{\partial z} \bigg|_{z=L_2} \tag{58}
\]

From Eq. (58), we obtain

\[
V_{F,D} - \phi_{0D} = \frac{q N_D L_3}{2 \varepsilon_{Si}} \left( \frac{1}{r_0} \right) \sinh \left( \frac{L_2}{k_d} \right) = \frac{\lambda}{r_0} \left( C_0 \exp \left( \frac{L_2}{r_0} \right) - C_1 \exp \left( -\frac{L_2}{r_0} \right) \right) J_0(\lambda r_0) \tag{59}
\]

Further simplification using Eqs. (57) and (59) yields the expressions for \( \phi_{0S} \) and \( \phi_{0D} \).

Appendix B

Substituting the potential model in Eq. (20) into the boundary condition in Eq. (17), we get

\[
\sum_{m=1}^{\infty} \left( C_0 + C_1 \right) J_0 \left( \frac{\lambda m}{r_0} \right) = \phi_{0S} - \phi_{1D} \tag{60}
\]

The above equation is solved by using Fourier–Bessel series

\[
C_0 + C_1 = \frac{1}{N} \left( \phi_{0S} \frac{J_1(\lambda)}{\lambda} - V_a \right) \tag{61}
\]

where

\[
V_a = \frac{1}{r_0} \int_0^{r_0} r \phi_{1D}(r) J_0 \left( \frac{\lambda}{r_0} \right) dr \tag{62}
\]

Similarly, using the boundary condition in Eq. (18), we get

\[
\sum_{m=1}^{\infty} \left[ C_0 \exp \left( \frac{\lambda m L_2}{r_0} \right) + C_1 \exp \left( -\frac{\lambda m L_2}{r_0} \right) \right] \times J_0 \left( \frac{\lambda m}{r_0} \right) = \phi_{0D} - \phi_{1D} \tag{63}
\]

and

\[
C_0 \exp \left( \frac{\lambda L_3}{r_0} \right) + C_1 \left( -\frac{\lambda L_3}{r_0} \right) = \frac{1}{N} \left( \phi_{0D} \frac{J_1(\lambda)}{\lambda} - V_a \right) \tag{64}
\]

\( C_0 \) and \( C_1 \) can also be obtained from Eqs. (61) and (64).

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