Isolated Single-ended Primary-inductive Converter with a Soft-switching Cell for Implementing Features of Zero-voltage Switching and Zero-current Switching

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(Received January 20, 2020; accepted June 3, 2020)

Keywords: isolated single-ended primary-inductive converter (ISEPIC), zero-voltage switching (ZVS), zero-current switching (ZCS)

In this paper, an isolated single-ended primary-inductive converter (ISEPIC) with a soft-switching cell for implementing features of zero-voltage switching (ZVS) and zero-current switching (ZCS) is proposed. The ISEPIC has the following advantages: (1) By changing the inductor element of the ISEPIC into a transformer element, the features of electrical isolation can be achieved. (2) By incorporating a soft-switching cell, the power switches (MOSFETs) of the ISEPIC can achieve ZVS and ZCS features during turn-on conditions. Therefore, the power losses of the power switches can be reduced during the turn-on transient, and the overall efficiency of the ISEPIC can be increased significantly. Finally, a prototype of the ISEPIC with a soft-switching cell is built. Experimental results are presented to verify the performance and feasibility of the proposed ISEPIC for implementing features of ZVS and ZCS.

1. Introduction

A number of nonisolated switching power converters have been developed and proposed. For example, Buck, Boost, Cuk, single-ended primary-inductive converter (SEPIC), and Zeta converters have attracted interest, which have simple structures and are widely used at low and medium powers. A nonisolated SEPIC is often adopted for step-down and step-up voltage applications, as shown in Fig. 1. However, the hard-switching conditions of the active switch (MOSFET) are a major contributor to switching losses in a nonisolated SEPIC, resulting in high power losses, high electromagnetic interference (EMI), and low conversion efficiency. To overcome these problems, a number of soft-switching techniques have been proposed. Soft-switching techniques improve the imperfect switching of power switches and thereby eliminate switching losses and EMI. Several soft-switching techniques have been developed in recent years. The soft-switching techniques can be divided into zero-voltage-switching (ZVS) and zero-current-switching (ZCS) techniques. Both techniques drive the voltage or current of the active switch to zero before any switching action, and avoid a concurrent high voltage and
high current in the switching transition. A SEPIC with ZVS and ZCS techniques will have no voltage and no current across the power switch at turn-on and turn-off transitions, as illustrated in Figs. 2 and 3, respectively.

In this paper, an isolated single-ended primary-inductive converter (ISEPIC) with a soft-switching cell for implementing features of ZVS and ZCS is presented, as shown in Fig. 4. The soft-switching cell has a simple structure, which consists of a transformer ($T_1$) and an auxiliary switch ($M_2$) to implement the ZVS feature of the main switch ($M_1$) and the ZCS feature of $M_2$. The operational principles of the proposed ISEPIC are described in Sect. 2. Experimental results obtained from a prototype of the proposed ISEPIC with a soft-switching cell for implementing features of ZVS and ZCS are presented in Sect. 3. Finally, a conclusion is given in Sect. 4.

2. Operational Principles

As shown in Fig. 4, the proposed ISEPIC with features of ZVS and ZCS consists of a SEPIC and a soft-switching cell. The soft-switching cell is composed of an isolated transformer ($T_1$),
$M_1$ and a power diode ($D_c$) to create a ZVS condition for $M_1$ and a ZCS condition for the auxiliary switch $M_2$. The operational principles of the proposed ISEPIC with a soft-switching cell for implementing features of ZVS and ZCS over one switching cycle can be divided into eight major operating modes. Figure 5 shows the current and voltage waveforms of the key components and the driving signals of the switches ($M_1$ and $M_2$). Figure 6 shows the equivalent circuits of the proposed ISEPIC. To simplify the description of the operational modes, the following assumptions are made:

1. To analyze the ZVS feature, the body diode ($D_1$) and parasitic capacitor ($C_1$) of $M_1$ will be considered in the steady-state operation of the circuit.

![Fig. 4. (Color online) Topology of ISEPIC with a soft-switching cell for implementing features of ZVS and ZCS.](image)

![Fig. 5. (Color online) Current and voltage waveforms of the key components and the driving signals of switches ($M_1$ and $M_2$) for proposed ISEPIC with a soft-switching cell for implementing features of ZVS and ZCS.](image)
Fig. 6. (Color online) Equivalent circuits of the proposed ISEPIC with a soft-switching cell for implementing features of ZVS and ZCS. (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4, (e) Mode 5, (f) Mode 6, (g) Mode 7, and (h) Mode 8.
(2) The output filter capacitor \((C_o)\) is large enough for the voltage across it to be constant over a switching cycle.

**Mode 1** [Fig. 6(a), \(t_0 < t < t_1\)]:

At time \(t_0\), \(M_1\) is turned on, and \(M_2\) is turned off. The inductor current \(i_{La}\) flowing through the path \(V_s \rightarrow L_f \rightarrow M_1 \rightarrow V_s\) is linearly increased, where \(V_s\) is an input source and \(L_f\) is a storage inductor. During this interval, the capacitor \((C_a)\) begins discharging. The current \(i_{ca}\) of \(C_a\) is flowing through the path \(C_a \rightarrow M_1 \rightarrow T_{r2} \rightarrow C_a\). At this time, the magnetic inductance current of the transformer \((T_{r2})\) is linearly increased. In the output terminal, the diodes \((D_a, D_b,\) and \(D_c)\) are turned off and the filter capacitor \((C_2)\) delivers power to the output load. The inductor current \(i_{La}\) can be expressed as

\[
i_{La}(t) = \frac{V}{L_a}(t - t_0).
\]  

The equivalent circuit is shown in Fig. 6(a).

**Mode 2** [Fig. 6(b), \(t_1 < t < t_2\)]:

At time \(t_1\), \(M_1\) is turned off, and \(M_2\) remains off. The inductor current \(i_{La}\) flowing through the path \(V_s \rightarrow L_a \rightarrow C_a \rightarrow T_{r2} \rightarrow V_s\) is linearly decreased. On the primary side of \(T_{r2}\), the magnetizing current \(i_{ca}\) is transferred to the secondary side to discharge \(C_b\). At this time, \(D_b\) is turned on by a forward bias, and \(D_a\) and \(D_c\) are turned off. The secondary current \(i_{cb}\) of \(T_{r2}\) flows through the path \(T_{r2} \rightarrow C_b \rightarrow D_b \rightarrow Load \rightarrow T_{r2}\). \(i_{La}\) can be expressed as

\[
i_{La}(t) = \frac{V_{ca} + V_{Tr2} - V_s}{L_a}(t - t_1).
\]  

The equivalent circuit is shown in Fig. 6(b).

**Mode 3** [Fig. 6(c), \(t_2 < t < t_3\)]:

At time \(t_2\), \(M_1\) remains off and \(M_2\) is turned on. Because the limiting current of the magnetizing inductance \((L_{m1})\) of \(T_{r1}\) increases instantaneously, \(M_2\) has a feature of ZCS in the conduction transient state. At this time, the main inductor current \(i_{La}\) is divided and flows through two paths: \(V_s \rightarrow L_a \rightarrow C_a \rightarrow T_{r2} \rightarrow V_s\) and \(V_s \rightarrow L_a \rightarrow T_{r1} \rightarrow M_1 \rightarrow V_s\). At this time, the magnetizing inductance current of \(T_{r1}\) is linearly increased. At the output end, because the voltage of \(C_b\) is discharged to zero, \(D_a\) is turned on by a forward bias, and the secondary current \(i_{cb}\) of \(T_{r2}\) flows through the path \(T_{r2} \rightarrow D_a \rightarrow Load \rightarrow T_{r2}\). \(i_{La}\) can be expressed as

\[
i_{La}(t) = i_{Tr1} + i_{ca} = \frac{V_{Tr1}}{L_{m1}}(t - t_2) + \frac{(V_{ca} - V_{La} - V_s)}{L_{m2}}(t - t_2).
\]  

The equivalent circuit is shown in Fig. 6(c).

**Mode 4** [Fig. 6(d), \(t_3 < t < t_4\)]:

At time \(t_3\), \(M_2\) continues to be turned on, and \(M_1\) remains turned off. When the main inductor current \(i_{La}\) is equal to the magnetizing inductor current \(i_{Tr1}\) of \(T_{r1}\), the current flowing
through $C_a$ drops to zero. At this time, $D_a$, $D_b$, and $D_c$ at the output end are turned off by a reverse bias, and the current required by the load is provided by $C_o$. $i_{La}$ can be expressed as

$$i_{La}(t) = \frac{(V_{La} + V_s)}{L_m1}(t - t_3). \quad (4)$$

The equivalent circuit is shown in Fig. 6(d).

**Mode 5** [Fig. 6(e), $t_4 < t < t_5$]:

At time $t_4$, $M_2$ remains on and $M_1$ remains off. The main inductor current $i_{La}$ continues to decrease linearly, while the magnetizing inductance current $i_{Tr1}$ of $T_{r1}$ continues to increase linearly. When the main inductor current $i_{La}$ is smaller than the magnetizing inductance current $i_{Tr1}$ of $T_{r1}$, the magnetizing inductance current $i_{Tr1}$ of $T_{r1}$ is divided and flows through two paths: $V_s \rightarrow L_a \rightarrow T_{r1} \rightarrow M_2 \rightarrow V_s$ and $T_{r1} \rightarrow M_2 \rightarrow C_1 \rightarrow T_{r1}$. $C_1$ of $M_1$ starts to be discharged. At this time, $D_a$, $D_b$, and $D_c$ at the output end continue to be reversely biased and cut off, and the current required by the load continues to be provided by $C_o$. $i_{La}$ can be expressed as

$$i_{La}(t) = i_{Tr1}(t - t_4) - i_{M1}(t - t_4). \quad (5)$$

The equivalent circuit is shown in Fig. 6(e).

**Mode 6** [Fig. 6(f), $t_5 < t < t_6$]:

At time $t_5$, $M_2$ continues to be turned on. When the voltage of $C_1$ of $M_1$ is discharged to zero, $D_1$ of $M_1$ is turned on, providing a zero-voltage conduction characteristic of $M_1$. The magnetizing inductance current $i_{Tr1}$ of $T_{r1}$ continues to be divided and flow through two paths: $V_s \rightarrow L_a \rightarrow T_{r1} \rightarrow M_2 \rightarrow V_s$ and $T_{r1} \rightarrow M_2 \rightarrow D_1 \rightarrow T_{r1}$. At this time, $D_a$, $D_b$, and $D_c$ at the output end continue to be reversely biased and cut off, and the current required by the load continues to be provided by $C_o$. $i_{La}$ can be expressed as

$$i_{La}(t) = i_{Tr1}(t - t_5) - i_{M1}(t - t_5). \quad (6)$$

The equivalent circuit is shown in Fig. 6(f).

**Mode 7** [Fig. 6(g), $t_6 < t < t_7$]:

At time $t_6$, $M_1$ is turned on by ZVS, and $M_2$ continues to be turned on. The current $i_{La}$ of $L_a$ starts to increase linearly, while the current flowing through $M_1$ and $T_{r1}$ starts to decrease linearly. At this time, $D_a$, $D_b$, and $D_c$ at the output end continue to be reversely biased and cut off, and the current required by the load continues to be provided by $C_o$. $i_{La}$ can be expressed as

$$i_{La}(t) = i_{Tr1}(t - t_6) - i_{M1}(t - t_6). \quad (7)$$

The equivalent circuit is shown in Fig. 6(g).
Mode 8 [Fig. 6(h), \(t_7 < t < t_8\):]

At time \(t_7\), \(M_1\) continues to be turned on, and \(M_2\) is turned off. The current \(i_{La}\) of \(L_a\) flows through the path \(V_s \rightarrow L_a \rightarrow M_1 \rightarrow V_s\), and the main inductor current \(i_{La}\) is linearly increased. At the same time, \(C_a\) starts to discharge, \(C_a\) current \(i_{ca}\) flows through the path \(C_a \rightarrow M_1 \rightarrow T_{r2} \rightarrow C_a\), and the magnetizing inductance current of \(T_{r2}\) is linearly increased. On the primary side of \(T_{r1}\), the magnetizing current \(i_{Tr1(pri)}\) is transferred to the secondary side, and then \(D_b\) and \(D_c\) are turned on by a forward bias. The secondary current \(i_{Tr1(sec)}\) of \(T_{r2}\) flows through the path \(T_{r1} \rightarrow D_c \rightarrow D_b \rightarrow \text{Load} \rightarrow T_{r1}\). \(i_{La}\) can be expressed as

\[
i_{La}(t) = i_{Tr1}(t - t_7) - i_{M1}(t - t_7).
\]  

The operational mode of the proposed ISEPIC with a soft-switching cell for implementing features of ZVS and ZCS over one switching cycle is completed. The equivalent circuit is shown in Fig. 6(h).

3. Experimental Results

To verify the feasibility of the ISEPIC with a soft-switching cell for implementing features of ZVS and ZCS, a 120 W prototype is built. The specifications of the ISEPIC are listed as follows:

- input voltage: \(V_s = 50\ V_{dc}\),
- output voltage: \(V_{01} = 120\ V_{dc}\),
- output current: \(I_{01} = 1\ A\),
- total output power: 120 W,
- switching frequency: \(f = 40\ \text{kHz}\).

Figure 7 shows the experimental signal waveforms of \(M_1\) and \(M_2\) at an operating frequency of 40 kHz. Figure 8 shows the experimental voltage and current waveforms of \(M_1\), from
which it can be seen that $M_1$ has a ZVS feature at the turn-on transition. Figure 9 shows the experimental voltage and current waveforms of $M_2$, from which it can be seen that $M_2$ has a ZCS feature at the turn-on transition. Figure 10 shows the efficiency measurements of the ISEPIC with a soft-switching cell for implementing features of ZVS and ZCS, from which it can be seen that the maximum efficiency can reach as high as 92%, about 4% higher than that of the nonisolated SEPIC (as shown in Fig. 1). The reason for the higher efficiency is that $M_1$ of the nonisolated SEPIC is still operated in a hard-switching manner during the turn-on and turn-off transitions.

4. Conclusions

In this study, the proposed ISEPIC with a soft-switching cell for implementing features of ZVS and ZCS has been built and implemented. It uses a soft-switching cell to implement the features of ZVS and ZCS under turn-on transitions for $M_1$ and $M_2$. Therefore, the power losses of the power switches can be reduced during the turn-on transient, and the overall efficiency of the ISEPIC can be increased significantly. The experimental results have verified that the proposed ISEPIC with a soft-switching cell is relatively suitable for the high-frequency requirements of power supplies.

Acknowledgments

This work was supported by National Chin-Yi University of Technology, Taiwan.

Author Contributions

All of the authors contributed to publishing this paper. Cheng-Tao Tsai wrote the paper, and Jyun-Mao Chen contributed to the experimental results of the circuit.
Conflicts of Interest

The authors declare that there are no conflicts of interest, regarding the publication of this paper.

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