Energy/Fuel Efficient and Enhanced Robust Systems Demonstrated with Developed Fractional Order PID Controller

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Abstract

In this brief article, the design and implementation of Fractional Order Proportional-Integral-Derivative (FOPID) controller is presented in analog and digital domains. Here we show the measured results for energy/fuel efficiency and enhanced robustness, as compared to classical PID controls. The FOPID controller is tested with DC-Motor, Magnetic Levitation System, and Brushless DC Motor, that we report in this article.

Keywords: Fractional calculus; PID; Fractional order PID; Fractional order Laplace variable; Pole-zero approximation; Iso-damping; Performance indices; Energy/fuel efficient control system

Introduction

Classical controls are in form of PID (Proportional Integral Derivative) controllers exist since 1910. The PID was invented in 1910 by Elmer Sperrys for ship auto pilot. However the ‘electronic’ circuit based conventional classical controllers such as PD, PI and PID have been applied in industry for over half-a-century to control linear and nonlinear systems. The tuning methods for PID controllers i.e. “Ziglers-Nichols” is well proven and exists since 1942.

Recently, such control schemes have been extended to their generalized form using fractional calculus (differentiation and integration of an arbitrary order). The FOPID controller has fractional order differ-integration operations [1-4]. In applications, where these non-integer order controllers (i.e. FOPID) are used there is added flexibility in adjusting the gain and phase characteristics as compared to integer order controllers as shown in Figure 1 [1,2]. The Figure 1a gives the transfer function (in frequency domain) of FOPID controller as \( C_{	ext{FOPID}}(s) = K_p + K_i s^{-\alpha} + K_d s^\beta \), with parameters \( \alpha \) and \( \beta \) and the non-integer values (greater than zero). These parameters \( \alpha, \beta \in \mathbb{R} \), give two extra degrees of freedom in tuning as compared to three in number for the classical PID where the transfer function is \( C_{	ext{PID}}(s) = K_p + K_i s + K_d s^2 \) [1,2]. Note that classical PD, PI, and PID take only three points namely (0,1), (1,0) and (1,1) in the entire \( \alpha - \beta \) plane, whereas the FOPID is having domain of operation in the entire first quadrant of \( \alpha - \beta \) plane (Figure 1a). This flexibility makes fractional order control more versatile tool in designing robust and precise control systems. The fractional Laplace operators in the transfer function (i.e. \( s^\alpha \) and \( s^\beta \)) of FOPID corresponds to fractional integration of order \( \alpha \) and fractional differentiation of order \( \beta \), respectively [1,2]. Thus, in the time domain the controller output i.e. \( u(t) \) which is obtained via operation on real time error signal i.e. \( e(t) \) is \( u(t) = K_p e(t) + K_i \left[D^{\alpha} e(t)\right] + K_d \left[D^{\beta} e(t)\right] \). This has operation of fractional integration and fractional differentiation (Figure 1b). The operation \( D^{\alpha} x(t) \) is fractional derivative/integration with respect to variable \( t \) for a function \( x(t) \) for fractional order \( \alpha \); \( \alpha \in \mathbb{R} \) [1-4]. When \( u=1 \), the operation is one-whole classical derivative, and with \( u=-1 \) the operation is classical one-whole order integration. This structure of FOPID controller is depicted in the Figure 1b. A better understanding of the potential of fractional calculus and the increasing number of studies related to the fractional order controllers led to the importance of studying aspects such as the analysis, design, implementation, tuning, and application of these controllers in diverse applications. Some of the results we briefly report in this article. For detailed study the readers may study the articles listed in references.

Algorithm for Practical Realization of the Fractional Order Differentiators and Integrators for Analog and Digital Circuits

Fractional order differentiators and integrators are not available commercially. The fractional order Laplace element i.e. \( s^{\alpha} \) when implemented into analog or digital circuits is called ‘fractance’ [5]. Implementation of these ‘fractance’ is by using a band-limited (\( \omega_s \leq \omega \leq \omega_w \)) integer order transfer function approximation. Thus, the fractional Laplace operator i.e. \( s^\alpha \); \( \alpha \in \mathbb{R} \) gets approximated by ratio of rational polynomials as \( s^{\alpha} \approx \left(\frac{s + z_1}{s + p_1}\right)\left(\frac{s + z_2}{s + p_2}\right)\cdots\left(\frac{s + z_n}{s + p_n}\right) \) in the band \( \omega_s \leq \omega \leq \omega_w \).
≤ ωh [1,2]. This rational approximation is then implemented by using analog circuit technique [6,7] and then using digital techniques [7-13].

A novel pole-zero interlaced approximation method (a new proprietary algorithm) is developed to approximate the fractional order Laplace operators [5,6]. The basic idea is of getting a constant phase by slope cancellation of asymptotic phase plots for zeros and poles [1,2,5,6]. For fractional order integrator, first pole p1 is selected such that its asymptotic phase plot passes through point (ω, φreq), then z1 i.e. the first zero gets selected; and thereafter subsequent poles and zeros are selected so as to keep the asymptotic plot constant at φreq = α(90°). For semi-integration operation α = -0.5 so we get φreq = -45°. Thus our objective is to have phase angle equal to φreq with an error less than or equal to ε allowed, i.e. ε ≤ ε allowed (Figure 2) for all frequencies ω such that ω1 ≤ ω ≤ ωh. For a n number pole zero-pair we have the essential formulas noted in the Figure 2, (tagged as Eqn). We note here the values of band limits i.e. ω1, ωh is based on system-identification, that is carried out a priori with the known dynamic model of the system [7,11-13].

In the described recurring relation tagged as Eqn in Figure 2 we have a trim-parameter µ which is normally zero but is selected as to adjust density of pi, zi in the phase plot to have ϕreq with an error less than or equal to ε allowed, i.e. ε ≤ ε allowed. The approximation will be reciprocal of what we obtained for semi-integration i.e. sα as above.

The rational approximation of semi-integration operation is thus following (from Table 1)

\[ S^{α} = \left( s + 7.0795 \right) \left( s + 51.286 \right) \left( s + 371.54 \right) \left( s + 2691.5 \right) \left( s + 19,498 \right) \left( s + 141,250 \right) \left( s + 993.34 \right) \left( s + 52,131 \right) \]

Table 1: The pole and zero of the rational approximation of semi-integration on band limited range of 100-10,000 radian/sec.

| i | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| p | -7.0795 | -51.286 | -371.54 | -2691.5 | -19,498 | -141,250 |
| z | -2.6128 | -19.933 | -1,037.12 | -7191.6 | -52,131 |

For a fractional order differentiator in the band limit of ω1 ≤ ω ≤ ωh we obtain digitized representation of semi-integration (Table 1) as following transfer function.

\[ S^{α} = \left( s + 0.7072 \right) \left( s + 0.752 \right) \left( s + 0.763 \right) \left( s + 0.964 \right) \left( s + 0.999 \right) \left( s + 0.013 \right) \left( s + 0.446 \right) \left( s + 0.471 \right) \left( s + 0.905 \right) \left( s + 0.986 \right) \left( s + 0.989 \right) \]

The discrete transfer function is implemented by using standard digital-filter algorithm [7,11-13]. With the obtained approximated fractional Laplace operator for sα, sβ the FOPID transfer function i.e. C_{FOPID}(s) = Kp + Ki*s^α + Kd*s^β is discretized to z domain (Figure 1). Thereafter choosing the standard digital-filter formula a difference equation for discretized C_{FOPID}(s) is obtained. This difference equation relates discretized e(t) stated as e_k to get discretized controller output u(t) stated as u_k which is given as u_k = \sum_{i=1}^{n} a_i e_{k-i} + \sum_{j=1}^{m} b_j e_{k-j} [7,11-13].

Analog FOPID Controller

The fractional order impedance or 'fractance' circuit is realized with two port network having passive components resistor (R) and capacitor (C) [5,6], along with operational amplifiers (Figure 3a). This analog circuit of Figure 3a is designed to generate the pole-zero pairs by use of available R - C components designed for a given fractional order (α; α < 1). The asymptotic phase plot of fractional order integrator is shown in Figure 3c for α = -0.5; for frequency band of 100° ≤ ω ≤ 10°. The Figure 3b shows a photograph of developed 'fractance' circuit with six poles-zero pair i.e. having six circuits i=1-6 of Figure 3a connected in series with different values of R1, R2, C1; R3'. Refer Table 2 for the values of the six circuits [6].

A semi-integrator for the required specifications of band-limited
approximation is realized by six poles-zero pairs as per algorithm of Figure 2, presented in Table 1. The resistors and capacitor values of the circuit of Figure 2a given in Table 2 is by formula [6].

\[
R = \frac{1}{pC}
\]

for fractional Integrator \( R \) = \( \frac{1}{z-p}C \),

\[
R = \frac{1}{z-C}
\]

for fractional differentiator \( R \) = \( \frac{1}{p-z}C \).

In the formula we select first the available value of capacitor and then the resistor value is calculated. The exact resistor value is adjusted by using standard E48 series resistors with a potentiometer in series. The algorithm, as shown in Figure 2, is developed to determine the actual values of resistor and capacitor components. Then these 'fractance' circuits are organized (with operational amplifiers) as shown in Figure 1b, to get analog FOPID controller. The analog FOPID controller is shown in Figure 4a, it has got facility to select fractional order of differentiation \( \beta \), and fractional order integrator \( \alpha \) as 0.2, 0.5 and 0.8; and also via potentiometer one can select the gain values of the 'gains' \( K_p, K_i, K_d \).

To verify the analog FOPID controller performance, a hardware emulator circuit of DC motor (i.e. plant) is developed. Plant consists of a DC motor and a load with specification as: Speed \( N=2000 \text{ rpm} \), armature resistance as \( R_a = 2 \Omega \), armature inductance as \( L_a =3mH \), rotor inertia \( J = 1.78 \times 10^{-4} \text{ Kg-m}^2 \), motor constant \( K_v = 1.02 \), DC armature voltage \( V_a = 24V \) [6]. The plant transfer function \( G(s) \) of DC motor a second order stable function realized by circuit is

\[
G(s) = \frac{K}{s(s + \frac{R}{L})}
\]

The complete hardware setup is shown in Figure 4a. Performance test result of DC motor model emulator circuit is shown in Figure 4b. The performance of the realized analog FOPID controller is tested with the DC motor emulator. The FOPID performance indicates that the controller with \( \alpha, \beta = 0.5 \) could make it possible to maintain the desired control on the output speed. The response of DC motor model with FOPID controller is shown in Figure 4c.

Enhanced Robustness- 'iso-damping' Observed

The variation in gain from 40 to 100 is set with PID and FOPID controllers. The recorded response is given in the CRO traces of Figures 5 and 6. From CRO traces of Figures 5a, 5b it is observed that the peak overshoot with a PID controller is varying widely, when the gain is changed from 40 to 100. Whereas, from CRO traces of Figures 6a, 6b the peak overshoot is almost constant in FOPID controlled system, while the gain is changed from 40 to 100. This phenomena of overshoot remaining constant over wide parametric spread is called 'iso-damping', is a feature what we get via using FOPID; thus we have enhanced robustness in controls [1,2,6]. The comparison of overshoot variation is also tabulated in Table 3 [6].

The Table 3 show that with variation in gain from 40-100 the closed loop response is having overshoot constant at about 25%. This is 'iso-damping', that is got by FOPID while the overshoot varies from 22-65% in case of PID. This is enhancement in robustness experimentally demonstrated by use of FOPID.

### Table 2: R-C values of six circuits for realizing the half order integrator.

| Circuit | 1     | 2     | 3     | 4     | 5     | 6     |
|--------|-------|-------|-------|-------|-------|-------|
| Circuit | 1µF   | 1µF   | 0.47µF| 0.068µF| 10nF  | 2.2nF |
| Circuit | 382.7kΩ| 52.9kΩ| 15.52kΩ| 14.8kΩ| 13.8kΩ| 8.71kΩ|
| Circuit | 223.9kΩ| 30.9kΩ| 9.08kΩ | 8.66kΩ| 8.13kΩ| 5.13kΩ|

### Table 3: Comparison of peak overshoots with variation of gain for PID and FOPID.

| Values of \( K_p \) (gain) | Close-loop PID | Close-loop FO-PID |
|-----------------------------|----------------|-------------------|
| % Peak overshoot simulation results | % Peak overshoot hardware results | % Peak overshoot simulation results | % Peak overshoot hardware results |
| 40 | 22 | 30 | 25 | 24 |
| 50 | 30 | 36 | 25 | 24 |
| 60 | 45 | 44 | 25 | 24 |
| 70 | 53 | 52 | 25.5 | 25 |
| 100 | 65 | 60 | 25.5 | 25 |

Digital FOPID Controller

Magnetic levitation system controlled by PID and FOPID controller

This designed digital FOPID controller is used to control highly non-linear and inherently unstable Magnetic Levitation System (Mag-Lev) in hardware-in-loop mode as shown in Figure 7a. Mag-Lev is basically an electromagnetic system which levitates ferromagnetic objects in space by the magnetic force induced due to the electric current flowing through the coils around a solenoid [7]. The tuned controllers that are compared are having transfer functions, for PD as \( C_{pd}(s) = 4 + 2s \), PID as \( C_{pid}(s) = 5.5 + 0.2s^2 + 2s \) and FOPID as \( C_{fopid}(s) = \).
7+12s^{0.4}. The continuous time pole-zero interlaced approximation method (Figure 2) to get rational approximation for \( s^{\alpha} \) is discretized, using Tustin digital formula (with \( T_s=0.01 \) Sec) converting s-domain to z-domain, with sampling time \( T_s=0.01 \) sec; in the band \( 10^2 \leq \omega \leq 10^6 \) and then a digital FOPID controller is developed [7].

The performance analysis for digital classical PID, PD, and FOPID is carried out. The results in CRO traces of Figures 7b, 7c, 7d that show a better control over position accuracy with lesser control efforts \( u(t) \) is achieved with FOPID over the conventional methods i.e. PID, PD [7]. In practical terms, this improvement of controlling with lesser effort translates to better energy/fuel efficiency [1,2,7-9].

The control signals \( u(t) \) along with measures as Performance Indices (P.I) those are Integral Absolute (IA), Integral Time Absolute (ITA), and Integral Square (IS) [10] are the indicator of energy utilized by the controller, an important factor in the industrial control paradigm. In this context, the fractional order controller proves to be superior to the classical controller. The comparison is presented between PD, PID, and FOPID controls in Figure 8, as for ball position error (Figure 8a) and controller performances (Figure 8b) via comparing performance indices IA, ITA, and IS, calculated on

(i) Error signal \( e(t) \) and
(ii) Control signal \( u(t) \) i.e. output of the controller.

**DC motor speed control by PID and FOPID controller**

The digital FOPID controller is tested for 1.5kW industrial DC motor drive [11,12]. Speed control scheme of buck converter fed DC motor drive is shown in Figure 9a. Here, a reference speed is given as set point for FOPID controller, which provides the control signal computing the error generated in the control scheme. The PWM pulses are generated at frequency of 25 KHz with corresponding duty-ratio proportional to the controller output [11,12]. This signal operates the switch of buck converter and regulates the armature voltage of the DC motor. The controller is implemented on Digital Signal Processor (DSP) TMS320F28027 and TMS320F28377s. An industrial DC motor drive is developed as shown in the Figure 9b.

Here, it is recorded that tuned PID used for this DC motor is \( C_{PID}(s) =115.6 +0.22 s^{-1}+1.6s \) and tuned FOPID used is \( C_{FOPID}(s) =15.2 +0.04 s^{-1.4} + 2.4s^{1.2} \). This tuning resulted in minimizing the Performance Indices (P.I) as shown in the Table 4, with respect to error signal \( e(t) \). The Table 5 gives the values of performance indices of controller effort with respect to control signal of the controller i.e. \( u(t) \). The measurement is done for armature current and armature voltage for various speed settings for DC motor, in no-load condition and with loaded condition (coupled to a generator and then loading the generator via resistive load banks). The Figure 10 displays the experimental result.

It is observed that averagely 21.3% less power is drawn from DC source at no-load condition and averagely 19.6% less power is drawn at loaded condition for speed settings from 500RPM to 1300RPM. This is direct evidence of having Energy/Fuel Efficiency by using FOPID.

**BLDC motor speed control by PID and FOPID controller**

The speed control scheme for FOPID controller fed brushless DC motor (BLDC) 0.5kW, 350 RPM [13] drive is shown in Figure 11a. Here, the scheme is having FPGA-in-the-loop. The digital FOPID controller is implemented on Altera FPGA DE2-115 board [13]. Figures 11b-11d gives the comparison between the tuned PID controller and tuned FOPID controller. The Figure 12 show the comparison of control
signal and phase current of BLDC motor controlled by PID & FOPID. We observe significant reduction in the RMS phase current drawn while controlling via FOPID controller as compared with classical PID controller.

The tuned FOPID transfer function is \( C_{\text{FOPID}}(s) = 4.25 + \frac{0.2s^{0.6}}{s^{1.21}} \) [13]. The fractional Laplace variables \( s^{1.21} \) and \( s^{0.6} \) we approximate as per algorithm described in the form \( s^{a} \approx \prod_{i=1}^{n} \left( s + \alpha_{i} \right) \prod_{i=1}^{n} \left( s + \beta_{i} \right) \) in the frequency band \( 10^{-1} \leq \omega \leq 10^{1} \) with phase angle error \( e_{\text{allowed}} = 1^\circ \) (Figure-2) Then the obtained expression for \( C_{\text{FOPID}}(s) \) we discretize by Tustin method [13] with \( T_{s}=0.001 \text{sec} \) to get FOPID in \( z \)-domain as following

\[
C_{\text{FOPID}}(z) = \frac{116.4z^{-1} - 773.7z^{-2} + 1797z^{-3} - 802.6z^{-4} + 3730z^{-5} + 6455z^{-6} - 1002z^{-7} - 6953z^{-8} + 6347z^{-9} + 914z^{-10} - 4282z^{-11} - 1860z^{-12} + 606.9z^{-13}}{336.2z^{-1} + 162.1z^{-2} + 29.75z^{-3} - 15.32z^{-4} + 1.24z^{-5}}
\]

Fractional Calculus Engineering Laboratory

All these experiments are kept in Fractional Calculus Engineering Laboratory a first of its kind [14]. This laboratory provides a platform to develop Fractional Order Control Systems for industry and academic institutes. This laboratory is in use since November, 2016; at Dept. of EE, VNIT-Nagpur.

Conclusions

These practical demonstrations of implementation of fractional calculus in control science, gives a first of its kind a laboratory called ‘Fractional Calculus Engineering Laboratory’; where our aim is to have more fractional calculus based controllers and advanced methods developed for industrial usage. Though there is no commercial manufacturer or R&D institute using fractional calculus in controls,
but not limited to the above, and take this laboratory to industry houses and academic institutes & universities. However, it is satisfying to see the long standing conjecture/hypothesis of fuel/energy efficient controls is realized via using fractional calculus. Still we have miles to go.

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