A D-band CMOS power amplifier for short-range data center communication

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Abstract This letter presents a D-band wideband power amplifier (PA) in a 65-nm CMOS process. By pole-tuning technique with T-type network, the PA achieves a flat gain response over a wide bandwidth. The high output power is achieved by combining the output power of two PA cells using a Y-type power combiner (YPC). The fabricated prototype achieves a peak gain of 11.5 dB at 115 GHz with a 3-dB bandwidth of more than 21 GHz and a fractional bandwidth of larger than 17.5%. At the operating frequency of 120 GHz, the saturation output power and the output 1dB compression point are 13 dBm and 8.7 dBm, respectively. The chip occupies a small silicon area of 0.59 mm² including all testing pads with a core size of only 0.32 mm².

Keywords: CMOS, wideband power amplifier (PA), bandwidth extension, T-type network, pole-tuning

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

In recent years, various CMOS amplifiers operating in exceeding 100 GHz [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17] have been successfully demonstrated for extremely high data rate wireless communications, and the achieved rate is around 10 to 20 Gbps for short-distance data center applications [13, 15, 18, 19]. In order to achieve data rate communications of tens of Gbps or higher, the high order modulation schemes such as QPSK, 16-QAM, and 64-QAM are adopted for the advanced wireless systems. However, even though higher modulation scheme can be used, the availability of a wide system bandwidth is the key to obtain huge capacity and data rates. As critical building blocks, the amplifier must provide an extremely wide bandwidth. CMOS technology is great promising for millimeter-wave (mm-wave) transceivers due to its great advantages in cost, integration, volume and yield.

However, the design of D-band CMOS wideband power amplifier (PA) faces many issues, due to the limitation of the power gain of the devices, the low breakdown voltage, and the large parasitic effects. Various techniques are employed to mitigate these problems over past few years [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20]. Conventionally, the power combiner with transformer [4, 5, 6, 9, 10] is used to improve the limited output power. However, the transformer will cause large insertion loss at operating at frequencies beyond 100 GHz due to its inherent low-quality factor in CMOS process. Capacitive cross-coupling neutralization technique [5, 9] and conjugate matching [6], gain boosting [14], are employed to enhance the gain performance; however the two aforementioned techniques may the issue of stability when they operating at above 100 GHz. Besides, some bandwidth extension techniques demonstrated for wideband CMOS amplifiers. In [1, 2, 7, 8, 10, 11, 12] wideband CMOS amplifiers were achieved by using transmission lines for impedance matching, which leads to large silicon size. More recently, dual-frequency interstage conjugate matching [1], and pole-converging [11], are adopted for extending the bandwidth.

In this work, a wideband D-band PA is proposed in a 65 nm CMOS process is presented. By exploiting pole-tuning technique for interstage bandwidth extension, the fabricated prototype achieves a peak gain of 11.5 dB at 115 GHz with a 3-dB bandwidth of more than 21 GHz. The paper is organized as follows. Section 2 presents the analysis and design of wideband PA. Section 3 demonstrates the measured results. Finally, the paper is concluded in section 4.

2. Circuit design

2.1 Wideband power amplifier topology

The presented wideband PA consist of two Y-type power combiners and two PA cells, as plotted in Fig. 1. For PA cell, the first stage uses cascode structure to achieve high reverse isolation, while the other stages use common source structure to provide available gain and output power. Pole-tuning technique is adopted in the PA cell for interstage bandwidth extension. The high output power is achieved by combining the output power of two PA cells using the Y-type power combiner. The Y-type power combiner is implemented using TLs with defected ground structure (DGS) for a high-quality factor and a compact footprint.

2.2 Pole-tuning technique

At operating frequency beyond 100 GHz, parasitic effects have serious substantial influences on the transistor characteristics, leading to lower gain and narrower bandwidth. The
pole-tuning technique is a useful method for bandwidth extension during wideband amplifier designs [21, 22]. By shunting inductor $L_2$ and double-series inductors $L_1$ & $L_3$, forming a T-type network, which can serve as the function of a transformer, the bandwidth of the amplifier is extended due to pole tuning, as demonstrated in Fig. 2. The locus of dominant poles with variations of inductors $L_1$ ($L_2$) & $L_3$ are plotted in Fig. 2 (b). With the increasing of $L_1$ ($L_2$) & $L_3$, the pole $p_1$ ($p_2$) moves away from the imaginary axis and shifts to lower frequencies, while the pole $p_3$ ($p_4$) moves fast toward the imaginary axis and shifts to lower frequencies. As a result, the bandwidth of the amplifier is enhanced by the T-type network. To gain deeper physical insight into the effects from the T-type network, simulated frequency responses versus variations of $L_1$ ($L_2$) & $L_3$ are demonstrated in Fig. 3. As the inductance increases, the magnitude of the second peak is enhanced significantly while the first is restrained, loading a flat frequency response. Therefore, by using pole-tuning to optimize the T-type network, a flat frequency response over a wide bandwidth can be achieved.

As aforementioned, the T-type network has the same equivalent circuit model as the transformer. The T-type network should also be implemented through transformer. Thus, the transformer can serve as the function of a T-type network, and provide good interstage DC isolation. However, the transformer will cause a relatively large insertion loss operating at above 100 GHz frequencies due to its low-quality factor in CMOS process. As a result, the gain of the amplifier is seriously deteriorated. As shown in Fig. 4, the primary and secondary windings of a regular octagon transformer, the quality factors of which are 7 and 4 at 120 GHz, respectively, have an insertion loss of about 4 dB at 120 GHz.

Instead, the T-type network is implemented using arc-shaped TLs with DGS for a high-quality factor and a compact footprint. As plotted in Fig. 5, the main signal lines are realized by the sub top-metal M8 with thickness of 3.3 μm while the ground plane is designed by the bottom metal M1 with thickness of 0.22 μm.

To improve power supply filtering and reduce DC voltage dropout, a 10 μm × 10 μm layout cell with decoupling capacitor is designed for power and bias routing. Decoupling capacitors, which must resonate beyond the operation frequency of the amplifier, are usually placed at the end of parallel passive components to provide a low-impedance AC ground [23, 24]. As illustrated in Fig. 6, the gate of nMOS transistor is terminated by the metal M2 plane while the source and drain of its transistor are connected together...
with the M1 plane. In the design, the finger width of 7-μm and gate length of 9-μm are chosen for the nMOS transistor. The nMOS transistor form a large on-state capacitance when the metal M2 plane is set to 1.2 V. Fig. 6 shows the simulated on-state capacitance result versus variations operating frequencies. The on-state capacitance is decreases from 858 fF to 849 fF as operating frequency increases from DC to 200 GHz.

### 2.3 Y-type power combiner

The high output power is achieved by combining the output power of two PA cells using the YPC. In order to achieve more accurate EM characteristic, the GSG pads and the YPC were modeled as a whole in HFSS, as illustrated in Fig. 7. The YPC is designed using thick metal M8 as the main signal line and bottom metal M1 as ground plane. The DGS is adopted here to enhance the real-part impedance, and improve the balance of the output ports Port 2 and Port 3 [25, 26]. The opening in the ground plane disturbs the return current distribution and thus, the current is confined to the edges of two rectangle slots. This results in the enhancement of the effective inductance due to the increase in the length of the current return path, as illustrated in Fig. 8. Further, by changing the DGS dimension, the port impedance can be changed to achieve desired impedance matching and get an additional design freedom [27, 28]. Fig. 9 shows the EM simulation results for the YPC.

In this work, the passive components including all T-type network, inductors, testing pads, interconnections, metal vias, and so on, are optimized using 3-D EM simulator High-Frequency Structure Simulator and circuit co-simulations.

### 3. Measurement results

The proposed wideband PA was implemented with a 65-nm bulk CMOS process. A die microphotograph of the chip is shown in Fig. 10. The core area occupies only 600 μm × 530 μm and the whole chip area including all testing pads is 785 μm × 750 μm. The power consumption of the PA is 128 mW from both 2-V (VDD1) and 1.2-V (VDD2) supply voltages.

The S-parameters of the PA were performed from 110 to 170 GHz through on-wafer probing. The simulated and
measured S-parameters of the proposed CMOS amplifier are plotted in Fig. 11. It can be observed that the PA exhibits a very flat frequency-gain response (|S_{21}|) with a peak value of 11.5 dB at 115 GHz. The measured 3 dB gain bandwidth is from 110 GHz to 131 GHz that is limited by the available testing facilities, but the low corner frequency of the 3-dB bandwidth down to 102 GHz can be expected. The measured input return loss (|S_{11}|) and output return loss (|S_{22}|) remain better than 10 dB from 110 GHz to 135 GHz. The measured reverse isolation (|S_{12}|) is more than 38 dB from 110 GHz to 145 GHz. Compared with simulated results, the measured 3-dB bandwidth shifts down by ~7.2 GHz and the measured gain degrades by ~3.5 dB. The discrepancies between measured results and simulated results are mainly due to the existence of the randomized dummy metallization, which is added to pass design rule check (DRC) by the foundry during fabrication. Besides, the limited accuracy of the active device’s model operating at D-band that foundry provided is also a probable reason. The stability factor $K$ and delta $\Delta$ calculated from the measured $S$-parameters are demonstrated in Fig. 12. From 110 GHz to 145 GHz, the minimum $K$ of the amplifier is larger than 14, and the $\Delta$ is smaller than 1, which indicates that the proposed CMOS PA is unconditionally stable.

The power-handling capability $P_{1\text{dB}}$ is not measured at 120 GHz due to power limitation of our available testing facilities. Because the maximum output power from frequency extension module is less than $-10 \text{ dBm}$
at D-band that was well below the input $P_{1dB}$ of tested CMOS PA. Instead, the large-signal characterization performance was simulated at 120 GHz for the CMOS PA, as illustrated in Fig. 13. The proposed amplifier achieves a simulated saturation output power of 13 dBm with peak power-added efficiency (PAE) 14.7%, while the simulated output 1 dB compression point ($O_{P1dB}$) is 8.7 dBm. Table I [29, 30] summarizes the performance of the proposed PA and comparison with recently reported wideband PAs operating over 100 GHz frequency range.

4. Conclusion

The using of pole-tuning technique in the design of wideband PA is veriﬁed to effectively extend its 3-dB bandwidth, while maintain the available gain. The proposed PA exhibits a ﬂat frequency response from 110 GHz to 131 GHz with a peak gain 11.5 dB. At 120 GHz, the saturation output power is 13 dBm with peak PAE 14.7%, while the output $P_{1dB}$ is 8.7 dBm. The proposed PA is suitable for short-distance data center communication as one of the key building blocks.

Acknowledgments

This work was supported in part by the National Natural Science Fundamental of China under Grants 61774113, 61574102, and 61404094, and in part by the Fundamental Research Funds for the Central Universities, Wuhan University, under Grants 2042017gf0052.

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