A Novel Reversible Carry Look Ahead Adder for Bio-Medical Applications

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Abstract. Reversible logic is becoming more important in VLSI architecture in order to minimize power dissipation. In computational technologies like digital signal processing, nanotechnology, low-power CMOS, etc., this logic is used. If it comprises an equal count of inputs and an equal count of outputs that provide mapping, it is said to be reversible. This research work shows the realization of a Carry Look ahead Adder (CLA) using Reversible Partial Adder (RPA) and Peres Gate (PG) that achieves speed through parallel carry computations. By comparing the introduced research to previous work, the adder circuit’s output is measured. The simulation results indicate that the proposed reversible CLA achieves better area, power and delay reduction. The adder circuit can be incorporated as a useful feature in the low power design for biomedical devices because it is energy efficient and highly durable.

1. Introduction

In modern-day VLSI designs, power consumption is an important concern. Low-power architecture is becoming a major issue in high-performance digital devices such as microprocessors, digital signal processors, and other applications. Using irreversible gates such as AND, OR and EX-OR gates that dissipate an immense amount of heat in the bit type that is erased during logical operations may be used to implement a digital device. Thus, when the typical gates are used, the energy is lost. Reversible logic came into being and was realized by different researchers in order to solve this problem. Currently, this logic has become an exciting area of research, with implementations in a wide range of technologies. Reducing quantum costs, circuit depth and the amount of trash outcome are key goals of designing reversible logic. Peres gate, Feynman gate, TSG gate, Fredklin gate, are few among reversible gates.

A reversible logic incorporated with the CLA is implemented in this proposed work. To achieve reduced area and power, reversible gates like RPA and PG are proposed in the implementation. RPA is used for obtaining carry generated signals, propagated signals, also sum output. Peres gate generates carry output signals. Before the sum, one or more carry bits are calculated by this adder, which decreases the waiting time for the larger-value adder bits to be measured, thereby improving the speed.

2. Related works

Logical irreversibility is synonymous with physical irreversibility, according to [1], which involves limited heat generation per cycle of the machine. There is a probability of zero energy dissipation since
the number of bits lost during the process is directly proportional to the amount of energy dissipated in the device [2]. Full adder cell in which the internal logic structure based on the theory of transmission mechanism is presented [3]. Many researchers have adopted this structure as a standard structure for the single bit full adder cells to prevent intermediate signals from being present. Since the output blocks are powered by these intermediate signals and are thus responsible for greater propagation delay and power consumption. A novel full adder unit with internal rationale is planned to minimize these issues [4].

The decomposition of reversible logic was suggested by Perkowski et al. [5] and it grew in popularity due to the fact that it had no internal energy waste. In comparison to previous works, Himanshu et al. [6] developed a parallel adder using TSG gate in which area and power consumption are optimized. A reversible CLA circuit with two new designs is proposed in [7] with improved performance compared to the current designs.

Yingtao Jiang et al. [8] operated on a full multiplexer-based low-power 1-bit adder containing 12 transistors. When compared to a traditional 28-transistor CMOS adder, the new adder saves over 26% energy. Reversible logical gates are needed to design quantum circuits [9]. Quantum-dot Cellular Automata [10], which are substantially smaller than CMOS, is a novel technique in which reversible logic is employed in the Nano-scale technology. Examples in the literature include a reversible logic based full adder [11-14] with gate cost, garbage output and constant input. QCA nanotechnology is suggested in [15] to design and validate effective arithmetic units which have a number of issues that prevent large-scale growth.

Thapliyal et al. [16] have focused on a novel reversible look-ahead adder technique. Reversible binary coded decimal adder [17] is supported which allows the addition of binary values. CLA for nanometric parity preservation [18] indicate that the designs will be optimal. In [19], CLA is implemented based on fault tolerant gate and double feynman gate to reduce delay and area. An 8-bit adiabatic high speed adder with pipelined architecture is proposed by Mahmoodi-Meimand [20] that predicts the area, power and delay. A quick energy-efficient reconfigurable approximate parallel adder proposed in [21] allow up to 49 percent and 19 percent reduction in area and delay than other approximate adders.

3. Proposed work

This section proposes a reversible 4-bit CLA. It is the high-speed adder since it produces sum and carry output signals without any delay. It prevents ripples from being carried across each adder. CLA can be constructed initially with the implementation of partial full adder and carry propagation, carry generation blocks. Using reversible gates like reversible partial adder and peres gate, the implementation of the proposed adder is carried out. RPA that acts as a partial full adder is used to generate the outputs as sum, carry propagation and carry generation. The carry output is generated by PG.

3.1. Partial full adder

This adder is identical to a full adder which generates S, P, and G signals. The partial full adder shown in figure 1 consists of inputs (Ai, Bi, Ci) and outputs (Si, Pi, Gi) where the carry propagated output is represented by Pi, carry generated signal by Gi, and the sum output by Si.
3.2. Reversible partial adder

Figure 2 shows the 4*4 RPA gate, where Q is propagate signal, R is the sum and S is the generate signal.

\begin{align*}
A &\rightarrow P = A \\
B &\rightarrow Q = A \oplus B \\
C &\rightarrow R = A \oplus B \oplus C \\
D &\rightarrow S = AB \oplus D
\end{align*}

Figure 2. Reversible partial adder

Figure 3 shows its combinational logic diagram. By assuming D to 0, the proposed RPA can be used effectively.

Figure 3. Logic implementation of RPA
3.3. Peres gate

Figure 4 shows the reversible peres gate. Comparing to other gates, it has a minimum quantum cost. This gate can work as a half adder with $C = 0$.

$$A \rightarrow P = A$$
$$B \rightarrow Q = A \oplus B$$
$$C \rightarrow R = AB \oplus C$$

![Figure 4. Peres gate](image)

Figure 5 shows its combinational logic diagram.

![Figure 5. Logic implementation of Peres gate](image)

3.4. CLA based on reversible logic

Reversible CLA is built based on reversible partial adder and the peres gate. The reversible partial adder is used to produce sum and carry generate, propagate signals. These signals are then sent to the peres gate that generates carry output signals. The schematic diagram of carry generation and carry propagation signals using RPA gate is shown in figure 6. This 4-bit Reversible Partial Adder (RPA 0–RPA 3) produces 4-bit carry generated signals (G0–G3), carry propagation signals (P0–P3) and sum output (S0–S3).

![Figure 6. Carry generation and carry propagation using reversible partial adder](image)
3.5. Design of Reversible CLA

Figure 7 shows the architecture of 4-bit reversible logic based CLA and its construction method is as follows: First, by means of reversible partial adder, 4-bit propagated carry and generated carry signals are obtained. Secondly, using a peres gate, carry-out signals are produced based on the propagated and generated carry signals.

4. Results & discussion

4.1. Simulation output of existing reversible CLA

In the previous work, CLA is developed based on PG and feynman gate and implemented in Xilinx 14.3 tool ISE design suite. Figure 8 shows the simulation output which represents a[3:0], b[3:0], C_in are the inputs and s[3:0], C_out is the output.
4.2. Simulation Output of proposed reversible CLA

The proposed CLA is designed using RPA with PG and implemented in Xilinx 14.3 tool ISE design suite. The simulation output shown in figure 9 represents $a[3:0]$, $b[3:0]$ and $C_{in}$ are the inputs and $s[3:0]$, $C_{out}$ is the output.

5. Performance Analysis

5.1. Comparison Analysis

The proposed reversible CLA is analyzed with respect to earlier CLA circuit [6] and it is evident from table 1 and figure 10 that the proposed CLA offers better results.
Table 1. Comparative analysis

| S.No. | Device Utilization | Existing Reversible CLA [6] | Proposed Reversible CLA |
|-------|-------------------|-----------------------------|-------------------------|
| 1.    | Number of gates   | 12                          | 6                       |
| 2.    | Stable inputs     | 8                           | 7                       |
| 3.    | Trash outputs     | 12                          | 6                       |

Figure 10. Performance analysis of proposed reversible CLA with existing reversible CLA

5.2. Analysis of the proposed circuit with respect to parameters

The newly presented CLA is analyzed with the existing CLA [6] in terms of parameters such as area, delay and power.

Table 2. Parameters of existing and proposed reversible CLA

| S.No. | Circuit                                | Area | Delay (ns) | Power (mw) |
|-------|----------------------------------------|------|------------|------------|
| 1.    | Existing reversible Carry Look Ahead adder [6] | 12   | 14.40      | 9.53       |
| 2.    | Proposed Reversible Carry Look Ahead adder | 6    | 6.49       | 4.67       |

It is revealed from table 2 that the implemented CLA delivers a lesser gate count, low delay and power when evaluated to the previous designs and its analysis is indicated in figure 11. This suggests that the reversible CLA requires less energy in biomedical applications.
Figure 11. Performance parameters of existing and proposed reversible CLA

6. Conclusion

In this proposed work, a new CLA based on reversible gates like RPA and PG is presented. It is evident that the RPA gate is best suited for producing the carry generation, carry propagation, sum output and peres gate for carry output computations. It is concluded from the experimental outcome that the presented CLA provides enhanced performance in contrast to the earlier works. Thus this newly introduced CLA results in gate reduction of about 50%, 55% of delay and 51% of power with already available reversible CLA designs. Finally, the presented work demonstrates the practical utility of a reversible CLA in IC design for bio-medical applications, offering a viable alternative for power and energy savings in complex arithmetic blocks.

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