Functionalized pentacene field-effect transistors with logic circuit applications

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Abstract

Functionalized pentacene, 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene), field-effect transistors (FET’s) were made by thermal evaporation or solution deposition method and the mobility was measured as a function of temperature and light power. The field-effect mobility ($\mu_{\text{FET}}$) has a gate-voltage dependent activation energy. A non-monotonic temperature dependence was observed at high gate voltage ($V_G < -30$ V) with activation energy $E_a \sim 60 - 170$ meV, depending on the fabrication procedure. The gate-voltage dependent mobility and non-monotonic temperature dependence indicates that shallow traps play important role in the transport of TIPS-pentacene films. The current in the saturation regime as well as mobility increase upon light illumination and is proportional to the light intensity, mainly due to the photoconductive response. Transistors with submicron channel length showed unsaturating current-voltage characteristics due to the short channel effect. Realization of simple circuits such as NOT (inverter), NOR, and NAND logic gates are demonstrated for thin film TIPS-pentacene transistors.

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I. INTRODUCTION

The use of organic material for the electronic devices has great importance for future application due to its low cost and easy fabrication procedures. Pentacene, one of most promising organic material for device application, has been studied intensively in polycrystalline or single crystalline structures due to its high room temperature hole mobility more than 1 cm$^2$/Vs. And other polyacene single crystals such as tetracene, anthracene as well as thin film structures were also investigated.

By attaching the side functional group, soluble and stable functionalized pentacene can be made and this make its fabrication methods versatile and increase application for devices. Transport measurement depending on its crystal direction shows different conducting properties and the persistent photoconductivity was already reported. Field-effect transistor (FET) application of these functionalized pentacene was shown and they can get room temperature mobility up to 0.4 cm$^2$/Vs with deposition under substrate heating and gate dielectric with self-assembled monolayer. Temperature dependence of mobility is key to elucidate its quality and transport mechanism. In the case of field-effect mobility, band-like temperature dependence is very rare and only observed at high temperature range in single crystal and thin film.

In addition to the electrical applications, its photosensitive properties can be used as light detector or optical switch. Light responsive properties of organic transistor have not been investigated as much as electrical properties. The performance of photoresponsivity in polymer and pentacene is still lower than that of amorphous silicon ($\sim 300$ A/W). However, this can be improved by optimization of device fabrication.

In this article, we report the electrical and optical properties of 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene) FET. For the electrical properties, we measured field-effect mobility of thin film or single crystal transistor. In temperature dependence, field-effect mobility exhibit gate voltage dependent activation energy and it shows nonmonotonous temperature dependence at $V_g < -30$ V region. This was also observed irrespective of fabrication method. At nanoscale electrodes we cannot observe current saturation as in the case of micron scale FET. The light illumination above absorption edge of TIPS-pentacene enhanced the saturation current of transistor more than 4 orders of magnitude and slightly increased its mobility. By adding off-chip resistor
to thin film transistor, we realized logic circuits such as NOT, NAND, and NOR at room temperature.

II. EXPERIMENT

TIPS-pentacene (Fig. 1 (a)) was synthesized as described in elsewhere\cite{6} and it was thermally evaporated with ($\sim 70 ^\circ C$) or without substrate heating at base pressure less than $5 \times 10^{-6}$ Torr. After drying of 2 wt. % toluene solution droplet, single crystalline films are formed on the surface. Predefined microelectrodes from photolithography with channel length ($L$) of 5 $\mu$m $\sim$ 40 $\mu$m and channel width ($W$) of 400$\mu$m $\sim$ 6 cm were used for source and drain contacts and heavily doped n-type Si substrate ($\rho < 0.002 \ \Omega \text{cm}$) served as a back gate. Thermally grown 300 nm SiO$_2$ layer used for gate dielectric without molecular modification. For the nanoelectrodes fabrication, we used e-beam lithography and lift-off process. Electrodes with 200 nm channel length and 2 $\mu$m channel width were used for nanochannel FET. The thickness of TIPS-pentacene is 50 nm to 800 nm and all the devices are bottom contact configuration.

Figure 1 (b) is typical scanning electron microscope (SEM) image of evaporated TIPS-pentacene film. Its X-ray diffraction data (not shown) shows clear c-axis orientation as evaporated pentacene film. Electrical characterization is performed using HP 4155C semiconductor parameter analyzer.

III. RESULTS AND DISCUSSION

A. Thin film and single crystalline transistor

Figure 2 is typical output characteristics of TIPS-pentacene FET at room temperature and inset shows transfer characteristics in the saturation regime ($V_{DS} = -25$ V). The gate voltage, $V_g$, was swept from 0 to -40 V in both cases. This device has room temperature mobility of 0.02 cm$^2$/Vs and on/off current ratio higher than $10^6$. The estimated subthreshold slope is 2.6 V/decade, that is comparable to the pentacene thin film and higher than some single crystal.\cite{15} Without any modification of electrodes and substrate, most of the samples have room temperature mobility between 0.002 to 0.03 cm$^2$/Vs.
The solution deposited film and evaporated thin film with substrate heating have slightly higher room temperature mobility of 0.08 cm$^2$/Vs and 0.05 cm$^2$/Vs and subthreshold swing of 3.8 V/decade and 2.1 V/decade respectively.

Several groups have measured single crystal FETs\[2, 3, 4, 16\] to get intrinsic properties of organic FET. We also have used TIPS-pentacene single crystal as synthesized and put it on top of electrodes under microscope. To improve contact, transparent polydimethylsiloxane (PDMS) stamp was laid on the crystal as described in elsewhere\[4\]. The schematic diagram and its optical image was shown in Fig. 3 (a). The channel length is 100 $\mu$m and effective channel width from the image is 300 $\mu$m. The output characteristics (Fig. 3 (b)) also show current enhancement at negative gate voltage and transfer characteristics ($V_{DS} = -40$ V) in the inset show room temperature mobility $\sim$ 0.007 cm$^2$/Vs and subthreshold swing of around 10 V/decade. Compared to the previous mentioned evaporated or solution deposited FET, the mobility is decreased and subthreshold swing is increased. A single crystal FET is very sensitive to surface status, however, from the optical microscope image the thickness of crystal is not uniform and the crystal direction is not optimized. Therefore, this can be improved in uniform and thin crystal with optimized crystal arrangement.

**B. Temperature dependence of mobility**

Figure 4 (a) shows temperature dependence of mobility at different gate voltages in evaporated film. To avoid persistent photoconductivity\[8\] we kept the sample in dark condition for a while. At low gate voltage, mobility shows monotonous temperature dependence with $\mu_{FET} \sim \exp(-E_a/k_B T)$ but at high gate voltage, it reaches maximum value ($T \sim 250$ K) and decreases with decrease of temperature. Unlike the gate-voltage independent mobility of tetracene or rubrene single crystals\[3, 16\], mobility of TIPS-pentacene thin film is gate-voltage dependent and increase linearly upon gate voltage. This means that induced charge carrier contribute to the conduction. And trap and grain boundary are important to this activation type conduction. Inset shows the change of activation energy depending on the gate voltage. The activation energy at low gate voltage is $E_a \sim 0.27$ eV, which is lower than that of bulk experiment(550 meV).\[8\] The activation energy decreased down to 60 meV with increasing gate voltage. This kind of gate voltage dependent activation process was widely observed in thin film pentacene\[17, 18\], single crystalline pentacene\[2, 19\].
or oligothiophene [19]. At low temperature region \((T < T_m)\), the activation energy is 60 - 80 meV at high gate voltage \((-40 \text{ V} < V_g < -30 \text{ V})\) region.

Typical temperature dependences of FET mobility from different fabrication processes are shown in Fig. 4 (b). Generally, FETs fabricated with substrate heating or deposited from solution have higher room temperature mobility than normally deposited film. Thin film with substrate heating has activation energy, \(E_a = 110 - 170 \text{ meV}\) with no mobility maximum in measured temperature range \((T_m > 310 \text{ K})\). On the other hand, activation energy of solution deposited film and thin film evaporated without substrate heating is 110 meV and 70 meV respectively. From all the temperature dependence, sample with higher \(T_m\) has high \(E_a\), which means that trap is more dominant in this case therefore intrinsic transport is suppressed. To explain this nonmonotous temperature dependence, several group have adopted following equation [3, 4]

\[
\mu \sim T^{-n}\exp\left(-\frac{E_t}{k_B T}\right) \quad (1)
\]

where \(E_t\) is the shallow trapping energy and \(k_B\) is the Boltzmann constant.

This nonmonotous temperature dependence can be understood that in the high temperature region, microscopic mobility would be dominant (i.e., intrinsic) and for low temperature region, thermally activated mobility would be important due to traps. This was widely observed in tetracene [3], anthracene [4], rubrene [16], and thin film pentacene [11].

The activation energy of TIPS-pentacene is larger than thermally evaporated pentacene thin film transistor \((38 \text{ meV} \text{ with room temperature mobility of } 0.3 \text{ cm}^2/\text{Vs}) [11]\) but less than precursor-route pentacene thin film [17].

The gate-voltage dependent mobility and nonmonotous temperature dependence mean that shallow traps play important role in the transport of TIPS-pentacene film.

C. Light illumination

We illuminated 30 mW He-Ne laser \((\lambda = 632.8 \text{ nm})\) to the evaporated TIPS-pentacene FET, channel length of 5 \(\mu\text{m}\) and channel width 6 cm. Since the absorption edge of TIPS-pentacene is around 700 nm, there is nearly 4 orders of current increase upon light illumination (Fig. 5 (a)). With \((V_g= -40\text{V})\) or without gate voltage, the current gain, \(I_{d\text{light}}/I_d\), due to light is \(\sim 10^4\). Illumination on the device generate electron-hole pairs in the channel.
TABLE I: Summary of TIPS-pentacene FET characteristics at room temperature

| Sample                 | mobility (cm²/Vs) | V<sub>T</sub> (V) | subthreshold swing (V/decade) | E<sub>t</sub> (meV) |
|------------------------|------------------|------------------|-------------------------------|--------------------|
| thin film<sup>a</sup>  | 0.02             | -14              | 1.9                           | 70                 |
| thin film<sup>b</sup>  | 0.08             | -18              | 2.1                           | 110                |
| single crystalline<sup>c</sup> | 0.05         | -12              | 3.8                           | 170                |
| single crystalline<sup>d</sup> | 0.007        | -15              | 10.0                          | na                 |

<sup>a</sup>without substrate heating.
<sup>b</sup>substrate heating at 70 °C.
<sup>c</sup>solution processed.
<sup>d</sup>as synthesized.

as well as in bulk TIPS-pentacene. Current saturation indicates that it is also channel restricted as observed in photoresponsive polymer FET<sup>12</sup>. Estimated photoresponsivity, shown in Fig. 5 (a), is around 0.03 A/W and we can get up to 0.4 A/W in some devices.

We used filter to control optical power. As shown in Fig. 4 (b), light illumination increases the source-drain current (I<sub>DS</sub>) and mobility in proportion to optical power. Unlike semi-logarithmic response of I<sub>d</sub> vs intensity in phototransistor<sup>20</sup>, photocurrent increase with light intensity, I<sub>ph</sub> ∝ P<sub>opt</sub><sup>α</sup>. In most photoconductive polymer films and organic materials, this exponent α = 1. However, in the case of bimolecular recombination instead of monomolecular recombination, α = 0.5<sup>21</sup>. The exponent of saturated current, I<sub>d,sat</sub> vs. optical power in Fig. 5 (b) is 0.78. When there is carrier traps, immobilized carrier cannot participate to recombination. This smaller exponent less than one means that traps play important role.

Generally, the increase of carrier density (∆N) can be estimated from ∆N = C<sub>i</sub> · ∆V<sub>T</sub>/e, where C<sub>i</sub> is the dielectric capacitance per unit area and ∆V<sub>T</sub> is the shift of the threshold voltage. In this device, ∆V<sub>T</sub> is around 30 V, hence ∆N can be estimated to be 1.9 × 10<sup>12</sup>/cm<sup>2</sup>. In the case of pentacene<sup>14</sup> or GaN nanowire<sup>22</sup>, light illumination increase only the carrier concentration and has small effect on the mobility. TIPS-pentacene shows mobility increase by factor of 5 upon light illumination.
D. Nanoscale FET

We reduced the channel length in the submicron range. The gate-dependent I-V characteristics of 200 nm channel length and 2 µm channel width FET is shown in Fig. 6. TIPS-pentacene was thermally evaporated on top of electrodes that was predefined by e-beam lithography. Unlike the micron scale FET, it doesn’t show any current saturation. This is due to short channel effect \[23, 24\], that source-drain electrodes themselves make depletion, and space charge limited conduction (SCLC) is preventing current saturation. The SCLC follows \[I_D \propto V_{DS}^n\], where \(n\) depends on the trap concentration and typically larger than 2. In TIPS-pentacene nanoscale FET, exponent \(n\) is between 2.5 and 3 (shown in the inset of Fig. 6).

Since there is no saturation region in this device, we assume the lower voltage region to linear regime of transistor for the estimation of mobility.

\[
\frac{\partial I_D}{\partial V_{GS}} = \frac{W}{L} \mu C_i V_{DS}
\]  

(2)

where \(C_i\) is the gate insulator capacitance per unit area.

The estimated mobility is 0.002 cm\(^2\)/Vs (at \(V_{DS} = -2.5\) V), that is similar to lower mobility sample in Fig. 4 (b).

E. Logic gate application

We have fabricated inverter (NOT) using this p-type TIPS-pentacene FET and off-chip resistor as shown in schematic diagram of Fig. 7 (a). A FET with room temperature mobility of 0.002 cm\(^2\)/Vs (thickness of 50 nm) and serial resistor of 10 MΩ were combined for inverter. When the input voltage is \(V_{in} \geq 2\) V (logical 0), the transistor resistance is larger than that of series resistor, therefore \(V_{out} = -10\) V (logical 1). When \(V_{in} = -10\) V (logical 1), the transistor resistance is lower than that of series resistor and \(V_{out} = 0\) V (logical 0). The maximum gain defined by \(dV_{out}/dV_{in}\) is up to 5.5 (other inverter shows gain up to 8) from the voltage sweep with driving voltage of -10 V. This value is comparable to other pentacene inverters \[1, 25\]. And this gain value increase as increase \(V_d\) as mentioned in Ref. \[25\]. Since all measurements for logic circuits were done under ambient condition, the device is normally "on" with positive threshold voltage at room temperature. Some
fresh device show negative threshold voltage but in ambient condition it shifted to positive as time goes on. That is the reason why we have to apply positive gate voltage, \( V_{in} \) to ”off” the FET. In actual application, this need additional level-shifting circuit. To avoid this complication, it’s important to reduce air exposure and light illumination.

By adding one more FET, NAND (Fig. 7 (b)) and NOR (Fig. 7 (c)) logic were constructed. Since the FET is ”on” at zero gate voltage (i.e. positive threshold voltage), we applied positive gate voltage to ”off” the transistor. In this operation, we used ”+10 V” for off state. Due to mismatch of current and mobility of two transistors, there is shift of offset voltage in ”off” state.

IV. SUMMARY

In summary, we measured the temperature dependence of mobility of functionalized pentacene(TIPS-pentacene). It shows gate-voltage dependent activation energy that is in the 60 - 170 meV at high gate voltage (\( V_g < -30 \) V) depending on the fabrication procedure. Temperature dependence can be ascribed to shallow trapping of charge carriers. Light illumination increase the mobility but it is photoconductive response. Logic gate circuit were also demonstrated. Inverter has gain upto 5.5 that is comparable to other pentacene device and NAND and NOR logic gates were also presented.

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FIG. 1: (a) Chemical structure of TIPS-pentacene. (b) SEM image of thermally evaporated TIPS-pentacene
FIG. 2: Typical output characteristics of TIPS-pentacene transistor with channel length of 5 µm and channel width of 6 cm in "bottom" contact configuration. From the transfer characteristics, estimated subthreshold slope is 2.6 V/decade and mobility is 0.02 cm²/Vs with threshold voltage of $V_T = -14$ V.
FIG. 3: (a) Schematic diagram for single crystal FET pressed by PDMS to improve contact and its optical microscope image. (b) Output characteristics measured at room temperature. Inset shows transfer characteristics at $V_{DS} = -40$ V.
FIG. 4: (a) Temperature dependence of mobility at different gate voltage. TIPS-pentacene was deposited without substrate heating. Inset shows the change of activation energy upon gate voltage. It decreases from 0.27 eV ($V_G = -5V$) to 60 meV ($V_G = -40V$). (b) Temperature dependence of mobility from different fabrication processes such as evaporated thin film with (♦) or without substrate heating (■) or solution deposition (●).
FIG. 5: (a) Change of I-V characteristics of TIPS-pentacene under the illumination of He-Ne laser (632.8 nm, 30 mW) without gate voltage. (b) $I_{DS}$ (at $V_{DS} = -40$ V, $V_G = 0$ V) and field-effect mobility as a function of illuminated light power at ambient condition.
FIG. 6: Gate effect of nanochannel FET of TIPS-pentacene. There is no current saturation in nanoscale device due to short channel effect. Inset shows log-log plot of output characteristics, which follow SCLC.
FIG. 7: (a) inverter, (b) NAND gate logic, and (c) NOR gate logic circuit made from thin film TIPS-pentacene with room temperature mobility of 0.003 cm²/Vs. Loading voltage ($V_d$) of -10 V and off-chip resistor of 10 MΩ are used in the circuit.