It has been suggested that all resistive-switching memory cells are memristors. The latter are hypothetical, ideal devices whose resistance, as originally formulated, depends only on the net charge that traverses them. Recently, an unambiguous test has been proposed to determine whether a given physical system is indeed a memristor or not. Here, such a test is experimentally applied to both in-house fabricated Cu-SiO$_2$ and commercially available electrochemical metallization cells. The results unambiguously show that electrochemical metallization memory cells are not memristors. Since the particular resistance-switching memories employed in the study share similar features with many other memory cells, the findings refute the claim that all resistance-switching memories are memristors. They also cast doubts on the existence of ideal memristors as actual physical devices that can be fabricated experimentally. The results then lead to formulate two memristor impossibility conjectures regarding the impossibility of building a model of physical resistance-switching memories based on the memristor model.

Although some publications$^{[1,2]}$ have claimed that the memristor$^{[3]}$ (in the ideal sense) has been found and all resistance-switching memories are memristors,$^{[4]}$ several researchers have raised serious doubts about such claims.$^{[5–10]}$ Indeed, the property of pinched hysteresis loops$^{[10,11]}$ alone (“If it’s pinched it’s a memristor”) cannot serve as a good indicator of memristors since that property is shared by different types of experimentally realizable devices (such as memristive devices and systems whose memory depends on some internal degrees of freedom, other than the charge$^{[11]}$).

Remarkably, the most important characteristic of any memristor,$^{[3]}$ namely, the functional dependence of its memory resistance (memristance), $R_M$, on only the net charge, $q$, that traverses it, $R_M(q)$, has never been demonstrated experimentally. However, it is obvious that any claim of the “memristor discovery” must be based on the experimental measurement of $R_M(q)$, and not merely on non-exclusive characteristics. Of course, since physical devices are not ideal, like any other circuit component (such as resistors, capacitors, and inductors), the memristor (if found) would show some deviations from the ideal behavior, depending on the operation conditions. However, such deviations should be small, say, within 10% of the ideal $R_M(q)$ curve, for such a device to be a good representation of its ideal counterpart. Otherwise, it would be a totally different device altogether.

In ref. [14], two of us (YVP and MD) have introduced a simple test to experimentally determine whether a resistor with memory is an ideal memristor or something else. The main idea of the test is based on the duality property of a capacitor–memristor circuit, whereby for any initial resistance state of the memristor and any form and amplitude of the applied voltage, the final state of an ideal memristor must be identical to its initial state, if the capacitor charge finally returns to its initial value.$^{[14]}$ In other words, our test verifies the $R_M(q)$ dependence.

To prove the ideality, a scan over a large range of parameters (initial state, shape/magnitude of the applied voltage, etc.) is clearly required. To prove the opposite, however, even one or a few measurements demonstrating the absence of such a duality within the operating range of the device would be enough. Here, we report the results of more than 60 memristor tests performed over several kinds of resistance switching devices using triangular and rectangular voltage pulses of positive and negative polarities. The results of these tests are in mutual agreement, and in agreement with the theoretical modeling of ref. [14].

In the present paper, we experimentally apply the ideal memristor test$^{[14]}$ to in-house fabricated Cu-SiO$_2$ and commercially available electrochemical metallization cells as model resistance-switching devices. Electrochemical metallization cells (ECMs)$^{[15]}$ constitute a large family of resistance-switching devices based on the cation diffusion through a solid electrolyte. Typically, such cells exhibit bipolar resistance switching with thresholds. This property allows us to use the tested devices as representatives of the entire class of bipolar threshold-type resistance-switching cells,$^{[16]}$ which also includes valence change memory cells (VCMs).$^{[17]}$ Moreover, to demonstrate explicitly that VCMs are not memristors,
Here, we present the results obtained at HP group. \[18\] We have found that the device resistance can be driven by several values of the pulse amplitude. We have also plotted the \( R_M(q) \) dependence of TaO devices for several driving conditions using an accurate model developed by the HP group.\[18\] We have found that the device resistance can not even be approximately described by the ideal relation \( R_M = R_M(q) \).

Our results show that the resistance-switching memories are not memristors, and cast further doubts on the existence of ideal memristors as actual physical devices that can be fabricated in the laboratory or found in Nature. This leads us to formulate two memristor impossibility conjectures, namely, that i) it is impossible to accurately model physical resistance-switching memories by adding small corrections to the ideal memristor model, and ii) it is impossible to build a circuit combining ideal memristors with any other ideal two-terminal devices (resitors, capacitors, and inductors) that emulates realistically the response of experimentally-realizable resistance-switching memories.

Figure 1a shows typical current–voltage characteristics of a selected Cu-SiO\(_2\) device. This plot demonstrates a bipolar switching with well-defined thresholds, and a hysteresis loop twisted at the origin. From this plot, we estimate the following parameters of our device: \( R_{on} \approx 19.5 \, \text{k}\Omega, R_{off} \approx 150 \, \text{k}\Omega, V_{+} \approx 0.7 \, \text{V}, \) and \( V_{-} \approx -0.8 \, \text{V}. \) Here, \( R_{on/ff} \) are the boundary resistance values and \( V_{+/-} \) are the threshold voltages.

The ideal memristor test, as represented in Figure 2, was performed at several values of the pulse amplitude \( V_0 \) (see Figure 2b) with the initial memristance set to \( R_M = 53 \, \text{k}\Omega. \) Here, we present the results obtained at \( V_0 = 0.4 \, \text{V} \) and \( V_0 = 1 \, \text{V}. \) Since these measurements were performed in sequence, the final state after the application of \( V_0 = 0.4 \, \text{V} \) served as the initial state for \( V_0 = 1 \, \text{V}. \) We emphasize that according to the test procedure, the initial and final charge on the capacitor is the same. Therefore, if the tested device were a memristor, its final and initial memristance would be the same too.

It is found that for \( V_0 = 0.4 \, \text{V} \), the final memristance is the same as the initial one (cf. Figure 3a,c). However, the larger value of \( V_0 = 1 \, \text{V} \) causes the device to switch into the lowest resistance state, \( R_{on} = 19.5 \, \text{k}\Omega \) (see Figure 4). As the final device state is different from the initial one when the capacitor has discharged, we conclude that our device has not passed the ideal memristor test. We observed similar results for all the other samples tested. Therefore, none of our devices have passed the ideal memristor test.

We note that the test was performed using 40 \( \mu \text{A} \) current compliance, which was not exceeded during the test. However, due to the nature of our test, its conclusions are independent of whether the current was limited or not by the compliance current. Moreover, the transition regions in the \( I(t) \) curves at \( t = 13.5 \, \text{s} \) in Figure 3 and \( t = 26 \, \text{s} \) in Figure 4 correspond to the capacitor discharge process. Zero current at the final moment of time indicates that the capacitor has been discharged.

We have also applied the memristor test to commercially available EMCs (Knowm, Inc.). Their operation is based on the movement of Ag atoms through a stack of chalcogenide layers with one of Ge\(_2\)Se\(_3\) layers doped either by W (BS-AF-W devices) or Cr (M+SDC Cr devices). The current–voltage curves of the samples used in the memristor test are presented in Figure 1b,c. Their form indicates the bipolar resistance switching mode, similar to the one in Figure 1a. We note that
the switching thresholds of the Knowm devices are smaller than those in our Cu-SiO$_2$ devices. Moreover, a large $R_{\text{off}} \approx 500 \ \Omega$ was observed in the M+SDC Cr device. To reduce the capacitor discharge time, we used a smaller $1 \ \mu F$ capacitor in experiments with the Knowm devices.

A series of more than 30 tests were applied to each BS-AF-W and M+SDC Cr sample. In these tests, we used the triangular (like in Figure 2b) and rectangular pulses of positive and negative voltage. The width of rectangular pulses was $2 \ \text{s}$; the slope of triangular pulses was about $0.025 \ \text{V s}^{-1}$. The resistance was measured using a $10 \ \text{mV}$ voltage; the waiting time before the final resistance measurement was $\geq 3 \ \text{s}$. The pulses were applied in an arbitrary order, and the results of these measurements are summarized in Figure 5.

Each point in Figure 5 corresponds to a single measurement like the one in Figure 3 or 4. For reference, the straight line represents the condition of equal initial and final states, $R_{\text{M},f} = R_{\text{M},i}$, and dashed lines correspond to $10 \ %$ deviations from this condition. So, if the device under test were a memristor, the measurement results would group between the dashed lines. Clearly, it is not the case of both BS-AF-W and M+SDC Cr electrochemical metallization cells. In agreement with the results of Figure 4, the tendency of $R_{\text{M},f} < R_{\text{M},i}$ for positive triangular pulses, and $R_{\text{M},f} > R_{\text{M},i}$ for negative triangular pulses can be recognized. In the case of rectangular pulses, the tendency is opposite as the final state is significantly defined by the falling front of the pulse. Overall, as most of the data point are outside of the dashed line interval, the conclusion is that also the Knowm devices are not memristors.

As VCMs are the second major class of resistive memory devices, it is of interest to understand how close their behavior is to the memristor model. For this purpose, we consider the transient dynamics of TaO cells, a representative of VCMs devices, and employ Equations (1) and (2) from Experimental Section to discuss their dynamics, as these have been shown to accurately reflect the experimental data.\[18\]

Figure 6 shows the resistance as a function of charge that flows through the cell found for a set of applied voltages. One can notice that starting from the same point, the $R_{\text{M}}(q)$ curve actually splits into individual curves for each voltage. Clearly, there is no single $R_{\text{M}}(q)$ that ideal memristors would satisfy, or a grouping around a certain $R_{\text{M}}(q)$ that could be taken into account by small corrections to the ideal model.

---

**Figure 3.** Ideal memristor test performed at $V_0 = 0.4 \ \text{V}$, $C = 10 \ \mu \text{F}$. a) A low-amplitude sweep is used to test the initial memristance (the relay is closed). b) Voltage and current versus time, when the testing voltage is applied (the relay is open). c) A low-amplitude sweep is used to test the final memristance (the relay is closed). The fitting lines in (a) and (c) correspond to the same $R_{\text{M}} = 53 \ \text{k}\Omega$.

**Figure 4.** Ideal memristor test performed at $V_0 = 1 \ \text{V}$, $C = 10 \ \mu \text{F}$. a) A low-amplitude sweep is used to test the initial memristance (the relay is closed). b) Voltage and current versus time, when the testing voltage is applied (the relay is open). c) A low-amplitude sweep is used to test the final memristance (the relay is closed). The fitting line in (a) corresponds to $R_{\text{M}} = 53 \ \text{k}\Omega$, while in (c) to $R_{\text{M}} = 19.5 \ \text{k}\Omega$.
We can further expand on these experimental results as follows: In this work, we have applied the ideal memristor test suggested in ref. [14] to in-house fabricated Cu-SiO$_2$-based ECMs and commercially available Ag-based ECMs, which are a type of resistance-switching memories. As part of the test, we have compared the initial device states with the final ones.

Figure 5. Final versus initial resistance found in a series of tests (with C = 1 μF) using triangular (T, as in Figure 2) and rectangular (R) pulses of positive and negative polarities. Results for BS-AF-W and M+SDC Cr devices are shown in (a) and (b), respectively. The dashed lines correspond to 10% deviation from $R_{M,f} = R_{M,i}$ line.

Figure 6. Resistance as function of charge that flows through a TaO device found for the cases of a) negative and b) positive constant voltages. These plots were obtained using Equations (1) and (2) from Experimental Section model with $x(t = 0) = 0.9$ in (a) and $x(t = 0) = 0.1$ in (b).
Chua argued that the resistance-switching memories are an exception of physical devices is different from the ideal behavior, see, e.g., ref. [16]. Accounting for the fact that the devices such as those studied experimentally in this work, or the memistor model is related, if at all, to physical resistance-switching memories are not memristors, irrespective of their specific device structures and switching mechanisms.

We also note that the triangular-shape voltage signal \( V(t) \) employed in our work has facilitated the ideal memistor test. Under the test conditions of Figure 2, the tested devices were subjected first to a relatively large positive voltage (the initial magnitude is \( V_0 \)), followed by a small negative voltage. The tested devices failed the test since the positive voltage across the devices was sufficient to switch \( R_M \) to \( R_m \), while the negative voltage was not sufficient for the inverse switching. Since, in principle, for any given pair of \( V_+ \) (positive voltage) and \( V_- \) (negative voltage), one can always choose the test signal such that \( V_0 > V_+ \) and \( V_M(t) > V_- \), one can further argue that there are no ideal memristors among the threshold-type resistance-switching memory cells.

At this juncture, the reader may ask how the ideal memistor model is related, if at all, to physical resistance-switching devices such as those studied experimentally in this work, or any other resistance-switching devices published in the literature, see, e.g., ref. [16]. Accounting for the fact that the response of physical devices is different from the ideal behavior, Chua argued that the resistance-switching memories are an “unfolding” theory extension of the ideal devices. More recently, he also proposed that the resistance-switching can be represented by a circuit combining ideal memristors with some other ideal devices. However, these statements are clearly incorrect.

In fact, unfolding relies on families of mathematical functions that are similar (close) to each other. When an idealized model is partially inadequate, the model can be improved by adding small corrections resulting in the new model: an unfolding of the original system. However, this approach is not applicable to the physical (experimentally-realizable) memristive devices because the difference between their physical models (as known in the literature) and the ideal memistor model cannot be bridged by small correction terms. Similarly, a circuit representation of physical memory devices by circuits of ideal components is highly unlikely for the same reason: the ideal memistor behavior is too different from that of physical devices.

Based on the above arguments, we formulate two memistor impossibility conjectures that may serve as foundations for future research.

**First memistor impossibility conjecture**: It is impossible to accurately model physical resistance-switching memories by adding small corrections to the ideal memistor model.

**Second memistor impossibility conjecture**: It is impossible to accurately model physical resistance-switching memories by a circuit combining ideal memristors with any kinds of non-linear ideal circuit elements.

In the second conjecture, we refer to the ideal elements defined in ref. [21]. It can be also formulated in the strong sense considering only the combinations of memristors with basic circuit elements (non-linear resistors, capacitors, and inductors).

In conclusion, we have employed a recently suggested test to experimentally verify whether currently existing resistance-switching memories are indeed memristors, as it was claimed in ref. [4], or not. Our results demonstrate unambiguously that they are not. Unlike the behavior of ideal memristors, the final states of the memory devices we have measured significantly deviate from their initial states. These deviations cannot be accounted for by small corrections to the ideal memistor relations.

This study has then led us to formulate two conjectures on the impossibility of building a model of physical (experimentally realizable) resistance-switching memories based on the ideal memistor behavior. The collection of these experimental results cast further doubts on the existence of the ideal memistor as a fourth circuit element that can be fabricated experimentally. In fact, various previous results reported in the literature such as, for example, threshold-type hysteresis curves of physical devices, stochastic switching, and CRS behavior are not compatible with the memistor model and thus support our conclusions.

**Experimental Section**

Figure 2a shows the experimental circuit used to implement the ideal memistor test. A source measure unit (Keysight B2911A) was used to generate the test voltage signal \( V(t) \) and control signal \( V_c \). The unit was controlled by a code written in C Sharp. To initialize and measure the device state, the relay (part number HI05-1A 66, Standex-Meder Electronics) was closed, thus connecting the tested device to the source measure unit directly. To run the test, the relay was opened and the test voltage signal (such as the triangular pulse in Figure 2b) applied across the capacitor (non-polarized 1 or 10 \( \mu \)F capacitor) connected in series with the tested device. In this work, the test was applied to i) in-house fabricated Cu-SiO-2-based electrochemical metallization memory cells, and ii) commercially available ECMs by Knowlum Inc. (BS-AF-W and M+SDC Cr devices). Moreover, a precise model of TaO VCMs (another wide class of memory devices) was used to show that their characteristics are in striking disagreement with the memistor model.

The Cu-SiO-2 resistance-switching devices studied in this work were fabricated by sputtering deposition technique on the surface of a silicon wafer (substrate). A thin adhesion layer (5 nm Ti) was first formed on the surface of the substrate. 30 nm Ru was used as an inert bottom electrode common for all devices. A 30-nm-thick SiO-2 layer was deposited using a shadow mask with 10 \( \times \)10 mm square openings. The top Cu electrodes of 30 nm thickness were deposited on top of SiO-2 using another shadow mask with square and circular openings of various sizes. In this paper, data are presented for a device with a circular top electrode of \( r = 710 \) \( \mu \)m. A 5 nm CoCrPt was used as a protective layer for the top electrodes (see inset of Figure 1a for a schematic of the structure of memory cells). In order to dope SiO-2 with Cu atoms, the devices were subjected to 580 °C, 1 h annealing in He environment. After that, the samples were slowly cooled down to the room temperature. The result is a typical resistance-switching memory cell with characteristics similar to many other experimental memory devices. The ideal memistor test was implemented on several randomly selected devices showing stable switching behavior.
The modeling results were obtained using an accurate model of TaO VCMs consisting of two equations

\[ I = G(x, V_M) \Delta V_M \]  
\[ \dot{x} = A \text{sinh} \left( \frac{V_M}{\sigma_{\text{off}}} \right) \exp \left( -\frac{x^2}{x_{\text{off}}^2} \right) \left[ \exp \left( \frac{1}{1 + \beta V_M} \right) H(-V_M) \right] + B \text{sinh} \left( \frac{V_M}{\sigma_{\text{on}}} \right) \exp \left( -\frac{x^2}{x_{\text{on}}^2} \right) \left[ \exp \left( \frac{1}{1 + \beta V_M} \right) H(V_M) \right] \]  

where Equation (1) is a generalized Ohms law, while Equation (2) describes the internal state dynamics. Here, the state variable \( x \) is the volume fraction of the oxygen-depleted channel with metallic transport, while the remaining fractional volume \( 1 - x \) is insulating (with nonlinear transport).\(^{[29]}\) According to Equation (2), the metallic channel either expands or shrinks depending on the bias polarity. In Equation (1), the memductance \( G(x, V_M) \equiv R_M(x) \) is

\[ G(x, V_M) = G_M x + a \exp \left( b \sqrt{V_M} \right) (1 - x) \]

where \( A, B, \sigma_{\text{off}}, \sigma_{\text{on}}, x_{\text{off}}, x_{\text{on}}, G_M, a, b, \) are constants, and \( H(\ldots) \) is the Heaviside step function. All simulations reported above were performed using the following set of parameter values\(^{[29]}\): \( A = 10^{-10} \text{ s}^{-1}, B = 10^{-4} \text{ s}^{-1}, \sigma_{\text{off}} = 0.013 \text{ V, } \sigma_{\text{on}} = 0.45 \text{ V, } \sigma_p = 4 \times 10^{-3} \text{ A V, } x_{\text{off}} = 0.4, x_{\text{on}} = 0.06, \beta = 500 \text{ A}^{-1} \text{ V}^{-1}, G_M = 0.025 \text{ S, } a = 7.2 \mu \text{ S, } b = 4.7 \text{ V}^{-1/2}. \)

Acknowledgements
The authors are thankful to Mr. H. Smith and Dr. T. M. Crawford for their help with sputtering deposition. This work was partially supported by a USC Provost grant.

Conflict of Interest
The authors declare no conflict of interest.

Keywords
memory materials, memristors, resistance switching memories

Received: January 3, 2020
Revised: March 25, 2020
Published online: June 17, 2020

[1] D. B. Strukov, G. S. Snider, D. R. Stewart, R. S. Williams, Nature 2008, 453, 80.
[2] F. Z. Wang, L. Li, L. Shi, H. Wu, L. O. Chua, J. Appl. Phys. 2019, 125, 054504.
[3] L. O. Chua, IEEE Trans. Circuit Theory 1971, 18, 507.
[4] L. Chua, Appl. Phys. A 2011, 102, 765.
[5] B. Mouttet, arXiv preprint arXiv:1201.2626, 2012.
[6] P. Meuffels, R. Soni, arXiv preprint arXiv:1207.7319, 2012.
[7] M. Di Ventra, Y. V. Pershin, Nanotechnology 2013, 24, 255201.
[8] S. Vongehr, X. Meng, Sci. Rep. 2015, 5, 11657.
[9] K. M. Sundqvist, D. K. Ferry, L. B. Kish, Fluct. Noise Lett. 2017, 16, 1771001.
[10] Y. V. Pershin, M. Di Ventra, Semicond. Sci. Technol. 2019, 34, 098001.
[11] It is interesting to note that the hysteresis loops of resistance-switching memories are typically twisted, not pinched.
[12] L. Chua, Semicond. Sci. Technol. 2014, 29, 104001.
[13] L. O. Chua, S. M. Kang, Proc. IEEE 1976, 64, 209.
[14] Y. V. Pershin, M. Di Ventra, J. Phys. D: Appl. Phys. 2018, 52, 01LT01.
[15] I. Valov, R. Waser, J. R. Jameson, M. N. Kozicki, Nanotechnology 2011, 22, 254003.
[16] Y. V. Pershin, M. Di Ventra, Adv. Phys. 2011, 60, 145.
[17] R. Waser, R. Dittmann, G. Staikov, K. Szot, Adv. Mater. 2009, 21, 2632.
[18] J. P. Strachan, A. C. Torrezan, F. Miao, M. D. Pickett, J. J. Yang, W. Yi, G. Medeiros-Ribeiro, R. S. Williams, IEEE Trans. Electron Devices 2013, 60, 2194.
[19] Self directed channel memristors, https://knowm.org/downloads/ Knowm_Memristors.pdf (accessed: March 2020).
[20] L. O. Chua, Semicond. Sci. Technol. 2019, 34, 098002.
[21] L. O. Chua, Proc. IEEE 2003, 91, 1830.
[22] J. Murdock, Scholarpedia 2006, 1, 1904, revision #91898.
[23] J. W. Bruce, P. J. Giblin, Curves and Singularities: A Geometrical Introduction to Singularity Theory, 2nd ed., Cambridge University Press, Cambridge 1992.
[24] S. Gaba, P. Knag, Z. Zhang, W. Lu, in 2014 IEEE International Symp. on Circuits and Systems (ISCAS), IEEE, Piscataway, NJ 2014, pp. 2592–2595.
[25] R. Naous, M. Al-Shedivat, K. N. Salama, IEEE Trans. Nanotechnol. 2016, 15, 15.
[26] E. Linn, R. Rosezin, C. Kügeler, R. Waser, Nat. Mater. 2010, 9, 403.
[27] E. Linn, A. Siemon, R. Waser, S. Menzel, IEEE Trans. Circuits Syst. I 2014, 61, 2402.
[28] C. Schindler, S. C. P. Thermadam, R. Waser, M. N. Kozicki, IEEE Trans. Electron Devices 2007, 54, 2762.
[29] A. Ascoli, V. Ntinas, R. Tetzlaff, G. C. Sirakoulis, Electron. Lett. 2017, 53, 1125.