Effect of variation in channel length and thickness of organic semiconductor in the bottom-gate configuration of OTFT

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Abstract-Advancing in the device and circuit performance a vast amount of study is going in the area of organic electronics. In the present work, we have patterned the features of the bottom-gate configuration of OTFT with the help of Technology Computer-Aided Design (TCAD) tools where ATLAS™ (Silvaco International) has been utilized as a 2D numerical device simulator to extract the electrical characteristics. To monitor the effect of variation in channel length and thickness of OTFT, we have altered the channel length (L) from 10um to 50um, which results in the reduction of the drive current from \(1.4 \times 10^{-10}\) A to \(2.7 \times 10^{-11}\) A (BGBC), and in contrary to that the performance of the device has been affected as the current ratio decrease from \(1.2 \times 10^{12}\) to \(1.4 \times 10^{3}\) (BGBC) with a thickness variation of organic semiconductor from 10nm to 50nm. Furthermore, the electrical characteristics as well as performance parameters like mobility, on/off current ratio, threshold voltage, etc., related to configured Bottom-Gate (top and bottom contacts) pentacene-based OTFT devices have been retrieved and compared.

Keyword- Organic thin film transistor, bottom-gate configurations, Organic semiconductor thickness, channel length variation, numerical simulation, electrical parameter.

1. Introduction

Organic electronics is emerging as an alternative to change conventional electronics' modernization due to unique features like flexibility, low cost, ease of processing, ultrathin, etc. The backbone of the organic electronics is the conducting organic material, which was firstly reported by Heeger, Diarmid, and skirakawa in 1977. For this novel invention, they were combinedly awarded the noble prize in 2000 [1]. After the influx of conducting organic material, organic devices came into the picture. The first organic field-effect transistor in 1986 was based on an organic macromolecule, polythiophene, used as the semiconductor (active layer) [2], which assisted in having better charge transport. Simultaneously, organic material mobility was observed to be less in contrast to the traditional semiconductor material. Research is going on to increase the mobility of organic field-effect transistor (OFET) devices by using different high performances of organic material and fabrication techniques to help these devices to be a part of plastic electronics, textiles electronics, and robotic skin [3-7]. All these implementations are only possible with the help of a transistor called an organic field-effect transistor. In recent times these pentacene organic field-effect transistors demonstrate in “functional logic circuitry”[8] and active-matrix liquid crystal display [9]. In the current scenario, the devices
related to organic electronics can compete against conventional electronics in the marketplace due to their novel features. The working principle of organic thin-film transistor (OTFT) is like a metal oxide semiconductor field-effect transistor (MOSFET). Still, the channel formation differs, and it works in the voltage-controlled current source when we apply a voltage between gate and source ($V_{gs}$), the accumulation process of the charge carrier starts at the interface of semiconductor and insulator, which help in the generation of current and voltage applied between drain and source ($V_{ds}$) help in the flow of current. OTFT is incorporated with the organic semiconductor layer, gate dielectric, and the electrodes, which include gate, drain, and source. These layers are arranged in different devices structure mainly; we determine the structure of OTFT by the position of the gate dielectric, which can be upward and downward. As a result, we termed as the top gate (TG) and bottom gate (BG) configuration and according to the source's location and drain contact regarding the organic semiconductor layer, which is also divided into top and bottom contact structure. This paper has discussed the OTFT with bottom gate configuration, where we have simulated the 2D structure and shown the comparative study between bottom gate top contact (BGTC) and bottom gate bottom contact (BGBC) structured OTFTs with high dielectric constant. Figure 1 shows the structure of the top and bottom contact bottom gate OTFT devices. The scope of application of these OTFTs is decided by various parameters, which mainly include mobility, threshold voltage, on/off current ratio and sub-threshold slope, etc. [10-12]; these parameters have been extracted using device simulator software ATLAS from Silvaco International [13]. Where the prime variations are being done in structural dimension, the material used in layers, the grain size of organic semiconductor thin film, and morphology of the semiconductor. Here also we have changed the structural dimension parameter like channel length [14] and thickness of the organic semiconductor, i.e., the polymer used [15], which affects the performance of the OTFT. Due to good organic material's conductivity and flexibility, it replicates analogous operations like other conventional electronics devices such as LED, TFT, FET, and many more.

![Figure 1. Bottom gate OTFT (a) Bottom gate top contact (b) Bottom gate bottom contact](image)

2. Device structure simulation and modeling setup

We have modeled the bottom gate configurations with top and bottom contact structure using an analytical model based simulator to realize the device physics. Examining the electrical characteristics by designing the top and bottom contact OTFTs, which is formed with the help of the Silvaco Atlas 2-D numerical device simulator. For comparison of top and bottom contact structure, an Aluminum gate electrode with thickness 0.02 μm is selected. HfO$_2$ gate dielectric with high dielectric constant 22.0 is used and deposited above gate electrode with thickness 5.7nm. The pentacene layer that is p-type organic semiconductor material is deposited over the oxide layer with a thickness of 30nm with a
doping concentration of $3 \times 10^{17}$, generation of the conducting channel took place. Since this is a simulated work but during the practical device fabrication, similar steps are involved as proposed by many researchers [16-23]. Deposition of the materials plays a central activity while determining the performance of different OTFTs. The generally used method for the deposition of thin-film of polymers on the substrate is a solution-processed spin-coating method [18, 19]. But the novel alternative approach for well-oriented, uniformly deposited polymer thin-film (OSC) is proposed as floating film transfer method (FTM) which has been widely adopted during the fabrication of PQT-12 polymer based practical OTFTs [20-23]. Further, for the metal contacts (Au) have been deposited over as deposited (source and drain) over active layer of OSC. In the present work the deposition of the source and the drain electrode is changed according to the structure with a thickness of 20 nm. Moreover, in table 1. the structure-based dimensional parameter with material and thickness is summarized [24,25]. The simulated device structure in TCAD Silvaco is shown in fig. 2.

![Figure 2. TCAD Silvaco Simulated Bottom gate configurations of (a) Top contact and (b) Bottom contact](image-url)
The procedure comprises mathematical models such as Poisson’s, Continuity, and transport equation that assist the TCAD tool in displaying the electrical parameter which is associated with the performance of the device.

2.1. Physical equation of devices:

Poisson’s Equation associates between electrostatic potential and local charge densities. Equation 1 and 2 expresses the mathematical relationship.

\[
\nabla \cdot (\varepsilon \nabla \psi) = -\rho \tag{1}
\]

\[
\nabla \cdot (\varepsilon \nabla \psi) = -q(p - n + N_d^+ - N_a^-) \tag{2}
\]

Where \( \psi \) and \( \varepsilon \) represent electrostatic potential, and local permittivity and \( \rho \) represents local space charge density. During the simulation, it always takes the intrinsic Fermi potential as a reference potential. The sum of fixed and mobile charges plays a significant role in the local space charge density. The sum includes the electron density (n), hole density (p), and ionized impurities such as \( N_d^+ \) represents ionized donor density, and \( N_a^- \) represents ionized acceptor density.

Continuity equation represents the dynamic of charge carrier arrangement with time. The equation for electron and holes as shown in equation 3 and 4:

\[
\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot J_n + G_n - R_n \tag{3}
\]

\[
\frac{\partial p}{\partial t} = \frac{1}{q} \nabla \cdot J_p + G_p - R_p \tag{4}
\]

Herein the above equations, the electronic charge magnitude has been represented by q, n and p are the electron and hole concentration, G and R are the corresponding generations and recombination rate. J is the current density. During the simulation, both Equations 3 and 4 take part, but we can turn off a particular equation that is not used for a specific model.

The transport equation, specify the device's physics for the electron and hole current densities, generation, and recombination rates. It uses a drift-diffusion charge transport model for the current density equation. Equation 5 and 6 describe the drift-diffusion model as follows:

\[
J_n = q \mu_n E_n + q D_n \nabla n \tag{5}
\]

\[
J_p = q \mu_p E_p + q D_p \nabla p \tag{6}
\]

Where \( n \) and \( p \) are the electron and hole density, \( \mu \) is the carrier mobility, \( E \) is the local electric field, \( D \) is the diffusion coefficient. Equation 7 and 8 describe the local electric field as follows:

\[
E_n = -\nabla (\psi + \frac{k T_L}{q} \ln n_{ie}) \tag{7}
\]

\[
E_p = -\nabla (\psi + \frac{k T_L}{q} \ln n_{ie}) \tag{8}
\]

Where \( n_{ie} \) and \( T_L \) represent the local effective intrinsic concentration and lattice temperature, respectively.

The Poole-Frenkel mobility model has been used to investigate the device's static and dynamic operation with finite element-based simulation. It can be expressed as-

\[
\mu(E) = \mu_0 \exp \left[ -\frac{\Delta}{k T} + \left( \frac{\beta}{k T} - \gamma \right) \sqrt{E} \right] \tag{9}
\]

Here, \( \mu(E) \) shows field-dependent mobility, \( \mu_0 \) is zero-field mobility which is depicted when the drain voltage is zero, \( E \) is the electric field and \( \Delta, \beta, \gamma \) is the activation energy, hole Poole-Frenkel constant, fitting parameter Table 2[24]. Shows the input parameter of the bottom-gate OTFT used during the simulation.
2.2. Density of defect states model

The total density of defect states (DOS), \( g(E) \), comprises four bands, two tail and two deep state function such as an acceptor-like \( (g_{TA}(E)) \) and a donor-like \( (g_{TD}(E)) \) exponential band tail function, an acceptor-like \( (g_{GA}(E)) \) and a donor-like \( (g_{GD}(E)) \) Gaussian deep state function. The equation 10 specified as total DOS:

\[
g(E) = g_{TA}(E) + g_{TD}(E) + g_{GA}(E) + g_{GD}(E)
\]

Where, \( E \) specify the state energy, subscripts \( (T, G, A, D) \) is tail, Gaussian (deep level), acceptor, and donor states. The equation 11 to 14 describing the term used in equation 10.

\[
g_{TA}(E) = N_{TA} \exp\left[\frac{E-E_C}{W_{TA}}\right]
\]

\[
g_{TD}(E) = N_{TD} \exp\left[\frac{E-V}{W_{TD}}\right]
\]

\[
g_{GA}(E) = N_{GA} \exp\left[-\frac{E-G_A}{W_{GA}}\right]^2
\]

\[
g_{GD}(E) = N_{GD} \exp\left[-\frac{E-G_D}{W_{GD}}\right]^2
\]

In exponential tails, DOS is specified by conduction and valence band intercept densities \( (N_{TA} \text{ and } N_{TD}) \) and its characteristic decay energy \( (W_{TA} \text{ and } W_{TD}) \). In Gaussian distributions, DOS is specified by the total state density \( (N_{GA} \text{ and } N_{GD}) \), and its characteristic decay energy \( (W_{GA} \text{ and } W_{GD}) \), and peak energy distribution \( (E_{GA} \text{ and } E_{GD}) \).

### Table 1. Device dimension of bottom-gate configuration top and bottom contact with the material

| Device Dimension | Material | Value |
|------------------|----------|-------|
| The thickness of OSC (tOSC) | Pentacene | 30nm |
| The thickness of dielectric (tOX) | HfO2 | 5.7nm |
| The thickness of the gate electrode (tG) | Aluminum | 20nm |
| Thickness of S/D contact (tS/D) | Gold | 20nm |
| Channel length | - | 10um |
| Channel width | - | 220um |

### Table 2. Simulation input parameter of OTFT

| Parameters | Values |
|------------|--------|
| The work function of source & drain (Au) | 5.1 |
| The work function of Gate (Al) | 4.28 |
| Doping Concentration | \(3 \times 10^{12} \text{ cm}^{-2}\) |
| The dielectric constant for HfO2 | 22 |
| Permittivity for pentacene | 4.0 |
| The activation energy for zero electric fields for holes | \(1.792 \times 10^{-2} \text{ eV}\) |
| Hole Poole-Frenkel factor | \(7.758 \times 10^{-5} \text{ eV} (\text{cm/V})^{1/2}\) |
| Effective density of state in the conduction band (Nc) | \(1.0 \times 10^{21} \text{ cm}^{-3}\) |
| Effective density of state in the valance band (NV) | \(1.0 \times 10^{21} \text{ cm}^{-3}\) |

3. Results and discussions

The electrical characteristics of bottom-gate configurations of top and bottom contact, electrical parameters like threshold voltage, subthreshold voltage, on/off ratio, transconductance, and mobility are evaluated and compared with the help of numerical simulation.
3.1. Comparison and performance of the bottom-gate top and bottom contact OTFT

The electrical characteristics of the top and bottom gate configuration are being compared. After the simulation by using the above dimensional parameter, we show the outcomes in Table 3. We analyzed that the on/off current ratio and mobility is high of bottom contact than top contact. It is observed that bottom gate Bottom contact shows the superior result when compared with top contact at gate voltage greater than 7.5 V with drain voltage -1V because the traveling path of charge carrier between source and drain is unlike [26] shown in figure 3 transfer characteristics curve. The dielectric material modification leads an essential part in determining the electrical parameter. Here, increase in the capacitance, C by a factor of k (dielectric constant) as shown in equation 15

\[ C = \frac{\varepsilon_0 k}{t_{ox}} \]  

(15)

Where t_{ox} is the dielectric layer thickness. The increased capacitance leads to a shift in charge distribution in dielectric material because of polarization induced by an external electric field. The high-k dielectric material is helpful for the low threshold voltage. Similarly, high on-current (with high current ratio) and a more downward subthreshold slope are observed [10]. Table 4 shows the comparison of the electrical parameter according to the reported literature. Here, low mobility results from surface roughness directing to the morphological disorders in OSC, which reduces the carrier's mobility.

| Parameters               | BGTC   | BGBC   |
|--------------------------|--------|--------|
| Threshold voltage V_T (V)| -0.601 | -0.666 |
| Sub-Threshold Slope SS (V/Decade) | 0.291  | 0.284  |
| Current On-Off Ratio I_{ON}/I_{OFF} | 3.7×10^4 | 4.1×10^4 |
| Transconductance g_m (μS) | 4.34×10^{-6} | 4.96×10^{-6} |
| Mobility μ (cm²/VS)     | 0.0578 | 0.0661 |

Figure 3. Bottom gate top and bottom contact transfer characteristic curve at drain voltage -1V
Table 4. Comparison of the electrical parameter of top and bottom contact bottom gate OTFT with the different dielectric material.

| Material of layer | Structure | $\mu$ (cm$^2$/Vs) | $I_{ON/OFF}$ | $V_T$(V) | SS (V/dec.) | Supply voltage $V_{ds}$(V) $V_{gs}$(V) | Ref. |
|------------------|-----------|------------------|-------------|--------|----------------|-----------------------------|-----|
| OSC-Pentacene, S/D-Gold, G- Aluminum, D-Aluminum oxide (Al$_2$O$_3$) | BGTC | NR | $6.9 \times 10^4$ | -0.5 | 0.34 | -1 | 0 to -20 | 24 |
| OSC-Pentacene, S/D-Gold, G- Aluminum, D-Aluminum oxide (Al$_2$O$_3$) | BGBC | 0.129 | $9.5 \times 10^4$ | -1.2 | 0.32 | -1 | 0 to -30 | 26 |
| OSC-Pentacene, S/D-Gold, G- n$^+$Si, D-Silicon dioxide(SiO$_2$) | BGTC | 0.085 | NR | -3.2 | NR | -25 | 0 to -20 | 27 |
| OSC-Pentacene, S/D-Gold, G- Aluminum, D- Hafnium oxide (HfO$_2$) | BGBC | 0.057 | $3.7 \times 10^4$ | -0.60 | 0.29 | -1 | 0 to -30 | Present Work |

Where G and D represent the gate and dielectric layer, respectively, S/D is source/drain. $V_{ds}$ is the drain to source voltage, and $V_{gs}$ is the gate to source voltage. $V_T$ and SS are the threshold voltage and subthreshold slope, $\mu$ is the mobility, and NR is not reported.

3.2. Effect of variation of channel length and organic semiconductor thickness on bottom gate top and bottom contact OTFT.

This segment represents the dimensional parameters influences, such as channel length from 10μm to 50μm and organic semiconductor thickness from 10nm to 50nm with a step size of 10. It shows the variation (in both cases) in the operation of bottom-gate OTFT significantly.

We show by increasing the channel length, the drive current reduces in Figures 4. (a) and (b). Such variation may be because channel length is inversely proportional to drive current [28]. We see mobility increment in BGBC while reducing the channel length. And other parameters such as the threshold voltage reduces, we see a slight variation in the current ratio($I_{ON/OFF}$) and also affect the other electrical parameter of devices, which is summarized in table 5.

Figure 4. Drain current variation due to variation in the channel length variation from 10 μm to 50μm in (a) BGTC (b) BGBC
Table 5. Electrical parameter of bottom-gate top and bottom contact OTFT during channel length variation

| Channel length | Device type | Threshold voltage $V_T$ (V) | $I_{ON}$ (A) | $I_{OFF}$ (A) | $I_{ON/OFF}$ | Sub-threshold slope $SS$ (V/decade) | Mobility $\mu$ (cm²/Vs) | Transconductances $g_m$ (µS) |
|----------------|-------------|-----------------------------|-------------|---------------|-------------|-------------------------------------|----------------------|--------------------------|
| 10μm BGTC      | -0.601      | -1.309×10⁻¹⁰              | -3.426×10⁻¹⁸| 3.78×10⁻⁴    | 0.291       | 0.0578                             | 4.34×10⁶            |
|                | BGBC        | -0.666                     | -1.437×10⁻¹⁰| -3.430×10⁻¹⁸| 4.16×10⁻⁴  | 0.284                              | 0.0661              | 4.96×10⁶               |
| 20μm BGTC      | -0.615      | -6.626×10⁻¹¹              | -1.691×10⁻¹⁸| 3.91×10⁻⁴    | 0.297       | 0.0597                             | 2.24×10⁶            |
|                | BGBC        | -0.679                     | -6.945×10⁻¹¹| -1.687×10⁻¹⁸| 4.11×10⁻⁴  | 0.287                              | 0.0639              | 2.40×10⁶               |
| 30μm BGTC      | -0.623      | -4.427×10⁻¹¹              | -1.119×10⁻¹⁸| 3.95×10⁻⁴    | 0.303       | 0.0603                             | 1.51×10⁶            |
|                | BGBC        | -0.685                     | -4.568×10⁻¹¹| -1.116×10⁻¹⁸| 4.09×10⁻⁴  | 0.287                              | 0.0631              | 1.58×10⁶               |
| 40μm BGTC      | -0.628      | -3.320×10⁻¹¹              | -8.359×10⁻¹⁸| 3.97×10⁻⁴    | 0.310       | 0.0602                             | 1.13×10⁶            |
|                | BGBC        | -0.689                     | -3.399×10⁻¹¹| -8.334×10⁻¹⁸| 4.07×10⁻⁴  | 0.287                              | 0.0622              | 1.17×10⁶               |
| 50μm BGTC      | -0.632      | -2.654×10⁻¹¹              | -6.671×10⁻¹⁸| 3.97×10⁻⁴    | 0.317       | 0.0608                             | 9.13×10⁵            |
|                | BGBC        | -0.691                     | -2.704×10⁻¹¹| -6.648×10⁻¹⁸| 4.06×10⁻⁴  | 0.287                              | 0.0623              | 9.38×10⁵               |

Increment in organic semiconductor thickness, the behavior of devices affected by the bulk traps and charge localization which is found in the interface of OSC-dielectric because of which the devices performance changes. The ON current of the device is affected by means of the variation in thickness of the semiconductor. However, an increase in OFF current with an increase in semiconductor (OSC) thickness is due to the subsequent rise in the bulk current. The switching activity drop-off with the larger magnitude of OFF current, which increases the power consumption and charge leakage in the device. Figure 5 shows transfer characteristics of both structures at $V_{ds}=-1$. Subsequently, decreasing the OSC thickness in BGTC, an increase in drain current (slight variation in case of BGBC based device) has been observed. From the current density profile, a very nominal variation in the drain current has been analyzed. The threshold voltage is reduced because of an increment in the free charge carrier with an increase in active layer thickness. Mobility in BGTC increases on increasing the thickness of the OSC layer. This is due to the decrease in the average value of the charge carriers [29,30]. From table 6, the same can be observed clearly along with other electrical parameters.

![Figure 5](image-url)
Table 6. Electrical parameter of bottom-gate top and bottom contact OTFT during organic semiconductor thickness variation

| OSC Thickness | Device type | Threshold voltage $V_T$ (V) | $I_{ON}(A)$ | $I_{OFF}(A)$ | Sub-threshold Slope SS (V/decade) | Mobility (cm²/Vs) | Transconductances $g_m$ (μS) |
|---------------|-------------|-----------------------------|-------------|--------------|------------------------------------|------------------|-----------------------------|
| 10nm          | BGTC        | -0.663                      | -1.401×10⁻⁷ | 2.6×10⁻⁹    | 0.065                               | 0.0640           | 4.82×10⁶                   |
|               | BGBC        | -0.695                      | -1.431×10⁻⁷ | 1.2×10⁻¹²   | 0.036                               | 0.0659           | 4.96×10⁶                   |
| 20nm          | BGTC        | -0.626                      | -1.350×10⁻⁷ | 1.6×10⁻⁹    | 0.036                               | 0.0606           | 4.56×10⁶                   |
|               | BGBC        | -0.681                      | -1.436×10⁻⁷ | 2.6×10⁻⁹    | 0.060                               | 0.0662           | 4.98×10⁶                   |
| 30nm          | BGTC        | -0.601                      | -1.309×10⁻⁷ | 3.7×10⁻⁹    | 0.291                               | 0.0578           | 4.34×10⁶                   |
|               | BGBC        | -0.666                      | -1.437×10⁻⁷ | 4.1×10⁻⁹    | 0.284                               | 0.0659           | 4.96×10⁶                   |
| 40nm          | BGTC        | -0.579                      | -1.271×10⁻⁷ | 3.9×10⁻⁹    | 0.636                               | 0.0554           | 4.17×10⁶                   |
|               | BGBC        | -0.652                      | -1.434×10⁻⁷ | 4.3×10⁻⁹    | 0.633                               | 0.0659           | 4.96×10⁶                   |
| 50nm          | BGTC        | -0.560                      | -1.244×10⁻⁷ | 1.2×10⁻⁹    | 0.765                               | 0.0535           | 4.03×10⁶                   |
|               | BGBC        | -0.638                      | -1.454×10⁻⁷ | 1.4×10⁻⁹    | 0.761                               | 0.0659           | 4.96×10⁶                   |

4. Conclusion

The performances of the bottom-gate configured top, as well as bottom contact OTFTs based on pentacene with high dielectric constant material, have been analyzed and compared. It is observed that BGTC shows a much better result as compared to BGTC. Besides this, the effect of channel length and organic semiconductor thickness is examined. We observed lower channel length produces a high drive current, and decreasing organic semiconductor thickness reduces the leakage current and leads to an increment in the current ratio. Such results are much desirous in displays and memory circuits.

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References

[1] Shirakawa H, Louis E J, Macdiarmid A G, Chiang C K and Heeger A J 1977 J. Chem. Soc. Chem. Commun. 39, pp. 1098-1101.
[2] Tsumura A, Koezuka H and Ando T 1986 Appl. Phys. Lett. 49, pp. 1210-12
[3] Klauk H, Gundlach D J and Jackson T N 1999 IEEE Electron Device Lett. 20, pp. 289-291.
[4] Halik M, Klauk H, Zschieschang U, Schmid G, Radlik W, Ponomarenko S, kirchmeyer S and Weber W 2003 Journal of Applied Physics 93, pp. 2977-81.
[5] Crone B K, Dodabalapur A, Sarapreshkar R, Filas R W, Lin Y-Y, Bao Z, O’Neil J H, Li W and Katz H E 2001 J. Appl. Phys. 89, pp. 5125-32.
[6] Lee J B and Subramanian V 2003 IEEE International Electron Devices Meeting (IEDM’03) pp. 199-202.
[7] Someya T and Sakurai T 2003 IEEE International Electron Devices Meeting pp. 203-6.
[8] Kane M G, Campi J, Hammond M S, Cuomo F P, Greening B, Sheraw C D, Nichols J A, Gundlach D J, Huang J R, Kuo C C, Jia L, Klauk H and Jackson T N 2000 IEEE Electron Device Letter 21, pp. 534-6.
[9] Sun H, Yin Y, Wang Q, Jun Q, Wang Y, Tsukagoshi K, Wang X, Hu Z, Pan L, Zheng Y, Shi Y and Li Y 2015 Appl. Phys. Lett. 88, pp. 053304-1-4.
[10] Kumar B, Kaushik B K and Negi Y S 2014 Polym. Rev. 54, pp. 33-111.
[11] Es-Saghiri A, Boufounas E-M, El Amrani A and Lucas B 2018 4th International Conference on Optimization and Applications (ICOA).
[12] Sharma S and Varma T 2018 *Materials Research Express* 6, pp. 1-11.
[13] ATLAS User’s Manual from SILVACO International.
[14] Mittal P, Kumar B, Negi Y S, Kaushik B K and Singh R K 2012 *Microelectronics Journal* 43, pp. 985-994.
[15] Resendiz L, Estrada M, Cerdeira A, Iniguez B and Deen M J 2010 *Org. Electron* 11, pp. 1920-27.
[16] Singh S, Tiwari P K, Kumar H, Kumar Y, Rawat G, Kumar S, Singh K, Goel E, Jit S, Park S 2017 *NANO*, pp. 1750137-1-8
[17] Singh MK, Pandey R K, Prakash R 2017 *Organic Electronics* 2017 50, pp. 359-66.
[18] Singh M K, Kumar A, Prakash R 2017 *Materials Science and Engineering: B* 217, pp. 12-7.
[19] Singh M K, Kumar A, Prakash R 2018 *Organic Electronics* 54 pp. 209-15.
[20] Kumar C, Rawat G, Kumar H, Kumar Y, Prakash R, Jit S 2018 *IEEE Transactions on Nanotechnology* 17, pp. 1111-7
[21] Kumar C, Rawat G, Kumar H, Kumar Y, Prakash R, Jit S 2017 12th *IEEE Nanotechnology Material and Devices Conferences* pp. 37-38
[22] Kumar C, Rawat G, Kumar H, Kumar Y, Kumar A, Prakash R, Jit S 2018 *IEEE Sensors Journal* 18, pp. 6085-91
[23] Kumar C, Rawat G, Kumar H, Kumar Y, Prakash R, Jit S 2017 *Organic electronics* 48, pp. 53-68
[24] Singh A and Singh M K 2020 *Asian Journal of Convergence in Technology* 6, pp. 1-4.
[25] Singh A and Singh M K 2020 *IEEE International Conference for Innovation in Technology* pp. 1-5.
[26] Kumari P and Dwivedi A D D 2019 *Global Journal of Research In Engineering* 19, pp. 6-12.
[27] Gupta D, Katiyar M, Gupta D 2009 *Organic Electronic* 10, pp. 775-784
[28] Singh A and Singh M K 2020 *International Conference on Advances in Computing, Communication & Materials (ICACCM)* pp. 301-5.
[29] Kumar B, Kaushik B K, Negi Y S 2014 *IET Circuits, Devices & Systems* 8, pp. 131-140
[30] Singh A and Singh M K 2020 *Journal of Physics: Conference Series* 1706, pp. 1-12