Reducing Redundancy in Data Organization and Arithmetic Calculation for Stencil Computations

Kun Li
Institute of Computing Technology, Chinese Academy of Sciences
University of Chinese Academy of Sciences
Beijing, China
likungw@gmail.com

Liang Yuan
Institute of Computing Technology, Chinese Academy of Sciences
Beijing, China
yuanliang@ict.ac.cn

Yunquan Zhang
Institute of Computing Technology, Chinese Academy of Sciences
Beijing, China
zyq@ict.ac.cn

Yue Yue
Institute of Computing Technology, Chinese Academy of Sciences
University of Chinese Academy of Sciences
Beijing, China
yyue1998@gmail.com

Hang Cao
Institute of Computing Technology, Chinese Academy of Sciences
University of Chinese Academy of Sciences
Beijing, China
caohang@ict.ac.cn

Pengqi Lu
Institute of Computing Technology, Chinese Academy of Sciences
University of Chinese Academy of Sciences
Beijing, China
lupengqi18s@ict.ac.cn

Abstract
Stencil computation is one of the most important kernels in various scientific and engineering applications. A variety of work has focused on vectorization techniques, aiming at exploiting the in-core data parallelism. Briefly, they either incur data alignment conflicts or hurt the data locality when integrated with tiling. In this paper, a novel transpose layout is devised to preserve the data locality for tiling in the data space and reduce the data reorganization overhead for vectorization simultaneously. We then propose an approach of temporal computation folding designed to further reduce the redundancy of arithmetic calculations by exploiting the register reuse, alleviating the increased register pressure, and deducing generalization with a linear regression model. Experimental results on the AVX-2 and AVX-512 CPUs show that our approach obtains a competitive performance.

Keywords Stencil, Vectorization, Register reuse, Data locality

1 Introduction
Stencil is one of the most important kernels widely used across a set of scientific and engineering applications. It is extensively involved in various domains from physical simulations to machine learning [8, 26, 36]. Stencil is also included as one of the seven computational motifs presented in the Berkeley View [3, 4, 51] and arises as a principal class of floating-point kernels in high-performance computing.

A stencil contains a pre-defined pattern that updates each point in a d-dimensional spatial grid iteratively along the time dimension. The value of one point at time t is a weighted sum of itself and its neighboring points at the previous time [11, 41]. The naive implementation for a d-dimensional stencil contains d + 1 loops where the time dimension is traversed in the outermost loop and all grid points are updated in inner loops. Since stencil is characterized by this regular computational structure, it is inherently a bandwidth-bound kernel with a low arithmetic intensity and poor data reuse [24, 51].

Performance optimizations of stencils has been exhaustively investigated in the literature. Traditional approaches have mainly focused on either vectorization or tiling schemes, aiming at improving the in-core data parallelism and data locality in cache respectively. These two approaches are often regarded as two orthogonal methods working at different levels. Vectorization seeks to utilize the SIMD facilities in CPU to perform multiple data processing in parallel, while
Prior work on vectorization of stencil computations primarily falls into two categories. The first one is based on the associativity of the weighted sums of neighboring points. Specifically, the execution order of one stencil computation can be rearranged to exploit common subexpressions or data reuse at register or cache level [6, 12, 33, 34, 54]. Consequently, the number of load/store operations can be reduced and the bandwidth usage is alleviated in optimized execution order. The second one attempts to deal with the data alignment conflict [17, 18], which is the main performance-limiting factor. The data alignment conflict is a problem caused by vectorization, where the neighbors for a grid point appears in the same vector registers but at different positions. One milestone approach is DLT method (Dimension-Lifting Transpose) [17], and it performs a global matrix transpose to address the data alignment conflict.

As one of the crucial techniques to exploit the parallelization and data locality for stencils, tiling, also known as blocking, has been widely studied for decades. Since the size of the working sets is generally larger than the cache capacity on a processor [27], the spatial tiling algorithms are proposed to explore the data reuse by changing the traversal pattern of grid points in one time step. However, such tiling techniques are restricted to the size of the neighbor pattern [24, 50]. Temporal tiling techniques have been developed to allow more in-cache data reuse across the time dimension [51].

The aforementioned two approaches of stencil computation optimizations often have no influence on the implementation of each other. However, the data organization overhead for vectorization may degrade the data locality. Moreover, most of the prior work only focuses on temporal tiling on the cache level. This only optimizes the data transfer volume between cache and memory, and the high bandwidth demands of CPU-cache communication is still unaddressed or even worse with vectorization. Thus, redundant calculation is performed on the same grid point iteratively due to massive CPU-cache transfers along the time dimension.

In this paper, we first design a novel transpose layout to overcome the input data alignment conflicts of vectorization and preserve the data locality for tiling simultaneously. The new layout is formed with an improved in-CPU matrix transpose scheme, which achieves the lower bounds both on the total number of data organization operations and the whole latency. Compared with conventional methods, the corresponding computation scheme for the new layout requires less data organization operations, whose cost can be further overlapped by arithmetic calculations.

Based on the proposed data layout, a temporal computation folding approach is devised to reduce the redundancy of arithmetic calculations. We perform a deep analysis of the expansion for multiple time steps, fold the redundant operations on the same point, and reassign a new weight for it to achieve a multi-step update directly. An improved in-CPU flops/byte ratio is obtained by reusing registers, and the calculation of intermediate time steps are skipped over to alleviate the increased register pressure. Furthermore, we utilize a shifts reusing technique to decrease the redundant computation within the innermost loops, and integrate the proposed approach with a tiling framework to preserve the data locality. Finally, the temporal computation folding approach is generalized for arbitrary stencil pattern by using a linear regression model.

The proposed scheme is evaluated with AVX-2 and AVX-512 instructions for 1D, 2D, and 3D stencils. The results show that our approach is obviously competitive with the existing highly-optimized work [17, 18, 51].

This paper makes the following contributions:

- We propose an efficient transpose layout and corresponding vectorization scheme for stencil computation. The layout transformation utilizes an improved matrix transpose of the lowest latency.
- Based upon the new proposed transpose layout, we design a temporal computation folding approach optimized by shifts reusing and tessellate tiling. It aims to reduce the redundancy of arithmetic calculation in time iteration space.
- We generalize our approach on various benchmarks, and demonstrate that it could achieve superior performance compared to several highly-optimized work [17, 18, 51] on multi-core processors.

The paper is organized as follows. Section 2 elaborates on the addressed data organization problem and formally describes the proposed vectorization scheme. The redundancy elimination of arithmetic calculation in time iteration space and its implementation are discussed in Section 3. Section 4 discusses the experimental results. In Section 5, we present the related work and Section 6 concludes the paper.

2 Spatial Data Organization

In this section, we first discuss the drawbacks of existing methods. Then we present a new transpose layout and its corresponding vectorized computation process. Next, we present an improved transpose implementation in our work.

2.1 Motivation

DLT is a promising method that extremely reduces the data reorganization operations. It performs a global matrix transpose to reconstruct the whole data layout in memory [17]. However, the elements in one vector are distant, thus there is no data reuse among them. Furthermore, DLT suffers from the overhead of explicit transpose operations executed before and after the stencil computation. For high-dimensional stencils and low-dimensional in other applications like image processing, the time size is small that makes the global
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matrix should be equal to \( v_l \), substituted by a two-dimensional matrix view. To perform a matrix transpose to a small sub-sequence of contiguous elements, we apply Locally Transpose to preserve the data locality and re-useability of data in CPU and the reuse ability of data in cache. Our scheme avoids data reloads compared with the multiple load operations per vector set. There are several considerations for devising this vectorization scheme. First, to avoid an additional array that is needed to store the transposed data as in DLT format, it’s desirable to complete the matrix transpose in CPU. The second reason is that transposing a matrix of size \( ol \times ol \) is cheaper to implement on modern CPU products. We will present a highly efficient algorithm for matrix transposition of size \( ol \times ol \) later. Moreover, the proposed vectorization scheme avoids data reloads compared with the multiple load method and frequent inter-vector permutations compared with the data reorganization method. The transpose layout could also be applied to higher-order and multidimensional stencils in the same manner.

### 2.3 Implementation

Unlike previous work [17] that performs a global dimension-lifted transformation, we only need a transpose on-the-fly for each register set twice throughout the whole process. Figure 3 illustrates the improved version by single-cycle non-parameter Unpack instructions. In the first stage, pairs of two vectors with distance 2, e.g., \((A, B, C, D)\) and \((I, J, K, L)\), exchange data using the Permute2f128 instruction. In the second stage, the pairs of two adjacent vectors, e.g., \((A, B, I, J)\) and \((E, F, M, N)\), swap elements by the Unpackhi or Unpacklo instructions.

**Vectors Computation**

The stencil computation of the vector set is straightforward as shown in Figure 2. The update of one vector set of the 3-point stencil requires two assembled vectors. One is the left dependent vector of its first vector and the other is the right dependent vector of its last vector. Figure 2 describes the data reorganization of these two vectors. The first vector is \((A, E, I, M)\) and its left dependent vector is \((Z, D, H, L)\) which is stored in two distant vectors in the transpose layout, \( (\ast, \ast, \ast, Z) \) and \((D, H, L, \ast)\). These two vectors are combined by a blend instruction followed by a permute operation to shift the components to the right circularly.

We then achieve an efficient vectorization scheme by performing lower-overhead matrix transpose and two data operations per vector set. There are several considerations for devising this vectorization scheme. First, to avoid an additional array that is needed to store the transposed data as in DLT format, it’s desirable to complete the matrix transpose in CPU. The second reason is that transposing a matrix of size \( ol \times ol \) is cheaper to implement on modern CPU products. We will present a highly efficient algorithm for matrix transposition of size \( ol \times ol \) later. Moreover, the proposed vectorization scheme avoids data reloads compared with the multiple load method and frequent inter-vector permutations compared with the data reorganization method. The transpose layout could also be applied to higher-order and multidimensional stencils in the same manner.

### 2.2 The Transpose Layout

**Locally Transpose**

To preserve the data locality and reduce the number of data organization operations, we apply a matrix transpose to a small sub-sequence of contiguous elements. Specifically, like the dimension-lifting approach in DLT, the one-dimensional view to the sub-sequence is substituted by a two-dimensional matrix view. To perform vectorization after a matrix transpose, the column size of the matrix should be equal to \( ol \), where \( ol \) is the vector length in vector elements. Figure 1 illustrates the transpose layout for a one-dimensional stencil with \( ol = 4 \). The matrix transposes of every sub-sequence of \( ol \times ol \) length is only performed twice before and after the stencil computation respectively. In the rest of the paper, we also refer to the \( ol \) vectors as a vector set. Note that in the implementation a vector set is always aligned to a 32-Byte boundary.

**Figure 1.** Register Transpose Layout for SIMD vector length of 4.

**Figure 2.** Illustration of stencil computation for transpose layout.

**Figure 3.** Transpose for double type using AVX-2 instructions.
instruction. In modern CPU architectures, these 8 instructions on 4 vectors can be launched continuously in 8 cycles, which are even less than the sum cost of them (4 cycles for a(n) add/multiply-add instruction). Similarly, the transpose by using AVX-512 instructions contains three stages where the last stage consists of in-line instructions.

3 Temporal Computation Folding

3.1 Overview of Approach

In general, all grid points are only updated once before the round starts for the next time step in stencil computation. Although most of the existing work utilizes blocking technique [5, 50, 51] to decrease the data transfers between main memory and cache, there is no in-register data reuse between $m$ successive time loops, where $m$ is called the unrolling factor. On the contrary, the straightforward implementation of reusing registers along the time dimension produces massive intermediate results at the time step $t$ to $t + m$, which exacerbates excessive register spilling.

The existing work and straightforward implementation represent opposite extremes of reusing register in time iteration space. Our approach is to seek a balance that the redundancy of arithmetic calculation is eliminated along the time dimension, and register pressure is alleviated simultaneously. To facilitate the process of reducing redundant calculation in time iteration space, we propose a computation folding approach to update the grid points for $m$ time steps directly in registers. The computation folding approach is elaborated thoroughly based upon a profitability analysis, and it is optimized with shifts reusing and tessellate tiling to obtain further performance gains. Additionally, we also describe an inductive generalization that promotes our computation folding approach on a wide variety of stencil kernels.

3.2 Scalar Profitability Analysis

Figure 4 shows a scalar arithmetic expression for a representative 9-point box stencil with unrolling factor $m = 2$ on the center grid point. A collect $C(E)$ in Equation 1 is defined to describe the number of instructions (add, multiply, multiply-add, etc.) used for $m$-step updates in the expression $E$.

$$C(E) = \bigcup_s \{(g, w_g) | (g, w_g) \in C(E_s)\}$$  \hspace{1cm} (1)

For the naive expression in Figure 4(a), the center point with neighboring eight grid points are all updated to the state $t + 1$ first, and then these updates are swept from registers to memory. When the next iteration for $t + 2$ begins, these grid points of $t + 1$ are reloaded again. To obtain a $2$-step updates on the center point, the computing instructions of ten subexpressions are all counted into the collect $C(E)$. In each subexpression $E_s$, a pre-defined weight $w_g$ is assigned on each grid point and then a 9-way addition result is obtained. Since nine distinct point references are engaged for each subexpression, we obtain $|C(E)| = 10 \times |C(E_s)| = 90$ for the expression $E$. It is worth noting that redundant arithmetic operations are performed iteratively on the same point in different subexpressions, and store/reload operations incur a costly interrupt during the computation process.

For the optimized expression in Figure 4(b), weights are all reassigned based on the $m$-step expansion. A new arithmetic expression $\mathbb{E}_\lambda$ is determined by the folding matrix comprised of new weights $\lambda$. The five associative grid points of the same column are folded with $\lambda$ first, and then a horizontal folding is performed to gather the obtained five folded values. Thus, the new collect in Equation 2 is 25, which is obtained from the computation folding on this point set with each grid point folded by $\lambda_g$.

$$C(\mathbb{E}_\lambda) = \{(g, \lambda_g) | \text{grid } g \text{ used in } \mathbb{E}_\lambda \text{ weighted with } \lambda_g\}$$  \hspace{1cm} (2)

The profitable index is evaluated in Equation 3, and a profitable folding means the fraction of the cardinalities on two sets at least exceeds a threshold $\theta \geq 1$. In this case, it gives a net profitable index of $P(E, \mathbb{E}_\lambda) = 90/25 = 3.6$ from Equation 3. Moreover, the interrupt cost of store/reload operations is also cut entirely in $\mathbb{E}_\lambda$.

$$P(E, \mathbb{E}_\lambda) = \frac{|C(E)|}{|C(\mathbb{E}_\lambda)|} \geq \theta$$  \hspace{1cm} (3)

3.3 Vectorized Multi-step Computation

In this subsection, we take a 2-step 2D9P box stencil [50, 51] as an example to illustrate the details on our computation folding approach in Figure 5, which is a vectorized process of the optimized arithmetic expression discussed in Section 3.2.

Layout Preparation Figure 5 depicts the codes and layout preparation for the box stencils. Based on the previous data organization in Section 2, the basic granularity of computation is also constructed as a $4 \times 4$ square of grid points denoted as $s_p$. They are loaded from cache to four registers as $v_0$ to $v_3$ respectively at time step $t$. The transpose layout proposed in Section 2 is utilized to manipulate the registers, and it can be adapted on multidimensional stencils. For example, 1D stencils with length of $4N$ grid points are viewed as a $4 \times N$ 2D grid points, and 3D stencils with volume of $N_x \times N_y \times N_z$ are manipulated as a $N_x$-layer $2D$ $N_y \times N_z$ slice.

Vertical Folding Vertical Folding is performed first to collect neighbor points in the same column. A new square of grid points derived from $s_p$ with vertical folding is called as a counterpart. Typically a $m$-step update contains $m + 1$ counterparts at most. Equation 4 describes how each counterpart
Figure 4. Illustration of scalar arithmetic expression for the 9-point box stencils with $m=2$. The approach is used to try to minimize the collect $C(E)$ during the computation process.

is obtained by vertical folding:

$$v_i^{(n)} = \sum_{l=-m}^{m} x_l^{(n)} \cdot u_{l+2}$$

, where $\lambda$ is the reassigned weight; superscripted $n$ is the counterpart number. For example, the weights for the first counterpart are reassigned as $\lambda^{(1)}=[1, 2, 3, 2, 1]$ by the folding matrix shown in Figure 5. According to Equation 4, each $v_i$ in the first counterpart $c_1$ is calculated by performing a sum on $v_{i-2}$, $2v_{i-1}$, $3v_{i}$, $2v_{i+1}$, and $v_{i+2}$.

**Horizontal Folding** With vertical folding completed, a local transpose is performed subsequently for further horizontal folding to collect the folded values in the same row:

$$v_i^{(c)} = \sum_{l=-m}^{m} u_{l+2}$$

, where $c$ is the total number of counterparts. Since reassigned weights for the other two counterparts $c_2$ and $c_3$ are represented by $\lambda^{(2)}=2\lambda^{(1)}=[2, 4, 6, 4, 2]$ and $\lambda^{(3)}=3\lambda^{(1)}=[3, 6, 9, 6, 3]$, the Equation 5 could be expanded as:

$$v_i^{(c)} = v_i^{(1)} + v_i^{(2)} + v_i^{(3)} + v_{i+1}^{(2)} + v_{i+2}^{(1)}$$

$$= v_i^{(1)} + 2v_{i-1} + 3v_i + 2v_{i+1} + v_{i+2}$$

. Thus, a coarse result $s_c$ for 2-step updates on a point square $s_o$ is obtained by only utilizing the square $c_1$.

**Weighted Transpose** Horizontal folding is followed by a weighted transpose at last. Conventionally the stencil of Jacobi style is implemented with two arrays $[7, 51]$, storing the value at odd and even time respectively. Therefore, the local transpose is optional here, and the result $s_c$ could be organized to the original layout by the transpose in horizontal folding alternately. The whole vectorized process is performed by using computation folding only on $c_1$ in practice, which correlates with the $v_i$ of scalar expression.
Figure 6. Illustration of shifts reusing in stencil computation.

in Figure 4. Thus the \(|C(E_\Lambda)|\) in Equation 3 is further decreased to 9, and we obtain a profitable index \(P(E, E_\Lambda) = 10\) theoretically.

### 3.4 Optimization

In this subsection, we present additional optimizations that we utilized in our approach.

**Shifts Reusing**  Figure 6 depicts a brief sketch of the scalar 1-step stencil computations between two adjacent grid points F and G in data space. It can be recognized from Figure 6 that there is potential for reusing shifts within the successive stencil computation from grid point F to G, and this gives us another reuse profitability of 2.25 by Equation 3. For our approach in Figure 5, the last two vectors of transposed counterpart \(c_i\) in each iteration can be reused as shifts between computing squares. Therefore, the optimization of reducing reloads across squares is enabled by utilizing the same data collected in the last round as input to be computed together, which contributes to further performance gains.

**Tessellate Tiling**  We also present a combination of our scheme and tessellate tiling [50] in our work. The tessellate tiling can be viewed as a tessellation in iteration space by utilizing shaped tiles. Figure 7 (a) and Figure 7 (b) illustrate the our scheme integrated with tiling for a 3-point stencil. The iteration space is tessellated by triangles and inverted triangles in alternative stages. Thus, concurrent execution is processed by two stages which are started in each triangle with a given time range first, followed closely by the execution of inverted triangles over the same time range concurrently. For the example in Figure 7 (a), the new state of each triangle contains \((0,1,2,3,4,3,2,1,0)\) where the center element is updated four steps and its neighbors are updated fewer steps proportional to the distance with the center element. To make all elements updated with the same steps, two half parts from adjacent triangles constitute new inverted triangles and the elements are updated with the state \((4,3,2,1,0,1,2,3,4)\). As Figure 7 (c) shows, all elements are updated to four steps by adding the projection of the triangles with inverted triangles. Moreover, the odd time steps are skipped over when computation folding approach is used with \(m=2\). The tessellate tiling could also be integrated into multidimensional stencil computations. For a \(d\)-dimensional stencil, tessellation in iteration space contains \(d+1\) stages. The spatial space in stage \(i\) is tessellated by \(tiles_i\) \((0 \leq i \leq d)\). \(tiles_1\) is a hypercube (typically a line segment in 1D, square in

2D, cube in 3D). \(tiles_{i+1}\) is built by recombining the sub-tiles split from adjacent \(tiles_i\) along some dimensions. Therefore, concurrent execution for different tiles is enabled over a given time range without redundant computation by the integrated tiling. The register transpose layout and time loop fusion also make it feasible to achieve multiple time steps computation in registers over the tiles efficiently without reloading operations.

### 3.5 Generalization

Although a standard 2D9P box stencil is illustrated as an example in Section 3.3, the computation folding approach can be extended in arbitrary stencil pattern by parameter tuning. It is observed that the computing expressions of different stencils reflect in the distinct \(\Lambda\) in folding matrix, and various counterparts are obtained by it. However, the \(\Lambda^{(m)}\) for counterpart \(c_m\) multiple of the other \(\Lambda^{(n)}\) for counterpart \(c_n\) is not guaranteed in some cases. Thus, we drill down into the computing process of these counterparts, and propose a linear regression model \([8, 10]\) to minimize \(|C(E_\Lambda)|\) by reusing the available counterparts. For the \(n^{th}\) counterpart \(c_n\), it can be obtained by Equation 7:

\[
c_n = \omega_{n-1} c_{n-1} + \omega_{n-2} c_{n-2} + \ldots + \omega_2 c_2 + \omega_1 c_1 + b_n = \omega c + b_n
\]  

where \(c\) is the vector of counterparts; \(\omega\) is the weight parameters for the counterpart \(c_n\); \(b_n\) is a bias for fine tuning results by the original square \(s_n\). For convenience, we define a function in Equation 8 that maps the solving cost of counterparts to collects:

\[
|C(E_\Lambda)| = \phi(c)
\]  

and the goal is to find the model parameter \(\omega\) which minimizes \(|C(E_\Lambda)|\) most. The search problem is then converted into a minimization problem on the opposite of the difference between optimized \(\phi(c^*)\) and original \(\phi(\hat{c})\), and the cost function \(J\) is formally described in Equation 9:

\[
J(\omega_i, b_i) = \sum_{j=1}^{n} (\phi(c_j^* (\omega_i, b_i)) - \phi(\hat{c}_j))^2
\]  

The parameters of \(\omega\) and \(b\) are subject to a constraint that a correct result is produced by them. Note that \(\hat{c}_j\) is computed by using \(s_j\) only without any counterpart reuse. For example, the counterpart \(c_2\) and \(c_3\) in Section 3.3 are both
4 Evaluation

In this section, we evaluate our proposed scheme on varied stencils used for real-world applications with AVX-2 and AVX-512 instructions.

4.1 Setup

Our experiments were performed on a machine composed of two Intel Xeon Gold 6140 processors with 2.30 GHz clock speed (turbo boost frequency of up to 3.70 GHz), which owns 36 physical cores organized into two sockets. Each core contains a 32KB private L1 data cache, a 1 MB private L2 cache, and a unified 24.75MB L3 cache. AVX-512 instruction set extension is supported and it’s able to conduct operations for 8 double-precision floating-point data in a SIMD manner, which yields a theoretical peak performance of 73.6 GFlop/s/core (2649.6 GFlop/s in aggregate).

Since the recent tiling technique (denoted as tessellation) proposed by Yuan [51] and the nested/hybrid tiling technique (denoted as SDSL, which is the name of the software package) presented by Henretty [18] outperform the other stencil research like Pluto [5, 7] and Pochoir [41], we take them as two bases of our work, which are vectorized by the compiler and DLT methods, respectively. All programs were compiled using the ICC compiler version 19.0.3, with the ‘-O3 -xHost -qopenmp -ipo’ optimization flags.

The detailed parameters for stencils used in experiments are described in Table 1, which consists of three star stencils (1D-Heat, 2D-Heat, and 3D-Heat) and three box stencils (1D5P, 2D9P, and 3D27P) corresponding to the references [18, 51]. Star and box equations are symmetric examples that can represent a wide variety of stencil kernels. Moreover, we also collect a series of classic benchmarks used in real-world applications [5, 31, 51]:

- APOP is a 1D3P stencil from two different input arrays to calculate the American put stock option pricing.
- The Game of Life is a cellular automaton proposed by Conway, and the update of each grid depends on all 8 of its neighbors.
- GB (general box) is an asymmetric 2D9P stencil that contains 9 different weights on the grid points in the computation process.

The default value of total time steps is 1000 or 200 in the references. Thus, we fix it as a larger value of 1000 in our experiments. Other parameters of each stencil are also fine-tuned based on references work to guarantee that the peak performance for all methods could be reached exactly. Since the performance is sensitive to the stencil parameters, significant efforts are required in automatic tuning and this will be done separately as future work.

| Type    | Pts | Problem Size     | Blocking Size |
|---------|-----|------------------|---------------|
| 1D-Heat | 3   | 10240000x1000    | 2000x1000     |
| 1D5P    | 5   | 10240000x1000    | 2000x500      |
| APOP    | 6   | 10240000x1000    | 2000x500      |
| 2D-Heat | 5   | 5000x5000x1000   | 200x200x50    |
| 2D9P    | 9   | 5000x5000x1000   | 120x128x60    |
| Game of Life | 8 | 5000x5000x1000   | 200x200x50    |
| GB      | 9   | 5000x5000x1000   | 200x200x50    |
| 3D-Heat | 7   | 400x400x400x1000 | 20x20x10      |
| 3D27P   | 27  | 400x400x400x1000 | 20x20x10      |
separately in two subfigures on the basis of the total time steps $T$. It can be seen that our method updating two time steps outperforms others apparently in both experiments, which demonstrates the effectiveness of the improvement of the flop/byte ratio. Our method without time loop fusion also achieves better performance results than the hand-written DLT in most cases. The performance has a decrease at the size of 1600 in L1 cache. This can be attributed to the cheaper dimension-lifting transpose operation in small size for DLT. The multiple loads method exhibits the worst performance among them due to the overhead caused by redundant loads. Moreover, the performance drops apparently as the problem size moves from L1 cache to the memory hierarchy, which is mainly caused by the cost of data transfers.

Table 2. Performance improvements on different storage level in single-thread blocking-free experiments

|                | Multiple Loads | Data Reorganization | DLT   | Our     | Our (2 steps) |
|----------------|----------------|--------------------|-------|---------|---------------|
| L1 Cache       | 1.00x          | 1.38x              | 2.06x | 2.16x   | 2.83x         |
| L2 Cache       | 1.00x          | 1.11x              | 1.37x | 1.80x   | 2.46x         |
| L3 Cache       | 1.00x          | 1.01x              | 0.95x | 1.73x   | 2.95x         |
| Memory         | 1.00x          | 1.00x              | 1.01x | 1.81x   | 2.68x         |
| Mean           | 1.00x          | 1.11x              | 1.35x | 1.98x   | 2.79x         |

To further investigate the effect of total time steps $T$, we perform a tenfold increase on the default value to $T = 1000$, which is illustrated in Figure 8 (b). It can be observed that the performance trends of $T = 10000$ are still largely consistent with the results in Figure 8 (a). However, the performance of our method falls slightly behind DLT in L1 cache, and this performance anomaly is primarily due to the diluted dimension-lifting transpose cost by overly long time steps. Notably, only the performance of DLT in L1 cache drops gradually as problem size increases for both results in Figure 8, which is resulted from a costly data layout transformation and indicates a potential bottleneck for cache-blocking.

We report the detailed results on the relative improvements of absolute performance for the time steps of 1000 on different storage levels in Table 2. The performance improvement of the series of our methods is the largest one in each case, which is unconstrained to the storage level. This reflects the best performance again and corresponds to the results of Figure 8.

4.3 Multicore Cache-blocking Experiments

In this subsection, we present the experiments that exhibit the benefits of our methods with the temporal blocking and parallelization scheme. The SDSL employs a split tiling technique (nested tiling in 1D, hybrid tiling for higher dimensions) to achieve temporal blocking [17]. The tessellate tiling technique utilized auto-vectorizing supported by the compiler [51].

Figure 9 shows the absolute performance comparison and speedups of the different benchmarks optimized by the blocking techniques. Since some benchmarks are not supported by SDSL, the speedups of each group are relative to the base which is annotated with the speedup value of 1. Taking all stencils with AVX-2 instructions into account, remarkable performance improvements are observed from our method updating two time steps, demonstrating that our vectorization scheme provides a significant benefit in a large problem size compared to the referenced work. Moreover, the optimization with AVX-512 instructions could obtain further performance gains. The performance of SDSL is inferior to tessellation, which is resulted from the blocking technique constrained to its data layout.

A closer look at Figure 9 indicates that the performance is relative to the shape, dimension, and weight of the stencils. For star-shaped stencils, higher performance improvements are obtained compared to the box-shaped due to fewer neighbor points. For lower-dimensional stencils, much higher reuse is achieved on the loaded inputs, which exhibits better performance. For the real-world stencils, we observed that the performance improvement obtained in GB benchmark is not prominent. This is mainly caused by the different weights for each input point in this asymmetric pattern. Although symmetric stencils are preferred in most real-world stencils, the GB benchmark can be viewed as a stress testing on our methods.

4.4 Scalability

We also evaluate the scalabilities of our schemes and benchmarks. The detailed parameters are given in Table 1, where all problem sizes exceed the L3 cache. Since our tiling framework is the same as the tessellation scheme, the performance improvements of our method with respect to the tessellation method are fully derived from the vectorization.

It can be observed in Figure 10 that our method could obtain the highest performance while the SDSL performs the lowest performance. In 1D3P stencils, all these methods achieve nearly linear scaling on both instruction sets and the proposed temporal computation folding provides a significant improvement. With the increase of the problem dimension, the scalability for all methods drops as a result of the inherent complexity for multidimensional stencil computations. Similarly, the overall performance of high-order stencils also falls behind the corresponding low-order results, which is resulted from complex data access patterns in high-order stencils. Compared to the results implemented with AVX-2 instructions, the performance of AVX-512 optimization shows a further increase.

The speedup for each method with 36 cores is given in Table 3. For scalability, our method obtains a 24.9x speedup.
while the value of SDSL is only 18.7x for 3D27P, which indicates a sustainable performance for our method in multidimensional stencils. Additionally, the largest speedup in each stencil column again corresponds to the performance shown in Figure 10, where our method outperforms others in most cases. Thus, our method could obtain a substantial performance improvement in all experiments.

4.5 Discussion
In this subsection, we provide an analysis of the performance on various configurations in previous experiments to tease

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**Figure 9.** Performance comparison and speedups for varied methods in multicore cache-blocking experiments.

**Figure 10.** Scalability for stencils of various orders with different dimensions in a multicore environment.

**Table 3.** Speedup over single core for different stencils

| Method          | 1D-Heat | 1D5P | APOP | 2D-Heat | 2D9P | GB   | Game of Life | 3D-Heat | 3D27P |
|-----------------|---------|------|------|---------|------|------|--------------|---------|-------|
| SDSL [17]       | 29.2x   | 27.9x| -    | 18.5x   | 22.1x| -    | -            | 15.3x   | 18.7x |
| Tessellation [51]| 29.8x   | 25.4x| 29.5x| 25.0x   | 29.1x| 22.0x| 23.2x        | 17.5x   | 19.2x |
| Speedup         | 30.8x   | 30.4x| 30.1x| 30.7x   | 30.4x| 23.9x| 24.2x        | 22.1x   | 24.7x |
| Our (2 steps)   | 32.1x   | 30.9x| 31.2x| 29.1x   | 29.3x| 22.8x| 24.7x        | 22.7x   | 24.9x |
| Our (2 steps, AVX-512) | 31.6x | 28.7x| 29.2x| 28.7x   | 29.6x| 23.2x| 24.5x        | 21.9x   | 24.9x |
out the contributions from different aspects of our proposed scheme. Sequential block-free experiments examine a variety of vectorization methods and demonstrate that our scheme with multiple time steps updating can achieve a considerable 3.32x improvement on average compared with the multiple loads method. Subsequently, the performance gains for larger time steps are still significant and consistent with the results of the small time steps. Moreover, DLT method is more appropriate only on the relatively small size and long time steps, and this is partly explained by the performance penalty associated with additional dimension-lifting transpose in memory. Since the problem size ranges from L1 cache to main memory, clear insights are provided that the overall performance trends drop consistently with the various memory hierarchy.

Multicore cache-blocking experiments conduct stencil cases with 36 cores, and an average 2.37x speedup is obtained by our method on the basis of SDSL. Due to the reduced arithmetic calculations by our time loop fusion, our method updated with two time steps is proved effective and achieves a further 3.29x speedup. Typically many modern processors contain AVX-512 instructions capable of performing on larger 512-bit registers, thus we also study the influence of them. The results reveal that they could contribute to better performance for our methods especially on 1D and 2D stencils. It is worth noting that the frequency reduction called throttling happens on CPUs when heavy AVX-512 instructions are involved. The slowdown is even worse with more cores employed. For example, the turbo frequency of the experimental machine drops significantly from 3.70 GHz to 3.00 GHz when active cores are expanded to full 18 on each processor [43]. AVX-512 implementation has a further decrease to 2.10 GHz, which can be blamed for the mediocre performance in 3D stencils. The overall trends are in accord with the sequential block-free experiments, and our method updated with two time steps outperforms others obviously.

The scalability experiments demonstrate that our vectorized scheme leveraging tessellate tiling successfully outperforms the referenced fastest multicore stencil work to date across a broad variety of configurations. Constrained to its specific data layout, DLT is slower than other methods. Since multidimensional or high-order stencils are more compute-intensive, more dependency data are loaded into cache while they are not fully utilized to perform their own stencil computation. Thus, the overall performance for each method falls gradually with the increasing dimensions or orders, and our method could still obtain a better performance.

5 Related Work

Research on optimizing stencil computation has been intensively studied [11, 23, 29, 40, 42], and it can be broadly classified as optimization methods to boost the computation performance, enhance the data reuse, and improve the data locality. Vectorization by using SIMD instructions is an effective way to improve computation performance for stencils. Henretty proposes a new method DLT [17, 18] to overcome input data alignment conflicts at the expense of a dimension-lifting transpose, which makes it infeasible to perfectly utilize the tiling technique as a result of its spatially separated data elements [24]. Essentially DLT can be viewed as the combination of strip-mining (1-dimensional tiling) and out-loop vectorization [18]. Specifically, the original innermost loop traverses the corresponding dimension from 1 to N. In DLT the loop is transformed to a depth-2 loop nest where the size of the outer loop equals the vector length vl and the inner loop processes each subsequence of length N/vl. Note that the strip-mining was also introduced for vectorization [2]. However, the conventional usage is to make the size of the innermost loop be the vector length and substitute it by a vector code. Furthermore, the in-place matrix transpose used for vectorization in our work has been widely studied and a kernel of 4×4 matrix transpose consists of two stages basically. Hormati splits the vector register to some 128-bit lanes [19], and the lane-crossing instructions for double incur a longer latency, typically 3 to 4 cycles. Zekri [52] use the in-lane instructions in four stages only for float type. Springer [38] utilize Shuffle and Permute2f128 instructions for double type in two stages, while it requires 8 integers as instruction parameters.

Data reuse has also been extensively recognized and exploited. Prior work [33, 34, 39, 54] on optimizing the order of execution instructions could decrease loads/stores operations to relieve the register pressure, while only the individual element in each vector could be reused. Basu designs a vector code generation scheme to reuse several vectors in the computation process, and it is constrained to constant-coefficient and isotropic stencils [6]. YASK [49] could improve data reuse by using common expression elimination and unrolling based on their vector-folding methods with fine-grained blocks [48], which is less feasible for high-order complex stencils [54]. Zhao [54] designs a greedy algorithm to decide the part of the computation with high reuse. For other parts not identified by the algorithm, they still utilize the original computation by gather operations. Rawat [33] utilizes a DAG of trees with shared leaves to describe the stencil computation, and devises a scheduling algorithm to minimize register usage by reordering instructions on GPUs. Common subexpression elimination (CSE) [1] is presented to reduce the redundant computation in successive iterations of the same loop by reusing partial sums of a subexpression. This method relies heavily on loop unrolling to find specific expressions. Deitz extends the CSE method as Array Subexpression Elimination (ASE) [13] by creating an abstraction called a neighborhood tablet. Since the ASE reuses partial
sums by subtablets via temporary variables, scalar dependencies are newly introduced and hinder the instruction-level parallelization by compilers.

Tiling [20, 25, 28, 44, 45] is one of the most powerful transformation techniques to explore the data locality of multiple loop nests. Notably work for stencil computations includes hyper-rectangle tiling [14, 30, 32, 35], time skewed tiling [21, 37, 46], diamond tiling [5, 7], cache oblivious Tiling [15, 40, 41], split-tiling [18] and tessellating [50]. Wonmacott and Strout present a comparison on the scalability of many existing tiling schemes [47]. Most of these techniques are compiler transformation techniques and this paper integrated the new proposed layout with the tessellation scheme for simplifying the implementation. For stencil computations, a variety of auto-tuning frameworks [9, 16, 22, 53] have been presented by using varied hyper-rectangular tiles to exploit data reuse alone. However, redundant computations are involved in these work to resolve the introduced inter-tile dependencies that hinder the concurrent execution of shaped tiles on different cores.

6 Conclusion

In this paper, we propose a novel transpose layout to overcome the data alignment conflicts efficiently for vectorization in the data space. Then a computation folding approach by reducing the redundancy of arithmetic calculations in time iteration space is devised on the basis of the proposed transpose layout. Furthermore, we describe how the proposed vectorization scheme is optimized with shifts reusing for enhancing data reuse and integrated with tessellate tiling for improving data locality. With the qualitative analysis and quantitative experiments, we demonstrate that significant performance improvements are achieved by our vectorization scheme over state-of-the-art products such as Intel’s ICC and recent work [18, 51].

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