Versatile Thin-Film Transistor with Independent Control of Charge Injection and Transport for Mixed Signal and Analog Computation

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New materials and optimized fabrication techniques have led to steady evolution in large area electronics, yet significant advances come only with new approaches to fundamental device design. The multimodal thin-film transistor introduced here offers broad functionality resulting from separate control of charge injection and transport, essentially using distinct regions of the active material layer for two complementary device functions, and is material agnostic. The initial implementation uses mature processes to focus on the device’s fundamental benefits. A tenfold increase in switching speed, linear input–output dependence, and tolerance to process variations enable low-distortion amplifiers and signal converters with reduced complexity. Floating gate designs eliminate deleterious drain voltage coupling for superior analog memory or computing. This versatile device introduces major new opportunities for thin-film technologies, including compact circuits for integrated processing at the edge and energy-efficient analog computation.

Large area electronics (LAE) based on thin-film transistors (TFTs) have an enormous potential for emerging applications in distributed autonomous sensors, wearables, and human–environment interaction. Incremental developments through technological refinement (e.g., process control) are complemented by less frequent, yet major, advances in material performance (e.g., carrier mobility, moisture resilience) (Figure 1a). It is, however, with the adoption of radical new approaches that large leaps forward are made.

We propose a TFT structure, named the multimodal transistor (MMT) (Figure 1b and Figure S1, Supporting Information), with superior functionality achieved by separately controlling charge injection from charge transport. This results in: low distortion for single-stage amplifiers; up to 90% faster response than other contact-controlled transistors; immunity to gain loss when used in analog floating gate (FG) applications; and substantial tolerance to geometrical registration errors. These features can be applied to highly topical areas, from compact, high-performance LAE signal-processing interfaces for sensors (e.g., amplification, event detection, and multiparameter decision—Figure 1c) to analog memory and neuromorphic computing.

Two factors make our approach timely. First, there is a consensus on the necessity for energy-efficient, high-performance autonomous sensors with integrated processing capability, where TFTs “at the edge” promise low-cost solutions for initial data handling. MMT circuits providing gain, decision, classification, and signal conversion would drastically reduce transistor count with important benefits to manufacturing yield, power efficiency, and circuit area. Second, MMT fabrication uses elements which are either strongly emerging or starting to be implemented commercially and increasingly, constructive use of often-avoided contact effects is finding its way into production, thereby reducing the technological barrier. Furthermore, multigate architectures have permeated display and sensor designs, as a means of enhancing performance or mitigating variability, indicating that the community is disposed to exploring multi-port TFTs.

To introduce the potential of the MMT, its operation is first described together with its basic functionality, followed by several examples of its versatility and breadth of application. As the device is technology agnostic, we demonstrate its features using established materials and processes. From initial results in microcrystalline silicon (μ-Si) complemented by technology computer-aided design (TCAD) analysis (see Experimental Section for materials, processes, and simulation parameters), we first clarify the origin of its fast switching. Next, we explore the basis of its constant transconductance and its relevance to...
minimal, low-distortion gain stages and compact, multilevel digital-to-analog converters. Finally, we describe the advantages of the MMT’s FG variant in suppressing deleterious capacitive coupling effects for facile analog processing, as a stepping-stone toward robust, efficient LAE neuromorphic systems.\[9\]

In its basic structure, the staggered-electrode MMT (Figure 1b) has the typical source and drain contacting a semiconductor with multiple control gates separated by insulating layers. There have been several ingenious applications of auxiliary gates in transistor structures, designed to preferentially select for one charge carrier type in ambipolar materials, or to increase the effective mobility.\[14,18\] Although structurally similar, the MMT contains a deliberately-engineered energy barrier at the source contact\[16,22–26\] as the foundation of the current control process involving one or more injection control gates (CG1). Situated opposite the source, CG1 provides the means for controlling the quantity of charge injected into the device. The channel control gate (CG2), situated above the source-drain gap, toggles the conduction state of the semiconductor between the source and drain. As such, CG1 exclusively controls the current level, whereas CG2 halts or permits the flow of current without affecting its magnitude. The combined “analog” injection and “digital” switching (Figure S2, Supporting Information) make possible the device’s exceptional versatility, enabled by modulating contact properties as its prime input.

To illustrate the operating principle of an n-type MMT, we refer to the schematic cross-sections in Figure 1d, in which the drain is positively biased. All analyses were performed in common-source configuration, and therefore we refer to node potentials relative to the grounded source. Positive CG1 potential $V_{CG1}$ accumulates the semiconductor–insulator interface, but charge transport to the drain is restricted by the highly resistive source-drain gap (Figure 1d, left). Similarly, an accumulated “channel” via CG2 positive bias $V_{CG2}$ produces no current flow in the absence of CG1 potential (Figure 1d, center). The simultaneous application of CG1 and CG2 bias allows charge injection at the source and transport to the drain (Figure 1d, right). The shaded area within the semiconductor indicates the depletion region created when the source energy barrier is reverse biased by the applied drain voltage, pinching-off the accumulation layer and resulting in low-voltage saturation of electrical characteristics.\[22,27–29\]
Band diagrams extracted from simulation are discussed in Figure S3, Supporting Information, while a qualitative conduction band energy profile is shown in Figure 1e. In the left panel, the device is conducting and in saturation. Drain voltage variations translate exclusively into changes in channel potential. As the magnitude of the current is solely controlled at the source by CG1, drain current is practically independent of both drain bias and of source–drain gap. Increasing the CG1 voltage (solid line; Figure 1e, center) boosts injection from the source area via two overlapping mechanisms discussed elsewhere.\(^{[22,27–30]}\) Finally, the effect of CG2 voltage is shown in the right panel. The device is “off” when no potential is applied. When channel conductance increases above a minimum value, applied CG2 voltage does not play a role in controlling drain current magnitude.

Figure 1f shows a typical microcrystalline silicon (μ-Si) MMT, denoting the source–drain gap (d), and source–CG1 overlap (S). As these devices have two control terminals, one set of output and two sets of transfer characteristics are measured to study device behavior. Output characteristics (Figure 1g) show the expected signs of purposeful contact-controlled injection: low dependence of drain current \(I_D\) on drain voltage \(V_D\) and low saturation voltage, \(V_{\text{DSAT}}\). The saturation coefficient \(\gamma = dV_{\text{DSAT}}/dV_{\text{CG1}}\) is estimated at 0.18, much smaller than the unity value of conventional TFTs, indicating low series voltage operation capability.\(^{[27,28]}\) Next, Figure 1h shows the effect of CG2 bias for a range of \(V_{\text{CG1}}\). As expected, when the channel is “on”, the current is largely independent of CG2 voltage, except for the presence of a moderate kink effect,\(^{[31,32]}\) discussed later. Devices in this batch have a negative threshold, therefore turning “off” the channel requires negative \(V_{\text{CG2}}\). Lastly, the CG1 transfer curve in Figure 1i confirms the expected modulation of drain current over several orders of magnitude with applied CG1 bias. Although \(I_D\) magnitude is low, these initial results confirm MMT operation. With optimization, MMTs should match the current density seen in other contact-controlled devices,\(^{[22,29]}\) and improve with advancements in materials and techniques (Figure 1a).

Further electrical data are included in Figure S4 and S5, Supporting Information.

Charge control at the source of the MMT closely resembles that in source-gated transistors (SGTs).\(^{[27–29,33]}\) As such, the analysis in the study by J. Zhang et al.\(^{[29]}\) applies in the first order. In saturation, we can describe the fundamental operation of an ideal MMT device by the following equation.

\[
I_D = \begin{cases} 
 g_m \cdot V_{\text{CG1}}, & V_{\text{CG2}} > V_{\text{th2}} \\
 0, & V_{\text{CG2}} < V_{\text{th2}}
\end{cases}
\]  

(1)

where \(g_m = dI_D/dV_{\text{CG1}}\) is the transconductance associated with CG1 and \(V_{\text{th2}}\) is the value of \(V_{\text{CG2}}\) above which it has no influence on \(I_D\).

It is essential to design the device so that electric fields generated by CG2 do not penetrate to the source. Optimized MMTs should show significant tolerance to gross misalignments (Figure S6 and S7, Supporting Information).

We now demonstrate the practical consequences of the independent MMT control processes via TCAD simulation of prototypical devices, focusing first on performance, and subsequently on functionality. The injection of charge at the source follows the behavior of SGTs.\(^{[22,29]}\) These extensively studied devices produce excellent d.c. characteristics, but an exceedingly long response time, arising from the low transconductance afforded by the rectifying contact, combined with the large gate–source overlap capacitance necessary for optimal injection.\(^{[15]}\) MMT construction allows the separation of the “slow” injection from the “fast” channel switching.

**Figure 2a** shows the comparative transient response time for TFT, SGT and MMT devices. An extremely fast initial transient is observed for the MMT. The settling time to 1% of final output voltage also reduces with \(V_{\text{CG2}}\), eventually outperforming the equivalent TFT (Figure 2b). This preloading effect of \(V_{\text{CG2}}\) eliminates the time required to accumulate the insulator interface in the source region. The CG1–CG2 interplay (Figure 2c) is studied further in Figure S8, Supporting Information. High \(V_{\text{CG2}}\), which may be expected to reduce transient time, could degrade the output conductance in certain semiconductors (Figure 2d), in which high electric fields seen at the channel extremities (Figure 2e) lead to hot-carrier effects\(^{[31,32]}\) depending on the biasing condition. Where possible, the lowest value should be chosen for \(V_{\text{CG2}}\), while ensuring that the channel: 1) is sufficiently conductive so that it does not impede the current flow set by \(V_{\text{CG1}}\) and 2) is never strongly pinched-off at the drain end.

Since MMT operation has the intrinsic ability to switch significantly faster than the SGT, in logic applications, connecting CG1 to the relevant power rail would lead to improved switching speed, at the same time preserving the noise margin, gain, and energy efficiency shared with SGTs. Thus, the MMT marks an order-of-magnitude performance gain in the transient capability of contact-controlled transistors.

As to the expansion of functionality granted by the distinct controls, CG2 can be conceived of as an “enable” signal. A compact multipurpose application is MMT-based digital-to-analog conversion (DAC). Several CG1 electrodes (Figure 2f and Figure S11, Supporting Information) act as inputs taking binary-coded values. Their contact areas \(A_i\) are such that \(A_1 = A_0 \cdot i\), where \(i\) is the respective power of 2 and \(A_0\) is the area corresponding to the least significant bit (LSB). CG2 is connected to a sample-and-hold (S/H) signal, thereby realizing an extremely compact circuit (Figure 2g), which produces an output voltage deflection proportional to the input digital value (Figure 2h).

The MMT DAC is a typical example of the device’s ability to provide complex functionality while significantly reducing component count, a paramount consideration for the success of LAE fabricated with extremely low-cost methods.\(^{[11]}\) For example, wireless powered, fully printed functional tags (Figure 2i) containing minimal circuitry for power management and digital data handling would only require this compact and robust DAC to produce, with low distortion, analog signals required by a display, alarm, or actuator module.

Up to this point, we have focused on device operation using CG2 as the main functional input. The following analysis concentrates on CG1, specifically on its role in attaining constant transconductance, \(g_m = dI_D/dV_{\text{CG1}}\). A linear input–output relationship is highly desirable for many signal-processing applications, but typically requires large linearization circuits. Achieving this behavior with a minimal set of components is essential in LAE technologies.\(^{[11]}\)
The source area of the MMT can be analyzed similarly to SGTs, observing that the injection along the length of the source can be ohmic and directly proportional to applied CG1 bias. To obtain close to linear dependence of total drain current on CG1 voltage, the contribution from the high field region at the edge of the source (x = 0 in Figure 1d) needs to be reduced.\[22\] In the MMT, this is assisted by the opportunity to keep the source–drain gap highly conductive regardless of the input signal on CG1. As such, MMTs can achieve constant $g_m$, confirmed by measurements on initial $\mu$-Si devices. Output curves (Figure 3a) have $\gamma \approx 0.16$ and good saturation, indicating contact-controlled operation. The transfer plot in Figure 3b shows remarkable linearity (constant $g_m$), with a 0 V abscissa intercept (direct proportionality).

We note that both linear behavior and direct proportionality result from the correct design of the transistor, and manifest in saturation, unlike in conventional TFTs, adding to the application versatility. Usual threshold control techniques can translate the transfer curve horizontally, while optimizing device electrostatics attains constant $g_m$, confirmed by measurements on initial $\mu$-Si devices. Output curves (Figure 3a) have $\gamma \approx 0.16$ and good saturation, indicating contact-controlled operation. The transfer plot in Figure 3b shows remarkable linearity (constant $g_m$), with a 0 V abscissa intercept (direct proportionality).

Figure 2. Outcomes of separating control for injection and conduction shown via TCAD simulation. a) MMT transient response is much faster than conventional contact-controlled TFTs and b) can be faster than ohmic contact TFTs. c) CG2 voltage affects not only transient response, but also d) in materials susceptible to hot carrier effects, such as poly-Si, output current saturation, e) due to generation in areas of high electric field. f) A MMT with multiple, appropriately sized CG1 gates can function as a digital-to-analog converter (DAC) with CG2 providing an enabling, sample-and-hold (S/H) function. g) Compact DAC circuit. h) Simulated 3-bit DAC response showing linear dependence of final output voltage on digital input value. i) Schematic representation of a fully integrated large area wirelessly powered system producing an output in accordance to received digital data.

This region starts at $V_{CG1}$ for which the whole source length contributes to charge injection, a value which depends on the electrostatics and conductivities of essential regions of the device. As linearity and saturation are affected by the properties and sizing of the semiconductor and insulator, a trade-off emerges (Figure 3f). With the present choice of materials, $t_s = 40$ nm and $t_i = 20$ nm result in the optimum linear transfer curve for lowest $V_{CG1}$ operation. The corresponding $\gamma \approx 0.39$ is comparable with the value of $\approx 0.32$ extracted from output characteristics (Figure S9c and S9d, Supporting Information) allowing low $V_{DSAT}$.

A direct application of these findings is in low distortion amplifiers, where gain stage non-linearity produces unwanted frequency components in the output signal (Figure 3g). We simulated a common-source MMT amplifier in which the channel was fully open, focusing exclusively on the performance of the drive transistor by choosing a purely resistive load. In this application, a zero-intercept of the MMT transfer curve is not required, but the amplifier output must not saturate. Low distortion is observed for relatively large input excursion, improving when reducing $t_i$. This is evidenced in the gain profile (Figure 3h) and the spectral analysis of the output signal obtained for a pure sinusoidal input (Figure 3i). The linearity of the transfer characteristic arises as a trade-off against maximum $g_m$, and consequently, the measured and simulated gain achievable in the current batch of devices is around 6–10. However, MMTs can be realized with higher $g_m$ at the expense of linearity, and output
conductance, \( g_d = dI_d/dV_d \), can be improved via the usual field relief strategies, for improved overall gain, \( A_V = g_m/g_d \). \[35\]

Similar benefits could be derived in certain pixel circuit designs where, for example, optical feedback may be used to create a simple means of compensating local pixel aging or large area non-uniformities (Figure 3j).

Yet another efficient use of constant \( g_m \) is in the DAC circuits of Figure 2f–h. By generating drain currents that are simultaneously proportional to CG1 width and CG1 voltage, multilevel digital signals can readily be converted with minimal error. Figure 3k shows the output waveform of a 3-bit 3-level DAC, and the error of output current \( I_{out} \) expressed as a percentage of \( I_{LSB} \). The optimum design for the current setup is \( S = 4 \mu m \) with \( t_s = t_L = 40 \, nm \), which offers low output error (\( \leq 1.2\% \) of \( I_{LSB} \)) for moderate to high input voltages. For digital data coded with lower voltage levels, \( t_s = 20 \, nm \) is optimal (Figure S12, Supporting Information), correlated with the improved low-voltage linearity (Figure 3c).

Leveraging the two control mechanisms and constant \( g_m \), conceivably the most attractive long-term application of MMTs is in the field of energy-efficient analog and neuromorphic computation (Figure 3l). Compact circuits with complex functionality can be realized, in line with the immediate benefits of TFT-based edge computing for sensors. One additional advantage of MMT operation emerges in the FG embodiment. Discussed next are the facile implementation of analog operations and the analog memory capability (Figure 3m), with enormous potential for learning and reconﬁgurability in neuromorphic thin-ﬁlm circuits.

As with the control method separation, we will analyze floating gate MMTs (FGMMTs) from both performance and functionality standpoints.

FG transistor architectures are widely used, typically for high-density non-volatile memory and analog signal processing. \[36,37\] In particular, scaled, thin-ﬁlm devices, in which the gate coupling region does not extend signiﬁcantly beyond the device active area, suffer a loss of intrinsic gain due to parasitic capacitive coupling of the channel and drain potential to the FG. For these devices to be effectively used in emerging non-von Neumann approaches to computing based on neuromorphic or analog...
strategies, inherent limitations need to be addressed. This is especially true in thin-film devices, which suffer from variability, bias effects, and non-linearity.\(^{[2,11,36]}\) For example, SGTs offer superior intrinsic gain\(^{[29,38]}\) and robustness\(^{[39]}\) when compared to conventional TFTs, but their gain characteristics suffer drastically in FG designs.

FGMMTs are immune to gain reduction by design, having potential for greatly expanding the applicability of FG devices to advanced, energy efficient analog circuits.

The first FGMMT design (Figure 4a) has a single control gate, CG, and two FGs: FG1 overlapping the source and FG2 spanning the source–drain gap. \(\mu\)-Si devices (Figure 4b and Figure S11a, Supporting Information) show low-voltage saturation with \(\gamma \approx 0.29\), quasi-constant transconductance, and flat output characteristics (Figure 4c) indicative of low output conductance, \(g_\text{d}\) and thereby retaining suitable gain.

TCAD simulations provide insight into gain loss in contact controlled floating gate SGTs (FGSGTs) and validate the superior behavior of MMTs.

In FGSGTs, the capacitive coupling of the FG to the channel (\(C_{\text{GCh}}\)) and drain (\(C_{\text{GD}}\)) (Figure S14, Supporting Information) results in an increase of FG potential with \(V_D\), promoting injection at the source and deteriorating \(g_\text{d}\) and \(A_V\) (Figure 4d and Figure S15, Supporting Information). This is further discussed in Figure S16 and S17, Supporting Information.

FGMMTs with separate FG1 and FG2 show no \(g_\text{d}\) degradation (Figure S18, Supporting Information). Although the potential in the channel increases with \(V_D\) (Figure S19a, Supporting Information).

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**Figure 4.** Floating gate multimodal transistors (FGMMTs). a) FGMMT schematic diagram. b) Micrograph of a \(\mu\)-Si FGMMT. c) Measured FGMMT output curves showing flat saturation, and therefore, no \(g_\text{d}\) degradation due to capacitive coupling to FGs. d) Simulated source-gated transistor (SGT) output illustrating its degraded behavior in FG configuration as a result of parasitic capacitive coupling to the FG, where \(V_{CG}\) was chosen to maintain a similar vertical electric field given the different insulator stack. e) Simulated FG potential plots explain the origin of FGMMT saturation performance. f) Low output conductance \(g_\text{d}\) is maintained in contrast with FGSGTs (simulated). g) Schematic reference voltage generation taking advantage of FGMMT characteristics. h) FGMMT in summing configuration, where CG2 acts as an enable switch. Measured summing FGMMT response to i) d.c. and j) periodic voltage inputs.
Information), the potential in the accumulation region along the source contact (denoted \(V_{\text{CH}}\) in Figure S14, Supporting Information, and primarily responsible for charge injection\(^{[29]}\)), remains constant, unlike in the FGSGT (Figure S19b, Supporting Information). Essentially, in the FGMMT, the channel and drain (see Figure S14c, Supporting Information) capacitively couple exclusively to FG2, which has the effect of shielding FG1 from drain-induced potential variations (Figure 4e). Since the conductance of the source–drain gap does not play a role in regulating current in contact-controlled transistors, a large change in FG2 induced by \(V_D\) produces no change in \(I_P\). Specifically, the FGMMT’s \(A_V\) is maintained by keeping an extremely low \(g_{ds}\) (Figure 4f).

Naturally, charge trapping on FG1 can be exploited in the usual ways,\(^{[40]}\) creating threshold shifts (Figure 3m), which allow operation as analog memory. Although programming experiments do not form part of the present study, this behavior is important, as it applies to a large range of widely used functional blocks, e.g., ultra-low power voltage references (Figure 4g), in which the low \(g_{ds}\) of the FGMMT would provide precision in a minimal layout.

A second FGMMT design (Figure 4h and Figure S13b, Supporting Information) takes advantage of the constant \(g_{in}\) and low \(g_{ds}\) to allow linear addition of analog signals using two inputs, CG1A and CG1B in a compact design. Figure 4i illustrates \(\mu\)-Si FGMMT drain current when voltages are asserted on either or both inputs, while Figure 4j depicts the results of summing two waveforms of different frequencies. As a strategy for producing decisions based on the concurrent behavior of multiple continuous signals, this approach improves on conventional designs through the low dependence on power supply fluctuations (low \(g_{ds}\)) and the extremely compact implementation.

More generally, and with disruptive implications, the FGMMT can function as an analog/neuromorphic processing element\(^{[9]}\) in a thin-film artificial neural network implementation. With multiple inputs, each with its own synaptic weight represented by FG charge programming, MMT neurons can readily emulate fully connected neural networks. For instance, with the achievement of energy-efficient, highly linear FGMMTs with a compact layout.

In summary, we have presented a low-complexity, highly versatile transistor structure with material agnostic operation. Its standardized fabrication process makes it well suited for integration in large-area circuits, side-by-side with conventional TFTs.

The current study is not intended as a performance benchmark. Rather, it is a demonstration, using an accessible and mature technology, of the MMT’s potential. Notably, high-speed switching, constant transconductance, and immunity to drain coupling in analog FG designs complement the desirable features that make contact-controlled devices attractive: energy efficiency in saturation and tolerance to both bias stress and geometrical variability.

Immediate applications are in display and imager array compensation, and data conversion. The architecture also holds the ingredients for medium-term implementation in powerful classification and event detection for fully integrated, low-cost autonomous sensors. Uniting the presented characteristics with usual analog memory functions would confer MMT circuits the ability to retrain and “learn” at runtime, a potential to be fully realized by highly multidisciplinary cooperation in a variety of material systems.

### Experimental Section

#### MMT Fabrication and Characterization

To demonstrate the capability of MMTs, bottom gate top contact (BGTC) devices were realized in \(\mu\)-Si using very low temperature technology (\(-200\) °C). This technology was based on microcrystalline silicon (\(\mu\)-Si)\(^{[19,20]}\) which presents 20–30 nm grain size, associated with a global crystalline fraction reaching 75%. With this low thermal budget, this technology could fit with a large range of flexible substrates and was based on plasma-enhanced chemical vapour deposition (PECVD) or inductively coupled plasma-CVD (ICP-CVD) equipment, as demonstrated in this study. ICP-CVD was capable of providing both \(\mu\)-Si and oxide layers, however, the main interest of this method was to perform the CVD process at low temperature and low pressure using the huge chemical density of its plasma, without applying bias voltage. Therefore, by using the aforementioned layers, we can fabricate on different carrier substrates (e.g., kapton, polyimide films, etc.) Devices could thus be fabricated on Si wafers, borosilicate glass, or polyimide films.

The first step consisted of a 150 nm Al deposition, realized by electron beam evaporation. After this, a 700 nm ICP-CVD oxide layer was deposited by photolithography and etching by Cl2 inductively coupled plasma reactive ion etching (ICP-RIE, Corial 200IL) to create the CG1 bottom gate. This gate was then covered by a 100 nm ICP-CVD oxide layer (Corial 210D) formed using a SiH\(_4\)/O\(_2\)/Ar mixture at 70 °C. The oxide layer was baked at 180 °C under N\(_2\) for 3 h to increase density and breakdown voltage. Contacts were opened by photolithography with oxide etching by CF\(_4\) plasma (Corial 200IL). The same process was used to define a 150 nm CG2 Al gate, which was also insulated with a similar 100 nm ICP-CVD oxide layer. This second oxide was opened by CF\(_4\) plasma etching at the location of the contacts. Following the second gate oxide, a 50 nm ICP-CVD (Corial 210D) \(\mu\)-Si active layer was deposited. The \(\mu\)-Si layer was formed using a SiH\(_4\) gas precursor with Ar and H\(_2\) at 180 °C. The active layer was etched with SF\(_6\) plasma (Corial 200IL) before being covered by a 20 nm ICP-CVD oxide layer for the formation of a field plate at the source edge, which provides relief from the lateral electric field at the drain.\(^{[12]}\) This field plate oxide was etched by SF\(_6\) plasma to intentionally decrease the etching rate of oxide, and increase the interferometric etch rate control contrast with respect to the active layer. Drain and source steps consisted of a Ni deposition by EBD and patterned by lift-off in acetone, assisted by ultrasonication. The final step was a 200 nm Al EBD deposition, which was etched in Cl2 plasma (Corial 200IL) for pads and metal path realization. An ohmic drain could be realized, but required additional processing steps.

Electrical characterization of the MMTs and FGMMTs was performed on a wentworth probe station. Measurements were taken using the eight B2902A source/measure unit (SMU) controlled by Keysight Quick IV Measurement Software v.4.0.1648.5970 with an additional Weir 413D voltage source. The eight B2902A source/measure unit (SMU) controlled by Keysight Quick IV Measurement Software v.4.0.1648.5970 with an additional Weir 413D voltage source as a constant voltage supply for either CG1 or CG2, depending on which variable was being swept. For the summing FGMMT with two CG1 inputs (CG1A and CG1B), two Keysight B2902A SMUs were used to supply sine waves of different frequencies on each CG1.

Measurements of Figure 1g–i were obtained from a \(\mu\)-Si MMT with dimensions: \(W = 50 \mu\text{m}\); \(S = 6 \mu\text{m}\); and \(d = 6 \mu\text{m}\). The \(\mu\)-Si MMT in Figure 3a,b had dimensions: \(W = 50 \mu\text{m}\); \(S = 54 \mu\text{m}\); and \(d = 18 \mu\text{m}\). Dimensions for the measurements of the FGMMT (Figure 4c) and summing FGMMT (Figure 4l,i) were: \(S = 54 \mu\text{m}\); \(d = 18 \mu\text{m}\); \(g_0 = 4 \mu\text{m}\); and \(W = 50 \mu\text{m}\) for each FG. The CG of the FGMMT overlapped both FG1 and FG2 (Figure 4a and Figure S13a, Supporting Information), while the summing FGMMT had CG1A and CG1B overlapping an FG above the source, with CG2 acting as an enable function (Figure 4h and Figure S13b, Supporting Information).
All MMTs and the summing FGMMT included a 2 μm Cu/Cu2 overlap, 2 μm field plate extension, and 20 nm field plate insulator. From previous studies, the field plate would be more effective if made somewhat shorter, as a proportion of the source–drain gap, and brought closer to the semiconductor surface. A conservative approach was adopted in this design to promote prototyping yield.

It should be noted that the schematic cross sections and 3D drawings of MMTs in Figure 1, 2, 4, Figure S6 and S14, Supporting Information, show bottom contact, top gate (BCTG) devices. This was preferred for clarity of presentation and consistency, facilitating the comparison between the various multi-input device implementations. Naturally, the MMT could be implemented in either BCTG or BGTC configuration.

Device and Circuit Simulation: Simulations provided insight into device operation and were not intended to match the fabricated devices. Silvaco Atlas v.5.24.1.R. was used, including its mixed-mode capability for exploring circuit behavior.

We had chosen materials with known limitations to provide challenging conditions for the various studies. For example, polysilicon (poly-Si) devices would usually suffer from significant kink effect, which would degrade the attainable gain, although amorphous silicon was chosen to illustrate the significant improvement in transient response.

Table S1, Supporting Information, contains device geometries and parameters for all TCAD simulation studies with the majority performed using a-Si unless otherwise stated. The CG1–CG2 gap for all devices was 1 μm and overhang height was 30 nm for all simulations. For the poly-Si MMT, a source field plate was included to provide drain relief. Field plate extension and height were 0.5 μm and 20 nm, respectively.

Table S2, Supporting Information, contains additional simulation parameters pertaining to the materials used. MMT and SG devices in a-Si included 3 × 10^{10} cm^{-2} n-type doping at the drain. The MMT in poly-Si used intrinsic material parameters. Conventional TFTs were doped 3 × 10^{12} cm^{-2} n-type under both source and drain to create ohmic contacts.

Mixed-mode simulations of the switching transient of CG2, the DAC, and the low distortion amplifier circuits contain additional components or specific geometries. All devices in the CG2 switching transient study (Figure 2a–c and Figure S8, Supporting Information) have \( W = 1 \) μm; \( S = 1 \); \( d = 4 \) μm; and \( t_s = t_i = 40 \) nm. The common source circuit configuration included \( R_s = 100 \) MΩ and, to aid convergence, \( C = 1 \) F.

For the DAC circuits (Figure 2h and 3k), the respective gate widths were: LSB \( W_{\text{LSB}} = 10 \) μm; MSB \( W_{\text{MSB}} = 40 \) μm; and \( C = 10 \) nF.

The low distortion common source amplifier (Figure 3i) device width was \( W = 100 \) μm. The load resistor value for \( t_s = 40 \) nm was \( R_l = 4 \) MΩ and for \( t_s = 80 \) nm, \( R_l = 8.5 \) MΩ to provide similar circuit transfer characteristics and gain.

### Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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### Conflict of Interest

The authors declare no conflict of interest.

### Keywords

analog circuits, contact barriers, floating gates, semiconductor devices, thin-film transistors

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[1] S. Jeon, S. C. Lim, T. Q. Trung, M. Jung, N. E. Lee, Proc. IEEE 2019, 107, 2063.
[2] H. E. Lee, J. H. Park, T. J. Kim, D. Im, J. H. Shin, D. H. Kim, B. Mohammad, I. S. Kang, K. J. Lee, Adv. Funct. Mater. 2018, 28, 1.
[3] J. S. Chang, A. F. Facchetti, R. Reuss, IEEE J. Emerg. Sel. Top. Circuits Syst. 2017, 7, 7.
[4] D. E. Schwartz, J. Rivnay, G. L. Whiting, P. Mei, Y. Zhang, B. Krusor, S. Kor, G. Daniel, S. E. Ready, J. Veres, R. A. Street, IEEE J. Emerg. Sel. Top. Circuits Syst. 2017, 7, 27.
[5] X. Guo, Y. Xu, S. Ogier, T. N. Ng, M. Caironi, A. Perinot, L. Li, J. Zhao, W. Tang, R. A. Sporea, A. Nejim, J. Carrabina, P. Cain, F. Yan, IEEE Trans. Electron Devices 2017, 64, 1906.
[6] R. A. Street, T. N. Ng, D. E. Schwartz, G. L. Whiting, J. P. Lu, R. D. Bringans, J. Veres, Proc. IEEE 2015, 103, 607.
[7] Y. Kuo, Electrochem. Soc. Interface 2013, 22, 55.
[8] M. Kaltenbrunner, T. Sekitani, J. Reeder, T. Yokota, K. Kuribara, T. Tokuhara, M. Drack, R. Schrödlauer, I. Graz, S. Bauer-Gogonea, S. Bauer, T. Someya, Nature 2013, 499, 458.
[9] C. Mead, Proc. IEEE 1990, 78, 1629.
[10] L. Petti, N. Münzenrieder, C. Vogt, H. Faber, L. Büthe, G. Cantarella, F. Bottacchi, T. D. Anthopoulos, G. Tröster, Appl. Phys. Rev. 2016, 3, 1.
[11] A. F. Paterson, T. D. Anthopoulos, Nat. Commun. 2018, 9, 1.
[12] M. A. McCarthy, B. Liu, A. G. Rinzler, Nano Lett. 2010, 10, 3467.
[13] F. Torricelli, L. Colalongo, D. Raiteri, Z. M. Kovac-Vajina, E. Cantatore, Nat. Commun. 2016, 7, 1.
[14] H. Yoo, M. Ghittorelli, D. K. Lee, E. C. P. Smits, G. H. Gelincik, H. Ahn, H. K. Lee, F. Torricelli, J. J. Kim, Sci. Rep. 2017, 7, 1.
[15] M. J. Seok, M. Mativenga, D. Geng, J. Jang, IEEE Trans. Electron Devices 2013, 60, 3787.
[16] V. K. Sangwan, M. E. Beck, A. Henning, J. Luo, H. Bergeron, J. Kang, I. Balla, H. Inbar, J. L. Lauhon, M. C. Hersam, Nano Lett. 2018, 18, 1421.
[17] M. Xu, H. Li, H. Ou, J. Chen, S. Deng, N. Xu, K. Wang, J. Disp. Technol. 2016, 12, 835.
[18] T. Uemura, T. Matsumoto, K. Miyake, M. Uno, S. Ohnishi, T. Kato, M. Katayama, S. Shimamura, M. Hamada, M. J. Kang, K. Takimiya, C. Mitsu, T. Okamoto, J. Takey, Adv. Mater. 2014, 26, 2983.
[19] A. Matsuda, J. Non. Cryst. Solids 2004, 338–340, 1.
[20] K. Kandoussi, C. Simon, N. Coulon, K. Belarbi, T. Mohammed-Brahim, J. Non. Cryst. Solids 2008, 354, 2513.
[21] S. Reynolds, K. Welter, V. Smirnov, Phys. Status Solidi Appl. Mater. Sci. 2019, 216, 1.
[22] R. A. Sporea, S. R. P. Silva, in Proc. Int. Semicond. Conf. CAS, IEEE, Sinaia 2017, pp. 155–158.
[23] L. Wang, Y. Sun, X. Zhang, L. Zhang, S. Zhang, M. Chan, Appl. Phys. Lett. 2017, 110.
[24] R. A. Sporea, K. M. Niang, A. J. Flewitt, S. R. P. Silva, Adv. Mater. 2019, 31.
[25] R. A. Sporea, K. D. G. I. Jayawardena, M. Constantinou, M. Ritchie, A. Brewin, W. Wright, S. R. P. Silva, ECS Trans., 2016, 75, 661.
[26] S. Lee, A. Nathan, Science 2016, 354, 302.
[27] J. M. Shannon, R. A. Sporea, S. Georgakopoulos, M. Shkunov, S. R. P. Silva, IEEE Trans. Electron Devices 2013, 60, 2444.
[28] R. A. Sporea, M. J. Trainor, N. D. Young, J. M. Shannon, S. R. P. Silva, Sci. Rep. 2014, 4, 1.
[29] J. Zhang, J. Wilson, G. Auton, Y. Wang, M. Xu, Q. Xin, A. Song, Proc. Natl. Acad. Sci. 2019, 116, 4843.
[30] A. Valletta, L. Mariucci, M. Rapisarda, G. Fortunato, J. Appl. Phys. 2013, 114, 064501.
[31] A. Valletta, P. Gaucci, L. Mariucci, G. Fortunato, S. D. Brotherton, Appl. Phys. Lett. 2004, 85, 3113.
[32] R. A. Sporea, M. J. Trainor, N. D. Young, J. M. Shannon, S. R. P. Silva, IEEE Trans. Electron Devices 2012, 59, 2180.
[33] Y. Kim, E. K. Lee, J. H. Oh, Adv. Funct. Mater. 2019, 1900650, 1.
[34] R. A. Sporea, M. J. Trainor, N. D. Young, X. Guo, J. M. Shannon, S. R. P. Silva, Solid State Electron. 2011, 65, 246.
[35] E. Bestelink, K. M. Niang, G. Bairaktaris, L. Maiolo, F. Maita, K. Ali, A. J. Flewitt, S. R. P. Silva, R. A. Sporea, IEEE Sens. J. 2020, XX, 1.
[36] S. T. Lee, S. Lim, N. Choi, J. H. Bae, C. H. Kim, S. Lee, D. H. Lee, T. Lee, S. Chung, B. C. Park, J. H. Lee, in Digest of Technical Papers – Symp. on VLSI Technology, Honolulu, HI 2018, pp. 169–170.
[37] H. Tsai, S. Ambrogio, P. Narayanan, R. M. Shelby, C. W. Burr, J. Phys. D. Appl. Phys. 2018, 51, 283001.
[38] R. A. Sporea, M. J. Trainor, N. D. Young, J. M. Shannon, S. R. P. Silva, IEEE Trans. Electron Devices 2010, 57, 2434.
[39] A. S. Dahiya, R. A. Sporea, G. Poulin-Vittrant, D. Alquier, Sci. Rep. 2019, 9, 1.
[40] Y. Kuo, H. Nominanda, Appl. Phys. Lett. 2006, 89, 1.