An embedded gate graphene field effect transistor with natural Al oxidization dielectrics and its application to frequency doubler

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Abstract: A high efficiency frequency doubler is realized based on a single embedded gate (EG) graphene field effect transistor (GFET) with natural Al oxidation dielectrics. Due to elimination of the step of depositing gate dielectrics, the fabrication process of the EG-GFET is improved compared to conventional EG-GFETs. The capacitive efficiency of the EG-GFET is improved up to 80 times compared to the conventional silicon back gate (BG) GFET with 300 nm thick SiO\textsubscript{2}, which is higher than that of most conventional EG-GFETs. Thanks to the high capacitive efficiency, the conversion gain of the frequency doubler is 14 times higher than that of the BG-GFET based frequency doubler.

Keywords: Embedded gate, graphene field effect transistor, natural Al oxidization dielectrics, frequency doubler, high efficiency

Classification: Electron devices, circuits and modules

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1 Introduction

Graphene is a single atomic layer material with the carbon atoms arranged in a honeycomb lattice. It has attracted much attention due to its unique nature such as outstanding carrier mobility, large current densities, thermal and mechanical stability [1, 2, 3]. One of the most promising applications of graphene in electronics is to be used as a channel material for FETs [4]. Unique devices such as frequency doubler and tripler have been realized due to the ambipolar property of graphene [5, 6, 7, 8, 9, 10, 11, 12].

A frequency doubler based on a single BG-GFET was realized for the first time in ref. [5], and more than 90% output power spectrum of the frequency doubler was concentrated at the doubled frequency [5]. However, its conversion gain is very low (less than 1/200) due to the small transconductance of BG-GFETs resulting from its low capacitive efficiency [6]. The capacitive efficiency of the silicon BG structure with 300 nm thick SiO2 is very low (gate capacitance is only 11.6 nF/cm²) [13, 14, 15, 16]. In order to improve capacitive efficiency and enhance conversion gain, usually, a top gate (TG) structure GFET was utilized as a
kernel for frequency doubler [6, 7, 8]. Although some EG-GFET based frequency doublers have been reported, the fabrication process is relatively complex [9].

In reality, the EG structure is a promising candidate for GFETs [17, 18, 19, 20, 21]. Nevertheless, in conventional EG-GFETs, dielectrics must be specially deposited before transferring graphene onto a substrate [17, 18, 19, 20, 21]. Al can be naturally oxidized in air [22, 23], which is used to form dielectrics in TG-GFETs [13, 14, 15, 16, 24, 25, 26]. Similarly, in EG-GFETs, naturally oxidized Al can be also used as dielectrics, which leads to improvement in the fabrication process and capacitive efficiency in comparison with conventional EG-GFETs.

In this paper, an EG-GFET using natural Al oxidation as dielectrics is fabricated. And based on it, a high efficiency frequency doubler is realized.

2 Device Fabrications

For convenience of comparison, the fabrication process of conventional EG-GFETs is shown in Fig.1 [17, 18, 19, 20, 21]. Dielectrics are deposited after defining metal gate. Obviously, the process step of depositing dielectrics is indispensable before transferring graphene onto a substrate.

Now that, thin film Al can be naturally oxidized in air and form an insulating medium [13, 14, 15, 16, 22, 23, 24, 25, 26, 27], the fabrication process of conventional EG-GFETs can be improved, as shown in Fig.2. Namely, Al is used as the pre-defined embedded gate. Thus, both gate electrode and dielectrics are formed after natural oxidation of Al.

Fig.2 illustrates the process flow of the proposed EG-GFET. A 1µm thickness SiO₂ layer is formed after thermal oxidation on a high resistivity Si substrate. A trench with 400 nm depth is formed by reactive ion etching. After 600 nm thick Al
depositing, the sample is polished and exposed in air for 48 hours to form natural Al oxidization dielectrics at a clean room. After monolayer graphene grown by chemical vapor deposition (CVD) transferring on the sample [28], a standard lithographical method is used to define the channel regions of GFETs. Then, the oxygen plasma etching follows. Raman spectroscopy of the CVD grown graphene is used to confirm the monolayer structure, as shown in Fig.3. A metal stack with 3 nm Ti/40 nm Ni is deposited by e-beam evaporation and patterned by liftoff to form the source and drain electrodes. Fig.4 is the optical micrograph of the EG-GFET with natural oxide Al dielectrics. The gate-length (gated channel region) and gate-width are 4 μm and 20 μm respectively. The separation between the source and drain is 10 μm and the total lengths of un-gated channel regions are 6 μm.

Fig.2. Fabrication flow of the EG-GFET with natural oxide Al dielectrics; (a) Reactive ion etching is used to form a deep trench in the SiO₂; (b) Al is deposited and the sample is polished; (c) Al gate is naturally oxidized in air to form natural Al oxidization dielectrics; (d) Graphene is transferred and patterned; (e) Source and drain electrodes are formed by e-beam evaporation and lift-off.

The step shown in Fig.2(c) performs simply, needless of manual intervention, which can simplify fabrication process and save cost. In addition, from Fig.2, in principle, there are following advantages [17, 18, 19, 20, 21]. (1) The pre-defined embedded gate reduces the possibilities of degrading graphene mobility due to eliminating the need of depositing gate dielectrics on graphene and avoiding electron irradiation which could happen in directly e-beam writing on the top of graphene channel. (2) A seed layer that is typically used in conventional TG schemes is eliminated [29]. (3) After being transferred onto a substrate, graphene undergoes fewer Process steps compared to conventional TG schemes, which contributes to reductions of contamination for graphene.
3 Device Characteristics

Fig.5 shows the DC characteristics of the EG-GFET. The devices were measured in a Cascade Probe Station under room temperature. The DC characterizations were done using an Agilent 4155B Semiconductor Parameter Analyzer. The output characteristic curves (Fig.5.a) are obtained with gate voltage swept from 0 to 4 V in 1 V step. Fig.5.b shows the transfer characteristic at $V_{ds}=1V$ with gate voltage varying from 0 to 4 V. The corresponding transconductance curve is also shown in Fig.5.b, which indicates the maximum $g_m$ is 39 $\mu$S/\mu m at $V_{gs}=0.9$ V. We fit the measured data and extract the carrier mobility of the EG-GFET [30]. The effective mobility is up to 2286 cm$^2$/Vs.

![Raman spectra](image)

**Fig.3.** Raman spectra.

![Optical micrograph](image)

**Fig.4.** Optical micrograph of the EG-GFET with 20 $\mu$m scale bar.

![DC characteristics](image)

**Fig.5.** DC characteristics of the EG-GFET. (a) Output characteristic; (b) Transfer characteristic and corresponding transconductance $g_m$. 
The thickness of dielectrics, formed by this natural oxidation process, was confirmed to be about 7–9 nm by spectroscopic ellipsometer [27], which is in agreement with the reported data in ref. [13, 14, 15, 16, 24, 27]. This natural oxidation technique has been already used in the fabrication of GFET with top-gate structure [13, 14, 15, 16, 24, 25, 26], while, it has not been reported in EG-GFETs. The gate capacitance of the EG-GFET is up to 875 nF/cm² [13, 14, 15, 16, 24] and the capacitive efficiency is up to 80 times relative to that of the BG-GFET with 300 nm SiO₂ [13, 14, 15, 16]. It is also higher than that of most conventional EG-GFETs [17, 18, 19, 20, 21]. What is more, the gate dielectric layer can be simply prepared without the step of depositing dielectric process, which simplifies the fabrication process of the EG-GFET.

In order to analyze the insulation properties of natural oxidation Al dielectrics, the gate-leak current is also measured. Fig. 6 shows the $I_{gs}$-$V_{gs}$. The gate current is only 10 pA even at $V_{gs}=4V$, which suggest that the natural oxidation Al dielectric layer exhibits good quality and excellent insulation.

The comparisons of the gate capacitance and formation method of dielectrics are given in the Table I. It can be seen from Table I, the EG-GFET have advantages over the other EG-GFETs.

![Fig.6. $I_{gs}$-$V_{gs}$ curve of the GFET.](image)

| Ref. | Gate structure | Gate capacitance (nF/cm²) | Dielectric material | Formation method |
|------|----------------|---------------------------|---------------------|------------------|
| 5    | BG             | 11.6                      | SiO₂                | Thermal oxidation|
| 17   | EG             | 221                       | Al₂O₃               | ALD              |
| 18   | EG             | 308                       | h-BN                | Exfoliation and transformation |
| 19   | EG             | 363                       | h-BN                | Exfoliation and transformation |
| 20   | EG             | 363                       | h-BN                | Exfoliation and transformation |
| 21   | EG             | 796                       | Al₂O₃               | ALD              |
| This work | EG         | 875                       | Al₂O₃               | Natural oxidation|

**4 GFET Frequency Doubler**

Due to ambipolar property of graphene, a frequency doubler can be readily realized using a single GFET, which is an important device in communication systems and widely used over all major areas of digital and analog
communications, radio astronomy, and terahertz sensing [5, 6, 7, 8, 9, 10, 11, 12].
The circuit schematic and working principle of a frequency doubler based on a
single EG-GFET are shown in Fig. 7.

The “V”-shaped transfer curve indicates that the drain current is based on
hole conduction when $V_{gs}$ is below the minimum conduction point voltage ($V_{g,min}$), while at higher $V_{gs}$, electron conduction dominates. When an input
signal $V_{gs} (V_{gs}=V_{g,dc}+V_{ac})$ is applied on the gate, an output signal whose frequency
is doubled to the $V_{ac}$ is obtained from the drain. Where the DC voltage $V_{g,dc}$ is used
to bias the operating point of the GFET to the Dirac point, an AC sinusoidal signal
$V_{ac} (1/2V_{pp}\sin \omega t)$ is superposed on $V_{g,dc}$.

![Fig.7. Circuit schematic and working principle. (a) Circuit schematic; (b) Working principle of the EG-GFET frequency doubler.](image)

The measured waveforms of the EG-GFET frequency doubler are shown in
Fig.8. In the measurements, the load resistor $R$ is 5 kΩ, the DC bias $V_{g,dc}$ is set 1.25
V and $V_{dd}$ is 1 V.

When a 10 kHz sinusoidal signal $V_{ac}$ with a peak-to-peak value $V_{pp}=600$ mV
and $V_{g,dc}=1.25$ V are applied to the EG-GFET gate, a 20 kHz sinusoidal signal
with a peak-to-peak value of about 44 mV is observed in the output as shown in Fig.8.a.
The frequency doubling is clearly visible.

The conversion gain (output/input voltage amplitude ratio) of the EG-GFET
based frequency doubler is about 1/14. The value is higher than that of the
BG-GFET based frequency doubler (the gain is about 1/200) in ref. [5] and the
TG-GFET based frequency doubler (the gain is about 1/20) in ref. [6]. The high
conversion gain is attributed to the high capacitive efficiency. By the Fourier
transform of the output signal of 20 kHz, the power spectrum is obtained, as shown
in Fig.8.b. Clearly, more than 90% of the output power is concentrated at 20 kHz,
which are results from a combination of the almost symmetric ambipolar
characteristic of the EG-FET and its sublinear behavior near the Dirac point.

From Fig.8.c, d, when a 600 kHz sinusoidal signal $V_{ac}$ with $V_{pp}=800$ mV is
applied to the gate, the frequency doubler functions normally and more than 90%
of the output power is concentrated at 1.2 MHz. The performance of the EG-GFET
is also demonstrated by the frequency doubler.
Discussion
It should be noted that the dominant factor behind the testing results with low working frequency is the restriction of the measurement equipments, while the gate length and the access resistance are the other two key factors. On one hand, the dependence of working frequency of a GFET follows a $1/L_g$ (gate length) relation [31, 32]. On the other hand, the access resistances resulting from un-gated channel regions are one of the important factors that affect the performance of a GFET [33, 34].

As for our frequency doubler, due to the large gate lengths (4 μm) and total lengths (6 μm) of un-gated regions, it is relatively difficult to achieve a high working frequency. Only testing results with low working frequency can be obtained because of the restriction of our current experimental conditions. However, we believe that better testing results will be achieved under more suitable experimental conditions.

Conclusion
An EG-GFET is realized by an improved fabrication process. The naturally oxidized Al is used as a feasible alternative for dielectrics in the novel process. The capacitive efficiency of the EG-GFET has 80 times improvement in comparison with the conventional silicon BG-GFET with 300 nm thick SiO2. Additionally, a
high efficiency frequency doubler based on a single EG-GFET is constructed. The conversion gain of the frequency doubler is increased 14 times compared to the BG-GFET based frequency doubler. In conclusion, the potential of the proposed method for GFET fabrication and its applications is experimentally demonstrate.

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