Simulating nanosecond voltage comparator with improved radiation hardness compatible with PECL logic

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Abstract. The typical voltage comparator circuits are considered. Shown that the use of series-parallel connection of cascades improves the accuracy, speed and hardness to single event transient effects.

1. Introduction
Ultrafast voltage comparators (VC) are widely used to construct parallel analog-to-digital converters (ADC) and also for recording high-frequency signals in nuclear electronics. To improve performance, these VC are compatible with PECL output. To reduce power consumption while maintaining high performance, generally used gated VC with trigger-latch. However, such VC comparisons accuracy is about of 5-10 mV. Two architectures are used to improve the accuracy of comparing the analog signal with a reference:
- with horizontal build-up stages;
- with vertical build-up stages.

The first case increases the switching delay by narrowing the bandwidth. The dynamic range of the input signal is reduced in the second. Commercially available CN compatible with the PECL, typically operate at a supply voltage from 3.3 V to 5 V. In the VC with vertical build-up stages specified supply voltage range is a challenge.

The main purpose of this work is to create a VC with a vertical build-up stages, operating at supply voltages from 3,3 V to 5 V and having an order of magnitude higher than the comparison accuracy with the VC given in Figure 1 and Figure 2.

2. Single stage voltage comparators with trigger-latch
First, [1] of the comparator circuit (Figure 1) is made on a differential stage with a trigger-latch. Using this architecture, most suitable for the ADC having 4-6 digits. However, the use of an emitter follower at the entrance reduces the performance of the VC. The second [2], [3] circuit (Figure 2) is made without the input of the emitter follower, with the bases of trigger-latches are connected to the low impedance emitter follower output bus to enhance the performance. The transient analysis in this configuration allows for a given technology clock frequencies up to 1 GHz. When using emitter follower clock speed is reduced to 500 MHz. The accuracy of the above VC static mode determined VC gain be approximately equal to 20.
Figure 1. Schematic diagram of the single-stage VC with emitter follower output.

Figure 2. Schematic diagram of the VC with improved speed.
3. Voltage comparator with series-parallel switching stages

To ensure the functioning of the VC at the supply voltage from 3,3 V to 5 V a series-parallel cascode including the first and the second stage is used (Fig. 3). Static gain is determined by the following equation:

\[ K_t = \frac{R_{26}}{r_{eQ21}} \times (1 + \frac{R_{37} \gamma}{r_{eQ103}}) \]  \hspace{1cm} (1)

where:

\[ \gamma = \frac{R_{\text{inQ103}}}{R_{\text{inQ103}} + r_{eQ107}} < 1 \]  \hspace{1cm} (2)

It can be shown that in such VC gain factor is about 5-10 times greater than in previous CN. Reducing the switching delay, in this case, is performed by increasing modal current of the second stage in the dynamic mode.

**Figure 3.** Schematic diagram of the VC with series-parallel switching stages.

Basic time characteristics of the two types of VC are shown in Fig. 4.
The sampling frequency is from 200 to 500 MHz and is mainly determined by the frequency of unity gain transistor ($F_t = 5$ GHz). Switching Time - 2 ns. Power dissipation ~ 5-10 mW.

4. **Single event transient impact on the transition process.**

Fig. 4 shows the reaction to the impact of SET of considered VC [4]. For the first comparator (index 1 in Figure 4) the transition process is 3 ns at an amplitude of 0.7 V. For the second - 1.7 ns, and 0.4 V, respectively. Transition process time of SET is reduced due to the increasing modal current of the second stage in the dynamic mode. Increasing the voltage gain influence the degradation of the gain transistor $\beta$ slightly.

5. **Conclusions**

VC with a series-parallel switching stages can increase the sensitivity of the circuit is almost an order of magnitude in comparison with the single-stage circuits CL and reduce the time of transient after SET.

**Acknowledgements**

This work was supported by the Competitiveness Program of NRNU MEPhI.

**References**

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