TDO-CIM: Transparent Detection and Offloading for Computation In-memory

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Abstract—Computation in-memory is a promising non-von Neumann approach aiming at completely diminishing the data transfer to and from the memory subsystem. Although a lot of architectures have been proposed, compiler support for such architectures is still lagging behind. In this paper, we close this gap by proposing an end-to-end compilation flow for in-memory computing based on the LLVM compiler infrastructure. Starting from sequential code, our approach automatically detects, optimizes, and offloads kernels suitable for in-memory acceleration. We demonstrate our compiler tool-flow on the PolyBench/C benchmark suite and evaluate the benefits of our proposed in-memory architecture simulated in Gem5 by comparing it with a state-of-the-art von Neumann architecture.

Index Terms—LLVM, compute in memory, memristor, pattern matching, Polly, Loop Tactics

I. INTRODUCTION

As we are moving toward exascale computing, the memory wall \cite{1} is becoming one of the toughest challenges for the traditional von Neumann architecture. Not only does the cost of moving data dwarf the cost of a floating-point operation but also the memory bandwidth is not able to meet the demand of today’s applications \cite{2}. Consequently, new architectures with a radical departure from the traditional von Neumann architecture start to arise. Computing in-memory (CIM) is one of them. CIM aims at processing information and storing computation data on the same physical unit using emerging devices referred to as memristive devices. Memristive devices such as phase change memory devices (PCM) can store data within their conductance state, which can be changed by altering the amorphous/crystalline phase within the device \cite{3}. Computation, on the other hand, is carried out through various physical mechanisms such as Ohm’s and Kirchhoff’s laws. Memristor devices are organized in a computational memory unit—which we refer to as CIM tile. As storing and processing happen in the same physical device, CIM completely diminishes the overhead of data movement between the CPU and the main memory, enabling data-intensive task in an efficient manner \cite{4}. A huge body of research has been done on the architecture side \cite{5}–\cite{7}. However, before CIM can be established as the de-facto solution for HPC and IoT applications a leap forward need to be done on the compilation toolchain and software stack, which is the purpose of this paper. Our contributions are:

1. An end-to-end compilation flow for CIM devices, which allows to automatically and transparently invoke CIM acceleration, without any user intervention. Therefore, enabling legacy code to exploit in-memory acceleration.
2. A lightweight run-time library for data allocation, transfer and execution of computational tasks on the CIM device.
3. We evaluate the benefits of CIM computation in terms of energy and performance by comparing it with a current state-of-the-art von Neumann architecture using the PolyBench/C benchmark suite.

II. COMPUTE IN MEMORY ARCHITECTURE

In this section, we first briefly discuss the physic behind the PCM device (Section \textsuperscript{II-A}). Afterward, we show how such devices can be interconnected together in a crossbar-like structure (Section \textsuperscript{II-B}) to create the basic block of our accelerator (Section \textsuperscript{II-C}).

A. Memristor Basics

PCM is a type of non-volatile memory that stores information by changing the cell resistance, switching between amorphous and crystalline states. The transition between the two states happens as a consequence of the application of external voltages that exceed the threshold voltage of a device. Figure \textsuperscript{1} (a) shows a cross-section of a PCM device. The phase change material is sandwiched between two electrodes, and current is applied through the heater in order to change the material state. A short, but intense, pulse—known as reset pulse—is used to bring the material in the amorphous phase (high-resistance). Contrarily, to switch back to low resistance the set pulse—a lower and longer pulse—is applied. To read the
device, an even lower pulse (read pulse) is used (Figure 1(b)). Thanks to the excellent scaling capabilities of PCM devices—which allows increasing main memory capacity in a cost-effective and power-efficient way—it is expected that PCM will play a significant role in future memory architectures [8]. But before this can happen, one main challenge needs to be addressed: endurance. PCM devices can stand $10^5$ - $10^8$ writes before they wear out making the lifetime of a PCM-based system last for a few years [9]. Despite a lot of effort on architecture support for wear-leveling and smart algorithms for data re-placement, no prior work tries to address this endurance problem at compile time. TDO-CIM addresses this obstacle by revisiting two common compiler transformations: tiling and fusion (Section II-B).

B. CIM Tile

The electrical conductance/resistance of the PCM depends on the material phase of the device. A single PCM can achieve several resistance levels that can be exploited for in-memory computations [10]. Each resistance level can be used to encode a particular binary value. For instance, a PCM device with $2^M$ levels can support a maximum of $M$-bit computation at full-resolution. To support higher resolutions with a low precision device, multiple columns in a crossbar can be used [11]. Each column in crossbar computes partial results, and the final result is computed by a weighted sum using traditional CMOS technology. Figure 2(c) shows how PCM devices can be organized in a crossbar-like structure to execute matrix-vector multiplication. A matrix can be stored in the crossbar as the conductance state of the PCM device ($G_{x,y}$ values). Afterward, the input vector is fed as a set of voltages to the crossbar, which multiplies by the conductance values. The resulting current sensed at the columns is the analog dot-product result [12]. The output currents are converted back into digital signals by analog to digital converters (ADC). To further improve the energy efficiency, ADCs are shared amongst multiple columns which are reused using sample and holds (S&H) [13]. In addition to the previously mentioned analog components, a digital interface is required to hook the CIM tile (Figure 2 (b)) with traditional CMOS logic. The digital interface is composed of row/column buffers, output buffers, and a digital logic block. The row/column buffers act as a data and mask registers for the crossbar [14]. During write operation, the column buffers contain the data that has to be written on the crossbar, and the row buffers supply a row-enable signal. Similarly, during a compute operation, the column buffers supply column-enable signal and the row buffers latch the inputs. The computed result will be stored in the output buffers. The digital logic block implements scalar compute functionality (i.e., reduction functions) to perform post-processing on the crossbar result.

C. Accelerator Organization

A CIM tile, a micro-engine, and a DMA unit for load and store operations make a standalone accelerator. The core is the CIM tile which computes a standard matrix-vector multiplication (GEMV) of complexity $O(N^2)$ in $O(1)$ constant time. The matrix-matrix computation (GEMM) can be implemented as a series of matrix-vector operations, and therefore the accelerator supports both GEMV and GEMM.

The accelerator uses a shared global memory interface for data sharing and exposes a set of context registers to the system via a memory-mapped IO interface. Context registers are used for control and offloading, and are read or written by the host. The micro-engine translates the high level-parameters stored in the context registers into a series of circuit-level operations such as loading the data from shared memory to row/column buffers, configuring the mask values, triggering the computation on CIM tile, and writing back the results from the output buffers to the shared memory. Additionally, it manages the control flow involved in decomposing GEMM to a series of GEMVs and supports double buffering for all the registers in the accelerator to hide the data latency of the memory accesses. Figure 2(d) shows a timeline of the events that happen after the host trigger the CIM accelerator.

D. Hardware Model

Figure 2(a) shows our emulated system with a host, main memory, and a CIM accelerator connected through a system bus. We implement the CIM accelerator as a cycle-accurate
model integrated into the Gem5 simulator [15]. The accelerator is based on a port-mapped IO (PMIO) and a DMA interface. The PMIO interface exposes context registers to the system, and the DMA provides a memory interface to the accelerator. The host mimics a dual-core Arm-A7 processor based on [16]. For the experiments in the paper, we run the simulator in full-system mode to capture the effects of the operating system, device drivers, and hardware interactions.

E. Software Stack

A software stack (Figure 3) allows applications running in the user space to interact directly with the hardware. The software stack is divided into kernel-space and user-space. At the lowest level of the stack, the kernel-space CIM driver reads and writes to the context registers of the accelerator through a ioctl system call. Besides, the driver translates the virtual address used by the host processor to a physical address as the accelerator can work only with physical addresses. On the other hand, the user-space CIM API is responsible for encoding CIM runtime library calls into context register parameters. Furthermore, with the help of the CIM driver, it implements the support for allocating and releasing the physically-contiguous pages in shared memory via the contiguous memory allocator (CMA) APIs exposed by the Linux kernel [17]. The use of CMA offers two main benefits compared to the traditional malloc-based approach: 1) the size of the shared memory region is not limited by the page boundary; 2) there is no need for explicit memory management in the driver routines, which diminishes overhead in the host.

To enforce memory coherence in the shared memory region, the kernel driver triggers a cache flush on the host side before invoking the accelerator. The accelerator, on its part, uses only un-cachable requests for memory access which automatically enforces memory coherence. Once the accelerator completes its execution, it updates the status in a specific context register. The host can either wait on spinlock or continue with other tasks and check the status of such register periodically.

III. OVERVIEW OF THE CIM COMPILER

The high-level design of our compilation flow is shown in Figure 4. It follows a classical compiler design with a front-end, a mid-level optimizer and targets specific back-ends. We extend this flow by introducing 1) Loop Tactics [18], [19]—a state-of-the-art declarative optimizer—in the mid-level. Loop Tactics enables automatic detection and offload of specific computational patterns; 2) A lightweight runtime library that provides optimized performance and memory usage for the CIM device. The library has been designed to be used directly by the application programmer, or an optimizer (i.e., Loop Tactics). It exposes a host-callable C API, similar to what cuBLAS or MKL offers for Nvidia GPU and Intel CPU, respectively.

A. A Bird's-eye View of TDO-CIM

The entry point in our compilation flow is an application written in a high-level language (i.e., C++). To handle a variety of languages front-ends lower the high-level language to an intermediate representation (IR) on which all the subsequent optimizations are spelled. For our work we use the LLVM compiler infrastructure, hence adopting its intermediate representation LLVM-IR. Given an application, we can use any of the LLVM-based front-ends (i.e., Clang) to lower the high-level language to LLVM-IR. At LLVM-IR level we rely on the polyhedral optimizer Polly [20] to detect, extract and model compute kernels. Internally Polly represents the schedule of each detected kernel as a tree, which we refer to as schedule tree. Schedule tree [21] is the way of representing the execution strategy of each kernel by mapping each dynamic statement instance with its execution order. This mapping is implicitly defined by the node parent-child relation within the tree. Loop optimizations and device mapping are expressed as tree modifications and carried out by Loop Tactics, which works as additional passes within Polly. Loop Tactics’ passes consume schedule trees and output a CIM-optimized schedule. The modified tree is then passed back to Polly which lowers it back to an imperative AST and then further down to LLVM-IR. In the back-end LLVM-IR is lowered to final executable. It is at this stage of the compilation pipeline where we link our executable with the CIM runtime library. Listing 4 shows at the top a GEMM kernel in C++ code, while at the bottom the mid-level optimizer output as pseudo-C++. For our example, we assume single-precision operands. The GEMM kernel has been detected and swapped by Loop Tactics with a function call to the CIM runtime library (polly_cimBlasSGemm). Blas parameters (i.e., values of alpha or leading dimensions) are automatically collected or computed by Loop Tactics. In addition, Loop Tactics inserts an initialization call to configure the CIM hardware (polly_cimInit) as well as all the function calls to orchestrate the data movement to and from the device (i.e., polly_cimMalloc and polly_cimDevToHost).

```c
for (int i = 0; i < M; ++i)
    for (int j = 0; j < N; ++j) {  
        C[i][j] = beta * C[i][j];
        for (int k = 0; k < K; ++k)
            C[i][j] += alpha * A[i][k] * B[k][j];
    }
/* ... */
// initialize CIM device 0
polly_cimInit(0);
```
Loop Tactics passes
LLVM-IR Tree Matcher
CIM Optimized
LLVM-IR Tree Builder
C++/C
Clang
Host backend
Assembler
Linker
CIM Runtime Library
Executable
Back-end

Fig. 4. LLVM-based compilation flow developed for the CIM accelerator.

```
// allocate data on CIM device
polly_cimMalloc((void**)&cim_C, M*N*4);
polly_cimMalloc((void**)&cim_A, M*K*4);
polly_cimMalloc((void**)&cim_B, K*N*4);

// execute GEMM kernel on CIM device
polly_cimBlasSGemm(transA, transB, M, N, K,
&alpha, cim_A, lda, cim_B, ldb,
&beta, cim_C, ldc);
// copy C back to host
polly_cimDevToHost(cim_C, host_C, M*N*4);
```

Listing 1. High-level code for a generalize matrix multiplication (GEMM) kernel (top). Loop Tactics generated code to offload GEMM kernel to the CIM accelerator (bottom).

B. TDO-CIM specific optimizations

We revisit loop fusion and tiling in the light of this new CIM computing paradigm trying to minimize write operations to crossbar to enhance endurance.

Revisited Loop Fusion: Loop fusion is a performance-oriented transformation that combines two loop nests in a new single-loop nest. In our case, we focus on a specific case of loop fusion: kernel fusion. Consider two consecutive kernels X and Y, with Y following X directly. We fuse X and Y if both kernels have the same access patterns (i.e., both are GEMM kernels) and are independent. Two kernels are independent if Y doesn’t read from or write to any output of X, and Y does not write to any input of X. An example is shown in Listing 2.

```
for (int i = 0; i < M; ++i)
  for (int j = 0; j < N; ++j) {
    for (int k = 0; k < K; ++k)
      s1: C[i][j] += @A[i][k]@ * B[k][j];
  }

for (int i = 0; i < M; ++i)
  for (int j = 0; j < N; ++j) {
    for (int k = 0; k < K; ++k)
      s2: D[i][j] += @A[i][k]@ * E[k][j];
```

Listing 2. Independent kernels with shared input (A matrix). TDO-CIM exploits shared inputs to increase endurance by avoiding multiple writes on the memristor crossbar.

By fusing two kernels, we get the following advantages: 1) we reduce the number of calls to the runtime library by using batched operations. The GEMMs in Listing 2 will be replaced by a single `polly_cimBlasGemmBatched` instead of two calls to `polly_cimBlasSGemm`. The interface for the batched operation is similar to the one provided for `polly_cimBlasSGemm` with the only exception of having arrays of pointers instead of single pointers. 2) We increase endurance by exploiting possible shared inputs. The A matrix (Listing 2) is shared and remains constant; we exploit this by writing only A in the crossbar and streaming B and E from the input buffers. This allows writing only one matrix on the crossbar in contrast with a naive mapping where B end E would have been written, and A streamed from the input buffers. Figure 5 shows the expected lifetime for the PCM crossbar comparing the naive mapping and the “smart” mapping applied by TDO-CIM. The x-axis shows the PCM cell endurance in an interval between 10 million to 40 million writes which is in the expected lifetime interval of a PCM device ($10^6$ to $10^8$). The expected lifetime is computed by applying the following equation [9]:

$$\text{SystemLifeTime} = \frac{\text{CellEndurance} \times S}{B}$$

where $S$ is the crossbar size, 512 KB in our case, while $B$ is the write traffic in GB/s for the kernel in Listing 2. $B$ is obtained by dividing the total number of writes by the kernel execution time. We assume squared matrices of 4096 byte-elements and the writes to be localized uniformly across the entire crossbar. As can be seen from Figure 5 the “smart” mapping allows to improve endurance by a factor of 2.

Revisited Tiling Transformation: Let us now focus on our revisited tiling optimization. Tiling is a well-known transformation to improve locality by reducing the reuse distance of memory accesses to the same location. Consider statement s1 in Listing 2 and assume that matrix A doesn’t fit in the CIM crossbar. We use tiling to split A into multiple tiles such that the working set of a single tile fits in the CIM...
crossbar. We then apply loop interchange on the tile loops \(jj\) and \(kk\) such that we can reuse tiles of A in consecutive executions of the point loops, hence once more increasing endurance. The outcome of our tiling transformation is shown in Listing 3 where the point loops will be replaced by a call to `polly_cimBlassGemm`.

Listing 3. Loop tiling and interchange to fit the operand on the CIM crossbar and reduce the number of writes by reusing A tiles in consecutive execution of the point loops.

```c
// tile loops
for (int ii = 0; ii < SIZE; ii += TILE)
    for (int kk = 0; kk < SIZE; kk += TILE)
        for (int jj = 0; jj < SIZE; jj += TILE)
            // point loops
            for (int jj = jj; jj < jj + TILE; jj++)
                for (int kk = kk; kk < kk + TILE; kk++)
                    C[i][j] += A[i][k] * B[k][j];
```

IV. DEMONSTRATION AND EVALUATION

In this section, we quantify the benefits of CIM computation for a set of linear-algebra kernels from the Polybench/C benchmark suite compiled with TDO-CIM.

a) Experimental Setup: We use the system shown in Figure 2 (a). We select an energy efficient dual-core Arm-A7 with a shared L2 cache. The simulator is a cycle-accurate model that imitates the functionality of the memristor computations and surrounding digital blocks [14]. The memristor crossbar is an 8-bit 256x256 PCM crossbar based on IBM’s 4-bit PCM [4]. To mimic an 8-bit cell with a 4-bit cell, two adjacent columns are used, one for 4 MSBs and the other for 4 LSBs. The final result is computed by a weighted sum of MSB and LSB columns in the digital logic block. The energy and latency model for the crossbar and mixed-signal circuitry is from [4] and [13] respectively. The energy model for the rest of the digital blocks is based on a synthesis report of commercial 40nm finFET technology. Table II summarises our system configuration and energy model.

b) Performance Evaluation: We use the compilation string shown in footnote 2 for the host and the host+CIM, respectively. Dynamic instruction count and run-time are profiled in Gem5 by inserting ROI markers. For energy estimates, we use the numbers shown in Table I. We do not include DRAM energy numbers in the estimates as the host and CIM-accelerator generate the same amount of traffic by accessing the same data. Figure 6 (left) shows the energy numbers obtained for the reference platform (Arm-A7), and for the Arm-A7+CIM where the kernel execution is performed on the in-memory accelerator. For the host, the energy numbers include the energy spent on computation and in the memory hierarchy. For the CIM, the energy numbers incorporate the energy spent on the driver (host side) and in the accelerator. GEMM-like kernels: 2mm, 3mm, gemm, and `conv` were able to achieve good energy improvements over the reference system. This is not the case for GEMV-like kernels (bicg, mvt, gesummv) due to their low compute intensity. From the CIM perspective, the compute intensity for a given kernel can be formulated as \(\frac{\text{Number of MAC operations}}{\text{Number of CIM writes}}\) which is very low for GEMV-like kernels as can be seen in Figure 6 (left). With such low compute intensity the energy is dominated by the overhead in host for offloading computations to accelerator and the number of writes which are costly for the CIM device 200pJ/byte (see Table I). Figure 6 (right) shows the energy-delay-product (EDP). It follows the same trend as the energy plot. We gain for GEMM-like kernels (up to 612x) while we lose for GEMV-like.

V. RELATED WORK

Code offloading: Several works address the issue, TOM [22] being perhaps the very first of them. TOM proposes an offloading decision based on a simple cost function. The idea is to statically identify the code section with the highest potential in bandwidth saving. Similarly, Pattanik et. al. propose an affinity prediction model based on memory-related metrics to decide where a given kernel should be executed (i.e., main CPU or in-memory accelerator) [25]. Previously mentioned works target GPU as an in-memory accelerator. On the other hand, in our case, we are targeting a memristor crossbar which means that only specific kernels must be offloaded as the accelerator is capable of executing only GEMM and GEMVs-like kernels. Nair et. al. propose a code offloading based on OpenMP 4.0 user annotation [24]. Contrary, our approach is completely transparent to the application and does not require any user intervention to exploit CIM acceleration. CAIRO relies on an LLC cache profiler and analytical models to decide potential offloading candidates [25]. The LLC profiler is not integrated into the compilation flow and requires to characterize the behavior of each kernel offline. Other works expose CIM acceleration via API [6], [7], which requires significant changes in the application, reducing application readiness, and hurdlng widespread adoption.

Enhance PCM endurance: Software and hardware wear-leveling techniques to distribute write operations uniformly across the memory module have been studied extensively. Hardware techniques require additional storage tables to keep track of heavily written blocks, that will be periodically get...
remapped to the lowest wear-out ones [9]. Software techniques, on the other hand, rely on lazy write-back policy [9], dynamic data management [26], data migration and recomputation [27]. All previous approaches are orthogonal to TDO-CIM, which tries to enhance endurance at compile time by intelligently mapping array references to the CIM crossbar.

VI. CONCLUSION

We present an end-to-end compilation flow for in-memory computing. Our approach automatically identifies, optimizes, and offloads computing kernels to our in-memory accelerator. We compile a set of linear-algebra kernels from the Polybench/C benchmark suite and prove the benefits of in-memory computation by comparing our in-memory architecture simulated in Gem5 with a state-of-the-art von Neumann architecture. The results show the benefits of in-memory computing by achieving average energy reduction of 32.6x and energy-delay-product improvement of 612x. We expect our compiler and Gem5 emulator to boost researches in the field by providing a transparent and automatic flow to compile entire applications on the CIM architecture and perform domainspace exploration by tweaking our simulator.

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