Recent Advances of Volatile Memristors: Devices, Mechanisms, and Applications

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Due to the rapid development of artificial intelligence (AI) and internet of things (IoTs), neuromorphic computing and hardware security are becoming more and more important. The volatile memristors, which feature spontaneous decay of device conductance, own the distinct combination of high similarity to the biological neurons and synapses and unique physical mechanisms. They are excellent candidates for mimicking the synaptic functions and ideal randomness source of the entropy for hardware-based security. Herein, the recent advances of volatile memristors in devices, mechanisms, and application aspects are summarized. First, a brief introduction is presented to describe the switching type, materials, and temporal response of volatile memristors. Second, the volatile switching mechanisms are discussed and grouped into ion effects, thermal effects, and electrical effects. Third, attention is focused on the applications of volatile memristors for access devices, neuromorphic computing (artificial neurons and synapses), and hardware security (true random number generators and physical unclonable functions). Finally, major challenges and future outlook of volatile memristors for neuromorphic computing and hardware security are discussed.

1. Introduction

With the explosive growth of data, the information processing and storage capacity of integrated circuit (IC) chips have been put forward higher requirements.[1–3] Powered by Moore’s law, the number of transistors in the chips doubles in 18 months and the performance of mainstream computers based on complementary metal oxide semiconductor (CMOS) technology has been greatly enhanced over the past few decades.[6–9] However, the state-of-the-art and the most mature semiconductor technology is facing the challenges in high-resolution fabrication and power consumption when the feature size is reduced to the 10 nm range. To continue the rapid development of ICs industry, more and more efforts have been devoted to developing novel device concepts and architectures.

One of the most promising candidates is the memristor (short for memory resistor), which establishes direct relation between the magnetic flux ($\varphi$) and charge ($q$). Memristors were proposed by Chua in 1971 as the fourth elemental circuit component.[10] In 2008, the first physical implementation of memristor was experimentally demonstrated by Strukov et al. in the Hewlett-Packard (HP) laboratories.[11] In general, the single memristor cell has a capacitor-like architecture, which is composed of an active layer sandwiched between two conductive electrodes (as shown in Figure 1b). Due to the simple structure, the memristors can be easily integrated in the crossbar array (Figure 1a) with a small area of $4F^2$ ($F$ is the minimum feature size) and vertically stacked in 3D structure.[12] In addition, the good compatibility with the existing CMOS process allows the memristors to develop rapidly. The recent reported memristors show attractive properties, such as high ON/OFF ratio, low power consumption, fast switching speed, and high endurance.

According to the retention time of the low resistance state (LRS), memristors can be divided into volatile and nonvolatile types. As for nonvolatile memristors, both high resistance state (HRS) and LRS can be maintained after the removal of voltage bias. Nevertheless, the volatile memristors would spontaneously return back to HRS from LRS after the removal of external excitation in milliseconds to nanoseconds. Such dynamics of the conductance change is closely related to the ion migration, thermal...
effects, and electronic effects, which could be modulated by external voltage amplitude, pulse width, ambient temperature, and so on. The unique delay and relaxation temporal responses of volatile resistance switching phenomena make the volatile memristors suitable for diverse applications in electronics, which contain the access devices for the memory, neural/synaptic components for neuromorphic computing, and randomness sources for hardware security.

Since the rapid development of volatile memristors, a comprehensive review that contains the recent progress of volatile memristors is urgently needed. In this progress report, we review the recently advances of volatile memristors in devices, mechanisms, and applications aspects. In Section 2, we give a brief introduction of volatile memristors in materials, switching types, and temporal response. We have summarized the wide accepted mechanisms of volatile switching behaviors in Section 3. The applications of volatile memristors in selectors, neuromorphic computing, and hardware security are discussed in detail in Section 4. In the last section, the challenges and the future outlook of volatile memristors are presented.

2. Volatile Memristor

2.1. Volatile Switching Type

Generally speaking, volatile memristors can be divided into digital switching (threshold switching [TS]) and analog switching types. The digital-type volatile memristor is characterized by an abrupt current/resistance switching with a large ON/OFF ratio. As shown in Figure 1c, the current of volatile memristor sharply increases when the applied voltage surpasses the threshold voltage ($V_{\text{th}}$). When the applied voltage is smaller than the hold voltage ($V_{\text{hold}}$), the current of volatile memristor decreases abruptly. In addition, the TS can occur in a short time (as low as nanoseconds) and own a large ON/OFF ratio, which promises high speed accessing operation. With the benefits of fast speed, high ON/OFF ratio, and good scalability, the digital switching-type volatile memristor is regarded as a good candidate for the access device and combinational logic circuit.

On the contrary, volatile memristors with analog-type switching behaviors, featuring continuous and incremental changes in device conductance with a relatively lower ON/OFF ratio (Figure 1d), are attractive in the neuromorphic computing and synaptic mimicking. Compared with the digital-type volatile memristor, volatile memristors with analog switching behaviors are more suitable for exploiting artificial neurons and synapses for implementing neuromorphic computing.

2.2. Materials

There is no discernible difference between the volatile and nonvolatile memristors on the device structure and material system level. Volatile switching and nonvolatile switching behaviors can even coexist and interconvert in the same device with appropriate conditions. A great number of materials have been explored as active layer and electrodes for volatile memristors in the past few decades (see Table 1). The active layer materials

Figure 1. a) Schematic of the vertical memristor array. b) Schematic of single cell in the memristor array, which consisted of two electrodes and an active layer. Current–Voltage curves schematic of c) digital/TS-type volatile memristor; d) analog switching-type volatile memristor.
can be roughly grouped into oxides (such as SiO$_2$\cite{17,21}, HfO$_2$\cite{18,23}, TiO$_2$\cite{19}, ZnO \cite{20}, CuO \cite{14}, CoO \cite{22}, ZrO$_2$ \cite{24}, NbO$_2$ \cite{25}, and VO$_2$ \cite{26}), 2D materials (e.g., h-BN \cite{13}, WS$_2$ \cite{16}, MoS$_2$ \cite{27}, and MoS$_2$/graphene \cite{35}), perovskites (e.g., Cs$_3$Sb$_2$Br$_9$ \cite{30}), and other materials (such as AsTeSi \cite{29}, GeTe \cite{30}, and GeTe$_8$ \cite{28}), and others (e.g., PEDOT:PSS \cite{14}, ferritin \cite{31}).

In the switching process, electrodes not only serve as transport terminals for carriers, but also affect the volatile switching phenomemn of specific storage media. So far, large amounts of materials have been reported as electrodes for volatile memristors. We grouped the common electrode materials into four categories based on composition of electrodes, including pure metal electrodes such as Au \cite{13,16}, Cu \cite{21}, Pt \cite{18}, W \cite{34}, and Ti \cite{20} nitride-based electrodes such as TiN \cite{23,30}, conductive oxide-based electrodes such as ITO \cite{22,33}, and semiconductor electrodes such as Si \cite{23} and so on.

Table 1. Summary of the recent reported material systems showing volatile switching behaviors and corresponding switching characteristics. The symbol “–” means that no data concerning that characteristic is found.

| Device | Switching type | Threshold voltage | Hold voltage | ON/OFF ratio | Delay time | Relaxation time | Cycle | Ref. |
|--------|----------------|-------------------|--------------|--------------|------------|----------------|-------|------|
| Pt/Ag/SiO$_2$/Ag/Pt | Threshold switching | 0.5 V | 0.3 V | >10$^4$ | 130 μs (0.5 V) | 100 μs (0.5 V, 1 ms) | 10$^7$ | [17] |
| Pt/HfO$_2$/Ag/Pt | Threshold switching | 0.3–0.1 V | 0.1–0.03 V | >10$^6$ | 100 ns (1.5 V) | 240 ns (1.5 V, 1 μs) | >10$^5$ | [18] |
| Ag/TiO$_2$/Pt | Threshold switching | 0.3 V | 0 V | >10$^7$ | 35 μs (1 V) | – | – | [19] |
| Au/Ti/GdO/Ti/Au | Threshold switching | ≈2.8 V | ≈1.4 V | >10$^6$ | – | – | >10$^5$ | [14] |
| Pt/ZnO/Ag/Ti/PET | Threshold switching | 0.4–0.5 V | 0–0.1 V | ≈10$^7$ | 100 ns (1 V) | 1 s (1 V, 300 ms) | >100 | [20] |
| Cu/SeO$_2$/Pt | Threshold switching | ≈0.7 V | 0 V | >10$^7$ | 4 μs (1.2 V) | 1 ms (1.2 V, 10 μs) | >50 | [21] |
| Pt/CoO/ITO | Threshold switching | ≈2.5–2.5 V | ≈1–1 V | ≈10$^2$ | 50 ns (6 V) | ≈40 ns (6 V, 500 ns) | >10$^3$ | [22] |
| Pt/HfO$_2$/TiN | Threshold switching | ≈5 V | ≈4.5 V | ≈10$^2$ | 80 μs (7.5 V) | ≈800 μs (7.5 V) | – | [23] |
| Ag/GeO$_2$/Pt | Threshold switching | 0.15–0.15 V | 0 V | >10$^6$ | – | – | >200 | [24] |
| Si/NbO$_2$/TiN | Threshold switching | ≈1.7–1.8 V | ≈1.5–1.6 V | ≈90 | – | – | >100 | [25] |
| Pt/TiO$_2$/Pt | Threshold switching | ≈1.2 V | ≈0.4 V | ≈160 | – | – | >2.5 × 10$^4$ | [26] |
| Au/Ti/h-BN/Au (150 nm × 200 nm) | Threshold switching | 4.5 V | 1.5 V | >10$^6$ | 7 μs (0.7 V) | ≈144.21 μs | >500 | [13] |
| Ag/Mo$_2$N$_2$/Au | Threshold switching | ≈0.35 V | ≈0.1 V | 10$^6$ | – | – | >5 × 10$^6$ | [27] |
| Ag/WS$_2$/Ag | Threshold switching | 0.3–0.6 V | <0.1 V | ≈70 | 700 ns (0.7 V) | ≈300 ns (0.7 V, 1 μs) | >90 | [16] |
| Au/TiN/Ag/GeTe$_2$/Ag/TiN/W | Threshold switching | ≈2.4–2.4 V | 0.5–0.2 V | ≈10$^8$ | 110 ns (5 V) | 240 ns (5 V, 1 μs) | >10$^5$ | [28] |
| Pt/AsTeSi/Pt | Threshold switching | ≈2.5–2.8 V | ≈1.5–1.8 V | >10$^2$ | 20 ns (4 V) | – | >100 | [29] |
| TiN/GeTe$_2$/TiN | Threshold switching | ≈1.8–1.9 V | ≈1–1 V | ≈10$^5$ | – | – | >100 | [30] |
| Pt/ferritin/Pt | Threshold switching | ≈0.7 V | ≈0.5 V | >10$^4$ | 0.7 μs (1 V) | – | – | [31] |
| Au/Co$_3$Sb$_2$Te$_6$/Au | Threshold switching | 2.5–2.5 V | 0.6–0.5 V | >10$^6$ | 0.6 s (6 V, 1 ms) | – | >200 | [32] |
| Au/Co$_3$Sb$_2$Te$_6$/Au | Analog switching | – | – | >10$^2$ | – | – | – | [33] |
| W/VO$_2$/PEDOT:PSS/Pt | Analog switching | – | – | >10$^2$ | – | – | – | [34] |

2.3. Temporal Response

The temporal responses of the volatile memristors can be obtained by measuring the current in time domain with external voltage pulses. As shown in Figure 2a, the resistance of memristor would switch from HRS to LRS within certain time duration (delay time) under the external voltage pulse. When the voltage bias is removed, it takes a certain amount of time for the resistance to return to its original value, known as the relaxation time or retention time. As the material (such as spices and morphology) and device configuration can greatly affect the switching behavior of a single device, the summarized delay time and relaxation time of different devices show large variances (as shown in Table 1). Apart from the effect of device itself, several other external factors can tune the temporal response of memristors such as ambient temperature, voltage amplitude, and pulse width.

As for the delay time, it is found that both voltage amplitude and ambient temperature are the critical influences. Some cases show that the delay time will decrease with the increase in voltage amplitude or the ambient temperature. As shown in Figure 2b,c, Yoo et al. found the exponential correlation between the delay time ($\tau_d$) and voltage amplitude/temperature in the Ag/HfO$_2$/Pt and Ag/TiO$_2$/Pt volatile memristors.\cite{19} The data of delay time could be fitted by Equation (1)

$$\tau_d = \tau_0 e^{\alpha E_0 d / kT}$$

where $\tau_0$ is the nucleation barrier energy at zero-field, $\alpha$ is a geometric factor, $E_0$ is the voltage acceleration factor, $d$ is the thickness of device, $T$ is the ambient temperature, and $V$ is the applied voltage. The similar results were also reported by others.\cite{17,38} 

In addition to the ambient temperature and the amplitude of voltage pulse, the width of pulse could also affect the relaxation time. Midya et al. observed that the relaxation time of
Pd/Ag/HfO$_x$/Ag/Pd volatile memristor was exponential with the reciprocal temperature. When the temperature increased, the relaxation time of the device would decrease with a constant voltage amplitude and pulse width (Figure 2d). In addition, Wang et al. reported the impact of applied voltage on relaxation time in the Pt/SiO$_x$N$_y$:Ag/Pt device. Higher voltage amplitude or longer pulse duration time could contribute to the formation of conductive filaments which became more difficult to rupture, leading to a longer relaxation time (Figure 2e,f).

### 3. The Switching Mechanism of Volatile Memristors

So far, there are various devices which have been reported with the volatile switching behaviors. However, as significant as the continual exploration of novel material systems, investigating the switching mechanisms and building the abstract models play fundamental and key roles for the prediction and improvement of device performance. During the past few years, the study on volatile memristor has made great progresses in the understanding of the switching mechanisms. In addition, many mechanisms have been put forward to explain the causes of volatile switching behaviors. As disputes still remain in some cases and mechanisms may function together in the same devices, we roughly divide the reported devices into three types based on their main switching effects.

#### 3.1. Ionic Effects

In many cases, the localized conduction channels in the devices are formed as a result of ion-related migration and redox processes. One big branch of the ionic effects is the migration of the active metal ions. Facilitated by the external electric field, the active electrode materials (such as Ag or Cu) will be oxidized ($X \rightarrow X^{n+} + n^{-}$) and the generated cations will migrate toward the inert electrode and be reduced ($X^{n+} + n^{-} \rightarrow X$), resulting in the formation and spontaneous rupture of conductive filaments in volatile memristors.

In 2014, a direct observation of a disconnected Ag filament for TS was reported by Sun et al. on a planar Ag/SiO$_x$/Pt device. The scanning electron microscope (SEM) image of operated device under a compliance current of 5 nA showed some isolated nanoparticles in the interelectrode area. With a larger compliance current (100 nA), the number of the nanoparticles increased and nanocrystal area widened. The high-resolution transmission electron microscopy (HRTEM) and electron energy loss spectroscopy (EELS) were used for investigating the structure and component of the nanoparticle, and the results revealed that the conductive filament was composed of Ag (Figure 3a–d). Furthermore, the I–V fitting of two switching regions and Kelvin probe force microscope (KPFM) characterization results indicated that the tunneling barrier modulation between discrete Ag nanocrystals played a key role in the switching process.

In 2017, Midya et al. reported a microscopic analysis of the switching behavior based on vertical Pd/Ag/HfO$_x$/Ag/Pd
Compared with the pristine device, the Ag profile of energy-dispersive spectroscopy (EDS) elemental mapping in the electrically operated device was snatchy. It was probably related to the Ag migration in the interlayer and electrodes during the operation. The EDS line scan results of the Ag peak further verified this hypothesis.

Later, Chae et al. used the in situ probing TEM technique to analyze the underlying switching mechanism in the Ag/TiO2/Pt devices. To overcome the shortcomings of the TEM technique in the nanosized conductive filaments in situ characterization, Chae et al. combined in situ TEM technique with the atom probe tomography (APT) method. The bright-field TEM images of anatase TiO2 conductive filaments (CFs) in memory switching (MS) and TS are shown in Figure 3e–h. Although the CFs showed the inverted triangle shape in both modes, a lower base-to-height ratio of CFs was observed in the TS mode. Compared with the MS mode, the area near the interface of between the oxide and Pt electrode showed the disappearance of crystalline structure in the TS mode, which provided a direct observation of the spontaneous relaxation to the initial HRS.

In addition to the volatile memristors based on the migration of active metal cations, another major branch of the ionic effects is the migration of the movable ions in the interlayer material. Yang et al. reported a diffusive memristor of Au/MAPbI3/ITO. With the increased applied voltage, the ions or vacancies in the interlayer would be drifted and accumulated near the interface of material and electrodes, resulting in self n-doping and self p-doping, respectively (as shown in Figure 3i). Because of the self-doping effects, the surface work functions of the perovskite would change, which decreased the Schottky barrier and improved the carrier injection efficiency. When the electric field vanished, the ions would return back to their initial position and the device switched off. In addition, the in situ KPFM was introduced to investigate the doping effect in the perovskite layer. Under a big positive voltage stress, the surface potential decreased gradually from anode side to cathode side, which was matched well with the self-doping effect (Figure 3j–l).

A lead-free monocristalline perovskite (Cs3Sb2Br9) volatile memristor was proposed by Mao et al. An extremely low electrical field of 2.2 \times 10^5 V m^{-1} was needed for TS behavior of the device with two inert Au electrodes in this work. In the volatile memristors, the electric field is defined as”.

Figure 3. a) The SEM image of planar structure Ag/SiO2/Pt device without any operation. b–d) The SEM image of Ag/SiO2/Pt with different compliance current (5 nA, 100 nA, 100 μA). Parts (a–d): Reproduced with permission. Copyright 2014, Wiley-VCH. e) Memory switching characteristics of Ag/amorphous TiO2/Pt device. f) The TEM image of CF in the memristor with a MS. g) The TS characteristics of Ag/amorphous TiO2/Pt device. h) The TEM image of CF in the memristor with a TS behavior. Parts (e–h): Reproduced with permission. Copyright 2017, Wiley-VCH. i) Schematic of the underlying switching mechanism to account for I–V characteristics of the Au/MAPbI3/ITO memristor. j–l) The KPFM potential mappings of MAPbI3 film and the contact potential before/after applying the tip bias. Parts (j–l): Reproduced with permission. Copyright 2020, Elsevier.
could not provide sufficient activation energy for the removal of Cs and Sb from the original lattice structure. The density functional theory (DFT) calculation result showed that Br vacancies ($V_{Br}$s) in the material could migrate with low activation energy of 0.22 eV. To further confirm the migration of $V_{Br}$s, EDS characterizations on perovskite nanoflakes were conducted to analyze the switching behavior. The element intensity of Br decreased along the direction of applied electric field; however, the element intensities of Sb and Cs remained nearly constant through the perovskite nanoflake, which clearly verified that Br ions or vacancies served as a key role in the switching process.

3.2. Thermal Effects

With the application of the external electric field, the current through the devices will inevitably generate Joule heating. When accumulated Joule heating exceeds a certain value, the thermal effects would lead to the rupture of the formed filament and even change the structure of materials, leading to the switching behavior.

The TS behaviors in the Mott materials (such as NbO$_2$ or VO$_2$) are always attributed to the Joule heating-induced reversible transformation (from insulator to metal phase). Pickett et al. reported a Mott memristor, in which the Mott material sandwiched between two platinum electrodes.[40] When large enough current flows through the device and the temperature of the Mott material surpasses its transition value, a conductive path in the device would be induced after the insulator to metal phase transition. The formation of the metal phase will disappear after the removal of external bias, thus the memristors return back to the HRS.

In the amorphous chalcogenide material system, the transition from amorphous phase to the crystalline phase demanded a large enough current and sufficient Joule heating. Because of the significant thermal energy, the switching behavior was described as a thermal breakdown effect in the films.[41] In 2007, Ielmini et al. explained the switching effects in amorphous chalcogenide-based devices with thermal-assisted Poole–Frenkel (PF) conduction. They assumed a nonequilibrium carrier distribution and nonuniformity of electric field in the film.[42] In 2018, Goodwill et al. explained that the whole TS process by Joule heating with thermal runaway caused fast transition. There was a positive feedback loop between device conductance and temperature in the model, and the positive feedback effects would result in a thermal runaway.[43]

The thermal dissipation through the electrode also can influence the switching behavior. In 2008, Chang et al. found that the bottom electrode (BE) thickness of Pt/NiO/Pt played a key role in the device resistance switching behaviors.[44] In their work, when the thickness of BE ($t_{BE}$) was smaller than 30 nm, the switching behavior of devices changed from resistive switching to TS. They conducted a 3D heat flow calculation using Fourier equation to verify the $t_{BE}$-dependent thermal dissipation effects. The heat dissipation would decrease with a thinner BE, so that the conductive filaments in the device would be more easily ruptured.

3.3. Electronic Mechanisms

In 1980, Adler et al. explained that the TS behavior in chalcogenide glass thin films as a pure electronic phenomenon.[45] In the proposed model, the chalcogenide glass materials were considered as homogeneously doped semiconductor materials with single trap and doping level close to conduction or valence band. When all the charged traps in the films were filled by the field-induced carriers during the delay time, the mobility of carriers in the material could be enhanced and the transition to ON state happened. When the recombinant of carriers dominated the switching process, the transition to OFF state happened. The switching mechanism was related to the Shockley Hall Reed (SHR) recombination through trap levels and the generation mechanism driven by electric field and carrier density.

In 2008, for accounting the TS process in the chalcogenide glasses, Ielmini explained the mechanism by energy gain of carriers in their hopping transport, modified by the phonon–electron interaction caused energy relaxation process.[46] The application of external electric field resulted in an energy gain of carriers, so a nonequilibrium carrier distribution in the amorphous semiconductor was formed. The energy gain would enhance the hopping rate of the localized carriers. However, the carrier mobility in the crystalline semiconductor was related to the scattering rate. Because of the phonon and impact ionization scattering, the scattering rate increased with an extra energy gain, which decreased the carrier ability. The TS was based on the interaction of the energy gain in hopping transport and energy loss by the scattering effects.

Woo et al. explained the switching mechanism of Pt/HfO$_2$/TiN device with the effects of the trap levels in the HfO$_2$ layer and the internal electric field, caused by the work function difference of two electrodes.[23] When an external voltage was applied on the device, the trap level of the interlayer was pulled down below the Fermi level of BE. The carriers were injected into the interlayer and captured by the trap level, resulting in the enhancement of the memristor conductance. When the external voltage was removed, those carriers would be easily released.

4. Applications

4.1. Volatile Memristor as Access Device

The passive array, with no series transistors or selectors, is very attractive for the low power consumption and high-density integration. However, the passive array suffers from the sneak path current and half-select issues during the writing operation or even the read process. Although the sneak path current can be served as the physical randomness for realizing physical unclonable function (PUF) device,[47] for the information storage, and neuromorphic computing applications, the disturbance would reduce the read accuracy, computation speed, and increase power consumption of storage and computing processes.[48] In addition, with the number of the memory cells increases, the leakage current is more severe, which hinder the large-scale circuit integration. So far, the most practical way to suppress the sneak path current and realize a large memristor array is to integrate memristors with MOS transistors (one-transistor-one-resistance switch, 1T1R).[49] The maturity of CMOS technology makes the fabrication of 1T1R array feasible, and the extra terminal (gate) can control the current to memristor, realizing the precise conductance modulation. However,
combining the three-terminal MOS transistors with two-terminal memristors would deprive the scaling merit of the latter and increase the footprint of layout. Another approach for mitigating the sneak path current is connecting the two-terminal selector devices with each cell (1S1R configuration). In this configuration, two-terminal volatile memristor devices act as the access device and can be stacked on the top of nonvolatile memristors, resulting in a less layout footprint and smaller layout area than 1T1R. Nevertheless, as a two-terminal device, volatile memristor cannot precisely control the current through the series device and merely perform the role of a switch.

Song et al. demonstrated an Ag/SiO₂-based TS selector in a via-hole configuration. The switching mechanism of the device was the formation and rupture of metal conductive filaments. The OFF-state resistance of this device was up to 10¹¹ Ω under a read voltage (0.1 V). When the applied voltage surpassed the threshold voltage (0.24 V, −0.5 V), the current would rapidly increase to the compliance value and the device would be switched to ON state. The current ON/OFF ratio can reach 10⁷ and the SET process slope achieves <5 mV dec⁻¹. According to device-to-device and cycle-to-cycle test, the Ag/SiO₂-based volatile devices showed good uniformity.

Hua et al. reported a bidirectional TS memristor based on Ag nanodots/HfO₂. By using anodic aluminum oxide (AAO) template as the pattern mask, the Ag nanodots were highly ordered on the dielectric layer. The volatile memristor could work well under different IᵥC without electroforming process. The device owned extremely large ON/OFF ratio over 10¹⁵, steep switching slope of 0.65 mV dec⁻¹ and good thermal stability. Furthermore, the volatile devices were connected with TaOₓ/Ta₂O₅ bilayer resistive random access memory (RRAM) as one-selector-one-resistor (1S1R) configuration. The OFF-state resistance of selector was much bigger than that of RRAM, so the voltage would mainly drop on selector before it switched to ON state. When the voltage exceeded the threshold voltage, the RRAM would be selected and change its state. The 1S1R device shows good suppression of sneak path current and excellent cycling performance over 10⁸.

Midya et al. reported one kind of one-selector-one-memristor configuration, which was consisted of a TS device based on Pd/Ag/HfO₂/Ag/Pd and a memristor based on Pd/Ta₂O₅/TaOₓ/Pd (the top-view SEM image and cross-sectional TEM image are shown in Figure 4a). Figure 4b,c shows the DC sweep characteristics of the volatile selector and the nonvolatile memristor, respectively. For the integrated device (shown in Figure 4d), the selector would turn on at about 0.5 V and the memristor would set at about 1.2 V (in the positive direction). On the contrary, the selector would be switched on at about −0.4 V and the memristor would be reset gradually (in the negative direction). The symmetric bidirectional TS selector device showed excellent features, for example, high selectivity up to 10¹⁰, steep turn on slope of under 1 mV dec⁻¹, high endurance beyond 10⁸ cycles, and fast ON/OFF switch speed less than 75/250 ns.

Figure 4. a) SEM image (top view) of the 1S1R structure (left). The cross-sectional TEM image of 1S1R configuration (right). b) Sweep cycles of the TS device. Inset is the structure illustration of the selector. c) Sweep cycles of the nonvolatile device. Inset is the structure illustration of the nonvolatile memristor. d) Repeatable bidirectional I–V curves of the 1S1R configuration. Inset is the structure schematic of 1S1R. Reproduced with permission. Copyright 2017, Wiley-VCH.
4.2. Volatile Memristor for Neuromorphic Computing

The modern big-data era has witnessed an exponential growth in the demand of data storage and processing, profoundly touching almost all the aspects of human’s life and work. There is no “universal memory” to fulfill all the requirements (speed, energy efficiency, retention performance, and endurance) of data storage. Therefore, a complex and multilevel hierarchy, consisting of volatile cache storage (static random-access memory, SRAM), main memory (dynamic random-access memory, DRAM) with fast operation speed and nonvolatile auxiliary memory including magnetic hard disk drive (HDD) and flash memory with relatively slow access speed, is used to achieve a compromise between cost and performance. Unfortunately, this architecture is essentially nonscalable and inefficient in terms of memory, computation, and communication. First, a physically separated central processing unit (CPU) and data storage units induce the von Neumann bottleneck. The data movements between CPU and memory units result in serious traffic jams. Second, with Moore’s law approaches to an end, further scaling down to facilitate integration of the increased amount of memory cells is impeded by fabrication complexity when using photolithography. Therefore, with the restriction of the von Neumann bottleneck and the ending of Moore’s law, the search for the revolutionary memory and computing techniques is highly needed to fill the upcoming power vacuum. There are great efforts on harnessing neuroscientific insights to construct non-von Neumann architectures which are scalable to large networks consisting of neurons and synapses, efficient with respect to space and energy, and flexible enough to run networks inspired by neural architectures. As such, brain-like neuromorphic computing system will be explored. The field-effect transistors and capacitors have been utilized to emulate artificial neurons and synapses, which demand significant numbers of elements and more complex circuit design. For the consideration of further practical implementation on high density of integration and low energy consumption, using memristors as basic components of the system and integrating with other primary devices can be an alternative solution.

4.2.1. Volatile Memristor as Artificial Neuron

The mission of a neuron is to process the input signal from synapses and decide whether a signal should be sent to the adjacent neuron. There are three common models to simulate neuron: Hodgkin–Huxley (HH) model, integrate-and-fire (IF) model, and leaky integrate-and-fire (LIF) model. HH model is the closest model to the biological neuron which depicts the movement of the ions and the biologically spikes comprehensively. However, achieving artificial HH neuron with LIF function is still a challenge for the absence of memristor devices with suitable performance. IF and LIF models mainly demonstrate the integration and firing processes in a neuron in detail. The input signal will be integrated and processed in a neuron, and then the neuron would compare local grade potential with threshold value and decide whether to fire a spike. The neuron based on IF model would maintain the potential until it fires. On the contrary, the neuron based on LIF model would leak out even though the potential is smaller than threshold value, which is in accordance with the phenomenon in a biological neuron. This “leaky” process allows the neuron to bring its resting potential around automatically whether the neuron fires a spiking signal or not, which corresponds to the character of volatile memristor. The representative work about artificial neurons based on memristive devices is shown in Table 2.

Huang et al. demonstrated a Quasi-Hodgkin–Huxley (Quasi-HH) neuron model based on volatile memristive devices, which were consisted of W/WO3/PEDOT:PSS/Pt. The protons from PEDOT:PSS layer could be injected into the junction of WO3/PEDOT:PSS and migrate in the WO3. The memristor shows volatile resistive switching behavior and battery effect, which are significant for the simulation of Quasi-HH neuron with LIF function combining with a dedicated electrical circuit (as shown in Figure 5b). As for the integration function, second-order memristors (e.g., SrTiO3-based memristor) with synaptic functions deliver the input signals to the neuron, and then the signal would be spatially and temporally integrated. It is worth noting that a negative feedback operational amplifier circuit is applied to operating the signal to an applicable value for the switching of memristor in this work. The local grade potential was decided by the voltage on R2. The off-state resistance of the memristor was large in comparison with the resistance of R3, so that the voltage divided on R2 was small and the local grade potential was lower than the threshold value in initial state. When the input signal was large enough to set the volatile memristor and the local grade potential became higher than the threshold voltage, the comparator would output a logic high signal. If the local grade potential was lower than the threshold value, the potential would leak out and the memristor would return back to the HRS. The logic high signal would trigger the spike generator to produce a spike signal, which is the firing

Table 2. Representative artificial neurons based on memristive devices.

| Neuron model | Memristive device | Device size | Device volatility | Voltage/threshold voltage | Auxiliary components | Ref. |
|--------------|-------------------|-------------|-------------------|---------------------------|----------------------|------|
| HH model     | Pt/NbO3/Pt        | 110 × 110 nm² | Volatile          | 1.75 V                   | DC voltage source, capacitor, and resistor | [40] |
| Quasi-HH model | W/WO3/PEDOT:PSS/Pt | –           | Volatile          | – (analog type)          | Operational amplifier, resistor, and flip-flop | [34] |
| IF model     | Ge2Sb2Te5         | ≥ (20)² nm   | Nonvolatile       | –                         | –                    | [38] |
| LIF model    | Au/AlPb1/ITO      | –           | Volatile          | – (analog type)          | Operational amplifier, resistor, and flip-flop | [33] |
| LIF model    | Ag/SiO2/Au        | 5 × 5 μm²    | Volatile          | 1 V                      | Capacitor and resistor | [57] |
| LIF model    | Si/NbO3/TiN       | –           | Volatile          | +1.8 V/−1.9 V             | Transistor            | [25] |
| LIF model    | Pt/FeO3/Au        | –           | Volatile          | 0.6 V                    | No                   | [59] |
function part of this model. Based on a reported model for battery effect,[60] the authors fitted up the signal generator with the memristor (the equivalent circuit of the memristor is shown in Figure 5c). Due to the battery effect, the output spike signal highly resembled the spike in the biological system (Figure 5d). The response of output signal to different input voltage amplitude and frequency is shown in Figure 5e,f.

Zhang et al. designed a circuit based on Ag/SiO2/Au threshold switching memristor (TSM) to emulate the integrate and fire function.[57] The neuron system is consisted of two resistors, one capacitor and one memristor. The circuit can be divided into two loops: charging loop (CL) and discharging loop (DL). There is a very important circuit parameter: resistor and capacitor (RC) time constant, which is determined by the resistance and capacitance of the loop. When a series of voltage pulses were applied on the input terminal, the current mainly flowed through the branch with capacitor and charges accumulated in capacitor. As the memristor was at HRS in the beginning, the RC time constant of DL was much larger than the one of CL, which indicated that the current leakage through the TSM was negligible. When the divided voltage on TSM exceeded the threshold value, the memristor would turn to LRS. As the resistance of the memristor decreases, the RC time constant of DL was much smaller than the RC time constant of CL. In the circumstances, the charges in capacitor would leak out and the output terminal would fire a voltage spike. Wang et al. reported a photomodulation of...
InP/ZnS quantum dots (QDs)-based memristor; the memristive mode of the device can be transited from nonvolatile resistive switching to volatile TS under UV illumination.\cite{61} In this work, the designed visual neuron based on LIF model was implemented on InP/ZnS QD-based memristor (Figure 6b). During the experiment, the memristor showed TS behavior under UV illumination. With series of voltage pulses, the charges were accumulated in the capacitor and the voltage drop on it would increase (integration). When the divided voltage on the memristor was beyond the threshold value, the device would turn from HRS to LRS and the capacitor would discharge (firing). The response of output signal to different input voltage frequency is shown in Figure 6d.

With the similar work mechanism, Wang et al. emulated the LIF neuron model with a diffusive memristor (Pt/SiO$_x$N$_y$:Ag/Pt), one resistor and one capacitor (Figure 7a,b).\cite{56} In addition, they integrated the designed neurons with synapses array, which is composed of nonvolatile memristors and a series n-type enhancement mode transistors, for building fully memristive artificial neural networks. Wang et al. utilized the networks for unsupervised learning to investigate the relationship among the features with unlabeled data and analyze the new input signal. In the demo case (Figure 7c), there was a 2 $\times$ 2 synapses array with two connected neurons. At the beginning of the experiment, all synapses were set to high resistance state (low weight) with minor deviation originated from instinct randomness. A triangular input signal or a series of rectangular input signal was applied to the array; only the column that owned the synapses with relatively high weight and received the external stimulus could prompt the corresponding neuron to fire. The firing of the neuron pulled down the potential of the BEs of corresponding synapses and further increased the weight of synapses. At the end of the work, the authors utilized an 8 $\times$ 8 memristors array and neurons for pattern classification with unsupervised learning (Figure 7d).

As for the practical application of neuromorphic computing, a large number of neurons and synapses are needed. However, the aforementioned neuron designs are not suitable for large-scale integration, due to the intricate circuit design and the attendance of capacitors. The two terminal devices own the similar device structure with capacitors (metal–insulator–metal, MIM sandwiched structure). Therefore, it is feasible to replace and reduce the capacitor for the realization of LIF function. Zhang et al. demonstrated a mott neuron based on 1T1R structure with a NbO$_x$ device and a transistor.\cite{25} In this work, the inherent parasitic capacitance of the device was used for the integration of input signal, so no external capacitors were needed. By adjusting the applied voltage on the gate terminal of the series transistor, the channel resistance $R_{\text{channel}}$ and the voltage on memristor could be precisely controlled. When an input voltage signal was applied on the gate terminal, the parasitic capacitor of the memristor would accumulate charges and lift up its voltage potential. When the potential was large enough to set the memristor, the circuit would fire a signal in the output terminal. The results show that the Mott neurons with 1T1R structure can be a promising candidate for realizing artificial neurons compared with the schemes mentioned earlier. Stoliar et al. demonstrated a LIF neuron model, which could be achieved by a single volatile memristor device based on Mott (GaTa$_4$Se$_8$) insulator.\cite{62} In this work, the whole LIF module was made of a Mott memristor and a series resistor (Figure 8a). Figure 8b shows the current response with
different spiking frequency. The increase in pulse width (tON) or the decrease in pulse interval (tOFF) would result in a decrease in NREF. Zhang et al. reported a LIF neuron model based on single volatile memristor (Pt/FeOx/Ag). [59] The I-V curves are shown in Figure 8d. When the positive sweep voltage surpasses the threshold voltage, the memristor would switch from HRS to LRS abruptly. Figure 8e shows the IF process of this memristor. A statistical analysis of the relaxation time under pulses (3.3 V, 200 μA) is shown in Figure 8f. The relaxation time last within 1 ms, which is comparable with the biological behavior.

4.2.2. Volatile Memristor as Artificial Synapse

As the junctions connecting adjacent neurons, synapses are significant to configure artificial neuron network (ANN) and carry out critical brain function. The synapses react to the activity of neurons and change the strength of interconnection, which is known as synaptic plasticity. In the past years, many circuits based on CMOS technology have been used to mimic synapses. [64–70] However, because of the finite similarity to the biological synapses, the three terminal devices need complex circuit design to imitate the synaptic behavior. As a better choice, two terminal devices (such as memristors), with less footprint and lower power consumption, are widely utilized to mimic synapses. [63, 71–75]

The strength of synaptic connection, known as synaptic weight, depends on the concentration of ions. Synaptic plasticity represents the changes of synaptic weight, which can be influenced by the spiking rate, interval of pre- and postsynaptic spiking and other factors. [76, 77] Various of memristors have been reported for realizing synaptic function, for example, short-term plasticity (STP), long-term plasticity (LTP), spike rate-dependent plasticity (SRDP), and spike timing-dependent plasticity (STDP). [78–80] STP is a dynamic phenomenon in which the synaptic strength will change provisionally within timescale from milliseconds to minutes. LTP is considered as a fixed modification of synaptic connection strength between neighboring neurons. STP contributes to facilitate kinds of computation function in the brain and LTP mainly dominate the learning and memory processes. SRDP demonstrates the impact of spike rate on synaptic plasticity. STDP is an important mechanism to reveal the connection strength, which requires accurate control of the relative time between the spikes that applied to different terminals.

Ohno et al. demonstrated a memory device based on Ag2S and studied the synaptic behaviors of it. [63] When an input signal with lower frequency applied on the devices, the conductance of memristor will shows a temporary increase and decay voluntarily. However, with a higher frequency, the memristors would have a consistent increase of conductance. In this work, Ohno et al. linked the temporary increase in conductance with STP (Figure 9a). In addition, they reported that the enhancement happened before the complete formation of thin Ag conductive filament, and the rupture of the conductive filament resulted in the decay of conductance. When a strong conductive filament was formed, the enhancement can be maintained for a long time (Figure 9b).

Wang et al. combined a diffusive memristor with a drift memristor to demonstrate SRDP and STDP. [17] The combination was similar to the synapse between the adjacent pre- and postsynaptic neurons (shown in Figure 9c). For the SRDP demonstration, a series of spiking signals with different frequency were applied on the combination. As the resistance in the HRS of the diffusive memristor was larger than that of drift memristor in this work, the spiking signal mainly acted on the diffusive memristor at the initial state. The signal with higher frequency would lead to a larger increase in the conductance of the diffusive memristor. So that the drift memristor would have a bigger voltage drop, which results in a more obvious change of resistance (Figure 9d). To study the STDP behavior, pre- and postsynaptic spikes were
applied to the diffusive memristor and drift memristor with a time difference ($\Delta t$). Each pre- or postspike included two parts (shown in Figure 9e): a high voltage with short width and a low voltage with long width, the two signals with same amplitude but inverse polarity. Due to the delay time of the diffusive memristor, the short voltage pulse with a high amplitude could not turn on the device. On the contrary, the low signal with long duration would turn on it. The drift memristor would not be switched by the first signal because the signal mainly acted on the diffusive memristor. After the removal of pulse signal, the diffusive memristor would generally decay to the HRS. Therefore, the effect of the second pulse on the drift memristor was related to $\Delta t$. A smaller $\Delta t$ corresponds to a smaller resistance of diffusive memristor, which would lead to a bigger conductance change of drift memristor (Figure 9f). If prespike came before postspike, the postspike was able to increase the conductance of drift memristor (known as potentiation); if prespike arrived behind postspike, the prespike would decrease the conductance of drift memristor (depression).

Reservoir computing systems make use of dynamic reservoirs that own short-term memory to extract characteristic from the input signal and configure a high dimensional feature space (Figure 10a). The reservoir computing systems are consisted of two parts: reservoir (connected with input) and readout function. The temporal signals transmit into the reservoir with fixed connectivity and the state of elements in the reservoir will change dynamically. To get a desirable outcome, the readout function parts will be trained. As the training process is only need in readout parts, the training cost of reservoir computing systems would be greatly reduced compared with the traditional recurrent neural networks (RNNs). To process the temporal input, the states of reservoir are related to both present and past input signal within certain time.

There are some works that have been reported the implementation of reservoir computing systems in the past decades, using field programmable gate arrays (FPGAs) and photonic systems. Because of the inherent nonlinearity and short-term memory features, memristors are identified as good candidates for the reservoir computing system in the pattern classification and signal processing. Here, we introduce two reservoir computing systems based on volatile memristors for pattern recognition.
Mao et al. reported a monocrystalline lead-free Cs$_3$Sb$_2$Br$_9$ perovskite (CSB) nano-flake-based lateral-structured memristor (Au/CSB/Au). With different channel length, the CSB device would show TS (long channel) and bipolar resistance switching (short channel). Figure 10c shows the probability of TS and bipolar switching at different channel length. When the external voltage applied on the device with a long channel, the Br/C0 anions would drift to the anode and a relative thin conductive filament composed of Br vacancies ($V_{Br}$) would form, which gave rise to the transition from HRS to LRS (shown in Figure 10e). In this work, Mao et al. utilized the CSB device working in volatile mode as the reservoir layer of a reservoir computing system, which was consisted of three layers including the input layer, reservoir layer, and the output layer. It is worth noting that the CSB device could differentiate the order of input signal with different temporal sequences, which could be used for letter recognition. Each letter in this work was divided into five temporal pulse signals, and those sequences were sent into five different devices. Figure 10i shows the current of CSB diffusive memristors with diverse input signals, which indicated the ability of identifying the temporal order. After the reservoir computing system was well trained, it showed good recognition accuracy over 96%.

4.3. Volatile Memristor for Hardware Security Applications

The information security has become a hot topic at present owing to the explosive increase in the information in our daily life. The major objective of security of internet communication was to protect the important data from the hackers. Midya et al. demonstrated a reservoir computing system by utilizing volatile memristors as reservoir elements and the nonvolatile memristors-based 1T1R configuration as the readout layer. When those bit-coded spikes were fed into the reservoir input terminal, the states of reservoir were dependent on the input streams, which could be used to analyze the input signal. Midya et al. clipped the digit image downloaded from Modified National Institute of Standards and Technology (MNIST) handwritten which had 28 x 28 pixels to 22 x 20 pixels, and then formed a 110 (22 x 5) x 4 matrix. The logic high (1.25 V, in this work) and low (0 V) signal were on behalf of the white and black pixels of the image, respectively. Those 4-bit spike streams were carried into input terminal of reservoir computing system in sequence. The readout layer was working in a supervised way based on error backpropagation to minimize a cross-entropy loss that updated the conductance of synapses. After the training process, the classification accuracy of the network can reach about 83%.
logging private account, storing important data, and completing online transactions, those common behaviors need personal authentication to guarantee the safety of the data communication. Information security has become as a research hotspot. Generally, there are two kinds of security solutions: software-based solutions and hardware-based solutions. As for the software-based solutions, they are easy to be implemented into security application and low cost. On the contrary, they are vulnerable to the attack for bugs. Hardware-based solutions have better security performance, but they are more expensive.

4.3.1. Volatile Memristor for True Random Number Generator

The integrated random number generator (RNG) plays a key role in the protection of communication by generator security code. The RNG can be divided into two parts (Figure 11): pseudorandom number generator (PRNG) and true random number generator (TRNG). However, the software-based PRNG, which generates numbers by a deterministic algorithm with a seed, is not suitable for the high security level verification. The representative kind of PRNG is based on shift register construction. The initial states of shift register in series are set by a seed, which is controlled by users and sent into the load terminal of PRNG. In addition, the output of flip-flops is connected by logical feedback circuit, and the output of logical circuit is sent to the first D flip-flop. D flip-flop is a kind of data storage device with memory function, which consists of four NAND gates. When the edge triggered signals reach the clock port, the current output depends on the value of D terminal, which is defined in Equation (2).

$$Q^* = D$$  \hspace{1cm} (2)

When no edge triggered signal arrives, the output terminal would hold its pervious state regardless of the value of D terminal. Triggered by different amounts of clock signals, the registers would generate a random-looking string of numbers. As the seed, feedback circuit, and operation time of the whole system...
are easy to be controlled and surveilled, the software-based PRNG is unable to meet the requirement of high-level information security. \[99\]

To realize true randomness, people try to find ways to utilize the intrinsic physical mechanism or phenomenon as a source of randomness. As one kind of hardware-based module, TRNG can offer better entropy quality and higher level of security performance compared with PRNG. \[100,101\] So far, a major part of TRNG is based on CMOS technology taking advantage of thermal noise from the circuits, such as oscillator, \[102–104\] MOSFET-operational amplifier, \[105\] and other metastable factors. \[106\] Thermal noise in the CMOS circuits is closely related to internal work process and external environment. Therefore, the negative feedback circuits are indispensable to reduce the disturbance and get exploitable noise signal. Those additional designs result in a more complicated layout, larger module area, and extra power consumption.

Due to the excellent property (simple structure, short switching time, low power consumption, good compatibility with modern CMOS technology, etc.), \[107–110\] memristors, both nonvolatile and volatile devices, have been used in the implement of TRNGs. Using random telegraph noise (RTN) in the memristors, Huang et al. reported a TRNG based on a RRAM. \[111\] The comparator in the circuit digitized the RTN and got random bits. However, due to lack of feedback portion, the proposed TRNG could be difficult to control and regulate the distribution of “0” and “1.” To optimize the controllability and the feasibility of memristor-based TRNGs, the stochastic switching voltage and delay time were used as the randomness source. Balatti et al. proposed an approach using the variation of switching voltage of nonvolatile memristors as entropy source. \[112\] To eliminate any influence of the previous state of the memory devices, they initialized the memristor devices after each work cycle, and then applied a sweep voltage signal on them. The peak value of the sweep signal was called random set voltage \(V_a\), a good bimodal distribution which serves as a source of randomness for the TRNGs could be obtained.

When the amplitude of pulse is comparable with SET voltage of a memristor, the resistance state of device would be switched from HRS to LRS after a certain period of time (delay time, \(t_D\)). The delay time is related to the external bias voltage, which is inversely related to the amplitude of applied voltage. Although the device-to-device and cycle-to-cycle switching behaviors are uncorrelated with each other, the data of delay time always obey statistical distribution (such as Poisson’s distribution \[113\] and normal distribution \[17\]) on the macrolevel, which can be accurately predicted and manipulated by controlling the bias voltage.

Jiang et al. demonstrated a TRNG using the stochastic switching time in a diffusive memristor (Pt/SiO\(_x\):Ag/Ag/Pt/Au), relied on the dynamic diffusion of active metal atoms in the switching layer (Figure 12a–c). \[17\] In their circuit design, the volatile memristor was connected with a resistor in series (Figure 12d). When a fixed input voltage applied on the memristor, the memristor was switched to LRS after a random delay time and induced the increase in output voltage \(V_2\). To get a well-formed voltage signal, the aforementioned voltage \(V_2\) was sent into a comparator and compared with reference voltage \(V_{ref}\) (Figure 12e). The output of comparator \(V_3\) owned a random pulse width, and then had a AND operation with a high-frequency clock signal, so that a stochastic number of pulses can be obtained (Figure 12f ). Finally, the flip-flops in counter would be frequently triggered by each signal (rising edge or falling edge) and output random numbers (0 or 1).

In addition, Woo et al. reported a novel method of realizing the TRNG using Pt/HfO\(_2\)/TiN (PHT) memristors (Figure 12g). \[23\] The sources of randomness come from the delay and relaxation times (Figure 12h,i) of the PHT volatile memory, depending on the electron trapping and detrapping processes. Compared with the TRNG design demonstrated by Jiang et al., their new circuit contains two volatile memristors, two AND gates, and a counter.
Two memristors (M1, M2) were biased by the same input voltage (V1) and switched to LRS after a stochastic delay time. After the removal of input pulse, there was a relaxation process for those memristors returning back to HRS. M1 and M2 would have different delay time and relaxation time in the same pulse cycle, so that the first AND gate (AND1) would output a digital pulse with stochastic width (Figure 12k). Then, V4 and a clock signal were sent to the second AND gate (AND2), and AND2 would produce a signal (V5) with different pulse numbers. Finally, the counter received signal (V5) and flipped with each
Both the volatile memristor-based TRNGs mentioned earlier are utilizing the variation in the switching time as randomness source. On the one hand, the traditional transistor-based comparator demands more transistors and occupies larger layout area than AND gate. The circuit design of Woo et al. reported TRNG replaces the comparator and resistor with the AND gate and an extra memristor, so that the TRNG circuit area can be reduced. On the other hand, the TRNG module would be invoked frequently and the energy consumption is a serious issue which cannot be neglected. The operation voltage of PHT volatile memristor (about 8 V) is much larger than the diffusive memristor (about 0.5 V) reported by Jiang et al., resulting in more power consumption.

In general, the pulse parameters, such as voltage amplitude, duty cycle, and frequency, should be carefully selected to balance the generation rate and the randomness of the bits. First, the amplitude and width of pulse should be large enough to guarantee the device can turn to ON state each cycle. Second, leaving adequate relaxation time after every SET process, so that the memristor can completely return back to its initial state. Last but not the least, blindly chasing bitrate would lead to a bad randomness of the bit current, all those parameters need to be optimized to achieve good property of the TRNG.\(^{17}\) Volatile memristor would turn back to the HRS spontaneously after the removal of stimulus; no extra power is needed to RESET the memristor device. Nonvolatile memristor can also be implemented in the delay time or relaxation time-based TRNG system; however, an additional RESET process is required to initialize the nonvolatile device, resulting in higher power consumption and more complex system design.

### 4.3.2. Volatile Memristor for Physical Unclonable Function

The rapid development of IoTs and cloud computing has brought soaring demand for information security. Nowadays, the common mobile security systems store the secret key in nonvolatile memory (NVM), such as electrically erasable programmable read only memory (EEPROM) or SRAM.\(^{114}\) However, such NVM without dedicated protection design is always very vulnerable facing to the external attack. The additional dedicated protection design for the NVM would increase circuit complexity and lead to extra cost.\(^{113}\) The need for a better security solution has become more important than ever.

One alternative way is to choose PUFs; PUFs take advantage of the inherent hardware-level randomness to produce a particular result, which acts as the identification of the system. Random difference of the devices can be regarded as unique physical “fingerprints” or “signatures” of hardware devices. Even the same device manufacturer with the same fabrication technology, these “fingerprints” and “signatures” cannot be replicated due to the intrinsic manufacturing process variations. This kind of randomness is cheap in comparison with EEPROMs and other expensive hardware devices, so PUFs are the promising innovative candidates for authentication and secret key storage. PUFs are the hardware system that input challenges \(c\), and output responses \(r = f(c)\). The correlation of inputs and outputs can be described as functions \(f(i)\) and the important parameters of \(f(i)\) come from the intrinsic physical variability of PUFs. According to the numbers of challenges that PUFs can process in a timeframe and the complexity of \(f(i)\), PUFs can be divided into two main categories: strong PUFs and weak PUFs (Figure 13). Strong PUFs usually own plenty of challenge–response pairs (CPRs), whereas weak PUFs often have limited number of CPRs. Furthermore, low-cost authentication and secure key generation are the two prime applications of PUFs. Strong PUFs are usually applied into authentication, and weak PUFs are applied into key generation and protection application.\(^{116}\) The PUF system will encrypt the input challenge and output its response; other modules can get the secret key by deriving that response. Figure 13 depicts the process of strong PUFs for authentication: at the beginning of the procedure, the manufacturers input numbers of challenges into the PUF module to obtain corresponding results. Then, they send those CPRs to a central verification authority and store in a database.

![Diagram](image.png)

**Figure 13.** The hardware authentication process of the PUF. Manufacturer sends the CRPs of a PUF (device X) to the database of central authority in advance. Once the users want to authentic the PUF device, they can make a request to the central authority and check the device.
When customers want to check the authenticity of an integrated hardware device, they can send requirement to the authority and verify whether their response \( r'_i \) matches with \( r_i \) stored in the database when input the same challenge \( c_i \). Only the two responses match with each other; the hardware device can pass the authentication.

Three important parameters can be used to assess the property of a PUF, such as uniqueness (UQ), uniformity (UF), and reliability.\(^{[117]}\) For a better description of those parameters, the interdistance and the intradistance for classification and identification are introduced. The interdistance is calculated as the distance between the two responses arising from applying the same challenge to two different PUFs. The intradistance is calculated as the distance between the two responses arising from applying the same challenge twice to the same PUF.\(^{[118]}\) Uniqueness represents the difference responses arising from applying the same challenge to two different PUFs. Uniformity shows the proportion of “0” and “1” in the responses results. Reliability is evaluated by the ability of a single PUF in reproducing the same responses in different measurement condition. The detailed definition, formula, and ideal value of those parameters are shown in Table 3.

In 2001, Pappu et al. realized a PUF (optical PUF) based on a laser location and polarization, one of the first implementations of a strong PUF.\(^{[119]}\) However, the CRP of optical PUF cannot be directly extracted without the attendance of external device. The practicability of those kinds of nonelectronic PUFs is limited by their poor compatibility with current CMOS fabrication processes. Owing to the rapid development of electronic industry, there are many kinds of novel PUFs, which are compatible with CMOS technology and can be directly integrated with IC, for example, arbiter PUF,\(^{[120,121]}\) ring oscillator PUF,\(^{[122–124]}\) and SRAM PUF.\(^{[125–127]}\) In recent years, due to those appealing characteristics (CMOS compatibility, low power consumption, small footprint, etc.), both nonvolatile and volatile memristors are becoming more attractive in the PUF application.\(^{[128–130]}\) Although the compositional and structural variations of the memristor array are the main drawback for memory and computing, those device-to-device variations can be used as a resource of randomness to implement in PUF.

Zhang et al. reported a volatile memristors-based weak PUF, in which the sources of randomness and unclonability were derived from the stochastic Ag clusters distribution in the active layer of different devices.\(^{[130]}\) The memristor consisted of three layers: 15 nm Au/2 nm Ti as the BE, 40 nm Au as the top electrode (TE), and a 10 nm Ag-doped SiO\(_2\) active layer.\(^{[128]}\) As for the generation of CRPs in the PUF system, the challenge signal (input) of each volatile memristor is the applied voltage and the response (output) is the current of each memory cell. If the volatile device switches to high current state with an applied voltage, it represents logic “1.” If it cannot be switched to LRS, the device represents logic “0” (Figure 14b).

5. Conclusion and Future Outlook

So far, we have reviewed some representative volatile memristors in devices, mechanisms, and electronic applications fields. To further exploit their potential for commercial purpose in electronics industry, there are still some problems that must be coped with.

For the practical implementation of memristors-based system, the devices would be required for mass production using the mainstream manufacturing technology. In addition, most of the present peripheral circuits/components for neuromorphic computing and hardware security are based on the current CMOS technology. Realizing the excellent integration and compatibility between memristors and CMOS devices/techniques are very important. Recently, diverse materials have been reported for fabricating the volatile memristors and showed good device properties. However, some of the materials are not compatible with the CMOS technology, which would not be accepted by the IC industry. Therefore, we should further investigate the switching mechanisms of those devices and find some proper material candidates, which are suitable for the commercial applications.

Table 3. The summary of PUF parameters.

| Parameters | Ideal value [%] | Definition | Formula |
|------------|----------------|------------|---------|
| Uniqueness | 50            | The difference responses arising from applying the same challenge to two different PUFs | \( UQ = \frac{1}{n} \sum_{i=1}^{n} \sum_{j=1}^{n} |\text{Inter}_\text{HD}(R_i, R_j)| \times 100\% \) where \( n \) is the number of chips, \( R_i \) and \( R_j \) are the responses to the challenge, and Inter_\text{HD} is the average interchip Hamming distance |
| Uniformity | 50            | The proportion of “0” and “1” in the response bits of the same PUF | \( UF = \frac{1}{m} \sum_{i=1}^{m} R_i \times 100\% \) where \( m \) is the number of challenges applied to the PUF and \( R_i \) is the response to the corresponding challenge |
| Reliability | 100           | The ability of PUF in reproducing the same response under external disturbance | Reliability = 100% − Intra_\text{HD}. Intra_\text{HD} is the average intrachip Hamming distance |
As the inherent and unique dynamics naturally resembles the relevant characteristic of various ion transport in biological neural systems, the TS behaviors of volatile memristors own great potential in brain-inspired computing. However, there is still plenty of space for the continuous progress. As for the sneak path current and half-select issue, an ideal selector should be scalable and stackable with excellent nonlinearity, fast switching speed (≈ ns scale), low power consumption (≈ fJ for each cycle), high endurance (more than 10¹⁰), and good device uniformity. A comprehensive summary of selectors has been reported by Xia et al. The selectors reported in recent years are only prominent in some aspects even in the single device level. To realize the large-scale memristive array, more in-depth studies on the material system and mechanisms of volatile memristors-based selectors are indispensable. For the artificial neurons, a simple circuit and system design, which does not contain capacitor and can exhibit superior performance, could be more desire for high density integration and cost-effective system. Utilizing the parasitic capacitance of two-terminal volatile memristors may be a good scheme, but the performance of the designed neurons should be further optimized. In addition, we can implement novel functional materials into the device fabrication and taking advantage of their inherent peculiarities to mimic biological neurons. As for artificial synapses, the power consumption of most memristor array for neuromorphic computing is still much larger than synaptic event in our brain. Device-to-device and cycle-to-cycle variation are big problems for fast and accurate computation. In addition, the scalability and stacking ability of memristors cannot be fully exploited with the common 1T1R configuration. More attention should focus on researching the mechanism of the memristor devices, which is helpful for controlling the performance of device and reducing the device variations. As for the system level optimization, we should develop the appropriative algorithms and peripheral circuits for memristors-based neuromorphic computing. Most of our efforts are focusing on finding the new devices or even tailor the device properties to match the existing computing architectures and algorithms, which sacrificed the unique performance of certain devices. In addition to enhance the research on material systems and mechanisms, modified and customized computing architectures/algorithms should be developed for the full play of the special device performance.

Apart from the compatibility issues, the device optimization of volatile memristors for TRNGs should aim at high-frequency operation (> 1 GHz), low-energy consumption for each random bit (≈ fJ range), high device endurance (> 10¹⁰), and small device area (≈ nm range). At the circuit level, smaller area occupation and simple design are more desirable in this application. Although the aforementioned memristors-based TRNG schemes do not need a postprocessing procedure or feedback circuit for the generation of random bits, the RTN, switching probability or the temporal responses of the memristors would change due to the external factors (such as the temperature and the device performance offset owing to frequent switching). However, for a more stable and reliable TRNGs, we should consider the necessity of adding negative feedback circuits, which is opposed to the simple circuit design. Compared with mature PRNGs using the traditional transistor resistor logic circuit, the TRNGs based on volatile memristors are still limited by poor cognition of the devices. Moreover, the randomness sources for both TRNG and PUF are significant. More work should be focused on the research on the switching behaviors and a better way to explain the mechanisms and establish the device model is desirable. The exact number of random bits for both TRNG and PUF would depend...
on the specific requirement, but it is sure that the number is huge. We should optimize material system of the memristors to improve device performance (especially the endurance and retention).

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

functional materials, neuromorphic computing, switching mechanism, temporal response, volatile memristors

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