A High-Speed Low Power Multi-Modulus Frequency Divider based on TSPC logic using 55nm CMOS

Yujuan Shao 1, Huiming Liu 1,*, Wenshen Wang 1,2

1 Tianjin Key Lab of Film Electronics and Communication Devices, School of Electrical and Electronic Engineering, Tianjin University of Technology, Tianjin, China
2 RF Microelectronics Corp., Tianjin, Chain

* Corresponding author e-mail: lhmdxx@tjut.edu.cn

Abstract. This paper presents an advanced architecture for programmable multi-modulus dividers (MMD) for high-speed and low-power synthesizers application in UMC 55nm CMOS technology. The proposed architecture used cascaded divide by divide-by-2/3. According to the design requirements, our MMD consists of 5 stages of the divide-by-2/3 dual-modulus dividers. The division ratio is ranged from 32 to 69 continually with the step of 1. Measurement results indicated a maximum operating frequency is 15GHz with 167 uW power consumption from a 1.2V supply voltage and occupied 50*14 um².

1. Introduction

Wireless communication is becoming a growing concern for military and commercial applications. As many wireless LAN (WLAN) standards operate in different frequency bands, the market-leading WLAN solution must provide multi-mode interoperability with transparent worldwide usage. The requirement for fast switching and high working frequencies make the design of frequency synthesizers a challenging task. The synthesizer can be an integer-N type with programmable integer frequency dividers or a Fractional-N type synthesizer. However, for multi-standard applications, the step size of an integer frequency synthesizer is limited by the reference frequency and it is usually difficult to cover multiple bands[1]. In the design of integer-N synthesizer, the reference frequency must be reduced to cover the fine step of multi-band channel frequency, which leads to high split ratio and high in-band phase noise. In contrast, the fractional-N synthesizers allow the frequency synthesizers to operate at a high reference frequency and also achieve fine step size by constantly swapping the loop division ratio between integer numbers, thus on average achieving a fractional number division. Meanwhile, Among the blocks in wireless communication systems, frequency synthesizers are indispensable building blocks to provide a stable Local Oscillator (LO). A generic architecture of the frequency synthesizer is shown in Figure 1[2].
Fig 1. depicts the architecture of our proposed frequency synthesizers, which mainly includes a phase frequency detector (PFD), a charge pump (CP), a low pass filter (LPF), a voltage-controlled oscillator (VCO), a frequency divider (DIV), and an auto frequency calibration (AFC) circuit. The frequency synthesizers output is given to receiver (RX) and transmitter (TX) in an RF communication system. Due to frequency requirements, the capacitance value in VCO is adjusted by switching capacitance module. A 5-bit register SW<4:0> allows 32 rough points for tuning synthesizer frequencies. The AFC circuit consists of a calibration module (CAL) and a preset voltage module (PVM). The CAL determines the appropriate value for register SW<4:0>, and the PVM provides a preset DC voltage (VPRE) as the initial VCO control voltage[3].

In a frequency synthesizer, a high-speed frequency multi-modulus frequency divider plays an important role. It is the most challenging part in a frequency synthesizer. Because it works at the highest frequency and must be controllable within a wider range in order to synthesize the desired output frequency. Therefore, a wide locking-range frequency divider with reasonable dc power consumption is a real challenge in high-frequency frequency synthesizer design.

In this paper, we propose an advanced architecture for programmable multi-modulus dividers for high-speed and low-power synthesis application. It consists of 5 stages of the divide-by-2/3 dual-modulus dividers. The division ratio is ranged from 32 to 69 continually with the step of 1. The rest of this paper is organized as follows. Section 2 introduces the programmable multi-modulus dividers architecture. Section 3 describes the design details of divide-by-2/3 dual-modulus and compare two types of divide-by-2/3 dual-modulus composed of different TSPC. Simulation results are discussed and compared with the state-of-the-art designs in the literature in Section 4. Finally, Section 5 concludes this paper.

2. The programmable multi-modulus dividers architecture

The divider is widely used in modern frequency synthesizers for a series of the desired output frequency. The division ratio of the divider decides the output frequency tuning range of the frequency synthesizer, so the wider division ratio range is very useful for multi-band or multi-mode wireless transceiver system and so on [4]. The choice of the divider architecture is therefore essential for achieving a wider output frequency tuning range of the frequency synthesizer.

The traditional frequency divider structure is based on a dual modulus prescaler. The well-known and powerful MMD architecture is illustrated in Figure 2, which is cascaded by numbers of divide-by-2/3 dual-modulus cells. However, a divide-by-2/3 dual-modulus only has two division ratios. Besides the dual-modulus prescaler, the architecture requires two additional counters for the generation of a desired given division ratio [5]. The signal Pn and Modn are the required additional counters, acting as the controlling bits. When they are both high, the divide-by-2/3 dual-modulus is in divide-by-3, while others cases are in divide-by-2. The Modn signal of the last stage is always high, ensuring that all stages divide by two when their input bits Pn are low. Thus, the frequency divider can realize any integer divider ratio between 2n and 2n+1. The architecture provides a division ratio of

\[ f_{\text{out}} = (2^n + P_{n-1} * 2^{n-1} + P_{n-2} * 2^{n-2} + \ldots + P_0) * f_{\text{in}} \]  \hspace{1cm} (1)
Where $f_{in}$ is the input signal of the frequency divider and it is also the output signal of VCO. The $f_{out}$ is the output signal of the frequency divider. By increasing or decreasing the number of 2/3 frequency division units, we can achieve the expansion or reduction of frequency division ratio range.

In this paper, our VCO frequency is 5.8GHz which becoming 1.45GHz after dividing by 4. And the PFD's reference input signal $f_{ref}$ is 32.768MHz, so the division ratio is 44.2505. According to (1), we need 5 divide-by-2/3 dual-modulus cells as shown in Fig. 3.

Due to the fractional-N frequency divider has to operate at the maximum output frequency of the synthesizer with low power dissipation, it is the key to choose the suitable architecture. Such divider usually consists of high-speed latches or flip-flops [6]. Although current-mode logic (CML) and inject locking prescaler can provide the working frequency of hundreds GHz with the process of SiO CMOS or InP DHBTs and so on, true single phase clock (TSPC) dual-modulus prescaler is widely utilized in several/tens GHz with standard CMOS process[4]. The TSPC D-Flip-Flop has the merits of single clock phase, low power, small area, and a large output swing. Furthermore, improving the speed of transformation is an important design issue for TSPC prescaler. So, in order to lower the power consumption and improve the speed of transformation, TSPC is used in the D-Flip-Flop, and the control logics are implemented in CMOS logic.

3. The divide-by-2/3 TSPC dual-modulus divider
In this paper, according to the design requirements, the programmable multi-modulus divider is made up of 5 stages of divide-by-2/3 dual-modulus dividers. The traditional divide-by-2/3 usually consist of D-latches and logic gates as shown in Fig.4. It consists of four D-latches and three AND gates. An improved structure is presented in this paper in Fig. 5. Compared Fig. 4 and Fig. 5 we can find Fig. 5 reduce two D-latches. It can simplify the structure and reduce the chip area. In Fig. 4 and Fig. 5, all D-latch is common logical gate D-latches that is lower power, but it cannot operate in high frequency.

At the input where the frequency is higher, the first two stages of divide-by-2/3 dual-modulus dividers must be operated in several/tens GHz. Figure 6 shows the improved divide-by-2/3 operating at high frequency. In the last section, we mentioned that TSPC D flip-flop can work at high frequencies. So the D flip-flop, as shown in Fig. 6, is made up TSPC.
TSPC logic gates refer to structures with a series of single-phase-clock controlled latches in their N-type MOS logic gates, P-type MOS logic gates or both. By cascading multiple stages of basic TSPC logic gates, which can be regarded as clocked inverters, we can construct an edge-triggered TSPC D-flip-flop (DFF). Fig. 7 shows a typical TSPC DFF consisting of three stages: an N latch, a dynamic inverter and a P latch.

Compared Fig. 5 and Fig. 6 we can find Fig. 6 reduce two AND gates. Because the proposed TSPC D-flip-flop is different from conventional TSPC D-flip-flop. In many literatures, the traditional TSPC D-flip-flop has two input signals: the clock signal clk, and input signal \( D \). Two output signals are produced: \( Q \) and its negational signal \( QN \) as shown in Fig. 8. In this paper, the proposed TSPC D-flip-flop has three input signals: clk, \( D1 \), and \( D2 \), as shown in Fig. 7. The output signal, \( Q \), is equal to \( D1&D2 \). That is why the proposed structure of TSPC divider-by-2/3 prescaler reduce two AND gates.

4. Simulation results and performance comparison
A complete analysis and comparison of the performance of the proposed divider-by-2/3 prescaler with two input signals TSPC from conventional divide-by-2/3 prescaler with one input signal TSPC is carried out. The comparisons included the highest working frequency and speed. Firstly, the proposed TSPC
divider-by-2/3 prescaler can operate in 15GHz according to simulation by Virtuoso. The waveform is shown in Fig. 9. A conventional version just operated up to 10GHz. Secondly, the speed refers to the time from low level to high level. The speed of the proposed TSPC divider-by-2/3 prescaler is 35.6 ps in 10GHz, the speed of conventional of TSPC divider-by-2/3 prescaler is 44.4ps in 10GHz. Obviously, the proposed structure is better than the conventional one in terms of speed. To make the difference more intuitive, we make a graph about their speed as shown in Fig. 10. Delay refers to the time used to change from low level to high level.

Obviously, as can be seen from the above comparison, the proposed divider-by-2/3 prescaler is significantly better than the conventional of it in both the highest working frequency and transfer speed.

![Fig. 9 waveform of the proposed structure of TSPC divider-by-2/3 prescaler](image)

![Fig. 10 simulation results of the conventional and proposed divider-by-2/3 prescaler](image)

To provide a better comparison, some other high-performance TSPC designs [4,6] are listed in table 1. The simulation results show that our divider-by-2/3 prescaler can reach a maximum operating frequency of 15GHz with power consumption of 115uW and 167uW in the divide-by 2 and divide-by-3 modes, respectively. The power-delay product (PDP) value is measured at the maximum working frequency and can be regarded as the normalized power consumption or the energy consumption per clock cycle. Table 1 shows the detailed simulation results against clock frequency simulation results for the prescalers in the divide-by-2 and divide-by-3 modes.

|                      | conventional TSPC divider-by-2/3 prescaler | proposed TSPC divider-by-2/3 prescaler | [4]  | [6] |
|----------------------|---------------------------------------------|----------------------------------------|------|-----|
| Number of Trans.     | 42                                          | 30                                     | 29   | 34  |
| Max frequency(GHz)   | 10                                          | 15                                     | 14.9 | 12.9|
| Power(uW)            | 107                                         | 115                                    | 153  | 263 |
| \(\div 2/\div 3\)    | /156                                        | /167                                   | /197 | /313|
| PDP(jJ)              | 7.32                                        | 5.02                                   | 8.55 | 14.7|
| \(\div 2/\div 3\)    | /9.97                                       | /9.07                                  | /11  | /17.5|

5. Conclusion

In this paper, a novel architecture for programmable multi-modulus dividers based on a proposed TSPC D-flip-flop are presented. The proposed divide-2/3-prescaler use a unique TSPC D-flip-flop logic on 55nm CMOS technology with 1.2V supply voltage. Measurement results show a maximum operating frequency of 15GHz with power consumption of 115uW and 167uW in the divide-by 2 and divide-by-3 modes. And, by comparing our proposed structure has a big performance improvement.
Acknowledgments
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