A Variation-Aware Quantum Circuit Mapping Approach Based on Multi-agent Cooperation

Pengcheng Zhu, Student Member, IEEE, Weiping Ding, Senior Member, IEEE, Lihua Wei, Xueyun Cheng, Zhijin Guan, Member, IEEE, and Shiguang Feng, Member, IEEE

Abstract—The quantum circuit mapping approach is an indispensable part of the software stack for the noisy intermediate-scale quantum (NISQ) device. It has a significant impact on the reliability of computational tasks on NISQ devices. To improve the overall fidelity of physical circuits, we propose a quantum circuit mapping method based on multi-agent cooperation. This approach considers the Spatio-temporal variation of quantum operation quality on the NISQ device when inserting ancillary operations. It consists of two core components: the qubit placement algorithm and the qubit routing method. The qubit placement algorithm exploits the iterated local search framework to find a desirable initial mapping for the reduced symmetric form of the original circuit. The qubit routing method generates the physical circuit through multi-agent communication and collaboration. Each agent inserts the ancillary gates independently according to its environment state. The quality of the physical circuit evolves according to an information-exchanging mechanism between agents, which combines the local search and global search. The experimental results confirm the performance of our approach in improving circuit fidelity. Compared with the state-of-the-art method, our method can improve the success rate by 25.86% on average and 95.42% at maximum.

Index Terms—quantum circuit mapping, qubit placement, qubit routing, multi-agent cooperation, Noisy Intermediate-scale Quantum (NISQ).

I. INTRODUCTION

In the past few years, remarkable progress has been achieved in the physical realization of noisy intermediate-scale quantum (NISQ) devices. Google has released a 53-qubit processor and demonstrated the quantum advantages [1] on it. IBM has also released a 127-qubit processor and will release quantum processors with more than 1,000 qubits in 2023. These NISQ devices have a great prospect in chemistry [2], finance [3], and artificial intelligence [4].

With the rapid progress of quantum hardware technology, the software stack for NISQ devices has also attracted more and more attention from both academia and industry. Quantum circuit mapping is an essential part of the kernel software for near-term quantum devices. It converts the quantum logic circuit that is hardware agnostic to the physical one that is hardware compliant by inserting additional quantum operations (such as SWAP gates). Those inserted operations will increase the gate count and the circuit depth, deteriorating the reliability of computation. Therefore, it is critical to minimize the number of additional gates to ensure the output fidelity of the hardware-compliant circuit. The problem of quantum circuit mapping is NP-complete [5], [6], so heuristic approaches [7]–[15] play a dominant role in efficiently solving this problem. As far as we know, the work in [7] proposes the first quantum circuit mapping method for the real-world quantum device, which divides the quantum circuit into layers and finds a topology compatible solution for each layer using the A* algorithm. The work in [13] presents a SWAP-based heuristic search algorithm, which employs the reverse traversal technique to optimize the initial mapping. The work in [9] demonstrates the quantum circuit mapping method used in the quantum computing compiler $t|ket\rangle$. The work in [15] proposes a quantum circuit mapping method based on subgraph isomorphism and depth-limited search. All these heuristic approaches aim to minimize the number of additional gates inserted during the circuit mapping process, oblivious to the variation of operation quality on the actual NISQ devices. However, in the current NISQ devices, the Spatio-temporal variation of qubit and quantum operation quality is inevitable and noticeable. It is crucial to consider this variation in the circuit mapping approach for the high fidelity of quantum computation. To this end, some recent works [16]–[19] propose the variation-aware approach and demonstrate its effectiveness in improving circuit fidelity. However, their experimental evaluation on only very small-scale circuits (with up to 5 qubits and dozens of gates) is not enough to fully demonstrate the advantages of the variation-aware strategy in improving fidelity. Furthermore, these approaches are essentially circuit mapping processes based on a single intelligent agent. Since these single-agent approaches generally use
the greedy search strategy, the solutions obtained usually have considerable space for further optimization in both gate count and circuit fidelity.

As discussed, although some effort has been dedicated to the variation-aware quantum circuit mapping approach, the noted algorithms suffer from the following limitations and challenges: (1) The single-agent scheme based on a simple accumulation of the local optima leaves considerable space for further optimization. (2) It is not comprehensive enough to perform experiments on only small-scale circuits.

To address these challenges, we propose a novel quantum circuit mapping scheme based on multi-agent cooperation. This approach considers the variation of gate errors and aims to optimize the overall reliability of quantum computation on actual NISQ devices. Our main contributions include:

1) We propose a qubit placement algorithm based on the iterated local search for the reduced symmetric form of the original logical circuit. This algorithm can guarantee both the quality and the diversity of the initial population of agents.

2) We also propose a qubit routing algorithm based on multi-agent cooperation. Each agent makes decisions independently according to the environmental status and evolves the circuit quality through a mechanism similar to the shuffled frog-leaping algorithm (SFLA).

3) We perform the experiments on a noisy simulator with gate error 10x lower than that of the state-of-the-art device of IBM. With the help of this simulator, we can reliably execute large-scale circuits beyond the capacity of current NISQ devices. Extensive experimental evaluation on various benchmarks confirms the effectiveness of our approach in improving circuit fidelity.

This paper is organized as follows. We briefly review the NISQ device and quantum circuit mapping in Section II. Section III and Section IV delineate the qubit placement algorithm and the qubit routing algorithm, respectively. Section V shows the experimental evaluation. Section VI gives further discussions and Section VII concludes this paper.

II. BACKGROUND

This section will review the characteristics of current NISQ devices through several quantum devices of IBM and briefly introduce the quantum circuit mapping problem.

A. The Characteristics of NISQ devices

IBM’s quantum devices are designed based on the superconducting transmon qubit. Such a qubit of this kind is not a natural atom, but an artificial circuit made of superconducting materials. For superconducting qubits, the single-qubit gates are usually driven resonantly by a microwave pulse, and the two-qubit gates can only act on the two qubits connected by a coplanar waveguide (CPW) resonator. In the rest of the paper, we denote the coupling graph by $CG(V,E)$, where $V$ and $E$ represent the node-set and the edge-set, respectively. Accordingly, $|V|$ and $|E|$ represent the cardinality of the set $V$ and the set $E$, respectively.

Due to the defects of manufacturing technology and the error of the control pulse signal, the superconducting qubits and quantum gates acting on them show remarkable variability in quality. Even the same quantum gate behaves differently on different qubits. Fig. 2 shows the distribution of CNOT gate error rates on the 5-qubit NISQ device IBMQ_belem (Fig. 1a). We can easily observe that the CNOT gate error varies apparently as the qubits change. Furthermore, the qubit quality and operation fidelity will inevitably drift over time, so IBM calibrates their devices periodically, at least once a day, to ensure everything is under control.

At present, the NISQ devices suffer from many noise sources, such as gate error, decoherence error, and readout error. In this paper, we focus on the variation of gate error, especially on that of two-qubit gate error, since the two-qubit gate error is a major source of noise.
on NISQ devices.

B. Quantum circuit mapping

The quantum circuit realizing a specific quantum algorithm is usually hardware-agnostic. We call it the quantum logical circuit to distinguish it from the physical circuit directly runnable on real quantum devices. We denote the quantum logical circuit as $LC(Q,G)$, where $Q$ and $G$ represent the set of logical qubits and the set of quantum gates, respectively.

The coupling graph $CG(V,E)$ of a NISQ device imposes a topology constraint on physically executing the quantum circuit. This topology constraint requires that every two-qubit gate should act on the two qubits connected by a bus. The quantum logical circuit with a sequence of two-qubit gates generally cannot satisfy this constraint. Quantum circuit mapping can make the quantum circuit compatible with the restricted topology through two main steps. The first step is the qubit placement, and the second is the qubit routing.

The qubit placement is to place each logical qubit of the circuit onto a physical qubit of the device. Mathematically, the relationship between logical and physical qubits is an injective function $\pi$ from the logical qubits $Q$ to the physical qubits $V$. We call this mapping relationship the initial mapping.

Given an initial mapping, the qubit routing moves all the two-qubit gates that do not meet the topology constraint to the two adjacent nodes in the coupling graph by inserting SWAP gates. The SWAP gate is a quantum operation that can interchange the quantum states of two qubits, and it can be decomposed into 3 CNOT gates, as shown in Fig. 3. In the qubit routing process, we insert a series of SWAP gates to move the logical qubits along the edge of the coupling graph until all two-qubit gates act on adjacent nodes. The circuit obtained after routing satisfies the topology constraint and thus is physically executable. We call it the physical circuit and denote it as $PC(V,G)$, where $V$ and $G$ are physical qubit set and gate set, respectively.

We give an example of the quantum circuit mapping problem as follows. For more illustrative examples, please refer to the previous work [7], [11], [13], [14].

Example 1. We show a quantum logical circuit for preparing the GHZ state in Fig. 4a and map it to IBMQ_belem (Fig. 4b). Given the identity initial mapping between the logical qubits and the physical qubits, we insert a SWAP gate to get the physical circuit (Fig. 4b), which is topology compliant.

When performing circuit mapping tasks, considering the variation of operation quality is crucial to improve computational reliability. Different strategies for qubit placement and qubit routing will lead to physical circuits with different fidelity. Recent work [16–18] provides some motivating examples for the importance of considering error variation.

III. QUBIT PLACEMENT ALGORITHM

Our multi-agent qubit routing approach requires numerous initial mappings, one for each agent. The quality and diversity of the initial agent population largely depend on the initial mappings generated by the qubit placement algorithm. However, most existing qubit placement algorithms [13], [14] are deterministic and thus lack diversity for the resulting initial mapping. The others based on the meta-heuristic algorithm, such as simulated annealing [19], [21], are stochastic but can not guarantee the quality of the generated initial mapping within a reasonable time. Therefore, we propose a qubit placement algorithm based on the iterated local search (ILS) to ensure both the quality and diversity of the initial mapping. In this section, we first introduce several related definitions, then present the construction of the reduced symmetric circuit, and finally focus on the ILS-based qubit placement method.

A. Related concepts

Definition 1: For a CNOT gate $CX(q_i,q_j)$, its physical distance on the coupling graph $CG(V,E)$ under the initial mapping $\pi$ is the length of the shortest path between the two physical nodes $\pi(q_i)$ and $\pi(q_j)$ on $CG$.

Definition 2: The front layer of a quantum logical circuit refers to the gates without any dependence on other gates.

The dependence between gates in the logical circuit can be expressed as a directed acyclic graph (DAG) [10], [11]. In the DAG, all the nodes without any predecessors constitute the front layer, that is, the first layer of the circuit. By removing the nodes in the front layer, we can derive the second layer of the circuit. In this way, we can partition the logical circuit into multiple layers from left to right.

Definition 3: A two-qubit quantum gate is executable if it is in the front layer and its physical distance is equal to 1. A single-qubit gate is executable if it is in the front layer.

A two-qubit gate satisfies the topology constraint imposed by the coupling graph only if its physical distance is 1.
backward. Although this approach can generate multiple
traversal technique that improves a randomly generated
observation, previous work [11] proposes the bidirectional
generating an appropriate initial mapping. With this ob-
adjacent physical qubits by inserting SWAP gates, thus
process can gather the logical qubits into a cluster of
strong links with low error rates. The qubit routing
physical qubits should have long coherence times and
improve the fidelity of the output state, these selected
with a similar qubit-interaction structure. Moreover, to
the logical qubits to a cluster of adjacent physical qubits
ensure the diversity and quality of the initial agent
mapping for each agent of the routing algorithm. To
C. ILS-based qubit placement algorithm
Our qubit placement algorithm provides an initial
mapping for each agent of the routing algorithm. To
ensure the diversity and quality of the initial agent
population, it should generate multiple different good
initial mappings. An advisable initial mapping allocates
the logical qubits to a cluster of adjacent physical qubits
with a similar qubit-interaction structure. Moreover, to
improve the fidelity of the output state, these selected
physical qubits should have long coherence times and
strong links with low error rates. The qubit routing
process can gather the logical qubits into a cluster of
adjacent physical qubits by inserting SWAP gates, thus
generating an appropriate initial mapping. With this ob-
ervation, previous work [11] proposes the bidirectional
traversal technique that improves a randomly generated
initial mapping by invoking qubit routing forward and
backward. Although this approach can generate multiple
initial mappings by inputting distinct random initial
mappings, the quality of the improved initial mapping
largely depends on the random initial mapping and thus
is very unstable. Moreover, this approach does not
consider the error variation of different qubits and links.
To better serve our multi-agent approach of qubit
routing, we propose a qubit placement algorithm based
on the iterated local search [22]. Our qubit placement
approach regards the qubit routing process as a discrete
function with the initial mapping as input and the
physical circuit as output. It searches the domain of this
function for the initial mapping that can lead to the
physical circuit with high fidelity by the iterated local
search. During each local search, the neighborhood of
the current initial mapping is generated by qubit routing
and evaluated by the fidelity of the resulting physical
circuit. The fidelity of a physical circuit is estimated by
the rate of successful trials obtained by executing this
circuit many times on a noisy simulator that mimics the
target devices. It is very time-consuming to route and
simulate the entire quantum circuit in an iterated way,
especially for the large-scale circuit. In contrast, it is triv-
ial in time overhead for the reduced symmetric circuit.
As discussed above, the reduced circuit can preserve
the same qubit-interaction relationship as the original
circuit. In addition, its mirror part can guarantee that
the updated initial mapping generated by qubit routing
is beneficial to the routing of the leftmost part of the
original circuit. Therefore, by replacing the original cir-
cuit with its reduced symmetric form, we can achieve a
good trade-off between the quality of the initial mapping
and the time overhead of generating and evaluating the
initial mapping.
We show our ILS-based qubit placement approach in
Algorithm 1. Line 1 of Algorithm 1 initializes the initial
mapping and the maximum value of estimated fidelity
of the resulting physical circuits. Line 4-10 constitute the
local search of the initial mapping. With the reduced
circuit (RC) and the current initial mapping ($\pi_0$) as input,
Line 5 invokes the qubit routing approach to generate
the physical circuit ($pc_0$) corresponding to $\pi_0$ along
with a novel initial mapping ($\pi_1$) for the next iteration. Line 6
calculate the estimated fidelity ($p_{\text{suc rate}}$ percentage of suc-
cessful trials) by running $pc_0$ multiple times on a noisy
simulator. Line 7-9 preserve the best initial mapping
leading to the physical circuit with the best fidelity so
far. Line 10 prepares for the next local search iteration.
After a limited number (defined by $J$) of consecutive
local search iterations, the logical qubits are gathered in
a local region of the hardware topology by the qubit
routing approach. In this case, it is very difficult for the
qubit routing approach to move the logical qubits further
to the other area of the hardware topology. Therefore,
to explore more areas of the hardware topology, we
perform a random shuffle perturbation on the best initial
mapping so far (Line 3). We repeat this search process $I$
times (Line 2) and return the best initial mapping found
(Line 13). We use the qubit routing approach of our

B. Reduced symmetric circuit
We take the reduced symmetric circuit as the input of
our ILS-based qubit placement approach. This reduced
circuit is a reduced form of the original logical circuit. It
preserves the qubit-interaction structure in the original
circuit while retaining only a small number of gates
of the original circuit. To create a reduced symmetric
circuit, we scan the original circuit from left to right,
skipping each single-qubit gate, and remaining only the
first two-qubit gate for each interacting qubit pair. The
reduced circuit plus its mirror circuit constitutes the
reduced symmetric circuit. The mirror circuit is obtained
by reversing the gate order of the reduced circuit.
We show the reduced symmetric circuit of the bench-
mark circuit '4gt13_92' in Fig. 5. The left part of the
quantum circuit in Fig. 5 is the reduced circuit. There are
six different interacting qubit pairs in '4gt13_92', and we
retain only the first two-qubit gate for each interacting
qubit pair, so there are six CNOT gates in the reduced
circuit. These CNOT gates maintain their dependency on
each other in the original circuit. The right part of the
quantum circuit is the mirror circuit, which is just the
reverse of the reduced circuit.
For any quantum circuit, its reduced symmetric circuit
contains a limited number of gates, with an upper bound
of twice the number of edges in the coupling graph. The
small number of gates ensures that the time overhead of
mapping or simulating the reduced circuit is trivial.

C. ILS-based qubit placement algorithm
Our qubit placement algorithm provides an initial
mapping for each agent of the routing algorithm. To
ensure the diversity and quality of the initial agent
population, it should generate multiple different good
initial mappings. An advisable initial mapping allocates
the logical qubits to a cluster of adjacent physical qubits
with a similar qubit-interaction structure. Moreover, to
improve the fidelity of the output state, these selected
physical qubits should have long coherence times and
strong links with low error rates. The qubit routing
process can gather the logical qubits into a cluster of
adjacent physical qubits by inserting SWAP gates, thus
generating an appropriate initial mapping. With this ob-
ervation, previous work [11] proposes the bidirectional
traversal technique that improves a randomly generated
initial mapping by invoking qubit routing forward and
backward. Although this approach can generate multiple
initial mappings by inputting distinct random initial
mappings, the quality of the improved initial mapping
largely depends on the random initial mapping and thus
is very unstable. Moreover, this approach does not
consider the error variation of different qubits and links.
To better serve our multi-agent approach of qubit
routing, we propose a qubit placement algorithm based
on the iterated local search [22]. Our qubit placement
approach regards the qubit routing process as a discrete
function with the initial mapping as input and the
physical circuit as output. It searches the domain of this
function for the initial mapping that can lead to the
physical circuit with high fidelity by the iterated local
search. During each local search, the neighborhood of
the current initial mapping is generated by qubit routing
and evaluated by the fidelity of the resulting physical
circuit. The fidelity of a physical circuit is estimated by
the rate of successful trials obtained by executing this
circuit many times on a noisy simulator that mimics the
target devices. It is very time-consuming to route and
simulate the entire quantum circuit in an iterated way,
especially for the large-scale circuit. In contrast, it is triv-
ial in time overhead for the reduced symmetric circuit.
As discussed above, the reduced circuit can preserve
the same qubit-interaction relationship as the original
circuit. In addition, its mirror part can guarantee that
the updated initial mapping generated by qubit routing
is beneficial to the routing of the leftmost part of the
original circuit. Therefore, by replacing the original cir-
cuit with its reduced symmetric form, we can achieve a
good trade-off between the quality of the initial mapping
and the time overhead of generating and evaluating the
initial mapping.
We show our ILS-based qubit placement approach in
Algorithm 1. Line 1 of Algorithm 1 initializes the initial
mapping and the maximum value of estimated fidelity
of the resulting physical circuits. Line 4-10 constitute the
local search of the initial mapping. With the reduced
circuit (RC) and the current initial mapping ($\pi_0$) as input,
Line 5 invokes the qubit routing approach to generate
the physical circuit ($pc_0$) corresponding to $\pi_0$ along
with a novel initial mapping ($\pi_1$) for the next iteration. Line 6
calculate the estimated fidelity ($p_{\text{suc rate}}$ percentage of suc-
cessful trials) by running $pc_0$ multiple times on a noisy
simulator. Line 7-9 preserve the best initial mapping
leading to the physical circuit with the best fidelity so
far. Line 10 prepares for the next local search iteration.
After a limited number (defined by $J$) of consecutive
local search iterations, the logical qubits are gathered in
a local region of the hardware topology by the qubit
routing approach. In this case, it is very difficult for the
qubit routing approach to move the logical qubits further
to the other area of the hardware topology. Therefore,
to explore more areas of the hardware topology, we
perform a random shuffle perturbation on the best initial
mapping so far (Line 3). We repeat this search process $I$
times (Line 2) and return the best initial mapping found
(Line 13). We use the qubit routing approach of our

Fig. 5. Reduced symmetric circuit of '4gt13_92'
Algorithm 1: Qubit placement based on iterated local search

Input: Reduced symmetric circuit $RC(Q,G)$ and coupling graph $CG(V,E)$

Output: Initial mapping $\pi$

1. $(p, p_{\text{best}}) = (\text{rand\_map}(), 0)$;
2. while $i + + \leq I$ do
3. $\pi_0 = \text{shuffling\_perturb}(\pi)$;
4. while $j + + \leq J$ do
5. $(p_0, \pi_1) = \text{qubit\_router}(RC, CM, \pi_0)$;
6. $p_{\text{suc}} = \text{simulate}(p_0, \pi_0)$;
7. if $p_{\text{suc}} > p_{\text{best}}$ then
8. $(\pi, p_{\text{best}}) = (\pi_0, p_{\text{suc}})$
9. end
10. $\pi_0 = \pi_1$;
11. end
12. end
13. return $\pi$;

previous work (Algorithm 3 of [23]) as the qubit router ($\text{qubit\_router}()$, Line 5) in Algorithm 1. However, indeed any heuristic qubit mapping approach based on SWAP gates is adequate. The qubit router of this kind traverses the quantum circuit from left to right and inserts the SWAP gate step by step to make all the two-qubit gates comply with the topology constraint. For more details of such heuristic qubit routers, please refer to the prior work [11], [13], [14].

We also take advantage of the iterated local search in another work of quantum circuit mapping. The ILS-based framework in this paper distinguishes itself from our previous work in three aspects. First and foremost, it searches and outputs the initial mapping producing the best circuit fidelity rather than the physical circuit with minimum additional gates. Second, it accounts for the variation of qubit quality and gate error by running physical circuits on a simulator that mimics the real quantum hardware. Third, it traverses the reduced circuit instead of the original one for time efficiency.

D. Time complexity

For the qubit router ($\text{qubit\_router}()$), the worst time complexity is $O(|V|^5 \cdot D \cdot |G|)$, where $D$ is the diameter of the coupling graph, $V$ is the set of physical qubits, and $G$ is the set of gates in the reduced circuit. There are at most $2|E|$ gates in the reduced circuit. In addition, $|E| \leq |V| \cdot (|V| - 1)/2$ and $D < |V|$. Therefore, a rough upper bound of this complexity is $O(|V|^6)$. Accordingly, the worst time complexity of Algorithm 1 is $O(I \cdot J \cdot |V|^6)$, which is polynomial.

IV. QUBIT ROUTING APPROACH BASED ON MULTI-AGENT COOPERATION

In this section, we present the multi-agent qubit routing approach. In particular, we emphasize the decision-making of any individual agent and the cooperation mechanism between agents.

A. Motivation

Most existing approaches for qubit routing aim to minimize the number of additional gates inserted to make the quantum circuit conforms to the hardware topology. Although gate count is an essential metric of the quality of quantum circuits, it is not comprehensive enough. In contrast, the computational success rate of quantum circuits (circuit fidelity) on quantum devices is more comprehensive, especially for NISQ devices. Some previous works of qubit routing take this metric as their first optimization goal. They exploit the variation of gate error to improve the overall circuit fidelity. Such approaches are more practical for nowadays quantum devices because the error variation is common at present. However, existing variation-aware qubit routing approaches insert SWAP gates by local-optimum strategies. Simple accumulation of the local optima generally cannot approach the global optima, so there is still a big gap between the approximate solution obtained by existing approaches and the global optima.

The research on swarm intelligence [24] shows that information sharing can effectively promote the evolution of the population. With the help of a proper information sharing mechanism, we can also continuously improve the quality of physical circuits for a population of multiple agents. Motivated by this, we present a qubit routing...
approach based on multi-agent communication and collaboration. We show the schematic of this approach in Fig. 6. As shown, multiple agents complete the quantum circuit mapping task cooperatively. Each agent starts from an initial environment state (see S1) and iteratively responds to its environment through a specially selected action (see S5) to gradually build the physical circuit. In each iteration, each agent can improve its partial physical circuit through global information exchange (see S2) and local information exchange (see S4). When the iteration satisfies the termination condition, we take the physical circuit of the best agent as output (see S6).

B. Decision-making of individual agent

An agent perceives its environment and makes decisions about actions to take. For the qubit routing problem, the status of the environment can be described by three elements. They are the injective mapping relation \( \pi \) between logical qubits and physical qubits, the remaining logical circuit \( \text{vcir} \) to be mapped, and the physical circuit \( \text{pcir} \) composed of already mapped gates and inserted SWAP operations. We thus use the triple \( (\pi, \text{vcir}, \text{pcir}) \) to represent the environment state. At the beginning of qubit routing, the environment status is initialized as follows: \( \pi \) is an initial mapping returned by Algorithm 1. \( \text{vcir} \) is obtained by removing all single-qubit gates and two-qubit gates executable on \( \pi \) from the original logical circuit; \( \text{pcir} \) consists of all executed gates removed from the original logical circuit. To achieve the task of qubit routing, the agent should take action by inserting SWAP gates until the \( \text{vcir} \) is empty. Therefore, the agent will choose which SWAP gate to insert according to the following steps.

Step 1. Evaluate the reward function for each candidate SWAP gate. Among all possible candidate SWAP gates, those that reduce the physical distance for at least one front gate constitute the candidate SWAP set. We show the reward function of the SWAP gate \( sw \) in (1), where \( \pi \) is the mapping relation between logical and physical qubits, \( L_0 \) is the set of front gates, \( d(g, \pi) \) is the physical distance of the gate \( g \). (1) accumulates the reduction in physical distance for all front gates. The larger the value of (1), the higher the short-term reward obtained by applying the SWAP gate.

\[
\text{reward}(sw, \pi) = \sum_{g \in L_0} (d(g, \pi) - d(g, sw \cdot \pi)) \quad (1)
\]

Step 2. According to the reward, select the best SWAP gate. We will choose the SWAP gate with the best reward. If there are multiple, we will choose the one through roulette-wheel selection. As shown in (2), the chosen probability of each SWAP gate depends on its fidelity. The higher the fidelity of a SWAP gate, the higher the probability of being selected. The SWAP gate can be realized by three CNOT gates, so its fidelity is the product of the fidelity of these CNOT gates. We show the fidelity of a SWAP gate in (3), where \( err() \) represents the error rate of the CNOT gate.

\[
p(sw_i) = \frac{\text{fid}(sw_i)}{\sum_{i=1}^{n} \text{fid}(sw_i)} \quad (2)
\]

\[
\text{fid}(sw(v_i, v_j)) = (1 - err(v_i, v_j))^2 \cdot (1 - err(v_j, v_i)) \quad (3)
\]

Step 3. Insert the SWAP gate and update the environment status \( (\pi, \text{vcir}, \text{pcir}) \). First, update \( \pi \) by applying the SWAP gate. Second, renew \( \text{vcir} \) by removing from it all gates executable on \( \pi \). Third, renew \( \text{pcir} \) by inserting the SWAP gate and all just executed gates into it.

The agent will repeat the above decision-making steps until \( \text{vcir} \) is empty. At last, \( \text{pcir} \) is the physical circuit that satisfies the hardware constraint.

Given the coupling graph \( CG(V, E) \), in the worst case, we should calculate (1) for \( |E| \) candidate SWAP gates. Since the front layer contains \( |V|/2 \) two-qubit gates at most, the time complexity of individual agent decision-making is \( O(|E| \cdot |V|/2) \).

C. Qubit routing based on multi-agent cooperation

Just a single agent is not enough to achieve essential improvements in circuit quality. To overcome this, we include multiple agents to form a population and adopt an intelligent information-exchanging mechanism. This communication mechanism is similar to that used by the shuffled frog-leaping algorithm (SFLA [25]). SFLA is a memetic meta-heuristic for combinatorial optimization. It combines the benefits of the local and global search to converge to the global optima with a good speed and likelihood. However, it is not practicable to treat the qubit routing problem as a traditional combinatorial optimization problem and solve it with SFLA. The reason is that, unless we make multi-stage decisions meticulously, we generally cannot obtain a feasible solution to this problem through mere observation. Even worse, we cannot get another feasible solution by simply perturbing one feasible solution. To adapt this communication mechanism to the qubit routing problem, we take the partial solution generated by each agent as the sharing information rather than the complete solution. Taking Fig. IV-C as an example, agents are arranged into two groups and cooperate through the local and global information exchange. Agents in the same group communicate through the local shared information, making the
worst agent (labeled with W) converge to the best one (labeled with B); agents in different groups communicate through the global information exchange. The global and local information exchange, plus the decision-making of every agent, constitute the iteration of our qubit routing approach based on multi-agent cooperation. As shown in Algorithm 2, our multi-agent qubit routing approach mainly consists of six steps.

**Step 1.** Initialize all agents. Similar to SFLA, there are \( N = m \times n \) agents partitioned into \( m \) groups. We set the initial state \((\pi, vcir, pcir)\) of the environment for each agent, respectively. More specifically, \( \pi \) is set to be the initial mapping returned by Algorithm 1, \( vcir \) and \( pcir \) are updated by checking executable gates in the original circuit based on \( \pi \). Algorithm 1 can generate various high-quality initial mappings through multiple runs, ensuring the diversity and quality of the initial population.

**Step 2.** Check termination condition. An agent completes the qubit routing process if the property \( vcir \) of its environment is empty. When the number of agents that have completed routing exceeds \( n \), we stop this algorithm because the remaining agents have a low probability of producing better physical circuits. Otherwise, go to the next step.

**Step 3.** Rank agents according to fitness (global information exchange). We compute the fitness value for each agent and sort the agents in descending order according to the fitness value, leading to an ordered list of agents \( A = [A_1, A_2, \ldots, A_{N-1}] \). The agent fitness is the circuit fidelity estimated based on its environmental state \((\pi, vcir, pcir)\), as shown in (4). In (4), \( \text{fid}(pcir) \) represents the fidelity of the partial physical circuit \( pcir \) and is obtained through (5); \( \text{fid}_{\text{worst}}(vcir) \), which is derived from (6), denotes the worst-case fidelity of the physical circuit corresponding to the remaining logical circuit \( vcir \).

\[
\text{fit}(agent) = \text{fid}(pcir) \cdot \text{fid}_{\text{worst}}(vcir) \quad (4)
\]

The first part of (5) is a penalty factor, which indicates that the fidelity of the quantum circuit decreases exponentially as the circuit depth increases. The second part of (5) is the fidelity product of all quantum gates (including the SWAP gates inserted so far) in \( pcir \). In (5), \( \text{dep}_{pcir} \) is the circuit depth of \( pcir \); \( |G_{ori}| \) is the number of two-qubit gates in the original logical circuit; \( D \) is the diameter of the coupling graph; \( |G_{ori}| \cdot (3D−2) \) denotes the worst-case circuit depth of the final physical circuit; \( \text{err}(\cdot) \) is the error rate of the two-qubit gate (CNOT gates in this paper), which comes from IBM’s device calibration data.

\[
\text{fid}(pcir) = e^{-\text{dep}_{pcir}} \cdot \prod_{g \in pcir} (1 - \text{err}(g)) \quad (5)
\]

(6) estimates the worst-case circuit fidelity of \( vcir \), where \( \epsilon_{\text{max}} \) denotes the maximum error rate of all possible two-qubit gates.

\[
\text{fid}_{\text{worst}}(vcir) = (1 - \epsilon_{\text{max}})^{|G_{ori}| \cdot (3D−2)} \quad (6)
\]

**Step 4.** Partition agents in groups. We divide the sorted list \( A \) into \( m \) groups \((S^0, S^1, \ldots, S^{m−1})\) so that each group has \( n \) agents. We assign the agents in \( A \) to different groups according to (7). An example of agent grouping is shown in Fig. 8, which divides 12 ordered agents into three groups.

\[
S^k = [S^k_j = A_{k+m(j−1)}, j = 0, 1, \ldots, n−1] \quad (7)
\]

where \( k = 0, 1, \ldots, m−1 \).

**Step 5.** Evolve the worst agent in each group (local information exchange). For the agent group \( S^k (k \in [0, m−1]) \), the agent with the worst fitness is \( S_{n−1}^k \), while the agent with the best fitness is \( S_0^k \). We decide whether to update \( S_{n−1}^k \) according to (8). In (8), \( r \) is a random number in \([0,1)\), \( \Delta G_{vcir} \) denotes the difference of \( S_{n−1}^k \) and \( S_0^k \) in terms of the gate count of their \( vcir \) property, and \( C \) is a predefined constant. (8) shows that the greater the difference between the best agent and the worst agent in the gate count or the fidelity, the higher the probability of evolving the worst agent. It is worth noting that we introduce the random number \( r \) in (8) to prevent the worst agent in each group from converging on the best agent (especially the best agent without a considerable advantage) too readily, thus ensuring the diversity of the agent population.
TABLE I

| Routing algorithm | Time complexity |
|-------------------|-----------------|
| HA [19]           | $O(|G|^2 \cdot |V|^3)$ |
| DL [13]           | $O(|G|^2 \cdot |V|^{2k})$ |
| Ours              | $O(N \cdot |G| \cdot |V|^4)$ |

D. Time complexity

In the worst case, an agent makes approximately $O(|G| \cdot D)$ decisions to complete the qubit routing task. In addition, an agent makes only one decision (in Step 6) in each loop. Therefore, Algorithm 2 has at most $O(|G| \cdot D)$ loops. In each loop, the decision-making and sorting of $N$ agents take $O(N \cdot |E| \cdot |V|/2)$ and $O(N \cdot \log N)$ time, respectively. Since $|E| \leq |V|/(|V| - 1)/2$, $D < |V|$, and $\log N$ is relatively small, the worst-case time complexity of Algorithm 2 is roughly $O(N \cdot |G| \cdot |V|^4)$. Table I gives the time complexity of several qubit routing approaches used in the experimental evaluation. As shown, the time complexity of our approach is polynomial in all parameters, so is HA’s, whereas DL’s time increases exponentially as the search depth $k$ grows. In addition, the time required by our algorithm is linear with the number of agents ($N$).

V. Experimental evaluation

In this section, to evaluate the effectiveness in improving circuit fidelity, we compare our multi-agent methodology with the state-of-the-art approach.

A. Experimental configuration

1) Algorithms for comparison: We compare the variation-aware multi-agent approach (MA) with the other three algorithms. First, to prove the effectiveness of the error-variation-aware strategy, we implement another multi-agent approach which is variation-agnostic (MA_NA). MA_NA is almost the same as MA, but it always assumes that all gates have the same error rate when calculating all fidelity-related equations (such as (3) and (8)). Second, to understand how much improvement MA can achieve in the circuit fidelity, we compare it with another variation-aware method (HA [19]) in the success rate of physical circuits. HA also aims to improve the overall circuit fidelity and show advantages over two approaches [11], [16] integrated into Qiskit. To obtain the experiment data of HA on the latest heavy-hex architecture, we download its code from Github and evaluate it with the same experimental configuration as our approach. Third, although the number of gates is not our first optimization goal, we also evaluate the gate count inserted by MA. To this end, we compare MA with the approach (DL [13]) that shows considerable improvements in reducing gates.

2) Target quantum devices: We use two well-known quantum devices of IBM as the target hardware platform. The first is a 16-qubit quantum processor, IBMQ_guadalupe. The topology of IBMQ_guadalupe is based on the latest heavy-hex lattice, which can provide a better Quantum Volume. Besides IBMQ_guadalupe, we also take another 20-qubit quantum processor, IBMQ_tokyo. Although BMQ_tokyo has already been deprecated due to high qubit frequency collision and high gate error rate, the experimental data of DL is given based on it. Therefore, we choose this architecture to compare with DL.

3) Benchmark circuit: We collect various benchmark circuits from the previous work [11], [13], [26]. For easy illustration, we divide all the benchmarks into three classes. The small-scale class refers to benchmarks without less than 100 gates; the medium-scale to those with 100 to 1,000 gates; and the large-scale to those with more than 1,000 gates.

4) Simulator of real quantum device: We use the simulator to execute quantum circuits rather than real quantum devices for three reasons. First, publicly available resources of quantum hardware are very scarce. Taking IBM as an example, they only provide public access to several 5-qubit devices. Such devices with very few qubits are not enough for demonstrating the advantage of automated approaches for quantum circuit mapping. Moreover, current quantum devices only allow very small-scale quantum circuits due to high gate error and low coherence time. In contrast, the simulator can support much larger circuits by adjusting the gate error or ignoring some physical resources. Therefore, experimenting on a simulator is more conducive to fully showing the performance differences of various algorithms.

We use the Qiskit Aer [27] to generate a noise model for a hardware device. This model takes the hardware calibration information as the input and thus can approximate the errors occurring on the actual device. We set two versions of noise models, that is, the basic one and the improved one. The basic model comes from the 16-qubit device IBMQ_guadalupe, while the improved model is obtained by reducing the gate error of the basic model by 10x. The 10x reduced gate error reaches the...
threshold of quantum error correction, so the improved model is a reasonable approximation of future quantum devices. In our experiment, we create a simulator based on the basic noise model for the small-scale benchmarks. Moreover, we also implement a simulator based on the improved noise model for the other circuits with hundreds of gates. However, this improved model alone is still insufficient to allow large circuits to output reliable results due to their long circuit depth. Therefore, the simulator for large circuits neglects the decoherence error. Furthermore, to focus on the impact of gate errors on circuit fidelity, both simulators also ignore the readout error, which happen at most once for each qubit during computation.

5) Figures of merit: Our approach aims to improve circuit fidelity, so the first merit is the probability of success trials (PST). As shown in (10), PST gives the success rate of running the physical circuit on the hardware. In the experiment, we run each physical circuit 8192 times. In addition, we also consider the number of gates and the circuit depth, another two important metrics of circuit quality.

\[
pst = \frac{\#\text{suc\_trail}}{\#\text{total\_trail}}
\]

6) Runtime environment: We implement our algorithm in Python and conduct all experiments on a personal computer with i7-4710HQ CPU and 16GB memory. In all experiments, MA and MA_{NA} both have 100 agents partitioned into 20 groups, and the constant \(C\) is set to 1. We choose the experimental configuration empirically to achieve a good trade-off of the circuit quality and the time. Our approach is publicly available on Github.

B. Effectiveness of error variation-aware strategy

To verify the effectiveness of the error variation-aware strategy in improving circuit fidelity, we use IBMQ_{guadalupe} as the target architecture and compare MA with MA_{NA} on various benchmarks. MA_{NA} assumes every two-qubit gate has the same error rate, so it gives preference to reducing the number of gates rather than improving the circuit fidelity. We can see from Table II that the number of additional gates required by MA_{NA} is less than or equal to that of MA. Although MA_{NA} has advantages in reducing gates, its circuit fidelity is much worse than MA. On all benchmarks, MA improves PST by 60.95% on average and 340.28% at most. Moreover, the improvement becomes more significant with the increase of the circuit scale, as shown in Fig. 9. Given that MA and MA_{NA} use the same multi-agent scheme, we attribute this improvement of MA to the error variation-aware strategy.

We also use MA and MA_{NA} to experiment on large-scale circuits. However, even with the simulator based on the improved noise model, the PST value is still too low, indicating the output is unreliable and meaningless. It confirms that quantum error correction is essential for the reliable execution of large-scale quantum circuits.

C. Evaluation of circuit fidelity

Both HA and MA consider the gate-error variation in the quantum circuit mapping process. We use IBMQ_{guadalupe} as the target platform to evaluate the efficiency of these two approaches in improving circuit fidelity. We show the experiment results in Table III and Fig. 10. Compared with HA, MA improves PST by 25.86% on average and 95.42% at most. Even on several benchmarks (mod5d264 and 4gt4-v0.72), MA requires more gates or circuit depth than HA, but it still shows better circuit fidelity. We owe the advantage of MA in improving the overall circuit quality to the multi-agent scheme. HA is a typical approach of quantum circuit mapping. It performs the locally optimal action in each step while discarding other possibilities. In contrast, MA updates the environment state of the agent with the worst fitness in each group while retaining the status of other agents. Combining with the local search (Step 5 of Algorithm 2) and global search (Step 3 of Algorithm 2), MA can evolve the overall circuit quality of the agent population gradually as the iteration goes.

Both HA and MA have polynomial time complexity, so the time overhead of both approaches is small for all benchmarks considered. In addition, since MA contains multiple agents, the time it consumes is generally more than that of HA.

D. Evaluation of gate overhead

DL does not consider the gate error issue and aims to minimize the number of gates. DL’s experiments use IBMQ_{tokyo} as the target platform. To compare with DL, we also give the experiment results of MA with IBMQ_{tokyo} as the target architecture, as shown in Table IV. Although MA takes circuit fidelity as the optimization goal, it can generally reduce the gate overhead. MA achieves improvement in gate count 16.81% on average and 66.67% at most. The advantage of MA in gate overhead comes from two main reasons. First,
the fitness function of the agent implicitly considers the gate overhead. The fitness decays as the number of gates increases. Second, the multi-agent scheme can effectively improve the overall fidelity of the circuit, and circuit fidelity is a comprehensive metric involving various factors, such as the number of gates, the circuit depth, and the gate error.

VI. DISCUSSION

As confirmed by the experiment, our multi-agent approach outperforms several noted methods in improving the circuit fidelity. The good performance of our approach mainly originates from the multi-agent cooperation mechanism. In each iteration, our approach discards the partial solution of the worst agent in each group but preserves the others’. In contrast, other approaches always keep a local optimal partial solution while ignoring other possibilities. Therefore, compared with other algorithms, our algorithm is less likely to fall into the local optimum. Moreover, although our approach aims to optimize the circuit fidelity, it can adapt to other optimization objectives (such as the number of gates and circuit depth) by adjusting the reward function and fitness function. Table IV gives the preliminary evidence that this method can also achieve improvement in the number of gates.

### Table II

| NO. | Benchmark circuits | name | n | gori | MA_NA | MA | Imprv |
|-----|-------------------|------|---|------|-------|----|-------|
| 1   | graycode6_47      | 6    | 7 | 0    | 95.70%| 98.73%| 5.89%|
| 2   | xor5_254          | 6    | 7 | 6    | 87.89%| 93.07%| 5.91%|
| 3   | 4mod5-v1_22       | 5    | 21| 9    | 85.94%| 85.74%| 7.33%|
| 4   | mod5mils_65       | 5    | 35| 18   | 64.45%| 69.34%| 2.16%|
| 5   | alu-v0_27         | 5    | 36| 21   | 71.19%| 71.34%| 0.24%|
| 6   | decod24-v2_43     | 4    | 52| 27   | 48.83%| 60.29%| 23.40%|
| 7   | mod5d2_64         | 5    | 53| 33   | 54.88%| 59.47%| 8.36%|
| 8   | 4gt13_92          | 5    | 66| 39   | 53.81%| 66.41%| 23.41%|
| 9   | alu-v0_26         | 5    | 84| 54   | 49.90%| 57.13%| 14.48%|
| 10  | 4gt5_76           | 5    | 91| 57   | 45.90%| 50.98%| 11.06%|
| 11  | qft_10            | 10   | 200| 96  | 67.29%| 98.52%| 22.50%|
| 12  | 4gt4-v0_72        | 6    | 258| 171 | 48.05%| 75.67%| 52.52%|
| 13  | sym6_316          | 14   | 270| 207  | 43.75%| 70.21%| 26.49%|
| 14  | rd53_135          | 7    | 380| 216  | 41.41%| 68.75%| 26.04%|
| 15  | mod8-10_177       | 6    | 395| 306  | 32.03%| 51.38%| 19.50%|
| 16  | cnt3-5_180        | 16   | 485| 348  | 21.39%| 54.39%| 154.34%|
| 17  | qft_16            | 16   | 512| 288  | 32.71%| 35.40%| 27.81%|
| 18  | rd53_133          | 7    | 580| 385  | 19.43%| 49.61%| 155.28%|
| 19  | 4gt4-v0_73        | 6    | 635| 261  | 31.84%| 63.09%| 98.16%|
| 20  | conl_216          | 9    | 954| 666  | 7.03% | 30.96%| 15.98%|

**name**: benchmark circuit; **n**: the number of qubits; **gori**: the number of gates in the original circuit; **gadd**: the number of additional CNOT gates inserted; **dep**: the depth of the circuit; **t**: the running time in seconds; **Imprv**: the improvement rate of MA in **t** compared to MA_NA.

### Table III

| NO. | Benchmark circuits | name | n | gori | HA | MA | Imprv |
|-----|-------------------|------|---|------|----|----|-------|
| 1   | graycode6_47      | 6    | 7 | 0    | 88.18%| 98.73%| 11.96%|
| 2   | xor5_254          | 6    | 7 | 6    | 69.82%| 93.07%| 33.29%|
| 3   | 4mod5-v1_22       | 5    | 21| 27   | 71.19%| 85.74%| 20.44%|
| 4   | mod5mils_65       | 5    | 35| 21   | 63.48%| 69.34%| 9.23%|
| 5   | alu-v0_27         | 5    | 36| 24   | 71.39%| 71.34%| 0.05%|
| 6   | decod24-v2_43     | 4    | 52| 33   | 51.37%| 60.29%| 17.30%|
| 7   | mod5d2_64         | 5    | 53| 33   | 56.84%| 59.47%| 5.58%|
| 8   | 4gt13_92          | 5    | 66| 46   | 52.54%| 66.41%| 26.39%|
| 9   | alu-v0_26         | 5    | 84| 66   | 51.41%| 57.13%| 27.97%|
| 10  | 4gt5_76           | 5    | 91| 96   | 38.67%| 50.98%| 30.82%|
| 11  | qft_10            | 10   | 200| 294  | 63.77%| 82.42%| 19.25%|
| 12  | 4gt4-v0_72        | 6    | 258| 189  | 67.19%| 75.68%| 16.52%|
| 13  | sym6_316          | 14   | 270| 348  | 58.89%| 70.21%| 19.24%|
| 14  | rd53_135          | 7    | 380| 252  | 59.28%| 68.75%| 19.58%|
| 15  | mod8-10_177       | 6    | 395| 432  | 44.63%| 56.15%| 25.28%|
| 16  | cnt3-5_180        | 16   | 485| 468  | 45.02%| 54.39%| 20.82%|
| 17  | qft_16            | 16   | 512| 864  | 29.88%| 58.40%| 30.52%|
| 18  | rd53_133          | 7    | 580| 528  | 35.16%| 49.61%| 14.45%|
| 19  | 4gt4-v0_73        | 6    | 635| 345  | 49.80%| 63.09%| 26.67%|
| 20  | conl_216          | 9    | 954| 801  | 24.02%| 30.96%| 8.86%|

**name**: benchmark circuit; **n**: the number of qubits; **gori**: the number of gates in the original circuit; **gadd**: the number of additional CNOT gates inserted; **dep**: the depth of the circuit; **t**: the running time in seconds; **Imprv**: the improvement rate of MA in **t** compared to MA.
Our approach contains multiple agents. Its time overhead increases linearly with the growth of the number of agents. As a result, our approach generally takes more time than other approaches, which is a disadvantage of our approach. However, since each agent makes its decision independently according to the environment state, we can implement the decision-making step (Step 6 of Algorithm 2) by parallel programming, so that all agents can make decisions simultaneously. In this way, we can solve this time issue.

In the decision-making step of our approach, we only consider the SWAP gates that reduce the physical distance for at least one front gate while ignoring other SWAP gates. Although those gates not considered may lead to better physical circuits, involving them in the decision-making process will seriously deteriorate the convergence of our approach, so we get rid of them. One of our future work is to consider more possible SWAP gates while ensuring the convergence of our approach.

There are three key parameters in our multi-agent approach. They are the constant value $C$ in (8), the number $m$ of agent groups, and the number $n$ of agents in each group, respectively. The assignment of parameter $C$ has a significant impact on the quality of the final physical circuit generated. If setting $C$ to 0, the worst individual in the population always evolves into the best individual, so that the whole population is filled with the best individual within a short time, resulting in the loss of population diversity and thus missing the possibility of exploring more potential solutions. Otherwise, if setting $C$ to a large value, it is scarcely likely for individuals to evolve, resulting in that the multi-agent cooperation scheme degenerates into the synchronous mode in which multiple agents complete the qubit routing task independently. Similarly, the two parameters, $m$ and $n$, have considerable influence on the convergence rate and the solution quality. Simply increasing $m$ and $n$ generally slows down the convergence rate but does not necessarily improve the solution quality. We observe from parameter-tuning experiments that when mapping various circuits to a specific quantum architecture, the optimal choice of these three parameters is generally not constant. However, for each parameter, there is a value interval that can bring high-quality solutions. In all the experiments of algorithm evaluation, we set each parameter approximately to the average of its value interval.

---

**TABLE IV**

| Benchmark circuits | DL | MA | Imprv |
|--------------------|----|----|-------|
| name               | $n$ | $g_{ori}$ | $g_{add}$ | $t$ | $g_{add}$ | $t$ | $g_{imp}$ |
| 4mod5-v1_22        | 5   | 21  | 0 | 0 | 0 | 0 | 0.00% |
| mod5mils_65        | 5   | 35  | 0 | 0 | 0 | 0 | 0.00% |
| alu-v0_27          | 5   | 36  | 9 | 0.07 | 3 | 0.03 | 66.67% |
| decod24-v2_43      | 4   | 52  | 0 | 0 | 0 | 0 | 0.00% |
| 4gt13_92           | 5   | 66  | 0 | 0 | 0 | 0.01 | 0.00% |
| ising_model_10     | 16  | 786 | 0 | 0 | 0 | 0.21 | 0.00% |
| ising_model_13     | 16  | 786 | 0 | 0 | 0 | 0.21 | 0.00% |
| vqft               | 15  | 343 | 72 | 5.01 | 372 | 5.85 | 40.95% |
| rd84               | 13  | 3439 | 630 | 19.85 | 498 | 2.96 | 15.69% |
| ising_model_25     | 11  | 3073 | 630 | 16.19 | 372 | 5.85 | 40.95% |
| alu-v1_10          | 10  | 200 | 153 | 21.06 | 129 | 2.96 | 15.69% |
| symbol_145         | 7   | 3888 | 513 | 2.93 | 402 | 5.85 | 40.95% |
| misexl_241         | 15  | 4813 | 786 | 24.62 | 450 | 5.97 | 42.75% |
| rd73_252           | 10  | 5321 | 1095 | 9.72 | 687 | 5.85 | 37.26% |
| cyclel0_2_110      | 12  | 6050 | 1194 | 10.93 | 897 | 12.16 | 24.87% |
| square_root_7      | 15  | 7630 | 1338 | 228.29 | 528 | 6.47 | 4.86% |
| sym_258            | 12  | 3073 | 630 | 16.19 | 372 | 5.85 | 40.95% |
| rd84_253           | 12  | 13658 | 2352 | 54.35 | 2088 | 29.30 | 11.22% |
| co14_215           | 15  | 4996 | 129 | 2.96 | 129 | 2.96 | 11.22% |
| sym9_193           | 11  | 34881 | 5589 | 70.29 | 4971 | 124.83 | 11.06% |

name: benchmark circuit; $n$: the number of qubits; $g_{ori}$: the number of gates in the original circuit; $g_{add}$: the number of CNOT gates inserted; $t$: the running time in seconds; $g_{imp}$: the improvement rate of MA in $g_{add}$ compared to DL.

---

Fig. 10. Comparison of MA and HA
If adjusting the parameters separately for each experiment, more improvement can be obtained. Therefore, compared with other heuristic algorithms, our approach requires an additional job of parameter adjusting, which is also a drawback.

VII. CONCLUSION

In this paper, we have proposed a quantum circuit mapping methodology based on multi-agent cooperation. This approach considers the variation of gate error on quantum hardware and aims to improve the overall circuit fidelity. It involves a population of multiple agents, which are arranged into various groups. Each agent starts from an initial environment state and evolves to the final state by making decisions stepwise. In each decision-making step, all agents exchange information according to a mechanism similar to SFLA, which integrates the local search and the global search. Based on the shared information, the agent with the worst fitness in each group can get a chance to evolve to the best-fitness agent in the group. After numerous iterations, this approach outputs the physical circuit of the agent with the best fitness. The experimental results confirm that this multi-agent scheme can effectively improve the overall circuit fidelity.

REFERENCES

[1] F. Arute, K. Arya, R. Babbush, D. Bacon, J. C. Bardin, R. Barends, R. Biswas, S. Boixo, F. G. Brandao, D. A. Buell et al., “Quantum supremacy using a programmable superconducting processor,” Nature, vol. 574, no. 7779, pp. 505–510, 2019.

[2] I. Tavernelli, A. Robert, P. Barkoutsos, and S. Woerner, “Resource-efficient quantum algorithm for protein folding,” Bulletin of the American Physical Society, vol. 65, 2020.

[3] D. J. Egger, R. G. Gutiérrez, J. C. Mestre, and S. Woerner, “Credit risk analysis using quantum computers,” IEEE Transactions on Computers, 2020.

[4] W. Jiang, J. Xiong, and Y. Shi, “A co-design framework of neural networks and quantum circuits towards quantum advantage,” Nature communications, vol. 12, no. 1, pp. 1–13, 2021.

[5] M. Y. Siraichi, V. F. d. Santos, S. Collange, and F. M. Q. Pereira, “Qubit allocation,” in Proceedings of the 2018 International Symposium on Code Generation and Optimization, 2018, pp. 113–125.

[6] A. Botea, A. Kishimoto, and R. Marinescu, “On the complexity of quantum circuit compilation,” in Eleventh Annual Symposium on Combinatorial Search, 2018.

[7] A. Zulehner and R. Wille, “One-pass design of reversible circuits: Combining embedding and synthesis for reversible logic,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 37, no. 5, pp. 996–1008, 2017.

[8] A. Kole, S. Hillmich, K. Datta, R. Wille, and I. Sengupta, “Im-proved mapping of quantum circuits to ibm qx architectures,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 39, no. 10, pp. 2375–2383, 2019.

[9] A. Cowtan, S. Dilkes, R. Duncan, A. Krajcnbrink, W. Simmons, and S. Sivarajah, “On the qubit routing problem,” arXiv preprint arXiv:1902.08091, 2019.

[10] A. M. Childs, E. Schoute, and C. M. Unsal, “Circuit transformations for quantum architectures,” arXiv preprint arXiv:1902.08102, 2019.

[11] G. Li, Y. Ding, and Y. Xie, “Tackling the qubit mapping problem for nisq-era quantum devices,” in Proceedings of the Twenty-Fourth International Conference on Architectural Support for Programming Languages and Operating Systems, 2019, pp. 1001–1014.

[12] H.-S. Zhong, H. Wang, Y.-H. Deng, M.-C. Chen, L.-C. Peng, Y.-H. Luo, J. Qin, D. Wu, X. Ding, Y. Hu et al., “Quantum computational advantage using photons,” Science, vol. 370, no. 6523, pp. 1460–1463, 2020.

[13] S. Li, X. Zhou, and Y. Feng, “Qubit mapping based on subgraph isomorphism and filtered depth-limited search,” IEEE Transactions on Computers, 2020.

[14] P. Zhu, Z. Guan, and X. Cheng, “A dynamic look-ahead heuristic for the qubit mapping problem of nisq computers,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 39, no. 12, pp. 4721–4735, 2020.

[15] L. Lao, H. van Someren, I. Ashraf, and C. G. Almudever, “Timing and resource-aware mapping of quantum circuits to superconducting processors,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021.

[16] P. Murali, J. M. Baker, A. Javaid-Ahbari, F. T. Chong, and M. Martonosi, “Noise-adaptive compiler mappings for noisy intermediate-scale quantum computers,” in Proceedings of the Twenty-Fourth International Conference on Architectural Support for Programming Languages and Operating Systems, 2019, pp. 1015–1029.

[17] S. S. Tannu and M. K. Qureshi, “Not all qubits are created equal: a case for variability-aware policies for nisq-era quantum computers,” in Proceedings of the Twenty-Fourth International Conference on Architectural Support for Programming Languages and Operating Systems, 2019, pp. 987–999.

[18] S. Nishio, Y. Pan, T. Satoh, H. Amano, and R. V. Meter, “Extracting success from ibm’s 20-qubit machines using error-aware compilation,” ACM Journal on Emerging Technologies in Computing Systems (JETC), vol. 16, no. 3, pp. 1–25, 2020.

[19] S. Niu, A. Suaa, G. Staffelbach, and A. Todri-Saniyal, “A hardware-aware heuristic for the qubit mapping problem in the nisq era,” IEEE Transactions on Quantum Engineering, vol. 1, pp. 1–14, 2020.

[20] B. Tan and J. Cong, “Optimality study of existing quantum computing layout synthesis tools,” IEEE Transactions on Computers, 2020.

[21] X. Zhou, S. Li, and Y. Feng, “Quantum circuit transformation based on simulated annealing and heuristic search,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 39, no. 12, pp. 4683–4694, 2020.

[22] H. R. Lourenco, O. C. Martin, and T. Stützle, “Iterated local search: Framework and applications,” in Handbook of metaheuristics. Springer, 2019, pp. 129–168.

[23] P. Zhu, S. Feng, and Z. Guan, “An iterated local search methodology for the qubit mapping problem,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021.

[24] J. C. Bansal, P. K. Singh, and N. R. Pal, Evolutionary and swarm intelligence algorithms. Springer, 2019.

[25] M. Eusuff, K. Lansey, and F. Pasha, “Shuffled frog-leaping algorithm: a memetic meta-heuristic for discrete optimization,” Engineering optimization, vol. 38, no. 2, pp. 129–154, 2006.

[26] A. Zulehner, A. Paler, and R. Wille, “An efficient methodology for mapping quantum circuits to the ibm qx architectures,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 38, no. 7, pp. 1226–1236, 2018.

[27] R. Wille, R. Van Meter, and Y. Naveh, “Ibm’s qiskit tool chain: Working with and developing for real quantum computers,” in 2019 Design, Automation & Test in Europe Conference & Exhibition (DATE). IEEE, 2019, pp. 1234–1240.
Weiping Ding (M’16–SM’19) received the Ph.D. degree in Computer Science, Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2013. In 2016, he was a Visiting Scholar at National University of Singapore (NUS), Singapore. From 2017 to 2018, he was a Visiting Professor at University of Technology Sydney (UTS), Ultimo, NSW, Australia. He is currently a Professor with the School of Information Science and Technology, Nantong University, China. His research interests include deep neural networks, multimodal machine learning, granular data mining, and medical images analysis. He served/serves as an Associate Editor of IEEE Transactions on Neural Network and Learning System, IEEE Transactions on Fuzzy Systems, IEEE/CAA Journal of Automatica Sinica, Information Sciences, Neurocomputing, Swarm and Evolutionary Computation.

Lihua Wei received the B.E. degrees in information and computation Science from Yancheng Teachers University, Yancheng, China, in 2006 and M.E. degrees in computer science from Jiangsu University, Zhenjiang, China, in 2011. She is currently a Lecturer with the Department of Information and Computing Science, Suqian University, China. Her current research interests include reversible logic design, quantum logic design, and computer-aided design of integrated circuits and systems.

Xueyun Cheng received the B.S. degree in computer science from Nanjing Normal University, Nanjing, China in 2001, and the M.S. degree in computational mathematics from Nanjing Normal University in 2007. She is currently an Associate Professor with the School of Information Science and Technology, Nantong University, China. Her current research interests include reversible logic synthesis, quantum information and quantum computation.

Zhijin Guan received the B.S. degree in mathematics from Harbin Normal University, China, in 1986, and the Ph.D. degree in Computer Application Technology from Nanjing University of Aeronautics and Astronautics, China, in 2005.

He is currently a Professor with the School of Information Science and Technology, Nantong University, China. His current research interests include quantum circuit logic design, secure computing, information-aware and computer-aided intelligent manufacturing, and computer-aided design of integrated circuits and systems.

Shiguang Feng received the B.S. degree in computer science and technology from Shandong Agricultural University, China, in 2006, and the Ph.D. degree in logic from Sun Yat-sen University, China, in 2012, and the Doctor of Natural Science degree in computer science from Leipzig University, Germany, in 2016.

He is currently an Associated Professor with the School of Information Science and Technology, Nantong University, China. His current research interests include complexity theory and mathematical logic.