Methodology for Designing Hardware for Measuring Parameters of a Digital Signal

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Abstract. In the production of various devices, various problems can arise, leading to the appearance of defects, both explicit and latent. This may be due to both poor quality materials and imperfect technology. To identify defects, devices are tested. If the device uses a digital signal transmission at high frequencies, it is usually considered sufficient to check the functioning of the individual components using technological programs. But at high transmission frequencies, or due to defects, the digital signal is distorted, and in devices where there is no error control, violations of the signal integrity during transmission can lead to failures and failures. Moreover, under normal conditions, the signal can meet the requirements, and in difficult conditions, go beyond the permissible limits. If an individual instance of a device can be susceptible to such failures, this can be identified in more detail by examining the signals flowing through its circuits. The most obvious way requires an oscilloscope, on the screen of which a person looks at the parameters of such a signal, time and amplitude characteristics. This is a very slow operation, so optimization might be the next step. For example, the use of flying probes, or probes with commutation, recording and automatic comparison of oscillograms with the exemplary one. In any case, these tests require equipment operating at frequencies much higher than the circuit itself, which means that at high baud rates, such equipment starts to be expensive.

1. Introduction
When developing measuring equipment, methodological restrictions are imposed restrictions caused by the imperfection of individual elements of the circuit, the mutual influence of individual parts of the device. The modern element base provides a wide range of electronic components, ranging from simple ones used in household equipment, and ending with precision parts and components for special applications (environmental conditions, requirements for accuracy, power, dimensions). Of course, the higher the demands placed on the individual elements, the higher the price of the final device. That is why special attention should be paid to the choice of the element base. In addition, functional elements that have different principles of operation, but the same functional purpose, can affect the resulting data. This study proposes a technique for measuring the parameters of a digital signal during the design and production of prototypes of printed circuit boards.
2. Measurement scheme
The functional diagram of the device for measuring the parameters of a digital signal is shown in Figure 1. The measured signal enters the input device, which converts it to the level required for further conversion. The sample and hold device captures and stores the signal value at a specific point in time. The need for it is due to the fact that the conversion has a certain duration, and the need for the measured signal is present all the time of conversion, and the signal itself can change during this time. From the sampling and storage device, the signal is fed to the analog-to-digital converter (ADC) input. Integrated ADCs may have their own sampling and storage device, but it may not meet the specified parameters. In an analog-to-digital converter, the continuous value of the input signal is converted into discrete and supplied to the data processing unit. The sample-and-hold device and the ADC are synchronized by the sampler. This node can be either separate or included in the data processing unit. In any case, the main requirement for the node is to generate a signal with an interval with a given random component. The data processing unit distributes the samples over intervals, analyzes the received data and makes a decision on compliance with the specified parameters. Depending on the degree of automation of the production stage in which the measuring device is used, for further use the results can be presented visually (analysis by the operator), saved on the recording device (in the case of long-term tests), or converted into a signal for a terminal device that can produce separation manufactured units according to the specified parameters (for example, do not pass the defective ones further along the conveyor).

![Figure 1. Functional diagram of the measuring device.](image)

3. Analog to digital conversion
According to the principle of operation, analog-to-digital converters are divided into three groups: readout ADC, comparison and subtraction ADC, integral ADC. ADC readings are divided into parallel, serial-parallel, and pipelined. All of them are distinguished by high speed, but also either by a large number of individual elements (parallel and serial-parallel ADCs), or by high requirements for their accuracy (pipelined ADCs), therefore they are used only when a high sampling rate is needed (hundreds of megahertz, units of gigahertz ). Figure 2 shows a block diagram of a parallel ADC [1]. A series of $2N-1$ comparators are used, taking a reference voltage from a resistive divider and comparing it to the voltage being measured. At the output, we have a $2N$-1-bit code, which is called thermometric (all the digits are uniformly filled with ones or zeros with the growth of the measured value), which is then converted to binary, often with an intermediate conversion to a unitary one (1 out of $2N$).
For the developed method, it is of interest that the unitary code is a sample already sorted by some intervals, which can significantly simplify the rest of the scheme. However, ADCs with a unitary output are not among the available solutions, and the manufacture of parallel ADCs on discrete components can be difficult for a large number of bits. But for a small number of intervals, and as a consequence of the bits, the use of a parallel ADC needs separate consideration. Non-integrating balancing ADCs are most widely used due to simple circuitry, a small number of precision elements, and good performance parameters. When converting to such ADCs, the measured voltage is compared with the exemplary one, changing according to a known law (more often linear) formed in the feedback circuit (Fig. 3).

The way the signal is balanced depends on the conversion time requirements and external commutation. So, for example, ADCs of sweeping balances perform well in multichannel circuits, with competent channel switching, allowing to achieve greater performance than simply switching inputs each cycle. Tracking ADCs do a good job of slowly changing signals. The most widespread in integrated performance, both in the form of individual microcircuits and as part of special microcontrollers, programmable logic circuits, systems on a chip, are ADCs of bitwise balancing. They have a fixed and, on average, a shorter conversion time (provided that the clock frequencies are equal, for the scanning ADCs the maximum number of clock cycles is equal to the number of samples 2N, and for the bitwise balancing ADC it is fixed for each execution, taking from the most efficient ones from N + 1 clock cycles, where N is the number of bits) and simple circuitry. It is these ADCs that are considered as the main ones for use in hardware implementations of the developed method. The principle of operation of integrating ADCs is based on measuring the time it takes to reach the threshold level by the voltage at the integrator's output, or on measuring the signal frequency after voltage-frequency conversion. One way or another, we are talking about measuring the accumulated parameter before a certain condition occurs. Hence, one of the requirements is high performance of the elements that keep the count: counters and their auxiliary logic. Integrating ADCs have filtering properties, they are immune to short-term voltage surges, which, together with a rather long conversion time, forces an increase in the sample-and-hold device capacity, and this negatively affects the timing characteristics of the measuring hardware. Despite this, integrating ADCs can be used for this method,
if the architecture of the processing device has advantages in measuring time or frequency. Of all the ADCs considered, the most suitable for use in meters for digital signal parameters is a bit-balanced ADC. This is due to the wide range of integrated circuits, and wide switching capabilities, and with the minimum number of external precision elements, in comparison with other integrated ADCs.

4. Sampling and storage

Sample and storage devices are designed to maintain the level of the measured signal during conversion. The need for this is mainly dictated by the fact that if the level changes during the conversion process, an erroneous result may appear, especially in the ADC of bitwise balancing. Most modern integrated ADCs have their own sampling and storage device. This saves development time and reduces the overall dimensions of the final device. However, if the ADC is designed for small sampling rates (10..100 thousand samples per second), then the sampling and storage device may not be designed for a rapidly changing signal, working as a low-pass filter. In this case, as well as in the absence of a ready-made one, it is necessary to develop a separate sampling and storage device. The simplest device for sampling and storage is an analog switch and a capacitor (Fig. 4).

![Figure 4. Sample and storage device model.](image)

This diagram perfectly illustrates how any analog sample and hold circuit works. Part of the time when the SA switch is closed, the capacitor C0 is charged (or discharged) from the source, when the SA switch is opened, the capacitor remains charged to the level that the signal Uin had at the moment of opening. However, when designing devices, it should be borne in mind that a capacitor connected to the measured circuit contributes to its parameters, besides, the initial charge current can be very large, which is likely to distort the signal. Therefore, between the input and the key, it is necessary to install a buffer stage - a repeater. Similarly, for the output of the device - a follower is needed to reduce the effect of the input resistance of the ADC and to reduce and make the self-discharge value known (Fig. 5). Therefore, it is preferable to use elements made by CMOS technology, due to their high input and low output resistance.

![Figure 5. Sampling and storage device.](image)

Some digital signal parameters may require additional quantities to compute, such as frequency (or number of hops) or tracking falling and rising edges. As a principle for measuring frequency, it is convenient to use the principle of counting pulses for a certain time. Provided that a stable frequency source is used, high accuracy can be obtained, and the counting principle itself requires only a few high-frequency counting stages, and the integrated circuits of the remaining stages can be made using the same technology as the rest of the device. To track the falling and rising edges, a device is needed that would give information about the sign of the derivative of the signal with respect to time. It is possible to find out the sign of the derivative with sufficient accuracy by comparing two signal values separated by a sufficiently short time interval $\Delta t$. For these purposes, you can use a comparator with a delay element connected to one of the inputs (Fig. 6).
Figure 6. Functional diagram of the gradient detector.

A single-stage RC filter can be used as a delay element. Its parameters are selected so as to minimize the influence of external interference and high-frequency noise component, but at the same time get a timely response to the beginning of the pulse front [2]. The voltage at the output of the comparator can be calculated using the formula:

\[
U_{\text{out}}(t) = K \left[ U(t) \pm e^{-\frac{t}{\tau}} \int_{0}^{t} \frac{e^{-\frac{\xi}{\tau}} U(\xi)}{RC} d\xi + U_{c0} \right],
\]

(1)

where \(U(t)\) is a function of the dependence of the input voltage voltage on time, \(U_{c0}\) is the initial voltage across the capacitor of the RC filter, \(K\) is the gain of the comparator.

The actual value of the output voltage is limited by the supply voltage. The reaction delay can be calculated by solving the inequality:

\[
\frac{U_{c0}}{K} \leq \left[ U(t-\Delta t) \pm e^{-\frac{\Delta t}{\tau}} \int_{0}^{\Delta t} \frac{e^{-\frac{\xi}{\tau}} U(\xi)}{RC} d\xi + U_{c0} \right],
\]

(2)

The response delay should generally not exceed the maximum capture time. To simplify calculations, as a function of the signal \(U(t)\), you can take a linear function in a suitable section, with a slope corresponding to the maximum rate of rise (fall) of the signal.

Typically, the output of an ADC is a signed or unsigned integer. Processing integers requires little resources, so if, in the end, you need to convert values to floating point numbers, then it is better to do it either at the very end of all conversions, or when operations related to multiplication and division can cause a painful error for numbers with a fixed comma. First of all, the operation of distributing samples over intervals is performed. The value can be distributed both directly upon receipt, for example, with a fixed width of the interval, and at the end of the accumulation of the entire volume, for example, with a fixed number of samples per interval, when sorting is required. If a microprocessor or microcontroller is used for data processing, then for distribution with a fixed width of the interval, instead of a large number of conditional operations, it makes sense to use index transitions (with a fixed width of the interval known at the design stage), index arrays (with an unknown number of intervals with the same width) and integer binary search algorithm (at intervals of different widths). When using a fixed number of samples per interval, one of the sorting algorithms should be used. After receiving a sorted sample, the parameters are calculated. The results can be recorded without processing into a storage device for further analysis, presented as visual information for the operator, or on their basis the data processing device makes a decision about the quality of the investigated product and issues it to the terminal device, which can sort, notify the operator, perform other actions provided by the technological process [3].

5. Stacked measurement

Let there be a parallel ADC with \(N\) comparators, which produces an \(N\)-bit thermometric code (Fig. 7). If the thermometric code is converted to a unitary code (1 of \(N\)), then at each output \(n\) unit will be
present only the time that this or that signal is in the interval from the threshold of the comparator \( n \) to the threshold of the comparator \( n + 1 \) (or the reference voltage for \( n = N \)).

**Figure 7.** Parallel ADC with unitary code output.

If each of the outputs of the decoder controls the switch connecting the current source and the capacitor, then after a certain time, the voltage across the capacitor \( C_n \) will be proportional to the time that the signal was in the interval \( n \) [4]. Thus, the transformation is continuous, without time quantization, without using sorting and comparisons, the intervals are set by the parameters of the elements that set the threshold for the comparators. In this implementation, the number of threshold elements is equal to the number of intervals, which greatly simplifies the construction of the transducer. Considering the absence of time quantization, and the fact that the time spent in the interval is a continuous value, the output voltage across the capacitors is also a continuous value and depends on the quality of the elements included in the circuit. In addition, the error associated with the randomness of the sample is eliminated. The disadvantages of such an implementation are the impossibility of dynamic restructuring of intervals and changing their number, the presence of a large number of measurement points, high requirements for driving elements, current sources and storage capacitors [5].

6. **References**

[1] Kang S, Moon J 2012 In Proceedings of the IEEE International Conference on Communications (ICC) Parallel LDPC Decoder Implementation on GPU based on Unbalanced Memory Coalescing

[2] John L 2007 Volakis, Antenna Engineering Handbook, Fourth Edition, McGraw-Hill Education (New York)

[3] Yu L, Barash L, Schur N 2013 Software Engineering On the generation of parallel streams of pseudo-random numbers pp 24-32

[4] Bauke H, Mertens S 2007 Physical Review E, Random Numbers for Large Scale Distributed Monte Carlo Simulations

[5] Bauke H 2014 Tina’s Random Number Generator Library

[6] Barnault L, Declercq D 2003 Inform. Theory Workshop, Fast Decoding Algorithm for LDPC over GF(2q) pp 70-73

[7] Yorozu Y, Hirano M, Oka K and Tagawa Y 1982 Electron spectroscopy studies on magneto-optical media and plastic substrate interface *IEEE Transl. J. Magn. Japan* vol. 2 pp 740-741