MIME: Adapting a Single Neural Network for Multi-task Inference with Memory-efficient Dynamic Pruning

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ABSTRACT
Recent years have seen a paradigm shift towards multi-task learning. This calls for memory and energy-efficient solutions for inference in a multi-task scenario. We propose an algorithm-hardware co-design approach called MIME. MIME reuses the weight parameters of a trained parent task and learns task-specific threshold parameters for inference on multiple child tasks. We find that MIME results in highly memory-efficient DRAM storage of neural-network parameters for multiple tasks compared to conventional multi-task inference. In addition, MIME results in input-dependent dynamic neuronal pruning, thereby enabling energy-efficient inference with higher throughput on a systolic-array hardware. Our experiments with benchmark datasets (child tasks)- CIFAR10, CIFAR100, and Fashion-MNIST, show that MIME achieves ~3.48x memory-efficiency and ~2.4 ~ 3.1x energy-savings compared to conventional multi-task inference in Pipelined task mode.

KEYWORDS
Multi-task inference, dynamic pruning, systolic-array, memory reduction & energy-efficiency

1 INTRODUCTION
Deep Neural Networks (DNNs) have increasingly been deployed for various applications ranging from computer vision, voice recognition to natural language processing and so forth [7, 9, 12]. Furthermore, in today’s era of Internet-of-Things, many of these applications need to operate in highly resource-constrained environments. As a result, designing efficient hardware accelerators for memory and energy-efficient implementation of DNNs has become imperative [1–3, 22].

Data such as images can have several common features that can be leveraged for multiple classification tasks. Thus, recent years have witnessed efforts to shift from the multi-task learning paradigm [6, 15, 19, 20]. To achieve multi-task learning, several algorithms have been proposed that use transfer learning. Traditional transfer learning techniques train a DNN model for a parent task (or dataset) and then fine-tune its parameters for multiple downstream tasks (or datasets) called child tasks [26]. This reduces the complexity of training a different neural network from scratch for every task.

Conventional task-specific fine-tuning during multi-task learning assumes the following: (i) every child task generates a new set of weight parameters. During inference on hardware, all of these parameters need to be stored in the off-chip DRAM that pose huge memory overhead (see blue curve in Fig. 1). (ii) for multi-task inference, a batch of inputs fed into a DNN on hardware consists of data (images) that belong to a single task (referred to as Singular task mode) [17, 18, 28]. However, let us consider a more realistic scenario wherein, a batch of inputs can have images belonging to multiple tasks in an interleaved fashion (referred to as Pipelined task mode). In this case, the number of accesses to the DRAM for fetching the task-specific weight parameters would increase significantly leading to high energy overhead.

As can be seen in Fig. 2(a) & (b), each neuron in a DNN is associated with a task-specific threshold parameter (t) against which the Multiply-and-Accumulate (MAC) output (y) of the neuron is compared and a binary mask (0 or 1) is generated. If the mask has a value equal to 1, the corresponding neuron is active and produces y as its output activation. Otherwise, the neuron is pruned and produces a zero activation value. Thus, based on the input and the child task being processed by the DNN, the corresponding set of threshold parameters are selected and different sub-networks within the same DNN model are activated during inference (shown in Fig. 2(b)). We will see in the upcoming sections, this input and task-dependent dynamic neuronal pruning manifests as reduction in computational and communication energies as well as increased throughput on hardware [31].

MIME requires the storage of threshold parameters specific to each child task in conjunction with W(parent) in the DRAM for inference. This is in contrast to storing a new set of fine-tuned weight parameters for every child task during conventional multi-task scenario. In this work, we show that the DRAM storage for...
In summary, the key contributions of this work are as follows:

- This work, for the first time, raises a practical/realistic question for multi-task scenarios, that is, How to improve energy-efficiency during inference when inputs in a batch belong to different tasks (i.e. Pipelined task mode)? We propose MIME to enable energy and memory-efficient multi-task DNN inference on hardware. In MIME, the weight parameters of a parent task $W_{parent}$ are reused during the inference of multiple child tasks.

- We propose an algorithm to learn the threshold parameters corresponding to the child tasks ($T_{child}$) that are used in conjunction with $W_{parent}$ for inference without huge training overhead.

- We evaluate the performance of MIME on Eyeriss-systolic-array based hardware architecture (in 65 nm CMOS technology) [3, 30] under two modes, namely Singular task mode and Pipelined task mode. For both the modes of operation, we adopt an output stationary (OS) dataflow for inference. We conduct ablation studies to suggest important design metrics for selecting the best trade-off between compute energy- and memory cost.

- We perform comprehensive experiments using a VGG16 DNN [24] on benchmark datasets—Imagenet [12] as parent task and, CIFAR10, CIFAR100 [11] and Fashion-MNIST [29] as child tasks. We find that in the Pipelined task mode, MIME leads to significantly lower DRAM accesses compared to the conventional multi-task inference scenario, thereby bringing in huge layerwise energy savings ($\approx 2.4 \times 3.1x$). MIME also leads to a significant layerwise improvement in throughput during inference ($\approx 2.8 \times 3.0x$), primarily attributed to the dynamic neuronal sparsity.

### 2 RELATED WORKS

**Conventional transfer learning:** There has been a body of work on transfer learning wherein the weight parameters of a DNN model trained for a parent task are fine-tuned to run a downstream child task [26]. On similar lines, knowledge distillation works enable learning of smaller child models by distilling the loss function of the larger parent model [8, 10]. Such approaches have been shown to significantly reduce the training complexity of the child models. However, when there are several downstream tasks with each task having its own set of weight parameters, traditional transfer learning or distillation approaches do not provide memory and energy-efficient solutions to store and access the parameters during inference on hardware.

**Pruning strategies:** Several pruning techniques have been devised to generate highly compressed and sparse DNNs. They can be categorized as static (only weights are pruned) or dynamic (both weights and activations are pruned). The sparse DNNs when deployed on hardware lead to high memory and energy-efficiencies during inference [4, 13, 25, 27, 31–33]. However, all prior pruning approaches only cater to a single task scenario with the pruning strategy defined for the given dataset/model.

**Continual learning:** There have been recent works on multi-task continual learning wherein data from numerous tasks (or numerous segments of a task) are sequentially shown to learn a DNN model [21, 23]. In contrast, MIME works under the assumption that the entire data for a child task is available. MIME simultaneously learns task-specific threshold parameters of the parent DNN model for multiple downstream child tasks keeping the parent weights frozen.

Table 1 provides a qualitative comparison between MIME and the above related works highlighting our key contributions.

### 3 METHODOLOGY AND SYSTEM IMPLEMENTATION

#### 3.1 Task-specific threshold generation for MIME

Consider a DNN model trained for a parent task with its weight parameters denoted by $W_{parent}$. Our objective is to carry out inference using $W_{parent}$ across multiple downstream tasks or child tasks. We, thus, propose an algorithm to train a set of threshold parameters specific to a child task ($T_{child}$), used in conjunction with $W_{parent}$. Training the threshold parameters with the child datasets includes forward and backward propagation through the DNN model as described in Fig. 3(a). During the forward pass, after getting the Vector-Matrix-Multiplications (VMMs) with DNN weights ($W_{parent}$) and input activations ($X$), we compare the VMM value of the $i^{th}$ output neuron ($y_{ij}$) with a threshold parameter ($t_i > 0$) to generate...
which would otherwise result in convergence issues. At the end of \( t \) (equation 1), we estimate the gradient using a piece-wise linear via masking the VMM outputs (parameters (threshold parameters are respectively loaded into the weight and

tecture \[3, 30\], we consider two modes of inference: Pipelined task mode and Pipelined task mode.

3.2 Implementation of MIME on a systolic-array hardware architecture during inference. The memory hierarchy includes: (1) accessing data from the off-chip DRAM and storing into the cache, (2) fetching task-specific parameters and activations from the cache to the spads, and (3) performing MAC operations in the PEs by fetching operands from the spads.

![Flow diagram showing the forward (blue) and backward (red) propagation steps involved in training task-specific threshold parameters for MIME.](image)

\[ L = L_{CE} + \beta \cdot L_t \] (3)

where, \( \beta \) is a hyper-parameter that assumes a value of \( 1 \times 10^{-6} \) for training with a batch size of 100. \( L_{CE} \) denotes the cross-entropy loss and the threshold-regularization term \( (L_t) \) is defined as:

\[ L_t = \sum_{l=0}^{\text{layers}} \sum_{i=1}^{n} \exp(t_i) \] (4)

The threshold-regularization term \( (L_t) \) prevents the threshold parameters \( (t_i) \) from assuming arbitrarily large positive values, which would otherwise result in convergence issues. At the end of the training for \( n \) child tasks, MIME yields the parameters: \([W_{parent}, T_{child-1}, T_{child-2}, \ldots, T_{child-n}] \) that need to be stored for inference on hardware. It is evident that the masking due to thresholds will yield input-dependent dynamic sparsity at every DNN layer that translates to energy savings and high throughput during hardware implementation.

3.2 Implementation of MIME on a systolic-array hardware

To understand the implications of generating task-specific thresholds for carrying out inference on a systolic-array hardware architecture \([3, 30]\), we consider two modes of inference: Singular task mode and Pipelined task mode.

As shown in Fig. 3(b), for a given DNN layer during inference, first the corresponding weight (of the parent task) and task-specific threshold parameters are respectively loaded into the weight and threshold caches and the previous layer’s non-zero activations are loaded into the activation cache from the off-chip DRAM. For the Pipelined task mode with MIME, even if the subsequent non-zero activations in the queue belongs to a different task (dataset), the weight parameters of the given DNN layer need not be reloaded. In contrast, in the conventional multi-task scenario wherein, each task has its own set of weight parameters, there has to be multiple fetch-load cycles of weight parameters. In MIME, pertaining to the task, only the threshold parameters need to be reloaded into the threshold cache from the DRAM, which typically has a lesser overhead than reloading weight parameters to the weight cache. This translates to higher energy-savings as we will see in the upcoming sections.

Next, to perform the VMM or MAC operations in the PEs, the operands are fetched from the caches to the scratchpads (spads) or local registers situated inside the PEs. Here, the fetches from the cache are carried out only for those weights which interact with the non-zero activations for MAC operations. Thus, the layerwise neuronal sparsity arising due to threshold-induced dynamic masking results in both compute energy and memory access savings due to zero-skipping. Also, we follow an OS dataflow in carrying out MAC operations in the PE array. Since, each output neuron of a convolutional layer is associated with a threshold parameter, OS dataflow helps reduce repeated accesses of the threshold parameters as well as the partial sums to and from the main memory. Inside the PEs, there are MAC computation and comparator (CMP) units that fetch operands from the local spads and compute the final masked output neuronal activations that are stored back into the off-chip DRAM.

4 EXPERIMENTS

We take a trained VGG16 DNN with Imagenet dataset (parent dataset) with 73.36% test accuracy, and obtain the \( W_{\text{parent}} \) parameters. Next, using \( W_{\text{parent}} \), we train the VGG16 DNN for the child tasks (datasets), namely CIFAR10, CIFAR100 and Fashion-MNIST (F-MNIST) to obtain \( T_{child-1}, T_{child-2} \) and \( T_{child-3} \) respectively. Note, CIFAR10 and CIFAR100 are two similar datasets or tasks consisting of RGB images of size \( 32 \times 32 \), while, the F-MNIST dataset consists of grayscale images of size \( 28 \times 28 \). We considered such different types of datasets to show that our method is transferable from one parent task to different kinds of child tasks. Training for the task-specific threshold parameters was carried out using the methodology shown in Fig. 3 for 10 epochs using ADAM optimizer with a learning rate of \( 1e-3 \). Thus, MIME incurs very low training overhead. The DNN test accuracies for the child tasks have been
reported in Table 2. We also present the average layerwise sparsity in the output activations, observed with MIME, for the VGG16 DNN across different child tasks in Table 2.

To analyze the benefits of MIME on hardware, we present the test accuracies and layerwise neuronal sparsities for our baseline models in Table 3. Note, the baselines are generated by normally training the VGG16 DNN on three child datasets and obtaining the weights and threshold parameters of the parent task (Imagenet) and its child tasks (CIFAR10, CIFAR100 and F-MNIST) for MIME. As discussed in Section 1, we find that for the parent task and its downstream child tasks, the memory savings with respect to conventional multi-task inference approach is $> n \times$ as has been annotated in the figure. For the Imagenet task along with CIFAR10, CIFAR100 and F-MNIST tasks (3 child tasks), we obtain $\sim 3.48 \times$ savings in DRAM storage. The absolute value of the savings in off-chip DRAM storage with MIME increases further with increase in the number of child task for the given parent task. This makes our approach highly memory-efficient.

Next, we implement the above models on the systolic-array architecture. For inference in Singular task mode, we consider a batch consisting of three input images, each belonging to one task (say, CIFAR10) and present our hardware analyses for this batch of inputs (see Section 5.2). For Pipelined task mode, we again consider a batch of three input images in succession belonging to three different tasks or datasets - CIFAR10, CIFAR100 and F-MNIST (see Section 5.3). In this study, we assume that the hardware has knowledge about the task it is currently processing and thus, can accordingly fetch the right set of parameters from the memory to the MAC compute units for inference. Unless otherwise stated, the specifications pertaining to the systolic-array accelerator are values listed in Table 4. Note, all energy values have been normalized with respect to the absolute energy of 1 MAC operation in the PE.

Table 2: Table showing test accuracy and average layerwise neuronal sparsity for VGG16 DNN for the child datasets (CIFAR10, CIFAR100 and F-MNIST) using MIME

| Child task | Test Accuracy (%) | conv2 | conv4 | conv5 | conv7 | conv8 | conv9 | conv10 | conv12 | conv13 | conv14 | conv15 |
|------------|-------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| CIFAR10    | 83.57             | 0.6493| 0.6081| 0.6587| 0.6203| 0.6233| 0.6449| 0.6679| 0.6477| 0.6553| 0.6855| 0.657  |
| CIFAR100   | 59.42             | 0.6522| 0.5951| 0.6373| 0.6100| 0.6121| 0.6279| 0.6374| 0.6388| 0.6703| 0.6703| 0.6571 |
| F-MNIST    | 88.36             | 0.6075| 0.5634| 0.6138| 0.5991| 0.5959| 0.6017| 0.6204| 0.6014| 0.6125| 0.6138| 0.6287 |

Table 3: Table showing test accuracy and average layerwise neuronal sparsity for VGG16 DNN for the baseline models (CIFAR10, CIFAR100 and F-MNIST) using conventional multi-task inference

| Baseline Child task | Test Accuracy (%) | conv2 | conv4 | conv5 | conv7 | conv8 | conv9 | conv10 | conv12 | conv13 | conv14 | conv15 |
|---------------------|-------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| CIFAR10             | 84.25             | 0.4983| 0.4506| 0.5390| 0.5015| 0.5097| 0.5341| 0.5635| 0.5358| 0.5420| 0.5627| 0.5608 |
| CIFAR100            | 60.55             | 0.5030| 0.4586| 0.5399| 0.5069| 0.5129| 0.5333| 0.5633| 0.5345| 0.5449| 0.5842| 0.6002 |
| F-MNIST             | 90.12             | 0.5114| 0.4796| 0.5488| 0.5230| 0.5260| 0.5329| 0.5503| 0.5280| 0.5343| 0.5507| 0.5820 |

Table 4: Table showing system parameters for the systolic-array hardware. Here, $\epsilon_{DRAM}$, $\epsilon_{cache}$ and $\epsilon_{reg}$ are respectively the energies corresponding to 1 DRAM, 1 cache and 1 spad based memory-access normalized w.r.t. energy of 1 MAC operation ($\epsilon_{MAC}$) [3]

| Parameter                        | Value       |
|----------------------------------|-------------|
| Technology                       | 65 nm CMOS  |
| Precision ($W$, $X$, $A$, $T$)   | 16 bits     |
| Cache size ($Activation$, Weight, Threshold) | 156 KB     |
| Spad size                        | 512 B       |
| PE array size                    | 1024        |
| $\epsilon_{DRAM}$, $\epsilon_{cache}$, $\epsilon_{reg}$, $\epsilon_{MAC}$ | 200X, 6X, 2X, 1X |

Figure 4: Plot showing savings in off-chip DRAM storage due to MIME (red) compared with conventional multi-task inference scenario (blue)

5 RESULTS AND DISCUSSION

5.1 Reduction in off-chip DRAM storage

Fig. 4 presents the total off-chip DRAM storage needed for storing the weights and threshold parameters of the parent task (Imagenet) and its child tasks (CIFAR10, CIFAR100 and F-MNIST) for MIME. As discussed in Section 1, we find that for the parent task and its $n$ downstream child tasks, the memory savings with respect to conventional multi-task inference approach is $> n \times$ as has been annotated in the figure. For the Imagenet task along with CIFAR10, CIFAR100 and F-MNIST tasks (3 child tasks), we obtain $\sim 3.48 \times$ savings in DRAM storage. The absolute value of the savings in off-chip DRAM storage with MIME increases further with increase in the number of child task for the given parent task. This makes our approach highly memory-efficient.

5.2 Results for Singular Task Mode

In Fig. 5, we plot the energy distribution (normalized w.r.t. energy of 1 MAC operation) of the convolutional layers of the VGG16 DNN processing a batch of 3 input images from the CIFAR10 dataset. The overall layerwise energy is distributed among total energy due to MAC computations ($\epsilon_{MAC}$), cache accesses ($\epsilon_{cache}$), scratchpad accesses in the PEs ($\epsilon_{reg}$) and the total energy expended during MAC computations ($\epsilon_{MAC}$). The results are presented for three
5.2 Results for Singular Task Mode
In the Singular task mode, the energy savings in case of MIME with respect to Case-1 or Case-2 are primarily attributed to the dynamic neuronal pruning at each layer. Quantitatively, we obtain \( \sim 1.8 \) – 2.5x energy savings with MIME with respect to baseline Case-1 and \( \sim 1.07 \) – 1.3x savings with respect to baseline Case-2. However, it is clear from Fig. 5 that the benefits of reduced DRAM accesses and hence, lower values of \( E_{DRAM} \) cannot be seen for the Singular task mode scenario with MIME. In fact, \( E_{DRAM} \) of MIME is slightly higher than the corresponding \( E_{DRAM} \) of Case-2 for each layer. This is because in addition to weight parameters, the threshold parameters also need to be fetched from the DRAM for MAC operations. Thus, to reap the benefits of MIME approach, we consider the Pipelined task mode of inference in the next section.

5.3 Results for Pipelined Task Mode
In Fig. 6, we plot the energy distribution of the even numbered convolutional layers of the VGG16 DNN for the Pipelined task mode. Since in the Pipelined task mode with OS dataflow MIME greatly reduces repeated accesses to the off-chip DRAM for weights as well as thresholds, MIME dramatically reduces the layerwise computation and communication energies, with savings being more significant for \( E_{DRAM} \) and \( E_{reg} \) based memory access energies in latter convolutional layers. On an average, we obtain \( \sim 2.4 \) – 3.1x savings in total energy expenditure per convolutional layer for MIME with respect to the baseline Case-1 and \( \sim 1.3 \) – 2.4x savings with respect to the baseline Case-2. Further in Fig. 7, we also present a similar comparison for the improvement in throughput achieved via MIME. Here, the layerwise throughput is normalized with respect to the baseline Case-1. We find \( \sim 2.8 \) – 3.0x improvement in throughput, that is primarily due to the reduced MAC computations in the PE arrays owing to the dynamic neuronal sparsity in MIME.

Comparison with highly compressed/pruned models for multi-task inference: To further evaluate the benefits of MIME in Pipelined task mode, we compare the layerwise energy against the conventional multi-task inference using highly compressed/pruned
We propose MIME, a memory and energy-efficient technique to conduct multi-task DNN inference on a systolic-array hardware. MIME uses the same weight parameters of a parent task to conduct inference for multiple child tasks. Each child task is associated with its own set of learnt threshold parameters used with the frozen parent weights for inference in a multi-task scenario. MIME leads to significant savings in off-chip DRAM storage compared to conventional approaches to multi-task inference. An important consequence of MIME is input and task-dependent dynamic neuronal pruning that unleashes several hardware benefits. We explore a more realistic and diversified mode of inference called Pipelined task mode and show that MIME leads to significant energy-savings and higher throughput on hardware when operated in this mode.

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