A new quasi-Z-source switched-boost four-switch three-phase inverter with independent shoot-through and non-shoot-through modulation indexes

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Abstract
Four-switch three-phase inverters (FSTPI) are the cost-optimised version of two-level voltage source inverters (TL-VSI), promoted for low-power/low-voltage machine drive systems. Adding impedance-based networks to the input of conventional VSIs provides both step-up and step-down features; however, the shoot-through (ST) modulation index limits the maximum attainable modulation index. Furthermore, in FSTPI, one switching leg has two series capacitors instead of power switches. Therefore, they are exposed to the voltage imbalance problem. This paper proposes a novel step-up FSTPI with independent shoot-through and non-shoot-through (NST) modulation indexes, improved boost factor, continuous input current, and high efficiency. This topology incorporates a quasi-z-source switched-boost network with independent power switches and three duty ratios that affords two active states and one shoot-through event. These features enhance the performance of this topology if compared with former FSTPI and quasi-z-source FSTPI. For evaluating the performance of this topology, simulation in MATLAB software and experiment on a prototype have been done. Simulation and experimentation results confirm the proposed topology.

1 | INTRODUCTION

Four-switch three-phase inverters (FSTPI) is the cost-optimised form of the conventional six-switch three-phase inverters, which are widely addressed by researchers for low-power cost-effective three-phase drive systems. Because of its conventional structure, most kinds of research concentrate on its control and modulation strategies [1, 2]. For example, the general PWM [3], scalar PWM method [4], general space vector modulation (SVM) [5], adaptive PWM method [6], unified PWM algorithm [7], and hybrid SVM [8] have been developed for FSTPI.

FSTPI is composed of four switches and two series capacitors. These two series capacitors form a separate leg, in which one phase of the load is connected to the capacitors’ midpoint. Reducing two power switches, in comparison with TL-VSI, yields improving efficiency. However, when using a capacitive leg, the inverter might be exposed to the voltage imbalance problem. Because the current of one phase comes in/out from the midpoint of this leg, the voltage of these capacitors may have different values. The voltage imbalance problem deteriorates the performance of FSTPI. Zhu, et al. [9] has introduced an adaptive method for the conventional PWM strategy in order to suppress the capacitors’ voltage difference in FSTPI. A bang-bang controller was introduced by [10] selects an appropriate inverter switching state in each sampling interval according to the difference between the voltages of capacitors. Although this method is valid, the steady-state error already does not eliminate. Kazemlou and Zolghadri [11] have proposed a novel SVM. The switching times and the sectors have been obtained according to the voltage difference between the capacitors. This strategy is implemented easily by digital signal processors.

The application of FSTPI in electrical machine drive systems is also broadly cited [2, 12–20], especially for permanent
magnet synchronous machines (PMSM) and brushless DC motors (BLDC). The direct torque control scheme of induction motors [11, 20], two-vector based predictive current control of synchronous reluctance motors [19], model predictive flux control (MPFC) [18], simplified model predictive current control of PMSM [17], current control of BLDC motor [16], sensorless control of interior PMSM [13], fuzzy logic control of induction motor [15], and simplified MPFC [12] have been presented and evaluated by researchers for FSTPI. Additionally, the application of FSTPI in flexible AC transmission systems (FACTS), as static compensators (STATCOM) and distribution STATCOMs (DSTATCOM), has been presented by [21, 22].

In recent years, the design of step-up inverters has received widespread attention in journals and conferences [23, 24]. Amongst several presented topologies, impedance-based step-up inverters are mostly cited due to single-stage conversion, high voltage gain, lower voltage stresses on power switches, acceptable efficiency, and some intrinsic protections. In these structures, one ST event is added to the switching algorithm. The ST period limits the inverter modulation index, and this case is a constraint. Impedance-based networks have also been adapted to FSTPIs. The main challenge is to find two split series capacitors branch in the impedance network. Antal, et al. [25] have combined a z-source network with an FSTPI. This article employed the traditional z-source network. High output current THD and discontinuous input current are the main disadvantages of the proposed topology. Different z-source FSTPI based on the conventional z-source network has been presented by [26]. This article has provided a capacitor leg for FSTPI from the input source so that it divides the voltage by using two series capacitors at the input section, and consequently, one phase of the load is linked to the neutral point of these capacitors. Nevertheless, still, the modulation index is limited by the ST time. A novel quasi-z-source FSTPI topology has been presented by [27]. This circuit incorporates a traditional quasi-z-source network. The internal capacitor of the conventional quasi-z-source network has been replaced with two series capacitors, and one phase of the load has been linked to the midpoint of them. This concept has two disadvantages: the voltage difference between the output terminals and dependent modulation and ST indexes.

This paper proposed a novel step-up FSTPI with independent ST and NST modulation indexes, improved boost factor, continuous input current, and high efficiency. This topology includes a quasi-z-source switched-boost network with independent power switches and three duty ratios that provides two active states and one shoot-through event. These features improve the performance of this topology in comparison with previous z-source and quasi-z-source FSTPIs. Simulations and experiments evaluate the performance of this structure. Results confirm the proposed topology. In the following, first, the principle of the proposed inverter is investigated. Then, in Section 3, simulation and experimental results are presented and evaluated, and results are compared with other similar works. Finally, all achievements are summarised in conclusion.

**FIGURE 1** Three conventional step-up FSTPI. (a) The converter of [25]. (b) The converter of [26]. (c) The converter of [27]

**FIGURE 2** The proposed quasi-z-source switched-boost FSTPI

## 2 THE PROPOSED TOPOLOGY

Figure 1 shows three conventional step-up FSTPI, presented by [25–27]. In those configurations, z-source and quasi-z-source networks added to the conventional FSTPI. Each topology has some drawbacks. In Figure 1a, the converter has discontinuous input current, and the modulation and ST indexes are dependent. In Figure 1b, the modulation and ST indexes are dependent. In Figure 1c, also, the modulation and ST indexes are dependent. Figure 2 represents the proposed step-up FSTPI. Due to combining the operation of a quasi-z-source network with a switched-boost cell, the resulted configuration is called quasi-z-source switched-boost network. The overall converter is named quasi-z-source switched-boost four-switch three-phase inverter (qZSSB-FSTPI). This step-up FSTPI contains six power switches (either IGBT or MOSFET), five capacitors, three inductors, and two fast diodes. The switches \( Q_1 \) and \( Q_2 \) are complementarily turned on/off; however, they have a specific overlap time for providing ST condition. Unlike other circuits, the capacitive leg of FSTPI, the ST and NST states of
the inverter are independent. In the following, the operating principle of the proposed qZSSB-FSTPI is described.

### 2.1 Operating principle of qZSSB-FSTPI

All components are assumed to be ideal. This converter operates in continuous current mode (CCM). Based on the switching states of $Q_1$ and $Q_2$, three equivalent circuits can be determined. Two of them relate to the NST state, and one of them corresponds to the ST state. Figure 3 depicts the equivalent circuits of these events.

#### 2.1.1 Mode 1-NST state 1 ($0 \leq t < d_1 T_3$)

In this switching mode, the switch $Q_1$ turns on, diode $D_2$ turns off, and diode $D_1$ is on. According to the equivalent circuit of Figure 3a, the following expressions are obtained.

\[ v_{L,1} = V_i - v_{C,1} \]  
\[ v_{L,2} = -v_{C,2} = v_{C,1} - V_x \]  
\[ v_{L,3} = V_x + v_{C,3} - V_{pos} \]  
\[ i_{C,1} = i_{C,2} + i_{L,1} - i_{L,2} = i_{L,1} - i_{L,3} \]  
\[ i_{C,2} = i_{L,2} + i_{C,3} = i_{L,2} - i_{L,3} \]  
\[ i_{C,3} = -i_{L,3} \]

#### 2.1.2 Mode 2-ST state ($d_1 T_3 \leq t < d_2 T_3$)

The next state correlates to the shoot-through state, in which the switches $Q_1$ and $Q_2$ are turned on simultaneously. Diodes $D_1$ and $D_2$ are off. Based on Figure 3b, the expressions (7)-(12) are determined. In this mode, the voltage $V_x$ is zero.

\[ v_{L,1} = V_i + v_{C,2} \]  
\[ v_{L,2} = v_{C,1} \]  
\[ v_{L,3} = v_{C,3} - V_{pos} \]  
\[ i_{C,1} = -i_{L,2} \]  
\[ i_{C,2} = -i_{L,1} \]  
\[ i_{C,3} = -i_{L,3} \]

#### 2.1.3 Mode 3-NST state 2 ($d_2 T_3 \leq t < T_3$)

At the beginning of this state, the $Q_1$ is off while $Q_2$ is on. As illustrated in Figure 3c, $D_1$ and $D_2$ are in forward-bias condition. Equations (7–9) is derived from the equivalent circuit of Figure 3c. In this mode, the voltage $V_x$ is equal to $v_{C,3}$. Therefore, since the NST state 1 is applied to the converter after the NST state 2, in NST state 1, the voltage of $V_x$ is also equal to $v_{C,3}$, and it is possible to replace $V_x$ by $v_{C,3}$.

\[ v_{L,1} = V_i - v_{C,1} \]  
\[ v_{L,2} = -v_{C,2} = v_{C,1} - V_x \]  
\[ v_{L,3} = v_{C,3} - V_{pos} \]  
\[ i_{C,1} = i_{C,2} + i_{L,1} - i_{L,2} = i_{L,1} - i_{L,3} \]  
\[ i_{C,2} = i_{L,2} - i_{x} \]  
\[ i_{C,3} = i_{x} - i_{L,3} \]

Voltage and current waveforms of components in the above three modes have been displayed by Figure 3d for the CCM condition.

### 2.2 Calculating the boost-factor and essential parameters

By applying the voltage-second balance theory of (19) and the Coulomb-second principle of (21) to (1–18), some essential identities are determined, which are shown by (21–28).
The boost-factor characteristics. (a) Variations of the boost-factor subject to $d_1$ and $d_{ST}$. (b) Comparison between boost-factors of different topologies.

For Figure 4, the boost-factor function has been illustrated for different $d_{ST}$ and $d_1$. The proposed topology has a higher voltage gain than topologies like introduced by [25–27], as shown in Figure 4b.

\[
BF = \frac{V_{pn}}{V_i} = \frac{1 + d_1}{2d_1 - 2d_2 + 1}.
\]

If $(d_2 - d_1)$ is assumed to be $d_{ST}$, Equation (30) simplifies to (31). The $d_{ST}$ denotes the shoot-through modulation index. Also, $d_1$ can be written in terms of $d_2$ and $d_{ST}$, according to Figure 3d.

\[
BF = \frac{1 + d_{ST}}{1 - 2d_{ST}},
\]

\[
d_1 = d_2 - d_{ST}.
\]

From Figure 2, $V_{pn}$ appears across the FSTPI section, and the voltages of capacitors $C_4$ and $C_5$ are equal to the half of $V_{pn}$. In Figure 4, the boost-factor function has been illustrated for different $d_{ST}$ and $d_1$. The proposed topology has a higher voltage gain than topologies like introduced by [25–27], as shown in Figure 4b. If it is assumed the input power and the output power (the input of the FSTPI stage) to be identical, as expressed in (33), the relevance between the input current value and the DC-bus current value is determined from (34).

\[
I_i = \frac{1 + d_1}{2d_1 - 2d_2 + 1} I_{par}.
\]

The average value of the input inductor current ($I_{L1}$) is equal to the input current. The average value of the output inductor current ($I_{L3}$) is equal to the output current. Moreover, the average current of $L_1$ and $L_2$ are identical. The following identities can be derived using $V_L = L \Delta I_L / \Delta t$.

\[
V_{pn} = \frac{(1 + d_{ST}) V_i}{2d_1 - 2d_2 + 1},
\]

\[
BF = \frac{V_{pn}}{V_i} = \frac{1 + d_1}{2d_1 - 2d_2 + 1}.
\]

\[
< i_L > = \int_{0}^{T_F} i_L(t) dt + \int_{D_T}^{T_F} i_L(t) dt = 0, \quad (19)
\]

\[
< i_C > = \int_{0}^{D_T} i_C(t) dt + \int_{D_T}^{T_F} i_C(t) dt = 0, \quad (20)
\]

\[
V_f = (1 + d_1 - d_2)V_{C1} - (d_2 - d_1)V_{C2}, \quad (21)
\]

\[
V_{C1} = \frac{1 + d_1 - d_2}{2d_1 - 2d_2 + 1} V_i, \quad (22)
\]

\[
V_{C2} = \frac{d_2 - d_1}{1 + d_1 - d_2} V_{C1} = \frac{d_2 - d_1}{2d_1 - 2d_2 + 1} V_i, \quad (23)
\]

\[
V_{pn} = (1 + d_1)V_{C3}, \quad (24)
\]

\[
V_{C3} = \frac{V_{C1}}{1 + d_1 - d_2}, \quad (25)
\]

\[
I_{L1} = \frac{1 + d_1}{2d_1 - 2d_2 + 1} I_{par} \quad (26)
\]

\[
I_{L2} = \frac{1 + d_1}{2d_1 - 2d_2 + 1} I_{par} \quad (27)
\]

\[
I_c = \frac{I_{L3}}{1 - d_2} = \frac{I_{par}}{1 - d_2} \quad (28)
\]

Consequently, from (22–25), the relation between the input voltage and $V_{pn}$ can be defined by (29). So, the boost-factor can be expressed by (30).
FIGURE 5  Results of sensitivity analysis. (a) The sensitivity of the boost-factor subject to $d_1$. (b) The sensitivity of the boost-factor respect to $d_2$

$$L_2 = \frac{d_1(d_1 - d_2)}{(2d_1 - 2d_2 + 1) \Delta l_{2} f_s} V_p, \quad (36)$$

$$L_3 = \frac{d_1(1 - d_1)}{(2d_1 - 2d_2 + 1) \Delta l_{3} f_s} V_p. \quad (37)$$

Furthermore, by using $I_C = C \Delta V_C / \Delta t$, the following results are achieved.

$$C_1 = \frac{d_1(2d_2 - d_1)}{(2d_1 - 2d_2 + 1) \Delta V_{C1} f_s} I_{ps}, \quad (38)$$

$$C_2 = \frac{d_1(2d_2 - d_1)}{(2d_1 - 2d_2 + 1) \Delta V_{C2} f_s} I_{ps}, \quad (39)$$

$$C_3 = \frac{d_1}{\Delta V_{C3} f_s} I_{ps}. \quad (40)$$

Equations (35–40) are used to determine appropriate values for inductors and capacitors of the proposed converter. Usually, the inductor current ripple value is chosen between 20% and 40% of the average inductor current value. Also, the capacitor voltage ripple is selected between 5% and 15% of the capacitor voltage value.

2.3  Sensitivity analysis

Figure 4a represents the effect of $d_1$ and $d_{ST}$ on the output voltage gain of the qZSSB-FSTPI. Based on Figure 4a, the maximum achievable ST duty cycle is 0.5. In Figure 5a and Figure 5b, the sensitivity analysis of the boost-factor subject to $d_1$ and $d_2$ has been presented. For this purpose, the differential sensitivity analysis theory is applied to (30). This analysis has been executed based on (41). The derivative of the boost-factor subject to $d_1$ and $d_2$ have been calculated. Equations (42) and (43) show these derivatives. The value of $d_1$ specifies the amount of additional gain in boost-factor function, and the amount of overlap between $d_1$ and $d_2$ defines the shoot-through duty cycle. According to the boost-factor function, if $d_1 = 1$ and $d_2 = 0$, then the overall gain is multiplied by 2. Consequently, the variation of $d_1$ has a limited impact. However, the variation of $d_2$ can change the amount of overlap between them, which directly affects the gain because the shoot-through event generates the main amount of gain.

$$\Delta (BF) = \frac{\partial BF}{\partial d_1} \Delta (d_1) + \frac{\partial BF}{\partial d_2} \Delta (d_2), \quad (41)$$

$$\frac{\partial BF}{\partial d_1} = \frac{1}{2d_1 - 2d_2 + 1} \frac{2(1 + d_1)}{(2d_1 - 2d_2 + 1)^2}, \quad (42)$$

$$\frac{\partial BF}{\partial d_2} = \frac{2(1 + d_1)}{(2d_1 - 2d_2 + 1)^2}. \quad (43)$$

2.4  Voltage and current of power semiconductors

Table 1 lists the voltage stress value of each semiconductor based on the converter operation shown in Figure 3. Values of $V_{C1}$, $V_{C2}$, $V_{C3}$, and $V_{ps}$ are determined from (22) and (23). The maximum current, which is passed through power

| Components | Voltage Stress |
|------------|----------------|
| $D_1$      | $V_C + V_p$    |
| $D_2$      | $V_C$          |
| $Q_1$      | $V_C$          |
| $Q_2$      | $V_C + V_p$    |

$$s_1 - s_4 = V_{ps}$$

Table 1  Voltage stress on power semiconductors
switches $Q_1$ and $Q_2$, are occurred during the ST condition ($d_2-d_1$) $T_0$. Therefore, $Q_1$ and $Q_2$ must tolerate the current value of $(I_{L1}+I_{L2})$. The maximum current that is passed through $D_2$ is obtained from $(I_{L1}+I_{L2})$ and $I_{L3}$. Furthermore, diode $D_2$ must withstand $(I_{L3})$ in its active state.

### 2.5 Operating principle of the FSTPI stage

FSTPI generates a switching voltage with 50 Hz frequency. The space vector modulation algorithm is applied to this stage. There are four possible switching states for the FSTPI. Capacitors’ voltage imbalance problem must be considered in selecting voltage vectors. Figure 6 compares the values of switching vectors with/without voltage imbalance in DC capacitors. It should be noted that phase B is connected to the midpoint of DC-link capacitors, as shown in Figure 2. Capacitors’ voltage imbalance changes the magnitude and angle of $V_2(1,0)$ and $V_3(0,1)$. Also, this problem only changes the magnitude of $V_1(0,0)$ and $V_3(1,1)$. This problem causes an unbalanced condition of the line-line output voltage. Table 2 organises the specifications of switching vectors, according to the voltage of capacitors $C_4$ and $C_5$. All voltage vectors divide the $\alpha\beta$-plane into four sectors. Based on the principle of the conventional SVM, each reference vector can be reproduced by using two adjacent vectors and one zero vector. However, the FSTPI does not possess any zero vector. Hence, one vector is picked as a semi-zero vector. Table 3 is used to distinguish the sector, too. Based on the voltage-second balance theory of (33), the reference vector can be rebuilt by two adjacent vectors.

$$ U_{r/f} T_0 = U_1 T_1 + U_2 T_2 $$

$$ T_0 = T_1 + T_2 + T_0 $$

In Equation (44), $U_1$ and $U_2$ are two switching vectors that are selected by considering the location of the reference vector. $T_1$ and $T_2$ define as switching times of $U_1$ and $U_2$, respectively. Also, $T_0$ denotes zero switching time. Equation (44) can be solved by considering Table 2 for each sector. Results are switching times in each sector based on the voltage of capacitors $C_4$ and $C_5$. It is assumed that $(V_{C4}=mV_{C3})$ and $(0<m<1)$. Hence, the switching times can be deduced from Equation (44), as listed in Table 3. Resulted times are applied to the FSTPI with a particular switching algorithm, as represented in Figure 7.

### TABLE 2 The specifications of each switching vector

| Vector | $|V|$ | $\Delta V$ |
|--------|------|------------|
| $V_1$  | $\frac{2\sqrt{3}}{3}$ | 0 |
| $V_2$  | $\sqrt{\frac{(\sqrt{3}+1)\sqrt{3}}{9}} + \frac{(\sqrt{3}+1)\sqrt{3}}{3}$ | $\tan^{-1}\left(\frac{3(\sqrt{3}+1)\sqrt{3}}{\sqrt{(\sqrt{3}+1)\sqrt{3}}}ight)$ |
| $V_3$  | $\frac{2\sqrt{3}}{3}$ | 180 |
| $V_4$  | $\sqrt{\frac{(\sqrt{3}+1)\sqrt{3}}{9}} + \frac{(\sqrt{3}+1)\sqrt{3}}{3}$ | $\tan^{-1}\left(\frac{3(\sqrt{3}+1)\sqrt{3}}{\sqrt{(\sqrt{3}+1)\sqrt{3}}}ight)$ |

### TABLE 3 The active switching times for sector 1 to 4

| Sector | Zone | $T_1/T_0$ | $T_2/T_0$ |
|--------|------|------------|------------|
| 1      | $\frac{11\pi}{6} \leq \phi_{r/f} < \frac{\pi}{6}$ | $0.5 \frac{|\phi_{r/f}|}{\sqrt{2}} \left(3\cos(\phi_{r/f}) - \sqrt{3} \left(\frac{1}{1+\delta} \sin(\phi_{r/f})\right)\right)$ | $\sqrt{3} \frac{|\phi_{r/f}|}{\sqrt{2}} \sin(\phi_{r/f})$ |
| 2      | $\frac{\pi}{6} \leq \phi_{r/f} < \frac{2\pi}{3}$ | $\sqrt{3} \frac{|\phi_{r/f}|}{\sqrt{2}} \sin(\phi_{r/f})$ | $0.5 \frac{|\phi_{r/f}|}{\sqrt{2}} \left(-3\cos(\phi_{r/f}) - \sqrt{3} \left(\frac{1}{1+\delta} \sin(\phi_{r/f})\right)\right)$ |
| 3      | $\frac{2\pi}{3} \leq \phi_{r/f} < \frac{7\pi}{6}$ | $-0.5 \frac{|\phi_{r/f}|}{\sqrt{2}} \left(3\cos(\phi_{r/f}) + \sqrt{3} \left(\frac{1}{1+\delta} \sin(\phi_{r/f})\right)\right)$ | $-\sqrt{3} \frac{|\phi_{r/f}|}{\sqrt{2}} \sin(\phi_{r/f})$ |
| 4      | $\frac{7\pi}{6} \leq \phi_{r/f} < \frac{11\pi}{6}$ | $-\sqrt{3} \frac{|\phi_{r/f}|}{\sqrt{2}} \sin(\phi_{r/f})$ | $0.5 \frac{|\phi_{r/f}|}{\sqrt{2}} \left(3\cos(\phi_{r/f}) + \sqrt{3} \left(\frac{1}{1+\delta} \sin(\phi_{r/f})\right)\right)$ |
Efficiency analysis

The qZSSB-FSTPI incorporates six power switches and one diode. The above modeling associates with an ideal topology. In an ideal condition, the series resistance of inductors, the voltage drop of the diode, the voltage drop of the power switch, and the on-resistance of the power switch \( r_{on} \) are neglected. Generally, these parameters affect the performance of topology, especially efficiency. The overall losses of the converter equalise to the summation of switching losses, conduction losses, and dead-time losses. The switching losses, including gate-charge loss and switching on/off loss, are determined by (45).

\[
P_{SW} = P_{\text{Switching}} + P_{\text{Gate}}, \\
P_{\text{Switching}} = 0.5V_{SW} f_{SW} (t_r + t_f) f_S, \\
P_{\text{Gate}} = Q_G V_{GS}^2 f_S. \tag{45}
\]

### Table 4  The converter specifications

| Parameters | Values |
|------------|--------|
| Input voltage [V] | 72 |
| Output voltage \( (V_{pm}) \) [V] | 500 |
| Output voltage \( (V_{\text{line-line}}) \) [V] | 250 |
| Output power [W] | 300 |
| Output frequency [Hz] | 50 |
| Switching frequency [Hz] | 6000 |
| \( L_1, L_2, L_3 \) [\( \mu \text{H} \)] | 1000, 1000, 10000 |
| \( C_1, C_2, C_3 \) [\( \mu \text{F} \)] | 2200, 2200, 1000 |
| \( C_4, C_5 \) [\( \mu \text{F} \)] | 1220 |
| Ferrite cores | Toroid R25 and EER2834 |
| Output resistance and inductance \( [\Omega, \text{mH}] \) | 10, 250 |
Switching losses depend on the voltage of power switch during off-state \( (V_{SW}) \) , the current of power switch during on-state \( (I_{SW}) \) , the rise-time and fall-time \( (t_r, t_f) \) , the switching frequency \( (f_s) \) , the gate charge \( (Q_G) \) , and the voltage of gate-source \( (V_{GS}) \) . Only four switches of the FSTPI stage have dead-time between their switching actions. A negligible amount of loss corresponds to dead-time loss, which is associated with dead-time in rising and falling edges \( (t_{dR}, t_{dF}) \) . In this condition, the output current may pass through the body-diode of power switches. The following expression describes the dead-time loss. \( V_{MBD} \) and \( I_{MBD} \) indicate the voltage drop and the current of body-diode, respectively.

\[
P_{D-T} = V_{MBD} I_{MBD} (t_{dR} + t_{dF}) f_s
\]

\[
P_{\text{on-off switch}} = r_{sw} I_{SW}^2 D.
\]

Conduction losses of the converter depend on the parasitic elements of components and power switches. The conduction loss, relevant to each switch of each switch, however, the conduction loss of the components and semiconductors of the quasi-z-source switched-boost stage should be determined from its loss modeling. For this purpose, Figure 8 has been taken into account. Based on Figures 8 and 3, and three switching modes of this converter, the following expressions can be established. By applying \( 19 \) and \( 20 \) to \( 48 \)–\( 54 \), the following results are achieved. Finally, the equation that has the loss parameters is expressed by \( 59 \). The conduction loss of the qZSSB circuit is expressed by \( 60 \). In order to bring a better analysis, a particular case is studied. It is assumed that \( d_1 = 0.4, d_2 = 0.4, V_p = 72V, V_{pe} = 500V \). A set of test cases have been designed to assess the effect of parasitic parameters on the efficiency and the conduction loss of the qZSSB circuit. The results of this analysis have been depicted in Figure 9. It is inferred from the results that in the design of this stage, choosing lower inductances and low loss power semiconductors are important.
\( V_i - 4d_s V_Q - V_f = \left[ \left( 1 + d_1 \right) \left( r_{L,1} + r_{L,2} + 8r_{on}d_s \right) R_L \right] \frac{1 + d_1}{1 - 2d_s} + \left( 1 - 2d_s \right) \frac{r_{L,3}}{1 + d_1} \right) V_{pot} \) \hspace{1cm} (59)

\[ P_{\text{cond,CSB}} = \frac{(r_{L,1} + r_{L,2} + 8r_{on}d_s)I_{pot}^2}{1 + d_1} + \frac{1 - 2d_s}{1 - d_1} r_{L,3} I_{pot}^2 + \frac{(4d_s V_Q + V_f)I_{pot}}{P_{\text{semi}}} \] \hspace{1cm} (60)
2.7 Design considerations

In order to design a qZSSB-FSTPI, the following procedure is required:

i. Choosing a suitable shoot-through duty-cycle by using (31).

ii. Calculating the average current of each inductor by using (26–28).

iii. Selecting proper values for $\Delta I_L$ and $\Delta V_C$.

iv. Identifying the inductances and capacitances, considering (35–40).

3 RESULTS AND ANALYSIS

This section presents and investigates simulation and experimental results. A low-voltage/low-power prototype has been designed in order to assess the proposed topology, its theory, and the working principle. Table 4 summarises the specifications of this prototype. In the simulation, MATLAB/Simulink software has been utilised. In this prototype, TMS320F28335PGFA digital signal processor (DSP) generates suitable PWM signals for the converter. The GW-INSTEK GDS-2074 oscilloscope has captured experimental results. Figure 10 shows the experimental setup and its components.

Figure 11a illustrates the PWM signals applied to the power switches in simulation and experiments, respectively. As can be seen, the shoot-through duty cycle is equal to 0.4 and $d_2=0.8$. So, based on (32), $d_1=0.4$. Figure 11b presents the output voltage in simulation and experiments. The maximum value of the line voltage is about 500V, which the RMS value is 350V. It follows the reference value. Thus, the boost factor is 7. If $d_1=0.4$ and $d_{ST}=0.4$, then, according to Figure 4a, the boost factor is 7. Hence, results confirm the theory. Figure 11c displays the output line current, in which both results are identical to 0.7 Apk. Figure 11d displays the voltage stress across the power switches $Q_1$ and $Q_2$, whenever they are off. The measured values are 352 V for both semiconductors, which are five times greater than the input voltage.

In order to compare the measured voltage stress with the theoretical values, Figure 12a and Figure 12b have been illustrated. For $d_1=0.4$ and $d_{ST}=0.4$, the voltage stress is five times further than the input voltage, as shown in Figure 12a and Figure 12b. Furthermore, other waveforms, such as the voltage of capacitors and inductors, and the voltage stresses on power diodes have been represented in Figure 13. The voltage of inductors do not lay on zero, in the whole wave; hence, their currents are changed continuously. This feature can be seen in both the laboratory results and the simulation results. Therefore, the converter operates in a CCM. Moreover, to compare the measured values for capacitors voltages with numerical values, Figure 12c has been drawn. It shows a graph, which describes how the voltage of capacitors changes with the shoot-through duty cycle. For $d_1=0.4$ and $d_{ST}=0.4$, results validate the derived values. There are some overshoots in capacitors voltage waveforms that indicate the charging events. As can be seen from Figure 13a, the voltage of $L_1$ is not reached to zero any time; so, the current $I_{L1}$ varies continuously. This current flows through the input source, and as a result, the input current is continuous. The voltage of capacitors $C_4$ and $C_5$ have been represented in Figure 14. These two capacitors form one leg of the FSTPI and can be exposed to the voltage imbalance problem.

The proposed converter cannot balance the voltage of them, and as same as other references, it must be done by the employed modulation technique. As mentioned before, SVM is implemented as a modulation strategy. Sectors are determined from Table 2, and the switching times are obtained from Table 3, which their values rely on the voltage of $C_4$ and $C_5$. The voltage of capacitors $C_4$ and $C_5$ is equal to half of $V_{ph}$ that is calculated by (24). According to (24), $V_{ph}=500$. Therefore, the voltage of $C_4$ and $C_5$ are 250 V, referred by theory.

The quality of the output current and the efficiency have also been investigated. Figure 15a shows the current THD. It
FIGURE 13  Other important waveforms in simulation and experiment. (a) $V_{L1}$, $V_{C2}$ and $V_{D1}$. (b) $V_{L2}$ and $V_{C1}$. (c) $V_{D2}$, $V_{C3}$ and $V_{L3}$. (d) $I_{L1}$, $I_{L2}$ and $I_{L3}$. 
FIGURE 14  Simulation and experimental results of the voltage of capacitors $C_4$ and $C_5$. (a) Simulation result. (b) Experimental result

FIGURE 15  Experimental current THD and efficiency analysis. (a) THD (b) Efficiency

is about 3.56%. Based on the harmonic analysis, carried out for the harmonic order of 200, all harmonics have been associated around the switching frequency. Thus, no filter is needed for inductive loads because THD has a standard value (<5%). Figure 15b depicts the efficiency under different output loads. This curve confirms the results of efficiency analysis in Figure 9. The losses of FSTPI section, which includes only four power switches are negligible [27]. The main contribution of four-switch three-phase inverters over the conventional six-switch three-phase inverters is the efficiency due to reducing two power switches from the inverter leg [27]. In this case, $r_{in} = 0.0015$, $r_{L1} = r_{L2} = 0.01$, $r_{L3} = 0.05$, $V_Q = 0.5$, and $V_F = 0.4$. Table 5 compares the specifications of some similar z-source FSTPI topology with the proposed quasi-z-source switched-boost FSTPI. The main advantages of the qZSSB-FSTPI in comparison with other similar converters are the continuous input current, higher boost factor with lower ST duty-ratios, semi-linear gain, independent ST and NST modulation indexes, high efficiency, and the ability to increase the number of inputs. The last feature is realised by adding another source, such as a battery, instead of capacitor $C_2$ [28]. Also, similar to other inverters, it is possible to implement modern control systems, such as the family of predictive controllers [29–31].

Table 6 compares the proposed topology with other similar topologies quantitatively. Due to the difference between the converter specifications of this paper and [25–27], the experimental efficiency of the proposed topology is compared with the simulated efficiency of [25–27]. Although the proposed
TABLE 5  Comparison between the proposed topology and other similar topologies

| Topology | Refs. | Pros. | Cons. |
|----------|-------|-------|-------|
|          | [25]  | √ The number of components | × Discontinuous input current |
|          |       | √ No need to input voltage divider | × Capacitors inrush current |
|          |       |                               | × Dependent modulation and ST indexes |
|          |       |                               | × Lower boost factor |
|          |       |                               | × Non-linear gain curve |
|          | [26]  | √ The number of components | × Discontinuous input current |
|          |       |                               | × Capacitors inrush current |
|          |       |                               | × Dependent modulation and ST indexes |
|          |       |                               | × Need to the input voltage divider |
|          |       |                               | × Lower boost factor |
|          |       |                               | × Non-linear gain curve |
|          | [27]  | √ The number of components | × Output voltage imbalance |
|          |       | √ No capacitors inrush current | × Dependent modulation and ST indexes |
|          |       | √ Continuous input current | × Lower boost factor |
|          |       | √ No need to input voltage divider | × Non-linear gain curve |
|          | The Proposed | √ No capacitors inrush current | × The number of components |
|          |       | √ Continuous input current | |
|          |       | √ Semi-linear gain curve | |
|          |       | √ Higher boost factor | |
|          |       | √ Independent NST and ST indexes | |
|          |       | √ No need to input voltage divider | |

TABLE 6  Quantitative comparison between the proposed topology and other similar topologies

| Refs. | Switch | Diode | Inductor | Capacitor | Boost Factor (BF) | \(D_{\text{shmax}}\) | \(D_{\text{shmin}}\) | BF @ \(D_{\text{shmin}}\) | eff@300W/BF @ 6 |
|-------|--------|-------|---------|-----------|------------------|----------------|----------------|----------------------|-----------------|
| [25]  | 4      | 1     | 2       | 3         | \(\frac{1}{1-2d_{\text{sh}}}\) | 0.5            | 0              | 1                    | 92%             |
| [26]  | 4      | 1     | 2       | 3         | \(\frac{1}{1-2d_{\text{sh}}}\) | 0.5            | 0              | 1                    | 93%             |
| [27]  | 4      | 1     | 2       | 3         | \(\frac{1}{1-2d_{\text{sh}}}\) | 0.5            | 0              | 1                    | 94.9%           |
| The proposed | 6     | 2     | 5       | 3         | \(\frac{1}{1-2d_{\text{sh}}}\) | 0.5            | 0              | 1 + \(d_{\text{l}}\)   | 95.5%           |

topology includes two power switches more than [25–27], this converter works with lower shoot-through duty cycles than [25–27]. Thus, it is more efficient than them. Furthermore, this converter operates with independent shoot-through and non-shoot-through modulation indexes, which this feature is not available for others. Topologies in [25, 26] operate in DCM, which is not suitable for connecting to batteries, fuel cells etc.

4  CONCLUSION

This paper presents a quasi-z-source switched-boost four-switch three-phase inverter. It provides continuous input current, higher boost factor with lower ST duty-ratios, semi-linear gain, independent ST and NST modulation indexes, and high-efficiency compared with previous efforts. A detailed analysis has been presented and evaluated by this paper, and simulation and experimental results confirm that this structure operates carefully with maximum efficiency of 96%. Also, the output current THD in the proposed step-up topology is 3.56%. This converter has semi-linear gain characteristics, which yields the comfortable design of control loops.

REFERENCES
1. Monfared, M., et al.: Overview of modulation techniques for the four-switch converter topology. In: 2008 IEEE 2nd International Power and Energy Conference, pp. 803–807. IEEE, Piscataway
2. Li, W., et al.: Investigation of a four-switch four-leg inverter: Modulation, control, and application to an ipmsm drive. IEEE Trans. Power Electron. 34(6), 5655–5666 (2019)
3. Correa, M.B.d.R., et al.: A general PWM strategy for four-switch three-phase inverters. IEEE Trans. Power Electron. 21(6), 1618–1627 (2006)
4. An, Q.T., et al.: Scalar PWM algorithms for four-switch three-phase inverters. Electron. Lett. 46(13), 900–902 (2010)
5. Liu, Y., et al.: General SVPWM strategy for three different four-switch three-phase inverters. Electron. Lett. 51(4), 357–359 (2015)
6. Zhou, W., Sun, D.: Adaptive PWM for four-switch three-phase inverter. Electron. Lett. 51(21), 1690–1692 (2015)
7. Sun, D., et al.: Unified PWM algorithm based on effective time for four-switch three-phase inverter. Electron. Lett. 52(24), 2009–2011 (2016)
8. Zeng, Z., et al.: Hybrid space vector modulation strategy for torque ripple minimization in three-phase four-switch inverter-fed PMSM drives. IEEE Trans. Ind. Electron. 64(3), 2122–2134 (2017)
9. Zhu, C., et al.: Adaptive suppression method for dc-link voltage offset in three-phase four-switch inverter-fed PMSM drives. Electron. Lett. 52(17), 1442–1444 (2016)
10. Zhou, D., et al.: Predictive torque control scheme for three-phase four-switch inverter-fed induction motor drives with dc-link voltages offset suppression. IEEE Trans. Power Electron. 30(6), 3309–3318 (2015)
11. Kazemlou, S., Zolghadri, M.R.: Direct torque control of four-switch three phase inverter fed induction motor using a modified SVM to compensate dc-link voltage imbalance. In: 2009 International Conference on Electric Power and Energy Conversion Systems (EPECS), pp. 1–6. IEEE, Piscataway (2009)
12. Sun, D., et al.: A simplified MPFC with capacitor voltage offset suppression for the four-switch three-phase inverter-fed PMSM drive. IEEE Trans. Ind. Electron. 66(10), 7633–7642 (2019)
13. Lu, J., et al.: High-frequency voltage injection sensorless control technique for IPM/SMS fed by a three-phase four-switch inverter with a single current sensor. IEEE/ASME Trans. Mechatron. 23(2), 758–768 (2018)
14. Zhu, C., et al.: Comprehensive analysis and reduction of torque ripples in three-phase four-switch inverter-fed PMSM drives using space vector pulse-width modulation. IEEE Trans. Power Electron. 32(7), 5411–5424 (2017)
15. Zaky, M.S., Metwal, M.K.: A performance investigation of a four-switch three-phase inverter-fed IM drives at low speeds using fuzzy logic and PI controllers. IEEE Trans. Power Electron. 32(5), 3741–3753 (2017)
16. Xia, C., et al.: A current control scheme of brushless dc motors driven by four-switch three-phase inverters. IEEE J. Emerg. Sel. Topics in Power Electron. 5(1), 547–558 (2017)
17. Su, J., Sun, D.: Simplified MPCC for four-switch three-phase inverter-fed PMSM. Electron. Lett. 53(16), 1108–1109 (2017)
18. Hua, W., et al.: Improved model-predictive-flux-control strategy for three-phase four-switch inverter-fed flux-reversal permanent magnet machine drives. IET Electr. Power Appl. 11(5), 717–728 (2017)
19. Lin, C., et al.: Two-vector-based modelless predictive current control for four-switch inverter-fed synchronous reluctance motors emulating the six-switch inverter operation. Electron. Lett. 52(14), 1244–1246 (2016)
20. Badsi, B.E., et al.: DTC scheme for a four-switch inverter-fed induction motor emulating the six-switch inverter operation. IEEE Trans. Power Electron. 28(7), 3528–3538 (2013)
21. Kumar, A.P., et al.: Three-phase four-switch DSTATCOM topologies with special transformers for neutral current compensation and power quality improvement. IET Gener. Transm. Distrib. 13(3), 368–379 (2019)
22. Jafari, E., Marjanian, A.: Theoretical implementation of a novel isolated three-phase induction generator with controllable output voltage using a three-phase four-switch STATCOM. In: 2011 2nd International Conference on Electric Power and Energy Conversion Systems (EPECS), pp. 1–6. IEEE, Piscataway (2011)
23. Forouzesh, M., et al.: Step-up dc–dc converters: A comprehensive review of voltage-boosting techniques, topologies, and applications. IEEE Trans. Power Electron. 32(12), 9143–9178 (2017)
24. Ellabban, O., Abu-Rub, H.: Z-source inverter: Topology improvements review. IEEE Ind. Electron. Mag. 10(1), 6–24 (2016)
25. Antal, R., et al.: Novel, four-switch, z-source three-phase inverter. In: IECON 2010—36th Annual Conference on IEEE Industrial Electronics Society, pp. 619–624. IEEE, Piscataway (2010)
26. Najmi, E.S., et al.: Z-source three-phase four-switch inverter with dc link split capacitor and comprehensive investigation of z-source three-phase four-switch inverters. In: 2012 3rd Power Electronics and Drive Systems Technology (PEDSTC), pp. 25–31. IEEE, Piscataway (2012)
27. Khorzavi, F., et al.: Design and implementation of a new four-switch modified quasi z-source inverter with improved space vector control method. Int. J. Circuit Theory Appl. 47(11), 1837–1855 (2019)
28. Omran, K.C., Mosallanejad, A.: SMES/battery hybrid energy storage system based on bidirectional z-source inverter for electric vehicles. IET Electr. Syst. Transp. 8(4), 215–220 (2018)
29. Eshekevari, A.L., et al.: Design and analysis of a simple predictive power controller for a 1.0-kV single-phase NPC PWM rectifier. Int. J. Circuit Theory Appl. 46(12), 2495–2511 (2018)
30. Eshekevari, A.L., Arasteh, M.: Virtual flux based model-predictive direct power control of three-phase three-level NPC PWM rectifier. In: 2017 8th Power Electronics, Drive Systems & Technologies Conference (PEDSTC), pp. 172–177. IEEE, Piscataway (2017)
31. Eshekevari, A.L., Arasteh, M.: Model-predictive direct power control of three-phase three-level NPC PWM rectifier. In: 2017 8th Power Electronics, Drive Systems & Technologies Conference (PEDSTC), pp. 78–83. IEEE, Piscataway (2017)

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