Integrating Owicki-Gries for C11-Style Memory Models into Isabelle/HOL *

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Abstract. Weak memory presents a new challenge for program verification and has resulted in the development of a variety of specialised logics. For C11-style memory models, our previous work has shown that it is possible to extend Hoare logic and Owicki-Gries reasoning to verify correctness of weak memory programs. The technique introduces a set of high-level assertions over C11 states together with a set of basic Hoare-style axioms over atomic weak memory statements (e.g., reads/writes), but retains all other standard proof obligations for compound statements. This paper takes this line of work further by showing Nipkow and Nieto’s encoding of Owicki-Gries in the Isabelle theorem prover can be extended to handle C11-style weak memory models in a straightforward manner. We exemplify our techniques over several litmus tests from the literature and a non-trivial example: Peterson’s algorithm adapted for C11. For the examples we consider, the proof outlines can be automatically discharged using the existing Isabelle tactics developed by Nipkow and Nieto. The benefit here is that programs can be written using a familiar pseudocode syntax with assertions embedded directly into the program.

1 Introduction

Hoare logic [17] is fundamental to understanding the intended design and semantics of sequential programs. Owicki and Gries’ [29] framework extends Hoare logic to a concurrent setting by adding an interference-free check that guarantees stability of assertions in one thread against the execution of another. Although several other techniques for reasoning about concurrent programs have since been developed [33], Owicki-Gries reasoning remains fundamental to understanding concurrent systems and one of the main methods for performing deductive verification. Mechanised support for Owicki-Gries’ framework has been developed for the Isabelle theorem prover [30] by Nipkow and Nieto [28] and is currently included in the standard distribution.

Our work is in the context of C11 (the 2011 C standard), which has a weak memory model that is designed to enable programmers to take advantage of weak memory hardware [6,20,23,24]. Unlike in sequentially consistent memory [20], states are graphs with several relations that are used to track dependencies between memory events (e.g., reads, writes, updates) [2,6,11,20,23,24]. This means that it is not possible to use the traditional Owicki-Gries framework to reason about concurrent programs under C11. Researchers have instead developed a set of specialised logics, e.g., [2], including those that extend Owicki-Gries framework [25] and separation logic [12,13,35,35,37] designed to cope with specific fragments of C11.

Our point of departure is the operational semantics of Doherty et al. [11] for the RC11-RAR fragment of C11 [23]. As indicated by the RAR, the memory model allows both relaxed and

* This work is supported by EPSRC grants EP/R032351/1, EP/R032556/1 and EP/R019045/2.
release-acquire accesses. Moreover, the model restricts the C11 memory model to disallow the “load-buffering” litmus test \cite{23,24}. A key advancement in the semantics developed by Doherty et al. is a transition relation over states modelled as C11 graphs, allowing program execution to be viewed as an interleaving of program statements as in classical approaches to concurrency. They provide a primitive assertion language for expressing properties of such states, which is manually applied to the message passing litmus test and Peterson’s algorithm adapted to C11. However, the assertion language itself expresses state properties at a low level of abstraction (high level of detail), and hence is difficult to mechanise. We\cite{19,20} have recently recast Doherty et al.’s semantics in an equivalent timestamp-based semantics \cite{19,20}. More importantly, we have developed a high-level set of assertions for stating properties of the C11 state \cite{9}. These assertions have been shown to integrate well with a Hoare-style proof calculus, and, by extension, the Owicki-Gries proof method. Interestingly, the technique enables reuse of all standard Owicki-Gries proof rules for compound statements. In this paper, we push this technique further by showing how this framework can be integrated into Isabelle via a straightforward extension of the Owicki-Gries encoding by Nipkow and Nieto \cite{28}. Unlike \cite{9}, where program counters are used to model control flow and relations over C11 states are used to model program transitions, the approach in this paper is more direct. We show that once a correct proof outline has been encoded, the proof outlines can be validated with minimal user interaction. Our extension is parametric in the memory model, and can be adapted to reason about other C11-style operational models \cite{24}.

**Contributions.** Our main contributions are thus:

1. A simple and generic extension to the standard Isabelle encoding of Owicki-Gries to cope with C11-style weak memory,
2. An instantiation of the RC11-RAR operational semantics within Isabelle as an example memory model,
3. An integration with a high-level assertion language for reasoning about weak memory states, and
4. Verification of several examples in the extended theory, including Peterson’s algorithm for C11.

**Overview.** In Section 2 we briefly present the Owicki-Gries encoding by Nipkow and Nieto \cite{28}, as well as the message passing litmus test which serves as a running example. We describe how this encoding can be generically extended to cope with weak memory in Section 3 then in Section 4 we present RC11-RAR as an example instantiation. In Section 5 we present a technique for reasoning about C11-style programs as encoded in Isabelle\cite{9}, which we apply to a number of examples. We present related work in Section 6.

## 2 Owicki-Gries in Isabelle/HOL

Nipkow and Nieto \cite{28} present a formalisation of Owicki-Gries method in Isabelle/HOL. Their formalisation defines syntax, its semantics and Owicki-Gries proof rules in higher-order logic. Correctness of the proof rules with respect to the semantics is proved and their formalisation is part of the standard Isabelle/HOL libraries. To provide some context for our extensions, we provide an

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\footnote{For the CAV reviewers: This work is under review. An anonymised copy of the paper has been uploaded \cite{9}.}

\footnote{Our entire Isabelle formalisation can be found as ancillary files here \url{https://arxiv.org/abs/2004.02983}.}
The defined programming language is a C-like \texttt{WHILE} language augmented with shared-variable parallelism (\texttt{||}) and synchronisation (\texttt{AWAIT}). Parallelism must not be nested, i.e. within \(c_1 || c_2 || ... || c_n\), each \(c_i\) must be a sequential program. The programming language allows program constructs to be annotated with assertions in order to record proof outlines that can later be checked. The language also allows unannotated commands that may be placed within the body of \texttt{AWAIT} statements. As in the original treatment [29], \texttt{AWAIT} is an atomic command that executes under the precondition of the \texttt{AWAIT} block.

In the datatype above, the concrete syntax is defined within (" ... "). \(\alpha\ \texttt{assn}\) and \(\alpha\ \texttt{bexp}\) represent assertions and Boolean expressions, respectively. \texttt{AnnBasic} represents a basic (atomic) state transformation (e.g., an assignment). \texttt{AnnSeq} is sequential composition, \texttt{AnnCond} is conditional, \texttt{AnnWhile} is a loop annotated with an invariant, and \texttt{AnnAwait} is a synchronisation construct. The command \texttt{Parallel} is a list of pairs \((c, q)\) where \(c\) is an annotated (sequential) command and \(q\) is a post-condition. The concrete syntax for parallel composition (not shown above) is: \texttt{COBEGIN} \(c_1 \{q_1\} || ... || c_n \{q_n\}\ \texttt{COEND}.

The semantics of programs are defined by transition rules between configurations, which are pairs comprising a program fragment and a state. The proof rules of the Owicki-Gries formalisation are syntax directed. A proof obligation generator has been implemented in the form of an Isabelle tactic called \texttt{oghore}. Application of this tactic results in generation of all standard Owicki-Gries proof obligations, each of which can be discharged either automatically or via an interactive proof.

We omit the full details of standard semantics and verification condition generator [28].

Example 1 (Message passing (MP)). To motivate our extensions to a C11-style weak memory model, we consider the \textit{message passing} litmus test given in Fig. 1. It comprises two shared variables: \(d\) (that stores some data) and \(f\) (that stores a flag), both of which are initially 0. Under sequential consistency, the postcondition of the program is \(r_2 = 5\). This is because the loop in thread 2 only terminates after \(f\) has been updated to 1 in thread 1, which in turn happens after \(d\) has been set to 5 by thread 1. Therefore, the only possible value of \(d\) for thread 2 to read is 5. The proof of this property straightforward, and can be easily handled by Nipkow and Nieto’s encoding [28]. We provide a partial encoding in Fig. 2 to provide an example instantiation of the overview of this encoding here; an interested reader may wish to consult the original paper [28] for further details.
abstract syntax above, and to better highlight the extensions necessary to handle C11-style weak memory. The state of the program is defined using an Isabelle record where all shared variables and local registers are modelled as its fields. For the proof outline in Fig. 2, the oghoare tactic generates 29 proof obligations, each of which is automatically discharged.

3 Extending Owicki-Gries to C11-Style Memory Models

We defer a precise description of a C11-style operational semantics to Section 4 in order to highlight the fact our Isabelle framework is essentially parametric in the memory model used. The fundamental requirement is that the memory model be an operational model featuring C-style, annotated memory operations. All that is needed to understand the rest of this section is some basic familiarity with weak memory models [9, 11, 19, 31]. The functions encoding the weak memory operational semantics \( \text{WrX}, \text{WrR}, \text{RdX}, \ldots \) will be instantiated Section 4 and for the time being can be considered to be transition functions that construct a new weak memory state for a given weak memory prestate. However, a reader may wish to first read Section 4 for an example C11 memory model prior to continuing with the rest of this section.

To motivate our language extension, we reconsider MP (Example 1) in a C11-style weak memory model. In particular, if all reads and writes are relaxed, C11 admits an execution in which thread 2 reads a “stale” value of \( d \) [19, 25]. Thus, it is only possible to establish the weaker postcondition \( r2 = 0 \lor r2 = 5 \) (see Section 4 for details). To regain the expected behaviour, one must introduce additional synchronisation in the program. In particular, the write to \( f \) in thread 1 must be a releasing write (denoted \( f := R1 \)) and the read of \( f \) in thread 2 must be an acquiring read (denoted \( r1 \leftarrow A f \)).

A weak memory state can be encoded as a special variable in the standard semantics. Moreover, for the semantics that we employ [9, 11], within each weak memory state, for each low-level weak memory event (e.g., read or write) we must keep track of the thread identifier (of type \( T \)), the shared variable (or location) that is accessed (of type \( L \)) and the value in that variable (of type \( V \)).

The syntactic extensions necessary for encoding C11-style statements in Isabelle are straightforward. For example, to capture the so-called RAR fragment, we require five new programming constructs: relaxed reads and writes, releasing writes, and acquiring reads. Moreover, we wish to support a \( \text{SWAP}[x, v] \) command [11, 39] that acquiringly reads \( x \) and releasingly writes \( v \) to \( x \) in a single atomic step. This command is used in Peterson's algorithm (see Fig. 10) and is implemented in our model using a read-modify-write update.
All of the new extensions are defined using a shallow embedding and their concrete syntax is enclosed in brackets < ... > to avoid ambiguities in the Isabelle/HOL encoding. The annotated versions of these statements are given below. For completeness, we also require syntax for unannotated versions of each command, but their details are elided.

**Syntax**

```
syntax
"_AnnWrX" :: "α assn ⇒ L ⇒ T ⇒ V ⇒ Cstate ⇒ α ann_com"
("(_ <_ :=_ _ R _ >)"
"_AnnWrR" :: "α assn ⇒ L ⇒ T ⇒ V ⇒ Cstate ⇒ α ann_com"
("(_ <_ :=R _ _ >)"
"_AnnRdX" :: "α assn ⇒ idt ⇒ T ⇒ L ⇒ Cstate ⇒ α ann_com"
("(_ <_ ←_ _ >)"
"_AnnRdA" :: "α assn ⇒ idt ⇒ T ⇒ L ⇒ Cstate ⇒ α ann_com"
("(_ <_ ←A _ _ >)"
"_AnnSwap" :: "α assn ⇒ L ⇒ V ⇒ T ⇒ Cstate ⇒ α ann_com"
("(_ <SWAP[_, _]_ >)"
```

Antiquotations of the form $x$ are used to denote that the element $x$ is a field of the record corresponding to the state of each program. For example, for the program in Fig. 2 the variables $d$, $f$, $r1$ and $r2$ of record $mp_state$ would be interpreted in the syntax using antiquotated variables. This allows the translations (see below) to update fields in an external record yet for the programs themselves to be written using a natural imperative syntax.

To cope with weak memory, we embed the weak memory state as a special variable in the standard encoding (see Figs. 7 and 8). Each operation induces an update to this embedded weak memory state variable that can be observed by subsequent operations on the weak memory state.

`_AnnWrX` defines a relaxed write. Its first argument is an assertion (the precondition) of the command, the second is the variable being modified, the third is the thread performing the operation, the fourth is the value being written, and the fifth is the weak memory prestate. Similarly, `_AnnWrR` is a releasing write. `_AnnRdX` defines a relaxed read, which loads a value of the given location (of type $L$) from the given weak memory prestate into the second argument (of type $idt$). An acquiring read, defined by `_AnnRdA` is similar. Finally, `_AnnSwap` defines a swap operation that writes the given value (third argument) to the given location (second argument) using an update operation.

The semantics of this extended syntax is given by a translation, which updates the program variables, including the weak memory state. For the commands above, after omitting some low-level Isabelle details, we have:

**Translations**

```
translations
"r < x :=_ t v ´ s>" →
"AnnBasic r (_update_name s (WrX´s x v t))"
"r < x :=R t v ´ s>" →
"AnnBasic r (_update_name s (WrR´s x v t))"
"r < x ←_ t y ´ s>" →
"AnnAwait r ((_update_name s (fst (RdX´s y t))),
(_update_name x (snd (RdX´s y t))))"
"r < x ←A t y ´ s>" →
"AnnAwait r ((_update_name s (fst (RdA´s y t))),
(_update_name x (snd (RdA´s y t))))"
"r <SWAP[x, v]_ t´s>" → "AnnBasic r (fst (Upd´s x v t))"
```

These translations rely on an operational semantics defined by functions $W_{RX}$ (relaxed write), $W_{RA}$ (releasing write), $R_{DX}$ (relaxed read), $R_{DA}$ (acquiring read) and $Upd$ (RMW update), which we define in Section 4.2.

Relaxed and acquiring writes update the embedded weak memory state to the state returned by $W_{RX}$ and $W_{RA}$, respectively. A read event must return a post state (which is used to update the value of the embedded weak memory state) and the value read (which is used to update the value of the local variable storing this value). In order to preserve atomicity of the read, we wrap both updates within an annotated $AWAIT$ statement. The translation of a $SWAP$ is similar.

Note that a relaxed (acquiring) read comprises two calls to $R_{DX}$ ($R_{DA}$), which one could mistakenly believe to cause two different effects on the weak memory state. However, as we shall see, these operations are implemented using Hilbert choice ($\text{SOME}$), hence, although there may be multiple values that a read could return, the two applications of $R_{DX}$ ($R_{DA}$) are identical for the same value for the same parameters.

4 A C11-Style Memory Model: RC11-RAR

In this section, we describe a particular instance of a C11-style memory model: the RC11-RAR fragment. This fragment disallows the load buffering litmus test [6, 23, 24], and all accesses are either relaxed, releasing or acquiring. It is straightforward to extend the model to incorporate more sophisticated notions such as release sequences and non-atomic accesses, but these are not considered as the complications they induce detract from the main contribution of our work. It is worth noting that RC11-RAR is still a non-trivial fragment [11].

4.1 Message Passing

To motivate the memory model, consider again the MP litmus test but for RC11-RAR (Figs. 3 and 4). In Fig. 3, all accesses are relaxed, and hence the program can only establish the weaker postcondition $r_2 = 0 \lor r_2 = 5$ since it is possible for thread 2 to read 0 for $d$ at line 4. In Fig. 4, the release annotation (line 2) and the acquire annotation (line 3) induces a happens-before relation if the read of $f$ reads from the write at line 2 [6]. This in turn ensures that thread 2 sees the most recent write to $d$ at line 5.

We use the operational semantics described in [9], which models the weak memory state using timestamped writes and thread view fronts [15, 19, 20, 21]. A timestamp is a rational number that totally orders the writes to each variable. A viewfront records the timestamp that a thread has encountered for each variable — the idea is that a thread may read from any write whose timestamp is no smaller than the thread’s current viewfront. Similarly, a write may be introduced at any timestamp greater than the current viewfront. The only caveat when introducing a write is that it may not be introduced directly after a covered write (see [9, 11]). This caveat is to ensure atomicity.

\begin{figure}[h]
\centering
\begin{align*}
\text{Init: } & d := 0; f := 0; \\
\text{Thread 1: } & 1: d := 5; \\
& 2: f := 1; \\
& 4: r_2 \leftarrow d; \{r_2 = 0 \lor r_2 = 5\}
\end{align*}
\begin{align*}
\text{Thread 2: } & 3: \text{do } r_1 \leftarrow f \\
& \text{until } r_1 = 1; \\
& 6: f := R_1; \\
& 8: r_2 \leftarrow d; \{r_2 = 5\}
\end{align*}
\caption{Unsynchronised MP under RC11-RAR}
\end{figure}

\begin{figure}[h]
\centering
\begin{align*}
\text{Init: } & d := 0; f := 0; \\
\text{Thread 1: } & 5: d := 5; \\
& 6: f := R_1; \\
& \text{until } r_1 = 1; \\
\text{Thread 2: } & 7: \text{do } r_1 \leftarrow A f \\
& \text{until } r_1 = 1; \\
& 8: r_2 \leftarrow d; \{r_2 = 5\}
\end{align*}
\caption{MP with release-acquire synchronisation}
\end{figure}
of RMW operations. In particular, a write to a variable \( x \) is covered whenever there is a RMW on \( x \) that reads from the write. In this instance, it would be unsound for another write to \( x \) to be introduced between the write that is read and the RMW (see [11] for further details).

**Example 2 (Unsynchronised MP).** Consider Fig. 5 depicting a possible execution of the unsynchronised MP example (Fig. 3). The execution comprises four weak memory states \( \sigma_0, \sigma_1, \sigma_2, \sigma_3 \). In each state, the timestamps themselves are omitted, but are assumed to be increasing in the direction of the arrows. The numbers depict the value of each variable at each timestamp. State \( \sigma_0 \) is the initial state. Each thread’s viewfront in \( \sigma_0 \) is consistent with the initial writes.

After executing line 1, the program transitions to \( \sigma_1 \), which introduces a new write (with value 5) to \( d \) and updates the viewfront of thread 1 to the timestamp of this write. At this stage, thread 2’s viewfront for \( d \) is still at the write with value 0. Thus, if thread 2 were to read from \( d \), it would be permitted to return either 0 or 5. Moreover, if thread 2 were to write to \( d \), it would be permitted to insert the write after 0 or 5.

After executing line 2, the program transitions to \( \sigma_2 \), which installs a (relaxed) write of \( f \) with value 1. Now, consider the execution of line 3. There are two possible poststates since there are two possible values of \( f \) that thread 2 could read. State \( \sigma_3 \) depicts the case where thread 2 reads from the new write \( f = 1 \). In this case, the viewfront of thread 2 is updated, but crucially, since there is no release-acquire synchronisation, the viewfront of thread 2 for \( d \) remains unchanged. This means that when thread 2 later reads from \( d \) in line 4, it may return either 0 or 5. We contrast this with the execution of the synchronised MP described in Example 3.

**Example 3 (Synchronised MP).** Consider Fig. 6 which depicts an execution of the program in Fig. 3. State \( \tau_1 \) is a result of executing line 5 and is identical to \( \sigma_1 \). However, after execution of line 6, we obtain state \( \tau_1 \), which installs a releasing write to \( f \) (denoted by \( 1^R \)). As in Example 2 the acquiring read in line 7 could read from either of the writes to \( f \). State \( \tau_3 \) depicts the case in which thread 2 reads from the releasing write \( 1^R \). Now, unlike Example 2, this read establishes a release-acquire synchronisation, which means that the viewfront of thread 2 for both \( f \) and \( d \) are updated. Thus, if the execution continues so that thread 2 reads from \( d \) (line 8), the only possible value it may return is 5.

### 4.2 Operational Semantics of C11 RAR in Isabelle/HOL

We now present details of the memory model from Section 4.1 as encoded in Isabelle/HOL. Recall that the main purpose of this section is to instantiate the functions \( \text{WrX}, \text{WR}, \text{RdX}, \text{RdA} \) and \( \text{Upd} \) from Section 3.
Recall that type $\mathbf{L}$ represents shared variables (or locations), $\mathbf{T}$ represents threads, and $\mathbf{V}$ represents values. We use type $\mathbf{TS}$ (which is synonymous with rational numbers) to represent timestamps. Each write can be uniquely identified by a variable-timestamp pair. The type $\mathbf{Cstate}$ is a nested record with fields

- $\text{writes}$, which is the set of all writes,
- $\text{covered}$, which is the set of covered writes (recalling that covered writes are used to preserve atomicity of read-modify-write updates),
- $\text{mods}$, which is a function mapping each write to a write record (see below),
- $\text{tview}$, which is the viewfront ($\mathbf{L} \Rightarrow (\mathbf{L} \times \mathbf{TS})$) of each thread, and
- $\text{mview}$, which is the viewfront of each write.

A write record contains fields $\text{val}$, which is the value written and $\text{rel}$, which is a Boolean that is True if, and only if, the corresponding write is releasing.

\begin{verbatim}
record Cstate =
  writes :: (\mathbf{L} \times \mathbf{TS}) set
  covered :: (\mathbf{L} \times \mathbf{TS}) set
  mods :: (\mathbf{L} \times \mathbf{TS}) \Rightarrow \text{write_record}
  tview :: \mathbf{T} \Rightarrow \mathbf{L} \Rightarrow (\mathbf{L} \times \mathbf{TS})
  mview :: (\mathbf{L} \times \mathbf{TS}) \Rightarrow \mathbf{L} \Rightarrow (\mathbf{L} \times \mathbf{TS})

record write_record =
  val :: \mathbf{V}
  rel :: \text{bool}
\end{verbatim}

Next, we describe how the operations modify the weak memory state.

**Read transitions.** Both relaxed and acquiring reads leave all state components unchanged except for $\text{tview}$. To define their behaviours, we first define a function $\text{visible_writes} \sigma t x$ that returns the set of writes to $x$ that thread $t$ may read from in state $\sigma$. For a write $w = (x, q)$, we assume a pair of functions $\text{var} w = x$ and $\text{tst} w = q$ that return the variable and timestamp of $w$, respectively. Thus, we obtain:

\begin{verbatim}
definition "\text{visible_writes} \sigma t x \equiv\{w \in \text{writes} \sigma . \text{var} w = x \land \text{tst}(\text{tview} \sigma t x) \leq \text{tst} w\}"
\end{verbatim}

We use a function $\text{getVW}$ to select some visible write from which to read:

\begin{verbatim}
definition "\text{getVW} \sigma t x \equiv\{\text{SOME} w . w \in \text{visible_writes} \sigma t x\}"
\end{verbatim}

Finally, we require functions $\text{read_transX} t w \sigma$ and $\text{read_transA} t w \sigma$ that update the $\text{tview}$ component of $\sigma$ for thread $t$ reading write $w$. Function $\text{read_transX} t w \sigma$ updates $\text{tview} \sigma t$ to $(\text{tview} \sigma t)[\text{var} w := w]$, where $f[x := v]$ denotes functional override. That is, the viewfront of thread $t$ for variable $\text{var} w$ is updated to the write $w$ that $t$ reads. The viewfronts of the other
threads as well as the viewfront of \( t \) on variables different from \( \text{var} \ w \) are unchanged. Thus, the function \( \text{RdX} \) required by the translation of a relaxed read command in Section 3 is thus defined by:

\[
\text{definition \ value } \sigma \ w \equiv \text{val} (\text{mods } \sigma \ w)
\]

\[
\text{fun \ RdX :: } L \Rightarrow T \Rightarrow \text{Cstate} \Rightarrow (\text{Cstate} \times V)
\]

\[
\quad \text{where}
\quad \text{RdX } x \ t \ \sigma = (\text{let } w = \text{getVW } \sigma \ t \ x; v = \text{value } \sigma \ w \ \text{in} \ (\text{read_transX } t \ w \ \sigma, v))
\]

We use \( \text{value } \sigma \ w \) to obtain the value of the write \( w \) in state \( \sigma \). The update defined by function \( \text{read_transA} \ t \ w \ \sigma \) for an acquiring read is conditional on whether \( w \) is a relaxed write. If \( w \) is relaxed, \( \text{tview } \sigma \ t \) is updated to \( (\text{tview } \sigma \ t)[\text{var } w := w] \) (i.e., behaves like a relaxed read). Otherwise, the viewfront of \( t \) must be updated to “catch up” with the viewfront of \( w \). In particular, \( \text{tview } \sigma \ t \) is updated to \( (\text{tview } \sigma \ t) \otimes (\text{mview } \sigma \ w) \), where

\[
(f \otimes g) \ x = \begin{cases} v_1 \ x & \text{if } \text{tst}(v_2 \ x) \leq \text{tst}(v_1 \ x) \\ v_2 \ x & \text{otherwise} \end{cases}
\]

Overall, we have:

\[
\text{fun \ RdA :: } L \Rightarrow T \Rightarrow \text{Cstate} \Rightarrow (\text{Cstate} \times V)
\]

\[
\quad \text{where}
\quad \text{RdA } x \ t \ \sigma = (\text{let } w = \text{getVW } \sigma \ t \ x; v = \text{value } \sigma \ w \ \text{in} \ (\text{read_transA } t \ w \ \sigma, v))
\]

**Write transition.** Writes update all state components except \( \text{covered} \). First, following Doherty et al. [11], we must identify an existing write \( w \) in the current state; the new write is to be inserted immediately after \( w \). Moreover, \( w \) must be visible to the thread performing the write and covered by an RMW update. We define the following function to

\[
\text{definition "getVWNC } \sigma \ t \ x \equiv
\text{SOME w . w } \in \ \text{visible_writes } \sigma \ t \ x \ \land \ w \not\in \ \sigma \ \text{covered}"
\]

where \( \text{NC} \) stands for “not covered”. The write operation must also determine a new timestamp, \( \text{ts} \) for the new write. Given that the new write is to be inserted immediately after the write operation \( w \), the timestamp \( \text{ts} \) must be greater than \( \text{tst } w \) but smaller than the timestamp of other writes on \( \text{var } w \) after \( w \). Thus, we obtain a new timestamp using:

\[
\text{definition "getTS } \sigma \ w \equiv
\text{SOME ts . \ \text{tst } w < \text{ts} \ \land
(\forall w' \in \text{writes } \sigma . \ \text{var } w' = \text{var } w \ \land \ \text{tst } w < \text{tst } w' \rightarrow
\text{ts < tst } w')"
\]

Finding such a timestamp is always possible since timestamps are rational numbers (i.e., are dense).

As with reads, we require a function \( \text{write_trans } t \ b \ w \ v \ \sigma \ \text{ts} \) that updates the state \( \sigma \) so that a new write \( w' = ((\text{var } w), \ \text{ts}) \) for thread \( t \) is introduced with write value \( v \). The Boolean \( b \) is used to distinguish relaxed and releasing writes. The write \( w \) is the write after which the new write \( w' \) is to be introduced. The effect of \( \text{write_trans} \) is to update \( \text{writes } \sigma \) to \( \text{writes'} \), \( \text{mods } \sigma \) to \( \text{mods'} \) and both \( \text{tview } \sigma \ t \) and \( \text{mview } \sigma \ w \) to \( \text{tview'} \), where:

\[
\text{writes'} = (\text{writes } \sigma) \cup \{w'\}
\]

\[
\text{mods'} = (\text{mods } \sigma \ w')[\text{val} := v, \text{rel} := b]
\]

\[
\text{tview'} = (\text{tview } \sigma \ t)[(\text{var } w) := w']
\]
Thus, writes' adds the new write w' to the set of writes of σ. The new mods' sets the value for w' to v and the rel field to b (which is True iff the new write w' is releasing). Finally, tview' updates tview of t for variable var w (the variable that both w and w' update) to w'.

Finally, the functions WrX and WrR required by the translations in Section 3 are given as follows:

```
fun WrX :: "L ⇒ V ⇒ T ⇒ Cstate ⇒ Cstate" where
  "WrX x v t σ = (let w = getVWNC σ t x ; ts' = getTS σ w in write_trans t False w v ts')"

fun WrR :: "L ⇒ V ⇒ T ⇒ C ⇒ state ⇒ Cstate" where
  "WrR x v t σ = (let w = getVWNC σ t x ; ts' = getTS σ w in write_trans t True w v ts')"
```

Update transition. Following Doherty et al. [11], we assume that an update performs both an acquiring read and a releasing write in a single step. It is possible to define variations that do not synchronise the read or a write, but we omit such details for simplicity.

We first define a function update_trans t w v σ ts that modifies σ so that a releasing write w' = ((var w), ts) by thread t is introduced with write value v immediately after an existing write w. The effect of update_trans is to update writes σ to writes', covered σ to covered', and mods σ to mods', and both tview σ t and mview σ w' to tview', where

```
writes' = (writes σ) ∪ {w'}
covered' = (covered σ) ∪ {w}
mods' = (mods σ w')[val := v, rel := True]
```

Thus, writes' adds the new write w' corresponding to the update to the set of writes of σ and covered' adds the write w that w' reads from to the covered writes set of σ. The new mods' sets the value for w' to v and sets the rel field to True. Finally, tview' updates tview of t in the same way as a read operation, except that the first case is taken provided the write w being read is releasing.

The function Upd required by the translation in Section 3 is given as follows:

```
fun Upd :: "L ⇒ V ⇒ T ⇒ Cstate ⇒ (Cstate × V)" where
  "Upd x v t σ = (let w = getVWNC σ t x ; ts = getTS σ w ; v = value σ w in
    (update_trans t w v σ ts , v))"
```
Function \texttt{writes_on } \sigma \ x \text{ returns the set of writes in } \sigma \text{ to variable } x. \text{ Function } \texttt{lastWr } \sigma \ x \text{ returns the write on } x \text{ whose timestamp is greater than the timestamp of all other writes on } x \text{ in state } \sigma.

In the definition of \texttt{wfs } \sigma, \text{ the first two conjuncts ensure that all writes recorded in } \texttt{tview} \text{ and } \texttt{mview} \text{ are consistent with } \texttt{writes } \sigma. \text{ The third ensures the set of writes in } \sigma \text{ is finite and the fourth ensures that for each write in } \sigma, \text{ the write's modification view of the variable it writes is the write itself. The final conjunct ensures that the last write to each variable (i.e., the write with the largest timestamp) is not covered. We have shown that } \texttt{wfs} \text{ is stable under each of the transitions } \texttt{WrX}, \texttt{WrR}, \ldots. \text{ Thus the well-formedness assumption made by the lemmas in Section 5 is trivially guaranteed.}

5 An Assertion Language for Verifying C11 Programs

In the previous sections, we discussed how the existing Owicki-Gries theories in Isabelle can be extended with a weak memory C11 operational semantics in order to reason about C11-style programs using standard proof rules. We mentioned that how a novel set of assertions introduced in [9] can be used in our extension to annotate programs w.r.t. C11 state and reason about them. In this section we introduce the assertion language and present their encodings in Isabelle through a number of examples and litmus tests. We also provide some of the rules (lemmas) that Isabelle uses to discharge proof obligations and validate the proof outlines. We show how C11 state is incorporated into the programs and shared variables are defined. We also present a fully verified encoding of the Peterson's mutual exclusion algorithm to further validate our approach.

5.1 Load Buffering

Our first example is the load-buffering litmus test given in Fig. 7. As discussed earlier, we use restricted C11 memory model described by Lahav et al. [23], and hence we prevent the program from terminating by reading 1 for both \( x \) in thread 1 and \( y \) in thread 2.

As mentioned earlier, the C11 state is represented as a field of the record corresponding to the state of the program (i.e. as a field of \texttt{lb_state} record for the load-buffering example). Updates to \( \sigma \) are via the underlying definition of the operations in accordance with the RC11-RAR operational semantics as described in Section 4.2. In our encoding, shared variables are represented as constants representing locations in the C11 state (\( \sigma \)).

Now consider the proof outline. The first assertion (lines 10-12) specifies the initial state of the program. The first two conjuncts are assertions on the value of local registers. The other four conjuncts are \textit{definite observation} assertions. A definite observation assertion denoted \([x = t \ n] \sigma\) states that thread \( t \)'s viewfront is consistent with the last write to \( x \) in \( \sigma \) and that this write has value \( n \). Thus, if \( t \) reads from \( x \), it is guaranteed to return \( n \). \( \sigma \). Formally,

\[
[x = t \ n] \sigma \equiv \text{tview } \sigma \ t = \text{lastWr } \sigma \ x \land \text{value } \sigma \ (\text{lastWr } \sigma \ x) = n
\]

All weak-memory assertions in the proof outline of Fig. 7 are definite value assertions, and this is sufficient to prove the postcondition. However, to discharge the generated proof obligations, we require the following two proof rules over C11 assertions, which are defined as Isabelle lemmas:
lemmas d_obs_RdX_pres and d_obs_WrX_diff_var_pres give conditions for preserving definite value assertions for relaxed read and write transitions, respectively for an arbitrary variable \( y \) and thread \( t' \). Note d_obs_WrX_diff_var_pres requires that the variable \( y \) that is written to is different from the variable \( x \) that appears in the definite value assertion. Both lemmas are proved sound with respect to the operational semantics in Section 4.2. Of course d_obs_RdX_pres also holds for an acquiring read transition and d_obs_WrX_diff_var_pres for a releasing write transition.\(^5\)

The assertions on lines 14 and 20 are locally correct because of the initial state. The assertions on lines 16 and 22 are locally correct using d_obs_RdX_pres. Local correctness of the assertions on lines 18 and 24 is trivial follows by the definite value assertion. Interference freedom of the assertions in lines 14, 16, 20 and 22 is also established using the two lemmas.

5.2 Message-Passing

We now consider the assertions used in the message-passing algorithm (Fig. 8). The first new assertion used in the proof outline is the possible observation assertion. This assertion (denoted \([x = t \_ u] (\text{WrX } y \_ v \_ t' )\) )

\(^5\) In fact, our Isabelle theory provides a generic lemma that applies to both cases simultaneously.

\begin{verbatim}
consts x :: L  y :: L

record lb_state =
  r1 :: V
  r2 :: V
  σ :: Cstate

COBEGIN
  \{ \[ y = 0 \] \sigma \land \[ x = 0 \] \sigma \land \}

\begin{verbatim}
consts d :: L  f :: L

record mp_state =
  r1 :: V  r2 :: V  σ :: Cstate

\begin{verbatim}
lemma d_obs_RdX_pres:
  assumes "wfs σ" and "[x = t \_ u] σ"  
  shows "[x = t \_ u] (\text{RdX } y \_ t' \sigma)"

lemma d_obs_WrX_diff_var_pres:
  assumes "wfs σ" and "[x = t \_ u] σ" 
  shows "[x = t \_ u] (\text{WrX } y \_ v \_ t' \sigma)"
\end{verbatim}

Fig. 7. Isabelle encoding of the load-buffering litmus test.

Fig. 8. Isabelle encoding of the message-passing litmus test.
\end{verbatim}
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\[ [x \approx_t n] \sigma \equiv \exists w. w \in \text{visible_writes} \sigma \ t x \land n = \text{value} \sigma w \]

The next assertion we introduce is the conditional observation assertion (denoted \([x = n] \llparenthesis y = t m \rrparenthesis \sigma\)) which states that if thread \(t\) reads a value \(n\) using an acquiring read for \(x\), it synchronises with the corresponding write and obtains the definite value \(m\) for \(y\). Note that this requires that any write to \(x\) with value \(n\) that \(t\) can read is a releasing write. The formal definition in Isabelle is as follows:

\[ [x = n] \llparenthesis y = t m \rrparenthesis \sigma \equiv \forall w. w \in \text{visible_writes} \sigma \ t x. \text{value} \sigma w = n \rightarrow mview \sigma w y = \text{lastWr} \sigma y \land \text{value} \sigma (\text{lastWr} \sigma y) = m \land \text{rel} (\text{mods} \sigma w) \]

Here we only introduce two of the interesting rules used in the proof, and refer the interested reader to the Isabelle theories for the remaining lemmas:

**Lemma c_obs_intro:**

assumes "wfs \sigma"
and "[y = t m] \sigma"
and "[x \approx_t n] \sigma"
and "x \neq y"
and "t \neq t'"
such that 
shows "[x = u][y = t v] (\text{WrR} x u t \sigma)"

**Lemma c_obs_transfer:**

assumes "wfs \sigma"
and "[x = u][y = t v] \sigma"
and "\text{snd}(\text{RdA} x t \sigma) = u"
shows "[y = t v] (\text{fst}(\text{RdA} x t \sigma))"

Consider the conditional observation assertion in line 17. Local correctness holds trivially by initialisation. Interference freedom under line 12 is straightforward. For interference freedom under line 14, we use \text{c_obs_intro}. In particular, the assertion at line 13 (i.e., the precondition of line 14) satisfies the critical premises of \text{c_obs_intro}. We use the conditional observation assertion (line 17 of thread 2) in combination with rule \text{c_obs_transfer} to establish a definite observation on a new variable in thread 2. We note that the variable read by the transition in rule \text{c_obs_transfer} is \(x\), whereas the definite value assertion in the consequent is on variable \(y\). Full details of this proof may be found in [9]; in this paper, we focus on automation, which we discuss in Section 5.5.

### 5.3 Read-Read Coherence

We have verified three versions of the read-read coherence (RRC) litmus test using our extended theories. We have provided the more interesting of the three in Fig. 9. The other two versions are provided Appendix A. In order to prove this example, a richer set of assertions is required. In particular, in addition to the assertions regarding observability of writes, we need assertions about the order of writes and the limits on the occurrence of values.

The first assertion used for this example that we discuss here is the possible value order assertion (denoted \([m \prec_x n] \sigma\)), which states that there exists a write to variable \(x\) with value \(n\) ordered after (i.e., with a greater timestamp) a write to \(x\) with value \(m\). Similarly, a definite value order assertion (denoted \([m \prec_x n] \sigma\)) states that all writes to \(x\) with value \(n\) are ordered after all writes to \(x\) with value \(m\). These are formally defined in Isabelle as follows:

\[ [m \prec_x n] \sigma \equiv \exists w. w \in \text{writes_on} \sigma x \land w' \in \text{writes_on} \sigma x \land \]
value $\sigma w = m \wedge value \sigma w' = n \wedge (tst w) < (tst w')$

$[m \prec x n] \sigma \equiv$

$(\forall w w'. \ w \in writes_on \sigma x \wedge w' \in writes_on \sigma x \wedge$

$\text{value} \ \sigma w = m \wedge \text{value} \ \sigma w' = n \rightarrow (tst w) < (tst w'))$

$\land [m \prec x n] \sigma$

The other two assertions appear in this proof outline fall into the value occurrence category:

$[0_x n]_i \sigma \equiv$\text{init} $\sigma x n \land \neg[i \prec x n]$

$[1_x n] \sigma \equiv \neg[n \prec x n]$

The last new assertion used in this proof outline is encountered value (denoted as $[x \equiv_t n]$)

$[x \equiv_t n] \sigma \equiv \exists w . w \in writes_on \sigma x \land value \ \sigma w = n \land$

$(\forall w' \in writes_on \sigma x . w \neq w' \rightarrow (tst w) < (tst w'))$

The five assertions above, together with other assertions introduced earlier, are sufficient to specify the behaviour of the three-threaded version of RRC. The conditional observation assertion on line 18, is used to capture the possible synchronisation between threads 1 and 2. The ordering assertions in thread 2 and 3 specify that if the writes have happened in a specific order, the read order must remain coherent with respect to the order of writes. Namely, if thread 2 synchronises with thread 1 (i.e., $r1$ is set to 1), then it must have observed the write of $x$ at line 12. Thus, the write to $x$ with value 2 at line 23 must have happened after. Therefore, it must be impossible for the third thread to read value 2 for $x$ at line 27, then subsequently read 1 for $x$ at line 29. This reasoning is captured by the postcondition of the program.

5.4 Peterson’s Algorithm for C11

The final non-trivial example in this paper is Peterson’s mutual exclusion algorithm (Fig. 10) as described in [39]. The proof outline for this algorithm has the new assertion covered (denoted $\text{cvd}[x, n] \sigma$). The assertion $\text{cvd}[x, n] \sigma$ means that every write to $x$ in state $\sigma$ except the last is covered and the value written by that last write is $n$. This assertion is formally defined in Isabelle as:

$\text{cvd}[x, n] \sigma \equiv \forall w . w \in writes \sigma \wedge \text{var} \ \sigma w = x \wedge w \notin \text{covered} \sigma \rightarrow$

$w = \text{lastWr} \ \sigma x \wedge \text{value} \ \sigma w = n$

6 Note that some of the notation in our Isabelle encoding is different. We use the notation from [9] here for a cleaner presentation.
consts
recc3_state =
\begin{align*}
\text{COBEGIN} &\quad \text{record} \quad rrc3\_state = \\
\text{COEND} &\quad a :: V \quad b :: V \quad r1 :: V \\
\sigma :: \text{Cstate} \\
\end{align*}

Fig. 9. Isabelle encoding of the read-read coherence litmus test with three threads. The proof additionally relies on a global invariant \([\text{init} \ x \ 0] \ \sigma \land [\text{init} \ y \ 0] \ \sigma \land [1, 1] \ \sigma \land [1, 2] \ \sigma\) Similar to the previous examples, in order to prove the Peterson’s algorithm we will need to introduce new proof rules to deal with assertions involving cvd.

The proof also uses auxiliary variables after1 and after2. We set after1 to True when turn is set in thread 1 and to False when thread 1 exits its critical section (i.e., when the flag is reset). This is a standard technique used in Owicki-Gries proofs of Peterson’s algorithm in the conventional, sequentially consistent, setting \cite{25,28}. Note that introduction of auxiliary variables must follow the same rules as the classical setting \cite{29} and must not be a shared constant that appears within the weak memory state \(\sigma\). This avoids the notions of unsoundness of auxiliary variables described in earlier work \cite{25}.

5.5 Verification Strategy

For each of the algorithms described above, we employ a generic verification strategy and outline the proof effort. After encoding the algorithm and the assertions, the main steps in each validating the proof outlines are as follows.

1. First, we use the built-in oghoare tactic to reduce an Owicki-Gries proof outline into a set of basic Hoare logic proof obligations over weak memory pre-post state assertions. This tactic is exactly as developed by Nipkow and Nieto \cite{28}, and is used without change.

2. We pipe this output (which is a set of proof obligations on atomic commands) to the Isabelle simplifier, transforming the set-based representation of assertions by Nipkow and Nieto into a predicate-based representation. This allows the lemmas for weak memory that we have adapted from \cite{9} to be automatically matched with the proof obligations.

For the simple litmus tests, the first two steps either discharge all the proof obligations, or leave a few (maximum 6) proof obligations unproved. These proof obligations require slightly more sophisticated application of the lemmas over weak memory state than can be discharged by the simplifier alone. However, they can be automatically discharged using Isabelle’s built-in sledgehammer tool \cite{7}.

This verification strategy works equally well for Peterson’s algorithm although it is a larger example that generates a significantly higher number of proof obligations. The oghoare tactic generates 258 subgoals, but over half of these are discharged by step 2 above, leaving 91 subgoals.
\[\begin{align*}
\text{after1} \land \neg \text{after2} \land [\text{flag1} = 1] \sigma \land [\text{flag2} = 2] \sigma \\
\land [\text{turn} = 1] \sigma \land [\text{turn} = 2] \sigma
\end{align*}\]

\text{COBEGIN}
\[\begin{align*}
\neg \text{after1} \land [\text{flag1} = 1] \sigma \land (\text{cvd}[\text{turn}, 0] \sigma \lor \text{cvd}[\text{turn}, 1] \sigma) \\
\land (\text{after2} \rightarrow \text{cvd}[\text{turn}, 1] \sigma \land [\text{turn} = 1][\text{flag2} = 1] \sigma) \\
\land \neg [\text{turn} \approx 2] \sigma
\end{align*}\]

\(<\text{flag1} := 11 \sigma>;;
\]

\[\begin{align*}
\neg \text{after1} \land [\text{flag1} = 11] \sigma \land \neg [\text{turn} \approx 2] \sigma \\
\land (\text{after2} \rightarrow \text{cvd}[\text{turn}, 1] \sigma \land [\text{turn} = 1][\text{flag2} = 1] \sigma) \]
\]

\(<\text{SWAP}[\text{turn}, 2], \sigma>,, \text{after1} := \text{True} >;;
\]

\text{DO}
\[\begin{align*}
\text{after1} \land (\text{after2} \land ([\text{flag2} \approx 1] \sigma \lor [\text{turn} \approx 1] \sigma) \rightarrow [\text{turn} = 2] \sigma))
\end{align*}\]

\(<\text{r1} := \text{flag2} \sigma>;;
\]

\[\begin{align*}
\text{after1} \land (\text{after2} \land (\text{r1} = 0 \lor [\text{turn} \approx 1] \sigma \lor [\text{flag2} \approx 1] \sigma) \rightarrow [\text{turn} = 2] \sigma))
\end{align*}\]

\(<\text{r2} := \text{0} \text{r1} \sigma>\)

\text{UNTIL} \ (\text{r1} = 0 \lor \text{r2} = 1)

\text{INV}
\[\begin{align*}
\text{after1} \land (\text{after2} \land (\text{r1} = 0 \lor \text{r2} = 1 \lor [\text{turn} \approx 1] \sigma \lor [\text{flag2} \approx 1] \sigma) \rightarrow [\text{turn} = 2] \sigma))
\end{align*}\]

\text{OD};;
\[\begin{align*}
\text{after1} \land (\text{after2} \rightarrow [\text{turn} = 2] \sigma))
\end{align*}\]

\(<\text{flag1} := R11 \sigma>,, \text{after1} := \text{False})$
\]

\[\begin{align*}
\text{True}
\end{align*}\]

\text{COEND}
\[\begin{align*}
\text{True}
\end{align*}\]

\text{Fig. 10.} Proof outline for Peterson’s algorithm under C11. The second thread (not shown here) is symmetric.

Although automatic, repeated applications of \text{sledgehammer} to discharge so many proof obligations is rather tedious. However, one can quickly discover common patterns in the proof steps allowing these proof obligations to be discharged via a few simple applications of \text{apply}-style proofs.

6 Related Work

As has been mentioned, the current paper builds on ideas found in \cite{11}. That paper did not develop a program logic based on Hoare triples, and was limited to invariance style proofs. Both \cite{11} and the current paper use the same definite value assertion, but the current paper employs a much richer and more powerful assertion language. In particular, the conditional value assertion is critical for enabling an Owicky-Gries based program logic. Finally, \cite{11} does not consider mechanisation or automation.

Of course, a great deal of work has been put into the development of separation logics for C11-style weak memory models \cite{12,14,19,37,38}. One of the most recent and perhaps most fundamental of these is the Iris framework \cite{19}. This framework has been formalised in the Coq proof assistant, and instantiations of it support a large fragment of C11. This fragment contains C11’s \text{nonatomic accesses} but not relaxed accesses and is therefore incomparable to our own. In particular, nonatomic access cannot legally race, whereas relaxed accesses are designed to enable
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More generally, separation logics can become complicated when applied to weak-memory, and we are partly motivated by the desire to build verification frameworks atop simple and natural relational models (other authors [25] have made similar observations).

There have been a number of recent attempts to develop mechanised deductive verification support for weak memory. Summers and Müller [34] present an approach to automating deductive verification for weak memory programs by encoding Relaxed Separation Logic [38] and Fenced Separation Logic [12, 14] into Viper [27]. Their work builds on separation logic, whereas ours builds on a relational framework. Apart from this fundamental difference, Summers and Müller encode the concurrent logics into the Viper sequential specification framework, which provides a high level of automation. On the other hand, and as the authors themselves note, encoding the logic in a foundational verification tool such as Isabelle provides a higher level of assurance about correctness. In particular, the entire development of our framework is verified in Isabelle, down to the operational semantics.

Another technique based on Owicki-Gries is that of [25], which defines a proof system for the release-acquire fragment of C11, a smaller fragment than the release-acquire-relaxed fragment that we treat in this paper. It is unclear how difficult it would be to extend [25] to deal with relaxed accesses. In any case, [25] does not deal with mechanisation or automation.

Alglave and Cousot have developed another extension to the Owicki-Gries method for weak memory models [2]. Because their method, like ours, is an extension of the Owicki-Gries method, their verification method first requires a proof outline. One novelty of their approach is that their method requires a communication specification (or CS), which involves specifying for each read operation in the program, which writes the variable can read from (which may be in another thread). Verifying that the proof outline and CS are together valid, and therefore that assertions of the proof outline do in fact hold for the program, involves two proof obligations. The first is to show that the proof outline is valid in our standard sense (so that it is locally correct and noninterfering), under the assumption that the CS is satisfied. The second obligation is that a given memory model satisfies the CS. This second obligation constitutes an additional proof effort, not required in our method. The advantage they gain is that once a proof outline is known to be locally correct and noninterfering under a given CS, then the algorithm is known to be correct under any memory model that satisfies the CS.

The operational semantics in the current paper is inspired by the semantics described in [19, 31]. The current paper is based on semantics and assertions found in [9], which also presents case-study verifications mechanised in Isabelle. The mechanisation in that paper is rudimentary. Programs are not represented in a while-style language as in the current paper. Instead, they use a program-counter based representation, where control flow must be explicitly modelled. As a consequence, proof obligations are not decomposed in the conventional Owicki-Gries style. Rather, the verifier must prove stability of a large global invariant mapping program counter locations to the assertions that hold at that location. Furthermore, there is little real automation, either in generating or discharging proof obligations. The current paper presents a highly-structured and mechanised Owicki-Gries framework supporting a high level of automation.

Dan et al. [10] introduce an abstraction for the store buffers of the weak memory model which reduces the workload on program analysers. They provide a source-to-source transformation that realises the abstraction producing a program that can be analysed with verifiers for sequential consistency. The approach is integrated with CONCURINTERPROC [18] and uses the Z3 theorem prover. Model checking has also been targeted for weak memory, e.g., by explicitly encoding architectural structures leading to weak behaviour, like store buffers [3, 30]. Ponce de León et al. [16, 32] have
developed a bounded model checker for weak memory models, taking the axiomatic description of a memory model as input. (Bounded) model checkers for specific weak memory models are furthermore the tools CBMC [4] (for TSO), NIDHUGG [1] (for TSO and PSO), RCMC [21] (for C11) and GENMC [22]. Others [8] present an approach for modelling and verifying C11 programs using Event-B and ProB model checker.

7 Conclusion

In this paper, we have introduced an extension to a twenty-year old formalisation of Owicki-Gries proof calculus in Isabelle [28] in order to tackle the verification problem of C11 programs under weak memory. We start by developing the necessary language support for defining C11 programs and have shown that existing operational semantics for the RC11-RAR fragment [11] can be encoded in a straightforward manner, which provides an example instantiation. We have provided a set of proof rules to facilitate verification of C11 programs, and exemplified our approach by verifying a number of example programs.

Our entire development has been carried out in the Isabelle theorem prover and is modular with respect to the underlying memory model. For the RC11-RAR fragment we consider, we have shown that the proofs are highly automated. As described in Section 5.5, a simple pattern of applying an Owicki-Gries specific proof method, and then invoking SMT solvers via Isabelle’s sledgehammer tool was sufficient for verifying every proof outline. Moreover, the use of Isabelle means that we have flexibility in the specific operational semantics that we use.

References

1. Abdulla, P.A., Aronis, S., Atig, M.F., Jonsson, B., Leonardsson, C., Sagonas, K.: Stateless model checking for TSO and PSO. Acta Inf. 54(8), 789–818 (2017)
2. Alglave, J., Cousot, P.: Ogre and Pythia: an invariance proof method for weak consistency models. In: Castagna, G., Gordon, A.D. (eds.) POPL. pp. 3–18. ACM (2017)
3. Alglave, J., Kroening, D., Nimal, V., Tautschnig, M.: Software verification for weak memory via program transformation. In: Felleisen, M., Gardner, P. (eds.) ESOP. LNCS, vol. 7792, pp. 512–532. Springer (2013)
4. Alglave, J., Kroening, D., Tautschnig, M.: Partial orders for efficient bounded model checking of concurrent software. In: Sharygina, N., Veith, H. (eds.) CAV. LNCS, vol. 8044, pp. 141–157. Springer (2013)
5. Apt, K.R., de Boer, F.S., Olderog, E.: Verification of Sequential and Concurrent Programs. Texts in Computer Science, Springer (2009)
6. Batty, M., Owens, S., Sarkar, S., Sewell, P., Weber, T.: Mathematizing C++ concurrency. In: Ball, T., Sagiv, M. (eds.) POPL. pp. 55–66. ACM (2011)
7. Böhme, S., Nipkow, T.: Sledgehammer: Judgement day. In: IJCAR. Lecture Notes in Computer Science, vol. 6173, pp. 107–121. Springer (2010)
8. Dalvandi, M., Dongol, B.: Towards deductive verification of C11 programs with Event-B and ProB. In: Proceedings of the 21st Workshop on Formal Techniques for Java-like Programs. p. 4. ACM (2019)
9. Dalvandi, S., Doherty, S., Dongol, B., Wehrheim, H.: Owicki-Gries reasoning for C11 RAR. In: ECOOP (2020), (To appear)
10. Dan, A., Meshman, Y., Vechev, M., Yahav, E.: Effective abstractions for verification under relaxed memory models. Computer Languages, Systems & Structures 47, 62–76 (2017)
11. Doherty, S., Dongol, B., Wehrheim, H., Derrick, J.: Verifying C11 programs operationally. In: Hollingsworth, J.K., Keidar, I. (eds.) PPoPP. pp. 355–365. ACM (2019)
12. Doko, M., Vafeiadis, V.: A program logic for C11 memory fences. In: VMCAI. LNCS, vol. 9583, pp. 413–430. Springer (2016)
13. Doko, M., Vafeiadis, V.: Tackling real-life relaxed concurrency with FSL++. In: ESOP. pp. 448–475 (2017)
14. Doko, M., Vafeiadis, V.: Tackling real-life relaxed concurrency with fsl++. In: European Symposium on Programming. pp. 448–475. Springer (2017)
15. Dolan, S., Sivaramakrishnan, K., Madhavapeddy, A.: Bounding data races in space and time. In: PLDI. pp. 242–255. PLDI 2018, ACM, New York, NY, USA (2018)
16. Gavrilenko, N., Ponce de León, H., Furbach, F., Heljanko, K., Meyer, R.: BMC for weak memory models: Relation analysis for compact SMT encodings. In: Dillig, I., Tasiran, S. (eds.) CAV. LNCS, vol. 11561, pp. 355–365. Springer (2019). https://doi.org/10.1007/978-3-030-25540-4_19
17. Hoare, C.A.R.: An axiomatic basis for computer programming. Commun. ACM 12(10), 576–580 (1969)
18. Jeannet, B.: Relational interprocedural verification of concurrent programs. Software & Systems Modeling 12(2), 285–306 (2013)
19. Kaiser, J., Dang, H., Dreyer, D., Lahav, O., Vafeiadis, V.: Strong logic for weak memory: Reasoning about release-acquire consistency in Iris. In: Müller, P. (ed.) ECOOP. LIPIcs, vol. 74, pp. 17:1–17:29. Schloss Dagstuhl - Leibniz-Zentrum fuer Informatik (2017)
20. Kang, J., Hur, C., Lahav, O., Vafeiadis, V., Dreyer, D.: A promising semantics for relaxed-memory concurrency. In: POPL. pp. 175–189. ACM (2017)
21. Kokologiannakis, M., Lahav, O., Sagonas, K., Vafeiadis, V.: Effective stateless model checking for C/C++ concurrency. PACMPL 2(POPL), 17:1–17:32 (2018)
22. Kokologiannakis, M., Raad, A., Vafeiadis, V.: Model checking for weakly consistent libraries. In: McKinley, K.S., Fisher, K. (eds.) PLDI. pp. 96–110. ACM (2019)
23. Lahav, O., Vafeiadis, V., Kang, J., Hur, C., Dreyer, D.: Repairing sequential consistency in C/C++11. In: PLDI. pp. 618–632. ACM (2017)
24. Lahav, O.: Verification under causally consistent shared memory. SIGLOG News 6(2), 43–56 (2019)
25. Lahav, O., Vafeiadis, V.: Owicki-Gries reasoning for weak memory models. In: Halldórsson, M.M., Iwama, K., Kobayashi, N., Speckmann, B. (eds.) ICALP. LNCS, vol. 9135, pp. 311–323. Springer (2015)
26. Lamport, L.: How to make a multiprocessor computer that correctly executes multiprocess programs. IEEE Trans. Computers 28(9), 690–691 (1979)
27. Müller, P., Schwerhoff, M., Summers, A.J.: Viper: A verification infrastructure for permission-based reasoning. In: International Conference on Verification, Model Checking, and Abstract Interpretation. pp. 41–62. Springer (2016)
28. Nipkow, T., Nieto, L.P.: Owicki-Gries in Isabelle/HOL. In: FASE. Lecture Notes in Computer Science, vol. 1577, pp. 188–203. Springer (1999)
29. Owicki, S.S., Gries, D.: An axiomatic proof technique for parallel programs I. Acta Inf. 6, 319–340 (1976)
30. Paulson, L.C.: Isabelle - A Generic Theorem Prover (with a contribution by T. Nipkow). LNCS, vol. 828. Springer (1994)
31. Podkopaev, A., Sergey, I., Nanevski, A.: Operational aspects of C/C++ concurrency. CoRR abs/1606.01400 (2016)
32. Ponce de León, H., Furbach, F., Heljanko, K., Meyer, R.: BMC with memory models as modules. In: Bjørner, N., Gurfinkel, A. (eds.) FMCAD. pp. 1–9. IEEE (2018)
33. de Roever, W.P., de Boer, F.S., Hannemann, U., Hooman, J., Lakhnech, Y., Poel, M., Zwiers, J.: Concurrency Verification: Introduction to Compositional and Noncompositional Methods, Cambridge Tracts in Theoretical Computer Science, vol. 54. Cambridge University Press (2001)
34. Summers, A.J., Müller, P.: Automating deductive verification for weak-memory programs. In: Beyer, D., Huisman, M. (eds.) TACAS. LNCS, vol. 10805, pp. 190–209. Springer (2018)
35. Svendsen, K., Pichon-Pharabod, J., Doko, M., Lahav, O., Vafeiadis, V.: A separation logic for a promising semantics. In: Ahmed, A. (ed.) ESOP. LNCS, vol. 10801, pp. 357–384. Springer (2018)
36. Travkin, O., Mütze, A., Wehrheim, H.: SPIN as a linearizability checker under weak memory models. In: Bertacco, V., Legay, A. (eds.) HVC. LNCS, vol. 8244, pp. 311–326. Springer (2013)
37. Turon, A., Vafeiadis, V., Dreyer, D.: GPS: navigating weak memory with ghosts, protocols, and separation. In: Black, A.P., Millstein, T.D. (eds.) OOPSLA. pp. 691–707. ACM (2014)
38. Vafeiadis, V., Narayan, C.: Relaxed separation logic: A program logic for c11 concurrency. In: Proceedings of the 2013 ACM SIGPLAN international conference on Object oriented programming systems languages & applications. pp. 867–884 (2013)
39. Williams, A. https://www.justsoftwaresolutions.co.uk/threading/petersons_lock_with_C++0x_atomics.html (2018), accessed: 2018-06-20
A Appendix

We present proofs of two additional variations of the RRC litmus test. Fig. 11 presents a simple two-threaded version with a writer thread that enforces a order of writes in program order and a reader thread that reads from these writes. The proof shows that the order of reads in the reader is consistent with the order of writes in the writer.

Fig. 11. Isabelle encoding of the read-read coherence litmus test with two threads.

\begin{verbatim}
consts
x :: L

record mp_state =
a :: V
b :: V
σ :: Cstate

\|-
\{ \aptive a = 0 \land b = 0 \}

COBEGIN
\{ \aptive [x = 1 \, \sigma] \land [0,1] \, \sigma \land [1,1] \, \sigma \land [0,2] \, \sigma \land [1,1] \, \sigma \}
\< x := 1 \ \sigma >;;
\{ \aptive [x = 1 \, \sigma] \land [x \enc 1 \, 1] \, \sigma \land [0,2] \, \sigma \land [1,1] \, \sigma \land [1,2] \, \sigma \}
\< x := 2 \ \sigma >
\{ \aptive [1,1] \, \sigma \land [1,2] \, \sigma \land [1 \, \prec \, x \, 2] \, \sigma \}
\| |
\{ \aptive [1,1] \, \sigma \land [1,2] \, \sigma \}
\< \aptive a \leftarrow 2 \, x \, \sigma > ;;
\{ \aptive [x \enc 2 \, a] \, \sigma \}
\< \aptive b \leftarrow 2 \, x \, \sigma >
\{ \aptive (a \neq b \rightarrow [a \prec x \, b] \, \sigma) \}
\| |
\| |
\< \aptive \bar{a} = 2 \rightarrow \aptive \bar{b} \neq 1 >
\| |
\end{verbatim}

Fig. 12 presents the standard four-threaded version in which the two writes to \(x\) occur in two different threads. There are two reader threads both of which read from \(x\) twice. One must prove that the order of writes read by both threads are consistent. In particular, if \(a\) is set to 1 and \(b\) to 2, then thread 3 must have seen the writes to \(x\) in that order. It should therefore not be possible for thread 3 to read 1 for \(x\) if it has already seen the value 2 in the first read at line 29.
\texttt{consts x :: L}
\texttt{record rrc4\_state = a :: V b :: V c :: V d :: V \sigma :: Cstate COBEGIN }
\texttt{||\{- [x = 1 \text{0}] \; \sigma \land [x = 2 \text{0}] \; \sigma \land [x = 3 \text{0}] \; \sigma \land [x = 4 \text{0}] \; \sigma \}\}}
\texttt{<x := 1 \; \sigma> \;}}
\texttt{|| \{- [0,1] \; \sigma \land [1,1] \; \sigma \}\}}
\texttt{<x := 2 \; \sigma> \;}}
\texttt{|| \{- True \}\}}
\texttt{<a ← 3 \; x\; \sigma> ;;}
\texttt{\{- [x = 3 \text{0}] \; \sigma \land [1,2] \; \sigma \land (a = 1 \rightarrow [1, a] \; \sigma) \}\}}
\texttt{<b ← 3 \; x\; \sigma>}
\texttt{\{- (a \neq b \rightarrow [a < x \; b] \; \sigma) \land (a = 1 \rightarrow [1, a] \; \sigma) \land (b = 2 \rightarrow [1, b] \; \sigma)\}\}}
\texttt{|| \{- True \}\}}
\texttt{<c ← 4 \; x\; \sigma> ;;}
\texttt{\{- [x = 4 \text{0}] \; \sigma \land (c = 2 \rightarrow [1, c] \; \sigma)\}\}}
\texttt{<d ← 4 \; x\; \sigma>}
\texttt{\{- (c \neq d \rightarrow [c < x \; d] \; \sigma) \land (c = 2 \rightarrow [1, c] \; \sigma) \land (d = 1 \rightarrow [1, d] \; \sigma)\}\}}
\texttt{COEND}
\texttt{\{- \sigma = 1 \land \sigma = 2 \land \sigma = 2 \rightarrow \sigma \neq 1 \}\}}

\textbf{Fig. 12.} Isabelle encoding of the read-read coherence litmus test with four threads.