Short circuit detection and driving control with no blanking time for high voltage high power insulated gate bipolar transistors

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Abstract
Insulated gate bipolar transistors (IGBT) short-circuit (SC) protection is one of the most important protection methods for IGBT converter equipment. The fast detection and protection response time could reduce the permanent damage of devices, and extend their use life cycle. At present, the collector emitter voltage \( v_{\text{ce}} \) desaturation method is widely used in the commercial IGBT drive circuit, which has blanking time of fault detection and protection. In this paper, an improved adaptive \( v_{\text{ce}} \) SC detection and protection is proposed to realize the blanking time adjustment under different SC conditions. By the determination of the \( \frac{di}{dt} \) characteristics of the current variation on the parasitic inductance between the power emitter and the Kelvin emitter of IGBT modules, the execution time of the two detection methods can be set. According to the switch process and the SC type, the corresponding logic processing will be carried out to realize the fast detection of different SC conditions. The circuit scheme without blanking time detection and protection is designed, and the circuit is modelled and simulated by Pspice. The IGBT driving circuit SC test without blanking time detection and soft turn-off protection has been carried out. Simulation and test results can verify the feasibility of the proposed circuit.

1 | INTRODUCTION

Insulated gate bipolar transistors (IGBTs) used in many high power industrial applications need to be protected from over-current and short-circuit failures under external fault conditions. Such faults mostly result from the occurrence of an abrupt variation or short circuit at the load end. To improve the reliability of IGBTs, there are multiple protection approaches designed in modern power electronics systems, including over-voltage, over-current and over-temperature protection. In particular, short-circuit protection is the most important among the existing protection technologies. Especially, IGBTs could withstand the short-circuit condition in less than 10 \( \mu s \). Shortening the short-circuit detection and protection time can reduce the short-circuit fault’s damage, and prolong the useful life of the IGBTs. The electrical parameters such as the gate voltage \( v_{\text{ge}} \), the collector voltage \( v_{\text{ce}} \) and the collector current \( i_c \) will change significantly under the short-circuit failures. In this way, various approaches have been proposed and studied to protect IGBTs [1]. For example, in [2] the authors use a printed circuit board (PCB) Rogowski coil to detect short circuits. In [3], the current sensing IGBT is used with a sense resistor, and the protection circuit detects the voltage drop of the resistor to measure the main IGBT current and protects the IGBTs from short-circuit faults. In [4] and [5], the technique using the induced voltage across the stray inductance between the Kelvin emitter (E) and power emitter (PE) terminal responds fast without taking various short-circuit faults into account. Due to the Miller effect, the waveforms of gate voltage under the normal and fault conditions are different. Thus, a fault-detection circuit using the IGBT gate-voltage pattern at turn-on transient has been proposed in [6–8]. Zeng et al. [9] proposed a global and real-time control with embedded hardware artificial neural network for imbalance current suppression. Wuest et al. [10] realized the turn-off delay control through parameter condition monitoring. Wang et al. [11] proposed a self-adaptive active gate driver to further optimize IGBT switching performance. Guo et al. [12] proposed a three-level gate driving method to increase IGBT’s damping to suppress the inrush current and improve the inrush energy loss distribution. The de-saturation technique...
detects the collector voltage $r_{ce}$ under short-circuit faults, which is widely used in modern gate drivers [13, 14]. Chen et al. [15] proposed an improved IGBT short-circuit protection method with self-adaptive blanking circuit based on $r_{ce}$ measurement, by feeding back the required minimum blanking time interval, which is decided by comparing $r_{ce}$ with the de-saturation reference voltage. The short-circuit faults are detected by combination of $dV/dt$ detection and $r_{ce}$ detection, which ensures the rapid and right responses [16]. Silicon-carbide (SiC) MOSFET modules exhibit narrow short-circuit withstand times and generally much lower short-circuit robustness than silicon (Si) IGBTs. Therefore, fast-and-reliable detection mechanisms are absolute necessities for SiC MOSFET modules. There are some improved detection methods for high-voltage high-power MOSFET in [17–19].

Considering the shortcomings of existing short-circuit detection methods, a short-circuit detection method without blanking time is presented in this paper to reduce short-circuit protection delay time and make the detection circuit suitable for different types of IGBT modules. It is based on the idea of using a combination of self-adaptive $r_{ce}$ detection and $dV/dt$ detection. The elimination of the blanking time is realized by using a complex programmable logic device (CPLD) to make logical judgement under different operation conditions. This paper is organized as follows: Section II introduces the state of arts of IGBT short-circuit faults detection. Section III analyses the short-circuit faults detection circuit without blanking time in detail. Section IV provides the simulation and experimental results, and the conclusions are given in Section V.

2 | IGBT SHORT-CIRCUIT BEHAVIOUR AND DETECTION

The short-circuit characteristics of IGBTs reflect the ability to withstand fault current, including the magnitude and duration of short-circuit current. However, the short-circuit characteristics and robustness of different types of IGBT modules are uncertain under different short-circuit fault conditions. Therefore, it is necessary to adopt corresponding detection methods for different short-circuit faults [20].

2.1 | Analysis of the short-circuit faults

The IGBTs’ short-circuit characteristics are affected by the gate voltage $r_{ge}$, the DC bus voltage $V_{DC}$, the operating junction temperature $T_J$ and the structure technology. Due to the transconductance effect, the collector current $I_c$ depends on the gate voltage $r_{ge}$. When the short-circuit fault occurs, the higher the gate voltage, the larger the short-circuit current. And the bus voltage $V_{DC}$ has obvious effects on the short-circuit characteristics, which directly determines the peak voltage overshoot during turn-off transition. The general IGBT short-circuit safe operation area (SCSOA) is obtained by manufacturers through the fixed bus voltage experiment. The voltage is generally 0.6–0.8 times the rated collector-emitter voltage. The operating junction temperature $T_J$ also has an impact on the short-circuit characteristics. $T_J$ is usually lower than the maximum junction temperature $T_J$ in datasheet under normal conditions. The short-circuit current and the short-circuit duration decrease with the increase of the junction temperature $T_J$ when the gate voltage $r_{ge}$ and $V_{DC}$ can be controlled to a certain value. Moreover, $T_J$ rises rapidly under the short-circuit fault because of the high short-circuit energy loss. And the IGBT self-heating effect would also impose strong impacts on the IGBT’s short-circuit characteristics [21]. In addition, the structure design and processing technique also determine the short-circuit characteristics. MOS channel in IGBT structure affects turn-off loss $E_{off}$ and on-state voltage drop $V_{CE(sat)}$. The wider the MOS channel, the larger the $E_{off}$ and the lower the $V_{CE(sat)}$. The device with a wide MOS channel will withstand the high short-circuit current, which requires the fast fault detection and protection time.

IGBT short-circuit modes can be classified into two scenarios according to fault conditions [22]. Short-circuit I (hard switching fault, HSF) is a direct turn-on of the IGBT under short-circuit conditions. And short-circuit II (fault under load, FUL) is the occurrence of short circuit during the on-state of the IGBT, which is a peak power-wise condition harder than that of HSF. Furthermore, in all typical IGBT applications, there are anti-parallel diodes in the IGBT modules. If a short-circuit fault occurs at the freewheeling diode, the normal operation of the IGBT will be affected. Thus, the occurrence of a short-circuit fault across the loading during the conducting mode of the freewheeling diode is denoted as short-circuit III (fault under freewheeling, FUF) [23].

As shown in Figure 1, the IGBT dynamic test circuit could be used to test the short-circuit characteristics of the bottom tube $T_{DUT}$ in half-bridge circuit. For either HSF or FUL, the short-circuit loop contains only circuit parasitic inductors and excludes the huge load inductor. Thus the copper bars or cables are usually used to replace the load inductance to simulate the HSF or FUL in the experiments.
Typical HSF waveforms are given in Figure 2(a). In this mode, the IGBT is off and the bus voltage $V_{DC}$ is supported across the device during the prefault stage. The rate at which the device begins to conduct current is related to the charging rate of the Miller capacitance $C_{gc}$. And $dv_{ce}/dt$ and $C_{gc}$ are much lower at higher voltage. So the displacement current $i_{gc}$ through $C_{gc}$ is small and hardly causes a change to $v_{ge}$. When the device is gated on, $v_{ge}$ reaches gate-threshold voltage $V_{ge(th)}$ and $i_{c}$ begins to rise very quickly. And short-circuit current depends on the applied $v_{ce}$ and turn-on gate resistor. A notch is gouged out of $v_{ce}$ due to the voltage drops occurring across the parasitic inductance of the circuit.

The device might be subjected to a short-circuit fault in normal conduction. The waveforms in Figure 2(b) illustrate FUL. Initially the IGBT is operating normally, carrying a stable load current within its ratings. And $v_{ce}$ falls to a low voltage drop, which is generally 2–4 V. During FUL, $i_{c}$ rapidly rises up to its saturation level which depends on the gate-drive voltage, pulling the IGBT out of its saturation state. As $v_{ce}$ is increasing to $V_{DC}$ during the short-circuit, the high $dv_{ce}/dt$ can induce $i_{gc}$ through $C_{gc}$. And the Miller effect has much more influence on FUL, particularly because $C_{gc}$ is very high at a low voltage. Hence, $v_{ge}$ sets higher and could cause an increase in the short-circuit current magnitude. In short, FUL could result in much higher fault current than HSF.

The waveforms of FUF is shown in Figure 2(c). FUF is the occurrence of short circuit across the load during the conducting mode of the freewheeling diode. Before the short-circuit, the IGBT is already turned on and its current is zero. At the same time, the inverse diode is conducting. If now the short circuit occurs at the load, the current is rapidly commutated from the diode to the IGBT, and the IGBT is passively turned into the short-circuit condition. Meanwhile, $v_{ce}$ increases to $V_{DC}$ while the IGBT transits to its de-saturation mode. The subsequent process is similar to the one seen in FUL. A dynamic short-circuit peak current occurs because of an increase of $v_{ge}$. When the short-circuit current falls to the fixed value, $di_{c}/dt$ affects the $v_{ce}$ peak value $V_{peak}$. Since the drop rate of the short-circuit cannot be controlled by $v_{ge}$, the $V_{peak}$ is higher than the one during the soft turn-off process.

FUL is more severe than HSF in practical applications due to the higher short-circuit current magnitude. Besides, HSF and FUL usually occur in the inverter circuits. FUF often occurs during the conducting mode of the freewheeling diode, such as the traction converters where the motor is used as generator.

### 2.2 Short-circuit fault detection methods

Many schemes have been discussed over the last few years for detecting the IGBT’s short-circuit fault conditions. According to the sampling signal from the IGBT module, existing detection methods can be divided into four types—the collector (PE) and Kelvin emitter (E) terminals, which is generally less than 10 nH. In the case of constant $L_{PE-E}$ under switching operation, $di/dt$ can be extracted by the induced voltage $v_{PE-E}$ across $L_{PE-E}$. Note that during the short-circuit period, $i_{c}$ rises very quickly so that $di/dt$ can be used as a short-circuit indicator.

As a result, $v_{PE-E}$ induced by the short-circuit event can be contrasted with normal $v_{PE-E}$ for fault detection, which is shown in Equation (1).

$$v_{PE-E} = -L_{PE-E} \times \frac{di}{dt}$$  \hspace{1cm} (1)
The di/dt detection has fast response time. But it does not take various short-circuit faults into account. Compared with FUL and FUF, the method is more effective for HSF because the di/dt change is much higher in that case.

Many commercial drivers with integrated \( r_{ce} \) detection have a measuring circuit to detect the short-circuit fault. When the IGBT is turned on normally, \( r_{ce} \) will fall to a low voltage drop from \( V_{DC} \), and \( i_c \) will rise to the load current level. Once the short-circuit fault occurs, the IGBT will exit the saturation state according to the output characteristic curves and \( r_{ce} \) will increase up to \( V_{DC} \). So it can be used to indirectly detect the short-circuit fault based on the change of \( r_{ce} \). As shown in Figure 4, the \( r_{ce} \) detection approach can be divided into two types: active detection and passive detection.

The active detection method implemented with a series of high voltage diodes \( D_1 \) is plotted in Figure 4(a). When the IGBT is normally turned on, a current generated by the power supply \( V_{CC} \) flows to the IGBT collector through the limiting resistors \( R_1 \) and \( R_2 \). Thus, the \( r_{ce} \) detection voltage \( r_A \) can be expressed by

\[
r_A = \frac{(V_{CC} - V_F - V_{CE(sat)}) \times R_1}{R_1 + R_2} + V_F + V_{CE(sat)} \tag{2}
\]

where: \( V_F \) is the total forward voltage drop of the high voltage diodes; \( V_{CE(sat)} \) is the collector-emitter saturation voltage drop.

On condition that \( R_1 \) is much smaller than \( R_2 \), Equation (2) can be simplified as follows

\[
r_A \approx V_F + V_{CE(sat)} \tag{3}
\]

During the on-state operation, \( r_A \) is lower than the desaturation reference voltage \( V_{REF} \), and the comparator outputs the low level signal. When short-circuit fault happens, the \( r_{ce} \) would increase quickly. And the high voltage diodes are reversely cut off, and then the capacitor \( C_1 \) is charged by \( V_{CC} \) across \( R_2 \). Finally, the measured \( r_A \) is charged to the value of \( V_{CC} \). Because \( V_{CC} \) is higher than \( V_{REF} \), the comparator outputs the high level fault signal. The gate driver would perform the soft turn-off protection.

As plotted in Figure 4(b), working principle of the passive detection circuit is similar to that of the active detection circuit, which consists of a series of resistors \( R_1 \) and \( R_2 \). When \( r_{ce} \) is \( V_{DC} \), the current \( i_{R1} \) flowing through \( R_1 \) is controlled at 0.6–0.8 mA, and \( r_A \) must be lower than \( V_{CC} \) in the situation. The capacitor \( C_1 \) and resistor \( R_2 \) are used to set the blanking time. The diodes \( D_1 \) and \( D_2 \) form the voltage clamping circuit. \( R_1 \) and \( R_2 \) can be designed by

\[
\begin{align*}
\frac{i_{R1}}{V_{DC}} &= \frac{1}{R_1 + R_2} \\
0.6 \times 10^{-3} &\leq i_{R1} \leq 0.8 \times 10^{-3} \\
\frac{V_{CE(sat)} + R_2}{R_1 + R_2} &\leq V_{CC} \\
\end{align*}
\tag{4}
\]

The \( r_{ce} \) detection is not enabled until \( r_{ce} \) falls to the saturation voltage drop. Thus, the method can only detect the de-saturation phenomenon of the IGBT, and cannot correctly judge the repeated changes of \( r_{ce} \). Therefore, the prerequisite for enabling the \( r_{ce} \) detection method is to ensure that the IGBT is already in the on state. Figure 5 shows the waveforms of \( r_{ce} \), \( i_c \) and \( v_{ge} \).

In order to properly protect the IGBT modules under short-circuit fault condition, certain time must be reserved to ensure that the IGBT is turned on normally. During the period, \( r_{ce} \) detection circuit is disabled, which is denoted as blanking time. The blanking time \( t_{blk} \) should cover the control signal delay time \( t_{d(on)} \) and the turn-on delay time \( t_r \). For the passive detection
method, the designed blanking time can be calculated by

$$t_{blc} = R_3 \times C_1 \times \ln \left( \frac{V_{CC} - V_{R1}}{V_{CC} - V_{REF}} \right)$$

(5)

During HSF, the $v_{ce}$ detection can only detect the fault condition after the blanking time, which will put the IGBT and human at risk.

3.1 ANALYSIS OF SHORT-CIRCUIT DETECTION AND PROTECTION WITHOUT BLANKING TIME

Based on the aforementioned analysis, the short-circuit detection scheme without blanking time (NBTD) consists of $v_{ce}$ detection method and $di/dt$ detection method with the logic control strategy. As shown in Figure 6, the principle of the proposed detection method is as follows: before normal turn-on, the detection circuit is disabled. Once the IGBT is turned on, the $di/dt$ detection is enabled immediately. And the $v_{ce}$ detection is disabled because $v_{ce}$ is higher than the $V_{CE(sat)}$. If HSF occurs during the turn-on transient, the gate driver detects the fault by the $di/dt$ detection circuit and takes the protection measures directly. And the $v_{ce}$ detection does not work in this condition. Otherwise, the $v_{ce}$ detection circuit is not enabled until the IGBT works normally in saturation state. Based on the above analysis, it is ensured that there is no blanking time in the whole operating process of the IGBT.

The waveforms of the proposed detection method are plotted in Figure 7 during the normal condition and short-circuit faults. The detailed working process is explained as follows.

During the off-period ($T_0-T_1$), the IGBT is off because $v_{ge}$ is lower than the gate-threshold voltage $V_{ge(th)}$. And $v_{ce}$ is always equal to $V_{DC}$. When $v_{ge}$ reaches $V_{ge(th)}$ at time $T_1$, $v_{ce}$ starts to fall to $V_{CE(sat)}$ from $V_{DC}$. In the Miller plateau ($T_2-T_3$), $v_{ce}$ decreases more quickly. In the stage ($T_3-T_4$), $v_{ce}$ is lower than the $v_{ce}$ detection enable-threshold $V_{REF2}$. Finally, $v_{ce}$ is equal to $V_{CE(sat)}$. During the turn-on period ($T_1-T_3$), $v_{ce}$ is higher than $V_{REF2}$, the comparator unit (5) outputs the low-level signal. At the same time, the output signal of the power amplifier unit (2) changes from low level to high level, and the inversion unit (6) outputs the low-level signal. Then, the output of the trigger unit (7) remains at the low level. Therefore, the output of the AND gate unit (9) is low-level, and $v_{ce}$ detection is disabled at this time.

If the HSF occurs before time $T_1$, the collector current $i_C$ rapidly increases, whose rate could reach several kA/µs. As shown in (1), the induced voltage $v_{PE-E}$ across the parasitic inductor $L_{PE-E}$ is a negative voltage, which is related to the rate of $i_C$. In this condition, $di/dt$ detection unit (3) outputs the high-level signal. Because the output signal of the power amplifier unit (2) $V_{out}$ is high-level, the AND gate unit (4) and OR gate unit (10) both output the high-level signal. The R-pin input signal of the trigger unit (11) is low-level. According to the preset logic, the trigger unit (11) outputs the high-level fault signal, so that the control generator unit (1) will block the control pulse signal and control the reducing-$v_{ge}$ and-soft-turn-off unit (12) to take short-circuit protection action.

If there is no short-circuit fault during the period ($T_0-T_3$), then $v_{ce}$ is lower than $V_{REF2}$. And the output signal of the
comparator unit (5) changes from low level to high level. At
the moment, the power amplifier unit (2) outputs the high-level
signal, and thus the inversion unit (6) outputs the low-level
signal. Based on the preset logic, the output of the trigger unit
(7) changes to low level. Therefore, the output signal of the
AND gate unit (9) is consistent with that of the comparator
unit (5), and $v_{ce}$ detection is enabled at this time. After time $T_4$, the IGBT enters the saturation area.

If FUL occurs under the on-state condition, $i_c$ rapidly
increases, pulling the IGBT out of its saturation state. And $v_{ce}$
starts to rise up to $V_{DC}$ quickly. Because the $v_{ce}$ detection fault-threshold $V_{REF3}$ is higher than $V_{REF2}$, the output signal of the comparator unit (5) changes from low level to high level once $v_{ce}$ is higher than $V_{REF3}$. And the output signal of the trigger unit (7) remains at the high level. The output signal of the AND gate unit (9) is high-level, which is consistent with that of the comparator unit (8). Thus, the OR gate unit (10) outputs the high-level signal. And the R-pin input signal of the trigger unit (11) is low-level. On the basis of the preset logic, the trigger
unit (11) outputs the high-level fault signal, so that the control
generator unit (1) will block the control pulse signal and control
the reducing-$r_{gc}$ and-soft-turn-off unit (12) to take short-circuit
protection action.

4 | SIMULATION AND EXPERIMENTAL RESULTS

4.1 | Simulation results

In order to verify the feasibility of the proposed detection
circuit, simulation using Pspice is performed. Figure 8 shows

![Simulated circuit of short-circuit detection without blanking time](image)

**Figure 8**

The simulation circuit. The parameters used for simulation are shown in Table 1.

As mentioned in Section II, short-circuit faults of IGBTs can be classified in two scenarios: HSF and FUL. According to the characteristics, the parasitic inductance in the HSF mode is a little smaller than the one in the FUL mode. Thus, Switch $S_1$ is closed to simulate HSF before the IGBT is turned on, where $L_{str2}$ is 30 nH. Similarly, $S_1$ is closed to simulate FUL when the IGBT is in the on state, where $L_{str2}$ changes to 5 µH.

Figure 9 shows the simulation waveforms under the HSF condition. In Figure 9(a), when $r_{gs}$ reaches the gate-threshold voltage, $i_c$ begins to rise rapidly and finally to the short-circuit current. And there is a notch in the $v_{ce}$ waveform. Figure 9(b) shows the fault detection logic simulation waveforms. When the IGBT is turned on, the increase of $i_c$ produces the inductive voltage $v_{PE-E}$ on $L_{PE-E}$. When $r_{PE-E}$ is lower than $V_{REF1}$ ($=-7.5$ V), the comparator output-signal out_1 changes to low level. And the $di/dt$ detection-signal error_di/dt is high-level, so that the fault detection-signal error_sc changes to high level.

| Table 1 Parameters for simulation |
| Parameter | Symbol | Value |
|---|---|---|
| Bus voltage | $V_{DC}$ | 1500 V |
| Load inductance | $L_{load}$ | 100 µH |
| Parasitic inductance of the power loop | $L_{str1}$ | 30 nH |
| Stray inductance between the Kelvin emitter and power emitter | $L_{PE-E}$ | 5 nH |
| Parasitic inductance under short-circuit fault | $L_{str2}$ | 30 nH/5 µH |
used to warn HSF. Because $v_{ce}$ does not drop to $V_{CE(sat)}$, the $v_{ce}$ detection enable-signal enable$_{VCE}$ remains at the low level, which indicates that the $v_{ce}$ detection is disabled. Then the $v_{ce}$ detection-signal error$_{VCE}$ also remains at the low level.

Similarly, Figure 10 shows the simulation waveforms under the FUL condition. In Figure 10(a), due to the increase of $i_c$, the IGBT exits the saturation area. And $v_{ce}$ rises from the saturation voltage drop to $V_{DC}$. Figure 10(b) shows the fault detection logic simulation waveforms. When $v_{ge}$ is higher than $V_{ge(th)}$, $i_c$ rises slowly to the load current level, and $v_{ce}$ falls to $V_{CE(sat)}$. Because the $v_{ce}$ detection voltage $v_A$ is lower than $V_{REF2}$, the output-signal out$_2$ changes to the high level. And the $v_{ce}$ detection enable-signal from trigger enable$_{VCE}$ is high-level, so that the $v_{ce}$ detection is enabled. During FUL, $i_c$ rapidly rises up and $v_{ce}$ also climbs up to $V_{DC}$. Since $v_A$ is higher than $V_{REF3}$, the output-signal out$_3$ changes to the high level. And the $v_{ce}$ detection-signal error$_{VCE}$ is high-level, so that the fault detection-signal error$_{sc}$ changes to the high level. The change of the collector current rate $di/dt$ under FUL is much smaller than the one in HSF. Therefore, $r_{PE-E}$ is higher than $V_{REF1}$ during FUL, so that the $di/dt$ detection-signal error$_{di/dt}$ remains at the low level, which indicates the $di/dt$ detection is disabled.

### 4.2 Simulated short-circuit tests

To analyse the feasibility of the proposed detection method, the simulated short-circuit tests are carried out. And the experimental results are shown in Figure 11. Based on the characteristics of the short-circuit faults, the induced voltage $r_{PE-E}$ is replaced with an adjustable DC voltage between the power emitter (PE) and Kelvin emitter (E) terminals of gate driver to simulate HSF. In the same way, the $v_{ce}$ detection voltage $v_A$ is replaced with a changing voltage signal to simulate FUL. In Figure 11(a), when the control signal PWM is high-level, $v_{ge}$ also changes to 15 V from $-15$ V, which enables the $di/dt$ detection. Because $r_{PE-E}$ ($=-10$ V) is lower than the $di/dt$-detection threshold $V_{REF1}$
(\(-7.5\) V), the detection circuit considers the fault as the HSF mode. Then the gate driver performs the soft turn-off protection quickly. \(v_{ge}\) falls to the intermediate voltage \(V_{st}\) (\(= 10\) V) and holds for 2.5 \(\mu\)s and then shuts down. It can be found that there is no detection blanking time and the whole detection time lasts about 400 ns. As shown in Figure 11(b), when \(v_{ge}\) remains 15 V and the measured voltage \(v_A\) is lower than the enable-threshold \(V_{REF2}\) (\(= 6.8\) V), the \(v_A\) detection is enabled. When \(v_A\) is higher than the fault-threshold \(V_{REF3}\) (\(= 6.8\) V), the detection circuit regards the fault as the FUL mode. Then the gate driver also performs the soft turn-off protection quickly. Then \(v_{ge}\) falls to the intermediate voltage \(V_{st}\) (\(= 10\) V) and holds for 2.5 \(\mu\)s and then shuts down.

It can be seen from the simulation results and the simulated short-circuit test results that there is no blanking time during the whole detection process. The proposed detection method can quickly detect HSF and FUL, which greatly shortens the duration of the short-circuit fault.

### 4.3 Double pulse tests

In order to test the stability and rationality of the gate driver in the actual circuit, the double-pulse setup is used to carry out the double-pulse test (using Infineon IGBT module: FF450R33TE3). The test schematic and the setup are shown in Figure 12. In the double-pulse test, the relationship between the load current change \(\Delta i_c\), the bus voltage \(V_{DC}\) and load inductance \(L_{load}\) can be expressed as

\[
\Delta i_c = \frac{V_{DC} \times \Delta t}{L_{load}}
\]

The test is done under the bus voltage 1500 V and gate-emitter voltage \(\pm 15\) V in which the load inductance is 150 \(\mu\)H. In the double-pulse test, firstly a steady turn-off signal is given to the top device \(Q_1\) and then a long turn-on pulse is applied to the bottom device \(Q_2\) in Figure 12. And \(V_{DC}\) is applied across the load inductor during this time interval, and therefore the collector current \(i_c\) rises. The duration of this pulse is adjusted according to the required test current. \(Q_2\) is turned off at the end of the first pulse. And \(i_c\) free-wheels through the diode while the IGBT is off. After a short while, \(Q_2\) is turned on again, and \(i_c\) commutates from the free-wheeling diode to the IGBT. The \(Q_2\) off time between these two pulses is kept short so that the change in inductor current is minor. Then \(Q_2\) is turned off again after a small time interval, and \(i_c\) flows through the diode until it gradually reduces to zero.

The double-pulse test waveforms for 1500 V and 450 A are shown in Figure 13. The device turn-off characteristics is obtained at the falling edge of the first pulse, and the turn-on characteristics is obtained at the rising edge of the second pulse. In Figure 13(a) the overall record during the double-pulse test is shown, while Figure 13(b) shows the turn-off transition and Figure 13(c) presents the turn-on transition. The width of the first pulse is set according to the rated current level, which is 450 A in this particular case. At the end of the first pulse, the IGBT turns off, and the peak overvoltage \(V_{peak}\) is 2010 V, which does not exceed the breakdown voltage. After a short while, the IGBT is turned on again, and the maximum current \(I_{peak}\) is 670 A, which is lower than the repetitive peak current.

According to the switching waveforms of the IGBT, both the turn-on and turn-off transitions are consistent with the actual application. And the gate driver can provide sufficient driving capacity to ensure the reliable operation of the IGBT, which fulfils the design requirements.

### 4.4 Short-circuit tests

In order to verify the effectiveness of the proposed detection method in the actual circuit, two kinds of short-circuit tests are
carried out. The test schematic and the setup are shown in Figure 14. The tests are done under the bus voltage 1500 V and gate-emitter voltage ±15 V for IGBT module FF450R33TE3. Similarly, a stable turn-off signal is applied to the top device Q1 in Figure 14. Considering that the IGBT can withstand the short-circuit condition for 10 \( \mu \text{s} \), thus a single pulse (15 V, 15 \( \mu \text{s} \)) is applied to the bottom device Q2. Moreover, the copper bars and the small inductor 6 \( \mu \text{H} \) are usually used to replace the load inductance to simulate HSF and FUL in the experiments. Figure 15 shows the hard-switch-fault test waveforms using the homemade and domestic QD series gate drivers. In Figure 15(a), the control signal is changed from low level to high level and \( v_{\text{ge}} \) begins to rise. After about 2 \( \mu \text{s} \), \( v_{\text{ge}} \) reaches \( V_{\text{ge(th)}} \) and \( i_{\text{c}} \) begins to rise quickly. At this time, \( v_{\text{ce}} \) drops slightly and \( v_{\text{PE-E}} \) starts to decrease because of \( \frac{\text{di}}{\text{dt}} \). After 1.8 \( \mu \text{s} \), the measured \( v_{\text{PE-E}} \) is lower than the \( \frac{\text{di}}{\text{dt}} \)-detection threshold \( V_{\text{REF1}} \) (\( = -7.5 \text{ V} \)). And the detection circuit recognizes that the IGBT is under the HSF condition. Then the gate driver performs the soft two-level turn-off protection quickly. The \( v_{\text{ge}} \) falls to the intermediate level and holds for 2.5 \( \mu \text{s} \) and then shuts down. As viewed from the waveforms, short-circuit detection and protection circuits work normally.

As shown in Figure 15(b), there is only the \( v_{\text{ce}} \) detection in the domestic QD series gate drivers without soft turn-off protection. With the conventional method, the IGBT is turned off 5 \( \mu \text{s} \) after the short-circuit event. Compared with the proposed
FIGURE 16 Fault under load test waveforms. (a) Homemade gate driver, (b) domestic QD series gate driver

detection method, the protection time is longer and the peak overvoltage $V_{\text{peak}}$ is higher.

Figure 16 shows the fault-under-load test waveforms using the homemade and domestic QD series gate drivers. The rising rate of the collector current $dI/dt$ under FUL is much lower than the one in HSF. Initially $v_{ce}$ falls to $V_{\text{CE(sat)}}$ from $V_{DC}$, which enables the $v_{ce}$ detection. In Figure 16(a), as $i_c$ increases and reaches 1300 A, $v_{ce}$ starts to rise up to $V_{DC}$. When the measured $v_A$ is higher than the $v_{ce}$-detection threshold $V_{\text{REF3}}$ ($=6.8$ V), the detection circuit recognizes that the IGBT is under the FUL condition. Then the gate driver also performs the soft two-level turn-off protection quickly. After about 5 $\mu$s, the IGBT exits the saturation state with an $L_{\text{load}}$ of 6 $\mu$H. Then the IGBT under the FUL is turned off 3 $\mu$s after the short-circuit event. During the soft turn-off protection process, $i_c$ gradually drops to twice the rated current, in which $V_{\text{peak}}$ is lower than the one when the IGBT is turned off.

As shown in Figure 16(b), the QD series gate drivers do not have the soft turn-off protection. When $i_c$ reaches 1150 A, the IGBT is pulled out of its saturation state. As $i_c$ continues to rise, the IGBT is turned off 1 $\mu$s after the short-circuit event. Without an intermediate level, the turn-off peak overvoltage $V_{\text{peak}}$ reaches 2500 V due to the higher turn-off current.

The performance of the homemade gate driver with the proposed detection method (NBTD-IDR) is compared with that of the domestic QD series gate driver (QDT-IDR) in Table 2. Different features confirm that the proposed detection method is superior to the conventional $v_{ce}$ detection method. In HSF, compared with the QDT-IDR, the proposed detection method reduces the fault-detection time and peak overvoltage $V_{\text{peak}}$ to 1.8 $\mu$s and 2000 V, respectively. In FUL, compared with the QDT-IDR, the proposed detection method reduces the fault-detection time and peak overvoltage $V_{\text{peak}}$ to 5.0 $\mu$s and 2100 V, respectively.

Moreover, Table 3 compares the proposed detection method with other conventional methods. The $v_{ce}$ detection method is quite cheap and easily implementable. However, it requires blanking time, which can prolong the short-circuit time. And the blanking time should be carefully designed for different types of IGBT modules, which increases the difficulty of driver design. The fault-detection time of the $v_{ge}$ detection method is short, but $v_{ge}$ is easily affected by parasitic parameters. Therefore, the detection circuit is complicated because of its extraordinary sensitivity, and has low reliability. The $i_c$ detection method using sense resistor or Rogowski coil is capable of measuring a very high $dI/dt$ with a short delay. However, it is susceptible to external electromagnetic interference and expensive to produce. The $dI/dt$ detection method responds fast with a low cost easy-to-integrate detection circuit. But it does not take various short-circuit faults into account.

Based on the combination of $v_{ce}$ detection and $dI/dt$ detection, the proposed detection method can quickly detect the short-circuit faults with a minimum delay time, and flexibly adjust the fault-detection threshold voltages. The elimination of the blanking time is realized with the logic control strategy under different operation conditions. The $dI/dt$ detection

| Features | NBTD-IDR | QDT-IDR |
|----------|----------|---------|
| Does it integrate the soft turn-off protection? | Yes | No |
| Blanking time | 0 $\mu$s | 4.0 $\mu$s |
| Time for detecting HSF | 1.8 $\mu$s | 5.0 $\mu$s |
| Peak overvoltage of HSF | 2000 V | 2200 V |
| Time for detecting FUL | 5.0 $\mu$s | 5.0 $\mu$s |
| Peak overvoltage of FUL | 2100 V | 2500 V |
| Fault-detection time | Short | Long |
| Peak overvoltage $V_{\text{peak}}$ | Low | High |
| Short-circuit energy loss | Low | High |

| Detection methods | For FUL | Complexity | Cost | Response time |
|-------------------|---------|------------|------|--------------|
| $v_{ce}$ method   | Yes     | Low        | Low  | Slow         |
| $v_{ge}$ method   | Yes     | High       | High | Medium       |
| $i_c$ method      | Yes     | High       | High | Fast         |
| $dI/dt$ method    | No      | Low        | Low  | Fast         |
| NBTD method       | Yes     | Medium     | Medium | Fast     |
method can detect HSF efficiently. For FUL, the $r_{ce}$ detection method is not enabled until $r_{ce}$ falls to $V_{CE(sat)}$. Once $r_{ce}$ begins to increase during the on-state, the soft turn-off protection is performed by gate driver immediately. Moreover, the two-level turn-off protection can reduce the short-circuit current and loss to a relatively safe level, in which the peak overvoltage can be suppressed to a safe range. Compared with other conventional methods, the proposed method can also reduce the design complexity and cost of the detection circuit, and improve the reliability and applicability of gate driver.

5 CONCLUSIONS

In this paper, the short-circuit failure modes and mechanisms of the IGBT have been discussed in an effort to determine the detection circuits. Methods of fault detection have also been discussed. Their general advantages and disadvantages are pointed out so that an appropriate detection method may be selected. A short-circuit detection method without blanking time is presented for the IGBT gate driver. And its principle and implementation are discussed in detail. Afterward, the feasibility of the proposed short-circuit detection scheme is verified by the simulation results. Meanwhile, three different types of experiments are carried out: simulated short-circuit fault tests, double pulse tests and short-circuit tests. And the results show that the proposed circuit can detect short-circuit faults with a minimum delay time and perform the soft two-level turn-off protection quickly, which can shorten the short-circuit fault duration, reduce the short-circuit fault damage and prolong the useful life of the IGBTs. Moreover, it is suitable for the application on different kinds and working conditions of IGBT modules and the applicability of gate driver can be improved effectively.

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