Two CMOS time to digital converters using successive approximation register logic

Himchan Park\textsuperscript{a), Qiwei Huang, Changzhi Yu, Seulki Kim, Gilcho Ahn, and Jinwook Burm\textsuperscript{b)}}

Department of Electronic Engineering, Sogang University, 35, Baekbeom-ro, Mapo-gu, Seoul, Republic of Korea
\textsuperscript{a}) hcparks@naver.com
\textsuperscript{b}) burm@sogang.ac.kr

Abstract: This letter presents two CMOS time-to-digital converters (TDCs) with a conventional successive approximation register (SAR) logic and SAR continuous disassembly (CD) logic. In a flash TDC, a high-bit thermometer to binary converter consumes a large silicon area and power, which prevents the simple flash TDC structure be widely used in modern electrical devices. By separating the delay chain in a flash TDC with binary sequences, the SAR logics can eliminate the thermometer to binary code converter essential for a flash TDC. The two TDCs using conventional SAR and SAR CD logics were fabricated in a 0.18 µm CMOS technology with power consumption of 1.5 mW and 1.3 mW at a sampling rate of 10 Msamples/s and occupied 0.074 mm\textsuperscript{2} and 0.041 mm\textsuperscript{2} active areas, respectively.

Keywords: time-to-digital converters (TDCs), successive approximation register (SAR)

Classification: Integrated circuits

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1 Introduction

A time-to-digital converter (TDC) is used to digitize a time difference to digital code for the further digital signal processor (DSP) in various applications, such as time-of-flight (ToF) measurements used in LiDAR systems [1, 6, 7, 8, 9, 10] and digital phase locked loop (DPLL) [2]. Also, by converting voltage to time difference, a time-based analog-to-digital converter (ADC) could be designed with a high resolution, while consuming less power [3]. Referring to ADC structures, researchers have developed various structures of TDC recently. A conventional SAR TDC has been presented in [4], and an SAR CD (continuous disassembly) TDC has been presented in [5], both of them are at integrated CMOS circuit level.

2 Circuit implementations

The flowcharts operation examples of the proposed TDCs are shown in Fig. 1. The digital output is d<5:0>, the time resolution is one delay cell’s delay time and the input time is assigned to variable ‘value’. For the conventional SAR logic, the ‘value’ is updated according to the corresponding d<i> and time weight 2^iΔt, where Δt is the minimum time step. For the SAR CD logic, the ‘value’ is updated only by the time weight 2^iΔt, while the digital output d<i> is generated from the exclusive nor operation of d<i+1> and d<i> (i.e., d<i+1> xnor d<i>).

For a better illustration, two operation examples with a 45.2Δt time input are shown in Fig. 1. For the conventional SAR TDC, 45.2 is larger than 32 at the first iteration, then d<5> = 1 and the time residue becomes 13.2. For the next iteration, 13.2 is smaller than 16, then d<4> = 0 and the time residue is also 13.2. Through the flowchart of conventional SAR logic, the final digital output is 101101 in the conventional SAR TDC. For the SAR CD logic, the first iteration is the same as the conventional SAR logic because 45.2 is larger than 32. For the second iteration, 13.2 is smaller than 16, then d<4> = 0 and being updated to 0 with xnor to d<5>, while the time residue does not relate to the digital output d<4> and is the absolute value of 13.2 – 16 = −2.8. After total six iterations, the final digital output is also 101101 as the conventional SAR TDC.

To reduce the circuit’s complexity, we propose two new circuit implementations of TDC with SAR and SAR CD logics at integrated CMOS circuit level as shown in...
Fig. 1. Flowcharts and operation examples of proposed TDCs with a 45.2\(\Delta_t\) time input (\(\Delta_t\) is omitted in the figure, a Conventional SAR logic, b SAR CD logic)
in Fig. 2. The time input of TDC is the time difference of EIN_{5} and LIN_{5}, where EIN_{i} represents the earlier signal (or the time for the rising edge of the earlier signal) and LIN_{i} represents the later signal (or the time for the rising edge of the later signal) for STEP_{i} with an index i. The compared delay time for STEP_{i} is 2^{i}Δ_{t}. The time residue at the output of each STEP is determined by the time difference of EIN_{i} and LIN_{i}. Since the later signal occurs later in time, EIN_{i} < LIN_{i} always holds.

For the process, EIN_{i} < LIN_{i} always holds.

Fig. 2. Circuit implementations of the proposed TDCs

a Conventional SAR TDC if (L_{IN_i} − E_{IN_i}) > 2^{i}Δ_{t}, then (L_{OUT_i} − E_{OUT_i}) = (L_{IN_i} − E_{IN_i}) − 2^{i}Δ_{t}, else (L_{OUT_i} − E_{OUT_i}) = (L_{IN_i} − E_{IN_i})

SAR CD TDC if (L_{IN_i} − E_{IN_i}) > 2^{i}Δ_{t}, then E_{OUT_i} = E_{IN_i} + 2^{i}Δ_{t}
and L_{OUT_i} = L_{IN_i}, else L_{OUT_i} = E_{IN_i} + 2^{i}Δ_{t} and E_{OUT_i} = L_{IN_i}. For the process, E_{IN_i} < L_{IN_i} always holds.
signal $E_{INi}$ and the later signal $L_{INi}$ have to wait for $2^i \Delta t$ to process the time information. Also, a delay longer than the response time of the arbiter and the multiplexers is necessary for the correction operation. For the SAR CD TDC as shown in Fig. 2b, the input time enters to STEP_5 and $E_{IN5}$ goes through the $2^5 \Delta t$ time delay. If the time difference is larger than $2^5 \Delta t$, the arbiter’s outputs $Sel = 0$ and $Q_5 = 1$, otherwise $Sel = 1$ and $Q_5 = 0$. Unlike the conventional SAR TDC, the output time residue for the next STEP is always the absolute value of $(E_{IN5} - L_{IN5} - 2^5 \Delta t)$. Again a delay accounting for the response time of the arbiter and the multiplexer is needed, however the delay time is smaller that that for conventional SAR logic (Fig. 2b). After processing in every STEP, the input time could be converted to a series code $Q_{5-0}$ and then to the final digital output $D_{5-0}$ from the xnor gates in Fig. 2b.

3 Measurement result

Fig. 3 shows the chip micrographs of the proposed TDCs. The two TDCs using conventional SAR and SAR CD logics were fabricated in a 0.18 $\mu$m CMOS technology with power consumption of 1.5 mW and 1.3 mW at a sampling rate of 10 Msamples/s and occupied 0.074 mm$^2$ and 0.041 mm$^2$ active areas, respectively.

Two crystal oscillators, whose measured frequencies are 10.0000224 MHz and 10.0000241 MHz measured by MS2690A signal analyzer are used to generate a ramp input time for the TDCs, and a logic analyzer collects the digital outputs of TDCs. The digital output code versus input time and their corresponding DNLs and INLs are shown in Fig. 4. The conventional SAR TDC has a time resolution of 54.6 ps, and the SAR CD TDC has a time a time resolution of 68.7 ps. The two TDCs were fabricated on different wafers, which introduced process variations to the time resolution. The two TDCs achieved the maximum DNLs of $\pm 0.57$ and $\pm 0.65$, INLs of $\pm 2.51$ and $\pm 1.96$, respectively. The SAR CD TDC has a better...
linearity performance than the conventional SAR TDC due to fewer delay cells were used to reduce the mismatches.

4 Conclusion

In this letter, we presented two TDCs using the conventional SAR logic and SAR CD logic to eliminate the thermometer to binary code converter, which consumes a large silicon area in high-bit flash TDC. It is also possible to use the proposed circuits to separate the delay chain in a Vernier TDC with binary sequences to improve the time resolution.

Acknowledgments

This research was supported by Institute for Information & communications Technology Promotion (IITP) grant funded by the Korea government (MSIT) (2016-0-00136 Development of Hall Effect Semiconductor for Smart Car and Device), by the MOTIE (Ministry of Trade, Industry & Energy) (project number 10080622) and KSRC (Korea Semiconductor Research Consortium) support program for the development of the future semiconductor device, by the MSIT.
(Ministry of Science and ICT), Korea, under the ITRC (Information Technology Research Center) support program (IITP-2018-0-01421) supervised by the IITP (Institute for Information & communications Technology Promotion) and by National Research Foundation of Korea under the contract No. NRF-2018R1D1A1B07049663. This work is also supported by IDEC (IPC, EDA Tool, MPW).