A Self-Powered and Area Efficient SSHI Rectifier for Piezoelectric Harvesters

SALAR CHAMANIAN (Member, IEEE), BERKAY ÇİFTÇİ (Member, IEEE), ALİ MUHTAROĞLU (Senior Member, IEEE), AND HALUK KÜLAH (Member, IEEE)

1Department of Electrical and Electronics Engineering, Middle East Technical University (METU), 06800 Ankara, Turkey
2Department of Electrical and Computer Engineering, University of California at San Diego, San Diego, CA 92093, USA
3Department of Electrical and Electronics Engineering, Middle East Technical University–Northern Cyprus Campus, 99738 Mersin, Turkey
4Center for Sustainability, Middle East Technical University–Northern Cyprus Campus (METU-NCC), 99738 Mersin, Turkey
5METU-MEMS Research and Applications Center, Middle East Technical University, 06800 Ankara, Turkey

Corresponding author: Salar Chamanian (salar.chamanian@metu.edu.tr)

This work was supported by the European Research Council (ERC) under the European Union’s Horizon 2020 Research and Innovation Program under Grant 682756.

ABSTRACT This article presents an area efficient fully autonomous piezoelectric energy harvesting system to scavenge energy from periodic vibrations. Extraction rectifier utilized in the system is based on synchronized switch harvesting on inductor (SSHI) technique which enables system to outperform standard passive rectifiers. Compared to conventional SSHI circuits, enhanced SSHI (E-SSHI) system proposed in this paper uses a single low-profile external inductor in the range of $\mu$H’s to reduce overall system cost and volume, hence broadening application areas of such harvesting systems. Furthermore, E-SSHI does not include any negative voltage converter circuit and therefore, it offers area efficient AC/DC rectification. Detection of optimal voltage flipping times in E-SSHI technique is conducted autonomously without any external calibration. Energy transfer circuit provides control over how much energy is delivered from E-SSHI output to electronic load. The proposed system is fabricated in 180 nm CMOS process with 0.28 mm² active area. It is tested using a commercial piezoelectric transducer MIDE V22BL with periodic excitation. Measured results reveal that E-SSHI circuit is capable of extracting up to 5.23 and 4.02 times more power compared with an ideal full-bridge rectifier at 0.87 V and 2.6 V piezoelectric open circuit voltage amplitudes ($V_{OC,P}$), respectively. A maximum voltage flipping efficiency of 93% is observed at $V_{OC,P} = 3.6$ V, owing to minimized losses on charge flipping path. Measured results are compared with state-of-the-art interface circuits. Comparison shows that E-SSHI design offers a huge step towards miniaturized harvesting systems thanks to its low-profile and fully autonomous design.

INDEX TERMS Autonomous, low-profile, piezoelectric energy harvester, SSHI, optimal charge flipping, area efficient, IC.

I. INTRODUCTION Downsizing in state-of-the-art and efficient wireless sensor networks (WSNs) makes them alluring for biomedical devices and many other applications where system size is a big concern [1]. Recently, power dissipation levels of such systems have been diminished thanks to advanced fabrication techniques which enable electronic circuits to support lower supply voltage levels. Still, maintaining power to portable electronic devices necessitates usage of external bulky batteries that enlarges system volume and restricts their application areas. Furthermore, batteries require continuous charging to keep electronic circuits inside WSN systems up and running for a long time. These bulky batteries with limited capacity can be removed from the system by making use of energy scavenging (i.e. energy harvesting) to power up electronic loads [1], [2]. Medical devices (health monitoring sensors, implantable pacemakers etc.), active RFID tags, and predictive maintenance could be counted as application areas for energy harvesting practices [1]. In an environment where temperature gradients and solar radiations are low, ambient vibrations are the most appealing ones owing to...
their abundance [3]. There are three main kinetic conversion principles (capacitive, inductive, and piezoelectric conversion principles) emerge for harvesting energy from vibrations or motions [4]. In centimetric or millimetric energy harvesting applications, piezoelectric energy harvesters (PEHs) are widely chosen to convert mechanical energy into electrical one thanks to their high power density and compatibility with standard CMOS fabrication processes [5]. PEH produces AC voltage of time-varying levels with excitation variations. Thus, rectification and regulation stages are needed before PEH can be utilized as a power source for WSN electronics.

During early days of PEH interface circuit design, usage of standard AC/DC rectification circuits such as full bridge rectifiers (FBRs) and voltage doublers were quite popular thanks to their simplicity [6], [7]. Yet, voltage drops on rectifier diodes hinders standard rectifiers to deliver all of generated energy on PEH to the loading circuitry. Moreover, built-in PEH capacitance needs to be charged and discharged to reach output voltage before charge transfer to the output load starts. Circuits in [8], [9] implement maximum power point tracking (MPPT) to match PEH impedance to output. However, they concentrate on matching the real parts and therefore, they lose considerable amount of energy at PEH capacitance. Nonlinear processing of piezoelectric voltage has been investigated deeply as a possible alternative solution to boost energy extraction from PEHs [3], [10]. Synchronous electric charge extraction (SECE) [5], [11]–[13] and synchronized switch harvesting on inductor (SSHI) [14]–[17] are two most common nonlinear switching techniques utilized in the literature. An external inductor is employed in SECE configuration to both decouple PEH from the system and transfer energy to output at maximum deflection of piezoelectric beam. Multi-stage energy extraction technique, published in [5], improves power conversion efficiency compared to conventional SECE circuits. To do so, it delivers load independent power through multiple energy packages, which reduces conduction losses on charging path. [11] reuses some of the charge transferred to battery as energy investment to PEH capacitance. Correspondingly, aforementioned circuit increases damping force and improves extracted output power.

Recently published SECE circuit in [13] is capable of harvesting energy from sporadic high voltage inputs thanks to its unique control circuit. Unfortunately, it contains on-chip FBR working as negative voltage converter, which hinders significant power extraction improvements. Another common nonlinear technique called SSHI utilizes an inductor to reverse the polarity of residual voltage on PEH capacitance after charging ends, and extends energy transfer duration to the battery. Output power delivered in SSHI method is unavoidably load dependent owing to the coupling between harvester and output load. Bias flip rectifier introduced in [14] offers improvement in power extraction capacity over FBRs by more than four times; however, it rectifies AC source voltage through an on-chip FBR and occupies more than 4 mm² chip area. The main focus of [15] is to attain a complete energy harvesting platform which integrates a conventional SSHI circuit and a MEMS harvester. Small external inductor causes poor voltage flipping efficiency, and therefore restricts power extraction improvement. SSHI rectifiers proposed in [16], [17] are both capable of scavenging energy from PEHs while incorporating maximum power point tracking (MPPT). [16] requires external calibration of sub-units to achieve MPPT, whereas perturb and observe (P&O) method employed in [17] necessitates complex control and evaluation circuits, which make both approaches hard to implement. Optimal SSHI circuit presented in [18] achieves optimum voltage flipping durations thanks to its active diodes. Unfortunately, MOSFET switches controlling energy transfer to the output load necessitate internal clock generation to determine charging interval. This clock generation demands external adjustment for different excitation frequencies and PEHs which will limit the application area. One important problem with current SECE and SSHI circuits is that they rely on bulky external inductors to reach desirable output power and power conversion efficiencies. These inductors limit application areas of energy harvesting in implantable micro-devices since they enlarge overall system volume significantly.

Lately, inductorless interfacing techniques have been proposed to shrink the size of energy harvesting systems [19]–[22]. They present a huge step towards system miniaturization. Instead of an external inductor, circuits in [19], [20] use switched capacitors (SCs) to flip residual voltage on PEH capacitance. Eight off-chip voltage flipping capacitors with matching values to PEH capacitance in [19] increase system volume. This problem is solved in flipping-capacitor rectifier (FCR) proposed in [20] which utilizes on-chip capacitors. Nevertheless, its functionality is limited to PEHs with inherent capacitance in pF range and excitation frequency around 100 kHz. Synchronized switch harvesting on capacitor (SSHC) circuit proposed recently in [21] is an advanced version of [19]. Thanks to split-electrode MEMS harvester utilized, voltage flipping capacitors are implemented on-chip. Due to significant number of switching required for voltage flipping, conversion efficiency and power extraction improvement are reduced. Besides, both SSHI [14], [16], [17] and inductorless [19]–[21] design techniques need external adjustments (i.e. calibrations) to achieve optimum voltage flipping times. Obtaining the moment of optimum voltage flipping in harvesting circuit is quite critical since this directly impacts maximum output power level.

The aim of this work is to implement an autonomous low-profile (i.e. volumes occupied by external components are small) interface circuit to extract energy from conventional PEHs. Enhanced SSHI (E-SSHI) rectification method that does not require any negative voltage converter (NVC free) is utilized to expand delivered output power in an area efficient (0.28 mm²) chip. Unlike SSHI [14], [16], [17] and Inductorless [19]–[21] designs, optimum charge flipping times and charging intervals are detected autonomously.
Autonomous charge flipping and low-profile design features of E-SSHI make this system desirable in miniaturized harvesting systems. Section II provides operation principle of E-SSHI circuit and theoretical output power calculation. Implementation details of sub-units are introduced in section III. Experimental results of the fabricated ICs and performance comparison with state-of-the-art are included in section IV. Finally, section V concludes the paper.

II. ENHANCED SSHI INTERFACE CIRCUIT

Fig. 1 depicts the proposed energy harvester interfacing system. AC/DC rectification is achieved by E-SSHI circuit. It makes use of the external inductor $L_{\text{EXT}}$ in the range of $\mu$H's to flip residual voltage on PEH capacitance and broadens the duration of storage capacitance $C_{\text{STOR}}$ charging. Resistor $R_{\text{BIAS}}$ helps tuning the internally generated reference voltage levels. Energy transfer circuit determines how much energy stored on $C_{\text{STOR}}$ is delivered to output capacitance $C_{\text{OUT}}$. External resistors $R_{\text{EXT}1}$, $R_{\text{EXT}2}$, and $R_{\text{EXT}3}$ provides fractions of storage voltage $V_{\text{STOR}}$ that are needed to govern energy transfer process. Low-dropout (LDO) regulator was added for the sake of system integrity. If needed, it provides desired regulated voltage levels (lower than $V_{\text{STOR}}$ voltage) for electronic loads.

A. E-SSHI OPERATION PRINCIPLE

Simplified schematic of E-SSHI circuit is provided in Fig. 2. Four MOSFET switches steer current flow in the system. Equivalent circuits constructed in each operation phase is shown in Fig. 3. Initially, $S_1$ is the sole ON switch and upward strain on piezoelectric beam caused by ambient vibrations generates the positive charge on PEH capacitance $C_{\text{PZ}}$ (Phase 1). During that phase, one terminal of PEH ($V_N$ node) is connected to ground and voltage $V_P$ increases. The moment when $V_P$ surpasses storage voltage $V_{\text{STOR}}$, switch $S_2$ starts conducting and charge accumulation on $C_{\text{STOR}}$ begins (Phase 2). In contrast to conventional SSHI circuits, this system does not require any negative voltage converter for battery charging purposes. Charging process ends when $V_{\text{STOR}}$ becomes less than $V_P$ and $S_2$ turns OFF. At the same time, $S_3$ turns ON to initiate voltage flipping on PEH capacitance $C_{\text{PZ}}$ (Phase 3). LC resonance circuit is established in order to transfer residual charge on $C_{\text{PZ}}$ firstly to external inductor $L_{\text{EXT}}$ and then back to $C_{\text{PZ}}$ with reverse polarity. Voltage flipping is finalized when there is no residual charge left on $L_{\text{EXT}}$. Then, $S_1$ stops its conduction and negative charge generation is initiated (Phase 4) where voltage on node $V_N$ rises with swinging of piezoelectric beam
(negative half cycle). Charge accumulated on $C_{PZ}$ during negative charge generation phase is transferred through $S_3$ and $S_4$ when $V_N$ exceeds $V_{STOR}$ (Phase 5). When $V_N$ recedes below $V_{STOR}$, $S_4$ is deactivated and conduction path between PEH capacitance $C_{PZ}$ and $C_{STOR}$ is broken. Meanwhile, system goes into the phase 6 in which $S_1$ is turned ON to launch negative voltage flipping on PEH capacitance $C_{PZ}$, just as in phase 3. When charge on $L_{EXT}$ is depleted, voltage on $C_{PZ}$ is reversed and system goes back into phase 1 by turning $S_3$ OFF. Fig. 4 depicts simulation waveforms of $V_{PZT}$, $V_N$, $V_P$, and inductor current $i_{FLIP}$ observed during operation phases.

**FIGURE 4.** Simulation waveforms of PEH terminals $V_{PZT}$ and $V_N$, inductor current $i_{FLIP}$, and the node $V_P$ observed during E-SSHI operation phases.

### B. OUTPUT POWER CALCULATION

PEH equivalent model parameters can be employed to express the extracted output power of E-SSHI interface circuit. Fig. 5 shows the electromechanical equivalent circuit of a piezoelectric harvester and representative waveform of voltage difference between the terminals of PEH when E-SSHI circuit is used as the interface electronics [4]. Voltage source $V_{MC} = maT$ represents the alternating (sinusoidal) input excitation force of the harvester ($T$ is the electromechanical coupling factor, $a$ is the acceleration, and $m$ is the mass of the piezoelectric beam). $L_{MC} = m/\Gamma^2$ is related to effective mass, $R_{MC} = d/\Gamma^2$ represents the damping, $C_{MC} = \Gamma^2/K$ gives effect of piezoelectric stiffness $K$, and $C_{PZ}$ is the inherent piezoelectric harvester capacitance [4], [23], [24]. Provided that the harvester is lowly coupled and/or highly damped, PEH model presented in Fig. 5 can be further simplified using inherent piezoelectric capacitance $C_{PZ}$ in parallel with the current source $i_{PZ}$ as shown in Fig. 2 [19], [23], [24].

In order to calculate theoretical harvested power of E-SSHI interface, we first assume that the circuit is at the beginning of the first phase in which electrical charge is accumulated on $C_{PZ}$ with swinging of piezoelectric beam. Moreover, PEH is excited with its natural resonance frequency and higher harmonic terms of $V_{MC}$ are ignored [23]. At the beginning of phase 1, which corresponds to time $t = 0$ and $t = T$ in Fig. 5, initial voltage $V_{PZ}(t = 0)$ on $C_{PZ}$ is:

$$v_{PZ} = V_F = \left(2\eta_F - 1\right) V_{STOR},$$

(1)

where $\eta_F$ is defined as voltage flipping efficiency:

$$\eta_F = \frac{V_F + V_{STOR}}{2 V_{STOR}} \Longleftrightarrow V_F = V_{STOR} \left(2\eta_F - 1\right),$$

(2)

where $V_F$ is the flipped voltage after charging. The terminal law for capacitors states:

$$i_{PZ} = C_{PZ} \frac{dv_{PZ}}{dt} \Longrightarrow i_{PZ} dt = C_{PZ} dv_{PZ},$$

(3)

where $i_{PZ} = I_{PZ} \sin(\omega_N t)$, $I_{PZ}$ is the amplitude of $i_{PZ}$, and $\omega_N = 2\pi/T$ is the natural resonance frequency of the PEH (PEH is excited at its resonance frequency). Assume that at $t = T_1$, $V_{PZ}$ becomes larger than $V_{STOR}$ and therefore, PEH starts charging $C_{STOR}$. This time is represented on the waveform in Fig. 5. Integration of both sides of equation (3) from $t = 0$ to $t = T_1$ results in:

$$\int_{t=0}^{T_1} I_{PZ} \sin(\omega_N t) dt = \int_{v_{PZ}(0)}^{v_{PZ}(T_1)} C_{PZ} dv_{PZ},$$

(4)

$$-\frac{I_{PZ}}{w_N} \cos(\omega_N t) \bigg|_{t=0}^{t=T_1} = C_{PZ} \left[ v_{PZ}(T_1) - v_{PZ}(0) \right],$$

(5)

where $v_{PZ}(T_1) = V_{STOR}$ and $v_{PZ}(0) = V_F = V_{STOR} (2\eta_F - 1)$. Then:

$$T_1 = \frac{1}{w_N} \cos^{-1} \left[ 1 - \frac{w_N C_{PZ} V_{STOR} (2\eta_F - 1)}{I_{PZ}} \right].$$

(6)
Following the charge accumulation phase, between \( t = T_1 \) and \( t = T/2 \) (Phase 2), \( C_{\text{STOR}} \) is charged \( (T = 2\pi/\omega N) \). Amount of power extracted on that phase is expressed as:

\[
P_{\text{OUT}} = \frac{1}{T/2 - T_1} \int_{t=0}^{T/2} V_{\text{STOR}} I_{PZ} \sin(w_N t) \, dt, \quad (7)
\]

under the assumption that \( V_{\text{STOR}} \) does not change much during charging. If \( \eta_F > 80\% \), then approximation \( T/2 - T_1 \approx T/2 \) holds. Therefore:

\[
P_{\text{OUT}} = \frac{2}{T} V_{\text{STOR}} I_{PZ} \left[ \cos(w_N T_1) \right]_{t=T_2}^{t=T}, \quad (8)
\]

Substituting for \( T_1 \) from equation (6) into (9), the following equation is derived,

\[
P_{\text{OUT}} = \frac{2V_{\text{STOR}} I_{PZ}}{\pi} - \frac{4}{T} C_{PZ} V_{\text{STOR}}^2 (1 - \eta_F), \quad (10)
\]

which is exactly the same as the expression found in [23]. Furthermore, optimum storage voltage calculation was provided in detail in [23] as:

\[
V_{\text{STOR,OPT}} = \frac{\pi V_{MC}}{8(1 - \frac{1}{\pi^2}(1 - \eta_F) f C_{PZ})}, \quad (11)
\]

where \( V_{MC} = ma/\Gamma \) and \( f = 1/T \). Optimum storage voltage \( V_{\text{STOR,OPT}} \) depends on PEH equivalent model parameters \( (C_{PZ}, \Gamma) \), input excitation of the harvester \( (V_{MC}, f) \), and interface circuit performance \( (\eta_F) \). Thus, to keep storage voltage level at optimum, a dedicated maximum power point tracking (MPPT) system is required which is not the focus of this study.

### III. CIRCUIT IMPLEMENTATION

Fig. 6 presents implementation details of enhanced SSSI (E-SSI) circuit. E-SSI circuit has five sub-units. Some of E-SSI sub-units, which are called start-up trigger circuit, reverse current detector, and voltage reference, are quite similar to the ones presented in [25]. Start-up block monitors storage voltage level \( V_{\text{STOR}} \) during cold start operation and generates a triggering signal \( \text{EN}_{\text{TRIG}} \) when sufficient charge accumulates on \( C_{\text{STOR}} \). This signal starts E-SSI operation phases illustrated in Fig. 3. It is important to note that during cold start, \( S_1 \) switch connects node \( V_N \) to ground and charging of \( C_{\text{STOR}} \) occurs through \( S_2 \). Reverse current detectors (RCDs) govern charging durations of output load \( C_{\text{STOR}} \) by comparing \( V_{\text{STOR}} \) with \( V_P \) and \( V_N \). They are disabled during voltage flipping phases to reduce system’s overall power consumption. Positive and negative charge flipping detectors (CFDs) check whether residual charge on external inductor \( L_{\text{EXT}} \) is transferred back to PEH capacitance \( C_{PZ} \). In contrast to conventional SSSI [14]–[16] and inductorless designs [19]–[21], they autonomously catch moments of optimum energy transfer from \( L_{\text{EXT}} \) to \( C_{PZ} \) in charge flipping phases (Phases 3 and 6) and communicate with switching control block using \( \text{DPC} \) and \( \text{DNC} \) signals. Switching control block, which makes use of control signals generated internally, is composed of various digital logic gates and SR latches. It determines ON and OFF durations of switches \( S_1 - S_4 \) and produces enable signals of other sub-units. These enabling signals help system to minimize its energy consumption. On-chip voltage reference circuit creates two stable voltage levels which are employed as biasing references in E-SSI system. Biasing voltage levels can be tuned externally via \( R_{\text{BIAS}} \). Sub-units inside E-SSI use \( V_{\text{STOR}} \) voltage as their supply voltage \( V_{\text{DD}} \) (E-SSI is a self-powered system).

#### A. START-UP TRIGGER

E-SSI circuit is capable of cold start-up operation. Thanks to \( S_1 \) and \( S_2 \), load capacitor \( C_{\text{STOR}} \) is charged passively during start-up, which does not demand usage of a negative voltage converter (NVC), unlike the scheme used in [16]. When \( V_{\text{STOR}} \) hits around 1.2 V, RCDs and SR latches in switching control block are enabled to sequence E-SSI phases. This sequencing is initiated by the start-up trigger circuit which is illustrated in Fig. 7.

Bias voltage levels develop at the gates of transistors \( M_1 \) and \( M_{11} \) during startup, while \( V_{\text{DD}} \) also builds up. The current through \( M_1 \) is mirrored through \( M_3 - M_4 - M_6 \) and charge is...
collected at M₈ and M₀ gates. Accumulated charge on the gates in a specific period can be adjusted using $V_{BIAS}$ voltage. M₈ and M₀ form an inverter that triggers generation of EN_TRIG signal, which in turn enables E-SSHI phases. Start-up trigger is deactivated entirely after the generation of EN_TRIG signal.

**B. REVERSE CURRENT DETECTORS**

E-SSHI circuit is capable of cold Autonomy in E-SSHI switching is secured by a set of reverse current detectors (RCDs) and charge flipping detectors (CFSs) which work in harmony. There exist two RCDs (RCD₁ and RCD₂) that are responsible for regulating $C_{STOR}$ (i.e. battery) charging duration in the course of positive and negative half cycles of piezoelectric motion. RCD circuit depicted in Fig. 8(a) benefits from a hybrid 2-stage comparator topology. Besides conventional differential input pair of M₉-M₁₀, transistors M₁₁ and M₁₂ form common gate configuration to facilitate detection sensitivity of the instant when $V_+$ first drops below $V_-$ ($V_{DD} = V_{STOR}$). Both RCDs are active for almost full duration of the piezoelectric half cycles. Therefore, their power dissipation levels have utmost importance on system efficiency. M₂₀ functions as a current limiter which curtails current drawn from supply voltage during RCD output transitions. Fig. 8(b) shows simulation waveforms of control signal generated by RCDs and CFDs. The waveform of C̄STOR charging current, $i_{CHARGE}$, is also provided in the same figure.

![FIGURE 8. (a) Schematic of reverse current detector (RCD) and (b) its simulation result showing generated control signals of both RCDs and charge flipping detectors (CFDs).](image)

**C. CHARGE FLIPPING DETECTORS**

The charge flipping sensors detect whether the current on the external inductor is depleted or not. Charge flipping action is accomplished when all current generated on the inductor $L_{EXT}$ flows back into the piezoelectric capacitance $C_{PZ}$. The structure presented in Fig. 9(a) senses the depletion point by monitoring voltage drops on S₁ and S₃. While the current on $L_{EXT}$ flows into $C_{PZ}$, sign change of voltage drops on switches indicates the end of charge flipping action.

![FIGURE 9. (a) Schematic of charge flipping detector (CFD) and (b) its simulation result indicating node voltage $V_P$, $V_N$, flipping current $i_{FLIP}$, and detection signal $D_{PCF}$.](image)

A current follower input stage monitoring switch voltage drops is followed by a common source amplifier and together they form the comparator as shown in Fig. 9(a). The transistor sizes are determined to provide required gain within sub-threshold biasing region. An offset is imposed by slightly mismatching the aspect ratio of M₈ and M₀ MOSFETs to avoid premature switching during transition. Mismatch is adjusted at differential stage through simulations to achieve 20 mV offset. High outputs of CFDs warn the system about the fact that inductor does not store any energy inside. Fig. 9(b) depicts simulation waveforms of $V_P$, $V_N$, $i_{FLIP}$ and detection signal $D_{PCF}$ observed in flipping action.

**D. VOLTAGE REFERENCE**

Biasing of E-SSHI sub-units is accomplished by the voltage reference circuit shown in Fig. 10(a). This is the modified version of PTAT bias-current generator designed in [11]. Gate-source voltage difference between M₁ and M₂ transistors builds a voltage drop on resistor $R_{BIAS}$. NMOS transistors M₃ and M₄ balance the bias current through M₁ and M₂. This supply independent current is mirrored through M₅ and M₆ and is then converted into reference voltage levels using NMOS saturated load transistors M₇, M₈, and M₉. M₅₁-M₅₅ and C₅ serve as start-up configuration. Generated reference
levels $V_{\text{REFH}}$ and $V_{\text{REFL}}$, whose simulation waveforms are provided against $V_{\text{DD}}$ in Fig. 10(b), can be tuned via $R_{\text{BIAS}}$.

**E. ENERGY TRANSFER CIRCUIT**

Amount of energy stored on $C_{\text{STOR}}$ (i.e. E-SSHI output) can be delivered to $C_{\text{OUT}}$ through energy transfer circuit (ETC) depicted in Fig. 11. As stated in output power calculation section, optimum storage voltage $V_{\text{STOR,OPT}}$ is contingent upon both PEH parameters and interface circuit performance. ETC is capable of providing controllable energy transfer in accordance with predetermined voltage threshold levels $V_{P1}$ and $V_{P2}$ to keep $V_{\text{STOR}}$ near its optimum value. These thresholds are adjusted with external resistors $R_{\text{EXT}}$, $R_{\text{EXT2}}$, and $R_{\text{EXT3}}$. ETC allows $V_{\text{STOR}}$ to obtain voltage levels in the range:

$$\frac{R_{\text{TOTAL}}}{R_{\text{EXT2}} + R_{\text{EXT3}}} V_{\text{PM}} > V_{\text{STOR}} > \frac{R_{\text{TOTAL}}}{R_{\text{EXT3}}} V_{\text{PM}},$$

(12)

where $R_{\text{TOTAL}} = R_{\text{EXT1}} + R_{\text{EXT2}} + R_{\text{EXT3}}$, and $V_{\text{PM}}$ is internally generated reference voltage connected to $V_{\text{REFH}}$ in Fig. 10(a). Hysteresis comparators inside ETC continuously monitor threshold voltage levels against $V_{\text{PM}}$ and generate controls for the SR-latch. An external enable switch activates ETC when needed. Along with the condition specified in equation (12), $V_{\text{STOR}}$ must be higher than $V_{\text{OUT}}$ to transfer energy from $C_{\text{STOR}}$ to $C_{\text{OUT}}$. Switch MOSFET $S_5$ prevents energy leakage from $C_{\text{OUT}}$.

**IV. MEASUREMENT RESULTS**

Proposed harvesting interface system is designed and fabricated in 180 nm CMOS technology with total of 0.28 mm$^2$ active area. Die micrograph of the fabricated chip is shown in Fig. 12. E-SSHI circuit occupies 300 $\times$ 400 $\mu$m$^2$ whereas voltage reference takes up 230 $\times$ 50 $\mu$m$^2$. Low-dropout (LDO) regulator and ETC use 500 $\times$ 56 $\mu$m$^2$ and 270 $\times$ 110 $\mu$m$^2$, respectively. Fig. 13 illustrates the experimental setup employed to validate the fabricated chips. A conventional piezoelectric harvester V22BL from MIDE company with 4.66 nF inherent capacitance ($C_{\text{PZ}}$) has been set onto a shaker table. This harvester included two electrically detached piezoelectric layers which were connected in series to enhance PEH voltage output during the experiments. PEH was excited periodically at 208 Hz resonance frequency in the vibration setup, which comprised of a test PCB, a shaker table, an amplifier, a controller, vibration software, and an oscilloscope. Acceleration of the shaker table was selected between 0.13 g and 0.53 g which corresponded to piezoelectric open circuit voltage amplitudes ($V_{\text{OC}}$) of 0.87 V and 3.6 V, respectively. Five SMD inductors with inductances 68 $\mu$H ($R_{\text{DC}} = 3.86$ $\Omega$), 330 $\mu$H ($R_{\text{DC}} = 1.93$ $\Omega$), 470 $\mu$H ($R_{\text{DC}} = 1.35$ $\Omega$), 680 $\mu$H ($R_{\text{DC}} = 2.02$ $\Omega$), and 820 $\mu$H ($R_{\text{DC}} = 2.53$ $\Omega$) have been utilized as $L_{\text{EXT}}$ for voltage flipping purposes.

Measured start-up operation is presented in Fig. 14. During start-up, $C_{\text{STOR}} = 449$ nF is charged passively through $S_1$ and $S_2$. Trigger circuit in Fig. 7 initiates E-SSHI phases.
when adequate charge accumulates on $C_{STOR}$. This voltage level corresponds to $V_{STOR} = 1.24$ V in Fig. 14. NVC free E-SSHI operation accelerates charging of $C_{STOR}$ significantly compared to passive charging. Fig. 15(a) depicts measured charging of $C_{STOR}$ with E-SSHI technique while Fig. 15(b) and 15(c) illustrate negative and positive voltage flipping operations, respectively. CFDs inside E-SSHI make it possible to attain optimum charge flipping without any external calibration. The system utilizes low-profile external inductors to obtain similar voltage flipping efficiency to conventional SSSI circuits with bulky external components [14], [17], [23]. Validation of energy transfer circuit (ETC) operation is depicted in Fig. 16. ETC regulates average $V_{STOR}$ to be about its optimum value $V_{STOR,OPT} \approx 2.68$ V for peak piezoelectric open circuit voltage of 1.31 V, while transferring energy from $C_{STOR} = 449 \text{nF}$ to $C_{OUT} = 2.2 \mu \text{F}$. Maximum and minimum voltage levels that $V_{STOR}$ can take is alterable via external resistors $R_{EXT1}$, $R_{EXT2}$, and $R_{EXT3}$ in Fig. 11.

Fig. 17 and Fig. 18 provide measured output power of E-SSHI operation under $V_{OC,P} = 0.87$ V and $V_{OC,P} = 2.6$ V peak piezoelectric open circuit voltage excitation levels, respectively. While $L_{EXT} = 820 \mu \text{H}$ is utilized, E-SSHI circuit is able to deliver a maximum of 3.84 $\mu \text{W}$ power to the load whereas on-chip full bridge rectifier (FBR) provides 0.62 $\mu \text{W}$ and ideal FBR can theoretically output a maximum of 0.734 $\mu \text{W}$. Ideal FBR can be delineated as a rectifier (without voltage drop across its diodes) which is able to provide theoretical maximum output power of $P_{\text{IDEAL-FBR}} = f_{EX} C_{PZ} V_{OC,P}^2$ [11], [14]. Fig. 17 illustrates that E-SSHI realizes 5.23 and 6.19 times relative output.
power performance over harvested power of an ideal FBR and on-chip FBR, respectively. It is possible to shrink $L_{EXT}$ inductance value down to 68 $\mu$H, which has small footprint (18 mm$^3$), in exchange for reduction in power extraction improvement. Relative power extraction improvement reduces while piezoelectric open circuit voltage increases, because damping of PEH strengthens with increased excitation levels (Fig. 18) [26]. Under high excitation, interface circuit suffers from elevated conduction and switching losses. Fig. 19 depicts output power of E-SSHI circuit under various piezoelectric excitation levels ($V_{OC,P}$) while $V_{STOR}$ is kept constant at 3.3 V. As observed in the plot, increased external inductance does not always enhance output power. Each inductor offers different voltage flipping efficiency, which leads to different optimum storage voltage value ($V_{STOR,OPT}$). Measured voltage flipping efficiencies ($\eta_F$) under different excitations are plotted in Fig. 20. Maximum $\eta_F = 93\%$ is observed for $L_{EXT} = 820$ $\mu$H at $V_{OC,P} = 3.6$ V. Even when $L_{EXT}$ is decreased down to 68 $\mu$H, E-SSHI still manages to grant maximum $\eta_F$ of 86% recorded at $V_{OC,P} = 2.6$ V.

Table 1 presents a performance comparison of E-SSHI proposed in this work against state-of-the-art PEH interface circuits in the literature. E-SSHI stands out among its peers in terms of fully autonomous charge flipping and area efficient design. Furthermore, it achieves flipping efficiencies comparable to conventional SSHI circuits [15]–[17] even with low-profile inductors under 1 mH. SECE based interface circuit in [12] was designed specifically for shock type excitations and its performance under periodic excitations is inferior with respect to E-SSHI. Recently, partial electric charge extraction (PECE) technique similar to SECE has been proposed in [13]. It focuses on extracting energy from PEH generating irregular high voltage outputs. In this circuit, AC/DC conversion was attained using conventional off-chip FBR that limited power extraction improvement. Circuit in [16] employed a bulky external inductor to accomplish a conventional SSHI interface that is able to extract energy from both periodic and shock excitations; however, it is not convenient for a miniaturized systems. Perturb and observe (P&O) maximum power point tracking (MPPT) method was integrated inside a conventional SSHI by Li et al. [17]. A complex control unit was required in this design and measured performance parameters fall behind E-SSHI circuit presented in this work. Peng [24] proposed a novel harvesting
interface called sense-and-set (SaS) rectifier which continuously monitors PEH’s charge generation and tries to keep battery voltage at optimum. Due to technology limitation, SaS circuit stops tracking optimum point after battery voltage passes 2 V. In addition, 1 mH external inductor increases system volume. Inductorless designs presented in [20], [21] integrates flipping capacitors on-chip which is a huge step towards miniaturization. Nonetheless, both interface circuits were designed for particular applications and harvesters: Flipping-capacitor rectifier (FCR) in [20] works with PEH inherent capacitances in pF range, and split-electrode synchronized switch harvesting on capacitor (SE-SSHC) utilizes custom MEMS harvester having four identical electrodes with equal capacitances and resonance frequencies. Area efficient E-SSHI circuit’s ability to operate with low-profile external inductor reduces system volume and cost and leads the way towards miniaturization. Unlike conventional SSHI methods and inductorless designs, autonomous operation phases eliminate external intervention for obtaining optimum voltage flipping moments.

V. CONCLUSION

In this paper, an autonomous low-profile SSHI based piezoelectric energy harvesting interface circuit has been proposed. Both optimum voltage flipping and energy transfer to the output load have been achieved autonomously by charge flipping and reverse current detectors. Since E-SSHI does not contain any negative voltage converter, it occupies less chip area than its counterparts. Energy transfer circuit is capable of transferring energy from E-SSHI output to electronic load to keep storage voltage at its optimum value. Proposed harvesting interface has been fabricated in 180 nm CMOS process and occupies 0.28 mm², which is smaller than other circuits in the literature. A maximum of 5.23 times relative performance improvement over ideal FBR is achieved by E-SSHI circuit. 93% voltage flipping efficiency has been measured for low-profile \( L_{EXT} = 820 \mu H \) at \( V_{OC,p} = 3.6 \) V. This work exhibits power improvement over conventional methods and offers a compact harvesting system for PEHs with several nF capacitance range.

REFERENCES

[1] R. J. M. Vullers, R. V. Schajik, H. J. Visser, J. Penders, and C. V. Hoof, “Energy harvesting for autonomous wireless sensor networks,” *IEEE Solid State Circuits Mag.*, vol. 2, no. 2, pp. 29–38, Feb. 2010.

[2] P. D. Mitcheson, E. M. Yeatman, G. K. Rao, A. S. Holmes, and T. C. Green, “Energy harvesting from human and machine motion for wireless electronic devices,” *Proc. IEEE*, vol. 96, no. 9, pp. 1457–1486, Sep. 2008.

[3] F. Dell’Anna, T. Dong, P. Li, Y. Wen, Z. Yang, M. R. Casu, M. Azadmehr, and Y. Berg, “State-of-the-art power management circuits for piezoelectric energy harvesters,” *IEEE Circuits Syst. Mag.*, vol. 18, no. 3, pp. 27–48, 3rd Quart., 2018.

[4] T. Hehn, F. Hagedorn, D. Maurath, D. Marinkovic, I. Kuehne, A. Frey, and Y. Manoli, “A fully autonomous integrated interface circuit for piezoelectric harvesters,” *IEEE J. Solid-State Circuits, vol. 47, no. 9, pp. 2185–2198, Sep. 2012.*

[5] S. Chamanian, H. Ulusan, A. Koyuncuoğlu, A. Muhtaroğlu, and H. Külah, “An adaptable interface circuit with multi-stage energy extraction for low power piezoelectric energy harvesting MEMS,” *IEEE J. Solid-State Circuits, vol. 49, no. 10, pp. 2277–2291, Oct. 2014.*

[6] T. T. Le, J. Han, A. Von Jouanne, K. Mayaram, and T. S. Fiez, “Piezoelectric micro-power generation interface circuits,” *IEEE J. Solid-State Circuits, vol. 41, no. 6, pp. 1411–1419, May 2006.*

[7] Y. Kushino and H. Koizumi, “Piezoelectric energy harvesting circuit using full-wave voltage doubler rectifier and switched inductor,” in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2014, pp. 2310–2315.

[8] N. Kong and D. S. Ha, “Low-power design of a self-powered piezoelectric energy harvesting system,” *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2739–2747, Mar. 2012.

[9] J. Dicken, P. D. Mitcheson, I. Stoianov, and E. M. Yeatman, “Power-extraction circuits for piezoelectric energy harvesters in miniature and low-power applications,” *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4514–4529, Nov. 2012.

[10] D. Kwon and G. A. Rincón-Mora, “A single-inductor 0.35 µm CMOS energy-investing piezoelectric harvester,” *IEEE J. Solid-State Circuits, vol. 49, no. 10, pp. 2277–2291, Oct. 2014.*
[12] D. Morel, A. Quelen, P. Gasnier, R. Gréaud, S. Monfray, A. Badel, and G. Pillonnet, “A shock-optimized SECE integrated circuit,” *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3420–3433, Dec. 2018.

[13] M. B. Khan, H. Saif, and Y. Lee, “A piezoelectric energy harvesting interface for irregular high voltage input with partial electric charge extraction with 3.9× extraction improvement,” in *Proc. IEEE Asian Solid State Circuits Conf. (A-SSCC)*, Nov. 2019, pp. 181–184.

[14] Y. K. Ramadass and A. P. Chandrakasan, “An efficient piezoelectric energy harvesting interface circuit using a bias-flip rectifier and shared inductor,” *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 189–204, Jan. 2010.

[15] E. E. Aktakka and K. Najafi, “A micro inertial energy harvesting platform with self-supplied power management circuit for autonomous wireless sensor nodes,” *IEEE J. Solid-State Circuits*, vol. 49, no. 9, pp. 2017–2029, Sep. 2014.

[16] D. A. Sanchez, J. Leicht, E. Jodka, E. Fazel, and Y. Manoli, “A 4.78W-to-1 mW parallel-SSHI rectifier for piezoelectric energy harvesting of periodic and shock excitations with inductor sharing, cold start-up and up to 681% power extraction improvement,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC)* Dig. Tech. Papers, Jan. 2016, pp. 366–367.

[17] S. Li, A. Roy, and B. H. Calhoun, “A piezoelectric energy harvesting system with parallel-SSHI rectifier and integrated MPPT achieving 417% energy-extraction improvement and 97% tracking efficiency,” in *Proc. Symp. VLSI Circuits*, Jun. 2019, pp. 324–325.

[18] L. Wu, X.-D. Do, S.-G. Lee, and D. S. Ha, “A self-powered and optimal SSCH circuit integrated with an active rectifier for piezoelectric energy harvesting,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 3, pp. 537–549, Mar. 2017.

[19] S. Du and A. A. Seshia, “An inductorless bias-flip rectifier for piezoelectric energy harvesting,” *IEEE J. Solid-State Circuits*, vol. 52, no. 10, pp. 2746–2757, Oct. 2017.

[20] Z. Chen, M.-K. Law, P.-I. Mak, W.-H. Ki, and R. P. Martins, “A 22×1.7 nm inductorless fully integrated flapping-capsitor rectifier (FCR) for piezoelectric energy harvesting with 483% power-extraction enhancement,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC)* Dig. Tech. Papers, Feb. 2017, pp. 372–373.

[21] S. Du, Y. Ji, C. Zhao, G. A. J. Amarutanga, and A. A. Seshia, “A fully integrated split-electrode SSHC rectifier for piezoelectric energy harvesting,” *IEEE J. Solid-State Circuits*, vol. 54, no. 6, pp. 1733–1743, Jun. 2019.

[22] P. Angelov and M. Nielsen-Lonn, “A fully integrated multilevel synchronized-switch-harvesting-on-capacitors interface for generic PEHs,” *IEEE J. Solid-State Circuits*, vol. 55, no. 8, pp. 2118–2128, Aug. 2020.

[23] D. A. Sanchez, J. Leicht, F. Hagedorn, E. Jodka, E. Fazel, and Y. Manoli, “A parallel-SSHI rectifier for piezoelectric energy harvesting of periodic and shock excitations,” *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2867–2879, Dec. 2016.

[24] Y. Peng, K. D. Choo, S. Oh, I. Lee, T. Jang, Y. Kim, J. Lim, D. Blaauw, and D. Sylvester, “An efficient piezoelectric energy harvesting interface circuit using a sense-and-set rectifier,” *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3348–3361, Dec. 2019.

[25] B. Ciftci, S. Chamanian, A. Koyuncuoglu, A. Muhtaroglu, and H. Kulah, “Low-profile autonomous interface circuit for piezoelectric micro-power generators,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 4, pp. 1458–1471, Apr. 2021.

[26] S. Chamanian, A. Muhtaroglu, and H. Kulah, “A self-adapting synchronized-switch interface circuit for piezoelectric energy harvesters,” *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 901–912, Jan. 2020.