Switching ferroelectricity in SnSe across diffusionless martensitic phase transition

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We experimentally investigate transport properties of a hybrid structure, which consists of a thin single crystal SnSe flake on a top of 5 μm spaced Au leads. The structure initially is in highly-conductive state, while it can be switched to low-conductive one at high currents due to the Joule heating of the sample, which should be identified as α-Pnma – β-Cmcm diffusionless martensitic phase transition in SnSe. For highly-conductive state, there is significant hysteresis in $dI/dV(V)$ curves at low biases, so the sample conductance depends on the sign of the applied bias change. This hysteretic behavior reflects slow relaxation due to additional polarization current in the ferroelectric SnSe phase, which we confirm by direct measurement of time-dependent relaxation curves. In contrast, we observe no noticeable relaxation or low-bias hysteresis for the quenched β-Cmcm low-conductive phase. Thus, ferroelectric behavior can be switched on or off in transport through hybrid SnSe structure by controllable α-Pnma – β-Cmcm phase transition. This result can also be important for nonvolatile memory development, e.g. phase change memory for neuromorphic computations or other applications in artificial intelligence and modern electronics.

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I. INTRODUCTION

Recent interest to chalcogenides is connected with their electronic, thermal and optical properties. For pure science, topological semimetals can be realized as three-dimensional single chalcogenides crystals. Also, they are usually considered as a platform for creating modern two-dimensional materials, due to the layered structure and high carrier mobility. For applications, they are mostly regarded for photodetectors, phototransistors or different photovoltaic devices. They also demonstrate thermoelectricity, piezoelectricity and ferroelectricity even at room temperature.

Ferroelectric properties of different chalcogenides are of great interest due to the underlying physics and potential applications. Recently, three-dimensional WTe$_2$ single crystals were found to demonstrate coexistence of metallic conductivity and ferroelectricity at room temperature. Out-of-plane spontaneous polarization of ferroelectric domains is found to be bistable, it can be affected by high external electric field. Also, in-plane ferroelectric polarization has been also demonstrated for layered SnSe monochalcogenide.

Ferroelectric properties are unambiguously connected with crystal symmetry. Monochalcogenides are often centrosymmetric in the bulk but lack inversion symmetry in single-layer or few-layer forms. On the other hand, crystal structure is subjected to modification in monochalcogenides across phase transition. For example, layered SnSe exhibits a low degree of lattice symmetry, with a distorted NaCl structure and an in-plane anisotropy. It belongs to orthorhombic α-Pnma phase at room temperature, which can be converted into the symmetric β-Cmcm phase at moderate temperatures. This transition should seriously affect, in particular, spontaneous ferroelectric polarization. Thus, correlation between the ferroelectric properties and crystal symmetry can be experimentally studied in chalcogenides, being also important for nonvolatile memory investigations, e.g. for phase change memory for neuromorphic computations or other applications in artificial intelligence and modern electronics.

Here, we experimentally investigate transport properties of a hybrid structure, which consists of a thin single crystal SnSe flake on a top of 5 μm spaced Au leads. The structure initially is in highly-conductive state, while it can be switched to low-conductive one at high currents due to the Joule heating of the sample, which should be identified as α-Pnma – β-Cmcm phase transition in SnSe. For highly-conductive state, there is significant hysteresis in $dI/dV(V)$ curves at low biases, so the sample conductance depends on the sign of the applied bias change. This hysteretic behavior reflects slow relaxation due to additional polarization current in the ferroelectric SnSe phase, which we confirm by direct measurement of time-dependent relaxation curves. In contrast, we observe no noticeable relaxation or low-bias hysteresis for the quenched β-Cmcm low-conductive phase. Thus, ferroelectric behavior can be switched on or off in transport through hybrid SnSe structure by controllable α-Pnma – β-Cmcm phase transition. This result can also be important for nonvolatile memory development.

II. SAMPLES AND TECHNIQUES

SnSe compound was synthesized by reaction of selenium vapors with the melt of high-purity tin in evacuated silica ampoules. X-ray diffraction pattern is shown in Fig. 1 (a). It confirms single-phase SnSe with orthorhombic crystal system (Pnma(62) space group, $a = 11.502(6)$ Å, $b = 4.153$ Å, and $c = 4.450$ Å). The SnSe...
single crystals with diameter 20 mm and length 80 mm were grown by vertical zone melting in silica crucibles under argon pressure. The inset to Fig. 1(a) demonstrates the Laue x-ray diffraction pattern of SnSe single crystal, the x-ray direction is perpendicular to the exfoliated planes with zone axis [100]. (b) Optical image of a sample. SnSe flake is placed over 100 nm thick Au leads, the leads profile can be seen under the ultra-thin SnSe flake (below 100 nm) flake. The relevant (bottom) SnSe surface is protected from any oxidation or contamination by SiO$_2$ substrate. The leads C1, C2, C3, C4 are separated by 5 µm intervals, they are used for two- and four-point electrical measurements, see the main text.

III. EXPERIMENTAL RESULTS

Fig. 2 shows the examples of two-point $dI/dV(V)$ curves for typical 100 kΩ sample. Differential conductance $dI/dV$ non-linearly increases for positive and negative bias voltages in Fig. 2(a). In addition, we observe significant hysteresis with bias sweep direction, which somewhat analogous to the previously reported for the ferroelectric chalcogenide WTe$_2$: for opposite voltage sweep directions, there is noticeable discrepancy between the curves within the ±1 V range. It is important, that $dI/dV(V)$ curves coincide perfectly in Fig. 2(a) if they are obtained for the same sweep direction, see red and blue or pink and green curves, respectively. Also, $dI/dV$ differential conductance is excellently stable at ±3 V, which are the boundaries of the voltage sweep range. Thus, the observed hysteresis can not be ascribed
Figure 2. (a-c) Two-point \(\frac{dI}{dV}(V)\) curves for typical 100 kOhm sample, arrows indicate sweep directions for the curves of the same colors. The curves coincide perfectly for the same sweep direction in (a), while there is noticeable hysteresis within the ±1 V range for opposite ones. Also, \(\frac{dI}{dV}\) differential conductance is excellently stable at ±3 V, which are the boundaries of the voltage sweep range. The sweep rate is diminishing from (a) to (c): the curves in (a) are obtained for 3 min sweep for the ±3 V range, it takes 100 min and 600 min for curves in (b) and (c), respectively. The hysteresis amplitude dependence on the sweep rate reflects some slow relaxation process. (d) Time-dependent relaxation \(\frac{dI}{dV}(t)\) at zero bias. The sample is kept at a fixed dwelling voltage (+3 V or -3 V) for 10 min, voltage bias is abruptly set to zero value afterward. \(\frac{dI}{dV}(V = 0)\) values are clearly different for the dwelling voltages of opposite signs.

to any artificial drifts, etc., and is defined by the sweep direction.

The hysteresis amplitude depends on the sweep rate, see Fig. 2 (a-c), so it reflects some slow relaxation process. The latter can be demonstrated by direct relaxation measurements in Fig. 2 (d). To obtain \(\frac{dI}{dV}(t)\) curves, the sample is kept at a fixed dwelling voltage (+3 V or -3 V) for 10 min, voltage bias is abruptly set to zero value afterward. The time-dependence of \(\frac{dI}{dV}(V = 0)\) is recorded, which demonstrates slow relaxation for significant time interval. However, \(\frac{dI}{dV}(t)\) curves show clearly different \(\frac{dI}{dV}(V = 0)\) values for the dwelling voltages of opposite signs, which confirms finite hysteresis amplitude for the lowest sweep rate in Fig. 2 (c).

To our surprise, the described above behavior can be controllably switched off or on by applying voltage bias above some threshold value, see Fig. 3. In a slow voltage sweep from zero to high negative values in Fig. 3 (a) (the red curve), differential conductance \(\frac{dI}{dV}(V)\) falls down in two orders of magnitude at approximately ≈-12 V. This step-like conductance jump is found to be reversible, \(\frac{dI}{dV}\) level is recovered for slow backward bias sweep, although with some voltage delay (at ≈10 V), see the left part of Fig. 3 (a) (the green curve). While continuing sweep from zero to positive biases, \(\frac{dI}{dV}(V)\) also falls down at ≈+12 V in the right part of Fig. 3 (a), so the threshold voltage is approximately the same for both bias polarities. Thus, it seems to be controlled by bias amplitude (e.g., due to local Joule heating) but not the electric field direction.

For backward sweep from the high biases, the low-conductive state can either be preserved down to the zero bias value, see Fig. 3 (b). In this case, there is no hysteresis in the narrow bias range, see Fig. 3 (c). \(\frac{dI}{dV}(V)\) curves are flat and independent of the voltage sweep direction, in contrast to ones in Fig. 2. Also, no relaxation can be observed for the "quenched" low-conductive state, as demonstrated by the blue curve in Fig. 3 (d). This "quenched" zero-bias state is not stable, it can be switched back to the highly-conductive one by moderate biases, as depicted in the right part of Fig. 3 (b).

We wish to mention the clearly visible noise in experimental curves in Fig. 2 (a-c) and and Fig. 3 (c). The noise level is minimal at zero bias, it is obviously increasing with \(\frac{dI}{dV}\) signal amplitude. The noise fluctuations are nearly reproducible for the curves, which are recorded in the same sweep direction. This behavior is just opposite to the expected for external electrical noise. It reflects some bias-dependent conductance fluctuations, which can be expected for ultra-thin flakes.

Similar \(\frac{dI}{dV}(V)\) behavior can be demonstrated for different samples, e.g. with much higher (≈10 kOhm) initial zero-bias conductance in Fig. 4 (a). Two-point \(\frac{dI}{dV}(V)\) increases non-linearly at positive and negative bias voltages, there is noticeable hysteresis with the sweep direction, the noise level is increasing with \(\frac{dI}{dV}\) signal amplitude. The relaxation \(\frac{dI}{dV}(t)\) curves also confirm slow relaxation process with two different \(\frac{dI}{dV}(V = 0)\) resistance states for the dwelling voltages of opposite signs in Fig. 4 (b).

10 kOhm samples also allow to directly define current \(I\) in the circuit, therefore, to measure the resulting voltage drop \(V\) both in two-point and four-point techniques. For the two-point connection scheme, \(dV/dI(t)\) curves of sample differential resistance are presented in Fig. 4 (a) for two current sweep directions. These curves are just inverted in respect to ones in Fig. 2 (a), they demonstrate the same hysteretic behavior, which is confirmed by \(dV/dI(t)\) relaxation curves in Fig. 4 (b).

\(dV/dI(t)\) behavior is drastically different in the four-point connection scheme, see Fig. 4 (c). The bulk SnSe differential resistance demonstrates no hysteresis, the general \(dV/dI(t)\) behavior is obviously different from one...
for the "quenched" low-conductive state (blue curve), in con-
verses for $dI/dV$ sweep directions for $dI/dV$.

Figure 3. (a-b) Switching between highly- and low-
conductive states of the sample, which we identify as $\alpha-Pnma$ – $\beta-Cmcm$ phase transition in SnSe. The arrows indicate sweep directions for $dI/dV(V)$ curves. (a) Differential con-
ductance $dI/dV$ falls down in two orders of magnitude at $\approx 12$ V. $dI/dV$ level is recovered for slow backward bias sweep at $\approx 10$ V, i.e. with some voltage delay. $dI/dV(V)$ also falls down at $\approx 12$ V, so the threshold voltage is approxi-
ately the same for both bias polarities. (b) The low-
conductive state can be preserved ("quenched") down to zero bias. (c) There is no hysteresis for the "quenched" low-
conductive state, $dI/dV(V)$ curves are independent of the voltage sweep direction. (d) No relaxation can be observed for the "quenched" low-conductive state (blue curve), in con-
trast to the pronounced relaxation from the highly-conductive one (red curve).

in Fig. 5 (a), while the conductance fluctuations are still increasing with the current bias, maybe, due to the local heating of the bulk SnSe region. Since the contacts are excluded for the four-point measurements, we have to conclude that the results in Figs. 2 3 4 originate from the Au-SnSe contacts’ areas.

Figure 5. $dV/dI(I)$ curves for the sample from Fig. 4 obtained both in two-point (a) and four-point (c) techniques. In this case, $I$ is defined and ac voltage drop $\sim dV/dI$ is mea-
sured. (a) Two-point curves are just inverted in respect to ones in Fig. 4 (a), they demonstrate the same hysteretic behavior, which is confirmed by slow $dV/dI(t)$ relaxation curves in (b). (c) Four-point curves $dV/dI(I)$ reflect the bulk SnSe differential resistance. They demonstrate no hysteresis, the general $dV/dI(I)$ behavior is obviously different from the two-
point one in (a). Thus, slow relaxation in (b) and consequent hysteresis in (a) originate from the Au-SnSe contacts’ areas.

IV. DISCUSSION

As a result, we demonstrate two different, highly- and low-conductive SnSe states. The highly-conductive one exists at low biases, it is characterized by noticeable hysteretic behavior with bias sweep direction. This state can be switched to the low-conductive one, the conductance jump is sharp and can be achieved for both bias signs. No hysteresis can be observed at low biases in the low-
conductive state.
SnSe is a typical layered narrow-gap chalcogenide\textsuperscript{18,20,36}, the initial state is orthorhombic $\alpha$-Pnma phase. In this state, SnSe is characterized by p-type conductivity\textsuperscript{34}, defined by intrinsic vacancies\textsuperscript{35}. Two-point $dI/dV(V)$ curves reflect the electrochemical potential shift at the Au-SnSe interfaces\textsuperscript{31}, which leads to nearly symmetric $dI/dV$ increase for both bias signs in Figs.\textsuperscript{2} (a) and 5 (a). In contrast, there is only negligible $dV/dI(t)$ dependence for the four-point curves in Fig. 2 (b) with excluded Au-SnSe interfaces.

For SnSe, there is well known martensitic type phase transition\textsuperscript{32} from initial low-symmetric $\alpha$-Pnma phase to the highly-symmetric $\beta$-Cmcm one, which occurs at 750-800 K\textsuperscript{33}. This temperature can be achieved locally in our setup at high currents, which we have tested by decomposition of black phosphorus flakes in similar experimental geometry\textsuperscript{31}. Sharp conductance change is a known fingerprint of martensitic type phase transitions\textsuperscript{32}, e.g. it occurs due to the charge density wave formation in layered semiconductors\textsuperscript{37-39}. More generally, charge density wave formation accompany any diffusionless phase transition, which is characterized by symmetry change and intrinsic strain. Conductivity falls down at the transition due to the charge density wave pinning by stress, impurities or defects. Also, the high temperature phase can be quenched at room temperature because of the non-thermoelastic character of the transition\textsuperscript{32}.

Thus, we can identify $\alpha$-Pnma – $\beta$-Cmcm phase transition by differential conductance jump in Fig. 3. From Fig. 3 (a), the conductance jumps can be observed for both bias polarities, which also confirms Joule heating origin of the effect. In this case, backward sweep of the bias leads to the quenching of the high-symmetric $\beta$-Cmcm phase down to zero bias. Since the quenched state is not stable, it can be destroyed by moderate heating, as depicted in Fig. 3 (b).

In general, hysteretic $dI/dV(V)$ behavior in Figs. 2 4 and 5 (a) is qualitatively analogous to ferroelectricity-induced one\textsuperscript{32} for another ferroelectric chalcogenide WTe$_2$.

Thin SnSe layers are characterized\textsuperscript{18} by in-plane spontaneous ferroelectric polarization at room temperatures. In this case, any variation of the source-drain bias leads to the additional polarization current due to the domain wall shift for varying electric field. Indeed, source-drain in-plain field $E_{sd} \sim V/d$ is induced by the voltage bias $V$, where $d = 5\mu$m is the separation between the Au leads. The achievable $E_{sd}$ values ($\sim 10^3$ V/m) are too small to align polarization of the whole SnSe flake, so $E_{sd}$ mostly affects the domain wall regions. Any variation of the domain wall positions lead to the additional polarization current. Since polarization current is connected with lattice deformation in ferroelectrics, we observe it as slow relaxation in $dI/dV$. In other words, the dc circuit of our experimental setup is equivalent to so called Sawyer-Tower’s circuit\textsuperscript{19,41}, so the difference between every two curves in Figs. 2 4 and 5 (a) represents a standard ferroelectric hysteresis loop.

In contrast to the bulk WTe$_2$ samples with broken inversion symmetry\textsuperscript{18}, ferroelectricity in SnSe is connected a low degree of lattice symmetry in thin layers\textsuperscript{17}. The critical thickness can be estimated\textsuperscript{22} as 200 nm for SnSe. We observe slow relaxation for ultra-thin\textsuperscript{20} flakes in planar experimental geometry, where electric field is mostly concentrated at the Au-SnSe interface. This is the reason not to observe $dI/dV(V)$ hysteresis in the four-point connection scheme for bulk SnSe resistance, see Fig. 4 (b). Also, polarization current is some addition to the ordinary one for the conductive samples, so the ferroelectric hysteresis loop is more pronounced for thinner (with higher resistance) samples, cp. in Figs. 2 and 4.

Ferroelectric properties are unambiguously connected with crystal symmetry\textsuperscript{18,19}, which can be utilized to confirm ferroelectric origin of the low-bias hysteresis. For example, gold adatom absorption at defects\textsuperscript{10} can not be sensitive to the crystal symmetry. We do not observe neither low-bias hysteresis (i.e. conductance dependence on the previously applied bias sign) nor slow relaxation in the quenched highly-symmetric $\beta$-Cmcm phase in Fig. 3 (c) and (d). Thus, relaxation can be switched on or off by controllable $\alpha$-Pnma – $\beta$-Cmcm phase transition in SnSe, which also confirms its ferroelectric origin. This result can also be important for nonvolatile memory development, e.g. phase change memory for neuromorphic computations or other applications in artificial intelligence and modern electronics.

V. CONCLUSION

As a conclusion, we experimentally investigate transport properties of a hybrid structure, which consists of a thin single crystal SnSe flake on a top of 5 $\mu$m spaced Au leads. The structure initially is in highly-conductive state, while it can be switched to low-conductive one at high currents due to the Joule heating of the sample, which should be identified as $\alpha$-Pnma – $\beta$-Cmcm phase transition in SnSe. For highly-conductive state, there is significant hysteresis in $dI/dV(V)$ curves at low biases, so the sample conductance depends on the sign of the applied bias change. This hysteretic behavior reflects slow relaxation due to additional polarization current in the ferroelectric SnSe phase, which we confirm by direct measurement of time-dependent relaxation curves. In contrast, we observe no noticeable relaxation or low-bias hysteresis for the quenched $\beta$-Cmcm low-conductive phase. Thus, ferroelectric behavior can be switched on or off in transport through hybrid SnSe structure by controllable $\alpha$-Pnma – $\beta$-Cmcm phase transition. This result can also be important for nonvolatile memory development.
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