A 110W 10Mb/s eTextiles transceiver for body area networks with remote battery power

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Additionally, by using dual capacitors $C_1$ and $C_2$ that are nominally discharged, this approach is advantageous, as capacitive-driving reduces output voltage medium with supply-rail-coupled (SRC) differential transmitters (Fig. 27.6.3). Time-sharing of the eTextiles medium with remote charging circuitry forces the external super capacitor, which functions as each node’s energy supply.

A block diagram of the proposed eTextiles transceiver SoC, used in both sensor nodes and the BS, is shown in Fig. 27.6.2. The two main inputs, $v_+$ and $v_-$, feed the RX front end (FE), and are the outputs of differential transmitters. Between packets, a fixed amount of time is allocated to activating transistors $M_1$ and $M_2$ on all sensor nodes and the BS, directly connecting $v_+$ and $v_-$ to the supply terminals of each chip. This permits the BS battery to remotely charge each node’s external super capacitor, which functions as each node’s energy supply.

Time-sharing of the eTextiles medium with remote charging circuitry forces the DC voltages on $v_+$ and $v_-$ to be at opposite rails at the beginning of packet communication. To save the energy otherwise required to completely charge and discharge the primarily capacitive medium, the DC voltages are held constant by high impedance resistors, and transmitted signals are AC coupled onto the medium with supply-rail-coupled (SRC) differential transmitters (Fig. 27.6.5). This approach is advantageous, as capacitive-driving reduces output voltage swing and driver load [6,7], irrespective of the network DC potential. Additionally, by using dual capacitors $C_1$ and $C_2$ that are nominally discharged and charged, respectively, a ternary signaling scheme can be used, simplifying capacitive divider ratio of $C_1$ and $C_L$. Asserting $p_{a[1]}$ would instead discharge $C_2$, producing a negative voltage swing on the output that is proportional to the capacitive divider ratio of $C_1$ and $C_2$. Asserting $p_{a[1]}$ would instead discharge $C_2$, generating a positive voltage swing. The opposite effects are arranged for TX, making the signaling scheme differential, yet operating at different DC levels. Both TX+ and TX- consist of 7 pairs of binary-weighted tri-state inverters and capacitive DACs to provide voltage swing configurability.

The RX FE samples and digitizes the SRC differential voltage across $v_+$ and $v_-$ using 4 time offset acquisition (AO) blocks (Fig. 27.6.4). An SRC common-mode independent sampling structure is implemented, exploiting the fact that $v_+$ and $v_-$ have DC potentials at opposite rails. Before packet reception, the sampling capacitors are purged. During the preset phase, the capacitors are charged to the supply rails; since the top plates are floating, their potentials settle to mid-rail. During sampling, the bottom capacitor plates are connected to the eTextiles network. As the inputs are already centered at opposite DC potentials and the top plates remain floating, only differential charge is sampled on top of the existing mid-rail charge residing on each capacitor. As a result, during the hold phase, the inputs to the comparators are differentially centered at mid-rail, requiring no additional biasing and reducing the CMRR requirements of the ensuing comparators.

Samples are converted to ternary digits (trits) by two clocked comparators sized for a 3σ offset under 25mV. Each comparator has 8 bits of differential pair and current source weighting, providing offsets that vary by ±60mV. The comparators are configured to have equal and opposite zero-offsets, such that any differential samples above or below the absolute offset level convert to trits ‘+1’ or ‘-1’, respectively; samples residing between the offset levels convert to ‘0’. The conversion is performed by an offset orientation-independent ternary encoder, permitting the comparator pair to swap roles. After calibration, this form of comparator configuration-redundancy improves the $\sigma$ of offset errors, measured as the difference between the desired and attained offset for each comparator, by 1.5-2.5X.

Each sample and conversion operation completes in two clock cycles, requiring two interleaved AO blocks to demodulate data at full rate. Synchronization is achieved in the RX back end (BE) by correlating incoming data using two additional AO blocks to ensure sampling occurs every half clock period (Fig. 27.6.5). A custom multiplier is implemented for the correlator ternary arithmetic, saving 2 bits in each adder stage over a traditional 2’s complement topology. If a correlator output crosses a programmable threshold, synchronization is achieved, and the two unused AO blocks are clock gated. Alternatively, the RX BE can be configured in an auto-correlation mode for a CSMA MAC.

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Shared eTextiles communication and power delivery medium

Basestation prototype (eTextiles transceiver & wireless relay)

Packet Diagram:

Beacon Req. PKT Node ID = BS TX / Node RX
= BS RX / Node TX
= No RX/TX

Payload Charge

eTextile nodes

Figure 27.6.1: Implemented eTextiles system with packet diagram shown.

Figure 27.6.2: eTextiles transceiver block diagram used for sensor nodes. The BS uses the same chip, but replaces the super capacitor with a battery.

Figure 27.6.3: Supply-rail-coupled (SRC) differential ternary transmitter.

TX+ (6:0)

TX- (6:0)

V+
V+
V DD
GND
V-
V-

Figure 27.6.4: RX front end (FE) consisting of four time-offset acquisition (AQ) blocks.

Figure 27.6.5: RX back end (BE) used for synchronization.

Figure 27.6.6: Measured transient waveforms and table of measured results.

Chip Summary

| [1] | [2] | [3] | [4] | [5] |
|-----|-----|-----|-----|-----|
| Work | Technology | Freq | Power | Data |
|      | 0.18µm | 100MHz | 0.11mW | 0.157mW |
|      | 0.83mm² | 2.7mW  | 2.7pJ  | 77pJ   |
|      | 2.7mW  | 68pJ  | 2.7pJ  | 77pJ   |

Figure 27.6.7: Chip summary of the eTextiles system.
Figure 27.6.7: Die photograph of the eTextiles transceiver.