A broadband high bandwidth utilization ECL static frequency divider in InP DHBT process

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Abstract This letter presents a broadband 2:1 static ECL frequency divider in a 0.8 μm InP DHBT process. The proposed divider is based on an ECL double emitter-followers structure. The maximum cut-off frequency \( f_t \) utilization of the device is improved up to 0.967 through theoretical analysis and calculation. The measurement shows that the divider can operate with input frequency from 1 GHz to 62 GHz in sinusoidal waveform, while the maximum \( f_t \) of the device is 150 GHz. Bandwidth utilization \( BW/f_t \) is 0.413, which is an extremely high value for InP devices at the same size.

Keywords: ECL static frequency divider, InP DHBT

Classification: Microwave and millimeter-wave devices, circuits, and modules

1. Introduction

High speed and wide-band frequency dividers are widely used in quadrature signal generation \([1, 2]\), time-interleaved THA and ADC systems \([3, 4, 5]\), and other high-speed communication fields \([6]\). A number of dividers based on different topologies and processes have been reported so far. Particularly, InP DHBT has a higher breakdown voltage and better frequency performance for devices at the same size \([7, 8]\), which means InP DHBT is a better choice for high-speed divider circuits. However, the operating frequency range of the circuit does not surpass a fraction of the cut-off frequency \( f_t \) related to the device process \([9]\), which limits the operating frequency of current-mode logic (CML) dividers \([9, 10]\). In order to improve the high-frequency performance of the divider circuit, efforts should be made to increase the utilization of operating frequency for devices with the same \( f_t \).

Numerous enhancement techniques have been published to extend the operating frequency range of frequency dividers, such as inductive peaking \([9, 11, 12, 13]\), split-resistor loading \([14, 15, 16]\), asymmetric latch \([17]\), dynamic frequency divider \([18, 19, 20, 21, 22]\) and double emitter-followers \([23, 24]\). However, maximum utilization of the device \( f_t \) for the circuit design is few reported. This letter presents an emitter-coupled logic (ECL) \([25, 26, 27]\) static frequency divider based on ECL master-slave latches configuration in 0.8 μm InP DHBT process. In order to improve the operating frequency of the divider, the relationship between device operating voltage and utilization of \( f_t \) was analyzed.

Using a single-ended input clock signal, two 50 GHz cables, and two 50 GHz probes, the ECL divider was measured to operate from 1 GHz to 62 GHz. For input frequencies near the input referred self-oscillation frequency (SOF) \([11, 24, 28, 29]\), the divider operates at the lowest input power level, which equals \(-70\) dBm. The output power range of the divider is from \(-6.3\) dBm to 0.5 dBm. The bandwidth utilization \( BW/f_t \) \([30]\) is 0.413, which is better than circuits fabricated with the same size device.

2. Design of the ECL divider

As shown in Fig. 1, the ECL divider consists of input buffer, ECL divider core, and output buffer. The ECL divider core contains two ECL latches which are powered by \(-2.5\) V and \(-3.5\) V. Two buffers are only powered by \(-2.5\) V. The output of the second ECL latch \((Q_n, Q_{n-1})\) is reversely connected to the input of the first ECL latch \((D, D_n)\), which provides a phase shift of 180°.

![Fig. 1 Block diagram of proposed ECL static frequency divider.](image)

2.1 Input buffer of the ECL divider

Input buffer is shown in Fig. 2. Such topology is able to convert a single-ended input clock signal into a differential signal and affect the \( f_t \) utilization of devices through the double emitter followers. The emitter area of the transistors in the input buffer is 0.8 μm\( \times 7.0\) μm.

2.2 ECL core and output buffer of the divider

The top of Fig. 3 is the output buffer of the ECL divider. To
reduce the effect of differential output cables on insertion loss, signal amplitude shifting errors, phase offset, and facilitate testing, the divider uses only one input port and one output port, rather than traditional dual ports in practical applications. The output port OUT is connected to an external termination of 50 Ω and its output load is also 50 Ω. As a result, half of the output power is lost compared to another 50 Ω port of the differential pair. For the balance of the differential pair’s operation, two load resistances seen from the transistors are usually set equal.

The ECL master-slave latches are the core of ECL divider. $I_p$ and $I_n$ are connected to the output of input buffer. In Fig. 3, there are four switching transistors in the ECL core named $Q_2$, $Q_3$, $Q_6$, and $Q_7$, and four emitter followers between the input buffer and the switching transistors named $Q_1$, $Q_4$, $Q_5$, and $Q_8$. To ensure a correct state of emitter followers and switching transistors, the power supply of switching transistor’s emitter resistors is adjusted to 3.5 V, which expand the operating frequency range but only add little power consumption. The emitter area of all transistors in the ECL core is 0.8 µm x 7.0 µm.

3. Analysis of maximum utilization of $f_t$

Emitter followers of ECL divider increase the $f_t$ of switches toward the maximum $f_t$ as much as possible. However, if the circuit parameters are not analyzed, it is difficult to achieve maximum utilization of $f_t$.

The $f_t$ versus $I_c$ characteristics of the device are shown in Fig. 4 (a) (the result was measured by Agilent N5230C VNA). As the voltage between the collector and the emitter ($V_{ce}$) increases, $f_t$ gradually reaches its maximum and then decreases as $I_c$ continues to grow. This trend can be attributed to the fact that the increase of $V_{ce}$ to some extent suppresses the Kirk effect. When $I_c$ is greater than 7.0 mA and $V_{ce}$ is 1.7 V, the $f_t$ curve is the best, and the maximum value of $f_t$ ($f_{tmax}$) is 150 GHz. According to frequency characteristics described above, the switches of divider core can be adjusted to a state which is closer to the maximum $f_t$, thereby maximum utilization of $f_t$ can be achieved. Fig. 4 (b) is the $f_{max}$ characteristics of the device. The maximum value of $f_{max}$ is 400 GHz.

The function of emitter followers is to increase the $V_{ce}$ of switches. From Fig. 2, equations (1) ~ (5) can be obtained and from Fig. 3, (6) ~ (10) can be obtained. The emitter voltage $V_{ce}$ of $Q_2$ is calculated by Eq. (7). The collector voltage $V_{ce}$ of $Q_2$ is determined by the top differential pair’s
not only amplify the AC current signals from the input buffer but improve the \( V_{ce} \) of switching transistors. If there are not any emitter followers, the \( f_t \) of switches will not exceed 100 GHz at the same \( I_c \), and the utilization of device \( f_t \) no more than 0.66. This may greatly limit the circuit’s ability to drive high frequency signals. It is difficult to achieve such a high device \( f_t \) utilization without analyzing the circuit parameters.

4. Experiment results

4.1 ECL divider measurement setup

The micrograph of the fabricated chip is shown in Fig. 6 (a). The power consumption of the divider and DFF core are 382 mW and 247 mW, respectively. The chip size is 0.44 mm x 0.44 mm (including the Pads).

As shown in Fig. 6 (b), the signal generator is AV1464, which can output RF signals from 150 kHz to 67 GHz with a power range of \(-125\) to \(+14\) dBm. The signal drives the chip through a 50 GHz cable and a 50 GHz GSG probe. The top of Fig. 6 (b) is a block diagram of the ECL divider testing setup while the photograph during the test is at the bottom. The single-end output spectrum and waveform of the ECL divider were measured by a 59 GHz spectrum analyzer (Keysight-DSAZ594A).

4.2 Measurement results

Fig. 7 (a) is the output spectrum (higher harmonics are not shown) of the divider when the input frequency is 1 GHz sinusoidal wave. As shown in Fig. 7 (b), the output waveform of 1 GHz input is not 500 MHz sinusoidal but rectangular wave, because transistor’s gain is high enough to swing collector current fully at such low frequencies. The highest output frequency of the ECL divider is 31 GHz when the input frequency is 62 GHz. The output spectrum and waveform are shown in Fig. 7 (c), (d).

The input frequency operating range of the ECL circuit is from 1 GHz to 62 GHz, and the output frequency is from 500 MHz to 31 GHz. The maximum \( f_t \) of the device is 150 GHz, thus the circuit’s \( BW/f_t \) is 0.413. The simulation result of the frequency range is from 200 MHz to 83 GHz. The performance difference may be mainly caused by the instability of the manufacturing process and frequency limitation of the input 50 GHz cable and the 50 GHz probe. For the reason
that there is not any access for higher performance testing, it is expected that the maximum operating frequency of the ECL divider can exceed 62 GHz.

Fig. 8 (a) is the output power of the ECL divider. The output peak power of the divider gradually decreases and goes sharply down at high frequencies, which may be due to the increase of cables and probes loss. The maximum output power is 0.5 dBm when the input frequency is 20 GHz. The

![Fig. 8](image-url) (a) Maximum output power. (b) Sensitivity of the ECL divider.

![Fig. 9](image-url) (a) Phase noise at 20 GHz carrier frequency. (b) The trend of the phase noise.

**Table I** Comparison with some previously reported dividers

| Refs   | [9]2017 | [11]2011 | [13]2010 | [31]2006 |
|--------|---------|---------|---------|---------|
| Process | SiGe    | InP     | InP     | InP     |
| (μm)    | 0.13    | 0.8     | 0.25    | 0.5     |
| Structure | CML   | CML     | Peaking | Peaking |
| Supply   | V, V−6V | V, V    | V, V    | V, V    |
| Power(total) | 0.056W  | 0.650W  | **      | 0.027W  |
| Power(core) | **     | **     | 0.29W   | **      |
| Output power | −22.66 ** | −19.8 ** | −57.8 ** | −9.7 ** |
| f_c(GHz) | 250     | 199     | 530     | 325     |
| BW(GHz)  | 2−92.5  | 0.5−40  | 5−200.6 | 4−61.2  |
| Minimum  | −40 **   | −31     | −16     |         |
| input power | (dBm)  | (dBm)   | (dBm)   | (dBm)   |
| BW/f_c  | 0.362   | 0.201   | 0.369   | 0.176   |

| Refs   | [25]2019 | [26]2019 | [27]2014 | **This work** |
|--------|---------|---------|---------|---------------|
| Process | InP     | InP     | InP     | InP           |
| (μm)    | 0.7     | 0.7     | 0.7     | 0.8           |
| Structure | ECL   | ECL     | ECL     | ECL           |
| Supply   | V, V    | V, V    | V, V    | V, −3.5V     |
| Power(total) | 0.23W   | 0.264W  | 0.62W   | 0.382W        |
| Power(core) | **     | **     | **      | 0.247W        |
| Output power | −4−0.5 | >0      | −25−2   | −6−0.5        |
| f_c(GHz) | 280     | 280     | 280     | 150           |
| BW(GHz)  | 0.5−43  | 1−48    | 1−83    | 1−62          |
| Minimum  | −20−10  | −7      | −7      | 0            |
| input power | (dBm)  | (dBm)   | (dBm)   | (dBm)         |
| BW/f_c  | 0.154   | 0.168   | 0.293   | 0.413         |

**Not mentioned.**
minimum output power level is \(-6.3\) dBm when the input frequency is 62 GHz. The input sensitivity curve is shown in Fig. 8 (b), where the minimum value of the input power level is \(-70\) dBm at SOF (53 GHz).

As shown in Fig. 9 (a), the Single Side Band (SSB) phase noise is \(-110.1\) dBc/Hz at 10 kHz offset with 40 GHz input. The phase noise is \(-110.47\) dBc/Hz at 100 kHz offset with 40 GHz input, and the phase noise is \(-131.29\) dBc/Hz at 1 MHz offset. Fig. 9 (b) illustrates the relationship between SSB phase noise and output frequency at 10 kHz, 100 kHz, and 1 MHz offsets.

As shown in Table I [31] and Fig. 10, the performance of the ECL divider is summarized and compared with some advanced results. The proposed ECL static divider demonstrates a competitive wideband input frequency range and higher \(BW/f_r\). It shows that the theoretical analysis and design methods of the emitter followers and switching transistors about the utilization of \(f_r\) are effective.

![Fig. 10](image-url)  
**Fig. 10** Previous reports of \(BW/f_r\).

## 5. Conclusion

In this paper, a broadband 2:1 ECL static frequency divider is implemented in a 0.8 \(\mu\)m InP DHBT process. The \(f_r\) of the switching transistors is designed to approach the maximum device \(f_r\) through theoretical analysis for the input buffer and ECL emitter followers. The highest utilization of device \(f_r\) is 0.967. The measurement results show that the bandwidth is from 1 GHz to 62 GHz, the output power dynamic range is from \(-6.3\) dBm to 0.5 dBm, and the \(BW/f_r\) is 0.413. The presented circuit achieves a very high device \(f_r\) utilization and bandwidth utilization compared with other ECL static dividers at the same InP device size. The analysis of device \(f_r\) utilization can make full use of the performance of the device. Our work could extend to the design of other similar type of dividers to reduce the loss of the circuit’s operating frequency.

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