Quasi-3D TCAD modeling of STI radiation-induced leakage currents in SOI MOSFET structure

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Abstract. Quasi-3D model for calculation of radiation leakage currents in modern submicron Silicon-on-Insulator (SOI) metal–oxide–semiconductor field-effect transistor (MOSFET) structures is proposed. The solution of a complex 3-dimensional problem is reduced to solving two tasks: 2D modeling of the traditional MOSFET cross-section and 3D modeling of the side parasitic transistor. The radiation-induced leakage current simulation in the 0.35 μm SOI MOSFET structure with taking account ionizing radiation with a dose of up to 500 krad was simulated. The results of the simulation show that in comparison with the traditional fully 3D modeling, which requires 11 hours of computer time, the computer time for the I_dV_g characteristic was reduced to 71 minutes (i.e. the computer time decreased by 9 times).

1. Introduction
Modern complementary metal-oxide-semiconductor (CMOS) SOI technology is a basic technology for manufacturing high-performance radiation-hardened Very Large Scale Integration (VLSI) due to the advantages of dielectric isolation on a semiconductor chip.

2D and 3D Technology Computer-Aided Design for semiconductor manufacturing technology (TCAD) modeling is an effective tool for investigating the radiation hardness of various designs and technological solutions of SOI MOSFETs. Radiation degradation assessments of such important MOSFET parameters as threshold voltage (V_th), cut-off amplification frequency (f_max/f_T), transconductance (S), leakage current (I_leak) can be obtained using TCAD modeling. The traditional 2D MOSFET modeling is sufficient to estimate the radiation dependencies of V_th and f_max/f_T. However, the 3D description of the MOSFET structure should be used to determine the leakage current I_leak. This is due to the fact that under the ionizing irradiation the positive charge Q_ox accumulates in a thick SiO2 layer of shallow trench isolation (STI) and a buried oxide layer (BOX) and also surface states with densities N_st are induced at the interface oxide-silicon (SiO2-Si). Moreover, the value of Q_ox and N_st depends on the intensity of irradiation. This leads to inversion of the near-surface layer along STI and BOX, and as the result to the formation of parasitic channels for the leakage current (see Fig. 1).

2. General approach to the leakage current simulation in SOI MOSFET structures
The STI areas surrounding the active MOSFET structure on the sides are embedded in the layers of the buried oxide in its lower part (see Fig. 2). This way, the side and bottom parasitic MOSFET are connected in parallel and their leakage currents are summed I_leak = I_leak_STI + I_leak_BOX. It was previously shown that the main component of the leakage current is the STI component [1, 2].
For modern submicron MOSFET structures, the leakage current of the top active transistor can be neglected. First, in a thin gate oxide layer (from 1 to 10 nanometers), the radiation-induced positive charge in the SiO₂ layer or/and the negative charge in the HfO₂ layer is quite small. Secondly, for a well-developed technology, the density of radiation-induced defects \( N_{it} \) at the oxide-silicon interface is also quite small. As a result, the drain leakage current and the threshold voltage shift on input \( I_dV_g \) characteristic of the active transistor are negligibly small compared to the parasitic side and bottom transistor structures. As an example, the input \( I_dV_g \) characteristics before and after irradiation for the active MOSFET (gate) and the parasitic MOSFET (field or edge) are shown in Fig. 3 [2].

The threshold voltage of the side transistor is quite large due to the large thickness of the side oxide before irradiation, but after irradiation a positive charge accumulates in the thick side oxide. This charge is enough to cause a noticeable shift in the threshold voltage. The threshold voltage shift can be so large that the current flowing along the sidewall will make a significant contribution to the total leakage current at \( V_{gs}=0 \) V (OFF regime). It should be noted that the current flowing through such a parasitic transistor depends on the gate voltage, since the leakage area is located in the corner between the STI and the gate oxide (see Fig. 2). As for the main transistor, the threshold voltage shift \( \Delta V_{th} \) and
the magnitude of the leakage current in the OFF regime are significantly less than for a parasitic transistor.

Figure 3. $I_dV_g$ characteristics before and after irradiation for the active MOSFET (gate) and the parasitic MOSFET (field or edge).

As noted above, it is impossible to take into account the influence of the side parasitic transistor in the case for 2D simulation of a MOSFET. Thereby, 3D modeling of the complete MOSFET structure together with STI region (fully 3D) must be carried out. Synopsys Sentaurus TCAD allows carrying out for fully 3D simulation. However, the number of the difference grid elements for calculating the structure is tens of thousands, which, together with the complexity of modeling the charge capture process in the oxide and inversion of the layer in the border region, leads to very large computer time expenditures. For example, the average simulation time of the I-V characteristic for the 3D MOSFET structure with a size $W/L=1.5/0.35 \mu m$ consisting of 165,000 difference grid elements (see Fig. 4) was 10 hours [3] on a computer with a quad-core Intel i7 (3400 MHz) processor and 16 GB RAM.

This example, as well as the results of other works ([1, 4]), show that fully 3D, taking into account the real transistor structure configuration and the physical effects, is a useful tool for studying various constructive-technological solutions of MOSFET structures. However, this approach requires large labor cost a preparatory description of the device structure, a lot of computer time for simulation, processing and interpretation of the obtained calculation results.

Figure 4. SOI MOSFET structure (left) and cross-section with the indication of the leakage area along the sidewall at the STI/Si interface (right).
3. Quasi 3D approach for leakage current modeling in SOI MOSFETs

As an instrument of a development engineer, fully 3D modeling is unsuitable for the rapid evaluation of the device characteristics in real operating conditions and for calculating a large number of variants, primarily because of the very high expenditure of computer time. First version of Quasi 3D model for calculation of radiation leakage currents in submicron SOI MOSFET structures is proposed in [5]. The solution of a complex 3-dimensional problem is reduced to solving a combination of two interconnected, much simpler and less time-consuming 2-dimensional tasks. The first problem is solved in the XY plane of the traditional device cross-section. The second problem is solved in the XZ plane of the longitudinal device cross-section (section A-A in Fig. 4). The simulation time has decreased by 10 times compared to the fully 3D approach for the 0.35 μm structure of the SOI MOSFET shown in Fig. 4. The simulation error in the range of ionization doses up to 300 krad did not exceed 15%.

The disadvantage of the previously proposed Quasi 3D model is the presence an intermediate stage of the merger the 2D structure simulation results in two different planes XZ and XY. The radiation-induced charge distributed over the sidewall in the XZ plane (see Fig. 4) needs to be integrated and transferred into the 2D model of the active transistor in the XY plane to calculate the component of the side leakage current.

A further development of the proposed method is 3D modeling of the leakage current for the side parasitic MOSFET structure. This current is determined directly from the simulation results of an “ultra-narrow” parasitic MOSFET, which is formed at the Si/STI vertical interface (see, Fig. 5). This transistor has a polysilicon gate, a thick “gate” oxide $t_{STI}$, a thin $\Delta Z_{SIDE}$ silicon layer in which radiation-induced charge is localized and also fictitious drain, source, substrate, and well contacts. In such the design, the currents of the side parasitic transistor are simulation on the contacts in the Sentaurus TCAD for any applied voltages and ionization doses.

![Figure 5](image)

Figure 5. “Ultra-narrow” parasitic MOSFET.

4. Simulation results by Quasi-3D TCAD model

0.35 μm SOI MOSFET manufactured using 0.13 μm technology with the following structure parameters $L/W=0.35/10$ μm, $t_{ox}=7$ nm, $t_{Si}=100$ nm, $t_{BOX}=145$ nm, $t_{STI}=130$ nm, $N_A=8\cdot10^{17}$ cm$^{-3}$ under the influence of ionizing radiation with a dose of up to 500 krad was simulated. Radiation models based on experimental data obtained for 0.13 μm CMOS technologies were used in modeling to...
determine the radiation-induced density of $N_0$ defects in SiO$_2$ oxide layers for BOX and STI regions and on Si/SiO$_2$ interfaces – $N_e$ [4, 6].

For all structures, the following physical models were used:
- Recombination: SRH(DopingDep), Auger;
- Mobility: PhuMob, CarrierCarrierScattering, DopingDep, Enormal;
- Band gap narrowing model.

The $I_dV_g$ simulation results are shown in the Fig. 6 and Fig. 7. The computer time for the quasi-3D simulation of the SOI MOSFET with the above parameters is 71 minutes, which is 9 times less than the time costs of a fully-3D calculation, which are about 11 hours. Simulation on a Quasi 3D model are in good agreement with experimental data [7], the calculations error does not exceed 10%.

**Figure 6.** Simulated $I_dV_g$ characteristics sidewall parasitic MOSFET before and after irradiation with a dose of 500 krad.

**Figure 7.** Comparison of experimental (points) [7] and simulating (lines) $I_dV_g$ characteristics before and after irradiation with a dose of 500 krad.

5. Conclusions
The Quasi 3D simulation of the parasitic MOSFET leakage current is proposed. This will make it possible to reduce the computing time by a dozen times and substantially simplify the preprocessor description of the device structure in the TCAD tool. The traditional 3D modeling of MOSFET structure in the Synopsys TCAD has replaced by the two standard subtasks by modeling the primary MOSFET and parasitic lateral STI structure. Both subtasks are solved independently, the components of the active transistor ($I_{leakTOP}$) and side parasitic transistor ($I_{leakSTI}$) leakage currents are determined,
and then these components are summed to determine the total leakage current
$I_{\text{leak}} = I_{\text{leak,TOP}} + I_{\text{leak,BOX}} + I_{\text{leak,STI}}$.

The results of the simulation show that in comparison with the traditional fully 3D modeling, which
requires 11 hours of computer time, the computer time for the $I_dV_g$ characteristic was reduced to
71 minutes (i.e. the computer time decreased by 9 times). Simulation for the quasi-3D model are in
good agreement with the experimental data, the error in the calculations does not exceed 10%.

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