Abstract—Graphene field-effect transistors (GFETs) are experimental devices which are increasingly seeing commercial and research applications. Simulation and modelling forms an important stage in facilitating this transition, however the majority of GFET modelling relies on user implementation. To this end, we present GFET Lab, a user-friendly, open-source software tool for simulating GFETs.

We first provide an overview of approaches to device modelling and a brief survey of GFET compact models and limitations. From this survey, we identify three key criteria for a suitable predictive model for circuit design: it must be a compact model; it must be SPICE-compatible; it must have a minimal number of fitting parameters. We selected Jimenez’s drain-current model as it best matched these criteria, and we introduce some modifications to improve the predictive properties, namely accounting for saturation velocity and the asymmetry in n- and p-type carrier mobilities.

We then validate the model by comparing GFETs simulated in our tool against experimentally-obtained GFET characteristics with the same materials and geometries and find good agreement between GFET Lab and experiment. We demonstrate the ability to export SPICE models for use in higher level circuit simulations and compare SPICE simulations of GFETs against GFET simulations in GFET Lab, again showing good agreement.

Lastly, we provide a brief tutorial of GFET Lab to demonstrate and encourage its use as a community-developed piece of software with both research and educational applications.

I. INTRODUCTION

Since the observation of the electric field effect in atomically thin carbon by Geim and Novoselov in 2004 [28], there has been a proliferation of research into graphene and related materials (GRMs). A key focus of research into electronic devices based on GRMs is the realisation of field-effect transistors (FETs), due to their potential in overcoming the limitations of conventional CMOS devices. One of the main attractions of GRMs is that they overcome short channel effects.

Graphene FETs (GFETs) have a channel made of single- or multi-layer graphene, rather than a semiconducting material such as silicon or germanium [33]. Unlike traditional semiconductors, graphene’s conduction and valence bands don’t overlap and instead meet at a single point, known as the Dirac point. Electrons at the Dirac point are effectively massless and so can have very high electron mobilities, with the room-temperature phonon-limited carrier mobility of graphene on SiO$_2$ being predicted to be around 200,000 cm$^2$V$^{-1}$s$^{-1}$ [4].

Although high electron mobilities result in more efficient flow of charge, the lack of a band gap means GFETs have low on-to off-current ratios and can never completely turn off, making them unsuitable for digital logic applications [13]. However, the poor on-to off-current ratios of GFETs in digital logic applications does not preclude their use in other areas. GFET-based sensors have applications in gas [31], biological [20], and chemical [23] sensing applications, and wafers consisting of multiple GFETs are available off-the-rack from companies including Graphenea [10] and BGT Materials [21], and others utilise GFET-based sensors as part of a larger system, such as Hexagonfab’s protein analyser [9]. Due to their high-mobility, GFETs also have utility in analogue high frequency (HF) applications as the lack of a bandgap and resulting small on-off ratios is not an issue [29], with Vicarelli et al. reporting GFET responsivities on the order of hundreds of GHz at room temperature [37].

As GFET research becomes more application-focused, these models and tools will be increasingly important. Simulation and modelling is a vital part in the design and development of new devices. Technology computer-aided-design (TCAD) is a process in the semiconductor industry which models the fabrication (process TCAD) and operation of semiconductor devices (device TCAD). The latter process models the behaviour of a device based on fundamental physics and comes in two main forms: physics-driven and compact models. The former is a more accurate description, though it is slow as a result, whereas the latter is faster, but less accurate, as the compact models often work one or more assumptions about device behaviour. The speed of compact models does however make them suitable for use with higher-level circuit simulation tools, such as SPICE or Verilog-A.

Our contributions in this article are as follows:

1) A brief survey of existing GFET modelling solutions and the motivation for our tool;
2) Realisation of an open-source, user-friendly software tool for rapid simulation of GFETs to speed up the design and research process;

3) A verification of the utility and versatility of our tool through comparisons to real devices with simulated devices with the same geometries;

4) A brief description of how to use the tool and how to contribute to further development.

II. BACKGROUND AND RELATED WORK

A. Background to Graphene Field-Effect Transistors

First demonstrated by Lemme et al. in 2007 [13], GFETs have since been the subject of an intense research focus, as a result of their unique properties when compared to conventional metal-oxide semiconductor FETs (MOSFETs), such as their high mobilities, fast switching speeds, and ambipolarity.

The vast majority of GFETs consist of a semiconductor/oxide substrate, single- or few-layer graphene channel, produced either via chemical vapour deposition (CVD), or mechanical exfoliation, metal source and drain contacts, and either a back gate, additional dielectric and top gate, or both. Figure 1 shows these three common GFET topologies. The first consists of a graphene channel on a semiconducting substrate, e.g., Si/SiO₂, with source and drain contacts deposited on top and the doped semiconducting layer used as a back gate. The second is similar to the first, except with the addition of a top gate contact, typically separated from the graphene channel with a dielectric material, such as Al₂O₃, however other dielectrics, such as ion-gels can be used [14].

The first topology, owing to the relatively small number of fabrication steps, is amongst the most common and many off-the-shelf GFETs feature this geometry. For sensing applications where interactions between surface adsorbents (e.g., gas molecules or proteins) and the graphene channel change the conductivity, this structure is necessary. However, graphene degrades in the air, with p-type doping as a result of moisture adsorption being a common defect. The second and third geometries, where the graphene channel is encapsulated by an insulating dielectric layer provides greater stability, although there is an impact on the electrical characteristics, namely the mobility, owing to phonon interactions between the oxides and the graphene channel.

However, these are not the only types of GFET. Graphene nanoribbon FETs (GNRFETs), are another form of GFET which are the subject of active research. GNRFETs are an approach to engineering a bandgap in graphene by slicing graphene into narrow ribbons. This results in a splitting of the usual 2D energy dispersion of graphene into a number of 1D modes [4], leading to the formation of a bandgap, as some of the 1D modes do not pass through the Dirac point.

Bilayer GFETs also offer a way to induce a bandgap in graphene, with the advantage of it being electrically tunable [42]. Such devices have a virtually identical structure to conventional monolayer GFETs, however these instead have two graphene layers. Due to the relative ease of scalable manufacture, these devices are potentially of greater interest than GNRFETs for commercialisation, however the on/off ratios are typically on the order of 100 [40] and the band gaps are small, typically on the order of a few hundred meV [42] [40], meaning they are unlikely to be a direct replacement for silicon-based transistors in many applications.

Tunnelling GFETs form another class of device which attempts to induce a bandgap in graphene. First reported by Brittell et al. [11], tunnelling GFETs generally consist of a heterostructure of graphene and another GRMs such as MoS₂ or hexagonal boron nitride (h-BN) which acts as a tunnel barrier. Compared to e.g., bilayer GFETs, such devices can have on/off ratios as high as 10⁷, however this is still several orders of magnitude short of the standard for digital CMOS logic.

B. Related Work

There is already a substantial body of work on the simulation of GFETs, with Meric et al. presenting the first GFET compact model [25] in 2008. The literature has grown to include both compact and physics-driven models, as well as models for different forms of GFET, including GNRFETs. We do not intend for this article to serve as a review of GFET modelling, instead focusing on the use of modelling as part of the research and development process, so we direct the interested reader to Lu et al.’s comprehensive survey of GFET compact models [22].

Currently, very few open-source, user-friendly tools for simulating GFETs or other devices exist. GFET Tool, by Pop and Lian [29], is limited in the characteristics and properties simulated, as well as the device structure and so has limited use for higher-level simulations. Leong et al. developed a tool called GFETSIM [19] which is implemented in MATLAB and features a GUI. However, this tool has a different focus to that which we envisage: Leong et al.’s tool simulates interface charge densities in GFETs based on measured characteristics of real devices. Other models rely mainly on user implementation, as they provide SPICE-compatible models or implementations, rather than being self-contained tools.

III. GFET LAB

A. Model Criteria

For predicting device characteristics, it is necessary to identify the criteria which make a suitable model for use in GFET Lab. What follows is an overview and justification of the criteria we establish.

1) Criteria 1: Compact Models: Models of GFETs exist at varying levels of abstraction and Fiori and Iannaccone [6] provide a comprehensive overview of these. We provide a brief overview below. The most complex models are ab initio models, which typically make use of techniques such as density functional theory (DFT). These models are computationally intensive however and become very inefficient for systems larger than a few hundred atoms. The next tier of abstraction is atomistic modelling, which predicts electronic properties of materials by defining a given system’s Hamiltonian on an atomistic basis set. Increasing the level of abstraction further is semiclassical device modelling, which is based on the Poisson equation and a transport equation (e.g., drift-diffusion model or Boltzmann transport equation), where parameters are determined either based on empirically measured device characteristics or from the results of ab initio or atomistic simulations. Analytical models form the final layer of abstraction. These, as a result of the assumptions required to make the necessary simplifications, are best suited to specific devices. As a result of their simplicity, analytical models best lend themselves to circuit simulation, rather than individual device simulations and are more likely to be compatible with other modelling tools such as SPICE or Verilog-A.

2) Criteria 2: SPICE Compatibility: As we intend GFET Lab to form part of a larger workflow, the ability to export a design to be used in higher-level simulations is vital. Simulation tools such as SPICE and Verilog-A depend on compact models and so was another important consideration when choosing which model to implement.
3) Criteria 3: Minimal Fitting Parameters: Another criteria we specify is that the number of fitting parameters in a model is kept to a minimum. Often, published models introduce empirical fitting parameters which make them better correspond to the characteristics of real devices. This can be an invaluable tool when demonstrating a proof-of-concept, e.g., when one wishes to explore how an array of their experimental device that may otherwise be prohibitively time-consuming or expensive to fabricate would perform in a given application. However, for the initial design process of a device, this would not make sense, as one cannot know the characteristics of a device before they fabricate it. The one exception we make here is for the carrier mobility ($\mu$), as this is a fundamental part of the expression for the drain current, but can only be determined by electrical characterisation, e.g., using a four-point probe.

In Section IV we evaluate the simulated characteristics of GFET Lab against a number of real devices, and thus give estimates of the mobilities in the accompanying tables, for specific device geometries, however the mobility is dependent on many factors, including dielectric material(s), whether the graphene channel is grown by CVD or mechanically exfoliated, the presence of surface impurities and also bias voltages so these are only rough estimates.

B. Limitations of GFET Lab

Modelling of devices is rarely perfect and GFET Lab also has a number of inherent limitations. The first limitation is that it makes no distinction between whether the device one is designing will use CVD or mechanically exfoliated graphene. Typically, the latter is of higher quality and has more ideal properties, as well as less impurities, however it is also not an easily-scalable process, unlike CVD and so the latter is more popular for this reason.

The second limitation is that models do not account for hysteresis in device characteristics. Many GFET transfer characteristics exhibit hysteresis in the form of a shift in the Dirac point position between forward- and reverse-gate voltage sweeps. This is contributed to by multiple factors, including charge trapping between the graphene channel and the dielectric layers [17], capacitive gating, which causes a negative shift in the position of the Dirac point, and charge transfer which causes a positive shift [18] in the Dirac point with respect to gate voltage.

A third limitation is that GFET models tend to be symmetrical, i.e., one expects the same drain current at equal distances either side of the Dirac point. However, in real devices, an asymmetry is often present, typically for positive gate voltages, i.e., the region dominated by p-type conductivity. Because this asymmetry is again the result of a number of contributing factors, it is hard to precisely quantify or predict without the introduction of empirical fitting parameters. Mukherjee et al.'s model [27] attempts to account for this by considering drain current as having two components, current from n-type carriers and current from p-type carriers, each with their own mobility, however this relies on one making assumptions about asymmetry.

A final limitation is the breadth of models considered. As discussed in Section II, a number of classes of GFETs exist, including GNRFETs, Bilayer GFETs, Tunneling GFETs, those using electrolytes or ionic gels as gates, and those with functionalised graphene channels. GFET Lab does not presently include models for such devices. At the time of writing, we are aware of models for a range of devices, such as Karimi et al.'s solution-gated GFET biosensor model [12], Mackin's model for electrolyte-gated GFETs [24], Cheli's model for a bilayer GFET [2] and Guo's review of GNRFET models [8]. However, as we discuss in Section V we intend for GFET Lab to be a tool contributed by the community, making it open source so that individuals and groups can tailor it to their specific needs and share these developments with the wider research community.

C. The Implemented Model

Lu et al.'s survey of compact GFET models [22] formed a useful starting point to determine which model(s) to implement. Certain models built upon previous models, forming a chronology. For example, Thiele [34] builds upon the early model of Meric [25], however Thiele's model is not compact and thus not SPICE-compatible. Fregonese [7] derived a compact solution to Thiele's model, from which Rodriguez [30] provided a further simplification to aid with hand-calculations.

The criteria outlined above helped limit our search and we further limited our search by not considering models for GNRFETs, bilayer GFETs, or tunneling GFETs. However, there remained a large number of compact models which exist in the literature and so we skip providing a comparison of each and our resulting justification for the model's inclusion or not for brevity. In general, we selected models with minimal fitting parameters, lower computational load, and which appeared to accurately predict the characteristics of real devices. We also verified the dimensionality of models, to ensure that the user-defined parameters give correct output by performing internal conversions where necessary (e.g., from meV to Joules).

At the time of writing, we have implemented Jimenez et al.'s model [11] (Table 1), as it appeared to best meet the criteria we outline above. We made several modifications to the model. Firstly, Jimenez et al.'s model does not account for the saturation velocity, $v_{Sat}$ and so we use the following expression from Mukherjee et al.'s model to replace the Fermi velocity, $v_F$ in the expression for the effective channel length, $L_{eff}$, in the Jimenez model:

$$v_{Sat} = \frac{\omega}{\sqrt{\frac{\pi Q_{Sat}}{n} + \frac{n_{pud} \pi}{2}}}$$

where $\omega$ is derived from the expression for the surface phonon energy, $E_s$, $Q_{Sat}$ is the net charge in the channel, given by $Q_{Sat} = \beta V_G |V_{GS}|$, and $n_{pud}$ is a constant which accounts for charge puddles that arise due to the spatial inhomogeneity of the graphene sheet, i.e., as a result of the substrate roughness and is given by:

$$n_{pud} = \frac{\Delta^2}{\pi (v_F)^2}$$

Here, $\Delta \approx 54$ meV and represents the electrostatic potential when $v_F = 1.3 \times 10^6$ [43]. To account for the asymmetry typically observed in GFET transfer characteristics, we also introduce a dimensionless parameter, $\alpha = \frac{\mu_n}{\mu_p}$, which is simply the ratio of the n- to p-type mobilities ($\mu_n$ and $\mu_p$ respectively). This applies when the dominant carrier type is n-type, i.e., for $V_{GS} - V_{G0} - V_{D0} + V_{GS} - V_{G0} - V_{D0} > 0$ ($V_{G0}$ = gate-source voltage, $V_{G0}$ = gate-source threshold voltage, $V_{D0}$ = back gate voltage, $V_{G0}$ = back gate threshold voltage, and $V_{D0}$ = source-drain voltage). Lastly, we assume the device mobility, $\mu_{av}$, is the average of the n- and p-type mobilities: $\mu_{av} = \frac{\mu_n + \mu_p}{2}$.

Lee et al.'s model for a single back-gated monolayer GFET (as in Figure 1(a)) appeared to be the only such model in the literature [16], however, as it does not account for quantum capacitance, we have decided to exclude it from GFET Lab. Thus, there are presently no models for such a device structure. Instead, we provide the option for one to select air as the back-gate dielectric material ($\epsilon_r = 1$) with infinite thickness and treat the top-gate as the back gate. This effectively corresponds to a zero-valued gate capacitance, which results...
in a division by zero when determining the $V_{bg0}$ term and so, in this scenario, we assume $V_{bg0} = 0$.

Many of the expressions involve standard physical and material constants: $\epsilon_r$ and $\epsilon_0$ are the relative and vacuum permittivities respectively, $q$ is the elementary charge, $\hbar$ is the reduced Planck constant, $\eta_F$ is the Fermi velocity, $k_B$ is Boltzmann’s constant, $T$ is the operating temperature, $E_F$ is the Fermi level and $E_C$ is the conduction band energy. $N_f$ is the dopant carrier density. Table II shows the dielectrics available in GFET Lab, as well as the associated parameters.

The remaining terms relate to the device geometry: $t_{tox}$ and $t_{box}$ are the top and back gate oxide thicknesses, $W$ and $L$ are the channel width and length and $x$ is the position along the channel. $C_t$ and $C_b$ are the top- and back-gate capacitances and are defined by $\frac{C_{tx}}{t_{tox}}$ and $\frac{C_{bx}}{t_{box}}$ respectively.

Another material parameter which arises in some models is the intrinsic Fermi level of undoped graphene ($E_F$), which is reported to be around 4.57 eV\textsuperscript{[41]}, however it is also given by $E_F = \hbar v_F \sqrt{\pi n}$ for monolayer graphene\textsuperscript{[23]}, where $n$ is the carrier density. Although the model we implement does not account for these, we include them in GFET Lab to ensure ease of integration for user-defined models.

The one fitting parameter that is essential for device modelling is the carrier mobility, $\mu$. This can be measured either using a four-point measurement, or calculated from electrical characterisation using the following expression:

$$\mu = \frac{L}{V_{ds} C_{ox} W} \frac{dI_{ds}}{dV_{gs}}$$

However mobility is a key parameter for calculations of the device characteristics and so one must assume a value. The mobility is dependent on a number of factors, with shorter channels having lower mobilities, as well as CVD graphene generally having lower mobilities than mechanically exfoliated graphene\textsuperscript{[36]}. Additionally, some models use the intrinsic carrier mobility, whereas others consider two regions of conductivity: that dominated by n-type carriers (i.e., electrons) and those dominated by p-type carriers (i.e., holes).

TABLE I

| Term     | Equation                                                                 | Meaning (Units)                     |
|----------|--------------------------------------------------------------------------|-------------------------------------|
| $I_D$    | $\frac{\mu_{av} k}{2} \frac{W}{t_{tox}} g (V_c) V_{ds}^2$               | Drain current (A)                   |
| $L_{eff}$| $L + \mu_{av} V_{ds} t_{box}$                                            | Effective channel length ($\mu$m)   |
| $g$      | $\frac{-V_c^2}{3} - \text{sign} (V_c) \frac{4V_c^3}{4E_C^2} + E_F$      | Channel conductance (S)             |
| $V_C$    | $[a]^{-1} (C_A + C_b) + \sqrt{(C_A + C_b)^2 + 2k_B [(V_{gs} - V_{tox} - V)C_A + (V_{ds} - V_{box} - V)C_b]}$ | Channel voltage (V)                |
| $k$      | $\left( \frac{2\alpha^2}{\pi^2} \right) \frac{1}{\eta_F}$             | Constant term ($\epsilon_0^2$ / T)  |

TABLE II

| Material | Relative Permittivity ($\epsilon_r$) | Surface-Phonon Energy (meV) |
|----------|-------------------------------------|-----------------------------|
| SiO$_2$  | 3.9                                 | 59.98                       |
| SiC      | 9.7                                 | 116                         |
| Al$_2$O$_3$ | 12.53                             | 55.01                       |
| AlN      | 9.14                                | 83.60                       |
| HfO$_2$  | 22.0                                | 19.42                       |
| ZrO$_2$  | 24.0                                | 25.02                       |
| h-BN     | 5.09                                | 101.6                       |

The common dielectrics, their relative permittivities and surface-phonon energies. All except h-BN adapted from\textsuperscript{[15]}, values for h-BN adapted from\textsuperscript{[23]}. Note that $V_{ds}$ and $V_{gs}$ are functions of $I_{ds}$ and $I_{ds}$ is a function of $V_{ds}$ and $V_{gs}$, meaning that these would typically need to be solved self-consistently, e.g., using the Newton-Raphson method. However, by considering the voltages used in the simulations as the intrinsic voltages, one can rearrange the above expressions for the extrinsic voltage and calculate the extrinsic voltages from the values of contact resistance and simulated drain current and plot the drain current against the calculated extrinsic voltage. In practise, this means one assumes that the $V_{ds}$ and $V_{gs}$ values used in the simulation are intrinsic and, once $I_{ds}$ values are simulated, these are combined with the intrinsic $V_{ds}$ or $V_{gs}$ values in the above expressions to calculate the extrinsic $V_{ds}$ and $V_{gs}$ values. One then plots the simulated $I_{ds}$ values against the calculated extrinsic $V_{ds}$ or $V_{gs}$ values. Although Verilog-A and SPICE models have some capacity to perform Newton-Raphson iteration, this is typically used for finding operating points of circuits, rather than component simulation. Thus, the above approach makes the implementations both simpler to compute and also SPICE and Verilog-A compatible.

IV. SIMULATION EVALUATION

A. Model Validation

To verify the applicability of our tool, it is worthwhile to compare the performance to real GFETs. We compare a number of devices with different geometries, shown in Table III to validate the versatility
of GFET Lab. Figure 3 shows comparisons of the simulated and experimentally-obtained transfer and I-V characteristics of GFETs with different channel geometries and dielectric materials. The first GFET (GFET 1) consists of an SiO2 substrate with an Au back gate, a 50 nm AlOx dielectric layer, a monolayer graphene channel with Au source/drain contacts, another 50 nm AlOx dielectric layer and an Au top gate. We describe the fabrication and characterisation of the GFET in a previous work [35]. We then validate the tool’s performance for both alternative device structures, as well as for the same fabrication process with different channel dimensions, by comparing simulated and experimental characteristics for several devices (GFETs 2-4 in Table III) from the Graphenea S10, an off-the-shelf die consisting of 36 graphene devices with various geometries. In all simulations, we take N_f to be 5 × 10^{15}. We attempted a naïve derivation of carrier mobility values from the experimental data using equation (3), however these values did not appear accurate and so, for the purposes of validation, we estimate values of mobility which provide a good fit to the data. We measured the output characteristics by measuring the GFET drain current (I_{ds}) as a function of the drain-source voltage (V_{ds}). Different factors in GFETs can cause poor current saturation including the lack of bandgap, interfacial phonon scattering and inadequate electrostatic control [25, 26]. This leads to a large region of linear output characteristics. This region is valuable for extracting various parameters, including the quality of the contact resistance. We obtained the transfer characteristics of GFET by measuring the drain current as a function of the gate voltage (V_{gs}) for constant V_{ds}. Resistivity (conductivity) and mobility which are important parameters of GFETs can be extracted from transfer characteristics. We performed electrical characterisation of the Graphenea S10 devices using a Keithley 4200 semiconductor characteriser system (Keithley, 4200 SCS) combined with a probe station in the air.

Figures 3(a) and (b) show the experimentally-obtained and simulated transfer and I-V characteristics for GFET 1. (a) shows multiple transfer characteristics for the same device, with V_{gs} bias voltages ranging from 0.2 to 1 V. The model matches the experimental data to a reasonable degree, with the orders of magnitude being relatively close to the measured data, although the on/off ratio shows some discrepancy: the on/off ratio for the experimental data ranges from 2.27 to 2.41, whereas the on/off ratios for the simulations range between 7.5 to 25. In real devices, a voltage sweep typically causes a shift in the position of the Dirac point as a result of changing charge trap densities, as accounted for by n_{pud}, influencing the mobilities and saturation velocity, however our model does not account for this and assumes a constant n_{pud}. This explains the discrepancy in on/off ratios, as, by equation (1), V_{sat} depends on n_{pud}. When the net channel charge, Q_{net} is small, i.e., when V_c ≈ 0, n_{pud} becomes the dominant factor in the value of V_{sat} and so discrepancies between this value and the actual value will translate to variations in the on/off ratio.

Figure 3(b) shows the IV characteristics for the same device, with V_{gs} bias voltages ranging from 0.2 to 1 V. The simulation and experimental characteristics, although on the same order of magnitude, show a larger discrepancy. In the IV characteristics simulation, we used a V_{bg} bias of -1 V, which gives reasonable agreement with the experiment, being of the same order of magnitude and similar values for the same bias voltages. Both characteristics show a point of inflection as expected for a GFET, however the point occurs at around 2 V in the simulation, compared to around 4 V in the experiment. In a real device, bias conditions will be different depending on the nature of the voltage sweep and thus influence other parameters which the model assumes are constant, such as the mobility and carrier velocity.

Figures 3(c) and (d) shows simulated and measured transfer characteristics for three GFETs from the Graphenea S10 [10] whose details are described in Table III. As the S10 devices have a single back gate, we treat the back gate in the model as a top gate with a 90 nm SiO2 dielectric. We account for the large shift in the Dirac point position in the experimental characteristics by adding a back gate bias voltage, V_{bg}. We consider the virtual gate oxide to be 1 nm thick with a dielectric constant equal to the vacuum permittivity. Again, the shape and order of magnitude of the simulated device is relatively close to the experimental data, however there is a discrepancy between the on/off ratios of the experimental and simulated GFETs. The experimental data have on/off ratios ranging between about 4 and 7, whereas the on/off ratios for the simulations range from about 153 to 530.

In each device, there are discrepancies between the simulated and real device characteristics, which are likely due to non-idealities which arise in devices. For example, asymmetries in the measured characteristics versus the modelled characteristics can arise due to unintentional doping as a result of the fabrication process or device degradation, something which many models don’t account for, however our introduction of the parameter α appears to account well for this. Additional fitting parameters and fine-tuning of the model would give a closer response, however, as our intention here is a generalised tool for predicting device characteristics, rather than fitting a model closely to a single device, these results suggest broadly good agreement with experiments. As fitting parameters are typically empirical in nature, this only really makes them useful after fabrication, e.g., when one wishes to simulate a circuit consisting entirely of fabricated devices, rather than to predict the characteristics of a device before fabrication.

A systematic way to quantify the influence of the fabrication process would be very useful, e.g., by considering fitting parameters as process parameters. For example, coefficients to denote CVD vs exfoliated graphene, doping as a result of the transfer and patterning processes, the influence of the growth substrate etc., with values determined by fabrication (e.g., establishing a relationship between resist etching
time and doping levels in electrical characteristics), could provide a more rigorous framework for device design and simulation.

B. Integration with Higher-Level Tools

We also verify the correct output for exported SPICE models. Figure 4 shows the simulated transfer and I-V characteristics both in GFET Lab using the exported models in LTSpice for GFETs 1-4. As the figure shows, the LTSpice simulation and GFET Lab transfer and I-V characteristics are consistent.

V. GFET LAB: USAGE AND OPEN-SOURCING

A. GFET Lab Tutorial Overview

As a stand-alone software tool, GFET Lab is intended to be used exclusively through the GUI. Figure 5 shows the main screen of the program.

At the top, a button to run the simulations, alongside drop-down menus for file I/O functionality is provided. The first menu allows users to load custom voltage sweeps, as well as exporting a template file which is in a readable format for GFET Lab. The second drop-down menu allows users to export simulation results and SPICE models. Figure 6 shows the options in each menu.

The left-hand frame forms the virtual laboratory aspect of the software, where the users can specify device and sweep parameters, as well as selecting the device model they wish to use. The “Device Parameters” tab is where the user specifies the device geometry (dielectric thickness(es), channel dimensions), the dielectric material (e.g., AlO$_2$, HfO$_2$...), the operating temperature and other material parameters, such as the carrier mobility, the Fermi velocity, the surface phonon energy and the effective dopant density.

The “Sweep Parameters” tab allows the user to define the GFET model to be used, as well as the voltage sweeps they wish to simulate. For example, whether to sweep the gate voltage or the source-drain voltage and the shape of the sweep (linear, logarithmic etc.). These settings are based on the functionality of the Keithley 2400 source-measure unit, a common tool for device electrical characterisation. There are two main plots used for the characterisation of transistors, a transfer characteristic plot, where the source-drain voltage is kept constant and the gate voltage is swept, and an I-V characteristics plot, where the gate voltage remains constant and the source-drain voltage is swept. As both use slightly different loops in the code, we provide both in separate tabs and a single simulation run will conduct both.

The “Sweep Parameters” tab allows the user to define the GFET model to be used, as well as the voltage sweeps they wish to simulate. For example, whether to sweep the gate voltage or the source-drain voltage and the shape of the sweep (linear, logarithmic etc.). These settings are based on the functionality of the Keithley 2400 source-measure unit, a common tool for device electrical characterisation.

The right-hand frame displays the simulation results. The user simply selects a given tab to display the plot they wish to see. In addition to the transfer and I-V characteristics, the software also plots the transconductance and transit frequency of the simulated device, both of which are often of interest to researchers.
B. Community Contribution

We developed the tool with two main motivations. Firstly to help in the development of GFET circuits, by allowing for rapid simulation of GFET characteristics with different parameters. These include bias voltages and device structures (i.e., gate oxide thickness, oxide material, channel dimensions), so desired characteristics can be easily determined and compared before embarking on an involved and time-consuming fabrication process. This also allows for prediction of ideal device and/or circuit behaviour, against which realised devices can be evaluated. Our second motivation is that our software has value as an educational tool. GFETs aren’t available as off-the-shelf components in the same scale, quantities or price as conventional transistors, and so the ability to experiment with GFET behaviour, based on verified models is valuable for training and familiarising non-experts with these devices.

As part of this, we provide the ability to export models for use in SPICE simulators such as LTSpice. We have only implemented the model discussed in the article, but the typical format of an exported SPICE model is as follows:

```plaintext
* n1=Top Gate, n2=Drain, n3=Source, n4=Back Gate
.subckt GFETModel n1 n2 n3 n4
    .params
    .ends GFETModel
```

We encourage others to contribute and expand on the software to maximise its utility, either by expanding the library of available GFET models by translating others from the literature, by expanding the functionality to better represent experiments one might conduct using GFETs, or by submitting bug reports.
class GFETModel:
    def __init__(self, params, ivSweep, transSweep, eps):
        self.ids = []
        def fnIds(self, Vtg, Vbg, Vds):
            ...
        (Model-dependent parameters, e.g., geometry, calculation of capacitances, contact resistances...)
        ...
        (Additional functions required by the model)
        ...
    def fnIds(self, Vtg, Vbg, Vds):
        ...
        (Expressions required, e.g., to determine effective channel length)
        return (Model expression of the drain current)
    def calculateIVChars(self):
        ...
    def calculateTransferChars(self):
        ...

Fig. 4. (a) Comparison of the simulated transfer characteristics of GFET 1 from both GFET Lab and the exported SPICE model for \( V_{ds} = 0.2 - 1 \) V; (b) Comparison of the simulated I-V characteristics of GFET 1 from both GFET Lab and the exported SPICE model for \( V_{ds} = 0.2 - 1 \) V; (c) Comparison of the simulated transfer characteristics of GFET 2 from both GFET Lab and the exported SPICE model; (d) Comparison of the simulated I-V characteristics of GFET 3 from both GFET Lab and the exported SPICE model; (e) Comparison of the simulated I-V characteristics of GFET 4 from both GFET Lab and the exported SPICE model. In each, the LTSpice and GFET Lab model parameters are the same as in Figure 3. In both, crosses correspond to GFET Lab simulations and dashes correspond to LTSpice simulations.

What follows is a demonstrative description of model implementation in GFET Lab. Each model is a class which takes as arguments the contents of the user-defined sweep and device parameter boxes. Each model has the following methods: init, fnIds, calculateTransferChars, and calculateIVChars. The first initialises the model class with the relevant device and sweep parameters, the second performs the calculation of the drain current, the third simulates the device transfer characteristics, transconductance and transit frequency, and the fourth simulates the I-V characteristics. Additional functions, such as those to determine channel voltage or saturation velocity may also be implemented. In principle, GFET Lab can be extended to model other 2D materials by implementing a suitable model, enhancing its value as a research tool.

```python
class GFETModel:
    def __init__(self, params, ivSweep, transSweep, eps):
        self.ids = []
        def fnIds(self, Vtg, Vbg, Vds):
            ...
            (Model-dependent parameters, e.g., geometry, calculation of capacitances, contact resistances...)
        ...
        (Additional functions required by the model)
        ...
    def fnIds(self, Vtg, Vbg, Vds):
        ...
        (Expressions required, e.g., to determine effective channel length)
        return (Model expression of the drain current)
    def calculateIVChars(self):
        ...
```
Fig. 5. (a) Screenshot showing the main screen when the program is launched. Here, the user can specify the parameters of the transfer characteristics sweep, as well as selecting the model they wish to use; (b) Screenshot showing the tab where the user can specify the device parameters, such as gate dielectric, channel dimensions, carrier mobility and others. The parameters used will depend on the selected model and so some parameters will be ignored for some models.

Fig. 6. These screenshots show possible import and export options for the simulator. (a) Shows the importing options for loading external sweeps, as well as allowing users to export a template sweep file for ease of use. (b) Shows the various data exporting options, including the transfer characteristics, the I-V characteristics, frequency response and a SPICE model of the simulated device.

VI. Conclusions

We have surveyed the GFET modelling literature, providing both a background and brief overview of the field, as well as discussing limitations of device modelling. Based on the survey, we identify three criteria for a suitable predictive device model. Such a model should be compact, SPICE-compatible, and require a minimal number of fitting parameters. Based on these criteria, we selected Jimenez et al.’s explicit drain-current GFET model and implemented it in a user-friendly software tool called GFET Lab. We then simulate GFET characteristics based on the geometries and materials of real devices in the software and compare the simulations to empirically-measured characteristics of the devices to validate the model and software. The characteristics show good agreement with the real devices, being of the correct order of magnitude for the same voltage sweeps and bias conditions, with the main discrepancy being the on/off ratio. The reasonable agreement between simulation and experiment demonstrates GFET Lab’s utility as both a research and educational tool. We also propose the notion of process parameters for device modelling, where fitting parameters are determined as functions of the fabrication process, allowing for models to account for variations which arise as a result of the fabrication process, e.g., doping due to wet-transfer, or the more pronounced asymmetry between n-type and p-type conductance in CVD graphene compared to exfoliated graphene. We then demonstrate good agreement between the simulated characteristics of GFET Lab and the exported SPICE models when simulated in LTSpice. Lastly, we provide a short tutorial to GFET Lab, as well as detail how members of the community can contribute to the software to maximise its potential as a research tool.

Acknowledgements

P. Stanley-Marbell is supported by an Alan Turing Institute award TUB/B/000096 under EPSRC grant EP/N510129/1, by EPSRC grant EP/V047507/1, and by the UKRI Materials Made Smarter Research Centre (EPSRC grant EP/V061798/1). N.J. Tye acknowledges funding from EPSRC grant EP/L016087/1. We also thank David Jimenez for his advice on model implementation, particularly in regards to considering intrinsic and extrinsic voltages, Giorgio Mallia for the photographs on the experimental setup in Figure 2, and Bilgesu Bilgin for fabricating GFET1 which we characterise in this article.

Code Availability

The full source code for GFET Lab is available at: https://github.com/physical-computation/gfet-simulator.

References

[1] R. Britnell, R. V. Gorbachev, J. Jalil, B. D. Belle, F. Schedin, A. Mishchenko, T. Georgiou, M. I. Katsnelson, L. Eaves, S. V. Morozov, N. M. R. Peres, J. Leist, A. K. Geim, K. S. Novoselov, and L. A. Ponomarenko. Field-effect tunneling transistor based on vertical graphene heterostructures. Science, 335(6071):947–950, 2012.

[2] M. Cheli, G. Fiori, and G. Iannaccone. A semianalytical model of bilayer-graphene field-effect transistor. IEEE Transactions on Electron Devices, 56(12):2979–2986, 2009.

[3] R. Britnell, R. V. Gorbachev, J. Jalil, B. D. Belle, F. Schedin, A. Mishchenko, T. Georgiou, M. I. Katsnelson, L. Eaves, S. V. Morozov, N. M. R. Peres, J. Leist, A. K. Geim, K. S. Novoselov, and L. A. Ponomarenko. Field-effect tunneling transistor based on vertical graphene heterostructures. Science, 335(6071):947–950, 2012.
[4] J.-H. Chen, C. Jing, S. Xiao, M. Ishigami, and M. S. Fuhrer. Intrinsic and extrinsic performance limits of graphene devices on sio2. Nature Nanotechnology, 3(4):206–209, 2008.

[5] Z. Chen, Y.-M. Lin, M. J. Rooks, and P. Avouris. Graphene nano-ribbon electronics. Physica E: Low-dimensional Systems and Nanostructures, 40(2):228–232, 2007.

[6] G. Fioni and G. Iannaccone. Multiscale modeling for graphene-based nanoscale transistors. Proceedings of the IEEE, 101(7):1653–1669, 2013.

[7] S. Frégonèse, N. Meng, H.-N. Nguyen, C. Majek, C. Maneux, H. Hppy, and T. Zimmer. Electrical compact modelling of graphene transistors. Solid-State Electronics, 73:27–31, 2012.

[8] J. Guo. Modeling of graphene nanoribbon devices. Nanoscale, 4:5538–5548, 2012.

[9] HexagonFab. Hexagonfab bolt. https://www.hexagonfab.com/products Accessed: 2021-07-20.

[10] G. Inc. Gfet-s10 for sensing applications. https://www.graphenea.com/products/gfet-s10-for-sensing-applications-10-mm-x-10-mm?variant=39420477243550s. Accessed: 2022-01-8.

[11] D. Jimenez. Explicit drain current, charge and capacitance model of graphene field-effect transistors. IEEE Transactions on Electron Devices, 58(12):4377–4383, 2011.

[12] H. Karimi, R. Yusof, R. Rahmani, H. Hosseinpour, and M. T. Ahmadi. Development of solution-gated graphene transistor model for biosensors. Nanoscale Research Letters, 9(1):71, Feb 2014.

[13] R. W. Keyes. What makes a good computer device? Science, 230(4722):138–144, 1985.

[14] B. J. Kim, H. Jang, S.-K. Lee, B. H. Hong, J.-H. Ahn, and J. H. Cho. High-performance flexible graphene field effect transistors with ion gel gate dielectrics. Nano Letters, 10(9):3464–3466, 2010. PMID: 20704323.

[15] A. Konar, T. Fang, and D. Jena. Effect of high-κ gate dielectrics on charge transport in graphene-based field effect transistors. Phys. Rev. B, 82:115452, Sep 2010.

[16] J. Lee, H. Shin, H.-J. Chung, J. Lee, J. Heo, H. Yang, S.-H. Lee, and S. Seo. Compact modeling of extremely scaled graphene fets. Journal of the Korean Physical Society, 61(11):1797–1801, Dec 2012.

[17] M. Lemme. Current status of graphene transistors. In Getting and Defect Engineering in Semiconductor Technology XIII, volume 156 of Solid State Phenomena, pages 499–509. Trans Tech Publications Ltd, 1 2010.

[18] M. C. Lemme, T. J. Echtermeyer, M. Baus, and H. Kurz. A graphene field-effect device. IEEE Electron Device Letters, 28(4):282–284, 2007.

[19] C. H. Leong, H. C. Chin, C. W. Ang, C. Khi Ng, F. Najam, C. S. Lim, S. C. Tan, and M. P. L. Tan. Gfetsim: Graphene field-effect transistor simulator of interface charge density. Journal of Nanoelectronics and Optoelectronics, 12(4):304–315, 2017.

[20] M. B. Lerner, F. Matsunaga, G. H. Han, S. J. Hong, J. X. Ai, C. Crook, J. M. Perez-Aguilar, Y. W. Park, J. G. Saven, R. Liu, and A. T. C. Johnson. Scalable production of highly sensitive nanosensors based on graphene functionalized with a designed g protein-coupled receptor. Nano Letters, 14(5):2700–2714, 2014. PMID: 24742304.

[21] B. M. Ltd. Grat-fet. https://www.bgmaterials.com/products_grat_fet.php Accessed: 2021-07-20.

[22] N. Lu, L. Wang, L. Li, and M. Liu. A review for compact model of graphene field-effect transistors. Chinese Physics B, 26(3):036804, mar 2017.

[23] Y. Lu, B. R. Goldsmith, N. J. Kybert, and A. T. C. Johnson. DNA-decorated graphene chemical sensors. Applied Physics Letters, 97(8):083107, 2010.

[24] C. Macklin, L. H. Hess, A. Hsu, Y. Song, J. Kong, J. A. Garrido, and T. Palacios. A current-voltage model for graphene electrolyte-gated field-effect transistors, IEEE Transactions on Electron Devices, 61(12):3971–3977, 2014.

[25] I. Meric, M. Y. Han, A. F. Young, B. Ozylmaz, P. Kim, and K. L. Shepard. Current saturation in zero-bandgap, top-gated graphene field-effect transistors. Nature Nanotechnology, 3(11):654–659, 2008.

[26] S. B. Mita, M. S. Choi, A. Nipane, F. Ali, C. Kim, J. T. Teherani, J. Hone, and W. J. Yoo. Electrical characterization of 2d materials-based field-effect transistors. 2D Materials, 8(1):012002, nov 2020.

[27] C. Mukherjee, J.-D. Aguirre-Morales, S. Frégonèse, T. Zimmer, and C. Maneux. Versatile compact model for graphene fet targeting reliability-aware circuit design. IEEE Transactions on Electron Devices, 62(3):757–763, 2015.

[28] E. Pop and F. Lian. Gfet tool, Jul 2011.

[29] S. Rodriguez, S. Vaziri, A. Smith, S. Frégonèse, M. Ostling, M. C. Lemme, and A. Rusu. A comprehensive graphene fet model for circuit design. IEEE Transactions on Electron Devices, 61(4):1199–1206, 2014.

[30] F. Schedin, A. K. Geim, S. V. Morozov, E. W. Hill, P. Blake, M. I. Katsnelson, and K. S. Novoselov. Detection of individual gas molecules adsorbed on graphene. Nature Materials, 6(9):652–655, Sep 2007.

[31] J. Schiefele, F. Solis, and F. Guinea. Temperature dependence of the conductivity of graphene on boron nitride. Phys. Rev. B, 85:195420, May 2012.

[32] F. Schierz. Graphene transistors. Nature Nanotechnology, 5(7):487–496, 2010.

[33] S. A. Thiele, J. A. Schaefner, and F. Schierz. Modeling of graphene metal-oxide-semiconductor field-effect transistors with gapless large-area graphene channels. Journal of Applied Physics, 107(9):094505, 2010.

[34] N. J. Tye, J. T. Meech, B. A. Bilgin, and P. Stanley-Marbell. A system for generating non-uniform random variates using graphene field-effect transistors. In 2020 IEEE 31st International Conference on Application-specific Systems, Architectures and Processors (ASAP), pages 101–108, 2020.

[35] A. Venugopali, J. Chan, X. Li, C. W. Magnuson, W. P. Kirk, L. Colombo, R. S. Ruoff, and E. M. Vogel. Effective mobility of single-layer graphene transistors as a function of channel dimensions. Journal of Applied Physics, 109(10):104511, 2011.

[36] L. Vicarelli, M. S. Vitiello, D. Coquillat, A. Lombardo, A. C. Ferrari, W. Knap, M. Polini, V. Pellegrini, and A. Tredicucci. Graphene field-effect transistors as room-temperature terahertz detectors. Nature Materials, 11(10):865–871, Oct 2012.

[37] H. Wang, Y. Wu, C. Cong, J. Shang, and T. Yu. Hysteresis of electronic transport in graphene transistors. ACS Nano, 4(12):7221–7228, 2010. PMID: 21047068.

[38] Y. Wu, Y.-m. Lin, A. A. Bol, K. A. Jenkins, F. Xia, D. B. Farmer, Y. Zhi, and P. Avouris. High-frequency, scaled graphene transistors on diamond-like carbon. Nature, 472(7341):74–78, Apr 2011.

[39] F. Xia, D. B. Farmer, Y.-m. Lin, and P. Avouris. Graphene field-effect transistors with high on/off current ratio and large transport band gap at room temperature. Nano Letters, 10(2):715–718, 2010. PMID: 20092332.

[40] Y.-J. Yu, Y. Zhao, S. Ryu, L. E. Brus, K. S. Kim, and P. Kim. Tuning the graphene work function by electric field effect. Nano Letters, 9(10):3430–3434, 2009. PMID: 19719145.

[41] Y. Zhang, T.-T. Tang, C. Girit, Z. Hao, M. C. Martin, A. Zettl, M. F. Crommie, R. Y. Shen, and F. Wang. Direct observation of a widely tunable bandgap in bilayer graphene. Nature, 459(7248):820–823, Jun 2009.

[42] W. Zhu, V. Perebeinos, M. Freitag, and P. Avouris. Carrier scattering, mobilities, and electrostatic potential in monolayer, bilayer, and trilayer graphene. Phys. Rev. B, 80:235402, Dec 2009.