An Ultra-Low Power TinyML System for Real-Time Visual Processing at Edge

Kunran Xu, Huawei Zhang, Yishi Li, Yuhao Zhang, Rui Lai, Member, IEEE, and Yi Liu

Abstract—Tiny machine learning (TinyML), executing AI workloads on resource and power strictly restricted systems, is an important and challenging topic. This brief firstly presents an extremely tiny backbone to construct high efficiency CNN models for various visual tasks. Then, a specially designed neural co-processor (NCP) is interconnected with MCU to build an ultra-low power TinyML system, which stores all features and weights on chip and completely removes both of latency and power consumption in off-chip memory access. Moreover, an application specific instruction-set is further presented for realizing agile development and rapid deployment. Extensive experiments demonstrate that the proposed TinyML system based on our tiny model, NCP and instruction set yields considerable accuracy and achieves a record ultra-low power of 160mW while implementing object detection and recognition at 30FPS. The demo video is available on https://www.youtube.com/watch?v=mIZPxtJ-9EY.

Index Terms—Convolutional neural network, tiny machine learning, internet of things, application specific instruction-set.

I. INTRODUCTION

RUNNING machine learning inference on the resource and power limited environments, also known as Tiny Machine Learning (TinyML), has grown rapidly in recent years. It is promising to drastically expand the application domain of healthcare, surveillance, and IoT, etc [1], [2]. However, TinyML presents severe challenges due to large computational load and memory demand of AI models, especially in vision applications. Popular solutions using CPU+GPU architecture has shown high flexibility in MobileML applications [3], but it is no longer feasible in TinyML for the much stricter constraints on hardware resources and power consumption. A typical TinyML system based on microcontroller unit (MCU) usually has only < 512KB on-chip SRAM, <2MB Flash, <1GOp/s computing capability, and <1W power limitation [2], [4]. Meanwhile, it is difficult to use off-chip memory (e.g., DRAM) in TinyML system for the very limited energy budget, showing a huge gap between the desired and available storage capacity for running visual AI models.

Recently, the continuously emerging studies on TinyML achieve to deploy CNNs on MCUs by introducing memory-efficient inference engines [1], [4] and more compact CNN models [5], [6]. However, the existing TinyML systems still struggle to implement high-accuracy and real-time inference with ultra-low power consumption. Such as the state-of-the-art MCUNet [1] obtains 5FPS on STM32F746 but only achieves 49.9% top-1 accuracy on ImageNet. When the frame rate is increased to 10FPS, the accuracy of MCUNet further drops to 40.5%. What’s more, running CNNs on MCUs is still not an extremely power-efficient solution due to the low efficiency of general purpose CPU in intensive convolution computing and massive weight data transmission. Considering this, we propose to greatly promote TinyML system by jointly designing more efficient CNN models and specific CNN co-processor. Specifically, we firstly design an externally tiny CNN backbone EtinyNet aiming at TinyML applications, which has only 477KB model weights and maximum feature map size of 128KB and still yields remarkable 66.5% ImageNet Top-1 accuracy. Then, an ASIC-based neural co-processor (NCP) is specially designed for accelerating the inference. Since implementing CNN inference in a fully on-chip memory access manner, the proposed NCP achieves up to 180FPS throughput with 73.6mW ultra-low power consumption. On this basis, we propose a state-of-the-art TinyML system shown in Fig. 2 for visual processing, which yields a record low power of 160mW in object detecting and recognizing at 30FPS.

Manuscript received 13 December 2022; accepted 14 January 2023. Date of publication 23 January 2023; date of current version 30 June 2023. This work was supported in part by the National Key Research and Development Program of China under Grant 2018YF070202000, and in part by the Natural Science Foundation of China (NSFC) under Grant 61674120. This brief was recommended by Associate Editor W. Zhao. (Kunran Xu and Huawei Zhang contributed equally to this work.) (Corresponding author: Rui Lai.)

Kunran Xu, Huawei Zhang, Yishi Li, Yuhao Zhang, and Rui Lai are with the School of Microelectronics, Xidian University, Xi’an 710071, China, and also with the Chongqing Innovation Research Institute of Integrated Circuits, Xidian University, Chongqing 400031, China (e-mails: aazzttcc@gmail.com; myyzhww@gmail.com; yshlee1994@outlook.com; styuyh@163.com; rla@mail.xidian.edu.cn).

Yi Liu is with the School of Microelectronics, Xidian University, Xi’an 710071, China, and also with the Guangzhou Institute of Technology, Xidian University, Guangzhou 510555, China (e-mail: yiliu@mail.xidian.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCSII.2023.3239044.

Digital Object Identifier 10.1109/TCSII.2023.3239044
In summary, we make the following contributions:
1) An extremely tiny CNN backbone named EtinyNet is specially designed for TinyML. It is far more efficient than existing lightweight CNN models.
2) An efficient neural co-processor (NCP) with specific designs for tiny CNNs is proposed. While running EtinyNet, NCP provides remarkable processing efficiency and convenient interface with extensive MCUs via SDIO/SPI.
3) Building upon the proposed EtinyNet and NCP, we promote the visual processing TinyML system to achieve a record ultra-low power and real-time processing efficiency, greatly advancing the TinyML community.

II. Solution of Our TinyML System

Fig. 1 shows the overview of the proposed TinyML system. It integrates MCU with the specially designed energy-efficient NCP on a compact board to achieve superior efficiency in a collaborative work manner. To the best of our knowledge, we are the first to propose such a collaborative architecture in TinyML field, which successfully balances the efficiency and flexibility in the inference.

Initially, MCU sends the model weights and instructions to NCP who has sufficient on-chip SRAM to cache all these data. During inference, NCP computes the intensive CNN backbone as indicated in Fig. 3(c), where $\phi_1$ is defined as

$$O = \sigma(\phi_2(\sigma(\phi_p(\phi_d(I))))))$$  \hspace{1cm} (1)

As shown in Fig. 3(a), the structure of proposed LB can be represented as $DCWconv-PWCconv-DCWconv$, which is apparently different from the commonly used bottleneck block of $PWCconv-DCWconv-PWCconv$ in mobile models, explained by the fact that increasing the proportion of $DCWconv$ is beneficial to the accuracy of tiny models.

Additionally, we introduce the dense connection into LB for increasing its equivalent width, which is important and necessary for a higher accuracy [8], as well as the very limited size of features and weights. We refer the resulting block to Dense Linear Depthwise Block (DLB) depicted in Fig. 3(b). Note that we take the $\phi_d$ as a whole due to the removal of ReLU, and add the shortcut connection at the ends of these two layers.

B. Architecture of EtinyNet Backbone

By stacking LBs and DLBs, we configure the EtinyNet backbone as indicated in Fig. 3(c), where $n$, $c$ and $s$ represent block repeated times, the number of output channels, and to the innovative model (EtinyNet), co-processor (NCP) and application specific instruction-set, the entire system yields both of efficiency and flexibility.

III. Parameter-Efficient EtinyNet Model

Since NCP handles CNN workloads entirely on-chip for pursuing extreme efficiency, we focus on reducing the model size for satisfying the memory constrains of IoT devices in TinyML, which is totally different from MobileML targeting at the reduction of MAdds. By presenting Linear Depthwise Block (LB) and Dense Linear Depthwise Block (DLB), we derive an extremely tiny CNN backbone EtinyNet, shown in Fig. 3.

A. Design of Proposed Blocks

We present the linear depthwise convolution by removing the ReLU behind $DCWconv$ of $\phi_1$ under the observation that this non-linearity harms accuracy in the design of extremely parameter-efficient architectures, forming a specific case of sparse coding. Then, we introduce additional $DCWconv$ of $\phi_2$ behind $PWCconv$ of $\phi_p$ to build a novel linear depthwise block (LB) by utilizing $DCWconv$'s parameter efficiency [7]. The LB is defined as

$$O = \sigma(\phi_2(\sigma(\phi_p(\phi_d(I))))))$$  \hspace{1cm} (1)

As shown in Fig. 3(a), the structure of proposed LB can be represented as $DCWconv-PWCconv-DCWconv$, which is apparently different from the commonly used bottleneck block of $PWCconv-DCWconv-PWCconv$ in mobile models, explained by the fact that increasing the proportion of $DCWconv$ is beneficial to the accuracy of tiny models.

Additionally, we introduce the dense connection into LB for increasing its equivalent width, which is important and necessary for a higher accuracy [8], as well as the very limited size of features and weights. We refer the resulting block to Dense Linear Depthwise Block (DLB) depicted in Fig. 3(b). Note that we take the $\phi_d$ as a whole due to the removal of ReLU, and add the shortcut connection at the ends of these two layers.

B. Architecture of EtinyNet Backbone

By stacking LBs and DLBs, we configure the EtinyNet backbone as indicated in Fig. 3(c), where $n$, $c$ and $s$ represent block repeated times, the number of output channels, and...
that could run without off-chip DRAM. The extreme compactness of EtinyNet makes it possible to design small footprint NCP backbone has only 477KB parameters and still achieves 66.5% ImageNet Top-1 accuracy. The first layer’s stride in each block (other layers’ stride equaling one) respectively. Since dense connection consumes more memory space, we only utilize DLB at high level stages with much smaller feature maps. It’s encouraging that EtinyNet backbone has only 477KB parameters and still achieves 66.5% ImageNet Top-1 accuracy. The extreme compactness of EtinyNet makes it possible to design small footprint NCP that could run without off-chip DRAM.

IV. APPLICATION SPECIFIC INSTRUCTION-SET FOR NCP

For easily deploying tiny CNN models on NCP, we define an application specific instruction-set. As shown in Table I, the set contains 13 instructions, belonging to neural operation type and control type respectively. It includes basic operations for tiny CNN models, and each instruction consists of 128 bits: 5 bits for operation code, and the rest for attributes of operations and operands. With each neural type instruction encoding an entire layer, the proposed instruction-set has a relatively coarser granularity, which simplifies the control complexity of hardware. Moreover, the basic operations included in the instruction-set provide sufficient ability to execute commonly-used CNN architectures (e.g., MobileNetV2 [9], MobileNeXt [10], etc).

V. DESIGN OF NEURAL CO-PROCESSOR

As shown in Fig. 4, the proposed NCP consists of five main components: Neural Operation Unit (NOU), Tensor Memory (TM), Instruction Memory (IM), I/O and System Controller (SC). When NCP works, SC decodes one instruction fetched from IM and informs the NOU to start computing with decoded signals. The computing process takes multiple cycles, during which NOU reads operands from TM and writes results back automatically. Once completing the writing back process, SC continues to process the next instruction until an end or suspend instruction is encountered. When NOU is idle, TM is accessed through I/O. We will fully describe each component in the following parts.

A. Neural Operation Unit

CNN workloads mainly come from operations of int8 conv, dwconv and float32 bn. To achieve a high energy efficiency, we respectively design special hardware units, termed NOU-conv, NOU-dw and NOU-post, focusing on optimizing the implementation of each operation. Furthermore, we deal with the design details in the following three aspects.

1) Different from other designs [11], [12] with fine grained instructions, we implement NOU-conv with a hardwired matrix multiply-accumulate (MAC) [13] array, which helps to improve efficiency with a simpler control logic. The MAC array is designed to perform matrix outer product with parallelism in spatial and output channel dimension for handling the most computational costly $3 \times 3$ Conv and PWConv with $im2col$ operation. In this way, the number of effective multiplications in each cycle is fixed to $T_{oc} \times T_{bw}$. Note that the number of channels varies across different convolution layers, which may lead to inefficient computation for other ways of implementation (e.g., dot product). Conversely, our implementation manner can avoid the above-mentioned problem and improve the overall efficiency in running PWConv of entire network. Moreover, the addition is realized by simple accumulation process instead of commonly-used adder tree with extra hardware overhead.

2) As for the implementation of DWConv, the above designed MAC array proves its efficiency only in diagonal units. Given this, we turn to the classical convolution processing pipeline [14], where nine multipliers and eight adders are arranged to compute DWConv in each channel. The independence between channels allows us to extend pipelines easily, implementing a parallelism of $T_{oc}$ to build NOU-dw. Since the feature length in spatial dimension is usually much larger than the pipeline depth, the DWConv can be performed in a fully pipelined manner, which yields NOU-dw an ultra high efficiency up to nearly 100%.

3) In NOU-post unit, modules of int2float, float32 multiply-add, float2int and ReLU are designed and interconnected to perform post-operations of float32 BN, ReLU and element-wise addition. To reduce memory access as much as possible, multiplexers are further utilized to select data from the output of NOU-conv, NOU-dw or TM, and connect modules as needed, allowing flexible fusion of post-operations with the previous convolution layer. By implementing $T_{oc}$ pipelines to match the throughput of convolution, we effectively maximize the efficiency of fusion operations.

B. Tensor Memory and Tensor Layout

1) TM is a single-port SRAM consisting of 6 banks, whose width is $T_{im} \times 8$ bits, as shown in Fig. 4. Thanks to the compactness of EtinyNet, NCP only requires totally 992KB on-chip SRAM. The BankI (192KB) is responsible for caching
The proposed layout conversion circuit is shown in Fig. 6. It consists of two register arrays 

A and B, working in a ping-pong mechanism. At the beginning, array A receives $T_{oc}$ inputs at a time, after $Thw$ cycles, A will be filled and start to output $Thw$ results at a time in the transposed dimension. Since reading A empty requires $T_{oc}$ cycles, the new coming data to be converted will be sent to array B in order to maintain the pipeline. When B is full and A completes the readout, the role of them are exchanged. This strategy obviously boosts the efficiency of valid memory access for computing.

C. Characteristics

We implement our NCP using TSMC 65nm low-power technology. While $T_{bm} = 32$, $T_{oc} = 16$ and $T_{hw} = 32$, NCP contains 512 of 8-bit MACs in NOU-conv, 144 of 8-bit multipliers and 16 of adder trees in NOU-dw, and 16 of float32 MACs in NOU-post. When running at the maximum frequency of 250MHz, NOU-conv and NOU-post are active every cycle, achieving a peak performance of 264 GOP/s.

VI. EXPERIMENTAL RESULTS

A. EtinyNet Evaluation

Table II lists the ImageNet-1000 classification results of well-known lightweight CNNs, including MobileNetV2 [9], MobileNetX [10], ShuffleNetV2 [15], and MCUNet series [16]. We pay more attention to the backbone because the fully-connected layer is generally not involved in most of visual models. Among these competitive models, MCUNet gets the highest accuracy at the cost of model size up to 2048K. Compared with tiny models in similar size, our EtinyNet reaches 66.5% top-1 and 86.8% top-5 accuracy, outperforming the most competitive MCUNetV2-M4 by significant 1.6% top-1 accuracy. Moreover, EtinyNet-0.75, the width of each layer is shrunk by 0.75, outperforms MCUNet-320kB by significant 2.6% top-1 accuracy with 60K fewer parameters. Obviously, EtinyNet yields much higher accuracy at the same level of storage consumption, and is more suitable for TinyML systems.

B. NCP Evaluation

As shown in Table III, running general CNN models usually needs DRAMs to store their enormous weights and features [11], [18], resulting in considerable power consumption and processing latency. As for no DRAM access methods, YodaNN [17] yields the highest peak performance and energy efficiency, but it is a dedicated accelerator only for binarized networks with very limited accuracy. Except that, Vega [12] gets the lowest power and the maximum latency, which leads
In addition, we benchmark the object detection performance on Pascal VOC dataset. The results indicate that our system also greatly improves its performance, which makes AIoT more promising in extensive applications.

VII. CONCLUSION

In this brief, we propose an ultra-low power TinyML system for real-time visual processing by designing 1) an extremely tiny CNN backbone EtinyNet, 2) an ASIC-based neural co-processor and 3) an application specific instruction-set. Our study greatly advances the TinyML community and promises to drastically expand the application scope of AIoT.

REFERENCES

[1] J. Lin, W.-M. Chen, Y. Lin, J. Cohn, C. Gan, and S. Han, “MCUNet: Tiny deep learning on IoT devices,” in Proc. Adv. Neural Inf. Process. Syst. Vol. III, 2020, pp. 11711–11722.
[2] M. Shafique, T. Theocharides, V. J. Reddi, and B. Murmann, “TinyML: Current progress, research challenges, and future roadmap,” in Proc. 58th ACM/IEEE Design Autom. Conf. (DAC), 2021, pp. 1303–1306.
[3] S. Mittal, “A survey on optimized implementation of deep learning models on the NVIDIA jetson platform,” J. Syst. Architect., vol. 97, pp. 428–442, Aug. 2019.
[4] L. Bai, N. Suda, and V. Chandra, “CMSIS-NN: Efficient neural network kernels for arm cortex-M CPUs,” 2018, arXiv:1801.06601.
[5] C. Banbury et al., “MCUNetV2: Neural network architectures for deploying tinyML applications on commodity microcontrollers,” in Proc. Mach. Learn. Syst., vol. 3, 2021, pp. 517–532.
[6] R. T. N. Chappa and M. El-Sharkawy, “Deployment of SE-squeezeNext on NXP bluebox 2.0 and NXP i.MX RT1060 MCU,” in Proc. IEEE Midwest Ind. Conf. (MIC), vol. 1, 2020, pp. 1–4.
[7] K. Xu, Y. Li, H. Zhang, R. Bai, and L. Gu, “EtinyNet: Extremely tiny network for tinyML,” in Proc. AAKJ Conf. Artif. Intell., 2022, pp. 4626–4636.
[8] S. Zagoryuky and N. Komodakis, “Wide residual networks,” 2016, arXiv:1605.07146.
[9] M. Sandler, A. G. Howard, M. Zhu, A. Zhmoginov, and L.-C. Chen, “MobileNetV2: Inverted residuals and linear bottlenecks,” in Proc. IEEE Comput. Soc. Annu. Symp. VLSI (ISVLSI), 2018, pp. 402–405.
[10] D. Zhou, Q. Hou, Y. Chen, J. Feng, and S. Yan, “Rethinking bottleneck structure for efficient mobile network design,” in Proc. Eur. Conf. Comput. Vis., 2020, pp. 680–697.
[11] A. Bytyn, R. Leupers, and G. Ascheid, “ConvAix: An application-specific instruction-set processor for the efficient acceleration of CNNs,” IEEE Open J. Circuits Syst., vol. 2, pp. 3–15, Nov. 2020.
[12] D. Rossi et al., “Vega: A ten-core SoC for IoT endnodes with DNN acceleration and cognitive wake-up from MRAM-based state-retentive sleep mode,” IEEE J. Solid-State Circuits, vol. 57, no. 1, pp. 127–139, Jan. 2022.
[13] M. E. Nojehdeh, S. Parvin, and M. Altun, “Efficient hardware implementation of convolution layers using multiply-accumulate blocks,” in Proc. IEEE Comput. Soc. Annu. Symp. VLSI (ISVLSI), 2021, pp. 402–405.
[14] T. Chen et al., “DianNao: A small-footprint high-throughput accelerator for ubiquitous machine-learning,” ACM SIGARCH Comput. Architect. News, vol. 42, no. 1, pp. 269–284, 2014.
[15] N. Ma, X. Zhang, H.-T. Zheng, and J. Sun, “ShuffleNet V2: Practical guidelines for efficient CNN architecture design,” in Proc. Eur. Conf. Comput. Vis. (ECCV), 2018, pp. 116–131.
[16] J. Lin, W.-M. Chen, H. Cai, C. Gan, and S. Han, “MCUNetV2: Memory-efficient patch-based inference for tiny deep learning,” 2021, arXiv:2110.15352.
[17] R. Andri, L. Cavigelli, D. Rossi, and L. Benini, “YodaNN: An architecture for ultrawide power binary-weight CNN acceleration,” IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 37, no. 1, pp. 48–60, Jan. 2018.
[18] A. Almair et al., “NullHop: A flexible convolutional neural network accelerator based on sparse representations of feature maps,” IEEE Trans. Neural Netw. Learn. Syst., vol. 30, no. 3, pp. 644–656, Mar. 2019.