GENIEx: A Generalized Approach to Emulating Non-Ideality in Memristive Xbars using Neural Networks

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ABSTRACT
Memristive crossbars have been extensively explored for deep learning accelerators due to their high on-chip storage density and efficient Matrix Vector Multiplication (MVM) compared to digital CMOS. However, their analog nature of computing poses significant issues due to various non-idealities such as: parasitic resistances, non-linear I-V characteristics of the memristor device etc. The non-idealities can have a detrimental impact on the functionality i.e. computational accuracy of crossbars. Past works have explored modeling the non-idealities using analytical techniques. However, several non-idealities have data dependent behavior. This cannot be captured using analytical (non data-dependent) models thereby, limiting their suitability in predicting application accuracy.

To address this, we propose a Generalized Approach to Emulating Non-Ideality in Memristive Crossbars using Neural Networks (GENIEx), which accurately captures the data-dependent nature of non-idealities. First, we perform extensive HSPICE simulations of crossbars with different voltage and conductance combinations. Based on the obtained data, we train a neural network to learn the transfer characteristics of the non-ideal crossbar. Next, we build a functional simulator which includes key architectural facets such as tiling, and bit-slicing to analyze the impact of non-idealities on the classification accuracy of large-scale neural networks. We show that GENIEx achieves low root mean square errors (RMSE) of 0.25 and 0.7 for low and high voltages, respectively, compared to HSPICE. Additionally, the GENIEx errors are 7x and 12.8x better than an analytical model which can only capture the linear non-idealities. Further, using the functional simulator and GENIEx, we demonstrate that an analytical model can overestimate the degradation in classification accuracy by ≥10% on CIFAR-100 and 3.7% on ImageNet datasets compared to GENIEx.

1 INTRODUCTION
The pervasiveness of deep learning in a wide-variety of applications such as object detection, language processing etc. has been a major force behind the recent success of Artificial Intelligence (AI). Consequently, there has been a growing interest in developing specialized accelerators to improve the efficiency of deep learning. Such accelerators include Google TPU [1], Microsoft BrainWave [2], and Nvidia V100. One key aspect driving these accelerators is moving computations closer to the memory, which has brought forth the paradigm of in-memory computing. Despite the breakthroughs in custom hardware, the storage and computation requirements of Deep Neural Networks (DNNs) have been increasing at a much faster rate than the efficiency improvements in digital CMOS hardware [3]. To this effect, researchers have explored Non Volatile Memory (NVM) [4, 5] based crossbar architectures to achieve higher on-chip storage density and efficient MVMs in the analog domain [6, 7].

NVM devices can store multiple states per device, and crossbars built with these devices can be integrated on chip leading to high storage density [4]. Second, the voltage-driven nature of these two-terminal devices enables crossbar-like arrangement to perform MVMs, at significantly higher efficiency compared to digital CMOS [8]. Despite the multifold promises of NVM technologies, the analog nature of computing in crossbars poses several challenges due to the device and circuit non-idealities such as: parasitic resistance, non-linearity from access transistors, and I-V characteristics of the NVM device. Parasitic resistances lead to undesirable IR-drops in the metal lines of the crossbar. On the other hand, the non-linearity leads to inaccurate multiplications at the cross-points. As a result, non-idealities can have an adverse effect on the MVM arithmetic. This gets exacerbated further due to the device variations. Eventually, the inaccuracies in the MVM arithmetic can accumulate over the multiple layers of a neural network, causing significant accuracy degradation [9].

To address this accuracy degradation, there have been efforts towards exploring techniques to model non-idealities and subsequently mitigating them [9–11]. The efficacy of these mitigation techniques strongly depend upon the modelling [9, 10, 12] approach to exhaustively capture the sources of the non-idealities and retraining of the neural network weights. The non-idealities in crossbars can be broadly categorized into non-data dependent or linear (for eg. parasitic resistances), and data-dependent or non-linear types (for eg. access transistors and device I-V characteristics). While the current analytical techniques can model the non-data dependent aspects [9, 10, 12], they fail to capture the data dependent non-idealities. Data-dependent non-idealities can have a pronounced effect on the crossbar outputs, particularly at higher operating voltages (discussed in Section 3). Thus, it is important to move away from approximate analytical models to data-based models in order to truly capture all the non-idealities. In this work, we present GENIEx, a neural network based modelling approach that provides an accurate as well as generalized representation of the non-ideal behavior of crossbars. The key contributions of this work are:

- Analyze the sources of non-ideality in crossbars through extensive SPICE simulations (Section 3).
- Propose GENIEx, a generalized approach for modelling non-idealities in crossbars using neural networks (Section 4).
TABLE 1: RELATED WORK COMPARISON

| Related Work | Linear • Non-linear Non-idealities | Large scale DNNs | Architecture model of MVM |
|--------------|-----------------------------------|------------------|--------------------------|
| GENIEx       | ✓                                 | ✓                | ✓                        |
| CxDNN [9]    | x                                 | ✓                | ✓                        |
| CrossSim [19]| ✓                                 | x                | x                        |
| NeuroSim [17]| ✓                                 | ✓                | x                        |
| AMS [18]     | x                                 | x                | x                        |

- Develop a PyTorch-based functional simulator which models the key architectural aspects namely tiling, and bit-slicing to evaluate large-scale DNNs using GENIEx (Section 5).
- Perform detailed analysis of different non-idealities on the classification accuracy of DNNs (Section 7).

To the best of our knowledge, this is the first work proposing an end-to-end framework for data-dependent crossbar modeling along with a functional simulator considering tiling, and bit-slicing. This enables studying the accuracy impacts of device and circuit properties at the application level. It is worth noting that due to the ability to capture data dependency of crossbar behavior (transfer characteristics), GENIEx can be used to model crossbars from both simulations as well as experimental measurements. We believe that our proposed approach paves the way for universal modeling of practical crossbars with the scope of seamless functional evaluation and mitigation. We plan to open-source the framework for further research on crossbar hardware.

2 RELATED WORK

Past research have explored modeling crossbar non-idealities and subsequently mitigating them [9–11, 13]. Jain et al [9] used matrix inversion techniques to model the effects of parasitic resistances due to input driver, metal lines etc. Liu et al [13] proposed an approximation technique based on sample input/output behavior. An alternative way of capturing effects such as stuck-at-faults [14] or device variations [15] is to map the distribution of the variations or defects. While the above modeling approaches [9, 13–15] consider linear (non-data dependent) non-idealities, GENIEx also captures the non-linear (data dependent) non-idealities. Note, there could be non-linearity during programming of NVM devices. Sun et al [16] propose analytical models to study such non-linearity during programming. However, analyzing the impact of non-linearity on the subsequent MVM computations (after programming) requires a data-dependent model like GENIEx.

Researchers have also proposed evaluation frameworks such as [9] and NeuroSim [17] to study the impact of these non-idealities using analytical models. Other works have explored the impact of quantization noise of ADCs for analog computing [18]. However, these frameworks do not consider the architectural aspects of MVM computations such as tiling and bit-slicing, which have a significant implication on classification accuracy (shown in Section 7.2). Our work explores a neural network based technique to model the crossbar non-idealities using a functional simulator with detailed MVM architecture. Table 1 summarizes our contribution with respect to the related work.

3 ANALYSIS OF NVM NON-IDEALITIES

**Background:** A typical memristive crossbar consists of NVM devices arranged in a crossbar fashion as shown in Figure 1. The two terminals of each NVM device connect to a horizontal word-line (WL) and a vertical bit-line (BL). These devices are accompanied by access transistors or selectors to avoid sneak path issues during writing [20]. This primitive can be used to compute Matrix Vector Multiplications (MVMs) in the analog domain by activating all the WLs and sensing all the BLs simultaneously. For example, to perform a multiplication between a $1 \times N$ vector and a $N \times M$ matrix, the vector is encoded as input voltages ($V_i$) while the matrix is encoded as conductances ($G_{ij}$). Consequently, the output current in the $j^{th}$ BL (for ideal crossbar) is the sum of currents through each NVM device in the corresponding column: $I_j = \sum_i V_i G_{ij}$. Thus, the currents from the $M$ columns constitute the output vector of the MVM operation. Typically, a crossbar requires peripheral circuits such as Digital-to-Analog Converters (DACs) and Analog-to-Digital Converters (ADCs) for system-level integration. The DACs convert the digital inputs into analog voltages while the ADCs convert the analog currents in the BLs to digital outputs. Due to the analog nature of computing, several non-idealities can lead to errors in the MVM computations. These non-idealities can be classified into two kinds - linear and non-linear, as shown in Table 2.

![Figure 1: A typical non-ideal crosspoint structure with NVM devices accompanied by a transistor at every junction of the word-lines (WL) and bit-lines (BL).](image)

**Table 2: Non-idealities in crossbar**

| Linear Non-idealities | Non-linear Non-idealities |
|-----------------------|---------------------------|
| Source Resistance ($R_{source}$) | Access devices or selectors |
| Sink Resistance ($R_{sink}$) | Device non-linearity |
| Wire Resistance ($R_{wire}$) | |

**Analysis:** Under the influence of non-idealities, the crossbar design parameters such as size, ON resistance, conductance ON/OFF ratio etc. can have a considerable effect on the magnitude of errors in computations. To analyze this effect, we perform SPICE analysis of a $64 \times 64$ crossbar. Herein, the linear non-idealities are modeled using parasitic resistances as shown in Figure 1. The access devices are based on transistor models from TSMC 65nm technology. The device models are adopted from a compact model of a filamentary RRAM [21], where the current flowing through the device can be expressed as: $I(d, V) = \lambda \exp(\frac{d}{d_0}) \sinh(\frac{V}{V_0})$. Here, $d$ is the gap-size between the tip of the filament and electrode, $d_0$, $d_0$ and $V_0$ are fitting parameters.

Figure 2 (a) shows a typical plot of ideal current ($I_{ideal}$) vs non-ideal current ($I_{non-ideal}$) of a crossbar. Here, we observe that different voltage ($V$) and conductance ($G$) conditions which lead to similar $I_{ideal}$ can result in a varying range of $I_{non-ideal}$ outputs, causing errors in computations. To quantify the error, we define...
a non-ideality factor (NF) as the relative error between the \( I_{\text{ideal}} \) and \( I_{\text{non-ideal}} \). NF is calculated as: 

\[
\text{NF} = \frac{I_{\text{ideal}} - I_{\text{non-ideal}}}{I_{\text{ideal}}}.
\]

We observe in Figures 2 (b) and (c) that lower ON resistances and higher crossbar sizes lead to higher NF. This is due to the fact that bigger crossbars have longer metal lines leading to higher \( R_{\text{wire}} \). Moreover, the parallel combination of resistances along the columns and rows results in a reduced effective resistance of the crossbar in case of bigger crossbars as well as low ON resistances. In addition, Figure 2 (d) shows that lower ON/OFF conductance ratio leads to high NFs. This is due to the fact that for a given ON resistance, the average resistance in the crossbar is low for lower ON/OFF ratio.

Next, we analyze the impact of non-linear non-idealities. We consider two cases i) only linear non-idealities, ii) both linear and non-linear non-idealities. Figures 3 (a) and (b) show the relative difference in output currents between the two cases. We observe that the output currents in case (i) vary noticeably from case (ii). This effect becomes even more prominent for higher supply voltage of \( V_{\text{supply}} = 0.5V \), thereby implying an inherent data dependence of \( I_{\text{non-ideal}} \) on the \( V \) and \( G \). This result underlines the drawbacks of analytical models which fail to capture the data-dependent non-idealities. We propose a neural network based modeling technique that captures the data-dependent errors in crossbar computations.

4 GENIEx - A NEURAL NETWORK BASED CROSSBAR MODEL

Neural networks project data to a high dimensional space which enables them to distinguish between different input patterns. We leverage this property of neural networks to propose GENIEx, which models the non-ideal behavior of memristive crossbars for different input voltage and conductance combinations. As discussed in Section 3, non-idealities in crossbars can lead to a varying range of NF for similar \( I_{\text{ideal}} \). Using a neural network can help us capture the data-dependent nature of such non-ideal behavior.

**NN Formulation:** The output current vector of an ideal crossbar \( (I_{\text{ideal}}) \) represents an MVM operation between \( V \) and \( G \). Meanwhile, the output current vector from a real crossbar is non-ideal and can be expressed as a distorted MVM function: \( I_{\text{non-ideal}} = f_{\text{D}}(V,G) \). Therefore, it represents multiplicative behavior between the input variables, \( V \) and \( G \). The objective here is to model such non-ideality function \( f_{\text{D}}(V,G) \) being input-dependent and having multiplicative behavior. The intuitive way of modeling \( f_{\text{D}}(V,G) \) using neural networks is to provide \( V \) and \( G \) as inputs and obtain \( I_{\text{non-ideal}} \) as output. However, as neural networks perform linear transformations, it is difficult for them to model multiplicative interactions between its inputs. To avoid such input multiplications, we propose extracting only the distortion information of the real output current from \( f_{\text{D}}(V,G) \). We define a function which represents the ratio of \( I_{\text{ideal}} \) to \( I_{\text{non-ideal}} \): \( f_{\text{E}}(V,G) = \frac{I_{\text{ideal}}}{I_{\text{non-ideal}}} \). \( f_{\text{E}}(V,G) \) represents the deviation of the \( I_{\text{non-ideal}} \) from \( I_{\text{ideal}} \), thus eliminating the need to capture multiplicative relationships. For an \( N \times N \) crossbar, the input vector to the neural network is a concatenation of \((N \times 1)\) voltage vector and \((N^2 \times 1)\) flattened conductance vector. The output vector obtained is \( f_{\text{E}}(V,G) \) which is of size \( N \times 1 \). Subsequently, the \( I_{\text{non-ideal}} \) is obtained using \( I_{\text{ideal}}/f_{\text{E}}(V,G) \).

**Dataset:** To train GENIEx for predicting the ratio \( f_{\text{E}}(V,G) \) for a set of \( V \) and \( G \) vectors, we create a dataset covering the exhaustive space of \( V \) and \( G \) combinations. Crossbar-based accelerators commonly use bit-slicing to perform high precision MVM operations [6, 7]. We observed this leads to high sparsity in \( V \) and \( G \) vectors across the popular deep learning tasks. To exhaustively capture the resulting sparse data distributions, we consider various degrees of sparsity while generating the training set of \( V \) and \( G \). We apply the \( V \) and \( G \) vectors to various crossbars and perform SPICE simulations to obtain the corresponding \( I_{\text{non-ideal}} \). The obtained \( I_{\text{non-ideal}} \) is used to calculate \( f_{\text{E}}(V,G) \), the prediction labels for the dataset. To evaluate the accuracy of GENIEx, we create a separate validation set of \( V \), \( G \) and expected \( f_{\text{E}}(V,G) \).

**NN Topology:** GENIEx considers a two layer fully-connected neural network consisting of an input layer, a hidden layer and an output layer. For a \( N \times N \) crossbar, the size of the neural network is given as: \((N^2 + N) \times P \times N\), where \( P \) is the number of neurons in the hidden layer. The training set mentioned above is used to train the neural network by feeding \( V \), \( G \) combinations as inputs and \( f_{\text{E}}(V,G) \) as the output.

**Benchmarking:** We compare the accuracy of GENIEx against HSPICE results and a baseline linear analytical model for the same test voltage and conductance combinations. We use the metric \( NF \), defined in Section 3, to compare the models with HSPICE.
5 FUNCTIONAL SIMULATOR

Several frameworks such as Ares [22], Distiller [23] etc. have been developed using TensorFlow and PyTorch to enable hardware-software codesign studies. However, such frameworks cannot emulate the implications of crossbar-based hardware, because of the intrinsic differences in the CMOS-based and Crossbar-based computation models. For CMOS, matrix operations (ops) in a ML model are expressed as General Matrix-Matrix Multiplications (GEMMs) that use floating/fixe point compute units, whereas Crossbar requires matrix ops expressed as Matrix-Vector Multiplications (MVM) that use bit-serial compute units [6, 7]. To address this, we design a functional simulator using PyTorch that implements the `conv2d` (convolution) and `linear` (fully connected) layers based on the crossbar-based computation (conv2d-mvm, linear-mvm).

Functional Simulator. As shown in Figure 6, the execution of a convolution layer is divided into three phases within the functional simulator: Iterative-mvm, Tiling, and Bit-slicing. Each phase depends on parameters that either capture the layer or architecture details pertinent to MVMs. Consequently, we extract the analog computing aspect of crossbar hardware and ignore any impact of memory and communication. First, Iterative-mvm expresses a convolution as repeated MVMs, where the weights forms the matrix and a block of pixels across all input channels form the vector (for an iteration). Each iteration produces an output vector which is comprised of one pixel from all output channels. Second, Tiling expresses the weight-matrix as a combination of several sub-matrices (or tiles) where, each sub-matrix’s size equals the crossbar size. A slice of input vector is shared by tiles in a row. Tiles in a column produce partial sums, which are added together to produce a slice of the convolution output. Third, Bit-slicing (both input and weight bits) expresses the bit-serial nature of crossbar computations [6, 7]. We will refer to a bit-slice (∋ 1 bit) of inputs and weights as stream and slice, respectively. Within each step, an input stream is applied to a crossbar’s rows to produce ADC outputs. Next, the shift-and-add units merge the ADC outputs of different weight slices. Eventually, the outputs of successive input streams go through shift-and-add units to produce the partial sums for a tile. Depending on the simulation mode (ideal or non-ideal), the ADC outputs are generated either by actual dot-product computation or a forward pass of GENIEx discussed in Section 4. In summary, the three phases together provide the projection of a layer’s execution on actual crossbar hardware.

PyTorch Modelling. The weight-matrix and input-vectors are modelled as multi-dimensional tensors of shape - (Slices, Tr, Tc, Xr, Xc), and (Batch Size, Tr, Xr, Streams), respectively. Here, the symbols - T, X, r, and c refer to a tile, crossbar, row and column. Accordingly, Tr refers to a “tile row” and so on. The tensor operations `torch.mul` and `torch.sum` execute the individual crossbar operations. Subsequently, reduction across the weight slices (Slices) and input streams (Streams) with scalar factors for shift-and-add generates the partial products. Subsequently, reduction across Tr dimension produces the convolution output. Multiple input vectors corresponding to different iterations of MVM are implemented as a batch of vectors (Batch Size). Table 3 lists the layer and architecture parameters supported by the functional simulator.

6 EXPERIMENTAL METHODOLOGY

Crossbar: We simulate memristive crossbars using HSPICE. The test vectors for V and G are collected from the dataset (CIFAR-100 and ImageNet) and the pretrained network models (ResNet) respectively. $l_{\text{non-ideal}}$ obtained from SPICE simulations is used to calculate the non-ideality ratio, $f_R$, described in Section 4. Finally, V, G and $f_R(V, G)$ are normalized to the range [0, 1] to form the training set for GENIEx. To verify the generalization and applicability of GENIEx, we generated datasets for crossbar configurations with different design parameters such as crossbar size (16, 32, 64), ON resistance (50kΩ, 100kΩ, 300kΩ), and conductance ON/OFF ratio.
(2, 6, 10). The non-ideality parameters are $R_{\text{source}} = 500\Omega/1000\Omega$, $R_{\text{sink}} = 1000\Omega/500\Omega$, $R_{\text{wire}} = 2.5\Omega$ per cell. The device parameters are $d_0 = 0.25nm$, $V_0 = 0.25V$, $I_0 = 0.1mA$ [24, 25].

**Functional Simulator:** The precisions of different components of the functional simulators are as follows: accumulator = 32-bit (24 fractional), ADC = 14-bit, inputs and weights = 16-bit (13 fractional), input Streams = 4-bit, weight Slices = 4-bit, unless otherwise specified. All networks use fixed-point (FxP) representations.

**DNN:** GENIEx has 500 hidden layer neurons and ReLU non-linearity [26]. We use PyTorch to evaluate large-scale neural networks on the functional simulator using GENIEx. For the CIFAR-100 dataset, we use the network architecture ResNet-20. For the ImageNet dataset, we considered ResNet-18 on a subset of 7680 test images of the dataset. We report the top-1 accuracies for both datasets. The ideal floating point 32-bit (FP) accuracies for CIFAR-100 and subset of ImageNet are 69.6% and 76.01% respectively.

### 7 RESULTS

#### 7.1 Impact on Design Parameters

First, we study the impact of non-idealities on the classification accuracy of DNNs under different design considerations of crossbar sizes, ON resistances, and conductance ON/OFF ratio. The studies are performed on ResNet-20 for CIFAR-100 dataset with the features of bit-slicing and bit-streaming using 4-bit Streams and Slices. The weights and activations for these networks have been considered as 16-bit fixed point representations.

We observe in Figure 7 (a) that the classification accuracy degrades by 12% for a $64 \times 64$ crossbar compared to an ideal 16 bit fixed-point (Ideal FxP) implementation. However, for lower crossbar sizes like $16 \times 16$, the degradation is ≤ 1%. This is due to reduced effective resistance for higher crossbar sizes, as discussed in Section 3. For higher ON resistances such as $300k\Omega$, we observe, in Figure 7 (b) that the accuracy degradation is 7.6% lower than the case with $100k\Omega$. This is because the parasitic resistances have more pronounced effect on crossbars with lower ON resistances, resulting in higher accuracy degradation. In 7 (c), we observe that for a given ON resistance ($100k\Omega$ in this case), lower ON/OFF ratio like 2 results in up to 46% degradation in accuracy due to the average resistances in the crossbar being low. With higher ON/OFF ratio such as 10, the accuracy degradation reduces to 8.6%.

Figure 7 (d) shows that there is a significant difference between the accuracies predicted by an analytical model and GENIEx. Further, it also illustrates that an analytical model overestimates the accuracy degradation by 12.34% for supply voltage, $V_{\text{supply}} = 0.25V$ and 11.6% for $V_{\text{supply}} = 0.5V$ compared to GENIEx. Note that the analytical model considers only linear non-idealities (parasitic resistances). It underscores that the device non-linearity which is captured by our model can push the behavior of the crossbar towards ideality, thus resulting in a lower accuracy degradation.

Figure 8: Impact of precision of weights and activations on classification accuracy under the influence of non-idealities.

Figure 8 (d) shows that the impact of non-idealities with crossbar design parameters (a) Crossbar Size, (b) ON resistance, (c) ON/OFF ratio, (d) Comparison between analytic model and GENIEx.
We present GENIEx, a generalized approach to emulating non-ideal crossbars. We study the effect of non-idealities on DNNs with different bit-precisions for weights and activations being 16-bit, 8-bit, and 4-bit with very high sparsity that makes the crossbar resilient to parasitic non-idealities. The proposed end-to-end framework for evaluating crossbar designs for future machine learning systems.

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