Fast and simple model generation for superjunction power MOSFETs

An easy way to get accurate SPICE models even without precise information from the data sheet

M. Fuchs, L. Spielberger, K. Odreitz, B. Deutschmann

This paper describes a new way to create a behavioral model for power MOSFETs with highly nonlinear parasitic capacitances like those based on superjunction (SJ) principles. The process ranges from a simple measurement to the final model for SPICE simulations. One of the benefits of the proposed modeling technique is that it does not require any information about the voltage-dependent capacitances of the MOSFET from the data sheet but instead relies on a simple measurement method using a vector network analyzer. The measurement data can be used for modeling all parasitic capacitances and inductances in the SPICE model. Compared to existing simulation models by the manufacturer, the proposed model promises better convergence, more accurate high-frequency behavior and faster simulation time. The advantages and disadvantages of this modeling technique are discussed.

Keywords: superjunction; power MOSFET; SPICE; modeling; power electronics

1. Introduction

Today, modern switched power electronic systems can be found in a variety of applications such as AC adapters, solar inverters, battery chargers, variable frequency motor drives, etc. They include modern power semiconductor switches which are increasingly based on superjunction techniques, silicon carbide (SiC) or gallium nitride (GaN) semiconductors. In simulations, it is becoming increasingly important to better represent the high-frequency behavior of MOSFETs. This makes it possible, for example, to take a closer look at control problems caused by strong load changes or to simulate the conducted electromagnetic emissions of an electronic system. In [1] it is described that one of the main challenges for accurate electromagnetic emission simulations is that the generated noise in a power electronic system is highly dependent on the circuit and semiconductor parasitics.

For accurate SPICE simulations in power electronics, accurate models of power MOSFETs are therefore essential. In many cases, manufacturers do not provide such models at all, or not for common SPICE simulators like LTSpice. Manufacturer models are also mostly analytical models which are based on precise physical knowledge of the internal structure, like shown in [2]. To generate such models without this knowledge, so-called behavioral models are commonly used [3–5].

This paper shows how behavioral models for SPICE simulation can be created using a simple measurement with a vector network analyzer (VNA). A special focus is put on modeling the voltage-dependent parasitic capacitances of superjunction (SJ) MOSFETs since they are highly nonlinear and therefore difficult to imposi-
Fast and simple model generation for superjunction power MOSFETs

2. Measurements

As described in [7], all parasitic capacitances and inductances required for a behavioral model of a power MOSFET with three pins can be determined by a single S-parameter measurement using a VNA. The measuring system shown in Fig. 1, which is described in great detail in [8], additionally offers the possibility to measure these parasitic capacitances voltage dependent. The power MOSFET is depicted with all parasitics. These include the voltage-dependent parasitic capacitances $C_{GD}$, $C_{GS}$ and $C_{DS}$ as well as parasitic terminal inductances of the bonding wires $L_D$, $L_S$ and $L_T$. The VNA is protected by two DC blocks from the high voltage source $V_{DS}$. The HF-filters prevent the measurement from being influenced by $V_{DS}$ which is stepped over the first 100 V in 1 V steps. From the obtained voltage-dependent S-parameters, the parasitic inductances as well as the voltage-dependent capacitances can be calculated in one single step. The extraction of the capacitances from the S-parameter measurements can be done at any frequency below the resonant frequency; the extraction of the inductances at any frequency above the resonant frequency. Secondary effects such as temperature or frequency dependence of the parasitics were thoroughly tested and can be excluded. Likewise, no significant fabrication tolerances could be determined by measurements on various components although such tolerances are not ruled out. For this specific power MOSFET, the S-parameters were sampled at a frequency of 10 MHz to calculate the capacitances because the S-parameter measurement was most accurate over the whole drain-source voltage range there. In a similar way, as it is described in [7], the equations (2) and (3) show this calculation using the drain-source capacitance as an example. The parasitic inductances are sampled at 1 GHz and are calculated similarly. These values are constant and amount to $L_D = 0.2 \, \text{nH}$, $L_S = 3.5 \, \text{nH}$ and $L_T = 1 \, \text{nH}$ for the given model.

Figure 2 shows the result of the measurements of the voltage-dependent input ($C_{GS}$), output ($C_{GS}$) and reverse transfer ($C_{DS}$) capacitances in comparison with the data sheet up to a drain-source voltage of 100 V, above which the values do not change significantly anymore. These capacitances are defined in terms of the equivalent circuit capacitances as:

$$C_{GS} = C_{DS} + C_{GD} \quad \text{(with } C_{GD} \text{ shorted)};$$

$$C_{DS} = C_{GD}; \quad C_{DS} = C_{DS} + C_{GD} \quad (1)$$

where $C_{GS}$ is referred to the capacitance due to the overlap of the source and the channel regions by the polysilicon gate and is more or less independent of the applied drain source voltage ($V_{DS}$).

$C_{GD}$ often consists of two parts. The first part of this capacitance is defined by the overlap of the gate (e.g. polysilicon) and the semiconductor material underneath in the drift region. The second part is associated with the depletion region under the gate. $C_{GD}$ is a non-linear function of the drain-source voltage. $C_{DS}$ is the capacitance associated with the body diode and strongly depends on the drain-source voltage.

The difference in the measured values of the reverse transfer capacitance $C_{DS}$ in Fig. 2 can be attributed to the insufficient measuring dynamics of the VNA used for the measurement. The measurement dynamics of a more modern VNA would be sufficient to measure this capacitance more accurately. However, as shown in Sect. 4, it turns out that these differences do not have a great influence on the resulting model. The small deviation of $C_{DS}$ from the data sheet values at approx. 25 V was confirmed by several measurements of different components of the same type. Furthermore, a linear extrapolation seems to be sufficient for all capacitance values above
Fig. 3. Illustration of the MOSFET model for LTspice. The parasitic capacitances, as well as the behavior of the MOSFET and the body diode, are modeled with the help of voltage controlled current sources.

100 V.

$$X_{CS} = \frac{2S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \cdot Z_0$$  \hspace{1cm} (2)

$$C_{DS} = \frac{2\pi f \cdot X_{CS}}{X_{CS}X_{CG} + X_{CS}X_{CS} + X_{CS}X_{CG}}$$  \hspace{1cm} (3)

3. Model creation in LTspice

Almost the entire model can be represented by voltage controlled current sources which provide several advantages compared to the models that are usually provided by the IC manufacturers. The entire model is shown in Fig. 3. In the following, modeling of the individual components is described.

3.1 Modeling of voltage-dependent parasitic capacitances

For modeling the nonlinear, voltage-dependent capacitance changes within the first 50 V are crucial since here especially the output capacity $C_{oss}$ and the reverse capacity $C_{rss}$ change by several orders of magnitude.

Looking at the measurement curves in Fig. 2 it becomes clear that a mathematical modeling of the capacity changes, like it is done in [3], becomes difficult to impossible in this case. Especially the nonlinearities around $V_{DS} = 25$ V, where the capacity values decrease by several decades, are very difficult to describe with sufficient accuracy by a function that interpolates the real curve. Doing so would most likely lead to sacrificing either simulation time or reliable convergence. For this reason, a table-based procedure based on the measurement results of Sect. 2 is presented.

The capacitances in Fig. 1 can be simulated in LTspice with the help of voltage controlled current sources. The values of the capacitances, which depend on $V_{DS}$, are passed to the simulator in form of a table which lists the corresponding capacitance in relation to $V_{DS}$. A voltage controlled current source models the behavior of the parasitic capacity ($C_{GSS}$, $C_{GS}$ and $C_{DSS}$ in Fig. 3) using the following equation as an example for $C_{DSS}$:

$$C_{DSS} = C_{DSS}(V_{DS}) \frac{dV_{DS}}{dt}$$  \hspace{1cm} (4)

The values are read by a voltage controlled voltage source ($V_{CGS}$, $V_{CGD}$ and $V_{CDSS}$ in Fig. 3) by using a classical look-up table whose interpolated output voltage is used in equation (4) for the values of $C_{DSS}(V_{DS})$.

3.2 Modeling of output characteristic

The output characteristic $I_D = f(V_{DS}, V_{GS})$ of the MOSFET and the forward characteristic $I_F = f(V_{GD})$ of the body diode are modeled with voltage controlled current sources as well. The characteristic curves and the threshold voltage $V_{T_D}$ can usually be taken from the data sheet or can be measured alternatively. The threshold voltage $V_{T_D}$, the on-resistance $r_{DSon}$ and two drain current values $I_{D1}$ and $I_{D2}$ with their respective gate-source voltages $V_{G1}$ and $V_{G2}$ at a certain drain-source voltage are passed to the model.

In the linear region, the output characteristic follows the root function in equation (5). Within the saturation region, the drain current is calculated by equation (6). The unknown parameters $c$ and $r$ are derived in equations (7) and (8). Right now, the temperature dependency is not considered but will be added in a future work. In addition, it is not possible to investigate possible tolerances on the basis of the given characteristics of the data sheet.

$$I_D = \sqrt{V_{DS}/r_{DSon}}$$  \hspace{1cm} (5)

$$I_D = c \cdot (V_{GS} - V_{T_D})^r$$  \hspace{1cm} (6)

$$c = \frac{I_{D1}}{(V_{G1} - V_{T_D})^r} \cdot \frac{\ln(I_{D2}) - \ln(I_{D1})}{\ln(V_{G1} - V_{T_D}) - \ln(V_{G2} - V_{T_D})}$$  \hspace{1cm} (7)

3.3 Modeling of breakdown voltage

Finally, the breakdown voltage is modeled by a simple parallel connection of a voltage source $V_{DE}$ and a diode in series. Although this value has no meaning for normal operation, the breakdown behavior of the MOSFET was modeled according to the manufacturer’s model and verified by simulation.

4. Model comparison

4.1 Half bridge test circuit

The described model is compared with two different complex models of the manufacturer (L0 and L3) by means of a simple test circuit. For this purpose, a half-bridge circuit, as seen in Fig. 4, is implemented as a step-up converter. The focus of the test setup was to test the MOSFET model for difficult convergence conditions while keeping the test setup as simple as possible. Therefore, a heavy load change was simulated. The load resistance $R_L$ is switched from
10 Ω to 1 MΩ after a settling time of 0.5 ms. All passive components of the half-bridge are modeled by their ideal component values with additional parasitics ($V_{in} = 50 V; L = 100 \mu H; R_L = 50 \Omega ; C_D = C_{out} = 1 \mu F, ESR = 1 \Omega$). The MOSFETs $M_1$ and $M_2$ are alternately clocked at 500 kHz by an ideal voltage source with a rise- and falltime of 1 ns with 1 ns dead time.

4.2 Simulation constraints
To run a simulation in LTSpice that includes the simulation models of the power MOSFET of the manufacturer, usually different parameters in the simulator must be used. These parameters are e.g. specified in application notes of the component manufacturer [9]. These parameter settings ensure that the simulation with the manufacturer models converges.

The following parameters are required to run a simulation with the manufacturer model:

$$g_{min} = 1 \times 10^{-10}; \quad \text{abstol} = 1 \times 10^{-10};$$
$$\text{reltol} = 3 \times 10^{-3}; \quad \text{cshunt} = 1 \times 10^{-15}; \quad \text{ttrtol} = 5$$

In order to compare the simulations of the test circuit when using the new models described in Sect. 3, these parameters were used for all simulations with the L3 model, although the new model would only need a single parameter, namely cshunt. In all the presented cases in this paper, the “modified trap” method, recommended by the LTSpice chief developer [10] and the application note of the manufacturer, was used as integration method. Nevertheless, simulations with other integration methods were also performed. The “gear” method shows comparable results for both models whereas the “trapezoidal” method leads to considerable convergence problems with the manufacturer model but not with the presented model.

4.3 Results
Figure 5 shows a comparison of the inductor current $i_L$ when using different MOSFET models for $M_1$ and $M_2$. The results with the proposed model are compared with those of two different complex manufacturer models. It can be clearly seen that the inductor current in the simulation with the proposed model corresponds approximately to that of the most complex manufacturer model (L3 model) in value. Deviations in the mean current $i_L$ are probably the result of different modeling of the characteristic curves of the proposed and the L0 model. Especially during load changes, the manufacturer’s model shows great overshoots of the current $i_L$ which can only be attributed to calculation errors due to its shape. This was verified by several simulations with other load changes. The manufacturer’s L3 model partly showed currents in the kA range which could not possibly correspond to realistic values. However, if the two models are compared under non-varying load, as shown in Fig. 6, they show similar behavior regarding the transient currents. The simulation time with the L3-model is about 3 to 4 times the duration with the presented model. The latter is similarly fast as the L0 model in almost all simulations.

The model proposed in this study only claims to offer a solution whose results correspond to the most complex manufacturer model with respect to its high-frequency behavior but with simpler methods and shorter simulation time which is successful. Which model delivers the more precise current, however, must be verified by measurements in a further work. Measurements of the actual switching behavior of the MOSFET are currently in progress. The comparison of the simulations with the manufacturer’s existing model already shows promising results that speak for the presented modeling variant. However, this variant has the great advantage that due to the simple measurement method using a VNA and an automatic modeling process, neither a model provided by the manufacturer nor exact knowledge about the MOSFET itself is required.

5. Conclusion
This paper shows an approach to simulate behavioral models of power MOSFETs with very strong nonlinear parasitic capacitances, particularly superjunction power MOSFETs. In combination with a simple measurement setup using a VNA, this new modeling method is possible without detailed knowledge of the internal structure of...
the MOSFET and its parasitics. With the obtained measurement results from the VNA, the nonlinear capacitances can be easily transferred into the SPICE model which makes it possible to automate the modeling process. By comparison with the manufacturer’s simulation model, it was shown that the approach of modeling with voltage controlled current sources shows promising results. As has been shown, certain manufacturer models only work in a narrow range with regard to the set simulation parameters. The proposed model tends to give better convergence in less simulation time and fewer simulation errors without requiring special settings in SPICE. Further performance tests regarding simulation time and convergence in more complex circuits are planned.

Funding Note Open access funding provided by Graz University of Technology.

Publisher’s Note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Open Access This article is licensed under a Creative Commons Attribution 4.0 International License, which permits use, sharing, adaptation, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons licence, and indicate if changes were made. The images or other third party material in this article are included in the article’s Creative Commons licence, unless indicated otherwise in a credit line to the material. If material is not included in the article’s Creative Commons licence and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder.

References

1. Giezendanner, F., et al. (2010): EMI noise prediction for electronic ballasts. IEEE Trans. Power Electron., 25(8), 2133–2141. https://doi.org/10.1109/TPEL.2010.2046542.
2. Castro, I., et al. (2016): Analytical switching loss model for superjunction MOSFET with capacitive nonlinearities and displacement currents for DC–DC power converters. IEEE Trans. Power Electron., 31(3), 2485–2495. https://doi.org/10.1109/TPEL.2015.2483015.
3. Duan, Z., et al. (2018): Improved SiC power MOSFET model considering nonlinear junction capacitances. IEEE Trans. Power Electron., 33(3), 2509–2517.
4. Hillenbrand, P., Belle, M., Terbohler, S. (2017): Sensitivity analysis of behavioral MOSFET models in transient EMC simulation. In IEEE international symposium on electromagnetic compatibility (pp. 4–9).
5. Turzyński, M., Kulesza, W. J. (2016): A simplified behavioral MOSFET model based on parameters extraction for circuit simulations. IEEE Trans. Power Electron., 31(4), 3096–3105.
6. Cittanti, D., et al. (2017): Role of parasitic capacitances in power MOSFET turn-on switching speed limits: a SiC case study. In 2017 IEEE energy conversion congress and exposition (ECCE) (pp. 1387–1394). https://doi.org/10.1109/ECCE.2017.8095992.
7. Liu, T., Wong, T. T. Y., Shen, Z. J. (2018): A new characterization technique for extracting parasitic inductances of Si power MOSFETs in discrete and module packages based on two-port S-parameters measurement. IEEE Trans. Power Electron., 33(11), 9819–9833.
8. Fuchs, M., Spielberg, L., Deutschmann, B. (2019): A new method for measuring parasitics of super junction power MOSFETs. In 2019 21st European conference on power electronics and applications (EPE ’19 ECCE Europe) (pp. 1–9).
9. Introduction to Infineon’s simulation models power MOSFETs. AN 2014-02. V 2.0. Infineon technologies. Feb. 2014.
10. Engelhardt, M. (2013): SPICE differentiation. Analog devices. http://cds.linear.com/docs/enllt-journal/LTJournal-V24n4-01-df-SPICEDifferentiation-MikeEngelhardt.pdf. Accessed 10 October 2020.

Authors

Michael Fuchs
received his BSc degree in electrical- and sound-engineering in 2014 and graduated with MSc in 2016 from Graz University of Technology – Austria. He is currently a PhD-student with the Institute of Electronics at Graz University of Technology. His research topics are electromagnetic compatibility of power electronics and EMC simulation.

Lukas Spielberg
has received the B.Sc. degree in electrical engineering from the University of Technology, Graz, Austria, in 2018. He is currently working towards the M.Sc. degree. During his studies, he is employed as a student assistant at the Institute of Electronics and the Institute of Technical Informatics at Graz, University of Technology.

Ko Odreitz
has received the B.Sc. degree in electrical engineering from the University of Technology, Graz, Austria, in 2019. He is currently working towards the M.Sc. degree. During his studies, he is employed as a student assistant at the Institute of Electronics and the Institute of Technical Informatics at Graz, University of Technology.

Bernd Deutschmann
received his M.Sc., and the Ph.D. degree in telecommunication engineering from the Graz University of Technology, Austria, in 1999 and 2002, respectively. In 2006, he joined the Automotive Power EMC Center of Infineon Technologies AG, where he worked on the improvement of the EMC of ICs for automotive power applications. Since 2014 he is with Graz University of Technology, as a Full Professor with the Institute of Electronics. During his research activities, he has applied for several patents and has authored and coauthored numerous papers and technical articles in the field of electromagnetic compatibility of integrated circuits.