Continuous monitoring for noisy intermediate-scale quantum processors

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We present a continuous monitoring system for intermediate-scale quantum processors that allows extracting estimates of noisy native gate and read-out measurements based on the set of executed quantum circuits and resulting measurement outcomes. In contrast to standard approaches for calibration and benchmarking quantum processors, the executed circuits, which are input to the monitoring system, are assumed to be out of any control. We provide the results of applying our system to the synthetically generated data obtained from a quantum emulator, as well as to the experimental data collected from a publicly accessible cloud-based quantum processor. In the both cases, we demonstrate that the developed approach provides valuable results about inherent noises of emulators/processors. Considering that our approach uses only already accessible data from implemented circuits without the need to run additional algorithms, the monitoring system can complement existing approaches. We expect that our monitoring system can become a useful tool for various quantum computers in the near-term horizon, including publicly accessible cloud-based platforms, and reduce resources that are required for their benchmarking and calibration.

I. INTRODUCTION

Quantum computers are considered as a tool for providing speed up in solving various computational problems [1–3], ranging from prime factorization [4] to simulating complex systems [5–7]. Currently, quantum devices are of intermediate size and significantly affected by noises, which manifests the era of noisy intermediate-scale quantum (NISQ) technology [2, 3, 8, 9]. Existing NISQ devices are actively used for searching quantum advantage [10, 11] and prototyping quantum algorithms [9], in particular, in the quantum chemistry domain [12, 13]. Various quantum computing devices are accessible via cloud services [14]. However, due to noise effects, the parameters of quantum computers, such as fidelity of state preparation, gates, and measurements, change with time significantly, which naturally affects the results of implementing quantum algorithms and limits the capabilities of quantum computing devices [2, 3]. This problem is typically tackled by calibrating quantum processors that involve standard techniques to characterize quantum states and processes, such as quantum tomography and special (randomized) benchmarking procedures [15–19]. Such procedures can be seen as “service quantum algorithms”, which require either running additional quantum circuits (thereby they use the computational time of the devices) or sometimes stopping the workflow of quantum processors. With the increased amount of requests to quantum computing devices [20], this problem will become more and more important.

A complementary approach is to consider a quantum processor as a ‘black box’ [see Fig. 1(a)] and use all the accessible information from the users of quantum computers for characterizing parameters of a quantum processor with certain accuracy. In this case, a set of quantum circuits that have been executed on a quantum processor and corresponding read-out results can be used. On the basis of these data, one can estimate the parameters of quantum computer components. A recent study [20] has analyzed the IBM quantum cloud over two years indicating that over 600,000 quantum circuit have been executed with almost 10 billion ‘shots’ or trials over 20 quantum computational devices. It is then reasonable to expect that with the increase of the amount of implemented circuits, the accuracy of such reconstructions will be increased. An advantage of such an approach is that it uses only already accessible data from implemented circuits without the need of running additional algorithms that spend resources of quantum processors, e.g. the quantum gate set tomography [19] or the randomized benchmarking [21]. It is also important to note that within the ‘black box’ approach the input circuits are assumed to be out of any control (e.g. they can be designed by remote users). However, the main challenge is to extract valuable information from the results of conducted quantum experiments. Moreover, classical simulation/emulation of the workflow of quantum processors is required, which limits the size quantum processors that can be monitored using this framework. One of the most advanced approach that can be efficiently used for this purpose is the tensor network approach [22].

In the present work, we develop a continuous monitoring framework for intermediate-scale quantum processors that allows extracting estimates of noisy native gate and read-out measurements based on the set of executed quantum circuits and resulting measurement outcomes [see Fig. 1(b)]. The operation of the system is based on employing an inherent tensor-network-based emulator. We provide technical details of the workflow of the monitoring system, and then show its performance on a synthetic and real data. The synthetic data is generated using an additional emulator of a noisy 5-qubit processor. Since the form of all noisy gates is known in this case, we are able to compare to the results of the monitoring system with the corresponding ‘true values’. We justify the correctness the monitoring system’s operation.
by showing the increase of prediction accuracy with a growth of processed circuits number. Then we apply the
developed system to the data obtained from publicly ac-
Cessible 5-qubit cloud-based superconducting processor.
In this case the true form noisy gates is unknown, yet we
demonstrate the correctness and usefulness of the mon-
itoring system by comparing its results with the data
obtained from an additionally launch measurement cali-
bration procedure.

Our work is organized as follows. In Sec. II, we formal-
ize an operation of a noisy quantum processor as a ‘black
box’. In Sec. III, the implementation of the monitoring
system is described. In Sec. IV, we apply the developed
system to synthetically generated and real data. The
conclude and discuss avenues of a future research and
development in Sec. IV

II. NOISY QUANTUM PROCESSORS OPERATION

One can think about the quantum processor as a ‘black
box’ taking certain inputs and providing outputs on these
inputs, as it is shown in Fig. 1(a). An input to the quan-
tum processor can be represented in the form of a quan-
tum circuit $c$ that is paired together with number of times
(shots) $K$ it has to be executed. Circuit $c$ can be con-
sidered as a list of (elementary) operations performed on
$n$ processor’s qubits, labeled by indices $0, \ldots, n-1$, and
formally can be represented as an ordered set

$$c = (l_0, t_0), \ldots, (l_{g-1}, t_{#g-1})$$

where $l_i$ denotes the label of the particular operation,
$t_i$ denotes target qubit(s) at which the operation acts,
and $#g$ is the total number of elementary operations in
the circuit. In what follows, we consider single-qubit and
two-qubit elementary operations, so targets $t_i$ can be rep-
resented either as a qubit’s index ($t_i \in \{0, \ldots, n-1\}$),
or as a pair of two distinct indices ($t_i = (t_i^1, t_i^2)$, $t_i^j \in
\{0, \ldots, n-1\}$, correspondingly.

We consider two types of operations: (i) single-qubit
state preparation and measurement (SPAM) operations
and (ii) realization of native gates. We assume that all
qubits are initially prepared in the state $|0\rangle$ that cor-
responds to the first $n$ entries in $c$ to be taken in the
form $(P, i)$ for $i = 0, \ldots, n-1$. The last $1 \leq m \leq n$
entries of $c$ determine single-qubit computational basis
measurements and have a special label $t_i = \text{M}$ (the cor-
responding target $t_i \in \{0, \ldots, n-1\}$ defines a qubit
to be measured). The set of native gates is assumed to be
consisted of the finite number of single-qubit and two-
qubit gates (i.e. $t_i \in \{H, S, T, CX\}$), which is a common
practice for existing quantum processors. We note that $c$
is the classical object, so it can be stored in the memory of
a classical computer efficiently.

The corresponding output is yielded as a list of $K$ bit
strings $s = (s^1, \ldots, s^K)$, where the length of each bit
string $s^j$ is given by the number of qubits $m$ measured
in the end of the circuit. We then refer to $s$ as a sam-
ple produced by circuit $c$. The essence of the quantum
processor’s operation is that output bit strings are gen-
erated from a certain probability distribution. In the
ideal (noiseless) case, this distribution is determined by
the sequence of unitary operators specified by gates in
the input circuit. However, due to various imperfections
causing decoherence, the actual probability distribution
for output bit strings in real NISQ devices appears to be
different from the ideal expected one.

Within our work on the development of the monitor-
ing system, we impose the following assumptions about
the noisy behaviour of the real quantum processor and processed circuits. First, we assume that noisy behaviour of elementary operations in a real processor can be described by assigning each operation with a completely positive trace-preserving (CPTP) map (quantum channel). In this way, we suppose that errors coming from realizations of each individual operation are independent. Second, though CPTP maps, corresponding to same gate acting on different qubits, can be different (e.g., a noisy Hadamard gate acting on qubit 1 may differ from a noisy Hadamard gate acting on qubit 2), we assume that the error fallibility of the gate does not depend on its time position in the circuit (i.e., a noisy Hadamard gate on qubit 1 in the beginning of the circuit is the same as the noisy Hadamard gate on qubit 1 in in the end of the circuit).

Taking into account these assumptions, we can write down an expression for the probability to obtain sample s from running circuit c. It is convenient to introduce a concept of a gate set. By a gate set $G$, we understand a set of triples of the following form:

$$G = \{(l, t, \Phi^l)\},$$

where $l$ and $t$ are the gate label and the target of elementary operation, respectively (exactly as in the case of circuits), and $\Phi^l$ is a CPTP map of the corresponding operation. In the case of the native gates realization, $\Phi^l$ describes the implementation of the gate with label $l$ on target $t$. In the case of SPAM operations, $\Phi_p$ is a CPTP map acting on the ideal initial state $|0\rangle$, and $\Phi_{M}$ is also a CPTP map preceding the ideal protective single-qubit computational basis measurement of qubit $t$. From the practical point of view, it is convenient to represent $\Phi^l$ in the form of a Choi matrix [23–25], i.e., $\Phi^l$ of a single-qubit (two-qubit) gate can be defined by $4 \times 4$ ($16 \times 16$) matrix satisfying standard conditions on Choi matrices. We then refer to the channel $\Phi^l[\cdot]$ that corresponds to the gate with label $l$ and target $t$, taken from the gate set $G$ as $G(l, t)[\cdot]$. By $G(l, t)[\cdot]$ we define a CPTP map that acts in the whole space of $n$ qubits:

$$\bar{G}(l, t)[\cdot] = (G(l, t) \otimes \text{Id}_n)[\cdot],$$

where $G(l, t)$ denotes $G(l, t)$ acting in the space of target qubit(s) $t$, and $\text{Id}_n$ denotes an identity map acting in the space of other $n-1$ (or $n-2$) qubits. Using the introduced notations, the whole CPTP map $\mathcal{F}_c(G)[\cdot]$ that is realized by circuit $c$ with gates from $G$ is given by

$$\mathcal{F}_c(G)[\cdot] = \bar{G}(l_{#G-1}, t_{#G-1}) \circ \ldots \circ \bar{G}(l_0, t_0)[\cdot],$$

where $\circ$ stands for the standard composition.

The probability of obtaining a sample $s = (s^1, \ldots, s^K)$ after $K$ shots of circuit $c$ realized with a quantum processor, whose operations are described by gate set $G$, is given by

$$P(s|c, G) = \prod_{j=1}^{K} P(s^j|c, G),$$

where

$$P(s^j|c, G) = \text{Tr} \left( |s^j\rangle\langle s^j| \mathcal{F}_c(G)[\rho_{in}] \right)$$

is $\mathrm{th}$ probability to obtain a bit string $s^j$, $\rho_{in} = (|0\rangle\langle 0|)^{\otimes n}$ is the fixed ideal initial state, and $|s^j\rangle\langle s^j|$ is the shorthand notation of the projector on $|s^j\rangle$ state in the space of measured qubits, i.e. qubits with $M$ gate in the end of the circuit $c$ (in the remaining space, $|s^j\rangle\langle s^j|$ acts as an identity). We note that logarithm of $P(s|c, G)$ can be written in a compact form as follows:

$$\log P(s|c, G) = \sum_{j=1}^{K} \log \text{Tr} \left( |s^j\rangle\langle s^j| \mathcal{F}_c(G)[\rho_{in}] \right) = \sum_{s \in \mathcal{S}} \#s \log \text{Tr} \left( |s\rangle\langle s| \mathcal{F}_c(G)[\rho_{in}] \right),$$

where $\#s$ is the number of times a bit string $s$ appears in sample $s$.

\section{III. DESIGN OF THE MONITORING SYSTEM}

Consider a quantum processor operating in a continuous regime, i.e. sequentially providing output samples $s_1, s_2, \ldots$ by processing a stream of input circuits with corresponding shots numbers $(c_1, K_1), (c_2, K_2), \ldots$. Importantly, here we assume that input circuits $c_i$ themselves are beyond the control: The particular circuits executed on the processor can be formed by remote users, while the monitoring system is launched by an administrator of the service, providing access to the quantum processor.

The goal of the monitoring system is in the gathering the actual information about the quantum processor without borrowing its computation time on running specific protocols. Consider a time moment right after the obtaining measurement outcomes for the $i$th circuit. At this moment the input to the monitoring system is given by the following expression:

$$D_i^M = (d_{\max(i-1-M)}, \ldots, d_i), \; d_j = (c_j, K_j, s_j),$$

where $M$ is the hyperparameter determining the maximal number of circuits to be processed by the monitoring system. One can set $M = \infty$ that corresponds to the processing of all previously launched circuits.

We note that due to the fact that the noise level of real quantum processor typically changes in time, it is a common practice to periodically suspend the operation of the processor for a maintenance and calibration purposes. In the case of such maintenance procedure, the introduced circuit counter is reset to zero.

The output of the monitoring system to the input $D_i^M$ is gate set $G_i^{\text{est}}$ that contain estimates of the ‘true’ gate set of the quantum processor. The estimated gate set is obtained as a solution of the following optimization problem

$$G_i^{\text{est}} = \arg \min_G \mathcal{L}(G|D_i^M),$$
where the minimization is performed over CPTP maps inside a gate set $\mathbf{G}$, and the cost function is given by
\[
\mathcal{L}(\mathbf{G}|D_t^M) = -\sum_{j=\max(1,i-M)}^i \log P(s_j|c_j, \mathbf{G}) + D_{\lambda_1,\lambda_2}^{\text{reg}}(\mathbf{G}).
\] (10)

Here, the first term is the standard log-likelihood function of the gate set $\mathbf{G}$ with respect to the input data $D_t^M$. The second term in Eq. (10) serves for regularization purposes and reads
\[
D_{\lambda_1,\lambda_2}^{\text{reg}}(\mathbf{G}) = \sum_{q=1,2} \sum_{l,t:q-\text{qubit}} \|\mathcal{C}(\mathbf{G}(l,t)) - \mathcal{C}(\mathbf{G}^{\text{ideal}}(l,t))\|^2_F.
\] (11)

where $\lambda_1,\lambda_2 \geq 0$ are regularization parameters, $\| \cdot \|_F$ stands for the Frobenius norm, $\mathcal{C}(\Phi)$ is the Choi matrix of channel $\Phi$, and $\mathbf{G}^{\text{ideal}}$ is the gate set consisted of the flawless realization of all operations. The Choi matrix for a single-qubit channel is defined as
\[
\mathcal{C}(\Phi) = \sum_{j,j'=0,1} \Phi(j|j') \otimes |j\rangle \langle j'|,
\] (12)

and for two-qubit one as
\[
\mathcal{C}(\Phi) = \sum_{j,j',k,k'=0,1} \Phi(jk|j'k') \otimes |jk\rangle \langle j'k'|.
\] (13)

All CPTP maps within $\mathbf{G}^{\text{ideal}}$ are represented by an action unitary operators
\[
\mathbf{G}^{\text{ideal}}(l,t)[\rho] = U_l \rho U_l^\dagger,
\] (14)

where $U_l$ is a unitary operator of the gate with label $l$. The flawless SPAM operation corresponds to $U_R = U_M = 1$, where $1$ is the identity matrix.

The essence of the regularization term (11) is the distance between the elements of the estimated gate set $\mathbf{G}_t^{\text{est}}$ and the ideal gate set $\mathbf{G}^{\text{ideal}}$. This term has a probabilistic interpretation of the contribution of the gate set prior probability distribution concentrated near the ideal gate set. Indeed, one expects the true gate set to be close to the ideal gate set. Note that in Eq. (11) we go separately through all single-qubit and two-qubit gates with different regularization parameters $\lambda_1$ and $\lambda_2$ correspondingly.

One of the main challenges related to the solving Eq. (9) is to compute the cost function $\mathcal{L}(\mathbf{G}|D_t^M)$ that requires obtaining probabilities for given outcomes in the form (6). This is a point where the inherent quantum emulator comes into play. We develop our own tensor networks-based quantum emulator that allows one to compute exact form of Eq. (7) for circuits of low width or depth. The operation of the emulator is based on contraction of a tensor-network specified by the circuit, gate set elements, and the particular measurement outcome.

We note that no approximations, i.e. the limitation of tensor ranks, is used while contraction.

The need in the emulator poses the main limitation of the developed system; specifically, the monitoring system can process classically simulatable circuits only. However, this is the case for a variety of existing developing quantum processors. Moreover, there are various techniques allowing simplifications in the simulation of quantum processors in the quantum advantage regime [26] (we place this discussion in Sec. V). As we demonstrate in the next section, the developed monitoring system copes with a task of monitoring existing five-qubit superconducting processors. We also provide additional benchmarks of the developed tensor-network-based emulator in Appendix B.

The minimization procedure in Eq. (9) with respect to the elements of $\mathbf{G}$, namely quantum channels $\{\Phi_i\}$, is realized by the gradient based Riemannian optimization technique [27, 28] that preserves CPTP constraints on the elements of $\mathbf{G}$. To calculate gradient of the loss function defined in Eq. (10), we utilize automatic differentiation [29]. In particular, the Riemannian adaptive moment estimation (RAdam) algorithm [30, 31] is efficient. The implementation of the RAdam algorithm for CPTP constraints is taken from QGOpt package [32].

IV. APPLICATION OF THE MONITORING SYSTEM

Here we consider an application of the developed monitoring system to the cloud-based 5-qubit quantum processor. We perform two kinds of numerical experiments: ‘synthetic’ and ‘real’ ones.

In the synthetic experiment, we replace the quantum processor under observation with a noisy quantum emulator with known noise parameters and known noisy gate set (do not confuse this emulator with the emulator inside the monitoring system). The goal here is to make sure that the monitoring system is able to learn the noise parameters of the emulator from the results of running random circuits, which is impossible to strictly confirm without prior knowledge of these parameters. In the real experiment the input data for the monitoring system comes from the publicly-accessible superconducting processor IBMQ_LIMA.

To achieve the consistency between two experiments, they take place under the same conditions. (i) The emulator in the synthetic experiment is considered to have the same coupling topology and native gate set as in the real processor. (ii) Synthetic input circuits and their corresponding shots numbers to produce the output samples are the same in the both experiments.

The rest of the section is organized as follows. First, we describe the architecture of the quantum processor under consideration and its noisy emulator. Next, we describe the construction of input circuits. Finally, we consider the results of synthetic and real numerical experiments.
A. Architecture of the processor

We consider a 5-qubit quantum processor IBMQ LIMA with a coupling map shown in Fig. 2. Each arrow in Fig. 2 corresponds to the ability to perform a native two-qubit CX (controlled NOT) gate

\[
U_{\text{CX}} = \begin{bmatrix}
1 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 \\
0 & 0 & 1 & 0 \\
0 & 0 & 1 & 0
\end{bmatrix}.
\]  

(15)

Though the both directions of CX gates within connection in the coupling map are allowed by the architecture of the processor, we fix the CX directions as it in shown in Fig. 2: Arrows are directed from control qubits to target ones.

![Diagram of quantum processor](image)

Figure 2. Architecture of the considered 5-qubit processor IBMQ LIMA. The arrows corresponds to an ability to perform CX gate: Arrows are directed from control qubits to target ones.

As native single-qubit gates, which can be applied to every qubit, we consider a finite set

\[
U_{\text{RZ}} = \begin{bmatrix}
e^{-i\pi/8} & 0 & 0 & 0 \\
0 & e^{i\pi/8} & 0 & 0 \\
0 & 0 & 1 & 0 \\
0 & 0 & 0 & 1
\end{bmatrix}, \quad U_{\text{X}} = \begin{bmatrix}0 & 1 \\
1 & 0
\end{bmatrix}, \quad U_{\text{ID}} = \begin{bmatrix}1 & 0 \\
0 & 1
\end{bmatrix}.
\]  

(16)

We note that the introduced gate set is universal and can be used for constructing any desired 5-qubit unitary operation up to preset accuracy.

B. Noisy emulator

In order to construct the noisy emulator of the considered processor, we assign to each native gate acting on a qubit (or a pair of qubits) its own quantum channel. In this way, we obtain a known true noisy gate set, which we denote as \(G^{\text{true}}\).

The construction of quantum channels is motivated by standard approach used for modelling noisy behavior of near-term quantum computers [33]. In particular, we take into account a longitudinal \((T_1)\) and transverse \((T_2)\) relaxation of qubit’s states, fluctuations of a length and/or intensity of control pulses, and general qubit errors modelled by depolarizing channel.

In the case of a single-qubit gate \(U\), the corresponding quantum channel is obtained in the form:

\[
G^{\text{true}}(U, t)[\rho] = \Phi^{\text{ap}}(\nu; U, t) \circ \Phi^{\text{depol}}(p) \circ \Phi^{\text{sm}}(\nu; U, t) \circ \Phi^{\text{ap}}(\nu; U, t)[\rho].
\]  

(17)

Here

\[
\Phi^{\text{ap}}(\nu; U, t)[\rho] = \Phi^{\text{ap}}(\mu)[\rho] \circ \Phi^{\text{p}}(\gamma)[\rho]
\]  

(18)

is a sequence of a phase damping

\[
\Phi^{\text{p}}(\mu)[\rho] = \begin{bmatrix}1 & 0 & 0 & 0 \\
0 & \sqrt{1-\mu} & 0 & 0 \\
0 & 0 & \sqrt{1-\mu} & 0 \\
0 & 0 & 0 & \sqrt{1-\mu}
\end{bmatrix}
\]  

(19)

and an amplitude damping

\[
\Phi^{\text{a}}(\gamma)[\rho] = \begin{bmatrix}1 & 0 & 0 & 0 \\
0 & \sqrt{1-\gamma} & 0 & 0 \\
0 & 0 & \sqrt{1-\gamma} & 0 \\
0 & 0 & 0 & \sqrt{1-\gamma}
\end{bmatrix}
\]  

(20)

channels, where \(\gamma, \mu \in [0, 1]\) are decoherence parameters; \(\Phi^{\text{depol}}(p)[\rho]\) is a standard depolarization channel

\[
\Phi^{\text{depol}}(p)[\rho] = (1-p)[\rho] + \frac{p}{2} \text{Tr}[\rho] 1
\]  

(21)

with depolarization parameter \(p \in [0, 1]\); and

\[
\Phi^{\text{sm}}(\nu; U)[\rho] = \int e^{-iH(U)^\tau} \omega_\nu(\tau) d\tau
\]  

(22)

with

\[
\omega_\nu(\tau) = \frac{1}{\sqrt{2\pi} \nu} \exp(-\frac{(\tau-1)^2}{2\nu^2}), \quad H(U) = i \log(U),
\]  

(23)

corresponds to implementing \(U\) by acting with the effective Hamiltonian \(H(U)\) over time period fluctuating according to Gaussian distribution with unit mean and standard deviation \(\nu\). Note that \(\Phi^{\text{sm}}(\nu; U)\) does not affect identity channel with \(U = 1\). The noise model for \(M\) gate is also obtained by Eq. (17). We note that the imperfections of SPAM operations are considered to be described by measurement \(M\) gates only (the preparation is considered to be ideal). We use the same assumption for the data from the real processor.

The channels for realization of two-qubit gates are obtained in similar way:

\[
G^{\text{true}}(U_{\text{CX}}, t)[\rho] = \Phi^{\text{ap}}(\nu_{\text{CX}}, \mu_{\text{CX}})[\rho] \circ \Phi^{\text{depol}}(p_{\text{CX}})[\rho] \circ \Phi^{\text{sm}}(\nu_{\text{CX}}; U_{\text{CX}})[\rho] \circ \Phi^{\text{ap}}(\nu_{\text{CX}}, \mu_{\text{CX}})[\rho].
\]  

(24)
damping and depolarizing channels act on both qubits, and a ‘smoothed’ CX realization $\Phi^\text{sm}(\nu^\text{CX}; U_{\text{CX}})$ is given by Eq. (22), (23).

The chosen noise parameters are presented in Tab. I. We note that in order to make the emulator to be more realistic, we set the strengths of amplitude damping $\gamma^l_t$ and phase damping $\mu^l_t$ to be the same for gates acting on the same qubit $t$. In Tab. I we also provide the resulting fidelities $F^l_t$ of noisy gates with respect to their ideal implementations given by

$$ F^l_t = \frac{1}{4} \langle \Psi_l \middle| C[G^\text{true}(l,t)] \middle| \Psi_l \rangle, $$

in the single-qubit case, and by

$$ F^l_t = \frac{1}{16} \langle \Psi_l \middle| C[G^\text{true}(l,t)] \middle| \Psi_l \rangle, $$

in the two-qubit case.

For efficient sampling of output bit strings the technique described in Appendix A is used.

**Table I. Noise parameters of the emulator and resulting fidelities for all the considered native gates.**

| $l$ | $t$ | $\nu^l_t$ | $\mu^l_t$ | $\gamma^l_t$ | $F^l_t$ | $l$ | $t$ | $\nu^l_t$ | $\mu^l_t$ | $\gamma^l_t$ | $F^l_t$ |
|-----|-----|-----------|-----------|-------------|------|-----|-----|-----------|-----------|-------------|------|
| ID 0 | 0 | 0.015 | 0.01 | 0.015 | 0.980 | X 0 | 0.012 | 0.012 | 0.015 | 0.982 | SX 0 | 0.18 | 0.017 | 0.01 | 0.015 | 0.960 |
| ID 1 | 0 | 0.01 | 0.022 | 0.012 | 0.979 | X 1 | 0.015 | 0.008 | 0.022 | 0.012 | 0.980 | SX 1 | 0.02 | 0.01 | 0.022 | 0.012 | 0.978 |
| ID 2 | 0 | 0.003 | 0.013 | 0.01 | 0.989 | X 2 | 0.11 | 0.033 | 0.013 | 0.01 | 0.939 | SX 2 | 0.01 | 0.005 | 0.013 | 0.01 | 0.987 |
| ID 3 | 0 | 0.005 | 0.005 | 0.009 | 0.992 | X 3 | 0.014 | 0.007 | 0.005 | 0.009 | 0.990 | SX 3 | 0.01 | 0.007 | 0.005 | 0.009 | 0.990 |
| ID 4 | 0 | 0.01 | 0.006 | 0.005 | 0.988 | X 4 | 0.025 | 0.005 | 0.005 | 0.005 | 0.991 | SX 4 | 0.013 | 0.013 | 0.006 | 0.005 | 0.986 |

The choice of single-qubit gates is taken uniformly at random from the set \{$X, SX, RZ, ID$\}. The pattern of CX gates implemented in two-qubit gates sublayers is also taken uniformly at random from set of three possible patterns shown in the bottom of Fig. 3(b).

**Figure 3.** In (a) the structure of random circuits used for generating input data for the monitoring system is shown. In (b) the variants for a random choice for single-qubit gates and patterns of CX gates in the two-qubit gates sublayers are presented.

**D. Monitoring the noisy emulator**

First, we apply the developed monitoring system to the data generated with the described emulator. We generate 1024 random circuits $c_i$ (according to Sec. IV C) and for each circuit get $K_i = 8192$ bit strings of length 5 packed into a sample $s_i$. Then we apply the monitoring system to the input datasets $D^\infty_i$ for $i = 2^1, 2^2, \ldots, 2^10$ and obtain the corresponding estimated gates sets $G^\text{est}_i$. We set regularization parameters $\lambda_1 = 100$, $\lambda_2 = 200$. We refer to the circuits $c_1, \ldots, c_i$ as a training set, and to all other circuits as a test set.

To characterize the ability of the monitoring system to predict an output probability distribution, we consider a quantity

$$ \Delta^\text{circ}_i(j) = \sum_s |P(s|c_j, G^\text{est}_i) - f(s|s_j)|, $$

where the summation is performed over all possible bit strings $s \in \{0,1\}^5$, and $f(s|s_j) = #s_j/K_j$ is a frequency of appearing of $s$ in the resulting sample $s_j$. The essence of $\Delta^\text{circ}_i(j)$ is an L1 distance between the observed distribution $f_j(s)$ obtained for the $j$-th circuit and the predicted distribution $P(s|c_j, G^\text{est}_i)$ obtained after learning the monitoring system on $i$ circuits.

The averaged values of $\Delta^\text{circ}_i(j)$ are shown in Fig. 4.
Here the averaging is performed over circuits with the same layer number \( n_l \) separately for circuits inside the train set \((j \leq i)\) and inside the test set \((j > i)\). One can see that the accuracy of prediction increases with the growths of the training set, yet the difference between the length of the training set \( i = 128 \) and \( i = 512 \) is quite small. Moreover, we see that the training curve and the test curve approach each other with the growth of \( i \) and are almost equal for \( i = 512 \). This result suggest to pick up the value of the hyper parameter \( M \) (the maximal number of processed circuits) on the level of 128-256.

![Figure 4. Mean values of prediction inaccuracy (27) obtained by averaging over circuits with the same number of layers inside the training and test sets for different number of processed circuits \( i \) (1024 circuits are considered in total). The input data for the monitoring system is generated with the described noisy quantum emulator.](image)

We then consider how the monitoring system reconstructs individual gates. We introduce two quantities, namely,

\[
\begin{align*}
\Delta^\text{true}_0(l; t; i) &= \|G^\text{est}_i(l, t) - G^\text{true}(l, t)\|_0, \\
\Delta^\text{ideal}_0(l; t; i) &= \|G^\text{est}_i(l, t) - G^\text{ideal}(l, t)\|_0,
\end{align*}
\]

(where \( \| \cdot \|_0 \) is the diamond norm) that provide a distance between an estimate gate \( G^\text{est}_i(l, t) \) obtained after training on \( i \) circuits and the corresponding true and ideal versions. Remind that the distance between the real and estimated gates can be obtained only for the synthetically generated data. We also note the monitoring system is not aware about the particular decoherence model chosen for \{\( G^\text{true}(l, t) \)\} and performs reconstruction of \{\( G^\text{est}_i(l, t) \)\} in the form of general CPTP maps.

For the special case of \( M \) gate, describing an imperfection of a read-out measurement, we consider quantities

\[
\begin{align*}
\Delta^\text{true}_{\text{POVM}}(t; i) &= \|M_0(G^\text{est}_i(M, t)) - M_0(G^\text{true}_i(M, t))\|_1, \\
\Delta^\text{ideal}_{\text{POVM}}(t; i) &= \|M_0(G^\text{est}_i(M, t)) - M_0(G^\text{ideal}_i(M, t))\|_1,
\end{align*}
\]

where \( \| \cdot \|_1 \) stands for the standard L1 norm, and

\[
M_0(\Phi) = \text{Tr}_2 \left[ (|k\rangle \langle k| \otimes 1)C[\Phi] \right]
\]

is a POVM effect resulting from placing single-qubit channel \( \Phi \) before the single-qubit computational basis measurement and corresponding to the outcome \( k \) (here \( \text{Tr}_2 \) denotes a partial trace with respect to the second qubit). The values of \( \Delta^\text{true}_{\text{POVM}}(t; i) \) (\( \Delta^\text{true}_{\text{POVM}}(t; i) \)) describe the maximal possible difference between probability distributions appearing in estimated and ideal (estimated and real) measurements.

The distances between the elements of the estimated gate sets \( G^\text{est}_i \) and the true gate set \( G^\text{true} \) as functions of processed circuit number \( i \) are presented in Fig. 5. One can see that that all the curves tend to the zero value with a growth of processed circuits \( i \), that justifies the proper operation of the monitoring system.

Next, we consider the distance between the estimated gate sets \( G^\text{est}_i \) and the ideal gate set \( G^\text{ideal} \). The behaviour of \( \Delta^\text{true}_{\text{POVM}}(l; t; i) \) and \( \Delta^\text{ideal}_{\text{POVM}}(l; t; i) \) is shown in Fig. 6. By the horizontal lines in Fig. 6 we also show values of distances between the elements of the real and ideal gate sets given by

\[
\begin{align*}
\Delta^\text{true}_{\text{POVM}}(l; t) &= \|G^\text{true}_{\text{POVM}}(l, t) - G^\text{true}_{\text{POVM}}(l, t)\|_0, \\
\Delta^\text{ideal}_{\text{POVM}}(t; i) &= \|M_0(G^\text{ideal}_i(M, t)) - M_0(G^\text{true}_i(M, t))\|_1.
\end{align*}
\]

One can see that though there are imperfections of estimates, the monitoring system allows one to identify clearly the most erroneous elements against the elements of same type (see e.g. \( X \) gate on 2-nd qubit, \( SX \) on 0-th qubit, and \( CX \) gate between 3-rd and 4-th qubits).

E. Monitoring the real device

Here we apply the monitoring system to analyzing samples that are obtained with the use of the IBM 5-qubit superconducting quantum processor \( \text{IBMQ}_\text{LIMA} \) (see the calibration data in Appendix D). In order to provide a fair comparison between the results obtained with the emulator and real device, we consider exactly the same input circuits, and shots number \( K_i = 8192 \).

First, we consider an (in)accuracy of the outcomes distribution predictions as a function of a number of processed circuits. The behaviour of averaged values of \( \Delta^\text{true}_{\text{circ}}(j) \), obtained in the same way as in the previous subsection, are shown in Fig. 7. We see that in general Fig. 7 has the same form as Fig. 4, yet there are some differences. One can see in Fig. 7 a clear monotonic increase of the prediction inaccuracy with growth of layers number in contrast to a saturation behaviour observed for the synthetic data. At the same time, the values of \( \Delta^\text{true}_{\text{circ}}(j) \) for the data from the real processor are 2-3 times higher than for the synthetic data. We suppose that this increase of discrepancies is due to the fact the the suggested model of the quantum processor does not fully
catch all the features of real processor. However, as we show next, the monitoring system still provides valuable results.

In Fig. 8 we show distances between elements of the es-
Figure 7. Mean values of prediction inaccuracy (27) obtained by averaging over circuits with the same number of layers inside the training and test sets for different number of training circuits \(i\) (1024 circuits are considered in total). The input data for the monitoring system is obtained from IBMQ\_LIMA.

We have tested the developed system using a synthetic data generated from a specifically designed emulator of a noisy quantum processor, and data obtained by launching circuits on the 5-qubit superconducting quantum processor IBMQ\_LIMA, which is available via cloud. In the case of the synthetic data, we have validated the performance of the monitoring system by comparing the output of the system (estimated gate set) with the true noisy gate set realized within the emulator. For the case of the data obtained from the quantum processor, we have seen the results of the monitoring system are in a pretty good agreement with the results obtained from specially launched read-out calibration routine. Thus we can conclude that the developed system successfully copes with assigned tasks.

The main limitation of the applicability of the considered approach relates to the necessity of inherent quantum emulator, which in fact mimics the behaviour of real quantum processor. This issue prevents the use of the monitoring system for processing large circuits intractable for tensor network-based simulation. However, the monitoring system is still applicable in the case where the set of launched circuits possess a subset of tractable, i.e., of low width or low depth, circuits. A prime example of this kind of circuits are ‘elided’ and ‘patch’ circuits with bounded amount of generated entanglement used for verification purposes in quantum advantage experiments [26]. In this way, even in a regime, where emulation time is larger then the real quantum computing time, the developed system still is able to provide valuable information by processing subsets of launched circuit. This subset can chosen according to expected emulation complexity (e.g., circuit width \(\times\) circuit depth), or taken at random (e.g., by processing every \(k\)th launched circuit for large enough \(k\)).

Another limitations of the developed system relate to inherent assumptions about the noise model. One of the used assumptions is Markovianity of noise in the sense...
that each noisy gate can be described with a CPTP map, and we also assume that noisiness of a gate acting on a particular qubit (pair of qubits) does not depend on the position if this gate within a circuit. We note that the first limitation can be overcome by introducing additional quantum information carries (i.e. qubits or qudits) that are responsible for memory effects. Then gates from input circuits can be mapped to quantum channels acting both on the original target and additional quantum information carries. This approach relates to the description of non-Markovian behaviour by using a Markovian embedding technique [35–37]. We leave a support of non-Markovian processes for further development of the monitoring system.

Finally, we note the developed system is capable of tracking drifts of noise parameters in the case where these drift appears on time scales larger than the number of circuits reliable training (based on the obtained results it is about $2^5 \ldots 2^8$ circuits). This tracking is possible by adjusting the hyperparameter $M$, defining the maximal number of recently launched circuits taken for input for the monitoring system. We expect that our monitoring system can become a useful tool for different quantum computing platforms, reducing additional resources needed for their calibration.

Figure 8. The distances between the ideal and estimated realizations of single-qubit gates (ID, X, SX, RZ), two-qubit gates (CX), and read-out measurements (M) for different (pairs of) qubits are shown as function of the number of processed circuits $i$. The input data for the monitoring system is obtained from IBMQ_LIMA.

Figure 9. Comparison of read-out measurement error rates obtained from the specially launched calibration routine $[e_{1\rightarrow0}^{\text{exp}}(t) \text{ and } e_{0\rightarrow1}^{\text{exp}}(t)]$ and the monitoring system trained on 1024 random circuits $[e_{1\rightarrow0}^{\text{est}}(t), e_{1\rightarrow0}^{\text{est,acc}}(t), \text{ and } e_{0\rightarrow1}^{\text{est}}(t)]$ is presented.

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Appendix A: Samples generation

The operation of the quantum processor emulator used for generating synthetic data requires an efficient algorithm of measurement outcomes sampling. Remind that each measurement outcome is a bit string \( s = (s_0, s_1, \ldots, s_{n-1}) \), where \( s_i \) takes either 0 or 1. The probability of getting a particular measurement outcome reads

\[
P(s_{n-1}, s_{n-2}, \ldots, s_0) = \text{Tr} \left( \bigotimes_{i=0}^{n-1} |s_i\rangle \langle s_i| \rho_i \right), \tag{A1}
\]

where \( \rho_i \) is the final state of a quantum processor after a sequence of instructions and \( |s_i\rangle \langle s_i| \) is a projector acting on the \( i \)-th qubit. Straightforward sampling from \( P(s_{n-1}, s_{n-2}, \ldots, s_0) \) requires an appeal to all possible bit strings whose number scales exponentially with \( n \). To circumvent such scaling we utilize chain rule for probabilities that reads

\[
P(s_{n-1}, s_{n-2}, \ldots, s_0) = \prod_{i=0}^{n-1} P(s_i|s_{i-1}, \ldots, s_0), \tag{A2}
\]

where conditional probabilities take the following form:

\[
P(s_i|s_{i-1}, \ldots, s_0) = \frac{P(s_i, s_{i-1}, \ldots, s_0)}{\sum_{x=0,1} P(x, s_{i-1}, \ldots, s_0)},
\]

\[
P(s_i, s_{i-1}, \ldots, s_0) = \text{Tr} \left( \bigotimes_{j=i+1}^{n-1} \mathbb{1} \bigotimes_{j=0}^{i} |s_j\rangle \langle s_j| \rho_i \right), \tag{A3}
\]

where \( \mathbb{1} \) is the identity matrix reflecting the fact that we have not yet observed the measurement outcomes for qubits number \( \{i+1, i+2, \ldots, n-1\} \).

The decomposition Eq. (A2) allows one to sample measurement outcomes sequentially, i.e. at the first step one samples a measurement outcome for the first qubit from the distribution \( P(s_0) \), at the second step on samples a measurement outcome for the second qubit given the measurement outcome for the first qubit from the distribution \( P(s_1|s_0) \) and so on. The complexity of this sequential strategy scales linearly with \( n \) in contrast with the exponential scaling for the straightforward approach.

Appendix B: Quantum emulator benchmarks

Here we provide an additional information about the performance of the tensor network-based quantum emulator employed in the developed monitoring system. We benchmark the emulator on \( n \)-qubit random circuits consisted of noisy gates, described by corresponding quantum channels (CPTP maps). Circuits structured in layers are considered. Each layers consists of single qubit gates applied to each of \( n \) qubits, and two-qubit gates applied to \( |n/2| \) randomly chosen disjoint qubit pairs. The considered native gates set consists of \( \text{ID}, \text{X}, \text{SX}, \text{RZ}, \text{M}, \) and \( \text{CX} \) gates. All-to-all connection topology for \( \text{CX} \) gates is assumed.

An average time for obtaining \( K \) outcomes as function of \( n, K \), and a number of layers is shown in Fig. 10. AMD Ryzen 5 3600 with 16 Gbyte RAM is used. We note that no optimizations related to GPU-based parallelization are present in the current version of the emulator. We also recall that the emulation is performed without any tensor rank contractions usually considered in the framework of tensor network-based representations.

Appendix C: Reconstructing single-qubit gates from random circuits

Here we provide an additional numerical experiment of reconstructing noisy quantum gates with the developed monitoring system. In particular, we consider a single-qubit processor with a universal gate set consisting of \( \text{RX} \) and \( \text{RZ} \) gates providing \( \pi/4 \) rotations around \( x \)- and \( z \)-axes of the Bloch sphere correspondingly. The input data for the monitoring system is obtained by running random circuits on the developed noisy emulator, described in Sec. IV B. The chosen noise whose parameters are listed in Table II.

The results of noisy channels reconstruction based on running random circuits are shown Fig. 11. Recall that the reconstruction in the monitoring system is performed with respect to general quantum channels completely independent of the noise model in the emulator used for data generation. The number of gates for each circuit is taken at random from the range \( \{1, 2, \ldots, 30\} \), and each

![Figure 10. Average emulation time of noisy random circuits using the employed tensor network-based emulator.](image-url)
Figure 11. The distances between the true and the estimated (left column), and the ideal and the estimated (right column) realizations of single-qubit gates ($RX$, $RZ$), and readout measurements ($M$). Horizontal lines in the right column show distances between the true and ideal realizations.

| True $\Delta$ | Ideal $\Delta$ |
|---------------|----------------|
| $RX$          | $RZ$           |
| $M$           |                |

Table II. Noise parameters of the emulator and resulting fidelities for the considered single-qubit case.

Appendix D: Calibration data

In Table III we provide additional calibration data for the employed ibmq_lima processor at the time of the demonstration. This demonstration data was downloaded using cloud-based interface.
Table III. Calibration data for the five-qubit superconducting processor ibmq_lima at the time of the demonstration discussed in Sec. IV E.

| Parameter                  | Q0      | Q1      | Q2      | Q3      | Q4      |
|----------------------------|---------|---------|---------|---------|---------|
| $T_1$ (μs)                 | 117.49  | 66.93   | 121.65  | 93.56   | 21.35   |
| $T_2^*$ (μs)               | 184.91  | 79.02   | 182.49  | 93.73   | 25.86   |
| Frequency (GHz)            | 5.029   | 5.127   | 5.247   | 5.302   | 5.092   |
| Anharmonicity (GHz)        | -0.33574 | -0.31834 | -0.3336 | -0.33124 | -0.3429 |
| Readout assignment error   | 0.0297  | 0.0133  | 0.0203  | 0.0267  | 0.0484  |
| Prob. meas 0 prep. [1]     | 0.0466  | 0.0216  | 0.0328  | 0.0374  | 0.0752  |
| Prob. meas 1 prep. [0]     | 0.0128  | 0.005   | 0.0078  | 0.016   | 0.0216  |
| Readout length (ns)        | 5351.11 | 5351.11 | 5351.11 | 5351.11 | 5351.11 |
| ID error                   | 2.039 $10^{-4}$ | 2.333 $10^{-4}$ | 2.414 $10^{-4}$ | 2.759 $10^{-4}$ | 6.108 $10^{-4}$ |
| SX error                   | 2.039 $10^{-4}$ | 2.333 $10^{-4}$ | 2.414 $10^{-4}$ | 2.759 $10^{-4}$ | 6.108 $10^{-4}$ |
| X error                    | 2.039 $10^{-4}$ | 2.333 $10^{-4}$ | 2.414 $10^{-4}$ | 2.759 $10^{-4}$ | 6.108 $10^{-4}$ |
| $\text{CX error}$         |         |         |         |         |         |
| Q0                         | 5.927 $10^{-10}$ | 5.744 $10^{-10}$ | 1.182 $10^{-9}$ |         |         |
| Q1                         | 5.744 $10^{-10}$ | 1.182 $10^{-9}$ |         |         |         |
| Q2                         | 1.182 $10^{-9}$ |         |         |         |         |
| Q3                         |         |         |         | 1.493 $10^{-9}$ |         |
| Q4                         |         |         |         | 1.493 $10^{-9}$ |         |
| Gate time (ns)             |         |         |         |         |         |
| Q0                         | 305.777 |         |         |         |         |
| Q1                         | 341.333 | 334.222 |         |         |         |
| Q2                         | 298.666 |         |         |         |         |
| Q3                         | 462.222 |         |         | 519.111 |         |
| Q4                         |         |         |         | 483.555 |         |

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