A continuous-time capacitance to voltage converter for micro-capacitive pressure sensors

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Abstract. This paper reports a continuous-time capacitance to voltage converter (CVC), based on the charge integration circuit, for capacitive pressure sensor applications. Unlike conventional charge integrators which need a large feedback resistor for biasing, the proposed method uses low duty cycle periodic reset to establish a robust dc bias at the sensing electrode. The CVC has the merits of low noise, linear transfer characteristics and low susceptibility to system offset. A CVC has been designed with standard 0.35μm CMOS technology. For a 3.3-V supply, it achieves 1mW power consumption, 0~0.8pF detection range and 0.06% resolution.

1. Introduction

Precise measurement of capacitance difference or ratio in a continuous form is very important for capacitive pressure sensors. Compared with discrete-time approaches, for example the switched-capacitor (SC) circuits, continuous-time voltage sensing has intrinsically higher resolution because it does not suffer from noise folding [1]. Recently, various methods have been reported [2]-[4] to deal with capacitance to voltage conversion. Some of them, for instance the method utilizing ratio-arm bridge [2], is symmetrical and sensitive, but it has the disadvantage that transformer coils have to be used which is difficult to implement monolithically. Others, for example the modified Martin oscillator with microcontroller [3], is not capable of handling capacitance changes with frequencies higher than 10Hz. Another approach is based on charge integration [4]. It is less susceptible to parasitics, however, a fairly large feedback resistor is usually needed to bias the sensing electrode. In the past, the large resistor can be implemented either by sub-threshold transistors or long transistors in triode region [5, 6]. However, values of such MOS resistors depend on the terminal voltages which are difficult to control. For pressure sensor applications, since the capacitance and output voltage of the CVC change over a wide range, the linearity of the feedback resistor degrades seriously. Besides, a large transistor will introduce parasitic capacitance which would cause signal attenuation in a capacitive sensing front-end.

This paper presents a continuous-time CVC which does not have the limitations mentioned above. Instead of using large feedback resistors, the bias voltage at sensing electrode is established by low duty cycle periodic reset. The proposed CVC has the advantages of low noise, linear capacitance to voltage transfer characteristics and low susceptibility to system offset. In section 2, circuit configuration is presented. Section 3 describes the op amp design, followed by digital control logic implementation in section 4. In section 5, system level simulation results are provided to verify the circuit performance and conclusion is finally drawn in section 6.
2. Circuit configuration

The basic CVC structure is shown in Figure 1(a). $C_i$ is the feedback capacitor. $C_s$ and $C_s + \Delta C$ are a pair of capacitive pressure sensors whose common node is connected to the inverting input of the op amp. $C_s$ represents the total parasitic capacitance at the sensing electrode. The square-wave bias reset signals are generated on-chip by four MOS switches, $S_1, S_1', S_2, S_2'$.

![Figure 1. (a) CVC for capacitive pressure sensors (b) timing diagram for bias reset signals](image)

The CVC operation can be divided into two consecutive phases, namely, the sensing phase and reset phase. As shown in Figure 1(b), in the sensing phase, $S_1$ and $S_1'$ are open, $S_2$ and $S_2'$ are closed. The CVC functions as a charge integrator and the output dc voltage is given by:

$$V_{\text{out}} = \frac{\Delta C}{C_i} \frac{V_{dd}}{2}$$  \hspace{1cm} (1)

During the reset phase, $S_1$ and $S_1'$ are closed, $S_2$ and $S_2'$ are open. By releasing the charge periodically, this switching bias strategy suppresses the undesirable charge leakage to or from the sensing electrode and eliminates the bias voltage drift caused by charging. When reset phase is over, $S_1$ and $S_1'$ are open before $S_2$ and $S_2'$ are closed to avoid shorting between power rails.

In order to assess the validity of the proposed CVC, it is used to convert the output of a three plate capacitive pressure sensor [7] to voltage. Under external pressure, the capacitance of the variable sensor changes from 1.26pF to 2.06pF while the reference sensor is fixed at 1.26pF. $C_p$ is typically around 4pF and feedback capacitor $C_i$ is selected to be 1.65pF as a tradeoff between the circuit noise density and the output voltage range [1]. According to the system requirements, the CVC should be able to detect 0.06% of the maximum capacitance change.

3. OP AMP design

Op amp being the key unit of the whole circuit, the CVC design is started with op amp design. To translate the CVC requirements to op amp specifications, several non-idealities have to be considered.

As indicated in equation (1), the CVC provides a nominal voltage gain of $\Delta C/C_i$. We now calculate the actual gain if the op amp exhibits a finite dc gain of $A_{VO}$. An exact analysis shows that the output voltage of the CVC can be expressed as [8]:

$$V_{\text{out}} = \frac{\Delta C}{C_i + C_p/A_{VO}} \frac{V_{dd}}{2} = \frac{\Delta C}{C_i} \left( 1 + \frac{C_p}{C_i A_{VO}} \right) \frac{V_{dd}}{2} - \frac{\Delta C}{C_i} \left( 1 - \frac{1}{F_{CV} A_{VO}} \right) \frac{V_{dd}}{2}$$  \hspace{1cm} (2)

where $C_i = 2C_s + \Delta C + C_p + C_s$ and $F_{CV} = C_i/C_s$. Equation (2) implies that the amplifier suffers from a gain error of $1/(F_{CV} A_{VO})$. Assume $F_{CV} = 0.193 (C_s = 1.65pF$ and $C_p = 8.57pF$), the op amp dc gain should be greater than 8600 so that the gain error is below 0.06%.
Another non-ideality is the offset. There are two types of offset: the mismatch between nominal capacitance of the sensor pair and op amp offset. To explore their effects on the circuit performance, let's consider the schematic diagram shown in Figure 2.

Several components have been added, $\Delta C_m$ is the pressure sensor nominal capacitance mismatch and $V_{OS}$ represents the op amp offset. The output voltage can be re-derived as:

$$v_{out} = \frac{\Delta C}{C_1} \frac{V_{dd}}{2} + \frac{\Delta C_m}{C_1} \frac{V_{dd}}{2} + V_{OS}$$

(3)

Equation (3) indicates that the output voltage is modified by including two additional terms. However, the second term and third term corresponding to two offset components are both constants, which can be easily cancelled through calibration.

Once the system non-idealities are explored, the next step is to determine an appropriate op amp topology for the CVC. Commonly used op amps are two-stage Miller, telescopic and folded cascade amplifiers. For pressure sensor applications, since the op amp needs to drive capacitive load and the output voltage should be able to go down to the same potential as the input, Miller and telescopic amplifiers are not suitable. Therefore, folded cascade op amp is chosen.
Schematic for the folded cascode amplifier is shown in Figure 3. Several design guidelines are followed to optimize the op amp noise performance. Thermal noise is minimized by choosing the (W/L) ratio of the input pair larger than one of the active load, whereas to curtail the flicker noise, the area of the input PMOS transistors is increased by using 0.6μm as the gate length and active load is made longer than the input pair [9]. Because the capacitance change of the variable pressure sensor and output voltage is always positive, modified cascode current mirror is used to improve the upward swing of the op amp.

Table 1 lists some op amp specifications from simulation. Important performance indexes, for example the dc gain and output swing are over-designed a bit in case of fabrication variation.

| Specification | DC gain | Output swing | Unity GB | Phase margin | Power consumption |
|---------------|---------|---------------|----------|--------------|------------------|
| Value         | 79dB    | 0.91–2.78V    | 35MHz    | 68°          | 1mW              |

4. Control logic implementation
To establish the bias voltage at sensing electrode, the CVC is reset once every 256 clock cycles to release the undesirable charge (this clock down-conversion ratio is non-critical and can be determined according to the system requirements). Small size MOS switches (W/L=1/0.35) are used to minimize both leakage current and parasitic capacitance. S1 and S2' are PMOS switches, S2 is NMOS switch and S1' is PMOS switch with half size dummy on the left. The generator circuit and simulation results are shown in Figure 4.

![Figure 4. (a) Generator and (b) clock diagram of bias reset signals](image-url)
In the sensing phase, switches S1 and S1’ are open, S2 and S2’ are closed. The CVC is basically a charge integrator. During the reset phase, switches S2 and S2’ are open and S1 and S1’ are closed and excess charge at the sensing electrode is released. When reset phase is over, S1’ is switched off first and almost half of its channel charge injects into the sensing electrode. Next, S1 is open, although it has the same charge injection problem as S1’, the injected charge from S1 does not disturb charge conservation at the sensing node because the bypass switch S1’ is already open. As can be seen from Figure 4(a), two inverters are placed between S1 and S1’ to introduce this small delay. The charge injected to compensate must remain in the sensing electrode and this cannot be the case if S1’ is still closed in the process of closing its dummy. Therefore, three inverters are added between S1’ and S1D’ (the dummy switch control signal) to achieve the delay. Finally, S2 and S2’ are closed and the CVC resumes sensing phase.

The ac impedance of the biasing circuit is determined by the off-resistance of the reset switches whose value is normally in the range of $G\Omega$. Parasitic capacitance of the biasing network is the junction capacitance of the small size switches which is only several fF. Compared with resistor-based biasing, this biasing strategy has the advantages of robust dc path, high ac impedance and small parasitic capacitance. Also, unlike the SC circuits, by resetting once every 256 clock cycles, the noise folding is reduced by a factor of 256 and thus becomes insignificant.

5. Simulation results and discussion

Simulation results have been provided in section 3 and section 4 to verify theoretical performance of the op amp and digital control logic. In this section, the two function blocks will be integrated and system level simulation will be carried out using 0.35\(\mu\)m device BSIM3 models. First, transfer characteristics between the capacitance change $\Delta C$ and output voltage $v_{out}$ is studied through parameter sweep. Then, noise analysis is carried out to obtain the output noise and compare it with the required capacitance resolution.

To extract the C-V curve, 100kHz square wave is selected to be the clock base and $\Delta C$ sweeps from 0 to 0.8pF with a step of 0.1pF. Simulation results are plotted in Figure 5. As shown, the C-V relationship is highly linear and the slope is equal to one, which is in accordance with equation (1). Also, the C-V curve is parallel shifted by the same amount as the offset voltage, which indicates that the offset error can be easily removed through calibration. The capacitance resolution obtained from simulation is 0.03%.

![Image of C-V transfer characteristic](image)

**Figure 5. C-V transfer characteristic**

Circuit configuration for noise analysis is shown in Figure 6. $R_p$ represents the interconnect resistance. $C_p$ is decomposed into three parts: parasitic of the pressure sensor $C_{ps}$, parasitic at the sensing electrode $C_{pa}$ and parasitic of the op amp input transistors (which is not shown in the diagram). $\Delta C$ is selected to be 0.4pF. As a simulation trick, a dummy huge resistor $R_{bias}=1G\Omega$ is used for biasing whose noise contribution can be ignored. Noise analysis sweeps frequency from 0.1Hz to 10GHz. 
From simulation, the output noise voltage at \( V_x \) is 156.8\( \mu \text{V} \), which corresponds to 0.0196\% of the total capacitance change and is below the required capacitance resolution 0.06\%.

The simulation results show that the targeted specifications have been met and the CVC can measure the capacitance change with high resolution. The CVC is designed mainly for a pressure sensor; however, it can be modified for other types of capacitive sensors as well. The capacitance change of accelerometers and gyroscopes, for instance, is differential and can be either positive or negative. Therefore, fully differential op amp should be used and downward swing of the op amp needs to be improved to make the CVC output swing symmetrical. Other applications require the noise floor of the CVC ultra low. In such cases, more advanced circuit topologies such as chopper stabilization amplifier can be utilized.

6. Conclusion
This paper presents a continuous-time capacitance to voltage converter suitable for micro-capacitive pressure sensor applications. The proposed CVC has the merits of low noise, linear capacitance to voltage transfer characteristics and low susceptibility to system offset. A CVC has been designed with standard 0.35\( \mu \)m CMOS technology for a three plate capacitive pressure sensor. For a 3.3-V supply, it achieves 1mW power consumption, 0-0.8pF detection range and 0.06\% resolution. Simulation results based on the proposed design are given which closely agree with the theoretical analysis. The CVC will be sent for fabrication and experimental results will be obtained in the near future.

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