Design and Implementation of Full Adder using Different XOR Gates

D. Durga Prasad, M. Dileep, Ch. Rama Krishna

Abstract: A Full Adder is a logical circuit that serves a great part in the design of application particular integrated circuits. It is the basic component found in VLSI and DSP applications. The applications of Full adder in VLSI include ALU design, Address generation in processors, Multipliers and so on. Power consumption is one of the most significant parameters of full adder. Therefore, reducing power consumption in full adder is very important. In this paper, Design XOR gate using Transmission gate logic (TGL), Pass transistor logic (PTL) and Static Complementary metal oxide semiconductor logic (CMOS). Also design Full Adder circuit using different XOR gate designs. These circuits are designed and implemented, simulated using Mentor Graphics Tool. After getting simulation results, compare the different XOR gate designs based full adders in terms of power consumption and delay. Using the comparative analysis for the designed Full Adders, an effective adder design can be chosen based on the performance criteria as required by the designer.

Keywords: Full Adder, TGL, PTL, Mentor Graphics Tool.

I. INTRODUCTION

There are different type of arithmetic operations as follow, Addition, Multiplication, Subtraction, Division and Address Calculation. In VLSI systems most commonly used operation is Addition. Full Adder is designed using binary adders and improving the performance of full adder by 1-bit is a significant role in VLSI. By using the various types of full adders we can design different technologies and logical designs, and an important goal of these technologies is to reduce power consumption and also to increase speed. The adder performance can be improved by two methods and one of the methods is as follows. The two methods are System level viewpoint method and Circuit style viewpoint method. In first method, System level viewpoint, in this longest signal path is determined in ripple adders also decrease the trail to scale back the full signal path delay. Where, the carry out bit of highly significant bit is calculated there will be a longest path. Coming to next method Circuit style viewpoint method, high performance full adder is designed by using semiconductor level design skills. To prevent decrease in signal magnitude, we require an optimized design, which also consume less power, provide small delays even at little voltage supply maintain consistency in critical paths while moving headed for smaller designs such as in nanometre range.

II. REVIEW OF XOR GATE

Mostly, By using XOR, AND, OR gates full adders are designed. While designing full adder, the major consumer of power is XOR gate. Consequently, The power consumption will be decreased in full adder, by designing the XNOR/XOR gates in optimum way. Mainly, the applications of digital circuits design are done by implementing XOR/XNOR gates. Also several other circuits are proposed with this implementation of XNOR/XOR gates.

By using Pass Transistor logic, Transmission gate logic and CMOS logic XOR gate was designed.

III. XOR GATE USING CMOS LOGIC

CMOS devices will have two important characteristics as mentioned below, they are high noisy immunity and low static power. One of transistor pair will be always in off condition. While switching between off and on states, significant power will be drawn by series combination momentarily. Where CMOS circuits will not produce that much waste heat likewise other logics, for example transistor-transistor logic (logic) or, N-type metal-oxide-semiconductor logic (NMOS), these will have a certain amount of standing current when they are not changing their state. In chip, high density logic functions are allowed by CMOS. Due to this reason, CMOS were highly used in implementing VLSI (very large scale integration) chips. The real architecture of particular field-effect transistors is referenced by the phrase “metal-oxide-semiconductor”, with an electrode of metal gate at the leading position of oxide insulator, and it is the turn on top of the semiconductor. Previously aluminium material was used, but now we are using polysilicon material. In CMOS process, remaining metal gates are come back with high-k dielectric material, during the time, which was announced by Intel for the 45-nanometre nodes and which are smaller in sizes. Many of the complex logics are involved with OR and AND logic gates require wielding the ways among gates that represents the logic. Both the two transistors will have low resistance when, path dwells of those transistors are in series. It also to the corresponding supply voltage, modelling an AND. Either one of both transistors will have low resistance when they are in parallel and corresponding supply voltage is modelling an OR. The below figure.
1 shows XOR Gate using CMOS Logic.

**B. XOR GATE USING TRANSMISSION GATE LOGIC**

The signal level from input to output will be selectively passes or blocked by an electronic element, which can be defined as an analog switch or transmission gate. pMOS and nMOS transistors are there in this solid state switch. Both the transistors are made on or off based on the biasing in a complementary manner of a control gates. With almost any voltage potential it can be blocked by a control signal or conduct in both directions, which is similar to relay. It is a switch based upon CMOS, in which nMOS passes a good output 0 but weak 1, and pMOS passes good output of 1 but weak 0. These two transistors, pMOS and nMOS work parallelly.

According to the basis, by using two field effect transistors we used to construct the transmission gate and substrate is not connected source terminal internally, which are in contrast with field effect transistors. The terminals of transistors, i.e., drain and source are contacted together because, a p and n-channels MOSFETS are contacted in shunt connection. To form control terminal we use inverter (NOT gate) to connect their gate terminals.

Here unlike the FET the source connection is not connected with the substrate terminal. To avoid the signal flow affect the parasitic diode is always reversely biased and to the respective supply potential we used to connect the substrate potential. To the positive supply potential substrate of p-channel MOSFET is connected. The n-channel MOSFET is connected to the negative supply potential. The below figure 2 shows the XOR Gate based on Transmission Gate Logic.

**III. RESULTS AND DISCUSSION**

In Mentor Graphics Tool we implemented and resembled all the circuits and observed the output waveforms of each circuit.
A. IMPLEMENTATION OF XOR GATE

In fig.4 the simulation schematic of XOR Gate based on Pass transistor logic is shown and in fig.5 simulation waveform is shown.

![Fig.4. Simulation schematic of XOR gate based on Pass Transistor logic](image)

![Fig.5. Simulation waveform of XOR Gate based Pass Transistor Logic](image)

In the below fig.6 the simulation schematic of XOR Gate based on the transmission gate logic is shown and in Fig.7 simulation waveform is shown.

![Fig.6. Simulation schematic diagram of XOR Gate based on transmission gate logic.](image)

In Fig.8 the simulation schematic diagram of XOR Gate using CMOS logic is shown and simulation waveform diagram is shown in Fig.9.

![Fig.7. Simulation waveform diagram of XOR Gate based on the Transmission gate logic](image)

![Fig.8: Simulation schematic of XOR using CMOS](image)

![Fig.9. Simulation waveform of XOR using CMOS](image)
Design and Implementation of Full Adder using Different XOR Gates

The below Table-I shows the differences between different XOR Gate designs in terms of power dissipation and delay.

### Table-I: POWER DISSIPATION AND DELAY COMPARISON OF XOR GATES

| XOR GATE Design          | Power Dissipation | Delay  |
|--------------------------|-------------------|--------|
| Pass Transistor Logic    | 132.5630 nWatts   | 239.64 ps |
| Transmission Gate Logic  | 301.7342 nWatts   | 49.971 ns |
| CMOS Logic               | 13.9140 mWatts    | 50.158 ns |

**B. IMPLEMENTATION OF FULL ADDER**

In below fig.10 the simulation schematic of full adder is shown.

![Simulation schematic of full adder](image)

**Fig.10. Simulation schematic of full adder**

The simulation waveform of full adder based on CMOS logic, Transmission gate logic & Pass Transistor logic is shown in Fig.11, Fig.12, Fig.13 respectively.

![Simulation waveform of Full Adder based on CMOS logic](image)

**Fig.11. Simulation waveform of Full Adder based on CMOS logic**

![Simulation waveform of Full Adder based on Transmission Gate logic](image)

**Fig.12. Simulation waveform of Full Adder based on Transmission Gate logic**

![Simulation waveform of Full Adder based Pass Transistor Logic](image)

**Fig.13. Simulation waveform of Full Adder based Pass Transistor Logic**

The below Table-II shows the comparison between Full Adder designs in terms of delay and power dissipation.

### Table-II: POWER DISSIPATION AND DELAY COMPARISON OF FULL ADDER

| FULL ADDER Design          | Power Dissipation | Delay  |
|----------------------------|-------------------|--------|
| Pass Transistor Logic      | 916.9071 nWatts   | 49.823 ns |
| Transmission Gate Logic    | 1.4584 uWatts     | 49.835 ns |
| CMOS Logic                 | 1.5880 uWatts     | 49.910 ns |

**IV. CONCLUSION**

Various types of full adder circuits with various logic styles have been implemented. By comparing all the techniques, the Pass Transistor logic based full adder consists of a very less number of transistors, because of a less number of transistors results in less switching activity and area. So Pass Transistor logic based full adder capitate less power dissipation and delay when compare with other logic styles based full adder.
REFERENCES

1. J M. Wang, S C. Fang, W S. Feng, “New efficient designs for XOR and XNOR functions on the transistor level”, IEEE journal of Solid-State Circuits 29 (7), 780-786, (1994).

2. S Issam, A Khater, A Bellouar, M I Elmasry, “Circuit techniques for CMOS low power high performance multipliers”, IEEE Journal of Solid-State Circuits, 31, 1535-1544, (1996).

3. R Zimmermann, W Fichtner, “Low-power logic styles: CMOS versus pass-transistor logic”, IEEE Journal of Solid-State Circuits 32, 1079-1090, (1997).

4. H T Bui, A K A1-Sheraiah, Y Wang, “New four-transistor XOR and XNOR designs”, Published in Proceedings of the 2nd IEEE Asia Pacific Conference ASIC’s pp. 25-28, (2000).

5. M Alioto, G Palumbo, “Analysis and comparison of the full adder block”, IEEE Transaction on Very large scale integration, 10(6), 806-823, (2002).

6. Arkady Morgenshtein, A Fish, Israel A Wagner, Gate-diffusion input (GDI): a power-efficient method for digital combinatorial circuits”, IEEE Transactions on Very large scale integration Systems, 566-581, (2002).

7. A M Shams, T K Darwish, M A Bayoumi, “Performance analysis of low-power 1-bit CMOS full adder cells”, IEEE Transactions on VLSI System 10(1), 20-29, (2002).

8. Y Jiang, A A1 Sheraiah, Y Wang , E Sha, J Chung, “A novel multiplexer-based low-power full adder”, IEEE Transactions on Circuits and Systems II, 51(7)(2004).

9. C H Chang, J Gu, M Zhang, “A review of 0.18 um full-adder performances for tree structure arithmetic circuits”, IEEE Transactions on VLSI Systems, 13 (6) (2005)

10. S Goel, A Kumar, M A. Bayoumi, “Design of robust, energy-efficient full adders for deep sub micrometer design using hybrid-CMOS logic style”, IEEE Transactions on VLSI Systems, 14(12), 1309-1321, (2006).

11. K Navi, M Maaen, V Foroutan, T Timarchi, O Kavehei, “A novel low power full adder cell for low voltage”, Elsevier, 42(4) 456-467, (2009).

12. M H Mosayyeri, R Faghhi Mirzaee, K Navi, T Nikoubin, O Kavehei, “Novel direct designs for 3-input XOR function for low power and high-speed applications”, International Journal of Electronics, 97(6), 647-662, (2010).

13. D Hassoune, I O Flandre, Connor, JD Legat, “ULPFA: a new efficient design of a power-aware full adder”, IEEE Transactions on Circuits and Systems- I, 57(8) (2010).

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