Sigma-Delta ADC Topology Implementation Based on Partial Discharge Detection using Rogowski Coil Sensor

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Abstract. Partial discharge (PD) diagnostic on high voltage (HV) power cables is a modern technology in order to investigate the insulation health. The trending technology such as wireless sensor network (WSN) and internet of thing (IoT) are mostly process in digital signal by microprocessor where looking toward on automatic system. The high performance of analog to digital converter (ADC) in term of sampling rate which is much expensive in order to convert the high frequency of analog PD signal that captured by Rogowski coil (RC) sensor. Thus, this paper propose the implementation of the Sigma-Delta (∑∆) ADC topology in Altera DE0-Nano development board as an effective method in this work to replace the conventional ADC chip and the cost is minimal. Then, peak PD detection technique is applied after the conversion of the digital PD signal. The Verilog hardware description language (VHDL) is used in Quartus II software which corporate with Altera DE0-nano development board for the prototype development. In order to achieve the accurate digital sampling of high frequency PD signal, the N-bit of voltage resolution is paramount.

1. Introduction
Nowadays, early detection on PD signal is useful for maintenance purposes or to schedule arrangement for replacing the HV power cable. The PD detection methods has been divided into four section, which optical detection, acoustic detection, chemical detection and electrical detection [1-2]. However, the electrical detection method is the most favored method in HV power cable for investigation between acoustic, optical and chemical detection due to on capturing the electrical signal [3-4]. The characteristic of the PD signal is low in amplitude and short duration current pulse within a nanosecond to microsecond [5-6]. The information about the insulation degradation and type of PD signal can be determined from the shape of the current pulse within alternating current (AC) cycle when it is occurring. Various types of the conventional current sensor are suggested to detect the PD signals either off-line or on-line technique such as shunt current sensor, HFCT, capacitive couple sensor, RC sensor, hall effect current sensor, giant magneto resistive (GMR) sensor and magneto impedance (MI) sensor [7]. The characteristic comparison between current sensors type are listed in...
Table 1. The selection of air-cored RC sensor as a PD sensor is based on the advantages of sensors which are wide bandwidth, lightweight, linearity, fast response, no hysteresis losses, low cost and easy to construct in the laboratory [8-9].

However, the new trending of technology such as using wireless sensor network (WSN) and internet of thing (IoT) are increasing popular over the world as a smart detection technique [10-13]. Based on previous works in [14-17], the researcher using the external of ADC component in order to convert the analog of PD signal. This paper present the design and implementation of ∑Delta ADC topology in Altera DE0-Nano development board. Figure 1 shows the block diagram of PD measurement setup in this work. The details of ∑Delta ADC topology design and implementation is describe in Section 2, while the PD detection technique is proposed in Section 3. The experimental work is conducted in order for testing and validate the performance for ∑Delta ADC by using the peak detection technique of PD signal captured by RC sensor. Normally, the PD signal range is from 0.5 MHz up to 20 MHz.

Table 1. Comparison between existing current sensors characteristic [7].

| Type of sensor           | Cost | Shunt | CT    | RC    | Hall | GMR    | MI    |
|-------------------------|------|-------|-------|-------|------|--------|-------|
|                         |      | Low   | Medium | Low   | High | Medium | Medium |
| Bandwidth               |      | DC ~ 10 MHz | 0.1 Hz ~ 100 MHz | 0.1 Hz ~ 100 MHz | <1 MHz | DC ~ 5 MHz | DC ~ 30 GHz |
| DC capability           |      | Yes   | No    | No    | Yes  | Yes    | Yes   |
| Linearity               |      | Very  | Fair  | Very  | Poor | Fair   | Fair   |
| Operating temperature   |      | -55 ~ 125 °C | -50 ~ 150 °C | -20 ~ 100 °C | -40 ~ 125 °C | -40 ~ 150 °C | -40 ~ 150 °C |
| Integrity ability       |      | Excellent | Good  | Excellent | Fair | Excellent | Very complicated |
| Material                |      | Simple | Simple | Simple | Complicated |                |
| Technology              |      | Simple | Simple | Simple | Complicated |                |

Figure 1. Block diagram of PD measurement setup

2. ∑Delta ADC Topology Implementation
The design and implementation of ∑Delta ADC using FPGA technology for PD signal output from the RC sensor is conducted in this work. Altera DE0-Nano development board with Cyclone IV chip is used as FPGA board and Quartus II software is a platform for programming and simulation. High speed ADC device is needed to sample the high frequency of PD signal. However, the conventional ADC in the market is commonly is much more expensive in high speed rate. Thus, the ∑Delta ADC topology is selected which has the advantages of using minimum number of small component, low cost and can be design depends on the sampling frequency required. The ∑Delta ADC topology is possible to implement
into the FPGA by taking advantages of the low voltage differential signalling (LVDS) receiver inside the FPGA. The LVDS inside the FPGA is used as a comparator which can reduce the overall external components. Figure 2 shows the basic layout of the ΣΔ ADC implementation on FPGA which divided into two sections, off-FPGA and on-FPGA. The off-FPGA components includes system clock, signal input from PD measurement signal and integrator circuit while, LVDS comparator, Phase-Locked loop (PLL), D flip-flop, summation, edge counter, accumulator, buffer and digital output are implemented digitally in the FPGA chip.

An external resistor, \( R \) and capacitor, \( C \) network known as integrator is required in the feedback system of ΣΔ ADC topology. The main purpose of the \( R \) and \( C \) network act as low pass filter to eliminate the out of band noise during bit stream generated from the sampling process while tracking the signal input. The optimal value of \( R \) and \( C \) can be determined by following Equation 1 based on the sampling frequency, \( f_s \) used in the ΣΔ ADC topology development. The value of \( C \) is fixed to 1 \( \text{nF} \). Thus, the calculated value of \( R \) is 320 \( \Omega \) for 4-bit resolution. By using the ΣΔ ADC topology, high precision component is not required and it has 5 % tolerance for each component. Thus, 300 \( \Omega \) is selected for the \( R \) value in the integrator component.

\[
R = \frac{2^N}{f_s \times C}
\]  

(1)

The Δ part in the yellow box as shown is Figure 2 is operated by the LVDS comparing between the input signal and close loop system from D flip-flop. The input signal from the RC sensor is connected to the positive LVDS comparator input, while the negative LVDS is connected to the integrator. The output of the D flip-flop consist of 1bit bitstream of data which represents the signal input and used for signal tracking through the integrator. To convert this 1bit bitstream of data into useable N-bit digital output, a decimation process is required. Decimation is a process of trading data rates for higher resolution. A uniform decimation process known as averaging decimation is used in the Σ part to demonstrate the effectiveness of the ADC topology. The uniform decimator consist of counter, accumulator and summers. The counter is depends on the number of \( 2^N \)-bit resolution. However, the analysis on different N-bit resolution such as 4, 5, 6, 7 and 8 bits are set in the Verilog HDL of ΣΔ ADC topology based on the selected switch on the FPGA. The summers in the topology will add the accumulated bitstream samples up to the sample number. For example, to convert the bitstream data to a 4-bit output, 16 samples are required and accumulated to produce the output. In this case, the output data rate is reduced by a factor of 16. Thus, if the output resolution is further increase, the output data rate will decrease.

Figure 2. Implementation of Sigma-Delta ADC in FPGA.
PLL is used to increase the 50 MHz on-board system clock to a higher clock frequency required by \( \Sigma \Delta \) ADC sampling. MegaWizard® plug-in manager in the Quartus II software is purposely used to generate the PLL for this system. 320 MHz is the maximum frequency that can be generated in the PLL manager for higher sampling signal. The conversion time of signals depends on the number of N-bit resolution. The N-bit resolution means the unique number of vertical levels of signal divided. The higher number of N-bit resolutions will increase the precision. However, the conversion time will be increased with the same PLL clock. The determination of conversion time, \( t \) is identified by following Equation 2, while the number of samples per 1 µs as follows in Equation 3.

\[
\text{Conversion time, } t = \frac{1}{\text{PLL Clock}} \times 2^{N-\text{bit resolution}}
\]

\[
\text{Number of sample} = \frac{1 \text{ µs}}{\text{Conversion time, } t}
\]

3. PD Detection Method
The PD detection method using a peak detector is introduced in this section. Figure 3 shows the process flow of peak detection technique that has been implemented in Verilog HDL using Quartus II software. The programming starts with the initialization of PD detection counter. The purpose of PD counter is to count the same peak signal in the certain time such as in 0.1 ms. Once the peak signal over than the threshold is detected, the FPGA will check the next peak signal within 0.1 ms. If it has the same peak signal over than the threshold voltage, thus, it is recognized as PD signal. Then, the FPGA will transmit a notification to the receiver at the main unit. If no peak signal is detected for the second time, this system will check for a new detection.

![Figure 3. Process flow for PD detection method.](image)
4. Experimental Setup

Altera DE0-Nano development board with Cyclone IV chip is used as FPGA development board that connected with the RC sensor directly as shown in Figure 1. The dip switch, LEDs, general purpose input output (GPIO) and on-board 50 MHz crystal clock (clk_in) is used in $\Sigma\Delta$ ADC implementation. The device setup should be properly assigned the I/O port for this implementation. The compiled VHDL for $\Sigma\Delta$ ADC only shown in Quartus II software. For hardware implementation, the assigned pin of I/O port using the pin planner, reflects the hardware I/O pin number. Four dip switches (SW) are used to trigger the number of N-bit resolution where, N is equal to 4, 5, 6, 7 and 8. The inLVDS and inLVDS (n) have been assigned for positive and negative input respectively, while eight LEDs (out8b) are used as an indicator of the converted signal from analog to digital.

Then, the FPGA development board is connected with computer (SignalTap II Logic Analyser) and DSO-X 3024A oscilloscope. The SignalTap II Logic Analyser is used as debugging tool in Quartus II software that captured and displays signal in circuit in circuits designed for implementing in FGPA development board. The SignalTap II analyser utilises a universal serial bus (USB) cable to communicate with the FPGA devices. In order to analyse the output from the FPGA, the SignalTap II is used to ensure the digital output is same with the value shows in the oscilloscope.

5. Measurement Results and Discussion

The conversion of the PD signal measured by RC sensor to digital is a key of success in this section. Then, the peak signal is recognized. The assessment begins with the hardware implementation of the basic $\Sigma\Delta$ ADC structure programmed in the Altera DE-0 Nano board with the external op-amp, active filter and RC sensor in PD pulse measurement. The analysis on the number of sample in 1 $\mu$s duration is evaluated based on the number of N-bit resolution as calculated in Table 2 based on Equations 2 and 3. The selection of N-bit resolution value is important to get the accurate peak voltage result as shown in Figure 4 which is 1.026 V.

![Figure 4. Amplify and filtering implementation on RC sensor output results for PD measurement.](image)

| N-Bit resolution | Conversion time, $t$ (ns) | Number of samples |
|------------------|--------------------------|-------------------|
| 4                | 50                       | 20.00             |
| 5                | 100                      | 10.00             |
| 6                | 200                      | 5.00              |
| 7                | 400                      | 2.50              |
| 8                | 800                      | 1.25              |

Table 2. Calculated Value for Sampling Time and Sampling Number in 1 $\mu$s PD Signal.

Figure 5 shows the digital output with a maximum peak of PD signal is 1.026 V at the input of the ADC with the different of resolutions captured by SignalTap II analyser. The aim of this research to implement the $\Sigma\Delta$ ADC topology to replace the conventional ADC chip and to determine the efficiency of high frequency PD sampling signal accuracy.
(a) 16-bit samples with 8 maximum digital output

Range output max. Peak to max. Peak

(b) 32-bit samples with 8 maximum digital output

Range output max. Peak to max.

(c) 64-bit samples with 13 maximum digital output

Range output max. Peak to max.

(d) 128-bit samples with 16 maximum digital output

Range output max. Peak to max. Peak
Figure 5. Sampling signal for PD measurement using $\Sigma\Delta$ ADC topology in SignalTap II analyzer, (a) 4-bit resolutions, (b) 5-bit resolutions, (c) 6-bit resolutions, (d) 7-bit resolutions, (e) 8-bit resolutions.

The analog signal and digital signal is compared in term of the maximum peak signal by following Equation 4 where, the output of Altera DE0-nano board is 3.3 V. The output voltage, $V_{out}$ for digital output signal is summarized in Table 3. Based on the results, it is conclude that, the low resolutions has higher number of samples which more accurate in term of the sampling signal. Thus, 4-bit resolutions is selected in this research as the best resolution for the $\Sigma\Delta$ ADC to sampling the PD measurement output. However, the thresholing method is challenging to decide due to the less of number resolutions. The minimum voltage for 4-bit resolutions is 0.206 V, compare with 8-bit resolutions is 0.013 V. Although, the higher resolutions has a better in minimum digital voltage, but it is difficult to identify the greatest peak voltage as shown in Figure 5 (e) due to the value is really close, compared with 16-bit voltage resolutions.

\[
Output \ voltage, V_{out} = \frac{Output \ of \ FPGA \ port}{Resolutions} \times \ Maximum \ digital \ output
\]  

(4)

Table 3. Digital Output Voltage in Different Resolutions.

| N-Bit | Samples | Maximum digital output | Output voltage, $V_{out}$ |
|-------|---------|------------------------|--------------------------|
| 4     | 16      | 5                      | 1.031                    |
| 5     | 32      | 8                      | 0.845                    |
| 6     | 64      | 13                     | 0.670                    |
| 7     | 128     | 16                     | 0.413                    |

6. Conclusion
FPGA technology is an attractive device to implement digital signal processing technique and applications. The applications of $\Sigma\Delta$ ADC topology is feasible to develop in the FPGA development board in order to convert high frequency of PD signal propagate on the power lines from analog to digital signal captured by RC sensor. The 16-bit voltage resolutions is selected due to the optimum sampling PD signal which have 20 sampling number in 1 µs. Hence, the $\Sigma\Delta$ ADC topology is a novel by implementing in wireless RC sensor development based on PD detection technique and become the preferred solution. The wireless sensor applications can reduce the cost of installation where the wiring is not necessary and no need for manually data collecting in PD monitoring system.
7. References

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