A Memory Controller with Row Buffer Locality Awareness for Hybrid Memory Systems

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This paper summarizes the idea and key contributions of the Dynamic Row Buffer Locality Aware Memory Controller (RBLA), which was published in ICCD 2012 [125], and examines the work’s significance and future potential. Non-volatile memory (NVM) is a class of promising scalable memory technologies that can potentially offer higher capacity than DRAM at the same cost point. Unfortunately, the access latency and energy of NVM is often higher than those of DRAM, while the endurance of NVM is lower. Many DRAM–NVM hybrid memory systems, also known as heterogeneous memory systems, use DRAM as a cache to NVM, to achieve the low access latency, low energy, and high endurance of DRAM, while taking advantage of the large capacity of NVM. A key question for a hybrid memory system is what data to cache in DRAM to best exploit the advantages of each technology while avoiding the disadvantages of each technology as much as possible.

We propose a new memory controller design that improves hybrid memory performance and energy efficiency. We observe that both DRAM and NVM banks employ row buffers that act as a cache for the most recently accessed memory row. Accesses that are row buffer hits incur similar latencies (and energy consumption) in both DRAM and NVM, whereas accesses that are row buffer misses incur longer latencies (and higher energy consumption) in NVM than in DRAM. To exploit this, we devise a policy that caches heavily-reused data that frequently misses in the NVM row buffers into DRAM. Our policy tracks the row buffer miss counts of recently-used rows in NVM, and caches in DRAM the rows that are predicted to incur frequent row buffer misses. Our proposed policy also takes into account the high write latencies of NVM, in addition to row buffer locality and more likely places the write-intensive pages in DRAM instead of NVM.

We evaluate our proposal using a hybrid memory consisting of DRAM and phase-change memory (PCM), a representative type of non-volatile memory. Compared to a conventional DRAM–PCM hybrid memory system that caches frequently-accessed data in DRAM, our row buffer locality-aware hybrid memory system improves average system performance by 14%, and average energy efficiency by 10%, on data-intensive server and cloud workloads. Our proposed hybrid memory system achieves a 31% performance gain over an all-PCM memory system, and comes within 29% of the performance of an all-DRAM memory system (not taking PCM’s capacity benefit into account) on our evaluated workloads.

1. Introduction

Multiprogrammed and multithreaded workloads on chip multiprocessors require large amounts of main memory to support the working sets of many concurrently-executing threads. The demand for memory is increasing rapidly, as the number of cores or accelerators (collectively called agents) on a chip continues to increase and data-intensive applications become more widespread [35, 87, 91, 109]. Dynamic Random Access Memory (DRAM) is used to compose main memory in modern computers. Though strides in DRAM manufacturing process technology have enabled DRAM to scale to smaller feature sizes, and, thus, higher densities (capacity per unit area), it is predicted that DRAM density scaling will result in higher costs and lower reliability as the process technology feature size continues to decrease [19, 45, 50, 64, 75, 87, 88, 91, 99, 117]. Satisfying increasingly higher memory demands with exclusively DRAM will soon become too expensive in terms of both cost and energy.\footnote{We refer the reader to our prior works [17, 18, 19, 20, 39, 40, 48, 49, 50, 51, 52, 53, 61, 62, 63, 64, 65, 67, 68, 93, 105, 107] for a detailed background on DRAM.}

1.1. Non-Volatile Memory

Emerging non-volatile memory (NVM) technologies such as phase-change memory (PCM) [55, 56, 57, 79, 97, 123, 126], spin-transfer torque magnetic RAM (STT-MRAM) [21, 38, 54, 92], resistive RAM (ReRAM) [24, 70, 110], and 3D XPoint [81], have shown promise for future main memory system designs to meet the increasing memory capacity demands of data-intensive workloads. With projected scaling trends, NVM cells can be manufactured more easily at smaller feature sizes than DRAM cells, achieving high density and capacity [21, 25, 26, 38, 54, 55, 56, 57, 70, 79, 92, 97, 99, 119, 123, 126, 131]. This is due to two reasons: (1) while a DRAM cell stores data in the form of charge, an NVM cell uses resistive values to represent the data, which is expected to scale to smaller feature sizes; and (2) unlike DRAM, several NVM devices use multi-level cell technology, which stores more than one bit of data per memory cell.

For example, PCM is a non-volatile memory technology that stores data by varying the electrical resistance of a material known as chalcogenide [55, 99, 123]. A PCM memory...
cell is programmed by applying heat (via electrical current) to the chalcogenide and then cooling it at different rates, depending on the data to be stored. Rapid quenching places the chalcogenide into an amorphous state which has high resistance, representing the bit value of ‘0’ in single-level cell PCM, and slow cooling places the chalcogenide into a crystalline state which has low resistance, representing the bit value of ‘1’ in single-level cell PCM. Multi-level cell PCM can store multiple bits of data by providing more than two distinguishable resistance levels for each cell, very similar to the MLC NAND flash technology that is prevalent in modern storage systems [6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 73, 96, 126].

However, NVM has a number of disadvantages. Compared to DRAM, NVM typically has a longer access latency, higher write energy, and lower endurance [55, 97]. For example, PCM’s long cooling duration required to crystallize chalcogenide leads to high PCM write latency, high read (sensing) latency, high read energy, and high write energy compared to those of DRAM [77]. Furthermore, the repeated thermal expansions and contractions of a PCM cell during programming lead to finite write endurance, which is estimated at $10^8$ writes, an issue not present in DRAM [55].

1.2. Hybrid Memory Systems

Hybrid memory systems [1, 4, 5, 22, 29, 30, 34, 66, 76, 94, 95, 97, 100, 129] aim to combine the strengths of DRAM and emerging memory technologies (e.g., NVM, reduced-latency DRAM [64, 80, 104], reduced reliability DRAM [74, 97]). Many previous DRAM-NVM hybrid memory system designs employ DRAM as a small cache [97] or write buffer [29, 129] to NVM of large capacity. In this work, we utilize PCM to provide increased overall memory capacity (which leads to reduced page faults in the system), while the DRAM cache serves a large portion of the memory requests at low latency and low energy with high endurance. The combined effect increases overall system performance and energy efficiency [97].

A key question in the design of a DRAM-PCM hybrid memory system is how to place data between DRAM and PCM to best exploit the strengths of each technology while avoiding their weaknesses as much as possible.

1.3. Memory Device Architecture

In our ICCD 2012 paper [125], we develop new mechanisms for deciding how data should be placed in a DRAM-PCM hybrid memory system. Our main observation is that both DRAM and PCM devices consist of banks that employ row buffer circuitry. The organization of a memory bank is illustrated in Figure 1. Cells (memory elements) are typically laid out in arrays of rows (cells sharing a common wordline) and columns (cells sharing a common bitline). An access to the array occur at the granularity of a row. To read from the array, a wordline is first asserted to select a row of cells. Then, through the bitlines, the contents of the selected cells are detected by sense amplifiers (labeled S/A in the figure) and latched by peripheral circuitry known as the row buffer.

Once the contents of a row are latched in the row buffer, subsequent memory requests to that row are served promptly from the row buffer, without having to bear the delay of accessing the array. Such memory accesses are called row buffer hits. However, if a row different from the one latched in the row buffer is requested, then the newly requested row is read from the array into the row buffer (replacing the row buffer’s previous contents). Such a memory access incurs the high latency and energy of activating the array, and is called a row buffer miss. Row buffer locality (RBL) refers to the repeated reference to a row while its contents are in the row buffer. Memory requests to data with high row buffer locality are served efficiently (at low latency and energy) without having to frequently re-activate the memory cell array.

2. Row Buffer Locality-Aware Caching Policy

Our ICCD 2012 paper [125] proposes Row Buffer Locality-Aware (RBLA) caching policies, which a hybrid memory controller can use to guide data placement. RBLA can be used in any hybrid memory system where each underlying memory technology consists of banks with row buffers. We study an example hybrid memory system that consists of a large amount of PCM backed by a small DRAM cache [66, 72, 76, 97], whose organization is shown in Figure 2. Our main observation is that memory requests that hit in the row buffer incur similar latencies and energy consumption in both DRAM and PCM [55, 57], whereas requests that miss in the row buffer...
incur higher latency and energy in PCM than in DRAM. As a result, placing data that mostly leads to row buffer hits (i.e., data that has high row buffer locality) in DRAM provides little benefit over placing the same data in PCM. On the other hand, placing heavily reused data that leads to frequent row buffer misses (i.e., data that has low row buffer locality) in DRAM avoids the high latency and energy of PCM array accesses.

This observation is illustrated in the example shown in Figure 3. In the example, the service timelines for memory requests to rows A–D are shown. Prior hybrid memory and cache management proposals seek to improve the reuse of data placed in the cache and reduce the access bandwidth of the next level of memory (e.g., [43, 98]). We call this approach to cache management conventional mapping. Conventional mapping (top half of Figure 3) can place rows A and B (which have low row buffer locality) both in PCM, causing the high PCM array latency to become a bottleneck. In contrast, row buffer locality-aware mapping (bottom half of Figure 3) places rows A and B in DRAM such that they can benefit from DRAM’s lower array latency, leading to faster overall memory service. Place rows C and D (high row locality) in DRAM provides little benefit over placing them in PCM.

Based on this observation, we devise a hybrid memory caching policy that caches in DRAM the rows that mostly miss in the row buffer and are frequently reused. To implement this policy, the memory controller maintains a count of the row buffer misses for recently-used rows in PCM, and places in DRAM the data of rows whose row buffer miss counts exceed a certain threshold (dynamically adjusted at runtime in the RBLA-Dyn mechanism, which we describe in Section 2.3).

### 2.1. Measuring Row Buffer Locality

The RBLA mechanism tracks the row buffer locality statistics for a small number of recently-accessed rows, in a hardware structure called the stats store. The stats store resides in the memory controller, and is organized similarly to a cache, however its data payload per entry is a single row buffer miss counter.

On each PCM access, the memory controller looks for an entry in the stats store using the address of the accessed row. If there is no corresponding entry, a new entry is allocated for the accessed row, possibly evicting an older entry. If the access results in a row buffer miss, the row’s row buffer miss counter is incremented. If the access results in a row buffer hit, no additional action is taken.

#### 2.2. Triggering Row Caching

Rows that exhibit low row buffer locality and high reuse will have high row buffer miss counter values. The RBLA mechanism selectively caches these rows by triggering the caching of a row in DRAM when the row’s row buffer miss counter exceeds a threshold value, MissThresh. Setting this MissThresh to a low value causes more rows with a higher row buffer locality to be cached.

Caching rows based on their row buffer locality attempts to migrate data between PCM and DRAM only when such data movement is beneficial. This affects system performance in three ways. First, placing in DRAM rows that have low row buffer locality improves average memory access latency, due to the lower row buffer miss latency of DRAM compared to PCM. Second, by selectively caching data that benefits from being migrated to DRAM, RBLA reduces unnecessary data movement between DRAM and PCM (i.e., data that frequently hits in the row buffer incurs the same access latency in PCM as in DRAM, and is thus left in PCM). This reduces memory bandwidth consumption, allowing more bandwidth to be used to serve demand requests, and enables better utilization of the DRAM cache space. Third, allowing data that frequently hits in the row buffer to remain in PCM contributes to balancing the memory request load between DRAM and PCM.

To prevent rows with low reuse from gradually building up large enough row buffer miss counts over an extended period of time to exceed MissThresh and trigger row caching, we...
apply a periodic reset to all of the row buffer miss count values. We set this reset interval to 10 million cycles empirically.

2.3. Dynamic Threshold Adaptation: RBLA-Dyn

We improve the adaptivity of RBLA to workload and system variations by dynamically determining the value of MissThresh. The key idea behind this scheme, which we call RBLA-Dyn, is that the number of cycles saved by caching rows in DRAM should outweigh the cost of migrating that data to DRAM. RBLA-Dyn estimates, on an interval basis, the first order cost and benefit of employing a certain MissThresh value, and increases or decreases the MissThresh value to maximize the net benefit (i.e., benefit minus cost).

Since data migration operations can delay demand requests, we approximate cost as the number of cycles spent migrating each row across the memory channels \( t_{\text{migration}} \) times the number of rows migrated \( \text{NumMigrations} \):

\[
\text{Cost} = \text{NumMigrations} \times t_{\text{migration}}
\]  

(1)

If these data migrations are eventually beneficial, the access latency to main memory will decrease. Hence, we can compute the benefit of migration as the number of cycles saved by accessing the data from the DRAM cache as opposed to PCM:

\[
\text{Benefit} = \text{NumReads}_{\text{dram}} \times (t_{\text{read,pcm}} - t_{\text{read,dram}}) + \text{NumWrites}_{\text{dram}} \times (t_{\text{write,pcm}} - t_{\text{write,dram}})
\]  

(2)

In this equation, \( \text{NumReads}_{\text{dram}} \) and \( \text{NumWrites}_{\text{dram}} \) are the number of reads and writes performed in DRAM after migration, \( t_{\text{read,dram}} \) and \( t_{\text{write,dram}} \) are the read and write latency of a DRAM row buffer miss, and \( t_{\text{read,pcm}} \) and \( t_{\text{write,pcm}} \) are the read and write latency of a PCM row buffer miss. RBLA-Dyn accounts for reads and writes separately, as they incur different latencies in many NVM technologies, such as PCM.

RBLA-Dyn uses a simple hill-climbing algorithm (see Algorithm 1 in our ICCD 2012 paper [125]) to find the value of MissThresh that maximizes the net benefit. The algorithm is executed at the end of each interval (10 million cycles in our setup). We refer the reader to Section IV-C of our ICCD 2012 paper [125] for more details on the RBLA-Dyn mechanism.

2.4. Implementation and Hardware Cost

The primary hardware cost incurred in implementing a row buffer locality-aware caching mechanism on top of an existing hybrid memory system is the stats store. We model a 16-way, 128-set, LRU-replacement stats store using 5-bit row buffer miss counters, which occupies a total of 9.25 KB. This stats store achieves within 0.3% of the system performance (and within 2.5% of the memory lifetime) of an unlimited-sized stats store for RBLA-Dyn.

3. Evaluation Methodology

We use a cycle-level in-house x86 multi-core simulator, whose front-end is based on Pin. The simulator is an early predecessor of Ramulator [53, 103] and the ThyNVM simulator [100]. We collect results using multiprogrammed workloads consisting of server- and cloud-type applications (including TPC-C/H [118], Apache Web Server, and video processing benchmarks) for a 16-core system. We compare our row buffer locality-aware caching policy (RBLA) against a policy that caches data that is frequently accessed (FREQ, similar in approach to [43]). We use this competitive baseline because we find that conventional LRU caching performs worse due to its high memory bandwidth consumption. FREQ caches a row when the number of accesses to the row exceeds a threshold value. FREQ-Dyn adopts the same dynamic threshold adjustment algorithm as RBLA-Dyn (Section 2.3). Our methodology and workloads are described in detail in Section VI of our ICCD 2012 paper [125].

4. Evaluation

Performance. Figure 4 shows the weighted speedup of the four caching techniques that we evaluate. As we observe from the figure, RBLA-Dyn provides the highest performance (14% improvement in weighted speedup over FREQ) among the four techniques. RBLA and RBLA-Dyn outperform FREQ and FREQ-Dyn, respectively, because the RBLA techniques place data with low row buffer locality in DRAM where it can be accessed at the lower DRAM array access latency, while keeping data with high row buffer locality in PCM where it can be accessed at the already-low row buffer hit latency.

![Figure 4: Weighted speedup of the four caching techniques: FREQ, FREQ-Dyn, RBLA, and RBLA-Dyn. Reproduced from [125].](image)

Thread Fairness. Figure 5 shows the fairness of each caching technique. We measure fairness using maximum slowdown [3, 27, 28, 51, 52, 86, 112, 113, 115, 121, 122], which is the highest slowdown (reciprocal of speedup) experienced by any benchmark within the multiprogrammed workload. A lower maximum slowdown indicates higher fairness. We observe from the figure that RBLA-Dyn provides the highest thread fairness (6% improvement in maximum slowdown over FREQ) out of all evaluated policies. RBLA-Dyn throttles back on non-beneficial data migrations, reducing the amount of memory bandwidth and DRAM space consumed due to such
we discuss in detail in our ICCD 2012 paper \[125\], RBLA-Dyn achieves the highest memory energy efficiency (10% improvement over FREQ) compared to other policies, in terms of performance per Watt. This is because RBLA-Dyn places data with low row buffer locality in DRAM, making the energy cost of row buffer miss accesses lower than it would be if such data were placed in PCM. RBLA-Dyn also reduces energy consumption by reducing the amount of non-beneficial or useless data migrations.

**Memory Energy Efficiency.** Figure 6 shows that RBLA-Dyn achieves the highest memory energy efficiency (10% improvement over FREQ) compared to other policies, in terms of performance per Watt. This is because RBLA-Dyn places data with low row buffer locality in DRAM, making the energy cost of row buffer miss accesses lower than it would be if such data were placed in PCM. RBLA-Dyn also reduces energy consumption by reducing the amount of non-beneficial or useless data migrations.

We provide the following other evaluation results in Section VII of our ICCD 2012 paper \[125\]:

- Impact of RBLA-Dyn on average memory latency (Section VII-A of \[125\]).
- Impact of RBLA-Dyn on DRAM and PCM channel utilization (Section VII-A of \[125\]).
- Memory access breakdown of each workload to DRAM and PCM (Section VII-A of \[125\]).
- Impact of RBLA-Dyn on PCM lifetime (Section VII-D of \[125\]).
- Comparison with all-PCM and all-DRAM systems (Section VII-E of \[125\]).

As we discuss in detail in our ICCD 2012 paper \[125\], RBLA-Dyn bridges the gap in performance between homogeneous all-DRAM and all-PCM memory systems of equal addressable capacity (achieving within 29% of the performance of an all-DRAM system, and improving performance by 31% over an all-PCM system), while providing close to seven years of memory lifetime.\(^3\)

We conclude that taking row buffer locality into account enables new hybrid memory caching policies that achieve high performance and energy efficiency.

5. Related Work

To our knowledge, our ICCD 2012 paper \[125\] is the first work to observe that row buffer hit latencies are similar in different memory technologies, and uses this observation to devise a caching policy that improves the performance and energy efficiency of a hybrid memory system. No previous work, as far as we know, considered row buffer locality as a key metric for deciding what data to cache and what not to cache. We discuss related work on caching policies and hybrid memory systems.

**Caching Based on Data Access Frequency.** Jiang et al. \[43\] propose caching only the data that experiences a high number of accesses in an on-chip DRAM cache (in 4–8 KB block sizes), to reduce off-chip memory bandwidth consumption. Johnson and Hwu \[44\] use a counter-based mechanism to track data reuse at a granularity larger than a cache block. Cache blocks in a region with less reuse bypass a direct-mapped cache if that region conflicts with another that has more reuse. We propose to take advantage of row buffer locality in memory banks when employing off-chip DRAM and PCM. We exploit the fact that accesses to DRAM and PCM have similar average latencies for rows that have high row buffer locality.

Ramos et al. \[98\] adapt a buffer cache replacement algorithm to rank pages based on their frequency and recency of accesses, and place the highly-ranking pages in DRAM, in a DRAM-PCM hybrid memory system. Our work is orthogonal, because the page-ranking algorithm can be adapted to rank pages based on their frequency and recency of row buffer misses (not counting accesses that are row buffer hits), for which we expect improved performance.

**Caching Based on Locality of Data Access.** Gonzalez et al. \[37\] propose placing data in one of two last-level caches depending on whether it exhibits spatial or temporal locality. They also propose bypassing the cache when accessing large data structures with large strides (e.g., big matrices) to prevent cache thrashing. Rivers and Davidson \[101\] propose separating out data without temporal locality from data with, and placing it in a special buffer to prevent the pollution of the L1 cache. These works are primarily concerned with on-chip L1/L2 caches that have access latencies on the order of a few to tens of processor clock cycles, where off-chip memory bank row buffer locality is less applicable.

\(^3\)Note that lifetime can be further improved by enabling more aggressive write optimization \[106\], and by taking advantage of application-level error tolerance \[74\].
There have been many works in on-chip caching to improve cache utilization (e.g., a recent one uses an evicted address filter to predict cache block reuse [108]), but none of these consider the row buffer locality of cache misses.

Caching Based on Other Criteria. Chatterjee et al. [22] observe that the first word of cache blocks is critical to performance, and propose to store only the first word of each block in fast DRAM. Phadke and Narayanasamy [95] propose to classify applications into three categories based on memory-level parallelism (MLP): latency-sensitive, bandwidth-sensitive, and insensitive-to-both. To estimate MLP, they profile the misses per kilo-instruction (MPKI) and stall time of each application offline during the compilation stage. Applications with high MPKI but low stall time are considered to have good MLP.

Hybrid Memory Systems. Qureshi et al. [97] propose increasing the size of main memory by adopting PCM, and using DRAM as a conventional cache to PCM. The reduction in page faults due to the increase in main memory size brings performance and energy improvements to the system. Our ICCD 2012 paper [125] proposes a new, effective DRAM caching policy to PCM, and studies performance effects without page faults present.

Li et al. [66] propose UHM, a utility-based hybrid memory management mechanism that expands upon our RBLA policy. UHM estimates the utility of each page, which is the benefit to system performance of placing each page in different types of memory (e.g., DRAM and NVM). UHM migrates to the fast memory of a hybrid memory system only those pages whose utility would improve the most after migration.

Ren et al. [100] propose ThyNVM, which manages the DRAM and PCM spaces carefully and adapts the granularity of management to the access patterns in a manner that provides crash consistency in a persistent memory system.

Dhiman et al. [29] propose a hybrid main memory system that exposes DRAM and PCM addressability to the software (OS). If the number of writes to a particular PCM page exceeds a certain threshold, the contents of the page are copied to another page (either in DRAM or PCM), thus facilitating PCM wear-leveling. Mogul et al. [82] suggest that the OS exploit metadata information available to it to make data placement decisions between DRAM and non-volatile memory. Similar to [29], their data placement criteria are centered around the write frequency to data. Our proposal is complementary to this work, and row buffer locality information, if exposed, can be used by the OS to place pages in DRAM or PCM.

Bivens et al. [4] examine the various design concerns of a heterogeneous memory system such as memory latency, bandwidth, and endurance requirements of employing storage class memory (e.g., PCM, STT-MRAM, NAND flash memory). Their hybrid memory organization is similar to ours and that in [97], in that DRAM is used as a cache to a slower memory medium, transparently to software. Phadke et al. [95] propose to profile the memory access patterns of individual applications in a multi-core system, and place their working sets in the particular type of DRAM that best suits the application’s memory demands. In contrast, RBLA dynamically makes fine-grained data placement decisions at a row granularity, depending on the row buffer locality characteristics of each page.

Agarwal et al. [1] propose a software-based approach to manage huge pages (e.g., 2MB pages) in hybrid memory systems. The mechanism profiles the memory access patterns of huge pages, and uses the profiling information to guide page migration between DRAM and NVM. Peña and Balaji [94] propose a profiling tool to assess the impact of distributing memory objects across memory devices in hybrid memory systems. Bock et al. [5] propose a scheme that allows concurrent migration of multiple pages between different types of memory devices without significantly affecting the memory bandwidth. Gai et al. [34] propose a data placement scheme that aims to minimize the energy consumption of hybrid memory systems. Liu et al. [69] propose a scheme that manages the entire memory hierarchy, which includes caches, memory channels, and DRAM/NVM banks. Dulloor et al. [30] propose a programmer-guided data placement tool, which requires programmers to modify the source code, and needs data from a representative profiling run of the application, prior to making placement decisions. Ideas from all of these works can be combined with RBLA for better performance and efficiency.

Exploiting Row Buffer Locality. Many previous works exploit row buffer locality to improve memory system performance, but none (to our knowledge) develop a cache data placement policy that considers the row buffer locality of the block to be cached. Lee et al. [55, 56, 57] propose to use multiple short row buffers in PCM devices, much like an internal device cache, to increase the row buffer hit rate. Meza et al. [77] examine the case for small row buffers for NVM devices. Sudan et al. [116] propose a mechanism that identifies frequently referenced sub-rows of data, and migrates them to reserved rows. By co-locating these frequently accessed sub-rows, this scheme aims to increase the row buffer hit rate of memory accesses, and improve performance and energy consumption. DRAM-aware last-level cache writeback schemes [60, 111] speculatively issue writeback requests that are predicted to hit in the row buffer. RBLA is complementary to these works, and can be applied together with them because RBLA targets a different problem.

Row buffer locality is also commonly exploited in memory scheduling algorithms. The First-Ready First-Come-First-Serve algorithm (FR-FCFS) [102, 132] prioritizes memory requests that hit in the row buffer, improving the latency, throughput, and energy cost of serving memory requests. Many other memory scheduling algorithms [3, 31, 32, 33, 36, 41, 42, 46, 47, 51, 52, 58, 59, 60, 71, 83, 84, 85, 86, 89, 90, 111, 112, 113, 114, 115, 120, 121, 124, 130] build upon this "row-hit first" principle.
Muralidhara et al. [86] use a thread’s row buffer locality as a metric to decide which channel the thread’s pages should be allocated to in a multi-channel memory system. Their goal is to reduce memory interference between threads, and as such their technique is complementary to ours.

6. Significance

Our ICCD 2012 paper [125] makes several novel contributions that we expect will have a long-term impact on the design of memory systems, and we believe that our work inspires several new research questions.

6.1. Long-Term Impact

The memory scaling bottleneck continues to be a significant hurdle to system performance and energy efficiency [87, 88, 91]. Emerging applications operate on increasingly-larger sets of data, and require high-capacity, high-performance main memories, but the poor scaling of DRAM limits the ability of these applications to fit their entire working sets within a DRAM-based main memory. Because DRAM cannot keep pace with application needs, we expect that the demand for alternative memory technologies will continue to grow in the coming years.

Hybrid memory systems can allow systems to harness these alternative memory technologies without fully sacrificing the benefits of DRAM. By combining slower but larger memories (e.g., NVM) with faster but smaller memories (e.g., DRAM), a hybrid memory system has the potential to provide the illusion of a fast and large memory system at a reasonable cost. However, as we discuss, this potential can only be realized by carefully considering which pieces of data are placed in each of the constituent memories of a hybrid memory system. To our knowledge, our ICCD 2012 paper [125] is the first to show that the organization of the underlying memory technologies, such as the existence of row buffers, can be used to make more intelligent data placement decisions.

While our ICCD 2012 paper [125] shows the impact of our proposed data placement policy on a hybrid memory consisting of DRAM and PCM, it can be used to enable a wide range of hybrid memory systems. For example, STT-MRAM devices can make use of a row buffer [2, 54, 77, 78], and expensive reduced-latency DRAM devices [80, 104] also make use of a row buffer. RBLA can be used to improve the performance of hybrid memories that include any of these memory technologies, as our general observations on row buffer locality remain the same. We expect that this versatility will increase the potential impact of RBLA, as no single memory technology has yet to emerge as the dominant replacement for DRAM.

6.2. Research Questions

As we show in our ICCD 2012 paper [125], the efficient management of hybrid memory systems requires the identification and consideration of the key similarities and trade-offs of each memory type. An open research question inspired by RBLA’s use of row buffer locality is what other properties of memory systems should hybrid memory management mechanisms consider? For example, one of our recent works [66] incorporates information on memory-level parallelism (MLP) into data placement decisions in hybrid memory management. As that work shows, we can use a combination of access frequency, row buffer locality, and MLP to predict the overall performance impact of migrating a page between each memory type. As future memory technologies are developed, we expect that other such properties will be important to consider, in order to maximize the benefits provided by the hybrid memory system.

Several works propose on-chip DRAM caches [23, 43, 127, 128], where a small amount of DRAM is used as a last-level cache to reduce the number of accesses to a larger off-chip DRAM. This is akin to the design of a hybrid memory system, but there are different trade-offs in each design. For example, while the row buffer hit latency is typically similar across memory technologies in hybrid memories, both a row buffer hit and a row buffer miss take longer when accessing the off-chip DRAM as opposed to accessing the on-chip DRAM cache. This inspires us to ask how can principles of hybrid memory systems be applied to DRAM cache management, and vice versa? Extending upon this, can we design general mechanisms that can be applied to both hybrid memory systems and DRAM cache management? As one example, our recent work [66] on predicting the utility of data placement decisions is highly parameterized, and these parameters can easily be tuned to represent the trade-offs in both hybrid memory systems and in systems with a DRAM cache. We believe and hope that future works should strive to develop other such general mechanisms.

7. Conclusion

Our ICCD 2012 paper [125] observes that row buffer access latency (and energy) in DRAM and PCM are similar, while PCM array access latency (and energy) is much higher than DRAM array access latency (and energy). Therefore, in a hybrid memory system where DRAM is used as a cache to PCM, it makes sense to place in DRAM data that would cause frequent row buffer misses as such data, if placed in PCM, would incur the high PCM array access latency. We develop a caching policy that achieves this effect by keeping track of rows that have high row buffer miss counts (i.e., low row buffer locality, but high reuse) and places only such rows in DRAM. Our final policy dynamically determines the threshold used to decide whether a row has low locality based on cost-benefit analysis. Evaluations show that the proposed row buffer locality aware caching policy provides better performance, fairness, and energy-efficiency compared to caching policies that only consider access frequency or recency. Our mechanisms are applicable to and can improve the performance of other hybrid memory systems consisting of different
technologies. We hope that our findings can help ease the adoption of emerging memory technologies in future systems, and inspire further research in data management policies.

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