Research on temperature sensitivity of Single-event Transient pulse width in 28-nm bulk technology

Bohan Zhang*, Bin Liang¹ and Yahao Fang¹

¹College of Computer Science, National University of Defense Technology, Changsha 410073, China
*Corresponding author’s e-mail: zhangbohan15@nudt.edu.cn

Abstract. The influence of temperature on single-event transient (SET) pulse width has always been a hot issue in the field of anti-irradiation. Based on 3D-TCAD simulation, the temperature sensitivity of the SET pulse width of 28-nm bulk devices has been studied. The simulation results show that the electrical characteristics of the device shows an anti-temperature effect, but the worst case of SET pulse width still occurs at high temperature rather than low temperature. The influence of the triple-well structure on the temperature sensitivity of the SET pulse width has also been studied. The N⁺ deep well can significantly increase the SET pulse width when hitting NMOS device and enhance the temperature sensitivity of the SET pulse width. The research content of this article will provide reference for the design of radiation resistant chip.

1. Introduction

Aerospace application integrated circuits usually need to work in a harsh space radiation environment, so radiation effects will happen when the integrated circuits are bombarded by many high-energy particles in space. In nano-integrated circuits, the single-event transient effect induced by high-energy particles in space seriously threatens the high-reliability and long-life operation of spacecraft in orbit[1]. With the scaling down of technology, single-event transient effect has become more and more serious in nano-integrated circuits[2]. It has become a hot issue in the field of anti-radiation. In the space environment, aerospace application integrated circuits often need to work in extremely low or extremely high temperature environments. Temperature has an impact on electrical parameters such as carrier mobility, threshold voltage, leakage current, and saturation current. The change of electrical parameters and the appearance of new features will all affect the charge collection of the device caused by single-event effect. The amount of charge collection will directly affect the SET sensitivity of the device. Therefore, it is important to study the influence of temperature on the SET pulse width.

The influence of temperature on the pulse width of SET has attracted much attention. It is generally believed that for technology nodes above 45-nm, as the temperature increases, the delay of the transistor increases. The parasitic bipolar amplification effect of the device increases. The charge collection of the device increases. All these lead the increases of SET pulse width[3-5]. As the technology continues to scale down, at technology nodes below 45-nm, the electrical characteristics of the device show an anti-temperature effect. When the temperature decreases, the delay of the transistor increases. That may cause the worst case of the SET pulse width to appear at low temperatures instead of high temperatures[6-7].

In this article, the effect of temperature on the SET pulse width in 28-nm bulk inverter are studied through the method of numerical simulation. The simulation results show that the electrical
characteristics of the 28-nm bulk device have an anti-temperature effect, but the worst case of the SET pulse width still occurs at high temperature rather than low temperature. The influence of triple-well structure on the temperature sensitivity of SET pulse width has also been studied. The experimental results are analysed and discussed from the perspective of charge collection mechanism and saturation current.

The article structure of this article is organized as follows. The second section introduces the establishment of three-dimensional simulation model and the setting of simulation experiment in detail. The third section give the experimental results of the effect of temperature on the SET pulse width. The fourth section study the influence of the triple-well structure on the temperature sensitivity of the SET pulse width. All the experimental results are analysed in depth. Finally, the fifth section summarizes the full text.

2. Device structure and simulation setup

Because the three-dimensional technology computer aided design (3D-TCAD) tool has powerful internal vision capabilities, it is widely used in the simulation study of the single-particle charge collection mechanism of the device. This article uses TCAD software to build device models of negative channel metal oxide semiconductor (NMOS) transistor and positive channel metal oxide semiconductor (PMOS) transistor. The 3D-TCAD models of the device are calibrated according to the 28-nm PDK Library. The 3D-TCAD model of the device and its corresponding structural parameters are shown in Figure 1. The relevant size parameters of the device are shown in Table 1.

\[ \begin{array}{c|c|c}
\text{Parameters} & \text{28-nm NMOS} & \text{28-nm PMOS} \\
\hline
L_g (nm) & 27 & 27 \\
L_s (nm) & 80 & 80 \\
L_d (nm) & 80 & 80 \\
W (nm) & 210 & 310 \\
T_{oxide\ gate} (nm) & 1.4 & 1.4 \\
T_{poly \ gate} (nm) & 14 & 14 \\
\end{array} \]

In order to obtain the SET pulse width caused by heavy ion striking, a first-level inverter is constructed from 28-nm bulk planar NMOS and PMOS transistors for measurement. Because only the devices in the off state are sensitive to the single event effect, the bombarded devices are kept in the off state when simulating heavy ion striking. Therefore, take the analog configuration of the inverter in

Figure 1. (color online) 28-nm bulk device structure diagram, a) NMOS structure diagram, b) PMOS structure diagram
the case of N-hit as an example: set the NMOS transistor to the off state, that is, the input of the inverter is low. The drain of the NMOS device is connected to the drain of the open-state PMOS device. The source, gate and substrate contacts of the NMOS device are respectively connected to the ground GND. The analog configuration of the inverter electrode in the case of P-hit is similar.

For 28-nm bulk devices, the supply voltage $V_{DD}$ is set to 0.9V and the room temperature is 298K. The entire simulation time is $T_0 = 300\text{ps}$, $LET = 40\text{MeV} - \text{cm}^2 / \text{mg}$ heavy ions are incident vertically when $T_i = 100\text{ps}$. Studies have shown that because of the "funnel effect" and the parasitic bipolar amplification effect, the drain region of device has always been the most SET sensitive area[8]. Therefore, the heavy ion striking position is the drain center of the device. The method of calculating the amount of charge collected is the integral of the drain current with respect to time. When removing the bipolar amplification effect and only considering the drift diffusion effect of the device, the transistor with floating source is suspended to simulate the corresponding diode device[9]. The charge collection caused by the parasitic bipolar amplification effect is the device charge collection minus the charge collection of the corresponding diode device.

These following physical models were used[10-11]: (1) Fermi-Dirac statistics, (2) band-gap narrowing effect, (3) doping dependent SRH recombination and Auger recombination, (4) temperature, doping, electric field and carrier-carrier-scattering impact on mobility, (5) hydrodynamic carrier transport model, and (6) Hydrodynamic carrier transport model. Unless otherwise specified, default models and parameters are used.

3. The influence of temperature on SET pulse width

As shown in Figure 2, the broken line shows the variation of SET pulse width with temperature in the inverter under different supply voltages. Because the 28-nm bulk planar device can only work in a small supply voltage range. The SET pulse width with temperature rising from 248K to 398K is measured at low voltage ($V_{DD}=0.7V$), normal supply voltage ($V_{DD}=0.9V$) and high voltage ($V_{DD}=1.1V$). The results are shown in Figure 2. As shown in Figure 2, under three different supply voltages, the SET pulse width in the inverter gradually increases as the temperature rises. The SET in the inverter is the narrowest at 248K while the SET pulse width is the widest at 398K. The worst case of SET occurs at high temperature rather than low temperature.

![Figure 2. (color online) The distribution of the SET pulse width with different temperature under three kinds of supply voltage](image)
temperature rises. As the supply voltage increases, the anti-temperature effect of the device's electrical characteristics is constantly weakening. When VDD=1.1V, the saturation current of the NMOS device at 398K is almost the same as the saturation current at 248K.

![Figure 3](image1.png)  ![Figure 4](image2.png)

**Figure 3.** (color online) The changes of I-V characteristics curve with temperature for 28-nm bulk NMOS device under different supply voltage a) VDD=0.7V, b) VDD=0.9V and c) VDD=1.1V

**Figure 4.** (color online) The changes of charge collection with temperature for 28-nm bulk NMOS device under different supply voltage a) VDD=0.7V, b) VDD=0.9V and c) VDD=1.1V

Figure 4 shows the change in the charge collection by the device with temperature when the supply voltage is 0.7V, 0.9V, and 1.1V. The red line stands for the change of the charge collection of the device with temperature. The green line stands for the change of the charge collection of the corresponding diode device. The difference between the two line is the charge collection caused by the bipolar amplification effect. As shown in Figure 4, the charge collection of the device gradually increases with temperature, but the charge collection of the diode device remains stable. That means the increase in temperature enhances the parasitic bipolar amplification effect of the device. Thereby enhancing the charge collection of the device.

As the temperature increases, the saturation current of the NMOS device gradually decreases, and the charge collection of the device gradually increases due to the parasitic bipolar amplification effect. Under the combined influence of the two factors, the SET pulse width increases with the rising of temperature. The worst case of SET occurs at high temperature rather than low temperature.

4. **The influence of triple-well structure on temperature sensitivity of SET pulse width**

Double-well structure and triple-well structure are two widely used manufacturing structures in bulk technology. Compared with the double-well structure, the triple-well structure is based on the double-well structure, and N+ deep well or P+ deep well are added according to the type of substrate. Because most devices are manufactured on P-type substrates, the triple-well process usually adds a N+ deep well. In the field of radiation strengthening, adding a P+ deep well on a P-type substrate is also a common choice. The P+ deep well has a very small effect on the I-V characteristics of the device. It can effectively reduce the potential disturbance of the well, thereby reducing the amount of charge.
collection of the device, so as to achieve the purpose of reducing the SET pulse width. Figure 5 shows a schematic diagram of the device's double-well structure and triple-well structure. For studying the effect of triple-well structure on the temperature sensitivity of the SET, the SET pulse width of the N+ deep well and P+ deep well are measured.

Figure 5. The schematic cross-sectional view of a) double-well structure and b) triple-well structure

Figure 6. (color online) The changes of SET pulse width with temperature under different well structure

Figure 7. (color online) The changes of charge collection with temperature under different well structure

Figure 6 shows the variation of the SET with temperature. For N-hit, the SET pulse width under the double-well structure and the P+ deep well structure is basically the same. The SET under the N+ deep well structure is significantly larger than that of the double-well structure. What's more, the SET under the deep N+ well structure is more sensitive to temperature than the double-well structure. Many
studies have shown that adding a N+ deep well or a P+ deep well under a dual-well structure has little effect on the I-V characteristics of the device. So the SET of the device mainly relies on the amount of charge collection. Figure 7 shows the change in charge collection with temperature. Under the triple-well structures, the charge collection of the device increases continuously with the temperature. Under the N+ deep well structure, the temperature shows the strongest influence on the collection of charge. While the SET pulse width of the device under P+ deep well show the weakest temperature sensitivity. For the NMOS device in the double-well structure is on a P-type substrate, the parasitic bipolar amplification effect in the NMOS device is very weak. And as the temperature increases, the bipolar amplification effect is relatively gradually increased. When adding a P+ deep well under a double-well structure, the potential perturbation of the substrate will be more difficult to occur than under a double-well structure. Therefore, under the P+ deep well structure, the bipolar amplification effect of the NMOS device is weaker than that under the double well structure. This leads to charge collection increasing slowly with temperature in the P+ deep well structure than in the double well structure. When a deep N+ well is added under the double-well structure, PN junction will be formed between the N+ deep well and the P-type substrate, which will prevent the holes ionized by heavy ions from diffusing into the substrate. This makes the substrate potential perturbation is more likely to occur in N+ deep well structure than in the double-well structure. Therefore, under the N+ deep well structure, the bipolar amplification effect of the NMOS device is stronger than that under the double well structure. This leads to a stronger tendency for the charge collection of the device to increase with temperature in the N+ deep well structure than in the double-well structure. This explains why the SET under N+ deep well shows stronger sensitive to temperature.

5. Conclusion
The single-event transient effect seriously threatens the high-reliability operation of spacecraft in orbit. The influence of temperature on single event transient pulse width has always been a hot issue in the field of anti-radiation. In this paper, the temperature sensitivity of the SET pulse width under the 28-nm bulk technology is comprehensively studied and analyzed. As the temperature increases, the electrical characteristics of the device show an anti-temperature effect, but the worst case of the SET pulse width still occurs at high temperature rather than low temperature. The effect of the triple-well structure on the temperature sensitivity of the SET pulse width is also studied. This article has obtained a lot of original data. The research content of this paper provides theoretical guidance for the research on the single event effect under bulk technology. With the continuous scaling down of the technology nodes, Fin Field-Effect-Transistor (FinFET) has gradually become the mainstream technology of integrated circuit design. So it is important and necessary to study the effect of temperature on SET under FinFET technology in the future research.

Acknowledgments
This project is supported by Natural Science Foundation of China (Grant No. 61974163). Authors would like to thank Lincan Li (Central South University) for her support and encouragement. Yaqing Chi and Jianjun Chen (National University of Defence Technology) are appreciated for the technical discussions.

References
[1] Mahatme, N. N., Jagannathan, S., Loveless, T. D., Massengill, L. W. et al. (2011) Comparison of combinational and sequential error rates for a deep submicron process. IEEE Trans. Nucl. Sci., 58: 2719–2725.
[2] Castellani-Coulie, K., Munteanu, D., Autran, J.L. et al. (2005) Simulation analysis of the bipolar amplification induced by heavy-ion irradiation in double-gate MOSFETs. IEEE Trans. Nucl. Sci., 52: 2137-2143.
[3] Chen, S. M., Liang, B., Liu, B. W., Li, Z. (2008) Temperature dependence of digital SET pulse width in bulk and SOI technologies. IEEE Trans. Nucl. Sci., 55: 2914–2920.
[4] Gadlage, M.J., Ahlbin, J.R., Ramachandran, V., Gouker, P., Dinkins, C.A. et al. (2009) Temperature Dependence of Digital Single-Event Transients in Bulk and Fully-Depleted SOI Technologies. IEEE Trans. Nucl. Sci., 56: 3115-3121.

[5] Chen, R. M., Diggins, Z. J., Mahatme, N. N., Wang, L., Zhang, E. X. et al. (2017) Effects of Temperature and Supply Voltage on SEU- and SET-Induced Single-Event Errors in Bulk 40-nm Sequential Circuits. IEEE Trans. Nucl. Sci., 64: 2122-2128.

[6] Kauppila, J. S., Kay, W. H., Haeffner, T. D., Rauch, D. L., Assis, T. R. et al. (2015) Single-Event Upset Characterization Across Temperature and Supply Voltage for a 20-nm Bulk Planar CMOS Technology. IEEE Trans. Nucl. Sci., 62: 2613-2619.

[7] Zhang, H., Jiang, H., Assis, T. R., Ball, D. R., Ni, K. et al. (2016) Temperature dependence of soft-error rates for FF designs in 20-nm bulk planar and 16-nm bulk FinFET technologies. In: IEEE International Reliability Physics Symposium (IRPS). California.

[8] Fang Y. P., Oates A. S. (2011) Neutron-induced charge collection simulation of bulk FinFET SRAMs compared with conventional planar SRAMs. IEEE Trans. Device Mater. Relib., 11: 551-554.

[9] Ferlet-Cavrois V, Vizkelethy G, Paillet P, et al. (2004) Charge enhancement effect in NMOS bulk transistors induced by heavy ion Irradiation-comparison with SOI. IEEE Trans. Nucl. Sci., 51: 3255-3262.

[10] Chen, J. et al. (2013) Novel layout technique for single-event transient mitigation using dummy transistor. IEEE Trans. Device Mater. Rel., 13: 177–184.

[11] Huang, P. C., Chen, S. M., Chen, J. J., Liang, B. B. (2014) Single event pulse broadening after narrowing effect in nano CMOS logic circuits. IEEE Trans. Device Mater. Rel., 14: 849–856.