Abstract- The advancement of silicon carbide (SiC) power devices with voltage ratings exceeding 10 kV is expected to revolutionize medium- and high-voltage systems. However, present power module packages are limiting the performance of these unique switches. The objective of this research is to push the boundaries of high-density, high-speed, 10 kV power module packaging. The proposed package addresses the well-known electromagnetic and thermal challenges, as well as the more recent and prominent electrostatic and electromagnetic interference (EMI) issues associated with high-speed, 10 kV devices. High-speed switching and high voltage rating of these devices creates significant EMI and high electric field. Existing power module packages are unable to address these challenges, resulting in detrimental EMI and partial discharge that limit the converter operation. This paper presents the design and testing of a 10 kV SiC MOSFET power module that switches at a record 250 V/ns without compromising the signal and ground integrity due to an integrated screen reduces the common-mode current by ten times. This screen connection simultaneously increases the partial discharge inception voltage by more than 50 %. With the integrated cooling system, the power module prototype achieves a power density of 4 W/mm².

I. INTRODUCTION

Wide-bandgap (WBG) semiconductors, such as silicon carbide (SiC), have demonstrated improved efficiency, reduced size and weight, and lower system cost compared to silicon [1],[2],[3],[4],[5]. SiC semiconductors have also demonstrated superior high-voltage capability [3],[4],[6]. While silicon devices have proven reliability and ruggedness, they have limited voltage ratings (typically 6.5 kV or less), thus requiring complex series connection of devices or multilevel converter topologies [7]. Moreover, medium-voltage silicon devices have slow switching speeds, which constrain the efficiency and switching frequency of the power converter [8],[9].

10 kV SiC MOSFETs are of great interest due to their high blocking voltage, fast switching speed, simple drivability, reverse conduction capability, and moderate on-state losses. These features can increase the efficiency, reliability, and switching frequency, and reduce the complexity, size, weight of medium- and high-voltage power conversion systems [10],[11]. Applications include electric ship propulsion [9],[13], data center distribution, direct renewable integration [14], fast charging stations [15], HVDC [16], FACTS [17],[18], and transformer-less intelligent substations [11],[14],[19],[20],[21].

Due to the vast possibilities for ≥10 kV SiC devices, resources have been devoted to their development. Though the majority of the reports on these devices have been focused on the characterization [6],[11],[19],[22],[23],[24], gate drive design [25],[26],[27],[28], and converter evaluation [11],[24],[29]. However, the packaging of the semiconductors has a significant impact on the performance, currently hindering their switching speed, voltage rating, and operating temperature. It is nontrivial to design a suitable package for 10 kV SiC MOSFETs, in addition to the well-known electromagnetic and thermal challenges associated with packaging WBG devices, the voltage rating creates new and more prominent electromagnetic interference (EMI) issues, which require an improved design to utilize the full capabilities of these devices. The first-generation 10 kV SiC MOSFETs were assembled into a power module using a modified 6.5 kV silicon carbide package [30]. Upon analysis and testing of the power module, it was found that the parasitic inductances and capacitances were large and unbalanced [31], limiting the device performance and causing significant EMI. An improved package for third-generation 10 kV SiC MOSFETs was presented in [32]. This package has lower and symmetrical parasitic inductances [32], though improvement in the EMI is unknown.

EMI arises from the voltage and current transients occurring during operation of the switching cell, and conducted through the electrical connections, or radiated by the surrounding space. Typically, filters are added to reduce the EMI; however, these increase the cost, size, and complexity of the power conversion system. Adding external filters diminishes the power density and some benefits gained by using 10 kV SiC MOSFETs.

In particular, conducted common-mode (CM) noise is a major issue with high-speed devices. CM noise is caused by the high-/dV/dt switching of the semiconductor devices, causing current to flow through the parasitic capacitance. These capacitances exist in the power module and auxiliary circuitry, such as the gate driver isolation. The latter has
addressed in other work by reducing the isolation capacitance of the gate driver power supply [25],[26],[27],[28].

To address the issue of current flowing through the parasitic capacitances within the package, [33] proposed a method for balancing the current back to the dc bus by using two stacked direct-bonded-copper (DBC) substrates, where the intermediate metal layer is connected to the positive or negative dc bus. The amount of current that is diverted will strongly depend on the high-frequency impedance of the connection back to the dc bus. Accordingly, the implementation of this screen is critical. In [33], wire bonds are used for the interconnections, and “lugs” are used for the terminals. These connection methods have large parasitic inductances, which will reduce the effectiveness of the screen.

In [34], a similar screen is proposed. The 1.2 kV SiC MOSFET power module in [34] uses a multilayer DBC substrate, and dc-link capacitors located close to the dies. Vias in the multilayer substrate create a low-inductance connection between the middle metal layer and the negative dc bus [34]. The module has a 14-dB reduction compared to the reference module [34],[35]. While this module has several advantageous features, there are some areas for improvement. First, by connecting the middle metal to the negative dc bus, as in [33], the top ceramic is providing all the voltage isolation, and thus the second ceramic is not being fully utilized. Second, by placing the capacitors on the same plane as the MOSFETs, the footprint of the module is significantly increased. Third, the module parasitics are not well balanced, which has been shown to cause greater high-frequency noise compared to balanced designs [36].

The high-voltage rating of the 10 kV SiC MOSFETs poses a challenge for the electrostatic performance. If the electric field exceeds the breakdown field strength of the insulation materials, such as the encapsulation or isolating substrate, then partial discharge (PD) can occur. Repetitive PD events can ultimately result in insulation failure, such as cracking of the ceramic substrate, as shown in [37], thus destroying the power module. Furthermore, the PD inception voltage (PDIV) has been shown to decrease with increased dv/dt and switching frequency [38]. Due to the high-speed switching capabilities of these 10 kV SiC MOSFETs, measures must be taken to reduce the electric field concentration within the power module to ensure sufficient PDIV and breakdown voltage.

In this work, an optimized high-voltage power module package was designed, prototyped, and tested using 10 kV SiC MOSFETs. With the proposed package, the 10 kV SiC MOSFETs are able to switch at record speeds with minimal ringing and voltage overshoot. This fast switching results in significantly reduced switching losses compared to medium-voltage silicon transistors, and allows the switching frequency of medium- and high-voltage converters to be increased by orders of magnitude, which drastically reduces the size of passive components, thereby increasing the system power density. To mitigate the conducted EMI that could result from this high dv/dt, this work proposes to fully integrate a low-inductance screen into the package that limits the amount of CM current that flows out of the power module.

In this paper, the EMI issues encountered during testing of the first-generation 10 kV SiC power modules from [39] are presented, followed by a description of the proposed package for 10 kV SiC MOSFETs. The analysis, implementation, and preliminary testing of the integrated screen will then be discussed. Methods for reducing electric field concentration within the power module were reviewed, and the proposed technique will be analyzed. Finally, the experimental switching tests that demonstrate high-speed transients and low CM current of the proposed package will be presented. Partial discharge tests validating the improved voltage capability provided by the CM screen will also be shown.

II. EMI LIMITATIONS FOR HIGH-VOLTAGE SiC POWER MODULES

The development of 10 kV SiC MOSFETs [39] and SiC junction barrier Schottky (JBS) diodes [40] gave rise to the first 10 kV SiC power module [30]. The half-bridge modules comprise twelve parallel 10 kV, 10 A DMOSFETs, and six parallel 10 kV, 10 A SiC JBS diodes [30]. The 10 kV SiC modules demonstrated higher efficiency, switching frequency potential up to 6.5 kV silicon IGBT modules [8], and were critical components in the development of a high-density 1 MVA solid-state power substation, employed soft switching techniques and was capable of switching up to 20 kHz [41]. These modules were also able to demonstrate the first medium-voltage impedance measurement unit (IMU) capable of characterizing in-situ source impedance of dc and ac networks up to 4160 V ac, 6 dc, 300 A, and 2.2 MVA [42]. Unfortunately, the full power levels could not be achieved due to significant, unresolvable EMI. Upon further evaluation, it was found that substantial current was flowing through the system ground. The contaminated ground was causing the control malfunction, thereby limiting the operating conditions.

As mentioned previously, under a voltage excitation, the parasitic capacitances can become a path for CM current to flow. Within the power module, parasitic capacitances across the ceramic substrate that isolates the semiconductor devices from the cooling system. Since the cooling system is generally grounded for safety, under high-speed transients, this parasitic capacitance becomes a path for CM current to flow through the system ground [36]. Therefore,
capacitance should be minimized, especially for fast-switching devices.

From ANSYS Q3D simulations, the parasitic capacitance between the output node of the half-bridge and the module baseplate is approximately 300 pF. Discrete switching tests were conducted on these power modules to characterize the dynamic performance [43]. At 4.7 kV and 100 A, the power modules had a maximum $dv/dt$ of 22 V/ns [43]. This measured $dv/dt$ and simulated parasitic capacitance give a calculated peak current of nearly 7 A. It should be noted that the 22 V/ns switching speed was achieved with internal and external gate resistances slowing down the devices. If these resistances were reduced or eliminated, then the switching speed would increase, which would raise the efficiency, but worsen the CM current. Therefore, this capacitance is limiting the operation of the 10 kV SiC MOSFETs. The package proposed in this work reduces this EMI without sacrificing the efficiency by minimizing the parasitic capacitance, and integrating a screen that contains the generated CM current within the power module.

III. MODULE OVERVIEW

Fig. 1 shows the designed half-bridge power module, which has three 10 kV, 350 mΩ SiC MOSFET dies in parallel per switch position. No external anti-parallel diodes are used. The module has a planar, sandwich structure, using metal posts and direct-bonded-aluminum (DBA) substrates as the die interconnection instead of wire bonds. Similar structures were proposed in [44] and [45] for lower-voltage silicon IGBTs. This type of structure allows for increased power density, and reduces the parasitic inductances and capacitances in the module, thereby improving the dynamic performance. Furthermore, by eliminating the wire bonds, the module will be able to withstand higher-energy faults, as shown in [46]. This structure also allows decoupling capacitors to be embedded within the module to further improve the dynamic performance without increasing the module footprint.

In total, four substrates are used in the power module: two beneath the dies (DBA1 and DBA2) and two on top (DBA3 and DBA4). DBA1 and DBA2 are used to reduce the CM current flowing through the system ground and to decrease the peak electric field strength within the power module. With the housing and integrated cooler, the module dimensions are 70 mm × 80 mm × 25 mm. Details on the design and prototyping of this power module are reported in [47],[48],[49].

Fig. 1 (a) Schematic and 3D models of the (b) bottom and (c) complete assemblies, (d) side-view of the module, (e) terminal arrangement, and (f) housing with integrated cooler. The colors in the 3D models correspond to the nodes in the schematic with the same color.

Fig. 2 10 kV SiC MOSFET module prototypes with (a) two 10 kV SiC MOSFET dies, and (b) six 10 kV SiC MOSFET dies.

IV. COMMON-MODE SCREEN

A. Impedance Analysis

In this section, the CM path impedances will be analyzed. Fig. 3 shows a schematic of the power module with the key impedances that will be considered. For the generated CM current to be diverted from the ground to the screen, the impedance of the screen path must be much lower than the ground path, especially at high frequency. The condition required for the screen to effectively divert the CM current from the ground path to the dc bus may be summarized as follows:

$$Z_{\text{screen}} \ll Z_{\text{pad}}$$
where \( Z_{\text{screen}} \) and \( Z_{\text{ground}} \) are the impedances of the screen and ground paths, respectively. Considering the parasitic elements shown in Fig. 3, these impedances can be defined as:

\[
Z_{\text{screen}} = oL_{\text{screen}} + 1/(j\omega C_{\text{screen}}) + R_{\text{screen}}
\]

(2)

\[
Z_{\text{ground}} = oL_{\text{ground}} + 1/(j\omega C_{\text{ground}}) + R_{\text{ground}}
\]

(3)

where \( L_{\text{screen}} \) and \( L_{\text{ground}} \) are the parasitic inductances in the screen and ground paths, \( R_{\text{screen}} \) and \( R_{\text{ground}} \) are the parasitic resistances in the screen and ground paths, \( C_{\text{screen}} \) is the decoupling capacitance, and \( C_{\text{ground}} \) is the parasitic capacitance of the bottom substrate, which is connected to ground (Fig. 1(d)). As shown by (2), to minimize \( Z_{\text{screen}} \), \( L_{\text{screen}} \) should be as small as possible, while \( C_{\text{screen}} \) should be large. From (3), it can be seen that a smaller \( C_{\text{ground}} \) results in a greater \( Z_{\text{ground}} \). Substituting (2) and (3) into (1) gives:

\[
oL_{\text{screen}} + 1/(j\omega C_{\text{screen}}) + R_{\text{screen}} < oL_{\text{ground}} + 1/(j\omega C_{\text{ground}}) + R_{\text{ground}}
\]

(4)

From (4), it can be seen that the effectiveness of the screen is dependent on the parasitic elements, which are determined by the implementation. To effectively reduce the CM current, the power module should be compact such that \( C_{\text{ground}} \) and \( L_{\text{screen}} \) are small, yet capable of accommodating sufficient decoupling capacitance \( C_{\text{screen}} \). The \( L_{\text{screen}} \) and \( R_{\text{screen}} \) will vary depending on the system integration, and are therefore out of the control of the power module designer. Accordingly, this work focuses on minimizing \( C_{\text{ground}} \) and \( L_{\text{screen}} \), and maximizing \( C_{\text{screen}} \). A more general theoretical analysis of CM impedances is presented in [50].

### B. Preliminary Testing

Prior to constructing the 10 kV SiC MOSFET power modules, it was desirable to understand the effects of the proposed screen on the CM noise. Accordingly, a half-bridge module with 1.2 kV, 80 mΩ SiC MOSFETS (2MM0080120ID) was built and tested in a boost converter. For the test, the module substrate was directly mounted onto a copper ground plane. No cooling system was added between the substrate and the ground plane to improve the measurement results. Due to the absence of a cooling system, the tests were conducted at low power (360 W). The output voltage was 60 V, and the switching frequency was 50 kHz.

For the prototyped 1.2 kV SiC modules, the parasitic capacitance from the output node to the metal layer \( C_{\text{D2}} \), was 20 pF, and the parasitic capacitance from the metal layer to the ground, \( C_{\text{G2}} \), was 150 pF. These values were measured on the prototype using an impedance analyzer, and were verified by calculation and Q3D simulation. The parasitic capacitance \( C_{\text{F2}} \) is less than \( C_{\text{D2}} \) because the middle and bottom metal layers contribute a small portion of the footprint.

For the tests, a high-frequency current transformer (HFCT) was used to measure the current of the line impedance stabilization network (LISN). The output of the HFCT was connected to an EMC analyzer. The measured current input cases are shown in Fig. 4. The first case has a single substrate and no decoupling capacitors. The second case has two stacked substrates and no decoupling capacitors. The third case has two stacked substrates and two 680-pF decoupling capacitors in parallel and two in series, but the middle layer of the substrate stack is left floating. The fourth case is similar to the third, but has two series 10-nF capacitors. The fifth case connects the middle metal layer of the substrate stack to the midpoint of the series decoupling capacitors.

When two substrates are stacked together (case 2), the high-frequency noise decreases by just a few dB compared to case 1 with a single substrate. This indicates that the reduction in the parasitic capacitance offered by the second substrate is not sufficient to lower the CM noise. The addition of 680-pF decoupling capacitors in case 3, on the other hand, reduces the high-frequency noise by more than 10 dB compared to case 2 with a single substrate. The decoupling capacitors also cause the resonant frequency to decrease. When the decoupling capacitance is increased to 10 nF (case 4), then the resonant frequency further decreases, and the high-frequency noise is reduced by a few more dB. This is in agreement with [50], which shows that increasing the decoupling capacitance further reduces the high-frequency impedance of the screen.

When the middle metal of the substrate stack is connected to the midpoint of the two series 10-nF capacitors (case 5), the high-frequency noise decreases by more than 15 dB; the larger frequency range. This is because there is now a pure inductance, high-frequency path for the generated CM noise to flow. This preliminary testing demonstrates the potential of the screen to reduce the CM noise.

The gate-source and drain-source voltages and drain of the 1.2 kV SiC MOSFET were also monitored during testing. By adding decoupling capacitors, the frequency in the drain-source voltage reduced, and the overshoot and amplitude ringing was decreased, resulting in greater current overshoot and amplitude ringing. This ringing and overshoot can be reduced by decreasing the parasitic inductance, which was optimized in this module prototype. Connecting the metal layer to the decoupling capacitor midpoint did not cause noticeable changes in the MOSFET voltage and waveforms. Therefore, if the parasitic inductances and...
decoupling capacitors are carefully designed, the proposed CM screen will have minimal impact on the MOSFET losses.

C. Implementation

To achieve a low-impedance implementation for the CM screen in the 10 kV power module, it is proposed to embed capacitors, and to use vias within the insulating ceramic substrates to make the connection between the middle metal layer and the capacitor potentials. In [50], the capacitors are placed above the semiconductor devices, creating a vertical high-frequency power loop that does not increase the module footprint, as it takes advantage of the third dimension. In this work, this vertical-capacitor-loop concept was adopted with some modifications. Each 10 kV SiC MOSFET switch pair has its own set of decoupling capacitors located above it (Fig. 1(c)), resulting in a symmetric power loop inductance of just 4.4 nH for each. In this embodiment, two capacitors are placed in series, and the midpoint, which is at half of the dc bus voltage, is connected to the middle metal of the substrate stack. By connecting the screen to the decoupling capacitors within the power module, the influence of the parasitic impedances external to the package are diminished thereby improving the effectiveness of the screen.

According to ANSYS Q3D simulations, this connection method has less than 2 nH parasitic inductance, allowing for a high proportion of the CM current to be diverted to the dc bus and contained within the power module. Additionally, the S1D2 pad area was designed as small as possible to minimize $C_{PD}$. For the proposed high-voltage 10 kV power module shown in Fig. 1 and Fig. 2(b), $C_{PD}$ is 46 pF, and $C_{PE}$ is 160 pF, according to ANSYS Q3D simulations. For the decoupling capacitors ($C_{PD}$), a surface-mount, 680 pF, COG, 5 kV multilayer ceramic capacitor was selected. As shown in Fig. 1(c), there are three capacitors in parallel—one above each MOSFET switch pair—giving an equivalent capacitance of 2.04 nF.

V. ELECTRIC FIELD REDUCTION

To address the enhanced electric field associated with high-voltage, high-density package, the ceramic substrate must be thoughtfully designed and evaluated. In power modules, the electric field concentrates at the intersection of the ceramic, metal, and encapsulation. In [52],[53],[54],[55], the electric field is known as the triple point. If this electric field exceeds the breakdown field strength of the insulation materials, then PD can occur. Repetitive PD events can ultimately result in insulation failure, such as cracking of the ceramic substrate as shown in [37], destroying the power module.

In the literature, it has been shown that the PDIV of a standard 1-mm-thick aluminum nitride (AlN) DBC substrate is less than 10 kV rms [37], and can be as low as 5 kV [56]. This does not provide sufficient margin for 10 kV MOSFETs. Accordingly, methods for reducing the electric field within the power module need to be explored. There have been several proposed solutions to reduce the electric field strength at the triple point, including: increasing the ceramic thickness [37]; varying the metal pad size [38]; and metal-ceramic interface geometry [39],[40],[41], and stacking multiple substrates [42]. None of these previously proposed solutions were implemented in an actual power module, and several of them complicate the module manufacturing. The method proposed in this work, is an adaptation of the latter method, which effectively increases the PDIV, and is simple to implement.

In [56], it was shown that stacking DBC substrates reduces the electric field strength within the bulk ceramic at the critical triple points. The PD tests revealed that the PDIV could be increased by 94 % by stacking two 0.32 mm-thick aluminum nitride (AlN) DBC substrates compared to having a single 0.63 mm-thick AlN substrate [56]. However, the practical implementation of this method was not explored. In a power module, the top and bottom metal layers are not symmetrical; the top metal is patterned to create the circuit (e.g., half bridge), and various traces are at different potentials during the operation. As a result, it is not clear what potential should be applied to the middle metal layer to achieve a meaningful reduction in the electric field strength. This key factor of the proposed CM screen. In this work, a 1.2 kV-SiC-based boost converter was used to show the effectiveness of the screen.

Fig. 4 shows the simulated 2D electric field distribution for the case when the top metal is patterned and has different potentials. One of the potentials represents that of the high-side switch, and the other represents the dc bus potential when the low-side switch is conducting. The former is consistently at the positive and negative dc bus potentials. The worst-case scenario occurs when the low-side switch is conducting and its drain is negative dc bus potential. This worst-case scenario is simulated when the low-side switch is conducting and its drain is negative dc bus potential. The positive dc bus is set to 10 kV, and the negative is set to 0 V. The bottom-most metal is at the same potential as the power system, which is grounded (0 V).
distribution is non-uniform within the bulk of the ceramic, and that the peak electric field occurs at the triple points. The peak electric field exceeds 20 kV/mm, which is the typical breakdown field strength for ceramic substrates.

Fig. 5(b) shows the simulated electric field plot for two stacked DBA substrates with the middle metal layer connected to the negative dc bus (0 V), as proposed in [33] and [34]. Comparing Fig. 5(a) and Fig. 5(b), it can be seen that connecting the middle metal to the negative dc bus does not reduce the peak electric field at the triple point, nor does it improve the distribution within the bulk ceramic, compared to the single substrate case. This is because the bottom substrate has 0 V across it, while the top substrate has 10 kV. In this implementation, the bottom substrate is not helping to support the voltage, and is therefore not being fully utilized.

If the middle metal is connected to the positive dc bus, as proposed in [33], then the triple points at which the peak electric field occur will change, and the electric field distribution within the bulk ceramic will shift. This is shown in Fig. 5(c). Although the distribution and critical triple points have changed, the peak electric field, and therefore the PDIV, are similar to the case with a single substrate. This is because both the top and bottom substrates have 10 kV across them.

If instead the middle metal is connected to half of the applied voltage, then both the top and bottom substrates have a potential of 5 kV across them. The simulated electric field distribution for this case is shown in Fig. 5(d). The simulated peak electric field is reduced by 58 % compared to the single-substrate case (Fig. 5(a)), and the electric field in the bulk ceramic is uniformly distributed in the two substrates. Therefore, in this work, the middle metal layer of the DBA stack is connected to half of the bus voltage.

The connection of the middle metal layer to half of the bus potential can be realized with the embedded decoupling capacitors. Each set of decoupling capacitors shown in Fig. 1(c) consists of two, 5 kV ceramic capacitors placed in series. From Fig. 1(d), it can be seen that the midpoint of the capacitors is connected to the middle metal layer of the bottom DBA stack through vias and metal posts. This connection allows the middle metal layer to be connected to half of the bus voltage, thus reducing the peak electric field in the power module.

VI. EXPERIMENTAL RESULTS

A. Switching Testing

To evaluate the switching performance of the proposed 10 kV power module, double-pulse tests (DPT) were performed on the low-current prototype shown in Fig. 2(a). The DPT schematic and setup are shown in Fig. 6. The gate driver used for the DPTs was adapted from the one presented in [60]. The low-side 10 kV SiC MOSFET was driven from +20 V in the on-state to -5 V in the off-state. The body diode of the high-side 10 kV SiC MOSFET was used as the free-wheeling...
diode. The gate driver PCB is mounted on top of the power module to achieve small gate-loop inductance between the driver and the module.

The gate-source and drain-source voltages of the low-side SiC MOSFET were monitored using a 300 V passive probe with a bandwidth of 1 GHz, and a 20 kV passive probe with a bandwidth of 75 MHz, respectively. As shown in Fig. 6(c), these probes are placed directly above the MOSFET terminals to minimize the parasitic inductance in the measurement loop. Due to the embedded decoupling capacitors, the drain current of the SiC MOSFETs could not be measured. A 15 kV power supply was used to charge the external decoupling capacitors. Each capacitor is 0.82 µF and rated at 3.3 kV (MP80CV824K [61]). Six total capacitors were used—two in series and three in parallel for a total capacitance of 1.2 µF and voltage rating of 6.6 kV. Three capacitors were put in parallel to increase the capacitance and to reduce the inductance; each capacitor has an equivalent series inductance of 30 nH [61].

Fig. 7 shows the gate-source and drain-source voltage waveforms for the turn-on and turn-off transitions for the DPTs performed on the module shown in Fig. 2(a). The switching tests were performed up to 5 kV and 20 A with turn-on and turn-off gate resistances of 0.33 Ω and 0.17 Ω, respectively. Table I lists the measured overshoot, undershoot, rise and fall times, and switching rates from the DPTs. During the turn-on transient, the fall time of the drain-source voltage is 16 ns, giving a dV/dt of 250 V/ns. At turn-off, the voltage rise time is 50 ns, which is a dV/dt of 80 V/ns. The voltage rise time is longer because it is controlled by the output capacitance and load current. Negligible voltage overshoot and ringing were measured, indicating low power- and gate-loop inductances. This is due to the low-inductance module design, as well as careful layout and connection of the gate driver, bus bar, external decoupling capacitors, and measurement probes.

To the best of the author’s knowledge, these are the fastest switching speeds reported for similarly-rated SiC MOSFETs and IGBTs. In fact, this is more than two times faster than those reported in [24],[32],[62],[63]. In [32], switching results for a module populated with a single die had turn-on and turn-off transition times of approximately 80 ns and 120 ns, respectively, giving switching speeds of 88 V/ns and 58 V/ns at a bus voltage of 7 kV, drain current of 15 A, and gate resistance of 21 Ω. The switching waveforms also showed a moderate voltage overshoot of approximately 300 V (4.3 %) [32].

For a discrete 4 kV silicon IGBT, the datasheet reports voltage rise and fall times of 146 ns and 514 ns at 1.25 kV, 30 A, and 2 Ω external gate resistance [64]. These switching times result in dV/dt values of 8.6 V/ns and 2.4 V/ns for the rise and fall, respectively, which are 10 and 100 times slower than the switching speeds achieved in this work. Accordingly, the proposed power module can enable faster-switching, higher-voltage power converters while maintaining high efficiency.

### Table I

| Parameter     | Gate-Source Voltage | Drain-Source Voltage |
|---------------|---------------------|----------------------|
| Overshoot     | None                | None                 |
| Undershoot    | None                | None                 |
| Rise Time     | 24 ns               | 50 ns                |
| Fall Time     | 26 ns               | 16 ns                |
| Rise dV/dt    | 0.9 V/ns            | 80 V/ns              |
| Fall dV/dt    | 0.8 V/ns            | 250 V/ns             |

### B. Common-Mode Screen Testing

To evaluate the effectiveness of the integrated CM screen on the 10 kV power module, switching tests were performed. As mentioned earlier, the CM current increases as the dV/dt and parasitic capacitances increase. To improve the signal-to-noise ratio of the CM current measurement, the dV/dt was reduced. This was achieved by lowering the bus voltage to 2 kV. To ensure sufficient CM current could be measured, the larger power module with three 10 kV SiC MOSFET dies in parallel per switch position was used (Fig. 2(b)) [65]. The C<sub>P1</sub> and C<sub>P2</sub> of this 10 kV prototype are 47 pF and 162 pF, respectively.

Fig. 8(a) shows the schematic of the tests when the CM screen is not connected (the middle metal layer of the substrate stack is floating). Fig. 8(b) shows the schematic of the tests when the CM screen is connected to the capacitor midpoint. An inductor with high-voltage wire for the winding was connected across the high-side switch of the half-bridge module. The body diode of the high-side SiC MOSFET was used to freewheel the current in the inductor when the high-side switch was off.

To validate the performance of the CM screen, the current through the ground path, I<sub>gnd</sub>, was measured, as shown in the figure.
PD tests were performed on a patterned, 1-mm-thick DBA substrate. The spacing between metal traces and the metal traces to the edge of the ceramic was 2 mm. Three cases were tested: 1) a single substrate, 2) two substrates with the middle metal connected to the ground, and 3) two stacked substrates with the middle metal connected to the source or ground. Each case was tested under two conditions: 1) S1D2 = D1 (the high-side switch is conducting and the low-side switch is blocking), and 2) S1D2 = S2 (the high-side switch is blocking and the low-side switch is conducting).

First, the PD tests were performed with the samples to have a high signal-to-noise ratio. These tests revealed that, as shown in the electrostatic simulations, the PD from DBA substrates will occur at the triple points. Specifically, PD will take place along the edge of the metal pad where the high potential is applied. The resulting PDIV for the cases when the samples are tested in air are listed in Table II. When S1D2 is equal to D1 (the applied voltage) and the middle metal is connected to the source, then there is 7.4 kV rms (10.5 kV peak). For this same case, breakdown occurred at 8.5 kV rms (12.0 kV peak). This means that the measured PDIV is lower than the previous switching tests because of the higher bus voltage and larger device capacitance due to the three MOSFET dies in parallel. The measured peak current through the ground path without the screen is 2 A. This peak current will increase as the dc bus voltage, and therefore the dv/dt, increases. With the CM screen connected, the measured peak current through the ground path is reduced to 0.2 A. This is an order of magnitude reduction.

Since the power module will be encapsulated, PD tests were also performed on a stacked substrate sample that was encapsulated with SilGel 612 from Wacker. For this case, the S1D2 potential was connected to S2 (the worst case) when the samples are tested in air. The measured PDIVs for this sample are listed in Table II. When the middle metal is connected to the source ground, the PDIV is 7.4 kV rms (10.5 kV peak). This means that the PDIV is lower than the previous switching tests because of the higher bus voltage and the voltage rating of the 10 kV SiC MOSFETs. When the middle metal is connected to half of the applied voltage, no PD could be measured up to 10.5 kV rms (14.8 kV peak). The testing was stopped at 10.5 kV rms due to the reduced signal-to-noise ratio. This suggests that encapsulated substrates with the middle metal connected to half of the applied voltage will have more than a 40 % higher PDIV than the SiC MOSFETs.

### Table II

Partial Discharge Testing Summary

| Sample               | Voltage of Middle Metal | Surrounding Medium | S1D2 Potential | PDIV (rms) |
|----------------------|-------------------------|--------------------|----------------|------------|
| Single Substrate     | N/A                     | Air                | D1             | 1.7 kV     |
| Stacked Substrates   | 1/2 × Vac               | Air                | D1             | 2.6 kV     |
| Encapsulated Stacked Substrates | 0 V                   | SilGel 612        | S2             | >10.5 kV   |
|                      | 1/2 × Vac               | SilGel 612        | S2             | >10.5 kV   |

**C. Partial Discharge Testing**

PD tests were conducted to validate the electrostatic simulation results. The PD tests were performed using a 50 kV, 100-mA, 60-Hz power supply as the excitation source. To detect the PD events, a Doble PD Smart with HFCT-300 sensor was used [66]. The Doble PD Smart complies with IEC 60270 and VDE 0434, among other standards [66]. PD signals at frequencies from 35 kHz to 20 MHz and an apparent charge as low as 0.2 pC can be measured [66].
This work proposed a high-density power module for 10 kV SiC MOSFETs with reduced CM current and electric field strength. The optimal layout and system interface enable the module to switch 5 kV in tens of nanoseconds with negligible ringing and voltage overshoot. This is the fastest switching speed reported to date for 10 kV SiC MOSFETs. To reduce the adverse EMI effects of this high-speed switching, a CM screen was incorporated into the power module design. This screen was realized by stacking two DBA substrates and connecting the middle metal to the midpoint of embedded decoupling capacitors through vias and metal posts. This proposed method creates a low-impedance path at high frequency, and contains the current that would normally flow to the system ground within the power module. With this screen, the measured CM current leaving the power module decreases by ten times. This proposed integrated screen will reduce the need for filtering at the system level, thereby increasing the power density, lowering the cost, and simplifying the design of power electronic systems. Moreover, it will permit the operation of the 10 kV SiC MOSFETs at faster speeds, thereby reducing losses and increasing efficiency.

This screen also increases the voltage rating of the power module. PD tests showed that stacking two substrates and connecting the middle metal to half of the applied voltage increases the PDIV by 53 % compared to a single substrate. When testing two encapsulated stacked substrates with the middle metal connected to the source ground, breakdown occurred at 8.5 kV rms (12.0 kV peak). This breakdown voltage limits the voltage rating of the package. When the middle metal of the encapsulated substrates is connected to half of the applied voltage, the PDIV exceeds 10.5 kV rms. This method for reducing the electric field is effective and simple to implement, and will enable high-voltage packages with greater power density.

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