Prevention of the current transformer saturation by using negative resistance

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Abstract
In the power grid, various conditions may occur that saturate the core of a current transformer. Saturation of the protection core of the current transformers can cause a malfunction in the protection relays. To prevent malfunction of the protection relays caused by the current transformer saturation, software and hardware methods can be used. In the software method changes in the protection relay algorithm are used. In the hardware method special devices are used. A new hardware method is presented here, which uses compensation to prevent the occurrence of current transformer saturation. In the proposed method, compensation is done by controlling an applied voltage to the current transformer secondary terminals using negative resistance. The proposed method, despite its simplicity and cost-effectiveness, has good performance in preventing saturation in various conditions. The high reliability in terms of the risk of secondary open circuit and its application in various saturation conditions, even in the case of severe saturation are the main advantages of the proposed method. Also, the proposed method does not produce distortion in the transformation of high-order harmonics by the current transformer. To verify the effectiveness of the proposed method, prototype design and construction have been performed. The simulation and experimental results of laboratory tests have been presented and analysed.

1  |  INTRODUCTION

The current transformer (CT) in the power grid is used for measuring the current flow and comprises two measuring and protection magnetic cores [1, 2]. In a high-voltage grid, CTS may have several cores of measurement type and several cores of protective type [3]. The measurement core sends the current samples to the measuring equipment such as counters, meters, and transducers. The protection core sends the current samples to the protection relays and event/fault recorder [4]. Some conditions such as over-current, high current fault with decaying DC, inrush current etc. may occur in the power grid, and cause one or both protection and measurement cores to be saturated [5, 6]. Saturation of the CT protection core can cause malfunction of the protection relays [7, 8]. Two types of solutions have been proposed to prevent this problem. The first type of solutions which are called software solutions are based on modifying the protective relay control algorithms. In software solutions, when saturation occurs in the CT protection core, the protection relays can detect it and block some of the relay functions that may cause malfunctioning. This method can only be implemented when the special types of digital relays are used for protection purposes. The software solutions are easy to implement due to the lack of need for circuitry changes [7, 9, 10].

The second type of solutions which are called hardware solutions are based on compensation or demagnetisation of the CT cores. In these methods, a suitable device must be added to the CT secondary circuit to prevent the CT cores from saturation. The hardware solutions increase the risk of the secondary open circuit because of adding a device in series to the CT secondary circuit. Unlike software solutions that only detect saturation, hardware solutions prevent the CT cores from saturation. Implementing the hardware solutions does not need any special digital protection relays [6, 11, 12]. Some of the hardware solutions use demagnetisation methods to mitigate the residual flux. These methods operate when the CT primary circuit is open and...
can be used in the auto-reclosing scheme or after the CT testing procedure [13, 14]. Some other hardware solutions use compensation methods to prevent saturation when a high current flows through the CT primary. These methods can be used in the case of over-current in the CT primary or presence of decaying DC component [12, 15].

The compensation methods operate by controlling the voltage of the CT secondary terminal [13]. In these methods, the voltage of the secondary terminal is controlled in such a way that the voltage drop caused by the CT burden on the secondary terminals can be reduced by using a suitable compensator as shown in Figure 1.

According to the voltage polarity shown in Figure 1, the CT secondary voltage can be obtained by (1) and the CT flux will be in the form of (2)

\[ V_{t,sec} = V_{burden} + V_{comp} \]  
\[ \emptyset = \frac{1}{N_{sec}} \int V_{t,sec} \, dt + \emptyset_0 \]  

where \( \emptyset_0 \) is the remnant flux, \( V_{t,sec} \) is the secondary terminal voltage, \( V_{burden} \) is the CT burden voltage drop, \( V_{comp} \) is the voltage applied for compensating, and \( N_{sec} \) is the turn number of the secondary CT winding. Substituting (1) into (2), (3) is obtained

\[ \emptyset = \frac{1}{N_{t,exc}} \int V_{burden} \, dt + \frac{1}{N_{sec}} \int V_{comp} \, dt + \emptyset_0 \]  

According to (3), if the \( V_{comp} \) is properly controlled, the CT core flux can be controlled so that the core is not saturated. However, it should be noted that \( V_{comp} \) is controlled and modified in such a way that it does not cause harmonic distortion in the secondary current and does not cause problems in transforming high-order harmonics in CT [16, 17]. In the existing compensation methods, \( V_{comp} \) is produced in three ways: (A) using negative voltage feedback, (B) using switching resistance, or (C) using controlled voltage source.

In method A, the negative voltage is obtained from a compensator transformer which is located on the secondary side of CT and acts as the negative feedback to oppose the CT excitation voltage. Using method A is simple and highly reliable, but due to the creation of a parallel path in the secondary circuit, an error in the measured current is made if the burden changes [18]. So any change in the CT burden makes this method useless. In method B, a switched resistor is placed in series in the secondary circuit. The value of this resistor changes in part of a current cycle. In this method, the performance is high, but the complexity of the control algorithm and the existence of switching devices increase the failure possibility and reduce reliability [12, 17]. In method C, a controlled voltage source is used in the secondary circuit which controls the CT secondary terminal voltage. Method C, like method B, is highly accurate and can be used in severe saturation, but in addition to the disadvantages of method B, it interferes with the transformation of high-order harmonics [15].

In this research, a compensation method for controlling the voltage of the CT secondary terminal is proposed. This method is based on the negative resistance technique and without the need for controllers and switching devices. The use of this technique to compensate the CT saturation is unprecedented. The proposed method removes the mentioned limitations of previous compensation methods. The high reliability in terms of the risk of secondary open circuit and its application in various saturation conditions, even in the case of severe saturation are the main advantages of the proposed method. This method also does not distort the measurement of high-order harmonics because of the lack of switching devices. Applying the proposed method reduces the total burden on the CT secondary. As a result, the total voltage drop on the CT secondary terminal decreases. The proposed compensator does not use processor and made with passive devices and simple integrated circuit (IC). So, the circuit topology in this method is reliable due to the circuitry simplicity. The high voltage CT price and financial loss caused by the outage and caused by undistributed energy that may occur due to the CT saturation is very high CT saturation. The cost of the proposed compensator and its installation is negligible compared to them.

The rest of this paper is presented in four sections. Section 2 contains the principles of the proposed compensation method using negative resistance. Section 3 includes the results of the simulations performed and their analysis. Section 4 includes the details of the design and construction of the prototype. Also, the experimental results of the proposed method are presented in this section, and Section 5 includes the conclusion.

## 2  |  PRINCIPLE OF THE NEGATIVE RESISTANCE COMPENSATION

In the negative resistance compensation principle, which the proposed method here, is based on this principle, the total burden of the CT secondary circuit is reduced by adding a negative resistance. Reducing the resistance in the secondary circuit reduces the voltage drop across the CT secondary terminal. According to (3), this decrease in voltage will reduce the flux in the core and prevent saturation. The circuit topology proposed in this research to implement this method is shown in Figure 2.

The section specified with the dashed line in Figure 2 shows the proposed circuit topology to create negative resistance in the CT secondary circuit. This topology uses a power amplifier.
and an auxiliary transformer. As can be seen in Figure 2, the proposed set is placed in series in the CT secondary circuit.

According to Figure 3, by analysing the circuit topology, (4)–(6) are obtained [19]

\[ R'_{\text{in}} = -\frac{R_1 R_3}{R_2} \]  
\[ V_{\text{nr}} = -I'_{\text{sec}} \frac{R_1 R_3}{R_2} \left( \frac{n_1}{n_2} \right)^2 \]  
\[ I_0 = -I'_{\text{sec}} \frac{R_2 + R_3}{R_2} \left( \frac{n_1}{n_2} \right). \]

The values of resistors \( R_1, R_2, \) and \( R_3 \) in (4)–(6) are determined in the design procedure. The \( R'_{\text{in}} \) resistor has a negative value, dependent on \( R_1 \) to \( R_3 \). The negative resistance shown in Figure 3 is acting as a negative load which injects energy into circuit in contrast to an ordinary load that consumes energy from it. This is achieved by controlling the voltage \( V_{\text{nr}} \) according to current \( I'_{\text{sec}} \) as shown in Figure 3 and (5). In the proposed circuit topology, in addition to the negative resistance unit shown in Figure 3, an Aux. Trans. is also used. This transformer is used for two purposes: (A) reducing the output current of the power amplifier \( I_0 \) and (B) preventing the secondary path opening circuit if any of the circuit elements fail. Therefore, by considering the Aux. Trans. in the proposed topology, (7)–(9) are obtained:

\[ R_{\text{in}} = -\frac{R_1 R_3}{R_2} \left( \frac{n_1}{n_2} \right)^2 + Z_{\text{aux}} \]  
\[ V_{\text{amp}} = -I_{\text{sec}} \frac{R_1 R_3}{R_2} \left( \frac{n_1}{n_2} \right)^2 \]  
\[ I_0 = -I_{\text{sec}} \frac{R_2 + R_3}{R_2} \left( \frac{n_1}{n_2} \right). \]

In (7)–(9), \( I_{\text{sec}} \) is the CT secondary current, \( n_1 \) and \( n_2 \) are the turn numbers of primary and secondary windings of the Aux. Trans., \( V_{\text{amp}} \) is the compensation voltage, and \( Z_{\text{aux}} \) is the impedance of the Aux. Trans. which in comparison with \( R'_{\text{in}} \) is negligible. The Aux. Trans. must have the magnetic core without air gaps. So, if any of the circuit elements on the secondary side of the Aux. Trans. fail and consequently \( I_{\text{sec}} \) drop to zero, the magnetic core will be saturated and as a result, the secondary current, \( I_{\text{sec}} \), will not be zero and the CT secondary circuit will not open [20]. The material and dimensions of the core and the primary and secondary winding turn numbers should be selected according to (10) and (11) so that \( Z_{\text{aux}} \) is very low and negligible at all frequencies:

\[ Z_{\text{aux}} \approx R_{\text{winding}} + jL\omega \]  
\[ L = \frac{n_1^2 A \mu_0 \mu_r}{I}. \]

3 | SIMULATION OF NEGATIVE RESISTANCE COMPENSATION METHOD

To evaluate the efficacy of the proposed method, two different cases have been simulated using Comsol and Matlab software. In Comsol, the magnetic behaviour of a steel-cobalt 2VP core, commonly used as the CT core, was simulated. So, magne-
TABLE 1 Circuitry parameter for the proposed topology

| Circuitry parameter | Value  | Circuitry parameter | Value  |
|---------------------|--------|---------------------|--------|
| \( R_1 \)           | 50 \( \Omega \) | \( I \)             | \( 7 \times 10^{-2} \text{ m} \) |
| \( R_2 \)           | 1 \( \Omega \)  | \( A \)             | \( 5 \times 10^{-1} \text{ m}^2 \) |
| \( R_3 \)           | 2 \( \Omega \)  | \( R_{\text{sec/og}} \) | 0.2 \( \Omega \) |
| \( \mu_1 \)         | 10      | \( \mu_r \)        | 19,000 |
| \( \mu_2 \)         | 50      | Power amplifier     | maximum output |
|                     |         | current             | 10 A    |

CT, current transformer.

TABLE 2 Parameters of the CT and network in the simulation

| Network parameter | Value  | CT parameter | Value  |
|-------------------|--------|--------------|--------|
| Nominal voltage   | 20 kV  | \( I_n \)    | 1 A    |
| Nominal current   | 300 A  | \( I_{p_r} \) | \( 300 \Omega \) |
| Frequency         | 50 Hz  | Burden (rated) | 10 VA |
| \( R_{\text{Network}} \) | 0.4 \( \Omega \) | Burden | 10 \( \Omega \) |
| \( X_{\text{Network}} \) | 10.15 \( \Omega \) | \( R_{\text{CT}} \) | 0.5 \( \Omega \) |
| Sample time       | \( 5 \times 10^{-5} \) | CT core material | Steel-cobalt 2VP |
| Short circuit current | 8 PU  | Network time constant | 85 ms |
| CT core cross-sectional area | 0.07 m \( \times 0.04 \) m | CT primary/secondary turn number | 2/600 |

EXPERIMENTAL RESULTS

In this test, due to the flow of pure sinusoidal current with large amplitude in the CT primary, the core saturates and the effect

power of the power amplifier is limited in practice. It is observed that \( I_o \) does not exceed 4.2 A according to Figure 4(c).

In the second case, the simulation was performed in the presence of a decaying DC value. The simulation parameters of the CT are as shown in Table 2. In this case, the amplitudes of the sinusoidal current and the decaying DC current injected into the CT primary are 5 per unit and 3 per unit, respectively. Considering \( L/R \) ratio in the CT primary circuit, the decaying DC time constant is 85 ms. The simulation results are shown in Figure 5. In Figure 5(a), the CT secondary current are compared for the two modes, without compensation and with compensation by the proposed method. It can be seen that in the case of uncompensated, the secondary current will be distorted from 27 ms onwards. But if compensation is done in the proposed way, the secondary current waveform will not be distorted. According to Figure 5(b), in the case of uncompensated, the core will be saturated in some of the time intervals, but if the compensation is done, the flux will not be saturated. Figure 5(c) shows the output current of the power amplifier (\( I_o \)).

To verify the reliability of the proposed method in terms of the secondary opening circuit, a condition has been simulated in which the current of the secondary side of the Aux. Trans. \( I_{sec} \) is brought to zero during normal CT operation at rated current.

Figure 6 shows the simulation results for the case of an open circuit on the secondary side of the Aux. Trans. which may occur due to circuit elements failure in the proposed topology. According to Figure 6(a) and (b), if the Aux. Trans. secondary current drop to zero, the core of the Aux. Trans. will saturate. Its magnetic reluctance will increase and the Aux. Trans. inductance seen from the CT secondary circuit will decrease to a negligible value. So, the CT secondary circuit will not open. But in this situation, the CT secondary will be distorted in both positive and negative half-cycles, as shown in Figure 6(a).

4 | EXPERIMENTAL RESULTS

To verify the effectiveness of the proposed compensation method in practical conditions, a prototype device was designed and constructed. The elements of this device and the results of the laboratory tests are presented in this section.

Figure 7 shows the prototype schematic diagram. In this prototype device, a module including a power amplifier for building the negative resistor, an auxiliary transformer, current and voltage sensors to sample the test results, and a storage module are used to capture and store the test results.

Laboratory tests were performed on a 20 kV CT. Table 3 shows the specifications of the CT under test. To examine the operation of the proposed method in preventing CT saturation, tests were performed in two cases: (A) pure sinusoidal high current and (B) current with decaying DC component.

4.1 | Pure sinusoidal high current

In this test, due to the flow of pure sinusoidal current with large amplitude in the CT primary, the core saturates and the effect
To perform this test, a current has been injected to the CT primary by the PRP-2000 device and its extension module. To increase the current on the primary side of the CT, the current injection cable has been twisted in five rings. In this way, the primary CT current will increase five times. The test was performed for two cases. In the first case, no compensation was applied, and in the second case, the prototype compensation method was placed in the secondary circuit to prevent saturation. The results of these tests are shown comparatively in Figure 9.

At first, pure sinusoidal current of 800 A root mean square (RMS) is injected into the primary cable by the current injection device. So the primary current of the CT is 4000 A (RMS) or 8 per unit. Figure 9(a) and (b) shows the primary and secondary currents for uncompensated mode and compensated with the proposed method, respectively. It can be seen that in the case of uncompensated, the core is saturated twice in each cycle, and as a result, the secondary current is distorted, but in the case of compensated, saturation does not occur. Figure 9(c) shows the output current of the power amplifier compared to the secondary current. This current is less than 5 A during the test.

4.2 Current with decaying DC component

To perform this test, the CPC-100 device [14] is used to inject current into the CT primary. A sinusoidal current of 2500 A (RMS), equivalent to 5 per unit, and a decaying DC component of 1500 A amplitude, equivalent to 3 per unit are injected into the CT primary. The time constant is 100 ms. The laboratory set-up for this test is shown in Figures 10 and 11.

The test was also performed for two cases. In the first case, no compensation is applied, and in the second case, the prototype compensation device is placed in the secondary circuit to prevent saturation. The results of this test are shown comparatively in Figure 11.
**FIGURE 5** Simulation results for high amplitude with decaying DC primary current: (a) CT secondary current, (b) core flux density, and (c) power amplifier output current

**FIGURE 6** Simulation results for secondary open circuit: (a) CT secondary and Aux. Trans. current and (b) core flux density
Table 3: Specification of the tested CT

| Parameter          | Value | Parameter          | Value |
|--------------------|-------|--------------------|-------|
| Burden             | 10 VA | Frequency          | 50 Hz |
| $I_{in}$           | 1 A   | $I_{ph}$           | 500 A |
| Class              | 10P   | $I_{ph}$           | 7 kA  |
| Insulation withstand | 3 kV  | R75                | 2 Ω   |
| Accuracy limit factor (ALF) | 5     | Weight             | 15 kg |

CT, current transformer.

Figure 11(a) shows the injected currents. Figure 11(b) compares the CT secondary current for the two modes, with and without compensation. It can be seen that without compensation, the core is saturated from 30 ms onwards and the secondary current is distorted. But with compensation using the proposed method, the secondary current will not distort.

Figure 11(c) shows the output current of the power amplifier and can be compared with the CT secondary current. This current is less than 5 A during the test, and its maximum occurs at the start time before the DC value starts decaying.

Measurement of high-frequency currents by CT is very important for the performance of some protection relays. For example, some protection relays use the second- and fifth-order harmonics to detect inrush current and over-flux, respectively. Therefore, it is important that CT properly transforms these harmonics. In these cases, it is important that the equipment that are placed into the CT secondary side, including saturation compensator, do not cause distortion. To investigate harmonic distortion for the proposed compensator, a harmonic study is performed and the results are shown in Table 4. The results presented in this table are extracted from the eighth cycle of test results shown in Figure 11(b). According to Table 4, the harmonic distortion in the secondary current for all frequencies is less than 1% which is acceptable.
FIGURE 8 Laboratory test set-up for high current saturation condition.

FIGURE 9 Experimental results for pure sinusoidal high amplitude primary current: (a) currents for uncompensated mode, (b) currents for compensated mode, and (c) power amplifier output current.
**FIGURE 10**  Laboratory test set-up for DC saturation condition

**FIGURE 11**  Experimental results for current with decaying DC in the primary: (A) primary currents, (b) secondary currents, and (c) power amplifier output current
| Frequency            | Amplitude Uncompensated current (%) | Amplitude Compensated current (%) | Error (%) |
|----------------------|-------------------------------------|-----------------------------------|-----------|
| 0 Hz (DC)            | 5.1                                 | 5                                 | 0.1       |
| 50 Hz (fundamental)  | 100                                 | 100                               | 0         |
| 100 Hz (2nd harmonic)| 3.8                                 | 4.1                               | 0.3       |
| 150 Hz (3rd harmonic)| 2.5                                 | 2.7                               | 0.2       |
| 200 Hz (4th harmonic)| 1.2                                 | 1.4                               | 0.2       |
| 250 Hz (5th harmonic)| 1.1                                 | 1.4                               | 0.3       |

5 | CONCLUSION

In this research, a hardware method was proposed which compensates the CT saturation by controlling the voltage of the secondary CT terminal by using a negative resistance, which is made by a power amplifier and an auxiliary transformer.

To evaluate the performance of the proposed method, simulation results, and practical results are presented here. The advantages of the proposed method include usability in high current and DC current conditions, high reliability, simple structure, and lack of harmonic distortion.

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REFERENCES

1. Bélecivc, N.M., Stojanovic, Z.N.: Algorithm for phasor estimation during current transformer saturation and/or DC component presence: definition and application in arc detection on overhead lines. IET Gener. Transm. Distrib. 14(7), 1378–1388 (2020)
2. IEC standard: Instrument transformers part 2: additional requirements for current transformers. IEC 61869-2:2012. European Committee for Standards, Brussels (2012)
3. IEEE standard: Guide for protective relay applications to transmission lines. C37.113-2015. IEEE, Piscataway, NJ (2016)
4. Ziegler, G.: Numerical Protection, Principles and Applications. Publicis Corporation Publishing, Erlangen (2005)

5. Blackburn, J., Domin, T.J.: Protective Relay Principals and Applications, 3rd ed. Taylor and Francis Group, New York (2007)
6. Aji, E.B., et al.: Compensation of the current-transformer saturation effects for digital relays. IEEE Trans. Power Delivery. 26, 2531–2540 (2011)
7. Abdoos, A.A.: Detection of current transformer saturation based on variational mode decomposition analysis. IET Gener. Transm. Distrib. 11(10), 2658–2669 (2016)
8. IEEE Standard: Guide for the Application of Current Transformers Used for Protective Relaying Purposes. C37-110. IEEE, Piscataway, NJ (1996)
9. Medeiros, R.P., Costa, F.B.: A wavelet-based transformer differential protection with differential current transformer saturation and cross-country fault detection. IEEE Trans. Power Delivery 33(2), 789–799 (2018)
10. Naseri, F., et al.: Fast discrimination of transformer magnetizing current from internal faults: an extended Kalman filter-based approach. IEEE Trans. Power Delivery 33(1), 110–119 (2018)
11. Davarpanah, M., et al.: Performance enhancement of the transformer restricted earth fault relay. IEEE Trans. Power Delivery 28, 467–474 (2013)
12. Davarpanah, M., et al.: A saturation suppression approach for the current transformer – part I: Fundamental concepts and design. IEEE Trans. Power Delivery 28(2), 1928–1935 (2013)
13. Haitipour, E., et al.: Residual flux mitigation of protective current transformers used in an auto-reclosing scheme. IEEE Trans. Power Delivery 31(4), 1636–1644 (2016)
14. OMICRON: CPC100 User Manual Primary Test System for Substation Equipment Commissioning and Maintenance. OMICRON electronics GmbH, Hong Kong (2007)
15. Haitipour, E., et al.: Current transformer saturation compensation for transformer differential relays. IEEE Trans. Power Delivery 30(5), 2293–2302 (2015)
16. Laurano, C., et al.: Improving the accuracy of current transformers through harmonic distortion compensation. In: IEEE International Instrumentation and Measurement Technology Conference (I2MTC), Auckland, New Zealand (2019)
17. Sanati, S., Alinejad-Beromi, Y.: Avoid current transformer saturation using adjustable switched resistor demagnetization method. IEEE Trans. Power Delivery 1-1 (2020). Early Access
18. Delzendeh M., Kazemi Karegar, H.: Current transformer saturation compensator by using negative voltage feedback. IEEE Trans. Power Delivery 35, 1200–1208 (2020). Early Access
19. Schubert, T.F., Kim, E.M.: Fundamentals of Electronics: Book 1 Electronic Devices and Circuit Applications. Morgan & Claypool, Fort Collins, CO (2015)
20. Cullity, B.D., Graham, C.D.: Introduction to Magnetism and Magnetic Materials. Wiley, NJ (2009)

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