Hot Carrier Degradation in MOSFETs at Cryogenic Temperatures Down to 4.2 K

Yuanke Zhang, Jun Xu, Tengteng Lu, Yujing Zhang, Chao Luo and Guoping Guo

Abstract—Wide attention has been focused on cryogenic CMOS (cryo-CMOS) operation because of its promising improvement of devices’ and circuits’ performance and wide application prospects. However, hot carrier degradation (HCD) limits the long-term reliability of cryo-CMOS. This article investigates HCD in 0.18 µm bulk CMOS at cryogenic temperature down to 4.2 K. Particularly, the relationship between HCD and the current overshoot phenomenon and the influence of substrate bias on HCD are discussed. Besides, we predict the lifetime of the device at 77 K and 4.2 K. It is concluded that cryogenic NMOS cannot reach the ten years’ commercial standard lifetime at standard VDD. And it is predicted that the reliability requirements can be reached when VDD ≤ 1.768 V and 1.734 V at 77 K and 4.2 K, respectively. Differently, the lifetime of PMOS is long enough even at low temperatures.

Index Terms—Cryogenic CMOS, hot carrier degradation, liquid helium temperature, current overshoot, substrate bias, lifetime prediction

I. INTRODUCTION

CRYO-CMOS has been widely used in neutrino physics experiments, space exploration, and has been researched for quantum computing in recent years [1]–[6]. In order to avoid introducing excessive thermal noise during signal transmission, the interface for the quantum devices using cryo-CMOS is placed at liquid helium temperature (4.2 K), providing a scalable solution for the interface development of quantum chips [7]–[9]. However, early research declared that HCD has a strong correlation with temperature and worsens upon cooling [4], [5], [10]–[12], which severely affects long-term cryo-CMOS operation [10], [13].

To date, HCD has been widely studied around room temperature (RT) [10], [14]–[20], and it leads to the degradation of amplification performance, delay of digital circuits and other adverse effects [14], [21]. In this paper, we investigate HCD in 0.18 µm bulk MOSFETs at cryogenic temperatures down to 4.2 K. The degradation mechanism is analyzed and the effect of temperature on HCD is explained physically. Particularly, the relationship between HCD and the current overshoot phenomenon and the influence of substrate bias on HCD are discussed.

This work was supported by the National Key Research and Development Program of China (Grant No.2016YFA0301700), the National Natural Science Foundation of China (Grants No. 12034018 and 11625419), the Anhui initiative in Quantum Information Technologies (Grants No. AHY080000), and this work was partially carried out at the USTC Center for Micro and Nanoscale Research and Fabrication. (Corresponding author: Chao Luo.)

The authors are with Department of Physics, CAS Key Lab of Quantum Information, University of Science and Technology of China, Hefei 230026, Anhui, China. (e-mail: kc0121@ustc.edu.cn)

The goal of this work is to evaluate the reliability of 0.18 µm bulk MOSFETs operating at cryogenic temperature. Therefore, we predict the cryogenic lifetime of the device, and the rated voltage that meets the reliability requirements is given. This work contributes to cryo-CMOS devices research and cryo-CMOS circuits design.

II. MEASUREMENT SETUP

MOSFETs studied in this work were fabricated by Semiconductor Manufacturing International Corporation (SMIC) 0.18 µm bulk CMOS Technology. The gate oxide thickness (Tox) is 3.6 nm and VDD = 1.8 V. The sample chips were bonded to the chip-carriers with aluminum wires, as shown in Fig. 1(a). The cryogenic measurements were performed in liquid nitrogen Dewar, liquid helium Dewar, and a 1.2 K refrigerator cryostat. All the MOSFETs’ electrical characteristics measurements and stress were performed by a Keysight B1500A semiconductor device analyzer and measured by the four-wire method to remove the influence of wire resistance. The stress was periodically interrupted to measure the device parameters.

To analyze the degradation of the device characteristics, transfer characteristics in both linear region (VDS = 50 mV) and saturation region (VDS = 1.8 V) were measured with the source and substrate terminal grounded. The maximum transconductance (Gmmax) was obtained from linear region transfer characteristics, and the threshold voltage VTH was extracted at the threshold current IT/H = 1.0 × 10⁻⁸ W/L (A).

In the measurements of PMOS, the above values were replaced by the opposite number.

III. RESULTS AND DISCUSSIONS

A. Low temperature characterization

Low temperature operation can improve the performance of MOSFETs, as shown in Fig. 1(b), Table I, and Table II. At low temperatures, the off-state current (IOFF, VDS = 1.8 V and VGS = 0 V) decreases and the saturation current (IDSAT, VDS = VGS = 1.8 V) increases, which greatly improves the ON/OFF ratio. VTH increases at low temperatures, which can be attributed to the decrease of intrinsic carrier concentration and the increase of Fermi potential.

Due to the longer band-to-band tunneling (BTBT) distance at low temperatures [22], the gate-induced drain leakage (GIDL) effect is ameliorated obviously [Fig. 1(b)]. The subthreshold swing (SS, obtained at |VDS| = 50 mV) is given by

\[ SS = \ln(10)nK_BT/q \]

where n, K_B, T, and q is subthreshold slope factor, Boltzmann constant, Kelvin temperature, and
the electron charge, respectively. Therefore, as the temperature decreases, $SS$ decreases significantly, resulting in faster switching speeds of the device. The low-field mobility ($\mu_0$) is extracted from the linear region transfer characteristics and can be expressed as [22]:

$$\mu_0 = \frac{G_{\text{max}} L}{C_{\text{OX}} V_{\text{DS}}} \tag{1}$$

where $C_{\text{OX}}$ is the gate oxide capacitance and the given $|V_{\text{DS}}|$ is 50 mV for our MOSFETs. At low temperatures, the reduced lattice scattering leads to larger $\mu_0$ and larger $G_m$, as shown in Table I and Fig. 1(c), respectively. Differently, $\mu_0$ and $G_m$ of PMOS are the largest at 77 K, as shown in Table II and Fig. 1(d). For PMOS, due to the difference between the work function of the poly gate and the substrate, a light boron implant in the channel is required to adjust $V_{\text{TH}}$, which leads to the formation of the buried-channel. Due to the freeze-out of the implant, the peak of buried-channel mobility is observed around 80 K [23]–[25]. Therefore, the maximum $\mu_0$ and $G_m$ are observed at 77 K.

![Sample chip, wire-bonded to a chip carrier with Al-wire bonds. (b) $I_{\text{DS}}$ versus $V_{\text{GS}}$ at RT, 77 K, and 4.2 K with $V_{\text{DS}} = 1.8$ V in NMOS. $G_m$ versus $V_{\text{GS}}$ at RT, 77 K, and 4.2 K in NMOS (c) and PMOS (d). (e) Output characteristics in W/L = 10 μm/180 nm NMOS at 4.2 K. The kink effect can be observed.](image)

Fig. 1. (a) Sample chip, wire-bonded to a chip carrier with Al-wire bonds. (b) $I_{\text{DS}}$ versus $V_{\text{GS}}$ at RT, 77 K, and 4.2 K with $V_{\text{DS}} = 1.8$ V in NMOS. $G_m$ versus $V_{\text{GS}}$ at RT, 77 K, and 4.2 K in NMOS (c) and PMOS (d). (e) Output characteristics in W/L = 10 μm/180 nm NMOS at 4.2 K. The kink effect can be observed.

The kink effect is observed in the output curve at 4.2 K [Fig. 1(e)], which is attributed to the decrease of $V_{\text{TH}}$ caused by the accumulation of holes in the substrate [26]. In addition, the kink effect can also cause an abnormally steep rise of $I_{\text{DS}}$ at 4.2 K, as shown in Fig. 1(b). When $V_{\text{GS}}$ overcomes $V_{\text{TH}}$, the channel is formed and the holes generated by impact ionization accumulate in the freeze-out substrate. Hence $V_{\text{TH}}$ decreases and $I_{\text{DS}}$ increases (i.e., the kink effect). The increased $I_{\text{DS}}$ generates more holes by impact ionization and repeats the above whole process. Therefore, the increase of $I_{\text{DS}}$ is an avalanche process and reaches the final value when the channel is in strong inversion [26], thus resulting in the abnormally steep rise of $I_{\text{DS}}$ from the off-state to the strong inversion.

| Table I | DC CHARACTERISTICS OF NMOSFETS (W/L = 10 μm/180 nm) AT 300 K, 77 K, AND 4.2 K |
|---------|---------------------------------|
| Temperature | $V_{\text{TH}}$ (V) | $SS$ (mV/dec) | $I_{\text{DSAT}}$ (mA) | $I_{\text{OFF}}$ (A) | $D_{\text{sat}}$ (mA/V) |
| 300 K | 0.356 | 85.05 | 5.87 | 7.6 × 10$^{-11}$ | 3.24 × 10$^2$ |
| 77 K | 0.557 | 28.44 | 7.80 | 4.8 × 10$^{-15}$ | 8.95 × 10$^2$ |
| 4.2 K | 0.591 | 12.54 | 8.45 | 4.6 × 10$^{-14}$ | 8.68 × 10$^2$ |

| Table II | DC CHARACTERISTICS OF PMOSFETS (W/L = 10 μm/180 nm) AT 300 K, 77 K, AND 4.2 K |
|---------|---------------------------------|
| Temperature | $V_{\text{TH}}$ (V) | $SS$ (mV/dec) | $I_{\text{DSAT}}$ (mA) | $I_{\text{OFF}}$ (A) | $D_{\text{sat}}$ (mA/V) |
| 300 K | 0.401 | 86.41 | 2.20 | 4.0 × 10$^{-11}$ | 0.78 × 10$^2$ |
| 77 K | 0.659 | 31.85 | 2.49 | 2.1 × 10$^{-15}$ | 1.34 × 10$^2$ |
| 4.2 K | 0.738 | 15.15 | 2.52 | 2.0 × 10$^{-14}$ | 1.23 × 10$^2$ |

This phenomenon is only observed when $V_{\text{DS}}$ is large enough ($V_{\text{DS}} > 1.4$ V in 10 μm/180 nm MOS, i.e., after the kink), and it is not obviously observed in PMOS.

Coulomb blockade oscillations are observed in small-size devices at deep-cryogenic temperatures, as shown in Fig. 2. The quasi-periodic Coulomb diamond suggests the existence of quantum dots (QD) in the channel [27]. At deep-cryogenic temperature and under low $V_{\text{DS}}$ and low $V_{\text{GS}}$ bias, $I_{\text{DS}}$ mainly depends on the electron transport between source, drain, and the quantum dot. This indicates that 0.18 μm MOSFETs can be used to construct quantum circuits or quantum-classical hybrid circuits.

B. HCD at low temperatures

It is necessary to investigate the worst-case condition of 0.18 μm MOSFETs to determine the limit of device lifetime, hence we carried out measurements on NMOS and PMOS in the case of $V_{\text{Gstress}} = V_{\text{Dstress}}$ (channel-hot electron degradation mode) and $V_{\text{Gstress}} = V_{\text{Istress}}$ (drain-avalanche hot carrier degradation mode, $V_{\text{Istress}} \approx 1/2V_{\text{Dstress}}$) at 300 K, 77 K, and 4.2 K, respectively. Under a given $V_{\text{DS}}$, the substrate current ($I_{\text{sub}}$) shows a bell-shaped behavior with the change of
$V_{GS}$ and $V_{Gstress}\cdot I_{submax}$ is the gate voltage corresponding to the maximum $I_{sub}$. The results show that the worst-case of NMOS is $V_{Gstress}\cdot I_{submax}$ and the worst-case of PMOS is $V_{Gstress}=V_{DSstress}$ at each measurement temperature. Given the difference of worst-case stress, NMOS and PMOS were tested under their respective worst-case condition in the following measurements. Besides, since the degradation process is inversely proportional to the length of the device [31], the measurements were taken on short channel devices to accelerate the HCD process.

Fig. 3(a)-(c) show the linear-region transfer characteristic degradation and transconductance degradation under different stress time at RT, 77 K, and 4.2 K, respectively. The peak of transconductance shifts to more positive $V_{GS}$ with increasing stress time. With the decrease of temperature, the transconductance curves under different stress time become more dispersed, indicating that HCD is more severe at cryogenic temperatures, which is consistent with the conclusion in [4], [5]. Fig. 3(d) shows the saturation-region transfer characteristic degradation. As shown in Fig. 3(e), $V_{TH}$ and $I_{DSAT}$ is positively and negatively shifted, respectively. The shift of $V_{TH}$ indicates the accumulation of negative charges in the gate oxide, which results from hot carriers trapped into the oxide or charged interface created at the oxide interface. Degradation of $G_{mmax}$ is used to analyze the HCD effect in this article, and the lifetime is defined as 10% $G_{mmax}$ degradation.

Degradation of device parameters complies with the power-law function of time [14], [18], [20]:

$$G_{mmax}(I_{DSAT}, V_{TH}) \text{ degradation} \propto t^n$$ (2)

where the parameter $n$ is the time power-law exponent and $t$ is the stress time. If HCD is due to interface state damage ($N_{it}$ degradation), $n$ is in the range of 0.5 to 1 and hot-carrier injecting into the gate oxide ($N_{ot}$ degradation) leads to a smaller $n$ from 0.1 to 0.3 [10], [14], [32]. Fig. 4(a) shows the time power-law exponent of NMOS at RT, 77 K, and 4.2 K. The values of power-exponent $n$ are similar at different temperatures and it indicates that the degradation mechanism is similar at different temperatures: the initial degradation is mainly caused by $N_{it}$ degradation and it changes into $N_{ot}$ degradation as the stress time increases. A time-varying power-law exponent can be used to characterize the HCD process at not only RT but also cryogenic temperatures.

Meanwhile, the relationship between the slope change point and the temperature is noticeable. The interface trap charges are generated and accumulated near the drain side. At cryogenic temperatures, the carrier mobility and the energy of hot carriers increase, hence hot carriers can accumulate enough energy closer to the source to form interface traps, resulting in a larger area of interface trap charge accumulation. Therefore, the larger area of interface traps at cryogenic temperatures leads to more severe $N_{it}$ degradation, and the slope change point shifts to more positive $G_{mmax}$ degradation [dotted line in Fig. 4(a)].

Similar phenomena have also been observed in PMOS, as shown in Fig. 4(b). The initial mechanism is the mixing mechanism of $N_{it}$ degradation and $N_{ot}$ degradation. Because the formation of $N_{it}$ saturates with increasing stress time, $N_{ot}$ degradation is the HCD mechanism for long-term stress time. In addition, due to the higher mobility of PMOS at 77 K (Table II), HCD at 77 K is more severe than that at 4.2 K.

![Image of Fig. 3](image3.png)

**Fig. 3.** At $V_{DSstress}=2.8$ V, $V_{Gstress}\cdot I_{submax}$ in 10 μm/180 nm NMOS, stress time = 0/500 s/1000 s/2000 s: linear region transfer characteristic and $G_{m}$ versus $V_{GS}$ at RT (a), 77 K (b) and 4.2 K (c). (d) Saturation region ($V_{DS}=1.8$ V) transfer characteristic at 4.2 K. Inset: $V_{TH}$ an $I_{DSAT}$ versus stress time at 4.2 K.

![Image of Fig. 4](image4.png)

**Fig. 4.** $G_{mmax}$ degradation versus stress time in 10 μm/180 nm NMOS (a) and PMOS (b) at RT, 77 K, and 4.2 K, plotted in a log-log scale.

C. HCD and the current overshoot

The current overshoot phenomenon at cryogenic temperatures is widely reported in large-size transistors (from 96 μm/12 μm to 10 μm/10 μm) [4], [33], [34], [36], but it is not reported in small size transistors. This is consistent with our measurement results: as shown in Fig. 5(a), the current overshoot phenomenon is observed in 10 μm/10 μm NMOS at 4.2 K and not observed in 10 μm/180 nm NMOS [Fig. 1(e)].

The current overshoot phenomenon can be attributed to the trapped charges in the Si-SiO₂ interface and the positive charges in the interface traps can lead to the decrease of $V_{TH}$ and the increase of $I_{DS}$. When $V_{DS}$ increases further, $I_{DS}$ decreases, which can be attributed to two reasons: (i) The increase of $V_{DS}$ leads to the channel pinch-off, forming the depletion region at the drain side and shortening the effective channel length, so that some interface trap charges do not affect the threshold voltage. (ii) The positive charges in the
The effect of substrate bias on the HCD process has only been studied around room temperature, and no common conclusion is reached [28], [38]. Hence, we investigate HCD with substrate bias at RT and 4.2 K. As shown in Fig. 6(a), at RT, forward substrate bias (FBB) can significantly reduce degradation, and the degradation becomes more severe as the substrate bias becomes more negative in NMOS. This is consistent with [28] but different from [38]. In the pinch-off region, the average value of the transverse (i.e., parallel to the channel) electric field $E_x$ can be expressed as:

$$E_x \approx \frac{V_{DS} - V_{DSAT}}{l}$$

(3)

where $l$ is the length of the pinch-off region, $V_{DSAT}$ is the saturation drain voltage, and $V_{DSAT} \approx V_{GS} - V_{TH}$. With FBB, $V_{TH}$ decreases and $V_{DSAT}$ increases, resulting in the decrease of the transverse electric field. The effective longitudinal (i.e., perpendicular to the channel) electric field $E_y$ can be expressed as:

$$E_y = \frac{1}{\varepsilon_s} \left( \frac{Q_i}{2} + Q_b \right)$$

(4)

where $\varepsilon_s$ is the dielectric constant, $Q_i$ is the inversion layer charge per unit area, and $Q_b$ is the depletion region charge per unit area. Under FBB, the depletion region becomes thinner and $Q_b$ decreases, so that $E_y$ decreases. Hence, in the pinch-off region ($Q_i \approx 0$), both the transverse and the longitudinal electric field decrease under FBB. The decrease of transverse electric field reduces the impact of carriers and the generation of hot carriers, and the decrease of longitudinal electric field reduces the carriers injecting into the gate oxide. Therefore, the reliability of devices is improved with FBB and degraded with reverse substrate bias (RBB).

The HCD process is almost the same under various $V_{Bstress}$ at 4.2 K, as shown in Fig. 6(b). This can be attributed to the freeze-out of the substrate. At 4.2 K, the holes produced by carriers impact ionization accumulate in the freeze-out
substrate, forming a positive substrate fixed potential and leading to the kink effect [Fig. 1(d)]. Therefore, the kink effect indicates the formation of floating substrate potential and the loss of control of the substrate potential [24], thus resulting in the HCD process not being affected by $V_{\text{sub}}$. Therefore, FBB is ineffective in extending the worst-case lifetime of NMOS at 4.2 K.

Differently, FBB can enhance the lifetime of PMOS at both RT and 4.2 K, as shown in Fig. 6(c) and (d). We performed measurements under the worst-case condition of PMOS (i.e., $V_{\text{GS}} = V_{\text{DD}}$), but the maximum $I_{\text{sub}}$ is near $V_{\text{GS}} = 1/2V_{\text{DS}}$. The small $I_{\text{sub}}$ at $V_{\text{GS}} = V_{\text{DS}}$ can not provide enough carriers to the freeze-out substrate to form a floating substrate potential, which means that the substrate potential is still controllable. Therefore, FBB can improve the worst-case lifetime of PMOS at both RT and cryogenic temperatures.

E. Lifetime prediction

The low-temperature lifetime prediction of deep submicrometer MOSFETs has been carried out at 77 K [13], and we extended this work to 4.2 K. Considering the influence of $V_{\text{DS}}$, the HCD power-law relation can be written as [31], [39]:

$$\text{Parameter degradation\%} = \alpha t^n \exp(\beta/V_{\text{DS}})$$

where $\alpha$ is a positive constant, $\beta$ is a negative constant, and $n$ is the time power-law exponent above. When the characteristic degradation percentage of a certain parameter is taken as the failure criterion, the lifetime ($\tau$) can be expressed as [13], [14]:

$$\tau = A \exp(B/V_{\text{DS}})$$

where $A$ is a constant and $B = -\beta ln(t)$. Because the change of $n$ all occurs after 10% $G_{\text{mmax}}$ degradation, $B$ is considered as a constant in this paper. If the definition of lifetime is different, such as 20% $G_{\text{mmax}}$ degradation, then the change of $n$ should be considered in the lifetime prediction. In addition, according to the conclusion in subsection B, with the further increase of temperature ($T > 300$ K), $n$ will change before 10% $G_{\text{mmax}}$ degradation [see Fig. 4(a)]. Therefore, Eq. (6) needs to be used carefully at high temperatures.

For NMOS, the lifetime is tested at the stress voltages: $V_{\text{Dstress}} = 2.8$ V, 2.6 V, and 2.4 V (2.4 V was replaced by 3.0 V at RT), $V_{\text{Dstress}} = I_{\text{submax}}$. For PMOS, the lifetime is tested at $V_{\text{Dstress}} = V_{\text{Gstress}} = -3.2$ V, -3 V, and -2.8 V. According to Eq. (6), experimental data is extrapolated, as shown in Fig. 7(a) and (b). The lifetime prediction of some common DC voltage is also shown in Table III. It shows that NMOS cannot meet the requirement of ten years’ lifetime under standard $V_{\text{DD}}$, which affects cryo-CMOS long-term reliability.

Due to the steeper $SS$ and the ameliorated ON/OFF ratio at cryogenic temperatures, slightly reducing $V_{\text{DD}}$ provides a solution to improve the lifetime without affecting the circuits’ performance, and also benefits the low power consumption design of cryo-CMOS. We calculated the rated $V_{\text{DD}}$ for ten years’ lifetime, as shown in Fig. 7(a). At 77 K and 4.2 K, $V_{\text{DD}}$ should be less than 1.768 V and 1.734 V to meet cryo-CMOS reliability requirements, respectively. Fortunately, the lifetime of PMOS at each temperature is much longer than ten years, as shown in Fig. 7(b). The holes have shorter mean free path, greater effective mass, and higher Si-SiO$_2$ potential energy barriers than the electrons, hence the lifetime of PMOS is much longer than that of NMOS.

### IV. Conclusion

A study of HCD at cryogenic temperature down to 4.2 K is presented in this article. Particularly, the relationship between HCD and the current overshoot phenomenon and the influence of substrate bias on HCD are discussed. Besides, the lifetime of the device is predicted. For NMOS, HCD becomes more severe and the lifetime cannot reach ten years’ commercial standard lifetime at cryogenic temperatures. By extrapolating the measurement data, it is concluded that reducing $V_{\text{DD}}$ to 1.768 V and 1.734 V can reach the rated lifetime at 77 K and 4.2 K, respectively. Fortunately, PMOS has sufficient reliability at each temperature.

### REFERENCES

[1] E. Charbon, F. Sebastianio, A. Vladimirescu, H. Homlule, S. Visser, L. Song, and R. M. Incandela, “Cryo-CMOS for quantum computing,” in EDIM Tech. Dig., Dec. 2016, pp. 13–15, doi: 10.1109/EDIM.2016.7838410.

[2] E. Charbon, “Cryo-cmos electronics for quantum computing applications,” in IEEE Euc Solid State Circuits Conf., Sep. 2019, pp. 1–6, doi: 10.1109/ESSCIRC.2019.8902896.

[3] J. R. Hoff, G. W. Deptuch, Guoying Wu, and Ping Gui, “Cryogenic Lifetime Studies of 130 nm and 65 nm nMOS Transistors for High-Energy Physics Experiments,” IEEE Trans. Nucl. Sci., vol. 62, no. 3, pp. 1255–1261, 2015, doi: 10.1109/TNS.2015.2433793.

[4] E. Gutierrez-D, J. Deen, and C. Claey, Low Temperature Electronics: Physics, Devices, Circuits, and Applications. San Diego, CA, USA: Academic, Oct. 2001, doi: 10.1016/B978-0-12-310675-9.5000-2.
Y. L. Tsai, J. F. Chen, S.-F. Shen, H.-T. Hsu, C.-Y. Kao, K.-F. Chang, and J. J. Tzou, C. C. Yao, R. Cheung, and H. W. K. Chan, “Hot-carrier-...rysicerosene, and E. Charbon.”  “Cryo-cmos electronic control for scalable quantum computing,” in Proc. Des. Autom. Conf., June 2017, p. 1–6, doi: 10.1109/50361639.3072948.

B. Patra, R. M. Incandela, J. P. G. van Dijk, H. A. R. Homulle, L. Song, M. Shahmohammadi, R. B. Staszewski, A. Vladimirescu, M. Babaei, F. Sebastiano, and E. Charbon. “Cryo-cmos circuits and systems for quantum computing applications.” IEEE J. Solid-State Circuits, vol. 53, no. 1, pp. 309–321, Jan. 2018, doi: 10.1109/JSSC.2017.2773549.

J. Wang-Ratkovic, R. C. Laco, K. P. MacWilliams, M. Song, S. Brown, and G. Yabiku, “New understanding of Idi nmos hot-carrier degrada-... device lifet ime and cryogenic temperatures,” Microelectron. Reliab., vol. 37, no. 10, pp. 1747 – 1754, 1997, doi: 10.1016/S0026-2714(97)00153-8.

C. Hwang, J. Gillick, C. Jenq, B. Hammond, and J. Woo, “Bias dependent hot-carrier reliability and lifetime over a wide temperature range,” J. Phys. IV France, vol. 6, no. C3, pp. C3–25–C3–28, 1996, doi: 10.1051/jp4:19960304.

G. Groeseneken, R. Bellens, G. V. den Bosch, and H. E. Maes, “Hot-carrier degradation in submicrometre MOSFETs: from uniform injection towards the real operating conditions,” Semicond. Sci. Technol., vol. 10, no. 9, pp. 1208–1220, Sep. 1995, doi: 10.1088/0268-1242/10/9/002.

J. R. Hoff, R. Arora, J. D. Cressler, G. W. Deptuch, P. Gui, N. E. Lourenco, G. Wu, and R. J. Yarema, “Lifetime studies of 130nm nmos transistors intended for long-duration, cryogenic high-energy physics experiments,” in IEEE Nucl. Sci. Symp. Rec., Oct. 2011, pp. 685–693, doi: 10.1109/NSSMIC.2011.6514083.

A. Gupta, C. Gupta, H. S. Jatana, and A. Dixit, “Investigation of hot-carrier degradation in 0.18-µm mosfets for the evaluation of device lifetime and digital circuit performance,” IEEE Trans. Device Mat. Rel., vol. 19, no. 4, pp. 609–614, Dec. 2019, doi: 10.1109/TDMR.2019.2938839.

J. F. Chen, T-J. Ai, Y-L. Tsai, H.-T. Tsu, C.-Y. Chen, and H.-P. Hwang, “Analysis of high-voltage metal–oxide–semiconductor transistors with gradual junction in the drift region,” Jpn. J. Appl. Phys., vol. 55, no. 852, p. 08PD04, Jul. 2016, doi: 10.7567/JJAP.55.08PD04.

K. R. Mistry, T. F. Fox, R. Preston, N. D. Arora, B. S. Doyle, and D. E. Nelsen, “Circuit design guidelines for n-channel mosfet hot carrier robustness.” IEEE Trans. Electron Devices, vol. 40, no. 7, pp. 1284–1295, Jul. 1993, doi: 10.1109/16.216434.

S. C. Kang, D. Lim, S. J. Kang, S. K. Lee, C. Choi, D. S. Lee, and B. H. Lee, “Hot-carrier degradation estimation of a silicon-on-insulator tunneling fet using ambipolar characteristics,” IEEE Electron Device Lett., vol. 40, no. 11, pp. 1716–1719, Nov. 2019, doi: 10.1109/LED.2019.2942837.

Y.-L. Tsai, J. F. Chen, S.-F. Shen, H.-T. Hu, C.-Y. Kao, K.-F. Chang, and H.-P. Hwang, “Investigation of characteristics and hot-carrier reliability of high-voltage MOS transistors with various doping concentrations in the drift region,” Semicond. Sci. Technol., vol. 33, no. 12, p. 125019, Nov. 2018, doi: 10.1088/1361-6641/aae060.

Y. Yun, J.-H. Seo, D. Son, and B. Kang, “Method to estimate profile of threshold voltage degradation in mosfets due to electret stress.” Microelectron. Reliab., vol. 88-90, pp.186–190, 2018, doi: 10.1016/j.microrel.2018.07.055.

J. J. Tzou, C. C. Yao, R. Cheung, and H. W. K. Chan, “Hot-carrier-induced degradation in p-channel Idi nmosfets.” IEEE Electron Device Lett., vol. 7, no. 1, pp. 5–7, Jan 1986, doi: 10.1109/EDL.1986.26273.

G. Mustafayev, N. Cherkesova, A. Khasanov, A. Mustafayev, and G. Mustafayev, “Impact of defects caused by charged carrierges on the digital vi parameters,” in Int. Symp. Electro, Electron. Eng., Atlantis Press, Aug. 2019.

Y. Liu, L. Lang, Y. Chang, Y. Shan, X. Chen and Y. Dong, “Cryo- genic Characteristics of Multinanoscales Field-Effect Transistors,” IEEE Trans. Electron Devices, vol. 68, no. 2, pp. 456-463, 2021, doi: 10.1109/TED.2020.3041438.

R. A. Wilcox, J. Chang, and C. R. Viswanathan, “Low-temperature character-...zation of buried-channel nmnmos,” IEEE Trans. Electron Devices, vol. 36, no. 8, pp. 1440–1447, Aug. 1989, doi: 10.1109/16.30957.