FusionStitching: Boosting Memory Intensive Computations for Deep Learning Workloads

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Abstract
We show in this work that memory intensive computations can result in severe performance problems due to off-chip memory access and CPU-GPU context switch overheads in a wide range of deep learning models. For this problem, current just-in-time (JIT) kernel fusion and code generation techniques have limitations, such as rough fusion plan exploration strategies and limited code generation ability. We propose FusionStitching, a deep learning compiler capable of fusing memory intensive operators, with varied data dependencies and non-homogeneous parallelism, into large GPU kernels to reduce global memory access and context switch overhead automatically. FusionStitching widens the range of operation combinations that fusion can target beyond previous JIT works by introducing data reuse of intermediate values. It explores large fusion spaces to decide optimal fusion plans with considerations of memory access costs, kernel calls and resource usage constraints. FusionStitching tunes the optimal stitching scheme with a domain-specific cost model efficiently. Experimental results show that FusionStitching can reach up to 2.21× speedup compared to state-of-the-art, with 1.45× on average. Besides these experimental results, we integrated our approach into a compiler product and deployed it onto a production cluster for AI workloads with thousands of GPUs. The system has been in operation for more than 4 months and saves 7,000 GPU hours on average for approximately 30,000 tasks per month.

1 Introduction
Recent years have witnessed a surge of industry scale applications of deep learning models, ranging from images/videos, text/NLP, to billion scale search and recommendation systems [49]. Such workloads are typically expressed as computation graphs, and mapped to hardware through domain specific frameworks (TensorFlow [2], PyTorch [1], MXNet [10], etc). Given the flexibility and expressiveness of modern execution frameworks, there are still challenges regarding to transforming high level computation graphs into efficient kernels to maximize the underlying hardware execution efficiency.

Many current research works mainly focus on compute intensive operations, referring to GEMM and convolution in this paper, as compute intensive operations dominate the execution time for many DNN workloads [6, 11, 34, 39, 46], such as CNN [20, 38, 41]). Compute intensive operations are usually realized as efficient libraries (cuDNN, cuBLAS).

However, recent advancement of deep learning domain has resulted in many novel model structures in which memory intensive patterns occupies a large proportion of time. In this paper, we refer to operators that are not GEMM or convolution as memory intensive ops, such as element wise [42], transpose [44] and reduction [43]. In addition, the amount of memory intensive operators in modern machine learning models can be very large, causing notable GPU kernel launch and framework scheduling overhead. Table 2 contains the collected metrics of various models with TensorFlow implementation. The execution time of memory intensive ops can be more than that of compute intensive ops in some cases, and the kernel calls can be up to 10,406. Optimizing compute intensive ops alone is inadequate to unlock the full performance potential for these models.

It is not feasible to build library for memory intensive operations, because a single memory intensive op is too simple while the combination of such ops various in different models and changes fast as the model evolves. Thus, memory intensive ops are usually generated just-in-time with compilation techniques in modern machine learning frameworks.

A common approach to address memory intensive patterns is computation fusion. Prior works have explored the basic idea in AI workloads [8, 29], database [50], image processing [4, 32, 34], and HPC applications [25, 48] ahead-of-time (AOT). However, how to fuse kernels just-in-time (JIT) efficiently, with unpredictable varied dependencies and non-homogeneous parallelism, is still an open problem. Note that the rapidly evolving AI models introduce diverse and complex combination patterns of ops.

Existing JIT kernel fusion techniques use simple code generation and fusion exploration approach. As for XLA [26],
state-of-the-art JIT optimization engine, it only focuses on memory access optimization for memory intensive ops, but lacks consideration of computation characteristics. In a fusion kernel generated by XLA, each thread is only capable of reading intermediate results produced by itself. If two threads require the same intermediate value, they will recompute it independently. It works good for light element-wise ops (like add, sub, mul), but introduces severer re-computation overhead for ops like reduction, tan, log and other expensive ops. XLA avoids re-computation overhead by only allowing expensive ops (reduction, tan, et.al.) appear in the tail of a fusion, that is not being a producer within a fusion. This trade-off limits the fusion exploration space. Meanwhile, XLA uses a conservative fusion exploration strategy. On one hand, it is a rule-based strategy which cannot cover the various combination of element wise ops and tensor shapes. On the other hand, it uses a greedy approach that is easily to fall into local solution.

We propose FusionStitching, a JIT optimization framework to systematically perform fusion space exploration and generate high-performance kernels efficiently. FusionStitching broadens the fusion exploration space by exploring data reuse between ops. If the intermediate data can be reused by a set of threads, these threads could exchange the intermediate data through register-shuffle and shared memory. This approach allows expensive ops to be fused in the middle of a kernel and widens the fusion possibility. With the expanded fusion exploration space, FusionStitching is able to compose a large set of ops with diverge and complex patterns into one GPU kernel. This is effective to reduce off-chip memory accesses and context switch overhead. Meanwhile, FusionStitching applies a more effective fusion exploration approach to find good fusion patterns. FusionStitching addresses two main challenges of large scope JIT fusion.

The first challenge is how to generate efficient GPU kernel given unpredictable complex fusion pattern just-in-time. A fusion pattern reveals a set of operators to be fused into a single GPU kernel. It is non trivial to handle a complex fusion pattern consisting of a broad range of memory intensive ops with various dependence relationships and tensor dimensions. We provide 4 types of stitching scheme abstractions covering the main patterns for memory intensive ops in machine learning workloads, including independent packing, re-computation, intra-warp reuse and intra-block reuse scenarios. With the stitching schemes, we design an approach that divides a fusion into several sub-groups. Different sub-groups use independent schedules and adjacent sub-groups communicate with proper stitching scheme. FusionStitching explores sub-group and stitching scheme settings automatically for a fusion pattern, along with launch dimension enumeration. Instead of using rule-based approach, we design a cost model for code generation tuning.

The second challenge is to find the optimal fusion plan given complex op graph. A fusion plan reveals how ops in a subgraph are grouped together to form a set of fusion patterns. Note that naive composition of multiple computations may cause notable performance slowdown, as different portions of the kernel may have conflicting memory layout, parallelization and on-chip resource requirements [56]. A deep learning computation graph usually brings huge search space about operation combinations. It is not feasible to evaluate all possible combinations with complexity of $O(2^V)$ where $V$ is the number of ops in the computing graph. We formulate the fusion plan searching as an approximate dynamic programming problem with complexity of $O(V + E)$, where $E$ is the number of edges in the graph. The approximate dynamic programming process produces a limited set of promising fusion patterns with a light-weight cost model. FusionStitching applies beam search to generate the overall fusion plan with these fusion patterns.

We realize FusionStitching into TensorFlow as an optimization component beyond XLA. All the optimizations are opaque to users. FusionStitching supports JIT optimization for both training and inference.

We evaluate FusionStitching on a set of common machine learning models, ranging from natural language processing, OCR, speech recognition to searching and recommendation models. FusionStitching achieves up to $2.21 \times$ speedup compared with XLA, with $1.45 \times$ on average.

In summary, this work makes the following contributions:

- It reveals the importance of memory intensive ops, and broadens the range of op combinations that JIT fusion targets by introducing data reuse of to-be-fused ops.
- It provides a set of fusion scheme abstractions for memory intensive ops in machine learning workloads, and proposes an approach to generate efficient GPU kernels given very complex fusion patterns.
- It proposes a technique to explore good fusion plans just-in-time in the expanded search space of op composition, along with a two-layer cost model of GPU kernels.
- It provides an industry level realization that is opaque to users and evaluates with various modern machine learning models on production cluster.

2 Motivation and Challenge

2.1 Motivation

JIT fusion is the state-of-the-art technique to reduce context switch and memory access overhead of intensive memory operations for machine learning workloads. As the state-of-the-art fusion engine, XLA only supports thread-local data transferring for fusion, which relies on index analyzing and re-computation to improve thread locality. A bad case is to put a reduction in the middle of a fusion pattern. If different threads require the same value of reduction result, each thread needs to recompute the reduction independently and redundantly. To avoid this, XLA does not fuse operations that lead to middle-
reductions. As a result, this strategy misses many optimization exploration space.

Figure 1: The difference of fusion pattern between XLA and FusionStitching for Layer Normalization.

Figure 1 shows how XLA and FusionStitching perform fusion for layer normalization. XLA forms 4 fusions, where fusion.3 and fusion.7 end with reductions and fusion.2 ends with expensive operation. XLA does not do other fusion to avoid re-computation overhead, with the drawback of CPU-GPU context switch and off-chip memory access overhead. While FusionStitching generates only one kernel with all intermediate results residing in on-chip memory and involves no CPU-GPU switching. No re-computation is introduced in FusionStitching.

Static libraries are not feasible to solve this problem as a single memory intensive operation is lightweight and the combinations of them vary in different models. TVM [11, 55] mainly focuses on compute intensive operations but not fusion optimization, whereas XLA only provides simple rule-based fusion strategies for memory intensive ops. In addition, TVM relies on pre-defined schedules for code generation and usually requires a long time for tuning.

2.2 Observation

In this work, we have analyzed a variety of machine learning workloads (Section 7), we get two main observations.

Severe Context Switch Overhead Context switch overhead between CPU and GPU is a severe performance issue. Table 2 shows the breakdown analysis of a wide range of machine learning applications. The count of GPU kernel calls (#) for TensorFlow implementation can reach up to 10,406, which leads to large kernel launch overhead. Even fused with XLA, the kernel calls can be still up to 6,842. As a result, both scheduling and pre-/post-processing time on CPU brought by machine learning framework dominate the execution time for some models (like BERT inference, DIEN, ASR, and CRNN).

Large Portion of Memory-intensive Ops Also in Table 2, the execution time of memory intensive ops can be up to 40% in the overall time for some models. Off-chip memory traffic time usually occupies a large portion of the overall execution time of memory intensive ops. By fusing a large quantity of operations, our system is able to reduce CPU-GPU context switch overhead and leverage high speed on-chip memory to reuse intermediate data between ops.

2.3 Challenges

Although data reuse is a potential opportunity to fuse a large scope of ops together to avoid redundant re-computation, there are several main challenges for both applying reuse for a given fusion pattern and deciding op fusion strategy.

As for applying reuse for a given fusion pattern to generate kernel:

• The first challenge is how to evaluate reuse benefit. Reuse is not always better than re-computation. Reuse will lead to extra inter-thread data communication, whereas re-computation introduces redundant compute overhead but without inter-thread communication. Besides, introducing reuse with shared memory may hurt kernel occupancy, thus hurts parallelism.

• The second challenge is how to apply reuse. There are two types of data reuse: intra-warp and intra-block reuse. Intra-warp/block reuse means that threads within a warp/block reuses intermediate data produced by other threads within the same warp/block. The tradeoff is that, intra-warp reuse has less memory access overhead while intra-block reuse has better parallelism.

For a given machine learning model, the challenge is to decide what ops should be fused together. XLA also tries to solve this challenge, but with limited exploration space. One main problem is that, forming a fusion pattern by data reuse is not always better than separate kernels. Reuse requires data locality within thread-block or warp, which can potentially limit parallelism. Take reduction as an example, reuse of reduction result requires to compute reduction within a block or warp. However, some reductions perform better with several blocks work together, which has higher parallelism. Not fusing such a reduction with its consumers may result in better performance, even with context switch and off-chip memory access overhead. Intra-block reuse may further hurt parallelism as it requires extra shared memory. Another typical problem is that, when operation A can be fused with either operation B or operation C, while B and C cannot be fused together due to some limitation, it is not always easy to decide which one to fuse for A. Rule-based approaches, like XLA, fail to find effective fusion plans for varied models.

3 Overview

3.1 Data Reuse

As described before, FusionStitching widens fusion possibilities by introducing data reuse, a rarely used method in
state-of-the-art JIT fusion techniques. Data reuse can be applied when different threads processing operation \( B \) requires the same value generated by operation \( A \). We assume \( B \) is the consumer of \( A \). The threads requiring the same value can read the same data with inter-thread communication, but do not have to re-compute it redundantly like in XLA. We observe that tensor shapes of a sequence of memory intensive operations always shrink and broaden frequently due to operations like reduce, broadcast, gather, and slice. Thereby the opportunity to explore data reuse is large.

In our work, we explore both intra-warp reuse and intra-block reuse, corresponding to warp composition and block composition in figure 3. Take reduction as an example, intra-warp reuse means that each warp does reduction for a row of data and stores result in the register of the first lane of the warp. Consumers of the reduction read data with register-shuffle from the first lane. Intra-block reuse does reduction for the row with all threads in the block and stores results in shared memory. Consumers of the reduction read data from shared memory. This approach enables stitching operations with on-chip memory while avoiding re-computation. Data locality should be guaranteed for correct data reuse. Intra-warp reuse requires warp level data locality, and intra-block reuse requires block level data locality.

4 Code Generation

Code generator takes a fusion pattern as input, and produces a GPU kernel that implements the fused operators. It is non-trivial to fuse multiple ops into one high performance GPU kernel due to various dependence scenarios and parallelism incompatibilities.

The combination patterns of memory intensive operators in machine workload are numerous, but basic kinds of memory intensive ops are limited. We made three classifications: light element-wise (most elem-wise ops), expensive element-wise (tan, exponential, et.al.), and reduction ops. We pre-define a set of schedules for each kind of memory intensive ops. The left problem of code generation is how to stitch different operators into one kernel and what schedule each individual op applies.

We first systematically investigate four kernel composition schemes (4.1) that covers common execution patterns for memory intensive operations. With these composition schemes, we used an automatic generation solution based on performance modeling (4.3) to find good schedules and generate code for the fusion pattern (4.2).

4.1 Kernel Composition Schemes

We study about four kernel composition schemes, which indicate main behaviors of common memory intensive ops. Different scheme indicates different data dependence and parallel behaviors of kernels to fuse, ranging from no dependence to complex cross-thread dependence, and from uniformed parallelism to non-homogeneous computations. Figure 3 illustrates
the four kind of composition schemes.

**Kernel Packing** packs computations of ops with no data dependence. This scheme is instrumental in reducing context switch overhead of kernel launch and framework scheduling. It also reduces loop control overheads in instruction level. To reduce control flow overhead, we perform aggressive loop fusion [5, 18] to merge as many element-wise ops as possible into a single loop structure when these ops have the same parallelism dimension.

**Thread Composition** fuses dependent ops and transfer intermediate results via registers within a local thread context. This is the fusion scheme XLA applies. This may introduce redundant computations between threads requiring the same value.

**Warp Composition** fuses dependent operators and apply intra-warp reuse. This scheme employs register shuffle to communicate between threads within a warp. A typical case is warp reduction and its consumers, which applies warp level reduction and leverages registers to transfer intermediate results to threads of its consumers.

**Block Composition** applies intra-block reuse and unlocks the potential to enable composing non-homogeneous computations into large fused kernels, as long as these computations can communicate within block level. It makes use of shared memory to transfer intermediate results for data reuse.

**Warp composition** and **block composition** are flexible schemes as they allow different ops to execute in independent schedules in the fused kernel. The only requirement is to keep warp/block locality between producers and consumers. These two schemes are essential to compose a broad range of op kinds with various parallelism characteristics and dependence relationships efficiently.

As far as we know, **FusionStitching** is the first work to thoroughly study about all above composition techniques for just-in-time compilation of memory intensive operations for machine learning workloads. XLA only realizes kernel packing and thread composition. We do not stitch ops that involves inter-block communications as it results in global memory level synchronization and introduces high overhead.

4.2 Kernel Generation

Code generation in **FusionStitching** is not as straightforward as XLA, because of the trade-off of composition schemes we discussed above. We use a cost model based tuning approach in **FusionStitching**, and ease the process by op grouping.

According to the four types of composition schemes, we pre-define a set of schedules for each kind of operators (light element-wise, expensive element-wise, and reduction ops). Specifically, we define a single template for light element-wise ops representing kernel packing and thread composition. Note that we find kernel packing and thread composition can be described with the same schedule. We define three schedules for expensive element-wise ops and reduction ops. The first one represents kernel packing and thread composition. The second one stores intermediate result to the register of the first lane in each warp, representing warp composition. The third one stores intermediate result to shared memory, representing block composition.

**FusionStitching** enumerates all schedule combinations of ops. It estimates these combinations according to cost model (sec 4.3). To ease the enumeration process, we divide ops in a fusion pattern into several groups. Each group applies one schedule and different groups transfer intermediate data with warp/block level reuse.

We group ops according to op types. Given a fusion pattern, we enumerate a small set of grouping strategies. We call sub-root as the output op of a group, and root as the output of the fusion. We first identify sub-roots and generate groups rooted from sub-roots and root. Reduce ops are always regarded as sub-root. Expensive element-wise ops are enumerated to both sub-roots and non sub-roots. Other ops are neither sub-roots. This leads to a set of groups rooted from reduction, expensive element-wise and root ops.

The insight of the grouping approach is that, the schedule of non sub-roots can be determined by the schedule of sub-roots by tensor indices propagation. Thus we only need to enumerate the schedule of sub-roots and root ops, and we can propagate to get schedules of all ops.

**FusionStitching** enumerates grouping strategies, and emulates schedules of every sub-root/root op and launch dimension of the fused kernel. As data reuse requires correct data locality in the reuse scope, schedules do not match data locality requirement are discarded. After estimating the performance of each enumeration with latency-evaluator, **FusionStitching** selects code generation strategy with the best estimated performance.

4.3 Kernel Evaluation: Latency-Evaluator

**FusionStitching** requires an accurate estimation for kernel performance for code generation strategy. Fortunately, as the searching space of code generation is not very large, we can tolerate a relative slow cost model.
We calculate we merge allocation information of all its operands, test the Also, we estimate shared memory usage by life time ana-

where warps in the same wave executes concurrently. L will be spitted into several waves to be executed on a GPU (FusionStitching)

The insight is that, Beside the reuse of intermediate result between producers and consumers with shared memory and register shuffles, FusionStitching fu-

also reduces thread local redundant calculations. Thread local redundant calculations mainly come from mem-

ory access index calculations and thread local intermediate values. It is because different parts in a fusion kernel may use different schedules, and index and some intermediate values are generated independently within each schedule, even in the same thread. Before generating the code, FusionStitching first analyzes the overall index and intermediate value characteristics and then organizes the output code to reuse computations and data as much as possible.

5 Fusion Exploration

As noted before, rule-based approach in XLA is not adequate to handle complex fusion decisions. We use a cost-based searching approach to find good fusion plans. We propose an approximate dynamic programming approach to search for a set of promising fusion patterns(5.2) which may overlap with each other. The searching process is guided by a light-weight domain-specific cost model(5.4). FusionStitching finally generates the overall fusion plan by selecting fusion patterns(5.3).

5.1 Fusion Problem Definition

We formulate fusion exploration as a subgraph searching problem. For computation graph G = (V,E), where V and E are sets of vertices and edges respectively. We define a fusion pattern P_i = (V_i,E_i) as a subgraph of G, with V_i ⊆ V, E_i ⊆ E. A fusion plan is a set of disjoint fusion patterns S = \{P_0, \cdots, P_{k-1}\}. The score function of P_i is annotated as f(P_i). The higher the performance is, the larger f(P_i) is. So the goal of computation fusion problem is to find fusion plan S with maximal \( \sum_{i=1}^{k} f(P_i) \).

5.2 Explore Fusion Patterns

A Brute-force way to enumerate all fusion patterns has a complexity of up to \( O(2^V) \) without pruning. We proposed an approximate dynamic programming approach with complexity of \( O(V+E) \) to find good fusion patterns.

The basic idea of fusion exploration is that, we generate candidate-patterns starting from each vertex in post-order in the graph, and select and compose final fusion plan with these candidate patterns. The candidate-patterns starting from vertex V_i is the set of fusion patterns whose producer node is V_i. We describe how we generate candidate-patterns for each vertex in this section and describe how to compose the final fusion plan in section 5.3

Given a computation graph G, we get a topological sorting list. We generate candidate-patterns for vertices in post-order, from the last vertex to the first vertex. This is to guarantee that each searching results in a fusion pattern with current vertex as producer.

Equation 2 shows the approximate dynamic programming process. C_i is the set of all consumers of V_i. PatternReduc-

4.4 Shared Memory Optimization

It is essential to use shared memory moderately as large amount of shared memory usage hurts kernel parallelism, especially for large granularity compositions. To use as much shared memory as possible while not hurting parallelism, we explore a dataflow based shared memory sharing technique. The insight is that, FusionStitching reuses previous allocated shared memory as much as possible to reduce unnecessary shared memory allocation.

We use dominance tree algorithm [12] for shared memory dataflow analysis. The approach takes a computation graph and shared memory requests as input, and outputs an allo-

cation map. To optimize shared space sharing, we traverse ops of the computation graph in topological order. When an op does not need shared space, previous allocation information will be propagated forward. If an op needs shared space, we merge allocation information of all its operands, test the dominance relation to check if we can share any previously allocated space for current op, and reuse the space if possible.

4.5 Computation Reuse Optimizations

Beside the reuse of intermediate result between producers and consumers with shared memory and register shuffles, FusionStitching also reduces thread local redundant calculations.
1. top 3 candidate-patterns for
   \( V_5 \): \{5\}, \{5,2\}, \{5,2,1\}
   \( V_6 \): \{6\}, \{6,3\}, \{6,3,1\}
   \( V_7 \): \{7\}, \{7,4\}, \{7,4,1\}

2. grouping of \( V_8 \)'s consumers: \{5,6\}, \{7\}

3.1 candidate-patterns of \( V_8 \) with group \{5,6\}:
   \{8\}, \{8,5,2\}, \{8,5,2,1\}, \{8,6\}, \{8,6,3\}, \{8,6,3,1\}, \{8,5,6\}, \{8,5,6,3\}, \{8,5,6,3,1\}, \{8,5,2,6\}, \{8,5,2,6,3\}, \{8,5,2,6,3,1\}, \{8,5,2,1,8\}, \{8,5,2,1,6,3\}
   get top-3: \{8,5,2,1,6,3\}, \{8,5,2,1\}, \{8,6,3,1\}

3.2 candidate patterns of \( V_8 \) with group \{7\}:
   \{8\}, \{8,7\}, \{8,7,4\}, \{8,7,4,1\}
   get top-3: \{8,7,4,1\}, \{8,7,4\}, \{8,7\}

4. merge 3.1 and 3.2 and get overall top-3:
   \{8,5,2,1,6,3,7,4\}, \{8,5,2,1,7,4\}, \{8,6,3,1,7,4\}

Figure 4: PatternReduction case to generate candidate-patterns for \( V_8 \).

**PatternReduction** is the approach to get candidate patterns of \( V_i \) according to all its consumers’ candidate patterns.

\[ P_i = \text{PatternReduction}(C_i) \]  \hfill (2)

We describe PatternReduction approach with an example shown in Figure 4, where \( V_0 \) is the root vertex who produces the output of whole graph. Assume that candidate-patterns for vertices before \( V_8 \) have already been generated. (We only explore top \( k \) patterns in candidate-patterns for each vertex according to score function \( f \). We set \( k = 3 \) in this case.) We will generate candidate-patterns of \( V_8 \) with its consumers’ information. A naive approach is to append \( V_8 \) to all possible combinations of patterns in its consumers’ candidate-patterns sets, and select the top 3 patterns within the appended combinations. However, the combinations will be huge when the consumer number and top \( k \) setting is large, noting that JIT approach requires timely optimization. Instead, we design an approximate divide-and-conquer process to find top 3 patterns with limited complexity as PatternReduction.

We first divide the consumers of \( V_8 \) into several groups and find candidate-patterns for \( V_8 \) considering these groups independently, and finally compose final candidate-patterns by reducing the above results of all groups. We assume the group number in this case is 2 (group \( \{V_5, V_6\} \) and group \( \{V_7\} \)). For group \( \{V_5, V_6\} \), we enumerate all combinations of patterns in candidate-patterns of \( V_5 \) and \( V_6 \). Specifically, there are 15 possible combinations between \( V_5 \) and \( V_6 \), including empty set. We append \( V_8 \) to each of the 15 combinations and select the top 3 patterns as the temporary candidates associated to group \( \{V_5, V_6\} \). We get another top 3 patterns considering group \( \{7\} \) as temporary candidates. We finally select the final top 3 patterns as candidate-patterns for \( V_8 \) from all above 6 temporary candidates. Note we validate top patterns according to score function \( f \).

The PatternReduction process above is recursive if consumers number of a vertex is very large. We first divide the consumers into two groups. To get candidate patterns of a group, we divide the group further until it is small enough.

A constraint of a fusion pattern is that, no cyclic dependence is allowed. Figure 6 shows an example that a cyclic dependence occurs after fusion. FusionStitching discards patterns with cyclic during the searching process. Meanwhile, FusionStitching only explores fusion patterns that the code generator can process. It does not form fusion patterns with cross-block communication requirement.

**Remote Fusion** To further reduce the context switch overhead between CPU and GPU, we try to merge fusion patterns that are not adjacent in the graph after above procedures. As is shown in Figure 5, we add a virtual vertex \( h \) as the producer for all vertices and apply PatternReduction. We finally get the candidate-patterns of \( V_h \), which includes the fusion of remote patterns that are not adjacent. The remote pattern fusion helps to reduce generated kernels and thus reduces the context switch overhead. Remote fusion results in kernel packing for code generation.

### 5.3 Generate Overall Fusion Plan

All candidate-patterns of all vertices, which may overlap with each other, form a new set \( E \). The insight of forming good fusion plan is to select non-overlapped patterns from \( E \) with high score of \( f \). Note \( f \) means how much cost the pattern saves (sec 5.4).

FusionStitching uses beam search \[17\] to generate top-3 (width of the beam) candidate fusion plans, and finally selects the best plan within the 3 candidates with latency-evaluator (sec 4.3).

Specifically, FusionStitching maintains 3 buffer sets to store candidate fusion plans. It traverses from the producer vertex.
to the consumer vertex in op graph $G$, and try to append each candidate pattern of each vertex to each buffer set in turn if it introduces no overlapping. It may result in more than 3 temporal sets after appending in each iteration, and will select top-3 with highest accumulated $f$ as new buffer sets.

After traversing all vertices, each buffer set forms a candidate fusion plan. FusionStitching will use the more accurate cost model latency-evaluator to estimate which candidate plan performs the best. The best one is the final fusion plan.

5.4 Fusion Evaluation: Delta-Evaluator

FusionStitching applies delta-evaluator to form the score function $f$. One insight is that, we only need to estimate the performance gain or loss when forming a fusion pattern, but do not require accurate estimation of the overall execution time. With this insight, the score function $f$ represents the performance gain or loss of a fusion pattern only.

There are three main factors in delta-evaluator: reduced memory access latency, reduced CPU-GPU context switch overhead, and performance penalty of kernel fusion. The score function $f$ is the summary of these three parts, shown in equation 3.

$$f = T_{\text{reduced\_mem}} + T_{\text{reduced\_calls}} - T_{\text{penalty}}$$

We estimate reduced memory access latency ($T_{\text{reduced\_mem}}$) with two factors. The first is the amount of memory traffics between operators to be fused, which can be calculated according to the shape and type of input and output tensors. And the second is the change of memory type to store the intermediate values between operations. We build a regression model to predict the reduced memory access latency when changing the memory type from global memory to register or shared memory, when given memory traffic amount. The regression model is based on latency data we collected offline on various GPU vendors with various amount of data traffic.

$T_{\text{reduced\_calls}}$ can be easily estimated by multiplying the number of fused kernels with a fixed value representing average CPU-GPU context switch time we collected.

The performance penalty ($T_{\text{penalty}}$) is estimated by a simplified version of latency-evaluator (sec 4.3). As fusion plan exploration faces a very large searching space, using latency-evaluator directly takes too long time for JIT optimization. The most time consuming part of latency-evaluator is the estimation of Occupancy. To estimate Occupancy fast, we use a fixed number (16) as registers number, and use the maximal shared memory usage in and between any ops within a fusion pattern as the overall shared memory usage. Life time analyzing of registers and shared memory is discarded in delta-evaluator.

6 Implementation

The fusion exploration and code generation techniques we studied requires heavy implementation efforts and will be a burden if left to users. Meanwhile, TensorFlow evolves fast and porting the realization of FusionStitching from one TensorFlow version to another one is heavy.

To ease the using of FusionStitching and make it portable to any version of TensorFlow, we build FusionStitching as a stand alone add-on. Users can make use of all the techniques without changing any model script, but only need to specify FusionStitching path and setup environment to enable FusionStitching beyond TensorFlow XLA.

Specifically, we add FusionStitching as an extra pass upon XLA framework. After XLA finishes all its optimizations, including its basic fusion pass, we feed the fusion results of XLA into fusion explorer to get larger scope fusions. We do not disable the basic XLAXL fusion pass as there is no conflict to apply FusionStitching based on the naive fusions and a basic fusion reduces optimization time of FusionStitching.

We realize a GPU IR emitter module with the techniques of code generator in FusionStitching. The fusion plan generated by fusion explorer goes through this IR emitter. The IR emitter will compile fusion patterns into llvm IR, GPU ptx IR, and finally GPU binary sequentially.

Note that the input of FusionStitching is the basic fusion results of XLA, and not every basic fusion will be merged into a FusionStitching fusion pattern as a result. The basic fusions not merged into larger fusions by FusionStitching will finally go through basic compilation pass of XLA.

All the above implementations are realized as a hook of TensorFlow, and will be called if FusionStitching is loaded and environment is set.

To hide the optimization tuning time, we develop async-compilation mode in FusionStitching library. As for training, if users set environment as async-optimization, the first several iterations will not execute binaries generated by FusionStitching while FusionStitching is still running in background asynchronously. After FusionStitching generates optimized kernels for the model, the non-optimized ops will be replaced with that of FusionStitching in latter iterations.

7 Evaluation

7.1 Experimental Setup

In this section, we evaluate FusionStitching using a variety of machine learning applications with different characteristics in different fields. Table 1 summarizes the various fields of the evaluated applications and the characteristics of these applications. These applications range from images (CRNN [37]), speech (ASR [52]), NLP (Transformer [47], BERT [15]), to internet scale E-commerce search and recommendation systems (DIEN [57]). The building blocks of these workloads...
We evaluate the speedup of FusionStitching with 16 GB device memory. The server runs Red Hat Enterprise Linux 7.2 with CUDA toolkit 10.2 and cuDNN 7.6.

### 7.2 Overview

We evaluate the speedup of FusionStitching by comparing inference cost or the training time of one iteration for TF, XLA and FusionStitching with the same batch-size. During our test, the accuracy in each iteration of training and the result of inference are the same with TF and XLA. We repeat 10 times and use the average performance to validate speedup. As for training workloads, we collect the execution time from the 11th iteration to the 20th (guaranteed to be stable), to avoid the initialization overhead of the early training iterations.

We show the speedup of FusionStitching in figure 7, where the execution time of TensorFlow is normalized to 1. Compared to TensorFlow, our approach achieves up to 2.42× speedup, with 1.66× on average. Compared to XLA, our approach achieves up to 2.21× speedup, with 1.45× on average. Note XLA shows performance degradation for DIEN (both training and inference), while FusionStitching does not show negative optimization in any of these cases.

We also test the inference workloads on NVIDIA T4 GPU and get the similar speedup.

We apply FusionStitching in production and measure the performance benefits. It shows that FusionStitching saves about 7,000 GPU hours for about 30,000 tasks in a month. The performance result on the cluster shows FusionStitching is robust. Note that XLA, as state-of-the-art JIT engine, cannot be enabled default as it suffers from negative optimizations for many cases.

Overall, the performance benefit of FusionStitching comes from both reduced CPU-GPU context switch and off-chip memory access. FusionStitching gives a good solution to the problems we found (see 2.2). We provide performance breakdown information in the following section.

### 7.3 Performance Breakdown

Table 2 shows the kernel breakdown information, including execution time (T) of memory intensive ops (Mem), compute intensive ops (Math), CPU time (CPU, kernel launch and framework scheduling), CUDA memcpy/memset activities (Cpy) and kernel call times (#). Note that the breakdown profiling process is different with the process to measure the end-to-end performance. This is because profiling introduces some overhead and makes the end-to-end time not accurate. We profile Mem, Math, Cpy time directly, and get CPU time by dividing other time from end-to-end time.

Before we analyze the effect of our technique, we need to point out that XLA affects the behavior of Matrix operations (GEMM and GEMV). It tends to fuse GEMVs into GEMM, and GEMMs to larger GEMM when there are Matrices sharing common input. Some other algebra transformation and loop-invariant code motion also reduces GEMM count. The difference in GEMM count in table 2 is caused by such reasons. Meanwhile, XLA affects the runtime behavior of TensorFlow and leads to more or less CUDA memcpy/memset activities. FusionStitching is built upon XLA and exhibits the same behavior.

According to Table 2, we have the following observations.

**Reduced context switch overhead.** FusionStitching effectively reduces the memory intensive kernel calls of all workloads, which results in reduced kernel launch and framework scheduling overhead. As is shown in Table 2, the number of memory intensive kernel calls with FusionStitching is 38.0% of that with XLA in average, ranging from 27.8% to 48.4%. Meanwhile, FusionStitching reduces CUDA memcpy/memset activities (Cpy time) than XLA, with 34.3% decrease in average. This is because we fuse more ops together into larger kernels than XLA and many CUDA memcpy/memset are combined together. The CPU time difference in table 2 indicates the reduced time due to the decrease of kernel calls and CUDA memcpy/memset activities. FusionStitching achieves up to 61.0% saving of the CPU time comparing with XLA, 41.0% in average.

Take DIEN-train as an example, the kernel call number for memory intensive ops is 2109 with FusionStitching, and 6842 with XLA. Meanwhile, the CUDA memcpy/memset activities is reduced to 1395, comparing to 1996 with XLA. The final CPU time with FusionStitching is significantly less than both TF and XLA, thanks for the reduced kernel calls. Note that XLA increases CUDA memcpy/memset activities and results
Table 2: Kernel execution breakdown. TF: naive TensorFlow. FS: FusionStitching. CPU: the scheduling and pre-/post-processing metrics on CPU. Math: compute-intensive kernels. Mem: memory-intensive kernels. Cpy: CUDA memcpy and memset calls. E2E: the end-to-end time of one iteration (in milliseconds). T: execution time. #: kernel calls number.

| Model | Tech | T/| CPU | Math | Mem | Cpy | E2E |
|-------|------|----|-----|------|-----|-----|-----|
| TF    | T    | 1.55 | 41.69 | 28.45 | 0.15 | 71.84 |     |
|       | #    | 98  | 561 | 102 | 761 |     |     |
| BERT  | T    | 2.3  | 41.89 | 9.56 | 0.15 | 53.9 |     |
| train | #    | 98  | 200 | 97 | 395 |     |     |
| XLA   | T    | 2.8  | 42.11 | 7.02 | 0.03 | 51.96 |     |
|       | #    | 98  | 98  | 20 | 216 |     |     |
| FS    | T    | 3.24 | 1.65 | 0.83 | 0.14 | 5.86 |     |
|       | #    | 70  | 365 | 106 | 541 |     |     |
| BERT  | T    | 0.78 | 2.50 | 0.60 | 0.13 | 4.02 |     |
| infer | #    | 98  | 277 | 94 | 469 |     |     |
| XLA   | T    | 0.59 | 2.46 | 0.40 | 0.04 | 3.49 |     |
|       | #    | 98  | 77  | 30 | 205 |     |     |
| DIEN  | T    | 90.13 | 7.77 | 32.54 | 7.12 | 137.56 |     |
| train | #    | 1218 | 10406 | 1391 | 13015 |     |     |
| XLA   | T    | 124.04 | 9.06 | 37.50 | 6.56 | 177.16 |     |
|       | #    | 1215 | 6842 | 1996 | 10053 |     |     |
| FS    | T    | 48.42 | 7.91 | 35.84 | 5.55 | 97.72 |     |
|       | #    | 1215 | 2109 | 1395 | 4719 |     |     |
| TF    | T    | 27.36 | 2.58 | 7.55 | 1.99 | 39.48 |     |
|       | #    | 406 | 3680 | 225 | 4311 |     |     |
| XLA   | T    | 44.21 | 2.24 | 6.12 | 0.94 | 53.51 |     |
|       | #    | 405 | 2585 | 627 | 3617 |     |     |
| FS    | T    | 17.54 | 2.45 | 3.51 | 0.7 | 24.20 |     |
|       | #    | 405 | 815 | 422 | 1642 |     |     |
| TF    | T    | 5.92 | 107.04 | 81.03 | 1.14 | 195.37 |     |
|       | #    | 399 | 2497 | 522 | 3418 |     |     |
| XLA   | T    | 11.59 | 106.58 | 38.33 | 1.20 | 157.70 |     |
|       | #    | 405 | 903 | 577 | 1885 |     |     |
| FS    | T    | 7.43 | 107.16 | 30.26 | 0.80 | 145.65 |     |
|       | #    | 400 | 423 | 369 | 1212 |     |     |
| TF    | T    | 9.36 | 2.84 | 3.06 | 0.63 | 15.89 |     |
|       | #    | 76  | 1359 | 439 | 1942 |     |     |
| XLA   | T    | 6.61 | 0.09 | 4.00 | 0.40 | 11.10 |     |
|       | #    | 4  | 236 | 257 | 647 |     |     |
| ASR   | T    | 5.51 | 0.11 | 3.10 | 0.45 | 9.18 |     |
|       | #    | 4  | 187 | 284 | 475 |     |     |
| TF    | T    | 23.31 | 6.05 | 6.14 | 1.60 | 37.10 |     |
|       | #    | 256 | 3674 | 890 | 4820 |     |     |
| CRNN  | T    | 12.17 | 0.30 | 11.37 | 1.04 | 24.88 |     |
| XLA   | #    | 7  | 993 | 406 | 1406 |     |     |
| FS    | T    | 6.35 | 0.31 | 7.69 | 1.01 | 15.36 |     |
|       | #    | 8  | 311 | 388 | 707 |     |     |

in severe performance drop here. FusionStitching avoids the increased memcpy/memset calls due to larger kernel granularity and do not suffer from the drawback. DIEN-infer has the similar behavior. Optimizing kernel fusions while considering runtime behaviors (like memcpy activities) could be a future research topic.

Reduced memory intensive op execution time. FusionStitching reduces the total execution time for memory-intensive operations. The speedup of memory-intensive ops for all workloads is $1.39 \times$ in average comparing with XLA, and up to $1.74 \times$. The performance speedup mainly comes from reduced global memory access. By fusing memory-intensive operations aggressively, the intermediate values can be cached in registers and shared memory.

Take CRNN as an example, it reads 667.6 MB global memory with XLA, while FusionStitching reduces the traffic to 225.8 MB. About 66% global memory access has been reduced for memory intensive ops. The execution time of all memory intensive computations thus achieves $1.48 \times$ speedup than XLA.

Overall speaking, FusionStitching supports more complex fusion patterns than XLA with effective kernel generation, which relaxes the fusion conditions and thus reduces the final kernel numbers and intermediate global memory transactions. These two factors are essential for the performance of memory intensive ops (see 2.2). Meanwhile, with well controlled performance estimation and reduced runtime memcpy activities than XLA, FusionStitching is less likely to result in bad case about optimization.

7.4 Fusion Pattern Analysis

We take the Layer Normalization case in Figure 1 again to analyze the fusion result of XLA and FusionStitching. Note Layer Normalization is a very common component in deep learning models.

XLA forms four different fusion kernels. While FusionStitching is able to fuse them all and generate a more efficient kernel. We collect the performance of all kernels of the two version. The single kernel with FusionStitching achieves a speedup of $1.23 \times$ comparing with the sum of all 4 kernels with XLA. For this test, we do not count the context switch overhead for the 4 kernels in XLA version, which further hurts the performance of XLA.

There are two factors that prevents XLA to fuse operators with a larger granularity in this case. The first reason is reduce op in xla-fusion.7 and xla-fusion.3. As we discussed before, XLA does not explore reuse of intermediate results of producer op. Fusing reduce op in the middle of a kernel results redundant computation of the same value in different threads, thus hurts the performance. The second reason is expensive element-wise ops with small tensor shape (xla-fusion.2). XLA does not tend to fuse expensive ops processing small tensors in the middle of a kernel as the fusion will introduce redundant computations of expensive instructions.

Instead, FusionStitching finds notable potential for larger granularity fusion in this case and fuses all operators into one kernel. It applies data reuse to prevent redundant computation. In this way, the intermediate global memory transaction and CPU-GPU context switch is avoided.
7.5 Overhead Analysis

Similar with XLA, FusionStitching is designed for tune-once-run-many-times scenarios, which is a basic characteristic of deep learning workloads. For the training that could take up to several days, FusionStitching only needs to run in the first training iteration. For an inference task, the executable kernels can be prepared once and run many times in the future.

We measure the one-time overhead introduced by FusionStitching compared to XLA for training. The value is the JIT compilation time of FusionStitching minus that with XLA. Results show that the extra overhead is less than 30 minutes for the workloads we evaluated in this paper, which is far less than the overall training time.

As for cost models, we tried to use complete latency-evaluator to estimate $T_{\text{penalty}}$ in delta-evaluator. The results show a much longer tuning time, but do not show better performance of tuning results. It demonstrates the simplified cost model works good for fusion exploration.

A problem of both FusionStitching and XLA is that, they cannot handle dynamic shapes, appears in some deep learning workloads, with low tuning overhead. The reason is that the design of XLA service framework is not friendly to dynamic shape, while FusionStitching is implemented based on XLA service framework. This implementation problem does not affect the insight that FusionStitching shows.

8 Related Work

Many current AI compilation optimization works mainly focus on compute intensive ops [11, 13, 24, 29, 30, 34, 45], but do not pay attention to memory intensive ops. XLA [26] is one work optimizing memory intensive ops in depth. It provides an just-in-time fusion engine to reduce context switch and off-chip memory access overhead. However, XLA lacks to explore data reuse of intermediate value and limits the fusion exploration space. Besides, it uses simple rules to explore fusion strategy, which is not adaptive to varied combinations of ops and tensor shapes. FusionStitching reveals the data reuse opportunity for JIT fusion and proposes cost-based approach for fusion searching and code generation tuning.

Some works study about fusion optimization of machine learning workloads for static patterns. Li et al. [27] explores horizontal fusion for GPU Kernels to increase thread-level parallelism. Appleyard et al. [7], Diamos et al. [16] study about kernel fusion technique to speedup RNN workloads. These works do not study about just-in-time fusion problem that processes fusion patterns unknown ahead. Neither do they explore op combination strategy. Abdolrashidi et al. [3] explores op combination strategies with Proximal Policy Optimization [36] algorithm. This is an ahead-of-time tuning approach that searches in simple fusion rules similar with XLA, and does not explore fusion of complex patterns.

Some works focusing on compute intensive ops have ability of op fusion. Recent TVM [11] and Ansor [55] implementation have fusion ability with simple rules for simple patterns. These two works usually requires a long time tuning process given a static computation description, but are not designed to handle varied combinations of ops timely. Tiramisu [9] applies a similar fusion approach with TVM. Tensor Comprehensions [46] provides a polyhedral based JIT compiler capable of fusing ops together. It focuses on the trade-off of parallelism and data locality. Glow [35] and Latte [45] supports basic fusion and does not explore complex combination scenarios. Astra [40] and Ashari et al.’s work [8] support GEMM and basic element-wise op fusion. None of these works reveal the fusion chance with intermediate data reuse between to-be-fused ops through shared memory and register shuffle just-in-time. They also lacks of a thoroughly study about just-in-time fusion strategy exploration.

Fusion approach has also been applied to a wide range of domains given a static computation description, like HPC [48], database [50], image processing [32, 33]. They meet different challenges comparing with just-in-time compilation of AI workloads. Specifically, they do not fuse kernels that are not known ahead and do not face the choice of fusing which ops together in a huge searching space.

CUDA Graph [19] reduces kernel launch overhead but suffers from severer initialization overhead and large extra GPU memory usage due to graph creation [31]. It does not reduce off-chip memory traffic.

Performance models for GPU and other accelerators is another related research topic [14, 23, 28, 51, 53, 54]. Yet we design a domain specific cost model system for fusion and code generation requirements.

9 Conclusion

This work tackles the problem of optimizing memory intensive operators in machine learning workloads. We show that memory intensive ops are vital to end-to-end performance of various deep learning models. We propose FusionStitching that supports to fuse operators, with complex dependence and non-homogeneous parallelism, to reduce memory access and context switch overhead just-in-time. FusionStitching broadens the fusion possibility beyond state-of-the-art JIT techniques by introducing reuse scheme. FusionStitching consists of fusion explorer and code generator. The fusion explorer selects candidate fusion patterns from the large searching space with appropriate computing complexity, and produces a fusion plan with promising performance expected. We provide a set of kernel composition schemes, with which code generator stitches operators and reuses intermediate values with on-chip memory as much as possible, and tunes the schedules to emit high performance GPU code for a given fusion pattern. A two-layer cost model helps the searching and tuning process of FusionStitching. Results show that FusionStitching outperforms state-of-the-art JIT techniques with up to $2.21 \times$ speedup, $1.45 \times$ on average.
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