Characterization of traps in SiC/SiO₂ interfaces close to the conduction band by deep-level transient spectroscopy

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1. Introduction

SiC metal–oxide–semiconductor field-effect transistors (MOSFETs) are regarded as promising candidates for next-generation high-voltage electrical power switches owing to the high critical electric field of SiC.¹⁻³ However, the low mobility in the SiC/SiO₂ interfaces hinders the potential performance of SiC MOSFETs. Thus, the improvement of the mobility in the SiC/SiO₂ interfaces is a central issue in the research and development of SiC MOSFETs. It is presumed that the traps in the SiC/SiO₂ interfaces are closely related to the degradation of mobility.⁴ In 2000, Saks and Agarwal reported that the low mobility in the SiC/SiO₂ interfaces is caused by the trapping of electrons in the high-density interface traps, on the basis of Hall effect measurements of SiC MOSFETs.⁵ According to their report, most of the electrons at the interface generated by the gate voltage are captured by the high density of interface traps near the conduction band. This high density of interface traps near the conduction band not only reduces the density of free electrons, which contribute to the transport, but also reduces the mobility of free electrons through Coulomb scattering by the trapped electrons. These two adverse phenomena to electron transport are combined, resulting in the deterioration of the effective mobility in the channel. The results of the subsequent detailed studies on the inversion electron transport of various types of SiC MOSFETs using Hall measurements support the degradation mechanism of mobility described above.⁶,⁷

However, the origin and the formation mechanism of the interface traps close to the conduction band are not yet fully understood, although many efforts have been made to clarify them.⁸⁻¹⁰ One of the reasons for the stagnation of the research on interface traps is the difficulty of their characterization. Conventional capacitance–voltage (C–V) methods are not suitable for characterizing them owing to the low activation energy.¹⁰ It is strongly needed to acquire fundamental data on interface traps, which will provide clues in the quest to elucidate what the interface traps are made of and how they are made. In this study, we focus on the dependence of their energy distribution on the process condition of the SiC/SiO₂ interfaces, that is, the oxidation atmosphere and crystal face, because the oxidation reactions and the trap density at the interfaces are expected to vary according to these process conditions.¹¹⁻¹² In fact, it is known that the mobility at the SiC/SiO₂ interfaces is sensitive to these process conditions. The typical mobility in the SiC/SiO₂ interfaces fabricated on the C-terminated face (C-face) by wet oxidation is approximately 90 cm²·V⁻¹·s⁻¹, whereas the typical mobility on the Si-terminated face (Si-face) is less than 10 cm²·V⁻¹·s⁻¹.¹³,¹⁴ Furthermore, the mobility in the SiC/SiO₂ interfaces fabricated by oxynitridation, which comprises annealing or oxidation in a nitric oxide (NO) or nitrous oxide (N₂O) atmosphere, is typically approximately 30 cm²·V⁻¹·s⁻¹, irrespective of the Si- or C-face.¹⁵⁻¹⁹ To characterize interface states, we employ constant-capacitance deep-level transient spectroscopy (CCDLTS), which enables us to estimate the energy distribution of the density of interface states close to the conduction band, by utilizing the dependence of the emission time on energy and temperature.²⁰⁻²² Furthermore, we discuss the effect of the interface states close to the conduction band on electron transport of SiC MOSFETs by simulating the density of trapped electrons, the density of free electrons and the density of total electrons induced by gate voltage at the SiC/SiO₂ interface.

2. Experimental methods

The samples characterized in this study were MOS capacitors on the C-face (0001) or Si-face (0001) of 4H-SiC n-type epitaxial wafers. The density of nitrogen in the epitaxial layer was approximately 1 × 10¹⁶ cm⁻³. The SiC/SiO₂ interfaces of the MOS capacitors were fabricated by the following gate-oxidation processes: (1) oxidation in an O₂ atmosphere at 1250 °C, followed by wet oxidation at 900 °C, followed by H₂ annealing at 800 °C on the C-face (DWHC); (2) oxidation in a N₂O atmosphere at 1250 °C, followed by a H₂ annealing at 1000 °C on the C-face (NHC); (3) oxidation in an O₂ atmosphere at 1250 °C, followed by wet oxidation at 900 °C on the Si-face (DWS); and (4) oxidation in an O₂ atmosphere at 1250 °C, followed by postoxidation annealing in a N₂O atmosphere at 1250 °C, followed by H₂ annealing at 800 °C on the Si-face (DNHS). The thickness of the oxide layer was approximately 50 nm, and the gate electrode was aluminum.
The mobilities of the MOSFETs fabricated by the processes of DWHC, NHC, DWS, and DNHS were approximately 80, 30, 8, and 30 cm²·V⁻¹·s⁻¹, respectively.\textsuperscript{14,18,23})

CCDLTS spectra were obtained by measuring the transient voltage signal generated by a feedback loop to maintain the capacitance at a constant value during the measurement of MOS capacitors in the temperature range from 78 to 400 K. In the CCDLTS measurements of DWHC and NHC samples, the pulse voltage and depletion bias were set to 6 and \(-1\) V at 78 K, respectively. The depletion bias was controlled to maintain the initial capacitance at depletion during the temperature scan. In the case of the DNHS sample, the pulse voltage and depletion bias were set to 6 and \(-3.6\) V at 78 K. The depletion bias was controlled in the same way as the C-face samples during the temperature scan. In this case, the \(C-V\) characteristics showed large voltage shift during the temperature scan. To minimize the effect of the voltage shift in the \(C-V\) characteristics, the pulse voltage was controlled to maintain the difference between pulse voltage and the depletion bias during the temperature scan. For the analysis of the transient voltage signal at each temperature, a deep-level transient Fourier spectroscopy (DLTFS) technique was used.\textsuperscript{20,21})

### 3. Results and discussion

First, we examined the effect of the atmosphere of gate oxidation on the SiC/SiO\(_2\) interfaces on the C-face.\textsuperscript{22}) Figures 1(a) and 1(b) show the \(C-V\) characteristics for both samples caused by the change in the temperature from around 300 to 78 K. From these results, the density of electrons captured and frozen at interface traps at 78 K was estimated to be around \(7 \times 10^{11}\) cm\(^{-2}\) for both samples. The activation energy of these interface traps, which caused the shift of the \(C-V\) characteristics, was more than around 0.2 eV when the cross section of traps was assumed to be \(1 \times 10^{-15}\) cm\(^2\).

Next, we show the CCDLTS spectra of an NHC sample and an DWHC sample in Fig. 2(a), where the vertical axis is the first order of the sine coefficient of the DLTFS signal (b1).

### Fig. 1
High-frequency (1 MHz) \(C-V\) characteristics for (a) NHC sample and (b) DWHC sample at 78 and 300 K.

### Fig. 2
(a) CCDLTS spectra of an NHC sample and a DWHC sample. The vertical axis is the first order of the sine coefficient of the DLTFS signal (b1).\textsuperscript{20,21}) (b) Arrhenius plot for the peak at approximately 90 K (C1) in the CCDLTS spectrum for the NHC sample. The vertical axis is the product of the density of states for electrons in the conduction band (\(N_C\)), thermal velocity (\(v_{th}\)), and the extracted lifetime (\(\tau\)) for C1 from the CCDLTS spectra of DLTFS signals.
with a period width ($T_W$) of 205 ms and a recovery time of 4 ms.\textsuperscript{20,21} In Fig. 2(a), a peak was observed at approximately 90 K in the CCDLTS spectrum for the NHC sample. We refer to this peak as C1 and examine it by Arrhenius-plot analysis. The result is shown in Fig. 2(b) where the vertical axis is the product of the density of states of the conduction band ($N_C$), thermal velocity ($v_0$), and the lifetime ($\tau$) of the C1 peak. We note that the lifetime of traps is calculated from the peak temperature and the correlation function of the CCDLTS spectra in the DLTFS scheme.\textsuperscript{20,21} The obtained activation energy of the traps that comprise the C1 peak (C1 traps) was estimated to be 0.16 eV. The capture cross section of the C1 traps was estimated to be $4 \times 10^{-15}$ cm$^2$. In contrast, the CCDLTS spectrum for the DWHC sample was almost constant and we could not find any peak in the spectrum.

The CCDLTS spectra can be transformed into the energy distribution of the density of the interface traps [$D_\theta(E)$] under the following two assumptions: (1) $D_\theta(E)$ depends only weakly on the energy, and (2) the capture cross section does not depend on the energy or temperature. Figure 3 shows the energy distributions of $D_\theta(E)$ for the DWHC and NHC samples calculated from the CCDLTS spectra. In the calculation of $D_\theta(E)$, the capture cross section for the NHC samples was assumed to be $4 \times 10^{-15}$ cm$^2$, which was derived by means of the Arrhenius plot analysis of the C1 peak. The capture cross section of the DWHC sample was inferred to be $1 \times 10^{-15}$ cm$^2$ by postulating that the capture cross section of traps in the DWHC sample is almost the same as that of C1 traps. $D_\theta(E)$ for the NHC sample steeply increased as the energy became close to the edge of the conduction band, whereas that for the DWHC sample gradually increased. As a result, $D_\theta(E)$ close to the conduction band for the NHC sample was larger than that for the DWHC sample. This large $D_\theta(E)$ close to the conduction band for the NHC sample was larger than that for the DWHC sample. This large $D_\theta(E)$ close to the conduction band for the NHC sample was larger than that for the DWHC sample. This large $D_\theta(E)$ close to the conduction band for the NHC sample was larger than that for the DWHC sample. 

At the end of this section, we estimate the effect of the C1 traps by using a simple analytical model. In contrast, it seemed that the small $D_\theta(E)$ close to the conduction band for the DWHC sample resulted in a relatively large interface mobility of 80 cm$^2$V$^{-1}$s$^{-1}$.

In Fig. 3, we also show the energy distributions of $D_\theta(E)$ characterized by the Hi-Lo method, where high-frequency C–V characteristics were measured at 100 kHz.\textsuperscript{24} It can be seen that the Hi-Lo method underestimated $D_\theta(E)$ compared with those estimated using CCDLTS spectra. This is partly because the frequency of the high-frequency capacitance measurement (100 kHz) was not high enough to measure the real “high-frequency capacitance” for the low-activation-energy side and partly because the voltage-scan time of the quasi-static capacitance measurement was not long enough to measure the real “low-frequency capacitance” for the high-activation-energy side.\textsuperscript{10} We note that the interface traps are modeled as a series connection of the resistance and the capacitance in the equivalent circuit of a MOS capacitor.\textsuperscript{24} Accordingly, the interface traps have cut-off frequencies. To measure the real “high-frequency capacitance”, the frequency of the C–V measurement should be higher than the cut-off frequency of the traps, which exponentially increases as the energy of traps approaches the edge of the conduction band.\textsuperscript{20} Therefore, the measured “high-frequency capacitance” was overestimated at an energy close to the edge of the conduction band, which led to the underestimation of $D_\theta(E)$. As for the deep traps (>0.5 eV), the capacitance measurements tended to be carried out in a nonequilibrium state, which also led to the underestimation of $D_\theta(E)$. For the NHC sample, the pile up of the nitrogen atoms at the SiC/SiO$_2$ interface\textsuperscript{25} may cause a deviation in the estimated trap energy in the C–V measurements. In summary, the $D_\theta(E)$ characterization of the SiC/SiO$_2$ interfaces by the Hi-Lo method at room temperature has a numbers of problems; thus, it should be avoided.

Hereafter, we discuss the effect of crystal faces on the C–V characteristics and the CCDLTS spectra to investigate the origin of the C1 traps and other defects at the SiC/SiO$_2$ interfaces. First, in Fig. 4, we show the C–V characteristics of MOS capacitors on the Si-face at 78 and 300 K: (a) DNHS (oxynitrided) sample and (b) DWS (wet oxidized) sample. In Fig. 4(a), the C–V characteristics of the DNHS sample showed a small voltage shift of around 0.2 V at 78 K compared with those at 300 K. The estimated electron density that was captured and frozen at interface traps at 78 K was less than $1 \times 10^{11}$ cm$^{-2}$. It should be noted that, although the voltage shift of the C–V characteristics at 78 K for the DNHS sample (Si-face) was smaller than that for the NHC sample (C-face), the mobility of the SiC MOSFET on the Si-face made by the DNHS process was almost the same as that on the C-face made by the NHC process. At first sight, it seemed that this fact would be contradictory to the widely accepted hypothesis that the interface states is the main cause of the low mobility of SiC MOSFETs. However, it should be pointed out that the energy distribution of interface traps is needed to discuss the effect of interface traps on mobility. At the end of this section, the discussion on the relationship between the energy distribution of interface states density and the mobility is given. In Fig. 4(b), it can be seen that the C–V characteristics for the DWS sample showed a large voltage shift of around 8 V at 78 K. The estimated density of electrons that were captured and frozen at interface traps at 78 K was more than $3 \times 10^{12}$ cm$^{-2}$. This interface trap density is
One of this type of SiC MOSFETs in conducting states. This means that the major portion of electrons at the interface in a conducting state of SiC MOSFETs fabricated by the DWS process are likely to be captured by the interface traps. Accordingly, the large voltage shift of the C–V characteristics with decreasing temperature seems to be consistent with the low mobility of SiC MOSFETs on the C-face fabricated by wet gate oxidation.

Next, we move on to the discussion of CCDLTS spectra. Figure 5 shows the CCDLTS spectra for the oxynitrided MOS capacitor on the C-face (the NHC sample) and that on the Si-face (the DNHS sample). We found two peaks (O1 and O2) in the CCDLTS spectrum for the DNHS sample, as shown in Fig. 5. From an Arrhenius-plot analysis, the activation energies of the O1 traps and O2 traps were estimated to be 0.14 and 0.37 eV, respectively. These peaks were also reported by Basile et al. It should be noted that the energy of the C1 trap at the SiC/SiO2 interface on the C-face was almost the same to that of the O1 trap on the Si-face. On the other hand, the O2 peak in the CCDLTS spectrum was specific to the SiC/SiO2 interface on the Si-face. The absence of the O2 peak in the CCDLTS spectrum of the SiC/SiO2 interface on the C-face suggested that the density of O2 traps on the C-face was, at least, negligible compared with that of the O1 traps. The dependence of the trap densities on the crystal faces provides an insight into the origin and formation mechanism of traps in the SiC/SiO2 interface.

Here, we review the structure of the SiC/SiO2 interface on the Si- and C-face. For the SiC/SiO2 interface on the Si-face, the uppermost Si atoms, which terminate the SiC layer, are connected to the O atoms in the SiO2 layer. For the SiC/SiO2 interface on the C-face, it may be reasonable to assume that the uppermost C atoms are connected to the O atoms in the SiO2 layer. However, first-principles molecular-dynamics calculations showed that this interface structure is not stable. Consequently, it is believed that the Si atoms in the SiO2 layer are connected to the uppermost C atoms in SiC. One of this type of SiC/SiO2 structure is proved to be stable according to first-principles molecular-dynamics calculations. Whatever else it might be, the SiC/SiO2 interface on the C-face may be more unstable than that on the Si-face. This may cause the high oxidation rate of the C-face, which is ten times higher than that of the Si-face. Furthermore, the oxidation mechanism may be different between the C- and Si-face. We speculate that the generation of O2 traps on the Si-face may be due to the oxidation mechanism specific to the Si-face.

Basile et al. reported that the O1 and O2 traps are defects in the oxide on the basis of a comparison of CCDLTS spectra of MOS structures on the Si-face of 4H-SiC and those on the Si-face of 6H-SiC. In consideration of their report, the C1 traps on the C-face, the O1 and O2 traps on the Si-face are likely to be oxide traps. Furthermore, the C1 traps on the C-face are likely to be the same as the O1 traps on the Si-face because the energy of each of them is almost the same. We presume that the origin of a C1 trap is one of C-related defects (variations of a carbon dimer or a single carbon defect) in SiO2 on the basis of the comparison of the energy of the C1 traps with the charge transition energy of a point defect in SiO2 using first-principles calculations.

CCDLTS spectra of SiC/SiO2 interfaces oxidized in a wet atmosphere on the C-face (a DWHC sample) and that on the Si-face (a DWS sample) are shown in Fig. 6. The CCDLTS spectrum of the DWS sample (Si-face) was much larger than that of the DWHC sample (C-face). The activation energy of the first peak was 0.17 eV, which corresponds to O1 traps. As
for the second peak, because of the broad and high density of the traps, we could not obtain the activation energy of O2 traps. This difference in the characteristics of the CCDLTS spectra between the Si-face and the C-face is consistent with the difference in mobilities between them (DWHC: 80 cm2·V−1·s−1, DWS: 8 cm2·V−1·s−1). The low mobility of SiC MOSFETs fabricated by the DWS process is caused by the decrease in the density of mobile electrons by the capture of electrons in the high density of O1 traps. This difference in mobility mechanism in a wet atmosphere is different between the C-face and the Si-face and that the difference in the oxidation mechanism causes the difference in the observed trap density between the C-face and the Si-face. A more detailed investigation of the wet oxidation of SiC in terms of first principles is needed to clarify the mechanism of removal of the C1 traps.

Next, we examined the effect of C1 traps on the electron transport at the SiC/SiO2 interface oxidized in a N2O atmosphere on the C-face by comparing the free electron density, the trapped electron density at C1 traps, and the total electron density at the interface induced by gate voltage. The density of the trapped electrons \( n_{\text{trapped}}(E_F) \) as a function of Fermi energy at the interface \( E_F \) is given by the product of interface trap density \( D_{\text{fi}}(E) \) and the Fermi–Dirac distribution function, as

\[
n_{\text{trapped}}(E_F) = \int_{-\infty}^{\infty} D_{\text{fi}}(E) \frac{1}{1 + 2 \exp[e(E - E_F)/(k_B T)]} dE, \tag{1}
\]

where the degeneracy factor is assumed to be 2. The free electron density \( n_{\text{free}}(E_F) \) in the inversion layer at the interface is also a function of \( E_F \) and is expressed as

\[
n_{\text{free}}(E_F) = \sqrt{\frac{2e_\infty e_0 N_C}{\varepsilon_C}} \exp[\frac{-e(E_C - E_F)}{e k_B T}] e^2, \tag{2}
\]

where \( e_\infty \), \( e_0 \), \( N_C \), and \( E_C \) are the relative permittivity of 4H-SiC, the vacuum permittivity, the effective density of states for electrons in the conduction band, and the edge of the conduction band. In this calculation, the doping of the p-body is assumed to be \( 1 \times 10^{16} \text{cm}^{-3} \). The total electron density \( n_{\text{total}}(E_F) \) is the sum of the free electron density and trapped electron density:

\[
n_{\text{total}}(E_F) = n_{\text{free}}(E_F) + n_{\text{trapped}}(E_F). \tag{3}
\]

The electric field in the oxide is

\[
F_{\text{OX}}(E_F) = q[n_{\text{free}}(E_F) + n_{\text{trapped}}(E_F) + n_{\text{dep}}(E_F)]/\varepsilon_{\text{OX}}, \tag{4}
\]

where \( \varepsilon_{\text{OX}} \) and \( n_{\text{dep}}(E_F) \) are the dielectric constant of oxide and the areal density of ionized acceptors in the depletion region. The approximate gate voltage is obtained by multiplying \( F_{\text{OX}}(E_F) \) by the thickness of the gate oxide. For example, roughly speaking, if the thickness of the gate oxide is 50 nm, the electric field of 2 MV/cm corresponds to the gate voltage of 10 V. The energy distribution of C1 traps was modeled by the Gaussian distribution. In Fig. 7, the measured energy distribution of C1 traps and the Gaussian distribution model of C1 traps used in the calculation are shown. In this model, the peak and the standard deviation of the Gaussian model were adjusted to reproduce the measured energy distribution of \( D_{\text{fi}}(E) \) around the peak of C1 traps. The integrated areal density of this model resulted in \( 5 \times 10^{13} \text{cm}^{-2} \). By using Eqs. (1), (2), and (3) and the C1 trap model, the trapped, free, and total electron densities as functions of the electric field in the gate oxide were calculated. The results are shown in Fig. 8. The calculation indicated that the trapping of electrons in C1 traps did not occur if the total electron density exceeded \( 1 \times 10^{12} \text{cm}^{-2} \), as shown in Fig. 8(a). The calculation also showed that the trapped electron density was higher than the free electron density if the total electron density was less than \( 7 \times 10^{11} \text{cm}^{-2} \), as shown in Fig. 8(b). That is to say, the trapping of electrons in C1 traps was predominant in the electron transport only just after the onset of the formation of the inversion layer, where the total electron density was less than \( 7 \times 10^{11} \text{cm}^{-2} \). If the density of induced electrons exceeded \( 1 \times 10^{12} \text{cm}^{-2} \), the trapping of electrons in C1 traps was negligible compared with electrons in the inversion layer induced by gate voltage. Therefore, it is concluded that C1 traps are not the direct cause of the degradation of the effective mobility in the SiC/SiO2 interfaces, because the electron density at the channel of the SiC...
MOSFETs in a conducting state is typically more than $1 \times 10^{12} \text{ cm}^{-2}$. In fact, it is reported that around half of the electrons induced by the gate voltage are trapped at the interface of a NO-annealed MOSFET. Our calculated results implied that the reported high incidence of the trapping of electrons at the interface is caused by the high density of traps that have lower energy than that of C1 traps.

In the previous discussions, we implicitly assumed that electrons captured by traps were frozen. However, in reality, trapped electrons and free electrons are shuffled through capture and emission processes, and therefore, it seems that most of the electrons at the interface contribute to the transport in the end. As the closing of these discussions, we examine the effect of the occasional exchange between trapped electrons and free electrons on mobility at the interface. First, we note that the mobility is proportional to the momentum relaxation time. The time scale of the momentum relaxation time is typically $10^{-14}$ s in the case of SiC MOSFETs, whereas the time scale of the trapping relaxation time is more than $10^{-12}$ s, even if we assume zero activation energy. Namely, the captured electrons can be considered to be frozen when we examine the mobility. Accordingly, the mobility is not directly affected by the capture and emission of electrons. We note that the Coulomb interaction from captured electrons at acceptor-type traps indirectly affects the mobility.

4. Conclusions

CCDLTS measurements were made to characterize $D_{opt}(E)$ close to the bottom of the conduction band for SiC/SiO$_2$ interfaces on the Si-face and the C-face fabricated by two techniques: oxynitridation and wet oxidation. The measured DLTS spectra showed that the $D_{opt}(E)$ for interfaces on the C-face and the Si-face fabricated by oxynitridation were larger than that for the interface on the C-face fabricated by wet oxidation. It was also shown that the $D_{opt}(E)$ for interfaces on the Si-face fabricated by wet oxidation was much larger than those for the other three types of interfaces. Arrhenius-plot analysis of the peak at approximately 90 K in the DLTS spectra for oxynitrided interfaces on the C-face and the Si-face was carried out. The traps comprising the peak in the case of the C-face were named C1, and the traps comprising the peak in the case of the Si-face were O1. Arrhenius-plot analysis showed that these traps had approximately the same energy of 0.16 eV. On the basis of this result, it was concluded that the C1 traps on the C-face were likely to be the same as the O1 traps on the Si-face. The origin of the C1 traps was speculated to be one of the carbon-related defects in the oxide close to the interface; such defects are common around the SiC/SiO$_2$ interfaces on the C- and Si-face. We also found that C1 traps were eliminated by wet oxidation only on the C-face. It was speculated that the elimination of C1 traps by wet oxidation on the C-face may be caused by the oxidation reaction specific to the combination of the C-face and H$_2$O.

To examine the effect of C1 traps on the electron transport at the interface, we calculated the trapped electron density in C1 and the free electron density at the interface as a function of applied electric field in the oxide. The calculation showed that the trapped electron density in C1 was predominant just after the onset of the formation of the inversion layer and that trapping of electrons in C1 did not occur when the SiC MOSFET was in a conducting state. Accordingly, we concluded that C1 traps were not the direct cause of the degradation of the effective mobility. It was speculated that the deterioration of the transport of electrons at the SiC/SiO$_2$ interfaces was caused by the high density of interface traps, which have lower energy than that of C1 traps.

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