The article addresses the issue of reliability of complex embedded control systems in the safety-critical environment. In this article, we propose a novel approach to design controller that (i) guarantees the safety of nonlinear physical systems, (ii) enables safe system restart during runtime, and (iii) allows the use of complex, unverified controllers (e.g., neural networks) that drive the physical systems toward complex specifications. We use abstraction-based controller synthesis approach to design a formally verified controller that provides application and system-level fault tolerance along with safety guarantee. Moreover, our approach is implementable using a commercial-off-the-shelf (COTS) processing unit. To demonstrate the efficacy of our solution and to verify the safety of the system under various types of faults injected in applications and in the underlying real-time operating system (RTOS), we implemented the proposed controller for the inverted pendulum and three degrees-of-freedom (3-DOF) helicopter.

CCS Concepts: • Hardware → System-level fault tolerance; Safety critical systems; • Computer systems organization → Reliability; Embedded software;

Additional Key Words and Phrases: Cyber-physical systems, fault-tolerance, full system restart, nonlinear systems, abstraction-based control

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1 INTRODUCTION

With the increased use of embedded systems in various safety-critical environments, these systems are expected to provide high performance with reliability. Delivering high performance drives the need for more complex systems.\(^1\) As a consequence, it increases the possibilities for errors and makes formal verification more challenging.

In the safety-critical environment, the use of complex embedded control systems where one or more control applications run on top of the real-time operating system (RTOS) and share the resources may lead to safety violations\(^2\) due to various software level faults. There are two main root causes of such faults. First, the control application may issue a set of unsafe commands due to the incorrect logic (bugs) or fail to generate any commands at all (referred to as application-level faults). Second, even with a bug-free control application, faults in underlying software layers such as the RTOS can disrupt the execution of the controller and jeopardize the safety (usually referred to as system-level faults). Ideally, all the components of these systems including the RTOS must be formally verified to ensure that they are fault-free. However, due to the high complexity, formal verification of the entire platform is very difficult. Therefore, designing architectures that enable the system designers to utilize components such as RTOS and vendor drivers without requiring to prove their correctness to guarantee safety is very important.

In this work, we proposed a novel approach to design controller that provides safety guarantee on the physical component in the presence of application-level and system-level faults. Moreover, the proposed solution provides fault-tolerance and liveliness guarantees only using one commercial-off-the-shelf (COTS) computing platform. The proposed approach uses full system restart to recover from such application and system-level faults. However, restarting in the safety-critical environment is very challenging. In our previous work\(^7\), we provided a solution for designing controllers ensuring fault-tolerance and safety for linear physical systems. Designing such controllers becomes very challenging if the physical components exhibit nonlinear dynamics (which is the case in most real applications). To address this, in this article, we provide a procedure for the synthesis of abstraction-based correct-by-construction controllers for nonlinear physical systems that enables the entire computing system to be safely restarted at runtime. This controller can keep the nonlinear control system inside a subset of safety region, only by updating the actuator input at least once after every system restart. In this article, we refer to this controller as Base Controller (BC).

Restarting a system is an effective approach for recovery from unknown faults at runtime with a very predictable outcome. As soon as a fault occurs that disrupts the execution of critical software components, a hardware watchdog timer (WD) restarts the system. During a restart, a fresh image of all the software (middleware, RTOS, and applications) is loaded from a read-only storage, which recovers the system into an operational state. Prior to this work, restarting was proposed as a way to increase the availability of non-safety critical systems\(^{15–17, 19–21, 40}\). Alongside, partial restarting of safety-critical systems using extra hardware was investigated in Refs\(^6\) and\(^11\). To the best of our knowledge, this is the first work that proposes safe restarting of the entire system in a safety-critical environment containing nonlinear physical components.

Having only BC and the WD mechanism, which enables restarting, allows the system to remain safe, tolerate faults, and recover from them. However, it does not make any progress toward its mission goal. To address this issue, BC is complemented with a Mission Controller (MC) (e.g., a neural network) and a Decision Module (DM). The MC is an unverified, high-performance, complex

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\(^1\) Such systems usually use the operating system (OS) primitives to perform I/O or to set up concurrent threads\(^{26}\), utilize vendor developed drivers and use open source libraries\(^{38}\).

\(^2\) In this article, safety means not to violate the constraints of the physical components.

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controller that drives the system toward the mission setpoints. It may contain unsafe logic or bugs that jeopardize safety. To maximize the progress toward the mission goals, in every control cycle, DM checks the MC command. If it satisfies the safety requirements, DM allows it to be sent to the actuators. Otherwise, BC command is applied to the system. By doing so, MC drives the system for as long as possible, and, whenever it is not possible, BC takes the control. The flushing task sends a control signal to an actuator and updates the hardware WD of the platform after sending the input signal. The logical view of this design is depicted in Figure 1.

In the proposed design, the only components that need to be verified for correct functionality are BC, DM, and Flushing Task. Any fault in the system software (System-Level or Application-Level) that results in a fail-silent failure (also known as fail-stop) of these two components leads to WD triggering a system-wide restart and recovery. However, our design does not protect the system from faults that alter the logic of BC or DM at execution times. In summary, this design enables the system to provide formal safety guarantees by verifying only the correctness of BC, DM, and Flushing Task instead of the entire MC, RTOS, and middleware.

The key contributions of our work are:

— Construction of formally verified base controllers for safety-critical applications with non-linear physical components, which guarantee safe full system restart for application and system level fault tolerance.
— Tolerating application-level faults as well as system-level faults using only one COTS processing unit.
— Empirical validation of both the practicality of our proposed design and the safety guarantees through fault-injection testing on a prototype controller for the nonlinear inverted pendulum system and a 3-DOF helicopter.

2 RELATED WORK

The concept of utilizing an unverified, complex controller along with a simple, verified safety controller for fault tolerance was initially proposed as Simplex Architecture in Refs [34]–[36]. In earlier simplex designs, fault tolerance was achieved in one of two ways. In some of these designs such as Refs [18] and [33]–[36], all three components (safety controller, complex controller, and decision unit) share the same computing hardware (processor) and software platform (OS, middleware). As a result, these designs only protect the safety against the faults in the application logic of the complex controller. And, there is no guarantee of the correct behavior in the presence of system-level faults. Our proposed design protects the system from both application-level and system-level faults.
Some Simplex-based designs such as System-Level Simplex [11], Secure System Simplex Architecture (S3A) [28], and other variants [41] run the safety controller and the decision logic on an isolated, dedicated hardware unit. By doing so, the trusted components are protected from the faults in the complex subsystem. However, exercising System-Level Simplex design on most COTS multicore platforms/system-on-chip (SoC) is challenging. The majority of commercial multicore platforms is not designed to achieve strong inter-core fault isolation due to the high-degree of hardware resource sharing. For instance, a fault occurring in a core with the highest privilege level may compromise power and clock configurations of the entire platform. To achieve full isolation and independence, one has to utilize two separate boards/systems. In contrast, the approach proposed in this article needs only one processor and tolerates system-level faults.

Note that the control domain of the proposed BC depends on the system dynamics and the restart time of the platform. Increased restart time shrinks the domain of the BC. For a given system, it may be empty; meaning that the dynamics of the system does not allow a controller with such properties to exist. System-Level Simplex does not have this limitation because it uses a dedicated hardware that is not impacted by faults (or restarts) in the complex controller unit. The proposed approach is especially suitable for the Internet of Things (IoT) applications, requiring increased robustness at low cost and without using extra hardware as System-Level Simplex requires.

The notion of restarting as a means of recovery from faults and improving system availability is previously proposed in the literature. These approaches are generally divided into two categories, viz., (i) revival, reactively restart a failed component, and (ii) rejuvenation, prophylactically restart functioning components to prevent state degradation [14]. Our approach, as described in this article, fits in the former category. However, with slight modification, our design can incorporate periodic self-triggered restarts to prevent future unscheduled unavailable times. In the second form, this work can also be categorized in the latter category. It is worth mentioning that rejuvenation is a very broad term and many fault-recovery techniques may perform some form of rejuvenation as well. The novelty of our work is not in the mechanism used for rejuvenation—restarting—rather, the controller logic, decision module logic, and the timing of the restarts and those that enable safety.

Most of the previous works on restarting are proposed for traditional non safety-critical computing systems such as servers and switches. Authors in Ref. [15] introduce recursively restartable systems as a design paradigm for highly available systems and use a combination of revival and rejuvenation techniques. Earlier literature [16, 17, 20] illustrates the concept of microreboot, which consists of having fine-grain rebootable components and trying to restart them from the smallest component to the biggest one in the presence of faults. The works of Refs [19], [21], and [40] focus on failure and fault modeling and try to find an optimal rejuvenation strategy for various systems. In this context, our previous work in Reset-Based Recovery [6] was an attempt to utilize restarting as a recovery method for computing systems in safety-critical environments. In Ref. [6], we used System-Level Simplex architecture and proposed to restart only the complex subsystem upon the occurrence of faults. This is feasible because the safety subsystem runs on a dedicated hardware unit and is not impacted by the restarts in the complex subsystem. The approach of the current article is significantly different and uses only one hardware unit.

3 CONTROL SYSTEM DESCRIPTION

3.1 Notations

The symbols \( \mathbb{N} \), \( \mathbb{N}_0 \), \( \mathbb{Z} \), \( \mathbb{R} \), \( \mathbb{R}^+ \), and \( \mathbb{R}_0^+ \) denote the set of natural, nonnegative integer, integer, real, positive, and nonnegative real numbers, respectively. We use \( \mathbb{R}^{n \times m} \) to denote a vector space of real matrices with \( n \) rows and \( m \) columns. The identity matrix in \( \mathbb{R}^{n \times n} \) is denoted by \( I_n \) and
zero matrix in $R^{n \times m}$ is denoted by $0_{n \times m}$. For $a, b \in (\mathbb{R} \cup \{-\infty, \infty\})^n$, $a \leq b$ component-wise, the closed hyper-interval is denoted by $[a, b] := \mathbb{R}^n \cap ([a_1, b_1] \times [a_2, b_2] \times \cdots \times [a_n, b_n])$. We identify the relation $R \subseteq A \times B$ with the map $R : A \rightarrow 2^B$ defined by $b \in R(a)$ if $(a, b) \in R$. Given a relation $R \subseteq A \times B$, $R^{-1} = \{(b, a) \in B \times A \mid (a, b) \in R\}$. $Q \circ R$ denotes the composition of maps $Q$ and $R$, $Q \circ R(x) = Q(R(x))$. The map $R$ is said to be strict when $R(a) \neq \emptyset$ for every $a \in A$.

3.2 Nonlinear Control Systems

Definition 3.1 (Nonlinear Control Systems). A nonlinear control system is a tuple $\Sigma = (\mathbb{R}^n, U, \mathcal{U}, f)$, where $\mathbb{R}^n$ is the state space; $U \subseteq \mathbb{R}^p$ is a bounded input set; $\mathcal{U}$ is a subset of the set of all functions of time from $\mathbb{R}_0^+$ to $U$; and $f$ is a locally Lipschitz continuous map from $\mathbb{R}^n \times U$ to $\mathbb{R}^n$.

The trajectory $\xi$ is said to be a solution of $\Sigma$ if there exists $v \in \mathcal{U}$, satisfying

$$\dot{\xi}(t) = f(\xi(t), v(t))$$

for any $t \in \mathbb{R}_0^+$. We emphasize that the locally Lipschitz continuity assumption on $f$ ensures existence and uniqueness of solution $\xi$ [37]. We use notation $\xi_{x,v}(t)$ to denote the value of solution at time $t$ under the input signal $v$ and starting from initial state $x = \xi_{x,v}(0)$.

3.3 Formulating Safety

In physical systems, maintaining all states and control inputs within safe limits is very important in order to avoid damages to the system itself or the environment around it. In this article, we define safety region $S$ as a subset of the state space. For example, one can define it as:

- polytope $S = \{x \in \mathbb{R}^n \mid H_x \cdot x \leq h_x\}$ parameterized by $H_x \in \mathbb{R}^{q \times n}$, $h_x \in \mathbb{R}^q$, or
- ellipsoid $S = \{x \in \mathbb{R}^n \mid \|L(x - y)\|_2 \leq 1\}$ parameterized by $L \in \mathbb{R}^{n \times n}$ and $y \in \mathbb{R}^n$.

In a similar way, the bounds on operational ranges of control inputs can be expressed as:

- polytope $S_u = \{u \in U \mid H_u \cdot u \leq h_u\}$ parameterized by $H_u \in \mathbb{R}^{q \times p}$ and $h_u \in \mathbb{R}^q$, or
- ellipsoid $S_u = \{u \in U \mid \|L_u(u - \bar{u})\|_2 \leq 1\}$ parameterized by $L_u \in \mathbb{R}^{p \times p}$ and $\bar{u} \in U$.

The nonlinear control system $\Sigma$ is said to be safe if the states of the system remain inside $S$ using only the control commands in $S_u$.

3.4 Reachable Set

Consider a nonlinear control system as in Equation (1) and a set $X_0 \subset \mathbb{R}^n$. The reachable set of states that can be reached starting from set $X_0$ under input signal $v$ at time $\tau$ is given by $\text{Reach}_\tau(X_0, v) := \bigcup_{x \in X_0} \xi_{x,v}(\tau)$. We use notation $\text{Reach}_{[a, \tau]}(X_0, v)$ to denote the reachable set that can be reached starting from $X_0$ under input signal $v$ up to time $\tau$ and can be defined as $\text{Reach}_{[a, \tau]}(X_0, v) := \bigcup_{t \in [a, \tau]} \text{Reach}_t(X_0, v)$. We use the notation $\text{Reach}_\tau(X_0, v)$ to denote an over-approximation of the set $\text{Reach}_\tau(X_0, v)$.

4 DESIGN APPROACH

As depicted in Figure 1, the proposed design consists of three main components—Base Controller (BC), Mission Controller (MC), and Decision Module (DM).

The BC is a verified, reliable controller that is only concerned with safety. It does not make progress toward the mission set points of the system (i.e., it does not provide liveliness). The MC, on the other hand, is the main controller that is concerned with the mission-critical requirements. This controller may have complex logic, and can be changed and upgraded while the system is running.
and may even contain unsafe logic and bugs. As an example, MC may be a neural network resulted from machine learning techniques.

All the components of the system run on top of the RTOS. The length of one control cycle of the system is $\tau_c$. The $k$th control cycle refers to the period $[(k - 1)\tau_c, k\tau_c]$, where $k \in \mathbb{N}$. The cycles count and the time origin are restarted after every system restart. Therefore, $k = 1$ always refers to the first cycle after the latest system restart. Furthermore, we assume that the length of the restart time, i.e., $\tau_r$, of the system is an integer multiple of $\tau_c$ (i.e., $\tau_r = m\tau_c$, where $m \in \mathbb{N}$). While the system is running, sensor values are sampled at $t = k\tau_c - \epsilon$ where $\epsilon \ll \tau_c$, and actuator inputs are updated at $t = k\tau_c$.

In every control cycle, after MC runs and generates its output $u_{mc}$, DM evaluates the safety requirements under $u_{mc}$ and decides whether $u_{mc}$ can be applied to the actuators. Then, DM writes its output, along with the corresponding MC command and a timestamp (cycle number) to a fixed memory address.

At the end of the control cycle, at time $k\tau_c - \epsilon$ after sensors are sampled, BC runs and generates $u_{bc}$. Then, a flushing task retrieves $u_{mc}$, $u_{bc}$, the decision of DM, and the corresponding timestamp from the memory. If the timestamp matches with the current cycle number, $k$, it updates the actuator commands with $u_{mc}$ or $u_{bc}$ based on the decision of DM and resets watchdog timer (WD). Non-matching timestamps indicate that one or both of the DM and BC tasks did not execute or missed their deadlines. In such cases, the flushing task does not update the WD. Consequently, WD expires at $t = k\tau_c$ and triggers a restart. Note that as a result of this mechanism, restarts are only triggered at times $t = k\tau_c$ and do not occur in between control cycles. The steps are illustrated in Figure 2.

In the rest of this section, we discuss the assumptions and the fault model of the system. Then, we introduce the properties of the BC and how it is able to safely tolerate the restarts. Finally, we discuss the safe switching logic of the DM.

### 4.1 Assumptions and Fault Model

In this section, we clarify several assumptions we make about faults and components of the system.

- In this work, we are not concerned about hardware faults, and we assume that hardware is reliable.
- We assume a single-rate control system.

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3 It includes the time for reloading the bootloader, OS, and the applications from the read-only storage, initializing the necessary sensors and peripheral, booting the OS and executing the control applications.

4 Restart time can be rounded up to match the closest $k\tau_c$. 
— BC, DM, and flushing task are independently verified and fault-free. They might, however, fail silently (no output is generated) due to the faults in the previously dependent software layers or other applications.
— System-level and application-level faults may cause BC, DM, and flushing task to fail silently but may not change their logic or alter their output.
— Once a command is sent to an actuator input, the actuator holds that value until the control system sends a new actuation command. Therefore, during a system-level restart, the actuators operate with the last command that was sent before the restart occurred.5
— We assume that the system-level faults do not happen within the first \( \tau_r \) seconds after the boot is complete so that the BC has the chance to execute correctly at least once. In other words, this assumption implies that the system is not completely dysfunctional. In Section 4.2, we demonstrate the necessity of this assumption.

4.2 Properties of the Base Controller

In this section, we provide the properties required for the BC as follows:

There exists a subset \( \mathcal{I} \) of the state space, such that for all \( x \in \mathcal{I} \) at time \( t_0 \in \mathbb{R}_0^+ \), there exists a control command \( u_{bc} \in S_u \), such that:

(i) \( \xi_{x,u_{bc}}(t_0 + \tau_c) \in \mathcal{I} \),
(ii) \( \xi_{x,u_{bc}}(t_0 + \tau_c + \tau_r) \in \mathcal{I} \), and
(iii) \( \xi_{x,u_{bc}}(t) \in S \) for \( t \in [t_0, t_0 + \tau_c + \tau_r] \).

Here, we abuse the notation by identifying \( u_{bc} \) with the constant input curve taking value \( u_{bc} \in U \) as \( v(t) = u_{bc} \) for all \( t \in [t_0, p] \), where \( p \in \{\tau_c, \tau_c + \tau_r\} \). Note that, in the rest of the article, we assumed that the actuators hold the control input constant within the period of \( [t_0, t_0 + \tau_c + \tau_r] \).

Intuitively, above properties imply that if the current state of the system is inside \( \mathcal{I} \), BC is able to generate a control command that keeps the physical system safe. For the intuition, consider \( t_0 = k\tau_c \). Property (i) implies that one control cycle after \( u_{bc} \) is applied to the actuators, at the end of the \( (k+1) \)th cycle, state is inside \( \mathcal{I} \). Therefore, if the system is still running and no faults have occurred, BC is able to find another safe command at \( t = (k + 1)\tau_c \). If a fault had occurred within the \( (k+1) \)th cycle, a restart will be triggered at the end of the cycle and BC will not be able to update the actuator input. Property (ii) implies that in such a case, the system will be in \( \mathcal{I} \) after the restart completes. This guarantees that the system can be kept safe after the restart completes. Finally, property (iii) ensures that the system remains inside the safety region during the \( (k+1) \)th cycle and a possible consequent restart.

A BC with the above properties, without any other components, can keep the system safe, only if it updates the actuator commands at least once after every restart \( \tau_r \). Under our fault model, faults can occur at any point during the control cycle (except the first control cycle). As we discussed, the faults taking place in the control cycle will not violate system safety if the controller satisfies these three properties.

4.3 Switching Logic of DM

A system with only BC remains safe and tolerates restarts but it does not make any progress toward the mission goal. In order to maximize the progress toward the mission goal, it is desirable to use the MC command in every cycle whenever it is possible.

5Commercial chips such as Ref. [3] are available that provide programmable PWM controller. Using these intermediate chips, one can prevent the invalid signals that may appear on the general-purpose input/output (GPIO) port of the board during a restart, from changing the actuation command.
In every cycle $k$, DM runs and evaluates the following conditions. If those conditions hold, $u_{mc}$ is safe to be applied to the actuator inputs at the end of the cycle (i.e., at time $t = k\tau_c$). Otherwise, DM chooses $u_{bc}$. Following conditions guarantee that the system remains safe and recoverable under $u_{mc}$ whether it restarts or not.

(i) $\text{Reach}_{\tau_c}(\hat{x}[k], u_{mc}) \subseteq I$

(ii) $\text{Reach}_{\tau_r+\tau_c}(\hat{x}[k], u_{mc}) \subseteq I$

(iii) $\text{Reach}_{[0,\tau_r+\tau_c]}(\hat{x}[k], u_{mc}) \subseteq S$

Here, $\tau_r$ and $\tau_c$ are the length of the restart time and of the control cycle of the platform. Notation $\hat{x}[k]$ denotes the state of the system when the actuator command is going to be applied to the system (i.e., the end of the cycle at time $t = k\tau_c$).

From properties of the BC, it is known that if the state is inside $I$, BC can find a control command that keeps the system in safe and restartable region. Condition (i) ensures that once the control cycle after $u_{mc}$ is applied to the system the state will be inside $I$. If no faults occur within the control cycle, BC is guaranteed to be able to find a safe control for the system. However, if a fault occurs within the cycle, WD triggers a system restart at the end of the cycle. Condition (ii) ensures that the state will be inside $I$ when the restart completes (i.e., at $\tau_c + \tau_r$). Furthermore, condition (iii) guarantees that during the control cycle and restart time (if it happens), the state remains inside the safety region.

Note that in the real implementation, calculating reachable set and therefore evaluating these conditions requires time and does not happen instantaneously. Therefore, assuming $k$ is the current cycle, above conditions have to be assessed before $t = k\tau_c$. At this time, however, $x[k] = x(k\tau_c)$ (state of the system when the actuator command is going to be updated) is not available yet. To address this issue, above conditions use $\hat{x}[k]$, which is the over-approximated prediction of $x[k]$ based on $x[k-1]$ (sampled sensor values in the previous cycle). Prediction $\hat{x}[k]$ can be computed in the following way:

$$\hat{x}[k] = \text{Reach}_{\tau_c}(x[k-1], u_{k-1}),$$

where $x[k-1]$ is the sampled state at the previous cycle (state of the system at the beginning of the current control cycle). Input $u_{k-1}$ is the control command sent to the actuators in the previous cycle. Since, in the first control cycle after a restart, $u_{k-1}$ is not available, the DM always chooses the BC in the first cycle.

There are various algorithms available in the literature for over-approximating the reachable set, and one can use any suitable algorithm that meets the timing criteria used while designing controllers. For computing over-approximation of the reachable set, the real-time reachability algorithm is proposed in Ref. [12] for linear and a class of nonlinear dynamical systems (see Refs [4] and [5] for its applications). The authors in Refs [30, Section VIII.c], [8], and [9] provide other approaches for over-approximating the reachable set for nonlinear control systems. We kindly refer the interested readers to Ref. [22] for the comparison between state-of-the-art reachable set computation algorithms for nonlinear systems.

5 BASE CONTROLLER DESIGN

In this section, we provide a systematic approach to design base controllers ensuring properties mentioned in Section 4.2. To design BC, we use a symbolic controller synthesis approach, which uses the discrete abstractions of nonlinear physical systems [39]. The advantage of using this approach is that it provides an automated synthesis of formally verified controllers for high-level specifications (usually expressed as linear temporal logic (LTL) formulae [10]) for nonlinear control systems. Apart from the ability to handling nonlinear systems, it efficiently handles constraints on
state and input space and provides maximally permissible controllers. One can readily see that the properties given in Section 4.2 are equivalent to invariance specification in the sense of LTL.

5.1 Transition Systems and Equivalence Relation

We recall the notion of transition system introduced in Ref. [39], which will later be used as unified framework to represent nonlinear control systems and corresponding discrete abstractions.

**Definition 5.1 (Transition System).** A transition system is a tuple \( S = (X, X_0, U, \rightarrow) \) where \( X \) is a set of states, \( X_0 \subseteq X \) is a set of initial states, \( U \) is a set of inputs, and \( \rightarrow \subseteq X \times U \times X \) is a transition relation.

We denote by \( x \xrightarrow{u} x' \) an alternative representation for transition \((x, u, x') \in \rightarrow\), where state \( x' \) is called a \( u \)-successor (or simply successor) of state \( x \), for some input \( u \in U \). We denote by \( \text{Post}_u(x) \) the set of all \( u \)-successors of state \( x \), and by \( U(x) \) the set of all admissible inputs \( u \in U \) for which \( \text{Post}_u(x) \) is non-empty. Now, we provide the notion of feedback refinement relation between two transition systems, introduced in Ref. [30], which is later used to relate nonlinear control systems and their discrete abstractions and to construct base controllers for nonlinear control systems \( \Sigma \).

**Definition 5.2 (Feedback Refinement Relation).** Consider two transition systems \( S_1 = (X_1, X_{10}, U_1, \rightarrow) \) and \( S_2 = (X_2, X_{20}, U_2, \rightarrow) \) with \( U_2 \subseteq U_1 \). A strict relation \( Q \subseteq X_1 \times X_2 \) is a feedback refinement relation from \( S_1 \) to \( S_2 \) if the following conditions hold for every pair \((x_1, x_2) \in Q\):

1. \( U_2(x_2) \subseteq U_1(x_1) \),
2. \( u \in U_2(x_2) \Rightarrow \text{Post}_u(x_1) \subseteq \text{Post}_u(x_2) \),

and the feedback refinement relation from \( S_1 \) to \( S_2 \) is denoted by \( S_1 \leq_Q S_2 \).

Intuitively, the above relation says that all admissible inputs of \( S_2 \) can be used in transition system \( S_1 \) such that all transitions in \( S_1 \) are associated with corresponding transitions in \( S_2 \). As a result, one can easily refine controller synthesized for \( S_2 \) using feedback refinement relation \( Q \) to make it compatible for \( S_1 \). Further details about feedback refinement relation and its role in the controller synthesis can be found in Ref. [30].

5.2 Sampled-Data Control System as a Transition System

As we discussed in the previous sections, the sampling time can take any value in \( h = \{\tau_c, \tau_r + \tau_c\} \) depending on the occurrence of fault. We assume that the value of control input is held for the respective sampling period. The transition system associated with the nonlinear control system \( \Sigma \) with such a sampling behavior can be given by the tuple

\[
S_h(\Sigma) = (X_h, X_{h0}, U_h, \rightarrow_h),
\]

where

\[
X_h = \mathbb{R}^n, X_{h0} = \mathbb{R}^n, U_h = U, \text{ and } \quad -x \xrightarrow{u} x' \text{ is a transition if and only if there exists } x' = \xi_{x,u}(\tau_c) \text{ or } x' = \xi_{x,u}(\tau_r + \tau_c), \text{ where } u \in U_h.
\]

Note that we abuse notation above by identifying \( u \) with the constant input curve with domain \([0, \tau_c]\) or \([0, \tau_r + \tau_c]\) and value \( u \).

For the transition system \( S_h(\Sigma) \), the finite or infinite run generated from initial state \( x_0 \in X_{h0} \) is given by \( x_0 \xrightarrow{u_0} h x_1 \xrightarrow{u_1} h x_2 \xrightarrow{u_2} \ldots \) such that \( x_i \xrightarrow{u_i} h x_{i+1}' \), for \( i \in \mathbb{N}_0 \).
By considering properties of BC mentioned in Section 4.2, one can view it as a safety controller synthesis problem for $S_h(\Sigma)$.

Definition 5.3 (Safety Controller). Consider a safe set $S \subseteq \mathbb{R}^n$ as given in Section 3.3, a safety controller for $S_h(\Sigma)$ is given by a map $C_h : X_h \rightarrow 2^{U_h}$ such that

(i) for all $x \in X_h$, $C_h(x) \subseteq U_h(x)$,
(ii) its domain $\text{dom}(C_h) = \{x \in X_h | C_h \neq \emptyset\} \subseteq S$,
(iii) for all $x \in \text{dom}(C_h)$ and $u \in C_h(x)$, $\text{Post}_u(x) \subseteq \text{dom}(C_h)$.

Essentially, a safety controller generates infinite runs $x_0 \xrightarrow{u_0}_h x_1 \xrightarrow{u_1}_h x_2 \xrightarrow{u_2}_h \ldots$ such that $x_i \in S$, for all $i \in \mathbb{N}_0$. At the end of this section, we provide a systematic way to compute such controller for linear control systems. However, finding such a control strategy for complex nonlinear control systems is quite difficult. This motivates the use of abstraction-based synthesis methods described below.

5.3 Discrete Abstraction

To design controllers for the concrete system $S_h(\Sigma)$ from its abstraction, the system and its abstraction must satisfy formal behavioral inclusions in terms of feedback refinement relations. Consider sampling times $\tau_c, \tau_r + \tau_c \in \mathbb{R}^+$ and quantization parameter $\eta \in (\mathbb{R}^+)^n$. The discrete abstraction of $S_h(\Sigma)$ is given by the tuple

$$S_q(\Sigma) = (X_q, X_{q0}, U_q, \xrightarrow{\text{q}}),$$

where

$-X_q$ is a cover of $X_h$, and elements of the cover $X_q$ are nonempty, closed hyper-intervals referred to as cells. For computation of the abstraction, we consider subset $\overline{X}_q \subseteq X_q$ of congruent hyper-rectangles aligned on a uniform grid parameterized with quantization parameter $\eta \in (\mathbb{R}^+)^n$ and given by $\eta \mathbb{Z}^n = \{c \in \mathbb{R}^n | \exists k \in \mathbb{Z}^n \forall i \in \{1,2,\ldots,n\} c_i = k_i \eta_i\}$, i.e., $x_q \in \overline{X}_q$ implies that there exists $c \in \eta \mathbb{Z}^n$ with $x_q = c + \|\frac{\eta}{2} + \frac{\eta}{2}\|$. The remaining cells $X_q \setminus \overline{X}_q$ are considered as "overflow" symbols; see Ref. [29, Sec III.A]

$-X_{q0} \subseteq X_q$,

$-U_q$ is a finite subset of $U_h$,

$-x_q \in \overline{X}_q$ and $u \in U_q$,

define $A := \{x'_q \in X_q | (x'_q \cap \text{Reach}_{\tau_c}(x_q, u_q)) \cup (x'_q \cap \overline{\text{Reach}}_{\tau_r+\tau_c}(x_q, u_q)) \neq \emptyset\}$. If $A \subseteq \overline{X}_q$, then $\text{Post}_u(x_q) = A$; otherwise, $\text{Post}_u(x_q) = \emptyset$. Moreover, $\text{Post}_u(x_q) = \emptyset$ for all $x_q \in X_q \setminus \overline{X}_q$.

For the exact procedure to compute such discrete abstraction, we refer interested readers to Ref. [32].

Theorem 5.4. If $S_q(\Sigma)$ is a discrete abstraction of $S_h(\Sigma)$ with sampling times $\tau_c, \tau_r + \tau_c \in \mathbb{R}^+$, and quantization parameter $\eta \in (\mathbb{R}^+)^n$, then $S_h(\Sigma) \preceq Q S_q(\Sigma)$.

Proof. The proof is similar to the proof of Ref. [30, Theorem VIII.4].

The abstract safe set $\hat{S}$ for $S_q(\Sigma)$ is given by $\hat{S} := \{x_q \in \overline{X}_q | Q^{-1}(x_q) \subseteq S\}$.

5.4 Controller Synthesis and Refinement

In this section, we consider the problem of synthesis of safety controller $C_h$ for $S_h(\Sigma)$ and safe set $S$. Because of the feedback refinement relation, we can solve safety controller synthesis problem
for the discrete abstraction $S_q(\Sigma)$ and abstract safe set $\hat{S}$. Let $C_q : X_q \rightarrow U_q$ be the maximal safety controller satisfying conditions in Definition 5.3 for $S_q(\Sigma)$ and safe set $\hat{S}$. Since $S_q(\Sigma)$ has finite states and inputs, we can use standard maximal fixed-point computation algorithm [39] for the computation of $C_q$. One can easily refine this controller for $S_h(\Sigma)$ and safe set $\hat{S}$ using the following theorem:

**Theorem 5.5.** If $S_h(\Sigma) \leq S_q(\Sigma)$ and $C_q$ is the safety controller for $S_q(\Sigma)$ and $\hat{S}$, then the refined controller $C_h := C_q \circ Q$ solves the safety problem for $S_h(\Sigma)$ and $\hat{S}$.

**Proof.** The proof is similar to the proof of Ref. [30, Theorem VI.3]. □

Intuitively, the refined controller $C_h$ for $S_h$ can naturally be obtained from the abstract controller $C_q$ by using the feedback refinement relation $Q$ as a quantizer to map $x_h$ to $x_q \in Q(x_h)$.

**Remark 5.6.** The above framework also allows us to synthesize base controllers that are robust with respect to various disturbances including plant uncertainties, input disturbances, and measurement errors. For a detailed discussion regarding minor changes required while computing transitions in discrete abstractions, we kindly refer readers to Ref. [30, Section VI.B].

**Remark 5.7.** The obtained controller $C_h$ solves the safety problem for the sampled system, i.e., the obtained base controller satisfies the first two properties mentioned in Section 4.2 with invariant set $\mathcal{I} = \text{dom}(C_h)$. However, one can ensure safety guarantee of inter-sampling trajectory (i.e., third property in Section 4.2) by shrinking the safe set by a magnitude computed using the global Lipschitz continuity property of map $f$.

Despite the applicability of the proposed approach for complex and nonlinear control systems, it suffers from the curse of dimensionality, i.e., the computational complexity increases exponentially with state-space dimensions of concrete systems. There are few results available to address this issue for some class of nonlinear control systems [42, 43]. In the next section, we provide an alternative approach to compute invariant set $\mathcal{I}$ and BC for linear control systems.

### 5.5 Base Controller for Linear Control Systems

In this section, we provide an algorithm to compute $\mathcal{I}$ using discretized linear-control systems. The continuous linear control system can be converted to a discrete control system with the sampling time of $\tau_c$ as:

$$\dot{x}(t) = Ax(t) + Bu(t) \rightarrow x[k + 1] = A_d x[k] + B_d u[k],$$

where $A_d = e^{At_c} = \sum_{k=0}^{\infty} \frac{1}{k!} (A t_c)^k \simeq \sum_{k=0}^{p} \frac{1}{k!} (A t_c)^k$, and $B_d = (\int_0^\tau e^{At} \, dt) \cdot B$.

In this section, we show how to construct a BC with the properties: $\forall x[k] \in \mathcal{I}, \exists u_0, u[p] = u_0, p \in \{k, k+1, \ldots, k+m\}$ such that (i) $x[k+1] \in \mathcal{I}$ and (ii) $x[k+1+m] \in \mathcal{I}$, where $m = \tau_r / \tau_c$ and $m \in \mathbb{N}$. However, these properties do not guarantee that the inter-sample behavior is in the safe region. To address this issue we need to readjust the safe region. For the systematic procedure to compute readjusted safe region $\mathcal{S}' \subseteq \mathcal{S}$, we refer the interested reader to Ref. [7, Section 5.1].

**5.5.1 Finding the Invariant Subset $\mathcal{I}$.** To compute the set $\mathcal{I}$, we closely follow the usual construction method based on backward reachable sets to compute the largest invariant set for linear discrete-time systems (see, e.g., in Ref. [13]). We slightly modify this procedure and present it in Algorithm 1 to compute the subset $\mathcal{I} \subseteq \mathcal{S}'$, such that for the discrete-time system in Equation (4), $\mathcal{I}$ satisfies the properties in Section 4.2.
In this algorithm, matrix $H^q_x$ and vector $h^d_q$ represent the adjusted safety region $S'$ as a polytope (cf. Section 3.3), and matrix $H^I_x$ and vector $h^I_x$ represent $I$ as a polytope. Matrix $H_u$ and vector $h_u$ also represent a polytope for operational ranges of control inputs. $A_d^{(m+1)}$ and $B_d^{(m+1)}$ are the matrices to find the state after $m + 1$ cycles, i.e., $x[k + m + 1] = A_d^{(m+1)} x[k] + B_d^{(m+1)} u[k]$, where $m = \tau_r/\tau_c$. We have $A_d^{(m+1)} = (A_d)^{m+1}$ and $B_d^{(m+1)} = (A_d^m + A_d^{m-1} + \cdots + I)B_d$.

Intuitively, this algorithm starts from $S'$ as initial region (line 2). In every iteration of this algorithm, this region is augmented in the extended state-control space $\mathbb{R}^{n+m}$ (line 5). This linear inequality is then projected back into the state space (line 6). The outcome of lines 5 and 6 is to calculate $I^{(p+1)}$, which is a subset of $I^{(p)}$ where a control value in $S_u$ exists such that, the state in one cycle and $m + 1$ cycle after are inside $I^{(p)}$.

The algorithm proceeds until either $I^{(p)} \subseteq I^{(p+1)}$ or $I^{(p+1)} = 0$. In the former case, procedure successfully ends (lines 7 to 8). The latter case indicates that the dynamics of the system do not allow such a region for the given restart time. There are cases in which the procedure does not terminate in a finite number of steps unless a finite $p_{\text{max}}$ is fixed. This may happen if $I^{(\infty)}$ has an empty interior, but it is not empty [13].

If matrix $A_d$ and $B_d$ are controllable, we can use ideas from Ref. [31] to ensure convergence. However, in general, we cannot guarantee that the procedure in Algorithm 1 will converge to a non-empty $I$. In such cases, one may have to loosen the safety constraints of the system (i.e., $S$) or may have to switch to a hardware platform with a shorter restart time to be able to apply this approach.

5.5.2 Base Controller in Runtime. Using invariant set $I$ computed as given in Section 5.5.1, one can compute a control input $u[k]$ at the $k$th sampling instance that satisfies the following
conditions:

\[
H_u \cdot u[k] \leq h_u,
\]
\[
H^T_s \cdot x[k + 1] \leq h^T_s,
\]
\[
H^T_s \cdot x[k + m + 1] \leq h^T_s.
\] (5)

By substituting \(x[k + 1]\) and \(x[k + m + 1]\), we get the following linear matrix inequalities:

\[
H_u u[k] \leq h_u,
\]
\[
H^T_s B_d u[k] \leq h^T_s - H^T_s A_d x[k],
\]
\[
H^T_s B_d^{(m+1)} u[k] \leq h^T_s - H^T_s A_d^{(m+1)} x[k].
\] (6)

At runtime, BC receives the sensors values, i.e., \(x[k]\), and calculates \(u[k]\) by solving these inequalities.

6 CASE STUDY AND EVALUATION

To demonstrate the practicality of the proposed approach, we implemented a controller for two benchmark systems: (i) inverted pendulum system and (ii) 3-DOF helicopter \([24]\) and empirically verify fault-tolerance guarantees. We utilize one COTS platform to implement our controller. We inject faults in the control logic, control application, and the operating system to demonstrate that the system remains safe, despite the faults, and recovers.

6.1 Experimental Setup

For the prototype of the proposed design, an i.MX7D application processor is used. This SoC provides two general purpose ARM Cortex-A7 cores capable of running at the maximum frequency of 1 GHz and one real-time ARM Cortex-M4 core that runs at the maximum frequency of 200 MHz. The real-time core runs from tightly coupled memory to ensure predictable behavior required for the real-time applications/tasks. The real-time core of the considered platform runs FreeRTOS \([2]\), an operating system for real-time applications. Because our control tasks have real-time constraints, we implement our controller on the real-time core. Ideally, the general purpose cores would have been completely disabled for the experiments. However, in i.MX7D platform, only Cortex-A7 cores have direct access to the flash memory, and only these two cores can load the binary images of the real-time core from flash into the real-time core’s memory after each restart. Hence, instead of permanently disabling those cores, they are only disabled after the software of the real-time core is loaded from flash into the memory. Note that this mechanism is specific to this particular platform and does not impact the generality of our proposed technique.

The manufacturer’s boot procedure of the board is designed to boot the general purpose cores and the real-time core at the same time. It includes extra initialization procedures that are necessary only for running the general purpose core’s kernel and mounting its file system. It loads the real-time core code only after those procedures are completed.

To reduce the boot time of the real-time core, we made two modifications to the bootloader (u-boot) source code, which can be found in Ref. \([1]\). (i) We included the binary of the real-time core executables (FreeRTOS, MC, BC, DM, and flushing task) as a static array in the u-boot source code and made it part of the u-boot binary after compilation. (ii) In our modified boot process, at the boot time, the general purpose processor copies u-boot binary (which includes the FreeRTOS and application binaries) from the SD-card into the RAM. After successful initialization of only the necessary peripherals and configuring the clock by the u-boot procedures, u-boot loads the binaries.
of the real-time core in its tightly coupled memory and releases it from reset. These modifications reduce the real-time core’s boot time from seconds to less than 250ms.\footnote{BC task activates one of the GPIO pins immediately after it executes. The restart time is measured externally using the signal on this pin. After multiple experiments, a conservative upper bound was picked for the restart time.}

### 6.2 Example 1: Inverted Pendulum

For the first case study, we consider a nonlinear inverted pendulum system [29] given by nonlinear differential equations as:

\[
\begin{align*}
\dot{\xi}_1(t) &= \xi_2(t) \\
\dot{\xi}_2(t) &= -\omega^2 \left( \sin(\xi_1(t)) + \cos(\xi_1(t))u(t) \right) - 2\gamma \xi_1(t),
\end{align*}
\]

with parameters $\omega = 1$ and $\gamma = 0.0125$. The states $\xi_1$ and $\xi_2$ are the angular position with respect to a downward vertical axis and the angular velocity of the pendulum, respectively. The control input $u(t)$ is restricted to $[-4, 4]$. We design MC as $u_{mc} = 2(\pi - \xi_1 - \xi_2)$ to stabilize the pendulum at upright position that is $\xi = [\pi, 0]^T$, which runs with frequency of 20Hz (i.e., $\tau_c = 50$ms) on real-time core of i.MX7D. To ensure safety of the system (i.e., to avoid pendulum to fall down), we consider safety region for the states given by a polytope parameterized by:

\[
H_x = \begin{bmatrix}
-1 & 0 \\
1 & 0 \\
0 & -1 \\
0 & 1
\end{bmatrix}
\quad \text{and} \quad
h_x = \begin{bmatrix}
-0.75\pi \\
1.25\pi \\
1 \\
1
\end{bmatrix}.
\]

To ensure fault-tolerance and safety during restart, we designed BC using abstraction-based approach as discussed in Section 5. To synthesize BC, we first constructed a discrete abstraction of the pendulum system in Equation (7) using quantization parameter $\eta = [0.05, 0.1]^T$, sampling time $\tau_c = 0.050$, and restart time $\tau_r = 0.250$. Further, we synthesize a safety controller using maximal fixed point computation algorithm. For the controller synthesis, we used toolbox SCOTS [32] with some modifications to adapt the construction of abstraction given in Section 5.3. The invariant states computed using the proposed approach is shown in Figure 3. To verify the efficacy of the designed controller, we implemented it on our experimental setup (i.MX7D) and tested in...
the closed-loop with inverted pendulum dynamics simulated in the computer under various test scenarios discussed in Section 6.4.

6.3 Example 2: 3-DOF Helicopter

3-DOF helicopter (displayed in Figure 4) is a simplified helicopter model, ideally suited to test intermediate to advanced control concepts and theories relevant to real-world applications of flight dynamics and control in the tandem rotor helicopters, or any device with similar dynamics [24]. It is equipped with two motors that can generate force in the upward and downward direction, according to the given actuation voltage. It also has three sensors to measure elevation, pitch, and travel angle as shown in Figure 4. We use the linear model of this system obtained from the manufacturer manual [24]. The BC is designed as discussed in Section 5.5.

For 3-DOF helicopter, the safety region is defined in such a way that the helicopter fans do not hit the surface underneath, as shown in Figure 4, while respecting the maximum angular velocities. The six dimensional state vector is given by $x = [\epsilon, \rho, \lambda, \dot{\epsilon}, \dot{\rho}, \dot{\lambda}]^T$, where variables $\epsilon$, $\rho$, and $\lambda$ are the elevation, pitch, and travel angles, respectively; $\dot{\epsilon}$, $\dot{\rho}$, and $\dot{\lambda}$ are the corresponding angular velocities. The $u = [v_l, v_r]^T$ represents input vector, where $v_l$ and $v_r$ are the voltages applied to right and left motors. The safe region for the state and input spaces are represented using polytopes as discussed in Section 3.3 and parametrized with

$$H_x = \begin{bmatrix} -1 & -0.33 & 0 & 0 & 0 & 0 \\ -1 & 0.33 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & -1 & 0 \end{bmatrix}, \quad h_x = \begin{bmatrix} 0.3 \\ 0.3 \\ 0.4 \\ 0.4 \\ 1.5 \\ 1.5 \end{bmatrix}, \quad H_u = \begin{bmatrix} -1 & 0 \\ -1 & 0 \\ 0 & 1 \\ 0 & -1 \end{bmatrix}, \quad \text{and} \quad h_u = \begin{bmatrix} 1.1 \\ 1.1 \end{bmatrix}.$$ 

FreeRTOS on the Cortex-M4 core restarts in 250 ms (upper bound). By using the algorithm in Ref. [7, Section 5.1], we computed readjusted safety constraint parameters as $h_x^a = [0.1418, 0.1418, 0.2828, 0.2828, 0.0825, 0.0825]^T$ and $H_x^a = H_x$. Using these readjusted safety constraints, the invariant region and BC are constructed using the Algorithms described in Sections 5.5.1 and 5.5.2. Algorithm 1 computed a region $\mathcal{I}$ confined with 106 inequalities after 14 iterations. The offline computation took 4 hours on Mac Book Pro with 2.5 GHz Intel Core i7 and 16 GB of memory. Finally, the BC is derived by solving linear inequalities in Equation (6).

6.3.1 Hardware Interface. The control tasks on the real-time core of i.MX7D run with a frequency of 20 Hz ($\tau_c = 50$ ms). Our controller interfaces with the 3DOF helicopter through a Peripheral Component Interconnect (PCIe)-based Q8 High-Performance H.I.L. Control and data acquisition unit [25] and an intermediate Linux-based PC. The PC communicates with the i.MX7D through the serial port. At the end of every control cycle, a flushing task on the real-time core communicates
Fig. 5. Simulated trajectory of the system under \( v_r = 0.6863 \) and \( v_l = 0.7709 \) is inside \( I \) (red region) at times \( \tau_c = 50 \text{ ms} \) (blue mark) and \( \tau_c + \tau_r = 300 \text{ ms} \) (green mark). White circles mark the beginning of the trajectory. The trajectory is projected into the four planes for clarity.

![Simulation trajectory](image)

Table 1. Our Approach Tolerates System-Level Faults Using Only One Hardware Unit

| Failure Type          | Fault Category       | Safety Application-Level Simplex (Single HW Board/SoC) | Safety System-Level Simplex (Additional HW/SoC) | Safety Our Approach (Single HW Board/SoC) | Restarted |
|-----------------------|----------------------|-------------------------------------------------------|-----------------------------------------------|------------------------------------------|-----------|
| No Output             | App.                 | ✔                                                     | ✔                                             | ✔                                         | No        |
| Maximum Voltage       | App.                 | ✔                                                     | ✔                                             | ✔                                         | No        |
| Time Degraded Control | App.                 | ✔                                                     | ✔                                             | ✔                                         | No        |
| Timing Fault—CPU      | RTOS/App.            | ✗                                                     | ✔                                             | ✔                                         | Yes       |
| Timing Fault—Resource | RTOS/App.            | ✗                                                     | ✔                                             | ✔                                         | Yes       |
| FreeRTOS Freeze       | RTOS                 | ✗                                                     | ✔                                             | ✔                                         | Yes       |
| Computer Reboot       | RTOS                 | ✗                                                     | ✔                                             | ✔                                         | Yes       |

Whereas, System-Level Simplex \cite{11} needs an extra board/SoC to tolerate these faults.

with the PC to receive the sensor readings (elevation, pitch, and travel angles) and send the motors’ voltages. It also updates the hardware WD of the platform after sending the motor voltages. The PC uses a custom driver written for Linux to send the voltages to the 3DOF helicopter motors and reads the sensor values.

6.3.2 Testing the Base Controller. To verify that the constructed base controller has the desired properties, we simulated the system with this controller from all vertices of region \( \bar{I} \) as starting points and observed that the system’s state at \( \tau_c \) and \( \tau_c + \tau_r \) time units after actuation was inside \( \bar{I} \). Figure 5 outlines one extreme example. The trajectory starts at \( \epsilon = -0.1410, \rho = 0, \dot{\epsilon} = -0.0281, \) and \( \dot{\rho} = 0.0513 \) (\( \lambda \) and \( \dot{\lambda} \) do not impact safety). The control command in this trajectory is \( v_r = 0.6863 \) and \( v_l = 0.7709 \). As shown in Figure 5, the trajectory remains inside the safety region.

Further, we implemented the obtained BC on the i.MX7D platform to validate our design approach under different fault scenarios given in the next section.

6.4 Fault Injection

In Table 1, a list of faults that were tested on the implementations are provided. We also compare them with Application-Level Simplex and System-Level Simplex. For the application-level faults, we verified that the mission controller was able to actuate the system as long as it did not jeopardize the safety, and when the system states approached the states where the safety conditions violated, BC took over and ensured safety. For the system-level faults, we observed that the WD restarted the system and after restart, the system continued its operation.

Some of these faults are elaborated in the rest of this section.
6.4.1 Maximum Control Input in Wrong Way. The system should not leave the safe region even if the MC outputs a control input that normally would result in a crash. We consider an extreme case of this scenario where the MC generates a control input that forces the system toward the unsafe region. The unsafe MC commands were detected by DM (they did not satisfy the system safety conditions), and the control was switched to the BC until the system was in the safety region and then control was handed back to MC.

6.4.2 Timing Faults (CPU and Resource). The proposed solution also protects the system from timing faults. A faulty task may behave differently in runtime from its expected/reported behavior. For instance, it may lock a particular resource used by other critical tasks for more than the intended duration. Or, it may run for more time than its reported worst-case execution time (WCET), which was used for the schedulability test of the system. Timing faults may also originate from RTOS or driver misbehaviors. If the fault delays/stopss the execution of the DM or BC, WD will trigger a system-wide restart. This recovers the system from the fault and keeps the physical system safe. We perform two experiments to test the fault-tolerance against timing faults.

In the first experiment, we run an additional task on the system that uses the serial port in parallel to the flushing task to communicate with the PC. We inject a fault into this task so that in random execution cycles, it holds the lock on the serial port for more than its intended period. This prevents the flushing task from updating the actuator (which needs the serial port) before the end of the control cycle. As a result, WD expires and restarts the system. We verified that the system recovers from the fault and remains safe during the restart.

In the second test, we introduce a task that runs at the same priority as the BC and DM. We inject a fault into the task such that in some cycles, its execution time exceeds its reported WCET. FreeRTOS runs the tasks with equal priority using round-robin scheduling with a context switch at every 1ms. Therefore, the faulty task delays the response time of the DM and BC. If the interference is too long, the output of BC may not be ready by the time the flushing task needs to update the actuators. When this happens, WD restarts the system.

7 DISCUSSION

Some limitations need to be considered before deploying proposed restart-based design to a physical plant or platform.

Restart Time: As the restart time of the platform increases, the domain of the BC shrinks. Therefore, the proposed solution in its current form may not suit some platforms with a longer restart time. However, many embedded systems have reboot times that range from tens of milliseconds to tens of seconds [27], which are considered non-significant for many real-time embedded applications (such as temperature/humidity management in storage/transportation industries, process control in chemical plants, and pressure control in water distribution systems).

High-speed Dynamics: The physical plants with high-speed dynamics may require very frequent restarts and will significantly reduce the control performance and the progress of the system. Frequent reboots may also pose implementation challenges.

Software Faults: The proposed approach does not handle software faults that modify the program logic or output of the BC and the DM at the execution time. Utilizing frameworks such as ARM TrustZone [23] and limiting access to these critical components can mitigate this issue. The proposed approach will also not withstand for any fault that lasts for the duration of system restart and the one that prevents the system from operating correctly for at least one cycle after the restart (e.g., permanent software fault).
Memory-less Controller: Due to the loss of the past state information after full system restart, the proposed restart-based approach is only suitable for the use of memory-less controllers BC and MC, where the control action is generated based on the current state of the plant.

The proposed restart-based implementation is most suitable for the CPS applications where the platform restart time is smaller than the speed of the plant dynamics. The proposed implementation provides an efficient solution to achieve fault-tolerance in less critical applications where cost is a bigger factor along with the safety requirements.

It is worth mentioning that rejuvenation-based solutions do not come with any guarantees and only improve the probability of success. Here is where the major value of our approach is added because, with the addition of minimal hardware (a timer), the same system can provide strong guarantees on the safety conditions. There are applications where a probabilistic solution would not be good enough. A potential area that could benefit from this architecture is medical devices where ultra-reliability is extremely important, and the physical systems do not have super fast dynamics. We can take a medical ventilator as an example. A medical ventilator is a machine designed to provide mechanical ventilation by moving breathable air into and out of the lungs, to deliver breaths to a patient who is physically unable to breathe or breathing insufficiently. In order to keep the patient safe, the oxygen level needs to stay higher than a threshold. Our body has a very low tolerance to lack of oxygen. Generally speaking, injuries begin at the one-minute mark, steadily worsening. Between 30–180 seconds of oxygen deprivation, one may lose consciousness. At the 1-minute mark, brain cells begin dying. Instead of adding a second back-up system to kick in when the original system fails, one could incorporate our design to ensure that the potential faults in the system would not lead to catastrophic fatalities.

8 CONCLUSION

Restarting is considered as a reliable way to recover the traditional computing system from software faults. However, restarting safety-critical CPS is challenging. In this work, we propose a novel approach that guarantees safety and liveness of nonlinear physical systems in the presence of application and system-level software faults, utilizing only one COTS processor based on complete system-level restarts.

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