Structured scale-dependence in the Lyapunov exponent of a Boolean chaotic map

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We report the experimental observations of microscopic discontinuities in a one-dimensional chaotic return map based on structures in a scale-dependent Lyapunov exponent. The chaos is realized in an autonomous Boolean network which is constructed using asynchronous logic gates to form a map operator that outputs an unclocked pulse-train of varying widths. The map operator executes pulse-width stretching and folding and the operator’s output is fed back to its input to continuously iterate the map. Using a simple model, we show that the structured scale-dependence in the system’s Lyapunov exponent is the result of the discrete logic elements in the map operator’s stretching function.

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Understanding the distinct roles of noise and determinism is important for all experimental chaotic systems. We examine a scale-dependent Lyapunov exponent (SDLE) of a Boolean chaotic system that iterates the dynamics a one-dimensional (1D) map. A SDLE was studied previously as a way to distinguish the entropy of microscopic noise from the entropy of macroscopic chaos [13]. This distinction is of increasing importance as physical random number generators that use chaotic systems as entropy sources continue to be developed [4–8]. Our experiment iterates a macroscopic tent map with microscopic discontinuities that are blurred by the noise of the system. Here, we demonstrate that scaling of these discontinuities manifests as a structured scale-dependence in the Lyapunov exponent of our Boolean chaotic system.

Boolean chaos is a term used to describe the phenomenon of deterministic dynamics in unclocked Boolean networks with an exponential divergence of neighboring trajectories. Originally, theories of continuous, ideal Boolean networks predicted non-repeating switching in certain networks, but without chaos [9]. Contrary to this prediction, recent experiments showed that physical logic gates can introduce non-ideal effects that give rise to chaos [10]. Boolean chaos has been reported in both autonomous and driven networks [6,11], both of which yield complex, multi-dimensional dynamics. One-dimensional (1D) Boolean chaotic maps were theorized for specific non-ideal effects [12]. Here, we examine the first experimental 1D Boolean chaotic map and report its unique, multi-scaled features.

Our experimental setup is influenced by recent studies of non-chaotic autonomous Boolean systems. In particular, asynchronous networks of logic gates were studied as excitable systems with synchronization patterns [13,14] and phase oscillators with chimera states [15,16]. One appealing feature of these Boolean systems is that they can be implemented entirely on a field-programmable gate array (FPGA), a common component in modern electronics. This platform allows for large dynamical networks of asynchronous logic gates to easily be built [8,13–16]. The implementation of our experiment is also facilitated by an FPGA, where we note that our system is not a simulation on a finite-state-machine (see [17] and references therein); it is an unclocked system with non-zero entropy and a potential continuum of dynamical states that are subject to analog effects and experimental noise.

Our experimental system is shown in Fig. 1, which is initialized by an input voltage pulse of initial pulse-width $w_0$. This pulse drives a map operator $M$ which consists of two separate functions: a pulse-width folding-function $f$ and a pulse-width gain-function $g$ that approximately doubles a pulse’s width (details provided later), where this combination of folding and stretching are sufficient conditions to see chaos [18]. The output voltage of $M$ is labeled as $v_{out}$, and a delay line routes $v_{out}$ back to the input of $M$, where the delay is long enough to ensure

\[ P(A) = \frac{\text{Probability of state } A}{\text{Total probability}} \]

FIG. 1. (a) Experimental system with operator $M$, initial pulse of width $w_0$ injected via OR gate, input voltage $v_{in}$, auxiliary voltage $v_a$, output voltage $v_{out}$, and feedback loop of delay $\tau_N \sim 60$ ns (realized using a $N = 200$ NOT gates) on an Altera Cyclone IV (EP4CE115F29C7N) using $\sim 1\%$ FPGA resources. (b)-(c) $v_{out}$ from $w_0 = 16$ ns. (d) $w_i$ as a function of iteration $i$. (e) Return map ($w_i, w_{i+1}$) with dashed line of slope 1 and normalized histogram of states showing the probability distribution function (pdf) of $w_i$. 

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only one pulse is in this feedback loop at a time. We note that this is a time-delay system with an infinite dimensional phase space, but neighboring pulses do not interact, allowing for 1D dynamics. This system remains in a stable steady state $v_{out} = 0 \text{ V}$ until we inject a pulse, and thus $w_0$ serves as its initial condition.

After an initial pulse is injected, the system produces a self-sustaining pulse-train. In Figs. 1a-c, we plot the temporal evolution of $v_{out}$, which contains pulses that occur with non-repeating pulse-widths $w_i$ and non-repeating spacings $y_i$. Thus, the transition times in $v_{out}$ are the state variables of the chaos. This is different from analog chaotic circuits that iterate 1D maps in discrete or continuous time and use voltage or current as the state variables [19, 20]. The power spectral density of $v_{out}$ (not shown) is broadband with prominent frequency components at integer multiples of $1/T \sim 13 \text{ MHz}$, where $T = \bar{w} + \bar{y} \sim 76 \text{ ns}$ is the average pulse-repetition period and can be adjusted with the feedback delay.

To analyze the dynamics, we study $w_i$, which is plotted in Fig. 1d; as we will show later, $y_i$ is a function of $w_i$ and contains no new information about the dynamics. We construct the return map using $(w_i, w_{i+1})$ in Fig. 1d, which shows a 1D structure similar to a tent map [18]. Figure 1e also shows that the density of the return map is non-uniform, which differs from an ideal tent map.

We fit Fig. 1e using a piecewise-linear function

$$f(w_i) = w_{i+1} \sim \begin{cases} mw_i, & w_i \leq \tau_n \\ m(2\tau_n - w_i), & \tau_n < w_i \leq 2\tau_n \end{cases}$$

where $m$ is the average slope and $\tau_n$ is the folding point. The fit yields $m_{fit} = 1.95 \pm 0.01$ and $\tau_{n, fit} = 11.7 \pm 0.01 \text{ ns}$, which shows that the map is not a tent-map of full height. We note that a tent map of full height in the experimental Boolean implementation can only show transient chaos before collapsing to the steady state $v_{out} = 0 \text{ V}$ due to short-pulses rejection (SPR) by the physical logic gates [10]. The slope $m = 1.95$ limits the grammar of the map and prevents pulse widths $w_i \lesssim 1 \text{ ns}$, allowing for non-transient chaos.

Interestingly, we might approximate the Lyapunov exponent $\lambda$ using $m_{fit}$ such that $\lambda \sim \ln(1.95)/T$ [18]. However, using this fit of the return map to estimate $\lambda$ assumes a continuous map. As we will discuss later, the discrete logic gates in the system’s design create discontinuities in the output of the operator $M$. To avoid assumptions about the experimental system, we instead compute a SDLE from $w_i$.

We define a SDLE as the divergence of neighboring trajectories, where neighbors $(w_i, w_j)$ satisfy $\epsilon < |w_i - w_j| < \epsilon + \Delta \epsilon$. An example of neighboring $(w_i, w_j)$ is shown in Fig. 2a. To calculate $\lambda(\epsilon)$, we average the separation of $(w_i, w_j)$ over neighboring trajectories for a given $\epsilon$. An example is shown in Fig. 2b, where a linear fit of the local divergence shows $\lambda(\epsilon)/T \sim 0.7$. The calculated $\lambda(\epsilon)$ for a scan of $\epsilon$ in 10 ps steps is shown in Fig. 2. In the figure, we use a scaling reference of $\tau_1$, which is the approximate delay time through a single logic element. We note that $\lambda(\epsilon)/T > 0$ is an indicator of trajectory separation at an exponential rate.

Figure 2[b] demonstrates that the experimental system exhibits exponential separation from both noise and chaos. Neighboring points on the return map with $d_o < \tau_1$ have an initial separation that is dominated by noise, while for $d_o > \tau_1$ the SDLE shows oscillations in the divergence rate at frequency $\sim 1/(2\tau_1)$ near $\lambda(\epsilon)/T \sim \ln(2)$ (the value of the Lyapunov exponent for a continuous tent-map of the full height). Thus, the rate of divergence shows a structured scale-dependence about a global rate that is described by the macroscopic features of the return map. Understanding this phenomenon is important for exploiting/avoiding scale-dependent entropy sources.

In the remainder of this paper, we briefly outline the design of Fig. 1a and examine the map operator’s functions to motivate a simple model that exhibits a similarly structured SDLE.

Our experimental system exploits the propagation delays of pulses as they transmit through logic gates. In the simplest example, the feedback loop $\tau_N$ in Fig. 1 is acts as a continuous delay line that routes pulses from the output of the map operator back to its input. This delay line is constructed using cascaded NOT gates [13], where even numbers of NOT gates are used to reduce asymmetries between rise and fall times of pulse edges that propagate [10] and preserve pulse widths. The number of NOT gates $n$ sets the propagation delay $\tau_n$.

In the map operator, a folding function $f$ is implemented with the circuit in Fig. 3a. In the figure, $v_{in}$ and $v_o$ are signals for input pulses of width $w_{in}$ and output pulses of width $w_{out}$, respectively, such that $w_o \sim w_{in}$ for $w_{in} \leq \tau_0$ and $w_o \sim (2\tau_0 - w_{in})$ for $\tau_0 < w_{in} \leq 2\tau_0$. To illustrate this circuit’s folding, in Fig. 3b we plot experimental examples of $(v_{in}, v_o)$ of the folding circuit, and in Fig. 3c, we scan $w_{in}$ and plot the respective $w_o$. We model $w_o = f(w_{in})$ from Eq. 1 with $m = 1$, and we...
We note \( f(w_{in}) \) does not address \( y_i \), but based on the folding circuit’s operation, we derive \( y_i = \tau_N + \tau_n - w_i \) for \( w_i \leq \tau_n \) and \( y_i = \tau_N \) otherwise.

The pulse-width gain function \( g \) of the map operator is shown Fig. 4(a). In the figure, an input pulse \( v_{in} \) is launched into a delay line of NOT gates, where AND gates compare the outputs of \( (k, 2k) \), where \( k \) is the index number of \( K \) total NOT gates such that \( 2k_{\text{max}} = K \). The AND-gate outputs drive a multi-input OR-gate, which outputs a pulse \( v_{out} \) of width \( w_{out} \) for \( \tau_K > w_{out} \), where \( \tau_K \) is the delay through \( K \) gates. To illustrate the pulse-width gain from this circuit, we plot examples of \( (v_{in}, v_{out}) \) and a scan of \( (w_{in}, w_{out}) \) in Figs. 4(b)-c, respectively. The resulting waveforms show approximate pulse-width doubling and the characterization of \( (w_{in}, w_{out}) \) has average slope \( \sim 2 \).

However, the discrete nature of the AND-gate comparisons of the delay line in Fig. 4(a) creates regularly-spaced, small-scale discontinuities that are not resolved in Fig. 4(a). Due to noise. Based on these discrete comparisons, we model the pulse-width gain as

\[
w_{out} = g(w_{in}) \sim 2 \tau_1 [w_{in}/\tau_1] + h(w_{in} - \tau_1 [w_{in}/\tau_1]),
\]

where \( \tau_1 [w_{in}/\tau_1] \) is a measure of \( w_{in} \) in single gate-delays, and \( h \) is a function that describes the width of an output pulse for a single gate. As \( w_{in} \) increases in Eq. \( 2 \), \( g \) is discontinuous and increases by steps of \( \tau_1 \). We define \( h(0) = 0 \) such that, when \( w_{in} \) is an integer multiple of \( \tau_1 \) \( (w_{in} - \tau_1 [w_{in}/\tau_1] = 0) \), the pulse-width gain is exactly 2. When \( w_{in} \) is not an integer multiple of \( \tau_1 \) \( h \) provides a corrective term that describes the continuous growth of pulse widths, where the input to \( h \) resets at each multiple of \( \tau_1 \). Thus, the function \( g \) has an average slope \( \sim 2 \) with discontinuities spaced regularly by \( \tau_1 \) and local slope(s) \( h'(w_{in}) \) in between each discontinuity.

For simplicity, we let \( h(w_{in}) = w_{in} \) such that the map \( w_{i+1} = M(w_i) = g(f(w_i)) \) is an example of a piecewise-linear system that exhibits noise-induced chaos. Noise-induced chaos occurs in chaotic systems that only show periodic or steady state dynamics without the presence of noise [1]. Similar models with fine-scaled discontinuities have been previously studied with the use of a SDLE, where with enough noise, these simulated chaotic maps exhibit characteristics of their macroscopic map structures [2]. A different choice for \( h \), such as a nonlinear function, can yield chaos without noise, but we choose the simplest model with noise to demonstrate the experimental observations. Noise in the FPGA causes jitter in \( w_{in} \), where we measure the jitter to be approximately Gaussian with standard deviation (STD) \( \sigma \sim 90 \) ps. We simulate the map \( w_{i+1} = M(w_i) \) using Eqs. \( 2 \) with \( m = 1, \tau_n = 12 \) ns, \( \tau_1 = 0.3 \) ns, and additive white-Gaussian-noise at every iteration (STD = \( \sigma \)).

The simulated return map is shown in Fig. 4(a) with a 1D structure similar to a tent map with slopes \( \sim \pm 2 \). The probability density of the map is also non-uniform, where clustering occurs at evenly-spaced intervals. This differs from the experimental density because, in the model, we can guarantee that \( \tau_n = L \tau_1 \), for integer \( L \). Even though there are an integer number of logic gates in the experimental \( \tau_n \), heterogeneities in gate delays due to physical effects and FPGA routing cause \( \tau_n = L \tau_1 \pm \epsilon_r \), where \( \epsilon_r \) is a cumulative timing difference. We implement a
timing difference in the model (not shown) and note that clustering in the return map changes with $\epsilon$.

We calculate the simulated SLDE $\lambda_{\text{sim}}(\epsilon)$ for the return map in Fig. 5 using the same method applied to the experimental data. The result is plotted in Fig. 5(b), demonstrating that $\lambda_{\text{sim}}(\epsilon)$ also has microscopic features $\sim O(\tau)$ that oscillate about the average divergence of the macroscopic map. Thus, the results from the simple model are quantitatively similar to those from the experimental Boolean system, where more agreement can likely be achieved by introducing individual gate-delay heterogeneities, using a macroscopic slope $m = 1.95$, and exploring nonlinear functions for $h$.

Interestingly, the structures in the simulated SLDE become more (less) pronounced for lower (higher) levels of noise, and for sufficiently high noise levels, the structures are no longer detectable. This suggests that some physical systems may have underlying scale-dependent structures that may or may not be detected depending on noise levels. Furthermore, introducing irregularly-spaced discontinuities in the model (not just at $\tau_1$ but at $\tau_1$, $2\tau_1$, etc.) also blurs these structures and suggests that heterogeneities may be a mechanism that removes structures in the SLDE. In our experiment, the spacings between discontinuities can be tuned by moving the AND-gate inputs in Fig. 4(b), and thus our 1D Boolean chaotic system is a good candidate to begin exploring these concepts.

In summary, we present an experimental chaotic system with a macroscopic 1D return map and microscopic, regularly-spaced discontinuities that are apparent in the structure of SLDE. These discontinuities are the result of the discrete nature of the logic gates in our design on the FPGA that stretches pulse widths as part of a 1D map operator. Using a physically-motivated, simple model, we reproduce a similarly structured scale-dependent Lyapunov exponent that warrants additional experimental and theoretical study.

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