New Carry Maskable Adder using Modified Full Swing GDI

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Abstract: Addition is an essential arithmetic operation that is used extensively in processing of digital information. Now a days approximate computing is emerging methodology in area of low power VLSI design that trades off accuracy for faster and power efficient designs. Accuracy Configurable Approximate Adders is an attractive option that provides a flexibility to user to configure adder as accurate or approximate. This paper presents a new Carry Maskable Adder realization based on Full Swing-Modified Gate Diffusion Input (GDI) technique. Proposed design is functionally verified through simulations in LTspice XVII. The performance comparison of proposed design with CMOS based counterpart show that the percentage reduction in delay is 32% while power consumption is reduced by 45%.

Keywords: Approximate computing, low power VLSI, Approximate adder, Accuracy configurable Approximate Adder, Carry Maskable adder, GDI technique

1. INTRODUCTION

As technology advances, the transistors in the integrated circuit are increasing and devices are becoming more compact every day. As a result, the demand for more compact circuit implementation is increasing. As adder is the main building block for the all arithmetic operations, many researchers have presented their research work [1] – [4] on optimizing the speed and power of adder using Approximate Computing. Approximate adders have gained importance for use in circuits where some error is tolerable. Approximate computing is an energy-saving method for error-acceptable/accuracy compromised applications because it can save power by losing some accuracy. Thus there is trade-off between accuracy and power consumption [1].

From power consumption and delay aspect, we concentrated on the structural design of an accuracy-configurable adder namely Carry MaskableFull Adder (CMFA)[5]. Here, carry propagation lengthmay be selected at run time to satisfy the quality requirements. Further, the static CMOS based CMA realization uses large number transistors so alternate realizations may be looked into. Gate Diffusion Input (GDI) [6] is one such technique that reduces transistor count significantly, it however does not give full swing. In [7], Full Swing-Modified Gate Diffusion Input (FS-MGDI) technique is put forward that gives full swing. In this paper, we focus on reduction of the number of transistors in CMFA by utilizing FS-MGDI technique.

The contents of the paper are organized in five sections. In section-2, the CMFA[5]is briefly discussed. A new Carry Maskable Full Adder (CMFA) circuit is proposed in section-3 using FS-MGDI Technique. Section-4 examines the validity of proposed CMFA circuit through simulations and the paper is concluded section-5.
2. CARRY MASKABLE FULL ADDER

Carry Maskable Adder (CMA) [5] block is shown in Fig. 1. It is an accuracy-configurable approximate adder which achieves accuracy configuration without any requirement of additional logic blocks. Carry-maskable adder (CMA) [5], is an adder which can be used either as a full adder or as an OR gate. This functionality is controlled by creating a mask signal for the masking of carry propagation.

![Fig 1. CMA Block](image)

The sum and carry output (Cout) for basic full adder is described by (1) and (2) respectively and gate level schematic of the same is given in Fig. 2.

\[
\text{sum} = (A' B + AB') \text{ XOR } C_{\text{in}} \tag{1}
\]

\[
C_{\text{out}} = (AB) + C_{\text{in}} (A'B + AB') \tag{2}
\]

![Fig 2. Basic Full Adder](image)

In CMFA, the basic full adder is modified and an extra control signal called mask signal MX is introduced. The signal MX is used to configure the adder in approximate and exact mode dynamically. For MX = 1, the functionality remains same as basic full adder. The functionality for MX = 0, however, is given by (3) and (4). The gate level schematic for CMFA is shown in Fig. 3. The schematic of CMFA using static CMOS is shown in Fig. 4.

\[
\text{sum} = A \text{ OR } B \tag{3}
\]

\[
C_{\text{out}} = 0 \tag{4}
\]

![Fig 3. Gate level schematic of CMFA [5]](image)
3. FULL SWING MODIFIED GDI TECHNIQUE AND PROPOSED CARRY MASKABLE ADDER

The GDI Cell uses an NMOS and PMOS transistor as shown in Fig. 5. Although GDI [6] Cell and inverter looks similar, but they are different as the modified GDI cell [6], has 3 input terminals Gate input (G), input to NMOS(N) source/drain and input to PMOS(P) source/drain. This Technique helps in considerable reduction of gate-leakage and sub-threshold currents when compared to static CMOS Process techniques.

By changing the input configurations of modified GDI cell different Boolean functionalities can be realized and they are illustrated in Table. 1. Realization of many of these Boolean functions takes a greater number of transistors in static CMOS but with GDI it takes only 2 transistors to implement these functions.
GDI has a drawback of threshold voltage drops which results in lesser current drive. There is reduction in output swing when GDI cells are used. To overcome the voltage swing reduction, swing restoration technique [7] is used where swing is restored with single transistor [7]. Figure 6 shows the structures of modified F1 and F2 [7] cells with full swing. Restoration XOR gate is also realized in GDI technique [8] and is shown in Fig. 7.

| N | P  | G  | OUT  | FUNCTION | T.C CMOS | T.C GDI |
|---|----|----|------|----------|----------|---------|
| 0 | B  | A  | A'B  | F1       | 8        | 2       |
| B | 1  | A  | A'+B | F2       | 8        | 2       |
| 1 | B  | A  | A+B  | OR       | 6        | 2       |
| B | 0  | A  | AB   | AND      | 6        | 2       |
| C | B  | A  | AC+A'B| MUX      | 6        | 2       |
| 0 | 1  | A  | A'   | NOT      | 2        | 2       |

T.C-Transistor Count

3.1 Proposed Carry Maskable Adder

In proposed CMFA F1 and F2 cells are used to implement the gates and XOR gate is also implemented using Full Swing -GDI technique. The schematic of proposed CMFA using Swing-Restoration GDI cells is depicted in Fig. 8. The CMFA which was implemented using 38 transistors by standard CMOS process can now be implemented using only 30 transistors with the help of proposed technique. The gate level schematic for proposed CMFA remains same as that of CMFA (Fig. 3).
Fig 8. Schematic of CMFA using Full Swing GDI

4. RESULTS

In this section, the proposed CMFA is examined for functionality. For this purpose, LTSpice XVII simulations are carried out using 45 nm technology parameters and power supply is taken as 1V. For fairer comparison CMOS based CMFA is also simulated using same technology parameters and supply voltage. The timing waveforms for CMOS and proposed CMFA are depicted in Figures 9 and 10 respectively; and it is noted that both adders gave the correct functionality. The number of transistors in proposed CMFA is 30 while CMOS based adder uses 38 transistors. The delay and power consumption for proposed adder are observed to be 35.4ps and 23.78μW respectively while the corresponding values for CMOS based CMFA are 52.2ps and 43.75μW. Thus the delay and power consumption in proposed CMFA are reduced by 32% and 45% respectively.

Fig 9. Timing wave forms of CMOS based CMFA
Further, to show the usability of the proposed CMFA 4-bit ripple carry adder is implemented using the schematic of Fig. 11. The timing waveforms are depicted in Fig. 12 which match with the theory.

**5. CONCLUSIONS**

A new circuit design has been proposed in this paper for Accuracy Configurable Carry Maskable Adder based on Full Swing Modified-GDI technique. The efficacies of the proposed Carry Maskable Full Adder and the existing CMFA have been verified using 45-nm PTM technology in LTSpice XVII. In proposed CMFA, there is considerable reduction in delay and power consumption in comparison to CMOS based CMFA.
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