Diode-Like Selective Enhancement of Carrier Transport through a Metal–Semiconductor Interface Decorated by Monolayer Boron Nitride

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2D semiconductors such as monolayer molybdenum disulfide (MoS$_2$) are promising material candidates for next-generation nanoelectronics. However, there are fundamental challenges related to their metal–semiconductor (MS) contacts, which limit the performance potential for practical device applications. In this work, 2D monolayer hexagonal boron nitride (h-BN) is exploited as an ultrathin decorating layer to form a metal–insulator–semiconductor (MIS) contact, and an innovative device architecture is designed as a platform to reveal a novel diode-like selective enhancement of the carrier transport through the MIS contact. The contact resistance is significantly reduced when the electrons are transported from the semiconductor to the metal, but is barely affected when the electrons are transported oppositely. A concept of carrier collection barrier is proposed to interpret this intriguing phenomenon as well as a negative Schottky barrier height obtained from temperature-dependent measurements, and the critical role of the collection barrier at the drain end is shown for the overall transistor performance.

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DOI: 10.1002/adma.202002716
Various ultrathin insulators such as Ta$_2$O$_5$,[42] TiO$_2$,[43,44] and MgO[45] have been demonstrated to reduce $R_c$, introduce the Fermi level depinning effect, and consequently improve the device performance, primarily due to the reduction of the SBHs, the suppression of metal-induced gap states, and the formation of electric dipoles. As an atom-thick 2D layered insulator, hexagonal boron nitride (h-BN) with a bandgap of $\approx$6 eV has been exploited in the MIS contact to depin the Fermi level and lower $R_c$.[46–50] In principle, the insulating decoration layer in the MIS contact configuration should be thick enough to suppress the MS interfacial interaction, yet thin enough to provide a high tunneling probability for carrier transport through the insulator. As a result, there is a trade-off between the dominations of barrier height and tunneling resistance to obtain the lowest $R_c$.

In this work, we designed an innovative platform where both the MS and MIS contacts can be achieved and compared on a single monolayer MoS$_2$ triangle domain. First, we demonstrated the improved contact condition and consequently the boosted device performance of MoS$_2$ field-effect transistors (FETs) by using the MIS contact decorated by a monolayer h-BN. Then, we discovered a novel diode-like selective enhancement of the carrier transport through the MIS contact, where the MIS contact can significantly reduce $R_c$ and augment the electron transport from the semiconductor to the metal, but has negligible effects on the electron transport oppositely. Finally, we exploited a concept of carrier collection barrier in a comparison with the conventional carrier injection barrier to understand the selective enhancement of the carrier transport through the MIS contact as well as a negative SBH obtained from temperature-dependent measurements, and showed the critical role of the collection barrier at the drain end for the overall transistor performance.

For a comparative study, we fabricate three types of global-back-gate transistor architectures and measure four different transistor configurations depending on the assignment of source and drain: an MS-source MS-drain (MS–MS) FET, an MIS-source MIS-drain (MIS–MIS) FET, an MS-source MIS-drain (MS–MIS) FET, and an MIS-source MS-drain (MIS–MS) FET, as shown in Figure 1 and Figure S1 in the Supporting Information. The MS contact is made by a Ti/Au (10 nm/100 nm) layer and a monolayer MoS$_2$ (=0.65 nm), and the MIS contact is made by adding a monolayer h-BN (=0.4 nm)[51,52] between the Ti/Au layer and the monolayer MoS$_2$. Both MoS$_2$ and h-BN are synthesized by chemical vapor deposition (CVD).[53,54] and their monolayer structures are confirmed by Raman spectroscopy and atomic force microscopy (AFM). Especially, we design and fabricate all three types of the device architectures on a monolayer MoS$_2$ triangular domain with identical geometries including channel length and width (see the Experimental Section). Therefore, all the devices share the same quality of the MoS$_2$ channel, and the difference of the device performance...
can be solely attributed to their contact conditions. We also fabricate the devices for transmission line measurement (TLM) to extract $R_c$ with the MS and MIS contacts.

For all four transistor configurations, a comparison of drain current density ($J_D$) versus drain voltage ($V_D$) at various gate voltages ($V_G$) is performed in both linear and logarithmic scales at room temperature, as shown in Figure 2. There are several features to note. First, the $J_D$-$V_D$ characteristics are not symmetric for the positive and negative $V_D$ even with the same type of the contacts at the source and drain, due to an asymmetric contact condition (i.e., the different contact areas and thus the different $R_c$ at the source and drain). Since each device is fabricated on a triangular corner, the device has a trapezoidal channel. We define the shorter metal contact as the source and the longer one as the drain for both the MS–MS and MIS–MIS FETs. The asymmetric factor, defined as the ratio of the current density magnitude at the positive $V_D$ to that at the negative $V_D$, can be calculated as a function of $V_G$ for the MS–MS and MIS–MIS FETs, as shown in Figure S2 in the Supporting Information. Second, the MS–MS FET at $V_G = 40$ V shows the highest $J_D$ of 1.2 nA μm$^{-1}$ and it increases up to 19.3 nA μm$^{-1}$ for the MIS–MIS FET. The asymmetric factor, defined as the ratio of the current density magnitude at the positive $V_D$ to the negative $V_D$, can be calculated as a function of $V_G$ for the MS–MS and MIS–MIS FETs, as shown in Figure S2 in the Supporting Information. Second, the MS–MS FET at $V_G = 40$ V shows the highest $J_D$ of 1.2 nA μm$^{-1}$ and it increases up to 19.3 nA μm$^{-1}$ for the MIS–MIS FET. The asymmetric factor, defined as the ratio of the current density magnitude at the positive $V_D$ to the negative $V_D$, can be calculated as a function of $V_G$ for the MS–MS and MIS–MIS FETs, as shown in Figure S2 in the Supporting Information. Second, the MS–MS FET at $V_G = 40$ V shows the highest $J_D$ of 1.2 nA μm$^{-1}$ and it increases up to 19.3 nA μm$^{-1}$ for the MIS–MIS FET. The asymmetric factor, defined as the ratio of the current density magnitude at the positive $V_D$ to the negative $V_D$, can be calculated as a function of $V_G$ for the MS–MS and MIS–MIS FETs, as shown in Figure S2 in the Supporting Information. Second, the MS–MS FET at $V_G = 40$ V shows the highest $J_D$ of 1.2 nA μm$^{-1}$ and it increases up to 19.3 nA μm$^{-1}$ for the MIS–MIS FET. The asymmetric factor, defined as the ratio of the current density magnitude at the positive $V_D$ to the negative $V_D$, can be calculated as a function of $V_G$ for the MS–MS and MIS–MIS FETs, as shown in Figure S2 in the Supporting Information. Second, the MS–MS FET at $V_G = 40$ V shows the highest $J_D$ of 1.2 nA μm$^{-1}$ and it increases up to 19.3 nA μm$^{-1}$ for the MIS–MIS FET. The asymmetric factor, defined as the ratio of the current density magnitude at the positive $V_D$ to the negative $V_D$, can be calculated as a function of $V_G$ for the MS–MS and MIS–MIS FETs, as shown in Figure S2 in the Supporting Information. Second, the MS–MS FET at $V_G = 40$ V shows the highest $J_D$ of 1.2 nA μm$^{-1}$ and it increases up to 19.3 nA μm$^{-1}$ for the MIS–MIS FET. The asymmetric factor, defined as the ratio of the current density magnitude at the positive $V_D$ to the negative $V_D$, can be calculated as a function of $V_G$ for the MS–MS and MIS–MIS FETs, as shown in Figure S2 in the Supporting Information. Second, the MS–MS FET at $V_G = 40$ V shows the highest $J_D$ of 1.2 nA μm$^{-1}$ and it increases up to 19.3 nA μm$^{-1}$ for the MIS–MIS FET. The asymmetric factor, defined as the ratio of the current density magnitude at the positive $V_D$ to the negative $V_D$, can be calculated as a function of $V_G$ for the MS–MS and MIS–MIS FETs, as shown in Figure S2 in the Supporting Information.
transport from either direction (see Figure 3c). The maximum $J_D$ obtained at $V_D = 40 \text{ V}$ in this FET is enhanced by a factor of $\approx 20$, which is higher than those in any other device.

Considering the description of $J_D$–$V_D$ characteristics at a specific $V_G$ condition as $J_D = V_D/R_{\text{tot}} = V_D/(R_{\text{cS}} + R_{\text{cD}} + R_{\text{ch}})$, it is possible to visualize the impact of the MIS contact on the $V_D$-dependent resistances, as shown in Figure 3d–f. Here, $R_{\text{tot}}$, $R_{\text{cS}}$ (or $R_{\text{cD}}$), and $R_{\text{ch}}$ are the total resistance, the contact resistance at the source (or at the drain), and the channel resistance, respectively. It is clear to see that the value of $R_{\text{tot}}$ is significantly reduced by introducing the MIS drain contact at the positive $V_D$ or the MIS source contact at the negative $V_D$. Because both the MS $R_c$ and $R_{\text{ch}}$ are consistent for all the devices in comparison, the reduction of $R_{\text{tot}}$ directly indicates a decrease of $R_c$ ($\Delta R_c$) by exploiting the MIS contact, as shown in Figure 3g. The value of $\Delta R_c$ can reach up to $\approx 400 \ \Omega$ m (for the MIS drain contact at $V_D = 0.5 \text{ V}$ and for the MIS source contact at $V_D = -0.5 \text{ V}$) only when the electrons transport from the semiconductor to the metal, but approximates zero for the electron transport oppositely. Furthermore, by taking the sum of $\Delta R_c$ from the 

Figure 3. Diode-like selective enhancement of carrier transport through MIS contact. a–c) Comparison of the revised $J_D$–$V_D$ characteristics ($V_C = 40 \text{ V}$) by including the asymmetric factor for the MS–MS, MS–MIS, MIS–MS, and MIS–MIS FETs, respectively. The MS–MS FET is used as a control sample. d–f) Comparison of the corresponding $R_{\text{tot}}$ for the MS–MS, MS–MIS, MIS–MS, and MIS–MIS FETs, respectively. g,h) The calculated $\Delta R_c$ as a function of $V_D$ for the MS–MIS, MIS–MS, and MIS–MIS FETs, in a comparison with the experimental value obtained from the MIS–MIS FET.
MIS–MS and MS–MIS FETs, the overall reduction of $R_c$ for the MIS–MIS FET can be estimated as a function of $V_D$, as shown in Figure 3h. The calculated $\Delta R_c$ in this method is in a good agreement with the experimental results, which is extracted from the difference of $R_{ch}$ between the MS–MS and MIS–MIS FETs. Its symmetric behavior for both the positive and negative $V_D$ is also consistent with the experimental data, serving as good evidence for the proposed theory.

We further investigate the dependence of the carrier transport on $V_D$ by plotting $\ln(J_D/V_D^2)$ versus $1/V_D$ curves, as shown in Figure 4. For the MS–MS FET, no linear dependence is found even $V_D$ is up to 2 V. However, by introducing the MIS drain contact in the MS–MIS FET, $J$–$V$ linearity induced by Fowler–Nordheim tunneling (FNT) appears when $V_D > 0.12$ V (see Figure 4a). Considering the identical MS source contact and the channel condition, it is clear that the drain contact plays an extremely important role in the overall transistor performance. The electron transport along the channel is governed by both the injection barrier at the source and the collection barrier at the drain, and thus the applied $V_D$ is divided by $R_{ch}$, $R_{cb}$, and $R_D$. Due to the significant reduction of $R_D$ by introducing the MIS drain contact, the effective $V_D$ drop over $R_S$ at the MS source contact becomes much higher compared to that in the MS–MS FET, and thus easily reaches to the threshold to enable the FNT at the MS source contact. In contrast, for the case of the MIS–MIS FET, a more effective $V_D$ drop is allocated over $R_{ch}$ due to the reduction of both $R_S$ and $R_{cd}$. Therefore, the carrier injection at the source is still dominated by direct tunneling (DT) and thermionic emission (TE) (see Figure 4b). The FNT at the source cannot occur unless a higher $V_D$ is applied.

The $J_D$–$V_D$ transfer characteristics of all the types of the FETs are shown in Figure 5a. The MIS–MIS FET shows the best performance in terms of on-current density, on–off ratio, and subthreshold swing, whereas the MS–MS FET has the worst performance. The MS–MIS and MIS–MS FETs show the intermediate performance, and their difference is attributed to the asymmetric channel geometry and the assignment of the source and drain contacts. Similar results, together with the Schottky-to-Ohmic contact improvement, have also been reproduced from other devices using a thinner insulator for the back gating, as shown in Figure S3 in the Supporting Information.

For all the types of the FETs, their maximum $J_D$ at $V_D = 0.5$ V is obtained at $V_C = 40$ V, and their temperature ($T$) dependence is measured from 203 to 303 K, as shown in Figure 5b and Figure S4 in the Supporting Information. As $T$ increases, all the devices show an increase of $J_D$ except for the MS–MIS FET. The virtual independence of the temperature suggests the quantum mechanical tunneling as the predominant carrier transport mechanism in the MS–MIS FET, which is also consistent with the demonstration of the FNT in our prior discussion (see Figure 4a). As a comparison, the MIS–MS FET shows a similar behavior like the MS–MS FET, because the MIS source contact under the positive $V_D$ barely affects the electron transport from the metal to the semiconductor (see Figure 3b–e). The field-effect mobility ($\mu_{FE}$), defined as $(L/W)(1/C_{ox})(1/V_D)\partial I_D/\partial V_G$, is calculated from the transfer characteristics, and the maximum values as a function of $T$ are shown in Figure 5c. Here, $L$ is the channel length, $W$ is the average channel width, and $C_{ox}$ is the capacitance of 285 nm thick SiO$_2$. It has to be mentioned that the direct comparison of the $\mu_{FE}$ values is not appropriate due to the asymmetry in the source and drain contacts as well as the channel geometry. However, their dependence on $T$, described by a power law as $\mu_{FE} \sim T^n$, can directly indicate the difference in the carrier transport mechanism. It is intriguing to see that all the devices with the MIS contact at the drain, either in the MIS–MIS or MS–MIS FETs, possess a strong and consistent temperature dependence of $\mu_{FE}$, and the exponent $n$ is obtained as $=0.6$. As a comparison, for all the devices with the MS contact at the drain, either in the MS–MS or MIS–MS FETs, the
value of \( \mu_{FE} \) has a relatively weak temperature dependence and \( \gamma \) approximates to \( \approx 0.1 \). This result clearly indicates that the drain contact for carrier collection plays an important role in the overall carrier transport and transistor performance. This result is also consistent with our prior discussion on the diode-like selective enhancement: the MIS contact can significantly affect the electron transport from the semiconductor to the metal (e.g., the MIS contact at the drain under the positive \( V_D \)) but barely vary the transport on the opposite direction (e.g., the MIS contact at the source under the positive \( V_D \)).

Following the discovery of the diode-like selective enhancement of the carrier transport through the MIS contact, we further investigate its impact on \( R_c \) and SBH using the TLM and \( T \)-dependent measurements. Two TLM devices are fabricated with an identical structure, but one has the MS contacts and another one has the MIS contacts. The value of \( R_c \) is extracted from a linear predication at room temperature and plotted as a function of \( V_G \), as shown in Figure 6a, where the off-state, on-state, and subthreshold regions are identified based on the transfer characteristics in Figure 5a. In both the off-state and on-state regions, \( R_c \) with the MS contact is higher compared to that with the MIS contact, but becomes lower in the subthreshold region.

The values of the SBH are extracted from the \( T \)-dependent output and transfer characteristics\(^{[18,56,57]} \) in the MS–MS and MIS–MIS FETs, and they illustrate several important features, as shown in Figure 6b and Figure S5 in the Supporting Information. First, for both the MS–MS and MIS–MIS FETs, the SBH varies from positive to negative as the devices switch from the off-state to the on-state. The negative SBH has also been reported in the h-BN-decorated\(^{[48]} \) or graphene-decorated metal contacts\(^{[58]} \) not only for 2D materials but also for the conventional semiconductors.\(^{[59]} \) Various underlying mechanisms are proposed and they are still under debate, for example, the overshadow effect by high series resistance\(^{[59,60]} \) and the electric-field-driven modulation effect of the work functions.\(^{[58,61,62]} \)

Figure 6. Comparison of contact resistance and barrier height with MS and MIS contacts. a) Room-temperature \( R_c \) as a function of \( V_G \) for the MS–MS and MIS–MIS TLM devices. The blue, yellow, and red backgrounds indicate the off-state, subthreshold, and on-state regions, respectively. Inset: Optical microscopy image of an MIS–MIS TLM device. Scale bar: 10 \( \mu \)m. b) SBH as a function of \( V_G \) for the MS–MS and MIS–MIS FETs. The positive and negative SBHs indicate metal-to-semiconductor carrier injection barrier height (solid symbol) and semiconductor-to-metal carrier collection barrier height (hollow symbol), respectively. c) The corresponding energy band diagram along the channel for the MIS–MIS FET at a positive \( V_G \) and various \( V_C \) conditions (\( V_C < V_{FB} \), \( V_C = V_{FB} \), and \( V_C > V_{FB} \), where \( V_{FB} \) is the flat-band gate voltage). The predominant injection barrier at the off-state and subthreshold regions is highlighted in red, and the collection barrier at the on-state region is highlighted in green.
Based on our experimental data, here, we propose a new theory using the concept of the collection barrier at the drain for interpretation. In the conventional approach to extract the thermionic SBH, the positive SBH is used to describe the energy potential barrier, which prevents the electron transport from the metal to the semiconductor at the source, and the contact at the drain is assumed to be an ideal Ohmic contact. However, if the drain contact is not an ideal case, the barrier at the drain could also prevent the electron collection, and thus the negative SBH can appeal, which describes the barrier preventing the carrier collection from the semiconductor to the metal. Here, we take the MIS–MIS FET as an example, and the energy band diagram with an applied positive $V_D$ is shown in Figure 6c. When the transistor is at the off-state, the electron transport is primarily limited by the injection barrier at the source, and the drain contact acts as an Ohmic contact. As $V_G$ increases, the transistor moves into the subthreshold region. When the transistor is at the on-state, the electron transport is mainly limited by the collection barrier at the drain, and the source contact is virtually transparent due to a high tunneling probability. Even the injected electrons have a relatively higher energy, most of the energy would be dissipated by collisions during the transport along the channel, and eventually face the collection barrier at the drain with the relatively low energy. Second, the absolute SBH value of the MIS–MIS FET, either for the carrier injection (positive SBH) or carrier collection (negative SBH), is always lower in the off- and on-state regions than that in the MS–MS FET but higher in the subthreshold region (see Figure 6b). This result is very consistent with the $V_C$-dependent $R_C$ obtained from the TLM devices (see Figure 6a), serving as good evidence to prove the concept of the collection barrier. Third, although the collection barrier increases with $V_C$, $J_D$ still increases. This is because the 2D carrier density in the channel increases significantly with $V_C$. Considering the actual collection barrier height obtained in this work is only $\approx 30$ meV at the maximum, its effect on the current is completely masked by the enlarged 2D carrier density as $V_C$ increases.

Moreover, based on the energy band diagrams of the collection barrier (see Figure 6c), one can expect that the carrier transport mechanism through the MIS drain contact is a combination TE and quantum tunneling. When the collection barrier dominates, the electrons with high kinetic energies transport from the semiconductor to the metal by the DT, and the ones with low energies transport by the TE and thermionic field emission (TFE). As $T$ increases, the electron distribution in the conduction band is widened to a higher energy range, and thus more electrons can tunnel through the MIS drain contact. This result is also consistent with the experimental observation of the strong $T$ dependence of $\mu_{ext}$ in MIS–MIS and MS–MIS FETs (see Figure 5c).

In conclusion, we designed and fabricated the innovative device architecture to serve a new platform to investigate the 2D MS and MIS contacts in both symmetric and asymmetric conditions. We confirmed the improvement of the contact condition and consequently the enhancement of the device performance of MoS$_2$ FETs by exploiting the MIS contacts decorated with the monolayer h-BN. Moreover, we revealed the novel diode-like selective enhancement of the carrier transport through the MIS contact. The MIS contact can significantly reduce the contact resistance and boost the electron transport from the semiconductor to the metal, but barely affect the electron transport oppositely. With the concept of the carrier collection barrier, we revealed the underlying physics of the selective enhancement of the carrier transport through the MIS contact. We also interpreted the negative SBH obtained from the $T$-dependent measurement using the carrier collection barrier, in a comparison with the positive SBH described by the carrier injection barrier. Our work has advanced the fundamental understanding of 2D MIS contacts, and demonstrated the critical role of the collection barrier in the carrier transport of 2D nanoelectronic devices.

**Experimental Section**

**Material Synthesis and Characterization:** The monolayer MoS$_2$ was synthesized using a customized two-zone CVD system. Specifically, ammonium heptamolybdate (AHM) was used as a water-soluble Mo precursor, and NaOH was used as a water-soluble promoter. Their mixed solution was spin-coated on a SiO$_2$/Si growth substrate. The reaction between Mo and Na produced Na$_2$MoO$_4$ compounds and then became MoS$_2$ after S vapor injection. The annealing time was optimized to control the size of the isolated monolayer triangular domains. After synthesis, the monolayer MoS$_2$ flakes were wet-transported onto a SiO$_2$/Si device substrate. The large-area CVD-grown monolayer h-BN was purchased from 6Carbon Technology. The Raman spectroscopy was performed by Renishaw inVia Raman microscope. The AFM analysis was performed by Bruker Dimension Icon with ScanAsyst.

**Device Fabrication and Measurement:** Both the FET and TLM devices were fabricated using electron-beam lithography (EBL) and evaporation with a Ti/Au (10 nm/100 nm) metal layer. Specifically, three types of global-back-gate transistors, including an MS–MS FET, an MIS–MIS FET, and an MS–MIS (or MIS–MS) FET, were fabricated on a single monolayer MoS$_2$ triangular domain with the identical channel length and width (see Figure 1 and Figure S1 in the Supporting Information). To ensure a consistent channel width for the comparison of all the types of the transistors, here, the average value of the source and drain contact lengths were taken as the channel width for the trapezoidal geometry of the channel. All devices were fabricated on n-type Si substrates (0.001–0.005 Ω cm), which have 285 and 90 nm SiO$_2$ layers. The electrical measurements were performed in a vacuum-chamber probe station (MSTECH M5VC) with a semiconductor parameter analyzer (Keysight B1500A), and the temperature varied from 203 to 303 K.

**Supporting Information**

Supporting Information is available from the Wiley Online Library or from the author.

**Acknowledgements**

This work was partially supported by the National Science Foundation (NSF) under Award ECCS-1944095, the New York State Energy Research and Development Authority (NYSERDA) under Award 138126, and the New York State Center of Excellence in Materials Informatics (CMII) under Award C160186. This work was also partially supported by faculty startup funding from the University at Buffalo. The authors acknowledge support from the Vice President for Research and Economic Development (VPRED) at the University at Buffalo. A.C. acknowledges support from the Presidential Fellowship Program at the University at Buffalo.
Conflict of Interest
The authors declare no conflict of interest.

Author Contributions
F.Y. and H.L. conceived and supervised the project. J.L., C.C., and F.Y. synthesized the MoS$_2$ samples. H.N.J. and R.D. fabricated the 2D FET and TLM devices. H.N.J., M.L., and S.S. performed the electrical characterizations. S.W. performed the material characterizations. A.C., Y.G., R.W., and J.M.L. participated in the sample preparation and device characterization. X.L. and C.L.Y. participated in the data analysis.

Keywords
hexagonal boron nitride, MoS$_2$, negative Schottky barrier, transistors

Received: April 21, 2020
Revised: June 21, 2020
Published online: July 28, 2020

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