A high swing charge pump with current mismatch reduction for PLL applications

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Abstract A charge pump (CP) is widely used in modern phase-locked loop (PLL) implementations. The CP current mismatch is a dominant source of static phase offset and reference spur in the PLL output signals. In this paper, a novel CP with small current mismatch characteristic over a wide output voltage range is proposed. The specially designed dual compensation circuits use the unity-gain feedback operational amplifier and current mirrors to reduce the current mismatch when the output voltage is closed to the supply voltage (V_{DD}) or ground (GND). And the additional feedback transistors are used to reduce the impact from the channel length modulation effect. Post-layout simulation results demonstrate that the output current of the proposed CP in a 40 nm CMOS technology is 115 µA. Moreover, the current mismatch is less than 0.97 µA or 0.84% over the output voltage range from 0.04 to 1.07 V covering more than 93.6% of the 1.1 V supply. Thus, the proposed CP maximizes the dynamic range, and reduces the phase offset and reference spur of CP-PLLs.

Keywords: charge pump, current mismatch, dynamic range, phase-locked loop

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

Benefit from the characteristics of high speed, low jitter and wide locking range, charge pump phase-locked loops (CP-PLLs) are broadly used in modern wireless communication systems. Fig. 1 shows a block diagram of the conventional integer-N CP-PLL. The CP circuit converts the phase error of the phase frequency detector (PFD) into the on-time difference between the charge and discharge current, which drives the loop filter (LF). The CP current mismatch is the major source of phase offset and reference spur in PLL. It causes phase offset in PFD input by closed-loop negative feedback of PLL, and generates CP output current ripple which is then converted to the ripple on the control voltage of the voltage-controlled oscillator (VCO) by the LF. This will result in the reference spur in the PLL output spectrum.

Various design techniques have been proposed to directly improve the current matching [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12] or to detect the current mismatch and then apply analog [13, 14, 15, 16, 17] or digital [18, 19, 20, 21, 22] calibration. The digital calibration technique [20] with a signed counter calibrates the current mismatch of CP by detecting the variation of steady-state phase offset and then changing the amplitude of CP charge or discharge current. However, the finite current step of the signed counter leads to the difficulty in achieving exact matching of the CP current. The auxiliary loop-based calibration method [23] uses successive approximation register (SAR) and DAC at the cost of taking a long time to return to the lock mode. On the other hand, an adaptive body bias technique [24, 25] using a number of resistances adjusts the threshold voltage of MOS transistors to reduces current variation caused by the process variation. However, the value of these resistors is easily affected by multiple factors. In addition, a common-mode feedback scheme [4], an active feedback circuit [26, 27, 28] and a gate bias technique [29] compensate the current mismatch based on the operational amplifier or the bulk driven cascode current mirror, but the reduction of the output dynamic voltage range is still inevitable in these methods.

In this paper, a novel CP utilizing the dual regulation circuits and feedback transistors is proposed, which improves the current matching and maximizes the output dynamic range at 1.1 V supply. The rest of the paper is organized as follows: Section 2 introduces circuit design of

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the proposed CP. Simulation results are presented in Section 3 to demonstrate the practicability of the proposed method. Finally, conclusions are drawn in Section 4.

2. Circuit design

The defects of the CP, such as current mismatch, charge sharing, charge injection and clock feedthrough, lead to non-idealities of static phase offset and reference spur of PLL, which directly results in the sub-optimally of the whole PLL system. The static phase offset \( \varphi_e \) caused by CP mismatches can be expressed as [30]

\[
[\varphi_e] = 2\pi \cdot \frac{\Delta I_{on}}{I_{CP}} \cdot \frac{\Delta I}{I_{CP}}
\]

(1)

The amount of the reference spur \( P_{spur} \) is approximately calculated as [30]

\[
P_{spur}(dBc) = 20\log\left[\frac{I_{CP} \cdot R_C \cdot K_{VCO} \cdot \Delta I_{on}}{I_{ref}} \cdot \frac{\Delta I}{I_{CP}} \right] - 20\log\left(\frac{f_{ref}}{f_{p1}}\right)
\]

(2)

where \( \Delta I_{on} \) refers to the turn-on time of the PFD, the CP current mismatch and the CP current are denoted by \( \Delta I \) and \( I_{CP} \), respectively. \( R_C \) is the resistor value in the LF and \( K_{VCO} \) is the VCO gain. \( f_{ref} \) and \( f_{p1} \) are period and frequency of reference clock, respectively. \( f_{p1} \) is the frequency of the pole in the LF. Eqs. (1) and (2) show that the phase offset and reference spurs \( \varphi_e \) and \( P_{spur} \) are proportional to the CP current mismatch \( \Delta I \), which means that the phase offset and reference spurs can be scaled down by decreasing the CP current mismatch.

2.1 Conventional charge pump

As shown in Fig. 2 (a), the conventional CP is based on a drain switching architecture which consists of charge and discharge output current source \( I_{UP} \) and \( I_{DN} \), respectively. The current mismatch refers to the amplitude difference between \( I_{UP} \) and \( I_{DN} \). Fig. 2 (b) shows that \( I_{UP} \) and \( I_{DN} \) deviate from each other due to the channel length modulation effect when the output voltage of CP \( (V_{CP}) \) varies. M1 and M2 in Fig. 2 (a) are the charge and discharge current source transistors in the CP, respectively. Their saturation currents in accordance with the channel length modulation effect can be expressed as

\[
I_{UP} = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right) \left(V_{DD} - V_{sat}\right) \left(1 + \lambda_p V_{DD}\right)
\]

(3)

\[
I_{DN} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) \left(V_{sat} - V_p\right) \left(1 + \lambda_n V_{sat}\right)
\]

(4)

\( I_{ss1} \) and \( I_{ss2} \) have the same current \( I_{ss} \). Assuming that NMOS transistors M2 and M4 have the same size \( (W/L) \) and PMOS transistors M1 and M3 have the same size \( (W/L) \), when \( V_{CP} \) is close to GND, M1 operates at the saturation region and M2 operates at the triode region. Taking no account of the channel length modulation effect temporarily, their currents and mismatch \( \Delta I_1 \) are given by

\[
I_{UP} = I_{SS} = I_{DN} = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right) \left(V_{DD} - V_{sat}\right)^2
\]

(5)

\[
I_{DN} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) \left(V_{sat} - V_p\right)^2
\]

(6)

\[
\Delta I_1 = \frac{1}{2} \mu_m C_{ox} \left(\frac{W}{L}\right) \left(V_{DD} - V_{sat}\right)^2
\]

(7)

When the \( V_{CP} \) is close to \( V_{DD} \), M1 operates at the triode region, and M2 operates at the saturation region. Without considering the channel length modulation effect temporarily, their currents and mismatch \( \Delta I_2 \) are given by

\[
I_{UP} = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right) \left(2\left(V_{DD} - V_{sat}\right) - V_{DD} - V_{sat}^2\right)
\]

(8)

\[
I_{DN} = I_{ss} = I_{dn} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) \left(V_{sat} - V_p\right)^2
\]

(9)

\[
\Delta I_2 = \frac{1}{2} \mu_m C_{ox} \left(\frac{W}{L}\right) \left(V_{DD} - V_{sat}\right)^2
\]

(10)

2.2 Proposed charge pump

The proposed charge pump utilizes two current mismatch compensation circuits to suppress the current mismatch when the output voltage is near \( V_{DD} \) or GND, as shown in Fig. 3. \( I_{ss1} \) and \( I_{ss2} \) generated by cascode biasing networks have the same current \( I_{ss} \). In order to simplify the circuit design, NMOS transistors M2, M4 and M7 have the same size \( (W/L) \), and PMOS transistors M1, M3 and M10 have the same size \( (W/L) \). The current mismatch reduction circuit 1 (CMRC1) consists of an operational amplifier OP1, NMOS transistor M7, and current mirrors. OP1 is deemed as the unity-gain feedback buffer to follow the voltage of the drain node \( n \) of M2 \( (V_{dn}) \). When \( V_{CP} \) is close to GND, CMRC1 senses the current mismatch \( \Delta I_1 \), given by Eq. (7). As \( V_{dn} \) is lower than \( V_{ds, sat} \) of M2, M7 turns on at the saturation region, which generates the mismatch compensation current \( I_{comp1} \), whose value is equal to \( \Delta I_1 \), then reducing the charge current \( I_{UP} \) to match the discharge current \( I_{DN} \) by the PMOS current mirrors M8 and M9.

Similarly, OP2 is regard as the unity-gain feedback buffer
to follow the voltage of the drain node dp of M1. When \( V_{CP} \) is close to \( V_{DD} \), the current mismatch reduction circuit 2 (CMRC2) senses the CP current mismatch \( \Delta I_2 \), given by Eq. (10), and then generates mismatch compensation current \( I_{comp2} \). And then, it adjusts the discharge current \( I_{DN} \) to follow the changes in charge current \( I_{UP} \) by the NMOS current mirrors M11 and M12.

However, due to the channel length modulation effect, the proposed CP cannot achieve exact matching of the output current. Thereby, in order to reduce the current mismatch caused by the channel-length modulation effect, transistors M17, M18, M19 and M20 are added to finely control the charge or discharge current \( I_{UP} \) and \( I_{DN} \), respectively. When \( V_{CP} \) decreases towards GND, the voltage at the node dp (\( V_{dp} \)) will turn on transistors M17 and M18 to reduce the \( I_{UP} \) to match the lower \( I_{DN} \). Similarly, when \( V_{CP} \) is close to \( V_{DD} \), the \( V_{dn} \) will turn on transistors M19 and M20 to change the \( I_{DN} \) to match the lower \( I_{UP} \).

Moreover, the dynamic current mismatch is inherent due to the non-ideal effects in switches. Thus, the non-ideal switches effects should be considered in the circuit design, such as clock feedthrough and charge sharing. To overcome the lack of charge sharing among the parasitic capacitances at the current sources’ drain nodes dp, dn and the capacitors in the LF, a current-steering topology [26, 27, 30] is adopted using transistors M13-M16 as switches-at-drain with operational amplifier, where \( I_{UP} \) and \( I_{DN} \) are either connected to \( V_{CP} \) or dumped to \( V_{dump} \). The operational amplifier OP3 which is served as the unity-gain feedback buffer is used to keep the output common mode constant during CP switching. By this way, \( I_{UP} \) and \( I_{DN} \) can be kept on all the time, and \( V_{dp} \) and \( V_{dn} \) are kept constant during CP switching. Thus, the LF-CP charge sharing is minimized to improve the dynamic current matching.

2.3 Loop stability issues
There are multiple feedback loops inside the proposed CP circuit. Thus, it is necessary to ensure their stability for proper operation. When \( V_{CP} \) is near \( V_{DD}/2 \), CMRC1 and CMRC2 are off. There are two positive feedback loops. Loop1 consists of M1 and M17, and loop2 is composed of M2 and M19, as shown in Fig. 4. Their loop gain can be expressed as Eqs. (11) and (12), respectively.

\[
A_{loop1} = \frac{g_{m11}}{\frac{g_{m11}}{R_{eq1}} + \frac{1}{R_{eq1}}} 
\]

\[
A_{loop2} = \frac{g_{m17}}{\frac{g_{m17}}{R_{eq2}} + \frac{1}{R_{eq2}}} 
\]

where \( R_{eq1} \) represents the equivalent resistance of switches, M2 and M19. \( R_{eq2} \) is the equivalent resistance of switches, M1 and M17. To make sure loop gain below 0 dB, M17 should be much smaller size than M1, making \( g_{m17} \) slightly smaller than \( g_{m1} \), so that loop1 remains stable. In the same way, the size of M19 should be much smaller than that of M2 to ensure stability of loop2.

When \( V_{CP} \) decreases towards GND, M2 operates in triode region, and M19 and CMRC2 are off. Given by Fig. 5, a positive feedback loop consists of M1 and M17. In addition, another one is a negative feedback loop. The feedback signal is produced by M18, then passing through M8, M9, M3 and M1, finally returning to the gate of M18. These two loops have the same feedforward path, and the
loop gain of the overall feedback is given by

\[ A_{\text{loop1}} = \left[ g_{m7} - g_{m5} \left( \frac{g_{ml}}{g_{m8} + g_{ds} + g_{dl}} \right) \right] \frac{1}{g_{ds1}} || R_{eq1} \]  
(13)

where \( R_{eq,t1} \) is the equivalent resistance of switches and M2. Similarly, the size of M17 and M18 must be chosen carefully to make sure that the loop gain is less than 0 dB. Furthermore, the third one is a positive feedback loop, which consists of OP1, M7, M8, M9, M3, M1 and M2. Its loop gain is obtained as

\[ A_{\text{loop3}} = g_{m7} \left( \frac{g_{ml}}{g_{m8} + g_{ds} + g_{dl}} \right) \left( r_{d2} || R_{eq3} \right) \]
\[ \equiv g_{m7} \left( g_{ds2} + \frac{1}{R_{eq3}} \right) \]  
(14)

\[ g_{m7} = u C_{in} \frac{W}{L} \left( V_{gs} - V_{ds} - V_{th} \right) \]  
(15)

\[ g_{ds2} = u C_{in} \frac{W}{L} \left( V_{gs} - V_{ds} - V_{th} \right) \]  
(16)

where \( R_{eq3} \) is the equivalent resistance of switches, M1, M8, M9, M17 and M18. Eqs. (14), (15) and (16) indicate that loop3 is stable as its loop gain is below 0 dB.

\[ A_{\text{loop2}} = g_{m19} - g_{m20} \left( \frac{g_{ml}}{g_{m17} + g_{ds} + g_{dl}} \right) \left( \frac{1}{g_{ds1}} || R_{eq2} \right) \]  
(17)

\[ A_{\text{loop4}} = g_{m10} \left( g_{ds1} + \frac{1}{R_{eq4}} \right) \]  
(18)

where \( R_{eq,t2} \) is the equivalent resistance of switches and M1. \( R_{eq,t1} \) refers to the equivalent resistance of switches, M2, M11, M12, M19 and M20. To ensure stability of these loops, their loop gains must be under 0 dB.

**3. Simulation results**

The proposed CP is implemented in 40 nm CMOS technology with a supply voltage of 1.1 V. Stability simulation of these feedback loops has been done to ensure that these loops are stable. Fig. 6 shows the loop gain and phase of multiple positive feedback loops versus frequency when the \( V_{CP} \) varies from 0.1V to 1V. The loop gains of these loops vary from -8.40 dB to -0.85 dB. Thus, the proposed CP is stable as their loop gains are below 0 dB. Fig. 7 shows the current transient response of charge and discharge current. The charge and discharge paths use the same control signals (i.e. UP/DN logic error signals from the PFD) with a period of 100 ns and a 50% duty cycle. And the CP output voltage \( V_{CP} \) directly drives LPF with \( C_{z} = 371 \) pF, \( R_{z} = 6.86 \) k\( \Omega \), \( C_{p} = 24.7 \) pF.

![Fig. 6 Loop stability analysis.](image)

![Fig. 7 Transient simulation results of charge and discharge current.](image)

The layout of the CP is shown in Fig. 8, whereas the active area is 91 \times 74 \mu m^2. The transistors of the current sources
are stacked for high output impedance and low noise. The post-layout simulation results reveal that the CP peak current is 115 \( \mu A \) with 0.72 mW power consumption, as given by Fig. 9. And the maximum current mismatch of the proposed CP was less than 0.97 \( \mu A \) when the output voltage ranges from 0.04 V to 1.07 V. Fig. 10 shows the CP output voltage transient simulation results with a control signal of 40 ns cycle. Moreover, in order to estimate the effects of process variation and random mismatch in CP circuit, and take into account the mismatch between \( I_{SS1} \) and \( I_{SS2} \), the 1000-samples Monte Carlo simulation of current mismatch has been done. As shown in Fig. 11, the mean of current mismatch is 1.701 \( \mu A \) and the standard deviation is 0.971 \( \mu A \). The simulated static phase offset and reference spur level in PLL are 6.6 ps and -79.3 dBc, respectively, as shown in Fig. 12, thus demonstrating the efficiency of the proposed CP in improving the reference spur and static phase offset performance of PLL. Table I compares the performance of the proposed CP with recent publications.

![Fig. 8 Layout of the proposed charge pump.](image)

![Fig. 9 Simulation results of current mismatch of proposed CP.](image)

![Fig. 10 Simulated \( V_{CP} \) in charging (a) and discharging procedure (b).](image)

![Fig. 11 Monte Carlo simulation results of current mismatch.](image)

![Fig. 12 Simulated static phase offset (a) and reference spur (b) against simulation conditions: \( I_{CP} = 115 \mu A \), \( \Delta I = 0.965 \mu A \), \( f_{ref} = 10 \) MHz, \( \Delta t_{on} = 0.8 \) ns, \( N = 80 \), \( V_{CO} = 170 \) MHz, \( R_{L} = 6.86 \) k\( \Omega \), \( f_{fB} = 1 \) MHz.](image)

### Table I. Performance comparison.

| Description                  | [9] | [12] | [25] | This work |
|------------------------------|-----|------|------|-----------|
| Technology (nm)              | 180 | 180  | 40   | 40        |
| Supply (Volt)                | 1.8 | 1.8  | 0.8  | 1.1       |
| CP current (\( \mu A \))     | 100 | 50   | 125  | 115       |
| Current mismatch (%)         | 2.11| 2.00 | 1.50 | 0.84      |
| Matching voltage (V, \%      | 0.30-1.45 | 0.35-1.48 | 0.02-0.76 | 0.04-1.07 |
| range                        | 63.9| 62.7 | 92.5 | 93.6      |
| Power (mW)                   | 1.80| 0.13 | NA   | 0.72      |
4. Conclusion

A novel charge pump implemented in the 40 nm CMOS technology with improved current matching and wide dynamic range has been presented in this paper. The proposed CP uses the operational amplifier-based dual current mismatch compensation circuits, the additional feedback transistors, and a current-steering topology to minimize the LF-CP charge sharing and improve the current matching performance. Post-layout simulation results show that the current mismatch under 0.84% is achieved when the output voltage ranges from 0.04 V to 1.07 V covering more than 93.6% of the 1.1 V supply. The CP consumes 0.72 mW with 115 μA of the CP output current, and the active chip area is 0.0067 mm². Thus, the propose CP is a suitable solution to reduce the static phase offset and the reference spur level in nano-meter CMOS PLL implementations.

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