Radiation tolerant, thin, passive CMOS sensors read out with the RD53A chip

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Abstract

The radiation hardness of passive CMOS pixel sensors fabricated in 150 nm LFoundry technology is investigated. CMOS process lines are especially of interest for large-scale silicon detectors as they offer high production throughput at comparatively low cost. Moreover, several features like poly-silicon resistors, MIM-capacitors and several metal layers are available which can help enhance the sensor design. The performance of a 100 µm thin passive CMOS sensor with a pixel pitch of 50 µm at different irradiation levels, $5 \times 10^{15}$ $n_{eq}$ cm$^{-2}$ and $1 \times 10^{16}$ $n_{eq}$ cm$^{-2}$, is presented. The sensor was bump-bonded and read out using the RD53A readout chip. After the highest fluence a hit-detection efficiency larger than 99% is measured for minimum ionising particles. The measured equivalent noise charge is comparable to conventional planar pixel sensors. Passive CMOS sensors are thus an attractive option for silicon detectors operating in radiation harsh environments like the upgrades for the LHC experiments.

Keywords: solid state detectors, pixel detectors, radiation-hard detectors, hybrid pixels, silicon sensors

1. Introduction

After the upgrade of the Large Hadron Collider (LHC) at CERN in 2026 [1], the accelerator aims to deliver 5 - 7 times the nominal luminosity of $1 \times 10^{34}$ cm$^{-2}$ s$^{-1}$. This results in new challenges in terms of data rate

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capabilities and radiation tolerance, especially for detector layers close to
the interaction point of the colliding proton beams. Therefore, the ATLAS
and CMS experiments will replace their currently installed tracking detectors
with detectors featuring larger areas of silicon and decreased pixel pitch [2, 3].
In particular, the ATLAS Inner Detector [4] is going to be replaced by an all-
silicon tracking detector, the ATLAS Inner Tracker (ITk) [2]. The expected
1 MeV neutron equivalent fluence\(^{1}\) for the innermost layer is approximately
\(1 \times 10^{16} \text{n}_{\text{eq}} \text{cm}^{-2}\), for the outer layers fluences\(^{2}\) from \(2 \times 10^{15} \text{n}_{\text{eq}} \text{cm}^{-2}\) up to
\(5 \times 10^{15} \text{n}_{\text{eq}} \text{cm}^{-2}\) are expected [2].

Since it was demonstrated in the past that hybrid pixel detectors [5] can
be successfully operated in such harsh radiation environments at the LHC,
it is foreseen to employ this technology also for the upgraded pixel detector.
However, the surface of the new ATLAS pixel detector is increased from
approximately \(2 \text{m}^2\) to \(13 \text{m}^2\) [2], demanding large-area solutions with cost-
effective designs. An approach of employing monolithic (active) CMOS pixel
detectors [6, 7] which combine the sensing and electronic processing functions,
and thus saving the time-consuming and expensive hybridisation process, has
been investigated [8, 9]. With this CMOS pixel development an interesting
option became attractive that utilises commercial CMOS process lines for
the fabrication of planar sensors as the sensing part of hybrid pixel detectors.
CMOS fabrications offer a high production throughput at comparatively low
cost. Further benefits arise from the fact that several features are available
to enhance the sensor design. For instance, polysilicon layers can be used to
connect each pixel to a bias grid making it possible to test the functionality of
the sensor at wafer level. Also, MIM (metal-insulator-metal) capacitors can
be used to AC-couple the sensor pixels to the readout chip pixels preventing
leakage current flowing into the readout channels. Moreover, several metal
layers are available that can be exploited as re-distribution layers such that
enlarged inter-gap pixels (between two readout chips) can be avoided. These
sensors are called passive CMOS sensors since they do not have any active
components implemented.

Passive CMOS sensors in a large pixel pitch design (\(50 \times 250 \mu\text{m}^2\) pixels)
were already investigated [10]. The characterisation of the small pixel pitch
design (\(50 \times 50 \mu\text{m}^2\) pixels) before irradiation can be found in [11]. In the

\(^{1}\) after an integrated luminosity of 2000 \(\text{fb}^{-1}\).
\(^{2}\) after an integrated luminosity of 4000 \(\text{fb}^{-1}\).
following the performance of irradiated passive CMOS sensors is studied to demonstrate their radiation tolerance and suitability for the upgrades of the LHC experiments.

2. LFoundry passive CMOS pixel sensor

2.1. Pixel sensor design

Passive CMOS n-in-p pixel sensors in 150 nm LFoundry [12] technology were manufactured on high-resistivity Czochralski wafers. The resistivity of the substrate is at least 2 kΩ cm, as specified by the foundry. Measurements suggest that the resistivity is between 5 and 6 kΩ cm [10]. The substrate was thinned to a thickness of 100 µm. The backside was processed by Ion Beam Services (IBS) [13] including backside implantation as well a backside metallisation allowing for backside bias application. The sensor consists of 64 × 64 pixels with a size of 50 × 50 µm², and has a total area of 3.8 × 3.8 mm².

Fig. 1 shows a simplified schematic cross section of one pixel, Fig. 2 depicts the layout of the pixel matrix. In order to investigate the charge collection properties and the pixel capacitance, various pixel designs were implemented. The left half of the pixel matrix consists of pixels with a regular n-implantation (n-well, denoted as NW), whereas the right half of the pixel matrix consists of pixels with an additional deep n-implantation (deep n-well, denoted as DNW). The size of the n-implantations varies in both dimensions between 30 µm (top of the matrix) and 15 µm (bottom of the matrix).
Figure 2: Left: Layout of the LFoundry passive CMOS pixel sensor. The left half of the pixel matrix consists of pixels with a n-implantation (NW), whereas the right half consists of pixels with an additional deep n-implantation (DNW). The size of the n-implantations varies in both dimensions between 30 µm (top of the matrix) and 15 µm (bottom of the matrix). Guard-rings isolate the pixels from the high voltage at the sensor edge. Right: Enlarged view of the different pixel designs.

isolate the pixels from each other a small p-implantation (p-stop) is used. Moreover, a fine-pitch polysilicon layer encloses the n-implantations with the intention to increase the breakdown voltage, especially after irradiation. The pixel matrix is surrounded by an n-implantation confining the active pixel region. In addition, six guard-rings isolate the pixels from the high voltage at the sensor edge.

The sensor is bump-bonded via solder bumps (by Fraunhofer IZM [14]) to the RD53A readout chip [15, 16], a prototype readout chip for the ATLAS ITk pixel detector.

2.2. Pixel sensor irradiation

The studied pixel detector has been step-wise irradiated to the target fluence to investigate the performance at different irradiation levels. In the first step, the detector was irradiated to a fluence of $5 \times 10^{15} \text{n}_{eq} \text{cm}^{-2}$ at
the MC40 cyclotron of the University of Birmingham [17] using 27 MeV protons. In the second step, the detector was irradiated to a total fluence of $1 \times 10^{16} \text{neq cm}^{-2}$ at the Proton Irradiation Site at the Bonn Isochronous Cyclotron [18] using 14 MeV protons. The irradiations were performed uniformly in a cold environment and the device was left unpowered during irradiation. After each irradiation step the device was annealed for 80 min at 60°C. The corresponding total ionising doses created by protons were estimated to approximately 660 Mrad (Birmingham) and 580 Mrad (Bonn).

3. Leakage current measurements

To test the functionality of the sensors and to determine their maximum operational voltage, the leakage current is measured as a function of the (reverse) bias voltage (IV-curve). Fig. 3 shows the IV-curves before and after

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3Important for surface damage affecting the readout chip.
irradiation of the tested sensor after bump-bonding. The IV-curve before irradiation was measured at room temperature, whereas the IV-curves after irradiation were measured at an environmental temperature of $-25^\circ C$. Before irradiation the maximum operational voltage is approximately 220 V. After irradiation the sensor is still functional and there is no breakdown visible anymore up to the maximum tested operational voltage of 350 V. Furthermore, the leakage current after a fluence of $5 \times 10^{15} \text{n_{eq} cm}^{-2}$ is approximately $23 \mu \text{A cm}^{-2}$ and meets the requirements for ATLAS ($< 35 \mu \text{A cm}^{-2}$). As expected, the leakage current at a fluence of $1 \times 10^{16} \text{n_{eq} cm}^{-2}$ is approximately twice as large as for a fluence of $5 \times 10^{15} \text{n_{eq} cm}^{-2}$. The power dissipation of the sensor needed for a hit-detection efficiency larger than 97% (see Sec. 5) is about $7 \text{mW cm}^{-2}$ ($35 \mu \text{A cm}^{-2}$ at 200 V) after a fluence of $1 \times 10^{16} \text{n_{eq} cm}^{-2}$. This is comparable to the power dissipation reported for 3D sensors [19].

4. Electronic noise

An important parameter to quantify the performance of a sensor is the equivalent noise charge (ENC). The ENC distributions of the investigated pixel detector at different irradiation steps can be seen in Fig. 4.

Before irradiation, an ENC of $73 \text{e}$ is measured. This is a value comparable to other planar sensor designs read out with the same amplifier chip. After irradiation, the ENC increases to about $100 \text{e}$. The reason for that is most likely an increase in shot noise due the higher leakage current after irradiation (approximately $90 \mu \text{A}$ corresponding to $22 \text{nA per pixel}$). In addition, the performance of the analogue front-end is degraded by irradiation (i.e. the transconductance $g_m$ decreases) and is likely responsible for an unspecifiable additional noise contribution. Further, it cannot be excluded that the detector capacitance increases after irradiation which would also lead to an increase in noise.

Comparing different pixel designs, there is no significant difference in terms of noise observed before irradiation, although the measured pixel capacitances are different for the various pixel geometries, $(33.5 \pm 0.2) \text{fF}$ for NW30 pixels and $(22.4 \pm 0.2) \text{fF}$ for NW15 pixels [20]. At a fluence of $1 \times 10^{16} \text{n_{eq} cm}^{-2}$, the noise of NW30 pixels is approximately 8% higher than for NW15 pixels. Since this difference is small, the benefits in terms of noise

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4 Measured at a temperature of $-17^\circ C$.
5 Including contributions due to routing and bump-bonds.
Figure 4: Equivalent noise charge distributions at different irradiation levels. The noise distributions for different pixel geometries are shown exemplary for the NW30 and NW15 pixels. The distributions are fitted with a Gaussian function to extract the mean noise. The uncertainties of the estimated means are approximately \(2\,\text{e} \).

reduction for pixels featuring small implants do not outweigh the disadvantages that arise in terms of hit-detection efficiency (see Sec. 5).

5. Hit-detection efficiency measurement

A crucial detector property is the hit-detection efficiency, i.e. the probability with which a hit (a particle traversing a pixel) is recognised by the detector. For the application as a tracking detector the hit-detection efficiency has to be high for efficient hit finding and track reconstruction. Especially after irradiation, the hit-detection efficiency is of interest, and for ATLAS ITk it is required to be above 97\% \cite{2}.

To measure the hit-detection efficiency the device under test (DUT) is placed in a beam-telescope setup consisting of six high-resolution Mimosa26 planes (EUDET-type beam telescope)\cite{21} and an ATLAS FE-I4\cite{22} reference plane. The Mimosa26 planes provide a high spatial resolution of approximately 3\,\mu m\cite{21} allowing a precise track reconstruction. However, the time resolution of the Mimosa26 sensors is limited due to their rolling shutter readout (duration of 115.2\,\mu s). In contrast, the FE-I4 reference plane
provides a very good time-stamping capability with a precision better than 25 ns. The challenge during track reconstruction is to ensure a correct time assignment of the Mimosa26 tracks, which is needed for a proper hit-detection efficiency measurement. Therefore, the ATLAS FE-I4 plane is used as a time reference plane such that the tracking hits in the Mimosa26 planes spatially match the hit in the timing reference plane, which thus provides the time stamp for the track.

The hit-detection efficiency of the investigated sensor was measured using a minimum ionising electron beam provided by the ELSA test beam facility [23] (2.5 GeV) and the DESY II test beam facility [24] (5 GeV). A scintillator in front of the telescope setup generates a trigger signal when particles traverse the setup. An EUDET-type Trigger Logic Unit (TLU) [25] is used to distribute and synchronise the trigger signals with the different read-out systems. The Mimosa26 telescope is read out without being triggered in continuous rolling shutter readout mode using the pymosa software [26]. The DUT is read out triggered using the BDAQ53 software [27] and the ATLAS FE-I4 plane was read out triggered using the PyBAR software [28]. The data is analysed using the beam telescope analysis software [29] including clustering, detector alignment, and track reconstruction as well as the final result analysis of the hit-detection efficiency and charge collection behaviour.

For all following measurements, the detector was tuned to a threshold of approximately 1000 e with a noise occupancy of less than $10^{-6}$ per pixel.

Fig. 5 illustrates the (unbiased) residual distribution (distance between hit and track intersection) in the y-dimension at the DUT. The residuals are centred around zero which indicates a correct alignment of the detector planes. Due to multiple scattering the residual distribution is smeared out and can be approximated with a Gaussian function. The deviation from the Gaussian function towards the tails originates from the fact that the probability for large scattering angles is enhanced as described in Molière’s theory [30]. From a fit a residual width (1-σ width) of 18.7 μm is extracted. This is in agreement with the expectation since the residual width for unbiased tracks is the quadratic sum of the intrinsic resolution of the DUT ($\frac{\text{pixel pitch}}{\sqrt{12}}$) and the pointing resolution at the DUT (a few μm). The pointing resolution in this setup is slightly worsened by the additional material of the cooling infrastructure (cooling box for DUT and PCB cooling plate). However, the resolution is still sufficient for in-pixel studies.

In order to reject noise hits (spatially uncorrelated) which artificially increase the hit-detection efficiency, hits are only considered as efficient if the
Figure 5: (Unbiased) residual distribution in one dimension at the DUT. The data is shown on a logarithmic scale. The distribution is fitted with a Gaussian function. The grey dashed line illustrates the maximum distance between a hit and track intersection (with the DUT) at which a hit contributes to the efficiency.

Figure 6: Hit-detection efficiency as a function of bias voltage for different pixel flavors and different irradiation levels. The grey dashed line represents the requirement of an (in-time) efficiency larger than 97%. For the sake of clarity, not all pixel designs are shown. The quoted error bars are purely statistical. Left: NW-flavors. Right: DNW-flavors.
Figure 7: In-pixel efficiency map after a fluence of $1 \times 10^{16} \text{n}_{\text{eq}} \text{cm}^{-2}$ for two different pixel flavors (left: NW30 and right: NW15) at a bias voltage of 400 V.

residual of the track is smaller than a given distance (of 120 µm). This efficiency search radius is illustrated in Fig. 5.

Fig. 6a shows the hit-detection efficiency before and after irradiation as a function of the applied (reverse) bias voltage for the NW30 and NW25 pixel designs (regular n-implantation with a size of 30 and 25 µm), Fig. 6b shows this for the DNW30 and DNW25 pixel designs (additional deep n-implantation with a size of 30 and 25 µm). For the sake of clarity, other pixel designs are omitted here since they have a lower efficiency after irradiation.

Before irradiation, an efficiency larger than 99.5 % is achieved at 5 V only and there is no significant difference across the various pixel designs visible. After irradiation, the efficiency increases with increasing bias voltage. The measured efficiency after a fluence of $5 \times 10^{15} \text{n}_{\text{eq}} \text{cm}^{-2}$ and a bias voltage of 350 V is (99.89 ± 0.01) % for the NW30 flavor and (99.88 ± 0.01) % for the DNW30 flavor. This is well above the requirement of 97 % after irradiation (grey dashed line in Fig. 6). After a fluence of $1 \times 10^{16} \text{n}_{\text{eq}} \text{cm}^{-2}$ the efficiency decreases further (especially for low bias voltages). However, at 400 V an efficiency of (99.79 ± 0.01) % for the NW30 and (99.78 ± 0.01) % for the DNW30 flavor can still be achieved. Especially, at the highest measured fluence, it is visible that flavors with a smaller implant size show a slightly lower efficiency. Furthermore, at low bias voltages, the hit-detection efficiency of designs with a deep n-well (same implant size) is higher compared to designs

6This is also true for the omitted (D)NW20 and (D)NW15 flavors.
Figure 8: In-pixel charge map in electrons after a fluence of $1 \times 10^{16} \text{n}_{\text{eq}} \text{cm}^{-2}$ for two different pixel flavors (left: NW30 and right: NW15) at a bias voltage of 400 V.

with only the standard n-well geometry, especially for smaller implant sizes.

Fig. 7 shows in-pixel efficiency maps (all data mapped onto a single pixel) at a fluence of $1 \times 10^{16} \text{n}_{\text{eq}} \text{cm}^{-2}$ for two different pixel flavors (NW30 and NW15) at a bias voltage of 400 V. One can see that the efficiency, for pixel designs with smaller implant size, is low at the pixel corners which is due to the low electric field (and charge sharing) in this region.

6. Charge measurements and charge-collection efficiency

In addition to the hit-detection efficiency, the charge collection behaviour was studied during test beams. The readout chip already provides an internal charge information, called ToT (time over threshold). However, the precision of this measurement needed for a charge calibration (using radioactive sources) or charge measurements during test beams is not sufficient. This problem is circumvented by using the so-called TDC method \cite{31}. This method makes use of the chip’s HitOR signal (logical OR of all discriminator outputs) whose length is proportional to the collected charge. This signal is sampled with a 640 MHz clock provided externally by the readout system, thus enabling a precise charge measurement.

In Sec. 5 it was shown that, after irradiation, the efficiency for pixel designs with smaller implant sizes is low in the pixel corners where the electrical field is low. The same behaviour (low charge in pixel corners) is observed for the collected charge. The corresponding in-pixel charge maps (only events with cluster size of 1), after a fluence of $1 \times 10^{16} \text{n}_{\text{eq}} \text{cm}^{-2}$, can be seen in
Figure 9: Measured charge distributions for different irradiation levels for the NW30 flavor. The distributions are fitted with a Landau-Gauss convolution to extract the most probable value (MPV). Before irradiation a MPV of $(6590 \pm 170)$ e is measured at 80 V. At a fluence of $5 \times 10^{15} \, n_{eq} \, cm^{-2}$ a MPV of $(5030 \pm 50)$ e is measured at 350 V, and at a fluence of $1 \times 10^{16} \, n_{eq} \, cm^{-2}$ a MPV of $(3670 \pm 50)$ e is measured at 400 V.

Fig. 8. This is in agreement with the expectations and explains the efficiency loss since a lower electric field after irradiation leads to more charge carrier trapping, and thus to a smaller collected charge which in turn results in a lower efficiency for a given threshold.

In Fig. 9 the measured charge distributions for the different irradiation levels measured using the NW30 pixel design are depicted. The distributions follow a Landau function convoluted with a Gaussian function due to electronic noise. Furthermore, it is visible that the most probable value (MPV) extracted from a fit decreases with increasing fluence. The reasons for that are the facts that a) after irradiation the sensor can no longer be fully depleted at reasonable bias voltages and b) charge carrier trapping during charge collection due to radiation damage of the bulk.

The collected charge as a function of the bias voltage, illustrated in Fig. 10 was studied. Each data point corresponds to the most probable value extracted from a fit to the measured charge distribution. The charge signal increases with bias voltage since the depleted volume extends with
Increasing bias voltage. Before irradiation, the amount of collected charge starts to saturate at approximately 40 V leading to a charge signal of about 6600 e. This indicates that the sensor is fully depleted at approximately 40 V. Assuming that 73 electrons per \( \mu \text{m} \) (extracted from a GEANT4 simulation) are created within the depletion zone, this yields a silicon bulk thickness of approximately 90 \( \mu \text{m} \). This value is reasonable since the nominal thickness of 100 \( \mu \text{m} \) includes also the metal layers with a thickness of a few \( \mu \text{m} \).

After irradiation, the amount of collected charge decreases due to the fact that the sensor can no longer be fully depleted and charge carrier trapping sets in. The measured charge signal after a fluence of \( 1 \times 10^{16} \text{n}_{\text{eq}} \text{cm}^{-2} \) is approximately 3700 e at the highest measured bias voltage of 400 V.

The measured charge signal can be translated to a charge collection efficiency (CCE), as shown in Fig. [10] (axis on the right-hand side). The charge collection efficiency is obtained by dividing the measured charge by the maximum measured charge before irradiation (6600 e). This yields a maximum charge collection efficiency of approximately 80\% at a fluence of \( 5 \times 10^{15} \text{n}_{\text{eq}} \text{cm}^{-2} \) and 55\% at a fluence of \( 1 \times 10^{16} \text{n}_{\text{eq}} \text{cm}^{-2} \), respectively.
7. Conclusion and outlook

The radiation tolerance of 100µm thin passive CMOS sensors fabricated in 150nm LFoundry technology has been investigated. The sensors are still functional even after a fluence of $1 \times 10^{16} \text{n}_{\text{eq}} \text{cm}^{-2}$ and can be successfully operated. At this fluence a hit-detection efficiency of $(99.79 \pm 0.01)\%$ is measured (at 400V) for the NW30 design. The charge collection efficiency is measured to be approximately 55% at the maximum tested bias voltage of 400V after the highest fluence. In addition, the power dissipation of the sensor needed to meet the ATLAS ITk requirements in terms of efficiency is comparable to 3D sensors. This demonstrates that passive CMOS sensors are radiation tolerant and withstand a fluence of $1 \times 10^{16} \text{n}_{\text{eq}} \text{cm}^{-2}$, the expected fluence for the future innermost ATLAS pixel detector layer. The performance of passive CMOS sensors in terms of noise and hit-detection efficiency equals that of conventional planar sensors. Full-size (RD53-sized) passive CMOS sensors using the NW30 geometry for the ATLAS and CMS experiments at the HL-LHC are already manufactured and currently under investigation.

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