250 MHz Multiphase Delay Locked Loop for Low Power Applications

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ABSTRACT

Delay locked loop is a critical building block of high speed synchronous circuits. An improved architecture of mixed signal delay locked loop (DLL) is presented here. In this DLL, delay cell based on single ended differential pair configuration is used for voltage controlled delay line (VCDL) implementation. This delay cell provides a high locking range with less phase noise and jitter due to differential pair configuration. For increasing the acquisition range and locking speed of the DLL, modified true single phase clock (TSPC) based phase frequency detector is used. The proposed design is implemented at 0.18 μm CMOS technology and at power supply of 1.8 V. It has power consumption of 1.39 mW at 125 MHz center frequency with locking range from 0.5 MHz to 250 MHz.

Keyword:
Delay locked loop
Voltage controlled delay line
Differential pair configuration
Phase frequency detector
Charge pump
Loop filter

1. INTRODUCTION

In the era of recent development in deep submicron technologies, requires high operating frequency of VLSI systems and subsystems. High speed ICs require properly synchronized on-chip clock signals for their operation. For clock synchronization operation in microprocessors and memory ICs, delay locked loop (DLL) and phase locked loop (PLL) are used to diminish the effect of jitter and skews of clock signals [1]. In DLL, VCDL is used in place of VCO which makes it differ from PLL. If frequency multiplier operation is not needed then a DLL is preferred over PLL because of high stability, less locking time and no jitter accumulation [2],[3]. DLL has a wide number of applications such as clock generators in DRAM ICs, microprocessors, clock de-skewing circuits [4],[5]. Locking time, lock range and jitter performance, static phase error, low power consumption and immunity against process voltage temperature loading (PVTL) variations are the most important metrics of a DLL. A DLL can be realized by a number of architectures; analog and digital DLLs are the two most important types among them [6]. Analog DLLs have better performance in terms of jitter, layout area, power supply rejection ratio, power consumption and clock skew.

This paper introduces a mixed mode DLL in which single ended differential pair based VCDL is used which provides high stability against temperature and power supply variations. The proposed circuit depicts superior performance in terms of speed, power consumption, and locking range. The organization of remaining four sections are starting with architecture of basic DLL followed by analysis of different blocks, simulation results and conclusion.
2. BASIC DLL

Delay locked loop (DLL) (block diagram is given in Figure 1) is a negative feedback structure, used to produce multiphase clock signals from a single clock signal [7]. A phase shift is developed at each stage by applying input reference clock signal to voltage controlled delay line (VCDL). The phase difference among reference clock signal and output clock signal is detected by phase detector (PD). For adjustment of control voltage of VCDL, the phase error is used by charge pump (CP) with loop filter. Phase error is finally reduced to zero due to negative feedback mechanism which is the indication of locked state and at that time delay of VCDL becomes equal to one clock period. If $\phi_{\text{in}}$ and $\phi_{\text{out}}$ are input and output clock signals respectively and $t_{\text{VCDL}}$ is delay provided by VCDL, the delay provided by DLL can be given by equation (1) as

$$\phi_{\text{out}} = \phi_{\text{in}} + t_{\text{VCDL}}$$

(1)

Figure 1. Block diagram of DLL

2.1. Linear analysis of DLL

For linear analysis, s-domain model of DLL is shown in Figure 2, which includes transfer function of different blocks.

$$\phi_{\text{in}} \xrightarrow{K_{PD}} I_{\text{CP}}/T_{\text{ref}} \xrightarrow{F(s)} K_{\text{VCDL}} \xrightarrow{\phi_{\text{out}}}$$

Figure 2. S domain model of DLL

In this model $K_{PD}$ (radian / second) denotes the phase detector gain. $I_{\text{CP}}(A)$ and $F(s)$ are the current through charge pump and loop filter transfer function, respectively. VCDL gain is given by $K_{\text{VCDL}}$ (radian / V) and it is proportional to the number of delay lines. Input clock signal has the period of $T_{\text{ref}}$ (s). For suppressing the jitter amplification over high frequencies, a second order loop filter is used, then $F(s)$ can be given by equation (2) as

$$F(s) = \frac{R_1 C_1 s + 1}{(R_1 C_2 s + C_1 + C_2) s}$$

(2)

Thus closed loop transfer function of DLL can be specified as

$$\frac{\phi_{\text{out}}(s)}{\phi_{\text{in}}(s)} = \frac{I_p K_{PD} K_{\text{VCDL}} (R_1 C_1 s + 1)}{R_1 C_2 s^2 + [C_1 + C_2 + I_p K_{PD} K_{\text{VCDL}} R_1 C_1 / T_{\text{ref}}] s + I_p K_{PD} K_{\text{VCDL}} / T_{\text{ref}}}$$

(3)
3. DIFFERENT FUNCTIONAL BLOCKS OF PROPOSED DLL

The design and analysis of different functional blocks of DLL i.e. phase detector, charge pump with loop filter and VCDL are discussed in the subsequent subsections.

3.1. Phase frequency detector

Phase detector is the most critical component of DLL. PD generates the phase error information corresponding to the phase difference between VCDL output clock and ref clock signal. Flip-flop based phase detectors are most commonly used because they have no duty cycle dependence problem due to edge detection [8].

Phase frequency detector (PFD) shown in Figure 3 is implemented using modified TSPC flip-flop. This PFD has high acquisition range and locking speed because it can detect both frequency and phase. When reference \(\text{ref}\) and reset signals are low, in the upper flip-flop, node N1 is charged to VDD through transistors M1 and M2. The output node Up is connected to ground through transistors M5 and M6 at the rising edge of the ref signal. When the reset signal goes high, node N1 is disconnected from VDD by transistor M2 and connected to ground by transistor M3. As soon as the node N1 is discharged, the output node is pulled up through transistor M4 [9],[10].

Signals \(\text{Up}\) and \(\text{Down}\) are generated by PFD according to the phase difference between the output signal of VCDL and rising edge of the reference signal. When D input is connected through ground then on the rising edge of the reference signal \(\text{ref}\) and VCDL output, zero is sent to the flip-flops output \(\text{Up}\) and \(\text{Down}\), correspondingly, which makes the output of NOR gate logic high. As D input of flip-flop is connected to output of NOR gate, as a result the signals \(\text{Up}\) and \(\text{Down}\) come again to logic high. When \(\text{ref}\) signal is greater than VCDL, it needs to speed up to pick up; this may leads to add to in the VCDL control voltage which adjusts the VCDL output delay [11].

Figure 3. Schematic diagram of phase frequency detector
Simulation results of phase frequency detector are shown in Figure 4. Total power dissipation by this phase detector is approximately 0.5196 mW.

![Simulation waveforms of PFD](image)

Figure 4. Simulation waveforms of PFD

### 3.2. Charge pump in the company of loop filter

Phase error detected by PFD is transferred to the charge pump in the form of voltage pulses. The CP adjusts the voltage level of loop filter by charging or discharging current and controls the delay of VCDL.

Charge pump which is a bipolar switched current source consists of current source and sink. According to Up and Down signals, output of charge pump is positive and negative current pulses into the loop filter of the DLL. Figure 5 is the schematic of charge pump along with loop filter; where transistor M1 and M4 behave as current source and sink respectively. Middle transistors M2 and M3 are operated as switches for which gate pulses are provided by PFD outputs [10].

Second ordered loop filter basically used to translate the output signal of PFD to control voltage. It filters out jitter at high frequencies so that jitter peaking effect is reduced. Charging or discharging of the capacitor of the loop filter takes place according to the CP output. When locked state is achieved then output of loop filter is almost constant. The Up and Down input voltages and the output of charge pump along with loop filter is shown in Figure 6 [11],[12].
3.3. Voltage controlled delay line

VCDL affects the jitter performance of output clock signal and stability of DLL so it is also a critical block of DLL. In VCDL a number of delay lines are connected in series. In locked state total delay provided by VCDL must be equal to one clock time period ($\tau_{ref}$) or phase shift of 360°. Output swing and delay range are the main design parameters of each delay cell.

Here active load differential pair configuration based delay cell is used for VCDL implementation as shown in Figure 6. It has advantage of both single ended and differential architecture of VCDL delay cell due to...
to which PVTL variations are minimized. In this delay cell inverter operation is performed by transistor M4 which is active loaded by transistor M2. Transistor M3 is a diode connected structure which controls the current flow through the transistor M2 by control voltage ($V_{ctrl}$) variation. In this delay cell only a single NMOS transistor performs inverting operation instead of CMOS configuration, so less parasitic capacitance is present at output which results delay minimization and high operating speed.

Proposed VCDL which consists of four delay cells is shown in Figure 8. At 0.18 $\mu$m CMOS technology delay variation with respect to control voltage is graphically presented in Figure 9 which shows that delay is almost constant at low control voltages and after that it decreases. So gain of VCDL ($K_{VCDL}$) is not so much varied with control voltages due to which DLL output jitter noise is small at larger delays.

Figure 7. Proposed delay cell

Figure 8. Schematic diagram of four stage VCDL
4. SIMULATION RESULTS

Proposed DLL, (Figure 10), is implemented at 1.8V supply voltage and 0.18 μm CMOS technology.

![Functional schematic of designed DLL](image)

Figure 10. Functional schematic of designed DLL

![Simulation waveforms of DLL in locked state](image)

Figure 11. Simulation waveforms of DLL in locked state
It has high operating speed and a good jitter performance as compared to existing delay cells. Performance specifications of proposed circuit are summarized in Table 1. This DLL has 1.3918 mW power consumption and 0.52 ns static phase error at 125 MHz operating frequency. VCDL output clock signal is properly phase aligned with reference clock signal as shown in Figure 11.

| Parameters             | Values                        |
|------------------------|-------------------------------|
| Process technology     | 0.18 μm CMOS                 |
| Supply voltage         | 1.8 V                        |
| Center frequency       | 125 MHz                      |
| Locking range          | 0.5 MHz–250 MHz              |
| Power consumption      | 1.3918 mW at 125 MHz         |
| Architecture           | Single loop                  |

The proposed DLL is also simulated at 0.35 μm CMOS technology and results are also compared with existing DLL. Comparative analysis of different performance parameters of proposed DLL and Multiphase output delay locked loop [13] is done in Table 2. From the table it can be concluded that proposed DLL has better performance in provisos of locking range and power utilization with similar supply voltage and less complex construction.

| Parameters        | Proposed Work | [13]          |
|-------------------|---------------|---------------|
| Center frequency  | 65 MHz        | 100 MHz       |
| Locking range     | 5 MHz–125 MHz | 85 MHz–115 MHz|
| Power consumption | 0.590 mW @ 100 MHz | 3.4 mW @ 100 MHz |

5. CONCLUSION

A high locking range and low power DLL is designed and implemented at 0.18 μm CMOS technology (Also designed at 0.35 μm CMOS technology but showing better performance at 0.18 μm CMOS technology) at which it has total power consumption of 1.3918 mW with very small locked time. Low power specification makes it useful for devices of longer battery life. Proposed DLL circuit performs a proper clock synchronization operation as output clock signal has negligible phase error from input reference clock signal. Layout of the proposed design can be done further for further post layout results.

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