A Novel Class AB CMOS Operational Amplifier

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ABSTRACT

A novel class AB two stage operational amplifier was presented to deal with the problem of the conventional class A two stage operational amplifier’s limited slew rate. The output stage quiescent current was controlled accurately and the slew rate and unity gain bandwidth were enhanced significantly, along with no additional static power dissipation. Simulation results show that the positive and negative slew rates were raised to 35 and 2.2 times and unity gain bandwidth was raised to 5 times when compared with conventional class A operational amplifier.

INTRODUCTION

A novel class AB two stage operational amplifier was proposed in this paper to deal with the slew rate and bandwidth problems of the traditional miller compensation class A CMOS operational amplifier (opamp).

In general, some difficulties accompany the class AB opamps: the output stage quiescent current is difficult to control. To deal with above problems, a new CMOS two stage class AB architecture with accurate control of quiescent current is proposed based on the traditional class A operational amplifier by adding a single resistance to translate the old class A to class AB to increase the slew rate extremely[1]. By the way, a similar cascode frequency compensation is used without additional power and branches through small changes of common active loads.

In this article, traditional two stage operational amplifier is reviewed in the second part. The details of quiescent current control, slew rate and stability are

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analyzed in the third section. Simulations and conclusions will be given in the fourth and fifth section separately.

TRADITION CLASS A TOW STAGE OPERATIONAL AMPLIFIER

The traditional two stage operational amplifier with PMOS input stage is demonstrated in figure 1, where Cc is compensation capacitor, RC is nulling resistance and CL is load capacitor. It has good performance in gain and bandwidth and negative slew rate. But the positive slew rate is very poor because of the limited current of M9, especially with large CL.

A NOVER CLASS AB TWO STAGE OPERATIONAL AMPLIFIER

The proposed novel class AB two stage operational amplifier is shown in figure 2 [2]. The quiescent current is provided through current source Ibias that could be realized by Widlar or peaking current source. Cc is compensation capacitor. Cb and R1 make the output stage obtain the class AB operation.

The Accurately Controlled Quiescent Current And Class AB Operation

In figure 2, The output stage is made up of M8 and M9 and the accurately controlled bias current is provided by Ibias. Assume that Cb and R1 are ignored for the moment, the output stage will have a typical class A structure. Under quiescent condition, a current mirror will arise from M7, M9 and M10 to accurately control the quiescent current with no current flowing through R1.

Node X will swing widely with large input signal. Cb and R1 make a high pass network and its cutoff frequency is smaller than input signal frequency. The voltage

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Figure 1. Traditional Class A CMOS Two Stage Operational Amplifier.

Figure 2. The proposed Novel Class AB CMOS Operational Amplifier.
change of node X will pass to node Y to make the output stage get class AB operation because of Cb acting as a floating battery that derives from the fact that Cb’s voltage couldn’t vary abruptly and Cb can’t charge or discharge through R1.

The value of Cb and R1 is of great concern. The change of node X would not couple to node Y quickly if the cutoff frequency determined by Cb and R1 is larger than input signal frequency. High valued R1 could realize better oscillation, but it could also occupy large area. It can be realized through linear operated and diode connected MOS transistor to save area. Cb is limited by the parasites of node Y. The capacitor of node Y (mainly consist of gate to source capacitor of M9) and Cb make up a capacitor divider, namely \( V_Y = V_X Cb / (Cb + C_Y) \). Small Cb will make an attenuated change couple to Y and \( Cb > 2C_Y \) would be enough for our demand.

Frequency Compensation

It is obvious that the circuit in figure 2 can’t be stable unless frequency compensation is applied. A revised cascode frequency compensation is utilized to improve the stability without introducing the drawbacks of traditional cascode compensation (gain reduction, limited bandwidth, increased power, complex structure) [3].

In figure 2, Cc is compensation element, and the novel active current mirror load is composed of M3~M6 transistors which is different with traditional current mirror. M3 and M4 are designed to operate in saturation region with M5 and M6 in triode region. Through this way, the swing will not change even and small signal resistance will be lifted at node X without increasing supply voltage because of M5 and M6’s insertion. M4 behaves as load and current buffer that inhibits the feed-through path from the first stage to the second one. As a result, the non-dominant pole is shifted towards higher frequency that improves GBW with better power supply rejection ratio (PSRR).

The buffer and cascode frequency compensation has been studied sufficiently in the past so that the detailed small signal analysis process will not be given and only conclusion will be shown below.

Assume that the dominant and non-dominant poles are separated enough, then the DC gain \( A_{dc} \), dominant pole \( p_0 \), non-dominant pole \( p_{nd} \), left-half plane zero \( z \), unity gain frequency \( W_r \) are listed as below.

\[
A_{dc} = g_{m12}(r_{d12} / / g_{m12}r_{d12}r_{d0}) \cdot g_{m3}(r_{d3} / / r_{d9})
\]

\[
1
p_0 \approx \frac{1}{(g_{m8} + g_{m9})g_{m8}(r_{d8} / / r_{d9})Cc(r_{d12} / / g_{m12}r_{d12}r_{d0})}
\]
\[ P_{nd} \approx -\frac{(g_{m8} + g_{m9})Cc}{(Cc + CL)C_{o1}} \]  

(3)

\[ z \approx -\frac{g_{m4}}{C} \]  

(4)

\[ w_f \approx \frac{g_{m1,2}}{Cc} \]  

(5)

The parameters above have their usual physical meanings (\( g_m \) denotes trans conductance and \( r_{ds} \) denotes output resistance of MOS transistors). From (1) to (5) we can draw the conclusion that the DC gain will increase from the increased small signal resistance at node X with the almost same dominant poles and unity gain bandwidth with traditional two stage miller compensation amplifier. The non-dominant pole will increase to maximize the GBW the derives from M8 and M9 ‘s class AB operation.

**SIMULATION AND VERIFICATION**

SMIC 0.18um 1P6M mixed signal process is applied and Spectre simulator is used to simulate and verify the circuits in figure1 and figure 2.

The circuits in figure1 and figure 2 are connected as unity gain with \( V_{dd}=1.8V \), \( I_{bias}=1uA \), \( CL=10pF \). The input signal peak to peak voltage is 0.5V with period of 40us and duty of 50%. The input and output voltage wave are shown in figure 3(a) and figure 3(b). It is obvious that the circuit in figure (1) is severely limited in slew.

![Figure 3](image)

Figure 3. The Input(Dotted) and Output(Solid) Waves of Figure 1(a) and Figure 2(b) Connected as Follower.
Figure 4. Open Loop Response of Figure 1(a) and Figure 2(b).

|                           | Figure 1     | Figure 2     |
|---------------------------|--------------|--------------|
| DC Gain (dB)              | 87           | 97           |
| Unity Gain Bandwidth (MHz)| 0.462        | 2.4          |
| Phase Margin (degree)     | 60           | 83           |
| SR+/SR-(V/us) (V/us)      | 0.08/0.67    | 2.8/1.5      |
| Icc (μA)                  | 4            | 4            |
| Supply Voltage (V)        | 1.8          | 1.8          |
| Power (μW)                | 7.2          | 7.2          |
| Load Capacitor (pF)       | 10           | 10           |
| Compensation Capacitor (pF)| 5            | 1            |
| Nulling Resistance (kΩ)   | 80           | -            |
| R1 (MΩ)                   | -            | >1           |
| Cb(pF)                    | -            | 3            |

rate with SR+=0.08V/us, SR-=0.67V/us. However, the circuit in figure 2 can almost follow the input voltage without overshoot and SR+ =2.8V/us, SR-= 1.5V/us. The positive and negative slew rates rise to 35 and 2.2 times compared with figure 1.

The frequency characteristics of figure 1 and 2 are shown in figure 4(a) and (b). The dc gain, unity gain bandwidth, phase margin are 87dB, 462kHz, 60 degree respectively with compensation capacitor 3pF and nulling resistor 100KΩ compared with 97dB, 2.4MHz, 83degree with 1pF compensation capacitor. It can be drawn that the proposed circuit has improved slew rate greatly with larger dc gain, unity gain bandwidth and smaller compensation capacitor. Some critical specifications are tabulated in table I.
CONCLUSIONS

A class AB two stage CMOS operational amplifier with accurately controlled quiescent current is proposed with detailed analysis of slew rate and stability. Compared with traditional amplifier, the proposed one has raised the positive and negative slew rate 35 times and 2.2 times with the same power consumption. It also increase the phase margin and unity gain bandwidth with performance being verified by simulations.

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