Low-frequency Selection Switch based Cell-to-Cell Battery Voltage Equalizer with Reduced Switch Count

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Abstract—A selection switch based cell-to-cell voltage equalizer requires only one dual-port dc-dc converter shared by all the cells. A cell-to-cell voltage equalizer is proposed that utilizes a capacitively level-shifted Cuk converter and low-frequency cell selection switches. The absence of isolation transformer and diodes in the equalizer leads to high efficiency, and the use of low-frequency selection switches significantly reduces the cost of the drive circuits. A low-frequency cell selection network is proposed using bipolar voltage buses, where the switch count is almost half, compared to the existing low-frequency cell-to-cell equalizers for the case of a large number of cells. A novel approach for cell voltage recovery compensation is proposed, which reduces the number of operations of the selection switches and the equalization time. The proposed equalizer is implemented with relays and verified with an 8-cell Li-ion stack. The developed prototype shows the efficiency of over 90% and good voltage balancing performance during charging, discharging, and varying load conditions. Experimental results also show about one order of magnitude reduction in the number of relay switchings and a significant reduction in equalization time using the proposed voltage compensation.

Index Terms—Cell-to-cell, cell balancing, Cuk converter, DPDT, low-frequency, selection switch, voltage equalizer.

I. INTRODUCTION

The cell voltages in a series-connected battery cell stack become unequal due to manufacturing tolerances, non-uniform aging, and unequal temperature distribution. The differences among the cell voltages increase with the number of charge-discharge cycles, leading to over-charge and over-discharge of some of the cells. A voltage equalizer is essential to improve the charge-capacity and the cycle life of the cell stack by avoiding such a situation. The passive voltage equalizers, which are the simplest and cheapest equalizers, dissipate a significant amount of stored energy [1]. On the other hand, the active equalizers transfer charge from the overcharged cells to under-charged cells to equalize all the cell voltages [2]. The operation of the active equalizers can be of two types: simultaneous equalization of all the cells and serial equalization of the selected cells, as shown in Fig. 1.

The first type of active equalizer uses multiple power converters or a multi-port power converter so that all the cells can take part in voltage equalization simultaneously. These equalizers can be classified into three categories: adjacent cell [3]–[8], multi-cell to stack [9]–[18], and multi-cell to multi-cell [19]–[28] equalizers, among which the multi-cell to multi-cell equalizers offer fastest voltage equalization. Each of these equalizers dedicates one converter port to each cell even though many of the cells in the cell stack may not require voltage equalization at a given point of time. Such dedicated connections result in a higher component count, under-utilization of converter components, and the requirement of many high-frequency isolated gate drivers.

The second type of active equalizer uses only one dual-port dc-dc converter shared by all the cells to reduce the component count and several selection switches for cell selection. When the number of cells increases, the dc-dc converter’s component count remains the same, and only the number of selection switches increases. The charge transfer method in these equalizers is either cell-to-stack or cell-to-cell. The cell-to-stack equalizers [29]–[38] selects only one cell is at a time, and charge transfer takes place between that cell and the entire cell stack. On the other hand, cell-to-cell equalizers [39]–[45] achieve a direct charge transfer from the most overcharged cell to the most under-charged cell. Thus, the cell-to-
cell equalizers offer about twice the equalization speed, but they require twice as many selection switches.

As the number of selection switches is proportional to the number of cells, any simplification or cost-reduction of the selection switches and their drive circuits is valuable in case of a higher number of cells in the stack. As discussed in Section II of this paper, a MOSFET, switched at a high-frequency, requires a complex gate-driver, which is often costlier than the MOSFET itself in case of low-power applications. Hence, the cell-to-stack equalizers in [33]–[38] and cell-to-cell equalizers in [43]–[45] have been proposed with low-frequency selection switches so that simpler drive circuits can be used. This work aims to propose a Low-Frequency Selection Switch based Cell-to-Cell (LFSSCC) voltage equalizer with high efficiency, simple implementation, and lower switch count. The advantages of the proposed equalizer compared to existing LFSSCC equalizers [43]–[45] are discussed below.

The dual-port dc-dc converters in [43], [44] use diodes with significant conduction loss and transformer with higher high-frequency losses and size, leading to lower conversion efficiency and increased equalizer size. The dc-dc converter in [45] achieves high-efficiency by achieving soft-switched operation with a higher component count. Thus, the dc-dc converters in the existing LFSSCC equalizers suffer from lower efficiency or higher circuit complexity. This work uses a capacitively level-shifted bidirectional Cuk converter, originally proposed for a multi-cell to multi-cell topology in [19]. The equalizer in [19] uses one closed-loop controlled Cuk converter for each cell, leading to a high component count and control requirements. On the other hand, this work uses only one Cuk converter for a large number of cells, reducing circuit complexity and control effort significantly. Thus, this converter is more suitable for a cell-to-cell equalizer and offers simpler implementation and high efficiency, as no transformer or diode is required in the conduction path. Section III discusses the converter topology.

The LFSSCC equalizers [43]–[45] can use either low-frequency switched MOSFETs or relays as selection switches. The selection switch networks in these equalizers require 2n Double Pole Double Throw (DPDT) switches for n series-connected cells. These switches can be implemented with either 8n low-frequency MOSFETs or 2n DPDT relays. This work proposes a low-frequency selection switch network with (n+2) DPDT and 2 SPST switches, leading to a significant reduction in the number of switches and drive circuits.

The voltage drop in cell impedance causes cell voltage recovery after equalization current is stopped. This voltage recovery leads to error in detecting end-of-equalization and a large number of switching of the selection switches. For a low-frequency selection switch based equalizer, a higher number of switching leads to longer equalization time and lower reliability. Different methods to reduce the number of selection switching are proposed based on voltage drop estimation [36], [44] and self-learning fuzzy logic based method [37]. These methods require additional computation resources and cell charge-discharge characteristics. A simpler method with cell voltage recovery compensation, which does not require charge-discharge characteristics, is proposed to reduce the number of switchings of selection switches significantly.

This work in the enhanced version of the work published in [46] with additional theoretical explanations and experimental results. Section IV explains the proposed low-frequency cell selection network, and Section V discusses the proposed cell voltage recovery compensation. Sections VI and VII provides a comparison with existing equalizers and experimental validation of the proposed equalizer respectively.

II. DRIVE CIRCUITS FOR SELECTION SWITCHES

If a selection switch is operated at high frequency, it is implemented with MOSFETs. In contrast, a low-frequency selection switch is implemented with either MOSFETs or relay with significantly simpler and cheaper driver circuits.

1) High-Frequency MOSFET Drive Circuit: A high-frequency switched MOSFET for cell selection requires isolated gate driver IC, capable of providing a peak current of a few Ampere to achieve quick turn-on and turn-off, as shown in Fig. 2(a). Such a driver IC requires an isolated power supply and is often costlier than a low-power MOSFET.

![Fig. 2. (a) High-frequency gate driver for MOSFET, (b) low-frequency gate driver for MOSFET, (c) driver for relay.](image-url)

2) Low-Frequency MOSFET Drive Circuit: Longer turn-on and turn-off times are acceptable for a low-frequency switched MOSFET. The gate drive resistor $R_g$ is in the order of a few kilo-Ohms, and the driver needs to supply only a few milli-Ampere peak current. Thus, a low-cost digital isolator can replace the costly gate driver IC, as shown in Fig. 2(b).

3) Relay Drive Circuit: The driver circuit for a relay is simpler and cheaper than a MOSFET driver. Fig. 2(c) shows a relay driver, which requires a signal MOSFET $S$, a gate resistor $R_g$, and a free-wheeling diode $D$. These components have to carry only a few tens of milli-Ampere peak current, leading to a very low-cost implementation compared to high-frequency MOSFET drivers.

Thus, the use of low-frequency selection switches reduces the complexity and cost of the equalizer significantly.

III. DC-DC CONVERTER TOPOLOGY

The capacitively level-shifted Cuk converter allows variable voltage difference between the input and output ports’ reference terminals without using any isolation transformer. This converter is used here to transfer charge from the most over-charged cell to the most under-charged cell, as shown in Fig. 3.

This converter has an additional capacitor $C_2$ compared to a conventional bidirectional Cuk converter to block the voltage difference between the grounds of the two ports. Using KVL
polarity reversal is required for each pair of voltage rails when match with the converter port polarities, two DPDT relays voltage rails. In case the polarities of the voltage rails do not thus, each common node can effectively be connected to two switches to select two cells at a time. One DPDT switch is selection network, which uses one SPST switch and

A. Proposed Cell Selection Network

Fig. 4(a) shows the proposed low frequency cell-to-cell selection network for bipolar voltage rails to reduce the polarity. This work proposes a new low-frequency cell-to-cell equalizers. The existing LFSSCC equalizers for a large number of cells.

Let’s consider that the selected cells are the kth and the lth cell, where k > l. Then, the kth cell is connected to port 1 and the lth cell is connected to port 2 with following steps,

- Turn on Spol1 if k is even.
- Turn on Spol2 if l is even.
- Turn on Sshort if the kth and the lth cells are adjacent.
- Turn on Sk, Sh−1, Sl, and Sh−1.

The selection network’s operation is explained here for eight cells in two different equalization situations, as shown in Fig. 5. The red lines indicate the current flow paths.

1) Two non-adjacent cells: Fig. 5(a) shows the current flow path between two non-adjacent cells, cell 2 and cell 7. The switches S1, S2, S6, and S7 are turned on to connect the cells to the converter ports. The polarity reversal switch Spol2 is turned on to ensure correct polarity connection.

2) Two adjacent cells: Fig. 5(b) shows the current flow path for two adjacent cells, cell 4 and cell 5. The switches S3, S4, S5, and Spol2 are turned on to connect cell 5 to port 1 and cell 4 to port 2 with the correct polarity. As the cell 4 and cell 5 are adjacent, their common node should be connected to the negative terminal of port 1 and positive terminal of port 2. This is achieved by turning on the shorting switch Sshort.

The corresponding cell is even-numbered. In the case of two adjacent cells, the common node is connected to both converter ports by an SPST switch Sshort. Thus, the proposed selection network requires (n + 2) DPDT and 2 SPST switches, and the selection switch count is reduced to almost half compared to the existing LFSSCC equalizers for a large number of cells.

IV. LOW-FREQUENCY CELL-TO-CELL SELECTION NETWORK

In an LFSSCC equalizer topology, it is possible to connect the dc-dc converter between any two cells at a time to achieve power transfer between them. The existing LFSSCC equalizers [43]–[45] require 2n DPDT switches to implement such a cell selection network for n series-connected cells, as shown in Fig. 4(a), where the voltage rails a, b, c, and d are of fixed polarity. This work proposes a new low-frequency cell-to-cell selection network with bipolar voltage rails to reduce the selection switch count.

A. Proposed Cell Selection Network

Fig. 5(b) shows the proposed low frequency cell-to-cell selection network, which uses one SPST switch and n DPDT switches to select two cells at a time. One DPDT switch is used here to connect each common node between two adjacent cells to a voltage rail. However, each voltage rail is switched to a second rail if an upstream DPDT switch is turned on.

Fig. 4. Schematic diagram of the low-frequency cell selection network in (a) existing and (b) proposed cell-to-cell equalizers.

Each inductor connected to the input or output port is split into two coupled inductors to make the circuit symmetric for reducing common mode oscillation. A more detailed discussion on the converter topology is provided in [46]. A PI controller controls the cell current in one of the converter ports in closed-loop. The converter is enabled when at least one cell voltage is out of the acceptable voltage range.

For a predetermined tolerance voltage Vtol and the average cell voltage Vavg, the kth cell voltage Vbk is in the acceptable voltage range if it satisfies the following condition,

\[ V_{avg} - V_{tol} \leq V_{bk} \leq V_{avg} + V_{tol} \quad \text{for all } k \in [1, n] \quad (2) \]

In Fig. 3 and assuming small voltage ripple, the voltage of the capacitors \( C_1 \) and \( C_2 \) are given by,

\[ V_{C1} = \sum_{j=l}^{k} V_{kj} \quad \text{and} \quad V_{C2} = \sum_{j=l+1}^{k-1} V_{kj} \quad (1) \]

Fig. 3. Schematic diagram of the capacitively level shifted Cuk converter connected to two cells of the stack.

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Lets consider that the selected cells are the kth and the lth cell, where \( k > l \). Then, the kth cell is connected to port 1 and the lth cell is connected to port 2 with following steps,

- Turn on \( S_{pol1} \) if \( k \) is even.
- Turn on \( S_{pol2} \) if \( l \) is even.
- Turn on \( S_{short} \) if the kth and the lth cells are adjacent.
- Turn on \( S_k, S_{k-1}, S_l, \) and \( S_{l-1} \).

The selection network’s operation is explained here for eight cells in two different equalization situations, as shown in Fig. 5. The red lines indicate the current flow paths.

1) Two non-adjacent cells: Fig. 5(a) shows the current flow path between two non-adjacent cells, cell 2 and cell 7. The switches \( S_1, S_2, S_6, \) and \( S_7 \) are turned on to connect the cells to the converter ports. The polarity reversal switch \( S_{pol2} \) is turned on to ensure correct polarity connection.

2) Two adjacent cells: Fig. 5(b) shows the current flow path for two adjacent cells, cell 4 and cell 5. The switches \( S_3, S_4, S_5, \) and \( S_{pol2} \) are turned on to connect cell 5 to port 1 and cell 4 to port 2 with the correct polarity. As the cell 4 and cell 5 are adjacent, their common node should be connected to the negative terminal of port 1 and positive terminal of port 2. This is achieved by turning on the shorting switch \( S_{short} \).
Fig. 5. Current flow paths between (a) the 2nd and the 7th cell, (b) the 4th and the 5th cell in the proposed low-frequency selection network.

B. Implementation of Selection Switches

The low-frequency selection switches can be implemented with MOSFETs or relays as discussed below.

1) DPDT switch for cell selection: Fig. 6(a) and (b) show the off and on states of the DPDT switches $S_1$ to $S_n$. Each switch blocks the voltages $V_{P1,T1b}$, $V_{P2,T2a}$ in on-state, and $V_{P2,T2a}$ in off-state. Fig. 4 and Fig. 5 show that $V_{P1,T1b}$ is bipolar and $V_{P2,T2a}$ are unipolar. Hence, the DPDT switch can be implemented with four MOSFETs, as shown in Fig. 6(c). Alternatively, it can also be implemented with a DPDT relay.

2) DPDT switch for polarity reversal: Fig. 7(a) and (b) show the off and on state of the polarity reversal DPDT switches $S_{pol1}$ and $S_{pol2}$. The voltage between each pole to each of its throw is positive or zero in off-state. The voltage between a throw and corresponding pole is positive or zero in on-state. The current in the DPDT switch is bi-directional. Hence, the DPDT switch can be implemented with a DPDT relay or four MOSFETs as shown in Fig. 7(c).

3) SPST switches: The SPST switches block unipolar voltages, and each of them can be implemented with an SPST relay or a MOSFET.

Thus, the proposed selection switch network can be implemented with $(n+2)$ DPDT and 2 SPST relays or with $(4n+10)$ MOSFETs.

V. CELL VOLTAGE RECOVERY COMPENSATION

When the discharging of a cell is stopped, the cell voltage $V_b$ recovers to a higher voltage after some time. Similarly, when the cell’s charging is stopped, $V_b$ falls and settles to a lower voltage. This recovery in $V_b$ is often modeled as a voltage drop across the cell impedance. Ideally, when the cell’s equalization is complete, $V_b$ should settle within the acceptable voltage band. However, if the cell’s equalization is stopped when $V_b$ reaches within the acceptable voltage band, $V_b$ settles outside of the band due to voltage recovery. Thus, further rounds of equalization for the same cell are necessary, resulting in a higher number of switching of the selection switches.

The control algorithm for a low-frequency cell selection network provides a small amount of time-gap, usually 10s to 30s for Li-ion cell, between two switching transitions for allowing the cell voltages to settle before selecting the next pair of cells for equalization. This time-gap helps to avoid high-frequency switching of the selection switches during transients in cell voltages. The measured cell voltages in low-frequency cell-to-stack [34], [38] and cell-to-cell [45] equalizers show the voltage recovery effect and resulting high number of charge or discharge rounds of each cell. Due to slow switching transitions and time-gap between transitions, a higher number of switchings leads to a longer equalization time.

Several attempts have been made to consider the effect of the cell voltage recovery within the equalization algorithm to avoid a higher number of switchings of selection switches. Estimation of the impedance drop [36], [44] and self-learning fuzzy logic based method [37] have been employed for this purpose. The impedance drop estimation methods are computationally intensive. The self-learning fuzzy logic algorithm requires additional computation resources and prior knowledge of charge-discharge characteristics. A cell voltage recovery compensation is proposed here to reduce the number of switchings of the selection switches. The proposed method is computationally simpler than the impedance drop estimation.
methods and the fuzzy logic method. It does not require any prior knowledge of the charge-discharge characteristics of the cells.

The cell voltage recovery effect is explained here with an example of an under-charged cell. The equalization strategy is to charge the cell so that its voltage becomes equal to the average voltage of all the cells. The equalizer charges the under-charged cell with current $I$ from time $t_1$ to $t_2$. Fig. 8 shows the cell voltage and current. At the beginning of charging at $t_1$, $V_b$ rises from $V_1$ and mostly settles within a short time $\Delta t$. However, the cell voltage continues to increase slowly after time $(t_1 + \Delta t)$ due to the charging of the cell. The charging is stopped at $t_2$ when the cell voltage is $(V_2 + V_{rcv})$. The cell voltage $V_b$ then settles to voltage $V_2$. Thus, if the cell charging is stopped when $V_b$ reaches the average voltage $V_{avg}$, then $V_b$ settles to $(V_{avg} - V_{rcv})$.

Hence, the equalizer should charge an under-charged cell until $V_b$ reaches $(V_{avg} + V_{rcv})$, so that $V_b$ settles to $V_{avg}$ after charging is stopped. Similarly, it should discharge an over-charged cell until $V_b$ reduces to $(V_{avg} - V_{rcv})$. However, the estimation of $V_{rcv}$ with internal battery parameters requires significant computation efforts and often suffers from estimation error. In this work, the change in $V_b$ in time $\Delta t$ from the start of the charging is measured and stored in memory as $V_{imp}$. The voltage $V_{imp}$ is used as an estimate of $V_{rcv}$. However, $V_{rcv}$ is a function of cell condition and, hence, the use of $V_{imp}$ as an estimate of $V_{rcv}$ will have a lower error when the time duration $(t_2 - t_1)$ is small.

The cell voltage recovery compensation based algorithm in this work charges an under-charged cell till its voltage reaches $(V_{avg} + V_{imp})$ and discharges an over-charged cell till its voltage reduces to $(V_{avg} - V_{imp})$. If the initial cell voltage $V_1$ is not close to the final cell voltage $V_2$, then $(t_2 - t_1)$ is large and $V_{imp}$ is not a good estimate of $V_{rcv}$. However, $V_b$ comes close to the acceptable voltage range after the first round of equalization and requires further charging or discharging for a shorter duration. In the second round of equalization, $(t_2 - t_1)$ is small and $V_{imp}$ is a good approximation of $V_{rcv}$. Thus, $V_b$ settles within the acceptable voltage range within a few rounds of equalization.

VI. COMPARISON OF CELL-TO-CELL SELECTION NETWORKS

A comparison of the component count and efficiency of the proposed equalizer with the existing LFSSCC equalizers, presented in Table I, shows that it can work with a lower number of selection switches compared to other LFSSCC equalizers. It can also be observed that the proposed equalizer achieves higher efficiency than [43], [44] with similar complexity of the dc-dc converter, which is significantly simpler than [45]. Thus, the proposed method achieves above 90% efficiency with simple circuit implementation.

Table II compares the proposed LFSSCC equalizer with different types of existing equalizers. The followings can be observed from the comparison of component counts, driver requirements, efficiency, equalization speed, and voltage difference dependence,

1) Although the adjacent cell and multi-cell equalizers can work with a lower number of MOSFETs, they require a large number of passive components and high-frequency isolated gate drivers.

2) The equalization current in the adjacent cell and multi-cell equalizers, except [22], is proportional to the cell voltage differences. Thus, these equalizers become less effective when the voltage difference is not large, especially in Li-ion cells, where even a large difference in SOC results in a small voltage difference. The work in [22] achieves voltage difference independence by controlling each of the cell currents simultaneously, leading to higher sensor and computation cost.

3) The proposed equalizer offers similar component counts, driver requirements, and efficiencies compared to low-frequency cell-to-stack equalizers, but achieves twice as fast equalization.

4) A relay-based implementation offers the lowest component count and driver requirements.

VII. EXPERIMENTAL RESULTS

An 8-cell prototype is developed to validate the proposed low-frequency selection switch cell-to-cell (LFSSCC) equalizer using DPDT relays as the selection switches. Table III provides the ratings of the equalizer components, and Fig. 9 shows the image of the developed prototype. The prototype is tested with eight 3.6 V, 2.6 Ah Li-ion cells [47] to verify the converter operation, equalizer efficiency, and the control algorithm. The current of the cell connected to port 1 of the converter is controlled to 0.5 A, and the equalization algorithm decides its direction based on cell voltages.
TABLE I
COMPARISON OF THE PROPOSED EQUALIZER WITH THE EXISTING LOW-FREQUENCY SELECTION SWITCH CELL-TO-CELL (LFSSCC) EQUALIZERS.

| Topology      | Type of selection switch | Number of components | Efficiency (%) |
|---------------|--------------------------|----------------------|----------------|
|              |                          | Selection switch network | Dc–dc converter |
|               |                          | MOSFET | DPDT relay | SPST relay | MOSFET | Capacitor | Inductor | Transformer | Diode |          |
| Ref. [43]    | MOSFET | 8n    | 0        | 0          | 1        | 2        | 0        | 1          | 1      | 59.4           |
|               | Relay   | 0      | 2n       | 0          |          |          |          |            |        |                |
| Ref. [44]    | MOSFET | 8n    | 0        | 0          | 2        | 2        | 0        | 1          | 2      | 85.3 to 89.5   |
|               | Relay   | 0      | 2n       | 0          |          |          |          |            |        |                |
| Ref. [45]    | MOSFET | 8n    | 0        | 0          | 5        | 2        | 2        | 0          | 5      | 98.6 to 99.5   |
|               | Relay   | 0      | 2n       | 0          |          |          |          |            |        |                |
| Proposed     | MOSFET | 4n+10 | 0        | 0          | 2        | 2        | 2        | 0          | 0      | 90.1 to 92.9   |
|               | Relay   | 0      | n+2      | 2          |          |          |          |            |        |                |

TABLE II
COMPARISON OF THE PROPOSED LOW-FREQUENCY SELECTION SWITCH CELL-TO-CELL (LFSSCC) EQUALIZER WITH OTHER TYPES OF EQUALIZERS.

| Topology | Type of Equalizer | Number of components | Number of drivers | Efficiency (%) | Equalization speed | Voltage difference dependent |
|----------|-------------------|----------------------|-------------------|----------------|---------------------|-----------------------------|
|          |                   | Semiconductor        | Relay Passives    |                |                    |                             |
|          |                   | MOSFET | Diode | DPDT | SPST | Cap. | Ind. | Trans. |               |
| Ref. [7] | Adjacent cell resonant-tank | 2n   | 0     | 0    | 0 | 2n-1 | n-1 | 0 | 2n | 0 | 98.2 | Low | Yes |
| Ref. [18]| Multi-cell to stack multi-winding trans. | n+1 | 0 | 0 | 0 | 2n+1 wind. | n+1 | 0 | 94.8 | Moderate | Yes |
| Ref. [27]| Multi-cell to multi-cell switched capacitor | 2n | 0 | 0 | 0 | n+1 | 0 | 94.8 | Moderate | Yes |
| Ref. [22]| Multi-cell to multi-cell dual-active bridge | 3n | 0 | 0 | 0 | 2n | 0 | 0 | 94.5 | Excellent | No |
| Ref. [36]| Cell-to-stack MOSFET based cell-selection | 4n+2 | 2 | 0 | 2 | 4n | 0 | 92.0 | Moderate | No |
| Ref. [38]| Cell-to-stack Relay based cell-selection | 1 | 1 | 0 | 2n | 2 | 2 | 0 | 1 | 2n | - | Moderate | No |
| Proposed | MOSFET based cell-to-cell | 4n+12 | 0 | 0 | 2 | 2 | 0 | 2 | 4n+10 | 90.1-92.9 | Good | No |
|          | Relay based cell-to-cell | 2 | 0 | n+2 | 2 | 2 | 2 | 0 | n+2 |          |          |          |

*Note: Cap.: Capacitor, Ind.: Inductor, Trans.: Transformer, wind.: winding, n represents the number of cells.

TABLE III
CIRCUIT COMPONENTS AND PARAMETERS OF THE PROPOSED EQUALIZER
PROTOTYPES BASED ON RELAYS.

| Component/parameter     | Ratings/part no.     |
|-------------------------|----------------------|
| Switching frequency     | 30 kHz               |
| Inductances in port 1: \(L_1, L_1', M_1\) | 62.5 \(\mu\)H, 0.7 A |
| Inductances in port 2: \(L_2, L_2', M_2\) | 62.5 \(\mu\)H, 0.7 A |
| Capacitors: \(C_1, C_2\) | 50 \(\mu\)F, 50 V |
| MOSFETs: \(Q_1, Q_2\) | BSC009NE2L51 |
| SPST relay              | OJE-SH-124LMH        |
| DPDT relay              | RT424024             |
| Wait time for \(V_{imp}\) measurement, \(\Delta t\) | 20 s |

A. Operation of Cuk Converter

Fig. 10 shows the measured current and voltage waveforms of the capacitively level-shifted Cuk converter in the prototype to verify the converter operation. The measured current waveforms show that the port 1 current is 0.5 A, and the peak-to-peak ripple present in each of the port currents is 100 mA. Fig. 10(c) shows the measured capacitor voltages for the case when cell 1 and cell 4 are selected for equalization. It can be observed that the capacitor \(C_1\) blocks the total voltage of 4 cells, and \(C_2\) blocks that total voltage of 2 cells, as expected theoretically in (1). The measured voltage ripples in \(V_{C1}\) and \(V_{C2}\) in Fig. 10(d) show peak-to-peak ripples of 20 mV for both of the capacitors.

The efficiency of the prototype is measured for different output powers up to 2 W and is plotted in Fig. 11. Fig. 11 shows that the prototype has a maximum efficiency of 92.9% and an efficiency of 90.1% at the rated power.

B. Voltage Convergence Test

The performance of the equalizer and its control algorithm with the proposed cell voltage recovery compensation is tested on an 8-cell stack under rest condition, and Fig. 12(a) shows the measured cell voltages. The maximum voltage difference...
The same test is performed without the cell voltage recovery compensation to verify the necessity of this compensation, and Fig. 12(b) shows the measured cell voltages. The initial cell voltages are close to those of the previous test for a proper comparison. The equalizer takes about 130 minutes in this case to converge the cell voltages within a band of 30 mV. Thus, the voltage convergence time is 30% longer when the cell voltage recovery compensation is not used. It can also be observed from Fig. 12(a) and (b) that the number of switchings of the relays is significantly lower when cell voltage recovery compensation is employed. For example, the highest switched relay’s number of switching transitions is reduced from 166 to only 18 using the compensation. The reduction of the number of switchings significantly improves the life and reliability of the relays.

C. Dynamic Performance of the Equalizer

The equalizer’s performance is tested during the charge-discharge cycle of the eight-cell Li-ion stack, and Fig. 13 shows the cell voltages. The cell voltages are initially unbalanced, with the maximum difference among them being 160 mV. The cell stack is discharged from this condition at 0.5 C-rate until the cell voltages reach 3 V. The cell stack is then subjected to constant current (CC) charging at 0.5 C-rate and constant voltage (CV) charging at 4 V. Once, the CV charging is finished the stack is discharged once again.

is 200 mV at the beginning. All the cell voltages converge within an acceptable voltage band of 20 mV in 100 minutes.
at 0.5 C-rate. It can be observed from the voltage plot that the equalizer equalizes the initially unbalanced cell voltages during the first discharge and maintains these voltages within 20 mV voltage band. Once the cell voltages are equalized, the equalizer is disabled. However, on the course of charging and discharging, one or two cell voltages occasionally gets out of the 20 mV voltage band the equalizer is enabled again, as observed near 115, 170, 180, and 190 minutes of Fig. 13. Fig. 14 also shows that a very few switchings of the relays are required to maintain the cell voltages within the 20 mV band after the initial voltage difference is mitigated.

The performance of the equalizer is also verified under variable load conditions. Fig. 14 shows the load current variation and the corresponding cell voltages. It can be observed that a sudden change in current often produces unbalance in cell voltages, and the equalizer is activated to eliminate this unbalance. The equalizer is also activated when any cell voltage is out of the 20 mV voltage band during constant current discharging between two step-changes in current, as observed near 65 and 70 minutes of Fig. 14. Thus, the proposed equalizer meets performance requirements under different practical operating conditions.

VIII. CONCLUSION

A cell-to-cell voltage equalizer with low-frequency selection switches is proposed based on a capacitively level-shifted Cuk converter. The avoidance of an isolation transformer and diodes for the proposed equalizer’s operation helps achieve high efficiency. The use of low-frequency selection switches with simple drive circuits in the proposed equalizer leads to lower component count and cost. A low-frequency cell-to-cell selection network is proposed with bipolar voltage buses. This reduces the number of selection switches to almost half compared to the existing low-frequency selection networks for a large number of cells. A comparison of the proposed equalizer with the existing LFSSCC equalizers shows its advantages in terms of switch count, drive circuit requirements, and efficiency. An 8-cell prototype of the proposed equalizer is implemented with relays, and the operation of the capacitively level-shifted Cuk converter is experimentally verified. The developed prototype shows an efficiency above 90% over its entire power range and a peak efficiency of 92.9%. The equalizer is shown to successfully converge the voltages of eight Li-ion cells within a voltage band of 20 mV from an initial voltage imbalance of 200 mV. The prototype shows good voltage balancing performance under different conditions such as constant current charging, constant voltage charging, constant current discharge, and varying load. A cell voltage recovery compensation scheme is proposed that estimates the voltage recovery due to cell impedance to reduce the number of switchings and the total equalization time. Experimental results show that the proposed compensation leads to the voltage convergence in a shorter time with about one order of magnitude reduction in the number of relay switchings. Thus, the proposed equalizer offers cell-to-cell voltage equalization with lower circuit complexity, component count, and good performance.

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