Area-Power Analysis of Carry Select Adder using Transmission gates

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Abstract: The main building block of microprocessors, microcontrollers, and digital signal processors is an arithmetic logic unit (ALU). The performance of ALU depends on its adder design. The Carry Propagation Delay (CPD), area and power are the important metrics in the structure of the adder. In this work, area and power analysis of carry select adder are presented. In this adder, the CPD is minimized with the common Boolean logic. The power and area of the adder are optimized by replacing CMOS gates with transmission gates. In this technique, the transistor count is greatly reduced from 987 to 512 for a 16-bit carry select adder. In addition, the power consumption is minimized from 0.63mW to 0.018mW and the power delay product is minimized from 0.53mW-ns to 0.021mW-ns.

Keywords: Arithmetic unit, Low-powerr, carry propagation delay, transmission gates

1. Introduction

For any arithmetic, unit addition is the basic mathematical operation. The extensively used operation has been classified as part of a range of real-time signal processing for general-purpose processors. The traditional carry select adder (CSLA) is a double RCA system that produces some words as an input-carry (Cin =1and 0) approximate pair and output carry bit sand select one of every pair for the final-output-carry and final-sum [1]. There is less Carrying Propagation Delay than the RCA in a traditional CSLA, however, the architecture is not desirable since it utilizes a double RCA. Just several efforts were required to prevent the double usage RCA in the CSLA structure. Instead of two RCAs where a multiplexer (MUX) is used for the add-on circuit [2] utilised, one RCA and one add-on circuit. A square-root (SQRT)-CSLA was proposed[3] for the development of wide bit-width adders less of delay. In a square-root-CSLA, CSLAs are related to increased size in the cascading system. The primary objective of the Square root-CSLA structure is to have a parallel route to the carrying propagation of that assists reduce the total adder delay. A binary CSLA based on BEC was suggested [4]. The BEC-based CSLA requires less logical resources than the traditional CSLA, but there is a slightly greater delay. In [5] and [6], a common Boolean logic-based CSLA is also suggested. The CSLA [7] based on CBL contains considerably less conceptual resources than in the traditional CSLA, and it also has a greater CPD, that is nearly equivalent to the RCA. SQRT-CSLA based on CBL was suggested in [8] to solve this problem. However, the architecture of the CBL-based SQRT CSLA [9] needs certain logic and latency than for the BEC-based square-root-CSLA [10]. All the obsolete logic found in the standard CSLA[1] has been eliminated.

On an extensive study on carrying propagation and generation within the Carry select adder. For the reduction of carrying propagation, we are suggesting carry select scheme in the adder design. In this paper, location-delay-power enriched CSLA is proposed to reduce carrying propagation delay.
The article is structured as follows; the topology of the adder is described in Section II. Section III explains the proposed area power-efficient CSLA design. Section IV employs a comparison of CSLA adder with the proposed scheme. Section V concludes.

2. Different Adder Topologies

A. Ripple Carry Adder (RCA)

Single-bit full-adders are cascaded for construction of the ripple carry adder [11]. Each full-adder prior carrying-out signals is ready in the RCA, then only begins its computation. In a carrying ripple adder, the carry-out propagation direction, therefore, specifies the critical path delay. As shown in Figure 1, For a full-adder N-bit, The essential paths in the full-adders are N-bit carrying propagation paths. The delay time in the N-bit RCA increases linearly as the N-bit increases. The time delay in the N-bit RCA can be represented as:

$$TRCA = T_{sum} + (N-1) T_{carry}$$  \hspace{1cm} (1)

![Figure 1. Construction of N-bit RCA using N number of full-adders](image)

B. Carry Select Adder (CSLA)

To reduce the linear dependency between the time of computation period and the input bit length for adder improvement, the carry select adder [4] is used. M sections of carrying ripple adders are designed for the carry select adder, while each section contains a duplicate (N / M)-bit RCA pair, as shown in Figure 2 as N= 4 and M= 16.

![Figure 2. Schematic of CSLA](image)

This repeated RCA pair is required to carry both probable input values, where the first RCA is calculated as the logic ’0’ is the carrying input value and the second ripple carry is calculated as the logic ’1’ is the carrying input value. If the definite carrying data is ready, the output of carrying the ’0’ path or the outcome of carrying the ’1’ pair is chosen according to its carrying input value by the path multiplexer Figure 3 demonstrates an illustration of a 5-bit adder for the carry set. The begin of the each M component RCA pair need not waiting for the arrival of the prior segment carrying input to anticipate potential input carrying values in advance. As a result, each M element RCA pair in the CSLA will compute parallel.

The critical path in the traditional bit-N RCA architecture is bit-N carrying path propagation plus one unit of description generation. Instead, with one description generation unit, the key deliverables in the N-bit CSLA is (N / M)-bit carrying propagation route plus M phase multiplexer.
As \( M \) is much shorter than \( N \) and the multiplexer delay in the maximal adder is smaller, the computational delay in the CSLA is much shorter than in the RCA. Even so, compared to the RCA, the realization of the adder with the replicated carry production circuit costs nearly twice the components and twice the energy efficiency. Thus, we mentioned an area-efficient CSLA in this article. By sharing CBL, the logic is streamlined, using transmission gates to enhance power and field. In this process, several transistor counts can be saved and a lower PDP can be achieved. The delay time in the N-bit CSLA is:

\[
T_{CSA} = T_{\text{sum}} + T_{\text{setup}} + M T_{\text{mux}} + (N/M) T_{\text{carry}}
\]

3. Proposed Adder Design

An area-efficient CSLA is suggested in this paper.
- Logic is simplified by the common Boolean logic being shared.
- Area and power are optimized using Transmission gates.

A. Construction of CSLA

On Through analyzing the single-bit full-adder truth table, We will notice that the summary signal output as the carrying-input signal is logic "0" as the carrying-in signal is logic "1" is the complement signal itself. The suggested area-efficient CSLA design in Figure 4 is the sharing of the general Boolean logic in the sum generating unit.

We only had to develop one XOR gate with one INVERTER to generating the summation signal set to share the general Boolean logic. If the carrying-input is ready, as per the logical state of the carrying-input signal, we can select the accurate summation output. As for the carry propagation path, to anticipate potential input carrying values in advance, we create one AND and one OR gate. Until the carrying-input signal is ready, as per the logical state of the carrying-input signal, the correct carry-out can be chosen. We may hold both the summation generation unit of the INVERTER gate, the XOR gate, the AND and OR gate carry-out unit of generation in parallel in this process. Since we still retain part of the traditional CSLA parallel construction, we can still retain some speed.
competition. On the way, in the traditional CSLA, we do not need to prepare the replicate adder cells, which will greatly minimize the transistors count and lower the power efficiency.

For the suggested 16-bit area-efficient CLSA, the delay time is:

\[ T_{\text{proposed}} = T_{\text{setup}} + (16-1) T_{\text{mux}} + T_{\text{sum}} \] (3)

Although the speed is slightly slower compared to the standard CLSA because the parallel path is less complex in our design. However, lower fuel, lower area consumption, and lower PDP can be achieved. Speed can be improved as compared to the ripple carry adder because many of the parallel construction is retained in the standard CLSA. The delay time is approximately equivalent to the bit number N in the suggested adder configuration, so the multiplexer delay time is lower than those of a full adder. Consequently, with almost the equal transistor count, almost the equal power usage, but with lower PDP and higher speed compared to the RCA, the area-efficient adder can work.

B. Power optimized CSLA using Common Boolean Logic

To simplify difficult and complicated logical functions utilizing a limited range of complementary transistors, the CMOS TG uses TGL. Using NMOS as well as PMOS [1], the conundrum of the low logic level is solved. A simple switch with a small resistance and capacitance ratio with less logic is the transmission gate. Also, this gate's DC characteristic is autonomous of input stages. It is constructed by connecting through the drain to the source terminal of NMOS and PMOS transistors to the drain and source. Since the NMOS transistor allows for stronger signal '0' and PMOS transistors allow for stronger signal '1' against the output, the authorization signals reverse each transistor on-off.

![Transmission gate and Symbol](image)

Figure 5 (a) Transmission gate (b) Symbol

The voltage on the A input is a logic one, and the active-low A input is added to Logic zero. It allows the ON state of each transistor and transmits the signal from X to Y. Once the voltage is a Logic zero on active-low input A, and Logic 1 is added to input A, turning every transistor OFF and having each X and Y a high impedance state. The schematic diagram (Figure 5(a)) contains the absolute labels for X and Y so if the label has been reversed, the circuit would work identically. Although not degrading the input signal, this design offers reciprocal properties. In standby mode, the circuit's leakage capacity is calculated. This illustrates how much energy is lost by the entire circuit if there is no input during the OFF state. The power of leakage is a result of supply voltage and current leakage [7]. The basic leakage power equation is shown in Eq. Oh. (4).

\[ P_{\text{Leak}} = I_{\text{Leak}} \times V_{\text{DD}} \] (4)

Implementation of XOR using conventional CMOS and Figure 6 shows the transmission gate.
Figure 6. XOR Gate (a) Convention CMOS (b) Transmission Gate

From figure 6 the delay performance of conventional CMOS and Transmission Gate are compared by considering one unit gate delay. The area and delay estimation for 1 Bit Full adder is depicted in table I.

| Adder      | Area | Delay |
|------------|------|-------|
| XOR Gate   | 4    | 2     |
| 2:1 MUX    | 4    | 2     |
| Full Adder | 8    | 4     |

Table 1. Comparison of Area, delay of 1 Bit Full adder

4. Performance Analysis of Adders

We analyzed and compared the performance of the proposed CSLA with RCA and CSLA. It simplifies the simplification of redundant logic CSLA design and partial sharing of logical circuits will make the CSLA most power-efficient and area-efficient. Table II summarizes the output catalogue of power, PDP, delay, transistor count. This work was developed using Verilog HDL. Using Xilinx 14.1, it is simulated and synthesized.

As compared with the CSLA, delay and power efficiency in suggested CLSA can be improved. However, the number of transistors is marginally increasing. The transistor count in the RCA is 448 for a 16-bit adder. In the suggested area-efficient CSLA, the transistor count is 512, which only increases by 7 percent. The transistor count, however, is 987 in the traditional CLSA, which increases approximately twice. We can save a lot of power in terms of power consumption by removing unnecessary logic and unnecessary signal switching using common Boolean logic term sharing. Figure 8 shows a comparison of adders.

Table 2. Comparison of Area, delay and Power Dissipation of adders

| Adder     | Power (mW) | Transistors | Delay (ns) | PDP (mW.ns) |
|-----------|------------|-------------|------------|-------------|
| RCA       | 1.86       | 448         | 2.62       | 4.87        |
| CSLA      | 0.63       | 987         | 0.85       | 0.53        |
| Proposed  | 0.018      | 512         | 1.2        | 0.021       |

Figure 7. Comparison of adders.

5. Conclusion

An area delay power-efficient CLSA is suggested in this paper. By using the popular Boolean logic number of the transistor are reduced from 987 to 512. By using transmission gates leakage current can be greatly reduced. Hence power requirement is drastically reduced from 0.63mW to 0.018mW. The proposed CSLA design, however, includes less region, delay and dissipation of power than the CSLA.
presented in[12]. This adder is ideally suited to the arithmetic unit of many data processing processors due to the small carrying performance delay. The results of the synthesis show that approximately a percent improvement in PDP is given by the proposed adder.

References

[1]. Mohanty, B. K., & Patel, S. K. 2014, Area–delay–power-efficient carry-select adder IEEE transactions on circuits and systems II: express briefs 61(6), 418-422
[2]. Pravalika, K., & Prasad, C. R. 2018, Fault-Tolerant Parallel Filters Based on ECC Codes. Advances in Computational Sciences and Technology 11(7), 597-605
[3]. Chandrakasan, A. P., et.al, 2008, Ultralow-power electronics for biomedical applications. Annual review of biomedical engineering 10
[4]. Pravalika, K., & Prasad, C. R. 2018, Fault-Tolerant Parallel Filters Based on ECC Codes. Advances in Computational Sciences and Technology 11(7), 597-605
[5]. Chakradhar, A., MD Hameed Pasha, and G. Shravan Kumar. Low Power Area Efficient Counter Using Pulse Triggered Flip-Flop
[6]. Kavitha, M., Prasad, C. R., & Ahmed, S. M. Vedic multiplier for RC6 Encryption Standards Using FPGA.
[7]. Bedrij, O. J. 1962, Carry-select adder IRE Transactions on Electronic Computers 3, 340-346
[8]. B. Parhami 2010, Computer Arithmetic: Algorithms and Hardware Designs, 2nd ed. New York, NY, USA: Oxford Univ. Press.
[9]. Kareemoddin, M., Kumar, A. A., & Ahmed, S. M. 2013, Design of low power comparator for SAR ADC in biomedical applications IJIRCE 1(5), 1161-1167
[10]. Masood, S., Shamshi, M. A. H., & Ahmed, S. M. 2017, An Efficient, Cost-Effective, All-Optical Implementation of Reversible Fast Adder Using Mach-Zehnder Interferometer Based Switches. ICRTEEECT 23-28
[11]. O. Bedrij 1962, Carry Select Adder IRE Trans. on Electronic Computers 11, 340-346
[12]. J. M. Rabaey 2003, Digital Integrated Circuits IEEE Trans. on VLSI Systems