Unveiling the Real Performance of LPDDR5 Memories

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ABSTRACT
LPDDR5 is the latest low-power DRAM standard and expected to be used in various application fields. The vendors have published promising peak bandwidths up to 50% higher than those of the predecessor LPDDR4. In this paper we evaluate the best-case and worst-case real bandwidth utilization of different LPDDR5 configurations and compare the results to corresponding LPDDR4 configurations. We also show that an upgrade from LPDDR4 to LPDDR5 does not always bring a bandwidth advantage and that some LPDDR5 configurations should be avoided for specific workloads.

CCS CONCEPTS
• Hardware → Dynamic memory; • Computing methodologies → Simulation evaluation.

KEYWORDS
LPDDR5, LPDDR4, DRAM, Bandwidth

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1 INTRODUCTION
The latest low-power DRAM standard LPDDR5 [9] was released by JEDEC in 2019. In the meanwhile, LPDDR5 has gradually replaced its predecessor LPDDR4 [8] and is used in various markets including mobile, automotive, AI and 5G [1]. However, since the standard comes with lots of changes including a completely new clocking scheme, the memory controllers also have to be largely redesigned. Thus, many companies are faced with the decision of whether to upgrade their existing system designs or continue with the well-established predecessor for their target applications. However, taking such a decision on the basis of performance numbers by DRAM vendors is difficult as they usually only publish peak bandwidths [3, 5–7, 11]. The real bandwidth utilization can vary significantly for different workloads and DRAM device configurations [2, 13].

Therefore, we conduct a simulation-based performance evaluation of different LPDDR5 configurations to sequential and random accesses, which are the best-case and worst-case input patterns with respect to bandwidth utilization. In addition, we vary the ratio of read and write requests and compare the results to the performance of corresponding LPDDR4 configurations. Finally, we derive several key observations to aid the selection of a suitable memory subsystem. All our experiments are carried out with the cycle-accurate DRAM simulation framework DRAMSys [12]. The remaining paper is structured as follows: Section 2 gives an overview of the LPDDR5 standard and its innovations compared to the predecessor. Section 3 describes the setup used for evaluation before the simulation results are presented in Section 4. Finally, Section 5 concludes the paper.

2 LPDDR5 OVERVIEW
As with every new JEDEC standard release also LPDDR5 enhances the most important DRAM key parameters, i.e., bandwidth, storage capacity and power consumption. LPDDR5 devices can operate at data rates up to 6400 MT/s\(^1\) compared to 4266 MT/s for LPDDR4. Since the clock signal would contribute a considerable amount to the total power at such high data rates, LPDDR5 devices use a slower continuously running command clock and a faster data clock that is disabled during idle times. Depending on the data rate the ratio between both clock signals can either be set to 2:1 (up to 3200 MT/s) or 4:1. To compensate for the slow command clock, commands are now transmitted at double data rate. While an LPDDR4 channel is always comprised of 8 banks, LPDDR5 introduces three different bank modes, which can be selected at power-up. For data rates up to 3200 MT/s a channel is comprised of 16 banks by default (16B mode). For higher data rates these 16 banks are divided into 4 bank

\(^1\)The latest revision of LPDDR5 (called LPDDR5X) even specifies data rates up to 8533 MT/s.
groups (called BG mode). Alternatively, a mode with 8 banks (8B mode) can be chosen where two internal banks are merged to form a single bank with double the capacity visible at the interface. This mode is supported at all data rates. The prefetch for 16B and BG mode is 16n with a default burst length of 16 and an optional burst length of 32. With 8B mode enabled the prefetch is increased to 32n and the burst length is also fixed to 32. One constraint of the BG mode in combination with burst length 32 is that the data is transmitted over the bus in an interleaved fashion, i.e., it is divided into two halves with a gap in between.

### 3 EVALUATION

For an extensive performance evaluation all possible data rates, bank modes (16B/BG/8B) and burst lengths (BL16/BL32) are taken into consideration. The simulated LPDDR5 devices have a density of 16 Gb and a single channel with a width of 16 bits, while the density of the LPDDR4 devices is only 8 Gb but with an identical channel configuration. For LPDDR5 speed grades up to 3200 MT/s the 2:1 clocking ratio is selected, for higher speed grades the ratio is changed to 4:1. All devices are operated with per-bank refresh. The controller uses a first-ready, first-come-first-serve (FR-FCFS) scheduler [10], 64-entry read and write queues and a row-column-bank (bank group) address mapping. As input stimuli either sequential or random traffics are considered. In addition, the ratio between read and write requests is either set to 0.5 (same number of reads and writes) or 1.0 (only reads). For sequential traffic the open-page policy is chosen, for random traffic the closed-page policy [4].

### 4 RESULTS

For sequential input traffic (see Figures 1a and 1b) we observe that irrespective of the burst length and bank mode both LPDDR4 and LPDDR5 devices achieve bandwidths very close to the theoretical maximum (data rate · data bus width). Only for the highest data rates and traffic with mixed reads and writes the bandwidth slightly drops up to a maximum of around 8.5% (LPDDR5 with BL16), which is still a very reasonable result for a single-rank memory channel. The main reasons for the low performance drop are the large number of row hits and the use of per-bank refresh, which allows refresh operations to be executed in the background with blocking only one or two banks and not the whole device at once. Thus, the results also show that for target data rates below 4266 MT/s an upgrade from LPDDR4 to LPDDR5 does not bring any advantage at all from a bandwidth perspective.

For random input traffic, however, the experiments reveal an entirely different behavior. With a burst length of 16 LPDDR4 cannot keep up the bandwidth utilization at all and already starts to saturate at data rates of 1600 MT/s, which is only around one third of the maximum (see Figure 1c). At the highest data rate 4266 MT/s the device only achieves 33% of the maximum theoretical bandwidth for mixed traffic and 35.5% for pure read traffic. The reason for the poor results is the low bank parallelism of LPDDR4. LPDDR5, on the other hand, comes with 16 banks and therefore keeps the bandwidth utilization up also at higher data rates. However, at the transition from the 2:1 to 4:1 clock ratio (dotted line between 3200 MT/s and 3733 MT/s) the bandwidth drops significantly and only reaches the previous peak bandwidth again at data rates of 6400 MT/s. This behavior has two main reasons. First, with 4:1 clocking the command bus operates at very low frequencies compared to the data bus and a burst of length 16 only occupies the data bus for two cycles in relation to the command clock. With random traffic, each access is usually a row miss, which translates into an activate command and a read/write command with auto-precharge. For LPDDR5 these two commands take a total of three clock cycles on the command bus. Thus, the command bus occupation limits the bandwidth utilization to 66% of the upper limit. Second, the low frequency leads to strongly overestimated timings because analog values have to be rounded to a multiple of one command clock cycle.

When doubling the burst length from 16 to 32 both LPDDR4 and LPDDR5 perform significantly better, since the number of row misses per time unit is halved. LPDDR4 and LPDDR5 in 8B mode show a similar behavior (saturation at 3200 MT/s) with a slight advantage for LPDDR4 because of its shorter timings (especially write recovery time) and less rounding. LPDDR5 in 16B/BG mode keeps the bandwidth close to the maximum even up to the highest data rate for pure read traffic and still reaches 67% of the maximum bandwidth for mixed traffic due to the higher bank parallelism.

The results can be summarized in the following key observations:

- For sequential traffic an upgrade from LPDDR4 to LPDDR5 only brings an advantage from a bandwidth perspective if data rates above 4266 MT/s are targeted.
- For random traffic and a burst length of 16 the 4:1 clock ratio of LPDDR5 should be avoided.
- For random traffic LPDDR5 in 16B/BG mode achieves much higher bandwidths than LPDDR4.
- For random traffic the burst length should be selected as high as possible.

### 5 CONCLUSION

In this paper we have analyzed the real bandwidth utilization of different LPDDR5 configurations and compared the results to the predecessor LPDDR4. We found out that for workloads with sequential traffic upgrading from LPDDR4 to LPDDR5 is not always worth it, while for random traffic LPDDR5 outperforms its predecessor in most cases. For future work we plan to extend the evaluation to a full-system simulation setup and analyze the performance of LPDDR5 for real application benchmarks.

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### REFERENCES

[1] Wendy Ehsaner and Nikos Nikolaou. 2020. Adding LPDDR5 support to DRAMCtrl. https://www.gem5.org/2020/05/27/memory-controller.html. last access 2022-08-25.
[2] Sangata Ghose, Tianshi Li, Nastaran Hajinazar, Damla Senol Cali, and Onur Mutlu. 2019. Demystifying Complex Workload-DRAM Interactions: An Experimental Study. 93–93.
[3] Kyung-Soo Ha, Chang-Kyo Lee, Dongkeon Lee, Daesik Moon, Hyong-Ryol Hwang, Dukha Park, Young-Hwa Kim, Young Hoon Son, Byongwook Na, Seungseob Lee, Youn-Sik Park, Hyuck-Joon Kwon, Tae-Young Oh, Young Sool Sohn,
Figure 1: Real Bandwidth Utilization of LPDDR4/LPDDR5 Configurations for Different Input Traffics

Seung-Jun Bae, Kwang-Il Park, and Jung-Bae Lee. 2020. A 7.5 Gb/s/pin 8-Gb LPDDR5 SDRAM With Various High-Speed and Low-Power Techniques. *IEEE Journal of Solid-State Circuits* 55, 1 (2020), 157–166. https://doi.org/10.1109/JSSC.2019.2933396

[4] A. Hansson, N. Agarwal, A. Kolli, T. Wensisch, and A.N. Udipi. 2014. Simulating DRAM controllers for future system architecture exploration. In *Performance Analysis of Systems and Software (ISPASS), 2014 IEEE International Symposium on*. 201–210. https://doi.org/10.1109/ISPASS.2014.6844484

[5] SK hynix Inc. 2021. SK hynix Starts Mass-production of LPDDR5 Mobile DRAM with Industry’s Largest Capacity. https://news.skhynix.com/sk_hynix_starts_mass-production_of_lpddr5_mobile_dram_with_industrys_largest_capacity/. last access 2022-08-25.

[6] Micron Technology Inc. 2020. Micron Readies World’s First Multichip Package With LPDDR5 DRAM for Mass Production. https://investors.micron.com/news-releases/news-release-details/micron-readies-worlds-first-multichip-package-lpddr5-dram-mass. last access 2022-08-25.

[7] Chang-Kyo Lee, Hyung-Joon Chi, Jin-Seok Hae, Jung-Hwan Park, Jin-Hun Jang, Dongkeon Lee, Jae-Hoon Jung, Dong-Hun Lee, Dae-Hyun Kim, Kihan Kim, Sang-Yun Kim, Dukha Park, Youngil Lim, Geuntae Park, Seung-Jin Lee, Seungki Hong, Dae-Hyun Kwon, Han-Hyeong Na, Kyung-Ryun Kim, Seok-Kyu Choi, Hyein Choi, Hang-Jung, Won-II Ba, Jeong-Don B, Seung-Jun Bae, Nam Sung Kim, and Jung-Bae Lee. 2021. An 8.5-Gb/s/12-Gb LPDDR5 SDRAM With a Hybrid-Bank Architecture, Low Power, and Speed-Boosting Techniques. *IEEE Journal of Solid-State Circuits* 56, 1 (2021), 212–224. https://doi.org/10.1109/JSSC.2020.3017775

[8] Jedic Solid State Technology Association. 2014. Low Power Double Data Rate 4 (LPDDR4) JESD209-4.

[9] Jedic Solid State Technology Association. 2019. Low Power Double Data Rate 5 (LPDDR5) JESD209-5.

[10] Scott Rixner, William J. Dally, Ujval J. Kapasi, Peter Mattson, and John D. Owens. 2000. Memory Access Scheduling. In *Proceedings of the 27th Annual International Symposium on Computer Architecture (Vancouver, British Columbia, Canada) (ISCA ’00)*. ACM, New York, NY, USA, 128–138. https://doi.org/10.1145/339647.339668

[11] Samsung. 2018. Samsung Electronics Announces Industry’s First 8Gb LPDDR5 DRAM for 5G and AI-powered Mobile Applications. https://news.samsung.com/global/samsung-electronics-announces-industrys-first-8gb-lpddr5-dram-for-5g-and-ai-powered-mobile-applications. last access 2022-08-25.

[12] Lukas Steiner, Matthias Jung, Felipe S. Prado, Kirill Bykov, and Norbert Wehn. 2020. DRAMSys4.0: A Fast and Cycle-Accurate SystemC/TLM-Based DRAM Simulator. In *Embedded Computer Systems: Architectures, Modeling, and Simulation*. Alex Oraloglou, Matthias Jung, and Marc Reichenbach (Eds.). Springer International Publishing, Cham, 110–126.

[13] Lukas Steiner, Matthias Jung, and Norbert Wehn. 2021. Exploration of DDR5 with the Open-Source Simulator DRAMSys. In *MBMV 2021 - 24. Workshop Methoden und Beschreibungsprachen zur Modellierung und Verifikation von Schaltungen und Systemen*. 31–41.