DTNN: Energy-efficient Inference with Dendrite Tree Inspired Neural Networks for Edge Vision Applications

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Abstract

Deep neural networks (DNN) have achieved remarkable success in computer vision (CV). However, training and inference of DNN models are both memory and computation intensive, incurring significant overhead in terms of energy consumption and silicon area. In particular, inference is much more cost-sensitive than training because training can be done offline with powerful platforms, while inference may have to be done on battery powered devices with constrained form factors, especially for mobile or edge vision applications. In order to accelerate DNN inference, model quantization was proposed. However previous works only focus on the quantization rate without considering the efficiency of operations. In this paper, we propose Dendrite-Tree based Neural Network (DTNN) for energy-efficient inference with table lookup operations enabled by activation quantization. In DTNN both costly weight access and arithmetic computations are eliminated for inference. We conducted experiments on various kinds of DNN models such as LeNet-5, MobileNet, VGG, and ResNet with different datasets, including MNIST, Cifar10/Cifar100, SVHN, and ImageNet. DTNN achieved significant energy saving (19.4\times and 64.9\times improvement on ResNet-18 and VGG-11 with ImageNet, respectively) with negligible loss of accuracy. To further validate the effectiveness of DTNN and compare with state-of-the-art low energy implementation for edge vision, we design and implement DTNN based MLP image classifiers using off-the-shelf FPGAs. The results show that DTNN on the FPGA, with higher accuracy, could achieve orders of magnitude better energy consumption and latency compared with the state-of-the-art low energy approaches reported that use ASIC chips.

1. Introduction

DNN outperforms many other methods in machine learning because of its human level performance in various kinds of application fields [30, 35, 2]. In particular, convolutional neural networks (CNN) have achieved state-of-the-art results on many computer vision problems, including object detection and image classification [22, 34].

In general, computations on DNN model consist of two parts, comprising of training NN model and inference using the trained model. However, both of the two parts are memory and computation intensive especially for CNN with deep depth. In order to facilitate NN computation, powerful Graphic Processing Units (GPUs) are adopted to train the DNN model [5]. However, GPUs are not suitable for inference especially when deployed in embedded systems to cope with real-world applications such as mobile applications and Internet of Things (IoT), which requires both low power and real-time speed [37, 24, 20, 11].

In order to accelerate DNN for efficient inference, various kinds of techniques are proposed. This includes model quantization that compresses network models so as to accelerate DNN inference [20, 6, 45, 41, 43, 38, 3]. Quantization of weights and activation can significantly reduce compute and storage overhead for efficient inference. Researchers from IBM even achieve 4-bit training with low accuracy loss [38]. However, radical quantization such as binarization of neural networks usually result in severe accuracy degradation [24, 21, 33]. To ensure the accuracy, researchers work towards pushing the bit width of the weight and activation to its limit without compromising the accuracy. The state-of-the-art work found that 3-bit to 6-bit is an optimal bit width range for both weight and activation to ensure accuracy and performance [41, 43]. However, even with low bit width weight and activation, weight memory access and costly arithmetic operations such as multiplication and addition are inevitable, which leads to considerable energy consumption and hardware footprint, hindering the deployment of edge AI. Therefore, in order to facilitate the deployment of neural network on embedded system and mobile applications, test-time inference without accuracy degradation that can totally
elicites the power hungry weight access and arithmetic operations is favored.

In this paper, we propose DTNN, which takes both model quantization and efficiency of operations into consideration. Inspired by the tree structure of the dendrite in neural cells and the model quantization technique, DTNN achieves energy-efficient inference by replacing multiply-and-add (MAC) operations with table lookups. Unlike traditional quantized model, in our DTNN design, weight could maintain the full bit width such as 32-bit or 64-bit, while only activation needs to be quantized, which makes DTNN not prone to accuracy drop. With full bit width weight and low-bit activation, our DTNN achieves comparable accuracy with the full bit width baseline. Meanwhile, by implementing nodes in tree structure with look-up tables, both costly weight access and compute-intensive arithmetic computations are eliminated in inference.

We conduct experiments from small to large DNN models ranging from LeNet-5, MobileNet to VGG, and ResNet. In order to show the scalability of DTNN, we test it with different datasets, including MNIST, Cifar10/Cifar100, SVHN, and ImageNet. According to the experiment results, DTNN achieves significant energy savings. With negligible loss of accuracy, it achieves 19.4× and 64.9× energy improvement on ResNet-18 and VGG-11 with ImageNet, respectively. To further validate the effectiveness of DTNN and compare with state-of-the-art low energy implementation for edge vision, we design and implement DTNN based MLP image classifiers using off-the-shelf FPGAs. The results show that DTNN on the FPGA could achieve orders of magnitude better energy consumption and latency compared with the state-of-the-art low energy approaches reported that use ASIC chips. Specifically, at the higher accuracy, our DTNN based image classifier running on FPGA consumed 1.13 nJ per image, or about 0.42% of the 268 nJ per image reported for IBM’s TrueNorth chip. In addition to such a high energy efficiency, DTNN on FPGA is five orders of magnitude faster than TrueNorth.

The contribution of this paper has four aspects:

1. Proposing DTNN for efficient inference by using efficient lookup operations to replace costly multiplication and addition.

2. Proposing activation-only quantization to support DTNN while ensuring accuracy.

3. Leveraging tree structure to enable efficient lookup operation in DTNN.

4. Achieving orders of magnitude improvement in energy consumption and latency compared with the state-of-the-art works.

2. Related Work

In order to alleviate the computation and energy demand, model compression technique is proposed, which includes three major methods: pruning, quantization, and weight sharing [8, 12, 39, 21, 20, 6, 45, 41, 43, 13, 15, 25, 42]. In quantization, the precision of the weights and the activations are decreased. In order to further reduce the computation cost of the models, more radical quantization methods are proposed such as BNN [20]. Binarization of both weights and activations reduces memory size and access, but results in severe accuracy degradation [24]. Therefore, researchers are working towards pushing the bit width limits without compromising the accuracy. In addition, many works propose model compression method specifically target to energy consumption of hardware [41, 44]. Wang et al. [41] first manually set a constraint of energy consumption and then explore the quantization policy under this predefined constraint. Yang et al. [44] specifically prune the weights that are energy-consuming estimated by hardware. The previous studies reduce the memory size and access and simplify the arithmetic operation by minimizing the bit width of weight and activations, but the weight access is still unavoidable and multiple bit width weight and activations incur multiplication and addition which limits the performance of the inference.

SNN approach is well known for its high energy efficiency due to its spike-based input/output, asynchronous computation/communication, and Non von Neumann architecture in hardware implementation [26, 11, 32]. It consumes energy only when there are spike events, which results in high energy efficiency. Dedicated chips are designed and fabricated for SNN such as TrueNorth and Tianjic [28, 32]. Using the TrueNorth platform, Esser et al. demonstrated the network that achieves the state-of-the-art energy efficiency for digit recognition [10].

Unlike the methods mentioned above, our proposed DTNN is a hardware-friendly neural network that is inspired by the bio-structure of the dendrite in neural cells. By taking advantages of model quantization and using much more energy- and latency-efficient lookup operations to replace the multiplication and addition, our DTNN could achieve orders of magnitude better energy consumption and latency compared with traditional state-of-the-art efficient inference design.

3. Method

3.1. Efficiency of different operations

As shown in Table 1, among the different kinds of operations, memory accesses consume the most energy. Floating point (FP) multiplication and addition operation consume nearly three orders of magnitude higher energy than a 6-input 1-output lookup operation. Fig. 1a shows a typical neural
network layer in a neural network. From a computation perspective, assuming that both weights and the activation are in full precision, the computation involved to compute $Y$ is the multiplication-accumulation (MAC) operation, which is the core operation in conventional artificial neural networks (ANN). If both weight and activation are binarized, then it is the binarized neural networks [7], which brings benefit to hardware implementation but results in severe accuracy degradation. If we leave weight with full precision and make activations binarized, then the training and output of computation in the neural network layer are both constrained to only two possible values (e.g. -1 or 1). With such a situation, the operations involved becomes additive accumulation (ACC). This is more efficient than MAC but is still costly because of the additions, and more importantly, of the memory accesses.

However, if we view the computation with binary digits inputs and output as a lookup operation as shown in Fig. 1b, then the situation can be completely different. A lookup table (LUT) of size $b2^n$ can implement any Boolean function whose $n$ inputs and $b$ outputs are binary digits [27]. It is the heart of the logic in field-programmable gate arrays (FPGAs), which has high reconfigurability and becomes a popular mean for verifying logic designs before ASIC fabrication. The key idea of DTNN is to use efficient lookup operation to replace costly floating point or fixed point multiplication and addition in inferences. We use a neuron unit with six binary digits inputs and a single binary digit output as an example to show how efficient it can be. Namely, in

![Diagram of neural network](https://example.com/diagram.png)

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### 3.2. Dendrite-tree inspired neural networks

In this section, we shall describe the structure of our proposed DTNN in detail. One of the key advantages of DTNN is that many of the state-of-the-art techniques, such as model compression with pruning, can be applied to DTNN.

#### 3.2.1 D-tree neuron

In neural network models, the basic building block is a neuron. In this section, we shall describe a general dendrite-tree inspired neuron unit we call a D-tree neuron that in theory can be used to approximate any neural network model. A quantized version of this is what is used to build DTNN.
A traditional neuron in the first hidden layer with \( n \) where \( x \) layer act as inputs to the next inner layer and so on. The function realized by the neuron with \( n \) inputs is shown in Eqn. 1:

\[
y = f \left( \sum_{i=0}^{n-1} w_i x_i + b \right),
\]

where \( x_i \) and \( y \) represent the input and output of the neuron, and \( w_i \) and \( b \) are the weights and bias respectively. The function \( f \) is a nonlinear activation function, such as rectified linear unit (ReLU) or a hyperbolic tangent function (Tanh). A traditional neuron in the first hidden layer with \( n \) inputs is shown as dark circles in Fig. 2a.

The Dtree neuron, designed to solve the large fan-in problem is shown in Fig. 2b. It is inspired by a biological neuron that utilizes a “tree” structure, the “dendrite,” to handle the large amount of inputs. Its biomorph is shown in Fig. 2c. Instead of connecting all the inputs to the neuron directly, the Dtree neuron uses a tree with intermediate neurons (inner neurons) that are organized as inner layers. Thus, Fig. 2b is the counterpart of the traditional neuron in Fig. 2a, both having \( n \) inputs and one output. The fan-in of each node in the tree structure can vary, but for simplicity, we constrain the maximum fan-in number to be \( i \). With this configuration, for a neuron with \( n \) inputs, the number of inner layers is \( \left\lfloor \log_i n \right\rfloor = L \), excluding the input layer. The number of nodes for the first inner layer is \( \left\lfloor \frac{n}{i} \right\rfloor = a \), and each of them has a fan-in of \( i \), except for the last node, which has \( n \mod i \) inputs. Subsequently, the outputs of first inner layer act as inputs to the next inner layer and so on. The function realized by the dendrite-tree inspired neuron is shown in Eqn. 2,

\[
y = f_{L-1} \left( \sum_i w_i^{(L-1)} \cdot f_{L-2} \left( \sum_j w_j^{(L-2)} \cdot \cdots \right) + b_{L-1} \right) + b_{L-2} \right) + b_{L-1},
\]

where \( w_i^{(L-1)}, w_i^{(L-2)}, \) and \( w_0^{(L)} \) are the weights in the inner layers, from the last inner layer all the way to the first inner layer. Similarly, \( b_{L-1}, b_{L-2}, \) and \( b_0 \) are the biases of the inner layers, and \( f_{L-1}, f_{L-2}, \) and \( f_0 \) are activation functions of the inner layers, from the last inner layer to the first inner layer. Note that the activation functions can be different for each inner layer.

A neural network can be viewed as a function that maps input features to outputs. The following lemma gives us the basis for approximating a traditional NN using Dtree neurons.

**Lemma 3.1.** Given a function that represents a traditional neuron with weights and bias, \( y = f \left( \sum_i w_i x_i + b \right), \) where \( w_i, b \in \mathbb{R} \) and \( f \) is an activation function, there exists weights, biases, and activation functions for a Dtree neuron that computes the same function.

**Proof.** Assume the traditional neuron has \( n \) inputs, and the function it can realize is of the form in Eqn. 1. Rewriting Eqn. 1, we get the equation shown below:

\[
y = f(W + b),
\]

\[
W = \sum_i w_i x_i.
\]

For an \( n \) input Dtree neuron with \( L \) inner layers, all the functions that it can represent are shown by Eqn. 2. We perform the following transformations on it: 1) set \( f_{L-1} \) to
Pointwise Convolution would act like a traditional neuron. We call this type of neuron the Type-I Dtree neuron. For the Type-II Dtree neuron, we can see that the activation function of the inner layers are the same as the neuron in this work. According to the lemma, as long as the number of weights is $n$, whereas for the $n$-input Type-II Dtree neuron, with $m$ as the fan-in number of each node in the tree structure, the number of weights is denoted by $N_D$, where

$$N_D = n + n \left(1 - \left(\frac{1}{m}\right)^{\log_m n}\right)$$

Although the weights of DTNN are in full precision, the quantization of activation would still result in the information loss. Fortunately, according to previous work, activations that are in 3-bit to 5-bit width range are sufficient to ensure accuracy in actual networks [41].

3.2.2 DTNN based fully connected and convolutional layer

In order to realize DTNN based neural networks, we just need to replace conventional neuron in NN by Dtree neuron. For fully connected layer, it is quite straightforward. For convolutional layer, we use MobileNet as an example to demonstrate how to build a DTNN based CNN. MobileNet [19] is inspired from the depthwise separable convolutions [4]. The regular convolution operations are replaced by the point-wise and depthwise convolutions, which could reduce large amount of MAC operations. As shown in Fig. 3, MobileNets stack multiple “depthwise – pointwise” blocks repeatedly. By replacing conventional neuron in MobileNet with Dtree neuron, we get DTNN based MobileNet, which is also shown in Fig. 3.

3.3. Input pre-processing

As DTNN belongs to quantized neural networks, there are two methods to feed in the input data. We use an image classification application as an example. In Method 1, a normal convolution layer is employed that takes as its input the high precision image. With this method, the first layer have to be implemented using traditional floating point processing unit, which incurs extra pre-processing cost in terms of energy and hardware resources.

In Method 2, in order to achieve ultra low energy consumption, we directly binarize the input pixel to binary values, which involves negligible pre-processing effort.
an input $x$, and output $y$, is simply

$$y = \begin{cases} 
1 & x > \text{threshold}, \\
0 & \text{otherwise}. 
\end{cases} \quad (6)$$

The threshold can be learnt or be preset. Details are given in Section 4.5. Please note this radical method does not work well for large models with large datasets due to considerable information loss.

### 4. Experiment

#### Datasets and models.

In this section, we will present experimental results of DTNN on various kinds of DNN models such as LeNet-5, MobileNet, VGG, and ResNet with different datasets, including MNIST, Cifar10, SVHN, and ImageNet. LeNet-5 is a simple neural network with only two neural layers [23]. MobileNet is a compact model with depth-wise and point-wise convolution, which is designed specifically for mobile vision application [19]. VGG is a standard model with conventional convolution and fully connected layers [36]. ResNet is a classical neural network used as a backbone for many current computer vision tasks [16]. It is featured with residual connections to prevent gradient from vanishing.

#### Training settings.

We conduct experiments using quantization-aware training in Pytorch [31]. For the MNIST and CIFAR10/Cifar100 dataset, the training takes a total of 220 epochs with a batch size of 512. The initial learning rate is set to 0.004 and then divided by 2 every 30 epochs. An Adam solver is adopted with betas=(0.9, 0.999), eps=10^{-8}, and a weight decay of 10^{-3}. For the SVHN dataset, the training takes a total of 70 epochs, and the rest of training settings are the same with MNIST and CIFAR10/Cifar100. For ImageNet, the training takes a total of 90 epochs with a batch size of 64. The initial learning rate is set to 0.1 and then divided by 10 at every 30 epochs. A SGD solver with momentum set at 0.9, and a weight decay of 10^{-4} was used.

#### 4.1. DTNN results on a small model, LeNet-5, with MNIST

Table 3 shows Accuracy and energy (uJ) numbers of DTNN based LeNet-5 with different bit width of activation implemented by lookup operations and ANN based LeNet-5 by conventional multiplication and addition for MNIST.

| Metrics | 4-bit | 5-bit | 6-bit | 32FP |
|---------|-------|-------|-------|------|
| Acc.    | 99.14%| 99.32%| 99.18%| 99.10%|
| Energy  | 0.5411| 0.5416| 0.5441| 40.73 |

Table 4 shows Accuracy of DTNN based ResNet-18 with different bit width of activation implemented by lookup operation and its ANN counterpart by conventional FP multiplication and addition.

| Dataset      | 3-bit | 4-bit | 5-bit | 6-bit | 32FP |
|--------------|-------|-------|-------|-------|------|
| Cifar10      | 88.8% | 92.4% | 92.7% | 93.1% | 93.0%|
| Cifar100     | 65.5% | 71.3% | 72.3% | 72.9% | 73.0%|
| SVHN         | 92.8% | 95.6% | 96.3% | 96.3% | 96.2%|
| ImageNet     | 57.9% | 67.1% | 69.6% | 70.3% | 69.8%|

Table 5 shows energy (uJ) of DTNN based ResNet-18 implemented by lookup operation and ANN based ResNet-18 by multiplication and addition in inference for one image.

| Dataset      | 4-bit | 5-bit | 6-bit | 32FP |
|--------------|-------|-------|-------|------|
| Cifar10/SVHN | 31.46 | 125   | 569.2 | 1.08 × 10^4 |
| Cifar100     | 31.46 | 125   | 569.3 | 1.09 × 10^4 |
| ImageNet     | 613   | 900   | 2.26 × 10^3 | 1.75 × 10^4 |

Table 6 shows results on another standard DNN model, VGG-11, with different datasets.

| Dataset      | 4-bit | 5-bit | 6-bit | 32FP |
|--------------|-------|-------|-------|------|
| Cifar10      | 64.5% | 69.5% | 71.0% | 70.4%|
| Cifar100     | 686.9 | 1.85 × 10^3 | 7.38 × 10^3 | 1.20 × 10^5 |

has no accuracy loss compared with its ANN counterpart. Up to 75.3× energy improvement is achieved. The reason why the consumed energy is similar for 4-bit to 6-bit activation implementation is because we implement the first layer in DTNN with traditional FP multiplication and addition, which consumes the most energy 0.54 uJ.

#### 4.2. DTNN results on large models, ResNet-18 and VGG-11, with different datasets

Table 4 shows accuracy of DTNN based ResNet-18 with different bit width of activation implemented by lookup operation and its ANN counterpart by conventional FP multiplication and addition. In order to show the scalability of DTNN, we test it with both small dataset including cifar10/SVNH and large datasets, i.e., cifar100/ImageNet. According to the table we can see that large dataset are more prone to accuracy drop due to the decrease of activation bit width, but both of them has negligible loss of accuracy with 4-bit to 5-bit activation and above.

Table 5 shows energy saving on ImageNet with negligible loss of accuracy. For small dataset, DTNN achieves 87.2× energy saving on cifar10.

Table 6 shows results on another standard DNN model, VGG-11, with ImageNet. 16.3× to 64.9× energy saving is
Table 7. Accuracy of DTNN based MobileNet with different bit width of activation implemented by lookup operation and its ANN counterpart by conventional FP multiplication and addition.

| Dataset   | 4-bit   | 5-bit   | 6-bit   | 32FP    |
|-----------|---------|---------|---------|---------|
| Cifar10   | 89.0%   | 90.4%   | 90.3%   | 90.9%   |
| Cifar100  | 61.4%   | 64.3%   | 64.7%   | 65.0%   |
| SVHN      | 94.0%   | 95.6%   | 96.1%   | 96.0%   |
| ImageNet  | 53.3%   | 64.15%  | 67.43%  | 68.9%   |

Table 8. Energy (uJ) of DTNN based MobileNet implemented by lookup operation and ANN based MobileNet by multiplication and addition in inference for one image.

| Dataset       | 4-bit  | 5-bit  | 6-bit  | 32FP   |
|---------------|--------|--------|--------|--------|
| Cifar10/SVHN  | 5.79   | 12.8   | 46.3   | 2.27 x 10^3 |
| Cifar100      | 5.80   | 12.9   | 46.4   | 2.33 x 10^3 |
| ImageNet      | 71.1   | 157    | 568    | 5.33 x 10^3 |

achieved by DTNN with similar accuracy compared with its ANN counterpart.

4.3. DTNN results on a compact model, MobileNet, with different datasets

Table 7 shows accuracy of DTNN based MobileNet with different bit width of activation implemented by lookup operation and its ANN counterpart by conventional FP multiplication and addition. According to the table, compared with standard DNN models, MobileNet, as a compact model for mobile application is more prone to accuracy drop due to the decrease of activation bit width.

Table 8 shows the energy of DTNN based MobileNet implemented by lookup operation and ANN based MobileNet by multiplication and addition in inference for one image. We can see that with negligible loss of accuracy, DTNN could achieve 9.4× and up to 181× energy saving on MobileNet with large dataset, i.e., ImageNet dataset and small dataset, respectively. This result is inline with our expectation because MobileNet is a compact model, which is not as capable as other standard models such as ResNet and VGG. Therefore, it is prone to accuracy drop in model quantization for the large dataset, which limits the power saving with DTNN.

4.4. Comparison with the state-of-the-art

Fig. 4 shows the energy improvement achieved by DTNN with LeNet-5 on MNIST compared with the state-of-the-art model compression methods [15, 13, 42, 25]. From the figure, we can see that DTNN achieves 75.3× energy improvement, which is much larger than that of other SOTA results.

Table 9 shows the comparison of accuracy and energy improvement between DTNN based MobileNet and SOTA model compression method on ImageNet.

| Metrics      | 5-bit DTNN | 6-bit DTNN | [41]CVPR'19 |
|--------------|------------|------------|-------------|
| Acc.         | 64.15%     | 67.43%     | 64.8%       |
| Energy Improv. | 40×        | 9.4×       | 11.2×       |

In order to further validate the effectiveness of DTNN, in this section, we design and implement DTNN based image classifiers using off-the-shelf FPGAs and compare it with state-of-the-art low energy ASIC implementation for edge vision. Please note that the work with SOTA energy results usually focus on the energy efficiency and don’t have SOTA accuracy. In order to conduct fair comparison, we design MLP classifiers, which as similar accuracy range as the SOTA energy-efficient work and compare with them on the energy efficiency. In this experiment we use Type-II Dtree neuron and input pre-processing Method 2 described in Section 3.3 to binarize the input image for higher energy performance.

Classifier architectures We adopt MLP in this experiment, because MNIST is a small dataset, which is easy to reach above 99% accuracy with small CNNs as shown in Section 4.1. Using CNN cannot get similar accuracy with SOTA energy efficient SNN works with ASIC chips. We built two classifiers based on structures of MLP (DTNN MLP-1/2) for MNIST, which are 28x28x1-10 and 28x28x1-216-10, respectively. We use Method 2 in Section 3.3 to generate the binary input from the dataset. As Method 2 directly binarizes pixels in input images with a single threshold, which would invariably lead to information loss, we build the classifier by utilizing an ensemble of 5 MLPs, where each individual
MLP receives as input the 784 pixels of an MNIST digit which has been binarized by a separate threshold value that is unique to that MLP. This allows the digit to be fed in at several different threshold values which mitigates the information loss that occurs due to binarization (which is analogous to HDR algorithms that capture more information about a scene by snapping multiple shots at different exposure levels). Although these threshold values could in principle be learnt, for simplicity we used five evenly spaced threshold values. For pixel range from 0 to 1, we set five thresholds as 0.2, 0.4, 0.5, 0.6, 0.8, respectively. An ensemble of 5 MLPs yields 5 output values per digit class, so in both our classifiers we apply a binarized linear function to each of the 5 values to reduce the output to a single binary value per digit class. The weights of the binarized linear function are learnt when training the ensemble of MLPs, and it, too, is constructed from Dtree neurons consisting of fixed 6-input inner neurons.

Training of DTNN based MLP-1/2 DTNN MLP-1/2 were trained using the Adam optimizer, minimizing the cross-entropy loss. The parameters of the Adam optimizer are shown as follows (learning rate = 0.001, beta = 0.9, beta2 = 0.999, epsilon = 10^-8). DTNN MLP-1 was trained with a batch size of 256 for up to 20,000 iterations. DTNN MLP-2 was trained with a batch size of 1024 for up to 500,000 iterations.

Results comparisons We implemented the DTNN MLP-1 design on AVNET Zedboard with Xilinx Zynq 7020 (XC7Z020-CLG484-1) FPGA, and the DTNN MLP-2 design on Alpha Data ADM-PCIE-7V3 with Xilinx Virtex-7 (XC7VX690T-2) FPGA. In general, our DTNN architecture is not limited to implementation on commercial FPGAs only. It can also be implemented on ASICs. However, even with generalized commercial FPGAs, we obtained much better results than other low power approaches on dedicated ASIC chips. Table 10 shows different metrics including the accuracy, energy consumption per image, and images processed per second.

DTNN MLP-1, with no hidden neurons, achieves 92.8% accuracy with 1.13 nJ consumption per image, which is 0.42% of the 268 nJ per image for the TrueNorth 92.7% accuracy NN. The second DTNN MLP-2, which has a hidden layer containing 216 neurons, achieved a higher accuracy of 96.55%, and an energy consumption of 21.97 nJ at a rate of 125M images per second. In comparison, a higher accuracy version on TrueNorth consumes 4000 nJ and runs at 1K images per second with a slightly lower accuracy.

5. Conclusion

Drawing inspiration from dendrites in neural cells, we proposed a novel Dtree neuron, and show how it can be used in deep neural networks with no loss of accuracy as compared to the traditional neuron. We then introduced a activation quantized version, and showed how a complete neural networks we called DTNN can be constructed and trained. By implementing the nodes in the DTNN model with lookup operations, both costly weight accesses and computationally expensive arithmetic computations are eliminated. To validate its effectiveness, we conducted experiment on DTNN with various kinds of DNN models such as LeNet-5, MobileNet, VGG, and ResNet with different datasets, including MNIST, Cifar10, SVHN, and ImageNet. DTNN achieved significant energy saving, specifically, 19.4× and 64.9× improvement on ResNet-18 and VGG-11 with ImageNet, respectively. To further validate the effectiveness of DTNN and compare with state-of-the-art low energy SNN implementation for edge vision, we design and implement DTNN based MLP image classifiers using off-the-shelf FPGAs, and demonstrated several orders of magnitude improvement in energy consumption and speed.
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