Research on MPDPC with FADRC control strategy for three-phase rectifying converter

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Abstract
Due to unpredictable factors, the model predictive direct power control (MPDPC) exists weak robustness when the parameters change of three-phase rectifying converter. Therefore, this paper introduced Fractional Active Disturbance Rejection Control (FADRC) into the MPDPC system to improve the robustness of rectifying converter, that is, the power loop of PID controller in conventional model predictive control is replaced by FADRC. In order to verify the effectiveness of the proposed control strategy in this paper, a model of three-phase rectifying converter is established in MATLAB, and the simulation is conducted. Compared with the control effects of the MPDPC with PID (MPDPC-PID) control strategy and MPDPC with Linear Active Disturbance Rejection Control (MPDPC-LADRC) under different operational scenarios, the simulation results demonstrate that the MPDPC with FADRC (MPDPC-FADRC) strategy has best disturbance rejection capability, robustness and rapidity, and it can significantly reduce the voltage fluctuation of DC bus. This study can provide a valuable guidance and reference for the design of the efficient and stable three-phase rectifying converter.

Keywords
Rectifying converter, MPDPC, LADRC, FADRC, robustness

Introduction
Three phase rectifier is widely used in Industrial production and manufacturing. The performance of rectifier is closely related to its control. The control strategy of rectifying converter mainly includes current closed-loop control strategy based on PI adjustment,¹,² Proportional-Resonant (PR) control strategy,³ deadbeat control strategy,⁴ hysteresis control strategy,⁵ etc. Each control method can achieve the effective control of the rectifying converter, but they all exist respectively deficiency. The mentioned control strategy mainly depends on the parameters of PI adjustment, and design of the PI parameters generally is quite complicated.⁶ The parameters of PR control strategy are difficult to adjust.⁷ The deadbeat control strategy is highly depending on the system parameters, and the selection of parameters largely determines the accuracy of the deadbeat control strategy. Hysteresis control strategy need high sampling frequency and high-order harmonics.⁸ In recent years, various high quality control strategies have been proposed by experts and scholars, among which the model predictive direct power control strategy is simple and easy to be implemented. Main Abbreviations in this paper is summarized in Table 1.

However, MPDPC strategy also has disadvantages such as large switching frequency and large current distortion.⁹ In order to solve the problems of MPDPC strategy, scholars have put forward a large number of corresponding algorithms to improve MPDPC strategy. In Literature,¹⁰,¹¹ the model predictive power is built by using the grid current and grid voltage together.
with its signal of delay, and the difference in capacitor voltage. Afterward, the optimal switching state under MPDPC is selected to effectively eliminate the double-frequency pulsation in the active power output from the rectifier as well as current harmonics, which can realize the accurate tracking of the given active power and reactive power. Literature,\textsuperscript{12,13} presented a predictive power control based on virtual flux for three-phase rectifier. The mathematical model of predictive power control for rectifying converter is established in coordinate frame. In each sampling cycle, the appropriate voltage vector and the conduction time are selected to control IGBT. In Literature\textsuperscript{14} presents an improved MPDPC strategy for three-phase rectifying converter. This strategy applies voltage vector pairs during the control period, then uses the Lyapunov function to select voltage vector pairs which satisfy the closed-loop stability criterion, and applies the voltage vector pairs the next control period. Compared with the conventional MPDPC method, this strategy can reduce the average of switching frequency and losses while reducing the amount of calculation.

However, the effects of external environment changes, uncertainty of system model and internal parameter disturbances on the voltage of DC and its stability have been ignored. The three-phase rectifying converter based on model predictive power control strategy is a typical, strong coupling system,\textsuperscript{15} which is very sensitive to disturbance and system parameter changes. Therefore, conventional linear control strategies are difficult to achieve ideal control effect. The LADRC strategy is a simple and robust algorithm, which does not rely on the accurate model of the controlled system.\textsuperscript{16} In order to increase the controllability of LADRC and improve the control precision, the literature\textsuperscript{17} proposed a FADRC strategy which is combined of ADRC technology with a fractional calculus theory. FADRC strategy not only has the advantages of LADRC strategy,\textsuperscript{18} but also increases the degree of freedom of controller parameters, thus the overall performance of the controlled object were improved.\textsuperscript{19}

Therefore, in this paper, the FADRC is applied to the three-phase rectifying converter control system to further improve the anti-disturbance ability of the DC bus voltage. This paper not just builds the power prediction model of the rectifying converter based on the FADRC but also designs a closed-loop power controller of the rectifying converter based on the FADRC. Finally, the rectifying converter model based on MPDPC is established in MATLAB. The effectiveness and superiority of the control strategy proposed in this paper are verified by the comparison of MPDPC-PID, MPDPC-LADRC, and MPDPC-FADRC.

**Voltage vector model of three-phase rectifying converter**

The topology structure of the three-phase rectifying converter is depicted in Figure 1. $L_d = L_b = L_c = L$ are the filter inductances at the AC side. $R_a = R_b = R_c = R$ are the line resistances. $C$ is the filter capacitor of DC. $VT_1 \sim VT_6$ are six switching transistors using IGBT.

According to Figure 1, the mathematical model of the three-phase rectifying converter in the three-phase static coordinate system is established by Kirchhoff’s Law,\textsuperscript{20} it can be written as

$$\begin{align*}
U_{aN} &= R_i a + L \frac{di_a}{dt} + e_a \\
U_{bN} &= R_i b + L \frac{di_b}{dt} + e_b \\
U_{cN} &= R_i c + L \frac{di_c}{dt} + e_c \\
C \frac{di_{dc}}{dt} &= i_{dc} - S_a i_a - S_b i_b - S_c i_c
\end{align*}$$

Equation (2) is the switching control state of the rectifying converter, $S_k (k = a, b, c)$ are the switching states of k-phase arms.

![Figure 1. Diagram of three-phase rectifying converter topology structure.](Image)

**Table 1. Abbreviations of main technical terms.**

| Technical term                        | Abbreviations |
|---------------------------------------|---------------|
| Model Predictive Direct Power Control | MPDPC         |
| Fractional Active Disturbance Rejection Control | FADRC         |
| Linear Active Disturbance Rejection | LADRC         |
| Fractional Tracking Differentiator   | FTD           |
| Fractional Extended State Observer   | FESO          |
| Linear State Error Feedback          | LSEF          |

$U_{aN}(k = a, b, c)$ are line voltage of the AC side, are three-phase current of AC, $i_{dc}$ represents the current of DC bus, $e_k (k = a, b, c)$ are three-phase AC voltage.

Equation (2) is the switching control state of the rectifying converter, $S_k (k = a, b, c)$ are the switching states of k-phase arms

$$S_k (a, b, c) = \begin{cases} 
1 & \text{The upper arm is on and the lower arm is off} \\
0 & \text{The upper arm is off and the lower arm is on} 
\end{cases}$$

The switching signal represented by space vector is written as

$$S = \frac{2}{3} \left(S_a + a S_b + a^2 S_c\right)$$
Table 2. Vector voltages in different switching states.

| $S_a$ | $S_b$ | $S_c$ | Vector voltages ($u$) |
|-------|-------|-------|-----------------------|
| 0     | 0     | 0     | $u_0 = 0$             |
| 1     | 0     | 0     | $u_1 = 2U_{dc}/3$     |
| 1     | 1     | 0     | $u_2 = U_{dc}/3 + j\sqrt{3}U_{dc}/3$ |
| 0     | 1     | 0     | $u_3 = -U_{dc}/3 + j\sqrt{3}U_{dc}/3$ |
| 0     | 0     | 1     | $u_4 = -2U_{dc}/3$    |
| 0     | 0     | 1     | $u_5 = -U_{dc}/3 - j\sqrt{3}U_{dc}/3$ |
| 1     | 0     | 1     | $u_6 = U_{dc}/3 - j\sqrt{3}U_{dc}/3$ |
| 1     | 1     | 1     | $u_7 = 0$             |

Figure 2. Diagram of converter voltage space vectors.

Thereinto, $a = e^{2\pi i/3}$

Output voltage vector can be written as

$$S = \frac{2}{3}(U_{aN} + aU_{bN} + a^2U_{cN})$$  \hspace{1cm} (4)

Form equations (3) and (4), the relationship between the output voltage vector $U$ and the switch states $S$ is obtained as

$$U = SU_{dc}$$  \hspace{1cm} (5)

The three-phase rectifying converter topology consists of six switches, so there are eight switching states, namely: 000 100 110 010 011 001 101 111, and the corresponding number of voltage vector is also eight. The vector voltages in different switching states are summarized in Table 2.

There are seven different states because of $U_0 = U_7$. Figure 2 is diagram of rectifier voltage space vectors. $U_a$, $U_b$ are the component of rectifier output voltage in the static coordinate system. $U_{out}$ is the output voltage of rectifier.

**Principle of the FADRC**

The fractional active disturbance rejection controller is composed of Fractional Tracking Differentiator (FTD), Fractional Extended State Observer (FESO), and Linear State Error Feedback (LSEF).\(^{22}\) Thereinto, FTD can smooth the start process and quickly track the input signal of the system without overshoot, and it can produce an excellent differential signal. FESO is the core of the active disturbance rejection controller, which can mainly estimate the error between the actual control object and the internal nominal control object. LSEF determines the quantity of the error feedback according to the system state error.

$v(t)$ represents the input signal, $r_1(t)$ and $r_2(t)$ are two output signals through FTD. $r_1(t)$ is the trace signal of the $v(t)$, $r_2(t)$ is the differential signal of the $v(t)$.

Thus, a FTD can be constructed as

$$\begin{cases}
  r_1^{(a)} = r_2(t) \\
  r_2^{(a)} = -r^2(r_1(t) - v_0) - 2rr_2(t)
\end{cases} \hspace{1cm} (6)$$

$r$ represents speed factor for adjusting system response speed.

Supposing a fractional system as

$$y^{(2a)} + a_2y^{(a)} + a_1y = w + bu$$  \hspace{1cm} (7)

$u$ and $y$ respectively represent the input and output signals of the fractional system; $w$ is external disturbance; $a_1, a_2, w,$ and $b$ are unknown. The estimate value for the gain is set to $b_0$. By linear transformation and substituting $b_0$ into equation (7), and then equation (8) can be obtained as

$$y^{(2a)} = -a_2y^{(a)} - a_1y + w + (b - b_0) \cdot u + b_0u$$  \hspace{1cm} (8)

where $f = -a_2y^{(a)} - a_1y + w + (b - b_0) \cdot u$; $f$ is the total disturbance. Think of all the fractional parts as disturbance of the system.

If the intermediate variables are set to $\dot{x}_1$, $\dot{x}_2$, and $\dot{x}_3$, the state equation of fractional system can be written as

$$\begin{cases}
  \dot{x}_1 = x_2 \\
  \dot{x}_2 = x_3 + bu \\
  \dot{x}_3 = h \\
  y = x_1
\end{cases} \hspace{1cm} (9)$$

Where $h = f^{(a)}$; $x_1$, $x_2$, and $x_3$ are the state variables. Equation (9) can be transformed into a continuous state space as

$$\begin{cases}
  X^{(a)} = AX + Bu + Eh \\
  y = CX
\end{cases} \hspace{1cm} (10)$$

Where equation (10), $A$, $B$, $E$, and $C$ respectively can be written as...
The corresponding FESO can be expressed as

\[
\begin{align*}
Z^{(a)} &= AZ + Bu + L(\hat{y} - y) \\
\hat{y} &= Cz
\end{align*}
\] (12)

Where \( L \) is the gain matrix of the FESO; \( Z = [z_1 \ z_2 \ z_3]^{T} \) is the state variable; \( \hat{y} \) is the estimate value of output \( y \).

Therefore, FESO of the fractional active disturbance rejection controller can be written as

\[
\begin{align*}
e &= z_1 - y \\
\dot{z}_1 &= z_2 - \beta_1 e \\
\dot{z}_2 &= z_3 - \beta_2 e + b_0 u \\
\dot{z}_3 &= -\beta_3 e
\end{align*}
\] (13)

Where \( z_1 \) represents the estimate value of \( x_1 \); \( z_2 \) represents the estimate value of \( x_2 \); \( z_3 \) represents the estimate value of \( x_3 \); \( \beta_1, \beta_2, \) and \( \beta_3 \) are the observer gains; \( e \) represents the tracking error.

Assuming the control quantity \( u \) of the system as

\[
u = (-z_3 + u_0)/b_0
\] (14)

The fractional order system expressed by equation (8) is transformed into a series of fractional integrators

\[
y^{(2a)} = f - z_3 + u_0 = u_0
\] (15)

Fractional active disturbance rejection controller can be designed as

\[
\begin{align*}
u_0(t) &= k_p(r_1 - z_1) - k_d(r_2 - z_2) \\
u &= (-z_3 + u_0)/b_0
\end{align*}
\] (16)

Where \( k_p \) and \( k_d \) respectively are the proportional and differential gains of the controller, and correspondingly \( k_p = \omega_c^{2a}, k_d = 2\omega_c; \omega_c \) is the controller bandwidth.

For varying disturbances of the system, the response speed of FESO is determined by its bandwidth, so the higher value of \( \omega_c \), the faster speed tracking of FESO, in addition the stronger anti-interference ability of LADRC. While the larger \( \omega_c \), the larger noise amplification effect of FESO, and the higher noise pollution of the system. Furthermore, the bandwidth parameter of FESO must make a compromise between the noise suppression performance and anti-interference ability of the system. Based on the above considerations, \( \omega_c = 55 rad/s \) is selected in this paper.

By substituting the observer bandwidth \( \omega_0 \), the gain of FESO respectively represent as \( \beta_1 = 3\omega_0, \beta_2 = 3\omega_0^2 \), and \( \beta_3 = \omega_0^3 \).

In order to ensure the observation accuracy of the observer for the total disturbance and realize the real-time compensation for the total disturbance, the bandwidth of the observer \( \omega_0 \) should be greater than \( \omega_c \) of the FADRC, which is generally chosen as \( (3-5)\omega_c \).

FADRC schematic diagram is depicted in Figure 3.

The transfer function of FADRC is written as

\[
G(s) = K_p + K_d \frac{1}{s^\lambda}
\] (17)

Where \( \lambda \) is the fractional integral order. Generally, the range of the of the \( \lambda \) value is between 0 and 1. In order to meet the requirements of controller performance in this paper, \( \lambda \) normally is set as 0.8.

Therefore, the closed-loop transfer function of the controlled object can be expressed as

\[
\frac{Y(s)}{V(s)} = \frac{k_p s^{\alpha} + k_p}{s^{\lambda} + k_p s^{\alpha} + k_p}
\] (18)

\( Y(s) \) represents the output; \( V(s) \) represents the input.

Since the fractional derivative of the step signal setting value is not a pulse signal, the control rate \( u_0 \) of \( r_2 \) cannot be omitted.

**FADRC predictive power control**

**Principle of model predictive control**

The basic principle of the model predictive direct power control strategy is illustrated in Figure 4.\(^{23}\) At time \( t_k \), all prediction results of the system \( x_{n(k+1)} \) can be obtained by the discrete-time model of the system which possess \( N(N = 1, \ldots, n) \) control behaviors. At time \( t_{k+1} \), the system behavior is obtained by the measured value \( x(k) \) and \( n \) switch control signals \( S_k \), and then \( n \) possible values \( x_0, x_1, \ldots, x_n \) are generated. \( x_{n(k+1)} \) is closest to the reference value \( x^* \), thus at time \( t_k \), \( S_2 \) is the optimal switching state at this time, and it selected to predict the next sampling period. At time \( t_{k+1} \),
Derivation of equation (19) leads to equation (20).

Component of function in two-phase static coordinate system, side voltage on \( S_k \) is expressed as

\[
\begin{align*}
U_a &= e_a i_a + e_b i_b \\
n &= e_b i_a - e_a i_b
\end{align*}
\]

Where \( e_a \) and \( e_b \) respectively are the components of AC side voltage on \( \alpha \) axis and \( \beta \) axis, \( i_a \) and \( i_b \) respectively are the components of line current on \( \alpha \) axis and \( \beta \) axis. Derivation of equation (19) leads to equation (20).

\[
\begin{align*}
\frac{d e_a}{dt} &= e_a \frac{du_a}{dt} + e_b \frac{du_b}{dt} + i_a \frac{di_a}{dt} + i_b \frac{di_b}{dt} \\
\frac{d e_b}{dt} &= -e_a \frac{du_a}{dt} + e_b \frac{du_b}{dt} + i_a \frac{di_a}{dt} - i_b \frac{di_b}{dt}
\end{align*}
\]

Calculation of equation (20) need to find the expression of voltage and current in the static coordinate system. Therefore, the AC side voltage in the static coordinate system can be expressed as

\[
\begin{bmatrix}
ed_a \\
ed_b
\end{bmatrix} = \frac{2}{3} \begin{bmatrix}
1 & \frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}}
0 & -\frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2}
\end{bmatrix} \begin{bmatrix}
ed_a \\
ed_b \\
ed_c
\end{bmatrix} = \begin{bmatrix}
U \sin(\omega t) \\
U \cos(\omega t)
\end{bmatrix}
\]

Where \( U \) is the peak value of the AC side voltage, and \( \omega \) is the angular frequency of the AC side voltage.

Derivation of equation (21) leads to

\[
\begin{align*}
\frac{de_a}{dt} &= \omega U_a \cos(\omega t) = -\omega e_b \\
\frac{de_b}{dt} &= \omega U_b \sin(\omega t) = \omega e_a
\end{align*}
\]

In the static coordinate system, line current can be expressed as

\[
\frac{di_a}{dt} = \frac{1}{I_a} (u_a - e_a - i_a R) \\
\frac{di_b}{dt} = \frac{1}{I_b} (u_b - e_b - i_b R) \\
\frac{dU_a}{dt} = \frac{1}{I_k} (i_k - \sum_{k = \alpha, \beta} S_k i_k)
\]

Where \( S_k \) is the component of \( \alpha \) and \( \beta \) axis of switch function in two-phase static coordinate system, \( i_k \) is the component of \( \alpha \) and \( \beta \) axis of grid-side current in two-phase static coordinate system.

\textbf{MPDPC of three-phase rectifying converter}

Principle of instantaneous active power and reactive power in the static coordinate system can be expressed as

\[
\begin{align*}
p &= e_a i_a + e_b i_b \\
q &= e_b i_a - e_a i_b
\end{align*}
\]

When the sampling frequency is high, equation (24) can be discretized by forward difference method, therefore equation (25) is obtained as

\[
\begin{align*}
(p(k + 1) - p(k)) &= \frac{1}{L} [e_a u_a(k) + e_b u_b(k) - U^2 - Rp(k)] \\
q(k + 1) &= \frac{1}{L} [e_b u_a(k) + e_a u_b(k) - Rp(k)] + \omega p(k)
\end{align*}
\]

Where \( p(k + 1) \) and \( q(k + 1) \) respectively are the value of active power and reactive power at time of \( k + 1 \); \( p(k) \) and \( q(k) \) respectively are the values of active power and reactive power at time of \( k \); \( u_a(k) \), \( u_b(k) \) are the value of output voltage of rectifying converter at time of \( k \); \( e_a(k) \), \( e_b(k) \) are grid voltage at time of \( k \).

At the time of \( t_k \), the system collects voltage and current, and predicts the power value of all switching states at time \( t_k + 1 \). In order to get the optimal switching state at the time of \( t_k + 1 \), a cost function \( g \) need to be established to continuously reduce the error, and then the minimum of the cost function can be obtained by selecting the optimal switching state. In this paper, the cost function is written as

\[
g = |P_{\text{ref}} - P(k + 1)| + |Q_{\text{ref}} - Q(k + 1)|
\]

\textbf{Design of MPDPC controller based on FADRC}

After the derivative of the third equation in equation (23) is simplified as
\[
\frac{d^2 U_{dc}}{dt^2} = \frac{1}{LC} \sum_{k=1}^{\alpha, \beta} (S_k i_k R - S_k v_k) + \frac{\omega}{C} (S_k i_\alpha - S_k i_\beta) \\
+ \frac{1}{LC} \sum_{k=1}^{\alpha, \beta} S_k U_k
\]

The differential equation of equation (27) is transformed into a state space expression, which can be written as

\[
\begin{pmatrix}
\dot{x}_1 \\
\dot{x}_2 \\
\dot{x}_3 \\
y
\end{pmatrix} =
\begin{pmatrix}
0 & 1 & 0 \\
0 & 0 & 1 \\
0 & 0 & 0 \\
x_1 & x_2 & x_3
\end{pmatrix}
+ \begin{pmatrix}
0 \\
b_0 \\
0 \\
h
\end{pmatrix}
\begin{pmatrix}
u
\end{pmatrix}
\]

Where \( f = \frac{1}{LC} \sum_{k=1}^{\alpha, \beta} (S_k i_k R - S_k v_k) + \frac{\omega}{C} (S_k i_\alpha - S_k i_\beta), \)
\( x_3 = f, b_0 = \frac{1}{LC}, x_1, x_2 \) are the state variables, \( x_1 \) is the real-time output, \( x_2 \) is the differential of \( x_1 \), \( x_3 \) is the total disturbance of the system, \( h \) is the differential of \( f \).

According to equation (13), the third order FESO of the power loop can be written as

\[
\begin{cases}
\dot{z}_1 = z_2 - 3\omega_0 (z_1 - y) \\
\dot{z}_2 = z_3 - 3\omega_0^2 (z_1 - y) + b_0 u \\
\dot{z}_3 = -\omega_0^3 (z_1 - y)
\end{cases}
\]

When the parameter \( \omega_0 \) is set accurately, \( z_1, z_2, \) and \( z_3 \) of the state observer respectively converge to the differential signals of DC bus voltage \( U_{dc} \), \( U_{dc} \) and the total disturbance \( f \).

The linear control law can be designed as

\[
\begin{pmatrix}
u_0 \\
u_0
\end{pmatrix} = \frac{\omega_0^2 (\omega_0^2 e^{-\omega_0 t} U_{dc} - z_1)}{2\omega_0^2 (e^{-\omega_0 t} - \omega_0^3 e^{-\omega_0 t}) - z_2} \]

Where \( U_{dc} \) is the given voltage of the DC bus, and \( i_\alpha \) is the given current.

The control structure of the three-phase rectifying converter is based on MPDPC-FADRC, MPDPC-LADRC and MPDPC-PID, respectively, which is illustrated in Figure 5. The voltage and output current of the converter are collected at time \( t_k \), which is transformed into two-phase static coordinate system by Clark transformation. Then, combined with the voltage vectors \( u_a \) and \( u_b \) in the switching state, the predicted power value at time \( t_k + 1 \) is obtained through the pre-

**Figure 5.** The three-phase rectifying converter based on MPDPC-FADRC, MPDPC-LADRC, and MPDPC-PID.

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The given value $i_a$ of the active current is generated by the FADRC controller, by which the active power expected value $P_{\text{ref}}$ of the FADRC controller can be calculated, moreover, the reactive power expected value $Q_{\text{ref}}$ is set according to the demand. Finally, the optimal switching state is selected to control “on” and “off” of transistors after the cost function calculation.

### Analysis of simulation results

In order to verify the effectiveness of the control strategy proposed in this paper, the system model of three-phase rectifying converter is established in the MATLAB. The main simulation parameters of the system are summarized in Table 3, and the main parameters of the controller are summarized in Table 4.

In order to verify that the MPDPC-FADRC strategy has good rapidity and disturbance performance, this paper compares MPDPC-FADRC, MPDPC-PID control, and MPDPC-LADRC. The control effect of MPDPC strategy combined with three control strategies are explored. Then, under the three control strategies, dynamic response speed and steady-state performance of the rectifying converter DC bus voltage are compared and analyzed, for verifying the superior robustness of the MPDPC-FADRC strategy which proposed in this paper. In addition, this paper was also analyzed system characteristic of two conditions, which are voltage drop on the AC side and DC load reducing.

### Analysis of simulation in normal operation

In the case of normal operation, other simulation conditions are kept identical, only the control strategy is different. Figures 6 and 7 respectively show the three-phase current and voltage waveform under the MPDPC-FADRC strategy. Figure 8 show the THD index of AC side current under MPDPC-FADRC, respectively. The MPDPC-FADRC strategy which is proposed in this paper can better suppress the current harmonic at the AC side. And the THD index is 4.34% which meets the requirements of power grid.

As exhibited in the Figure 9, the comparison of DC bus voltages under three control strategies of MPDPC-FADRC, MPDPC-PID control and MPDPC-LADRC is obtained. It can be observed that the DC bus voltages under three control strategies can achieve basically the same control effect as the given reference value of 400 V. However, the time of reaching stability is

### Table 3. Simulation parameters of system.

| Parameters       | Value     |
|------------------|-----------|
| Line resistance $R$ | 0.1 Ω     |
| Line inductance $L$ | 0.005 H   |
| Filter capacitor $C$ | 1500 μF   |
| Load resistance $R_{\text{Load}}$ | 40 Ω     |
| Three-phase voltage $e$ | 110 V    |
| Frequency of AC bus $f$ | 50 Hz    |
| Voltage of DC bus $U_{\text{dc}}$ | 400 V    |

### Table 4. Simulation parameters of controller.

| Parameters       | Value     |
|------------------|-----------|
| Bandwidth of controller $\omega_c$ | 55 rad/s |
| Bandwidth of observer $\omega_0$ | 235 rad/s |
| Fractional integral order $\lambda$ | 0.8      |
| Control gain $b_0$ | 7600 dB   |

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different for the DC bus voltage. Under the MPDPC-PID and MPDPC-LADRC control strategies, the time of reaching stability is respectively 1.87 and 0.76 s for the DC bus voltage. Compared with MPDPC-PID and MPDPC-LADRC, the DC bus voltage based on MPDPC-FADRC can stabilize within 0.48 s, and the ripple coefficient can be maintained around 0.02 V.

Figure 10 illustrate the measurement values of active and reactive power based on MPDPC-FADRC strategy. The given active power $P_{\text{ref}} = 4000 W$ and the given reactive power $Q_{\text{ref}} = 0 \text{ var}$ are transmitted from DC side to the AC side. It can be seen from the Figure 10 that the actual output active power $P$ is stable at around 4000 W, the error of which is not more than 10 W.

**Simulation experiment analysis under distribution**

The symmetrical voltage drops of 25% on the AC. The voltage symmetry drop amount caused by the fault was set as 25%. The fault starts at time of 3.3 s and ends at time of 4 s, therefore, the fault remained time was 0.7 s. When other simulation conditions were identical, the voltage waveforms of the DC bus were compared under the three control strategies. Figure 11 shows the comparison of DC bus voltage waveforms of three control strategies under fault of voltage symmetry drops 25% on AC side.

When the voltage of AC side suddenly decreases to 75%, the DC bus voltage decreases by 0.58 V under the MPDPC-PID control strategy, and the DC bus voltage can hardly reach stability within the experimental time. When decreases to 75%, the DC bus voltage decreases by 0.58 V under the MPDPC-PID control strategy, and the DC bus voltage can hardly reach stability within the experimental time. Under MPDPC-LADRC control strategy, the DC bus voltage decreases by 0.47 V and the voltage returns to steady state in 0.44 s when the fault occurred. Under MPDPC-FADRC strategy, the bus voltage is only reduced by 0.07 V, which can not only restore the voltage to a stable state in 0.33 s, but also have higher steady-state precision after voltage recovery. Compared with MPDPC-PID control and MPDPC-LADRC, the DC bus voltage of FADRC only increases by 0.08 V When the AC side voltage begins to recover. And the DC bus voltage wave of MPDPC-PID control and MPDPC-LADRC are 0.39 and 0.31, respectively. Therefore, it can be concluded that the MPDPC-FADRC control on three-phase rectifying converter is not easily affected by the voltage fluctuation of the AC side, consequently, the voltage fluctuation is less obvious when the fault occurs.

The load of DC side increased or decreased by 50%. The load of DC side increased or decreased caused by the fault was set as 50%. The fault starts at time of 3.3 s and end at time of 4 s, therefore, the fault remained time was 0.7 s. When other simulation conditions were identical, the voltage waveforms of the DC bus were compared under the three control strategies. Figure 12 shows the comparison of bus voltage waveforms of three control strategies under the fault of increasing or decreasing load of 50%. When the load at the DC side suddenly decreases by 50%, the voltage of AC bus will decrease due to the sudden reduction of the power at the load side. Under the MPDPC-PID control, the voltage of the DC bus drops to 386 V at most, and the bus voltage cannot return to steady state after 0.7 s; under MPDPC-LADRC control strategy, the voltage of the DC bus drops to 396 V, and the voltage returns to
steady state at 3.88 s. However, under MPDPC-FADRC strategy, the voltage of the DC bus only drops to 398 V, which can not only restore the voltage to a stable state in 3.64 s, but also have higher steady-state precision after voltage recovery. When the DC side of the load starts to recover, the voltage of the DC bus drops to the DC bus voltage increases only by 2 V under the MPDPC-FADRC, however, the MPDPC-PID and MPDPC-LADRC are 12 and 4.5 V, respectively.

Therefore, under the same operating conditions, the MPDPC-FADRC can significantly reduce the voltage fluctuation of the DC side, shorten the transition time of the system, and improve the tracking performance and disturbance attenuation ability of the system. The MPDPC-FADRC strategy can make the rectifying converter respond to the external disturbance quickly and stabilize the DC bus voltage accurately to the reference value.

Conclusions

In order to further remedy the deficiency of weaker robustness, weaker ADRC and lower response speed of the MPDPC-PID strategy of three-phase rectifying converter, this paper respectively proposed MPDPC-LADRC strategy and MPDPC-FADRC strategy. Simulations results verify that under operational scenarios of the symmetrical voltage drops on the AC and the load change of DC side, compared with MPDPC-PID control and MPDPC-LADRC, MPDPC-FADRC can more quickly track the load change and deal with the disturbance of unbalanced voltage on AC side in time. Therefore, the MPDPC-FADRC strategy has best disturbance rejection capability, robustness and rapidity, and it can significantly improve steady state accuracy of the voltage of DC bus. And this study can provide a significance reference for practical application when designing control strategies of the three-phase rectifying converter.

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