Development of the read-out ASIC for muon chambers

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Abstract. A front-end prototype ASIC for muon chambers is presented. ASIC was designed and prototyped in the CMOS UMC MMRF 180 nm process via Europractice. The chip includes 8 analog processing channels, each consisting of a preamplifier, two shapers (fast and slow), differential comparator and an area efficient 6 bit SAR ADC with 1.2 mW power consumption at 50 Msps. The chip also includes the threshold DAC and digital serializer. The design has the following features: dynamic range of 100 fC, channel hit rate of 2 MHz, ENC of 1000 e- at 50 pF, power consumption of 10 mW per channel, 6 bit SAR ADC.

1. Introduction

The Compressed Baryonic Matter (CBM) experiment will be one of the major scientific pillars of the future Facility for Antiproton and Ion Research (FAIR) in Darmstadt [1,2]. The muon chamber (MUCH) is part of the equipment. MUCH is based on the gas electron multiplier (GEM) detectors [3]. GEM detectors will be operating at a high gas gain in the range of 1000 to 8000. The MUCH set up has 25000 64-channel chips to handle totally 1.5 x 10\(^6\) channels. Also, GEM muon chambers will have projective segmentation with the smallest pad size being as small as 4.1 x 4.1 mm\(^2\) in the inner region and as large as 2.1 x 2.1 cm\(^2\) in the outer region of the chamber.

This sets up the following ASIC features:

- dynamic range of 1–100 fC;
- wide \(C_{\text{DET}}\) range of 1–50 pF;
- S/N maximization at the periphery pads;
- hit rate up to 2 MHz at the central pads;
- low (less than 10 mW/ch.) power consumption.

In accordance to the specifications two prototype ASICs were designed.

2. Preamplifier prototype

The preamplifier prototype for CBM MUCH (MUCH ASIC v.1) was designed, fabricated and tested [4]. The prototype includes 10 preamplifier channels. Figures 1 and 2 show the measurement results for the CSA transfer function. MUCH ASIC v.1 has generally met the MUCH front-end requirements and therefore it was taken as a basis for the new prototype chip design described in section 3.
3. 8-channels ASIC prototype

The 8-channel ASIC prototype for muon chambers of the CBM experiment (MUCH ASIC v.2) was designed and fabricated in the 0.18 μm CMOS process of UMC (Taiwan).

The chip structure includes 8 analog processing channels, 2 threshold DACs, 8 SAR ADCs and a digital part. Each analog channel contains the preamplifier, followed by two shapers (fast and slow) and differential comparator (see figure 3).

The preamplifier is based on the folded cascode CSA architecture with additional gain boosting. The gain is set to 4 mV/fC and its noise level is estimated by ENC = 1500 el. at 50 pF.

Output CSA response on the test input pulse via the 1.2 pF capacitor has the following parameters: rise time – 30 ns, fall time – 500 ns, signal duration – 600 ns (see figure 4).

The slow channel is optimized for S/N ratio in order to use it in the periphery, and the fast channel is adapted to the hit rate of the inner detector part, where the occupancy is the highest. Both channels are realized with CR-RC shapers.
Slow and fast shaper output signals were obtained. Shaping times of the slow and fast shapers are equal to 250 ns and 50 ns correspondingly. Due to the double differentiation of the fast channel, the fast shaper output response has a bipolar form. Such a form allows to recognize 2 neighbour hits when the discriminator threshold is low (see figure 5). Channels linearity was studied in the signal dynamic range of 1 – 100 fC. Transfer functions of the CSA, fast and slow channels are shown in figure 6. The ENC of the fast and slow shaper outputs are 2000 el and 1500 el correspondently at 50 pF of the equivalent detector capacitance (see figure 7).

![Figure 4. CSA output response.](image)

![Figure 5. Shapers output response.](image)

![Figure 6. Dynamic range of preamplifier and shapers. Errors lie inside data points. Solid line – linear fit.](image)

![Figure 7. ENC vs Cdet. Errors lie inside data points.](image)

The schematic of the MUCH ASIC v.2 ADC [5] is shown in figure 8. The single-ended architecture was chosen to save design area. The schematic and layout of comparator were optimized to eliminate errors, arising from the kick-back effect in single-ended architecture. The comparator with the preamplifier stage before latch was used to isolate the capacitor matrix from output signal swing.

![Figure 8. ADC structure.](image)
Prototypes of the gas-filled detectors based on the GEM and TGEM technologies have been studied with the prototype front-end ASIC. A prototype read-out system is being developed jointly by PNPI and MEPhI. $^{55}\text{Fe}$ (5.9 keV) spectrum was obtained (see figure 9). The measured noise of 1000 electrons at a 20pF input capacitance increases up to 2500 electrons at the input capacitance of 80 pF. Figure 10 shows the MUCH ASIC v.2 die photo.

![Figure 9. $^{55}\text{Fe}$ spectrum (5.9 keV).](image_url)

![Figure 10. 8-channel prototype chip photo.](image_url)

Comparison of the simulated and measured parameters is shown in table 1.

| Parameter                               | Simulation | Measurements |
|-----------------------------------------|------------|--------------|
| Dynamic range (fC)                      | 1 – 100    | 1 – 100      |
| CSA rise time (ns)                      | 20         | 30           |
| Shaping time (fast) (ns)                | 60         | 50           |
| Shaping time (slow) (ns)                | 260        | 250          |
| Slow channel gain (mV/fC)              | 5          | 4.4          |
| Fast channel gain (mV/fC)              | 5.5        | 5            |
| Slow channel ENC @ 50 pf C$_{det}$ (el)| 800        | 1500         |
| Fast channel ENC @ 50 pf C$_{det}$ (el)| 1200       | 2000         |
| Power consumption (mW/channel)          | 10         | 13           |

4. Conclusion

The development of the mixed-signal front-end ASIC for muon chambers has been presented. The ASIC was made as a mixed-signal 8 channel chip for reading out the signals of GEM detectors. The next steps towards the 64-channel ASIC version are the development of time stamp with 10 ns resolution, built-in spark protection, digital peak detector, serial interface and slow control.

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