Evaluation of Low-Cost Thermal Laser Stimulation for Data Extraction and Key Readout

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Abstract—Recent attacks using thermal laser stimulation (TLS) have shown that it is possible to extract cryptographic keys from the battery-backed memory on state-of-the-art field-programmable gate arrays (FPGAs). However, the professional failure analysis microscopes usually employed for these attacks cost in the order of 500k to 1M dollars. In this work, we evaluate the use of a cheaper commercial laser fault injection station retrofitted with a suitable amplifier and light source to enable TLS. We demonstrate that TLS attacks are possible at a hardware cost of around 100k dollars. This constitutes a reduction of the resources required by the attacker by a factor of at least five. We showcase two actual attacks: data extraction from the SRAM memory of a low-power microcontroller and decryption key extraction from a 20 nm technology FPGA device. The strengths and weaknesses of our low-cost approach are then discussed in comparison to the conventional failure analysis equipment approach. In general, this work demonstrates that TLS backside attacks are available at a much lower cost than previously expected.

Index Terms—IC Security, Optical Attacks, Thermal Laser Stimulation, FPGA Security

I. INTRODUCTION

Data extraction from integrated circuits (ICs) can pose a serious threat to the secrets stored within. Extraction of cryptographic keys, sensitive data stored in memory, or device fingerprint information, as used in physically unclonable functions (PUFs), allows attackers to break security features. Physical attacks, such as side-channel attacks, are one of the main approaches to extract data contained in embedded devices.

Thermal laser stimulation (TLS) is one such technique, which analyzes changes in the current consumption of the device in response to applied laser radiation. In the past, it has been used to read out the content of static random-access memory (SRAM) and thus allows the characterization of SRAM PUFs [1]. It was also applied to extract the key from the battery-backed random-access memory (BBRAM) contained within the encryption unit of a 20 nm technology field-programmable gate array (FPGA) [2]. Furthermore, TLS can be considered as a suitable technique for the readout of microcontroller SRAM working memory [3]. Therefore, it is a powerful data extraction tool for an attacker on hardware level.

However, all previously mentioned experiments have been conducted using professional failure analysis (FA) equipment, more specifically a Hamamatsu Phemos-1000 laser scanning microscope (LSM). Such a system typically costs around 500k to 1M dollars, and even when renting, costs for the development of a TLS attack are still in the range of thousands of dollars [4]. As a consequence, even though TLS is a powerful attack technique, the connected costs might discourage attackers from applying it.

Yet, it needs to be kept in mind that FA equipment usually offers a lot more features than an attacker might actually need, for instance, support for wafer handling and automated testing equipment, very fast acquisition times, and integration of other measurement techniques, such as photon emission. In principle, however, all that is needed for a TLS attack is a way to move a laser spot over the device and simultaneously measure a current. This raises the question, if attackers might be able to use simpler, more low-cost setups. If so, the threat posed by TLS techniques would be larger than expected so far. The main aim of this work is to determine if this is the case.

To evaluate this question, suitable alternatives to the usually employed FA systems need to be considered. One such candidate are commercially available setups used for evaluation of laser fault injection (LFI) which are by a factor of around five to ten cheaper than FA LSMs. Such systems usually feature a laser with focusing optics and some mechanical means to move the laser spot on the device under test (DUT), e.g., via motorized stages. The only thing required to perform TLS with such a system would thus be a current preamplifier and a laser of suitable wavelength. Hence, it seems plausible that such a setup could be modified to perform TLS attacks at a low cost. However, it is unclear if the expected slower scanning speeds of motorized stages, as opposed to galvanometric mirrors usually used in FA solutions, might make attacks infeasible.
II. BACKGROUND

A. Thermal Laser Stimulation (TLS)

Techniques from failure analysis (FA) that use laser radiation to impact the device under test (DUT) are referred to as laser stimulation techniques. Usually, the laser is scanned over the DUT while device parameters like the current consumption are monitored, grayscale-encoded and plotted over the scanning position, see Fig. 1. The resulting response map shows areas where laser radiation causes changes in the current consumption of the DUT. For thermal laser stimulation (TLS), the laser wavelength is chosen to have a photon energy smaller than the silicon bandgap, which consequently only causes local heating and no photocarrier generation.

When drain or source of a single metal-oxide semiconductor field-effect transistor (MOSFET) are thermally stimulated, effectively a voltage source between the corresponding metal contact and the channel is generated [1, 5]. This voltage source is also referred to as Seebeck generator, since it is caused by the Seebeck effect [9]. When the channel of the transistor is low-ohmic, this generator is connected between drain and source. In contrast, when the channel is high-ohmic, one connection of the generator is floating and the generated voltage is ineffective. The sign of the generated voltage depends on whether drain or source are stimulated and on the type of the MOSFET (n- or p-type) [6].

A memory cell, as implemented in complementary metal-oxide semiconductor (CMOS) technology, basically consists of two cross-coupled inverters, see Fig. 2. As can be seen, the circuit stays in one of two states because of the cross-coupling. While being in a stable state, for ideal transistors there is no current flow between VCC and GND, since one of the transistors in each connection from VCC to GND is high-ohmic. However, under stimulation, the Seebeck generator causes the creation of a voltage \( U_{\text{Seebeck}} \), which is added to the existing voltage levels. When assuming 0 V as GND level and, for instance, the drain of transistor P1 is stimulated, effectively \( U_{\text{Seebeck}} \) is applied to the gate of N2. Consequently, the resistance of N2 decreases via exponential sub-threshold operation, which in turn results in an increased current flow between VCC and GND. The same applies for transistor P1 when the drain of P2 is stimulated. The change in current consumption can be expected to be in the nanoampere range [1].

If a laser with a beam diameter approximately equal to the transistor size is scanned over the cell, a TLS response map as shown in Fig. 2 can be expected. Due to the increased current consumption, the sensitive transistors will be shown as brighter pixels. If the memory cell is in the inverted state, the other two transistors are sensitive. The cell’s state can thus be deduced from the TLS response map.

Note that due to the chosen laser wavelength only thermal stimulation occurs, which can increase the leakage current of the memory cell but cannot change its state.

B. TLS for PUF Characterization and Data Extraction

The extraction of data stored in SRAM on microcontrollers can pose a threat to secrets stored within. For instance, the authors of [1] show that the extraction of data from SRAM memory on microcontrollers down to the 180 nm technology..
node is possible. More specifically, they demonstrate the characterization of a proof-of-concept SRAM-based PUF implementation on a microcontroller using TLS on professional FA equipment. Similarly, the authors of [3] show the potential to read out the whole working memory on a 180 nm technology microcontroller using TLS. It should be noted that for both attacks it was necessary to put the DUTs into a low-power mode, to reduce the noise of the system.

Such attacks on SRAM memory of microcontrollers are hereafter referred to as SRAM data extraction attacks.

C. TLS for Decryption Key Extraction

The authors of [2] demonstrate that the battery-backed random access memory (BBRAM) on a 20 nm technology field-programmable gate array (FPGA) can be read out with TLS using professional FA equipment. The BBRAM stores a 256-bit key used for bitstream decryption. To retain the key while the FPGA is powered off, the BBRAM is powered by a coin-cell battery. During the attack, the TLS signal is acquired by measuring the current consumption on this battery line. Since the BBRAM is the only circuit powered by the battery, the noise on this battery line is very low. It should be noted that the attack was successful because the memory cell size is approximately 2.8 × 3.1 μm, which is about 10 times larger than expected minimum size on a 20 nm technology device [2]. This can be explained by reliability, leakage, and low current consumption considerations.

For their attack approach, the authors assume that the BBRAM is located close to the configuration logic. They consult the documentation to get an estimate of its location on the chip. By conducting a TLS scan over the candidate area, they can find the BBRAM. Afterward, they prove a data dependency in the measurements and create a mapping from memory cell locations to logical bits. Finally, they show that a key stored in the BBRAM can be extracted using TLS in a manual or automated fashion within minutes.

Although the BBRAM is typically only battery-backed SRAM, this attack type is hereafter referred to as BBRAM key readout attack.

III. SETUP

A. Laser Stimulation Setup

As core of our setup we use an ALPhANO Single Laser Microscope Station (S-LMS), which was designed for laser fault injection purposes [7]. It is a microscope-based setup that allows the injection of different laser sources. In our case we use a 1424 nm laser diode capable of delivering more than 300 mW in continuous waveform (CW) mode. The laser power can be controlled via PC software. The laser is focused through objectives, which are mounted on a manual turret, into the IC backside. For thermal stimulation we use a 50x/0.65NA objective with silicon thickness correction, for optical images we additionally use 20x/0.5NA and 2.5x/0.1NA objectives. The whole microscope is mounted on XYZ motorized stages, which allow movements with a resolution of 50 nm. The stages are controlled via PC software or a joystick. The S-LMS is also equipped with infrared (IR) lighting and a short-wave infrared (SWIR) camera. This allows the user to monitor the laser spot position and perform optical navigation.

For measuring the current consumption during stimulation, we use a Stanford Research Systems SR570 current preamplifier, which has a bias voltage feature. The preamplifier outputs a voltage proportional to the current which is digitized using a National Instruments "PCI-6259" card.

To realize the scanning functionality and TLS response map creation, we developed a scanning software in the “LabView” programming environment from National Instruments. In this software, the scanning parameters, such as step size, step resolution, scanning speed and number of samples per pixel can be entered. The stage, and thus also the laser spot, is then moved continuously over the DUT while the preamplifier output is sampled. From this data, a TLS response map is created, in which higher current consumption of the DUT corresponds to brighter pixels. The whole setup is visualized in Fig. 3. Note that all results shown in this work have been achieved with this setup.

B. Devices Under Test (DUTs)

1) DUT for SRAM Data Extraction: As mentioned in Sect. [1-B] reading out SRAM via TLS has been demonstrated down to the 180 nm technology node. Thus, a 180 nm Texas Instruments MSP430F5131 microcontroller is used in our experiments. It is equipped with 1 KB of SRAM with a cell size of approximately 2.5 × 1.9 μm [3]. For access to the silicon, the backside packaging material and the metal chip carrier were removed.

During the experiments, VCC of the DUT is supplied with 2.6 V via an auxiliary power supply. The core, which contains the SRAM, is supplied via the internally generated VCORE voltage, which is also available externally at a pin. To this pin we connect the SR570 current preamplifier and set the bias voltage to 2.1 V, which is slightly above the VCORE voltage of 1.9 V. In this way, a significant amount of the core voltage is supplied by the SR570.

A JTAG debugging interface is connected to the device. This allows to directly write arbitrary data into the SRAM.
For noise reduction on the VCORE net, the DUT is send to low-power mode 4 (LPM4) during the TLS scan.

For all experiments on the MSP430, the current amplification of the SR570 was set to 1 nA V$^{-1}$ and the input offset to 500 nA. The laser current was set to 600 mA, which corresponds to a total power of about 43 mW for the 50x lens. The silicon thickness correction of the objective was set to 350 µm.

2) DUT for BBRAM Key Readout: The target platform for bitstream key extraction is a Xilinx Ultrascale FPGA development board from AVNET (model AES-KU040-DBG). It contains a Xilinx Ultrascale XC7U040-1FBVA676 FPGA manufactured with 20 nm technology in a flip-chip ball grid array (BGA) package. Due to the flip-chip package, direct access to the silicon is available and no preparation is necessary. The thickness of the substrate is about 750 µm [2].

The 256-bit key used for bitstream decryption can be stored in a battery-backed RAM (BBRAM) which is programmed via a JTAG interface [8]. While the device is powered off, the BBRAM is supplied by a battery via the $V_{BATT}$ line. To measure the current consumption of the BBRAM during TLS, we soldered cables to the battery connector and connected them to the input of the SR570 current amplifier. During key programming, the board is powered via its external supply. During TLS experiments, however, the board is powered off and the $V_{BATT}$ voltage is supplied via the bias voltage feature of the SR570.

For all experiments on the Ultrascale FPGA, the current amplification of the SR570 was set to 2 nA V$^{-1}$ with no input offset. The laser current was set to 500 mA, which corresponds for the 50x lens to a total power of about 26 mW. The silicon thickness correction of the objective was set to 750 µm.

IV. MEASUREMENT RESULTS

A. SRAM Data Extraction

1) SRAM Overview: To localize the SRAM optically, the camera of the setup was used, see Fig. [4]. After zeroizing the whole SRAM via JTAG, the device is sent to low-power mode by code run from flash. A TLS scan with 0.5 µm scan step size was then acquired, see Fig. [5]. It can be seen that most of the memory shows a regular structure, except for some irregular vertical strips, mainly in the bottom left quadrant. Closer investigation revealed that this is data placed in SRAM by the code which enters the low-power mode. This already demonstrates that data dependencies can be observed. The SRAM seems to be sub-divided into four blocks with a small offset of about one cell width in between, as already discovered in [3]. In addition, some cells seem to be more sensitive to TLS, as can be seen by some irregular bright spots. This can be explained by manufacturing variability. The TLS response becomes increasingly blurry in the right half of the scan, which can be explained by thermal and mechanical drift of the DUT due to the long scan duration of 43 min. This could be avoided by scanning smaller areas and refocusing for each measurement.

2) Extraction of Single Bits: To demonstrate the extraction of single bits, we compare measurements of a small area of the SRAM, see Fig. [6]. For the first measurement, the centered bit (framed in red) is set to 1, while all other bits are 0. For the second measurement, all bits, including the highlighted one in the center, are 0. A pattern similar to the response map in Fig. [2] can be observed. For bit value 1, bottom left and top right of the cell are the most sensitive spots. In contrast, for bit value 0, the sensitive spots are in the other corners of the cell. The subtraction of both response maps reveals the change more clearly.

These results show that the resolution of our setup is sufficient for extracting data from arbitrary SRAM cells on the MSP430 device. Consequently, an SRAM PUF implemented with a similar feature size could be characterized with this setup. If the memory layout would be reverse-engineered using TLS, the full working memory of the MSP430 could be read out as well.

B. BBRAM Key Readout

1) Localization and Optical Overview: In the attack scenario of [2], the BBRAM has first to be localized inside the configuration area. For this, we performed a scan of that area with a pixel size of 5 µm and a stage speed of 2 mm s$^{-1}$ in about 5 min. The response map, see Fig. [7a], reveals two sensitive areas when the BBRAM is activated. If the BBRAM is deactivated, only one sensitive area remains, see Fig. [7b]. Fig. [8] shows an optical image of the area where TLS
sensitivity occurred. The two highlighted block-like structures on the left correspond to the area where the TLS signal was dependent on BBRAM activation. These are the BBRAM block candidates, which are already known from [2]. The structure on the right-hand side was always sensitive and thus can be disregarded. The results show that the BBRAM can be localized using our setup. In the next step, the detailed TLS response map has to be analyzed.

2) TLS Overview Scan: To observe data dependencies in the TLS response of the BBRAM, we first programmed a random key and an all-zeros key and acquired TLS response maps, see Fig. 9a and 9b. It can be seen that different keys lead to different patterns in the response map.

To further investigate the key dependency of the TLS response, a single memory cell can be examined.

3) Extraction of a Single Bit: To identify a single bit in the TLS response map, we scanned a small area of the BBRAM with high resolution (pixel size 50 mm, stage speed 50 µm s⁻¹) with different bit values for one memory cell, see Fig. 10. While the sensitive spots for bit value 1 are on the top left and bottom right, the spots for value 0 are on the top right and bottom left of the cell, cf. Fig. 2. The subtraction of the two response maps clearly shows that the state and thus the bit value of the centered BBRAM cell differs in the two measurements. Hence, this experiment proves that the optical resolution of our setup is sufficient for extracting the bit value stored in one BBRAM cell. The observed cell size is about $3.2 \times 2.8$ µm.

4) Key Extraction: Since we have already shown that data extraction of single bits from the BBRAM is possible with our setup and the mapping from physical to logical bit positions is known from [2], now a complete key can be extracted. For this, we subtract the response map of the all-zeros key (Fig. 9b) from the response map of the random key (Fig. 9a). On the difference image, see Fig. 11, areas with large black and white spots correspond to bit value 1, the others to value 0. By adding a grid to optically show the SRAM cell size and position, the key bits can be easily extracted manually. Note that the top row is used to store security-relevant information, such as a configuration counter and error-detection bits [2].

The scan of the whole BBRAM for a pixel size of 250 nm and a stage speed of 50 µm s⁻¹ takes about 7 min.

Given the above, the bitstream decryption key can be extracted from the BBRAM using our setup within minutes. This proves that the complete attack on the FPGA bitstream decryption key can be conducted with a much cheaper setup than previously expected.

V. DISCUSSION

A. Low-Cost vs. FA Setup

1) Acquisition Time: The experiments have shown that the time needed for acquisition is substantially longer when using the low-cost setup. This is due to the fact that for an FA laser scanning microscope (LSM) only small and light galvanometric mirrors are moved to scan the beam. In our case, though, the optical setup is moved on mechanical stages and the connected inertia poses a limit on the maximum scan speed. To give some exemplary numbers, for an FA LSM an acquisition time of 1.2 minutes can be expected for BBRAM key extraction [2]. With our setup, 7 minutes were needed.
This is an increase by a factor of 5.8, but makes measurements due to the generally short duration still unproblematic. For TLS SRAM data extraction, experiments performed by the authors have resulted in 4.8 minutes of acquisition time on an FA LSM. Using the low-cost setup, a complete SRAM scan on the MSP430 takes 43 minutes. This is an increase by a factor of 9. For such a long acquisition time, negative effects such as sample drift will lead to complications. This could already be observed in Fig. 5 (Sect. IV-A). It can thus be seen that with the approach demonstrated in this paper, attackers will have to trade cost for time. Additionally, procedures such as refocusing might be needed to prevent negative side effects, although these are relatively easy to implement.

For a low-cost approach, mechanical stages seem to be the obvious choice, since they are available in virtually any laboratory and microscope setup, as also in the used fault injection stages. Yet, the optical setup is more demanding, especially the requirements on the objective rise, since the field of view has to be sufficiently large.

2) Resolution: In terms of optical resolution, FA LSMs and the low-cost approach are virtually identical. This is due to the fact that the optical resolution is mainly determined by the wavelength and the numerical aperture of the objective lens. Using the same lens and wavelength should thus yield the same resolution in both setups. For the 50x lens and laser used in our setup, an optical resolution of about 1 μm can be expected.

For scan step resolution, the situation is different. The angular stepping resolution of an LSM’s scanning mirror is translated by the objective lens into a spatial scanning resolution. This means that the scanning resolution can be increased by using larger magnification lenses. In contrast, the scan step resolution for the low-cost setup is simply the resolution of the stage, 50 nm in our case. Both the LSM’s and the low-cost setup’s scan resolution are significantly lower than the optical resolution and can be expected to not be a limiting factor.

In general it can be said that our setup is not better or worse compared to an LSM in terms of resolution. However, it should be noted that FA LSMs can be equipped with a solid immersion lens (SIL), which can increase the resolution by a factor of around 4.3 in case of the Hamamatsu Phemos system [9].

3) Cost: Our setup only consists of commercially available components. The core of the setup is a “S-LMS” station by ALPhANOV. In a configuration suitable for retrofitting TLS, the system costs about 102k USD, including a 1.4 μm laser. Additionally, the SR570 current preamplifier for 2,595 USD [10] and the NI-6259 digitizer card for 1,940 USD [11] have to be acquired. Including the control PC and a LabView license, the price of the complete setup is expected to be below 110k USD.

Compared to a Phemos-1000 Failure analysis setup with a price between 500k and 1M USD, our setup is five to ten times cheaper. Furthermore, the setup can in principle be set up on a single desk and purchasing of the equipment is expected to require less effort.

B. Attack Feasibility and Limitations

The feasibility of TLS attacks on SRAM in general depends on the spatial distance between the sensitive transistors. Consequently, the limiting factor is the laser spot size. The minimum possible spot diameter is about 1 μm without SIL and 235 nm with a recent SIL, which corresponds to cell dimensions of 2 μm and 470 nm, respectively. Thus, the attack is expected to work at least down to these cell sizes. Furthermore, it can be expected that with post processing of the TLS signal, for instance, by deconvolution, an additional resolution enhancement by a factor of two is possible. However, to the best of our knowledge, the actual SRAM cell size limit for TLS attacks is unknown and should be subject of future research. It should also be noted that with the switch to new technologies, like FinFET, changes in the behavior of the stimulated cells might occur.

Next to the cell size, the attack is also limited by the amount of noise present in the TLS signal. Specifically, the leakage current of the transistor affected from stimulation should be higher than the fluctuations in the overall current consumption. In our experiments, this was fulfilled by the low noise on the battery line of the FPGA, and by sending the microcontroller to low-power mode.

Readers interested in more details regarding the attack feasibility are directed to [2].

C. Countermeasures

The possible countermeasures against TLS attacks from the chip backside can be divided into two categories. On the one hand, techniques could be applied to obstruct the access to the chip or the measurement signal, and on the other hand, active attack detection mechanisms could be employed.

An approach for the former class could be to reduce the resolution of the laser beam by scrambling the incoming light from the chip backside, and thus increasing the beam diameter within the silicon. In [12] this approach is applied against optical contactless probing. The authors introduce the usage
of nanopyramid structures, which scramble the reflected light. However, adding the nanopyramids between chip backside and the transistors is only possible for bonding-based SOI devices. Furthermore, the countermeasure was not tested with respect to thermal stimulation. Yet, it might be an interesting approach for further research.

Another approach for the first category of countermeasures could address the destruction of the data dependency in the TLS signal. Since the attack relies on low noise in the current consumption of the target device, noise injection can be used for this purpose. In [13] a noise source has been successfully designed and integrated to protect an encryption core from power analysis attacks. This shows that on-chip noise-based mitigation techniques can work. Against TLS attacks on SRAM, a proof of concept countermeasure was presented in [2]. By injecting noise on the battery line of a BBRAM key storage, TLS data extraction can be made much harder or possibly even unfeasible. The authors show that this can be an effective mitigation technique, even with negligibly lower battery life time.

A more thorough approach is the protection of the chip backside by employing an opaque coating layer to obstruct optical access completely. However, a solely passive layer could be easily removed by polishing. As evaluated in [14], the integrity of the coating layer can be assured by in-silicon light emitters and sensors. This combines an obstruction approach (first category) with an active detection countermeasure (second category). Yet, due to the high power consumption of the photo sensors, this protection scheme can not protect devices with a very restricted power profile, such as the BBRAM key storage.

To actively detect the temperature changes induced by the laser radiation, temperature sensors could be useful [2]. However, it is questionable whether the very small temperature changes with a power of less than 50 mW can be detected with a small amount of false positives. Furthermore, the current consumption of temperature sensitive circuits, such as ring oscillators, is typically high [15]. Hence, for power constrained devices like the BBRAM, this does not seem to be a feasible solution.

VI. CONCLUSION

In this work, we have shown that constructing a low-cost setup for TLS is indeed feasible. By retrofitting an LFI setup with the necessary equipment, we have demonstrated a solution for TLS five to ten times cheaper than traditional FA equipment. Although with slower signal acquisition, we were still able to show that two state-of-the-art attacks, specifically against SRAM on a microcontroller and BBRAM on an FPGA, are possible in reasonable time. Consequently, the attacker model must be rethought and adapted to better reflect the lower-than-expected hurdle for an attacker to apply TLS. Therefore, better protection mechanisms against attacks from the chip backside will have to be deployed.

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