A 5.8 GHz RF Receiver Front-End With 77.6 dB Dynamic Range AGC for a DSRC Transceiver

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ABSTRACT This paper presents a 5.8 GHz highly sensitive, high-dynamic-range RF receiver front-end with Automatic-Gain Control (AGC) and a high image-rejection for a Dedicated Short-Range Communication (DSRC) application. It is formed by a transceiver common matching, a single to differential Low-Noise Amplifier (LNA), an active mixer with an Image Rejection Filter, and an AGC unit. The proposed AGC unit is composed of a power-detector over the intermediate-frequency signals of the downconverter mixer. The power detector produces a wide dynamic range response signal, which eases the controllability of the AGC unit. In addition, external components are minimized, and area occupation is optimized. The proposed RF-FE is fabricated and measured in a 130-nm RF CMOS process. Experimental results show an overall dynamic range of 77.6 dB while a high sensitivity performance to an input power level of $-85$ dBm is measured. An overall gain of 26.4 dB for the RF-FE is obtained. The input referred P1dB is measured to be around $-28.3$ dBm. The 2-stage RC poly-phase filter that is applied to reject the image signal results in a maximum image rejection ratio of 39 dB.

INDEX TERMS Automatic gain control, high dynamic range, dedicated short-range communication, image rejection, power detector, 5.8 GHz receiver.

I. INTRODUCTION Recently, Intelligent Transportation Systems (ITS) have been recognized as an essential research trend in Information and Communication Technology (ICT). Interesting applications such as vehicular safety, Electronic Toll Collections (ETC), and traffic control applications are the examples that motivate researchers to enhance new research and design across a wide range of new advances. Among these applications, traffic wireless communication is the target of recent research [1]. To obtain a high-speed secured direct communication between the vehicles and the surrounding infrastructure while any kind of wireless connectivity like cellular infrastructure is not involved, Dedicated Short Range Communication (DSRC) is proposed.

The DSRC is a wireless communication based on IEEE 802.11p [1], which is an amendment to the IEEE
FIGURE 2. The proposed architecture for the RF-FE with AGC.

802.11 standard. DSRC communication is shown in Fig. 1. It defines enhancements to support ITS applications [2]. The operating frequency of the DSRC is around 5.8 GHz. It must meet an implementation with direct, low latency in terms of information exchange between vehicles and the infrastructure. The DSRC operational band is 5.855–5.925 GHz, which is divided into seven channels, with 10 MHz channel spacing. The frequency band is characterized by a high anti-interference design. Recently, the new Electronic Toll Collection (ETC) system has also been switched to the 5.8 GHz band [3]–[8]. Using DSRC is a principal for an ETC system when it comes to two-way wireless communication between the Onboard Units (OBUs) and the Roadside Units (RSUs).

Nowadays, the mainstream of a DSRC band is 5.8 GHz band for ITS applications, which results in a challenging design with outstanding performance, inexpensive cost, and an optimized architecture requirement for the Receiver (RX) of the transceiver. The common issue with the DSRC transceivers is the momentary high power RF signal from the antenna, which occurs due to the close distance between the transmitters and the receivers. The high-power input RF signal can lead the receiver to saturation.

In [2], a Received Signal Strength Indicator (RSSI) block is placed after the downconverter mixer, which demands its own Analog to Digital Converter (ADC). The provided bits will be used in the digital of the baseband to have a control over the gain. The drawback of using the RSSI is the large area of occupation while its output detected levels are linear rather than the logarithmic output of the Power Detectors (PDs). In [3], an automatic gain control is performed over the Transimpedance Amplifiers (TIAs) which are located after the mixer.

The block-diagram of the proposed receiver is shown in Fig. 2. The PD is located after the mixer over the Intermediate Frequency (IF) signals. The benefit of this implementation is to avoid an additional matching network for the power detector. The cost of this implementation is that the PD is not located in the earlier stages after LNA which could provide a faster reaction to the input power. On the other hand, the proposed implementation does not need any matching network for the PD which results in a smaller area occupation. Also, it is satisfying the requirements for the reaction response which are required for the gain reconfiguration of the LNA. In compare with the RSSI, it is more area efficient.

II. PROPOSED RF FRONT END DESIGN ARCHITECTURE

The top block diagram of the proposed RF-FE for a DSRC transceiver is shown in Fig. 2. The architecture is a low-IF architecture rather than a zero-IF one due to its better noise performance and better DC offset performance [11], [12]. The architecture is formed by the sub-blocks such as a Single-Pole Double-Throw (SPDT), Low-Noise Amplifier (LNA), an active four-phase down-conversion mixer, and the Automatic Gain Control (AGC) unit.

The low-IF receiver provided a simpler implementation with a lower complexity in term of the hardware which results in a lower power consumption. In spite with the benefits, the image rejection is necessary to overcome the image problem in the low-IF receiver.

The image rejection and the complexity of the IF circuits in the Band-Pass Filter (BPF) are occurring because when IF is going to lower frequencies, the ripples of the PD’s output and its settling time will be too long. Also, image rejection becomes more challenging. Inversely, by increasing the IF, the Gain-Bandwidth (GBW) product of the BPF must be larger.

III. THE DESIGN OF THE COMPONENTS

A. LNA WITH TUNABLE LC LOAD STRUCTURE

To avoid an external passive balun, an active balun must be considered as the solution to provide a differential output for
the LNA. The LNA of the receiver is based on a buffered feedback topology [13], which is shown in Fig. 3. The topology, which is resistive shunt feedback, provides a wideband input impedance matching by negative feedback [14], [15]. The LNA implementation of the proposed receiver is shown in Fig. 4. In combination with the feedback loop, the AC-coupling through C3 to the gate of cascode M4 results in a smaller channel noise and non-linearity contribution than M3 [16]. The input transistors provide large transconductance to achieve a high gain with a low Noise Figure (NF). The L-C tank load provides adjustable band-pass characteristics in the desired frequency range using the tunable capacitance banks. The gain mode of the LNA is switched between the high and low gain modes through the M7 switch. Due to the high-quality factor of the LC-tank load, the open-loop gain of the LNA follows as below [13]:

\[ A_v = g_{m1} R_L, f_r = g_{m1} 2\pi f_r L_1 (Q_1 + \frac{1}{Q_1}) \]  

where \( L_1 \) and \( Q_1 \) are the load inductor value and quality factor at the frequency of \( f_r \) which is proportional to the \( C_{load} \)

\[ f_r = \frac{1}{2\pi \sqrt{L_1 C_{load}}} \]  

where the \( C_{load} \) is the total LNA load capacitance considering the parasitic capacitors. The tunability of the gain of the LNA is proportional to \( C_{load} \) which is tunable by the cap-banks at the load. The total noise factor at the input (\( F_{input} \)) follows (3):

\[ F_{input} \approx 1 + \gamma \left( \frac{1}{g_{m1} R_S} \right) \left( 1 + \frac{R_S}{R_F} \right)^2 + \frac{R_S}{R_F} \]  

For higher \( g_{m1} \) and higher closed-loop voltage gains, the NF of the LNA will be smaller. Equations (2) and (3) are related to the resonance frequency and noise figure of the proposed LNA with the high gain mode of operation while M7 switch is turned off. The proposed LNA can be switched to low gain mode when M7 switch is turned on.

B. QUADRATURE I/Q MIXER

A quadrature down-conversion core stage and a Poly-Phase Filter (PPF) in a two-stage configuration form the image rejection mixer to generate a quadrature signal. The core of the mixer is an active architecture. The passive PPF provides the phase shift to perform the IF image rejection.

Due to the low IF implementation of the receiver, an active 4-phases down-converter mixer is used, which is shown in Fig. 5 and is formed by the Gilbert unit. The input RF transconductance stage is shared among the I and Q paths. Also, the input transistors have an important advantage from the noise influence. In the I/Q paths, the generated noise at the image frequency is correlated in the I/Q paths. Therefore, the noise of these two paths can be offset and the noise figure be lowered by 3 dB.

The PPF operates as a phase shifter to cancel the image signal tone, and the image signal is rejected by the gain and phase imbalance where there is a 90-degree phase difference in the I/Q paths. The two-stage image-rejection network is shown in Fig. 6. Since the frequency range is not wide, a two stage PPF can be utilized to attenuate the image signal sufficiently over the frequency range of 5.855 GHz to 5.925 GHz. The filter can discriminate between positive and negative image-tones, and the RC filter can distinguish between the relative phase sequences of I/Q signals. Therefore, the proposed mixer has the down conversion operation over the RF signal while rejecting the image components.

C. AUTOMATIC GAIN CONTROL (AGC)

AGC manages the gain-mode of the LNA when the power of the RF signal through the antenna is too large. The proposed AGC is formed by a PD, two comparators, and the control logic, which is shown in Fig. 7. The output of the AGC unit is connected to the LNA gain control. When the input power is larger than the input referred 1 dB compression point (P1dB) of the high-gain mode (LNA_GCTRL < 1:0 >= 11), the output of the PD, which is a voltage level corresponding to
the received power, will be compared with both lower and high reference voltages.

While the higher reference level is corresponding to the input referred P1dB the gain mode will switch to the low gain mode (LNA_GCTRL < 1:0 == 0). Consequently, this operation avoids the saturation of the LNA and results in a wider input dynamic range and guarantees the linearity of the receiver. Here, the input dynamic range is obtained by the minimum input signal power level, which is proportional to the sensitivity of the receiver, and the maximum input signal power level that maintains the front-end operating in linear region.

Fig. 8 illustrates the operation of the AGC unit. While gain modes are switching, the power of the received signal is varying and its corresponding voltage at the output of the PD is going more than or less than the Vref_High and Vref_Low, respectively. These references define the active operation window of the AGC unit.

**FIGURE 8. AGC operation of the proposed RF-FE.**

**FIGURE 9. The proposed power detector.**

**FIGURE 10. PD’s response to a range of input powers.**

**FIGURE 11. The chip-micrograph of the RF-FE as a part of a DSRC transceiver chip property.**

**FIGURE 12. The chip-micrograph of the RF-FE as a part of a DSRC transceiver chip property.**

D. INTERMEDIATE-FREQUENCY POWER DETECTOR (IF-PD)

To perform the ALC operation, an IF-PD is proposed which measures the power level of the quad-phase IF signals provided by the mixer. The superiority of the IF-PD is a wider output dynamic which eases the controllability of the active window which is set by the low and high voltage references. The other beneficial aspect is due to the lack of a matching network which is required for RF-PD ones [10]. In compare with the RSSI which is used in similar works the PD occupies a much smaller area.

The simulation results show a 3.5 dB NF for the LNA. The results are obtained while PAD and Single Pole Double Throw (SPDT) effects are considered. The mixer has a conversion gain of 5.56 dB and an input referred P1dB of −9.75 dBm. When AGC switches the LNA to low gain mode, it results in a higher dynamic input range and avoids the LNA operating with power over its input referred P1dB to enhance the overall linearity of the RF-FE. Finally, to suppress image signals caused by the low IF implementation, a two-stage poly-phase filter Image Rejection (IR) filter is used, which results in −38 dB Image Rejection Ratio (IRR) in the post-layout simulation.

IV. EXPERIMENTAL MEASUREMENT

The proposed RF-FE is fabricated in a 130-nm RF-CMOS process. The chip-micrograph of the proposed receiver is
shown in Fig. 11. The occupation areas of the LNA, Mixer, and IR Filter are 500 × 550, 300 × 250, 530 × 200, and 400 × 360 µm², respectively. The measurement setup is formed by a signal generator, a network analyzer, a power supply, and the test board, which are shown in Fig. 12.

The measured NF is obtained as 3.7 dB, which shows a 0.2 dB increase in comparison with the post-layout simulation results. The input referred P1dB is measured as −28.3 dBm. The sensitivity and dynamic range are measured. The measurement results show a maximum sensitivity of −85 dBm in the high-gain mode and a dynamic range of 49.5 dB is obtained, while the dynamic range is enhanced to 59.8 dB when the gain-mode of the LNA is switched to the low gain mode. The overall dynamic range of the receiver is 77.6 dB. Therefore, the receiver operates at an input power level of −81 dBm. The image rejection performance measurement result is displayed in Fig. 14. The IRR is obtained at around 39 dB with respect to a −50 dBm input power level, and the output power is −23.6 dBm, so that the gain of the total frontend is 26.4 dB. The maximum and minimum gain of the front-end are measured at 26.4 dB and 13.8 dB, respectively. To examine the AGC unit operation, the input power is gradually increased, and the output power level is recorded. The higher reference voltage is set to the input referred P1dB level. Therefore, the LNA’s gain mode switches to low and high gain modes when the detected power level reaches P1dB as in Fig. 15. Table 1. presents the performance comparison for the proposed RF-FE. The proposed receiver front-end has a higher performance in terms of sensitivity, which is −85 dBm, compared with references. A wider dynamic range is obtained at 77.6 dB. It also represents a better P1dB as −28.3 dBm for high gain mode while this value is enhanced up to −7.4 dBm for the low-gain mode.

| Parameters                  | [1]    | [17]   | [18]   | This Work |
|-----------------------------|--------|--------|--------|-----------|
| Technology                  | 65 nm CMOS | 130 nm CMOS | 130 nm CMOS | 130 nm CMOS |
| Frequency (GHz)             | 2-5.8 | 5.8    | 0.5-2.5 | 5.8       |
| Supply Voltage (V)          | 1.2    | 1.5    | 0.9    | 1.2       |
| Gain (dB)                   | 22-23  | 45     | 29-35  | 26.4      |
| Current Consumption (mA)    | 30-45  | 22     | 24.4-44.4* | 13.8     |
| Noise Figure (dB)           | 2.9    | N/A    | 2.1-2.6 | 3.7       |
| Input Referred P1dB (dBm)   | -18-38 | N/A    | N/A    | -28.3     |
| RX Sensitivity (dBm)        | N/A    | -75    | N/A    | -85       |
| RX Dynamic-Range (dB)       | N/A    | 67     | N/A    | 77.6      |

*The current consumption is obtained from the power consumption (mW) and a 0.9-V supply.
The current consumption also is kept in a lower value in a cost of a lower gain but higher input referred P1dB.

V. CONCLUSION

A 5.8 GHz image-rejection RF receiver front-end with AGC for a DSRC application is fabricated in a 130-nm RF CMOS process. The experimental result shows an overall dynamic range of 77.6 dB while a high sensitivity performance for an input power level of −85 dBm is measured. An overall gain of 26.4 dB for the RF-FE is obtained. The input referred P1dB is measured to be around −28.3 dBm. The 2-stage RC poly-phase filter that is applied to reject the image results in a maximum image rejection ratio of 39 dB.

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