The PLL synthesizer based on 6-12 GHz wideband hybrid VCO

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Abstract. This article describes the design of PLL synthesizer based on developed wideband hybrid VCO. In particular, the structure of such device has been defined, and its components have been chosen. It ensures the frequency range from 6 GHz to 12 GHz. The measured characteristics of PLL synthesizer are in good agreement with the calculation results. That is why developed VCO may be used for the implementation of wideband PLL system.

1. Introduction
Microwave voltage-controlled oscillator (VCO) is a key component of phase-lock-loop (PLL) synthesizers which may be used in different telecommunication, navigation and monitoring radio systems. Also these devices are important part of many RF and microwave test-and-measurement systems [1-5].

The main characteristics of the PLL synthesizers are significantly dependent on the parameters of used VCO. First of all a desired frequency range of PLL synthesizers is determined by the frequency tuning range of VCO. That’s why to design wideband frequency synthesizers, wideband VCOs are necessary [1-6].

A similar situation is observed in the measurement of the noise characteristics of PLL synthesizers. That is, the noise characteristics of VCO significantly affect the noise characteristics of the entire synthesizer. Note that the noise parameters of VCO completely determine the frequency synthesizer noise outside a loop bandwidth [1-7].

Since VCO is an important component of the frequency synthesizers, research of this oscillator as part of the PLL synthesizer is a relevant and significant task.

This article describes the analysis of the wideband VCO [8, 9] work in the PLL synthesizer.

2. PLL synthesizer design

2.1. Selection of PLL synthesizer components
The works [8, 9] consider wideband hybrid VCO which provides the tuning range of 6 to 12 GHz when the control voltage varies from 1 to 13 V. The output power about 1.5 - 2 dBm has been achieved with a phase noise of better than −90 dBc/Hz at 100 kHz offset from the carrier.

Figure 1 shows the board of PLL synthesizer based on developed VCO.
Most of modern reference oscillators generate a signal with a frequency of the order of several hundred MHz [2]. Typical frequencies are 100, 120, and 200 MHz.

In the PLL synthesizer shown in Figure 1, MX037/14P series oscillator was chosen as a reference oscillator 100 MHz. It is an ultralow power high stability miniature OCXO which also provides fast warming up [10].

LTC6947 chip is a high performance, low noise microchip with phase frequency detector (PFD). This microchip also includes a reference divider, ultralow noise charge pump, fractional feedback divider, and VCO output divider. Note that all device settings are controlled through widespread SPI-compatible serial port [11].

HMC451 is the power amplifier required to match the levels of the LTC6947 chip and developed VCO. This 50 Ohm matched amplifier does not require any external components and the RF I/O’s are DC blocked, making it an ideal linear gain block for this application [12].

HMC862 chip was chosen as a frequency divider to match the operation of the LTC6947 chip and VCO. This device provides the low phase noise, wide frequency range and flexible division ratio making it ideal for high performance and wide band communication systems [13].

LP38798 chip is necessary to form the required supply voltage. It is a high-performance, low-noise LDO that can supply up to 800 mA output current. This device provides ultralow output noise and high PSRR at switching power supply frequencies [14].

Since the developed VCO tune voltage range is greater than the LTC6947’s charge pump voltage range, it is necessary to use an active filter based on an op amp. The OPAx211 series amplifier was chosen as this op amp because it provides low current noise, high speed, and wide output swing. This device achieves very low 1.1 nV/√Hz noise density with a supply current of only 3.6 mA [15].

### 2.2. Selection of the loop bandwidth

It is necessary that the loop bandwidth (BW) is near the crossover frequency of the VCO’s phase noise and the phase noise floor of the reference oscillator, referred to the PFD chip output. The phase noise floor of the reference oscillator $L_{\text{ref \ out}}$, referred to the PFD chip output, may be calculated as follows [2]:

$$ L_{\text{ref \ out}} = L_{\text{ref \ in}} - 10 \log(R) + 20 \log(N), \quad (1) $$

where $L_{\text{ref \ in}}$ is the input referred reference phase noise, $R$ is a reference frequency division factor, and $N$ is a VCO’s frequency division factor.

Selection of $R$ and $N$ depends on the required values of the output signal frequency, frequency of the reference oscillator signal, and the acceptable level of phase noise. It should be noted that increase of $R$ value leads to a deterioration of the PLL synthesizer noise characteristics. That’s why to design
this synthesizer based on the developed oscillator $R$ was chosen equal to 1 and 2 ($N = 60 \div 120$ for $R = 1$ and $N = 120 \div 240$ for $R = 2$). A further increase of $R$ value leads to large phase noise level.

For selected values of $R = 1$ and $N = 60 \div 120$: \[L_{\text{ref out}} = -165 - 10\log(1) + 20\log(60 \div 120) = -129 \ldots -123 \text{ dBc/Hz}.\] (2)

For selected values of $R = 2$ and $N = 120 \div 240$: \[L_{\text{ref out}} = -165 - 10\log(2) + 20\log(120 \div 240) = -126 \ldots -120 \text{ dBc/Hz}.\] (3)

Considering the noise parameters of the developed oscillator [8-9] and equations (2), (3), we can conclude that $BW \approx 1.5 \div 2$ MHz.

2.3. Calculation of loop filter

Figure 2 shows circuit of active filter based on OPAx211 series op amp.

![Figure 2. Circuit of active filter](image)

This circuit is the most common configuration of loop filter designed to work with high-voltage VCO.

Considering defined loop bandwidth (see subsection 2.2) and using a special program for LTC6947 chip («Linear Technology FracNWizard»), we can calculate all filter parameters: 1) $C_1 = C_3 = 39 \text{ pF}$, $L = 2.2 \text{ uH}$, $R_1 = R_2 = 374 \text{ Ohms}$, and $C_2 = 960 \text{ pF}$ for $R = 1$; 2) $C_1 = C_3 = 20 \text{ pF}$, $L = 4.7 \text{ uH}$, $R_1 = R_2 = 698 \text{ Ohms}$, and $C_2 = 510 \text{ pF}$ for $R = 2$.

In fact, when calculating filter parameters, we can vary by 2 parameters: $K_{VCO}$ ($K_{VCO}$ is parameter of VCO measured in MHz/V) and $I_{CP}$ ($I_{CP}$ is parameter of PFD chip measured in mA).

Studies have shown that using a geometric mean of $K_{VCO}$ gives the best results. In some cases this geometric mean of $K_{VCO}$ provides 2 dBc/Hz less noise parameter than an arithmetic mean of $K_{VCO}$.

It was also found that when calculating the filter parameters it is best to choose the average current value of the charge pump, or slightly less than the average. If necessary, this makes it possible to change value of $I_{CP}$ in both directions (in the direction of decreasing and in the direction of increasing) in order to ensure the most optimal value of $BW$.

3. Experiments

A CXA signal analyzer N9000A (9kHz to 26.5 GHz) [16] was used for the experiments.

Figure 3 shows several plots of this PLL synthesizer (see figure 1) phase noise power spectral density versus offset frequency obtained during the experimental studies.
Figure 3. PLL synthesizer noise characteristics for $f = 8$ GHz: (a) $R = 1$; (b) $R = 2$
Table 1 shows the calculated \((L_{PLL_{calc}})\) and measured \((L_{PLL_{exp}})\) values of phase noise power spectral density for \(R = 1\).

**Table 1. Phase noise power spectral density of PLL synthesizer for \(R = 1\).**

| \(f\) (GHz) | \(L_{PLL_{calc}}\) (dBc/Hz) | \(L_{PLL_{exp}}\) (dBc/Hz) |
|-------------|-------------------------------|-----------------------------|
| 6.4         | -109.9                        | -108.5                      |
| 7           | -109.1                        | -107.6                      |
| 8           | -107.9                        | -106.4                      |
| 9           | -106.9                        | -105.1                      |
| 10          | -106.0                        | -104.2                      |
| 11          | -105.2                        | -103.3                      |
| 12          | -104.4                        | -102.0                      |

Table 2 shows the calculated \((L_{PLL_{calc}})\) and measured \((L_{PLL_{exp}})\) values of phase noise power spectral density for \(R = 2\).

**Table 2. Phase noise power spectral density of PLL synthesizer for \(R = 2\).**

| \(f\) (GHz) | \(L_{PLL_{calc}}\) (dBc/Hz) | \(L_{PLL_{exp}}\) (dBc/Hz) |
|-------------|-------------------------------|-----------------------------|
| 6           | -107.4                        | -106.2                      |
| 7           | -106.1                        | -104.8                      |
| 8           | -104.9                        | -103.8                      |
| 9           | -103.9                        | -102.6                      |
| 10          | -102.9                        | -101.6                      |
| 11          | -102.1                        | -101.4                      |
| 12          | -101.4                        | -101.3                      |

Table 1 and table 2 show good agreement between calculated and measured values of phase noise power spectral density.

Thus, studies have shown that on the basis of the developed oscillator it is possible to design a working wideband PLL synthesizer. Note that the measured characteristics are in good agreement with the calculation results. That’s why the developed wideband VCO may be used in PLL synthesizers.

4. **Conclusion**

Following the studies conducted, wideband PLL synthesizer based on the developed hybrid VCO has been designed. This device ensures the frequency tuning in the range from 6 to 12 GHz. Note that phase noise is in good agreement with the calculation results.

The developed VCO may be used for the implementation of wideband PLL system.
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