Mask-programmable on-chip photovoltaic cell array

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Abstract. We propose a gate-array style easy configuration method for voltage photovoltaic cell for rapid prototyping of on-chip IoT system. Using the same design chips fabricated by standard CMOS process and only changing the mask pattern for post processes, we successfully achieved two type chips: one generates 68 V open circuit voltage output photovoltaic cell and the other does 10 times higher short circuit current than it with 5.4 V open circuit voltage output.

1. Introduction

More and more applications of IoT devices are now proposed and each device requires different characteristic for power sources, and photovoltaic cells are widely used because of its high efficiency. A simple photovoltaic cell, however, can only generate low open circuit voltage (0.7 V ~ 1.1 V), which is not necessarily enough to drive the component of IoT devices, such as LSIs and sensors. Getting higher voltage without loss of area and energy, cells have to be connected serially corresponding to its purpose. To achieve this, serial connection of photovoltaic cells is employed and to connect these cells on a chip, some methods are reported (Ref.[1] and Ref.[2]). Among these methods, we proposed the photovoltaic diodes fabricated by post-CMOS process (Ref.[3]). This method can carry out the conventional bulk CMOS process without forming on SOI wafers, thus we could achieve high-quality photovoltaic cells with low cost. However, to modify the output characteristics, the method requires whole design modification with high cost and taking time. Therefore, simple modification method is needed, which is very attractive for fast prototyping of IoT devices.

In this paper, we propose gate-array style easy configuration method for getting required characteristic photovoltaic cells.

Figure 1. Connection and output characteristics configuration method.
(a)Before CMOS post-processed four diodes. Only anodes are connected by substrate.
(b) Serially connected four diodes for getting higher voltage. Each diode is mesa-isolated.
(c) Parallel connected four diodes for getting higher current.
2. Proposal Method

Figure 1 shows the configuration method of four diode connection. Each side of a diode has eight connectors for wiring with other diodes. After standard CMOS fabrication, diodes are connected as shown in Fig. 1(a). All anodes are connected by substrate and cathodes are isolated. To connect these diodes serially for getting higher voltage (Figure 1(b)), these diodes are wired from anode side connector to cathode side one, and all diodes have to mesa-isolated. For getting higher current (Figure 1(c)), diodes are wired from cathodes connector to cathodes one, and these diodes are not mesa-isolated to keep their anodes connected.

3. Experiment

In this experiment, we designed 12 by 12 diodes on 7.5 mm by 7.5 mm chip for master slice. This design wafers are fabricated by foundry service on SOI wafers, whose thickness of device layer was 9 µm. For the demonstration, we fabricated two types design. One was that all diodes were connected in series for generating highest voltage which this design chip could generate (type A). The other was each row (12 diodes) were connected parallel, and columns were connected serially. This version is designed for driving LSIs, which require around 5 V (type B).

With those designs, two chips ware fabricated at the same time. Wires were patterned at first, and following process was almost the same as the previous research (Ref.[3]). Figure 2(a) shows the fabricated PV cell array (type A), and the close-up SEM image (Figure 2(b)) shows all the PV cells are completely isolated. These chips ware measured with light bulb and semiconductor device parameter analyzer (Keysight B1500A).

4. Results

Measurement results were illustrated as shown in Figure 3. Type A generated 68 V open circuit voltage with 15 µA short circuit current, and fill factor was 68%. Type B generated 5.4 V open circuit voltage with 150 µA short circuit current, and fill factor was 77%.

References

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