Performance Comparison of LDPC Block and Spatially Coupled Codes over GF(q)

Kechao Huang, Student Member, IEEE, David G. M. Mitchell, Member, IEEE, Lai Wei, Student Member, IEEE, Xiao Ma, Member, IEEE, and Daniel J. Costello, Jr., Life Fellow, IEEE

Abstract

In this paper, we compare the finite-length performance of protograph-based spatially coupled low-density parity-check (SC-LDPC) codes and LDPC block codes (LDPC-BCs) over GF(q). In order to reduce computational complexity and latency, a sliding window decoder with a stopping rule based on a soft bit-error-rate (BER) estimate is used for the q-ary SC-LDPC codes. Two regimes are considered: one when the constraint length of q-ary SC-LDPC codes is equal to the block length of q-ary LDPC-BCs and the other when the two decoding latencies are equal. Simulation results confirm that, in both regimes, (3, 6)-, (3, 9)-, and (3, 12)-regular non-binary SC-LDPC codes can significantly outperform both binary and non-binary LDPC-BCs and binary SC-LDPC codes. Finally, we present a computational complexity comparison of q-ary SC-LDPC codes and q-ary LDPC-BCs under equal decoding latency and equal decoding performance assumptions.

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K. Huang and X. Ma are with the Department of Electronics and Communication Engineering, Sun Yat-sen University, Guangzhou, GD 510006, China (e-mail: hkech@mail2.sysu.edu.cn; maxiao@mail.sysu.edu.cn). K. Huang is also with the Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556, USA.

D. G. M. Mitchell, L. Wei, and D. J. Costello, Jr. are with the Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556, USA (e-mail: david.mitchell@nd.edu; lwei1@nd.edu; costello.2@nd.edu).
Index Terms

Decoding latency, LDPC block codes, LDPC convolutional codes, protograph-based codes, $q$-ary LDPC codes, spatially coupled codes.

I. INTRODUCTION

Low-density parity-check block codes (LDPC-BCs) [1], combined with low complexity belief propagation (BP) decoding algorithms, are a class of capacity-approaching codes with decoding complexity that increases only linearly with block length [2]. In [1], in addition to binary LDPC-BCs, Gallager also introduced a class of non-binary LDPC-BCs defined over an arbitrary alphabet size. In [3], Davey and MacKay considered LDPC-BCs defined over a finite field $\text{GF}(q)$, $q \geq 2$, and generalized Gallager’s BP decoding algorithm for binary LDPC-BCs to a $q$-ary sum-product algorithm (QSPA) and demonstrated that $q$-ary LDPC-BCs achieve excellent performance. To reduce decoding complexity, a more efficient QSPA based on the fast Fourier transform (called FFT-QSPA) was proposed in [4]. In addition, extended min-sum (EMS) algorithms [5–7] can be used to further reduce decoding complexity. Due to their excellent decoding performance for short-to-moderate block lengths [3], $q$-ary LDPC-BCs have received significant attention in the recent literature [8–11].

The convolutional counterpart of LDPC-BCs, called spatially coupled LDPC (SC-LDPC) codes, was proposed in [12]. Analogous to LDPC-BCs, SC-LDPC codes are defined by sparse parity-check matrices, which allow them to be decoded using iterative message-passing algorithms, such as BP decoding algorithms. It was shown in [13] that the BP decoding thresholds of SC-LDPC code ensembles are numerically indistinguishable from the maximum a posteriori (MAP) decoding thresholds of underlying regular and irregular LDPC-BC ensembles. Subsequently, it was proven that random SC-LDPC code ensembles exhibit threshold saturation, i.e., they achieve the MAP thresholds of the underlying LDPC-BCs, on memoryless binary-input symmetric-output channels under BP decoding, which in turn implies that SC-LDPC codes can achieve capacity by increasing the density of the parity-check matrix [14, 15]. In [12], a parallel, high-speed, pipeline-decoding architecture for binary SC-LDPC codes was introduced, and several implementation aspects of the pipeline decoder were discussed in [16]. However, since capacity approaching performance can require a large number of iterations, the latency and memory requirements of the pipeline decoder, which depend on the number of iterations, may be unacceptably high.
In [17], a sliding window decoding architecture with reduced latency and memory requirements was proposed. This is a variant of the sliding window decoder introduced in [13] for the purpose of iterative decoding threshold analysis. A construction method for $q$-ary SC-LDPC codes was introduced in [18], and in [19] the authors proved that the threshold saturation effect proved in [14] for binary SC-LDPC codes also holds for $q$-ary SC-LDPC codes on the binary erasure channel (BEC). Recently, based on numerical techniques, the threshold performance of $q$-ary SC-LDPC codes constructed from protographs [20] with sliding window decoding was presented in [21, 22].

In contrast to [21, 22], in which the authors consider an asymptotic performance analysis of $q$-ary SC-LDPC codes, in this paper we focus on finite-length performance comparisons of protograph-based $q$-ary SC-LDPC codes and $q$-ary LDPC-BCs, assuming transmission over a binary-input additive white Gaussian noise (BI-AWGN) channel. Due to the large decoding latency of the pipeline-decoding architecture, a sliding window decoder for $q$-ary SC-LDPC codes is considered. In order to reduce computational complexity, a stopping rule based on a soft bit-error-rate (BER) estimate is applied to the iterative decoding process. Two regimes are considered: one when the constraint length of $q$-ary SC-LDPC codes is equal to the block length of $q$-ary LDPC-BCs and the other when the two decoding latencies are equal. We also investigate the relationship between the protograph lifting factor, the decoding window size, and the decoding performance of $q$-ary SC-LDPC codes when the decoding latency is fixed. Finally, we compare the computational complexity of $q$-ary SC-LDPC codes to $q$-ary LDPC-BCs when either the decoding latency or the decoding performance is fixed.

The paper is structured as follows. In Section II, we give a brief review of protograph-based LDPC-BCs and then describe the construction of protograph-based $q$-ary SC-LDPC codes. In Section III, we describe the pipeline and sliding window decoding architectures and introduce a stopping rule based on a soft BER estimate for $q$-ary SC-LDPC codes. In Section IV, we present a performance comparison of $q$-ary SC-LDPC codes and $q$-ary LDPC-BCs when the constraint length of $q$-ary SC-LDPC codes is equal to the block length of $q$-ary LDPC-BCs, and in Section V we compare their performance on the basis of equal decoding latency. Then, in Section VI, we compare the computational complexity of $q$-ary SC-LDPC codes and $q$-ary LDPC-BCs under equal decoding latency and equal decoding performance assumptions. Finally, some concluding remarks are given in Section VII.
II. PROTOGRAPH-BASED LDPC CODES OVER GF(\(q\))

A. LDPC-BCs over GF(\(q\))

A block code protograph with design rate \(R = b/c\) is a small bipartite graph with \(c\) variable nodes and \(c-b\) check nodes, which can be used to derive the graph of design rate \(R = b/c\) block codes of various block sizes with the same degree distribution.\(^1\) An example of a block code protograph with \(c = 2\) variable nodes of degree 3 and \(c-b = 1\) check node of degree 6 is shown in Fig. 1. Let GF(\(q\)) be a finite field with \(q = 2^m\) elements, where \(m\) is the number of bits used to represent a symbol over GF(\(q\)). Let \(M\) (typically a large integer) be the protograph lifting factor. A \(q\)-ary LDPC-BC with code length \(n_{BC} = Mc\) can be obtained from the \((c-b) \times c\) bi-adjacency matrix \(B = [B_{i,j}]\) of the protograph, called the base matrix, via the following two steps:

1) replace each nonzero entry \(B_{i,j}\) in \(B\) with a summation of \(B_{i,j}\) nonoverlapping \(M \times M\) permutation matrices and each zero entry in \(B\) with the \(M \times M\) all-zero matrix, where the elements \(B_{i,j}\) in \(B\) are non-negative integers and the permutation matrices are chosen randomly and independently, resulting in a binary parity-check matrix \(H\) that is \(M\) times as large as \(B\), and

2) replace the nonzero entries in \(H\) with randomly selected nonzero elements from the finite field GF(\(q\)), resulting in a \(q\)-ary parity-check matrix \(H_{BC}\) of a \(q\)-ary LDPC-BC.

For LDPC-BCs, data is typically transmitted in a sequence of independent blocks. At the decoder, an entire block must be received before BP decoding begins. Consequently, the decoding latency for a \(q\)-ary LDPC-BC constructed as described above over GF(\(q\)), in terms of bits, is

\(^1\)The term “design rate” is used since the resulting parity-check matrix may have redundant rows. In this case, the code rate is slightly higher than the design rate.
given by
\[ T_{BC} = n_{BC} \cdot m = Mmc. \] (1)

B. SC-LDPC Codes over GF(q)

Analogous to LDPC-BCs, SC-LDPC codes can also be derived using the protograph expansion method. Consider a \((c - b) \times c\) base matrix \(B\). We can use an edge spreading technique [23] to construct a rate \(R = b/c\) spatially coupled convolutional base matrix with syndrome former memory \(m_s\) from \(B\) as

\[
B_{SC} = \begin{bmatrix}
B_0 \\
B_1 & B_0 \\
\vdots & \vdots & \ddots \\
B_{m_s} & \ddots & \ddots \\
\end{bmatrix},
\] (2)

where the \(m_s + 1\) component submatrices \(B_0, B_1, \ldots, B_{m_s}\), each of size \((c - b) \times c\), satisfy

\[
\sum_{i=0}^{m_s} B_i = B.
\] (3)

An example of a rate \(R = 1/2\) \((3, 6)\)-regular SC-LDPC code protograph with \(m_s = 1\) constructed using the edge spreading procedure is shown in Fig. 2. The graph lifting operation is then applied to \(B_{SC}\) by replacing each nonzero entry in \(B_{SC}\) with (a sum of) randomly selected permutation matrices of size \(M \times M\) and each zero entry in \(B_{SC}\) with the \(M \times M\) all-zero matrix, as described above, and then replacing the nonzero entries in the resulting convolutional parity-check matrix \(H_{SC}\) with randomly selected nonzero elements from the finite field \(GF(q)\), resulting in an unterminated \(q\)-ary SC-LDPC code with constraint length \(v_s = (m_s + 1)Mc.\)

The resulting \(q\)-ary SC-LDPC parity-check matrix \(H_{SC}\) is given in (4), where the blank spaces in \(H_{SC}\) correspond to zeros and the submatrices \(H_i(t)\) have size \((c - b)M \times cM\), \(\forall i, t:\)

\[ H_{SC} = \begin{bmatrix}
\vdots & \vdots & \ddots & \vdots \\
\vdots & \vdots & \ddots & \vdots \\
\vdots & \vdots & \ddots & \vdots \\
\vdots & \vdots & \ddots & \vdots \\
\end{bmatrix}.
\] (4)

\(^2\)The constraint length determines the maximal width (in symbols) of the nonzero area of \(H_{SC}\).
A $(3,6)$-regular SC-LDPC code protograph with $m_s = 1$ constructed using the edge spreading procedure. The component submatrices used in the edge spreading are $B_0 = [2 \ 1]$ and $B_1 = [1 \ 2]$, where $B = [3 \ 3]$ is the base matrix of the underlying LDPC-BC.

$$H_{SC} = \begin{bmatrix}
H_0(0) & H_0(1) & \cdots & \cdots \\
H_1(1) & H_0(1) & \cdots & \cdots \\
\vdots & \vdots & \ddots & \ddots \\
H_{m_s}(m_s) & H_{m_s-1}(m_s) & \cdots & H_0(m_s) \\
H_{m_s}(m_s+1) & H_{m_s-1}(m_s+1) & \cdots & H_0(m_s+1) \\
\vdots & \vdots & \ddots & \ddots 
\end{bmatrix}.$$  (4)

In this paper, we restrict consideration to SC-LDPC codes with syndrome former memory $m_s = 1$, due to their superior performance with sliding window decoding (see, e.g., [17, 21, 22, 24, 25]). We also focus our attention on $(d_v, d_c)$-regular SC-LDPC codes, i.e., codes whose parity-check matrices have constant weight $d_v$ in each column and constant weight $d_c$ in each row, due to their complexity advantage compared to irregular codes and the fact that $(d_v, d_c)$-regular SC-LDPC code ensembles are capable of achieving capacity (see [13–15]).

In order to compare LDPC-BCs and SC-LDPC codes fairly, the freedom to select permutation matrices has been fixed in the following way. Consider two matrices $B_0$ and $B_1$, each of size $(c - b) \times c$, chosen such that $B_0 + B_1$ is $(d_v, d_c)$-regular. The base matrix of a $(d_v, d_c)$-regular
LDPC-BC is constructed as

$$B_{BC} = \begin{bmatrix} B_0 & B_1 \\ B_1 & B_0 \end{bmatrix}_{2(c-b)\times2c},$$

where $B_{BC}$ has weight $d_v$ in each column and weight $d_c$ in each row.\(^3\) Then the block protograph expansion method described in Section II-A is used to form the parity-check matrix of a $(d_v, d_c)$-regular LDPC-BC as

$$H_{BC} = \begin{bmatrix} H_0(0) & H_1(2) \\ H_1(1) & H_0(1) \end{bmatrix}_{2(c-b)M\times2cM}.$$  

We construct the related SC-LDPC code in the following way. A $(d_v, d_c)$-regular SC-LDPC base matrix is constructed in the form of (2) using component submatrices $B_0$ and $B_1$ as

$$B_{SC} = \begin{bmatrix} B_0 \\ B_1 & B_0 \\ & B_1 & B_0 \\ & & B_1 & \cdots \\ & & & \cdots \end{bmatrix},$$

and a $(d_v, d_c)$-regular SC-LDPC parity-check matrix is then constructed using the usual protograph expansion method as

$$H_{SC} = \begin{bmatrix} H_0(0) \\ H_1(1) & H_0(1) \\ & H_1(2) & H_0(0) \\ & & H_1(1) & H_0(1) \\ & & & \cdots \end{bmatrix}.$$  

Remarks: Note that the SC-LDPC code is time-varying with period 2, and its parity-check matrix $H_{SC}$ uses exactly the same permutation matrices and elements from GF($q$) as $H_{BC}$, now repeated periodically. This construction can be viewed as the unwrapping approach first presented in [12] for deriving an SC-LDPC code from an LDPC-BC. Note also that, even though we refer

\(^3\)The “weight” of a row (column) of $B_{BC}$ is the real sum of all the non-zero entries in the row (column).
TABLE I

Component matrices used in the construction of \((d_v, d_c)\)-regular \(q\)-ary LDPC-BCs and \(q\)-ary SC-LDPC codes with field size \(q = 2^m\)

| Codes             | Component matrices | Block/constraint length |
|-------------------|--------------------|-------------------------|
| \((2, 4)\)-regular | \(B_0 = B_1 = [1 \ 1]\) | \(4Mm\)                |
| \((3, 6)\)-regular | \(B_0 = [2 \ 1], B_1 = [1 \ 2]\) | \(4Mm\)                |
| \((3, 9)\)-regular | \(B_0 = [1 \ 2 \ 2], B_1 = [2 \ 1 \ 1]\) | \(6Mm\)                |
| \((3, 12)\)-regular| \(B_0 = [1 \ 1 \ 2 \ 2], B_1 = [2 \ 2 \ 1 \ 1]\) | \(8Mm\)                |

to a \((d_v, d_c)\)-regular SC-LDPC base matrix and code, \(B_{SC}\) is not exactly \((d_v, d_c)\)-regular, since its first \((c - b)\) rows have weight less than \(d_c\). This slight “structured irregularity” associated with \((d_v, d_c)\)-regular SC-LDPC codes is in fact the reason behind their capacity-approaching thresholds (see, e.g., [13]).

The parity-check matrices \(H_{BC}\) and \(H_{SC}\) of \((d_v, d_c)\)-regular \(q\)-ary LDPC-BCs and \(q\)-ary SC-LDPC codes are constructed over \(GF(q)\) in the form of (6) and (8), respectively, using the component submatrices shown in Table I. Given a protograph lifting factor \(M\), the block length (in bits) of the \((d_v, d_c)\)-regular \(q\)-ary LDPC-BCs and the constraint length (in bits) of the \((d_v, d_c)\)-regular \(q\)-ary SC-LDPC codes are both equal to \(2Mmc\), where the field size is \(q = 2^m\).

III. PIPELINE AND SLIDING WINDOW DECODING FOR SC-LDPC CODES OVER \(GF(q)\)

Although the Tanner graph of a \(q\)-ary SC-LDPC code has an infinite number of nodes, the distance between two variable nodes that are connected to the same check node is limited by the constraint length of the code. This restriction gives rise to efficient decoder implementations such as the high-throughput pipeline decoder [12, 16] and the low-latency sliding window decoder [13, 17, 24].

A. Pipeline Decoding

An example of a pipeline decoder operating on the protograph of a \((3, 6)\)-regular \(q\)-ary SC-LDPC code with \(m_s = 1\) is shown in Fig. 3(a). Given some fixed number \(I\) of decoding iterations, the pipeline decoder employs \(I\) identical copies of a message-passing processor operating in parallel.\(^4\) Each processor includes only one constraint length, i.e., \(v_s = (m_s + 1)Mc\), of variable

\(^{4}\)A serial decoding architecture [26] can be used to reduce the number of processors at a cost of reduced throughput.
Fig. 3. (a) Example of a pipeline decoder operating on the protograph of a (3, 6)-regular q-ary SC-LDPC code with \( m_s = 1 \). (b) Example of a sliding window decoder with window size \( W = 3 \) operating on the protograph of the same (3, 6)-regular q-ary SC-LDPC code with \( m_s = 1 \) at times \( t = 0 \) (left), and \( t = 1 \) (right).

nodes, and during a single decoding iteration messages are only passed within a single processor, so equating the processor complexity of SC-LDPC codes and LDPC-BCs means equating the constraint length of SC-LDPC codes to the block length of LDPC-BCs [16, 27]. Note that \( I v_s = I (m_s + 1) M c \) represents the total decoding latency in received symbols and the total number of soft received values that must be stored in the decoder memory at any given time. Since capacity approaching performance can require a large number of iterations \( I \), these latency and memory requirements of pipeline decoding may be unacceptably high.

B. Sliding Window Decoding

In this subsection, we propose a sliding window decoding architecture for q-ary SC-LDPC codes, which is an extension of the sliding window decoding architecture presented in [17] for binary SC-LDPC codes.

An example of a sliding window decoder with window size \( W = 3 \) operating on the protograph of a (3, 6)-regular q-ary SC-LDPC code with \( m_s = 1 \) is shown in Fig. 3(b). Assuming a window size of \( W M c \) symbols, decoding proceeds until a fixed number of iterations has been performed or some stopping rule (see Section III-C) is satisfied, after which the window shifts \( M c \) positions and the \( M c \) symbols shifted out of the window are decoded. The first \( M c \) symbols in any window
are called target symbols. The decoding latency of the sliding window decoder for \( q \)-ary SC-LDPC codes, in terms of bits, is given by

\[
T_{SC} = WMmc. \tag{9}
\]

The iterative decoding algorithm within a window can be implemented with existing algorithms, such as the FFT-QSPA [4], EMS algorithms [5–7], and so on.

C. A Stopping Rule for Sliding Window Decoding

For LDPC-BCs, iterative decoding is stopped if the decoded sequence is a valid codeword, i.e., if and only if all of the parity-check equations are satisfied. However, this stopping rule cannot be used with sliding window decoding of SC-LDPC codes, because we only decode one set of target symbols at a time. In this subsection, we propose a stopping rule based on a soft BER estimate for sliding window decoding of \( q \)-ary SC-LDPC codes, which is motivated by the method presented in [25].

Let \( P_t^{(j)}(b) \) for \( 0 \leq j < Mc \) be the probability that the \( j \)-th symbol \( v_t^{(j)} \) in a window at time \( t \) is \( b \in \text{GF}(q) \), given the decoder input from the channel and the constraints of the \( q \)-ary SC-LDPC code. After each iteration of the BP algorithm at time \( t \), we make hard decisions \( \hat{v}_t^{(j)} \) on \( v_t^{(j)} \) based on the probabilities \( P_t^{(j)}(x), x \in \text{GF}(q) \), computed at the decoder by choosing \( \hat{v}_t^{(j)} = x \) as the symbol with the maximum probability. The probability that \( \hat{v}_t^{(j)} \) is wrong is then given by

\[
e_t^{(j)} = 1 - P_t^{(j)}(x = \hat{v}_t^{(j)}), \tag{10}
\]

and the estimated soft BER \( \hat{P}_t \) can be calculated as

\[
\hat{P}_t = \frac{1}{Mc} \sum_{j=0}^{Mc-1} e_t^{(j)}. \tag{11}
\]

The proposed stopping rule is as follows: the window shifts only when either a fixed number of iterations \( I_{\text{max}} \) has been performed or \( \hat{P}_t \) is less than a preselected target BER.

In the simulation results presented in this paper, the nodes within a decoding window are updated according to a uniform parallel (flooding) schedule, so that all the nodes within the window are updated in parallel during each decoding iteration. Note, however, that the node updates can also be performed serially and/or non-uniformly in order to reduce computational complexity (see, e.g., [28, 29]).
Fig. 4. Required $E_b/N_0$ to achieve a BER of $10^{-4}$ with different protograph lifting factors $M$ for $(2, 4)$-regular codes over $GF(2)$, $GF(4)$, $GF(8)$, $GF(16)$, and $GF(32)$. The window size of the sliding window decoder is $W = 12$. Solid curves represent LDPC-BCs, while dotted curves represent SC-LDPC codes.

IV. AN EQUAL BLOCK LENGTH AND CONSTRAINT LENGTH COMPARISON

In this section, we focus on the case of equal decoder processor (hardware) complexity, i.e., when the constraint length of the $q$-ary SC-LDPC codes is equal to the block length of the $q$-ary LDPC-BCs. We consider binary phase-shift keying (BPSK) modulation over the BI-AWGN channel. For $q$-ary LDPC-BCs, the FFT-QSPA with the parity-check-based stopping rule is applied with $I_{\text{max}}$ set to 100. For $q$-ary SC-LDPC codes, sliding window decoding is also implemented with the FFT-QSPA, $I_{\text{max}}$ is set to 100, and the stopping rule proposed in Section III-C with a preselected target BER of $10^{-6}$.

A. $(2, 4)$-Regular LDPC Codes over $GF(q)$

The values of the bit signal-to-noise ratio (SNR) $E_b/N_0$ needed to achieve a BER of $10^{-4}$ with different protograph lifting factors $M$ for rate $R = 1/2$ $(2, 4)$-regular codes over $GF(2)$,

\footnote{It should be noted that, in this case, the latency of the SC-LDPC code is higher than for the LDPC-BC. An equal latency comparison is the subject of the next section.}
GF(4), GF(8), GF(16), and GF(32) are shown in Fig. 4. The window size of the sliding window decoder for the $q$-ary SC-LDPC codes is $W = 12$. From Fig. 4, we see that the performance of $(2,4)$-regular $q$-ary LDPC-BCs and $q$-ary SC-LDPC codes improves as the protograph lifting factor $M$ increases. We also see that $(2,4)$-regular $q$-ary SC-LDPC codes with short constraint length (corresponding to small $M$) achieve substantial “convolutional gains” compared to the underlying LDPC-BCs, but the gains diminish as the protograph lifting factor $M$ increases. For example, the convolutional gain of the SC-LDPC code compared to the LDPC-BC over GF(16) when $M = 24$ is about 1.0 dB, but it decreases to only 0.2 dB when $M = 480$. These results are consistent with the asymptotic (large $M$) threshold performance analysis presented in [22], where the thresholds of $(2,4)$-regular SC-LDPC codes with these field sizes are shown to be only slightly better than those of $(2,4)$-regular LDPC-BCs.

It is also observed in [22] that, compared to $(2,4)$-regular $q$-ary SC-LDPC codes, $(d_v,d_c)$-regular $q$-ary SC-LDPC codes with $d_v \geq 3$ provide capacity-approaching performance using window decoding when both the field size $q$ and the window size $W$ are relatively small. Since small $q$ is desirable to reduce complexity and small $W$ is desirable to reduce latency, we focus on $(d_v,d_c)$-regular $q$-ary LDPC codes with $d_v \geq 3$ in the rest of the paper.

B. $(3,6)$-Regular LDPC Codes over GF($q$)

The values of $E_b/N_0$ needed to achieve a BER of $10^{-4}$ with different protograph lifting factors $M$ for rate $R = 1/2$ $(3,6)$-regular codes over GF(2), GF(4), GF(8), and GF(16) are shown in Fig. 5. The window size of the sliding window decoder for the $q$-ary SC-LDPC codes is $W = 12$. Similar to the $(2,4)$-regular $q$-ary codes, we see in Fig. 5 that the performance of the $(3,6)$-regular $q$-ary LDPC-BCs and $q$-ary SC-LDPC codes improves as the protograph lifting factor $M$ increases. We also observe that $(3,6)$-regular $q$-ary SC-LDPC codes achieve substantial convolutional gains compared to the underlying LDPC-BCs over the entire range of lifting factors, with the amount of gain declining gradually as $M$ increases. For example, the convolutional gain of the SC-LDPC code compared to the LDPC-BC over GF(8) when $M = 48$ is about 1.1 dB, and it decreases to around 0.8 dB for $M = 320$. By comparing Figs. 4

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6We choose BERs of $10^{-4}$ ($10^{-5}$ in Section V) for comparison because they represent target BERs commonly used in many practical applications.
Fig. 5. Required $E_b/N_0$ to achieve a BER of $10^{-4}$ with different protograph lifting factors $M$ for $(3,6)$-regular codes over GF(2), GF(4), GF(8), and GF(16). The window size of the sliding window decoder is $W = 12$. Solid curves represent LDPC-BCs, while dotted curves represent SC-LDPC codes.

and 5, we see that the convolutional gains, relative to the LDPC-BCs, of the $(3,6)$-regular SC-LDPC codes are larger than those of the $(2,4)$-regular SC-LDPC codes. This is again consistent with the asymptotic threshold performance analysis presented in [22], where the thresholds of $(3,6)$-regular SC-LDPC codes are shown to be substantially better than those of $(3,6)$-regular LDPC-BCs.

**Remark:** Although it has been reported in [13] that the BP thresholds of $(4,8)$-regular binary SC-LDPC codes are better than those of $(3,6)$-regular binary SC-LDPC codes, we found from simulation that $(3,6)$-regular $q$-ary SC-LDPC codes perform better than $(4,8)$-regular $q$-ary SC-LDPC codes at (low) SNRs and when (short-to-moderate) constraint lengths are considered, i.e., $(4,8)$-regular SC-LDPC codes typically require a large lifting factor $M$ to outperform $(3,6)$-regular SC-LDPC codes. This is consistent with the discussion concerning the practical design of SC-LDPC codes in Section VI-A of [14], where it is noted that large (variable node and check node) degrees imply slower convergence for finite-length ensembles to the asymptotic performance limit. For these reasons, we focus the rest of our discussion on $(d_v, d_c)$-regular $q$-ary SC-LDPC codes for which the variable node degree is fixed at $d_v = 3$. 
Fig. 6. Required $E_b/N_0$ to achieve a BER of $10^{-4}$ with different protograph lifting factors $M$ for high-rate codes over GF(2), GF(4), GF(8), and GF(16). The window size of the sliding window decoder is $W = 12$. Solid curves represent LDPC-BCs, while dotted curves represent SC-LDPC codes.
C. High-Rate LDPC Codes over $GF(q)$

The values of $E_b/N_0$ needed to achieve a BER of $10^{-4}$ with different protograph lifting factors $M$ for rate $R = 2/3$ and $3/4$ $(3, 9)$- and $(3, 12)$-regular codes over $GF(2)$, $GF(4)$, $GF(8)$, and $GF(16)$ are shown in Fig. 6. The window size of the sliding window decoder for the $q$-ary SC-LDPC codes is $W = 12$. From Fig. 6, we see that the performance of $(3, 9)$-regular and $(3, 12)$-regular $q$-ary LDPC-BCs and $q$-ary SC-LDPC codes improves as the protograph lifting factor $M$ increases. We also observe that both $(3, 9)$-regular and $(3, 12)$-regular $q$-ary SC-LDPC codes achieve substantial convolutional gains compared to the underlying LDPC-BCs over the entire range of lifting factors, with the amount of gain declining gradually as $M$ increases. This is again consistent with the asymptotic threshold performance analysis presented in [22], where the thresholds of $(3, 9)$- and $(3, 12)$-regular SC-LDPC codes are shown to be substantially better than those of $(3, 9)$- and $(3, 12)$-regular LDPC-BCs, respectively.

V. AN EQUAL LATENCY COMPARISON

In addition to decoding performance, the latency introduced by employing channel coding is a crucial factor in the design of a practical communication system. For example, minimizing latency is of major importance in applications such as personal wireless communication, real-time audio and video, and command and control military communication. In this section, we consider the case when the decoding latency of $q$-ary SC-LDPC codes and $q$-ary LDPC-BCs is the same.

A. $(3, 6)$-Regular LDPC Codes over $GF(q)$

For the rate $R = 1/2$ $(3, 6)$-regular $q$-ary SC-LDPC codes with $H_{SC}$ given by (8), the decoding latency of the sliding window decoder is given by

$$T_{SC} = 2WM_{SC}m,$$

whereas the rate $R = 1/2$ $(3, 6)$-regular $q$-ary LDPC-BCs with $H_{BC}$ given by (6) have decoding latency

$$T_{BC} = 4M_{BC}m,$$

where we now distinguish between the lifting factors $M_{SC}$ of the SC-LDPC codes and $M_{BC}$ of the LDPC-BCs.
In Fig. 7, (3,6)-regular 8-ary SC-LDPC codes are compared to (3,6)-regular 8-ary LDPC-BCs and the values of the protograph lifting factors $M_{SC}$ and $M_{BC}$ are chosen such that the decoding latency of the LDPC-BCs and the SC-LDPC codes are the same. Even in this case, we see that the performance of the SC-LDPC codes is still significantly better than that of the LDPC-BCs. From Fig. 7, we also see that the SC-LDPC code constructed with a larger lifting factor $M_{SC}$ and decoded with a smaller window size $W = 6$ outperforms the SC-LDPC code constructed with a smaller $M_{SC}$ and decoded with a larger window size $W = 12$ (both have the same decoding latency). In other words, selecting a smaller $W$, which is typically detrimental to decoder performance, is compensated for by allowing a larger $M_{SC}$, which improves code performance. For example, at a BER of $10^{-5}$, the 8-ary SC-LDPC code with $M_{SC} = 64$ and decoded with window size $W = 12$ gains 0.3 dB compared to the equal latency 8-ary LDPC-BC with $M_{BC} = 384$, while the gain increases to 0.4 dB by using the 8-ary SC-LDPC code with $M_{SC} = 128$ and $W = 6$. Similar behavior for binary SC-LDPC codes was reported in [24, 25].

The $E_b/N_0$ required to achieve a BER of $10^{-5}$ for equal latency (3,6)-regular 8-ary LDPC-BCs and (3,6)-regular 8-ary SC-LDPC codes as a function of decoding latency is shown in Fig. 8, where we observe that the performance of the SC-LDPC codes (with fixed protograph
Fig. 8. Required $E_b/N_0$ to achieve a BER of $10^{-5}$ for (3,6)-regular 8-ary LDPC-BCs and (3,6)-regular 8-ary SC-LDPC codes as a function of decoding latency.

The lifting factor $M_{SC}$ improves as the window size $W$ (and hence the latency) increases, but it does not improve much further beyond a certain window size (roughly $W = 10$). Also, beyond a certain latency, using a larger protograph lifting factor $M_{SC}$ with a smaller window size $W$ gives better performance. For example, when the decoding latency is 2304 bits, the performance of the 8-ary SC-LDPC code with $M_{SC} = 64$ and decoded with $W = 6$ is better than that of the SC-LDPC code with $M_{SC} = 32$ and decoded with $W = 12$ and, when the decoding latency is 4608 bits, the performance with $M_{SC} = 128$ and $W = 6$ is better than with $M_{SC} = 64$ and $W = 12$. Furthermore, we observe that the LDPC-BCs always perform worse than the SC-LDPC codes except when either $M_{SC}$ and/or $W$ are too small.

Note that increasing the window size $W$ improves decoder performance and increasing the protograph lifting factor $M_{SC}$ improves code performance. For example, from Fig. 8 we see that when the decoding latency is 2304 bits, the decoding performance of the 8-ary SC-LDPC code with $M_{SC} = 64$ and decoded with $W = 6$ is better than that of the SC-LDPC code with $M_{SC} = 128$ and decoded with $W = 3$, the reverse of the situation for the same codes when the latency is 4608 bits (obtained for window sizes $W = 12$ and $W = 6$, respectively). In this case, for a latency of 2304 bits, the performance loss caused by the small window size ($W = 3$) is
Fig. 9. Required $E_b/N_0$ to achieve a BER of $10^{-5}$ for $(3,6)$-regular 8-ary SC-LDPC codes with different window sizes $W$ and decoding latencies of 2304, 4608, and 5760 bits.

not compensated for by the larger lifting factor ($M_{SC} = 128$), whereas, if we double the window sizes (increasing the latency to 4608 bits), the code with the larger lifting factor ($M_{SC} = 128$) has a large enough window size ($W = 6$) to outperform the smaller lifting factor ($M_{SC} = 64$) code with $W = 12$. This raises the interesting question of how to choose $M_{SC}$ and $W$ in order to achieve the best performance when the decoding latency of the sliding window decoder is fixed.

Fig. 9 shows the $E_b/N_0$ required for $(3,6)$-regular 8-ary SC-LDPC codes to achieve a BER of $10^{-5}$ with different window sizes $W$ and decoding latencies of 2304, 4608, and 5760 bits. We observe that the required $E_b/N_0$ decreases dramatically until around $W = 4$ to $W = 6$, and then it increases gradually as the window size $W$ increases. This increase results from the fact that the improved decoder performance obtained by increasing $W$ is not compensating for the decrease in code performance as a result of the smaller lifting factor. We therefore conclude that, for $(3,6)$-regular 8-ary SC-LDPC codes, $W = 6$ is a good choice for optimum performance. Similar behavior has also been observed for other field sizes, as shown in Fig. 10.

Table II shows the minimum $E_b/N_0$ required to achieve a BER of $10^{-5}$ for some $(3,6)$-regular $q$-ary LDPC-BCs and $(3,6)$-regular $q$-ary SC-LDPC codes with different field sizes and decoding
Fig. 10. Required $E_b/N_0$ to achieve a BER of $10^{-5}$ for $(3, 6)$-regular $q$-ary SC-LDPC codes with different window sizes $W$ when the decoding latency is 4608 bits.

### Table II

| Required $E_b/N_0$ (dB) | LDPC-BC | SC-LDPC ($W = 6$) |
|-------------------------|---------|-------------------|
|                         | GF(2)   | GF(4)   | GF(8)  | GF(16) | GF(2)   | GF(4)   | GF(8)  | GF(16) |
| Latency of 2304 bits    | 2.1     | 2.0     | 2.0    | 2.2    | 2.3     | 1.9     | 1.7    | 1.7    |
| Latency of 4608 bits    | 1.8     | 1.7     | 1.8    | 1.9    | 1.6     | 1.5     | 1.4    | 1.4    |
| Latency of 6912 bits    | 1.7     | 1.6     | 1.7    | 1.8    | 1.5     | 1.3     | 1.2    | 1.2    |
| Latency of 9216 bits    | 1.6     | 1.5     | 1.6    | 1.7    | 1.3     | 1.2     | 1.1    | 1.1    |
| Latency of 13824 bits   | 1.5     | 1.4     | 1.5    | 1.6    | 1.2     | 1.1     | 1.0    | 1.0    |

It is observed that the non-binary SC-LDPC codes outperform both the binary and non-binary LDPC-BCs and the binary SC-LDPC codes for fixed decoding latency. In general, in contrast to $q$-ary LDPC-BCs, the required $E_b/N_0$ for $q$-ary SC-LDPC codes to achieve a BER of $10^{-5}$ decreases as we increase the field size $q$. This is consistent with results obtained for the iterative decoding thresholds in [22], where it is shown that, for increasing $q$, the thresholds of $(3, 6)$-regular $q$-ary SC-LDPC codes approach capacity,
but those of \((3, 6)\)-regular \(q\)-ary LDPC-BCs diverge from capacity. Finally, note that, for a latency of 2304 bits, the minimum \(E_b/N_0\) required to achieve a BER of \(10^{-5}\) for \((3, 6)\)-regular binary SC-LDPC codes is higher than for \((3, 6)\)-regular binary LDPC-BCs, which is due to the error floor effect of binary SC-LDPC codes with short constraint lengths. This effect is not observed at higher BERs or larger latencies, as can be seen for latencies of 4608, 6912, 9216, and 13824 bits, where binary SC-LDPC codes outperform binary LDPC-BCs.

B. High-Rate LDPC Codes over \(GF(q)\)

For rate \(R = 2/3\) \((3, 9)\)-regular \(q\)-ary SC-LDPC codes, the decoding latency of the sliding window decoder is given by

\[
T_{SC} = 3W M_{SC} m,
\]

whereas \(R = 2/3\) \((3, 9)\)-regular \(q\)-ary LDPC-BCs have decoding latency

\[
T_{BC} = 6M_{BC} m.
\]

For \(R = 3/4\) \((3, 12)\)-regular \(q\)-ary SC-LDPC codes, the decoding latency of the sliding window decoder is given by

\[
T_{SC} = 4W M_{SC} m,
\]

whereas \(R = 3/4\) \((3, 12)\)-regular \(q\)-ary LDPC-BCs have decoding latency

\[
T_{BC} = 8M_{BC} m.
\]

The \(E_b/N_0\) required to achieve a BER of \(10^{-5}\) for equal latency \((3, 9)\)-regular and \((3, 12)\)-regular 8-ary LDPC-BCs and SC-LDPC codes as a function of decoding latency is shown in Fig. 11. Similar to the \((3, 6)\)-regular 8-ary case, we observe that the performance of both \((3, 9)\)- and \((3, 12)\)-regular SC-LDPC codes (with fixed protograph lifting factor \(M_{SC}\)) improves as the window size \(W\) increases, but it does not improve much beyond a certain window size (roughly \(W = 8\)). Moreover, under an equal latency constraint, both \((3, 9)\)- and \((3, 12)\)-regular LDPC-BCs always perform worse than the corresponding \((3, 9)\)- and \((3, 12)\)-regular SC-LDPC codes except when either \(M_{SC}\) and/or \(W\) are too small.

Fig. 12 shows the \(E_b/N_0\) required for the \((3, 9)\)-regular and \((3, 12)\)-regular 8-ary SC-LDPC codes to achieve a BER of \(10^{-5}\) with different window sizes \(W\) and different decoding latencies.
Fig. 11. Required $E_b/N_0$ to achieve a BER of $10^{-5}$ for high-rate 8-ary LDPC-BCs and 8-ary SC-LDPC codes as a function of decoding latency.
Fig. 12. Required $E_b/N_0$ to achieve a BER of $10^{-5}$ for high-rate 8-ary SC-LDPC codes with different window sizes $W$ and different decoding latencies.
TABLE III
MINIMUM $E_b/N_0$ REQUIRED TO ACHIEVE A BER OF $10^{-5}$ FOR (3, 9)-REGULAR AND (3, 12)-REGULAR $q$-ARY LDPC-BCs AND SC-LDPC CODES WITH DIFFERENT FIELD SIZES

| Required $E_b/N_0$ (dB) | LDPC-BC | SC-LDPC ($W = 4$) |
|-------------------------|---------|-------------------|
|                         | GF(2)   | GF(4) | GF(8) | GF(16) | GF(2) | GF(4) | GF(8) | GF(16) |
| (3, 9) codes with latency of 4320 bits | 2.4 | 2.3 | 2.3 | 2.4 | 2.5 | 2.2 | 2.0 | 2.0 |
| (3, 9) codes with latency of 8640 bits | 2.2 | 2.1 | 2.1 | 2.2 | 2.2 | 1.9 | 1.8 | 1.8 |
| (3, 12) codes with latency of 4608 bits | 2.8 | 2.7 | 2.7 | 2.8 | 3.0 | 2.7 | 2.6 | 2.5 |
| (3, 12) codes with latency of 9216 bits | 2.7 | 2.6 | 2.6 | 2.7 | 2.7 | 2.4 | 2.3 | 2.3 |

We observe that the required $E_b/N_0$ for both (3, 9)-regular and (3, 12)-regular 8-ary SC-LDPC codes decreases dramatically until $W = 4$, and then it increases gradually as $W$ increases. We therefore conclude that, for (3, 9)-regular and (3, 12)-regular 8-ary SC-LDPC codes, $W = 4$ is a good choice for optimum performance.

Table III shows the minimum $E_b/N_0$ required to achieve a BER of $10^{-5}$ for some (3, 9)-regular and (3, 12)-regular $q$-ary LDPC-BCs and SC-LDPC codes with different field sizes. Similar to the (3, 6)-regular case, it is observed that both (3, 9)-regular and (3, 12)-regular non-binary SC-LDPC codes outperform both binary and non-binary LDPC-BCs and binary SC-LDPC codes for fixed decoding latency, and in general, in contrast to $q$-ary LDPC-BCs, the required $E_b/N_0$ for $q$-ary SC-LDPC codes to achieve a BER of $10^{-5}$ decreases as we increase the field size $q$. This is again consistent with results obtained for the iterative decoding thresholds in [22], where it is shown that, for increasing $q$, the thresholds of both (3, 9)-regular and (3, 12)-regular $q$-ary SC-LDPC codes approach capacity, but those of both (3, 9)-regular and (3, 12)-regular $q$-ary LDPC-BCs diverge from capacity. Finally, note that the minimum $E_b/N_0$ required to achieve a BER of $10^{-5}$ for both (3, 9)-regular and (3, 12)-regular binary SC-LDPC codes is not less than for binary LDPC-BCs for the (relatively low) latencies considered, which is again due to the error floor effect of binary SC-LDPC codes with short constraint lengths.

VI. A COMPUTATIONAL COMPLEXITY COMPARISON

In [27], the authors investigated the cost of the convolutional gain of binary SC-LDPC codes compared to binary LDPC-BCs in terms of several aspects (computational complexity, processor complexity, decoder memory requirements, and decoding latency) of the pipeline
decoder architecture. In this section, we will compare the computational complexity of \( q \)-ary SC-LDPC codes to \( q \)-ary LDPC-BCs under certain assumptions, i.e., equal decoding latency or equal decoding performance.

As stated in [4], for \( q \)-ary LDPC codes implemented with the FFT-QSPA, the computational complexity per iteration at a check node is \( O(qm) \), while that at a variable node is \( O(q) \). Let \( I_{BC} \) denote the average number of iterations performed to decode the entire block for LDPC-BCs, and let \( I_{SC} \) denote the average number of iterations performed to decode the target symbols in a window for SC-LDPC codes at a particular time instant. For a \((d_v, d_c)\)-regular LDPC-BC with design rate \( R = \frac{d_c - d_v}{d_c} \), the computational complexity per block is then given by

\[
O \left( \frac{T_{BC}}{m} d_v q + \frac{T_{BC}}{m} (1 - R) d_c qm \right) I_{BC} = O \left( \left( \frac{d_v}{m} + d_v \right) q T_{BC} \right) I_{BC}. \tag{18}
\]

Thus, the computational complexity per decoded bit for a \((d_v, d_c)\)-regular LDPC-BC is

\[
O \left( \left( \frac{d_v}{m} + d_v \right) q \right) I_{BC}. \tag{19}
\]

For a \((d_v, d_c)\)-regular SC-LDPC code, for simplicity we consider the section of the graph covered by the window to be \((d_v, d_c)\)-regular, even though the check nodes at the beginning of the window and the variable nodes at the end of the window have lower degrees. Thus the computational complexity per window is (approximately) given by

\[
O \left( \left( \frac{d_v}{m} + d_v \right) q T_{SC} \right) I_{SC}. \tag{20}
\]

Note that the number of decoded (target) bits for the window decoder at each time instant is \( T_{SC}/W \), and thus the computational complexity per decoded bit for a \((d_v, d_c)\)-regular SC-LDPC code is

\[
O \left( \left( \frac{d_v}{m} + d_v \right) q T_{SC} \right) I_{SC} = O \left( \left( \frac{d_v}{m} + d_v \right) q \right) W I_{SC}. \tag{21}
\]

By comparing (19) and (21), we see that if \( I_{BC} = W I_{SC} \), \((d_v, d_c)\)-regular LDPC-BCs and \((d_v, d_c)\)-regular SC-LDPC codes with the same field size \( q \) will have the same computational complexity.

In the remainder of this section we restrict our attention to \((3, 6)\)-regular LDPC codes; however, similar behavior has also been observed for other \((d_v, d_c)\)-regular LDPC codes. For the SC-LDPC codes, the window size is set to \( W = 6 \).
TABLE IV
AVERAGE NUMBER OF ITERATIONS $I_{BC}$ AND $I_{SC}$ OF (3, 6)-REGULAR $q$-ARY LDPC-BCS AND (3, 6)-REGULAR $q$-ARY
SC-LDPC CODES WITH DIFFERENT FIELD SIZES AND DECODING LATENCIES OF 4608, 6912, AND 13824 BITS

| Average number of iterations | $I_{BC}$ | $I_{SC}$ ($W = 6$) |
|-----------------------------|----------|-------------------|
|                             | GF(2)    | GF(4)  | GF(8) | GF(16) | GF(2) | GF(4) | GF(8) | GF(16) |
| Latency of 4608 bits        | 13.8     | 12.3   | 11.1  | 10.1   | 3.3   | 3.2   | 3.0   | 2.8   |
| Latency of 6912 bits        | 15.6     | 14.1   | 12.6  | 11.4   | 3.9   | 3.7   | 3.4   | 3.1   |
| Latency of 13824 bits       | 19.0     | 16.9   | 15.5  | 13.1   | 5.3   | 4.8   | 4.4   | 4.1   |

Fig. 13. Computational complexity per decoded bit of (3, 6)-regular $q$-ary SC-LDPC codes and (3, 6)-regular $q$-ary LDPC-BCs as a function of field size $q$ with decoding latencies of 4608, 6912, and 13824 bits. The window size of the sliding window decoder for the SC-LDPC codes is $W = 6$. Solid curves represent LDPC-BCs, while dotted curves represent SC-LDPC codes.

A. Equal Decoding Latency

In this subsection, we compare the computational complexity of $q$-ary SC-LDPC codes and $q$-ary LDPC-BCs under an equal decoding latency assumption. Table IV shows the average number of iterations $I_{BC}$ and $I_{SC}$ of (3, 6)-regular $q$-ary LDPC-BCs and (3, 6)-regular $q$-ary SC-LDPC codes with decoding latencies of 4608, 6912, and 13824 bits. We observe that $I_{BC}$ for LDPC-BCs is significantly higher than $I_{SC}$ for SC-LDPC codes with the same field size $q$. This results from the fact that, for a given latency, one must decode $W$ times as many target
symbols for an LDPC-BC as for an SC-LDPC code. We also note that the required number of iterations for both LDPC-BCs and SC-LDPC codes decreases with $q$; however, the overall complexity increases (see Fig. 13) because the complexity per iteration is higher.

The resulting computational complexity per decoded bit of $(3, 6)$-regular $q$-ary SC-LDPC codes and $(3, 6)$-regular $q$-ary LDPC-BCs with decoding latencies of 4608, 6912, and 13824 bits is shown in Fig. 13. We observe that the computational complexity of both SC-LDPC codes and LDPC-BCs increases exponentially with field size $q$, and the complexity of SC-LDPC codes is generally about 35% higher than that of LDPC-BCs with the same field size $q$. From Fig. 13, we also observe that the complexity of binary SC-LDPC codes is about 10% higher than that of 4-ary LDPC-BCs, and that the complexity of 4-ary SC-LDPC codes is about 80% higher than that of binary LDPC-BCs. However, under the equal latency assumption, binary SC-LDPC codes gain about 0.3 dB compared to 4-ary LDPC-BCs, and 4-ary SC-LDPC codes gain about 0.4 dB compared to binary LDPC-BCs (see Table II in Section V-A). So, even though complexity is higher for the SC-LDPC codes, the performance improvement is significant and, moreover, it is not possible to achieve this improved performance by increasing the complexity of the LDPC-BCs, i.e., allowing further iterations for LDPC-BCs will not decrease the gap in performance. We therefore conclude that, for a given latency, SC-LDPC codes provide attractive and flexible trade-offs between BER performance and computational complexity that are not available with LDPC-BCs.

B. Equal Decoding Performance

In this subsection, we compare the computational complexity of $q$-ary SC-LDPC codes and $q$-ary LDPC-BCs under an equal decoding performance assumption. The computational complexity per decoded bit of $(3, 6)$-regular $q$-ary SC-LDPC codes and $(3, 6)$-regular $q$-ary LDPC-BCs requiring $E_b/N_0 = 1.5$ dB to achieve a BER of $10^{-5}$ is shown in Fig. 14. In general, we note that under an equal performance assumption, the SC-LDPC codes have approximately equal

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7The computational complexity results for SC-LDPC codes shown in Figs. 13 and 14 are calculated exactly for each case, such that the slight node irregularity at the beginning and end of the window is incorporated. The resulting complexity is thus slightly lower than would be estimated using (21), where the graph is assumed to be regular within a window.

8The $(3, 6)$-regular 16-ary LDPC-BC does not appear in the figure due to its large decoding latency and high computational complexity.
computational complexity as the LDPC-BCs for the same field size $q$, but a significantly reduced latency. For the SC-LDPC codes, the decoding latency decreases as the field size $q$ increases until $q = 8$, and then it begins to increase as $q$ increases further, while the computational complexity increases gradually with increasing $q$ until $q = 8$, and then it increases dramatically as $q$ increases further. This implies that, under these conditions, it is not worth using an SC-LDPC code with field size $q > 8$. We observe the same trend for the LDPC-BCs, but with much larger latencies, and we note that the latency begins to increase for smaller values of $q$ than for the SC-LDPC codes. To be more specific, the decoding latency for the LDPC-BCs (which is higher than for the SC-LDPC codes) decreases as the field size $q$ increases from $q = 2$ to $q = 4$, and then it increases as $q$ increases further, while the decoding complexity increases in line with the SC-LDPC codes. This implies that, under these conditions, it is not worth using an LDPC-BC with field size $q > 4$.

From Fig. 14, we also observe that the computational complexity of the binary SC-LDPC code is about 15% less than that of the 4-ary LDPC-BC, with about 55% less latency. Finally, we observe that the computational complexity of the 4-ary SC-LDPC code is about 25% higher than that of the binary SC-LDPC code, but with about 35% less latency, and the complexity
of the 4-ary SC-LDPC code is about 35% higher than that of the binary LDPC-BC, but with about 70% less latency. We therefore conclude that, for the same performance, 4-ary SC-LDPC codes provide attractive and flexible trade-offs between latency and computational complexity compared to using binary LDPC codes.

C. Discussion

- If we fix decoding latency, we gain in decoding performance by using $q$-ary SC-LDPC codes, but at the cost of slightly higher computational complexity. For example, when the decoding latency is fixed, non-binary SC-LDPC codes with small field size $q$ outperform both binary and non-binary LDPC-BCs and binary SC-LDPC codes, while their computational complexity is slightly higher.
- If we fix decoding performance, we can reduce decoding latency by using $q$-ary SC-LDPC codes, but this comes at the cost of slightly higher computational complexity. For example, when the decoding performance is fixed, non-binary SC-LDPC codes with small field size $q$ have lower decoding latency than both binary and non-binary LDPC-BCs and binary SC-LDPC codes, while their computational complexity is slightly higher.
- Overall, these results imply that $(3, 6)$-regular 4-ary SC-LDPC codes possess a particularly attractive combination of small decoding latency, low computational complexity, and good decoding performance.

VII. Conclusions

In this paper, we considered a finite-length performance comparison of protograph-based $q$-ary SC-LDPC codes and $q$-ary LDPC-BCs. We proposed a sliding window decoding algorithm with a stopping rule based on a soft BER estimate for $q$-ary SC-LDPC codes. Simulation results confirm that $(2, 4)$-, $(3, 6)$-, $(3, 9)$-, and $(3, 12)$-regular $q$-ary SC-LDPC codes achieve substantial convolutional gains compared to the underlying LDPC-BCs, where the constraint length of the SC-LDPC codes is equal to the block length of the LDPC-BCs.

We also examined the relationship between the protograph lifting factor, the decoding window size, and the BER performance of $q$-ary SC-LDPC codes for fixed decoding latency in comparison to $q$-ary LDPC-BCs. It was observed that, under an equal latency constraint, $(3, 6)$-regular non-binary SC-LDPC codes outperform both binary and non-binary LDPC-BCs and binary SC-LDPC
codes. Moreover, for fixed field size and latency, the decoding performance of \((3, 6)\)-regular \(q\)-ary SC-LDPC codes improves as the window size \(W\) increases up to a certain point (around \(W = 6\)), and then it degrades slightly as \(W\) increases further. Similar behavior was also observed for \((3, 9)\)-regular and \((3, 12)\)-regular \(q\)-ary SC-LDPC codes in comparison to their \(q\)-ary LDPC-BC counterparts.

Finally, we compared the computational complexity of \(q\)-ary SC-LDPC codes to \(q\)-ary LDPC-BCs under equal decoding latency and equal decoding performance assumptions. It was observed that \((3, 6)\)-regular 4-ary SC-LDPC codes have a particularly attractive combination of small decoding latency, low computational complexity, and good decoding performance. An interesting future research topic to complement the work reported here would be to design the permutations and edge labels used in the construction process, rather than to select them randomly, to further improve the performance of \(q\)-ary SC-LDPC codes for a given decoding latency.

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