Experiments Design on Contrastive Measuring of Assignment between Signal and Variable in FPGA

Huanyin Zhou\textsuperscript{1,2}, Jiewei Hu\textsuperscript{1}, Yanhui Xie\textsuperscript{1,*}, Weiqi Huang\textsuperscript{1}, Zhongping Yang\textsuperscript{1}, Zhanzhan Lu\textsuperscript{1}

\textsuperscript{1}College of Chemical Defense, PLA, Beijing 102205, China
\textsuperscript{2}China Institute of Atomic Energy, Fangshan, Beijing 102423, China
*Corresponding author email: eva_xiexie@126.com

Abstract: Signal and variable are two kinds of important data objects in FPGA. They are widely used in FPGA digital system design. It is pointed out that their assignments are different in many textbooks. A variable can be assigned immediately but a signal cannot. The difference of assignment is hard to understand because signal and variable have some similarities and they are abstract. In this paper, some experiments of gate circuit ring vibrator are designed ingeniously to study the difference of assignment between signal and variable in FPGA. The assignment of the two data objects is contrastively measured, and the measurement principle is analyzed. According to the experiments, the assignment difference is demonstrated clearly.

1. Introduction
Every cell can operate in parallel in FPGA, so the speed of signal processing via FPGA can be very fast. This is useful in instrument design and it is widely used in recent years. In FPGA, signal and variable are two kinds of important data objects. Both of their state values can be changed, and they can be assigned continuously. However, they are different in some aspects. For example, signal is a global value, and it can be valid in any process, but variable is a local one, and it can only be used in a defined process. In some textbooks\cite{1}\cite{2}, it is pointed out that signal assignment needs some delay time, but variable assign does not. This difference is hard to understand because signal and variable have some similarities and they are abstract. To demonstrate this problem clearly, some experiments are designed ingeniously. The assignment of the two kinds of data objects in FPGA is contrastively measured as follows.

2. Experiments of contrastive measuring

2.1. Principle of gate circuit ring vibrator
The response time of a logic cell in FPGA can be measured through a gate circuit ring vibrator\cite{3}. According to this principle, assignment of signal and variable can be measured through a gate circuit ring vibrator too.

As we know, odd number of NOT gates can make a ring vibrator\cite{4}. Fig.1 shows the principle of the vibrator. If the frequency or period of the vibrating signal is measured, the response time of the logic gate can be calculated. For example, if the vibrator circuit is made of three NOT gates, and the period of the vibrating signal is measured $T$, the response time of the NOT gate can be calculated $T/6$. 

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{fig1.png}
\caption{Principle of gate circuit ring vibrator.}
\end{figure}

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{fig2.png}
\caption{Diagram of gate circuit ring vibrator.}
\end{figure}
2.2. Implement ring vibrator using FPGA

To implement the ring vibrator in Fig. 1 using FPGA, three signals sig2, sig1 and sig0 can be defined as std_logic. Their initial values are assigned ‘1’, ‘0’ and ‘1’ respectively. The vibrator can be described in VHDL as process 1.

```
---process 1: NOT gate vibrator---
process(sig2,sig1,sig0)
begin
  if ctrl = '1' then
    sig2 <= not sig1;
    sig1 <= not sig0;
    sig0 <= not sig2;
  end if;
end process;
```

The above process can generate a schematic as Fig. 2.

![Schematic of gate circuit ring vibrator](image)

In process 1, the three statements operate in parallel, so the states of the signals will change as the following sequence.

101 → 001 → 011 → 010 → 110 → 100 → 101.

After six times of response time, the state value of the signals returns to the initial value and finishes one cycle. This method is usually used to measure the response time of an FPGA cell.

In fact, the response time of a signal is just the assignment time of the signal. Each signal needs 6 times of signal assignment operation in one cycle, so the period of this vibrator is equal to 6 times of assignment time. If the period of the vibrating signal is measured, we can calculate the assignment time of the signal. In this program, the signal of “ctrl” is used to control the vibrator’s run or stop.

To measure the assignment time, a counter is design to count the vibrating times of the ring vibrator in a given width of time. At first, a gate control signal “gate” is designed as process 2.

```
--------process 2: gate set----------
process(clk)
begin
  if falling_edge(clk) then
    if clkdv <= 5000 then
      clkdv <= clkdv + 1;
      gate <= '1';
    else
      if clkdv <= 5000000 then
        clkdv <= clkdv + 1;
        gate <= '0';
      else
        clkdv <= x"00000000";
      end if;
    end if;
  end if;
end process;
```

Because the clk frequency is 50MHz, according to process 2, a gate control signal with a width of 100μs is set, and the gate control signal can be generated once per second.

The following process is designed to count the pulses of sig0 in the gate control time of 100μs.

---process 3: count in gate-----
process (gate, sig0)
begin
if (falling_edge(sig0))
   if (gate = '1')
      N_CNT <= N_CNT + 1;
      N <= N_CNT;
   else
      N_CNT <= x"0000";
   end if;
end if;
end process;

When the above processes are operated on a Xilinx FPGA developing board, the average value of \( N \) can be measured “4AC0”. This hexadecimal value can be transformed to a decimal one “19136”. The measurement shows that there are 19136 pulses generated in 100μs, so the period of the vibrating signal is 5.226ns. The response time of the signal can be calculated 0.871ns, and then the assignment time of sig0 is 0.871ns. The experiment shows that signal assignment needs assignment time. This assignment time has a close relationship with the device’s types, technology, fan-in, fan-out, and so on[5].

2.3. Add variable assignment in vibrator

If the vibrator is designed via adding variables, the program is described as process 4.

---process 4: add variables in vibrator-----
process (ctrl)
variable variable1, variable2: std_logic;
begin
if (ctrl = '1')
   sig1 <= not sig0;
   sig2 <= not sig1;
   variable1 := not sig0;
   variable2 := variable1;
   sig0 <= variable2;
end if;
end process;

According to process 4, signals are assigned 6 times and variables are assigned 4 times in one vibrating cycle. Contrasting with process 1, variable assignment is added 4 times in one cycle, so a period of vibrating cycle contains 6 times of signal assignment and 4 times of variable assignment altogether. Under this condition, we measure the period of vibrating signal generated from process 4 again. A same method as the former measurement is used. The average value of \( N \) is “4ABF”. The result is almost the same as the former measurement of the vibrator with no adding variables. The result shows, variable assignment is added 4 times in one cycle, but the period of vibrating signal nearly dose not change. According to the above contrastive measurements, we can conclude that variable assignment needs no assignment time.

If the signals and variables are all described as NOT logic operations, the process will be changed to the process 5. This process contains of three signal NOT operations and 2 variable NOT operations.

---process 5: add not variables in vibrator-----
process (ctrl)
variable variable1, variable2: std_logic;
begin
if (ctrl = '1')
   sig1 <= not sig0;
   sig2 <= not sig1;
   variable1 := not sig0;
   variable2 := not variable1;
   sig0 <= not variable2;
end if;
end process;
According to same method measurement, the period of the vibrating signal almost has no change. Even if variable assignment is added more times in one cycle in the vibrator, the period has no change either. The experiment demonstrates that variable assignment needs no time further.

2.4. Add signal assignment in vibrator
If signal assignment is added twice in process 1, the process will change to process 6. Process 6 has two more NOT operations than process 1.

```vhdl
begin
if ctrl = '1' then
    sig1 <= not sig0;
    sig2 <= not sig1;
    sig3 <= not sig2;
    sig4 <= not sig3;
    sig5 <= not sig4;
end if;
```

Under this condition, the period of vibrating signal will increase, and it is approximately proportional to the amount of NOT gates. The increasing of the period is mainly caused of the increasing of the signal assignment times, so we can see that signal needs assignment time again.

3. Conclusion
As can be known from the above experiments, signal assignment time can be measured based on the principle of gate circuit vibrator. If variables are added or increased in the vibrator, the period of vibrating signal will not change nearly. But signals are added in the vibrator, the period of vibrating signal will increase and it is in proportion to the amount of the signals. The contrastive measurements demonstrate clearly that signal assignment needs assignment time, but variable assignment does not need. According to the above experiments, the assignment of the two kinds of data objects in FPGA is contrastively demonstrated clearly.

References
[1] Lei Furong. VHDL and Circuits Design[M]. Tsinghua University Press, 2006:43-47
[2] Zhao Junchao. VHDL Course for IC Design[M]. Beijing Hope Electronic Press, 2002:19-22
[3] Zhou Huanyin, Xu Mei. An Experiment Design for Measuring Response Time of FPGA Logic Cell[J]. JIMEC2018, Atlantis Highlights in Engineering, volume 3, 2018,12:129-132
[4] Yan Shi. Fundamentals of Digital Electronic Technology[M]. Higher Education Press, 2006: 483-484
[5] Victor P. Nelson, H. Troy Nagle, Bill D. Carroll, J. David Irwin. Digital Logic Circuit Analysis & Design[M]. Prentice-Hall International, Inc 1999