ReveR: Software Simulator of Reversible Processor with Stack

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Abstract

A software model of a reversible processor ReveR with the stack is discussed in this paper. An architecture, the minimal set of elementary reversible operations together with an implementation of the basic control flow structures and procedures calls using simple assembler language are described.

1 Introduction

An origin of this work was the research of models of programmable quantum processors [1], but this presentation does not require any knowledge about quantum algorithms. A program simulator of reversible processor ReveR is discussed. It may be useful for the research of the reversible computation even without an application to the quantum information science. Irreversible instructions may be implemented using the idea of history tape [2].

The simulator uses minimal set of operations briefly represented below without a discussion and comparison with many well known modern models of reversible processors [2] [4] [5]. The main purposes of the current version is the consideration of the control flow in a reversible processor, e.g. unconditional and conditional jumps, loops and calls of procedures using the stack for a return address. The reversible implementation of procedure calls and basic control flow structures with minimal set of basic instructions is demonstrated.

2 Architecture

2.1 Registers and Basic Processing Principles

The current model of the processor ReveR has eight 32-bit registers: CM — the current instruction (command), IP — the instruction pointer, DIP — the increment (delta) of the instruction pointer, SP — the stack pointer, MP — the memory pointer, RA, RB, RC — registers A,B,C.

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A standard step formally uses two phases, an external and an internal. Between the steps the register CM has zero value and IP points to the address of a current instruction. The external phase is fixed and changes only the registers CM and IP and the internal phase may change all, except these two registers.

\[
CM := CM + MEM[IP]; \\
\text{Internal}(CM); \\
CM := CM - MEM[IP]; \ IP := IP + DIP
\]

The internal phase is also quite simple. It is used an idea to choose a minimal set of elementary reversible operations and to represent an instruction as the sequence of such operations without any internal branching and changes of the CM, IP registers. It guarantees the reversibility of any instruction and a relative simplicity of a program flow.

The processor ReveR uses an array of “nanoprograms”\(^1\), i.e. sequences of indexes of the reversible instructions.

\[
\text{with Nanoprogram}[CM] \text{ do } \ \\
\text{for } nIP := 0 \text{ to } \text{Length}(RevCodes) - 1 \text{ do } \ \\
\text{RevOps}[RevCodes[nIP]].\text{Perform}
\]

Here is used an internal processor counter denoted as nIP. RevCodes is an array of codes for given instruction, Nanoprogram[CM] and RevOps points to a reversible operation for given code (see the table\(^1\) below with examples of the codes, n and associated operations). For any instruction is known an inverse one and so such step is reversible. The inversion of a nanoprogram should perform inverse operations in opposite order

\[
{\ldots} \text{ for } nIP := \text{Length}(RevCodes) - 1 \text{ downto } 0 \text{ do } \{\ldots\}
\]

### 2.2 Elementary Internal Operations

For the simplest implementation it is enough to use sixteen elementary instructions shown in the table\(^1\). A short notation \([MP]=MEM[MP]\) for contents of memory with address MP and \([IP+1]=MEM[IP+1]\) for a number NX immediately after current instruction is used in the table. It is also used notation \(A \leftrightarrow B\) for the exchange and \(\leftarrow\) for the left assignment in the reversible operations like \(A \leftarrow B - A\). Yet another shortcut is the step-like function \(G_C\) equal to unit for any positive \(C\) and zero otherwise. So the operation CNSUB may be written as \(A = (C > 0) ? B - A : -A\) in a C-like language.

The operations with codes 0 – 13 are self-inverse (involutions). The exceptions from such a rule are CLRA and UCLA necessary only for the simulation of irreversible operations with a “history tape” and mentioned for completeness. CLRA “pushes” value of RA to a “trash” and supplies RA with “new” zero. The inverse operation UCLA should be never used directly and may appears only during the reverse running of the processor. In such a case an application of UCLA to nonzero RA may appears only due to some error and results an exception in the ReveR.

\(^1\)Such an informal term is used here instead of more common “microprogram,” due to actuality of the quantum and reversible computations in nanoscale.
2.3 Memory Access

The direct access of the ReveR to a memory is ensured due to the instruction SWP MEM via an exchange of RA and the memory with an address stored in MP. In the current model data, addressed by MP, instructions, addressed by IP and the stack share the same physical memory. After initialization of the registers, of the ReveR SP points to the last address of the memory and all other registers are zero. An access to the stack is discussed further and uses simple nanoprograms with the temporary exchange MP and SP.

Yet another method to obtain some number is provided by the access to the address immediately after IP (\(Nx = [IP+1]\)) using operations such as NX SUB and CNX SUB. An operation for a direct exchange of some register with \([IP+1]\) is not provided because formally it could change program itself, but it would not be in agreement with some principles of suggested architecture. The operation NSUB IP also could provide a similar functionality in a less direct way and may be considered as redundant.

3 Instructions and Control Flow

3.1 Basic Instructions (“Nanoprograms”)

In the table 2 are provided the description of nanoprograms for the basic set of instructions used in the current version of the processor ReveR4104. Simplest instructions such as Nop, Swap RA, ... are equivalent to single internal operations, other nanoprograms may call from 2 to 14 elementary operations. The codes of the operations are provided in the table 3.

Any program should start with Inc DIP, because the ReveR is initialized with zero DIP register and without such instruction IP would not increase after each step. Before instructions such as Add RA, [IP+1] (with am immediate number in the next address) DIP should be increased again to make double steps.

The instruction Jmp dNx uses an immediate number to increase DIP and make the unconditional jump. A destination address of such a jump also should contain Jmp dNx with a negative increment to restore an initial value of DIP.

An example is provided below. Here semicolons are used for comments, colons for
Table 2: Descriptions of basic instructions for ReveR4104.

| CM | Name       | Description                  | CM | Name       | Description                  |
|----|------------|------------------------------|----|------------|------------------------------|
| 0  | Nop        | NOP                          | 17 | Neg RA     | A ← − A                     |
| 1  | Inc DIP    | DIP ← DIP + 1               | 18 | Jmp dNx    | DIP ← DIP + [IP + 1]         |
| 2  | Dec DIP    | DIP ← DIP − 1               | 19 | Subr       | DIP ← [SP]; DIP ← DIP + 1;   |
|    |            |                              |    |            | SP ← SP − 1                  |
| 3  | Inc RA     | A ← A + 1                   | 20 | Ret        | SP ← SP + 1; DIP ← DIP − 1;  |
|    |            |                              |    |            | DIP ← [SP]; DIP ← [IP + 1]−DIP |
| 4  | Dec RA     | A ← A − 1                   | 5–10| Swap RA,...| A ↔ ...                      |
|    |            |                              | 11 | Add RA, RB | A ← A + B                   |
| 12 | Sub RA, RB | A ← A − B                   | 13 | Add RA,[IP+1] | A←A+[IP+1]                  |
|    |            |                              | 14 | Sub RA,[IP+1] | A←A−[IP+1]                  |
| 15 | Add RA,IP  | A ← A + IP                  | 16 | Sub RA,IP  | A ← A − IP                  |
|    |            |                              | 17 | Neg RA     | A ← − A                     |
| 18 | Jmp dNx    | DIP ← DIP + [IP + 1]         | 19 | Subr       | DIP ← [SP]; DIP ← DIP + 1;   |
|    |            |                              |    |            | SP ← SP − 1                  |
| 20 | Ret        | SP ← SP + 1; DIP ← DIP − 1;  |    |            | DIP ← [SP]; DIP ← [IP + 1]−DIP |
| 21 | CJmp dNx   | if C > 0, DIP ← DIP + [IP + 1] |
| 22 | CAdd RA, RB| if C > 0, A ← A + B         |
| 23 | Push RA    | A ← [SP]; SP ← SP − 1       |
| 24 | Pop RA     | SP ← SP + 1; [SP] ← A       |
| 25 | Clear RA   | 0 ↔ A ↔ History             |

labels (like @1, @2) and the # prefix for immediate values, e.g. #@2−@1−1 is equal to the difference between addresses marked by labels @2 and @1 decreased by unit.

Inc DIP ; To start program, DIP = 1
: @1 ; Label before jump instruction
Jmp dNx ; Jump instruction (set DIP = @2−@1)
#@2−@1−1 ; Immediate value, increment of DIP
Nop ; To skip next instructions
Nop ; Label to jump here
Jmp dNx ; "Fake" jump instruction, set DIP = 2
#@1−@2+2 ; Immediate negative value, decrement of DIP
Dec DIP ; To set DIP = 1

The application of the conditional jump CJmp dNx is similar and may be used for “if RC > 0 then ...” structures.

Inc DIP ; To start program, DIP = 1
Inc RA ; RA = 1
Swap RA,RC ; RC = 1
Inc DIP ; Set DIP = 2 to omit immediate value after jump
Nop ; The gap is necessary due to DIP = 2
: @1 ; Label before jump instruction
CJmp dNx ; Conditional jump (if RC > 0 then DIP = @2−@1)
#@2−@1−2 ; Immediate value, increment of DIP
Nop ; Skipped, because RC > 0
Nop ; Label to jump here
Jmp dNx ; "Fake" jump instruction, set DIP = 2
Different control structures with loops also may be implemented with CJmp dNx commands. An example below shows a loop like: For RC := 0 to 9 do Inc RB.

| Inc DIP | Swap RA, RB | CJmp dNx | :@2 |
|---------|------------|----------|------|
| ; to start loop | ; If RC + 1 > 9 | #@4-@3-2 | CJmp dNx |
| Inc DIP | Swap RA, RC | Swap RA, RC | #@1-@2-2 |
| Nop | Inc RA | Nop | :@4 |
| :@1 | Inc DIP | Add RA, [IP+1] | CJmp dNx |
| CJmp dNx | Nop | #9 ; count | #@3-@4+2 |
| #@2-@1+2 | Sub RA, [IP+1] | Dec DIP | Dec DIP |
| Dec DIP | #9 ; count | Swap RA, RC | ; end of loop |
| ; Inc RB | Swap RA, RC | ; continue | Swap RA, RC |
| Swap RA, RB | Nop | Inc DIP | Dec RA |
| Inc RA | :@3 ; exit loop | Nop | Swap RA, RC |

The more difficult case is a procedure call, because it requires the tracing of the return address if the same procedure may be called from different locations. The stack should be used for the return positions to allow nesting of the calls.

### 3.2 Procedures and Reversible Stack

Instruction Push RA and Pop RA represented in table 2 look simple, yet each uses nine reversible internal codes due to necessity of auxiliary swaps of MP, SP, and RA. The instruction Push RA exchanges RA with content of memory with address stored in SP and decreases SP on unit to point on previous address. The Pop RA is inverse of Push RA.

It is suggested for proper work, that SP always points to address with zero value to ensure RA = 0 after Push RA. So, it is necessary to keep zero value of RA before Pop RA.

So, if contents of RA is not known, it should be used CLRA command and it is not purely reversible computations. It may be shown, that procedure calls with stack may be performed without CLRA.

Simple program below demonstrates principle of such reversible calls.

| ; To start program | Dec DIP ; DIP = 1 | ; ... etc. |
|-------------------|-------------------|----------|
| Inc DIP | :@2 ; Second call | :@3 ; Procedure label |
| :@1 ; First call | Jmp dNx ; -> to @3 | Subr ; To push DIP |
| Jmp dNx ; -> to @3 | #@3-@2-1 | ; ... do something |
| #@3-@1-1 | Jmp dNx ; <- from @4 | #@4-@2 |
| Jmp dNx ; <- from @4 | #@4-@1 | Ret ; Return |
| #@4-@1 | Dec DIP ; DIP = 1 | #@3-@4+2 |

Already mentioned Jmp dNx is used here, but the Subr instruction at very beginning of the procedure stores DIP in the stack. The instruction Ret at end of the procedure restores value of DIP from the stack and uses the immediate value (@2-@3+2) to calculate
the size of the jump to an instruction after the procedure call. This instruction should be \texttt{Jmp dNx} with an appropriate immediate negative value to set \texttt{DIP = 2} (followed by \texttt{Dec DIP} to set \texttt{DIP = 1}, if it is necessary).

4 Conclusion

A software model with rather small set of codes providing necessary control flow instructions in a reversible processor is considered in presented work. Nested procedure calls are implemented using the stack.

References

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| CM | Name                      | Internal codes                          |
|----|---------------------------|----------------------------------------|
| 0  | Nop                       | NOP                                    |
| 1  | Inc DIP                   | SWP DIP; NOT RA; NEG RA; SWP DIP       |
| 2  | Dec DIP                   | SWP DIP; NEG RA; NOT RA; SWP DIP       |
| 3  | Inc RA                    | NOT RA; NEG RA                         |
| 4  | Dec RA                    | NEG RA; NOT RA                         |
| 5  | Swap RA,RB                | SWP RB                                 |
| 6  | Swap RA,RC                | SWP RC                                 |
| 7  | Swap RA,DIP               | SWP DIP                                |
| 8  | Swap RA,SP                | SWP SP                                 |
| 9  | Swap RA,MP                | SWP MP                                 |
| 10 | Swap RA,[MP]              | SWP MEM                                |
| 11 | Add RA,RB                 | NEG RA; NSUB                           |
| 12 | Sub RA,RB                 | NSUB; NEG RA                           |
| 13 | Add RA,[IP+1]             | NEG RA; NX SUB                         |
| 14 | Sub RA,[IP+1]             | NX SUB; NEG RA                         |
| 15 | Add RA,IP                 | NEG RA; NSUB IP                        |
| 16 | Sub RA,IP                 | NSUB IP; NEG RA                        |
| 17 | Neg RA                    | NEG RA                                 |
| 18 | Jmp dNx                   | SWP DIP; NEG RA; NX SUB; SWP DIP       |
| 19 | Subr                      | SWP SP; SWP MP; SWP SP; SWP DIP; NOT RA; NEG RA; SWP DIP; SWP SP; SWP MP; SWPSP; NEG RA; NOT RA; SWP SP |
| 20 | Ret                       | SWP SP; NOT RA; NEG RA; SWP MP; SWP SP; SWP DIP; NEG RA; NOT RA; SWP MEM; SWP SP; SWP MP; SWPSP; NX SUB; SWP DIP |
| 21 | CJmp dNx                  | SWP DIP; NEG RA; CNX SUB; SWP DIP      |
| 22 | CAdd RA,RB                | NEG RA; CNSUB                          |
| 23 | Push RA                   | SWP SP; SWP MP; SWP SP; SWP MEM; SWP SP; SWP SP; SWP MP; NEG RA; NOT RA; SWP SP |
| 24 | Pop RA                    | SWP SP; NOT RA; NEG RA; SWP MP; SWP SP; SWP SP; SWP SP; SWP MEM; SWP SP; SWP MP; SWP SP |
| 25 | Clear RA                  | CLR A                                  |

Table 3: Codes (nanoprograms) for basic instructions of ReveR4104.