Monotone One-Port Circuits

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Abstract—Maximal monotonicity is explored as a generalization of the linear theory of passivity, aiming at an algorithmic input/output analysis of physical models. The theory is developed for maximal monotone one-port circuits, formed by the series and parallel interconnection of basic elements. These circuits generalize passive linear, time-invariant (LTI) transfer functions. Input–output behaviors can be efficiently computed using a maximal monotone splitting algorithm, which decomposes the computation according to the circuit topology. A new splitting algorithm is presented, which applies to any monotone one-port circuit defined as a port interconnection of monotone elements.

Index Terms—Circuit theory, convex optimization, monotone operators, nonlinear systems.

I. INTRODUCTION

PASSIVITY is the backbone of linear circuit theory. As a system theoretic concept, it provides a fundamental bridge between physics and computation, well beyond electrical circuits. The concept of passivity first arose in the study of interconnections of basic circuit elements [1], [2], [3], and passive transfer functions are precisely those that can be realized as port interconnections of passive elements [4]. The KYP lemma provides an algorithmic framework for the analysis of passive circuits by convex optimization [5], [6], [7]. The circuit concept of passivity has generated amongst the most important developments of control theory over the last several decades, including dissipativity theory [8], [9], nonlinear passivity theory [10], [11], [12], and passivity based control [13], [14], [15], [16].

The strong physical and computational properties of linear passive circuits fail to generalize to the nonlinear world. The mere existence and uniqueness of solutions can no longer be taken for granted, let alone an algorithm to compute them. Contrary to physical intuition, a nonlinear passive resistor may have regions of negative resistance [17]. Negative resistance circuits behave quite differently from linear passive circuits, being the source of switches and oscillations [18]. This article explores maximal monotonicity as a generalization of linear passivity that retains both its physical and algorithmic significance in nonlinear circuits. In the spirit of the early work of Foster [1], Cauer [2], Brune [3], Bott and Duffin [4], and the “tearing, zooming, and linking” methodology advocated by Willems [19], we consider a class of systems formed by port interconnections of basic elements, possibly nonlinear. The primary message of this article is that, like passive linear, time-invariant (LTI) transfer functions, this class is both physical and computationally tractable.

This proposal is classical, and indeed the property of maximal monotonicity first arose in efforts to extend the tractability of linear, time invariant, passive networks to networks of nonlinear resistors. The prototype of a maximal monotone element was Duffin’s quasi-linear resistor [20], a nonlinear resistor with a nondecreasing $i$–$v$ characteristic. Other early forms of monotonicity are found in the work of Golomb [21], Zanantonello [22] and the work of Dolph [23] on “dissipative” linear mappings. Quasi-linearity was refined by Minty [24], [25], [26] to produce the modern concept of maximal monotonicity, in the context of an algorithm for solving networks of nonlinear resistors. Desoer and Wu [27] studied existence and uniqueness of solutions to networks of nonlinear resistors, capacitors, and inductors defined by maximal monotone relations.

Following the influential paper of Rockafellar in 1976 [28], maximal monotonicity has grown to become a fundamental property in convex optimization [29], [30], [31], [32], [33], [34], forming the basis of a large body of work on tractable first-order methods for large scale and nonsmooth optimization problems, which have seen a surge of interest in the last decade. The principle notion is that of splitting: for operators, which can be separated into sums of monotone operators, a splitting algorithm can be applied, which separates computation for each element of the sum, allowing computation to be distributed across multiple devices. This is the basis for many popular first-order methods, including alternating direction method of multipliers (ADMM) and proximal gradient. For a comprehensive bibliography, we refer the reader to the literature review of [31, Ch. 2]. It seems, however, that the physical significance of maximal monotonicity has been somewhat forgotten. In this article, we revisit the study of nonlinear circuits in light of modern developments in the theory of splitting algorithms.

Maximal monotonicity also plays a fundamental role in a long line of research on analysis and simulation of state space systems interconnected with nonsmooth and set-valued components, recently surveyed by Brogliato and Tanwani [35]. The first connection between maximal monotone operators and passive linear systems appears in this area, in the work of Brogliato [36].

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This work inspired a line of research on Lur’ë systems consisting of a passive LTI system in feedback with a nonsmooth maximal monotone operator (see, for instance, [35], [37], [38], [39], [40], [41]). Maximal monotone differential inclusions were first studied by Brézis, who, in particular, proved existence of periodic solutions when such differential inclusions are periodically forced by a locally integrable input [42, Ch. 3, Sec. 6]. Existence and uniqueness of solutions to such differential inclusions have since been studied extensively [40], [43]. Solutions can be constructed using the classical time-stepping algorithm surveyed in [35, Sec. 5.2]. A number of other time domain simulation algorithms have been developed for Lur’ë systems with maximal monotone nonlinearities in the feedback [44], [45]. Two algorithms for computing the periodic response of such Lur’ë systems are given by Heemels et al. [46], which both involve iteratively computing the resolvent of a differential inclusion. Lur’ë systems with maximal monotone nonlinearities may also be modeled as linear complementarity systems, and specialized methods for computing steady-state oscillations in such systems have been developed by Ianelli et al. [47] and Meingast et al. [48]. Other methods for computing periodic responses of nonlinear systems are either approximate and limited in their applicability, as in harmonic analysis [49], [50], [51], [52] or involve performing a transient simulation and waiting for convergence [53], [54].

In this article, we also study the periodic response of maximal monotone circuits. However, our approach in grounded in input–output rather than state-space descriptions. We treat circuits as a physical interconnection of basic components, each of which is required to be a maximal monotone operator on the space of T-periodic i–v trajectories. Rather than performing an integration forwards in time, we pose the periodic response of the circuit as a zero of an operator on the space of periodic trajectories, and draw on the splitting algorithms of convex optimization. This method is reminiscent of frequency response analysis of an LTI transfer function. Standard splitting algorithms allow the computation to be organized using the interconnection structure in the case of purely series or purely parallel circuits, an observation first made in the conference version of this article [55]. Here, we further develop this idea and show that the circuit topology of the circuit can be put in direct correspondence with its algorithmic solution. We introduce a splitting algorithm suited to arbitrary series/parallel circuits, which generalizes existing splitting algorithms, which find zeros of sums of maximal monotone operators, to nested sums and inverses of maximal monotone operators.

The rest of this article is organized in three parts. The first part of this article describes, in general terms, the class of systems formed from the series/parallel interconnection of maximal monotone one-port elements—referred to throughout this article as monotone one-port circuits. In Section II, we motivate the study of this class by contrasting it with interconnections of passive elements. While monotone one-port circuits retain the fundamental properties of interconnections of LTI resistors, these properties are lost for passive nonlinear elements. In Section III, we review the basic theory of maximal monotone operators. In Section IV, we revisit port interconnections of maximal monotone elements, and formalize the class of systems studied in this article.

The second part of this article develops an algorithmic framework for studying the periodic response of monotone one-port circuits. In Section V, we first show that off-the-shelf optimization algorithms can be used to compute the periodic response of circuits composed of purely parallel or purely series interconnections. We then introduce a new splitting algorithm (Algorithm 1).

The final part of this article studies particular, physical classes of monotone one-port circuits. Section VI applies the theory to nonlinear RLC circuits, and gives two detailed computational examples, including a large-scale circuit consisting of 300 000 elements. Section VII applies the theory to memristive systems, using the specific example of a neuronal potassium conductance. Finally, Section VIII concludes this article.

II. MOTIVATING EXAMPLE

We begin with a simple example, which motivates the developments of this article: the series interconnection of two resistors (see Fig. 1).

Consider first the linear, time invariant case, \( v_j = R_j \omega_j \), where each \( R_j > 0 \). The series interconnection maps the applied voltage \( v \) to the port current \( i \) by the relation \( i = v/(R_1 + R_2) \). The interconnection has the property that for any T-periodic applied voltage, there exists a unique T-periodic port current. This property seems natural for a circuit of passive elements.

The fundamentals of the circuit remain unchanged if the resistor \( R_1 \) is replaced by a linear, time-invariant, and passive transfer function \( R_1(s) \), which obeys, by the positive real lemma, \( \Re R_1(j\omega) \geq 0 \) for all \( \omega \). The resulting transfer function from current to voltage is given by \( 1/(R_1(s) + R_2) \); given a T-periodic voltage \( v \), the unique corresponding current can be found by taking the Fourier series of \( v \) and multiplying each coefficient \( \hat{v}_n \) by \( 1/[(R_1(jn\omega \pi/T) + R_2) \). Since \( \Re R_1(j\omega) \geq 0 \) and \( R_2 > 0 \), this complex number always has finite magnitude.

If we replace \( R_1 \) by a nonlinear, but passive resistor, however, a T-periodic voltage no longer guarantees a T-periodic current. A passive resistor can have regions of negative slope in its \( i\rightarrow v \) curve ([17] give a catalogue of physical examples). The voltage to current map of such a resistor is then multivalued, and it is not guaranteed that the current corresponding to a T-periodic voltage is uniquely defined, nor T-periodic.

If, however, we replace \( R_1 \) with a monotone nonlinear resistor, the fundamentals of the LTI case remain unchanged. Monotonicity of a resistor means its \( i\rightarrow v \) curve is nondecreasing. The interconnection with \( R_2 > 0 \) means the \( i\rightarrow v \) curve of the circuit

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\[ + v_1 \quad i \quad R_1 \quad v_2 \quad + \]

Fig. 1. Series interconnection of two resistors.

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\footnote{The code for the examples of this article is available at github.com/ThomasChaffey/monotone-one-port-circuits.}
is strictly increasing, so invertibility of the interconnection is retained, as illustrated in Fig. 2. This idea will be formalized for monotone RLC circuits in Theorem 2.

III. MAXIMAL MONOTONE OPERATORS

We begin by introducing some mathematical preliminaries.

A. Operators and Relations

Definition 1: An operator on a space X is a set-valued mapping $S : X \mapsto X$. The relation or graph of an operator $S$ is a subset $\text{gra} S \subseteq X \times X$ of input–output pairs $(u, y)$.

Throughout this article, we will treat an operator and its relation as equivalent, and often merely write $S$ when we are strictly referring to $\text{gra} S$. The operator notation $y \in S(u)$ is equivalent to the relational notation $(u, y) \in \text{gra} S$.

The usual operations on functions can be extended to set-valued operators

$$S^{-1} = \{ (y, u) \mid y \in S(u) \}$$

$$S + R = \{ (x, y + z) \mid (x, y) \in S, (x, z) \in R \}$$

$$SR = \{ (x, z) \mid \exists y \text{ s.t. } (x, y) \in S, (y, z) \in R \}.$$

Note that the relational inverse $S^{-1}$ always exists, but in general, $SS^{-1} \neq I$, where $I$ is the identity relation $\{(x, x) \mid x \in X\}$.

B. Signal Spaces

Throughout this article, we let $\mathcal{H}$ be a Hilbert space with inner product $\langle \cdot, \cdot \rangle$ and induced norm $\|x\| = \sqrt{\langle x, x \rangle}$. The particular Hilbert spaces, we consider are spaces of periodic signals, described by a single period. A trajectory $w(t)$ is said to be $T$-periodic if $w(t) = w(t + T)$ for all $t$.

Let $L_{2,T}$ denote the space of signals $u : [0, T] \to \mathbb{R}^n$, which are square integrable, that is,

$$\int_0^T u^\top(t)u(t) \, dt < \infty.$$

This is a Hilbert space with inner product

$$\langle u, y \rangle := \int_0^T u^\top(t)y(t) \, dt$$

and induced norm $\|u\| := \sqrt{\langle u, u \rangle}$. The discrete-time counterpart of $L_{2,T}$ is denoted by $l_{2,T}$, the space of length $T$ sequences, which are square summable

$$\sum_{t=0}^T u^\top(t)u(t) < \infty.$$

Again, this is a Hilbert space with inner product

$$\langle u, y \rangle := \sum_{t=0}^T u^\top(t)y(t)$$

and induced norm $\|u\| := \sqrt{\langle u, u \rangle}$. $L_{2,0,\infty}$ and $L_{2,-\infty,\infty}$ are defined analogously to $L_{2,T}$, but with time intervals $[0, \infty)$ and $(-\infty, \infty)$, respectively.

C. Maximal Monotonicity

The property of monotonicity connects the physical property of energy dissipation in a device to algorithmic analysis methods. Monotonicity on $\mathcal{H}$ is defined as follows.

Definition 2: An operator $S : \mathcal{H} \mapsto \mathcal{H}$ is called monotone if

$$\langle u_1 - u_2, y_1 - y_2 \rangle \geq 0$$

for any $(u_1, y_1), (u_2, y_2) \in \text{gra} S$. A monotone operator is called maximal if its relation is not properly contained in the relation of any other monotone operator.

By way of example, an operator $S : \mathbb{R} \mapsto \mathbb{R}$ is monotone if its graph is nondecreasing, and maximal if its graph has no endpoints. Note that this definition refers to monotonicity in the operator theoretic sense, and this is distinct from the notion of monotonicity in the sense of partial order preservation by a state-space system (see, for example, [56]).

Monotonicity is preserved under a number of operations. The proof of the following lemma may be found in [31].

Lemma 1: Consider operators $G$ and $F$, which are monotone on $\mathcal{H}$. Then

1) $G^{-1}$ is monotone;
2) $G + F$ is monotone;
3) $\alpha G$ is monotone for $\alpha > 0$.

Maximality is preserved under inversion. However, in general, maximality is not preserved when two relations are added (indeed, their sum may be empty). We make the following assumption on summations throughout the rest of this article, which guarantees maximality of the sum, by [58, Th. 1].

Assumption 1: Any summation of two operators $G$ and $F$ obeys

$$\text{int dom}(F) \cap \text{dom}(G) \neq \emptyset$$

or $\text{int dom}(G) \cap \text{dom}(F) \neq \emptyset$

where dom$(S)$ denotes the domain of the operator $S$, and int denotes the interior of a set.

This assumption is sufficient (but not necessary) for the existence of solutions to the summation (that is, the resulting relation is nonempty). We omit the proof of this fact.

D. Stronger Monotonicity Properties

Definition 3: An operator $S : \mathcal{H} \mapsto \mathcal{H}$ has a Lipschitz constant of $\lambda > 0$, or is $\lambda$-Lipschitz if, for all $(u_1, y_1), (u_2, y_2) \in \text{gra} S$

$$\|y_1 - y_2\| \leq \lambda \|u_1 - u_2\|.$$

If $\lambda < 1$, $S$ is called a contraction. If $\lambda = 1$, $S$ is called nonexpansive.
Note that if $S$ is $\lambda$-Lipschitz, it is also $\lambda$-Lipschitz for all $\lambda > \lambda$.

Definition 4: Given $\mu > 0$, an operator $S : \mathcal{H} \rightarrow \mathcal{H}$ is $\mu$-coercive or $\mu$-strongly monotone if, for all $(u_1, y_1), (u_2, y_2) \in \text{gra } S$
\[
\langle u_1 - u_2, y_1 - y_2 \rangle \geq \mu \| u_1 - u_2 \|^2.
\]

$S$ is called $\mu$-hypomonotone in the case that $\mu < 0$. If the sign of $\mu$ is unknown, we simply say $S$ is $\mu$-monotone.

Definition 5: Given $\gamma > 0$, an operator $S : \mathcal{H} \rightarrow \mathcal{H}$ is $\gamma$-cocoercive if, for all $(u_1, y_1), (u_2, y_2) \in \text{gra } S$
\[
\langle u_1 - u_2, y_1 - y_2 \rangle \geq \gamma \| y_1 - y_2 \|^2.
\]

$S$ is called $\gamma$-cohypomonotone in the case that $\gamma < 0$.

It is seen immediately that $F$ is $\mu$-coercive if and only if $F^{-1}$ is $\mu$-cocoercive. It also follows from the Cauchy–Schwarz inequality that $F$ has a Lipschitz constant of $1/\gamma$ if $F$ is $\gamma$-cocoercive. Finally, if $A$ is $\mu$-coercive (resp. $\gamma$-cocoercive) and $B$ is monotone, $A + B$ is monotone, $A$ and $B$ is $\mu$-coercive (resp. $\gamma$-cocoercive). For more details on these properties, we refer the reader to [57, Sec. 2.2] and [58].

IV. MONOTONE ONE-PORT CIRCUITS

The systems considered in this article are electrical one-port circuits. Analogous to the classical realization of passive LTI transfer functions by series/parallel interconnections of resistors, capacitors, and inductors [4], we consider the class of systems, which can be realized as series/parallel interconnections of basic one-port elements, which are modeled as monotone operators.

One-port circuits have two external terminals. The port voltage $v$ may be measured across these terminals, and the port current $i$ may be measured through them. We assume that each of these variables takes values in $\mathbb{R}$. A one-port circuit $E$ is defined by an operator on $L_{2,T}$ between current and voltage. We denote by $d(E) \in \{ i \rightarrow v, v \rightarrow i \}$ the direction of the operator $E$, either current to voltage (current controlled) or voltage to current (voltage controlled). We will often denote current controlled circuits by $R$, and voltage controlled circuits by $G$. These may in general be arbitrary impedances or admittances, and are not restricted to being memoryless. We say that $E$ is a $\mu$-monotone one-port if it is defined by a $\mu$-monotone operator.

A. Series and Parallel Interconnections

Two one-ports may be combined to build a new one-port by series or parallel interconnection. These are illustrated in Fig. 3.

![Series and Parallel Interconnections](image)

Fig. 3. Series (left) and parallel (right) interconnections of two 1-ports.

When two one-ports are connected in parallel, their operators must be from voltage to current. If they are not, one or both operators must be inverted before interconnection. Let $G_1$ and $G_2$ be two one-port circuits such that $d(G_1) = d(G_2) = v \rightarrow i$. For a parallel interconnection, the composition of Kirchoff’s laws and the operators $G_1$ and $G_2$ creates a natural forward operator from voltage to current, as follows.

1) KVL: $v = v_1 = v_2$.
2) Device: $(v_1, i_1) \in G_1$, $(v_2, i_2) \in G_2$.
3) KCL: $i_1 + i_2 = i$.

We, therefore, have a new operator $G = G_1 + G_2$, $d(G) = v \rightarrow i$. This is illustrated in the left of Fig. 4. Calculating the inverse operator, we have

\[
i \in (G_1 + G_2)(v)
\]

\[
G_1(v) \in i - G_2(v)
\]

\[
v \in G_1^{-1}(i - G_2(v))
\]

which is the negative feedback interconnection of $G_1^{-1}$ and $G_2$, illustrated in the right of Fig. 4.

For a series interconnection, the roles of current and voltage are reversed. Letting $R_1$ and $R_2$ be two one-port circuits such that $d(R_1) = d(R_2) = i \rightarrow v$, their series interconnection gives an operator from current to voltage, as follows.

1) KCL: $i = i_1 = i_2$.
2) Device: $(i_1, v_1) \in R_1$, $(i_2, v_2) \in R_2$.
3) KVL: $v_1 + v_2 = v$.

The new operator is $R = R_1 + R_2$, with $d(R) = i \rightarrow v$. The inverse operator, from $v$ to $i$, is the negative feedback interconnection of $R_1^{-1}$ and $R_2$. This is illustrated in Fig. 5. Properties of a parallel interconnection always hold for a series interconnection when the roles of $i$ and $v$ are exchanged; as such, in several results which follow, we will state results for parallel interconnections only.

A standard result is that monotonicity of circuits is preserved under series and parallel interconnection [59]. Precisely, we have the following.
**Proposition 1:**

1. Let $E_1$ and $E_2$ be monotone one-port circuits such that 
   \[ d(E_1), \, d(E_2) \in \{ i \to v, \, v \to i \}. \]
   Then, the series and parallel interconnections of $E_1$ and $E_2$ are both monotone one-ports.
2. Let $G_1$ and $G_2$ be one-port circuits such that $G_1$ is \( \alpha \)-monotone, $G_2$ is \( \beta \)-monotone, and 
   \[ d(G_1) = d(G_2) = v \to i. \]
   Then, the parallel interconnection of $G_1$ and $G_2$ is \( (\alpha + \beta) \)-monotone.

**Proof:** The proof of Part 1 follows directly from the preservation of monotonicity under inversion and addition (Lemma 1).

Part 2 follows from the fact that if $E$ is \( \alpha \)-monotone and $E_2$ is \( \beta \)-monotone, $E_1 + E_2$ is \( (\alpha + \beta) \)-monotone.

\[ \langle u_1 - u_2, (E_1 + E_2)u_1 - (E_1 + E_2)u_2 \rangle \]
\[ \geq (\alpha + \beta) \|u_1 - u_2\|^2. \]

Repeatedly applying series and parallel interconnections allows a collection of one-port circuits to be assembled into a single, larger one-port circuit, using the relational operations of inversion and addition.

We conclude this section by remarking that the preservation of monotonicity under port interconnection, proved in Proposition 1, can be reinterpreted in terms of negative feedback. As shown in Fig. 4, the negative feedback interconnection of two operators $F$ and $G$ can be represented as a parallel interconnection of $F^{-1}$ and $G$. Proposition 1 then allows us to recover the incremental form of the fundamental theorem of passivity.

**Corollary 1:** Given two operators $F$ and $G$, each monotone on a Hilbert space $\mathcal{H}$, their negative feedback interconnection $\left( F^{-1} + G \right)^{-1}$ is monotone on $\mathcal{H}$.

**V. Algorithmic Steady-State Analysis of Series/Parallel Monotone One-Ports**

In this section, we develop an algorithmic method for computing the periodic input/output behavior of a monotone one-port. We consider a circuit made of series and parallel interconnections of one-port elements, each defining a (discrete time) monotone operator on $l_2(T)$. The circuit defines a monotone operator $M$. Concrete examples of such circuits are given in Sections VI and VII.

Without loss of generality, we consider the problem of computing the “output” current $i^*$ of the monotone operator $M$ corresponding to an “input” voltage $v^*$.

We compute the solution as the fixed point of an iterative splitting algorithm determined from the series and parallel structure of the circuit. The algorithm is first presented for two elements, then generalized to an arbitrary composition of series and parallel interconnections.

**A. Splitting Algorithms for Two Element Circuits**

There is a large body of literature on splitting algorithms, which solve problems of the form $0 \in M_1(u) + M_2(u)$, where $M_1 + M_2$ is a maximal monotone operator. If $M$ consists of two elements, connected in series or parallel, we can convert our problem to this form by writing $0 \in M_1(i) + M_2(i) - v^*$ (assuming a series interconnection—the parallel interconnection is obtained by exchanging $i$ and $v$). The offset $-v^*$ does not affect the monotonicity properties of $M$. Splitting algorithms distribute the computation on the components $M_1$ and $M_2$. They are useful when computation for the individual components is easy, but computation for their sum is hard. Here, we describe two splitting algorithms—the forwards/backwards splitting, and the Douglas–Rachford splitting. Given an operator $S$ and a scaling factor $\alpha$, the $\alpha$-resolvent of $S$ is defined to be the operator

\[ \text{res}_{\alpha S} := \left( I + \alpha S \right)^{-1}. \]

If $S$ is maximal monotone, $\text{res}_S$ is single-valued [25].

1) **Forward/Backward Splitting:** This is the simplest splitting algorithm [60], [61], [62]. Suppose $M_1$ and $\text{res}_{\alpha M_2}$ are single-valued. Then

\[ 0 \in M_1(x) + M_2(x) \iff 0 \in x - \alpha M_1(x) - (x + \alpha M_2(x)) \iff (I + \alpha M_2)x \ni (I - \alpha M_1)x \iff x = \text{res}_{\alpha M_2}(I - \alpha M_1)x. \]

The fixed point iteration $x^{k+1} = \text{res}_{\alpha M_2}(x^k - \alpha M_1(x^k))$ is the forward/backward splitting algorithm. When $M_1$ and $M_2$ are monotone, the convergence conditions for the forward/backward splitting are standard in the literature (see, for instance, [30]). [59, Sec. 6] generalize these conditions to cases where $M_1 + M_2$ is monotone, but either $M_1$ or $M_2$ is hypomonotone. These conditions may be summarized as follows.

**Proposition 2:** Let $\mu \geq 0$, $\omega \geq 0$, and $\beta > 0$, and $M_1$ and $M_2$ be operators on a Hilbert space $\mathcal{H}$. The forward/backward algorithm, with scaling factor $\alpha \in (0, 2/(\beta + 2\mu))$, converges to a zero of $M_1 + M_2$, if one exists, in each of the following cases.

1) $M_1$ is maximally $\mu$-monotone, $M_1 - \mu I$ is $1/\beta$-cocoercive, $M_2$ is maximally $(-\omega)$-monotone and $\mu \geq \omega$.
2) $M_1$ is maximally $(-\omega)$-monotone, $M_1 + \omega I$ is $1/\beta$-cocoercive, $M_2$ is maximally $\mu$-monotone and $\mu \geq \omega$.
3) $M_1$ is $\beta$-Lipschitz, $M_2$ is maximally $\mu$-monotone and $\mu \geq \beta$.

2) **Douglas–Rachford Splitting:** This most successful splitting algorithm forms the basis of the alternating direction method of multipliers [63], [64], [65].

The reflected resolvent, or Cayley operator, is the operator

\[ R_{\alpha S} := 2\text{res}_{\alpha S} - I. \]

Given two operators $M_1$ and $M_2$, a scaling factor $\alpha$ and an initial value $z^0$, the Douglas–Rachford algorithm is the iteration in $k$ given by

\[ z^{k+1} = T(z^k) \]
\[ x^k = \text{res}_{\alpha M_2} z^k \]

where $T$ is given by

\[ T = \frac{1}{2} (I + R_{\alpha M_1} R_{\alpha M_2}). \]

(1)
Theorem 5.1 in [58] gives the most general conditions for convergence of the Douglas–Rachford algorithm, again allowing one operator in the sum to be hypomonotone.

**Proposition 3:** Let $M_1$ and $M_2$ be operators on a Hilbert space $\mathcal{H}$. Let $\mu > \omega \geq 0$ and $\alpha \in (0, (\mu - \omega)/2\mu)$. The Douglas–Rachford algorithm converges to a zero of $M_1 + M_2$, if one exits, in each of the following cases.

1) $M_1$ is maximally $(-\omega)$-monotone and $M_2$ is maximally $\mu$-monotone.
2) $M_2$ is maximally $(-\omega)$-monotone and $M_1$ is maximally $\mu$-monotone.

**B. Nested Splitting Algorithm for Three Element Circuits**

If $M$ is composed of three elements, with one series interconnection and one parallel interconnection (see Fig. 6), $M$ has the form $M = M_3 + (M_2 + M_1)^{-1}$, and we can convert our problem to the form $0 \in (M_3 + (M_2 + M_1)^{-1})(u)$ again by offsetting by the input current or voltage. One approach to solving this problem is to use a splitting algorithm, such as the forward/backward algorithm, with the resolvent step applied for $M_3$ and the forward step applied for $(M_2 + M_1)^{-1}$. Applying this forward step amounts to solving $y = (M_2 + M_1)^{-1}(u)$ for some $u$, which may be rewritten as $0 \in (M_2 + M_1)(y) - u$. This can be solved by again applying the forward/backward algorithm.

This procedure has poor complexity: for every forward/backward step for $M_3 + (M_2 + M_1)^{-1}$, an entire fixed point iteration has to be computed for (an offset version of) $M_2 + M_1$. In this section, we propose an alternative procedure. Rather than applying a forward step for the relation $(M_2 + M_1)^{-1}$, we simply apply a single step of the fixed point iteration needed to compute this forward step, using the forward/backward algorithm. Assume, without loss of generality, that $d(M_3) = i \rightarrow v$ and $d(M_2) = d(M_1) = v \rightarrow i$ (the configuration shown on the left of Fig. 6). Suppose that $v^* \in (M_3 + (M_2 + M_1)^{-1})(i)$. Assume that $M_1$, $\text{res } \alpha_1 M_2$, and $\text{res } \alpha_2 M_3$ are single-valued. We then have

$$v^* \in v + M_3(i)$$

$$v \in (M_2 + M_1)^{-1}(i)$$

where $v$ is the voltage over $M_2$, illustrated on the left of Fig. 6. Equation (2) gives

$$i + \alpha_2 M_3(i) \ni i - \alpha_2 v + \alpha_2 v^*$$

$$i = (I + \alpha_2 M_3)^{-1}(i - \alpha_2 v + \alpha_2 v^*)$$

$$i = \text{res } \alpha_2 M_3(i - \alpha_2 v + \alpha_2 v^*)$$

Equation (3) gives

$$i \in (M_2 + M_1)(v)$$

$$v + \alpha_1 M_2(v) \ni v - \alpha_1 M_1(v) + \alpha_1 i$$

$$v = (I + \alpha_1 M_2)^{-1}(v - \alpha_1 M_1(v) + \alpha_1 i)$$

$$v = \text{res } \alpha_1 M_2(v - \alpha_1 M_1(v) + \alpha_1 i).$$

This shows that a fixed point of the iteration

$$v^{k+1} = \text{res } \alpha_1 M_2(v^{k} - \alpha_1 M_1(v^{k}) + \alpha_1 i^k)$$

$$i^{k+1} = \text{res } \alpha_2 M_3(i^k - \alpha_2 v^{k+1} + \alpha_2 v^*)$$

is a solution to our original problem. In the following section, we generalize this algorithm to an arbitrary series/parallel monotone one-port, and in Theorem 1, we give a general condition under which the algorithm is guaranteed to converge to such a fixed point. The three element circuits of this section are revisited in Example 1.

**C. Nested Splitting Algorithm for Arbitrary Series/Parallel Circuits**

In this section, we introduce a new splitting algorithm, the nested forward/backward algorithm, which generalizes the algorithm described in the previous section to monotone one-ports with arbitrary series and parallel interconnections, which have the general form shown in Fig. 7 (allowing elements to be open circuits, short circuits, or whole subcircuits). We assume for simplicity that the relations $G_j$ and $R_j$ are single-valued, although the extension to multivalued relations is straightforward.

The $v \rightarrow i$ operator of the circuit in Fig. 7 is given by

$$i_n = \left( R_n + \left( G_n + \ldots + (R_1 + R_0)^{-1} \ldots \right)^{-1} \right)^{-1}(v_n).$$

(5)

If each inversion is solved using a fixed point iteration, the number of fixed points that must be computed scales with order $O(m^n)$, where $n$ is the number of inverses in (5), and $m$ is the number of steps needed to compute each inverse. Following the argument of the previous section, the nested forward/backward algorithm, given in Algorithm 1, solves equations of the form (5) by replacing inverse operators with a single step of the forward/backward iteration needed to compute them. In this way, every inversion is computed simultaneously, using a single fixed point algorithm.

**Theorem 1:** Algorithm 1 converges to a solution of (5) as $k \rightarrow \infty$ if $R_0$ is coercive and Lipschitz, all the $R_j$, $G_j$ are monotone for $j = 1, \ldots, n$, and the eigenvalues of $A$ all lie within the unit
Algorithm 1: Nested Forward/Backward Algorithm.

1: Data: Series/parallel one-port with $2n$ elements, step sizes $\alpha_j > 0$, $j = 1, \ldots, 2n - 1$, external signal $v_n$, convergence tolerance $\epsilon > 0$.
2: for $j = 1, \ldots, n$ do
3: Initialize $v_{j-1}^k, i_j^k$.
4: end for
5: $k = 1$
6: do
7: \[ v_{j}^{k+1} = \text{res}_{\alpha_j, R_j} (v_{j}^k - \alpha_j R_0 (v_{j-1}^k) + \alpha_j v_{i_j}^k) \]
8: for $j = 2, \ldots, n$ do
9: \[ v_{j}^{k+1} = \text{res}_{\alpha_2, -G_j} (v_{j-1}^k - \alpha_2 \gamma_2 (v_{j-2}^k - \gamma_2 i_{j-1}) + \alpha_2 \gamma_2 i_{j}^k) \]
10: \[ i_{j}^{k+1} = \text{res}_{\alpha_2, -G_j} (i_{j}^k - \alpha_2 \gamma_2 (i_{j-1}^k - \gamma_2 v_{j-2}) + \alpha_2 \gamma_2 v_{j-1}) \]
11: end for
12: $k = k + 1$
13: while $\max_j (|v_{j}^{k+1} - v_{j}^k|, |i_{j}^{k+1} - i_{j}^k|) > \epsilon$

For this circuit, the matrix $A$ is given by
\[
\begin{pmatrix}
\gamma_1 \beta_1 & \gamma_1 \alpha_1 \\
\alpha_2 \beta_1 \gamma_2 \alpha_1 & \gamma_2 (1 + \gamma_1 \alpha_2) \\
\alpha_3 \alpha_2 \beta_1 \gamma_2 \gamma_2 \alpha_1 & \alpha_3 \gamma_2 (1 + \gamma_1 \alpha_2) \\
\alpha_4 \alpha_3 \alpha_2 \beta_1 \gamma_2 \gamma_2 \gamma_2 \alpha_1 & \alpha_4 \alpha_3 \gamma_2 \gamma_2 (1 + \gamma_1 \alpha_2)
\end{pmatrix}
\]

and so on, where, for $j = 1, \ldots, n$, $\gamma_{2j-2}$ is a Lipschitz constant of $\text{res}_{\alpha_2, -G_j}$, $\gamma_{2j-1}$ is a Lipschitz constant of $\text{res}_{\alpha_2, -G_j}$, and $\beta_1$ is a Lipschitz constant of the operator $(I - \alpha_1 R_0)$.

To clarify, the constants $\alpha_j$ may be chosen to tune the convergence rate of the algorithm. The constants $\beta_1$ and $\gamma_j$ must be Lipschitz constants for the relevant operators. Coercivity and Lipschitz continuity of $R_0$, say with constants $\mu$ and $\lambda$, respectively, means that $\alpha_j$ can always be chosen so that $0 < \beta_1 < 1$ by the formula $\beta_1 = 1 - 2 \mu \alpha_1 + \lambda \alpha_1^2$ [57, p. 39]. Monotonicity of $R_j$ and $G_j$ for all $j$ implies that all resolvents used in the algorithm are nonexpansive, so the $\gamma_j$ are at most equal to 1.

If, furthermore, an element $R_j$ or $G_j$ is $\mu_j$-coercive, we have $\gamma_j = 1/(1 + \alpha_j \mu_j)$. In the limiting case $\alpha_j = 0$ for all $j$, the matrix $A$ is the identity, and has all its eigenvalues on the boundary of the unit disc. Before giving the proof of Theorem 1, we revisit the three element circuits of Section V-B.

Example 1: Consider the circuit shown in the left of Fig. 6, consisting of three elements, $M_1, M_2$, and $M_3$. Section V-B describes a special case of Algorithm 1 for this circuit. In this example, we apply Theorem 1 to this circuit, and give a convergence condition for the fixed point iteration given by (4a).
Let $u^k$ and $w^k$ be two sequences of iterates generated by Algorithm 1, with the same input $u^k_n = u^k_m = v^k$, and denote $u^j - w^k_j$ by $\Delta u^j_k$. It then follows from lines 7, 9, and 10 of Algorithm 1 that, for $j = 1, \ldots, 2n - 1$

$$
\|\Delta u^j_{k+1}\| \leq \gamma_1 \|\Delta u^j_k\| - \alpha_1 \Delta R_0(u^k) + \alpha_1 \Delta u^j_{k+1}
$$

and for $j = 1, \ldots, n$

$$
\|\Delta u^j_{k+1}\| \leq \gamma_j \|\Delta u^j_k\| - \alpha_j \Delta R_1(u^k) + \alpha_j \Delta u^j_{k+1}
$$

from which it follows, via the triangle inequality that

$$
\|\Delta u^j_{k+1}\| \leq \gamma_1 \beta_1 \|\Delta u^j_k\| + \gamma_1 \alpha_1 \|\Delta u^j_{k+1}\|
$$

and

$$
\|\Delta u^j_{k+1}\| \leq \gamma_j \beta_j \|\Delta u^j_k\| + \gamma_j \alpha_j \|\Delta u^j_{k+1}\|
$$

where $\Delta u^j_k = 0$ for all $k$. Let $n(\Delta u^k)$ denote the vector $(\|\Delta u^1_k\|, \|\Delta u^2_k\|, \|\Delta u^3_k\|, \|\Delta u^4_k\|, \ldots)$. It follows that

$$
n(\Delta u^k_{k+1}) \leq A n(\Delta u^k) \leq A^k n(\Delta u^1)
$$

where $A$ is the matrix given in the statement of the theorem. It follows from the nonnegativity of $n(\Delta u^k_{k+1})$ (or from the elementwise nonnegativity of $A$) that $A^k n(\Delta u^1)$ is elementwise nonnegative for all $k$. We then have $0 \leq n(\Delta u^k_{k+1}) \leq z^{k+1}$, where $z^{k+1}$ is the solution to the difference equation $z^{k+1} = A z^k$ with initial condition $n(\Delta u^1)$. Since the eigenvalues of $A$ are within the unit circle, it is a standard result of linear systems theory that there exist a norm $\|\cdot\|_P$ and rate $0 < \lambda < 1$ such that $\|z^{k+1}\|_P \leq \lambda \|z^k\|_P$. It follows that the sequence $n(\Delta u^k)$ converges to the zero vector in the norm $\|\cdot\|_P$ at least as fast as the sequence $z^k$. It then follows from the Banach fixed point theorem that each $u^k_j$ converges to a limit $u^j_k$ as $k \to \infty$, which completes the proof.

Theorem 1 demonstrates the validity of Algorithm 1, in that it proves the existence of circuits for which the algorithm is guaranteed to converge. In simple cases, like that of Example 1, the condition can furthermore be used as a design tool. Theorem 1 raises several questions for future research. The first is whether a general solution exists for the step sizes $\alpha_j$, which minimizes the spectral radius of $A$. Furthermore, Theorem 1 is conservative, relying on a small gain argument and proving contraction, a strong convergence property. An interesting question is whether there exist less conservative convergence conditions.

VI. RLC CIRCUITS

Here, we consider one-port circuits formed by the series and parallel interconnection of resistors, capacitors, and inductors. This is the class of circuits considered in the conference version of this article [55].

A resistor is an operator $R$ on $\mathbb{R}$, the device law, between current and voltage

$$
R = \{(i, v) \in \mathbb{R} \times \mathbb{R} | v \in R(i)\}.
$$

A resistor defines a 1-port operator on $L_{2,T}$ by applying the operator $R$ at each time

$$
\mathcal{R} = \{(i, v) \in L_{2,T} \times L_{2,T} | (i(t), v(t)) \in R \text{ for all } t\}.
$$

Given $i, v \in L_{2,T}$, define the charge $q(t) = \int_0^t i(\tau) \, d\tau$ and the magnetic flux linkage $\phi(t) = \int_0^t v(\tau) \, d\tau$. A capacitor is an operator $C$ on $L_{2,T}$ between voltage and current, defined by a device law $C(\cdot) : \mathbb{R} \to \mathbb{R}$ which maps voltage to charge. We assume that $C$ is single-valued and differentiable

$$
C = \{(v, i) \in L_{2,T} \times L_{2,T} | q = C(v), \frac{d}{dt} q = i\}.
$$

An inductor is given by an operator $L$ on $L_{2,T}$ between the current and voltage, defined by a device law $L(\cdot) : \mathbb{R} \to \mathbb{R}$, which maps current to magnetic flux linkage. Again we assume $L$ to be single-valued and differentiable

$$
L = \{(i, v) \in L_{2,T} \times L_{2,T} | \phi = L(i), \frac{d}{dt} \phi = v\}.
$$

The following proposition shows that resistors map $T$-periodic inputs to $T$-periodic outputs, capacitors map $T$-periodic voltages to $T$-periodic currents, and inductors map $T$-periodic currents to $T$-periodic voltages.

Proposition 4: Single-valued memoryless operators and the derivative map $T$-periodic inputs to $T$-periodic outputs.

Proof: Let $f$ be a single-valued memoryless operator, that is, an operator between $u$ and $y$ such that $y(t) = f(u(t))$. Then, $y(t + T) = f(u(t + T)) = f(u(t)) = y(t)$. The property also holds for the derivative

$$
\frac{du(t)}{dt} = \lim_{h \to 0} \frac{u(t) + u(t + h)}{h} = \lim_{h \to 0} \frac{u(t + T) + u(t + T + h)}{h} = \frac{du(t + T)}{dt}.
$$

The following proposition gives a characterization of the monotonicity of resistors on $L_{2,T}$ in terms of their device laws.

Proposition 5: A resistor is monotone on $L_{2,T}$ if and only if its device law defines a monotone operator on $\mathbb{R}$ between $i(i)$ and $v(t)$ for all $t$.

Proof: If: By monotonicity of the device law on $\mathbb{R}$, we have

$$
(i_1(t) - i_2(t))(v_1(t) - v_2(t)) \geq 0 \forall t
$$

from which it follows that

$$
(i_1(t) - i_2(t))(v_1(t) - v_2(t)) = \int_0^T (i_1(t) - i_2(t))(v_1(t) - v_2(t)) \, dt \geq 0.
$$

Only If: Assume by contradiction that the device law is not monotone on $\mathbb{R}$, that is, there exist $i_1, i_2 \in \mathbb{R}$ such that

$$
(i_1 - i_2)(R(i_1) - R(i_2)) < 0.
$$

Taking the constant signals $i_1(t) = i_1, i_2(t) = i_2$ on $L_{2,T}$ shows that the resistor is not monotone on $L_{2,T}$. A natural question is whether the same can be said for inductors and capacitors—are these devices monotone if their device
laws $C$ and $L$ are monotone? A striking result of [66] is that this is true if and only if the device laws are linear.

**Proposition 6**: Capacitors and inductors with monotone device laws on $\mathbb{R}$ are monotone on $L_{2,T}$ for all $T \geq 0$ if and only if their device laws are linear.

**Proof**: The result is given by [67, Lemma A.2], noting that the signals used in their proof (A.4) are truncated square waves, which are signals on $L_{2,T}$ for $T$ equal to the length of the truncation.

We now collect some results, which show that, under mild conditions, series/parallel RLC circuits define operators on $L_{2,T}$.

**Proposition 7**: A parallel interconnection of $n$ one-ports which map $T$-periodic voltages to $T$-periodic currents also maps $T$-periodic voltages to $T$-periodic currents.

**Proof**: Periodicity is preserved under summation of signals, and therefore, preserved by Kirchoff’s laws. Indeed, if $y(t) = u_1(t) + u_2(t)$, and $u_1$ and $u_2$ are both $T$-periodic, then $y(t + T) = u_1(t + T) + u_2(t + T) = u_1(t) + u_2(t) = y(t).

Next, we show that one-port circuits, which obey simple conditions on their interconnections map periodic inputs to periodic outputs. Other classes of systems with this property include contractive state space systems [67] and approximately finite memory input/output maps [68].

**Theorem 2**: Let $M$ be the operator on $L_{2,T}$, from either $v$ to $i$ or $i$ to $v$, of a 1-port constructed from the series and parallel interconnection of $n$ constituent one-ports $M_i$, such that the construction obeys the following conditions:

1. $M_i : L_{2,T} \rightarrow L_{2,T}$ for all $i$;
2. any one-port which must be inverted during the construction is coercive and Lipschitz.

Then, $M$ maps any input in $L_{2,T}$ to a unique output in $L_{2,T}$.

**Proof**: By assumption, each of the relations $M_i$ maps $T$-periodic inputs to $T$-periodic outputs (we denote this property by PIPO for the rest of this proof). We show that constructing a circuit under the given conditions preserves this property. This amounts to showing that the PIPO property is preserved under summation and inversion. We have already observed that it is preserved under summation in Proposition 7. It remains to show that inversion preserves the PIPO property if the one-port to be inverted is coercive and Lipschitz. Let $F$ be $\mu$-coercive and $\lambda$-Lipschitz. We will proceed by showing that $F$ is invertible on $L_{2,T}$: for every $y^* \in L_{2,T}$, there exists $u^* \in L_{2,T}$ such that $u^* \in F^{-1}(y^*)$. This shows that $F^{-1}$ maps periodic $y^*$ to periodic $u^*$, that is, has the PIPO property.

Let $y^* \in L_{2,T}$ be arbitrary and define the incremental relation $\Delta F(u) = F(u) - y^*$ on $L_{2,T}$. $\Delta F$ has the same coercivity and Lipschitz properties as $F$, independent of the choice of $y^*$. Given $\gamma > 0$, it is straightforward to check that the operator $I - \gamma \Delta F$ is an operator on $L_{2,T}$. We show that this operator is a contraction mapping on $L_{2,T}$ for small enough $\gamma > 0$, using the standard argument for proving convergence of the forward step algorithm [31, Sec. 2.4.3]. Indeed

$$
\| (I - \gamma \Delta F)(x) - (I - \gamma \Delta F)(y) \|^2
= \| x - y \|^2 - 2 \gamma \langle x - y, \Delta Fx - \Delta Fy \rangle + \gamma^2 \| \Delta Fx - \Delta Fy \|^2
\leq (1 - 2 \gamma \mu + \gamma^2 \lambda^2) \| x - y \|^2
$$

where the inequality follows from the definitions of coercive and Lipschitz operators. Solving $0 < (1 - 2 \gamma \mu + \gamma^2 \lambda^2) < 1$ gives an allowable range of $\gamma \in (0, 2 \mu / \lambda^2)$ for $I - \gamma \Delta F$ to be a contraction mapping on $L_{2,T}$. It then follows from the Banach fixed point theorem that $I - \gamma \Delta F$ has a unique fixed point $u^* \in L_{2,T}$ [57, Sec. 2.4.2], [69]

$$
u^* = u^* - \gamma \Delta F(u^*)
\iff \Delta F(u^*) = F(u^*) - y^* = 0
\iff F(u^*) = y^*.
$$

As $y^* \in L_{2,T}$ is arbitrary, this shows that $F$ is invertible on $L_{2,T}$.

When applied to RLC circuits, condition 1 of Theorem 2 requires capacitors to be connected in parallel and inductors to be connected in series.

Nonlinear RLC circuits have also been recently studied as port interconnections of incrementally port-Hamiltonian systems [70]. While port-Hamiltonian systems are always passive, the authors observe that incrementally port-Hamiltonian systems are not always monotone. They arrive at the same conclusion that those RLC circuits that are monotone are precisely those with nonlinear monotone resistors and LTI capacitors and inductors.

An interesting question is whether the class of monotone resistors, capacitors, and inductors can be extended beyond those allowed by Propositions 5 and 6. One possibility is to allow time-varying energy storage devices. Georgiou et al. [71] define time-varying, or adjustable, capacitors and inductors, termed the varcapacitor and varinductor

$$
i(t) = c(t) \frac{d}{dt} (c(t)v(t)) \quad \text{varcapacitor}
$$

$$
v(t) = l(t) \frac{d}{dt} (l(t) i(t)) \quad \text{varinductor}.
$$

If $i(t), v(t), l(t)$, and $c(t)$ are $T$-periodic, these devices are monotone on $L_{2,T}$.

**Proposition 8**: Varcapacitors with $T$-periodic $c(t)$ and varinductors with $T$-periodic $l(t)$ are monotone on $L_{2,T}$.

**Proof**: For a varcapacitor, we have

$$
\int_0^T (v_1(t) - v_2(t)) (i_1(t) - i_2(t)) \ dt
= \int_0^T c(t) (v_1(t) - v_2(t)) \frac{d}{dt} (c(t) (v_1(t) - v_2(t))) \ dt
= \int_0^T \frac{d}{dt} \frac{1}{2} c^2(t) (v_1(t) - v_2(t))^2 \ dt
= \frac{1}{2} c^2(T) v^2(T) - \frac{1}{2} c^2(0) v^2(0)
= 0.
$$

Likewise, for a varinductor, we have

$$
\int_0^T (v_1(t) - v_2(t)) (i_1(t) - i_2(t)) \ dt
= \int_0^T l(t) (i_1(t) - i_2(t)) \frac{d}{dt} (l(t) (i_1(t) - i_2(t))) \ dt
$$
We now give two detailed examples of the steady-state analysis of an RLC circuit. In order to obtain operators on \( i_2, \tau \), the derivative is discretized to give an operator \( D \). Any discretization may be used. For the examples in this article, we use the backwards finite difference, given by the relation

\[
D = \left\{ (u, y) \mid y = \tau D_\tau u \right\}
\]

where \( D_\tau \) is the \( \tau \times \tau \) matrix

\[
D_\tau = \begin{bmatrix}
1 & 0 & \ldots & 0 & -1 \\
-1 & 1 & \ldots & 0 & 0 \\
0 & -1 & \ldots & 0 & 0 \\
\vdots & \vdots & \ddots & \vdots & \vdots \\
0 & 0 & \ldots & -1 & 1 \\
\end{bmatrix}
\]

Note that \( D \) is a maximal monotone operator, as \( D_\tau + D_\tau^\top \succeq 0 \) [57, Sec. 2.2.3]. To obtain an accurate discrete model, a sufficient number of time steps must be used.

**Example 2:** An envelope detector is a simple nonlinear circuit consisting of a diode in series with an LTI RC filter (see Fig. 9). It is used to demodulate AM radio signals.

We model the diode using the Shockley equation:

\[
v_{\text{diode}} = R_{\text{diode}}(i) := nV_T \ln \left( \frac{i}{I_s} + 1 \right)
\]

where \( I_s \) is the reverse bias saturation current, \( V_T \) is the thermal voltage, and \( n \) is the ideality factor. The \( i - v \) graph of the diode operator is strictly increasing with no endpoints; the diode operator is, therefore, maximal monotone.

The RC filter is itself a parallel interconnection of a resistor and capacitor, which maps voltage to current

\[
G_{\text{RC}} = CD + \frac{1}{R} I
\]

where \( I \) is the \( \tau \times \tau \) identity matrix. As \( G_{\text{RC}} \) is linear, it has a Lipschitz constant \( L \) equal to its largest singular value (which will grow with the size of \( D \)) and is coercive with constant

\[
m = \lambda_{\min}((G_{\text{RC}}^2 + G_{\text{RC}}^\top)^2)/2 \]

The Incremental voltage \( \Delta v = v - v^* \) is given as an operator of \( i \) by

\[
\Delta v = R_{\text{diode}}(i) + R_{\text{RC}}(i) - v^.*
\]

Given an input voltage \( v^* \), we solve for the corresponding current \( i^* \) using the Douglas–Rachford splitting. This involves applying both the resolvents \( \text{res}_{\text{RC}} \) and \( \text{res}_{\text{diode}} \). The resolvent \( \text{res}_{\text{RC}} \) is given by \( (I + \lambda G_{\text{RC}}^{-1})^{-1} \). This matrix is precomputed and stored in memory. The resolvent of the diode, \( \text{res}_{\text{diode}} \), is given by \( \text{res}_{\text{diode}}^{-1}(x) = (I + \lambda R_{\text{diode}}(x) - \lambda v^*) \). There is no analytic expression for this operator. Rather, the resolvent is computed numerically using the guarded Newton algorithm [32].

Fig. 10 shows the results of performing this scheme with an input of \( v^* = \sin(2\pi t) \) A, with \( R = 1 \Omega \), \( C = 1 \text{ F} \), \( I_s = 1 \times 10^{-14} \text{ A} \), \( n = 1 \), and \( V_T = 0.02585 \text{ V} \). Algorithmic parameters are \( \alpha = 0.01 \), \( \epsilon = 1 \times 10^{-5} \), and 500 time steps used is 500.

**Example 3:** In this example, we analyze the large-scale circuit shown in Fig. 11, which consists of \( n \) identical units, each consisting of a diode and LTI RC filter. The diode and RC filter are modeled as in Example 2.

When viewed as an interconnection of one-ports, the circuit has a recursive structure. Following the notation of Fig. 11, for \( 1 \leq m \leq n \), we have

\[
v_m = R_m(i_m)
\]

\[
= R_{\text{diode}}(i_m) + G_n^{-1}(i_m)
\]

\[
i_m = G_{m-1}(v_{m-1})
\]

\[
= G_{\text{RC}}(v_{m-1}) + R_{m-1}^{-1}(v_{m-1}).
\]

The base case is \( G_1 = G_{\text{RC}} \). This circuit has the form of Fig. 7, with \( R_0 = G_{\text{RC}}^{-1}, R_j = R_{\text{diode}}, \text{and } G_j = G_{\text{RC}} \) for all \( j > 1 \). The circuit is solved using the nested forward/backward algorithm introduced in Section V.C.

Fig. 12 shows the results of performing this scheme with \( n = 100,000 \) repeated units (a total of 300,000 components). The input is \( v^* = 1 + \sin(2\pi t) \) A, with circuit parameters \( R = 1 \Omega \), \( C = 1 \text{ F} \), \( I_s = 1 \times 10^{-14} \text{ A} \), \( n = 1 \), and \( V_T = 0.02585 \text{ V} \). The number of time steps used is 256. Every \( \alpha_j \) is set to 1.5. With \( n = 100,000 \) units, computation took 1937 s on a standard desktop computer. With \( n = 10 \) units, computation took an average of 243 ms, over 21 runs.
This model class describes systems, which behave like resistors, in that they cannot store energy and do not produce a phase shift, but, unlike resistors, do have memory. This work was motivated by systems such as the Hodgkin–Huxley neural membrane model [74], thermistors and discharge tubes. In this section, we investigate the maximal monotonicity of some memristive circuits.

If \( \dot{x} = f(x, u) \) is a contractive, time-invariant state-space system and \( u(t) \) is a \( T \)-periodic input, there is a unique, globally asymptotically stable \( T \)-periodic output \( y(t) \) to the memristive system (6) [75]. The memristive system then defines an operator on \( L_{2,T} \), mapping the \( T \)-periodic input \( u(t) \) to the \( T \)-periodic output \( y(t) \).

To determine the monotonicity properties of memristive systems, we use the scaled relative graph (SRG). The SRG of an operator is a region of the extended complex plane, from which the incremental properties of the operator can be easily read. SRGs were recently introduced by [76] for the study of monotone operator methods in optimization, and have been used for the study of systems in feedback by the authors in [77] and [78]. We refer the interested reader to these references for the details of SRG analysis. An operator is \( \mu \)-monotone if and only if its SRG lies in the region \( \{ z \in \mathbb{C} \mid \text{Re}(z) \geq \mu \} \) [77, Proposition 3.3 and Th. 3.5].

**Example 4:** The Hodgkin–Huxley model represents a nerve axon membrane as a parallel interconnection of active ion channels with a capacitor [74]. Each ion channel is a time-varying conductance, which may be modeled as a memristive system. In this example, we consider the potassium conductance \( i = G_K(v) \), which is given by the equations

\[
\dot{i} = \bar{g}_K n^4 (v - v_K)
\]

\[
\frac{dn}{dt} = \alpha_n(v)(1 - n) - \beta_n(v) n
\]

\[
\alpha_n(v) = \frac{0.01(1 + v)}{\exp(1 + v/10) - 1}
\]

\[
\beta_n(v) = 0.125 \exp(v/80).
\]

Following [79], the constants \( \bar{g}_K \) and \( v_K \) are set to 19 mho/cm² and 12 mV, respectively. The dynamics in \( n \) are contractive [81, Proposition 1], therefore, the potassium conductance defines an operator on \( L_{2,T} \).

The analytical SRG of the potassium conductance is difficult to determine, but we can test its monotonicity by sampling its
the characteristic zero-crossing Lissajous figure of a memristive system [73].

VIII. CONCLUSION

In this article, we have shown that monotone—unlike passive—nonlinear circuits retain the strong physical and computational significance of passive linear circuits. Splitting algorithms allow the computation to be separated in a way which mirrors the topology of the circuit, and a new splitting algorithm has been introduced, which is suited to circuits with nested series/parallel interconnections. This method has been demonstrated on the classes of circuits built from maximal monotone resistors and LTI capacitors and inductors, and memristive dynamic conductances, such as the neuronal conductances of the Hodgkin–Huxley model.

The mathematical property of monotonicity connects the physical property of energy dissipation with a well-established algorithmic theory for computation, for systems modeled as nonlinear operators. This mirrors the connection between energy dissipation in LTI state space systems and computational methods for LMs, established by the theory of dissipativity [8]. Preliminary work by the authors [81] shows that the algorithmic methods proposed here may be extended beyond the class of systems formed by the interconnection of monotone elements, to those systems formed by the difference of monotone elements. This includes systems with self-sustaining oscillations.

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