Hardware Versus Software Fault Injection of Modern Undervolted SRAMs

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Abstract—To improve power efficiency, researchers are experimenting with dynamically adjusting the supply voltage of systems below the nominal operating points. However, production systems are typically not allowed to function on voltage settings that is below the reliable limit. Consequently, existing software fault tolerance studies are based on fault models, which inject faults on random fault locations using fault injection techniques. In this work we study whether random fault injection is accurate to simulate the behavior of undervolted SRAMs.

Our study extends the Gem5 simulator to support fault injection on the caches of the simulated system. The fault injection framework uses fault maps, which describe the faulty bits of SRAMs, as inputs. To compare random fault injection and hardware guided fault injection, we use two types of fault maps. The first type of maps are created through undervolting real SRAMs and observing the location of the erroneous bits, whereas the second type of maps are created by corrupting random bits of SRAMs. During our study we corrupt the L1-Dcache of the simulated system and we monitor the behavior of the two types of fault maps on the resiliency of six benchmarks. The difference among the resiliency of a benchmark when tested with the different fault maps can be up to 24%.

Index Terms—Fault Injection, Fault Models, Voltage Underscaling, SRAMs

I. INTRODUCTION

As predicted by Moore’s Law, the scalability of semiconductor manufacturing process has been the driving force behind the increase in the capabilities of computer systems. However, scaling in lower nanometer geometries has led to variability of transistor characteristics, resulting into increased failure rates in modern CPUs. Conventional techniques for providing reliable execution include extra provisioning in logic and memory circuits in the form of increased voltage margins and reduced operating frequencies (so-called guardbands), as well as special error correction circuitry. But all these techniques consume more power, thus they are not very attractive in light of the ambitious goal to reach exascale performance with constrained power budgets. More specifically, guardbanding may increase power dissipation in the order of 35% [9].

A promising way to increase the energy efficiency of modern systems, is to remove these guardbands by reducing the supply voltage of the system while keeping the operating frequency constant. By doing so, the energy/power consumption of the system is decreased on average by 20% [14], [16]. One of the key aspects of this technique is that the performance remains the same, since frequency remains the same, all the energy saving results from the power reduction of the system.

On the one hand, there are many studies which perform supply voltage underscaling on real systems and monitor the system. These studies either focus on very specific architectures and technologies, for example SRAMs [1], [12], [19] or they perform voltage underscaling on the entire system and monitor the system as a black box [14], [15]. In the first case, the studies provide very accurate descriptions of the fault locations and the timings of the faults, however the specific observations are limited to the specific system and technology. On the second case, there is almost no information on the actual fault rate as errors are observed in the output of the software, thus masked faults are not captured at all.

On the other hand, there are studies which implement software based fault tolerance techniques which try to yield the energy benefits of voltage underscaling and will handle potential errors at the software level [2], [16]. To evaluate these techniques, they employ fault injection mechanisms which are guided by fault models and predicts the probability of a fault for a specific voltage setting. Fault models typically, uniformly distribute faults to all faulty locations. The uniform distribution of errors is not accurate. For example, when underscaling the supply voltage of SRAMs, spatially related errors are common [18], [19].

In this paper, we compare the accuracy of random based fault injection with the accuracy of hardware guided fault injection when undervolting the SRAM of a system. We implemented a fault injector framework which uses fault maps as inputs in Gem5 [6]. The faults are injected during the execution of the simulation. In the end we observe the manifestation of faults to the applications output. The fault maps are created using 1) A fault model in which the number of injected faults is guided by the number of faults appearing on different real SRAMs, but the faulty location is randomly selected [11]. 2) Actual fault maps publicly available from [17]. These fault maps describe the number of errors as well as their specific bit location of actual undervolted SRAMs.

The main contributions of this work are the following:

• We extend the Gem5 simulator to support fault injection on the different caches of the system. The fault injection framework uses as input a fault map, which describes the location of the faults. These faults are injected during the execution of the simulation
• We evaluate two fault types of fault maps, the first fault maps are created with random fault injection fault
model, whereas the second are fault maps created by undervolting real SRAMs and capturing the location of the errors.

The rest of the paper is structured as follows. In Section II we motivate our study. Section III describes the methodology we used to perform our analysis and study. In Section IV we present our evaluation. Section V outlines the related work and Section VI concludes the paper.

II. MOTIVATION

In this paper, we study whether random fault injection guided only by a fault rate is sufficient to capture the realistic fault manifestation of undervolted errors. Evaluating fault models is of great importance as the coverage of any software error detection technique actually depends on the fault model. On the one hand, spending resources to detect errors which will never appear is not efficient. On the other hand understanding the actual manifestation of undervolted errors on the software/architecture level can result to more accurate error detection mechanisms.

Fault models guide the procedure of fault injection, which is the typical method to evaluate the robustness of a system. Depending on the approach different fault injections techniques can be utilized. For example, when trying to detect errors during the execution of the application, researchers typically use random based fault injection techniques. This random fault injection is usually guided by a fault model which determines the number of errors to inject in each experiment [7], [11], [16] depending on the supply voltage. These models are agnostic to the actual hardware fault location. Since their techniques are agnostic to the underlying architecture and thus they should detect a wide range of errors without focusing on how these faults are propagated to the software level.

However, a specific SRAM block will behave deterministically when applying voltage underscaling. In other words, the errors will appear on deterministic fault locations for the specific SRAM and the specific supply voltage [18]. Although, the same SRAM structure on different chips will present different fault locations, all of the studied undervolted SRAMs present a spatial error locality [19]. In other words, bits that are in close proximity from a faulty bit have higher probability to be also faulty. Moreover, when undervolting an SRAM structure there exist a fault inclusion property [19]. Namely, when a bit is faulty for an undervolted supply voltage setting \( V_u \) it will be faulty for any supply voltage \( V_x < V_u \). This behavior is again not captured by random based fault injection methods.

In Figure 1 we present two different fault maps, the first one in Figure (a) is created by using a random fault model, the second one, in Figure (b) is a fault map of an actual publicly available SRAM at [17]. Noticeably, although both fault maps present the same number of errors, the faulty locations are different. Namely in the random fault map, each bit has the same probability to manifest an error, therefore, all errors are distributed through the entire structure. On the other hand, on actual hardware, a few errors exist in the higher part of the figure, whereas most of them are clustered in the bottom of the figure. Interestingly, most of the errors are gathered in a column wise manner, in other words when an error appears in a specific column, there are many errors on the same column on lower lines [19].

III. METHODOLOGY

Our objective is to identify whether the hardware fault location matters from the perspective of the software when undervolting the SRAMs of the system. The methodology consists of 3 steps. The first step is the creation of fault maps. A fault map is a description of which bit or bits are faulty for a specific SRAM. Each generated fault map is given as input to a fault injection framework. The fault injection framework, is the second step of our methodology. It is based on Gem5 and simulates a faulty system. During the simulation, it corrupts the respective bits in the cache as described in the fault map. The procedure performs a single simulation for each fault map. The fault injection framework can inject errors to any cache of the system. Since simulation based fault injection is a timing consuming procedure, in this work we opt to study only the effect of faults corrupting the L1-DCache and not the remaining cache levels. The third step corresponds to the classification of the output. After each simulation we compare the output of the application with a golden output, an output that is created by the application when executed with no errors.

Depending this comparison the experiments are categorized into different categories. In the following sections we provide more detailed information for each of this steps.

A. Fault Map Generation

The hardware guided fault injection fault maps are provided in [17]. There exist different fault maps for a SRAM structure of 28nm for 7 different undervolted supply voltage settings, 0.54V – 0.60V with a step of 0.01V. For each of these settings there are 2060 individual fault maps, each one of them represents a single SRAM structure. Each SRAM is
of size 16K bits. There exist in total 2060 * 7 = 14420 different fault maps. From these fault maps only the 2174 maps manifest errors during the undervolting. The errors are stuck-at-0 ones, as previous studies show that the majority of undervolting SRAMs errors are stuck-at-0 [13, 19]. The number of errors in each fault map differs depending on the specific map. In Figure 2 we present from the faulty SRAM structures how many of them (Y-axis) exist with a specific number (X-axis) of errors. As depicted in Figure 2, most of the SRAMs structures present a small number of faults, namely 37%, 15%, 9% and 5% of the faulty SRAMs present 2, 4, 6, 8 of fault bits respectively.

The random fault injection fault maps are generated with the following methodology. For each of the faulty hardware faults maps we create an equivalent fault map in terms of number of faults. For example if the hardware fault map contains 4 faults we create a random fault map with also 4 faults. However, the location of the faults are distributed randomly in the bits of the SRAM. By doing so we can compare only the effect of the faulty location to the applications resiliency while preserving the error rate exactly the same among the two methods. From now on the hardware guided fault injection will be referred as HW FI whereas the random one as RND FI. In Figure 3 we depict the probability of a fault to occur on a specific bit using two fault map generation techniques. As it is obvious in the RND FI all bits have the same probability whereas in the HW FI bit on the higher addresses are more probable to manifest errors.

B. Fault Injection Framework

The fault injector framework uses a fault map, which was provided with one of the methods described above, as an input. During the initialization of the simulator the fault map is read and the framework creates a C++ object for each of the faults. A fault is described by the location, the timing, and corruption type. The location is described in a hierarchical order, type of cache (D / L1 cache), the cache level (L1, L2 etc), which byte to corrupt in the cache line and which bit in the byte. The timing behavior of the fault can be expressed as a transient, intermittent or permanent. Transient faults are injected once on a user defined simulation tick, intermittent ones are described by the duration of the fault and the initial simulation tick in which the fault start to appear. The permanent faults constantly corrupt the faulty bit. Finally the corruption type describes whether to set the bit on a specific value, this simulates stuck-at-X faults, or to just perform a a bit flip.

In Figure 3 we depict the probability of a fault to occur on a specific bit using the two fault map generation techniques. As it is obvious in the RND FI all bits have the same probability whereas in the HW FI bit on the higher addresses are more probable to manifest errors.

Fig. 2: Number of faulty SRAMs (X-axis) that manifest different number of stuck-at-0 faults (Y-axis)

Fig. 3: Figures representing the probability of an error to be faulty.

(a) Probability of error for every bit using RND FI.

(b) Probability of error for every bit using HW FI.
simulated with the Gem5 simulator and is orthogonal to the underlying Instruction Set Architecture (ISA). In this work we focus on a X86_64 system using system emulation mode. To project accurately the realistic SRAMs fault maps with the L1-D cache we use the same size of 16K\textit{bits} as the one used at the undervolting.

C. Benchmark description and categorization

To compare the random based location with hardware guided location fault models, we used 6 different benchmarks. 1) \textit{Jacobi}: an iterative numerical solver for determining the solutions of a diagonally dominant system of linear equations. 2) \textit{Blackscholes}: a benchmark of the Parsec suite \cite{5}. It implements a mathematical model for a market of derivatives, which calculates the buying and selling of assets so as to reduce the financial risk. 3) \textit{DCT}: Discrete Cosine Transform is a module of the JPEG compression and decompression algorithm \cite{20}. 4) \textit{MC}: applies a Monte Carlo approach to estimate the boundary of a sub-domain within a larger partial differential equation (PDE) domain, by performing random walks from points of the sub-domain boundary to the boundary of the initial domain \cite{21}. 5) \textit{Sobel}: a 2D filter for edge detection in images. 6) \textit{K-Means}: an iterative algorithm for grouping data points from a multi-dimensional space into \textit{k} clusters.

After each fault injection experiment the output is classified as: 1) \textit{Correct}. The applications’ output after injecting the faults is bitwise exact with the \textit{golden} output. 2) \textit{Silent Data Corruption (SDC)}, the application terminated normally, however, the output is not bitwise exact in comparison with the \textit{golden} one. 3) \textit{Crash}, the application failed to terminate.

The first categorization performs a classification of the faults on the resiliency of the application. However, this is not sufficient to completely characterize the effect of the faults to the quality of the application. Therefore we perform a further analysis on the quality of the output for the experiments that resulted into the \textit{SDC} category. For the visualization benchmarks \textit{DCT, Sobel} we use \textit{Peak Signal to Noise Ratio (PSNR)} as a quality metric, the largest the value the better the quality of the output. For the numerical applications \textit{Blackscholes, MC, Jacobi} we use the \textit{Average Relative Error}. Finally, for the \textit{K-Means} we use a quality metric the percentage of data points that were classified to the correct cluster. The second analysis of the quality of the output is of great importance. It actually captures whether the errors had a negative impact on the quality or not. Stating that an experiment is an \textit{SDC} is not sufficient. For example, there are cases in \textit{Sobel} in which two experiments were categorized as \textit{SDCs}, however, the first experiment resulted to a single wrong pixel, whereas the second just computed a black image.

IV. EVALUATION AND ANALYSIS

In Figure 4 we present the high level classification of the two fault injection methodologies for all the benchmarks we studied. Interestingly 99\% of the observed crashes were due to accessing unmapped memory regions (Segmentation faults), therefore we do not provide any further classification of crashes. As depicted, three benchmarks demonstrate significant differences among the two fault injection types. Namely \textit{Jacobi, Sobel} and \textit{Kmeans} present a 23\%, 24\% and 11\% higher crashing rates respectively in the case of \textit{RND FI}. In the case of \textit{HW FI} the higher addresses of the cache are more often corrupted, whereas in \textit{RND FI} all addresses have equal probability to be corrupted. These three benchmarks, store pointer values to lower addresses, therefore in the case of \textit{HW FI} this values are way more infrequently corrupted, hence the decreased \textit{crash} rates. The average fault probability of the two different fault injection methods are presented in Figure 5 as depicted in \textit{HW FI} the higher addresses are more probable to result into errors.

In Figure 5 we present the accumulated results for all the benchmarks, depending on the number of bit flips that occur per experiment. We only present experiments that corrupt up to 16 bits, since, as presented in figure 2 the number of SRAM structures that present more faults is very small, and therefore they do not provide any statistical significance. Interestingly, both fault injection methods can capture accurately the resiliency of the application to mask errors, since both correct

![Fig. 4: Classification of the fault injection experiments using the two different fault injection methods.](image1)

![Fig. 5: Classification of the fault injection experiments for all the benchmarks depending on the number of faulty bits.](image2)
In HW FI faults present a spatial locality, in other words the distance between any error is much smaller than the distance between errors of the RND FI. For example, in Sobel, which stores mainly pixel values in a specific cache line, any error corrupting this cache line will result to an SDC. In HW FI as the number of faults increase the probability to corrupt any cache line in the system does not increase equally, the same cache line or neighboring cache lines (which also store pixel values due to data locality) have a higher probability to have a corruption. Consequently, it is more likely for errors in HW FI to corrupt the same application structures and therefore, not deteriorating the outcome of the application even more.

A. Effect of faults to the Quality of the Output

Figure 6 depicts the quality of the output for each benchmark for the experiments that resulted into the SDC category. The quality of the benchmarks in the first row is presented in PSNR and % Correct Classifications in which the higher the value the better the quality is. The second row of the figure the quality is presented as Relative Error (RE) in which the lower the value the better the quality is. Since RE can be infinitely large, we bounded it to be up to 1.0, therefore there are small 'triangles' created on the top of each of the graphs, this is due to the concentration of experiments which present RE larger than 1.0.

Interestingly across all experiments the HW FI technique results in outputs with higher quality of the output, except of the Monte Carlo benchmark. To be more precise, in Sobel ( in Figure 6a ) the width of the ‘violin’ is broader at higher PSNR values, hence more experiments resulted to outputs with better quality. This is also depicted by the small white dot inside the violins, which represents the average accuracy with both fault injection methods, as the widest part of the ‘violin’ is observed at the value 100%. Consequently, although the algorithm resulted to different cluster centers, during the classification of the observations where assigned to the correct cluster. In any case, the HW FI presents once more a wider ‘violin’ at the highest value, therefore more experiments resulted in better quality values. The same effect can be observed in DCT, Blackscholes and in Jacobi. In Monte Carlo is the only benchmark which depicts identical qualities among the two fault injection methods, this is due to the randomization of the algorithm, Monte Carlo performs random walks, even if errors occur that corrupt the randomness of the application, the application itself considers these erroneous
values as a normal random value. Consequently in the end, the quality of the output for the 2 different fault injection approaches is almost identical.

V. RELATED WORK

The reliability implications as well as the energy efficiency of undervolted systems is heavily studied in literature. Bacha et al. \cite{3}, \cite{4} presents an approach which dynamically reduces voltage margins while always preserving safe operation. Their technique is based on the error correction ECC hardware built on modern processors such as the server-class Intel Itanium. Several approaches propose methods which ensure correct operation of caches under undervolted conditions at the microarchitectural level \cite{5}, \cite{6}, \cite{7}. Architectural techniques are presented to eliminate data corruption, and by extension enable cache operation at scaled voltage settings. The authors in \cite{18}, \cite{19} study the effect of undervolting on several SRAMs of FPGA and they observe the fault patterns and fault location. In our work we study the accuracy of random fault injection models to simulate the behavior of undervolted SRAMs. The authors in \cite{11} present a failure model of Near-Threshold Voltage (NTV) FinFET SRAMs. They propose the use of a Compound Poisson distribution for projecting yield estimates for memory arrays operating in the NTV region. Their model does not take into account the spatial locality that faults present when operating in the NTV region. In our work we experimentally monitor the effect of the fault spatial locality to the application resiliency and quality of output. The authors in \cite{2} simulate systems with undervolted Branch Predictor Unit and discuss the trade-offs of energy efficiency with the accuracy of the predictor. In this work we focus on undervolting the L1-DCache using real fault maps, and we discuss whether location agnostic fault injection approaches are sufficient to characterize the resiliency of applications.

VI. CONCLUSIONS

In this paper we present an approach to apply real undervolting SRAM fault maps to a simulated system and observe the resiliency of the applications. We compare the hardware guided fault injection approach with a random guided fault injection approach. There are significant differences in the coarse categorization of the resiliency of the application, which become more obvious as the number of faulty bits increases. There are also differences when inspecting the quality of the output among the two techniques. This is because in a realistic system not all fault locations have the same probability to present faults, therefore from the software perspective the faults can propagate to a limited number of software structures.

This result does not limit the applicability of random based fault injection. When designing a software fault tolerance technique the designer needs to take into account all possible fault locations, as the technique should be effective regardless of the underlying hardware. However, there is value in optimizing the fault tolerance techniques for a specific system. Similar to compilers, which optimize the source code for the specific hardware, given a set of realistic fault maps that describe the underlying hardware, one can optimize the fault tolerance techniques to be more effective against realistic errors, while being more efficient as the faulty locations are pruned.

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