Modelling transport in single electron transistor

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Abstract. We introduce a model of single electron transistor (SET). Simulation programme of SET is used as the exploratory tool in order to gain better understanding of process and device physics. This simulator includes a graphic user interface (GUI) in Matlab. The SET was simulated using GUI in Matlab to get current-voltage (I-V) characteristics. In addition, effects of device capacitance, bias, temperature on the I-V characteristics were obtained. In this work, we review the capabilities of the simulator of the SET. Typical simulations of the obtained I-V characteristics of the SET are presented.

Keywords: Coulomb blockable oscillation, single electron transistor, graphic user interface, I-V characteristics.

1. Introduction
Incredible progress in microelectronics has pushed the MOSFET dimension toward the nanoscale limits (10 nm). In the future it is probable that MOSFETs will be replaced by fundamental new devices, such as single electron transistors (SET). SETs have recently attracted much attention because of their nano feature size, ultralow power dissipation, new functionalities and CMOS compatible fabrication process. SET shows unique advantages in terms of low power consumption and of new characteristics related to its Coulomb blockage oscillations.

Until now, only two compact analytical models (Uchida et al, for single gate resistive symmetric SET [1] and Mahapatra et al, for asymmetric SET [2]) have been reported. We propose an improved model, which is more flexible and can be adapted for symmetrical and asymmetrical device geometries.

The aim of this work is to propose a model of SET, to build a simulator, and to simulate current-voltage characteristics of SET using graphic user interface (GUI) in Matlab.

In this work, we also review the capabilities of the simulator, summarize the theoretical approach and experimental results, and give examples of typical simulations of SET’s current-voltage characteristics.

2. Simulation results
A model of SET is shown in figure 1a. A SET is made from two tunnel junctions that share a common electrode. A tunnel junction consists of two pieces of metal supported by a very thin (about 1 nm) insulator. The only way for electrons is one of the metal electrodes to travel to the other electrode to tunnel through the insulator. Since tunnelling is a discrete process, the electric charge flows through the tunnel junction in multiples of e, the charge of electrons.
A quantum dot (QD) is usually formed in two dimensional electron gas (2DEG) in GaAs/AlGaAs using standard electron beam lithography. The QD is connected to the source and drain electrodes through tunnel barriers. The potential in the dot can be controlled by the gate electrode which is capacitive coupled to the QD (figure 1b). The current through the dot can be periodically modulated by the gate voltage (Coulomb oscillations). When the current is zero (Coulomb blockade), the number of electrons is fixed.

A proper operation of a SET device requires: 1) the tunnel junction resistances (drain resistance, $R_D$ and source resistance, $R_S$) to be greater than the quantum resistance (25.8 $\Omega$) to confine the electrons in the QD, 2) the charging energy of the QD capacitance to be larger than the available thermal energy to avoid electron tunnelling due to the thermal emission, and the total capacitance of QD is equal to the sum of all device capacitances, i.e. $C_T = C_G + C_D + C_S$.

![Figure 1](image1.png)

**Figure 1.** a) Structure of single electron transistor, b) equivalent diagram of SET.

The QD is connected to the source and drain electrodes through small tunnel barriers. The potential in the QD can be modified by the gate electrode which is capacitive coupled to the QD. The DC bias ($V_{DS}$) is applied and the current is measured as a function of $V_{DS}$ and $V_{GS}$. The SET parameters are: $C_S$, $C_D$, $C_G$, $\Gamma_S$, $\Gamma_D$.

The energy diagram of the SET is presented in figure 2 and it shows quantization in QD.

![Figure 2](image2.png)

**Figure 2.** Energy level diagram for SET and quantization in QD.

We have developed the model by solving the state equation for single electron tunnelling [3]. The drain current can be calculated by using the tunnelling rate of an electron through the tunnelling junction. The drain current ($I$) of single electron transistor is obtained from

$$I = |e| [P_0 \Gamma_D f_D - P_1 \Gamma_D (1 - f_D)] = |e| \left( \frac{\Gamma_S \Gamma_D}{\Gamma_S + \Gamma_D} \right) (f_D - f_S) = |e| \Gamma (f_D - f_S) ,$$

(1)

where

$$P_1 = 1 - P_0, \quad P_0 = \frac{\Gamma_S (1-f_S) + \Gamma_D (1-f_D)}{\Gamma_S + \Gamma_D} ,$$

(2)
\[ f_D = \frac{1}{1 + e^{-\frac{\mu_{S+1} - \mu_D}{k_B T}}} = \frac{1}{1 + e^{-\frac{\mu_{S+1} + V_D}{k_B T}}}, \quad (3) \]

\[ f_S = \frac{1}{1 + e^{-\frac{\mu_{S+1} - \mu_S}{k_B T}}} = \frac{1}{1 + e^{-\frac{\mu_{S+1}}{k_B T}}}, \quad (4) \]

and

\[ \mu_{N+1} = E_0 - \mu_{C_G} V_G + C_D V_D = -\mu_{C_G} (V_G - V_c) + C_D V_D \]

\[ \frac{C_T}{C_G^2} \]

Here, \( \Gamma_S \) and \( \Gamma_D \) are the electron tunnelling rate from source to island and from island to drain, respectively. The number of electrons in the island could be 0 or 1, \( P_n \) is the probability of finding \( n \) electrons in the island. \( f_S, f_D \) are probable distribution functions in source and drain, respectively. \( \mu \) is Fermi energy (electrochemical potential).

**Figure 3.** Typical I<sub>DS</sub>-V<sub>GS</sub> characteristics simulated by the simulator with value of \( V_{DS} = 1 \) mV. The symmetrical SET device parameters are: \( C_G = 2 \) aF, \( C_S = C_D = 1 \) aF, \( R_D = R_S = 1 \) MΩ.

The calculations of drain current (I) are awkward. Therefore, the characteristics of SET devices are usually calculated with numerical simulators. By utilizing the model, the I<sub>DS</sub> – V<sub>GS</sub> characteristics of SET having the parameters of \( C_S = C_D = 1 \) aF, \( C_G = 2 \) aF, and \( R_D = R_S = 1 \) MΩ are calculated as shown in figure 3. The results numerically calculated using the simulator are also illustrated. There are two factors undermining characteristics of SET: temperature and the drain voltage. Figure 3 demonstrates the typical Coulomb blockade oscillation behaviour in symmetrical SET I<sub>DS</sub>-V<sub>GS</sub> characteristics (\( R_D = R_S = 1 \) MΩ). It shows that the SET Coulomb blockade oscillation period (\( e/C_G \), \( e \) is the electronic charge) is dictated by SET gate capacitance. Here, it should be emphasized that the peak and the valley currents of Coulomb oscillations are perfectly represented by the model despite its simplicity.

**Figure 4.** Typical I<sub>DS</sub>-V<sub>GS</sub> characteristics simulated by the simulator with value of \( V_{DS} = 1 \) mV. The asymmetrical SET device parameters are: \( C_G = 2 \) aF, \( C_S = C_D = 1 \) aF, \( R_D = 0.5 \) MΩ, \( R_S = 1.5 \) MΩ.
Figure 4 demonstrates the typical Coulomb blockade oscillation behaviour in asymmetrical SET $I_{DS}$-$V_{GS}$ characteristics ($R_D = 0.5 \, M\Omega$, $R_S = 1.5 \, M\Omega$) with the same voltage, $V_{DS}$.

Figure 5 represents $I_{DS}$-$V_{GS}$ characteristics with value of $V_{DS} = 1 \, mV$ at different temperatures. One can note that the effects of temperature on Coulomb oscillations. The Coulomb oscillations of SET are clear at low temperature (10K). Current-voltage ($I_{DS}$-$V_{GS}$) characteristics showing the suppression of the Coulomb blockade by broadening at higher temperature (100 K). It also reveals the fact that it is not possible to obtain the Coulomb blockade in the device characteristics at high temperature.

Figure 5. Typical $I_{DS}$-$V_{GS}$ characteristics with value of $V_{DS} = 1 \, mV$ at different temperatures. Temperature range is from 10 K (top curve) to 100K (bottom curve) and the step is 50K. The symmetrical SET device parameters are: $C_G = 2 \, aF$, $C_S = C_D = 1 \, aF$, $R_D = R_S = 1 \, M\Omega$.

Figure 6 demonstrates $I_{DS}$-$V_{DS}$ characteristics of symmetrical SET at low temperature (10 K).

Figure 6. Typical $I_{DS}$-$V_{DS}$ characteristics of SET. The SET device parameters are: $C_S = 2 \, aF$, $C_G = C_D = 1 \, aF$, $R_D = R_S = 1 \, M\Omega$.

Figure 7. The effect of temperature ($T$) on $I_{DS}$-$V_{DS}$ characteristics. The Coulomb blockade region at low temperature (10 K) becomes thinner at higher temperature (100 K).

The effects of temperature on $I_{DS}$-$V_{DS}$ characteristics of SET are demonstrated in figure 7 and it shows that the Coulomb blockade region becomes thinner at higher temperature. Therefore, our
accurate analytical model can be able to capture both the effect of temperature and the effect of high $V_{DS}$ on the device characteristics. Figure 8 demonstrates conductance of SET device and it shows that the simulator can be able to compute another important characteristic of SET ($I_D/V_{DS}$).

![Figure 8. Conductance of the SET device.](image)

3. Conclusions
A model for SET devices has been reported. The proposed model has been verified at device level for both symmetrical and asymmetrical devices. A set of simulations is then successfully performed for different parameters of SET devices. The model is able to accurately describe the $I_{DS}$-$V_{DS}$ and $I_{DS}$-$V_{GS}$ SET characteristics at different temperature.

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