Multi-Core Platforms Energy Saving Scheduling Algorithm

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Abstract. In the world of embedded architecture, reliable performance and energy consumption are two most dominant parameters that need to be studied. When an embedded architecture is used as an Internet of objects, these two specifications play a major role in achieving good performance. Many algorithms for power consumption have been developed in the architecture and systems installed. This document provides an overview of previous research on energy savings through practical scheduling algorithms. It provides algorithms for efficient energy planning, contained in the literature on multimedia and multimedia platforms. An important part of the research described in this paper is the real-time energy-saving algorithms of multi-core platforms

Keywords: Scheduling, Multi-core, Performance, Energy, Processor, ISA.

1. Introduction
With the rapid growth in technology, the contemporary computing systems available in today's era are shrinking in size and weight, exhibiting high performance and are capable of communicating with each other over the network. This has made embedded systems common place in everyday life. Unlike general purpose systems, embedded systems receive input from different sources through sensors and provide output to different devices through actuators without human intervention. These systems are used in many diverse application areas namely, automated industry applications, automotive applications, avionics, defence applications, consumer electronics etc. embedded system are particularly made to perform real time tasks and in which timing of task plays a vital role.

Embedded systems [1] are made up of one or more micro-processors / microcontrollers that are connected via interconnection network. The power supply is nonuniformly distributed over various components of the system which leads to variable power density. The components that are used frequently and do intensive computations consume more power than other components. The areas with more power density generate more heat and result in increase in temperature and may lead to system failure.

In addition, heat dissipation becomes more challenging in embedded systems as compared to general purpose systems due to their small size. Therefore, energy optimization is an important issue in order to get longer battery life as well as for keeping the system free from failures.

In real time embedded system, realizing that demand of high-performance multi-core processors [2] in battery operated are increasing so that many researchers have concentrated on the energy efficiency of these systems. Many solutions have been proposed by hardware and software designers to deal with the problem of energy optimization in embedded systems and researchers are further working in this area.

This paper addresses the issue of energy consumption [3] of multi-core processor in real time embedded systems [4] at the level of operating system with the help of task scheduling on real time and various optimization techniques for energy. This paper gives various energy efficient task
scheduling algorithms for the optimization of both dynamic and static energy consumptions on multi-core platforms.

2. Related Works

Krainless, Shoaib Akram et.al.[5], proposed a real-time understanding of multi-core ISA and considered different ways to achieve accuracy. The authors also apply the same time and time constraints and combine all flows into one large core in the same amount of time, but equal time does not lead to the same progress. In addition, an equal progress chart is proposed that seeks to promote all flows equally.

Jian Chen and Lizy K. John, [6], proposed to plan programs in a non-hereditary multi-core system that uses ambiguous logic to calculate the compatibility between the program and the core by analyzing the characteristics of the program and the validation obtained, and then scheduling the program in the system.

Adeel Ahmed, David J Brown, et.al. [7], considering each CPU kernel as a resource that can be actively backed up and distributed. Based on this load forecast, you be predicting the load on the server and the core of the processor.

Tao Zhang, Xiaohui Pan, Wei Shu et.al. [8], effectively capture the symmetrical and asynchronous loads on the heterogeneous architecture, two scheduling mechanisms have been proposed, namely the priority table and the larger core distribution table. Methods of multi threaded program scheduling.

Seungwon Lee and Won Woo Ro [9], used optimal threads for core mapping, which are important issues for improving the processing of non-homogeneous multi-cores, are used and have non-homogeneous cores. By scheduling, heavy workloads can be made in the form of an out-of-order core, while other workloads can be made in sequence.

These papers suggest that heterogeneous multi-core architecture may offer significant advantages over the same multi-core architecture. The advantage of steam is the ability to apply the genetic process in parallel at the level of the thread, as well as the result of differences between the inside and outside of the thread.

To better understand the possibility of implementing a multi-core architecture, an assessment was made of a set of thread detection mechanisms. In parallel, it offers a wide range of inherited architectural threads, which are performed on average 18% better than the same architecture.

Extensive experiments have been performed to determine brain function, energy consumption and efficiency.

Experiments give important results and observations, for example, there are no power models running on different computer systems, and even for the same workload, brain power is not always an indicator of power consumption. For example, in some scenarios, such as hybrid processing and input / output, energy consumption is disproportionate and does not change with brain power.

Different computer systems with different configuration systems, such as processors, memory, and disks, have different power curves depending on the power consumption ratio, as different subsystems use different base power and dynamic power. Perform various workloads [10-12].

3. Conclusion

In this paper, different algorithms for scheduling multi-core architecture and energy efficiency in heterogeneous systems are discussed. The scheduling algorithms have been developed to reduce dynamic power for multi-core platforms. The algorithms considered in this paper allow reducing the dynamic energy consumption of the hard deadlines by performing the task of scheduling in all tasks.

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