HPIPE: Heterogeneous Layer-Pipelined and Sparse-Aware CNN Inference for FPGAs

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Abstract—We present both a novel Convolutional Neural Network (CNN) accelerator architecture and a network compiler for FPGAs that outperforms all prior work. Instead of having generic processing elements that together process one layer at a time, our network compiler statically partitions available device resources and builds custom-tailored hardware for each layer of a CNN. By building hardware for each layer we can pack our controllers into fewer lookup tables and use dedicated routing. These efficiencies enable our accelerator to utilize 2x the DSPs and operate at more than 2x the frequency of prior work on sparse CNN acceleration on FPGAs. We evaluate the performance of our architecture on both sparse Resnet-50 and dense MobileNet ImageNet classifiers on a Stratix 10 2800 FPGA. We find that the sparse Resnet-50 model has throughput at a batch size of 1 of 4550 images/s, which is nearly 4x the throughput of NVIDIA’s fastest machine learning targeted GPU, the V100, and outperforms all prior work on FPGAs.

I. INTRODUCTION

Recent work has shown that we can maintain accuracy and prune nearly 90% of the weights from neural networks [1]. If computation of the pruned parameters can be skipped with custom hardware accelerators, we can potentially realize latency and throughput improvements of up to 10x; however, the pruning process makes the data layout irregular and more challenging to efficiently accelerate. Recent works have tried to overcome this challenge by taking advantage of the flexible logic, routing, and memories available on FPGAs, but works targeting sparse Convolutional Neural Networks (CNNs) have been limited by low multiplier utilization and some inefficiencies in mapping certain layers to their hardware architecture [1].

Layers in a neural network each have a different set of properties (e.g. input dimensions, stride, kernel size, etc.) that make it challenging to optimize one type of Processing Element (PE) that is efficient for all of them, and the less regular structure of sparse CNNs heightens this challenge. For example, a convolutional layer with a kernel size of 7 x 7 in a neural network with 50 layers imposes a requirement that the PEs must be able to handle kernels that large, even if all of the other layers only use kernels of size 3 x 3. During most of the execution time, any additional hardware to support those larger kernels is underutilized. While not all architectures pay a substantial cost for variable kernel size specifically, they likely pay some penalty for some set of parameters that vary through the network. Most FPGA and ASIC accelerators use a PE architecture that overprovisions hardware in each PE to handle a variety of layer types.

In this paper we present a novel accelerator architecture that solves these problems by tailoring hardware specifically to each neural network layer and which naturally supports weight sparsity. We then pipeline across network layers to achieve high throughput and low latency. Since building custom PEs for each layer of every CNN architecture manually would be intractable, we also developed a network compiler that accepts a TensorFlow graph as input, performs per-layer optimizations, and produces a synthesizable verilog accelerator that implements the network. We integrate this with a PCIe core and validate network accuracy and accelerator throughput in physical hardware.

The contributions of this paper are as follows:

• The novel HPIPE architecture that allows layer-specific optimizations and dramatically reduces the amount of soft logic required to implement 0-weight skipping in convolutional neural networks.

• An automated flow that converts TensorFlow network models directly to an optimized HPIPE hardware implementation.

• An evaluation of the HPIPE architecture on a sparse ResNet-50 and two variants of MobileNet that both demonstrate the efficiency of our approach and yield higher throughput at batch size 1 than any FPGA or GPU solutions known to the authors.

II. BACKGROUND AND RELATED WORK

A. Convolutions

There are three types of 2D convolutions discussed in this work. The most basic is a 2D convolution that operates on a 3D tensor and outputs a 3D tensor. The weights have 4 dimensions, $k_h \times k_w \times c_i \times c_o$, where $k_h$ is the height of the weight tensor, $k_w$ the width, $c_i$ the size of the $z$ dimension of the 3D input tensor, and $c_o$ the size of the $z$ dimension of the output 3D tensor. At each $(x,y)$ point in the input image $c_o$ slices of the kernel with shape $k_h \times k_w \times c_i$ are multiplied element-wise and reduced by summation to produce $c_o$ output points.

The second type of convolution is a pointwise 2D convolution, which is a special case of the standard 2D convolution where $k_h \times k_w = 1 \times 1$.

The final type is what is called a depthwise convolution. In contrast to the basic convolution, the kernel is of shape $k_h \times k_w \times c_i \times n$ where $n$ is a channel multiplier that is typically 1. Also in contrast to the basic 2D convolution, the summation following the element-wise product reduces along only the $x$ and $y$ dimensions, so while there is no $c_o$, the
number of channels is preserved (or multiplied by the channel multiplier).

B. Sparsity and Weight Pruning

Weight pruning is the process of removing (assigning to zero) unimportant weights in a trained neural network. Recent works have shown that as many as 90% of the weights can be removed without impacting classification accuracy [1, 2]. This offers the opportunity to save memory and memory bandwidth by storing compressed weights, and also the opportunity to skip ineffectual multiplications by pruned (zero) weights.

C. Related Work

Many accelerators targeting FPGAs have taken advantage of sparsity for Fully Connected (FC) or Long Short Term Memory (LSTM) units [3, 4, 5, 6]. But fewer have taken advantage of sparsity in convolutional layers. FC layers and LSTMs have no weight re-use and are memory bound to begin with, so weight pruning provides both a computational and memory bandwidth reduction. By contrast convolutions share many weights so while we can reduce the computational requirements by pruning, the memory bandwidth reductions are less significant and come with an added cost of less regular computation and lower activation re-use. The authors are aware of two other attempts to accelerate sparse convolutions on FPGAs.

In [7], Kung et al. used a novel technique to prune weights and subsequently compress them back into dense weights by combining columns of non-overlapping weights together. The result was a very efficient accelerator, but the technique only works for pointwise convolutions. They also implemented a shift unit that implements something similar to a depthwise convolution, but their accelerator can only support one very specific type of neural network.

In [1], Lu et al. developed a PE-based sparse CNN accelerator that handles a wider variety of convolutions than [7]; however, their performance was limited by a lower frequency than comparable dense accelerators (200MHz), poor mappings of particular layers to their PEs, and a low DSP utilization of only 45% for an application that is primarily multiplication-bound.

A number of sparse CNN accelerator ASICs have been proposed [8, 9, 10]. In this paper we qualitatively assess some of the high level architectural features of SCNN [9] and determine they do not translate well to FPGAs. NullHop [10] also provided FPGA device utilization numbers (they validated their design on an FPGA) which show that they consume 83% of the logic while using only 6.3% of the DSPs and run at a frequency of only 60MHz. The zero-weight skipping architecture of Lu et al. [1] finds a more efficient solution for FPGAs, but their soft logic utilization still limits them to only 45% DSP utilization.

Our approach differs from prior work in how it leverages the hardware of FPGAs. While other works have proposed generic PEs that are used for all layers, our work dedicates hardware to every component of an input neural network. This better leverages the programmable routing and logic resources of FPGAs and enables DSP utilization of 87% on a sparse Resnet-50 model and 89% on a dense MobileNet-V1 model.

III. Architectural Choices

Convolutions are the most computationally expensive operation in a typical CNN. Other works have reduced their computational complexity by applying Winograd’s minimal filtering algorithm [11, 12, 13, 14] or a Discrete Fourier Transform (DFT) [15]. While both of these techniques can reduce the number of multiplications required to implement a convolution, they limit our flexibility to perform other optimizations such as precision reductions, and make it more complicated to support a wide variety of convolution configurations (stride, kernel shape, etc.) [14]. In addition to the limits on flexibility, a recent trend in CNN architecture has been to separate convolutions into depthwise and and pointwise convolutions [16]. Of these two operations, pointwise convolutions are more computationally expensive, but their complexity cannot be reduced with these transforms. As a result, we look only at direct convolution methods.

A. Scatter or Gather Convolution

To perform a direct convolution with sparse weights we have the option to either (a) gather the correct activations for a group of weights and multiply and accumulate them in place as shown in Figure 1a; or (b) multiply all of the weights applicable to a particular input channel with the activations in that input channel and scatter them to a buffer for accumulation, like in [9] and as shown in Figure 1b. While the latter may be an efficient choice for an ASIC, on an FPGA we would like to make use of as many hardened resources as possible. The Stratix 10 DSP blocks include high precision accumulators as well as internal interconnections, called chain-out and chain-in, that allow efficient systolic accumulations within a DSP column, saving power and routing resources. If we were instead to scatter and accumulate into a buffer outside the DSP column we would require additional soft logic to perform the scatter and addition. Additionally, accumulation would require both a read and a write every cycle, and streaming completed data out would require another port. Such a 3-port RAM could be implemented with Stratix 10’s quad port RAMs; however, each RAM would then have a maximum width of only 10 bits, which is not suitable for accumulation. For these reasons we elected to perform a gather-based convolution.

B. Activation Partitioning

After selecting a convolution method we had to determine a data layout and partitioning scheme to process activations in parallel. We qualitatively evaluated three different partitioning schemes:

1) Distribute: A scheme similar to Intel’s DLA [12] that broadcasts activations to PEs from a global buffer and parallelizes multiply accumulate operations across output channels
2) Local Transfer: A scheme similar to SCNN [9] that partitions activations across PEs along the width and height dimensions for a single layer
3) Pipeline: A scheme that partitions activations in the width and height dimensions across all layers simultaneously
1) **Distribute:** Intel’s DLA [12] uses a PE architecture that streams and duplicates input features across multiple processing elements that each compute a different output channel. *Distribute* works very well for a dense accelerator; however, with a sparse accelerator targeting around 85% weight sparsity, only 15% of the activations are used per output channel computation, as illustrated in Figure 2a. Since each PE would only use 15% of the activations broadcast to it, we would either need to have that PE compute multiple output channels serially (which constrains our ability to parallelize the computation) or we would need to increase the activation distribution bandwidth, at a substantial hardware cost, to match the throughput of the DSPs. Additionally, if we parallelize across output channels then we need each processing element to perform its own address calculations, which are more complicated and expensive for a sparse accelerator. From this assessment of the *Distribute* architecture we conclude that a hardware efficient sparse accelerator needs to (a) minimize activation movement since activation re-use is relatively much lower in a sparse accelerator, and (b) share address computations for a large number of output activations computed in parallel.

2) **Local Transfer:** SCNN [9] is a sparse ASIC accelerator that minimizes activation movement by partitioning input activations across tiled PEs in their height and width dimensions for a single layer. In this architecture activations needed by multiple PEs are directly sent to adjacent PEs. While this solves the activation bandwidth issue we had with *Distribute*, this partitioning scheme has a PE under-utilization issue since the activations cannot be split across many PEs when the height and width dimensions of the activations shrink. Figure 2b shows two sets of activations being partitioned across a PE array. The one with large height and width dimensions works well, but the second one with many channels but small height and width dimensions only utilizes 4 PEs.

3) **Pipeline:** The last partitioning we considered was to build a fixed pipeline of layers and pass activations directly between the stages. Figure 2c shows how we can have multiple stages each computing a portion of different layers, which we call a partition, in parallel. Notice that the earlier layers will compute multiple partitions before later stages begin (since they are waiting for data from prior layers). The primary disadvantage of this architecture is that it requires a tremendous amount of memory bandwidth for weights. Each of the *Computing* (see Figure 2c) partitions require the entire set of weights to finish an output line. To reduce weight memory bandwidth requirements other accelerators typically load a set of weights and multiple input images, then use the weights to complete output activations for multiple inputs. By contrast, the *Pipeline* architecture uses all of the weights to complete only a portion of a single input. It then needs to load all of the weights again to complete the next portion of that input.

### C. Comparison

We have summarized our findings about each of the architectures in Table I. A brief summary of the reasons we assigned different values to each architecture is provided below:

- **Activation Locality:** *Distribute* requires that activations all come from and are written back to a global buffer on the chip, while *Local Transfer* transfers them directly to adjacent PEs, and *Pipeline* passes them directly to a small computation unit where they will next be needed.
we minimize activation transfer and duplication by passing
The
Pipeline
Balanced
target 5000 Stratix 10 DSP blocks. The dots show the device
bars show the cycle counts after we have recompiled the network to
parameters optimized for balanced throughput. The
of the convolution stages in our accelerator for ResNet-50.
shows the cycle counts from independent simulations of each
area to balance the throughput of all of the layers. Figure 3
determines the throughput for the entire pipeline we had to
the same throughput. Since the slowest stage in a pipeline
parallelism settings, the layers in ResNet-50 do not all have
activations directly from the output of one computational unit
IV and V. We can also share address computation units
in the neural network with optimizations described in Sections
Pipeline
scores lower here since it requires multiple input
to completely fill the pipeline and take advantage
of all of the multipliers.

None of the architectures scored perfectly in all categories. The
Pipeline architecture performs well across all of our metrics
except weight bandwidth, where it performs very poorly. We
can solve this problem by requiring that all weights fit into
on-chip storage. That may seem like a substantial disadvantage,
but we feel that a combination of (a) the general trend towards
reduced parameters in neural networks [16], (b) our aggressive
parameter reduction through pruning, (c) lower precisions
lowering storage requirements, (d) more on-chip memory on
newer devices, and (e) Microsoft’s approach of connecting
multiple FPGAs together to fit an entire network into on-chip
storage [17], make this requirement a fair price to pay for the
other substantial benefits Pipeline
offers.

With Pipeline
we can tailor modules to every single layer
in the neural network with optimizations described in Sections
IV and V. We can also share address computation units
across a large number of multipliers in each layer. Finally,
we minimize activation transfer and duplication by passing
activations directly from the output of one computational unit
to the input buffer of the next.

IV. NETWORK COMPILER AND TOOL FLOW

When mapped to our convolution unit with the default
parallelism settings, the layers in ResNet-50 do not all have
the same throughput. Since the slowest stage in a pipeline
determines the throughput for the entire pipeline we had to
design parameterized hardware that can make use of additional
area to balance the throughput of all of the layers. Figure 5
shows the cycle counts from independent simulations of each
of the convolution stages in our accelerator for ResNet-50.
The Unbalanced
bars show the cycle counts for stages without
parameters optimized for balanced throughput. The
Balanced
bars show the cycles after we have recompiled the network to
target 5000 Stratix 10 DSP blocks. The dots show the device
utilization for the Balanced
accelerator broken down into the
fraction of total device ALMs, registers, M20Ks, and DSPs.
Generating these parameters along with the hardware itself
and the memory initialization files for the hardware manually
would be tedious so we elected to automate this process.

Others have built tools that generate neural network accelerators
for FPGAs. Moreau et al. [18] built a platform independent
Intermediate Representation (IR) to which they compile graphs
from a number of machine learning frameworks. Noronha et al.
[19] created their own LLVM passes to translate LLVM IR
they obtained from TensorFlow’s Accelerated Linear Algebra
(XLA) back end to LLVM IR that the open source High
Level Synthesis (HLS) tool LegUp can accept and convert
into Verilog. Sharma et al. [20] built a tool that translates a
Caffe protobuf description of a neural network into a series of
instructions for their own accelerator, then builds an accelerator
tailored to the instructions used by the input network and a
particular FPGA. Chen et al. [21] built a tool that maps from
Caffe protos to HLS templates and builds a full system that
can have parts of a network run in software. While these tools
all have something to offer, we elected to implement our own
solution.

Like Sharma et al. [20] we wanted to write our own highly
optimized Register Transfer Level (RTL) description of a select
set of neural network operations to target the highest possible
performance; however, our layer-pipelined architecture is too
dissimilar from theirs to reuse any of their optimized hardware.
The IR from Moreau et al. [18] would have allowed HPIPE
to accept networks from a variety of frameworks; however,
mapping from IR to our hardware would have been challenging
since we would have needed to infer the type of operation
from a control flow graph. Importing TensorFlow graphs gives
us the structure of a wide variety of different neural networks
at a level of abstraction that is appropriate for our hardware.

Our compiler accepts a TensorFlow graph, a DSP target
that provides it with a coarse estimate of the resources on the

| TABLE I | COMPARISON OF ACTIVATION DISTRIBUTION/PARTITIONING ARCHITECTURES |
|---------|---------------------------------------------------------------|
| Distribution | Activation Locality | Address Computation | Shape Flexibility | Weight Bandwidth | Latency |
| Distribute | Poor | Good | Good | Excellent | Excellent |
| Local Transfer | Good | Poor | Excellent | Poor | Excellent |
| Pipeline | Excellent | Excellent | Poor | Excellent |

Fig. 3. Comparison of Individual Layer Latency Before and After Balancing,
and Resource Utilization per Layer as Percentages of the Total Chip Resources
target device, and a precision annotations file that allows a user to specify a particular fixed point format independently for each of the operations in the graph. [22] and [23] found that there is no single optimal precision for neural network acceleration, so the ability to tune the precision of activations and weights independently for each operation has the potential for large efficiency gains. Figure 4 shows the overall flow of our compiler from a user perspective. The output is a directory containing a series of verilog files that implement the input neural network, and a number of memory initialization files that contain compressed weights and auxiliary data that are described in more detail in section V.

To prepare a TensorFlow graph to be built into an HPIPE accelerator our compiler first attempts to merge all of the batch normalization operations into convolution and bias operations. While batch normalization must run as an independent operation during training, during inference it simplifies to a multiplication by a constant and an addition with a constant. Folding batch normalizations into other operations is commonly performed to prepare neural networks for inference, and a utility for performing this operation is included in TensorFlow r1.11; however, this utility only looks to see if the operation can be merged into its immediate neighbours. We run a series of graph transformations that break batch normalizations into an addition and a multiplication and then swap the execution order of certain operations so that they can be merged with operations that were not initially neighbours. After these transformations are complete we dump a new TensorFlow graphdef that can be run through TensorFlow to validate that the transformations did not impact the accuracy of the network.

We allow our compiler to swap batch normalizations with max pool and padding operations, as well as move the multiplication component of the batch normalization after ReLUs. We have run these optimizations on the official TensorFlow ResNet-50 model and found they allowed the compiler to successfully fold all batch normalizations into other operations with no impact to either top 1 or top 5 accuracy on ImageNet [24].

After merging batch normalizations we merge padding operations into pooling or convolution operations and build a balanced plan for the target DSP count. To enable balanced throughput our convolution module has an \texttt{n\_channel\_splits} parameter that allows us to unroll the computation of output activations along the input channel dimension. With an analytic model that estimates the throughput of a convolution operation, given this parameter, we can loop over the slowest operations and increment \texttt{n\_channel\_splits} until we hit the DSP Target.

Initially our model assumed a linear relationship between \texttt{n\_channel\_splits} and the throughput of a module. This proved to be a poor assumption for some layers with a high degree of sparsity due to the distribution of the zeros within that layer. We rectified this by computing the actual weight partitioning and padding that a later stage of the compiler performs, which improved our estimates to within 1% of the actual throughput and improved the throughput of the accelerator by 23%. As you can see in Figure 3, our algorithm is able to balance the stages of our 85% sparse ResNet-50 model such that nearly all of the layers have throughput within 10% of each other, which results in a throughput improvement of 30x versus the unbalanced design. The algorithm runtime is only a few seconds.

Once we have come as close to the DSP target as possible without exceeding it, we pass the plan with the computed parameters to our accelerator generator. This generator iterates over all of the nodes in the optimized TensorFlow graph, instantiating modules for every node with the parameters contained in the plan, then iterates over all of the edges and connects the modules together. Finally, it dumps a directory containing verilog and memory initialization files that implement the graph for the target FPGA.

V. DETAILED IMPLEMENTATION

We have implemented and verified modules that can execute the TensorFlow Placeholder, Conv2D, DepthwiseConv2D, MatMul, BiasAdd, MaxPool, Relu, Relu6, Add, and Mean operations. As described in Section V, we have also implemented a series of graph transformations that allow us to merge all of the BatchNormalization operations in the official TensorFlow ResNet-50 V1 (r1.11), MobileNet-V1, and MobileNet-V2 models into Conv2D and BiasAdd operations. Our implementations of MaxPool, Conv2D, and DepthwiseConv2D can support any kernel shape and stride and are further parameterized to allow our network compiler to allocate additional device resources to layers that have higher computational requirements. This section first gives an overview of the the general data flow through the circuit, then it details the internal implementation of the convolution block and provides an overview of the other blocks.

A. Data Flow

Figure 5 shows the first 10 TensorFlow operations from our optimized 85% weight sparse ResNet-50 V1 model. Each of these operations is implemented as a module instantiation, and the arrows between them are pipelined wires connecting producers to consumers (for example, in Figure 5 the Placeholder is a producer for the Conv2D it is connected to). Some of the operations buffer the input data, while others simply
process it as it comes in and immediately write it out. The nodes that have buffers have a limited amount of storage space, so they export a coarse-grained back-pressure signal to all of their producers indicating if there is space in the buffer. The nodes that do not buffer input simply pass the signal from their consumers to their producers.

Each stage in HPIPE processes one line of output data at a time. We call this an output channel group and it has a shape of $1 \times W \times C_o$, where $W$ is the output width and $C_o$ is the number of output channels. Additionally, all modules contain both a controller and a data path. The controllers typically compute addresses, load weights and biases, and communicate with their producers and consumers.

### B. Convolution and Matrix Vector Multiplication

Figure 6 shows a block diagram of our convolution module (note that we have omitted all of the registers not essential to the functionality of the circuit) with $n\_channel\_splits$ set to 4. We use this module to implement both convolutions and Matrix-Vector multiplications (a convolution with a kernel shape of $1 \times 1 \times c_i \times c_o$ with an input shape of $1 \times 1 \times c_i$ is the same as a matrix-vector multiplication of shape $c_o \times c_i$). The function of each of the blocks is as follows:

- **Pad Muxes:** For layers with vertical padding the Input Buffer Controller will write zeros into the first $P_t$ lines of the Input Activation Buffers prior to deasserting its coarse backpressure signal (where $P_t$ is the top padding), and do the same for the bottom padding before a new input can be processed.
- **Input Activation Buffers:** Are a series of ring buffers into which the input activations are packed.
- **Weight Buffer:** Stores compressed weights, runlengths that encode the $y$ and $z$ position of a weight as an offset from the position of the previous weight, and x-indices that indicate the weight’s $x$ position.
- **Input Buffer Controllers:**
  - Control when to write padding.
  - Decode runlengths from the weight buffer into addresses from which activations are read from the Input Activation Buffers.
  - Store the amount of space remaining in the Input Activation Buffers and assert coarse_backpressure if there is no longer enough space to write a full line (all channels).
- **X Muxes:** One $k_w$-to-1 mux for each multiplier that allows selection of activations from different $x$ locations.
- **DPS:** The circles with Xs are multipliers, and each DSP contains two multipliers, plus two adders (circles with +s) and either an accumulation register or a delay register. The dotted red lines in Figure 6 from the delay register in one DSP block to the adder in the next DSP block indicates chaining of $n\_channel\_splits/2$ DSP blocks together.
- **Accum/Valid Controller:** Has a memory containing the number of weight lines per output channel that it loads into a down counter that stops accumulation and asserts the new_oc signals whenever it reaches zero.

At a high level the operation of the block is as follows:
1. Data enters from producers through data lines 1 to $W$, and gets written whenever the new_oc signal is asserted.
2. Every time the input new_oc is asserted the address to which the input activations are written is incremented.
3. Once the buffer contains $k_h$ full input lines (where $k_h$ is the kernel height for the layer), it begins to read from the weight buffer.
4. The Input Buffer Controller begins to decode runlengths into addresses and distributes them to the input activation buffers.
5. The activations loaded by the Input Activation Buffer are shifted by the X Muxes by the amount specified by the corresponding X Index from the Weight Buffer.
6. The shifted activations are multiplied with the corresponding weight and accumulated.

At the top of Figure 6 you can see the $n\_channel\_splits$ parameter that we use to configure the throughput of the convolution block. As shown in the diagram $n\_channel\_splits$ is the number of Weight Buffers, Input Buffer Controllers, Input Activation Buffers, and X Muxes we instantiate. It also controls the number of multipliers; however, it does not control the number of accumulators. As we increment $n\_channel\_splits$ and add additional multipliers, we use the chain-out from the DSP to string multiple DSPs together, using only the last one in the chain to perform the accumulation. Since each additional DSP in the chain introduces one cycle of delay, we shift the Weights, X Indices, and Runlengths for every second channel.
We compare to three sets of related accelerators. First, we evaluate our throughput on ResNet-50, a popular and high accuracy but compute-intensive CNN. The highest performance GPU and FPGA implementations of ResNet-50 are dense, so we compare to these, but our implementation leverages sparsity and achieves higher throughput at a modest accuracy cost. Second, we compare to a prior sparse-CNN FPGA accelerator and show that we can exploit all the device DSPs, while their higher logic utilization limits the number of DSPs they can use. Third, we compare throughput vs. a GPU and a prior FPGA accelerator on the compute-efficient and dense MobileNet CNNs (V1 vs. a GPU and V2 vs. the prior FPGA accelerator). This comparison shows we outperform these accelerators even without leveraging sparsity and while running at 2x the precision.

A. Highest Throughput Accelerators

On ResNet-50 we evaluate against the highest performance machine learning optimized GPU (an NVIDIA V100 with up to 260 trillion operations per second of 8-bit matrix multiply performance) using the optimized numbers reported by NVIDIA [25], an academic performance model of Intel’s DLA [12] (we refer to this as DLA-Like), and Microsoft’s Brainwave [17]. The only available numbers for DLA-Like and Brainwave are from Arria 10 (A10) FPGAs, so we also provide scaled numbers for Stratix 10 (S10). For DLA-Like we scaled them by a compounded 3.4x for the ~2.3x increase in 18×18 multipliers and a 1.5x improvement in frequency. For Brainwave we use the Peak TFLOPs numbers they provide for S10 and A10 to scale their A10 throughput and latency numbers. Figure 8 shows the throughput versus latency of each of these accelerators. Since the GPU has throughput improvements when it is run with larger mini-batches we have shown the latency throughput trade-off curve and annotated the batch size. HPIPE has nearly 4x the throughput of the V100 at a batch size of 1. Moving up to a batch size of 8 the V100 has 72% of the throughput, but with 2.2x the latency, and the requirement that it must batch 8 images. Similarly, HPIPE outperforms Brainwave and DLA-Like by 1.6x and 7.4x, respectively, even when we compare to scaled numbers that assume throughput scales perfectly with peak TFLOPs.

Each of the devices are running variants of ResNet-50; however, there are slight differences in each of the models summarized in Table III. We collected our accuracy by running the 50,000 image ImageNet validation set on actual hardware, using PCIe to transfer data to and from the accelerator. Our top-1 and top-5 accuracies of 71.9% and 90.8% match the input TensorFlow model when it is run on a GPU. This is lower than typical ResNet-50 accuracy of top-1 and top-5 of 76.0% and 93.0% [26], respectively; however, we believe we could increase this with a different pruning technique that does not restrict us to the same sparsity in each layer.

B. Sparse CNN on FPGA

Lu et al. [1] do not provide latency or throughput numbers for their accelerator, so we can only compare resource utilization. Table V shows that our frequency is nearly 3x theirs, and our DSP utilization is nearly double theirs. They use a smaller FPGA, but we expect that if they scaled up to a larger FPGA, their DSP-to-logic utilization ratio would remain roughly the same and their accelerator would still be unable to take advantage of all of the available multipliers.

C. Dense MobileNet-V1 and MobileNet-V2

Table V shows a comparison of HPIPE to the V100 GPU running MobileNet-V1 and a comparison of HPIPE to the FPGA accelerator from Wu et al. [27] running MobileNet-V2. NVIDIA does not report accuracy for their implementation of MobileNet-V1. In the comparison against the GPU we are behind in latency by 0.43ms, but we demonstrate higher throughput despite running at 2x the precision and not leveraging the sparse acceleration capabilities of our accelerator.

While the V100 and S10 2800 are both the largest monolithic chips sold by NVIDIA and Intel, the Zynq ZU9 is not, so we must normalize the results in some way to compare to Wu et al. [27]. We cannot simply divide throughput by DSP count.
We believe this performance derives from a combination of a) which we compare, though the two MobileNet accelerators have
we ran out of input channels to unroll. In the future we could
version of HPIPE only unrolls the input channel dimension and
ran all of our experiments with a 16-bit fixed point precision.

In this paper we have demonstrated that a gather-based
layer-pipelined approach to CNN acceleration can leverage
sparsity without the added hardware cost from prior works. This approach enables inference throughput at a batch size of 1
that is 4x higher than the fastest GPU for machine learning on
a large but sparse CNN. On smaller and more efficient dense
models that do not leverage our 0-weight skipping we still
achieve higher throughput than the GPU and another FPGA
accelerator while running at twice the precision. Our variable
precision support and throughput balancing algorithms will
allow future accelerators based on this architecture to prune
weights only from layers where accuracy does not suffer, and
reduce the precision in particular layers where higher precision
is less important. Looking towards future FPGA architectures
with DSP support for lower precision multipliers, these features
could provide further performance improvements per area of
2x or more.

VIII. CONCLUSION

In this paper we have demonstrated that a gather-based
layer-pipelined approach to CNN acceleration can leverage
sparsity without the added hardware cost from prior works. This approach enables inference throughput at a batch size of 1
that is 4x higher than the fastest GPU for machine learning on
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with DSP support for lower precision multipliers, these features
could provide further performance improvements per area of
2x or more.

TABLE II
RESOURCE COUNTS AND UTILIZATION FOR HPIPE ON STRATIX 10 2800

| CNN        | ALMs Needed | ALMs for Memory | ALM Registers | Hyper-Registers | M20Ks   | DSPs | Frequency |
|------------|-------------|-----------------|---------------|-----------------|---------|------|-----------|
| ResNet-50  | 591,882 (63%)| 122,850 (26%)   | 1,417,297 (17%)| 372,592         | 11,278 | 5,022| 580 MHz  |
| MobileNet-V1 | 371,500 (40%)| 110,950 (24%)   | 874,713 (23%)  | 147,671         | 4,283  | 5,133| 430 MHz  |
| MobileNet-V2 | 290,486 (31%)| 41,550 (9%)     | 766,604 (21%)  | 105,810         | 4,512  | 2,964| 390 MHz  |

TABLE III
PERFORMANCE OPTIMIZATIONS AND IMPACT ON ACCURACY – RESNET-50

| CNN        | V100 [25] | Brainwave [17] | HPIPE | DLA-Like |
|------------|-----------|----------------|-------|----------|
| Sparsity   | 0%        | 0%             | 85%   | 0%       |
| Winograd   | No        | No             | No    | Yes      |
| Precision  | 8-Bit     | 11-Bit         | 16-Bit| 16-Bit   |
| Format     | Fixed     | Block Float    | Fixed | Fixed    |
| Top-1 Accuracy | 74.93% | ~ 76%†          | 71.9% | –        |

† Fowers et al. [17] provides only a statement that accuracy degradation is negligible

either, because one Xilinx Ultrascale+ DSP slice is a single
27x18 multiplier while the Intel S10 DSP block is two 18x18
multipliers. To ensure our comparison is rigorous we will divide
our throughput by the number of 18x18 multipliers we use and
divide their throughput by the number of 27x18 multipliers they
use (despite the 27x18 multipliers taking more area). Doing
this yields throughput per multiplier a 1.95x higher for HPIPE
than Wu et al. [27], even though they use half our precision.

We believe this performance derives from a combination of a)
our higher frequency of 390MHz vs. 333MHz and b) under-
utilization of their DSP blocks due to imperfect mapping of
some layers onto their PEs.

Unlike MobileNet-V1 and ResNet-50, for MobileNet-V2 we were
unable to fully utilize the S10 2800 DSPs. The current
version of HPIPE only unrolls the input channel dimension and
we ran out of input channels to unroll. In the future we could
update HPIPE to unroll output channels to extract additional
parallelism. As it is, our DSP utilization is still higher than
our soft logic or M20K utilization, and we could fit on an S10
1650 and utilize 94% of the DSPs.
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