Simplifying heterogeneous migration between x86 and ARM machines

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Abstract
Heterogeneous computing is the strategy of deploying multiple types of processing elements within a single workflow, and allowing each to perform the tasks to which is best suited. To fully harness the power of heterogeneity, we want to be able to dynamically schedule portions of the code and migrate processes at runtime between the architectures. Also, migration includes transforming the execution state of the process, which induces a significant overhead that offsets the benefits of migrating in the first place. The goal of my PhD is to work on techniques that allow applications to run on heterogeneous cores under a shared programming model, and to tackle the generic problem of creating a uniform address space between processes running on these highly diverse systems. This would greatly simplify the migration process. We will start by examining a common stack layout between x86 and ARM binaries, focusing on these two widely spread architectures, and later we will try to generalize to other more diverse execution environments. On top of that, the performance and energy efficiency of the above effort compared to current approaches will be benchmarked.

CCSConcepts: • Computer systems organization → Heterogeneous (hybrid) systems; • Software and its engineering → Compilers.

Keywords: Heterogeneous Systems, Migration, Compilers

1 Introduction
In both industry and academia there is the belief that in order to achieve higher performance, energy efficiency and lower cost, attention must be given to specialized hardware [11]. Combining this special-purpose hardware (e.g. GPUs, TPUs, accelerators) with general-purpose hardware (e.g. CPUs), and reconfigurable integrated circuits (e.g. FPGAs), leads to heterogeneous architectures, allowing mixed workloads to be executed in the most suitable hardware [1]. The different processing units may share the same ISA, like in the big.LITTLE architecture [10], or even employ heterogeneous-ISAs. A heterogeneous-ISA approach yields even more diversity to exploit, like different code density, register depth and width or decode instruction complexity [18]. For example, smartNIC and smartSSD processors are increasingly adopted in the data center [12, 15], and they are usually paired with x86 host processors, which could lead to large-scale live migration between architectures.

Whatever the type of heterogeneity supported, a shared memory programming (SMP) model is usually the most convenient solution for the programmer. Moreover, bus standards like OpenCAPI [7] have emerged, aiming to provide improved coherency and synchronization in heterogeneous systems, favoring SMP programming models. Therefore, we will focus on the setting of SMP models in heterogeneous-ISA environments.

An approach like Popcorn [3], allows applications to migrate during runtime at equivalence points of computation in the program [17], but requires first the stack transformation of the program between architectures. This creates an overhead to the migration, which grows linearly with the number of stack frames, and the number of variables, but also poses additional engineering effort for creating the transformation toolchain. Also, the above technique generates two fat binaries, with some metadata necessary for migration, which are more difficult to deploy in embedded systems. In order to harness the power of various heterogeneous techniques, it is necessary to have efficient process migration at runtime, otherwise the migration costs will offset the benefits of heterogeneity.

One effective way to exploit heterogeneity would be to circumvent the stack transformation at runtime by imposing a uniform stack layout between the target architectures. The focus currently is between the x86-64 [8] and ARMv8 [16] target ISAs. The first fundamental part of this idea, is to keep the Application Binary Interface (ABI) the same between the architectures. On top of that, we need to explore the effect of various optimizations (target-dependent or not) that affect spills and refills in memory. To this end, we modify the LLVM’s backend infrastructure [14], controlling the emitted assembly instructions, and tune the optimization flags accordingly.

The first difference from existing works like bit.LITTLE, is that we focus on heterogeneous-ISA architectures, instead of homogeneous ones. In the context of ISA heterogeneity, some of the current approaches require the transformation at runtime of the stack from one architecture to another, in order to migrate a thread, like in the case of Popcorn software [4] or Venkat’s work [5]. We will try to avoid this transformation. Ultimately, our goal would be to extend this work to multiple architectures, instead of relying solely on the 64-bit versions of x86 and ARM, or on other commonly used combinations, as described in Section 5.
2 Overview of the proposed work

Our initial focus is to find ways to overcome the stack transformation overhead at runtime. The way an application interacts with its stack, doing load and store instructions, is determined by various factors, such as the ABI, the optimizations done at compile-time and the target-dependent code generation.

The first step was to modify LLVM’s backend for the x86-64 and Aarch64 targets. First of all, the number of registers available in the architecture (register depth) affects the register pressure, i.e. the number of simultaneously live variables at an instruction) and, consequently, the frequency of spills and refills in the stack [6]. Therefore, we modified the architecture backend, to get the same register depth. We have, also, mapped the various registers one-to-one, taking into consideration their occasional target specific functionality, e.g. the platform register in ARMv8. Moreover, the procedure calling convention dictates the number of registers that will be spilled at the boundary of the stack frame as arguments. In the same way, it enumerates the callee-saved registers, which will also be saved in the stack frame in case they are to be modified. Hence, we implemented the same calling conventions for both targets.

However, even if these differences are completely resolved, we still have to observe the dynamic behaviour of the executed application, and its interaction with the stack. Ideally, we aim to generalize our solution to other architectures, with different register depths, pointer sizes and other architecture specifics.

3 Preliminary results

A main concern is to ensure that forcing some characteristics on an architecture does not impact performance a lot during program execution, given that we are missing some architecture-specific optimizations. For instance, we have removed 15 of the general purpose registers (GPRs) of the Aarch64 LLVM target, which had 32 GPRs, to match the 17 GPRs of the x86-64 architecture (including the stack pointer). So far, we have run experiments only on integer benchmarks, consuming more stack area.

In order to address architectures with smaller number of registers, we may have to emulate some registers by consuming more stack area.

Finally, we will check experimentally that implementing a similar address space does not lead to performance issues, for execution on only one architecture.

4 Work to be done

Now we will describe the necessary changes to the LLVM backends of the targets. Where a register in an architecture does not have a reciprocal to the other architecture (e.g. there is no platform register in x86-64), we plan to either emulate the same behaviour, or ignore it if it has no important role to our prototype.

In addition, there are some fundamental differences between our targets that lead to stack mismatch during execution. For example, the x86 architecture is CISC and includes operations between the memory and the registers. On the contrary, the ARM architecture is RISC and employs the load-compute-store philosophy, which creates additional register pressure, especially now that we have reduced the number of ARMv8 registers to match the number of x86-64 registers. Therefore, we need to empirically identify stack layout differences at runtime and pinpoint the causes of these differences.

Following the above, we may have to mitigate those differences, either at the intermediate representation (IR) level (e.g. with a flag like mem2reg, to reduce unnecessary loads), or at a target-dependent level. If tuning the flags is not sufficient, we may again need to modify the code generation of the respective backend, to emulate the desired behaviour.

After this work has matured enough, we will try to generalize our approach by analyzing the fundamental properties of an architecture that shape its stack at runtime. Consequently, we will examine the feasibility of an architecture design and/or a specification of a more universal ABI, that allows us to expand to more diverse targets, like CPU/DPU systems. In order to address architectures with smaller number of registers, we may have to emulate some registers by consuming more stack area.

5 Related Work

Having a unified address space in heterogeneous environments, is not a new idea. AMD started originally the Heterogeneous System Architecture (HSA) framework, supporting a single address space accessible to both CPU and GPU, through virtual address translation [13]. Still, it is the programmer’s responsibility to identify and schedule the workloads statically. In the Popcorn compiler toolchain and state transformation runtime [3], a separate binary is created for each architecture, which is augmented with metadata by the middle- and backend LLVM passes, necessary for the state transformation. When a migration occurs, the runtime converts all function activations from the source ISA format to the destination ISA format [17]. In another case, Venkat[18] and DeVuyst [9] use dynamic binary translation for one fat binary, until the binary reaches a migration point and state transformation takes
place. These last efforts also included smaller register widths, like 32 bits, but we foresee that architectures with at least 64 bits will dominate, hence we focus on them for now.

6 Conclusion
This paper presents the outline of our proposed approach, for simplifying heterogeneous ISA migration. Our plan is to come up with solutions that create a uniform address space between the processes, whereas eliminating the overhead of state transformation at runtime. Preliminary results indicate that enforcing a similar stack layout, through an identical ABI between x86-64 and Aarch64 targets, does not deteriorate performance significantly, while it paves the way for actually creating identical stack layouts. An ultimate goal would be to extend this work, in order to ease portability of migration to various targets, other than x86-64 and ARMv8.

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