Cyber-physical systems (CPS) are engineered systems that are built from, and depend upon, the seamless integration of computational algorithms and physical components. Advances in CPS will enable capability, adaptability, scalability, resiliency, safety, security, and usability that will far exceed the simple embedded systems of today. Tremendous progress has been made in advancing CPS technology over the past years. At the same time, the system reliability and quality control emerges as a major challenge in CPS development. Undiscovered design problems could lead to severe safety issues and significant financial loss.

This Special Issue focuses on the state-of-the-art research results on architecture and systems to realise smart, efficient, reliable, and high-quality CPS. The issue contains four papers presented at the International Symposium on Quality Electronic Design (ISQED) conference in 2017, representing various CPS and different development requirements, including IoT applications, wearable health monitoring, object localisation in indoor environments, and terahertz band on-chip communication.

Challenges and frameworks for developing IoT applications

The paper ‘Developing IoT applications: challenges and frameworks’ by Itorobong S. Udoh and Gerald Kotonya presents a comprehensive review and a comparative analysis of existing IoT application development frameworks and toolkits, illustrating their strengths and weaknesses. As IoT systems involve a wide range of hardware and software components on a variety of communication and distributed system technologies, the study will assist in finding the most appropriate IoT application development paradigm for the desired IoT application. The work also highlights future research directions to improve existing and future frameworks and toolkits for IoT applications.

Energy efficient wearable health monitoring

‘Biopotential acquisition unit for energy efficient wearable health monitoring’ by Wazir Singh and Sujay Deb is aimed at wearable health monitoring system development, where energy consumption is a key concern. The work particularly focuses on transmitter optimisation and presents a compressive sensing-based biopotential acquisition unit to reduce the overhead of wirelessly transmitting and storing data. The implementation in 65 nm complementary metal–oxide–semiconductor (CMOS) technology shows a high common mode rejection ratio (CMRR) and low noise.

Indoor positioning systems

‘A machine learning based system for multi-sensor 3D localisation of stationary objects’ by Everton L. Berz, Deivid A. Tesch and Fabiano P. Hessel investigates the localisation of objects and people in indoor environments. More specifically, the work proposes a multi-sensor indoor positioning system (IPS) able to estimate the 3D location of stationary objects using off-the-shelf equipment. By using radio-frequency identification (RFID) technology, machine learning models and artificial neural networks are proposed to enhance RFID localisation. The system has been implemented and evaluated using real experiments.

High-frequency and low-energy plasmonic interconnects

‘Terahertz band communication using plasma wave propagation in multilayer graphene heterostructures’ by S. Rakheja focuses on multilayer graphene as the building block to implement high-frequency and low-energy plasmonic interconnects for on-chip signalling in next-generation systems. Two specific plasmonic interconnect geometries are analysed: single waveguide (SWG) and parallel-plate waveguide (PPWG). Analytical models of energy-per-bit and bandwidth density for both SWG and PPWG interconnects were developed and used to quantify optimal interconnect length scales for which plasmonic interconnects provide lower energy and higher bandwidth.

Conclusion

The papers selected for this Special Issue present a large diversity of cyber-physical systems that involve a wide range of hardware and software components and requires a variety of communication and distributed system technologies. Nevertheless, the system reliability and quality control emerges as a major challenge in CPS development, and these papers show the approaches at circuit, architecture, and system levels to meet the emerged challenges.

Guest Editor Biographies

Hai ‘Helen’ Li is currently the Clare Boothe Luce Associate Professor of Electrical and Computer Engineering Department at Duke University USA. She works on hardware/software co-design for accelerating machine learning, brain-inspired computing systems, and memory architecture and optimisation. She has authored or co-authored more than 200 technical papers in these areas and has written a book published by CRC Press. Dr Li is a recipient of the NSF CAREER Award (2012), the DARPA Young Faculty Award (2013), TUM-IAS Hans Fisher Fellowship from Germany (2017) and seven best paper awards. Dr Li is a senior member of IEEE and a distinguished member of ACM, a distinguished speaker of ACM (2017–2020), and a distinguished lecture of IEEE CAS society (2018–2019).

Brian Cline is a Principal Research Engineer in the Devices, Circuits, and Systems research group at Arm, based in Austin, USA. His research interests and responsibilities include...
the circuits- and system-level design impact of emerging logic devices (primarily post-CMOS), memory devices, next generation lithography (e.g., EUV, DSA), and next generation integration strategies (e.g., fine-grained 3D bonding, monolithic/sequential 3D). Dr Cline also has interests in Electronic Design Automation (EDA) tools and methodologies and Design-Technology Co-optimisation (DTCO), mainly with respect to high-speed, power-efficient digital logic design. Brian received his B.S. degree in electrical engineering from the University of Texas, Austin, USA, in 2004, and his M.S. and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, USA, in 2006 and 2010, respectively. From 2006 to 2010, he was a Graduate Fellow with Semiconductor Research Corporation (SRC). Dr Cline was recently chosen as one of the recipients of the SRC Mahboob Khan Outstanding Industry Liaison award, awarded to “individuals who have made significant contributions to the SRC community in their roles as liaisons.” Brian has published more than 25 papers, including a number of best paper award nominees, invited papers, and plenary sessions.

Gang Qu received his M.S. and Ph.D. degrees in Computer Science from University of California at Los Angeles (UCLA), USA, in 1998 and 2000, respectively. Previously, he had studied Mathematics at the University of Science and Technology of China (USTC) and the University of Oklahoma USA. He joined the Department of Electrical and Computer Engineering in the University of Maryland at College Park (UM, USA) in 2000. He is a joint associate professor at UMIACS and an affiliate associate professor at the Computer Science Department. Dr Qu is a member of IEEE and ACM. He is also an individual member of the Virtual Socket Interface (VSI) Alliance. His research interests include VLSI intellectual property reuse and protection, low power system design, computer-aided synthesis, artificial intelligence, and wireless sensor networks. He has published more than 60 journal and conference papers in these areas and co-authored the first book in VLSI Design intellectual property protection. He won the ACM SIGMOBILE MobiCom best student paper award in 2001. He has served on the technical program committee for many conferences and also served as the general co-chair for the 16th ACM Great Lakes Symposium on VLSI (GLSVLSI 2006).