An eight-switch five-level inverter with zero leakage current

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Abstract
This paper examines a multilevel transformer-less grid-tied inverter topology is proposed for PV applications. Nowadays, transformer-less inverters are more desirable due to their small filter size, cheaper and higher efficiency. However, the removal of transformer results in the existence of leakage current due to absence of galvanic isolation. The flow of leakage current is the cause of personal safety and deteriorating power quality. A transformer-less inverter topology is proposed which is able to solve the leakage current issue. Besides, it has the ability to generate the boosted voltage without the need of magnetic component or boosting circuit. It works on the principle of flying/switched capacitor which are able to naturally balance the voltage. Hence, it does not have the limitation of modulation index and no need of complex control scheme to balance or regulate the voltage across an auxiliary capacitor. The performance of the proposed topology is verified by implementing a laboratory prototype which validates the operation and performance of the proposed topology. Results depicting the output voltage, load current and voltage across the auxiliary capacitor are presented for various operating conditions. Moreover, a comprehensive comparison is done, in terms of component count, level and boosting ability of output voltage with leakage current condition.

1 | INTRODUCTION

Rapid increase in electricity demand has been a challenge to the costly oil, climate changes and depleting fossil fuel. As a result, to fulfill the electricity demand generation from renewable energy sources is continuously increasing. Among all renewable energies photovoltaic (PV) production have exponential hike in industrial and residential application. In the grid-tied PV systems power electronic converters are a very important part for the integration of PV sources into the power grid. These converters are generally classified as galvanic-isolated and non-isolated system. Transformers are connected on the ac or dc side of the inverter which provides the galvanic isolation. AC side transformers have low frequency, hence they are big in size, lower efficiency, high in cost and tough to install. Whereas, high frequency transformers results in smaller in size and cheaper while energy conversion stages (dc-dc and dc-ac) are more which leads to decreased efficiency and increased complexity of the system as compared to ac side transformer. Therefore, in renewable energy application transformer-less grid-tied inverters are more beneficial [1, 2] due to their small size, low cost and higher efficiency. Absence of transformer results leads to the flow of leakage current between PV-to-grid [3–5]. The leakage current injects the harmonics in the grid current, causes personal safety problems, electromagnetic interference (EMI) and increased system losses. Hence it is necessary to eliminate the leakage current and lot of transformer-less inverter topologies have been proposed previously. By maintaining a constant common mode (CM) voltage leakage current can be minimized.

In order to reduce a common mode voltage various proposed topologies are based on the conventional H-bridge inverter, such as H-5 [6, 7], H-6 [8], HERIC inverters families [9] etc. As shown in Figure 1(a), H-5 inverter has one additional which is connected between dc-bus and h-bridge. Whereas, H-6 inverter has two extra switches which are inserted in the middle of dc-bus terminals and bridge arms, as depicted in Figure 1(b). HERIC based topologies have freewheeling branch which is inserted between h-bridge output terminal and load side filters,
as depicted in Figure 1(c). These additional switches and branches are inserted for isolating the path from PV array to utility grid during freewheeling mode. For such topologies, it is very difficult to reduce the leakage current due to parasitic capacitance of switches. In addition, these inverters need two filter inductors results in increased size and expensive [10]. Moreover, conduction losses are high due to more than three conducting switches in series during active mode [11]. Another H-Bridge based five-level inverter proposed in [12], it consists of eight switches, two flying capacitors, one diode and two filter inductors. Additionally, one five-level topology is presented in [13], which made of six switches, two flying capacitors and two filter inductors. Again these topologies are not able to generate the boosted voltage.

Other topologies are based on the half-bridge, where middle-point of the dc-bus tied with utility neutral, as shown in Figure 2(a) [14]. These topologies reduces the leakage current with single filter inductor while the required input voltage is twice of the generated output [15]. Another variant namely active NPC (ANPC) inverter is the popular version of NPC where in the passive diodes are substituted with the active switches [16]. Hence, additional boosting circuit is required to meet the grid voltage requirement. Which results in extra power conversion stage, hence efficiency is decreased and increased cost [16]. Additionally, efforts are made to integrate the boosting feature in to the inverter without much consideration to the issue of ground leakage current [17, 18].

Recently, a popular is proposed in the literature which are common ground type (CGT) inverter topologies [19] and are shown in Figure 2. As compared to other available inverter topologies, CGT based inverter is able to eliminate the leakage current completely due to short-circuiting of PV-to-ground parasitic capacitance. Karschny transformer-less inverter is also CGT based, which consists of five power semi-conductor switches, two diodes, one storage and one filter inductors with one capacitor. The circuit diagram of karschny transformer-less inverter, as depicted in Figure 2(b) [20] is very complicated and needs sophisticated control structure and also it is not able to deliver the reactive power to the power grid. The virtual dc-bus inverter is based on the concept of utilizing the intermediate charged capacitor for the generation of negative voltage levels. A switched-capacitor is used for the creation of virtual dc-bus. The achievable peak output voltage is the same as input dc-link voltage like in the case of the conventional full-bridge inverter. The virtual dc-bus inverter, as shown in Figure 2(c) [21] consists of five switches, two capacitors, single filter inductors and reduced/zero ground leakage current. Another CGT based topology is presented in [22], which suppresses the leakage current completely while it is incapable to generate the boosted voltage. Another, five-level inverter is presented in [23] based on CGT, reduces the count of components and eliminates the leakage current but again is incapable to generate the boosted output voltage. Further, CGT based single phase inverter topology is proposed in [24] which works on the principle of flying capacitor. It is constructed with four switches, one diode, one flying capacitor and filter inductor is also one. The beneficial feature of this topology is that during the power transfer mode, the maximum number of on state switches is 2, leads to improved efficiency. The above discussed topologies are able to eliminate the leakage current but incapable to generate a boosted output voltage. Other concerns is, auxiliary capacitors charging and discharging operation and balanced voltage at a desired level. In practical applications, it is desirous to generate multilevel voltage in order to reduce the filter size, reduce voltage stress and
increase efficiency. Hence, with the increased number of voltage levels count of auxiliary capacitors is also increases which leads to more number of required sensor and circuit becomes costly. Another CGT based five-level inverter topology presented in [25], yields in zero leakage current. It consists of six switches, one diode, two flying capacitor and a single inductor with no voltage boosting ability. Also, it requires voltage and current sensors which leads to increased cost. Other CGT based five-level topology in [26], consists of nine switches, two flying capacitor and a single inductor. Recently, boosting inverter topologies are proposed in [27, 28]. Despite many efforts toward the topological advancement has been made, still there exists a huge scope for synthesizing of reduced component based CGT topology with boosting ability.

This paper examines a transformer-less grid-tied inverter topology is proposed which is common ground type (CGT), where the ground of utility is connected with the negative terminal of dc source. This results in a short circuit of PV-to-ground parasitic capacitance leads to complete elimination of the CM leakage current. It has the ability of inherent boosting voltage without any additional circuit. The proposed inverter topology generates five-level output voltage leads to minimized voltage stress, decreased filter size and higher efficiency. Auxiliary capacitors are naturally balanced, hence proposed topology does not have any limitation on the achievable modulation index. Maximum conducting switch in the grid current path is ≤ 3 during the energy transmission mode, which results in increased efficiency. The major contribution of the presented work is the devising of a five-level inverter with zero leakage current with reduced component count for PV application.

The paper is organized as follows: structure and operating modes of the proposed inverter topology are explained in Section II. Common mode behaviour is elucidated in Section III. Sections IV and V describes the design guidelines and power loss analysis. A quantitative comparison of existing grid-tied inverter topologies with proposed inverter is done in Section VI. Experimental results of are explained to validate the feasibility of the presented topology in Section VII. Finally, the paper is concluded in the following section.

2 | STRUCTURE OF THE PROPOSED INVERTER TOPOLOGY

2.1 | Structural description of the proposed five-level boosted inverter topology

The schematic of the proposed topology is shown in Figure 3. It consists of seven power switches, two auxiliary capacitors and one diode for synthesizing a five-level output voltage waveform. The appropriate switching states to be employed are listed in Table 1. The switches $S_1$, $S_2$ and $S_3$ work in complementary to switches $\bar{S}_1$, $\bar{S}_2$ and $\bar{S}_3$ respectively. The input voltage is designated as $V_{dc}$. The auxiliary capacitor $C_2$ helps to generate the negative levels of the output voltage. Voltage across the auxiliary capacitors $C_1$ and $C_2$ are to be maintained at $V_{dc}$ and $2V_{dc}$ respectively to produce five-level voltage.

## Table 1

| $V_{out}$ | $S_1$ | $S_2$ | $S_3$ | $\bar{S}_3$ | $D$ | $C_1$ | $C_2$ |
|-----------|-------|-------|-------|-------------|-----|-------|-------|
| $2V_{dc}$ | on    | on    | on    | off         | off | down  | up    |
| $V_{dc}$  | off   | on    | on    | off         | on  | up    | -     |
| 0         | on    | on    | off   | on          | off | down  | up    |
| $-V_{dc}$ | off   | off   | off   | on          | on  | up    | -     |
| $-2V_{dc}$| off   | off   | off   | off         | on  | up    | -     |

2.2 | Analysis of operating modes

Working modes of the proposed inverter topology are shown in Figure 4. The proposed topology has five working modes, as per the direction of output voltage, current and level of output voltage. The figure describes the switching state of switches, charging/discharging structure of auxiliary capacitors and output-current path. The different working modes are analyzed in details as follows.

**Mode I:** $i_L > 0$, $V_{out} > 0$. In this mode, power is transferred from PV to grid side through $S_1$, $S_2$, and $S_3$, as shown in Figure 4. The auxiliary capacitor $C_2$ charges from the source and $C_1$ up to $2V_{dc}$ through $\bar{S}_1$, $\bar{S}_2$, and $\bar{S}_3$ over the whole period. Mathematically, the output voltage can be expressed as:

$$V_{out} = V_{dc} + V_{cl} = 2V_{dc}, \quad i_L > 0 \quad (1)$$

During this operating mode inductor current ($i_L$) increases rapidly passing through grid and is expressed as:

$$i_L = \frac{2V_{dc} - V_{g}}{L_f}. \quad (2)$$

**Mode II:** $i_L > 0$, $V_{out} > 0$. In this mode, power is transferred from auxiliary capacitor $C_1$ to grid side through $\bar{S}_1$, $\bar{S}_2$, and $\bar{S}_3$, as shown in Figure 4. The auxiliary capacitor $C_2$ charges from the source up to $V_{dc}$ through diode and $\bar{S}_1$ over the whole period, $C_2$ is disconnected and its voltage remains intact. Mathematically, the generated voltage can be expressed as:

$$V_{out} = V_{cl} = V_{dc}, \quad i_L > 0 \quad (3)$$

![Figure 3 Schematic of the proposed inverter topology with boosting ability](image-url)

![Figure 4 Working modes of the proposed inverter topology](image-url)
and inductor current \( i_L \) is expressed as:

\[
    i_L = \frac{V_{dc} - V_g}{L_f}
\]

**Mode III**: \( i_g > 0 \) or \( < 0 \), \( V_{out} = 0 \). In this mode, the inductor charges or discharges to grid through \( S_3 \) and \( S_B \), as shown in Figure 4. The auxiliary capacitor \( C_2 \) charges from the source and \( C_1 \) up to \( 2V_{dc} \) through \( S_1, S_2 \) and \( S_B \) over the whole period. The generated voltage is:

\[
    V_{out} = 0, \quad i_g > 0 \text{ or } < 0.
\]

During this mode \( i_L \) passes through \( S_3 \) and \( S_B \) and linearly decreases, is expressed as:

\[
    i_L = -\frac{V_g}{L_f}.
\]

**Mode IV**: \( i_g < 0 \), \( V_{out} < 0 \). In this mode, energy is transferred from grid to dc side through \( S_3 \), \( S_2 \) and \( S_1 \), as shown in Figure 4. For positive load current the auxiliary capacitor \( C_2 \) discharges to \( C_1 \) and grid while for negative load current, vice-versa over the whole period. Mathematically, the generated voltage can be expressed as:

\[
    V_{out} = V_{c2} - V_{c1} = -2V_{dc}, \quad i_g < 0.
\]

During this operating mode \( i_L \) increases rapidly in reverse direction passing through grid, expressed as:

\[
    i_L = \frac{2V_{dc} - V_g}{L_f L}.
\]

**Mode V**: \( i_g < 0 \), \( V_{out} < 0 \). In this mode, energy is transferred from auxiliary capacitor \( C_2 \) to the grid side through \( S_1 \) and \( S_2 \), as shown in Figure 4. The auxiliary capacitor \( C_1 \) charges from the source up to \( V_{dc} \) through diode and \( S_1 \) over the whole period. Mathematically, the generated voltage can be expressed as:

\[
    V_{out} = V_{c2} = -2V_{dc}, \quad i_g < 0.
\]

During this mode \( i_L \) passes through \( C_2, S_1 \) and \( S_2 \), which is expressed as:

\[
    i_L = \frac{2V_{dc} - V_g}{L_f L}.
\]
These working modes are analyzed and if the load requires reactive power then charging/discharging structure of auxiliary capacitors are varied according to load current direction, as shown in Figure 4.

### 2.3 Pulse-width modulation scheme

This section describes the gating-signals for each switch, which is developed by using logic gates and comparators. A sinusoidal reference signal ($V_{\text{ref}}$) is compared with carrier signals which are $V_{\text{c}1}$, $V_{\text{c}2}$, $V_{\text{c}3}$, and $V_{\text{c}4}$, as depicted in Figure 5. Logic function is developed for all switches to perform the desirous operation according to the operating modes demonstrated in Section II. The rationale behind the logic operation involves those entries wherein a particular switch needs to be ON. For example, consider for $S_1$, since it is ON for zero and $2V_{dc}$ level, the comparator outputs corresponding to these two levels are added (logical OR). Using the same principle the logic expression for rest of the switches have been derived.

### 3 COMMON MODE BEHAVIOUR

By maintaining a constant CM voltage, ground leakage current is minimized/eliminated. In this section the capability of proposed topology in maintaining a constant CM voltage by considering the effect of the parasitic capacitor of switches is illustrated. The equivalent circuit during mode I and II by considering the parasitic capacitors of switches, is demonstrated in Figure 6. According to the equivalent circuit of mode I, shown in Figure 6(a) the voltage at point A with respect to point B is:

\[
V_{AN} = 2V_{dc} \tag{11}
\]

\[
V_{BN} = 0. \tag{12}
\]

The total CM voltage $V_{\text{cm-all}}$ is expressed by [9]:

\[
V_{\text{cm-all}} = \frac{V_{AN} + V_{BN}}{2} + \frac{(V_{AN} - V_{BN})}{2(L_2 + L_A)} L_2 - L_A
\]

\[
= \frac{2V_{dc} + 0}{2} + \frac{(2V_{dc} - 0)}{2(0 + L_A)} 0 - L_A = 0. \tag{13}
\]
As per circuit equivalent circuit of mode II, shown in Figure 6(b) the voltage $V_{AN}$ is given by:

$$V_{AN} = V_{dc}$$

(14)

$$V_{BN} = 0.$$  

(15)

Further the CM voltage is expressed by:

$$V_{cm-all} = \frac{V_{dc}}{2} + \frac{(V_{dc} - 0) \cdot 0 - L}{2(0 + L)}$$

$$= \frac{V_{dc}}{2} - \frac{V_{dc}}{2} = 0$$

(16)

where $V_{AN}$ and $V_{BN}$ is voltage between the phase A and point N, phase B and the point N, respectively as shown in Figure 6 and $C_{PV}$ capacitor between PV neutral and grid neutral. The ground leakage current is expressed as:

$$i_{cm} = C_{PV} \cdot \frac{dV_{cm-all}}{dt} = 0 .$$

(17)

Since, the CM voltage is effected by the presence of switch parasitic capacitance of switches, hence the proposed topology is able to eliminate the ground leakage current completely.

### 4.1 Inductance value

The passing current of filter inductor within a complete switching cycle is obtained as

$$i_L(t) = \frac{1}{L_f} \int_0^{T_s} V_L(t) d(t) + i_L(0).$$

(22)

Hence, ripple current of the inductor is obtained as:

$$\Delta i_L = \frac{(2V_{dc} - V_g) DT_s}{L_f}.$$  

(23)

By using (31) in (23), it ripple current is:

$$\Delta i_L = \frac{1}{L_f f_s} \left(2V_{dc} - 3V_g + \frac{V_g^2}{V_{dc}}\right).$$  

(24)

So, $L_f$ can be calculated as:

$$L_f = \frac{1}{\Delta i_L f_s} \left(3V_g - \frac{V_g^2}{V_{dc} - 2V_{dc}}\right).$$

(25)

### 4.2 Capacitance value

For sizing of the auxiliary capacitors value, following equation is used -

$$C_1 = \frac{i_g \cdot \Delta t}{\Delta V_c \cdot V_{dc}}$$

(26)

where $i_g$ is the load peak current, $\Delta t$ is charging or discharging time for capacitor, $V_c$ is the voltage for capacitors i.e. $V_{dc}$ for $C_1$ and $2V_{dc}$ for $C_2$ and $\Delta V_c$ is the % of maximum ripple content in capacitor voltage. During $2V_0 = 2V_{dc}, \Delta t$ is $DB_s$, hence

$$C_1 = \frac{i_g DB_s}{\Delta V_c \cdot V_{dc}}$$

$$= \frac{i_g DB_s}{f_s \Delta V_c \cdot V_{dc} \left(\frac{V_g}{V_{dc}} - 1\right)}.$$  

(27)

### 5 LOSS CALCULATION AND ANALYSIS

In the practical applications semi-conductor switches has energy losses, which includes conduction and switching losses. These losses occur due to their turning on/off time, passing active current, their blocking voltage and ON-state resistance.


5.1 Zone I

The output voltage during zone I as shown in Figure 5 is defined as:

\[
V_0 = \begin{cases} 
2V_{dc} & 0 < t < D_1 T_i \\
V_{dc} & D_1 T_i < t < T_i .
\end{cases}
\] (28)

Therefore, voltage across filter inductor is defined as:

\[
V_L = \begin{cases} 
2V_{dc} - V_g & 0 < t < D_1 T_i \\
V_{dc} - V_g & D_1 T_i < t < T_i .
\end{cases}
\] (29)

By using the volt-second balance principle:

\[
\int_{0}^{D_1 T_i} (2V_{dc} - V_g) dt + \int_{D_1 T_i}^{T_i} (V_{dc} - V_g) dt = 0.
\] (30)

Solving (30) yields duty ratio \( D_1 \) as,

\[
D_1 = \frac{V_g(t)}{V_{dc}} - 1.
\] (31)

1. Conduction loss: Average conduction loss for a switch could be expressed as:

\[
P_{\text{cond.}} = \frac{1}{2\pi} \int_{0}^{\pi} i_s(t) v_s(t) D_s(t) d(\omega t)
\] (32)

Where \( i_{s1,2}(t) = I_w \sin \omega t + I_s, i_{s3}(t) = I_w \sin \omega t \) and \( i_{sB}(t) = I_s \).

Voltage across switches is \( v_s(t) = i_s(t) R_{ds}, v_g(t) = v_m \sin \omega t \) and \( D_s(t) = \left( \frac{V_g(t)}{V_{dc}} - 1 \right) \). \( I_s \), passing current through flying capacitor \( C_2, I_s = C_2 \frac{dV_g}{dt} \).

Conduction loss for switch \( S_1 \) and \( S_2 \)

\[
P_{\text{cond.1,2}} = \frac{1}{2\pi} \int_{0}^{\pi} (I_w \sin \omega t + I_s)(I_w \sin \omega t + I_s) R_{ds} \left( \frac{v_m \sin \omega t}{V_{dc}} - 1 \right) d(\omega t).
\] (33)

By solving this equation conduction loss for switch \( S_1 \) and \( S_2 \) is calculated as:

\[
P_{\text{cond.1,2}} = \frac{2I_w^2}{3\pi} \left( \frac{v_m}{v_{gb}} - \frac{1}{2} \right) + I_s^2 \left( \frac{v_m}{2v_{gb}} - \frac{2}{\pi} \right) R_{ds}.
\] (34)

Conduction loss for switch \( S_3 \)

\[
P_{\text{cond.3}} = \frac{1}{2\pi} \int_{0}^{\pi} I_w^2 R_{ds} \sin^2 \omega t \left( \frac{v_m \sin \omega t}{V_{dc}} - 1 \right) d(\omega t).
\] (35)

Using the above equation the conduction loss for switch \( S_3 \) is obtained as:

\[
P_{\text{cond.3}} = \frac{I_w^2}{2\pi} R_{ds} \left( \frac{4v_m}{3V_{dc}} - \frac{\pi}{2} \right).
\] (36)

Conduction loss for switch \( S_B \)

\[
P_{\text{cond.3}} = \frac{1}{2\pi} \int_{0}^{\pi} I_w^2 R_{ds} \left( \frac{v_m \sin \omega t}{V_{dc}} - 1 \right) d(\omega t).
\] (37)

The conduction loss for switch \( S_B \) is obtained as:

\[
P_{\text{cond.3}} = \frac{I_w^2}{2\pi} R_{ds} \left( \frac{v_m}{V_{dc}} - \pi \right).
\] (38)

Switches \( S_2 \) and \( S_3 \) both are off, hence conduction loss for these switches are zero during zone I.

2. Switching loss: Generally, switching losses occur due to cross over of voltage and current waveform at the time of commutation, which can be expressed as:

\[
P_s = \frac{1}{6} \int_{0}^{t_{on}} v_{gb} I_w \sin \omega t dt + \int_{0}^{t_{off}} v_{gb} I_w \sin \omega t dt.
\] (39)

Switching loss for switch \( S_1 \)

During zone I, passing current of \( S_1 \) is:

\[
I_{s1} = \begin{cases} 
\frac{I_w}{\pi} + I_s & 0 < t < D_1 T_i \\
0 & D_1 T_i < t < T_i .
\end{cases}
\] (40)

Average of passing current of \( S_1 \) calculated as:

\[
I_{savg} = \frac{1}{T_i} \int_{0}^{D_1 T_i} \left( \frac{I_w}{\pi} + I_s \right) dt = \left( \frac{I_w}{\pi} + I_s \right) D_1
\] (41)

\( i_s(t) = I_w \sin \omega t \), Hence \( i_{savg} = \frac{I_w}{\pi} \). And blocking voltage of \( S_1 \) is \( V_{gb} \), hence switching losses is obtained as:

\[
P_{sw1} = \frac{1}{6} \int_{0}^{t_{on}} V_{gb} \left( \frac{I_w}{\pi} + I_s \right) D_1 dt + \int_{0}^{t_{off}} V_{gb} \left( \frac{I_w}{\pi} + I_s \right) D_1 dt.
\] (42)

\[
P_{sw1} = \frac{1}{6} \int_{0}^{t_{on}} V_{gb} I_w \sin \omega t dt + \int_{0}^{t_{off}} V_{gb} I_w \sin \omega t dt.
\] (43)
The effective junction temperature for a switching device is expressed as [29, 30]:

\[ T_j = T_A + P_{tot} \times R_{jg} \]  

(48)

where \( T_A \) is ambient temperature, \( P_{tot} \) is total power loss which is \( P_{cond.} + P_{sw} \) and \( R_{jg} \) junction thermal impedance. Junction temperature for switch \( S_1 \) is obtained as:

\[ T_j = T_A + (P_{cond.1} + P_{sw1}) \times R_{jg}. \]  

(49)

If \( R_{jg} \) is 40 °C/W and power loss across \( S_1 \) is 1.15 W, \( T_j \) is obtained as:

\[ T_j = 25 + 1.15 \times 40 = 71^\circ C. \]  

(50)

Hence \( S_1 \) is able to sustain the 71 °C junction temperature.

### 6 | COMPARISON WITH OTHER SIMILAR TOPOLOGIES

A comprehensive yet qualitative comparison of the proposed topology against the state-of-the-art inverters is carried out in this section. Table 3 summarizes the different figures of merits considered for the comparative study. The comparison is done in terms of component count, on-state switches during each mode, existence of leakage current, levels and boosting ability of output voltage. The number of power switches is a critical feature in inverters to dictate the overall size and cost. The more number of switches escalates the cost, size and complexity of the circuit, while the number of conducting switches affects the overall conduction and switching losses, and in turn the efficiency of the inverter. From the literature survey, it can be seen that the topologies based on the half-bridge inverter requires twice the peak grid voltage. None of them have the boosting ability, hence additional conversion circuit is needed to fulfill the grid voltage requirement. To overcome all problems the topology is proposed in this paper which all merits that are desirous.

Gate driver circuits are developed to control and generate the gating pulses to switches. Higher number of gate driver...
TABLE 3 Comparative analysis of available grid-tied inverters with proposed topology

| Inverter Topologies | Number of Components | Maximum Conducting Switches | Output Voltage levels | Leakage current | Boosting Ability | Input DC-link voltage |
|---------------------|----------------------|-----------------------------|-----------------------|----------------|-----------------|----------------------|
|                     | \(N_h\) | \(N_f\) | \(N_{Cap}\) | \(N_{Ind}\) | \(N_{Lf}\) |   |   |   |   |   |   |
| H-Bridge [3]        | 4      | 0      | 0          | 0          | 2             | 2      | 3      | No-Zero | No | \(V_{dc}\) |
| HS [7]              | 5      | 0      | 1          | 0          | 2             | 3      | 3      | Non-Zero | No | \(V_{dc}\) |
| H6 [8]              | 6      | 2      | 2          | 0          | 2             | 3      | 3      | Non-Zero | No | \(V_{dc}\) |
| HERIC [9]           | 6      | 0      | 1          | 0          | 2             | 3      | 3      | Non-Zero | No | \(V_{dc}\) |
| Half-Bridge [14]    | 2      | 0      | 2          | 0          | 1             | 1      | 2      | No-Zero | No | \(2V_{dc}\) |
| NPC [15]            | 4      | 2      | 2          | 0          | 1             | 2      | 3      | Non-Zero | No | \(2V_{dc}\) |
| ANPC [16]           | 6      | 0      | 2          | 0          | 1             | 2      | 3      | Non-Zero | No | \(2V_{dc}\) |
| Conergy NPC [10]    | 4      | 0      | 2          | 0          | 1             | 3      | 3      | No-Zero | No | \(V_{dc}\) |
| Karschny [20]       | 5      | 2      | 1          | 1          | 1             | 3      | 3      | No-Zero | No | \(V_{dc}\) |
| Inverter in [22]   | 4      | 2      | 3          | 0          | 1             | 2      | 3      | No-Zero | No | \(V_{dc}\) |
| Inverter in [21]   | 5      | 0      | 2          | 0          | 1             | 3      | 3      | No-Zero | No | \(V_{dc}\) |
| Inverters in [24]  | Type-I | 4      | 1          | 2          | 0          | 1      | 2      | 3      | No-Zero | Vdc |
|                     | Type-II| 4      | 1          | 2          | 0          | 1      | 2      | 3      | No-Zero | Vdc |
|                     | Type-III| 4    | 0          | 2          | 0          | 1      | 2      | 3      | No-Zero | Vdc |
| Inverters in [23]  | Type-I | 4      | 0          | 2          | 0          | 1      | 2      | 3      | No-Zero | Vdc |
|                     | Type-II| 6      | 0          | 3          | 0          | 1      | 3      | 5      | No-Zero | Vdc |
| Inverter in [12]   | 8      | 0      | 2          | 0          | 2          | 4      | 5      | Non-Zero | No | \(V_{dc}\) |
| Inverter in [13]   | 6      | 0      | 2          | 0          | 2          | 5      | 5      | No-Zero | No | \(V_{dc}\) |
| Inverter in [25]   | 6      | 1      | 2          | 0          | 1          | 3      | 5      | Zero    | No | \(V_{dc}\) |
| Proposed Topology  | 8      | 1      | 2          | 0          | 1          | 3      | 5      | Zero    | Yes | 0.5\(V_{dc}\) |

TABLE 4 Voltage stress on power switches

| Switch | \(S_1\) | \(S_1\) | \(S_2\) | \(S_2\) | \(S_3\) | \(S_3\) | \(S_4\) |
|---------|---------|---------|---------|---------|---------|---------|---------|
| Voltage stress | \(V_{dc}\) | \(V_{dc}\) | \(2V_{dc}\) | \(2V_{dc}\) | \(2V_{dc}\) | \(2V_{dc}\) |

7 7 7 EXPERIMENTAL VERIFICATION

This section describes the experimental outcomes of the proposed inverter topology. A small-scale laboratory prototype is developed to verify the operation and workability of the proposed topology. The ratings of different elements and other parameters are indexed in Table 5. TLP250 drivers are used
to drive the power switches. The proposed topology has six unidirectional and one bidirectional switch. Hence, it requires seven driver circuit due to bidirectional switch which leads to decreased cost. DS1202/1302 dSPACE controller is used for the generation of pulse width modulation signal. The dc source voltage is set to 50 V and the inverter is switched at 1 kHz. The corresponding blocking voltage of each switch is shown in Table 4.

The five-level output voltage as well as voltage across the auxiliary capacitors at no-load, is depicted in Figure 7. The voltage across auxiliary capacitors are well balanced, which is achieved without the need for any voltage or currents sensors. The balanced voltage across $C_1$ and $C_2$ is $V_{dc}$ and $2V_{dc}$ respectively, that is 50 V and 100 V. Further, the output waveforms pertaining to loading of the inverter, are demonstrated in Figure 8. Figure 9 demonstrates the performance of the proposed inverter for variable source voltage. The behaviour of proposed inverter typology during variable load condition is demonstrated in Figure 10. The peak value of load current is 5 A at the lagging power factor, which shows that the proposed topology is able to provide the reactive power to load. To compare the efficiency of proposed topology with other existing topologies, the efficiency versus output power curve is depicted in Figure 11. The curves are obtained for same circuit parameters, input and output voltage. From the curve, it can be observed that the efficiency of
the proposed topology is competent enough with those of its popular counterparts.

8 | CONCLUSION

This paper examines a five-level boosting grid-tied transformerless inverter is proposed based on common-ground type connection. Hereby, the negative pole of dc-link and neutral of utility grid is short circuited, hence leakage current is totally eliminated. In the proposed inverter switched capacitor technique is used, so it has boosted output voltage capability. It generates five-level output voltage which leads to minimize harmonics, less filter size and high efficiency with less component count. To balance/regulate the voltages across the auxiliary capacitor required controller is less complex and it is accomplished by using less number of logic gates and comparators. Also, it does not have any limitation of modulation index since auxiliary capacitors are naturally balanced. In order to verify the performance of the proposed inverter topology a laboratory prototype is developed in lab and results are obtained to confirm the operation and feasibility of the proposed inverter. Obtained results demonstrates the output voltage, load current and balanced voltage across auxiliary capacitors. Moreover, the quantitative comparison study confirms the benefits of the proposed inverter topology regarding boosted voltage, complete elimination of leakage current and reduced part count.

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   (b) Arun Kumar Verma: Supervision.
   (c) Sandeep N: Conceptualization, supervision, Writing-original draft, Writing-review and editing.
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