2D Linear Trap Array for Quantum Information Processing

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An ion-lattice quantum processor based on a two-dimensional arrangement of linear surface traps is presented. The design features a tunable coupling between ions in adjacent lattice sites and a configurable ion-lattice connectivity, allowing one, for example, to realize rectangular and triangular lattices with the same trap chip. Detailed trap simulations of a simplest-instance ion array with 2 × 9 trapping sites are presented and the fabrication of a prototype device in an industrial facility is reported on. The design and the employed fabrication processes are scalable to larger array sizes. Trapping of ions in rectangular and triangular lattices and transport of a 2 × 2 ion-lattice over one lattice period are demonstrated.

1. Introduction

Trapped ions are one of the most successful platforms for quantum information processing to date, with high gate fidelities and long coherence times.[1–5] Trapped-ion quantum processors have been used to implement quantum algorithms, such as Grover’s and Shor’s algorithms,[6,7] to implement quantum error correction protocols,[8,9] and have also been successfully employed as quantum simulators, for instance, for the observation of many-body dynamical phase transitions,[10,11] the simulation of particle-antiparticle generation in lattice gauge theories,[12] or to calculate molecular ground state energies of simple molecules.[13] Currently, the biggest challenge for trapped-ion quantum processors is to scale-up the number of qubits. One approach toward scalable systems is to distribute the quantum register over several trapping zones using a so-called QCCD-architecture (quantum charge-coupled device) and to eventually modularize the processor.[14–16] In such a QCCD processor, each trapping zone contains only a small number of ions that can be manipulated with high-fidelity, while exchange of quantum information among the zones requires splitting, shuttling, and merging of ion strings.[14–16,20] Complementary to this approach, one can also couple and entangle ions in different trapping potentials utilizing adiabatic well-to-well interactions or, as recently proposed, broadband pulse sequences with high-power lasers.[25] Following this idea, microfabricated ion trap arrays have been realized in order to create 2D ion lattices on a microchip,[26–31] and recently, first quantum simulations have been performed in such a system.[32] Arrays of individual traps have the advantage that the ions are not subjected to excess micromotion, in contrast to 2D ion lattices naturally forming in a single trapping potential.[33,34] In addition, microfabricated trap arrays offer a much finer control of the confining potential landscape and allow one to set the structure of the ion lattice by choice of the electrode geometry and control voltages.

Previous designs of ion-lattice quantum processors have mainly investigated surface point traps as fundamental building block of the trap array.[26,27,29–31] An exception is the work of Tanaka et al.,[28] where two parallel linear traps have been used. In our article, we further develop this latter approach: realizing a scalable trapped-ion quantum processor based on parallel linear surface traps. Our design enables tunable site-to-site coupling by combining the concepts of variable radio-frequency (RF) voltages with island-like electrodes, where static (DC) voltages are applied. The usage of linear traps as building block of the array thereby offers additional advantages compared to point traps. First, ions can be shuttled along the linear trap axes, giving rise to a configurable ion lattice connectivity and allowing for transport of quantum information, physically encoded in the ions, over large distances through the lattice. These points will be further discussed in the next sections. Second, due to the linear nature of the RF traps, multiple ions can be trapped in each site of the ion lattice without subjecting them to excess micromotion. Storage of multiple ions per site could be useful to increase the dipole–dipole coupling across adjacent sites thereby reducing the gate time for inter-site entangling operations. Furthermore, one could use sympathetic cooling techniques and apply standard quantum gate operations to ions within one site, potentially allowing for even more complex quantum...
simulations to be run. Our design employs variable RF voltages to temporarily decrease the ion spacing, allowing for an enhanced site-to-site coupling in the ion lattice. For an array of parallel linear traps, such RF shuttling requires only two independent RF voltages, independently of the array size. This is a drastic reduction compared to our previous work with point trap arrays where the number of required RF voltages scales linearly with the array size.\[39\] Furthermore, the use of RF voltage tuning allows one to use an ion-electrode separation \( d \) that is significantly increased compared to the one required in an array with sufficiently small ion–ion distance and fixed RF voltage. The separation \( d \) thereby remains basically constant during RF tuning. This point will be further discussed in Section 2 and in Appendix D. Larger separations \( d \) can help reduce the motional decoherence rate (ion heating rate), which is a limiting factor in previous 2D ion lattices.\[34\]

The article is structured as follows: In Section 2, the conceptual design and functionality of the proposed trap array are outlined. In Section 3, we consider a minimal instance array consisting of two parallel linear traps with segmented DC electrodes. This minimal instance design possesses the core functionality of the proposed processor, which we show by trap simulations in Section 3.1. In Section 3.2, we describe the fabrication process and show electrical characteristics of the fabricated trap chips. In Section 3.3, we demonstrate ion-trapping in multiple trapping sites and characterize a trap chip in terms of electric stray fields and motional heating. Future improvements of the trap design and fabrication, as well as an outlook on future designs are discussed in Section 4. This discussion is complemented by simulations of a trap array with \( 10 \times 10 \) trapping sites, shown in Appendix C.

2. Conceptual Design

The electrode geometry of the proposed quantum processor is a linear trap array, as illustrated in Figure 1. Colinear rails for radiofrequency (RF) voltage (green) are alternated with segmented rails (blue) that are grounded in the RF domain. This configuration creates parallel linear traps for ions with a spacing \( s_x \) at a distance \( d \) above the chip surface. Within each linear trap, an additional multiwell potential with periodicity \( s_x \) is established along the \( z \)-direction by applying spatially periodic static voltages (DC) on the blue electrode segments. The combination of RF and DC fields thus creates a 2D lattice of trapping sites with trap spacings \( s_x \) and \( s_z \). The quantum states of ions confined within the same trapping site are manipulated using state-of-the-art protocols.\[22,26\] Quantum operations between ions in adjacent trapping sites, such as entangling gates or effective spin-spin interactions, are realized via the coupling of their motional states.\[23\] Of central importance for this is the motional coupling strength\[22,23\]

\[
\Omega_c = \frac{\zeta_j Q^2}{2\pi\varepsilon_0 M \omega_x s_j^3}, \quad \text{with } \zeta_j = \begin{cases} \frac{1}{2} & \text{for } j = z \text{ (coupling along } z) \\ 1 & \text{for } j = x \text{ (coupling along } x) \end{cases}
\]

Here, \( M \) is the mass of the ions in each site, \( Q \) their charge, and \( \omega_x \), their (resonant) axial frequencies.\[37\] The motional coupling strength \( \Omega_c \) depends crucially on the trap spacings \( s_x \) and \( s_z \), respectively. This has important consequences for the design of the trap array. For the proposed quantum processor, Figure 1, we can envision two distinct design choices: (i) the ion lattice has small trap spacings with sufficient motional coupling \( \Omega_c \) at all times; (ii) the ion lattice has relatively large trap spacings which need to be temporarily decreased to realize an inter-site quantum operation.

Feasible parameters for design choice (i) would be a trap spacing \( s_x \approx 40 \mu \text{m} \) with a coupling rate \( \Omega_c \approx 2\pi \times 1 \text{ kHz} \), as used in ref. [31]. Furthermore, the coupling strength \( \Omega_c \) between any pair of adjacent trapping sites could be tuned by adjusting the values \( s_x \). This can be achieved by controlling the RF and DC voltages in the trap array as explained later on. A downside of design choice (i) is the required small ion-surface separation \( d \lesssim s_x \) (see Appendix D for details). Such a close proximity to the trap surface typically entails a large motional decoherence rate (heating rate) \( \Gamma_h \). High heating rates \( \Gamma_h \gg \Omega_c \) are a serious impediment for realizing inter-site quantum gates with high fidelity.\[23,24\] While cryogenic trap operation and surface cleaning have been demonstrated to strongly reduce the heating rate, the physical origin of the electric field noise remains unknown, and there exists no general procedure that would guarantee a small \( \Gamma_h \).\[38\] Even if an ion-surface separation \( d \gg s_x \) with a lower \( \Gamma_h \) could be realized, for instance by using an electrode geometry different to that in Figure 1, such a trap array would unavoidably have inefficient operating conditions due to the exponential decrease of electrode potentials for distances \( d \) much larger than the electrode dimensions.\[39\] Indeed, trap arrays typically operate in the regime \( d \lesssim s_x \).\[26,27,29–31\]

For design choice (ii) one picks modest trap spacings \( s_x \approx (100–150) \mu \text{m} \) that allow for a larger electrode-ion separation \( d \approx s_x \). The increased distance between ions and trap surface can lead to significantly lower heating rate, since \( \Gamma_h \propto d^{-4} \) for many sources of electric field noise.\[38\] In the remainder of this article, we will therefore focus on design choice (ii). The potential reduction in ion heating rate is traded for having only small motional coupling strengths \( \Omega_c \approx 2\pi \times 100 \text{ Hz} \) between adjacent trapping sites (cf. Equation (1)). Quantum operations between adjacent trapping sites hence need to be realized in a sequential fashion using ion-shuttling operations that temporarily decrease \( s_x \). This is illustrated in Figure 2. Starting from the default configuration (Figure 2a), the trap spacing \( s_x \) can be strongly reduced by lowering the RF voltage on the RF rail between two adjacent trapping sites (bright green) (Figure 2b). Similarly, adjacent ions can be brought close along the axial direction \( z \) by adjusting the DC
votages on the DC segments (Figure 2c). At a reduced distance $s_z = (30–50) \mu m$, coupling strengths $\Omega_c$ in the kHz range can be achieved, sufficient for coherent operations.\cite{2,3} The ability to reduce the trap spacing can now be employed to sequentially realize inter-site quantum operations such as entangling gates: Once the desired coupling strength is reached, the secular modes are tuned into resonance and the ions’ electronic states are entangled under simultaneous irradiation with laser light (see e.g., ref. [23]). Parallelized entangling operations of pairs of nearest neighbor ions across the array are possible using a global laser field; unwanted coupling between non-nearest neighbors could be drastically reduced by choosing different resonance frequencies for adjacent pairs.\cite{2,9,10,21,22,23,24,40} as outlined in Appendix E. Subsequently, the lattice spacing is restored to the original value. Entanglement between all nearest neighbors on a rectangular lattice of ions, illustrated in Figure 2d, can thus be created using four parallelized shuttling-steps. We emphasize that the ion entanglement, once established, does not depend anymore on the physical arrangement of the ions. This enables the realization of different lattice connectivities using additional ion-shuttling operations along the trap axis $z$. For instance, starting from the connected rectangular lattice, a shift of ions by one lattice spacing along $z$ followed by additional entangling operations along $x$ allows one to establish a triangular lattice connectivity, illustrated in Figure 2e. In a similar fashion, $z$-translations of ions can be used to enable entanglement between more distant ions, for example, next-nearest neighbors on the rectangular lattice or even ions at different ends of the lattice.

The sequential coupling scheme outlined above is useful for various applications. For instance, the motional coupling between ions in adjacent trapping sites could be used for the simulation of spin models in a sequential way (digital quantum simulator).\cite{2,9} Another possibility might be to extend recent studies of entanglement propagation in a linear ion chain\cite{24} to a 2D ion lattice. Furthermore, one could create cluster states by applying a controlled phase gate (e.g., realized by an entangling operation and single qubit rotations) to every pair of neighboring sites in the rectangular ion lattice.\cite{41} The cluster states could then be used as a resource for a measurement-based quantum processor.\cite{44}

In addition to qubit–qubit operations across adjacent trapping sites, the envisioned quantum processor will need single qubit gates, requiring laser-addressing of individual trapping sites. For small and moderate-sized arrays, this could be achieved with a Raman gate.\cite{45} employing a crossed Raman beam geometry to address a specific ion. Cross talk could be reduced by moving untargeted ions along the trap axes, out of the beam path. For larger arrays, more scalable solutions will eventually be required: integrated optics such as waveguides with Bragg couplers integrated into the trap chip,\cite{46} or global microwave radiation fields in combination with magnetic field gradients.\cite{47}

### 3. Simplest Instance: Linear Twin-Trap

The simplest instance of the linear trap array outlined in the previous section is given by two parallel linear traps with segmented DC electrodes, referred to as linear twin-trap in what follows. Figure 3a gives an overview of the electrode geometry. The twin-trap has a central region, surrounded by four identical quadrants (NW, NE, SW, SE). Confinement in the radial ($xy$-) plane is produced by the three RF rails (green), that stretch over the entire length of the trap. In between the RF electrodes, there are two segmented DC rails with segment lengths $l_{DC}$. (Figure 3b). The RF and DC rail widths $w_{RF}$, $w_{DC}$ and $w_{DC}$ are optimized for maximum trap efficiency, which also leads to close-to-optimal trap depth.\cite{48,49} Within each trap quadrant, the DC segments are periodically connected as indicated by the different tones of blue. This enables the creation of multiwell potentials for axial confinement along the $z$-axis with a lattice spacing $s_z = 3 l_{DC}$. Additional outer DC electrodes at the edge of the structure (dark blue) are needed to overlap the two DC multiwells with their respective RF null. Within each trap quadrant, the DC segments and outer DC electrodes can be controlled independently.
The electrode geometry of the linear twin-trap is shown in Figure 3. (a) Three colinear RF rails (green) with lengths $l_r = 6\,\text{mm}$ create radial confinement for two parallel linear traps. The rails have widths of $w_o = 252\,\mu\text{m}$ (outer rails) and $w_i = 73\,\mu\text{m}$ (inner rails). (b) The two DC rails with widths $w_{DC} = 102\,\mu\text{m}$ are broken up into island-like DC segments of length $l_{DC} = 102\,\mu\text{m}$. Additional DC rails with width $w_{DC} = 202\,\mu\text{m}$ at the edge of the structure are not segmented. The segments in each trap quadrant (NW, NE, SW, SE) are connected periodically to the same voltage supply channel as indicated by the different tones of blue. Electrode voltages in different quadrants can be set independently. (c) At the trap center, an axial interaction zone is realized by DC segments with a smaller length of $l_{DC}/3$ and an independent segment of the outer DC rails with length $l_{DC,D} = 306\,\mu\text{m}$.

The periodic assignment of voltages to the DC segments, shown in Figure 3b, allows one to control the DC multipoles with only 4 DC channels each (3 DC segments and 1 outer DC). Furthermore, the DC multipoles in the left and right linear trap can be independently translated along the $z$-axis, as required for establishing different lattice connectivities. Ion transport within one linear trap thereby employs the periodicity of the DC segments, similar as in other surface trap designs. The independent transport in two parallel linear traps relies on the fact that the left multivolt is mainly controlled by DC segments in the left linear trap, while the segments in the right trap have a significantly weaker influence due to the larger spatial separation, and vice versa. This principle should be easily extendable to a larger number of parallel traps.

The DC islands at the trap center, shown in Figure 3c, are further split in three segments of length $l_{DC}/3$, and also the outer DC rails have an independent segment of length $l_{DC,D}$. The finer segmentation in this axial interaction zone allows one to reduce the lattice spacing $s_z$ locally for the central pairs of trapping sites. Alternatively, the three central segments can be treated as one electrode of length $l_{DC}$ for a seamless transport of the DC multipoles across the central region during axial shuttling operations.

The twin-trap design (Figure 3) is similar to the trap used by Tanaka et al., where parallel ion strings with different RF configurations, leading to different string distances, were demonstrated. We extend that work by adding segmented DC electrodes, which is indispensable for a scalable design and requires multilayer fabrication techniques (described in Section 3.2). The segmentation of the DC rails is also essential to investigate the core functionality of our approach: nearest neighbor interactions within the ion lattice in two spatial dimensions and a configurable lattice connectivity. In ref. [28], different RF amplitude values have been realized using mechanically tuned capacitors. In contrast, the realization of entangling operations in the twin trap design requires to dynamically adjust the RF amplitudes. Dynamic control can be achieved using two phase-stabilized RF resonators; a prototype of such an electrically tunable resonator that can be operated at cryogenic temperatures is described in ref. [49]. We note that the number of required RF resonators does not scale with the size of the trap array (see the section on RF shuttling in Appendix C).

### 3.1. Trap Simulation

We demonstrate the functionality of the twin-trap design by trap simulations, considering $^{40}\text{Ca}^+$ ions. First, we analyze the trap confinement in the default configuration of a rectangular lattice with $2 \times 9$ sites and trap spacings $s_x \approx 105\,\mu\text{m}$ and $s_z \approx 306\,\mu\text{m}$. Second, we characterize an independent axial translation process where the two adjacent DC multipoles are shifted continuously over one lattice period relative to each other. Such translations are a key requirement for the envisioned configurable lattice connectivity. Third, we simulate tuning of the trap spacings down to values $s_x = 40\,\mu\text{m}$ and $s_z = 50\,\mu\text{m}$, respectively, giving rise to a motional coupling rate between single ions in adjacent sites of $\Omega_c \gtrsim 2\pi \times 1\,\text{kHz}$ in both directions. For all simulated configurations, we obtain suitable trapping parameters, that is, secular...
frequencies on the order of 1 MHz, a trap depth of several tens to hundreds of meV, and required voltages of $U_{RF} \approx (100–400)\; V$ at RF and a few to a few tens of V DC.

3.1.1. Default Trapping Configuration

In the default trapping configuration, the inner and outer RF rails are set to the same RF voltage and the DC voltages are applied periodically across all DC segments, with a mirror symmetry between the left and right linear traps. Details on the calculation of DC voltage sets are given in Appendix A. The total trapping potential $\Phi$ in this configuration is shown in Figure 4. The potential has 18 individual trapping sites that are arranged in two columns along the two RF nulls, forming a rectangular lattice with trap spacings $s_x = 306\; \mu m$ and $s_y = 105\; \mu m$ (the sites at $|z| \approx 1500\; \mu m$ are not confined). The ion-surface separation is $d \approx 120\; \mu m$. An RF voltage of $U_{RF} = 142\; V$ at $\Omega_{RF} = 2\pi \times 23\; MHz$ yields a stability factor $q = a_0 \sqrt{8/\Omega_{RF}} \approx 0.4$, where $a_0$ is the radial frequency in absence of DC fields (details of the determination of RF parameters are given in Appendix A). The DC voltages for axial confinement are on the order of 1 V and give rise to an axial frequency $\omega_z = 2\pi \times 1.0\; MHz$. The DC confinement leads to a splitting of the radial frequencies, $\omega_{r1,2} = 2\pi \times (3.1, 3.3)\; MHz$, and causes a tilt $\theta_r = 41.2^\circ$ of the radial modes with respect to the vertical direction $y$. The tilt allows for almost equal laser cooling conditions for both radial modes, assuming laser beam propagation parallel to the trap surface. The axial mode is aligned with the $z$-axis, $\theta_z = 0$. The trapping sites are separated from each other by multilayer barriers $U_{0,\text{twin}}^{(0)} = U_{0,\text{twin}}^{(1)} = 59\; meV$ along the $z$-direction and the RF barrier $U_0 = 48\; meV$ along the $x$-direction. The barrier $U_0 = 102\; meV$ defines the global trap depth for ions in radial direction. These trap depths are significantly higher than the depths in other ion-lattice processors, and allow for an operation of the trap at room temperature. Deviations in the trapping parameters across the lattice due to finite-size effects are relatively small, with variations of the secular frequencies of about 10 kHz and of the radial mode tilt $\theta_r$ by about 5°. The biggest deviations are found at the outermost sites, $z \approx \pm 1230\; \mu m$, where the trap depths $U_0$ and $U_{\text{twin}}$ are reduced by about 25%. The outermost sites are also slightly displaced from the RF null leading to a residual RF electric field $E_0 \approx 730\; V/m$ in the laser plane ($xz$). This field causes excess micromotion with a micromotion modulation index $\beta = k z_{\text{max}} \approx 0.73$ [55] where $z_{\text{max}}$ is the micromotion amplitude and $k$ is the wavenumber of the $729\; nm$ laser beam driving the $4^2 S_{1/2} \leftrightarrow 3^2 D_{3/2}$ qubit transition in $^{40}\text{Ca}^+$. For the next inner trapping sites, $z \approx \pm 920\; \mu m$, the shift off the RF null is already notably smaller, with $E_0 \approx 270\; V/m$ and $\beta \approx 0.27$. These finite size effects result from the finite lengths of the RF rails and the fact that DC fields calculated for the central sites are non-ideal for sites at the trap edges. In future trap designs, such effects could be reduced by increasing the number of independent DC segments and by elongating the RF rails.

3.1.2. Independent Axial Translations

One of the goals of the twin trap is to demonstrate a configurable ion lattice connectivity, for example, switch from a rectangular to a triangular lattice. This requires that ions in the left and right linear traps can be moved relative to each other along the trap axis $z$ by at least one lattice period $s_z$. The ions in each linear trap are confined in DC multiwell potentials created by the periodic assignment of voltages to the DC segments. The basic principle of independent axial translations in this setup is illustrated in Figure 5a.

Grouping the DC electrodes in eight groups (six periodically repeating segments and two edge electrodes), as indicated by the different segment colors, we calculate voltage sets that simultaneously create axial confinement for two trapping sites at axial positions $z_0^{(0)}$ and $z_0^{(2)}$ in the left and right RF null, respectively (details in Appendix A). The periodicity of the voltages assigned to the DC segments then creates multilayers with trapping sites at $z_0^{(0)} \pm ms_z$, where $m = 0, 1, 2, \ldots$ is an integer number. To
The trap depths, values for electrodes DC1l and DCE1, are on the order of (1–10) V. For electrodes DC1l and DCE1, the secular frequencies shown in Figure 5d, maintain the nominal value of $\omega_z = 2\pi \times 1$ MHz. The axial frequency, shown in Figure 5d, maintains the nominal value of $\omega_z = 2\pi \times 1$ MHz with high accuracy for all pairs of positions. The radial modes (Figure 5e,f) show a variation of $\approx 10\%$ across the full parameter space. Other trap parameters (not shown) show slight variations as well. For instance, the radial mode tilt relative to the $y$-axis varies between $\theta_r \approx 30^\circ$–$40^\circ$. For the trap depths, values $U_0$, $U_{\text{low}} > 48$ meV, and $U_0 > 98$ meV are maintained, similar to the default configuration. More information is given in ref. [49]. We note that one can choose the axial frequencies $\omega_z^{(l)}, \omega_z^{(r)}$ independently, even to the point that one multiwell is switched off. However, trap depths are maximized when both multiwells are operated with similar $\omega_z$.

Any trajectory through the simulated parameter space $(z_0^{(l)}, z_0^{(r)}) \in [-s_z/2, +s_z/2]^2$ corresponds to a specific axial translation process. The ability to maintain the multiwell confinement for the entire parameter space demonstrates that translation processes with arbitrary multiwell positions are possible. Furthermore, the simulation of such a wide range of control parameters has the advantage that promising parameter space trajectories, for instance those with a minimal variation in secular frequency or mode tilt, can be quickly identified. However, the approach does not deliver a time-dependent voltage sequence that implements a specific temporal dependence $z_0^{(l)}(t), z_0^{(r)}(t)$ of the well positions. Such voltage sequences can be engineered in various ways. Typically, the aim is to maintain low motional excitation during the shuttling (adiabatic transport) [58,59] or to cancel excitations at the end of the sequence (diabatic transport) [60,61]. The full parameter scan presented here may serve as a starting point for the calculation of such sequences.

We emphasize that the grouping of DC segments significantly reduces the required number of DC control voltages for axial translation processes. In the present design, only eight control voltages are needed to independently move the two multiwells over arbitrary distances. Other adjustments of the trapping potential can be realized using additional groups of segments, foremost the independent segments in the axial interaction zone that allow one to reduce the trap spacing $s_z$ (see next section). In future designs, one could add even more DC segments to improve the control of the trapping potential at individual sites, for example, for micromotion compensation and secular frequency adjustments.

### 3.1.3. Adjustment of Trap Spacings

The creation of entanglement between ions in adjacent lattice sites requires a reduction of the trap spacings to enhance the coupling rate $\Omega_z$. Along the $x$-direction, the trap spacing $s_x$ is reduced by attenuating the RF voltage $U_{RF}^{(l)}$ on the inner RF rail relative to the voltage $U_{RF}^{(o)}$ on the outer RF rails. Figure 6 shows the trapping potential in such an “attenuated RF” configuration for a reduced trap spacing $s_x = 40 \mu$m. The axial multiwell confinement is preserved for all 18 trapping sites with an axial frequency $\omega_z = 2\pi \times 1$ MHz. The corresponding motional coupling rate for two $^{40}$Ca$^+$ ions in adjacent trapping sites across the...
RF barrier is $\Omega_z = 2\pi \times 1.4 \text{ kHz}$ (cf. Equation (1)). The RF double well potential, shown in the inset (Figure 6b), is well defined with a radial barrier of $U_b = 8.5 \text{ meV}$. The required RF voltages in this configuration are $U_{RF}^{(0)} = 296 \text{ V}$ and $U_{RF}^{(w)} = 372 \text{ V}$ with a stability factor $q = 0.4$, identical to the default configuration. The increase of the voltage $U_{RF}^{(w)}$ on the outer rails, required by the decreased efficiency of the trap, significantly improves the trap depth to $U_b = 702 \text{ meV}$. Other trap parameters are similar to the default configuration. The radial frequencies are $\omega_{r,1}, \omega_{r,2} = 2\pi \times (3.1, 3.3) \text{ MHz}$, the multiwell barrier is $U_{\text{max}} \approx 60 \text{ meV}$. The axial mode remains aligned with the $z$-axis, $\theta_z = 0$, and the radial mode tilt is $\theta_r = 10.2^\circ$. The DC voltages required to sustain the axial multiwell potential remain on the order of 1 V. We note that the trap spacing $s_z$ slightly differs along the trap axis, with values $s_z = 40 \mu\text{m}$ at the trap center, $z = 0$, and $s_z \approx 43 \mu\text{m}$ at the outermost sites, $z \approx \pm 1200 \mu\text{m}$. The difference in trap spacing is caused by finite size effects in the trap and leads to a variation in coupling strength of about $\Delta \Omega_z \approx 2\pi \times 0.3 \text{ kHz}$. The finite size effects could be decreased in future designs (see section 3.1.1).

Along the axial direction, the trap spacing $s_z$ can be reduced in the axial interaction zone at the trap center where the DC island electrodes have a finer segmentation. Ions outside the interaction zone remain in a periodic DC multiwell potential as in the default configuration. Figure 6c shows the confining potential for a configuration where the axial distance in the interaction zone is reduced to $s_z = 50 \mu\text{m}$; Figure 6d shows a magnified view of the two central sites forming a double well. These sites have radial frequencies $\omega_{r,1}, \omega_{r,2} = 2\pi \times (3.1, 3.3) \text{ MHz}$ identical to the default configuration. The axial mode has a frequency $\omega_z = 2\pi \times 0.91 \text{ MHz}$ and is tilted by $\theta_z = 8.0^\circ$ relative to the $z$-axis (currently, $\theta_z$ is an unconstrained parameter, which could be improved in future designs by adding additional DC electrodes). The central sites are separated from each other by an axial double well barrier $U_{b}^{(m)} = 1.1 \text{ meV}$, shown in (Figure 6e). The expected motional coupling between single $^{40}\text{Ca}^+$ ions in these sites is $\Omega_z = 2\pi \times 1.5 \text{ kHz}$, (cf. Equation (1)). The axial frequencies in the two central sites can be tuned independently. Micromotion compensation, however, is limited to shifting both sites simultaneously due to the small axial separation $s_z = 50 \mu\text{m}$. On the other hand, given that $s_z$ is substantially smaller than the ion-surface distance $d = 120 \mu\text{m}$, stray fields should be relatively homogeneous across the two sites. Due to the condition $s_z < d$, the double-well potential in the axial interaction zone is not created efficiently, and up to 34 V must be applied to the central DC segments. The outer 16 trapping sites, $|z_{\pm m}| \geq 459 \mu\text{m}$, are maintained by the periodically connected DC segments with trapping parameters similar to the default configuration. We note that the configuration with reduced axial distance (Figure 6c) can be seamlessly transformed to the default configuration in Figure 4 using a two-stage shuttling process. In the first step, the initial separation $s_z = 50 \mu\text{m}$ between the innermost sites is increased to $306 \mu\text{m} = 3l_{DC}$, realizing a multiwell configuration with constant lattice spacing across the entire length of the chip. The second step then uses an axial translation of the ion lattice to shift the central multiwell site into the origin at $z = 0$.

### 3.2. Trap Fabrication

The linear twin-trap design requires multiple metal layers and vertical interconnect access (via) due to the presence of island-like electrodes. The fabrication is carried out at the industrial facilities of Infineon Technologies in Villach, Austria. In general, our fabrication is similar to the CMOS foundry processes recently used for ion traps. However, while typical CMOS processes are set up for low-voltage logic applications, our processes are optimized for high power and high current applications more suited for ions traps. We also employ a dedicated workstream for the trap fabrication and are therefore not affected by the requirements of other technologies on the same wafer. Established design rules.
Figure 7. Main fabrication steps, shown for a vertical interconnect access (via) between metal layers 2 and 3. (a) Thermal oxidation of the silicon substrate. Deposition of (b) metal 1, (c) inter-metal-oxide (imox) 1, (d) metal 2, (e) imox 2, and (f) metal 3. All layers are structured by optical lithography and subsequent etching.

Continuous process monitoring, inline testing, and analysis capabilities provide high precision and reproducibility of the devices. For the fabrication of a prototype version of the linear twin-trap, 90 process steps were applied on top of a 725 μm thick silicon substrate [64] to produce six main functional layers as sketched in Figure 7: First, a 1300 nm thick SiO₂ layer is created by thermal oxidation of the Si substrate. This bottom oxide has low defect density and low interface roughness and serves as electrical insulation between substrate and the metal 1 layer. Subsequently, three metal layers are deposited, separated by two 2200 nm thick inter-metal oxide layers (imox). The 750 nm thick metal 1 layer provides i) shielding of the substrate from RF fields and lasers [63] and ii) shielding of the ion from charge fluctuations in the substrate. The 1000 nm thick metal 2 layer is mainly used for routing of the island-like electrodes to the bonding pads. Metal 3 has a thickness of 2000 nm and defines the trap electrodes.

All metal layers are made from AlSiCu, an alloy consisting mainly of aluminium. 1% silicon and 0.5% copper are included to suppress eutectic mixing with the silicon substrate and to increase the resilience to high currents, respectively. The metalization for electrodes and routing has to be low-ohmic in order to minimize RF pickup voltages on the DC electrodes, to minimize Johnson noise, and to minimize heating of the RF rails by capacitive loading currents during trap operation. The imox layers consist of SiOₓ, x ≈ 2, created by low-temperature plasma deposition since the thermal budget of AlSiCu is limited to a maximum temperature T_{max} ≈ 400 °C.

Standard optical lithography followed by etching is performed to define the structures within each layer. Vias between the metal layers are defined by etching a funnel-shaped aperture into the separating imox layer which guarantees reliable coverage of the vias’ sidewalls by the upper metal. The structuring of the imox layers is optimized using a focus exposure matrix. In order to guarantee process stability, in-line data of layer thicknesses, critical dimensions, reflectivities, and overlay precision are measured and recorded automatically.

After mechanical dicing into individual chips, electrical analysis (resistance and DC breakdown measurements at room temperature and T ≈ 20 K) as well as physical analysis (inspection of cross sections) are performed for quality control. The cross section of a via between metal 2 and 3 is shown in the scanning electron microscope (SEM) image in Figure 8. In order to provide high material contrast, the sample has been cut and polished followed by a 10 s exposure to hydrofluoric acid which etches a few nanometers of SiO₂ and emphasizes the material boundary of SiO₂. Finally, the sample is sputter-coated with about 2 nm of palladium to maximize the total contrast in the SEM image. The cross section confirms the reliable via connection between metal 2 and 3.

A microscope image of the full prototype device is shown in Figure 9a. The 80 trap electrodes (bright) in the metal 3 layer are separated by 9 μm-wide gaps (dark) and are connected to the bonding pads on the left and right sides of the chip. Vias and traces in lower layers are visible due to the surface topology of the chip. Figure 9b shows a magnified view of the island-like DC segments DC1, DC2, and DC3 in one of the trap quadrants. Every third segment is connected to the same lead on metal 2, as required for the creation of DC multiwell potentials and axial translations. The color code in Figure 9c and in the cross...
Leads on metal 2 (blue) connect to the DC segments with two vias (yellow) per segment. Additional shield leads (red) on metal 2 reduce the parasitic capacitance between the segment leads and the adjacent RF electrodes. The shields are connected to the metal 1 ground with vias (green). The dashed arrow marks the z-position of the schematic cross section shown in (d). (e) Magnified view of the trap center with the axial interaction zone. (f) The same view with a color overlay. The central DC electrodes are routed underneath the RF rail through metal 1 leads (blue). A grounded shield (hatched red) on metal 2 reduces the parasitic capacitance between the DC leads and the RF rail. The dashed arrow marks the z-position of the schematic cross section shown in (g).

section (Figure 9d) illustrates the routing to the DC segments on metal 2. RF-pickup on the segments is minimized by two measures: First, vias at both ends of each segment reduce the lead resistance $R_{\text{lead}}$, since the metal 2 and metal 3 layers are routed in parallel. Within the segmented rail region, the calculated reduction of the lead resistance is about 27%. Second, additional shield electrodes connected to GND reduce the parasitic coupling capacitance $C_p$ between the DC segments and the adjacent RF electrodes. We quantify the shielding with finite element simulations of a trap cross section: The presence of the metal 1 GND layer reduces $C_p$ by about 92%; the grounded shields on metal 2 lead to an additional reduction of about 19%. To further minimize the coupling capacitance, crossing of DC leads below the RF rails is avoided whenever possible. Figure 9e shows a magnified view of the axial interaction zone at the trap center. The routing to the individually connected central DC segments has to cross the RF rails, as shown in Figure 9f,g. Therefore, the routing is moved to the metal 1 layer to make room for a shield electrode on metal 2. This minimizes RF-pickup on the lines while maintaining the screening of the Si substrate from laser light. From finite element simulations, we estimate a parasitic coupling capacitance to the RF rails of $C_p \lesssim 0.01$ pF for any DC electrode.

The trap chips are produced on wafers with a diameter of 200 mm (8"), holding more than 700 chips. Multiple trap geometries are fabricated simultaneously. In addition to the design with ion-surface separation $d = 120 \mu$m described in this article, a slightly adapted geometry with $d = 80 \mu$m is on the wafer. Additionally, both electrode geometries are realized in two versions. In one version, metal 1 is unstructured, apart from the routing to the central DC segments. The continuous metal
Table 1. Resistivity $\rho$ of the three metal layers at $T \approx 20$ K.

| Layer         | $\rho$ [Ω m] |
|---------------|--------------|
| Metal 3       | $2.41(\pm0.03) \times 10^{-9}$ |
| Metal 2       | $2.58(\pm0.02) \times 10^{-9}$ |
| Metal 1       | $2.54(\pm0.01) \times 10^{-9}$ |

Table 2. Intermetallic via resistances $R_{\text{via}}$ at $T \approx 20$ K.

| Via type                  | $R_{\text{via}}$ [mΩ] |
|---------------------------|-----------------------|
| Metal 3 to metal 2        | $2.70(\pm0.02)$       |
| Metal 2 to metal 1        | $6.52(\pm0.03)$       |
| Metal 3 to metal 1        | $4.94(\pm0.04)$       |

1 layer ensures shielding of the substrate from laser light and reduces the penetration of RF fields into the substrate. In a second version, about 79% of the metal 1 layer is removed below the RF electrodes. This trades substrate shielding for a lower capacitance of the RF lines ($\approx 11$ pF instead of $\approx 29$ pF, estimated from a parallel plate capacitor model), allowing for a larger voltage gain of a step-up resonator, provided the substrate has negligible RF loss.

The wafer layout also contains structures dedicated to the electrical testing of the resistivity of the metal layers and of the resistances of the intermetallic vias. These quantities are used to estimate the amount of RF pickup and Johnson noise on the trap electrodes. The layer resistivities and via resistances are determined in a 4-wire measurement at $T \approx 20$ K. The results are listed in Tables 1 and 2. We find reproducible values of the AlSiCu bulk resistivity of $\rho \approx (2.4–2.6) \times 10^{-9}$ Ω m, which is comparable to other low-resistivity alloys of aluminium at $T = 20$ K. The via resistance depends on the aspect ratio of the metallized vias and the distance between the connected metal layers. Vias connecting metal 1 to metal 3 are realized with one metal 2 to metal 3 via and two metal 1 to metal 2 vias in parallel to reduce the resistance. All via resistances are on the order of a few mΩ, demonstrating a good electrical connection across metal layers.

From the measured resistances, we estimate the amount of Johnson noise on the trap electrodes and the corresponding heating rate for a trapped ion (details in Appendix B). The dominant contribution to the Johnson noise seen by an ion comes from the metal 2 leads for the periodically connected DC segments. These leads have a resistance of $R_{\text{lead}} \approx 0.46$ Ω at $T \approx 20$ K; the via resistances can be neglected. The axial ion heating rate caused by Johnson noise across $R_{\text{lead}}$ is $\Gamma_h \approx 0.015$ phonons/s, calculated for a $^{40}$Ca$^+$ ion with an axial frequency of $\omega_x = 2 \pi \times 1$ MHz (in radial direction the heating rate is on the same order of magnitude). Such a low heating rate is negligible for all practical purposes.

The RF pickup voltage $U_p$ on the DC electrodes is estimated from an electrical model, considering the electrodes’ grounding in the RF domain (details in Appendix B). Large pickup voltages can induce significant RF electric fields at the ion position, which in turn result in excess micromotion that cannot be compensated. We estimate a very small amount of RF pickup $|e_p| = |U_p/U_{RF}| \approx 1 \times 10^{-6}$, where $U_{RF}$ is the applied RF voltage at a frequency $\Omega_{RF} = 2\pi \times 25$ MHz. Excess micromotion from the corresponding RF electric fields should therefore be negligible.

The maximum required RF voltages on the trap are about $U_{RF} = 400$ V, needed in the configuration with reduced trap spacing $s_{\text{t}}$ between the two linear traps (cf. Section 3.1.3). For a reliable trap operation, the dielectric imox layers need to withstand such RF voltages without electrical breakdown. We measure the DC dielectric breakdown voltage between metal layers 2 and 3 directly on the d = 120 μm prototype chips at room temperature and in vacuum. From a set of ten devices, we observe dielectric breakdown voltages of 800 V < $V_{BD}$ < 1000 V. This is in reasonable agreement with the typical dielectric strength 5.6 MV cm$^{-1}$ of sputter-deposited SiO$_2$ given the 2 μm thickness of the imox layers. Furthermore, the measured $V_{BD}$ is well above the required voltage of 400 V assuming similar dielectric breakdown mechanisms for DC and RF.

3.3. Trap Characterization

We have performed tests of the fabricated linear-twin traps by means of ion measurements with $^{40}$Ca$^+$ ions. The tests include trapping and axial translations of multiple ions, as well as a characterization of stray electric fields and heating rates. The experiments are performed in a closed-cycle cryostat with a base temperature of $T \approx 10$ K, while the ion trap is at an operation temperature of $T \approx 50$ K. The elevated temperature of the trap is due to RF absorption in the Si substrate at the location of the RF rails’ bonding pads, where there is no grounded shield layer on metal 1. This heating effect could be significantly reduced in future designs by extending the metal 1 shield layer to the bonding pads, thereby inhibiting the RF field penetration into the substrate while adding only slightly to the trap capacitance.

$^{40}$Ca$^+$ ions are produced from a neutral atom flux by a two-step photoionization process using overlapped laser beams at 422 and 379 nm wavelength. In order to cool the ions into the motional ground state, we use Doppler and resolved sideband cooling techniques. The $4S_{\frac{3}{2}} \leftrightarrow 4P_{\frac{3}{2}}$ dipole transition at 397 nm is used for Doppler cooling and detection. The $4S_{\frac{1}{2}} \leftrightarrow 3D_{\frac{3}{2}}$ quadrupole transition at 729 nm is used for resolved-sideband operations and spectroscopy. Additional lasers at 866 and 854 nm are employed to repump population from the D states back to the P levels. The 397, 866, and 854 nm beams are shaped by a set of cylindrical lenses to obtain highly elliptical beams with a beam waist $w_0 \approx 900$ μm in the horizontal plane and (20–30) μm in the vertical direction. These elliptical beams are used to cool and image ions in multiple lattice sites simultaneously, as well as during ion shuttling. All other laser beams are circular and address a single trapping site at a time. For trap operation, we apply an RF amplitude $U_p \approx 180$ V at 25 MHz to all three RF rails, resulting in radial frequencies $\omega_x \approx 2 \pi \times (2–3)$ MHz. Axial multiwell confinement with $\omega_z \approx 2 \pi \times 1$ MHz is achieved by applying DC voltages on the order of 1 V, using the segment connectivity shown in Figure 5a. The periodic assignment of voltages to the DC segments is extended across the entire length of the trap chip to allow for seamless axial translations of ions in the left and right linear trap. However, due to a short in one of the cables of the cryostat, electrodes DC2l and DC2r had to be
connected to the same supply line. Thus, the freedom of moving the two chains independently was limited in the experiments.

In a first experiment, we investigate the ability of the twin-trap to confine ions in different lattice configurations. Figure 10 shows images of ions, simultaneously trapped in multiple trapping sites. The ion-surface separation is \( d = 120 \mu \text{m} \). In Figure 10a, six ions are trapped in a rectangular lattice with trap spacings \( s_x \approx 100 \mu \text{m} \) and \( s_y \approx 300 \mu \text{m} \). Ions at the center (sites 1 and 2) are brighter than the ions further out, mainly due to a small tilt of the major axis of the elliptical imaging beam relative to the trap surface and partly due to different micromotion conditions. Figure 10b shows five ions trapped in a triangular lattice configuration, which results from the rectangular lattice in Figure 10a by a shift of the left and right DC multiwells by a quarter lattice period in opposite directions. To trap ions in multiple lattice sites, we employ a combination of two loading techniques. First, the two photoionization beams at 422 and 379 nm are sequentially directed to the trapping sites where single ions are to be trapped. Loading ions in some of the trapping sites was difficult, which we attribute to stray electric fields. These sites were filled using shuttling of ions from adjacent sites.

We further demonstrate shuttling of an entire ion lattice: In Video S1, Supporting Information, we show a simultaneous translation of a rectangular lattice of four ions over a distance of one lattice period, \( s_x = 306 \mu \text{m} \). While all ions remain trapped during the transport, three of the four crystallized ions temporarily melt. This mainly happens due to an asynchronous update of the different DC voltages provided by the supply; in parts also due to a variation of the stray electric field. We emphasize that during the shuttling we applied only a constant, global micromotion compensation field. The successful transport thus indicates a relatively constant stray electric field over the entire shuttling distance of 600 \( \mu \text{m} \). A total of only eight DC control voltages is imposed onto a background image of the trap electrodes (gray scale), obtained by illumination with a 395 nm LED source. (a) Trapping of six ions in a rectangular lattice configuration. The axial ion spacing in the left and right multiwells is \( s_y \approx 300 \mu \text{m} \), and the spacing between the two multiwells is \( s_x \approx 100 \mu \text{m} \). (b) Trapping of five ions in a triangular lattice configuration. The ion spacing, nominally identical to (a), is not perfectly uniform due to stray electric fields.

Figure 10. Images of ions simultaneously trapped in different lattice configurations. The images of ion fluorescence at 397 nm (blue-white) is superimposed onto a background image of the trap electrodes (gray scale), obtained by illumination with a 395 nm LED source. (a) Trapping of six ions in a rectangular lattice configuration. The axial ion spacing in the left and right multiwells is \( s_y \approx 300 \mu \text{m} \), and the spacing between the two multiwells is \( s_x \approx 100 \mu \text{m} \). (b) Trapping of five ions in a triangular lattice configuration. The ion spacing, nominally identical to (a), is not perfectly uniform due to stray electric fields.

Table 3. Stray electric field components \( E_x, E_y \) at different trapping sites.

| Site | \( E_x [\text{V m}^{-1}] \) | \( E_y [\text{V m}^{-1}] \) |
|------|-----------------|-----------------|
| 4    | 174 (15)        | \( \approx 60 \) |
| 2    | \(-640 (30)\)   | \( \approx 60 \) |
| 5    | 116 (10)        | \( \approx 60 \) |

After several weeks of trap operation, we observed a substantial change of the stray electric field, resulting in ion loss during shuttling operations. Using a single ion as a probe, we characterized the spatial variation of the stray electric field at sites 4, 2, and 5 (cf. Figure 10a). The measurement is done by adjusting the micromotion compensation voltages to maximize ion fluorescence at 397 nm close to the atomic transition frequency. The stray field is then given by the compensation field, with opposite sign. The data, listed in Table 3, reveal that the stray field component \( E_x \) in the central site 2 has a five times larger amplitude than in sites 4 and 5 and is pointing in opposite direction. The component \( E_y \) is significantly smaller than \( E_x \) and approximately constant for all sites. The precision of the measurement of \( E_y \) is lower than that of \( E_x \). The 397 nm beam used to detect stray-field induced micromotion propagates in the z-plane, parallel to the trap surface, and is not sensitive to micromotion in the y-direction. One axis of the RF quadrupole field is tilted by only \( \alpha \approx 22^\circ \) from the y-direction.

In addition, ions could be loaded in sites 1 and 2 at the chip center without applying axial confinement. The residual axial frequency \( \omega_z \approx 2 \pi \times 600 \text{ kHz} \), independent of the applied RF voltage, stayed approximately constant over the whole trap operation period. As zones 1 and 2 where often used for ion loading, this stray confining field may have been caused by laser-induced charges or by inhomogeneous contamination arising from the loading process.\(^{76–79}\)
Finally, heating rate measurements were performed to further explore the potential of the linear twin-trap prototype for ion-ion coupling. The measurements were taken in sites 1, 2, and 3 (cf. Figure 10a) using the sideband-ratio method. \[^{[75]}\] The results are listed in Table 4. The measured values, obtained at axial frequencies \(\omega_z \approx 2\pi \times (1.2-1.5) \text{ MHz} \), are in a range \(\Gamma_z \approx (100-500) \text{ phonons per second} \) for the three trapping sites. Given the targeted ion-ion coupling rate \(\Omega \approx 2\pi \times 1 \text{ kHz} \), these heating rates should allow the observation of ion-ion coupling on a few quanta level. \[^{[21,22]}\] However, to harness the coupling for spin-spin interactions or high-fidelity entangling operations between ions in adjacent sites, a significantly lower heating rate would be required. A further characterisation is necessary to determine whether the measured heating rates are limited by technical noise that could be filtered out or by surface noise. In fact, surface contamination is a possible reason for the high heating rates. While the trap chip has been cleaned of photoresist residues and dicing debris at the Infinenon facilities, no further cleaning steps were done prior to loading into the vacuum chamber. Additional chemical cleaning or ex situ surface treatments \[^{[60,61]}\] could lower the observed heating rates. Also, a change in electrode material from AlSiCu to a noble metal might significantly reduce the experienced heating due to the absence of native oxide layers. \[^{[82]}\] We currently work on a new chip version with gold electrodes. Another option would be in situ cleaning of trap electrodes by argon ion bombardment, which has been reported to drastically lower the heating rate. \[^{[83,84]}\]

### Table 4. Ion heating rate at different trapping sites.

| Site | \(\omega_z/(2\pi)\) | \(\Gamma_z\) [phonons per second] |
|------|---------------------|----------------------------------|
| 1    | 1.45 MHz            | 288 (35)                         |
| 2    | 1.48 MHz            | 472 (50)                         |
| 3    | 1.24 MHz            | 131 (13)                         |

4. Conclusion

In summary, we have proposed, built, and operated a new design of an ion-lattice quantum processor based on 2D arrays of linear surface traps. A core aspect of our approach is the usage of ion-shuttling operations in two spatial dimensions that enable a dynamical configuration of the ion lattice in terms of lattice connectivity and ion-spacing. The latter enables tunable interactions between ions in adjacent lattice sites. We have shown the feasibility of our approach by means of detailed trap simulations of a simplest-instance version, consisting of two parallel linear traps with 2 × 9 trapping sites. The simulated trapping potentials facilitate interaction strengths between ions in adjacent sites in the kHz range, while maintaining a moderate ion-surface separation \(d = 120 \mu\text{m}\) to keep the electric field noise low. We demonstrate the scalability of this design with additional simulations of an array with 10 × 10 sites, shown in Appendix C. We have built several versions of the 2 × 9 array in an industrial facility using multilayer microfabrication. The employed fabrication processes are compatible with further scaling-up the array size where the growing number of island-like electrodes will require a more dense routing: Up to six metal layers can readily be realized, and even more layers are possible by adding planarization steps. In the future, our CMOS fabrication process could also be extended to include waveguide structures for integrated optical addressing of single ions and pairs of ions.\[^{[46]}\]

We have experimentally demonstrated the basic operability of a prototype device with 2 × 9 trapping sites, showing simultaneous trapping of ions in multiple lattice sites. DC voltage-controlled shuttling, and resolved-sideband operations (heating rate measurements). The cooling beams were elliptical to cover multiple trapping sites at once; in the future, steerable beams or multiple beams \[^{[85]}\] may be employed to reduce the optical power needed. We have further demonstrated the ability to configure the ion lattice, showing trapping in a rectangular lattice and a triangular lattice configuration and translation of an entire ion lattice by one lattice period. This configurability is only possible in a linear trap array and is one of the principle points of our design. For shuttling along the trap axis, we have employed a periodic voltage assignment to the trap’s DC segments, which allows one in principle to axially transport ion sub-lattices over arbitrary distances using only a small number of DC control voltages. The shuttling speed, being currently limited by the stable DC supply, could in the future be increased by orders of magnitude using a faster supply.\[^{[58,60,61]}\] Axial translations can also be employed as a technique for fast sequential loading of an entire ion lattice: Ion loading takes place at one dedicated site per linear trap and loaded ions are subsequently shuttled together with all other ions in the multilowell to the adjacent site using axial translations (cf. Section 3.1.2). This technique does not require ionization beams to be steered across the array and could be combined with a pre-cooled source of atoms to further increase the loading rate.\[^{[29]}\] A draw-back of the periodic voltage assignment is the limited control of the trapping potential at different lattice sites. Lattice translations in our prototype design using only a global micromotion compensation field were successful at first, but were eventually limited by a spatially-varying stray electric field. Indeed, we find the vulnerability to stray charges to be the biggest limitation of our prototype device. This problem can be tackled in future chip versions: First, the creation of stray charges on exposed dielectrics can be inhibited by reducing the electrode gap size (currently 9 \(\mu\text{m}\)) and by using a noble metal for the top metal layer, for example, gold. Second, the electrode design can be adapted to allow for a larger number of control electrodes for independent micromotion compensation in more lattice sites. Another limitation of our prototype device is the relatively high heating rate \(\Gamma_z \approx (100-500) \text{ phonons per second} \) at \(\omega_z \approx 2\pi \times 1.5 \text{ MHz} \), which is only slightly smaller than the targeted ion-ion coupling rate \(\Omega \sim 2\pi \times 1 \text{ kHz} \). Such a heating rate does not allow for the ion–ion coupling to be used for quantum simulations. We emphasize that the heating rate in our setup is not limited by Johnson noise from the trap electrodes as the electric field noise estimates based on the resistance measurements show. We have discussed several means to reduce the heating rate, particularly by changing the electrode material and by applying surface cleaning procedures.

### Appendix A: Calculation of RF and DC Voltages

The twin trap’s RF drive parameters are chosen in the following way: First, a maximally applicable RF voltage \(U_{\text{RF}} \approx 400 \text{ V} \) is assumed. In the configuration with reduced RF voltage on the
inner RF rail (Figure 6a), where the trap efficiency is decreased, the drive frequency $\Omega_{\text{rf}}$ is then set to yield a stability factor of $q = 0.4$. Keeping $\Omega_{\text{rf}}$ constant, the RF voltage $U_{\text{rf}}$ is then adjusted to achieve $q = 0.4$ in the default configuration (Figure 4).

For the simulation of DC multiwell confinement and ion shuttling, we use an algorithm that calculates DC voltage sets for axial confinement and micromotion compensation simultaneously at two arbitrary trapping positions $r_0^{(o)}$ and $r_0^{(l)}$ in the left and right RF null, respectively. This includes different axial trapping positions $z_0^{(o)} \neq z_0^{(l)}$. The voltage set for confinement at these two sites automatically creates additional sites with a spacing of 3 $\ell_{\text{DC}}$ along the trap axes due to the periodic assignment of voltages to the DC segments. Necessary conditions for a trapping site at position $r_0$ to be a vanishing axial electric field, $E_z(r_0) = 0$, and a positive curvature, $\frac{\partial^2 \phi(r_0)}{\partial z^2} > 0$. In addition, $r_0$ needs to be overlapped with the RF null, that is, $E_x(r_0) = 0$. The sets for micromotion compensation require control over the radial electric field components $E_r(r_0)$. A shift of the trapping position along $z$ can be realized by the axial field component $E_z(r_0)$. This amounts to eight field parameters (six electric field components and two curvatures) for the two trapping sites at $r_0^{(o)}$ and $r_0^{(l)}$. Let now $b$ be a vector of the desired eight field parameters. Further, let $x$ be the unknown vector of voltages applied to the set of DC electrodes that produces $b$. Then it holds $b = Ax$, where the entries in the square matrix $A$ are the contributions of the individual electrodes to the eight field parameters. These entries are determined by trap simulation. The unknown voltage set $x$ is then found by inversion of matrix $A$. This method only succeeds if $A$ is of full rank, which requires at least eight electrodes whose field and curvature contributions are linearly independent. For the simulations of trap confinement in the default configuration (Figure 4) and for the simulation of independent axial translations (Figure 5), the DC segments are grouped in eight independent electrodes, as shown in Figure 5a. For the simulation of confinement in the axial interaction zone (Figure 6), the segments are differently grouped, as shown in Figure A1. Here, the voltages on the electrodes are assumed to have a mirror symmetry along both the central RF rail and along the x-axis through the center of the trap. In this way, the control of two trapping sites, one at $z_0^{(o)}$ within the interaction zone and the other at $z_0^{(l)}$ in the outer region, is sufficient to create multiwells across the entire length of the trap. The position $z_0^{(o)}$ of the first site sets the reduced axial distance $\delta_z$ between the central trapping sites. The position $z_0^{(l)}$ of the second site controls the location of all the outer trapping sites, which have a fixed spacing given by the trap spacing $3\ell_{\text{DC}}$.

**Appendix B: Calculation of Johnson Noise and RF Pickup**

In this section, the estimates for the ion heating rate due to Johnson noise in the trap electrodes, as well as the magnitude of the RF pickup voltage on the DC electrodes are derived. For the estimate of the heating rate, we consider the leads for the periodically connected island electrodes on the metal 2 layer, which have by far the largest resistance on the trap chip. These leads have a maximal length between bonding pad and furthest DC segment of about $l = 3.56$ mm and a width of $w = 20 \mu$m, resulting in a resistance of $R_{\text{lead}} = l \rho_{\text{metal}}/(wd) \approx 0.46 \Omega$ at $T \approx 20$ K, where $l = 1000$ nm is the thickness of the metal 2 layer. The via resistances can be neglected. The amount of electric field noise created by this resistance at the position of a trapped ion $16^{[38]}$ $S_{\epsilon}^{(n)} = 4k_B T R_{\text{lead}}/\delta_z^2 = 1.06 \times 10^{-16}$ $\text{V}^2 \text{m}^{-2} \text{Hz}^{-1}$, where $k_B$ is the Boltzmann constant and $T = 20$ K. The characteristic distance of the segmented DC electrode, $\delta_z$, is found by trap simulation and has a maximal value $\delta_z = 2.19$ mm along the axial direction for all axial positions (for the radial directions, $\delta_z$ is at most about a factor 2 smaller). This electric field noise corresponds to an axial heating rate of $16^{[38]} \Gamma_{\epsilon}^{(n)} = Q^2 S_{\epsilon}^{(n)}/(4 M \hbar \omega_z) \approx 0.015$ phonons/s, where $Q$ and $M$ are the charge and mass of a $^{40}\text{Ca}^{+}$ ion, $\hbar$ is the reduced Planck constant and $\omega_z = 2\pi \times 1$ MHz is the ion’s axial frequency.

For the estimate of the RF pickup voltage on the trap’s DC electrodes, we consider the simplified electrical circuit in Figure A2. The RF drive voltage $U_{\text{rf}}$ is applied to the trap’s RF electrode (green box). The parasitic capacitance $C_p$ between the trap electrodes couples the DC electrode (blue box) to the RF electrode, leading to an RF pickup voltage $U_p$ on the DC electrode. The
value of $U_p$ depends on how well the DC electrode is connected to GND, $U_p = \epsilon_p U_{RF}$, with the complex RF pickup ratio

$$\epsilon_p = \frac{Z_{lead} + Z_C}{Z_{lead} + Z_{C_p} + Z_C}$$  \hspace{1cm} (A1)$$

and $Z_C = -i/(\Omega_{RF} C)$ being the impedance of a capacitance $C$ at frequency $\Omega_{RF}$. To give an upper bound on the pick up ratio $\epsilon_p$, we consider one of the periodically connected island electrodes which have the largest parasitic coupling capacitance $C_p$ and largest lead impedance $Z_{lead}$. We estimate the parasitic coupling capacitance $C_p \approx 0.01 \text{ pF}$ from finite element simulations of the trap geometry[86] (cf. Figure 9d). The lead inductance $L_{lead} \approx 0.2 \text{ nH}$ is calculated from the simulated capacitance matrix.[87] The lead resistance, calculated above, is $R_{lead} \approx 0.46 \text{ } \Omega$ and dominates the lead impedance $Z_{lead} = R_{lead} + i \Omega_{RF} L_{lead} \approx (0.46 + 0.03)i \Omega$ at the RF drive frequency $\Omega_{RF} = 2 \pi \times 25 \text{ MHz}$. The grounding capacitance $C_g \approx 330 \text{ nF}[88]$ is given by the capacitance of the low-pass filters used in our setup. These filters are located on a printed circuit board (PCB) within the cryogenic setup, only a few cm from the trap chip. Finally, assuming that the connection line impedance is dominated by the lead impedance $Z_{lead}$, we arrive at an upper bound for the RF pickup ratio of $|\epsilon_p| \approx 7.2 \times 10^{-7}$.

Appendix C: Simulation of a Linear Trap Array with 10 $\times$ 10 Trapping Sites

In this section, we show that the twin-trap design (Figure 3) can be extended to a larger number of parallel linear traps. For this, multiwell confinement and RF shuttling in a linear trap array with 10 $\times$ 10 trapping sites are simulated. DC shuttling along the axial direction is not simulated since this aspect is already covered by the studies in the twin-trap: confinement with reduced axial distance (Figure 6c) and independent axial translations of two adjacent DC multiwells with nine trapping sites each (Figure 5). It should be emphasized that the simulations presented here are intended only as a proof-of-principle study. The electrode geometry is not optimized and can be further improved.

The geometry of the simulated 10 $\times$ 10 trap array is shown in Figure A3. RF confinement in the radial ($xy$) plane is produced by parallel RF rails with alternating widths $w_e = 88 \mu m$ and $w_o = 70.4 \mu m$, referred to as even and odd RF rails, respectively, in what follows. A total of 15 RF rails leads to 14 parallel linear traps, out of which the innermost 10 linear traps are used for ion storage. The widths of the even and odd RF rails differ by about 20%. This leads to a tilt of the radial modes with respect to the trap normal in the presence of DC confinement, allowing for simultaneous laser cooling of all secular modes with laser beams parallel to the trap surface. The segmented DC rails have a width $w_{DC} = 79.2 \mu m$ and a segment length $I_{DC} = 74.8 \mu m$. Like in the twin-trap design, the segments are periodically connected, with the same voltage being applied to every third segment. This allows one to create DC multiwell confinement with a well period of $3 l_{DC} \approx 224 \mu m$.

Inhomogeneities of the RF potential across the array caused by edge effects are mitigated in three ways: First, an additional GND electrode at a distance $y = 1.0 \text{ mm}$ above the trap surface is introduced, which also increases the trap depth by roughly a factor 1.5, compared to a design without GND layer. A top GND electrode could be realized for instance with a glass plate coated with indium tin oxide (ITO) and mounted rigidly above the trap chip. ITO remains conductive and optically transparent at cryogenic temperatures.[89] Second, an additional pair of linear dummy traps is added at either side of the array. The 10 central linear traps used for the quantum register are thereby increased to 14 linear traps. Ions loaded accidentally in the outer dummy traps could be deterministically pushed out by using, for instance, suitable DC control fields on the outermost DC electrodes. Third, the width of the outermost RF rails is increased to $w_{RF} = 228.8 \mu m$. We note that the simplified geometry in Figure A3 only shows the minimum of DC electrodes necessary for creating a 2D ion lattice. For a realistic operation as ion-lattice quantum processor, a further segmentation of the DC rails would be necessary. In particular, control electrodes for stray electric field compensation (micromotion compensation) and for fine control of secular frequencies (and potentially mode orientations) would be required.

C.1. Multiwell Confinement

To simulate multiwell confinement, a voltage set for axial confinement is calculated for a single trapping site at the center of the array. Upon applying this set, the periodicity of the RF and DC electrodes automatically creates a rectangular array of trapping sites. DC voltages are applied to the DC segments as well as to the RF rails, in order to gain the required number of control parameters for axial confinement and micromotion compensation. In the default trapping configuration, an equal RF voltage $U_{RF}$ is applied to the even and odd RF rails and a DC voltage set for axial multiwell confinement is applied. The
total confining potential $\Phi$ in this configuration is shown in Figure A4. The cross sections in panels (a), (b) and (d) show a rectangular lattice of $14 \times 12$ trapping sites out of which the central $10 \times 10$ sites are to be used for ion storage. The additional sites at the trap edges are dummy sites. The ion-surface separation of the central $10 \times 10$ sites is about $d \approx 102 \mu$m. An RF voltage of $U_{RF} = 172$ V at $\Omega_{RF} = 2\pi \times 30$ MHz yields a stability $q$-factor of 0.4. The DC voltages for axial confinement are on the order of 1 V. The secular frequencies are $\omega_x = 2\pi \times 1.0$ MHz axially and $\omega_{x1}, \omega_{x2} = 2\pi \times (4.0, 4.4)$ MHz radially, with a radial mode tilt $\theta_r = 8.4^\circ$ with respect to the surface normal. The axial mode is aligned with the z-axis, $\theta_z = 0$. The axial multiwell barrier $U_{x0w} = 45$ meV, the RF barrier $U_{RF} = 116$ meV and the global trap depth $U_0 = 330$ meV all have high values, well above the average kinetic energy $E_k\approx 26$ meV of thermal gas molecules at room-temperature. The global trap depth $U_0$ is defined as the potential $\Phi$ at the position of the top GND layer, $y = 1$ mm. The inner $10 \times 10$ trapping sites show a very good homogeneity: The variation in ion-surface separation $d$ is about 1 $\mu$m. The stability $q$-factor varies within 0.404 and 0.409 for all sites. Variations in secular frequencies are about $4$ kHz axially and $30$ kHz radially. The radial mode tilt varies within $8.0^\circ$ and $13.1^\circ$, the axial mode tilt stays below $0.1^\circ$. Radial shift of the sites off the RF null are below $1$ $\mu$m. Variations in the trap depths are negligible.

C.2. RF Shuttling

Entanglement between ions in adjacent linear traps is facilitated by a reduction of the distance $s_x$ between adjacent RF nulls. This is achieved by reducing the RF voltage $U_{RF}$ on either the even or the odd RF rails. At a separation $s_x = 40$ $\mu$m, one calculates a motional coupling rate $\Omega_{m} = 2\pi \times 1.4$ kHz, using Equation (1) and assuming an axial frequency $\omega_z = 2\pi \times 1$ MHz. Once the reduced distance $s_x$ is reached, the axial mode frequencies of ions that are to be coupled are tuned into resonance using DC control fields; unwanted coupling, for example, between non-nearest neighbors is avoided by detuning the frequencies of these wells,[21–23] as outlined in Appendix E. The trap confinement in the reduced distance $s_x$ is shown in Figure A5. The cross sections in panels (a) and (d) show how the $14 \times 12$ trapping sites are rearranged upon attenuation of the RF voltage on the even and odd RF rails, respectively. In both configurations, the sites form pairs of columns such that for any trapping site a reduced distance $s_x \approx 40$ $\mu$m to either the adjacent site on the right or on the left can be realized.[89] The ion-surface separation is in both configurations about $d \approx 100$ $\mu$m, almost identical to the default configuration in Figure A4. In general, the ion-surface separation is practically unchanged during RF shuttling. The insets, Figure A5b,e, show a magnified view of the marked pairs of trapping sites. The double-well potentials connecting the two sites of each pair are shown in Figure 15c,f. In the two configurations, the RF voltage is either attenuated by about 59.4% on the even RF rails, or by 41.4% on the odd rails, relative to the respective other rail which is at $U_{RF} = 350$ V. The difference in required RF attenuation for the two configurations stems from the different RF rail widths. In either configuration, the axial multiwell confinement can be maintained using DC voltages on the order of 1 V with standard secular frequencies of $\omega_x = 2\pi \times 1.0$ MHz axially and $\omega_{x1}, \omega_{x2} = 2\pi \times (2.0–3.0)$ MHz radially. The axial mode remains aligned with the z-axis, $\theta_z = 0$, the radial mode tilt is increased to about $\theta_r \approx 35^\circ$. The reason for the smaller radial frequencies in comparison to the default configuration is the decreased trap efficiency, just as in the case of the twin-traps. For the simulations, a maximally applicable RF voltage $U_{RF} = 350$ V was assumed, limiting the stability $q$-values to 0.21 and 0.26, respectively. Likewise, the double-well barrier is limited to $U_{x0w} \approx 3.9$ meV and $U_{RF} \approx 6.1$ meV. The multiwell barrier $U_{x0w} \approx 35$ meV and the trap depth $U_0 = (192, 334)$ meV remain at large values.

Concerning the homogeneity of the central $10 \times 10$ trapping sites, the most notable variation exists in the reduced trap spacing $s_x$. For attenuation on the even RF rails, this distance changes from $s_x \approx 39$ $\mu$m at the central linear traps, $x \approx \pm 158$ $\mu$m, to $s_x = 44$ $\mu$m at the next pair of traps, $x \approx \pm 476$ $\mu$m. For attenuation on the odd RF rails, the distance changes from $s_x = 40$ $\mu$m at the array center, $x = 0$ $\mu$m, to $s_x = 39$ $\mu$m at the next pair of traps, $x \approx \pm 316$ $\mu$m, and further to $s_x = 35$ $\mu$m at the outer pair of traps, $x \approx \pm 632$ $\mu$m. The variation in trap spacing $s_x$ is caused by the edge effects of the trap array along the x-direction and limits the possibility of parallelized entangling operations across the entire lattice due to the difference in expected coupling rate $\Omega_x$. Edge
Figure A5. Trap confinement in the reduced RF configuration with \( s_z \approx 40 \mu m \), achieved by attenuating the RF voltage on the even RF rails (a–c), and on the odd rails (d–f). Panels (a) and (d) show cross sections of the total potential \( \Phi \) in the \( xz \)-plane, crossing the trapping site at \( r_0 = (139, 98, -112) \mu m \) and \( r_0 = (20, 101, -112) \mu m \), respectively. The color scale is non-linear, a quartic potential has been subtracted from the data for better visibility of the minima, and we set \( \Phi(r_0) = 0 \). The insets show a magnified view (b,e), of the marked pair of trapping sites, and the line potential through them (c,f).

Effects due to the finite number of RF rails also cause a variation in the stability \( q \)-factor and, therefore, in the radial frequencies. For attenuation on the even rails, the \( q \) values are between 0.21 and 0.35, allowing for simultaneous stable trapping, and the radial frequencies vary within \( \omega_r = 2\pi \times (2.0–3.6) \text{MHz} \). For attenuation on the odd rails, the effect is weaker, with the \( q \)-factor ranging between 0.26 and 0.22 and a radial frequency variation of \( \omega_r = 2\pi \times (2.2–2.8) \text{MHz} \). The differences in \( \omega_r \) and in trap spacing \( s_z \) across the array cause a variation in the double-well barrier \( U_b \). However, \( U_b \) does not fall below 2 meV across the entire array and in both configurations. For motional coupling between adjacent sites, the variation in radial frequencies is not a concern if the axial mode is employed. The finiteness of the array leads to additional inhomogeneities in conjunction with the fact that the voltage set for axial confinement is calculated only for a single site at the array center. This makes the axial multiwell potential non-ideal at the array edges. Due to this, the axial frequency \( \omega_z \) varies by 74 kHz for attenuation on the even RF rails. For attenuation on the odd rails, the effect is significantly smaller with a variation in \( \omega_z \) of 7 kHz. Lastly, edge effects lead to small shifts of the trapping sites off the RF null of about 1 \( \mu m \) for both configurations, comparable to the default configuration.

We note that many of the above-mentioned limitations could be mitigated in an optimized trap geometry. In particular in the reduced RF configuration, one could achieve a much better homogeneity of the reduced trap spacing \( s_z \) across the array, and therefore of the ion coupling strength \( \Omega_c \), by adjusting the RF and DC rail widths. A first step in this direction was made by increasing the width of the outermost RF rails, allowing for a match of the stability \( q \)-values of the linear traps in the default configuration. Even with remaining variations in \( \Omega_c \) across the array, parallelized entangling operations could still be realized. The correct gate time for each \( \Omega_c \) could be set by the time that the trapping wells are kept resonant, using DC control fields, or the reduced spacing \( s_z = 40 \mu m \) could be consecutively set for the different pairs of linear traps using multiple adjustments of the RF voltage. Another important improvement would be a further segmentation of the DC rails. This would allow for tuning of additional parameters such as the mode tilts and the axial trap spacing \( s_z \).

Appendix D: Advantages of RF Tuning in Linear Trap Arrays

For the successful application of a trap array for quantum information processing, the inter-site coupling rate \( \Omega_c \) needs to significantly exceed the motional heating rate \( \Gamma_h \). In surface traps, the heating rate typically increases drastically as the ions approach
the trap surface.[38] Therefore, one would like to maximize the ion-surface separation $d$ while maintaining a small trap spacing $s$ that yields a sufficient coupling rate $\Omega_c$ (cf. Equation (1)).

In this section, we consider a trap array without RF tuning and with a trap distance $s_x = 40 \mu$m. For such an array, the ion-surface separation cannot exceed $d_{\text{max}} \approx 30 \mu$m, as we show below. In contrast, using RF tuning we achieve more than three times larger ion-surface separation $d \approx 100 \mu$m for the same ion-ion spacing $s_x$ (cf. Figure A5). This increased separation $d$ corresponds to a two orders of magnitude lower ion heating rate $\Gamma_h$, assuming a typical $d^{-4}$ dependence of surface noise.[91,92] In addition, the use of RF voltage tuning in linear trap arrays can also lead to a greatly increased trap depth, as shown below.

We consider a linear trap array with alternating RF and GND rails, Figure A6a. An additional grounded plane at a distance $y = 1 \text{ mm}$ above the trap surface is assumed.[93] The important difference to the array in Figure A3 is that the RF voltage is identical on all RF rails, that is, there is no RF tuning. Therefore, the trap distance $s_x$ is simply given by the periodicity of the structure, $s_x = w_{\text{GND}} + w_{\text{RF}}$, neglecting edge effects. We further consider a fixed ion-ion spacing, $s_x = 40 \mu$m, the same value as proposed for the ion-ion coupling in Figure A5. We then simulate the trapping potential for different RF rail widths, spanning the entire range $w_{\text{RF}} \in [0, s_x]$. With $w_{\text{GND}} = s_x - w_{\text{RF}}$, the electrode geometry is thus fully determined. In this way, we find all possible values for the ion-surface separation $d$ that can be realized. As seen in panel (b), the maximum achievable ion-surface separation is about $d_{\text{max}} \approx 30 \mu$m. This is more than a factor 3 smaller than the ion-surface separation $d \approx 100 \mu$m in Appendix C, making loading of ions extremely challenging.

### Appendix E: Suppression of Parasitic Motional Coupling between Non-Nearest Neighbors

For the realization of parallelized pairwise entangling operations between ions in adjacent trapping sites, we suggest to employ the motional coupling of the ions’ axial modes. Using RF shuttling, a motional coupling strength $\Omega_c \approx 2\pi \times 1 \text{ kHz}$ between nearest neighbor ions can be reached at a reduced trap distance $s_x = 40 \mu$m (see Appendix C). However, the desired coherent evolution of the ions’ motional states can be disrupted by additional unwanted motional couplings to non-nearest neighbors. While these parasitic couplings become rapidly weaker for higher order neighbors due to the $1/s^3$ scaling of the motional coupling strength $\Omega_c$ (cf. Equation (1)), their presence can still degrade the gate fidelities. In this section, we outline a scheme to considerably reduce the parasitic coupling to non-nearest neighbor ions. The outline considers parallelized entangling operations along the $x$-direction; the scheme works in the same fashion for operations along the axial direction $z$.

The scheme makes use of the fact that a strong coupling of the ions’ motion requires their axial well frequencies to be resonant; for a well detuning $\delta \gg \Omega_c$, the ion motion can be considered independent.[21–23] It is therefore possible to pairwise couple multiple ions simultaneously by picking a different resonance frequency for different ion pairs, effectively turning off the parasitic coupling between the non-nearest neighbors. To be more concrete, we consider the ion lattice illustrated in Figure A7. The ions are arranged in pairs with a nearest neighbor distance $s_y = 40 \mu$m along the $x$-direction, giving rise to a coupling strength $\Omega_c \approx 2\pi \times 1 \text{ kHz}$ at a resonant axial frequency $\omega_y \approx 2\pi \times 1 \text{ MHz}$. The distance to the next-nearest neighbor ions is assumed to be $s_x = 200 \mu$m, similar to the trapping potential in Figure A5. For simplicity, we further assume an isotropic lattice,
where the distance $s_1$ and the motional coupling strength $\Omega_c$ are identical along the $x$- and $z$-direction.\cite{95} For the suppression of the first order parasitic coupling between ions at distance $s_1$, one can use a checkerboard pattern for the well detuning, as shown in Figure A7a. Axial well frequencies within a red or blue square are detuned by $+\delta^{(1)}$ and $-\delta^{(1)}$, respectively, relative to the resonant well frequency $\omega_z$. For the required detuning, it holds $\delta^{(1)} \gg \Omega_c^{(1)} = \Omega_c^{(0)} (s_1/s_1)^3 \approx 2 \pi \times 8 \text{ Hz}$. Already for $\delta^{(1)} = 10 \Omega_c^{(1)} \approx 2 \pi \times 100 \text{ Hz}$, a drastic reduction of the parasitic coupling should be observable. The second-order parasitic coupling is between ions at a distance $s_2 = \sqrt{2}s_1$, along the diagonal of the lattice. This coupling can be suppressed with an additional detuning $\pm \delta^{(2)}$, applied to adjacent rows of ions on a striped pattern as shown in panel (b). Here, $\delta^{(2)} \gg \Omega_c^{(2)} = \Omega_c^{(0)} (s_1/s_1)^3 \approx 2 \pi \times 2.8 \text{ Hz}$. It is important to note that the detuning $\delta^{(2)}$ partially cancels the detuning $\delta^{(1)}$ for some pairs of ions. To account for this cancellation, the detuning $\delta^{(2)}$ must be increased accordingly. Hence, the suppression of both first- and second-order parasitic couplings requires four different well frequencies for the pairs of ions across the array: $\omega_z + \delta^{(1)} + 2\delta^{(2)}$, $\omega_z + \delta^{(1)}$, $\omega_z - \delta^{(1)}$, $\omega_z - \delta^{(1)} - 2\delta^{(2)}$. The scheme can be further extended to suppress higher order couplings by successively increasing the cell size of the checkerboard and striped patterns, as shown in panels (c) and (d) for the third- and fourth-order coupling, respectively. We note that a complete suppression of parasitic couplings up to infinite order is impossible due to the partial cancellation of detunings for different orders: the accumulated compensation for the cancellation leads to diverging well frequencies in the limit of infinite order couplings. In practice, however, higher order couplings $i$ can be neglected once their coupling strength $\Omega_c^{(i)}$ falls below the ion heating rate $\Gamma_i$, the fundamental limit for uncontrolled motional excitation. For instance, in the considered array, already the fourth order coupling has a strength $\Omega_c^{(4)} < 2 \pi \times 1 \text{ Hz}$. Suppressing parasitic coupling up to the fourth order requires 16 different well frequencies for adjacent pairs of ions with a maximum detuning from each other on the order of a few hundred Hz. Such detunings are small compared to the well frequency $\omega_z \approx 2 \pi \times 1 \text{ MHz}$ and can be readily implemented using individual DC control electrodes below each trapping site.

**Supporting Information**

Supporting Information is available from the Wiley Online Library or from the author.

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**Conflict of Interest**

The authors declare no conflict of interest.

**Keywords**

ion lattice, ion traps, quantum information processing, surface trap array

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