Designing Conductive-Bridge Phase-Change Memory to Enable Ultralow Programming Power

Zhe Yang, Bowen Li, Jiang-Jing Wang, Xu-Dong Wang, Meng Xu, Hao Tong, Xiaomin Cheng, Lu Lu, Chunlin Jia, Ming Xu,* Xiangshui Miao,* Wei Zhang,* and En Ma*

Phase-change material (PCM) devices are one of the most mature nonvolatile memories. However, their high power consumption remains a bottleneck problem limiting the data storage density. One may drastically reduce the programming power by patterning the PCM volume down to nanometer scale, but that route incurs a stiff penalty from the tremendous cost associated with the complex nanofabrication protocols required. Instead, here a materials solution to resolve this dilemma is offered. The authors work with memory cells of conventional dimensions, but design/exploit a PCM alloy that decomposes into a heterogeneous network of nanoscale crystalline domains intermixed with amorphous ones. The idea is to confine the subsequent phase-change switching in the interface region of the crystalline nanodomain with its amorphous surrounding, forming/breaking “nano-bridges” that link up the crystalline domains into a conductive path. This conductive-bridge switching mechanism thus only involves nanometer-scale volume in programming, despite of the large areas in contact with the electrodes. The pore-like devices based on spontaneously phase-separated Ge\textsubscript{13}Sb\textsubscript{71}O\textsubscript{16} alloy enable a record-low programming energy, down to a few tens of femt joule. The new PCM/fabrication is fully compatible with the current 3D integration technology, adding no expenses or difficulty in processing.

1. Introduction

Artificial intelligence (AI) and other data-intensive technologies are pushing forward the frontiers of non-volatile memory and neuro-inspired computing devices. Correspondingly, the requirements on the materials implementing these functions have also escalated, demanding increasingly fast switching speed, long-term data retention, low power consumption, high cycling endurance, low resistance drift, and efficient emulations of artificial neural network. Chalcogenide phase-change materials (PCM), based on the Ge\textsubscript{2}Sb\textsubscript{2}Te\textsubscript{5} (GST) alloy currently used in commercial memory products, are one of the leading material candidates\cite{1–10} with properties being systematically tailored toward one (or more) of the targeted directions listed above.\cite{2,11} For instance, the recently designed Sc\textsubscript{0.2}Sb\textsubscript{2}Te\textsubscript{3} alloy with ultrafast nucleation rate brings the programming time down to hundreds of picoseconds, extending the memory-oriented application of PCM toward non-volatile cache-type memories.\cite{12,13} Another example is the new concept of phase-change heterostructure (PCH), employing TiTe\textsubscript{2}/Sb\textsubscript{2}Te\textsubscript{3} as confinement/PCM nanolayers. The PCH enables memory programming with ultralow drift and noise, potentially suitable for neuro-inspired computing operations of high accuracy and consistency.\cite{14,15} In the following, we aim to push the envelope for yet another key attribute, that is, energy consumption needed to accomplish memory switching. This is important for storage-oriented applications, particularly in compact 3D stacked arrays where heat dissipation has been a nagging problem. In fact, the current 3D XPoint PCM product is limited to a few stackable layers, because otherwise the large amount of heat generated during the RESET process would degrade the device quickly. Minimizing the power consumption for energy-efficient memories therefore remains a major challenge.

The SET and RESET operations in phase-change memory devices are accomplished by crystallization and amorphization of the PCM under external electrical pulses through joule heating. The large contrast in electrical resistance between the amorphous phase—high resistance state (HRS “0”) and the crystalline phase—low resistance state (LRS “1”) of PCM is used to encode digital information. The major power cost in devices resides...
Figure 1. Design concept. A) Sketch of conventional mushroom-type memory. B) Concept of conductive-bridge phase-change memory (cbPCM), showing the programmable layer with necklace-like network comprised of crystalline nanodomains intertwined with amorphous domains (left panel), and a potential conductive bridge linking nearby crystalline nanodomains for charge transport (close-up view in the right panel). Phase change is expected to occur mostly at the narrow connection gaps (open or close the “bridge”). C) The DFMD snapshots of the Ge-Sb-O model after fast and slow quenching, and the swapped model. The Ge, Sb, and O atoms are rendered with red, purple, and cyan spheres. The size of Ge and O atoms is enlarged for a clear view of the co-segregation of Ge and O. The degree of local enrichment of Ge and O in the amorphous state increased upon slow quenching.

with the RESET operation, in which the crystalline phase needs to be melted first at temperature $T_m \approx 900$ K, and then rapidly quenched to form the amorphous phase. Typical PCM devices require tens of picojoule to nanojoule and a large current density of $>1$ MA cm$^{-2}$ for each RESET operation.\cite{17} To reduce the RESET energy $E_{\text{RESET}}$, various approaches have been developed, including materials optimization and design,\cite{12,17–21} interface and electrode engineering,\cite{22–25} nanowires,\cite{26,27} nanocrystals,\cite{28,29} as well as superlattices.\cite{30–31} Yet the power consumption remained on the order of multiple picojoules or the RESET current ranged from tens to hundreds of $\mu$A. An extreme case was reported in ref. \cite{34}, where nanoscale gaps were created in carbon nanotubes (CNT), and then filled with $\approx 10$ nm thick GST films. An ultralow $E_{\text{RESET}} \approx 100$ fJ was achieved in this device setup, with a RESET current $\approx 5$ $\mu$A, as the contact area between the CNT electrodes (diameter $\approx 3$ nm) and GST that is, the switching (programming) volume, is made extremely small. The energy consumption is further improved to $\approx 80$ fJ by using self-aligned GST nanowires and CNT electrodes (diameter $\approx 1.7$ nm), with a RESET current $\approx 1.6$ $\mu$A.\cite{35} However, such a nanowire/tube route requires delicate nanofabrication protocol, posing formidable challenges for the mass production of PCM devices and chips. Therefore, there is a pressing need for a practical materials solution toward processing-friendly low-power devices.\cite{16}

All the approaches so far follow a direct scaling between the power consumption and the size of the data storage device. This correlation also holds for PCM memory cells. As seen in the mushroom-shape geometry shown in Figure 1A, the programming volume is determined by the contact area of the PCM with the bottom electrode. The smaller the diameter of the bottom electrode, the lower the power consumed in the switching operation. So far, the size of the bottom electrode is down to few tens of nm,\cite{23} and further device miniaturization is still being pursued. In this work, we present a materials design strategy to break the proportional dependence of power consumption on device size, leading to an ultralow $E_{\text{RESET}}$ of tens of fJ in a normal-sized device (250 nm hole diameter). The new alloy scheme enables a drastic energy reduction, by more than four orders of magnitude, with respect to GST devices in the same device geometry. The alloy can be synthesized through sputter deposition with no added fabrication procedure, which provides an alternative approach for high-density integration of PCM cells.
2. Results

2.1. The Concept of Conductive-Bridge Phase-Change Memory

The essence of our idea is to create inside the PCM alloy a conductive channel with the dimension of a few nanometers, such that the switching volume is minimized and the current path can be easily open and shut. To this end, our conductive channel is made of low-resistance and low-$T_c$ PCM regions, that is, crystalline nanodomains (CNDs) chained together, which are surrounded by high-resistance amorphous regions. These CNDs are nearly-interconnected, separated only by minute amorphous gaps. The amorphous-crystalline phase change during cyclic switching is then executed merely in the left-over gaps in between the CNDs. In other words, the electrical resistance of the current path is controlled by the tiny bridges linking up the CNDs. This scheme makes use of joule-heating induced phase transition at edges, which was demonstrated possible in a nanofabrication-patterned (and doped-) GST memory cell (reducing the RESET current to 20 μA).[28] We aim to i) design a PCM alloy to spontaneously generate nano-sized conductive channel in a normal-sized cell without lithography patterning, ii) minimize the effective switching volume to only one conductive channel, and as such iii) reduce the RESET current and power consumption to a few μA and tens of μA.

To make this advance possible, the PCM we desire is an alloy that spontaneously decomposes into a network of nanodomains having spatially varied chemical composition and thermal and electrical resistance. As schematically depicted in Figure 1B, the electric current and the resulting joule heat are likely to be concentrated to form a conductive necklace across many CNDs, by converting the missing link (red region) into conductive bridge. For this conductive-bridge PCM (cbPCM) scheme to work, the alloy selection needs to meet the following criteria. First, the base PCM should be of the growth-type, such that the phase change is in the form of expansion/shrinkage at the crystalline-amorphous interface. Stochastic and undesired nucleation inside the amorphous domains is to be suppressed. Second, a small addition of alloying element should lead to strong phase separation with smooth interfaces under external stimulus such as heating or electrical pulses, leading spontaneously to the desired necklace-like network microstructure. Third, one set of the domains should be highly resistive to both electrical currents and heat flow, staying robust in amorphous state (with a high $T_c$) that remains nearly unchanged during service. This necessities an alloying element as a strong stabilizer for the amorphous phase. Fourth, the other set of domains should have low $T_c$ and $T_{in}$, offering a low barrier for phase transition. This facilitates the back-and-forth expansion/retraction of the crystal boundary around these CNDs, serving the function of a “conductive bridge” that can be “open” or “shut” during cyclic programming. Fifth, the new material should be compatible with the current PCM and semiconductor technology, to keep the fabrication practical for mass production.

2.2. Design and Synthesis of Heterogeneous Ge-Sb-O Alloys

In the classical PCM Ge-Sb-Te ternary diagram, two well-studied growth-type PCM families are located around the compositions Sb, Te and Sb.[31] Alloys based on them have enhanced amorphous stability, and the extensively used materials are Ag$_{x}$In$_{y}$Sb$_{z}$Te$_{t}$ and Ge$_{x}$Sb$_{y}$Te$_{z}$.[37–40] Here we choose the latter, because Sb has a much lower $T_c$ and high growth rate,[41–43] and Ge-Sb alloys are known to be prone to phase separation after many cycles.[44,45] As for the alloying element that further increases the driving force for chemical decomposition, a possible candidate is O, which was reported to induce molecular-scale phase separation in the Ge-Sb glass.[46] We settled on its homologue oxygen (O). This selection of Ge-Sb-O is based on the following indicators.

First, our density functional theory (DFT) calculation shows a difference in the energy of formation, $E_{form}$, which is $-2.09$ and $-1.85$ eV per atom for Ge-O and Sb-O crystals, respectively. The Ge-O chemical bonds are also quantitatively more robust than Sb-O, as determined by the crystal orbital Hamilton population (COHP) analysis (Figure S1, Supporting Information). We therefore conjecture that upon heating of amorphous Ge-Sb-O, domains enriched in Ge and O would be created, together with Sb-enriched ones. Second, Ge-O is known to form very good glasses with crystallization temperature above 950 K,[48] which is even higher than the melting temperature of Sb and GST ($≤900$ K). The third and most direct justification of our alloy selection is that our DFT-based molecular dynamics (DFMD) simulations indicate a clear trend of phase separation in Ge-Sb-O glass. To see this, we constructed a Ge-Sb-O model with 36 Ge, 288 Sb, and 36 O atoms, randomized the model at 3000 K for 10 ps to remove any possible atomic correlations, and then quenched it from 1000 K down to 0 K in 5 and 100 ps (denoted as the fast-quenched and slow-quenched model). At 600 K, we tentatively swapped the position of some Ge and O atoms with Sb atoms in the Sb-poor regions of the latter model, and equilibrated the new model for 30 ps and then quenched it down to 0 K in 60 ps (denoted as the swapped model). As shown in Figure 1C, Ge atoms tend to form bonds with O atoms, and most of Ge-O bonds remain robust during the quenching process. The Ge and O atoms have a clear tendency to cluster together in the slow-quenched model than the fast-quenched one, and the former is $≈36$ meV per atom lower in energy than the latter. Upon further clustering the Ge and O atoms in the swapped model, the energy difference with respect to the fast-quenched model is enlarged to $≈41$ meV per atom (as a benchmark for comparison, the energy difference between melt-quenched and aged models of amorphous GeTe is about $≈8$ meV per atom)[49]). This indicates a strong tendency toward phase separation into a Ge-O stabilized glass, and a Sb-enriched one that is prone to crystallization (i.e., the formation of CNDs) and easy to switch, all inside the amorphous alloy film. As such, all the materials selection criteria in the preceding paragraph are satisfied.

To see if this new O-doped PCM works, we synthesized Ge-Sb-O thin films $≈100$ nm in thickness, with varied compositions from Ge$_{x}$Sb$_{100-x}$ targets with $x = 7, 10,$ and $15$, using magnetron sputtering in a mixed argon and oxygen pressure of 0.5 Pa. Note that for most of PCM applications, oxidation needs to be avoided to guard against undesired changes in crystallization performance. Yet, for the applications that require high thermal stability and small density contrast for switching, oxygen doping was also used.[50–53] Previous optical experiments demonstrated that Ge-Sb maintains the growth-dominant crystallization mechanism as long as the O alloyed into the system is less than 16%, precluding that undesired nucleation upon device
Figure 2. Ge-Sb-O alloy thin films. A) Resistance–temperature curves of three Ge-Sb-O alloys upon heating. The less the Sb content, the higher the crystallization temperature. The Ge15Sb85-O thin film was annealed at 200 °C for 30 min for transmission electron microscope (TEM) and atom probe tomography (APT) characterization. The composition is determined to be Ge13Sb71O16 (GSO) using APT. B) A high-resolution TEM image of the annealed GSO thin film and C) the corresponding Fast Fourier Transform (FFT) pattern, showing the mixture of amorphous and crystalline domains. D) An overall 3D APT reconstruction of a GSO needle in an 87 × 74 × 71.5 nm³ volume, showing an inhomogeneous distribution of Sb (purple), Ge (red), and O (cyan) atoms. E) Iso-concentration surfaces (in red) of 15 at% Ge. The surface marked by the yellow circle was used for the proximity histogram concentration profiles in (F). F) Approaching the interior region of the red cluster pointed by white arrows, the concentration of Sb changes from ≈80 to ≈20 at% across an interfacial region 2 to 4 nm in width, while that of Ge and O increases sharply.

2.3. Heterogeneous Network Achieved Under Thermal or Electrical Stimuli

We subjected the Ge-Sb-O alloy having the highest stability to thermal annealing, to see if the phase-separating microstructure would evolve in the way we desire. The thin film, covered by an ≈10 nm electron-transparent ZnS-SiO₂ capping layer (to prevent further oxidation), was annealed at 200 °C for 30 min in a high vacuum furnace. As seen under the transmission electron microscope (TEM), the microstructure is found to be more inhomogeneous than the as-sputtered case, as we conjectured. It now consists of almost-interconnected domains of partially crystallized regions coexisting with amorphous regions, as observed in the TEM image in Figure 2B and further confirmed via Fast Fourier Transform (FFT) analysis of the TEM image of selected areas (Figure 2C).

The chemical composition of the thin film is quantitatively determined using atom probe tomography (APT). Overall, the alloy has the composition Ge₁₃Sb₇₁O₁₆ (referred to as GSO hereafter). The variation in local chemical composition is clearly revealed by APT. Figure 2D shows a 3D reconstruction of the GSO specimen, in which Ge, Sb, and O atoms are in red, purple, and cyan (each dot denotes an atom). The heterogeneity in elemental distribution is clearly observed. The complex decomposed network is further mapped out by highlighting the iso-composition surfaces of 15 at% Ge (red surfaces) in Figure 2E. One such surface is analyzed in detail, shown in Figure 2F, which shows a strong compositional variation from ≈82 at% Sb to only ≈24 at% Sb, moving inward in the direction of the white arrows in Figure 2E.
The concentration of O atoms shows a strong correlation with Ge atoms, as expected from the phase separation tendency predicted in our DFMD model of the Ge-Sb-O glass. It has been established that crystalline PCMs are stabilized by metavalent bonding (MVB)\([56–58]\) while covalent bonding prevails in amorphous PCMs. The bonding difference between the two phases is evidenced by their distinct dielectric functions\([59]\) and be revealed in direct measurements of bond rupture events using APT\([60–62]\). Our experiments show that the average probability of multiple bond rupture events (e.g., several bonds are broken simultaneously, which is the feature of MVB in crystalline PCMs) is \(\approx 48.8\%\) in Sb-rich regions, but is only \(\approx 24.4\%\) in the Sb-poor regions, indicating that the GSO thin film is indeed a heterogeneous network of crystalline and amorphous nanodomains upon heating. Notably, the elemental concentration changes continuously but rapidly at the interface, from Sb-rich to Sb-poor across a distance of only \(\approx 2\) nm. In other words, the GSO alloy is indeed a suitable precursor for the desirable cbPCM microstructure depicted in Figure 1B.

From the observations above, the GSO in devices would also undergo “microstructure patterning” into heterogeneous network, if electrical stimuli are used in lieu of thermal annealing. In fact, to set the stage for cbPCM, a necessary step is to accomplish the self-patterning process using voltage/current, to establish the desired microstructure network needed for subsequent phase switch. We fabricated pore-like devices with a hole diameter of 250, 500, 750, and 1000 nm, denoted as \(D_{250}, D_{500}, D_{750},\) and \(D_{1000}\), and filled the pores with sputter-deposited GSO, as sketched in Figure 3A. A GST-based device using the same \(D_{250}\) setup was also prepared, to facilitate a direct comparison. The as-fabricated device is highly resistive with a cell resistance value above \(10^{10}\) \(\Omega\). Cross-sectional TEM of as-deposited GSO film shows that it is in a fully amorphous state but with obvious chemical segregation into Sb-rich and Sb-poor domains (Figure S2, Supporting Information); this partial network patterning is enhanced by further decomposition during the device fabrication process as a result of the unavoidable rise in temperature. The patterning is subsequently completed by crystallizing the Sb-rich domains via a couple of \(100\) ns SET current pulses with an increasing amplitude up to \(8\) \(\mu\)A. This accomplishes the first SET operation, and the cell resistance turns into LRS with \(\approx 2 \times 10^6\) \(\Omega\). The device is then ready for subsequent cbPCM memory programming. One caveat to keep in mind here is to avoid too strong SET pulses, because the crystalline fractions could get so high that the cell resistance drops down to \(k\Omega\) level, making the subsequent RESET operations too difficult (requiring much larger currents). The amplitude of RESET pulses should stay low as well, to avoid large morphological change of the heterogeneous network, for example, large \(U_{\text{RESET}}\) (over 2 eV in Figure 3B) could lead to undesired crystallization.
2.4. Ultralow Programming Power for RESET Operations

To investigate the RESET process and find the optimal operation voltage in the GSO-D_{250} device, we applied a series of voltage pulses with the same duration of 48 ns but increasing amplitude up to 3.0 V, see Figure 3B. This results in a gradual increase in cell resistance from LRS (≈10^{10}–10^{11} Ω) to HRS (≈10^{10} Ω and above). To SET the GST-D_{250} device into LRS (Figure 3C), voltage pulses with long decay width are needed, while much shorter current pulses, for example, 103 ns, are already sufficient for SET operations (Figure S3, Supporting Information). The resistance window is found to be rather wide, with at least one order of magnitude difference in resistance. It is also robust over time, as shown in Figure S4, Supporting Information, where the measured drift coefficient ν is as low as ≈0.003 for LRS and ≈0.014 for HRS. The latter value is much lower than that in GST devices (≈0.11).[61] This can be attributed to the fact that the heterogeneous network in our GSO devices corresponds to a well-aged state, consisting of separated Sb-rich CNDs (with Sb concentration >80%, Figure 2F) and GeO-rich glass domains that do not undergo much structural relaxation with time. Aging effects are possible in the switchable edges, where the Sb concentration is lower than 80%, but the volume fraction of these regions is very limited. As such, our GSO devices are not subject to obvious drift in cell resistance (Figure S4, Supporting Information).

Next, we evaluate the cycle-to-cycle and device-to-device variability for memory programming. For a typical GST-D_{250} cell, we fixed the RESET voltage (U_{RESET}) at 1.6 V and SET voltage at 1.2 V, with the pulse shape shown in the inset of Figure 3B,C. The electrical measurement of over 2 × 10^{5} switching cycles using this cell is presented in Figure 3D, showing consistently an ≈30-fold contrast window between the average HRS and LRS values. This indicates that the crystal-glass network pattern and the resulting conductive channels maintain similar morphology from cycle to cycle in the cycle range we experimented, because otherwise the resistance would have shown much larger variation. The high contrast stability also holds in our cell-to-cell uniformity tests, as shown in Figure 3E (we tested 30 independent GST-D_{250} cells using similar operation protocols, and averaged the resistance of the first 100 cycles for each cell). Taking into account both cycling and inter-device variations, the contrast in electrical resistance between the highest LRS and the lowest HRS is about fivefold, which is sufficient for binary storage. These results indicate that even though the network pattern reached through phase separation is unlikely to be identical for different memory cells, the functional conductive paths always bear sufficient similarity in physical dimensions and morphology, such that the performance of the resultant cells is satisfactorily reproducible, guaranteeing adequate reliability for binary programming applications.

The RESET energy can be estimated as E_{RESET} = I × U × Δt = U_{RESET} × Δt/R_{SET}. As shown in Figure 3D, the average R_{SET} upon cycling is ≈2.3 MΩ, and Δt = 48 ns (full width at half maximum). The RESET energy is estimated as ≈53 fJ for this particular cell. After taking into account the minor cell-to-cell variations (e.g., slightly different U_{RESET} and R_{SET} for the 30 memory cells) shown in Figure 3E, the average RESET energy is found to be only ≈43 fJ. As presented in Figure 3F, all cells show consistently low power consumption at a few tens of fJ, always below that of CNT-GST devices (80–100 fJ).[34,35] Note that if GST is used in the same D_{250} device setup, the average E_{RESET} value would be of nJ level,[62] which is 4–5 orders of magnitude higher than the GSO-D_{250} devices.

The low power consumption of GSO devices is further supported by the ultralow current needed for RESET operation. This is demonstrated using Figure S3, Supporting Information, in which a larger device, GSO-D_{500}, is directly programmed using current pulses. The pulse width was fixed as 103 ns (the minimum window of our home-made testing setup), and the pulse amplitude was ramped up with 100 nA increments. RESET is accomplished at ≈1.5 μA, which is a current more than 3 orders of magnitude lower than that in GST-D_{500} pore-like devices, for which the current needed is as large as ≈3.0–11.4 mA.[64] Notably, our I_{RESET} is comparable to that realized in nanowire devices, that is, the CNT-GST devices (≈5 and ≈1.6 μA for CNT diameters of ≈3[61] and ≈1.7 nm[51]). This is an indication that the effective switching volume for RESET operations in our device is indeed on nanoscale dimensions and the bridges being open and shut must be very few. What the RESET action does is only to break open the narrowest nano-segment(s) of the conductive bridge, turning the cell into a HRS.

2.5. Cross-Sectional Device Characterization Lending Support to the Switching Mechanism

Next, we provide microstructural evidence lending support to the conductive bridge switching mechanism described above, using cross-sectional TEM experiments on a couple of GSO-D_{250} cells. Figure 4A shows a slice of the device in SET state. The thickness along the viewing direction is ≈80 nm. Figure 4B shows a detailed map of Sb signals obtained using energy-dispersive X-ray spectroscopy (EDX), in which a clear variation, that is, undulating Sb-rich and Sb-poor regions, is observed. Figure 4C shows a local view that the Sb-rich domain has a clear crystal lattice feature, while no crystalline feature is visible in the Sb-poor domain. The dim halos in the FFT pattern also confirm the amorphous nature of the latter. We performed extensive high resolution TEM investigations of this SET state cell, and map out a complex network of amorphous and crystalline domains, as displayed in Figure 4D and Figure S5, Supporting Information.

These findings are consistent with what we predicted and discussed earlier, in regards to the microstructural features underlying the SET state. For the RESET state, we conducted similar experiments on a different cell. This memory cell also shows the expected network comprised of amorphous and crystalline domains with different chemical compositions, as shown in Figure 4E and Figure S6, Supporting Information. In other words, although it is not possible to know the exact location of the switching necks in such complex network and directly pinpoint the local phase transition that completed the conductive bridge in real devices, this set of observations in the unconfined TEM foils does serve the purpose of proving that Figure 1B is based on a correct microstructural picture. Again, our ultralow RESET current ≈1.5 μA, in comparison with the miniaturized nanowire CNT-GST device with an ≈2.3 nm² contact area, where the RESET current is ≈1.6 μA,[35] is also a manifestation that the switching area involved in RESET operation must be on the scale of a few nm,
Figure 4. Cross-sectional TEM showing intertwined nanodomains. A) An overview of a GSO-$D_{250}$ cell in SET state. The specimen is $\approx 80$ nm in thickness along the viewing direction. B) The EDX element mapping of the middle part of the specimen. Sb-poor and Sb-rich domains are clearly identified. C) Local view of an interface area. The Sb-poor domain shows maze-like amorphous feature with a dim halo in the FFT pattern, while the Sb-rich domain is clearly crystallized with lattice fringes. D) The high-resolution TEM image and FFT of a local area in the cell in SET state, showing intermixed nanoscale crystalline and amorphous domains. The same also holds for RESET state: the networked mixture is observed in E) for another cell.

despite the large (electrodes) contact area ($\approx 10^5–10^6$ nm$^2$) used in our devices.

2.6. Defying the Scaling Between Switching Energy and Device Size

Finally, we examined the power consumption at larger device sizes. We tested multiple GSO-$D_{500}$ devices and always observed small $E_{\text{RESET}}$ values below 100 fJ under suitable pulse setting. Only a slight increase to 150–200 fJ was found for even larger devices such as $D_{750}$ and $D_{1000}$. Such a low $E_{\text{RESET}}$ suggests that the effective switching volume always remains small on nanoscale, further supporting the cbPCM switching mechanism. Moreover, as compared in Figure 5 with literature data plotted as a function of contact area size,[12,15,20–35,50,65] our cbPCM devices not only have achieved an unprecedented low power consumption in comparison with all devices of similar contact sizes, but also clearly breaks the previously established scaling (dashed line) of energy with the contact area. This is a major advantage of our heterogeneous alloy approach, as it achieves the minimization of the effective switching volume without the need to miniaturize the size of the electrodes or PCM cell, greatly reducing the complexity and costs for device fabrication. Before closing, we also note that the cbPCM switching mechanism is distinct from the conductive-bridge mechanisms reported in filamentary resistive-switching random access memories (RRAM) using metal oxides,[1–5] as there the ionic conducting channels change their transport.
direction upon reversing the voltage polarity. In contrast, our cbPCM device shows unipolar switching feature (Figure S7, Supporting Information), confirming that phase transition is the underlying switching mechanism in our case. Such a phase transition mechanism occurring at certain local spots avoids the extensive ion transport as well as the randomness associated with the formation and dissolution of conductive filaments in RRAM.

3. Conclusion and Outlook

We have successfully designed and fabricated PCM devices with nanoscale conductive-bridge using a carefully selected GSO alloy, breaking the energy-size direct-scaling correlation to reach a record low programming energy for phase-change memory cells. To enable the new conductive bridge switching mechanism, we purposely “self-patterned” the GSO microstructure to consist of layers, and thus much increased data storage density. The alloy is compatible with the current semiconductor fabrication lines and can be achieved in one-off sputtering, ensuring simple and low-cost production. Scaling down the size of the device, but keeping it well above the amorphous/crystalline domain dimensions (5–20 nm), could further reduce the stochasticity of conductive channels as well as the device variation. Therefore, we advocate cbPCM as a potential candidate for phase-change data storage in binary scheme. If needed, further optimization of the Ge-Sb-O chemical composition and potential doping is possible, to tailor the switching speed, thermal stability, as well as the size of the resistance window.

As a possible tweak toward yet another phase-change application, our GSO-based devices could also be made to present multilevel resistance capability. To further widen the resistance window to accommodate more states, one could use stronger RESET pulses to enlarge the switching bridge or break more necks, or longer SET pulses to crystallize larger fractions of the heterogeneous network. This programming mode would however result in larger fluctuation and variability from cycle to cycle and from device to device, due to more extensive changes to the heterogeneous network. Nevertheless, such features might turn out to be useful for the emulation of stochastic phase-change neurons,[66] which play a key role in signal encoding and transmission in biological neural networks.[67] With power consumption approaching biological neural network, the GSO-based cbPCM devices may then enable performance superior to the conventional GST-based PCM devices.

4. Experimental Section

Film Synthesis and Characterization: Ge-Sb-O thin films were obtained by magnetron sputtering three alloy targets, Ge8Sb92, Ge10Sb90, and Ge15Sb85, under the same condition with a mixed argon and oxygen pressure of 0.5 Pa. The ≈100 nm thick Ge-Sb-O thin films were grown on SiO2/Si substrate and annealed at 200 °C for 30 min in a high vacuum furnace. The composition of the Ge8Sb92-O thin film was identified as GSO using APT. For TEM characterization, the GSO films ≈80 nm in thickness were deposited onto ultra-thin carbon film (≈5 nm) coated copper grids and were covered by ≈10 nm electron-transparent ZnS-SiO2 capping layers to prevent further oxidation. The samples were then annealed at 200 °C for 30 min in high vacuum furnace.

Atom Probe Tomography Experiments: The needle-shaped tip was prepared from the annealed GSO film by using the standard lift-out process with a FEI Helios NanoLab 600 focus ion beam (FIB) system. The diameter of the tip was about 79 nm, and the tip was put into high vacuum (3 × 10−11 mbar) in a local electrode atom probe (LEAP 5000 XR, Cameca Instruments). By applying a DC voltage of 2.0−6.5 kV and illumination with 30 ps laser pulses in the APT chamber, atoms on the surface of the needle-shape sample were ionized. These ions and ionic clusters were projected onto a position-sensitive detector (PSD). The coordinates of ions or ionic clusters captured by the PSD were analyzed to reconstruct the 3D atomic map of the tip. The reconstruction and analyses of 3D maps were conducted using software IVAS 3.6.14.

Transmission Electron Microscopy Experiments: The high-resolution TEM and high-angle annular dark-field (HAADF) characterization of the GSO thin film samples were performed on a JEOL ARM200F microscope, operated at 200 kV with a low beam intensity. The recording time for TEM and HAADF images were a few seconds and ≈1 min, respectively. No visible structural changes were observed during the imaging process. Cross-sectional TEM specimen of the GSO-based devices were prepared using a FEI Helios 450 s dual beam FIB system with a Ga ion beam of 30 keV energy. The finishing touches for thinning and cleaning used lower energies of 5 and 2 keV, respectively. The final sample thickness was ≈80 nm.
The high-resolution TEM and energy dispersive X-ray (EDX) spectroscopy characterizations were conducted at 200 kV on a FEI Titan Themis 200 microscope equipped with a spherical aberration corrector and a Bruker Super-X EDX system. The TEM snapshots, EDX line scan, and EDX maps were performed using a low beam intensity within a few seconds, \( \approx 2 \) min and \( \approx 5 \) min, respectively.

**Device Fabrication and Electrical Measurements:** Four Pt electrodes were patterned and sputtered on four corners of GSO films for in situ sheet resistance–temperature \((R–T)\) measurement, which was performed using Keithley 4200 in a probe station of Instec mK2000 Temperature Controller with a heating rate of 6 °C min\(^{-1}\) in \(N_2\) environment. Pore-like device structure was fabricated for electrical measurements. An \( \approx 85 \) nm thick Pt layer was sputter-deposited to serve as the bottom electrode. An \( \approx 80 \) nm dielectric layer SiO\(_2\) coating was applied, via plasma-enhanced chemical vapor deposition (PlasmaPro 800 Stratum), for heat diffusion inhibition and electrical insulation. The through holes (to fill in the GSO) were obtained through electron beam lithography patterning and SiO\(_2\) dry etching. Four different pores with the diameter ranging from 250 to 1000 nm were filled with \( \approx 55 \) nm thick GSO film. Another 90 nm thick Pt film was deposited as the top electrode. The device performances were characterized using Keysight B1500A semiconductor device parameter analyzer, which could generate voltage pulses to stimulate the device. The resistance–current \((R–I)\) measurements switched by electric current pulses were performed by a parameter analyzer (Keithley 2400C) and a current pulse generator (Tektronix AWG5200B).

**Ab Initio Simulations:** DFT calculations were carried out with the Vienna Ab initio Simulation Package (VASP).[68] The Perdew–Burke–Ernzerhof (PBE) functional[49] and the projector augmented wave[70] pseudopotentials were used for VASP calculations. The chemical bonding analysis was performed using the Local Orbital Structure Reconstructed (LOBSTER) code.[71] For the formation energy and chemical bonding analysis, the crystalline structures with the most favorable formation energy were chosen. DFMD were performed using the CP2K package[50] and VASP. The PBE functional and the Goedecker pseudopotentials[71] were used for CP2K calculations. A Ge-Sb-O model with 36 Ge, 288 Sb, and 36 O atoms was fully randomized at 3000 K for 10 ps and then quenched to 1000 K. The model was then quenched down to 0 K in 5 ps or 100 ps. For the slow-quenched model, a snapshot was taken at 600 K, and Ge and O atoms were moved to the middle part and this segregated model was annealed at this temperature for 30 ps, then quenched down 0 K in 60 ps.

**Statistical Analysis:** To analyze the device-to-device variation, resistance data in Figure 3E were obtained by switching 30 independent GSO cells, and each cell was operated over 100 cycles. The resistance values of each cell presented in Figure 3E were averaged over 100 cycles, with the error bars covering the mean ± standard deviation (SD) of the data. The statistic distribution of RESET energy in Figure 3F was calculated from the mean resistance value in Figure 3E. The RESET energy of the GSO devices in Figure 5 was averaged over all GSO cells of the same size, with the error bars spanning across the mean ± SD of the RESET energy data.

**Supporting Information**

Supporting Information is available from the Wiley Online Library or from the author.

**Acknowledgements**

Z.Y., B.L., and J.-J.W. contributed equally to this work. The authors acknowledge Dr. M. Zhu, Dr. F. Rao, and Dr. X.B. Li for useful discussions, and technical support of APT experiments at Shanghai Institute of Microsystem and Information Technology. Parts of the TEM experiments were conducted at SAE Technologies Development (Dongguan) Co., Ltd. The work at HUST was supported by the National Key R&D Plan of China (Grant no. 2019YFB2205301, 2017YFB0701700) and National Science and Technology Major Project of China (Grant no. 2017ZX02301007-002). M.X. acknowledges the National Natural Science Foundation of China (Grant no. 62174060). X.M. acknowledges the funding for Hubei Key Laboratory of Advanced Memories. W.Z. acknowledges the National Natural Science Foundation of China (Grant no. 61774123), 111 project 2.0 (BP20180008), and the International Joint Laboratory for Micro/Nano Manufacturing and Measurement Technologies of XJTU. W.Z. and E.M. also acknowledge the support of XJTU for their work at CAID.

**Conflict of Interest**

The authors declare no conflict of interest.

**Data Availability Statement**

All data are available in the manuscript or the Supporting Information, and are available from the corresponding authors upon reasonable requests.

**Keywords**

chalcogenide glass, low-power devices, materials design, non-volatile memory, phase-change memory
