A CMOS QVCO using combined capacitor-coupling, bottom-series coupling and splitting switched biasing techniques

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Abstract: A quadrature voltage-controlled-oscillator (QVCO) is presented and fabricated in standard 0.18 µm RF CMOS technology. Passively capacitor coupling, actively bottom-series (BS) coupling and splitting switching biasing (SSB) techniques are combined and employed for the QVCO to improve its phase noise performance without loss of the voltage headroom. Measured results show the proposed QVCO achieves a tuning range from 0.88 to 1.04 GHz, phase noise of $-71.2$ dBc/Hz@1 kHz and $-113.1$ dBc/Hz@1 MHz, and a phase-noise figure-of-merit (FOMT) of 189.7 dBc/Hz from an offset frequency of 1 kHz, with an occupied die area of 1283 µm × 715 µm and power consumption of 11 mW from a 1.8 V voltage supply.

Keywords: quadrature VCO, splitting switched biasing, capacitor-coupling, bottom-series coupling, phase noise

Classification: Integrated circuits

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1 Introduction

Quadrature signals are widely used for I/Q modulation and demodulation in wireless transceivers [1, 2] or clock and data recovery in wireline transceivers [3]. Several quadrature signal generation methods have been reported, such as combination of a voltage-controlled-oscillator (VCO) and a poly-phase filter [4], a double-frequency VCO followed by a divide-by-2 frequency divider [5], and a quadrature VCO (QVCO) [6]. However, the first two methods have the disadvantages of narrow operation frequency ranges or high power consumption. Among them, the QVCO is universally favored because of its low phase noise, low power, wide operation frequency range, and so on.
The LC QVCO consists of two identical single-phase LC VCOs which are forced to oscillate in quadrature by some kind of coupling mechanism. Just like any other kinds of VCOs, phase noise is one of the most essential specifications for LC QVCOs. Besides LC resonant tanks, the commuting differential pairs and tail current sources within the two embedded single-phase LC VCOs, the phase noise of the LC QVCO is mainly influenced by coupling devices, coupling methods and the effective Q-factor, $Q_{\text{eff}}$.

The parallel-coupled QVCO (P-QVCO) using fixed biasing (FB) [7], shown in Fig. 1(a), has poor phase noise performance because of noisy active coupling devices, nonzero resonator phase shift, flicker noise from fixed biasing tail current sources, and bad coupling mechanism, and so on. With the parallel coupling mechanism, the coupling transistors are connected directly with the resonant tank, and the most largest noise energy injection happens at the zero-crossings of the VCO oscillation swing, where the VCO phase noise is very sensitive to incurred disturbance. The P-QVCO using splitting switched biasing (SSB) [8] has better phase noise performance than the P-QVCO using FB, because of the improved tank voltage amplitude and reduced flicker noise from its special tail current source configuration. However, due to the existence of the nonzero resonator phase shift and/or the parallel coupling mechanism, the phase noise performance of the P-QVCO using SSB is still not good. Because the zero resonator phase shift can be realized, the series-coupled QVCO (S-QVCO) [9] can achieve much better phase noise performance at the expense of the reduction of voltage headroom. A bottom-series coupled QVCO (BS-QVCO) [10], is shown in Fig. 1(c), in which the tail current source is removed to improve the voltage headroom and flicker noise performance.

A CMOS LC QVCO using combined passively capacitor-coupling, actively bottom-series coupling and splitting switched biasing techniques, which achieves excellent phase noise performance without loss of the voltage headroom, is presented in this work. The paper is organized as follows. The proposed QVCO is designed and analyzed in Section 2. The experimental results are depicted and discussed in Section 3. Finally, this work is concluded in Section 4.
2 Circuit design

In order to achieve minimum phase noise for LC QVCOs, some measures should be taken as follows. Firstly, the involved two single-phase LC VCOs should be optimized for low phase noise, e.g. high-Q resonant tanks, which have been addressed largely in a number of previously literatures. Secondly, low-noise coupling devices and proper coupling mechanism should be employed to reduce the contribution of the noise from coupling devices to the phase noise of the QVCO. Finally, $\pm \pi/2$-phase shift should be introduced in the coupling paths with explicit or implicit phase shifters and then the resonator phase shift approaches to zero degree, which will maximize the effective quality-factor, $Q_{\text{eff}}$, of the QVCO [11]. On the contrary, at nonzero resonator phase shift, the oscillation frequency $\omega$ is displaced from the tank resonance frequency $\omega_0$, so the $Q_{\text{eff}}$ will be degraded.

The proposed QVCO, depicted in Fig. 2, is composed basically of two identical differential LC VCOs, which are coupled passively by capacitors, $C_C$, and coupled actively by transistors $M_C$, simultaneously. In each LC VCO, the LC resonant tank consists mainly of two back-to-back varactors, $C_V$, and one inductor, $L$. Both the PMOS cross-coupled pair, $M_{\text{SP}}$, and the NMOS cross-coupled pair, $M_{\text{SN}}$, are adopted to generate negative resistance to compensate for the loss of the LC tank. The NMOS transistors $M_T$ and $M_C$ are both bottom-series with the $M_{\text{SN}}$ and provide splitting switched biasing for the VCO to achieve both improved oscillation amplitude and $1/f$ noise. Unlike the $M_{T1}$ in Fig. 1(b), which is used only for the SSB [8], the $M_T$ in the proposed QVCO plays a dual role in both coupling and biasing.

Define the ratio of the gate-width of $M_C$, $W_{MC}$, to the gate-width of $M_T$, $W_{MT}$, as the parameter $K$, i.e., $K = W_{MC}/W_{MT}$. To maintain approximately constant power consumption, the sum of $W_{MC}$ and $W_{MT}$ remains basically constant. In order to study the effects of the coupling capacitor $C_C$ and the transistors $M_C$ and $M_T$ on the performance of the QVCO, the tuning range (TR) and the phase noise

![Fig. 2. Schematic diagram of the proposed QVCO.](image-url)
(PN) versus the coupling capacitance $C_c$ and the parameter $K$ are simulated and plotted in Fig. 3, under the condition of the same power consumption.

As shown in Fig. 3, it is seen that to increase the coupling capacitors Cc will decrease the TR of the QVCO obviously; however, the $K$ has little impact on the TR. This is because, according to Fig. 2, to alter Cc does change the fixed capacitances introduced into the resonator, whereas to alter $K$ only changes the ratio of $W_{MC}$ and $W_{MT}$ and hardly changes the introduced fixed capacitances from transistors $M_C$ and $M_T$.

![Fig. 3. Simulated phase noise and tuning range versus $C_C$ and $K$](image)

Furthermore, it can easily observed that for each $K$ (0.5, 1, or 2), there exists an optimum phase noise which corresponds to a different coupling capacitance. When $C_C$ is small, e.g. below 100 fF or so in this example, the phase noise becomes worse as $K$ increases. On the contrary, when $C_C$ is large, the phase noise becomes better as $K$ increases. To change Cc and $K$ (or coupling transistor $M_C$) will induce different phase shifts and then change the phase noise of the proposed QVCO. Every optimum phase noise point corresponds to an optimum combination of $C_C$ and $K$ for an optimum phase shift, that is, zero resonator phase shift.

In order to get a deeper insight into the internal mechanisms, the analysis strategy similar to the one adopted in Ref. [10, 12] is applied here. The small-signal circuit model and its optimal phasor diagram corresponding nearly to zero resonator phase shift for the part of the proposed QVCO are given in Fig. 4, respectively. The $i$ is the current flowing into the drain of $M_{SN}$ at the node $V_{IP}$, which is approximately equivalent to the current flowing from the involved resonator. The $g_{m,SN}$, $g_{m,c}$ and $g_{m,T}$ are the small-signal transconductances of $M_{SN}$, $M_C$ and $M_T$, respectively. $C_{gs,SN}$ is the gate-source capacitance of $M_{SN}$. $C_{gd,C}$ and $C_{gd,T}$ are the gate-drain capacitances of $M_C$ and $M_T$, respectively. $r_{ds,C}$ and $r_{ds,T}$ are the on-resistance of $M_C$ and $M_T$ in triode region.

According to the Kirchhoff's Current Law equation at node $V_x$, the relationship between $i$ and $V_{IN}$ is derived as
where 

\[
C_1 = C_C + C_{gd,C}, \quad C_2 = C_{gs,SN} + C_{gd,T} \quad \text{and} \quad r_{ds} = r_{ds,C} \parallel r_{ds,T}.
\]

The phase shift \( \theta \) between \( i \) and \( V_{IN} \) can be calculated as

\[
\theta = \angle \left( \frac{i}{V_{IN}} \right) = \tan^{-1} \left( \frac{g_{m,C} - g_{m,T}}{\frac{1}{r_{ds}}} \right) = \tan^{-1} \left( \frac{g_{m,SN} + \frac{1}{r_{ds}}}{\frac{1}{r_{ds,T}} + \frac{1}{r_{ds,C}}} \right)
\]

According to Eq. (2), \( g_{m,C} \) and \( C_1 \), equivalent to \( K \) and \( C_C \), have the opposite effect on \( \theta \). Therefore, in the case of the proposed QVCO, \( \theta \) can converge to zero by appropriately setting the sizes of \( M_C, M_T \) and \( C_C \) which correspond to a specific combination of \( K \) and \( C_C \). At this time, as shown Fig. 4(b), \( i \) is nearly in-phase with \( V_{IN} \), which leads to the maximized \( Q_{eff} \) and then the optimal PN. The PN curve trends indicated in Fig. 3 can be easily verified by these derivations. For example, from an optimal combination of \( K \) and \( C_C \) corresponding to zero \( \theta \), if \( C_C \) is increased further, a higher \( g_{m,C} \), equivalent to a higher \( K \), is required in order for a reduced \( \theta \) and then lower PN.

The simulated transient waveform of the proposed QVCO, and the corresponding waveforms from three kinds of other QVCOs, BS-QVCO, and P-QVCOs using FB and SSB respectively, are shown in Fig. 5. All of the QVCOs are optimized to dissipate the same power consumption from a voltage supply of 1.8 V. It can be easily found that, due to the SSB and special coupling techniques, the amplitude of the proposed Q-VCO ranks top. The amplitude of the BS-QVCO is larger than that of the P-QVCO using FB because the tail current source transistors are removed. The amplitude of the P-QVCO using SSB exhibits the second largest amplitude because of the adopted SSB technique.

The simulated relationships between the tank voltage swing and supply voltage for the four QVCOs are indicated in Fig. 6. Except for the P-QVCO using FB, which can work under the lowest supply voltage but an inferior voltage swing, the
proposed QVCO can operate under lower supply and larger voltage swing than the other two QVCOs. It also means that the proposed QVCO exhibits higher reliability. It needs to be noted that though the similar SSB technique is used, compared to the P-QVCO using SSB, the proposed QVCO can operate at a lower supply voltage because the currents through the coupling capacitor $C_c$ can help the currents through the transistors $M_{SN}$.

According to [13], the phase noise of a VCO in the $1/f^2$ region of the spectrum can be calculated as
\[ L(\Delta \omega) = 10 \cdot \log \left[ \frac{2FkT}{P_{\text{sig}}} \cdot \left( \frac{\omega_0}{2Q_{\text{eff}} \cdot \Delta \omega} \right)^2 \right] \] (3)

where \( F \) is the empirical parameter, \( k \) is the Boltzmann’s constant, \( T \) is the absolute temperature, \( \omega_0 \) is the oscillation frequency, \( \Delta \omega \) is the offset frequency from the oscillation carrier, \( Q_{\text{eff}} \) is the effective quality of the tank, and \( P_{\text{sig}} \) is the average power consumption of the tank directly proportional to the tank oscillation amplitude.

Eq. (3) indicates that, when other conditions are constant, the phase noise the \( 1/f^2 \) region is reversely proportional to the tank oscillation amplitude and \( Q_{\text{eff}} \).

In the light of the above discussion, it can be predicted that the proposed QVCO can exhibit the most excellent phase noise performance among the four QVCOs, because of the largest tank oscillation amplitude, the maximized \( Q_{\text{eff}} \), the improved \( 1/f \) noise and noiseless passively coupling capacitors. This is verified in Fig. 7, by simulated comparisons among the four QVCOs, which are carried out under the condition of the same power consumption and oscillation frequency.

It can also be seen that the P-QVCO exhibited the relatively poor phase noise performance because of the degraded \( Q_{\text{eff}} \) and noisy coupling mechanisms.

[Fig. 7. Simulated phase noise @ 920 MHz for the four QVCOs.]

At a frequency offset of 1 MHz, the phase noise of the proposed QVCO is improved by up to 10.8 dB than that of the P-QVCO using FB, and 5.6 dB than that of the P-QVCO using SSB. Because the \( Q_{\text{eff}} \) of the BS-QVCO can also be maximized, the phase noise of the BS-QVCO is much better than the two P-QVCOs, and only slightly worse than the proposed QVCO.

### 3 Measurement results

The proposed QVCO was designed and fabricated in standard 0.18 \( \mu \)m CMOS technology. The whole die occupies an area of 1283 \( \mu \)m \( \times \) 715 \( \mu \)m.
graphs of the bonding chip, the test PCB and the test-site are shown in Fig. 8, respectively. According to Fig. 8(c), it can be easily found that the chip is measured on board mainly by the Agilent E5052A Signal Source Analyzer and the Agilent MSO9404A Mixed-signal oscilloscope. The QVCO core dissipates 11 mW from a 1.8 V power supply.

The measured four output voltage waveforms of the proposed QVCO are given in Fig. 9. Also, it can be observed that there exist some duty cycle distortions and imperfect phase relationships between different outputs because of low power CMOS output buffers and mismatched layout/cables/adapters, respectively.

The measured tuning curve of the proposed QVCO is shown in Fig. 10. It can be easily seen that the oscillation frequency of the QVCO ranges from 0.88 to 1.04 GHz corresponding to the control voltage varied from 0 to 1.8 V. Fig. 11 shows the measured phase noise versus the offset frequencies. The measured phase noise is $-71.2 \text{ dBc/Hz@1 kHz}$ and $-113.1 \text{ dBc/Hz@1 MHz}$.

In order to evaluate the overall performance of a VCO, the contributions from all aspects must be considered comprehensively and therefore the figure of merit ($FOM_T$) is adopted, in which the influence from the tuning range is also included. The $FOM_T$ is defined as [14]
\[ FOM_T = -L(\Delta f) + 20 \log \left( \frac{f_0}{\Delta f} \right) + 10 \log \left( \frac{1 \text{ mW}}{P_{DC}} \right) + 10 \log \left( \frac{TR(\%)}{V_{Tune}} \right) \]  

(4)

where \( \Delta f, L(\Delta f), f_0, P_{DC}, TR(\%) \) and \( V_{Tune} \) represent the offset frequency, the phase noise, the oscillation frequency, the power consumption, the relative tuning range and the tuning voltage range, respectively. The \( FOM_T \) of the proposed QVCO are 189.7 dBc/Hz and 171.6 dBc/Hz, which correspond to the offset frequencies of 1 kHz and 1 MHz, respectively. The reason why the \( FOM_T \) at the offset frequency of 1 MHz became worse is that the phase noise is degraded which caused mainly by thermal noise.
Table I summarizes the performance of the proposed QVCO and compares it with prior arts. From the $FOM_T$ of 189.7 dBc/Hz at the offset frequency of 1 kHz, the proposed QVCO achieves the most excellent performance among Table I. And even from the $FOM_T$ of 171.6 dBc/Hz at the offset frequency of 1 MHz, it also exhibits performance comparable to the first three previously published QVCOs.

| Ref  | Freq. (GHz) | Power (mW) | Area (mm²) | TR (%) | Phase Noise (dBc/Hz) | $FOM_T$ (dBc/Hz) |
|------|-------------|------------|------------|--------|----------------------|-----------------|
| [11] | 4.9         | 21.2       | 3.31       | 6.2    | −113@2 MHz           | 171.1           |
| [15] | 5           | 19.8       | 0.88       | 14.6   | −114.3@2 MHz        | 175.8           |
| [16] | 10          | 14.4       | 0.17       | 15.0   | −95.0@1 MHz         | 172.6           |
| [17] | 7.91        | 24         | 0.68       | 3.1    | −117.0@1 MHz        | 186.1           |
| This work | 0.885      | 11         | 0.92       | 18.0   | −71.2@1 kHz/      | 189.7/          |
|      |             |            |            |        | −113.1@1 MHz       | 171.6           |

4 Conclusions

A CMOS LC QVCO is presented and fabricated in standard 0.18 µm CMOS technology, in which passively capacitor coupling, actively bottom-series coupling techniques and the splitting switched biasing technique are combined to improve its phase noise. Measured results shows that from a 1.8 V power supply and an oscillation frequency of 885 MHz, the proposed QVCO achieved phase noise of $−71.2$ dBc/Hz@1 kHz and $−113.1$ dBc/Hz@1 MHz.
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