Investigation of 7T SRAM Cell for IoT based devices

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Abstract. Internet of Thing (IoT) based devices require the design of ultra-low power Static Random Access Memory (SRAM) to sustain the long battery life. In present work, for execution different types of SRAM cell methodologies Cadence Virtuoso tool is used and all considered methodologies read and write operations have been supervised out. These SRAM cell methodologies various parameters also have been calculated, there are read static noise margin (RSNM), write static noise margin (WSNM), read delay, write delay, read power and write power. For low read, write power dissemination and faster read and write working new 7T SRAM cell methodology is proposed. It has been recognized that new 7T SRAM cell methodology as collated to 6T to 9T SRAM cell methodologies read power consumption reduced by 1.60× to 4×. New 7T SRAM cell methodology as collated to traditional 6T, 8T and 9T SRAM cell write power consumption is decreased by 2.3× to 2.6×. It is also noticed that as collated to 6T, 8T and 9T SRAM cell methodology that new 7T SRAM read delay suppressed by 2.40× to 2.60× and its write delay is also suppressed by 3.80× to 99×. As collate to 6T to 9T SRAM cell methodologies write operation robustness of new 7T SRAM cell is 3.0× to 6.5× perform in better way. New 7T SRAM cell has the tradeoff that its read operation robustness is 6× to 14× lesser as collate to 6T, 8T and 9T SRAM cell methodologies. Due to low power consumption and less delay new 7T SRAM cell methodology is suitable for Internet of things (IOT) based devices.

Keywords: Write Delay, Read Delay, Write Power, Read Power, SRAM Cell.

1. Introduction
An enormous growth has been carried out in the field of Internet of Things (IoTs) based devices such as sensor nodes, remote sensing etc. In such devices, Static random access memory (SRAM) is utilized to store the information and also occupy a large portion of system on chip area. A huge part of system energy is dominated by SRAM which becomes the key supplier of power dissipation. Therefore, low power SRAM cell design is a big challenge for such applications to maintain long battery life. Now a day’s semiconductor SRAMs are broadly used in computer systems, microprocessors and systems on chips (SoCs) based totally equipments. Memory consists of seventy to eighty percentage locations of processors that capacity its take a lot of area in the system. In other meaning we can say that its electricity consumption will be extra and its leakage electricity dissipation will additionally be high [2,3]. SRAM and DRAM holds the information but each the working strategies are different. DRAM wants that information to be refreshed or hold the information after a defined time but SRAM does not have this problem. SRAM does no longer required to be refresh again and again. SRAM is uncertain in nature that shows it does not holds the...
information in terms of zero’s and one’s when the supply is cut off completely. To refresh the DRAM again and again it requires extra networks which make the DRAM steady and bulky [4,5]. One greater complication with the DRAM is its electricity consumption is also excessive as compare to SRAM. So the DRAM is much less advisable as examine to SRAM. Due to these above motives SRAM is extensively used in SoCs due to ease of usability and excessive speed. Different kinds of SRAMs are on hand in market like traditional 6T to 9T SRAM cells. SRAM cell based caches are plenty famous in the market. Internet of things (IOT) contains SRAM, wireless devices, microcontroller and sensors. Battery life is main parameter for IOT devices because these devices are portable and light weight so we have to focus on low power consumption SRAM cell [6,7].

2. Literature Methodologies

2.1 Traditional 6T SRAM Cell

Traditional 6T SRAM cell diagram is appeared in fig.1. For the read performance word line to be logic high at that point pulling up pass transistors NM3 and NM4 are used. It presents the input pass to the PM2, NM2 and PM0 and NM0 transistors. For small time period pull down transistor and pull up transistor turns into short when the switching operation operates in the circuit. It generates the static impact in the network i.e. the power supply VDD and ground that will increase the static power consumption so the gross power consumption will become increases [5, 6] and implementation of gating NMOS transistor at pull down facet of the circuit static power consumption can be reduce.

2.2 7T SRAM Cell

7T SRAM cell is carried out to decrease the static power consumption and enhance the read cycle. In this methodology another transistor M7 is treated as feedback to intensify excessively larger value from second inverter to first inverter and at the write operation transistor NM4 is switched off and all through the write performance transistor NM4 is switched off. The read cycle can be enhanced due to gauging of transistors NM3 and NM4 [1, 2]. This methodology diagram is appeared in fig.2.

![Fig: 1. Traditional 6T SRAM Cell](image-url)
2.3 8T SRAM Cell
In this 8T SRAM cell another inverter network is connected to detach the unintended write throughout the read cycle performance. When the read cycle is executed then the read bit line capacitor is charge up to VDD. The read performance takes place solely when read word line (RWL) and read bit line (RBL) additionally logic "0" and logic "1" and it relies upon on both the Q is "1" or Q is "0" respectively.

2.4 9T SRAM Cell
To save one bit of information two inverter circuits are consecutively attached. For writing into the cell write bit line (WBL) is utilize, read bit line (RBL), transistor NM1, NM2, NM4, NM5 and PM2 are used at the time of read performance. Due to this construction data steadiness can be upgraded [2, 4]. 9T SRAM cell diagram is appeared in fig.4.
3. Proposed Methodology

3.1 New 7T SRAM Cell Methodology

Due to the fact NMOS is enough to passing ground; one NMOS is attached between circuits and ground in proposed New 7 T SRAM cell methodology. To provide input to this additional transistor, this NMOS transistor gate terminal is connected with Q terminal. This impact reduces the dynamic power and static power dissipation so the average power dissipation reduces [6,8,9]. New 7T SRAM cell methodology diagram is shown in fig.5. In 90 nm technology, with the usage of Cadence virtuoso new 7T SRAM cell methodology has been proposed. New 7T SRAM cell provides the suitable performance in the way of low power consumption; larger speed and desirable read performance with the small trade off in write stability. The read and write operation SRAM cells depends upon the bit lines BL, BL_Bar and word line (WL). When the WL is linked with the supply VDD, it allows the access to the nodes Q and Q_bar through pass transistors NM2 and NM3.
Same as for the read performance, word line (WL) is connected with power supply VDD so each bit line and bit line bar additionally to be high through pass transistor NM2 and NM3. If either of the nodes Q or Q_bar is low, so adjoining bit line BL or BL_Bar lines begins discharging and finally the information can be accessed by the sense amplifier.

### 4. Simulation Results

**Table 1. SRAM Cell Methodologies for Read and Write Power**

| SRAM Cell Methodologies | Read Power in μW | Write Power in μW |
|-------------------------|------------------|-------------------|
| 6T SRAM Cell            | 25.7             | 53.9              |
| 7T SRAM Cell            | 20.0             | 67.8              |
| 8T SRAM Cell            | 69.6             | 29.8              |
| 9T SRAM Cell            | 33.8             | 67.93             |
| New 7T SRAM Cell        | **17.0**         | **47.0**          |
The proposed New 7T SRAM cell read power consumption is 17.0 μW. It is 4× and 2× smaller as collated to 8T and 9T SRAM cell respectively and also 68% and 16.5% smaller as collated to 6T and 7T SRAM cell respectively.

New 7T SRAM cell methodology write power consumption is 47.0 μW. It is 13%, 45% and 45.5% smaller as collated to traditional 6T, 7T and 9T SRAM cell. Its write power consumption is 36.0% more as collated to 8T SRAM cell.

| SRAM Cell Methodologies     | Read Delay in ps | Write Delay in ns |
|-----------------------------|------------------|-------------------|
| 6T SRAM Cell                | 415.8            | 53.9              |
| 7T SRAM Cell                | 53.8             | 2.15              |
| 8T SRAM Cell                | 454.9            | 56.0              |
| 9T SRAM Cell New 7T SRAM    | 420              | 0.90              |
| Cell                        | **17.7**         | **0.56**          |
New 7T SRAM cell methodology read delay measurement is 17.7ps. It is 2.5×, 2.6× and 2.4× smaller as collated to 6T, 8T and 9T SRAM cell methodologies respectively and 3.3× larger as collated to 7T SRAM cell.

New 7T SRAM cell methodology write delay measurement is 0.56ns. It is 96×, 3.8× smaller as collated to 6T and 7T SRAM cell respectively. Its write power consumption is also 99× and 1.5× smaller as collated to 8T and 9T SRAM cell methodologies.

| SRAM Cell Methodologies | WSNM (mV) | RSNM (mV) |
|-------------------------|-----------|-----------|
| 6T SRAM Cell            | 165       | 160       |
| 7T SRAM Cell            | 79.8      | 14.9      |
| 8T SRAM Cell            | 139.5     | 349.5     |
| 9T SRAM Cell New        | 159.2     | 149.4     |
| 7T SRAM Cell            | 189       | 24.9      |
In this paper, a detailed analysis of the New 7T SRAM cell methodology shows that the write static noise margin (WSNM) is 189mV. This is 15%, 92%, and 87% more compared to 6T, 7T, and 9T SRAM cell methodologies respectively, and 83.8% smaller compared to 8T SRAM cell.

Fig.10A: SRAM Cell Methodologies VS WSNM

New 7T SRAM cell read static noise margin is 24.9mV. It is 6.5× and 3.0× less compared to traditional 6T and 7T SRAM cell. Its value is also 5.8× and 6.5× less compared to 8T and 9T SRAM cell.

Fig.10B: SRAM Cell Methodologies VS RSNM

5. Conclusion

In this manuscript, Cadence virtuoso tool has been utilized to design and simulate the proposed 7T SRAM cell. We have calculated the read and write power consumption, read and write delay measurement, RSNM and WSNM of the New 7T SRAM topology of all 6T to 9T SRAM cells. New 7T SRAM cell methodology is 1.6× to 4.2× power compatible in the way of read power consumption and 2.4× to 2.6× power compatible in the way of write power consumption. It is also calculated that new 7T SRAM cell methodology is 2.5× to 2.6× rapid in terms of read delay measurement and 3.8× to 99× rapid in the way of write delay measurement. It is 3× to 6.6× sturdy for the write behavior and also its read sturdiness is 6.2× to 14.2× less which is not in the favorable position compared to 6T to 9T SRAM cell methodologies so its takes as the tradeoff.

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