Monolithic microfabricated ion trap chip design for scaleable quantum processors

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Abstract. A design is proposed for a novel ion trap quantum processor chip, microfabricated using a process based on planar silica-on-silicon techniques. The trap electrodes are of gold-coated silica and are spaced by highly doped silicon in a monolithic structure. This design allows a unit aspect-ratio trap with an ion-electrode separation below 100 $\mu$m, when using current fabrication techniques. The trapping potential is modelled and the operating parameters required to achieve motional frequencies of a few MHz are calculated. RF loss and the resultant heating of the trap chip are not found to be a factor limiting the trap’s operation. This monolithic unit aspect-ratio trap is therefore expected to exhibit a deep potential well, high trap efficiency, and a low RF loss, when compared to other microfabricated traps. This technological approach is in principle scaleable to complex devices, and may form the basis for large-scale ion trap quantum processors.

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1. Introduction

The prospect of an operational quantum information processor [1] is the most significant driver for ion trap research at present. Experimental demonstrations such as quantum gates [2, 3], algorithms [4, 5], deterministic teleportation [6, 7], and ion–photon entanglement [8] have positioned trapped ions as a viable technology for quantum information processing (QIP). While current experiments have been performed using only a few qubits at most [9, 10] the scaling up of devices to contain large numbers of qubits remains a significant challenge. The original proposal for QIP with trapped ions [11] requires a linear string of ions in a single trapping potential, where the ions’ internal electronic energy levels represent the qubit logic states, and the mutual Coulomb interaction facilitates the transfer of quantum information between the ions. The technical challenges associated with manipulating a large number of ions in a single trap are considerable, hence an alternative architecture based on an array of many interconnected ion traps has been proposed as a processor for a large number of qubits [12]. Such a device would contain distinct logic and memory zones for processing and storing qubits respectively, and would shuttle ions between the zones. This paper describes a general design for a monolithic ion trap chip, which is scaleable to many (i.e. 10^2–10^3) trapping segments, and which can be fabricated using a process based on conventional planar silica-on-silicon techniques.

Traps made of gold-coated, laser-machined alumina [13]–[15] have been used to demonstrate QIP operations and shuttling of ions. The limitations of this fabrication technology (the minimum achievable feature size, requirement for post-processing assembly, and serial fabrication process) mean that it is unlikely to be used for a large-scale ion trap quantum processor. A two-layer ion trap, with electrodes of boron-doped silicon spaced by borosilicate glass, has also been demonstrated [16], but requires post-processing assembly of the electrode and insulator layers. Geometries suitable for monolithic microfabricated ion traps include asymmetric planar electrode structures [17], and symmetric, three-dimensional (3D) high aspect-ratio structures [18]. Operational ion traps based on these geometries have been demonstrated recently [19, 20]. The latter geometry is perhaps more demanding to fabricate than the former; however it enables
greater optical access and results in a deeper trapping potential. This paper proposes a symmetric trap geometry that is also monolithic and suitable for microfabrication, but which possesses additional advantages over the GaAs semiconductor chip trap demonstrated by Stick et al [20]. Specifically, our design possesses a unit aspect-ratio resulting in a deeper trapping potential (up to $\sim 7$ times that of the GaAs trap), while maintaining adequate optical access ($f/# = 1$). In addition, it uses metallic electrodes and a low-loss dielectric, resulting in significantly lower heating of the ion trap chip. It is expected that by using silica-on-silicon processing techniques, this design can be used to create traps where the characteristic ion-electrode separation, $R$, varies by over an order of magnitude in the range $20 \mu m < R < 350 \mu m$.

Other groups are also investigating alternative microfabrication approaches. For example, Slusher [21] has been developing planar ion traps constructed on a p-doped silicon wafer; the electrodes are tungsten/aluminium conductors and are spaced by SiN and SiO$_2$ dielectrics. Compatibility with CMOS technology is one of the criteria central to this design. In contrast, MEMS techniques have been employed by Blain et al [22]–[24] to develop planar segmented traps; the trap is constructed on a silicon substrate, uses SiO$_2$ and Si$_3$N$_4$ as dielectrics, and has gold-coated tungsten electrodes. 3D trap configurations are possible using MEMS processes.

This paper is organized as follows: section 2 provides an explanation of the basic concept and geometry of the trap. The structure described can be fabricated using standard silica-on-silicon processing techniques (or variations thereof), which are outlined in section 3. Finite element models have been used to demonstrate that the proposed design provides a trap potential suitable for QIP applications; these are described in section 4. A few possible practical limitations to effective trap operation are considered in section 5, where it is also shown that these can be overcome.

2. Geometry

A linear Paul trap [25] can be deformed significantly from its idealized hyperbolic geometry, yet still maintain a harmonic potential, provided the ion is close to the trap axis (i.e. the ion’s vibrational quantum number, $n$, is small). Examples of such deformations to the trap geometry include changing the number of electrodes [13, 26] or having all of the electrodes in a plane [17]. However, while different realisations of linear Paul traps may appear dissimilar, the basic physics of the trapping potential remains unchanged, save for a dimensionless geometrical factor, $\eta$, known as the trap efficiency. Different trap designs are all necessarily constrained by the physics of the trapping potential, fabrication considerations, and practical limitations such as material properties.

The most elementary unit cell of the trap required to provide a confining potential is shown in figure 1. The radially confining potential is created by applying an RF voltage, $V_0$, to a pair of electrodes which run the full length of the trap, while all other electrodes are held at RF ground. The ion is confined axially by a DC voltage, $V_{DC}$, applied to the four end-cap segments. For realistic traps, imperfections in processing and stray charges on insulating surfaces can displace the ion from the trap axis, leading to excess micromotion [27]. By applying DC voltages, $V_{C1}$, $V_{C2}$, to the compensation electrodes and across the trap segment electrodes, micromotion can be minimized independently in each trapping region. Throughout this paper, we use the co-ordinate reference frame shown in figure 1, with unit vectors $\hat{x}$ (perpendicular to the trap axis, in the plane of the wafer), $\hat{y}$ (perpendicular to the plane of the wafer), and $\hat{z}$ (parallel to the trap axis).
Figure 1. Elementary unit cell and electrode connections. An RF voltage, $V_0$, on each of two electrodes running the full length of the trap provides the radial ($xy$) trapping potential, where the trap axis is shown as a dotted line. A DC voltage, $V_{DC}$, is applied to the four end cap electrodes and provides axial ($z$) confinement. The voltages $V_{C1}$ and $V_{C2}$ can be applied to compensate for micromotion.

Figure 2. Trap design concept and parameter definitions. The electrodes are made of gold-coated SiO$_2$ layers, which are spaced by doped silicon. The entire construction is created from a single silicon wafer, and the section shown can be extended to include many more than three segments, or more complicated geometries.

A cut-away section of the design proposed in this study is shown in figure 2. The electrodes shown in figure 2, formed by a 5 $\mu$m layer of gold overlaid on 15 $\mu$m of SiO$_2$, are spaced by highly doped silicon. In the calculations presented here, we consider silicon wafers of different thickness, $d$, in the range 40 $\mu$m < $d$ < 500 $\mu$m. However, we note that thinner wafers are routinely available. The structure shown in the figure is part of a larger ‘chip’, the dimensions of which are dictated by packaging and electrical connectivity requirements. The un-etched areas of the chip, away from the trapping region, provide mechanical support for the trap electrodes,
Table 1. Typical dimensions for different sizes of traps. All of these dimensions are achievable using existing silica-on-silicon fabrication processes.

| Parameter                          | Value | Units |
|------------------------------------|-------|-------|
| Ion–electrode separation, $R$      | 350   | $\mu$m |
| Wafer thickness, $d$               | 500   | $\mu$m |
| Electrode separation, $a$          | 500   | $\mu$m |
| Recess depth, $h$                  | 300   | $\mu$m |
| RF-DC electrode spacing, $G$       | 50    | $\mu$m |
| DC-DC electrode spacing, $g$       | 10    | $\mu$m |
| Electrode length, $b$              | 20 to 1000 | $\mu$m |
| Silica thickness, $w$              | 15    | $\mu$m |
| Gold thickness, $t$                | 5     | $\mu$m |
| RF electrode width, $l$            | 20    | $\mu$m |
| Distance to edge of chip, $L$      | $\sim$4000 | $\mu$m |

and are gold patterned with bonding pads for electrical connectivity. The size of the trap is characterized by $R$, the distance from the trap axis to the nearest point on the electrodes. Table 1 lists examples of the physical dimensions indicated in figure 2, for three traps of differing size.

The three segments considered here give a single trapping zone. However, by extending the design to include more segments, many independent trapping zones can be achieved. The geometry of different trapping zones can then be optimized for specific purposes, e.g. for loading, storing, shuttling and optically addressing ions, and for bringing together and separating small numbers of ions.

3. Fabrication

The structure described above can be micro-fabricated using planar processing techniques developed in the photonics industry. The processing steps required involve standard techniques, although some are used in a novel context. To fabricate the proposed trap design, a silicon wafer is oxidized and then processed using lithographic patterning, anisotropic and isotropic etching, and metallic evaporation and electroplating. A simplified version of the processing stages is illustrated schematically in figure 3; these are now outlined sequentially.

1. Thermal oxidation of silicon wafer, resulting in a 15 $\mu$m thick layer of SiO$_2$ on both surfaces of the silicon wafer.
2. Inductively coupled plasma (ICP) etch of SiO$_2$, thus exposing the silicon where the volume of free space is desired.
3. Evaporation of 100 nm of gold on SiO$_2$, resulting in electrode pattern. This also forms the mask for etching the segmented DC electrodes.
4. ICP etch of SiO$_2$ to create individual segmented DC electrodes. The compensation and RF electrodes are masked from this processing step.

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5. Isotropic wet etch of silicon to create the clear aperture through the structure and the free-space undercut between the two parallel SiO\textsubscript{2} layers.

6. Shadow evaporation of gold to coat the edges and surface of the SiO\textsubscript{2} in the undercut. This creates a continuous surface of gold from the outside of the electrodes to the underside. A nickel mask is then evaporated on to gold surfaces of the DC electrodes in the undercut.

7. Wet etch of the gold between the DC segments, then removal of the nickel mask. A further wet etch of silicon ensures no electrical connection between gold in the undercut and the silicon.

Titanium is laid down as a base layer on the SiO\textsubscript{2}, prior to the gold evaporation, to ensure the gold adheres to the surface. Following the processing steps listed above, the gold electrodes are electroplated to a thickness of 5 \(\mu\text{m}\), with surface roughness specified to be \(< 10\) nm RMS. The steps described involve standard techniques, although some are used in a novel context—most notably coating the underside of the SiO\textsubscript{2} cantilevers (step 6). This processing step can be achieved by tilting the angle of the wafer with respect to the evaporation source, while using the 3D structure to mask the section of the undercut that should not be coated. The use of existing structures to shadow-mask certain regions during evaporation of metals (including gold) is an established and controllable technique. It has been used for some time in the fabrication of high contrast grating structures [28], and provides a high quality surface finish [29]. It has also been used to fabricate thin film microstructures [30]. While the technique is in principle established, we expect that it may require some development for the application presented in this work.

The trap designs specified by figure 2 and table 1 (where 150 \(\mu\text{m} < d < 500\) \(\mu\text{m}\)), are expected to be achieved using existing processes, or modifications thereof. However, the process does set limits on the degree to which particular parameters can be varied. Currently, the minimum wafer thickness \((d \sim 100\) \(\mu\text{m}\)) is set by the decreasing yields expected for increasingly thin and fragile wafers. This limit may be overcome by further process development, or by using silicon-on-insulator (SOI) fabrication methods. The maximum SiO\textsubscript{2} layer thickness in our design is
limited by the rate at which it can be grown. The duration of the thermal oxidation process increases exponentially with the required oxide thickness, e.g. 1 µm of SiO₂ can be grown in ~ 3 hours, while the 15 µm used in our designs takes 24 days. (In contrast, the minimum SiO₂ thickness is set by RF heating considerations which are described in section 5.) This thermal oxidation process is used in the fabrication of photonic devices containing silica-on-silicon planar lightwave circuits (typically constructed on a plane of 16 µm thick SiO₂). The low-loss optical quality of resulting devices demonstrates the low density of defects present in the thermal oxide, together with the uniformity of the oxide density [31]. It may be noted that other oxidation techniques, such as high pressure oxidation, can deposit SiO₂ faster, although these oxides are of a lower optical quality than thermal oxides. The dimensions of the gold features in the xz plane are constrained by the fabrication process to be greater than or equal to the gold layer thickness. The 5 µm thickness of the gold layer is chosen to ensure that the resistance of the RF lines is sufficiently small to avoid excessive resistive heating. However, this constraint can be relaxed in smaller traps where the required RF voltages are smaller. Further details of this reasoning are given in section 5.

Extending the design to incorporate many segments of varying sizes is simply a matter of mask design. Increasingly complex traps do not necessarily lead to increased complexity of fabrication. Masks can be positioned with alignment accuracy of 1 µm between the top and the bottom of the wafer allowing precise placement of the electrode structures, even for traps fabricated on the 10 µm scale.

4. Trapping potential modelling

This section considers the effective potential due to a somewhat idealized set of electrodes. Motional frequencies and trap depths are calculated for a range of trap sizes, voltages and drive frequencies. This is done to show that in principle, the geometry described here can provide a stable trapping potential for achievable experimental parameters.

4.1. Motional frequencies

For a given fidelity of operation, the speed of a Cirac–Zoller type ion trap quantum processor scales as the geometrical mean of the ions’ motional frequency and the photon recoil frequency associated with the ion string [32]. Any practical ion trap for QIP applications should therefore have as high a motional frequency as possible. Frequencies currently realized are in the range of several megahertz, e.g. an axial centre of mass (COM) mode of \( \omega_{\text{COM}}/2\pi = 3.4 \text{ MHz} \) has been used when creating a six ion-entangled state [9], and a breathing mode for two ions of \( \omega_{\text{b}}/2\pi = 2.1 \text{ MHz} \) was used in a C-NOT gate [2]. (For comparison, this implies \( \omega_{\text{COM}}/2\pi = 1.2 \text{ MHz} \).) Operation in this regime is therefore a criterion for the proposed trap design.

The physics of linear RF ion traps is well understood, and there exist extensive reviews in the literature [33, 34]. If the axial confinement of a linear string of \( N \) ions is too strong compared to the radial confinement, then the string undergoes a dimensional phase transition from 1D to 2D. The strength of the confinement is characterized by the ions’ motional frequencies, and it has been found numerically that to maintain a linear string, the motional frequencies must obey...
the inequality [35]⁴:

\[ \omega_{z\text{COM}} < 1.57N^{-0.87}\omega_{r-}, \]  

(1)

where \( \omega_{r-} \) is the lower radial motional frequency (in the general case where the radial frequencies are non-degenerate). It should be noted that the axial COM motional frequency of a string of \( N \) ions is independent of \( N \) [11, 36]. To achieve a linear string of four ions with \( \omega_{z\text{COM}}/2\pi = 2 \text{ MHz} \) therefore requires \( \omega_{r}/2\pi > 4.3 \text{ MHz} \).

In calculating the requirements for such a radial motional frequency, the trapping potential must first be stable, which requires that a dimensionless stability parameter, \( q \), must be within certain limits [37]. Typically, trap operating conditions are chosen such that \( q \sim 0.6 \) (e.g. [15, 20]). Given a fixed \( q \), an ion’s radial motional frequency, \( \omega_r \), is proportional to the drive frequency, \( \Omega_T \). Provided \( q^2 \ll 2 \), and neglecting pertubations from the end cap voltages, this can be approximated as [34, 38]:

\[ \omega_r \simeq \frac{q}{2\sqrt{2}}\Omega_T. \]  

(2)

The RF voltage required to achieve a certain \( q \) is dependent on the characteristic size of the trap, \( R \), and on the mass of the ion, \( M \). It is given by

\[ V_0 = \frac{4M\omega_r^2R^2}{q\eta Q}, \]  

(3)

where \( V_0 \) is the RF amplitude, \( Q \) is the charge on the ion, and \( \eta \) is the so-called ‘efficiency’ of the trap. This efficiency is the ratio of the quadrupole part of the potential generated by a given trap, to that of a hyperbolic trap with the same ion-electrode separation, \( R \) [18]. This is equivalent to the ratio of an ion’s motional frequency in a given trap, to its motional frequency in a hyperbolic trap of the same \( R \). In general this geometrical factor cannot be calculated analytically, but requires a numerical approach.

The proposed design’s trapping potential (and hence efficiency) was modelled using the finite element package FEMLAB⁵ and following the reasoning of Madsen et al [18]. In this approach the transverse potential is calculated for a specific electrode geometry. A standard MATLAB⁶ fitting algorithm decomposes this into a series of cylindrical harmonics; the magnitude of the quadrupole term is then compared to that of an ideal hyperbolic trap of the same dimension, \( R \). The ratio of these two terms is the trap efficiency. The largest uncertainty in the calculation is due to the coarseness of meshing in FEMLAB, which is set by practicalities of computing power and duration of the calculation. Comparisons with analytically solvable examples (namely a trap in the limit of high aspect ratio [18], and a hyperbolic trap) suggest an uncertainty in the calculated efficiency of less than 1%. It is possible that boundary element methods (BEM) may offer improvements in precision and speed of calculation over the finite element methods (FEM) used here [39].

⁴ Note: (1) is derived from figure 4 of this reference. The figure requires that \( c = 10^{0.395} \), rather than \( c = 0.395 \) as given in the text.

⁵ FEMLAB 3.2, COMSOL, Inc., MA. 2004. Now called COMSOL Multiphysics.

⁶ MATLAB 7.1, The MathWorks, Inc., MA. 2005.

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For traps of the design proposed here, the efficiency increases with decreasing size, from $\eta = 70\%$ for a trap with $R = 350 \mu m$, to $\eta = 79\%$ for $R = 90 \mu m$. This is because the ratio $(w + 2t)/d$ increases with decreasing $R$ (see figure 2 and table 1) [18]. Using the calculated efficiencies, the voltages required to operate traps of different sizes can be calculated from (3).

Examples of the RF voltage required for different trap sizes, as a function of $\omega_r$, are shown in figure 4. For $R = 160 \mu m$, $\omega_r/2\pi = 4.3 \text{ MHz}$ is realized using $V_0 = 160 \text{ V}$ and $\Omega_T/2\pi = 20 \text{ MHz}$, thus demonstrating that reasonable frequencies can be reached with achievable experimental parameters.

The DC voltages applied to the four end-cap electrodes lift the degeneracy of the radial motional modes. This was modelled in 3D using FEMLAB. For the axial frequencies quoted above, end-cap voltages of a few volts are required. This means that the principal axes of motion will lie along the diagonal lines ($\hat{x} \pm \hat{y}$), and have frequencies split by a few hundred kHz. This orientation of the principal axes of motion is advantageous for cooling, as both radial degrees of freedom can be cooled by a single laser with a $k$-vector along the $y$-axis of the trap.

4.2. Trap depth

It is desirable that the trap depth is significantly greater than the kinetic energy of ions loaded directly from a thermal atomic source. This enhances the probability of loading ions, and minimizes the likelihood of ion loss due to collisions with the background gas [20]. In practice, this requires potential depths of $\sim 1 \text{ eV}$. To calculate the depth of the proposed trap, the potentials due to the different electrodes were calculated numerically in 3D using FEMLAB, and then the total effective potential determined as the sum of the pseudo-potential [18] and the DC end-cap potentials.

To compare different sized traps, $\Omega_T$, $V_0$ and $V_{DC}$ were chosen to ensure that up to four ions can be trapped in a stable linear string. The results for traps with $R = 160 \mu m$ and $R = 90 \mu m$ are summarized in table 2. The trap design presented here was also compared to a microfabricated trap which has demonstrated successful operation; the calculation of trap depth was repeated running the proposed trap design under the same conditions ($R$, $\Omega_T$, $V_0$ and $V_{DC}$) as were used for the high aspect ratio GaAs trap [20]. The silica-on-silicon trap proposed here has a potential depth of 0.6 eV, which is seven times deeper than that of the GaAs trap. This demonstrates an advantage to be gained from a unit aspect ratio geometry.

5. Practical considerations

Beyond demonstrating that the proposed design will provide a suitable trapping potential, with motional frequencies and trap depths appropriate for QIP applications, there are several practical factors that must also be considered. Specific requirements of the trap include: an integrated way of compensating micromotion; adequate dissipation of heat generated in non-perfect conductors and dielectrics; electrical breakdown voltages which are well above required operating conditions; minimal ion heating rate, $\dot{n}$; and mechanical integrity of the structure.

5.1. Micromotion compensation

Imperfections in fabrication or stray charges on insulators can perturb the ideal trapping potential in a real trap, leading to excess micromotion [27]. The area of the bare insulating surfaces
Figure 4. Voltage required to achieve a specific radial motional frequency for traps of ion–electrode separation in the range $30 \mu m < R < 350 \mu m$, assuming $q = 0.6$ and $^{88}\text{Sr}^+$ ion species.

Table 2. Summary of trap depths for different trapping conditions. For $160 \mu m$ and $90 \mu m$ traps the parameters $V_0$, $V_{DC}$, and $\Omega_1$, were chosen to confine four ions in a 1D string with $\omega_z/2\pi = 2$ MHz. For the $30 \mu m$ trap, the conditions were chosen to mimic those of [20].

| Parameter                              | Value | Units |
|----------------------------------------|-------|-------|
| Trap size, $R$                         | 160   | $\mu m$ |
| $^{88}\text{Sr}^+$, $^{88}\text{Sr}^+$ | 90    | $\mu m$ |
| $^{111}\text{Cd}^+$                   | 30    | $\mu m$ |
| Wafer thickness, $d$                   | 250   | $\mu m$ |
| RF voltage, $V_0$                      | 170   | V     |
| End-cap voltage, $V_{DC}$              | 5.1   | V     |
| Trap drive frequency, $\Omega_1/2\pi$ | 21    | MHz   |
| Radial motional frequency, $\omega_r/2\pi$ | 4.5   | MHz   |
| Axial secular frequency, $\omega_z/2\pi$ | 2.0   | MHz   |
| Trap depth                             | 5.3   | 0.6 eV |

near the trap has been reduced as much as possible: the underside of the SiO$_2$ in the undercut is coated to within $50 \mu m$ of the silicon, and the silicon itself is grounded and doped to be highly conducting. Nonetheless, dedicated compensation electrodes are required to move the ion back to the trap centre if the potential is perturbed. Ideally, the trap design should allow independent compensation of micromotion in each trapping segment. This is achieved in the proposed design using (i) compensation electrodes behind the RF electrode, and (ii) an additional potential difference across the DC trap segment electrodes (see figure 1).

The distances over which the ion is expected to move for applied compensation voltages were calculated using FEMLAB, and are illustrated for a trap with $R = 160 \mu m$ in figure 5. By applying a voltage $V_{C1}$ to the compensation electrodes (see figure 1), the potential minimum moves along the line $0.09 \hat{x} - 0.99 \hat{y}$. Adding a voltage $V_{C2}$ across the trapping segment electrodes
Figure 5. Displacement of the ion as a function of applied compensation voltage, for the $R = 160 \mu m$ trap specified in table 2. For no applied compensation voltage ($V_{C1} = V_{C2} = 0 \text{ V}$) the displacement is zero. The open points show the position of the trap minimum for increasing compensation voltage $V_{C1}$ (with $V_{C2} = 0 \text{ V}$), where each successive point is for a 1V increase in voltage. The closed points do the same for $V_{C2}$ (with $V_{C1} = 0 \text{ V}$) at 0.1V intervals.

shifts the potential minimum in the direction $-0.71 (\hat{x} + \hat{y})$. These are sufficient degrees of freedom to minimize micromotion in 2D. For example, an ion displaced by ($\Delta x = -3 \mu m$, $\Delta y = 2 \mu m$) from the trap axis because of stray charges, must be compensated by an opposite shift ($\Delta x = 3 \mu m$, $\Delta y = -2 \mu m$) to minimize the micromotion. Point S in figure 5 shows that this can be achieved using voltages $V_{C1} = 6 \text{ V}$, $V_{C2} = -0.5 \text{ V}$. Typical compensation voltages required in an existing apparatus [40], together with numerical calculations, indicate that displacements of up to 4 $\mu m$ are required to minimize micromotion.

5.2. RF heating of substrate

One of the reasons put forward for avoiding silicon-based technology [17] is the power dissipated in the material, as even highly doped silicon has a high RF loss compared to low resistivity metals, such as gold. The proposed design is expected to circumvent these problems, as the electrodes themselves are made of gold rather than silicon. The silicon is simply used as a spacing material, and is isolated from the electrodes by a 15 $\mu m$ layer of SiO$_2$. The RF loss is therefore expected to be a less significant problem than if the silicon were used as the electrode material [41, 42]. However, at RF frequencies there is still a non-negligible capacitive coupling from the gold to the silicon through the SiO$_2$ dielectric, so heating in the silicon and SiO$_2$ layers must still be considered.

To calculate the heating effects due to this RF loss, each part of the trap was modelled as a lumped element, as shown in the circuit in figure 6. This lumped element approximation is valid since the trap features ($< 5 \text{ mm}$) are much smaller than the RF wavelength ($\sim 10 \text{ m}$). The
most significant elements are: (i) resistance of the gold tracks leading to the RF electrodes, $R_A$; (ii) resistance of the gold RF electrodes, $R_B$; (iii) resistance of the DC electrodes, $R_C$; (iv) resistance of the silicon from the trapping region to ground, $R_D$; (v) capacitance between the RF electrode and the compensation electrodes, through the SiO$_2$, $C_E$; (vi) capacitance between the gold track to the RF electrodes and the silicon substrate, through the SiO$_2$, $C_F$. Other dissipative elements were also considered, but were found to be negligible compared to those listed here. To model the power dissipated in the trap structure, capacitances were calculated assuming the components consisted of either a pair of parallel plates or long thin wires, depending on which geometry was the closer approximation. The loss in the capacitors is due to the loss tangent of the SiO$_2$, $\tan \delta = 4 \times 10^{-5}$ [43].

The introduction of a dopant can change the silicon resistivity by several orders of magnitude. In the limit of the silicon having a high resistance, no current would flow through it, while in the limit of low resistance, no voltage would be dropped across it. In both cases very little resistive heating occurs, but between the two extremes significant amounts of heat may be produced. Using the circuit shown in figure 6, and for a trap with $R = 160 \mu$m; RF electrode length, $L_{RF}$, of 3.2 mm (cf figure 2) and $\omega_r/2\pi = 4.5$ MHz, the power dissipated in the various parts of the trap is shown in figure 7. Pure silicon is near the worst case, with the total thermal power generated $P_{th} \sim 1$ W. No reduction in heating occurs when the silicon resistivity is below $\sim 10^{-3}$ $\Omega$cm, since losses in other materials dominate. Choosing this value of the silicon resistivity, $P_{th} = 0.4$ mW. With reference to figure 6, the dominant sources of heat are capacitances $C_E$ and $C_F$, and resistances $R_B$ and $R_D$.

In calculating the upper limit to the chip’s temperature rise due to 0.4 mW of generated heat, it is assumed that radiation is the only effective heat loss mechanism. The heat is generated in localized volumes within the chip, and must be conducted efficiently throughout the chip to
avoid excessive local heating. A very simple thermal transport model was developed to estimate the temperature gradient across the chip. By modelling each part of the trap as a lumped thermal resistance, a heat load of 0.4 mW leads to a temperature variation of less than 100 mK across the chip. The temperature gradient is small because any heat generated in the thin SiO₂ layer is well heatsunk to the gold and silicon layers, which are good conductors. Given this expected thermal uniformity, it is reasonable to model the chip as a blackbody radiator of uniform temperature, in a room temperature heat bath. Of the chip’s total surface area, ~ 50% is likely to be gold-coated tracks leading to the trap electrodes. Since gold has a very low emissivity (ε = 0.03) compared to SiO₂ (ε = 0.8), only ~ 50% of the surface area is an effective radiator. For a 9 mm × 9 mm square chip, 0.4 mW of heat yields a 10 K temperature rise to 303 K.

This calculation has been performed for traps of other sizes. The RF electrode length, $L_{RF}$, was scaled with R and the chip size remained as a 9 mm × 9 mm square. The results of this calculation are presented in table 3, and show that as the characteristic trap size $R$ decreases, the thermal power generated and the chip’s temperature rise also decrease. An approximate reasoning suggests that this is to be expected: for a constant motional frequency, $\omega_t$, $P_{th} \propto R^4$ (because $P_{th} \propto V_0^2$ and $V_0 \propto R^2$ cf (3)). In reality, as the trap size is reduced, not all the components are scaled in proportion. Specifically, the SiO₂ thickness, and the gold thickness remain at a constant value. This means that the trap efficiency, $\eta$, is not constant, and the RF losses of different components do not scale exactly with size. A full calculation was performed to investigate how $P_{th}$ scales with $R$, while maintaining a fixed motional frequency. The results, presented in figure 8, do indicate that $P_{th} \propto R^4$ is in fact a good approximation. This scaling relationship applies to the thermal power generated by a single linear trap comprising several segments. However, to realize arrays of ions stored and manipulated in a large number of interconnected traps [12],
Table 3. Summary of heating effects. Heating rates are calculated for a 9 mm × 9 mm chip, for a fixed number of segments, where the axial length, $b$, of each segment is scaled with $R$. As the traps are reduced in size, the thermal power generated in the traps is reduced, and the temperature rise due to a given number of trapping electrodes becomes smaller.

| Parameter                  | Value  | Units |
|----------------------------|--------|-------|
| Trap size, $R$             | 350    | µm    |
| RF voltage, $V_0$          | 250    | V     |
| Radial motional frequency, $\omega_r/2\pi$ | 2.3    | 4.5 MHz |
| Thermal power generated, $P_{th}$ | 800    | 400 36 µW |
| Ave. temperature gradient, $dT/dx$ | 40 20 | 1 mK mm$^{-1}$ |
| Temperature rise, $\Delta T$ | 16 10 | 1.2 K |

Figure 8. Power dissipated in the trap as a function of size. A simple model suggests that the power dissipated in the trap should scale with $R^4$ (see text), as indicated by the solid line. The points show results of a full calculation using the circuit shown in figure 6 and demonstrate that the simple approximation holds reasonably well for this design.

the areal density, $n_a$, of unit aspect-ratio traps on a single chip will need to increase. The total thermal power generated on chip, $P_{tot}$, scales with the areal density according to $P_{tot} \propto P_{th}n_a$. Since $n_a \propto R^{-2}$, then $P_{tot} \propto R^2$. As $R$ decreases to enable devices of increasing density and complexity, $P_{tot}$ and the resulting temperature rise are therefore not expected to limit the device performance.

5.3. Further considerations

There are several places in the trap where the RF electrode is in close proximity to a conductor at RF ground. It must therefore be ensured that under the operating conditions required, there is no danger of electrical breakdown. The most likely point for breakdown is expected to be
between the RF electrode and the compensation electrodes, across the surface of the SiO₂. At this point the electrodes are close, and surface effects can mean that arcing along the SiO₂–vacuum interface can occur at much lower voltages than would be possible through either vacuum or bulk SiO₂ alone [44]. This effect is not well understood, but is known to be dependent on many factors including the RF frequency, the geometry, surface finish, adsorbed gasses in the material and any history of previous arcing events. Blackburn et al [45] report devices with a DC breakdown field of ∼ 430 V µm⁻¹ across an SiO₂–vacuum interface. Results showing an AC (100 MHz) breakdown field of ∼ 30 V µm⁻¹ between sharp-edged electrodes through vacuum were presented by Gerhard et al [46]. Given the uncertainty regarding surface breakdown effects the proposed design uses a 50 µm separation between the RF and compensation electrodes, resulting in a maximum AC electric field of 5 V µm⁻¹. We conclude that this should be sufficiently low to avoid surface flashover and vacuum breakdown at a few tens of MHz.

The most significant process contributing to the heating of the ions’ motion is thought to be fluctuating patch potentials on the electrode surface. This is far from understood, although observations indicate that the ions’ heating rate, ˙n, is inversely proportional to R⁴ [13, 47]. For metallic electrodes, surface quality is also thought to be a significant parameter affecting patch potential fluctuations. The trap design proposed here uses electrodes of gold-coated silica which, after electroplating, will have a surface roughness of <10 nm RMS. This figure is entirely limited by the electroplating process and not by the surface quality of the SiO₂. This compares favourably with other traps in the literature (see for example [15]), and should help minimize the ions’ heating rate.

When a voltage is applied to the RF electrode there is an attractive force between this electrode and the DC electrodes on the opposite side of the wafer. The electrodes are therefore mechanically driven at twice the trap drive frequency, 2Ω₁/2π. It must be ensured that the mechanical resonance of the electrodes are far from this frequency. To calculate this, the electrodes were modelled as SiO₂ cantilevers of uniform rectangular cross-section with thickness, w, and length, h. These will have a resonant frequency of [48]:

$$\frac{\omega_{\text{res}}}{2\pi} = 0.16 \sqrt{\frac{E}{\rho}} \frac{w}{h^2},$$  (4)

where E = 73 GPa [43] is the Young’s modulus of SiO₂, and ρ = 2.2 × 10³ kg m⁻³ [43] is its density. For a trap with h = 300 µm, w = 15 µm (see figure 2 and table 1), this gives a resonant frequency of 154 kHz. Given that the cantilever is expected to have a mechanical Q of at least several thousand [49], this should be sufficiently far from 2Ω₁/2π to avoid resonant effects.

6. Conclusions

A design for a novel monolithic linear RF ion trap has been described. The 3D symmetric trap structure, which can be microfabricated on a chip using silica-on-silicon processing techniques, is of significant interest for implementations of QIP using trapped ions. The trap electrodes are formed by gold-coated SiO₂, and are spaced by highly doped silicon. Using current silica-on-silicon processing techniques, together with shadow evaporation techniques (used in grating and thin film microstructure fabrication), ion-electrode separations down to 90 µm can be achieved.
In principle this could be reduced to around 20 \( \mu \text{m} \) with further process development. Finite element modelling has shown that under practical operating conditions, the trap design provides deep potentials with motional frequencies of several MHz. Our design also incorporates the means to compensate micromotion independently in each of the chip’s trapping segments. Heating of the trap chip due to RF loss has been investigated, and is not anticipated to be a factor that limits the trap’s performance, even in traps with larger ion-electrode distances. The silica-on-silicon fabrication method should enable the scaling up of devices to create ion trap chips containing large 2D arrays of trapping segments, and hence many qubits.

The microfabricated trap design detailed in this paper has specific advantages over surface electrode traps [17, 19] and the high aspect-ratio GaAs chip trap [18, 20]. The unit aspect-ratio trap results in a significantly greater trap depth compared to the surface trap and the GaAs trap (up to a factor of \( \sim 7 \) deeper in the latter instance). A further consequence of the design is a greater trap efficiency; the unit aspect-ratio structure presented in this study has an efficiency twice that of the GaAs trap. As in the surface electrode trap, the gold electrodes in our trap design have a low resistive impedance, and the SiO\(_2\) dielectric has a low capacitive reactance. These features result in RF losses (and subsequent heating of the trap chip) that are calculated to be significantly lower than in the GaAs trap. Thus our design for a monolithic unit aspect-ratio trap is expected to exhibit a deep potential well, a high trap efficiency, and a low RF loss, which contrasts with some features of the other microfabricated traps. These differences will contribute to an increased understanding of ion trap materials and structures for QIP applications.

Not only is silica-on-silicon a technology which is scaleable to more complex devices, but it could be integrated with other technologies such as optical fibres, on-chip waveguides and MEMS optical components. Furthermore, as with photonics components, construction of hybrid devices which integrate electronics components on to the silica-on-silicon trap chip are feasible. Planar silica-on-silicon technology therefore has the potential to form the basis for large-scale ion trap quantum processors.

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