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DOCTORAL DISSERTATION

Title of PhD dissertation: Optimization of hybrid parallel application execution in heterogeneous high performance computing systems considering execution time and power consumption

Title of PhD dissertation (in Polish): Optymalizacja wykonania hybrydowych aplikacji równoległych w heterogenicznych systemach obliczeniowych wysokiej wydajności z uwzględnieniem czasu wykonania i poboru mocy

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ABSTRACT

English:

Many important computational problems require utilization of high performance computing (HPC) systems that consist of multi-level structures combining higher and higher numbers of devices with various characteristics. Utilizing full power of such systems requires programming parallel applications that are hybrid in two meanings: they can utilize parallelism on multiple levels at the same time and combine together programming interfaces specific for various types of computing devices.

The main goal of parallel processing is increasing the processing performance, and therefore decreasing the application execution time. The international HPC community is targeting development of "Exascale" supercomputers (able to sustain 10^{18} floating point operations per second) by the year 2020. One of the main obstacles to achieving this goal is power consumption of the computing systems that exceeds the energy supply limits. New programming models and algorithms that consider this criterion are one of the key areas where significant progress is necessary in order to achieve the goal.

The goal of the dissertation is to extract a general model of hybrid parallel application execution in heterogeneous HPC systems that is a synthesis of existing specific approaches and developing an optimization methodology for such execution aiming for minimization of the contradicting objectives of application execution time and power consumption of the utilized computing hardware. Both meanings of the application hybridity result in multiplicity of execution parameters of nontrivial interdependences and influence on the considered optimization criteria. Mapping of the application processes on computing devices has also a significant impact on these criteria.

The dissertation consists of an Introduction, two theoretical Chapters, three empirical Chapters and a Summary. The Introduction includes motivations for the study, research problem formulation, scope, main contributions, claims and overview of the thesis. Chapter 2 contains a review of existing approaches in the area of executing, modeling and simulation of hybrid parallel applications along with examples of such applications and the meaning of their hybridity. Chapter 3 contains a critical analysis of existing approaches to parallel application optimization considering execution time and power consumption with a particular emphasis on multi-objective optimization methods, computing resource management and auto-tuning of application execution parameters.

Chapter 4 describes five real-life parallel applications from various practical fields and five diverse computing systems that were the subject of experiments included in the dissertation. In Chapter 5, an optimization methodology of hybrid parallel application execution in heterogeneous HPC systems is proposed that consists of specific execution steps and a simulation method for fast evaluation of points in the solution search space. Chapter 6 presents results of experiments
with applying the consecutive execution steps to chosen real-life applications and using the proposed optimization methodology as a whole to one application of deep neural network training for automatic speech recognition.

As shown in the dissertation, the execution steps specific in the context of the proposed model, including preliminary process optimization, process mapping, parameter tuning and actual execution allow to optimize execution time of hybrid parallel applications in heterogeneous high performance computing systems, while the proposed modeling and simulation method allows for fast and accurate identification of the set of optimal solutions to the problem of multi-objective execution time and power consumption optimization.
Wiele istotnych problemów obliczeniowych wymaga wykorzystania systemów obliczeniowych wysokiej wydajności, w których skład wchodzą kilkupoziomowa struktura łącząca coraz większe liczby urządzeń o różnych charakterystykach. Wykorzystanie pełnej mocy takich systemów wymaga programowania aplikacji równoległych, które są hybrydowe w dwóch znaczeniach: potrafią jednocześnie wykorzystać równoległośność na wielu poziomach oraz łączą ze sobą interfejsy programistyczne charakterystyczne dla różnych typów urządzeń obliczeniowych. Głównym celem przetwarzania równoległego jest zwiększenie wydajności przetwarzania, a więc zmniejszenie czasu wykonania aplikacji. Międzynarodowa społeczność skupiona wokół systemów obliczeniowych wysokiej wydajności postawiła sobie za cel zbudowanie do roku 2020 superkomputerów "skali Exa", to znaczy mających możliwość wykonania $10^{18}$ operacji zmienнопrzecinkowych na sekundę. Jedną z głównych przeszkód stojących na drodze do tego celu jest pobór mocy systemów obliczeniowych przekraczający możliwości dostawy energii. Nowe modele programistyczne i algorytmy uwzględniające to kryterium są jednym z kluczowych pól, na których istotne postępy są konieczne, aby osiągnąć postawiony cel.

Celem rozprawy jest wyodrębnienie ogólnego modelu wykonania hybrydowych aplikacji równoległych w heterogenicznych systemach obliczeniowych wysokiej wydajności będącego syntezą istniejących podejść szczegółowych oraz opracowanie metodologii optymalizacji takiego wykonania aplikacji z uwzględnieniem minimalizacji przeciwnawych kryteriów czasu wykonania aplikacji i poboru mocy wykorzystywanego sprzętu obliczeniowego. Oba znaczenia hybrydowości aplikacji równoległych wiążą się z mnogością parametrów wykonania o nietrywialnych współzależnościami i wpływie na rozpatrywane kryteria optymalizacyjne. Istotny wpływ na owe kryteria ma także sposób mapowania procesów aplikacji na urządzenia obliczeniowe.

Rozprawa składa się ze wstępu, dwóch rozdziałów literaturowych, trzech rozdziałów empirycznych i podsumowania. We wstępie umotywowano podjęcie badań, sformułowano problem badawczy, przedstawiono zakres, główne oryginalne osiągnięcia, tezy oraz przegląd rozdziałów rozprawy. W rozdziale drugim zawarto przegląd istniejących rozwiązań w zakresie wykonania, modelowania i symulacji hybrydowych aplikacji równoległych oraz opisano przykłady takich aplikacji z różnych dziedzin wraz ze znaczeniem ich hybrydowości. W rozdziale trzecim dokonano krytycznej analizy istniejących podejść do optymalizacji aplikacji równoległych z uwzględnieniem czasu wykonania i poboru mocy, ze szczególnym uwzględnieniem metod optymalizacji wielokryterialnej, zarządzania zasobami obliczeniowymi oraz automatycznego strojenia parametrów wykonania aplikacji.

W rozdziale czwartym opisano pięć praktycznych aplikacji równoległych z różnych dziedzin zastosowań oraz pięć różnorodnych systemów obliczeniowych wykorzystywanych w eksperyment-
tach zawartych w rozprawie. W rozdziale piątym zaproponowano metodologię optymalizacji wykonania hybrydowych aplikacji równoległych w heterogenicznych systemach obliczeniowych wysokiej wydajności, składającą się z określonych kroków wykonania oraz metody symulacji do szybkiej ewaluacji punktów w przeszukiwanej przestrzeni rozwiązań. W rozdziale szóstym przedstawiono wyniki eksperymentów polegających na zastosowaniu poszczególnych proponowanych kroków do wybranych rzeczywistych aplikacji oraz zastosowaniu metodologii optymalizacji w całości do aplikacji treningu głębokiej sieci neuronowej do automatycznego rozpoznawania mowy.

Jak wykazano, wykonanie specyficznych w kontekście proponowanego modelu kroków wstępnej optymalizacji procesów, mapowania procesów, strojenia parametrów i właściwego uruchomienia, pozwala na optymalizację czasu wykonania hybrydowych aplikacji równoległych w heterogenicznych systemach obliczeniowych wysokiej wydajności, a proponowana metoda modelowania i symulacji umożliwia szybkie i dokładne wyznaczenie zbioru optymalnych rozwiązań w problemie wielokryterialnej optymalizacji ich wykonania z uwzględnieniem czasu wykonania i poboru mocy.
To my parents Beata and Roman, who gave me
the rare privilege of choosing my own path
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Glossary

**A** - hybrid parallel application,

**$D_S$** - set of computing devices of heterogeneous HPC system $S$,

**$ET (A, S, m, \vec{v})$** - execution time of hybrid parallel application $A$ in heterogeneous HPC system $S$ with process mapping function $m$ and application execution parameters $\vec{v}$,

**$F$** - vector of objective functions of a multi-objective optimization problem,

**$K$** - set of all possible communication operations,

**$L_S$** - set of network links of heterogeneous HPC system $S$,

**$MPC (A, S, m, \vec{v})$** - maximum power consumption of executing hybrid parallel application $A$ in heterogeneous HPC system $S$ with process mapping function $m$ and application execution parameters $\vec{v}$,

**$M_{A,S}$** - feasible set of process mapping functions for hybrid parallel application $A$ and heterogeneous HPC system $S$,

**$PCL$** - power consumption limit,

**$PC (A, S, m, \vec{v})$** - average power consumption of executing hybrid parallel application $A$ in heterogeneous HPC system $S$ with process mapping function $m$ and application execution parameters $\vec{v}$,

**$P$** - set of all possible parallel processes,

**$S (D_S, L_S)$** - graph representing heterogeneous HPC system $S$,

**$V_{A,S}$** - set of application execution parameter vectors feasible for hybrid parallel application $A$ and heterogeneous HPC system $S$,

**$\Phi_A$** - set of process implementations $\{p^1, p^2, ..., p^{\Phi_A}\}$ provided by hybrid parallel application $A$,

**$\Theta$** - set of all possible computation operations,

**$\hat{x}$** - optimum of a single-objective optimization problem,

**$\kappa \in K$** - communication operation,

**$F^*$** - Pareto front,

**$X^*$** - Pareto set,

**$X$** - feasible set of an optimization problem,

**$\theta \in \Theta$** - computation operation,

**$\vec{r}_{\text{max}_A}$** - vector of maximal process requirements of hybrid parallel application $A$,

**$\vec{r}_{\text{min}_A}$** - vector of minimal process requirements of hybrid parallel application $A$,

**$\vec{v}$** - vector of application execution parameters,

**activeoperations** $(d, t)$ - number of operations executed on computing device $d$ at time $t$,

**commtime** $(\kappa, l)$ - execution time of communication operation $\kappa$ using network link $l$,
comptime $\theta(d)$ - execution time of computation operation $\theta$ using computing device $d$,
c $(d, p)$ - number of instances of process $p$ that device $d$ in heterogeneous HPC system $S$ is capable of executing,
d $\in D_S$ - one of the computing devices available in heterogeneous HPC system $S$,
ec $(d, A)$ - total energy consumption (including while idle) of computing device $d$ during the execution of hybrid parallel application $A$,
et $(p, d)$ - execution time of parallel process $p$ on device $d$,
f - objective function of an optimization problem,
l $\in L_S$ - one of the network links available in heterogeneous HPC system $S$,
m $(d, p)$ - process mapping function that determines the number of instances of parallel process $p$ mapped for execution on device $d$,
ncores $(d)$ - number of cores of computing device $d$,
n - number of objectives optimized in a multi-objective optimization problem,
pcidle $(d)$ - idle power consumption of computing device $d$,
pcpeak $(d)$ - peak power consumption of computing device $d$,
$pc(d, t)$ - power consumption of computing device $d$ at time $t$,
$\text{poperation}(d, t)$ - additional power consumption of running an operation on computing device $d$ at time $t$,
p $\in P$ - parallel process, a sequence of operations $(p_1, p_2, ..., p_{|p|})$,
rmax $A_j$ - maximal requirement of hybrid parallel application $A$ for the number of instances of a particular parallel process $p_j$,
rmin $A_j$ - minimal requirement of hybrid parallel application $A$ for the number of instances of a particular parallel process $p_j$,
x - point in the decision space of an optimization problem,

APC - Average Power Consumption matrix,
ASR - Automatic Speech Recognition,
AST - Abstract Syntax Tree source code representation,
CCT - Coflow Completion Time,
CPU - Central Processing Unit,

DaC - Divide and Conquer paradigm,
DAG - Directed Acyclic Graph,
DCFS - Dynamic Core and Frequency Scaling technique,
DIANA - Data Intensive and Network Aware scheduling technique,
DVFS - Dynamic Voltage and Frequency Scaling technique,
ETC - Estimated Times to Compute matrix,

Flop/s - floating operations per second, measure of computer performance,

GDE3 - Generalized Differential Evolution,
GPU - Graphics Processing Unit,

HCS - Heterogeneous Computing System,
HPC - High Performance Computing,

IDW - Inverse Distance Weighting interpolation method,
ILP - Integer Linear Programming,

LAN - Local Area Network,
LSTM - Long Short-Term Memory neural network architecture,

MPI - Message Passing Interface,

PASS - Power Aware Strong Scaling model,
PGAS - Partitioned Global Address Space parallel programming model,
PTF - Periscope Tuning Framework,

SGE - Sun Grid Engine computing cluster software,
SPMD - Single Program, Multiple Data paradigm,

WAN - Wide Area Network,
WER - Word Error Rate metric of automatic speech recognition performance.
1. INTRODUCTION

High Performance Computing (HPC) matters.

It is crucial for modern scientific findings in areas such as genetics, drug discovery, particle physics [1], predictive models for cancer and infectious diseases [2] as well as technological development including video classification, automatic speech recognition, language representation and many others [3]. All these fields require parallel processing. Due to its unique requirements, the deep learning [4] method used in many scientific applications is a good example of such an application, because it requires a combination of three different types of parallelism [2]. First, model parallelism, that is splitting the machine learning model among multiple machines, is an example where parallelism is needed due to the problem size not fitting into the memory of a single machine. Second, data parallelism is needed because large quantities of data are required for the processing. In practice, finishing a contemporary deep neural network training takes days, or even weeks [5]. Discovering optimal results often involves a large-scale search of hyperparameters that requires utilizing the third type of parallelism - executing multiple versions of the same training application to search a space of thousands of model configurations [2]. Execution time of such workloads is critical and for analogous reasons, HPC architectures are essential for many practical applications.

Responding to these needs, because the traditional doubling of computing device clock speeds every 18-24 months is no longer valid, hardware manufacturers replace it by doubling of cores, threads or other parallelism mechanisms [6]. This has allowed to develop supercomputers whose performance is measured in PFlop/s, which means that they are capable of executing a multiple of $10^{15}$ Flop/s (floating operations per second). For example, Sunway TaihuLight, the most powerful supercomputer according to the top500 list for November 2017, has the performance of 93.014 PFlop/s and consists of 10 649 600 cores of Sunway MPP Central Processing Units (CPUs). The HPC community is targeting development of supercomputers able to sustain one ExaFlop/s ($10^{18}$ Flop/s) by the year 2020 [1]. To scale up their floating point throughput, the current generation supercomputers rely heavily on massively-parallel computing accelerators, which makes them heterogeneous in terms of utilized computing devices. For example, Tianhe-2, the second most powerful supercomputer on the aforementioned list has a performance of 33.862 PFlop/s and consists of both Intel Xeon CPUs and Intel Xeon Phi computing accelerators, and the third most powerful, Piz Daint, consists of both Intel Xeon CPUs and NVIDIA Tesla Graphics Processing Units (GPUs).

The primary obstacle to achieving the goal of Exascale computing is power consumption [1]. The upper limit for a reasonable system design adopted by the Exascale Initiative Steer-

\footnote{http://top500.org/}
ing Committee at the US Department of Energy is 20MW, while peak power consumption of the TaihuLight, Tianhe-2 and Piz Daint supercomputers is 15.371, 17.808 and 2.272 MW respectively. This means that over 20x improvement in energy efficiency is required. To achieve the goal of Exascale, architectural improvements, circuit design and manufacturing technologies are required [1], but also software solutions such as system software, programming models, algorithms, frameworks and compilers [7].

Given the multi-level parallelism and heterogeneity of the contemporary HPC systems, their efficient utilization requires developing hybrid parallel programs that have the advantage of exploiting inter-node distributed-memory scalability and intra-node shared-memory performance [8] as well as the ability to run on a heterogeneous infrastructure [9], where certain computing devices can be more efficient for specific parts of the computations. Complexity of such applications brings the requirement for automatic tuning and resource control support to optimize the utilization of resources [7]. One of the key challenges for time- and energy-efficient execution of the applications is to determine optimal values from within a potentially high-dimensional space of configurations [8].

1.1. Motivations

The multiplicity of the possible configurations of hybrid parallel application execution stems from various parameters of the execution and feasible allocations of hardware to individual parts of the application. An example of an execution parameter connected with the utilized hardware is the number of threads executed in parallel. Figure 1.1 presents the influence of this parameter on execution times of a parallel regular expression matching application (see Section 4.1.2) and a geospatial interpolation application (see Section 4.1.3) depending on the number of used threads on two different computing devices. The first device is a GTX 480 GPU belonging to the HPC system described in Section 4.2.1 and the second device is an Intel Xeon Phi 7120P computing accelerator belonging to the HPC system described in Section 4.2.4.

The charts show that the same execution parameter can take completely different values depending on the specific application and utilized computing device - for the GPU the optimal value is in the order of thousands of threads and for the Xeon Phi accelerator, dozens of threads. Efficient execution of a multi-level application running in a heterogeneous HPC system may require individual tuning of the execution parameters for each utilized device. Finding a single optimal value may be also non-trivial due to the presence of local optima.

The multiple parameters of the execution may also originate from the application domain. An example of such parameter is size of packages into which the input data should be partitioned for parallel execution. The application described in Section 4.1.4, given a number of points in a
high-dimensional space, computes similarity measures between the points in parallel by distributing data packets among the available computing devices. The influence of the number of points in such a data packet on the execution time on the HPC system described in Section 4.2.1 for a space of 200 000 dimensions is shown in Figure 1.2.

Fig. 1.2. Influence of data partitioning on the execution time depending on problem size [10]

The chart shows that there is a certain optimal value of this parameter which differ depending on the problem size. In the case of 1000 data points, the best partitioning is to 30 points in data packet, but in the case of 2000 data points it is 50. There can be dozens of such parameters in one application execution and their optimal values may depend on each other. Indication of such parameters for specific applications in various fields and examination of their interdependence and influence on execution time and power consumption of the application is an important research direction. Multiple possibilities of mapping parts of the application to computing devices cause that the space of configurations is even more complex.
Many existing approaches focus on tuning specific execution parameters or solving a specific scheduling problem, with regard to both execution time and power consumption optimization goals, which are often formulated using analytical formulas. Defining a specific formula for execution time and power consumption is often required for each individual application, which is complicated and requires full a priori knowledge about the components of the application and their behavior. In the light of contemporary heterogeneous and multi-level systems there is a need for analysing these approaches, experiments with practical applications from various fields and extraction of a general execution model and optimization methodology that includes all the important aspects and takes into account the opposing objectives of execution time and power consumption.

In many existing approaches, evaluating an execution configuration requires running an actual execution with this configuration. Considering high dimensionality of the configuration space and prohibitively long execution times, there is a need for a method for fast and accurate evaluation of configurations. A modeling and simulation method could be used for this purpose. Research in the field of modeling and simulation of parallel application execution and experiments involving simulation of real applications is needed to verify if a simulation approach can provide fast and accurate estimations of execution time and power consumption and, thus, support optimization of practical applications.

1.2. Problem Formulation

The process optimized within this thesis is execution of a hybrid parallel application in a heterogeneous high performance computing system. The primary components of a hybrid parallel application are computation and communication operations:

Definition 1. Let $\Theta$ denote the set of all possible computation operations, where $\theta \in \Theta$ is a computation operation.

Definition 2. Let $K$ denote the set of all possible communication operations, where $\kappa \in K$ is a communication operation.

A computation operation utilizes a certain computing device in order to perform computations, while a communication operation utilizes a certain network link to perform communication between two processes. Operations are characterized by operation parameters, for example computational complexity of a computation operation or data size for a communication operation.

The operations are executed within processes:

Definition 3. Let $P$ denote a set of all possible processes, where parallel process $p \in P$ is a sequence of computation and communication operations $(p_1, p_2, ..., p_{|P|})$ where $p_i \in \Theta \cup K$.

Parallelism of a hybrid parallel application can be taken into account by the proposed model on two
levels: first, there might be many processes in an application which are executed simultaneously on different hardware. Secondly, the process itself may execute the computations in parallel. For example, an application consisting of of many MPI processes which execute parallel codes on GPUs is parallel at both levels.

A hybrid parallel application consists of one or more process implementations, which define the sequence of operations in each process of the application:

**Definition 4.** Let \( \Phi_A = \{p^1, p^2, ..., p^{\Phi_A}\} \subset P \) denote a set of process implementations provided by a hybrid parallel application \( A \).

A process implementation results from the code of the application, but can be also represented as an arbitrary schedule of operations, computer program or log from a completed application. The operation sequences of two processes may also depend on each other if at some moment of execution there occurs communication between these two processes.

An application has certain process requirements:

**Definition 5.** Let vectors \( \vec{r}_{\text{min}}^A = [r_{\text{min}}^A | \Phi_A], \vec{r}_{\text{max}}^A = [r_{\text{max}}^A | \Phi_A] \) denote process requirements of an application, where \( r_{\text{min}}^A, r_{\text{max}}^A \) are minimal and maximal numbers of instances of process \( p^i \in \Phi_A \) that are required by an application to be executed.

The process requirements may for example depend on the parallel paradigm of the application. For instance, a master/slave application would require exactly one master \( (r_{\text{min}}^A_{\text{master}} = r_{\text{max}}^A_{\text{master}} = 1) \). It would also require at least one slave \( (r_{\text{min}}^A_{\text{slave}} = 1) \) and the maximal number of required slaves could be a value depending on data partitioning limitations or none (infinity).

Summarizing, a hybrid parallel application is defined as follows:

**Definition 6.** Let \( A = (\Phi_A, \vec{r}_{\text{min}}^A, \vec{r}_{\text{max}}^A) \) denote a hybrid parallel application, where \( \Phi_A \subset P \) is a set of process implementations of the application and \( \vec{r}_{\text{min}}^A \) and \( \vec{r}_{\text{max}}^A \) are minimal and maximal process requirements of the application.

It should be noted that a set of independent hybrid parallel applications can be modeled, where processes of each application never communicate with processes of another application. Thus, we can still treat such a set of applications as one hybrid parallel application.

Hybrid parallel applications are executed on heterogeneous HPC systems, also called heterogeneous computing systems (HCS):

**Definition 7.** Let a graph \( S(D_S, L_S) \) denote heterogeneous HPC system, where \( D_S \) is a set of computing devices \( (D_S = \{d_1, d_2, ..., d_{|D_S|}\}) \) and \( L_S \) is a set of network links between computing devices \( (l_{ij} - \text{network link between devices } d_i \text{ and } d_j) \).
The computing devices represented by $d_i$ are hardware devices capable of performing computations. Depending on the considered granularity they might represent computing cores, processing units, computer nodes, groups of nodes, high performance clusters, voluntary computing systems etc. Analogously, a network link can represent a system bus, local area network (LAN), wide area network (WAN) etc. Computing devices and network links are characterized by hardware parameters, for example computational performance of a computing device or bandwidth of a network link. Utilizing hardware with different hardware parameters makes a system heterogeneous.

Each computing device has certain hardware capabilities, which resemble technical possibility to execute certain processes (depending on software stack possibilities, available computing capabilities etc.):

**Definition 8.** Let function $c(d, p) \in \mathbb{N}$ denote hardware capabilities defining how many instances of process $p$ can be executed on device $d$.

Execution of an application depends also on application execution parameters:

**Definition 9.** Let $V_{A,S}$ denote the space of application execution parameters feasible for a hybrid parallel application $A$ and a heterogeneous HPC system $S$.

The space of application execution parameters can potentially be highly dimensional. Multiple examples of execution parameters are described in Chapter 2. The application execution parameters consist of two groups:

- **application parameters** - related to the algorithms used in the application, parallel paradigm, data partitioning, assumed problem constraints, buffer sizes, etc.;
- **execution parameters** - related to possible configurations of the hardware used at multiple parallelization levels, including numbers of threads, thread affinity, GPU grid configurations, DVFS modes etc.

For a specific execution of a hybrid parallel application in a heterogeneous HPC system, specific values of the application execution parameters have to be set:

**Definition 10.** Let $\vec{v} \in V_{A,S}$ denote a vector of application execution parameters of a hybrid parallel application.

Also, the processes have to be mapped to specific computing devices:

**Definition 11.** Let function $m(d, p)$ denote process mapping of a hybrid parallel application to a heterogeneous HPC system, where $m(d, p)$ defines how many instances of process $p$ should be run on a computing device $d$ during a certain application execution.

It should be noted that given a hybrid parallel application $A$ and a heterogeneous HPC system $S$, a feasible process mapping function $m$ belongs to the following feasible set of process
mapping functions $M_{A,S}$:

$$M_{A,S} = \{ m(d, p) | \forall p' \in \Phi_A, \forall d \in D_S (m(d, p') \leq c(d, p')) \land \forall p' \in \Phi_A (r_{min}^A \leq \sum_i m(d_i, p') \leq r_{max}^A) \}.$$ 

The primary outcomes of executing a hybrid parallel application are the results that depend on the purpose of the application. The optimization problem considered in this thesis assumes that these primary results are correct and focuses on the secondary results of the execution, related to execution time and power consumption:

**Definition 12.** Let function $ET(A, S, m, \bar{v})$ denote execution time of a hybrid parallel application $A$ on a heterogeneous HPC system $S$ with process mapping function $m$ and vector of application execution parameters $\bar{v}$. Specifically, the execution time is defined as the time from the start of the application execution (which involves starting all process instances in the application) until finishing of all process instances on the devices assigned by the process mapping function: $ET(A, S, m, \bar{v}) = \max_{p \in \Phi_A} (\max_{d \in D_S} m(d, p))$ where $m(d, p)$ is execution time of a parallel process $p$ on device $d$.

**Definition 13.** Let function $PC(A, S, m, \bar{v})$ denote average power consumption of all computing devices of a heterogeneous HPC system $S$ during the execution a hybrid parallel application $A$ with process mapping function $m$ and vector of application execution parameters $\bar{v}$. Specifically, the average power consumption is defined as the total energy consumption (including while idle) of all computing devices in the system throughout the application execution divided by the execution time: $PC(A, S, m, \bar{v}) = \frac{\sum_{d \in D_S} ec(d, A)}{ET(A, S, m, \bar{v})}$ where $ec(d, A)$ is the total energy consumption of a computing device $d$ during the execution of a hybrid parallel application $A$.

**Definition 14.** Let function $MPC(A, S, m, \bar{v})$ denote maximum power consumption of all computing devices of a heterogeneous HPC system $S$ during the execution a hybrid parallel application $A$ with process mapping function $m$ and vector of application execution parameters $\bar{v}$: $MPC(A, S, m, \bar{v}) = \max_{t} \sum_{d \in D_S} pc(d, t)$ where $pc(d, t)$ is the power consumption of a computing device $d$ at time $t$.

The following multi-objective optimization problem, is solved within this thesis, with the objective space consisting of execution time $ET$ and average power consumption $PC$. Given a hybrid parallel application $A$ and a heterogeneous high performance computing system $S$:

$$\min_{m, \bar{v}} F(A, S, m, \bar{v}) = [ET(A, S, m, \bar{v}), PC(A, S, m, \bar{v})]$$

subject to $m \in M_{A,S}$,

$\bar{v} \in V_{A,S}$. 

(1.1)
Pareto method is used for multi-objective optimization where the expected solution to the optimization problem is a set of Pareto-optimal points from the search space. The search space consists of the feasible set of process mapping functions $M_{A,S}$ and the space of feasible application execution parameters $V_{A,S}$. A point is Pareto-optimal if every other point in the search space results in higher execution time or higher average power consumption than this point. The Pareto method is described in more detail in Section 3.1.1.

In this thesis we assume that the HPC system $S$ is given and cannot be modified, although optimization that considers introducing new, currently unavailable hardware to the system can be considered as future work. Changes to the processes $p \in \Phi_A$ of the application $A$ are possible, but limited. The computational goals of the application have to be maintained, so the optimization of the processes can be only performed manually by a specialist. Such optimizations are included in the execution steps proposed in this thesis as an optional first step of preliminary process optimization, after which the application $A$ cannot be modified. The remaining parameters of the execution can be optimized automatically and define the search space of the considered process mapping and parameter tuning problem.

The following related problems are also considered in the thesis:

- Optimization of execution time under power consumption constraints - given a hybrid parallel application $A$, heterogeneous high performance computing system $S$ and power consumption limit $PCL$:

$$\min_{m,\vec{v}} \text{ET}(A, S, m, \vec{v})$$
subject to

$$m \in M_{A,S},$$
$$\vec{v} \in V_{A,S},$$
$$\text{MPC}(A, S, m, \vec{v}) \leq PCL.$$  \hfill (1.2)

- Optimization of execution time - given a hybrid parallel application $A$ and heterogeneous high performance computing system $S$:

$$\min_{m,\vec{v}} \text{ET}(A, S, m, \vec{v})$$
subject to

$$m \in M_{A,S},$$
$$\vec{v} \in V_{A,S}.$$ \hfill (1.3)

The model of hybrid parallel application execution in a heterogeneous HPC system proposed in this Section is referenced by Claim 1 of this dissertation.
1.3. **Scope of the Dissertation**

The work described in this thesis is related to six main areas:

- specific **hybrid parallel applications** and their implementations;
- solutions for executing **hybrid parallel applications in heterogeneous HPC systems**;
- modeling and simulation of parallel applications in **heterogeneous HPC systems**;
- multi-objective optimization of parallel applications;
- energy-aware resource management in **heterogeneous HPC systems**;
- parameter auto-tuning in parallel applications.

Figure 1.3 presents to what extent the contributed papers related to this thesis are relevant to each of these main areas.

In the area of specific **hybrid parallel applications**, the scope of this thesis includes an overview of existing applications in Section 2.1.2 and the applications described in Section 4.1, used in the experiments. In the most application-oriented paper [11] we proposed a regular expression matching application with configurable data intensity for testing **heterogeneous HPC systems**. Certain descriptions and analyses of the corresponding considered applications have also been provided in papers [10, 12, 13, 14, 15, 16].

Chosen existing approaches to executing parallel applications in **heterogeneous HPC systems** have been described in Section 2.2. The framework for multi-level high performance computing using clusters and workstations with CPUs and GPUs introduced in [13] is proposed in this thesis as a software solution for executing the proposed optimization methodology. Execution of a parallel deep neural network training application on a cluster with multiple GPUs is described in [15]. An approach to using distributed databases for data management in **heterogeneous HPC systems**...
systems is proposed in [17]. Certain aspects regarding execution of the considered applications have been also discussed in papers [11, 18, 19, 20].

An important contribution of this thesis is the method for modeling and simulation of hybrid parallel application execution on heterogeneous HPC systems described in Section 5.2. Section 2.3 provides an overview of existing approaches to simulation and modeling in this field. In [21] we discussed the existing simulation systems and provided motivations for a new discrete-event simulation environment introduced in [14]. An example of execution time modeling using this environment has been described in [10], and an example of modeling energy consumption in [12]. In [16] we proposed an approach, described also in Section 6.2.2, to exploring power/time trade-off of a deep neural network training application using this simulation environment. Additionally, simulation has been used in the approach to optimization of execution time under power consumption constraints proposed in [19] and described in Section 6.1.2 to determine optimal data partitioning. In [20], a method of configuring process labels in the system model has been proposed that simplifies executing simulations with fine-grained granularity.

The problem solved within this thesis, defined in Section 1.2, is a multi-objective optimization problem. In Section 3.1 we discuss approaches to multi-objective optimization of parallel applications and choose the Pareto method for the approach proposed in this thesis. In [19] we focused on the problem of execution time optimization under power consumption constraints defined in Equation 1.2. Pareto method has been used for exploring the power/time trade-off of a parallel deep neural network training application described in [16] and in Section 6.2.2.

The task mapping aspect of the optimization problem solved within this thesis, connected with finding the optimal process mapping function \( m \) lies in the field of resource management. The approach proposed in this thesis is compared to chosen approaches to energy-aware resource management in heterogeneous HPC systems in Section 3.2. The task mapping problem has been considered in the context of optimization of execution time under power consumption constraints in [19]. Resource management has been also considered in [17] in the context of network-aware scheduling and in [18] in the context of computing system monitoring. Finding the optimal number of used computing devices in [16] is also connected with resource management.

The aspect of the considered optimization problem connected with finding the optimal set of application execution variables \( \vec{v} \) lies in the field of parameter auto-tuning. Chosen approaches to parameter auto-tuning in parallel applications are described in Section 3.3. Auto-tuning of execution variables such as thread numbers, GPU grid configurations and data partitioning is an important part of the optimization methodology proposed in [13] and the generalized version in Chapter 5. Data partitioning has been also tuned in [19] and [10]. In [16] the tuned variable is connected with resource mapping, namely the number of devices used for computations.
The problem solved in this thesis combines the following problems from the fields of multi-objective optimization, resource management and parameter auto-tuning:

- multi-objective optimization of execution time and power consumption problem;
- suboptimal-approximate energy-aware global static task mapping problem;
- offline auto-tuning of system parameters problem

into one bi-objective Pareto optimization problem of execution time and power consumption.

1.4. Main Contributions of the Dissertation

This work contains the following original contributions made by the author:

- proposition of a new model of hybrid parallel application execution in heterogeneous HPC systems described in Section 1.2 that focuses on execution time and power consumption of processes consisting of computation and communication operations and considers process mapping and application execution parameters;
- implementations connected with specific hybrid parallel applications, namely: heterogeneous OpenCL implementation of the regular expression matching application described in Section 4.1.2; multi-level heterogeneous OpenCL + MPI implementation of the application described in Section 4.1.3 and integration of the application with the KernelHive framework (this air pollution interpolation application was used in the SmartCity system developed for the local government of the city of Gdańsk, Poland); implementation of the model of the large vector similarity measure computation application described in Section 4.1.4 in the MERPSYS environment; extension of the existing deep neural network training application described in Section 4.1.5 by MPI message passing for multi-level execution and implementation of the model of this application in the MERPSYS environment (the application was used for acoustic model development by VoiceLab.ai, a company based in Gdańsk, Poland);
- proposition of specific execution steps for hybrid parallel applications in heterogeneous HPC systems described in Section 5.1 consisting of preliminary process optimization, process mapping, parameter tuning and actual execution, and implementation of these steps in the KernelHive framework;
- co-design of the simulation method of hybrid parallel application execution in heterogeneous HPC systems described in Section 5.2 and proposition of using this method for fast evaluation of process mappings and application execution parameter values in the multi-objective execution time and power consumption optimization. Co-implementation of this method within the MERPSYS simulation environment. Specifically, implementation of the scheduler mechanism, framework for executing multiple parallel simulations,
power consumption computation and multiple improvements of the simulator;

- demonstration of the proposed execution steps on the example of multi-level task farming applications described in Section 6.1 including computation and communication overlapping, network-aware and power constrained scheduling, tuning of grid configurations and data partitioning and execution in heterogeneous HPC systems with CPUs and GPUs using the KernelHive framework;

- demonstration of the proposed optimization methodology as a whole including the execution steps and simulation method on the example of a deep neural network training application described in Section 6.2 including overlapping of training and data preprocessing, power-aware device selection and execution on a professional cluster of workstations with GPUs using the contributed multi-level implementation;

1.5. Claims of the Dissertation

1. The execution steps specific in the context of the proposed model, including preliminary process optimization, process mapping, parameter tuning and actual execution allow to optimize execution time of hybrid parallel applications in heterogeneous high performance computing systems. Empirical proofs for this claim are provided in Chapter 6. Specifically, proofs related to preliminary process optimization are presented in Sections 6.1.1 and 6.2.1, process mapping in Sections 6.1.2 and 6.2.2, parameter tuning in Sections 6.1.3 and 6.2.2, and actual execution in Sections 6.1.4 and 6.2.3.

2. The proposed modeling and simulation method allows for fast and accurate identification of the set of Pareto-optimal solutions to the problem of multi-objective execution time and power consumption optimization of hybrid parallel applications in heterogeneous high performance computing systems. Empirical proofs for this claim are provided in Section 6.2.2.

1.6. Overview of the Dissertation

The remainder of this thesis is organized as follows. A state of the art review is provided in Chapters 2 and 3. Chapter 2 discusses hybrid parallel applications, examples of applications from various fields, software solutions for executing them in heterogeneous HPC systems and approaches to modeling and simulation of their execution. Chapter 3 covers approaches to optimization of parallel application execution in the contexts of multi-objective execution time and power consumption optimization, energy-aware resource management and parameter auto-tuning.

In Chapter 4 specific applications and systems are described, that have been used in the
experiments within the thesis. The main contribution of this thesis is the optimization methodology proposed in Chapter 5. An empirical evaluation of the methodology, described in Chapter 6, is based on case studies involving optimization of specific executions of hybrid parallel applications in heterogeneous HPC systems. Finally, conclusions and discussion about the possible future work are provided in Chapter 7.
2. EXECUTION, MODELING AND SIMULATION OF HYBRID PARALLEL APPLICATIONS

In Section 2.1 we provide examples of hybrid parallel applications and describe the systems, APIs and frameworks used by these applications as heterogeneous HPC systems in Section 2.2. An important part of the optimization methodology proposed in this thesis is a method for modeling applications and systems and simulating application execution. In Section 2.3 we provide an overview of existing approaches to modeling parallel applications and systems, as well as simulating the execution.

2.1. Hybrid Parallel Applications

We characterize the common denominator shared by parallel applications which could benefit from the methodology proposed in this thesis by naming them hybrid parallel applications. In Section 2.1.1 we explain our interpretation of the term hybrid in the context of parallel applications by comparing it to existing works. In Section 2.1.2 we provide examples of specific applications in the fields similar to the applications considered in our experiments. Possible application parameters are emphasized.

2.1.1. Hybridity of the Applications

The term hybrid in the context of parallel applications appears in two main meanings. First, mixing different types of computing devices [22, 23, 24, 25], for example CPU + GPU. Second, mixing programming APIs on different parallelism levels [26, 27, 28], for example MPI + OpenMP. In both cases the aim is utilizing more computing devices in order to achieve better performance or performance/power consumption ratio. The first meaning implies the heterogeneity of the utilized HPC system, and the second meaning implies that the system is multi-level. It is worth noting that, in essence, both these meanings are related to the properties of the HPC system, namely that it is heterogeneous and multi-level. Examples of such systems are discussed in Section 2.2.3.

Having said that, the term hybrid may seem redundant in the context of parallel applications themselves. However, we decided to emphasize this word due to another meaning. A crucial factor of the model of parallel application execution proposed in this thesis is the set of parameters which influence its execution. In a heterogeneous multi-level system these parameters may include various aspects of execution, often related to certain types of computing devices or parallelization levels. The term hybrid is gaining importance in the cases where changing one of these application parameters influences the optimal value of another.

For example, the term hybrid has been used in the context of a hybrid Xeon/Xeon Phi
system in [24]. Within the paper, a parallel application for computing similarity measures between large vectors is optimized for scalability in a system consisting of Intel Xeon CPUs along with Intel Xeon Phi coprocessors. Proposed optimizations include load balancing, loop tiling, overlapping and thread affinity setting. The system is hybrid in the sense of utilizing different types of computing devices, which makes it a heterogeneous computing system. What is more significant, executing computations on the Intel Xeon Phi influences the optimal number of cores used on the host processor for computations: one core should be left free, so it can be efficiently used for handling the accelerator.

Situations when the optimal values of execution parameters depend on each other often occur in practical approaches. In the above example, changing one execution parameter (whether or not to use the coprocessor) influences the optimal value of another execution parameter (number of used cores of the host processor used for the computations). Such relationships concern also application-specific parameters. For instance, when the authors of [29] fixed one of three application parameters of a GS2 physics application and plotted the performance as a function of two other application parameters, it turned out that the optimization surface was not smooth and contained multiple local minima.

The mutually dependent parameters include also meta-parameters resulting from code optimizations. One example would be an approach to optimizing parallel application execution using a combination of compiler and runtime techniques proposed in [30]. In this approach, regions of the tuned applications are subject to source-to-source transformations. Parameters of these transformations belong to the set of tuned variables. The authors observe that optimal transformation parameter values or even distinct transformation sequences depend on another execution parameter, namely the number of threads. This observation is a motivation for multi-versioning approach proposed in the paper, where a set of optimal solutions is encoded by the compiler into one executable and the runtime system dynamically chooses between the versions depending on changing circumstances and objectives.

Another example is simultaneous loop tiling and unrolling program transformations for minimizing execution time of selected numeric benchmarks in [31]. The authors claim that combining the best tiling transformation with the best unrolling factor does not necessarily give the best overall transformation. What is more, it is shown that small deviations from optimal tile sizes and unroll factors can cause such an increase in execution time, so that it is even higher than in the original program. Previously used static cost models which attempt to give an analytical expression for the execution time were vulnerable to such varying optimization spaces. Instead, an approach called iterative compilation is proposed, where many versions of the program are generated and executed for determining optimal values of the optimization parameters.
Although the two latter approaches concern programs that are neither multi-level nor executed on a heterogeneous platform, they illustrate non-trivial dependencies between application execution parameters, which cause a need for specific optimization algorithms. In contemporary multi-level HPC applications executed in heterogeneous HPC systems, dependencies of this type are increasingly likely, and it is getting harder and harder to describe them using analytical models.

Summarizing, in the sense of this work, a parallel application is hybrid if it is multi-level or executed in a heterogeneous HPC system, but more importantly when there are non-trivial dependencies between the application execution parameters and the optimization objectives, such as execution time and power consumption. This deeper meaning of the term hybrid is essential in the model and optimization approach proposed in this thesis, because it means that instead of finding optimal parameter values separately, in many cases there is a need to take into account the whole space of decision parameters.

2.1.2. Examples of Hybrid Parallel Applications in Selected Fields

In order to provide examples of what the discussed class of applications can be useful for, in this section we describe chosen applications from fields similar those developed and used in the experiments within this thesis, described in Chapter 4.1.

The sample application described in Section 4.1.1 is distributed MD5 hash breaking using a cluster with CPUs and GPUs. A similar approach to distributed password cracking has been proposed in [32], where a cluster of up to 88 GPUs has been used for password recovery through brute-force attack, achieving good scalability thanks to the proposed efficient password distribution scheme. The solution is hybrid in the multi-level sense, but the computing system is homogeneous (CPUs are not used for computations). In the field of cryptography, parallel applications that are hybrid in the sense of device heterogeneity are also used. For example in [33], a cluster system integrating CPU and GPU devices from various vendors is used for efficient encryption and decryption of large amounts of data. Application parameters in password cracking may be related to the method of dividing workload across the used workers, namely the number of passwords to be checked by each worker in an iteration and expected minimum/maximum password length which influence the average time of recovering the password.

The regular expression matching application described in Section 4.1.2 belongs to the field of text pattern matching. Pattern matching algorithms are widely used in signature-based network intrusion detection systems (NIDS) [34]. The objective of such systems is to examine if incoming network packet payloads contain malicious content defined as "signatures" or "patterns" and generate alert messages for system administrators. Examples of application parameters in this problem are maximum length of a signature and size of slices into which the traffic is parti-
tioned. Hybrid CPU/GPU pattern matching for deep packet inspection has been proposed in [25], where the incoming packets are pre-filtered using CPU and suspicious packets are sent to the GPU for complete matching. The GPU workload is reduced thanks to the CPU pre-filtering stage.

Geostatistical interpolation applications are a fundamental task in geographic information science and are used for prediction of environmental phenomena at non-observed locations. Computational cost of the used algorithms grows with the number of data points from the observed locations and the number of locations for which the interpolated values are needed. The contemporary interpolation workloads are critical, for example in weather forecast systems, and efficient implementations of geostatistical interpolation algorithms are needed. The same algorithm that the one described in Section 4.1.3 has been adapted to massively parallel computing environments in [35] and [36]. An efficient GPU implementation of another popular geostatistical interpolation method called kriging has been proposed in [37]. An exemplary application parameter in the geostatistical interpolation problem could be related to the used strategy of data point partitioning. For example, quad trees have been used in the approach to another geoscientific problem: constructing digital elevation models from high resolution point clouds acquired using LIDAR technology [27]. A hybrid MPI/GPU implementation for solving this problem has been proposed. The application is hybrid in the multi-level sense, with multiple GPU-equipped hosts independently interpolating a portion of data and assembling the final model from partial results with balancing of I/O, computation and communication in mind.

The application described in Section 4.1.4 concerns large-vector similarity measure computation. This task is a crucial part of clustering which means grouping a set of objects into classes of similar objects. Algorithms using pattern similarity have been successfully applied to large data sets in DNA microarray analysis, e-commerce applications, such as collaborative filtering [38] as well as real-time searching for similar short messages for the purposes of a social networking service with a dataset of over billion messages [39]. Faiss [28] is a recent open-source library for efficient similarity search and clustering of dense vectors. A key problem addressed by this approach is to, given a large database of objects, construct a k-NN graph - a directed graph whose nodes represent objects from the database and edges connect them to k nearest neighbors, according to one of the supported distance functions. The solution is capable of using multiple GPUs on one server for constructing a high accuracy k-NN graph. For example, construction of a graph connecting 1 billion vectors in less than 12 hours on 4 NVIDIA Maxwell Titan X GPUs has been reported. The presented application of the library is constructing a k-NN graph for a database of 95 million images and finding a path in this graph, resulting in a sequence of smooth transitions from a given first to a given last image. Application parameters of the large-vector similarity measure computation problem include the maximum dimensionality of an object and size of packages.
in which the objects are transferred to the computing devices.

Finally, there are multiple applications of parallel deep neural network training, the field of the application described in Section 4.1.5. Many of them are hybrid in the multi-level sense, because often multiple computing devices are used for training. For example, a neural network for classifying positions in the Go game according to archival expert moves was trained using asynchronous stochastic gradient descent on 50 GPUs in [40]. The training took around three weeks, because 340 million training steps were needed to contribute to the achievement of winning 99.8% games against other Go programs and defeating the human European Go champion by 5 games to 0. There have also been hybrid CPU/GPU approaches to deep neural network training. A version of the popular deep learning framework Caffe proposed in [41] allows using both CPUs and GPUs for training a deep neural network, which on a single convolutional layer achieves 20% higher throughput than only on a GPU. A hybrid CPU/GPU implementation [42] has been also proposed for A3C, a parallel method for reinforcement learning, which can for example learn to successfully play an Atari game only from raw screen inputs. The proposed hybrid implementation generates and consumes training data for large deep neural networks up to 45 times faster than its CPU counterpart. An application parameter in the field of parallel deep neural network training can for example be the frequency of model synchronization between many training workers.
2.2. Executing Parallel Applications in Heterogeneous HPC Systems

Depending on the hardware utilized by a parallel application, various software solutions are used for its execution. In this section we describe selected tools, frameworks and APIs used for executing parallel applications. We put particular emphasis on related execution parameters, which may belong to a set of decision variables in the optimization problem solved in this thesis. Section 2.2.1 is devoted to systems, where multiple threads can run in parallel and communicate and synchronize through shared memory. Distributed memory systems, where each process has its own private memory and some form of interconnection is needed for communication are described in Section 2.2.2. Finally, Section 2.2.3 focuses on systems that allow executing applications that are hybrid in two meanings described in Section 2.1.1 – with multiple levels of parallelization and with heterogeneous computing devices.

2.2.1. Shared memory systems

From the viewpoint of a parallel application programmer, a program running in a shared memory system typically consists of one or more threads - sequences of programmed instructions, which are executed concurrently. POSIX threads \[43\] is a popular parallel execution model that defines C-language functions for thread management and synchronization, which implementations are available for many operating systems. Analogous mechanisms are available for many popular programming languages, for example threading library in Python, Java threads \[44\] etc. If the utilized runtime supports it, some of the concurrent threads may be executed in parallel, resulting in reduction of application execution time.

Parallel applications that utilize the threading execution model are very often executed on CPUs with multiple cores (multi-core). An evident execution parameter of such applications is the number of used threads. The optimal number of threads should allow to efficiently utilize available CPU cores, which does not necessarily mean that the optimal number is equal to the number of CPU cores. The capacity of utilizing many cores in parallel depends on the algorithms used by the application. Additionally, modern CPUs support hardware multithreading techniques such as simultaneous multithreading (SMT), which allow multiple threads to be executed simultaneously on one core. Although the threads are completely separated from each other, running them on one core influences the computation performance. Apart from the proper number of used threads, in such non-uniform computing architectures, efficient utilization of the multi-core computing devices requires taking into account how the application threads are mapped to the available cores. This can be achieved by configuring thread affinity, which allows binding and unbinding certain threads to certain CPU cores and is another example of a parallel application execution parameter.

Modern high performance computing accelerators are equipped with dozens of physical
computing cores. For example, the *Knights Landing* architecture used by the second generation of Intel MIC accelerators is built from up to 72 cores with possibility to run four threads per core. Shared-memory multiprocessing APIs such as OpenMP are often used to develop parallel programs for such multi-core architectures. Multithreading can be achieved using OpenMP by extending sequential C/C++ and Fortran codes with compiler directives that take care of thread creation, data sharing, synchronization, scheduling etc. For example, a C/OpenMP implementation of a parallel large vector similarity measure computation application was used in [24] to test various thread affinities, but also allocating memory in large pages for improved data transfer rate. The latter is an example of an *execution parameter* specific for the used device - in this case the Intel Xeon Phi coprocessor.

Arguably, the most popular computing accelerators recently are GPUs (graphics processing units). They consist of several streaming multiprocessors, which in turn consist of multiple processing elements known as CUDA cores. The name is connected with the CUDA parallel computing platform and API created by NVIDIA. In this execution model, the code written in a form of a *kernel* is executed by multiple threads at once. For example, the NVIDIA Tesla V100 data center GPU is equipped with 5120 CUDA cores and allows to run 163840 threads simultaneously. The threads are logically aligned in a hierarchy called *grid* that consists of a number of *blocks* constructed from a number of threads. Numbers of blocks in a grid and threads in a block can be arranged by the programmer in up to three dimensions. This setting is called *grid configuration* and its optimal values may depend on the GPU device model, but also on the application, its computation to communication ratio, code branches etc. Finding the optimal values often requires tuning through testing the application performance for multiple combinations of the grid size parameters. The GPU grid configuration is another example of a parallel application *execution parameter*.

A similar hierarchical application structure can be found in OpenCL framework [45], which allows to write programs that can be executed across heterogeneous platforms, including GPUs. Here, the equivalent of *grid* is called *NDRange*, consists of *work groups*, which in turn consist of *work items*. The actual mapping of this structure to the computing *device* architecture depends on the chosen *installable client driver* (ICD). Multiple OpenCL implementations offered by different vendors support various computing devices. Different *NDRange* configurations can be optimal depending on the OpenCL implementation and the utilized computing device, which makes the selection of appropriate *execution parameters* even harder if the code is executed in a heterogeneous system.

Heterogeneous systems can be also programmed using OpenACC, a programming standard aimed for simplification of programming of CPU/GPU systems. Similarly to OpenMP, C/C++
and Fortran codes can be annotated using compiler directives responsible for parallelization, with a particular emphasis on parallelizing loops. The API defines also runtime functions responsible for device and memory management. An important aspect of programming with OpenACC is optimizing data locality by providing the compiler with additional information about the data location. This allows to reuse data on the same device and minimize data transfer, which can be particularly beneficial on systems where used devices have separate memories. Selecting the appropriate strategies of data creation, copying and address management is another example of a parallel application execution parameter.

An execution parameter crucial in terms of power efficiency is setting the "gear" of a computing device using the Dynamic Voltage and Frequency Scaling (DVFS) technique. Often the most efficient setting in terms of compute capacity is not the most power efficient, because modern computing devices often have asymmetric power characteristics. For example Volta, the latest NVIDIA GPU architecture at the time of this writing, is claimed by its vendor to achieve up to 80% of the peak performance at half the power consumption. Performance vs energy trade-offs can be found on both modern CPUs and GPUs [46]. The effects of scaling core voltage and frequency depend not only on the computing device architecture, but also on the application characteristics [47], which makes finding the optimal setting non-trivial.

Summarizing, the optimal values of execution parameters of parallel applications executed in shared memory systems are hard to find, because they often depend on each other, on algorithms used in the application, its input/output characteristics as well as utilized hardware. Finding the appropriate value often comes down to empirical verification and tuning.

2.2.2. Distributed memory systems

Computing systems in which each computing device has its own private memory are called distributed memory systems. Programming applications for such systems requires taking care of not only process synchronization, but also data transmission between the processes. Message Passing Interface (MPI) [48] is the de facto standard communication protocol for point-to-point and collective communication, with several well-tested and efficient implementations. The MPI interface provides the essential virtual topology, synchronization and communication functionality between a set of processes. In order to achieve the best possible performance of an MPI-based application, certain runtime parameters of the used MPI implementation should be optimized for the target platform, including the cross-over point for point-to-point operations between the eager and the rendezvous protocol, network specific values such as internal buffer sizes and algorithms to be used for collective operations. OpenMPI, a popular MPI implementation has been equipped with the Open Tool for Parameter Optimization (OTPO) [49] which systematically
tests large numbers of combinations of OpenMPI runtime tunable parameters to determine the best set for the given platform, based on selected benchmarks.

Message passing interfaces such as MPI allow to implement applications employing many well known parallel processing paradigms [50]. The task-farming paradigm, also known as master/slave consists of two kinds of processes. The first one, master, is responsible for decomposing the problem into small tasks and iteratively distributing them across a farm of processes of the second kind, called slaves. The slave processes perform a simple cycle: get a message with the task, process the task, send the results back to the master. Paradigm-related application parameters in this case include the number of slaves used at each iteration, task allocation and load balancing strategies as well as granularity of problem decomposition which may influence message sizes.

In the Single-Program Multiple-Data (SPMD) paradigm, data required by the application is split among available processors and each process executes the same code on a different part of the data. This paradigm is especially useful for problems with a geometric structure, where communication between the processes is spatially limited, for example physical problems and simulations. Efficient execution of SPMD programs in multi-core environments often requires managing communication heterogeneities that cause unbalanced workload. For example, the methodology evaluated on a MPI SPMD application in [51] allowed for 43% efficiency improvement through scheduling policies that allow to determine the number of tasks to be assigned to each core, which allows computation and edge communication overlapping and optimal load balancing. The number of tasks per each core is another example of an application parameter.

Another, more fine-grained paradigm which also reflects data dependencies of the application is data pipelining. Functional decomposition of the application allows to organize a pipeline of processes, each corresponding to a given stage of the algorithm. The efficiency of this paradigm depends on the capability of balancing the load across the stages of the pipeline. Efficient implementation of such pipelines becomes even more challenging in the case of real-time or near-real-time systems with small messages, due to the trade-off between the system throughput and latency. Processing the messages directly as they occur results in very frequent, small communication operations which significantly limit the throughput. Batching techniques can be used to improve the throughput at the cost of the latency. For example, incurring a small latency to group small messages together allows improving throughput in Kafka [52], a real-time publish-subscribe system that can handle more than 10 billion message writes each day. The incurred latency value can be tuned at the application level and is another example of an application parameter which optimal value may depend on the characteristics of the target system.

Divide and Conquer (DaC) is a well known approach in algorithm development which can be also used as a parallel processing paradigm. In this approach a problem is decomposed
into subproblems which can be solved independently and their results are combined to give the final result. The problems can be decomposed recursively, which results in an execution tree that defines a hierarchy of split, compute and join computational operations. Given appropriate complexity proportions between the splitting and joining operations compared to the computing operations, performance of the DaC approach can benefit from parallel execution. For example, a multi-threaded framework based on OpenMP proposed in [53] allowed to obtain speed-ups around 90 for an irregular adaptive integration code executed on an Intel Xeon Phi accelerator. The framework allows developing parallel DaC applications by coding only basic DaC constructs such as data partitioning, computations and result integration, while parallelization is handled by the contributed runtime layer. The degree of parallelism can be controlled by setting two application parameters: k_max which specifies the maximum depth of the execution tree and max_thread_count which is the total number of threads that can be run at any given time.

Frameworks for automatic parallelization of computations are very much needed, for instance in the field of big data processing. For example MapReduce [54] is a programming model similar to Divide and Conquer where the programmer specifies two functions: map and reduce. Given a single key/value pair, the map function generates a set of intermediate key/value pairs. Intermediate values with the same key are merged by the reduce function. This simple model allows to express many real world tasks, especially in the field of big data processing. Due to the availability of tools for automatic parallelization of programs written in the MapReduce paradigm such as Hadoop [55], programmers can relatively easily utilize the resources of a large distributed system without any experience in parallel computing. Although input data partitioning, scheduling, failure and communication management are handled by the runtime system, certain optional execution parameters can be tuned, including maximum number of used machines and memory limits for each map and reduce task.

One limitation of the DaC-based computing paradigms is that they support only acyclic data flow, while in many practical applications a working set of data needs to be reused across multiple parallel operations. Spark [56] is an example of a popular framework that supports these applications by introducing data abstraction called resilient distributed datasets - read-only collections of objects partitioned across a set of machines. An operation invoked on such a dataset results in creating a task to process each partition of the dataset and sending these tasks to preferred worker nodes using a technique called delay scheduling [57]: when the job that should be scheduled next according to fairness cannot launch a local task, it waits for a small amount of time, letting other jobs launch tasks instead. This allows for significant performance improvements for chosen applications, especially those with iterative and interactive computations. Certain execution parameters can be tuned in Spark, including job scheduling policies, data serialization,
memory management policies, data locality and level of parallelism.

2.2.3. Multi-level and Heterogeneous Systems

In paper [58] hybrid parallel programming has been narrowed down to combining distributed memory parallelization on a node inter-connect with shared memory parallelization inside of each node. The presented experiments included results from executions of applications written using message passing (namely MPI) on the distributed memory level and directive-based parallelization (OpenMP) on the shared memory level. Various schemes of MPI + OpenMP programming models have been discussed and compared based on benchmarks executed on several computing platforms. The paper underlines the importance of the communication and computation overlapping optimization technique. In our work this method falls into the preliminary process optimization step, one of the execution steps proposed in Section 5.1 and was used in the experiments described in Section 6.1.2.

Authors of [59] argue that although using MPI for internode communication and another shared-memory programming model for managing intranode parallelism has become the dominant approach for utilizing multi-level systems, the significant downside of this approach is complexity of using two APIs in the same application. They propose a shared-memory programming model which is incorporated into MPI as an extension to its communication interface. The implementation allows to automatically adjust the shared-memory mapping, which for several provided use-cases resulted in improved performance.

Utilization of large-scale multi-level computing architectures using a single API is possible in the partitioned global address space (PGAS) [60] parallel programming model. In this model, a number of parallel processes jointly execute an algorithm by communicating with each other via a single shared memory address space. The memory is conceptually shared (technically realized by several interconnected memories), which aims to improve programmer productivity. At the same time, the PGAS model provides additional abstractions to distinguish between local and remote data accesses, in order to allow implementations aiming for high performance. About a dozen languages exists that adhere to the PGAS model [60]. For example, Java programs can use the PCJ library [61] that has the ability to work on multi-node multi-core systems and hiding the details of inter- and intra-node communication. Experiments involving running a set of HPC applications show good performance scalability of the PCJ library compared to native implementations of the same algorithms in C++ with MPI and Java 8 with parallel streams mechanism, while maintaining the usability typical for the PGAS model implementations.

Many solutions for executing applications utilizing a single parallelization API on multi-level computing systems are also aimed at utilizing heterogeneous devices [62, 63, 64, 65, 66, 67]. For
example Many GPUs Package (MGP)[62] provides C++ and OpenMP APIs that allow to extend existing applications executed on one hosting-node, so that they can transparently utilize cluster-wide devices. What is more, the package includes also an implementation of OpenCL specifications that allows executing OpenCL code on a cluster with many CPU and/or GPU devices without any modifications of the code. This reduces the complexity of programming and running parallel applications on cluster, especially since MGP provides an API for scatter-gather computations and takes care of dependencies between the split sub-tasks, queuing and scheduling them as well as managing buffers.

Frameworks for multi-level parallel computing on heterogeneous systems are also developed with specific type of application in mind. For example, TensorFlow [3] is an interface for expressing machine learning algorithms and an implementation for their execution. TensorFlow applications are constructed from operations which constitute a dataflow graph, where each node has zero or more inputs and zero or more outputs. Many implementations can be provided for each operation that can be run on a particular type of device. This way, various device types can be used by one application in order to efficiently utilize a heterogeneous system. Various kinds of parallelism can be expressed through replication and parallelization of the graph, including model parallelism and data parallelism. Additionally, an operation implementation can be parallel itself, using for example the parallel capabilities of a GPU, which means that TensorFlow applications can be multi-level.

There are solutions for executing parallel applications in hybrid multi-level systems that take into account energy efficiency. For example the authors of [68] argue that high-end GPU-based accelerators feature a considerable energy consumption, so a solution is needed that would enable each node in a cluster to run efficient computations on a GPU while avoiding attaching a GPU to every node of the cluster. The proposed rCUDA framework for remote GPU acceleration allows this, introducing only a small overhead for chosen sample applications from CUDA SDK.

Energy efficiency has been considered also in the context of hybrid CPU/GPU architectures in [9] where GreenGPU, a framework for GPU/CPU heterogeneous architectures was proposed. The solution provides load balancing between CPU and GPU by dynamic splitting and distributing workloads based on its characteristics, so that idle energy consumption is minimized. Additionally, GPU core and memory frequency as well as CPU frequency and voltage are dynamically throttled based on their utilization. The holistic approach that includes workload division and frequency scaling achieves an average energy saving of 21.04% and only 1.7% longer execution for the kmeans and hotspot workloads from the Rodinia benchmark [69].
2.3. Modeling and Simulation of Parallel Applications in Heterogeneous HPC Systems

Formulating the optimization problems in Chapter 1 and describing the proposed optimization methodology in Chapter 5 required defining a formal model of hybrid parallel application execution in a heterogeneous HPC system. The model is also necessary for performing simulation which is proposed as a method for fast evaluation of process mappings and application execution parameters in Section 5.2.

The proposed model assumes that the a priori knowledge about the behavior of processes in the system is limited and precise analytical models of execution time and power consumption of the application are hard to formulate. Instead, a general execution model of hybrid parallel applications in heterogeneous HPC systems is proposed, that allows to express many practical applications. In this section we describe chosen existing approaches to modeling and simulation of parallel application execution in heterogeneous HPC systems. In Section 2.3.1 we focus on the system models. We divide the considerations of application modeling to execution time models described in Section 2.3.2 and power consumption models described in Section 2.3.3. Finally, in Section 2.3.4 we describe chosen simulation approaches.

2.3.1. Modeling Heterogeneous HPC Systems

A heterogeneous HPC system is basically a set of computing devices of various types connected by a network. In numerous approaches to optimization of parallel application execution, the system is modeled just as a set of computing devices with certain characteristics. For example in [70], a heterogeneous computing system is modeled as a set of heterogeneous processors with certain characteristics, including voltage and frequency. The heterogeneity of the system is accounted for by including these hardware characteristics in the considered objective functions such as performance and power consumption. The formulas used to compute the objective functions are usually defined within the system model, aimed for a certain optimization problem setup. Similarly, the model considered in this thesis assumes that execution time functions are defined for all computation and communication operations and idle and stress power consumption functions and core numbers are defined for all computing devices. The model allows for different specifications of these functions and hardware characteristics which makes expressing various specific problem formulations within the proposed framework.

Treating a HPC system simply as a set of computing devices does not take into account the network which connects the devices and its topology, however it is sufficient for many optimization problems. In the cases when network topology is considered, it is usually modeled as a graph. For example in [71], the topology of the computing platform is denoted as host graph, where each vertex denotes a processor or a switch and each edge represents a direct link or cost.
of communication. Although we do not put particular emphasis on network topology in our work, we decided to adopt a graph-based system model, in order to emphasize the importance of network in HPC systems and express network-aware optimizations described in Section 6.1.2.

2.3.2. Modeling Execution Time of Parallel Applications

According to the nomenclature introduced in [72], there are three basic approaches to modeling an application understood as a set of modules that make up the computation. In the first one, the modules execute independently and there is no communication between them. This is not the case in our work, because we assume possible communication between the processes.

The second approach is the task-based model, where the modules are called tasks and are arranged in a directed acyclic graph (DAG). The model is commonly used by the researchers interested in scheduling problems, for example [73, 74, 75, 76, 77, 71]. The application is modeled as an acyclic graph with nodes representing tasks and edges representing the precedence relationship between them. Weights are associated with nodes, representing task execution time, as well as with edges, denoting communication time between the connected tasks. There are various forms of this model. For example, in the macro-dataflow model [78], there is a limited number of computing resources to execute the tasks. Given that task $T$ is a predecessor of task $T'$, if both tasks are assigned to the same processor, no communication overhead is paid. On the contrary, if $T$ and $T'$ are assigned to different processors, a communication delay is paid, which depends upon both tasks and both processors. Another example is the data stream graph (DSG) model [77], which emphasizes data streams, modeled as directed edges in the task precedence graph. Each edge is characterized by a tuple containing an identifier and communication cost of this edge. In our work we do not employ the task-based model, because we assume no a priori knowledge about the precedence relationships between the operations.

The third approach is the process-based model, where processes are arranged in undirected graphs where an edge represents volume of communication between the processes. Despite the coincidence of names, the processes considered in this work are different. In this work, the equivalent of such processes are operations. The sequences of these operations are not known a priori and depend, in turn, on the processes defined in this work. It should be noted all these three approaches to modeling parallel applications can be expressed using the model proposed in this thesis by proper implementation of the computation and communication sequences.

Computation and communication operations have been distinguished in the model used in [79]. The considered problem is mapping a set of independent applications onto a set of heterogeneous processors including CPUs and GPUs. Each application consists of several computational kernels, which are chained together according to some computation logic. However, unlike
in our approach, these dependencies between kernels are known and modeled as edges in the computation graph. The execution time of each kernel on each processor is estimated a priori using the sampling functionality of the StarPU [80] task scheduling platform.

One apparent way to create a model of an existing parallel application in the framework proposed in this thesis is to analyze its source code and indicate which fragments can be simplified to computation and communication operations. Then, simulation can be performed in order to establish the exact sequence of operations resulting from the code logic and communication between the processes. The researcher responsible for the modeling process has to decide how detailed the model should be, bearing in mind that the more detailed the model, the more computationally costly it is to perform simulation of the application. It should be noted that distinguishing the appropriate code regions could be done automatically. For example in the PATUS framework [81] in order to distinguish parts of the code (stencil computations) to be optimized through code generation, a strategy mechanism is used to separate them from the parts related to parallelization and bandwidth optimization.

Apart from the dependencies between certain parts of an application, the application model should define execution time of each part. The general model proposed in this thesis in Section 1.2 delegates this task to the computation time function which can adopt different forms depending on the specific model. For example, the computation time functions for models of applications described in Section 4.1.4 and Section 4.1.5 are defined as functions of the number of floating point operations of the computation operation (which in turn depends on the input data size) and the floating point operation performance of the used processor.

Many optimization approaches are based on an assumption that a matrix is given with estimated times to compute (ETC) each task on each processor (see also Section 3.2.3). Some application modeling approaches propose how to construct this matrix based on the task and processor characteristics. For example in [70] the application is modeled as BoT (Batch of Tasks or Bag of Tasks [82]), meaning a set of independent tasks that belong to different applications and can be run simultaneously. The ETC matrix is derived from the number of cycles of a task and frequency of the processor for each task-processor pair. A similar derivation can be used within the approach proposed in this thesis, through proper implementation of the compTime modeling function (see Section 5.2). On the other hand, the approach proposed in this thesis is different from the BoT approach, because there are communication dependencies between the operations (which are the equivalent of tasks).
2.3.3. Modeling Power Consumption of Parallel Applications

According to [82], among memory, disks, networks, fans, cooling system and other components of a heterogeneous computing system, significant portion of energy is consumed by its processors. Like in the paper, in this thesis only energy consumption of the computing devices available in the system is considered.

Many scheduling optimization approaches focus on DVFS-enabled HPC systems [82, 83, 77, 84, 85], where processor cores can operate in discrete performance states. This capability could be included in the system model. For example, a performance predictor for managed multithreaded applications proposed in [40] can accurately predict the impact of scaling voltage and frequency of a processor. The authors of [86] claim that even dynamic processor shutdown should be considered as an option for reducing power consumption of embedded multiprocessors, due to the trend of significantly increasing static power consumption.

Analogously to the ETC matrix used for execution time modeling, some optimization solutions assume that an average power consumption (APC) matrix is given that defines average power consumption of a certain type of task on a certain type of machine. The authors of [87] indicate that these matrices are usually obtained from historical data in real environments. Some approaches are based on assumptions strictly connected with the nature of their considerations, like for example in the topology-aware task mapping approach [71], where energy required for data transmission between processors depends directly on the total traffic load of the interconnect network. In [70] energy consumption of executing a certain task on a certain processor depends on two components: dissipation power and dynamic power. The first one is a static property of the processor. The second one depends on another static property, namely physical capacitance, as well as two values decided at runtime: supply voltage and frequency of operation. This approach resembles the one adopted in this thesis, described in Section 5.2, where idle power consumption is the static component and the dynamic component is derived from current runtime parameters.

An important decision that must be made in modeling energy consumption of parallel applications is if the idle energy consumption of the computing devices should be included in the total energy consumption. In some approaches the idle energy consumption is not taken into account. For example in the approach to energy-efficient scheduling of batch-of-tasks applications on heterogeneous computing systems proposed in [70] the overall energy consumption is computed as a sum of all task executions, assuming that due to static scheduling the idle slots are negligible. In the experiments presented in [87] all the systems have zero idle power consumption, but setting power consumption to 10% of the mean power for each machine type is used to model the case when the server is powered off but a management controller is still responsive to remote power on signals.
Some approaches to multi-objective time, power and energy optimization of HPC applications focus on finding a set of Pareto-optimal solutions, in order to give the system administrator or programmer the chance to choose the most appropriate solution according to their needs. The authors of [88] propose to take into account a measurement error margin, which enlarges the set of optimal solutions so that no potentially important solution is overlooked.

Analogously to execution time of computation and communication operations, the simulation method proposed in this thesis in Section 5.2 delegates the task of power consumption modeling to the idle and stress power consumption functions which can adopt different forms depending on the specific model. Although these aspects were not considered in the experiments within this thesis, the proposed model allows to include the DVFS states and processor shutdown into the energy consumption function and passing the chosen state from the application model as a parameter. The same applies to using an APC matrix, focusing only on the network traffic or considering physical parameters of the processors.

The model used in this thesis considers power consumption in idle state of the used hardware as well as additional power consumption under stress. In this approach the idle power consumption can be configured to a certain value or a percentage of the stress power consumption. In particular, experiments that assume no idle power consumption can be configured by setting this value to zero.

2.3.4. Simulation of Parallel Application Execution

In computer simulation, the role of a simulator is to compute consecutive states of a model which is a simplified representation of a certain real object. Models used for simulation of parallel application execution in heterogeneous HPC systems have been discussed in Sections 2.3.1, 2.3.2 and 2.3.3. In this section we provide examples in what way such models can be used by a simulator.

A crucial aspect of computer simulation is to choose succeeding points in time for which the simulator should calculate consecutive states of the modeled system. Majority of the approaches to simulation of parallel application execution are based on discrete-event simulation [14], which means that the consecutive states are computed for consecutive events that occur in a discrete sequence in time. An event might represent the end of processing of a certain task by a computing device or transmission of a certain message between two devices. The sequence of events depends on the used application model. The approach used for simulation in this thesis is also based on discrete-event simulation.

SimJava [89], a layered discrete-event simulation framework based on the Java programming language is a foundation for many simulation environments aimed for specific aspects of
computing systems. For example GridSim [90] is a toolkit for modeling and simulation of distributed resource management and scheduling focusing on components of grid systems. It allows for modeling and simulation of heterogeneous grid resources, users and application models and provides primitives for creating application tasks and mapping tasks to resources. Another simulator based on SimJava is OMNeT++ [91], a C++ simulation library and framework focusing on computer networks and other distributed systems. It is mainly used for building network simulators, but the MARS [92] framework based on it contains also modules modeling computing components. In that case, the events in simulation depend on replaying traces of MPI calls.

The approaches to simulation based on traces of previous application executions are called trace-driven and can combine different types of traces with different application models. For example SST/macro [93] uses an application model based on MPI along with MPI trace files in two formats: Open Trace Format and DUMPI. A trace-driven approach has been also proposed for assessing the performance of hierarchical dataflow applications in RADA [94]. The simulation environment used for simulations in this thesis is not trace-driven but tuning of the model to the results of real application executions is suggested. There are approaches to simulated evaluation of parallel application execution where application model is tuned to some existing combinations of execution parameters. For example, it is the case in [95], where curve fitting is used to obtain model parameters for the purpose of evaluating different scheduling policies.

The authors of [94] in further work [96] point out that the performance of simulations is often limited, because synchronization of a large number of processes/threads is required. To overcome the limited scalability, they proposed to use virtualization based on Linux Containers. In the environment used for simulations in this thesis, the number of simulation threads is unlikely to become prohibitively large for one simulation, because instances of processes with the same process implementation running on the same computing device are aggregated and handled by one simulation thread. The simulator is also designed for performing multiple concurrent simulations by utilizing threads and distributed processes connected to a queue of simulation instances, which allows for high scalability.

Machine learning along with traces of previous application executions can be used for evaluating application execution time instead of an application model. For example, a formulation-based predictor is used for evaluating Hadoop MapReduce application execution time in order to find approximately optimal solutions by tuning the application parameters in [97]. The predictor fits to logs of previous Hadoop MapReduce jobs and uses a 2-level machine learning ensemble model consisting of random forest, extra trees and gradient boosting regressors to predict the median, standard deviation and wave of the application execution time.

Established toolkits such as SimGrid [98] for studying the operations of large-scale dis-
tributed computing systems, provide good basis for implementation and simulation of a wide range of algorithms. However, the authors of [99] point out that in most cases the experiments have to be developed from scratch, using just the basic functionality of the toolkit, and the experiments are rarely useful for other researchers. To address this issue, the authors propose the Grid Scheduling Simulator (GSSIM), a comprehensive simulation tool for distributed computing problems. GSSIM includes an advanced web portal for remote management and execution of simulation experiments which allows to share workloads, algorithms and results by many researchers. The MERP-SYS environment co-developed by the author of this thesis and described in Section 5.2 also allows sharing application and system models as well as simulation results by the users, thanks to provided simulation database and Web application.
3. OPTIMIZATION OF PARALLEL APPLICATIONS CONSIDERING EXECUTION TIME AND POWER CONSUMPTION

The most obvious goal of developing parallel programs can be found in the sole HPC (High Performance Computing) keyword. Parallel solutions to existing, as well as new problems are always developed with performance in mind, no matter if measured as execution time of an application or throughput of a real-time system. For this reason, optimization of parallel applications is often connected with only this one objective: performance. However, experience in running HPC applications shows that in many real life scenarios, other, often contradicting objectives need to be taken into account.

For example, running an application in parallel can significantly influence its reliability. In [100] an exponential probability of failure is assumed for each processor in a heterogeneous system. Task scheduling algorithms are proposed, which optimize both makespan (performance) and reliability, letting the user choose a trade-off between reliability maximization and makespan minimization. A scheme for scheduling independent tasks on uniform processors proposed in [101] allows generating an approximate Pareto set of the bi-objective makespan an reliability optimization problem.

Another optimization objective that is increasingly important is power consumption. In this Chapter we focus on existing work in the field of multi-objective optimization of parallel applications with respect to execution time and power consumption. In Section 3.1 we describe the problem of multi-objective optimization and provide examples of existing approaches in HPC.

One of the execution steps proposed in this thesis is task mapping, and more specifically proper assignment of individual parts of the computations of an application to the available computing devices. In Section 3.2 we situate our approach in the area of resource management with special emphasis on energy-awareness and heterogeneous computing systems. Another proposed execution step is parameter tuning. We describe chosen solutions in the field of parameter auto-tuning in parallel applications in Section 3.3.

3.1. Multi-objective Optimization of Parallel Applications

The outline of this section is as follows: In Section 3.1.1 we provide formulation of the multi-objective optimization problem, discuss the possible approaches to taking many objectives into account in the optimization process and choose the Pareto method for consideration in this work. In Section 3.1.2 we describe chosen existing solutions to the problem of optimization of execution time under power consumption constraints, which is investigated in Section 6.1.2 of this thesis. In Section 3.1.3 we discuss examples of existing work which show that this trade-off
exists for execution time and power consumption in various hardware configurations and executed applications. Finally, in Section 3.1.4 we provide examples of existing solutions considering Pareto optimization in the field of parallel computing.

3.1.1. Multi-objective Optimization Problem Formulation

In general, the goal of solving an optimization problem is to find a point in a given decision space, for which the value of a given objective function is minimal.

**Definition 15.** Let \( f \) denote an objective function of an optimization problem.

For example, in our work the objectives are application execution time and power consumption. Usually there are certain constraints which have to be fulfilled in order for the decision point to be a feasible solution to the problem. In this work the constraints may be related to numbers of available computing devices, possible sizes of data chunks, numbers of processes required by the application etc. The constraints are often expressed as mathematical functions, however a more general statement would be that the decision point should belong to a feasible set, which results from the constraints.

**Definition 16.** Let \( \mathcal{X} \) denote the feasible set of an optimization problem.

Having defined the objective function \( f(x) \) and the feasible set \( \mathcal{X} \), a mono-objective optimization problem can be stated as follows:

\[
\min_x f(x) \quad \text{subject to} \quad x \in \mathcal{X}
\]

The convention in optimization problems assumes minimization of a function, however the definition can be easily used for maximizing (for instance real-time application throughput), by using a function \( f'(x) = -f(x) \) as an objective. Because there is only one objective, the definition of optimum is straightforward:

**Definition 17.** A point \( \hat{x} \in \mathcal{X} \) is an optimum of an optimization problem if and only if:

\[
\forall x \in \mathcal{X} \quad f(\hat{x}) \leq f(x). \quad (3.1)
\]

In the case of multi-objective optimization problems, defining the optimal solution is less straightforward, because the objective consists of \( n \) objective functions:

**Definition 18.** Let vector \( F(x) = [f_1(x), \ldots, f_n(x)] \) denote a vector of objective functions, where \( n \) is the number of simultaneously optimized objectives.
Then, following the train of thought proposed in [102], the optimization problem can be written as:

\[
\text{"min" } F(x) = [f_1(x), \ldots, f_n(x)]
\]

subject to \( x \in \mathcal{X} \)

The quotation marks in the "min" notation are used for a reason. In the case of multiple objectives, different interpretations can be associated with the minimization operator. Various interpretations have been discussed in [102]. In the field of energy aware scheduling, a taxonomy of optimization approaches has been presented in [75]. The multi-objective approaches are divided into three classes: aggregation, lexicographic and Pareto.

The traditional lexicographic approach assumes some preference order of the objectives. A set of mono-objective problems is solved sequentially for the consecutive objectives until a unique solution is found.

In the case of aggregation methods, a function is used to transform the multi-objective optimization problem into a mono-objective one by combining the objective functions into a single in one aggregation function. For example, the authors of [70] propose algorithms which optimize two objectives (minimization of makespan and energy consumption) at the same time. The objectives are combined into one weighted aggregation cost function. A parameter \( \alpha \) denoting the weight of each of the objectives is set to the value 0.5, so the both objectives are equally prioritized.

In this work we focus on the third approach: the Pareto method. In this case, instead of one point, the solution to the optimization problem is a set of Pareto-optimal points:

**Definition 19.** We say that \( F(x_1) \leq F(x_2) \) if \( \forall i=1, \ldots, n : f_i(x_1) \leq f_i(x_2) \). Point \( x_1 \in \mathcal{X} \) is Pareto-optimal if there is no such \( x_2 \in \mathcal{X} \) that \( F(x_2) \leq F(x_1) \). Let set of points \( \mathcal{X}^* \in \mathcal{X} \) denote the Pareto set.

In other words, the solution to the optimization problem is the set \( \mathcal{X}^* \) of all such points \( \hat{x} \in \mathcal{X}^* \in \mathcal{X} \), that for all other points there is at least one objective function which value is lower for the point \( \hat{x} \). This means that in the case of two objectives considered in this work, if a point \( \hat{x} \) is in the Pareto set \( \mathcal{X}^* \), then for every other point in the decision space the point \( \hat{x} \) has at least lower execution time or power consumption.

Additionally, it is important to distinguish the notion of Pareto front:

**Definition 20.** Let set of objective function values of all Pareto-optimal points \( \mathcal{F}^* = \{ F(x) : x \in \mathcal{X}^* \} \) denote the Pareto front.

As indicated in [88], the Pareto front contains significantly richer information that one obtains from single-objective formulations. The solution provides not only solutions globally optimal in terms of the consecutive objectives, but also fully illustrates the trade-off between the objectives. The authors notice that a multi-objective formulation is needed for the auto-tuning problem.
In the context of trade-offs between time, energy and resource usage, authors of [103] state that the multi-criteria scenario "requires a further development of auto-tuners, which must be able to capture these trade-offs and offer the user either the whole Pareto set or a solution within it".

Indeed, authors of [104] state that multi-objective approaches have not been extensively researched in the past and stress the advantages of generating the whole Pareto front for the problem of multi-objective auto-tuning of programs. Firstly, the user can visually explore the Pareto set and select the solution which fits his interest best. Secondly, some kind of aforementioned aggregation method can be used for automatic selection of an optimal solution. Having access to the whole Pareto front before constructing an aggregation function allows for normalizing the function in order to avoid drawbacks resulting from different value ranges of the objective functions. Finally, the authors notice that computing the Pareto front does not necessarily require additional computational effort comparing to a single-objective approach.

Summing up, in this work we focus on the multi-objective Pareto optimization problem of execution time and power consumption defined in Equation 1.1 and two related mono-objective optimization problems defined in Equations 1.2 and 1.3. The difference between the two latter lies in the feasible set: the first one is constrained by the power consumption limit.

3.1.2. Optimization of Execution Time Under Power Consumption Constraints

A particular type of multi-objective optimization problem is when there are strict constraints imposed on one of the objectives. In the case of the bi-objective problem formulation considered in our work this would mean a strict deadline for the execution or limit of power consumption of the computing system utilized by an application. For example, multi-objective optimization using Particle Swarm Optimization (PSO) algorithm with energy-aware cost function and task deadlines has been proposed in [105] for partitioning tasks on heterogeneous multiprocessor platforms. In both cases of deadlines (energy or performance), although there are two objectives taken into account, a solution to the problem can be a single point like in the single-objective problem in Definition 17, provided that the constraint on the other objective is fulfilled.

Optimization of throughput of single power-constrained GPUs has been investigated in [106]. The authors notice that although throughput is proportional to the product of the number of operating cores and their frequency, because of limited parallelism of some applications, it might be beneficial to scale these parameters. A technique has been proposed for dynamic scaling of the number of operating cores, the voltage/frequency of cores and bandwidth of on-chip interconnects/caches and off-chip memory depending on application characteristics. Experimental results of executing 15 CUDA applications from GPGPU-Sim [107], Rodinia [69] and ERCBench [108] benchmark suites show that the proposed technique can provide on average 20% higher through-
put than the baseline GPU under the same power constraint. Although the benefits from applying the proposed technique have been presented by extensive exploring of arbitrarily chosen combinations in the search space, the work leaves open questions in the field of optimization - how to automatically find the optimal values using an optimization algorithm and simulations or real executions.

Optimization of a HPC system throughput with power constraints has been also considered on a larger scale of parallelization in data centers [95]. The problem of maximizing throughput of HPC data centers under a strict power budget has been formulated as an Integer Linear Programming (ILP) problem. The proposed online resource manager uses overprovisioning [109], power capping through RAPL interface [110] and moldable/malleable job scheduling to achieve high job throughput of power-constrained data centers. Both real experiments on a 38-node Dell PowerEdge R260 cluster and simulations of large scale executions show improvements in job throughput compared to the well-established power-unaware SLURM [111] scheduling policy.

Because taking into account all variables for start and end time of jobs would make the ILP problem "computationally very intensive and thus impractical in many online scheduling cases", the authors proposed a greedy objective function that maximizes the sum of so called "power-aware speedup" for all jobs that are ready for execution. This "power-aware speedup" is a value resulting from the Power Aware Strong Scaling (PASS) model contributed in the paper, which is a power-aware extension of the model for speedup of parallel programs proposed in [112]. Using the single objective function made the ILP problem computationally adequate for online scheduling.

A strict constraint on execution time has been imposed on multi-threaded applications optimized in terms of energy consumption due to off-chip memory accesses in [113]. In the proposed DVFS-based algorithm, the throughput-constrained energy minimization problem has been formulated as multiple-choice knapsack problem (MCKP). A cost function is defined for binary variables which denote if a certain frequency level should be assigned or not to a given process. The algorithm uses a performance model based on regression of data points reported by hardware performance counters and a power model that focuses on numbers of floating point instructions, branch instructions, L1 and L2 data cache references and L2 cache misses. Similarly to the scheduling algorithms described in Section 3.2.3, the proposed optimization algorithm assumes strong a priori knowledge about the application behavior.

However, in order to relax this assumption, authors propose also P-DVFS, a predictive online version of the algorithm which, similarly to the scheduling algorithms described in Section 3.2.4, does not require a priori knowledge about the application. The proposed prediction technique relies on the similarity between present and future MPI distributions. Experimental results from 11 chosen benchmark applications from SPEC2000 [114] and ALPBench [115] bench-
mark suites executed on a Pentium Dual Core processor proved around 10% average power reduction as compared to the most advanced related work.

Dynamic Core and Frequency Scaling (DCFS) [116], a technique for optimizing the power/performance trade-off for multi-threaded applications is an extension to DVFS which apart from CPU frequency, adjusts also core counts (core throttling). The adjustments are made dynamically during the application execution, in order to optimize performance under a certain power consumption constraint. During the training phase, the application is executed for a short period of time for chosen combinations of core numbers and CPU frequencies. The optimal configuration is chosen based on measured IPS (instructions per second). The proposed technique dynamically reacts to the changes in application behavior: the IPS values are measured during the execution phase and if the value changes by a given threshold, the application is switched to the training phase for a certain period.

The proposed technique has been evaluated on ten benchmark applications from PARSEC [117] executed on AMD Opteron and Intel Xeon processors. Although the average performance improvement of multiple benchmark applications is 6%, the majority of this score depends on one, poorly scalable application from the domain of enterprise storage for which the performance improvement is 35%. There is barely any performance improvement in the cases of other applications, even for two poorly scalable ones, because they are the most memory-bounded. These results mean that the proposed technique is suitable only for a specific kind of applications. One of the reasons of low performance is the overhead of the training phase. The authors consider various lengths of the training phase period, as well as IPS change thresholds. The DCFS method could benefit from a computationally cheaper way to adjust the execution parameters, for example a simplified application model and/or simulation scheme.

3.1.3. Energy/Time and Power/Time Trade-offs in Parallel Applications

A multi-objective approach to optimization would not be needed if the considered objectives were not contradicting in some cases. Existence of a trade-off between energy consumption and execution time of an application may seem counter-intuitive. One could argue that the shorter a program runs, the less energy it consumes. This was indeed the case for a discrete Fourier transforms application executed on Intel Pentium M microprocessor investigated in [118], as long as the application was optimized only via an algorithm selection software technique. As expected, the authors state that for a given voltage-frequency setting of the microprocessor, the fastest algorithm was also the lowest energy algorithm. However, in cases when voltage-frequency scaling was also considered, trade-offs between energy consumption and execution time have been reported. Namely, for some problem configurations it was possible decrease overall energy consumption
at the cost of increasing the execution time by executing the program on a lower microprocessor gear.

Energy/time trade-offs have been also shown in [119] on the example of executing programs from the Numerical Aerodynamic Simulation benchmark [120] on a power-scalable cluster using MPI. The hardware in the cluster allowed energy saving by scaling down the CPUs. The decision space concerned choosing among available gears at which the processors were operating, as well as the number of processors used for execution. In the cases when the number of processors utilized by the application was fixed, there were usually single or few Pareto-optimal points in the decision space. However, when the number of used processors ranging from one to nine was a degree of freedom in the optimization, energy/time trade-offs were reported for several applications. The trade-offs vastly depended on the scalability of the programs. In some cases energy and time could be saved by executing a program on more nodes at a slower gear rather than on fewer nodes at the fastest gear. This shows that non-trivial trade-offs between energy consumption and execution time can appear during parallel execution.

These trade-offs may be even more complicated if the computing devices available in high performance computing systems are heterogeneous, the application consists of multiple tasks and execution time of a particular task can differ depending on the assigned device. Such a model has been studied in [121], where the Variation (COV) method [122] has been used to model a heterogeneous set of machine types and task types. Different resource allocations resulted in different makespan and energy consumption values, giving a wide set of Pareto-optimal options to choose from. Examples of Pareto fronts for a system modeled in such a way have been also presented in [87] for various numbers of computing machine types.

The authors of [121] focused on discovering the Pareto front using the NSGA-II evolutionary algorithm, but also investigated in detail how solutions in the Pareto front differ from one another. For this purpose, the authors analyzed the individual finishing times and energy consumptions for chosen points in the Pareto front. Apparently, the location of a point in the Pareto front depends on balancing of the individual tasks both in terms of execution time and energy consumption. In the case of the points with extremely low execution time, the finishing times of individual jobs were fairly balanced and relatively low, while the energy consumption values were uneven with the highest values on a relatively high level. On the other hand in the case of points with extremely low energy consumption, the task completion times were uneven, while the energy consumption levels were balanced. This observation helps to understand that in the case of highly heterogeneous systems, the trade-off between execution time and energy consumption can be partly explained as a trade-off between fair balancing of the completion times and energy consumption values of individual tasks of the application.
The relationships between execution time, power consumption and energy consumption of HPC codes have been studied in [88]. Pareto fronts for energy/time and power/time trade-offs are shown for a set of chosen HPC applications executed on chosen parallel architectures. The results include measurements from real executions of:

- finite-difference time domain [123], sparse matrix multiplication [124] and quick sort [125] on an Intel Xeon Phi coprocessor;
- finite-difference time domain, bi-conjugate gradient and Jacobi computation [123] on an Intel Xeon E5530 processor;
- fine element mini-application miniFE [126] on a Vesta IBM Blue Gene/Q 10-petaflop supercomputer.

In all presented power/time charts the Pareto front consisted of several points, which proved that the power/time trade-off exists for the selected problem configurations. However, energy/time trade-off was reported only for the miniFE application, due to considering the parameter of the number of used nodes. In other experiments there was only one point in the energy/time Pareto front. This means that in these experiments there was no energy/time trade-off, because there was one solution that was optimal for both objectives.

The authors notice that since power corresponds to a rate of energy, the problem of bi-objective optimization of execution time and power consumption is clearly related to the problem of bi-objective optimization of execution time and energy consumption. Moreover, the authors prove that all points on the energy/time Pareto front have a corresponding point on the power/time Pareto front. Specifically, denoting the time, power and energy objectives by T, P and E respectively, the authors prove that $X^*_{E} \subseteq X^*_{P}$ where $X^*_{P} \subseteq \mathcal{X}$ is the set of Pareto-optimal points for the vector of objective functions $F = [T, P]$ and $X^*_{E} \subseteq \mathcal{X}$ is the set of Pareto-optimal points for the vector of objective functions $F = [T, E]$.

The conclusion from these findings is that exploring the power/time trade-off gives richer information about the potentially favorable execution configurations, including those in the energy/time Pareto set. For this reason in this work we focus on bi-objective optimization of execution time and power consumption.

3.1.4. Pareto Optimization of Parallel Application Execution

One method of finding optimal values of decision variables in an optimization problem is exhaustive search [127], which means evaluating the values of objective functions for all possible combinations of decision variable values. This approach may be infeasible in many cases of optimization of execution time and power consumption in HPC. First, precise evaluation of the objective functions may involve actual execution of the application, which is often extremely costly.
In this work we propose using the simulation method described in Section 5.2 to evaluate the objective functions at low cost.

Secondly, the decision space of the optimization problem may be high-dimensional and, thus, exhaustive search may require vast numbers of evaluations. Even in the case of using a low cost model or simulator, the number of evaluations often makes the exhaustive search method infeasible. One approach to solve this problem is to use derivative based optimization techniques, such as gradient descent. However, this approach requires the objective functions to be differentiable. Some models of parallel application execution provide differentiable formulas for execution time and power consumption, but it is rarely the case considering complexity of the contemporary parallel applications and systems.

In other cases derivative-free approaches are needed, such as genetic algorithms, particle swarm optimization etc. Their assumption is that the explicit mathematical formula behind the objective functions is unknown and evaluations are possible for certain points in the decision space, however the number of evaluations is treated as the main computational cost of the algorithm. Such a simulator for evaluating the objective functions, as the one proposed in this work can be used as an evaluation function in the derivative-free algorithms.

For example, the framework for multi-objective auto-tuning proposed in [30] (described more broadly in Section 3.3.3) allows to compute the Pareto set for the trade-off between execution time and percentage of hardware utilization of parallel codes. The optimizer uses a combination of compiler and runtime techniques and the decision parameters include tile sizes in loop tiling, thread counts and choosing between code versions. The authors claim that in the considered testbed, the Pareto set is prohibitively large, making exhaustive search impossible. A simple genetic algorithm is proposed, but still the number of required steps is too large to represent a viable option. Finally, the differential evolution GDE3 [128] algorithm is used in the optimization phase. At runtime, the system can choose an optimal configuration from the computed Pareto set using weights provided for each optimization goal.

Pareto fronts have also been explored to trade-off energy and performance in a heterogeneous HPC system where multiple optimal solutions resulted from different task assignments [129]. The estimated times to complete of each task on each machine were assumed to be given in an ETC matrix (generated randomly for the experiments). The finishing times and energy consumption were modeled by strict mathematical formulas, so evaluating one solution was relatively cheap computationally. Still, in the testbed with 1100 tasks of 30 types and 36 machines of 9 types, exhaustive search was infeasible for the scheduling process, which needs to be fast in order not to add a significant overhead to the overall processing time.

For this reason, as an alternative to the exhaustive search solution, NSGA-II algorithm [130]
has been used, which is a popular adaptation of the genetic algorithm optimized to find the Pareto front for a multi-objective optimization problem. The algorithm modifies the fitness function of the genetic algorithm to work well for discovering the Pareto front. An important phase of a genetic algorithm is seeding the initial population. Employing the basic seeding method using the optimal energy solution, suboptimal minimum makespan solution and a random initial population, the algorithm needed hours of computations to discover a reasonable approximation of the Pareto front in [129]. The authors proposed a different seeding strategy for generating configurations with full allocations. This modification allowed the optimization algorithm to achieve significantly closer approximations of the Pareto front in just dozens of seconds.

It should be stressed that in the cases where defining a strict mathematical formula for the optimization objectives is possible, there is often no need to use a simulator and search for the optimal solutions either by exhaustive search or evolutionary algorithms. For example, the performance of the NSGA-II algorithm has been significantly outperformed by a linear programming solution in [87] for multi-objective optimization of energy and makespan of Bag of Tasks applications. However, using this technique requires defining linear objective functions for the considered objectives. As discussed in Section 2.3, in this work we focus on cases where exact formulas for the optimization objectives are unknown and, thus, we consider the evolutionary algorithms for potential utilization in the proposed optimization methodology.
3.2. Energy-aware Resource Management in Heterogeneous HPC Systems

Mapping processes to computing devices is an important part of the optimization methodology proposed in this thesis. In this section we provide background for our work in the field of resource management. In Section 3.2.1 we introduce the global static task mapping problem, which is an important part of the problem formulation proposed in Chapter 1. We discuss chosen scheduling optimization solutions focusing on network topology in Section 3.2.2. The remaining related work is divided into solutions with strong a priori knowledge about the optimized application in Section 3.2.3 and with limited knowledge in Section 3.2.4.

3.2.1. Global Static Task Mapping Problem

Resource management has been a crucial topic in distributed computing for many years. Numerous different problem formulations have been stated, also in other fields, such as control theory, operations research and production management. Comparing the approaches has become hard because of their vast number and essential differences resulting from particular setups and applications. In order to achieve categories of comparable approaches, a taxonomy of distributed scheduling approaches has been proposed in [131].

According to this taxonomy, the approach proposed in this thesis is global, because it considers where to execute a process and assumes that local scheduling is the task of the operating system of the computing device. This local scheduling is connected with assigning processor time to processes, as well as optimizing the utilization of device internals. These tasks are solved by the operating system and increasingly often by internal schedulers in the devices. This work does not explore the details of these tasks, focusing on the problem of global scheduling.

Global scheduling problems are divided in the taxonomy to static and dynamic scheduling problems. In the case of static scheduling, information regarding the total mix of possible processes in the system is available before the application execution. In this sense, the approach proposed in this thesis considers a static scheduling problem, because a static schedule in the meaning of assignment of processes to computing devices is fixed at the beginning of the execution.

Global static scheduling problems are divided in the taxonomy to optimal and suboptimal problems. As indicated in [131]: "In the case that all information regarding the state of the system as well as the resource needs of a process are known, an optimal assignment can be made based on some criterion function. Examples of optimization measures are minimizing total process completion time, maximizing utilization of resources in the system, or maximizing system throughput. In the event that these problems are computationally infeasible, suboptimal solution may be tried". In this sense, the approach proposed in this thesis is suboptimal, because not all information
about the processes is known a priori. For example, there is no estimation of execution time or resource needs of each process. We argue that for many applications it is hard or impossible to prepare a feasible criterion function, which could be used for preparing an optimal assignment.

Global static suboptimal scheduling problems are divided in the taxonomy to heuristic and approximate problems. Heuristic algorithms make use of special parameters which are correlated to system performance in an indirect way, and such alternate parameters are much simpler to monitor or calculate. Such heuristic algorithms make the most realistic assumptions about a priori knowledge concerning process and system loading characteristics. The assumptions can be made in approaches to optimization of specific applications in specific systems. In this thesis we propose a general approach which cannot include such assumptions. Hence, it is an approximate approach, in which “instead of searching the entire solution space for an optimal solution, we are satisfied when we find a ‘good’ one” [131], based on certain evaluation metrics.

According to [131], important factors that determine if the suboptimal-approximate approach is worthy of pursuit include availability of a function to evaluate a solution and the time required to evaluate it. Results from real execution of a parallel application can be such a function. In cases when the factor of evaluation time is prohibitively large, we propose using functions based on modeling and simulation, as described in Section 5.2.

To sum up, the approach proposed in this thesis is giving a suboptimal-approximate solution to the global static scheduling problem, also known as task scheduling, task mapping or task allocation. The problem of task partitioning among heterogeneous multiprocessors has been proven NP-hard in [132].

In [133], the resource management process was divided into three stages:

- scheduling – deciding when each job should run;
- allocation – determining which nodes take part in the computation;
- task mapping – matching the job to individual computational elements (nodes/cores).

The authors assumed that the first two stages are usually done at the system level and focused on improving the task mapping stage, which in that case meant mapping tasks to MPI ranks.

In this nomenclature, the approach proposed in this thesis focuses on the task mapping stage which includes allocation, because assigning no processes to a device means not allocating the device. In this sense, scheduling of operations in the proposed approach depends on the process implementations given in the application model. According to [100], the problem of mapping each task of an application onto the available heterogeneous resources in order to minimize the application runtime is known to be NP-hard.
3.2.2. Network-aware Scheduling

One of the important factors that influence execution of parallel applications in HPC systems is network topology. In [78], the authors point out that the traditional macro-dataflow model of application execution was inconvenient, because it assumed unlimited network resources, allowing simultaneous communications on a given link. They propose a communication-aware and one port model in order to take into account the influence of network topologies on the scheduling algorithms. For example, the Data Intensive and Network Aware (DIANA) scheduling technique proposed in [134] takes into account not only data and computation power, but also network characteristics such as bandwidth, latencies, packet loss, jitter and anomalies of network links.

Network-aware scheduling is still an active branch of scheduling studies. For example, the objective for scheduling optimization in [71] is defined as minimization of numbers of hops in shortest paths between devices. This problem is called topology-aware task mapping or just topology mapping.

Resource scheduling in data centers with two-tiered and three-tiered network architectures has been studied in [135]. The authors propose a topology-aware scheduling heuristic and demonstrate its performance using the GreenCloud [136] packet-level simulator.

In [77] the response time of a real-time stream computing environment is optimized by minimizing the latency of a critical path in a DAG representing the application. The proposed ReStream solution has been verified in a simulation environment based on the Storm [137] platform.

A simulator for evaluating the fitness of the intermediate solutions in an optimization algorithm was used for example in [133]. The authors propose a local search algorithm which tries swapping pairs of tasks in order to minimize the application execution time by reducing the number of network hops. Fitness of the solutions is measured by a simulator [138] and a swap is preserved if it decreases the number of hops. The proposed solution, aimed for applications with stencil communication patterns, has been proven useful on the example of a shock physics model application executed on a Cray XE6 system.

In the model proposed in this thesis, network topology can be taken into account in the system model through proper implementation of the $\text{commtime}$ function (see Section 5.2). Network topology plays also an important role in experiments with real application execution regarding network-aware optimizations described in Sections 6.1.1 and 6.1.2.

3.2.3. Heuristics Based on Strong a Priori Assumptions

There are numerous approaches to task scheduling which assume that the (ETC) matrix is given [139, 140, 75, 79, 84, 85, 70]. The matrix contains the expected execution times of each task on each processor. Variations of this assumption are sometimes used, for example a
computation cost matrix [141]. A similar approach is often used towards power consumption, for example authors of [87] assume that the APC matrix is given.

In such problem frameworks, meta-heuristics are often used, including genetic algorithms [139, 140, 75], tabu search [140], simulated annealing [140], A* [140] and shuffled frog-leaping [84]. The objective is to obtain an optimal schedule, namely the assignment of tasks to processors as well as determining order of execution within each processor. A thorough review of traditional and energy-aware algorithms based on ETC matrix has been provided in [70]. The authors also propose two new scheduling algorithms which introduce a task migration phase for minimizing the makespan and energy consumption of the application.

The task mapping problem has been also considered in the topology-aware context in [71]. The authors propose two graph-theoretic mapping algorithms: a generic one with inter-node and intra-node mapping and a recursive bipartitioning one for torus network topology, which takes into account compute node coordinates.

Focusing on the aspect of heterogeneous CPUs, paper [142] proposes Heterogeneity Aware Meta-scheduling Algorithm (HAMA), claimed to reduce between 23 and 50% of energy consumption. The grid meta-scheduler described in the paper, collects information about the grid infrastructure and users, and periodically passes it to the HAMA algorithm. Based on parameters such as average cooling system efficiency, CPU power, frequency and computation time slots, the algorithm first selects the most energy efficient resources. What is more, if possible, it utilizes the Dynamic Voltage Scaling capabilities of the CPUs.

3.2.4. Approaches With Limited a Priori Knowledge

The model proposed in this thesis is especially useful for modeling applications for which, at a given granularity level, it is hard or impossible to estimate the exact graph of individual tasks and communication dependencies between them, before actual execution of the application. Chosen approaches that also assume limited a priori knowledge about the application and its processes are described in this section. For example authors of [83] notice that task execution times in large heterogeneous computing systems may vary due to factors which are hard to incorporate into the model, like cache misses or data dependence of the execution times. They propose a stochastic measure for minimizing the probability of violating the makespan and energy constraints. This robust measure is used as the objective function for various heuristic algorithms, including tabu search and genetic algorithm with local search.

The application model in [82] is a Bag of Tasks, which could have different execution time for different inputs. Because of that, the authors interpret task execution times as random variables and consider stochastic task scheduling. They propose algorithms with an objective to improve
the weighted probability of meeting both deadline and energy consumption budget constraints. The proposed algorithms are performing significantly better than the traditional heuristics in an experimental setting with DVFS-enabled HCS, for both randomly generated BoT applications and real-world multimedia applications.

Authors of [143] propose a simulated annealing approach to optimizing task allocation in a grid environment with respect to execution time. Comparison to an ad-hoc greedy scheduler shows that in certain cases the simulated annealing approach allows to avoid local minima in the optimization. During the optimization process, the solutions are evaluated using a hand-crafted performance model. The approach is verified on a simplistic testbed consisting of 15 machines, running a parallel numerical solver application. The authors emphasize, that the usefulness of their approach depends vastly on the accuracy of the performance model, for which the simulation method proposed in this thesis might be a convenient replacement.

The uncertainty about the processes has been also considered in the field of cloud computing. The authors of [76] notice that the existing efficient schedulers require a priori information about the processes and ignore cluster dynamics like pipelining, task failures and speculative execution. They propose a new scheduling algorithm for minimizing average coflow completion time (CCT) in data centers by prioritizing the processes (coflows) across a small number of priority queues. The coflows are separated into the queues based on their past activity in the cluster. The solution is proven efficient by experiments run on 100-machine EC2 clusters.

Lack of knowledge about the task processing times has been also studied in the context of game theoretic approach to distributed scheduling [144]. The considered problem is a scheduling game, where each player owns a job and chooses a machine to execute it. Even if there exists an equilibrium in this game, the global cost (makespan) might be significantly larger than in the optimal scenario. There exist policies that reduce the price of anarchy, but typically they have access to the announced execution times of all tasks in the system. Policies studied in the paper are non-clairvoyant, which means that they assume that the task processing times are private for the players and, hence, not available a priori.
3.3. Parameter Auto-tuning in Parallel Applications

A significant part of the parallel application optimization methodology contributed in this thesis can be described in terms of parameter auto-tuning. In this section we provide background for our work in this field. In Section 3.3.1, the problem solved within this thesis is classified as a problem of offline auto-tuning of system parameters. Then, chosen approaches to parallel application auto-tuning are described, divided into those involving exhaustive search of the optimization search space in Section 3.3.2 and those involving combinatorial search in Section 3.3.3.

3.3.1. Offline Auto-tuning of System Parameters Problem

According to the proceedings of a recent seminar in the field of automatic application tuning for HPC architectures [127], approaches to application auto-tuning can be divided into black-box and white-box. The search process in white-box algorithms can be guided, because there is some a priori understanding of the underlying problem. Notable examples of white-box auto-tuning approaches are ATLAS [145] for automatic tuning of linear algebra applications and Spiral [118] for automatic generation of linear transform implementations. In the ELASTIC [146] environment for large scale dynamic tuning of parallel MPI programs, the knowledge required to guide the auto-tuning process is integrated as plugins which implement an API for modeling performance and abstraction models of the application.

Many auto-tuning solutions focus on optimizing parallel programs by choosing between multiple alternatives of semantically equivalent but syntactically different versions of a program. Two ways of source code adaptation are distinguished in [145]. The first one is to supply various hand-tuned implementations and allow the optimization algorithm to choose between them. The second method is automatically generating the code by using manual transformations or compiler options.

For example, an auto-tuning framework introduced in [147] is able to parse Fortran 95 codes in order to extract Abstract Syntax Tree (AST) representations of stencil computations. The framework generates multiple versions of optimized stencil codes by multiple transformations of the AST code representation. The results of the transformations depend on a number of serial and parallel optimization parameters. In order to achieve a feasible subset of parameter spaces, architecture-aware strategy engines are used. Then, an auto-tuner performs exhaustive search on the limited parameter space. Additionally, the framework allows migrating existing Fortran codes to emerging parallel APIs such as CUDA. Focus on stencil computation has been also put in the PATUS framework [81], which allows generating code of stencil computation kernels from initial codes called specifications. The framework automatically distinguishes regions of the code which contain so-called operations responsible for the stencil computations and generates different ver-
In contrast to white-box approaches, in black-box approaches there is an assumption that the only knowledge about the optimized application can be obtained through evaluating an instance of parameter set, and not through analysis of its code. In this sense, the execution steps proposed in this thesis in Section 5.1 consist of both white-box and black-box steps. The first step, process optimization is a white-box optimization step, where an analysis of processes in the application can be made in terms of the underlying operations and modifications of the operation sequences can be made. After this step has finished, the succeeding steps solve a black-box optimization problem, because no further modifications of the processes are allowed.

Similarly to scheduling approaches described in Section 3.2.2, there are also tuning approaches that stress the importance of network interconnect. Authors of [148] argue that optimization of application execution in next generation large-scale platforms, especially for energy efficient performance, should not only use CPU frequency scaling, but could also benefit from tuning other platform components, for example network bandwidth scaling. The paper exploits power measurement capabilities of Cray XT architecture and proposes a static tuning approach which demonstrates energy savings of up to 39%. It is noted that a dynamic approach is also an important area of investigation, though it is challenging due to reliability issues and overhead of frequency state transitions.

According to [104], execution parameters such as numbers of threads, their affinity, processing frequency and work-group/grid sizes of GPU applications are equally important tuning parameters, called system parameters. Even the mapping of threads onto physical cores (discussed in more detail in Section 3.2) can be considered as a part of the parallel application auto-tuning process. Two classes of auto-tuning approaches are distinguished in the paper: offline and online. In the offline version the program is tuned before running it in production mode. The online version has challenging aspects, because while being executed during the application execution it implies performance overhead and makes the execution more exposed to possible poor performing parameter configurations. The optimization approach proposed in this thesis is based on evaluating multiple execution configurations before the actual execution, thus in the sense of this classification it focuses on the problem of offline auto-tuning of system parameters, to which we refer to as application execution parameters and process mappings. Using simulation for re-evaluating certain application execution parameters during the actual application execution can potentially be beneficial for specific types of application and is an interesting direction for future work.
3.3.2. Auto-tuning Approaches with Exhaustive Search

A plugin-based approach has been used in the European AutoTune project to extend the PERISCOPE [149] performance analysis tool by a number of tuning plugins, producing the Periscope Tuning Framework (PTF) [150]. The plugins may employ expert knowledge or machine learning to perform multi-aspect application tuning with regard to energy consumption, inter-process communication, load balancing, data locality, memory access and single core performance. The tuning process starts with preprocessing C/C++ or Fortran source code files using MPI or OpenMP in order to distinguish code regions and parameters that may influence their performance. For each code region, tuning scenarios defined by the plugins perform search strategies in the parameter search space in order to minimize a tuning objective, defined as a function which may take into account measurements like execution time and energy consumption.

The applicability of the PTF framework was presented in [150] on the examples of the following plugins:

- maximizing throughput of high-level pipeline patterns written in C/C++ with OpenMP pragma-annotated while loops, executed on single-node heterogeneous manycore architectures using StarPU [80] for execution on CPUs and GPUs. The main tuning parameters were stage replication factors and buffer sizes;
- minimizing execution time of HMPP codelets - computational units written in C or Fortran, annotated with directives which allow the special CAPS compiler to translate them to hardware-specific languages such as CUDA and OpenCL. Considered tuning parameters were connected with the codelet internals such as unrolling factors, grid sizes, loop permutations and also target-specific variables and callbacks available at runtime;
- minimizing energy consumption of applications executed on shared memory processors with CPU frequency scaling. The tuned parameters were energy efficiency policies and used CPU frequencies;
- minimizing execution time of MPI SPMD programs by tuning MPI annotated code variants and environment parameters including numbers of executed tasks, task affinity, communication buffer sizes and message size limits;
- reducing execution time of sequential programs by tuning the selection of compiler flags.

The PTF framework has been also used in [151] to minimize execution time of MPI programs by tuning the parameters of MPI-IO communication interface. The proposed PTF plugin aimed for automatically optimizing the values of selected MPI-IO hints and MPI parameters, which are normally optimized by programmers who have a deep understanding of the application behavior on the target system. The authors state that because of high dimensions, the space of tuning
parameters still needs to be restricted using expert knowledge. Exhaustive search is used to find the optimal parameter values. Exploring more elaborate search algorithms as well as parallel application models is listed as future work.

The importance of application auto-tuning has been stressed in the context of code portability in [152], where an OpenCL implementation of convolutional layers for deep neural networks is proposed. Codes in OpenCL can be executed without changes on various hardware by compiling them using local compilers dedicated to certain computing architectures. However, usually due to the differences between architectures, in order to develop a highly efficient implementation, one needs to take into account specific coding practices and low-level details. The authors propose to implement the kernel in a tunable way, accepting size of the input images, filters and computing thread work-groups for each layer of the optimized neural network as inputs. The approach achieves full portability of the kernels without the need to develop multiple specific implementations, while maintaining good performance. For the auto-tuning problem, the optimization space is searched exhaustively, however automatic space pruning is done, so that only nearly 20% of the configurations are tested. Auto-tuning a single layer out of the five layers of the neural network takes about one hour, which is claimed not to be a significant overhead compared to the entire network training time that could take weeks of repeatedly running the same set of kernels.

Often the search space of an auto-tuning problem is high dimensional and prohibitively large to perform exhaustive search. One approach to perform auto-tuning in such situations is to explicitly prune the search space. For example, a search space reduction procedure has been proposed for auto-tuning of a parallel implementation of the 2D MPDATA EULAG algorithm, executed in a hybrid CPU-GPU architecture [22]. The algorithm consists of 16 stages linked with non-trivial data dependencies and the implementation consists of 16 kernels. The parameters that constitute the search space in the auto-tuning problem have been divided into two groups. The parameters in the first group create a local search space for each kernel individually, and include work-group sizes and sizes of vectors for vectorization. The second group consists of specific parameters related to the entire algorithm (this division of parameters is similar to the one proposed in this thesis, with the local parameters resembling execution parameters and algorithm-related parameters resembling application parameters). The size of the global search space defined by ranges of all applicable parameters is above 524 million combinations, which makes testing all the configurations unacceptably expensive. The authors provide a group of methods which allow to radically reduce the search space by applying certain domain-specific constraints. This allows to prune the search space to over 379 thousand and 965 thousand combinations for ATI Radeon and NVIDIA GPU respectively. Then, the auto-tuning mechanism evaluates all configurations in the search space to select the best configuration corresponding to the shortest execution time.
3.3.3. Auto-tuning Approaches with Combinatorial Search

In many cases when search space pruning is infeasible, approaches alternative to exhaustive search are used, where only chosen combinations of the parameters are evaluated. This section discusses chosen approaches that use such methods, that are called combinatorial search methods.

The Insieme Compiler and Runtime infrastructure\(^2\) has been used in \([30]\) as a test platform for tuning loop tiling in cache-sensitive parallel programs. A combination of compiler and runtime techniques allows tuning parameters of code regions, such as tile sizes, loop ordering and unrolling factors. An optimizer is proposed, which generates multiple application configurations and evaluates them by running the programs on the targeted platform in order to find optimal solutions. However, because the solutions are evaluated by real program executions and the parameter space is large, it is impossible to perform an exhaustive search evaluating all the parameter combinations. To address this problem, a RS-GDE3 search algorithm based on Differential Evolution and rough set theory is proposed.

Approximate optimal values of the application parameters are found by the Generalized Differential Evolution (GDE3) algorithm, which allows to decrease the search time by evaluating each of the configurations from a population in parallel. A search space reduction using the rough sets method proposed in \([153]\) is used to reduce the search space in every iteration of the search algorithm. The solution is evaluated on a case study of a nested loop matrix multiplication application on a target platform employing 10-core Xeon E7-4870 processors. The proposed search algorithm finds similar solutions as an exhaustive brute-force search, but uses from 90% to 99% fewer evaluations.

The Insieme infrastructure and the RS-GDE3 search algorithm have been used for multi-objective optimization of parallel applications also with regard to energy consumption \([103]\). The solution was tested on matrix multiplication and linear algebra applications, stencil codes and n-body simulation executed in a shared-memory system with 8-core Intel Xeon E5-4650 Sandy Bridge EP processor. The proposed algorithm outperformed chosen general-purpose multi-objective optimization algorithms such as hierarchical and random search and NSGA-II \([130]\).

The 8-core Intel Xeon E5-4650 processors were also used for a comparison of the RS-GDE3 search algorithm with mono-objective auto-tuners using local search, simulated annealing, genetic algorithm and NSGA-II based on a n-body simulation application \([104]\). Loop tile sizes, thread numbers and processor clock frequencies were the tunable parameters. These experiments confirmed superiority of RS-GDE3 in the multi-objective setup.

Application-specific parameters have been tuned in \([29]\) to optimize performance of a

\(^2\)http://insieme-compiler.org
GS2 physics application for studying low frequency turbulence in magnetized plasma. Unlike in our work, the considered problem is online tuning, focused on performance variability. The tuned parameters can be changed during the program execution and optimal parameter values can change during the runtime. The PRO (Parallel Rank Ordering) algorithm is proposed as an alternative to the traditional Simplex algorithm, which is claimed to have unpredictable performance in the case of tuning more than one parameter. The proposed algorithm belongs to a class of direct search algorithms known as GSS methods and is resilient to performance variability.

Execution time of large-scale dataset processing applications with Apache Hadoop is optimized by parameter tuning in [97]. Out of more than 130 configuration parameters of the Hadoop MapReduce system, 20 most affecting the system performance have been chosen arbitrarily. These parameters specify the way how the data should be processed in each phase of the MapReduce job execution with regard to parallelism, memory capacity, job flow and data compression. The impact of these features on the application execution time is identified using the random forest feature importance method. Five most influential parameters are chosen for optimization in the experiments.

In the optimization process, the application configuration parameters are repeatedly modified by an optimizer and evaluated by a predictor, a model that predicts median, standard deviation and wave of the application execution time, as described in Section 2.3.4. The optimizer uses the predicted values as input to machine learning ensemble regression methods. The authors assume adequate efficiency of the predictor and solve the black-box optimization problem using the RHC method (combination of Random Sampling and Hill-Climbing). A high dimensional space is used as the feasible set of parameters. In the exploration phase, the parameter space is examined by random sampling to find areas with high probability of approximately optimal parameters. In the exploitation phase, the hill-climbing algorithm is used to search these areas more deeply.

The solution is evaluated on original MapReduce jobs such as TeraSort and WordCount, text processing and hive-aggregation, executed on an 8-node cluster with Intel i7 CPUs. The approximately optimal parameter settings found by the proposed algorithm enable up to 8.8-fold improvement of execution times as compared to the default values of the parameters. The authors claim that this automatic tuning approach is useful in real life setups because it is hard for the system administrators to set the multiple parameters by hand.
4. INVESTIGATED APPLICATIONS AND SYSTEMS

Apart from the literature review in Chapters 2 and 3, the contributions of this thesis are driven by the needs revealed by empirical experiences from developing, executing, simulating and optimizing multiple parallel applications in various HPC systems. Chosen applications that directly served for the experiments and examples provided in this thesis are described in Section 4.1. Chosen HPC systems used for execution of these applications are described in Section 4.2.

4.1. Investigated Hybrid Parallel Applications

In this thesis, big emphasis is put on the practical use of the proposed contributions. For this reason, we aimed to base our experiments on diverse applications that are useful in real life. In this section we describe the applications developed for the sake of this thesis, including MD5 hash breaking in Section 4.1.1, regular expression matching in Section 4.1.2, geostatistical interpolation of air pollution values in Section 4.1.3, large vector similarity measure computation in Section 4.1.4 and training deep neural networks for automatic speech recognition in Section 4.1.5. A description of each application is given, including the specification in what way the application is hybrid.

4.1.1. Multi-level Heterogeneous CPU/GPU MD5 Hash Breaking

The MD5 hash breaking application has been used as a verifying application for the framework for automatic parallelization of computations in heterogeneous HPC systems co-developed by the author of this thesis and described in [13]. The purpose of the application is to retrieve a lost password, given its MD5 hash. The brute-force attack method is used, which means performing the encryption procedure for all passwords from a given range and comparing their hashes to the given one. The application implements the task farming parallel programming paradigm, where the master orders the slaves to search specific subranges of the feasible password space.

In order to ensure fair comparison of execution time for various data partitionings, the application checks all passwords in a given range, whether or not the appropriate password is found. Thus, depending on the assumptions about the possible password length and character set, quite different problem sizes can be achieved, which makes the application useful for execution experiments in systems with various computing powers. For example, employing both CPU and GPU of one "des" workstation from the department laboratory described in Section 4.2.1 it took around 30 seconds to search all passwords up to six characters long, while for passwords up to eight characters long the execution time was much larger - around 4.5 hours. In the context of recovering passwords which often consist of multiple characters, reducing the application execution time would be a crucial improvement of the application.
The application is hybrid in two meanings. First, using the functionality of *KernelHive*, the application can be executed on multiple clusters consisting of multiple nodes equipped with multiple computing devices, which in turn can be parallel on a lower level. This way, the application is hybrid in the multi-level sense. Secondly, due to the implementation in OpenCL and parallelization capabilities of *KernelHive*, the application can be executed on heterogeneous computing devices if they provide an OpenCL runtime. This makes the application hybrid in the sense of computing device heterogeneity.

### 4.1.2. Heterogeneous Regular Expression Matching with Configurable Data Intensity

Optimal configuration for efficient execution of a parallel application strongly depends on the application profile, namely whether it is computationally intensive, requires frequent interprocess communication or if it mostly depends on the input data and how efficiently it can be delivered to the computing device. The idea behind the regular expression matching application proposed by the author of this thesis in [11] was to develop one application that has a different ratio of computational intensity to data intensity depending on the given input data.

The goal of the application is to find all matches of a given regular expression in a given text file. The regular expressions consist of characters which have to appear in the text in the given order and a special character "***" which is a wildcard that matches one or more occurrences of any character. This way, a complex signature of the sought text can be defined. As the application searches the whole given text file regardless of line endings, the computational cost of the search strongly depends on the assumed maximal number of characters matched by the wildcard character, as well as the number of wildcard characters in the signature. Because of this, various application profiles can be achieved, ranging from extremely compute intensive (~431s for searching a 1MiB file) to extremely data intensive (~3s for searching a 512MiB file).

The application is hybrid both in the multi-level and heterogeneous sense, because it is implemented in OpenCL and integrated with the *KernelHive* framework. This allows for testing the influence of the computational/data intensity ratio on the application execution on various computing devices.

### 4.1.3. Multi-level Heterogeneous IDW Interpolation for Air Pollution Analysis

The geostatistical interpolation application investigated within this thesis has been implemented within the master thesis by the author of this dissertation [154] as a part of a module for the SmartCity system designed to support the local government of the city of Gdańsk, Poland. The goal of the module is to provide the user with visualizations of particulate matter air pollution. Preparing the visualizations requires estimating the air pollution level at non-observed locations.
based on real measurements from ten regional monitoring stations, taken in hourly schedule.

The used interpolation method, inverse distance weighting (IDW), derives the interpolated value for each point on the requested area from the real measurement values, normalized proportionally to the distance between the interpolated point and the measured point. To perform the interpolation for one point in time, a basic Python implementation running on one core of the Intel Core i7-4770 processor needed around 36 minutes. Given the hourly measurement schedule, this performance would be enough to render visualizations in real time, however a practical use case was to render visualizations for multiple sets of historical data. Rendering the visualizations for measurements from one year would require around seven months of computations.

For this reason, a massively parallel implementation has been proposed and tested on a single computing device in [154]. In [13] the author of this thesis contributed reducing the execution time of the application by scaling it to a multi-level setup using the proposed KernelHive framework. Being implemented in OpenCL and integrated with the KernelHive framework, the application is hybrid both in the multi-level and heterogeneous sense. Additionally, a hybrid multi-level version using MPI + OpenCL has been contributed by the author of this thesis as a test application in [13].

4.1.4. Multi-level Large Vector Similarity Measure Computation

The application first proposed in [10] for verification of the proposed simulation method is large vector similarity measure computation for big data analysis in a parallel environment. The goal of the application is to compute a similarity matrix for a large set of points in a multidimensional space, assuming that the size of the processed data does not fully fit into the memory. The implementation in C/MPI uses the master-slave parallel programming paradigm, where the master partitions the input data into chunks and distributes them to slaves which compute Euclidean distances between the points in a given chunk.

The implementation that uses MPI allows to spawn slave processes across multiple nodes in a cluster where each process utilizes a single CPU core. Thus, in the case of running multiple processes per node, the application is hybrid in the multi-level sense, because it is parallelized across many nodes in a cluster and many cores within each node. An important parameter of the application that influences its execution time is the number of points in each data chunk. Finding the optimal value of this parameter through comparing times of many real executions could be prohibitively time consuming. For example, computing similarity measures for 2000 points in a space of 200000 dimensions on all 128 virtual cores of 16 "des" workstations (see Section 4.2.1) takes around 8 hours.

The main contribution of the author of this thesis in the paper was developing a model
of the application and conducting the described experiments with simulation of the application. In order to estimate relatively fast the execution times of the application for different problem sizes, application parameters and utilized hardware, a simulation model was proposed. Execution times of the most significant computation and communication operations have been modeled as functions of the data chunk size. The model allows to find the optimal number of points in data chunk. What is more, it can be used to predict execution times while using different, currently unavailable computing resources.

4.1.5. Multi-level Deep Neural Network Training for Automatic Speech Recognition

The deep neural network training application optimized and modeled in the case study described in Section 6.2 of this thesis is a part of the automatic speech recognition (ASR) system developed at the VoiceLab.ai company based in Gdańsk, Poland. One of the crucial elements of the recipe based on the Kaldi toolkit [155] is the acoustic model implemented as an artificial neural network. The goal of the acoustic model is to classify each audio frame in a given recording to one of the possible speech units called phonemes. The input of the network for each frame is a set of its features, in this case 13 mel-frequency cepstral coefficients (MFCC).

The specific application considered in this thesis is parallel neural network training with natural gradient and parameter averaging [156] using chosen 100 hours from the internal Voice-Lab.ai corpora consisting of over 4200 hours of Polish speech from about 5700 speakers. The model is a recurrent neural network constructed from 4 layers of long short-term memory (LSTM) cells. The training consists of iterations of backpropagation algorithm performed by multiple GPUs on separate copies of the model on different training data chunks and averaging the model weights at the end of each iteration. One training epoch consists of such a number of iterations that all training examples are used. In a usual training procedure, 15 training epochs are executed, which on two workstations, cuda5 and cuda6 from the VoiceLab.ai cluster (see Section 4.2.5) takes over 11 hours. Developing an efficient acoustic model requires testing many neural network architectures trained with multiple values of training parameters and thus, running many instances of the training. Execution time reduction would be a crucial improvement of the application.

The training can utilize GPUs from multiple computing nodes in a cluster, which makes the application multi-level. It is also heterogeneous, because the backpropagation algorithm is executed on GPUs, while data preprocessing and model averaging are executed on a CPU. What is more, the capability of the application to efficiently utilize different GPU models is often a practical requirement. Clusters used by companies are regularly upgraded with new, more powerful computing devices and proper load balancing is required to make the most of the whole cluster without inefficiencies resulting from lower speed of the older devices.
4.2. Investigated HPC Systems

Similarly to the applications described in Section 4.1, we aimed to base our experiments on many diverse high performance computing systems. In this section we describe chosen utilized systems, including a collection of laboratory workstations with GPUs in Section 4.2.1, a collection of servers with computing accelerators in Section 4.2.2, a cluster with 864 CPU cores in Section 4.2.3, a pilot laboratory for massively parallel systems in Section 4.2.4 and a professional cluster of workstations with GPUs in Section 4.2.5.

4.2.1. Des - Department Laboratory Workstations

"Des" workstations are machines available in the high performance computing and artificial intelligence laboratory located at the Department of Computer Architecture - home department of the author of this thesis. Although the main purpose of the laboratory is engaging students in classes concerning parallel algorithms, high performance computing systems and massively parallel processing, in certain reserved time windows it can also be used for experiments involving the heterogeneous hardware resources of the laboratory. In particular, the 18 laboratory machines called "des01-18", equipped with an Intel i7-2600K CPU with 8 logical cores and 8GB of RAM each can be utilized as a heterogeneous computing cluster, because all nodes have also NVIDIA GeForce GTS 450 GPUs with 192 CUDA cores installed, except for one node with NVIDIA GeForce GTX 480 with 480 CUDA cores.

4.2.2. Apl - Department Computing Accelerator Servers

The computing resources available at the Department of Computer Architecture include also four servers called "apl09-12" with high performance CPUs and computing accelerators. Apl09 and apl10 are equipped with Intel Xeon W3540 CPU with 8 logical cores, 12 GB of RAM and GPUs: NVIDIA Tesla C2050 and NVIDIA GeForce GTX 560 Ti, both with 448 CUDA cores. Apl09 is also equipped with a NVIDIA Quadro FX 3800 GPU with 192 CUDA cores. Apl11 is a server with two Intel Xeon E5-2680 v2 CPUs with 12 logical cores each, 64GB of RAM and two Tesla K20m GPUs with 2496 CUDA cores each. Apl12 is a server with two Intel Xeon E5-2680 v2 CPUs with 20 logical cores each and two Intel Xeon Phi 5100 accelerators with 240 logical cores each. Despite fast aging of equipment, especially the GPUs, regular upgrades of the apl high performance computing server infrastructure makes it a good experiment environment, particularly in the context of efficient utilization of heterogeneous computing infrastructure by a single application.
4.2.3. **K2 - Department High Performance Computing Cluster**

The Department of Computer Architecture maintains also K2, a high performance computing cluster consisting of 3 racks of 36 nodes each. Each node is equipped with two Intel Xeon E5345 4-core CPUs and 8GB of RAM, giving a total of 864 CPU cores. The nodes are connected with an InfiniBand interconnect supported by Mellanox Technologies MT25204 network cards. The cluster is particularly useful for applications that can scale to hundreds of cores, such as the IDW interpolation application described in Section 4.1.3.

4.2.4. **MICLAB - Pilot Laboratory for Massively Parallel Systems**

MICLAB is a laboratory at the Institute of Computer and Information Sciences of the Technical University of Czestochowa, built within the project "Pilot laboratory for massively parallel systems". The aim of the project is to create a virtual laboratory, where the nationwide scientific community can investigate the usage possibilities and define application directions of contemporary massively parallel computing architectures in leading fields of science.

The computing infrastructure of the laboratory consists of 10 high performance computing nodes. Eight of them are equipped with two Intel Xeon E5-2699 v3 CPUs and 256 GB of RAM each. The processors have 36 logical cores each, but the significant computing power lies also in the Intel Xeon Phi 7120P coprocessors with 244 logical cores each. Two such coprocessors are installed in the eight latter nodes, and also in two other nodes, each equipped with two Intel Xeon E5-2695 v2 CPU with 24 logical cores each and 128 GB of RAM. The two remaining nodes are also equipped with two Intel Xeon E5-2695 v2 CPUs and 128 GB of RAM, but in their case the installed computing accelerators are two NVIDIA Tesla K80 GPUs with 4992 CUDA cores each.

4.2.5. **Cuda567 - Professional Workstations With GPUs**

The professional high performance computing infrastructure at the VoiceLab.ai company is dedicated to deep neural network training applications, such as the one described in Section 4.1.5. The computing power for deep learning is based mostly on GPUs, which are commonly used accelerators for this purpose. Cuda567 is a subset of the infrastructure, consisting of three nodes, each with 4 NVIDIA GeForce GTX Titan X GPUs with 3072 CUDA cores. The first node, cuda5 is equipped with two Intel Xeon E5-2620 v3 CPUs with 12 logical cores each and 128GB of RAM. The two other nodes, cuda6 and cuda7 are also equipped with 128GB of RAM, but stronger CPUs: two Intel Xeon E5-4650 v2 CPUs with 20 logical cores each.
5. PROPOSED OPTIMIZATION METHODOLOGY

The main contributions of this thesis result from the analysis of applications, systems and optimizations described in Chapters 2 and 3, as well as multiple experiments involving real executions of hybrid parallel applications on heterogeneous HPC systems. Selected applications and systems, described in Chapter 4 were used for the experiments described in Chapter 6 and motivations provided in Chapter 1. Based on the literature analysis and experiments, a general optimization methodology for executing hybrid parallel applications in heterogeneous HPC systems has been developed, that focuses on execution time and power consumption of the applications. The proposed optimization methodology consists of execution steps described in Section 5.1 and a simulation procedure proposed in Section 5.2 as a method for accomplishing two of the execution steps.

5.1. Execution Steps

The following steps related to Claim 1 of this thesis are proposed to optimize the execution of a hybrid parallel application:

1. preliminary process optimization - if possible, modification of the implementations of parallel processes \( p \in \Phi_A \), in such a way that the result of the application remains valid, but the sequence of operations is changed in order to reduce the process execution time;
2. application execution optimization:
   (a) process mapping - finding the process mapping function \( m \in M_{A,S} \);
   (b) parameter tuning - finding the vector of application execution parameters \( \mathbf{v} \in V_{A,S} \);
3. actual execution.

The first step has been included in the proposed execution steps in order to stress the importance of profiling and performance analysis of the application. In many practical situations, the most significant reduction of application execution time can be achieved through relatively straightforward modifications of the parallel algorithm that result for example in overlapping of certain operations or more efficient sequence of operations in terms of memory performance (e.g. loop tiling [157] or avoiding false sharing [158]). An analysis should be performed to determine the most time consuming parts of the application and identify the corresponding utilized hardware resources. If two consecutive operations require different hardware elements (for example a computing device and a network device), often an overlapping technique allows to perform these operations simultaneously. This step is particularly useful in cases of hybrid parallel applications where different hardware elements can be specialized for certain types of tasks, for example a CPU for handling I/O operations and a computing accelerator for massively parallel computations.
Step 2a is connected with the global static task mapping problem described in Section 3.2. Step 2b is connected with the offline auto-tuning of system parameters problem described in Section 3.3.

Steps 1, 2a or 2b may be omitted. For certain applications introducing preliminary process optimization may be infeasible. Similarly, there might be only one feasible process mapping or value of certain application execution parameters. The appropriate choice of performed execution steps may differ throughout applications and systems. If at all, the preliminary process optimization step should be performed as the first one, because the optimal process mappings and application execution parameters depend on the exact process implementations. They might also depend on each other, hence Steps 2a and 2b could be performed repeatedly in turns or performed simultaneously.

Although the last of the proposed steps, actual execution, may seem obvious and straightforward, performing it might require significant technical effort, especially in multi-level and heterogeneous systems. Dozens of software frameworks and programming interfaces are used for execution of parallel applications, depending on the target system, application characteristics and field, used programming language etc. In a multi-level heterogeneous system, a software solution is required that allows execution of the application on various types of computing devices available in the system, as well as communication through a hierarchical network infrastructure. Chosen software solutions for executing parallel applications in multi-level heterogeneous HPC systems have been described in Section 2.2.3. Many of them are mixing different APIs in one solution, which requires know-how and specialized programming effort.

In order to perform all proposed steps using one, easy to use software environment, we propose using KernelHive, a framework for parallelization of computations in multi-level heterogeneous HPC systems first introduced in the master thesis [159] by the author of this dissertation, available as free software\(^3\). The system allows parallelization of applications among clusters and workstations with CPUs and GPUs. KernelHive applications are developed using a graphical tool hive-gui by constructing a dataflow graph and implementing computational kernels assigned to the graph nodes. Custom graph nodes can be developed by implementing the IDataProcessor kernel interface, and a library of sample implementations and templates is provided. Automatic parallelization is possible through an unrollable node mechanism illustrated by Figure 5.1, where apart from a data IDataProcessor kernel, two other kernels are defined for the node: IDataPartitioner responsible for dividing the problem into a given number of subproblems and IDataMerger responsible for merging the results of multiple tasks solving these subproblems. This way, any application that implements the IDataPartitioner, IDataProcessor and IDataMerger kernels can

\(^3\)https://github.com/roscisz/KernelHive
be automatically parallelized to a given number of computing devices.

Task mapping and allocation, data transfer and automatic parallelization through the *unrollable nodes* is performed under the hood, allowing programmers to benefit from parallel execution while focusing only on the application rather than the complicated parallelization internals. Details about the available infrastructure along with application progress can be monitored in a graphical tool [18]. Overview of the architecture of the KernelHive system is presented in Figure 5.2.

The components of the framework are arranged in a hierarchical structure corresponding to the used computing system. An example of such a hierarchy can be seen in Figure 6.2. The central component is the *Engine* which interacts via a Simple Object Access Protocol (SOAP) interface with the computing nodes through instances of the *Cluster* component, part of the Cluster and node management layer implemented as Java system daemons installed in access
nodes to particular clusters available in the system. The Cluster instances interact via a Transmission Control Protocol (TCP) interface with the underlying Unit component instances, running as C++ system daemons in each available computing node. Using this hierarchical architecture, the framework is able to discover available computing devices in all connected nodes. Data about the currently available computing devices, their hierarchy and state is gathered in an object-oriented data structure in the central Engine subsystem.

The proposed hierarchical framework architecture allows to take various characteristics of the system into account during optimization of the execution and, what is more, setting and auto-tuning various application execution parameters concerning different levels of the computing system. Technically, the optimization is done using a mechanism of interchangeable Optimizers focused on different goals, such as optimization of execution time, power consumption or application reliability. The user of the framework can develop and plug in a new Optimizer corresponding to their needs, but choosing from the available implementations or mixing them is also possible.

The essential processing in the KernelHive framework is performed by tasks implemented as OpenCL kernels. The process responsible for running consecutive tasks is unit, a subsystem of KernelHive running as a system daemon on a given node. Tasks in KernelHive are orchestrated by the engine subsystem, the central module of KernelHive, which supports submitting multiple applications for execution. The applications are represented as DAG which nodes represent computing tasks and edges represent data flow. The Engine keeps track of the current state of each application, in particular which tasks have already been completed and for which the input data is already gathered so they are ready for execution. An interchangeable optimizer interface allows plugging in different scheduling implementations that periodically analyze the set of jobs ready for execution and decide which ones should be executed next and on which available computing devices, according to a given optimization strategy.

An improved and tested version of KernelHive has been described in [13] along with a specific execution methodology consisting of the following steps:

- selection of computing devices;
- determination of best grid configurations for particular compute devices;
- determination of the preferred data partitioning and granularity;
- actual execution.

The execution steps proposed in this thesis is a more general version of the latter, extended with Step 1, preliminary process optimization. Step 2a, process mapping is a broader term for selection of computing devices while Step 2b, parameter tuning includes determination of both grid configurations (one of the possible execution parameters) and data partitioning (one of the possible application parameters). The actual execution step remains unchanged.
5.2. Modeling and Simulation for Fast Evaluation of Execution Configurations

As noted in Section 5.1, steps 2a (process mapping) and 2b (parameter tuning) could be performed simultaneously. In fact, these two steps represent solving the optimization problem defined in Equation 1.1 in Section 1.2 when the process implementations $\Phi_A$ are already optimized and will not be changed any more. Chosen solutions to similar optimization problems are discussed in Chapter 3. Different methods can be suitable for this task depending on the size of the search space and cost of evaluating each solution. If both the search space and the cost of solution evaluation are small, exhaustive search can be used, which guarantees finding a global optimum, because it consists of systematic evaluation of every possible alternative. In all other cases we propose using simulation method for fast solution evaluation.

In the cases of small search space but high cost of solution evaluation or small cost of solution evaluation but big search space without possibility of space pruning, combinatorial search methods could be used, such as local search, simulated annealing or evolutionary algorithms which do not guarantee finding neither a local nor global optimum. Availability of an accurate enough simulation method would allow to still perform exhaustive search. In extreme cases of prohibitively big search spaces and high costs of solution evaluation, such a simulation method could also be useful as a fast evaluation method for combinatorial search algorithms. In this Section we propose a simulation for these purposes, related to Claim 2 of this Thesis.

Searching for a suitable simulation tool, in [21] we reviewed chosen existing parallel application simulators and provided motivations for developing a new discrete-event simulator of parallel application execution on large-scale distributed systems. MERPSYS, the simulation environment proposed in [14] allows to accurately predict execution time and power consumption of parallel applications and analyze the power/time trade-off by performing the following steps:

1. preparing the application model $A = (\Phi_A, \vec{r}_{min}^A, \vec{r}_{max}^A)$ by defining:
   - the process implementations $\Phi_A$ using the Editor graphical tool for writing code in a Java-based meta-language which provides API for modeling various types of computation and communication operations. This requires identifying the crucial operations and thus deciding on the granularity of the model by analyzing code of an existing application or providing them from scratch. The granularity level should allow to define the modeling functions described in point 3;
   - process requirements $\vec{r}_{min}^A, \vec{r}_{max}^A$ by inserting their values into a form;
2. preparing the system model $S(D_S, L_S)$ by using the Editor graphical tool for building the hardware graph from computing devices and network links available in a database;
3. defining hardware capabilities $c$ by inserting values for each process into a form available after selecting a certain device in the Editor;
4. defining certain modeling functions using a Web application for filling in JavaScript snippets that have access to computing device characteristics and operation parameters. The functions may be based on analytical performance and power consumption models. If possible, we suggest tuning these functions using results of real application executions. The following modeling functions are required by the proposed simulator:

- \( \text{comptime}(\theta, d) \) - execution time of a computation operation \( \theta \) using a computing device \( d \);
- \( \text{commtime}(\kappa, l) \) - execution time of a communication operation \( \kappa \) using a network link \( l \);
- \( \text{pcidle}(d) \) - idle power consumption of a computing device \( d \);
- \( \text{pcpeak}(d) \) - peak power consumption of a computing device \( d \).

Additionally, a hardware parameter \( n\text{cores}(d) \) is required, which denotes the number of cores of a computing device \( d \).

5. simulating the application execution and analysis of the resultant values of execution time \( ET(A, S, m, \vec{v}) \) and average power consumption \( PC(A, S, m, \vec{v}) \) through:

- providing a scheduling mechanism which defines the process mapping function \( m \)
  by choosing or writing an implementation of a Scheduler programming interface;
- using the Editor graphical tool for choosing specific values of application execution parameters \( \vec{v} \), enqueuing a single simulation instance and analyzing its results;
- running one or more instances of the Simulator program which would execute in parallel all simulation instances enqueued in the simulation queue;
- using the Web interface for enqueuing an optimizer suite - an automatically populated set of simulation instances based on the previously executed single simulation instance, with a range of varying values of certain application execution parameters \( \vec{v} \) and, thus, defining the space of application execution parameters \( V_{A,S} \);
- using a ParetoVisualizer tool for viewing a chart of results for all simulation instances in a suite with execution time and power consumption as axes, indicated set of Pareto-optimal solutions and values of the varying application execution parameters accessible by hovering over a data point.

The proposed simulation environment performs a discrete-event simulation that runs the application model codes of all defined processes and increases appropriate execution time and energy consumption counters for all computation and communication operations. It should be noted that, in the case of communication operations, the simulator ensures proper synchronization.
between the processes, so that for each process, possible waiting for another process is included in the execution time of the operation. The execution time of a process is modeled as the sum of the execution times of all computation and communication operations:

\[ et(p, d) = \sum_{i: p_i \in \Theta} \text{comptime}(p_i, d) + \sum_{i: p_i \in K} \text{commtime}(p_i, d) \]  

(5.1)

Hence, considering Definition 12, the execution time of the whole application is modeled as:

\[ ET(A, S, m, \vec{v}) = \max_{p \in \Phi} \left( \max_{d \in D_S: m(d, p) > 0} \left( \sum_{i: p_i \in \Theta} \text{comptime}(p_i, d) + \sum_{i: p_i \in K} \text{commtime}(p_i, d) \right) \right) \]  

(5.2)

The average power consumption of the application is computed as sum of idle power consumptions of all devices in the system plus all additional energy consumption caused by the computation operations of the application divided by the total application execution time, computed as the execution time of the operation multiplied by the power consumption of the used device at the time \( t_p \) of execution of the operation \( p \) \((\text{poperation}(d, t_p))\):

\[ PC(A, S, m, \vec{v}) = \sum_{d \in D_S} \text{pcidle}(d) + \frac{\sum_{d \in D_S} \left( \sum_{p \in \Phi: m(d, p) > 0} \left( \sum_{i: p_i \in \Theta} \text{comptime}(p_i, d) \cdot \text{poperation}(d, t_p) \right) \right)}{ET(A, S, m, \vec{v})} \]  

(5.3)

The simulator keeps track of the number of operations running on each computing device at each time throughout the application execution \((\text{activeoperations}(d, t))\). This allows to simulate the power consumption of the device at a given moment of execution as a value between the idle level \( \text{pcidle} \) and the peak level \( \text{pcpeak} \), proportionally to the number of cores used by the operations, but not exceeding the number of available cores:

\[ \text{poperation}(d, t) = \min \left( \frac{\text{activeoperations}(d, t)}{\text{ncores}(d)}, 1 \right) \cdot \left( \text{pcpeak}(d) - \text{pcidle}(d) \right) \]  

(5.4)

This way, the power consumption estimation takes into account that the computing device can be utilized by multiple processes. It should be noted that the simulator allows also to implement a non-linear increase of power consumption until a saturation point, as proposed in [160].

The novelty of the proposed simulation method is that it combines mathematical modeling (at the granularity level for which it is feasible) with discrete-event simulation at the level of parallel processes for which operation sequences and synchronization with other processes are difficult to model analytically. Additionally, the contributions of the author of this thesis include experiments
with modeling execution of various applications.

In [10] we provided an example of developing and tuning an application model in MERPSYS based on the large vector similarity measure computation application described in Section 4.1.4. The proposed simulator allowed to predict the shapes of time curves beyond the area where empirical results could be obtained. In [12] we provided examples of energy consumption modeling based on two types of parallel applications: geometric SPMD and DaC. Experiments of running up to 512 and 1024 processes of the two applications respectively, on a large cluster from Academic Computer Center in Gdańsk, demonstrated high degree of accuracy between simulated and measured results.

The web application included in the MERPSYS simulation environment allows to define suites of simulations through providing ranges of selected parameters, so that multiple simulation instances with different values of these parameters are created automatically. A distributed simulation framework contributed by the author of this thesis in [20] whose architecture is presented in Figure 5.3 provides two ways of handling such simulation suites. In the first one, all simulation instances in the suite are enqueued to a simulation queue and processed by distributed simulators. The results of the simulations can be browsed in the web application afterwards. This way, exhaustive search of parameter space can be performed.

Fig. 5.3. Architecture of the distributed simulation framework [20] in MERPSYS
The second way of handling the simulation suites involves an Optimizer component. The MERPSYS environment provides a $SimulationOptimizern$ programming interface whose implementations have access to the parameter search space and can adopt various strategies of evaluating simulation instances in the suite. The input for such an optimizer is a $SimulationTask$ that includes the application model, system model, feasible combinations of application execution variables and process mapping constraints. This allows the Optimizer implementations to enqueue selected groups of simulation instances in iterations, where results of the instances selected in the previous iteration can be used to select new candidates, until the optimizer algorithm decides that a suboptimal approximate solution has been found. This way, combinatorial search methods can be used for application optimization. The architecture allows also to develop custom optimization tools, for example the ParetoVisualizer contributed by the author of this thesis in [16] which, instead of iterative evaluation, performs exhaustive search and provides visualization of the found set of optimal solutions.
6. EMPIRICAL EVALUATION OF THE PROPOSED METHODOLOGY

In this Chapter we describe case studies of using the methodology proposed in Chapter 5 to optimize execution of specific hybrid parallel applications in specific heterogeneous HPC systems. In Section 6.1 we describe examples of applying the individual execution steps to independent cases of multi-level task farming applications. Section 6.2 describes a case study of applying the proposed optimization methodology as a whole to optimize one deep neural network training application executed on a professional cluster of workstations with GPUs. The aim of these case studies is empirical evaluation of the proposed methodology. Table 6.1 lists the specific actions that were performed within the proposed execution steps.

**Table 6.1. Action selection for particular execution steps for the considered case studies**

| Step                          | Individual steps                                         | Full Case Study                        |
|-------------------------------|----------------------------------------------------------|----------------------------------------|
| 1. Preliminary process        | Computation and communication overlapping                | GPU training and CPU data pre-processing overlapping |
| optimization                  |                                                          |                                        |
| 2a. Process mapping           | Network-aware and Power Constrained Scheduling           | Exploring the front of Pareto-optimal solutions using the proposed simulation environment |
| 2b. Parameter tuning          | Tuning data partitioning and grid configurations         |                                        |
| 3. Actual execution           | Execution in KernelHive                                  | Execution using MPI and Kaldi          |

As indicated in the table, method of simulation for evaluating process mappings and application execution parameters proposed in Section 5.2 has been used in the full case study within the combined process mapping and parameter tuning steps.

6.1. Multi-level Task Farming on Heterogeneous Systems with CPUs and GPUs

On the example of multi-level task farming applications, the case studies described in this section show how all execution steps proposed in this thesis can be performed using the KernelHive framework and address Claim 1 of this thesis by proving the significance of these steps. In the preliminary process optimization step, a data prefetching optimization is proposed that results in overlapping of computations and communications, as described in Section 6.1.1. Example of the process mapping step, namely network-aware and power constrained scheduling are described in Section 6.1.2. Tuning of GPU grid configurations and data partitioning within the parameter tuning step is described in Section 6.1.3. Finally, the step of actual application execution using the KernelHive framework is described in Section 6.1.4.

6.1.1. Preliminary Process Optimization - Computation and Communication Overlapping

In the first of the execution steps proposed in this thesis, preliminary process optimization, overlapping of certain operations can be implemented. This requires analyzing the operations of the processes in the application at a chosen granularity level and searching for the possibility
of overlapping certain operations that use different hardware. In this section we provide such an
analysis for the regular expression matching application described in Section 4.1.2, implemented
in the KernelHive framework and we describe the proposed modification that allows overlapping
of certain communication and computation operations.

In the basic version of the application, the default Optimizer implementation is used that,
in each iteration of application workflow processing, schedules the jobs ready for execution to
devices available in the system in a round-robin fashion. In terms of processes and operations,
this means that the engine process \( p^{\text{engine}} \in \Phi_A \) that runs on the central node \( d^{\text{engine}} \) consists of
iterations of the following communication operations: ordering the appropriate unit subsystem to
execute a next available task and receiving the ID of the computation result package afterwards.

For each task, the sequence of operations of the unit process resulting from its process
implementation \( p^{\text{unit}} \in \Phi_A \) is as follows:

1. \textit{communication} operation that downloads input data from a given database;
2. \textit{computation} operation that is execution of a given task kernel on a given target device;
3. \textit{communication} operation that uploads the resulting output data to a given database;
4. \textit{communication} operation that reports the ID assigned to the output data to the engine.

Depending on the computationally intensive, data intensive or communication intensive
profile of the specific application, different operations of the unit process can have significant exe-
cution time. Profiling of a moderately data intensive configuration of the regular expression match-
ing application described in Section 4.1.2 executed in a multi-level HPC system revealed that the
most costly operations are the two first ones. Since they require different hardware elements (a
chosen computing device and a network interconnect), the operations could be potentially over-
lapped if only in the application there were multiple tasks without mutual data dependencies.

This is the case in the considered application, which gives the motivation for the overlap-
ping optimization contributed by the author of this thesis in [161]. The optimization benefits from
the feature of KernelHive, that multiple databases can be used for storing the input, output and
partial data packages. In terms of the notation proposed in Section 1.2, the optimization modifies
the process implementations belonging to the application \( \Phi_A \) by introducing a modified imple-
mentation of the \( p^{\text{engine}} \) process - \( p^{\text{engine}} \in \Phi_A \) and a new supporting process \( p^{\text{prefetching}} \in \Phi_A \).
The architecture of the proposed prefetching scheme is shown in Figure 6.1. Apart from the main
database, accessible by the unit processes through a network interconnect, one locally installed
database per each unit has been used. The unit process remained unchanged, but an additional
prefetching process has been defined, executed by another subsystem, cluster placed on the
cluster access node \( d^{\text{cluster}} \), which is an entry point for accessing the units that are in a local
network, possibly not directly visible by the engine. The \( p^{\text{prefetching}} \) process executes the following
communication operations:

1. downloading input data from the main database;
2. uploading the data to a given local database;
3. reporting the ID of the prefetched data package to the engine.

In order to utilize this prefetching mechanism, a new Optimizer has been developed for the engine, which changes the sequence of communication operations. For each selected computing device, at the beginning of the sequence resulting from the modified process $p_{\text{engine}} \in \Phi_A$, there is an operation of ordering the appropriate cluster to execute a prefetching job related to the next
available task. Then, the following operations are performed in each iteration:

1. receiving the ID of the prefetched data package from the appropriate cluster;
2. ordering the appropriate cluster to execute a prefetching job for a next available task;
3. ordering the appropriate unit to execute the task for which data has been prefetched;
4. receiving the ID of the computation result package.

As a result, the first operation in the unit process downloads the input data directly from the local database, which reduces the operation execution time. Assuming that the main database is installed on device \( d_{\text{main}} \in D_S \) and the unit subsystems with their local databases are running on devices \( d_{\text{unit}} \in D_S \), apart from data intensity of the application, the benefit from the proposed optimization depends on the properties of the network link \( l_{\text{main},\text{unit}} \in L_S \) between these devices, which depends on the heterogeneous HPC system graph \( S(D_S, L_S) \). The gain from the proposed optimization depends also on the number of tasks in the application and thus the number of iterations.

The experiments described in [161] involved executing the application on a heterogeneous cluster consisting of apl09 and apl10 servers described in Section 4.2.2 and a remote machine was used as the device \( d_{\text{main}} \). In the case of one iteration the difference in execution time was negligible, because in fact no overlapping occurred. However, for higher iteration numbers the gain from the optimization ranged from around 11% to 16%. These results prove that the preliminary process optimization step included in Claim 1 of this dissertation allows to significantly reduce execution time of the optimized application.

6.1.2. Process Mapping - Network-aware and Power Constrained Scheduling

Apart from preliminary process optimization described in the previous Section, the topology of the HPC system resulting from the heterogeneous HPC system graph \( S(D_S, L_S) \) can be also taken into account in the process mapping execution step. For example, a network-aware scheduling scheme for a KernelHive optimizer proposed in [17] schedules the tasks equally between the clusters, understood as sets of nodes connected by a local area network. Reported simulation results show that such an approach can significantly reduce total execution time of the application, provided that only a subset of computing devices available in the system are used for computations.

Utilizing only a subset of devices available in a HPC system is a common case. This is often caused by limited scalability of the application, when there is an optimal number of subtasks into the computations could be divided and further division results in reduced efficiency. Another reason for using only a subset of available devices is an imposed power consumption limit. Solving the problem of execution time optimization under power consumption constraints, defined in
Equation 1.2 in Section 1.2 requires optimal selection of the computing devices subset within the process mapping \( m \in M_{A,S} \), so that their total maximum power consumption does not exceed a given limit \( PCL \).

In [19] we formulated this selection problem as a 0/1 knapsack problem (given power consumption levels and performance of \( |D_S| \) devices, put these items in a knapsack of capacity \( PCL \)).

The aim of the experiments was to minimize the execution time of the task farming application for password breaking described in Section 4.1.1 under different values of imposed power limit in a heterogeneous system combined from the computing infrastructure described in Sections 4.2.1 and 4.2.2, presented in Figure 6.2. The paper shows how a greedy solution to the knapsack problem can be deployed in a real framework able to parallelize computations in a multi-level heterogeneous computing infrastructure.

![Fig. 6.2. Heterogeneous computing system used in the experiments with imposed power limits](image)

One of the challenges of this approach was the ability to dynamically divide the computa-
tions into a number of subtasks which could change at application runtime. In order to meet this challenge, the *unrollable node* functionality of *KernelHive* has been used. The application was represented as a dataflow graph with a single node implementing the *unrollable node* mechanism. The *partitioner* kernel implemented division of the range of examined passwords and the *merger* implemented checking if the password has been broken in any task. Our approach is similar to the "moldable jobs" concept discussed in [95], where "the user specifies the range of nodes (the minimum and the maximum number of nodes) on which the job can run. The job scheduler decides the number of nodes within the specified range to be allocated to the job". It should be noted that apart from the *process mapping* function $m$, during the process of computing device selection, also an *execution parameter* is modified, namely the number of running tasks. This is an example how in some situations the *process mapping* and *parameter tuning* steps have to be performed simultaneously.

![Comparison of execution times under power limits with theoretical ideal values](image)

**Fig. 6.3.** Comparison of execution times under power limits with theoretical ideal values

For the sake of the experiments described in [19], maximum power consumption of each used device model when running the application has been measured using a hardware power meter. The application has been executed on a heterogeneous computing system consisting of eight "des" nodes described in Section 4.2.1 (seven with a GTS450 GPU and one with a GT4X80 GPU) and "apl09" server described in Section 4.2.2. Real execution times of the application under varying power consumption limits have been compared to the theoretical ideal execution times based on relative performance of the used devices. The comparison of execution times is shown in Figure 6.3.

Although the shapes of the real and ideal curves are similar, the higher power limit, the bigger the difference between them. The reason for this is that the ideal curve does not consider
Fig. 6.4. Speedup comparison of real executions under power limits with theoretical and simulated values
communication and scheduling overheads which occur in real executions. In order to better explain the real execution results, the speedups were compared also with the values resulting from simulations that reflected the key dependencies by taking into account the scheduling and communication overheads. The speedup comparison in Figure 6.4 shows that the proposed process mapping method allows to achieve nearly ideal speedups of the application under a strict power consumption constraint. This proves that the process mapping step included in Claim 1 of this dissertation allows to optimize the execution time of the considered application.

6.1.3. Parameter Tuning - Grid Configurations and Data Partitioning

One of the advantages of using the KernelHive framework for executing parallel applications is the possibility to dynamically tune the values of certain application execution parameters depending on the specific executed computational kernel or the specific device used for the computations. For example, the GPU grid configuration execution parameters described in Section 2.2.1 including the total number of threads $v_{\text{threadstotal}}$ and number of threads per block $v_{\text{threadsblock}}$ can be fixed using an appropriate form in the hive-gui user interface or programmed in the engine subsystem to take into account the used device model and determine the best configuration by probing chosen values. The latter approach has been used in [13] for the password breaking application described in Section 4.1.1. In terms of the notation proposed in Section 1.2, the problem solved in this case study can be expressed as follows:

$$\min_{\vec{v}} \ ET(A, S, m, \vec{v})$$

subject to $\vec{v} = [v_{\text{threadstotal}} \in T, v_{\text{threadsblock}} \in B]$. (6.1)
where $T$ is the set of feasible total numbers of threads and $B$ is the set of feasible block sizes.

Comparison of execution times of searching through $10^9$ hashes depending on grid configurations is presented in Figure 6.5 for GeForce GTX 480 GPU, Figure 6.6 for GeForce GTS 450 GPU and Figure 6.7 for Tesla C2050 GPU.

![Fig. 6.5. Execution time depending on grid configurations for GeForce GTX 480](image)

The comparison shows that setting the appropriate values of execution parameters can have a great impact on the application execution time and what is more, optimal values of one parameter can depend on the selected value of another parameter. Setting too low number of $v_{\text{threadsblock}}$ (64) results in significantly longer execution time for all analyzed computing devices. For example, for the GeForce GTS 450 GPU it results in execution time of roughly 5.5s compared to roughly 3.5s in the case of optimal setting. However, increasing this number above a certain
value also increases the execution time. The value of $v_{\text{threadsblock}}$ chosen in the parameter tuning step for the analyzed application on each analyzed device is 128. Regarding the $v_{\text{threadstotal}}$ parameter, increasing it to a certain value results in a significant speedup. While GTS 450 is able to maintain a constant performance with more threads, GTX 480 and Tesla C2050 have difficulties with scheduling the threads, resulting in peaks in execution time. To avoid such problems, the value of $v_{\text{threadstotal}}$ chosen in the parameter tuning step for all devices was 32,768.

Apart from execution parameters, also certain application parameters can be tuned using KernelHive. Let the application execution parameter $v_{\text{nnodes}} \in \mathbb{N}$ denote the number of nodes used by the application. In task farming applications executed in heterogeneous computing systems, there often occurs a load imbalance resulting from differing speeds of the used computing devices. For example, if the computational problem is divided into a number of subproblems equal to the number of nodes $v_{\text{nnodes}}$, the time of computing the resulting single task on the slowest used device determines the total application execution time. All the faster devices are idle while waiting for the slowest device to finish, which makes the execution inefficient.

A common way to address this problem is to divide the computational problem to a higher number of smaller subproblems, so that the execution time on the slowest device is reduced, and the faster devices can be dynamically loaded with consecutive tasks. The higher performance differences across the devices in $D_S$, the more tasks are needed to ensure proper load balancing. On the other hand, increasing the number of tasks comes at a cost of additional communication overheads for distributing the tasks. In the parameter tuning step, the optimal number of tasks should be determined for the specific application and utilized system. In KernelHive, the number of tasks can be dynamically set thanks to the unrollable node mechanism described in Section

Fig. 6.7. Execution time depending on grid configurations for Tesla C2050
6.1.2. For the considered task farming applications, the number of subproblems is derived from the number of utilized devices multiplied by a *application parameter* \( \nu_{dpm} \in \mathbb{N} \) called *data package multiplier*. In terms of the notation proposed in Section 1.2, finding the optimal number of used *computing devices* and value of the *data package multiplier* can be expressed as follows:

\[
\min_{\bar{\nu}} \quad \operatorname{ET}(A, S, m, \bar{\nu}) \\
\text{subject to} \quad \bar{\nu} = [\nu_{nodes} \in \mathbb{N}, \nu_{dpm} \in \mathbb{N}].
\] (6.2)

The influence of the \( \nu_{dpm} \) parameter on the execution time of the password breaking application described in Section 4.1.1, searching through \( 5 \times 10^{12} \) hashes is shown in Figure 6.8. The application has been executed on a system consisting of \( \nu_{nodes} = 16 \) "des" nodes described in Section 4.2.1, each consisting of an Intel i7-2600K CPU and a NVIDIA GeForce GTS 450 GPU.

![Fig. 6.8. Influence of the package number multiplier \( \nu_{dpm} \) on the real application execution time](image)

The figure shows how significant the influence of a single *application parameter* can be on the application execution time. While there is a point of optimal load balancing with \( \nu_{dpm} \) equal to 18, increasing it only to 19 ruins the load balancing and results in nearly two-fold increase of the execution time. Such "steps" in the chart are periodic and result from imbalance of processing times between CPUs and GPUs. Because for this application the CPUs are less efficient than the GPUs, for some numbers of packets the GPUs are idle waiting for the CPUs to finish previously ordered data packets. The height of the consecutive "steps" in the chart is decreasing, because higher number of data packets also means that they are smaller, hence smaller differences between processing times of CPUs and GPUs. On the other hand, the local minima before the "steps" are increasing, because high numbers of data packets introduce additional communi-
cation overheads of packet transfers. Based on results of simulations that take into account these overheads, for the same application, Figure 6.9 shows how the shape of the "steps" changes depending on the number of used nodes $n_{nodes}$.

![Simulated execution time](image)

Fig. 6.9. Influence of the package number multiplier $dpm$ and node number $n_{nodes}$ on simulated application execution times

The execution time is significantly higher for lower $n_{nodes}$, but the Figure shows another important fact: the optimal value of the application parameter $dpm$ depends on the value of an execution parameter $n_{nodes}$. In particular, a local execution time minimum for a certain value of $n_{nodes}$ can be a local maximum for another $n_{nodes}$. For example, if only one node is computing the application with $dpm$ set to the optimal value of 24, adding a second computing node without changing $dpm$ does not improve the execution time due to load imbalance. Because the local minima are increasing and local maxima are decreasing, a constant high value of $dpm$ can be used to avoid extreme execution time values, regardless of the $n_{nodes}$ value. However, this comes at a cost of unnecessary communication overheads. In order to execute the application efficiently, both $dpm$ and number of used nodes have to be tuned together. Execution times (Figure 6.10) and speedups (Figure 6.11) are compared depending on $n_{nodes}$ in two cases: using a constant high $dpm = 85$ and using an optimal $dpm$ value for each number of used nodes. Although both approaches achieve good scalability, the second one results in significantly lower execution times, close to theoretically ideal ones.

The parameter tuning examples discussed in this section show that proper tuning of both application parameters and execution parameters has a significant influence on the application execution time. Tuning this parameters is crucial for solving the problem of execution time optimization, defined in Equation 1.3 in Section 1.2. This proves that the parameter tuning step
included in Claim 1 of this dissertation allows to optimize the execution time of the considered application. Simulation can be used to establish optimal parameter configuration in cases when the dependencies between the parameters are non-trivial and an analytical formula for the optimal parameter values is unavailable.

6.1.4. Actual Execution - KernelHive

In this section we describe how the execution configurations established by aforementioned optimization steps are used in practice during actual execution of a hybrid parallel application. Provided the application defined by the user as a DAG with OpenCL kernel implementations corresponding to the graph nodes, KernelHive can perform the step of actual execution through
distributing the appropriate kernels across the chosen nodes, dynamically compiling them for the target platform and handling input and output data transfers. Such execution can be achieved using a mix of existing APIs, for example OpenCL + MPI, but such approach would require programming expertise in these APIs. Using KernelHive simplifies application development and provides automatic parallelization of the application and efficient utilization of the available HPC system.

Figure 6.12 presents scalability of two chosen task farming applications executed using KernelHive on two different systems. Figure 6.12a shows good scalability of the geostatistical interpolation application described in Section 4.1.3 executed in the K2 system described in Section 4.2.3 with the number of used cores exponentially increasing up to 320 (40 nodes with two 4-core CPUs each). Improvement of execution time of the task farming applications executed using KernelHive is also possible in the case of utilizing heterogeneous HPC systems where significant differences in performance of the available computing devices are present. For example, Figure 6.12b shows execution times of the password breaking application described in Section 4.1.1, searching through $5 \times 10^{12}$ hashes, depending on the selection of used "des" and "apl" workstations described in Sections 4.2.1 and 4.2.2, equipped with both CPUs and GPUs. Even though for this application the CPUs are significantly slower than the GPUs [13], using additional resources, up to 284 heterogeneous compute units in the largest case, improves the execution time.

Fig. 6.12. Scalability of chosen task farming applications executed using KernelHive

These results show that proper implementation of the actual execution of hybrid parallel applications allows to reduce their execution time through adding more and more utilized computing devices. This applies to applications that are parallel in both hybridity meanings: executed in multi-level systems combining intra-node and inter-node parallelism, as well as in heterogeneous systems combining different models of computing devices (in this case CPUs and GPUs). This proves the importance of the actual execution step included in Claim 1 of this dissertation.
6.2. Deep Neural Network Training on a Professional Cluster of Workstations With GPUs

The case study described in this section concerns the deep neural network training application described in Section 4.1.5 executed in a professional cluster of workstations with GPUs, described in Section 4.2.5. The case study concerns performing all proposed execution steps on one application, and the provided results support Claim 1 of this thesis. As indicated in Table 6.1, the preliminary process optimization execution step in this case involves minimization of distribution overheads and overlapping of CPU and GPU computations described in Section 6.2.1. Section 6.2.2 describes how the process mapping and parameter tuning steps were performed simultaneously using the simulation method proposed in Section 5.2 and its results support Claim 2 of this thesis. Finally, actual execution of the application using a hybrid Kaldi + MPI solution is described in Section 6.2.3.

6.2.1. Preliminary Process Optimization - Training and Data Preprocessing Overlapping

The considered application is based on Kaldi [155], a free, open-source toolkit for speech recognition research. A crucial part of a speech recognition solution is the acoustic model, trained on a corpus of transcribed speech data. The aim of the training process is to achieve the best efficiency of the acoustic model which requires running several training epochs. An epoch consists of such a number of iterations that every example from the training set is used. In each iteration the backpropagation algorithm [162] is used to train the model using a certain number of audio frames, which is an application parameter \( v_{fpi} \) (frames per iteration). Due to the used method of parallel training with model averaging [156], \( v_{fpi} \) influences both final acoustic model efficiency and training time. In this method, multiple copies of the model are trained in parallel on different parts of the training set and at the end of each iteration the parameters of the model copies are averaged. Each iteration of the parallel training using Kaldi consists of the following steps:

1. distributing and launching the training jobs;
2. reading the model from a network filesystem by each training job;
3. reading and preprocessing on CPU the training data from the local filesystem by each training job;
4. performing the training on a GPU by each training job on the current data;
5. writing the partial model by each training job to the network filesystem;
6. launching the averaging job;
7. reading model from the network filesystem by the averaging job;
8. averaging the models on a CPU;
9. saving the averaged model to the network filesystem.

For the experiments described in this section, the training data was a set of randomly
selected 100 hours (around 90k utterances) from the internal VoiceLab.ai corpora of Polish speech
data. The used HPC system consisted of "cuda5" and "cuda6" workstations described in Section 4.2.5 and the number of used GPUs was gradually increased from 4 to 8 throughout the training.

In order to perform the first of the proposed execution steps, preliminary process optimization, the baseline version of the application has been profiled and three most time consuming operations have been extracted. First, the communication operation of distributing and launching the training programs, because at each time it required using Sun Grid Engine for running a binary on the target machine and allocating a GPU. Secondly, the computation operation of preprocessing (on CPU) the training data from the local filesystem, because it included copying, shuffling and merging the training examples. Finally, the computation operation of actual training using the backpropagation algorithm (on GPU). The other steps were negligible in terms of execution time. The models weighed 27MB each, so reading and saving them did not introduce significant overhead. Neither did launching and executing the averaging program, because it required only a few weight scaling and adding operations on the CPU.

The training program in Kaldi consists of a set of Bash scripts, which perform consecutive steps by launching appropriate binaries and ensuring data flow between them. In the cases when the binaries need to be distributed across available hardware, Sun Grid Engine (SGE) [163] is used, which introduces overhead of launching, managing and queuing of the distributed job binaries. Additionally, each training job introduces overhead of allocating the GPU device. In order to minimize these overheads, a modified, MPI-based training program has been contributed by the author of this thesis in [15]. The application consists of two processes: one master process and a number of slave processes equal to the final, maximum number of used GPUs. The communication operation of job distribution and GPU allocation is performed only once, at the beginning of the training. Between the consecutive iterations, only sending the model back and forth between the master and the slaves is done, which is a significantly less time consuming communication operation.

Since the two computation operations in the baseline version of the application (training data preprocessing and actual training) are executed on different devices in the heterogeneous computing system (CPU and GPU respectively), there is a potential for overlapping these operations. The MPI version of the training program proposed in [15] has been extended with such overlapping. In this version, the following steps are performed at the beginning of the training:

1. master and slave jobs are distributed and launched using MPI;
2. master distributes the archive numbers for the first iteration through message passing across the slaves;
3. data reading and preprocessing is executed by each slave in a separate CPU thread.
Then, each iteration consists of the following steps:

1. **master** distributes the model and training parameters for the current iteration and archive numbers for the next iteration through message passing across the **slaves**;
2. **slaves** perform in parallel:
   - training on a GPU on the previously loaded data;
   - reading and preprocessing the next archive of training data from the local filesystem in a separate CPU thread;
3. sending the model back to the **master** by each **slave** through message passing;
4. averaging the models by the **master**;
5. saving the averaged model to the network filesystem.

Figure 6.13 presents a comparison of execution times of 15 training epochs depending on three chosen values of $v_{fpi}$, for the baseline and the optimized version of the application.

![Fig. 6.13. 15 training epochs execution time comparison depending on the used version of the training program for three chosen values of $v_{fpi}$](image_url)

The following facts can be concluded from the comparison. First, the lower value of $v_{fpi}$, the higher the execution time. This is due to the communication overheads. Low value of $v_{fpi}$ means that a small number of audio frames is processed per each iteration, so the model averaging is performed very often, which increases the communication overheads. Analogously, the lower value of $v_{fpi}$, the higher the benefits of the proposed optimizations: comparing to the baseline version, the optimized version reduces the execution time by 85.5% for $v_{fpi} = 100k$, by 55% for $v_{fpi} = 600k$ and by 40% for $v_{fpi} = 1600k$.

If the $v_{fpi}$ parameter had influence only on the training performance, the most desirable value would be the highest possible, so that the model averaging would be done only once. In such case, the benefits from the proposed optimization would be negligible. However, model averaging is an important part of the parallel training algorithm which influences the performance of the final model measured by the word error rate (WER) metric which is the edit distance between
a reference word sequence and its automatic transcription. The influence of $v_{fpi}$ on the efficiency of the trained model has been examined by the author of this thesis in [15], and out of several considered values, 600k turned out to be the best. In machine learning applications the efficiency of the trained model is of highest priority and cannot be traded off for computation efficiency. This is the motivation for the proposed optimizations. The execution times for $v_{fpi}$ values of 100k and 1600k are presented as extreme values illustrating the influence of the proposed optimizations but the $v_{fpi}$ parameter is not subject to the parameter tuning step, and the true outcome of the proposed optimizations is execution time reduction by 55%. It is a significant improvement, because in practice it allows to try out twice as many machine learning hypotheses in the same time period. In the case of running a single training, reducing the execution time from over 11 hours to 4 hours and 58 minutes allows to obtain the trained model and draw conclusions during the same working day. It should be noted that the main influence (47.7%) on this significant execution time reduction was contributed by the elimination of redundant initialization operations, which was necessary to implement the overlapping. The overlapping itself resulted in relative execution time reduction by 13.6% [15] which is still a significant improvement.

6.2.2. Process Mapping and Parameter Tuning - MERPSYS Simulation

In the deep neural network training case study we used the simulation approach proposed in Section 5.2 to simultaneously perform the process mapping and parameter tuning execution steps proposed in Section 5.1. Evaluating each execution configuration through actual execution of the application would take from 10 to 45 hours depending on the configuration, so testing multiple configurations would be prohibitively long. The proposed modeling and simulation approach allowed exploring power/time trade-off of the application and was the main contribution of the author of this thesis in [16]. The considered optimization problem was multi-objective optimization of execution time and power consumption, defined in Section 1.2 in Equation 1.1. The decision space of the parameter tuning step consisted of the number of used GPU devices and thus, it was directly connected with process mapping. From the practical viewpoint, finding the set of Pareto-optimal solutions in this multi-objective optimization problem helps engineers responsible for running the training to choose the trade-off between performance and power consumption. Having access to a set of computing devices, they can decide if in the given circumstances the computations should finish as soon as possible or if it is acceptable that they run longer but consume less resources, which could be used more efficiently for other applications or stay idle in order to save energy.

In order to perform the simulations, an application model $A = \langle \Phi_A, r_{\min A}, r_{\max A} \rangle$ has been developed in MERPSYS (see Section 5.2). The modeled application was the one described
in Section 4.1.5 in the optimized master/slave version described in Section 6.2.1. A set of two process implementations \( \Phi_A = \{ p^{\text{master}}, p^{\text{slave}} \} \) has been implemented in the proposed Java based meta-language. The \( p^{\text{master}} \) process is responsible for orchestrating the training through distributing and averaging the neural network models and ordering data archive numbers, and the \( p^{\text{slave}} \) process is responsible for performing the model optimization. The modeled process implementations reflect the code of the real application where chosen fragments are replaced by API calls representing operations. Three operations are used in the application model:

- \( \theta_{\text{train}} \) - a computation operation representing an iteration of deep neural network training on a GPU;
- \( \kappa_{\text{send}} \) - a communication operation representing sending the neural network model;
- \( \kappa_{\text{recv}} \) - a communication operation representing receiving the neural network model.

The \( p^{\text{master}} \) process runs multiple iterations of \( \kappa_{\text{send}} \) and \( \kappa_{\text{recv}} \) operations for each instance of the \( p^{\text{slave}} \) process. The \( p^{\text{slave}} \) process consists of a loop that consists of the \( \kappa_{\text{recv}} \) and \( \kappa_{\text{send}} \) communication operations and a \( \theta_{\text{train}} \) operation between them.

In the experiments discussed in this section, the process requirements for \( p^{\text{master}} \) were set to \( r_{\text{min}}^{\text{master}} = r_{\text{max}}^{\text{master}} = 1 \), because there is always exactly one \( p^{\text{master}} \) process in the modeled application. The process requirements for \( p^{\text{slave}} \) were set to \( r_{\text{min}}^{\text{slave}} = 1, r_{\text{max}}^{\text{slave}} = 8 \), so that at least one \( p^{\text{slave}} \) process could be executed, but maximally 8 (the number of GPUs available in the system). The number of actually used GPUs was correlated with the \( v^{\text{nslaves}} \) execution parameter, which in this experiment was the only degree of freedom in the space of application execution parameters \( V_A, S \) [16].

As shown in Figure 6.14, the graphical Editor tool from the MERPSYS environment has been used to prepare the system model resembling the real hardware configuration used at the VoiceLab.ai company. The heterogeneous HPC system \( S(D_S, L_S) \) consisted of 2 workstations connected through a Gigabit Ethernet interconnect, each containing of 4 GeForce GTX TITAN X GPU computing devices connected with a Xeon CPU through an artificial interconnect called "CUDA Device To Host", representing the CPU-GPU interconnect. The hardware capabilities function allowed to run a master process on one CPU device \( (c(d_{\text{CPU}}, \text{\text{CPU}}_0, p^{\text{master}}) = 1) \) and one slave process on each GPU device: \( (\forall i c(d_{\text{GPU}}, p^{\text{slave}}) = 1) \).

The function modeling computation time for the \( \theta_{\text{train}} \) computation operation on each \( d_{\text{GPU}, i} \) device is a linear function \( \text{comptime}(\theta_{\text{train}}, d) = \varphi \cdot \frac{\text{dataSize}(\theta_{\text{train}})}{\text{performance}(d)} + \psi \) where \( \varphi \) and \( \psi \) are tunable constants, \( \text{dataSize}(\theta) \) is an operation parameter denoting size in bytes of the processed data package and \( \text{performance}(d) \) is a hardware parameter denoting performance of the used computing device. The communication time function modeling the \( \kappa_{\text{send}} \) and \( \kappa_{\text{recv}} \) operations, is a linear function \( \text{comptime}(\kappa, l) = t_{\text{startup}}(l) + \frac{\text{dataSize}(\kappa)}{\text{bandwidth}(l)} \), where \( t_{\text{startup}}(l) \) and \( \text{bandwidth}(l) \) are hardware
parameters denoting startup time and bandwidth of a network link, and data\textit{Size}(\kappa) is \textit{operation parameter} denoting the size of the transferred data package. For the GPUs utilized by the \textit{computation operation}, power consumption was set to approximate values measured for real GeForce GTX TITAN X GPUs through the nvidia-smi tool: \(\forall_i (pcidle(d_{GPU_i}) = 70W, pcpeak(d_{GPU_i}) = 140W)\). Analogously to the real application, the model assumes that a GPU is either fully utilized or idle, so the power consumption scaling according to number of threads is not used in this experiment and \(\forall_i (ncores(d_{GPU_i}) = 1)\).

The coefficients \(\psi\) and \(\varphi\) in the \textit{computation time} function have been found using ordinary least squares regression to results from real executions of the training application on one GPU. Execution times of the training \textit{computation operation} have been measured and averaged from four runs, for 25 consecutive iterations. As shown in Figure 6.15, the model tuned on the results from executions with \(v_{\text{slaves}} = 1\) is accurate also in the case of multiple instances of \(p_{\text{slave}}\), with mean percentage error up to 2.7%. Consequently, the simulation results are reliable and can be used for evaluating execution times of whole training epochs that consist of hundreds of training iterations.

It should be noted that in the first attempt to tuning the \textit{computation time} function, a different \textit{operation parameter} was used, namely the number of training examples from the given archive used in the neural network training algorithm. However, in that case the regression results did not show correlation between this \textit{operation parameter} and execution time of an iteration, while in the case of data size in bytes, the correlation was present. Although the number of training examples used by the training algorithm was the same across the archives, it appeared that the
Fig. 6.15. Execution times of consecutive iterations depending on $v_{\text{slaves}}$ (number of $p_{\text{slave}}$ process instances) in the deep neural network training application.
data preprocessing step which shuffled all data in the archive was also significant in terms of execution time. This way, the modeling process allowed the author of this thesis to find a data imbalance bottleneck that the engineers using the application were not aware of. Getting rid of this data imbalance bottleneck would require significant engineering effort, so an estimate of the influence of this bottleneck on the performance of the whole application was needed in order to make the decision if engineering resources should be assigned to this task.

The simulations were repeated for a hypothetical case when the input data would be equally distributed across the input packages. The execution times for this case is denoted in Figure 6.15 by dotted lines. In the case of $v_{nslaves} = 1$ the execution times with balanced data packages are equal to the mean of execution times of the original application. However, the higher value of $v_{nslaves}$, the higher would be the benefit from fixing the data package imbalance, because the more GPUs have to sit idle until the largest data package is processed.

To verify the average power consumption estimations returned by the simulator, their values were compared to a linear model that multiplies the number of used GPUs by the peak power consumption of a single GPU, as shown in Figure 6.16. The simulation results are close to the linear model estimations. It should be noted that the simulated values are getting lower than the ones based on the linear model with the increase of the number of utilized GPUs. This is because the simulator takes into account that the GPUs do not consume additional energy during the idle time resulting from communication, which significance increases with the number of simultaneously utilized devices.

![Fig. 6.16. Verification of the Simulated Average Power Consumption Estimations with a Linear Model](image)

Execution model tuned this way was used to explore the power/time trade-off of the application, which, in terms of the notation proposed in Section 1.2, means using the Pareto method to solving the following optimization problem:
\[
\min_{m, \bar{v}} \quad F(A, S, m, \bar{v}) = [ET(A, S, m, \bar{v}), PC(A, S, m, \bar{v})]
\]

subject to \[ m \in M_{AS} = \{ m(d, p) \mid (m(d_{CPU_0}, p_{\text{master}}) = 1) \]
\[ \land (\forall j, m(d_{GPU_j}, p_{\text{slave}}) \leq 1) \]
\[ \land (1 \leq (\sum_i m(d_{GPU_i}, p_{\text{slave}}) = v_{\text{nslaves}}) \leq 8) \}, \]
\[
\bar{v} = [v_{\text{nslaves}} \in \mathbb{N}^{[1,8]}].
\]

In order to do this, we first executed a simulation of one training epoch consisting of 1061 iterations, where only one GPU took part in the computations. Then, as presented in Figure 6.17, the MERPSYS Web interface was used to order an optimizer suite based on the resultant single simulation instance, allowing the \( v_{\text{nslaves}} \) to vary from 1 to 8 with a step of 1.

![Fig. 6.17. Screenshot of the Optimizer Suite Definition Interface in the MERPSYS Simulation Environment](image)

We defined two such suites - “Suite 1” resembling the real application and “Suite 2” resembling the aforementioned version with equal data distribution. We started the MERPSYS Optimizer component configured to run the ParetoVisualizer module. The Optimizer enqueued all 8 feasible simulation instances for each of the suites and passed the results to the ParetoVisualizer.

A screenshot of the ParetoVisualizer is shown in Figure 6.18. It presents a chart, where horizontal axis represents one optimization objective (execution time) and the vertical axis the second objective (average power consumption). Each point in the chart represents results for one simulation instance. The results depending on \( v_{\text{nslaves}} \) are presented in Figure 6.19, both for the
Fig. 6.18. Screenshot from the MERPSYS ParetoVisualizer after simulating Suite 1 with real archive sizes and Suite 2 with hypothetical ideal load balancing.

| $v_{nslaves}$ | Actual | | Balanced | |
|---|---|---|---|---|
| | Time (s) | Power (W) | Time (s) | Power (W) |
| 1 | 163 528 | 74.189 | 163 528 | 74.189 |
| 2 | 110 282 | 128.267 | 108 965 | 129.804 |
| 3 | 83 646 | 181.006 | 81 685 | 185.332 |
| 4 | 67 425 | 233.532 | 65 348 | 240.939 |
| 5 | 56 538 | 284.916 | 54 405 | 296.125 |
| 6 | 48 846 | 336.171 | 46 699 | 351.602 |
| 7 | 42 995 | 386.517 | 40 842 | 406.780 |
| 8 | 38 286 | 437.595 | 36 218 | 462.498 |

Fig. 6.19. Simulated execution time and average power consumption values for the deep neural network training application, depending on $v_{nslaves}$ and presence of load balancing actual and hypothetical balanced case. In both cases, all points in the decision space belong to the Pareto set, because each number of used GPUs results in either lower power consumption or lower execution time than all others. Hovering with the cursor over a point, the user can see values of $v_{nslaves}$ that were used in the given simulation.

It should be noted that total time of the simulations run on an Intel Core i7-4712HQ CPU used to draw the chart in Figure 6.18 was 2 hours and 10 minutes, while real execution times of the 16 configurations vary from 10 to 45 hours, giving the total execution time of 335 hours. This shows that the proposed simulation method can predict the execution parameters in significantly shorter time than the proper application execution. This proves Claim 2 of this thesis. Although preparing the model and performing the simulation requires a few hours of additional work, the model can be useful for further evaluations in cases of other execution configurations, even currently unavailable. An example of such an unavailable configuration is the hypothetical version.
of the application with balanced load described in this Section, but evaluating different hardware configurations or application execution parameters could also be a practical use case.

6.2.3. Actual Execution - Hybrid Kaldi + MPI

The Kaldi framework used by the considered application consists of a collection of various speech recognition tools, among which there are multiple versions of deep neural network training programs for acoustic modeling. The program used originally by the considered application is called "nnet3-ctc-train", because it uses the "nnet3" deep neural network setup and the Connectionist Temporal Classification [164], loss function. The program utilizes massively parallel GPU computations for deep neural network training through a built-in matrix operation library called CUDA Matrix. The program itself does not handle multiple computing devices, however the Kaldi framework includes a collection of scripts that support queuing the training programs using the SGE cluster resource management system. Multiple training programs can be executed simultaneously on potentially heterogeneous computing devices and a distributed filesystem is required to support data transfers between the programs. This makes it a hybrid parallel application, both in the sense of multi-level and heterogeneous.

Apart from the overhead of GPU initialization by each separate program described in Section 6.2.1, a disadvantage of the original version of the application is that it requires installing and configuring both the SGE cluster management software and a distributed filesystem. In [15] the author of this thesis contributed a modified implementation of the training program called "nnet3-ctc-train-mpi", which mixes the Kaldi API with MPI and uses message passing for transferring the current neural network model data between distributed training programs, coordination of consecutive training iterations and controlling the $v_{\text{slaves}}$ parameter. The proposed program is a hybrid Kaldi + MPI multi-level application that supports overlapping of data preprocessing on CPU and neural network training on GPU. Running the training program does not require additional effort of configuring cluster management software or distributed filesystem. The proposed version of the training program is available as open-source software.

The actual execution step in the case of hybrid parallel applications, which are often multi-level and executed on heterogeneous computing infrastructure, requires advanced, efficient implementation. The proposed hybrid Kaldi + MPI implementation is compared to the original version in terms of performance in Figure 6.13 in Section 6.2.1. This implementation is a practical example of using the execution parameters, established within the optimization steps, during real execution of the application in a professional cluster of workstations with GPUs. This supports the importance of the actual execution step included in Claim 1 of this dissertation.

4https://github.com/roscisz/kaldi-mpi
7. CONCLUSIONS AND FUTURE WORK

The goal of this thesis was to develop an optimization methodology for hybrid parallel application execution in heterogeneous HPC systems. For this purpose, in Chapter 2, existing hybrid parallel applications have been investigated considering the meaning of their hybridity, methods of their execution, possible execution parameters and approaches to modeling their execution on large-scale HPC systems with execution time and power consumption in mind. Approaches to optimization of parallel applications have been discussed in Chapter 3, with a particular emphasis on the trade-offs between execution time and power consumption, computing resource management and parameter auto-tuning.

Multiple experiments have been conducted with real executions involving hybrid parallel applications and heterogeneous HPC systems described in Chapter 4. Based on the experiences from this research, an optimization methodology has been proposed in Chapter 5. The methodology has been verified on a series of case studies described in Chapter 6. Taking into account the results presented in Chapter 6, the claims of the thesis stated in Section 1.5 can be addressed and proven as follows:

1. The execution steps specific in the context of the proposed model, including preliminary process optimization, process mapping, parameter tuning and actual execution allow to optimize execution time of hybrid parallel applications in heterogeneous high performance computing systems.
   - The preliminary process optimization step allowed for a significant reduction of execution time in both relevant case studies described in Chapter 6. Section 6.1.1 provides results for the case study where the step was implemented as computation and communication overlapping that reduced execution time of the considered application up to 11 – 16%. Section 6.2.1 describes a case study where the step was implemented as overlapping of training and data preprocessing, resulting in reduction of execution time of the considered application by 13.6%;
   - The process mapping step implemented as power-aware selection of computing devices allowed to achieve nearly ideal speedups under a strict power consumption constraint in the case study described in Section 6.1.2;
   - In the case study described in Section 6.1.3, the parameter tuning step implemented as tuning of GPU grid configuration allowed to efficiently utilize the computing devices. Additionally, implemented as selection of data partitioning granularity and number of used computing devices, the step allowed to achieve execution times close to theoretically ideal ones;
   - The combined process mapping and parameter tuning steps, implemented as
simulation for exploring the power/time trade-off of the application, allowed to find a set of Pareto-optimal execution configurations in the second case study. The results are described in Section 6.2.2;

- Section 6.1.4 describes a practical example how the actual execution of two task farming applications can be implemented and executed in a large-scale cluster and a heterogeneous system with CPUs and GPUs using the proposed Kernel-Hive framework. The implementation allows to reduce the application execution time through adding utilized computing devices, both in a homogeneous and a heterogeneous hardware configuration. Another example of the actual execution step considering execution of a parallel deep neural network training application, in this case in a professional cluster of workstations with GPUs, is described in Section 6.2.3. The performance results of this implementation presented in Section 6.2.1 show that proper execution of a hybrid parallel application lead to reduction of its execution time by 47.7%, because it eliminated redundant initialization operations.

2. The proposed modeling and simulation method allows for fast and accurate identification of the set of Pareto-optimal solutions to the problem of multi-objective execution time and power consumption optimization of hybrid parallel applications in heterogeneous high performance computing systems.

- The proposed modeling and simulation method allowed to identify the set of Pareto-optimal solutions to the problem of multi-objective time and power consumption optimization in the case study described in Section 6.2. The simulation results were highly accurate and the simulation time was multiple times lower than the time of the simulated executions. These conclusions are based on the results presented in Section 6.2.2.

Although applying the proposed optimization methodology is indeed useful for multiple practical applications, it should not be blindly applied to a given new application. There is a multitude of possible choices of specific actions that could be performed within the proposed execution steps, as well as approaches to execution modeling and simulation, deciding on the application model granularity level, application execution parameters, operation parameters etc. Applying the methodology to new hybrid parallel applications, both in terms of performing the execution steps and developing simulation models, possibly representing various parallel computing paradigms, should be considered as future work. Regarding the proposed simulation method, a possible future work direction could be enabling it for on-line auto-tuning of applications with dynamic re-evaluation of the application execution parameters at application runtime, as well as using the
simulation method for supporting decisions about purchasing new hardware, depending on the expected computational workloads.

Future work could also include approaches to making relaxed assumptions about the applications, for example accepting a certain simplified problem formulation such as ETC and APC matrices, and generating synthetic problem instances. Such an approach might allow to develop sophisticated optimization algorithms aimed for more complex formulations of the optimization problem, in particular considering high-dimensional search spaces. Such algorithms could become useful for emerging real applications, where increasing complexity of the application and execution parameters as well as process mapping constraints can be expected.

The author hopes that the presented viewpoint on the current challenges, selection of discussed literature and proposed practical solutions will be found a valuable contribution.
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