Electret: An Entirely New Approach of Solving Partial Discharge Caused by Triple Points, Sharp Edges, Bubbles, and Airgaps

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ABSTRACT
For the vast majority of applications that involve medium-to-high-voltage operation, partial discharge (PD) has been a chronic issue that causes accelerated dielectric material aging and device failure. Nowadays, with the increasing power density of various medium-to-high-voltage applications, the dielectric challenges introduced by PD are increasing. However, the elimination of PD has been considered virtually impossible due to manufacturing defects that are unavoidable. In this paper, we introduce an entirely new approach that utilizes electrets as a solution to the dielectric challenges caused by PD. Here, we theoretically show that the incorporation of electret layers substantially reduces the undesired high electric fields that promote PD activities. The results suggest that high electric field around sharp edges, triple points, airgaps, and bubbles can be reduced substantially either by controlling the distance between an electret layer and a high-field surface or by tailoring the surface charge density of the electret layers. The required distance and surface charge density for electric field mitigation are theoretically derived and confirmed by finite element analysis. We demonstrate the validity of the proposed method by applying it to laminated structures, in which triple points, airgaps, and bubbles exist. We also report practical considerations and limitations associated to the proposed use of electrets as a solution to PD. The long-term goal of the research is providing enhanced resiliency to the emerging technologies that involve higher electric field and higher power density.

INDEX TERMS
Electric stress, partial discharge, laminated busbars, power electronic modules, electret, sharp edges, triple point, airgap, bubble, dielectric material aging, device failure, high field, high power density.

I. INTRODUCTION
The key trends that drive technological advancements and innovations in recent years in the field of power and energy have been high efficiency, high field, and high power density. Next generation power modules utilizing wide bandgap (WBG) semiconductors with higher breakdown voltage, faster switching speed, and improved efficiency are outperforming the conventional silicon (Si)-based devices [1]. Faster switching speed enables the size and weight reduction of passive components while higher breakdown voltage provided by silicon carbide (SiC) enables fewer number of series connected devices in multilevel converters, all of which results in increasing power density [2]. Additionally, the development of elaborate packaging methods and powerful cooling systems is facilitating high power density operations. Along with the development of WBG power semiconductors, the requirements of laminated busbars also evolved. With the high $dv/dt$ offered by WBG devices and the increasing power density requirements, using thinner insulation layers became increasingly important for parasitic inductance reduction and cooling performance enhancement. The combination of thinner insulation layers in laminated busbars and the increasing voltage blocking capabilities of WBG power modules increases power density. However, this also increases dielectric challenges as reduced thickness and increased voltage inevitably increase electric stress (i.e., electric field) to the level that have not been typically seen in conventional power applications [3]–[5]. The challenges are mainly caused by the intensified local electric fields promoting partial discharge (PD) activities that initiates electrical treeing (a common pre-breakdown phenomenon.
that progresses through electrically stressed solid insulators, 
reduce device lifetime, accelerate dielectric material aging, 
and increase the chance of device failure [6], [7]. Typically, 
PD occurs actively on sharp edges, triple points, airgaps, 
and bubbles as shown in Fig. 1. Triple points are where 
three different types of materials coexist. The difference of 
material properties (i.e., resistivity and permittivity) among 
the three results in generating high electric fields around triple 
points. In addition, airgaps and bubbles are inevitably created 
during bonding processes. These defects may increase and 
crack may occur as devices go under numerous thermal 
cycles and mechanical stresses over time. Depending on 
the material properties of these defects that are generally 
filled with a type of gas, high electric fields may occur 
and become increasingly active in PD that threatens system 
resiliency [8]–[10].

Studies on reducing PD activities on sharp edges and triple 
points have been reported in the literature. Some of them 
are geometry- and material-based solutions that reduce local 
electric fields in power modules [11]–[14]. The geometric 
solution proposed in [11] avoids creating sharp edges by 
rounding the edges of metallization layers and protrudes ceramic substrate layer to relocate triple point and to avoid 
tangential electric field. The material-based approach 
proposed in [12], [13], [15] utilizes zinc oxide (ZnO) microvaristor 
technology. A nonlinear resistive field grading material is 
made by dispersing ZnO microvaristor additives in matrices 
such as epoxy resin. The shape, size, and percolation 
threshold of the additives are the main factors that determine 
the nonlinearity of the material [13]. By covering the sur-
face of the metallization layers and ceramic substrates that 
emit high electric fields with the nonlinear resistive field 
grading material that has resistivity varying nonlinearly as a 
function of electric-field, high electric fields on sharp edges 
and triple points are reduced. This approach is a type of 
resistive field grading method widely used in conventional 
high-voltage applications including cable terminations and 
rotating machines [16]. In general, the resistive field grading 
method utilizes conductive current to reduce locally enhanced 
electric fields [15]. Therefore, the method is prone to Joule 
heating, which is one of the reasons why it was avoided in 
several high-voltage applications [12], [16].

In this paper, we propose an entirely new approach for 
solving the aforementioned dielectric challenges emerging in 
the field of power engineering. We demonstrate that electrets 
can effectively address the dielectric challenges in high-
power-density applications comprised of laminated struc-
tures that inevitably contain sharp edges, protrusions, triple 
points, bubbles, and airgaps. Electrets, which are the electric 
counterpart of permanent magnets, are dielectric materials 
that emit electric fields due to the embedded electric charge 
or dipole orientation [19]. The magnitude of electric field 
generated by electrets is determined by the surface charge 
density, which is reported to be as high as 1,200 μC/m² [20], 
[21]. Electrets can be made of various materials including 
silicon dioxide (SiO₂)-based inorganic materials and 
polymer-based organic materials such as polytetrafluoroethy-
lene (PTFE), high-density polyethylene (HDPE), polyimide 
(PI), and polyvinylidene fluoride (PVDF) [20]–[22]. Numerous 
papers and scientific reports have been published on elect-
ret applications including filters, microphones, and micro 
energy harvesters [23]–[26]. However, no research groups 
have proposed the use of electrets as a means of solving PD 
and the dielectric challenges of emerging technologies.

We utilize two parameters in the electret layer design to 
mitigate the undesired high electric fields. The parameters 
are the surface charge density of the electret layer and the 
distance between a high-field surface and the electret layer. 
First, we theoretically explain the fundamental principles of 
using electret layers for local electric field reduction. Subse-
quently, we incorporate the analytically derived expressions 
into laminated geometries in Comsol Multiphysics software 
to validate the proposed idea of using electrets. Moreover, 
we demonstrate that the proposed method can be used to con-
trol electric fields around triple points, airgaps, and bubbles 
in laminated structures. Furthermore, we discuss the practical 
considerations and the limitations of the proposed method.

II. FUNDAMENTAL PRINCIPLE

Fig. 2 is an illustration of a scenario with two surfaces of arbi-
trary electric potentials and an electret layer in between. The 
bottom surface has a localized high electric field that could 
be caused by triple points, airgaps, and bubbles. We assume 
that the surface on the top has the charge of Q₁, the bottom
surface has the charge of \( Q_2 \), and the electret layer has a surface charge density of \( \sigma_e \). The distance and electric potential difference between the top surface and the electret layer are \( d_1 \) and \( v_1 \), and those between the electret layer and the bottom surface are \( d_2 \) and \( v_2 \). The distance between the top and bottom surface is \( D = d_1 + d_2 \). We define the electric field \( E_1 \) across \( v_1 \) pointing towards the top surface and the electric field \( E_2 \) across \( v_2 \) pointing towards the bottom surface. Assuming that the area of all three surfaces is \( A \), the total amount of charge of the electret is \( Q_e = A\sigma_e \). With the presence of the electret layer, the electric potential difference between the top and bottom surfaces is given as follows.

\[
v_1 - v_2 = v \tag{1}
\]

Charge induced on the top and bottom surfaces, and the total charge of the electret layer are equal in magnitude but opposite in polarity. Hence, the net charge is zero as follows.

\[
Q_1 + Q_2 + Q_e = 0 \tag{2}
\]

Assuming \( C_1 \) and \( C_2 \) are the capacitance across \( v_1 \) and \( v_2 \), respectively, (2) can be expressed as

\[
C_1 v_1 + C_2 v_2 - Q_e = 0 \tag{3}
\]

By applying the definition of capacitance, (3) becomes the following.

\[
\frac{\varepsilon_0 \varepsilon_r v_1}{d_1} + \frac{\varepsilon_0 \varepsilon_r v_2}{d_2} - \sigma_e = 0 \tag{4}
\]

Solving (1) and (4) for \( v_2 \) results in the following.

\[
v_2 = \frac{\sigma_e d_1 d_2}{\varepsilon_0 \varepsilon_r D} - \frac{d_2 v}{D}, \tag{5}
\]

where \( D = d_1 + d_2 \). By dividing (5) by \( d_2 \), we obtain \( E_2 \) as shown below.

\[
E_2 = \frac{\sigma_e d_1}{\varepsilon_0 \varepsilon_r D} - \frac{v}{D} \tag{6}
\]

Similarly, \( v_1 \) and \( E_1 \) are derived as the following.

\[
v_1 = \frac{d_1 v}{D} + \frac{\sigma_e d_1 d_2}{\varepsilon_0 \varepsilon_r D}, \tag{7}
\]

\[
E_1 = \frac{v}{D} + \frac{\sigma_e d_2}{\varepsilon_0 \varepsilon_r D}. \tag{8}
\]

Assuming that a point of high electric field exists on the bottom surface as shown in Fig. 2, the goal is to eliminate the enhanced electric field, which causes of PD and accelerated dielectric material aging. To achieve the goal, we derive surface charge density \( \sigma_e \) and distance \( d_2 \) that satisfy the condition of \( E_2 = 0 \) as shown below.

\[
\sigma_e = \frac{v \varepsilon_0 \varepsilon_r}{d_1} \tag{9}
\]

\[
d_2 = D - \frac{v \varepsilon_0 \varepsilon_r}{\sigma_e} \tag{10}
\]

Equations (9) and (10) show that either the surface charge density \( \sigma_e \) or the distance between the electret layer and the bottom surface \( d_2 \) can be utilized to achieve the zero electric field condition.

III. VALIDATION OF THE PROPOSED METHOD

To validate the required surface charge density and the required distance, we incorporated the design parameters of (9) and (10) into a model that has a triple point on the bottom surface (Fig. 3 and 4). In addition, we show that more than one electret layers can be used to mitigate high electric fields occurring on multiple surfaces (Fig. 5). Furthermore, we discuss the possibility of using stacked electret layers that consist of individual electret layers with low surface charge density (Fig. 6). In all models, both top and bottom layers are copper (Cu) separated by a 2 mm-thick aluminum nitride (AlN) layer. To simulate scenarios with triple points, a section of the Cu layers have been replaced by PTFE. We performed the study with the parameters summarized in Table 1 and 2. It should be noted that the materials were mainly selected to simulate the scenarios with triple points. Hence, the choice of conductive and dielectric materials may vary depending on the requirements of applications. In finite element analysis (FEA), electric fields of sharp edges depend on mesh size. As mesh size decreases, higher electric field results by FEA. However, due to finite mesh size, virtual edge radii that prevent singularity (i.e., formation of infinite electric field) are created around sharp edges. One of the common practices that prevents data misinterpretation on edges, which we used in this study, is measuring electric fields around them. We applied sufficiently fine meshes by decreasing mesh size until electric field at the points of measurements no longer varied as a function of mesh size. Measurement points of interest were set close to edges and triple points, but not exactly on top them to ensure the reliability of the data. Also, the measurement points, which are indicated by arrows in the figures of this study, were consistently maintained within

| Symbol | Equation (9) | Equation (10) |
|--------|-------------|-------------|
| \( w \) | 15 mm | 15 mm |
| \( D \) | 2 mm | 2 mm |
| \( v \) | 24 kV | 12–24 kV |
| \( d_2 \) | 0.1 mm | \( D - \frac{v \varepsilon_0 \varepsilon_r}{\sigma_e} \) mm |
| \( \sigma_e \) | \( \frac{v \varepsilon_0 \varepsilon_r}{d_1} \) C/m² | 1.000 \( \mu \)C/m² |
FIGURE 3. Electric field distributions with a triple point on the bottom layer. (a) Model description. (b) Without any electret layer. (c) With an electret layer with $\sigma_e$ calculated from (9). Note that the gap distance between the electret layer and the bottom layer is 0.1 mm. Each case study to ensure fair comparison. Furthermore, we kept electret domains even in models without electrets to maintain identical mesh conditions between models with and without electret layers.

A. SURFACE CHARGE DENSITY

In Fig. 3, a constant distance between the electret layer and the bottom surface is assumed ($d_2 = 0.1$ mm) while the surface charge density of the electret $\sigma_e$ is adjusted according to (9) to achieve the $E_2 = 0$ condition. The electric potential of 24 kV is applied on the bottom Cu layer while the top Cu layer is grounded. Fig. 3 (b) is the baseline case, in which no electret layer has been introduced into the system. The baseline case shows a locally enhanced electric field of 114.2 kV/mm near the triple point, where Cu, PTFE and AlN layers meet. The electric field of 114.2 kV/mm shown in Fig. 3(b) is high enough to cause PD in bubbles and airgaps that may exist in the vicinity of the triple point. PD reduces the lifetime of dielectric materials and threaten system resiliency. Therefore, it is crucial to mitigate such high electric fields as much as possible. To reduce the locally intensified electric field near the triple point and to prevent PD and accelerated dielectric aging, electret layers are placed above the triple point as shown in Fig. 3(c). The magenta dashed line represents the electret layer with surface charge density $\sigma_e$. Fig. 3(c) shows that the surface charge density of the electret $\sigma_e$ determined by (9) reduces the high electric field around the triple point to 15.8 kV/mm (i.e., more than 86 % reduction). The main reason why the results do not show a field reduction close to 100 % is because (9) is derived based on the assumption that both top and bottom layers are identical in area with a small portion of a distinct material on the bottom layer while the model used in Fig. 3 has a PTFE layer that accounts for a large portion of the bottom layer. Further electric field reduction can be achieved by tuning $\sigma_e$, but we will use the $\sigma_e$ values calculated from (9) in this study.

B. DISTANCE

In Fig. 4, instead of changing $\sigma_e$, a constant surface charge density of the electret (1, 000 $\mu$C/m$^2$) is assumed while the distance between the electret layer and the bottom Cu layer $d_2$ is adjusted to maintain the $E_2 = 0$ condition for the electric potential ranging from 12 to 24 kV using (10). The equation suggests that $d_2$ should be decreased with increasing voltage $v$. Accordingly, Fig. 4 shows the decreasing $d_2$ with increasing system voltage. Although $d_2$ can be utilized to reduce the locally-enhanced electric fields, ultimately, it is best to minimize $d_2$ since it will result in minimizing the necessary value of $\sigma_e$. Therefore, in the following sections, we will keep the distance between electret layers and surfaces with high electric field to 0.1 mm in all scenarios and adjust $\sigma_e$ based on (9).
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C. MULTIPLE TRIPLE POINTS

Here we discuss a scenario, in which triple points exist on both top and bottom surfaces as shown in Fig. 5. In this scenario, electric field around the triple point of the opposite surface is increased when only one electret layer is utilized to mitigate the high electric field at one of the two triple points (Fig. 5 (b)). The reason for the electric field enhancement on the other side of the electret layer is explained by (8). As the equation shows, $E_1$ increases with the electret surface charge density $\sigma_e$. Fig. 5 (b) also shows that placing an electret layer only on one side of the two conductive surfaces rather intensifies the local electric fields. Compared to the 77.9 kV/mm electric field shown in Fig. 5 (a), the electric field is increased to as high as 240.7 kV/mm by having only one electret layer installed. The solution for this phenomenon is placing another electret layer close to the opposite side surface. The $\sigma_e$ values of identical magnitude and opposite polarity are applied on each electret layers as shown in Fig. 5 (c). In this scenario, the top electret layer has a negative $\sigma_e$ while the bottom one has a positive $\sigma_e$ to cancel out the electric field. The resulting electric field of 6 kV/mm at the triple points (i.e., more than 92% reduction) is shown in Fig. 5 (c). The results suggest that placing electret layers on both surfaces is an effective way of reducing the locally-enhanced electric fields.

D. SCALABILITY

In this section, we discuss the scalability of the proposed electret-based dielectric solution. As discussed in the previous sections, the maximum achievable surface charge density $\sigma_e$ of an electret is reported to be around 1, 200 $\mu$C/m$^2$ [20]. However, since higher $\sigma_e$ is required for higher voltage as shown by (9), more than one electret layers may be required to mitigate the locally-enhanced electric fields. Fig. 6 (a) shows the case, in which 5 electret layers are stacked and placed near the high-field surfaces. Each electret layer has the $\sigma_e$ of 101 $\mu$C/m$^2$ that is much lower than the reported maximum surface charge density of electrets [20]. Fig. 6 (b) is a magnified view of the red box of Fig. 6 (a). Compared to the results of the single layer case, where single electret layer with high $\sigma_e$ was used (Fig. 5 (c)), the stacked multiple electret layers resulted in a marginally lower electric field near the triple point: 4.7 kV/mm. The decreased electric field near the triple point likely have been caused by the increasing distance between the electret layers and the copper layer with the additional number of electret layers introduced into the system. Although $\sigma_e$ can be further adjusted for each electret layer to further reduce the electric field near the triple point, for practicality, we simply divided the required $\sigma_e$ that is calculated by (9) by the number of electret layers without recalculating $\sigma_e$ for each individual layer. Overall, the results suggest that stacking multiple electret layers with low $\sigma_e$ can effectively control and mitigate electric fields. The results also indicate that the proposed use of electret layers as a dielectric solution is scalable to the voltage rating of a given application.

IV. APPLICATION: LAMINATED BUSBARS

In this section, we apply the proposed electret approach to solve the dielectric challenges of high-power-density laminated busbars. We assume that the electret layers have a thickness of 0.01 mm and the electret layers are made of PVDF, which is one of the many dielectric materials used for fabricating electrets [19], [20], [27]. The structure of the studied laminated busbar is assumed to be
GPO-Cu-Epoxy-GPO-Epoxy-Cu-GPO. The top half of the structure is shown in Fig. 7. Epoxy, the adhesive layer of the busbar, is 100 µm thick, Cu layers are 200 µm thick, and the GPO layer separating the two Cu layers is 1.8 mm thick. We assumed that the surrounding medium as well as the bubbles and airgaps are filled with air. The electret layer is placed between the epoxy and the GPO layer. The relative permittivity and electrical conductivity of all materials used in the study are summarized in Table 2. We assume that the top Cu layer has an electric potential of 24 kV while the bottom Cu layer is grounded. It should be noted that the electric field measurement locations, indicated by the arrows, are consistent throughout the study for comparison, and the discussion on triple points will not be repeated here as we already discussed the topic in the preceding sections.

A. AIRGAPS IN INTERFACES

Airgaps, where solid materials are completely absent between layers, inevitably exist in conductor and dielectric layer interfaces of laminated structures. An airgap between Cu and GPO layers is shown in Fig. 7. A carefully designed and manufactured busbar may initially have minimum size and number of airgaps, but thermal and mechanical stresses and the coefficient of thermal expansion (CTE) mismatch could increase airgaps in the interfaces over time. Both under DC and AC electric fields, airgaps are good sources of PD due to the relatively weak dielectric strength of gas (air) and high electric field generated in them. Fig. 7 shows a scenario, in which an airgap exist in a conductor and dielectric layer interface. Fig. 7 (b) shows the electric field distribution of a conventional laminated structure without any electret layer in place. Local high electric fields are generated in the GPO layer close to the airgap (62.7 kV/mm) as well as in the airgap itself (53.8 kV/mm). Such high electric field, especially in the airgap, easily causes PD. The conventional way of addressing this issue has been minimizing the number and size of the airgaps as much as possible. Unfortunately, it is practically impossible to completely get rid of all airgaps. Hence, an approach that can mitigate high electric field without removing airgaps is necessary. The proposed use of electrets is a promising solution for such requirement. We introduce an electret layer in the laminated structure as shown in Fig. 7 (c). The surface charge density of the electret layer $\sigma_e$ was chosen based on (9). With the electret layer in place, the high electric field in the airgap reduced to 4.4 kV/mm and that in the GPO layer reduced to 9.5 kV/mm. Based on the proposed electret method, we achieved 92 % and 85 % reduction in the electric fields, respectively. The results suggest that PD activities in laminated structures can be substantially reduced, even with the presence of airgaps, by using electrets as a dielectric solution. The relatively simple placement of a properly designed electret layer can effectively reduce, if not eliminate, the undesired high electric fields generated around the airgaps. The proposed solution is also economical as it dispose of the need for complicated and expensive manufacturing processes that minimize the size and number of airgaps.

B. BUBBLES IN ADHESIVES

Adhesives are used in laminated busbars to attach the layers as well as to displace airgaps between layers. However, like airgaps that are not completely removable, bubbles within adhesives are also not completely avoidable.

### TABLE 2. Material properties used in Sections IV and V.

| Material          | Relative Permittivity | Conductivity [$\text{s/m}$] |
|-------------------|-----------------------|-----------------------------|
| AIN               | 9 [15]                | $10^{-12}$ [15]             |
| Silicone          | 2.86 [15]             | $10^{-12}$ [15]             |
| PVDF              | 6.28 [28], [29]       | $10^{-13}$ [30]             |
| PTFE (Teflon)     | 2.1 [28], [29]        | $10^{-14}$ [29]             |
| Air               | 1                     | $10^{-15}$ [29]             |
| Fi (Kapton)       | 3.5 [31]              | $7.0 \times 10^{-16}$ [31]  |
| Epoxy (3M DP105G)| 9.2 [32]              | $7.8 \times 10^{-9}$ [32]   |
| Epoxy (3M DP420G)| 4.6 [32]              | $1.5 \times 10^{-12}$ [32]  |
| GPO (Glass Polyester) | 4.8 [32]     | $1.8 \times 10^{-13}$ [32]  |
| HDPE              | 2.4 [29], [32]        | $1.9 \times 10^{-15}$ [29], [32] |
Although bubbles can be partially removed and reduced by vacuuming the adhesives (i.e., degassing process), their complete removal is unlikely. Bubbles in adhesives are also great sources of PD due to the same physical reasons that apply to airgaps. Fig. 7 shows the presence of bubbles in the adhesive layer. Although they are not as severe as in airgaps, bubbles also show considerable levels of electric fields that are sufficiently large enough to cause PD. As shown in Fig. 7 (b) and (c), the proposed method of using electret layers reduces the electric field from 5.0 kV/mm to 0.3 kV/mm (94% reduction). The result suggests that the proposed electret method can effectively solve the dielectric challenges associated with bubbles regardless of their size and shape.

C. NONLINEAR RESISTIVE FIELD GRADING (NRFG)

It is worth discussing the nonlinear resistive field grading (NRFG) method as it is one of the conventional methods used for electric field reduction in electric machines and cable terminations. Materials with electric field dependent resistivity such as ZnO microvaristors, which have been used widely in surge arresters, are the main provider of the nonlinear resistive properties [12], [13], [16]. Recently, the idea of adopting the nonlinear field grading method to power electronics modules has been reported in the literature [14], [15]. The studies report that the resistive field grading materials can effectively reduce the high electric fields generated on edges and triple points in power modules. However, it should be noted that nonlinear resistive field grading involves current conduction that causes Joule heating [12]. The severity of generated heat in the NRFG of power modules is yet to be determined, but Joule heating was one of the major reasons why the resistive field grading was avoided in some high voltage applications [12].

To confirm whether the NRFG method can effectively reduce high electric fields around bubbles and airgaps, we replaced the epoxy adhesive layer with the NRFG layer. Electric field distribution when nonlinear resistive field grading (NRFG) layer is used instead of the epoxy adhesive layer. In contrast to the effective field mitigation achieved by the proposed electret approach shown in Fig. 7 (c), NRFG layer is not capable of mitigating high electric fields occurring around bubbles and airgaps.

\[ \sigma = \sigma_0 \left( 1 + \left( \frac{E}{E_b} \right)^{\alpha - 1} \right), \]

where \( E_b = 2 \text{kV/mm} \) and \( \alpha = 7 \). \( E_b \) determines the electric field, at which the conductivity increases nonlinearly and \( \alpha \) determines the nonlinearity (i.e., slope) of the increasing conductivity when \( E \) exceeds \( E_b \). We assume that the field dependent material is ZnO microvaristor that has a relative permittivity \( \varepsilon_r = 12 \) and base conductivity \( \sigma_0 = 3.3 \times 10^{-11} \text{S/m} \). Fig. 8 shows the electric field distribution of the laminated structure with 24 kV applied on the Cu layer. The results do not show any sign of electric field reduction compared to the field distributions shown in Fig. 7 (c), where the proposed electret method was used. The results suggest that the NRFG materials can only reduce high electric field when they are exposed to it. Since high electric field also occurs in airgaps and bubbles, where NRFG doesn’t exist, high fields cannot be reduced with the use of NRFG. The results demonstrate that the NRFG method cannot effectively reduce high-intensity electric fields in airgaps and bubbles although this method can reduce high electric fields occurring on protrusions and triple points as reported in [13], [15].

D. ELECTRET MATERIAL SELECTION

Electric field distribution in electret layers changes depending on the material properties of the base material of the electret layers. Under DC electric stresses, electrical conductivity dominates the field distribution while the relative permittivity of the electret material dominates the field distribution under AC electric stresses. We focus on DC electric fields in this study, so we investigate the impact of using various materials of distinct electrical conductivity. For the study, we simulated PTFE, HDPE, PI, and PVDF as shown in Fig. 9. These materials are commonly-used base materials for electrets. As listed in Table 2, the electrical conductivity of PTFE is the lowest and PVDF is the highest. Since larger potential drop occurs through materials with higher resistivity, PTFE-based electrets result in the highest internal electric stress while that of the PVDF is the lowest. From the dielectrics perspective, it is best to use PVDF as the electret layer as it results in the lowest electric stress. However, since many polymeric dielectric materials have dielectric strengths around tens of kV/mm or higher, the electric fields in the electret layers shown in Fig. 9 are not particularly significant stresses to the materials. For instance, the maximum electric field measured in HDPE shown in Fig. 9 (b) is 50.7 kV/mm. Although this is a high electric field for air, 50.7 kV/mm is much lower than the dielectric strength of HDPE, which is reported to be on the range of several hundreds of kV/mm. Furthermore, it should be noted that the highest electric fields are mainly generated at the edges of the electret layers as shown in Fig. 10. These high fields can be controlled by proper edge design and finishing materials that are discussed in the following section.
FIGURE 9. Electric field distributions in a laminated busbar with various types of electret materials. (a) PTFE (Teflon) electret. (b) HDPE electret. (c) PI (Kapton) electret. (d) PVDF electret.

ELECTRET EDGE TREATMENT

In practice, the edges of electret layers could be flush, indented, or protruded than the rest of the layers in laminated structures. Hence, in this section, we discuss the correlation between electric field distribution and the various types of electret layer edges. The electric field distribution resulting from the three edge types are shown in Fig. 10. In all three subfigures, all model parameters except for the edge of the electret layer are identical. The results indicate that the flush edge results in the lowest electric field near the edge (Fig. 10 (a)) while the short edge results in the highest electric field (Fig. 10 (b)). Thus, ideally, it is best to have a flush edge to achieve minimum electric field. Nevertheless, achieving a perfectly flush edge is impossible in practice as there will always be some degree of protrusion or indentation on the edges.

The high electric fields occurring on the electret layer edges can be reduced by covering them with dielectric materials that have properties (i.e., conductivity for DC stresses, permittivity for AC stresses) similar to the surrounding materials. This is to avoid high electric fields caused by the dissimilarity of materials properties. Here, we selected an epoxy resin (3M DP420 in Table 2) that has a similar electrical conductivity and relative permittivity as GPO to reduce electric field enhancements. As shown in Fig. 11, the thickness of the epoxy finish layer is 200 µm in all cases, which is large enough to fully cover the protruded electret layer. Interestingly, the flush edge with the epoxy finish resulted in increasing the electric field from 37.3 kV/mm (Fig. 10 (a)) to 46.7 kV/mm (Fig. 11 (a)). The intensified electric field is mainly due to the combined effect of the electrical conductivity of the four different materials (3M DP105, 3M DP420, GPO, and PVDF) around the flush edge. Again, we show the flush edge case for study purposes only and would like to note that having a perfect flush edge is unlikely in real applications. In the cases of the short and long edges (Fig. 11 (b) and (c)), electric field reduced with the epoxy finish layer in place. In the short edge case, it is assumed that the epoxy finish layer completely fills the airgap created by the short electret edge. Again, in reality, it is difficult to completely fill such airgaps, which results in creating electric-field-intense air pockets. Therefore, the best way of ensuring the absence of airgaps is to have the electret layers protruding from the rest of the layers and to cover the edges with epoxy finish as shown in Fig. 11 (c). This approach results in reducing the maximum electric field from 53.9 kV/mm (Fig. 10 (c)) to 16.8 kV/mm (Fig. 11 (c)).

V. APPLICATION: POWER ELECTRONIC MODULES

One of the key features in the power electronic modules is the constantly switching voltage of metallization layers. Assuming a unipolar half bridge inverter, the output voltage constantly switches between zero and $V_{dc}$. Since the surface charge density of electrets is determined during the design process, the surface charge density value that minimizes electric field at the maximum voltage (i.e., $V_{dc}$) will induce the same magnitude of electric field of opposite polarity at ground potential. To avoid this phenomena, the surface charge density of electrets should be 50 % of that minimizes electric field at the maximum voltage of $V_{dc}$. This also indicates that electric field can be reduced by 50 % in power electronic modules where the voltage of a metallization layer constantly switches between $V_{dc}$ and zero. Although the 50 % electric field reduction achievable in power modules is not as great as the 92 and 94 % reduction shown in the laminated busbar example (Fig. 7), the 50 % reduction could substantially mitigate PD provided that the electric field falls below the PD inception field.

Fig. 12 shows the electric field distributions in a power electronic module without electret layers installed, in which the voltage of the Cu metallization layer switches between 24 kV and 0 V. Fig. 12 (a) shows the laminated structure of the power module without electret installed. The bottom Cu metallization is electrically grounded while the voltage of the top Cu layer constantly switches. As shown in
Figs. 12 (b)–(d), high electric field occurs around the triple point indicated by the red arrows. As expected, the maximum electric field of 118.4 kV/mm occurs at the voltage of 24 kV. On the other hand, the electric field distributions in a power module with electret layers installed are shown in Fig. 13. As shown in Fig. 13 (a), electret layers are installed 0.2 mm away from the Cu metallization layers. It should be noted that we assumed the distance of 0.2 mm for the study, but the location of the electret layers could be closer to or farther away from the Cu metallization layers in practice. Figs. 13 (b)–(d) show the electric field distributions as voltage varies between 24 kV and 0 V. The figures show that, in any moment of switching voltage, electric field is kept below 60 kV/mm with the electret layer installed. Because the surface charge density of electrets used in this case is 50 % of the maximum value due to the reasons discussed earlier, negligible field appears at 12 kV (rather than at 24 kV) while the electric fields of about 59 kV/mm occur at 0 V and 24 kV (i.e., 50 % of 118.4 kV/mm in Fig. 12). Although electric field occurs at even 0 V, the maximum electric field is reduced by 50 % compared to the case without electrets. From the perspective of dielectrics and electrical insulation, what matters most is the intensity of the maximum electric field. Therefore, the use of electrets in power electronic modules is beneficial for the lifetime enhancement of the devices. It is worth noting that the application of electret is limited to unipolar operation and is unsuitable for bipolar operation, in which voltage, for instance, switches between + and − \( V_{dc} / 2 \).

Except for in DC systems, electric field distribution (i.e., electric stress distribution) is governed by both resistive and capacitive currents. Even though power electronics driven systems are categorized as non-AC systems, due to high \( dv/dt \) occurring in these systems, electric stress is mainly determined by capacitively distributed electric fields as in AC systems. In other words, the relative permittivity of dielectric layers plays a major role in the distribution of electric fields. However, the effect of permittivity-driven electric field distribution may be reduced as power electronics technology continues to advance and enable higher switching speeds because the polarization of dielectric materials may no longer be fast enough to react against the extremely high \( dv/dt \). Furthermore, space charge accumulation may also significantly impact dielectric performance under non-AC conditions. However, the details of this phenomenon are not discussed here since the topic is beyond the scope of this study.

VI. DISCUSSION
A. NECESSARY IMPROVEMENTS
As shown by the results of this study, the proposed use of electret is effective in mitigating high electric fields of local hot spots in laminated structures. However, a major
disadvantage of using electrets originates from their low thermal conductivity. Due to the low thermal conductivity of electret materials, the incorporation of electret layers is likely to decrease the heat transfer of laminated structures. For example, PVDF, one of the electret materials discussed in this study, has a thermal conductivity of $1.2 \text{ Wm}^{-1}\text{K}^{-1}$ while AlN, the ceramic substrate layer, has a thermal conductivity of $310 \text{ Wm}^{-1}\text{K}^{-1}$. The likely increase of temperature caused by the incorporation of electrets may considerably alter the conductivity of dielectric layers and cause changes in the electric field distribution. This indicates that locations exposed to high electric stresses may also change as a function of temperature. A point to note is that the variation of electric field distribution caused by temperature is likely to be dominated by electrical conductivity as it is much more sensitive to temperature variation than permittivity.

One of the methods of minimizing the reduction thermal conductivity of electret layers along metallization layer edges is shown in Fig. 14 (a). This approach significantly reduces the footprint of electret layers in laminated structures thereby minimizing the reduction of heat flow through base substrates. Although this approach negligibly impacts the original thermal conductivity of substrate layers, it has a limitation of not being able to mitigate high electric fields occurring beneath metallization layers except for those along the edges. Other methods of minimizing the thermal conductivity reduction caused by electret incorporation are minimizing the thickness of electret layers and increasing the thermal conductivity of electret materials by mixing them with thermally conductive nanoparticles such as silicon carbide (SiC), which has a thermal conductivity of $360 \text{ Wm}^{-1}\text{K}^{-1}$.

**B. SPRAY COATED ELECTRET**

One of the means of fabricating electrets is spray coating [33]. The method is particularly suitable for incorporating electrets in power-dense applications comprised of laminated structures owing to its versatility. The process of electret incorporation based on spray coating is introduced in Fig. 14 (a). Step 1 is the fabrication of protruded AlN substrate layers that can be achieved by various sputtering and etching processes [34]–[36]. Step 2 is the spray coating of electret layers on the AlN substrate. Here, electrets are selectively coated only along the edges to mitigate field enhancements occurring on sharp edges and triple points. Step 3 is the bonding process of Cu metallization layers. The versatility provided by the spray coating of electret enables the effective
incorporation of electrets with minimal footprint, which is beneficial for minimizing their impact on the inherent thermal properties of laminated structures.

Electric field distributions of the power electronic module substrate without and with the sprayed electret layers are shown in Figs. 14 (b) and (c). The top Cu metallization layers are applied with +12 kV and -12 kV, respectively, while the bottom Cu layer is electrically grounded assuming it is connected to a heat sink beneath it. The power module substrate without the coated electret layers results in high electric fields around the edges of the top Cu metallization layers. In contrast, the substrate with the coated electret layers shows electric fields substantially lower than in the previous case without electrets. The maximum electric field of 36.2 kV/mm reduced to 2.7 kV/mm with the sprayed electret layers. The results of Fig. 14 demonstrate that the spray coating method of electret layers effectively mitigates electric fields in power modules with minimal footprint.

C. BREAKDOWN STRENGTH

There are several breakdown mechanisms associated to solid dielectrics. These include electrical, thermal, and electrochemical processes. The fastest mechanism among the three is electrical breakdown that occurs due to high electric field applied to solid dielectric materials. Similar to dielectric breakdown processes in gases, excessive electron-lattice ionization collisions cause electron avalanche that leads to immediate dielectric breakdown. Such immediate breakdown rarely occurs in systems equipped with proper insulation coordination under normal operation. Thermal breakdown is a slower process than the electrical breakdown mechanism. This breakdown mechanism is caused by solid insulator heating. The rise in temperature increases conductivity, which increases leakage current and dielectric loss. If cooling is insufficient, the heating process develops into a thermal runaway and causes dielectric breakdown. The most challenging mechanism is the electrochemical breakdown, which includes PD and treeing. These mechanisms are subtle and slow, hence difficult to detect and even more difficult to avoid. They do not cause immediate failure, but they are the main culprits of device aging in various applications that utilize medium- to high-voltage. The breakdown strength (i.e., breakdown voltage per unit length) of each mechanism varies over a wide range. However, minimizing the strength of electric field is a common goal regardless of the breakdown mechanisms.

As demonstrated by the results of this study, the proposed use of electrets reduces electric field without altering the material properties of preexisting insulation layers. With the dielectric strength of the preexisting insulation kept identical, the reduction of electric field decreases the likelihood of all three breakdown mechanisms. In short, the use of electrets improves breakdown strength by enabling higher voltage operation with reduced electric fields.

VII. CONCLUSION

In this study, we introduced an entirely new approach of utilizing electrets to address PD in laminated structures including laminated busbars and power electronic modules. We showed that the distance and surface charge density of electret layers can be tailored to effectively mitigate undesired high electric fields, which are the main causes of PD. Reduction of locally-enhanced electric fields around sharp edges, triple points, bubbles, and airgaps is crucial for preventing accelerated dielectric material aging and device failure caused by PD and PD-initiated electrical treeing. The following list summarizes the key results of our study.

- High electric fields generated around triple points can be reduced by more than 92% with the use of electret layers with $\sigma_e$ determined by (9). The results are shown in Fig. 5.
- Stacked layers of multiple electrets can be used in situations where $\sigma_e$ per electret layer is insufficient. The results demonstrate the scalability of the proposed electret method. The results are shown in Fig. 6.
- High electric fields generated in and around bubbles and airgaps can be reduced by 94% with the use of electret layers with $\sigma_e$ determined by (9). The results are shown in Fig. 7.
to the materialization of resilient next-generation power electronic modules. The proposed idea of using electrets in laminated busbars and power electronic modules showed great promise towards solving dielectric challenges in the field of power and energy, in which higher power density is increasingly demanded. More practical aspects related to improving thermal conductivity, fabricating electrets, and implementing them in real applications will be reported in our future publications. We anticipate the proposed electret method to contribute to the materialization of resilient next-generation power technologies.

REFERENCES

[1] A. O. Adan, D. Tanaka, L. Burgyan, and Y. Kakizaki, “The current status and trends of 1,200-V commercial silicon-carbide MOSFETs: Deep physical analysis of power transistors from a Designer’s perspective,” IEEE Power Electron. Mag., vol. 6, no. 2, pp. 36–47, Jun. 2019.

[2] C. M. DiMarino, R. Burgos, and B. Dushan, “High-temperature silicon carbide: Characterization of state-of-the-art silicon carbide power transistors,” IEEE Ind. Electron. Mag., vol. 9, no. 3, pp. 19–30, Sep. 2015.

[3] H. Lee, V. Smet, and R. Tummala, “A review of SiC power module packaging technologies: Challenges, advances, and emerging issues,” IEEE J. Emerg. Sel. Topics Power Electron., vol. 8, no. 1, pp. 239–255, Mar. 2020.

[4] E. A. Jones, F. F. Wang, and D. Costinett, “Review of commercial GaN power devices and GaN-based converter design challenges,” IEEE J. Emerg. Sel. Topics Power Electron., vol. 4, no. 3, pp. 707–719, Sep. 2016.

[5] X. She, A. Q. Huang, O. Lucía, and B. Ozpineci, “Review of silicon carbide power devices and their applications,” IEEE Trans. Ind. Electron., vol. 64, no. 10, pp. 8193–8205, Oct. 2017.

[6] P. Wang, G. C. Montanari, and A. Cavallini, “Partial discharge phenomena and induced aging behavior in rotating machines controlled by power electronics,” IEEE Trans. Ind. Electron., vol. 61, no. 12, pp. 7105–7112, Dec. 2014.

[7] P. Wang, A. Cavallini, and G. C. Montanari, “Characteristics of PD under square wave voltages and their influence on motor insulation endurance,” IEEE Trans. Dielectr. Electr. Insul., vol. 22, no. 6, pp. 3079–3086, Dec. 2015.

[8] G. C. Montanari, R. Hebner, P. Morshuis, and P. Seri, “An approach to insulation condition monitoring and life assessment in emerging electrical environments,” IEEE Trans. Power. Del., vol. 34, no. 4, pp. 1357–1364, Aug. 2019.

[9] T. Liu, Q. Li, X. Huang, Y. Lu, M. Asif, and Z. Wang, “Partial discharge behavior and ground insulation life expectancy under different voltage frequencies,” IEEE Trans. Dielectrics Electr. Insul., vol. 25, no. 2, pp. 603–613, Apr. 2018.

[10] P. Romano, T. Hammarstrom, T. Bengtsson, A. Impuglia, A. Madonia, F. Viola, and S. M. Gabanski, “Partial discharges at different voltage wave-shapes: Comparison between two different acquisition systems,” IEEE Trans. Dielectr. Electr. Insul., vol. 25, no. 2, pp. 584–593, Apr. 2018.

[11] H. Reynes, C. Buttay, and H. Morel, “Protruding ceramic substrates for high voltage packaging of wide bandgap semiconductors,” in Proc. IEEE 5th Workshop Wide Bandgap Power Devices Appl. (WiPDA), Albuquerque, NM, USA, Oct. 2017, pp. 404–410.

[12] T. Christen, L. Donzel, and F. Greuter, “Nonlinear resistive electric field grading part 1: Theory and simulation,” IEEE Elect. Insul. Mag., vol. 26, no. 6, pp. 47–59, Nov. 2010.

[13] L. Donzel, F. Greuter, and T. Christen, “Nonlinear resistive electric field grading part 2: Materials and applications,” IEEE Elect. Insul. Mag., vol. 27, no. 2, pp. 18–29, Mar. 2011.

[14] L. Donzel and J. Schuderer, “Nonlinear resistive electric field control for power electronic modules,” IEEE Trans. Dielectr. Electr. Insul., vol. 19, no. 3, pp. 955–959, Jun. 2012.

[15] M. M. Tousi and M. Ghassemi, “Characterization of nonlinear field-dependent conductivity layer coupled with protruding substrate to address high electric field issue in high-voltage high-density wide bandgap power modules,” IEEE J. Emerg. Sel. Topics Power Electron., vol. 8, no. 1, pp. 343–350, Mar. 2020.

[16] X. Yang, X. Zhao, Q. Li, J. Hu, and J. He, “Nonlinear effective permittivity of field grading composite dielectrics,” J. Phys. D: Appl. Phys., vol. 51, no. 7, Feb. 2018, Art. no. 075304.

[17] S.-K. Lee and W.-H. Tuan, “Eliminating voids at Al2O3-cu interface during bonding,” Int. J. Appl. Ceram. Technol., vol. 12, no. 5, pp. 1020–1026, Sep. 2015.

[18] D. P. Hamilton, S. Riches, M. Meisser, L. Mills, and P. Mawby, “High temperature thermal cycling performance of DBA, AMB and thick film power module substrates,” in Proc. 9th Int. Conf. Integ. Power Electron. Syst., Mar. 2016, pp. 1–5.

[19] V. N. Kestelman, L. S. Pinchuk, and V. A. Goldade, “Partial discharges at different voltage waveforms,” IEEE Trans. Power Del., vol. 25, no. 2, pp. 603–613, Apr. 2010.

[20] D. Y. Yeom, E. Shim, and B. Pourdeyhimi, “Boehmite nanoparticles incorporated electret power generators,” IEEE Trans. Power Syst., vol. 25, no. 2, pp. 448–456, Apr. 2010.
[28] Z. Ahmad, “Polymer dielectric materials,” in Dielectric Material. London, U.K.: IntechOpen, 2012, doi: 10.5772/50638., doi: https://www.intechopen.com/books/dielectric-material/polymer-dielectric-materials

[29] A. Kuchler, High Voltage Engineering: Fundamentals—Technology—Applications. Berlin, Germany: Springer, 2018. [Online]. Available: https://www.google.com/books/edition/High_Voltage_Engineering/FgQkDwAAQBAJ?hl=en&gbpv=0

[30] R. Ram, M. Rahaman, and D. Khomeir, “Electrical properties of polyvinylidene fluoride (PVDF)/multi-walled carbon nanotube (MWCNT) semi-transparent composites: Modelling of DC conductivity,” Compos. A, Appl. Sci. Manuf., vol. 69, pp. 30–39, Feb. 2015.

[31] Dupont Kapton Summary of Properties, DuPont, Wilmington, DE, USA, 2017.

[32] Y. Xu, X. Feng, J. Wang, C. Gao, R. Burgos, D. Boroyevich, and R. E. Hefner, “Medium-Voltage SiC-Based Converter Laminated Bus Insulation Design and Assessment,” IEEE J. Emerg. Sel. Topics Power Electron., vol. 7, no. 3, pp. 1715–1726, Sep. 2019.

[33] Y. Xu, A. Luo, A. Zhang, Y. Zhang, B. Tang, K. Wang, and F. Wang, “Spray coating of polymer electret with polystyrene nanoparticles for electrostatic energy harvesting,” Micro Nano Lett., vol. 11, no. 10, pp. 640–644, Oct. 2016.

[34] M.-A. Dubois and P. Muralt, “Stress and piezoelectric properties of aluminum nitride thin films deposited onto metal electrodes by pulsed direct current reactive sputtering,” J. Appl. Phys., vol. 89, no. 11, pp. 6389–6395, Jun. 2001.

[35] X.-H. Xu, H.-S. Wu, C.-J. Zhang, and Z.-H. Jin, “Morphological properties of AlN piezoelectric thin films deposited by DC reactive magnetron sputtering,” Thin Solid Films, vol. 388, nos. 1–2, pp. 62–67, Jun. 2001.

[36] D. Zhuang and J. H. Edgar, “Wet etching of GaN, AlN, and SiC: A review,” Mater. Sci. Eng., R, Rep., vol. 48, no. 1, pp. 1–46, Jan. 2005.

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