Embracing the Unreliability of Memory Devices for Neuromorphic Computing

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Invited Paper

Abstract—The emergence of resistive non-volatile memories opens the way to highly energy-efficient computation near- or in-memory. However, this type of computation is not compatible with conventional ECC, and has to deal with device unreliability. Inspired by the architecture of animal brains, we present a manufactured differential hybrid CMOS/RRAM memory architecture suitable for neural network implementation that functions without formal ECC. We also show that using low-energy but error-prone programming conditions only slightly reduces network accuracy.

I. INTRODUCTION

Emerging nonvolatile memory technologies such as resistive, phase change and spin torque magnetoresistive memories offer considerable opportunities to advance microelectronics, as these memories are faster than flash memories, while being compact and compatible with the integration in the backend-of-line of modern CMOS processes [1], [2]. However, although these technologies are usually more reliable than flash memories, they remain considerably less reliable than volatile charge-based random access memories. Strategies for reducing errors due to device variation and limited endurance involve costly materials and technology developments [3], energy-consuming special programming strategies [4], and quite universally, the reliance on advanced multiple error correcting codes (ECC) [1], [5], requiring large area and energy hungry decoding circuitry [6].

The existence of errors in emerging memories is also a severe limitation for the development of in or near-memory computing schemes, which aim at achieving highly energy efficient computation by eliminating the von Neumann bottleneck [1], [7]. In or near-memory computing schemes are indeed hardly compatible with ECC, as computation is performed with multiple row selection or in the sensing circuit [8], [9]. These constrains are in sharp contrast with animal brains, which function with vastly unreliable, redundant, memory devices (synapses) without using formal error correction [10], [11].

In this work, we show through an example that in computing architectures inspired by brains (neuromorphic architectures), memory device variability can to a large extent be ignored, and even embraced, and that this attitude can provide important benefits. We first present a differential memory architecture optimized for the ECC-less in-memory implementation of biarized neural networks. We show based on experimental measurements on a fabricated CMOS/RRAM hybrid chip and on network simulations that this architecture can mostly ignore device variation, and investigate the benefits of accepting errors. Based on a modeling study, we show that the same methodology could be transferred to MRAM.

II. AN IN-MEMORY COMPUTING MEMORY BLOCK THAT FUNCTIONS WITH ERROR-PRONE DEVICES

In this work, we propose the use of a memory architecture where each bit is stored in a two-transistor/two-resistor (2T2R) cell. We implemented a kilobit version (2,048 devices) of this architecture in a 130 nm CMOS technology, with hafnium oxide-based RRAM fully embedded in the backend-of-line (Fig. 1). This test chip was initially introduced in [8], [9]. Bits are stored in a differential fashion between the two devices to reduce errors. Doing so, during the read phase, a high
III. Benefits at the Network Level

Binarized Neural Networks (BNNs) [14], or the highly similar XNOR-NETs [15], are a recently proposed type of neural network, where synaptic weights and neuron states can take only binary values (meaning $1$ and $-1$) during inference (whereas these parameters assume real values in conventional neural networks). Therefore, the equation for the activation $A$ of a neuron in a conventional neural network

$$A = f \left( \sum_{i} W_i X_i \right),$$  

(statistical measurements on the fabricated test chip, taken with diverse programming currents, allowing evaluating the bit error rates (BER) benefits of the 2T2R approach in different conditions. It is apparent in this Figure that the 2T2R strategy always reduces the amount of bit errors, with the highest benefits seen at lower BERs. The detailed methodology for obtaining Fig. 3(a) is presented in [9].

Quite interestingly the error reduction benefits of the 2T2R approach are similar to the one of a Single Error Correcting Double Error Detecting ECC (SECDED, or extended Hamming), but without the high peripheral circuit overhead required by this ECC [9], and associated read performance degradation (Fig. 3(b)). Moreover, this result is obtained considering the same memory capacity (2T2R without ECC versus 1T1R plus extra bit for correction code storage).
Fig. 5. Impact of the BER of memories on applications of Binarized Neural Network: handwritten digit recognition (MNIST), image recognition (CIFAR-10, ImageNet TOP-1 and TOP-5). Details about the neural network architectures are provided in [9].

Fig. 6. Number of errors on a one kilobit array using the 2T2R strategy (with PCSA) for different programming conditions (compliance current $I_C$, RESET voltage $V_{appReset}$, and programming pulse duration $t_{pulse}$). Error bars represent the minimum and the maximum number of errors over five trials of the experiment. Figure adapted from [9].

Fig. 7. Mean programming energy (per bit) of RRAM cells in the (a) SET and (b) RESET processes for the programming conditions shown in Fig. 6.

Fig. 8. Endurance measurement for two devices (bit line BL and bit line bar BLb), programmed in weak conditions ($V_{appReset} = 1.5V$, $I_C = 200\mu A$, $t_{pulse} = 1\mu s$). Figure adapted from [9].

(2) POPCOUNT is an integer function that counts the number ones. $sign$ is the sign function, and $T$ is the threshold of the neuron, obtained during training by the use of the batch-normalization technique [16].

BNNs can achieve surprisingly high accuracy in vision [15], [17] or signal-processing [18] tasks. BNNs have highly reduced memory requirements with regards to real neural networks, and have the added benefit of not requiring any multiplication, as this operation is replaced by XNOR logic operations. These advantages make BNNs outstanding candidates for in-memory computing [19]–[26].

The architecture of Fig. 1 is particularly adapted for the ECC-less implementation of such neural networks. For example, Fig. 4 shows a full system using memory circuits of Fig. 1 to implement a BNN. The architecture uses the sense amplifier of Fig. 2(b) [12] to implement XNOR operations directly in each memory circuit during the read phase, whereas the POPCOUNT operation, as well as neuron activation are performed on foot of array columns using fully digital circuits. Refs. [9], [27] describe this architecture in detail, as well as some its variations, and show that this architecture features...
The combination of the fact that the 2T2R approach allows reducing the amount of bit errors, and that the BNN application features inherent tolerance to bit errors has important consequences in practice. It allows us to use RRAM devices in regimes where they are extremely unreliable. This can provide important energy savings: we can use devices with very weak programming conditions (low current and voltages, short programming time), where they feature high amounts of bit errors. Figs. 6 and 7 show statistical measurements of our test chip in various conditions, and highlight the energy benefits of accepting more errors. Finally, operating devices in high BER regimes allows using conditions where they feature outstanding endurance. Fig. 8 for example shows endurance measurements of two devices programmed with low RESET voltages (1.5V). An endurance of more than $10^{10}$ cycles is seen, which is particularly high for such technology. This type of high cyclability opens the way to the possibility of training neural networks on chip, as seen in the results reported in [32]. A more detailed analysis of the energy benefits (which can reach a factor ten) of embracing bit errors in RRAM-based BNNs, and of the associated endurance benefits, is presented in [9].

The strategy reported in this work is not limited to RRAM, and can be applied to other types of memories. Fig. 9 shows, based on neural network simulation, the energy that could be saved by varying the programming time of 28 nm Spin Torque Magnetoresistive RAM (ST-MRAM) using the same approach as the one presented here. We see that high energy savings can be achieved. The methodology and model for obtaining these results are presented in [13].

IV. Conclusion

Digital computing usually assumes and requires perfection in the memory bits, and this accuracy comes at important costs in terms of area and energy consumption. In contrast, neuromorphic circuits, including fundamentally digital ones such as binarized neural networks can get away with imperfect memory cells. In this work, we use a differential approach to reduce errors and to be compatible with in or near-memory computing. This differential coding, in combination with the inherent tolerance of neural network, shows that it is possible on one side to embrace memories as “non ideal” without noticeable impact on neural network accuracy, and on the other side to get important benefits in terms of tuning of operating conditions (endurance, energy), opening the way to on-chip learning.

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