A high precision TDC design based on FPGA+ARM

MengDi Zhang\textsuperscript{1,2,3}, HuaChuang Wang\textsuperscript{1,2*}, Bo Liu\textsuperscript{1,2}

\textsuperscript{1}Key laboratory of space optoelectronic precision measurement technology, CAS;
\textsuperscript{2}Institute of Optics and Electronics, Chinese Academy of Sciences, Chengdu 610209, China;
\textsuperscript{3}University of Chinese Academy of Sciences, Beijing 100049, China
*Corresponding author’s e-mail: wanghuachuang@163.com

Abstract. In this paper, a high precision time digital converter (TDC) is designed based on FPGA and ARM. It includes coarse module, delay chain module, look-up-table module, ringosc module and spi module in the FPGA chip. The ARM chip is used for reading the timestamp and printing through the serial port. The key technology of this design is using the CARRY4 block of Xilinx Artix-7 series to construct a delay chain for fine count. The system clock is used as the coarse count. The timestamp is obtained by the combination of fine time and coarse time. In addition, the precision of TDC is improved by code density test. The experiment result shows that precision of TDC is 43.2 ps.

1. Introduction
Precision time measurement is widely used in lidar, range finders, drones and robotics, advanced driver and assistance system (ADAS), collision detection systems, flow meters and other fields. The measurement precision is closely related to the technical level of these fields. Time to digital converter is a basic means of time interval measurement.

There are several approaches to implement TDC design. Most of them are based on Application Specific Integarted Circuits (ASICs) and FPGA. Compared with ASIC-TDC, TDC designed by FPGA has the advantages of low cost, high flexibility and short design cycle, which is more and more popular among researchers. Traditionally, TDC designs have been implemented using direct counting. However, in order to obtain a TDC with a resolution below 1 ns, a system clock with a GHz bandwidth is required, this solution is not feasible in most currently available FGPA\textsuperscript{s}.\footnote{In 2008, the optimization algorithm of Wave Union A and Wave Union B proposed by wu jinyuan of fermillaboratories in the United States verified the single-channel TDC accuracy of 25 ps and 10 ps on Cyclone II FPGA.\textsuperscript{5} In 2014, J. Torres used CARRY4 as the delay unit, and implemented a 24-channel TDC design on the Xilinx KC705 board with an RMS accuracy of 22.7 ps.\textsuperscript{1}}

The possibility of implementing high precision TDC on FGPA\textsuperscript{s} has already been demonstrated.\footnote{In 2008, the optimization algorithm of Wave Union A and Wave Union B proposed by wu jinyuan of fermillaboratories in the United States verified the single-channel TDC accuracy of 25 ps and 10 ps on Cyclone II FPGA.\textsuperscript{5} In 2014, J. Torres used CARRY4 as the delay unit, and implemented a 24-channel TDC design on the Xilinx KC705 board with an RMS accuracy of 22.7 ps.\textsuperscript{1}}

Carry chain design has great advantages of high precision and resolution, but there are some key technical problems to be solved. Firstly, it is difficult to construct a delay chain. Secondly, the delay time is non-linear due to the “look ahead” feature of the carry chain and it is influenced by temperature and voltage, so it is necessary to calibration TDC.
2. Measure Principle

TDC measurement principle is shown in figure 1, \( t_0 \) is the initial time of TDC and \( t_1 \) is the timestamp of channel 1 signal, \( t_2 \) is the timestamp of channel 2. \( N_1 \) is the coarse count of channel 1 and \( N_2 \) is the coarse count of channel 2. \( T_1 \) is the fine time of channel 1 and \( T_2 \) is the fine time of channel 2. The time interval between channel 1 and channel 2 can be expressed as:

\[
\Delta T = t_2 - t_1 = (N_2 - N_1)gT_{clk} + (T_2 - T_1) \tag{1}
\]

![Figure 1. Measure principle](image)

Coarse count is generally realized by the 25bit 125MHz system clock, which can enable TDC to obtain a larger dynamic range of measurement, and then combine with the fine measurement techniques to measure the time interval of less than one clock cycle. In this paper, TDC adopts the carry chain for the fine count.

3. TDC Structure and implementation

Figure 2 is the structure diagram of the TDC. The whole TDC measurement system can be divided into three parts: coarse measurement module, fine measurement module, ARM control module.

![Figure 2. TDC structure](image)
3.1 Coarse module

The oscillator with a jitter of 20 ppm is used as the system clock for coarse count. When the time range is larger and larger, the accuracy of coarse time will be worse and worse. The widths of which are 25 bits, and the system clock cycle is 8ns, so the dynamic range is 268ms.

3.2 Fine measure module

The fine measurement module uses CARRY4 primitive as carry chain in Artix-7 device for fine count. We use four MUXCY in the every CARRY4 module as the delay unit. Once the position of the first CARRY4 is constrained, 124 CARRY4 will be distributed inside the chip in a cascade mode. The fine time measurement is obtained by injecting the signal into the tapped delay line which gives a measurement analogous to a thermometer after the taps are sampled by D flip-flops. The D-flip-flops in carry chain adopts adjacent D-flip-flops in slice to ensure that the output signal of each delay unit can be sampled by the global clock consistently. In order to avoid metastable phenomenon, two-stage D flip-flops is used to store data. Then, the encoder converts the thermometer code locked by D-flip-flops into binary code, and the fine count can be obtained. Finally, the fine time is obtained by the average calibration test or the code density test.

According to the paper[3], the average calibration will bring great error, and the code density calibration can improve the precision. Before measurement, a ring oscillator based on 31 NOT gates generates a calibration signal. This signal is independent of the oscillator and the carry chain. The calibration signal enters the delay chain to obtain the binary code of the fine time. It can be seen from equation 2 that if there are enough random signals then the delay time is proportional to the number of events. The histogram composed of RAM can be used to estimate the delay time of the delay unit.

N_i the number of hits in the histogram at output n, N is the total number of hits in the histogram, \( T_{CLK} \) is the system clock period, then the delay time \( \tau_i \) of each delay unit is:

\[
\tau_i = \frac{N_i}{N} g T_{clk} \quad (2)
\]

So the fine count \( T_i \) can be expressed as

\[
T_i = \tau_1 + \tau_2 + L + \tau_i \quad (3)
\]

After 200000 calibration signals are accumulated in the sampling times of each delay unit, the calibration signal is stopped and the discrete histogram of each delay unit is obtained. As figure 4 shows, delay of delay units obtain from chipscope. For the system clock period of 8 ns, the last tap reached was 461, which means that the accumulated delay corresponds, precisely, to the system clock period. At the beginning of measurement, we only need to find the delay time of the corresponding delay unit to get the fine time.

![Figure 3. Dealy of every unit](image-url)
3.3 ARM control module
The TDC module in FPGA is encapsulated into a core, which is suspended on the wishbone bus as a slave, and SPI module is added in FPGA as a host interface, which is also suspended on the wishbone bus, so that the SPI module and TDC module are bridged on the wishbone bus. At the same time, the SPI module leads out MISO, MOSI, CS, CLK and ARM for interactive communication. ARM software can read the register values of Coarse Count and fine count in TDC core, and display the timestamp. Wishbone bus communication protocol is handshake protocol, which can effectively process cross clock signals.

4. TDC measure
As shown in figure 4, the signal generator is used to generate two signals to be tested, signal1 and signal2. The time interval between the rising edge of the two signals to be tested is 66.66ns. The two signals to be tested are transferred from two equal BNC to SMA lines into the FPGA board. Two timestamps can be seen in keil’s debugging interface, and the difference between the two timestamps can be printed out through serial port for data analysis.

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The experimental results in Figure 5 show that the approximate distribution of the timestamp difference between channel 1 and channel 2 is 66.922ns, the accuracy is 43.2ps, and the Gaussian distribution of the error peak value is 297ps. It can be seen that there is a fixed delay of 262ps, which is caused by the difference between the fixed line delay of two signals to be tested from the IO port of FPGA to the delay chain.

Figure 5. Measure Result
5. Conclusion

Based on FPGA + ARM, a high-precision TDC design is completed. Aiming at the nonlinearity of the delay unit on the delay chain in the channel, the code density calibration test is used to calibrate the fine time. The experimental results show that the dynamic range is 268ms and precision is 43.2ps. It can meet the demand of large range and high precision pulse laser ranging and provide some practical value for lidar ranging.

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