Analysis and comparison of 13 level inverter topology

K. Dhineshkumar. 1 C. Subramani 2 G. Prakash 3
1 Department of EEE, Agni College of Technology, Thalambur, Chennai-600130
2 Department of Electrical and Electronics Engineering, SRM Institute of Science and
Technology, Kancheepuram 603203, India.
3 Department of EEE, Srisairam Institute of Technology, Chennai
*csmsrm@gmail.com

Abstract: In this paper distinctive topology of 13 level inverter has been analyzed with various
number of switches. In traditional topologies more number of switches and it can be decreased by
planning the diverse topologies the distinctive topology dissected and looked at .this proposed
topology gives the better outcomes. This can be utilized as a part of various inverter applications

1. Introduction
The virtue of more semiconductors there might be a probability of Some switch might be fizzle. The
business expecting immovable yield from the power segment. For that reason the calculation built up that
sidestep the denounce changes and endeavored to give unsurprising yield voltage and is exhibited in [1]. It
broke down 3 and 4 level inverter utilizing flying capacitor based chopper circuit arrangement. The
control figuring is utilized as a part of [2]

This structure utilizes a solitary dc Source and three stage transformer to get 13 level inverter. This
framework gives a Neutral clipped and capacitor adjusts Techniques. The control techniques executed for
16 bit little scale controller. The test reason utilized 1 KW light based board and utilized as a bit of PC and
AC systems. The effectiveness around 92% and examined in [3] inverter modules which are connected
with the sun energized photovoltaic sheets having climb to DC voltage degrees, the capacitor voltages
over the DC joins. The voltage and rehash of the multilevel inverter was balanced utilizing close circle
control, i.e., the most essential power stream to the cross area was capable even under changing
framework voltage. The execution of the total structure has been checked under various transient state is
appeared in [4] This examination talked about around a profitable PWM exchanging limit as for adjusted
H-interface based multilevel inverter and it expanded the measure of yield voltage levels by including
switch areas and dc input voltage sources. In the event that it utilizes seven switches and three dc sources,
the measure of yield voltage winds up without a doubt seven. Notwithstanding the way that its THD
characteristics have been enhanced, it needs yield channel to meet general yield voltage THD basic, i.e.,
5% below. To coordinate this issue, we proposed a beneficial PWM exchanging strategy for the earlier H-
relate based multilevel inverter and by the utilization of this, it joined more sinusoidal waveform.[5] This
layout showed another multilevel time period width-change (PWM) inverter think up for the use of remain
particular photovoltaic structures. It incorporates a PWM inverter, a get-together of LEVEL inverters,
making staircase yield voltages, and fell transformers. Operational standards and examination had been depicted all the way. The realness of the proposed framework was checked through PC maintained augmentations and test happens utilizing models conveying yield voltages of a 11 level and a 29 level, freely, and their outcomes are separated and regular accessories is shown in [6].

Another topology for a solitary stage fell H-interface multilevel inverter (CHB MLI) with a concentration to diminish the measure of essentialness exchanging contraptions in the way for the surge of current. It permitted a Multicarrier Modulation (MCPWM) way to deal with the way toward making the beats for organizing the PWM yield voltage. The use of a more little of changes to achieve the yield voltage demonstrated cases the cutoff of the consider outlining to widen the level of the CHBMLI is shown in [7]. This combination of half and half arrange air beat width change approach fitting for fell multilevel inverter. A cream PDPWM had been made in context of low rehash PWM and high rehash sinusoidal PWM. A streamlined dynamic exchanging configuration was comfortable in this technique with adjust electro static and electro engaging worry among the power gadgets. Also, the mutt PDPWM offered better consonant execution emerged from its standard PWM accessory. Proliferation happens have been united into this examination to acknowledge the possibility of the appeared in [8].

The CHB topology to refresh the execution of indicated topology another change method had been acknowledged and this alters technique passed on smallest voltage THD (5.270%) with overhauled RMS voltage (86.52 V) at the store side another cross breed topology with u-shape control system had been finished in ask about office based test arrange and the outcomes were supported in. [9]

2. Proposed topologies comparison

![Figure 1. The proposed system of multilevel inverter with 9 switches](image)

The proposed circuit diagram for the 13 level inverter with 9 switches and which has one h bridge and 5along with one leg connected as shown in the figure 1
Figure 2. The proposed system of multilevel inverter with 8 switches

The figure shows the The s-type PV based 13 level symmetric Multilevel inverter as shown in the figure 4. The proposed topology has 8 switches whereas conventional topologies has 10 switches, and hence thermal stress and operating time of this circuit better than the conventional systems. This system uses basic pulse width modulation as a switching the switches.

Different modes of operation of Proposed Multilevel inverter as explained in step by step as explained.

The S-Type PV based 13-level multilevel inverter has 11 Modes of operation for both positive and negative half cycle, the output voltages are \( V_{dc}, 2V_{dc}, 3V_{dc}, 4V_{dc}, 5V_{dc}, 6V_{dc}, -V_{dc}, -3V_{dc}, -4V_{dc}, -5V_{dc}, -6V_{dc} \) are obtained. The operation of switches is illustrated in the Table 1. The 2 switch operated at a one mode.
Table 1. Switching table for 13 level multilevel inverter

The table 1 Shows the diverse methods of operation of Pulse example of the 13-level multilevel inverter and for every mode the two legs are works at the moment, and the relating voltage got from the extension

3. Different Modes of Operation

Different modes of operation of Proposed Multilevel inverter as explained in step by step as explained

The S-Type PV based 13-level multilevel inverter has 11 Modes of operation for both positive and negative half cycle, the output voltages are, \( V_{dc}, 2V_{dc}, 3V_{dc}, 4V_{dc}, 5V_{dc}, 6V_{dc}, 0, -V_{dc}, -3V_{dc}, -4V_{dc}, -5V_{dc}, -6V_{dc} \) are obtained. The operation of switches is illustrated in the Table 1. The 2 switch operated at a one mode

| Voltage | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 |
|---------|----|----|----|----|----|----|----|----|
| 6       | 1  | 0  | 1  | 0  | 0  | 0  | 0  | 0  |
| 5       | 1  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |
| 4       | 1  | 0  | 0  | 0  | 1  | 0  | 0  | 0  |
| 3       | 1  | 0  | 0  | 0  | 0  | 1  | 0  | 0  |
| 2       | 1  | 0  | 0  | 0  | 0  | 0  | 1  | 0  |
| 1       | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |
| 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| -1      | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 0  |
| -2      | 0  | 1  | 0  | 1  | 0  | 0  | 0  | 0  |
| -3      | 0  | 1  | 0  | 0  | 1  | 0  | 0  | 0  |
| -4      | 0  | 1  | 0  | 0  | 0  | 1  | 0  | 0  |
| -5      | 0  | 1  | 0  | 0  | 0  | 0  | 1  | 0  |
| -6      | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 1  |
Figure 3. Mode I operation of Proposed inverter (S1&S8 –ON)

In figure 3 the Switch S1 and S8 is ON uniting the heap positive terminal to ground and other controlled switch are OFF, The current path is (+Vs S 1, S 8, C7+Vs) . During the time The capacitor C7 is charging and Voltage +Vs/6 appears across the output voltage

Figure 4. Mode II operation of Proposed inverter (S1&S7 –ON)

In figure 4 the Switch S1 and S7 is ON uniting the heap positive terminal to ground and other controlled switch are OFF, The current path is (+Vs S 1, S 7, C6C7+Vs) . During the time The capacitor C6 and C7 is charging and Voltage +Vs/5 appears across the output voltage.

In figure 5 the Switch S1 and S6 is ON uniting the heap positive terminal to ground and other controlled switch are OFF, The current path is (+Vs S 1, S 6, C5C6C7+Vs) . During the time The capacitor C5, C6 and C7 is charging and Voltage +Vs/4 appears across the output voltage.
In figure 6 the switch S1 and S6 is ON uniting the heap positive terminal to ground and other controlled switch are OFF. The current path is (+VS, S1, S5, C6, C7, C5, +VS). During the time the capacitor C4, C5, C6 and C7 is charging and Voltage +VS/3 appears across the output voltage.

Figure 5. Mode III operation of Proposed inverter (S1&S6 –ON)

Figure 6. Mode IV operation of Proposed inverter (S1&S5 –ON)
In figure 7 the switch S1 and S6 is ON uniting the heap positive terminal to ground and other controlled switch are OFF. The current path is (+Vs, S1, S5, C6, C7, C5, -Vs). During the time the capacitor C3, C4, C5, C6 and C7 is charging and voltage +Vs/2 appears across the output voltage.

In figure 8 the switch S1 and S6 is ON uniting the heap positive terminal to ground and other controlled switch are OFF. The current path is (+Vs, S1, S5, C6, C7, C5, +Vs). During the time the capacitor C2, C3, C4, C5, C6 and C7 is charging and voltage +Vs appears across the output voltage.

In figure 8 the switch S1 and S6 is ON uniting the heap positive terminal to ground and other controlled switch are OFF. The current path is (+Vs, S1, S5, C6, C7, C5, +Vs). During the time the capacitor C2, C3, C4, C5, C6 and C7 is charging and voltage +Vs appears across the output voltage.
In figure 9 the switch S2 and S3 is ON uniting the heap Negative terminal to ground and other controlled switch are OFF. The current path is \((-V_s, -L, S_3, C_1, -V_s)\). During the time the capacitor \(C_2, C_3, C_4, C_5, C_6, \) and \(C_7\) is charging and Voltage \(-V_s/7\) appears across the output voltage.

In figure 10, similarly the switches S2, S4, S5, S6, S7, S8 are conduct periodically to obtain negative voltage stepped waveform of the Multi level inverter.

### 4. Results and discussion

#### 4.1 Simulation Proposed System

The simulation of proposed system with 13 level inverter with 9 switches, which uses sine PWM Technique as shown in the figure 11.

The simulation of PV based S-type multilevel inverter produced 13 level stepped waveforms \((V_{dc}, V_{dc}/2, V_{dc}/3, V_{dc}/4, V_{dc}/5, V_{dc}/6, 0, -V_{dc}, -V_{dc}/2, -V_{dc}/3, -V_{dc}/4, -V_{dc}/5, -V_{dc}/6)\) are obtained in
the proposed inverter as shown in the figure 12. This results indicates a reduced Total Harmonic Distortion.

Figure 11. proposed system with 13 level inverter with 9 switches

4.2. Output voltage wave form of the inverter

Figure 12. Simulation of thirteen level multilevel inverter with 9 switches
4.3 simulation of proposed system with reduced switches

The figure 13 shows the proposed system as solar based 13 level multilevel inverter with 8 switches and switches are reduced with respect to the first simulation as represented in figure 11.

Figure 13. Simulation of Proposed Multilevel inverter with 8 switches

Figure 14. Output voltage waveform of Simulation of thirteen level multilevel inverter with 8 switches
multilevel inverter produced 13 level stepped waveform $V_{dc}, V_{dc}/2, V_{dc}/3, V_{dc}/4, V_{dc}/5, V_{dc}/6, 0, -V_{dc}, -V_{dc}/2, -V_{dc}/3, -V_{dc}/4, -V_{dc}/5, -V_{dc}/6$ are obtained in the proposed inverter as shown in the figure 12 and 14.

5. Conclusion

This diverse topologies and are examinations and a portion of the topology contrasted and the recreation and proposed has les add up to consonant bending and les switches, The proposed topology can be utilized for every single numerous application.

References

[1] Amini J and Moallem M M 2016 A Fault-Diagnosis and Fault-Tolerant Control Scheme for Flying Capacitor Multilevel Inverters systems *IEEE Trans. on Power Electronics* 64 pp-1818-1826.
[2] Anshuman Shukla 2010 Arindam Ghosh Flying-Capacitor-Based Chopper Circuit for DC Capacitor Voltage Balancing in Diode-Clamped Multilevel Inverter *IEEE Transactions on Industrial Electronics* 57 pp 2249 – 2261.
[3] Ismael Araujo-Vargas and Kevin Cano-Pulido, Jazmin Ramirez-Hernandez; Nancy Mondragon-Escamilla; Caren-Ivet Nicolas-Villalva 2014 A Single DC-Source Seven-Level Inverter for Utility Equipment of Metro Railway, Power-Land Substation *IEEE Transactions on Industry Applications* 50, pp-3876 - 3892.
[4] Jana Chandra Kartick, Biswas K. Sujit, Kar Chowdhury Suparna 2016 Dual reference phase shifted pulse width modulation technique for a N-level inverter based grid connected solar photovoltaic system *IET Renewable Power Generation* 10, pp-928 – 935.
[5] Won-Kyun Choi, Feel-soon Kang 2009 H-bridge based multilevel inverter using PWM switching function *IEEE International Telecommunications Energy Conference* 18-22.
[6] Feel-Soon Kang, Sung-Jun Park, Su Eog Cho, T.Ise 2005 Multilevel PWM inverters suitable for the use of stand-alone photovoltaic power systems *IEEE Transactions on Energy Conversion*, 20, PP-906-915.
[7] S Usha, C Subramani, A Geetha, 2018, “Performance Analysis of H-bridge and T-Bridge Multilevel Inverters for Harmonics Reduction” *International Journal of Power Electronics and Drive Systems*, 9 (1), pp:231-239.
[8] Jayaprakash Sabarad, and Kulkarni G H 2015 Comparative Analysis of SVPWM and SPWM Techniques for Multilevel Inverter” *Power and Advanced Control Engineering (ICPACE)*, *IEEE Xplore* 27 pp-232-237.
[9] K. Dhinesh kumar, C. Subramani, G. Prakash, 2018, ‘Kalman Filter Algorithm for Mitigation of Power System Harmonics’ *International Journal of Electrical and Computer Engineering*, 8(2), pp:771-779, April 2018