Exploiting the electrothermal timescale in PrMnO$_3$ RRAM for a compact, clock-less neuron exhibiting biological spiking patterns

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Abstract

Spiking neural networks (SNNs) are gaining widespread momentum in the field of neuromorphic computing. These network systems integrated with neurons and synapses provide computational efficiency by mimicking the human brain. It is desired to incorporate the biological neuronal dynamics, including complex spiking patterns which represent diverse brain activities within the neural networks. Earlier hardware realization of neurons was (a) area intensive because of large capacitors in the circuit design, (b) neuronal spiking patterns were demonstrated with clocked neurons at the device level. To achieve more realistic biological neuron spiking behavior, emerging memristive devices are considered promising alternatives. In this paper, we propose, PrMnO$_3$ (PMO)-resistive random-access memory (RRAM) device-based neuron. The voltage-controlled electrothermal timescales of the compact PMO RRAM device replace the electrical timescales of charging a large capacitor. The electrothermal timescale is used to implement an integration block with multiple voltage-controlled timescales coupled with a refractory block to generate biological neuronal dynamics. Here, first, a Verilog-A implementation of the thermal device model is demonstrated, which captures the current-temperature dynamics of the PMO device. Second, a driving circuitry is designed to mimic different spiking patterns of cortical neurons, including intrinsic bursting and chattering. Third, a neuron circuit model is simulated, which includes the PMO RRAM device model and the driving circuitry to demonstrate the asynchronous neuron behavior. Finally, a hardware-software hybrid analysis is done in which the PMO RRAM device is experimentally characterized to mimic neuron spiking dynamics. The work presents a realizable and more biologically comparable hardware-efficient solution for large-scale SNNs.

Keywords: PrMnO$_3$ (PMO), RRAM, neuron spiking patterns, spiking neural network (SNN)

(Some figures may appear in colour only in the online journal)

1. Introduction

A spiking neural network (SNN) mimics the human brain to perform complex computations. The ability to perform tasks parallelly, along with low power consumption, gives SNN an edge over traditional von Neumann architecture, which is limited by the von Neumann bottleneck. The human brain consists of two main components; a neuron, which fires according to the input signal, and a synapse, which interconnects two neurons. Whenever a neuron receives a stimulus, it integrates the input signal to its membrane potential. Once the membrane
potential reaches a threshold, it falls back down to low levels, exhibiting a spike. The spike timing of the neuron and the strength of the synapse are crucial for information processing. As illustrated in figure 1, a neuron can exhibit different spiking patterns, and each spiking pattern plays a unique role in the functioning of the brain [1]. For example, neurons that exhibit ‘Tonic Bursting’ are thought to be responsible for the ‘Gamma Wave Oscillations’ in the brain. Some neurons are also used for concentration gradient computations in chemotaxis in C. elegans, which is used to translate from biology to algorithms [2]. Since the biological neurons exhibit a rich variety of spiking patterns, we need artificial neurons which mimic these spiking patterns to build SNNs which can perform a wider variety of tasks (figure 1). Further, the refractory period occurs after spiking when the neuron is quiescent and does not effectively integrate inputs. The tuning of the refractory period is another critical element of the neuron to control the dynamics of brain waves [3] and navigational circuits [2]. Thus, the neuron has various timescales—both during spiking and refractory phases.

Previously, many mathematical models of the neuron have demonstrated different spiking patterns of the cortical neuron. A popular model has been the Izhikevich Model, which is biologically plausible and computationally efficient [4]. While such models help study large-scale SNNs in a simulation environment and providing us insights into brain functioning, they are not useful for hardware implementation of SNNs. For hardware realization of SNNs, we need devices that mimic different spiking patterns of the neuron while being area efficient and consuming less power.

Various device-based neurons have been demonstrated [5–10]. Here, the ‘integration’ operation is implemented by charging the external capacitor. The size of the capacitor and the input determine the spiking frequency, and to show different integration timescales, the area of the capacitor needs to be changed. Also, these neurons consume a large area, making the large-scale implementation of SNNs challenging especially when realizing longer real-world signal timescales (e.g. speech). Different spiking patterns have also been implemented using digital circuitry [11]. The implementation can demonstrate a wide range of spiking patterns while being biologically plausible. However, the circuitry of a single neuron is complex as it involves multiple buffers, counters, multiplexers, and pipelines (which consist of adders), and the implementation is clocked. It shows an implementation for a small SNN, but for bigger SNNs, the resulting digital circuitry will be large and complex.

Recently, resistive random-access memory (RRAM) based implementation of neurons was demonstrated, which utilized the internal timescales of the RRAM device (either gradual resistive switching or electrothermal timescale) to perform the integration operation, which eliminated the need of using an external capacitor [12, 13]. Specifically, a Pr$_{1−x}$Ca$_x$MnO$_3$ (PCMO) based RRAM device was proposed to implement an integrate and fire (IF) neuron [12]. The paper also demonstrated different spiking patterns, such as intrinsically bursting (IB), and chattering (CH) patterns. Also, the neuron utilized the internal timescale of resistive switching to perform integration operation. The PCMO RRAM can show different conductance levels and exhibits different spiking frequencies for these different conductance levels. These two features eliminated the need for an external capacitor. The major disadvantages of the PCMO RRAM neuron implementation were that the neuron did not exhibit a ‘Leaky’ behavior, which is integral to the functioning of a biological neuron, and it utilizes a clock to operate, whereas human brains do not use a clock [14].

A PrMnO$_3$ (PMO) RRAM-based leaky IF (LIF) neuron was demonstrated experimentally [13]. PMO-based RRAM devices are non-filamentary and highly scalable, making them attractive for compact neurons. Here, the internal electrothermal timescales in PMO material were used to perform integration, eliminating the use of an external capacitor. The PMO RRAM-based neuron was asynchronous and demonstrated only a single spiking pattern.

In this paper, we demonstrate an asynchronous, capacitor-free, PMO RRAM-based neuron that can exhibit different spiking patterns of a cortical neuron. The neuron utilizes the multiple voltage-controlled electrothermal timescales of PMO RRAM to construct an integration block coupled to a refractory block to enable a compact capacitor-free timescale control. We propose a simulation setup consisting of a physics-based Verilog-A model of the RRAM, and a behaviorally modeled driving circuit, to model and predict different spiking patterns. The voltage across the device from the simulation setup is extracted, approximated, and applied across the PMO RRAM to experimentally demonstrate the different biological spiking patterns. The work provides a strategy to investigate different biological spiking patterns in simulations as well as experimentally in area-efficient memristor-based synaptic arrays.

2. Device details

The stack of PMO-based RRAM is as shown in figure 2(a). The silicon (Si) substrate is used for RRAM fabrication. SiO$_2$ is thermally grown on the Si wafer followed by deposition of a bilayer of titanium (Ti) followed by platinum (Pt) deposited through DC sputtering. A blanket layer of PMO film (60 nm) is then deposited using RF sputtering at room temperature. The PMO film is annealed in O$_2$ ambient at 750 °C for 30 s. Finally,
3. Electrothermal RRAM device model

To capture the device’s current-temperature dynamics, an electrothermal model is demonstrated. The current is calculated using the analytical model shown in equations (1)–(3), and the temperature is calculated using equation (4) [15]

\[ I = I_{\text{Ohmic}} + I_{\text{SCLC}} \] (1)

\[ I_{\text{Ohmic}} = qA\mu N_e \left( \frac{T}{T_{\text{amb}}} \right)^{3/2} e^{-\frac{\phi_B}{kT}} \left( \frac{V}{L} \right) \] (2)

\[ I_{\text{SCLC}} = A\mu\epsilon_o\epsilon_{\text{PMO}} \left( \frac{N_e}{N_T} \right) \left( \frac{T}{T_{\text{amb}}} \right)^{3/2} e^{-\frac{E_{\text{trap}}}{kT}} \left( \frac{V^2}{L^3} \right) \] (3)

\[ \frac{T - T_{\text{amb}}}{R_{\text{th}}} + C_{\text{th}} \frac{dT}{dt} = IV. \] (4)

The equations are modeled in Verilog-A and simulated in Cadence Virtuoso. The flowchart for the model is as shown in figure 3. The model is initialized by setting the temperature as ambient temperature (300 K) and applying voltage bias. Using equations (1)–(4), temperature and current are solved self-consistently.

The equivalent thermal coefficients are \( R_{\text{th}} \) (thermal resistance) and \( C_{\text{th}} \) (thermal capacitance). Here, the temperature \( T \) is an ‘effective’ temperature of the device. Figures 4(a) and (b) show the transient currents for experiments and simulations for different applied voltages. The spike time of the model is calibrated to match those of experiments, and the results are shown in figure 4(c). The parameters used in simulations are mentioned in table 1.

4. Input voltage dependent electrothermal timescale control

As shown in the flowchart figure 3, current and temperature are dependent quantities. Therefore, with an increase in current, temperature increases, which further increases the current. The positive feedback between current and temperature results in a current shoot-up. A constant voltage pulse of different magnitudes is applied across the device, and the current through the device is observed (figure 4). The time for the current to shoot up and reach the compliance depends upon the applied voltage. Thus, a higher voltage will trigger a faster shoot-up, and a lower voltage will slow down the current shoot-up. The current-temperature time dynamic is used as an integration timescale in the proposed PMO RRAM-based neuron.
5. Circuit implementation

5.1. Exhibiting different spiking patterns

Biological neurons are capable of exhibiting different spiking patterns. To mimic that behavior in hardware using RRAM, the following circuit concept and operation are proposed. A neuron integrates the input with a timescale to raise its membrane potential, and a spike is issued when a threshold is reached. The spike patterns are characterized by the position- ing of spikes or spike timings for constant input. A neuron can generate spike patterns by using the electrothermal timescale for integration controlled by the input voltage, which is slowly time-varying input from synapses. Complex biological spiking patterns can be generated by modulating the input voltage applied either directly or with an additional resistive drop across RRAM based on an internal binary state variable of the neuron to modulate the integration timescales dynamically. Further, the refractory period control is enabled by coupling another RRAM block to the integration block—whose electrothermal timescale is voltage-controlled.

To enable the above operation, the driver circuit shown in figure 5 is proposed. The circuit is capable of showing different spiking patterns. The working of each component is explained below. RRAM is referred to as $R_D$.

5.1.1. Resetting switch ($S_1, S_2$). The switches $S_1, S_2$ are used to connect or disconnect the voltage source from the RRAM. If the input to the switch is 0, the switch is closed, connecting the input voltage to the RRAM. If the input to the switch is 1, the switch is opened, disconnecting the input voltage from RRAM.

5.1.2. Series resistor ($R_S$). A series resistor ($R_S$) is connected in series with the RRAM. The voltage drop across $R_S$ ($V_A$) is linearly dependent on the current through RRAM. If the current exceeds a threshold, so does $V_A$. The voltage $V_A$ is used to detect spikes.

5.1.3. 4-bit register (register 1). A register is implemented, which stores a sequence of 1s and 0s according to the desired spiking pattern. For example, the register would initially store 1110 bits for the CH pattern, which will lead to three spikes with a smaller spike time and one with a larger spike time. It requires a trigger signal to perform the left-shift operation, which it receives from the voltage $V_A$ once the neuron has fired.

5.1.4. Control resistor ($R_C$). Control Resistor has two states; it either acts as a short circuit (SC) or as a resistor. When $R_C$ acts as a SC, the input voltage drops across the $(S_1 + R_{D1} + R_{S1})$ network. When $R_C$ acts as a resistor, a reduced voltage drops across the $(S_1 + R_{D1} + R_{S1})$ network. The most significant bit (MSB) of the register 1 controls the state of the $R_C$; if MSB = 1, $R_C$ acts as a SC, and if MSB = 0, $R_C$ acts as a resistor.

5.1.5. Refractory block. In a biological neuron, after a neuron has fired, it does not respond to the external stimulus for a period called the ‘Refractory Period.’ On a circuit level, control over this refractory period is desirable. The driving circuit consists of two neurons; one neuron (in the integration block) is driven by the input signal, and the second neuron (in the refractory block) is driven by a constant voltage signal which controls the refractory period.

5.1.6. Toggle block. The toggle block ensures that either the Integration Block or the Refractory block stays active at a given time. The toggle block has an OR gate, which detects if either of the neurons has spiked via voltage $V_{A1}$, and a 2 bit register (Register 2) whose MSB controls the switches $S_1$ and $S_2$. Once a neuron has fired, the 2 bit register performs a left
shift operation and flips the MSB bit (as only 0 and 1 is stored, and MSB is connected back to least significant bit (LSB)). This disconnects the neuron which has fired from the voltage source and reconnects the other neuron to its voltage supply. This operation of switching between two blocks is repeated as long as the neuron spikes.

In figure 6, a state diagram and a timing diagram is demonstrated, which explains the interplay between the input neuron and the refractory neuron. The state diagram does not include the 4 bit register and the control resistor for simplicity. Either the Neuron N1 or N2 remains ON at any given time. The input to the N2 neuron is chosen such that it will always elicit a spike. Once N1 fires, N1 turns OFF and turns ON N2, and vice versa. After N1 has fired, it will stay OFF for a duration equal to the spike time of the N2 neuron, achieving a refractory period. During this duration, N1 will not perform any integration operation. In figure 7, a flowchart is demonstrated which explains the working of the neuron to exhibit different spiking patterns. The flow chart does not include the refractory block for simplicity. Initially, the input pulse voltage is applied, S1 is closed, and \( R_C \) acts as a SC. \( V_{in} \) is applied to RRAM, and current is computed according to the RRAM electrothermal model. If the voltage at node A (\( V_A \)) exceeds the threshold voltage (\( V_{th} \)), registers 1 and 2 detect the event and perform a left shift operation. For register 1, if MSB = 1, \( R_C \) acts as SC, else acts as a resistor. For register 2, if MSB = 1, S1 opens up, else closes. To achieve different spiking patterns, a different set of bits are stored in the register. All transitions...
occur asynchronously, without a need for an external global clock.

6. Simulation results and discussion

The components of the driving circuit shown in figure 5 are modeled behaviorally in Verilog-A, and the circuit simulations are performed in Cadence Virtuoso. The simulation results are presented and discussed below.

6.1. Voltage controlled spiking frequency

Figure 8 shows the simulation results for $V_{\text{input}} = -1.6$ V and $V_{\text{input}} = -1.8$ V. As explained in section 4, high input voltage leads to a higher spiking frequency and vice versa.

6.2. Voltage controlled refractory period

Figure 9 shows the simulation results for $V_{\text{input}} = -2.2$ V, and a refractory period of 200 ns and 400 ns provided by the refractory neuron. A high input voltage to the refractory neuron ($V_{\text{refractory}}$) leads to a smaller refractory period, and a small voltage leads to a longer refractory period. Different voltages modulate the electrothermal timescales of the refractory neuron and hence the spike timing of the refractory neuron. As spike timing of refractory neuron controls the refractory period of the input neuron, $V_{\text{refractory}}$ controls the refractory period.

6.3. Time varying input

The circuit shown in figure 5 is used for demonstration, with the control resistor and the register (register 1) removed. Two sinusoids with frequency = 250 KHz, and 350 KHz, voltage amplitude = $-0.7$ V, and the DC voltage level = $-0.7$ V are superimposed and applied as an input to the circuit. The resulting input signal has two regions with high voltage, two regions with moderate voltage, and two regions with low voltage. Figure 10 shows the simulation results. The high voltage region leads to a fast and dense spiking, the moderate voltage region leads to a slower and sparsely distributed spiking, while the low voltage region does not issue a single spike. The output behavior is attributed to the transient Joule heating mechanism in the device. When the voltage is low, the thermal feedback within the device is not established, hence no current shoot-up, resulting in no spikes. As the voltage is increased, the positive feedback builds up, current levels rise, and spiking patterns are observed.

6.4. Different spiking patterns

The circuit shown in figure 5 is used. For demonstration, IB and CH patterns are simulated and the results are shown in...
To achieve CH and IB spiking patterns, bits 1110 are stored in the register. For CH spiking pattern, MSB and LSB are connected to one another, whereas for the IB spiking pattern, MSB and LSB are disconnected from one another. A high voltage is applied at the input terminal. Initial MSB = 1 ensures that the control resistor acts as a switch, and the voltage drops across the $R_{D1}$. Once a spike is issued, the switch S1 opens up, disconnecting $R_{D1}$ from the input voltage source, and voltage $V_A$ triggers the register 1 to left shifts its contents. Once the spike is over, the register holds 1101 (for CH) and 1100 (for IB). The next two spikes will elicit a similar current response of faster spikes. At the end of the three spikes, the contents of the register would be 0111 (for CH) and 0000 (for IB). MSB = 0 forces the control resistor to act as a resistor, reducing the voltage drop across the RRAM. Lower voltage drops lead to a longer spike time. After the spike corresponding to MSB = 0 is issued, the next MSB is either 1 or 0, depending on the desired spiking pattern.

7. Experimental results

7.1. Experimental setup

The DC-IV measurements are performed using the Agilent B1500 semiconductor analyzer, while the transient measurements are performed using the B1530 waveform generator/ fast measurement unit. All the measurements are done at room temperature. To observe the spiking patterns in PMO RRAM device, waveforms of the voltage signals across the RRAM device from simulations are approximated and applied to the RRAM device during experiments.

7.2. Results and discussion

7.2.1. Voltage controlled spiking frequency. The response of the neuron with a pulsed input voltage is presented in figure 12. The current response is shown for two different voltages $V_{input} = -1.6$ V and $V_{input} = -1.8$ V, and it can be observed that the higher voltage led to faster spiking and vice versa. Figure 12(c) shows numerical of spiking frequency vs input voltage between the simulations and experiments. The average error is 4.4%.

7.2.2. Time-varying input. The same voltage signal as that in the simulation of the time-varying input signal (figure 10) is applied to the RRAM device. Voltage is reduced to 0 wherever necessary to mimic the resetting behavior. The results are presented in figure 13. The current response of the neuron shows dense spiking for high voltages, sparse spiking for moderate, and no spiking for low voltages. The experimental results corroborate the simulation results (figure 10).

7.2.3. Different spiking patterns. The CH and IB patterns are demonstrated experimentally and the results are presented in figure 14. To observe CH behavior, three consecutive pulses of $V = -2.4$ V and a single pulse of $V = -1.7$ V are applied alternatively to the RRAM. To observe IB behavior, three consecutive pulses of $V = -2.4$ V are applied to the RRAM, followed by consecutive pulses of $V = -1.9$ V. The spiking patterns obtained experimentally qualitatively align with the simulation results (figure 11).
Figure 13. Experimental spiking pattern for time varying input: input voltage is combination of two time-varying sinusoidal signals of equal magnitude and different frequencies.

Figure 14. Experimental spiking patterns (a) intrinsic bursting (b) chattering.

8. Relative compactness of electrothermal vs. RC based timescale implementation

Figure 15 shows two different implementations of a neuron using RRAM. Previously, RRAM has been used as a switching element only [18, 19] (figure 15(a)). It has two resistance states with which the electrical capacitor either charges or discharges. In such neurons, the capacitor performs integration with an electrical timescale. The RRAM switching has its own timescale, which depends on the switching mechanism, e.g. insulator to metal transition (IMT) or self-heating. The relatively longer electrothermal RRAM switching timescales are proposed in this paper to replace the large electrical capacitors for integration functionality.

The electrothermal timescale from the 10 µm × 10 µm RRAM is experimentally shown as 100 ns–1 µs with a max current of 10 mA. To implement an electrical RC timescale, assuming a 2 nm thick SiO₂ based capacitor of the same area will produce capacitance of 1.7 pF, which results in a time constant of 0.1 ns for a 1 V threshold for firing. This is a 100–1000× smaller timescale. For an equivalent timescale of 100 ns–1 µs, a 100–1000× larger area capacitor is needed with the same RRAM size to adversely affect area efficiency.

Figure 15. (a) RRAM based neuron where RRAM device acts as a switching element and integration timescale is controlled by the external capacitor, (b) proposed RRAM based neuron where RRAM device provides the electrothermal integration timescale in addition to being a switch.

As devices scale, the electrical-time constant is largely area independent—given by the following:

\[ \tau_{RC} = \frac{CV}{I} = \frac{\epsilon A}{d} \cdot \frac{V}{J_D A} = \frac{\epsilon V}{d J_D} \]  

(5)

where \( C \) is electrical capacitance which depends on dielectric constant \( \epsilon \), the thickness of insulator \( d \), and capacitor area \( A \), \( V \) is the threshold voltage, \( I \) is charging current through the RRAM, which depends on the switching current density \( J_D \) and area \( A \) assumed to be the same as the capacitor. The electrothermal timescale is also approximately scaling independent and is given by the following:

\[ \tau_{th} = \frac{C_{th} \Delta T}{H} = C_r A L \cdot \frac{\Delta T}{V J_D A L} = (C_r) \cdot \frac{\Delta T}{V J_D} \]  

(6)

where \( C_{th} \) is thermal capacitance, which depends upon specific heat capacity \( C_r \), area of device \( A \), and the thickness of the device, \( L \), \( \Delta T \) is a change in device temperature. So, the ratio of the timescale benefit will remain approximately constant. This largely sustains the large area efficiency with scaling.

9. Conclusion

In summary, we demonstrate different spiking patterns of a cortical neuron using a PMO RRAM-based neuron. The benchmarking of the PMO-based neuron circuit is shown in table 2. In the proposed circuit, 6 bit register consisting of six flip flops, one OR gate, two switches, and three transistors for one resistor will be used, with a total transistor count of 119, based on which a feature size of 11.9 × 10³ F² is estimated. The neuron implementation shown in this paper is capacitor-less as PMO RRAM uses the internal self-heating timescales for integration operation and hence eliminates the use of a capacitor. Unlike previous demonstrations, an asynchronous simulation-based analysis with the driving circuitry and electrothermal model of the PMO RRAM device demonstrated realistic bursting patterns. Experiments guided by simulations validate the simulation results. With scalable PMO
### Table 2. Benchmarking with previous Neuron implementations

| Platform       | Wijekoon [7] | Joubert [8] | Tuma [20] | Dutta [10] | Lashkare [12] | Lashkare [13] | Gao [18] | Shukla [19] | This Work |
|----------------|--------------|-------------|-----------|-----------|---------------|---------------|----------|-------------|-----------|
| Circuit Type   | Analog + Asynch  | Digital + Synch. | Mixed + Synch. | Analog + Asynch. | Mixed + Synch. | Mixed + Asynch. | —        | —          | PMO + CMOS |
| Neuron Model   | LIF          | LIF         | IF        | LIF        | LIF           | LIF           | —        | —          | Mixed + Asynch. |
| Spiking        | RS, FS, IB, CH | RS         | RS        | RS         | RS            | RS            | —        | —          | RS, IB, CH |
| Behavior*      | Fixed        | Fixed       | Fixed     | Fixed      | Fixed         | Fixed         | —        | —          | Control   |
| Refractory     | Cap          | Cap         | —         | Floating Body Effect | Gradual Resistive Switching | Electro-thermal | Cap      | Cap         | Electro-thermal |
| Period         |              |             |           |            |               |               |          |             |           |
| Timescale      |              |             |           |            |               |               |          |             |           |
| Generation     |              |             |           |            |               |               |          |             |           |
| RRAM Usage     | —            | —           | —         | Integrator  | Integrator    | Switch        | Switch   | —           | —         |
| Area ($\times 10^3 F^2$) | 23          | 127         | 2551      | 1.767      | 3.086         | —             | —        | —           | 11.908    |

Notes: Green represents superior, Red represents inferior, and Yellow represents acceptable.
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RRAM devices integrated with digital components for the driving circuit, a compact neuron can be designed, which is highly attractive for large-scale SNNs.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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