High-Throughput FPGA-based QC-LDPC Decoder Architecture

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Abstract—We propose without loss of generality strategies to achieve a high-throughput FPGA-based architecture for a QC-LDPC code based on a circulant-1 identity matrix construction. We present a novel representation of the parity-check matrix (PCM) providing a multi-fold throughput gain. Splitting of the node processing algorithm enables us to achieve pipelining of blocks and hence layers. By partitioning the PCM into not only layers but superlayers we derive an upper bound on the pipelining depth for the compact representation. To validate the architecture, a decoder for the IEEE 802.11n (2012) QC-LDPC is implemented on the Xilinx Kintex-7 FPGA with the help of the FPGA IP compiler [2] available in the NI LabVIEWTM Communication System Design Suite (CSDSTM) which offers an automated and systematic compilation flow where an optimized hardware implementation from the LDPC algorithm was generated in approximately 3 minutes, achieving an overall throughput of 608 Mb/s (at 260 MHz). As per our knowledge this is the fastest implementation of the IEEE 802.11n QC-LDPC decoder using an algorithmic compiler.

Index Terms—5G, mm-wave, QC-LDPC, Belief Propagation (BP) decoding, MSA, layered decoding, high-level synthesis (HLS), FPGA, IEEE 802.11n.

I. INTRODUCTION

For the next generation of wireless technology collectively termed as Beyond-4G and 5G (hereafter referred to as 5G), peak data rates of upto ten Gb/s with overall latency less than 1 ms [3] are envisioned. However, due to the proposed operation in the 30-300GHz range with challenges such as short range of communication, increasing shadowing and rapid fading in time, the processing complexity of the system is expected to be high. In an effort to design and develop a channel coding solution suitable to such systems, in this paper, we present a high-throughput, scalable and reconfigurable FPGA decoder architecture.

It is well known that the structure offered by QC-LDPC codes [4] makes them amenable to time and space efficient decoder implementations relative to random LDPC codes. We believe that, given the primary requirements of high decoding throughput, QC-LDPC codes or their variants (such as accumulator-based codes [5]) that can be decoded using belief propagation (BP) methods are highly likely candidates for 5G systems. Thus, for the sole purpose of validating the proposed architecture, we chose a standard compliant code, with a throughput performance that well surpasses the requirement of the chosen standard.

Insightful work on high-throughput (order of Gb/s) BP-based QC-LDPC decoders is available, however, most of such works focus on an ASIC design [6, 7] which usually requires intricate customizations at the RTL level and expert knowledge of VLSI design. A sizeable subset of which caters to fully-parallel [8] or code-specific [9] architectures. From the point of view of an evolving research solution this is not an attractive option for rapid-prototyping. In the relatively less explored area of FPGA-based implementation, impressive results have recently been presented in works such as [10], [11] and [12]. However, these are based on fully-parallel architectures which lack flexibility (code specific) and are limited to small block sizes (primarily due to the inhibiting routing congestion) as discussed in the informative overview in [13]. Since our case study is based on fully-automated generation of the HDL, a fair comparison is done with another state-of-the-art implementation [14] in Section IV. Moreover, in this paper, we provide without loss of generality, strategies to achieve a high-throughput FPGA-based architecture for a QC-LDPC code based on a circulant-1 identity matrix construction.

The main contribution of this brief is a compact representation (matrix form) of the PCM of the QC-LDPC code which provides a multi-fold increase in throughput. In spite of the resulting reduction in the degrees of freedom for pipelined processing, we achieve efficient pipelining of two-layers and also provide without loss of generality an upper bound on the pipelining depth that can be achieved in this manner. The splitting of the node processing allows us to achieve the said degree of pipelining without utilizing additional hardware resources. The algorithmic strategies were realized in hardware for our case study by the FPGA IP [2] compiler in LabVIEWTM CSDSTM which translated the entire software-pipelined high-level language description into VHDL in approximately 3 minutes enabling state-of-the-art rapid-prototyping. We have also demonstrated the scalability of the proposed architecture in an application that achieves over 2 Gb/s of throughput [15].

The remainder of this paper is organized as follows. Section II describes the QC-LDPC codes and the decoding algorithm chosen for this implementation. The strategies for achieving high throughput are explained in Section III. The case study is discussed in Section IV and we conclude with Section V.
II. QUASI-CYCLIC LDPC CODES AND DECODING

LDPC codes (due to R. Gallager [16]) are a class of linear block codes that have been shown to achieve near-capacity performance on a broad range of channels and are characterized by a low-density (sparse) PCM representation.

Mathematically, an LDPC code is a null-space of its $m \times n$ PCM $H$, where $m$ denotes the number of parity-check equations or parity-bits and $n$ denotes the number of variable nodes or code bits [4]. In other words, for a rank $m$ PCM $H$, $m$ is the number of redundant bits added to the $k$ information bits, which together form the codeword of length $n = k + m$. In the Tanner graph representation (due to Tanner [17]), $H$ is the incidence matrix of a bipartite graph comprising of two sets: the check node (CN) set of $m$ parity-check equations and the variable node (VN) set of $n$ variable or bit nodes; the $i^{th}$ CN is connected to the $j^{th}$ VN if $H(i, j) = 1$, $1 \leq i \leq m$ and $1 \leq j \leq n$. A toy example of a Tanner graph is shown in Fig. 1. The degree $d_c (d_v)$ of a CN ($V$) node is the number of $1$'s along the $i^{th}$ row ($j^{th}$ column) of $H$.

For constants $c_c, c_v \in \mathbb{Z}_{>0}$ and $c_c < < m, c_v < < n$, if $\forall i,j$, $d_{ci} = c_c$ and $d_{vj} = c_v$, then the LDPC code is called as a regular code and is called an irregular code otherwise.

A. Quasi-Cyclic LDPC Codes

The first LDPC codes by Gallager are random, which complicate the decoder implementation, mainly because a random interconnect pattern between the VNs and CNs directly translates to a complex wire routing circuit on hardware. QC-LDPC codes belong to the class of structured codes that are relatively easier to implement without significantly compromising performance.

The construction of identity matrix based QC-LDPC codes relies on an $m_b \times n_b$ matrix $H_b$ sometimes called as the base matrix which comprises of cyclically right-shifted identity and zero submatrices both of size $z \times z$ where, $z \in \mathbb{Z}^{+}, 1 \leq i_b \leq (m_b)$ and $1 \leq j_b \leq (n_b)$, the shift value,

\[
s = H_b(i_b, j_b) \in \mathcal{S} = \{-1\} \cup \{0, \ldots, z - 1\}
\]

The PCM matrix $H$ is obtained by expanding $H_b$ using the mapping,

\[
s \rightarrow \begin{cases} 
I_c, & s \in \mathcal{S}\setminus\{-1\} \\
0, & s \in \{-1\}
\end{cases}
\]

where, $I_c$ is an identity matrix of size $z$ which is cyclically right-shifted by $s = H_b(i_b, j_b)$ and $0$ is the all-zero matrix of size $z \times z$. As $H$ is composed of the submatrices $I_c$ and $0$, it has $m = m_b \cdot z$ rows and $n = n_b \cdot z$ columns. $H$ for the IEEE 802.11n (2012) standard [1] (used for our case study) with $z = 81$ is shown in Table 1.

B. Scaled Min-Sum Algorithm for Decoding QC-LDPC Codes

LDPC codes can be decoded using message passing (MP) or belief propagation (BP) [16, 18] on the bipartite Tanner graph where, the CNs and VNs communicate with each other, successively passing revised estimates of the log-likelihood ratio (LLR) associated, in every decoding iteration. In this work we have employed the efficient decoding algorithm presented in [19], with pipelined processing of layers based on the row-layered decoding technique [20], detailed in Section III-C.

**Definition 1.** For $1 \leq i \leq m$ and $1 \leq j \leq n$, let $v_j$ denote the $j^{th}$ bit in the length $n$ codeword and $y_j = v_j + n_j$ denote the corresponding received value from the channel corrupted by the noise sample $n_j$. Let the variable-to-check (VTC) message from VN $i$ to CN $j$ be $q_{ij}$ and, let the check-to-variable (CTV) message from CN $i$ to VN $j$ be $r_{ij}$. Let the a posteriori probability (APP) ratio for VN $j$ be denoted as $p_j$.

The steps of the scaled-MSA [4, 21] are given below.

1) Initialize the APP ratio and the CTV messages as,

\[
p_j^{(0)} = \ln \left( \frac{P(v_j = y_j)}{P(v_j = 1 - y_j)} \right), \quad 1 \leq j \leq n \tag{1}
\]

\[
r_{ij}^{(0)} = 0, \quad 1 \leq i \leq m, 1 \leq j \leq n
\]

2) Iteratively compute at the $t^{th}$ decoding iteration,

\[
q_{ij}^{(t)} = p_j^{(t-1)} - r_{ij}^{(t-1)} \tag{2}
\]

\[
r_{ij}^{(t)} = a \cdot \prod_{k \in \mathcal{N}(i) \setminus \{j\}} \text{sign} (q_{ik}^{(t)}) \cdot \min_{k \in \mathcal{N}(i) \setminus \{j\}} \left\{ |q_{ik}^{(t)}| \right\} \tag{3}
\]

\[
p_j^{(t)} = q_{ij}^{(t)} + r_{ij}^{(t)} \tag{4}
\]

where, $1 \leq i \leq m$, and $k \in \mathcal{N}(i) \setminus \{j\}$ represents the set of the VN neighbors of CN $i$ excluding VN $j$. Let $t_{\text{max}}$ be the maximum number of decoding iterations.

3) Decision on the code bit $v_j$, $1 \leq j \leq n$ as,

\[
\hat{v}_j = \begin{cases} 0, & p_j < 0 \\
1, & \text{otherwise}
\end{cases} \tag{5}
\]

4) If $\hat{v} H^T = 0$, where $\hat{v} = (\hat{v}_1, \hat{v}_2, \ldots, \hat{v}_n)$, or $t = t_{\text{max}}$, declare $\hat{v}$ as the decoded codeword.
length, $N$ decoding, let us first define the decoding throughput

**Definition 2.** Let $F_c$ be the clock frequency, $n$ be the code length, $N_i$ be the number of decoding iterations and $N_c$ be the number of clock cycles per decoding iteration, then the throughput of the decoder is given by, $T = \frac{F_c \cdot n}{N_c \cdot N_i}$ b/s

Even though, $n$ and $N_i$ are functions of the code and the decoding algorithm used, $F_c$ and $N_c$ are determined by the hardware architecture. Architectural optimization such as the ability to operate the decoder at higher clock rates with minimal latency between decoding iterations can help achieve higher throughput. We have employed the following techniques to increase the throughput given by Definition 2.

### A. Linear Complexity Node Processing

As noted in Section II-B, separate processing units for CNs and VNs are not required unlike that for the flooding schedule. The hardware elements that process equations (2)-(4) are collectively referred to as the Node Processing Unit (NPU).

Careful observation reveals that, among equations (2)-(4), processing the CTV messages $r_{ij}$, $1 \leq i \leq m$ and $1 \leq j \leq n$ is the most computationally intensive due to the calculation of the sign, and the minimum value operations. The complexity of processing the minimum value is $O(d_{ci}^2)$. In software, this translates to two nested for-loops, an outer loop that executes $d_{ci}$ times and an inner loop that executes $(d_{ci} - 1)$ times.

To achieve linear complexity $O(d_{ci})$ for the minimum value computation, we split the process into two phases or passes: the *global* pass where the first and the second minimum (the smallest value in the set excluding the minimum value of the set) for all the neighboring VNs of a CN are computed and the *local* pass where the first and second minimum from the set excluding the minimum value operations. The complexity of processing the minimum value is $O(d_{ci})$.

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In software, this translates to two consecutive for-loops, each complexity from illustrating the opportunity to parallelize Local NPU (LNPU). The algorithm is given below.

1) Global Pass:
   i. Initialization: Let $\ell$ denote the discrete time-steps such that, $\ell \in \{0 \cup \{1, 2, \ldots, |\mathcal{N}(i)|\}\}$ and let $f(\ell)$ and $s(\ell)$ denote the value of the first and the second minimum at time $\ell$ respectively. The initial value at time $\ell = 0$ is,
   
   \[
   f^{(0)} = s^{(0)} = \infty. \tag{6}
   \]

   ii. Comparison: Let $k_i(\ell) \in \mathcal{N}(i), \ell = \{1, 2, \ldots, |\mathcal{N}(i)|\}$, denote the index of the $\ell$th neighboring VN of CN $i$. Note that, $k_i(\ell)$ depends on $i$ and $\ell$, specifically, for a given CN $i$ it is a bijective function of $\ell$. An increment from $(\ell-1)$ to $\ell$ corresponds to moving from the edge CN $i \leftrightarrow$ VN $k_i(\ell-1)$ to the edge CN $i \leftrightarrow$ VN $k_i(\ell)$.
   
   \[
   f^{(\ell)} = \begin{cases}  
   \{|q_k i(\ell)|, f^{(\ell-1)}), |q_k i(\ell)| \leq f^{(\ell-1)} \text{ otherwise.} 
   \end{cases} \tag{7}
   \]

   \[
   s^{(\ell)} = \begin{cases}  
   \{|q_k i(\ell)|, f^{(\ell-1)} < |q_k i(\ell)| < s^{(\ell-1)} \text{ otherwise.} \end{cases} \tag{8}
   \]

   Thus, $f^{(\ell_{max})}$ and $s^{(\ell_{max})}$ are the first and second minimum values for the set of VN neighbors of CN $i$, where, $\ell_{max} = |\mathcal{N}(i)|$.

2) Local Pass: Let the minimum value as per equation (3) for VN $k_i(\ell)$ be denoted as $q_{\text{min}}^{(\ell)}$, $\ell \in \{1, 2, \ldots, |\mathcal{N}(i)|\}$ then,

   \[
   q_{\text{min}}^{(\ell)} = \begin{cases}  
   \{f^{(\ell_{max})}, s^{(\ell_{max})}, |q_k i(\ell)| \neq f^{(\ell_{max})}, s^{(\ell_{max})} \text{ otherwise.} \end{cases} \tag{9}
   \]

   In software, this translates to two consecutive for-loops, each executing $(d_{ci}-1)$ times. Consequently, this reduces the complexity from $O(d_{ci}^2)$ to $O(d_{ci})$. A similar approach is also found in [22], [9]. The sign computation is processed in a similar manner.

   \[
   \begin{array}{c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c} 
   \text{VN}_{2} & \ldots & \text{VN}_{3} & \ldots & \text{VN}_{s_{(J+1)-1}} \\
   \hline
   \text{NPU}_{0} & 0 & \ldots & 0 & 1 & 0 & \ldots & 0 \\
   \hline
   \text{NPU}_{1} & 0 & \ldots & 0 & 1 & 0 & \ldots & 0 \\
   \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\
   \text{NPU}_{s-2} & 0 & \ldots & 0 & 0 & 0 & \ldots & 0 \\
   \text{NPU}_{s-1} & 0 & \ldots & 1 & 0 & 0 & \ldots & 0 \\
   \end{array}
   \]

   Table II: Arbitrary submatrix $I_s$ in $H$, $0 \leq J \leq n_b-1$, illustrating the opportunity to parallelize $z$ NPUs.

B. z-fold Parallelization of NPUs

The CN message computation given by equation (3) is repeated $m$ times in a decoding iteration i.e. once for each CN. A straightforward serial implementation of this kind is slow and undesirable. Instead, we apply a strategy based on the following understanding.

**Fact 1.** An arbitrary submatrix $I_s$ in the PCM $H$ corresponds to $z$ CNs connected to $z$ VNs on the bipartite graph, with strictly 1 edge between each CN and VN.

This implies that no CN in this set of $z$ CNs given by $I_s$ shares a VN with another CN in the same set. Table II illustrates such an arbitrary submatrix in $H$. This presents us with an opportunity to operate $z$ NPUs in parallel (hereafter referred to as an NPU array), resulting in a $z$-fold increase in throughput.

C. Layered Decoding

From Remark 1, it is clear that, in the flooding schedule all nodes on one side of the bipartite graph can be processed in parallel. Although, such a fully parallel implementation may seem as an attractive option for achieving high-throughput performance, it has its own drawbacks. Firstly, it becomes quickly intractable in hardware due to the complex interconnect pattern. Secondly, such an implementation usually restricts itself to a specific code structure. In spite of the serial nature of the algorithm in II-B, one can process multiple nodes at the same time if the following condition is satisfied.

**Fact 2.** From the perspective of CN processing, two or more CNs can be processed at the same time (i.e. they are independent of each other) if they do not have one or more VNs (code bits) in common.

The row-layering technique used in this work essentially relies on the above condition being satisfied. In terms of $H$, an arbitrary subset of rows can be processed at the same time provided that, no two or more rows have a 1 in the same column of $H$. This subset of rows is termed as a row-layer (hereafter referred to as a layer). In other words, given a set $L = \{L_1, L_2, \ldots, L_s\}$ of $I$ layers in $H$, $\forall u \in \{1, 2, \ldots, I\}$ and $\forall i, i' \in L_u$, then, $\mathcal{N}(i) \cap \mathcal{N}(i') = \emptyset$. Observing that, $\sum_{u=1}^{I} |L_u| = m$, in general, $L_u$ can be any subset of rows as long as the rows within each subset satisfy the condition in Fact 2 implying that, $|L_u| \neq |L_{u'}|, \forall u, u' \in \{1, 2, \ldots, I\}$ is possible. Owing to the structure of QC-LDPC codes, the choice of $|L_u|$ (and hence $I$) becomes much obvious. Submatrices $I_s$ in $H_b$ (with row and column weight of 1) guarantee that, for the $z$ CNs corresponding to the rows of $I_s$, always satisfy the condition in Fact 2. Hence, $|L_u| = |L_{u'}| = z$ is chosen.

From the VN or column perspective, $|L_u| = z, \forall u = \{1, 2, \ldots, I\}$ implies that, the columns of $H$ are also divided into subsets of size $z$ (hereafter referred to as block columns) given by the set $B = \{B_1, B_2, \ldots, B_J\}, J = \frac{n}{z} = n_b$. Observing that VNs belonging to a block column may participate in CN equations across several layers, we further divide the
block columns into blocks, where a block is the intersection of a layer and a block column. Two or more layers $L_u, L_w$ are said to be dependent with respect to the block column $B_w$ if $H_b(u, w) \neq \pm 1$ and $H_b(u', w) \neq \pm 1$ and are said to be independent otherwise.

### Table III: Illustration of Message Passing in row-layered decoding in a Section of the PCM $H_b$

| Layers | Blocks |
|--------|--------|
|        | $B_2$  | $B_3$  | $B_4$  |
| $L_1$  | $\downarrow$ | $\downarrow$ | $\downarrow$ |
| $L_2$  | $\downarrow$ | 28 | $\downarrow$ |
| $L_3$  | $\downarrow$ | $\downarrow$ | $\downarrow$ |
| $L_4$  | $\downarrow$ | 53 | $\downarrow$ |
| $L_5$  | $\downarrow$ | $\downarrow$ | $\downarrow$ |
| $L_6$  | $\downarrow$ | 79 | 79 | $\downarrow$ |
| $L_7$  | $\downarrow$ | $\downarrow$ | $\downarrow$ |
| $L_8$  | $\downarrow$ | $\downarrow$ | $\downarrow$ |
| $L_9$  | $\downarrow$ | $\downarrow$ | $\downarrow$ |
| $L_{10}$ | $\downarrow$ | 45 | 70 |
| $L_{11}$ | $\downarrow$ | 56 | 57 |
| $L_{12}$ | $\downarrow$ | $\downarrow$ | 61 |

to $L_4$ to $L_2$ to $L_5$

For example, in Table III we can see that layers $L_4, L_7, L_{10}$ and $L_{11}$ are dependent with respect to block column $B_2$. Assuming that the message update begins with layer $L_1$ and proceeds downward, the arrows represent the directional flow of message updates from one layer to another. Thus, layer $L_7$ cannot begin updating the VNs associated with block column $B_2$ before layer $L_4$ has finished updating messages for the same set of VNs and so on. The idea of parallelizing $z$ NPU arrays can process message updates for multiple independent layers. It is clear that, dependent layers limit the degree of parallelization available to achieve high-throughput. In Section III-B we discuss pipelining methods that allow us to overcome layer-to-layer dependency and improve throughput.

### D. Compact Representation of $H_b$

Before we discuss the pipelined processing of layers, we present a novel compact (thus efficient) matrix representation leading to a significant improvement in throughput. To understand this, let us call 0 submatrices in $H$ as invalid blocks, where there are no edges between the corresponding CNs and VNs, and the submatrices 1 as valid blocks. In a conventional approach to scheduling (for example in [7]), message computation is done for all the valid and invalid blocks. To avoid processing invalid blocks, we propose an alternate representation of $H_b$ in the form of two matrices: $\beta_1$ (Table IV), the block index matrix and $\beta_S$ (Table V), the block shift matrix. $\beta_1$ and $\beta_S$ hold the index locations and the shift values (and hence the connections between the CNs and VNs) corresponding to only the valid blocks in $H_b$, respectively. Construction of $\beta_1$ is based on the following definition.

**Definition 3.** Construction of $\beta_1$ is as follows.

For $u = \{1, 2, \ldots, I\}$

- set $w = 0$, $j_b = 0$
- for $j_b = \{1, 2, \ldots, n_b\}$
  - $j_u = j_b + 1$
  - if $H_b(u, j_u) \neq \pm 1$
    - $w = w + 1; \beta_1(u, w) = j_b; \beta_S(u, w) = H_b(u, j_b)$

To observe the benefit of this alternate representation, let us define the following ratio.

**Definition 4.** Let $\lambda$ denote the compaction ratio, which is the ratio of the number of columns of $\beta_1$ (which is the same for $\beta_S$) to the number of columns of $H_b$. Hence, $\lambda = \frac{J}{n_b}$.

The compaction ratio $\lambda$ is a measure of the compaction achieved by the alternate representation of $H_b$. Compared to the conventional approach, scheduling as per the $\beta_1$ and $\beta_S$ matrices improves throughput by $\frac{1}{\lambda}$ times. In our case study, $\lambda = \frac{8}{24} = \frac{1}{3}$, thus providing a throughput gain of $\frac{1}{\lambda} = 3$.

**Remark 2.** In the irregular QC-LDPC code in our case study, all layers comprise of 7 blocks each, except layer $L_7$ and $L_{12}$ which have 8. With the aim of minimizing hardware
### Table V: Block shift matrix $\beta_8$ showing the right-shift values for the valid blocks to be processed.

| Layers ↓ | Blocks → |
|----------|----------|
|          | $b_1$ $b_2$ $b_3$ $b_4$ $b_5$ $b_6$ $b_7$ $b_8$ |
| $L_1$    | 57 50 11 50 79 1 0 -1 |
| $L_2$    | 3 28 0 55 7 0 0 -1 |
| $L_3$    | 30 24 37 56 14 0 0 -1 |
| $L_4$    | 62 53 53 3 35 0 0 -1 |
| $L_5$    | 40 20 66 22 28 0 0 -1 |
| $L_6$    | 0 8 42 50 8 0 0 -1 |
| $L_7$    | 69 79 79 56 52 0 0 0 |
| $L_8$    | 65 38 57 72 27 0 0 -1 |
| $L_9$    | 64 14 52 30 32 0 0 -1 |
| $L_{10}$ | 45 70 0 77 9 0 0 -1 |
| $L_{11}$ | 2 56 57 35 12 0 0 -1 |
| $L_{12}$ | 24 61 60 27 51 16 1 0 |

### Table VI: Rearranged Block Index Matrix $\beta'_I$ used for our work, showing the valid blocks (highlighted) to be processed.

| Layers ↓ | Blocks → |
|----------|----------|
|          | $b_1$ $b_2$ $b_3$ $b_4$ $b_5$ $b_6$ $b_7$ $b_8$ |
| $L_1$    | 0 4 8 13 6 10 12 -1 |
| $L_2$    | 9 0 4 8 13 14 2 -1 |
| $L_3$    | 15 9 0 4 8 5 14 -1 |
| $L_4$    | 7 15 16 0 4 8 1 -1 |
| $L_5$    | 17 7 3 16 0 4 8 -1 |
| $L_6$    | 6 17 18 11 -1 0 4 8 |
| $L_7$    | 19 6 0 8 1 2 18 12 |
| $L_8$    | 4 19 5 0 8 20 10 -1 |
| $L_9$    | 21 4 11 5 0 8 20 -1 |
| $L_{10}$ | 1 21 4 3 22 9 8 -1 |
| $L_{11}$ | 0 1 23 4 3 22 10 -1 |
| $L_{12}$ | 8 0 2 23 4 12 7 11 |

complexity by maintaining a static memory-address generation pattern (does not change from layer-to-layer), our implementation assumes regularity in the code. The decoder processes 8 blocks for each layer of the $\beta_I$ matrix resulting in some throughput penalty. The results from processing the invalid blocks in $L_7$ and $L_{12}$ are not stored in the memory.

### E. Layer-Pipelined Decoder Architecture

In Section [III-C](#) we saw how dependent layers for a block column cannot be processed in parallel. For instance, in $H_b$ in Table II VNs associated with the block column $B_1$ participate in CN equations associated with all the layers except layer $L_{10}$, suggesting that there is no scope of parallelization of layer processing at all. This situation is better observed in $\beta_I$ shown in Table IV.

**Fact 3.** If a block column of $\beta_I$ has a particular index value appearing in more than one layer, then the layers corresponding to that value are dependent with respect to that block column.

**Proof:** Follows directly by applying Fact 2 to Definition 2.

In other words, $\forall u, u' \in \{1, 2, \ldots, I\}$, $\forall w \in \{1, 2, \ldots, J\}$, if $\beta_I(u, w) = \beta_I(u', w)$ then, the layers $L_u$ and $L_{u'}$ are dependent. It is obvious that, to process all layers in parallel ($L_1$ to $L_{12}$ in II), the condition,

$$\beta_I(u, w) \neq \beta_I(u', w)$$

must hold for $\forall u, u' \in \{1, 2, \ldots, I\}$. We call the set of layers $\mathcal{L}$ satisfying Fact 3 as a superlayer. As will be seen later, the formation of superlayers of suitable size is crucial to achieve parallelism in the architecture.

The idea is to rearrange the $\beta_I$ matrix elements from their original order. If $\beta_I(u, w) = \beta_I(u', w)$, $u < u'$ then stagger the execution of $\beta_I(u', w)$ with respect to $\beta_I(u, w)$ by placing $\beta_I(u', w)$ in $\beta'_I(u', w')$ such that $w < w'$. To understand how layers are pipelined, let us first look at the non-pipelined case.

Without loss of generality, Fig. 2(a) shows the block-level view of the NPU timing diagram without the pipelining of layers. As seen in Section III-A, the GNPU and LNPU operate in tandem and in that order, implying that the LNPU has to wait for the GNPU updates to finish. The layer-level picture is depicted in Fig. 3(a). We call this version as the $1x$ version. This idling of the GNPU and LNPU can be avoided by introducing pipelined processing of blocks given by the following Lemma.

**Lemma 1.** Within a superlayer, while the LNPU processes messages for the blocks $\beta_I(u, w)$, the GNPU can process messages for the blocks $\beta'_I(u + 1, w)$, $u = \{1, 2, \ldots, |\mathcal{L}| - 1\}$ and $w = \{1, 2, \ldots, J\}$.

**Proof:** Follows directly from the layer independence condition in Fact 2.

**Fig. 2(c)** illustrates the block-level view of this 2-layer pipelining scheme. It is important to note that, the splitting of the NPU process into two parts, namely, the GNPU and the LNPU (that work in tandem) is a necessary condition for Fact 3 and hence Lemma 1 to hold. However, at the boundary of the superlayer the Lemma 1 does not hold and pipelining has to be restarted for the next layer as seen in the layer-level view.
shown in Fig. 3(c). We call this version as the $2x$ version. This is the classical pipelining overhead. In the following, we impose certain constraints on the size of the superlayers in $\mathbf{H}$.

**Definition 5.** Without loss of generality, the pipelining efficiency $\eta_p$ is the number of layers processed per unit time per NPU array.

For the case of pipelining two layers shown in Fig. 3(c),

$$\eta_p^{(2)} = \frac{|\mathcal{L}|}{|\mathcal{L}| + 1}$$

(11)

Thus, we impose the following conditions on $|\mathcal{L}|$:

1) Since, two layers are processed in the pipeline at any given time, provided that $I$ is even,

$$|\mathcal{L}| \in \mathcal{F} = \{x : x \text{ is an even factor of } I\}$

It is important to note that, for any value of $|\mathcal{L}| \in \mathcal{F}$, $\mathcal{L}$ must be a superlayer.

2) Given a QC-LDPC code, $|\mathcal{L}|$ is a constant. This is to facilitate a symmetric pipelining architecture which is a scalable solution.

3) Choice of $|\mathcal{L}|$ should maximize pipelining efficiency $\eta_p$,

$$l^* = \arg \max_{|\mathcal{L}| \in \mathcal{F}} \eta_p$$

**Case Study:** Table VI shows one such rearrangement of $\beta_{I}$ for the QC-LDPC code for our case study in Table IV. Unresolved dependencies are shown in blue in Table VI. $I = m_b = 12$, $\mathcal{F} = \{2, 4, 6\}$ and, $l^* = \arg \max_{|\mathcal{L}| \in \mathcal{F}} \eta_p = 6$. The rearranged block index matrix $\beta_{I}'$ is shown in Table VI and the layer-level view of the pipeline timing diagram for the same is shown in Fig. 3(d).

**High-level FPGA-based Decoder Architecture:** The high-level decoder architecture is shown in Fig. 4. The ROM holds the LDPC code parameters specified by the $\beta_{I}'$ and the $\beta_{I}^*$ along with other code parameters such as the block length and the maximum number of decoding iterations. The APP memory is initialized with the channel LLR values corresponding to all the VNs as per equation (1). The barrel shifter operates on blocks of VNs (APP values in equation (3)) of size $z \times f$, where $f$ is the fixed-point word length used in the implementation for APP values. It circularly rotates the values to the right by using the shift values from the $\beta_{I}'$ matrix in the ROM, effectively implementing the connections between the CNs and VNs. The cyclically shifted APP memory values and the corresponding CN message values for the block in question are fed to the NPU arrays. Here, the GNPUs compute VN messages as per equation (2) and the LNPUs compute CN messages as per equation (3). These messages are then stored back at their respective locations in the RAMs for processing the next block.

**IV. CASE STUDY**

To evaluate the proposed strategies for achieving high-throughput, we have implemented the scaled-MSA based decoder for the QC-LDPC code in the IEEE 802.11n (2012). For this code, $m_b \times n_b = 12 \times 24$, $z = 27$, 54 and 81 resulting in code lengths of $n = 24 \times z = 648$, 1296 and 1944 bits respectively. Our implementation supports the submatrix size of $z = 81$ and hence is capable of supporting all the block lengths for the rate $R = \frac{1}{2}$ code. At the time of writing this paper, we have successfully implemented the two aforementioned versions.

1) $Ix$: The block-level and the layer-level view of the pipelining is illustrated in Fig. 2(b) and 3(b) respectively.

2) $2x$: Pipelining is done in software at the algorithmic description level. The block and layer level views of the pipelined processing are shown in Fig. 2(d) and 3(d) respectively. With an efficiency $\eta_p^{(2)} = 0.86$, the $2x$ version is 1.7 times faster than the $Ix$ version.

We represent the input LLRs from the channel and the CTV messages with 6 signed bits and 4 fractional bits. Fig. 5 shows the bit-error rate (BER) performance for the floating-point and the fixed-point data representation with 8 decoding iterations. As expected, the fixed-point implementation suffers by about 0.5dB compared to the floating point version. The decoder algorithm was described using the LabVIEW CSDS software. The FPGA IP compiler was then used to generate the VHDL code from the graphical dataflow description. The VHDL code was synthesized, placed and routed using the Xilinx Vivado compiler on the Xilinx Kintex-7 FPGA available on the NI PXIe-7975R FPGA board. The decoder core achieves an overall throughput of 608Mb/s at an operating frequency of 200MHz and a latency of 5.7µs. Table VII shows that the resource usage for the $2x$ version (almost twice as fast due to pipelining) is close to that of the $Ix$ version. The FPGA IP compiler chooses to use more FF for data storage in the $Ix$ version, while it uses more BRAM in $2x$ version. Compared to a contemporary FPGA-based implementation in [14] using high-level algorithmic description compiled to an HDL, our implementation achieves a higher throughput with relatively lesser resource utilization. Authors of [14] have implemented a decoder for a $R = \frac{1}{2}$, $n = 648$, IEEE 802.11n (2012) code that achieves a throughput of 13.4Mb/s at 122MHz, utilizes 2% of slice registers, 3% of slice LUTs and 20.9% of Block RAMs on the Spartan-6 LX150T FPGA with a comparable BER performance.

**2.06 Gbs/s LDPC Decoder** [23]: An application of this work has been demonstrated in IEEE GLOBECOM’14 where the QC-LDPC code for our case study was decoded with a throughput of 2.06 Gbs/s. This throughput was achieved by using five decoder cores in parallel on the Xilinx K7 (410t) FPGA in the NI USRP-2953R.

**V. CONCLUSION**

In this brief we have proposed techniques to achieve high-throughput performance for a MSA based decoder for QC-LDPC codes. The proposed compact representation of the PCM provides significant improvement in throughput. An IEEE 802.11n (2012) decoder is implemented which attains a throughput of 608Mb/s (at 260MHz) and a latency of 5.7µs
Figure 2: Block-level view of the pipeline timing diagram. (a) General case for a circulant-1 identity submatrix construction based QC-LDPC code (see Section II) without pipelining. (b) Special case of the IEEE 802.11n QC-LDPC code used in this work without pipelining (c) Pipelined processing of two layers for the general QC-LDPC code case in (a). (d) Pipelined processing of two layers for the IEEE802.11n QC-LDPC code case in (b).

Figure 3: Layer-level view of the pipeline timing diagram. (a) General case for a circulant-1 identity submatrix construction based QC-LDPC code (see Section II) without pipelining. (b) Special case of the IEEE 802.11n QC-LDPC code used in this work without pipelining (c) Pipelined processing of two layers for the general QC-LDPC code case in (a). (d) Pipelined processing of two layers for the IEEE802.11n QC-LDPC code case in (b).
z: submatrix size
n: codeword length
N: number of columns in Hₜ
dₜ: check node (CN) degree
f: implementation word length

Figure 4: High-level decoder architecture, showing the z-fold parallelization of the NPUs with an emphasis on the splitting of the sign and the minimum computation given in equation (3). Note that, other computations in equations (1)-(4) are not shown for simplicity here. For both the pipelined and the non-pipelined versions, processing schedule for the inner Block Processing loop is as per Fig. 2 and that for the outer Layer Processing loop is as per Fig. 3.

Figure 5: Bit Error Rate (BER) performance comparison between uncoded BPSK (rightmost), rate=1/2 LDPC with 4 iterations using fixed-point data representation (second from right), rate=1/2 LDPC with 8 iterations using fixed-point data representation (third from right), rate=1/2 LDPC with 8 iterations using floating-point data representation (leftmost).

| Device | Throughput(Mb/s) | FF(%) | BRAM(%) | DSP48(%) | LUT(%) |
|--------|-----------------|-------|---------|----------|--------|
| 1x     | 337             | 9.1   | 4.7     | 5.2      | 8.7    |
| 2x     | 608             | 5.3   | 6.4     | 5.2      | 8.2    |

Table VII: LDPC Decoder IP FPGA Resource Utilization & Throughput on the Xilinx Kintex-7 FPGA.

on the Xilinx Kintex-7 FPGA. The FPGA IP compiler greatly reduces prototyping time and is capable of implementing complex signal processing algorithms. There is undoubtedly more scope for improvement, nevertheless, our current results are promising.
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