We present a physics-based circuit-compatible model for double-gated two-dimensional semiconductor-based field-effect transistors, which provides explicit expressions for the drain current, terminal charges, and intrinsic capacitances. The drain current model is based on the drift-diffusion mechanism for the carrier transport and considers Fermi–Dirac statistics coupled with an appropriate field-effect approach. The terminal charge and intrinsic capacitance models are calculated adopting a Ward–Dutton linear charge partition scheme that guarantees charge conservation. It has been implemented in Verilog-A to make it compatible with standard circuit simulators. In order to benchmark the proposed modeling framework we also present experimental DC and high-frequency measurements of a purposely fabricated monolayer MoS$_2$-FET showing excellent agreement between the model and the experiment and thus demonstrating the capabilities of the combined approach to predict the performance of 2DFETs.

We introduce a physics-based circuit-compatible model for 2D semiconductor-based FETs (2DFETs) combining intrinsic capacitances, the drain current and terminal charges for the static regime. The drain current model is based on the drift-diffusion mechanism for the carrier transport and considers Fermi–Dirac statistics coupled with an appropriate field-effect approach. The terminal charge and intrinsic capacitance models are calculated adopting a Ward–Dutton linear charge partition scheme that guarantees charge conservation. It has been implemented in Verilog-A to make it compatible with standard circuit simulators. In order to benchmark the proposed modeling framework we also present experimental DC and high-frequency measurements of a purposely fabricated monolayer MoS$_2$-FET showing excellent agreement between the model and the experiment and thus demonstrating the capabilities of the combined approach to predict the performance of 2DFETs.

**INTRODUCTION**

Since the emergence of graphene, over a surprisingly short period of time, an entire new family of two-dimensional materials (2DMs) has been discovered. Some of them are already used as channel materials in FETs, being promising candidates to augment silicon and III–V compound semiconductors. In this context, the development of electrical models for 2D semiconductor-based FETs (2DFETs) is essential to: (1) interpret experimental results; (2) evaluate their expected digital/RF performance; (3) benchmark against existing technologies; and (4) eventually provide guidance for circuit design and circuit-level simulations.

Several compact models for three-terminal FETs based on graphene and related 2D materials (GRMs) have been recently published encompassing both static and dynamic regimes. In particular, Suryavanshi et al. proposed a semi-classical transport model for the drain current combining the intrinsic FET behavior with models of the contact resistance, traps and impurities, quantum capacitance, fringing fields, high-field velocity saturation and self-heating. However, the dynamic regime is described using a charge model derived for bulk MOSFETs that fails to capture the specific physics of the 2D channel, since it considers that the channel is always in a weak-inversion regime and therefore the channel charge can be assumed to be linearly distributed along the device. Wang et al. reported on a compact model restricted to the static regime of graphene FETs and based on the virtual-source approach, valid for both the saturation and linear regions of device operation. Also based on the virtual-source approach, Rakheja et al. studied quasi-ballistic graphene FETs. Nevertheless, they also employed the approximation derived for bulk MOSFETs for the dynamic regime description even though the channel material considered is graphene. Jiménez early developed a model describing the drain current for single layer transition metal dichalcogenide (TMD) FETs based on surface potential and drift-diffusion approaches but the dynamic behavior of the TMD-FETs was not treated. Also based on surface potential and drift-diffusion arguments, Parrish et al. presented a compact model for graphene-based FETs for linear and non-linear circuits, but the dynamic regime description was roughly estimated in a way that splitting the total gate capacitance between gate-drain and gate-source capacitances. A charge-based compact model for TMD-based FETs only valid for the static regime but simultaneously including interface traps, ambipolar current behavior, and negative capacitance was proposed by Yadav et al. Taur et al. presented an analytic drain current model for short-channel 2DFETs combining a subthreshold current model based on the solution to 2D Poisson’s equation and a drift-diffusion approach to get an all-region static description. Rahman et al. discussed a physics-based compact drain current model for monolayer TMD-FETs considering drift-diffusion transport description and the gradual channel approximation to analytically solve the Poisson’s equation. Unfortunately, none of them faced the dynamic regime operation. Finally, Golhipour et al. proposed a compact model that combines both the drift-diffusion and the Landauer–Buttiker approaches to properly describe the long- and short-channel FETs in flexible electronics, respectively. As a key feature, the mechanical bending is considered by linearly decreasing the channel material bandgap with respect to the applied strain. However, the capacitance model was roughly approximated by considering that the top (back) gate-drain and top (back) gate-source capacitances are just the geometrical top (back) gate capacitance. In summary, up to date the dynamic description of 2DFETs has been either roughly approximated or not specifically addressed for such devices. Our aim is to develop an accurate and physics-based compact model of the terminal charges and corresponding intrinsic capacitances of four-terminal (4T) 2DFETs valid for all operation regimes. In doing so, we present such a model together with the drain current equation, developed by

**ARTICLE**

**Large-signal model of 2DFETs: compact modeling of terminal charges and intrinsic capacitances**

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We present a physics-based circuit-compatible model for double-gated two-dimensional semiconductor-based field-effect transistors, which provides explicit expressions for the drain current, terminal charges, and intrinsic capacitances. The drain current model is based on the drift-diffusion mechanism for the carrier transport and considers Fermi–Dirac statistics coupled with an appropriate field-effect approach. The terminal charge and intrinsic capacitance models are calculated adopting a Ward–Dutton linear charge partition scheme that guarantees charge conservation. It has been implemented in Verilog-A to make it compatible with standard circuit simulators. In order to benchmark the proposed modeling framework we also present experimental DC and high-frequency measurements of a purposely fabricated monolayer MoS$_2$-FET showing excellent agreement between the model and the experiment and thus demonstrating the capabilities of the combined approach to predict the performance of 2DFETs.

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some of us,\textsuperscript{12} based on drift-diffusion theory where the surface potential is the key magnitude of the model. So that, the combination of both approaches gives rise to a compact large-signal model suitable for commercial TCAD tools employed in the simulation of circuits based on 2DFETs. The model has been shown to reproduce with good agreement DC and high-frequency measurements of a fabricated \textit{n}-type MoS\textsubscript{2}-based FET, and has been used to predict the output transient of a three-stage ring oscillator.

RESULTS

Large-signal model of four-terminal 2DFETs

We first deal with the development of the large-signal model of 4T 2DFETs by the sequential formulation of the electrostatics, the drain current equation, the terminal charge model, and the corresponding intrinsic capacitance description. The cross-section of the considered dual-gated 2DFET is depicted in Fig. 1a. For the sake of brevity, we derive here the expressions for an \textit{n}-type device (the extension to a \textit{p}-type transistor can be obtained straightforwardly). Provided that the semiconductor bandgap is not too small, we can assume that \( p(x) \ll n(x) \) in all regimes of operation, where \( p(x) \) and \( n(x) \) are the hole and electron carrier densities, respectively. Upon application of 1D Gauss’ law to the double-gate stack shown in Fig. 1b, the electrostatics can be described using the equivalent circuit depicted in Fig. 1c:

\[
Q_{\text{net}}(x) + Q_\text{it}(x) = -C_i(V_g - V_g0 - V(x) + V_t(x)) - C_b(V_b - V_b0 - V(x) + V_c(x)),
\]

(1)

where \( Q_{\text{net}}(x) = q[p(x) - n(x)] \) is the overall net mobile sheet charge density and \( q \) is the elementary charge. \( C_i = \epsilon_i t_i / \epsilon_0 \) (\( C_b = \epsilon_b t_b / \epsilon_0 \)) is the top (back) oxide capacitance per unit area where \( \epsilon_i (\epsilon_b) \) and \( t_i \) (\( t_b \)) are the top (back) gate oxide relative permittivity and thickness, respectively; and \( V_g - V_g0 \) (\( V_b - V_b0 \)) is the overdrive top (back) gate voltage. These latter quantities comprise work-function differences between the gates and the 2D channel and any possible additional charges due to impurities or doping. The energy \( qV_c(x) = E_c(x) - E_f(x) \) represents the shift of the quasi-Fermi level with respect to the conduction band edge and \( qV_t(x) = E_t(x) \) is the quasi-Fermi level along the channel. This latter quantity must fulfill the boundary conditions: (1) \( V(x = 0) = V_g \) (source voltage) at the source end; (2) \( V(x = L) = V_d \) (drain voltage) at the drain end.

2D crystals are far from perfect and suffer from diverse nonidealities. In particular, interface traps are unavoidable in FETs, even for those processed by state-of-the-art CMOS technology,\textsuperscript{13} impacting negatively the performance of 2DFETs.\textsuperscript{14} Therefore, it is mandatory to include them in order to achieve an accurate predictive TCAD tool. For \textit{n}-type devices, acceptor-like traps (which are negatively charged when occupied by electrons and are energetically located in the upper half of the bandgap\textsuperscript{15}) contribute the most to the device electrical characteristics.\textsuperscript{16} Assuming the traps are situated at an effective energy \( E_s - qV_f \) below the conduction band, the occupied trap density can be written as \( n_k = N_k(1 + \exp(V_c - V_f/V_n)) \), where \( N_k \) is the effective trap density considered to be a delta function in energy. The trap charge density is then \( Q_{\text{it}} = -qn_k \) and the interface trap capacitance \( C_{\text{it}} \) at the oxide-semiconductor interface (taken as a combination from both interfaces of the ultra-thin 2D channel) can be computed as:

\[
C_{\text{it}} = \frac{dQ_{\text{it}}}{dV_c} = qN_k \frac{1}{2V_{\text{th}}[1 + \cosh(V_c - V_f/V_n)]},
\]

(2)

where \( V_{\text{th}} = k_BT/q \) is the thermal voltage, \( k_B \) is the Boltzmann constant, and \( T \) is the temperature. The term \( C_{\text{it}} \) adds to the quantum capacitance \( C_q \), as shown in Fig. 1c.

We can, thus, find an expression to calculate the overall net mobile sheet density assuming a parabolic dispersion relationship modeled in the effective mass approximation and using Fermi–Dirac statistics\textsuperscript{17}:

\[
Q_{\text{net}}(x) = -q\rho_n(x) = -C_{\text{it}}V_{\text{th}}u(V_c); \quad u(V_c) = \ln \left( 1 + e^{\frac{V_c}{V_{\text{th}}}} \right),
\]

(3)

where \( C_{\text{it}} = q^2D_0 \) is defined as the degenerated-quantum capacitance, which corresponds to the upper-limit achievable when the 2D carrier density becomes heavily degenerated.\textsuperscript{17} \( D_0 = g_x(m^2/2\hbar^2) + g_q(m^2/2\hbar^2)\exp[-\Delta E_2/k_BT] \) is the 2D density of states, with \( \hbar \) being the reduced Planck’s constant, \( g_x (g_q) \) the degeneracy factor and \( m^2 \) the conduction band effective mass at the \( K \) (\( Q \)) band valley. In most TMDs, the second conduction valley, labeled as \( Q \) valley, is non-negligible since the energy separation between the \( K \) and \( Q \) conduction valleys, \( \Delta E_2 \), is only around 2\( k_BT \).\textsuperscript{18,19} Thus, two conduction band valleys may participate in the transport process. The rest of valleys are, on the contrary, far away in energy to contribute to the electrical conduction,\textsuperscript{20} and hence can be neglected for practical purposes.

The quantum capacitance of the 2DM can be computed by evaluating \( C_q = dQ_{\text{net}}/dV_c \) resulting in:

\[
C_q = C_{\text{it}}[1 - e^{1-u}].
\]

(4)

Due to the complexity of Eq. (1) and considering the relation between \( Q_{\text{net}} \) and \( V_c \) given by Eq. (3), it is not possible to get an explicit expression for \( V_c \) as a function of the applied bias. However, an iterative Verilog-A algorithm can be implemented to evaluate the chemical potential at the source and drain edges,

\[\text{Fig. 1} \quad \text{a} \text{ Cross-section of the 2DFET considered in the modeling framework. A 2DM plays the role of the active channel. b} \text{ Scheme of the 2DM-based capacitor showing the relevant physical and electrical parameters. c} \text{ Equivalent capacitive circuit of the 2DFET.}\]
which are the relevant quantities determining the drain current. In doing so, \( V_{G} = V_{Gd}-V_s \) and \( V_{Gd} = V_{Gd}-V_{bs} \) are obtained, respectively, from Eqs. (1) and (3) by a construct\textsuperscript{21,22} which lets the circuit simulator to iteratively solve both equations during run-time.

In the diffusive regime, the drain current of a 2DFET can be accurately computed by the following compact expression\textsuperscript{12}:

\[
i_{ds} = \frac{W}{L} C_{ds} V_{th} \left[ \left( 1 + \frac{C_{dd}}{C_{ds}} \right) \left( \frac{u_s^2 - u_d^2}{2} \right) + (e^{-u_s} - e^{-u_d}) \right],
\]

(5)

where \( u_s = u(V_{Gd}) \) and \( u_d = u(V_{Gd}) \); \( C_{dd} = C_t + C_b \); \( W \) and \( L \) are the device width and length, respectively; and \( \mu \) is the carrier mobility which has been assumed to be dependent of the applied electric field, carrier density, and temperature as in ref.\textsuperscript{2}. Once we have a suitable expression for describing the static behavior of the device, the dynamic response must be analyzed to build a large-signal model. In doing so, the terminal currents in the time domain can be computed as:

\[
i_i(t) = \frac{dQ_i}{dt} = C_{ik} \frac{dV_k}{dt} + C_{id} \frac{dV_d}{dt} + C_{is} \frac{dV_s}{dt} + C_{ib} \frac{dV_b}{dt},
\]

(6)

where \( k \) stands for \( g, d, s, \) and \( b \), i.e. top gate, drain, source and back-gate, respectively. The terminal currents, thus, can be obtained by either computing the time derivative of the corresponding terminal charge or by the weighted sum of the time derivative of the terminal voltages, where the weights are given by the intrinsic capacitances.

The intrinsic capacitances of FETs are modeled in terms of the terminal charges. Specifically, from the electrostatics given in Eq. (1) the following relations are derived\textsuperscript{23,24}:

\[
Q_{gb} = Q_g + Q_b = -W \int_0^L Q_{nt}(x) dx,
\]

(7)

\[
Q_g = -Q_0 - \frac{WC_t}{C_{tb}} \int_0^L Q_{nt}(x) dx,
\]

(8)

\[
Q_b = -Q_0 - \frac{WC_b}{C_{tb}} \int_0^L Q_{nt}(x) dx,
\]

(9)

\[
Q_{db} = Q_d = W \int_0^L \frac{1}{L} Q_{nt}(x) dx,
\]

(10)

\[
Q_s = (Q_g + Q_b + Q_d) = W \int_0^L \left( 1 - \frac{x}{L} \right) Q_{nt}(x) dx.
\]

(11)

The above expressions can be conveniently written using \( u \) as the integration variable, as it was done to model the drain current in Eq. (5). Based on the fact that the drain current is the same at any point \( x \) along the channel (i.e. we are under the quasi-static approximation framework), we get from the transport model the following equations needed to evaluate the charges in Eqs. (7)–(11):

\[
dx = \frac{W}{L} \frac{dQ_{tot}(u)}{du} \frac{dV_k}{du} \frac{dV_d}{du} \frac{dV_s}{du} \frac{dV_b}{du} du,
\]

(12)

Replacing Eq. (12) in Eqs. (7) and (10), the following compact expressions are obtained for the terminal charges \( Q_{gb} \) and \( Q_d \):

\[
Q_{gb} = Q_d = 2 \left( \frac{2L}{u_s(C_{Gd} + C_b)} + \frac{Q_s}{C_{dd}} \right) \left( u_s^2 - u_d^2 \right) + \frac{u_s^2 - u_d^2}{2} + \frac{2Q_s}{C_{dd}} \left( u_s^2 - u_d^2 \right) - \frac{2Q_d}{C_{dd}} \left( u_s^2 - u_d^2 \right),
\]

(13)

where \( Q_{2D} = WLC_{tot}V_{in} \). Equation (13) can be replaced in Eqs. (8), (9) and (11) to get the terminal charges \( Q_g, Q_b \) and \( Q_s \) respectively. \( Q_s \) in Eq. (13) has been simplified by assuming that the term \( e^{(2u_d + 2u_s)} \) is prevalent over other low-order terms, e.g., \( e^{(u_d)} \) and \( e^{(u_s)} \).

Once the terminal charges are evaluated, a four-terminal FET can be modeled with 4 self-capacitances and 12 intrinsic transcapacitances given by:

\[
C_{ij} = -\frac{\partial Q_i}{\partial V_j} i \neq j \quad C_{ii} = \frac{\partial Q_i}{\partial V_i} i = j \quad i, j = g, d, s, b,
\]

(14)

where \( C_{ij} \) describes the dependence of the charge at terminal \( i \) with respect to a varying voltage applied to terminal \( j \) assuming that the voltage at any other terminal remains constant. Due to charge conservation and considering a reference-independent model, only nine independent capacitances are needed to describe the 4T device. In addition, taking advantage of the relations between the top- and back-gate capacitances,\textsuperscript{25} the computation of only four capacitances is enough; for instance, \( C_{ggb}, C_{gdb}, C_{dgb} \) and \( C_{dd} \) can be chosen as the independent set.

Model validation

In order to validate the presented model, we perform the DC and RF measurements of an experimental monolayer MoS\textsubscript{2}-FET. The fabricated device consists of an \( n \)-type channel of a chemical vapor deposited (CVD) MoS\textsubscript{2} monolayer transferred onto 285 nm intrinsic Si/SiO\textsubscript{2} wafer. The 150-nm-long MoS\textsubscript{2} channel is contacted with a stack of 2/70 nm Cr/Au and electrostatically controlled by an embedded gate formed by a 10-nm barrier of atomic layer deposited Al\textsubscript{2}O\textsubscript{3} and a gate metal stack consisting of 2/23 nm Ti/Au. More details on the fabrication and characterization process can be found in the Methods section. Table 1 summarizes the input parameters used for simulating the device under test. The extracted 2D semiconductor–metal contact resistance for the device is 3.5 kΩ μm and has been included in the simulation by connecting lumped resistors to the source and drain terminals.

We first test our model by comparing the DC transfer characteristics (TCs) obtained at two different drain voltages. A good agreement between both, measurements and simulations, has been achieved as shown in Fig. 2. The model predicts the DC behavior accurately in all regimes of operation with current values ranging between \( 10^{-3} \) up to \( 10^{2} \) μA/μm. However, the experimental device departs from the exponential trend for values in the limit of the 1D transcapacitance specification for low-power applications, being the OFF current actually limited by the onset of hole current at negative \( V_{gs} \) (see Supplementary Notes and Supplementary Fig. 51 for a detailed discussion). This small mismatch, however, does not impact the dynamic operation prediction. Indeed, we have assessed the expected RF performance of such device in Fig. 3 by benchmarking the simulated small-signal current gain (\( h_{21} \)) and unilateral power gain (\( U \)) against the results extracted from

| Table 1. Input parameters of the 2DFET under test. |
|-----------------|-----------------|-----------------|
| \( L \)         | 150 nm          | 21.2 cm\textsuperscript{2}/Vs |
| \( W \)         | 10 μm           | 0.48 m\textsuperscript{2} |
| \( L_t \)       | 10 nm           | 0.57 m\textsuperscript{2} |
| \( L_b \)       | 285 nm          | 9.11 \times 10^{-3} kg |
| \( \varepsilon_f \) | 9               | 22.27 cm\textsuperscript{2} |
| \( \varepsilon_r \) | 3.9             | 6.07 cm\textsuperscript{2} |
| \( V_{gs} \)    | 0.42 V          | 1.8 \times 10^{16} m\textsuperscript{-2} |
| \( T \)         | 300 K           | 0.085 eV |

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_carriers and the device operates in the OFF state. This situation happens for overdrive gate biases lower than the threshold voltage, $V_{th}$, according to Fig. 5e. Given the aforementioned conditions then $C_{gg} \approx C_{dd}V_C/WL$, and $C_{gd} \approx C_{sd} \approx C_{dd} = 0$, see to the left of A1 point in Fig. 5c.

*Saturation regime (ON operation)*: On the other hand, when $V_{ds} > 10V_{th}$, while $V_{cs} < 10V_{th}$, the pinch-off is originated at the drain side. This situation is produced for overdrive gate biases between $V_{a}$ and $V_{b}$ in Fig. 5e (“A–B” section). Both $C_{gg}$ (“A1–B3” section) and $C_{gd}$ (“A1–B2” section) jump because the channel charge at the source side becomes very sensitive to the Fermi level location when it is close to the conduction band edge. However, $C_{gd}$ and $C_{dd}$ are negligible (“A1–B1” section) because the depletion region close to the drain prevents this terminal to control the channel charge. The saturation regime is also observed at the right column of Fig. 5 for drain biases higher than $V_{C}$ (drain saturation voltage) in Fig. 5f (right of C point). The intrinsic capacitances $C_{gg}$ (right of C3 point) and $C_{dd}$ (right of C2 point), shown in Fig. 5d, decrease with respect to the linear regime (left of C point, explained below) because the channel is depleted at the drain side, so both $Q_{gg}$ and $Q_{dd}$ become less sensitive to $V_{ds}$, as compared to the linear regime. On the other hand, $C_{gd}$ and $C_{cd}$ are negligible (right of C1 point), as $Q_{gd}$ and $Q_{cd}$ cannot be controlled anymore by the drain terminal after the depletion of the channel drain side, which is confirmed in Fig. 5b.

*Linear (ohmic) regime (ON operation)*: This regime takes place when both $V_{cd}$ and $V_{cs} < 10V_{th}$. This situation is produced for gate overdrive voltages higher than $V_{a}$ in Fig. 5e (right of B point), where the channel starts to leave the depletion scenario at the drain side. Then a jump is observed in $C_{gg}$ (right of B3 point), $C_{dd}$ (right of B2 point), $C_{gd}$ and $C_{cd}$ (right of B1 point) as a consequence of the recovered electrical connection between the channel and the drain terminal (see Fig. 5a, c). The linear regime can be also observed at the right column of Fig. 5 for drain biases lower than $V_{C}$ (see Fig. 5f). The negative value of $V_{C}$ means that the channel is degenerated at the source side for the specific bias considered in this study. In Fig. 5d, it can be seen that $C_{gd}$ (left of C3 point), $C_{cd}$ (left of C2 point), $C_{gd}$ and $C_{dd}$ (left of C1 point) decrease with $V_{ds}$ as the channel gets closer to the drain depletion condition reached at $V_{ds} = V_{C}$.

Finally, with the aim of showing the potential of the developed TCAD tool, a relevant circuit commonly used to evaluate the performance of a digital technology, namely, a ring oscillator (RO) is simulated. The design of a three-stage based RO encompasses both DC and transient simulations. Each device has been described by the parameters shown in Table 1 that have been demonstrated to accurately reproduce the fabricated MoS2-based...
FET in Figs. 2 and 3. Specifically, we have designed the three-stage RO to oscillate at a specific frequency $f_{\text{osc}} = 3^{1/2}/(2\pi R_{\text{dd}} C) \approx 1 \text{ GHz}$ by using a resistor connected to each drain of $R_{\text{dd}} = 20.4 \text{ k}\Omega$ and capacitors connected to the output of each stage with $C = 13.5 \text{ fF}$. In doing so, each single stage has been designed to show a voltage gain of $3.7$ at $f_{\text{osc}}$, upon biasing it at $V_{\text{gs}} = 1.25 \text{ V}$ and $V_{\text{ds}} = 3.5 \text{ V}$. Figure 6 shows how the technology assessed in this work provides a suitable switching characteristic around $1 \text{ GHz}$. The simulation predicts a distorted sinusoidal as the AC component goes over a large range of bias with imperfect linearity. It is worth noticing that a small-signal model (in contrast with a large-signal model) could not predict that feature. Supplementary Fig. S3 provides a comparison of the compact model outcome against experimental measurements of bilayer MoS$_2$ FETs$^{26}$ comprising the assessment of transfer characteristics, output characteristics, the performance of an inverter, and a five-stage ring oscillator based on such devices, the latter validating the large-signal prediction capability of the model.

**DISCUSSION**

A physics-based large-signal compact model of four-terminal 2D semiconductor-based FETs, implemented in Verilog-A, has been presented. The model captures the terminal charges and capacitances covering all the operation regimes, so accurate time domain simulations and frequency response studies at the circuit level are feasible within the validity of the quasi-static approximation. The model can be incorporated to existing commercial circuit simulators enabling the simulation of digital and RF applications based on emerging 2D technologies. We have checked that the
model outcome is consistent with our experimental measurements of MoS₂-FET devices targeting RF applications. Finally, a design of a three-stage ring oscillator has been carried out to exhibit the potential of the TCAD tool presented and showing the feasibility of using this technology in switching applications in the gigahertz range.

METHODS

Fabrication

The MoS₂ FET reported in this paper belongs to the same batch as the devices published in ref. 23 by some of the authors. The fabrication process begins with patterning two embedded gate fingers on intrinsic Si/SiO₂ (>20 kΩ cm). Then, the embedded 150-nm gate metal stack consisting of 2/23 nm Ti/Au was defined and deposited by using electron beam lithography (EBL) and e-beam evaporation. Large area atomic single layer CVD MoS₂, grown by a standard vapor transfer process as described in ref. 24, was then transferred by poly(methyl methacrylate)-assisted wet transfer. Phosphoric acid etching was used to connect the embedded gate fingers and the gate pad. The active MoS₂ channel was etched using Cl₂/O₂ plasma. Finally, source and drain (S/D) contacts consisting of 2/70 nm Cr/Au were patterned through a final EBL step.

Electrical measurement

The electrical DC characterization was done on a Cascade Microtech Summit 11000B-AP probe-station using an Agilent B1500A parameter analyzer. Microwave performance was characterized using an Agilent two-port vector network analyzer (VNA-E8361C). All measurements were taken at room temperature, in ambient atmosphere, and in the dark. The intrinsic microwave performance is obtained after de-embedding the measured data using OPEN and SHORT structures. The OPEN de-embedding was performed on the as-measured device-under-test by etching away the MoS₂ in the active regions. The SHORT de-embedding is subsequently carried out by depositing a strip of metal across the channel region, shorting out all pads.

Circuit simulation

The developed large-signal model of 4T 2DFETs is implemented in Verilog-A and included as a separate module in Keysight® Advanced Design System (ADS), a popular electronic design automation software for RF and microwave applications. It calculates the electrostatics by iteratively solving Eqs. (1) and (3) during run-time using a construct, 21,22 and computes the static and dynamic response of the device by evaluating Eqs. (5) and (6), respectively, using the compact expressions derived in this work.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

CODE AVAILABILITY

The large-signal model of 2DFETs implemented in Verilog-A is available from the corresponding author upon reasonable request.

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AUTHOR CONTRIBUTIONS
F.P. and D.J. performed the development of the analytic model and the Verilog-A implementation. F.P., E.G.M., A.T.-L., and F.G.R. contributed to perform and interpreting the simulations. A.G. and D.J. overall supervised the compact model development and analyzed the results. S.P. performed the synthesis and characterization of the MoS₂ films, as well as performed the design conception, fabrication, and measurements of the MoS₂ transistors under the direction and supervision of D.A. F.P., and D.J. wrote the manuscript. F.P., E.G.M., F.G.R., A.G., D.A., and D.J. contributed to the scientific discussions. All authors revised and approved the final manuscript.

COMPETING INTERESTS
The authors declare no competing interests.

ADDITIONAL INFORMATION
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Supplementary Information: Large-signal model of 2DFETs: Compact modeling of terminal charges and intrinsic capacitances

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Extended transfer characteristics of the MoS₂ FET under test

Fig. S1 – Extended transfer characteristics covering all operation regimes for two different drain voltages. Dashed lines highlight both the IRDS high-performance and low-power off current limits.

Fig. S1 shows the transfer characteristics (TCs) over an extended range of gate voltages. According to our simulations (solid lines), the threshold voltage of the analyzed device is $V_{th} \sim 0.42$ V. It can be observed that from the near-threshold down to the subthreshold region, the model departs from the experimental DC measurements (symbols). This is likely to happen because of the channel ambipolarity [1],[2], which has not been considered in the model. In spite of the n-type contact design, the fabricated device was not optimized to suppress hole conduction. Consequently, a residual hole current at negative $V_{gs}$ appears as can be expected in intrinsic or low doped channels. It is worth noticing that the mismatch between the model and the experimental measurements is observed for current values below the IRDS limit for the OFF current in both low-power ($10^{-4} \mu$A/µm) and high-performance applications ($10^{-1} \mu$A/µm) (horizontal dashed lines in Fig. S1) what limits its impact in practical circuit applications and has a negligible effect in the circuit-level predictions of the model. Nevertheless, our model works properly for other devices that do not exhibit the residual hole current, as demonstrated in Refs. [3], [4].
Simplified capacitance model used to compare the proposed model

Equations 13 and 14 of the main manuscript are written here for convenience:

\[
Q_{gb} = Q_{2D} \frac{2}{6C_{ib}} \left( e^{\nu_s} (1 + u_t) - e^{\nu_d} (1 + u_d) + e^{\nu_s} e^{\nu_d} \left( C_{dq} + C_{ib} \right) \left( u_d^3 - u_t^3 \right) \right)
\]

\[
Q_d = -Q_{2D} \frac{2}{15} \frac{3u_d^5 - 5u_d^3u_t^2 + 2u_t^5}{(u_d^2 - u_t^2)^2}
\]

\[
C_q = -\frac{\partial Q_i}{\partial V_j} \quad i \neq j \quad C_q = \frac{\partial Q_i}{\partial V_j} \quad i = j \quad i, j = g, d, s, b
\]

The well-known simplified capacitance model presented for bulk MOSFETs [5] and later used to model 2DFETs [4] is obtained by evaluating the partial derivatives in (S.2) using the following simplified expressions for the terminal charges:

\[
Q_{gb} = -(Q_d + Q_s)
\]

\[
Q_d = Q_{n0} \frac{4 + 8n + 12n^2 + 6n^3}{15(1+n)^2}
\]

\[
Q_s = Q_{n0} \frac{6 + 12n + 8n^2 + 4n^3}{15(1+n)^2}
\]

\[
Q_{n0} = -WL \frac{Q_{net}(x=0) + Q_{net}(x=L)}{2}
\]

This simplified charge model uses an empirical function of the drain bias, \( \eta \), to provide a continuum between the different regions of the transistor operation [4]–[6] going from the linear regime \( \eta = 1 \) to the saturation regime \( \eta = 0 \). It also assumes that the net charge density is linear along the channel \( (Q_{n0}) \), being this approach accurate only when either a low drain bias is applied or if the device is operated in the subthreshold regime [5], which in turn is in agreement with the comparison shown in FIG. 4 of the main text. In addition, Fig. S2 depicts the charge density profile along the 2D channel for different drain biases showing that it departs from linearity for higher drain biases, a fact that is captured by the model presented in this work (S.1).

Fig. S2 – Channel charge density along the normalized channel length of the n-type MoS\(_2\) based FET described in Table I of the main text \((V_{gs} - V_{g0} = 1\text{V}; V_{ds} = 0.2 \text{ to } 1\text{V in steps of 0.2V})\).

Note that using the set of equations in (S.1) instead of the set in (S.3), provides a picture more consistent with the underlying physics, as demonstrated in the main text of this work (see Fig. 5 of the main text). Specifically, the difference between both models is shown in solid lines (S.1) and dashed lines (S.3) in Fig. 4 of the main text.
**Five-stage ring oscillator based on bilayer MoS$_2$ transistors**

![Graphs and diagrams illustrating the performance characteristics of bilayer MoS$_2$ transistors and a five-stage ring oscillator.](image)

**Fig. S3** – Measurements (symbols) and simulations (solid lines) of **A** the transfer characteristics of depletion (D-) mode and enhancement (E-) mode bilayer MoS$_2$ FETs; **B** the output characteristics of the E-mode bilayer MoS$_2$ FET; **C** the output voltage as a function of the input voltage for a bilayer MoS$_2$ logic inverter (inset: schematics of the bilayer MoS$_2$ based inverter); and **D** the output voltage of a five-stage ring oscillator at a supply bias of 2V. The fundamental oscillation frequency is ~1.6 MHz corresponding to a propagation delay per stage of 62.5 ns.

To assess the validity of the proposed compact model, we have performed a variety of simulations comprising dc transfer (TCs) and output characteristics (OCs), the inverter characteristics and the performance of a five-stage ring oscillator based on depletion (D-) and enhancement (E-) mode bilayer MoS$_2$ FETs reported in Ref. [7]. Both D- and E-mode 2D-FETs effectively shift their threshold voltage by about ~0.76V due to a difference in the work function of each metal gate employed in the fabrication process. Specifically, the metals were Al and Pd [7]. Table S1 shows the input parameters used for simulating both devices, where a difference of 0.8V has been applied to the parameter $V_{g0}$ to split the FET operation into D- and E-modes. This parameter has been defined in the main text as a quantity that comprises work-function differences between the gate materials and the 2D channel and any possible additional charges due to impurities or doping.

Fig. S3A shows the comparison between measurements and simulations of the TCs of both devices. Similarly to the TCs of our device (see Fig. S1), residual holes dominate the current at negative gate voltages. It is worth noticing a shift in the threshold voltage likely induced by the drain bias, which is not captured by our model. However, that effect is not apparent in the device analyzed in the main manuscript. Fig. S3B shows the
comparison of the OCs of the E-mode bilayer MoS$_2$ FET. In the saturation region, a mismatch between the model prediction and the dc measurements is detected which we attribute to a channel-length modulation effect [5], not considered in our model. In spite of these small mismatches the model captures to a very good degree large-signal operation. In particular, Fig. S3C shows the output voltage as a function of the input voltage in a bilayer MoS$_2$ based inverter formed by the series combination of a D-mode FET in resistor configuration and an E-mode FET (see inset of Fig. S3C). A voltage gain close to 5 is achieved and used to build a five-stage ring oscillator. In doing so, a loop is constructed by connecting five inverters in series. Fig. S3D shows the output voltage switching at a fundamental frequency of ~1.6 MHz corresponding to a propagation delay per stage of 62.5 ns.

TABLE S1. Input parameters of the D- and E-mode bilayer MoS$_2$ FETs reported in [7].

| Parameter | Value |
|-----------|-------|
| $L$       | 1 µm  |
| $W$       | 4 µm  |
| $L_t$     | 18 nm |
| $L_b$     | 285 nm|
| $\varepsilon_t$ | 25    |
| $\varepsilon_b$ | 3.9   |
| $V_g0$    | -0.4 V and 0.4 V |
| $V_b0$    | 0 V   |
| $\mu_0$  | 22 cm$^2$/Vs |
| $m^k$ [8] | 0.542$m_0$ |
| $m^d$ [8] | 0.579$m_0$ |
| $m_0$     | 9.11·10$^{-31}$ kg |
| $g_k$     | 2     |
| $g_0$     | 6     |
| $\Delta E_2$ [8] | 0.066 eV |
| $T$       | 300 K |

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