A way out of this dilemma is to stop treating generated code and its performance as an intangible black box but to make accurate predictions instead about the resulting performance. This is accomplished by a metric estimator that computes the inputs for a performance model.

The main advantage of this approach is a much quicker evaluation time compared to the generation-compilation-benchmark cycle. We design the hardware metric estimator with two goals in mind: It must only require high-level features from the code generator that are already available before the actual source code text is generated, and it must be quickly evaluable.

Since there is no actual code execution in this process, it does not require the target hardware, saving valuable resources especially when high-end GPUs are involved. It also enables the performance comparison of different GPU models, including hypothetical GPUs for architectural exploration. A performance model can not just evaluate different code configurations on different hardware, but it can also grant insight into why the performance is the way it is. Knowing the performance-limiting factors can inform further development of both algorithms and code generation capabilities.

B. Pystencils

We show the utility of our performance estimator and how it can be used in a code generator using the open-source python library pystencils [1] as an example. With pystencils, mathematical models can be directly described in an abstract representation. It is possible to automatically derive essential numerical schemes like the finite difference or the finite volume method from the abstract representation. Thus, complex mathematical models like multi-phase solidification models [1] can be described in a high-level latex-like representation close to usual descriptions in the literature. Furthermore, other packages like the Lattice-Boltzmann-Method (LBM) code generation framework lbmpy [2]. [3] build on top of pystencils to derive highly optimized numerical schemes for solving flow problems. From the numerical schemes, pystencils then generates low-level C/OpenMP code to target CPUs or CUDA/OpenCL for GPUs.

As an example, consider the following 2D4Pt stencil:

\[
dst[0,0] = (src[1,0] + src[-1,0] + 
src[0, 1] + src[0, -1]) / 4
\]
This example consists of a single assignment with relative field access to the destination and the source field dst and src. Pystencils then lowers this representation to its target dependent intermediate representation, where the relative field accesses are replaced with expressions computing the referenced addresses based on the thread coordinates, and the iteration space is realized either with explicit loops or mapped over hardware thread coordinates. For example, for the access src[1,0] to the left neighbor, the referenced address would be computed on a GPU by this expression:

```
src_W = src +
    (threadIdx.x + blockIdx.x*blockDim.x + 1) +
    (threadIdx.y + blockIdx.y*blockDim.y) * w
```

The address expressions must contain only the base address of the field, and the thread and block coordinates as free fields. Our performance estimator takes these address expressions, together with the launch configuration, field sizes and field alignments as the only high level information required from a code generator. Our estimator is therefore not specific to pystencils, but can be integrated with any code generation framework that is able to generate these artifacts.

The requirements on the address expressions also introduces limitations to the applicability of our performance estimator. First, variables like grid sizes need to be known at generation time and indirect addressing is not supported. It possible to work around this using representative proxy values.

Second, control flow needs to be fully resolved beforehand. For very likely or unlikely, branches, it is often possible to simplify the control flow and still get a meaningful result. The frequent if(tidx >=N ) return 0; at the top of many GPU kernels, is false for almost all grid points and thus can be dropped without changing the result.

Another example are grid stride loops, where each thread would iterate over many points of the computational domain. In this case, the code generator can emit the address expressions for just use one or a few iterations, and normalize the performance to the amount of work performed in these loop iterations.

C. Contributions

In this paper, we make the following significant contributions. We extend the roofline performance model for GPUs by two additional limiters related to cache bandwidth. We present a method to estimate the cache hierarchy data volume metrics required for this model based on the address expressions used to compute the memory addresses referenced by a GPU program. We propose the combination of the model and the metric estimator for use by code generators, which can generate these address expressions and use the combination to classify different code generation options and run configurations. In this context, we demonstrate the usefulness of the method for distinguishing badly- from well-performing configurations and identifying which type of configuration performs best on a V100 GPU on two different, challenging applications implemented in the stencil code generation framework pystencils.

D. Related Work

There are numerous code generation frameworks for stencils on GPUs. These frameworks use either autotuning, or a performance model that is specific to their requirements. For example, the authors of [4] use a model to optimize the computation/register ratio, which is important for the class of stencils they are targeting. In [5], a standard roofline model with a fixed, theoretical memory volume is used for a full exploration of the configuration space, followed by benchmarking the top five candidates.

Similarly to our strategy, the framework LIFT [6], [7] extracts low-level features from an intermediate representation (IR), and then uses a machine learning approach to predict performance based on the extracted code features.

The roofline model [8], owes its popularity and wide applicability to its simplicity, as it uses just two performance limiters that apply to any architecture: memory bandwidth and peak floating-point performance. These have been extended with cache-related limiters in the hierarchical roofline model [9] where data transfers volumes measured via hardware performance counters are used to determine how close each memory level’s bandwidth is to being a limiter. NVIDIA’s own mvp and nsight profiling applications do not just measure hardware quantities using performance counters but also evaluate the measured results by comparing them with the maximum possible rates. This could be regarded as a multi-limiter performance model that includes every limiter that is measurable with performance counters.

In order to make a prediction, performance models focused on the memory hierarchy require application specific inputs in the form of the data volumes transferred in the memory hierarchy.

One work that attempts to estimate these metrics for GPUs is [10]. They put GPU simulator traces into a reuse-distance-based model with time stepping that can also resolve timing-based effects, which is potentially more precise in determining memory hierarchy data volumes than our approach. They however employ much more involved simulations and require GPU execution traces.

The work presented in [11] targets the same usage scenario and uses a similar performance model to ours. It also describes capacity miss effects probabilistically and performs a similar evaluation to ours. The biggest difference is in using analytical formulas specific to a particular stencil to compute the memory volumes, which limits the applicability to stencils, whereas our estimator does not have such a limitation.

II. Theory

A. Performance Model

The naive roofline model is often imprecise because frequently, applications can saturate neither of the two performance limits. In this work we additionally consider the data transfers between L2 and L1 and between L1 and the registers, which may become the bottlenecks instead in applications with effective cache reuse.
The four limiters considered here are a reasonable selection out of a wide range of options. They yield a more differentiated performance ranking by finding performance deviations between among variants which the roofline model would consider equivalent. The selected set of limiters is general enough to be applicable to all common GPU architectures, the underlying these mechanisms can be reasoned about without too much architectural inside knowledge, and the associated metrics can be accurately estimated using high-level methods, as shown in the next section.

III. METRIC ESTIMATION

A. Floating Point Execution

The number of floating-point operations, needed for the FP throughput limiter, is straightforward to get from the source code. The code generator performs common optimizations such as constant folding and common subexpression elimination to anticipate the changes that the compiler probably would do. For the applications and configurations covered here, the floating-point execution rate is never the limiter and will thus not be considered for the rest of this paper.

B. L1 Cache to Register Transfers

The number of cycles required to transfer data from the L1 cache to the registers depends on the access patterns. In the best case, Volta and Ampere can transfer 128B per cycle, or one unique 8B double precision (DP) value for each thread in a 16-wide half warp. The 128B cache lines are distributed over 16 cache banks, each of which can deliver 8B per cycle. A half warp memory access instruction can access data from different cache lines in a single cycle, as long as at most one value per cache bank is required. Each additional address per cache bank requires an additional cycle. Consider the four loads in the following listing and the illustration in figure 1:

```
  double a = A[threadIdx.x];
  double b = B[threadIdx.x*2];
  double d = D[threadIdx.x*32];
```

The consecutive addresses in the load from A have no bank conflicts and result in one cycle per half warp. Load B loads only every other 8B address, resulting in two addresses per cache bank, which are loaded in two cycles per half warp. The worst case is represented by the load from D, where all addresses are in the same cache bank and have to be loaded over 32 cycles per half warp.

C. Data Volumes

A key property of memory accesses is their spatial and temporal locality. For GPUs, temporal and spatial locality of a single thread’s accesses is less relevant than the collaborative reuse among multiple threads running on the same cache level. It is therefore not enough to look at a single thread in isolation to determine the amount of transferred data, but at the group of threads that share a cache level.

We denote the total volume of data transferred by a cache level (reads and writes) due to incoming requests from the level above it as $V_{up}$, and the volume of data caused by requests of that cache level to the level below it as $V_{down}$ (see figure 2).

For memory hierarchy levels $N$ and $N-1$ (the latter being closer to the registers), we have $V_{up}^N = V_{down}^{N-1}$. $V_{down}$ can be split into three components [12]:

$$V_{down} = V_{comp} + V_{cap} + V_{conflict} \quad (1)$$

D. Compulsory Misses

$V_{comp}$ is caused by misses on the very first access to addresses. Every piece of data has to be transferred into a cache at least once for each set of threads that have the chance to share data in a cache level. We refer to such a set of threads as a collaborative group for that cache level. The total data volume $V_{up}$ between a cache level and the memory hierarchy level above can be split up into the compulsory volume $V_{comp}$, which consists of the data accessed for the first time by that collaborative group, and the redundant volume $V_{red}$ comprising repeated requests for data:

$$V_{up} = V_{comp} + V_{red} \quad (2)$$

A collaborative group’s compulsory data volume $V_{comp}$ for a cache level is its unique data footprint in that level. The unique data footprint is the set of unique addresses accessed by the threads in the group at the granularity of cache lines.
To estimate the footprint, we compute the cardinality of the set of cache lines referenced by all threads in a representative collaborative group in all memory accesses of a kernel. Figure 3 shows an example where for each of the four memory accesses, the four threads access four different addresses. The total amount of accessed addresses is then 16, but the unique footprint consists of only 10 addresses since 6 are redundant.

We do this individually for each array and replace the unknown base address of the array either by zero or by the alignment of that array. Averaging over several representative groups makes sure that the computed data is not an outlier caused by, e.g., being a set of threads on a boundary by or alignment issues. We employ two different methods to compute data footprints from addresses.

1) Enumeration: The first method is a direct enumeration of all addresses. Listing 4 shows an example of how we use a generic grid iteration function that can be customized with different visitors for different applications. The example uses a visitor that counts unique 32B cache lines to compute the L2 load block footprint. The different accessed fields are counted separately, because the base addresses of the arrays are replaced by the alignment, so that addresses of different fields could not be kept apart. This assumes no aliasing among different fields. The evaluation of the thread coordinates inside a collaborative group is vectorized using numpy’s meshgrid function. This explicit enumeration has the advantage of the performance being largely independent of the complexity of the address expressions. However, the evaluation runtime shares the $O(n \log n)$ complexity of the unique function regarding the number of threads in the collaborative group. This can become relevant for the computation of large grids.

2) ISL: The second method avoids this complexity by using abstract representations of the address sets and computing these sets using the Integer Set Library (ISL). For example, the following definition could be used to specify the set of all two-dimensional thread coordinates in a 128×4 thread block:

$$\text{threads} := \{(tidx, tidy) : 0 \leq tidx < 128 \land 0 \leq tidy < 4\}$$

For each access to an array, a mapping from a two-dimensional thread coordinate to a linear index is defined. This example shares the

$$O(n \log n)$$

of the address expressions. However, the evaluation runtime

$$\text{cap} = 100 \times \frac{\text{red}}{V}$$

The advantage of this method is the decoupling of the evaluation runtime from the number of threads in the grid, which is good for large thread grids. The ISL also allows to compute more advanced set relationships, like the intersection of two address sets, which we use to compute the overlap of the two different data footprints.

E. Capacity Misses

Capacity Misses happen when a redundant access misses because the data has already been evicted due to insufficient capacity hold both that piece of data and all the data accessed since the first access. While the order of memory accesses inside a thread is fixed, the memory access order among different warps is not deterministic. It is therefore impossible to analytically compute the exact amount of capacity misses, but it is possible to identify scenarios where capacity misses happen at all and to estimate the extent.

We define the capacity miss ratio $R_{\text{cap}}$ as the the portion of redundant accesses that will miss the cache:

$$R_{\text{cap}} = \frac{V_{\text{cap}}}{V_{\text{red}}}$$
We assume that the major factor that influences this portion is the data volume \( V_{alloc} \) allocated for the collaborative group in the cache. The allocation volume can be different from \( V_{cap} \), for example in the case of Volta’s L1 cache that uses a 128B for cache line allocation, but a 32B granularity for data transfers. We define the oversubscription factor of that cache level as the ratio of the available cache capacity \( V_{cache} \) and the allocation volume:

\[
O = \frac{V_{cache}}{V_{alloc}}
\]  

It is impossible to give an analytic formula \( R_{cap}(O) \) for even a single application, but the behavior of that relationship in the limit can be characterized. For an oversubscription factor less than one, there is enough cache capacity for the complete footprint and \( R_{cap} \) should be zero. At the opposite end of the spectrum for very large oversubscription, \( R_{cap} \) should be large but not exceed one.

As a stand-in for a smooth transition between the two states we fit a sigmoid function of the form \( \hat{R}(O) = ae^{-be^{-cO}} \). This function is not grounded in any real world mechanism, and other functions that smoothly interpolate between the two states could be used.

The capacity miss volume is then the product of the capacity miss ratio and the redundant volume, which can be computed as the difference between \( V_{up} \) and \( V_{comp} \):

\[
V_{cap} = \hat{R}_{cap}(O)V_{red} = \hat{R}_{cap}(O)(V_{up} - V_{comp})
\]  

Conflict Misses happen when data is being evicted earlier than necessary because cache aliasing reduces the effective cache capacity. They are not considered in this paper as a phenomenon separate from the capacity misses, as the occurrence of aliasing is to dependent on the details of an architecture’s cache organization and also highly volatile.

**F. L2 to L1 Cache Transfers**

The relevant cooperative group for the L1 cache are the threads in a thread block, which can share data in the L1 cache of the SM they run on. We do not consider sharing between threads of different thread blocks running on the same Streaming Multiprocessor (SM), as mostly only thread blocks that are neighbors in the thread block grid have overlap in their data footprints. As the kernel launch execution progresses, the assignment of thread blocks to SMs becomes increasingly incoherent, and we consider the scheduling of neighbouring thread blocks to the same SM as the unlikely case.

Volta’s L1 cache allocates at the granularity of 128B cache lines, but transfers data the granularity of the 32B cache line sectors. Therefore, we compute the unique data footprint using 128B for \( V_{alloc} \), but using 32B cache line sectors for \( V_{comp} \).

The L1 cache uses a write-through policy, so that repeated stores to the same address have to be counted individually for \( V_{down} \), so that \( V_{up} = V_{down} \) for stores. Though loads can hit in the L1 cache on stored data, we do consider this in our estimator, as numerical code rarely mix reading and writing to the same memory locations in the same kernel.

**G. DRAM to L2 Cache Transfers**

The L2 cache is a chip-wide shared resource, so that all threads running on all SMs can share data in the L2 cache. Only a comparatively small portion of the thread blocks in a kernel call grid can run concurrently. New thread blocks are scheduled in \( X - Y - Z \) order as older thread blocks complete, which results in a transient wave of running thread blocks with sharp leading edge. To simplify this, we subdivide the total thread block grid into discrete waves of concurrently running thread blocks. Inside the wave, all thread blocks are considered to run simultaneously and do not have any execution order. Considering only sharing data inside a wave, the compulsive DRAM-L2 cache volume is the unique memory footprint of all threads of that wave.

To account for the reuse of data from the previously running wave, we not only compute the unique L2 data footprint \( V_{curr} \) of the current representative wave, but also compute its overlap \( V_{overlap} \) with the previous wave’s footprints \( V_{prev} \). This overlap \( V_{overlap} \) would then represent the data that the currently running wave could hit on from the previous wave and would not have to be transferred again. We treat capacity misses in this volume differently from other volumes, as we assume that all accesses the previous wave happen before the accesses of the current wave and will also be replaced first. Therefore, instead of the oversubscription factor \( O \), we use the coverage factor \( C \) as the ratio of the previous’ wave volume and the remaining L2 cache capacity after the new volume has been deducted:

\[
C_{over} = \frac{V_{cache} - (V_{curr} - V_{overlap})}{V_{prev}}
\]  

The coverage factor can become negative, if the current wave’s footprint already exceeds the L2 cache capacity.

Different to the L1 cache, repeated stores are not directly written through but get cached in the L2 cache. Because store cache lines are potentially replaced differently, we use separate fit functions \( R_{L2,store}^{cap} \) and \( R_{L2,load}^{cap} \).

**IV. EVALUATION**

**A. Test Environment**

All measurements are made on a NVIDIA Tesla V100-PCIe-32GB GPU using CUDA version 11.3. This V100 GPU consists of 80 SM’s clocked at 1.38 GHz. The L2 cache has a capacity of 6MB and the the L1 cache is configured at 128kB. We measured a memory bandwidth for stream kernel scale of 790GB/s, and a L2 cache bandwidth of 2500GB/s.

**B. Data Points**

The accuracy of the metric estimator and the performance model is evaluated by comparing predictions and estimates for a range of different thread block sizes \((X, Y, Z)\) that fulfill:
The grid size for the stencil is $640 \times 512 \times 512$.

### D. Multi Phase LBM

The second application is a LBM kernel using the conservative Allen-Cahn model, which can solve highly complex two-phase-flow phenomena.

We will focus on the kernel doing the interface tracking, which is one of two LB schemes that this method consists of. The curvature of the phase field is computed with a finite difference discretization, which adds a 3D7pt stencil to the conventional, very memory intensive D3Q15 LBM stencil. This makes it particularly complicated to achieve good performance results [3], but at the same time interesting for automatic performance estimations, which can give significant insight into the complex structure of the compute kernels.

Each lattice cell is resolved with 15 pdf values for the LB calculation, and additionally, the information of the phase-field of 6 neighboring lattice cells is needed. For propagating the pdf values to the neighboring lattice cells, a pull scheme is used. Thus the stores are aligned, and the loads are not. The D3Q15 stencil LBM part of the kernel transfers a data volume of $2 \times 15 \times 8B = 240B/Lup$ read and write without any reuse, compared to the just $16 - 64B/Lup$, depending on the cache effectiveness, for the finite-difference stencil.

### E. L1 Load Volume

Figure [3] shows the prediction of how many cycles each warp occupies a SM’s L1 cache for a single lattice update. For the access patterns of the two kernels, the thread block width is also the width of the contiguous blocks of accessed memory. For 16 threads or higher, each half-warp of 16 threads loads a single contiguous block without any bank conflicts, that can be loaded in a single cycle. With each decrease in the thread block width, the number of bank conflicts increases. The L1 time per lattice update can be decreased through thread folding, which

---

**Fig. 5:** Estimated cycles for one lattice update of a 32 wide warp

**Fig. 6:** 3D25pt/range 4 star stencil

**Fig. 7:** LBM Kernel

Predicted vs measured L2-L1 loaded data volume. Data points colored by block size. Gray markers and arrows show comparison without modeling capacity misses.
is shown for one data point and 2× thread folding in the y-direction, because values can be reused from registers instead of reloading them.

F. L2-L1 Data Volume

Figures 6 and 7 plot the estimate of the L2-L1 cache load data volume in comparison to the actual data volume measured using hardware performance counters. Plot points on the diagonal would be block sizes where the estimate is identical to the actual value, whereas points in the upper-left / lower-right triangular area of the plot are over / under estimated.

In figure 8 these predictions are broken down into compulsory and capacity reason for a selected number of thread block sizes. The shown L1 cache volume is an upper limit on the L2-L1 volume, and would be completely filled by the capacity miss bar if $R_{cap} = 1$, and empty if $R_{cap} = 0$.

For the stencil, the different thread block sizes cause a wide range of L2-L1 cache data volumes. Pale, low saturation colors, representing thread block sizes with balanced, cube shaped dimensions, e.g. (16, 8, 8), have the lowest volumes due to their low surface volume ratio. For the same reason, thread block sizes with one short dimension, e.g. (512, 2, 1) or (2, 512, 1), colored in more saturated primary colors, have higher data volumes. A very short x dimension e.g. (1, 16, 64), represented with colors without red, i.e. green and blue, lead to both inefficient use of the transferred 32B cache line sectors, and also inefficient allocation of 128B cache lines and consequently, large amount of capacity misses.

Thread folding in the right dimension leads to lowered compulsory volumes, but also to increased capacity misses. The majority of the data points that have capacity misses are using thread folding.

The difference in the compulsory volumes is less pronounced for the LBM kernel, due to the high amount of streaming data volume. The streaming component favors a x dimension as large as possible, as this minimizes the percentage of partially used cache lines used by unaligned loads. As a compromise with the preference of the stencil part for cubed shapes, thread block sizes like (32, 2, 2) show the lowest volumes here. The amount of capacity misses is generally very low. We assume that the non-LRU replacement policy of Volta’s L1 cache replaces data with streaming access patterns preferentially, so that the data of the stencil component is not displaced by the large data volume loaded by the LBM part.

As a future extension, it would be possible to automatically classify allocated data volume into streaming, i.e. a single reference, and reuse volume to differentiate the two scenarios.

Figure 9 plots the measured $R_{cap}$ against the oversubscription factor of the L2 cache, and the sigmoid fit function that we use to estimate $R_{cap}$.

G. DRAM-L2 Data Volume

The factor $R_{overmiss}$ can be derived from a memory volume measurement by deducting the minimal compulsive data volume excluding the overlapping data volume from the measured data volume and dividing the difference by overlapping volume. This derived overlapping data miss ratios is plotted in Figure 10 against the the previous wave coverage, together with the fit of a sigmoid function that we use to model $R_{overmiss}$.

The values for $R_{cap}^{L2,load}$ and $R_{cap}^{L2,store}$ can be similarly derived from the measurements by deducting the compulsory volumes and overlap capacity misses from the measured data volumes, the results of which are plotted in Figures 11 and 12 against the oversubscription factor. Both ratios again are not a simple function of the oversubscription factor, but show a transition from low capacity miss rates at sufficient coverage to a range of miss rates at higher oversubscription, which we represent with the shown sigmoid fit functions.

Figure 14 shows a comparison of the memory load volume predictions of all stencil data points against the measured volumes. The plot shows that thread blocks can be sorted by color into three categories, which are also represented in the detailed breakdown by component in figure 13. Purple or violet colors, i.e. wide and deep thread block sizes with large x and z dimensions, e.g. (32, 1, 32), have the lowest volumes. Yellow/orange colors, representing wide and tall thread block sizes with large x and y dimensions, e.g. (32, 32, 1), have larger data volumes. Green, tall thread blocks with a large y component, e.g. (2, 512, 1), have the highest data volume.

The deeper thread block sizes, i.e. large z dimension, result in a lower balance because the grid is filled with thread blocks in x, y, z order. Most of the time a wave consists only of one layer of thread blocks in the z direction, making the z extent of the whole wave entirely dependent on the depth of a single thread block. A very shallow wave, i.e. low z extent, results in little reuse in z direction and hence high volumes.

The capacity miss effects are largest for tall blocks with a large y component and short x component. These block sizes combine large L2 cache data allocations with many redundant L2-L1 data transfers, each of which is a potential capacity cache miss.

Thread folding in the right dimension can reduce the compulsory data volume, see e.g. (32, 32, 1). A 2y thread folding is counterproductive here, as the y component of the wave was already large. The resulting large overlap with the previous wave does not come to fruition due to the increased L2 cache allocation and correspondingly increased capacity miss rates.

The 2x thread folding instead doubles the z extent of the wave from one to two, which improves the surface volume ration of the wave and leads to a smaller compulsory volume.

Figures 16 and 17 show the same data for the LBM kernel. The streaming nature of the LBM part of the kernel leads to a much smaller dependence on the z extent than the stencil. Instead, the memory data volumes for the LBM kernel are mostly influenced by the thread block x dimension. The shorter the x extent of a thread block, the fewer complete cache lines
are loaded by a thread block in comparison to the partial cache lines loaded at the thread block boundary due to the unaligned LBM component loads, and the larger the amount of redundant loads. This is even more valid for $x = 1, 2$, where all loads access only partial cache lines. This is reflected in the component breakdown in figure 15 by decreasing L2 load volumes with increasing $x$ extent. Combined with increased L2 cache allocation when a wave does not fill a $x$ row completely, this leads to capacity misses for small $x$ extents.

H. Performance

Figures [17] and [18] show comparisons of the predicted performance using the estimated data volumes as input for the presented performance model. The gray comparison markers show the difference to a phenomenological prediction that uses the same performance model but measured data volumes. For both applications, the performance model shows overprediction, regardless of whether estimated or measured data volumes are used.

For the 3D25pt range-four star stencil, the predictions are able to rank the different configurations by performance and clearly captures the performance differences between well-performing and badly-performing configurations. The configuration with the best predicted performance, $(16, 2, 32)$ without thread folding, is the 13th best out of 162 configurations at 86% $(27.6GLup/s)$ of the performance compared with the fastest measured configuration, $(32, 2, 16)$ with 2$z$ thread folding at 31.9GLup/s. The inability to find the actual fastest configuration is not due to inaccurate data volumes, as the phenomenological performance model using measured data volumes picks the same configuration as the fastest. The performance model cannot resolve the differences among the collection of well-performing configurations. It does, however, correctly identify the general type of configuration that performs well, as the best-predicted and best-measured configuration do have similar shapes.

This is a relevant accomplishment, which is illustrated by comparison with the thread block sizes found in [13]. They
find that among the sizes \((8, 8, 8), (16, 16, 4)\), and \((32, 32, 1)\), the first one performs best for the application of a very similar stencil to the one we used. However, we find that in our measurements, the best predicted thread block size \((16, 2, 32)\) is \(36\%\) faster than a \((8, 8, 8)\) thread block size. It is a nonintuitive insight that a \((16, 2, 32)\) thread block size performs better than the \((8, 8, 8), (16, 16, 4)\), or \((32, 32, 1)\) thread block sizes they have selected.

For this stencil, the most important limiter, especially with the fastest configurations, is the DRAM bandwidth. Although fewer configurations are limited by the L2 cache bandwidth, the thread block sizes with the lowest DRAM balance like \((32, 1, 32)\) are L2 cache bandwidth limited because of their flat shape. The L1 cache limitation comes into play only for thread block sizes with very small \(x\) dimensions.

For the LBM kernel, the performance model manages to correctly identify the worst-performing configurations with short \(x\) dimensions. Apart from that, it cannot distinguish the averagely performing from the well performing configurations. Just as with the stencil kernel, the fault is not with the estimated data volumes, but with the performance model, which does not capture the relevant mechanisms here. The LBM kernel, due to its streaming nature, is limited entirely by the DRAM bandwidth.

V. Conclusion and Outlook

We have demonstrated an automated performance modeling process for loop kernels on GPUs that is based on tracking data accesses via address expressions. Our method can estimate the data volumes transferred between the levels of the memory
hierarchy with high accuracy. Its versatility for a wide range of GPU programs has been demonstrated by evaluating it with two challenging and diverse kernel types, a long-range star stencil and a complex LBM kernel with a mix of access characteristics.

We have shown the usefulness of these data volumes to gain insight into the performance characteristics of a program and to classify different code generation configuration by their performance. However, our evaluation also showed that the simple performance model does not capture all the performance relevant mechanics and fails to differentiate between configurations at the top of the ranking. Identifying and modeling these mechanisms is an important topic for future work. Modeling Translation Lookaside Buffer (TLB) misses would be one of the candidates, where the relevant program metric would be TLB pages accessed by the current wave.

Another topic of future work is the testing and extension for different hardware architectures. The general hardware model with a local L1 cache and a shared L2 cache is applicable for all current GPU architectures, but details like cache line sizes and cache capacities have to be adapted. For example, AMD’s current CDNA architecture’s much smaller L1 cache would lead to many more capacity misses. On NVIDIA’s Ampere, the much larger L2 cache is split, which leads to traffic between the two halves.

We are also looking to verify the applicability of our method for more applications and more complex code transformations like temporal blocking. For temporal blocking and other complex stencil iteration schemes, our solution could be used to choose parameters like blocking factors and parallelization schemes.

REFERENCES

[1] M. Bauer, J. Hötzer, D. Ernst, J. Hammer, M. Seiz, H. Hierl, J. Hönig, H. Köstler, G. Wellein, B. Nestler, and U. Rüde, “Code generation for massively parallel phase-field simulations,” in Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis, ser. SC ’19. New York, NY, USA: Association for Computing Machinery, 2019. [Online]. Available: https://doi.org/10.1145/3295500.3356186.

[2] M. Bauer, H. Köstler, and U. Rüde, “Ilbmpy: Automatic code generation for efficient parallel lattice boltzmann methods,” 2020.

[3] M. Holzer, M. Bauer, H. Köstler, and U. Rüde, “Highly efficient lattice boltzmann multiphase simulations of immiscible fluids at high-density ratios on CPUs and GPUs through code generation,” The International Journal of High Performance Computing Applications, vol. 35, no. 4, pp. 413–427, 2021. [Online]. Available: https://doi.org/10.1177/10943420211016525.

[4] M. Jin, H. Fu, Z. Lv, and G. Yang, “Libra: An automated code generation and tuning framework for register-limited stencils on GPUs,” in Proceedings of the ACM International Conference on Computing Frontiers, ser. CF ’16. New York, NY, USA: Association for Computing Machinery, 2016, p. 92–99. [Online]. Available: https://doi.org/10.1145/2903150.2903158.

[5] K. Matsumura, H. R. Zohouri, M. Wald, T. Endo, and S. Matsuoka, “An5d: Automated stencil framework for high-degree temporal blocking on GPUs,” in Proceedings of the 18th ACM/IEEE International Symposium on Code Generation and Optimization, ser. CGO 2020. New York, NY, USA: Association for Computing Machinery, 2020, p. 199–211. [Online]. Available: https://doi.org/10.1145/3368826.3377904.

[6] T. Remmelg, B. Hagedorn, L. Li, M. Steuwer, S. Goriatch, and C. Dubach, “High-level hardware feature extraction for GPU performance prediction of stencils,” in Proceedings of the 13th Annual Workshop on General Purpose Processing Using Graphics Processing Unit, ser. GPGPU ’20. New York, NY, USA: Association for Computing Machinery, 2020, p. 21–30. [Online]. Available: https://doi.org/10.1145/3366428.3380760.

[7] L. Stolitzius, M. Emani, P-H. Lin, and C. Liao, “Data placement optimization in GPU memory hierarchy using predictive modeling,” in Proceedings of the Workshop on Memory Centric High Performance Computing, ser. MCHPC’18. New York, NY, USA: Association for Computing Machinery, 2018, p. 45–49. [Online]. Available: https://doi.org/10.1145/3286475.3286482.

[8] S. Williams, A. Waterman, and D. Patterson, “Roofline: an insightful visual performance model for multicore architectures,” Communications of the ACM, vol. 52, no. 4, pp. 65–76, 2009.

[9] C. Yang, T. Kurth, and S. Williams, “Hierarchical roofline analysis for GPUs: Accelerating performance optimization for the NERSC-9 perlmutter system,” Concurrency and Computation: Practice and Experience, vol. 32, no. 20, p. e5547, 2020.

[10] C. Nugteren, G-J. van den Braak, H. Corporea, and H. Bal, “A detailed GPU cache model based on reuse distance theory,” in 2014 IEEE 20th International Symposium on High Performance Computer Architecture (HPCA), 2014, pp. 37–48.

[11] H. Su, X. Cai, M. Wen, and C. Zhang, “An analytical GPU performance model for 3D stencil computations from the angle of data traffic,” The Journal of Supercomputing, vol. 71, pp. 2433–2453, 2015.

[12] D. A. Patterson and J. L. Hennessy, Computer Architecture: A Quantitative Approach. San Francisco, CA, USA: Morgan Kaufmann Publishers Inc., 1990.

[13] R. Sai, J. Mellor-Crummey, X. Meng, M. Araya-Polo, and J. Meng.
“Accelerating high-order stencils on GPUs,” in 2020 IEEE/ACM Performance Modeling, Benchmarking and Simulation of High Performance Computer Systems (PMBS), 2020, pp. 86–108.