Impact of different NBTI defect components on sub-threshold operation of high-k p-MOSFET

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Abstract. A study of the NBTI reliability of high-k p-MOSFET device for application in sub-threshold operation based on different defect mechanism is presented. The impact of the different defect mechanism is studied based on modelling the sub-threshold operation using Two-Stage NBTI model and NBTI-induced positive charges based on energy profiling approach. The time exponent of 0.1 is observed in sub-threshold operation modelled based on the Two-Stage NBTI model while time exponent of 0.3 is observed in sub-threshold operation modelled based energy profiling approach. Considerable threshold voltage shifts are observed during sub-threshold operation based on both defect mechanisms. Extraction of E’ centres and E’/Pb H Complex as well as positive charges was found to be temperature dependence hence the degradation is also thermally activated during subthreshold operation for both defect mechanisms.

1. Introduction

Operations in a transistor’s sub-threshold regime was critically essential for meeting a system’s stringent power desires in ultra low-power uses. However, seeing the aggressive downscaling of complementary metal-oxide-semiconductor (CMOS) transistors, stress-induced Negative Bias Temperature Instability (NBTI) has appeared as a reliability risk even in low-power systems. As a result of scaled oxide thickness in sub-nanometre regime devices, the increased electric field further enhanced the NBTI degradation effects. Many studies that used circuit-level simulation used the Reaction-Diffusion (R-D) model to investigate the effects of NBTI degradation on a circuit’s performance [1], [2]. However, as the oxide trapping/de-trapping effect mechanism affect device performance considerably [3], [4], [5] a device-level analysis of the effect of NBTI, which involved both oxide and interface traps under sub-threshold operation regime, is necessary. From the device-level perspective, operation in sub-threshold regime for Ultra – Effective Oxide Thickness, (UT-EOT) devices were contributed by the minority carrier and holes under the gate and diffuses due to the application of V_{DS}. However, different mechanisms occurred given the very thin EOT. Direct tunnelling of holes from substrate to bulk oxide will be trapped in the E’center defect precursor, which further degraded the device performance [6]. Previous study on sub-threshold effect due to NBTI was discussed based on hydrogen transport as the underlying mechanism [7]. Here, we present a study of the NBTI reliability of SiO₂/Hf (2/0.6 nm) with gate length of 32 nm under sub-threshold operation.
The modelling of NBTI-induced positive charges for degradation in sub-threshold operation is based on energy profiling approach. The subthreshold effects based on defect mechanism of interface trap and hole trapping effect with positive charges induced are presented.

2. Device and Simulation Conditions

2.1. Device process

The testbed PMOSFET devices with high-$k$/SiO$_2$ gate stacks simulated in this study were based on the foundry-standard 32-nm CMOS process. The fabrication process incorporated shallow trench isolation, deposition of high-$k$ dielectrics with metal gate, stress engineering using epi-SiGe pockets, silicidation, and dual-stress liner [8], [9]. The device fabrication process flow in this simulation is presented in figure 1. This simulation process, which is based on the gate-first scheme, was adopted to overcome the process-related problems (such as ultra-shallow junction formation), suppress the leakage current, and improve the on-and-off state drain current. Incorporating the laser annealing process can help to suppress transient-enhanced diffusion. To experimentally validate the testbed device, the electrical characteristics of IdVg obtained using this process flow was compared with experimental data in [9] and shown in figure 2. The main performance characteristics based on this study are compared in table 1. Given the information shown this table, it can be concluded that the process flow for the testbed devices used in this work was approximately within the range of the characteristics of the device fabricated by [9]. The validation of testbed device method is similar to other simulation work which confirms that the Id-Vg simulation results matched the experimental data [10]. This is to ensure that the impact of NBTI degradation in this study is realistically assessed.

- Shallow trench isolation formation
- Well implantation
- High-$k$ gate dielectric and metal gate deposition
- HALO implantation
- S/D extension
- SDE extension
- Sidewall spacer
- Two-step recess SiGe pocket
- Epitaxial SiGe growth
- HDD implantation
- Spike and laser annealing
- Nickel silicide
- Dual-stress liner deposition

Figure 1. The process flow of the simulated advanced-process 32 nm high-$k$ PMOS transistor [11]
Figure 2. Comparison Id-Vg characteristics between simulation and experimental data in [9]

|                     | This work (Lg = 32 nm) | (Lg = 24 nm) [9] |
|---------------------|------------------------|-----------------|
| Vdd (V)             | 1                      | 0.9             |
| Ion (A/um)          | $5.16 \times 10^{-4}$  | $5.25 \times 10^{-4}$ |
| Ioff (A/um)         | $2.22 \times 10^{-7}$  | $3.70 \times 10^{-7}$ |

2.2. Simulation conditions
For the 32 nm technology high-k metal gate devices, both drift diffusion and hydrodynamic models were used in the simulation which solved the Poisson equation and carrier continuity equations for 2D simulation involved in high-k devices. The drift diffusion model was activated for the entire region, while the hydrodynamic model was only activated in the silicon region. The models were used selectively according to the region to ensure the convergence in the simulation is achieved. In addition to that, the hydrodynamic transport was restricted to only one type of carrier for a particular device. This helps to increase the simulation speed that guaranteed the accuracy.

In this work, the hydrodynamic transport model is used due to the effects of carrier heating in the largely-varying electric fields can be accurately captured inside a sub-micron device subjected to the extreme conditions of NBTI stresses. The relatively simpler drift-diffusion simulation model neglects the carrier heating effect, hence more physically-accurate simulation results is yielded using the hydrodynamic transport model as shown in figure 3. The drift-diffusion model underestimated the NBTI-induced $\Delta V_{th}$ by as much as 12% where this underestimation appears to be rising with prolonged stress time [5].
2.3. NBTI Simulation

The threshold voltage degradation in this simulation was determined using the widely adopted on-the-fly (OTF) method [12]–[15]. Application of pre-stress voltage was needed in this model to equilibrate the occupancy of different states and thus ensuring that all states were not empty at the early phase of stress period [16].

The investigation, based on different defect mechanism is conducted using default Two-stage NBTI models and redefine the energy level using an energy profiling approach model. Table 2 shows the different energy level for each defects used in this work.

| Defect             | Two-stage NBTI model                             | Redefine energy model using energy profiling approach |
|--------------------|-------------------------------------------------|------------------------------------------------------|
| Pre-existing defect| Below valence band                               | Below valence band                                   |
| E’center           | $0 < E < 0.3$                                    | Within energy band gap                               |
| E/Pb H complex     | $0 < E < 0.5$                                    | Above energy band gap                                |

The energy profiling approach is based on the probing of energy distribution of positive charges in the gate dielectric [4]. The defects energy level as defined in a default model is redefined in order to have defect with characteristics based on positive charges. Hence, the pre-existing defect, E’center and E/Pb H Complex are the positive charges below, within and above energy band gap which known as grown hole traps (AHTs), cyclic positive charges (CPCs) and antineutralization positive charges (ANPCs) respectively based on [4]. The features of pre-existing defect, E’center and E/Pb H complex are similar to AHT, CPC and ANPC [4], [17], [18] hence the redefining of energy levels is important to accurately access the device degradation due to NBTI.
3. Results and Discussion

3.1. Simulation validation

To validate the simulation approach, figure 4 shows comparison between simulation result and experimental data in [4], [19]. The features of each charges contributed in the degradation was proven to be in agreement with the previous experimental works [4], [19]–[22]. The graph shows a simulation trend which agrees with the experiment for the region below Ev, within and above energy band gap.

![Graph showing simulation and experimental data comparison](image)

*Figure 4. Simulation of HfSiO$_2$/SiO$_2$ compared with experimental data of Hf-based devices*

The time exponent, n for redefine (new) and default (old) energy level varied significantly during the sub and super-threshold operations as observed in figure 5. The old energy level showed that the time exponent, n was around 0.1. However, the super-threshold voltage gave a different n. The n for new define energy level can be varied up to 0.3 as observed in most experimental works involving defects associated with DLHT or ANPC [23] which shown to be distributed closer or above E$_c$.

The total positive charges contributed in the degradation for new and default energy level is shown in figure 6. Significant differences can be seen in the new define energy level based on the applied stress temperature. Higher temperature gave more total positive charges contributed towards the degradation during sub and super-threshold operation regime for the new defines energy level. However, the default energy level showed no temperature effects upon the generated total positive charges.
3.2. Comparison of defect component characteristics

The behavior of defect components which contributed in the degradation for different stress voltages as shown in figure 7 (a) and (b) for E’centres or CPCs and E’/Pb H complex or ANPCs concentration respectively is compared. As observed in figure 7 (a), the sub-threshold operation voltage shows that the generation of CPCs was almost saturated, but slightly increased, approaching 10000s stress time while the super-threshold voltage shows the increasing of the CPCs generation when the stress time increased. In contrast, the E’centers concentration saturated and slightly reduced approaching 10000s stress time. The generation of E’centres concentration was smaller compared to CPCs for both sub and super-threshold voltage.

In figure 7 (b), first impression on the concentration of E’/Pb H complex and ANPCs increased as the stress time increased for both sub and super-threshold voltage. Closer observation indicated that
the generated of $E'/PbH$ complex and ANPCs during super-threshold operation regime increased throughout the stress duration. In contrast, the generated $E'/PbH$ complex and ANPCs during the sub-threshold operation regime only increased when the stress time was approaching above 1000s. Another closer observation indicated that the generated ANPCs was shown to be as compared to $E'/PbH$ complex.

![Figure 7. Defect components generated during NBTI stress for (a) E’ center and CPC (b) E’/Pb H Complex and ANPC](image)

Figure 8 (a) and (b) shows the CPC and ANPC complexes under different stress voltages and stress temperatures using new and default energy level respectively. As shown in figure 8 (a), the concentrations of generated CPC were higher than generated ANPC during the sub and super-threshold operation regime and under higher stress temperature. This is in agreement with previous experimental works which highlighted that the generated of positive charges were thermally activated [24]. Both components of positive charges were found to be temperature dependence. Therefore, the degradation during the sub-threshold operation regime was also thermally activated. This is not in agreement with [7] because the threshold voltage shift observed was not dependent on temperature.
during sub-threshold operation which is suspected due to the contributed defect mechanism studied based on interface trap.

For comparison, the plot of default energy level presented in figure 8 (b) gave different kinetics based on different stress temperatures for the sub and super-threshold operation regime. Above 1000s stress time duration, the E’center concentration was higher for the lower stress temperature during the super-threshold voltage. In contrast, for sub-threshold operation, similar generated E’center concentration was observed for both stress temperatures. Upon approaching the 1000s, the generated E’center concentration started to reduce more for higher stress temperature, hence during the 10000s stress duration, more generated E’ centers concentration was observed during smaller stress temperature. However, the generated E’/Pb H Complex concentration for both sub and super-threshold is stress time and temperature dependence. As the stress time and stress temperature increased, the generated E’/Pb H Complex concentration too increased.

3.3. Lifetime prediction
The lifetime of sub-threshold operation based on a hundred-year lifetime was estimated. The $\Delta V_{th}$ as a function of device lifetime which can be used in simulation study for circuit level degradation projection based on application-specific criterion [7] where it was readily understandable. Figure 9 (a) and (b) shows the level of device degradation in terms of $\Delta V_{th}$ as a function of device lifetime for new and default energy levels respectively for sub-threshold and super-threshold operation regime. The $\Delta V_{th}$ lines for each voltage were extrapolated to 10 and 100 years. The level of degradation in NBTI effect was assessed based on failure criterion $\Delta V_{t}= 30mV$ [7]. In the first impression for sub-threshold operation regime, based on the failure criterion target, the device can satisfy a hundred-year lifetime at sub-threshold operation voltage which was suitable for biomedical application which require extended device lifetime [7] for both new and old energy level. A closer observation as presented in figure 9 (c) shows that the threshold voltage shifted during the 10 and 100 years operation. For biomedical application devices, the sub-threshold operation regime which is for $V_g - V_{tho} = -0.2\,\text{V}$ and up to $V_g - V_{tho} = 0.2\,\text{V}$ meet the failure criterion target. The percentage difference for threshold voltage shift extracted based on new define and default energy level is shown in the figure. There was a significant difference in the prediction using default and new define energy level.

Conclusion
For sub-threshold operation, the time exponent observed for default and new define energy level was 0.1 and 0.3 respectively. The time exponent of 0.1 was referred to the pre-existing defect available in the device while the 0.3 was referred to the total generated defect contributed to the degradation consist of the CPC and ANPC which located near and above conduction energy level respectively. The degradation which characterized based on the redefines energy level found that the degradation was significant when stressed at higher temperature as compared to lower temperatures during the sub-threshold regime. However, the characterization using default energy level found that the degradation was not influenced by the stress temperature. More degradation was observed based on redefine energy level where the concentrations of generated CPC were higher than generated ANPC during sub and super-threshold operation regime and under higher stress temperature.
Figure 8. Plot of defect components during sub and super-threshold voltage under different stress temperatures for (a) Redefine energy levels (b) default energy level.
Figure 9. Power-law time dependence of extrapolated $\Delta V_{th}$ with respect to lifetime during sub and super-threshold operating regime for (a) New energy level (b) default energy level and (c) Estimation of $\Delta V_{th}$ after 10 and 100 years operation with the percentage different of estimation using new define and default energy level.
References

[1] W. Wang, S. Yang, S. Bhardwaj, S. Vrudhula, F. Liu, and Y. Cao, “The Impact of NBTI Effect on Combinational Circuit ;,” IEEE Trans. Very Large Scale Integr. Sytems, vol. 18, no. 2, pp. 173–183, 2010.

[2] J.-S. Yuan, W.-K. Yeh, S. Chen, and C.-W. Hsu, “NBTI reliability on high-k metal-gate SiGe transistor and circuit performances,” Microelectron. Reliab., vol. 51, no. 5, pp. 914–918, May 2011.

[3] D. S. Ang, Z. Q. Teo, T. J. J. Ho, and C. M. Ng, “Reassessing the Mechanisms of Negative-Bias Temperature Instability by Repetitive Stress / Relaxation Experiments,” IEEE Trans. Device Mater. Reliab., vol. 11, no. 1, pp. 19–34, 2011.

[4] S. W. M. Hatta, Z. Ji, J. F. Zhang, M. Duan, W. D. Zhang, N. Soin, B. Kaczer, S. De Gendt, and G. Groeseneken, “Energy Distribution of Positive Charges in Gate Dielectric: Probing Technique and Impacts of Different Defects,” IEEE Trans. Electron Devices, vol. 60, no. 5, pp. 1745–1753, May 2013.

[5] S. F. W. M. H. and Y. A. W. H. Hussin, N. Soin, M. F. Bukhori, “Effects of Gate Stack Structural and Process Defectivity on High-Dielectric Dependence of NBTI Reliability in 32 nm Technology Node PMOSFETs,” Sci. World J., vol. 2014, pp. 1–13, 2014.

[6] M. Cho, J.-D. Lee, M. Aoulaiache, B. Kaczer, P. Roussel, T. Kauerauf, R. Degraeve, J. Franco, L.-Å. Ragnarsson, and G. Groeseneken, “Insight Into N/PBTI Mechanisms in Sub-1-nm-EOT Devices,” IEEE Trans. Electron Devices, vol. 59, no. 8, pp. 2042–2048, Aug. 2012.

[7] J. Franco, S. Graziano, B. Kaczer, F. Crupi, L.-Å. Ragnarsson, T. Grasser, and G. Groeseneken, “BTI reliability of ultra-thin EOT MOSFETs for sub-threshold logic,” Microelectron. Reliab., vol. 52, no. 9–10, pp. 1932–1935, Sep. 2012.

[8] S. F. W. M. Hatta, N. Soin, D. A. Hadi, and J. F. Zhang, “NBTI degradation effect on advanced-process 45nm high-k PMOSFETs with geometric and process variations,” Microelectron. Reliab., vol. 50, no. 9–11, pp. 1283–1289, Sep. 2010.

[9] N. Yasutake, T. Ishida, K. Ohuchi, N. Aoki, N. Kusunoki, S. Mori, I. Mizushima, T. Morooka, K. Yahashi, S. Kawanaka, K. Ishimaru, and H. Ishiiuchi, “A High Performance pMOSFET with Two-step Recessed SiGe-S/D Structure for 32nm node and Beyond,” in Proceeding of the 36th European Solid-State Device Research Conference, 2006, pp. 77–80.

[10] M. F. Bukhori, “Simulation of Charge-Trapping in Nano-Scale MOSFETs in the Presence of Random-Dopants-Induced Variability,” 2011.

[11] “Sentaurus Technology Template : 32-nm Gate-First Flow and CMOS Processing.” TCAD Sentaurus Application Note, Version F-2011.09, 2011.

[12] S. Mahapatra and M. A. Alam, “Defect Generation in p-MOSFETs Under Negative-Bias Stress : An Experimental Perspective,” IEEE Trans. Device Mater. Reliab., vol. 8, no. 1, pp. 35–46, 2008.
[13] T. Yang and W. J. Liu, “Understand NBTI Mechanism by Developing Novel Measurement Techniques,” *IEEE Trans. Device Mater. Reliab.*, vol. 8, no. 1, pp. 62–71, Mar. 2008.

[14] V. D. Maheta, E. N. Kumar, S. Purawat, C. Olsen, K. Ahmed, and S. Mahapatra, “Development of an Ultrafast On-the-Fly IDLIN Technique to Study NBTI in Plasma and Thermal Oxynitride p-MOSFETs,” *IEEE Trans. Electron Devices*, vol. 55, no. 10, pp. 2614–2622, 2008.

[15] V. Huard, M. Denais, and C. Parthasarathy, “NBTI degradation: From physical mechanisms to modelling,” *Microelectron. Reliab.*, vol. 46, no. 1, pp. 1–23, Jan. 2006.

[16] S. Gupta, B. Jose, K. Joshi, A. Jain, M. A. Alam, and S. Mahapatra, “A Comprehensive and Critical Re-assement of 2-Stage Energy Level NBTI Model,” in *IEEE Int. Reliab. Phys. Symp*, 2012, pp. 1–6.

[17] T. Grassner, B. Kaczer, W. Goes, H. Reisinger, T. Aichinger, P. Hemenberger, P. Wagner, F. Sranovsky, J. Franco, M. T. Luque, and M. Nelliebel, “The Paradigm Shift in Understanding the Bias Temperature Instability: From Reaction – Diffusion to Switching Oxide Traps,” *IEEE Trans. Electron Devices*, pp. 1–15, 2011.

[18] J. F. Zhang, “Defects and instabilities in Hf-dielectric/SiON stacks (Invited Paper),” *Microelectron. Eng.*, vol. 86, no. 7–9, pp. 1883–1887, Jul. 2009.

[19] S. W. M. Hatta, Z. Ji, J. F. Zhang, W. D. Zhang, N. Soin, B. Kaczer, S. D. Gendt, and G. Groeseneken, “Energy distribution of positive charges in high-k dielectric,” *Microelectron. Reliab.*, vol. 54, no. 9–10, pp. 2329–2333, Aug. 2014.

[20] J. F. Zhang, “Defects and instabilities in Hf-dielectric/SiON stacks (Invited Paper),” *Microelectron. Eng.*, vol. 86, no. 7–9, pp. 1883–1887, Jul. 2009.

[21] J. F. Zhang, C. Z. Zhao, A. H. Chen, G. Groeseneken, and R. Degraeve, “Hole Traps in Silicon Dioxides — Part I: Properties,” *IEEE Trans. Electron Devices*, vol. 51, no. 8, pp. 1267–1273, 2004.

[22] C. Z. Zhao, J. F. Zhang, M. H. Chang, a. R. Peaker, S. Hall, G. Groeseneken, L. Pantisano, S. De Gendt, and M. Heyns, “Stress-Induced Positive Charge in Hf-Based Gate Dielectrics: Impact on Device Performance and a Framework for the Defect,” *IEEE Trans. Electron Devices*, vol. 55, no. 7, pp. 1647–1656, Jul. 2008.

[23] S. W. M. Hatta, “Probing Technique For Energy Distribution Positive Charges In Gate Dielectrics and Its Application to Lifetime Prediction. PhD. Thesis.,” LJMU/UM, 2013.

[24] A. A. Boo, D. S. Ang, Z. Q. Teo, and K. C. Leong, “Correlation Between Oxide Trap Generation and Negative-Bias Temperature Instability,” *IEEE Electron Device Lett.*, vol. 33, no. 4, pp. 486–488, Apr. 2012.