Design considerations for the semi-digital hadronic calorimeter (SDHCAL) for future leptonic colliders

A. Pingault on behalf of the CALICE-SDHCAL groups

Ghent University, Department of Physics and Astronomy,
Proeftuinstraat 86, B-9000 Gent, Belgium

E-mail: antoine.pingault@ugent.be

ABSTRACT: The first technological SDHCAL prototype having been successfully tested, a new phase of R&D, to validate completely the SDHCAL option for the International Linear Detector (ILD) project of the International Linear Collider (ILC), has started with the conception and the realisation of a new prototype. The new one is intended to host few but large active layers of the future SDHCAL. The new active layers, made of Glass Resistive Plate Chambers (GRPC) with sizes larger than $2 \text{m}^2$ will be equipped with a new version of the electronic readout, fulfilling the requirements of the future ILC detector. The new GRPC are conceived to improve the homogeneity with a new gas distribution scheme. Finally the mechanical structure will be achieved using the electron beam welding technique. The progress realised will be presented and future steps will be discussed.

KEYWORDS: Calorimeters; Detector design and construction technologies and materials; Gaseous detectors; Resistive-plate chambers

ArXiv ePrint: 1605.05075
1 Introduction

The CALICE-SDHCAL technological prototype has been successfully built and commissioned [1]. Its first published results [2] constitute a major step in the demonstration that highly-granular gaseous hadronic calorimeters are compatible with the requirements of the future ILC detectors in terms of efficiency, compactness and power consumption. A new prototype with fewer but larger layers and its dedicated mechanical structure, improved electronics and a new gas distribution system is in an advanced phase of development.

After a general description of the current SDHCAL prototype, the second section presents of the R&D status for the next prototype. It includes discussions on the improvements made to the gas system, the electronics and the acquisition boards, the new mechanical structure developed to support the new chambers and a few other challenges.

2 The CALICE-SDHCAL technological prototype

The SDHCAL prototype hosts 48 GRPC with a size of $1 \times 1$ m$^2$. Signals from the chambers are read out by 9216 pick-up pads of $1 \times 1$ cm$^2$ each, corresponding to more than 442000 channels in the complete prototype. All the electronics is directly embedded inside the stainless steel structure of the layer. The prototype can work in power pulsed mode and take data without an external trigger as required for the ILC. No cooling system is needed when running with a power pulsing cycle following the cycle from the ILC spill. For test beam purposes, where power pulsing is less efficient due to the spill cycle, a simple cooling system is used.
The prototype has been exposed to particle beams at CERN on several occasion during tests beam campaigns. Efficiencies exceeding 90% for the majority of the layers were obtained [2]. It also demonstrated, after calibration, a good energy resolution with a linear response (within ± 5%) over a large range of hadronic energies (5–80 GeV).

3 Towards larger prototypes

One of the geometry selected for the HCAL design of the ILD is the so-called Videau-geometry [3]. As can be seen on figure 1, the particularity of this design is the variable size of the different layers constituting a single module. Whereas the width of 94 cm is the same for every active layer, their length is ranging from a few tens of centimetres to about 2.94 m. For comparison, the largest RPCs in the CMS¹ experiment at CERN are made from Bakelite with a surface of about 2 m². The first SDHCAL prototype proved that layers up to 1 × 1 m² can be mass produced with good results, the next logical step is to demonstrate the same with chambers up to 3 × 1 m².

(a) Full detector with barrel and endcaps. (b) Single barrel module.

Figure 1. Sketches of a HCAL using the Videau design [3].

The foreseen goal for the next couple of years is to achieve the construction and commissioning of a prototype containing few (3 to 4) active layers of 2 × 1 m². Given the good results of the 1 × 1 × 1.3 m³ prototype, one objective will be to keep the overall construction process wherever possible, capitalising on the know-how and equipment available.

3.1 Gas distribution scheme

A proper homogeneity of the gas circulation inside the RPC volume is of the utmost importance to ensure high efficiency of detection and low noise. When designing the gas distribution system one has to keep in mind that a requirement for the ILD is to have all the servicing of the detector on one side.

The current set-up consists in a pair of inlet and outlet each at the opposite end of the servicing side. Inside the chamber along the frame following the inlet and outlet a small canal is perforated in several places to let the gas enter or exit the chamber. Simulation studies conducted on the gas circulation scheme showed that this arrangement will be less efficient for chambers bigger than

¹The Compact Muon Solenoid.
The current circulation system. The development of a new scheme shows improvement on the gas homogeneity (figure 2). In this new design, the outlet is moved to the middle of the servicing side and a second inlet is added in its place.

3.2 Electronics

The current electronics for each $1 \times 1 \text{ m}^2$ chamber consist of three Detector InterFace (DIF) boards each attached to a slab of two daisy-chained Active Sensor Unit (ASU). An ASU hosts a Printed Circuit Board (PCB) with its 24 embedded HARDROC2 [4] Application Specific Integrated Circuit (ASIC). Finally each ASIC can receive data from 64 channels. This adds up to 9216 channels connected to a matrix of $1 \times 1 \text{ cm}^2$ copper pads in charge of reading out the electric signal from the RPC. Larger prototypes will use a similar architecture with updated electronics. Consequently, the biggest active layers will have three times more channel. The following sections will present the improvements made to each part of this electronic.

3.2.1 Detector InterFace board

The DIF links the Data Acquisition (DAQ) system to the ASICs. It conveys the DAQ commands (slow control, clock, etc.) to the ASICs on one way and the read out data from the ASICs to the DAQ system on the other way. A block diagram representing the functionalities of the new DIF board is shown in figure 3.

The main goal here is to go from three to one board per layer. The new DIF will have to handle up to 432 HARDROC3 chips [4] for the biggest chamber instead of the 48 HARDROC2 chips currently. This will reduce consumption and simplify the cabling.

Other improvements on the functionalities were also done. Clocks signals are now sent through optical fibres using Timing, Trigger and Control signals (TTC) [5] instead of the HDMI interface. This is a much welcomed improvement as most of the synchronisation and cabling hassle on the current prototype is coming from these HDMI cables. Passing of the slow control commands is done via 12 Inter-integrated Circuit (I2C) buses instead of shift registers giving the ability to control ASICs independently. Two of the old shift registers buses were kept for backup and redundancy. Ethernet replaces USB2 protocol for data read out, increasing reliability and speed capability.
The discussion about the connection of the DIF to the ASU slab is still open. The board needs to be in a dedicated space outside the detection area and as small as possible to meet the compactness requirement of the ILD. The connector needs to be able to withstand a large number of signals (one for each ASIC) and high current on its power pin (up to 30 A). One foreseen solution to meet all the constraints would be to integrate directly the DIF into a longer PCB. This has not yet been implemented.

### 3.2.2 Active Sensor Unit

The ASU board is the main PCB hosting the read out electronics. Keeping the same design for $2 \times 1 \, \text{m}^2$ layers would effectively double the number of ASU to ASU connection. Given that each connection adds a weak point to the electronics, one will want to reduce them to the minimum achievable. To this purpose, boards with a longitudinal size of 100 cm have been produced to host 48 ASICs. This ensures a more viable design to scale to the biggest chamber.

### 3.2.3 Application Specific Integrated Circuit

OMEGA$^2$ and IPNLyon$^3$ developed a third generation of ROC chips. The new electronic will again use the HARDROC version which has been updated to comply with the ILD demands. The 64 channels have now current amplifier and are independent, allowing for zero suppression on chip. The dynamic range has been extended from 15 pC to 50 pC, giving the ability for higher thresholds acquisition. A triple voting I2C protocol replaces the shift registers to handle the slow control parameters. Providing individual control of each ASIC and a better radiation hardness. A fast clock generator is also integrated in the chip, simplifying synchronisation of data exchange between ASICs and the DIF board. Finally, the chip can also emulate the HARDROC2 version as a fall-back solution.

---

$^2$Laboratoire OMEGA — École Polytechnique, CNRS/IN2P3, Palaiseau, F-91128 France.

$^3$Univ. Lyon, Université Lyon 1, CNRS/IN2P3, IPNL 4 rue E Fermi 69622, Villeurbanne CEDEX, France.
A few hundred chips were produced and tested, 83.3% of them passed all the required tests, the majority of defect came from dead channels. Gain correction was successfully applied to effectively reduce the spread in the electronic response of the ASICs.

3.3 Mechanical structure

Given the size of the chambers in development, a new mechanical structure is under construction by CIEMAT,\(^4\) with the collaboration of CERN services, in order to host them. The current structure for the \(1 \times 1 \text{ m}^2\) prototype is assembled with lateral spacers and staggered bolts. In order to reduce deformation and lateral dimensions the Electron Beam Welding (EBW) technique is under investigation for the assembly. Results using these more robust and less deforming welding techniques are encouraging.

One of the requirements for the structure is a thickness tolerance under \(50 \mu\text{m}\) and a planarity under \(500 \mu\text{m}\). This was achieved for the \(1 \times 1 \text{ m}^2\) prototype but difficult, time consuming and expensive for longer length. The use of the roller levelling technique reduces these constraints while still accomplishing planarity of less than \(500 \mu\text{m}\) over \(3\) m long [6].

3.4 Other challenges

Another challenge not yet fully overcome is the construction of the cassette enclosing the chamber and its electronics. With the given design, the total thickness of a layer (including electronics and steel cassette) is \(11\) mm. Going to sizes of two to three meters may pose deformation issues capable of damaging the glass electrodes. One obvious solution would then be to increase the thickness of the cassette, therefore reducing the inter layer size of the mechanical structure to keep the same energy deposit in between each gas gap. Indeed, one idea behind the success of this detector lies in the fact that there is no absorber added to the structure between each layer: the structure itself, including the cassette, plays this role.

This would lead to a stiffer but heavier cassette and lighter but more fragile support. Knowing that a full \(1 \times 1 \text{ m}^2\) chamber with \(11\) mm thickness is already weighting more than \(70\) kg, going to \(3\) \(\text{m}^2\) chambers and augmenting the cassette thickness might pose handling issues.

The resistive coating is applied with the silk screen method using a liquid paint mix, then cured. This painting process should not pose trouble for bigger layer size but the curing step might as no production site is equipped with oven with the required dimensions. Other coating methodology are under study to overcome this problem.

To reduce both the running costs and the impact on the environment, a recirculating system of more than \(90\%\) of the gas is under development.

4 Conclusion

The efforts on the development of the next CALICE-SDHCAL technological prototype are under way. The first of these prototypes will host few but larger layers without deteriorating the efficiency thanks to a renewed gas system. Lots of improvements have been made on the read out electronics notably giving the ability to control each ASIC individually and extending the dynamic range.

\(^4\) CIEMAT, Centro de Investigaciones Energeticas, Medioambientales y Tecnologicas, Madrid, Spain.
The acquisition boards and the rest of the electronics have also been upgraded in order to keep up with the new features of the ASICs. The assembly of the mechanical structure with improved techniques is also in an advanced stage and is very encouraging. Construction and testing of this prototype is scheduled to be done by next year. All challenges are not yet fully overcome but results are promising thanks to a fruitful joint effort inside and outside the SDHCAL group of the CALICE collaboration.

Acknowledgments

This work is conducted thanks to a fruitful collaboration between team from CIEMAT (Madrid, Spain), CERN (Geneva, Switzerland), GWNU (Gangneung, South Korea), IPNL (Lyon, France), LPC (Clermont-Ferrand, France), NCEPU (Beijing, China), OMEGA (Orsay, France), UCL (Louvain, Belgium), UGent (Ghent, Belgium).

References

[1] G. Baulieu et al., Construction and commissioning of a technological prototype of a high-granularity semi-digital hadronic calorimeter, 2015 JINST 10 P10039 [arXiv:1506.05316].

[2] CALICE collaboration, V. Buridon et al., First results of the CALICE SDHCAL technological prototype, 2016 JINST 11 P04001 [arXiv:1602.02276].

[3] T. Behnke et al., The International Linear Collider Technical Design Report — Volume 4: Detectors, 2013.

[4] S. Callier, J.B. Cizel, F. Dulucq, C.d.L. Taille, G. Martin-Chassard and N. Seguin-Moreau, ROC chips for imaging calorimetry at the International Linear Collider, 2014 JINST 9 C02022.

[5] RD12 Project collaboration, B.G. Taylor, TTC distribution for LHC detectors, IEEE Trans. Nucl. Sci. 45 (1998) 821.

[6] CALICE collaboration, M.C. Fouz, Technological Semi-Digital Hadronic Calorimeter (SDHCAL) prototypes for future Lepton colliders, presented at the International Workshop on Future Linear Colliders (LCWS2015), Whistler, Canada, November 2015.