A design scheme for harmonic suppression network of high efficiency class-F power amplifier

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Abstract. This paper presents a design scheme of class-F PA harmonic suppression network. This scheme combines the advantages of lumped parameter elements and distributed parameter elements, and makes use of the characteristics of high Q value (quality factor), large adjustability of capacitance and high reusability of the microstrip line, so that the harmonic suppression network has the advantages of them. Based on the proposed scheme, a class-F PA with a frequency of 2.4GHz and a maximum PAE of 68.86% is designed, the output power of which can reach 17.5W (42.42dBm), so as to verify the feasibility of the proposed scheme. This scheme can improve the output power of UHF (300 ~ 3000MHz) class-F PA and reduce the difficulty of circuit design under the condition of high PAE.

1. Introduction
Class-F PA has the characteristics of low loss and high efficiency, so it is widely used in the high-efficiency energy transmission system in RF (Radio Frequency) and microwave frequency band. Ideally, a class-F PA needs to achieve a short circuit (low resistance) for even harmonics and an open circuit (high resistance) for odd harmonics at the drain end of PA [1], in which the harmonic impedance transformation is mainly affected by the harmonic suppression network. The harmonic control ability of the harmonic suppression network will directly affect the output efficiency of the class-F PA and the Q value (quality factor) of the whole circuit, and the simplicity of the harmonic suppression network will also affect the size of the whole circuit, so how to design the harmonic suppression network has become a key problem in the design of class-F PA.

Generally, when the UHF is 300 ~ 3000MHz, as shown in Fig1, lumped parameter elements or distributed parameter elements for circuit design are used in the traditional class-F PA harmonic suppression network. The harmonic suppression network designed by lumped parameter element is based on the principle of resonance. By setting the corresponding harmonic parallel resonance network to achieve high resistance, the purpose of harmonic suppression is achieved. Because of the large frequency change rate of lumped parameter elements and the wide variety thereof, it has the advantages of the high-quality factor, convenient debugging and great flexibility. However, when the number of harmonics needed to be used is large, the order of the harmonic suppression circuit will be higher; resulting in the circuit area becomes too large. When there are many inductors and capacitors, the parasitic parameters may have a great influence in practice, which may cause a variety of circuit errors and affect the overall performance of the circuit. The harmonic suppression circuit designed with distributed parameter elements uses the transmission line theory to change the impedance through
the electrical length of the microstrip line, so as to achieve the function of harmonic suppression. Because the same physical length of the microstrip line will present different electrical lengths for different times of harmonics, resulting in different impedance transformation effects, so it has the advantage of strong element reusability, which makes the circuit more concise. However, the frequency selection characteristics of distributed parameter elements are usually not as good as those of lumped parameter elements, so the circuit quality factor is low. Moreover, when a variety of harmonics are needed, the design of the circuit is difficult, and the debuggability of the microstrip line is poor in practice.

Fig1 Harmonic Suppression Network Based on Lumped and Distributed Parameter Elements

In order to solve the deficiency of harmonic suppression network designed by lumped parameter elements and distributed parameter elements, and considering the frequency effectiveness of lumped parameter elements, this paper proposes a hybrid design scheme of harmonic suppression network with lumped parameter elements and distributed parameter elements for the UHF of 300 ~ 3000MHz. By combining the advantages of the two traditional design methods, the proposed scheme makes the class-F PA circuit more concise, the circuit adjustability is enhanced, and the difficulty of circuit design is further reduced. This paper uses a class-F power amplifier working at 2.4GHz designed by the GaN HEMT of Cree Company as an example to illustrate the principle of the proposed scheme and verify the feasibility of the design scheme.

2. Materials and Methods

In order to discuss the scheme of harmonic suppression network using lumped parameter element and distributed parameter element proposed in this paper, this paper will take a class-F PA based on the proposed scheme and working at 2.4GHz as an example to illustrate the principle of this scheme. Fig2 shows the topology of the harmonic suppression network based on the proposed scheme.

First, in order to maximize the output power, according to the load traction, the impedance of Term1 is set as the optimal load impedance of traction, which is 18.433-j*7.076 Ohm. Then, in order to ensure that the matching network does not affect the harmonic impedance transformation of the harmonic suppression network, it is necessary to realize that the harmonic impedance presents low resistance (approaching 0 or 0) to the harmonic at point D relative to the ground. In this scheme, parallel capacitor $C_3$ is added, making the impedance of $C_3$ relative to the ground $Z_{C3}$ at point D is in parallel with $Z_{MK}$, if $C_3$ is large enough to make the nth harmonic impedance $Z_{C3n}$ small enough (near 0), then the parallel impedance $Z_{C3n}/Z_{MK}$ of $Z_{C3n}$ tends to $Z_{MK}$ zero, realizing that the harmonic impedance of the harmonic suppression network is almost unaffected by the matching network. Second, as we can see from Figure 2, according to the impedance transformation principle of Smith circle diagram, as long as the capacitance value of $C_3$ is large enough, the impedance $Z_{PI}/C_3$...
of Part 1 and $C_3$ will show a capacitive impedance relationship and be closer to the lower edge of Smith circle, when part1 parallels with $C_3$, which is large enough, it means that the fundamental impedance will change clockwise along the equal conductance circle and intersect with the equal Q value circle with a larger value, so that the Q value of matching network for fundamental impedance matching will be higher, and the purpose of improving the frequency selection characteristics of the circuit will be achieved, as shown in Fig3, the arrow represents the impedance change of parallel capacitor Change direction. According to the above analysis, the smaller $Z_{C_n}$ is, the smaller the influence of the matching network on harmonic impedance transformation of harmonic suppression network will be. According to the impedance expression of capacitance:

$$Z_C = \frac{1}{\omega C}$$  \hspace{1cm} (1)

It be known that $Z_{C_n}$ is one nth of the impedance $Z_{C_1}$ on the fundamental wave of $C_3$, so for $C_3$, the higher harmonic impedance is closer to 0 than the fundamental impedance. Furthermore, because $C_3$ is in parallel with the matching network, the influence of the matching network on the parallel impedance $Z_{C_{111}}$ is less than that of the fundamental wave. This also means that as long as the capacitance is within effective range, choosing the appropriate $C_3$ can realize that tends to 0; and $C_{31}$ does not completely tend to zero, so that $Z_{P_{11}/C_3}$ tends to zero, and $Z_{P_{11}/C_{31}}$ does not completely tend to zero. In practical engineering design, this is of great significance, because for the design of a matching circuit with impedance not close to 0, the difficulty is lower than that with an impedance approaching to 0. At the same time, according to the basic knowledge of the circuit, the signal will flow preferentially to the path with the smaller impedance. In order to ensure that the fundamental energy can be fed into the matching network without passing to the ground via $C_3$, it is needed to meet the condition that $Z_{C_3}$ is greater than $Z_{M_1}$. Obviously, it’s inevitable that $Z_{C_n}$ will be greater than $Z_{M_1}$; as shown in Fig2, $Z_{P_{11}}$ is parallel with $Z_{C_n}$. When the circuit matches, $Z_{P_{11}}$, $Z_{C_1}$ and $Z_{M_1}$ have the following relationship:

$$Z_{M_1} = Z_{P_{11}} // Z_{C_1}$$  \hspace{1cm} (2) 

yields:

$$Z_{M_1} < Z_{C_1}$$  \hspace{1cm} (3)

Finally, because the class-F PA designed in this paper considers the suppression of the 2nd, 3rd, 4th and 5th harmonics, it is necessary to realize the low resistance of the 2nd and 4th harmonics and the high resistance of the 3rd and 5th harmonics at point B in Fig2. First, the third harmonic suppression circuit is designed. Considering the layout of the actual space, it is set in this paper that $TL_1$ appears 120° electrical length relative to the fundamental wave (considered the actual microstrip line welding space), and $TL_1$ appears 360° electrical length relative to the third harmonic wave (that is, 2 times of 180° electrical length). Because the impedance of point C is 0, according to the formula:

$$Z_m(\theta = 180^\circ) = Z_L$$  \hspace{1cm} (4)

With the condition that $Z_L = Z_C = 0$, the impedance of the third harmonic relative to the ground at point A can be obtained as: $Z_{A3} = Z_m = 0$. Set $TL_3$ appear 30° electric length relative to the fundamental wave, $TL_2$ will appear 90° electric length relative to the third harmonic. According to the formula:

$$Z_{m2}(\theta = 90^\circ) = \frac{Z_0^2}{Z_L}$$  \hspace{1cm} (5)

With the condition that $Z_L = Z_{A3} = 0$, the impedance of the third harmonic relative to the ground at point B can be obtained as $Z_{B3} = \infty$, so the third harmonic can be suppressed at the input of the output network. And because of $Z_{A3} = 0$, it is equivalent to that the circuit composed of $TL_3$ and Part 2 connects with 0 resistance in parallel at point A, which means no matter the circuit composed of $TL_3$ and Part 2 changes, it will not affect $Z_{A3}$, in other words, it will not affect $Z_{B3}$. Second, in order to
design the second, fourth and fifth harmonic suppression circuit, this paper derives the electric length of $TL_1$, $TL_4$ and $TL_5$ relative to the fundamental wave backward according to the harmonic impedance value of the whole harmonic suppression circuit topology presented at point B, so as to determine the relationships between $TL_1$, $TL_4$ and $TL_5$ and $C_1$, $C_2$ and $C_3$. It is known that the impedance of harmonic relative to the ground at point D tends to 0, and $C_1$ is a DC blocking capacitor, so only $C_2$ has a great influence on the impedance value of the harmonic at point B relative to the ground. According to Fig2, the impedance expression of each harmonic at point B can be listed as follows:

$$Z_B(nf_0) = Z_{TL_k}(nf_0) + Z_{TL_k}(nf_0) \| Z_{TL_k}(nf_0) \| \left[ Z_{TL_k}(nf_0) + Z_{TL_k}(nf_0) + Z_{C_3}(nf_0) \right]$$  \hspace{1cm} (6)$$

where “n” is the harmonic order, whereupon, according to the impedance of each harmonic at point B, combined with the Formula (6), it can be deduced that:

$$Z_B(2f_0) = Z_{TL_2}(2f_0) + Z_{TL_2}(2f_0) \| Z_{TL_2}(2f_0) \| \left[ Z_{TL_2}(2f_0) + Z_{TL_2}(2f_0) + Z_{C_1}(2f_0) \right] = 0$$  \hspace{1cm} (7)$$

$$Z_B(4f_0) = Z_{TL_4}(4f_0) + Z_{TL_4}(4f_0) \| Z_{TL_4}(4f_0) \| \left[ Z_{TL_4}(4f_0) + Z_{TL_4}(4f_0) + Z_{C_2}(4f_0) \right] = 0$$  \hspace{1cm} (8)$$

$$Z_B(5f_0) = Z_{TL_5}(5f_0) + Z_{TL_5}(5f_0) \| Z_{TL_5}(5f_0) \| \left[ Z_{TL_5}(5f_0) + Z_{TL_5}(5f_0) + Z_{C_3}(5f_0) \right] = \infty$$  \hspace{1cm} (9)$$

There is also the impedance formula of the microstrip line:

$$Z_{TL_k}(nf_0) = jZ_{K0} \tan(n\theta)$$  \hspace{1cm} (10)$$

$$Z_{TL_k}(nf_0) = -jZ_{K0} \cot(n\theta)$$  \hspace{1cm} (11)$$

where $Z_{K0}$ is the characteristic impedance of the Kth transmission line, and its value can be determined by setting the width of the microstrip line according to the actual situation. Bring formula (10) and (11) into formulas (7), (8), and (9) and solving them simultaneously, the relationships between the electric lengths of $TL_1$, $TL_4$ and $TL_5$ relative to the fundamental wave and $C_2$ will be obtained. That is, if the value of $C_2$ is determined, the electric lengths of $TL_1$, $TL_4$ and $TL_5$ relative to the fundamental wave can be determined. Herein, we add $C_2$ is to improve the frequency selection characteristics of harmonic suppression network by using the characteristic that the Q value of capacitance is higher than that of the microstrip line.

To sum up, for the scheme proposed in this paper, it is only needed to determine the capacitance of $C_2$ and $C_3$ according to the actual situation, the whole harmonic suppression network can be designed. It can be seen that this scheme is very suitable for UHF (300 ~ 3000MHz) class-F PA with a high Q value. Because this scheme makes the design of harmonic suppression network more simple and flexible, this scheme has great engineering value for the design of class-F PA in practice.

![Fig3 Smith Admittance Chart](image)

3. Results & Discussion

In order to verify the feasibility of the scheme proposed in this paper, as shown in Fig4, an ideal harmonic suppression circuit composed of class-F PA is designed by using an ideal microstrip line, which works at 2.4GHz and suppresses the second, third, fourth and fifth harmonics. The results are shown in Fig5. It can be seen that the designed harmonic suppression circuit realizes the effect of a
short circuit to the second and fourth harmonics, and an open circuit to the third and fifth harmonics at the port. In port 2, the impedances of all the used harmonics are close to 0.

Fig4 Harmonic Suppression Circuit for Class-F PA at 2.4GHz (length/width: mm/mm)

In this paper, a class-F PA is designed with RO4350B board at 2.4GHz frequency. The dielectric constant of the board is 3.66. The thickness of the substrate is 0.762mm. The thickness of the copper sheet is 0.035mm. In order to improve the design accuracy, this paper transforms the ideal microstrip line model into the actual microstrip line model by using EDA tools and adds the input and output matching network and bias circuit. Finally, through optimization simulation, the general schematic diagram of class-F PA with actual microstrip line parameters of harmonic suppression circuit is obtained, as shown in Fig4. As shown in Fig7, with the situation that the input RF signal power is 28.5dBm, the simulation realizes the maximum additional efficiency of 70.07%, the output efficiency of 72.71%, the output power of 17.83W(42.511dBm), and the power ratios of the second, third, fourth and fifth harmonic power to the fundamental wave less than -47.675dBc. It can be seen that the simulation results show that the overall class-F PA circuit has high harmonic suppression.

Fig5 Port Impedance Information of Harmonic Suppression Circuit for Class-F PA at 2.4GHz

In this paper, according to the simulation board diagram, the actual processing of PCB is carried out, as shown in Fig8. As shown in Fig7, when the output power of the drive stage is 28.6dBm, the maximum PAE of the designed class-F PA is 68.86% and the output power is 17.5W(42.42dBm), the power ratio of the third harmonic to the fundamental is -30.8dBc, the power ratio of the second, fourth and fifth harmonic to the fundamental is less than -48.2dBc, and the output end of PA has 40.1dB attenuation. Comparing Fig6 with Fig7, it is found that the additional efficiency of the power amplifier in the actual debugging is lower than that in the simulation, which may be due to the lower suppression of the third harmonic than that in the simulation. The output power is lower than that of the simulation, which is caused by the actual lumped parameter element loss and the possible
mismatch. To sum up, it can be seen that the harmonic suppression circuit proposed in this paper improves the frequency selection characteristics of class-F PA, and achieves high harmonic suppression and high power output under high efficiency.

![Fig7 Spectrum of Actual Class-F PA](image)

![Fig8 Class-F PA after Actual Debugging](image)

In order to further illustrate the advantages of class-F PA based on the scheme proposed in this paper, we compare the results in this field through Table1 with that of class-F PA. It can be found from Table1 that the class-F PA designed in this paper has advantages in the comprehensive index, and it achieves high power output and high PAE.

| Table1 Comparison of characteristics |
|--------------------------------------|
| Ref | Frequency (GHz) | Peak PAE% | Output Power | Class of PA |
|-----|-----------------|-----------|--------------|-------------|
| [2] | 5.8             | 66%       | 15dBm        | F           |
| [3] | 2.4             | 70.9%     | 40.8dBm      | F           |
| [4] | 0.9             | 70%       | 30dBm        | F           |
| This work | 2.4       | 68.86%    | 42.42dBm     | F           |

4. Conclusions
This paper is a research on UHF (300 ~ 3000MHz) class-F PA harmonic suppression network. It aims to provide a design scheme with high practicability, which can improve the circuit Q value and make the harmonic suppression circuit design faster and more efficient. By combining the advantages of the harmonic suppression circuit designed by lumped parameter elements and distributed parameter elements, a new design scheme of mixed-use of lumped parameter elements and distributed parameter elements is proposed. Based on the proposed scheme, a class-F PA operating at 2.4GHz frequency is designed, and the output power reaches 17.5W (42.42dBm) when the maximum PAE is 68.86%.

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