Power Quality Improvement Using an Active Power Sharing Scheme in More Electric Aircraft

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Abstract—This article proposed a harmonic suppression scheme that used a dc-dc converter as an active harmonic injector to cancel voltage harmonics on the HVdc bus within a hybrid power generation centre (HPGC). A permanent magnet synchronous generator and a battery are considered to supply power to a common HVdc bus through their dedicated ac-dc and dc-dc converters respectively within the HPGC. We proposed simplified mathematical models of harmonics from the ac-dc and dc-dc converters. Thereafter, an active power sharing scheme between the PMSG and the battery is developed to control the magnitudes of targeted harmonics to be the same. The targeted harmonics on the HVdc bus can thus be cancelled by properly tuning the carrier signal phase angles within ac-dc and dc-dc converters. A closed-loop control scheme has been developed and this scheme is with no extra hardware cost. To demonstrate the effectiveness of the proposed scheme, we selected the first-band harmonic \( (f_c - 3f_0) \) as the targeted harmonic component. The harmonic cancellation scheme for this component has been developed and validated using experimental results. It has been demonstrated that the proposed method can achieve over 90% reduction of this specific harmonic component on the HVdc bus within this HPGC using one dc-dc converter.

Index Terms—Capacitors, dc power generation, harmonics, power sharing ratio.

I. INTRODUCTION

TO ACHIEVE more efficient and environmentally friendly solutions of travel, more electric aircraft (MEA) concept is one of the major trends towards future aerospace development [1], [2]. Onboard MEA, pneumatic, hydraulic, and mechanical subsystems are replaced by their electrical equivalences, which results in a significant increase in power demand. To supply electrical loads onboard, the common dc bus architecture has received significant attention these days [3], [4]. With the common dc bus architecture, electrical generators are supplying a dc bus through an ac-dc converter together with energy storage elements. As shown in Fig. 1, the dc bus is supplied by an electrical generator and a high-voltage battery through their dedicated converters. A permanent magnet synchronous generator (PMSG) is used to extract electrical power from the high-speed engine shaft. An energy storage system (ESS) with a battery is integrated for the flexible operation of power flow. These two power sources, together with a high-voltage bus capacitor, form a hybrid power generation centre (HPGC), as shown in Fig. 1.

With such a structure, expected benefits include less need for cables, high flexibility of power management, and higher redundancy ability under fault conditions. The hybrid dc power generation system has been widely considered not only for the MEA but also for hybrid vehicle [5], ships [6], and microgrid [7].

In the HPGC system shown in Fig. 1, the capacitor bank is used to filter out high-frequency fluctuated currents and flatten the dc-bus voltage, such that the dc-bus voltage meets the DO-160E [8] and MIL-STD-704F [9] standard. However, the capacitor is always bulky and expensive. With reduced harmonics, reduced size and weight of the dc-bus capacitor can be achieved. This, in return, gives the system a higher efficiency, reduced mass and lower fuel consumption. Furthermore, with lower harmonics, the capacitor lifetime is extended as well [10].
Active suppression methods have attracted more attention to suppressing harmonics on capacitors due to their flexibility and high performance. The fundamental idea of those methods is to adjust the switching actions of power converters to minimize the harmonics.

Adding an extra circuit is the most straightforward solution for reducing capacitor harmonics generated from switching frequencies [12]–[15]. This kind of methods can be implemented on all systems with power electronic devices. However, it requires extra elements and thus increases the cost and complexity of systems.

Some researchers have investigated harmonic suppression in the second switching frequency for the dc power system [16], [17]. However, the first-band harmonics are not considered, which contributes more to dc-link fluctuation when the PMSG works under high modulation index [18]. In [19], the authors proposed a dynamic pulse width modulation (PWM) interleaving method to suppress the first-band harmonic. However, as a side effect of this method, the ac harmonic current of PMSG deteriorates, which limits its application on MEA.

In this article, we proposed a new power-sharing control scheme to achieve power sharing (between PMSG and the battery) and harmonic suppression at the same time. Through active power sharing, magnitudes of harmonic components from the ac-dc and dc-dc converters can be actively controlled. Controlling targeted harmonic components ($f_c - 3f_0$ component studied in this article) from the ac-dc and dc-dc converters of the same magnitudes, appropriate phase shifting between those harmonic components will enable the harmonic suppression and cancellation.

This article is a follow-on research of our previous publication [16], where harmonics of two ac/dc power converters have been actively controlled with one ac-dc converter used as a harmonic sink. In this article, we focus on using the dc-dc converter as an active harmonic damping device to suppress the first carrier sideband harmonic ($f_c - 3f_0$ frequency harmonic component from one ac-dc converter). Although we select some specific harmonic components for suppression, the proposed method can essentially be used to suppress any harmonic component of interest by simply changing the feed-back component.

The article is organized in the following manner. Sections II and III present basic mathematical analysis of switching harmonics generated from the ac-dc and dc-dc converters, respectively. Based on the mathematical models, Section IV illustrates an enhance harmonic suppression method by adjusting power sharing between PMSG and ESS system and actively tuning the phase-shift angle of the carrier signals. Section V gives the experiment results of the proposed method. Section VI concludes this article.

II. MATHEMATICAL MODEL FOR DC-BUS CURRENT HARMONICS ON A TWO-LEVEL CONVERTER UNDER THE SINUSOIDAL PWM (SPWM) OPERATION

In the system shown in Fig. 1, the PMSG supplies electrical power to an HVdc bus through an ac-dc converter, with details shown in Fig. 2(a). To develop a harmonic cancellation scheme for the HVdc bus, it is essential to derive the mathematical model of its harmonics before the capacitor. In this study, a standard two-level ac-dc converter is considered for ac-dc conversion because it is known as the most used rectifier for PMSG based power generation system. It is assumed that the common asymmetrical regular sampling PWM is implemented in the ac-dc converter, as shown in Fig. 2(b). Due to the converter switching actions, dc-link current $i_{dc}$ will be with harmonics as shown in Fig. 2(c) with its spectrum. It can be noticed that significant components of the current harmonics are observed in $f_c \pm 3f_0$ and $2f_c$. Here, $f_c$ is the switching frequency, $f_0$ is the fundamental frequency from PMSG. Harmonics in higher frequencies are not considered because of their lower impact on the dc-bus.

In our recent publication [16], the $2f_c$ harmonic component has been studied in detail. In this section, we will focus on the development of the mathematical models of ($f_c \pm 3f_0$) harmonics.

A. Mathematical Analysis of DC-Bus Harmonic Based on Double-Fourier Method

The double Fourier method is commonly used to study the harmonics of PWM operation [18]. Some analysis has been investigated in [16], which will be briefly reviewed here.

Assuming the current on the ac side is ideally sinusoidal for a two-level converter, ac side currents can be written as

$$i_{ac}^{[k]}(t) = I_{ac}\cos\left(2\pi f_0 t + \beta + \frac{2k\pi}{3}\right)$$

where $I_{ac}$ is the amplitude of the fundamental component of ac current, $f_0$ is the fundamental frequency, $\beta$ is the angle between phase current and its ac side voltage, $k = 0, 1$ and 2 represent phase A, B, and C, respectively.
Assuming the positive current on dc bus \(i_{dc}\) is from the converter to the dc-link capacitor, as shown in Fig. 2(a). Its switching function for each phase leg can be expressed as

\[
sf^{[k]}(t) = K_{0,1} \cos \left(2\pi f_0 t + \beta + \alpha + \frac{2k\pi}{3}\right) + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} K_{m,n} \cos \left[m \left(2\pi f_c t + \theta_c^{[k]}\right) + n \left(2\pi f_0 t + \beta + \alpha + \frac{2k\pi}{3}\right)\right]
\]

(2)

where \(f_c\) is the switching frequency, \(\theta_c^{[k]}\) is the phase angle of the triangular carrier signal for each leg, \(\alpha\) is the phase angle between ac fundamental current and ac-side converter voltage (i.e., power factor angle), \(K_{m,n}\) is the harmonic amplitude using the Bessel function of the first kind. Based on double Fourier analysis \([18]\), \(K_{m,n}\) can be expressed as

\[
K_{m,n} = \frac{1}{q_{m,n}} J_n(q_{m,n} M) \sin \left[(m + n) \frac{\pi}{2}\right]
\]

(3)

where

\[
q_{m,n} = \left(m + n \frac{f_0}{f_c}\right) \frac{\pi}{2}
\]

(4)

In (3), \(J_n()\) is the Bessel function of the first kind. \(m\) and \(n\) are orders of switching harmonic and its sidebands respectively. For instance, when \(m = 1\) and \(n = 3\), \(K_{m,n}\) means the magnitude of harmonic with a frequency of \(f_c + 3f_0\). Using (1)–(4), the dc-bus harmonic currents generated from one phase leg can be derived as

\[
i_{dc}^{[k]}(t) = i_{ac}^{[k]}(t) \cdot sf^{[k]}(t)
\]

\[
= \frac{I_{ac}}{2} K_{0,1} \left[\cos \left(4\pi f_0 t + 2\beta + \alpha + \frac{4k\pi}{3}\right) + \cos \beta\right] + \frac{I_{ac}}{2} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} K_{m,n} \left\{\cos \left[2\pi (m f_c + (n + 1) f_0) t + \sigma_{m,n}^{[k]}\right]\right. + \left.\cos \left[2\pi (m f_c + (n - 1) f_0) t + \varphi_{m,n}^{[k]}\right]\right\}
\]

(5)

where \(\sigma_{m,n}^{[k]}\) and \(\varphi_{m,n}^{[k]}\) are phase angles of each component, which are

\[
\sigma_{m,n}^{[k]} = m \theta_c^{[k]} + (n + 1) \left(\beta + \frac{2k\pi}{3}\right) + n\alpha
\]

(6)

\[
\varphi_{m,n}^{[k]} = m \theta_c^{[k]} + (n - 1) \left(\beta + \frac{2k\pi}{3}\right) + n\alpha.
\]

(7)

Extracted from (5), the dc-link current harmonics in a specific frequency \((f_c + jf_0)\) should be expressed as a sum of components from three legs as

\[
i_{dc,i,j}^{[g]}(t) = \frac{I_{ac}}{2} K_{i,j-1} \sum_{k=0}^{2} \cos \left[2\pi (i f_c + j f_0) t + \sigma_{i,j-1}^{[k]}\right]
\]

\[
+ \frac{I_{ac}}{2} K_{i,j+1} \sum_{k=0}^{2} \cos \left[2\pi (i f_c + j f_0) t + \varphi_{i,j+1}^{[k]}\right]
\]

(8)

where \(i\) and \(j\) mean switching and band side orders of dc-bus current harmonics. For instance, substituting \(i = 1\) and \(j = 3\) into (8) gives the expression of harmonic in the frequency of \(f_c + 3f_0\). Here, we use a superscript \([g]\) indicating this harmonic is associated with the generator connected to the ac-dc converter and is to differentiate it from the dc-dc converter harmonic, which will be discussed in the later sections.

### B. Harmonics on \(i_{dc} \pm 3f_0\)

As shown in Fig. 2(c), significant harmonics appear in the frequencies of both \(f_c - 3f_0\) and \(f_c + 3f_0\). Furthermore, along the whole spectrum, their magnitude cannot be ignored.

This subsection will analyse the harmonic in \(f_c - 3f_0\) first. Considering no phase shift on carrier signals among the three legs, i.e., \(\theta_c^{[1]} = \theta_c^{[2]} = \theta_c^{[3]} = \theta_c\), substituting \(i = 1\) and \(j = -3\) into (8) gives

\[
i_{dc,1,-3}^{[g]}(t) = \frac{3I_{ac}}{2} K_{1,-4} \cos \left[2\pi (f_c - 3f_0) t + \sigma_{1,-4}\right]
\]

\[
+ \frac{3I_{ac}}{2} K_{1,-2} \cos \left[2\pi (f_c - 3f_0) t + \varphi_{1,-2}\right].
\]

(9)

For the coefficient \(K_{1,-4}\) and \(K_{1,-2}\), we have

\[
K_{1,-4} = \frac{2}{(1 - 4f_0/f_c)} J_4 \left(\frac{\pi}{2} \left(1 - 4f_0/f_c\right) M\right)
\]

(10)

\[
K_{1,-2} = -\frac{2}{(1 - 2f_0/f_c)} J_2 \left(\frac{\pi}{2} \left(1 - 2f_0/f_c\right) M\right).
\]

(11)

Assuming that \(f_c >> f_0\) (in typical cases, \(f_c\) is at least 20 times the frequency of \(f_0\)), the term \(f_0/f_c\) can be neglected as it is approximately equal to 0. Then, (9) can be approximated as expressed in (12)

\[
i_{dc,1,-3}^{[g]}(t) \approx \frac{3I_{ac}}{\pi} J_4 \left(\frac{\pi}{2} M\right) \cos \left[2\pi (f_c - 3f_0) t + \sigma_{1,-4}\right]
\]

\[
- \frac{3I_{ac}}{\pi} J_2 \left(\frac{\pi}{2} M\right) \cos \left[2\pi (f_c - 3f_0) t + \varphi_{1,-2}\right].
\]

(12)

Comparing the two terms in (12), their magnitudes have different Bessel functions and are given in (13)

\[
\frac{3I_{ac}}{\pi} J_4 \left(\frac{\pi}{2} M\right) \text{ and } -\frac{3I_{ac}}{\pi} J_2 \left(\frac{\pi}{2} M\right).
\]

(13)

In (13), modulation index \(M\) is always less than 1, because of the limited output voltage of the ac-dc converter. Comparison between the two Bessel function terms when \(M < 1\) is shown in Fig. 3. It can be seen that \(J_4(\pi M/2)\) is almost zero, and \(J_2(\pi M/2)\) is more than 20 times the magnitude of \(J_4(\pi M/2)\).
where voltage, achieved from voltages and currents in modulation index.

Fig. 3. Comparison between $J_d(\pi M/2)$ and $J_q(\pi M/2)$ with increased modulation index.

Hence, the first term is neglectable in (12). Therefore, the expression in (12) becomes as in (14)

$$i_{dc,1,3}^{[q]} (t) \approx \frac{3I_{ac}}{\pi} J_2 \left(\frac{\pi}{2} M\right) \cos \left[2\pi (f_c - 3f_0) t + \varphi_{1,2} + \pi\right].$$

(14)

With (14), its magnitude is convenient for a controller to calculate. There, $M$ will be a fixed value if PMSG works under flux-weakening operation (which is a normal case for aerospace application). $I_{ac}$ is measured by current sensors which is given as

$$I_{ac} = \sqrt{I_{d}^2 + I_{q}^2}$$

(15)

where $i_d$ and $i_q$ are the $d$- and $q$-axes currents of the PMSG. Apart from magnitude, the phase angle of the component in (14) can be derived from (7) which gives the expression as

$$\varphi_{1,2} + \pi = \theta_c - 2(\alpha + \beta) - \beta + \pi$$

(16)

where $\beta$ is the angle between phase current and its ac side voltage, $\alpha$ is the power factor angle. Both of them can be achieved from voltages and currents in $dq$-frame, which are

$$\alpha + \beta = \text{atan2} (v_q, v_d)$$

(17)

$$\beta = \text{atan2} (i_q, i_d).$$

(18)

Here, the function $\text{atan2}(y, x)$ gives the angle of complex value $(x + iy)$. Therefore, the magnitude ($I_{dc,1,3}^{[q]}$) and phase angle ($\theta_{dc,1,3}^{[q]}$) of the harmonic in $f_c - 3f_0$ can be summarized from (14) to (18) as

$$I_{dc,1,3}^{[q]} \approx \frac{3\sqrt{I_d^2 + I_q^2}}{\pi} J_2 \left(\frac{\pi}{2} M\right)$$

(19)

$$\theta_{dc,1,3}^{[q]} \approx \theta_c - 2\text{atan2} (v_q, v_d) - \text{atan2} (i_q, i_d) + \pi.$$  

(20)

Following the same process, the magnitude and phase angle of the harmonic in $f_c + 3f_0$ can be calculated and simplified as

$$I_{dc,1,3}^{[q]} \approx \frac{3\sqrt{I_d^2 + I_q^2}}{\pi} J_2 \left(\frac{\pi}{2} M\right)$$

(21)

$$\theta_{dc,1,3}^{[q]} \approx \theta_c + 2\text{atan2} (v_q, v_d) + \text{atan2} (i_q, i_d) + \pi.$$  

(22)

From (19) and (21), it is important to notice that the simplified magnitudes of these two components of frequencies $f_c - 3f_0$ and $f_c + 3f_0$ are essentially the same. A comparison between the simplified magnitudes and original models is given in Fig. 4(a). The error is always less than 3 A, which is less than 10% of the original model. Meanwhile, the phase angle between the simplified model and the original model is also neglectable (less than 0.05 rad), as shown in Fig. 4(b). Therefore, the simplified model can be adopted and used for the harmonic suppression method.

From Fig. 4, it is important to note that the simplified magnitudes of the $f_c - 3f_0$ and the $f_c + 3f_0$ components will have the same increment when more power is generated from the PMSG. This is a useful finding for harmonic suppression and will be discussed in Section IV.

III. HARMONIC ANALYSIS OF A DC-DC CONVERTER

This section will discuss harmonic generated from a typical buck-boost dc-dc converter. As shown in Fig. 5, the bidirectional buck-boost dc-dc converter consists of two power switches (S1 and S2) with antiparallel diodes and a filtering inductor $L_d$. The port on the left is connected to a battery with a voltage $V_b$, and the port on the right is connected to a dc-bus with voltage $V_{dc}$. This dc-dc converter allows the battery to work under both charging and discharging modes.

Within the hybrid electric power generation centre, a secondary level supervision unit is used to provide the reference power (thus defines inductor current $I_L$) to the dc-dc converter local control. When $I_L > 0$, the current flow from the battery to

![Fig. 4. Comparison between the simplified and original models on $I_c$ - $3f_0$ and $I_c + 3f_0$. a) Magnitudes. b) Phase angles.](attachment:fig4.png)
the dc-link. The dc-dc converter operates under boost mode and the battery is in the discharging mode. On the contrary, when $i_L < 0$, the dc-dc converter operates under buck mode and the battery is in discharging mode.

Typical PWM generation diagrams of the dc-dc converter are shown in Fig. 6(a) and (b) (battery in discharging and charging mode). PWM signals are generated to control switches S1 and S2. The switching behaviour of these switches causes the dc-link current ripples. In Fig. 6, the switching signals are generated by comparing the duty cycle reference and carrier signal with a triangle waveform. The period of a carrier signal is defined as $T^{[b]}$. The average of the dc current $i_{dc}^{[b]}$ and its contained harmonics is dependent on the power reference (and thus $i_L$).

Similar to ac-dc converters, the $i_{dc}^{[b]}$ harmonics phase angle can be controlled by shifting the phase angle of the carrier signal. Similar to ac-dc converters, harmonics in switching frequencies are difficult to measure. Hence, their mathematical modeling is critical for harmonic suppression of the dc-link capacitor.

To simplify the analysis, the inductor current is assumed to be constant as $I_L$, and the converter works under continuous current mode. Then, the current in one cycle flowing into the dc-bus capacitor, $i_{dc}^{[b]}$, is given as

$$i_{dc}^{[b]} = \begin{cases} I_L, & 0 < t < \frac{(1-D)T^{[b]}}{2} \\ 0, & \frac{(1-D)T^{[b]}}{2} < t < \frac{(1+D)T^{[b]}}{2} \\ I_L, & \frac{(1+D)T^{[b]}}{2} < t < T^{[b]} \end{cases}.$$  

Fig. 5. Bidirectional buck-boost converter.

Considering the symmetry and using Fourier expansion, the current $i_{dc}^{[b]}$ can be expressed as

$$i_{dc}^{[b]} = I_0^{[b]} + \sum_{k=1}^{\infty} I_k^{[b]} \cos \left( 2k\pi f_c^{[b]} t + k\theta_c^{[b]} \right)$$  

where

$$f_c^{[b]} = \frac{1}{T^{[b]}}.$$  

From (24), it can be seen that the phase angle of current $i_{dc}^{[b]}$ harmonics are related to the carrier signal phase angle $\theta_c^{[b]}$. The Fourier coefficients in (24) are derived as

$$I_0^{[b]} = I_L \left( 1 - D \right)$$  

$$I_k^{[b]} = \int_{0}^{T^{[b]}} i_{dc}^{[b]}(t) \cos \left( 2k\pi f_c^{[b]} t \right) dt = \frac{2I_L}{k\pi} \sin \left( k\pi D \right).$$  

This article focuses on suppressing the first-order harmonic on dc-link capacitors. Substitute $k = 1$ into (24) and (27), the harmonic in $f_c^{[b]}$, which is $i_{dc,1}^{[b]}$, can be expressed as

$$i_{dc,1}^{[b]} = I_1^{[b]} \cos \left( 2\pi f_c^{[b]} t + \theta_c^{[b]} \right)$$  

where

$$I_1^{[b]} = \frac{2I_L}{\pi} \sin \left( \pi D \right).$$  

Fig. 6. Conventional PWM strategy of the dc-dc converter. a) Boost (discharging) mode. b) Buck (charging) mode.

From (29), it can be observed that the magnitudes of harmonic components $I_{dc,1}^{[b]}$ is proportional to the inductor current $I_L$. There, when $I_L > 0$, the battery operates under the discharging mode. When $I_L < 0$, the battery operates under the charging mode. With a higher output/input power, $I_{dc,1}^{[b]}$ will be with a
higher absolute value. From (28), it can be seen that the phase angle of this harmonic is related to the carrier signal phase angle \( \theta_{dc}^{[b]} \). By adjusting \( I_L \) and \( \theta_{dc}^{[b]} \), active controls of magnitude and phase angle of current \( I_{dc}^{[b]} \) can be achieved. The harmonic frequency \( f_c^{[b]} \) can further be set to be the same as that of the targeted harmonic component on the HVdc bus. Thus, the dc-dc converter can potentially be used to cancel some specific harmonics on the dc bus as discussed in the following section.

IV. CAPACITOR HARMONIC MINIMIZATION METHOD

A. Proposed Method

The hybrid generation centre with more details is shown in Fig. 7. Within such a system, a PMSG supplies power to an HVdc bus through an ac-dc converter. A high-voltage battery supplies power to the HVDC bus (270 V) via a dc-dc converter. Both converters share the dc-link capacitor. The ac-dc converter and the dc-dc converter are controlled with their local primary controller.

A system controller is used for high-level supervision (secondary) control. The system-level control is to define power sharing between PMSG and the battery by defining their power references \( (i_{dc}^{[b]} \) and \( i_{L}^{*} \)). The local controllers thus control converters of the PMSG and the battery individually. This way the voltage regulation can be achieved.

This article focuses on harmonic suppression in the frequency of \( f_c - 3f_0 \). In Fig. 7, two converters will inject required DC currents on this frequency to the HVdc bus.

The local control diagram of PMSG is shown in Fig. 8. A cascaded control structure has been used, with the current control being the inner loop. A flux-weakening control is applied in the outer control loop. This is due to the fact that in MEA applications, PMSG is driven by the high-speed shaft of an aircraft engine. The stator output voltage \( \sqrt{v_d^2 + v_q^2} \) is controlled by injecting a negative flux current component \( i_d \). The output current \( i_{dc} \) of the ac-dc converter is also controlled with its reference \( i_{dc}^{[b]} \) given by the system-level controller. With measured currents \( i_d \), \( i_q \), voltage references \( v_d \) and \( v_q \) modulation index \( M \), the information of harmonic component \( f_c - 3f_0 \) can be derived, with its magnitude \( I_{dc1,-3}^{[b]} \) and its phase angle \( \theta_{dc1,-3}^{[b]} \) from (19) and (20). The fundamental frequency \( f_0 \) can be obtained from a machine speed sensor. These features of the \( f_c - 3f_0 \) component, i.e., magnitude, frequency, and phase angle are then sent to the controller of the dc-dc converter and the system controller.

The cancellation scheme of the harmonic component of \( f_c - 3f_0 \) from the ac-dc converter is essentially based on the fact that two sinusoidal currents of the same magnitude will cancel each other if they are 180° phase shift to each other. With this fact, we can use the dc-dc converter as an active harmonic injection source to cancel the \( f_c - 3f_0 \) harmonic component from the ac-dc converter. This approach has the advantage of not requiring extra hardware to the system since the dc-dc converter is an integral part of the HPGC. To achieve that, the frequency of the carrier signal \( f_c^{[b]} \) of the dc-dc converter should be set to \( f_c - 3f_0 \) i.e.

\[
f_c^{[b]} = f_c - 3f_0.
\]

To achieve the phase angle difference of 180° between the two harmonics, the phase angle of the PWM carrier signal should be adjusted according to (20) and the battery’s working status (discharging or charging). When the battery operates under discharging mode \( (I_L > 0) \), both the \( f_c - 3f_0 \) harmonic magnitudes of the ac-dc and dc-dc converters \( I_{dc1,-3}^{[b]} \) and \( I_{dc1}^{[b]} \) are positive, which can be derived from (19) and (29). With (20), the phase angle of the dc-dc converter’s PWM carrier signal should be set as

\[
\theta_c^{[b]} = \theta_{dc1,-3}^{[b]} - \pi = \theta_c - 2\arctan2 (v_q, v_d) - \arctan2 (i_q, i_d).
\]

Then, a phase angle difference of 180° between two harmonics can be achieved. On the contrary, when the battery operates under the charging mode \( (I_L < 0) \), \( I_{dc1}^{[b]} \) becomes negative, and thus the phase angle of the PWM carrier signal should be
set as
\[
\theta_c = \theta_{dc,1,-3} = \theta_c - 2\tan^{-1}(v_q/v_d) - \tan^{-1}(i_q/i_d) + \pi
\]
(32)
where \(\theta_{dc}^{[b]}\) is the phase angle of the carrier signal of the dc-dc converter.

Therefore, the carrier signal frequency \((f_c^{[b]})\) and the phase angle \((\theta_c^{[b]})\) can be selected based on the harmonic information sent from the PMSG controller. The control diagram of the dc-dc converter is shown in Fig. 9. The magnitude of the \(f_c^{[b]}\) harmonic from the dc-dc converter \(I_{dc,1}^{[b]}\) is also calculated using (29). This will be used in the system controller in the next discussion.

The control scheme of the dc-dc controller only gives a 180° phase difference between components generated from the ac-dc and dc-dc converters. To fully suppress the harmonic on the dc-link capacitor, the magnitudes of the two components need to be adjusted to the same value. Such an adjustment is achieved in the system controller, as shown in Fig. 10.

In the harmonic control block of Fig. 10, magnitudes of two components \(I_{dc,1,3}^{[g]}\) and \(I_{dc,1}^{[b]}\) are controlled to be the same by a PI controller. If \(I_{dc,1}^{[b]}\) is lower than \(I_{dc,1,3}^{[g]}\), the proportional integral (PI) controller will give a higher \(I_{dc,1}^{[b]}\) to increase \(I_{dc,1}^{[b]}\). Here, the absolute value of the magnitudes is taken to make the control feasible under either the discharging or charging mode of the battery.

Meanwhile, another PI controller gives the total DC current reference \(i_{dc}^{[g]}\) to control the dc link voltage \(V_{dc}\). Then the reference of PMSG output current is also achieved from \(i_{dc}^{[g]}\) and \(i_t^{[g]}\) according to the discharging/charging mode of the battery.

In power management of the power generation system, the state of charge (SOC) of the battery is one of the major concerns. Generally, the SOC of a battery should be within a required range. The battery should be discharged when the SOC is over the upper limit and be charged when the SOC is under the lower limit. In Fig. 10, the system controller also integrates a SOC controller to determine the discharging/charging mode of the battery. The drawback of this concept is that the charging and discharging speeds of the battery are limited by the harmonic suppression effect. This issue is a tradeoff and can be further studied in the future.

In a system without a centralized controller, the voltage control block and harmonic control block can be distributed into the local controllers of the PMSG and the battery. A similar harmonic suppression effect can be achieved. However, this is not what this article focuses on, and will not be discussed in detail.

**B. Discussion on the \(f_c + 3f_0\) Harmonic Component**

As discussed in previous sections, the proposed method is with two actions: adjusting the switching frequency of the dc-dc converter and adjusting the power sharing ratio to control \(I_{dc,1}^{[b]}\) to be the same as \(I_{dc,1,3}^{[g]}\). With the first action, the proposed method should eliminate the components on dc-link currents in both the frequencies of \(f_c\) and \(f_c - 3f_0\). This shows the superiority of the proposed control method when comparing to the conventional control. However, for the second action, although the magnitude of the \(f_c - 3f_0\) component is suppressed to zero, the \(f_c + 3f_0\) component (from the ac-dc converter) varies when changing the output power of the PMSG. Hence, this section will discuss the sum value of the first-band harmonics on the dc-link current.

When the \(f_c - 3f_0\) components from the ac-dc and dc-dc converters counteracted each other with a 180° phase difference, the total harmonic in the first switching band \((I_{dc,1,totall})\) can be expressed using the simplified harmonic models in Section II.

\[
I_{dc,1,totall} = I_{dc,1,-3} + I_{dc,1,3}
= I_{dc,1}^{[g]} - I_{dc,1}^{[b]} + I_{dc,1}^{[g]}
\]

(33)
where \(I_{dc,1}^{[g]}\) is the simplified magnitude of the \(f_c - 3f_0\) and \(f_c + 3f_0\) components from the ac-dc converter (discussed in Section II-B), \(I_{dc,1}^{[b]}\) is the magnitude of the \(f_c - 3f_0\) component from the dc-dc converter when its switching frequency is adjusted to \(f_c - 3f_0\). In (33), term \(I_{dc,1}^{[g]} - I_{dc,1}^{[b]}\) is the absolute harmonic on the dc-link current in the frequency of \(f_c - 3f_0\) (from the ac-dc and the dc-dc converters together) and the term \(I_{dc,1}^{[g]}\) is the harmonic in \(f_c + 3f_0\) (from the ac-dc converter only). Considering the value of \(I_{dc,1}^{[b]}\) and \(I_{dc,1}^{[g]}\), (33) can be
TABLE I

| Category       | Parameters                  | Values          |
|----------------|----------------------------|-----------------|
| PMSG parameters| Rotor speed                 | 20kRPM          |
|                | Switching frequency         | 32kHz           |
|                | Maximum modulation index    | 0.9             |
| Battery        | Voltage                     | 200V            |
|                | Inductance                  | 500μH           |
|                | Switching frequency         | 32kHz or 29kHz  |
| DC-link        | Capacitance                 | 400μF           |
|                | Load power                  | 40kW and 60kW   |

rewritten as

\[
I_{dc,1,\text{total}} = \begin{cases} 
I_{[b]}^{[b]} & I_{dc,1}^{[g]} 
\leq I_{dc,1}^{[b]} \\
2I_{dc,1}^{[g]} - I_{dc,1}^{[b]} & I_{dc,1}^{[g]} > I_{dc,1}^{[b]} 
\end{cases} 
\tag{34}
\]

When \(I_{dc,1}^{[b]} \leq I_{dc,1}^{[b]}\), and the dc-dc converter operates under the boost mode, if we increase the power of the battery and thus the power of the PMSG is decreased, then the total first band harmonics will be increased because total harmonic in this case \(I_{dc,1}^{[b]}\), as shown in (34)] will increase because of the increase of the battery power.

On contrary, when \(I_{dc,1}^{[b]} > I_{dc,1}^{[b]}\), if we decrease the battery power and thus PMSG power will be increased. Then, \(I_{dc,1}^{[b]}\) will increase and \(I_{dc,1}^{[b]}\) will decrease. The total power \(2I_{dc,1}^{[g]}-I_{dc,1}^{[b]}\), as shown in (34)] will also increase because of an increased term \(2I_{dc,1}^{[g]}\) minus a reduced term \(I_{dc,1}^{[b]}\) gives a higher value.

Hence the total harmonic is at its lowest level when \(I_{dc,1}^{[s]} = I_{dc,1}^{[b]}\). This proves that the proposed power sharing adjustment gives the best operation point for suppressing the total first band switching harmonics. When the battery operates under the buck mode, the harmonic is more complicated. However, with a proper phase-shift between the two converters, both the harmonics in \(f_c\) and \(f_c - 3f_0\) can be suppressed. Maybe it is not the best operation point (\(f_c + 3f_0\) could be higher), but the harmonic suppression is still effective compared to the conventional control.

V. SIMULATION AND EXPERIMENT STUDY

A. Simulation Study

To evaluate the performance of the proposed harmonic model and cancellation method, a simulation is implemented on MATLAB/Simulink and PLECS. It includes a PMSG, an ac-dc converter, a battery, a dc-dc converter, capacitors and the load. Some basic control parameters are given in Table I. In the simulation, the PMSG is the one developed in [20]. As the simulation time elapses, the simulation is divided into three cases, as shown in Table II.

The simulation results are shown in Fig. 11. Before the time 10 ms, the output power of the system is 40 kW and no harmonic suppression algorithm is applied. The power sharing ratio between the PMSG and the battery is set as 1:1. The ac-dc converter and the dc-dc converter share the same carrier signal. For the dc-link currents in this case \((i_{dc}^{[s]}, i_{dc}^{[b]}, i_{\text{cap}})\), the PMSG generates significant components in frequencies of \(f_c \pm 3f_0\) and 2\(f_c\), while the battery generates significant components in \(f_c\) and 2\(f_c\). These components are summed up on the capacitor current \(i_{\text{cap}}\). Hence there are significant components shown on \(i_{\text{cap}}\) in the frequencies of \(f_c \pm 3f_0\) and 2\(f_c\), as shown in the spectrum of Case 1.

Then, the proposed harmonic suppression scheme is applied at 10 ms, the switching frequency of the dc-dc converter should be adjusted as \(f_c \pm 3f_0\) (29kHz in this case). The inductor current of the dc-dc converter is also adjusted from 100 to 90.3 A to fully suppress the \(f_c - 3f_0\) harmonic on the dc-link. In the zoom-in view, the current variations are reflected on the magnitude of pulses on \(i_{dc}^{[b]}\) and \(i_{\text{cap}}^{[b]}\) and \(i_{dc}^{[b]}\), which are increased because of higher output power of the dc-link. In the zoom-in view, the current variations are reflected on the magnitude of pulses on \(i_{dc}^{[b]}\) and \(i_{\text{cap}}^{[b]}\) and \(i_{dc}^{[b]}\), which are increased because of higher output power of the ac-dc converter. However, the \(f_c - 3f_0\) harmonic on the dc-link is still suppressed to 2.38 A. Compared to the \(f_c + 3f_0\) component (48.31 A), which was not suppressed, the reduction is about 95.1%. Therefore, the simulation validates the dynamic performance of the proposed method.

B. Experiment Study

To validate the proposed harmonic cancellation scheme, an experimental rig has been set up as shown in Fig. 12. To simplify
test rig setup, PMSG is represented by a programmable ac source together with three-phase inductors. A phase-locked loop (PLL) is implemented in the controller to achieve phase angle of fundamental ac voltages. The battery is represented by a dc power supply which is connected to the dc-dc converter. Since the harmonic cancellation scheme is related to ac-dc and dc-dc converter, using a three-phase ac source and a dc power supply to represent the PMSG and battery respectively will not affect the effectiveness of the proposed harmonics cancellation scheme. The dc source is used to represent the battery with a constant voltage output of 200 V. The system is controlled using TI DSP TMS320F28379D. The parameters of the experiment are shown in Table III. The total output power of the ac-dc converter and dc-dc converter is 2 kW. The ac fundamental frequency is 50 Hz. The switching frequency of the ac-dc converter, $f_c$, is set at 4 kHz. For the proposed suppression method, the carrier signal frequency for the dc-dc converter is set to be $f_c - 3f_0$, i.e., 3.85 kHz. This frequency is a little lower than that in the case with no optimization. Therefore, this makes the following comparison reasonable.

Compared to the conventional control, the proposed method needs some extra computations, i.e., harmonic estimation from the ac-dc and dc-dc converters (in Figs. 7 and 8) and harmonic suppression control (in Fig. 10). The total computation time of these actions is 11.7 $\mu$s. In the experiment, these actions are implemented every 10 ms (dc-link current control loop). Therefore, the computation intensity of the proposed method is not a problem for the system.

![Fig. 12. Experiment setup.](image)

Fig. 13 shows the DC-bus currents from the ac-dc converter and dc-dc converter ($i_{\text{dc}}^{[a]}$ and $i_{\text{dc}}^{[b]}$). The current flowing into the capacitor $i_{\text{cap}}$ and its spectrum are also shown in Fig. 13. In Fig. 13(a), the output power of the ac-dc and dc-dc converters are the same, i.e., $P^{[a]} = 1$ kW, $P^{[b]} = 1$ kW. Two converters use the same carrier signal. Then, results with the proposed method are shown in Fig. 13(b). In Fig. 13(b), the power sharing is adjusted between two converters.

With the proposed method, the switching frequency of the dc-dc converter should be adjusted as $f_c - 3f_0$ (3.85 kHz in this case). Thus, the switching cycle of the dc-dc converter is changed from 250 to 259 $\mu$s, as shown in the zoom-in views of Fig. 13(a) and (b). From these views, the inductor current of the dc-dc converter is also adjusted from 5.2 to 4.6 A to fully suppress the $f_c - 3f_0$ harmonic on the dc-link. In zoom-in views, the current variations are reflected on the magnitude of pulses on $i_{\text{dc}}^{[b]}$. In Fig. 13(b), $i_{\text{dc}}^{[a]}$ and $i_{\text{dc}}^{[b]}$ tend to counteract each other, and thus a suppressed $f_c - 3f_0$ harmonic on $i_{\text{cap}}$ can be achieved.

Comparing the two results in Fig. 13 and considering the current spectrums on the dc-link, the harmonic in $f_c - 3f_0$ is suppressed from 1.63 to 0.09 A (94.5% reduction). In $f_c$, there is a component with 2.06 A in the conventional case [Fig. 13(a)], but no component shown when the proposed method is applied [Fig. 13(b)]. This is because the switching frequency of the dc-dc converter is modified from $f_c$ to $f_c - 3f_0$. It is also interesting to note the change of the second-order harmonics of $i_{\text{cap}}$. There are two components on such a band because of the change in the switching frequency of the dc-dc converter.

| Category      | Parameters                  | Values                  |
|---------------|-----------------------------|-------------------------|
| DC-link       | DC link capacitance         | 4.4 mF                  |
|               | DC bus voltage              | 270V                    |
|               | Output power                | 2 kW                    |
| AC-DC         | Phase inductance            | 1 mH                    |
|               | Frequencies of AC side $f_a$| 50 Hz                   |
|               | Voltages of AC side $V_a$   | 250 V                   |
|               | Switching frequency $f_c$   | 4 kHz                   |
|               | Modulation index $m$        | 0.90                    |
|               | $i_{\text{dc}}^{[b]}$ control loop frequency | 100Hz                   |
| DC-DC         | Inductance                 | 30 mH                   |
|               | Carrier frequency $f_c^{[a]}$ | 4 kHz (no optimization) |
|               | Carrier frequency $f_c^{[b]}$ | 3.85 kHz (in proposed method) |

**TABLE III**

**EXPERIMENT PARAMETERS**
The dc power generation system suffers dynamic load change in the MEA. For the proposed method, the power sharing ratio should also be adjusted when such a dynamic change happens, as shown in Fig. 14(a). The DC load changes from 2 to 3 kW, and it results in a dc-link voltage drop and recovery. The power sharing ratio changes according to the new working status. The dc-link current reference of the ac-dc converter ($i_{dc}[g]^*$) changes from 4.5 to 8.0 A and the dc-link current reference of the dc-dc converter ($i_{dc}[b]^*$) changes from 3.4 to 3.9 A. With the proper power sharing and phase shift angle, a suppression of $i_{cap}$ can be achieved when the output power is 3 kW, as shown in Fig. 14(b). Comparing to Fig. 13(b), the magnitudes of $i_{cap}$ components in $f_c + 3f_0$, $2f_c$ are increased because of higher output power of the ac-dc converter. However, the $f_c - 3f_0$ harmonic on the dc-link is still suppressed to almost zero (0.06 A), which validates the effectiveness of the proposed method under different output power.

Considering the SoC management of the battery, the dc-dc converter may work under buck-mode (charging mode for the battery). In this case, the proposed method can still work effectively, as shown in Fig. 15. The output power of the system is 1 kW. The inductor current of the dc-dc converter is adjusted to $-4.8$ A in this case. The pulses on $i_{dc}[b]^*$ becomes negative, and it counteracts with $i_{dc}[g]^*$. Then, the $f - 3f_0$ harmonic on the dc-link is suppressed to almost zero (0.06 A).

VI. CONCLUSION

This article proposed a dc-link harmonic suppression scheme within a dc power generation system which used a cooperation control between the ac-dc and dc-dc converters. The switching frequency of the dc-dc converter is set according to the fundamental frequency of the ac-dc converter. Then, using a simplified harmonic model and adjusting the power sharing ratio between the ac-dc and dc-dc converters, the targeted harmonic component (in our example case $f - 3f_0$) has been suppressed significantly. The proposed method was feasible when the battery operates under
either discharging or charging modes. There was a tradeoff between harmonic suppression and the charging/discharging speed of the battery. The effectiveness of the proposed method was validated by the experimental results. Furthermore, the extra computation burden of the proposed method is very low, and the dc power generation system does not need extra hardware. Thus, the proposed method was convenient to implement and can preserve the simple control.

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