A simple and controlled single electron transistor based on doping modulation in silicon nanowires

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A simple and highly reproducible single electron transistor (SET) has been fabricated using gated silicon nanowires. The structure is a metal-oxide-semiconductor field-effect transistor made on silicon-on-insulator thin films. The channel of the transistor is the Coulomb island at low temperature. Two silicon nitride spacers deposited on each side of the gate create a modulation of doping along the nanowire that creates tunnel barriers. Such barriers are fixed and controlled, like in metallic SETs. The period of the Coulomb oscillations is set by the gate capacitance of the transistor and therefore controlled by lithography. The source and drain capacitances have also been characterized. This design could be used to build more complex SET devices.

The first and most common Coulomb blockade device is the Single Electron Transistor (SET) made with metallic leads and island, and tunnel oxide barriers. It is used as sensitive electrometers or electron pumps allowing to control the transfer of electrons one by one. Since then very important efforts have been devoted to fabricate silicon SETs, mostly to integrate SETs together with regular transistors for building logic circuits, and more recently for quantum logic experiments with single charge or spin in silicon quantum dots. An important challenge is to increase the temperature of operation from the typical sub-kelvin range of original devices up to much higher temperatures. The required size of the island is of the order of the nm, and therefore out of control of current fabrication processes. Researchers took advantage of natural disorder to create such extremely small islands, mostly with constrictions in disordered thin films. More recently undulated thin films have been used, as well as pattern-dependent oxidation.

We followed another approach based on etched silicon nanowires without constrictions, as pioneered by Tilke et al. and more recently Namatsu et al., and also Kim et al. and Fujiwara et al. In the two first cases the formation of a Coulomb island in a nanowire underneath a very large gate was studied. In the two others two gates were defined above a nanowire, each of them acting as a tunable barrier for entering/exiting the single electron box delimited by these gates. Although this scheme allowed logic operations to be performed at 300K, it remains a complex architecture since up to 4 gates are needed for proper operation. Our SET is much simpler since it requires a single gate to define the quantum dot, while the barriers are fixed, like in metallic SETs. Periodic Coulomb blockade is observed, with a period solely determined by the surface area of a single gate. It is therefore controlled by lithography, not by disorder. With current state of the art electron beam lithography the limit in operating temperature is of the order of 10 K. The schematics of our device is essentially similar to the original metallic SETs, the tunnel oxide barriers being replaced by low-doped regions under spacers producing a doping modulation along the wire, while the electrostatic gate capacitor is replaced by the MOS gate of the transistor (see Fig. 1d). We first used single electron charging effects in silicon nanocrystals embedded within a gate oxide stack to fabricate few-electron memories. Interestingly the use of doping modulation along a nanowire has already been used in grown devices, where the control of dopants is easier than ion implantation in very thin films.

The design is a silicon on insulator (SOI) thin film transistor fabricated on a 200 nm CMOS platform. First a SOI film is thinned down to approximately 17 nm, then 200 nm long nanowires are defined by e-beam lithography and wet etching (see Fig. 1). The width is as small as 30 nm for the presented devices. A first low doping
FIG. 2: Linear drain-source conductance versus gate voltage in a W=40 nm, L=30 nm device with $t_{ox}=10$ nm, at various temperatures. Very small drain-source voltages are necessary at low temperature to stay in the linear regime: $V_{ds}$ is 500 µV at 300 K, 100 µV at 110 K and 4.2 K and 80 µV at 1 K. Inset: zoom on periodic Coulomb oscillations in linear scale.

of the whole nanowire and access is performed at this stage. A SiO$_2$/Poly-Si gate stack is then defined perpendicularly to the wire, with a length as small as 30 nm. Doping modulation is achieved by using the gate as a mask for subsequent ion implantation. In previous designs we only used this gate and doped the nanowire moderately. In a second one we added 50 nm long silicon nitride spacers on both side of the gate and heavily doped all the uncovered regions. This scheme gives much more regular oscillations and lower background charge noise and is the one presented here. The high doping of the uncovered wire creates low resistance contacts, and the MOSFET gate allows to accumulate electrons in the channel created under the gate. In between these regions (i.e. under the spacers) are the low doped ‘access region’ acting as tunnel barriers on both sides of the channel (see Fig. 1). We already observed Coulomb blockade in non-overlapped MOSFETs. The $I_d-V_g$ characteristics are shown in Fig. 2 at various temperature. The FET characteristics at 300 K is replaced at lower temperature by very periodic and perfectly reproducible oscillations, with a contrast increasing as the temperature decreases (see Fig. 3). The period $\Delta V_g = e/C_g$ is an extremely sensitive, in-situ measurement of the gate capacitance: capacitances smaller than 10 aF are easily measured, with very small signals. We checked that the Coulomb island is the channel of the FET transistor by comparing the measured period with the calculated MOS gate capacitance. The results are shown in the inset of Fig. 3 for samples with various geometries and three gate oxide thicknesses: $t_{ox} = 4, 10$ and 24 nm. As expected the measured period scales with the surface area of the channel and the gate oxide. We believe the observed dispersion is mostly due to approximations in the simple calculation we used for a capacitor with metallic electrodes. More accurate estimations should include one semiconducting electrode, but nevertheless estimating the spatial extent of the quantum dot below the spacers remains a challenge.

Although it is well known theoretically and demonstrated experimentally that Coulomb blockade occurs with resistive access, it is difficult in this case to predict the source and drain capacitances ($C_s$ and $C_d$), and hence the charging energy. Here the barriers do not rely on 1D constrictions or impurities, instead the wire is low doped, on the insulating side of the metal-insulator transition at 0K, providing enough resistance for confinement. We calculated the doping profile and potential along the wire at 300 K (see Fig. 3). The doping drops abruptly below the spacers and gate, inducing a flattop potential barrier.
at zero gate voltage. Increasing this voltage creates a well that pushes back down the potential in the center of the low doped region. This potential well is responsible for single electron effects at low temperature. If the resistance of this region is below a threshold value (typically of the order of 100 kΩ at large gate voltage (see Fig. 2). Beyond the resistance we have characterized the source and drain capacitances by measurements in the non-linear regime. We observed very stable Coulomb diamond features, as shown in the upper panel of Fig. 4. The slope of the rhombuses is a direct measurement of $C_s$ and $C_d$ as we already know the gate capacitance. For the data shown in Fig. 4 we found $C_g \approx 13.6 \pm 0.3 \text{aF}$ from the peak spacing and $C_s \approx 42 \text{aF}$ and $C_d \approx 32 \text{aF}$ from the Coulomb diamonds slopes. A major issue and a limitation in SET devices comes from switching background charges inducing a large 1/f noise and changing the phase of the Coulomb oscillations. We observe very low noise in our devices: once at cryogenic temperatures the phase of the oscillations is stable within measurement uncertainties, as long as large gate voltage sweeps (larger than 1 volt) are not performed. The few anomalies we observe are attributed to charge traps with sufficiently fast dynamics to not increase the noise within the bandwidth of our measurement.

In conclusion, we have shown that a precise control of doping along etched silicon nanowires allows to make a very simple, reliable and predictable single-gate SET. The period is entirely set by the transistor gate capacitance, i.e. by lithography. Furthermore we have characterized the source and drain capacitances arising from the low doped regions under gate spacers. We believe this basic device will be useful to realize more complex circuits fully compatible with CMOS technology.

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