A Design of High Power Beidou L-Band Power Amplifier

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Abstract. According to the optimization problem of power amplifier output power, linearity and other performance indicators, this paper proposes an improved three-level cascade overall design framework, designed by the load traction method, source traction method and power back-off method for the driver stage and final stage power. The amplifier better improves the output power and linearity of the system and the high-gain pre-stage power amplifier is designed by the small-signal S-parameter method. After the performance analysis, simulation design, physical production and testing of the cascaded power amplifier, the output power of the system is 15W. This paper implements high power, high gain, high linearity power amplifier design, and applies this result to BeiDou Navigation Satellite System (BDS).

1. Introduction
BDS is an important national space infrastructure that China has built and operated independently to meet the needs of the development of science and technology in the new era, and can provide all-weather, all-weather, high-precision positioning, navigation and timing services for global users. In order to better promote the development of Beidou satellite navigation system in marine fishery, agriculture, forestry and animal husbandry, transportation and other fields, Beidou satellite navigation system has developed short message communication function based on radio measurement service [1, 2, 3, 4].

As an important part of satellite communication system, the power amplifier mainly plays a significant role of signal power amplification in the system. At present, many domestic manufacturers are committed to the research of the power amplifier of Beidou satellite navigation system. However, the application of the power amplifier in Beidou communication terminal is limited by the low output power and poor linearity. For instance, [5] proposed a kind of high-power amplifier whose output power is only 5W. Due to its poor performance, the test success rate of the communication terminal is relatively low. In this paper, the three-stage cascade power amplifier structure is employed to improve the output power of the system, and the linearity of the system is optimized by the power fallback method to further reduce the cross-modulation distortion and interference.
2. System design

2.1. System analysis
The output power of the power amplifier proposed in this paper is 15 W (41.76 dBm), and the input signal is a BPSK signal with a power of 0 dBm output from the RF chip. Therefore, the power gain of the power amplifier needs to reach 41.76 dB to meet the requirements. As can be seen in Fig. 1, we employ a three-stage cascade amplifier structure. The system consists of power amplifier, matching network and other unit circuits.

![Figure 1. System design of the power amplifier.](image)

To meet the requirements of the system, the 1 dB compression point of the output power amplifier should be slightly greater than 15 W. Because the AB type LDMOS tube has the advantages of large output power, good linearity and high cost performance, the N-channel enhanced LDMOS field effect transistor is employed as the final power amplifier, with an output power of 15 W and a gain of 12.5 dB. In this paper, we set the backoff value to 3 dB based on the power backoff value and linearity. The 1 dB compression point of the driver stage is proposed to be 32 dBm to satisfy the requirements of the final gain and overall gain. Due to the linearity of the pre and driver stage has a greater impact on the system, both them employ Class A power amplifiers. Therefore, the 1 dB compression point of the field effect transistor selected by the driver stage should be 32 dBm, and the gain should be 12 dB.

After the final two-stage amplifier is fixed, the pre-stage is intended to employ a fixed gain module. The chip has been matched within 50Ω. Only the RF choke, bypass capacitor and other components are required to complete the design, and the gain is 18 dB.

2.2. Gain analysis
The gain of system needs to reach 41.76 dB when the output is 15 W. According to the chip selection of the system, good index allocation can improve the system's linearity, output power, gain and other performance parameters. The distribution of gain is shown in Fig. 2.

![Figure 2. Power amplifier gain index allocation.](image)

Where G is the gain, IL is the insertion loss, which is mainly caused by the matching network and connector loss from three stages. As can be seen from Fig. 2, the total gain is about 41.7 dB, which meets the design requirements.

3. Circuit design

3.1. Final power amplifier design
The purpose of the final power amplifier is to obtain 15 W output power, and needs to have the advantages of high linearity, high power, high efficiency, etc. Therefore, the load traction method and
the source traction method are adapted to find the best load impedance and the best source impedance [6, 7, 8] to complete the design of input and output matching network.

The design process can be summarized as: First, select a suitable static operating point through DC simulation. Then, select the appropriate bias circuit for design, and add the relevant filter capacitors. Finally, insert the load traction template in the ADS, replace the FET model with the model of the selected device [9], and then the range of the load traction is determined by the load traction method. The simulation results are shown in Fig. 3.

![Simulated Load Impedances](image)

**Figure 3.** Simulation results of load traction.

In this paper, we give priority to the output power index, and the best load impedance value is $Z_L = 1.487 + j0.836$, and the output power corresponding of the impedance point is 41.81 dBm. We intend to combine distributed parameters with lumped parameters to design the output matching network. On the basis of the load impedance value, Smith chart is called to complete the output impedance design. The design result is shown in Fig. 4.

![Performance of the final output matching network](image)

**Figure 4.** The performance of the final output matching network.

As we can see, IL of the output matching network is only 0.192 dB, and its $S_{11}$ and $S_{22}$ indicators both reach the -30 dB. It indicates that the system has fewer reflected waves, that is, the matching performance is fine. The design process of source traction is basically the same as that of load traction, and no more detailed will be describe. After simulation and optimization, the simulation results of the final power amplifier are shown in Fig. 5.
It can be seen from Fig. 5 that the output power of the final power amplifier is 41.795 dBm. It can be seen that the working point of the power amplifier designed in this paper is located near the 1 dB compression point. At the same time, the system can better balance the relationship between linearity and efficiency.

3.2. Design of Driver stage and pre-stage amplifier

Dominated by high power output and linearity, the high-performance design of the driver stage is consistent with the final stage power amplifier. The simulation results are shown in Fig. 6.

It can be seen from Fig. 6 that the output power of the driver stage power amplifier is 29.146 dBm, which can meet the requirements of driving the final stage power amplifier.

Compared with the driver stage and the final stage, the emphasis of the pre-stage design is on high gain and high linearity, which puts forward higher requirements for the distortion-free design of the signal. The pre-stage of this design considers the design of Class A power amplifier. After matching the design, the simulation results are shown in Fig. 7.

**Figure 5.** Output power and efficiency of the final power amplifier.

**Figure 6.** Output power and efficiency of the driver and power amplifier.

**Figure 7.** Simulation results of pre-stage power amplifier.
As can be seen from Fig. 7, the gain of the pre-stage power amplifier is 18.132 dB, and the gain flatness in the band is fine, which basically meets the requirements.

3.3. Design of Inter-stage matching circuit

To ensure the maximum transmission power between the front and rear stages, it is necessary to insert an impedance matching network to achieve conjugate matching, which can reduce the power loss between the stages. In this paper, we comprehensively adopt integrated capacitors, inductors and microstrip lines for impedance matching design, by combining the advantages of the two to achieve high performance and easy mass production. Taking the matching network between the driver stage and the last stage as an example, the simulation results are shown in Fig. 8.

![Figure 8. The performance of the matching network between the driver stage and the final stage.](image)

As can be seen from Fig. 8, IL of the matching network between the driver stage and the final stage can be lowered to 0.254 dB, and its S11 and S22 indicators have reached more than -20 dB.

3.4. System Simulation

We can obtain cascaded power amplifiers through the design of power amplifiers and matching networks at all levels above. After joint tuning, the simulation curve of the output power and efficiency of the cascade power amplifier is shown in Fig. 9.

![Figure 9. Output power and efficiency of cascaded power amplifier.](image)

As can be seen from above, the output power of the cascaded power amplifier is 41.790 dBm. In addition, the system has fine linearity.

4. Physical testing and analysis

We draw the schematic diagram and PCB layout of the power amplifier through Altium Designer09 software. It is worth paying attention to the problems of vias, anti-interference, and RF routing during design. After the circuit board design, the cavity structure is designed by AutoCAD software, and the shielding function and thermal conductivity of aluminum are employed to improve the performance of the system. To further optimize the performance of the cavity, conductive oxidation treatment is
performed on the design process. After debugging, we test the output signal through the spectrum analyzer N9000A, and corrects the error of the attenuator and RF line before testing (total 42 dB). The test results are shown in Fig. 10.

![Figure 10. System output spectrum.](image)

As can be seen from the spectrogram, the actual output power is 41.817 dBm, and the test results are basically consistent with the simulation results.

5. Conclusion

According to the requirements of the Beidou RDSS terminal for power amplifiers, we propose an overall design framework based on a three-stage cascaded power amplifier and completes the selection of related electronic components. Combined with the load traction technology, small signal S-parameter design method, and multi-objective joint optimization method, the design and simulation of the amplifier circuits at all levels are carried out. Through the design and manufacture of the three-stage power amplifier, the high-power power amplifier applied to the Beidou RDSS terminal has been realized. The design has been mass-produced, indicating that the research results have practical application value.

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