Identification of dislocation-related luminescence participating levels in silicon by DLTS and Pulsed-CL profiling

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Abstract. We present a study of the dislocation network that occurs in the space charge region of a Schottky diode, by means of DLTS and our recently developed cathodoluminescent (CL) technique called Pulsed-CL. The details of the Pulsed-CL technique are provided. We establish a correspondence between the CL spectra of dislocation-related luminescence in silicon in the vicinity of the so-called D1 band and levels determined from DLTS measurements. The centres responsible for the 815 meV CL component are related to dislocations cores while the centres responsible for the 795 meV CL component are related to some defects outside of the dislocation cores.

Introduction
Dislocation networks (DN) in silicon are nowadays highly reproducible and controllable structures with a number of promising applications [1]. Among them is the perspective to use DN as a base of a light emitting diode (LED) fully compatible with silicon technology, which addresses a need of the modern microelectronics industry. Efficient and reliable LEDs that implement dislocation related luminescence (DRL) in silicon are impossible unless the intrinsic mechanisms of DRL as well as the electronic levels they involve are determined. One of the key problems that remain open so far is how to find among the electrical levels detected with space charge region (SCR) spectroscopy those that are responsible for DRL.

Previously, a new approach to solve this problem was suggested based on control of the electrical level occupancy in the SCR of the Schottky-diode. This was achieved by varying the bias voltage, and a correlation between the cathodoluminescent (CL) and electrical properties of DN was demonstrated [2]. Recently that approach was further developed into a new technique referred to as Pulsed-CL, which incorporates the use of a filling pulse instead of DC bias. It is therefore complimentary to conventional DLTS/MCTS profiling but is sensitive to optical transitions only. Details of this new technique are described in section 2.

The main purpose of the present work is to establish direct correspondence between DRL CL spectroscopy components and the levels determined from DLTS measurements, and the role of deep and shallow levels in DRL processes.
1. Experimental Method

We used boron doped Cz-Si 300 mm diameter wafers with initial doping concentration of about $10^{15}$ cm$^{-3}$. They have a (100) surface orientation and were hydrophilically bonded with a small misorientation tilt angle of about 0.5º and twist angle of about 3º. These were thinned so that the DN was 150 nm from the surface. Details of the bonding procedure can be found elsewhere [3]. The piece cleaved from the central part of the bonded wafers was etched in HF:10·H$_2$O solution for 2 minutes to remove the native oxide layer and then semitransparent titanium contacts of a thickness of 50-100 nm were deposited from the thinned side of bonded wafers to prepare a Schottky diode. The diode was examined in a planar geometry inside the chamber of a field-emission scanning electron microscope (FESEM) Zeiss Supra 40 VP with Gatan LHe cryostage and Gatan MonoCL3 system.

The structural properties of the DN were STEM examined using the same FESEM in planar geometry. The space between twist dislocations in the DN was 7 nm, in good agreement with theoretical prediction. The STEM results are reported in another proceeding paper of this conference.

CL was measured with sample excitation through a metal electrode in a spot mode to enable us to measure the electric field effects. The CL signal was acquired in the vicinity of the D1 band of DRL in the range 0.76 – 0.88 eV with LN2 cooled InGaAs 1024 elements array CCD detector Princeton Instruments OMA-V. The stable beam current of the FESEM (change of current is less than 0.2% per hour) coupled with the CCD acquisition system allowed us to perform CL measurements for sufficiently long timescales (typically tens of minutes) to reach desirable accuracy. The electron beam acceleration voltage was 30 kV and electron beam current was 10 nA. The presence of electroluminescence was monitored at each bias and was below the system sensitivity at every applied bias voltages used in our experiments.

DLTS measurements were performed using a SULA DLTS spectrometer and Janis closed cycle helium cryostat with Lakeshore LS-331 temperature controller.

The new technique named Pulsed-CL that we have recently developed was used to profile the levels participating in the DRL process. The temporal sequence of the Pulsed-CL measurements is shown in figure 1A and is similar to that of a DLTS experiment. The bias voltage pulses of value $V_p$ and width $\tau_p$ are applied periodically to fill the traps with the majority carriers within the SCR of the Schottky diode. For the rest of time it is kept under a sufficiently large reverse bias $V_{rb}$.

![Figure 1. Experimental sequence of Pulsed-CL technique (A) and energy band bending diagrams (B) illustrating sample in three main states occurring during such measurements:](image)
Simultaneously with the refilling voltage pulses the electron beam is removed from the sample by the fast beam blanker. The CL signal is collected during the time interval $\tau_{\text{acq}}$ which should be short enough to neglect carrier thermo-emission at the measurement temperature.

The band bending diagrams in figure 1B show the electronic processes which occur during the three main stages of Pulsed-CL measurements.

Stage (1) corresponds to the situation when reverse bias $V_{\text{rb}}$ was applied to the diode for a long time, allowing the DN levels, initially filled with majority carriers, to completely empty. In this stage, the CL signal arises only due to recombination of excess carriers generated by the electron beam. The minority carriers come to DN mostly from the sample bulk provided that the electron beam penetrates the sample much deeper than the SCR width. Only majority carriers that are generated in the close vicinity of the DN can participate in the recombination. Due to a high electrical field value at the DN the excess carriers are swept away from the SCR and only a weak CL signal is expected.

Stage (2) takes place during the application of the filling pulse $V_p$ to the diode when the electron beam is switched off. The DN levels fill with the equilibrium majority carriers to the occupancy degree that is controlled by the $V_p$ value in accordance with Fermi-Dirac statistics.

Stage (3) corresponds to the moment just after the restoration of the reverse bias $V_{\text{rb}}$ and of the electron beam on the sample. Now, the minority excess carriers can recombine with majority carriers trapped by DN levels during the filling pulse. For a short period of time until the DN levels reaches the stationary occupancy defined by the carriers generated by the electron beam, the CL signal exceeds the value detected in the stage (1).

Since the occupancy degree of the DN levels is determined by the refilling pulse voltage in both DLTS and Pulsed-CL experiments the comparison of the dependencies of CL spectral line intensities and of DLTS-peak magnitudes on $V_p$ can be used to establish one-to-one correspondence between the optical transitions and electric levels.

2. DLTS and Pulsed-CL investigations of DRL participating interfacial electronic states

DLTS spectrum of our Schottky-diode with built-in DN is shown in figure 2. The spectrum consists of four peaks, in agreement with previously obtained data on similar silicon samples with DN [3]. Analyzing the Arrhenius plots for DLTS spectral peaks we have derived energy levels for majority carriers in the lower half of the band gap which might be responsible for DRL. These are: shallow level $E_V + 0.1$ eV (narrow peak at about 60 K), and deep levels $E_V + 0.25$ eV, $E_V + 0.3$ eV, $E_V + 0.35$ eV (wide local maxima near 120 K, 150 K, and 200 K respectively). Note that the activation energies for the deep levels could not be obtained precisely due to the overlapping of neighbouring peaks.

The dependence of DLTS peak magnitudes on the refilling voltage pulse level is plotted in figure 3. The curve measured at $T = 147$ K corresponds to the deep levels near $E_V + 0.3$ eV. It exhibits a rapid increase starting from the pulse level of 0.25 V and the saturation at about 0.6 V. The second curve shown in figure 3 was measured at $T = 60$ K and is associated with shallow levels of about $E_V + 0.1$ eV. The DLTS-signal exhibits a rapid increase starting at $V_p = 0.6$ V followed by saturation at $V_p = 1.3$ V.

Both curves show an additional slow increase after plateau regions that occur starting from the filling pulse levels $V_p = 1$ V and $V_p = 1.7$ V for DLTS peaks at 147K and 60K respectively. The origin of the slow increase is not known precisely. They might be simply an artefact due to overloading of the capacitance bridge since the starting pulse voltages coincide well with the voltages responsible for the rapid increase of the diode forward current.
Figure 2. DLTS spectrum of p-Si sample with DN measured at reverse bias $V_{rb} = -2$ V, filling pulse level $V_p = 1.1$ V, and emission rate window of 20 ms.

Figure 3. DLTS enhancement profiles measured at $V_{rb} = -2$ V versus filling pulse magnitude at temperatures corresponding to different peaks of DLTS spectra. DLTS signals at 60 K or 147 K correspond to the levels $E_v + 0.1$ eV or $E_v + 0.3$ eV respectively.

Figure 4. Pulsed-CL spectra acquired at the reverse bias of -2 V after the traps filling with pulses of voltage level varying from -2 V to +1.8 V. $T=70$ K.

Figure 5. Panchromatic Pulsed-CL enhancement profile plotted as integral intensity of CL spectra enhancement in the vicinity of D1 band versus filling pulse magnitude measured at 70 K.

The CL measurements were carried out using filling pulse width $\tau_f = 1$ $\mu$s that enabled complete filling of the trap. The acquisition time was $\tau_{acq} = 5$ $\mu$s, significantly less than the thermoemission time constant for both deep and shallow levels but longer than the time constant of CL recombination.

Examples of Pulsed-CL spectra measured at different values of filling pulse are presented in figure 4. CL spectra exhibit the main maximum at about 815 meV conveniently called the D1-band of DRL in silicon, as well as a low energy shoulder. The relative enhancement of the panchromatic integral intensity of CL for different filling pulse magnitudes retrieved from experimental data of figure 4 is
plotted in figure 5. The Pulsed-CL profile in figure 5 increases from the zero level of the filling pulse value up to saturation at about $V_p = 1.3$ V. Comparing the panchromatic Pulsed-CL voltage profile with DLTS profiles in figure 3 we conclude that the D1 luminescence goes via the shallow levels responsible for the DLTS peak at 60 K but not via the deeper levels responsible for the DLTS signal at 147 K since the latter saturates at significantly lower filling pulse values of about 0.6 V. On the other side, the minimum pulse voltage for CL-enhancement is significantly less than that for appearance of the DLTS-peak at 60K, indicating an influence of deep level occupancy on D1 DRL. The possible reasons for that will be discussed in the next section.

Figure 6 shows DLTS spectra measured at different filling pulse values in the range from 0.8 V to 1.7 V. It is seen that the peak at 60 K has a low temperature shoulder which exhibits a faster increase with the increase of filling pulse magnitude than the peak at 60 K. This lower temperature shoulder reflects the presence of even shallower levels than Ev + 0.1 eV. Figure 7 represents CL enhancement spectra that were obtained by subtraction of the CL spectrum registered without filling pulses and by smoothing. It is seen that the shape of the CL spectra changes upon applied voltage pulse magnitude and can be decomposed into two components: one at 785 meV and another at 815 meV.

Figure 6. DLTS spectra measured with filling pulse values $V_p$ varying from 0.8 V to 1.7 V ($V_{rb} = -2$ V) in temperature range of 30 – 75 K demonstrating different behavior of shallow levels. Emission rate window was 20 ms.

Figure 7. Pulsed-CL enhancement spectra retrieved from experimental Pulsed-CL spectra for filling pulse magnitudes varying from 0 V to + 1.8 V at temperature of 70 K. Calculation includes subtraction of CL spectrum registered without filling pulses and smoothing.

The relative DLTS signal enhancement versus filling pulse value plots measured at $T = 44$ K and at $T = 60$ K are shown in figure 8. As expected, the voltage profile for the shallower level with the peak at $T = 44$ K is shifted to the larger filling pulse values at about 0.15 V from the profile measured at 60 K. The voltage profiles for relative Pulsed-CL enhancement measured at photon energies of 795 meV and of 815 meV are plotted in figure 9. The profile for the 815 meV component is shifted to the higher values of filling pulse from the profile measured at a photon energy of 795 meV by a value of 0.15 V that coincides well with the pulse voltage difference for the above described DLTS peaks. Thus, from comparison of Pulsed-CL and DLTS pulse voltage profiling we can identify the CL components of 795 meV and of 815 meV with the levels responsible for DLTS peak at 60 K and at 44 K respectively.
3. Discussion

CL spectra measured in the vicinity of the so-called D1 band of DRL in silicon corresponded in our sample with DN containing at least two components: 815 meV and 795 meV. The original Cz-Si wafers themselves do not show any luminescence in the region 0.7 eV – 0.9 eV, as confirmed by CL measurements with backside excitation of our bonded wafers. Thus, both components of the CL spectra must be related to the presence of the DN.

From the comparison of DLTS and Pulsed-CL refilling voltage profiles it was concluded that both 815 meV and 795 meV DRL components could be identified with shallow levels near $E_v + 0.1$ eV. Moreover, the 815 meV and 795 meV components were found to have well distinguishable pulse voltage profiles. Lastly, the CL component at 795 meV vanishes at small reverse bias voltages (without application of refilling pulses) while the 815 meV component of the CL spectrum persists and does not change significantly within the reverse voltage ranges of several volts. That indicates a large difference in the carrier cross section for the defects responsible for these CL signals. There is a difference between the larger majority carriers capture cross-section of centres responsible for the 815 meV component, and those responsible for the 795 meV CL component. This difference can be explained by the existence of an attractive electrical potential which could be the deformation potential of dislocations. A confirmation of the existence of the attractive electrical potential is the Pool-Frenkel effect registered in [3] for the shallow level on the same sample. Removal of the 795 meV CL signal by an electrical field means that these centres do not have such an attractive electrical potential.

These findings lead us to the conclusion that the luminescence centres of the 815 meV CL component are related to dislocations cores but the centres responsible for the 795 meV CL component are related to defects outside the dislocations cores, and their deformation potential band bending. The last CL component often accompanies D1 and is commonly thought to be associated with some oxygen complexes or clusters in the silicon matrix [2, 4] that are segregated at the DN. These oxygen complexes might be either artefacts of hydrophilic process in which initial wafers are oxidized before bonding or products of segregation of oxygen dissolved in Cz-Si crystals.

Detailed comparison of refilling pulse voltage profiles of the Pulsed-CL and DLTS reveals that Pulsed-CL profiles are more expanded towards lower pulse voltages than DLTS profiles for the shallow levels (compare figures 8 and 9). The threshold pulse voltages for CL-enhancement are close to those that are observed for the DLTS signal from the deep levels (compare figures 9 and 3). The initial bias voltage for the voltage region where the Fermi-level is pinned by the shallow level appears
as a plateau on capacitance-voltage curves (not shown for brevity). Thus it appears we can explain the smoothness of the Pulsed-CL voltage profile by an indirect effect of the emptying or filling of the deep levels with the majority carriers on CL-intensity as follows.

At the end of the period of the excitation of the sample with the electron beam, deep level occupancy decreases. This gives rise to a corresponding decrease of the potential at DN with respect to its equilibrium value without any excitation, and to a lower voltage pulse level to start the filling of the shallow states responsible for DRL at the beginning of the refilling period. In addition, just after the end of the refilling period and the recovery of the reverse bias voltage, the filled deep DN levels cause the reduction of the electrical field direction in the region between the DN and metal electrode, or even its inversion as was reported in [2]. Such an effect could be illustrated by the energy band bending diagrams plotted for different bias values in figure 1B. When the deep levels are empty the electrical field is large and the majority carriers generated by the electron beam are swept out from the SCR without recombination. When the deep levels are being filled with majority carriers during the filling voltage pulse the electrical field decreases and the after-pulse capture rate for majority carriers effectively increases.

4. Summary
Two components of CL spectra related to the presence of DN in the silicon wafer bonding interface were registered in the vicinity of the D1 band, at 795 meV and 815 meV. A new technique called Pulsed-CL capable of registering CL spectra depending on the initial occupancy conditions of carriers traps controlled by the filling pulse was described. The correspondence between DLTS and DRL peaks in the photon energy range from 0.75 eV – 0.9 eV was established by comparison of DLTS profiles and Pulsed-CL profiles. It was found that both 795 meV and 815 meV CL components are caused by recombination through shallow levels with energy of about Ev + 0.1eV. From the analysis of the data it is concluded that the centres responsible for the 815 meV CL component are related to dislocations cores but the centres responsible for the 795 meV CL component are related to defects outside the dislocations cores.

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