Design and Implementation of Carbon Nano-tube based Full Adder at 32nm Technology for High Speed and Power Efficient Arithmetic Applications

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Abstract. Due to physical, material, technological, power-thermal and economical difficulties, scaling of CMOS transistors will stop very soon. Due to efficiency of power and speed compared to CMOS transistors, Carbon Nano-tube transistors are best suitable element to design logic circuits. So, CNTFETS have been utilized in designing of proposed full adder (FA) and 4-bit ripple carry adder (RCA) in this paper. Proposed FA and RCA have been compared to rival designs on bases of power, speed and power-delay-product (PDP). FA and RCA circuits have been analysed with the variation of temperature from 0°C to 100°C while the variation of supply voltages is from 0.7V to 1.3V. For all temperatures and all supply voltages, proposed FA and proposed RCA have the least power consumption, shortest delay and lowest PDP. SPICE has been utilized for simulating FAs and RCAs in 32 nm process node. Even though the fabrication is complicated than CMOS counterparts but simulation results confirm usefulness of proposed FA and RCA for high speed and power efficient arithmetic applications.

1. Introduction
The Addition is the most basic arithmetic operation. The adders are basic building blocks of numerous VLSI (Very large-scale integration) digital circuits such as CPU (central-processing-unit) and DSP (digital signal processor). The adder circuit is on critical path in many cases and decides the overall performance of the above defined systems. The ALU (arithmetic-logic-unit) is a combination of many logic circuits to execute arithmetic & logic instructions in CPU of processors/micro-controllers, adder is the fundamental element of ALU [1]. Designing an optimal full adder (FA) will have a remarkable effect on performance of the ALU and other digital circuits and systems [2]. Normally, Full Adder circuit is the mostly used component in arithmetic operations. Besides addition, the full adder can be used in other arithmetic operations like multiplication, exponentiation, division and subtraction [3].

In computer arithmetic operations, the role of FA is divided into two important parts. One classification has chain structured applications [4], like array multipliers and ripple carry adders RCA (ripple carry adders). In this classification, mostly from Carry In (C_i) to Carry Out (C_{out}) of the FA, is critical path. The slower Carry Out (C_{out}) production will increase the worst case delay and also generate further glitches in coming stages. So, it will result in increased power dissipation. The second classification has tree structured applications that is often applied in Wallace–Dadda tree multipliers and multiplier-less digital filters [5].
The full adder is a three-input logic circuit which determines sum of the two bits x and y as operands and a carry-bit from the former stage (C_i). It generates two outputs Sum (S_out) and Carry Out (C_out).

The Boolean equation of Sum and Carry Out are given as:

\[ S_{out} = x'y'z + x'yz' + xy'z + xyz \]  
\[ C_{out} = xy + xz + yz \]  

The scaling of transistor’s size not only improves the performance but also increases the power density. However, the CMOS technology faced various challenges due to scaling of transistor’s size. The further downscaling is looking to be very much difficult [6-9]. The new material, which has potential to replace CMOS technology, is carbon nano-tube and CNTFET (carbon nano-tube field effect transistor) [10]. On the ground of number of tubes, there are two types of CNTs:

1. S.W.C.N.Ts. (Single wall carbon nanotubes)
2. M.W.C.N.Ts. (Multi wall carbon nanotubes)

S.W.C.N.T is graphite sheet of one atom thickness, rolled and caped at the terminations to form a seamless cylinder as shown by Figure 1a, while in M.W.C.N.T there is a tube within a tube as illustrated by Figure 1b [11-14].

S.W.C.N.Ts can be categorised as armchair, zig-zag and chiral type as shown by Figure 2. A S.W.C.N.T is a metallic or semiconducting 1-D conductor depending on the layout of carbon atoms decided by the direction of roll of graphene sheet (Chirality, C_h). Its amplitude is shown in equation (3)[15].

\[ C_h = a \sqrt{ (n_1^2 + n_2^2 + n_1 n_2) } \]  

The relationship of CNT’s diameter (D_{CNT}) and Chirality (C_h) is shown in equation (4) [15]

\[ D_{CNT} = C_h / \pi \]  

where a is the “graphene lattice constant (0.249 nm)” and n_1, n_2 are +ve integers that denote the tube’s chirality.

2. Existing Full Adder Architectures

2.1 Conventional Full Adder

There are two inputs ‘A’, ‘B’ and an incoming carry from the previous stage ‘C_i’ and there are two outputs Sum ‘S_0’ and carry out ‘C_0’. The implementation of the conventional FA is represented by Figure 3 [16].
2.2 Full Adder Circuit Presented by S. Goel et al.
S. Goel et al. presented Hybrid-CMOS FA (FA-Goel) in [17] shown in Figure 4. Pass transistor logic (PTL) with static CMOS circuit techniques has been used in this circuit. Exclusive OR-Exclusive NOR, sum and carry, the adder has 3 logic modules. FA-Goel adder produces outputs of Exclusive-OR and Exclusive-NOR, concurrently. The output of Exclusive OR-Exclusive NOR, module is utilized to produce sum \( S_0 \) and carry output \( C_0 \).

2.3 Full Adder Circuit Presented by C.K. Tung et al.
C.K. Tung et al. presented multiplexer based FA [18]. FA-Tung has 3 logic modules: Exclusive OR-Exclusive NOR, sum and carry modules to produce circuit output, sum and carry respectively. FA-Tung is shown by Figure 5.

If \( H=0 \), \( C_0 = A \) \hspace{1cm} (5)
and if

\( H=1 \), \( C_0 = C_i \) \hspace{1cm} (6)

The delay from \( C_i \) to \( C_o \) is delay of only an NMOS. Thus FA by C.K. Tung produce fast carry propagation. The logic equations of sum \( S_0 \) and carry output \( C_0 \) are illustrated by equations (7) & (8) respectively.

\[
S_0 = C_i H_b + C_0 \bigcirc H \hspace{1cm} (7)
\]

\[
C_0 = C_i H + H_b A \hspace{1cm} (8)
\]

Where \( H = A \oplus B \), \( H_b = A \odot B \)

3. Proposed Full Adder Architecture
In this paper, carbon nano-tube based FA architecture has been proposed. The proposed FA is divided into three modules. In module 1, concurrent production of Exclusive-OR and Exclusive-NOR is needed to produce non-skewed outputs because these are utilized as select lines of the multiplexer (MUX). In the proposed work, full-swing and concurrent Exclusive-OR and Exclusive-NOR’s outputs have been generated. The remaining two modules depend on the output of first module \( (S_0 \text{ and } S_b) \), so the speed of first module is very crucial. Two cross-coupled p-type CNTFETs increase the speed of the first module. Thus the proposed FA is faster as compared to rival adders.
The module 2 is needed to produce the Sum output ($S_{out}$). $S$, $S_b$ and $C_i$ are three inputs to this module. This module also acts as XOR or XNOR and can be utilized in the first module. In some adders four transistors are used in module 2 to generate $S_{out}$ but there will be problem of threshold loss in these adders and may result in failure or longer delay in switching a transistor. That may further result in consuming more power and glitches. In the proposed FA represented by Figure 6, six CNTFET transistors are used in module 2 to avoid these problems, however this will increase area. In proposed FA, CNTFET static Inverter is utilized to generate $S_{out}$ to have increased driving capability.

Output of module 3 is given by equation (9)

$$C_{out} = X.S_b + C_i.S$$  \hspace{1cm} (9)

This equation can be implemented by 2:1 MUX using $S$ and $S_b$ as select lines. One of the possible options to realize MUX is using TGs (transmission gates), but the essential driving capability to drive other stages of adder will not be delivered. If we use output buffer with TGs, extra delay and area will be introduced.

The other possible way of realization of module 3 is given by the expression:

$$C_{out} = [(X \ (XOR) 
Y). C_i + X'.Y]'$$  \hspace{1cm} (10)

An inverter and a TG are used to realize[$(X \ (XOR) 
Y). C_i$]. $S$ and $S_b$ are the control signals of this TG. Two PCNTFET and Two NCNTFET are utilized to produce $X'.Y'$. A CNTFET inverter is used to generate $C_{out}$. Thus in this work, to produce $C_{out}$, hybrid-CNTFET stage is used with a CNTFET inverter to have enhanced performance and driving capabilities.
4. Simulation Results and Discussion

4.1 Full Adders

Table 1 shows power consumption and input carry ($C_i$) to output carry ($C_{out}$) propagation delay of existing and proposed full adders with the variation of temperature from 0°C to 100°C. The table shows that FA-proposed has up to 112.90, 80.28 and 56.77 times lesser power consumption as compared to existing FA-Conventional, FA-Goel and FA-Tung respectively. The power performance of FA-proposed improves with increase in temperature. The table also shows that the proposed FA has up to 6.01, 5.81 and 2.31 times shorter propagation delay as compared to existing FA-Conventional, FA-Goel and FA-Tung respectively. Figure 7 shows the power consumption and input carry $C_i$ to output carry $C_{out}$ propagation delay of existing and proposed full adders as a function of temperature. It is clear from the figure that for every discussed temperature FA-proposed has the least power consumption and shortest delay.

Table 1. Power consumption and input $C_i$ to output $C_{out}$ Propagation Delay of full adders with temperature variation

| Temperature (°C) | FA-Conventional | FA-Goel | FA-Tung | FA-proposed | FA-Conventional | FA-Goel | FA-Tung | FA-proposed |
|------------------|-----------------|---------|---------|-------------|-----------------|---------|---------|-------------|
| 0                | 70.01           | 49.81   | 35.23   | 2.63        | 20.12           | 21.81   | 12.43   | 8.26        |
| 25               | 120.62          | 85.94   | 60.68   | 2.63        | 23.95           | 21.80   | 12.72   | 8.26        |
| 50               | 194.77          | 138.73  | 97.96   | 2.63        | 27.24           | 27.86   | 12.77   | 6.07        |
| 75               | 296.92          | 211.13  | 149.30  | 2.63        | 31.37           | 31.78   | 13.74   | 8.26        |
| 100              | 430.99          | 305.56  | 216.65  | 2.63        | 36.45           | 35.26   | 14.03   | 6.07        |

Table 2 shows power-delay-product (fJ) for Input $C_i$ to output $C_{out}$ of full adders with temperature variation

| Temperature (°C) | FA-Conventional | FA-Goel | FA-Tung | FA-proposed |
|------------------|-----------------|---------|---------|-------------|
| 0                | 1408.60         | 1086.36 | 437.91  | 21.72       |
| 25               | 2888.85         | 1873.49 | 771.85  | 21.72       |
| 50               | 5305.53         | 3865.02 | 1250.95 | 15.96       |
| 75               | 9314.38         | 6709.71 | 2051.38 | 21.72       |
| 100              | 15709.59        | 10774.05| 3039.60 | 15.96       |

Table 2 shows power-delay-product for input carry $C_i$ to output carry $C_{out}$ of existing and presented full adders with the variation of temperature from 0°C to 100°C. The table shows that the FA-proposed has up to 984.31, 675.07 and 190.45 times lesser power-delay-product as compared to existing FA-
Conventional, FA-Goel and FA-Tung respectively. Figure 8 shows PDP for input carry $C_i$ to output carry $C_{out}$ of existing and presented full adders as a function of temperature. It can be observed that for all temperatures FA-proposed has the least PDP.

Table 3. Input A to output ($C_{out}$) Propagation Delay and PDP of full adders with temperature variation

| Temperature ($^\circ$C) | Input A to output ($C_{out}$) Propagation Delay (pS) | PDP for Input (A) to output ($C_{out}$) ($\Omega$) |
|--------------------------|-----------------------------------------------------|--------------------------------------------------|
|                          | FA-Conventional | FA-Goel | FA-Tung | FA-proposed | FA-Conventional | FA-Goel | FA-Tung | FA-proposed |
| 0                        | 17.27          | 26.22   | 36.39   | 9.56        | 1209.07        | 1306.02 | 1282.02 | 25.14       |
| 25                       | 20.86          | 28.92   | 27.45   | 9.56        | 2516.13        | 2485.38 | 1665.67 | 25.14       |
| 50                       | 24.20          | 31.51   | 25.36   | 5.20        | 4713.43        | 4371.38 | 2484.27 | 13.68       |
| 75                       | 27.87          | 34.32   | 25.21   | 9.56        | 8275.16        | 7245.98 | 3763.85 | 25.14       |
| 100                      | 31.36          | 36.92   | 25.29   | 5.20        | 13515.85       | 11281.28 | 5479.08 | 13.68       |

Table 3 shows input A to output carry ($C_{out}$) propagation delay and PDP of existing and presented full adders with the variation of temperature from 0$^\circ$C to 100$^\circ$C. The table shows that FA-proposed has up to 6.03, 7.1 and 4.88 times shorter propagation delay as compared to existing FA-Conventional, FA-Goel and FA-Tung respectively. The table shows that the FA-proposed has up to 988, 824.66 and 400.52 times lesser power-delay-product as compared to existing FA-Conventional, FA-Goel and FA-Tung respectively. For every discussed temperature FA-proposed has the shortest delay and least PDP.

Table 4. Power Consumption and Input $C_i$ to output $C_{out}$ Propagation Delay of full adders with supply variation

| Supply voltage (V) | Power Consumption (nW) | Propagation Delay (pS) |
|-------------------|------------------------|------------------------|
|                   | FA-Conventional | FA-Goel | FA-Tung | FA-proposed | FA-Conventional | FA-Goel | FA-Tung | FA-proposed |
| 0.7               | 32.57          | 23.41   | Failed  | 2.02        | 47.17          | 45.97   | Failed  | 10.33       |
| 0.9               | 120.62         | 85.94   | 60.68   | 2.63        | 23.95          | 21.80   | 12.72   | 8.26        |
| 1.1               | 480.48         | 334.20  | 216.02  | 3.25        | 13.11          | 18.93   | 12.89   | 6.52        |
| 1.3               | 2287.0         | 1504.60 | 853.50  | 3.90        | 9.15           | 16.57   | 8.53    | 5.73        |

Table 4 shows power consumption and input carry ($C_i$) to output carry ($C_{out}$) propagation delay of existing and presented full adders with the variation of supply voltage from 0.7V to 1.3V. The table shows that FA-proposed has up to 586.41, 385.80 and 218.85 times lesser power consumption as compared to existing FA-Conventional, FA-Goel and FA-Tung respectively. At 0.7V FA-Tung has
very degraded output. The power performance of FA-proposed improves with increase in supply voltage. The table also shows that FA-proposed has up to 4.57, 4.45 and 1.98 times shorter propagation delay as compared to existing FA-Conventional, FA-Goel and FA-Tung respectively. Figure 9 and Figure 10 represent the power consumption and input carry ($C_i$) to output carry ($C_{out}$) propagation delay of existing and presented FAs with the variation of supply voltage respectively. It is clear from the figure that for every discussed supply voltage, FA-proposed has the least power consumption and shortest delay.

**Table 5.** Power-delay-product ($fJ$) for input carry ($C_i$) to output carry ($C_{out}$) with supply variation

| Supply voltage (V) | FA-Conventional | FA-Goel | FA-Tung | FA-proposed |
|-------------------|-----------------|---------|---------|-------------|
| 0.7               | 1536.33         | 1076.16 | Failed  | 20.87       |
| 0.9               | 2888.85         | 1873.49 | 771.85  | 21.72       |
| 1.1               | 6299.09         | 6326.41 | 2784.50 | 21.19       |
| 1.3               | 20926.05        | 24931.22| 7280.36 | 22.35       |

**Figure 11.** PDP for input carry ($C_i$) to output carry ($C_{out}$) as a function of supply voltage

**Figure 12.** Input A to $C_{out}$ Propagation Delay as a function of supply voltage

**Table 6.** Input A to output $C_{out}$ Propagation Delay and PDP of full adders with supply variation

| Supply voltage (V) | Input a to output $C_{out}$ Propagation Delay (pS) | PDP for Input a to output ($fJ$) |
|--------------------|---------------------------------------------------|---------------------------------|
|                    | FA-Conventional | FA-Goel | FA-Tung | FA-proposed | FA-Conventional | FA-Goel | FA-Tung | FA-proposed |
| 0.7                | 43.55            | 45.92   | Failed  | 17.36       | 1418.42         | 1074.99 | Failed  | 35.07       |
| 0.9                | 20.86            | 28.92   | 27.45   | 9.56        | 2516.13         | 2485.38 | 1665.67 | 25.14       |
| 1.1                | 12.11            | 21.53   | 17.28   | 10.75       | 5818.61         | 7195.33 | 3732.83 | 34.94       |
| 1.3                | 7.38             | 16.37   | 13.83   | 5.28        | 16878.06        | 24630.30| 11803.91| 20.59       |

Table 5 shows power-delay-product for input carry ($C_i$) to output carry ($C_{out}$) of existing and presented FAs with the variation of supply voltage from 0.7V to 1.3V. The table shows that the FA-proposed has up to 936.29, 1115.49 and 325.74 times lesser power-delay-product as compared to existing FA-Conventional, FA-Goel and FA-Tung respectively. The PDP of FA-proposed improves with increase in supply voltage. Figure 11 shows PDP for input carry ($C_i$) to output carry ($C_{out}$) of existing and proposed full adders as a function of supply voltage. This can be observed from the figure that for every discussed voltage, FA-proposed has the least PDP. Table 6 shows input A to output carry ($C_{out}$) propagation delay and PDP of existing and proposed full adders with the variation of supply voltage from 0.7V to 1.3V. The table also shows that FA-proposed has up to 2.51, 3.10 and 2.87 times
shorter propagation delay as compared to existing FA-Conventional, FA-Goel and FA-Tung respectively. The table shows that the FA-proposed has up to 819.72, 1196.23 and 573.28 times lesser power-delay-product as compared to existing FA-Conventional, FA-Goel and FA-Tung respectively. Figure 12 represents input A to output carry (C\textsubscript{out}) propagation delay of existing and proposed full adders as a function of supply voltage. This can be observed from results that for every discussed voltage FA-proposed has the shortest delay and least PDP.

### 4.2 4-bit Ripple Carry Adder (RCA)

In this paper, 4-bit Ripple Carry Adders have been implemented using all four discussed existing and proposed full adders. The simulation results have been discussed under this heading. Table 7 illustrates power consumption and input C\textsubscript{i} to output carry of 4\textsuperscript{th} FA (C\textsubscript{4out}) propagation delay of existing and presented 4-bit RCA with the variation of temperature from 0°C to 100°C. The table shows that RCA-proposed has up to 164.03, 116.29 and 82.43 times shorter propagation delay as compared to existing RCA-Conventional, RCA-Goel and RCA-Tung respectively. The power performance of RCA-proposed improves with increase in temperature. The table also shows that RCA-proposed has up to 6.05, 7.60 and 500.25 times shorter propagation delay as compared to existing RCA-Conventional, RCA-Goel and RCA-Tung respectively. It is clear from the table that for every discussed temperature in this paper RCA-proposed has the least power consumption and shortest delay. Table 8 shows power-delay-product for input carry C\textsubscript{i} to output carry C\textsubscript{4out} of existing and proposed RCA with the variation of temperature from 0°C to 100°C. The table shows that the RCA-proposed has up to 991.95, 883.47 and 11550.28 times lesser power-delay-product as compared to existing RCA-Conventional, RCA-Goel and RCA-Tung respectively. The performance of RCA-Tung is very poor at low temperatures. For all temperatures, RCA-proposed has the lowest PDP.

**Table 7.** Power consumption and input C\textsubscript{i} to output C\textsubscript{4out} propagation delay of 4-bit RCA with temperature variation

| Temperature (°C) | 4-bit RCA Conventional | 4-bit RCA -Goel | 4-bit RCA -Tung | 4-bit RCA proposed | 4-bit RCA Conventional | 4-bit RCA -Goel | 4-bit RCA -Tung | 4-bit RCA proposed |
|------------------|------------------------|----------------|----------------|------------------|------------------------|----------------|----------------|------------------|
| 0                | 280.033                | 199.25         | 140.93         | 10.51            | 80.480                | 103.28         | 12061.00       | 24.11            |
| 25               | 482.491                | 343.75         | 242.69         | 10.51            | 95.800                | 119.48         | 12060.00       | 24.11            |
| 50               | 779.096                | 554.89         | 391.77         | 10.51            | 108.960               | 139.27         | 934.28         | 24.11            |
| 75               | 1187.70                | 844.49         | 597.06         | 10.51            | 125.480               | 160.56         | 69.62          | 24.11            |
| 100              | 1724.00                | 1222.20        | 866.29         | 10.51            | 145.800               | 183.17         | 75.73          | 24.11            |

**Table 8.** Power-delay-product for input C\textsubscript{i} to output C\textsubscript{4out} of 4-bit RCA with temperature variation

| Temperature (°C) | 4-bit RCA Conventional | 4-bit RCA -Goel | 4-bit RCA -Tung | 4-bit RCA proposed |
|------------------|------------------------|----------------|----------------|------------------|
| 0                | 22537.06               | 20578.54       | 1699756.73     | 253.40           |
| 25               | 46222.64               | 41071.25       | 2926841.40     | 253.40           |
| 50               | 84890.30               | 77279.53       | 366022.88      | 253.40           |
| 75               | 149032.60              | 135591.31      | 41567.32       | 253.40           |
| 100              | 251359.20              | 223870.37      | 65604.14       | 253.40           |

Table 9 shows power consumption and input carry (C\textsubscript{i}) to output carry of 4\textsuperscript{th} FA (C\textsubscript{4out}) delay of existing and proposed 4-bit RCA with the variation of supply voltage from 0.7V to 1.3V. The table shows that RCA-proposed has up to 587.20, 385.87 and 218.85 times improvements in power...
consumption as compared to existing RCA-Conventional, RCA-Goel and RCA-Tung respectively. At lower supply voltages, RCA-Tung has poor performance. The power performance of RCA-proposed improves with increase in supply voltage. The table also shows that RCA-proposed has up to 6.13, 7.33 and 500.21 times improvements in propagation delay as compared to existing RCA-Conventional, RCA-Goel and RCA-Tung respectively. It is clear from the table that for every discussed voltage RCA-proposed consumes the lowest power and has shortest delay. Table 10 shows power-delay-product for input carry (C_i) to output carry (C_{4out}) of 4bit RCAs with the variation of supply voltage from 0.7V to 1.3V. The table shows that the RCA-proposed has up to 1671.53, 2077.88 and 15723.49 times improvements in power-delay-product as compared to existing RCA-Conventional, RCA-Goel and RCA-Tung respectively. The performance of RCA-Tung is very poor. For all supply voltage, RCA-proposed has the lowest PDP.

**Table 9.** Power consumption and input C_i to output (C_{4out}) propagation delay of 4-bit RCA with supply variation

| Supply Voltage (V) | Power Consumption (nW) | Input C_i to output (C_{4out}) Propagation Delay (pS) |
|--------------------|------------------------|------------------------------------------------------|
|                    | 4bit RCA Conventional   | 4bit RCA -Goel | 4bit RCA -Tung | 4bit RCA proposed | 4bit RCA Conventional | 4bit RCA -Goel | 4bit RCA -Tung | 4bit RCA proposed |
| 0.7                | 130.281                | 93.64         | Failed        | 8.08             | 188.660            | 225.62         | Failed        | 30.77          |
| 0.9                | 482.491                | 343.75        | 242.69        | 10.51            | 95.800             | 119.48        | 12060.00      | 24.11          |
| 1.1                | 1922.00                | 1336.60       | 863.85        | 13.01            | 52.452             | 85.43         | 931.48        | 22.36          |
| 1.3                | 9148.50                | 6011.90       | 3409.70       | 15.58            | 36.608             | 69.25         | 923.94        | 12.86          |

**Table 10.** Power-delay-product (fJ) for Input C_i to output (C_{4out}) of 4-bit RCA with supply variation

| Supply Voltage (V) | 4bit RCA Conventional | 4bit RCA -Goel | 4bit RCA -Tung | 4bit RCA proposed |
|--------------------|------------------------|----------------|----------------|-------------------|
| 0.7                | 24578.81               | 21127.06       | Failed         | 248.62            |
| 0.9                | 46222.64               | 41071.25       | 2926841.40     | 253.40            |
| 1.1                | 100812.74              | 114185.74      | 804659.00      | 290.90            |
| 1.3                | 334908.29              | 416324.08      | 3150358.22     | 200.36            |

**5. Conclusion**

Due to many difficulties, scaling of CMOS transistor will stop very soon. Owing to efficiency of power and speed compared to CMOS transistors, Carbon Nano-tube transistors are best suitable transistors to design logic circuits. So, CNTFETS have been utilized in designing of proposed FA and RCA in this paper. FA-proposed and RCA-proposed have been compared to rival designs on bases of power, speed and power-delay-product (PDP).

FA and RCA circuits have been analysed with the variation of temperature from 0°C to 100°C and with variation of supply voltages from 0.7V to 1.3V. The power performance of FA-proposed improves with increase in temperature. It can be observed from simulation results that for all temperatures FA-proposed has the least power consumption, shortest delay and lowest PDP among discussed FAs. At 0.7V FA-Tung has very degraded output. The power performance of FA-proposed improves with increase in supply voltage and for every discussed voltage, FA-proposed has the least power consumption, shortest delay and lowest PDP. For all supply voltages, FA-proposed also improves with increase in supply voltage.

The performance of RCA-Tung is very poor at low temperatures. The power performance of the RCA-proposed improves with increase in temperature however, for all temperatures RCA-proposed has the least power consumption, shortest delay and lowest PDP. At lower supply voltages, RCA-Tung has poor performance. The power performance of RCA-proposed improves with increase in supply voltage, however, for every discussed voltage; RCA-proposed has the least power
consumption, shortest delay and lowest PDP. SPICE has been utilized for simulating FAs and RCAs in 32 nm process node. Even though the fabrication is complicated than CMOS counterparts but FA-proposed and RCA-proposed are speed and power efficient.

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