A 28-nm Convolutional Neuromorphic Processor Enabling Online Learning with Spike-Based Retinas

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Abstract—In an attempt to follow biological information representation and organization principles, the field of neuromorphic engineering is usually approached bottom-up, from the biophysical models to large-scale integration in silico. While ideal as experimentation platforms for cognitive computing and neuroscience, bottom-up neuromorphic processors have yet to demonstrate an efficiency advantage compared to specialized neural network accelerators for real-world problems. Top-down approaches aim at answering this difficulty by (i) starting from the applicative problem and (ii) investigating how to make the associated algorithms hardware-efficient and biologically-plausible. In order to leverage the data sparsity of spike-based neuromorphic retinas for adaptive edge computing and vision applications, we follow a top-down approach and propose SPOON, a 28-nm event-driven CNN (eCNN). It embeds online learning with only 16.8-% power and 11.8-% area overheads with the biologically-plausible direct random target projection (DRTP) algorithm. With an energy per classification of 313nJ at 0.6V and a 0.32-mm² area for accuracies of 95.3% (on-chip training) and 97.5% (off-chip training) on MNIST, we demonstrate that SPOON reaches the efficiency of conventional machine learning accelerators while embedding on-chip learning and being compatible with event-based sensors, a point that we further emphasize with N-MNIST benchmarking.

I. INTRODUCTION

The field of neuromorphic engineering takes its roots into the discovery that the MOS transistor operated in subthreshold could directly emulate the ion channels dynamics in the brain [1]. This led to a long tradition of bottom-up design since the late 1980s, going from neuroscience observation and biophysical neuron and synapse models to analog and digital small-scale [2]–[7] and large-scale [8]–[12] integrations in silico. Bottom-up neuromorphic processors are thus ideal as experimentation platforms for cognitive computing and neuroscience [13], [14], for which they even help to reverse-engineer the brain with analysis by synthesis (Fig. 1). However, the key challenge lies in applying them to real-world scenarios, which is yet to be demonstrated with an efficiency advantage compared to conventional frame-based artificial and convolutional neural network (ANN, CNN) hardware accelerators [14], [15].

In order to address the difficulty of bottom-up neuromorphic designs in tackling real-world problems efficiently, a few top-down designs have recently been proposed for adaptive edge computing (e.g., [15]–[18]), ensuring both robustness to uncontrolled environments and low-cost deployment for applications power- and resource-constrained during the training phase. Starting from this applicative problem, top-down designs investigate how to embed online learning with a focus on hardware efficiency and biological plausibility (Fig. 1). However, top-down designs currently appear to be either spiking neural networks (SNNs) with event-driven processing at the expense of accuracy [16], [17] or binary neural networks (BNNs) with high accuracy at the expense of conventional frame-based processing [15]. The chip from Chen et al. [18] allows exploring both sides with an SNN embedding STDP that can also be programmed as a BNN using offline-trained weights.

Therefore, in this work, we propose SPOON (standing for spiking online-learning convolutional neuromorphic processor), an event-driven CNN (eCNN) for adaptive edge computing. Event-driven convolutions with time-to-first-spike coding leverage sparsity from event-based neuromorphic retinas [19], an idea now also explored for conventional machine learning accelerators [20], while a combination with frame-based processing ensures maximum data reuse and parallelism in fully-connected layers. SPOON embeds online learning at low power and area overheads with the biologically-plausible direct random target projection (DRTP) algorithm [21], which we introduced recently to release the key issues of the successful error backpropagation (BP) algorithm [22] precluding hardware efficiency and biological plausibility. We demonstrate that, to the best of our knowledge, only SPOON allows reaching the efficiency of conventional machine learning accelerators while embedding on-chip learning and being compatible with event-based sensors. The architecture of SPOON is described in Section II, implementation details and benchmarking results on MNIST and N-MNIST are given in Section III.

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Fig. 1: Summary of bottom-up and top-down neuromorphic design approaches.

Fig. 2: Block diagram of the SPOON event-driven CNN (eCNN) processor.
II. ARCHITECTURE

A block diagram of SPOON is shown in Fig. 2. Four-phase-handshake address-event representation (AER) buses [23] are used for event-driven handling of input sensor spikes and of output inferences. All weights and parameters can be programmed and readback with an SPI bus. As neuromorphic vision sensors send spikes encoding temporal contrast [24], pixels with the highest luminosity change spike first with an ON (positive delta) or OFF (negative delta) event, conveying useful data for edge detection. In order to efficiently extract this information, we use time-to-first-spike encoding (i.e. timing code) [25] in the convolutional layers, which are handled in the CONV core (Section II-A). In order to match the time constant of SPOON with the given application, time ticks can be retrieved either from an external reference pin TICK_EXT or generated internally by a configurable synchronous on-chip tick generator. Fully-connected layers are handled in the FC core (Section II-B), which uses a combination of frame-based and event-driven processing for maximum data reuse and efficient handling of DRTP updates (Section II-C).

A. Convolutional (CONV) core

The CONV core consists of a convolutional layer with 10 5×5 8-bit programmable kernels followed by a stride-4 maxpooling layer, kernels are randomly initialized upon reset. The circuit architecture is shown in Fig. 3(a). Following the dataflow highlighted in Fig. 2, convolutions are carried out in an event-driven fashion, while frame-based maxpooling is triggered before processing the fully-connected layers. Input AER events from the sensor are encoded with an 11-bit address, which covers the pixel \( \{x,y\} \) coordinates for 32×32 images and an ON/OFF polarity bit. Based on the TICK time reference and the DATA_SYNC pin that signals the start of an input sample, input events are concatenated with an 8-bit timestamp before being pushed into a 32-stage FIFO.

Event-driven convolutions follow the timing diagram of Fig. 4(a), where the 10 kernels are processed sequentially. The 9-bit timestamp, including the input event polarity bit, is first multiplied with all values in the current kernel \( i \) in a 5x5 multiplier array. The partial sums (psums) of the feature map elements associated to kernel \( i \) and input pixel \( \{x,y\} \) coordinates, stored in a 16-kB SRAM, are then updated. Due to SRAM aspect ratio constraints, this update is split in four 256-bit read/write accesses whose locations are given by an address decoder. An overflow protection mechanism emulates a hardtanh activation function. Maxpooling is automatically carried out after the FIFO has been emptied and the 8-bit timestamp counter falls to zero. It is followed by a quantization to 6 bits with configurable rescaling. The CONV core then outputs 490 6-bit activations (CONV_OUT) and a CONV_DONE trigger to enable the FC core, which is clock-gated otherwise.

Depending on the event-driven sensor use case, two features can be used to adjust the accuracy-energy tradeoff. First, the first-spike gating block can be enabled to keep only the most-informative first spike of each pixel, thus dropping subsequent events. Second, the INFER_REQ pin can be used...
to request inference at any time by triggering maxpooling before the 8-bit timestamp counter falls to zero, thus ignoring all subsequent less-informative events.

B. Fully-connected (FC) core

The FC core consists of a 128-neuron fully-connected hidden layer followed by a 10-neuron output layer, both with 8-bit programmable weights that are automatically initialized to zero for online learning (Section II-C). The circuit architecture and the associated timing diagram are shown in Figs. 3(b) and 4(b), respectively. As highlighted in Fig. 2, the hidden layer output \( y_{hid} = f_{hid}(W_{hid}x) \) is computed with a conventional frame-based approach as all the inputs are immediately available when receiving the CONV_DONE trigger, where \( W_{hid} \) represents the hidden layer weights, \( f_{hid} \) is the hidden layer activation function and \( x \) is the input from the CONV core (Fig. 5). The hidden neurons are evaluated sequentially and inputs are processed by batch of 64. It requires 8 cycles to retrieve the 500 weights associated to a hidden neuron, including both the 490 weights \( W_{hid,i} \) connecting to the inputs and the 10 weights \( W_{out,i} \) connecting to the output layer neurons, where the index \( i \) denotes hidden neuron \( i \). Once the weighted sum of inputs \( W_{hid,i}x \) of hidden neuron \( i \) has been computed, output layer processing is trigged in an event-driven fashion to ensure maximum data reuse:

- the activation \( y_{hid,i} \) is obtained by quantizing \( W_{hid,i}x \) to 3 bits with a hardtanh function, whose binary derivative is one in the linear range and zero elsewhere (HID_ACT and HID_GRAD in Fig. 3(b)),
- if the derivative is non-zero, DRTP updates can be directly applied to \( W_{hid,i} \) (Fig. 4, orange), otherwise they are skipped (Section II-C),
- \( W_{out,i} y_{hid,i} \) is added to the 10 output psums,
- as the final activation and derivative of the output neurons are not yet available for the current sample, a DRTP update of \( W_{out,i} \) is triggered based on buffered previous sample data (Section II-C).

Finally, when all the hidden neurons have been processed, the output layer activation \( y_{out} = f_{out}(W_{out} y_{hid}) \) is obtained by quantizing the output psums to 3 bits with a hardsign function, whose binary derivative is one in the linear range and zero elsewhere (OUT_ACTS and OUT_GRADS in Fig. 3(b)).

C. On-chip online training with direct random target projection (DRTP)

Building on feedback alignment techniques [26], [27], which were proposed to solve the weight transport problem of BP [22] (i.e. requirement for weight symmetry in the forward and backward pathways), we proposed in [21] the direct random target projection (DRTP) algorithm to release not only the weight transport problem, but also update locking (i.e. requirement for full forward and backward passes before the weights can be updated). As these are the two key issues that preclude BP from being hardware-efficient and biologically plausible [21], DRTP is a low-cost algorithm suitable for deployment at the edge. It relies only on feedforward and local computation (Fig. 5) and estimates the hidden layer loss gradient \( \delta y_{hid} \) as a projection of the target vector \( t^* \) (i.e. one-hot encoded labels) with a fixed random matrix \( B_{hid} \). This operation corresponds to a simple label-dependent random vector selection, which can be quantized down to binary resolutions with only a negligible impact on DRTP performance. The hidden layer weight updates \( \Delta W_{hid} \) can then be computed as

\[
\Delta W_{hid} = -\eta_{hid} (\delta y_{hid} \odot f_{hid}(W_{hid}x) T)
\]

(1)

where \( \eta_{hid} \) is the hidden layer learning rate and \( \odot \) denotes element-wise multiplication. As opposed to BP, \( \delta y_{hid} \) is always non-zero in DRTP; the weights can thus be initialized to zero without precluding training convergence. The DRTP output layer update is identical to the BP update, i.e.

\[
\Delta W_{out} = -\eta_{out} (e \odot f_{out}(W_{out} y_{hid}) T)
\]

(2)

where \( \eta_{out} \) is the output layer learning rate.

The circuit architecture for the DRTP weight update module of SPOON is shown in Fig. 6. According to Eq. (1), the derivative \( f_{hid}(\text{HID_GRAD}) \) of hidden neuron \( i \), taking values 0 or 1, can be used as an enable signal for the hidden layer update module (Section II-B). The fixed random binary matrix \( B_{hid} \) is stored in a register file. A specific bit is selected based on the current hidden layer neuron index (HID_IDX) and the training sample label (LABEL). Therefore, the only required computation is a label-dependent sign inversion to the inputs from the CONV core (HID_IN), processed by batch of 64. The
obtained values are then used as probabilities conditioning random increments/decrements to the hidden layer weights \( W_{hid,i} (W_{HID}) \), depending on the values generated by a linear feedback shift register (LFSR) and a configurable learning rate. In order to parallelize the generation of 64 12-bit seeds with a single LFSR, we applied the unfolding technique [28], similarly to the stochastic update mechanism that we proposed for the MorphIC SNN in [7].

The output layer update follows Eq. (2), whose terms are buffered so that updates from the previous sample to output layer weights \( W_{out,i} (W_{OUT}) \) can be applied concurrently with the hidden layer updates of the current sample. The error \( e \) is computed based on the previous label and output activations \( \text{OUT}_\text{ACTS} \), where the binary output derivatives \( \text{OUT}_\text{GRADS} \) act as a gating signal. If the previous hidden neuron activation is zero, updates are skipped. Otherwise, it is multiplied with the error and used in the stochastic updates array, which operates as in the hidden layer update module.

III. IMPLEMENTATION AND BENCHMARKING RESULTS

SPOON has been taped out in a 28-nm FDSOI CMOS process, the layout is presented in Fig. 7, while the specifications and pre-silicon performance metrics are reported in Table I. It occupies an area of only 0.32mm\(^2\) at 0.6V. SPOON has a leakage power of 61\(\mu\)W at 0.6V and an energy consumption of 1.7nJ/event at 0.6V. The energy for the FC core is 55nJ/inference at 0.6V. Table I. It occupies an area of only 0.32mm\(^2\) with area overheads of 16.8\% and 11.8\% compared to a design without online learning, respectively. In order to accelerate benchmarking, the accuracy results in the subsequent text were retrieved from an FPGA implementation of SPOON.

The accuracy-area-energy tradeoff on the MNIST dataset of handwritten digits [29] is shown in Fig. 8 for conventional ANN and CNN machine learning accelerators [30]–[32], the BNN from Park et al. [17], the SNN offline-trained as a BNN from Chen et al. [18], SNNs [7], [11], [15], [17] and SPOON, which requires only 313nJ and 17\(\mu\)s per inference for an area of 0.32mm\(^2\) using a time-to-first-spike encoding. Training SPOON for MNIST using an off-chip optimizer based on PyTorch [35] with quantization-aware training [36], we reach a test-set accuracy of 97.5\%. When enabling on-chip DRTP-based online learning, where the convolution kernels are initialized and fixed to random values and plastic fully-connected weights are initialized to zero, SPOON reaches a test-set accuracy of 92.8\% after one epoch and 95.3\% after 100 epochs on the 60k-sample training set. It appears from Fig. 8 that only SPOON reaches the efficiency of conventional machine learning accelerators while being compatible with event-based sensors and embedding on-chip online learning.

The neuromorphic MNIST (N-MNIST) dataset [37] is a spiking version of MNIST generated by an ATIS silicon retina [38] mounted on a pan-tilt unit and moved in three saccades. As each active pixel spikes in average 4.8 times per saccade, leading to redundant information in time-to-first-spike coding, we use the single-spike-per-pixel mode of SPOON. Using only the first saccade of each sample, SPOON reaches a test-set accuracy of 93.8\% with offline-trained weights and of 90.2\% (one epoch) or 93.0\% (100 epochs) using on-chip online training, while consuming 665nJ per inference.

IV. CONCLUSION

In this paper, we presented the SPOON event-driven CNN, following a top-down neuromorphic design approach. We demonstrate that combining event-driven and frame-based processing with weight-transport-free update-unlocked training supports low-cost adaptive edge computing. Indeed, SPOON has an accuracy-area-energy tradeoff superior to SNNs and comparable to conventional machine learning accelerators while enabling online learning with spike-based sensors.
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