Abstract. Electrical Impedance Tomography (EIT) is a non-invasive imaging method that can generate image of impedance distribution inside an object. In this imaging method, measured voltages are complex quantities that contain real and imaginary parts. To increase the accuracy of image reconstruction in EIT systems, it is necessary to utilize both real and imaginary parts of measured voltages. Phase sensitive demodulator can accurately specify the two parts of measured voltages. In this paper, a digital phase sensitive demodulator (DPSD) has been designed and implemented using a DSP board. Floating point 32-bit arithmetic with high speed of 225 MHz of the DSP core allows this digital demodulator to accurately measure real and imaginary parts of measured voltages with a desired SNR in an EIT system. This paper describes the theory and implementation of DPSD on a TMS320C6713 DSP board. Next, simulation data generated by the Code Composer Studio software and the data of an EIT phantom are applied to the DPSD. The simulation data results show a 0.12 degree phase error and a 0.37 % amplitude error with high SNR of 130.6 dB. The EIT phantom results present the 0.76 degree phase error and the 0.91 % amplitude error.

1. Introduction
Electrical impedance tomography (EIT) is a non-invasive imaging technique that provides image of impedance distribution inside an object, based on the knowledge of the applied current patterns and the measured surface voltages [1]. In this imaging method, measured voltages are complex quantities that contain real and imaginary parts. In EIT systems, a small perturbation on the boundary measured data will cause large changes in the solution of update impedance distribution resulting the image reconstruction problem is ill-posed. Therefore, boundary voltages must be measured with high accuracy. On the other hand, the number of measurements is limited; it is then necessary to utilize both real and imaginary parts of measured voltages. In other bio-impedance measurements, it is needed to accurately measure amplitudes and phases of voltages when applying current sources. In order to obtain accurate bio-impedance measurements, high precision phase sensitive demodulator is required.

Phase sensitive demodulation is a very powerful technique for accurately measuring in-phase and quadrature components of the voltage signal. The amplitude and phase of the signal can be computed from the two components. Most EIT systems use this demodulating technique for the boundary voltage measurements [2-7]. The demodulator affects the output signal to noise ratio (SNR) so it is necessary to design the demodulator with a desired SNR in an EIT system.

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2. Digital Phase Sensitive Demodulation

2.1. DSP-based DPSD Implementation

For the implementation of the Digital Phase Sensitive Demodulator, we have used a DSP board from Texas Instrument TMS320C6713 DSK. It has a 32-bit floating point DSP running at 225 MHz (TMS320C6713 Digital Signal Processor) with 16 MB of on-chip memory (static RAM). The DSK uses a Texas Instruments AIC23 (TLV320AIC23) stereo codec for input and output of signals with the following on-chip features: a. Two 16-bit ADCs and two 16-bit DACs, with a maximum sample rate of 96 kilo samples per second (ksps), b. Programmable Gain Amplifiers (PGA) and antialiasing filters for the inputs, c. Smoothing filters and programmable attenuators for the outputs. The codec communicates using two serial channels: McBSP0 is used to send commands to the codec control interface while McBSP1 is used for digital audio data. These characteristics make this codec suitable for our range of frequencies and required resolution. A schematic block diagram of the DSK board is shown in Figure 1.

![Figure 1. Block Diagram of C6713 DSK board [8].](image)

The codec has two 16-bit input channel Line in Left and Right that can operate separately. The measured voltage signal and sinusoidal reference signal convert to digital samples through two codec input channels, line in left and right, simultaneously. At first, input signals is amplified by an Programmable Gain Amplifier (PGA), to reach an acceptable level. The signals, have also passed through an antialiasing filter. Resultant signals, then convert to digital samples by means of a ADC that utilize sigma-delta technique. These samples are sent to DSP through McBSP1 channel. Sampled measured voltage signal, $V_{in}(i)$ are multiplied by reference signals. Cosine reference signal, also can be provided by a delay from sinusoidal reference signal as follows [9-11]:

$$\cos \frac{2\pi}{N} i = \sin \frac{2\pi}{N} [i + \frac{N}{4}]$$

After digitizing input analog signal and sinusoidal reference signal with a high speed and high resolution analog to digital converter, samples of measured signal are multiplied by corresponding cosine and sinusoidal reference signal samples. Then the outputs can be achieved by filtering the DC frequency. The resulting DC components at the output of the lowpass filtering stage contain the phase and amplitude information of the measured voltage. These data are saved to on-board DSP memory. Figure 2 shows a block diagram of a DSP-based DPSD.
3. Experimental Results

3.1. Emulation
To test the designed DPSD system, a reference sinusoidal signal with unit amplitude and zero initial phase and an input sinusoidal signal with an amplitude of 2000 mV and a phase delay of 30 degrees both at frequency of 24 kHz are produced in Code Composer Studio software. These signals are used as inputs of the DPSD system. The sampling frequency of the codec set to maximum value of 96 kHz. To increase the SNR, 1000 samples are used from 250 cycles (4 samples per cycles). Simulation data results, with 6 times repetition of the experiment, show a 0.12 degree average phase error and a 0.37 % amplitude error with high SNR of 130.6 dB. Table 1 shows the simulation data results of the DPSD system together with the simulation data results from a FPGA-based DPSD [12].

Table 1. The simulation data results of the demodulation system

|                  | DPSD Emulation | [12] |
|------------------|----------------|------|
| N (Samples)      | 1000           | 200  |
| Phase- Error(deg)| 0.12           | 1.03 |
| Amplitude- Error(%)| 0.37           | 3.1  |
| SNR(dB)          | 130.6          | >100 |

3.2. Phantom
The second experiment is carried on a phantom (P.V.C. cylindrical tank) with prototype circuit board and the results are sent to a PC. The phantom has 15 cm radius and 35 cm height, and 32 Ag/AgCl electrodes. It is filled with 3 % standard saline water. The four electrodes, located in the middle of side wall of the phantom, are used in the measurement. A hardware system simulator to [13] is used to generate the current source. A digital oscilloscope (GW Instek GDS-2204) is also used to compare with DPSD results. The average of measured results of DPSD, with 10 times repetition experiments, show a phase delay of 23.43 degrees and magnitude of 575.17 mV with 130.6 dB SNR. These results present a phase delay error of 0.76 degree and a magnitude error of 0.91 %. Table 2 depicts the measured results with DPSD and oscilloscope.
4. Conclusion
This paper has presented a design of a digital phase sensitive demodulator and implemented using digital signal processing technology for an EIT system. The simulation data results show a 0.12 degree phase error and a 0.37 % amplitude error with high SNR of 130.6 dB. The EIT phantom results present the 0.76 degree phase error and the 0.91 % amplitude error.

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