Run-Time Accuracy Reconfigurable Stochastic Computing for Dynamic Reliability and Power Management

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Abstract—In this paper, we propose a novel accuracy-reconfigurable stochastic computing (ARSC) framework for dynamic reliability and power management. Different than the existing stochastic computing works, where the accuracy versus power/energy trade-off is carried out in the design time, the new ARSC design can change accuracy or bit-width of the data in the run-time so that it can accommodate the long-term aging effects by slowing the system clock frequency at the cost of accuracy while maintaining the throughput of the computing. We validate the ARSC concept on a discrete cosine transformation (DCT) and inverse DCT designs for image compressing/decompressing applications, which are implemented on Xilinx Spartan-6 family XC6SLX45 platform. Experimental results show that the new design can easily mitigate the long-term aging induced effects by accuracy trade-off while maintaining the throughput of the whole computing process using simple frequency scaling. We further show that one-bit precision loss for input data, which translated to 3.44dB of the accuracy loss in term of Peak Signal to Noise Ratio for images, we can sufficiently compensate the NBTI induced aging effects in 10 years while maintaining the pre-aging computing throughput of 7.19 frames per second. At the same time, we can save 74% power consumption by 10.67dB of accuracy loss. The proposed ARSC computing framework also allows much aggressive frequency scaling, which can lead to order of magnitude power savings compared to the traditional dynamic voltage and frequency scaling (DVFS) techniques.

I. INTRODUCTION

One of the important paradigm changes for today’s emerging computing workloads such as deep learning, AI, computer vision, imaging and audio processing is that accurate computing becomes less important as those applications are much more error tolerant with analog-like outputs for human interaction. As a result, accuracy can be traded off to improve hardware footprint, power/energy efficiencies via so-called approximation computing. One important approach for approximate computing is by means of stochastic computing (SC), in which the value is presented as the signal probability in a bit stream. Approximation computing. One important approach for approximate computing is by means of stochastic computing (SC), in which the value is presented as the signal probability in a bit stream. Approximation computing. One important approach for approximate computing is by means of stochastic computing (SC), in which the value is presented as the signal probability in a bit stream.

Fig. 1: The maximum working frequency decreases over years because of aging.

On the other hand, stochastic computing has been emerging as a new computing paradigm due to its low-cost and error-resilient features. One of the major benefits for SC is that many arithmetic operations such as multiplication can be simply implemented by AND operation (or XNOR gate for bipolar). SC has been applied to error-correcting codes [8], image processing [9], and recently deep neural networks (DNNs) [10]–[13].

Traditional SC, however, suffers long computing time and high randomness of the stochastic numbers for accuracy. As a result, many research works have been proposed to mitigate those shortcomings such as high-quality random number generators (RNGs) that exhibit zero or close to zero correlation, including low-discrepancy sequences [14], bit scrambling methods [15], [16]. Recently, a more efficient and also accurate SC multiplier was proposed to partially mitigate the two mentioned problems in the traditional SC [12]. Instead of using an AND gate for the multiplication of two bit-streams, the new multiplier essentially counts the one in one bit-stream based on the value of another bit-stream. Further more, the bit-stream to be counted can be generated in a deterministic way. As a result, the whole design is simplified into two counters and a simple bit-stream generator. In this work, we call this design counter-based SC multiplier (CBSC-Multiplier). CBSC-Multiplier brings two important benefits: first, it does not require the randomness of the two bit streams anymore without loss of accuracy. Second, it can be faster than traditional SC as it drops the requirement of counting all bits in a bit-stream.

Based on those observations, in this paper, we propose a new accuracy-reconfigurable stochastic computing (ARSC) technique for dynamic long-term reliability management and more power efficient computing. It leverages the latest CBSC computing frameworks for more energy-efficient SC implementation. Different than existing stochastic computing works, where the accuracy versus power/energy trade-off is carried out in the design time, the new stochastic computing can change accuracy or bit-width of the data in the run-time so
that it can accommodate the long-term aging effects by slowing the system clock frequencies at the cost of accuracy while maintaining the throughput of the computing. As many emerging workloads are error tolerant, the new accuracy-reconfigurable stochastic computing essentially provides viable solution to mitigate the challenging long-term reliability problems due to the increasing degradation effects such as biased temperature instability (BTI) and electromigration (EM) as technology advances. Further more, the proposed reconfigurable SC method can provide new knob to dynamically regulate the active power of a chip as one can scale the frequency in much larger range (compared to traditional voltage and frequency scaling techniques) to trade the accuracy for power in a progressive way.

We validate the ARSC concept on a discrete cosine transformation (DCT) and inverse DCT designs for image compressing/decompressing applications, which are implemented on Xilinx Spartan-6 family XC6SLX45 platform. Experimental results shows that the new design can easily mitigate the long-term aging induced effects by accuracy trade-off while maintaining the throughput of the whole computing process using simple frequency scaling. We further show that one-bit precision loss for input data, which translated to 3.44dB of the accuracy loss in term of Peak Signal to Noise Ratio for images, we can sufficiently compensate the NBTI induced aging effects in 10 years while maintaining the pre-aging computing throughput of 7.19 frames per-second. At the same time, we can save 74% power consumption by 10.67dB of accuracy loss. The proposed ARSC computing framework also allows much aggressive frequency scaling, which can lead to order of magnitude power savings compared to the traditional dynamic voltage and frequency scaling (DVFS) techniques.

II. REVIEW OF STOCHASTIC COMPUTING

Stochastic computing (SC) provides an alternative way for arithmetic computing when the exact results are not required. At the same time, the SC based hardware can be designed with extremely low cost and low power than traditional binary digital designs.

A. Conventional stochastic computing:

Fig. 2 shows the conventional stochastic computing (SC) multiplier, where the number or stochastic number, SN, is represented by a bitstream, whose signal probability, or frequency of ‘1’, determines its value. Naturally, the value is defined in the range $[0, 1]$, called unipolar, or over $[-1, 1]$ called bipolar. For instance, Fig. 2, the number $X$ represents $4/8$ as we have four ‘1’ in the 8-bit bitstream. One of the major benefits for SC is that the multiplication can be simply implemented by AND operation as shown in this figure.

$$x = \frac{3}{8}, y = \frac{2}{3}, z = \frac{1}{2}$$

Fig. 2: Traditional SC number and multiplier.

To generate the random number for SC, stochastic number generator, SNG, which essentially converts binary number to stochastic number, takes $n$-bit binary number and generates the random bitstream as shown in the bottom part of Fig. 3. SNG typically is implemented by $n$-bit linear feedback shift register (LFSR) and $n$-bit comparator, which generates ‘1’ if the random number is less than the input binary number, and ’0’ otherwise.

For stochastic computing unipolar encoding, the multiplication can be done by AND gate and for bipolar encoding, the multiplication is achieved by XNOR operation. Finally, the addition can be simply done by a multiplexer (MUX) or up-down counter for bipolar coding.

Due to its simple hardware implementation compared to the common arithmetic operations, SC is very low-cost and energy efficient. But the traditional SC, however, suffers from long latency and inherent random fluctuation errors, which are mitigated by the recently proposed binary interfaced stochastic computing method mentioned below.

B. Counter-based SC multiplication

Assume the bit width is $n$ for the given two binary numbers $x$ and $w$. The conventional SC multiplier using AND gate (for unipolar encoding) will take $2^n$, which is the length of bit-stream of stochastic number (SN), cycles to finish the work. To improve this, Sim et al. in [12] proposed a counter-based SC multiplier design shown in Fig. 3. The multiplier mainly consists of two counters.

The down counter counts the binary value of the input $w$ and the up counter counts the result $x \cdot w$. So the operation only takes $w \cdot 2^n$ cycles to finish. One example is given in Fig. 4. More importantly, the stochastic number of input $x$ can be generated in a deterministic way without hurting the accuracy (actually more accurate). As a result, such design is more simple as we eliminate the two traditional stochastic number generators or SNGs (typically using Linear Feedback Shift Registers) and AND gates in exchange of a down-counter, which is much cheaper than SNG.

III. PROPOSED RUN-TIME ARSC FOR 2D DCT/IDCT

In this section, we present the proposed accuracy-reconfigurable stochastic computing (ARSC) method based on the counter-based SC framework. The key idea is to dynamically adjust the bit-width of the coming data for multiplication intensive computing so that we can reduce the accuracy of the computing progressively using SC. At the same time, we also reduce effective latency of the computing logic so that we can compensate aging-induced delay increases. Since we reduce effective latency of computing logic, we can reduce the frequency while still being able to maintain the same throughput of the whole computing process as required by the application.

We will illustrate the proposed ARSC method using an image compression application based on computing intensive 2D discrete cosine transformation, DCT and inverse DCT algorithms.
We first briefly review DCT and IDCT computing processes. 2D discrete cosine transform (DCT) filter is an effective method for eliminating high-frequency noise, by transforming the image data into spatial frequency domain, masking the high-frequency components, and then transforming back to the original space domain. A 2D DCT consists of two separate 1D DCT operations, which can be denoted as

$$f_k = a_0 \sqrt{N} + \sqrt{\frac{2}{N}} \sum_{i=1}^{N-1} a_i \cos \left( \frac{(2i + 1)k\pi}{2N} \right), \quad 0 \leq k < N,$$

where vector \(\{a_i\}\) is the original data, and \(\{f_k\}\) is the result of 1D DCT. A 2D DCT is completed by applying 1D DCT on each column and then on each row of the matrix. With the image data \(T(x, y)\) transformed into its 2D frequency domain \(F(x, y)\), a filtered frequency map \(\mathcal{F}(x, y)\) can be obtained by applying a mask

$$\mathcal{F}(x, y) = F(x, y)m(x, y),$$

where \(m(x, y)\) is the mask map valued 0 at high frequencies and 1 at low frequencies. The filtered data \(T(x, y)\) is then obtained by taking the inverse 2D DCT on the filtered frequency map \(\mathcal{F}(x, y)\). Similar to its forward counterpart, the inverse 2D DCT consists of two separate inverse 1D DCT steps on the rows and columns respectively. The inverse 1D transformation of \(f\) is

$$a_i = \frac{f_0}{\sqrt{N}} + \sqrt{\frac{2}{N}} \sum_{k=1}^{N-1} f_k \cos \left( \frac{(2i+1)k\pi}{2N} \right), \quad 0 \leq i < N.$$

As we can observe, the primary computing in the 2D DCT/IDCT algorithms are essentially multiply-accumulate operation (MAC).

A. ARSC architecture for the 2D DCT/IDCT

Fig. 4 shows the proposed ARSC-based MAC unit used in the DCT/IDCT applications.

The ARSC MAC unit includes the input data truncation/reconfiguration block, the multipliers and the adder block. We use the counter-based SC multiplier to realize SC multiplication as shown in Fig. 4. The proposed ARSC module does the dynamic accuracy arrangement by adjusting the bit width of the input data that participate in the counter-based SC multiplier in the ARSC MAC unit, which is realized by the data truncation block. For instance, when the initial data is \(m\)-bit, represented in signed-and-magnitude form, \(X_{i,1}, (i = 1, 2, \ldots, N)\) in Fig 5. In this line, an \(x\)-bit accuracy selection signal \(SEL\) is used to tell the truncation block how many bits it needs to keep. In our design, for instance, we have 5 states representing from 10-bit to 6-bit configurations, so \(x=3\) will be enough to distinguish the 5 states. After data truncation, \(X_{i,1}\) is transformed to \(X_{i,1}^\prime\), which is an truncated \(\alpha\)-bit binary number. Fig. 6 illustrate how the data truncation block works. Notice that we keep the sign bit, and truncate the least significant bits from the right side, which is compatible with the bit-width based progressive SC computing scheme.

After the ARSC MAC process finishes, we will add 0 at the end of the output number to make it the same bit width as the input binary number to keep bit-width compatibility between different computing modules. As SC computing time is directly proportional to the bit-width, or more precisely proportional to \(O(2^{bitwidth})\), one bit-width reduction can dramatically reduce the SC computing time by half, which can be very effective for mitigate the aging effects.

Notice that our counter-based SC multiplier only deals with unipolar number multiplication, whose range in \([0, 1]\). We keep the sign bits for all the DCT coefficients \(C_i\) (\(i = 1, 2, \ldots, N\)). The sign bit of \(C_i\) and the sign bit of \(X_{i,1}^\prime\) will perform an \(XOR\) operation to determine whether the product obtained from the counter-based SC multiplier is positive or negative before participating in the add operation which is carried out at the adder block.

![Fig. 5: The proposed ARSC-based MAC unit](image)

![Fig. 6: Data truncation example](image)
synthesized using Xilinx ISE 14.7 for XC6SLX45 device of Spartan-6 family. Different from the ASIC-based module, FPGA mainly use the LUT-based operations [18]. So for the design area measurement, we simply count the number of LUTs after the module is synthesized. As mentioned in Sec. III, the design totally utilizes 17569 LUTs to support the parallel SC blocks. We show the details of the FPGA hardware resource utilization information in Table I. To evaluate the power consumption, we use the Xilinx Power Estimator downloaded from the official website, which can easily obtain the total power consumption. We’ll discuss the power consumption of the design later in Sec. V. For the delay measurement, we obtain the critical path of the ARSC design from the Xilinx ISE 14.7 timing summary after the design is synthesized, showing that the hardware delay, which is calculated from the worst case critical path, is 11.348ns. It means that the highest frequency the ARSC design can run is 88.1M. Since we use the digital clock manager (DCM) IP of Xilinx ISE 14.7 to generate the clock signal and the input system clock of the DCM is 100M for the Spartan-6 family boards. The highest frequency DCM can output is 85.7M. So we choose this frequency to be the initial global clock signal of the ARSC design.

V. EXPERIMENTAL RESULTS AND DISCUSSION

In this section, we present results from the proposed ARSC computing method for the aging mitigation. The proposed ARSC DCT/IDCT image compression algorithms were implemented on the Xilinx XC6SLX45 FPGA platform.

We first show the image compression results with different accuracy in Fig. 8(a). The Fig. 8(b) shows the original figure without any compression. And Fig. 8(c) to Fig. 8(f) show the image quality after the DCT/IDCT sequence computing with different accuracy, from 10-bit to 6-bit. We use PSNR (Peak Signal to Noise Ratio) to evaluate the accuracy of the image compressing/decompressing process, which is shown in Table II.

If we consider the NBTI induced aging process, which causes the chip frequency going down over time due to the increased threshold voltage. To measure the amount of frequency decrease, we use the time dependent degradation aware Nangate 45nm standard cell library from Karlsruhe Institute of Technology (KIT) [32] to calculate the chip frequency after 10 years. We use Synopsys design suite to synthesize the ARSC-based DCT/IDCT design. The timing analysis shows that frequency of the ASIC-based design of DCT/IDCT will decrease from 1205M to 1064M, as shown in Fig. 8. To simulate the aging process by FPGA, we simply adjust the frequency output from the DCM by the same ratio, which is 85.7M to 75.7M (we note that such mapping may not be perfect as the design technologies used in our ASIC and FPGA are different). For the DCT/IDCT process, the aging effect directly affect the throughput. The time of the whole process, including both of the DCT and IDCT process, is used to calculate the throughput.

We show that the throughput with different precision at different clock frequencies in Fig. 9. The x-axis is the bit width we use in the stochastic multiplication when we perform the DCT/IDCT computing. The y-axis is the throughput, meaning the number of operations per second.
| Bit Width | Frequency (MHz) | Power (W) | PSNR (dB) | Latency (s) |
|-----------|----------------|-----------|-----------|-------------|
| 10        | 85.7           | 0.292     | 38.12     | 0.139       |
| 9         | 43.8           | 0.177     | 34.68     | 0.071       |
| 8         | 22.9           | 0.120     | 31.27     | 0.037       |
| 7         | 12.4           | 0.092     | 28.70     | 0.020       |
| 6         | 7.1            | 0.077     | 27.45     | 0.012       |

TABLE II: Key performance metric comparison under the same throughput.

images the design can deal with per second. Fig. 9 also shows the throughput of 7.19 images per second for different frequencies and precision with the dashed black line. As we can see, initially (when the aging process hasn’t started yet), if we use the full 10-bit precision, the throughput at 85.7 MHz clock frequency is 7.19. When the clock frequency decreases to 43.8 MHz, we can still keep the same throughput if we truncate the precision by only one bit (from 10 to 9). Due to the aging process, the throughput will decrease to 6.35. If we degrade the precision by one bit (9-bit), the throughput will increase to 12.42, which obviously, is larger than the initial throughput. The red line of dashes in Fig. 9 shows this very clearly. And, by decreasing the precision of SC multiplication to 6-bit, the throughput will be about 12 times of the 10-bit precision, which shows huge space we can mitigate the aging effects if such accuracy is still accepted in practical applications.

Due to the difficulty of obtaining the hardware delay of the scenarios in which the data bit width is not 10-bit during SC computing process, we use the effective latency to evaluate the timing performance of our design. The effective latency of the ARSC design is actually the inverse of the throughput, since it represents the time interval between the input and the output. We show the latency at the 5th column of Table II.

From Table II, we observe that our design can do the dynamic power management by adjusting the working frequency as well. By doing the trade-off between the throughput and the accuracy mentioned before, we can keep the throughput by sacrificing accuracy when the frequency is cut down due to some low power consumption requirement situation. For example, if we want to keep the throughput as 7.19 here, when the power goes down, the frequency of the ARSC design will also decrease. Thus, the precision (bit width) of the data our proposed ARSC design can work will also decrease. We show this clearly in Fig. 10. We notice that we can save near 74% of power consumption by sacrificing 10.67 dB of the accuracy loss. We also observed that the proposed ARSC computing framework allows much aggressive frequency scaling, which can lead to order of magnitude power savings compared to the traditional dynamic voltage and frequency scaling (DVFS) techniques.

VI. Conclusion

In this paper, we have proposed a novel accuracy-reconfigurable stochastic computing (ARSC) framework for dynamic reliability and power management. The new ARSC design can dynamically change accuracy via bit-width change of the data. In this way, the new method can accommodate the long-term aging effects by slowing the system clock frequency at the cost of accuracy while maintaining the throughput of the computing. We designed and validated the ARSC-based discrete cosine transformation (DCT) and inverse DCT designs for image compressing/decompressing applications on the Xilinx Spartan-6 family XC6SLX45 platform. Experimental results show that one can easily mitigate the long-term aging effects by accuracy reduction while maintaining the throughput of the whole computing process using simple frequency scaling. In our example, we show that one-bit precision loss for the input data, which translated to 3.44 dB of the accuracy loss in term of Peak Signal to Noise Ratio (PSNR) for images, one can sufficiently compensate the NBTI induced aging effects in 10 years while maintaining the pre-aging computing throughput of 7.19 frames per second. At the same time, one can save 74% power consumption by 10.67 dB of accuracy loss. The proposed ARSC computing framework allows much aggressive frequency scaling, which can lead to order of magnitude power savings compared to the traditional dynamic voltage and frequency scaling (DVFS) techniques.

REFERENCES

[1] A. Alaghi, W. Qian, and J. P. Hayes, “The promise and challenge of stochastic computing,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 37, no. 8, pp. 1515–1531, 2018.
[2] “Failure Mechanisms and Models for Semiconductor Devices.” In JEDEC Publication JEP122-A, Jedecl Solid State Technology Association, 2002.
[3] “Critical Reliability Challenges for The International Technology Roadmap for Semiconductors (ITRS),” 2003. In International Sematech Technology Transfer Document (3024377A-TR), 2003.
[4] “Degradation-aware cell libraries,” vol.1.0. [http://ces.itec.kit.edu/dependable-hardware.php]
[5] S. X.-D. Tan, H. Aminouch, T. Kim, Z. Sun, C. Cook, and J. Henkel, “Recent advances in EM and BTI induced reliability modeling, analysis and optimization,” Integration, the VLSI Journal, vol. 60, pp. 152–152, Jan. 2018.
[6] S. X.-D. Tan, M. Tahoori, T. Kim, S. Wang, Z. Sun, and S. Kiamehr, VLSI Systems Long-Term Reliability – Modeling, Simulation and Optimization. Springer Publishing, 2019.
[7] H. Aminouch, B. Khaleghi, A. Gerstlauer, and J. Henkel, “Towards aging-induced approximations,” in Proceedings of the 54th Annual Design Automation Conference 2017, pp. 1–6, 2017.
[8] A. Naderi, S. Mannor, M. Savan, and W. J. Gross, “Delayed stochastic decoding of ldpc codes,” IEEE Transactions on Signal Processing, vol. 59, no. 11, pp. 5617–5626, 2011.
[9] P. Li, D. J. Lilja, W. Qian, K. Bazargan, and M. D. Riedel, “Computation on stochastic bit streams digital image processing case studies,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 3, pp. 449–462, 2013.
[10] K. Kim, J. Kim, J. Yu, J. Seo, J. Lee, and K. Choi, “Dynamic energy-accuracy trade-off using stochastic computing in deep neural networks,” in 2016 53nd ACM/EDAC/IEEE Design Automation Conference (DAC), pp. 1–6, IEEE, 2016.
[11] H. Sim, D. Nguyen, J. Lee, and K. Choi, “Scalable stochastic-computing accelerator for convolutional neural networks,” in 2017 22nd Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 696–701, IEEE, 2017.
[12] H. Sim and J. Lee, “A new stochastic computing multiplier with application to deep convolutional neural networks,” in 2017 54th ACM/EDAC/IEEE Design Automation Conference (DAC), pp. 1–6, IEEE, 2017.
[13] R. Hojabr, K. Givaki, S. Tayarani, P. Esfahanian, A. Khonsari, D. Rahmati, and M. H. Najafi, “Skippyn: An embedded stochastic-computing accelerator for convolutional neural networks,” in Proceedings of the 56th Annual Design Automation Conference 2019, p. 132, ACM, 2019.
[14] S. Liu and J. Han, “Energy efficient stochastic computing with sobol sequences,” in Proceedings of the Conference on Design, Automation & Test in Europe, pp. 650–653, European Design and Automation Association, 2017.
[15] F. Neugebauer, I. Polian, and J. P. Hayes, “Building a better random number generator for stochastic computing,” in 2017 Euromicro Conference on Digital System Design (DSD), pp. 1–8, IEEE, 2017.
[16] K. Kim, J. Lee, and K. Choi, “An energy-efficient random number generator for stochastic circuits,” in 2016 21st Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 256–261, IEEE, 2016.
[17] B. R. Gaines, “Stochastic computing,” in Advances in information systems science, pp. 37–172, Springer, 1969.
[18] Y. Guo, H. Sun, and S. Kimura, “Small-area and low-power fpga-based multipliers using approximate elementary modules,” in 2012 5th Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 599–604, IEEE, 2020.