Quantum Transport in 40-nm MOSFETs at Deep-Cryogenic Temperatures

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Abstract—In this letter, we characterize the electrical properties of commercial bulk 40-nm MOSFETs at room and deep cryogenic temperatures, with a focus on quantum information processing (QIP) applications. At 50 mK, the devices operate as classical FETs or quantum dot devices when either a high or low drain bias is applied, respectively. The operation in classical regime shows improved transconductance and subthreshold slope with respect to 300 K. In the quantum regime, all measured devices show Coulomb blockade. This is explained by the formation of quantum dots in the channel, for which a model is proposed. The variability in parameters, important for quantum computing scaling, is also quantified. Our results show that bulk 40-nm node MOSFETs can be readily used for the co-integration of cryo-CMOS classical-quantum circuits at deep cryogenic temperatures and that the variability approaches the uniformity requirements to enable shared control.

Index Terms—MOSFET, quantum dot (QD), Coulomb blockade, cryogenic temperature, quantum information processing (QIP).

I. INTRODUCTION

Silicon-based electronics has shown great potential as a platform for quantum information technology [1]. From a physics perspective, single-electron spins can be confined in gate-defined quantum dots (QDs) to realize qubits [2]–[4], which can provide long coherence times and be operated close to fault-tolerance fidelity levels [5], [6], and elevated temperatures [7], [8]. From a technological perspective, QDs can be manufactured in a similar fashion to field-effect transistors (FETs) [9], [10] with a small footprint (100 × 100 nm²). This gives the opportunity to leverage very large scale integration (VLSI) techniques to scale up the technology beyond state-of-the-art 2-qubit processors [6], [11]–[13] to two-dimensional QD arrays [14], [15], a requirement for fault-tolerant quantum computing [16].

II. EXPERIMENT

We study bulk MOSFETs in a commercial 40-nm process. The devices under test (DUT) are planar n-type low threshold voltage FETs with gate length $L_g = 40$ nm and gate width $W_g = 120$ nm. We characterize charge transport at 300 K and 50 mK in a dilution refrigerator (Oxford Instruments Triton). The drain voltage $V_{ds}$, gate voltage $V_g$, and drain current $I_d$ are applied and measured by a parameter analyzer (HP 4156A). We extract classical parameters such as threshold voltage $V_{th}$, subthreshold slope $SS$, transconductance $g_m$, and drain induced barrier lowering (DIBL) from a standard $I - V$ measurement. We measure the Coulomb blockade parameters such as charging energy $E_C$, lever arm $\alpha$ and source-drain capacitance ratio $C_s/C_d$ from a stability map (Coulomb diamonds) at low drain
Coulomb diamonds (Fig. 2(a)) are observed, but also devices with quasi-periodic blockade oscillations are observed in all DUTs in this letter. However, we notice that not only devices with quasi-periodic Coulomb diamonds (Fig. 2(a)) are observed, but also devices with irregular Coulomb diamonds (Fig. 2(b)), suggesting a double or multiple QD system.

For the single QD case, the full set of capacitances, the gate, source and drain capacitances, can be extracted from a Coulomb diamond diagram as in Fig. 2(a). The charging energy is $E_C = \frac{e^2}{2\epsilon}$, where $C_{\Sigma}$ is the total capacitance to the quantum dot, namely $C_{\Sigma} = C_g + C_s + C_d$. We find $E_C = 18.4$ meV, indicating that Coulomb oscillations should still be observable up to liquid helium temperature as $E_C \gg k_B T$ at 4.2 K. This has also been confirmed by measurement. The capacitance between the gate and QD can be expressed as $C_g = C_{\Sigma} - C_d$, where $\Delta V_g$ is the gate voltage separation between adjacent Coulomb peaks. We find $C_g = 5.34$ aF, corresponding to a QD with an equivalent diameter of 14.7 ± 0.7 nm, which suggests that by reducing the channel width, for instance using 28-nm node, the probability of forming multiple QDs can be lowered. The capacitances between $QD$/$Source$ ($C_g$) and $QD$/$Drain$ ($C_d$) can be estimated from the slopes of the Coulomb diamond’s boundaries as

$$C_g \approx \frac{e^2}{2\epsilon_0 \pi r^2},$$

where $\epsilon_0$ and $\epsilon_1$ are SiO2 permittivity and vacuum permittivity, respectively, $r$ is the radius of quantum dot disc and the separation between the gate electrode and quantum dot disc ($EOT=\epsilon_0 L$) is 1.2 nm is used based on $ITRS$ 2001 and $ITRS$ 2003.

### TABLE I

| Temperature  | 300 K | 50 mK |
|--------------|-------|-------|
| $V_{th}$ (V) | 0.1   | 1.0   |
| $V_{in}$ (V) | 0.388±0.030 | 0.442±0.036 |
| $SS$ (mV/dec) | 86.41±2.43 | 86.88±1.69 |
| $g_m$ (µS) | 21.48±1.79 | 118.07±7.48 |
| $\Delta V_g$ (V) | 0.126±0.017 | 0.067±0.011 |
| DIBL (mV/V) | 162.22±27.85 | 113.33±24.67 |
| $V_{th}$ (mV) | 0.488±0.039 | 0.588±0.111 |
| $C_g/C_d$ | 1.265±0.754 |  |
QD2

DUT to DUT. A small gate control voltage variation,

\( V_{g,1st} \)

statistical characterization of our analysis to the first Coulomb oscillation, we obtain a edge. Surface roughness and remote charges in the gate stack performed in the voltage region close to the conduction band the origin of Coulomb blockade since our measurements are out the implantation and activation annealing processes. Also, we rule

indicated in Fig. 2(a): \( C_s = \frac{C_0}{m_1} \) and \( C_d = \frac{C_0(1-m_2)}{m_2} \). Thus,

\[
\frac{C_s}{C_d} = \frac{-m_2}{m_1(1-m_2)}. \tag{1}
\]

And finally, we define the gate lever arm

\[
\alpha = \frac{\Delta V_{ds}}{\Delta V_g} = \frac{C_g}{C_{\Sigma}}. \tag{2}
\]

For multi-QD systems, as in Fig. 2(b), the measured \( I_d \) is a result of multiple parallel paths: (i) Source-QD1-\( V_{g,1st} \)-Drain; (ii) Source-QD2-\( V_{g,1st} \)-Drain; (iii) Source-QD1-QD2-\( V_{g,1st} \)-Drain as in Fig. 4(a), and hence it is not possible to extract the full set of capacitances. However, by restricting our analysis to the first Coulomb oscillation, we obtain a statistical characterization of \( V_{g,1st} \), the voltage where the first Coulomb oscillation occurs (Fig. 1(d), \( \alpha \) and the \( C_s/C_d \) ratio across the die (Fig. 3). We find a fairly consistent \( V_{g,1st} = 0.488 \pm 0.039 \) V, suggesting a small variation from DUT to DUT. A small gate control voltage variation, \( \Delta V_g < \Delta V_{g,1st} \), is essential for quantum computing requiring shared control schemes [25]. We find that the DUTs approach this requirement, but further variability reduction is still necessary.

For the lever arm, we find \( \alpha = 0.6 \pm 0.1 \) eV/V (Fig. 3(b)), a value comparable larger than other planar quantum dot devices [30]–[32] and just below those reported for 3D geometries [33]. Large \( \alpha \) is essential in dispersive readout schemes [18], [26], [27], [33] and 40-nm bulk MOSFETs should provide a good platform. Finally, the \( C_s/C_d \) ratio can be used for estimating the location of QD in the channel, since in general the capacitance is inversely proportional to the separation between two conductors. \( C_s/C_d \) of all DUTs is summarized in Fig. 3(c), and the result suggests that the QDs tend to locate well centered in the channel with good reproducibility and an average deviation of 0.2 \( \pm \) 6.5 nm from the center. Therefore, we conclude that the QDs are formed from the charge carrier accumulation due to the applied gate bias rather than from the dopants close to Source and/or Drain diffused during the implantation and activation annealing processes. Also, we rule out the p-type dopants in the body of the n-MOSFET as the origin of Coulomb blockade since our measurements are performed in the voltage region close to the conduction band edge. Surface roughness and remote charges in the gate stack may as well contribute to the formation of the dots [34], [35]. With all these considerations in mind we depict a to-scale schematic of how Coulomb blockade transport occurs in 40-nm bulk MOSFETs, see Fig. 4.

IV. CONCLUSION

This letter presents a statistical characterization of 18 commercial 40-nm MOSFETs at room and deep-cryogenic temperatures (50 mK). DUTs behave as classical MOSFETs at 300 K and at 50 mK under high bias, with improved performance. At 50 mK under low bias, observed Coulomb oscillations indicate that QD systems are formed in the channel in the subthreshold region. We have statistically characterized the properties of the QD systems, such as \( V_{g,1st} \), gate coupling parameter \( \alpha \), and dot-to-electrode capacitances \( C_g \), \( C_s \) and \( C_d \), and found that these devices could be a useful resource for large-scale QIP given their low variability, planar geometry and high \( \alpha \). Our results suggest that 40-nm MOSFETs can be used to build both classical circuits and quantum circuits or to co-integrate the two into quantum-classical hybrids at liquid helium temperatures and below.

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