21st Century Computer Architecture
CGO/HPCA/PPoPP 2014 Keynote

Mark D. Hill
Computer Sciences Department
University of Wisconsin-Madison
markhill@cs.wisc.edu

Abstract

This talk has two parts. The first part will discuss possible directions for computer architecture research, including architecture as infrastructure, energy first, impact of new technologies, and cross-layer opportunities. This part is based on a 2012 Computing Community Consortium (CCC) whitepaper effort led by Hill, as well as other recent National Academy and ISAT studies. See: http://cra.org/ccc/docs/init/21stcenturyarchitecturewhitepaper.pdf

The second part of the talk will discuss one or more examples of cross-layer research advocated in the first part. For example, our analysis shows that many “big-memory” server workloads, such as databases, in-memory caches, and graph analytics, pay a high cost for page-based virtual memory: up to 50% of execution time wasted. Via small changes to the operating system (Linux) and hardware (x86-64 MMU), this work reduces execution time these workloads waste to less than 0.5%. The key idea is to map part of a process’s linear virtual address space with a new incarnation of segmentation, while providing compatibility by mapping the rest of the virtual address space with paging.

Categories and Subject Descriptors  C. [Computer Systems Organization], D. [Software].

General Terms  Algorithms, Measurement, Performance, Design, Economics, Reliability, Security, Languages, Verification.

Keywords  computer systems; architecture; programming methods; performance; energy; new technology.

Biography

Mark D. Hill (http://www.cs.wisc.edu/~markhill) is the Gene M. Amdahl Professor of Computer Sciences and Electrical & Computer Engineering at the University of Wisconsin–Madison, where he also co-leads the Wisconsin Multifacet project. His research interests include parallel computer system design, memory system design, computer simulation, and transactional memory. He earned a PhD from University of California, Berkeley. He is an ACM Fellow, a Fellow of the IEEE, co-inventor on 30+ patents, and ACM SIGARCH Distinguished Service Award recipient. His accomplishments include teaching more than 1000 students, having 40 Ph.D. progeny so far, developing the 3C cache miss taxonomy (compulsory, capacity, and conflict), and co-developing "sequential consistency for data-race free" that serves as a foundation of the C++ and Java memory models.