TurboTransformers: An Efficient GPU Serving System For Transformer Models

Jiarui Fang, Yang Yu, Chengduo Zhao, Jie Zhou
Pattern Recognition Center, Wechat AI, Tencent Inc
Beijing, China
{jiaruifang, josephyu, chengduozhao, withtomzhou}@tencent.com

Abstract

The transformer is the most critical algorithm innovation of the Nature Language Processing (NLP) field in recent years. Unlike the RNN models, transformers are able to process on dimensions of sequence lengths in parallel, therefore leads to better accuracy on long sequences. However, efficient deployments of them for online services in data centers equipped with GPUs are not easy. First, more computation introduced by transformer structures makes it more challenging to meet the latency and throughput constraints of serving. Second, NLP tasks take in sentences of variable length. The variability of input dimensions brings a severe problem to efficient memory management and serving optimization.

To solve the above challenges, this paper designed a transformer serving system called TurboTransformers, which consists of a computing runtime and a serving framework. Three innovative features make it stand out from other similar works. An efficient parallel algorithm is proposed for GPU-based batch reduction operations, like Softmax and LayerNorm, which are major hot spots besides BLAS routines. A memory allocation algorithm, which better balances the memory footprint and allocation/free efficiency, is designed for variable-length input situations. A serving framework equipped with a new batching scheduler using dynamic programming achieves the optimal throughput on variable-length requests. The system can achieve the state-of-the-art transformer model serving performance on GPU platforms and can be seamlessly integrated into your PyTorch code with a few lines of code.

Keywords: Transformers, Deep Learning Runtime, Serving System, GPU

1 Introduction

The recent success of Nature Language Processing (NLP) techniques is enabled largely by the transformer-based Deep Learning (DL) models, such as Seq2seq [28], BERT [7], GPT2 [24], and XLNet [29], ALBERT [14]. With the support of the attention mechanism, the transformer models can capture long-range dependency in long sequences. In data centers, GPU has proven to be the most effective hardware for deploying deep learning (DL) services. The DL service accepts network requests and performs inference computation by performing a feed-forward pass on the model. Although there are mature solutions for CNN and RNN services, deploying transformer services with low latency and high throughput on GPU still faces two critical challenges.

Despite their success in model accuracy, transformer models are notorious for the massive amount of computation. For the inference of a 40 words sequence, the base BERT model requires 6.9 Gflops. To translate a 20 words sentence from Chinese to English, a typical Seq2seq may model requires around 20 Gflops. In comparison, for the inference of a 3x224x224 image, the ResNet50 [11], GoogleNet [27] and AlexNet [13] require 3.9, 1.6 and 0.7 Gflops, respectively. Generally, transformer models lead to more computations than previous DNN models.

Besides enhanced computation requirement, transformer models introduced the problem of variable-length input, where intermediate tensor dimensions have to change according to the input sequence length during a serving process. Although also facing at variable-length input, RNN-based models, like LSTM [12] and GRU [4], split the variable-length input into multiple fixed-length inputs and execute them sequentially. Unlike models with fixed-length input, transformer models cannot benefit from pre-optimization of memory space allocated for intermediate tensors with known lengths, resulting in memory optimization challenges. In addition, due to variable-length input, the optimization of the serving framework becomes more complicated. Conventional serving frameworks take advantage of batching techniques to increase GPU execution efficiency. Extra computations brought by zero-padding of short requests in a batch of variable-length requests often conflict with the performance gains of batching computing.

Existing online serving solutions are not able to resolve both the large computation demand and the variable-length input issues, especially the latter one. The deficiencies can be summarized from the three following aspects. First, directly employing a training framework, such as TensorFlow [1] or PyTorch [22], on inference tasks is not able to fully utilize the hardware resources. Inference differs from training in a way that it does not perform backward propagations which require extra memory space for intermediate tensors and eliminate the opportunity for operator fusion. Second, currently existing DL inference frameworks such as onnxruntime [18], TensorFlow XLA [10], TVM [3], tensorRT [21] use techniques

A preprint version, 2020

2020.
designed for fixed-length input workloads and have insufficient capability in dealing with variable-length input. Most of these current frameworks need a time-consuming preprocessing step to tune the computation pattern and memory usage of the model operators according to their pre-determined input dimension. In order to work with transformer models, they usually convert variable-length requests into fixed-length requests through zero paddings, which not only introduces additional computational overhead but also limits the maximum length allowed to the pre-determined value. Few of the current frameworks (i.e. onnxruntime [18]) can handle variable-length input, but there is still some distance from the ultimate performance for the transformer model. Third, none of the existing solutions have investigated serving optimization for variable-length input workloads. The request batching, which is the technique most helpful for performance, adopted in modern serving systems, such as TF-serving [9], Clipper [5], Nexus [26], are suitable for only fixed-length input.

To solve the challenges of deploying an efficient transformer service, we proposed a serving system called Turbo-Transformers. The system consists of a computation runtime and a serving framework. The runtime adopts a variable-length-input-friendly design to avoid time-consuming preprocessing specified with dimensions of the intermediate tensor. After loading a pre-trained model, the runtime rewrites the computation graph by fusing non-GEMM kernels, and provides efficient CUDA implementations for them. Before launching an inference, it conducts light-weight memory usage optimizations according to the input sequence length. The runtime is able to achieve state-of-the-art performance compared with existing DL runtimes. Moreover, it is extremely easy to use, which can bring end-to-end speedup by adding a few lines of Python code. Building upon the runtime, the serving framework improves response throughput and reduce latency through a variable-length-aware batching technique. The innovative contributions of the paper are listed as follows.

- We proposed a new parallel algorithm for Batch Reduction kernels like Softmax and LayerNorm, which pushes the efficiency boundary of these kernels on GPU.
- We proposed a sequence-length-aware memory allocation algorithm. Facing variable memory usage requirement, It remains a low execution overhead and shrinks the overall footprint.
- We proposed a sequence-length-aware batching scheduler. It utilizes a dynamic programming algorithm to organize an optimal batching scheme to achieve the best throughput and lower the latency.

2 Backgrounds

2.1 Transformer Models

Self-attention is the key idea behind the transformer model. It has the ability to attend to different positions of the input sequence to compute a representation of that sequence. A transformer model handles variable-length input using stacks of self-attention layers instead of RNNs or CNNs. An encoder-decoder model architecture is illustrated in Figure 1.

Multi-head attention consists of four parts, a set of linear layers that are split into heads, a scaled dot-product attention, a concat, and a final linear layer. Each multi-head attention block gets three tensors as inputs; Q (query), K (key), V (value). These are put through the linear layers and split up into multiple heads. The scaled dot-product attention computes the dot products of the query with all keys, and applies a Softmax function to obtain the weights on the values. The attention output for each head is then concatenated and put through the linear layers and split up into multiple heads. The scaled dot-product attention computes the dot products of the query with all keys, and applies a Softmax function to obtain the weights on the values. The attention output for each head is then concatenated and put through a final linear layer. In addition to multi-head attention, each of the layers in our encoder and decoder contains a fully connected feed-forward network to improve the capacity of the model. It consists of two linear transformations with activations in between. By introducing parallelism on the sequence length, dimensions of Q, K, and V tensors change unpredictably during serving. Take a real-time translation system as an example. After a short greeting phrase including a few words as input, a long paragraph of hundreds of words maybe its next input.

Figure 1 shows a transformer architecture with both encoder and decoder parts. Note that decoder parts are not necessary in transformer-based model, for example the widely-used BERT model only contain the encoder parts.

2.2 Serving Systems

Leveraging the power of transformer-based models to NLP online applications requires joint efforts in both training and serving stages. Training is the process of building a model
from offline data, which requires iteratively forward and backward passes. Serving, consisting of repeated inferences, is the process of using the model to extract useful features from user online input through a forward pass. Although inference does not involve complex backward computation and iterative processing, its performance requirements are more demanding. The serving process must run in real-time with low latency and sometimes should have the capacity of handling orders of magnitude more throughput than during training. A serving system can be divided into two components, a DL inference runtime, and a serving framework.

Training frameworks have been widely used as inference runtimes. For instance, TF-serving [9] is wrapped with TensorFlow. Considering the poor performance of applying training framework in inference, some works have been dedicated to inference-specific runtimes, such as onnxruntime [18], TensorFlow XLA [10], TVM [3], and TensorRT [21]. Due to time-consuming preprocessing specific to the dimension of inputs, most of these runtimes can not be applied in variable-length input tasks. Among them, the only onnxruntime is able to be used in the variable-length input tasks, with dynamic axis supports after version 1.3. Faster Transformers [19] is a transformer boost software developed by NVIDIA. However, it is not a complete runtime because it has no memory manager and has to be used as an operator for TensorFlow. The comparison between this work and them are listed in Table 1.

Table 1. Comparison of our runtime and existing GPU DL Inference runtimes.

| Related Work       | Speed   | Preprocess | Variable-Len | Usage |
|--------------------|---------|------------|---------------|-------|
| Tensorflow-XLA [10]| Medium  | Yes        | No            | Easy  |
| PyTorch [22]       | Medium  | No         | Yes           | Easy  |
| TensorFlow [23]    | Fastest | Yes        | No            | Hard  |
| Faster Transformers [19] | Fast | Yes | No | Hard |
| ONNX-runtime [18]  | Fast    | Yes        | Yes           | Medium|
| TurboTransformers  | Fastest | No         | Yes           | Easy  |

The serving framework wraps the runtime into a service exposing gRPC/HTTP as endpoints. The advanced functionalities of the serving framework include batching, caching, model version management, and model ensembles. Batching boosts throughput substantially by combining multiple inference requests into a batch to increase GPU usability, which is the main focus of this paper. TF-serving enforces a static batch size by concat multiple requests together and has to pad zeros if requests are not enough. Clipper [5] proposed an adaptive batching scheme to dynamically find and adapt the maximum batch size. Nexus [26] further designed a batching scheduler to serve multiple different models on the same GPU. Ebird [6] is a prototype system designed an elastic batch scheduler based on an inference engine supporting multiple batches of the same model running concurrently. All of the above works are targeted at fixed-length input, which does not consider performance harm brought by zero-padding of short requests in a batch of variable-length requests. To avoid the zero-padding problem in RNN, BatchMaker [8] breaks the computation graph into a graph of cellulars and dynamically decides the set of cellulars should be batched together. It takes advantage of the weight sharing between multiple forward passes of RNN, which is not applicable in transformer models.

3 Design Overview

As shown in the Figure 2, there are two ingredients of TurboTransformers, an inference runtime and a serving framework. Section 4 will elaborate on the details of the runtime, and Section 5 will focus on the serving framework.

![Figure 2. The serving system architecture adopted by TurboTransformers.](image)

4 Inference Runtime

Inference runtime focuses on increasing computation efficiency and optimizing memory allocation.

4.1 Computational Optimizations

4.1.1 Kernel Fusion. Without backward propagations, there is a lot of room left for inference customized optimizations. When using training frameworks, like TensorFlow or PyTorch to infer a transformer model on the GPU, a significant amount of time is spent on some non-computational intensive kernels. Take PyTorch as an example. For the case where batch size and sequence length are both relatively large, PyTorch BERT brings low efficiency due to the inefficient implementations of non-GEMM kernels. For a BERT inference on a Tesla V100 GPU using input with batch size as 20 and sequence length as 128, only 61.8% of the time is spent on GEMM kernels, and 38.2% is spent on non-GEMM intensive cores, such as LayerNorm, Softmax, Add Bias, Transpose, etc. For the case where batch size and sequence length are relatively small, PyTorch leads to poor efficiency due to the launch overhead of the CUDA kernels. For a BERT model inference on a Tesla V100 GPU with batch size as 1 and sequence length as 40, GPU is completely idle 80.64% of the time.
Kernel fusion is able to increase computation efficiency by reducing the number of memory accesses, increasing cache locality, and reducing kernel launch overhead. Similar to many popular frameworks, such as TensorFlow, and Theano [2], our runtime represents the DNN forward propagation by constructing a computation graph, in which nodes are operators and edges are tensors. As shown in Figure 3, the computation graph of a transformer can be reorganized into a more compact graph by fusing all the kernels between two GEMM kernels into a single one. The fused non-GEMM kernels are non-standard DNN operators, so it is impossible to take advantage of existing DNN operator libraries, such as cuDNN [20]. For example, there is no such API to combine matrix addition and transpose operation in a single CUDA kernel.

TurboTransformers implements all the non-GEMM kernels using CUDA, which can be categorized into two types. One type of kernel, such as fused activation functions and fused transpose operations, are composed of element-wise operations. There is no dependency between the processing of two different tensor elements, so we can process them in embarrassingly parallel. The second type of kernels, including Softmax and fused LayerNorm, are composed of reduction operations, which is notorious for being hard to parallelized. The latter is the focus of our performance improvement.

4.1.2 GPU-based Batch-Reduction. Both of Softmax and LayerNorm based kernels can be viewed as Batch Reduction operations. On the lower dimension of a 2D tensor, Softmax calculates summation and maximum and LayerNorm calculates the mean and variance. In other words, they both need to reduce a batch of 1D arrays in parallel. Table 2 shows the proportion of time of the two operators in the attention layer. We can observe that they are two big hotspots if not carefully optimized.

Realizing the inefficiency of PyTorch operators, some efforts are spent on optimize GPU batch reduction. According to the programming model of CUDA, efficient reduction algorithms need to fully utilize the power of three hardware levels. First, by splitting on the batch dimension, streaming-processors (SMs) level parallelism is exploited by the process of the workload on different SMs in parallel. Second, warp level parallelism is exploited by taking advantage of the warp-level inter-thread communication mechanism provided by CUDA beyond the 9.0 version. Third, instruction-level parallelism is exploited by overlapping memory access and computation instructions. A classical implementation adopted in Faster Transformers [19] is shown in the top part of the Figure 4. It is derived from work [16], which proposed a best practice for 1-D array reduction operations on the GPU. Reduction workloads of \( n \) rows (inside the dotted line on the top of the figure) are assigned to a thread block, which is scheduled to be executed on an SM. The thread block sequentially performs \( n \) times independent 1-D array reduction, which is finished with two-pass. In the first pass, each warp of the SM conducts a warpReduce operation on 32 aligned elements, and then store reduction results of them inside shared memory. In the second pass, a warp load at most 32 partial results to register and conduct another warpReduce to obtain the final results.

In this paper, we push the efficiency boundary of classical batch reduction algorithms on GPU. Note that some space is still left for improvement of warp level and instruction parallelism in the above algorithm. First, due to the accesses of shared memory, synchronizations of warps inside an SM introduce huge overheads. Second, if the input array is not 32-aligned, warp divergence resulting from boundary processing also introduces extra overhead. Third, warpReduce leads to poor efficiency of instruction issuing. As pointed out by work [16], there is a dependency between shuffle and add instructions. In the upper right corner of the figure, the target register R3 in an SHFL DOWN instruction is required immediately as a source register in FADD instruction. The FADD instruction can only be issued until the SHFL is completely finished, whose latency is more than 1 cycle.

The above three shortcomings can be overcome by leveraging parallelism between multiple 1-D reduction operations. As shown in the bottom part of Figure 4, a new subroutine warpAllReduceSum_XElem (\( X = 2 \) in our figure) is introduced, which combine X warp as a batch and do their reduction together. First, only one synchronization is required for

![Figure 3. Kernel fusion of a transformer encoder. The part in darker color is a multi-head attention. The part in lighter color is a feed forward network.](image-url)

| Table 2. Proportion of batch reduction operations in attention layer before and after optimizing. |
|---------------------------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| (batch size, seq len)           | (1, 10)        | (1, 100)       | (1, 500)       | (20, 10)       | (20, 100)      | (20, 500)      |
| Softmax/Attention before        | 29.20%         | 21.72%         | 18.96%         | 10.61%         | 52.59%         | 83.38%         |
| Softmax/Attention after         | 4.56%          | 4.40%          | 4.08%          | 5.14%          | 6.44%          | 4.24%          |
| LayerNorm/Attention before      | 29.20%         | 21.72%         | 18.96%         | 10.61%         | 52.59%         | 83.38%         |
| LayerNorm/Attention after       | 4.56%          | 4.40%          | 4.08%          | 5.14%          | 6.44%          | 4.24%          |

\(^1\)In the table, the execution time of Softmax and LayerNorm is measured using PyTorch. Attention time is measured using our runtime after replaced Softmax and LayerNorm with PyTorch’s implementations, respectively.
X elements reduction in blockReduceSum_XElem, therefore, reduces \((X - 1)/X\) synchronization cost. Second, \(X\) independent boundary processing can be merged into a single one, therefore reduce warp divergence. Third, the instruction issuing is more efficient because we eliminate instructions dependency. As shown in the figure, the target register of SHFL DOWN has required two cycles later by FADD as a source register. Another SHFL DOWN with no dependency on the previous one can be issued immediately.

Especially for the LayerNorm kernel, TurboTransformers further derives a mathematical optimization trick to improve efficiency. LayerNorm requires the variances of elements of 1-D arrays. There are two equivalent formulas of variance, as shown in the Equation 1. The first one used in [19] requires two separate reductions for \(x\) and \(x - E(x)\), during which one synchronization between. We use the second one to compute variances. The warpAllReduceSum_2Elem can simultaneously reduce \(x\) and \(x^2\), which not only increases the efficiency of instruction execution but also reduces half of the number of synchronizations.

\[
\text{Var}(x) = E((x - E(x))^2) = E(x^2) - E^2(x)
\]  

(1)

Figure 5 shows the speedups of Softmax and LayerNorm kernels in TurboTransformer compared with the other implementations. The baseline of both kernels is used implementations from [19]. For the Softmax kernel, we also compare with the Softmax routine cuDNNv7.5. In most cases, our optimization strategy has achieved obvious acceleration. Due to the batch dimension is larger for Softmax, its performance boost is more significant.

4.2 Memory Manager

Besides computing optimizations, memory management is also vital to a DNN runtime. It is evaluated by two metrics. The allocation efficiency, which determined by the number of times and the amount of the memory is allocated and released, affects the overall execution speed of the runtime. The memory footprint affects the possible size of the model as well as the maximum batch size of requests. Three types of memory are managed by the runtime, i.e., input tensors, intermediate tensors, layer parameters. Dimensions of intermediate tensors change frequently during inferences in case of variable-length input. Adversely, for fixed-length input, the dimensions of intermediate tensors are determined in advance and allocation scheme never changes during inference processes. Therefore, the memory usage and positions of tensors can be pre-optimized and fixed during serving. However, The optimal memory allocation strategy is different in case of the different input lengths. Allocator of variable-length processes. Therefore, the memory usage and positions of tensors should be allocated when needed, and released immediately when not required. Frequent allocation and release of small memory space on GPU will lead to a worse runtime efficiency. For example, in this case, 50% of the computing resources idle wait for memory allocation ready on Tesla M40 (batch size = 20, sequence length = 128). To achieve the best allocation efficiency, the memory should be allocated in advance and cached for repeated use in the future the inferences without any extra allocation. However, it is challenging to predict maximum memory usage to meet the requirement of a long-term serving process. Even if we know.
Memory Allocation of seq len= 200

Although the allocator for fixed-length input has been well studied, the one for variable-length input is still not perfect. For fixed-length input, by taking advantage of the topology of the computation graph, works [23] [15] figure out the optimal memory usage by reusing the same memory space for intermediate tensors do not coexist. For variable-length input, The existing solutions have to tradeoff allocation efficiency and footprint. PyTorch [22] designed a custom caching tensor allocator which incrementally builds up a cache of CUDA memory and reassigns it to later allocations. PaddlePaddle [17] used a similar method, which is all inspired by the caching device allocator implemented in the NVlab’s cub library [25].

Experiments have shown that these methods cannot achieve optimal memory usage, because they do not consider the DNN’s computation graph.

We adopted an innovative memory optimization method for variable-dimension intermediate tensors, which evoke a lightweight variable-length-aware memory manager after knowing the length of each inference. To achieve more efficiency and less footprint, the allocator used in TurboTransformers combines the idea of memory cache and graph-topology-aware space reuse. First, it organizes memory space in units of the chunks, which is a small block, for example, 2MB of memory. By reusing already allocated chunks, allocation efficiency can remain at a high level during serving. Second, it utilizes the computation graph to know the life cycle of each intermediate tensor in advance, and calculate the offset of each tensor within a specific chunk as soon as it recognizes the sequence length of the new arrival request. In this way, tensors with no overlapping life cycle can reuse the same memory space, therefore reduce memory footprint as much as possible.

Our sequence-length-aware allocation method is shown as Algorithm 1. The input tensor usage record is a list of tuples (first_op, last_op, size), where first_op, last_op are indices of the first and last operator that use the tensor. The indices are from the topological sorting of the DNN’s computation graph. It first sorts the usage records in non-increasing order based on the size of the tensor. FindGapFromchunk is used to determine if there exists a free gap inside a chunk to fit for that tensor. If no such gap is found in all existing chunks, we append a new chunk to the end of the chunk list. The size of the new chunk is the maximal one of DEFAULT_chunk_SIZE (2MB in our implementation) and the size of tensor times $K_{SCALE}$ (1.2 in our implementation).

FindGapFromchunk of Algorithm 2 finds the best gap in a memory chunk. It is equivalent to a special case of the 2D strip packing problem, which is NP-hard. We slightly modify the Greedy by Size for Offset Calculation Algorithm in [15] to solve FindGapFromchunk in $O(n^2)$ time complexity. The inputs are a target tensor $t$ and a target chunk $chunk$. For each record $x$ in the chunk, the algorithm first check whether $x$ and the target tensor $t$ overlap in usage time (L6 - L8), in order to find the smallest gap between them such that current tensor fits into that gap (L9 - L13). If we found such a gap before the end of the chunk, we assign the tensor $t$ to the gap. Otherwise, the function return invalid. (L17 - L24).

### Algorithm 1 Sequence-length-aware allocation algorithm

**Require:** tensor_usage_records: a list of tuples (first_op, last_op, size), chunk_list: a chunk contains size, mem addr, a list of pairs(tensor_id, offset)

1: sort tensor_usage_records in non-increasing order of size
2: for each record $r \in$ tensor_usage_records do
3:   is_assigned $\leftarrow$ false
4:   for each chunk $c \in$ chunk_list do
5:     offset $\leftarrow$ FindGapFromchunk($t$, chunk)
6:     if offset is valid then
7:       assigned_chunk $\leftarrow$ chunk_id
8:       assigned_offset $\leftarrow$ offset
9:       is_assigned $\leftarrow$ True
10:   break
11: end if
12: end for
13: if is_assigned is false then
14:   new_chunk_size $\leftarrow$ max(DEFAULT_chunk_SIZE, $t_{size} \times K_{SCALE}$)
15:   assigned_chunk $\leftarrow$ len(chunk_list)
16:   assigned_offset $\leftarrow$ 0
17:   append a new chunk of size new_chunk_size to chunk_list
18: end if
19: end for
20: release unused chunk in chunk_list
21: return assigned_chunk, assigned_offset, chunk_list

![Algorithm 1 Sequence-length-aware allocation algorithm](image)

Figure 6. A memory allocation example uses our proposed variable-length-aware allocator.
Algorithm 2 FindGapFromChunk

Require: t : tensor_id, chunk
1: get chunk_size from chunk
2: smallest_gap ← ∞
3: prev_offset ← 0
4: best_offset ← NIL
5: for each record x ∈ chunk do
6:  max_first_op ← max (first_opi, first_opx)
7:  min_last_op ← min (last_opi, last_opx)
8:  if max_first_op ≤ min_last_op then
9:      gap ← offsetx − prev_offset
10:     if gap ≥ sizei and gap < smallest_gap then
11:         smallest_gap ← gap
12:         best_offset ← prev_offset
13:     end if
14:  prev_offset ← max(prev_offset, offsetx + sizex)
15: end if
16: end for
17: if best_offset = NIL and chunk_size − prev_offset ≤ sizei then
18:    best_offset ← prev_offset
19: end if
20: if best_offset is NIL then
21:    return INVALID
22: else
23:    return best_offset
24: end if

Figure 6 shows an example of applying our algorithm on a BERT inference application. When the input length changes from 200 to 240, we allocate one more chunk and adjust the offsets. Figure 7 compares the memory footprint and allocation efficiency of our allocator and an allocator using Greedy by Size for Offset Calculation (GSOC) algorithm, which achieved a near-optimal footprint for fix-length input inference. In addition 440 MB memory for model parameters as well as 93.76 MB embedding for matrix, the maximum total memory usage of all cases is no more than 540 MB. In contrast, memory consumption of PyTorch on this test is stable at around 1.1 GB. In 50 tests, 0.70MB of memory was used for new requests on average using our method, while, on average, 2.78 MB is required by GSOC algorithm.

4.3 Usability

Our runtime provides C++ and Python APIs. As shown in the following code snippet, adding 3 lines of python code (L3, 12, 13) can bring end-to-end speedup to your inference computation.

```python
import torch
import transformers
torch_model = transformers.BertModel.from_pretrained(model_id)
```

5 Serving Framework

Based on the computation runtime, a serving framework is required to attain enough serving throughput under latency constraints to satisfy a Service Level Objectives (SLOs). The serving framework of TurboTransformers is shown in Figure 2. The user’s requests first arrive at a Message Queue (MQ) and then are sent to runtime for inference computation after two serving-level optimizations, i.e. Caching and Batching. For caching, similar to Clipper [5], by caching the inference results in a database, the Resp Cache component in the figure responses the frequent requests without evaluating the model. For batching, the Batch Scheduler component is responsible for packaging requests that come in a period of time into a batch. In most application scenarios, the input of the user is a single inference request with batch size as 1. It has been known that small batch sizes lead to low GPU hardware utilization. Packaging multiple requests into a relatively larger batch and conducting inference on them together can improve hardware utilization. As shown in Figure 8, serving requests in batch brings significant speedup, especially for short sequences. The batch schedulers adopted by conventional serving systems, like TF-serving [9] and Nexus [26], are designed to packages requests with fixed-length into a batch. Currently, serving systems are lack of critical ability to handle variable-length requests.

![Figure 7. Comparison of two memory allocators in the case of variable-length input.](image_url)

![Figure 8. Batching brings performance gain for the base BERT serving on RTX 2060 GPU. The y-axis illustrates the normalized latency of inferring a request of batch size 1.](image_url)
different lengths into a batch, then all requests in the batch will be zero-padded with regards to the maximum length of the request in the batch. Zero paddings will introduce a lot of extra computations. An efficient batch scheduler has to carefully balance the overheads of padding and the benefits of batching. For example, assume that there are five inference requests to be served, with lengths of 17, 18, 52, 63, and 77, respectively. Packing a single batch with 5 instances is less efficient than no batching. The batching scheme achieving the optimal throughput is packing three batches. As shown in Figure 9, the response throughput (resp/sec) improved 35% by the optimal scheduling scheme.

Figure 9. An example of batch scheduler for variable-length requests.

For variable-length request serving, we proposed an innovative sequence-length-aware batch scheduler in Algorithm 3. The core idea is to use dynamic programming (DP) to solve a optimization problem which maximizes the response throughput as the objective in $O(n^2)$ time complexity. The inputs of the algorithm consist of two data structures. The request list is the list of input requests with variable length. The cached cost is a dictionary. It uses two keys as indices, namely the sequence length and batch size. Its value is the inference cost with the parameter from the corresponding key. The values of cached cost are collected by a warm-up phase after the service first starts on specific hardware, which utilizes the runtime to run inferences under all possible batch sizes and sequence lengths. They are stored on disk or database (database in Figure 2) and reloaded to memory when the serving module is restarted. First, the request list are sorted in increasing order according to the sequence length. Then line 3 initializes an array called states to store intermediate information. Specifically, state[i] records the minimum time overhead for processing the sublist request list[0 : i]. The algorithm traverses each request in request list and uses a DP algorithm to update the state[i] at the corresponding position i. The Bellman equation of this DP problem is shown in Equation 2.

$$\text{state}[i] = \min_{0 \leq j \leq i} (\text{cached cost}[\text{request list}[i].\text{len}][i - j + 1] \times (i - j + 1) + \text{states}[j - 1])$$

(2)

Note that the premise of this algorithm work is that there exists a scheduling strategy for requests in MQ that can meet SLO on this server. In a multi-server environment, an upper-level load balancer as the one in Nexus [26] can ensure that the requests assigned to each server will not be overloaded. There are two options to decide when to evoke the batch scheduler. The first one is a hungry strategy. When the runtime is idle, we immediately start the batch scheduler to batch requests in MQ. This strategy is suitable for the situation where request throughput is high and the GPU have to run at full load. The second one is a lazy strategy. Similar to delayed batching of Clipper, we sets a timeout value and a maximum batch size. Once the number of requests in the batch exceeds the maximum batch size, or the timeout is reached, we start the batch scheduler. Due to the reordering of requests in Algorithm 3, requests that arrive early may be served late. We check the elapse between the current time and the recorded arrival timestamp of request at the front of the MQ, and start the batch scheduler immediately if the elapse plus the estimated execution latency of current requests in batch exceeds half of the latency constraints. This strategy is suitable when the runtime is extremely inefficient at a small batch size.

Algorithm 3 Batch Scheduler With Dynamic Programming

Require: request list, cached cost
1: sort request list in increasing order with regards to sequence length
2: $N \leftarrow $ Size(request list)
3: Create states, start_idx list as lists of size $N + 1$
4: states[0] $\leftarrow$ 0, i $\leftarrow$ 1
5: while i $\leq$ N do
6:   j $\leftarrow$ i - 1
7:   cur_length $\leftarrow$ request list[i - 1].length
8:   min_cost $\leftarrow$ cached_cost[cur_length][i] + states[j]
9:   start_idx $\leftarrow$ i - 1
10: while j $> 0$ do
11:   tmp_cost $\leftarrow$ states[j - 1] + cached_cost[cur_length][i - j + 1] $\times$ (i - j + 1)
12:   if tmp_cost $< min_cost$ then
13:      min_cost $\leftarrow$ tmp_cost
14:      start_idx $\leftarrow$ j - 1
15:   end if
16:   j $\leftarrow$ j - 1
17: end while
18: states[i] $\leftarrow$ min_cost, start_idx list[i] $\leftarrow$ start_idx
19: i $\leftarrow$ i + 1
20: end while
21: i $\leftarrow$ N
22: while i $> 0$ do
23:   end_idx $\leftarrow$ i, start_idx $\leftarrow$ start_idx list[i]
24:   pack request list[start_idx : end_idx] into a batch
25:   i $\leftarrow$ start_idx - 1
26: end while
6 Experimental Results

6.1 Performance of the Runtime

The runtime is evaluated on three transformer networks, including Bert [7], Albert [14] and a Seq2Seq Decoder [28], the parameters of which are shown in Table 3.

| Model    | Parameters                             |
|----------|----------------------------------------|
| Bert     | num_layer=12, num_head=12, hidden_size=64 |
| Albert   | num_layer=12, num_head=12, hidden_size=64 |
| Decoder  | beam_size=4, max_target_len=500         |

6.1.1 Efficiency on variable-length input. The ability to handle variable-length input is evaluated by sequential execution of the runtime using inputs of different lengths on NVIDIA RTX 2060. For Bert and Albert, the input is randomly sampled text, with a length ranging from 5 to 500. For Decoder, it is applied in a Chinese-English translation task, and its input is randomly sampled Chinese text with a length ranging from 28 to 137. Note that our sampling is completely random and the random seed is the same for different tests, although the figure displays in order of input length from small to large for the sake of clearness.

As shown in Figure 10, TurboTransformers’ runtime shows obvious performance advantages. For all test cases, we compare our runtime with PyTorch (version 1.5.0). Especially, for Bert, we export the PyTorch model to onnx format and run it by onnxruntime-gpu (version 1.3.0). In the case of Bert inference, the speedups of Turbo to PyTorch are ranging from 1.10x-2.58x; The speedups of Turbo to onnxruntime are ranging from 1.35x-2.26x. In the case of Albert inference, the speedups of Turbo to PyTorch are ranging from 0.84x-1.68x. The two cases without acceleration are 5 and 12 in length, whose execution time is very short. The longer the sequence, the more significant the speedup of the turbo. In the case of Albert inference, the speedups of Turbo to PyTorch are ranging from 1.85x-2.51x. The performance improvement comes from our optimization of non-GEMM operators, in which batch reduction is particularly significant. 6.1.2 Efficiency on fixed-length input. To evaluate the improvement resulting from our computation optimizations, we also compared with another three popular runtimes that only support fixed-length input. 1) TensorFlow-XLA is implemented with TensorFlow (version 1.13) and preprocessed with XLA. 2) Faster Transformers is a transformer boost software developed by NVIDIA, which implements a set of customized fused kernels like us. However, it has no memory management and using the memory allocator of the TensorFlow framework. 3) NVIDIA TensorRT is an SDK for high-performance deep learning inference. The above three solutions require an time-consuming pre-tuning process based on the input dimension in advance, so they cannot be applied in the handling of the real-time variable-length requests.

For the sake of fairness, we chose BERT as the transformer model to be evaluated on a fixed-length input task, for which every runtime has been specifically optimized for it, and an official example is provided. We selected a parameter space consisting of two parameters, in where the sequence length ranges from 10 to 500 and the batch size includes 1 and 20. Each runtime executes 150 times to calculate the average latency for each group of parameters. The speedup of TurboTransformers on RTX 2060 and V100 to the other runtimes is shown in Figure 11. On RTX 2060 GPU, except for the lowest workload case (1, 10), our runtime is the best in performance. Especially for the parameter space of a higher workload, the speedup is more significant. On V100 GPU, the most potent competitor is TensorRT, however, ours is better than it in 13 cases out of 20 cases. Ours is especially better on more heavy workload cases.

6.2 Performance of Serving Framework

The efficiency of the serving framework is evaluated on the server equipped with an AMD Ryzen 7 3700X CPU and one RTX 2060 GPU. We choose a BERT service as our target application, which is used to classify a paragraph of text. The text is randomly sampled from a chitchatting dataset and the sequence length of text satisfies a normal distribution from 5 to 500. The requests are sent to the serving system
with Poisson inter-arrival times. We turned off the caching optimization.

The throughput and latency results are illustrated in Figure 12 and Table 4. The x-axis of Figure 12 indicates how many requests arrive at the serving system per second, which is ranging from 20 req/sec to 1500 req/sec. The y-axis of Figure 12 represents how many responses can be obtained per second. The critical point for service latency to remain stable is that request throughput and response throughput are equal. When request throughput is higher than the critical point, the requests will accumulate in the message queue and it will lead to long delays of latter requests. In the long run, its latency will gradually tend to infinity (+∞) and cause the network packet loss. We observed that the throughput of the worse version of our implementation (PyTorch-NoBatch) is significantly efficient than TF-serving, which has to pad sequences to the maximum length and brings huge overhead.

We then analyze the improvement of our innovative batch scheduler. Turbo-Naive-Batch is a serving implementation with a naive batch scheduler, which packs the requests currently inside the message queue into a single batch. Turbo-DP-Batch is a serving implementation with our proposed variable-length-aware batch scheduler. Both of them is using our proposed runtime. The batch scheduler of our system employs the hungry strategy and the maximum batch size is 20. The response throughput of Turbo-DP-Batch is saturated at 144 req/sec, while the response throughput of Turbo-NoBatch is saturated at 98 req/sec. Due to the additional zero-padding overhead, The performance of Turbo-NoBatch is even worse than Turbo-NoBatch. Compared with Turbo-NoBatch, the throughput is increased by 20% from 120 req/sec to 144 req/sec. Compared with PyTorch-NoBatch, the throughput is increased by 140%. Under the same request throughput rate, Turbo-DP-Batch usually brings the lower average and maximum service latency. For example, when request throughput is 120, Turbo-DP-Batch reduce the average/maximum latency from 32.91/127.61 ms to 23.18/81.83 ms, which are 30/36% reduction.

7 Conclusion
TurboTransformers improves latency and throughput for deploying transformer-based DL services in GPU datacenter. It solves two critical problems introduced by the transformer model, which are unprecedented computation pressure and variable-length input. For these purposes, it proposed three innovations in computing, memory and serving levels, including a new parallel batch reduction algorithm for Softmax and LayerNorm kernels, a sequence-length-aware memory allocator as well as a sequence-length-aware batching scheduler. The runtime achieves better performance than PyTorch, TensorFlow-XLA, onnxruntime, and FasterTransformers in as the runtime to replace ours. The throughput of PyTorch-NoBatch as runtime is saturated at 60 resp/sec, while the response throughput of using Turbo-NoBatch is saturated at 120 resp/sec. When request throughput is 60 req/sec, the average/maximum latency of PyTorch-NoBatch is 77.71/158.06 ms while the average latency of Turbo-NoBatch is at 8.05/20.53 ms. Our runtime optimization brings 2x speedup on possible serving throughput and 87% reduction on maximum latency.

Table 4. The latency of four serving systems. Each item in the table represents the average (minimum, maximum) latency in milliseconds.

| Request Throughput (req/sec) | PyTorch NoBatch | NaiveBatch | Turbo NoBatch | Turbo-DP Batch |
|-----------------------------|-----------------|------------|---------------|----------------|
| 60                          | (10.61, 158.06) | (3.06, 121.96) | (2.76, 20.53) | (2.70, 27.42)  |
| 98                          | +∞              | (2.96, 65.09) | 24.83         | 13.79          |
| 120                         | +∞              | +∞          | (3.14, 127.61) | 23.18          |
| 144                         | +∞              | +∞          | +∞            | 38.21          |

Figure 11. Runtime comparison on fixed-length input task on RTX 2060 and V100 GPU. The y-axis indicates normalized speedup of TurboTransformers.

Figure 12. Response throughput of serving under different request throughput.
both fixed-length and variable-length input cases. While conventional batching is invalid for variable-length request, the serving framework achieves higher throughput and lower latency using the proposed batch scheduler. In a real-time BERT service, our system improves the throughput limitation by 140% to a PyTorch implementation.

References

[1] Martin Abadi, Paul Barham, Jianmin Chen, Zhifeng Chen, Andy Davis, Jeffrey Dean, Matthieu Devin, Sanjay Ghemawat, Geoffrey Irving, Michael Isard, et al. 2016. Tensorflow: A system for large-scale machine learning. In 12th USENIX symposium on operating systems design and implementation (OSDI16). 265–283.

[2] James Bergstra, Olivier Breuleux, Frédéric Bastien, Pascal Lamblin, Razvan Pascanu, Guillaume Desjardins, Joseph Turian, David Warde-Farley, and Yoshua Bengio. 2010. Theano: a CPU and GPU math expression compiler. In Proceedings of the Python for scientific computing conference (SciPy), Vol. 4. Austin, TX, 1–7.

[3] Tianqi Chen, Thierry Moreau, Zheng Jiang, Lianmin Zheng, Eddie Yan, Haichen Shen, Meghan Cowan, Leyuan Wang, Yuwei Hu, Luis Ceze, et al. 2018. TVM: An automated end-to-end optimizing compiler for deep learning. In 13th USENIX Symposium on Operating Systems Design and Implementation (OSDI 18). 578–594.

[4] Kyunghyun Cho, Bart Van Merriënboer, Dzmitry Bahdanau, and Yoshua Bengio. 2014. On the properties of neural machine translation: Encoder-decoder approaches. arXiv preprint arXiv:1409.1259 (2014).

[5] Daniel Crankshaw, Xin Wang, Guiluo Zhou, Michael J Franklin, Joseph E Gonzalez, and Ion Stoica. 2017. Clipper: A low-latency online prediction serving system. In 14th USENIX Symposium on Networked Systems Design and Implementation (NSDI 17). 613–627.

[6] Weihtao Cui, Mengze Wei, Quan Chen, Xiaomin Tang, Jingwen Leng, Li Li, and Mingyu Guo. 2019. Ebird: Elastic Batch for Improving Responsiveness and Throughput of Deep Learning Services. In 2019 IEEE 37th International Conference on Computer Design (ICCD). IEEE, 497–505.

[7] Jacob Devlin, Ming-Wei Chang, Kenton Lee, and Kristina Toutanova. 2018. Bert: Pre-training of deep bidirectional transformers for language understanding. arXiv preprint arXiv:1810.04805 (2018).

[8] Pin Gao, Lingfan Yu, Yongwei Wu, and Jinyang Li. 2018. Low latency rnn inference with cellular batching. In Proceedings of the Thirteenth EuroSys Conference. 1–15.

[9] Google. 2020. TensorFlow Serving. https://github.com/tensorflow/serving. [Online; accessed July-2020].

[10] Google. 2020. XLA: Optimizing Compiler for Machine Learning. https://www.tensorflow.org/xla. [Online; accessed July-2020].

[11] Kaiming He, Xiangyu Zhang, Shaoqing Ren, and Jian Sun. 2016. Deep residual learning for image recognition. In Proceedings of the IEEE conference on computer vision and pattern recognition. 770–778.

[12] Sepp Hochreiter and Jürgen Schmidhuber. 1997. Long short-term memory. Neural computation 9, 8 (1997), 1735–1780.

[13] Alex Krizhevsky, Ilya Sutskever, and Geoffrey E Hinton. 2012. Imagenet classification with deep convolutional neural networks. In Advances in neural information processing systems. 1097–1105.

[14] Zhenzhong Lan, Mingda Chen, Sebastian Goodman, Kevin Gimpel, Piyush Sharma, and Radu Soricut. 2019. Albert: A lite bert for self-supervised learning of language representations. arXiv preprint arXiv:1909.11942 (2019).

[15] Juhyun Lee, Nikolay Chirkov, Ekaterina Igansheva, Yuriy Pisarchyk, Mogan Shieh, Fabio Riccardi, Raman Sarokin, Andrei Kulik, and Matthias Grundmann. 2019. On-device neural net inference with mobile gpus. arXiv preprint arXiv:1907.01989 (2019).

[16] Yuan Lin and V Grover. 2019. Using cuda warp-level primitives. Retrieved from https://devblogs. nvidia. com/using-cuda-warp-level-primitives/. Accessed (2019).

[17] Yanjun Ma, Dianhai Yu, Tian Wu, and Hai Feng Wang. 2019. PaddlePaddle: An open-source deep learning platform from industrial practice. Frontiers of Data and Computing 1, 1 (2019), 105–115.

[18] MicroSoft. 2020. ONNX Runtime is a cross-platform inferencing and training accelerator compatible with many popular ML/DNN framework. https://github.com/microsoft/onnxruntime. [Online; accessed July-2020].

[19] NVIDIA. 2019. FasterTransformer V1, a highly optimized BERT equivalent Transformer layer for inference. https://github.com/NVIDIA/DeepLearningExamples/tree/master/FasterTransformer. [Online; accessed April-2020].

[20] NVIDIA. 2020. cuDNN. https://developer.nvidia.com/cudnn. [Online; accessed August-2020].

[21] NVIDIA. 2020. NVIDIA TensorRT. https://developer.nvidia.com/tensorrt. [Online; accessed July-2020].

[22] Adam Paszke, Sam Gross, Francisco Massa, Adam Lerer, James Bradbury, Gregory Chanan, Trevor Killeen, Zeming Lin, Natalia Gimelshein, Luca Antiga, et al. 2019. Pytorch: An imperative style, high-performance deep learning library. In Advances in neural information processing systems. 8026–8037.

[23] Yuriy Pisarchyk and Juhyun Lee. 2020. Efficient Memory Management for Deep Neural Net Inference. arXiv preprint arXiv:2001.03288 (2020).

[24] Alec Radford, Jeffrey Wu, Rewon Child, David Luan, Dario Amodei, and Ilya Sutskever. 2019. Language models are unsupervised multitask learners. OpenAI Blog 1, 8 (2019), 9.

[25] NVIDIA Research. 2020. CUB. https://github.com/NVlabs/cub. [Online; accessed August-2020].

[26] Haichen Shen, Lequn Chen, Yuchen Jin, Liangyu Zhao, Bingyu Kong, Matthai Philipose, Arvind Krishnamurthy, and Ravi Sundaram. 2019. Nexus: a GPU cluster engine for accelerating DNN-based video analysis. In Proceedings of the 27th ACM Symposium on Operating Systems Principles. 322–337.

[27] Christian Szegedy, Wei Liu, Yangqing Jia, Pierre Sermanet, Scott Reed, Dragomir Anguelov, Dumitru Erhan, Vincent Vanhoucke, and Andrew Rabinovich. 2015. Going deeper with convolutions. In Proceedings of the IEEE conference on computer vision and pattern recognition. 1–9.

[28] Ashish Vaswani, Noam Shazeer, Niki Parmar, Jakob Uszkoreit, Llion Jones, Aidan N Gomez, Lukasz Kaiser, and Illia Polosukhin. 2017. Attention is all you need. In Advances in neural information processing systems. 5998–6008.

[29] Zhilin Yang, Zihang Dai, Yiming Yang, Jaime Carbonell, Russ R Salakhutdinov, and Quoc V. Le. 2019. Xlnet: Generalized autoregressive pretraining for language understanding. In Advances in neural information processing systems. 5753–5763.