Evaluating Modern GPU Interconnect: PCIe, NVLink, NV-SLI, NVSwitch and GPUDirect

Ang Li, Shuaiwen Leon Song, Jieyang Chen, Jiajia Li, Xu Liu, Nathan Tallent, and Kevin Barker

Abstract—High performance multi-GPU computing becomes an inevitable trend due to the ever-increasing demand on computation capability in emerging domains such as deep learning, big data and planet-scale simulations. However, the lack of deep understanding on how modern GPUs can be connected and the real impact of state-of-the-art interconnect technology on multi-GPU application performance become a hurdle. In this paper, we fill the gap by conducting a thorough evaluation on five latest types of modern GPU interconnects: PCIe, NVLink-V1, NVLink-V2, NVLink-SLI and NVSwitch, from six high-end servers and HPC platforms: NVIDIA P100-DGX-1, V100-DGX-1, DGX-2, OLCF’s SummitDev and Summit supercomputers, as well as an SLI-linked system with two NVIDIA Turing RTX-2080 GPUs. Based on the empirical evaluation, we have observed four new types of GPU communication network NUMA effects: three are triggered by NVLink’s topology, connectivity and routing, while one is caused by PCIe chipset design issue. These observations indicate that, for an application running in a multi-GPU node, choosing the right GPU combination can impose considerable impact on GPU communication efficiency, as well as the application’s overall performance. Our evaluation can be leveraged in building practical multi-GPU performance models, which are vital for GPU task allocation, scheduling and migration in a shared environment (e.g., AI cloud and HPC centers), as well as communication-oriented performance tuning.

Index Terms—Performance Evaluation, GPU, Interconnect, NUMA, PCIe, NVLink, NVSwitch, SLI, GPUDirect, RDMA, NCCL

1 INTRODUCTION

MULTI-GPU execution nowadays becomes an inevitable trend for warehouse GPGPU computing. This is due to the ever-increasing demand of computation capability from emerging domains such as machine learning, big data and planet-scale simulations [1], [2]. With increasingly larger problem to solve, scalable GPU computing becomes necessary. Recently, a research group from Sony leveraged 3,456 GPUs to train a ResNet-50 neural network for ImageNet in 122 seconds, achieving near optimal GPU scaling efficiency [3]. The Swiss National Supercomputing Center (CSCS) relied on 4,888 GPUs in the Piz Daint supercomputer to simulate near-global climate in ultra-high resolution [2].

Multi-GPU execution scales in two directions: vertically scaling-up in a single node and horizontally scaling-out across multiple nodes. Good examples to describe the intra-node scale-up scenario are the latest NVIDIA DGX-1 [3] and DGX-2 [5] super-AI servers, which incorporate 8 and 16 P100/V100 GPUs connected by NVLink and NVSwitch, respectively. For the inter-node scale-out scenario, the U.S. Department of Energy (DOE) has recently deployed two GPU-accelerated supercomputers Summit [6] and Sierra [7] in Oak Ridge and Livermore National Laboratories, with more than 3400 GPU-integrated nodes interconnected.

Gaining performance from multi-GPU scaling, however, is not trivial, mainly because (i) There are no mature multi-GPU parallel programming, execution and performance models, largely due to the limited knowledge on how modern GPUs are interconnected as well as their communication patterns; (ii) Traditionally, inter-GPU communication shares the same bus interconnect as CPU-GPU communication, such as PCIe. This situation recently changed due to the introduction of GPU-oriented interconnect such as NVLink, NV-SLI and NVSwitch. However, their characteristics, as well as the performance impact on real-world multi-GPU applications are still unknown, limiting the efforts to leverage them for advanced performance tuning and delivery.

In this paper, we fill this gap by thoroughly characterizing a variety of modern GPU interconnects, including PCIe, NVLink Version-1, NVLink Version-2, NV-SLI, NVSwitch, and GPUDirect. We measured their raw startup latency, sustainable uni/bi-directional bandwidth, network topology, communication efficiency, routing, and NUMA effects, under the two communication patterns: Peer-to-Peer (P2P) and Collective (CL). Based on these results, we summarize several observations, challenges to address, and potential research topics regarding to multi-GPU execution. Through this evaluation, software designers can gain deeper knowledge about the latest GPU interconnects, paving the way for building more mature multi-GPU programming, execution and performance models, and reliable simulators for better guiding application development and performance tuning.

2 MODERN GPU INTERCONNECT

We focus on six types of modern GPU interconnect: PCIe, NVLink-V1, NVLink-V2, NV-SLI, NVSwitch, and GPUDirect-enabled InfiniBand. Table 1 lists the platforms we used for evaluation. For GPU-GPU communication, P100-DGX-1, V100-DGX-1 are for evaluating PCIe, NVLink-V1 and NVLink-V2. SLI is for NV-SLI, DGX-2 is for NVSwitch. SummitDev and Summit are for assessing inter-node InfiniBand interconnect with GPUDirect-RDMA. We first briefly review every technology.
TABLE 1: Evaluation Platforms. “Arch” refers to GPU architecture generation. “SP/DP GFlops” refer to GPU theoretical single/double floating-point performance. “Rtm” refers to CUDA runtime version.

| Platform          | Configuration | Interconnect | CPU              | Compiler | GPU | CPU Arch | SP/DP GFlops | CPU Memory            | Rtm          |
|-------------------|---------------|--------------|------------------|----------|-----|----------|---------------|-----------------------|--------------|
| P100-DGX-1        | Single node, 3 GPUs | NVLink-V1   | Intel Xeon ES-2689 | gcc-4.8.4 | Tesla-P100 | Pascal     | 108097/5304 | 16GB HBM2 @ 725 GB/s | 8.0          |
| V100-DGX-1        | Single node, 8 GPUs | NVLink-V2   | Intel Xeon ES-2689 | gcc-5.4.0 | Tesla-V100 | Volta      | 148997/7450 | 16GB HBM2 @ 900 GB/s | 9.0          |
| DGX-2             | Single node, 16 GPUs | NVSwitch    | Intel Xeon P-8168 | gcc-7.3.0 | Tesla-V100 | Volta      | 148997/7450 | 16GB HBM2 @ 900 GB/s | 9.0          |
| SLI               | Single node, 2 GPUs | NVLink-SLI  | Intel Xeon ES-2680 | gcc-4.8.5 | RTX-2080 | Turing     | 100687/5146 | 8GB GDDR6 @ 448 GB/s | 10.0         |
| SummitDev         | 54 nodes, 4 GPUs/node | NVLink-V1   | IBM Power-8      | xlc-13.1.6 | Tesla-P100 | Pascal     | 108097/5304 | 16GB HBM2 @ 725 GB/s | 8.0          |
| Summit            | 4600 nodes, 6 GPUs/node | NVLink-V2 | IBM Power-9      | xlc-16.1.1 | Tesla-V100 | Volta      | 148997/7450 | 16GB HBM2 @ 900 GB/s | 9.2          |

2.1 PCIe

Peripheral-Component-Interconnect-Express-Bus (PCIe), is a high-speed serial computer expansion bus standard. Traditionally, a GPU-integrated system connect one or multiple GPU devices to the CPUs via PCIe. However, compared to the interconnect between CPU and DRAM, PCIe is much slower. It often becomes a major performance bottleneck for GPU-acceleration [8], [9], [10]. Such a condition exacerbates when PCIe based GPU P2P communication is adopted [4].

The dash-lines in Figure 1(A) illustrate how the eight GPUs are interconnected by PCIe (and QPI) in DGX-1. As is shown, the PCIe network in DGX-1 forms a balanced tree structure, e.g., GPU-0 and GPU-1 are connected via a PCIe switch. The switch is further connected to CPU Socket-0. Similar scenarios apply to other GPUs. Finally, the dual CPU sockets are bridged by QuickPath Interconnect or QPI [11]. PCIe in DGX-2 also form a tree-based topology, adopts two-level PCIe switches, as shown in Figure 4.

2.2 NVLink-V1

Known as the first generation of NVLink, NVLink-V1 is a wire-based communication interface for near-range devices based on High-Speed-Signaling-Interconnect (NVHS) [1], [12]. It supports P2P communication that enables CPU-GPU or GPU-GPU linking. It allows direct read and write on remote CPU’s host-memory and/or peer GPU’s device-memory. Remote atomic operations are also feasible. NVLink is bidirectional; each link consists of two sublinks — one for each direction. Each sublink further contains eight differential NVHS lanes. An embedded clock is integrated for transmission. The packet size varies from 16 bytes to 256 bytes (one 128-bit flit to sixteen 128-bit flits). The communication efficiency is strongly correlated to the packet size. Overall, it is reported to be twice as efficient as PCIe [12].

An NVLink can be viewed as a cable with two terminal-plugs whereas each GPU incorporates several NVLink slots. How these slots are connected via the NVLink cables dictate the topology and bandwidth of the GPU network. Multiple cables can be ganged together to enhance bandwidth when they are linking the same endpoints. A Pascal-P100 GPU has quad NVLink slots. Therefore, for a dual-GPU system, a direct setting would be two GPUs connected by four NVLinks, leading to 4× bandwidth of a single link.

P100-DGX-1: The GPU network topology for DGX-1 is known as Hypercube Mesh. As shown in Figure 1(A), each GPU occupies a corner of the cube and all the 12 edges are NVLink connections. For the upper and lower planes, the diagonals are also connected, forming two fully-connected subsets. Such a topology design is balanced, with stronger connectivity inside a plane. In other words, accessing within a plane is UMA, while accessing nodes across planes leads to NUMA (when they are not directly linked, e.g., from GPU-0 to GPU-7). In fact, NVLink is not self-routed when the two terminals are not directly linked. It relies on explicit routing through a user-specified intermediate node.

SummitDev: The interconnect topology inside a machine node in SummitDev is illustrated in Figure 2(A). As can be seen, the four P100 GPUs per node are partitioned into two subsets; two GPUs per subset. A subset, together with a Power-8 CPU socket, constituting a triple-node fully-connected subnetwork. Every two nodes (either CPU or GPU) in a subnetwork are connected by two NVLink-V1 links. The two subnetworks communicate via an X-Bus at 38 GB/s. Note, unlike DGX-1, there is no direct connection between GPUs from separated subnetworks, as all the four NVLink slots of the P100 GPUs have already been occupied.

2.3 NVLink-V2

The second generation of NVLink improves per-link bandwidth and adds more link-slots per GPU: in addition to 4 link-slots in P100, each V100 GPU features 6 NVLink slots; the bandwidth of each link is also enhanced by 25%. Besides, a low-power operating mode is introduced for saving power in case a link is not being heavily exploited. The extra two link-slots have enabled certain alternation to the original network topology.

V100-DGX-1: Shown in Figure 1(B), the V100-DGX-1 does not choose to further strengthen the connectivity within a plane, but forming a fast Backbone Ring inside the Hypercube-Mesh network. Each connection in this ring enables 2× bandwidth compared to other links. We suspect...
this is to improve the efficiency of collective communication, as further discussed in Section 3.2.

**Summit:** Figure 3(B) shows the interconnect network topology for a machine node in Summit. The six GPUs are also organized in two subnetworks, but each with three GPUs. A subset, together with a Power-9 CPU socket, forming a quad-node fully-connect subnetwork. Every two nodes (either CPU or GPU) in a subnetwork are connected by two NVLink-V2 links. The two subnetworks are connected again via an X-Bus, at 64 GB/s. With one more node in the subnetwork, all the 6 NVLink slots per V100 GPU are fully utilized; there is no GPU direct connection between subsets.

### 2.4 NVLink-SLI

**Scalable Link Interface** (SLI) [13], or Crossfire [14], are traditionally used for graphic purposes only [15]. However, the recent Turing architecture GPUs (e.g., TU102, TU104) bring with them a new form of high-speed multi-GPU bridge, based on the NVLink-V2 interconnect technology. The bridge pairs up two GPUs so they can communicate with each other and co-render games, co-run GPGPU tasks, or co-share GPU memory spaces. In our SLI platform, the TU104 based RTX2080 GPU offers one x8 NVLink-V2 links, with up to 25 GB/s per direction per link, delivering an aggregate bidirectional bandwidth of 50 GB/s. Only two-way NVLink-SLI is supported for Turing GPUs.

### 2.5 NVSwitch

**NVSwitch** [15] is proposed mainly to address all-to-all communication in many emerging applications such as deep neural network training. NVSwitch currently only appears in DGX-2. The topology for NVSwitch and PCIe in DGX-2 are shown in Figure 3 and Figure 4 respectively. NVSwitch is an NVLink-V2 based switch chip for intra-node communication, featuring 18 ports of NVLink per switch. Shown in Figure 3 there are two baseboards; each contains 6 NVSwitches and hosts 8 GPUs. This is because a V100 GPU incorporates 6 NVLink slots, being able to connect to 6 NVSwitches simultaneously, each target per link, at 50 GB/s bidirectional bandwidth. Each NVSwitch is a 18x18 fully connected non-blocking crossbar: (1) 8 of the 18 ports are used for intra-baseboard communication, which means any of the 8 GPUs on one baseboard can talk with any other GPUs on the same baseboard at a full bandwidth of 50 GB/s × 6 switches =300 GB/s via a single NVSwitch hop; (2) Another 8 of the 18 ports are used to connect to the opposite baseboard, meaning that each of the GPUs on one baseboard can talk to any GPUs on the other baseboard also at a full bandwidth of 300 GB/s, but through 2 NVSwitch hops. The baseboard-to-baseboard raw bisection bandwidth is thus 25 GB/s × 8 links/switch × 6 switches=2.4 TB/s; (3) The left 2 ports per NVSwitch are reserved (e.g., the red circle in Figure 3).

To keep data integrity, **Cyclical Redundancy Coding** (CRC) is imposed to detect NVLink transfer errors and replay the transfer when necessary. **Error-Correcting Codes** (ECC) is enabled for the datapaths, routing, and state structures. In addition, final hop-address fidelity checks and buffer over/under-flow checks can be enforced in NVSwitch. To avoid illegal out-of-range access, a fabric manager monitors the routing tables for each particular application.

### 2.6 InfiniBand with GPUDirect-RDMA

**GPUDirect InfiniBand**

**GPUDirect InfiniBand:** We will not discuss InfiniBand itself since it is already widely used for HPC platforms today and has been extensively studied. Instead, we focus on its relation with GPU. Since the Kepler architecture, NVIDIA GPUs have introduced **GPUDirect-RDMA** [18] (Correspondingly, AMD proposed **ROCn-RDMA** [19]). It enables third-party PCIe devices, especially the IB Host-Channel-Adapter (i.e., HCA) to directly access GPU device memory via PCIe without any assistance from CPU or staging through the main memory, which significantly improves the efficiency of inter-node GPU communication. To achieve IB RDMA, GPU vendors offer an OS kernel extension to return a DMA bus mapping for GPU device memory. When a user creates an IB region, it signals the IB driver with the target address of the GPU device memory. IB driver then calls a routine to obtain the DMA mapping. Finally, a normal IB virtual memory structure is returned to the user program as if it targets normal CPU memory. GPUDirect-RDMA is enabled for both SummitDev and Summit.

### 3 GPU INTERCONNECT MICROBENCHMARKING

We evaluate the basic characteristics of the six GPU interconnects using the microbenchmarks (listed in Table 2) from the **Tartan Benchmark Suite** [24] on the platforms listed in Table 1 focusing on both **Peer-to-Peer (P2P)** and **Collective (CL)** communication patterns. For intra-node P2P, we especially concentrate on assessing the new node-level NVLink, NVSwitch and NV-SLI technologies in terms of topology, latency, bandwidth, efficiency on message size and NUMA effects. For inter-node P2P, we discuss properties such as latency, bandwidth and efficiency on message size. We use `cudaEvent` to measure the latency and calculate the bandwidth.
3.1 Intra-Node P2P Communication

3.1.1 Start-up Latency

Figure 5 shows the start-up communication latency (i.e., raw latency for transmitting the shortest message) among arbitrary pair of GPUs via PCIe and NVLink for the P100 and V100 DGX-1 platforms. As already mentioned, NVLink is not PCIe self-routed; for GPUs that are not directly connected by NVLink (e.g., G0 and G5 in Figure 1), there are two routing paths that only require a single transit (e.g., from G0 to G5, either G1 or G4 can be the router). In such scenarios, Figure 5 shows the path exhibiting shorter latency.

PCIe Latency: Figure 5(A) and (B) demonstrate that the communication latency for accessing different pairs of GPUs via PCIe are similar, implying that no NUMA effects appear in latency through PCIe. In other words, the three types of latency by going through one PCIe switch (e.g., G0 and G1), across local CPU socket (e.g., G0 and G2), and across the QPI bridge (e.g., G0 and G6) in Figure 1 are roughly the same. Meanwhile, comparing Figure 5(A) and (B), the PCIe latency is increased slightly (e.g., from green to light blue) from P100-DGX-1 to V100-DGX-1. As the bandwidth keeps unchanged, this may suggest a deeper communication pipeline design in V100-DGX-1 with Little’s Law [26].

NVLink V1&V2 Latency: Compared to PCIe in Figure 5(A) and (B), NVLink in Figure 5(C) and (D) shows significant NUMA effects. For nodes that are directly connected, the latency is around 9µs; for nodes that require manual routing, the latency is increased by about 2x for P100-DGX-1 and 3x for V100-DGX-1. Again, we observe that NVLink-V2 exhibits higher latency than NVLink-V1, potentially due to a deeper pipeline or lower operating frequency.

NV-SLI Latency: Figure 8 shows the latency for PCIe and NV-SLI in the SLI platform. For the dual-GPU system, there are three latency levels: local access which is about 5µs; NV-SLI access to the opposite GPU which is about 8µs; and PCIe access to the opposite GPU, which is about 13µs. Note, the two GPUs are directly linked by NV-SLI without any intervention from other units such as CPU, DMA, etc.

NVSwitch Latency: Figure 11 shows the latency for PCIe and NVSwitch in the DGX-2 platform. There are in total 16 GPUs in the system, so the grid is much finer. The pattern is very regular: all the remote access are homogeneous, either for PCIe or NVSwitch, confirming that NVSwitch is all-to-all fully-connected. Although accessing GPUs on the other baseboard incurs two switch hops, we can see that the difference of latency is very small, almost negligible.

3.1.2 Sustainable Bandwidth

Figure 6 and 7 illustrate the uni- and bidirection sustainable bandwidth for PCIe and NVLink of the two DGX-1 platforms, respectively. Figure 9 and 10 show the uni- and bidirection bandwidth for PCIe and NV-SLI in the SLI platform. Finally, Figure 12 and Figure 13 show the uni- and bidirection bandwidth for PCIe and NVSwitch in DGX-2.

PCIe Unidirectional Bandwidth: From Figure 6(A) and (B), we can observe slight NUMA effects on PCIe accesses: two GPUs sharing the same PCIe switch (e.g., G2 and G3 in Figure 1) exhibit lower bandwidth in the measurement. For other GPUs, no matter whether sharing the same socket, the bandwidth appears to be the same. Similar effects have also been observed in Figure 12(A), in which four GPUs sharing the same Level-2 PCIe switch (e.g., G0 to G3 in Figure 4) deliver lower bandwidth.

PCIe Bidirectional Bandwidth: The NUMA effects on bidirectional bandwidth for GPUs sharing the same PCIe switch...
(e.g., Figure 7(A) and (B), Figure 13(A)) are much more prominent than those on unidirection bandwidth. The PCIe NUMA effect here is an interesting novel observation: it describes a scenario that nearby access presenting lower performance than remote access. We label such a NUMA effect as “anti-locality”. To the best of our knowledge, few existing work have discussed this phenomenon before, without mentioning leveraging it for performance tuning practice. The anti-locality effect is possibly due to the unbalanced physical signal paths on the PCIe-switch chipsets [27]. Note, this PCIe anti-locality effect is only observed for bandwidth.

NVLink Unidirection Bandwidth: The NVLink scenario is more complicated. For NVLink-V1 in Figure 3(C), there are three connection types: local access, neighboring nodes directly connected by NVLink, and remote nodes requiring additional routing, corresponding to the topology illustrated in Figure 1(A). For NVLink-V2 in Figure 3(D), there are four connection types: local access, close neighboring nodes connected by dual links (i.e., the “backbone ring”), general neighboring nodes connected by one link, and remote nodes, corresponding to the topology in Figure 1(B). As such, there are three types of NUMA effects for NVLink:

- NUMA among neighbors and remote nodes for NVLink-V1 and V2 on both latency and bandwidth.
- NUMA among neighbor nodes for NVLink-V2. This is due to different number of links (either 1 or 2) to connect neighboring nodes in V100-DGX-1. Typically, the latency remains similar but these two types of links introduce bandwidth difference.
- NUMA among remote nodes for NVLink-V2. This is caused by the choice of routing. Figure 1(C) and (D) show the bandwidth disparity for choosing different paths.

NVLink Bidirection Bandwidth: The three types of NVLink NUMA effects for bidirectional bandwidth are much more obvious than that for unidirectional bandwidth, as discussed in the caption of Figure 7.

NV-SLI Unidirection Bandwidth: Since NV-SLI only incorporates two GPUs, where the communication is symmetric, showing no NUMA effect in Figure 3(B).

NV-SLI Bidirection Bandwidth: The bidirectional condition is similar to unidirection condition, except that the bandwidth doubles, as shown in Figure 10(B).

NVSwitch Unidirection Bandwidth: Shown in Figure 12(B), the bandwidth for all remote access through NVSwitch are consistent or UMA, implying that one more NVSwitch hop does not degrade bandwidth.

NVSwitch Bidirection Bandwidth: Bidirectional bandwidth condition is similar, except that the bandwidth doubles, as shown in Figure 13(B).

3.1.3 Routing

For all the GPU interconnects we discuss here, only the one for remote access in the DGX-1s via NVLink may require explicit routing. Here, we further explore the NUMA effects on alternative routing choices. For demonstration purposes, we take G0 in Figure 7 as the source node for P2P communication. There are three remote nodes for G0: G5, G6 and G7. From G0 to G5, either G1 or G4 can be specified for routing. From G0 to G6, either G2 or G4 can be selected; and from G0 to G7, either G3 or G4 can be selected. We use microbenchmarks from Tartan to measure the latency, unidirection bandwidth and bidirection bandwidth of each routing path from G0 to G5, G6, G7 respectively on both DGX-1 platforms. Figure 14 shows the results for unidirection and bidirection bandwidth. As can be seen, for NVLink-V1 in P100-DGX-1, there are no NUMA effects; all the bars appear in the same height. This is because the NVLinks in P100-DGX-1 are isomorphic — any connection incorporates just one link. However, for NVLink-V2 in V100-DGX-1, different
3.1.4 Efficiency on Message Size

Figure 15 illustrates the P2P latency, unidirectional and bidirectional bandwidth with respect to message size via PCIe, NVLink-V1 and V2 for P100-DGX-1 and V100-DGX-1. Figure 16 illustrates the plot for NV-SLI and PCIe in the SLI-system. Figure 17 illustrates the plot for NVSwitch and PCIe in the DGX-2 system.

Latency: The latency remains unchanged for data communication less than or equal to 16KB for P100-DGX-1 (except local access). For V100-DGX-1, this value increases to 64KB, suggesting higher link bandwidth to saturate and deeper communication pipeline on NVLink-V2. The conditions are similar for SLI and NVSwitch in the SLI and DGX-2 platforms. The interesting observation is that in Figure 17 there is slight divergence for PCIe-local (including PCIe-neighbor and PCIe-one-switch) and PCI-remote access latency with large messages (i.e., ≥4MB).

Bandwidth: For unidirectional bandwidth, it can be seen that the interconnect starts to saturate at about $2^{22} = 4$MB for both NVLink-V1 and V2, implying that to reach the optimal sustainable bandwidth of the interconnect, one needs at least 4MB data to transmit at a time. This is also true for bidirectional bandwidth in Figure 15(E) and (F). In addition, observing the fact that the latency starts to increase at 16KB and 64KB, but the bandwidth begins to saturate at 4MB, implies that from 64KB, we suffer from extra delay, but still gain overall bandwidth improvement until the bandwidth saturation point. For DGX-2 NVSwitch unidirectional and bidirectional bandwidth in Figure 17(B) and (C), we see that NVSwitch-one-hop and NVSwitch-two-hop curves are fully aligned, confirming that accessing remote baseboard imposes no extra overhead. For PCIe bidirectional bandwidth in Figure 17(C), the observation is that when message size is larger than 64KB, the PCIe anti-locality effect appears: PCIe-remote access delivers higher bidirectional bandwidth than PCIe-neighbors (L1 & L2). In fact, the anti-locality effect also exists between L1-PCE-neighbors and L2-PCE-neighbor in DGX-2, as can be seen, the bandwidth of L2-PCE-neighbor is slightly better than L1-PCE-neighbor, showing a second level anti-locality. Finally, all GPU local access bandwidth in these figures stagers at about 4MB, possibly due to exceeding page boundary.

3.2 Intra-Node Collective Communication

Different from P2P communication only including a single sender and receiver, collective communication (CL) involves multiple senders and receivers so it is more complicated. CL generally follows certain patterns, including broadcast, scatter, gather, all-gather, reduce, all-reduce, all-to-all, etc. It is extensively used in many key applications such as deep learning, molecular dynamics, graph analytics, etc.

Efficiently implementing CL communication is challenging because (a) it needs to understand the underlying hardware network topology in order to enable orchestrated mapping; (b) it needs to handle the issue of synchronization, overlapping and deadlock; and (c) performance metrics can differ subject to application features (e.g., latency-oriented for small transfers but bandwidth-oriented for large transfers). To relieve these burdens from users, NVIDIA provides Collective Communication Library (NCCL) [22], [23], using similar primitives as MPI collectives, while AMD offers RCCL [25]. NCCL currently supports five CL patterns: broadcast, all-gather, reduce, all-reduce, and reduce-scatter.

To offer the maximum bandwidth, NCCL constructs ring network among the communication participants so that broadcasting and reduction can be efficiently realized by partitioning data into small chunks, and transmitting them along the ring in a pipeline fashion. It is claimed that the ring algorithm can provide near optimal bandwidth for most of the standard CL operations and can be easily applied to various network topology [4]. Figure 18 as an example, describes how a ring-network is constructed for PCIe, NVLink-V1 and NVLink-V2 in DGX-1s, respectively.

There are two versions of the NCCL library: NCCL-V1 [22] is opensource but only supports intra-node PCIe/QPI interconnect network. NCCL-V2 [22] is closed-source but supports NVLink, PCIe, NVSwitch, NV-SLI, IB and IP networks, and can automatically integrate them to maximize overall bandwidth. Although the combination improves overall performance, it also introduces difficulty in independently measuring the CL communication efficiency for a particular interconnect. Consequently, NCCL-V1 is employed for PCIe CL evaluation while NCCL-V2 is adopted for NVLink/NVSwitch/NV-SLI CL evaluation.

3.2.1 DGX-1 CL Communication

CL Latency: Figure 19 illustrates CL communication startup latency with respect to the number of GPUs involved for NCCL-V1 and V2 on the two DGX-1 platforms respectively, corresponding to PCIe/QPI and NVLink. We have the following observations: (1) latency increases with participating GPUs almost in a linear fashion; (2) comparing (A) and (C), (B) and (D), the behaviors of NCCL-V1 and V2 on the two DGX platforms are similar; (3) comparing (A) (B) with (C) (D), the latency of NVLink increases faster than PCIe (except all-reduce), while NVLink-V2 increases faster than NVLink-V1; (4) for PCIe, all-reduce shows the largest latency. The disalignment of the curves in (B) and (D) for odd number of GPUs (e.g., 3, 5) is likely due to NCCL algorithm design rather than NVLink-V2 P2P NUMA effects, as will be discussed later.

CL Bandwidth: Figure 20 shows CL's sustainable communication bandwidth with increased number of GPUs under 1GB payload. As can be seen, (1) for PCIe, CL bandwidth decreases with more GPUs, which is due to bus contention in a tree-network, see Figure 18(A); (2) for NVLink, however, CL bandwidth essentially increases with more GPUs due to more connected links in a hypercube mesh network, see Figure 18(B) and (C); (3) PCIe and NVLink behavior on P100-DGX-1 and V100-DGX-1 are in similar trend. However, NVLink-V2 exhibits significantly better bandwidth with 4 GPUs (~1.6x) and 8 GPUs (~2x) compared to NVLink-V1, showing the strength of dual-links and backbone ring
reduce Latency (us) Latency (us) Latency (us) Latency (us) (A) P100-DGX-1 P2P Latency (B) V100-DGX-1 P2P Latency (C) P100-DGX-1 Unidirectional BW (D) V100-DGX-1 Unidirectional BW (E) P100-DGX-1 Bidirectional BW (F) V100-DGX-1 Bidirectional BW

Fig. 15: P2P communication latency, unidirectional and bidirectional bandwidth with increased message size via PCIe and NV-Link for DGX-1.

Fig. 16: P2P communication latency, unidirectional and bidirectional bandwidth with increased message size via PCIe and NV-SLI for the SLI-system.

Fig. 17: P2P communication latency, unidirectional and bidirectional bandwidth with increased message size via PCIe and NVSwitch for DGX-2.

Fig. 18: NCCL Rings for PCIe, NV-Link-V1 and NV-Link-V2 Interconnect. (A) for PCIe, the ring is to traverse the binary-tree network; (B) for NV-Link-V1, there are two independent rings, marked in red-solid line and blue-dash line; and (C) for NV-Link-V2, the lines with 2 links form a fast ring (i.e., the backbone network) while the lines with 1 link form a slow ring.

CL Efficiency on Message Size: Figure 19 shows CL bandwidth with respect to message size increasing from 8B to 1GB for 8 GPUs. As can be seen, for PCIe, CL bandwidth saturates at about $2^{24} = 16$MB; whereas for NV-Link, bandwidth saturates around $2^{28} = 256$MB. Again, the five CL patterns exhibit similar trend in terms of bandwidth when scaling the message size.

3.2.2 NV-SLI CL Communication

CL Latency and Bandwidth: Since the SLI-system contains only two GPUs, we use histogram figures to show the latency and bandwidth for the 5 CL communication patterns. As can be seen in Figure 22 and 23, the latency for NV-SLI is similar, around 18$\mu$s; but for PCIe, reduce and all_reduce show significantly lower latency than the other three, even less than on NV-SLI. The bandwidth is similar for both PCIe and NV-SLI, except that reduce_scatter showing poorer bandwidth than the others on both PCIe and NV-SLI.

(Figure 19) (4) the NUMA effects appear quite significant with 5 GPUs, implying that there may be a congestion when forming a NCCL ring among 5 GPUs. One should avoid adopting 5 GPUs in their application setup.
CL Efficiency on Message Size: Figure 24 shows CL bandwidth with respect to message size for the two GPUs. Both PCIe and NV-SLI bandwidth start to saturate at about $2^{20} = 1$MB. The figure confirms that reduce_scatter bandwidth is lower than the others for large message size, but at the same time indicating that all_gather delivers a relative low bandwidth with the same message size before saturated.

3.2.3 NVSwitch CL Communication

CL Latency and Bandwidth: Figure 25 illustrates CL communication latency with respect to the number of GPUs on DGX-2, corresponding to PCIe and NVSwitch. As can be seen, due to UMA for NVSwitch, the five curves in Figure 25(B) are rather aligned. Figure 25(B) confirms the long latency for all_reduce on tree-based PCIe interconnect, in consistent with Figure 19(A) and (C). Also note that except all_reduce, the other CL primitives show lower startup latency on PCIe than on NVSwitch when the participating GPUs are more than three, implying that the advantage of NVSwitch (as well as NVLink) is on bandwidth rather than latency. This observation is confirmed in Figure 26. As can be seen, NVSwitch shows tremendously higher bandwidth than PCIe, particularly for reduce, all_reduce and broadcast. reduce_scatter and all_gather show staggering behavior on bandwidth for NVSwitch; the values are much better with 2, 4, 8 and 16 GPUs than other numbers of GPUs, in consistent with NVLink scenarios in Figure 20(B)/(D). Since NVSwitch is UMA, it implies that this staggering issue is not due to interconnect topology but NVCL’s implementation.

3.3 Inter-Node P2P Communication

We measure the latency and bandwidth of inter-node P2P communication on SummitDev Supercomputer 29 and Summit Supercomputer 6 from Oak Ridge National Laboratory. SummitDev is a supercomputer system with 54 nodes. Each node contains two IBM Power-8 CPUs and four NVIDIA P100 GPUs. The GPU interconnect is NVLink-V1. Summit features 4,608 nodes, each with two IBM Power-9 CPUs and six NVIDIA V100 GPUs. The GPU interconnect is NVLink-V2. Both SummitDev and Summit support GPUDirect.

For inter-node P2P, we conduct our measurements under five configurations: (i) GPUDirect-RDMA is to directly access GPU memory among nodes with GPUDirect enabled (“GPUDirect” here refers to a system option. On SummitDev,
it is `OMPI_MCA_pml_pami_enable_cuda=1`. On Summit, it is `−smpiargs="−gpu"`). (ii) PinnedMem-GPUDirect is to first copy data from GPU memory to the pinned host memory, then transfer the data to another node’s pinned host memory and finally copy to the targeted GPU memory, with GPUDirect enabled; (iii) PinnedMem is similar to (ii) but with GPUDirect disabled; (iv) UnpinnedMem-GPUDirect is to copy via host unpinned memory with GPUDirect enabled; and (v) UnpinnedMem is similar to (iv) but with GPUDirect enabled.

The measured latency and bandwidth with respect to message size (from 4B to 1GB) under the five testing scenarios are illustrated in Figure 28 and 29 for SummitDev and Summit, respectively. For better illustration, the latency curves use log-scale Y-axis while bandwidth curves use normal-scale Y.

**SummitDev:** From Figure 28 we draw the following observations: (i) Until $2^{12} = 4KB$, there is little difference among the five curves in terms of both latency and bandwidth; (ii) GPUDirect-RDMA shows the worst performance in the range from 4KB to 64KB for latency and from 4KB to 256KB for bandwidth, especially at 32KB. This is possibly due to limitations in some chipsets for P2P access through the CPU/IOH [30]. (iii) From 4MB on, GPUDirect-RDMA shows its advantage on bandwidth and obtains its optimal bandwidth — 12GB/s at 64MB. However, this is still lower than the PinnedMem-GPUDirect scheme, which demonstrates more than 14GB/s sustainable bandwidth with large message size; (v) it is also interesting to observe that the bandwidth of GPUDirect-RDMA actually degrades dramatically after 64MB, implying that breaking large messages into multiples of 64MB could be a better way to transfer in practice on SummitDev.

**Summit:** Regarding Figure 29 we have the following observations: (i) Unlike SummitDev, GPUDirect-RDMA shows the best performance among the five configurations on Summit: it always delivers the lowest latency, especially for small message size ($\leq 1MB$); it always exhibits the highest bandwidth, especially for large message size ($\geq 16KB$). Meanwhile, the strange performance drop (i.e., latency increase and bandwidth degradation) in Figure 28 for SummitDev, disappear in Figure 29 for Summit. These two points suggest that the technology of GPUDirect has been improved significantly from SummitDev to Summit, and becomes the best choice for GPU inter-node communication.

### 3.4 Inter-Node Collective Communication

Regarding inter-node collective communication, we measure the latency and bandwidth with respect to the number of participant nodes on both SummitDev and Summit. We tune the number of nodes from 2 to 8, with 1 GPU per node being utilized. Similarly, the startup latency is measured with 4B data transfer while the sustainable bandwidth is measured with sufficiently large data transfer (1GB). The latency results are shown in Figure 30 (A) and Figure 31 (A) for SummitDev and Summit, respectively. The bandwidth results are shown in Figure 30 (B) and Figure 31 (B).
bandwidth change with increasing message size is shown in Figure 30 (C) and Figure 31 (C). We tried to illustrate the difference between enabling and disabling GPUDirect, but found that the results are in fact very similar. We suspect that GPUDirect-RDMA is internally enabled in NCCL-V2.

**CL Latency:** As shown in Figure 29 (A), for SummitDev’s IB fat-tree network, the latency-change for performing the five CL operations remains flat when scaling the number of nodes, except all-reduce. A similar observation is also drawn in Figure 31 (A) for Summit, the divergence is much less for all-reduce. This may imply that it is a joint-effect of algorithm implementation in NCCL and the interconnect technology of GPUDirect.

**CL Bandwidth:** In terms of bandwidth in Figure 30 (B), similar to NVLink (Figure 29 (B) and (D)), strong NUMA effects emerge under 3 and 5 nodes for reduce_scatter and all_gather on SummitDev. And for Summit, this happens under 3, 5, 6, 7 nodes in Figure 31. Nevertheless, the bandwidth overall remains unchanged. This is different from the bandwidth scenarios exhibited by both PCIe (decreasing) and NVLink (increasing) in the inter-node P2P communication study.

**CL Efficiency on Message Size:** Finally, the bandwidth for the five CL operations converge and saturate around 32/64MB message size, demonstrating nearly 16/32 GB/s sustainable peak bandwidth on SummitDev in Figure 31 (C), and Summit in Figure 31 (C), respectively. Overall, Summit delivers much better GPU inter-node communication performance than SummitDev.

### 4 GPU INTERCONNECT BENCHMARKING

The microbenchmarking exhibit some basic characteristics of modern GPU interconnects. However, in terms of real multi-GPU applications, their impact remains unknown. In this section, we use the Tartan Benchmark Suite 25 to evaluate the impact of the GPU interconnect. The applications are listed in Table 3. Particularly, we focus on two aspects: (1) the impact of a faster GPU interconnect such as NVLink, compared with PCIe on intra-node scale-up applications; (2) the impact of GPUDirect-RDMA on inter-node scale-out applications. We perform two types of scaling measurement: (a) strong scaling, which fixes the problem size and measures the time reduction when increasing the number of GPUs; (b) weak scaling, which measures the time reduction when increasing the number of GPUs with fixed problem size per GPU. For overall performance, we use the entire application speedup (measured by CPU-side time command for whole application elapsed-time) as the performance metric, making a fair comparison across applications. For scale-up applications, we use the vendor-provided nvprof to measure the three types of GPU communication: HostToDevice (H2D), DeviceToHost (D2H) and DeviceToDevice (D2D) in order to gain more knowledge about the underlying communication.
pattern. All the reported data points of the figures in this section are the average results of multiple times’ execution.

4.1 Intra-node Scale-up

For intra-node scale-up scenarios, we evaluated the seven scale-up applications on P100-DGX-1 and V100-DGX-1, with and without NVLinks. Since many of these applications are hard-coded to leverage all the available GPUs in the system, we configure the system environment through export CUDA_VISIBLE_DEVICES=× to manipulate the number of GPUs being visible to the applications. Figure 32 and 33 illustrate the break out of the latency for the three types of communication (i.e., H2D, D2H, and D2D) regarding the original implementation (i.e., Baseline) and our modification (i.e., via NCCL) as described in Section IV-A, for intra-node strong and weak scaling on P100-DGX-1. The intention is that the original implementation will show the performance of PCIe, while our modification would convert a big portion of CPU-GPU communication to GPU-GPU communication, so as to show the performance gain from NVLink. Figure 34 and 35 show the results on V100-DGX-1. The performance change of the entire application is given in the supplementary file due to space limitation.

Impact of NVLink. Although our observation from microbenchmarking in Section 3 show that NVLink can significantly improve inter-GPU communication efficiency, based on these figures, it is clear that those improvements do not directly transform into overall communication latency reduction, nor the whole application speedup (see the supplementary file); except CSM and GMM, there is not very significant difference between the Baseline and NCCL bars for both platforms. There are several reasons behind this. First, based on our experience on assessing the over 50 multi-GPU application candidates, most of those scale-up cases are based on master-slave programming model, where the CPU is the master, handling the sequential portions of code and GPUs are the slaves, processing the parallel portions. Under this model, communication only occurs between CPU and GPUs; no inter-GPU transaction is presumed. In addition, the CPU-GPU communication is also highly optimized. This is true for CSM, GMM, KMN, MTC, PLN and TRK. For CSM, PLN, GMM, and TRK, we manage to convert some CPU-GPU communication into GPU-GPU communication through NCCL. As can be seen, for CSM, the effect is obvious: a large portion of the D2H and H2D communication is replaced by D2D. For GMM, although we gained ~6% latency reduction, from the `nvprof` trace file, we did not observe any D2D communication transactions (but rather D2H and H2D) before/after NCCL’s `BroadcastKernelSmall()` kernels. This is potentially caused by the flexible design strategy adopted by NCCL-V2 to efficiently leverage all available interconnect bandwidth (Section III-B). When the data size per transmission is small, it may not choose D2D communication via NVLink. Similar conditions also observed for PLN and TRK. For KMN and MTC, there is no GPU-GPU communication at all. The D2D in KMN is actually local data movement within the same GPU. For CNN, the figures do not show bars under 8 GPUs because CNN implementation requires arbitrary data copying among arbitrary peers at runtime, which currently fails when 8 GPUs are utilized. However, since not every two GPUs are directly connected by NVLink under the current NVLink topology. As it internally uses `cudaMemcpyDefault` and `unified-space` for data copying across GPUs, NVLink is already internally enabled by CUDA for an NVLink-equipped machine such as DGX-1. We tried to modify the `CUDA` code so that PCIe can be essentially enforced but did not run correctly with success. This is why the two bars of CNN exhibit the same value for all four figures. It is also interesting to see that when more than 4 GPUs participant in the computation, the D2H communication increases dramatically, potentially due to the gradient merging overhead in the backpropagation. Secondly, since today’s scale-up applications are mostly based on the master-slave programming model, communication often only accounts for a small fraction of the total execution time, let alone the inter-GPU communication which tended to be avoided previously when creating applications, thus hardly become the system bottleneck. Finally, employing NVLink (either P2P or CL) introduces additional overhead (e.g., enable/disable peer access, routing, NCCL initialization, etc).

To summarize, a faster GPU interconnect such as NVLink has been reported to be beneficial for accelerating modern deep-learning frameworks [31], [32]. However, regarding general GPGPU applications, without (i) replacing the underlying CPU-centric master-slave programming model by a more distributed parallelization model, or (ii) migrating the communication master role to a GPU (e.g., offloading GPU communication control from CPU to GPU via techniques such as NVSHMEM [33]), optimized inter-GPU communication via faster intra-node GPU interconnect such as NVLinks can hardly become significant enough to lift the entire application’s speedup. Therefore, we believe that this observation paves the road for developing interconnect-
friendly programming models for multi-GPU scale-up scenarios so that faster interconnect (e.g., NVLinks) can truly play a role in improving the overall application efficiency.

4.2 Inter-node Scale-out

For inter-node scale-out scenarios, we run the seven scale-out applications from Tartan on SummitDev and Summit (see Table 1), with each MPI rank binding to a node using only a single GPU. Similar to the discussion in Section 3.3, we measured the overall application performance under five scenarios: GPU Direct-RDMA, PinnedMem-GPU Direct, PinnedMem, UnpinnedMem-GPU Direct and UnpinnedMem.

Figure 35 and 36 illustrate the speedups with respect to single-node UnpinnedMem for strong and weak scaling tests, respectively, on SummitDev. Figure 37 and 38 illustrate the speedups for strong and weak scaling on Summit. As can be seen, compared with the intra-node scale-up cases, the MPI-based inter-node scale-out applications exhibit much better scaling behavior in both strong and weak scaling tests, implying that compared with the intra-node fast interconnect, the inter-node network is much easier to become the system bottleneck. Improving inter-node network speed can lead to significant performance gain for multi-GPU applications.

Regarding to GPU Direct-supported IB interconnect, we have the following observations: (i) Enabling GPU Direct can bring immediate performance enhancement, whether or not the transmitted data reside in CPU memory or GPU memory; (ii) Using pinned memory is also beneficial, especially in coordination with GPU Direct enabled; (iii) GPU Direct+RDMA can be especially helpful in certain applications (e.g., BRQ and MAM) for SummitDev, and overall for Summit. This is potentially due to the significant improvement on GPU Direct-RDMA performance in Summit than SummitDev; (iv) Overall, the multi-node performance scaling on Summit is less obvious than on SummitDev, especially for strong scaling. This is not due to any degradation in communication efficiency in Summit, but essentially the reverse: Summit improves the fundamental communication bandwidth, which enhances the baseline performance. That is why the relative speedups drop on Summit, compared to SummitDev. Overall, we suggest the application developers to adopt PinnedMem-GPU Direct for SummitDev, and GPU Direct-RDMA for Summit.

All in all, for scale-out applications to benefit from a faster inter-node interconnect (e.g., IB-RDMA), the major difficulty is not from the hardware or the application, but from the communication abstract interfaces such as MPI. If a new MPI implementation can internally integrate NCCL, further harvesting multi-GPU interconnect performance (e.g., NVLink and IB-RDMA) can be much more easier. Again, initiating communication completely on the GPU side without CPU intervention (e.g., via GPU Direct-Async or GPU-triggered networking) may also be critical for good GPU performance delivery.
Modern GPU interconnect technologies such as NVLink are claimed to be transparent but in reality it is more complicated to be leveraged for high performance. (1) NUMA effect. Among the five types of intra-node GPU interconnect techniques, PCIe, NVLink-V1 and V2 show strong NUMA effect in the tested platforms, due to various reasons including topology, position, connectivity, routing, sharing, chipset, etc. NVSwitch and NV-SLI show UMA. (2) Heterogeneity. All the tested platforms incorporate more than one type of interconnect network. These networks have their own characteristics and can work exclusively, concurrently, or cooperatively, depending on the system design. Therefore, one has to handle the interconnect heterogeneity: choosing one interconnect over the others (e.g., NVLink shows strong advantage on bandwidth rather than latency over PCIe), leveraging them simultaneously, or cooperatively integrate them as an inclusive solution. This is especially difficult at runtime. (3) Communication Efficiency. There are several factors restricting the delivery of optimal communication performance, including message size, system design (dual isolated subnetworks in Summit and SummitDev), hardware limitation (e.g., PCIe antilocality, GPUDirect-RDMA in SummitDev), and library implementation (e.g., NCCL on DGX-1 with 3 and 5 nodes). All these lead to the difficulties in leveraging modern GPU interconnect for high-efficient inter-GPU communication.

Our evaluation motivates the following research directions: (1) Developing novel multi-GPU programming models. Existing multi-GPU programming models rely on CPU-oriented parallel programming models, such as OpenMP and MPI, to manage multiple GPUs. Consequently, either there is a mismatch (e.g., CPU-master-GPU-slave model can hardly benefit from inter-GPU network), or there is a legacy in adopting new GPU interconnect technologies (e.g., integrating NCCL into MPI, as it is shown that NCCL delivers better communication efficiency than MPI on allreduce [36]). Therefore, new multi-GPU programming models are highly desired, especially those that are adaptive, portable, tractable, and being able to effectively address the complexity aforementioned. In addition, existing multi-GPU algorithms are usually designed to minimize or even eliminate communications, due to the huge performance gap between local access and remote access (e.g., via PCIe). With the emergence of new GPU interconnect, and foreseeing their fast development trend, it may be the right time to reconsider the role of inter-GPU communication when designing new parallel models and algorithms. (2) Developing practical multi-GPU performance models. This is for performance prediction, optimization, and analytics in multi-GPU application development and tuning. In addition, an appropriate performance model is crucial for GPU task al-
location, scheduling and migration in a shared environment (e.g., Cloud and HPC centers). (3) Developing new communication patterns and libraries for better matching the underlying interconnect and delivering high-performance. For example, regarding the dual-subnetwork interconnect topology for NVLink in Summit, it is worth to figure out how to efficiently distribute and exchange data among the two islands, taking data reuse and X-bus bandwidth into consideration. Give another example, a recent work shows that a 2D-Torus communication pattern can deliver better communication efficiency than NCCL’s ring pattern for all-reduce. This new pattern can be obviously migrated from inter-node to the intra-node NVLink interconnect in DGX-1s, or NVSwitch in DGX-2, where multiple communication ring-raths can be constructed. This is especially desired when porting traditional CPU-based HPC applications onto the new GPU-based exascale systems, such as Summit [6], Sierra [7] and Perlmutter [37]. As part of the community effort, we are planning to pursue these research directions in our future work with our past experience on GPU analytic modeling [56], [57], [58], [59], [60] and performance optimization [41], [42], [43], [44], [45], [46], [47], [48], [49], [50], [51].

6 Related Work

Intra-node GPU Computing. Spafford et al. [52] analyzed the NUMA effects in a multi-GPU node and provided optimization guidance. Kim et al. [53] proposed to rely on hybrid-memory-cubes (HMCs) to build a memory network for simplifying multi-GPU memory management and improving programmability. Wang et al. [54] presented a design to realize GPU-Aware MPI to support data communication among intra-node GPUs with standard MPI. Ben-Nun et al. [55] described an automatic multi-GPU partition framework to distribute workload based on their memory access patterns. Cabezas et al. [56] showed a software solution, including programming interfaces, compiler support and runtime, to partition GPU kernels for multi-GPU execution in a single node. Finally, Sun et al. [57] evaluated the potential performance benefit and tradeoffs of AMD’s Radeon Open Compute (ROC) platform for Heterogeneous System Architecture (IISA).

Multi-node GPU Computing. For MPI-based multi-node GPU computing, Wang et al. [58] introduced a MPI design that integrates CUDA data movement transparently with MPI. Gysi et al. [59] proposed a hardware approach to overlap computation and communication in a GPU cluster. Klenk et al. [60] analyzed the exascale proxy applications on their communication patterns and proposed a matching algorithm for GPUs to comply with MPI constraints. Awan et al. [61] proposed a pipelined chain design for MPI broadcast collective operations on multi-GPU nodes to facilitate various deep learning frameworks.

7 Conclusion

In this paper, we characterize and evaluate six types of modern GPU interconnects, including PCIe, NVLink-V1, NVLink-V2, NV-SLI, NVSwitch, and InfiniBand with GPU-Direct-RDMA, using the Tartan Benchmark Suite over six GPU servers and HPC platforms: NVIDIA’s P100-DGX-1, V100-DGX-1, DGX-2, RTX2080-SLI systems, and ORNL’s SummitDev and Summit supercomputers, covering both Peer-to-Peer and Collective communication patterns. We addressed four new types of NUMA effects for intra-node GPU communication, and proposed some insightful observations for enabling practical optimization guidelines. This evaluation study attempts to help the HPC community to push forward multi-GPU research and development, particularly the construction of more mature multi-GPU programming, execution, and performance models.

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