Two-Dimensional-Like Amorphous Indium Tungsten Oxide Nano-Sheet Junctionless Transistors with Low Operation Voltage

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In this work, we have successfully demonstrated the junctionless (JL) transistors with two-dimensional-like (2D-like) nano-sheet (NS) material, amorphous indium tungsten oxide (a-IWO), as an active channel layer. The influences of the different gate insulator (GI) materials and the scalings of GI thickness, a-IWO channel thickness, and channel lengths on the a-IWO NS JL transistors (a-IWO NS-JL Ts) have been studied for the purposes of low operation voltage (gate voltage ≤ 2V) and high performance. The 2D-like a-IWO NS-JL Ts exhibit low operation voltage, low source/drain (S/D) contact resistance (R\text{C}) and other key electrical characteristics, such as high field-effect mobility (\(\mu\text{Fe}\)), near ideal subthreshold swing (S.S.), and large ON/OFF currents ratio (I\text{ON}/I\text{OFF}). The remarkable device characteristics also make the proposed 2D-like a-IWO NS-JL Ts promising for system-on-panel (SoP) and vertically stacked (VS) hybrid CMOS applications.

As devices scaling continues, Si-based ultra-thin body (UTB) field-effect transistors (FETs) and FinFET with low leakage currents and good gate controllability allow gate/channel length reduction through Fin (body) thickness scaling. Furthermore, the single crystalline silicon (Si)/polycrystalline silicon (poly-Si)-based nanowires (NWs) and nano-sheet (NS) junctionless (JL) devices with low operation voltage and near ideal subthreshold characteristics have been proposed and demonstrated for lower thermal budgets and easier processes. Since the gradient of a doping concentration is absent, the issues of the sharp doping profile formation and the impurities diffusion are completely eliminated. Nevertheless, FETs/FinFET with sub-5nm technology node require sub-3nm-thick body for better channel controllability. Most Si-based devices with such an ultra-thin body thickness will face several challenges, including the control of channel thickness (T\text{ch}), high source/drain (S/D) parasitic resistance (R\text{SD}), and uniform S/D and channel heavy doping for JL FET devices. Therefore, as Si-based CMOS scaling approaches its limits, it is highly urgent and desirable to investigate other ultra-thin/two-dimensional (2D) channel materials with relatively wide band gaps and high mobility. Such ultra-thin/2D channel materials can potentially suppress short channel effects (SCEs) and achieve high ON/OFF currents ratio (I\text{ON}/I\text{OFF}) owing to good gate electrostatics and low leakage currents for digital circuit applications.

Recently, indium oxide (InO\text{x})-based transparent amorphous oxide semiconductor thin film transistors (TAOS TFTs) with wide band gaps have been developed and applied not only for display but also for other applications, like flexible electronics, optoelectronics, and mobile electronics owing to superior uniformity, low-temperature processes, and high field-effect mobility (\(\mu\text{Fe}\)). In the last few years, the vertically stacked (VS) hybrid complementary metal-oxide-semiconductor (CMOS) consisted of low-temperature c-axis aligned crystalline In-Ga-Zn-O (CAAC-IGZO) FETs with 60 nm technology node and p-channel SI MOSFETs with 65 nm technology node have been successfully fabricated and demonstrated. Back-end of line (BEOL) compatible nano-scaled CAAC-IGZO FETs with ultra-low OFF-state currents (I\text{OFF}) and SCE immunity are promising candidates for low power large-scale integration (LSI) and internet of things (IoT) applications. Although CAAC-IGZO FETs exhibit a \(\mu\text{Fe}\) ~10 cm\text{^2}/V-s, the \(\mu\text{Fe}\) and subthreshold swing (S.S.) of CAAC-IGZO FETs are degraded by increasing channel width. Consequently, further improvements in \(\mu\text{Fe}\) and the stability of the TAOS TFTs are urgently required to broaden their range of potential applications. To achieve these targets, an
amorphous indium tungsten oxide (a-IWO) semiconducting material with high mobility and stability, which is free from both Ga and Zn, was studied for an alternative choice to a-IGZO TFTs\textsuperscript{13–15}. We have successfully fabricated and demonstrated the low thermal budget 2D-like a-IWO NS JL transistors (a-IWO NS-JLTs) in bottom metal gate (BMG) configurations with high $\mu_{FE} \sim 25.3$ cm$^2$/V-s, near ideal S.S. $\sim 63$ mV/dec., and improved hysteresis characteristics for the first time\textsuperscript{16}. The thickness of conductive a-IWO NS channel can be well controlled by radio-frequency (RF) magnetron sputtering at room temperature. The a-IWO NS-JLTs with metal S/D electrodes exhibit ultra-low leakage currents owing to the wider band gap of a-IWO compared to Schottky-barrier Si devices with high leakage currents\textsuperscript{17}. Furthermore, the $R_{on}$ also can be significantly reduced by using metal S/D electrodes.

In this work, we will study the influences of the different gate insulator (GI) materials and the scalings of GI thickness, a-IWO channel thickness, and channel lengths on the electrical characteristics and performances of a-IWO NS-JLTs. In addition, a low power and high performance CMOS inverter based on low temperature devices is the basic and essential component in digital circuits for the pressing applications such as wearable electronics and IoT technology. Although some hybrid CMOS inverters constructed by low temperature n-channel TAOS and p-channel poly-Si TFTs had been studied and realized, the electrical characteristics of TFTs were performed with high operation voltage, poor S.S, and large $I_{OFF}$ in these previous studies\textsuperscript{18,19}. A conceptual VS hybrid CMOS structure consisted of BEOL compatible n-channel a-IWO NS-JLTs and p-channel poly-Si TFTs will be proposed and characterized in this work. The matched electrical characteristics of n- and p-channel devices with low operation voltage and low $I_{OFF}$ are exhibiting the promising candidate for future VS Hybrid CMOS applications.

**Methods**

The structure diagram of proposed BMG a-IWO NS-JLTs is schematically shown in Fig. 1(a). The proposed devices can be fabricated on Si wafers with 550-nm-thick buffer thermal SiO$_2$ or on glass substrates\textsuperscript{16}. Firstly, a layer of 25-nm-thick Mo film was deposited subsequently by the direct current (DC) sputtering and patterned as the gate electrode through photolithography. Secondly, a layer of 10-nm or 20-nm or 30-nm-thick HfO$_2$ was deposited by atomic layer deposition (ALD) as the gate insulator (GI). Next, a layer of 4-nm or 10-nm-thick a-IWO channel was deposited by RF magnetron sputtering of an In-W-O (contained 4 wt.-% of WO$_3$) ceramic plate target at room temperature. Then, the a-IWO channel active layer was patterned through photolithography. Thirdly, a layer of 25-nm-thick Mo film was deposited by DC sputtering and patterned as the source/drain (S/D)
voltage applications. Therefore, we will focus the BMG a-IWO NS-JLTs with HfO2 GI weakest gate control on channel, resulting in the absence of an OFF-state within V GS = 2V. The transfer characteristics of a-IWO NS-JLTs with different GI materials, different HfO2 GI thickness, and different a-IWO channel thickness. The most positive V TH, highest I ON/I OFF, and steepest S.S. (~63 mV/dec.) are accomplished in BMG a-IWO NS-JLTs with HfO2 GI = 10 nm and a-IWO channel = 4 nm.

Figure 2. The transfer characteristics of a-IWO NS-JLTs with different GI materials, different HfO2 GI thickness, and different a-IWO channel thickness. The most positive V TH, highest I ON/I OFF, and steepest S.S. (~63 mV/dec.) are accomplished in BMG a-IWO NS-JLTs with HfO2 GI = 10 nm and a-IWO channel = 4 nm.

electrodes using the lift-off technique. Finally, after channel passivation processes, contact holes to the gate and S/D electrodes were patterned and opened through photolithography.

To investigate the influences of different GI materials on the devices, the a-IWO NS-JLTs in bottom Si-sub gate (BSG) configurations with a-IWO NS channel = 4 nm were also fabricated on a heavily doped n-type Si wafer with 30-nm-thick high-quality thermal SiO2 GI, as shown in Fig. 1(b). Additionally, the low metal contamination Ni-induced lateral crystallization (LC-NILC) poly-Si TFTs with 50-nm-thick poly-Si channel and 10-nm-thick HfO2 GI were also fabricated on Si-substrates to study the OFF-state electrical characteristics for VS hybrid CMOS applications. The detail LC-NILC processes were shown in our previous work20.

Results and Discussion
Figure 1(c) displays the cross-sectional transmission electron microscope (TEM) images of proposed BMG a-IWO NS-JLTs, the IL between the HfO2 GI and the a-IWO NS channel is negligible, resulting in near ideal S.S. and improved hysteresis characteristics16.

Figure 2 exhibits the transfer characteristics of a-IWO NS-JLTs with different GI materials, different HfO2 GI thickness, and different a-IWO channel thickness. In JL configurations, the doping or carrier concentration of the source/drain (S/D) and channel is uniform, heavy, and homogenous, which significantly reduces thermal budgets of processes and simplifies fabrication7. However, there are more negative V TH and worse subthreshold characteristics in JL devices with thicker channel (a-IWO channel = 10 nm) or under poorer gate controls (HfO2 GI = 30 nm for BMG and SiO2 GI = 30 nm for BSG) in Fig. 21. Among these devices, the transfer characteristics of BSG a-IWO NS-JLTs with a-IWO channel = 4 nm and SiO2 GI = 30 nm exhibit the weakest gate control on channel, resulting in the absence of an OFF-state within V GS = −2V ~ V GS = 2V. The ON-state currents (I ON) and S.S. of BMG a-IWO NS-JLTs are enhanced by shrinking the HfO2 GI thickness (HfO2 GI = 10 nm) thanks to the better gate controllability. Although BMG a-IWO NS-JLTs with HfO2 GI = 10 nm and a-IWO channel = 10 nm have the highest I ON and μ FE, the most positive V TH, highest I ON/I OFF, and steepest S.S. are accomplished in BMG a-IWO NS-JLTs with HfO2 GI = 10 nm and a-IWO channel = 4 nm for low operation voltage applications. Therefore, we will focus the BMG a-IWO NS-JLTs with HfO2 GI = 10 nm and a-IWO channel = 4 nm in the latter discussions.

In order to enhance the I ON, it is necessary to improve both of μ FE and the contact resistance (R c) between S/D metal electrodes and TAOS channel. The normalized output characteristics of a-IWO NS-JLTs with (a) channel length (L) = 40 μm and (b) L = 5 μm are shown in Fig. 3. It is noted that as the thickness of HfO2 GI scaling down from 30 nm to 10 nm, the driving currents of a-IWO NS-JLTs with 10-nm-thick HfO2 GI operated at gate overdrive voltage (V GS − V TH) = 2V are enhanced more than 3 times of magnitude compared with the one with 30-nm-thick HfO2 GI. The significant enhancements in driving currents are attributable to the improvements in R c between the S/D metal electrodes and the a-IWO NS channel.

Transmission line model (TLM) measurement can be used to extract the R c of metal-semiconductor junction22. Figure 4(a) demonstrates the plot of total resistance (R T total) versus channel length (L) at V GS − V TH = 2V. Figure 4(b) displays the results of the extracted width-normalized R c under different V GS − V TH for the a-IWO NS-JLTs with different thicknesses of HfO2 GI. The width-normalized R c in the inset of Fig. 4(b) is plotted in logarithm scale. The R c is significantly improved by elevating the vertical electric-field between the gate and the overlapped S/D electrodes via increasing V GS − V TH and scaling down the thickness of HfO2 GI, especially in V GS − V TH = 2V and HfO2 GI = 10 nm.
Figure 3. The normalized output characteristics of IWO NS-JLTs. (a) The a-IWO NS-JLTs with $L = 40 \mu m$ and (b) the a-IWO NS-JLTs with $L = 5 \mu m$. The driving currents of IWO NS-JLTs with 10-nm-thick HfO$_2$ are more than 3 times as large as those of IWO NS-JLTs with 30-nm-thick HfO$_2$ at $V_G - V_{TH} = 2V$.

Figure 4. The extraction of $R_C$ from the plot of $R_{Total} - L$ and the diagrammatic explanation of $R_C$ in relation to the gate voltage and the thickness of HfO$_2$ GI. (a) The plot of $R_{Total} - L$ at $V_G - V_{TH} = 2V$; (b) the results of the extracted width-normalized $R_C$ under different $V_G - V_{TH}$ in a-IWO NS-JLTs with different thicknesses of HfO$_2$ GI; (c) the schematic structure of gate-to-source overlap region; (d) the illustration of band diagram along A-A'. The $R_C$ is significantly improved by increasing $V_G - V_{TH}$ and scaling down the thickness of HfO$_2$ GI, especially in $V_G - V_{TH} = 2V$ and HfO$_2$ GI = 10 nm.
The transfer characteristics of a-IWO NS-JLTs with different channel lengths. The inset shows the extracted $V_{TH}$ roll-off. The a-IWO NS-JLTs with very small $V_{TH}$ roll-off exhibit high gate controllability and good SCEs immunity.
The technology potential for low-temperature processes applications on a glass substrate had been demonstrated\(^\text{16}\). In JL devices, the path of current transport is concentrated in the center of heavy uniform doping channel, which reduces the effects at the oxide/channel interface, resulting in near ideal subthreshold characteristics\(^\text{6}\).

It is well known that \(\mu_{FE}\) is significantly decreasing as scaling channel thickness. The proposed 2D-like BMG a-IWO NS-JLTs with \(\mu_{FE} \approx 25.3\ \text{cm}^2/\text{V-s}\) exhibit near ideal S.S. and improved hysteresis characteristics because of the NS channel, JL configurations, and the good interface characteristics between the HfO\(_2\) GI and the a-IWO NS channel\(^\text{16}\).

**Conclusion**

In summary, we have studied the influences of the different GI materials and the scalings of GI thickness, a-IWO NS channel thickness, and channel lengths on the electrical characteristics and performances of the 2D-like a-IWO NS-JLTs. Since a-IWO NS-JLTs are fabricated by using Ga-free a-IWO thin films, the material costs can be minimized compared with typically adopted a-IGZO. The Ga- and Zn-free a-IWO NS channel layers with low cost, high mobility, and good stability could be a promising alternative to a-IGZO for the advanced oxide-based TFT technology. Also, the 2D-like BMG a-IWO NS-JLTs significantly minimize the IL thickness, resulting in near ideal S.S. and improved hysteresis characteristics. The 2D-like BMG a-IWO NS-JLTs with small \(V_{TH}\) roll-off, large \(I_{ON}/I_{OFF}\), near ideal S.S., high \(V_{TH}\), low \(R_c\), and low operation voltage appears highly promising potentials for system-on-panel (SoP) and VS hybrid CMOS applications in the future.

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Author Contributions
P.Y. Kuo designed experiments and directed the research direction including experimental and theoretical investigations for the devices. C.M. Chang and I.H. Liu fabricated the devices and measured the electrical characteristics of devices. P.Y. Kuo and P.T. Liu wrote the main manuscript text. P.T. Liu supervised all experiments.

Additional Information
Competing Interests: The authors declare no competing interests.

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