FPGA-based electronic system for the control and readout of superconducting qubit systems

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This paper reports the development of an electronic system for the control and readout of superconducting qubits. The system includes a timing control module (TCM), four-channel arbitrary waveform generators (AWGs), four-channel data acquisition modules (DAQs), six-channel bias voltage generators (BVGs), a controller card, and mixers. The AWGs have a 2-GSa/s sampling rate and a 14-bit amplitude resolution. The DAQs provide a 1-GSa/s sampling rate and 12-bit amplitude resolution. The BVGs provide an ultra-precise DC voltage with a noise level of ~6 μVp-p. The TCM sends system clock and global trigger to each module through a high-speed backplane to achieve precise timing control. These modules are implemented in a field-programmable gate array (FPGA). While achieving highly customized functions, the physical interface and communication protocol are compatible with each other. The modular design is suitable for quantum computing experiments of different scales up to hundreds of qubits. We implement a real-time digital signal processing system in the FPGA, enabling precise timing control, arbitrary waveform generation, parallel IQ demodulation for qubit state discrimination, and the generation of real-time qubit-state-dependent trigger signals for active feedback control. We demonstrate the functionalities and performance of this system using a fluxonium quantum processor.

I. INTRODUCTION

Quantum computing offers the possibility of an exponential computational advantage for certain types of hard problems.\textsuperscript{1, 2} With the continuous advancement of quantum computing algorithms, how to perform them on physical system has become a research hotspot. Since the measurement and manipulation of a single quantum system was demonstrated,\textsuperscript{3} a variety of quantum technologies have been investigated to implement qubits.\textsuperscript{4, 5, 6, 7, 8} Different from classical bits, qubits usually suffer from a short decoherence time. Decoherence, described as a continuous drain of quantum information from the quantum system due to the coupling between qubits and their environment, is the primary error source and obstacle to the realization of large-scale superconducting quantum computers. To protect the qubit information from decoherence, quantum error correction (QEC) is needed. It can significantly improve system fidelity, enabling running arbitrary complex quantum algorithms without the accumulation of errors.\textsuperscript{9} The realization of QEC algorithms requires a hardware system controlling logical qubits encoded in a large number of physical qubits. It is necessary to perform closed-loop feedback within a small portion of the decoherence time,\textsuperscript{10} placing strong real-time performance requirements on the qubit control and readout system.\textsuperscript{11}

Considering the decoherence time and scalability of physical systems, superconducting quantum circuits become a promising platform for the implementation of quantum computing.\textsuperscript{13, 14, 15} Superconducting quantum computing architectures rely on classical electronics for control and readout.\textsuperscript{16} In a superconducting quantum
computing system, the electronics system serves as a bridge between the quantum programming language and quantum processors. The control and readout precision directly affect the accuracy of gate operations and the readout efficiency of qubits. In the control system, an arbitrary waveform generator (AWG) generates a control pulse sequence, which is then upconverted to the qubit frequency through a mixer. The pulse reaches the qubit through microwave coaxial cables passing in and out of a cryostat. Driven by microwave pulses, qubits undergo operations that enable universal quantum computing. In the readout system, the AWG generates a probe signal, which is upconverted to a microwave signal and travels to the superconducting resonators on the processor through similar coax cables. The transmitted signal from the resonator, which carries the qubit state information, is amplified, down-converted and sent to the data acquisition (DAQ) module, whereupon the qubit status can be obtained by data processing. To ensure optimal qubits performance, an ultra-high-precision bias voltage or current generator is required. In order to improve the accuracy of qubit control and reduce the impact on ambient temperature, the electronic system output should have a low noise level.

Google, ETH Zurich, Keysight, LBNL and UC Berkeley have recently built the control and readout systems of superconducting quantum computing. Google’s work uses a self-developed electronics system to achieve the control and readout of 54 qubits. They use daisy chain to build the system trigger architecture which would bring synchronization timing issues in the larger system. ETH Zurich and Keysight provide advanced commercial boards and instruments for quantum experiments. Commercial products have shortcomings such as firmware solidification, fixed interface, and redundant design, which are not conductive to system design and expansion. LBNL and UC Berkeley develop an open-source qubit controller. However, the hardware based on the development board cannot be expanded on a large scale.

As mentioned above, the electronics systems suitable for rapid development of superconducting quantum computer should have the characteristics of scalability, reconfiguration, low noise, low latency, and strong real-time processing. Here, we present a customized field-programmable gate array (FPGA)-based electronics system for the control and readout of superconducting qubit processors to accommodate new qubit types, new operation modes, and eventually the demonstration of QEC at scale.

II. SYSTEM DESIGN

First, we show the architecture of a two-qubit superconducting quantum computing system as an example in Fig. 1. The electronics system is integrated in a 3U chassis. System communication is realized based on the PXIe protocol, as the 8 GB/s data transmission bandwidth of the PXIe bus enables the fast loading waveforms and uploading readout data. The board-to-board communication, system clock, and trigger tree are through high-speed digital backplane transmission. The main modules are implemented based on FPGA, allowing specific functions to be realized while ensuring the compatibility of the physical structure. Hence, different modules can be combined to adapt to different needs in experiments. As shown in Fig. 1, a two-qubit system can be supported by two AWGs, a bias voltage generator (BVG), a timing control module (TCM), and a DAQ; adding an AWG enables the support of a three-qubit system.

Fig. 1. System architecture. A two-qubit system can be supported by two AWGs, a BVG, a TCM, and a DAQ.

A. Clock and trigger system

In superconducting quantum computing systems, the electronics are required to generate or measure the control and readout signal of different qubits at specific times. The
typical operation duration is on the order of tens to hundreds of nanoseconds. To achieve real-time control and precise synchronization in large-scale systems, we design a scalable clock and trigger scheme based on a TCM, as shown in Fig. 2.

As shown in Fig. 2, the analog clock region and digital logic clock region of the electronics system are both related to the 10-MHz system clock. Such a multi-level clock tree architecture, with a star connection to the backplane and strictly equal-length on-board wiring, ensures the overall synchronization performance of the system.

configuration information (implemented in the FPGA). The DACs and ADCs emit gate sequence waveforms and sample the probe signal carrying the qubit status information according to the level-2 trigger, thus realizing control and measurement of a qubit.

In quantum experiments, the electronics system completes a series of control and readout operations with strict timing according to the upper-level algorithm. The timing of operations depends on the corresponding trigger. To facilitate the concrete realization of an upper-level algorithm in the circuit, we design a flexible multi-level timing trigger architecture. Fig. 3 shows how the trigger system works with a simple qubit control and readout example.

B. Arbitrary waveform generator

A block diagram of the AWG is shown in Fig. 4. This module mainly includes the following parts:

1. A high-performance FPGA (XCKU060).
2. Four digital-to-analog converter (DAC) modules (AD9739) and an analog circuit (2-Gsa/s sampling rate, 14-bit resolution).
3. Clock synchronization module.
4. Power.
The FPGA and DAC communication interface link time is the main factor in the AWG latency. In the proposed system, we use 112 pairs of low-voltage differential signaling (LVDS) to realize data transmission between the FPGA and four DACs. On the FPGA side, we use 112 parallel OSERDES3 units to achieve high-speed data serialization (4:1). In UltraScale devices, OSERDES3 is a dedicated parallel-to-serial converter with specific clocking and logic features designed to facilitate high-speed source-synchronous applications. The utilization of the LVDS interface contributes to a nanosecond-level latency time. Although the PCB layout is used to constrain all the data lines to have equal lengths, the precision limitation and a large number of differential pairs mean that the delay of each LVDS data transmission line will be different. A high-precision synchronous clock and an adjustable delay function are required to ensure timing integrity and allow the data to meet the setup and hold time requirements. We use dual-loop PLLs to generate the sampling clock, synchronization clock, and FPGA clock required by the AWG reference to the input system clock. The device clockloop architecture of the DACs and FPGA ensures that the clocks at both ends of the LVDS interface have a definite time relationship. Simultaneously, the phase relationship between the data and clock can be adjusted through the DELAY module in the FPGA.

The waveform generator module has the lowest latency of waveform generation. The waveform data sent by the host are prestored in block random-access memory (BRAM) and can be directly sent to the DAC without calculation. Compared with the Gb-level storage capacity of double-data-rate fourth generation (DDR4) memory, the available BRAM storage resources on the FPGA are somewhat lower, at approximately 30 Mb. However, the readout latency of BRAM is much lower than that of DDR4. To overcome any problems caused by the small storage space, we optimize the waveform data and generate waveform sequences through timing control. Based on the multi-level trigger architecture, the control waveform (up to the milliseconds) is decomposed into a series of short waveforms (up to the tens of nanoseconds). Replace the idle data in the long control waveform with the delay between short waveforms, which greatly reduces the storage space and satisfies the experimental requirements.

C. Data acquisition module

The DAQ module is implemented with two analog-to-digital converters (ADCs: AD12D1000), which provide a two-channel 1-GSa/s sampling rate and a 12-bit amplitude resolution. To reduce the communication interface link time between the FPGA and ADCs, we also use 96 pairs of LVDS to realize data transmission. A real-time demodulation function is realized in the DAQ module, which saves large-trunk data transmission and processing on the control unit.

Fig. 5 shows an overview of the digital signal processing circuit. Readout signals at intermediate frequency (IF) IQ are digitized by the ADCs and quantized into a 2×12×1-G/s digital signal stream. Each channel is transmitted to the FPGA through 12 pairs of 500 MHz LVDS. In the FPGA, the data are first converted to a 2×4×12×250-M/s signal stream through input dual data-rate (IDDR) serial-to-parallel conversion (1:2). Under the 250-MHz clock, pipeline processing is performed.

We digitally demodulate the readout signal to obtain the I and Q components. After a proper IQ quadrature rotation, the state of the qubit can be obtained through state discrimination. The DAQ module generates corresponding feedback signals based on the measurement results, and

![FIG. 5. Overview of the digital signal processing circuit.](image-url)
uploads the measurement results to the controller through PCIe.

We realize digital demodulation through I and Q digital mixing followed by an accumulator module to improve the signal-to-noise ratio. In the digital mixer, the input signals $V_{ADC1}$ and $V_{ADCQ}$, as defined in Eq. (1), are multiplied by a complex exponential of $\omega_{IF}$ to realize digital down-conversion. The complex output signal $S(t)$ is obtained as:

$$S(t) = (V_{ADC1} + V_{ADCQ} e^{j}) * e^{-j\omega_{IF}n}$$

$$= (V_{ADC1} \cos(\omega_{IF}n) + V_{ADCQ} \sin(\omega_{IF}n)) + j * (V_{ADCQ} \cos(\omega_{IF}n) - V_{ADC1} \sin(\omega_{IF}n)).$$

In the FPGA implementation, we use the fs/4 (\(\omega_{IF} = 250 \text{ MHz}\)) IF frequency. This digital mixing structure has the lowest latency (1 clock cycle = 4 ns) because no multiplier is needed.

D. Bias voltage generator

The BVG provides a static magnetic flux that biases the qubit loop so that the qubit can be at any desired operation points. Qubit frequency and decoherence are highly sensitive to the flux bias. Therefore, the bias voltage noise of the BVG need to be extremely low (less than 10 \(\mu\text{V}\)). To achieve such a low noise level, the design is based on a 20-bit DAC (AD5791), ultra-low noise and low-temperature drift amplifiers, reference voltage circuits, and low-temperature-coefficient resistors. We characterize the low-frequency noise to evaluate the DC performance of the circuit. In the 0.1–10 Hz bandwidth, the design generates about 0.6 \(\mu\text{V}\) p-p noise from the DAC, about 0.66 \(\mu\text{V}\) p-p noise from the amplifiers, and about 1.2 \(\mu\text{V}\) p-p noise from the voltage reference. The equivalent output noise is about 1.6 \(\mu\text{V}\) p-p, which meets our requirements. We have integrated six channels on a 3U board, which can support six qubits.

III. TESTING

Figure 6 shows a photograph of the hardware. In this section, we test the performance of the electronics system. The test platform is based on the NI-1085 chassis. The self-developed TCM, AWG, DAQ, BVG, and Keysight M9037 PXIe embedded controller communicate through the backplane. By changing the experimental code in the controller, we fully tested the performance of each board and measured the jitter, digital demodulation processing, and feedback latency.

A. Arbitrary waveform generator

For different qubits coupled to the same readout line, each readout resonator has a decimated frequency and a certain frequency spacing with respect to other resonators to prevent frequency collision. A higher AWG bandwidth means that more qubits can be readout simultaneously in a frequency multiplexing scheme. As shown in Table I, the AWG has good performance in the range from DC–500 MHz (which can be extended to 800 MHz by changing the low-pass filters) and can support the readout of more qubits than commercial boards.

The spurious-free dynamic range (SFDR) is a crucial specification that can be used to characterize the dynamic performance of AWGs. SFDR specifies the relationship between the amplitude of the fundamental frequency being generated and the amplitude of the most prominent harmonic. The AWG output spectrum was measured by a Keysight N9010B spectrum analyzer with a frequency range of DC–2 GHz. The results of a 400-MHz output signal are shown in Fig. 7. Table I reports the SFDR at six frequency points.

![Fig. 7. Spectrum of the AWG output at 400 MHz.](image-url)
| Frequency (MHz) | SFDR (dB) |
|----------------|-----------|
| 10             | 70.8      |
| 100            | 60.2      |
| 200            | 55.7      |
| 300            | 58.1      |
| 400            | 66.2      |
| 500            | 64.5      |

**TABLE I. SFDR test results.**

**B. Data acquisition module**

The DAQ module was tested according to IEEE standard 1241-2010. We used a radio frequency signal generator (SMA100) to generate the test signals. Figure 8 shows the spectrum of 398-MHz signals acquired by the DAQ. Table II presents the DAQ test results (where SNR denotes the signal-to-noise ratio, THD is the total harmonic distortion, and ENOB is the effective number of bits). Note that the 400MHz analog bandwidth of the DAQs means that we can frequency multiplex the readout of 10 qubits (with 40MHz separation) on the same readout line.

| Frequency (MHz) | SNR (dB) | THD (dBc) | ENOB (bit) |
|----------------|----------|-----------|------------|
| 19.9           | 60       | 65.5      | 9.4        |

**FIG. 8.** Spectrum of a 398 MHz signal acquired by the DAQ.

**TABLE II. DAQ test results.**

**C. Bias voltage generator**

The output noise of the BVG is sensitive to environmental temperature changes. We test BVG in an A/C laboratory. The output noise of the BVG was tested using a 6 1/2 Digital Multimeter (DMM, Fluke 2638A). The 10-h output values at 0.86 V are shown in Fig. 9, where Vpp is about 6 μV, which is equal to 0.3 ppm over a 20-V range. Such a low noise level can accurately control the magnetic flux biasing the loop for the qubit.

**FIG. 9.** +0.86 V output over 10 h from Fluke 2638A.

**D. Jitter of the electronics system**

Increasing the SNR of the collected signal and obtain the statistical probability of the qubit superposition state requires a large number of repetitive operations in quantum computing. The phase of the signals sample at different times will be affected by the system jitter, which reduces the accuracy of qubit state measurement. The jitter is mainly caused by the system clock jitter, trigger jitter, AWG phase noise, and ADC noise. To test the jitter of the electronics, the AWG output was connected to the DAQ input, and the TCM cycle generated 5000 triggers to the AWG and DAQ. The initial phase of the 5000 acquired data were then
analyzed. Figure 10 shows the histogram of the waveform initial phase. The standard deviation shows that the phase jitter of the electronics is approximately 0.013 degrees (IF=10 MHz). Converted to time, the jitter of the electronics is approximately 3.6 ps.

E. Digital processing of feedback

As discussed in Sect. II C, real-time demodulation and state discrimination were implemented in the DAQ module. To verify the correctness of the implementation and the closed-loop feedback latency of the electronics part, we built a test platform using the AWG, DAQ, TCM, a controller, and an oscilloscope.

1. We first generate a series of waveform data on the controller in which the phase was evenly distributed from 0 to $2\pi$. The AWG was directly connected to the DAQ, triggered by the TCM. The DAQ samples the AWG output and performs real-time demodulation. The digital demodulation result was sent to the controller through PCIe, and the result was plotted in the IQ plane. If the demodulation is correct, the result point (I, Q) will rotate an angle in turn until the $2\pi$ phase is traversed. Figure 11 shows 100 demodulation results in which (I, Q) points form a circle. The circle-plot test verifies the correctness of the digital demodulation algorithm implemented in the FPGA.

1. We generate two sets of IQ signals representing the qubit ground state and the excited state signals. To better observe the timing of different signal processing stages, the parallel data in the FPGA were uploaded to the controller via PCIe, and a parallel-to-serial conversion was performed in the software. The signal at different processing stages is shown in Fig. 12. Blue squares (ground state) and red squares (excited state) represent the corresponding digital signals obtained from the FPGA design. The digital processing takes a time of $\tau_{\text{proc}} = 20$ ns, which matches the design value in Figure 5.

2. We define the latency of the feedback as the time from the beginning of the measurement pulse to the generation of the next control pulse conditioned on the measurement result. The total feedback latency is the sum of the ADC latency, signal processing latency, AWG latency, cable delays, and readout time. Except for the cable delays and readout time, all contributions are from the electronics system. We used two AWGs, one DAQ module, and one TCM to build the test platform. Channels 1 and 2 of AWG1 generated probe IQ signals representing qubit state information and sent them directly to the DAQ module, while Channels 3 and 4 generates the same waveforms are connected to an oscilloscope for observation. The DAQ sampled the probe signal and generates the corresponding feedback trigger signal after digital processing. The feedback trigger signal is then sent to AWG2 and the oscilloscope through a 1:2 power divider. AWG2 generates a feedback pulse based on the received feedback trigger and sent it to the oscilloscope. The signal sampled by the oscilloscope is shown in Fig. 13. The measured electronic system feedback latency is about 125 ns (excluding the readout time of 48 ns).
IV. EXPERIMENTS

To demonstrate the performance of this control and readout electronics system, we performed a qubit characterization using fluxonium superconducting processor. The experiment mainly included single-tone spectroscopy, two-tone spectroscopy, $T_1$ measurement, and Ramsey measurement ($T_2^*$).

A. Calibration

Before starting the experiment, we calibrated the XY drive line. Due to the mixer’s DC offset and the imbalance of the IQ analog channel, the output signals from the mixer have LO leakage and sideband leakage. The frequency of the LO leakage and sideband signals is within the passband of the filter, so they cannot be filtered out. These leakage tones could interfere the qubit control and readout.

Based on the experimental platform, we built an automated calibration apparatus for IQ mixer offset and imbalance calibration. The calibration process is shown in Fig. 14. The calibrated parameters were stored.

As shown in Fig. 15, the LO leakage and sideband leakage can be suppressed to approximately -70 dBm, which meets the requirements.
B. Characterization

After mixer calibration, the electronics system was used to perform a qubit characterization using fluxonium superconducting processor. First, we conduct single-tone spectrum experiments to find the “sweet spot” of the fluxonium qubit and its readout parameters. The readout probe signal frequency and the BVG’s output voltage were swept to perform a resonator spectroscopy as shown in Fig. 16 (a) (b). According to the measurement results, the BVG output voltage was set to 0.87 V and the readout probe signal frequency was set to 6.1642 GHz. After setting the qubits to the desired operating point, we determined the qubit frequency by two-tone spectroscopy experiments. By continuously send a readout probe signal to the qubit and analyze the transmission signal, the XY line drive signal frequency and BVG’s output voltage were swept to perform the qubit frequency domain response as shown in Fig. 16 (c) (d). To characterize the life time of the qubit, we measured the relaxation time T1 and the dephasing time T2*. T1 measurement was performed by preparing the qubit in the excited state with a π-pulse and wait for a variable time twait to measure the qubit state (Fig.16 (e)). Ramsey measurement was performed by preparing the qubit in the superposition state with a π/2-pulse and wait for a variable time twait to applying another π/2-pulse and measure the qubit state (Fig.16 (g)). Fig.16 (f) and Fig.16 (h) show qubit T1 and T2* measurements (90μs and 19μs).

V. Conclusions

We have described the design and implementation of a high-performance electronics system for the control and readout of superconducting qubits. This system has a modular design that is reconfigurable and can be used in quantum computing experiments of different scales. We measured the state-of-the-art coherence time of fluxonium qubits, demonstrating the low noise performance of the system. This system also enables real-time analysis of the qubit state, which greatly speed up the readout. The low-latency design significantly reduces the feedback latency to 125 ns, significantly less than the decoherence times of the qubit. The system we proposed and realized integrates several key ingredients of next generation quantum computing control electronics: compatible with high coherence qubits, supporting feedback-based advanced operations like active qubit reset and dynamic algorithms, and capable of scaling up to hundreds of qubits. This work constitutes the foundations towards the demonstration of quantum error correction and logical qubits in a superconducting quantum computing system.
DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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