Study of irreversible degradation processes in gate dielectric of MIS structures

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Abstract. In this paper we propose an improved method for accelerated tests of the MIS structure gate dielectric and for studying the irreversible processes in it. This method is based on applying a ramping current load to a sample with a short injection measurement mode between the increments of the current load. This method allows obtaining a time history of the voltage drop across MIS structure at a constant level of measurement injection current for the whole current load range. This time history can be used to find the parameters characterizing irreversible processes of charge degradation such as density and localization of a charge accumulating in the dielectric film, cross-sections of electron and hole traps, nature of the evolution of charge effects and etc.

1. Introduction
Present time integrated circuits and semiconductor devices with metal-insulator-semiconductor (MIS) structure are at the basis of most electronic devices. Reducing of linear sizes of integrated circuit elements becomes a faster process than lowering of power voltages. Because of that, high fields take place at working modes of usage of MIS devices [1-3]. The main part of MIS devices, defining their reliability, is a thin gate dielectric film. Under the influence of high fields through the gate dielectric, a tunnel current starts to flow. This current, as a rule, is caused by Fowler-Nordheim injection of electrons [1-12]. The flow of high-field injection current results in the processes, such as the accumulating of charges in the gate dielectric and at the interface dielectric/semiconductor, generation of the charge traps, structural defects of dielectric, etc. Most of these processes are irreversible and result in degradation of the dielectric film and its electrical breakdown, and, as a consequence, MIS structure failure [1,3,12,14].

The paper considers the improved method of accelerated tests of thin dielectric films of MIS structures, which is based on applying to the sample the ramping current stress. The suggested method introduces the measurement mode allowing to study the irreversible processes of gate dielectric degradation until the sample breakdown.

2. Method description
At high-field tunnel injection of electrons into a thin gate dielectric of MIS structure, which is based on the thermal SiO₂ film, the main mechanisms of the MIS structure degradation are [5-13]:
- the accumulation of holes in the gate dielectric, appearing at thermalization of hot electrons in the dielectric and/or the gate. The density of these holes is described by the following equation [9,10]:
\[ q \frac{dp}{dt} = J_{inj} \cdot \alpha \cdot \sigma_p \left(N_p - p\right) - J_{inj} \cdot \sigma_n \cdot p , \]  

- the capture of electrons by traps in SiO₂ bulk. Density of these electrons is described by the following equation:

\[ n_i = \sum_{k=1}^{t} N_{ik} \left[1 - \exp\left(-\frac{\sigma_{ik} \cdot Q_{inj}}{q}\right)\right], \]

where \( q \) – electron charge; \( J_{inj} \) – density of injection current; \( \alpha \) – ionization coefficient for SiO₂ film of MIS structure being under high-field injection; \( N_p \) and \( \sigma_p \) – density and cross-sections of hole traps; \( \sigma_n \) – cross-section of injected electrons by filled hole traps; \( N_{ik} \) and \( \sigma_{ik} \) – density and cross-section of \( k \) electron traps in the SiO₂ film; \( L \) – amount of variants of electron traps; \( Q_{inj} \) – charge injected into the dielectric.

One of the main methods of researching quality and defectiveness of thin dielectric films of MIS structures under stress are methods based on the high-field injection of electrons into the dielectric [1-14]. Currently, the method of raising current stress (J-ramp) is widely used for conducting accelerated tests of thin dielectric films of MIS structures, for researching degradation processes, charge effects, defectiveness of the dielectric films, their steadiness to high-fields, radiation, and other stresses [1,4,15]. In this method the test starts with a low level of current. The density of injection current flowing though the dielectric film is raised exponentially (step-by-step) until the dielectric breaks down. However, utilizing the J-ramp method for research of the irreversible processes of charge degradation of the gate dielectric introduces significant difficulties caused by varying conditions of the charge injection (at each step). In order to eliminate the mentioned disadvantage, we propose an improved method of tests. Figure 1 shows plot of electrical current load and voltage across researched MIS structure vs. time for the developed method. We suggest including measurement current (\( I_m \)) in testing algorithm and apply the measurement current for a short time period before switching the test current load to a step with a higher value. The measurement current provides injection mode for the structure. We suggest setting the value of \( I_m \) to the current value at the first step or at a step for which intensity of processes of charge degradation of MIS structure is not yet significant. Besides, when choosing, one should take into account a requirement to minimize the transient currents taking place at switching between steps. As a result, it is possible to determine the time histories of the voltage drop across MIS structure at a constant value of injection current \( I_m \) for a full range of current load until the sample breaks down. This time history allows acquiring the important parameters that characterize the irreversible processes of charge degradation: density and spot of localization of charges accumulated in the dielectric film, cross-sections of the electron and hole traps, the character of the evolution of charge defects, and etc. [5-12].

3. Experimental results and discussion

The experiments were conducted for MIS capacitors fabricated on semiconductor wafers of n-type silicon with a resistivity of 4.5 Ω·cm and crystallographic orientation of <100> in-situ with a batch of CMOS ICs. Silicon dioxide with a thickness of 65 nm was fabricated by thermal oxidation of silicon in dry oxygen at the temperature of 1000 °C with 3 % HCl adding. As a gate, we used poly-silicon film with a thickness of 0.6 μm and the area of 10⁻² cm² doped with phosphorus to 20 Ω·cm.

We observed the quality of the gate dielectric by utilizing a setup described in [16] at the positive polarity of load applied to the gate and that provided injection of electrons from silicon substrate and accumulation mode at the near-surface area of silicon. Figure 2 demonstrates distribution histograms of MIS structures by charge injected until the breakdown which are acquired for one silicon substrate for different measurement modes. Histograms 1 and 2 in figure 2 were obtained under mode of constant injection current during the test: \( 1 - J_{inj} = 0.1 \text{ mA/cm}² \); \( 2 - J_{inj} = 10 \text{ mA/cm}² \). Figure 2 shows that at a higher density of injection current (histogram 2) we can observe more frequent breakdowns at the initial step of injection and lowering of the average amount of charge injected until the breakdown. These effects are in good agreement with literature [17-20] and can be explained by a higher intensity
of processes of charge degradation of the gate dielectric in the condition of higher electric fields which are a result higher density of injection current. Histogram 3 in figure 2 is acquired by using the method proposed in the paper for which the current flowing through the dielectric is changed in accordance with the algorithm shown in figure 1. Short-time switching of injection to measurement mode does not noticeably influence the test. The use of the algorithm allowed obtaining the histograms of MIS structure distribution by charge injected until the breakdown. Besides, it also enabled acquiring the relationship of voltage change across MIS structure at measurement level of current (1 μA/cm²) on the density of injected charge (figure 3, curve 3). Besides, figure 3 demonstrates dependencies of voltage change across MIS structure at tunnel Fowler-Nordheim injection of electrons from silicon under the mode of constant current flowing. The demonstrated dependencies are similar to histograms 1 and 2 shown in figure 2: 1 – \( J_{\text{inj}} = 0.1 \text{ mA/cm}^2 \); 2 – \( J_{\text{inj}} = 10 \text{ mA/cm}^2 \).

Figure 1. Time history of current load applied to the sample (a) and the voltage across the MIS structure (b).

Figure 3 shows how the processes of charge degradation of gate dielectric change at different modes of measurement of gate dielectric quality. Processes which are responsible for the degradation of gate dielectric change more frequently when using J-ramp method. At the initial step of stress at low values of injection current the charge degradation is insignificant and at this step only a small amount of MIS structures is under breakdown (figure 2, histogram 3). At higher values of injected charge, the density of injection current reaches relatively high values and that results in higher electric fields applied to gate dielectric, and, as a consequence, in intensification of processes of charge degradation. As a result, at this step an amount of MIS structures under breakdown significantly increases.
Figure 2. Histograms of distribution of MIS structures by charge injected until the breakdown for a one semiconductor substrate at different measurement modes: $1 - J_{\text{inj}} = 0.1 \text{ mA/cm}^2$; $2 - J_{\text{inj}} = 10 \text{ mA/cm}^2$; at the mode of current raising.

Figure 3 demonstrates that the main mechanism of gate dielectric degradation at low values of injection current for electric fields in a range up to 6.5 MV/cm is capturing of electrons in SiO$_2$ bulk by initial electron traps. At injection currents enabling electric fields higher than 6.5 MV/cm the
generation of positive charge in gate dielectric at a distance of 3–5 nm from the cathode influences the charge degradation quite significantly. The generation of positive charge is for the most part caused by accumulation of holes which is presented in the dielectric as a result of band-to-band impact ionization and injection of holes from the anode [1,3,9]. This process is properly described by equation (1). The generation of positive charge is the dominating mechanism of charge degradation at injection of charge of 1–5 mC/cm². Then trapping of electrons in SiO₂ bulk by newly created electron traps becomes the main process of charge degradation of gate dielectric. This result is in good agreement with literature and our previous researches [1,3,10,21,22]. Thus, the proposed method allows acquiring information about processes of charge degradation of MIS structures similar to the information obtained from method of constant current. Besides, the proposed method allows choosing the measurement modes for the J-ramp method more correctly.

4. Conclusions
The paper proposes the improved method of accelerated tests of thin dielectric films of MIS structures. The method is based on applying an increasing current load to a sample. A short switch to the injection mode with a constant measurement level of current I_m is done before stepping up the current load. At the level I_m no significant degradation of dielectric is observed. As a result, we can acquire time history of the voltage drop across MIS structure for a full range of current load including breakdown level by measuring the voltage drop across MIS structure at every switch in the mode of flowing measurement current I_m. Analysis of this time history allows studying the processes of charge degradation of gate dielectric when using the J-ramp method and determine density and spot of localization of charges accumulated in the dielectric film. Besides, it allows to determine the character of charge defects evolution and choose the measurement modes for the J-ramp method more correctly.

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