A 1.2 GHz Bandwidth and 88 dB Gain Range Analog Baseband for Multi-Standard 60 GHz Applications

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Abstract This paper proposes a 55-nm CMOS analog baseband (ABB) with wide tunable bandwidth (BW) and large tunable gain, which consists of a variable-gain amplifier (VGA) and a low-pass filter (LPF) for multi-standard 60 GHz applications. A modified dual-feedback Cherry-Hooper-based VGA achieves a large gain range of -15–73 dB. Through the analog and switched-capacitor (SC) tuning, the 8th-order \( G_m\)-C-based LPF features a widely and continuously tunable bandwidth of 100–1200 MHz. A linear 8-bit digital-to-analog converter (DAC) is integrated for bandwidth and gain tuning. Measurement results show that the output linearity (OP1dB) is -35.5–3.8 dBm, and the noise figure (NF) is less than 21 dB when the gain is 56 dB while consuming 12 mW of power.

key words: Analog baseband (ABB), Dual feedback, Variable-gain amplifier (VGA), \( G_m\)-C low-pass filter (LPF), Analog and switched-capacitor tuning, Digital-to-analog converter (DAC)

Classification: Integrated circuits

1. Introduction

The 60 GHz wireless bands regulated by IEEE 802.11ad [1], 802.15.3c [2], ECMA-387 [3] and China Wireless Personal Area Network (CWPAN) [4] protocols is an attractive option for short-range wireless communication for its high spatial isolation and wide bandwidth [5,6]. As shown in Fig. 1(a), these wireless communication bands [1–3] are uniform from 57.24 to 65.88 GHz, including 4 channels (1, 2, 3, 4) with a bandwidth of 2.16 GHz [7]. However, China only opens 59.40-63.72 GHz in a total of 4.32 GHz for 60 GHz applications, as illustrated by the red line in Fig. 1(a). The CWPAN protocol divides the band into 6 logical channels, of which two channels (2, 3) take up a bandwidth of 2.16 GHz and four sub-channels (5, 6, 7, 8) occupy a bandwidth of 1.08 GHz [4,8].

In wireless transceiver, the receiver analog baseband (ABB) generally locates between the mixer and the ADC [9–12], mainly including VGA and LPF. Fig. 1(b) shows a 60 GHz zero-IF receiver involved in this design. Since the intermediate frequency \( \omega_{IF} = 0 \), the baseband signal bandwidth is half of the RF channel bandwidth [13–15], 1.08 GHz and 540 MHz, respectively. The path-loss range will exceed 73 dB when the communication distance is 0.2–20 m in typical residence, office and laboratory environments [1,2].

Many schemes have been reported to achieve a wide dynamic range ABB. The ABB shown in [16] consists of a current-mode VGA and LPF with 3-31 dB gain range and 0.6-1 GHz BW range. The LPF shown in [17] adopts a feedback transimpedance amplifier, of which the BW can be tuned by adjusting the feedback capacitance, realizing a 0-3 GHz tunable BW range. However, it is also power-hungry while consuming 44.5 mW from two power supplies of 1.5 and 2.5 V, not suitable for low-power applications. A temperature-robust VGA [18] based on the differential amplifier with diode load, results in a -16-16 dB quasi-linear gain range, while the maximum BW is less than 1 GHz.

In this paper, a low-power wideband receiver ABB is proposed, whose bandwidth tuning range, gain tuning range and linearity are compatible with most of transceiver requirements for international 60 GHz wireless communications. The VGA adopts a modified Cherry-Hooper amplifier (MCHA) with active and passive dual feedback to achieve a large gain range while using the constant differential resistor (CDR) to suppress gain fluctuation. The Nauta-OTA cell is employed in the \( G_m\)-C LPF. The analog and switched-capacitor (SC) tuning are combined to realize wide bandwidth range and low power consumption.

2. ABB with Tunable Gain and Bandwidth

Fig. 1(c) shows the block diagram of the proposed tunable gain and BW ABB. The input adopts AC-coupling to eliminate DC offset from the preceding circuit, and the DC offset caused by the ABB itself is suppressed by the DCOC block. The cut-off frequency of AC-coupling and DCOC block are both less than 500 kHz to avoid SNR deterioration. The VGA and LPF are both cascaded by 4-stage units, while the VGA is composed of 4-stage cascaded MCHA structures and the LPF consists of 4 bi-quadratic \( G_m\)-C units. The VGA provides adjustable gain to meet system requirement, while realizing an outranged BW to ensure that the system bandwidth is determined by the LPF. The testing buffer is used to drive pads, ESD and the external 50 Ω impedance of measurement instruments and its gain is 0 dB. Since the

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DOI: 10.1587/elex.17.20190742
Received December 17, 2019
Accepted December 23, 2019
Publicized January 9, 2020
receiver ABB is sensitive to noise, a low-noise pre-amplifier is inserted at the input to provide a constant 10 dB gain and suppress noise contributions from successive stages.

### 2.1 MCHA-based VGA using dual feedback and CDR

Fig. 2 shows a modified Cherry-Hooper amplifier (MCHA) [19] structure with dual feedback and constant differential resistor (CDR) for the proposed VGA. Adopting the active feedback technique, it only increases the gain bandwidth product (GBW) by $\omega_f / \omega_{-3dB}$ [20]. The large-sized transistor array for switching resistors is not friendly to layout placement, while increasing parasitic capacitance of the connected nodes and limiting the bandwidth. The passive feedback path resistors of $R_f$ are realized by the PMOS transistors operating at linear region. Combining with the active feedback path of $G_{mf}$, the presented dual-feedback MCHA structure can boost the GBW to

$$A_0 \cdot \omega_{-3dB} = \omega_f \cdot \left( \omega_f + \frac{1}{R_f C_2} \right) \cdot \frac{1}{\omega_{-3dB}}$$

(1)

where $C_2$ is the output capacitance of $V_{out}$. Due to the process variations, the minimum physical resistance (PR) fluctuation is larger than 15%, which would lead to a large gain deviation of the implemented VGA if it is used as the load. As shown in Fig. 2, in order to suppress the gain fluctuation, a CDR structure is exploited, the resistor is realized by PMOS ($MR_{1,1}$ and $MR_{1,2}$) operating at linear region. The common-mode feedback (CMFB) amplifier $A_1$ clamps differential output common-mode level to $V_{ref}$. As the bias current of $IB_1$ is constant, the equivalent resistance can be calculated as

$$R_1 = \frac{2(V_{DD} - V_{ref})}{IB_1}$$

(2)

Table I shows the simulated maximum gain of the 4-stage VGA when utilizing the PR and CDR, respectively. The deviation is optimized from “-9~+5 dB” to “-3~+1 dB”.

| Process Corner | PR Max-Gain (dB) | PR Offset (dB) | CDR Max-Gain (dB) | CDR Offset (dB) |
|----------------|-----------------|---------------|-------------------|-----------------|
| TT             | 58              | -             | 58                | -               |
| FF             | 49              | -9            | 55                | -3              |
| SS             | 63              | 5             | 58                | 0               |
| FS             | 61              | 3             | 59                | 1               |
| SF             | 53              | -5            | 55                | -3              |

#### 2.2 Dual tuning of analog and SC in the $G_m$-C LPF

The transconductor amplifier is suitable for broadband filter since it is working in open-loop state, of which the maximum operating frequency is GBW. Fig. 3(a) shows block diagram of the $G_m$-C bi-quadratic LPF. Eqs. (3) and (4) present its transfer function and the standard 2nd-order butterworth filter transfer function as

$$H(s) = \frac{G_{m1} G_{m2} G_{m3}}{s^2 + G_{m2} C_1 s + G_{m3} G_{m4} C_1 C_2}$$

(3)

$$B_{2nd}(s) = \frac{A_0 \omega_c^2}{s^2 + \sqrt{2} \omega_c s + \omega_c^2}$$

(4)

The filter is butterworth type if $2G_{m3}G_{m4}C_1 = G_{m2}^2C_2$, and its DC gain of $A_0$ and 3-dB BW of $\omega_c$ are respectively as

$$A_0 = \frac{G_{m1}}{G_{m4}}, \omega_c = \sqrt{\frac{G_{m2} G_{m3}^2}{C_1 C_2}}$$

(5)

In order to provide a linear 1-Vpp output amplitude, the Nauta-$G_m$ [21–26] OTA with high transconductance efficiency and linearity is utilized as shown in Fig. 3(b). The main transconductances $g_{m1}$ and $g_{m2}$ employs the inverter topology, setting the input and output common mode voltage as $V_{DD}/2$ to achieve better input and output linearity. The current of PMOS and NMOS are reused to improve power efficiency. Due to the pseudo-differential structure, the transistor takes 5 times $L_{min}$ channel size to improve the matching characteristic. Besides the differential layout placement, the power and ground lines are nearby connected to INV1.
To realize a larger BW tuning range, the V+ is realized by the R-2R structure. The 8-bit is employed to realize the tuning range and the NF performance. The bandwidth can be continuously tuned from 100 to 1200 MHz, and the in-band NF is less than 0.2 LSB.

Fig. 3: (a) The Gm-C bi-quadratic LPF with the SC tuning, (b) the Nauta-Gm OTA cell, and (c) the implementation scheme of the analog tuning in LPF.

and INV2, achieving > 60 dB CMRR and PSRR in post-layout simulation. The Nauta-Gm’s CMFB is composed of g_m3–g_m6, and the CMFB loop stability requires (g_m3+g_m4) = (g_m5+g_m6) ≥ 0.66G_m. A factor of 0.75 is selected to achieve 10% margin. In addition, the CMFB transconductance can alleviate the insufficient differential-mode gain problem caused by the limited output impedance. Eq. (6) shows the differential-mode resistance at the output node, the g_m6 is slightly larger than the g_m5 to create a negative resistance to compensate the output resistance and improve the OTA differential-mode gain.

\[ R_{op,diff} = \frac{1}{g_{ds1} + g_{ds5} + g_{ds6} + g_{m5} - g_{m6}} \] (6)

The Nauta-Gm transconductance shown in Fig. 3(b) can be calculated as

\[ G_m = \mu_n C_ox \left( \frac{W}{L} \right)_n (V_{DD}/2 - V_{THN}) + \mu_p C_ox \left( \frac{W}{L} \right)_p (V_{DD}/2 - |V_{THP}|) \] (7)

When the W/L of PMOS and NMOS are determined, the transconductance is proportional to the V_{DD}. Thus, from Eqs. (5) and (7), the LPF bandwidth can be linearly adjusted through changing the supply voltage. Fig. 3(c) presents a tunable BW LPF implementation scheme using this analog tuning method. Where the V_CC is 1.2 V, the V_DD is the operating voltage of LPF, M1 is the current source transistor, the OTA clamps V_DD to V_bw, so that the filter bandwidth is regulated by V_bw. The BW tuning is limited since the V_DD only can be tuned from 0.7 to 1.15 V to ensure the saturation operation of Nauta-Gm. Therefore, a pair of switched-capacitor (SC) shown in Fig. 3(a) are introduced at X and Y nodes to realize a larger BW tuning range. The C_X and C_Y complying with 2G_m3G_m4C_1=G_m2C_2 will provide butterworth response for both on and off states.

2.3 Linear 8-bit R-2R DAC programming block

The DAC is adopted to tune BW and gain. Since there is no output current requirement for V_{bw} and V_{g} at gate terminals, it is realized by the R-2R structure. The 8-bit is employed to achieve gain-step with 0-0.6 V V_{g} and BW-step with 0.6-1.2 V V_{bw}. Fig. 4 shows schematic and layout of the integrated 8-bit DAC. To ensure the consistency of resistance, the 2R consists of 2-unit R in series. B0~B7 control bits are assigned to R-2R network through input buffers, all buffers are realized with the large W/L to reduce on-resistance R_{on} ≪ R, otherwise the cumulative R_{on} will affect the ratio of 2R:1R. In order to reduce resistance mismatch caused by the process gradient error, the P+ Non-silicided diffusion resistor with the smallest mismatch coefficient of 6.25×10^{-3} is selected. The R is placed in the middle of the cell, the 2R at both sides, the 8-bit R-2R unit is arranged in the order of B7-B5-B3-B1-B0-B2-B4-B6 with a common-centroid layout to improve linearity. The simulated static results show that the integral non-linearity (INL) and differential non-linearity (DNL) are both less than ±0.2 LSB.

3. Measurement Results

The ABB is fabricated in a 55-nm CMOS process with an area of 650×210 μm². The LPF and VGA parts are also independently realized for measurement comparison. The in-phase and quadrature ABB are both realized by the proposed LPF and VGA. The chip is packaged in QFN64. Figs. 5(a), 5(b) and 5(c) show the die photograph, the printed circuit board (PCB) and the testing environment, respectively. The measurement results show that the ABB consumes 10 mA from 1.2 V supply. Fig. 6 shows the measured BW tuning range and the NF performance. The bandwidth can be continuously tuned from 100 to 1200 MHz, the V_{bw} code of 6~22 corresponds to a BW of 100~320 MHz, 38~51 corresponds to 220~1200 MHz, and the in-band NF is less than 21 dB when the gain is 56 dB. Fig. 7 shows the measured input linearity (IP1dB) and output linearity (OP1dB), the
Table II: Performance summary and comparison with the prior works.

| Reference          | Tech. | BW−3dB (MHz) | Gain (dB) | Linearity (dBm) | NF (dB) | Power (mW) |
|--------------------|-------|--------------|-----------|-----------------|---------|------------|
| [11] IEICE 2018    | 180-nm| 0.5~30       | 0~80      | \               | \       | 4.1        |
| [16] RFIC 2013     | 65-nm | 980~1000     | 3~31      | IP1dB is -4~31  | 6~21    | 16~24      |
| [27] RWS 2013*     | 90-nm | 1000         | -25.3~59  | IP1dB is -1     | 15      | 21.9       |
| [28] MWSYM 2014    | 180-nm| 3~1700       | -1.4~30.2 | OP1dB is -4     | \       | 35         |
| [29] TMTT 2016*    | 65-nm | 2000~2200    | 2~24      | OP1dB is 1.8    | 24~29   | 3.5        |
| [30] WAMICON 2016* | 65-nm | 700~1760     | Range is 55 | \       | \       | 14         |
| [31] LS SC 2018    | 130-nm| 980~1000     | 3~31      | IP1dB is -4~31  | 6~21    | 16~24      |
| **This Work**      | 55-nm | 100~1200     | -15~73    | OP1dB is -35.5~3.8 | 21  | 12         |

* VGA only

Fig. 5: (a) ABB die photo, (b) the PCB, and (c) the testing environment.

Fig. 6: Measured ABB (a) BW tuning range and (b) noise figure. OP1dB is -35.5~3.8 dBm. The measured ABB gain range is -15~73 dB as shown in Fig. 8. Simulation results show that the proposed ABB gain switching time from 0.8 to 60.7 dB is less than 0.5 µs and can meet Wigig short-distance communication requirement (< 1.2 µs) [32, 33]. The measured performance is summarized and compared with the prior works as shown in table II.

4. Conclusion

This paper proposes a 55-nm CMOS ABB for multi-standard 60 GHz wireless communication applications. The VGA
employs a modified Cherry-Hooper amplifier (MCHA) structure with dual feedback and CDR techniques to realize a large gain range and suppress fluctuation, simultaneously. The LPF combines analog tuning and switched-capacitor tuning to achieve a wide BW tuning range and high power efficiency. The measurement results show that the ABB achieves -15 ~ 73 dB gain range and covers 100 ~ 1200 MHz BW range while consuming 12 mW power. Comparing with the prior works, the proposed ABB is competitive in BW tuning range, gain tuning range and power consumption and appropriate for multi-standard 60 GHz transceivers.

Acknowledgments
The authors would like to appreciate Yoshihiro Yasue, Tatsuya Sumida, Jacob Chen and Liangfu Lo from MIE Fujitsu for chip fabrication support.

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