Data Criticality in Multi-Threaded Applications: An Insight for Many-Core Systems
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Abstract—Multi-threaded applications are capable of exploiting the full potential of many-core systems. However, Network-on-Chip (NoC) based inter-core communication in many-core systems is responsible for 60-75% of the miss latency experienced by multi-threaded applications. Delay in the arrival of critical data at the requesting core severely hampers performance. This brief presents some interesting insights about how critical data is requested from the memory by multi-threaded applications. Then it investigates the cause of delay in NoC and how it affects the performance. Finally, this brief shows how NoC-aware memory access optimisations can significantly improve performance. Our experimental evaluation considers early restart memory access optimisation and demonstrates that by exploiting NoC resources, critical data can be prioritised to reduce miss penalty by 10–12% and improve system performance by 7–11%.

Index Terms—Data criticality, multi-threaded applications, many-core systems, network-on-chip (NoC), miss penalty.

I. INTRODUCTION

APPLICATIONS running in any computing device can be broadly classified as either multi-programmed or multi-threaded. Many-core systems have made way for applications with massive processing requirements; something which was not possible earlier. The processing power of many-core systems comes from a collection of relatively simpler processing cores, unlike a single powerful core in uni-core systems. Hence, to exploit the full potential of many-core systems, applications need to be parallel, thus multi-threaded. Modern many-core systems employ Network-on-Chip (NoC) based inter-core communication, and it is reported that NoC is responsible for 60–75% of the miss latency in multi-threaded applications [1]. Delay in arrival of the critical data at the requesting core hampers performance of such applications. Hence, it is very important to get an insight into how multi-threaded applications request critical data and how NoC contributes to the miss latency (miss penalty) of such applications.

While running an application, a core usually requests for a single word from memory, called critical word [2]. The critical word is first searched in the cache memory and returned to the core if found. However, if the word is not found in the cache, it is requested from the next level of memory. The smallest unit of data transfer between different levels of memory is in blocks, where a block consists of multiple words. So, even though the core requests a single word, a complete block (containing the critical word) is brought from the next level of memory in the form of a packet through the underlying NoC. Nevertheless, transfer bandwidth in NoC is limited to channel width called flit. A data block (packet) is divided into multiple flits (flit << block) and sent in sequence, as shown in Figure 1. The critical word can be in any of the incoming flits and hence would accordingly impact the performance. On their way, the incoming flits experience indefinite router delays due to congestion, which impact their arrival on the requesting core, which again hampers the performance.

The purpose of this brief is to share some interesting insights about running multi-threaded applications in many-core systems. It specifically presents the pattern of critical words requested from the memory. Then it describes the pattern of delays experienced by the flits while travelling from source to their destination. The brief finally shows how using these insights can significantly improve the performance of existing optimisations on miss penalty reduction. Specifically, this brief makes the following major contributions:

1) In a first, it presents the position of critical word within the requested block and the corresponding flits for PARSEC 3.0 [3] and SPLASH-2x [4] benchmarks.
2) It describes the difference in arrival times of the first and last flit of an incoming data block and how it impacts...
3) It proposes a modified version of the popular early restart optimisation [2] by considering the insights from (1) and (2), which performs better than the original.

II. DATA CRITICALITY IN APPLICATIONS

In a multi-threaded application, multiple tasks (threads) may run concurrently and independently by using the shared resources. This is the reason why multi-threaded applications utilise the resources of many-core systems better. Current many-core systems like Intel Xeon Phi Processor (2016) [5], Princeton Piton Processor (2015) [6], MIT Scorpio Processor (2014) [7], and others have private L1 caches and a shared L2 cache. In most of these processors, the L2 cache is divided into multiple banks and distributed across all the cores, as shown in Figure 1. When the critical word is not found in the L1 cache (miss), the core requests the word from the corresponding L2 cache bank. The entire block containing the critical word is transferred from L2 to L1 cache (refer Figure 1). In a conventional system, even though the core requires only the critical word to resume its execution, it is made to wait till the arrival of the entire block. We know that a block contains multiple words, so imagine a scenario where the very first word of the block is the critical word. The core could resume its execution after the arrival of the first word, but instead, it needs to wait till the last word of the block. Hence we are motivated to profile state-of-the-art multi-threaded applications to know the pattern in which critical words are spread in their corresponding block. This insight will help us to understand how popular memory access optimisations like Early Restart and Critical Word First [2] can benefit the corresponding applications (explained in Section III).

We profile PARSEC 3.0 [3] and SPLASH-2x [4], the two most popular suite of multi-threaded benchmarks. We model an equivalent implementation of Intel Xeon Phi Processor 7235 [8], one of the latest many-core systems, on gem5 simulator [9]. Our system configuration is given in Table 1 for reference. We profile those data requests for whom the critical word was not found in the L1 cache. These are the requests that travel through the underlying NoC to reach L2 cache bank and get data, thus suffers NoC related delay [1].

To the best of our knowledge, this profiling is a first of its kind for any multi-threaded applications. Figure 2 shows the average position of critical word in the corresponding blocks requested from L2 cache. To understand with an example, during the entire run of blackholes benchmark from PARSEC 3.0 suite, for 67.20% of the time, the first word is the critical word, for 3.17% of the time, the second word is the critical word, for 8.17% of the time, the third word is the critical word and so on. There is a very interesting trend: the first word is the critical word for most of the requested blocks. This pattern is observed for the majority of the benchmarks of both PARSEC 3.0 and SPLASH-2x suites even though they are from diverse domains like computer vision, media processing, computational finance, enterprise servers, animation physics, high-performance computing, etc. However, the trend is unusual but not unreasonable, as the existing literature has proof of critical word regularity [10][11]. Literature states that it is reasonable to expect that data in a given region may be accessed in similar order on multiple occasions.

While explaining the individual memory access patterns for each of the benchmarks is beyond the scope of this brief, we give some common characteristics that justify the pattern on the location of a critical word. Benchmarks that traverse through data arrays exhibit critical words near the beginning of the data block, most often to word 0. Also, the benchmarks having strided access with the smallest stride length of 0 have word 0 as the critical word. On the other hand, there are also benchmarks like canneal and radix, where the critical word is somewhat uniformly distributed. Benchmarks whose memory accesses are generated due to pointer chasing exhibits better distribution of the critical word. Based on these observations, specific memory access optimisation can be implemented for a class of applications exhibiting a specific behaviour to reduce the miss penalty of the critical word and improve performance.

III. CRITICALITY AWARE MANY-CORE SYSTEMS

The most popular memory access optimisations to reduce miss penalty of the critical word are early restart and critical word first [2]. In early restart, as soon as the critical word is received at the L1 cache, it is forwarded to the processor to resume its execution without waiting for the entire block. In critical word first, the critical word is forwarded out-of-order...
Table 2: Position of critical word in the corresponding flits. Note that head flit (H) does not carry any words of the data block and hence its corresponding column is left empty.

| #  | Suite          | Benchmark        | Flits of an incoming requested block |
|----|----------------|------------------|--------------------------------------|
|    |                |                  | H | B0 | B1 | B2 | T  |
| 1  | PARSEC 3.0     | blackscholes     | 70.37 | 11.94 | 7.95 | 9.74 |
| 2  | PARSEC 3.0     | bodytrack        | 45.90 | 17.91 | 17.38 | 18.81 |
| 3  | PARSEC 3.0     | canneal          | 54.49 | 17.20 | 13.38 | 14.93 |
| 4  | PARSEC 3.0     | facesim          | 82.06 | 7.06 | 5.40 | 5.48 |
| 5  | PARSEC 3.0     | ferret           | 67.60 | 15.04 | 8.56 | 8.80 |
| 6  | PARSEC 3.0     | flundaminate     | 67.47 | 14.34 | 8.23 | 9.96 |
| 7  | PARSEC 3.0     | freqmine         | 57.50 | 13.67 | 12.32 | 16.51 |
| 8  | PARSEC 3.0     | rthread          | 45.59 | 20.08 | 16.26 | 18.07 |
| 9  | PARSEC 3.0     | swaptions        | 56.33 | 14.21 | 14.04 | 15.42 |
| 10 | SPLASH-2X      | barnes           | 43.70 | 14.69 | 19.4 | 22.21 |
| 11 | SPLASH-2X      | cholesky         | 67.19 | 12.27 | 10.26 | 10.28 |
| 12 | SPLASH-2X      | fft              | 39.10 | 14.69 | 7.14 | 39.07 |
| 13 | SPLASH-2X      | fmm              | 50.46 | 15.19 | 13.94 | 20.41 |
| 14 | SPLASH-2X      | lu_cb            | 70.99 | 6.37 | 4.32 | 18.32 |
| 15 | SPLASH-2X      | lu_ncb           | 58.41 | 34.25 | 3.70 | 3.64 |
| 16 | SPLASH-2X      | ocean_cp         | 58.96 | 14.55 | 13.27 | 13.42 |
| 17 | SPLASH-2X      | radix            | 37.68 | 22.81 | 15.47 | 24.04 |
| 18 | SPLASH-2X      | raytrace         | 45.03 | 22.51 | 24.03 | 8.43 |

by the L2 cache to be received as the first word in the L1 cache to resume processor execution at the earliest. In NoC based many-core systems, everything travels as packets, including data blocks. Due to limited on-chip channel width, packets are further divided into multiple flits. A head flit (H) carries the packet (message) header containing the routing information and does not carry any part of the data block. Multiple body flits (Bi), ended by a tail flit (T) carries the data block from source to the destination. Hence, a data block (of 8-words, refer Table 1) is transferred as a sequence of head flit, followed by the body flits (of 2-words each) and a tail flit (of 2-words) (H, B0, B1, B2, T). Table 2 presents the percentage of critical words that fall on different flits of a data block.

To understand the observation, when the requested data block in blackscholes benchmark of PARSEC 3.0 suite is transferred through flits, 70.37% of the time, critical words are in flit B0, 11.94% in flit B1, 7.95% in flit B2 and 9.74% in the tail flit T. It can be seen that the first body flit (B0) contains the critical words most of the time. It was evident from the fact that most of the critical words are the first word of a data block (refer Figure 2) and B0 carries the first two words of the block. Hence, early restart optimisation can be very effective in these kinds of applications. Critical word first optimisation involves sending the critical word in the first flit by allowing out of order travel. Since by their very nature, the majority of the applications have their critical word in the first flit itself, critical word first might not be required. Avoiding critical word first also brings in the advantage of avoiding the complexity of sending the word out of order and then reordering the words at their destination.

Both early restart and critical word first optimisations are oblivious of the underlying on-chip communication infrastructure. These optimisations were introduced in the era of bus based on-chip communication, where a data block is transferred as a continuous stream of words. Hence, the data block is transferred within a fixed time, and the core could resume execution at the earliest as per the corresponding optimisation. However, modern many-core systems use NoC based on-chip communication where the data block is transferred as multiple flits in a discrete fashion. On their way to the destination, flits experience indefinite router delay due to on-chip congestion. As a result, the effectiveness of early restart and critical word first reduces in many-core systems.

To understand about the delay experienced by incoming flits, we conduct an experimental analysis for all the PARSEC 3.0 and SPLASH-2x benchmarks. We consider a metric from the literature called, Reply Difference Time (RDT) [12] which calculates the difference between the arrival of the first flit and last flit of a data block in the requesting core. Figure 3 shows the average, minimum and maximum time difference between the arrival of the first and last flit of the data block. The minimum RDT remains 4 for both PARSEC 3.0 and SPLASH-2x benchmarks. It implies that all the flits reach back to back without any delay (ideal case). However, the maximum RDT is surprisingly high (during congestion): 39 for PARSEC 3.0 and 59 for SPLASH-2x benchmarks. Even the average RDT is 8.01 and 7.98, more than the minimum RDT meaning, flits are generally getting delayed. If memory access optimisations are made aware of the pros and cons of the underlying on-chip communication infrastructure, they may yield even better benefits. The purpose of this brief is not to provide NoC-aware implementations of all the existing critical word based memory access optimisations. Instead, we take just one of the most popular memory access optimisations, early restart, and demonstrate that an NoC-aware early restart is effective in significantly improving the overall system performance.

IV. NOC-AWARE EARLY RESTART OPTIMISATION

This section proposes an NoC-aware early restart optimisation in many-core systems based on the observations from Figure 2, Table 2 and Figure 3. For the ease of illustration, we call the original early restart optimisation as ER and our proposed version of NoC aware early restart as ER-NoC.

A. Critical Flit Identification

When the core (processor) needs a critical word from the private L1 cache, it sends a request to the L1 cache controller (L1 CTLR) giving the address of the corresponding data block which contains the word. L1 CTLR maps into the corresponding set using the set index bits of the requested address, as shown in Figure 4. After the set is identified, L1 CTLR checks the tag bits for hit/miss detection. The corresponding data lookup is also done in parallel to reduce

Figure 3: Reply Difference Time
memory access latency. If the tag checker returns true (cache hit), the requested data block is present in the L1 cache. L1 CTLR identifies the critical word using the offset bits of the given address and sends it to the processor. However, if the tag checker returns false (cache miss), the data block needs to be brought from the corresponding L2 cache bank through the underlying NoC. While the block is being fetched from the L2 cache bank, ER optimisation uses the offset bits to check for the arrival of the critical word. As soon as the critical word is fetched at L1 cache, it is sent to the processor to resume its execution, without waiting for the arrival of the entire block. While the processor resumes execution, the remaining words of the block are fetched in the background. Since data transfer is still performed at block-level granularity, the underlying cache coherence remains unaffected.

We define critical flit as the flit carrying the critical word of the block through the underlying NoC. The proposed ER-NoC optimisation adds a tiny module at L1 CTLR to identify the critical flit, as shown in red in Figure 4. This module takes as input the offset bits and flit size to return a 2-bit value (00/01/10/11) called critical flit identifier (CFI). If the CFI value is 00, it means that the critical word will be transferred in the body flit B0, if 01 then B1, if 10 then B2 and if 11 then in the tail flit T. The proposed module added in L1 CTLR to get CFI runs in parallel with tag checker and data lookup modules and hence does not incur any additional delay in memory access latency. If the tag checker returns true, the CFI value is ignored as the requested block is already in L1 cache and there will be no flit transfer. However, if the tag checker returns false, the CFI value is added to the message/packet header when the block request is sent to the L2 cache bank.

**B. Critical Flit Prioritisation**

Upon receiving the request, the L2 cache bank controller (L2 CTLR) replies with the data block as multiple flits through the underlying NoC. For the proposed ER-NoC optimisation, L2 CTLR puts the corresponding CFI value back into the packet header (H) of the reply. When the head flit traverse through the NoC routers towards its destination, the CFI values are stored in a counter C in each router, as shown in Figure 5. ER-NoC modifies the traditional round-robin based priority policy to use the CFI counter for priority during routing and arbitration. The motive behind this move is to reduce the router delay for critical flits so that they reach the destination at the earliest. However, with priority, there is always a risk of starvation for lower priority flits. To minimise such a risk, our priority policy does not prioritise all the flits of a data block; rather, it just prioritises up to the critical flit. For example, if the critical flit is B1 for a data block, the proposed policy just prioritises B0 and B1 of that block. This is done because all the flits preceding the critical flit of the block should reach L1 at the earliest, then only the critical flit will reach. Once the critical flit is prioritised, the succeeding flits of the block (B2 and T) can reach L1 at their own pace as they are not required to resume processor execution.

When two flits of two different block compete for the same output port, one with the lower CFI counter is prioritised. When a flit wins the arbitration, the corresponding CFI counter is decremented by 1. This way, when the critical flit reaches the router, the counter becomes 0, meaning the highest priority. Hence the proposed policy prioritises only and until critical flit of a data block. Exploiting NoC infrastructure to prioritise based on data criticality reduces miss penalty and improve overall system performance. This brief does not claim that the proposed priority policy gives the lowest starvation and best performance. The purpose is to show that it is beneficial to make existing ER like memory access optimisations aware of the NoC infrastructure in NoC-based many-core systems.

**C. Experimental Evaluation**

We consider the following architectures for evaluation:

- **Baseline**: Without any optimisation.
- **ER**: Original early restart optimisation.
- **ER-NoC**: Proposed NoC-aware early restart optimisation.

The system configuration used for evaluation is already given in Table 1. Each multi-threaded benchmark runs 64 threads in 64 different cores of the system. We use sim-medium [3] input set and report the results for the run of entire region-of-interest. We consider miss penalty and system speedup as the performance metrics for evaluation. All the results are normalised with respect to the baseline architecture.

**L1 Miss Penalty**: It is defined as the number of cycles required to replace an existing data block from L1 cache with the incoming requested block. Miss penalty directly reflects the effectiveness of the proposed ER-NoC optimisation. Figure 6a and 6b shows the normalised miss penalty for PARSEC 3.0 and SPLASH-2x benchmarks suites. The existing ER optimisation reduces miss penalty by 6% for PARSEC 3.0 and 2% for SPLASH-2x. Exploiting the observed insights, our
proposed ER-NoC performs better and significantly reduces miss penalty by 12% and 10%, respectively. Our prioritisation scheme is not optimal as we can see it performs poorly for blacksholes when compared to ER. The focus is not to propose an optimal prioritisation scheme, rather highlighting the optimisation opportunities by exploiting the insights.

System Speedup: System speedup (S) is given by, $S = \frac{ExecTime_{baseline}}{ExecTime_{proposed}}$, where $ExecTime_{baseline}$ and $ExecTime_{proposed}$ are the execution time of baseline and proposed architectures, respectively. Figure 6c and 6d show the normalised system speedup for PARSEC 3.0 and SPLASH-2x benchmarks suites. As expected, reduction in miss penalty directly translates into the improvement of overall system performance. Our proposed ER-NoC optimisation achieves an average system speedup of 11% and 7% for PARSEC 3.0 and SPLASH-2x suites, respectively.

V. RELATED WORKS

The existence of critical word and memory access optimisations to prioritise critical words are available on the classic textbook by Hennessy and Patterson [2]. One of the first attempts to understand criticality for data requests from L1 to L2 cache is by Gieske [10]. He reported that for multi-programmed benchmark suites SPEC CPU 2000 and 2006, sufficient regularity in critical word exists. Exploiting this criticality information, quite a few optimisations are proposed in the recent past [11][13][14][15]. However, none of them explicitly studied the behaviour of critical words for multi-threaded benchmark suites like PARSEC 3.0 and SPLASH-2x.

VI. CONCLUSION AND FUTURE WORK

In this brief, we shared two crucial insights about running multi-threaded applications in NoC based many-core systems. First, we show that critical words follow a particular pattern when requested from the memory. Then, we show that flits carrying the critical words gets indefinitely delayed in NoC. Finally, taking an existing memory access optimisation as a case study, we demonstrated that an NoC-aware optimisation can effectively utilise the two observed insights to significantly improve the overall system performance. In our future work, we will explore the utilisation of the insights to optimise existing memory access optimisations and apply them for developing an optimal critical word prioritisation policy.

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