Normally-off sputtered-MoS2 nMISFETs with TiN top-gate electrode all defined by optical lithography for chip-level integration

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We demonstrate chip-level integrated n-type metal–insulator–semiconductor field effect transistors with a sputtered molybdenum disulfide (MoS2) thin channel and titanium nitride top-gate electrode all defined by optical lithography. The devices successfully exhibit a normally-off operation and the highest off-voltage. This is achieved by the single dielectric layer and forming gas annealing, which reduce the positive fixed charges in aluminum oxide (Al2O3) film and interface trap densities between the MoS2 and Al2O3 films, respectively. These normally-off MISFETs are suitable for internet-of-things edge devices with low energy consumption using two-dimensional materials in the future.

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In 2011, the single-layer MoS2 FET with exfoliation method was first reported with excellent channel charge modulation, high on/off-ratio and mobility of approximately 200 cm2 V−1 s−1, despite an extremely small thickness of 0.65 nm.1) The high mobility of MoS2 film is attributed to its layered structure and no dangling bond in the out-of-plane direction. The MoS2 film has flexibility and transparency as well.2,3) Therefore, transition-metal di-chalcogenides such as MoS2 have been attracting attention as channel materials for advanced field-effect transistor (FET), internet-of-things (IoT) and wearable devices.4) Considering on applications, the MoS2 films have been widely formed by thermal chemical vapor deposition (CVD) and metal-organic CVD (MOCVD).5,6) However, to synthesize large MoS2 film, a special treatment with alkali metal such as potterylene, 3,4,9,10-tetracarboxylic acid tetrapotassium salt is necessary, and it influences in the Fermi level.7−11) In contrast in the MOCVD, contamination derived from organic precursors is a concern.4,12) Therefore, we selected radio-frequency (RF) magnetron sputtering to synthesize a large and uniform MoS2 thin film, reducing contaminations because of the high vacuum process.13−15) Previously, we demonstrated chip-level integrated MoS2 nMISFETs using H2S annealing and the double layer aluminum oxide (Al2O3) passivating procedure for sulfur compensation and prolong process endurance of sputtered-MoS2 film. However, the normally-on operation remains to be solved.16) This is due to the fixed charge (Qf), interface trap densities (Qit) of double layer Al2O3 and high carrier densities in MoS2 film annealed in H2S ambient at 400 °C.15)

In this study, to reduce Qf and Qit, a single-Al2O3 dielectric layer and forming gas (F.G.) annealing were introduced. Moreover, the sulfur powder annealing (SPA) at 700 °C was newly applied to reduce carrier density. We integrated the sputtered-MoS2 nMISFET with all these techniques to achieve normally-off operation in accumulation mode.

In the experiments, Fig. 1(a) shows the process flow of chip-level integrated nMISFETs.17) As the S/D regions for n-type operation, the n-doped poly-Si contact was patterned via optical lithography and chemical dry etching in CF4 ambient. To remove the photo resist, piranha cleaning at 120 °C for 10 min was performed. A Mo film was deposited by sputtering at room temperature and a MoS2 film was formed at 700 °C in argon (Ar) gas.17−20) Just after the piranha cleaning to remove the residual Mo film,21) a 2.7 nm thick MoS2 film was directly deposited on the SiO2 substrate via RF magnetron sputtering at 400 °C with RF power of 50 W, distance of 230 mm between the target and substrate, Ar flow of 7.0 sccm, and partial pressure of 0.75 Pa.13,22) The MoS2 film was annealed via SPA at 700 °C under 100 Pa for 1 h to compensate for the sulfur vacancies and suppress the carrier density.15) As a dielectric layer, a single Al2O3 film was deposited on the MoS2 film by atomic layer deposition (ALD) method at 300 °C. After the isolation of the MoS2 channel region via optical lithography and reactive ion etching (RIE) using Cl2 ambient, a 50 nm thick SiN film was deposited on the patterned photo resist via sputtering. After lift-off process, a residual SiN sidewall encapsulated the MoS2 channel with Al2O3 film to prolong its endurance. A 150 nm thick titanium nitride (TiN) top-gate electrode was deposited through sputtering, and etched via optical lithography and RIE using Cl2 ambient. Therefore, the single Al2O3 gate-dielectric with SiN sidewall is realized to reduce Qf values. S/D contact holes through the Al2O3 film were opened using diluted hydrogen fluoride, and contact metals with Ti of 20 nm and TiN of 30 nm were formed by sputtering and the lift-off process. Finally, the F.G. annealing was performed on the sputtered MoS2 channel at 300 °C for 30 min to reduce the Qf and Qit values, as shown in Fig. 1(b).23,24)

As results and discussion, a test elementary group (TEG) on a chip of 2.5 × 2.5 cm2 area was successfully fabricated, as depicted in plane scanning electron microscope (SEM) images in Fig. 1(c).17) The cross-sectional transmission electron microscope images in Fig. 2 exhibits the final gate-stack structure with the sulfurized MoS2 channel, single ALD-Al2O3 gate-dielectric, and TiN top-gate electrode. From Fig. 2(a), it is confirmed that the MoS2 film with
uniform thickness through 200 nm wide was preserved, and also that the single Al2O3 film with approximately 16.4 nm thick was uniformly formed. A four-layer MoS2 film with approximately 2.7 nm thick is successfully observed in Fig. 2 (b). Therefore, the thickness per layer is approximately 0.7 nm, which matches the reported thickness. In Fig. 3(a), the log(Id, Is, Ig)–Vgs characteristics at Vds = 1–5 V are depicted with only SPA, only F.G. anneal, and SPA & F.G. anneals having a drawn channel length (Lch) and width (Wmask) of 10 and 160 μm, respectively. When only F.G. annealing is performed, the field effect is not observed because the sputtered MoS2 film has sulfur vacancies, seriously. In contrast, when only SPA to compensate the sulfur vacancies is performed, the field effect is observed, however the off voltage (Voff) seems to be negative. Here, Voff is the voltage at the minimum current defined by off current (Ioff). When both SPA and F.G. annealing processes were performed, a normally-off n-type operation in accumulation mode was successfully realized. This is considered to be because of the simultaneous suppression of Qf and Qit values with sulfur compensation. The minimum subthreshold slope (SS), the maximum on/off ratio and drain-induced barrier lowering (DIBL) are approximately 800 mV dec⁻¹, 100 and 190 mV V⁻¹ respectively, which mean that the performance of our FETs is required to be improved. The If-Vds characteristics at Vgs = 0–4 V with SPA & F.G. anneals are shown in Fig. 3(b). The field effect and following pinch-off are remarkably observed, however the Schottky-type junction is still observed at small values of Vds. In addition, a negative differential conductance in Fig. 3(b) is observed due to the presence of parallel transistors which have different parasitic resistance. Furthermore, the on/off ratio in Fig. 3(a) is as small as approximately 10², which is still due to remaining parasitic resistance.

To extract the external parasitic resistance (Rext) and the effective channel length (Leff), the resistance dependence on the Lch value is depicted in Fig. 4. From the bunch of nMISFETs in the TEG, ΔL and Rext values were respectively extracted as −1.20 μm and 2.95 × 10¹⁰ Ω·μm, and also Leff is calculated as follows:

\[ L_{\text{eff}} = L_{\text{ch}} - 2\Delta L. \]  

(1)

2ΔL is attributed to the difference between the drawn and electrical channel lengths. The Rext value is higher than that of the CVD-MoS2 FET with back-gate electrode. Therefore, it is necessary to further suppress the parasitic resistance such as the contact resistance between the MoS2 and MoSi2 films.

To confirm whether Leff precisely expresses the electrical channel length, normalized gₘ characteristics by the Leff, Wmask of 160 μm, and overlap of 10 μm are shown in Fig. 5. From this figure, variation in gₘ values among the three Leff values are small, suggesting that the fabrication and measurements were successfully accomplished in a stable manner.
However, the $g_m$ value itself is small, and also the peak value of the field effect mobility with SPA & F.G. anneals is evaluated as 0.12 cm$^2$ V$^{-1}$ s$^{-1}$ through deducting $R_{	ext{ext}}$, $L_{	ext{eff}}$, and $V_{	ext{th}}$ values calculated as approximately 1.0 V using the $g_{m\max}$ method. The equivalent SiO$_2$ thickness of the Al$_2$O$_3$ film was calculated as 10 nm with the relative dielectric constant of Al$_2$O$_3$ film on the MoS$_2$ channel as 5.8. Therefore, to enhance $g_m$ and mobility values with normally-off operation, the grain size of the sputtered MoS$_2$ film needs to be enlarged to suppress the carrier scattering in such atomically thin channel by controlling the number of nucleation sites as compared to the CVD method.

In addition, the enlargement of grain size is expected to improve SS, on/off ratio and DIBL, because a small grain size having each small channel length and many grain boundaries deteriorates the quality of channel and interface between Al$_2$O$_3$ and MoS$_2$ films.

Figure 6 is the benchmarks of $I_{	ext{off}}$ and $V_{	ext{off}}$ with MoS$_2$ FETs. As shown in this figure, this study shows the
largest \( V_{\text{off}} \) of approximately 1.0 V and comparatively low \( I_{\text{off}} \) value of \( 10^{-6} - 10^{-7} \mu A \mu m^{-1} \). Here, \( I_{\text{off}} \) is the current when the channel resistance is relatively higher than the parasitic resistance. Therefore, it is indicated that our nMISFETs have the low standby power similar to other MoS\(_2\) FETs.

In conclusion, we successfully realized top-gate sputtered MoS\(_2\) nMISFETs integrated on a chip, which exhibited normally-off operation and the highest \( V_{\text{off}} \) value in accumulation mode. This is attributed to the reduction of \( Q_e \), \( Q_{\text{ox}} \), and carrier density values by a bunch of process-integration improvements. Although the mobility of 0.12 cm\(^2\) V\(^{-1}\) s\(^{-1}\) was still low, our \( I_{\text{off}} \) value was comparable with previous reports elsewhere. Therefore, this chip-scale 2D device integration scheme helps for future applications such as the IoT and wearable electronics with low energy consumption.

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