Transient Analysis of DC-link voltage for Z-Source Converter Considering Parasitic Parameters

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Abstract

This paper now presents an equivalent circuit model and transient analysis of a voltage-type Z-source impedance converter (ZSC) with circuit stray parameters and parasitic parameters existing in passive component of ZSC taken into consideration. Through detailed analysis, the paper studies unwelcome high frequency parasitic oscillation phenomena of the DC-link voltage. The non-linear constitutive differential equations are set up to characterize the transient behavior in the time domain. Simulation results obtained using saber software and experimental results obtained using a laboratory prototype are presented, show parasitic oscillation phenomena of the DC-link voltage, and the simulation results agreed approximately with the experimental ones.

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Keywords: Z-Source Converter; Parasitic Parameters; Equivalent Circuit Model; Transient Analysis; Parasitic Oscillation

1. Introduction

Power inverters are increasingly being used in modern energy conversion systems, including uninterruptible power supplies, motor drives. Z-source inverters are new single-stage electronic power converters with both voltage-buck and boost capabilities. The general Z-source converter (ZSC) structure, which consists of inductors and capacitors connected in X shape to couple the inverter circuit to the dc voltage source, as shown in Fig. 1(a). Its operating principle has been described in [1].

Due to the obvious advantages of ZSC, it has been adopted for various applications, such as fuel cell energy conversion systems [1] and motor drives [2-3]. So far, some of the currently available literature [4–8] mainly focuses on steady-state analysis, mathematical ac small-signal analysis, or controller design from different perspectives including various loading and, therefore, not attempted in this paper. In all these literatures, only the parasitic resistances of inductors, either/or the equivalent series resistance (ESR) of capacitors are considered, which doesn’t fully represent the converter high-frequency characteristics. The effect of equivalent series inductance (ESL) is usually neglected when the converter performance is analysed and evaluated. However in power converter applications, the ESR and ESL introduce DC-link voltage spike and possible circuit resonance with other components or parasitic elements in the circuit effects on the converter performance.

Therefore, this paper presents a more accurate equivalent circuit model of a voltage-source type Z-source converter considering detailed parasitic parameters, which has not been previously attempted. Furthermore, the parasitic oscillation phenomena of the DC-link voltage are discussed by through mathematical formulation.
and time domain analysis. The next section of this paper is to establish equivalent circuit models for ZSC with
detailed parasitic parameters taken into consideration, and presents the transient analysis of DC-link voltage.
Simulation results using obtained based on Saber simulation platform are presented to validate the
effectiveness of the equivalent circuit models. Experimental results obtained using laboratory prototypes are
explored and compared with the simulation ones.

2. Equivalent circuit of ZSC

The ESL plays a very important role on capacitor high frequency (HF) performance, which significantly
affects the DC-link voltage. The ESL and capacitance can resonate and make a capacitor perform like an
inductor at HF range; therefore it is necessary to consider the ESL of capacitors.

For this work, the VS-type Z-source impedance network is analysed, and its equivalent circuit in which the
load is in parallel with an active switch as shown in Fig. 1, where the parasitic resistances of inductors, ESR
and ESL of capacitors, and an input diode are clearly indicated (The forward voltage drop of the input diode is
modelled by a fixed voltage drop $V_D$). The converter circuitry and external load are replaced by a single
switch and a series RL connected in parallel to simplify the modelling. $C_T$ is a total capacitor of an equivalent
capacitor of the switch’s antiparallel diode and parasitic capacitor of the DC-link. Since the on-resistance of
switch S is much smaller than the load impedance, it is neglected in the modelling and analysis.

![Fig. 1 Equivalent circuit considering parasitic parameters](image1)

![Fig. 2 Equivalent circuit of active state](image2)

The operating state of the impedance network is decided by the states of the input diode and switch S. The
possible operating states and the steady state behaviour of a Z-source inverter have been analysed in [3,8].
This paper only focuses on three typical operating states. The equivalent circuits and characteristics of these
three operating states can be described separately, as given in the following sections by considering the
presence of parasitic parameters.

3.1 Active state

As can be seen in the equivalent circuit given in Fig. 2, the switch S is turned off, and the diode is
conducting. The converter is in a non-shoot through state. The equations that define the active state are given
by:

$$v_{dc} = v_{L_1} + i_{c_1} R_{c_1} - v_{C_1} - L_{c_1} d i_{c_1} / dt - R_{c_1} i_{c_1}$$

$$i_{c_1} = i_{c_1} + i_{load} = i_{L_1} + i_{C_2} + i_{load}$$

Assuming that, the Z-source capacitor voltage and the Z-source inductor current are constant during this
period. Since the ESL of capacitors is much smaller than the Z-source inductor, it is neglected in the high
frequency parasitic oscillation analysis of the DC-link voltage. Then the simplified equivalent circuit of active
state can be seen in Fig. 3.

![Fig. 3 Simplified equivalent circuit of active state](image3)
Fig. 3 Simplified equivalent circuit of active state

Fig. 4 Equivalent circuit of DCM state

Where \( L_x = L_{C_1} + L_{C_2} \), \( R_x = R_{C_1} + R_{C_2} \)

\[
V_i = V_{C_1} + V_{C_2} - (V_{in} - V_D) = 2V_c - V_{in} + V_D
\]

(2)

we get

\[
L_x \frac{d_i_{L}}{dt} + R_i_{L} + v_{dc} = V_i
\]

\[
i_{L} = C_T \frac{dv_{dc}}{dt} + i_{load}
\]

\[
v_{dc} = L_{load} \frac{di_{load}}{dt} + R_{load}i_{load}
\]

The capacitor voltage is higher than the input voltage during boost operation when there are shoot through states; thus, the inductor current decreases. As time goes on, the inductor current keeps decreasing to a level where the input current or the diode current is decreased to zero; this state ends, and the inverter enters to a new state.

3.2 Discontinuous current mode (DCM) state

In this state, the switch \( S \) remains in the off state as shown in Fig. 4. The current through the diode becomes to zero and the diode is turned off. This state is undesirable and is to be avoided by proper sizing of the inductors and capacitors of the impedance converter.

This state doesn't contribute to the power conversion process and should be avoided. Thus, detailed transient analysis is not attempted in this paper.

3.3 Shoot through state

The circuit is in a switch shoot-through zero state as shown in Fig. 5. The diode is reverse biased, and the capacitors charge the inductors. The voltage source at the input terminals of the ZSC is disconnected. And there is a source free series RLC circuit at the output terminals.

Fig. 5 Equivalent circuit of shoot through state

Fig. 6 DC-link voltage with parasitic voltage

3. Transient characteristic

3.1 Active state

The equation (3) can be simplified by making the assumption that \( L_x \parallel L_{load} \) and \( R_x \parallel R_{load} \),

\[
L_x C_T \frac{d^2 v_{dc}}{dt^2} + \frac{L_x}{R_{load}} \frac{dv_{dc}}{dt} + \frac{R_{load}}{C_T} \frac{dv_{dc}}{dt} + v_{dc} = V_i
\]

(4)

As we know, it is difficult to derive the analytical closed-form of \( V_{dc} \) from the differential Eq. 4. But we can discuss the effect of parasitic parameters on parasitic voltage of DC-link. \( L_x, C_T, R_{load}, L_{load} \) and \( R_x \) both will affect the additional parasitic voltage. \( R_{load} \) and \( L_{load} \) determine the time required to reach steady state of DC-link voltage. \( L_x \) is one of the key components which significantly affect the DC-link voltage spike.

For this case, the input data of the system can be listed as,
\[ V_{in} = 48V, V_D = 1.5V, R_{load} = 5\Omega, L_{load} = 100\mu H, C = 300\mu F, R_C = 0.055\Omega, L_C = 100nH, C_T = 1\mu F, \text{ shoot through duty cycle } D = 0.1. \]

Fig. 6 shows \( V_{dc} \) with parasitic voltage.

### 3.2 Shoot through state

The DC-link voltage equation for this state is

\[ v_{dc} = v_c = \frac{A_1}{C_1} + \frac{A_2}{C_2} e^{st} \]

\[ s_1 = \frac{R_{load}}{2L_{load}} + \sqrt{\frac{R_{load}}{2L_{load}}} \frac{1}{L_{load}C_T} \]

\[ s_2 = \frac{R_{load}}{2L_{load}} - \sqrt{\frac{R_{load}}{2L_{load}}} \frac{1}{L_{load}C_T} \]

Where the constants \( A_1 \) and \( A_2 \) are determined from the steady values \( i_{load} \) and \( di_{load}/dt \) of non-shoot through state.

### 4. Simulation and experimental results

Computer simulation for circuit model is carried out using Saber software. A ZSC converter prototype has been designed and built in the laboratory. As shown in this section, simulation results agree well with the experimental values. The operational conditions and electrical specifications used in simulation and experiment are given below.

\[ C = 300\mu F, L = 36.5\mu H, \text{ switching frequency } f_s = 20kHz. \]

Fig. 6 shows simulation and experimental waveforms of ZSC operating at boost mode under the test conditions of \( V_{in} = 30V, R_{load} = 5\Omega, L_{load} = 200\mu H, C_T = 10\mu F, L_C = 160nH, R_C = 0.055\Omega, D = 0.2. \]

From Fig. 7, the \( V_{dc} \) was boosted and the unwelcome high frequency oscillation phenomena of \( V_{dc} \) and capacitor voltage \( V_c \) can be seen clearly. Then from Fig. 7(a) and (b), one can see both waveforms contain a damped oscillation at the time of the step change in the duty cycle. And the damped oscillation seen in \( V_c \) have the same characteristics with the damped oscillation seen in \( V_{dc} \) except the magnitude of the oscillation is halved in the former case.

**Fig. 7(a)** Simulation result of Boost-mode operation (top: \( V_{dc} \); bottom: \( V_c \))

**Fig. 7(b)** Experiment result of Boost-mode operation (top: \( V_{dc} \); bottom: \( V_c \))

**Fig. 8** shows simulation and experimental waveforms of ZSC operating at DCM state under the test conditions of \( V_{in} = 24V, R_{load} = 30\Omega, D = 0.15. \) The inductor current has high ripple and becomes discontinuous, and the output voltage gets distorted.

**Fig. 8** Simulation result of DCM mode operation (top: \( V_{dc} \); bottom: \( V_c \))
5. conclusion

A more accurate equivalent circuit model considering parasitic parameters has been established to study the transient behaviours of the DC-link voltage in ZSC. Computer simulation results are provided to verify the effectiveness of the proposed equivalent circuit. Experimental results obtained by a laboratory prototype propose parasitic oscillation phenomena caused by parasitic parameters, and show very good agreement with respect to the theoretical predictions and simulation results.

Although this paper has focused on modelling and parasitic oscillation analysis for ZSC, issues related to the method for suppressing the DC-link parasitic voltage can be discussed in future publications.

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