Effect of input phase mismatch in Doherty power amplifiers

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Abstract: In this paper, a new method is proposed to calculate transconductance ratio of the main and the peaking transistor of a Doherty power amplifier (DPA) which employs output matching circuits and offset lines. Cascade ABCD two-port parameters are used to analyze output section of the DPA. It is shown that output matching circuits has impact on the magnitude and the phase of the transconduction ratio. The effect of the input phase mismatch on the output power and efficiency is analyzed analytically. A 100 W dual drive Gallium Nitride (GaN) Doherty power amplifier is realized to experimentally verify the results. The drain efficiency measured as 68% at the correct phase, 65% for 30° input phase mismatch and 56% for 45° input phase mismatch.

Keywords: Doherty power amplifier, GaN HEMT
Classification: Microwave and millimeter-wave devices, circuits, and modules

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1 Introduction

The multimedia applications and services require high data rate in both wired and wireless communication systems. For the wireless communication the demand for
high data rate has motivated the use of carrier aggregation (CA) up to 100 MHz in LTE-Advanced. One of the main practical challenges that come with CA is the severe increase of peak-to-average power ratio (PAPR) of the corresponding generated time domain OFDM signal, thus affecting the power amplifier efficiency [1]. To ensure high efficiency at a large back-off power (BOP) from the saturation power, various efficiency enhancements techniques have been studied [2, 3, 4, 5]. Among those efficiency improvement techniques, Doherty power amplifiers have been widely investigated to provide high efficiency and linearity. Doherty power amplifiers still have importance in latest wireless communication systems such as 5G and mm-wave [6].

A basic DPA comprises two amplifiers, connected at their outputs by a quarter-wave transformer, as shown in the Fig. 1. The main amplifier operates continuously, while the peaking amplifier only operates at higher power levels starting from the BOP point. After the point of BOP, the peaking amplifier contributes to the output power of the DPA.

In a DPA, efficiency improvement is achieved by providing high impedance termination to the main amplifier to reach an early saturation at the back of power (BOP). For increasing levels of the amplifier’s input drive beyond the BOP, the impedance termination of the main amplifier is gradually reduced by the quarter-wave impedance transformer such that the output power keeps increasing while the main amplifier remains in the saturation region (Fig. 2) [7]. For the asymmetrical DPA’s the BOP point can be lower than the basic DPA to ensure high efficiency at high PAPR. In order to ensure the saturation condition for the main amplifier, the peaking amplifier’s current should increase properly regarding to the BOP point of the Doherty power amplifier (Fig. 3). This situation is analyzed for the ideal DPAs that employ only two ideal amplifiers and a quarter-wave impedance transformer [8].

Due to the high nonlinearity of the RF power transistors, simulation and optimization tools with computer aided design (CAD) are widely used for the power amplifier design to achieve higher power efficiency and gain. However, there
are many system parameters which affect the power efficiency and gain. Therefore, analytical expressions are not only useful to validate the numerical results, but also may help to understand the mechanism behind the effects which limit the performance of the power amplifier.

Comprehensive analyses have been done for Doherty power amplifiers starting from early 2000s [9, 10, 11, 12, 13]. The full load matching circuits is demonstrated by using offset lines at the output of the matching circuits for proper Doherty operation at both low and high power region [14]. An analytical analysis is proposed by using s-parameter of the output branches of the main and the peaking amplifiers to calculate offset lines [15]. Similar analysis has been done by using cascade ABCD two port parameters and effect of offset lines is demonstrated analytically considering saturation conditions by using voltage and current equations [16].

In this paper, the magnitude and the phase of the transconductance ratio of the peaking and the main devices is derived by using cascade ABCD two-port parameters for a DPA with output matching networks and offset lines. Effect of the input phase mismatch is analyzed and a 100 W GaN DPA is designed and manufactured to verify results experimentally.
2 Analytical analysis of the Doherty power amplifier

For the basic DPA, maximum efficiency occurs at half of the maximum input voltage. At this point, the output power is 6 dB below from the maximum output power. Voltage and current characteristics are shown in Fig. 2 for the basic DPA. Raab analytically showed the possibility of extending the peak efficiency region over a wider range of output power [17]. In this case, the slope of the output current of the peaking amplifier should be higher than the slope of the output current of the main amplifier.

2.1 Analysis of the basic Doherty power amplifier

As it can be seen from Fig. 1 and Fig. 3, at BOP point, \( V_I = V_{I,BOP} \), output current of the peaking amplifier \( I_p = 0 \), and \( V_m = V_{DC} \). At low power region, because of the property of the quarter-wave transformer, the impedance seen by the main amplifier is \( Z_0^2 / R_L \), where \( Z_0 \) is the characteristic impedance of the quarter-wave transformer and \( R_L \) is the load. Then we can write following equation:

\[
(V_m)_{BOP} = V_{DC} = \frac{V_{I,BOP}}{V_{I,max}} \frac{Z_0^2}{R_L}.
\]  

(1)

Similarly, at the peak envelope power (PEP), using two-port cascade ABCD parameters of the quarter-wave transformer, following equation can be written [17]:

\[
(V_m)_{PEP} = V_{DC} = Z_0 \left[ \frac{Z_0}{R_L} I_{m,max} - jI_{p,max} \right].
\]  

(2)

By Eq. (1) and Eq. (2), maximum current ratio of the main and peaking devices can be found as [18]:

\[
\frac{I_{p,max}}{I_{m,max}} = \frac{V_{I,max} - V_{I,BOP}}{V_{I,BOP}} = -j(\gamma - 1),
\]  

(3)

where \( \gamma = V_{I,max} / V_{I,BOP} \). The pure imaginary value of the ratio indicates that the phase of the peaking device’s current must be \(-90^\circ\) comparing the main device’s current. Assuming that RF drive levels are equal at the input of the main and the peaking devices, the transconductance ratio of the peaking and the main devices will be:

\[
\frac{g_{mp}}{g_{mm}} = -j\gamma.
\]  

(4)

where \( g_{mp} = I_{p,max} / (V_{I,max} - V_{I,BOP}) \) and \( g_{mm} = I_{m,max} / V_{I,max} \). Noting that current rating of the devices should satisfy Eq. (3). Eq. (4) can be satisfied with a 90\(^\circ\) input phase offset line and proper input drive levels related with main and peaking amplifier’s transconductance ratio [19, 20]. Noting that Eq. (4) is derived for an ideal Doherty configuration which employs two ideal current sources and a quarter-wave transmission line transformer. However, considering that the active devices are not ideal, the use of impedance transformation networks (ITN) is required to draw maximum power from the device. Additionally, for the proper active load modulation, offset lines should be used at the output of both the main and the peaking amplifier [14].
2.2 Calculation of the transconductance ratio of the main and peaking amplifiers with output matching circuits

The DPA’s output section with output matching circuits and offset lines shown in Fig. 4. Output parasitic capacitor of the transistors is included in the impedance transforming networks [15].

\[
V_m = \frac{[B_m(C_pR_L + D_p) + A_mD_pR_L]I_m}{D_m(C_pR_L + D_p) + C_mD_pR_L} + \frac{[A_mD_m - B_mC_m]R_L]I_p}{D_m(C_pR_L + D_p) + C_mD_pR_L}, \quad (5)
\]

\[
V_L = \frac{(D_pI_m + D_mD_p)R_L}{D_m(C_pR_L + D_p) + C_mD_pR_L}. \quad (6)
\]

where \(V_m\) and \(V_p\) are drain voltages, \(I_m\) and \(I_p\) are the output current of the main and peaking branches respectively, and \(V_L\) is the load voltage. \(V_m\) and \(V_L\) depend on the impedance transforming network parameters \((T_{ITNm} \cdot T_{ITNp})\), offset lines \((T_{offsetm} \cdot T_{offsetp})\) and quarter-wave transformer \((T_{2/4})\) parameters as well as the load, \(R_L\). Independent variables are the main and the peaking transistors output currents, \(I_m\) and \(I_p\) respectively.

As discussed in the previous section, the main principle of the proper operation of the Doherty amplifier is to keep the main amplifier on the limit of the saturation region via the judicious active load modulation. This approach maximizes the efficiency of the amplifier keeping its operating point between BOP and maximum output power. In order to satisfy this rule, \(V_m\) should be constant after the BOP point.

Assuming same \(V_f\) is applied to the main and the peaking amplifier, we can write:
\[ I_m = g_{mn} V_I, \quad (7) \]
\[ I_p = g_{mp} V_I. \quad (8) \]

Rewriting (5) by using (7) and (8):
\[ V_m = \frac{[B_m(C_p R_L + D_p) + A_m D_p R_L] g_{mn} V_I}{D_m(C_p R_L + D_p) + C_m D_p R_L} + \frac{[(A_m D_m - B_m C_m) R_L] g_{mp} V_I}{D_m(C_p R_L + D_p) + C_m D_p R_L}. \quad (9) \]

After the BOP point, input voltage can be written as:
\[ V_I = V_{I,BOP} + V'_I, \quad V_I > V_{I,BOP}. \quad (10) \]

Considering that \( V_I = V_{I,BOP} \) and \( V'_I = 0 \) at the BOP point, then for the high power region we can write:
\[ V_m = V_{m,BOP} + \frac{[B_m(C_p R_L + D_p) + A_m D_p R_L] g_{mn} V'_I}{D_m(C_p R_L + D_p) + C_m D_p R_L} + \frac{[(A_m D_m - B_m C_m) R_L] g_{mp} V'_I}{D_m(C_p R_L + D_p) + C_m D_p R_L}. \quad (11) \]

At high power region, to satisfy \( V_m = \text{constant} = V_{DC} \), second and third term of Eq. (11) should be equal with opposite sign, then:
\[ \frac{[B_m(C_p R_L + D_p) + A_m D_p R_L] g_{mn} V'_I}{D_m(C_p R_L + D_p) + C_m D_p R_L} = - \frac{[(A_m D_m - B_m C_m) R_L] g_{mp} V'_I}{D_m(C_p R_L + D_p) + C_m D_p R_L}. \quad (12) \]

Resulting in:
\[ \frac{g_{mp}}{g_{mn}} = - \frac{[B_m(C_p + D_p/R_L) + A_m D_p]}{[(A_m D_m - B_m C_m) R_L]} \quad (13) \]

Noting that for reciprocal two-port circuit, we can write:
\[ A_m D_m - B_m C_m = 1 \quad (14) \]
thus:
\[ \frac{g_{mp}}{g_{mn}} = -[B_m(C_p + D_p/R_L) + A_m D_p] \quad (15) \]

For the basic Doherty amplifier without ITN and offset lines, it employs only quarter-wave transformer as shown in Fig. 1, the cascade ABCD two-port parameters will be:
\[ A_m = D_m = 0, \quad B_m = jZ_0, \quad C_m = j/Z_0, \]
\[ A_p = D_p = 1, \quad B_p = C_p = 0 \quad (16) \]

Then, transconductance ratio of the main and the peaking amplifiers:
\[ \frac{g_{mp}}{g_{mn}} = -jZ_0/R_L \quad (17) \]

where \( Z_0 \) is the characteristic impedance of quarter-wave transmission line and \( R_L \) is the load. Noting that Eq. (17) which is derived from Eq. (13) for an ideal basic Doherty amplifier is given in the literature first by Raab [17]. Eq. (13) is generalized form of the transconductance ratio for a Doherty amplifier as shown in Fig. 4. Input phase offset at the peaking amplifier’s input should be 90° for an ideal Doherty amplifier as explained in the previous section [18], but this is not the case for a Doherty amplifier that employs output matching circuits and offset lines. In that case the input phase offset, \( \theta_i \), will be:
\[ \theta_i = \angle \left[ j \frac{g_{mp}}{g_{mm}} \right] = \angle - \left[ B_m(C_p + D_p/R_L) + A_mD_p \right] \] (18)

Noting that, in order to satisfy the saturation condition, this input phase value is depending to the parameters of the output branches. Making the output currents in-phase at the summing point as reported in [21] and [22] may cause over saturation for both the main and the peaking amplifier. The phase differences between input branches of the main and the peaking amplifiers should be corrected as well [23].

In the next section, the saturation condition of the main amplifier will be investigated for different input phases by using equivalent circuit of the output branch of the realized 100 W GaN DPA. Then, effect of input phase mismatch on the power efficiency will be demonstrated.

3 Simulations and results

As discussed in [16] a dual drive Doherty power amplifier designed for UHF channel 61–69 (790–862 MHz). Main amplifier’s gate bias voltage is \(-1.54\) V, drain voltage is \(28\) V and drain current is set to \(700\) mA. Peaking amplifier’s gate bias voltage is \(-3.77\) V and drain voltage is \(28\) V. Outputs of the both amplifiers are combined by using the offset lines and quarter-wave transformer as shown in Fig. 5. The main and the peaking offset lines are also optimized with respect to the output power and efficiency [21]. The maximum drain efficiency of the manufactured DPA is 66\% at 51.3 dBm output power and the gain is 14 dB with the variation of \(\pm 1.5\) dB versus output power.

![Fig. 5. Schematic diagram of the realized 100 W GaN dual drive DPA.](image)

In order to validate the analytical analysis by simulation on the AWR design tool, output parasitic capacitors of NPT1010 transistor are included in \(ITN_m\) and \(ITN_p\) as explained in the preceding section. Then ABCD parameters of the main and the peaking branch are extracted by using two-port ABCD parameter simulation tool on the AWR as below:

\[
\begin{align*}
A_m &= 0.1326 - j0.00473, & B_m &= -0.1488 - j21.40 \\
C_m &= 0.000511 - j0.0467, & D_m &= 0.00631 - j0.299
\end{align*}
\]
Then, by using Eq. (15) and assuming the transconductance of the main amplifier is equal to one, the magnitude and the phase offset of the peaking transistor is calculated as 2.0469 and 81.142° respectively. Noting that for the ideal basic DPA, the magnitude and the phase offset would be 2 and 90° respectively.

To simulate the input phase mismatch effect on PA’s efficiency a new schematic is created on AWR which is shown in Fig. 6.

Similarly the peaking branch is added to the schematic. Two controlled current source are used for each branch to simulate the load voltage, the drain voltages of the main and the peaking amplifiers. As it can be shown in Fig. 7, the load voltage, the main and the peaking drain voltages are simulated versus the input drive level. The simulation is done for three different input phase: correct input phase offset, 30° mismatch and −30° mismatch. At the high power region, the peaking amplifier
starts to operate. At the correct input phase offset which is 81.142°, the main drain voltage is constant in the high power region. But both 30° and −30° input phase mismatches, the main drain voltage is higher than the saturation limit which cause over saturation and lower efficiency.

There is no load voltage changes observed in the Fig. 8 since the saturation condition is not applied to the simulation. In practice, the drain voltages are limited with the DC supply voltage. This voltage limitation is simulated by using diodes at the output of controlled current source as shown in Fig. 6.

![Fig. 8. Simulation results for the load voltage, main and peaking drain voltages versus input phase mismatch at the maximum input drive level for both DC voltage limitation and without DC voltage limitation, and drain efficiency with DC voltage limitation.](image)

The load voltage, the main and the peaking drain voltages are shown in Fig. 8 versus input phase mismatch at the maximum input drive level for both with DC voltage limitation and without DC voltage limitation. The simulated drain efficiency with DC voltage limitation is also shown in the figure. Noting that the main drain voltage is at the saturation limit, but the peaking drain voltage is lower than the saturation limit both for minus and plus input phase mismatches. The drain efficiency drop around the midpoint is not symmetrical as in the peaking drain voltage. Results of the simulation of the load voltage, the main and the peaking drain voltages are verified in MATLAB environment.

The drain efficiency is simulated for various input phase mismatch by using different phase length for the transmission line. For the measurement, a digitally controlled phase shifter is used at the input of the peaking amplifier. Measurement results are shown in Fig. 9. As shown from the figure, drain efficiency decreases regarding to the amount of the input phase mismatches.
4 Conclusion

Active load modulation in Doherty power amplifiers ensures high power efficiency at the back-off power point by keeping the main amplifier at saturation limit. In this study, transconductance ratio of the peaking and the main amplifiers is derived using two-port ABCD parameters of the output section of the DPA. In order to satisfy the saturation condition, the magnitude of the transconductance of the peaking transistor should be properly selected or proper input drive level should be applied regarding to transconductance of the main transistor. The phase of the transconductance ratio should be satisfied with a proper circuitry; in addition to the correction of the phase mismatch at the input branches of the DPA. The aim of these corrections is not to make the output currents of the main and the peaking branches in-phase at the summing point, instead it is to prevent over saturation of the main amplifier, otherwise, the main amplifier will be over saturated, which results nonlinearity and lower efficiency in the high power region. Effect of the input phase mismatch on the drain voltages is analyzed by using AWR design tool. A 100 W GaN DPA designed and manufactured, then power efficiency degradation regarding to amount of input phase mismatch is demonstrated. The drain efficiency measured as 68% at the correct phase, 65% for 30° input phase mismatch and 56% for 45° input phase mismatch.