The prediction of the quality of results in Logic Synthesis using Transformer and Graph Neural Networks

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In the logic synthesis stage, structure transformations in the synthesis tool need to be combined into optimization sequences and act on the circuit to meet the specified circuit area and delay. However, logic synthesis optimization sequences are time-consuming to run, and predicting the quality of the results (QoR) against the synthesis optimization sequence for a circuit can help engineers find a better optimization sequence faster. In this work, we propose a deep learning method to predict the QoR of unseen circuit-optimization sequences pairs. Specifically, the structure transformations are translated into vectors by embedding methods and advanced natural language processing (NLP) technology (Transformer) is used to extract the features of the optimization sequences. In addition, to enable the prediction process of the model to be generalized from circuit to circuit, the graph representation of the circuit is represented as an adjacency matrix and a feature matrix. Graph neural networks(GNN) are used to extract the structural features of the circuits. For this problem, the Transformer and three typical GNNs are used. Furthermore, the Transformer and GNNs are adopted as a joint learning policy for the QoR prediction of the unseen circuit-optimization sequences. The methods resulting from the combination of Transformer and GNNs are benchmarked. The experimental results show that the joint learning of Transformer and GraphSage gives the best results. The Mean Absolute Error (MAE) of the predicted result is 0.412.

CCS CONCEPTS • Hardware → Electronic design automation → Logic synthesis • Computing methodologies → Machine learning

Additional Keywords and Phrases: logic synthesis, deep learning, transformer, graph neural network

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1 INTRODUCTION

As the intermediate layer of most electronic design automation (EDA) processes, logic synthesis is defined as the process of optimizing a given Boolean network and mapping it to a gate-level netlist while optimizing quality-of-results (QoR). In the pre-mapping phase of logic synthesis, researchers have developed several structural transformations to improve the QoR of the circuit [1]. Circuits are represented as And-Inverter Graphs (AIG) in the state-of-the-art academic logic synthesis tool ABC [2]. These technology-independent structural transformations are used to reduce the size of the graph to achieve circuit optimization. As the complexity of the design and technology grows, developers need to combine these structural transformations into logic synthesis optimization sequences (hereafter referred to as optimization sequences) based on their knowledge and after extensive iterative testing to meet the optimization goals. However, logic synthesis techniques lack predictability, and hence it is difficult for developers to know the performance of optimization sequences. Hence, predicting the performance of optimization sequences without actual testing is of great value [3].

Deep learning (DL) has developed rapidly in recent years. Through the powerful fitting ability of deep neural networks, it can learn a large number of mapping relationships between inputs and outputs, without requiring a precise mathematical representation between inputs and outputs. Hence, logic synthesis researchers aim to take advantage of advances in DL to facilitate the convergence rate of the logic synthesis phase.

In [4], [5], the logic synthesis optimization process is modeled as a Markovian decision process, and reinforcement learning algorithms incorporating graph neural networks are used to explore the design space. In [6], circuit area under delay constraints is minimized using reinforcement learning algorithm A2C. In [7], a milestone step by releasing the dataset is taken. Yu et al. [8] mapped Logic Synthesis Optimization to a multi-classification problem. The main idea is to use convolutional neural networks (CNN) to classify the logic synthesis optimization sequences encoded as one-hot to the best and worst. In [9], QoR prediction of optimization sequences for a specific design is implemented using Long Short-Term Memory (LSTM) networks. However, in [8], [9], the input to the neural network contains information about the optimization sequence only, and the neural network cannot learn information about the structure of the circuit. Hence, the trained network can only work for a specific circuit. In this work, a framework for predicting the QoR of unseen circuit-optimization sequence pairs is proposed. Specifically, graph neural networks (GNNs) are used to process adjacency and feature matrices containing circuit structure information to learn circuit structure features. The GNNs utilized are Graph Convolutional Network (GCN) [13], Graph Attention Network (GAT) [14], and GraphSage [15]. In addition, optimization sequences are treated as sentences in natural language and modeled as learnable embedding vectors. Advanced natural language processing (NLP) techniques are used to learn the features of the optimization sequences.

The main contributions of this paper are as follows:

- An optimization sequence feature extractor based on the NLP algorithm Transformer is proposed. The input is an optimization sequence that has been transformed into a vector by the embedding method, while the output is a feature vector extracted from the optimization sequence that can be used for downstream QoR prediction tasks.
- A circuit feature extractor is developed based on three typical graph neural networks, functioning to extract features of the circuit structure where the circuits are represented as adjacency matrix and feature matrix.
- A joint learning policy is proposed for the optimization sequence feature extractor and circuit feature extractor, enabling the model to predict the performance of unseen circuit-optimization sequence pairs. Furthermore, experiments are conducted on the nine methods resulting from the combination, and suggestions for their uses are given for different scenarios, providing a basis for experimental analysis of subsequent related problems in logic synthesis.
- The code for this work will be open source at https://github.com/Chenghao-Yang/QoR-Prediction.
2 FUNDAMENTALS

To understand the potential of deep learning for the problem of predicting the QoR of optimization sequences, preliminary knowledge about Transformer [12] and graph neural networks is presented. In addition, two classical NLP feature extractors CNN [10] and LSTM [11], which are used as baselines, are also introduced.

2.1 CNN Basics

A convolutional neural network contains a feature extractor consisting of a convolutional layer and a sub-sampling layer. A convolutional layer typically contains several feature maps, and each feature map consists of several rectangularly arranged neurons. A neuron is connected to only part of the neighboring neurons. The neurons in the same feature map share weights, where the shared weights are the convolutional kernel. The convolutional kernel is generally initialized in the form of a random algebraic matrix, and the kernel will learn to obtain reasonable weights during the training process of the network. The direct benefit of shared weights (convolution kernels) is to reduce the parameters in each layer of the network, while reducing the risk of overfitting. Subsampling, also called pooling, is generally available in the form of mean pooling and max pooling. Subsampling can be seen as a special kind of convolution process. Convolution and subsampling greatly simplify the model complexity and reduce the parameters of the model. The process of extracting optimization sequence features using CNN is shown in Section 4.1.3.

2.2 LSTM Basics

![Figure 1: LSTM unit illustration.](image)

Long short-term memory (LSTM) [11] is a recurrent neural network (RNN) architecture. It is to solve long-term dependency problems by adding control gates to recurrent units. As shown in Figure 1, a common architecture of an LSTM unit consists of cell, input gate, output gate, and forget gate. Input gates receive inputs from sequences and other units of the neural network and are trained to add information to the cell at an appropriate time. Similar to the input gate, the output gate learns to output the information from the cell at the appropriate moment. The forget gate learns the appropriate moment to remove information from the cell when it is no longer useful.

These gates consist of a sigmoid layer and a pointwise multiplication to allow selective passage of information.

2.3 Transformer Basics

The Transformer network architecture was proposed by Ashish Vaswani et al [12] and used for machine translation tasks. In contrast to previous network architectures, the encoder and decoder do not use a network architecture such as RNN or
Figure 2: Transformer Architecture.

CNN, but an architecture that relies entirely on attention mechanisms. As the model processes each input vector, self-attention helps the model to look at other positions in the input sequence to find relevant cues for better encoding. The basic architecture of the Transformer is shown in Figure 2, where the left half is the Encoder part and the right half is Decoder part. The transformer has six layers of such structure. In each layer, the Encoder converts the input sequence into an encoded representation, while the Decoder produces a new sequence as the output based on the encoded representation.

Since this work does not require converting the input optimization sequence to another sequence, the direct application of the transformer is not applicable. How to extract features of the optimization sequence using partial components of the transformer is shown in 4.1.2.

2.4 Graph Neural Networks

GNNs are neural networks that operate directly on graph data structures. Take learning the embedding vector of each node in the input graph for example. The features of node $v$ are represented by $x_v$, and the network learns to represent the node by a $d$-dimensional vector (state) $h_v$, which contains information about its neighborhood.

$$h_v = f(x_v, x_{e[v]}, h_{ne[v]}, x_{ne[v]})$$  \hspace{1cm} (1)

where $x_{e[v]}$ denotes the features of the edge connected to $v$, $h_{ne[v]}$ the embedding features of the neighboring nodes of $v$, $x_{ne[v]}$ the features of the neighboring nodes of $v$. $f$ is the transfer function that projects these inputs into the $d$-dimensional space. Since a unique solution for $h_v$ is being solved, Banach Fixed Point Theorem can be applied and the above equation can be rewritten as an iterative update procedure.

$$H^{t+1} = F(H^t, X)$$  \hspace{1cm} (2)

$H$ and $X$ denote all connections of $h$ and $x$, respectively. The output of GNN is calculated by passing state $h_v$ as well as feature $x_v$ to the output function $g$.

$$o_v = g(h_v, x_v)$$  \hspace{1cm} (3)

Both $f$ and, here, $g$ can be interpreted as feedforward fully connected (FC) neural networks.
GNN basic tasks are classified according to graph structure elements and can be divided into nodes, edges, subgraphs, and graph-related tasks. In this paper, GNNs are used to learn graph embeddings of circuits, which contain structural features of the circuits and can be used for downstream QoR prediction tasks.

3 MOTIVATION
There is a correlation between the structural transformations used to optimize the circuit. In other words, the use of structural transformations in conjunction with each other can produce different optimization effects. For example, in ABC, zero-cost replacements (rewrite-z) do not immediately reduce the number of nodes in the AIG graph, and other structural transformations are required to complete the optimization. Self-attention in Transformer processes each vector in the input sequence by computing the correlation of that vector with other vectors in the sequence and looking for relevant clues. Hence, the architecture of the transformer is well suited for extracting the features of optimization sequences. In addition, in ABC [2], circuits are represented as graphs (e.g. AIG), and a significant number of structure transformation algorithms are based on graph structures. In previous work [8], [9], the input to the neural network only contains information about the optimization sequence, and it is not possible to establish the correlation between the optimization sequence and the circuit structure. Hence, this paper combines a graph neural network with a joint policy to learn both optimization sequence features and circuit structure features. We aim to achieve QoR predictions for unseen Circuit-Optimization sequences.

4 APPROACH
The input and the architecture of the model for neural networks are mainly described. The input is the optimization sequence, which is converted into a vector representation after the embedding layer. The neural network architecture consists of an optimization sequence feature extractor and a circuit feature extractor which are used to predict the QoR of the optimization sequence for different circuits after adopting a joint learning policy.

4.1 Optimization Sequence Feature Extractor
The implementation of an optimization sequence feature extractor based on the Transformer is presented here. In addition, for a comprehensive comparison, the classical LSTM and the CNN used in [8], [9] are implemented as well.

4.1.1 Optimization Sequence Embedding
The input optimization sequence in this paper consists of seven ABC structure transformations, specifically refactor, refactor -z, rewrite, rewrite -z, resub, resub -z, balance, and a sequence of these seven structure transformations is assumed to be [rewrite, resub, refactor, balance]. In the following, we will show how to convert the optimization sequence into a vector that can be processed by the neural network.

First, the original seven structural transformations are used as dictionaries. Each structural transformation is considered as a word in natural language and is assigned an index of 0 to 6, respectively. To make the neural network learn better, the embedding matrix is further created. Each index is assigned three latent factors, that is, represented by a vector of length 3. For better illustration, we randomly initialize an embedding matrix for seven structural transformations:
The row numbers of the matrix correspond to the index values, and each row vector represents the embedding vector corresponding to the index. As an example, an optimization sequence [rewrite, resub, refactor, balance] can be considered as a sentence composed of a dictionary. By querying the indexes in the dictionary, the optimization sequence can be transformed to [2, 4, 0, 6]. By querying rows 2, 4, 0, 6 of the embedding matrix by indexes, respectively, the optimization sequence is represented as the following embedding vector:

\[
\begin{bmatrix}
-0.5706 & -0.2703 & 2.2453 \\
-1.1936 & -0.0705 & 0.3704 \\
-0.4093 & -1.1011 & 0.0790 \\
0.4327 & -0.9486 & 2.2643
\end{bmatrix}
\]

Each row represents a structural transformation performed at a one-time step. Note that not every structural transformation is replaced by a vector, but is replaced by the index used to find the vectors in the embedding matrix. The values of the entire embedding matrix are used as part of the training, as the model is trained, the embedding vector gets the appropriate values.

4.1.2 Transformer-based optimization sequence feature extractor

Here, how to use the partial modules in the transformer for optimization sequence feature extraction will be presented.

a) Computation of self-attention

As the core part of the transformer, optimization sequence feature extraction using the self-attention mechanism is introduced first. As shown in Figure 3, the structural transformations in the optimization sequence [rewrite, resub, refactor, balance] are transformed into vectors \(a_1, a_2, a_3, \) and \(a_4\) by the optimization sequence embedding in 4.1.1 and added with the position information \(e^i\), respectively. For position information \(e^i\), the method proposed in [16] is used in this paper, a
simpler method than the original transformer. This approach is similar to that of generating word vectors, where the position encoding is first initialized and then put into the training process to train a position vector for each position.

The next step is to compute self-attention. In the first step, each input vector \( a_i \) is multiplied with the parameter matrices \( W_Q, W_K, \) and \( W_V \) to obtain the query vector \( q_i \), the key vector \( k_i \), and the value vector \( v_i \), respectively. The second step is to compute the score. Figure 3 demonstrates the process of computing the self-attention vector for the first structural transformation 'rewrite'. During the computation, each structural transformation in the input optimization sequence needs to be used to score 'rewrite'. This score determines how much attention should be given to the rest of the input sequence when encoding the structural transformation 'rewrite'. It is computed by the dot product of the query vector of 'rewrite' with the key vector of each structural transformation. For example, the first score is the dot product of \( q_1 \) and \( k_1 \), and the second score is the dot product of \( q_1 \) and \( k_2 \). To make the gradient smoother, the obtained score is divided by \( d \) as follows:

\[
a_{1,i} = q_1 \cdot \frac{k_i}{\sqrt{d}} \tag{4}
\]

where \( d \) is the dimensionality of \( q \) and \( k \). Then, the softmax score is obtained by normalizing the scores using the softmax function with the following equation:

\[
\hat{a}_{1,i} = \frac{\exp(a_{1,i})}{\sum_j \exp(a_{1,j})} \tag{5}
\]

This makes the scores all positive and sum to 1. In the third step, each value vector \( v_i \) is multiplied by the softmax score and summed, which gives the output of the self-attention layer at the first position in the sequence, \( b_1 \). A similar calculation for the remaining \( a_2, a_3, \) and \( a_4 \) gives \( b_2, b_3, \) and \( b_4 \). The final self-attention matrix is formed by combining all the \( b_i \). In practice, the computation is performed as a matrix that can be accelerated by the GPU. To extend the ability of the model to focus on different positions, the multi-headed attention mechanism is further utilized.

![Figure 4: The process of computing multi-headed self-attention.](image)

In this paper, two heads are used and each head has an independent query, key, and value weight matrix. As shown in Figure 4, each attention head independently performs the same operation as the single head in the previous paragraph to obtain the corresponding \( b_i \). Matrices \( Z_0 \) and \( Z_1 \) are formed by combining the corresponding \( b_i \). After that, \( Z_0 \) and \( Z_1 \) are concatenated and multiplied by an additional weight matrix \( W_O \) to obtain the final self-attention matrix \( Z \).
b) Transformer-based extractor

The transformer-based optimization sequence feature extractor is completely demonstrated here. A block of the optimization sequence feature extractor is shown in Figure 5. To extract sequence features, the input optimization sequence is first transformed into vectors $a_i$ by the optimization sequence embedding in 4.1.1. These vectors are added with the corresponding position encoding to become the new vector $a_i$. After that, the vector $a_i$ is passed into the two head self-attention in section 4.1.2.a for computing the self-attention matrix $Z$. The next layer is the residual connection and layer normalization module. The residual connection is adding the self-attention matrix $Z$ with the corresponding input vector $a_i$, to prevent network degradation. The added matrix is layer normalized [17] to normalize the activation values for that layer. The output after layer normalization is linearly transformed by feed-forward layer. Finally, the input and output of the feedforward network are residual-connected and then layer-normalized to obtain the final output. In this paper, the optimization sequence feature extractor consists of three blocks stacked together. In addition, the output of the extractor does dimensional scaling through a linear layer.

\[ \text{Sequence Feature} = \text{Embedding} + \text{Positional Encoding} \]

Figure 5: Transformer-based optimization sequence feature extractor.

4.1.3 The optimization sequence feature extractor based on CNN and LSTM

As a comparison, the CNN and LSTM, which were used in [8], [9] respectively, are implemented in this paper. An example of a CNN-based optimization sequence feature extractor is shown in Figure 6. The embedding vector representation of the optimization sequence is reshaped and features are extracted using a convolution kernel. Specifically, the convolution kernel slides top-down in steps of two. With each slide, the convolution kernel is dot producted with the embedded vectors within the window of the convolution kernel, and the final sequence features consist of the results of each dotted product.

\[ \text{Feature} = \text{Convolution} \]

Figure 6: Extraction of optimization sequence features using CNN.
Detailed parameters are shown in Table 2. The example procedure using LSTM to extract features of the optimization sequence is shown in Figure 7. The optimization sequence is considered as time-series data input to the LSTM network, and each unit in the LSTM updates the cell state and output hidden state based on the existing input and the output of the previous unit. In this paper, the last hidden state of each layer is used as the embedding feature of the whole optimization sequence. Detailed parameters are shown in Table 2.

\[
F(a, b, c) = \neg(a \land b \lor b \land b)
\]

**Figure 8: AIG example of the logic** \(F(a, b, c) = \neg(a \land b \lor b \land b)\).

### 4.2 Circuit feature extractor

Since the circuit can be represented as a directed acyclic graph, the graph neural network can be used to extract information about the structural features of the circuit. Figure 8 shows an example of AIG (8-a), which has three inputs and one output. The solid and dashed lines represent the buffer and inverter, respectively, and the node in the middle is the AND logic. In Figure 8-b, the AIG is converted to a graph representation. To distinguish the attributes of different nodes, different feature vectors are added to the nodes in the graph representation. For illustration, the first iteration of the simplified propagation rule will be shown below.

\[
A = \begin{bmatrix}
0 & 0 & 0 & 1 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 1 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 1 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 1 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\end{bmatrix},
\]

\[
F = \begin{bmatrix}
0 & 0 \\
0 & 0 \\
2 & 0 \\
2 & 0 \\
2 & 0 \\
2 & 0 \\
2 & 2 \\
2 & 2 \\
\end{bmatrix},
\]

\[
\rightarrow X = A \times F = \begin{bmatrix}
2 & 0 \\
1 & 0 \\
2 & 2 \\
2 & 2 \\
2 & 2 \\
2 & 2 \\
4 & 0 \\
2 & 0 \\
\end{bmatrix}.
\]
where \( A \) is the adjacency matrix representing the graph connectivity, \( F \) is the feature matrix representing the node attributes, and the feature addition rules follow [7]. Each node is initialized with a feature vector of length 2. The first dimension of the feature matrix represents the node type, where the input, output and AND gates are denoted as 0, 1 and 2, respectively. The second dimension is the number of inverters of the node inputs. The matrix \( X \) obtained after multiplying \( A \) and \( F \) represents the node embedding after propagation, e.g., the row vector \([2,0]\) in row 0 of \( X \) stands for node 0 after propagation. The following will describe how three typical graph neural networks learn circuit features.

4.2.1 GCN-based circuit feature extractor

A graph convolutional neural network, much like a regular convolution, creates convolutions by aggregating nodes and their neighbors to form new nodes. Like any other neural network, GCNs can be stacked with multiple layers. For each layer, the aggregation of nodes, also known as convolution, can be expressed as an equation:

\[
H^{(l+1)} = \sigma \left( \tilde{D}^{-\frac{1}{2}} \tilde{A} \tilde{D}^{-\frac{1}{2}} H^{(l)} W^{(l)} \right)
\]

\( \tilde{A} \) is the adjacency matrix with the addition of a self-loop, which makes each node include its own features in the calculation. \( \tilde{D} \) is the degree matrix of \( \tilde{A} \), which is used to normalize nodes with larger degrees. \( H^{(l)} \) denotes the node embedding for the output of layer \( l \), which is also the input to the next layer. Initially, \( H^{(0)} = F \), and \( F \) is the feature matrix of the node. \( W^{(l)} \) represents the weight matrix of the \( l \)-th layer. \( \sigma \) is the activation function, e.g., ReLU.

The GCN-based circuit feature extractor used in this paper is shown in Figure 9. First is the input, where each vector representing the node type is converted to a \( 1 \times 3 \) vector by the embedding layer, and then is concatenated with a vector representing the number of inverters for each node input to become a \( 1 \times 4 \) node feature vector. Two GCN layers are also included, enabling each node to learn node embeddings from their neighbors' neighbor nodes. Each GCN layer is followed by batch normalization (BN) which helps to improve the training speed and accuracy. The activation function ReLU is used to increase the nonlinear properties of the network. Finally, the graph embedding consists of global max pooling and global mean pooling of node embeddings. The final graph embeddings will be used as extracted circuit features for downstream QoR prediction tasks.

4.2.2 GAT-based circuit feature extractor

The weights on the edges of the GCN are fixed at the time of aggregation for each convolution. GAT introduces the attention mechanism to let the model learn the weight assignment. The weight learning formula is as follows:

\[
\alpha_{ij} = \frac{\exp(\text{LeakyReLU}(\tilde{a}^T [\tilde{W} \hat{h}_i \| \tilde{W} \hat{h}_j]))}{\sum_{k \in N_i} \exp(\text{LeakyReLU}(\tilde{a}^T [\tilde{W} \hat{h}_i \| \tilde{W} \hat{h}_k]))}
\]

Figure 9: GCN-based circuit feature extractor.
where $\alpha_{ij}$ denotes the attention coefficient between the $i$-th node and the $j$-th node, $\vec{h}_i$ is the node feature, and the other $\vec{a}^T$, $\mathbf{W}$ are the learnable model parameters. The formulation first concatenates the representations of the target and source nodes and computes the correlation through the parameter network $\vec{a}^T$. After that, the correlation is passed through the activation function leakyReLU. Finally, the computed results are normalized by the softmax function to obtain the attention score $\alpha_{ij}$. Feature aggregation is performed according to the attention score with the following equation:

$$
\vec{h}'_i = \sigma \left( \sum_{j \in N_i} \alpha_{ij} \mathbf{W} \vec{h}_j \right)
$$

The aggregation process is equivalent to weighted summation. In this paper, the GAT-based circuit feature extractor is adapted from the module in Figure 9. Specifically, the GCN layer in it is replaced by the GAT layer, which means the aggregation process is changed to a weighted summation based on the attention coefficients. In addition, the activation function is changed from ReLU to elu.

4.2.3 GraphSage-based circuit feature extractor

In GraphSage, the feature aggregation process is represented as a function. The (structural and feature) information of nodes is passed from point to point. Through the aggregation function, a node can aggregate the information of its neighbors and update the information of the current node through the update function (neural network). In this paper, we use MEAN aggregate with the following equation:

$$
\vec{h}^k_v \leftarrow \sigma(\mathbf{W} \cdot \textnormal{MEAN}([\vec{h}^{k-1}_v] \cup [\vec{h}^{k-1}_u, \forall u \in N(v)]))
$$

The mean aggregator concatenates the $k-1$-th layer vectors of the target and neighbor nodes, then operates to find the mean value for each dimension of the vector, and does a nonlinear transformation of the obtained result to produce the node embedding of the $k$-th layer for the target node. In addition, as shown in Figure 10, to save computational resources, GraphSage allows sampling a certain number of neighboring nodes for each node as the nodes to be aggregated information. In the GraphSage-based circuit feature extractor in this paper, the GCN layer in Fig. 9 is replaced with GraphSage.

4.3 Joint learning policy

To predict the QoR of unseen circuit-optimization sequence pairs, optimization sequence feature extractor and circuit feature extractor are adopted as a joint policy. As shown in Figure 11, first, the optimization sequence and the AIG graph are passed into the sequence feature extractor and the circuit feature extractor, respectively.
Figure 11: Sequence feature extractor and circuit feature extractor adopted a joint learning policy for predicting the QoR of optimization sequences.

Table 1: Hyperparameters of the circuit feature extractor. In the GAT-based module, both GAT layers use two-head attention. Among them, the two-head attention of Layer1 is concatenated and the two-head attention of Layer2 is averaged.

| GNN Type | Input | Layer1 | Layer2 | Pool      | Output |
|----------|-------|--------|--------|-----------|--------|
| GCN      | 4     | 64     | 64     | Max+Mean  | 128    |
| GAT      | 4     | 32×2   | 64     | Max+Mean  | 128    |
| GraphSage| 4     | 64     | 64     | Max+Mean  | 128    |

Table 2: Hyperparameters of the optimization sequence feature extractor. The dimension of batch size is omitted.

| Transformer | Input | Num_Head | Dim_feedforward | Num_layers | Linear | Output |
|-------------|-------|----------|-----------------|------------|--------|--------|
| (20, 4)     | 2     | 32       | 3               | 50         | 50     |

| LSTM        | Input | Hidden_Size | Num_layers | Output |
|-------------|-------|--------------|------------|--------|
| (20, 3)     | 64    | 2            | 64         |

| CNN         | Input | Filters | Kernels | Stride | Output |
|-------------|-------|---------|---------|--------|--------|
| 60          | 4     | 21, 24, 27, 30 | 3     | 50     |

Table 3: Hyperparameters of the fully connected layer. The input dimensions are divided into two types, 178: Transformer/CNN + GNN, 192: LSTM + GNN.

| FC Stack    | Input | Linear1 | Linear2 | Linear3 | Linear4 | Dropout |
|-------------|-------|---------|---------|---------|---------|---------|
| 178/ 192    | 512   | 256     | 256     | 1       | 0.2     |

Then, the sequence features and circuit features output from the two extractors are concatenated together. The concatenated features are passed through three linear layers with the activation function ReLU. Finally, a linear layer outputs the predicted QoR. With such a structure, the neural network can learn features of both the optimization sequence and the circuit and link them together. This allows predictions to be passed from circuit to circuit rather than being restricted to a specific circuit. The detailed parameters of the network are presented in Tables 1, 2, and 3.
Table 4: Characteristics of the circuits in the dataset OpenABC-D [7] used in this paper. Primary Inputs (PI), Primary outputs (PO), Nodes (N), Edges (E), Inverted edges (I), Netlist Depth (D).

| Circuit     | PI | PO | N     | E     | I     | D   |
|-------------|----|----|-------|-------|-------|-----|
| spi [21]    | 254| 238| 4219  | 8676  | 5524  | 35  |
| i2c [21]    | 177| 128| 1169  | 2466  | 1188  | 15  |
| ss_pcm [21] | 104| 90 | 462   | 896   | 434   | 10  |
| usb_phy [21]| 132| 90 | 487   | 1064  | 513   | 10  |
| sasc [21]   | 135| 125| 613   | 1351  | 788   | 9   |
| wb_dma [21] | 828| 702| 4587  | 9876  | 4768  | 29  |
| simple_spi [21]| 164| 132| 930   | 1992  | 1084  | 12  |
| pci [21]    | 3429| 3157| 19547| 42251| 25719| 29 |
| wb_conmax [21]| 2122| 2075| 47840| 97755| 42138| 24 |
| ac97_ctrl [21]| 2339| 2137| 11464| 25065| 14326| 11 |
| mem_ctrl [21]| 1187| 962 | 16307| 37146| 18092| 36 |
| des3_area [21]| 303| 64 | 4971  | 10006| 4686  | 30 |
| sha256 [22]| 1943| 1042| 15816| 32674| 18459| 76 |
| aes_xcrypt [23]| 1975| 1805| 45840| 93485| 36180| 43 |
| aes_seckm [24]| 3087| 2604| 40778| 84160| 45391| 42 |
| fir [22]    | 410| 351| 4558  | 9467  | 5696  | 47 |
| tv80 [21]   | 636| 361| 11328 | 23017| 11653| 54 |
| tiny_rocket [26]| 4561| 4181| 52315| 108811| 67410| 80 |
| fpu [25]    | 632| 409| 29623 | 59655| 37142| 819 |
| dynamic node [26]| 2708| 2575| 18094| 38763| 23377| 33 |

Table 5: Experimental results of the joint model of circuit feature extractor and optimization sequence feature extractor for the QoR prediction task (the lower the better). Results are averaged over 3 runs with 3 different seeds.

| Model       | Transformer | CNN | LSTM |
|-------------|-------------|-----|------|
|             | Acc/MAE     | Epoch/Total | Acc/MAE | Epoch/Total | Acc/MAE | Epoch/Total |
| GCN         | 0.436±0.008 | 16.241      | 0.471±0.002 | 16.11hr | 0.443±0.003 | 15.83hr |
| GAT         | 0.456±0.007 | 16.270      | 0.494±0.001 | 16.14hr | 0.463±0.009 | 16.04hr |
| Graph/Sage  | **0.412±0.008** | 16.08hr | **0.444±0.005** | 16.05hr | **0.424±0.006** | 15.82hr |

5 EXPERIMENT RESULTS

The training is performed on a 2× Intel Xeon Silver 4210R, 64GB ram, and RTX 3090 Linux workstation. The loss function in training is mean square error (MSE), the adam optimizer [18] is used, the learning rate = 0.001, the Batch size is 32, and a total of 80 epochs are trained. The experiments are implemented in python 3.9 using the deep learning framework PyTorch [19] and the graph neural network framework PyTorch-geometric [20]. The data used for training and testing is taken from 22 circuits in the dataset OpenABC-D [7]. The characteristics of these 22 circuits are summarized in Table 4. Each circuit is run with K = 1500 optimization sequences, each of length L = 20, consisting of seven structural transformations of refactor, refactor -z, rewrite, rewrite -z, resub, resub -z, balance. The total size of the dataset is 33000, and the labels are the number of nodes after the circuit has been optimized.

A model that adopts a joint learning policy is trained with training data processed from a random selection of 80% of the optimization sequences for all circuits, and the model is tested for its ability to predict QoR given an unseen circuit-optimization sequence pair. This simulates the development of optimization sequences by experts for certain circuits, and
the user needs to know how these optimization sequences will perform on other circuits, but without the time-consuming actual runs. Of this, 20% of the training data is used for validation.

Table 5 shows the results of nine combinations of optimization sequence feature and circuit feature extractor after adopting a joint learning policy. The combination of transformer and GraphSage achieves the best result with a mean absolute error (MAE) of 0.412. This demonstrates the usefulness of the self-attention mechanism for capturing optimization sequence features and the positive impact of learning aggregation functions for extracting circuit features. In contrast to the usual graph task, GAT obtained the worst score. We conjecture that the act of assigning different attention scores to each neighbor node does not learn the features of AIG well, and that the importance of its neighbors is perhaps determined by the input as buffer or inverter. This phenomenon will be thoroughly investigated in future work. In further, we note that the LSTM-based sequence feature extractor achieves slightly worse results than the transformer but with a shorter training time. This is since LSTM is lighter compared to the transformer, while the currently used circuits still lack large-scale industrial data and the coverage of circuit features is not comprehensive enough. Hence, using LSTM as a sequence feature extractor is a lighter choice in small-scale usage scenarios. However, the upper limit of the transformer is high, and the potential of the transformer will be exploited in future work using more comprehensive data. Figure 12 illustrates the training curve. Partial test results are visualized in Figure 13. The performance of the model varies for different circuits.
For a circuit like `aes` (Figure 13-a), the inference results are close to the true QoR values. But for a circuit like `des3_area` (Figure 13-d), the model cannot distinguish well between the QoR values of the optimization sequence, indicating that the data distribution during training is much different from the test distribution, and the model cannot make a good generalization for this type of circuit. Hence, a comprehensive collection of circuits with different feature distributions will be a priority in future work.

6 CONCLUSION

This work proposes a joint learning policy based on GNN and Transformer, that estimates the QoR of unseen circuit-optimization sequence pairs. This allows users to quickly know the optimization results of an optimization sequence for a circuit rather than performing time-consuming actual runs, reducing the difficulty of developing high-quality optimization sequences in a short time. To enable Transformer to parse optimization sequences, embedding methods for optimization sequences are proposed so that any optimization sequence can be represented as a vector with learning capabilities. In the proposed joint learning policy, three NLP feature extractors and GNNs are used respectively. The combination of Transformer and GraphSage achieves optimal performance with an MAE of 0.412. In addition, the combination of LSTM and graph neural network provides suboptimal results and can be a lighter alternative when the data size is not too large.

Future work includes: 1. making a more comprehensive dataset of circuit features and exploiting the full potential of the transformer. 2. using GNNs that can learn edge features to fully extract the features of the circuit.

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