A broadband Doherty power amplifier design by optimizing its load modulation network

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Abstract: A kind of broadband power amplifier for wide-band coverage of the next-generation base station communications systems is obtained through using GaN HEMT transistor CGH40010 supplied by CREE as carrier or peak power amplifiers, and a novel load modulation network (LMN) is presented in this paper. With continuous wave (CW) measurements, the results for the obtained Doherty power amplifier (DPA) show that the saturation drain efficiency is between 61% and 71%, the 6 dB back off efficiency is greater than 35%, and the maximum efficiency is 52% in the 2.8–4.0 GHz frequency range. The performance of this improved DPA is more excellent than that of the unimproved one. Furthermore, 20 MHz long term evolution (LTE) modulated signals are applied for and digital pre-distortion (DPD) to evaluate its linearization performance. And lower than −46 dBc adjacent leak power ratio (ACLR) can be achieved at 3.5 GHz.

Keywords: Doherty, power amplifier, high efficiency, broadband

Classification: Microwave and millimeter-wave devices, circuits, and modules

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1 Introduction

Due to the rapid growth of wireless communication services, greater demands are being placed on the performance of wireless communication systems, especially on high speed data transmission and wide frequency coverage [1, 2]. For achieving high-speed data transmission capability, multi-carrier digital modulation technology is widely used [3, 4, 5]. However, this makes the modulation signal have a high peak-to-average power ratio (PAPR) [4, 5, 6, 7, 8, 9, 10, 11, 12, 13]. For overcoming this critical issue, the power amplifiers (PAs) should be operated at a deep power back-off (PBO) level, which would cause severe degeneration of the efficiency. So far, the classic two-way DPA has been recognized to be an effective way to achieve high efficiency at PBO level. And there are also many published researches on further improving the back-off efficiency of DPA [5, 6, 7], but the solutions described in these articles only work with narrow bandwidth, and it cannot meet the requirement in broadband application due to the bandwidth limitations caused by the DPA’s load modulation effect [8].

To improve the broadband performance of a classical DPA, a number of different DPA design strategies have been proposed to mitigate bandwidth limitations such as Simplified real-frequency technique [9], eliminating or replacing the \(\lambda/4\) impedance inverter with a Chebyshev converter [10], or releasing the effect of \(\lambda/4\) impedance inverter by reducing impedance transmission ratio of the \(\lambda/4\)
impedance inverter [11, 12] such as parallel DPA architecture [13]. However, these types of solutions would make the complexity of circuits design increase and cost a lot. Therefore, it is necessary to explore a more convenient way to improve the bandwidth.

In this article, based on $\lambda/4$ impedance inverters with reduced impedance transformation ratios, a novel load modulation network is presented, and a broadband DPA is designed. In addition, since GaN HEMT technology enables high efficiency, large breakdown voltage, high power density, and significantly higher broadband performance, here the carrier and peak power amplifiers adopt CGH40010F GaN HEMT transistors produced by CREE.

2 Broadband and highly efficient design method

The classical two-stage Doherty amplifier has limited bandwidth capability in a low-power region since it is necessary to provide an impedance transformation from 25 $\Omega$ to 100 $\Omega$ by the $\lambda/4$ impedance inverter when the peaking amplifier is turned off [8]. And this $\lambda/4$ impedance inverter is a key component of the LMN. The deviation of the operating frequency from the center frequency is proportional to the amount of phase shift, and the increase in the amount of phase shift causes the corresponding modulation impedance to deviate from the optimum impedance, resulting in poor performance of the amplifier. Therefore, it is very difficult to achieve a wide bandwidth feature on classical DPA.

From the above analysis, the $\lambda/4$ impedance inverter of the carrier power amplifier is the main reason for limiting the bandwidth. The fractional bandwidth expression [11] of the $\lambda/4$ impedance inverter is given as follows:

$$\frac{\Delta f}{f_0} = 2 - \frac{4}{\pi} \arccos \left( \frac{\Gamma_m}{\sqrt{1 - \Gamma_m^2}} \cdot \frac{2\sqrt{Z_{in}Z_{out}}}{|Z_{in} - Z_{out}|} \right).$$  \hspace{1cm} (1)

Where $Z_{in}$ is the load impedance of the carrier amplifier, and $Z_{out}$ is the output impedance after impedance transformation by the $\lambda/4$ impedance inverter of the carrier power amplifier. $\Gamma_m$ is the acceptable maximum amplitude of the $\Gamma$ ($\Gamma$ is the reflection coefficient of a wave incident on a load $Z_{out}$, from the $Z_{in}$). From the above equation i.e. Eq. (1), the smaller the ratio of $Z_{in}$ and $Z_{out}$ is, the greater the fractional bandwidth is also. Therefore, reducing the impedance transformation ratio of $Z_{in}$ to $Z_{out}$ can theoretically improve the DPA bandwidth performance. According to the previous description, the output impedance of the classical DPA is converted from 100 $\Omega$ ($Z_{in}$) to 25 $\Omega$ ($Z_{out}$) after the impedance transformation by the $\lambda/4$ impedance inverter of the carrier power amplifier. And the value of the impedance transformation ratio is 4.

Fig. 1(a) shows the parallel DPA architecture before improving the LMN. In this case, when the peaking amplifier is turned off, the required impedance of 100 $\Omega$ seen by the carrier power amplifier output is achieved by using a single $\lambda/4$ transmission line with a characteristic impedance of 70.7 $\Omega$ to match with a 50 $\Omega$ load, and the value of the impedance transformation ratio is 2. However, this structure leads to high circuit complexity and high cost. Therefore, a novel LMN is proposed in this paper, as shown in Fig. 1(b). The detailed description is as follows.
Aiming at the improvement of the parallel DPA architecture, the impedance of the \( \lambda/4 \) impedance inverter for the carrier power amplifier is set to 35.3 \( \Omega \). Thus, this can make the value of the impedance transform from 50 \( \Omega \) (\( Z_{\text{in}} \)) to 25 \( \Omega \) (\( Z_{\text{out}} \)) when the peaking amplifier is turned off (Meanwhile, the value of the impedance transformation ratio is 2). Furthermore, Fig. 2 gives the LMN of both parallel DPA and proposed DPA. And comparing the LMN of parallel DPA with that of the proposed DPA, the impedance transformation ratio of the proposed DPA structure is the same as that of the parallel DPA architecture, but the impedance transform of the proposed one is 50 \( \Omega \) to 25 \( \Omega \) (the impedance transform of the parallel DPA is 100 \( \Omega \) to 50 \( \Omega \)). while the circuit structure is more compact than the parallel DPA architecture, and the transformation ratio is half of conventional DPA. Furthermore, from the above equation i.e. Eq. (1), the conventional DPA follows that the fractional bandwidths \( \Delta f/f_0 = 17\% \) and 35\% can be achieved for maximum reflection coefficients amplitudes \( \Gamma_m = 0.10 \) and 0.20, and the proposed DPA follows that the fractional bandwidths \( \Delta f/f_0 = 36.9\% \) and 78\% can be achieved for maximum reflection coefficients amplitudes \( \Gamma_m = 0.10 \) and 0.20. Obviously, the proposed DPA has a wider fractional bandwidth.

3 Broadband DPA implementation and measurements

Fig. 3 shows a schematic of the proposed DPA. And the difference in this DPA and the classic DPA is that a novel LMN is proposed for extending the bandwidth, and match the load impedance of the carrier amplifier to the appropriate value in order
to achieve impedance matching between the carrier amplifier and LMN. Moreover, an offset line is also added before the input matching network (IMN) of the peak power amplifier to achieve phase equilibrium between the carrier and the peak power amplifier.

To verify the feasibility of the above scheme, the DPA adopts Cree’s CGH40010F GaN HEMT transistor and it was fabricated on a Rogers 4350B substrate with a plate thickness of 0.254 mm, a copper layer thickness of 0.035 mm, and a dielectric constant of 3.66. Finally, the test board of the proposed DPA with a novel load modulation structure is obtained, as shown in Fig. 4. And the experiment is implemented as the drain voltage is 28 V, and the gate bias voltages of the carrier and peak power amplifiers are −2.7 V and −5.3 V, respectively. As a result, Fig. 5 and Fig. 6 show the variation of the performance parameters with frequency for the DPA at saturation power state and 6 dB back-off power state, respectively. The detailed illustration is as follows.

As shown in Fig. 5, in an amplifier saturation mode, the drain efficiency is more than 60% with an input power of 34 dBm and an average output power is more than 43 dBm. At the same time, as shown in Fig. 6, high drain efficiency over 35% (up to 52% maximum) at 6 dB back-off output powers can potentially be achieved across the frequency range of 2.8–4.0 GHz, the fractional bandwidth is 35%. Obviously, the measured fractional bandwidth value is close to the fractional bandwidth value obtained when \( \Gamma_m = 0.10 \) in Eq. (1), so it can be inferred that
when the reflection coefficient of the circuit is kept at a low level. The measured fractional bandwidth is consistent with the calculation of the Eq. (1). Both Fig. 5 and Fig. 6 show that the simulated results are well consistent with the measured ones. Fig. 7 shows the DPA measured drain efficiency at different frequencies versus output powers, and it proves that the proposed DPA can maintain high efficiency in both saturation power and back-off power state in wide bandwidth range. Fig. 8 shows the DPA simulated drain efficiency at different frequencies versus output powers. Comparing the measured and simulated results, the measured performance of the proposed DPA decreases at both ends of the bandwidth, but the performance is better than the simulation result near the center frequency. It can be seen from Fig. 7 and Fig. 8 that the measured results basically conform to the design results.

Furthermore, the LTE signals are also excited to this broadband DPA to evaluate its modulated characteristic. 20 MHz LTE signal with 7.5 dB PAPR is applied to this broadband DPA. The measurement results are shown in the Fig. 9. From Fig. 9, adopting DPD program to this DPA, well-linearized ACLR of the output signals which is lower than −46 dBc are obtained at 3.5 GHz. In addition, Table I lists some performance parameters of the recently published DPAs. In
Table I, it is indicated that the proposed DPA has superior performance in drain efficiency (in peak-power region and back-off power region) across a wide frequency range.

Fig. 6. Measured and simulated peak powers, gains and drain efficiencies versus frequency at 6 dB back-off power.

Fig. 7. Measured Gain and drain efficiency profiles versus output power

Fig. 8. Simulated Gain and drain efficiency profiles versus output power
4 Conclusion

In this article, a broadband DPA design, which adjusts the impedance value of the $\lambda/4$ impedance inverter of the carrier power amplifier, and matches the output impedance of the carrier power amplifier to 25 $\Omega$ by the output matching network, is presented. And the measured results for the broadband DPA show that high drain efficiency over 35% (up to 52% maximum) at 6 dB back-off output powers can be achieved across the wide frequency range of 2.8–4.0 GHz, and the fractional bandwidth is 35%. Furthermore, the modulated-signal measurement indicates the good linearity of this DPA. Adopting DPD program to this DPA, well-linearized ACLR of the output signals is also obtained. It predicts the satisfaction of this DPA in wireless communication system and also demonstrates this broadband DPA design method.

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Table I. Comparison between some recently published DPAs and this paper

| Ref | Frequency (GHz) | BW (%) | DE at Psat (%) | DE at 6 dB OBO (%) | Year |
|-----|----------------|--------|----------------|--------------------|------|
| [9] | 2.2–2.9        | 27.4   | 50–73          | 40                 | 2012 |
| [13] | 1.7–2.7      | 45     | -              | 40–45              | 2012 |
| [6]  | 3.5            | -      | 64             | 52                 | 2013 |
| [10] | 2.0–2.6       | 28     | 61.5–75        | 45–64              | 2017 |
| This work | 2.8–4.0       | 35.3   | 61–71          | 35–52              | 2018 |

Fig. 9. Measured output power spectrum density with and without DPD program at 3.5 GHz.