NUMA-aware FFT-based Convolution on ARMv8 Many-core CPUs

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Abstract—Convolutional Neural Networks (CNNs), one of the most representative algorithms of deep learning, are widely used in various artificial intelligence applications. Convolution operations often take most of the computational overhead of CNNs. The FFT-based algorithm can improve the efficiency of convolution by reducing its algorithm complexity, there are a lot of works about the high-performance implementation of FFT-based convolution on many-core CPUs. However, there is no optimization for the non-uniform memory access (NUMA) characteristics in many-core CPUs. In this paper, we present a NUMA-aware FFT-based convolution implementation on ARMv8 many-core CPUs with NUMA architectures. The implementation can reduce a number of remote memory access through the data reordering of FFT transformations and the three-level parallelization of the complex matrix multiplication. The experiment results on a ARMv8 many-core CPU with NUMA architectures demonstrate that our NUMA-aware implementation has much better performance than the state-of-the-art work in most cases.

Index Terms—CNNs, Convolution, FFT, NUMA, ARMv8, Many-Core

I. INTRODUCTION

Convolutional Neural Networks (CNNs) have been widely adopted in various fields of artificial intelligence [1]–[4]. For instance, the scientific community applies CNNs into scientific analysis and discovery [1], and many works focus on analyzing medical images using CNNs [3]. However, it’s very time-consuming to train CNNs. Convolution operations often take more than 80% of the computational overhead of CNNs. Therefore, high-performance implementation of convolution operations is particularly important for improving the computational efficiency of CNNs.

The popular algorithms for implementing convolution operations are matrix multiplication-based, Winograd-based, Fast Fourier Transform (FFT)-based and direct algorithms [5]–[11]. The FFT-based algorithm converts convolutions into complex matrix multiplication by means of fast Fourier transform, and includes four stages: input transformation, kernel transformation, complex matrix multiplication, and output transformation. Compared with other three algorithms, the FFT-based convolution has lower arithmetic complexity while the accuracy loss can be ignored. Thus, there is a lot of work about studying high-performance implementation of FFT-based convolution algorithm on different platforms. Mathieu and Vasilache et al. [12], [13] first proposed how to implement convolutions by the FFT-based algorithm on modern GPUs, and introduced different FFT-based convolution implementations on GPUs. Zlateski et al. [14]–[16] mainly put their optimizing efforts into the implementations of FFT-based convolutions on Intel multi- and many-core CPUs. Lin et al. [17] presented a decomposition strategy to optimize FFT convolution on GPUs. Wang et al. [11] proposed a parallel FFT-based convolution implementation on ARMv8 CPUs, which does not depend on any other computing libraries. However, none of the work above involves the utilization of non-uniform memory access (NUMA) characteristics in modern many-core CPUs.

The state-of-the-art many-core system designs often use NUMA techniques to scale the number of cores and the memory bandwidth. Some vendors have built processors with tens of cores based on the NUMA architecture, such as AMD EPYC series [18] and Phytium FT-2000plus [19]. Further, multiple processors can be organized into a multi-socket computing node in a NUMA manner. This paper mainly focuses on the former, many-core processors with NUMA architecture. In a many-core CPU with NUMA architecture, a core can directly access the local memory of the NUMA node it belongs to, and access the remote memory attached to the other NUMA nodes through the network-on-chip. Thus, when the core and the memory are located in different NUMA nodes, the memory access latency will increase significantly. In other words, parallel implementations without considering NUMA characteristics may get very bad performance on such many-core CPUs.

In this paper, we propose a NUMA-aware FFT-based convolution algorithm named nFFT, targeted at the convolution optimization on ARMv8 many-core CPUs with NUMA architectures. The complex matrix multiplication occupies most of the total computing overhead of the FFT-based convolution algorithm. Therefore, the design philosophy of our algorithm is improving the performance of the complex matrix multiplication as much as possible without significantly increasing the overhead of the left stages. In nFFT, we design the three-level parallelization of the complex matrix multiplication,
and reorder the results of input and kernel transformations to minimize the number of remote memory access in the complex matrix multiplication. We benchmark 17 convolution configurations from three famous CNN architectures Alexnet, VGG and Resnet on a ARMv8-based Phytium FT-2000plus 64-core processor. Compared with the prior implementation [11] on ARMv8 architectures, our nFFT achieves a speedup of 1.01 - 1.84 times in most cases. In order to understand the improvement, we also make a level-2 cache miss rate comparison between nFFT and the prior.

The structure of this paper is as follows. Section II introduces FFT-based convolution algorithm and the architecture of ARMv8-based Phytium FT-2000plus processor. Section III analyzes the influences of NUMA architecture on the performance of FFT-based convolution algorithm. Section IV describes our proposed NUMA-aware FFT-based convolution algorithm and implementation on ARMv8 many-core CPUs in detail. The performance results and analysis are placed in Section V. Finally, Section VI concludes this paper and gives our future work.

II. BACKGROUND

A. FFT-based Convolution

Convolution operation involves three variables: input feature maps (I), kernels (K) and output feature maps (O). In BCHW (batch, channel, height, width) layout, these variables can be written as $I[B][C][H][W]$, $K[C'][C][H_k][W_k]$ and $O[B][C'][H_o][W_o]$, where $C'$ and $C$ are the number of output and input channels, $B$ stands for the batch size, and $H_{i/o/k}$ and $W_{i/o/k}$ represent the spatial dimension sizes. According to these data formats, convolution operation in CNNs can be obtained as:

$$O_{b,c',w_α,w_β} = \sum_{c=0}^{C-1} \sum_{h_k=0}^{H_k-1} \sum_{w_k=0}^{W_k-1} (I_{b,c,h_α,h_k,w_α+w_k} \times K_{c',c,h_k,w_k}),$$

where $0 \leq b < B$, $0 \leq c' < C'$, $0 \leq h_k < H_k$, $0 \leq w_α < W_α$, $0 \leq c < C$, $0 \leq h_k < H_k$, $0 \leq w_β < W_β$.

The FFT-based convolution algorithm consists of four stages: the FFT transformation of input feature maps and kernels, the complex matrix multiplication, and the inverse FFT (IFFT) transformation of output feature maps. The equation 2 describes these four stages above:

$$O_{b,c'} = F^{-1}(\sum_{c' \in C} F(I_{b,c}) \cdot F^*(K_{c',c})).$$

where $F$ and $F^{-1}$ are 2D FFT and IFFT respectively, $\cdot$ represents element-wise multiplication which would be converted to the classical complex matrix multiplication. As $H_k$ and $W_k$ are often much smaller than $H_{i/o}$ and $W_{i/o}$, the tiling approach is used to minimize the overhead of padding. If there is no tiling approach, the kernel needs to be expanded to the size of the input feature map, which requires lots of overhead of padding.

We label the coordinates of a tile in the tiling as $(α, β)$. So, the FFT-based convolution algorithm can be expressed as:

$$O_{b,c',α,β} = F^{-1}(\sum_{c'' \in C} F(I_{b,c',α,β}) \cdot F^*(K_{c'',c})).$$

(3)

Each element of the element-wise multiplication is labeled as $(ϕ, γ)$. There are a total of $P$ elements in the element-wise multiplication. The third stage of FFT-based convolution algorithm is actually a batched complex matrix multiplication as follows:

$$Z^{(ϕ, γ)} = G^{(ϕ, γ)} D^{(ϕ, γ)},$$

(4)

Where $D^{(ϕ, γ)} = F(I_{b,c',α,β})^{(ϕ, γ)}$ and $G^{(ϕ, γ)} = F^*(K_{c'',c})^{(ϕ, γ)}$. $Z$, $G$, and $D$ are the matrices of $P \times M \times C'$, $P \times M \times C$ and $P \times C \times C'$ sizes, where $M = B \times X \times Δ$, and $X \times Δ$ represents the number of tiles in each feature map.

The native implementation and the optimization of FFT-based convolution algorithm without considering NUMA architecture on ARMv8 many-core CPUs can refer to [11].

B. Architecture of Phytium FT-2000plus

Fig. 1 shows the architecture of Phytium FT-2000plus, which is the Phytium’s second-generation many-core architecture and code-named Mars II [20]. It consists of eight NUMA nodes, each of which directly connects a local Memory Controller (MC). All NUMA nodes are connected together by a configurable on-chip network, and each NUMA node can access a remote memory controller through the on-chip network. The memory access bandwidth evaluation [21] shows that a NUMA node can access local memory at the highest memory bandwidth while the bandwidth of accessing remote memory drops sharply. Thus, it’s necessary for the performance optimization to minimize the number of remote memory access.

Each NUMA node includes eight ARMv8-based cores [22], two Directory Control Units (DCU) and one routing cell. The working frequency of these cores is 2.3 GHz. Each core features a super-scalar out-of-order pipeline, and can issue up to four instructions per cycle. The vector units in each core can deal with 4 single precision operations at a time. Each core has a 32 KB private L1 instruction cache and a 32 KB private L1 data cache. Four cores share a 2 MB inclusive L2 cache. All the caches of eight NUMA nodes are kept coherent by 16 distributed DCUs.

III. ANALYSIS

As mentioned in the previous section, FFT-based convolution algorithm takes two tensors (I and K) as input and one tensor (O) as output, and includes four stages: the transformations of input feature maps and kernels, the complex matrix multiplication, and the inverse transformation of output feature maps. The prior optimization implementation of FFT-based convolution (named wFFT) [11] also involves three other tensors (D, G and Z), which are used to store the result of the first three stages, respectively. In order to obtain stable performance on many-core systems with NUMA architecture,
the Linux command `numactl –interleave=all` is often executed to evenly distribute the data of each tensor on all NUMA nodes.

Fig. 2 illustrates the communication between NUMA nodes in wFFT. We can find that all four stages load input tensors from all NUMA nodes and store output tensors back to all NUMA nodes. There may be a large number of remote memory accesses in each stage, drastically increasing the total overhead. In this paper, the input and output tensors (I, K and O) of convolution operations are also uniformly stored on all NUMA nodes, and it is not cost-effective to find the node where each element of these tensors is located. So the remote memory access in the fetching (1st in Fig. 2) of the first two stages and the writing (6th in Fig. 2) of the last one stage can not be eliminated or reduced. And the complex matrix multiplication often takes most of the total overhead of the FFT-based convolution algorithm. Thus, our goal is to avoid or eliminate remote memory access in the complex matrix multiplication so as to maximize its performance, while the overhead of the left three stages is not significantly increased.

IV. ALGORITHM AND IMPLEMENTATION

According to Section III, a new NUMA-aware algorithm is proposed to reduce remote memory access in FFT-based convolution, as shown in Fig. 3. Compared with wFFT, our nFFT eliminates remote memory access in the fetching (3rd in Fig. 3) of the complex matrix multiplication, by means of rearranging the distribution of the results of the first two transformations on all NUMA nodes and designing the three-level parallelization of the complex matrix multiplication. P complex matrix multiplications are evenly dispatched to all NUMA nodes.

A. Data Transformation

For the transformations of I and K, wFFT only stores half of the FFT results based on the Hermitian symmetry, and the other half are obtained by complex conjugate. For example, if the tile size is $\delta \times \delta$, only $\delta \times \delta$ real numbers is stored. In the following complex matrix multiplication, we still use vector units to deal with $L$ matrix multiplications in parallel. Thus, a transformed tile is further divided into tuples of $2 \times L$ size, and $P$ is equal to $\frac{H \times L}{P}$. There are $\frac{P}{L}$ tuples in a tile after the transformations. Our nFFT introduce a NUMA-aware tuple partitioning method shown in Fig. 3. The method stores the corresponding $\frac{P}{\delta \times \delta}$ tuples of $G$ and $D$ on the same nodes, where $N$ represents the number of NUMA nodes. The partitioning in our nFFT just stores the specified tuples on the specified NUMA nodes where the corresponding task resides, while the transformations in wFFT randomly store all tuples on all NUMA nodes. For example, the tile size is 16 x 16 and the number of NUMA nodes is 8, so the first and second four tuples are stored back to NUMA 0 and NUMA 1, respectively. Compared with wFFT, nFFT usually doesn’t incur huge additional overhead in three other stages except the complex matrix multiplication. For a specified NUMA node, the transformations of I and K also store their results in the access order of the complex matrix multiplication.

For the inverse transformation of O, all tuples in a tile are needed to be gathered together. There are two methods to deal with the operation. The one is the complex matrix multiplication stores its results on the specified node and the 5th memory access in Fig. 3 fetches the specified tuples from the specified nodes, which is the reverse process of NUMA-aware tuple partitioning. The other is the complex matrix multiplication randomly store its results on all NUMA nodes, and the 5th memory access randomly fetches all the tuples in a tile into a node. According to our experiments, even though the former can usually achieve higher performance in the complex matrix multiplication, the latter usually has better overall performance than the former. As a result, nFFT still adopts the latter method like wFFT.

B. Complex Matrix Multiplication

As shown in Fig. 3 each node performs its own matrix multiplication, and the detailed algorithm of the complex matrix multiplication is shown in Algorithm 1. There are node-
Fig. 2. NUMA communication in wFFT.

Fig. 3. NUMA communication in nFFT, NUMA-aware FFT-based Convolution.

Fig. 4. NUMA-aware Tuple Partitioning after transformations.

level, core-level and vector-level parallelizations. For the node-level parallelization (Line 6), each NUMA node carried out $P/N$ complex matrix multiplications on its own cores, which fetch the sub-tensors of the tensors $G$ and $D$ by means of the NUMA local memory access. For the core-level parallelization (Lines 10 - 12), all cores of a specified NUMA node deal with the complex matrix multiplications in parallel. The order of the loops in Lines 9 - 13 are determined by maximizing data reuse in two-level caches of Phytium FT-2000plus. For the vector-level parallelization (Line 14), vector units in a core are used to process $L$ matrix multiplications simultaneously. The detailed derivation of the block sizes ($B_r$, $C'_r$, $C'_{l1}$ and $C'_{l2}$) can refer to [11].

For the implementation, nFFT uses the function `numa_alloc_onnode()` to allocate the memory space on the specified nodes, which is for storing the tensors $G$ and $D$. The left tensors are evenly distributed on all the NUMA nodes. There are $U$ cores in a NUMA node and a total of $N$ NUMA nodes. On Phytium FT-2000plus, each core usually runs one thread for the optimal performance. Thus, a total of $N \times U$ threads are created, and divided into $N$ groups. The
The detailed configurations of these convolutional layers is shown in Table I, where A, V, and R stand for Alexnet, VGG and Resnet, respectively. Three common batch sizes are set, namely 32, 64 and 128.

We measure and analyze the performance of wFFT and NUMA-aware FFT-based convolution (nFFT) on Phytium FT-2000plus. In both wFFT and nFFT, the tile size is 16×16. All the tests are carried out 100 times, and the median execution time among all the iterations is reported as the final performance of a test.

B. Performance Comparison

The performance comparison between wFFT and our NUMA-aware FFT-based convolution is shown in Fig. 5-6. In these figures, the abscissa represents different convolutional layers, the ordinate indicates the speedup of nFFT based on wFFT, and the column bars of different colors represent different batch sizes.

Fig. 5 shows our nFFT is better than wFFT for most of the convolutional layers from VGG. The maximum speedup of 1.84 times is obtained. For some convolutional layers, such as Vconv1.2, nFFT is worse than wFFT. The main reason is that the three-level parallelization of the complex matrix multiplication in our nFFT can not get much better performance than the two-level parallelization of the complex matrix multiplication in wFFT.

Fig. 6 shows our nFFT surpasses wFFT for all the convolutional layers from Alexnet and Resnet. For Alexnet and Resnet, our nFFT can get the speedups of 1.01 - 1.62 and 1.06 - 1.50 times against wFFT, respectively.

C. Performance Analysis

To evaluate our optimizations, we further glean some events from performance monitor units (PMU) on Phytium FT-2000plus. As the PMUs don’t support NUMA-related events, we mainly collect two events: Level-2-data-cache-refill and Level-2-data-cache-access. We compare nFFT and wFFT using the Level-2 (L2) cache miss rate, which is the L2 cache miss rate averaged among all the L2 caches.

Table: The configuration parameters of all tested convolutional layers

| Conv Layers | B | C | C' | H1 × W1 | H2 × W2 |
|-------------|---|---|---|----------|----------|
| Vconv1.1    | 32/64/128 | 364 | 224 | 224 | 3 × 3 |
| Vconv1.2    | 32/64/128 | 64 | 64 | 224 | 224 | 3 × 3 |
| Vconv2.1    | 32/64/128 | 64 | 64 | 128 | 128 | 3 × 3 |
| Vconv2.2    | 32/64/128 | 128 | 128 | 112 | 112 | 3 × 3 |
| Vconv3.1    | 32/64/128 | 128 | 256 | 56 | 56 | 3 × 3 |
| Vconv3.2    | 32/64/128 | 256 | 256 | 56 | 56 | 3 × 3 |
| Vconv4.1    | 32/64/128 | 256 | 512 | 28 | 28 | 3 × 3 |
| Vconv4.2    | 32/64/128 | 512 | 512 | 28 | 28 | 3 × 3 |
| Vconv5      | 32/64/128 | 512 | 512 | 14 | 14 | 3 × 3 |
| Aconv2      | 32/64/128 | 48 | 128 | 27 | 27 | 5 × 5 |
| Aconv3      | 32/64/128 | 256 | 384 | 13 | 13 | 3 × 3 |
| Aconv4      | 32/64/128 | 192 | 192 | 13 | 13 | 3 × 3 |
| Aconv5      | 32/64/128 | 192 | 128 | 13 | 13 | 3 × 3 |
| Rconv2.2    | 32/64/128 | 64 | 64 | 56 | 56 | 3 × 3 |
| Rconv3.2    | 32/64/128 | 128 | 128 | 28 | 28 | 3 × 3 |
| Rconv4.2    | 32/64/128 | 256 | 256 | 14 | 14 | 3 × 3 |
| Rconv5.2    | 32/64/128 | 512 | 512 | 7 | 7 | 3 × 3 |

V. EXPERIMENTAL RESULTS

This section introduces the performance comparison of our nFFT against wFFT on Phytium FT-2000plus, and an in-depth analysis of the results.

A. Experimental Setup

We benchmark 17 unit stride convolutional layers from three popular CNNs: Alexnet [23], VGG [24] and Resnet [25]. The detailed configurations of these convolutional layers is shown in Table I where A, V, and R stand for Alexnet, VGG and Resnet, respectively. Three common batch sizes are set, namely 32, 64 and 128.

We measure and analyze the performance of wFFT and NUMA-aware FFT-based convolution (nFFT) on Phytium FT-2000plus. In both wFFT and nFFT, the tile size is 16×16. All the tests are carried out 100 times, and the median execution time among all the iterations is reported as the final performance of a test.

Algorithm 1: Complex Matrix Multiplication of NUMA-aware FFT-based Convolution.

```
input : G, D
output: Z
1 N is the number of NUMA nodes.
2 P = ϕ^2/(2×L), where ϕ^2 is the tile size, and L is the vector register width given a specific datatype.
3 X × Δ is the number of tiles in each feature map.
4 B_r, C'_r, C_11 and C'_12 are the block sizes in complex matrix multiplications.
5 z', g'_n and d'_n are the sub-tensors of the tensors Z, G and D, where g'_n and d'_n are located on the nth NUMA node, and z' are distributed on all the NUMA nodes.
// Node-level Parallelization
6 for δ = 0: P/N: P do in parallel
7 Get the ID (n) of a NUMA node.
8 for δ = 0: 1: P/N do
9 for cs = 0: C: C do
10 // Core-level Parallelization
11 for cs' = 0: C_2: C' do in parallel
12 for bs = 0: B: B do in parallel
13 for μ = 0: 1: X × Δ do in parallel
14 for cof's = 0: C': C'_2 do
15 // Micro-kernel:
16 Vector-level Parallelization
17 z'[B_r][C'_r][2×L] + =
18 \sum_{cs+1}^{C} \sum_{c_1}^{C_1} \sum_{c_2}^{C_2} g'_n(c', c_1, c_2)[2×L] ×
19 d'_n(c', c_1, c_2)[2×L]
store z' back to matrices Z

function pthread_setaffinity_np() is called to bind each thread in one group to all U cores of a specified NUMA node.
```
Fig. 5. Speedup of our NUMA-aware FFT-based convolution implementation (nFFT) based on wFFT on all 8 NUMA nodes of Phytium FT-2000plus, where the column bars from left to right indicate convolutional layers from VGG.

Fig. 6. Speedup of our NUMA-aware FFT-based convolution implementation (nFFT) based on wFFT on all 8 NUMA nodes of Phytium FT-2000plus, where the column bars from left to right indicate convolutional layers from Alexnet and Resnet.

For the convolutional layers of VGG in Fig. 7 our nFFT can get lower miss rate than wFFT in most cases. In Fig. 8 our nFFT is superior to wFFT on all the convolutional layers of Alexnet and Resnet. At the same time, It is worth noting that L2 cache misses may have different effects on the performance, depending on whether the misses are caused by local memory access or remote memory access.

VI. CONCLUSION

In this paper, we have presented a NUMA-aware FFT-based convolution algorithm on ARMv8 many-core CPUs with NUMA architectures. Based on the analysis of the influence of NUMA architectures on FFT convolution, the algorithm redesigns the parallelization of the complex matrix multiplication, and reorders the results of input and kernel FFT transformations. For the complex matrix multiplication, the three-level parallelization is proposed, including node-level, core-level and vector-level parallelization, and the remote memory access is reduced as much as possible without substantially increasing transformations overhead. The algorithm distributes the results of input and kernel FFT transformations on the specified NUMA nodes, based on the three-level parallel implementation of the complex matrix multiplication. Our NUMA-aware algorithm is evaluated on a ARMv8-based Phytium FT-2000plus 64-core CPU. For the convolutional layers in the popular networks, our nFFT is much better than
the prior work in most cases. And the level-2 cache miss rates of our nFFT and the prior work are directly compared.

In the future, we will focus on the optimization of Recurrent Neural Networks on ARMv8 many-core CPUs with NUMA architectures.

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