DuVisor: a User-level Hypervisor Through Delegated Virtualization

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Abstract

Today's mainstream virtualization systems comprise of two cooperative components: a kernel-resident driver that accesses virtualization hardware and a user-level helper process that provides VM management and I/O virtualization. However, this virtualization architecture has intrinsic issues in both security (a large attack surface) and performance. While there is a long thread of work trying to minimize the kernel-resident driver by offloading functions to user mode, they face a fundamental tradeoff between security and performance: more offloading may reduce the kernel attack surface, yet increase the runtime ring crossings between the helper process and the driver, and thus more performance cost.

This paper explores a new design called delegated virtualization, which completely separates the control plane (the kernel driver) from the data plane (the helper process) and thus eliminates the kernel driver from runtime intervention. The resulting user-level hypervisor, called DuVisor, can handle all VM operations without trapping into the kernel once the kernel driver has done the initialization. DuVisor retrofits existing hardware virtualization support with a new delegated virtualization extension to directly handle VM exits, configure virtualization registers, manage the stage-2 page table and virtual devices in user mode. We have implemented the hardware extension on an open-source RISC-V CPU and built a Rust-based hypervisor atop the hardware. Evaluation on FireSim shows that DuVisor outperforms KVM by up to 47.96% in a variety of real-world applications and significantly reduces the attack surface.

1 Introduction

System virtualization (or called virtualization for brevity) is a key technique to efficiently run concurrent virtual machines (VM). This technique has gone through three rough stages of evolution since its inception (Fig. 1(a)-(c)). It multiplexed scarce resources of large and expensive mainframe machines in the first stage. In the early 1970s, IBM's VM/370 hypervisor, for example, ran on System/370 hardware [46, 57]. All virtualization functions were in kernel mode due to the small code size and high reliability of hypervisors at the time [43, 84]. In the second stage, virtualization was leveraged to achieve high scalability on multiprocessors without major modifications to existing operating systems (OS) [41, 94]. Mainstream hypervisors started to offload some virtualization functions to user mode, which issue system calls to take advantage of a host OS [42] or a management VM [38]. Other functions remained in kernel mode, such as instruction emulation [79] and memory virtualization [91].

The third stage began with the release of hardware extensions (e.g., Intel VMX [20], AMD SVM [1], and ARM VE/VHE [3]), which improved VM performance by running most VM code directly, enabling stage-2 address translation, etc. Such extensions shifted more virtualization functions to hardware, further reducing the kernel involvement in virtualization. But commercial hypervisors still depends on a kernel-resident driver (e.g., KVM [48, 64]) to access the interface of hardware extensions at runtime.

The third-stage hypervisor architecture popularized for nearly two decades because it significantly reduces hypervisor complexity with acceptable virtualization overhead. However, it still has both security and performance issues. First, despite the fact that many functions have been moved out of the kernel mode, the kernel driver remains a large Trusted Computing Base (TCB), leading to a number of security vulnerabilities. For instance, KVM, whose code base consists of 57K lines of code (LoC), has accumulated a total of 127 CVEs over the course of its evolution [22]. Since the driver locates in the kernel mode, a vulnerability can be maliciously exploited to take control of the host kernel and even gain illegal access to other VMs' data [15, 19] or cause denial of service (DoS) attacks [11, 17].

Second, existing hypervisor architecture may incur nontrivial virtualization overhead. The kernel driver invokes rich functionalities (e.g., physical memory allocation) implemented by the host kernel, but these general functionalities are not well optimized for virtualization. Worse, some VM exits in the traditional hypervisor are forwarded to the user-mode management software for processing, causing excessive ring crossings and thus performance overhead [59]. To mitigate the ring crossing issue, some I/O virtualization functions are put back to kernel mode (like vhost-net [32]), but

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this design sacrifices security for performance and even leads to VM escape (e.g., V-gHost [26]).

A long line of research has tried to minimize the kernel part and deprive unnecessary functions to user mode [45, 74, 88, 95]. Yet, they face a fundamental tradeoff: a smaller kernel driver improves system security, yet offloading more functions may bring more ring crossings as they have to depend on the kernel to drive the hardware extension [95].

The root cause of this performance-security tradeoff is the unnecessarily tight coupling of hardware virtualization to kernel mode. Fortunately, we observe that recent hardware advances can expose physical resources to user mode that used to be managed only by the kernel. One prominent example of them is that Intel and RISC-V both released user-level interrupts, which allow a user-level process to handle physical interrupts [21, 29]. Another example is physical memory checking (e.g., RISC-V Physical Memory Protection or PMP [66]) that limits the physical memory range a program can access. With such recent hardware features, we believe it is time to rethink the design of hypervisor architecture. To this end, we propose delegated virtualization, which allows a user-level hypervisor (called DuVisor\(^1\)) to securely and efficiently control all virtualization functions in user mode (see Fig. 1(d)), with a tiny kernel driver only for the initialization of DuVisor and handing of fatal faults.

We design the delegated virtualization by a novel hardware extension called Delegated Virtualization Extension (DV-Ext). DV-Ext mostly reuses existing virtualization extensions with only minor modifications and securely exposes its hardware interface to user mode. With the new extension, the user-level hypervisor is able to handle runtime VM operations without trapping into the host kernel. Specifically, DuVisor directly utilizes DV-Ext’s registers and instructions in user mode to serve runtime VM exits caused by sensitive instructions, stage-2 page faults, and I/O operations. The host kernel is the control plane [39, 77], waking up occasionally only to extend physical resources for DuVisor and handle fatal faults such as DuVisor illegally accessing another VM’s memory regions (a DuVisor process supports one VM).

DuVisor efficiently provides different virtualization functions in user mode with strong security guarantees. For CPU virtualization (§ 5.1), a DuVisor process creates a dedicated thread (vthread) for each virtual CPU (vCPU), and the vthread makes use of DV-Ext to handle this vCPU’s VM exits in user space. All DuVisor threads are managed by the host kernel scheduler, which allows the host kernel to decide how to consume physical CPU resources. For memory virtualization (§ 5.2), DuVisor configures a stage-2 page table for its VM and processes stage-2 page faults in user mode via allocating physical memory in user mode. The physical memory range used by DuVisor is restricted by the host kernel and DV-Ext via hardware physical memory checking. For I/O virtualization (§ 5.3), para-virtualized (PV) backend drivers in user mode directly communicate with their frontends in VMs. DuVisor further boosts I/O performance by using user-level inter-processor interrupts (UIPI) to completely bypass the host kernel when sending notifications to its VM.

We have implemented DV-Ext based on RISC-V Rocket CPU using FPGAs. DV-Ext can be easily implemented by reusing existing hardware features, including virtualization extension (H-Ext) and user-level interrupts (N-Ext). Therefore, DV-Ext only costs 420 lines of Chisel code. Based on DV-Ext, we use Rust to build DuVisor, and the code size is about 8K LoC. We also extend the Linux kernel v5.10.26 with a kernel driver to cooperate with DuVisor by adding 362 LoC. Performance evaluation on architectural operations and real-world applications show that DuVisor outperforms KVM by up to 47.96%.

The contributions of the paper are:

- We propose delegated virtualization to break the security/performance tradeoff faced by traditional hypervisors.
- We design a user-level hypervisor that serves VMs without involving the kernel driver at runtime.
- We implement the hardware extension on RISC-V and build a Rust-based hypervisor, both of which will be

\(^1\) Short for Delegated user-level HyperVisor

Fig. 1. The architectural evolution of mainstream hypervisors: (a) Stage-1: The monolithic hypervisor puts all virtualization functions in kernel mode; (b) Stage-2: Offloading some functions to a helper process can reuse host OS/management VM that manage hardware resources; (c) Stage-3: Virtualization extensions boost some functions through hardware; (d) The DuVisor approach delegates hardware interfaces to user space and eliminates runtime intervention of the host kernel.
2 Background and Motivation

2.1 Hardware Virtualization Extension

Despite minor differences in hardware interfaces, today’s virtualization extensions [1, 3, 20, 27] provide comparable functionalities, such as selective trapping of sensitive instructions, stage-2 address translation, interrupt virtualization etc. They all demand that their interface be accessed in host kernel mode. We take RISC-V H-Ext [27] (see Fig. 1(c)) as an example to explain existing hardware extension. H-Ext has two special modes, which are orthogonal to existing privilege levels (U and K for user and kernel respectively \(^1\)). The H mode is for the hypervisor while VMs run in V mode. Only the kernel level in H mode is capable of using virtualization interface like starting/resuming a VM, installing a stage-2 page table (S2PT), and injecting virtual interrupts. So a helper process (like QEMU [25]) must invoke system calls (ioctl) to request a kernel driver (KVM) to control VMs. The hardware wakes up the driver to handle it when VM exits trigger, most of which can be served directly by the driver without switching to the helper. Take a stage-2 page fault (S2PF) as an example, the driver invokes the host kernel to allocate a physical page and inserts a new address mapping to the VM’s S2PT, which records mappings from guest physical address (GPA) to host physical address (HPA). Some VM exits, such as MMIO trapping, cannot be handled by the driver and should be forwarded to the user-level helper for emulation.

2.2 Hypervisor Architecture Issues

This section explains the tradeoff faced by today’s hypervisor architecture via QEMU/KVM \(^2\). On the one hand, the traditional hypervisor relies on the KVM driver, which has a large TCB and invokes rich kernel APIs that are not well optimized for virtualization. On the other hand, while shifting most of the driver to user space decreases its TCB, the deprivileged execution will have a higher cost owing to the more frequent kernel’s involvement in each VM exit handling [59, 88, 95].

2.2.1 Conventional Hypervisors

Huge TCB and Weak Isolation. A conventional hypervisor (or the kernel driver) has weak security and fault isolation, making it the system’s single point of failure. An adversary could exploit vulnerabilities to target not only the hypervisor, but the entire system, including the host kernel and all other cloud tenants’ VMs. Table 1 shows that even for KVM that is just a kernel driver, it has a large TCB (57K LoC on x86-64) and a number of vulnerabilities. There have been 127 disclosed vulnerabilities of KVM [22] since 2008, 62.99% of which leak information from the host OS, result in DoS on the host [11, 17, 86] or even allow a guest to escalate privilege [13, 15, 19, 26, 75, 85, 87]. Other hypervisors have the same isolation issue. There have also been 423 and 77 CVEs for Xen [34] and VMware ESXi [33] since 2007 and 2008 respectively. 76.36% and 37.66% of Xen’s CVEs and VMware ESXi’s CVEs enable the guests to attack the host kernel.

Suboptimal Internal Mechanism in Kernel. KVM is designed to call existing host kernel functions to avoid reinventing the wheel. However, their implementation can be used in general scenarios but incurs non-negligible performance impacts for virtualization. One typical example is the S2PF handling procedure. When an S2PF occurs, the CPU control flow traps from a VM into KVM, which invokes Linux to allocate physical memory before adding mappings to this VM’s S2PT. The memory allocation function comprises complex logic for versatility. For example, this function needs to use the memslot abstraction to translate a GPA to the corresponding HPA, but the memslot involves the use of RCU mechanism, lock dependency checking, reference count checking, etc. So this physical memory allocation for the fault address accounts for 2,939 cycles (57.32%) of the S2PF handling procedure in KVM (more details in § 8.2).

2.2.2 Deprivileged Execution

Deprivileging most parts of the kernel driver to user space leads to frequent communication with a long path between

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\(^1\)https://github.com/IPADS-DuVisor

\(^2\)Even though the kernel mode in RISC-V is called “supervisor” (S) mode, we still call it kernel mode.

\(^3\)Type-1 hypervisors like Xen [38] and VMware ESXi [2] use the split architecture as well: user-level processes to run VMs and the kernel-level software to drive hardware extension and resources.

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Table 1: CVE analysis of KVM [22], Xen [34] and VMware ESXi [33]. Host stands for the vulnerabilities that could lead to an attack on the host kernel. PE, DoS, and DL stand for privilege escalation, denial of service and data leakage. LoC shows their lines of code on x86-64. (VMware’s code size is unclear due to the fact that it is proprietary.) Starting Year stands for the earliest year in which the vulnerabilities were exposed.

| Hypervisor | Total | Host | Other | LoC | Starting Years |
|------------|-------|------|-------|-----|---------------|
| KVM        | 127   | 17   | 53    | 10  | 57K           | 2008 |
| Xen        | 423   | 109  | 189   | 25  | 302K          | 2007 |
| VMware     | 77    | 13   | 6     | 10  | -             | 2008 |

Table 2: Breakdown of an MMIO read in QEMU/KVM on both ARM and x86-64. Kernel represents the cycles spent on the in-kernel transfer operations. User is the cycles of the I/O emulation and the consumption of VM entry/exit.
the VM and the user-level hypervisor. Since the hypervisor has to utilize the host kernel to drive the hardware virtualization extension, more interactions between VM and the unprivileged hypervisor involve the host kernel, resulting in larger performance overhead. To understand the cost brought by the kernel involvement, we break down the handling procedure of an MMIO read operation in QEMU/KVM show the VM-VM communication cost and find out that 73.04% and 58.63% of CPU cycles account for in-kernel transfer operations on ARM and x86 respectively (Table 2). Minimizing the host kernel part by unprivileged more kernel functionalities to user space [88, 95] will experience much more overhead, because each VM exit has to be forwarded by the kernel to user space, and vice versa.

3 DuVisor Overview

In this paper, we present delegated virtualization to break the tradeoff facing the conventional hypervisor architecture. It allows all virtualization functions to be delegated to user mode so that we can build a user-level DuVisor. We have two design goals for DuVisor: First, the runtime interactions of a guest and its hypervisor should not involve the host kernel. Second, the vulnerabilities of DuVisor should be confined in user space, which does not affect other guest VMs or the host kernel. We obtain these properties via redesigning the hardware interface of the virtualization extension and taking the control plane/data plane separation idea [39, 77]. The host kernel works as the control plane and is removed from all runtime interactions (data path) between DuVisor and its VM.

The architecture, which consists of three major components, is shown in Fig. 2. First, Delegated Virtualization Extension (DV-Ext) should be installed on the hardware (§ 4). It empowers the host kernel to decide whether or not to delegate hardware virtualization functions to hypervisor user mode, so that DuVisor can directly control a VM’s behaviors and handle VM exits without trapping into the host kernel.

Second, a DuVisor process utilizes hardware instructions to manage and serve an unmodified VM without trapping into the host kernel (§ 5). Most VM exits of its corresponding VM can be handled by DuVisor directly, including S2PF. DuVisor also configures an S2PT for its VM. So it adds a new mapping entry into the S2PT if an S2PF happens due to missing a page mapping. A single VM is served by a DuVisor process. If multiple VMs are needed, separate DuVisor processes should be created for each VM. DuVisor creates multiple threads for different vCPUs (we name these threads as virtreads), like traditional hypervisors. It also provides virtual memory, PV I/O devices, virtual interrupt and timer for this VM. DuVisor can not only depend on the host kernel to manage external devices like storage media and network cards, but also control devices in user mode by DPDK [18] to boost I/O virtualization.

Lastly, a tiny control-plane (CP) driver enhances the host kernel to become the control plane for DuVisor (§ 6). The CP driver has the privilege to determine whether or not to delegate hardware virtualization functions to a process. It allocates hardware resources for DuVisor during its startup phase, creates the DuVisor process, and handles emergency cases such as a page fault triggered by an illegal stage-2 address mapping. We rely on the host kernel to schedule DuVisor and its VM. Recent advances in user-defined scheduling policies [60] can be applied to DuVisor in the future.

Assumptions and Threat Model. We assume that the hardware and DV-Ext are correctly implemented and trusted. The host kernel is trusted as well, even though it may contain vulnerabilities. We consider that the attacker can take full control of a guest VM and further compromise DuVisor by exploiting its vulnerabilities. Therefore, DuVisor is untrusted by the host kernel.

4 Delegated Virtualization Extension

Recent hardware advances reveal a trend that disentangles the management of physical resources from their protection. A user-level process can utilize physical resources freely within a predefined range configured by the OS kernel, but unauthorized use outside the range will trigger an exception
to wake up the kernel. These hardware features shed light on a new scenario where the kernel can expose hardware resources to user mode for efficiency while retaining protection.

Inspired by such hardware trend, we present a novel interface of hardware virtualization: Delegated Virtualization Extension (DV-Ext), whose registers and instructions are shown in Table 3. DV-Ext empowers the hypervisor kernel mode (HS-mode) to decide whether or not some hardware virtualization functions (their corresponding registers and instructions) can be delegated to the hypervisor user mode (HU-mode). Afterwards, HU-mode software can directly control the delegated virtualization functions and resources without relying on the host kernel. Through reusing recent hardware features with minor modifications, DV-Ext prohibits a hostile HU-mode hypervisor from maliciously manipulating delegated hardware resources.

4.1 HU-mode Registers and Instructions

One straightforward method to enable HU-mode is to allow the HU-mode to access all virtualization registers and instructions. But it may disclose unnecessary information to HU-mode, making DV-Ext difficult to implement. We observe that most registers are only configured during VM initialization and rarely touched at runtime. So these registers can be regarded as control-plane registers and will not be exposed to HU-mode. The data-plane registers, on the other hand, are the remaining registers that are frequently used at runtime. DV-Ext permits these data-plane registers to be accessed in HU-mode, which are shown in Table 3 as registers beginning with “hu”. These data-plane registers can be accessed in HU-mode only when HS-mode turns on DV-Ext by configuring h_enable. The data-plane registers are classified into two categories. The first category records the VM information for VM exits, such as hu_er and hu_einfo. The hypervisor reads these registers for handling VM exits. The second category affects the runtime behaviors of the hypervisor or VMs. For instance, a hypervisor configures hu_vitr to inject a virtual interrupt to a vCPU.

Today’s hardware can delegate physical interrupts and exceptions to user mode (e.g., RISC-V user-level interrupt extension or N-Ext). DV-Ext retains such feature to support delegatable VM exits (DVE) that can be delegated to HU-mode. DVE is configured by the host kernel by setting up the h_deleg register, whose individual bit controls the delegation of one specific type of VM exit. The host kernel in HS-mode can delegate S2PF and sensitive instruction faults (such as WFI) to HU-mode by setting the corresponding bits in h_deleg. When a DVE happens, the hardware locates a hypervisor handler whose address is specified in hu_ehb. DV-Ext also provides the HURET instruction for HU-mode to resume the VM execution, whose entry point is stored in the hu_vpc register.

4.2 Dynamic HPA Checking

DV-Ext does not expose the register holding the base address of an S2PT to HU-mode since it is rarely modified after a VM is booted. But it still allows a user-level hypervisor to freely configure S2PT address mappings in HU-mode. One natural challenge is how to prevent the hypervisor from maliciously configuring the S2PT to access arbitrary HPA. Today’s hardware usually contains a mechanism to dynamically check physical memory range according to hardware register configurations, such as ARM TrustZone and RISC-V Physical Memory Protection (PMP). DV-Ext leverages such mechanisms to restrict the physical memory range that the hypervisor and its VM can touch.

The physical memory checking (PMC) mechanism provides a set of per-core registers that specify different physical memory regions accessible to software. In our current implementation, the largest number of different regions for a physical core is 64. PMC examines the length and attributes of a physical memory access according to these registers and triggers an exception if detecting illegal physical addresses. Since the dynamic checking is implemented by comparing offset, its overhead is negligible. DV-Ext slightly extends an existing PMC mechanism to make it only work for HPA translated from guest physical addresses (GPA). Specifically, DV-Ext adds a “Virtualization” (V) bit to each range register to indicate that it is valid only for HPA from the stage-2 address translation.

4.3 Boosting Interrupt Virtualization

DV-Ext proposes a user-level notification mechanism to boost virtual interrupt injection, which is built based on existing user-level interrupt mechanism [21, 29]. An HU-mode program in one physical core can invoke HUSUIPI instruction to send a user-level inter-processor interrupt (UIPI) to another physical core. If the receiving core is running in V-mode, this UIPI causes a VM exit to the HU-mode. The sending core should write its VMID and VCPUID to two registers (h_vmid and hu_vcpuid) and specify the receiver’s VCPUID as the operand for HUSUIPI. The hardware will check the ID information when delivering a UIPI. An illegal operand will trigger a fault into the HS-mode to wake up the host kernel.

5 DuVisor Design

5.1 Handling VM Exits

Equipped with DV-Ext, a DuVisor process is able to serve a VM in HU-mode without trapping into the host kernel. Before using DV-Ext, DuVisor should invoke a system call (ioctl) to ask the CP driver to turn on DV-Ext (write h_enable) and delegate VM exits to HU-mode. After that, DuVisor can freely utilize DV-Ext registers and instructions. Fig. 3 shows an example of how DuVisor handles VM exits. DuVisor first installs a VM exit handler by writing its address into hu_ehb. Before running the first vCPU, DuVi-
DuVisor sets up the VM execution environment, including configuring an S2PT and preparing virtual I/O devices. It also initializes general-purpose registers and system registers for the vCPU.

DuVisor invokes an HURET instruction to enter V-mode and starts to run the guest’s code. When a VM exit like a sensitive instruction (WFI) or an S2PF triggers, hardware directly calls the handler specified in hu_ehb, which then handles this VM exit by reading corresponding HU-mode registers. For example, it reads hu_er to check whether this is an S2PF and gets fault address by accessing hu_einfo. After finishing processing the VM exit, DuVisor resumes the VM by invoking HURET again.

Even though the host kernel is not involved in the runtime interactions between DuVisor and the VM, it is still responsible for scheduling all processes. Therefore, physical timer interrupts are not delegated to DuVisor. These interrupts cause VM exits into the host kernel, giving it the opportunity to reclaim control of the physical cores assigned to DuVisor periodically. When a timer interrupt happens if a vCPU is running, the VM exit traps into the host kernel, which saves the current state of the vCPU before switching to another process. The kernel will restore the vCPU’s states before resuming it again.

### 5.2 Restricted Memory Virtualization

A hypervisor needs to create an S2PT for its VM, which records mappings from GPAs to HPAs. As we have analyzed in §2, the traditional kernel driver like KVM relies on the complex memory management in Linux to manage S2PTs, leading to runtime overhead. In contrast, DuVisor builds the S2PT and memory in HU-mode directly, simplifying the complexity of memory virtualization. Since an S2PT records mappings from GPA to HPA, DuVisor should see HPA in HU-mode. Hence, it asks the host kernel to pre-allocate a contiguous pinned memory region and return the base physical addresses (HVA and HPA) of this region. The memory region is pinned by the host kernel so that the region’s pages will not be swapped out during runtime. Each S2PF wakes up DuVisor to allocate a free physical page from the memory region and add this page into the VM’s GPA space by modifying the S2PT.

**Restricting Physical Memory Regions in HU-mode.** However, it is dangerous for an untrusted process to modify an S2PT because it could maliciously map another VM’s physical memory pages to a malicious VM, which then reads (or alters) sensitive data in the victim VM’s memory and passes the data to DuVisor. Worse, the rogue VM can even read and modify the host kernel memory. This threat can be mitigated by a straightforward approach, which requires DuVisor to invoke system calls to ask the host kernel to check this table before installation. Specifically, DuVisor should manage a fake S2PT instead of the really used one. The host kernel maintains a table to track page ownership and checks each page table mappings passed by DuVisor before synchronizing to the real S2PT. Although this approach sounds reasonable, it frequently involves the kernel involvement at runtime, leading to significant cost for memory-intensive workloads. Moreover, it complicates memory virtualization in the CP driver.

We take a different approach that allows DuVisor to freely modify the real S2PT in HU-mode without trapping into kernel mode. We propose to take advantage of the existing hardware PMC mechanism as we have introduced in §4.2. Equipped with PMC, we can optimistically allow DuVisor to freely configure its S2PT. The MMU automatically checks whether HPAs accessed by the VM exceed a predefined range limit of the allocated physical memory regions. If so, the MMU triggers a fault to wake up the CP driver. This design completely eliminates the stage-2 memory management module in the CP driver.

However, the existing PMC mechanism is not specially designed to restrict memory accesses from VMs. It checks all physical memory used by the current physical core. Therefore, it may even restrict the host kernel and the DuVisor process from using physical addresses exceeding the register ranges, which is a severe limitation given that the host kernel and DuVisor can possibly access all physical memory space. That is the reason why DV-Ext slightly modifies the existing PMC mechanism by adding a V bit in these registers as we have introduced in §4.2. This bit indicates whether or not this region takes effect in V-mode. The MMU only checks HPA translated from S2PT or S2PT page table pages if the bit is set.

**Put the Pieces Together.** Before configuring an S2PT, DuVisor...
The CP driver then set PMC registers to mark the start and end addresses of this region. It also enables the V bit for this region to indicate the MMU only checks physical addresses from V-mode (Please note that the S2PT pages are also guarded). The CP driver then returns the base physical address of the region and its region size. Afterwards, DuVisor builds an S2PT for its VM. When running out of physical memory, DuVisor can invoke system calls to request more memory regions from the CP driver.

Fig. 4 shows an example of how a GVA is translated into an HPA and finally used to load memory content. During runtime, if the MMU cannot find mappings or lack enough permissions for one translation request for S1PT or S2PT, it will generate a page fault to invoke the corresponding handler in the guest kernel or DuVisor. After the stage-2 translation, the output HPA will be checked by the MMU before loading memory contents. If the HPA exceeds the region limit, a page fault is triggered and wakes up the host kernel to handle this situation.

5.3 I/O and Interrupt Virtualization

DuVisor provides PV (e.g., virtio) and emulated (e.g., tty) I/O devices for its VM. During the initialization of a VM, DuVisor creates dedicated I/O thread(s) for each virtual device. These threads are typically in charge of dealing with I/O requests for the VM and interacting with host I/O devices. For example, to receive network packets from the host physical NIC and insert them into the guest VM, one RX thread is created for the RX queue of a virtio network device. The design of DuVisor can be combined with a kernel-bypass virtio approach like vhost-user to further boost I/O virtualization. Specifically, the RX thread keeps polling on the NIC in Hu-mode to process incoming network packets and notifies the guest VM via injecting virtual interrupts.

In a traditional hypervisor, if I/O threads intend to inject virtual interrupts to a vCPU, it invokes a system call to send an *eventfd* to a vCPU. Then the host kernel injects a virtual interrupt to the vCPU. To ensure that the guest VM receives and handles interrupts in a timely manner, we present an efficient user-level notification mechanism based on a UIPI technique, which requires no kernel involvement and greatly reduces network latency overhead in traditional hypervisors. In fact, the UIPI technique has already been presented by Intel [21]. We slightly extend this technique to fit the virtualization scenario.

The notification mechanism in DuVisor consists of two cases. In the first case where the target vCPU is not running, the sending thread just writes the interrupt information in the vCPU’s state area. Before the vthread resumes the vCPU execution, it will inject the virtual interrupt into the vCPU via loading the state area information into the *hu_vintr* register. The second case is that the vCPU is running. The sending thread first writes the interrupt information to the target vCPU state area and then invokes HUSUIPI to send a UIPI to the target vCPU. Since a UIPI is a physical interrupt, it will shoot down the running vCPU to cause a VM exit into DuVisor. Afterwards, the corresponding vthread injects a virtual interrupt into the vCPU and resumes its execution.

Nevertheless, a malicious process may exploit HUSUIPI to keep sending UIPIs, and the frequent VM exits could lead to a DoS attack, which seriously disturbs other VMs. So the DV-Ext forbids Hu-mode from explicitly specifying any target physical core it intends to send UIPIs to. Instead, it can only send UIPIs by specifying a VCPUID, which is written in *hu_vcpuid* by each vthread before running the corresponding vCPU. Only the receiver’s VCPUID matches the HUSUIPI’s operand and the sender and receiver share the same VMID, the hardware will inject the UIPI to the receiver’s core.

Fig. 5 depicts how DuVisor securely supports UIPI. Before DuVisor starts to run, the CP driver initializes a VMID and writes this value to *h_vmid* registers in each physical core DuVisor will run (core 0 and 1 in this figure). The vthreads also specify VCPUIDs into their corresponding *hu_vcpuid* registers. During runtime, the sending thread invokes HUSUIPI and provides the target VCPUID as the operand. The hardware will generate a physical UIPI to the target CPU and cause a VM exit when the vCPU is running. Then the VM exit handler is called, whose exit reason is UIPI. If the thread tries to send a wrong VCPUID or the sending thread does not have the same VMID as the receiver, the invocation of HUSUIPI will trigger an exception and wake up the CP driver to handle this issue.

6 Implementation

6.1 DV-Ext Implementation

We choose the RISC-V platform to implement DV-Ext since it has rich open-sourced implementations of system-on-chip (SoC). We use a 5-stage in-order scalar processor (RISC-V Rocket Core [30]), whose configuration is: 16KB L1 ICache, 16KB L1 DCache, 512KB shared L2 cache, and 16GB external DRAM.

DV-Ext does not require extensive modifications to the
CPU hardware to implement these data plane registers and instructions. These registers are just aliases of existing HS-mode registers. For example, \texttt{hu\_er} and \texttt{hu\_einfo} are aliases of \texttt{ucause} and \texttt{utval} from RISC-V N-Ext (i.e., the user-level interrupt extension) and \texttt{HURET} is implemented based on N-Ext’s \texttt{URET}. Therefore, most architectural implementation for these registers and instructions can be reused. The RISC-V N-Ext also supports the delegation of exceptions from the kernel to the user space. DV-Ext enhances this feature to support DVE so that VM exits could directly trap to HU-mode and get handled by Duvisor directly.

Our DV-Ext implementation adds 420 lines of Chisel to extend the existing H-Ext implementation [31]. Moreover, we implement a part of the N-Ext with 70 lines of Chisel, as its implementation is not yet available but is necessary to support user-level exception handling (e.g., VM exits from V-mode to HU-mode). 14 lines of Chisel are added to extend RISC-V PMP for physical memory restriction and enable UIPI for user-level notification mechanism.

6.2 Software Implementation

Our prototype system of Duvisor consists of 8K LoC (6,732 lines of Rust, 1,632 lines of C and 163 lines of assembly). In the implementation of CPU and memory virtualization, 4,706 lines of Rust are written for the main logic, such as VM exit handling and virtual interrupt emulation. Another 163 lines of C and assembly are used for accessing RISC-V CSRs (Control and Status Register) and invoking libc routines such as system calls.

To reduce the code effort, our prototype of Duvisor reuses a portion of the I/O backend implementation (i.e., virtio block and virtio network) from the kvmtool and add 68 lines of C to glue the Rust and C. We apply our design (e.g., user-level notification mechanism) to its implementation as well as make some optimizations. Since there is no available DPDK support for RISC-V platforms currently, we implement a kernel-bypass NIC driver whose code size is 623 in the network backend to achieve similar performance to OVS-DPDK.

We write a tiny Linux kernel module to work as the CP driver, which works as the control plane for Duvisor. The driver has 317 LoC. CP driver provides an \texttt{ioctl} system call for Duvisor to request services. First, the CP driver allows Duvisor to turn on DV-Ext for one process before using HU-mode and other features. Second, the driver allocates contiguous physical memory regions for Duvisor and prevents them from being swapped out. Then it configures PMP registers to restrict the HPA range that Duvisor can use during runtime. The host kernel should also have a PMP fault handler that destroys the fault process. Lastly, the CP driver initializes a VMID for Duvisor to be used by UIPI. We also modify the context switch logic (45 LoC) in the host kernel to save and store the DV-Ext registers if the process has enabled DV-Ext.

7 Security Analysis

In this section, we analyze the overall system security of Duvisor from the perspective of attackers. We also combine CVE cases to illustrate the security advantages of Duvisor.

Attack from Guest to Host Kernel. Since most VM exits directly trap to Duvisor in HU-mode, the host kernel’s attack surface is minimized. A malicious guest may exploit the vulnerabilities, such as CVE-2021-29657 [19] and V-gHost [26], to escape from a VM and compromise the traditional hypervisor and the host kernel directly. In Duvisor, such attacks could only compromise a user-level process. The attacker cannot further take over the host kernel without additional kernel vulnerabilities that are beyond the consideration of this paper. Moreover, the host kernel can apply sandboxing techniques (such as seccomp [24]) to further restrict the Duvisor process.

Attack from Guest to Guest. A malicious guest could attack the other guests on traditional hypervisors [7–9, 14]. For example, CVE-2020-29480 [14] allows the guest to leak information of the other guests via the shared hypervisor. Also, CVE-2016-3159 [9] and CVE-2016-3158 [8] allow guests to obtain sensitive register content information from other guests. The isolation provided by the new design with dedicated hypervisors is effective in preventing such guest-to-guest attacks, for there is no shared data or resources between Duvisors.

Attack from Guest to Duvisor. In the analysis above, we assumed that Duvisor could suffer from all the vulnerabilities of the traditional hypervisors, but please note that Duvisor is developed in Rust, a high-performance language with guarantees of memory-safe and thread-safe, and the ratio of unsafe code is kept below 4.7%. This greatly reduces the security risk caused by memory vulnerabilities [4, 5, 10, 13, 16] and threading vulnerabilities [6, 12, 16], such as the use-after-free vulnerabilities [10, 13] in traditional hypervisors developed in C/C++. In addition, vulnerabilities of the user-level Duvisor can be patched promptly without rebooting the host OS.

Attack from Duvisor to Host Kernel. Although this paper does not consider the original vulnerabilities of the kernel, the newly introduced CP driver cannot be ignored. A compromised Duvisor process may attack the kernel via the privileged code of the CP driver. However, compared to the complex logic and huge code base of traditional hypervisor drivers, the CP driver only has 317 LoC. Such a tiny code base with simple logic allows the CP driver to be checked more easily for security vulnerabilities.

Furthermore, the DV-Ext interface does not grant Duvisor more capabilities to compromise the host kernel. First, although the CP driver allows user-level processes to request physical memory, it can still effectively isolate them with...
the help of dynamic physical memory checking mechanisms. Second, the data-plane register and instructions are configured and restricted by the control-plane registers in the CP driver. So they only affect the VM’s behavior. Also, the host kernel saves and restores these registers on context switches to avoid affecting other processes.

8 Performance Evaluation

8.1 Experimental Setup

We run experiments on the cycle-accurate Firesim platform [62], which consists of two FPGA boards. Each FPGA board has eight RISC-V cores (3.2GHz, rv64imafdc), 16GB RAM and 115GB storage. For network related benchmarks, we build a local area network (LAN) between the two boards through 200Gbps IceNICs. Both FPGA boards are controlled by an EC2 instance that runs CentOS 7.6.1810 on 16-core Intel E5-2686 v4 CPU (2.3GHz) and 240GB RAM. The firmware for RISC-V is OpenSBI v0.8 [28]. The host kernel is Linux kernel 5.10.26 that is equipped with the CP kernel. We record the cycles between the start of the hypercall and its return position. The vCPU and the RX I/O thread are pinned to separate cores. The first vCPU sends a virtual IPI to the second vCPU and then waits for the completion response. When the second vCPU receives the virtual IPI, it notifies the first vCPU by sending a virtual IPI back. We collect the cycles between issuing the virtual IPI and receiving the completion on the first vCPU. DuVisor is 78.09% (3,914 cycles) faster than KVM. According to the breakdown, the acceleration mainly comes from the faster UIPI as in Fig. 6(d). A virtual IPI issued by the guest VM is trapped into the host kernel for emulation. If the receiver vCPU is executing on a separate physical CPU core, the hypervisor will kick it by sending a hardware IPI to that core. To send an IPI, DuVisor executes the HUS/IP instruction in HU-mode without any mode switches. Nonetheless, the host kernel (HS-mode) relies on the firmware (M-mode) to issue an IPI, which in the RISC-V KVM implementation includes an ECALL (environment call, the instruction which causes a software trap to a more privileged mode on RISC-V [29]) to the firmware. By removing mode switches, DuVisor achieves a considerable reduction in virtual IPI latency compared with KVM.

For I/O notification, we breakdown the RX process of network packets from the backend driver to the interrupt handler of the single-vCPU guest VM during the Netperf UDP latency test. The vCPU and the RX I/O thread are pinned to different pCPUs. As shown in Fig. 6(e), DuVisor is 63.16% (17,914 cycles) faster than KVM: The UIPI-based user-level notification in DuVisor boosts the virtual interrupt inserting by 78.92% (9,371 cycles) compared with KVM. Meanwhile, processing a virtual interrupt in the guest VM in DuVisor
Fig. 6. Breakdown of different hypervisor primitives (Unit: cycles). (a) shows a null hypercall. Exit: from invoking a hypercall in the guest VM to arriving at the hypercall handler in the hypervisor. Entry: the reverse procedure of Exit. Handling: processing in the hypercall handler. (b) is shows an MMIO emulation. Transfer: transfers between the kernel in HS-mode and the user-space VMM in HU-mode, which DuVisor gets rid of. Mapping: the PTE update in the 52PT. Other: other logic. (c) is a virtual IPI sending. Entry/Exit: the 1st vCPU’s VM exit and the 2nd vCPU’s VM entry. vPI Insert: the whole process of inserting a virtual interrupt to the 2nd vCPU and kicking it by sending IPI (KVM) or UIPI (DuVisor) in the hypervisor. (e) is an I/O notification during the Netperf UDP test. IRQ-Chip Emul: the emulation of the interrupt controller. U-K Switch: the users-kernel mode switch. vIRQ Insert: inserting a virtual interrupt and kicking vCPU in the hypervisor. vIRQ Handle: ACK, processing and EOI a virtual interrupt in the guest VM.

costs 53.6% (7,579 cycles) less than KVM because of the fact that accessing the virtual interrupt controller on current RISC-V platforms incurs MMIO VM exits to the user-space hypervisor.

### 8.3 Real-world Applications Performance

| Name       | Description                                                                 |
|------------|-----------------------------------------------------------------------------|
| Netserver  | Netserver v2.6.0 on the local server (guest VM) and Netserver v2.6.0 on the remote client (native) to test the UDP latency for 5 seconds. |
| iperf3     | iperf v3.9 on both the local server (guest VM) and the remote client (native) to test the TCP throughput for 10 seconds.                  |
| Memcached  | Memcached v1.6.10 running the memtier benchmark: 1,000 transactions per second on the remote client to test transactions per second. The thread number is set to the same as the number of server vCPUs. Each round of test lasts 5 seconds. |
| FileIO     | FileIO test in sysbench v0.4.12 with 4 threads concurrently and 512MB file size in random read/write mode.                              |
| Hackbench  | Hackbench using Unix domain sockets and default 10 process groups running in 100 loops, measuring the time cost.                       |
| Unitar     | Unitar extracting the benchmark v2 tarball using the standard tar utility, measuring the time cost.                                 |
| CPU-Prime  | CPU test in sysbench v0.4.12 that calculates prime numbers up to the max prime 10000. The thread number is set to the same as the number of server vCPUs. |

Table 4: Descriptions of application benchmarks.

In this section, we evaluate the performance of a variety of real-world applications, compare the results between KVM and DuVisor, and analyze the reasons for these performance differences. Table 4 lists applications we used for benchmark. We measure the performance in four types of guest VMs with 1, 2, 4, and 6 vCPUs. All VMs are equipped with 512MB memory, virtio-based network and block devices. For single-VM tests, we enable the kernel-bypass NIC driver in the network backend for both KVM and DuVisor. Each vCPU of a guest VM is pinned to a separate physical CPU core to avoid potential instability caused by the host kernel scheduler. The kernel-bypass NIC driver dedicates two CPUs for RX and TX I/O threads respectively to maximize network performance. In multi-VM tests, we still use the kernel network stack because our current implementation of the kernel-bypass NIC driver does not support network switching. If the total number of vCPU and I/O threads exceeds eight, we first ensure that vCPUs are on different physical cores, while I/O threads may co-locate with vCPUs.

As shown in Fig. 7(a), all applications in a 1-vCPU guest VM in DuVisor have better performance than KVM. Memcached, a network-intensive application, shows about 43% improvement. According to our microbenchmark, the major reason for this improvement is that the network I/O notification in DuVisor costs merely one-third the price of KVM. We further gather the time cost of VM exits during the Memcached benchmark: VM exits caused by MMIO are of the highest percentage in both KVM (58.64%) and DuVisor (66.34%). The time cost of DuVisor’s MMIO handling time cost is merely 35.87% of KVM, resulting in the large performance improvement. But we believe that the DuVisor architecture will not deliver such huge performance gains on platforms that provide hardware interrupt virtualization (e.g., ARM vGIC) to reduce excessive MMIO VM exits. Other I/O-intensive applications have less than 10% improvements: FileIO and iperf3 benchmarks aim to saturate the I/O bandwidth, and the virtio optimizes such scenario by reducing the frequency of I/O notifications. Therefore, the less I/O notification is the reason why their performance improvements are smaller than Memcached. Netperf evaluates the network latency in a ping-pong method between the client and the server. Though DuVisor’s I/O notification is much faster, the time cost of network stacks in both client and server dominates the whole procedure (network stacks cost 50 µs out of the total 60 µs), lowering the performance improvement.

Fig. 7(b) shows the performance of a 2-vCPU guest VM, DuVisor achieves up to 35% improvement over KVM in the Memcached benchmark. In addition to DuVisor’s faster I/O notifications, the more efficient virtual IPI delivery in DuVisor is another factor of the improvement. In a multithreaded application, one thread needs to perform operations such as event notifications and message passing to communicate
with other threads. When two threads that require communications are running on different vCPUs, one must send a virtual IPI in the guest VM to notify the other side.

Fig. 7(c) and (d) shows the performance of 4-vCPU and 6-vCPU guest VMs, similar to the 2-vCPU case, DuVisor outperforms KVM by up to 48% and 36%.

**Performance Impact on KVM VMs:** To investigate the performance impact of DuVisor’s host kernel modifications and DV-Ext on KVM VMs, we evaluate the performance of all real-world applications in KVM VMs after porting the modifications to the host kernel and running it on the DV-Ext enabled hardware. The results in Fig. 8(a), (b), (c) and (d) show that there is no discernible performance degradation when compared with unmodified KVM VMs, demonstrating that the impact of supporting DV-Ext in the host kernel is negligible.

### 8.4 Scalability

**Scaling vCPU number:** To show DuVisor’s vCPU scalability compared with KVM, we choose Memcached as the benchmark because its multi-threading model is able to benefit from multiple vCPUs. We test Memcached in a guest VM with 512MB memory and increase its vCPU number from 1 to 2, 4 and 6. The result is shown in Fig. 9(a). DuVisor keeps outperforming KVM in all cases from 34.65% to 47.96% and thus scales well as the number of vCPUs grows.

**Scaling Memory:** To show DuVisor’s memory scalability compared with KVM, we run STREAM [71], a memory-intensive benchmark, in a 4-vCPU guest VM with 512MB, 1024MB, 1536MB and 2048MB memory. As shown in Fig. 9(b), DuVisor achieves slightly better performance than KVM in all cases. Compared with the memory virtualization in KVM, DuVisor enables the HU-mode to configure the S2PT via extending the PMP checking with minor modifications, so that there is little impact on the memory access latency and thus scales well as the memory size grows.

**Scaling VM number:** To reflect the scalability of DuVisor in the situation of multiple VMs, we evaluate the performance of different numbers of guest VMs in DuVisor and KVM. We test CPU-Prime as a CPU-intensive workload in 1, 2, 4 and 8 VMs concurrently. As shown in Fig. 9(c), DuVisor has good scalability and performs as well as KVM.

### 8.5 PMP Checking

DuVisor slightly extends the PMP hardware with a V bit to verify the validity of memory accesses from guest VMs. We set up a guest VM with 4-vCPU and 1024MB memory to evaluate and compare performance with and without PMP V bit hardware to see if this checking mechanism imposes additional memory access overhead on VMs. We utilize Memcached as the memory-intensive benchmark and allocate 900MB of memory to it. The results reveal that the performance of the VM with and without PMP checking has little difference. As a result, the physical memory restriction imposed by DuVisor has invisible effect on VM performance.

| Improvement | 10% | 20% | 30% | 40% | 50% |
|-------------|-----|-----|-----|-----|-----|
| Performance | 0%  | 42.87% | 47.96% | 51.12% | 55.28% |

| Overhead | 0% | 0.25% | 0.5% | 0.75% | 1% |
|----------|----|-------|------|-------|----|
| Performance | 0%  | 0%  | 0%  | 0%  | 0%  |

**Fig. 7.** Normalized performance of real-world applications of DuVisor compared with KVM. The Y-axis indicates the performance improvement of DuVisor over KVM.

**Fig. 8.** Normalized performance of real-world applications of KVM with context switch logic of DV-Ext compared with vanilla KVM. The Y-axis presents the overhead brought by the context switch logic of DV-Ext.

**Fig. 9.** The evaluation of DuVisor’s scalability using Memcached compared with KVM. (a) and (b) show DuVisor’s normalized improvement of a different numbers of vCPUs and sizes of memory respectively.

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**Table:**

| Improvement | 10% | 20% | 30% | 40% | 50% |
|-------------|-----|-----|-----|-----|-----|
| Performance | 0%  | 4.287% | 47.96% | 51.12% | 55.28% |

| Overhead | 0% | 0.25% | 0.5% | 0.75% | 1% |
|----------|----|-------|------|-------|----|
| Performance | 0%  | 0%  | 0%  | 0%  | 0%  |
9 Discussion

Virtual Machine Management. All VM states are completely managed by DuVisor, so that it can support normal VM management operations. First, cloud operators can suspend the VM at any time to make a VM checkpoint and restore it from this image afterwards. Second, different intrusion detection systems (IDS) [52, 80] and virtual machine introspection (VMI) [55] tools can be implemented in DuVisor to monitor VM behaviors. Moreover, DuVisor can support different live VM migration strategies [44, 81] since it is able to suspend a VM and keep copying its dirty pages to a remote instance.

Rapid Development and Deployment. Delegated virtualization enables developers to leverage rich development resources and debugging tools in user space to quickly react to various security vulnerabilities, rapidly evolving hardware features and application requirements. Besides, a user-level hypervisor accelerates the hypervisor upgrade cycle since developers can replace the old hypervisor without rebooting the host kernel.

Nested Virtualization. The existing nested virtualization [40, 96] mandates that all VMs exits have to be intercepted by L0 hypervisor (bare-metal one) before being handled by L1 hypervisor (nested one), which incurs tremendous runtime overhead. More levels of nested virtualization further increase the overhead exponentially. In the future, we plan to extend the idea of delegated VM exits (DVE) to optimize nested virtualization, which allows the VM exits to trap directly to the L1 hypervisor that has the information to handle them without involving the L0 one.

10 Related Work

This section compares DuVisor with closely related work, including approaches that protects VMs, reduces virtualization overhead, deprivileges kernel features to userspace, and design new hardware for systems.

10.1 Securing VMs

Many studies have considered how to achieve better isolation for VMs with unreliable hypervisors to mitigate security threats. One solution is to propose hardware extensions to remove the vulnerable hypervisor out of TCB [37, 61, 63, 89]. In particular, NoHype [63] proposes to completely remove the hypervisor to reduce the attack surface and avoid VM exits. It dedicates physical cores, memory, I/O devices by implementing these virtualization functions in hardware chips, which disallows resource oversubscription and is thus inviable for practical deployment. Different from these work, DuVisor puts virtualization functions to user mode to minimize the runtime attack surface of a hypervisor. Even if a malicious VM takes over its own hypervisor, it cannot make direct attacks on other VMs, including DoS attacks.

Existing studies also have explored how to defend VMs via software methods [?, 45, 67, 86, 88, 92, 93, 93]. NOVA [88] builds a microhypervisor based on the microkernel architecture. For KVM that is widely deployed in commercial scenarios, DeHype [95] tries to move most parts of KVM into user mode. However, it still needs a HypLet in kernel mode since the sensitive instructions of virtualization can only be used in this mode. Such design incurs a large number of system calls and thus runs slower than KVM, which has already brought non-trivial performance overhead due to excessive ring crossings. For Xen [38] hypervisor, Nexen [86] deconstructs it into different instances of non-privileged service slices. HypSec [67] decouples the hypervisor into a small corevisor and untrusted hypervisor via exploiting ARM TrustZone and virtualization extension. All these software approaches leverage the traditional interface of hardware virtualization, DuVisor proposes a novel hardware interface and downgrades the whole hypervisor to user space while also reducing world switches.

10.2 Reducing Virtualization Overhead

One major cause of virtualization overhead is costly world switches [59, 72, 97]. To this end, existing approaches try to reduce the number of world switches [35, 36, 50]. To boost the interrupt virtualization, ELI [56] passes interrupts directly to guest VMs without the involvement of the hypervisor. CloudVisor-D [72] leverages an Intel instruction (VMF-MFUNC) to allow a VM to directly interact with the hypervisor without trapping into the privileged mode, which effectively reduces the number of world switches. But it can only support nested virtualization and needs to modify the guest OS to proactively invoke the VMFUNC instruction. BM-Hive [97] offers a physically isolated machine to run a VM via bare-metal virtualization, totally avoiding the virtualization overhead. In contrast, DuVisor reduces the virtualization overhead by hardware-software co-design and removing the kernel host from the path of VM exit handling.

Memory translation is another source of virtualization overhead since it may lead to at most 24 memory accesses for walking two page tables [54]. Solutions have been proposed either to increase the number of TLB entries [76, 82] or use huge pages to increase the TLB hit rate [78]. All these optimization techniques can be applied to DuVisor to further improve the virtualization performance.

10.3 Moving Kernel Functions to Userspace

Deprivilieng kernel features to user space is a classic approach to ease kernel development or improve system reliability. Microkernels are one typical design [53, 65, 68], where system services such as file systems and drivers run in user mode. Therefore, costly inter-process communication (IPC) is frequently used to connect these services [65]. For monolithic kernels, similar methods also exist, which implement the file systems [49, 73], scheduler [60], network service [70]...
This paper presents delegated virtualization via retrofitting existing hardware with a new delegated virtualization extension. We build a user-level hypervisor atop the hardware extension, called DuVisor, that directly handles all VM operations without trapping into the kernel at runtime. Experimental results show that DuVisor outperforms traditional hypervisors.

11 Conclusion

This paper presents delegated virtualization via retrofitting existing hardware with a new delegated virtualization extension. We build a user-level hypervisor atop the hardware extension, called DuVisor, that directly handles all VM operations without trapping into the kernel at runtime. Experimental results show that DuVisor outperforms traditional hypervisors.

References

[1] AMD64 architecture programmer’s manual, volume 2: System programming. https://www.amd.com/system/files/TechDocs/24593.pdf. Referenced December 2021.
[2] The architecture of VMware ESXi. https://www.vmware.com/content/dam/digitalmarketing/vmware/en/pdf/techpaper/ESXi_architecture.pdf. Referenced December 2021.
[3] ARM architecture reference manual armv8, for armv8-a architecture profile. https://developer.arm.com/documentation/102105/latest. Referenced December 2021.
[4] CVE-2013-1796. https://cve.mitre.org/cgi-bin/cvename.cgi?name=CVE-2013-1796. Referenced December 2021.
[5] CVE-2014-0049. https://cve.mitre.org/cgi-bin/cvename.cgi?name=CVE-2014-0049. Referenced December 2021.
[6] CVE-2014-7842. https://cve.mitre.org/cgi-bin/cvename.cgi?name=CVE-2014-7842. Referenced December 2021.
[7] CVE-2015-8555. https://cve.mitre.org/cgi-bin/cvename.cgi?name=CVE-2015-8555. Referenced December 2021.
[8] CVE-2016-3158. https://cve.mitre.org/cgi-bin/cvename.cgi?name=CVE-2016-3158. Referenced December 2021.
[9] CVE-2016-3159. https://cve.mitre.org/cgi-bin/cvename.cgi?name=CVE-2016-3159. Referenced December 2021.
[10] CVE-2018-16882. https://cve.mitre.org/cgi-bin/cvename.cgi?name=CVE-2018-16882. Referenced December 2021.
[11] CVE-2019-19332. https://cve.mitre.org/cgi-bin/cvename.cgi?name=CVE-2019-19332. Referenced December 2021.
[12] CVE-2019-6974. https://cve.mitre.org/cgi-bin/cvename.cgi?name=CVE-2019-6974. Referenced December 2021.
[13] CVE-2019-7221. https://bugs.chromium.org/p/project-zero/issues/detail?id=1760. Referenced December 2021.
[14] CVE-2020-29480. https://cve.mitre.org/cgi-bin/cvename.cgi?name=CVE-2020-29480. Referenced December 2021.
[15] CVE-2021-22543. https://cve.mitre.org/cgi-bin/cvename.cgi?name=CVE-2021-22543. Referenced December 2021.
[16] CVE-2021-29657. https://cve.mitre.org/cgi-bin/cvename.cgi?name=CVE-2021-29657. Referenced December 2021.
[17] CVE-2021-43056. https://cve.mitre.org/cgi-bin/cvename.cgi?name=CVE-2021-43056. Referenced December 2021.
[18] DPDK. https://www.dpdk.org/. Referenced December 2021.
[19] An EPYC escape: Case-study of a KVM breakout. https://googleprojectzero.blogspot.com/2021/06/an-epyc-escape-case-study-of-kvm.html. Referenced December 2021.
[20] Intel® 64 and ia-32 architectures software developer’s manual. https://www.intel.com/content/dam/www/public/us/en/documents/manuals/64-ia-32-architectures-software-developer-vol-3c-part-3-manual.pdf. Referenced December 2021.
[21] Intel® architecture instruction set extensions programming reference. https://software.intel.com/content/www/us/en/develop/download/intel-architecture-instruction-set-extensions-programming-reference.html. Referenced December 2021.
[22] KVM CVE. https://cve.mitre.org/cgi-bin/cvekey.cgi?keyword=KVM. Referenced December 2021.
[23] KVM RISC-V. https://github.com/KVM-riscv. Referenced December 2021.
[24] Linux seccomp. https://en.wikipedia.org/wiki/Seccomp. Referenced December 2021.
[25] QEMU: A generic and open source machine emulator and virtualizer. https://www.qemu.org/. Referenced December 2021.
[26] QEMU-KVM guest to host kernel escape vulnerability: vhost/vhost_net kernel buffer overflow. https://bugs.gentoo.org/show_bug.cgi?id=CVE-2019-14835. Referenced December 2021.

[27] RISC-V Hypervisor Extension, version 1.0.0-rc. https://github.com/riscv/riscv-isa-manual/blob/master/src/hypervisor.txt. Referenced December 2021.

[28] RISC-V OpenSBI, version 0.8. https://github.com/riscv-software-src/opensbi/releases/tag/v0.8. Referenced December 2021.

[29] RISC-V Privileged Architectures, version 1.12. https://github.com/riscv/riscv-isa-manual/releases/download/Priv-v1.12/riscv-privileged-20211203.pdf. Referenced December 2021.

[30] Rocket Chip. https://github.com/chipsalliance/rocket-chip. Referenced December 2021.

[31] Rocket Chip H-Ext PR. https://github.com/chipsalliance/rocket-chip/pull/2841. Referenced December 2021.

[32] vhost-net: a kernel-level virtio server. https://lwn.net/Articles/346267/. Referenced December 2021.

[33] VMware CVE. https://cve.mitre.org/cgi-bin/cvekey.cgi?keyword=VMware+ESXi. Referenced December 2021.

[34] Xen CVE. https://cve.mitre.org/cgi-bin/cvekey.cgi?keyword=Xen. Referenced December 2021.

[35] Ole Agesen, Jim Mattson, Radu Ruginiga, and Jeffrey Sheldon. Software techniques for avoiding hardware virtualization exits. In Gernot Heiser and Wilson C. Hsieh, editors, 2012 USENIX Annual Technical Conference, Boston, MA, USA, June 13-15, 2012, pages 373–385. USENIX Association, 2012.

[36] Irfan Ahmad, Ajay Gulati, and Ali José Mashtizadeh. vic: Interrupt coalescing for virtual machine storage device IO. In Jason Nieh and Carl A. Waldspurger, editors, 2011 USENIX Annual Technical Conference, Portland, OR, USA, June 15-17, 2011. USENIX Association, 2011.

[37] Ahmed M. Azab, Peng Ning, Zhi Wang, Xuxian Jiang, Xiaolan Zhang, and Nathan C. Skalsky. Hypersentry: Enabling stealthy in-context measurement of hypervisor integrity. In Proceedings of the 17th ACM Conference on Computer and Communications Security, CCS ’10, page 38–49. New York, NY, USA, 2010. Association for Computing Machinery.

[38] Paul Barham, Boris Dragovic, Keir Fraser, Steven Hand, Tim Harris, Alex Ho, Rolf Neugebauer, Ian Pratt, and Andrew Warfield. Xen and the art of virtualization. In Proceedings of the Nineteenth ACM Symposium on Operating Systems Principles, SOSP ’03, pages 164–177. New York, NY, USA, 2003. Association for Computing Machinery.

[39] Adam Belay, George Prekas, Ana Klimovic, Samuel Grossman, Christos Kozyrakis, and Edouard Bugnion. IX: A protected dataplane operating system for high throughput and low latency. In 11th USENIX Symposium on Operating Systems Design and Implementation (OSDI 14), pages 49–65. Broomfield, CO, October 2014. USENIX Association.

[40] Muli Ben-Yehuda, Michael D. Day, Zvi Dubitzky, Michael Factor, Nadav Har’El, Abel Gordon, Anthony Ligouri, Orit Wasserman, and Ben-Ami Yassour. The turtles project: Design and implementation of nested virtualization. In Proceedings of the 9th USENIX Conference on Operating Systems Design and Implementation, OSDI ’10, page 423–436, USA, 2010. USENIX Association.

[41] Edouard Bugnion, Scott Devine, and Mendel Rosenblum. Disco: Running commodity operating systems on scalable multiprocessors. SIGOPS Oper. Syst. Rev., 31(5):143–156, oct 1997.

[42] Edouard Bugnion, Scott Devine, Mendel Rosenblum, Jeremy Sugerman, and Edward Y. Wang. Bringing virtualization to the x86 architecture with the original vmware workstation. ACM Trans. Comput. Syst., 30(4), nov 2012.

[43] J. P. Buzen and U. O. Gagliardi. The evolution of virtual machine architecture. In Proceedings of the June 4–8, 1973, National Computer Conference and Exposition, AFIPS ’73, page 291–299, New York, NY, USA, 1973. Association for Computing Machinery.

[44] Christopher Clark, Keir Fraser, Steven Hand, Jacob Gorm Hansen, Eric Jul, Christian Limpach, Ian Pratt, and Andrew Warfield. Live migration of virtual machines. In Proceedings of the 2nd Conference on Symposium on Networked Systems Design & Implementation - Volume 2, NSDI’05, pages 273–286, USA, 2005. USENIX Association.

[45] Patrick Colp, Mihir Nanavati, Jun Zhu, William Aiello, George Coker, Tim Deegan, Peter Loscocco, and Andrew Warfield. Breaking up is hard to do: Security and functionality in a commodity hypervisor. In Proceedings of the Twenty-Third ACM Symposium on Operating Systems Principles, SOSP ’11, page 189–202, New York, NY, USA, 2011. Association for Computing Machinery.

[46] R. J. Creasy. The origin of the vm/370 time-sharing system. IBM Journal of Research and Development, 25(5):483–490, 1981.

[47] Christoffer Dall, Shih-Wei Li, Jin Tack Lim, Jason Nieh, and Georgios Koloventzos. Arm virtualization: Performance and architectural implications. In Proceedings of the 43rd International Symposium on Computer Architecture, ISCA ’16, pages 304–316. IEEE Press, 2016.

[48] Christoffer Dall and Jason Nieh. KVM/arm: The design and implementation of the linear arm hypervisor. In Proceedings of the 19th International Conference on Architectural Support for Programming Languages and Operating Systems, ASPLOS ’14, page 333–348. New York, NY, USA, 2014. Association for Computing Machinery.

[49] Mingkai Dong, Heng Bu, Jifei Yi, Benchoa Dong, and Haibo Chen. Performance and protection in the zofs user-space nvm file system. In Proceedings of the 27th ACM Symposium on Operating Systems Principles, SOSP ’19, page 478–493. New York, NY, USA, 2019. Association for Computing Machinery.

[50] Yaozu Dong, Dongxiao Xu, Yang Zhang, and Guangdeng Liao. Optimizing network I/O virtualization with efficient interrupt coalescing and virtual receive side scaling. In 2011
IEEE International Conference on Cluster Computing (CLUSTER), Austin, TX, USA, September 26–30, 2011, pages 26–34. IEEE Computer Society, 2011.

[51] Dong Du, Zhichao Hua, Yubin Xia, Binyu Zang, and Haibo Chen. Xpc: Architectural support for secure and efficient cross process call. In Proceedings of the 46th International Symposium on Computer Architecture, ISCA ’19, page 671–684, New York, NY, USA, 2019. Association for Computing Machinery.

[52] George W. Dunlap, Samuel T. King, Sukru Cinar, Murtaza A. Basrai, and Peter M. Chen. Revert: Enabling intrusion analysis through virtual-machine logging and replay. SIGOPS Oper. Syst. Rev., 36(SI):211–224, dec 2003.

[53] Vinod Ganapathy, Matthew J. Renzelmann, Arini Balakrishnan, Michael M. Swift, and Somesh Jha. The design and implementation of microdrivers. In Proceedings of the 13th International Conference on Architectural Support for Programming Languages and Operating Systems, ASPLOS XIII, page 168–178, New York, NY, USA, 2008. Association for Computing Machinery.

[54] Jayneel Gandhi, Mark D. Hill, and Michael M. Swift. Agile paging: Exceeding the best of nested and shadow paging. In Proceedings of the 43rd International Symposium on Computer Architecture, ISCA ’16, page 707–718. IEEE Press, 2016.

[55] Tal Garfinkel and Mendel Rosenblum. A virtual machine introspection based architecture for intrusion detection. In Proceedings of the Network and Distributed System Security Symposium, NDSS 2003, San Diego, California, USA. The Internet Society, 2003.

[56] Abel Gordon, Nadav Amit, Nadav Har’El, Muli Ben-Yehuda, Alex Landau, Assaf Schuster, and Dan Tsafrir. Eli: Bare-metal performance for i/o virtualization. In Proceedings of the Seventeenth International Conference on Architectural Support for Programming Languages and Operating Systems, ASPLOS XVII, page 411–422, New York, NY, USA, 2012. Association for Computing Machinery.

[57] P. H. Gum. System/370 extended architecture: Facilities for virtual machines. IBM Journal of Research and Development, 27(6):530–544, 1983.

[58] Gernot Heiser and Ben Leslie. The OKLA microvisor: Convergence point of microkernels and hypervisors. In Proceedings of the First ACM Asia-Pacific Workshop on Workshop on Systems, APSys ’10, page 19–24, New York, NY, USA, 2010. Association for Computing Machinery.

[59] Jack Tigar Humphries, Kostis Kaffes, David Mazières, and Christos Kozyrakis. A case against (most) context switches. In Proceedings of the Workshop on Hot Topics in Operating Systems, HotOS ’21, page 17–25, New York, NY, USA, 2021. Association for Computing Machinery.

[60] Jack Tigar Humphries, Neel Natu, Ashwin Chaugule, Ofrir Weisse, Barret Rhoden, Josh Don, Luigi Rizzo, Oleg Rombak, Paul Turner, and Christos Kozyrakis. GhOSt: Fast & Flexible User-Space Delegation of Linux Scheduling, page 588–604. Association for Computing Machinery, New York, NY, USA, 2021.

[61] Seongwook Jin, Jeongseob Ahn, Sanghoon Cha, and Jaehyuk Huh. Architectural support for secure virtualization under a vulnerable hypervisor. In Proceedings of the 44th Annual IEEE/ACM International Symposium on Microarchitecture, MICRO-44, page 272–283, New York, NY, USA, 2011. Association for Computing Machinery.

[62] Sagar Karandikar, Howard Mao, Donggyu Kim, David Bincolin, Alon Amit, Dayeol Lee, Nathan Pemberton, Emmanuel Amaro, Colin Schmidt, Aditya Chopra, Qijing Huang, Kyle Kovacs, Borivoje Nikolic, Randy Katz, Jonathan Bachrach, and Krste Asanović. Firesim: Fpga-accelerated cycle-exact scale-out system simulation in the public cloud. In Proceedings of the 45th Annual International Symposium on Computer Architecture, ISCA ’18, page 29–42. IEEE Press, 2018.

[63] Eric Keller, Jakub Szefer, Jennifer Rexford, and Ruby B. Lee. Nohype: Virtualized cloud infrastructure without the virtualization. In Proceedings of the 37th Annual International Symposium on Computer Architecture, ISCA ’10, page 350–361, New York, NY, USA, 2010. Association for Computing Machinery.

[64] Avi Kivity, Yaniv Kamay, Dor Laor, Uri Lublin, and Anthony Liguori. KVM: the linux virtual machine monitor. In Proceedings of the Linux symposium, volume 1, pages 225–230. Dttawa, Dntorio, Canada, 2007.

[65] Gerwin Klein, Kevin Elphinstone, Gernot Heiser, June Andronick, David Codd, Philip Derrin, Dhammika Elkaduwu, Kai Engelhardt, Rafal Kolanski, Michael Norrish, Thomas Sewell, Harvey Tuch, and Simon Winwood. Sel4: Formal verification of an os kernel. In Proceedings of the ACM SIGOPS 22nd Symposium on Operating Systems Principles, SOSP ’09, page 207–220, New York, NY, USA, 2009. Association for Computing Machinery.

[66] Dayeol Lee, David Kohlbrenner, Shweta Shinde, Krste Asanović, and Dawn Song. Keystone: An open framework for architecting trusted execution environments. In Proceedings of the Fifteenth European Conference on Computer Systems, EuroSys ’20, New York, NY, USA, 2020. Association for Computing Machinery.

[67] Shih-Wei Li, John S. Koh, and Jason Nieh. Protecting cloud virtual machines from hypervisor and host operating system exploits. In Nadia Heninger and Patrick Traynor, editors, 28th USENIX Security Symposium, USENIX Security 2019, Santa Clara, CA, USA, August 14-16, 2019, pages 1357–1374. USENIX Association, 2019.

[68] J. Liedtke. On micro-kernel construction. SIGOPS Oper. Syst. Rev., 29(5):237–250, dec 1995.

[69] Jin Tack Lim, Christoffer Dall, Shih-Wei Li, Jason Nieh, and Marc Zynigier. Neve: Nested virtualization extensions for arm. In Proceedings of the 26th Symposium on Operating Systems Principles, SOSP ’17, page 201–217, New York, NY, USA, 2017. Association for Computing Machinery.

[70] Michael Marty, Marc de Kruijff, Jacob Adriaens, Christopher Alfeld, Sean Bauer, Carlo Contavalli, Michael Dalton, Nandita Dukkipati, William C. Evans, Steve Gribble, Nicholas Kidd, Roman Kononov, Gautam Kumar, Carl Mauer, Emily Musick, Lena Olson, Erik Rubow, Michael Ryan, Kevin Springborn,
Paul Turner, Valas Valancius, Xi Wang, and Amin Vahdat. Snap: A microkernel approach to host networking. In Proceedings of the 27th ACM Symposium on Operating Systems Principles, SOSP ’19, page 399–413, New York, NY, USA, 2019. Association for Computing Machinery.

[71] John McCalpin. Stream: Sustainable memory bandwidth in high performance computers. http://www.cs.virginia.edu/stream/, 2006.

[72] Zeyu Mi, Dini Li, Haibo Chen, Binyu Zang, and Haibing Guan. (Mostly) exitless VM protection from untrusted hypervisor through disaggregated nested virtualization. In Srdjan Capkun and Franziska Roesner, editors, 29th USENIX Security Symposium, USENIX Security 2020, August 12-14, 2020, pages 1695–1712. USENIX Association, 2020.

[73] Samantha Miller, Kaiyuan Zhang, Mengqi Chen, Ryan Jennings, Ang Chen, Danyang Zhuo, and Thomas E. Anderson. High velocity kernel file systems with bento. In Marcos K. Aguilera and Gala Yadgar, editors, 19th USENIX Conference on File and Storage Technologies, FAST 2021, February 23-25, 2021, pages 65–79. USENIX Association, 2021.

[74] Derek Gordon Murray, Grzegorz Milos, and Steven Hand. Improving xen security through disaggregation. In Proceedings of the Fourth ACM SIGPLAN/SIGOPS International Conference on Virtual Execution Environments, VEE ’08, page 151–160, New York, NY, USA, 2008. Association for Computing Machinery.

[75] Gaoning Pan, Xingwei Lin, Xinlei Ying, Jiashui Wang, and Chunning Wu. Scavenger: Misuse error handling leading to qemu/KVM escape. In Black Hat Asia, 2021.

[76] Chang Hyun Park, Taekyung Heo, and Steven Hand. Hybrid tlb coalescing: Improving tlb translation coverage under diverse fragmented memory allocations. In Proceedings of the 44th Annual International Symposium on Computer Architecture, ISCA ’17, page 444–456, New York, NY, USA, 2017. Association for Computing Machinery.

[77] Simon Peter, Jialin Li, Irene Zhang, Dan R. K. Ports, Doug Woos, Arvind Krishnamurthy, Thomas Anderson, and Timothy Roscoe. Arrakis: The operating system is the control plane. In 11th USENIX Symposium on Operating Systems Design and Implementation (OSDI 14), pages 1–16, Broomfield, CO, October 2014. USENIX Association.

[78] Binh Pham, Ján Veselý, Gabriel H. Loh, and Abhishek Bhattacharjee. Large pages and lightweight memory management in virtualized environments: Can you have it both ways? In Proceedings of the 48th International Symposium on Microarchitecture, MICRO-48, page 1–12, New York, NY, USA, 2015. Association for Computing Machinery.

[79] Gerald J Popek and Robert P Goldberg. Formal requirements for virtualizable third generation architectures. Communications of the ACM, 17(7):412–421, 1974.

[80] Sebastian Roschke, Feng Cheng, and Christoph Meinel. Intrusion detection in the cloud. In 2009 Eighth IEEE International Conference on Dependable, Autonomic and Secure Computing, pages 729–734, 2009.

[81] Adam Ruprecht, Danny Jones, Dmitry Shiraev, Greg Harmon, Maya Spivak, Michael Krebs, Miche Baker-Harvey, and Tyler Sanderson. Vm live migration at scale. In Proceedings of the 14th ACM SIGPLAN/SIGOPS International Conference on Virtual Execution Environments, VEE ’18, page 45–56, New York, NY, USA, 2018. Association for Computing Machinery.

[82] Jee Ho Ryoo, Nagendra Gular, Shuang Song, and Lizy K. John. Rethinking tlb designs in virtualized environments: A very large part-of-memory tlb. In Proceedings of the 44th Annual International Symposium on Computer Architecture, ISCA ’17, page 469–480, New York, NY, USA, 2017. Association for Computing Machinery.

[83] David Schrømme, Samuel Weiser, Stefan Steinegger, Martin Schwarzl, Michael Schwarz, Stefan Mangard, and Daniel Gruss. Donky: Domain keys - efficient in-process isolation for RISC-V and x86. In Srdjan Capkun and Franziska Roesner, editors, 29th USENIX Security Symposium, USENIX Security 2020, August 12-14, 2020, pages 1677–1694. USENIX Association, 2020.

[84] L. H. Seawright and R. A. MacKinnon. Vm/370—a study of multiplicity and usefulness. IBM Systems Journal, 18(1):4–17, 1979.

[85] Zhijian Shao, Jian Weng, and Yue Zhang. 3d red pill: A guest- to-host escape on qemu/KVM virtio devices. In Black Hat Asia, 2020.

[86] Le Shi, Yuming Wu, Yubin Xia, Nathan Dautenhahn, Haibo Chen, Binyu Zang, and Jinming Li. Deconstructing xen. In 24th Annual Network and Distributed System Security Symposium, NDSS 2017, San Diego, California, USA, February 26 - March 1, 2017. The Internet Society, 2017.

[87] Baibhav Singh and Rahul Kashyap. Back to the future: A radical insecure design of KVM on arm. In Black Hat USA, 2018.

[88] Udo Steinberg and Bernhard Kauer. Nova: A microhypervisor-based secure virtualization architecture. In Proceedings of the 5th European Conference on Computer Systems, EuroSys ’10, page 209–222, New York, NY, USA, 2010. Association for Computing Machinery.

[89] Jakub Szef and Ruby B. Lee. Architectural support for hypervisor-secure virtualization. In Proceedings of the Seventeenth International Conference on Architectural Support for Programming Languages and Operating Systems, ASPLOS XVII, page 437–450, New York, NY, USA, 2012. Association for Computing Machinery.

[90] Lluís Vilanova, Marc Jordà, Nacho Navarro, Yoav Etsion, and Zhi Wang and Xuxian Jiang. Hypersafe: A lightweight approach to provide lifetime hypervisor control-flow integrity. In 31st IEEE Symposium on Security and Privacy, S&P 2010, 16-19 May 2010, Berkeley/Oakland, California, USA, pages 380–395. IEEE Computer Society, 2010.
[93] Zhi Wang, Chiachih Wu, Michael Grace, and Xuxian Jiang. Isolating commodity hosted hypervisors with hyperlock. In Proceedings of the 7th ACM European Conference on Computer Systems, EuroSys ’12, page 127–140, New York, NY, USA, 2012. Association for Computing Machinery.

[94] Andrew Whitaker, Marianne Shaw, and Steven D. Gribble. Scale and performance in the denali isolation kernel. In 5th Symposium on Operating Systems Design and Implementation (OSDI 02), Boston, MA, December 2002. USENIX Association.

[95] Chiachih Wu, Zhi Wang, and Xuxian Jiang. Taming hosted hypervisors with (mostly) deprivileged execution. In 20th Annual Network and Distributed System Security Symposium, NDSS 2013, San Diego, California, USA, February 24-27, 2013. The Internet Society, 2013.

[96] Fengzhe Zhang, Jin Chen, Haibo Chen, and Binyu Zang. Cloudvisor: Retrofitting protection of virtual machines in multi-tenant cloud with nested virtualization. In Proceedings of the Twenty-Third ACM Symposium on Operating Systems Principles, SOSP ’11, page 203–216, New York, NY, USA, 2011. Association for Computing Machinery.

[97] Xiantao Zhang, Xiao Zheng, Zhi Wang, Hang Yang, Yibin Shen, and Xin Long. High-density multi-tenant bare-metal cloud. In Proceedings of the Twenty-Fifth International Conference on Architectural Support for Programming Languages and Operating Systems, ASPLOS ’20, page 483–495, New York, NY, USA, 2020. Association for Computing Machinery.