Performance Analysis of a novel Fusion Adder/Subtractor design

JosephAnthonyPrathap, R.Nithya, P.Jegadeeshwari, Dr. Gowrishankar Kasilingam

1Associate Professor, Department of Electronics & Communication Engineering, Vardhaman College of Engineering, Hyderabad, India
2,3Assistant Professor, Department of Electronics & Communication Engineering, Cuddalore, Tamil Nadu, India
3Associate Professor, Department of Bio-medical Engineering, Rajiv Gandhi College of Engineering and Technology, Puducherry, India

emails: 1 japtuhi1116@gmail.com

Abstract--This paper proposes a novel fusion 1 bit Adder/ Subtractor design using the CMOS transistor. The proposed novel fusion 1 bit Adder/Subtractor is utilized in the design of parallel adder/ subtractor with the resolution upto 27 bits. Though there are several design technologies like static CMOS logic, Dynamic CMOS, CPL, Transmission Gate Array, the proposed Fusion Design is advantageous for minimized chip area, low power consumption and high speed of operation. In this work, two circuit topologies are proposed by utilizing the 8T and 12T XOR CMOS design for the novel Fusion Adder/Subtractor. This paper compares the parametric values of power, delay and area with the existing methods. The proposed design is developed using the Cadence Virtuoso Tool with the technology of 45 nm. The proposed fusion design exhibits low power and delay as the resolution of the design is increased. Also the chip area is 0.3138µm² for the 28T FAS circuit and 0.165 µm² for the proposed 24T FAS circuit.

Keywords--Adder/ Subtractor, CMOS transistors, Low Power Design, EDA tools

1. INTRODUCTION

Among the arithmetic operators, the additions and subtractions are integral part of any hardware implemented system. The transistor level design of 1 bit full adder has evolved in years from the conventional static CMOS technology to the hybrid logic in order to achieve the advantages like the reduced number of transistors, minimization on chip area, low power consumption and high speed of operation. Though there are different topologies developed for the transistor level adder circuit design, the parametric analysis is enhanced either by the hybridization or by the technology with which the adder circuit is developed. The power consumption of the individual adder circuit is the key factor in the design.

The adder circuit implemented with the conventional CMOS transistor has the same speed and power consumed as compared to the TG and LP based adder circuit [1]. Also the transistor level full adder design without inverter consumes low power [2][3]. The influence of the design technology is directly proportional to the performance of the circuit. The 90 nm and 55 nm technology design of the full adder shows high performance under varying voltage and...
temperature [4]. The positive feedback adiabatic logic based adder saves more power than the conventional CMOS adder design [5]. Although the adder designed with 65 nm technology maintains the speed, the leakage power is high [6]. The full adder developed using the 180nm and 65nm technology operates at the low voltage and generates the full swing outputs [7].

With the advent of hybrid technology, the adder circuits are dominant in the many applications. The hybrid CMOS design when supplied to voltage from 1V to 2.4V, has better parametric evaluations with respect to power, delay and PDP [8]. The extension of the full adder circuit to higher resolution adders introduces delay in the design. The 56 bit hybrid adder produces group carry propagates and generates by utilizing the complement Ling’s carries [9]. By developing a library which consists of twenty different full adder topologies, the circuit designers can select any of these full adder based on the requirement of the applications and parameters like power, performance and area [10].

This paper proposes a novel fusion adder/subtractor circuit which performs as adder and subtractor subjected to the activation of the enable signal. In this work, the Fusion Adder/Subtractor (FAS) proposes two design topologies (i) Proposed 28 Transistor based FAS and (ii) Proposed 24 Transistor based FAS. The designed circuits are implemented with the different resolutions and compared with the parameters of Power, Delay and Area. The schematic and layout of the proposed fusion is designed using the 45 nm technology in the Cadence Virtuoso Tool.

2. PROPOSED FUSION ADDER/SUBTRACTOR

The proposed method includes two transistor topologies for the XOR circuit of the FAS. The two XOR circuit topologies consist of 12T and 8T CMOS transistors which constitute proposed 28T FAS and 24T FAS respectively.

A. Proposed 28T FAS design

In this proposed 28T FAS method, the external input control line E is applied with carry input of the LSB of the full adder. This control line decides the type of operation, whether addition or subtraction.

i. Addition Operation of Proposed 28T-FAS

The addition operation in the proposed 28T FAS circuit is performed by assigning the LOW value for the input E which will ON the P2 and OFF the N4 transistor as shown in Fig.1. When the HIGH value is given in B, the inverter circuit switches OFF the P0 and switches ON the N0 which yields the output of the inverter to be LOW. This LOW will switch ON the P3 and OFF the N1 transistor. Also the HIGH at the B input will simultaneously OFF the P1 and P4. Since the E is LOW, the inverter consisting of P5 and N5 give the HIGH output. This HIGH makes the N2 and N3 as switched ON. The ON mode of P3 and N3 transistors give LOW value as input to the third inverter (P6 and N6) to produce the HIGH output which is similar to the B input. When the value of B is LOW, the inverter out is HIGH which will switch OFF the P3 and ON the N1 transistor. The P1 and P4 will be ON as the input of B is given as LOW. As E is LOW, the second inverter will give a HIGH value that switch ON the N2 and N3 transistors. Now the ON mode of transistors P1, P2, N1 and N2 give the HIGH to the third inverter input to generate the same LOW value of B at the output of the third inverter.

Now if the value of A and B = HIGH, the P7 will OFF and N7 will ON and ensures the LOW value to pass through the N7 as input to the fourth inverter to make P9 as OFF and N9 as ON and in parallel activates the N11 which connects the transmission pairs N12 & P12 and N13 & P13. The LOW/HIGH value of the fourth inverter input/output accordingly switches ON the N12 and P12 pairs to produce the COUT/BORROW output as HIGH. The output to the fourth inverter HIGH will make P11 as OFF and its source is connected with HIGH value of E and simultaneously N10 is ON gives the output of SUM/DIFFERENCE as LOW. Similar discussion can hold true for the remaining three combinations of A and B values.
ii. Subtraction Operation of Proposed 28T-FAS

The subtraction operation in the proposed 28T FAS circuit is performed by assigning the HIGH value for the input E which will OFF the P2 and ON the N4 transistor. When the HIGH value is given in B, the inverter circuit switches OFF the P0 and switches ON the N0 which yield the output of the inverter to be LOW. This LOW will switch ON the P3 and OFF the N1 transistor. Also the HIGH at the B input will simultaneously OFF the P1 and P4. Since the E is HIGH, the inverter consisting of P5 and N5 give the LOW output, which switches OFF the N2 and N3. The ON of P3 and N4 transistors give HIGH value as input to the third inverter (P6 and N6) to produce the LOW output which is complement to the B input. When the value of B is LOW, the inverter out is HIGH which will switch OFF the P3 and ON the N1 transistor. The P1 and P4 will be ON as the input of B is given as LOW. As E is HIGH, the second inverter will give a LOW value that switch OFF the N2 and N3 transistors. Now the ON mode of transistors P1, N1, P4 and P4 give the LOW to the third inverter input to generate the HIGH value (complement of B) at the output of the third inverter.

Now if the value of A & B= HIGH, the P7 will OFF and N7 will ON and ensures the HIGH value to pass through the N7 as input to the fourth inverter to make P9 as OFF and N9 as ON and activates the N11 which connects the transmission pairs N12 &P12 and N13 &P13. The HIGH/LOW value of the fourth inverter input/output accordingly switches ON the N13 and P13 pairs to produce the BORROW output as HIGH. The output to the fourth inverter LOW will make P11 as ON and its source is connected with HIGH value of E and simultaneously N10 is ON gives the output of DIFFERENCE as HIGH. The remaining three combinations of A and B can be evaluated in the similar manner. The transistor scaling for the proposed 28T FAS design with the 45 nm technology is presented in the Table 1.

**Table 1: Transistor Scaling of the Proposed 28T FAS Circuit**

| Transistor Name | 28T FAS in 45 nm Technology |
|-----------------|----------------------------|
| Width (W) (nm)  | Length (L) (nm)            |
| P0, P5, P6, P9  | 240                        | 45                        |
| N0, N5, N6, N9  | 120                        | 45                        |
| P1, P2          | 480                        | 45                        |
| N1, N2          | 120                        | 45                        |
| P3, P4, P7, P8, P10, P11 | 360           | 45                        |
| N3, N4, N7, N8, N10, N11 | 120           | 45                        |
| P12, P13        | 120                        | 45                        |
| N12, N13        | 120                        | 45                        |
B. Proposed 24T Fusion Adder/Subtractor

In this proposed 24T FAS, the XOR gate implemented by using 8 Transistors. Fig. 2 shows the circuit of the proposed 24T FAS. By implementing XOR with 8T, the transistor count of the circuit is reduced and hence the power consumed is low.

i. Addition operation of Proposed 24T-FAS

The addition operation in the proposed 24T FAS circuit is performed by assigning the LOW value for the E input, which gives the direct pass through of B value. If the value of B is HIGH, then the inverter circuit switches OFF the P0 and switches ON the N0 which yields the output of the inverter to be LOW. This LOW will switch ON the P2 and as E is LOW, P1 is switched ON and N1 is switched OFF. Also, the P1 is ON and the source value of LOW is connected from the first inverter output will pass through to produce the HIGH output at the second inverter output which is the direct transfer of B value. This HIGH output is connected to the third inverter circuit to produce the HIGH and to switch ON N6 transistor. The LOW from the third inverter switches ON the P6 transistor. Now if the value of A and B are LOW, the P5 will ON and N5 will OFF and the third inverter output LOW will ON the P6 and ensures the LOW value to pass through the P6 as input to the fourth inverter to make P7 as ON and N7 as OFF and E=0 activates the P8 which connects the transmission pairs N10 &P10 and N11 & P11. The LOW/HIGH value of the fourth inverter input/output accordingly switches ON the N10 and P10 pairs to produce the COUT/BORROW output as LOW. The output to the fourth inverter HIGH will make P9 as OFF and its source is connected with LOW value of E and simultaneously N8 is OFF gives the output of SUM/DIFFERENCE as LOW.

ii. Subtraction operation of Proposed 24T-FAS

The subtraction operation of the proposed 24T PAS circuit includes E as HIGH which complements the value of B to represent the 1’s Complement of the given value. If the value of B is HIGH, then the inverter circuit switches OFF the P0 and switches ON the N0 which yield the output of the inverter to be LOW. This LOW will switch ON the P2 and as E is HIGH, P1 is switched OFF and N1 is switched ON. Also, the N1 source is connected to HIGH from B will pass through to switch OFF P3 and switch ON N3 and produce the LOW output. This LOW output is connected to the third inverter circuit to produce the HIGH and to switch OFF N6 transistor.

| Transistor Name | 24T FAS in 45 nm Technology |
|-----------------|-----------------------------|
| Width(W) (nm)   | Length(L) (nm)              |
| P0, P3, P4, P7  | 240                         | 45                        |
| N0, N3, N4, N7  | 120                         | 45                        |
| P1, P2, P5, P6, P8, P9 | 360                       | 45                        |
| N1, N2, N5, N6, N8, N9 | 120                     | 45                        |
| P10, P11        | 120                         | 45                        |
| N10, N11        | 120                         | 45                        |
The HIGH from the third inverter switches OFF the P6 transistor. When the value of A and B are LOW, the P5 will ON and N5 will OFF and the third inverter output HIGH will OFF the P6 and ensures the HIGH value to pass through the P5 as input to the fourth inverter to make P7 as ON and N7 as OFF to give LOW output at the fourth inverter. As E=1, it activates the N8 which connects the transmission pairs N10 &P10 and N11 &P11. The HIGH/LOW value of the fourth inverter input/output accordingly switches ON the N10 and P10 pairs to produce the COUT/BORROW output as HIGH. The LOW output of the fourth inverter will make P9 as ON and its source is connected with HIGH value of E and simultaneously N8 is ON gives the output of SUM/DIFFERENCE as LOW. Similarly, the remaining three combinations of A and B values can be verified accordingly. Table 2 shows the transistor scaling of the proposed 24T FAS circuit.

3. RESULTS AND DISCUSSIONS

The simulation of the proposed 28T and 24T FAS is carried out using 45-nm technology due to the limitation of the Virtuoso tool in the lab. It is observed that in the present design, the power consumption could be minimized by mainly sizing the transistors in inverter circuits; while the carry propagation delay could be improved by mainly sizing the transistors of the transmission gates present between the paths from Cin to Cout. Power consumption, propagation delay, and PDP of the proposed 28T and 24T FAS are given in Table 3-8. The use of less number of transistors (24T) improved the speed. The power reduction in the proposed method is due to the transistor sizing of the inverter transistors at 240 nm PMOS devices for the proposed Fusion adder as depicted in Table 1 and 2. By the reduction in average power consumption and propagation delay, the PDP of the proposed 28T FAS and 24T FAS are given in Table 3-8. The behavior of the carry propagation delay when extended from $2^1$ to $2^7$ bits shows that the carry propagation delay increased almost linearly with respect to the proposed 1-bit full adder. The comparison of the proposed 28T FAS and 24T FAS with respect to the power consumption increases linearly as the resolution of the circuit is increased as shown in Fig.4. The delay of the proposed 28T FAS shows the consistent value with the increase in the design resolution. With respect to the 24T FAS design, the delay varies for every resolution of the design as depicted in Fig.5.
Fig. 6 presents the PDP for the 28T FAS and 24T FAS which is slightly increased for the 24T FAS at the design resolution of 2^2 and 2^3 bits. The reason for this increase is the high delay variation with the 24T FAS circuit. The transistor count of the proposed 28T and 24T FAS is increased as the resolution of the design increases as given in Fig. 7. The proposed 28T and 24T FAS method with the 180 nm technology exhibits low power consumption of 0.01488 µW and minimum delay of 56.39 ps yielding the PDP as 0.00084 fJ as given in Table 3. The proposed method is validated using the 90 nm technology that produces the power consumed as 0.659 µW and delay of 3.04 ps which is comparatively high as given in Table 4. Though the delay of the proposed method is high, the reduced power consumption generates the PDP as low as 0.002003 fJ as given in the Table 4. The Table 3 and 4 assure that the proposed FAS out performs the existing methods in terms of the parametric analysis.

Table 5 shows the power and delay analysis of the proposed 28T and 24TFAS design in 45nm technology with 0.7V supply voltage. The delay of the 28T and 24T FAS are 10.19 ps and 4.385 ps respectively. This slight increase in the delay is due to the increase in the number of transistors which is accepted as the proposed method is a Fusion of Adder and Subtractor circuit. Moreover the power is 0.2166 µW for 28T FAS and 0.197 µW for 24T FAS. These low power values compensate the increased delay to generate low PDP value as 0.002207 fJ for the 28TFAS and 0.000863 fJ for the 24T FAS. Table 6 depicts the parametric evaluation of the proposed 28T FAS and 24T FAS for different resolutions with the 45 nm technology. The delay value and the PDP are low for the 26 and 27 bit resolution of the 24T FAS in 45 nm technology as shown in Table 6. The layout of the proposed 24T FAS is designed using the Virtuoso Tool with 45 nm technology. The area occupied for the physical design is 0.3138 µm² for the proposed 28T FAS circuit and 0.165 µm² for the proposed 24T FAS circuit as given in Table 7.

![Fig. 3: Implementation of the proposed 128 bit 24T FAS using the Virtuoso Tool](image)

![Fig. 4: Comparison of the Average Power Consumption of 28T FAS and 24T FAS for different resolutions](image)
Fig. 5: Comparison of the Propagation Delay of 28T FAS and 24T FAS for different resolutions

Fig. 6: Comparison of the PDP of 28T FAS and 24T FAS for different resolutions

Fig. 7: Comparison of the Transistor Count of 28T FAS and 24T FAS for different resolutions
Fig. 8(a). Layout of 28T FAS circuit and 8(b) Layout of 24T FAS in 45nm technology using Virtuoso Tool

TABLE 3: PARAMETRIC ANALYSIS COMPARISON OF THE PROPOSED METHOD WITH 180 NM TECHNOLOGY AT 1.8 V SUPPLY VOLTAGE

| Design          | Avg. Power (µW) | Delay (ps) | PDP (fJ) | Transistor Count | Reference |
|-----------------|-----------------|------------|----------|------------------|-----------|
| C-CMOS          | 6.2199          | 292.1      | 1.8168   | 28               | [15]      |
| Mirror          | 6.0797          | 281.6      | 1.7121   | 28               | [15]      |
| CPL             | 7.7198          | 183.9      | 1.4202   | 32               | [16,17]   |
| TFA             | 8.2491          | 287.1      | 2.3683   | 16               | [18]      |
| TGA             | 8.4719          | 293.9      | 2.8989   | 20               | [19,20]   |
| 14T             | 12.721          | 381.7      | 4.8558   | 14               | [21]      |
| HPSC            | 6.3798          | 273.7      | 1.7461   | 22               | [23]      |
| Majority        | 6.3227          | 185.4      | 1.1722   | --               | [24]      |
| 24T             | 15.91           | 314.2      | 4.998    | 24               | [25]      |
| FA_Hybrid       | 5.978           | 252.3      | 1.508    | 24               | [26]      |
| FA_DPL          | 19.56           | 226.6      | 4.432    | 22               | [27]      |
| FASRCPL         | 20.78           | 220.6      | 4.585    | 20               | [27]      |
| Hybrid_FA       | 4.1563          | 224        | 0.931    | 16               | [30]      |
| 28T             | 0.0148          | 56.39      | 0.0008   | 28               | Proposed  |
### Table 4: Parametric Analysis Comparison of the Proposed Method with 90 nm Technology at 1.2V Supply Voltage

| Design  | Average Power (µW) | Delay (ps) | PDP (fJ) | Transistor Count | References |
|---------|--------------------|------------|----------|------------------|------------|
| C-CMOS  | 1.5799             | 0.126      | 0.20048  | 28               | [15]       |
| Mirror  | 1.5701             | 0.122      | 0.19249  | 28               | [15]       |
| CPL     | 1.7598             | 0.079      | 0.1392   | 32               | [16,17]    |
| TFA     | 1.7363             | 0.319      | 0.55526  | 16               | [18]       |
| TGA     | 1.7619             | 0.231      | 0.40823  | 20               | [19,20]    |
| 14T     | 3.3297             | 0.338      | 1.12843  | 14               | [21]       |
| HPSC    | 1.56               | 0.220      | 0.34429  | 22               | [23]       |
| Majority| 1.5751             | 0.093      | 0.1479   | --               | [24]       |
| 24T     | 7.707              | 0.140      | 1.0836   | 24               | [25]       |
| FA_Hybrid| 6.21              | 0.143      | 0.888    | 24               | [26]       |
| FA_DPL  | 7.34               | 0.254      | 1.864    | 22               | [27]       |
| FASRCPL | 7.4                | 0.167      | 1.235    | 20               | [27]       |
| Hybrid_FA| 1.17664           | 0.091      | 0.10742  | 16               | [30]       |
| 28T     | 0.659              | 3.04       | 0.00200  | 28               | Proposed   |

### Table 5: Parametric Analysis Comparison of Proposed Method

| Design Technology | Average Power (µW) | Delay (ps) | PDP (fJ) | Transistor Count | References |
|-------------------|--------------------|------------|----------|------------------|------------|
| 45nm              | 3.053              | 0.344      | 0.00105  | 14               | [28]       |
| 180nm             | 55                 | 289        | 15.89    | --               | [27]       |
| 180nm             | 60.6               | 278        | 16.85    | --               | [27]       |
| 45nm              | 0.2166             | 10.19      | 0.002207 | 28               | Proposed   |
| 45nm              | 0.197              | 4.385      | 0.000863 | 24               | Proposed   |

### Table 6: depicts the parametric evaluation of the proposed 28T FAS and 24T FAS for different resolutions with the 45 nm technology

| Resolution of the Design | Proposed Fusion Adder/Subtractor with 28T | Proposed Fusion Adder/Subtractor with 24T |
|--------------------------|------------------------------------------|------------------------------------------|
| 1bit                     | PWR (µW)  0.2166  6 Delay (ps) 10.19 PDP (fJ) 0.002207 7 Transistor Count 28 | PWR (µW) 0.197 4 Delay (ps) 4.385 PDP (fJ) 0.000863 3 Transistor Count 24 |
| 2bit                     | PWR (µW) 0.4014 Delay (ps) 10.13 PDP (fJ) 0.004066 6 Transistor Count 56 | PWR (µW) 0.442 20.08 Delay (ps) 0.08887 4 Transistor Count 48 |
| Design        | Area, µm² | References |
|---------------|-----------|------------|
| C-CMOS        | 8.13      | [29]       |
| CPL           | 10.462    | [16, 17]   |
| TFA           | 6.66      | [18]       |
| TGA           | 8.18      | [20]       |
| 16T-Hybrid    | 7.27      | [30]       |
| 10T           | 5.12      | [31]       |
| GDI           | 4.93      | [32]       |
| 14T MVT-GDI   | 6.32      | [28]       |
| AIL, PT       | 246, 243  | [27]       |
| Hybrid_FA     | 102.94    | [30]       |
| Hybrid_FA     | 25.84     | [30]       |
| 28T           | 0.3138    | Proposed   |
| 24T           | 0.165     | Proposed   |

### 4. CONCLUSION

In this paper, a low-power Fusion 1-bit binary full adder/subtractor has been proposed and the design has been extended for higher resolutions from 2² bits to 2⁷ bits. The simulation was carried out using standard Cadence Virtuoso tools for the proposed 28T and 24T FAS using the 45-nm technology. The parametric analysis of power, delay, PDP and area were manipulated, and found to be satisfactory. The performance analysis, in comparison with the existing circuits validates the effectiveness of the proposed method with area as low as 0.3138µm² for 28T FAS and 0.165µm² for 24T FAS. The use of buffers at appropriate stages of the high resolution FAS circuits would further regularize the delay variation of the proposed method. Further works could be analyzed with the inclusion of buffer in higher resolution using reduced nm technology.
5. REFERENCES

[1] Massimo Alioto and Gaetano Palumbo, “Analysis and Comparison on Full Adder Block in Submicron Technology”, IEEE Transactions on Very Large Scale Integration Systems, Vol. 10, No. 6, pp. 806-823, December 2002.

[2] Ahmed M. Shams and Magdy A. Bayoumi, “A Novel High-Performance CMOS 1-Bit Full-Adder Cell”, IEEE Transactions On Circuits And Systems—II: Analog And Digital Signal Processing, Vol. 47, No. 5, pp. 478-481, May 2000.

[3] Vishesh Dokania, Richa Verma, Manisha Guduri, Aminul Islam, “Design of 10T full adder cell for ultralow-power applications”, Ain Shams Engineering Journal, Vol. 9, No. 4, pp. 2365-2372, December 2018.

[4] Pankaj Kumar, Rajender Kumar Sharma, “Low voltage high performance hybrid full adder”, Engineering Science and Technology, an International Journal, Vol. 19, No. 1, pp. 559-565, March 2016.

[5] Akshitha, Niju Rajan, “Power Reduction of Half Adder and Half’ Subtractor using Different Partial Adiabatic Logic Styles”, International Conference on Intelligent Sustainable Systems (ICISS 2019), IEEE Xplorer, DOI: 978-1-5386-7799, pp.87-91, 2019.

[6] Sohan Purohit and Martin Margala, “Investigating the Impact of Logic and Circuit Implementation on Full Adder Performance”, IEEE Transactions on Very Large Scale Integration Systems, Vol. 20, No. 7, pp. 1327-1331, July 2012.

[7] Priya Agrawal, D.K.Raghuvanshi, M.K.Gupta, “A Low-Power High-Speed 16T 1-Bit Hybrid Full Adder”, Proceeding International conference on Recent Innovations in Signal Processing and Embedded Systems (RISE-2017), pp.348-352, October 2017.

[8] Venkata Rao Tirumalasetty & Madhusudhan Reddy Machupalli, “Design and Analysis of Low Power High Speed 1-Bit Full Adder Cells for VLSI Applications”, International Journal of Electronics, Vol. 106, No 4, pp. 521-536, November 2019.

[9] Yuke Wang, C. Pai, and Xiaoyu Song, “The Design of Hybrid Carry-Lookahead/Carry–Select Adders”, IEEE Transactions On Circuits And Systems—II: Analog And Digital Signal Processing, Vol. 49, No. 1, pp. 16-24, January 2002.

[10] Ahmed M. Shams, Tarek K. Darwish, and Magdy A. Bayoumi, “Performance Analysis of Low-Power 1-Bit CMOS Full Adder Cells”, IEEE Transactions On Very Large Scale Integration Systems, Vol. 10, No. 1, pp. 20-29, February 2002.

[11] K. Navi, M. Maeen, V. Foroutan, S. Timarchi, and O. Kavehei, “A novel low-power full-adder cell for low voltage,” VLSI J. Integr., Vol. 42, No. 4, pp. 457–467, Sep. 2009.

a. Radhakrishnan, “Low-voltage low-power CMOS full adder,” IEEE Proceedings Circuits Devices Systems, Vol. 148, No. 1, pp. 19–24, Feb. 2001.

[12] R. Zimmermann and W. Fichtner, “Low-power logic styles: CMOS versus pass-transistor logic,” IEEE Journal on Solid-State Circuits, Vol. 32, No.7, pp. 1079–1090, Jul. 1997.

[13] M. Alioto, G. Di Cataldo, and G. Palumbo, “Mixed full adder topologies for high-performance low-power arithmetic circuits”, Microelectron. Journal, Vol. 38, No. 1, pp. 130–139, Jan. 2007.

[14] C. H. Chang, J. M. Gu, and M. Zhang, “A review of 0.18-μm full adder performances for tree structured arithmetic circuits,” IEEE Transactions on Very Large Scale Integration Systems, Vol. 13, No. 6, pp. 686–695, Jun. 2005.

[15] A. M. Shams, T. K. Darwish, and M. A. Bayoumi, “Performance analysis of low-power 1-bit CMOS full adder cells,” IEEE Transactions on Very Large Scale Integration Systems, Vol.10, No.1, pp. 20–29, Feb. 2002.

[16] M. Vesterbacka, “A 14-transistor CMOS full adder with full voltageswing nodes,” in Proceedings IEEE Workshop Signal Process. Systems (SiPS),Taipei, Taiwan, Oct. 1999, pp. 713–722.

[17] M. Zhang, J. Gu, and C.-H. Chang, “A novel hybrid pass logic with static CMOS output drive full-adder cell,” in Proceedings International Symposium on Circuits and Systems, pp. 317–320, May 2003.
[18] K. Navi, M. H. Moaiyeri, R. F. Mirzaee, O. Hashemipour, and B. M. Nezhad, “Two new low-power full adders based on majority-not gates,” Microelectronics Journal, Vol. 40, No. 1, pp. 126–130, Jan. 2009.

[19] C.-K. Tung, Y.-C. Hung, S.-H. Shieh, and G.-S. Huang, “A low-power high-speed hybrid CMOS full adder for embedded system,” in Proceedings IEEE Conference Design Diagnostics Electron. Circuits Systems, Vol. 13, pp. 1–4, Apr. 2007.

[20] S. Goel, A. Kumar, and M. A. Bayoumi, “Design of robust, energy-efficient full adders for deep-submicrometer design using hybrid-CMOS logic style,” IEEE Transactions on Very Large Scale Integration Systems, Vol. 14, No. 12, pp. 1309–1321, Dec. 2006.

[21] Mariano Aguirre-Hernandez and Monaco Linares-Ardana, “CMOS Full-Adders for Energy-Efficient Arithmetic Applications”, IEEE Transactions on Very Large Scale Integration Systems, Vol. 19, No. 4, pp. 718-721, April 2011

[22] Kishore Sanapala, Ramachandran Sakthivel, “Ultra-low-voltage GDI-based hybrid full adder design for area and energy-efficient computing systems”, IET Circuits, Devices & Systems, Vol. 13, No. 4, pp. 465-470, May 2019.

[23] Navi, K., Foroutan, V., Azghadi, M.R., ‘A novel low-power full-adder cell with new technique in designing logical gates based on static CMOS inverter’, Microelectronics Journal, Vol. 40, No. 10, pp. 1441–1448, 2009.

[24] Bhattacharyya, P., Kundu, B., Ghosh, S., et al.: 'Performance analysis of a low-power high-speed hybrid 1-bit full adder circuit’, IEEE Transactions on Very Large Scale Integration Systems, Vol. 23, No.10, pp. 2001–2008, 2015.

[25] Dokania, V., Verma, R., Manisha, G., et al.: ‘Design of 10T full adder cell for ultralow-power applications’, Ain Shams Engineering Journal, Vol. 9, No. 4, pp. 2363–2372, 2018.

[26] Lee, P.M., Hsu, C.H., Hung, Y.H.: ‘Novel 10-T full adders realized by GDI structure’. in Proceedings IEEE ISIC., Singapore, pp. 115–118, 2007.

[27] Kishore Sanapala, Ramachandran Sakthivel, “Ultra-low-voltage GDI-based hybrid full adder design for area and energy-efficient computing systems”, IET Circuits, Devices & Systems, Vol. 13, No. 4, pp. 465-470, May 2019.

[28] Navi, K., Foroutan, V., Azghadi, M.R., et al.: ‘A novel low-power full-adder cell with new technique in designing logical gates based on static CMOS inverter’, Microelectronics Journal, Vol. 40, No. 10, pp. 1441–1448, 2009.

[29] Bhattacharyya, P., Kundu, B., Ghosh, S., et al.: ‘Performance analysis of a low-power high-speed hybrid 1-bit full adder circuit’, IEEE Transactions on Very Large Scale Integration Systems, Vol. 23, No.10, pp. 2001–2008, 2015.

[30] Dokania, V., Verma, R., Manisha, G., et al.: ‘Design of 10T full adder cell for ultralow-power applications’, Ain Shams Engineering Journal, Vol. 9, No. 4, pp. 2363–2372, 2018.

[31] Lee, P.M., Hsu, C.H., Hung, Y.H.: ‘Novel 10-T full adders realized by GDI structure’. in Proceedings IEEE ISIC., Singapore, pp. 115–118, 2007.