Letters

Monitoring of SiC MOSFET Junction Temperature with On-state Voltage at High Currents

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Abstract: A junction temperature monitoring method has been presented based on the on-state voltage at high currents. With a simplified physical model, this method mapped the relationship between junction temperature and on-state voltage. The tough calibration and signal sensing issues are solved. Verified by body-diode voltage detecting method, the presented method shows a good performance and high accuracy, in the meantime, it would not change the modulation strategy and topology of the converter.

Keywords: Junction temperature monitoring, SiC MOSFET, conduction voltage

1 Introduction

In the last two decades, with the demonstration of electrical and thermal advantages, silicon carbide (SiC) devices have exhibited attractive benefits, and were believed to be an alternative for conventional silicon (Si) devices. However, due to limitations such as technology status and production volume, the performance of SiC devices is still far away from their theoretical value, their price is five to eight times of regular Si devices [1-2].

To make better use of SiC devices, junction temperature monitoring can assure the normal operation of a power device under the thermal limit. In several applications, the working condition of converters may have unpredictable changes. Junction temperature monitoring will provide additional protection apart from over-current sensing and over-voltage sensing. Furthermore, because SiC dies have lower current rating compared with Si dies, it needs to contain more dies in a power module. The current sharing imbalance will generate several hotspots with higher temperatures. Junction temperature monitoring can supervise this phenomenon, improve the reliability of the power module, increase the capacity of inverter, and further enhance the power density [3-5]. The difficulties and drawbacks of junction temperature monitoring methods are presented in Tab. 1.

According to Ref. [9], the junction temperature monitoring method can be classified into four categories, namely conduction contact-based method, electro-thermal model-based method, optical methods, and temperature sensitive electrical parameters (TSEPs)-based methods [9]. Ref. [17] analyzed the benefits and drawbacks of each category considering various aspects such as accuracy, control strategy invasion, and hardware invasion. Because of the existing flaws in the state-of-the-art SiC wafers, electrons may be trapped after the high current conduction. This issue brings the random change of static parameters and unstable measurement. It baffles engineers to monitor the SiC metal-oxide-semiconductor field-effect transistor (MOSFET) through the same method used by Si insulated gate bipolar transistor (IGBT). A few previously presented junction temperature measurement
methods are listed in Tab. 1, and the difficulties and drawbacks have been introduced. Ref. [16] presents a body-diode voltage detection-based method in which a negative voltage is applied to the gate-source terminal of the SiC MOSFET. Since, it can only measure the junction temperature of SiC MOSFET without any additional anti-parallelled diode, this method cannot be used for on-line monitoring [16].

From Tab. 1, on-state voltage method is the most feasible method for on-line junction temperature monitoring of SiC. However, there are two issues that have to be resolved before applying this method in a real-world application. The first one is the calibration of the temperature-voltage relationship without heating up the dies at a high current. The second one is the accuracy of the low voltage measurement circuit which can also bear high voltage switching.

This paper presents an accurate and feasible temperature monitoring method, which completely solves the abovementioned issues. A simplified physical model was presented to describe the relationship between temperature and on-state voltage. With the introduction of a reasonable on-state voltage measurement circuit and some practical considerations, the temperature monitoring method was developed and verified by the body-diode based method with a cautious experimental design.

2 Relationship between conduction voltage and junction temperature

The on-resistance in the MOSFET consists of eight parts [15], namely, the drain contact resistance ($R_{CD}$), substrate resistance ($R_S$), drift zone resistance ($R_D$), JFET zone resistance ($R_{JFET}$), cumulative resistance ($R_A$), channel resistance ($R_{CH}$), N$^+$zone resistance ($R_{NC}$) and the source base resistance ($R_{CS}$), which are depicted in Fig. 1.

![Cross-section of a MOSFET cell](image)

Fig. 1 Cross-section of a MOSFET cell

$R_{CH}$, $R_{JFET}$ and $R_D$ play a key role and account for approximately 90% of the on-resistance of the entire MOSFET, which can be expressed as

$$R_{on} \approx R_D + R_{JFET} + R_{CH}$$

(1)

$R_D$ can be calculated as

$$R_D = \frac{1}{2Zq\mu_D N_D} \ln \left( \frac{a + 2t}{a} \right)$$

(2)

where $Z$ is the cell length, $q$ is the unit charge, $\mu_D$ is the
carrier mobility in the drift region, $N_D$ is the doping concentration, $a$ and $t$ are the relevant parameters of the semiconductor structure depicted in Fig. 1.

$$R_{\text{JFET}} = \frac{x_{\text{ip}}}{Z_0 \mu_n N_D (W_G - 2x_{\text{ip}} - 2W_G)}$$

(3)

where $\mu_n$ and $N_D$ are the carrier mobility and doping concentration in the JFET region, respectively; $x_{\text{ip}}$, $W_G$ and $W_0$ are the relevant parameters of the semiconductor structure depicted in Fig. 1.

$R_{\text{CH}}$ can be expressed as\(^{[21]}\)

$$R_{\text{CH}} = \frac{L_{\text{CH}}}{Z \mu_{\text{ai}} C_{\text{OX}} (V_G - V_{\text{TH}})}$$

(4)

where $L_{\text{CH}}$ is the channel length, $\mu_{\text{ai}}$ is the inversion laminar carrier mobility, $C_{\text{OX}}$ is the gate oxide capacitance, $V_G$ is the gate drive voltage, $V_{\text{TH}}$ is the MOSFET threshold voltage\(^{[22]}\).

In all the abovementioned equations, $\mu_{\text{ai}}, \mu_D$, $\mu_n$ and $V_{\text{TH}}$ are the temperature related parameters.

The inversion laminar carrier mobility can be expressed as

$$\mu_{\text{ai}} = 140 \left(\frac{T}{300}\right)^{-2.7}$$

(5)

where $T$ is the temperature (in Fahrenheit) of the MOSFET.

The MOSFET JFET region is also located in the drift region. To simplify the calculation, $\mu_D$ and $\mu_n$ can be expressed by $\mu_a$

$$\mu_a = \mu_{\text{ai}} \left(\frac{T}{300}\right)^{-k}$$

(6)

where $\mu_{\text{ai}}$ can be $\mu_{\text{D0}}$ or $\mu_{\text{lab}}$ which is an equivalent mobility at 300 K; $k$ is the coefficient related to the concentration of doping.

MOSFET threshold voltage can be expressed as

$$V_{\text{TH}} = \frac{\sqrt{4e_{\text{SiC}} KTN_A \ln(N_A / n_i)}}{C_{\text{OX}}} + \frac{2KT}{q} \ln \left(\frac{N_A}{n_i}\right)$$

(7)

where $e_{\text{SiC}}$ is the dielectric constant of the SiC material, $K$ is the Boltzmann coefficient, $N_A$ is the intrinsic carrier concentration.

With simplification, all parameters in the on-resistance of SiC MOSFET can be divided into two categories: temperature-sensitive parameters and structure-related constants which can be expressed as

$$R_{\text{ON}} = \frac{A_1}{\mu_n (V_G - V_{\text{TH}})} + \frac{A_2}{\mu_n}$$

(8)

$$\mu_a = \mu_{\text{ai}} \left(\frac{T}{300}\right)^{-A_3}$$

(9)

where $A_1$, $A_2$, and $A_3$ are structure-related constants. $A_1$ is the semiconductor parameter related to channel resistance, $A_2$ is the semiconductor parameter related to the resistance of the JFET and drift regions, $A_3$ is the semiconductor parameter related to comprehensive mobility. $A_1$, $A_2$, and $A_3$ obtained through the experimental data can ascertain the relationship between $R_{\text{ON}}$ and junction temperature, and thereafter the $I_T$-$T$-$V_{\text{DSon}}$ relationship can be characterized.

The temperature-voltage relationship can be approximated by polynomial equations. With cautious calibration and mapping, a thermo-electrical coupling model can be established and used for monitoring.

### 3 On-state voltage measurement and junction temperature monitoring

#### 3.1 On-state voltage measurement

In a feasible on-state voltage measuring circuit, high accuracy (mV-range), high blocking capability (kV-range) and rapid dynamic responses (μs-range) are required simultaneously. Because of the transition between the switch-on and switch-off states, an active control method (as depicted in Fig. 2) was used in this study. To simplify the circuit, the measurement circuit and the driving circuit shared the same power supply. During the on-time of the device under test (DUT), the on-state voltage was measured by injecting the bias current. During the off-time of the DUT, $V_{DS}$ rises to the DC link voltage (hundreds volts), and the diode $D_1$ can block the DC link voltage and protect the amplifier. $D_1$, $D_2$ and $D_3$ are the same type of rapid recovery diode STTH112UFY. An adjustable voltage regulator LM317 was used to generate the bias current for $D_1$ and $D_2$. Signal MOSFET BSS138N was adopted to filter invalid measurement data when the DUT is in off-state and to provide a discharge loop for $I_{\text{Bias}}$. To improve the sampling accuracy, a second-order
A low-pass filter circuit was added to filter the high-frequency noise generated during the switching process. Thereafter, a proportional amplifier circuit adjusted the measured signal to fit the isolation transformer and analog to digital converter (ADC). Finally, the analog signal is transmitted to the ADC of the processor through a compact capacitive isolation op amp.

Fig. 2 On-state voltage measurement circuit

The calibration circuit that indicates the temperature-voltage relationship is depicted in Fig. 3. This approach uses a half bridge module and a single pulse generator. The load is a fixed value power resistor, which can quickly set up and cut off the current. The amplitude of the pulse current can be controlled by a single pulse and DC voltage. Similar to other single pulse test circuits, a DC bus capacitor having a large value was required. A heater was used to control the junction temperature of the DUT.

Fig. 3 $T_J-V_{DSon}$ calibration schematic

Because the switching process of SiC MOSFET is rapid, high current oscillations will be noticed when turned on, which are affected by the parasitic parameters. A necessary delay (a few $\mu$s) is required to mitigate the oscillations. But a long delay will cause die self-heating and affect the calibration result. From a thermodynamic model, the influence of self-heating within 100 $\mu$s could be ignored. Therefore, the sampling time in this study was chosen to be in the range of 10-100 $\mu$s.

A house packaged SiC module rated at 1 200 V/300 A was tested, and the hardware is depicted in Fig. 4. The three-dimensional relationship of $I_D-T_J-V_{DSon}$ was mapped, as depicted in Fig. 5. It is necessary to align the current value and on-state voltage.

Fig. 4 Photograph of the calibration

Fig. 5 Waveform obtained during the calibration

Fig. 6 depicts the temperature-voltage relationship with varying currents. The SiC MOSFET module maintains a good linearity and high resolution at high currents. With a relatively large resolution (approximately 10 mV/°C), it is very suitable for on-line temperature monitoring. In the case of a fixed current, the application of the first-order polynomial fitting can satisfy engineering applications, as shown in Eq. (10)

$$T_J(V_{DS}, I = I_0) = kV_{DS} + b \quad (10)$$
3.2 Junction temperature monitoring and verification

To demonstrate the junction temperature monitoring ability and accuracy, a comparison and verification test was conducted, as depicted in Fig. 7. The body-diode voltage detecting-based method was used for verification. By comparing the predicted junction temperature, the feasibility of the presented method could be verified. Thus, there are two sets of temperature measurement circuits in Fig. 7. One is the on-state voltage measuring part for the conduction mode of SiC MOSFET (based on Fig. 2), which uses the same power supply as that of the DUT driver. The other circuit is the body-diode voltage measuring part with a low current injection when SiC MOSFET is shut down using a negative gate voltage. Because the body-diode requires the injection of a low reverse current, this part of the circuit requires another isolated power supply. $I_H$ is the high current source. When $S_2$ cuts off the high current flowing through the DUT, it is necessary to turn on $S_1$ in advance to provide a freewheeling loop for $I_H$. $I_{Bias}$ is the bias current injected into the MOSFET, $I_L$ is the low current injected into the body diode, these two currents are controlled by MOSFET S4 and S5.

At the beginning, the auxiliary switch $S_2$ was turned on, the DUT $S_3$ was turned on, and the adjustable current source fed a fixed large current. DUT $S_3$ heats itself and was water cooled to prevent it from reaching excessive temperature levels. During this step, the on-state voltage was recorded to predict the junction temperature. Thereafter, the freewheeling loop was turned on at time point 1, and $S_1$ was turned off at time point 2 to cut off the high current. After the high conduction current is cut off, the gate signal of SiC MOSFET was closed by a negative voltage at time point 3. Finally, a low current $I_L$ was injected into the body-diode. After time point 4, the body-diode voltage was recorded to detect the junction temperature. Fig. 8
depicts test waveform with physical quantities and scales marked in it. Because the DUT was shut down in a short time (100 μs in Fig. 8), the junction temperature changes slightly. Thus, the junction temperature measured by the two methods are comparable.

![Fig. 8 Test waveform with high current switching to low current](image)

The body-diode voltage of DUT was then calibrated as depicted in Fig. 9. \(I_L\) is a low constant current source, which is injected to the body-diode of the DUT, and its power loss can be ignored. During the calibration step, the junction temperature of the DUT was controlled using a heater, and the DUT was to be triggered off by a negative gate voltage. The calibrated temperature-voltage approximation line at different constant currents is depicted in Fig. 10. The curve also maintains a good linearity. However, the resolution is relatively small (approximately \(-2 \mu V/\circ C\)).

![Fig. 9 T-j-V calibration schematic](image)

The comparison of measurement results is listed in Tab. 2. When the current level is high (greater than or equal to 50% \(I_{D,\text{continuous}}\)), both the methods agree well with each other, and the error is less than 6%. Thus, the presented on-state voltage at a high current indicates the potential of this approach and can be used in the monitoring of junction temperature.

![Fig. 10 Calibration curves of body diode voltage-based method](image)

| \(I_D/A\) | \(V_{DS(UC)}(V)\) | Relationship at high current | \(T_{SHUC}/\circ C\) | \(T_{OLUC}(\mu\text{A-diode})/\circ C\) |
|---|---|---|---|---|
| 100 | 0.49 375 | \(T_{SHUC} = k V_{DS} + b\) | 54.75 | 49.90 |
| 200 | 1.08 125 | \(T_{SHUC} = k V_{DS} + b\) | 65.35 | 68.30 |
| 250 | 1.63 750 | \(T_{SHUC} = k V_{DS} + b\) | 97.45 | 102.40 |
| 300 | 2.46 250 | \(T_{SHUC} = k V_{DS} + b\) | 142.09 | 150.96 |

### 4 Conclusions

This study established a temperature-voltage model, and presented anti-interference, reliable and stable signal acquisition circuits for on-state voltage-based junction temperature monitoring method. By determining a reasonable sampling time, the trading-off between self-heating and accuracy was mitigated during the calibration stage. Verified by the on-state voltage via body-diode, the capability of temperature monitoring was demonstrated. This resulted in the considerable achievement of enhancing the power density and reliability of converter systems.

### References

[1] B Mouawad, A Hussein, A Castellazzi. A 3.3 kV SiC MOSFET half-bridge power module. 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Chicago, IL, 2018: 463-466.

[2] J D Vanwyk, F C Lee, Z Liang, et al. Integrating active, passive and emi-filter functions in power electronics systems: A case study of some technologies. IEEE Transactions on Power Electronics, 2005, 20(3): 523-36.
[3] B Lu, W Dong, Q Zhao, et al. Performance evaluation of CoolMOS™ and SiC diode for single-phase power factor correction applications. *Eighteenth Annual IEEE Applied Power Electronics Conference and Exposition*, 2003. Miami Beach, FL, USA, APEC’03, 2003(2): 651-657.

[4] Q Chen, Y Xu, J Liu, et al. Practical design considerations for IPEM-based PFC converter employing CoolMOS and SiC diode. *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition*, 2006, Dallas, TX, APEC’ 06, 2006: 1-6.

[5] B W Shook, A Nizam, Z Gong, et al. Multi-objective layout optimization for multi-chip power modules considering electrical parasitics and thermal performance. *2013 IEEE 14th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2013, Salt Lake City, UT, COMPEL2013, 2013: 1-4.

[6] P Q Ning, T Yuan, Y Kang, et al. Review of Si IGBT and SiC MOSFET based on hybrid switch. *Chinese Journal of Electrical Engineering*, 2019, 5(3): 20-29.

[7] K Li, G Y Tian, L Cheng, et al. State detection of bond wires in IGBT modules using eddy current pulsed thermography. *IEEE Transactions on Power Electronics*, 2014, 29(9): 5000-5009.

[8] X Perpina, X Jorda, M Vellvehi, et al. Long-term reliability of railway power inverters cooled by heat-pipe-based systems. *IEEE Transactions on Industrial Electronics*, 2011, 58(7): 2662-2672.

[9] Y Avenas, L Dupont, Z Khatir. Temperature measurement of power semiconductor devices by thermo-sensitive electrical parameters: A review. *IEEE Transactions on Power Electronics*, 2012, 27(6): 3081-3092.

[10] S Yang, A Bryant, P Mawby, et al. An industry-based survey of reliability in power electronic converters. *IEEE Transactions on Industry Applications*, 2011, 47(3): 1441-1451.

[11] H Luo, Y Chen, P Sun, et al. Junction temperature extraction approach with turn-off delay time for high-voltage high-power IGBT modules. *IEEE Transactions on Power Electronics*, 2015: 5122-5132.

[12] Z Zhang, F Wang, D J Costinett, et al. Online junction temperature monitoring using turn-off delay time for silicon carbide power devices. *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, Milwaukee, WI, ECCE2016, 2016: 1-7.

[13] M H M Sathik, J Pou, S Prasanth, et al. Comparison of IGBT junction temperature measurement and estimation methods: A review. *2017 Asian Conference on Energy, Power and Transportation Electrification (ACEPT)*, 2017, Singapore, ACEPT2017, 2017: 1-8.

[14] A Griffò, J Wang, K Colombage, et al. Real-time measurement of temperature sensitive electrical parameters in SiC power MOSFETs. *IEEE Transactions on Industrial Electronics*, 2018, 65(3): 2663-2671.

[15] H Mhiesan, J Umahouza, K Mordi, et al. Evaluation of 1.2 kV SiC MOSFETs in multilevel cascaded H-bridge three-phase inverter for medium-voltage grid applications. *Chinese Journal of Electrical Engineering*, 2019, 5(2): 20-29.

[16] C Herold, J Sun, P Seidel, et al. Power cycling methods for SiC MOSFETs. *2017 29th International Symposium on Power Semiconductor Devices and IC’s (ISPSD)*, 2017, Sapporo, 2017: 367-370.

[17] N Baker, M Lisserre, L Dupont, et al. Improved reliability of power modules: A review of online junction temperature measurement methods. *IEEE Industrial Electronics Magazine*, 2014, 8(3): 17-27.

[18] J Wu, L Zhou, X Du, et al. Junction temperature prediction of IGBT power module based on BP neural network. *Journal of Electrical Engineering and Technology*, 2014, 9(3): 970-977.

[19] N Baker, S Munk-Nielsen, F Iannuzzo, et al. Online junction temperature measurement using peak gate current. *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, Charlotte, NC, APEC2015, 2015: 1270-1275.

[20] J L Hudgins, G S Simin, E Santi, et al. An experimental study on estimating dynamic junction temperature of SiC MOSFET. *IEEE Transactions on Power Electronics*, 2003, 18(3): 907-914.

[21] S Fukunaga, T Funaki, S Harada, et al. An experimental study on dynamic junction temperature estimation of SiC MOSFET with built-in SBD. *IEICE Electronics Express*, 2019, 16(17): 1-3.

[22] D Schweitzer, H Pape, L Chen, et al. Transient dual interface measurement: A new JEDEC standard for the measurement of the junction-to-case thermal resistance. *Annual IEEE Semiconductor Thermal Measurement & Management Symposium*, 2011, 9(1): 222-229.