Computational Complexity Evaluation of Neural Network Applications in Signal Processing

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Abstract—In this paper, we provide a systematic approach for assessing and comparing the computational complexity of neural network layers in digital signal processing. We provide and link four software-to-hardware complexity measures, defining how the different complexity metrics relate to the layers’ hyper-parameters. This paper explains how to compute these four metrics for feed-forward and recurrent layers, and defines in which case we ought to use a particular metric depending on whether we characterize a more soft- or hardware-oriented application. One of the four metrics, called ‘the number of additions and bit shifts (NABS)’, is newly introduced for heterogeneous application. One of the four metrics, called ‘the number of additions and bit shifts (NABS)’, is newly introduced for heterogeneous application. One of the four metrics, called ‘the number of additions and bit shifts (NABS)’, is newly introduced for heterogeneous application. This metric takes into account the impact of the weights’ quantization type on the bitwidth used in the operation but also the type of quantization used in the arithmetical operations. We intend this work to serve as a baseline for the different levels (purposes) of complexity estimation related to the neural networks’ application in real-time digital signal processing, aiming at unifying the computational complexity estimation.

Index Terms—Neural network, Computational complexity, Hardware estimation, Signal processing.

I. INTRODUCTION

O VER the last few decades, neural networks (NNs) have begun to find widespread usage in a wide range of signal processing applications: filtering, parameter estimation, signal detection, system identification, pattern recognition, signal reconstruction, time series analysis, signal compression, signal transmission, etc. [1]–[4]. Audio, video, image, communication, geophysical and radar scanning data, are the examples of important signal types that typically undergo various forms of signal processing [5]–[7]. The key capabilities of NNs in signal processing are: performing distributed processing, emulating nonlinear transformations and processes, self-organizing, and enabling high-speed processing communication applications [8]–[10]. With these properties, NNs can provide a very powerful means of solving many signal processing tasks, particularly in the areas related to the nonlinear signal processing, real-time signal processing, adaptive signal processing, and blind signal processing [5], [11]–[13].

Real-time signal processing, as an example, is a field that enables technological breakthroughs by effectively incorporating signal processing in hardware: real-time and onboard signal processing is the key to the evolution of phones and watches into smartphones/smartwatches. To the best of our knowledge, one of the first real-time applications of NNs was discussed in 1989 [14], and numerous works since then have deliberated the challenges of implementing such solutions in hardware exploiting the notion of computational complexity [15]–[24].

From a computer science perspective, computational complexity analysis is almost always attributed to the Big-$O$ notation of the algorithm [25]–[27]. In general, the Big-$O$ notation is used to express an algorithm’s complexity while assessing its efficiency, which means that we are interested in how effectively the algorithm scales with the size of the dataset in terms of running time [28]–[30]. However, from the engineering standpoint, the Big-$O$ is often an oversimplified measure that cannot be immediately translated into the hardware resources required to realize the algorithm (NNs) in a hardware platform [16].

Due to this problem that refers to the absence of some “universal” measure, various works started to present complexity in terms of multiply and accumulate (MAC) [15]–[18], Kolmogorov complexity [19], the number of bit-operations (BOP) [20], [21], the number of real multiplications (RM) [22]–[24]. However, it is not always clear when to use each specific metric, and, more importantly, none of the metrics mentioned above shows the benefits of using different strategies of quantization for saving the complexity of implementing the multipliers.

As far as we know, no work has so far unified the computational metrics itemized above such that we have no universal metrics to compare the complexity when different types of quantization are applied for NN structures. In this paper, we solve this issue by carrying out a systematic computational complexity analysis for a zoo of NN layer types. In addition, we introduce a new useful metric: we coined ‘the number of additions and bit shifts’ (NABS). This metric takes into account the impact of the weights’ quantization type on the reduction of the multipliers’ implementation complexity used in an NN layer. Overall, we intend our work to give largely universal measures of complexity to establish a comparison baseline depending on whether the application is software- or hardware-based.

The paper is organized as follows. In Sec. [I] we describe the details of different computational metrics from soft- and hardware implementation levels. Sec. [III] presents how to compute the computational complexity of different NN layers. Sec. [IV] describes the results of our evaluation of how complexity grows against the design parameters of...
each NN layer. We also address the impact of quantization on different computational complexity metrics. Our findings are summarized in the conclusion.

II. FOUR METRICS OF COMPUTATIONAL COMPLEXITY

Accurate computational complexity evaluation is critical in the design of digital signal processing (DSP) devices to better understand the implementation feasibility and bottlenecks for each device’s structure. With this in mind, we summarize the four most commonly used different criteria for assessing the computational complexity, from the software level to the hardware level, in Fig. 1.

The first, most software-oriented, level of estimation traditionally deals only with counting the number of real multiplications of the algorithm \[31, 32\] (quite often defined per one processed element, say a sample or a symbol). This metric is the number of real multiplications (RM). When comparing computational complexity, the purpose of this high-level metric is to consider only the multipliers required, ignoring additions, because the implementation of the latter in hardware or software is initially considered cheap, while the multiplier is generally the slowest element in the system and consumes the largest chip area \[31, 33\]. This ignoring the additions can also be easily understood by looking at the Big-\(O\) analysis of multiplier versus adder. When multiplying two integers with \(n\) digits, the computational complexity of the multiplication instance is \(O(n^2)\), whereas the addition of the same two numbers has a computational complexity of \(\Theta(n)\) \[34\]. As a result, if you are dealing with floating-point values with 16 decimal digits, multiplication is by far the most time-consuming part of the implementation procedure. Therefore, when comparing solutions that use floating-point arithmetic with the same bitwidth precision, the RM metric provides an acceptable comparative estimate to qualitatively assess the complexity against some existing benchmarks (e.g. against the DSP operations for optical channel equalization tasks \[32\]).

When moving to fixed-point arithmetic, the second metric known as the number of bit-operations (BOP) must be adopted to understand the impact of changing the bitwidth precision on the complexity. The BOP metric provides a good insight into mixed-precision arithmetic performance, since we can forecast the BOP needed for fundamental arithmetic operations like addition and multiplication, given the bitwidth of two operands. In a nutshell, the BOP metric aims to generalize floating-point operations (FLOPs) to heterogeneously quantized NNs, as far as the FLOPs cannot be efficiently used to evaluate integer arithmetic operations \[21, 35\]. For the BOP metric, we have to include the complexity contribution of both multiplications and additions, since now we evaluate the complexity in terms of the most common operations in NNs: the multiply-and-accumulate operations (MACs) \[21, 35, 36\]. However, the BOP accounts for the scaling of the number of multipliers with the bitwidth of two operands, and the scaling of the number of adders with the accumulator bitwidth. Note that since most real DSP implementations use dedicated logic macros (e.g. DSP slice in Field Programmable Gate Arrays [FPGA] or MAC in Application Specific Integrated Circuit [ASIC]), the BOP metric fits as a good complexity estimation metric inasmuch as the BOP also accesses the MAC taking into account the particular bitwidth of two operands.

| Number of Real Multiplications | Number of Bit Operations | Number of Shift and Add Operations | Number of Hardware Logic Gates |
|--------------------------------|--------------------------|-----------------------------------|-------------------------------|
| which the NN model operates    |                          | where the bit precision of input, weights and activation function is taken into account | where only shifts and adders are used to implement all arithmetic operations of the NN model |
| Number of multiply-accumulate operations with bitwidth consideration |                          |                                  | Number of logic gates required in hardware when implementing the NN model |

Fig. 1: Diagram of computational complexity metrics illustrating the various levels of complexity measurement from software to hardware.

| TABLE I: Capacity ranges for XC4000 Series CLB Resources given in Ref. \[37\]. |
|---------------------------------|--------------------------|
| CLB Resource                    | Logic Gate Range         |
| Gate range per 4-input LUT (2 per CLB) | 1 to 9                  |
| Gate range per 3-input LUT      | 1 to 6                   |
| Gate range per flip-flop (2 per CLB) | 6 to 12                 |
| Total gate range per CLB        | 15 to 48                 |
| Estimated typical number of gates per CLB | 28.5                     |

\(^1\)The Big-\(O\) notation represents the worst case or the upper bound of the time required to perform the operation, Big Omega (\(\Omega\)) shows the best case or the lower bound whereas the Big Theta (\(\Theta\)) notation defines the tight bound of the amount of time required, in other words, \(f(n)\) is claimed to be \(\Theta(g(n))\) if \(f(n) = O(g(n))\) and \(f(n) = \Omega(g(n))\).
The progress in the development of new advanced NN quantization techniques [38–41] allowed implementing the fixed point multiplications participating in NNs efficiently, namely with the use of a few bit-shifters and adders [42–44]. Since the BOP lacks the ability to properly assess the effect of different quantization strategies on the complexity, a new, more sophisticated metric is required there. We introduce the third complexity metric that counts the number of total equivalent additions to represent the multiplication operation, called the number of additions and bit shifts (NABS). The number of shift operations can be neglected when calculating the computational complexity because, in the hardware, the shift can be performed without extra costs in constant time with the $O(1)$ complexity. Even though the cost of bit shifts can be ignored due to the aforementioned reasons, and only the total number of adders has to be accounted for to measure the computational complexity, we prefer to keep the full name “number of additions and bit shifts” to highlight that the multiplication is now represented as shifts and adders.

Finally, the metric which is closest to the hardware level is the number of logic gates (NLG) that is used for our evaluating method’s hardware (e.g. ASIC or FPGA) implementation. It is different from the NABS metric, as now the true cost of implementation is to be presented. In this case, the activation function cost, represented by look-up tables (LUT) is also taken into account. Additionally, other metrics like the number of flip-flops (FFs) or registers, the number of logic blocks used for general logic and memory blocks, or other special functional macros used in the design, are also relevant. As it is clear from this explanation, there will be no straightforward equation to convert the NABS to NLG as the latter depends on the circuit design adopted by the developer. Tools such as Synopsys Synthesis [45] for ASIC implementation can provide this kind of information. However, with regard to the FPGA design, it is harder to get a correct estimate of the gate count from the report of the FPGA tools [46].

In this paper, we advocate that the NLG metric should be applied to count the number of logic gates used to implement the hardware piece, similar to the concept of the Maximum Logic Gates metric for FPGA devices [37]. The Maximum Logic Gates metric is utilized to approximate the maximum number of gates that can be realized in the FPGA for a design consisting of only logic functions $^{2}$ Additionally, this metric is based on an estimate of the typical number of usable gates per configurable logic block (CLB) or logic cell multiplied by the total number of such blocks or cells [37]. With regard to the correspondence between CLB and logic gates number, see Table I [37].

It should be noted that Table I is based on an older, now obsolete, 4-input LUT architecture [37]. Newer FPGA families now feature a 6-input LUT architecture, and to address the resource consumption for the new generation of devices, a reasonable approximation would be to increase the ‘maximum gate range equivalent per LUT’ figure used in [37] by 50%. Note that the gate equivalence figures for FFs (registers) still hold true for the 6-input architecture. It is also worth

$^{2}$On-chip memory capabilities are not factored into this metric.

To conclude, we comment on universal metrics between the FPGA and the ASIC implementations. We emphasize that calculating an ASIC gate equivalent to an FPGA DSP slice is not a straightforward task because not all features are necessarily required when implementing the specific arithmetic function in an ASIC. However, utilizing the estimation approach laid out in Ref. [37], a figure can be obtained. Using the Xilinx Ultrascale + DSP48E2 slice basic multiplier functionality as an example (see Xilinx UG579 Fig. 1-1 in Ref. [47]) and pipelining it for maximum performance, it is possible to estimate the number of FFs and adders required for such an ASIC equivalent. Taking into account the structure of the multiplication of a $m$-bit number by a $n$-bit number, implemented using an array multiplier architecture, it is equivalent to $m \times n$ AND gates, $n$ half adders, and $(m - 2) \times n$ full adders. For example, the ASIC equivalence of a $27 \times 18$ multiplier in an FPGA would have 486 AND gates, 18 half adders, 450 full adders, and 90 Flip Flops.

### III. Mathematical Complexity Formulation

In this section, we provide a brief introduction to various types of NN: dense layer, Convolutional Neural Networks (CNN), Vanilla Recurrent Neural Networks (RNN), Long Short-Term Memory Neural Networks (LSTM), Gated Recurrent Units (GRU), and Echo State Networks (ESN). We investigate the computational complexity for each network in terms of RM, BOP and NABS. In this work, the computational complexity is formulated per layer, and the output layer is not taken into account for the complexity calculation to eliminate redundant computations if multiple layers or multiple NN types are combined. Table III in the section’s end summarizes the formulas for the RM, BOP, and NABS for all NN types studied.

#### A. Dense Layer

A dense layer, also known as a ‘fully connected layer’, is a layer in which each neuron is connected with all the neurons from the previous layer with a specific weight $w_{ij}$. The input vector is mapped to the output vector in a nonlinear manner by the dense layer, due to the participation of a non-linear activation function. Dense layers can be combined to form a Multi-Layer Perceptron (MLP), which is a class of a feed-forward deep NN.

$^{3}$Note that a half adder is equivalent to 1 AND gate + 1 XOR gate, and a full adder is equal to 2 AND gates + 2 XOR gates + 1 OR gate.
where \( n \) is the number of features in the input vector and \( n_w \) represents the number of neurons in the layer, we can readily see that the RM of a dense layer can be computed according to the simple well-known formula:

\[
\text{RM}_{\text{Dense}} = n_n n_i.
\]

Finally, the bitwidth of the resulting number is truncated to \( b_u \), where \( b_u \) is the bitwidth of the activation function [16].

When calculating the BOP for a dense layer, the costs of both multiplications and additions need to be included. Then, the BOP formula takes the form of the sum of two constituents, \( \text{BOP}_{\text{Mul}} \) and \( \text{BOP}_{\text{Bias}} \), corresponding to vector-matrix multiplication and bias addition:

\[
\text{BOP}_{\text{Mul}} = n_n [n_i b_u b_i + (n_i - 1)(b_u + b_i + \lceil \log_2(n_i) \rceil)],
\]

\[
\text{BOP}_{\text{Bias}} = n_u (b_u + b_i + \lceil \log_2(n_i) \rceil).
\]

Eq. (5) shows the cost of the number of one-bit full adders calculated from the dot product of \( n_i \)-dimensional input vector and weight matrix, as in Refs. [21], [48]. The cost takes into account the bitwidths of the weights and input, \( b_w \) and \( b_i \). To compute the product of the two operands, we have to use \( n_i n_w \) multiplications and \( n_u (n_i - 1) \) additions. The multiplication cost can be calculated by the number of multiplications multiplied by \( b_w b_i \), which is related to the bit operation, and the number of additions multiplied by the accumulator bitwidth required to do the operation. The final BOP is the contribution of multiplication and the addition of bias of the dense layer. For the convenience of the forthcoming presentation, let us define the short notations:

\[
\text{Mult}(n_i, b_w, b_i) = n_i b_u b_i + (n_i - 1)(b_u + b_i + \lceil \log_2(n_i) \rceil),
\]

and

\[
\text{Acc}(n_i, b_w, b_i) = b_u + b_i + \lceil \log_2(n_i) \rceil.
\]

The Acc expression represents the actual bitwidth of the accumulator required for MAC operation, as shown in Fig. 2. Then, the BOP of the dense layer expressed through the layer parameters becomes:

\[
\text{BOP}_{\text{Dense}} = \text{BOP}_{\text{Mul}} + \text{BOP}_{\text{Bias}}
\]

\[
\approx n_n n_i [b_u b_i + (b_u + b_i + \lceil \log_2(n_i) \rceil)]
\]

\[
\approx n_n n_i [b_u b_i + \text{Acc}(n_i, b_w, b_i)].
\]

Now, we note that with the advancement in NN quantization techniques, there arises the opportunity to approximate multiplication by using shift and few add operations only while still maintaining a good processing accuracy, since the NNs can diminish the approximation error that the quantized approximation introduces [43], [49]. As mentioned in Sec. II, the number of shifts can be neglected compared to the contribution of adders. The number of adders is different for different types of quantization. To be more specific, let \( X \) represent the number of adders required, at most, to perform the multiplication and let \( b \) be the bitwidth of the quantized matrix. For uniform quantization, we have: \( X = b - 1 \). And, for example, when the weight matrix with bitwidth of \( b_w \), is quantized, we have \( X_w = b_w - 1 \) as the number of adders we need at most to perform the multiplication of the weights.
In the case of Power-of two (PoT) quantization, we have: $X = 0$, because each multiplication costs just a shift $[42, 53]$. Lastly, for the Additive Powers-of-Two (APoT) quantization, we have: $X = n$, where $n$ denotes the number of additive terms. In APoT, the sum of $n$ PoT terms is used to represent each quantization level $[38]$. Eventually, the NABS of a dense layer can be derived from its BOP equation, Eq. (7):

$$\text{NABS}_{\text{Dense}} \approx n_n n_i \left[ X_w \text{Acc}(n_i, b_w, b_i) + \text{Acc}(n_i, b_w, b_i) \right]$$

$$\approx n_n n_i (X_w + 1) \text{Acc}(n_i, b_w, b_i).$$

(8)

As in Eq. (8), the multiplication term $b_w b_i$ in Eq. (7) is converted into the number of adders needed to operate the multiplication times the accumulator bitwidth required: $X_w \text{Acc}(n_i, b_w, b_i)$.

**B. Convolutional Neural Networks**

In CNN, we apply the convolutions with different filters to extract the features and convert them into a lower-dimensional feature set, but still preserve the original properties. CNNs can be used in 1D, 2D, or 3D networks depending on the applications. In this paper, we focus on 1D-CNNs, which are applicable to processing sequential data $[3]$. For simplicity of understanding, the 1D-CNN processing with padding equal to 0, dilation equal to 1, and stride equal to 1, can be summarized as follows:

$$y_i^f = \phi \left( \sum_{n=1}^{n_k} \sum_{j=1}^{r} x_{i+j-1,n} \cdot b_{j,n}^f + b_f \right),$$

(9)

where $y_i^f$ denotes the output, known as a feature map, of a convolutional layer built by the filter $f$ in the $i$-th input element, $n_k$ is the kernel size, $n_i$ is the size of the input vector, $x_{i,n}$ represents the raw input data, $b_{j,n}^f$ denotes the $j$-th trainable convolution kernel of the filter $f$ and $b_f$ is the bias of the filter $f$.

In the general case, when designing the CNN, the parameters like padding, dilation, and stride also affect the output size of the CNN. It can be formulated as:

$$\text{OutputSize} = \left[ \frac{n_s + 2 \text{padding} - \text{dilation}(n_k - 1) - 1}{\text{stride}} + 1 \right],$$

(10)

where $n_s$ is the input time sequence size.

The RM of a 1D-convolutional layer can be computed as follows:

$$\text{RM}_{\text{CNN}} = n_f n_n k \cdot \text{OutputSize},$$

(11)

where $n_f$ is the number of filters, also known as the output dimension. As in Eq. (11), there are $n_n n_k$ multiplications per sliding window, and the number of times that sliding window process needs to be repeated is equal to the output size. Then, the procedure is executed repeatedly for all $n_f$ filters.

The BOP for a 1D-convolutional layer, after taking into consideration the multiplications and additions, can be represented as:

$$\text{BOP}_{\text{CNN}} = \text{OutputSize} \cdot n_f \text{Mult}(n_i n_k, b_w, b_i) + n_f \text{Acc}(n_i n_k, b_w, b_i).$$

(12)
Eq. (12) is derived from Eq. (9) and Eq. (11). The first term is associated with the convolution operation between the flattened input vector and the sliding windows, and the latter term corresponds to the addition of the bias.

The procedure to derive the NABS is similar to that described in details in the case of a dense layer, Sec. III-A. The NABS of a 1D-convolutional layer is given by:

$$\text{NABS}_{\text{CNN}} = \text{OutputSize} \cdot n_f \left[ n_h n_k (X_w + 1) - 1 \right] \cdot \text{Acc}(n, n_k, b_w, b_i) + n_f \text{Acc}(n, n_k, b_w, b_i).$$

(13)

To obtain the 1D-convolutional layer’s NABS, the multiplication in Eq. (12) is represented by the number of adders required, at most, to perform the multiplication times the accumulator bitwidth.

C. Vanilla Recurrent Neural Networks

Vanilla RNN is different from MLP and CNN in terms of its ability to handle the memory, which is quite beneficial for time series data. RNNs take into account the current input and the output that the network has learned from the prior input. Even though the RNNs introduced the efficient memory handling, it still suffers from the inability to capture the long-term dependencies because of the vanishing gradient issue [54]. The equations for the vanilla RNN given a time step $t$ are as follows:

$$h_t = \phi(W x_t + U h_{t-1} + b),$$

(14)

where $\phi$ is, again, the nonlinear activation functions, $x_t \in \mathbb{R}^{n_x}$ is the $n_x$-dimensional input vector at time $t$, $h_t \in \mathbb{R}^{n_h}$ is a hidden layer vector of the current state with size $n_h$, $W \in \mathbb{R}^{n_h \times n_x}$ and $U \in \mathbb{R}^{n_h \times n_h}$ represent the trainable weight matrices, and $b$ is the bias vector. For more explanations on the vanilla RNN operation, see Ref. [55]. The RM of a vanilla RNN is:

$$\text{RM}_{\text{RNN}} = n_s n_h (n_i + n_h),$$

(15)

where $n_h$ notes the number of hidden units. From Eq. (15), the RM for a time step is $n_h (n_i + n_h)$. It can be separated into two terms; the $n_h n_i$ term corresponds to the multiplication of the input vector $x_t$ and the weight matrix, and the $n_h^2$ term arises because of the multiplication to the prior cell output $h_{t-1}$. Finally, $n_s$, which denotes the number of time steps in the layer, should be taken into account, as the process is repeated $n_s$ times.

The BOP for a vanilla RNN is given as:

$$\text{BOP}_{\text{RNN}} = n_s n_h \text{Mult}(n_i, b_w, b_i) + n_s n_h \text{Mult}(n_h, b_w, b_h) + 2n_s n_h \text{Acc}(n_h, b_w, b_a).$$

(16)

From Eq. (16), the first term is associated with the input vector multiplied by the weight matrix, and the second term corresponds to the multiplications of the recurrent cell outputs. The final term is the contribution of the addition between $W x_t + U h_{t-1}$ and the addition of the bias vector in Eq. 14; one can see that the size of the accumulator used in this term is $\text{Acc}(n_h, b_w, b_a)$. It is due to the assumption that $\text{Acc}(n_h, b_w, b_a)$ is dominant because it should be greater than $\text{Acc}(n_i, b_w, b_i)$ as a result of the inequality $n_h > n_i$.

As in the case of a dense layer, the NABS of vanilla RNN can be calculated from its BOP equation by converting the multiplication to the number of adders needed at most ($X$) depending on the quantization scheme and the accumulator size:

$$\text{NABS}_{\text{RNN}} = n_s n_h [n_i (X_w + 1) - 1] \text{Acc}(n_i, b_w, b_i) + n_s n_h [n_h (X_w + 1) + 1] \text{Acc}(n_h, b_w, b_a).$$

(17)

D. Long Short-Term Memory Neural Networks

LSTM are an advanced type of RNNs. Although RNNs suffer from short-term memory issues, the LSTM network has the ability to learn long-term dependencies between time steps ($t$), insofar as it was specifically designed to address the gradient issues encountered in RNNs [56, 57]. There are three types of gates in an LSTM cell: an input gate ($i_t$), a forget gate ($f_t$), and an output gate ($o_t$). More importantly, the cell state vector ($C_t$) was proposed as a long-term memory to aggregate the relevant information throughout the time steps. The equations for the forward pass of the LSTM cell given a time step $t$ are as follows:

$$i_t = \sigma(W^i x_t + U^i h_{t-1} + b^i),$$

$$f_t = \sigma(W^f x_t + U^f h_{t-1} + b^f),$$

$$o_t = \sigma(W^o x_t + U^o h_{t-1} + b^o),$$

$$C_t = f_t \odot C_{t-1} + i_t \odot \phi(W^c x_t + U^c h_{t-1} + b^c),$$

$$h_t = o_t \odot \phi(C_t),$$

(18)

where $\phi$ is usually the “tanh” activation functions, $\sigma$ is usually the sigmoid activation function, the sizes of each variable are $x_t \in \mathbb{R}^{n_x}$, $f_t, i_t, o_t \in (0, 1)^{n_h}$, $C_t \in \mathbb{R}^{n_h}$ and $h_t \in (-1, 1)^{n_h}$. The $\odot$ symbol represents the element-wise (Hadamard) multiplication.

The RM of a LSTM layer is:

$$\text{RM}_{\text{LSTM}} = n_s n_h (4 n_i + 4 n_h + 3),$$

(19)

where $n_h$ is the number of hidden units in the LSTM cell. Similarly to RNNs, the RM can be calculated from the term associated with the input vector $x_t$ and the term corresponding to the prior cell output $h_{t-1}$; however, each term occurs four times, as we can see in Eq. (18). Therefore, we have $4n_h n_i$ and $4n_h^2$, respectively. Moreover, we also need to include the element-wise product that is operated three times in Eq. (18), which costs $3n_h$. Finally, the process is repeated $n_s$ times, hence, $n_s$ is multiplied to the overall number.

The BOP for a LSTM layer is computed based on Eq. (19), but also includes the bitwidth of the operands and the number of additions. As a result, the BOP can be represented as:

$$\text{BOP}_{\text{LSTM}} = 4n_s n_h \text{Mult}(n_i, b_w, b_i) + 4n_s n_h \text{Mult}(n_h, b_w, b_h) + 3n_s n_h b^2 + 9n_s n_h \text{Acc}(n_h, b_w, b_o).$$

(20)

To give more details on the expression, the first two terms in Eq. (20) are the contribution of the input vector multiplications
and the recurrent cell output association, respectively. The term \( 3n_s n_b b_a^2 \) refers to 3 times of the element-wise product of two operands with \( b_a \) bitwidth, see Eq. (13). For each time step, there are \( n_h \) elements in each vector needed to be multiplied. The last term is for all the additions, since we assume that \( \text{Acc}(n_h, b_w, b_a) \) gives the dominant contribution, as described in Sec. III-C. Finally, the process is then restarted \( n_s \) times.

The NABS of a LSTM layer is derived from the Eq. (20) by replacing the multiplications with the shifts and adders including their cost, as mentioned in Sec. III that the shifts would not be included. The number of adders depends on the quantization technique. The NABS would be as follows:

\[
\text{NABS}_{\text{LSTM}} = 4n_s n_h \left[ n_i (X_w + 1) - 1 \right] \text{Acc}(n_i, b_w, b_i) \\
+ 4n_s n_h \left[ n_h (X_w + 1) + 1 \right] \text{Acc}(n_h, b_w, b_a) \\
+ 6n_s n_h b_a. 
\]

The first and second terms are the results of input vector multiplications and the recurrent cell operation combined with all addition operations, respectively. In this case, the third term comes from \( 3n_s n_h(b_a + b_a) \). Due to the element-wise product of two operands with bitwidth \( b_a \), the resulting bitwidth becomes \( b_a + b_a \) as mentioned in Fig. 2.

E. Gated Recurrent Units

Like LSTM, the GRU network was created to overcome the short-term memory issues of RNNs. However, GRU is less complex, as it has only two types of gates: reset \( (r_t) \) and update \( (z_t) \) gates. The reset gate is used for short-term memory, whereas the update gate is responsible for long-term memory [58]. In addition, the candidate hidden state \( (h'_t) \) is also introduced to state how relevant the previous hidden state is to the candidate state. The GRU for a time step \( t \) can be formalized as:

\[
\begin{align*}
    z_t &= \sigma(W^z x_t + U^z h_{t-1} + b^z), \\
    r_t &= \sigma(W^r x_t + U^r h_{t-1} + b^r), \\
    h'_t &= \phi(W^h x_t + r_t \odot U^h h_{t-1} + b^h), \\
    h_t &= z_t \odot h_{t-1} + (1 - z_t) \odot h'_t,
\end{align*}
\]

where \( \phi \) is the typical “tanh” activation function and the rest of designations are the same as in Eq. (18).

The RM of the GRU is calculated in the same way as we did for the LSTM in Eq. (19), but the number of operations with the input vector \( x_t \) and with the previous cell output \( h_{t-1} \) is reduced from four (LSTM) to three times as shown in Eq. (22). Thus, the expression for the RM becomes:

\[
\text{RM}_{\text{GRU}} = n_s n_h (3n_i + 3n_h + 3). 
\]

The BOP for the GRU can be calculated in the same manner as we did for the LSTM in Eq. (20). However, now the expression is slightly different in the number of matrix multiplications as the number of gates is now lower. The BOP number can be represented as:

\[
\begin{align*}
    \text{BOP}_{\text{GRU}} &= 3n_h n_b \text{Mult}(n_i, b_w, b_i) \\
    &+ 3n_s n_h \text{Mult}(n_h, b_w, b_a) \\
    &+ 3n_s n_h b_a^2 \\
    &+ 8n_s n_h \text{Acc}(n_h, b_w, b_a). 
\end{align*}
\]

The explanation for each line here is identical to that in Eq. (20).

The NABS of the GRU is derived similarly to the LSTM case:

\[
\begin{align*}
    \text{NABS}_{\text{GRU}} &= 3n_s n_h \left[ n_i (X_w + 1) - 1 \right] \text{Acc}(n_i, b_w, b_i) \\
    &+ n_s n_h \left[ 3n_h (X_w + 1) + 5 \right] \text{Acc}(n_h, b_w, b_a) \\
    &+ 6n_s n_h b_a. 
\end{align*}
\]

Again, the explanation for each term in this expression is identical to Eq. (21).

F. Echo State Networks

ESN belongs to the class of recurrent layers, but more specifically, to the reservoir computing category. ESN was proposed to relax the training process, while being efficient and simple to implement. The ESN comprises three layers: an input layer, a recurrent layer, known as a reservoir, and an output layer, which is the only layer that is trainable. The reservoir with random weight assignment is used to replace back-propagation in traditional NNs to reduce the computational complexity of training [59]. We notice that the reservoir of the ESNs can be implemented in two domains: digital and optical [60]. With the optical implementation of the reservoir, the computational complexity dramatically falls, however, the degradation of the performance due to the change of domain is noticeable [61]. In this work, we only examine the digital domain implementation. Moreover, we focus on the leaky-ESN, as it is believed to often outperform standard ESNs and is more flexible due to time-scale phenomena [62, 63].

The equations of the leaky-ESN for a certain time step \( t \) are given as:

\[
\begin{align*}
    a_t &= \phi \left( W^r s_{t-1} + W^{in} x_t \right), \\
    s_t &= (1 - \mu) s_{t-1} + \mu a_t, \\
    y_t &= W^o s_t + b^o,
\end{align*}
\]

where \( s_t \) represents the state of the reservoir at time \( t \), \( W^r \) denotes the weight of the reservoir with the sparsity parameter \( s_p \), \( W^{in} \) is the weight matrix that shows the connection between the input layer and the hidden layer, \( \mu \) is the leaky rate, \( W^o \) denotes the trained output weight matrix, and \( y_t \) is the output vector.

The RM of an ESN is given by

\[
\text{RM}_{\text{ESN}} = n_s N_r (n_i + N_r s_p + 2 + n_o),
\]

where \( N_r \) is the number of internal hidden neuron units of the reservoir and \( n_o \) denotes the number of output neurons. From Eq. (29), the \( N_r n_i \) multiplications occur from the input vector operations, and the term \( N_r^2 s_p \) is included due to the reservoir layer; to be more specific, the latter term is multiplied with the sparsity parameter \( s_p \) which indicates the ratio of zero values in the matrix. Eq. (27) results in \( 2N_r \) multiplications. Unlike the other network types, now we have to include the contribution of the output layer explicitly because it contains the trainable weight matrix, and this layer contributes \( N_r n_o \) multiplications. Eventually, the process is repeated for \( n_s \) times.
TABLE III: Summary of the three computational complexity metrics per layer (the number of real multiplications, the number of bit operations, the number of additions and bit shifts) for a zoo of neural network layers as a function of their design hyper-parameters: the number of neurons \((n_u)\), the number of features in the input vector \((n_i)\), the number of filters \((n_f)\), the kernel size \((n_k)\), the input time sequence size \((n_h)\), the number of hidden units \((n_h)\), the number of internal hidden neuron units of the reservoir \((N_r)\), sparsity parameter \((s_p)\), the number of output neurons \((n_o)\), weight bitwidth \((b_w)\), input bitwidth \((b_i)\), activation bitwidth \((b_a)\) and the number of adders required at most to represent the multiplication \((X_w)\).

| Network type | Real multiplications (RM) | Number of bit-operations (BOP) | Number of additions and bit shifts (NABS) |
|--------------|---------------------------|---------------------------------|------------------------------------------|
| MLP          | \(n_u n_i\)               | \(n_u n_i [b_w b_i + \operatorname{Acc}(n_s b_w b_a)]\) | \(n_u n_i [X_w + 1] \operatorname{Acc}(n_s b_w b_a)\) |
| 1D-CNN       | \(n_f n_h n_k \cdot \text{OutputSize}\) | \(\text{OutputSize} \cdot n_f \operatorname{Mult}(n_f n_x b_w b_i) + n_f \operatorname{Acc}(n_s n_k b_w b_a)\) | \(\text{OutputSize} \cdot n_f [n_s n_k (X_w + 1) - 1] \operatorname{Acc}(n_s b_w b_a)\) + \(n_f \operatorname{Acc}(n_s n_k b_w b_a)\) |
| Vanilla RNN  | \(n_s n_h (n_i + n_h)\)  | \(n_s n_h \operatorname{Mult}(n_s b_w b_i) + 3 n_s n_h b_a^2\) + \(n_s n_h \operatorname{Acc}(n_s b_w b_a)\) | \(n_s n_h \operatorname{Acc}(n_s b_w b_a)\) + \(n_s n_h (X_w + 1) \operatorname{Acc}(n_s b_w b_a)\) + \(6 n_s n_h b_a\) |
| LSTM         | \(n_s n_h (4 n_i + 4 n_h + 3)\) | \(4 n_s n_h \operatorname{Mult}(n_s b_w b_i) + 4 n_s n_h \operatorname{Mult}(n_s b_w b_a) + 3 n_s n_h b_a^2\) + \(9 n_s n_h \operatorname{Acc}(n_s b_w b_a)\) | \(4 n_s n_h \operatorname{Acc}(n_s b_w b_a)\) + \(4 n_s n_h (X_w + 1) \operatorname{Acc}(n_s b_w b_a)\) + \(6 n_s n_h b_a\) |
| GRU          | \(n_s n_h (3 n_i + 3 n_h + 3)\) | \(3 n_s n_h \operatorname{Mult}(n_s b_w b_i) + 3 n_s n_h b_a^2\) + \(8 n_s n_h \operatorname{Acc}(n_s b_w b_a)\) | \(3 n_s n_h \operatorname{Acc}(n_s b_w b_a)\) + \(3 n_s n_h (X_w + 1) + 5 \operatorname{Acc}(n_s b_w b_a)\) + \(6 n_s n_h b_a\) |
| ESN          | \(n_s N_r (n_i + N_r s_p + 2 + n_o)\) | \(n_s N_r \operatorname{Mult}(n_s b_w b_i) + n_s N_r s_p \operatorname{Mult}(N_r b_w b_a) + n_s N_r \operatorname{Mult}(n_o b_w b_a) + 2 n_s N_r b_a^2\) + \(4 n_s N_r \operatorname{Acc}(N_r b_w b_a)\) | \(n_s N_r \operatorname{Acc}(N_r b_w b_a)\) + \(n_s N_r [s_p (N_r X_w + N_r - 1) + 4 \operatorname{Acc}(N_r b_w b_a) + n_s N_r (X_w + 1) - 1 \operatorname{Acc}(n_o b_w b_a) + 4 n_s N_r b_a\) |

The BOP number for an ESN can be represented as:

\[
\text{BOP}_{\text{ESN}} = n_s N_r \operatorname{Mult}(n_s b_w b_i) + n_s N_r s_p \operatorname{Mult}(N_r b_w b_a) + n_s N_r \operatorname{Mult}(n_o b_w b_a) + 2 n_s N_r b_a^2 + 4 n_s N_r \operatorname{Acc}(N_r b_w b_a). \tag{30}
\]

In Eq. \(30\), the first term is the input vector contribution, the second one is contributed by the reservoir layer, the third term refers to the output layer multiplications, and the fourth term stems from the multiplications in Eq. \(27\). Eventually, all the addition operations are accounted for by the final term.

The NABS of an ESN, which can be calculated in a similar way as in the LSTM case in Sec. III-D is:

\[
\text{NABS}_{\text{ESN}} = n_s N_r \left[ n_i (X_w + 1) - 1 \right] \operatorname{Acc}(n_i b_w b_i) + n_s N_r [s_p (N_r X_w + N_r - 1) + 4 \operatorname{Acc}(N_r b_w b_a) + n_s N_r \left[ n_o (X_w + 1) - 1 \right] \operatorname{Acc}(n_o b_w b_a) + 4 n_s N_r b_a. \tag{31}
\]

By changing the multiplication terms in Eq. \(30\) to the number of adders required at most, we obtain the ESN’s NABS. The input vector multiplication contributes the first term. The reservoir layer and all the addition operations result in the second term. The third term comes from the output layer of the ESN. The last term is the contribution of Eq. \(27\).

IV. COMPARATIVE ANALYSIS OF THE COMPLEXITIES FOR EACH NN STRUCTURE

The comparison of the complexity in terms of RM is illustrated in Fig. 3 for feed-forward NNs and in Fig. 4 for recurrent networks. In feed-forward networks, we first address the computational complexity for a dense layer. In order to reach over \(2 \times 10^6\) real multiplications, which we use as a threshold (highlighted by a maroon color), we can have up to around 1500 input features \((n_i)\) and 1500 neurons \((n_u)\) which is clearly a high value for a single dense layer. The \(n_u n_i\) term in Eq. \(3\) forms a hyperbolic curve, as can be seen in Fig. 3a. For the 1D-convolutional layer, as predicted by Eq. \(11\) we reach a high complexity (maroon) region using less input features than the dense layer case because now the complexity growth depends on more than 2 variables (e.g. to reach the complexity threshold, the number of time steps \(n_s\) can be set to 275 with the kernel size \(n_k\) equal to 150, and we fixed \(n_i = 100\), \(n_u = 1\), \(padding = 0\), \(dilation = 1\), and \(stride = 1\)). According to the exemplary chosen parameters above, the \(n_k \leq n_s\) condition derived from Eq. \(10\) must be satisfied in order to obtain at least the output size equal to 1; therefore, in Fig. 3b the white region corresponds to unavailable output and the heat-map has a hyperbolic form because only \(n_s\) and \(n_k\) parameters vary and the other parameters are kept constant.

The RNN-based networks apparently have higher complexity than the feed-forward NNs. The vanilla RNN in Fig. 4a shows the least complexity among the RNN-based networks studied, while the LSTM’s complexity growth is the fastest,
which can be seen from the size of the maroon area in Fig. 3. The GRU in Fig. 4 shows slightly lower complexity than the LSTM because it has a lower number of gates in its architecture. If we look at the equations of GRU and LSTM in Table 1, the LSTM has a multiplier of 4 for the \( n_t \) and \( n_h \), whereas for the GRU the multiplier is 3. The ESN with fixed \( n_o = 100 \) and \( s_p = 0.5 \) in Fig. 4 has higher complexity than the vanilla RNN, but less complexity than the GRU, because the ESN by design has a less complex architecture due to the use of the reservoir [64]. For all RNN-based networks, we readily infer that the number of hidden units \( n_h \), or \( N_r \) for the ESN, plays the most crucial role in defining the layer’s computational complexity in terms of RM metric. In Fig. 4 we observe that the top face of all cubes which corresponds to the highest number of \( n_h = 100 \) has the largest maroon areas. In terms of the effect on the complexity behaviour, the second most important quantity is the number of time steps \( n_s \); we can see in Fig. 4 that the right face of the cubes, referring to the highest number of \( n_s = 100 \), has the second-largest maroon areas. Finally, the dimensions of the input vector \( n_i \) have the least impact on the RM, as shown by the left face (\( n_i = 100 \)) of all cubes in Fig. 4 with the smallest maroon areas compared to other faces. See Eqs. (3), (11), (15), (19), (23), and (29) for the exact dependencies.

Furthermore, to highlight the computational complexity trend over those different recurrent layers, we plotted the RM versus the number of hidden units (\( n_h \) for vanilla RNN, LSTM, and GRU, or \( N_r \) in ESN) in a scenario where all other hyper-parameters are constant. Fig. 5a depicts the result of this analysis when \( n_s = 100 \), \( n_i = 100 \) for all networks, and \( n_o = 100 \), \( s_p = 0.5 \) for the ESN. By considering those parameters as fixed, the complexity of all four recurrent layers scales quadratically with the number of hidden units (\( n_h^2 \)), which is traditionally interpreted as having the same \( O(n^2) \). However, Fig. 5a brings an important fact that there are significant differences in the computational complexity in terms of RM between all four recurrent layers. Ultimately, this means that the Big-O notation is not sensitive enough to assess the complexity of the NNs in digital signal processing. We can spot that the LSTM complexity escalates the fastest followed by the GRU, ESN, and RNN, respectively. These differences result mainly from the scaling terms on the \( n_h^2 \) of each RM complexity expression for these layers. Note that for the ESN (Eq. (29)), the complexity increases more steadily, as far as, \( N_r \) is multiplied to the sparsity parameter \( s_p \). Moreover, as noted in Sec. III-F, the reservoir can be implemented in the optical domain, so the complexity can be reduced further at the expense of performance trade-off.

We notice that not only the hyper-parameters like \( n_h \) and \( n_s \), affect the computational complexity, but also the bitwidth or precision of each parameter can impact the complexity when we quantify it in terms of the BOP. The effects produced by bitwidth value of weight \( (b_w) \), input \( (b_i) \), and activation \( (b_a) \) are examined in this study. The full-precision or 32-bit precision can be considered over-redundant because 8-bit or less is often enough to provide comparable performance, as stated by many works in the field [65]–[68]. Here, we did not provide the study of the BOP versus different hyper-parameters and bitwidth, because we believe that this is a straightforward analysis that approximately follows what we already studied with the RM metric. Instead, we focus on answering the following question: which variable bitwidth \( (b_w, b_i, b_a) \) produces the highest saving in the BOP complexity when its precision is reduced? This question can guide the design of a low complexity NN structure by identifying which parameter of the NN is the key to producing the higher saving in complexity. To address this question, we compare the reduction of the BOP when using 8-bit precision versus the 4-bit precision for each parameter \( (b_w, b_i, b_a) \) in different network types; the results of the comparison are shown in Fig. 5b. The bitwidth of the weight matrix \( b_w \) is the most significant parameter to consider when trying to reduce the layer’s complexity, as the BOP
is decreased by around 40% for all network types when we halved the precision of \( b_w \). For the dense and 1D-convolutional layers, the precision for input \( b_i \) is as important as the \( b_w \), while reducing the bitwidth of the bias vector \( b_a \) does not have a noticeable impact on the BOP. In the RNN-based networks, converting from 8-bit to 4-bit precision for \( b_i \) and \( b_a \) shows a nearly equivalent reduction in the BOP, except for the ESN case, where decreasing the \( b_a \) precision results in more reduction in the BOP than when we reduce the \( b_i \) precision.

Lastly, we analyze the NABS metric considering various quantization techniques: uniform, PoT and APoT quantization, as described in Sec. III-A. Note that each technique needs a different number of shifts and adders to perform the multiplication. As mentioned before, the shifts incur no extra cost in hardware implementation; therefore, we focus on evaluating the NABS metric of each layer for certain quantization techniques versus the number of adders required at most to perform the multiplication, denoting it as \( X \). More specifically, if the weight matrix has \( b_w \) as its bitwidth and the uniform quantization is utilized, the number of adders required at most \( (X_w) \) is equal \( b_w - 1 \). In the case of PoT, \( X_w = 0 \), and for APoT, \( X_w \) varies between 1 and \( b_w - 2 \), in this case. Fig. 5c shows the NABS versus \( X_w \) analysis when considering that: \( b_w, b_i, b_a = 8 \) for all networks, \( n_i = 1000 \) and \( n_o = 2000 \) for a dense layer, \( n_i = 100, n_s = 300, n_o = 1, padding = 0, dilation = 1, stride = 1 \) and \( n_k = 100 \) for a 1D-convolutional layer, \( n_i = 100, n_s = 100 \) and \( n_h = 100 \) for all RNN-based networks, and \( n_o = 100, s_p = 0.5 \) for the ESN.

As it is shown in Fig. 5c, for all types of networks, when the PoT quantization is used, the NABS can drop around 8 times lower compared to the NABS when using the uniform quantization. Since APoT is a quantization scheme represented by a sum of PoT terms, APoT provides a smooth transition between PoT and uniform quantization. In various works, PoT was claimed to have very low complexity because the multiplications are replaced by just shifts [53], [69], [70]. However, when we consider that the multiplication in the uniform quantization can be represented by shifts and adders, and we have a fair metric like NABS to compare between different quantization techniques, the NABS when applying PoT is only around an order of magnitude lower than the NABS when using the uniform quantization. To be more specific, even though PoT converts all multipliers into bit shifters, we still have a number of adders coming from the sum operations which are not related to the multipliers, but are they are key for the operational structure of the NN layers. Therefore, the NABS metric can provide a reliable
assessment of the computational complexity of NNs before their implementation in hardware, where the NLG will be the ultimate metric. Note that we intentionally increased the values of the hyper-parameters for the feed-forward NNs in order to compare them in the same graph as the RNN-based networks. For the complexity with regard to NABS, the LSTM apparently needs the highest number of shifts and adders. In conclusion, the three matrices of complexity: the RM, the BOP, and the NABS, have the same trend, meaning that the LSTM requires the most computational resources, followed by the GRU. However, the complexity depends on the particular NN design and can be reduced if we can tolerate a more accurate trade-off: varying the values of hyper-parameters can affect the accuracy, but, simultaneously, work in favour to reduce the computational complexity.

V. Conclusion

In this work, we described the systematic approach for how to evaluate the computational complexity in terms of the three metrics (noticing that the fourth one, the number of logic gates, is hardware dependent and cannot be calculated without referring to a particular setup): the number of real multiplications (RM), the number of bit operations (BOP), and the number of additions and bit shifts (NABS); this itemization implies that we are gradually changing from the software to hardware level. The introduction of such detailed metrics has offered us an opportunity to establish a baseline for the complexity calculation in a more consistent way, depending on the purpose. We investigated the computation of RM, BOP, and NABS in feed-forward and recurrent layers, addressing, namely, a dense layer, a 1D-convolutional layer, a vanilla RNN, LSTM, GRU, and ESN architectures in rather general form.

First, we evaluated the RM metric showing how complexity evolves when changing different hyper-parameters of each NN layer. Specifically, for the recurrent layers, as it was actually expected, the LSTM has the highest complexity among the examined NNs, because of RNN’s architecture featuring different types of gates; moreover, the LSTM complexity grows dramatically with the rise of the number of hidden units. The least complex recurrent architecture is the vanilla RNN. For all recurrent networks, the most complexity-impactful hyper-parameter is the number of hidden units, followed by the number of time steps; the size of the input vector is the least influential. Here, we note that the dense layer is the NN layer type that is the cheapest in terms of complexity, because it is just a matrix multiplication, while all other layers imply a more complex processing procedure.

Our paper also shows the importance of bitwidth (or the precision) for defining the complexity expressed in terms of BOP, i.e. when we descend closer to the hardware level. With the two times reduction in bitwidth, especially in the bitwidth of the weights, the BOP gets drastically reduced, becoming around 40% lower for all types of NNs. This fact shows that when designing the NN solutions, we should prioritize low precision bit in the NN weights to achieve a better reduction in complexity.

Finally, this paper introduces the new metric named NABS to highlight the effects of different quantization techniques: uniform, PoT, and APoT. Different from the other papers claiming that the complexity can be reduced drastically when applying the PoT, our current work shows that by using a fair complexity metric like the NABS, the true complexity (i.e. the NABS metric) gets reduced by only around one order of magnitude when using the PoT compared to the uniform quantization for all NN layers. Thus, we claim that the new metric NABS identifies the true complexity level (or the reduction level) better than the previously used RM or BOP.

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