Effects of COVID-19 on a CMOS fabrication course: An integrated design experience

Seung-Joon Paik1 | A. Bruno Frazier2

1Institute for Electronics & Nanotechnology, Georgia Institute of Technology, Atlanta, Georgia, USA
2School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, Georgia, USA

Correspondence
A. Bruno Frazier, School of Electrical and Computer Engineering, Georgia Institute of Technology, 791 Atlantic Dr. Atlanta, GA 30332, USA.
Email: bruno.frazier@ece.gatech.edu

Abstract
In the CMOS fabrication course described herein, the lecture component provides the theoretical background for semiconductor materials and integrated circuit fabrication processes. The laboratory component provides the hands-on experience required to fabricate and electrically characterize CMOS circuits in a one-semester format. A strong semiconductor device process design thread is achieved in the course by integrating the laboratory experience and process simulation modeling and theoretical calculations. The risks associated with the COVID-19 pandemic have forced significant course modifications. The lecture is switched to a remote learning format, including pre-recorded content and weekly advanced Q&A sessions. The laboratory provides both in-person and remote sessions. Approved social distancing and cleaning protocols are practiced in the facility for in-person learning. Complementary remote learning resources are made available to all the students such as pre-recorded laboratory instructions, live video-based laboratory sessions, and web-based supplementary information. Compared to pre-pandemic semesters, the average students' GPA of the pandemic period has increased, attributed to larger and archived volumes of instructional material. Overall student comments related to course changes necessitated by the pandemic are mixed with both positive and negative feedback.

KEYWORDS
complementary metal oxide semiconductors (CMOS), COVID-19, microfabrication

1 | INTRODUCTION

Microfabrication educational laboratory facilities at institutions for higher learning have been in place for many years. These educational facilities have focused on a variety of end-product technologies including as examples—complementary metal oxide semiconductors (CMOS),1,2 microelectromechanical systems (MEMS),3,4 integrated optical systems,5,6 and nano devices.7 While these educational laboratories have great purpose and meaning, most if not all are technology limited by many of the same factors including physical space and state-of-the-art semiconductor processing equipment costs. For these reasons among others, it is not practical for universities and other institutions to operate these educational facilities on the cutting edge of commercially available technologies for producing electronic circuitry, MEMS, integrated optical systems, etc.

One solution to the dilemma of costs versus facility technologies is to focus the micro-/nanofabrication educational laboratory experience on how to fabricate basic micro-/nano-devices/systems while tying the laboratory experience to the underlying semiconductor physics associated with semiconductor materials and device/system
performance. By using this dual approach, a strong design thread can be introduced into the student learning experience.

In recent semesters, from spring 2020 to present, there have been significant changes to the course described herein forced by the recent COVID-19 societal pandemic. The COVID-19 pandemic resulted in massive changes to the methods used by universities to deliver course content and provide person-to-person interactions related to educational activities. The need for COVID-19-related course modifications has been especially relevant for laboratory-based courses such as a CMOS fabrication course discussed herein.

In this paper, the organization and delivery of a design-based CMOS educational laboratory experience will be discussed. Additionally, changes to the laboratory-based course initiated by the presence of the recent COVID-19 pandemic will be presented and compared to the traditional face-to-face methods of content delivery.

2 | COURSE DESCRIPTION

With a focus on creating a design experience, the CMOS fabrication course has a lecture component and a laboratory component. In the lecture, students are taught the theoretical underpinnings of common microelectronic processes such as photolithography, semiconductor impurity doping processes, deposition processes, and growth processes (see Figure 1). In addition, students are introduced to semiconductor process modeling software for the common microelectronic processes. In the laboratory, the students fabricate MOS devices, common CMOS circuits, and other common integrated components such as resistors, capacitors, and test structures. By practicing hands-on skills during each laboratory session, students learn how to handle wafers, operate machines of the microfabrication processes, and measure process results.

The lecture component of the course provides the theoretical background for all the fabrication processes utilized and characterization data collected in the laboratory. The lecture topics include semiconductor materials basics, theory of common semiconductor fabrication technologies, theory of advanced semiconductor CMOS fabrication technologies, and common semiconductor packaging processes/technologies. Additionally, the lecture covers the theory and operation common of advanced processing technologies beyond those experienced during the CMOS fabrication process such as through-silicon via technologies and microelectromechanical systems using CMOS-relevant fabrication technologies. Finally, the lectures include a modeling component in which simulation software is used to predict the results of CMOS fabrication processes. The simulation software is used as a bridge to help correlate the theoretical principles learned in the lecture and the experimental results gained in the laboratory.

![Figure 1 Process flow for the CMOS fabrication course](image-url)
The laboratory component of the course provides a fabrication experience that allows students to individually process wafers through a CMOS fabrication process flow in a one-semester format. The process flow is shown in Figure 1. The students begin with an n-type silicon wafer and go through a standard CMOS process to fabricate PMOS devices in the bulk silicon material and to fabricate NMOS devices within P-well structures (Figure 2). The first laboratory session starts with characterizations of the n-type silicon substrate such as dopant type and resistivity. Each session accumulates and repeats the microfabrication processes to make the CMOS devices completed. While they are fabricating the devices, the students measure processing data including thicknesses of silicon dioxide layers, sheet resistances of dopant-diffused regions, and junction depths for the p-well, MOS sources, and MOS drains. Afterward, the monolithic devices on the wafers are characterized using a wafer probing system and electrical testing instruments. Throughout the lab sessions, students record processing parameters, visual observations, and characterization results on cleanroom notebooks. A laboratory instructor is closely and actively involved in the sessions and providing one-on-one training on relevant cleanroom equipment, demonstrations on batch processes, and safe handling of chemicals.

A schematic of the layout is shown in Figure 3. As can be seen, the chip layout includes stand-alone PMOS and NMOS devices with gate widths of 2.0, 5.0, 10.0, 20.0, and 40.0 μm; a capacitor; four resistors (one resistor per doping cycle shown in Figure 2); and CMOS circuits including inverters, a ring oscillator, an AND gate, a NAND gate, and a NOR gate. After completion of the CMOS process, the students electrically characterize the devices on the wafer using a classic probe station and common semiconductor analyzer equipment.

Integration of the lecture component and the laboratory component enables a rich CMOS process design experience. Integration of the theoretical and experimental components of the course is accomplished via periodic laboratory reports throughout the semester and the end-of-semester CMOS process design project. As the semester unfolds, the students are challenged to calculate, simulate, and obtain experimental data related to specific material and process characteristics. Further, the students are challenged to investigate the differences in the relevant values obtained from these three sources of data. Students are asked to answer the question, “What is the difference and why is there a difference in the calculated result compared to the simulated result compared to the experimental data?” The specific material and process characteristics explored in the laboratory reports are shown in Table 1. In addition to the laboratory reports, the students complete an end-of-semester design project to further the design experience. The design project is focused on challenging the students to make improvements to the current CMOS fabrication process. The end-of-semester project is based on the post-processing electrical testing and characterization of the devices and circuits shown in Figure 3. The smaller MOS devices on the chip are intentionally designed with channel geometries smaller than the minimum spacing design rule for the fabrication process. Therefore, the smaller MOS devices do not have ideal forward bias characteristics. An example of a common nonideal characteristic for the small MOS devices is lack of a saturation region in the commonly known MOS transistor I–V curve showing the drain current dependence on the source-to-drain voltage and gate voltage. Furthermore, the CMOS circuits do not operate ideally due to mismatches between the PMOS and NMOS transistors. An example of nonideal CMOS operation is the switching voltage of the inverters. Ideally, the inverters are designed to switch at 50% of the supply voltage. If the threshold voltages of the NMOS and PMOS transistors are not matched, then the inverter switching voltage will shift away from the ideal switching voltage. Students are challenged to discover the physical origin of the nonideal MOS device and CMOS circuit characteristics, followed by student recommendations for changes to the
fabrication process to improve device and circuit performance, followed and supported by updated models with simulations demonstrating the students proposed changes to the fabrication process. Integrating the theoretical component and the experimental component of the course through periodic laboratory reports and an end-of-semester design project provides a strong process design thread to the course.

**FIGURE 3** Chip layout and design with passive devices, MOS devices, test devices, and CMOS circuits

| Measured quantity | Physical measurement | Experimental method(s) | Theoretical quantity | Simulated quantity |
|-------------------|----------------------|------------------------|----------------------|-------------------|
| Sheet resistance  | - Bulk silicon       | - 4-point probe        | - Resistivity, $\rho = \rho_s t$ | Average doping concentration |
|                   | - Doped layers after thermal diffusion pre-deposition and drive-in processes | - Van der Pauw structures using Montgomery method at end of process | - Conductance $\rho = \frac{1}{\sigma} = q(\mu_n n + \mu_p p)$ | |
| Junction depth    | Position and movement tracked throughout process for the P-well, PMOS/NMOS source/drain | - Cleave and etch and stain | - Pre-deposition $x_j = 2\sqrt{Dt} \text{erf}^{-1}\left(\frac{C^b}{C_s}\right)$ | Junction depth |
|                   |                      | - Groove and stain     | - Drive-in $x_j^2 = 4Dt \ln\left(\frac{C^b}{C_s}\right)$ and $C_s = \frac{s}{\sqrt{4Dt}}$ | |
| Silicon dioxide thickness | - Field oxide        | - Refractometer        | $t_{ax} = \frac{-A + \sqrt{A^2 + 4B(t+d)}}{2}$ | Silicon dioxide thickness |
|                   | - Gate oxide         | - Ellipsometer         |                      |                   |

Note: Here, $\rho$ = resistivity, ohm·cm; $\rho_s$ = sheet resistance, ohms/square; $\sigma$ = conductivity; $q = 1.6 \times 10^{-19}$ C; $\mu_n$ = electron mobility, cm²/V·sec; $\mu_p$ = hole mobility, cm²/V·sec; $n$ = electron concentration, cm⁻³; $p$ = hole concentration, cm⁻³; $x_j$ = junction depth, µm; $D$ = diffusivity, $t$ = time, seconds; $C_b$ = background concentration, cm⁻³; $C_s$ = surface concentration, cm⁻³; $t_{ax}$ = silicon dioxide thickness, cm; $A$, $B$ & $\tau$ = Deal Grove tabulated values.¹
Significant course modifications were required as a result of the COVID-19 societal pandemic. Prior to the pandemic, the course had two in-person lectures per week and one in-person laboratory session per week. As a result of the pandemic, the lecture component of the course was converted to 100% remote learning, and the laboratory component of the course underwent significant changes as described below.

For the lecture component, the lectures were pre-recorded for asynchronous delivery to the students. Additionally, the two weekly lecture periods were converted to advanced Q&A sessions centered on clarifying difficult lecture content and providing additional examples to augment the pre-recorded lecture content. The changes resulted in a format similar to the well-known flipped classroom approach to course delivery.

With regard to the laboratory component, the Institute for Electronics and Nanotechnology (IEN) of Georgia Institute of Technology (Georgia Tech) initiated modified the protocols surrounding the use and occupancy of the associated cleanroom facilities. The COVID-19 protocols extended to the educational facilities as well. For the CMOS fabrication course, the laboratory sessions of the course were modified to limit the exposure and spread of the viruses by encouraging social distancing and disinfection. The main changes were to limit the maximum number of people in the gowning area and the cleanroom; to provide low- or no-touch dispensing systems of pre-gowning items; and to sanitize personal and shared items. In the IEN’s cleanroom, the allowed occupancy was up to two people in the gowning area and one person in every 36 square footage of the educational facility. No-touch dispensers of hand sanitizer, gloves, and step-on shoe covers have been exploited, and each student’s cleanroom garments were stored separately in a plastic garment bag. To reduce face-to-face encounters in the laboratory area, pre-recorded video materials of laboratory instruction content and laboratory demonstrations were provided in advance. The students could start the fabrication processes after reduced face-to-face instruction time in the laboratory and review step-by-step training procedures from the video clips afterward. The students and the instructor were also encouraged to take a weekly virus surveillance test provided by Georgia Tech.

Physical presence and hands-on practices at the laboratory sessions have been mandatory to the students since the microfabrication processes require the special environment provided by the cleanroom, a safe work area for chemicals, and expensive machines with high accuracy. It is important to keep the microfabrication schedule on time for the completion of the circuit devices and design project at the end of the term. During the pandemic, however, students can choose whether to attend the laboratory sessions in-person or remotely.

During the fall semester in 2020, for example, some students took the course fully remotely, and others attended a few sessions remotely due to quarantine and testing positive for the COVID-19 virus during the semester. Virtual lab sessions enabled by developing online materials and live weekly lab sessions through videoconferencing platforms provided course content for the remotely participating students. The videoconferencing platform enabled live broadcasting and recording of the laboratory sessions, showing all the lab activities such as preparation, machine operation, and data measurement. The online materials included step-by-step instructional slides and pre-recorded video demonstrations. Microfabrication processes such as photolithography, etching, and metallization were recorded and edited in video clips. Each remote lab session was provided with relevant presentation slides and voice recordings of them. All the digital materials were provided by using the Georgia Tech’s CANVAS system so students could access the educational material seamlessly from anywhere and anytime. In addition, IEN supported web pages on the relevant fabrication, characterization, and microelectronic devices were made available to provide supplementary information (Figure 4).

Student performance was measured for three separate offering of the CMOS fabrication course. The average students’ GPA increased when compared to the pre-pandemic course grades. The average pre-pandemic GPA for this senior-level elective course was 3.23 ± 0.12/4.00. The average pandemic period GPA for the course was 3.51 ± 0.13/4.00. The increase in the average student GPA was attributed to an increased availability and an increased volume of instructional materials for the course.

Student feedback was collected over a three-separate offering of the modified CMOS fabrication course. Overall, feedback was mixed with some common positive and negative feedback for the new course delivery methodologies. Common positive student comments were given in regard to the increased availability of course lecture content,
increased clarity of the CMOS fabrication process, and increased instructional support by teaching assistants and instructors. Common negative comments were a decrease in informal course discussions, a decrease in student connectivity to the course, and a lack of in-person interactions.

5 | CONCLUSION

CMOS educational facilities can provide a strong design component to the student educational experience by integrating the theoretical lecture component and the experimental laboratory component. Integration of theory and experimental results provides student insight into the design of CMOS fabrication processes. The rise of the COVID-19 pandemic forced significant changes to the laboratory-based course. The changes included switching the lecture component to remote learning and offering the laboratory component as either in-person or remote learning. To overcome the challenges of remote learning necessitated by the pandemic, the lectures were pre-recorded and made available on the course website; the laboratory sessions content was pre-recorded; live video-based laboratory sessions were offered and recorded; and weekly help sessions were held. Additionally, to overcome the challenges of the pandemic in the laboratory setting, social distancing and extra personal hygiene measures were put into place. Overall, these modifications were considered positive. Moving forward, student feedback on the course will be used to integrate online educational content in an effective and complementary manner with respect to in-person learning. For example, pre-recorded lectures will become the norm and advanced lectures held during in-person course meeting times.

FIGURE 4 Navigation page of the Instructional Center, providing microfabrication information (https://sums.gatech.edu/content/aboutic)
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AUTHOR BIOGRAPHIES

Seung-Joon Paik is a senior research engineer of the Institute for Electronics and Nanotechnology (IEN) at Georgia Institute of Technology. He received his BS, MS, and PhD degrees at the Electrical Engineering and Computer Science in Seoul National University, Seoul, South Korea. Since 2013, he has been a research faculty member at IEN, where he has been managing and coordinating laboratory elements for College of Engineering courses within IEN cleanrooms which provides instructions to students about microfabrication technologies for CMOS and MEMS devices. He has published more than 60 peer-reviewed journal and conference papers and held 13 patents in the United States and South Korea.

A. Bruno Frazier received BS and MS degrees in electrical engineering from Auburn University in 1986 and 1987, respectively, and the PhD degree from Georgia Institute of Technology in 1993, with an emphasis in microelectronics and micromachining technologies. From 1987 to 1990, he was with Intergraph Corporation as a custom circuit designer and advanced packaging engineer. From 1994 to 1995, he was a visiting scholar with the Solid-State Electronics Laboratory, University of Michigan. From 1995 to 1999, he held a joint faculty position as a professor of electrical engineering and bioengineering at the University of Utah. Since 1999, he has been a faculty member with the School of Electrical and Computer Engineering, Georgia Institute of Technology, where he is currently a full professor. He has published work in several areas including advanced packaging technologies, magnetic separation systems, dielectrophoretic separation systems, integrated detection systems for microfluidic separations, integrated analytical systems for neural cultures, and micro-needle technologies.

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