Modified natural frame control of single-phase cascaded H-bridge multilevel converter under distorted grid voltage

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Abstract
Cascaded H-bridge multilevel converter is widely applied in flexible AC transmission and grid connection of renewable energy, but its current quality decreases as the grid voltage distortion continues to deteriorate. A modified natural frame control method to enhance the harmonic elimination ability of converters is proposed in this paper. A single-phase cascaded delayed signal cancellation operator is applied to deal with the distorted grid voltage signals. Benefit from a system structure without any feedback loops or integral items, the transient response of single-phase cascaded delayed signal cancellation operator is faster than commonly-used second-order generalised integrator. The settling time of single-phase cascaded delayed signal cancellation operator facing grid voltage phase jump is less than one grid period. After immunising the synchronisation reference against harmonic distortion by using the single-phase cascaded delayed signal cancellation operator, the modified natural frame control method can then generate high-quality sinusoidal current. Phase-locked loop and coordinate transformation are unnecessary for the proposed method, which decreases the system complexity. Various simulations and experimental tests based on a down-scaled platform demonstrate the performance of the proposed modified natural frame control method under distorted grid voltage.

1 INTRODUCTION

Multilevel converter topologies, such as cascaded H-bridge (CHB), flying capacitor (FC), and neutral-point-clamped (NPC), have been extensively studied over the last decade [1]. Among these multilevel topologies, CHB, which was first presented in 1975, has attracted plenty of attention due to the modularity, extensibility, and reduction of power semiconductors. These advantages make CHB well-suited for medium- and high-voltage applications such as active power filters [2], solid-state transformers [3], static synchronous compensators [4], and photovoltaic inverters [5], among others.

From the perspective of the coordinate frame, the control of pulse width modulation (PWM) converters occurs under the synchronous or the stationary frame [6–8]. Synchronous frame control transforms controlled variables to the equivalent DC terms, therefore, using a proportional-integral (PI) controller is sufficient to track the reference [9]. Controlled variables in stationary frame control are relatively alternating, so a proportional-resonant (PR) controller is necessary to achieve zero steady-state error [10]. These methods exhibit good performance under sinusoidal grid voltage, but still have the following drawbacks:

1. Coordinate transformations are necessary to decouple active and reactive components [6];
2. The grid voltage phase angle is necessary for coordinate transformation. Usually, a phase-locked loop (PLL), which is a typical closed-loop grid synchronisation strategy, is utilised to acquire the phase angle. Facing a complicated power grid, modified PLLs, such as enhanced PLL (EPLL), multiple synchronous reference frame PLL (MSRF-PLL) are proposed. These PLLs make the system complexity to inevitably increase [11], and may even lead to coupling with other control loops;
3. Besides, when applying synchronous frame control to a single-phase system, fictive voltage or current need to be created because a single variable cannot be decoupled via coordinate transformation [7].

Furthermore, the grid voltage is easily distorted because of the increase of nonlinear loads and distributed generators [12]. The PWM converters control under distorted grid voltage dates back to two decades ago [13, 14]. The converter’s actual input current can be divided into two parts according to [15]: one is related to the current reference, the other is related to the grid voltage, which indicates that different solutions may be applied. For instance, modified controllers have been proposed to enhance the precision of the current regulator to the reference [16, 17]. Similarly, some previously proposed methods [18–20] have focused on the construction of advanced feedforward paths to reduce the negative impact of grid voltage.

Among the various modification strategies, the application of advanced filters in grid synchronisation to reduce the influence of distortion during the generation of current reference deserves attention. Figure 1 presents some typical filters applied in grid synchronisation. In classic PLLs, a low-pass filter (LPF) is initially utilised as the loop filter to eliminate double-frequency oscillation [21]. Lowering the cut-off frequency of the LPF can enhance its capacity to remove high-order harmonics, but the system stability will worsen. Similarly, a notch filter (NF) can filter out specified frequency components for synchronisation [22]; however, excessive numbers of NFs may be needed because the grid voltage distortion is always complicated. The second-order generalised integrator (SOGI) is a resonant filter that can extract a specified frequency component. The SOGI-PLL proposed by Ciobotaru [23] is extensively used to deal with distortion. The complex coefficient filter (CCF) applied in [24] is a special band-pass filter (BPF) with a unique polarity-selective property. It can separately deal with positive and negative sequence components. Recently, the moving average filter (MAF) and delayed signal cancellation (DSC) operator, both comb filters, have become increasingly popular because of improved harmonic elimination performance and favourable linear phase feature [25, 26]. Moreover, the inspiration to combine modified filters with numerical optimisation methods continues to attract a significant amount of research interest [27].

In order to eliminate the influence of distorted grid voltage on the single-phase CHB converter, a modified natural frame control (MNFC) method, enhanced by a single-phase cascaded delayed signal cancellation (1 ph-CDSC) operator, is proposed in this paper. Utilising the inherent periodicity and symmetry of sinusoidal signals, the 1 ph-CDSC operator possesses an outstanding ability to eliminate integer harmonics as compared with widely-used SOGI. In addition, the 1 ph-CDSC operator consists of only forward paths and simple arithmetic, which guarantees a fast transient response. Moreover, the structure of 1 ph-CDSC operator can be adjusted flexibly owing to its modularity. The harmonic distortion in the grid voltage is filtered by the 1 ph-CDSC operator. An active voltage unit vector (AVUV) and reactive voltage unit vector (RVUV) are then introduced to support the traditional natural frame control (TNFC) method proposed in previous research [28]. The natural frame control method can overcome the aforementioned drawbacks of synchronous frame control, and reduces the system complexity, thereby making it more suitable for practical applications.

Finally, in the CHB topology, DC-link voltage unbalance easily appears among cascaded chains. The reasons for this could be the discrepancies between the theoretical and actual parameters of devices, limited control accuracy, and different DC-link loads. These problems always lead to differences in the switching delay and power consumption for each H-bridge [29]. As a result, the current quality of the converter will deteriorate, and devices security will be threatened and may even lead to system collapse. Therefore, maintaining the equality and stability of the DC-link voltage is very important. An active component of the grid voltage under the natural frame can be superposed to individual modulation signal to realise DC-link voltage balance efficiently.

The rest of this article is organised as follows. In Section 2, the principles of the 1 ph-CDSC operator and the MNFC method are presented. Section 3 demonstrates the simulation results. Section 4 provides the experimental results. Finally, the conclusions are given in Section 5.

2 | SYSTEM STRUCTURE AND CONTROL STRATEGY

2.1 | Main circuit of the single-phase CHB converter

A three-cell single-phase CHB converter topology is shown in Figure 2, in which \( u \) and \( i \) respectively denote the grid voltage and input current, \( L \) and \( R \) respectively denote the input inductor and its equivalent resistance, \( u \) denotes the output voltage...
of the converter, \(u_{DCi} (i = 1, 2, 3)\) denotes the DC-link voltage of each H-bridge, \(u_{DC}\) is the sum of \(u_{DCi}\). Finally, \(R_i (i = 1, 2, 3)\) denotes the resistance loads of the H-bridge.

### 2.2 Principle of the 1 ph-CDSC

The stationary frame harmonic voltage \(u_{αβ}(t)\) can be expressed as a space vector:

\[
u_{αβ}(t) = U_β e^{jωt + φ_β}\]  

where \(β\) is the harmonic order \((β = 1, 2, 3, \ldots)\), \(U_β\) is the voltage amplitude, \(ω\) is the angular frequency, \(φ_β\) is the initial phase angle of the \(β\)th harmonic.

The stationary frame vector of the fundamental grid voltage rotates counterclockwise at the angular frequency \(ω\), while the vector of the \(β\)th harmonics rotates counterclockwise at the angular frequency \(bω\). Harmonics with different orders have different rotation angular frequencies, so they can be separated by delaying for a specific time.

Delay \(u_{αβ}(t)\) by \(T/n\) to get \(u_{αβ}(t - T/n)\), which can be expressed as:

\[
u_{αβ}(t - \frac{T}{n}) = U_β e^{j(ωt - \frac{T}{n}) + φ_β} = e^{-jφ_β}e^{jω(t - \frac{T}{n})}\]  

where \(T\) represents the grid period, \(n\) is the delay factor, and \(φ_β\) is the angle of the delayed vector \(u_{αβ}(t - T/n)\) lagging the initial vector \(u_{αβ}(t)\), \(φ_β = bωT/n = 2πb/n\).

Multiply a rotation angle \(θ_r\) with the delayed vector obtains the rotated vector. A delayed signal cancellation (DSC) operator can be constructed by the initial vector and rotated vector as follows:

\[
DSC_n \left[ u_{αβ}(t) \right] = \frac{1}{2} \left[ u_{αβ}(t) + e^{-jθ_r}u_{αβ}(t - \frac{T}{n}) \right]
\]

\[
= \frac{1}{2} \left[ u_{αβ}(t) + e^{-jθ_r}u_{αβ}(t) \right] = \frac{1 + e^{-jθ_r}}{2}u_{αβ}(t) = G_{n}u_{αβ}(t)
\]

Define \(G = Ge^{jφ_G}\) as the harmonic gain in Equation (3). According to the vector relationship described in Figure 3, the amplitude \(G\) and phase angle \(φ_G\) of \(G\) are:

\[
\begin{align*}
G & = \left| \frac{\cos \left( \frac{θ_r + φ_β}{2} \right)}{2} \right| \\
φ_G & = - \frac{θ_r + φ_β}{2}
\end{align*}
\]

According to Figure 3 and Equation (4), when \(θ_r = -φ_β\), \(G = 1\) and \(φ_G = 0\), the rotated vector and the initial vector have the same amplitude and the same phase; whereas when \(θ_r = π - φ_β\), \(G = 0\), that is, the magnitude of the rotated vector and the initial vector are equal, and the phases are opposite.

![FIGURE 3 Vector diagram of the delayed signal cancellation module](image)

**TABLE 1** Elimination of harmonics by \(αβDSC_n\)

| Delay factor \(n\) | Arbitrary integer \(k\) | Corresponding eliminable harmonic order \(h\) |
|-------------------|--------------------------|---------------------------------------------|
| 2                 | 0/1/2/3/4/5/6/7/8/9      | 2/4/6/8/10/12/14/16/18/20                  |
| 4                 | 0/1/2/3/4               | 3/7/11/15/19                               |
| 8                 | 0/1                     | 5/13                                       |
| 16                | 0                       | 9                                           |
| 32                | 0                       | 17                                          |

Equation (3) can be rewritten in the time domain as:

\[
DSC_n \left[ u_{αβ}(t) \right] = \frac{1}{2} \left[ u_{αβ}(t) + R(θ_r)u_{αβ}(t - \frac{T}{n}) \right]
\]

The rotation matrix and rotation angle are:

\[
\left[ R(θ_r) \right] = \begin{bmatrix} \cos θ_r & \sin θ_r \\ -\sin θ_r & \cos θ_r \end{bmatrix}
\]

\[
θ_r = -\frac{2πb^r}{n}
\]

In Equation (6), \(b^r\) is a constant determines which order to reserve \((b^r = 1\) here to acquire the fundamental grid voltage to calculate the voltage unit vectors). When voltage order \(b = b^r\), the output remains the same as the input; when with harmonics order \(b = b^r + (2k + 1) n/2\) \((k = 0, ±1, ±2, \ldots)\), \(θ_r = π - φ_β\), these signals suffer zero gain, which means they are eliminated by the DSC operator. Noticing that the harmonic gain amplitude \(G\) is never greater than 1 for any \(b\), it does not enlarge the remaining harmonics. So different DSC operators can be cascaded to construct a cascaded-DSC (CDSC) operator, which is able to eliminate all undesired harmonics stepwise [30].

Table 1 tabulates how harmonics no higher than 20th are eliminated by different stationary frame DSC operators (also known as the \(αβDSC\) operator). Because the value of \(k\) varies, any DSC operator may handle a series of harmonics. An \(αβCDSC_{2,4,8,16,32}\) operator can be constructed by cascading five \(αβDSC\) operators with \(n = 2, 4, 8, 16, 32\). It is able to block all low order harmonics within 20th.

Traditional \(αβDSC\) is proposed in the stationary frame. When applied in a single-phase system, usually a fictive orthogonal signal is necessary. However, treating the input as an
imbalance input, the $\alpha\beta$CDSC$_{2,4,8,16,32}$ can be simplified [26]. Considering the $\beta$-axis input is zero, a DSC$_2$ operator can be removed, and then a DSC$_4$ operator in $\alpha$-axis can be ignored. These modifications of the $\alpha\beta$CDSC operator create a novel 1 ph-CDSC operator which is well-suited for the single-phase system.

As depicted in Figure 4, the 1 ph-CDSC operator only contains time delay submodules and simple arithmetic, and no feedback loops. The input $u_i$ can be any single-phase distorted grid voltage, the outputs are respectively the grid voltage fundamental frequency component $u^*_i$ and its corresponding orthogonal component $\hat{u}^*_i$.

The magnitude and phase responses of the 1 ph-CDSC operator are illustrated in Figure 5 to be compared with widely-used SOGI. Proportional gain (PG) is an important coefficient of SOGI [23]. The value of PG is directly related to its transient response, but inversely to its harmonic elimination capability.

As depicted in Figure 5, the magnitude response of all SOGIs at fundamental frequency ($h = 1$) is 0 dB and the phase shift is 0°, which means that the fundamental component is completely preserved. At other integer harmonic frequencies, the magnitude responses of 1 ph-CDSC are less than −40 dB, indicates that these harmonic components have been reduced by over 100 times. By contrast, even quite a small PG is chosen (PG = 0.3), which brings a slow dynamic, the integer harmonics elimination ability of SOGI is not comparable to that of the 1 ph-CDSC operator.

2.3 Principle of the natural frame control

Independent control of each phase is the most important feature of the TNFC, which gives the entire control system clear physical meaning and reduces control interaction. The power distribution of a system indicates its actual operation state. The system instantaneous active power $p$ can be calculated by the sum of every single-phase instantaneous power:

$$p = e_a i_a + e_b i_b + e_c i_c.$$  \hspace{1cm} (7)

where $e$ is the instantaneous phase voltage, and $i$ is the instantaneous phase current, $a$, $b$, and $c$ are the index of three phases.

$\mathbf{e}_s = (e_a, e_b, e_c)$ can then be defined as the active voltage vector because the dot product of it and the instantaneous current vector $\mathbf{i}_s = (i_a, i_b, i_c)$ represents the instantaneous active power $p$.

Similarly, $\hat{\mathbf{e}}_s = (\hat{e}_a, \hat{e}_b, \hat{e}_c)$, which is the corresponding orthogonal vector of $\mathbf{e}_s$, can be defined as the reactive voltage vector because the dot product of it and $\mathbf{i}_s$ represents the instantaneous reactive power $q$. Figure 6 demonstrates the relationship between the vectors mentioned above. Notably, when applied in a single-phase system, the voltage unit vector contains only single phase parameters.

The preceding analysis is on the premise of a sinusoidal and balanced grid voltage. With harmonics, the vector relationship will be complex, so a pre-filtering stage is needed. Being able to eliminate harmonics and generate orthogonal fundamental component, the proposed 1 ph-CDSC operator is well-suited for natural frame control.

Suppose single-phase voltage $e_a$ is distorted, through the process of 1 ph-CDSC can get the fundamental frequency component $e^*_a$ and its corresponding orthogonal component $\hat{e}^*_a$, and then the AVUV $e_a$ and the RVUV $w_a$ can be calculated by:

$$\begin{bmatrix} e_a \\ w_a \end{bmatrix} = \frac{1}{\sqrt{e_a^2 + \hat{e}_a^2}} \begin{bmatrix} e^*_a \\ \hat{e}^*_a \end{bmatrix}$$  \hspace{1cm} (8)

The voltage unit vectors are then applied in natural frame control to orient, making it possible to regulate active or reactive current independently.
2.4 MNFC of the single-phase CHB converter under distorted grid voltage

As illustrated in Figure 7, the proposed MNFC method is with multiple feedback loops. Two cascaded main feedback loops regulate the DC-link cluster voltage and the input current, and the other feedback loops are applied to achieve DC-link voltage balance.

Grid voltage \( u_s \) may contain different harmonic components, the 1 ph-CDSC operator is able to acquire \( u^*_s \) and \( u^*_a \). The AVUV \( u_a \) and RVUV \( u_d \) can then be calculated via Equation (8).

The outer DC-link cluster voltage loop regulates the total DC side voltage \( u_{DC} \) to the reference \( u^*_{DC} \) by calculating the active current reference \( i^*_p \) with a PI controller, the active component of input current \( i^*_p \) under the natural frame is derived as follows:

\[
 i^*_p = i^*_p u_a 
\]  
(9)

Similarly, the reactive component of input current \( i^*_q \) under the natural frame is derived as follows:

\[
 i^*_q = i^*_q w_a 
\]  
(10)

where \( i^*_q \) is the reactive current reference. Unlike \( i^*_p \), \( i^*_q \) is set by the users of converter directly. When the converter is used as an inverter or rectifier, setting \( i^*_q \) to zero ensures a unit power factor. And if the converter needs to generate reactive current, a positive or negative value can be assigned to \( i^*_q \).

The input current reference \( i^*_a \) is then derived as follows:

\[
 i^*_a = i^*_p + i^*_q 
\]  
(11)

The error between the measured current \( i_a \) and \( i^*_a \) is inputted to the PR controller, generating the basic modulation voltage signal \( u^*_sa \).

The DC-link voltage balance controller diagram is depicted in Figure 7. The errors between each of DC-link voltages \( u_{DC} \) and reference \( u_{DC}/3 \) are input to the corresponding PI controllers, generating DC-link voltage balance active compensations \( \Delta p_1 \), \( \Delta p_2 \), and \( \Delta p_3 \), and then three balance compensation modulation references \( u_{p1} \), \( u_{p2} \), and \( u_{p3} \) can be calculated by:

\[
 \begin{bmatrix}
 u_{p1} \\
 u_{p2} \\
 u_{p3}
 \end{bmatrix} = \begin{bmatrix}
 \Delta p_1 \\
 \Delta p_2 \\
 \Delta p_3
 \end{bmatrix}  
\]  
(12)

Modulation signals for individual H-bridges, denoted as \( u^*_sa \), \( u^*_sb \) and \( u^*_sc \) in Figure 7, are the sum of the basic modulation voltage signal, balance compensation modulation reference, and an optional feed-forward term. Selecting \( u_a \) as the feed-forward term can decrease the negative influence of grid voltage distortion.

A carrier-phase-shifted PWM (CPSPWM) is employed for generating gate signals.

3 SIMULATION RESULTS

The MATLAB R2018a/Simulink software is chosen to run different simulations, testing the performance of the proposed 1 ph-CDSC operator and MNFC method.

3.1 Simulation of MNFC under distorted grid voltage

The main circuit in simulation is as that illustrated in Figure 2, and the control structure is as that presented in Figure 7. The system parameters are exhibited in Table 2. After consulting experimental settings given in some relevant literatures [12, 15, 18], combined with existing experimental conditions, simulated voltage distortion is set to include 2nd, 5th, 7th, and 8th
TABLE 2 Simulation parameters of the system

| Description                         | Symbol | Value   |
|-------------------------------------|--------|---------|
| fundamental grid voltage rms value  | usf    | 90 V    |
| fundamental grid frequency          | f      | 50 Hz   |
| sampling frequency                  | fs     | 12.8 kHz|
| input inductance                    | L      | 3.0 mH  |
| DC-link cluster voltage reference   | u*dc   | 150 V   |
| DC-link capacitance                 | C      | 4700 µF |
| Cluster voltage controller parameter| P, I   | 0.1, 10 |
| Current controller parameter        | P, R, w| 0.2, 300, 6.28 |

Figure 8 presents the simulation results of grid voltage and input current in a steady state when the reference current is set as capacitive. Adding harmonics at 0.7 s, the total harmonic distribution (THD) of us becomes 18.83%, but that of u*s is close to 0 after the 1 ph-CDSC operator is enabled at 0.8 s. The negative influence on the calculation of the voltage unit vector is eliminated. Moreover, the THD of iwd decreases from 14.03% to 2.47%, proving the effectiveness of the proposed MNFC method.

Simulation result under a grid perturbation of voltage phase jump is obtained at 0.86 s, considering that the current is at its peak, the sudden phase jump only causes a small current spike. Taking the zero crossing point of fundamental voltage as reference, the current follows the phase within one grid cycle. During the adjustment process, only small current amplitude fluctuations were produced.

3.2 Comparative simulation of advanced filters facing phase jump

As depicted in Figure 9, facing the signal phase jump, the dynamics of advanced filters are not excellent because the harmonic elimination inevitably takes more time. However, among these strategies, SOGI displays the slowest transient response because it needs a small proportion gain (PG = 0.3) to achieve a qualified harmonic elimination effect which weakens its dynamic badly. The 1 ph-CDSC operator can track the jump within one grid period, better than traditional αβCDSC because a fictive signal is not necessary. The simulation results indicate that 1-ph DSC operator achieves a good balance between harmonics elimination and transient response.

3.3 Simulation of voltage balance control

The same 15 Ω resistance loads are first parallel to the DC-link of the chains. And then the resistance should be varied to test the voltage balance control strategy, one chain changes to 10 Ω, and the other two remain at 15 Ω. These configurations imitate unbalanced loads among chains.

Figure 10 presents the change of the DC-link voltage under different situations with and without balance controllers. As presented in the upper picture, the absence of balance control results in obvious differences between the DC-link voltages. By contrast, as depicted in the lower image, the balance operation is well achieved, as it benefits from the proposed DC-link voltage balance controller.

4 EXPERIMENTAL RESULTS

4.1 Experimental platform

A single-phase three-cell CHB converter based experimental platform is constructed to test the MNFC method. Figure 11(a) is the photo of the experimental platform and its
FIGURE 11 Single-phase three-cell CHB converter experimental platform. (a) Photo of the experimental platform, (b) Structure diagram of the experimental platform

structure diagram is depicted in Figure 11(b). Three INFINIEON F4100R12KS4 single-phase H-bridge modules are cascaded to form a three-cell CHB converter. A single-phase programmable AC source (Chroma 6530) is used as the distorted grid voltage source for the experimental platform.

The MNFC algorithm is implemented in the powerful floating-point DSP (TI TMS320F28377D). Benefit from up to four build-in analogue-to-digital converters (ADCs) and PWM channels with enhanced features, all the voltage and current signals required for calculation and protection can be sampled using build-in ADCs, and the CPSPWM can be easily configured in the DSP. Considering the requirement of the time delay submodule in the 1 ph-CDSC operator, the switching frequency is configured to be the same as sampling frequency, both in 12.8 kHz. Other experimental platform parameters are the same as those in Table 2.

A TEKTRONIX TPS2024 scope is used to acquire the experimental waveforms. A FLUKE 435 power quality analyser is applied to analysis the THD of grid voltage and current.

4.2 Experimental results of the MNFC method under distorted grid voltage

Set the experimental grid voltage THD to 18.83%, and the system configurations are the same as those in the simulation. As shown in Figure 12, facing heavily distorted grid voltage, the TNFC method generates a heavily distorted input current with a THD of over 17%. By contrast, the proposed MNFC method makes the input current become sinusoidal, and its THD decrease to 2.7%, better than common power quality standards 5% in IEC61727 and IEEE 1547.

Notably, under heavily distorted grid voltage, the experimental results cannot be the same as those under sinusoidal grid voltage. A slight distortion is then introduced to test the proposed MNFC method, which is closer to normal working condition. As depicted in Figure 13, the THD of the grid voltage is set to 10%, including 9.38% 3rd, 3.44% 5th, and 1.15% 9th harmonics. The THD of the input current becomes 1.8%, almost the same as that under sinusoidal grid voltage, proving that the negative influence of slightly distorted grid voltage can be perfectly eliminated by the proposed MNFC method. A
perturbation of voltage sag (30%) occurs to test the performance of the proposed control strategy. As shown in Figure 14, the experimental current is still stable during the voltage sag, which indicates the robustness of the MNFC method.

4.3 Comparison with SOGI-PLL based single-phase $dq$ control

For $dq$ control under the synchronous frame, a PLL with advanced filters can also improve the performance when faced with distorted grid voltage. SOGI-PLL is one of the most popular modified PLLs which can be easily applied in $dq$ control [23]. A current reference step change was completed with these two methods to compare the transient response of the SOGI-PLL based $dq$ control with that of the proposed MNFC method. For the sake of fairness, three DC power supplies of the same model replace the DC-link capacitors of the H-bridge, thereby reducing the influence of the outer cluster voltage loop.

Figures 15–16 illustrate that the SOGI-PLL based $dq$ control can also generate a sinusoidal current under the distorted grid voltage. However, the transient responses with the step current reference change are different. As observed in these figures, the MNFC method results in rapid, precise, and smooth system responses. As for the SOGI-PLL based $dq$ control, no matter an active or reactive current step change is set, it cannot track the reference as fast as the MNFC method, and at least a quarter of the grid period is required. This is because that the fictive orthogonal current must be constructed in the SOGI-PLL based single-phase $dq$ control, which always results in current delay.

4.4 Experimental results of voltage balance control

The change of resistance loads emulates a serious DC-link voltage unbalance scenario, which can better verify the proposed voltage balance controller. Figure 17 presents the comparative experimental results between the absence and presence of the proposed DC-link voltage balance controller. Initially, identical 15 $\Omega$ resistance loads are paralleled to three DC-link capacitors, each of the DC-link voltages can stabilise at the reference 50 V. However, as depicted in Figure 17(a), without the balance controller, DC-link voltages diverge when load $R_3$ changes to 10 $\Omega$. The DC-link voltages $u_{dc1}$ and $u_{dc2}$, which resistance loads are larger all increases to 53 V, but the DC-link voltage with smaller load $u_{dc3}$ decreases to 41 V. In Figure 17(b), facing the same load change, all DC-link voltages with the balance controller can stabilise to 50 V after about five grid period. The experimental
results prove the effectiveness of the proposed DC-link voltage balance controller.

5 | CONCLUSION

This paper proposes an MNFC method for single-phase CHB multilevel converter with an advanced 1 ph-CDSC operator. The 1 ph-CDSC operator exhibits not only better elimination of integer harmonics, but also faster transient response to disturbances as compared with extensively used SOGI. Typically, the settling time of 1 ph-CDSC is less than one grid period when faced with grid voltage phase jump. In addition, the 1 ph-CDSC can be adjusted flexibly benefit from its modularity. The effectiveness of the proposed MNFC method in generating sinusoidal current and balancing DC-link voltage under distorted grid voltage is validated by comparative simulations and experiments. As neither PLL nor coordinate transformation is required in the proposed MNFC method, the system complexity is reduced, thereby making it more suitable for practical application.

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DATA AVAILABILITY STATEMENT

Data available on request from the authors.

AUTHOR CONTRIBUTIONS

D.Y.: Conceptualization; investigation; project administration; resources; writing—original draft. S.C.: Formal analysis; methodology; validation; writing—review and editing. X.Z.: Software; validation. L.Y.: Validation; visualization. J.L.: Writing—review and editing. D.S.: Writing—review and editing

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