Co-Designed Architectures for Modular Superconducting Quantum Computers

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ABSTRACT

Noisy, Intermediate Scale Quantum (NISQ) computers have reached the point where they can show the potential for quantum advantage over classical computing. Unfortunately, NISQ machines introduce sufficient noise that even for moderate size quantum circuits the results can be unreliable. We propose a collaboratively designed superconducting quantum computer using a Superconducting Nonlinear Asymmetric Inductive eLement (SNAIL) modulator. The SNAIL modulator is designed by considering both the ideal fundamental qubit gate operation while maximizing the qubit coupling capabilities. First, the SNAIL natively implements √iSWAP gates realized through proportionally scaled pulse lengths. This naturally includes √iSWAP, which provides an advantage over CNOT as a basis gate. Second, the SNAIL enables high-degree couplings that allow rich and highly parallel qubit connection topologies without suffering from frequency crowding. Building on our previously demonstrated SNAIL-based quantum state router we propose a quantum 4-ary tree and a hypercube inspired corral built from interconnected quantum modules. We compare their advantage in data movement based on necessary SWAP gates to the traditional lattice and heavy-hex lattice used in latest commercial quantum computers. We demonstrate the co-design advantage of our SNAIL-based machine with √iSWAP basis gates and rich topologies against CNOT/heavy-hex and FSIM/lattice for 16-20 qubit and extrapolated designs circa 80 qubit architectures. We compare total circuit time and total gate count to understand fidelity for systems dominated by decoherence and control imperfections, respectively. Finally, we provide a gate duration sensitivity study on further decreasing the SNAIL pulse length to realize √iSWAP qubit systems to reduce decoherence times.

1. INTRODUCTION

Quantum Computers (QCs) leverage the physics of quantum information with the promise to change the computing landscape by solving problems that are intractable for classical computers. The ingenuity of QCs comes from quantum superposition and entanglement which, unlike classical computers, allows the QC core computing element, or qubit, to conceptually interact with all other qubits simultaneously. However, to achieve practical quantum-advantage requires fault-tolerance, i.e., passing a threshold of sufficient QC size and fidelity rates to build error-correcting schemes [1]. The field is currently in the the Noisy Intermediate-Scale Quantum (NISQ) era where quantum machines with more than a hundred qubits exist and the fidelities of quantum operations among one or more qubits, typically referred to as gates, above 99.9% are possible, yet remain too small and sensitive to error to perform error-correction [2]. Therefore, NISQ machines are crucially constrained by the duration of the circuits to limit gate noise and qubit decoherence.

NISQ QCs operate by qubit coupling mechanisms which produce different gate operations and neighborhoods of qubit connectivity. Practically, this qubit-qubit coupling arises from a physical connection between them, such as a simple capacitive coupling to a more elaborate nonlinear circuit. We will refer to them generally as modulators, which may target pairs of qubits via layout geometry, unique frequencies or frequency differences, and which, together with applied control signals, govern the fundamental gate operations implemented in the quantum computer. Due to the strict constraints of duration and decoherence, it is necessary to advance the design of modulators to produce high-fidelity qubits and couplings.

The realized potential of quantum computing is furthered when elements of the quantum computing stack, shown in Fig. 1, are designed synergistically. This requires development of the physical mechanisms and modulators, which realize the physical qubits, and the native hardware gates and connectivity topologies, respectively are collaboratively designed with the quantum algorithms we want to implement. Thus, these quantum circuits more successfully execute a quantum program with higher reliability to advance the applicability of NISQ computers.

In this paper we propose a novel co-designed superconducting QC architecture based on a “SNAIL” (Superconducting Nonlinear Asymmetric Inductive eLement) quantum

![Figure 1: Traditional quantum computing stack. The SNAIL allows co-design of rich connectivity topologies and native hardware basis gates for improved basis translation, placement, and routing of important quantum algorithms.](image-url)
2. BACKGROUND AND PRELIMINARIES

In this section we provide some relevant background on quantum computing principles and relevant preliminary statements about co-design methodologies.

2.1 Transmon Qubits

Qubits have been realized from a variety of quantum systems, including atoms, electrons, nuclear spins, etc. In this work we focus on superconducting qubits which are nanofabricated, nonlinear microwave-frequency circuits [9]. The nonlinear element of choice in these circuits is the Josephson junction (JJ), which can be thought of as a non-linear inductor. The most commonly used superconducting qubit is the transmon, which consists simply of a JJ shunted with a large capacitance [10]. The transmon is ubiquitous because it is insensitive to charge and flux noise and can achieve very high coherence [11, 12]. It is also easy to fabricate, control, and couple to other circuit elements [13].

Superconducting qubits are almost always controlled and read out by embedding them in a linear oscillator; this platform of qubit + cavity as the basic unit goes by the name circuit Quantum Electrodynamics or cQED [13].

The cavity is coupled to the qubit dispersively via the “cross-Kerr term” which shifts the mode of the cavity when the qubit gains a photon. This allows for a pulse transiting the cavity to encode the state of the qubit, and is the basis for qubit readout. More, dispersive interactions and cross-Kerr interactions can also be used to couple qubits to each other, to a resonator, or to another nonlinear object, and so are often the physical basis for two qubit gates as well.

2.2 Quantum Gates

Quantum gates are unitary matrix operations that act on quantum state vectors. In general, for NISQ machines single-qubit gates (1Q) and two-qubit gates (2Q) form the building blocks of quantum circuits [14]. A native QC gate set, analogous to a classical computer’s instruction set architecture, defines which unitary operations are available to use on a particular machine. In the same way that NAND and NOR gates are universal digital logic gates, as either gate can implement any boolean logic expression, the requirement for a quantum gate set to be universal is that it can implement any arbitrary unitary to arbitrary accuracy. A basic universal gate set consists of arbitrary single qubit gates plus a single two qubit gate, most often CNOT [15], shown in Eq. 1.

The CNOT gate acts like a classical reversible-XOR gate, with the crucial difference that its inputs can be in superposition. Like many other universal 2Q gates, CNOT is a perfect entangler [16], meaning that it can take a separable state to a maximally entangled state. Entangled states are ones in which we can only describe the state of two qubits jointly and losing information about one qubit destroys information in its entangled partner. A different, potentially more convenient, physical coupling of a QC may result in a different basis gate. For example the family of fractional-$\sqrt{i}$SWAP gates, as in Eq. 2, for which $i$SWAP and $\sqrt{i}$SWAP are also universal gates.

\[
\text{CNOT} = \begin{bmatrix}
1 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 \\
0 & 0 & 0 & 1 \\
0 & 0 & 1 & 0
\end{bmatrix}
\]

\[
\sqrt{i}\text{SWAP} = \begin{bmatrix}
1 & 0 & 0 & 0 \\
0 & \cos(\pi/2n) & i\sin(\pi/2n) & 0 \\
0 & i\sin(\pi/2n) & \cos(\pi/2n) & 0 \\
0 & 0 & 0 & 1
\end{bmatrix} \tag{2}
\]

2.3 Gate Translation and Decomposition

Translating a quantum program between basis gates such as CNOT or $\sqrt{i}$SWAP uses a process called gate decomposition.
Decomposition converts arbitrary unitaries from the quantum program into an equivalent sequence of unitaries only compromised of gates from the basis set of the target system. Note, in the superconducting quantum computers, 1Q gates are generally much faster and higher fidelity than 2Q gates and are often treated as negligible or perfect [17].

Prior work has shown at most only 3 √iSWAP gates plus four interleaved rounds of 1Q gates (given as U₁ to U₆) are required to decompose any 2Q unitary [6], depicted in Eq. 3. Cartan’s KAK is an efficient exact decomposition method that uses geometric relationships between 2Q unitaries to solve for the interleaved 1Q gate values, where intuitively unitary transformations are thought of as movement inside a periodic coordinate basis known as the Weyl Chamber [18]. KAK decomposition shows that many unitaries may in fact be decomposed into only 2 √iSWAP. As similar decomposition is more widely known for CNOT, while a higher proportion of unitaries require 3 CNOTs than 3 √iSWAPs [6].

\[
U = \begin{bmatrix}
U₁ & \sqrt{iSWAP} & U₃ & \sqrt{iSWAP} & U₅ & \sqrt{iSWAP} \\
U₂ & \sqrt{iSWAP} & U₄ & \sqrt{iSWAP} & U₆ & \\
\end{bmatrix}
\]

While it is possible to convert circuits in a CNOT basis into the √iSWAP basis, it is more efficient to decompose the original unitaries of the algorithm directly into the basis gates. CNOT can be realized by 2 √iSWAP. In the best case a unitary can be realized in 2 CNOT. Conversion would require 4 √iSWAP, while direct decomposition would require, at worst, 3 √iSWAP. This is particularly bad for unitaries that require 3 CNOT that can be directly decomposed to 2 √iSWAP, for which conversion would require 6 √iSWAP, making conversion a 1.3–3× increase in 2Q gates over direct decomposition.

When direct decomposition for a basis gate has not been solved, an alternative is to use approximate decomposition using numerical optimization techniques. An optimizer is run to minimize the distance, or variance between the requested 2Q gate and the approximation, on the candidate circuit structure, either by converging on a set of 1Q gate parameters or expanding the circuit template to include more target 2Q gate instances [19]. The primary limitation of numerical decomposition is that for quantum circuits with moderate to large gate counts, it can take orders of magnitude longer time compared to the closed-form substitution rules. Nonetheless, numerical decomposition can be helpful to study new basis gates without needing to mathematically derive analytic decomposition rules for each new 2Q basis gate, such as for the fractional durations √iSWAP gates.

In the next section the coupling neighborhoods, formed from the combination of modulator and physical connections, are described in more detail.

### 2.4 Qubit Coupling and Topologies

To perform both 1Q and 2Q gates, the control signals applied to all qubits and their associated modulators must be unique. For example, in the case of two qubits coupled via a central modulator, a 1Q gate on qubit 1 must operate without creating spurious 2Q gates or drive qubit 2. This is typically accomplished via a combination of (1) spatial selectivity, in which drive lines couple only to a single qubit or modulator and/or (2) frequency selectivity, in which, for example nearest-neighbor qubits have deliberately spaced frequencies to suppress cross-talk among 1Q gates.

Conceptually there is no limit to the density of qubit coupling connections in the neighborhood. In practice, connectivity is limited by these requirements and is typically relatively small, with qubits having 2-4 neighbors and 2-6 couplings.

Accordingly, a graph G = {V, E} is used to represent the organization of the quantum computer where physical qubits form the vertices in V and a coupling capability to perform 2Q gates between qubits are edges in E.

A complicating factor in discussing QC topology is that the choice of gate type and coupling topology are not independent, as they are both determined by the choice of modulator. Thus, in the remainder of this section we will introduce the most common qubit modulators as comparison points.

#### 2.4.1 Cross-resonance gate

The first modulator/gate originally proposed by IBM [20], is the ‘cross-resonance’ (CR) or ZX gate. It utilizes the dispersive cross-Kerr interaction [13] between two qubits to realize a 2Q gate. CR drives the second qubit at the first qubit’s frequency. In the driven frame, the interaction this drive creates couples the Z-component of the first qubit to an X rotation on the second qubit (H = Z₁X₂). This action resembles a CNOT gate but is most often translated into a true CNOT by adding 1Q gates as noted in Eq. 5. In quantum computers the linkage between the two qubits is affected via a third mode [20, 21, 22].

\[
ZX(\theta) = \begin{bmatrix}
\cos \theta / 2 & 0 & -i \sin \theta / 2 & 0 \\
0 & \cos \theta / 2 & 0 & i \sin \theta / 2 \\
-i \sin \theta / 2 & 0 & \cos \theta / 2 & 0 \\
i \sin \theta / 2 & 0 & 0 & \cos \theta / 2
\end{bmatrix}
\]

This gate has successfully realized high fidelities in large systems, and is used throughout IBM’s fleet of QCs. The challenges this gate faces are that: (a) the un-driven cross-Kerr interaction creates Z₁Z₂ errors continuously while off, (b) the qubits should be close in frequency, which does not allow for many-to-many interactions, and (c) given the former, CR gates require very precise fabrication to avoid cross-talk, which has motivated IBM’s shift to more sparsely connected Heavy-Hex architectures [22].

\[
ZX(\frac{\pi}{2}) = \begin{bmatrix}
\begin{array}{c}
S^+ \\
\sqrt{X}^+
\end{array}
\end{bmatrix}
\]

#### 2.4.2 Direct photon exchange: √iSWAP and FSIM gates

Another category of gate is direct photon exchange. This two qubits are coupled resonantly for a period of time to exchange light via the photon-exchange interaction. To form a gate requires turning this interaction on and off. Typically either the qubit frequencies must be tuned together in frequency
to exchange, and then far apart to stop the interaction [23, 24], or by using a ‘tunable coupler’ in between [25]. Direct exchange naturally yields $i\text{SWAP}$-family gates. The exponent of the unitary is determined by the combination of interaction strength and gate duration. The coupler approach has been adopted by Google Quantum AI [7] in their Sycamore (SYC) architecture among other groups [26, 27, 28, 29]. SYC gates accrue a phase on the $|11\rangle$ state in addition to $i\text{SWAP}$, termed FSIM given in Eq. 6. $\theta$ and $\phi$ are determined by the pulses applied to the coupler.

$$\text{FSIM}(\theta, \phi) = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & \cos \theta & -i \sin \theta & 0 \\ 0 & -i \sin \theta & \cos \theta & 0 \\ 0 & 0 & 0 & e^{-i\phi} \end{bmatrix}$$ (6)

SYC sets $\theta = \pi/2, \phi = \pi/6$. The FSIM gate set yields respectable on/off ratios, but suffers from challenges due to: (a) the difficulty of implementing rapid, extremely precise baseband flux control [30] and strong sensitivity to flux noise in these controls [31], (b) the requirement for equal-frequency qubit and concomitant qubit-qubit cross talk issues, and (c) the recent demonstration of strong flux-noise based noise and qubit dephasing in the couplers [32]. $\sqrt{i\text{SWAP}}$ is realized by setting $\theta = -\pi/4, \phi = 0$.

### 2.4.3 Data Movement on the Topology

Movement between physical qubits is accomplished using non-entangling $\text{SWAP}$ gates. $\text{SWAP}$s can be directly decomposed to 3 $\text{CNOT}$s, as well as $3\sqrt{i\text{SWAP}}$, although the latter requires additional 1Q unitaries. A quantum algorithm, represented as a graph $G = (V', E')$, is mapped to hardware topology by embedding $G'$ in $G$ and inducing $\text{SWAP}$ gates when edges cannot be directly realized. As $\text{SWAP}$ gates consist themselves of noisy 2Q hardware gates, it is important to reduce this cost to maximize the overall fidelity of the circuit. Increasing the connectivity in the QC topology will reduce the overhead $\text{SWAP}$ gate cost compared to a sparsely connected graph, similarly impacting fidelity.

### 2.4.4 Common Qubit Topologies

A simple topology that couples qubits to each of their four nearest-neighbors is the Square-Lattice, Fig. 2a, which is regular and straight-forward to expand. IBM’s early Penguin machines attempted higher connectivities with diagonals on alternating tiles of the Square-Lattice, Fig. 2c, with limited success due to issues of frequency crowding at the cost of fidelity. For this reason, IBM has over time reduced the connectivity, moving to a Hex-Lattice, Fig. 2d, and now currently to Heavy-Hex topologies, Fig. 2b [33]. All of these topologies have been demonstrated experimentally with varying degrees of success using FSIM and/or $\text{CR}$ drive protocols.

These topologies are guided by the constraints of two-dimensional circuits whose modulators do not, in general cross each other or span long distances across the chip, despite however beneficial that might be. Instead, a richly connected topology of particular interest in applications of networking and parallel computing is the hypercube, or n-dimension cube. Hypercubes are of particular theoretic interest to qubit coupling topologies because for $2^n$ nodes, both the number of edges incident on every node and the distance between any pair of nodes are exactly $n$, hence scaling regularly and efficiently the neighborhoods of qubit couplings and enforcing $\text{SWAP}$ operations. Implementing such a topology requires us to be able to link a given qubit to $n$ neighbors, which in turn requires a modulator with with this connectivity.

Besides just comparing structural properties of each topology, we demonstrate this experimentally in Section 3.2 to seed our study of the effects of connectivity on computational efficiency. Lattice, Hex-Lattice, and Heavy-Hex topologies and various gates have been examined independently to study the efficiency of routing and decomposition algorithms, respectively [34]. In contrast, we demonstrate the value in considering both gate and topology together to benefit quantum workloads given the state-of-the-art transpilation—i.e., decomposition, placement, routing—algorithms.

### 3. MOTIVATION

To develop a NISQ quantum computer with improved fidelity and scalability there are several factors which lead to the need for collaborative design methodology. First, it is desirable to design a machine that has a target gate type in which it is efficient to map relevant quantum algorithms. Second, it is important to provide a rich and flexible topology to minimize the need for $\text{SWAP}$ gates. From the observations...
in this section we guide the design of our proposed quantum system described in Section 4.

3.1 Normalizing Native Gate Sets

We idealize different physically realizable gates and establish how, with factors such as qubit coherence removed, we might determine whether a basis gate is more computationally useful than another. As previously noted, we treat 1Q gates as negligible.

Unlike classical computing, where the primary concerns are performance and energy consumption, the principal concern for quantum calculation is fidelity of the gates which perform computation. Moreover, infidelity in quantum computers can come from different sources. Some are only present during the gate operation, for example, driving the qubits to unwanted/error states and the imprecision/instability of the control electronics. Other sources of error are always present, for example, the loss of information from bits due to decoherence and energy loss. Common measures of gate fidelity, such as those experimentally determined by randomized benchmarking [35], combine the two together, further confusing the issue. However, if one source of error dominates over the other then the strategy for circuit design must change. Qubits which are idle retain their coherence, and a good figure of merit is just the total number of gates in the circuit [31]. In contrast, if time is the dominant source of error for all qubits in the system, then circuit duration is the best figure of merit, irrespective of the number of gates involved [36, 37, 38]. To address these two scenarios we produce throughout the remainder of the paper two parallel datasets: first, the total gate count, and second, the critical path gate count i.e. total circuit duration, for a given circuit size, topology, algorithm, and basis.

Observation 1. We consider decomposition efficiency of the native basis gates realized by different modulators to predict their relative success. The best choice basis gate is SYC, CNOT, and √1SWAP for FSIM, CR, and SNAIL modulators, respectively. Both CNOT and √1SWAP require at most three instances to implement an arbitrary 2Q gate, whereas the best known analytical decomposition for SYC requires exactly four [39]. In NISQ machines, data movement via SWAP gates can dominate many algorithms which requires three uses of SWAP, CNOT either, or iSWAP. However, for a random distribution of 2Q gates, the SYC achieves this at a total of 53 uses for QFT, it scales comparatively better for critical path SWAPs. On average for an 80-qubit QAOA circuit, Heavy-Hex required 1.92×, 1.53×, and 2.83× critical path SWAPs more than Square-Lattice, Lattice+AltDiagonals, and Hypercube, respectively. This clearly demonstrates the need for richer topologies when scaling QC sizes.

Observation 2. Unsurprisingly, topologies with higher connectivity generally scale better than sparse meshes. However, topologies that prioritize reducing distance everywhere rather than dense neighborhoods of connectivity, i.e. avoiding bottlenecks of data movement, are more tolerant to scaling.

4. QUANTUM CO-DESIGN WITH SNAILS

Based on the observations in the prior section, there are several important factors to consider in the co-design a quantum architecture. From observation 1, we should select a basis gate that minimizes the expected duration for decomposed 2Q gates. From observation 2, we should construct a topology that efficiently scales in diameter while providing rich local connectivity. Collectively, our choice of basis gate should be designed collaboratively with a modulator that allows for increased qubit-qubit coupling neighborhoods.

Next, we propose building a novel quantum architecture using the SNAIL quantum modulator. Using the SNAIL allows natively implementing the √1SWAP family and for a rich qubit couplings without frequency crowding. Additionally, the connectivity of SNAILS introduces the exploration of new topology configurations.

4.1 SNAIL Parametric Modulator

Quantum mechanics describes how a state evolves in time by unitary transformations (gates). The interactions of a system, specified by a Hamiltonian, yield a set of allowed energy eigenstates which determine the time-evolution unitary operator. SNAILS offer a way to control the Hamiltonian of superconducting circuit elements, such that the unitary transformations, i.e., quantum gates, are controlled.

The SNAIL is a flux-tunable device which can, for a certain applied flux, create a strong third-order Hamiltonian term while canceling all 4th and higher even terms. The third-order term allows many discrete coupling frequencies while the fourth-order and higher even terms eliminated in the SNAIL and found in the CR and other modulators create cross-talk interactions which lead to frequency crowding.

Thus the the Hamiltonian of SNAIL can be represented as:

\[ H_{\text{SNAIL}} = h_0 \hat{a} \hat{\sigma}^+ + g_3 (\hat{a}^\dagger \hat{\sigma} + \hat{\sigma}^\dagger \hat{a})^3 \]  

When coupled with other linear objects (e.g., harmonic oscillators) and non-linear objects (e.g., qubits), the total system inherits all possible three-body interaction terms from the SNAIL. For instance, driving at the difference of two qubit resonant frequencies \( \omega_{\text{drive}} = \omega_1 - \omega_2 \) creates the effective interaction:

\[ H_{\text{int}}^{\text{eff}} = g_{12}^\text{eff} (\hat{d}_1^\dagger \hat{d}_2 + \hat{d}_1 \hat{d}_2^\dagger) \]  

The \( \hat{d}_1^\dagger \hat{d}_2 + \hat{d}_1 \hat{d}_2^\dagger \) term creates an iSWAP relationship between qubits 1 and 2 with a rotation intensity governed by \( g \).
If \( g = \frac{\pi}{2} \text{rad} \) the unitary/gate \( U = \sqrt{\text{iSWAP}} \) and follows the transformation matrix:

\[
U(t) = e^{iHt/\hbar} = \begin{bmatrix}
1 & 0 & 0 & 0 \\
0 & \cos(gt) & i\sin(gt) & 0 \\
0 & i\sin(gt) & \cos(gt) & 0 \\
0 & 0 & 0 & 1
\end{bmatrix}
\] (9)

Additionally, a stronger third-order term results in a higher coupling strength \( g \), which is inversely proportional to time. In other words, it gives a stronger pump power with a faster rate of gate, reducing errors due to decoherence loss.

SNAILs are based on the concept of parametric coupling. IBM’s CR modulator uses fixed capacitive coupling and Google’s FSIM modulator uses tunable coupling. The parametric coupling idea of SNAIL modulators has long been used in parametric amplifiers [41, 42, 43], and has recently been used to demonstrate qubit-qubit [44], cavity-cavity [45], and qubit-cavity [46, 47] gates. However, the SNAIL [3] has been designed to increase the frequency difference to several GHz for distinguishing qubit-qubit coupling pairs, which increases their resilience against frequency crowding.

In this system, which gate is produced from driving the SNAIL is controlled strictly by frequency selection; to create an addressable series of gates among many modes each must have a unique difference frequency not shared by another term in the Hamiltonian. Compared to the CR modulator, which requires a strong cross-Kerr term to operate, third-order parametric gates have much smaller cross-Kerr due to static-Z\(_1\)Z\(_2\) interactions. Thus, SNAIL modulators allow operation of multiple gates in parallel in the same neighborhood, or even create three- or more-mode (≥3Q) gates by applying multiple, simultaneous drivers to the SNAIL.

Combined with low frequency crowding, these features of the SNAIL modulator allow flexible, parallel topologies with many to many superconducting qubit interactions, even across modules each with their own SNAILs. Thus, some qubits can participate in multiple modules as topologies scale.

### 4.2 Example SNAIL Quantum Computer

To demonstrate and characterize the capabilities of a superconducting quantum computer using SNAIL modulators, in previous work [4], we constructed a quantum state router and a number of quantum modules with an overall architecture shown in Fig. 5a. In each module, four qubits are directly coupled to the same SNAIL using unique frequency modes allowing \( \sqrt{\text{iSWAP}} \) gates between each qubit pair.

The router is made with a SNAIL chip placed inside a 3D superconducting waveguide. The SNAIL and the TE\(_{10k}\) modes of the waveguide all couple to the SNAIL. Thus all qubits in module \( M_k \) can couple with waveguide mode \( W_k \). \( W_k \) is coupled both to the SNAIL in \( M_k \) as well as the SNAIL in the quantum state router and can form a gate with any element in either the module or quantum state router. In our system \( W_k \) is constructed as a cavity, which has slightly different properties than a qubit, but can still function to build \( \sqrt{\text{iSWAP}} \) gates. Conceptually, \( W_k \) can also be built as a qubit.

Fig. 5b shows our preliminary physical implementation of the “Tree,” only with each module replaced by a simpler design to evaluate the performance of the router independently. In future experiments, an advanced module prototype depicted in Fig. 5c will be coupled to the router, which, together form the Tree architecture as depicted in Fig. 5a. In each module, a SNAIL couples to all qubits for intra-module communication. Then, the modules are connected to the central SNAIL in the router through the piece marked as the waveguide.

Currently, the 4-port state router and 4-qubit module subsystems have been physically realized in two separate experiments. Preliminary results of the router [40] have demonstrated all-to-all exchange interactions among four modules. For 4-qubit module experiment, representative data of one qubit-qubit exchange is shown in Fig. 6, which shows an excitation swapping between qubits when the SNAIL is pumped at different durations and detunings. This figure depicts how
Figure 5: Proposed modular quantum computer with quantum router and module (a) Schematic of one quantum router coupled to four quantum modules. Each module has the same structure as module 4, forming a tree-like architecture. (b) Photograph of the SNAIL based quantum router and four simple modules (adapted from Ref. [40]). (c) Rendered representation and picture of the four qubit SNAIL-based quantum module.

Figure 6: Parametrically driven exchange between two qubits, $Q_2$ and $Q_4$ of the quantum module

gate operations are continuous in time, as we see each qubit oppositely alternating states along the y-axis duration of the gate. Also, it depicts a sense of the fidelity of the operation, as the darker hues represent a purer distribution of measured state outcomes. We have demonstrated that the router is capable of performing iSWAP family gates and can create entanglement between arbitrary qubit pairs from different modules, with an average inter-module gate fidelity of $\sim 97\%$. We have also shown that by keeping the $W_k$ device empty, it is possible to build SWAP gates using a single 1SWAP.

The primary fidelity limit in this device is the ratio of gate time to qubit coherence time [4]. Qubit lifetimes depend on their internal loss which comes from many sources such as loss from the metal package or drive ports as well as through coupling to the SNAIL. One source of decoherence is due to flux-noise, which can detune the SNAIL and cause qubits to dephase. Addressing these challenges requires engineering effort to move from devices created in the lab to industry research products on their way to commercialization. With a similar amount of effort SNAILs can reach pulse speeds and decoherence of other modulators that have received this engineering investment. Thus, to evaluate that core potential and decoherence of other modulators that have received similar amount of effort SNAILs can reach pulse speeds possible to build gates using a single iSWAP...

4.3 SNAIL-based Topologies

Based on the demonstrated prototype quantum computer from Fig. 5, in our new research, we have extrapolated feasible topologies that can be realized using the SNAIL modulator. The basic design is the 20-qubit Tree topology, seen in Fig. 7a. The major difference between this topology and the demonstrated prototype system in Fig. 5a is that central nodes, which are analogs to the $W_k$ elements, are considered to be qubits rather than cavities, as noted previously. However, the standard Tree design contains bottlenecks in the router qubits. Thus, we explore a theoretical alternative design where each qubit in a neighborhood $k$ is connected to each $W_k ... W_l$ in “round robin” fashion. The goal is to eliminate the bottleneck of the $W_k$ qubits, to allow data to move more easily between neighborhoods in parallel. This design, called a “Round Robin Tree” (Tree-RR) decreases the maximum distance between all pairs.

Figure 7: Two-level 4-ary (20-qubit) tree topologies from SNAILs.

We append additional levels, where each module is con-
connected to the following level’s router, to create 84-qubit versions of both the Tree, depicted in Fig. 8 and Tree-RR topologies. For the 84-qubit Tree-RR, each module couples to a different second-level router qubit, and each second-level router qubit is coupled to a different first-level router qubit as shown in Fig. 7b.

As we explored the potential of the hypercube topology in Section 3, we explore topologies enabled by the SNAIL with similar properties. To avoid frequency crowding, a SNAIL can typically interact among as many as six qubits. For our modular design, a module will contain one SNAIL and up to four qubits. SNAILs interact with all qubits in their module. Then to realize larger topologies, qubits link between modules and are coupled with the neighboring module’s SNAIL and qubits. We see this in the Tree, with each module containing four qubits and one SNAIL connected to a shared qubit to cross module boundaries.

Using this constraint, it was desirable to build a topology that maintained the low-diameter property of hypercubes without the required connectivity dimension scaling. Thus we proposed a Corral structure inspired by the 4D hypercube and explored an analog of Tree and Tree-RR for these Corrals. In Fig. 9, red vertical cylinders represent SNAILs and green or yellow horizontal bars are the qubits coupled between them. We call them Corrals due to their resemblance to fence-posts. By building an octagonal ring of modules, each SNAIL with 2 levels of qubits, is defined by a pattern of fence-post connections. Whereas Fig. 9a is the easiest to physically realize, with each qubit coupled to the nearest adjacent SNAIL, denoted Corral1, we might also realize differing strides, which is reminiscent of the hypercube. The Corral1, shown in Fig. 9b creates groups of 4 qubit all-to-all coupling, whereas Corral1,2 shown in Fig. 9c, connects its second fence to the second-nearest neighbor, decreasing the average distance between all pairs of qubits. The resulting topology is shown in Fig. 9d.

Despite initially appearing similar to a ring, we note that the Corral topologies actually exhibit an coupling in neighbors (5 or 6 qubits) analogous to a 4-D hypercube of the same size (4 qubits).

The module from 5c is realized in a 3-dimensional structure. If we define the Corrals as modules with two qubits and a SNAIL, we can also realize these in a 3-dimensional structure resembling Fig. 9a and 9c. For instance, presume each SNAIL (the fence-post) and the two qubits to the right are part of each module. Then the SNAIL from the the right module can also control this module’s qubits, and the SNAIL from this module can also govern the left module’s qubits. Alternatively, we can create heterogeneous modules where one module (mod1) contains a SNAIL and four qubits, and another module (mod2) contains only a SNAIL that forms the boundary between two mod1’s. Thus, Corrals can be scaled by adding more posts (modules) in the ring. However, other approaches could be to combine Corrals with Tree-like modules or to layout Corrals in a lattice pattern.

One benefit of SNAILs is that they isolate the set of distinguishable qubit frequencies in a scope, which is not limited to within a module. Thus, inter-module frequencies have the same fidelity as intra-module frequencies. In the next section we describe our methodology to compare SNAIL-based NISQ QCs with systems using CR (IBM) and FSIM (Google) modulators.

5. EXPERIMENTAL SETUP

To compare the SNAIL-based superconducting quantum computer with machines from IBM and Google we use the metrics for normalization as described in Section 3.1. For simplicity, we presume all gates have uniform fidelity. We explore two sizes of machine. One of the scope for which we have a hardware prototype with 16-20 qubits. These designs are summarized in Table 1. The table includes the number of nodes (qubits), the diameter of the topology (Dia.), the average distance between any two qubits (AvgD), and the average
connectivity of a qubit (AvgC). Tree, Tree-RR, Corral11, and Corral12, are all topologies realizable by the SNAIL. Square-Lattice is included as a baseline and hypercube is included for comparison against the corrals.

Table 1: Topologies and Connectivities

| Topology    | Qubits | Dia. | AvgD | AvgC |
|-------------|--------|------|------|------|
| Heavy-Hex   | 20     | 8.0  | 3.77 | 2.1  |
| Hex-Lattice | 20     | 7.0  | 3.37 | 2.45 |
| Square-Lattice | 16   | 6.0  | 2.5  | 3.0  |
| Tree        | 20     | 3.0  | 2.15 | 4.6  |
| Tree-RR     | 20     | 3.0  | 2.03 | 4.6  |
| Corral11    | 16     | 4.0  | 2.06 | 5.0  |
| Corral12    | 16     | 2.0  | 1.5  | 6.0  |
| Hypercube   | 16     | 4.0  | 2.0  | 4.0  |

We scale the size of the machine to a system with 84 qubits as described in Table 2. The Tree and Tree-RR are expanded with a third level router as described in Section 4.3. We retain the hypercube as a Corral-like design to see the potential of building larger scaled Corrals in addition to scaled Heavy-Hex, Hex-Lattice, Square-Lattice, and Lattice+AltDiag as comparison points. While it is relatively straightforward to remove nodes from the lattice patterns to match 84 nodes, for the Hypercube we must a node from each dimension to reduce the size while maintaining the regular structure.

To generate circuits for these QCs, we extended the Qiskit Terra 0.20.0 transpiler. We provided new backends that support analytical \(\sqrt{\text{SWAP}}\) and SYC decompositions using Cartan’s KAK method. We also extended the transpiler to include the our proposed Tree, Tree-RR, Corrals, Hypercube, and Lattice+AltDiagonals topologies. For design-space exploration we ensure that each basis gate can be assigned to each topology. Note Qiskit already includes an Carton’s KAK CX decomposition backend, as well as Square-, Hex-Lattice, and Heavy-Hex topologies. We use Qiskit’s DenseLayout for initial qubit mapping and StochasticSwap for routing SWAPs.

We tested the machine configurations with workloads that include widely used quantum circuits that can be scaled to different problem sizes. Our parameterized circuits are QuantumVolume, QFT, and CDKM ripple Carry Adder from Qiskit and QAOAAnillaProxy, HamiltonianSimulation, and GHZ from Supermarq [48]. We select these circuit benchmarks over other popular algorithms, such as VQE, because they can be parameterized as a function of qubit size and be generated automatically, while VQE and other similar benchmarks would require hand-coded designs for all problem sizes.

Table 2: Scaled Topologies and Connectivities

| Topology    | Qubits | Dia. | AvgD | AvgC |
|-------------|--------|------|------|------|
| Heavy-Hex   | 84     | 21.0 | 8.47 | 2.26 |
| Hex-Lattice | 84     | 17.0 | 6.95 | 2.71 |
| Square-Lattice | 84 | 17.0 | 6.26 | 3.55 |
| Lattice+AltDiag | 84 | 11.0 | 4.62 | 5.12 |
| Tree        | 84     | 5.0  | 3.91 | 4.71 |
| Tree-RR     | 84     | 5.0  | 3.65 | 4.71 |
| Hypercube   | 84     | 7.0  | 3.32 | 6.0  |

During transpilation (Fig. 10) we collect 4 sets of data over each backend, for each circuit of incremental size. We use Qiskit’s functionality to count total gates and critical path gates. After the routing pass, we count the total induced SWAP and critical path SWAP gates. After the final basis translation pass, we count the total 2Q gates and critical path 2Q gates. Note, we use 2Q basis gate count and its associated pulse duration as a surrogate for determining overall reliability as described in Section 3.1. These experimental settings were used to generate the charts shown in Section 3 as well as the experimental results that we describe next.

6. RESULTS

To evaluate the potential of the SNAIL QCs we explore the impact of the newly possible topologies similarly to Sec. 3, in a gate agnostic fashion, then combine the topology and gate impacts to represent the co-design advantage. Finally, we explore the potential of other basis gates in the \(\sqrt{\text{SWAP}}\) family by investigating fidelity of \(n > 2\) decompositions.

6.1 Evaluation of SNAIL-enabled topologies

We evaluate the proposed SNAIL-coupling corral topologies against the previously discussed topologies, shown in Fig. 11. The scaling of total and critical SWAP gates moderately obeys the expected ordering, as when average connectivity goes up and average distance goes down, less SWAP gates are required. Despite the smaller circuits not quite converging to steady trends, excitingly, the corral topologies are still unambiguously the best performers. Noticeably, the transpiler manages to find an initial mapping that often requires zero SWAP gates for Corral11, an indicator of its rich connectivity.

To extrapolate to larger topologies, we revisit the topologies from Section 3.2, now including the SNAIL topologies Tree and Tree-RR, shown in Fig. 12. Hex-Lattice and Lattice+Diag are not shown for readability and redundancy. This gives us a comparison relating to the previous set of benchmarks. Once again, the constant properties of the topologies appear to generally coincide with performance. In fact, for an 80-qubit QV circuit, we compute from Heavy-Hex to Tree a 54.3% decrease in total SWAP gates or a 79.8% decrease in critical path SWAP gates. However, the Tree designs do not quite match the performance of the hypercube, as from Tree to hypercube experiences an additional 42.5% decrease in total SWAP or 54.3% decrease of critical path SWAP gates.

6.2 Evaluation of Collaborative Design

Next, we continue the decomposition into each topology’s basis gate, in order to count the total number of 2Q gates and the number of 2Q gates in the critical path, i.e. the pulse duration of the circuit, shown in Fig. 13 and Fig. 14. As noted
before, each basis gate is approximately the same with some preference going to $\sqrt{\text{SWAP}}$ over CNOT, and CNOT over SYC, effectively adding a scaling factor enough to bring the SYC gate on Square-Lattice above the C8 gate on Heavy-Hex.

This data also exhibits important principles of parallelism on the topologies, meaning when a curve flattens from total gate count to duration, that means more gates are not contributing to the duration and therefore are in parallel time steps. As an example, the Tree on the QV benchmark flattens its total 2Q gate count onto the duration plot, suggesting a comparatively high degree of gate parallelism. Of particular note, the co-design method shows that the Corral topology combined with the $\sqrt{\text{SWAP}}$ enabled with the SNAIL modulator consistently outperforms all other designs for all benchmarks.

When scaling to larger topologies, Fig. 14 we see interesting trends. Heavy-Hex scales the worst for QV, and the best for QFT, meanwhile, Tree-RR scales the worst for QFT and the best for GHZ. This solidifies the variability of different applications on a topology and should temper excitement about a singular benchmark (even QFT) succeeding on a topology without evidence that other workloads also have positive trends. Interestingly, the hypercube is generally among the best for all benchmarks which lends support to further development of its inspired topologies like Corral. Note, the transpilation placement and routing heuristics appear noisy with some problem sizes more naturally embedding $G'$ into $G$s than others. This may explain why gate counts are not always monotonic on the same topologies and could be a source of inefficient use of more rich topologies.

Thus far we have investigated a set of qubit coupling modulators and both the native gate basis and topology architectures they produce. Most importantly, that Tree topologies make a large improvement in connectivity without needing to sacrifice gate fidelity. We identified decreasing connec-

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**Figure 11:** Total (top) and critical path (bottom) SWAP gates required for 16-qubit implementations of proposed SNAIL topologies.

**Figure 12:** Total (top) and critical path (bottom) SWAP gates required for 84-qubit implementations comparing proposed SNAIL topologies against common topology baseline.
Figure 13: Total (top) and critical path (bottom) 2Q gate counts, decomposed into the respective native basis sets, required for 16-qubit implementations comparing proposed SNAIL topologies against common topology baseline.

Figure 14: Total (top) and critical path (bottom) 2Q gate counts, decomposed into the respective native basis sets, required for 84-qubit implementations comparing proposed SNAIL topologies against common topology baseline.

As previously discussed, using the SNAIL to realize gate couplings yields a $\sqrt{1SWAP}$ family of gates. $\sqrt{1SWAP}$ has been studied as a naturally good candidate for forming a basis, which already decreases the basis gate pulse duration by $\frac{1}{4}$. However, exploring even smaller fractions of $1SWAP$ for decomposition to decrease duration and decoherence time have not been studied. While $\sqrt{1SWAP}$ is the smallest fraction that is a “perfect entangler” [6], decompositions to $\sqrt{1SWAP}$ where $n > 2$ may result in high-fidelity decompositions. However, no analytical decomposition to these gates has been discovered, thus we use an approximate decomposition engine to explore this possibility.

We reproduce a version of NuOp [49] to build template circuits, which interleave the desired $\sqrt{1SWAP}$ gate with 1Q gates (Eq. 10) similar to the exact decomposition method in Section 2.3. However, because the decomposition is approximate, this introduces another form of error beyond decoherence, the error from the decomposition approximation. Thus, the similarity between unitaries, used as the decomposition fidelity is defined using the Hilbert-Schmidt inner product between the template and target from Eq. 11.
However, given our goal is to improve fidelity by reducing decoherence, we also approximate that decoherence scales linearly over time, as shown in Eq. 12. To illustrate, consider an iSWAP some base duration that increases decoherence such that fidelity reduces to 90%. A gate with half the duration has approximately half the decoherence, hence infidelity is reduced from 10%, to 5%, yielding a 95% fidelity from the duration of a√iSWAP gate.

\[ F_b(\sqrt{iSWAP}) = 1 - \frac{1 - F_b(iSWAP)}{n} \]  

As a result, the best total fidelity of the unitary decomposition is the product of the total sum delay of k applications of the basis gate (maxk) and the infidelity of the approximation of each of the k basis gates in the decomposition described in Eq. 13. We ignore the delay of the 1Q gates as in previous decomposition. To study this we generated circuits for the Haar distribution of 2Q unitaries and to find the best total fidelity, we iterate the template size k based on Eq. 13.

\[ F_t = \max_k F_d^{(k)}(F_b)^k \]  

As evidenced by Fig. 15(top left), smaller fractional √iSWAP need more repetitions (larger k) to reach near-exact decompositions, visible by reaching < 10−6 fidelity with higher values of k. However, the savings pulse duration exceeds the larger number of gates, reducing the total pulse duration. For example, given high-fidelity decomposition for √iSWAP in k = 3 and √iSWAP in k = 4, the total duration is reduced from 1.5 to 1.33. This is verified again in Fig. 15(top right), where as n grows, the total pulse duration decreases. Fig. 15(bottom) shows the total fidelity of decoherence and approximate decomposition with decoherence due to iSWAP pulse length on the x-axis and total fidelity on the y-axis. We find that for Haar-randomly sampled 2Q unitaries and for a 99% fidelity iSWAP basis, for k = {3, 4, 5} √iSWAP decreases infidelity by 14%, 25%, and 11%. This evidence continues to support the SNAIL modulator for its realization of a powerful basis set, with the ability to modify duration of the continuous operator to maximize gate fidelities.

7. CONCLUSION

In this work, we demonstrate the data movement overheads and penalties from lattice-based NISQ machines on a range of algorithms. The SNAIL-based modulator and modular architectures provide significant improvements over 2D lattices, particularly for smaller node sizes, whereas a directly scalable 4-ary Tree structure shows mixed performance over the benchmark workloads for larger node sizes. The central node can create bottlenecks for QFT and QAOA which require frequent long-distance connections. However, the Tree performs very well for the Quantum Volume and GHZ-creation tasks due to their rich local connections. We also observe that a hypercube structure, which has rich local connections and low diameter, is superior to both lattices and the Tree and its variants, with exception of the highly ordered GHZ-state creation. We found that on an average of Quantum Volume circuits ranging from 16 to 80 qubits, a hypercube topology induces 2.57× less total SWAP gates and 5.63× less critical path SWAP gates compared to Heavy-Hex. We have explored hypercube inspired ‘Corral’ structures which are both feasible given the demonstrated capabilities of SNAIL modulators for 16 nodes and provide superior computational performance particularly when coupled with √iSWAP (see Fig. 13).

All of our connectivity designs are physically realizable with our demonstrated SNAIL modulators, and represent excellent targets for ours and others’ next-generation quantum computers. Our results point to the need for both dense connectivity and a mix of short- and long-range links in future NISQ machines. Finally, the strong performance of √iSWAP, which is native to the SNAIL modulator, inspired us to explore whether smaller fractions of √iSWAP can yield a superior approximate implementations. We found that for 2Q unitaries and for a 99% fidelity iSWAP basis, √iSWAP decreases infidelity on average by 25% compared to √iSWAP, leading to further co-design advancements.
In future work, determination of analytical decompositions for $\sqrt{\text{SWAP}}$ where $n > 2$ can benefit decoherence time without introducing approximate decomposition error. Additionally, exploration of heterogeneous basis gates to further reduce pulse time is an important direction. Finally, exploring methods to scale Corral or develop new SNAIL realizable topologies to compete with aspiration hypercube topologies for larger qubit numbers is an important next step.

ACKNOWLEDGMENTS

This work is partially supported by the Laboratory of Physical Sciences and NSF Award CNS-1822085. MX, MJH, and PL are partially supported by the U.S. Department of Energy, Office of Science, National Quantum Information Science Research Centers Co-Design Center for Quantum Advantage under contract DE-SC0012704.

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