Improvement in Voltage Gain of Interleaved High Step-Down Converter

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Abstract: An interleaved high step-down converter is presented herein, which utilized a diode-capacitor module so as to make the step-down voltage gain under the same duty cycle as well as the voltage stresses on switches and diodes relatively low as compared with the existing circuits. Also, under the same voltage gain, the proposed circuit had a relatively large duty cycle, making the elapsed time per cycle for the connection between the input and the output enlarged, and hence the controller was not interrupted by noises. This converter can be used in low-output-power high-output-current applications. In this study, the basic operating principles of the proposed converter were firstly described and analyzed, and finally, its effectiveness was demonstrated by experiment.

Keywords: interleaved high step-down converter; energy-transferring capacitor; field-programmable gate array (FPGA); voltage gain

1. Introduction

With the fast development of technology, the high step-down converter is widely used in the relatively low output voltage of the power supply feeding batteries and light emitting diode (LED) lamps, among others. If an extremely small duty cycle in the traditional buck converter is needed, it is difficult to control this converter and the accompanying power loss would be increased.

For the step-down converter to be considered, the studies [1–5] present two-stage converters. Such converters can effectively improve the step-down converter ratio. However, these converters need a relatively large number of components, gate driving circuits, and other additional factors. In addition, the efficiency of the two-stage converter is the product of individual efficiencies, thereby making the overall efficiency relatively low.

For the multiple phases to be considered, the converter needs interleaved control. In general, this converter has two or more identical circuits that are paralleled and are then connected to the output load. Each phase has an angle difference angle of \( \pm \frac{360^\circ}{N} \) between the two adjacent phases, if \( N \) phases are used. By doing so, the current stresses on components are reduced, the overall efficiency is improved, and the output current ripple is reduced, thus rendering the low output capacitance needed, as well as the output capacitor lifespan enlarged. Recently, many multiphase interleaved high step-down converters have been presented [6–20]. The papers [6–8] present two-phase interleaved step-down converters based on coupling inductors so as to attain high step-down voltage gains. The papers [8–12] and [15–20] present the converters with energy-transferring capacitors so as to achieve high step-down voltage gains and current balance as well as to reduce switch/diode voltage stresses. The paper [13] presents a two-phase interleaved high step-down
converter, which is based on the energy-transferring capacitor so as to improve a high step-down voltage gain as well as to reduce switch voltage stresses. Nevertheless, the currents in two phases are not identical. The paper [14] presents a four-phase interleaved synchronously rectified (SR) buck converter to improve the step-down voltage gain. As for the papers [18–20], the output voltages were floating due to the switches connected in series with the ground. By doing so, the galvanic isolation between the input and the output is required.

On the basis of the aforementioned papers, the proposed converter was derived from the converter shown in [13], so as to improve the step-down conversion ratio in [13]. As compared with the circuit shown in [13], the proposed circuit had a relatively large duty cycle under the same voltage gain, thereby causing the elapsed time per cycle for the connection between the input and the output to be enlarged, and hence the controller to not be interrupted by noises.

2. Basic Operating Principles

Figure 1 displays the proposed high step-down converter, which is constructed by five switches $Q_1$, $Q_2$, $Q_3$, $Q_4$, and $Q_5$; three diodes $D_1$, $D_2$, and $D_3$; three energy-transferring capacitors $C_1$, $C_2$, and $C_3$; two inductors $L_1$ and $L_2$; and one output capacitor $C_o$. Regarding the load, it was built up by one output resistor $R_o$. It is noted that the diode-capacitor module was composed of $D_1$, $D_2$, $D_3$, $C_1$, $C_2$, and $C_3$, making the voltage gain of the proposed converter lower than that of the converter shown in [13].

Some symbols and definitions are to be given prior to dealing with this section, and are listed below:

1. The input voltage is signified by $V_i$, and the output is denoted by $V_o$.
2. The values of the capacitors $C_1$, $C_2$, and $C_3$ are large enough such that the voltages across them can be regarded as some constant values.
3. The currents in $Q_1$, $Q_2$, $Q_3$, $Q_4$, and $Q_5$ are expressed by $i_{o1}$, $i_{o2}$, $i_{o3}$, $i_{o4}$, and $i_{o5}$, respectively; the currents in $C_1$, $C_2$, and $C_3$ are represented by $i_{c1}$, $i_{c2}$, and $i_{c3}$, respectively; the currents in $L_1$ and $L_2$ are indicated by $i_{l1}$ and $i_{l2}$, respectively; the current $i_o$ is the sum of $i_{o1}$ and $i_{o2}$; the currents in $D_1$, $D_2$, and $D_3$ are signified by $i_{d1}$, $i_{d2}$, and $i_{d3}$, respectively; the current $R_o$ is expressed by $i_o$.
4. The voltages on $L_1$ and $L_2$ are denoted by $v_{l1}$ and $v_{l2}$, respectively; the voltages on $C_1$, $C_2$, and $C_3$ are expressed by $v_{c1}$, $v_{c2}$, and $v_{c3}$, respectively; the voltage across $C_o$ is represented by $v_o$.
5. The switching period and frequency are indicated by $T_s$ and $f_s$, respectively.
6. The gate driving signals for $Q_1$, $Q_2$, $Q_3$, $Q_4$, and $Q_5$ are denoted by $v_{g1}$, $v_{g2}$, $v_{g3}$, $v_{g4}$, and $v_{g5}$, respectively. Furthermore, $v_{g1}$ is in phase with $v_{g5}$ but is complimentary to $v_{g4}$, whereas $v_{g2}$ is complimentary to $v_{g4}$ and is shifted by $180^\circ$ from $v_{g1}$. In addition, the duty cycle of $v_{g1}$ is $D_1$, the duty cycle of $v_{g2}$ is $D_2$, and $D_1 + D_2 = D$.
7. Because the proposed circuit operates in the continuous conduction mode (CCM), there are four operating states over one switching period as shown in Figure 2.
2.1. Basic Operating Principles

2.1.1. State 1: \([t_0 \leq t \leq t_1]\)

As displayed in Figure 3, the switches \(Q_1, Q_3,\) and \(Q_5\) are turned on but the switches \(Q_2\) and \(Q_4\) are turned off, whereas the diode \(D_1\) is turned off but the diodes \(D_2\) and \(D_3\) are turned on. During this state, the input voltage \(V_i\) minus \(V_o\) is across the energy-transferring capacitor \(C_1\) and the inductor \(L_2\), thereby making \(C_1\) charged and \(L_2\) magnetized. At the same time, the energy-transferring capacitors \(C_2\) and \(C_3\) are discharged, and the inductor \(L_1\) is demagnetized due to the voltage across \(L_1\) being \(-V_o\), thus rendering the current \(i_{L1}\) flow through the switch \(Q_5\).

\[v_{gs1} (=v_{gs3})\]
\[T_s\]
\[i_{C1}\]
\[i_{C2} (=i_{C3})\]
\[i_{D1}\]
\[i_{L1}\]
\[i_{L2}\]
\[i_o\]

\(0\)
\(0\)
\(0\)
\(0\)
\(t_0\)
\(t_1\)
\(t_2\)
\(t_3\)
\(t_0 + T_s\)

Figure 2. Illustrated key waveforms relevant to the proposed converter with \(D_a = D_b = D\).
2.1.2. States 2 and 4: \([t_1 \leq t \leq t_2, t_3 \leq t \leq t_4 \leq T_3]\)

As displayed in Figure 4, the switches \(Q_s\) and \(Q_o\) are turned on but the switches \(Q_i\), \(Q_2\), and \(Q_L\) are turned off. During this state, the diodes \(D_1\), \(D_2\), and \(D_3\) are turned off. At the same time, the inductors \(L_1\) and \(L_2\) are demagnetized due to the voltages across \(L_1\) and \(L_2\) being \(-V_o\), thereby rendering the currents \(i_{ds}^{1}\) and \(i_{ds}^{2}\) flow through the switches \(Q_i\) and \(Q_s\), respectively.

2.1.3. State 3: \([t_2 \leq t \leq t_3]\)

As displayed in Figure 5, the switches \(Q_2\) and \(Q_s\) are turned on but the switches \(Q_i\), \(Q_o\), and \(Q_k\) are turned off, whereas the diode \(D_1\) is turned on but the diodes \(D_2\) and \(D_3\) are tuned off. During this state, the energy stored in the energy-transferring capacitor \(C_1\) releases energy to the energy-transferring-capacitors \(C_i\) and \(C_o\), the inductor \(L_1\) and the load, thereby making \(C_i\) and \(C_o\) charged and \(L_2\) magnetized. At the same time, the inductor \(L_3\) is still demagnetized, thus making the current \(i_{ds}^{2}\) flow through the switch \(Q_s\). It is noted that the diode-capacitor module is composed of \(D_i\), \(D_2\), \(D_3\), \(C_i\), \(C_o\), and \(C_s\).

Figure 3. Current flow of state 1.

Figure 4. Current flow of states 2 and 4.

Figure 5. Current flow of state 3.
2.2. Voltage Gain

By applying the voltage-second balance to the inductors \( L_1 \) and \( L_2 \), the following expressions can be obtained with \( D_a = D_b = D \) as

\[
\begin{align*}
(V_{C_1} - V_{C_2} - V_{C_3} - V_o)D &= V_o(1 - D) \\
(V_o - V_{C_1} - V_{C_2} - V_o)D &= V_o(1 - D) \\
(V_{C_2} - V_o)D &= V_o(1 - D) \\
(V_{C_3} - V_o)D &= V_o(1 - D)
\end{align*}
\]

(1)

(2)

(3)

(4)

By substituting (3) and (4) into (1), the following expression can be found as

\[
V_{C_1}D = 3V_o
\]

(5)

Finally, by substituting (5) into (2), the voltage gain can be obtained as

\[
\frac{V_o}{V_o} = \frac{D}{4}
\]

(6)

2.3. Boundary Conditions of \( L_1 \) and \( L_2 \)

The condition of the boundary conduction mode (BCM) of the inductor \( L_1 \) can be described as follows:

\[
2I_{L_1} = \Delta i_{L_1}
\]

(7)

where \( I_{L_1} \) and \( \Delta i_{L_1} \) are the DC and AC values of the current \( i_{L_1} \), respectively.

The condition of the BCM of the inductor \( L_2 \) can be described as follows:

\[
2I_{L_2} = \Delta i_{L_2}
\]

(8)

where \( I_{L_2} \) and \( \Delta i_{L_2} \) are the DC and AC values of the current \( i_{L_2} \), respectively.

First of all, let two inductors be the same and three capacitors \( C_1, C_2, \) and \( C_3 \) be identical. Accordingly, on the basis of the capacitor ampere-second balance of \( C_1 \) and from states 1 and 3, the following expression can be obtained:

\[
\frac{1}{3} \cdot I_{L_2} \cdot D_b \cdot T_s = I_{L_1} \cdot D_a \cdot T_s
\]

(9)

Since \( D_a = D_b = D \), from (9), the relationship between \( I_{L_1} \) and \( I_{L_2} \) can be obtained as

\[
I_{L_1} = \frac{1}{3} I_{L_2}
\]

(10)

According to Kirchhoff’s current law, the following expression of DC value of \( i_{L_0} \), called \( I_{L_0} \), can be obtained as:

\[
I_{L_0} = I_{L_1} + I_{L_2} = I_o
\]

(11)

By substituting (10) into (11), the currents \( I_{L_1} \) and \( I_{L_2} \) can be represented as:

\[
\begin{cases}
I_{L_1} = \frac{1}{4} I_o \\
I_{L_2} = \frac{3}{4} I_o
\end{cases}
\]

(12)

Also,

\[
I_o = \frac{V_o}{R_o}
\]

(13)

Therefore, by substituting (13) into (12), the following equations can be obtained as:

\[
\begin{cases}
I_{L_1} = \frac{V_o}{4R_o} \\
I_{L_2} = \frac{3V_o}{4R_o}
\end{cases}
\]

(14)
2.3.1. BCM Curve of \( L_1 \)

The ripple of the current flowing through the inductor \( L_1 \), called \( \Delta i_{L_1} \), can be expressed by:

\[
\Delta i_{L_1} = \frac{v_{L_1} \Delta t}{L_1} = \frac{V_o (1 - D) T}{L_1}
\]  
(15)

Therefore, as \( 2I_{L_1} \geq \Delta i_{L_1} \), the inductor \( L_1 \) will operate in the CCM, namely,

\[
2I_{L_1} \geq \Delta i_{L_1}
\]
\[
\Rightarrow 2 \times \frac{V_o}{4R_o} \geq \frac{V_o (1 - D) T}{L_1}
\]
\[
\Rightarrow \frac{L_1}{R_o T} \geq 2(1 - D)
\]
\[
\Rightarrow K_1 \geq K_{crit1}(D)
\]  
(16)

where \( K_1 = \frac{L_1}{R_o T} \) and \( K_{crit1}(D) = 2(1 - D) \).

From (16), if \( K_1 \geq K_{crit1}(D) \), the inductor \( L_1 \) works in the CCM; otherwise, the inductor \( L_1 \) works in the DCM. Therefore, the boundary curve between the two modes can be drawn as shown in Figure 6.

![Figure 6. Boundary curve between the two operating modes for the inductor \( L_1 \).](image)

2.3.2. BCM Curve of \( L_2 \)

The ripple of the current flowing through the inductor \( L_2 \), called \( \Delta i_{L_2} \), can be indicated by

\[
\Delta i_{L_2} = \frac{v_{L_2} \Delta t}{L_2} = \frac{V_o (1 - D) T}{L_2}
\]  
(17)

Therefore, as \( 2I_{L_2} \geq \Delta i_{L_2} \), the current \( L_2 \) will operate in the CCM, namely,

\[
2I_{L_2} \geq \Delta i_{L_2}
\]
\[
\Rightarrow 2 \times \frac{3V_o}{4R_o} \geq \frac{V_o (1 - D) T}{L_2}
\]
\[
\Rightarrow \frac{L_2}{R_o T} \geq \frac{2}{3}(1 - D)
\]
\[
\Rightarrow K_2 \geq K_{crit2}(D)
\]  
(18)

where \( K_2 = \frac{L_2}{R_o T} \) and \( K_{crit2}(D) = \frac{2}{3}(1 - D) \).
From (18), if \( K_2 \geq K_{\text{crit}}(D) \), the inductor \( L_2 \) works in the CCM; otherwise, the inductor \( L_2 \) works in the DCM. Therefore, the boundary curve between the two modes can be plotted as shown in Figure 7.

**Figure 7.** Boundary curve between the two operating modes for the inductor \( L_2 \).

### 2.4. Circuit Comparison

In this subsection, the proposed converter is compared with the existing circuits shown in [13,17,19,20] in terms of voltage gain, number of components, voltage stresses on switches and diodes, and floating output. The results are tabulated in Table 1.

The proposed circuit has the same voltage gain as the circuits shown in [17,19], it has a lower voltage gain than the circuits shown in [13,20], it has a smaller component count than the circuits in [17,19], and it has a greater component count than the circuits in [13,20]. Furthermore, the proposed circuit and the circuit shown in [17] have no floating output. In addition, the average values of voltage stresses on switches and diodes for the circuits in [20], [13], [17], and [19], were 3/8\( V_{\text{in}} \), 5/8\( V_{\text{in}} \), 7/15\( V_{\text{in}} \), and 11/32\( V_{\text{in}} \), respectively. From this, it can be seen that the proposed has a smaller average value than the former two and a larger average value than the last two. In addition, for the proposed converter to be considered, the voltage across \( L_1 \) is \( V_{\text{in}} - V_{C_1} - V_o \) during the magnetizing period, whereas the voltage across \( L_2 \) is \( V_{C_1} - V_{C_2} - V_{C_3} \) during the magnetizing period. For the converter shown in [20] to be considered, the voltages across \( L_1 \) and \( L_2 \) are both 0.5\( V_{\text{in}} - V_o \) during the magnetizing period. Because the values of \( V_{\text{in}} - V_{C_1} - V_o \) and \( V_{C_1} - V_{C_2} - V_{C_3} \) are both smaller than 0.5\( V_{\text{in}} - V_o \), the former has a lower voltage gain than the latter.
Table 1. Circuit comparison.

| Circuit | Voltage Gain | Component Number | Switch Voltage Stress | Diode Voltage Stress | Floating Output |
|---------|--------------|------------------|-----------------------|---------------------|-----------------|
| Proposed | $\frac{D}{4}$ | 14 | $V_{d1} = V_{d4} = V_{d5} = \frac{V_o}{4}$ | $V_{d1} = V_{d2} = V_{d3} = \frac{V_o}{4}$ | No |
|         |              |                  | $V_{d2} = V_{d5} = \frac{3}{4} V_o$ |                     |                 |
|         |              |                  | $V_{d1} = V_o$; $V_{d4} = \frac{V_o}{2}$ |                     |                 |
| [20]    | $\frac{D}{2}$ | 9 | $V_{d2} = V_{d5} = \frac{V_o}{2}$ |                    No | Yes |
|         |              |                  | $V_{d1} = \frac{V_o}{3}$ |                     |                 |
| [13]    | $\frac{D}{3}$ | 10 | $V_{d2} = V_{d5} = \frac{2}{3} V_o$ |                     No | Yes |
|         |              |                  | $V_{d4} = V_{d5} = \frac{V_o}{3}$ |                     |                 |
| [17]    | $\frac{D}{4}$ | 16 | $V_{d1} = \frac{V_o}{4}$ |                    No |                  |
|         |              |                  | $V_{d2} = V_{d5} = \frac{V_o}{2}$ |                     |                 |
| [19]    | $\frac{D}{4}$ | 17 | $V_{d1} = V_{d3} = V_{d4} = \frac{V_o}{2}$ |                    Yes |                  |
|         |              |                  | $V_{d1} = \frac{V_o}{4}$ |                     |                 |

3. Design Considerations

Table 2 shows the system specifications. On the basis of this table, the associated components are designed.

Table 2. System specifications

| System Parameters                        | Specifications |
|------------------------------------------|----------------|
| Operating mode                           | CCM            |
| Rated input voltage ($V_{in}$)           | 60 V           |
| Rated output voltage ($V_o$)             | 1.8 V          |
| Rated output current ($I_{out}$)/power ($P_{out}$) | 20 A/36 W |
| Minimum output current ($I_{min}$)/power ($P_{min}$) | 2 A/3.6 W |
| Switching frequency ($f_s$)/period ($T_s$) | 100 kHz/10 µs |

3.1. Design of Inductors $L_1$ and $L_2$

According to Table 1 and (6), the corresponding duty cycle $D$ can be obtained:

$$D = \frac{4V_o}{V_{in}} = \frac{4 \times 1.8}{60} = 0.12$$

From (16), if the inductor $L_1$ works in the CCM, then the value of the inductor $L_1$ should be satisfied with the following inequality:

$$L_1 \geq (1 - D) \times 2 \times R_{r, \text{max}} \times T_s$$

$$\Rightarrow L_1 \geq (1 - D) \times \frac{2V_o}{I_{r, \text{min}}} \times T_s$$

(20)
where $R_{\text{on},\text{min}}$ is the load resistance at the minimum load. By substituting the system specifications shown in Table 1 and (19) into (20), the value range of the inductor $L_1$ can be expressed as

$$L_1 \geq (1 - 0.12) \times \frac{2 \times 1.8 \times 10 \mu}{2}$$

$$\Rightarrow L_1 \geq 15.84 \mu \text{H}$$

From (18), if the inductor $L_2$ works in the CCM, then the value of the inductor $L_2$ should be satisfied with the following inequality:

$$L_2 \geq \frac{(1 - D) \times 2 \times R_{\text{on},\text{min}} \times T_s}{3}$$

$$\Rightarrow L_2 \geq \frac{(1 - D) \times 2 \times V \times T_s}{3 \times I_{\text{on},\text{min}}}$$

By substituting the system specifications shown in Table 1 and (19) into (22), the value range of the inductor $L_2$ can be expressed as

$$L_2 \geq \frac{(1 - 0.12) \times 2 \times 1.8 \times 10 \mu}{3 \times 2}$$

$$\Rightarrow L_2 \geq 5.28 \mu \text{H}$$

Finally, the values of $L_1$ and $L_2$ are identical and equal to $20 \mu \text{H}$ in order to meet the requirement of $I_{L2} = 3I_{L1}$.

### 3.2. Design of Energy-Transferring Capacitors $C_1$ to $C_3$

As shown in state 1, the current waveform of the energy-transferring capacitor $C_1$ is the same as that of the inductor $L_1$, and hence the corresponding constant values can be expressed by

$$I_{C1,\text{DaTs}} = I_{L1,\text{DaTs}} = I_{L1}$$

From (1) to (4) and Table 1, the voltage across $C_1$, $V_{C1}$, can be signified by

$$V_{C1} = \frac{3 \times V_a}{D} = \frac{3 \times 1.8}{0.12} = 45 \text{V}$$

In addition, by assuming that the voltage ripple of $C_1$ is $0.1\%$ of $V_{C1}$ and by substituting the results from (12), (19), and (25) into (26), the value of $C_1$ can be obtained as

$$C_1 \geq \frac{I_{C1,\text{DaTs}} \times D_a T_s}{0.1\% \times V_{C1}}$$

$$= \frac{I_{L1} \times DT_s}{0.001 \times V_{C1}}$$

$$= \frac{5 \times 0.12 \times 10 \mu}{0.001 \times 45} = 133.3 \mu \text{F}$$

As shown in state 3, the current waveforms of the energy-transferring capacitors $C_2$ and $C_3$ are the same as that of the inductor $L_1$, and hence the corresponding constant value can be represented by:

$$I_{C2,\text{DaTs}} = I_{C3,\text{DaTs}} = I_{L1,\text{DaTs}} = I_{L1}$$

From (1) to (4) and Table 1, the voltages across $C_2$ and $C_3$, $V_{C2}$ and $V_{C3}$, can be obtained as

$$V_{C2} = V_{C3} = \frac{V}{D} = \frac{1.8}{0.12} = 15 \text{V}$$

In addition, by assuming that the voltage ripples of $C_2$ and $C_3$ are both $0.1\%$ of $V_{C2}$ and by substituting the results from (12), (19), and (28) into (29), the values of $C_2$ and $C_3$ can be obtained as
Finally, in order to meet the assumption for (11), the values of $C_1$, $C_2$, and $C_3$ are all set at 470 $\mu$F.

3.3. Design of Output Capacitor $C_o$

The current flowing through the output capacitor $C_o$ is the sum of the currents $i_{L_1}$ and $i_{L_2}$, namely,

$$\Delta i_{c_o}(t) = \Delta i_{L_1}(t) + \Delta i_{L_2}(t)$$

$$\Rightarrow \Delta i_{c_o}(D_{1}T_s) = \Delta i_{L_1}(D_{1}T_s) + \Delta i_{L_2}(D_{2}T_s)$$

$$\Rightarrow \Delta i_{c_o}(D_{2}T_s) = \left(\frac{V_{in} - V_{c_1} - V_{c_2}}{L_1} + \frac{D}{f_s} \times \frac{-V_{oc}}{L_2} + \frac{D}{f_s} \right)$$

Because $L_1 = L_2 = L_2$ (30) can be rearranged as

$$\Delta i_{c_o} = \frac{(1 - 2D) \times V_{oc}}{L \times f_s}$$

(31)

After this, by assuming that the output voltage ripple of $C_o$ is 0.1% of $V_o$, and by substituting the results from Table 1, (19), and (31) into (32), the value of $C_o$ can be obtained to be

$$C_o \geq \frac{\Delta i_{c_o,DaSh} \times D_{2}T_s}{0.1\% \times V_o} = \frac{(1 - 2D) \times V_{oc} \times DT_s}{8 \times 0.001 \times V_o \times L \times f_s}$$

$$= \frac{(1 - 2 \times 0.12) \times 0.12 \times 10 \mu F}{8 \times 0.001 \times 20 \mu F \times 100k} = 57 \mu F$$

Eventually, the value of $C_o$ was chosen as 68 $\mu$F. In addition, Table 3 lists the component specifications of the proposed converter.

| Components | Specifications |
|------------|---------------|
| MOSFET     | $Q_1$, $Q_4$, $Q_5$, FDP047AN |
| Diode      | $D_1$, $D_2$, $D_3$, STPS30L45CT |
| Energy-transferring Capacitor | $C_1$, 47 470 µF/100 V Rubycon Electrolytic Capacitor |
| Capacitor  | $C_2$, $C_3$, 470 µF/35 V Rubycon Electrolytic Capacitor |
| Inductor   | $C_o$, 68 µF/6.3 V Rubycon Electrolytic Capacitor |
| Gate driver| Core CH330125, $L_1 = L_2 = 20 \mu H$, TLP250 |

4. System Control Strategy

Figure 8 shows the system configuration of the proposed interleaved high step-down converter, which is composed of the main power circuit and the feedback control circuit. As for the feedback control circuit, the output signal is extracted from the voltage divider. Afterwards, such an analog signal is sent to the analog-to-digital converter (ADC) and then is transferred to the digital signal. This digital signal is sent to the field programmable gate array (FPGA) so as to obtain the corresponding gate control signals. Finally, these control signals are used to drive the corresponding switches after individual gate drivers so as to keep the output voltage constant at some value.
5. Experimental Results

5.1. Measured Waveforms

Figure 9 shows the gate driving signals for the switches Q1, Q2, Q3, Q4 and Q5, called Vq1, Vq2, Vq3, Vq4, and Vq5, respectively. Figure 10 displays the voltages across Q1, Q2, Q3, and Q4, called Vds1, Vds2, Vds3, and Vds4. Figure 11 shows the voltages across Q1 and Q2, called Vds1 and Vds2. Figure 12 displays the voltages across the energy-transferring capacitors C1, C2, and C3, called Vc1, Vc2, and Vc3, respectively. Figure 13 shows the voltages on the diodes D1, D2, and D3, called Vin, Vd2, and Vd3, respectively. Figure 14 displays the currents i1, i2, and i3.

From Figure 9, it can be seen that the gate driving signal sequence met the requirements. From Figures 10 and 11, it can be seen that the voltage stresses on Q1, Q3, and Q5, without voltage spikes considered, were all about 15 V, corresponding to Vds1–Vc1, whereas the voltage stresses on Q2 and Q4, without voltage spike considered, were about 45 V, corresponding to Vc1. As for voltage spikes on switches during the turn-off period, they came from the resonance between line parasitic inductances and switch body capacitances. From Figure 12, it can be seen that the voltages across C1, C2, and C3 were kept at the values of 45.5 V, 15.5 V, and 15 V, respectively, which were slightly larger than the calculated values shown in Equations (25) and (28) at 45 V, 15 V, and 15 V, respectively. From Figure 13, it can be seen that the voltages across D1, D2, and D3 were three-level and the voltage stresses on these diodes were all about 15 V, corresponding to Vc2. From Figure 14, it can be seen that the current i3 was the sum of the currents i1 and i2, whereas the DC values of i1 and i2 were about 5 A and 15 A, respectively, satisfying Equation (12).
Figure 9. Experimental waveforms at rated load: (1) $v_{gs1}$, (2) $v_{gs2}$, (3) $v_{gs4}$, (4) $v_{gs5}$.

Figure 10. Experimental waveforms at rated load: (1) $v_{ds1}$, (2) $v_{ds2}$, (3) $v_{ds4}$, (4) $v_{ds5}$.

Figure 11. Experimental waveforms at rated load: (1) $v_{ds1}$, (2) $v_{ds3}$. 
5.2. Efficiency Measurement

The means of measuring the efficiency is given herein, and the accompanying result follows. As displayed in Figure 15, the input current was attained by measuring the voltage across the current sensing resistor according to the digital meter named Fluke 8050 A. Afterwards, the input voltage
was also obtained by the digital meter. Hence, the input power can be obtained. Concerning the output power, the output current was read from the digital load and the output voltage was also attained by the digital meter. Hence, the output power can be obtained. Eventually, the resulting efficiency can be known. Accordingly, Figure 16 displays the curve of efficiency versus load current. From Figure 16, it can be known that the efficiency all over the load range was above 81.4% and the maximum efficiency was 85.1%.

![Figure 15. Efficiency measurement block diagram.](image)

![Figure 16. Plot of efficiency versus load current.](image)

5.3. Power Loss Breakdown Analysis

In the following section, the power loss breakdown analysis, not based on circuit modeling [21–31] but based on component datasheets, is shown under the condition that the converter operated at a rated load of 36 W.

5.3.1. Power Losses in Switches

The power loss in each switch, called $P_{\text{loss}}$, can be calculated on the basis of Equation (33).

$$
P_{\text{loss}} = P_{\text{on,cond}} + P_{\text{turn-on}} + P_{\text{turn-off}} = \frac{i_{\text{rms}}^2}{2} \cdot R_{\text{on}} + \frac{V_{\text{th}} \cdot I_{\text{th, max}} \cdot t_{\text{r}} \cdot f}{6} + \frac{V_{\text{th}} \cdot I_{\text{th, max}} \cdot t_{\text{f}} \cdot f}{6}$$

(33)

where $P_{\text{on,cond}}$ indicates the turn-on conduction loss, $P_{\text{turn-on}}$ signifies the switching loss during the turn-on period, $P_{\text{turn-off}}$ represents the switching loss during the turn-off period, $R_{\text{on}}$ indicates the turn-on resistance, $t_{\text{r}}$ signifies the turn-on rising time, and $t_{\text{f}}$ represents the turn-off falling time. According to the FDP047AN datasheet, it can be known that the values of $R_{\text{on}}$, $t_{\text{r}}$, and $t_{\text{f}}$ are 4 mΩ, 88 ns, and 45 ns, respectively.
Therefore,
\[ P_{Q1,\text{loss}} = 2.5^2 \cdot 4 \cdot 10^{-3} + \left( \frac{15 \cdot 5.132 \cdot 133 \cdot 10^{-9} \cdot 100k}{6} \right) = 0.195W \] (34)
\[ P_{Q2,\text{loss}} = 1.95^2 \cdot 4 \cdot 10^{-3} + \left( \frac{45 \cdot 5.396 \cdot 133 \cdot 10^{-9} \cdot 100k}{6} \right) = 0.55W \] (35)
\[ P_{Q3,\text{loss}} = 3.548^2 \cdot 4 \cdot 10^{-3} + \left( \frac{45 \cdot 10.264 \cdot 133 \cdot 10^{-9} \cdot 100k}{6} \right) = 1.07W \] (36)
\[ P_{Q4,\text{loss}} = 14.43^2 \cdot 4 \cdot 10^{-3} + \left( \frac{15 \cdot 20.792 \cdot 133 \cdot 10^{-9} \cdot 100k}{6} \right) = 1.52W \] (37)
\[ P_{Q5,\text{loss}} = 7.139^2 \cdot 4 \cdot 10^{-3} + \left( \frac{15 \cdot 15.66 \cdot 133 \cdot 10^{-9} \cdot 100k}{6} \right) = 0.724W \] (38)

Additionally, the total switch power loss, called \( P_{Q,\text{loss,total}} \), can be obtained from (34) to (38) as
\[ P_{Q,\text{loss,total}} = P_{Q1,\text{loss}} + P_{Q2,\text{loss}} + P_{Q3,\text{loss}} + P_{Q4,\text{loss}} + P_{Q5,\text{loss}} 
= 0.195 + 0.55 + 1.07 + 1.52 + 0.724 = 4.059W \] (39)

5.3.2. Power Losses in Diodes

The power loss in each diode, called \( P_{D,\text{loss}} \), can be calculated on the basis of (40).
\[ P_{D,\text{loss}} = V_F \cdot I_{D,\text{avg}} \] (40)
where \( V_F \) signifies the forward bias voltage, and \( I_{D,\text{avg}} \) represents the forward current.
\[ P_{D1,\text{loss}} = 0.095 \cdot 0.68 = 0.0646W \] (41)
\[ P_{D2,\text{loss}} = 0.096 \cdot 0.505 = 0.0485W \] (42)
\[ P_{D3,\text{loss}} = 0.097 \cdot 0.505 = 0.0489W \] (43)

In addition, the total diode power loss, called \( P_{D,\text{loss,total}} \), can be obtained from (41) to (43) as
\[ P_{D,\text{loss,total}} = P_{D1,\text{loss}} + P_{D2,\text{loss}} + P_{D3,\text{loss}} 
= 0.0646 + 0.0485 + 0.0489 = 0.162W \] (44)

5.3.3. Power Losses in Inductors

The power loss in each inductor, called \( P_{L,\text{loss}} \), can be calculated on the basis of (45).
\[ P_{L,\text{loss}} = i_{L,\text{loss}}^2 \cdot R_{DC} \] (45)
where \( R_{DC} \) signifies the copper resistance.
\[ P_{L1,\text{loss}} = 5^2 \cdot 14.7 \cdot 10^{-3} = 0.3675 W \] (46)
\[ P_{L2,\text{loss}} = 15^2 \cdot 10.5 \cdot 10^{-3} = 2.3625 W \] (47)

Additionally, the total inductor power loss, called \( P_{L,\text{loss,total}} \), can be obtained from (46) and (47) as
\[ P_{L,\text{loss,total}} = P_{L1,\text{loss}} + P_{L2,\text{loss}} 
= 0.3675 + 2.3625 = 2.73 W \] (48)

5.3.4. Estimated Efficiency

From Equations (39), (44), and (48), the power losses of components are drawn in Figure 17. In addition, the estimated efficiency was 83.8%, which is higher than the measured efficiency of 81.4%.
6. Conclusions

An interleaved high step-down converter is presented herein. Compared with the related existing circuits [13,20] shown in Table 1, the proposed circuit had a relatively low step-down voltage gain under the same duty cycle, and had relatively low voltage stresses on the switches and diodes, thereby causing the switches with low turn-on resistances and the diodes with low forward bias voltages to be chosen. The main reason was that a diode-capacitor module utilized in the proposed converter can make inductors magnetized with relatively low voltages. Moreover, under the same voltage gain, the proposed circuit had a larger duty cycle than the circuits shown in [13,20], thereby rendering the elapsed time per cycle for the connection between the input and the output enlarged, and hence the controller not interrupted by noises.

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