The Effect of Source and Drain Pocketing on the Performance of Double-Gate Tunnelling Field-Effect Transistor

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Abstract. In this paper the digital and analogue performance of double-gate tunnelling FET, DGTFET, is reported, when a pocket of different dielectric is inserted near the source, drain or both. The variation of these pocket lengths and their relative shift to the edge of source or drain region affects device performance. The investigated performance parameters include the ON/OFF ratio, the maximum cut-off frequency, f_T, the subthreshold swing, SS, and the ambipolar current, I_ambi. With the aid of TCAD simulator, the effect of pocket parameter variation is studied. Our study shows that when the main gate dielectric is hafnium dioxide, the source pocket is favored to be of low dielectric constant and high width. However, for the drain case, it is better to have shorter pockets with a low dielectric constant. The investigation shown here proves that pocketing the DGTFET can enhance its whole performance in terms of investigated parameters.

1. Introduction
Four decades ago, the trend in electronics industry was to scale down transistor dimensions, voltages and scale up doping [1,2]. Extra power usage of ICs limits scaling down of transistors [3]. TFET depends on tunnelling phenomena to transport carriers from source to drain rather than thermionic emission as usual MOSFETs to generate current. However, its subthreshold swing is less than MOSFET subthreshold swing, SS, of 60 mV/decade 300 K [4].

As we compare different transistors together, we consider the DC properties of transistor like subthreshold swing, ambipolar current, ON/OFF ratio and ON current are important. For optimum performance, one needs less SS, ambipolar current and higher ON/OFF ratio. Ultimately, by designing the TFET, we aim to integrate it with current CMOS technology. Some obstacles retard such integration, some obstacles retard such integration, TFET devices must have specific ON current for operating supply voltages less than 0.5V [5]. Unfortunately, band-to-band-tunnelling (BTBT) produces less ON current compared to thermionic emission used in MOSFETs.

Several techniques were used to boost the performance of DGTFET. To increase the ON current (hence increasing the ON/OFF ratio), device designers used high dielectric material below the gate [6–10]. Also, the use of multiple gate materials enhances the performance of DGTFET and was

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used to enhance the ON current and to suppress the OFF current [11]. Gate work function engineering was used to shift the device transfer characteristics away from zero [12]. The use of multiple materials under the gate electrode was introduced to enhance the device performance in [10].

Reference [13] has investigated the effect of moving a high-k dielectric pocket above the channel region on the DC, analogue and transient response of hetero-gate TFET. The authors of [13] found several trade-offs in the performance of TFET. All the analysis proposed by them was for a single length of 5 nm. The best device obtained was when the pocket is shifted from the source under the gate by 1.5 nm [13]. In our work, we are studying a generic pocket with different shifts and widths, the studied pockets are shifted away from the channel (easier in fabrication). Additionally, we solve the trade-offs between parameters by introducing a statistical figure-of-merit, FOM, and propose a study for the interaction of input parameters like pocket widths and pocket shifts- to affect device quality represented by FOM.

In this paper, we use a high dielectric material like hafnium dioxide as gate dielectric and study the device when a pocket is inserted at the source, of different widths and relative shifts. Likewise, we do the same at the drain side. We study the performance when the inserted pocket is silicon dioxide or aluminium oxide. Afterward, we insert two pockets and study the device performance. We check the efficiency of pocket insertion by using analysis of variance [14].

The paper will be organized as follows, section 2 explains the structure of TFET in terms of constituent materials and their dimensions, then the used software, and respective simulation models are clarified. Finally, the calibration of simulation software to experimental data is shown and the parameter definitions are stated. Section 3 shows the study results as we study the source pocket only, the drain pocket only and when both pockets are present. At the end, we present the best obtained device as a result of our simulations.

2. Device Structure and Simulation Approach

Figure 1 illustrates the schematic view of a double gate nTFET with two pockets at source and drain. The widths of pockets are $W_S$ and $W_D$ respectively, and the source pocket is shifted in the left direction with distance $S_s$, and the drain pocket is shifted from the drain edge in the right direction for a distance of $S_D$. The source pocket has the relative permittivity $\varepsilon_1$ and the permittivity of the drain pocket is $\varepsilon_2$. Both pockets are uncovered by a contact electrode, so they are not considered as a part of the gate; in addition, the remaining gate electrode is hafnium dioxide.

The device dimensions are constant and are as following: the oxide thickness tox is 3 nm from both sides of the silicon body which is 10-nm thick. Both the source and the drain are equal in length of 60 nm. While the channel is 50 nm. Concerning doping levels, the source has $1 \times 10^{20}$ cm$^{-3}$ of acceptors, while drain has $1 \times 10^{19}$ cm$^{-3}$ of opposite polarity dopants. The channel has the
lowest doping levels compared to source and drain of $1 \times 10^{17}$ cm$^{-3}$ of donors.
During our simulations we used two materials in both pockets whose properties are shown in table 1. We also fixed the gate work function to be 4.3 eV, because it gives optimum performance as shown in [15]. The pockets’ properties are shown in table 1.

| Table 1. Design parameters used in device simulation. |
|---------------------------------|-----------------|
| Parameter                      | Value           |
| Pocket Widths and Shifts ($W_s$, $W_D$, $S_s$, $S_D$) | 0-25 nm 5 nm step |
| Pocket Materials                | $\text{Al}_2\text{O}_3-\text{SiO}_2$ |
| Pocket Relative Permittivity    | 9.1-3.9         |
| Gate Work Function              | 4.3 eV          |

All the simulations are carried out using Silvaco, version 5.19.20.R [16]. Silvaco ATLAS was used to build the device structure and to obtain the current-voltage characteristics of TFET. The variation of pocket parameters was implemented by Deckbuild Internal [17]. Results are analysed on MATLAB.

Several simulation models were used to account for several phenomena. For tunnelling across the channel, non-local band-to-band tunnelling model is utilized. For carrier statistics, Fermi-Dirac statistics model worked for highly doped regions. For carrier mobility, mobility dependence on doping concentration and on applied electric field was considered. Moreover, band gap narrowing was modelled in highly doped regions. Shockley-Read-Hall and concentration-dependent Shockley-Read-Hall models are used as recombination models [16].

At first, the nonlocal band-to-band tunnelling needs to be calibrated to an experimental work. Ahmed Shaker et al [18], using the same simulation software, tunnel-FET structure and simulation models- tuned the values of electron and hole tunnelling effective masses to match the IV characteristics of tunnel-FET to that of Kumar in [19] which is based on experimental data by IBM for the fabrication of tunnelling diode [19]. Accordingly, the electron tunnelling mass of $m_e=0.11$ and a hole tunnelling mass of $m_h=0.17$ are used in the simulation.

In order to make the results comparable to other works, we centred the transfer characteristics at zero volt, and measured the ON, OFF current and SS depending on that. That convention was proposed in [18] to compare the performance of TFET to MOSFET neglecting the effect of gate work function engineering [1]. The ON, and OFF and ambipolar currents are calculated at $V_{GS}=V_{min}=0.5$ V, 0 V and -0.5 V respectively while $V_{min}$ is the gate voltage of minimum current. The voltage thresholds when the drain current rises to 0.1 µA/µm and the subthreshold swing is the mean swing between $V_{GS}=V_{min}$ (OFF state) and $V_{GS}=V_{th}$ (ON state).

3. Results and Discussion

3.1. Source Pocket Performance
At the beginning we made two case studies for source and drain. In the first one, we inserted a pocket at the source side, and tried two materials silicon dioxide and aluminium oxide, we studied the effect of shift and pocket width on the performance of the DGTFET. Figure 2 (a)-(c) shows the performance in silicon dioxide case. It is shown that the performance parameters SS, ON/OFF ratio, ambipolar current and cut-off frequency does not depend that much on the pocket width. The performance is approximately identical for different widths as shown in figure 2- (a). However as shown in figure 2 (c) there is a little variation due to the change of width: the ambipolar current increases slightly (in a fraction of nanoampere per micron) when we increase the pocket width from 5 nm to 15 nm to 25 nm. Similar slight increase is present in the cut-off frequency as shown...
in figure 2 (c)-(d) Such increase can be attributed to the increase of nonlocal tunnelling by pocket [13].

As we increase the shift from the source edge, the performance deteriorates to a point where further shifting does not affect the device anymore. This is evident in SS, where it increases to the maximum at 5 nm then saturates with further increase of the shift as illustrated in figure 2 (a)-(b). Likewise, the ON/OFF ratio reaches the minimum at 5 nm then saturates. For ambipolar behaviour, the shift increases ambipolar behaviour with a tiny increment that it is almost constant.

In order to compare devices in our simulation I used a figure-of-merit of the device quality. In a previous work, [15], figure of merit was used to assess device performance,. It was utilized to solve multi-objective device optimization problems with aid of genetic algorithms as in [20]. The figure-of-merit tells us how much the device is good with respect to simulated dataset. Equation (1) shows how the figure-of-merit, FOM uses the Q-function for ranking devices.

\[
FOM(p_1, p_2, \ldots, p_n) = 1 - \sum_{i=1}^{n} w_i Q \left( \frac{p_i - \mu_i}{\sigma_i} \right)
\]

Such that \(p_i\) is a device parameter and \(w_i\) is its importance weight and all weights are positive and sum up to 1. Table 2 shows optimization parameters and their related constants. The parameter properties such as mean or standard deviation are of the simulated data set in our study.

**Table 2.** Parameters involved in FOM estimation.

| Order (i) | Weight | Parameter          | Mean (\(\mu_i\)) | Standard Deviation (\(\sigma_i\)) |
|-----------|--------|--------------------|-------------------|----------------------------------|
| 1         | 0.25   | \(f_T\)            | 132.8 GHz         | 36.1 GHz                         |
| 2         | 0.25   | ON/OFF             | \(2.9 \times 10^9\) | \(1.3 \times 10^9\)              |
| 3         | 0.25   | \((I_{ambi})-1\)   | \(1.3 \times 10^{13}\) (\(\mu\text{m}/\text{A}\)) | \(1.1 \times 10^{14}\) (\(\mu\text{m}/\text{A}\)) |
| 4         | 0.25   | (SS)-1             | 0.02 dec/mV       | \(8.8 \times 10^{-4}\) dec/mV    |

When we rank devices pocketed by silicon dioxide the average rank was 47.4255 %, In case of aluminium oxide, the average rank was 47.5797 %. There is a slight difference between both,
however the best device performance was achieved by silicon dioxide of 86.31% when the pocket width was 25 nm and not shifted from the source edge. The device recorded 300.97 GHz maximum cut-off frequency, 36.55 mV/decade SS, 8.65 x 10⁹ ON/OFF ratio at 0.5 gate voltage and ambipolar current small as 205.567 nA/µm. So based on average performance, changing dielectric constant in our range does not influence the device behaviour that much, however, silicon dioxide pocket is much better in performance parameters.

3.2. Drain Pocket Performance
Second, we inserted a pocket at the drain, it is shown that contrary to the source pocket, the width of the pocket influences the device performance in a stronger manner. Increasing the pocket width enhances the performance up to a specific width then it saturates. As shown in figure 3-(a), as we increase the width from 5 nm to 15 nm, the SS decreases noticeably, especially when the pocket shift is still below 10 nm. The same is true, for ON/OFF ratio, it increases largely when we increase the width as depicted in figure 3-(a)-(b). However, the performance does not almost change when we increase the pocket width up to 25 nm. Which means that inserting larger pockets may be useless.

The shift effect was apparent for shifts below 10 nm, otherwise, the performance saturates with any shift. At 10 nm, the device had minimal ambipolar current after which the ambipolar current is not much affected. Up to 5 nm of shift, the shift deteriorates device performance by increasing the subthreshold swing and decreasing both the ON/OFF ratio and the maximum cut-off frequency. As shown in Fig 3 (a)-(b), the change of pocket material, alters the device performance. In general, the increase of dielectric constant, enhances SS (by decreasing it), deteriorates ON/OFF ratio. In addition, the ambipolar current is suppressed and cut-off frequency is decreased.

In terms of FOM with coefficients shown in table 2, the average rank of silicon dioxide devices was 40.8482% and that of aluminium oxide was 42.6279%. However, the best device has 67.3415% performance and it was a silicon dioxide pocket of 5 nm width with no shift. This best obtained device had 142 GHz $f_T$, 41.1335 mV/decade SS, 4.64 x 10⁹ ON/OFF ratio and 116130 nA/µm ambipolar current.
Figure 4. FOM of silicon dioxide pockets at the source and the drain.

The FOM can be better traced for SiO$_2$ pockets as shown in figure 4-(a)-(b). It is shown that for best performance we need to have little shift of the pocket at source and drain. Besides, we need little width at the drain and larger length at the source.

3.3. Comparison between both pockets

It is apparent that drain pocketing is less effective than source pocketing to enhance device performance. The ambipolar current increases multiple orders of magnitude compared to its value with a source pocket present, and the maximum cut-off frequency that a device can have decreases to half its value as shown in figure 2-3 (c)-(d).

We compared the performance of regular device without pockets to the case when there are 5-nm unshifted SiO$_2$ pocket at either the drain or the source as this material gave best performance in single-pocket case. The problem was mainly in the ambipolar behaviour of the device, so we studied the device when $V_{GS}$ = -0.5 V just below the gate dielectric. The energy bands of regular device and source-pocketed device are similar while the drain-pocketed device shows steeper energy band near the drain region and smaller tunnelling distance as shown in figure 5- (a). It is also shown that pocketing with SiO$_2$ increases the electric field near the pocket as shown in figure 5- (b); however, drain pocketing increases field in uncontrollable manner due to the fringing capacitance of the inserted pocket and its effect on total device current [21,22]. Consequently, the electric field pushes energy bands downward decreasing the tunnelling width and allowing more electrons to tunnel as shown in figure 5–(c). The IV characteristics, figure 5- (d), shows that source pocketing increases ON current and drain pocketing increases ambipolar current in case of unshifted SiO$_2$ single pocket.
Figure 5. Comparison between unpocketed device and pocketed devices at either source or drain. Pockets are SiO$_2$, 5-nm wide and unshifted. For a cut line below the dielectric $V_{GS} = -0.5$ V; the energy bands (a), electric field magnitude (b) and nonlocal BBT electron tunneling rate (c) are depicted. The IV characterstics is shown for three devices at (d). Tunneling rate and drain current are on logarithmic scale.

3.4. Performance with Both Pockets Present

If we insert both pockets in the device, the study becomes more complicated. For each pocket there are three parameters: its dielectric constant, width and relative shift. In total, we have six variables. We can do a full factorial test [23] by assigning two levels (low and high) for each factor. The whole number of trials is $2^6 = 64$ runs. We fitted the results to a generalised linear mixed effect model of the form in equation (2).

$$FOM \sim 1 + W_s + W_d + S_s + S_d + \epsilon_1 + \epsilon_2 + W_s W_d + \cdots W_s W_d S_s S_d \epsilon_1 \epsilon_2$$  \hspace{1cm} (2)

The model includes all possible interactions, and coefficients of input parameters here represent
the relative importance of a parameter or an interaction of parameters on the performance of the device as a rank. Positive coefficient means that this parameter enhances the device by its increment, while a negative coefficient (or effect) means that the increase of that parameter or product of parameters deteriorates the device performance. A chart showing the ten most prominent effects of parameters and their products is shown in figure 6.

![Pareto Plot for pocketed DGTFET FOM](image)

**Figure 6.** Pareto effect plot for the performance of DGTFET.

As shown from figure 6, shift of source pocket is the most prominent in affecting device performance negatively. As a result, source pockets need to be closer to edge of source-channel junction., the successive prominent parameter is the width of the drain pocket. And then the type of the material, it is shown that it is better to perform pocketing with a low-dielectric material than to do with a higher dielectric. Moreover, it is better to shift the drain pocket to enhance the device performance. Afterward, other parameter interactions are less important in enhancing or deteriorating the device performance.

According to our analysis the best obtainable device had two 25-nm pockets of silicon dioxide, one at the edge of source and the other is shifted 25 nm from the drain edge. The device recorded 300.97 GHz maximum cut-off frequency comparable to 180 GHz if we inserted a single pocket below the gate that is shifted 1.5 nm as shown in reference [13], 36.55 mV/decade SS, $8.65 \times 10^9$ ON/OFF ratio at 0.5 gate voltage and ambipolar current small as 205.561 nA/μm. The addition of drain pocket minimized the ambipolar current slightly than the best obtained device of source pocket case.

4. Conclusion

In this paper an investigation of the DGTFET performance was done after the insertion of a single pocket at source and at the drain, then after the insertion of both pockets. It was shown that source pocketing is more efficient than drain pocketing. In addition, the interaction of several pocket parameters on the performance of the DGTFET was investigated and plotted. The best device had two pockets of equal width, 25 nm, and different shifts. This study has a lot of applications in terms of its methodology and results on the design and optimisation of emerging TFET devices; the study shows how pockets placed away from the channel region, without electrodes can be used to enhance device performance.
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