Process Yield and Device Stability Improvement for Sol-gel Alumina Passivation layer based GFETs

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Abstract

The stability of GFET devices is a major problem and needs a good passivation layer for the same. Low cost and low-temperature sol-gel alumina passivation layer-based GFETs is studied here with the goals to improve stability of the device and achieve high process yield. The process yield and device stability are explored for two different molarities of 0.1 M and 0.05 M. The parameters like mobility, trap charge density, minimum conductivity plateau width and minimum conductivity are extracted to compare the stability of devices. The results indicate that GFETs with 0.1 M have problems of process yield due to crack formation in the channel region post-annealing, where close to half of the devices are working, and also working devices are not stable and degrading very fast within a week’s time. On the other hand, 0.05 M sol-gel Alumina-based sample exhibits 100% process yield with all working devices and observed stable behavior for more than two months. Hence we propose an optimized process recipe for a sol-gel Alumina-based passivation layer to achieve the best possible process yield and device stability for GFETs.

Keywords: Monolayer graphene, GFET, sol-gel Alumina, Dirac point, DUV annealing

1. Introduction

The ambipolar carrier modulation through the electric field [1], the absence of bandgap and the remarkable electronic properties like high carrier mobility [2] with ballistic transport of the carriers [3] and high-velocity saturation [4] have convinced the device community to explore the two-dimensional material graphene for the high-speed radio frequency (RF) applications [5]. Along with the exceptional electronic properties, CMOS process compatibility, mechanical strength, and flexibility [6, 7] have made graphene a popular material for transistor devices.

Besides several advantages of graphene transistors, there are few challenges like yield problem and unintentional doping which contributes to the total stability of GFETs. The yield has been contributed from the several factors in particular (i) defect free CVD graphene growth [8] (ii) careful graphene transfer (delamination from growth substrate, handling during transfer and removal of the handling material) [8] (iii) good dielectric environment such as substrate surface [9], passivation [10, 11] and top gate dielectric [12] [13, 14] (iv) proper selection of contacts [15]. The process stability in each fabrication step add to the total yield of the device [16].

The unintentional doping in graphene transistors are due to the environment adsorbates, residues from the fabrication processes that limits the usage of the graphene in the practical applications which in turn affects the graphene based FETs and their reliability. Passivation layer is a key process to circumvent the above issues. Several passivation techniques like deposition of polymers, inorganic oxides and SAMs like Pentacene [17], PECVD Si$_3$N$_4$ [6], Self Assembled Monolayer (SAM) viz. 1-aminodecane [18], H-BN [19] and ALD Al$_2$O$_3$ [10, 11, 20, 21, 22, 23] by few groups.

Among various deposition techniques, the sol-gel based deposition techniques have advantages due to its high deposition rate, no vacuum requirement, low cost method, tuning of the precursor composition [24, 25]. The quality of the sol-gel film will affect the transistor stability and overall sample yield. The two important parameters for any solution processed film are molarity of the film and annealing technique [26]. The molarity of the film need to be optimized as higher or lower...
molarity of the film results in poor film quality in terms of density of the film [27] and shrinkage stress generated during densification of the film [28]. The annealing technique and recipe plays an important role in densification process of the film [29], as effective annealing technique leads to densification of the film at lower thermal budget with minimum shrinkage stress [30]. Recently the sol-gel Alumina (Al₂O₃) has been extensively used in the solar cells as a field-effect passivation layer [31] due to its good interface quality and dielectric breakdown. Park et.al [32, 33] and Bae et.al [34] have explored sol-gel Alumina on the graphene transistors as dielectric layer and pH sensing membrane and none of them have explored for the passivation of the graphene transistors.

In our previous work, we have shown that DUV annealing technique is better than thermal annealing in terms of reduced thermal budget and lower shrinkage stress. We have also proposed two step seed layer deposition technique to resolve the crack issue in sol-gel Alumina film post annealing. In this work, we continue to use DUV annealing technique with two step seed layer deposition method. Here we are investigating process yield and device stability and propose a method to improve both using optimized molarity of the film. The sol-gel alumina film quality is studied on blanket wafer using UV-VIS, ellipsometry and XPS techniques. The detail electrical characterization (transfer characteristics, hysteresis and pulse hysteresis) and analysis (mobility and trap density extraction) of GFET devices is also presented in the work.

2. Experimental

2.1. Synthesis of sol-gel Alumina precursor

The sol-gel Alumina was prepared by dissolving the Aluminium nitrate nonahydrate (solute) (Al(NO₃)₃.9H₂O) (from Sigma Aldrich ) in Iso-propyl alcohol (solvent). The choice of the salt was due to its low thermal decomposition temperature (200°C) [25]. The resultant mixture was stirred at 1000 rpm at 55°C for one hour to dissolve the salt completely in solvent. In addition to that, the chelating agent Acetyl-acetone was added to the above solution and stirred for 12 hours and the resultant solution was kept to aging for 3 days. The addition of chelating agent to the solution could reduce the residual stress during the annealing process [28]. These chelating coordination bonds hinder the hydrolysis and/or poly condensation, making the gel network flexible, and allowing structural relaxation in films during annealing and also enhance the DUV absorption [28]. The resultant solution was filtered using membrane filter 0.22 µm and used for the deposition on the fabricated devices. The solution was prepared for different molarities of 0.1 M and 0.05 M was spin coated on RCA cleaned silicon wafers followed by the drying at 110°C for 15 minutes. The Deep Ultra violet (DUV) annealing (Figure 1 (c)) has been performed in UV Ozone cleaner (Jelight company Inc.) with intensity of 11 mW/cm² in N₂ ambience for the densification of the sol-gel Alumina. The unintentional heating temperature during DUV annealing was around 70°C and measured using the thermocouple inside the chamber during annealing process.

2.2. Fabrication of graphene FETs

The 3-D schematic process flow for sol-gel Alumina passivation layer based GFETs is shown in Figure 1. We have purchased graphene monolayer grown on a copper foil using a CVD process from Graphenea Inc. Primarily, we prepared a carrier substrate to transfer the graphene layer from copper foil. An RCA cleaned 2-inch silicon wafer with resistivity 0.001-0.005 Ω-cm, was used as a carrier substrate. To provide reliable isolation from the substrate and enable an optical contrast to spot the graphene monolayer, we have thermally grown 90 nm SiO₂ on the carrier wafer. Next, we have transferred the graphene monolayer on the SiO₂ layer. The large area Graphene monolayer was patterned to respective channel lengths and widths using photo-lithography followed by Oxygen plasma exposure for 5 min with RF power of 50 Watts. After the stripping of the resist (AZ 5214E) in AZ 100 remover, the sample was patterned for contacts. The stack of Ni/Au (20 nm / 30 nm) contact was deposited using an Electron beam evaporator at the 2.2X10⁻⁸ torr vacuum followed by lift-off. After that, the electrical characteristics of as-fabricated GFET were performed. Next, the sequential deposition of the seed layer of thickness 1.5 nm from the E-beam evaporation and 1.5 nm from the sputtering was performed. After that, the prepared sol-gel solution of different molarities was spin-coated at 5000 rpm for 45 seconds followed by drying at 110°C. Then the DUV annealing was performed, followed by the patterning of the film for contacts opening using 7:1 BHF as shown in the Figure 1 (h).

2.3. Characterization

The Microscope images were taken using an Olympus microscope. The Scannig Electron Microscopy (SEM) image was performed using JEOL JSM-7600F FEG-SEM. The Atomic Force Microscopy (AFM) was
performed using tapping mode using MFP-3D AFM, Asylum research, Oxford instruments. The UV-VIS spectroscopy was performed on the sol-gel Alumina solution using a Perkin-Elmer UV-VIS-NIR spectrometer. The X-ray Photoelectron Spectroscopy (XPS) of the sol-gel Alumina film samples was studied using PHI 5000 versa probe II with monochromatic Al Kα X-ray source. The thickness measurement was analyzed using an ellipsometer from SENTECH instruments. The electrical characterization on the respective samples was done using a Keysight B1500A semiconductor device analyzer.

3. Results and discussion

3.1. Process yield and device reliability study at 0.1 M

To check if DUV is an effective annealing technique for sol-gel Alumina film, the absorbance of precursor solution was carried out using UV-VIS spectroscopy between 200-800 nm (Figure 2(a)). The absorbance peak in the range of 200-300 nm confirms that DUV will be an effective technique to anneal sol-gel Alumina film. To further find out the optimized DUV annealing time which can completely remove solvent from the film, annealing time splits were carried out on blanket deposited film. The pre and post-annealing film thicknesses were measured using ellipsometry, and the shrinkage ratio was extracted as shown in Figure 2(b). The thickness reduction of sol-gel is due to the accelerated polycondensation process due to the formation of OH radicals [35, 30]. In the reported work, the Aluminium nitrate nonahydrate salt will dissociate and give NO₂ and OH radicals as shown below.

It can be seen from Figure 2(b) that (i) average thickness of pre-annealing films across different samples is 82 nm, (ii) as the annealing time increases, the film thickness reduces till 40 minutes, beyond which the film thickness got saturated to 30 nm, and there was no more thickness reduction and (iii) the shrinkage ratio of 0.1 M film is close to 60%, which means that there was a significant amount of solvent present in the film and hence it might be taking longer time to remove the solvent altogether. This could lead to higher shrinkage stress due to a longer annealing time.

The GFETs were fabricated with DUV annealing of
20 minutes. The optical microscopic picture of sample with array of GFETs was shown in Figure 3 (a). When the devices were inspected at 50X, it was found that some of the devices had crack (Figure 3 (e)) in the sol-gel film post-annealing, and some of them did not have the crack (Figure 3 (d)). The devices were also inspected, and crack formation was confirmed using SEM images shown in Figure 3 (e) (without crack) and Figure 3 (f) (with crack). This crack formation could be due to the combined effect of inadequate densification of the sol-gel precursor, insufficient removal of the solvents and the stress due to shrinkage during DUV annealing.

Figure 3 (a) shows the DC transfer characteristics of the graphene FET before and after sol-gel deposition. The mobilities of both hole and electron branches were found to be 2025 cm²/V-sec and 2315 cm²/V-sec for as-fabricated GFET. The mobilities have been extracted from the FTM method [36]. The As fabricated GFET shows n-type doping which was shown as a shift in the Dirac point towards negative voltage i.e. at -6.8 V, which could be due to photo-resist stripper [37] and the asymmetry in transfer characteristics and lower conductance in the electron branch could be due to work-function difference between contacts and graphene [38].

After sol-gel Alumina deposition followed by DUV annealing, the hole and electron mobilities were degraded and have been found to be 481.8 cm²/V-sec and 412.7 cm²/V-sec. This could be due to increase of the charge impurity scattering [39]. These scatters were formed due to the OH ion generation during the redox reaction from the diffusion of O₂ and H₂O from the atmosphere through the grain boundaries of sol-gel Alumina layer, or it could be due to trapped solvents in the metal oxide network which could act as a remote coulomb scatters. The trapped solvents could also form the redox reaction with the electrons at the graphene interface leading to OH scatters causing the degradation [21]. The transfer characteristics got further degraded after one week, causing the degradation of hole and electron branch with mobilities of 289.8 cm²/V-sec and 270.5 cm²/V-sec. This could be due to diffusion of the H₂O and O₂ from the ambient atmosphere through the
grain boundaries [21] of sol-gel Alumina layer, causing more degradation with time which can also be supported by a shift in Dirac point towards positive voltage direction showing P-type nature. The width of DC-IV characteristics around Dirac point ($\Delta V_{g\text{-}min}$) broadens after one week which could be due to increase in concentration of charge impurities ($n_{\text{imp}}$) [39] and the values of $\Delta V_{g\text{-}min}$ were extracted by intersecting a line through the minimum conductivity around Dirac point [40] as shown in the table.

![Figure 4: (a) DC-IV characteristics of GFET before and after sol-gel deposition with 0.1 M molarity (b) DC-IV hysteresis characteristics before and after Alumina deposition with 0.1 M molarity](image)

The minimum conductivity ($\sigma_{\text{min}}$) reduction after DUV annealing and one week also reveals that the sample has become dirtier as per adam et.al [41] which means there were more concentration of charged impurities ($n_{\text{imp}}$) [41].

To further explore, the hysteresis has been explored as shown in Figure 4 (b). The hysteresis characteristics show the positive direction of hysteresis [42] before and after DUV annealed sol-gel Alumina layer. The hysteresis could be due to both redox and charge tunneling components [43]. The hysteresis has increased after DUV annealing treatment which can be anticipated due to an increase in both the redox and tunneling components [43]. This has been shown through the charge trap density at the graphene interface from the equation $N_{\text{trap}}=C_{\text{ox}}*(\Delta V_{\text{Dirac}})/q$ where $C_{\text{ox}}$ os the SiO$_2$ oxide capacitance and $\Delta V_{\text{Dirac}}$ is the difference in the voltages at the Dirac point. The charge trap density for the as fabricated GFET was $2.9\times10^{12}$/cm$^2$ for the $\Delta V_{\text{Dirac}}$ of 12.4 V and after the DUV annealing was $4.5\times10^{12}$/cm$^2$ for the $\Delta V_{\text{Dirac}}$ of 19.2 V. However, after one week, the hysteresis has reduced i.e. $\Delta V_{\text{Dirac}}$ of 14.4 V resulting charge trap density of $3.37\times10^{12}$/cm$^2$, which could be due to partial reduction of tunneling component i.e. the charge trapping (fast component) into adsorbates (H$_2$O) [43] which means the H$_2$O has been utilized for the formation of OH$^-$ ion generation through redox reaction (slow component), which has degraded the mobility as shown in the Figure 4 (a). The extracted parameters from transfer and hysteresis characteristics have been tabulated in table.

### Table 1: Parameter extraction of GFET with 0.1 M sol-gel Alumina

| Parameters | As fabricated GFET | After DUV annealing | After one week |
|------------|------------------|---------------------|------------|
| $\mu_h$ (cm$^2$/V-sec) | 2025 | 481.5 | 289.5 |
| $\mu_e$ (cm$^2$/V-sec) | 2315 | 412.7 | 270.5 |
| $\Delta V_{g\text{-}min}$ (V) | 5.4 | 8.4 | 12.3 |
| $\sigma_{\text{min}}$ (q/cm$^2$/h) | 4.75 | 1.45 | 1.37 |
| $\Delta V_{\text{Dirac}}$ (V) | 12.4 | 19.2 | 14.4 |
| $N_{\text{trap}}$ (/cm$^2$) | 2.9e12 | 4.5e12 | 3.37e12 |

Based on the above discussion, there were two problems, (i) process yield was not good as many devices shows crack in sol-gel Alumina layer above graphene channel and (ii) device stability is not good, and keeps degrading in terms of absolute current and mobility. In order to resolve the issues, we propose sol-gel Alumina with low molarity (0.05M).
3.2. Process yield and device reliability study at 0.05 M

To circumvent the shrinkage stress with 0.1 M, the sol-gel Alumina molarity has been reduced to 0.05 M. Figure 5(a) shows the annealing time optimization of the 0.05 M sol-gel Alumina respectively with different DUV annealing time (For reference, the hot plate drying is carried at 100°C for 15 minutes and also 60 minutes). The final thickness obtained after DUV annealing time was around 22 nm. The shrinkage ratio with DUV annealing time was also plotted, showing that the thickness got saturated at 50% at 10 minutes showing less shrinkage stress during DUV annealing. To explore the stochiometry of sol-gel Alumina after the DUV annealing, XPS measurement was performed on the samples and oxygen (O 1s) peak is deconvoluted for Al-O-Al peak and Al-OH at 531.0 and 532.3 respectively, as shown in the Figure 5(b). After the deconvolution, the Al-O-Al concentration and Al-OH concentration is plotted as a function of DUV annealing time as shown in Figure 5(c) and (d). The zero minute sample in Figure 5(c) and (d) is as-spun coated followed by drying on a hotplate at 100°C for 15 minutes. From the graph 5(c) and (d), it was conveyed that the Al-O-Al and Al-OH concentration is almost constant after the 20 minutes. To investigate the effect and advantage of DUV annealing, the sample was kept on a hot plate at 100°C for 60 minutes.

During the DUV annealing process, the sample will undergo unintentional heating to around 75-80 °C. Still, to see the effect of DUV annealing on the densification
process, the hot plate treated sample for 60 min at 100°C was investigated to have a fair comparison. It didn’t show much change in the Al-O-Al and Al-OH concentration even after 60 minutes. However, the DUV annealed sample at 60 minutes showed the reduction in Al-OH concentration as shown in Figure 5 (c) and (d).

Optical image in Figure 6(a) shows sample with 100% yield concerning crack removal in the sol-gel Alumina layer on the graphene channel. This could be due to the reduction of shrinkage stress component with 0.05 M. Figure 6 (b) shows the enlarged version of one of the devices showing no crack in the active region. This can be further confirmed from the SEM, as shown in the Figure 6 (c).

Figure 7 (a) shows the DC transfer characteristics of GFET before and after sol-gel deposition. The As fabricated GFET shows n-type doping, which has been established as a shift in the Dirac point towards negative voltage, i.e., at -10.8 V, which could be due to resist stripper [37] and the asymmetry in transfer characteristics and lower conductance in the electron branch was due to the work-function difference [38].

After the DUV annealing of sol-gel Alumina for 20 minutes, there is a slight shift in the Dirac point. The decrease of the mobility in electron and hole branch, which inherently decreases current, the broadening of minimum conductivity plateau in the transfer characteristics have been observed. The shift in the Dirac point was at -6.4 eV, which shows the graphene FET is still n-type doped. The mobility has been extracted from the FTM method [36]. The hole and electron mobility before sol-gel deposition were 2670 cm²/V-sec and 2839 cm²/V-sec. The hole and electron mobility after the sol-gel deposition were 1081 cm²/V-sec and 1319 cm²/V-sec, and the same mobilities were maintained for two months. This shows that the 0.05 M sol-gel Alumina layer does not degrade the hole and electron mobilities compared to the 0.1 M sol-gel Alumina layer. Hence the device stability has improved compare to 0.1 M based GFETs.

Figure 7 (b) shows the hysteresis transfer characteristics that show the positive direction of hysteresis [42]. The hysteresis has been contributed from charge tunneling into the adsorbates (fast component) and redox couple reaction (slow component) [43]. The charge trap density for the as fabricated GFET was $4.21 \times 10^{12}$/cm² for the $\Delta V_{\text{Dirac}}$ of 18 V and after the DUV annealing was $4.02 \times 10^{12}$/cm² for the $\Delta V_{\text{Dirac}}$ of 17.2 V. The minute reduction in charge trap density after the DUV annealing could be due to removal of water and oxygen to some extent from the oxide network.

In order to further explore about the hysteresis, pulse IV characterisation has been performed with SMU pulse with the pulse width of 500 µsec on graphene FET before and after sol-gel Alumina deposition as shown in the Figure 7 (c). The charge trap density for the as fabricated GFET was $8.42 \times 10^{11}$/cm² for the $\Delta V_{\text{Dirac}}$ of 3.6 V and after the Alumina deposition charge trap density was $1.02 \times 10^{12}$/cm² for the $\Delta V_{\text{Dirac}}$ of 4.4 V which shows less hysteresis. As the pulse IV characterization is time dependant measurement and the pulse width of 500 µs. It will bypass the slow component (redox component), leaving the fast component leading to more negligible hysteresis. The extracted parameters from transfer and hysteresis characteristics have been tabulated in table 2.

The broadening of the minimum conductivity plateau in transfer characteristics was due to dominant charge impurity scattering from the dielectric [41]. To support this argument, the XPS in Figure 5(b) shows that there was still OH concentration even after the 20 minutes. These OH present in the oxide could act as charge im-
purities and scatter the carrier in the graphene channel. These scatters could act as charge impurities at the interface and as scattering centers leading to the reduction in the mobilities [45]. Table 3 shows the summary of passivation layer-based GFETs using different deposition techniques. It can be seen that the present work of GFETs with 0.05M sol-gel alumina-based passivation layer is a low-temperature-based process with reasonably good mobility values when compared to others. The process also has 100% yield with excellent device stability for more than two months.

### 4. Conclusion

The low-cost and low-temperature sol-gel alumina passivation layer was explored with the goal of improving the process yield and device stability of GFET devices. The 0.1 M-based passivation layer led to two problems, (i) process yield was poor as almost half of the devices exhibited crack formation in the channel region, and (ii) the remaining half of working devices showed poor stability, as they degraded in a short time of one week. The degradation has caused a decrease in electron and hole branch of drain current by one order, decreasing mobility by seven times with time respectively. The hypothesis for poor yield and stability was thought to be stress generated during densification annealing of the film. Hence we proposed a film with lower molarity of 0.05 M, which has led to improved process yield with 100% working devices without crack, and working devices are also showing good stability even after two months. The devices show no further degradation in drain current, mobility, and trap density. Hence in this work, we proposed an optimized sol-gel alumina passivation layer recipe to achieve the best yield with good stability. The table shows a comparison of our work some of the other reported work. The proposed solution can pave the way to make low-cost and low-temperature-based sol-gel alumina-based GFETs for various applications.

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Table 3: Benchmark table for different Alumina deposition on GFETs and their extracted mobilities

| Ref | Graphene type | Type of gate | W/L (µm/µm) | Type of deposition | Process temperature (°C) | Mobility (cm²/V-sec) (Before deposition) | Mobility (cm²/V-sec) (After deposition) |
|-----|---------------|--------------|-------------|-------------------|----------------------------|------------------------------------------|----------------------------------------|
|     |               |              |             |                   |                            | µh | e   | µh | e   |
| [34] | CVD            | Back gate    | 10/10       | Sol-gel Alumina + Hot plate annealing | 250                         | NA | NA | 550 | NA |
| [32] | Mechanical exfoliation | Top gate | 40/2         | Sol-gel Alumina + Hot plate annealing | 250                         | NA | NA | NA | 9000 |
| [33] | Epitaxial growth on SiC | Top gate | 1/1          | Sol-gel Alumina + Microwave annealing | 500                         | NA | NA | 8.6 | 9.7 |
| [10] | CVD            | Back gate    | 10/25       | Thermal ALD       | 150                        | NA | NA | 5000 | 5000 |
| [21] | CVD            | Back gate    | 2/2          | Thermal ALD       | 150                        | 1730 | 161 | 1524 | 1310 |
| [23] | CVD            | Back gate    | 30/9         | Thermal ALD       | 130                        | NA | NA | NA | 8600 |
| [20] | Mechanical exfoliation | Back gate | 2.5/2.5    | Thermal ALD       | 150                        | NA | NA | NA | 3000 |
| [44] | Epitaxial grown on SiC | Back gate | 10/10   | Anodic Oxidation | NA                         | NA | NA | NA | 120 |
| Present work | CVD            | Back gate    | 5/30        | Sol-gel Alumina + DUV annealing | 70                         | 2670 | 2839 | 1081 | 1319 |
