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Improved and accurate low-frequency average modelling and control of a conventional power factor correction boost converter in continuous conduction mode

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Abstract
When dealing with power factor correction (PFC) rectifiers that require the use of high filter capacitances, conventional small-signal modelling techniques are not capable of reproducing the converter behaviour accurately owing to the impact of the low-frequency dynamics on the system. In this context, this work presents an improved modelling technique applied to a conventional PFC boost converter operating in continuous conduction mode (CCM). The proposed approach leads to a more accurate analysis than the traditional modelling developed for dc–dc converters, which is often extended to rectifiers. It consists of a fast and concise solution for the implementation of several PFC techniques from the derived transfer functions. The introduced method is described aiming at the development of a boost-based PFC stage using the well-known one-cycle control technique (OCC). Simulation and experimental results are presented and thoroughly discussed to validate the theoretical assumptions.

1 INTRODUCTION

Power factor correction (PFC) rectifiers are employed as front-end stages in a wide variety of applications, which include battery chargers, switch-mode power supplies (SMPSs), uninterruptible power supplies (UPSs), motor drives, renewable energy conversion systems, light-emitting diode (LED) drivers, among many others [1]. Such converters are capable of providing nearly sinusoidal currents drawn from the ac mains, which remain in phase with the supply voltages and present reduced harmonic content [2].

For applications rated above a few hundred watts, PFC rectifiers operating in continuous conduction mode (CCM) are better recommended owing to lower current stresses on the semiconductors when compared with the discontinuous conduction mode (DCM) [3]. For this purpose, a closed-loop control system is required to allow emulating the behaviour of a resistive load and achieving compliance with international standards such as IEC 61000-3-2 and IEC 61000-3-4 [4, 5]. Several control techniques have been proposed so far in the literature, which can be implemented using either analogue or digital circuits [6]. Besides, it is possible to classify the aforementioned control approaches basically into two types: direct and indirect. Direct techniques require sensing the rectified input voltage to provide a sinusoidal shape to be imposed to the filter inductor current. Average current mode control (ACMC), peak current mode control (PCMC), and hysteresis control (HC) rely on this operating principle [7]. On the other hand, the so-called indirect techniques do not require a sample of the rectified line voltage and typically present reduced implementation complexity when compared with their direct counterparts. This is the case of one-cycle control (OCC) and self-control (SC), which were introduced in [8] and [9], respectively. Considering that the aforementioned techniques rely on the implementation of closed-loop control systems, it is necessary to determine some relevant transfer functions for this purpose. However, most datasheets and application notes provided by manufacturers of commercial integrated circuits (ICs) contain limited information on this...
topic. In this context, small-signal modelling is an important tool that allows determining distinct mathematical expressions involving variables of interest. For instance, the implementation of ACMC depends on two transfer functions associated with the cascaded control loops, i.e., control-to-inductor current and inductor current-to-output. On the other hand, the OCC technique does only require the knowledge of the inductor current-to-output transfer function, which is associated with the dc-link voltage control [9].

Average state-space modelling is perhaps the most popular technique used for this purpose [10–12]. This general-purpose technique can be employed in a wide variety of practical applications, which include some very specific approaches, e.g., the analysis of dc–dc converters operating with current-mode control in [13]. However, it relies on a significant amount of mathematical manipulations in a quite time-consuming task, which becomes more complex as the system order increases.

It is possible to obtain the very same results with the pulse width modulation (PWM) switch model. It allows determining both dc and ac small-signal models of dc–dc converters operating in CCM [14] and DCM [15], but using only basic concepts involving electric circuits theory. Besides, it can be fairly extended to the analysis of other topologies, which also include PFC rectifiers [16].

Since the switching frequency is much higher than the line frequency, the input voltage is considered constant over one switching period and the PFC rectifier can be analysed analogously to a dc–dc converter. However, PFC rectifiers often require high capacitances, i.e. rated at hundreds of microfarads to some millifarads depending on the application. Such filter elements are used to attenuate the low-frequency ripple at twice the line frequency that appears in the dc-link voltage waveform. Under this condition, both the aforementioned small-signal modelling techniques do not lead to accurate results [17]. This aspect motivated the studies developed in [18] and [19], which are dedicated to PFC converters operating in CCM. These works aim at improving the modelling analysis by incorporating the low-frequency dynamics into the system, even though the applied methods are quite complex and not intuitive. The small-signal models derived in [18] and [19] rely on a large-signal representation and high-time consuming calculations involving both the converter and PWM circuit. In either case, the small-signal model is linearized around an operation point.

On the other hand, the work presented in [20] is simply based on circuit averaging, which makes the modelling technique more intuitive for an application engineer. Even though the authors claim that it can be applied to any topology, only the small-signal modeling of PFC rectifiers in DCM was addressed. Considering that a concise and similar modelling approach for the operation of PFC rectifiers in CCM was not presented so far, the main contribution of this work lies in the introduction of a simple and straightforward methodology that takes into account the low-frequency ripple of the dc-link voltage. Thus, it is possible to obtain the desired transfer functions for the implementation of the closed-loop control system of PFC converters in CCM.

The remainder of this work is organized as follows. The OCC technique applied to a PFC boost converter in CCM is analysed in detail in Section 2. The proposed modelling technique is introduced in Section 3, while the main characteristics and parameters for the model validation are presented in Section 4. Section 5 addresses a design example involving the derived methodology to provide high input power factor and regulated dc-link voltage. Furthermore, experimental validation is accomplished in Section 6, where results on a laboratory prototype are thoroughly evaluated. Finally, remarkable conclusions are given in Section 7, while the main aspects and contributions are discussed.

2 | BRIEF ANALYSIS OF THE PFC BOOST CONVERTER IN CCM

The simplest solution for the implementation of a general-purpose switched-mode power supply SMPS relies on single-stage converters, since they can provide high input power factor, output voltage control, low component count, and reduced low-frequency ripple, although they generally require the use of high dc-link filter capacitances [21]. Besides, a high-voltage dc link can be employed depending on the application, while the low-frequency filtering capacitance will be significantly reduced in this case, which may enable the use of long-life film capacitors.

The ac–dc single-stage boost converter in CCM is perhaps the most popular solution for overall PFC applications rated at a few hundred watts owing to inherent simplicity, reduced number of power stage elements, and the continuous nature of the input current. Besides, it leads to reduced current stresses on the semiconductors, which are proportional to the input current. The conventional ac–dc boost configuration is presented in Figure 1, where PFC can be achieved using distinct control techniques. Even though ACMC is the most popular approach owing to the wide availability of dedicated commercial ICs, the control system implementation aggregates increased complexity and higher component count [7]. Indirect techniques such as the OCC are capable of overcoming such drawbacks, since they do not require multipliers, dividers, and a sample of the rectified input voltage [8]. IR1150 is the only commercial IC dedicated to OCC and will be used in this work as described in the forthcoming sections [22].

The expressions for calculating the filter elements of the ac–dc boost converter, i.e. $L_d$ and $C_d$ are given by Equations (1)
and (2), respectively [23].

\[ I_{ls} = \frac{V_g}{f_s(PFC)} \frac{\Delta I_{lb}}{\Delta I_{lb}} \]  

(1)

\[ C_{dc} = \frac{P_o}{2 \cdot (2\pi f_i) \cdot V_{dc} \cdot \Delta V_{dc}} \]  

(2)

where:

\[ \beta = \frac{V_{dc}}{V_g} \]  

(3)

\[ \Delta I_{lb} = \frac{\beta}{4} \]  

(4)

Besides, \( V_g \) is the peak value of the input voltage; \( f_s(PFC) \) is the switching frequency; \( \Delta I_{lb} \) is the normalized inductor current ripple defined according to parameter \( \beta \); \( \Delta I_{lb} \) is the inductor current ripple at the peak grid voltage; \( P_o \) is the rated output power, \( f_i \) is the line frequency; \( V_{dc} \) is the average dc-link voltage; and \( \Delta V_{dc} \) is the dc-link voltage ripple.

The development of a simplified PFC small-signal modelling approach applied to the ac-de boost converter will be presented in the forthcoming section. As previously mentioned, this technique considers the low-frequency dynamics associated with the ac mains and the eventual need for high dc-link capacitances used in the implementation of distinct control techniques.

### 3 | SMALL-SIGNAL MODELLING TECHNIQUE FOR PFC CONVERTERS IN CCM

In PFC converters operating in CCM, the low-frequency component is the dominant portion in the dc-link voltage, since it influences the dynamic behaviour of the whole system directly. Therefore, the modelling methodology can be better represented in terms of an average analysis carried out for a half period of the ac grid voltage. It consists in substituting the switching elements, i.e. the active switch and diode by controlled current sources, which represent small-signal disturbances in the average currents through the semiconductors. Then, this model can be employed to analyse the influence of disturbances on the PFC converter.

First, let us consider a PFC boost converter in CCM, as some key parameters must be defined. Some typical low-frequency and high-frequency waveforms are represented in Figure 2, from which important expressions can be obtained. The rectified sinusoidal input voltage and the duty cycle, which are both time-variant, are given by Equations (5) and (6), respectively.

\[ v_g(t) = V_g \cdot \sin(\omega_L t) \]  

(5)

\[ \frac{V_{dc}}{V_g \cdot \sin(\omega_L t)} = \frac{1}{1 - d(t)} \implies d(t) = 1 - \frac{V_g \cdot \sin(\omega_L t)}{V_{dc}} \]  

(6)

The developed waveforms of a PFC boost rectifier in CCM (Figure 2) and (2), respectively [23].

\[ \langle i_{ls} \rangle_{Ts} = I_{lb} \cdot \sin(\theta), \quad 0 < \theta < \pi \]  

(7)

where \( v_g(t) \) is the instantaneous input voltage; \( \omega_L = 2\pi f_i \) is the line angular frequency in rad/s; and \( d(t) \) is the time-variant duty cycle.

In the presented approach, the inductor current is considered constant over the switching period \( T_s \), thus simplifying the analysis. Then, the average value of the instantaneous inductor current can be properly represented by a rectified sinusoidal waveform considering only the positive half cycle of the grid voltage. The average values of the instantaneous inductor current and instantaneous input voltage are then described by Equation (7).

\[ \langle i_{ls} \rangle_{Ts} = I_{lb} \cdot \sin(\theta), \quad 0 < \theta < \pi \]  

(7)

\[ \langle i_{ls} \rangle_{Ts} = \frac{I_{lb} \cdot \sin(\theta)}{1 - d(t)} \cdot \langle i_{lb} \rangle_{Ts} \]  

(8)

Substituting the duty cycle and the inductor current represented by Equations (6) and (7) in Equation (8), respectively, Equation (9) can then be obtained.

\[ \langle i_S \rangle_{Ts} = \left(1 - \frac{V_g \cdot \sin(\theta)}{V_{dc}}\right) \cdot \langle i_{lb} \rangle_{Ts} \]  

(9)

The relationships in Equation (9) must be then integrated while considering one period of the rectified input voltage, i.e. \( T_s/2 = 1/(2\pi f_i) \), resulting in the average currents through the
active switch and diode given in Equations (10) and (11), respectively. Thus, Equations (10) and (11) describe the currents in terms of both high-frequency and low-frequency components.

\[
I_S = \left(\langle i_S^b \rangle_{T_f/2} \right) = \frac{1}{\pi} \int_0^{\pi} \langle i_S^b \rangle_{T_f}(\Theta) \, d\Theta
\]
\[
I_S = \frac{1}{\pi} \int_0^{\pi} \left[ \left( I_{lb} \cdot \frac{V_g}{V_d} \right) \sin(\Theta) \right] \, d\Theta
\]
\[
I_S = I_{lb} \cdot \left( \frac{2}{\pi} - \frac{V_g}{2V_d} \right)
\]

\[
I_D = \left(\langle i_D^b \rangle_{T_f/2} \right) = \frac{1}{\pi} \int_0^{\pi} \langle i_D^b \rangle_{T_f}(\Theta) \, d\Theta
\]
\[
I_D = \frac{1}{\pi} \int_0^{\pi} \left[ \left( I_{lb} \cdot \frac{V_g}{V_d} \right) \sin(\Theta) \right] \, d\Theta
\]
\[
I_D = \frac{I_{lb} \cdot V_g}{2V_d}
\]

The average small-signal model is based on perturbing and linearizing the average circuit variables so that they can be represented in the frequency domain. Therefore, the Laplace representation for the average currents can be obtained by adding disturbances to each input parameter. Considering the active switch, the disturbance is given by Equation (12).

\[
\Delta \left(\langle i_S^b \rangle_{T_f/2} \right) = G_{SG} \cdot \Delta v_g + G_{SO} \cdot \Delta v_{dc} + G_{SI} \cdot \Delta i_{lb}
\]

where \(G_{SG}, G_{SO}\), and \(G_{SI}\) are the partial derivatives of the active switch current with respect to the input voltage, output voltage, and inductor current, respectively; \(\Delta v_g, \Delta v_{dc}\), and \(\Delta i_{lb}\) are the disturbances associated with the input voltage, dc-link voltage, and inductor current, respectively.

The time-dependent expression can then be represented in the frequency domain as in Equation (13).

\[
i_S(\tau) = G_{SG} \cdot \delta(\tau) + G_{SO} \cdot \delta_{dc}(\tau) + G_{SI} \cdot \delta_{lb}(\tau)
\]

where \(\delta(\tau), \delta_{dc}(\tau)\), and \(\delta_{lb}(\tau)\) correspond to the input voltage, output voltage, and inductor current represented in the frequency domain, respectively.

The partial derivatives of the switch current must be solved for each particular case while considering the linearized operating point. Therefore, Equations (14)–(16) result from the substitution of Equation (12) in (10).

\[
G_{SG} = \frac{\partial}{\partial V_g} \left[ I_{lb} \left( \frac{2}{\pi} - \frac{V_g}{2V_d} \right) \right] = \frac{I_{lb}}{2V_d}
\]

\[
G_{SO} = \frac{\partial}{\partial V_{dc}} \left[ I_{lb} \left( \frac{2}{\pi} - \frac{V_g}{2V_d} \right) \right] = \frac{I_{lb} \cdot V_g}{2V_{dc}^2}
\]

\[
G_{SI} = \frac{\partial}{\partial i_{lb}} \left[ I_{lb} \left( \frac{2}{\pi} - \frac{V_g}{2V_d} \right) \right] = \frac{2}{\pi} - \frac{V_g}{2V_d}
\]

The same analysis can be performed in the frequency domain for the passive switch, i.e. the diode according to Equation (17), resulting in Equation (18).

\[
\Delta \left(\langle i_D^b \rangle_{T_f/2} \right) = G_{DG} \cdot \delta_g + G_{DO} \cdot \delta_{dc} + G_{DI} \cdot \delta_{lb}
\]

where \(G_{DG}, G_{DO}\), and \(G_{DI}\) are the partial derivatives of the diode current with respect to the input voltage, output voltage, and inductor current, respectively.

\[
i_D(\tau) = G_{DG} \cdot \delta_g(\tau) + G_{DO} \cdot \delta_{dc}(\tau) + G_{DI} \cdot \delta_{lb}(\tau)
\]

Substituting Equation (17) in (11), the partial derivatives of the diode current can be obtained by Equations (19) to (21).

\[
G_{DG} = \frac{\partial}{\partial V_g} \left[ \frac{I_{lb} \cdot V_g}{2V_d} \right] = \frac{I_{lb}}{2V_d}
\]

\[
G_{DO} = \frac{\partial}{\partial V_{dc}} \left[ \frac{I_{lb} \cdot V_g}{2V_d} \right] = -\frac{I_{lb} \cdot V_g}{2V_{dc}^2}
\]

\[
G_{DI} = \frac{\partial}{\partial i_{lb}} \left[ \frac{I_{lb} \cdot V_g}{2V_d} \right] = \frac{V_g}{2V_d}
\]

The peak inductor current \(I_{lb}\) can be calculated from the power balance applied to this element as described by Equation (22).

\[
\frac{I_{lb} \cdot V_g}{2} = P_o \cdot A_{lb} = \frac{2 \cdot P_o}{V_g}
\]

As long as \(i_S(\tau)\) and \(i_D(\tau)\) are defined in the frequency domain, an equivalent average circuit can be proposed as in Figure 3, where \(R_{eq}\) is the equivalent load resistance. Thus, the average small-signal model of the PFC stage can be obtained applying Kirchhoff's circuit laws to obtain the desired transfer functions.

It is well known that the series resistance of the boost inductor does not influence the dynamic response of the boost converter significantly, but only the voltage conversion ratio, while it can be neglected in the proposed modelling as suggested by [18, 19]. On the other hand, the equivalent series resistance (ESR) of the dc-link capacitor must be properly analysed.
depending on the construction technology. Metallized polypropylene film (MPF) capacitors present prominent advantages regarding long lifespan and extremely low ESR values when compared with their electrolytic counterparts [24]. Consequently, such parasitic element can be neglected in the desired transfer functions for particular applications that employ only long-life film capacitors in the dc link, mainly when high voltage levels exist as it was previously stated in Section 2, thus simplifying the analysis drastically. Otherwise, in applications where the use of electrolytic capacitors is inevitable, their respective ESRs should be properly incorporated to the model.

The ratio between the output voltage and the input voltage can be determined by analysing the output node of the circuit in Figure 3 while neglecting the inductor-current-dependent portion in this case, resulting in Equation (23), which can be solved to obtain $\frac{v_{dc}(s)}{v_{g}}$ as in Equation (24). On the other hand, if the capacitor ESR should in fact be considered in a given application, this particular transfer function will be given by Equation (25), which of course can be simplified in terms of Equation (22) when the ESR is negligible.

$$G_{Dg} \cdot \frac{v_{dc}(s)}{v_{g}} + G_{Do} \cdot v_{dc}(s) = v_{dc}(s) \left( \frac{1}{R_{o(eq)}} + \frac{s}{C_{dc}} \right)$$ (23)

$$M_{v} \left( s \right) = \frac{v_{dc}(s)}{v_{g}} = \frac{R_{o(eq)} \cdot G_{Dg}}{1 - R_{o(eq)} \cdot G_{Do} + s \left( R_{o(eq)} \cdot C_{dc} \right)}$$ (24)

$$M_{v(ESR)} \left( s \right) = \frac{v_{dc}(s)}{v_{g}} = \frac{R_{o(eq)} \cdot G_{Dg}}{1 - R_{o(eq)} \cdot G_{Do} + \frac{s \left( R_{o(eq)} \cdot C_{dc} \right)}{R_{o(eq)} \cdot C_{dc} + 1}}$$ (25)

A general-purpose block diagram regarding the development of current-mode control techniques is presented in Figure 4, where $H_{L}$ and $H_{m}$ represent the sampling gains of the inductor current and dc-link voltage, respectively. The transfer function of the inductor current to the output voltage, i.e., $Z_{v}(s)$, must be determined in Figure 5 for the implementation of the control law associated with the external voltage loop. At this point, it is important to observe that this particular control loop is the one that incorporates the low-frequency dynamics of the system, while its transfer function is then required to control the output voltage accurately in a PFC rectifier.

In order to obtain $Z_{v}(s)$, the output in Figure 3 can also be analysed while neglecting the term that depends on the input voltage. For this purpose, Equation (26) must be considered, which results in Equation (27) after some algebra. Also in this case, if the filter capacitor ESR is supposed to be considered in a particular application, such transfer function can be modified to reflect its influence as in Equation (28).

$$G_{D0} \cdot v_{dc}(s) + G_{Di} \cdot \frac{v_{dc}}{v_{g}}(s) = v_{dc}(s) \left( \frac{1}{R_{o(eq)}} + \frac{s}{C_{dc}} \right)$$ (26)

$$Z_{v}(s) = \frac{v_{dc}(s)}{\frac{v_{dc}}{v_{g}}(s)} = \frac{R_{o(eq)} \cdot G_{Di}}{1 - R_{o(eq)} \cdot G_{Do} + s \left( R_{o(eq)} \cdot C_{dc} \right)}$$ (27)

$$Z_{v(ESR)}(s) = \frac{v_{dc}(s)}{\frac{v_{dc}}{v_{g}}(s)} = \frac{R_{o(eq)} \cdot G_{Di}}{1 - R_{o(eq)} \cdot G_{Do} + \frac{s \left( R_{o(eq)} \cdot C_{dc} \right)}{R_{o(eq)} \cdot C_{dc} + 1}}$$ (28)

4 | MODEL VALIDATION BY SIMULATION USING OCC

As previously mentioned, IC IR1150 is employed in this work, which performs PFC particularly using the OCC technique. In this case, the inner current loop compensator $C_{i}(s)$ is dynamically controlled by the user [25]. However, the external voltage loop $C_{v}(s)$ must be designed according to the transfer function $Z_{v}(s)$.

The operating principle of OCC is presented in Figure 5. Considering this simplified schematic, the dc-link voltage $V_{dc}$ can be sensed with linear voltage sensors, e.g., a resistive divider, and compared with a reference signal $V_{dc(Ref)}$, resulting in an input error signal for the proportional-integral (PI) controller. Since $V_{dc}$ varies slowly, this signal can be considered constant over the switching period and used to provide a linear ramp from a set-reset (SR)
frequency ripple at the inverter. From the analysis of Equation (2), it is reasonable to state that high capacitances are often required to minimize the low-frequency ripple at 2\(f\), i.e. 120 Hz, which is transmitted from the input voltage source to the load as associated with the dc-link voltage. Besides, this issue affects the accuracy of the small-signal model as demonstrated in [20]. In this work, the low-frequency ripple of the dc-link voltage is chosen as \(\Delta V_{dc}\). Thus, the gating signal \(V_{Sb}\) is generated by the flip-flop, which is synchronized by a clock signal that defines the switching frequency for the active switch [22].

The specifications given in Table 1 will be adopted in this work for designing the power stage of the ac–dc boost converter. From the analysis of Equation (2), it is reasonable to state that the perturbed variable in \(Z_r(i)\) in Equation (27) is effectively the inductor current, although varying the input voltage has direct impact on such parameter. From the obtained waveforms, it is possible to use only long-life film capacitors with negligible ESR in the converter, whereas the transfer function in Equation (27) can be applied [26]. The filter inductance was calculated from Equation (1) using the design constraints given in Table 1, resulting in \(L_b = 2.7\, \text{mH}\) to ensure the converter operation in CCM.

### TABLE 1 Design parameters of the PFC boost converter

| Parameter (symbol) | Value and unit |
|--------------------|----------------|
| Rms line voltage \(V_{rms}\) and line frequency \(f_l\) | 220 V, 60 Hz |
| Average dc-link voltage \(V_{dc}\) | 400 V |
| Rated power \(P_r\) | 500 W |
| Switching frequency \(f_s\) | 60 kHz |
| Current ripple of the boost inductor \(\Delta I_{lb}\) | \(20\% \times I_{lb} \approx 0.64\, \text{A}\) |
| Ratio between the dc-link and input voltages \(\beta\) | 1.28 |
| Low-frequency ripple of the dc-link voltage \(\Delta V_{dc}\) | \(5\% \times V_{dc} \approx 20\, \text{V}\) |

### TABLE 2 Design parameters for PFC stage modelling

| Parameter (symbol) | Value and unit |
|--------------------|----------------|
| Peak line voltage \(V_{p}\) \((@ f_l = 60\, \text{Hz})\) | 311 V |
| Average input voltage \(V_{avg}\) | 198 V |
| Output power \(P_o\) | 500 W |
| Peak inductor current \(I_{lb}\) | 3.2 A |
| Average dc-link voltage \(V_{dc}\) | 400 V |
| Dc-link capacitance \(C_{dc}\) | 160 \(\mu\)F |
| Equivalent load resistance \(R_{load}\) | 320 \(\Omega\) |

To assess the performance of the proposed model with respect to certain disturbances, the averaged parameters in Table 2 were considered as the operating point of the PFC boost converter. A preliminary analysis must consider the operation in open-loop condition with respect to the voltage compensator. Therefore, the input disturbances will directly impact on the amplitude of the output voltage. This means that the converter dynamic response and its respective average model can be properly compared and analysed by simulation when such disturbances are applied.

The resulting waveforms are presented in Figures 6, 7, where small-signal variations are applied to the input voltage and to the reference control signal, respectively. The peak voltage in Figure 6 first increases from 311 to 322 V and returns 311 V, i.e. the nominal value. Then, it decreases to 300 V and finally returns to its nominal condition. Besides, the dc reference control signal in Figure 7 increases from 7 to 7.5 V, returns to 7 V, decreases to 6.5 V, and then returns to 7 V. It is important to emphasize that the perturbed variable in \(Z_r(i)\) is effectively the inductor current, although varying the input voltage has direct impact on such parameter. From the obtained waveforms, it is reasonable to state that the derived model is capable of predicting the behaviour of the PFC converter accurately.

At this point, it is very important to effectively demonstrate that conventional modelling techniques developed for dc–dc converters are not capable of providing good accuracy when applied to PFC converters in CCM, which often use high capacitances [13, 14]. As previously stated, such traditional methods...
consider that the switching frequency is much higher than the line frequency and, therefore, the input voltage remains nearly constant over one switching period. Then, the PFC rectifier can be analysed analogously to a dc–dc converter. The only difference is that the output filter capacitance is rated between hundreds of microfarads or even tens of millifarads depending on the operating point.

This aspect should be taken into account in the modelling of ac–dc rectifiers owing to the need of incorporating the low-frequency dynamics associated with the attenuation of the rectified input voltage. In this context, Figures 8 and 9 present simulation results for the analysis of transfer function $\frac{v_{dc}(s)}{i_{Lb}(s)}$ obtained with the well-known average state-space modelling described in [13], while this particular operating condition is represented by Equation (30). According to Equations (5) and (6), the minimum instantaneous value of the duty cycle can be found as $D_{\text{min}} = 0.222$, which is found at the line voltage peak, i.e. $V_g(\pi) = V_g$. The complementary duty cycle will be then given by $D_s = 1 - D_{\text{min}} = 0.778$. The same operating point described in Table 2 is also adopted in this case, considering that the behaviour of the converter and the conventional model is also investigated.

$$\frac{v_{dc}(s)}{i_{Lb}(s)} = \frac{R_{o(eq)}D_s}{1 + sR_{o(eq)}C_{dc}} = \frac{248.96}{1 + s(51.2 \times 10^{-3})}$$  \hspace{1cm} (30)

When comparing the transfer functions represented by Equations (29) and (30), it is possible to notice the difference in their respective denominator coefficients. Thus, the pole angular frequency in Equation (29) will be reduced to half of the value given by Equation (30), while the gain in Equation (30) will also be modified. This means that the dynamic behaviour of the analysed models will not be the same.

From Figures 8 and 9, it is clearly observed that the average model derived from the classical technique does not lead to accurate results when the input voltage and reference signal are perturbed. The transient and steady-state behaviour of the model do not represent the converter adequately, which may imply the inaccurate design of the voltage control loop. It is worth mentioning that the PWM switch model in CCM also employs the same modelling principle, i.e. assuming that the input voltage is constant over the switching period [14], thus leading to the very same results and conclusions.

Aiming at a frequency response analysis of the proposed model, the averaged circuit in Figure 10 was simulated in PSIM®. The proposed model was then compared with the frequency-domain Bode plots obtained from the converter simulation with averaged input parameters. Therefore, for a sinusoidal peak voltage of 311 V, the average input rectified voltage is given by $V_{g_{\text{avg}}} = (2/\pi)V_g \approx 198$ V and the duty cycle $D_{\text{avg}}$ for the averaged case is obtained from Equation (31) for the operating point in Table 2. It is important to notice in Figure 10 that the small-signal ac disturbance is applied to the input variable of $Z_s(s)$, i.e. the boost inductor current $i_{Lb}$, while the output parameter is taken by means of the dc-link voltage $v_{dc}$.

$$D_{\text{avg}} = 1 - \frac{V_{g_{\text{avg}}}}{V_{dc}} = 0.505 \hspace{1cm} (31)$$

The Bode plots of the converter and its respective average model are presented in Figure 11 for a frequency range from 1 Hz to 10 kHz. Based on the frequency response, it is observed that the resulting curves are nearly overlapped, thus validating the model represented by Equation (27). It is worth mentioning that the average model is valid up around the rectified line frequency ($2f_s/2 = 60$ Hz). Therefore, the frequency
response is quite satisfactory, also ensuring effectiveness to the proposed modelling technique for the accurate design of controllers required by the voltage loop in PFC converters.

In order to derive a complete dynamic model of the converter, it is also necessary to discuss about the inner current loop associated with the OCC technique and IC IR1150 [22, 25, 27]. This loop is capable of providing PFC by integrating the error signal generated by the comparison between the sampled inductor current and the reference signal of the inner current loop. Consequently, the resulting inductor current will present sinusoidal shape, which ensures an input current with low total harmonic distortion (THD$_i$).

Typically, the inner current loop must present very fast response, while only the high-frequency system dynamics is considered in the modelling. Therefore, there is no need to employ an advanced low-frequency-related modelling technique in this case as it was previously described for the external voltage loop. Then, well-known high-frequency-based modelling methods such as the average state-space or the PWM switch model can be satisfactorily applied [14, 17]. In this case, the transfer function associated with the current control loop represented by $\mathcal{G}_i(s)$ corresponds to a resettable integrator in the OCC, which is internally set inside IC IR1150 and cannot be externally modified by the user. Only a sample of the rectified inductor current is required for the accurate operation of the current loop, which can be obtained from a simple shunt resistor or a Hall effect sensor.

Although $v_{dc}(s)/d(s)$ represents the control-to-output transfer function, it is important to emphasize that only the portion corresponding to $Z_v(s)$ is used to design the control system. Therefore, the design procedure is restricted to the external voltage loop, while the tuning process of its respective controller $C_v(s)$ is addressed in the forthcoming section.

5 | DESIGN METHODOLOGY OF THE CONTROL SYSTEM

The previously derived average model can be used to design the compensator associated with the external voltage loop of the PFC converter. It will also ensure that the employed control technique will not distort the input sinusoidal current when input voltage disturbances come to occur.

The controller must be properly tuned aiming at some predefined assumptions, which have been adopted as guidelines for the implementation of the voltage loop controller. In order to avoid distorting the inductor current, the voltage loop must be designed with slower response than the current loop, which can be accomplished by ensuring a high attenuation of the low-frequency component of the error signal at $2\cdot f_L$, i.e. the low-frequency ripple. First, the open-loop crossover frequency of the compensated loop must be less than one third of the ac grid frequency, 10 Hz being a fair choice. Fast dynamic response without high overshoot in the dc-link voltage can be obtained if
the open-loop phase margin is chosen to be equal to or greater than 60°. On the other hand, the open-loop gain margin is chosen as higher as possible to provide good stability when rejecting low-frequency input disturbances.

Within this context, an integral control action ensures that the steady-state error regarding the dc-link voltage will be as low as possible, while the proportional action provides fast dynamic response [28]. Capacitive filtering is also employed in this case, which mitigates high-frequency noise and minimizes de-link voltage overshoot during transients. Bearing in mind the aforementioned directives, a modified proportional-integral (PI) type-2 controller has been employed in this work, whose transfer function is shown in Equation (33). This expression shows the proportional gain \( k_p \) with the zero- and pole-related time constants \( T_c \) and \( T_p \), respectively, as well as the pole at the complex plane origin.

In order to achieve the desired performance, the proper frequency allocation of the zero and the poles of the compensator must be performed. In this work, SISO Design Tool of Matlab® was employed to accomplish this task. As previously mentioned, the crossover frequency of the compensated voltage loops was chosen as 10 Hz with a phase margin close to 60°. One of the poles must be placed at the origin of the complex plane to ensure nearly null steady-state error, i.e. 0 Hz. The other pole can be placed at one tenth of the switching frequency, i.e. 6 kHz to mitigate the high-frequency noise. The zero is allocated at one tenth of the crossover frequency, i.e. 1 Hz aiming at improving the transient response. From the aforementioned methodology, the values of the controller parameters have found to be \( k_p = 70.6 \, [1/V] \), \( T_c = 12.8 \, ms \), and \( T_p = 12.4 \, ms \). The designed voltage loop compensator \( C_v(s) \) is then represented by Equation (33).

The components used in implementation of the PI controller, i.e. the resistor and capacitors can be determined by comparing Equation (34) with (33), resulting in \( C_p = 120 \, nF \), \( C_z = 470 \, nF \), and \( R_{gm} = 100 \, k\Omega \). These values ensure high attenuation of the component at 2\( f_s \), i.e. \(-55.2 \, dB\) as represented by the Bode plots in Figure 12. Besides, Figure 13 presents the open-loop root locus with the respective compensator, where the poles and the zero of the system are highlighted. Still in Figure 13, the related Bode plots show a phase margin close to 60° and infinite gain margin, which result in a stable loop. Therefore, the control parameters ensure proper system stability without impairing the input current performance.

\[
C_v(s) = k_p \cdot \frac{T_c s + 1}{T_c s + 1} \cdot \frac{1}{s(T_p s + 1)}
\]

\[
C_v(s) = 70.6 \cdot \frac{0.0128 s + 1}{s} \cdot \frac{1}{0.0124 s + 1} = \frac{0.904 s + 70.6}{s(0.0124 s + 1)}
\]

\[
C_v(s) = \frac{\gamma_m}{C_p + C_z} \cdot \frac{R_{gm} C_z s + 1}{s} \cdot \frac{1}{R_{gm} C_z C_p + C_p s + 1}
\]

where \( \gamma_m = 0.042 \, mA/V \) is the internal transconductance gain of IC IR1150 [27].

## 6 EXPERIMENTAL RESULTS

In order to analyse the performance of the PFC converter associated with the closed-loop control system, the operating point previously presented in Table 1 was adopted. The components employed are summarized in Table 3 and the prototype is shown in Figure 14, where \( D_{ch} \) is a diode required to previously charge the de-link capacitor and avoid high-current start-up transients [27]. Besides, \( R_{DS} \) and \( C_{Dh} \) are designed according to the guidelines given in [27] to mitigate the current spikes in the boost diode \( D_b \) during turn-on. The detailed description of the remaining components used in the printed-circuit board (PCB) associated with the control system will not be presented here for simplicity, although it can be found in [25] and [27].

A programmable ac voltage source by California Instruments, a power meter WT-230 by Yokogawa, and a digital oscilloscope DPO3014 by Tektronix were employed in the laboratory tests to obtain the experimental results.

Figure 15 shows the input current, the input voltage, and the inductor current waveforms, thus denoting the operation in CCM. Besides, a detailed view of the high-frequency ripple of the inductor current at the line voltage peak is presented, which is in accordance with the design specifications. The input current is nearly sinusoidal and remains in phase with the input voltage, resulting in an input power factor of 0.992 and THD\( _i = 5.56\% \). It is observed that the employed modelling technique associated with proper design constraints for the implementation of OCC is capable of ensuring an input current without significant distortion, while also providing high input power factor.

The harmonic content of the input current has been also obtained using the fast Fourier transform (FFT). Figure 16 shows a comparison of the frequency components with the limits imposed by standard IEC 61000-3-2 regarding class-C equipment. It can be stated that the limits are strictly respected for the first thirty-nine harmonic components as expected [4].

Figure 17 shows the de-link voltage. The low-frequency voltage ripple is about 21 V, which corresponds to the attenuation provided by the film capacitor employed in the de link. Besides,
FIGURE 13  Root locus and Bode plots of the compensated open-loop transfer function

TABLE 3  Components employed in the prototype

| Component                  | Value and description |
|----------------------------|-----------------------|
| Boost inductor ($L_b$)     | 2.7 mH, Ferrite Core NEE 55-28-21, 3×AWG 24, 90 turns |
| Low-frequency filtering de-link capacitor ($C_{dc}$) | 160 µF (2×80 µF/450 V) |
| High-frequency filtering capacitors | 100 nF/500 V (input capacitor $C_i$), 470 nF/1 kV (output capacitor $C_{hf}$) |
| Semiconductors elements    | KBU8K (diode bridge), MOSFET IRFP460 ($S_b$), ultrafast diode MUR 860 ($D_b$), ultrafast diode MUR 8100 ($D_{ch}$) |
| RC snubber                 | 100 Ω ($R_{Db}$), 100 pF ($C_{Db}$) |
| Shunt resistor             | 0.2 Ω ($R_{sh}$) |
| PI compensator             | 100 kΩ ($R_{gm}$), 120 nF ($C_p$), 470 nF ($C_z$) |

FIGURE 14  Experimental prototype of the PFC boost converter employing OCC with a detailed view of the control board

FIGURE 15  Input voltage $V_g$ (CH1—250 V/div), input current $I_g$ (CH2—5 A/div), inductor current $I_{L_b}$ (CH4—2.5 A/div), and detailed view of the high-frequency current ripple in $I_{L_b}$. Time scale: 10 ms/div
FIGURE 16  Comparison between the harmonic spectrum of the input current and the limits imposed by standard IEC 61000-3-2

FIGURE 17  DC-link voltage $V_{dc}$ and detailed view of the low-frequency voltage ripple (CH3—100 V/div). Time scale: 10 ms/div

the average dc output current is about 1.25 A as desired. The efficiency has been measured as 96.8% using power meter WT-230 by Yokogawa.

Figure 18 shows the dynamic results for the PFC converter connected to a resistive load, where the input voltage was modified under step variations in order to evaluate the response of the dc-link voltage. It is worth mentioning that this quantity is supposed to be properly regulated by $C_v(s)$, which was tuned according to the guidelines provided in the previous section. Besides, it must be capable of ensuring that the dc-link voltage can be controlled while not distorting the input current. It can be stated that the type-2 compensator leads to reduced steady-state error and fast transient response, where the settling time is about 33 ms. Thus, the dc-link voltage remains regulated at 400 V after both negative and positive steps of the input voltage, i.e. 14%, and 7%, corresponding to rms grid voltages of 190 and 235 V, respectively. The input current also remains nearly sinusoidal and in phase with the input voltage in steady state.

Aiming at an in-depth analysis regarding the transient behaviour of the closed-loop system, the comparison of some key control parameters related to the experimental converter and the simulated model is presented in Table 4. Considering a positive step applied to the input voltage, there are only slight differences between the dc-link voltage overshoot and settling time obtained experimentally and by simulation. Such results are in accordance with the accurate response of the proposed model as demonstrated in Figures 6, 7, and 11.

The converter dynamic response was also analysed for positive and negative load steps of 8%, i.e. from 500 to 545 W and from 500 to 455 W, respectively, while the results are shown in Figure 19. Once again, the waveforms clearly denote that the dc-link voltage remains regulated at 400 V and the input current presents low harmonic distortion.

All aforementioned results clearly validate the introduced modelling technique in terms of a stable control system that could only be accurately designed while incorporating the low-frequency dynamics for the proper tuning of the required compensators.
7 CONCLUSIONS

This work has presented a general small-signal modelling procedure for PFC rectifiers operating in CCM. Considering that traditional techniques such as average state space and PWM switch model are not capable of reproducing the low-frequency dynamics of such converters accurately when high-value filter capacitors are used, the introduced methodology can be regarded as a simple, concise, and straightforward solution. A front-end boost rectifier was analysed in detail, whose choice is owing to the fact that this is a quite popular topology for general-purpose applications. Besides, OCC could be successfully implemented from the transfer function derived in the mathematical analysis.

The small-signal model was properly validated in both time and frequency domains from relevant waveforms and Bode plots, respectively, thus showing that it is capable of reproducing the behaviour of the PFC rectifier adequately even when high-value filter capacitors are used. In this context, the design procedure of the control system was also employed in the development of an experimental prototype. Considering that high input power factor, nearly sinusoidal input current in phase with the supply voltage, and regulated dc-link voltage could be obtained, it is reasonable to state that the modelling technique leads to reliable results in terms of the accurate design and tuning of controllers required by the existing loops. Furthermore, the closed-loop control system performance related to the measured overshoot and settling time ensured the accuracy and applicability of the proposed low-frequency modelling technique, since only slight differences were verified when comparing the experimental prototype with the simulated model.

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