BB-ML: Basic Block Performance Prediction using Machine Learning Techniques

Hamdy Abdelkalik*, Shamminuj Akhtar†, Yehia Arafa‡, Atanu Barai§, Gopinath Chennupati‡, Nandakishore Santhi†, Nishant Panda†, Nirmal Prajapati†, Nazmul Haque Turja†, Stephan Eidenbenz†, Abdel-Hameed A. Badawy‡

*Klipsch School of ECE, New Mexico State University, Las Cruces, NM 88003, USA
†Los Alamos National Laboratory, Los Alamos, NM 87545, USA
‡Qualcomm Inc, USA
§Intel Corporation, USA
¶Amazon Inc, USA

{enghamdy, saktar, yarafa, atanu, nhturja, badawy}@nmsu.edu {nsanthis, nishpan, eidenben, prajapati}@lanl.gov

Abstract—Recent years have seen the adoption of Machine Learning (ML) techniques to predict the performance of large-scale applications, mostly at a coarse level. In contrast, we propose to use ML techniques for performance prediction at a much finer granularity, namely at the Basic Block (BB) level, which are single entry, single exit code blocks that are used for analysis by the compilers to break down a large code into manageable pieces. Utilizing ML and BB analysis together can enable scalable hardware-software co-design beyond the current state of the art. In this work, we extrapolate the basic block execution counts of GPU applications and use it for predicting the performance for large input sizes from the counts of smaller input sizes.

We trained a Poisson Neural Network (PNN) model using random input values as well as the lowest input values of the application to learn the relationship between inputs and basic block counts. Experimental results show that the model can accurately predict the basic block execution counts of 16 GPU benchmarks. We achieved an accuracy of 93.5% for extrapolating the basic block counts for large input sets when the model is trained using smaller input sets. Additionally, the model shows an accuracy of 97.7% for predicting basic block counts on random instances. In a significant case study, we applied the ML model to CUDA GPU benchmarks for performance prediction across a spectrum of applications, spanning linear algebra to machine learning benchmarks. We employed a diverse set of metrics for evaluation, including global memory requests, tensor cores’ active cycles, and the active cycles of ALU and FMA units. The results from the case study demonstrate that the model is capable of predicting the performance of large datasets with high accuracy. For example, the average error rates for global and shared memory requests are 0.85% and 1.07%, respectively. Furthermore, to address the utilization of the main functional units in Ampere architecture GPUs, we calculated the active cycles for units like tensor cores, ALU, FMA, and FP64 units. Our predictions for the active cycles show an average error of 2.3% for the ALU and 10.66% for the FMA units, while the maximum observed error across all tested applications and units reaches 18.5%.

Index Terms—Performance Modeling, Basic Block, GPGPU Application, Machine Learning

I. INTRODUCTION

Graphics Processing Units (GPUs) have rapidly advanced to become the most common accelerators for high-performance computing. Modern GPUs are equipped with thousands of processors, capable of reaching up to 9.7 TFLOPS (trillion floating-point operations per second) for mixed-precision tasks [2]. Their highly parallel structure, exceptional floating-point computation capabilities, and memory parallelism make them ideal for a range of scientific and engineering applications in High-Performance Computing (HPC) environments. The most recent TOP500 list shows that the newest generation of supercomputers predominantly features GPU-accelerated systems [7]. This widespread adoption has sparked considerable research into the performance modeling and simulation of modern GPUs.

Modeling and simulation tools play a significant role in designing and evaluating new hardware features and understanding the limiting factors on application performance. Due to modern GPU complexity, improving its hardware performance has become more complex. Using ModSim (Modeling and Simulation) tools, GPU architects get insight into the impact of any changes in hardware design on application performance, area, and power consumption. Thus, these tools enable design space exploration. On the other hand, ModSim tools are also used extensively in hardware-software co-design to tune application performance. They help system designers choose the proper hardware for any specific workload. Additionally, application developers can tune their applications for a wide variety of GPUs without having access to the physical hardware. Scalable ModSim tools are necessary to allow quick and accurate design space exploration.

Performance analysis centered around the software concept of a basic block, defined as a single entry, single exit section of code, has recently been proposed for CPU architectures [10], [13], [17], [27]. The number of times a basic block is executed in a specific application is a good measure of the impact on the performance of that basic block for the whole application. A higher count leads to a higher impact. Thus, knowing the number of times (count) a BB executes is necessary for BB-level performance analysis.

By characterizing the performance signature of the basic
blocks and extracting the counts and other relevant information at a basic block level granularity, we can predict the performance of an application in finer granularity more efficiently and scalably. However, extracting the BB execution counts for large input sizes of an application can be very costly and become a scalability bottleneck, as it requires executing and/or profiling the application. Thus, addressing this inefficiency is necessary to achieve scalable performance prediction for ModSim tools, enabling hardware-software co-design. Therefore, BB count extrapolation enables scalable ModSim tools that use BB analysis in their performance prediction flow [13], [15], [17]. Furthermore, BB analysis is needed in compiler analysis passes [1], and this work could be leveraged for such purposes.

In this paper, we introduce BB-ML, which uses Deep Neural Networks (DNN) to predict basic block execution counts of GPU applications. First, we build a Poisson Neural Network (PNN). PNN is a probabilistic model that treats basic block counts as a Poisson random variable and leverages Deep Neural Networks to learn to predict basic block counts for GPU applications. It also can extrapolate basic block counts for larger application input configurations (sizes). To train the model, we use labeled data where the input parameters of applications are used as input features for the neural networks, while the BB counts are used as the output of the networks. Results show that our model can accurately extrapolate basic block counts for large input configurations and random input values of the applications.

The contributions of the paper are:
- To our knowledge, this is the first work to predict BB counts for GPU applications.
- We introduce Poisson Neural Network (PNN), a probabilistic DNN model that treats BB counts as Poisson distributions to capture the relationship between input sets of a program and BB counts.
- We demonstrate that the trained model showed competitive accuracy on the set of benchmarks used. The model achieved 93.5% accuracy for extrapolating basic block counts from higher input configurations and 97.7% accuracy for predicting block counts on random instances.
- We applied our model on a study case for validation.

The rest of the paper is organized as follows: Section II summarizes the relevant related work and sets this work apart from the relevant related work. Section III covers the necessary background and shows a control flow graph with basic blocks of a small sample program. Section IV overviews the basic block trace extraction, the two neural network architectures, and their training. Section V goes over the experimental results of our NN models. It compares the two models and shows detailed results. Finally, Section VI concludes the paper.

II. RELATED WORKS

BB-level performance prediction attracted much research in both CPU [14], [17] and GPU [15] domains. Tools such as llvm-mca [1] from LLVM or IACA [8] from Intel perform BB-level program analysis. This section shows some of the work centered around BBs, predicting their count, and throughput, or leveraging the BB information to predict the whole program execution time.

In the CPU domain, Mendis et al. [22] proposed Ithemal, a tool for predicting the throughput of basic blocks in applications. The authors used a regression-based model alongside with a Long Short-Term Memory (LSTM) recurrent neural network to predict how many times the BB gets executed. Their model takes the BB assembly instructions as input and provides the basic block throughput as output. In the same spirit, Abel et al. [10] proposed a parametric pipeline model and basic block throughput predictor for Intel processors. Their model also addresses some limitations in the Ithemal model. Other works, such as PPT-AMMP [17] proposed by Chennupati et al., demonstrated a regression-based technique to predict the BB counts of CPU applications for large input sets. They used the counts to predict the run-time of serial applications on a single-core CPU.

In the GPU domain, Betts et al. [15] developed a model that uses basic block (BB) execution information, such as execution traces and time, to predict an application’s worst-case execution time. They extracted BB traces using a cycle-accurate simulator, which is notably slow; such simulations can take weeks or even months for extensive input sizes [11]. Another limitation is the necessity to extract traces anew with each input change, which is not a daunting task on cycle-accurate simulators.

To our knowledge, no prior work exists that predicts the BB executions throughput for GPU architectures. Adopting this work in the future can reduce the time and space of trace extraction for performance prediction models [11], [15]. Thus, enabling scalable predictions that can train the model once per application on small input sizes and reconstruct a trace for higher input sizes.

III. BACKGROUND

A. Basic Blocks

A basic block represents a straight code sequence with no branches. In other words, a BB is a linear code sequence with a single entry and a single exit point with no branches in between. In a program Control Flow Graph (CFG), if a program execution enters a BB, all the instructions in that BB execute until a branch instruction is encountered. Generally, the compiler breaks down the program into multiple BBs during analysis.

Figure 1 shows the control flow graph of an example program. There are five BBs in this program. The BBs BBI ... BBn represent the vertices or the nodes in the CFG. A directed edge (BBi → BBj) exists if program control flows from BBi to BBj. Special nodes Enter and Exit are the source and the sink of the graph. A loop is composed of multiple basic blocks. For
example, \(BB2\), \(BB3\), and \(BB4\) represent a loop. Conditional statements like if statements represent their own basic blocks, e.g., \(BB2\) and \(BB3\).

B. GPU Execution Hierarchy

In the CUDA programming language, a group of threads is called a CUDA block. CUDA blocks are grouped into a grid. A GPU program or kernel is a function executed concurrently as a grid of thread blocks. GPU programs utilize data, thread, and task parallelisms. From the software perspective, GPUs have three execution levels: block-level, warp-level, and thread-level, to achieve such parallelisms. Additional information can be found in the CUDA programming model [5].

C. Machine Learning Techniques

Researchers from diverse domains widely employ machine learning for solving complex problems. Machine learning utilizes mathematical models and data analysis to learn information directly from data. Probabilistic models assist machine learning by examining the underlying distribution of datasets and learning the pattern from inputs and outputs. Regression is one of the machine learning techniques from supervised learning where the model learns from labeled samples. Regression methods are used to predict numerical outcomes based on insights gained from a dataset with predefined labels. The most commonly used regression techniques are linear regression, logistic regression, and polynomial regression [18].

Deep Neural Networks, inspired by human brain information processing, use hidden layers to store and find the relationship between the inputs and the outputs. A neural network consists of input, hidden, and output layers, where information is passed through the layers and updated using feedback mechanisms. The activation function, learning mechanism, and loss function are used in the neural network to optimize the training process. An artificial neural network composed of multiple hidden layers is a Deep Neural Network (DNN). DNNs are efficient in modeling complex non-linear real-world problems. Some commonly used DNN frameworks are TensorFlow [9], PyTorch [24], and Keras [20].

IV. METHODOLOGY

This section goes over the various steps needed for BB count prediction. We first explain the BB trace extraction. Then, we detail the architecture of the Neural Network models, and, finally, the training of the models.

BB-ML can utilize any NVIDIA GPU, given its configuration parameters. We are limited to NVIDIA GPU since we use their tools for BB count profiling. The methodology can be extended to other GPUs as long as we can collect the necessary traces. Figure 2 shows a high-level overview of BB-ML. It comprises various components that feed off of each other to predict the BB counts eventually. First, the BB Trace Extraction Tool extracts BB traces by running the application on a physical GPU. Then, the collected BB traces are fed to the two Neural Network models to get the BB Count Predictions.

A. BB Trace Extraction

The first step of the model is extracting the BB execution traces. To extract the BB trace, we extended NVBit [25] to get the trace dynamically. NVBit is a dynamic binary instrumentation tool from Nvidia Research that can implement profilers, perform error checking, and collect various traces, including those of memory, instructions, and BBs. In our work, we adapted the NVBit tool to dynamically collect the BB counts per kernel for GPU applications.

We extract an application-dependent BB trace. Thus, we can use any Nvidia GPU. We extract the different application traces using several GPUs: a Tesla A100 Ampere GPU, a Titan V Volta GPU, and a Tesla V100 Volta GPU.

Algorithm 1 shows a high-level overview of the logic of extracting the BB trace using NVBit. The first step for the
algorithm is to instantiate and initialize the necessary variables (BB ID, Kernel ID, and the arrays holding the BB count for each BB and the array of kernel IDs) as shown in lines [1-4]. We set the array sizes to 1000 for illustration purposes, but the array size varies by the number of BBs for each kernel and the number of kernels in a GPU application. NVBit assigns an automatic ID for each BB and kernel, but these values are very large and not in order. For simplicity, we use the ID_BB and ID_ker variables in lines [1,2] to assign new in-order IDs for the BBs and the kernels. In lines [5-14], we go over all the kernels and the basic blocks in the application and inject a function after each BB to collect the IDs of the BB and the kernels. In lines [15-21], we use another function to receive the IDs dynamically and calculate the BB counts. In line 19, we store the kernel ID in the same index as the BB count because we need to associate the specific kernel that each BB belongs to.

We follow the methodology suggested in the NVBit tool to profile the applications at run-time. We wrote a script that automates the BB traces automatically while changing the input at each invocation. We collect the BB counts per thread block per kernel per application and feed it to the ML model afterward.

B. Deep Neural Network Model Architecture

This section describes the Poisson Neural Network Model (PNN), a probabilistic model that treats the underlying distribution of BB execution counts as a Poisson probability distribution. The task of predicting counts is often modeled as a regression problem in various domains [21], [23], [26].

A Poisson probability distribution models the occurrence of an event within a fixed period of time. It is commonly used to model a system where the target variable is a discrete count variable. BB execution counts are always positive and discrete in nature. We analyze the distribution of BB counts and their relationship to the input parameters. Figure 3 presents a kernel density estimation (KDE) plot of counts for one BB of the ‘bicg’ dataset from Table I. The X-axis represents the BBs counts, and the Y-axis shows the probability density function for the kernel density estimation. The density plot shows the underlying distribution of BB counts, which is Poisson-like, where each count is independent. From the distribution, we find that BB counts can be modeled as a Poisson random variable with mean $\lambda$. We propose a machine learning model that can learn mapping ($f$) from input parameters ($x$) to predict BB count. Suppose $x$ is our input parameter vector, and $Y$ is the BB count. In that case, we model the BB count as a Poisson random variable with mean $\lambda$, where $\lambda$ only depends on input parameter $x$. Thus, the probability that $Y$ has count $j$ is given by:

$$P(Y = j) = \frac{e^{-\lambda(x)}\lambda(x)^j}{j!}$$  \hspace{1cm} (1)

The Poisson Neural Network (PNN) uses a Poisson loss function to minimize the loss and maximize the likelihood of the data. PyTorch’s Poisson negative log likelihood ($nn.Poisson.NLLLoss$) loss function is used to compute the loss in the training process where we choose the log_input parameter to be False [4]. The loss is a scalar value that is computed from input and target as,

$$loss(input, target) = input - target + log(input + eps)$$  \hspace{1cm} (2)

where $eps$ is a small value which is added to avoid computation of $log(0)$. We implemented the PNN model using PyTorch. The input layer neurons are fully connected to the hidden layer, and the hidden layer is also fully connected to

---

**Algorithm 1 Trace Extraction Algorithm**

1: $ID\_BB = 0$  \hspace{1cm} //Basic Block ID  
2: $ID\_ker = 0$  \hspace{1cm} //GPU Kernel ID  
3: $BB\_counts\_array[1000]$  
4: $kernel\_IDs\_array[1000]$  
5: procedure INSTRUMENTATION_FUNCTION  
6:   while kernel\_found = 1 do  
7:     while $BB\_found = 1$ do  
8:       Send( $ID\_BB$ )  
9:       Send( $ID\_ker$ )  
10:       $ID\_BB \leftarrow ID\_BB + 1$  
11:     end while  
12: $ID\_ker \leftarrow ID\_ker + 1$  
13: end while  
14: end procedure  
15: procedure RECEIVE_FUNCTION  
16:   while data\_available = 1 do  
17:     $X \leftarrow$Read( )  
18:     $BB\_counts\_array, X.ID\_BB\_array \leftarrow BB\_counts\_array, X.ID\_BB\_array$  
19:     $kernel\_IDs\_array, X.ID\_ker\_array \leftarrow kernel\_IDs\_array, X.ID\_ker\_array$  
20: end while  
21: end procedure

---
the output layer. The hidden layer’s size is ten, and the output
layer is 1, where the input layer size depends on the number of
inputs of the application. We used the\( \tanh \) activation function
to transform the weighted sum of the input into an output.
Adam optimizer is used in PNN to update weights and the
learning rate in the training stage. We tune the hyperparameters
(number of epochs, batch size, and learning rate) to optimize
the training process. Rigorous tuning shows that the network
gets minimal loss for specific values of the hyperparameters.
Therefore, we train the models for 300 epochs using a batch
size of 10 and choose the learning rate to be \( 10^{-4} \).

C. Training the Neural Network

We have three sets of training and testing data generated
from the same original collected data. We split the data into
high-low, mixed high-low, and random data. Here, we explain
how the data is split. First, for the high-low data, we assign
the lower 70% of the input range of the input samples to be
the training set and the remaining 30% of the input range,
which represents the higher range input samples to be the test
set. There are some input values with a combination of low
and high values. We first train our models without these mixed
input values and calculate accuracy. To examine the effect
of mixed input values, we also train the models with a training
dataset that includes the mixed range of input samples (mixed
high-low data). Lastly, we randomly assign 70% of the samples
to a training set and the rest 30% to the testing set to measure
the overall accuracy of our model.

Prediction and extrapolation on the PNN model from Sec-
tion IV-B generate scalar values of basic block counts. To
compare the predicted and actual basic block counts, we use a
normalized error metric, Mean Squared Error (MSE), defined
as follows,

\[
MSE = \frac{1}{n} \sum_{i=1}^{n} (Y_i - \hat{Y}_i)^2 \tag{3}
\]

where \( n \) is the number of samples, \( Y_i \) is the predicted counts,
and \( \hat{Y}_i \) is the actual basic block count.

We also compute the Pearson correlation coefficient [3],
and Spearman correlation coefficient [6] between predicted
values and actual values of basic block execution counts for
each benchmark. Pearson correlation measures the strength
of the linear relationship between predicted and measured
counts. Spearman correlation assesses whether there is a linear
relationship between variables equal to the Pearson correlation
between the rank values of those two variables.

V. RESULTS

A. Experimental Setup

We choose 16 broadly used GPU benchmarks listed in
Table I to verify our prediction models. We use 12 applications
from the Polybench benchmark suite [19] and four applications
from the Rodinia benchmark suite [16]. We train the PNN
model using these benchmarks with the different training and
testing datasets described in Section IV-C.

B. Predictions Results

First, we evaluate the performance of our trained models
using the test dataset from the random splitting of the sample
set. We calculate the MSE with respect to the ground truth
for each benchmark. Table II shows the average MSE and
correlation statistics for predicting basic block counts for un-
seen test inputs from the random dataset with an overall MSE
of less than 0.023. For all benchmarks except for Gaussian,
mvt, lud, and lu, the MSE for predicting basic block counts
is close to zero (MSE < 0.003). Other applications have less
than 0.012 MSE error for random test set prediction except for
the lu benchmark. We also find good Pearson and Spearman
correlation values for almost all the benchmark applications
(Table II).

To further investigate, we separate the low input values
and high input values from the dataset by setting a cut-off

\begin{table}[h]
\centering
\caption{Benchmark applications used from Rodinia [16] (indicated with \( \ast \)) and Polybench [19] (indicated with \( \ast \)) benchmark suites in this work. The table lists the total number of BB samples collected, input parameters, and BBs for each application.}
\begin{tabular}{|c|c|c|c|c|}
\hline
Benchmark & Description & \# of BB Samples & \# of Inputs & \# of Basic Blocks & Domain \\
\hline
\ast 2mm & 2 Matrix Multiplications & 11505 & 4 & 21 & Linear Algebra \\
\ast atax & Matrix Transpose and Vector Multiply & 25865 & 2 & 21 & Linear Algebra \\
\ast bicg & BiCGStab Linear Solver & 27281 & 2 & 21 & Linear Algebra \\
\ast covariance & Covariance Computation & 9595 & 2 & 54 & Data Mining \\
\ast correlation & Correlation Computation & 5020 & 2 & 135 & Data Mining \\
\ast doigen & Multiresolution Analysis Kernel & 6009 & 3 & 13 & Linear Algebra \\
\ast gemm & Matrix Multiplications & 81219 & 3 & 10 & Linear Algebra \\
\ast gesummv & Scalar, Matrix-Matrix Multiply & 9998 & 1 & 10 & Linear Algebra \\
\ast lu & LU Decomposition & 4347 & 1 & 31 & Linear Algebra \\
\ast gramschmit & Gram-Schmidt Decomposition & 3117 & 1 & 83 & Linear Algebra \\
\ast syrk & Symmetric Rank-k Operations & 9900 & 2 & 15 & Linear Algebra \\
\ast mvtx & Matrix-Vector Product Transpose & 8189 & 1 & 21 & Linear Algebra \\
\dagger gaussian & Gaussian Elimination & 2070 & 1 & 36 & Linear Algebra \\
\dagger lud & LU Decomposition & 2052 & 1 & 11 & Linear Algebra \\
\dagger inw & Needleman-Wunsch & 3357 & 1 & 21 & Bioinformatics \\
\dagger pathfinder & Path-Finder & 65171 & 3 & 6 & Dynamic Programming \\
\hline
\end{tabular}
\end{table}
value. We train the PNN model with samples that have only low input values for each benchmark and evaluate the model with large input instances. Table III shows the extrapolation result of basic block counts on high input values when the model is trained using low input values as well as mixed input values. Among the 16 applications, gaussian, lu, nw, and lud have greater than 0.1 MSE. Investigating these datasets shows that they have a significant number of zero basic block counts. Similar to random prediction results, we find higher correlation values which indicate a good linear relationship between extrapolation and actual basic block counts in the PNN model.

The reason for obtaining correlation values less than 0.95 in certain applications, such as lu and Gaussian, is the multiple executions of the same kernel. Depending on the input size, these application kernels are invoked multiple times to apply the algorithm to varied sections of the entire matrix in each iteration. We observed that the basic block (BB) counts for the initial executions of each recurrent kernel, consistent with Nvidia Nsight methodology, remain constant. Yet, when aggregating the BB counts across all executions, the resulting data yields a less accurate model than other applications. We opted for the aggregate of all iterations as it offers a more comprehensive perspective on the overall application performance. The PNN model, on average, shows 93.6% accuracy for extrapolation learned from lower input configuration and 97.7% accuracy for random instance prediction.

A better representation of extrapolation is shown in Figure 4 for PNN. The heatmaps show extrapolation of basic block execution counts on high input values with respect to the actual basic block counts for those inputs. Each heatmap includes all basic block predictions for one benchmark. The extrapolated BB counts are expected to be close to the actual count i.e. we expect all points along the identity line \((y = x)\). We find higher density near the identity line for most benchmarks except Gaussian, lu, lud, and nw. The heatmaps represent the closeness of our extrapolation counts with actual counts.

Figure 5 shows the change in test accuracy when we vary the training sample percentage for the PNN model. This plot represents the relationship between model accuracy and training sample size. From the plot, high test accuracy for a small fraction of training samples indicates that we have sufficient samples for each benchmark application. We find that test accuracy decreases with higher samples for some benchmarks; they actually fit better with a small sample size. Although the accuracy for those applications shows slight improvement initially with increasing sample size, it decreases later with more samples. Overall, we find that PNN model is sensitive to the sample size; the test accuracy slightly increases for most benchmarks with increasing training sample size.

### C. BB Prediction: Case Study

In our quest to elucidate the capabilities of our machine learning model, particularly in its fine-grained performance prediction at the Basic Block (BB) level, we turned our focus to CUDA benchmarks. We chose a wide range of benchmarks ranging from linear algebra applications such as 2mm, gemm, atax, and mvt to complex applications and ending with more complex machine learning benchmarks such as cutlass. This varied suite effectively underscores the adaptability of our model.

Figure 6 shows the Global memory access errors are consistently low across most benchmarks, but there is an exception in the last benchmark, which exhibits an average error of 5.88%.

---

**Table II**

AVERAGE MSE AND CORRELATION FOR BASIC BLOCK COUNTS PREDICTION ON RANDOM INPUT INSTANCES FOR THE BENCHMARKS LISTED IN TABLE I.

| Benchmark | Avg. MSE | Pearson Corr. | Spearman Corr. |
|-----------|----------|---------------|----------------|
| 2mm       | 0.019    | 0.999         | 0.999          |
| atax      | 0.036    | 0.998         | 0.999          |
| bscg      | 0.017    | 0.999         | 0.999          |
| gemm      | 0.026    | 0.999         | 0.999          |
| gaussian  | 0.139    | 0.757         | 0.797          |
| pathfinder| 0.004    | 0.995         | 0.997          |
| lu        | 0.208    | 0.648         | 0.621          |
| covariance| 0.039    | 0.998         | 0.999          |
| mvt       | 0.024    | 0.999         | 0.999          |
| syrk      | 0.187    | 0.907         | 0.922          |
| gramSchmit| 0.054    | 0.996         | 0.999          |
| nw        | 0.113    | 0.981         | 0.999          |
| correlation| 0.087  | 0.983         | 0.984          |
| dotigen   | 0.001    | 0.999         | 1.000          |

**Table III**

AVERAGE MSE AND CORRELATION FOR BASIC BLOCK COUNTS EXTRAPOLATION ON HIGH INPUT INSTANCES FOR THE BENCHMARKS LISTED IN TABLE I.

| Benchmark | Avg. MSE | Pearson Corr. | Spearman Corr. |
|-----------|----------|---------------|----------------|
| 2mm       | 0.015    | 0.999         | 0.999          |
| atax      | 0.003    | 0.999         | 0.999          |
| bscg      | 0.008    | 0.999         | 0.999          |
| gemm      | 0.002    | 0.999         | 0.999          |
| gaussian  | 0.080    | 0.939         | 0.928          |
| pathfinder| 0.001    | 0.999         | 0.998          |
| lu        | 0.177    | 0.850         | 0.929          |
| covariance| 0.001    | 0.999         | 0.999          |
| mvt       | 0.002    | 0.999         | 0.999          |
| syrk      | 0.048    | 0.958         | 0.973          |
| gramSchmit| 0.002    | 0.999         | 1.000          |
| nw        | 0.012    | 0.999         | 0.999          |
| correlation| 0.002  | 0.999         | 0.997          |
| dotigen   | 0.001    | 0.999         | 1.000          |
For active cycles of the different units measured, we found that the average error is 2.3% for the FMA and 10.66% for the ALU, while the maximum average error which comes from the ATAX application is 18.5%.

VI. DISCUSSION & CONCLUSION

This work presents a Basic Block count prediction tool, BB-ML. BB-ML uses probabilistic and regression networks to predict GPU BB execution counts.

Predicting the counts of BBs executions can be valuable for various purposes, such as performance analysis, code optimization, and enhancing program understanding. With an accurate prediction of BBs execution count, we do not need to perform profiling to analyze the runtime behavior of a program or the active cycles for the included computational units. The predicted BBs could provide a static overview of potential performance bottlenecks without requiring runtime execution. Additionally, we can collect memory traces to perform a comprehensive performance memory analysis in combination with the predicted basic blocks. This synthesis becomes particularly powerful when employing performance analysis tools such as PPT-GPU [12] for a holistic evaluation of GPU applications.

In our research, we presented a probabilistic Poisson Deep Neural Network that has showcased remarkable proficiency in handling a broad range of input values with good BB prediction accuracy. Simultaneously, our performance prediction model has effectively demonstrated its capability in gauging the benchmarks’ performance. The PNN model stand
as testament to our commitment to pushing the boundaries in GPU application analysis and optimization.

REFERENCES

[1] “Llvm machine code analyzer,” https://llvm.org/docs/CommandGuide/llvm-mca.html.
[2] “Nvidia ampere architecture in-depth — nvidia developer blog,” https://developer.nvidia.com/blog/nvidia-ampere-architecture-in-depth/.
[3] “Pearson correlation coefficient,” https://en.wikipedia.org/wiki/Pearson_correlation_coefficient.
[4] “Poissonnllloss — pytorch 1.10 documentation,” https://pytorch.org/docs/stable/generated/torch.nn.PoissonNLLLoss.html.
[5] “Programming guide :: Cuda toolkit documentation,” https://docs.nvidia.com/cuda/cuda-c-programming-guide/#thread-hierarchy.
[6] “Spearman’s rank correlation coefficient,” https://en.wikipedia.org/wiki/Spearman%27s_r.
[7] “Top500,” https://www.top500.org/.
[8] “Intel architecture code analyzer,” https://www.intel.com/content/www/us/en/developer/articles/tool/architecture-code-analyzer.html, 2019.

Fig. 5. Training dataset sample percentage plot against test data accuracy of all benchmarks for PNN network

Fig. 6. Percentage error for all benchmarks and metrics...