A Probabilistic Shaping Approach for Optical Region-of-Interest Signaling

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Abstract—We propose a probabilistic shaping approach for region-of-interest signaling, where a low-rate signal controls the desired probabilistic ranges of a high-rate data stream using a flexible distribution controller. In addition, we introduce run-length-aware values for frozen bit indices in systematic polar code to minimize the run-length without using run-length-limited code. Our compact system can support soft-decision forward-error-correction decoding with excellent spectral efficiency compared with related work based on hybrid modulation schemes.

Index Terms—Region-of-interest signaling, probabilistic shaping, forward error correction, visible light communication.

I. INTRODUCTION

REGION-of-interest (RoI) signaling has been introduced by IEEE 802.15.7m group (TG7m) for vehicular optical camera communication (OCC) systems [1]. In this technique, the low-rate and high-rate data streams are transmitted simultaneously. The low-rate stream is used for RoI identification, whereas the high-rate stream is used for high-speed data communication on the selected RoI. Low-rate and high-rate streams are modulated by hybrid modulation schemes such as twinkle variable pulse position modulation (VPPM), or hybrid spatial phase-shift keying (HS-PSK). In detail, the low-rate stream is modulated by undersampled frequency-shift on-off keying (UFPSOK), undersampled phase-shift on-off keying (UPPSOK), or spatial-2 phase-shift keying (S2-PSK), whereas the high-rate stream is modulated by twinkle VPPM or dimming spatial-8 phase-shift keying (DS8-PSK) [2]. Both streams can be decoded by a dual-camera receiver, where the low-speed camera decodes the low-rate stream, and a high-speed camera decodes the high-rate stream. Hence, the computational load of the single-camera receiver is mitigated.

Dimming support is one of the critical considerations in visible light communication (VLC) and OCC specifications [1]. Dimming can be controlled by adjusting the ON (1’s) or OFF (0’s) ratio, which varies from 0% to 100%. In normal cases, dimming control comprises puncturing and compensation symbol (CS) insertion where many redundant bits are added to the frame, which degrades the achievable rate [3]. In addition, the dimming method in twinkle VPPM and HS-PSK changes the position and duty cycle of groups of high-rate pulses over time. Hence, it is challenging to demodulate twinkle VPPM and DS8-PSK signals on the receiver side because each pulse must be sampled, synchronized, and decoded at rigorous timing [4]. In conventional VLC systems, run-length-limited (RLL) codes keep DC balance with equal 1’s and 0’s in every symbol to avoid long runs of 1’s and 0’s, which causes flicker and clock and data recovery (CDR) issues. In fact, there is a trade-off between ease of implementation and rate loss in RLL codes such as Manchester, 4B6B, 8B10B [5]. Besides, most RLL decoders produce hard outputs for hard-decision (HD) forward error correction (FEC) decoder in joint FEC-RLL based systems, which show poor error-correction performance. A soft-input soft-output (SISO) RLL decoder has been introduced by Kim et al. [6], which produces soft outputs for soft-decision (SD) FEC decoding algorithms to improve the overall system reliability. However, the decoding algorithm of the SISO RLL code is bulky and hard to adopt in VLC receivers.

In this letter, we propose a probabilistic shaping approach for RoI signaling applications based on a flexible distribution controller (FDC) and systematic polar encoder/decoder (SPE/SPD) with run-length-aware (RLA) frozen bit values. The proposed system can simultaneously transmit high-rate and low-rate data with low rate-loss overhead. Besides supporting SD FEC decoders, our system guarantees the flicker mitigation without using RLL code.

II. SYSTEM MODEL

A. Proposed system

Fig. 1 shows the block diagram of the proposed system. The dual inputs of the system are a high-rate binary sequence \( \mu = (\mu_1, \mu_2, ..., \mu_k) \) and a low-rate signal \( v \) for \( v = 0, 1 \). We denote the ratios of 1’s in a \( n \)-bit FDC codeword \( u \) and a \( l \)-bit FEC codeword \( y \) as \( \phi(\%) \) and \( \omega(\%) \), respectively. In our transmitter, the FDC encodes a binary vector \( \mu \) with Bernoulli...
distribution into a codeword \( u = (u_1, u_2, ..., u_n) \) with a desired distribution. Indeed, \( \omega \) is different from \( \phi \) when the message \( u \) is encoded by a FEC encoder. We apply an SPE to preserve probabilistic shapes of \( \omega \) for the two dimming ranges. In addition, RLA frozen bit values are applied to the SPE to limit the run-length of \( y_i \) instead of using RLL code as in conventional VLC systems. For a dual-camera receiver, a low-speed camera (frame rate \(< 100 \text{ frames per second (fps)}\) with long exposure time detects the dimming ranges of light-emitting diode (LED) and decodes the low-rate bit sequence, which is used for ROI identification. A high-speed global shutter camera (frame rate \(> 10000 \text{ fps} \)) decodes the high-rate data stream on the selected ROI connection. An SD successive SPE to limit the run-length of ranges. In addition, RLA frozen bit values are applied to the low-speed camera (frame rate \( \approx 0.1 \text{ as a maximum threshold of } \phi \) for the two dimming.

Finally, the inverse FDC decodes the message \( u' \) for high-rate binary sequence \( \mu' \). OOK modulation and demodulation are selected because of their simplicity and popularity.

\[ B. \text{Flexible distribution controller (FDC)} \]

The distribution controller (DC) modifies the probability of 1's in a sequence of bits to a desired distribution using arithmetic decompresion algorithm. Let \( S' = \{u_1, u_2, ..., u_{M-1}, u_M\} \) where \( M = \binom{b}{n} \) denote the set of binary \( n \)-tuples with weight \( m \). A source model which emits \( M \) sequences in \( S' \) with probability equal to \( P(u_i) = 1/M \) for \( i = 1, 2, ..., M-1, M \). Other sequences of length \( n \) which are not in \( S' \) have zero probability. Let \( S = \{\mu_1, \mu_2, ..., \mu_K\} \) where \( K \leq M \) denote the set of \( k \)-bit information words. A one-to-one correspondence is established between \( K \) information words in \( S \) and a subset of \( K \) sequences in \( S' \) based on the source statistics introduced in \( \text{[7]} \). The code-rate loss \( \Delta_{DC} \), which indicates the average number of redundant bits carried by each DC-encoded bit, is given as

\[
\Delta_{DC} = 1 - \left[ \log_2 \left( \frac{n}{m} \right) \right] = 1 - \frac{\log_2 \binom{n}{m}}{n} \tag{1}
\]

where \( \lfloor \cdot \rfloor \) denotes the floor function, \( \lfloor \log_2 \frac{n}{m} \rfloor \) outputs the largest \( k \) satisfying the inequality \( K \leq M \) where \( K = 2^k \).

Fig. 2 shows the rate-loss analysis for various DC code lengths. For code length \( n = 100 \), it can be seen that \( \Delta_{DC} > 0.1 \) when \( \phi < 36\% \) and \( \phi > 64\% \). Hence, we select 0.1 as a maximum threshold of \( \Delta_{DC} \) to design probabilistic ranges of DC outputs. We denote the maximum \( \phi \) of the logic-0 probabilistic range as \( \Upsilon_0 \) (0\%, \( \Upsilon_0 \)) and the minimum \( \phi \) of the logic-1 probabilistic range as \( \Upsilon_1 \) (1\%, \( \Upsilon_1 \)), where \( \Delta_{DC} = 0.1 \) when \( \phi = \Upsilon_0, \Upsilon_1 \). For \( n = 100 \), \( \Upsilon_0 = 36\% \) and \( \Upsilon_1 = 64\% \). The reason for \( \Upsilon_0 \notin (36\%, 50\%) \) and \( \Upsilon_1 \notin (50\%, 64\%) \) is that the low fps camera on the receiver cannot discriminate the LED ON or OFF states when \( \phi \) is close to 50\%. In addition, it can be seen that \( \Upsilon_0 < 36\% \) and \( \Upsilon_1 > 64\% \) when \( n > 100 \). However, we select \( n = 100 \) and use FEC code length \( l = 128 \), which is compatible with short frame lengths in most VLC specifications.

We propose the FDC, which produces codewords with a flexible distribution of \( \phi \), which is denoted as \( \phi_{flex} \). The \( \phi_{flex} \) can be any value in the logic-0 probabilistic range (0\%, \( \Upsilon_0 \)) or logic-1 probabilistic range (1\%, \( \Upsilon_1 \)). A low-rate signal \( v \) controls which probabilistic range the \( \phi_{flex} \) stays in. For instance, if \( v = 0 \), the FDC will produce a codeword \( u \), which has \( \phi_{flex} \) in the range (0\%, \( \Upsilon_0 \)); if \( v = 1 \), it will produce one with \( \phi_{flex} \) in the range (1\%, \( \Upsilon_1 \)). For \( 1 < m < 5 \), let \( C_m \) denote how many times larger the codebook of \( n \)-tuples of weight \( m \) is than the codebook of \( n \)-tuples of weight \( m - 1 \), which is given as

\[
C_m = \frac{n}{m} / \left( \frac{n}{m-1} \right) = \left( \frac{n-m+1}{m} \right) \tag{2}
\]

The number of codewords in the codebook of the FDC when \( \phi_{flex} \in (0\%, \Upsilon_0) \) and \( \phi_{flex} \in (1\%, \Upsilon_1) \) are given as follow

\[
Z_{0, \Upsilon_0} = \binom{n}{1} + \binom{n}{2} + \cdots + \binom{n}{\Upsilon_0 n - 1} + \binom{n}{\Upsilon_0 n} \tag{3}
\]

\[
Z_{1, \Upsilon_1} = \binom{n}{\Upsilon_1 n} + \binom{n}{\Upsilon_1 n + 1} + \cdots + \binom{n}{n - 2} + \binom{n}{n - 1} \tag{4}
\]

Assume that \( \Upsilon_0 = 1 - \Upsilon_1 \), we have

\[
\binom{n}{\Upsilon_1 n} = \binom{n}{1} \left( 1 - \Upsilon_0 n \right) = \binom{n}{1} \left( n - \Upsilon_0 n \right) = \binom{n}{\Upsilon_0 n} \tag{5}
\]

\[
\binom{n}{\Upsilon_1 n + 1} = \binom{n}{\Upsilon_0 n - 1} + \binom{n}{\Upsilon_0 n} \tag{6}
\]

From (2), (5), (6) can now be written as

\[
Z_{0, \Upsilon_0} = Z_{1, \Upsilon_1} = \binom{n}{1} + C_2 \left( \binom{n}{1} \right) + \cdots + C_{\Upsilon_0 n - 1} \left( \binom{n}{1} \right) + C_{\Upsilon_0 n} \left( \binom{n}{1} \right) \tag{7}
\]

To calculate the code-rate loss of the FDC, which is denoted as \( \Delta_{FDC} \), from \( \Delta_{DC} \), we replace \( \binom{n}{m} \) in (1) with (7), we have

\[
\Delta_{FDC}(0, \Upsilon_0) = \Delta_{FDC}(1, \Upsilon_1) = 1 - \left[ \log_2 \left( \frac{Z_{0, \Upsilon_0}}{n} \right) \right] \tag{8}
\]

\[
\Delta_{FDC}(0, \Upsilon_0) = \Delta_{FDC}(1, \Upsilon_1) = 1 - \left[ \log_2 \left( 1 + C_2 + \cdots + C_{\Upsilon_0 n - 1} + C_{\Upsilon_0 n} \right) \right] \tag{9}
\]

From (8), it can be seen that \( \Delta_{FDC}(0, \Upsilon_0) \) and \( \Delta_{FDC}(1, \Upsilon_1) \) are symmetric with respect to \( \phi = 50\% \) when \( \Upsilon_0 = 1 - \Upsilon_1 \).
can be seen from the figure, the two probabilistic ranges, of low-rate signal FDC can produce two probabilistic shapes under the control size of the FDC is much larger than that of the DC. In short, the R

\[ \Phi \]

\[ \Omega \]

\[ \Delta \]

\[ \gamma \]

\[ \nu \]

\[ \phi \]

\[ \omega \]

C. RLA frozen bit values for SPC

To create two dimming ranges in an FEC-based system, a systematic FEC encoder should be applied to preserve the two probabilistic shapes of \( \phi_{\text{flex}} \). Furthermore, the run-length of FEC codewords should be limited to avoid flickering at the system’s optical clock. We solve these issues by employing the SPE with RLA frozen bit values. An SPC is specified by \( (l, n, F) \), where \( l \) is the code length, \( n \) is the number of information bits encoded per codeword, and \( F \) is a set of \( l-n \) indices which indicate locations of frozen bits, where \( F \subset \{1, 2, 3, \ldots, l\} \), \( |F| = l-n \). Given the SPC with code rate \( R = n/l \), at a design signal-to-noise ratio (design-SNR), a construction algorithm over an additive white Gaussian noise (AWGN) channel selects \( n \) best among \( l \) bit channels for information bit indices, and the remaining \( l-n \) channels for frozen bit indices. As the conventional setting, all \( 0 \)'s are assigned to frozen bits, which increases the \( 0 \)'s run-length of codewords. Hence, we introduce the RLA frozen bit values, which is addressed in Algorithm 1. As shown, the bit-channel metrics vector \( z \), which is created by Arikan’s Bhattacharyya bounds \[ 8 \], is sorted in ascending order. For frozen bit indices, a bit sequence where the inverse values of bit-0 and bit-1 are placed one after another is assigned. By this setting, the free run of \( 0 \)'s or \( 1 \)'s is prevented.

Algorithm 1: Method of setting RLA frozen bit values

Input: Vector of bit-channel metrics \( z \in \mathbb{R} \) generated from Bhattacharyya bounds \[ 8 \]

Output: - Vector of frozen bit locations \( f; |f| = l-n \) - Vector of RLA frozen bit values \( \phi; |\phi| = l \)

begin
\[ t = \text{sort}(z,'\text{ascending}') \]; // metrics ranking
/* Best metrics for information bits, worst metrics for frozen bits */
\[ F = \text{sort}([t ; l], '\text{ascending}'); \] /* Sorting frozen bit locations in ascending order */
for \( i = 1 : l - n \) do
\[ j = F[i]; \]
if \( \text{modulo}(i, 2) = 0 \) then
\[ y[j] = 0; \]
else if \( \text{modulo}(i, 2) = 1 \) then
\[ y[j] = 1; \]
/* A sequence of 0,1,0,1... is assigned for frozen bit indices */
end

III. Simulation results

It can be seen from Fig. 2 that with \( n = 100 \), \( \Delta_{\text{FDC}} = 0.09 \) when \( \phi_{\text{flex}} \in (0\%, \Theta_0) \) for logic 0 and \( \phi_{\text{flex}} \in [\Theta_1, 100\%) \) for logic 1. On the other hand, \( \Delta_{\text{DC}} > 0.1 \) when \( \phi < \Theta_0 \) and \( \phi > \Theta_1 \). This can be explained by the fact that the codebook size of the FDC is much larger than that of the DC. In short, the FDC can produce two probabilistic shapes under the control of low-rate signal \( \nu \) at very low rate loss.

Fig. 3 shows the post-FEC-encoder probabilistic shapes. As can be seen from the figure, the two probabilistic ranges, \( \omega \in (0\%, 50\%) \) and \( \omega \in [50\%, 100\%) \), are not overlapped when the the FDC outputs are encoded by the SPE. In contrast, they overlap and stretch on the wide range, \( \omega \in (10\%, 90\%) \), and tend to converge to the mid-range \( \omega \in (40\%, 60\%) \) when a nonsystematic polar encoder (NSPE) is applied with the FDC. To enable low-rate communication from the two dimming ranges, the probabilistic ranges must not overlap each other to be discriminated by the low-speed camera on the receiver. Therefore, the SPE is selected as the FEC encoder in our system.

We also evaluated the maximum run-length of codewords encoded by the SPE, which is denoted as \( \gamma \). As shown in Fig. 4 when the RLA values are assigned to frozen bits, \( \gamma = 63 \) is reduced by a factor of 2.03 compared to when all-zeros are assigned to them. To avoid flicker, the LED’s brightness should change within the maximum flickering time period (MFTP \( \leq 5 \text{ms} \) \[ 5 \]). Hence, with \( \gamma = 63 \), our system guarantees the flicker-free operation with optical clock rates higher than 12.6 kHz without using an RLL code.

Table I compares the proposed method with related work addressed in the image sensor communication PHY-IV modes added to TG7m \[ 2 \]. The clock rate of our system (minimum is 12.6 kHz) is almost equivalent to that of related approaches.
minimizes the run-length and preserves probabilistic shapes in the FDC. The SPC with the RLA frozen bit values of high-rate bit sequences are controlled by low-rate signal applied for RoI signaling. The desired flexible distribution then the high-speed camera decodes the high-rate data stream rate data from two dimming ranges to identify the RoI, and created by the FDC. The low-speed camera decodes the low-rate A\omega_m \in (0, 0.8) have been introduced in PHY II modes of IEEE 802.15.7 and PHY-IV modes of TG7m [1, 5], we have evaluated our system with a polar code (128,100) with \( R = 0.78 \), where the reason for short code length \( l = 128 \) is explained in section II-B. With the FDC’s rate loss \( \Delta \rho_{fro} \leq 0.09 \), our system achieves a spectral efficiency 0.91 (bits/s)/Hz, which is better than systems based on hybrid modulation schemes.

Without the support of RLL code (none-RLL), the CDR issues should be considered. Let \( \beta \) denote the number of required image frames that the high-speed camera uses to synchronize the timing and decode the bit sequence on the receiver. In our previous work [9], experimental results showed that when there is a clock difference between the transmitter and receiver, stable bit error rate (BER) performance is achieved with \( 60 \leq \beta \leq 100 \). Fig. 4 shows that the transmitted bit sequence in our system has maximum run-length \( \gamma = 63 \). It can be seen that by referring to \( \gamma \), we can set \( \gamma \leq \beta \leq 100 \) to guarantee the CDR in case of a long run of 1’s or 0’s appears in the bit sequence.

The fact that two cameras use different mechanisms in demodulating the signals, we applied two different AWGN channel models to estimate the BER and frame error rate (FER) performances of the low-rate and high-rate data streams. Table I shows the BER performance of the low-rate stream which is estimated from the overlap probability between the logic-0 and logic-1 probabilistic ranges of \( \omega \) at different SNRs, without the support of error-correction scheme. Meanwhile, the FER of the high-rate stream is calculated when data are decoded by the SD-SPD and the inverse FDC. The BER performance of the low-rate stream can be improved with \( \gamma_0 \leq 36\% \) and \( \gamma_1 > 64\% \) if the system affords a higher code-rate loss. Fig. 5 also shows that the coding gain of SD-SPD-based and HD-SPD-based systems differ by 1 dB when FER = 2E-4. In brief, due to the none-RLL feature, SD FEC decoders can be applied in our system to enhance system reliability.

\[ R \in (0.5, 0.8) \]

| Modulation/Coding | RLL | Optical clock rate | FEC | Bit rate | Spectral efficiency (BER excluded) |
|-------------------|-----|--------------------|-----|----------|-----------------------------------|
| Twinkle VPPM      | N/A | 16 kHz             | Reed-Solomon (15,11) | 4 kbps | 0.25 (bits/s)/Hz                  |
| HS-PSK            | 1/2 code rate for S2-PSK; None for DS8-PSK | 10 kHz | Temporal error-correction; Outer FEC with GF(16) | 22 kbps | 0.1375 (bits/s)/Hz\(^1\) |
| FDC (Proposed)    | None | >12.6 kHz          | Systematic polar code (128,100) | >11.47 kbps | 0.91 (bits/s)/Hz                  |

\(^1\) HS-PSK: 2 light sources, 8 LEDs for each source. Average spectral efficiency = (Bit rate/(clock rate×8×2)).

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