Radiation-hard Active Pixel Sensors for HL-LHC Detector Upgrades based on HV-CMOS Technology

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Outline

- HV2FE14 introduction
  - “Sensor”
  - Readout chip
- Lab results
- Test beam results
- Irradiation results
- Outlook
  - Alternative submissions
  - Summary
  - ATLAS Smart CMOS Pixel Collaboration
HV2FEI4 Concept

• Use bulk of commercial HV/HR-CMOS process as sensor
• Deep n-well → collection electrode
  • PMOS transistors unshielded from charges → design constraints
  • p-well used for NMOS transistors
• AMS prototypes in characterization (HV2FEI4)
HV2FEI4 Sensor

- Limited logic implementation in sensor:
  - CSA + Discriminator
  - Adjustable sub-pixel output pulse (for AC coupled signal to FE)
  - Adding of sub-pixel pulses
HV2FEI4 Sensor

- Limited logic implementation in sensor:
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  - Adding of sub-pixel pulses
- Six sub-pixels connect to two FE pixels

![Diagram of HV2FEI4 sensor and readout chip](image)
Readout Chip – FE-I4

- Use IBL readout chip: FE-I4
- Huge complexity
- Designed for passive sensor
- Pixel size 50 x 250 µm → area of 3 „sensor“ chips
- „Smart sensor“ glued to FE-I4
- Analog information (TOT) → Can be used for sub-pixel decoding
Source Scan Occupancy

Figure 7.4: The HitOR signal of the FE-I4 readout chip (top waveform), the Strobe signal used to issue an injection (middle waveform) and the preamplifier output waveform of the HV2FEI4 operated with USBpix (bottom waveform). The response of the HitOR signal to a charge injection issued in the sensor by the USBpix system (a) as well as by a particle originating from a radioactive source (b) is shown.

Figure 7.5: Occupancy maps of the HV2FEI4 glued to an FE-I4 readout chip obtained with electrons from a 90Sr source. The full FE-I4 map (a) with entries in the HV2FEI4 position and a zoom into the region of the HV2FEI4 (b).

→ Full FE-I4 pixel matrix active
→ Charges generated in sensor transmitted to FE-I4 (AC coupled)
AC Coupled Signal Transmission

Figure 7.6: The TOT information recorded by the FE-I4 (a). The TOT is not correlated to the charge collected in the sensor. The color coded mean TOT per pixel in the area covered by the HV2FEI4 (b) and the mean TOT projection along the columns (c).

- Mean ToT Map
- Mean ToT Projection

→ ToT indicator for AC coupling strength
→ Tilt of sensor or output pulse amplitude
Source Hit Timing and Cluster

Hit Timing Resolution

- Hits with significant delay recorded, time-walk sources present twice
- Sub-pixel resolution + dedicated algorithm mandatory for investigation
- Large hit clusters present

Hit Cluster Size
Sub-Pixel Resolution

→ Convoluted scans possible with new HVCMOS support in USBpix
→ Puls adding disabled, test charge injections

![Out-Pulse to ToT Calibration](image1)

- Distinct ToT peaks → sub-pixel resolution demonstrated
- Tuning algorithm and test beam necessary for spatial resolution measurement
Test Beam Results – Introduction

• Tuning algorithm for “full matrix sub-pixel reconstruction” under development
  → Single test system for “smart sensor + FE-4” mandatory
    → USBpix integration

• No sub-pixel reconstruction serious challenge for test beam measurements (temporally):
  → Alternating pixel connection pattern → challenging alignment
  → Sub-pixel resolution mandatory for in-pixel efficiency measurements

→ Careful conclusions on radiation hardness from test beam / lab results, although very promising
  (Samples “alive” after up to $10^{16} \text{ n}_{\text{eq}} \text{ cm}^{-2}$)
Test Beam Results – Timing Resolution

→ DESY test beam, 4 GeV e

→ Hits with delayed detection

![Histograms showing Hit Timing Resolution](image)

| Region               | Entries | Mean | RMS  |
|----------------------|---------|------|------|
| Col 2-11, Row 165-187: region with normal pixels | 61630   | 7.199 | 1.379 |
| Col 2-11, Row 190-210: Region with radiation hard pixels | 60459   | 2.757 | 0.4364 |

(a) C09

(b) ref. plane
Test Beam Results – Mean Efficiency

Efficiency Map

→ Reduced efficiency at edges and around dead pixels to be investigated
→ Again column dependency → Powering of HVCMOS columns
Test Beam Results - Scans

Bias Voltage Scan

Efficiency [%] vs. Bias Voltage [V]

→ Bias voltage increases efficiency

HVCMOS n-irradiated $10^{15} \text{n}_{eq}$
Test Beam Results – Column Efficiency

Drop in efficiency for high threshold
Efficiency depends on column
Global threshold setting smaller than column threshold variation

EFFICIENCY VS COLUMN

⇒ Drop in efficiency for high threshold
⇒ Efficiency depends on column
⇒ Global threshold setting smaller than column threshold variation
Irradiation Studies – Bulk Damage

→ Reasonable leakage current increase with
  - Dose, - Temperature
→ Need further results for CCE, hit efficiency, etc.

HVCMOS n-irradiated $10^{16}$ $n_{eq}$

HVCMOS n-irradiated $10^{15}$ $n_{eq}$
Irradiation Studies – Electronics

→ Decrease of Preamplifier gain with irradiation
→ Annealing periods observable
→ Parameter tuning recovers to 90% gain after ~ 900 Mrad
Smart CMOS Pixel Submissions Overview

Submissions targeting R&D with FE-I4 readout

HVC莫斯:
• AMS 180 nm – V1: First prototype
  In test
• AMS 180 nm – V2: Radiation hard electr. design
  In test

HRC莫斯:
• GF 130 nm: First prototype
  In test
• LFoundry 150 nm: First prototype
  In design
  (→ march/april 2014)
Conclusions

- Promising HVCMOS and HRCMOS prototypes submitted and in hand
- Large step towards on sensor analog signal processing + digital FE
- AC coupled signal transmission demonstrated
  → Research on gluing techniques started
- Sub-pixel resolution possible
  → Detailed characterization to come
  → Complicated tuning and reconstruction algorithms under development
- Radiation hardness of process very promising
  → Physics hits detected after several hundred Mrad (not shown here)
  → Radiation hard electronics for LHC environment feasible

- A lot achieved – more work ahead!
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