The front end and trigger unit for an analogue transient recorder ASIC

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ABSTRACT: A front end and trigger circuit was developed at GSI which is foreseen to be used in a transient recording read out ASIC. It consists of an input buffer with configurable low pass characteristics and a trigger which could be operated as leading edge discriminator as well as switched capacitor trigger which is sensitive to the first derivative of the input signal. The front end was produced on a test ASIC and characterisation results will be presented.

KEYWORDS: Analogue electronic circuits; Front-end electronics for detector readout; VLSI circuits

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1 Introduction

Currently a set of transient recorder ASICs is under development at GSI with various front ends and a common back end [1]. One of these front ends is a fully differential input buffer and trigger unit which is foreseen to connect the transient recorder to an external preamplifier developed at GSI for the electromagnetic calorimeter of PANDA experiment [2]. The front end is designed in the 180 nm technology of UMC and was realised on a dedicated test chip for characterisation. Figure 1 shows a die photograph of this test chip. The chip contains the input and trigger unit as well as the threshold DACs. In addition test structures of the analogue transient recorder are integrated which are not in the scope of this paper.

![Die photograph of the front end test chip](image)

**Figure 1.** Photograph of the front end test chip with a size of 1.5 mm × 1.5 mm.
After this introduction the requirements, the architecture and the measurement results of the input buffer are described in section 2. The trigger unit and its characterisation is presented in section 3.

2 Input buffer

The main task of the input buffer is to interface the external preamplifier with the analogue memory array of the transient recorder described in \cite{1}. Given by the aimed dynamic range of the transient recorder of $\geq 10^3$ and the maximum sampling rate of 100 MS/s the buffer has to be able to charge the memory capacitances (1 pF) as well as the load given by the trigger unit and the overall parasitics within less than 10 ns to 99.9\% of the final value.

Defined by the foreseen external preamplifier \cite{2} the buffer needs to have a high impedance fully differential input which has to cope with a $\pm 1$ V input range and a common mode voltage of 1.2 V.

2.1 Architecture

The used technology provides two voltages: 1.8 V and 3.3 V. To get more margin on the input side 3.3 V was chosen as supply voltage of the input buffer. The central component of the input buffer is a fully differential folded cascode amplifier with a source follower output stage. The output stage was optimised in simulation to fulfill the speed requirement with minimum power consumption. Finally a drain current of 2 mA and a $g_m$ of the source follower transistor of 16.95 mS was chosen. The output common mode voltage of 900 mV fits to the subsequent transient recorder.

The input buffer circuit is shown in figure 2. The input impedance is configurable to 30 kΩ or 50 kΩ. Due to switchable capacitors which can be added to the feedback in seven steps a low pass characteristics with configurable corner frequencies is realised. This can be used for antialiasing and high frequency noise suppression if the used sampling frequency is below the maximum possible sampling frequency of the transient recorder (100 MS/s). In an eighth step the input buffer can be used with full bandwidth. Because of the large driving capability of the input buffer no additional output drivers are required on the test device.

![figure 2](image-url)

**Figure 2.** Input buffer circuit.
2.2 Characterisation results

The input buffer was tested for noise, input range, dynamic range and frequency response. The input voltage is only limited to the voltage rails by the ESD protection diodes. In an input voltage range $V_{pp}$ from 0 V to 2.9 V ($V_{cm} = 1$ V, $f_{in} = 50$ kHz) the measured buffer linearity is better than ±1%. Within the rail limits an arbitrary common mode voltage can be used.

The observed frequency response is in almost perfect agreement to a first order low pass characteristics. Minimum and maximum corner frequency and the full bandwidth as well as the measured noise density are given in table 1 for both input impedances.

| Characteristics                  | 30 kΩ       | 50 kΩ       |
|----------------------------------|-------------|-------------|
| Minimum corner frequency         | 1.07 ± 0.02 | 0.69 ± 0.01 | MHz         |
| Maximum corner frequency         | 6.63 ± 0.03 | 4.35 ± 0.03 | MHz         |
| Full 3 dB bandwidth              | 43.97 ± 4.04| 34.03 ± 3.07| MHz         |
| Noise density                    | 52.9 ± 1.7  | 64.7 ± 2.1  | nV/√Hz      |

3 Trigger and threshold DAC

3.1 Architecture

The trigger unit is used to trigger the transient recording of the digitisation back end and can be operated in two modes. The first mode is a simple leading edge discriminator with a threshold given by an integrated 10 bit $R - 2R$ DAC. In a more sophisticated mode a switched capacitor circuit is used to trigger on the differentiated input signal. As the derivative of a cyclic signal is proportional to the frequency, low frequency signals are suppressed this way. This can be used to be insensitive to low frequency interferences like baseline drifts or low frequency noise and interferences e.g. power supply noise.

Figure 3 shows a schematic diagram of the switched capacitor trigger. During phase $\Phi_1$ the input voltage is stored in $C_1$ and the threshold voltage is stored in $C_2$. The used OTA [3] has an offset compensation which is calibrated during $\Phi_1$ also. Then in phase $\Phi_2$ the $C_1$ is switched into the feedback and the charge stored in $C_2$ is transferred to $C_1$. The output voltage of the switched capacitor stage which is now $U_{in} - C_2/C_1 \times U_{thres}$ is used as threshold voltage of the following comparator. On the leading edge of $\Phi_1'$ the comparator takes the decision:

$$U_{in}(t) > U_{in}(t - \Delta t) - \frac{C_2}{C_1} U_{thres}$$

$$\Rightarrow \frac{\Delta U_{in}}{\Delta t} < \frac{2 C_2}{T C_1} U_{thres}.$$  (3.1b)

According to the 2-phase clock $\Delta t$ is half of the clock cycle time $T$. $\Phi_1$, $\Phi_1'$ and $\Phi_2$ are adjusted with small delays to avoid charge loss during phase transitions and guarantee a stable input at the comparator decision. The design maximum clock frequency is 100 MHz corresponding to the
transient recorders sampling rate and the design value of the ratio $C_2/C_1$ is a tradeoff between trigger threshold granularity and range. It was chosen to be 0.5. The trigger noise has to be smaller than the preamplifier noise which is 4 mV rms in the designated application [4].

**Figure 3.** Schematic diagram of the switched capacitor trigger.

### 3.2 Characterisation results

The trigger unit was tested and characterised in both modes. In addition the characteristics of the threshold DAC was determined which is a common component used in both modes. This DAC is a 10 bit differential DAC operating rail to rail on the 1.8 V supply. The usefull digital input range with a DAC output range of ±1V is 200 to 800. Inside this range the measured mean DAC voltage step is $U_{\text{LSB}} = 3.29$ mV with a standard deviation of 0.26 mV and the integral linearity is better than 1$U_{\text{LSB}}$.

#### 3.2.1 Leading edge discriminator

In the leading edge discriminator mode the trigger was characterised by threshold scans at various DC levels at the input. For each input DC level a Gauss error function is fitted to the trigger incidence versus DAC value data points. The mean DAC value and the noise width of these fitted error functions are plotted in dependency of the input DC voltage in figure 4 on the left side.

**Figure 4.** Center and width of $S$-curves fitted to threshold scans versus input voltage in the leading edge mode (left) and the differential mode (right).
3.2.2 Switched capacitor trigger

The switched capacitor trigger was realised on silicon for the first time. On the test chip the sample and hold (S & H) stage output of one channel is connected to output pads. This enables tests of this stage directly. As expected it has a linear characteristic with an offset given by the threshold DAC. Remarkable is that the slope of the S & H stage characteristic is significantly below 1 (0.984(3)). This affects the differentiation and reduces the suppression of the level sensitivity of the trigger. The offset dependency from the DAC voltage that is connected to the ratio $C_2/C_1$ in eq. (3.1b) is 0.506 which is very close to the design value of 0.5.

Figure 4 shows on the right side the results of threshold scans in the switched capacitor mode. For perfect operation a constant function would be expected. For the observed S & H gain below 1 a DC dependency was calculated which is shown as green data points and the measured characteristic is shown as blue data points. The slope of a linear function fitted to the measurement (87.0 V$^{-1}$) is 4.4 times larger than the linear slope for the calculated data points (19.7 V$^{-1}$).

The trigger noise shows an asymmetry. At negative input voltages it is comparable to the leading edge discriminator noise while it is larger at positive input voltages.

To evaluate the response of the switched capacitor trigger on signals first derivative a ramp transient generated with a Tektronix AWG5208 was feed into the test device and threshold scans were performed in the baseline region as well as in the ramp region as shown in figure 5. On the left side of figure 6 it is visible that the distance from baseline to ramp threshold scans grows with increasing ramp slope. The threshold distance $\Delta N_{DAC}$ which is defined as difference of ramp threshold and baseline threshold are shown on the right side of figure 6. From eq. (3.1b) with $U_{\text{Thres}} = \Delta N_{DAC} \times U_{\text{LSB}}$ and $T = 100$ ns corresponding to a clock frequency of 10 MHz one would expect a slope sensitivity of 32.9 mV/μs while the value one gets from the measurement in figure 6 is 33.9(1) mV/μs.

![Figure 5. Ramping transient and threshold scans for evaluation of switched capacitor trigger.](image-url)
Figure 6. Left side: threshold scans of ramp signal. The trigger incidence is plotted versus DAC value. The blue line corresponds to the threshold scan in the baseline one and the red line to the ramp zone. Right side: threshold distance over ramp slope.

4 Conclusion

The input buffer works as expected and fulfills its requirements. The trigger unit including the new switched capacitor trigger option works as designed. While the trigger unit fulfills the noise requirements in the leading edge discriminator mode the performance of the switched capacitor mode is not yet satisfying. Open issues which are currently under investigation are the asymmetry of the trigger noise and the weak suppression of the level sensitivity of the trigger.

Acknowledgments

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