HAO: Hardware-aware Neural Architecture Optimization for Efficient Inference

Zhen Dong*, Yizhao Gao*, Qijing Huang, John Wawrzynek, Hayden K.H. So, Kurt Keutzer
University of California, Berkeley
The University of Hong Kong
{zhendong,qijing.huang,johnw,keutzer}@berkeley.edu, {yzgao,hso}@eee.hku.hk

Abstract—Automatic algorithm-hardware co-design for DNN has shown great success in improving the performance of DNNs on FPGAs. However, this process remains challenging due to the intractable search space of neural network architectures and hardware accelerator implementation. Differing from existing hardware-aware neural architecture search (NAS) algorithms that rely solely on the expensive learning-based approaches, our work incorporates integer programming into the search algorithm to prune the design space. Given a set of hardware resource constraints, our integer programming formulation directly outputs the optimal accelerator configuration for mapping a DNN subgraph that minimizes latency. We use an accuracy predictor for different DNN subgraphs with different quantization schemes and generate accuracy-latency pareto frontiers. With low computational cost, our algorithm can generate quantized networks that achieve state-of-the-art accuracy and hardware performance on Xilinx Zynq (ZU3EG) FPGA for image classification on ImageNet dataset. The solution searched by our algorithm achieves 72.5% top-1 accuracy on ImageNet at framerate 50, which is 60% faster than MnasNet [37] and 135% faster than FBNet [43] with comparable accuracy.

I. INTRODUCTION

Modern complex deep neural networks (DNNs) are able to achieve unparalleled accuracy in a wide range of applications at the expense of their much increased computing requirements. To successfully deploy these computationally demanding DNNs in resource-constrained edge systems such as an embedded FPGA, while maintaining real-time performance, system designers must therefore engage in difficult tradeoffs between model accuracy and implementation efficiency. There are three common approaches to improve the efficiency of DNN and the corresponding hardware design for edge deployment: 1) quantize the model to achieve efficient representations of DNNs, 2) select less compute-intensive operations and design efficient DNN architectures, and 3) design specialized hardware. The three design techniques altogether form a large design space for developing efficient DNN accelerator solutions at the edge.

Quantization [9], [19], [50], [53] is a general and effective technique that uses low bitwidth (such as 4-bit or 8-bit) to represent the floating-point weights/activations in neural networks. To achieve a better trade-off between accuracy and efficiency, mixed-precision quantization was introduced to allow different layers to have different bitwidths. Mixed-precision quantization leads to an exponentially large search space to find the optimal bitwidths. Prior work [11], [40], [44] adopts differentiable search, reinforcement learning, or sensitivity analysis to tackle this problem. However, the computational cost of these approaches is non-trivial. Besides, these works solely focus on quantization without co-considering the neural architecture design or efficient hardware implementation.

The second approach to achieve efficient inference is designing compact neural network architecture. Compared to manually designing networks, neural architecture search (NAS) algorithms [6], [26], [27], [37], [55] can automatically find network architectures that are more accurate and efficient. However, the NAS algorithm typically requires training sampled networks/sub-networks to get feedback on different neural architectures, which makes NAS algorithms computationally expensive to gain enough feedback and achieve good performance. In practice, NAS algorithms either heuristically prune the architectural search space or use proxy tasks to reduce the computational cost, leading to sub-optimal DNN architectures.

The hardware design, in common practice, is performed separately with software. Such practice can lead to sub-optimal performance because quantization and NAS target hardware-agnostic metrics such as model size or FLOPs. These performance proxies do not guarantee high inference speed on different hardware designs. As an example, the quantization algorithm may select a mixture of every bitwidth from 1 bit to 8 bit, and the NAS algorithm may choose to jointly use convolution with different kernel and group sizes. Though this solution can be small in model size or FLOP counts, on embedded FPGA devices with limited resources (such as Zynq ZU3EG), supporting all these operations at the same time is inefficient or even infeasible.

Consequently, a joint search among quantization, neural architecture, and hardware implementation is necessary to expose the optimal configurations of DNN and the corresponding accelerator design. Previous work [20], [44], [49] searched quantization schemes with different hardware configurations, but left their DNN architecture untouched. [6], [37], [43] searched for efficient neural architectures on specific hardware platforms, but did not consider the impact of quantization and hardware design. [1], [14], [15], [21] covered hardware design and neural architectures in their search space but did not include quantization. Though [7], [20], [25], [28] covered all three aspects, their search space is limited.

In this work, we explore the joint search space of neural
architecture, quantization, and hardware design. Instead of pruning the space by heuristics, or applying reinforcement learning or derivative-based search algorithms, we formulate the search as an integer programming problem, so that efficient optimization algorithms can be used to reduce computational cost. Based on our hardware latency model and network accuracy predictor, we propose a hardware-aware neural architecture optimization (HAO) method to generate pareto-optimal DNN designs to run on embedded FPGAs. Our contributions are as follows:

1) We formulate the design of neural architecture, quantization, and hardware design jointly as an integer programming problem.
2) We use a subgraph-based latency model for FPGAs, and we use a network accuracy predictor to reduce the computational cost of the automatic design flow.
3) HAO achieves state-of-the-art performance on ImageNet with Zynq ZU3EG FPGA. Our model can achieve 72.5% Top-1 accuracy running with 50 FPS, which is 60% faster than MnasNet and 135% faster than FBNet with comparable accuracy.

II. RELATED WORK

A. Efficient Deep Learning

Quantization [7], [9], [11], [19], [40], [50], [53] is a practical method to achieve efficient inference, which uses low bitwidth to represent weights and activations in a given neural network model. Since uniformly applying ultra-low precision quantization can cause accuracy degradation, mixed-precision quantization [10], [40], [54] is used to recover the accuracy. Mixed-precision quantization allows different layers in a neural network to have different bitwidth, leading to an exponentially large search space for the optimal bitwidth setting. [40] applies reinforcement learning to explore the space, and [44] uses differentiable search to decrease the required search time. [10] introduces Hessian-based sensitivity analysis to determine bitwidth, while obtaining the Hessian information has a high computational cost.

Instead of compressing a large pre-trained model, previous work [18], [29], [33], [38] focus on directly designing compact neural network architectures that can achieve decent accuracy with small model size or FLOPs. To avoid manual efforts, neural architecture search (NAS) algorithms have been proposed to automatically design pareto-optimal network architectures. Previous NAS methods [26], [55] use a reinforcement learning agent to explore the design space of neural architectures, which typically requires a large number of computational resources (48,000 GPU hours). [52] applies evolutionary algorithm to search for efficient neural architectures, which is feasible but also costly (75,600 GPU hours). Differential search based NAS methods [6], [27], [37], [43] significantly reduce the search cost by 1) using a supernet with weight sharing [50] and 2) applying continuous relaxation on the discrete search space so that gradients can be used to assist searching. However, differentiable NAS algorithms often lead to a small search space due to the limitation of supernets, which makes it sub-optimal if the design space is not already well-explored.

B. Hardware-aware Search

Since inference speed is dependent on characteristics of specific hardware platforms, simply applying quantization or NAS algorithms based on proxy metrics (model size or FLOPs) can be sub-optimal. To solve this problem, many hardware-aware search algorithms have been introduced to seek efficient deployment of DNNs on targeted hardware platforms. These methods [41], [6], [22], [34], [37], [40], [43], [48] usually retrieve latency or energy feedback from a given hardware platform, and search for optimal DNNs that can meet certain application constraints. Note that the hardware design is fixed in these methods, and thus is not in the search space.

To further improve the efficiency, in recent years, a few works have extended the NAS framework by integrating hardware design into the search space [1], [2], [14], [15], [20], [21], [25], [28], [46], [51]. Generally, these software/hardware co-search algorithms adopt pre-defined hardware design templates and incorporate several high-level design hyperparameters in the search framework. In addition to neural architectures, some works also incorporated quantization in their search space. [28] captures the relationship between quantization bitwidth and LUTs consumption on FPGA, and developed a NAS algorithm under the constraint of LUTs. In [20], the authors integrate several model compression techniques in the search framework and use quantization to reduce the latency of weight loading. [25] proposes a uniformed differentiable search algorithm using gumbel-softmax to sample discrete implementation hyperparameters including quantization bitwidth.

Although previous methods consider hardware design choices, the size of searchable space is still limited by the search algorithm efficiency and the total computation budget. Consequently, enlarging hardware search space may result in the shrinkage of software search space. In this work, we propose a subgraph-based hardware latency model, together with an accuracy predictor for neural architectures and quantization. Based on these, we are able to formulate the software/hardware co-search as an integer programming problem, which can be effectively optimized with a very small computational cost.

III. METHODOLOGY

In HAO, we expose a large design space in both hardware and algorithm configurations to accelerate DNNs. To efficiently navigate the search space, we first apply integer programming to prune the hardware configuration space by minimizing the latency subject to a set of hardware resource constraints. We then narrow the DNN architecture space by adopting Monte Carlo tree search (MCTS) [24] to minimize the quantization accuracy perturbation while satisfying a given latency constraint. In addition, we develop an accuracy predictor to estimate the accuracy of the DNN to further reduce the overall feedback time for each sample. Our flow produces a pareto-optimal curve between latency and accuracy.
A. Hardware Design

We target FPGA in this work to demonstrate how co-designed hardware and DNN fully exploit the optimization opportunities in hardware with limited resources while achieving on-par accuracy. In this section, we model the resource consumption and the computation latency for different types of convolution kernels. On top of that, we formulate the overall resource constraints and latency objectives as an integer programming problem for the subgraph-based design, which will serve as the latency simulator in the following DNN architecture optimization.

1) Hardware Subgraph Template: As shown in Fig. 1 in HAO, we adopt a subgraph-based hardware design. A subgraph consists of several convolution kernels that are spatially mapped on hardware, which also corresponds to the major building block of neural architecture. For a given hardware subgraph, the possible building blocks for neural architecture also include all the sub-layers of the subgraph since each kernel is implemented with a skip signal to bypass its compute in hardware. Each invocation to the accelerator computes one subgraph in the DNN architecture. The intra-subgraph results are buffered and streamed on FPGA and the inter-subgraph activations are communicated through DRAM.

We implement a parameterizable accelerator template in high-level synthesis (HLS). The generated dataflow accelerator can contain M convolution kernels chained through FIFOs to exploit pipeline-level parallelism. Each convolution kernel can be chosen from one of the three convolutions from the kernel pool: Conv k × k, Depthwise Conv k × k [9], and Conv 1 × 1. The hardware implementation of each kernel typically comprises a weight buffer, a line buffer, a MAC engine, and a quantization unit to rescale outputs. All the computational units are implemented using integer-only arithmetics as in [19].

2) Hardware Resource Modeling: This section describes the modeling details of different FPGA resources. We adopt a bottom-up design flow to model the utilization of LUTs and DSPs for low-bit multiply-accumulate (MAC) operations on FPGA. In addition, our model derives the BRAM utilization based on data size and precisions as well as the parallelization factors of the compute kernels. Table I lists the notations used in this paper.

LUTs: Both DSPs and LUTs can be used for computation on FPGA. It is more efficient to perform ultra low-bit computation on LUTs compared with DSPs. We use pragma to direct the mapping of low-precision MAC operations to LUTs in HLS. To build a precise model, we perform full logic synthesis to obtain the LUTs consumption on low-bitwidth multipliers and adders. Fig. 2 shows the LUTs consumption on different activation and weight bitwidths ranging from 2 to 8. We denote the LUT resource lookup function of multipliers as $L_M(Q_w, Q_a)$ where $Q_w$ and $Q_a$ represent the bitwidth of weights and input activations respectively. Derived from the logic synthesis results, the LUT consumption of the adders $L_A(Q_p)$ for carrying out $Q_p$ bit partial sum accumulation can be expressed as $L_A(Q_p) = Q_p + 7$.

DSP: The embedded DSP slice on FPGA supports the MAC operation in the following format:

$$P_1 = A \times (B + C) \quad (1)$$

In naive HLS mapping, one DSP slice is configured to support one MAC. To improve DSP throughput for low-bit operations, we use the shift-and-pack method in [12] to efficiently map two MACs on one DSP by leveraging the additional pre-adder. Given the input activation $a$ and the weights $w_1$ and $w_2$ for two different output channels, as shown in Fig. 3, the packing algorithm first sign-extends $w_1$ to 27 bits and left shifts $w_2$ by 18 bits. The output $P$ can be further accumulated with the partial sum or separated into two products $P_1$ and $P_2$. This
shift-and-pack method can be applied to the situation when \(w_1\) and \(w_2\) are no larger than 8 bits.

**BRAM:** We assume a buffering scheme in which we fully exploit reuse opportunities. The 18-Kb BRAMs usage \(B_w\) for the weight buffer can be calculated as:

\[
B_w = \left\lceil \frac{N_w \times Q_w}{PF} \right\rceil \times PF
\]

where \(N_w\) is the maximum number of weights to store on-chip, \(Q_w\) is the bitwidth of weights, and \(PF\) is the BRAM partition factor of the weights buffer. For convolution kernel with size \(k > 1\), we implement a line-buffer to maximize input reuse. The number of BRAMs \(B_i\) needed for line buffer is:

\[
B_i = \left\lceil \frac{(W \times C)_{\text{max}}}{Q_w} \right\rceil \times k
\]

where \((W \times C)_{\text{max}}\) is the maximum product between the size of image width \(W\) and channel \(C\) over the entire network. Our line buffer implementation merges the input width and channel dimension of the feature map into one dimension, and \(k\) rows of line buffers are allocated for \(k \times k\) convolution kernel.

3) **Hardware Resource Allocation:** With the resources modeling, we can further estimate the optimal resource allocation for a hardware subgraph under the resource constraints of the target FPGA. For full \(k \times k\) Conv, given the input channel parallelization factor \(PI\) and output channel parallelization factor \(PO\), the compute engine loads \(k^2 \times PI\) inputs in parallel and computes \(PO\) output partial sums. The total BRAM usage \(N_{wbuf}\) for on-chip buffers is:

\[
N_{wbuf} = \begin{cases} 
B_w + B_i & k > 1 \\
B_w & k = 1 
\end{cases}
\]

The engine is composed of \(k^2 \times PI \times PO\) MAC units that can be mapped to either DSPs or LUTs, incurring usage in LUTs \(N_{luts}\) or DSPs \(N_{dsp}\):

\[
N_{luts} = k^2 \times PI \times PO / 2
\]

\[
N_{dsp} = k^2 \times PI \times PO \times (L_M(Q_w, Q_a) + L_A(Q_p))
\]

For \(k \times k\) Depthwise Conv where each output channel result is corresponding to the inputs from the same channel, we use only \(PO\) to denote the channel dimension parallel factor. The \(k \times k\) computation engine takes \(k^2 \times PO\) input and computes \(PO\) partial sums concurrently. Similarly, the BRAM usage for the compute kernel is:

\[
N_{wbuf} = B_w + B_i
\]

The LUT or DSP usage to support depthwise convolution grows linearly with the \(PO\) parallelism factor:

\[
N_{luts} = k^2 \times PO \times (L_M(Q_w, Q_a) + L_A(Q_p))
\]

\[
N_{dsp} = k^2 \times PO
\]

Regarding the Quantization unit that converts partial sum in high-precision to quantized input for the next layer, we implement it with DSP with a parallelization factor of \(PO\). Its overall resource usage is:

\[
N_{dsp} = PO, N_{wbuf} = B_w
\]

Since we perform channel-wise quantization on weights, each output channel has its own quantization scale. We thus set the number of buffered scales \(N_q\) to \(OC\). The calculation of \(B_w\) is similar to \(B_w\) in Eqn. [2] The bitwidth of scale \(Q_w\) ranges from 16-24 depending on the actual value range after obtaining the integer scale using the inference scheme in [19]. The total BRAM usage \(N_{bram}\) is a sum of weight buffer usage \(N_{wbuf}\) and scale buffer usage \(N_{sbuf}\):

\[
N_{bram} = N_{wbuf} + N_{sbuf}
\]

4) **Hardware Latency Objective:** Given a layer with input channel size \(IC\), output channel size \(OC\), input height \(H\) and width \(W\), the compute latency is:

\[
Lat_{comp} = \begin{cases} 
H \times W \times \left\lceil \frac{IC}{PI} \right\rceil \times \left\lceil \frac{OC}{PO} \right\rceil & \text{if full} \\
H \times W \times \left\lceil \frac{IC}{PO} \right\rceil & \text{if depthwise} 
\end{cases}
\]

Depending on if the kernel type is full or depthwise convolution. The communication latency for loading the activation on-chip and off-chip can be roughly calculated as:

\[
Lat_{in} = H \times W \times IC \times Q_w / bw
\]

\[
Lat_{out} = H \times W \times OC \times Q_w / bw
\]

where \(bw\) is the practical bandwidth of off-chip memory. Similarly, the latency of loading weights can be estimated as:

\[
Lat_{w} = \begin{cases} 
k^2 \times IC \times QC_w / bw \times \left\lceil \frac{OC}{PO} \right\rceil & \text{if full} \\
k^2 \times IC \times QC_w / bw & \text{if depthwise} 
\end{cases}
\]

Based on the latency model for a single layer, we can further derive the latency of computing a subgraph. A hardware subgraph design with \(M\) convolution kernels can be represented as \(S = \{K_1, K_2, ..., K_M\}\) with specific quantization bitwidths \(Q = \{Q_1, Q_2, ..., Q_M\}\). For a given network architecture \(A = \{a_1, a_2, ..., a_N\}\), the subgraph mapping \(\{g_1, g_2, ..., g_L\}\) can be generated using a grouping function \(f_m\):

\[
\{g_1, g_2, ..., g_L\} = f_m(\{a_1, a_2, ..., a_N\})
\]

To model the overlapping of the dataflow architecture, the latency of computing each \(g_i\) can be approximated using the maximum latency over all the subgraph layers. Besides, to execute each layer on hardware, the accelerator will preload the weights to the on-chip buffer before the kernel starts, and apply double-buffering to hide the communication overhead.

### Table I

Notations for hardware design

| Notation | Description | Notation | Description |
|----------|-------------|----------|-------------|
| \(H\)    | feature map height | \(Q\)    | quantization setting |
| \(W\)    | feature map width  | \(Q_w\)  | activation bitwidth |
| \(PO\)   | parallelism on output channel | \(PF\)   | array partition factor |
| \(PI\)   | parallelism on input channel | \(L_M\)  | LUTs usage of a Multiplier |
| \(LUTs\) | LUTs usage of an Adder   |
| \(B_w\)  | line buffer BRAM usage  |
| \(B_i\)  | weights BRAM usage    |
| \(A\)    | hardware subgraph          |
| \(N\)    | number of layers in \(A\) |

\(N_{bram}\) is the sum of weight buffer usage \(N_{wbuf}\) and scale buffer usage \(N_{sbuf}\):
of the input activations. The overall latency for computing a subgraph can be written as:

\[
Lat(g_i) = \max(Lat^{1}_{i1}, Lat(a_{i1}), ..., Lat(a_{iM}), Lat^{M}_{iM}) + \sum_{j=1}^{M} Lat^{j}_{ij}
\]  

(14)

With the hardware analytical model above, we can then formulate the automatic hardware design problem as an integer programming that minimizes the overall latency:

\[
\begin{align*}
\min & \quad \sum_{i=1}^{L} Lat(g_i) \\
\text{s.t.} & \quad \sum_{k \in S} N^{k}_{dip} \leq T_{dip} \\
& \quad \sum_{k \in S} N^{k}_{lun} \leq T_{lun} \times \beta \\
& \quad \sum_{k \in S} N^{k}_{bbram} \leq T_{bbram}
\end{align*}
\]  

(15)

where \(T_{dip}, T_{lun}, T_{bbram}\) are the total resources available on the target FPGA device. Note that \(\beta\) is an empirical parameter describing the percentage of total LUTs allocated for MAC computation, which is set to 50% in our experiments. We treat this formulation as a sub-program to the DNN design optimization which will be covered in the next section. Given the explicitly expressed constraints and objective, we are able to directly generate the corresponding hardware implementation that minimizes the latency for different DNN design choices with different quantization schemes and kernel types.

B. DNN Design

Co-search of hardware-friendly neural network architectures and mixed quantization precisions is computationally intensive and time-consuming. In HAO, we formulate the search to an integer programming problem. In Sec. [III-B1] we present our search space of neural architectures. Given a latency constraint, we can first search feasible neural architectures and corresponding mixed-precision bitwidth settings by applying the aforementioned hardware latency model as well as a model quantifying the effect of quantization perturbation. We then use an accuracy predictor to compare across different networks and find the pareto-optimal architectures and quantization settings among all candidates.

1) Search Space of Neural Architectures: In HAO, we construct the neural network architectures from subgraphs with feasible hardware mappings on FPGAs. Our subgraphs are combinations of operations such as convolution or depthwise convolution with kernel size of \(1 \times 1\) or \(k \times k\) as mentioned in the previous section. Although only one subgraph can be chosen on hardware, the possible building blocks for neural architecture search include the sub-layers of the subgraph. This is because each layer in the subgraph can be decided whether to bypass or not using a skip signal in hardware.

We set no limit on the total number of subgraphs and choose the channel size for different layers from \(\{16, 32, 64, 128, 256, 512, 1024\}\). We also consider input resolution in HAO with potential configuration from \(\{96, 128, 160, 192, 224, 256\}\). Consequently, our search space is significantly larger compared to the prior work [6], [27], [37], [43], [45]. For example, in [37], the same cell configuration is repeated within every block. A standard search setting is to use 5 blocks with 3 identical cells in each block, and each cell, typically with 3 layers, has a sub-search space of 432, resulting in a search space of size \(432^5 \approx 10^{13}\). In comparison, even with a simple subgraph \(\{1x1 \text{ convolution}, 3x3 \text{ depthwise convolution}\}\), assume the number of layers is 45 (same as [37]), the size of search space in HAO is \((2 \times 7)^{45} \approx 10^{27}\). The large search space of HAO makes it more likely to encompass designs with good efficiency and high accuracy for broader deployment scenarios with various hardware and latency constraints.

2) Integer Programming: Given a latency constraint \(Lat_0\), we use integer programming to obtain feasible neural architectures and corresponding quantization settings. Specifically, based on the aforementioned hardware simulator, inference latency (Lat) is a function (denoted as \(L\)) of neural architecture (A) and the quantization setting (Q) for subgraph. In Eqn. 16, \(i\) and \(j\) are layer index, \(N\) represents the total number of layers, and \(M\) represents the number of layers in a subgraph.

\[
Lat = L(A, Q), \\
A = \{k_i, H_i, W_i, IC_i, OC_i, S_i, i \in [1, N]\} \\
Q = \{Q^i_{a}, Q^i_{w}, j \in [1, M]\}
\]  

(16)

In HAO, perturbation, denoted as \(Pert\), is used to estimate the accuracy degradation caused by quantization. For a given neural architecture, the accuracy of the full-precision pretrained model is irrelevant to quantization setting \(Q\). The perturbation models the relative accuracy change to the pretrained network among different \(Q\). As shown in Eqn. 17, the perturbation should be multiplied with a constant \(\lambda\) to have the same scale as accuracy, but this will not change relative accuracy ranking since \(PretrainedAcc\) in Eqn. 17 is a constant. As in [10], the total perturbation \(Pert\) can be estimated by summing the perturbation contributed from each layer \(Pert_i\). Using the norm of \(\Delta W_i\) (the distance between the quantized tensor and the original tensor \(W_i\)) and the trace of Hessian matrix \(H_i\), the \(Pert_i\) can be calculated as follows (\(i\) is the layer index).

\[
\begin{align*}
Acc &= PretrainedAcc - \lambda Pert, \\
Pert &= \mathbb{P}(A, Q) = \sum_{i=1}^{N} Pert_i, \\
Pert_i &= \overline{tr} H_i \cdot \|\Delta W_i\|_2^2,
\end{align*}
\]  

(17)

With a latency constraint \(Lat_0\), we need to find feasible neural architecture \(A\) and then determine corresponding quantization setting \(Q\) to minimize perturbation. Note that \(A\) contains integer architectural parameters (kernel size, feature resolution, channel number, stride, etc), and \(Q\) contains the bitwidths of layers in the subgraph, which are integer values chosen from \(\{2, 3, 4, 5, 6, 7, 8\}\). Therefore, the task to find \(A\) and \(Q\) satisfying latency constraint \(Lat_0\) can be formulated as an integer programming problem as shown in Eqn. 18.
Fig. 4. Illustration of HAO pipeline.

\[
\min_{Q} P(A, Q), \\
\text{s.t. } L(A, Q) \leq Lat_0
\]  

(18)

The latency constraint in Eqn. (18) can be modified to Eqn. (19) to reduce the number of neural architecture candidates. This modification is based on the assumption that neural architectures with higher latency tend to have more complex structures and higher expression capability, and therefore higher accuracy. \( \alpha \) here is a hyperparameter ranging from 0 to 1. A larger \( \alpha \) can lead to a lower search cost.

\[
\alpha Lat_0 \leq L(A, Q) \leq Lat_0
\]  

(19)

We apply Monte Carlo tree search (MCTS) \(^{24}\) for better sample efficiency on finding feasible neural architectures and quantization bitwidths that satisfy Eqn. (18) and Eqn. (19). Benefiting from its online model, MCTS can dynamically trade off exploration and exploitation, which makes MCTS hard to be trapped in local optimum compared to other methods such as Bayesian optimization or greedy algorithms. With the heuristic that \( L(A, 2bit) \leq L(A, Q) \leq L(A, 8bit) \), we first find \( A \) that satisfies Eqn. (20) and then solve for appropriate quantization setting \( Q \). We follow the standard to set \( A \) (then \( Q \) in the next step) as state, and our actions are selected from \{increase/decrease channel, increase/decrease resolution, skip/unskip a layer, add/delete a subgraph, termination\}. More details about MCTS can be found in \(^3\), \(^{24}\), \(^{41}\).

\[
\alpha Lat_0 \leq L(A, 8bit) \\
L(A, 2bit) \leq Lat_0
\]  

(20)

3) Accuracy Predictor: As discussed in Sec. III-B2, given a latency constraint \( Lat_0 \), neural architecture candidates and corresponding quantization settings can be obtained with different perturbation. To compare among different neural architectures, a predictor is used to estimate the accuracy of pre-trained models with given architectures. In HAO, we directly stack architectural parameters of each layer together as the input vector, and then we apply a support vector regression (SVR) model to predict the accuracy. It should be noted that we choose SVR predictor for simplicity and better sample efficiency, since SVR models generally require fewer data to train compared to neural networks used in \(^39\), \(^{32}\). To quickly train the predictor, we collect \{architecture, accuracy\} data by training 10 large neural networks from scratch and then reusing the weights while fine-tuning them to 200 different architectures. In our experiments, all neural networks are built by linearly stacking subgraphs, meaning that they are generally similar to each other. To support more complicated architectures such as DenseNet \(^{16}\) or LSTMs \(^{56}\), as suggested in \(^39\), \(^{42}\), using a better strategy (such as autoencoder) for neural architecture representation, using semi-supervised learning with unlabelled data, and using graph convolutional networks (GCN) as the predictor can further improve performance, with the cost of more computation resources and time.

We use the accuracy predictor to sort candidates that satisfy the latency constraint \( Lat_0 \). Since the accuracy predictor can be shared with different subgraphs, we repeat the aforementioned process for all subgraphs and select the top neural architectures and corresponding quantization settings\(^1\). We finally train them from scratch on ImageNet and then quantize the models as the final results of HAO.

IV. RESULTS

A. Simulator Performance

In Sec. III-A, we present an analytical latency simulator that can quickly estimate the inference latency given a DNN architecture. The optimization algorithm in Sec. III-B2 uses the simulator to obtain quick latency feedback.

To test the effectiveness of our latency simulator, we synthesize several accelerators for different MobileNetV2 and HAO designs. The hardware parameters of different implementations are automatically generated by hardware optimization in Eqn. (15). To calibrate our latency model for the target FPGA, we first perform linear regression to fit the cycle prediction to the hardware execution latency. We obtain a calibrated latency model \( 1.27 \times Lat + 3.8 \) and use it for our latency prediction. Then for different accelerator implementations, we obtain the latency pairs from our simulator and the real hardware execution and plot them in Fig. 5. We observe a strong linear relationship \( (r = 0.998) \) between the real inference latency and the estimated latency.

In addition to the hardware latency simulator, HAO also uses an accuracy predictor to reduce the computational cost. We show the performance of the predictor in Fig. 5. As can be seen, for different CNN models in our search space, the

\(^1\)In our experiments we train top 5 architectures with corresponding quantization settings and choose the best one for a given latency constraint.
results of our accuracy predictor align well with the actual test accuracies on ImageNet validation dataset.

B. Experimental Results

In this section, we present the accuracy and latency results of HAO on the Ultra 96 board with a Xilinx Zynq ZU3EG FPGA. We show that HAO outperforms manually designed solutions, as well as solutions with automatically searched DNN architectures and quantization settings.

Fig. 6 shows the pareto frontier of HAO with respect to accuracy and latency. MobileNetV2 [33] is a popular neural architecture manually designed for efficient inference. The original MobileNetV2 is in floating-point format. To achieve a fair comparison, we quantize MobileNetV2 to 8-bit weights and 8-bit activations, and then run it on FPGA with a \{1x1 convolution, 3x3 depthwise convolution, 1x1 convolution\} subgraph. We follow [33] to change the channel width multiplier (selected from \{1.0, 0.75, 0.5, 0.3\}) and input resolution (selected from \{224, 192, 160, 128, 96\}) of MobileNetV2, in order to trade-off latency and accuracy. In comparison, the neural architecture (including input resolution) and quantization bitwidth setting are automatically selected in HAO. As can be seen, HAO outperforms MobileNetV2 on a wide range of latency values. HAO can achieve 72.5% top-1 accuracy with 20ms latency (50 fps), which is more than 1% higher accuracy than MobileNetV2 while running 15% faster. In the cases with a more strict latency constraint (for example autonomous vehicles), HAO can still preserve 66% accuracy with only 8ms latency (125 fps). This is significantly higher than the 63% of MobileNetV2 while being faster. Furthermore, we compare with results from MnasNet [37], which is a hardware-aware neural architecture search method. As in Fig. 6, HAO also outperforms MnasNet by a large margin.

In addition to comparing pareto-frontier performance with our own hardware implementation, we also compare HAO with various previous work in Table II. [13], [23], [31], [35] are manually designed solutions. [20], [25] are search-based methods. Note that these prior works target larger FPGA boards with more resources, and some use more complex neural architectures, 16-bit fixed-point or floating-point precision. For a fair comparison, we further compare HAO with [4], [33], [37], [43], [47], which have the same hardware platform (Zynq ZU3EG) as our\(^1\). For HAO, we apply layer-wise quantization for activations and channel-wise quantization for weights, with standard linear quantizer and static quantization for the simplicity of deployment. As can be seen in Table II, HAO achieves state-of-the-art performance on embedded FPGA with limited resources. With higher top-1 accuracy (68.8% vs 68.3%), HAO solution is significantly faster than Synergy [47] (94fps vs 66fps), albeit Synergy is assisted by extra operations such as shift. Moreover, when the framerate is 50fps, HAO can achieve 72.5% top-1 accuracy on ImageNet, which is more than 1% higher than MnasNet-A1 (71.4%) while being 14% faster. Comparing with FBNet-iPhoneX, HAO obtains slightly better accuracy (72.7% vs 72.6%), while having a much higher framerate (45 vs 21). It should be noted that for different hardware platforms or different latency constraints, previous methods need to repeat the whole search pipeline to find appropriate solutions, while the predictor in HAO can be shared so that no additional search cost will be required.

Table III shows the hardware resource utilization and power usage for HAO on Zynq ZU3EG FPGA. We observe 4.3W
TABLE II
Performance comparison on ImageNet with prior works.

| Platform | Input Resolution | FrameRate(fps) | Quantization Bitwidth | Top-1 Accuracy(%) |
|----------|------------------|----------------|-----------------------|-------------------|
| EDD-Net-2 | Zynq ZU3EG | 224 × 224 | 125.6 | W16A16 | 74.56 |
| HotNas-MnasNet | Zynq ZU3EG | 224 × 224 | 200.4 | NA | 73.24 |
| HotNas-ProxylessNAS | Zynq ZU3EG | 224 × 224 | 205.7 | NA | 73.39 |
| EDD-Net-3 | Zynq ZC7045 | 224 × 224 | 40.2 | W16A16 | 74.4 |
| VGG16 | Zynq XCV7045 | 224 × 224 | 27.7 | W16A16 | 69.3 |
| VGG-SVD | Zynq XCV7045 | 224 × 224 | 4.5 | W16A16 | 64.64 |
| VGG16 | StrataX-V | 224 × 224 | 3.8 | W8A16 | 66.58 |
| VGG16 | Zynq TZ020 | 224 × 224 | 5.7 | W8A8 | 67.72 |
| Dorefa | Zynq TZ020 | 224 × 224 | 106.0 | W2A2 | 46.10 |
| Synergy | Zynq ZU3EG | 224 × 224 | 66.3 | W4A4 | 68.30 |
| FINN-R | Zynq ZU3EG | 224 × 224 | 200.0 | W1A2 | 50.30 |
| MobileNetV2 | Zynq ZU3EG | 224 × 224 | 43.5 | W8A8 | 71.40 |
| MnasNet-A1 | Zynq ZU3EG | 224 × 224 | 22.3 | W8A8 | 74.60 |
| MnasNet-A1 | Zynq ZU3EG | 192 × 192 | 27.8 | W8A8 | 73.33 |
| MnasNet-A1-0.75 | Zynq ZU3EG | 160 × 160 | 31.0 | W8A8 | 72.70 |
| MnasNet-A1-0.37 | Zynq ZU3EG | 160 × 160 | 35.8 | W8A8 | 71.35 |
| FBNet-B | Zynq ZU3EG | 224 × 224 | 24.6 | W8A8 | 73.20 |
| FBNet-iPhoneX | Zynq ZU3EG | 224 × 224 | 21.3 | W8A8 | 72.62 |
| HAO | Zynq ZU3EG | 256 × 256 | 44.9 | W-mixed A8 | 72.68 |
| HAO | Zynq ZU3EG | 256 × 256 | 50.0 | W-mixed A8 | 72.45 |
| HAO | Zynq ZU3EG | 224 × 224 | 58.9 | W6A8 | 71.76 |
| HAO | Zynq ZU3EG | 224 × 224 | 77.0 | W-mixed A8 | 70.06 |
| HAO | Zynq ZU3EG | 192 × 192 | 93.5 | W-mixed A8 | 68.80 |

TABLE III
Hardware resources utilization and power

| LUTs | FF | DSP | BRAM | Power |
|------|----|-----|------|-------|
| 61362(87.0%) | 55136(69.0%) | 360(100%) | 431(99.8%) | 5.5W |

In this work, we propose HAO to jointly optimize the neural architecture, quantization, and hardware design. To reduce the computation required for evaluating different designs, we develop a subgraph-based hardware latency model as well as an accuracy predictor for neural architectures. We formulate the algorithm and hardware co-search as an integer programming problem, which significantly prunes the total search space. On an embedded FPGA device, we show that our HAO method finds the pareto-optimal designs which outperform previous solutions on both latency and accuracy.

V. CONCLUSIONS

In this work, we propose HAO to jointly optimize the neural architecture, quantization, and hardware design. To reduce the computation required for evaluating different designs, we develop a subgraph-based hardware latency model as well as an accuracy predictor for neural architectures. We formulate the algorithm and hardware co-search as an integer programming problem, which significantly prunes the total search space. On an embedded FPGA device, we show that our HAO method finds the pareto-optimal designs which outperform previous solutions on both latency and accuracy.

ACKNOWLEDGMENTS

This work was supported by Facebook Reality Labs, Google Cloud, Alibaba, Samsung SAIT, by the Berkeley ADEPT Lab, Berkeley Deep Drive, the Berkeley Wireless Research Center, by the Croucher Innovation Award, and by CONIX Research Center.
Quantization and training of neural networks for efficient integer-arithmetic-only inference. In Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition, pages 2704–2713, 2018.

[20] Weiyi Jiang, Lei Yang, Edwin H-M Sha, Qingfeng Zhuge, Shouzhen Gu, Sakyasingha Dasgupta, Yiyu Shi, and Jingtong Hu. Hardware/software co-exploitation of neural architectures. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 39(11):4154–4165, 2020.

[21] Weiyi Jiang, Xinyi Zhang, Edwin H-M Sha, Lei Yang, Qingfeng Zhuge, Yiyu Shi, and Jingtong Hu. Accuracy vs. efficiency: Achieving both through fpga-implementation aware neural architecture search. In Proceedings of the 56th Annual Design Automation Conference 2019, pages 1–6, 2019.

[22] Li Jiao, Cheng Luo, Wei Cao, Xuegong Zhou, and Lingli Wang. Accelerating low bit-width convolutional neural networks with embedded fpga. In 2017 27th International Conference on Field Programmable Logic and Applications (FPL), pages 1–4. IEEE, 2017.

[23] Levente Kocsis and Csaba Szepesvári. Bandit based monte-carlo planning. In European conference on machine learning, pages 282–293. Springer, 2006.

[24] Yuhong Li, Cong Hao, Xiaofan Zhang, Xinheng Liu, Yao Chen, Jinjun Xiong, Wen-mei Hwu, and Deming Chen. Edi: Efficient differentiable dnn architecture and implementation co-search for embedded ai solutions. arXiv preprint arXiv:2005.02563, 2020.

[25] Chencheng Liu, Barret Zoph, Maxim Neumann, Jonathon Shlens, Wei Hu, Li-Jia Li, Li Fei-Fei, Alan Yuille, Jonathan Huang, and Kevin Murphy. Progressive neural architecture search. In Proceedings of the European Conference on Computer Vision (ECCV), pages 19–34, 2018.

[26] Hanxiao Liu, Karen Simonyan, and Yiming Yang. Darts: Differentiable architecture search. arXiv preprint arXiv:1806.09055, 2018.

[27] Qingsong Lu, Weiyi Jiang, Xiaowei Xu, Yiyu Shi, and Jingtong Hu. On neural architecture search for resource-constrained hardware platforms. arXiv preprint arXiv:1911.00105, 2019.

[28] Ningning Ma, Xiangyu Zhang, Hai-Tao Zheng, and Jian Sun. Shufflenet v2: Practical guidelines for efficient cnn architecture design. In Proceedings of the European conference on computer vision (ECCV), pages 116–131, 2018.

[29] Hieu Pham, melody Y Gun, Barret Zoph, Quoc V Le, and Jeff Dean. Efficient neural architecture search via parameter sharing. arXiv preprint arXiv:1802.03268, 2018.

[30] Jiatao Qiu, Jie Wang, Song Yao, Kaiyuan Guo, Boxun Li, Erjin Zhou, Jincheng Yu, Ningsi Xu, Sen Song, et al. Going deeper with embedded fpga platform for convolutional neural network. In Proceedings of the 2016 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, pages 26–35, 2016.

[31] Esteban Real, Alok Aggarwal, Yanping Huang, and Quoc V Le. Regularized evolution for image classifier architecture search. In Proceedings of the 2019 Conference on Artificial Intelligence, volume 33, pages 4780–4789, 2019.

[32] Mark Sandler, Andrew Howard, Menglong Zhu, Andrey Zhmoginov, Li-Jia Li, Li Fei-Fei, Alan Yuille, Jonathan Huang, and Kevin Murphy. Mobilenetv2: Inverted residuals and linear bottlenecks. In Proceedings of the IEEE conference on computer vision and pattern recognition, pages 4510–4520, 2018.

[33] Florian Schiederger, Luca Benini, Costas Bekas, and A Cristiano I Malossi. Constrained deep neural network architecture search for iot devices accounting for hardware calibration. In Advances in Neural Information Processing Systems, pages 6056–6066, 2019.

[34] Naveen Suda, Vikas Chandra, Ganesh Dasika, Abinash Mohanty, Yufei Ma, Sarma Vrudhula, Jae-sun Seo, and Yu Cao. Throughput-optimized opencl-based fpga accelerator for large-scale convolutional neural networks. In Proceedings of the 2016 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, pages 26–35, 2016.

[35] Martin Sundermeyer, Ralf Schl¨uter, and Hermann Ney. Lstm neural network for language modeling. In Proceedings of the 2016 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, pages 26–35, 2016.

[36] Martin Sundermeyer, Ralf Schluter, and Hermann Ney. Lstm neural network for language modeling. In Proceedings of the 2016 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, pages 26–35, 2016.

[37] Martin Sundermeyer, Ralf Schluter, and Hermann Ney. Lstm neural network for language modeling. In Proceedings of the 2016 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, pages 26–35, 2016.

[38] Martin Sundermeyer, Ralf Schluter, and Hermann Ney. Lstm neural network for language modeling. In Proceedings of the 2016 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, pages 26–35, 2016.

[39] Martin Sundermeyer, Ralf Schluter, and Hermann Ney. Lstm neural network for language modeling. In Proceedings of the 2016 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, pages 26–35, 2016.

[40] Martin Sundermeyer, Ralf Schluter, and Hermann Ney. Lstm neural network for language modeling. In Proceedings of the 2016 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, pages 26–35, 2016.

[41] Martin Sundermeyer, Ralf Schluter, and Hermann Ney. Lstm neural network for language modeling. In Proceedings of the 2016 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, pages 26–35, 2016.
[39] Yehui Tang, Yunhe Wang, Yixing Xu, Haning Chen, Boxin Shi, Chao Xu, Chunjing Xu, Qi Tian, and Chang Xu. A semi-supervised assessor of neural architectures. In Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition, pages 1810–1819, 2020.

[40] Kuan Wang, Zhijian Liu, Yujun Lin, Ji Lin, and Song Han. Haq: Hardware-aware automated quantization with mixed precision. In Proceedings of the IEEE conference on computer vision and pattern recognition, pages 8612–8620, 2019.

[41] Linnan Wang, Saining Xie, Teng Li, Rodrigo Fonseca, and Yuandong Tian. Sample-efficient neural architecture search by learning action space. arXiv preprint arXiv:1906.06832, 2019.

[42] Wei Wen, Hanxiao Liu, Yiran Chen, Hai Li, Gabriel Bender, and Pieter-Jan Kindermans. Neural predictor for neural architecture search. In European Conference on Computer Vision, pages 660–676. Springer, 2020.

[43] Bichen Wu, Xiaoliang Dai, Peizhao Zhang, Yanghan Wang, Fei Sun, Yiming Wu, Yuandong Tian, Peter Vajda, Yangqing Jia, and Kurt Keutzer. Fbnet: Hardware-aware efficient convnet design via differentiable neural architecture search. In Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition, pages 10734–10742, 2019.

[44] Bichen Wu, Yanghan Wang, Peizhao Zhang, Yuandong Tian, Peter Vajda, and Kurt Keutzer. Mixed precision quantization of convnets via differentiable neural architecture search. arXiv preprint arXiv:1812.00090, 2018.

[45] Yuhui Xu, Lingxi Xie, Xiaopeng Zhang, Xin Chen, Guo-Jun Qi, Qi Tian, and Hongkai Xiong. Pc-darts: Partial channel connections for memory-efficient differentiable architecture search. arXiv preprint arXiv:1907.05737, 2019.

[46] Lei Yang, Weiwang Jiang, Weichen Liu, HM Edwin, Yiyu Shi, and Jingdong Hu. Co-exploring neural architecture and network-on-chip design for real-time artificial intelligence. In 2020 25th Asia and South Pacific Design Automation Conference (ASP-DAC), pages 85–90. IEEE, 2020.

[47] Yifan Yang, Qijing Huang, Bichen Wu, Tianjun Zhang, Liang Ma, Giulio Gambardella, Michaela Blott, Luciano Lavagno, Kees Vissers, John Wawrzynek, et al. Syntegra: Algorithm-hardware co-design for convnet accelerators on embedded fpgas. In Proceedings of the 2019 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, pages 23–32, 2019.

[48] Yang Yang, Chao Wang, Lei Gong, and Xuehai Zhou. Fpnet: Customized convolutional neural network for fpga platforms. In 2019 International Conference on Field-Programmable Technology (ICFPT), pages 399–402. IEEE, 2019.

[49] Zhewei Yao, Zhen Dong, Zhangcheng Zheng, Amir Gholami, Jiali Yu, Eric Tan, Leyuan Wang, Qijing Huang, Yida Wang, Michael W Mahoney, et al. Hawq3: Dyadic neural network quantization. arXiv preprint arXiv:2011.00680, 2020.

[50] Dongqing Zhang, Jiaolong Yang, Dongqiangzi Ye, and Gang Hua. Lq-nets: Learned quantization for highly accurate and compact deep neural networks. In Proceedings of the European conference on computer vision (ECCV), pages 365–382, 2018.

[51] Xinyi Zhang, Weiwang Jiang, Yiyu Shi, and Jingdong Hu. When neural architecture search meets hardware implementation: from hardware awareness to co-design. In 2019 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pages 25–30. IEEE, 2019.

[52] Xiaofan Zhang, Junsong Wang, Chao Zhu, Yonghua Lin, Jinjun Xiong, Wen-mei Hwu, and Deming Chen. Dnbuilder: an automated tool for building high-performance dnn hardware accelerators for fpgas. In 2018 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pages 1–8. IEEE, 2018.

[53] Aojun Zhou, Anbang Yao, Yiwen Guo, Lin Xu, and Yurong Chen. Incremental network quantization: Towards lossless CNNs with low-precision weights. International Conference on Learning Representations, 2017.

[54] Yiren Zhou, Seyed-Mohsen Moosavi-Dezfooli, Ngai-Man Cheung, and Pascal Frossard. Adaptive quantization for deep neural network. In Thirty-Second AAAI Conference on Artificial Intelligence, 2018.

[55] Barret Zoph and Quoc V Le. Neural architecture search with reinforcement learning. arXiv preprint arXiv:1611.01578, 2016.