A Total Dose Irradiation Test System

Kun Zhang¹, Na Yan¹, Fan Yang² and Xiaodong Zhao²

¹ Xi’ an Taiyi Electronics Co., Ltd., Xi’an, Shanxi, 710065, China
² Northwestern Polytechnical University, Unmanned System Research Institute, Xi’an Shanxi, 710072, China

*Corresponding author’s e-mail: yf4095@mail.nwpu.edu.cn

Abstract: In this paper, a set of generalized test system for total dose irradiation test is designed. Through the establishment of related hardware platform and related test chip according to the adaptation requirements, the device can be observed in real time under the radiation environment. The total dose test was irradiated with the ⁶⁰Co source, and it worked normally when different total doses were selected. In this article, a unit library test chip based on 130nm SOI technology is selected for testing. During the test, the system works stably and functions normally.

1. Introduction

The space radiation environment mainly comes from galactic cosmic rays, solar electromagnetic radiation and the earth’s radiation belt. The galactic cosmic rays are particles with extremely high energy, mainly protons, with strong penetrating ability. The solar cosmic rays are mainly high-energy protons, which are ejected when large solar flares occur. The Earth’s radiation belt poses the greatest radiation threat to aerospace electronic components. They are mainly composed of high-energy protons and high-energy electrons. Microelectronic devices and circuits are to be used in a radiation environment, and the reliability of their radiation resistance must be considered.

The total dose effect (TID) is that when the device is exposed to ionizing radiation, the radiation will generate electron-hole pairs in the oxide layer. Related to the energy of the incident particle is the energy obtained by the ionized electrons or holes, and more electrons and holes will be ionized. Yes, in the silicon dioxide, a part of the electrons and holes will recombine, and the remaining electrons will be swept out of SiO₂ and enter the electrode. The remaining holes will be trapped by the traps in the SiO₂ and become positive oxide trap charges. The interface state is induced at the interface, and the trapped charge and interface state of the irradiated oxide layer will cause the threshold of the device to drift, which will lead to characteristic degradation or circuit failure.

In order to effectively study and suppress the impact of the total dose effect on the integrated circuit, in addition to theoretical analysis of the total dose effect and related reinforcement strategies, it is also necessary to test the specific radiation resistance ability of the integrated circuit through a certain test method. Ground radiation sources mainly use ⁶⁰Co, ¹³⁷Cs, X-rays, etc. as simulated radiation sources. The ⁶⁰Co source is a commonly used radiation source and is used as a standard radiation source for total dose radiation experiments. This article proposes a universal irradiation system for the ⁶⁰Co source radiation environment, which is used to test the total dose irradiation test.

[1] proposed an effective TID method to solve the problems of actual ionization dose deposition and charge production in a small volume. (Applicable to ⁶⁰Co source), [2] is committed to the development and verification of a new method for the combined use of X-ray and gamma-ray radiation for TID...
investigations. [3] studied the geometric scaling of key simulation design parameters of MOS transistors irradiated under high TID. [4] proposed an on-chip $^{90}$Sr/$^{90}$Y electron source as an alternative method for TID testing. Comparing the complexity and experimental results of $^{60}$Co and $^{90}$Sr/$^{90}$Y TID test setups for complex SoCs, [5] studied and proved the use of X-ray testing as a supplement to the method of flip-chip FPGA TID testing to identify the most sensitive circuits. This test method can be used to test any flip-chip FPGA based on Flash and SRAM.

The test system proposed in this paper includes a power control board for power supply and excitation, and a test board for the cell library circuit. Under the $^{60}$Co radiation source, the test is carried out by means of online test and displacement test.

2. Total dose irradiation test system

![Figure 1 Schematic diagram of total dose test environment](image1)

The test system designed in this article is mainly composed of a power management board, a test board to be tested, cables, and power supply and observation instruments. Figure 1 is a schematic diagram of the test system. The following is the detailed design of each part of the system.

2.1 Power control management board

On the test control and power management board, a power management module is provided to supply power to the control board. In addition, four power management modules will be provided, which can supply power to 4 test boards at the same time. It uses a 5V input voltage and a regulated power supply can be used in the test. This board provides 3.3V and 1.2V output power supply. The four power modules are powered by four independent power supply interfaces, which is convenient for independent observation of the working current of four or less tested samples.

In addition, the power control management board also uses commercial MCU devices to manage stimulus signals such as clocks and reset signals.

The design scheme of the test control and power management board is shown in Figure 2. The physical map is shown in Figure 3.

![Figure 2 Schematic diagram of power management](image2)
![Figure 3 Physical diagram of power management](image3)
2.2 Test board to be tested

A socket is placed on each total dose test board, and the test sample is placed in the socket to facilitate sample replacement. During the total dose test, all samples are in a dynamic running state. Therefore, it is necessary to provide current to the test board from the outside, and some pins of the test samples need to be in a fixed bias state to reduce the number of leads. The structure of the total dose test board in this article is shown in Figure 4. The board includes a CQFP128 test socket, an input end plug-in, an output end plug-in, and four SMB connectors to suit part of the output signal observation. The input ports that are not connected to the input plug-in adopt a fixed bias; the output ports that are not connected to the output plug-in are all in a floating state.

The board to be tested is connected to the power supply through various connectors and outputs signals through the connectors. The actual test board to be tested is shown in Figure 5.

3. Introduction to the unit library test chip

The irradiation test system designed in this article is tested by a 130nm SOI process cell library test chip, which can effectively detect the working status of the system under the irradiation environment. The following is the introduction of the test chip.

Figure 6 is a photo of the layout of the unit test chip. The DIE size without the dicing slot is 3.94mm*4.04mm. The package form adopts CQFP128.

The unit test chip concentrates on the test for each library unit, including the STD unit and the IO unit. Its core feature is to cover the functional test of all units. Through the chain structure design, the performance test is realized. The library test chip design is based on the STD library design of HVT. The library test chip design follows the rule table as shown in Table 1.
Table 1 The library test chip design follows the rule table

| Serial | Test | Structure |
|--------|------|-----------|
| 1      | delay | INV/BUF/DEL test chain, 4000 units, 2 drive capabilities, 2 loads |
| 2      | function | All STD CELL function tests, input signal traversal |
| 3      | register | Carry out the register chain test, covering the reset, set, and test |

Figure 7 is a schematic diagram of the structure of the unit test chip.

Figure 7 Schematic diagram of unit test chip Figure 8 Schematic diagram of the total dose test board

Figure 9 is a schematic diagram of a combinational logic test structure. The input of each combinational logic is generated by frequency division of the input clock CLK_in. The output of each tested cell is output after time-sharing selection by State_l. Among them, the registers of the InputGenerate part and State_MUX part adopt a three-mode structure.

Figure 9 Schematic diagram of combinational logic test structure

Only the test sample is placed on the total dose test board, and the sample is in the worst biased state during the test, and is in a normal working state. The sample is subjected to functional tests and ATE tests before and after irradiation.

4. Total dose test procedure and conclusion

This paper designs a unit test chip testchip for total dose irradiation test.

In order to test the suppression ability of the unit library test circuit to the total dose irradiation environment, Table 2 shows the basic overview of the total dose test.

Table 2 Basic overview of total dose test

| Test name | Total dose irradiation test |
|-----------|-----------------------------|
| Test content | Unit library test chip total dose irradiation experiment |
| Number of samples | 4 |
| Sample technology | 130nm SOI |
| Dose rate | 49.8 Rad(Si)/s |
| Total dose | 300K Rad(Si) |
| Experimental test plan | Online test + ATE test |
This total dose test adopts online test plus ATE shift test method. The specific test arrangement is as follows: During the total dose effect test, the test sample is placed on the test circuit board, the test circuit board is placed at the radiation source, and the power supply circuit board is about 5 meters away from the test circuit board. The board provides power, clock and other working conditions for the circuit on the test circuit board. The power management board is interconnected with control and test equipment such as the power supply outside the shielded wall through a 50-meter cable. The test sample on the test board is under power-on dynamic test conditions, and the output result is observed through the power supply to observe the current and voltage, and the output signal through the oscilloscope. The test environment includes three parts: the test control system, the test irradiation system, and the test monitoring system. The test irradiation system is the test irradiation panel, which is placed at the irradiation source. The test control system provides power for the irradiation test panel, and the test monitoring system is placed in the observation room to receive the test status of the test test system, observe the current and voltage changes of the test board, and output the signal to the oscilloscope through a long cable for signal observation.

The total dose test process is shown in Figure 10. When the specified total dose is irradiated, the electrical parameter test after the radiation is performed. If the electrical parameter test after the radiation is abnormal, the room temperature annealing is performed and the electrical parameter test is performed; If the electrical parameter test is normal, continue with the 50% excess irradiation test, and perform the high-temperature annealing experiment, and perform the electrical parameter measurement. The total dose set in this article is 300K Rad (Si). After the 300K Rad (Si) irradiation is completed, the sample is taken out and tested for ATE. Then carry out 450K Rad (Si) over-dose irradiation, after finishing the irradiation, carry out high temperature annealing for 168 hours, and then carry out ATE test.

The test platform works stably under the irradiation environment of 300KRad (Si) and overdose 450KRad (Si). It functions normally. It supplies power to the test board under test and provides excitation signals. After a long period of operation, there is no functional error.

5.Concluding
In this paper, a test system for total dose irradiation is developed, and the self-developed 130nm SOI unit test chip is subjected to irradiation test through this system. The specific irradiation test data of the unit test chip is obtained, which proves this total-dose irradiation test system designed in the paper has the characteristics of stable work in a radiation environment, complete functions, and long-term stable work. It is a set of total-dose irradiation test system with strong versatility.

Acknowledgments
The work is financially supported by the Aviation Science Foundation (201907053005) and Aviation Science Foundation(2019ZC053018). The authors thank the editor and reviewers for their valuable and helpful suggestions.

References
[1] D. Lambert et al., "TID Effects Induced by ARACOR, 60Co and ORIATRON Photon Sources in MOS Devices: Impact of Geometry and Materials," in IEEE Transactions on Nuclear Science.
[2] L. N. Kessarinskiy et al., "Compendium of TID Comparative Results under X-Ray, Gamma and LINAC Irradiation," 2014 IEEE Radiation Effects Data Workshop (REDW), 2014, pp. 1-3.
[3] L. Chevas et al., (2018)"Investigation of Scaling and Temperature Effects in Total Ionizing Dose (TID) Experiments in 65 nm CMOS," 2018 25th International Conference "Mixed Design of Integrated Circuits and System" (MIXDES), pp. 313-318.
[4] A. Menicucci et al., (2018)"Simplified Procedures for COTS TID Testing: A Comparison Between 90Sr and 60Co," 2018 IEEE Radiation Effects Data Workshop (REDW), pp. 1-6.
[5] N. Rezzak, J. Wang, V. Nguyen and D. Dsilva, (2017)"Combined x-ray and gamma ray testing to investigate the TID tolerance of flip-chip FPGAs," 2017 17th European Conference on Radiation and Its Effects on Components and Systems (RADECS), pp. 1-7.
[6] J. B. Habarulema and Z. Katamzi, (2014) "TID related studies using satellite and ground based data over the African sector," 2014 XXXIth URSI General Assembly and Scientific Symposium (URSI GASS), pp. 1-1.

[7] J. Hofman, (2013) "In-Situ, Low Dose Rate, TID Test of the Power Supply Block of RadEx, a CubeSat Class Radiation Experiment Module," 2013 IEEE Radiation Effects Data Workshop (REDW), pp. 1-4.