Wafer-scale solution-processed 2D material analog resistive memory array for memory-based computing

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Realization of high-density and reliable resistive random access memories based on two-dimensional semiconductors is crucial toward their development in next-generation information storage and neuromorphic computing. Here, wafer-scale integration of solution-processed two-dimensional MoS2 memristor arrays are reported. The MoS2 memristors achieve excellent endurance, long memory retention, low device variations, and high analog on/off ratio with linear conductance update characteristics. The two-dimensional nanosheets appear to enable a unique way to modulate switching characteristics through the inter-flake sulfur vacancies diffusion, which can be controlled by the flake size distribution. Furthermore, the MNIST handwritten digits recognition shows that the MoS2 memristors can operate with a high accuracy of >98.02%, which demonstrates its feasibility for future analog memory applications. Finally, a monolithic three-dimensional memory cube has been demonstrated by stacking the two-dimensional MoS2 layers, paving the way for the implementation of two memristor into high-density neuromorphic computing system.

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dalog non-volatile memory devices capable of multi-states like memristors, promise to enable new classes of energy-efficient computation like in-memory computing and neuromorphic computing to disrupt conventional graphics processing unit (GPU)-based neural-network accelerators. In this case, memory devices assume compute roles beyond just data storage. As such, memory device endurance and variability comparable to logic devices are now desired. However, endurance and variability for analog resistive random access memory (RRAM), especially for resistive switching devices based on traditional amorphous and polycrystalline metal oxides continues to suffer material-level challenges due to the unavoidable tradeoffs between defect stability and defect recovery, forcing limited optimization window between endurance, programming voltage, and memory retention.

Two-dimensional (2D) materials with a wide variety of electronic properties including an expanded range of vacancy activation energies offer a new palette to engineer the switching materials and their defects for resistive memories. With improved large-scale growth techniques and the compatibility with CMOS integration, emerging 2D materials have attracted increasing attention in memristive devices. Recent studies have revealed that 2D materials, with their unique edge and layered properties, can be more accurately tuned to enhance their switching characteristic not seen in oxide-based memristive devices. Several intriguing performance milestones have been achieved so far in 2D memristive devices, eg., sub-pA current with femtojoule per bit energy consumption; operation up to 50 GHz in radio frequency switches; switching thresholds approaching 100 mV; stable operation up to 340 °C and switching in sub-nanometer thickness. However, most of these reports are based on isolated device without indication of its viability in large-scale arrays. Despite 10 × 10 memristive crossbar arrays being demonstrated by chemical vapor deposition (CVD) h-BN, the high growth temperature and post-synthesis transfer process increase the integration complexity, thus impeding their implementation in large-scale circuit application. With low process temperature and compatibility with high-precision optical lithography patterning, solution-processed 2D materials offer a practical approach to co-integrate 2D material with Si CMOS to enhancing future on-chip computational functionality.

The liquid-exfoliated 2D nanosheets retain pristine crystal quality and clean van der Waals interfaces, thus ensuring excellent charge transport. Analogous to the grain boundaries defects in CVD-grown 2D materials, the edge defects in the liquid-exfoliated nanosheets assist the interlayer diffusion of conductive filament (CF) and present an efficient pathway for resistive switching (RS) modulation. This is further enhanced by the ability to control the size distribution and edge defects density of the liquid exfoliated 2D nanosheets. Despite the promises, the solution-processed 2D memristors devices reported to date are still challenged by poor endurance, low yield, and large device-to-device variation.

In this work, we demonstrate a reliable and scalable approach to fabricate memristor arrays at wafer-scale. Through solution processing and spin-coating on wafer, we produce a continuous thin-film network of monodispersed MoS2 nanosheets. Remarkably, the MoS2 memristor exhibits forming-free switching with a high endurance of $1 \times 10^7$ cycles, low device-to-device variability (19.7% for set and 18.5% for reset), excellent retention for 10 years, and a remarkable wafer-scale crossbar arrays scalability. Depth materials and property characterization reveal that the RS characteristics of the 2D MoS2 memristors are modulated by the sulfur vacancies ($V_S$) percolation along the flake edges. As a demonstration, we implemented a 3-layer convolutional neural network (CNN) model using the MoS2 memristors for the recognition of MNIST handwritten digits. With excellent switching linearity and low variation, our CNN model achieved high recognition accuracy of 98.02%. Furthermore, we proposed a 3D memory cube through layer-by-layer stacking the 2D MoS2 nanosheets in a transfer-free manner, opening a promising pathway for building 3D integrated circuits with 2D materials.

Results

Production of MoS2 nanosheets dispersion. The MoS2 bulk crystal was exfoliated into nanosheets by electrochemical intercalation followed by a mild sonication as illustrated in Fig. 1a (see Method). This process creates a dark green MoS2 suspension (Fig. 1b inset). The optical UV-Vis absorption spectroscopy of the obtained MoS2 suspension exhibits two excitonic peaks near 678 nm and 614 nm, suggesting the high-quality semiconducting MoS2 nanosheets. Raman spectroscopy indicates the existence of monolayer to few-layer MoS2 nanosheets. Distinct peak positions and high intensity at around 678 nm and 614 nm in photoluminescence spectroscopy (PL) are also observed in exfoliated MoS2 monolayers, consistent with the UV-Vis absorption spectroscopy, further confirming that the intrinsic electronic properties of MoS2 are preserved.

Fabrication and characterization of the MoS2 Film. Using the MoS2 nanosheets suspension, we prepare uniform MoS2 thin film on standard 2-inch Si/SO2 wafer via a simple spin coating process, achieving a smooth and continuous surface with roughness of 1.2 nm and average thickness ranging from 10.5 to 11.4 nm (Fig. 2a, Supplementary Fig. S3, 4). The smooth and continuous surface plays a significant role in the enhancement of device yield and reduction of the performance variability. Raman mapping of the patterned letters ‘NUS’ (Fig. 2b–d) together with identical Raman spectra at random spots on the MoS2 film (Fig. 2e) further confirm the superior uniformity and full coverage of the MoS2 film. With 2D layered morphology, the ultrathin MoS2 nanosheets can evenly and tightly overlap with each other to form a continuous thin film with reduced areal density of grain boundaries within the horizontal plane as evidenced by the scanning electron microscopy image (Fig. 2f).

The obtained MoS2 thin film possesses high crystallinity with perfect hexagonal atomic arrangement of Mo and S atoms in MoS2 basal planes (Fig. 2g), typical of a high-quality MoS2 flake. In addition, the tightly stacked MoS2 layers in the vertical direction have been confirmed by the cross-sectional scanning transmission electron microscopy (STEM) imaging and corresponding electron energy loss spectroscopy (EELS) mapping. As shown in Fig. 2h, the MoS2 stacking layers exhibit large-area plane-to-plane contact with nearly atomically flat 2D interfaces, ensuring efficient charge transport across the MoS2 stacks. EELS mapping of the MoS1 layers demonstrates the preservation of its...
Fig. 1 The liquid exfoliation of MoS₂ Nanosheets. a Schematic illustration of the liquid exfoliation process of bulk MoS₂ crystal. b UV-vis absorption spectrum of MoS₂-IPA solution. Inset is the photograph of the MoS₂-IPA dispersion. c Raman spectra of exfoliated MoS₂ nanosheets. Raman signal of bulk MoS₂ crystal is also presented for comparison. d Atomic force microscopy statistics indicating the flake thickness distribution of the MoS₂ dispersions. e The lateral flake size distribution of three types of MoS₂ dispersions. To be noted, arb. units refer to arbitrary units.

Fig. 2 Characterization of spin-cast MoS₂ thin film. a Optical image of the wafer-scale MoS₂ thin film. b optical image of patterned MoS₂ thin film and corresponding Raman mapping of E₁₂g mode (c) and A₁₁g mode (d). The scale bar in (b) is 10 μm. e Raman spectra collected on random spots from a. f SEM image of the MoS₂ thin film. The wrinkles are the edges of MoS₂ nanosheets. g Atomic resolution high-angle annular dark field (HAADF) STEM image of MoS₂ nanosheets (false-colored). h Cross-sectional HAADF-STEM image and i. corresponding elemental mapping of MoS₂ thin film. j The cross-sectional ADF-STEM image taken at the junction region of the MoS₂ thin film. k EELS spectra of region A and B taken from j.
intrinsic chemical composition without noticeable oxidation due to the room-temperature processing involved in materials preparation and device fabrication (Fig. 2i and Supplementary Fig. S5). Figure 2j shows the junction region of the two MoS2 stacking layers. Two EELS spectra of the S-L1,2 and the Mo-M4.5 edges have been obtained exactly at the junction site (region B) and away from the junction site (region A), respectively (Fig. 2k).

It clearly shows that region B has a weaker intensity in S-L1,2 edge, indicative of the sulfur deficiency at the junction region of MoS2 stacks. Furthermore, as an electron donor, V5 can effectively tune the work function of MoS2. As shown in Supplementary Fig. S6, the peripheral regions of MoS2 nanosheets possess distinctly more negative potential than the central region, corresponding to lower work function induced by V5. The defective edges serve as a vertical percolation path for V5 across the MoS2 stacks, offering a unique approach for the RS modulation of the solution-processable MoS2 memristor by engineering their flake sizes.

**Electrical characterization of the solution processable MoS2 memristor.** In order to gain insight into the underlying transport mechanism associated with V5 in the MoS2 switching layer, RS switching characteristics of a single MoS2 flake are examined. As shown in the conductive AFM (C-AFM) measurement (Supplementary Fig. S7), a large hysteresis window at low voltage in the I-V curve is observed at the flake edges, while being absent at the center of the flakes, thus revealing the importance of the V5 in the RS phenomenon. To be noted, the observed hysteresis in the C-AFM experiment shows the stable and repeatable RS behavior of the MoS2 memristors even in scaled devices down to 10 nm (tip size), demonstrating their ability for high-density memory integration. Furthermore, by applying constant voltage stress on the MoS2 memristors, we observe the characteristic random telegraph signal with two discrete conductance states, revealing the charge trapping and de-trapping related to V5 (Supplementary Fig. S8). The sweep rate-dependent set/reset threshold voltages imply that the memory effect of MoS2 memristors is dominated by nanionics transport mechanism (Supplementary Fig. S9)16, further confirming the significant role that V5 plays in the RS conduction mechanism in MoS2 memristor.

Considering that the V5 are confined at the edges of the MoS2 nanosheets, a strong correlation between MoS2 nanosheet size and the corresponding RS characteristics is expected. To validate that assumption, memristors with different MoS2 nanosheet sizes are fabricated (Supplementary Fig. S10). Their typical I-V characteristics are shown in Fig. 3a–c. All MoS2 memristors exhibit forming-free switching characteristics, promoted by the presence of V5 in the exfoliated MoS2 nanosheets, which would be favorable to produce smooth dielectric breakdown18,22,34–36. A clear bipolar switching with stable low resistance state (LRS) and high resistance state (HRS) is observed. Due to the presence of edge-confined V5, an anomalous nanosheet-size dependent RS characteristic have been observed, where the shrinking in the average nanosheets size (λ) results in a reduced set/reset voltage (V_set/V_reset) and their cycle-to-cycle variations. Specifically, the memristor with the smallest MoS2 nanosheets exhibits the lowest V_set (0.65 V)/V_reset (~0.90 V) and cycle-to-cycle switching voltage variations. The discrepancy in the switch voltage arises from the difference in nanosheet size-related V5 defect density. Consequently, smaller nanosheets are expected to have higher V5 density attributed to increased edge-to-basal plane ratio, implying the possibility of achieving ultra-low switching voltage by modulating the nanosheet size. Meanwhile, the nanosheet size plays an important role in the reduction of the cycle-to-cycle switching voltage variations. This is attributed to more uniform average V5 percolation length under the circumstance of smaller MoS2 nanosheets (Supplementary Fig. S11). Small MoS2 nanosheets are expected to provide a smoother and more uniform pathway for V5 percolation while larger flakes would produce more tortuous channels. The statistical analyses of 50 devices under different flake sizes further confirm the flake size dependent RS characteristics in MoS2 memristor (Supplementary Fig. S12). In order to better understand the geometric effect of the MoS2 nanosheets on the RS characteristics, the diffusion energy landscape of V5 is further explored by the density functional theory (DFT) calculations (details in Supplementary Note 1, Figure S13). Figure 3d shows the impact of the MoS2 molecular sizes on the V5 migration barriers. Clearly, decreasing the MoS2 molecular size results in the reduction of the diffusion energy barrier for V5, reaching a small V5 diffusion energy barrier of 0.75 eV, which is consistent with the reported behavior of polycrystalline MoS2 memristor17. Supported by the DFT calculations, the kinetics of the V5 diffusion reveals that the nanosheet size effect is highly related to the V5 diffusion barrier along the nanosheet edges, representing an effective way for the engineering of RS in MoS2 memristor.

Given that the migration of V5 is a thermodynamic process, it is expected that the MoS2 memristor should be influenced by temperature. Temperature dependent I-V sweeps at HRS and LRS states have been performed as shown in Fig. 3e, f. For both LRS and HRS profile, the current shows a non-linear relationship with voltage and increases with the increase of temperature, suggesting the existence of Schottky barrier. By considering different transport models, the I-V relationship under HRS and LRS states are well-fitted with Schottky emission model as a linear dependence of I on $E^{1/2}$ is obtained, where $J$ is the current density and $E$ is the electric field (Fig. 3g, h). The Schottky emission function is expressed as below:

$$J \propto A^* T^2 \exp[-q(\Phi_B - \sqrt{qE/4\pi\varepsilon\varepsilon_0}/(kT))]$$

where $T$ is the absolute temperature, $q$ is the electronic charge, $A^*$ is the effective Richardson constant, $\Phi_B$ is the Schottky barrier height, $k$ is the Boltzmann’s constant, $\varepsilon_0$ is the vacuum permittivity, and $\varepsilon$ is the optical dielectric constant. From the Schottky emission equation, the barrier height for HRS is calculated as high as 500 meV, whereas, the barrier height is greatly reduced to only 93 meV in LRS state. The double-logarithmic plots of the I-V curve of MoS2 memristor shows that the HRS state follows trap-associated space-charge limited conduction (SCLC) theory, while the LRS state is governed by Ohmic conduction behavior which is caused by the formation of conductive filaments (Supplementary Fig. S14). At HRS states, since the height of the Schottky barrier is very large, only few electrons can be injected from the metal to the semiconductor in MoS2 because the thermionic current exponentially decreases with the increasing of barrier height. In LRS state, the current gradually increases with increasing temperature, showing semiconductor-like behaviors, excluding the metal conductive filaments (Fig. 3e, g). By plotting $\ln I$ as a function of $T^{-1/4}$ (Fig. S14), the transport characteristics can be well fitted with the Mott-Variable range hopping model (Mott-VRH) at temperature above 110 K38,39. This suggests that the electrons hop through the conductive filament composed of V5 in the LRS states.

Based on the above observation, the mechanism of the MoS2 memristor is schematically illustrated in Fig. 3i, j. At HRS, the conduction mechanism follows the SCLC conduction. When positive voltage is applied to the top contact (Ti), the positively charged V5 diffuse along the MoS2 nanosheet edges towards bottom contact (Pt). As V5 approaching the Pt electrode, the Schottky barrier height is reduced at the Pt-MoS2 interface.
The continuous positive bias causes a large accumulation of VS and eventually results in the formation of VS conductive filaments, bridging the Ti and Pt electrode. The device is set to the LRS state (Fig. 3i). At LRS state, the conduction mechanism follows the Mott-VRH model, where electrons hop through the conductive filament composed of VS. When a negative bias is applied to the top electrode, VS are extracted backwards and the conductive filaments rupture (Fig. 3j). The device is reset to the HRS state. Meanwhile, the depletion of VS at the Pt-MoS2 interfaces leads to the increase in the Schottky barrier associated with reduced current conductance. Due to the migration of VS under voltage bias, we observe a dynamic modulation of the Schottky barrier near the MoS2-Pt interface with 500 meV and 93 meV under HRS and LRS, respectively. Overall, the conduction mechanism in the MoS2 memristors is dominated by the formation and rupture of the conductive filaments due to the percolation of VS along the nanosheet edges. Unlike the stochastic formation of CF in amorphous oxide-based memristor, the solution-processed MoS2 memristor enables a better control over RS characteristic due to the unique edge-confined VS conduction mechanism. Therefore, it provides an effective engineering way for the modulation of the RS characteristics via controlling the size of the MoS2 nanosheets, not possible in conventional oxides-based memristors.

Implementation of CNN with the solution-processed MoS2 memristor. The MoS2 memristor shows robust and reliable switching characteristics as supported by their excellent endurance and retention. As shown in Supplementary Fig. S15, the time-dependent resistance exhibits little change in ON and OFF state for $1 \times 10^5$ s without degradation and demonstrates extrapolated 10-year retention at 85 °C. Moreover, the repeatability has been studied through setting/resetting the device by voltage pulses up to $1 \times 10^7$ cycles (Fig. 4a). The resistances at the LRS and HRS extracted from different pulse cycles show record-high endurance, even comparable to the typical endurance of commercial flash memories. The uniform bipolar RS behavior can also be preserved when the device size is reduced to 100 nm × 100 nm (Supplementary Fig. S16), demonstrating good scalability of the proposed process. Given the superior uniformity of the MoS2 thin film and reliable performance in our MoS2 memristors, the wafer-scale MoS2 memristors arrays (Fig. 4b inset and Supplementary Fig. S17) were fabricated. To address the device-to-device reproducibility, the distributions of $V_{\text{set}}$ and $V_{\text{reset}}$ obtained by measuring 73 devices over the entire wafer has been done. As shown in Fig. 4b, the variations (defined as $\sigma/V_{\text{mean}}$) for set and reset voltages are calculated to be only 19.7% and 18.5%, which are much smaller as compared to other solution-processed 2D memory devices. Furthermore, the conductance of a 6 × 6 MoS2 memristor array was programmed into displaying the number “2” and alphabet “D”; spatially representing the analog conductance states across the array, over a period of 1 h without losing its programmed state (Supplementary Fig. S18).

The dynamic response of the solution-processed MoS2 memristors have been studied under pulsed electric stimuli with different amplitudes, durations and intervals. Overall, an accurate CNN training requires multibit analog resistive states and symmetric conductance change. Therefore, we characterized the

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**Fig. 3** Electrical performance characterization of the MoS2 memristors. a–c 200 representative I-V curves of MoS2 memristors made from suspensions A, B, and C, respectively. To be noted, the electrode size is 5 × 5 μm. d Calculated $V_d$ diffusion barrier energy versus flake size. I-V characteristics of MoS2 memristor measured at different temperatures in LRS (e) and HRS (f). Schottky emission fitting for LRS (g) and HRS state (h). Schematic diagrams of the set (i)/reset (j) process and corresponding interface band alignment. The light blue balls represent VS.
analog conductance response by applying sequence of pulse train consisting of set (1.5 V, 1 μs) and reset (-2 V, 10 μs) for potentiation-depression (P-D) pulses and read pulses (0.1 V, 1 μs) after each P-D pulse. As shown in Fig. 4c, the conductivity of the MoS2 memristors show analog potentiation and depression between different resistive states with a remarkably high on/off ratio of 160. The high analog on/off ratio in our MoS2 memristor is beneficial for accessing multiple synaptic weight values in neural network algorithms. Each of the ten selected conductive states shows no degradation in conductance over time, indicating excellent multilevel retention capability of the MoS2 memristor (Fig. 4d). The multiple memory states are programmable within single device, and further demonstrated to be highly reproducible among different devices. Despite our MoS2 memristor showing high analog memory states, the weight updates in an asymmetry way, especially at the start of the P-D cycle where the MoS2 memristor conductance abruptly arises and decays. The abrupt weight update can be ascribed to the fast switch time in our MoS2 memristors due to mobile V_S with reduced diffusion barrier energy. Indeed, as shown in Supplementary Fig. S21, the MoS2 has a fast switch time of 40 ns at a pulse amplitude of 2.0 V. Therefore, to avoid the abrupt potentiation and depression and reach a linear weight update, an incremental voltage operating scheme with a shorter pulse width and lower amplitude (potentiation: 1.0 V to 1.75 V with 15 mV steps, pulse width 100 ns; depression: -1.5 V to -2.25 V with steps of 15 mV; pulse width 500 ns) was applied to the MoS2 memristor. As a result, symmetric conductance potentiation and depression with nearly linear modulation have been achieved, with an on/off conductance ratio of 10, which is essential to implement reliable low-complexity and low-energy analog in-memory matrix multiplication. To estimate the effect of the MoS2 memristor on the pattern recognition accuracy, we performed a three-layer CNN simulation based on the MNIST handwritten data set. After training the 3-layer deep convolutional neural network (DCNN) implemented...
on MoS₂ RRAM array with 50,000 images using the in-memory computation technique, we achieved a high accuracy of 98.02% (Fig. 4f and Supplementary Table 1). Supplementary Table 1 benchmarks the overall performance metrics of different 2D materials-based memristors as well as the conventional oxide-based memristors. Our MoS₂ memristor shows the best performance in the integration size, endurance, learning accuracy and number of conductance states relative to other 2D materials. Especially, our proposed processes are transfer-free and room-temperature based, offering great compatibility with thermal budget limited 3D monolithic integration as well as flexible electronics. Moreover, our devices feature an alternate process dimension of performance modulation via flake size engineering, which is lacking in current oxide-based RRAMs. Despite limitations in high switching power and relatively large device variations of the current design, we believe there is still significant opportunity for improvement by materials, devices and circuits co-optimization in the future.

Demonstration of monolithic 3D memory cube. Monolithic 3D integration (M3D) of memory and logic component leads to high-density device, providing a promising avenue to address the integration (M3D) of memory and logic component leads to demonstration of monolithic 3D memory cube opportunity for improvement by materials, devices and circuits structure (Fig. 5b). The delicate 3D structure has been further ensuring the effective switching characteristics analog to their planar memristor counterpart (Fig. 5d, Supplementary Fig. S25d–f). Ultimately, a monolithic 3D circuit has been proposed based on the solution-processable 3D MoS₂ memristors. Figure 5e depicts a vertically stacked memory architecture with solution-processed 2D MoS₂ thin film as the active switching layer, sandwiched between metal lines of top and bottom electrodes. Etch node at the cross-point of the arrays represents an individual memory cell. Benefits provided by room-temperature process, the storage nodes are vertically stacked in a facile manner through a sequential spin-coating of 2D MoS₂ and deposition of metal contacts. Based on our previous reports on M3D integration⁴⁶,⁴⁷, inter-layer dielectric between each layer of metal lines and selectors at each node of cross-point can be readily integrated in our monolithic 3D circuits to minimize the cross-talk issue and accurately program each memory cell. As an example, the M3D integrated one transistor one RRAM (1T1R) arrays with corresponding circuit diagram are illustrated in Supplementary Fig. S26. Our demonstration shows that the solution-processed 2D materials can be 3D monolithically integrated in back-end-of-line (BEOL) for high density embedded memory for storage and analog computing.

Discussion

In summary, we demonstrate wafer-scale memristor arrays by using solution-processed MoS₂ nanosheets. The solution-processed MoS₂ memristor arrays exhibit robust and reliable performance with excellent endurance, low device-to-device variation, linear weight updates and high analog on/off ratio. Materials characterization and electrical measurement reveals that the migration of Vs along the edges of the MoS₂ nanosheets play a critical role, which provides a flake-based way for the RS modulation. The transfer-free processing of 2D layers at room temperature has the potential to be scaled up for mass production, and enable their integration on flexible substrates, thus providing a versatile platform for flexible and wearable electronics. With the excellent properties, the solution-processed MoS₂ memristor arrays can achieve 98.02% pattern recognition accuracy. Furthermore, a fully functional 3-layered memristors have been demonstrated based on the solution-processed 2D memristors, which provides a promising strategy for the M3D integration of 2D materials. The present work opens a door for large-scale and reliable memory integration based on 2D materials for neuromorphic computing implementation.

Methods

Preparation of MoS₂ nanosheets dispersions. Typically, MoS₂ single crystal was intercalated with tetraethylammonium bromide (Sigma-Aldrich) solution in acetonitrile (5 mg mL⁻¹). After the electrochemical intercalation, the MoS₂ crystal was rinsed with isopropyl alcohol (IPA) three times, followed by ultrasonication in dimethylformamide (DMF). The MoS₂ dispersion was centrifuged at 1000 rpm for 3 min. The supernatant was collected and named A. To prepare nanosheets with different sizes, the supernatant was collected and subjected to a second sonication for 6 h. Subsequently, the supernatant was centrifuged at 1000 rpm for 3 min. The sediment was collected and named D.

Fabrication of RRAM devices. To make the device, the MoS₂ nanosheets dispersion was directly spin-coated onto Si/SiO₂ substrate with pre-patterned bottom contact of Ti/Pt (30 nm/30 nm) at room temperature. After that, Ti contacts (30 nm) were deposited capped with Pt (30 nm) by e-beam evaporator to form the Ti/Pt-MoS₂-Ti/Pt crossbar devices.

Characterization. Room-temperature electrical measurement was conducted in a four-probe station connected to semiconductor parameter analyser (Agilent B1500A) and a waveform function generator (B1530, Agilent). Varied temperature...
Elemental mapping of the 3D stacked MoS$_2$ memristor. Cross-sectional TEM images of the full stack (a) and middle layer (b) of MoS$_2$ memristor. c Elemental mapping of the 3D stacked MoS$_2$ memristor. d I-V characteristics of 3D stacked MoS$_2$ memristors, showing stable and bipolar resistive switching at each layer. e Schematic diagram of 3D memristor array with buried metal interconnects and logic circuits.

Calculation details. All calculations were carried out using the density functional theory (DFT) with the generalized Perdew-Burke-Ernzerhof (PBE) and the projector augmented-wave (PAW) pseudopotential plane-wave method as implemented in the Vienna Ab initio Simulation Package (VASP) code. For the PAW pseudopotential of Mo, we included 4$d^3$ and 5$s^2$ as valence. For S, the $n=3$ shell was included as valence (3$s^2$ and 3$p^4$). A 12 × 12 × 1 Monkhorst-Pack $k$-point grid was used for monolayer unit cell geometry optimization and a plane-wave basis set with an energy cut-off of 500 eV was adopted. The optimized unitcell was used to build the multilayer MoS$_2$ flake with different sizes. In this study, we carried out calculations with the van der Waals correction by employing optB88-vdW functional. Good convergence was obtained with these parameters and the total energy was converged to 1.0 × 10$^{-6}$ eV per atom. No spin polarization was considered in this study. The energy minimization was performed using the limited memory BFGS method. The climbing-image Nudged Elastic Band (NEB) method was used to figure out the diffusion of S vacancy in the minimum energy landscape and energy barriers.

Data availability
The authors declare that the data that support the findings of this study are available within the article and its Supplementary Information files. All other relevant data are available from the corresponding author upon request.

Code availability
All relevant code or algorithm are available from the corresponding author upon request.

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Author contributions

B.T., and A.V.-Y.T. conceived the project and wrote the paper. B.T., Y.L., J.F.L., and M.S. fabricated the RAM devices. B.T. performed the MoS2 exfoliation, UV–vis, Raman, PL, and electrical measurements. Z.G.Y. and Y.-W.Z. performed the DFT calculation. H.V. contributed to the CNN simulation and data analyses. E.Z. contributed to the AFM measurement and analysis. M.W. and J.W. performed STEM and data analysis. B.T., and A.V.-Y.T. provided input into the design of the experiments and the preparation of the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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