A Standalone FPGA-based Miner for Lyra2REv2 Cryptocurrencies

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Abstract—Lyra2REv2 is a hashing algorithm that consists of a chain of individual hashing algorithms, and it is used as a proof-of-work function in several cryptocurrencies. The most crucial and exotic hashing algorithm in the Lyra2REv2 chain is a specific instance of the general Lyra2 algorithm. This work presents the first hardware implementation of the specific instance of Lyra2 that is used in Lyra2REv2. Several properties of the aforementioned algorithm are exploited in order to optimize the design. In addition, an FPGA-based hardware implementation of a standalone miner for Lyra2REv2 on a Xilinx Multi-Processor System on Chip is presented. The proposed Lyra2REv2 miner is shown to be significantly more energy efficient than both a GPU and a commercially available FPGA-based miner. Finally, we also explain how the simplified Lyra2 and Lyra2REv2 architectures can be modified with minimal effort to also support the recent Lyra2REv3 chained hashing algorithm.

Index Terms—Lyra2, Lyra2REv2, Lyra2REv3, hardware miner, FPGA miner, MPSoC miner, cryptocurrency

I. INTRODUCTION

RECENTLY, there has been a surge in the popularity of cryptocurrencies, which are digital currencies that enable transactions through a decentralized consensus mechanism. Most cryptocurrencies are based on a blockchain, which is an ever-growing list of transactions that are grouped in blocks. Individual blocks in the chain are linked together using a cryptographic hash of the previous block, which ensures resistance against modifications, and every transaction is digitally signed, typically by using public-key cryptography. Various mechanisms are used in order to deter denial-of-service attacks and, in particular, double-spending attacks where the same digital coin is used in multiple concurrent transactions. Many popular cryptocurrencies, including Bitcoin [2], use a proof-of-work (PoW) mechanism, which was first proposed in [3] to combat the problem of junk mail. The proof-of-stake (PoS) and proof-of-burn (PoB) mechanisms are other notable proposals.

The PoW system requires that new blocks provide proof that a function that requires a significant amount of a limited resource was used to construct them before they get accepted into the chain. For example, the employed function can be limited by the available processing power, the available memory, or the network bandwidth and latency. Cryptocurrencies usually use functions that are limited by the available processing power, the most common approach being that random numbers are appended to a block until its cryptographic hash meets a certain condition (e.g., some of its most-significant bits are equal to 0). The chain with the most cumulative PoW is accepted as the correct one, so that an attacker must control more than half of the active processing power on the network to perform a double-spend attack. This is unlikely to happen in practice if the processing power is large enough and is owned by non-colluding entities. Processing nodes that help to compute the hashes of new blocks are called miners, and are rewarded with a fraction of the cryptocurrency when a new block is accepted into the blockchain.

The first cryptocurrency, i.e., Bitcoin [2], was initially mined using desktop CPUs. Then, GPUs were used to significantly increase the hashing speed. Eventually, GPU mining was out-paced by FPGA miners, which were in turn surpassed by ASIC miners. Nowadays, the majority of the computing power on the Bitcoin network is found in large ASIC farms, each operated by a single entity, which makes the decentralized nature of Bitcoin debatable. To solve this issue, new PoW algorithms have been proposed that aim to be ASIC-resistant. ASIC resistance is achieved by using hashing algorithms that are highly serial, memory-intensive, and parameterizable so that a manufactured ASIC can easily be made obsolete by changing some of the parameters. Since the cost of manufacturing new ASICs whenever some parameters change is prohibitive, GPU mining of ASIC-resistant cryptocurrencies is generally much more low-risk and cost-effective. A prime example of an ASIC-resistant hashing algorithm is Lyra2REv2 (and its recently introduced Lyra2REv3 modification), which is used by Monacoin [4], Verge [5], Vertcoin [6], and some smaller cryptocurrencies. The chained structures of Lyra2REv2 and Lyra2REv3 are shown in Fig. 1 and Fig. 2, respectively. The BLAKE [7], Keccak [8], Skein [9], Blue Midnight Wish (BMW) [10], and CubeHash [11] hashing algorithms are well-known and have been studied heavily, both from theoretical and hardware-implementation perspectives (e.g., [12]–[15]), as they were all candidates in the SHA-3 competition. On the other hand, to the best of our knowledge, apart from our own previous work [1], no hardware implementation of the simplified Lyra2 and Lyra2MOD versions of Lyra2 [16], [17] as used in the Lyra2REv2 and Lyra2REv3 algorithms,
respectively, have been reported in the literature.

One potential issue with ASIC-resistant cryptocurrencies is that GPUs are generally much less energy efficient than ASICs, meaning that a massive adoption of ASIC-resistant cryptocurrencies would significantly increase the (already very high) energy consumption of cryptocurrency mining. FPGA-based miners, on the other hand, are flexible, energy efficient, and readily available to the general public at reasonable prices. Thus, provided that public and user-friendly FPGA-based miners become available, we believe that FPGAs are in fact an attractive platform for ASIC-resistant cryptocurrencies that should not be shunned by the community.

Contributions: This work presents the first FPGA implementation of the simplified Lyra2 hashing algorithm as used in Lyra2Rev2. Moreover, contrary to our previous work [1] which only contained an implementation of the Lyra2 core, in this work we describe an FPGA-based hardware implementation of a fully functional standalone Lyra2Rev2 miner on a Xilinx Multi-Processor System on Chip (MPSoC). While we do not provide explicit implementation results for Lyra2MOD or for a Lyra2Rev3 chain, which is currently only used by the (somewhat less popular) Vertcoin cryptocurrency, we explain in detail how the presented architecture can be modified correspondingly. We present post-layout results for a Xilinx MPSoC for the complete standalone Lyra2Rev2 miner as well as for the individual hashing cores. These results show that the proposed Lyra2Rev2 hardware architecture can achieve a hashing throughput of 31.25 MHash/s with an energy efficiency that is up to 4.3 times better than existing solutions at 0.80 µJ/Hash, while requiring approximately 85% of the programmable logic (PL) resources of the MPSoC.

Outline: The remainder of this paper is organized as follows. Section II provides the necessary background for the PoW concept and for the Lyra2 algorithm. Section III gives an in-depth explanation of the simplifications that Lyra2Rev2 and Lyra2Rev3 make to the generic Lyra2 algorithm. The hardware implementations of the simplified Lyra2 and Lyra2MOD algorithms are described at length in Section IV. Section V describes an MPSoC-based hardware architecture that implements the Lyra2Rev2 miner, which can be easily modified to also implement a Lyra2Rev3 miner. Implementation details and results for the standalone Lyra2Rev2 miner are provided in Section VI. Section VI also includes results for the individual hashing cores, notably including the proposed simplified Lyra2 core. Finally, Section VII concludes this paper.

II. BACKGROUND

This section provides the necessary background on the PoW concept, as well as some components of the Keccak and BLAKE2 hashing algorithms which are used in Lyra2.

A. Proof of Work

In order to explain the PoW concept in more detail, we use Bitcoin as an example [18], but it is important to note that many other Bitcoin-derived cryptocurrencies, such as MonaCoin and Vertcoin, use the same structure. Each block in the Bitcoin blockchain has an 80-byte (or 640-bit) header that contains information about the block, as shown in Table I. The version field dictates which version of the block validation rules needs to be followed. The previous block header hash and merkle root hash contain hashes of the headers of previous blocks to ensure that no previous transaction in the blockchain can be modified without also modifying the header of the current block. The time field contains the Unix epoch at which each miner started performing the PoW, which must be strictly greater than the median time of the previous 11 blocks. The nBits and nonce fields are the most relevant to the PoW. Specifically, nBits defines a 256-bit numerical value using an encoding explained in [18], while nonce can be chosen freely by the miner. The PoW that each miner performs amounts to finding a value for nonce so that a (chained) hash function of the header has a numerical value that is strictly smaller than the target threshold defined by nBits. Since hash functions possess the property of preimage resistance, i.e., they are not invertible, this can only be achieved by testing a very large number of nonce values until the target threshold is satisfied.

B. The Keccak Duplex

Keccak is a family of hashing algorithms based on a cryptographic sponge [20], [21]. A cryptographic sponge is a function that takes an arbitrary-length input to produce an arbitrary-length hashed output. Lyra2 uses a specific implementation of the sponge, called the duplex construction, which has a state that is preserved across different inputs. The duplex construction with naming conventions as adopted in Lyra2 is shown in Fig. 3. It consists of a permutation function $f$ that operates on a $w$-bit state vector, where $w = b + c$ and the parameters $b$ and $c$ are called the bitrate and the capacity of.
the sponge, respectively, as well as a padding rule pad. Note that the permutation $f$ is iterative and performs a pre-defined number of iterations, also called rounds.

A call to the duplex construction proceeds as follows. An input string $M$ is first fed into the duplex. Then, it is padded to length $b$ and XOR’d into the lower $b$ bits of the state. The state is then fed through the permutation $f$. The output of $f$ is the new state of the duplex, while its lower $l$ bits are the output hash, where $l \leq b$. If the duplex construction is considered as an object $H$, then the aforementioned procedure is referred to as a method $H\text{.duple}(M, l)$. The following two auxiliary methods are useful to simplify the notation: $H\text{.absorb}(M)$ updates the state using the input $M$ but discards the output (equivalent to $H\text{.duple}(M, 0)$), while $H\text{.squeeze}(l)$ reads $l$ output bits and then calls $H\text{.absorb}(\emptyset)$, where $\emptyset$ denotes an empty input string.

C. The BLAKE2b Round Function

BLAKE2 [22] is a family of hash functions designed for fast software implementations. It is the successor of BLAKE as submitted to the SHA-3 competition [23]. The Lyra2 algorithm heavily draws from the round function of BLAKE2b, the 64-bit variant of BLAKE2. The round function consists of an arrangement of blocks that apply a so-called G-function to a 16-word state, where one G-function operates on 4 different state words. For BLAKE2b a word has 64 bits meaning that 16 state words amount to 1024 bits. The total round transforms these 1024 bits using four G-blocks, rearranges the output, and then does a four G-block transformation again. Algorithm 1 describes the modified BLAKE2b G-function as used in Lyra2, where $x \gg y$ denotes a $y$-bit right rotation of $x$ and $\boxplus$ denotes a word-wise modulo-2$^m$ addition where the word width of both the operands and the result is $m$ bits.

III. The Simplified Lyra2 Algorithms Used in Lyra2REV2 and Lyra2REV3

Lyra2 was initially created as a password hashing scheme (PHS) for secure storage [16], [17]. Lyra2 uses the duplex construction from Keccak, where the permutation function $f$ is the round function from BLAKE2b. The reasoning for this choice is twofold and stems from the concept of favoring CPUs. On one hand, the G-function of BLAKE2b is software-oriented (e.g., the rotations are chosen to specifically benefit from SIMD instructions). On the other hand, the permutation of BLAKE2b has been shown to be secure even with a reduced number of rounds [24], whereas a full permutation normally consists of 12 rounds. As explained in more detail in the sequel, after every permutation, the Lyra2 algorithm performs a memory access. A reduced number of rounds in a permutation allows more memory accesses for the same execution time, making low-memory attacks on parallel platforms more costly. In the remainder of the text, calls to a full-round (i.e., 12 iterations) duplex are denoted as calls to $H$, while reduced-round duplexing as calls to $H\rho$, where $\rho$ denotes the reduced number of rounds. Because the G-functions are specified to operate on an array of 16 64-bit words, Lyra2 uses a duplex with a width of $w = 16 \cdot 64 = 1024$ bits. Pseudocode for the simplified version of Lyra2 that is used specifically in Lyra2REV2 is given in Algorithm 2 and can be compared to
the original Lyra2 pseudocode available in [16, Algorithm 2]. In the following sections, we first explain each phase of the simplified Lyra2 algorithm used in Lyra2REv2 and how it differs from the reference implementation of Lyra2 in detail. Then, we explain the differences between Lyra2 used Lyra2REv2 and Lyra2MOD used in the updated Lyra2REv3 algorithm.

A. Bootstrapping Phase

In the bootstrapping phase, the duplex is initialized with a state that depends on the input \(pwd\), a salt (which in Lyra2REv2 is set to be equal to \(pwd\) for simplicity), and the parameters \(T\), \(R\), and \(C\) by using a full-round absorb. The duplex \(H\) in Algorithm 2 internally uses a bitrate \(b = 768\) bits and a capacity \(c = 256\) bits. The \(H.absorb(\cdot)\) call on line 5, however, considers only inputs of 512 bits instead of \(b\) bits, so as to not overwrite the upper part of the initialization state, i.e., the 512-bit initialization value \(IV\) specified by BLAKE2b. This results in two full-round absorbs, where the first and second absorbs process \((pwd||pwd)\) and \(pad(params)\), respectively.

B. Setup Phase

During the setup phase of Lyra2, an \(R \times C \times b\) memory matrix \(M\) is initialized using the single-round duplex \(H_1\). The simplified version of Lyra2 in Lyra2REv2 uses \(R = C = 4\). Rows are initialized from first to last, while columns within each row are initialized from last to first. From the second row onward, a previous row is re-read, making it impractical to only store parts of the memory matrix. Also, from the third row onward, in addition to the previous row, i.e., \(prev^0\), a specific pre-initialized row, i.e., \(row^1\), is revisited (i.e., read and updated) in a deterministic manner. Rows are re-read or revisited from the first to the last column. Revisited rows use a rotated version of the duplex output, where the rotation number is chosen as \(\omega = 64\) in Lyra2REv2. Note that the general revisiting scheme for \(row^1\) is significantly more complicated when \(R > 4\), as rows to be revisited can be chosen from within a specific window.

C. Wandering Phase

The wandering phase is configurable to be the most time-consuming of the four phases. This is done through a timecost parameter \(T\), that sets a number of rows \(2R \cdot T\) to be revisited. In Lyra2REv2, there is only a single iteration over the memory matrix, as \(T = 1\). Specifically, it revisits two rows \(row^0\) and \(row^1\), where \(row^0\) is chosen deterministically but \(row^1\) is chosen in a pseudorandom fashion by using the least significant part of the duplex output. Note that the pseudorandom and deterministic row can collide, resulting in the operations on lines 26 and 27 to sequentially read from and then write to the same matrix cell. Also note that the reference implementation of Lyra2 selects not only \(row^1\), but also \(row^0\) pseudorandomly. Furthermore, whereas the simplified Lyra2 in Lyra2REv2 uses a deterministic column counter \(col\), the reference implementation features pseudorandom counters \(col^0\) and \(col^1\). Lastly, similar to \(prev^0\) as the previous \(row^0\), \(prev^1\) is introduced to track the previous \(row^1\). These extra variables appear, for example, on line 25, where the simplified Lyra2 has a two-operand word-wise addition, but the reference implementation would pass \(M[row^0][col] \oplus M[row^1][col] \oplus M[prev^0][col^0] \oplus M[prev^1][col^1]\) as input to the sponge.

D. Wrap-up Phase

The wrap-up phase consists of a full-round absorb of a specific cell of \(M\) followed by a squeeze of the hashed output \(K\). This specific cell is likewise pseudorandom, as it is selected as the first cell of the last revisited pseudorandom row. The requested squeeze length \(k = 256\) is lower than the bitrate \(b = 768\), which means that the final output is provided directly from the duplex state without a permutation \(f\).

E. From Lyra2REv2 to Lyra2REv3

Recently, the developers of Lyra2REv2 proposed Lyra2REv3 with the goal to make ASIC miners for Lyra2REv2, that became available on the market, obsolete. Vertcoin is currently the only Lyra2REv2-based cryptocurrency that has performed a hard fork to force the miners to use Lyra2REv3 [25]. Fig. 2 illustrates the new chained hashing algorithm. Compared to the Lyra2REv2 chain in Fig. 1, it can be seen that the Keccak-256 and Skein-256 hashing algorithms were removed from the chain, and a second instance of a Lyra2-based hashing algorithm was added. The developers justified the removal of both Keccak-256 and Skein-256 by mentioning the existence of significantly more efficient hardware implementations of these algorithms compared to their software counterparts. In addition to these changes, the simplified Lyra2 algorithm itself has been modified.

The updated Lyra2 algorithm as used in Lyra2REv3, called Lyra2MOD, is illustrated in Algorithm 3, where the changes from the simplified Lyra2 algorithm used in Lyra2REv2 are highlighted in blue (lines 4, and 24–26). While the changes appear to be minor, the Lyra2MOD modifications are non-conventional in the Lyra2 scheme. Lyra2MOD introduces a new variable called \(instance\), that can take the value of the four least-significant bits of any word in the \((b+c)\)-bit sponge state. This assignment is non-conventional, because it does not exclude the four words that make up the sponge capacity \(c\). Within its specifications, the sponge construction does not allow for such an operation that directly reads bits from the capacity part of the sponge [20]. The variable \(instance\) is then used to update \(row^1\), which can now similarly be assigned some least significant part of any state word. The assignments to \(instance\) and \(row^1\) require defining a new operation on the sponge \(H\) that requests the current state without performing any rounds. We call this new operation \(squeeze\) for its similarity with the \(squeeze\) operation, with the difference that the former is not restricted to requests of \(l \leq b\) bits on the state. To omit the round functionality of the sponge, we call \(squeeze\) on \(H_0\), i.e., the sponge reduced to zero rounds. The intended effect of these changes is to further serialize the algorithm, making hardware implementation more challenging. The impact of these changes on resource requirements and on performance is briefly described in Section IV-D.
Algorithm 3 Lyra2MOD algorithm as specified in Lyra2REv3.

```plaintext
1: PARAMS: H, ρ, ω, T, R, C, k, b as H, b, c as H, c
2: INPUT: pwd
3: OUTPUT: K

▷ Bootstrapping Phase
4: instance ← 0
5: params ← len(K) || len(pwd) || len(pwd) || T || R || C
6: H.absorb(pwd || pwd || params)

▷ Setup Phase
7: for col ← 0 to C - 1 do
8: M[0][C - 1 - col] ← Hρ.squeeze(b)
9: end for
10: for col ← 0 to C - 1 do
11: M[1][C - 1 - col] ← M[0][col] ⊕ Hρ.duplex(M[0][col], b)
12: end for
13: for row0 ← 2 to R - 1 do
14: prev0 ← row0 - 1
15: row1 ← row0 - 2
16: for col ← 0 to C - 1 do
17: rand ← Hρ.duplex(M[row1][col] ⊕ M[prev0][col], b)
18: M[row0][col] ← M[row0][col] ⊕ rand
19: M[row1][col] ← M[row1][col] ⊕ (rand ⊕ ω)
20: end for
21: end for

▷ Wandering Phase
22: for row0 ← 0 to R · T - 1 do
23: prev0 ← row0 - 1
24: rand ← Hρ.squeeze(b + c)
25: instance ← rand’[instance] mod 16
26: row1 ← rand[instance] mod R
27: for col ← 0 to C - 1 do
28: rand ← Hρ.duplex(M[row1][col] ⊕ M[prev0][col], b)
29: M[row0][col] ← M[row0][col] ⊕ rand
30: M[row1][col] ← M[row1][col] ⊕ (rand ⊕ ω)
31: end for
32: end for

▷ Wrap-up Phase
33: H.absorb(M[row1][0])
34: K ← H.squeeze(k)
```

IV. PROGRAMMABLE LOGIC IMPLEMENTATION OF SIMPLIFIED LYRA2

This section describes how the Lyra2 algorithm, which is the most complex algorithm of the Lyra2REv2 chain, can be efficiently mapped to a hardware implementation. The hardware implementation of the full Lyra2REv2 hashing chain is discussed in Section V, as well as the changes that would be required for a Lyra2REv3 chain. Similarly to the previous section, we first describe an implementation of Lyra2 for Lyra2REv2, and we then explain the necessary changes to implement Lyra2MOD for Lyra2REv3.

Recall that, in the current instance of Lyra2 as used in Lyra2REv2, the timecost parameter is \( T = 1 \), the number of rows in the memory matrix is \( R = 4 \), the number of columns in the memory matrix is \( C = 4 \), and the desired hashing output length is \( k = 256 \) (note that the same parameter values are also used for Lyra2MOD in Lyra2REv3). The architecture described in this work is optimized for these parameter values, but can be modified relatively easily to accommodate potential changes in the aforementioned parameters. Moreover, for \( R = C = 4 \) and \( b = 768 \), the memory matrix \( M \) is 1.5 kB in size, which is clearly not prohibitively large to be implemented either in PL or on an ASIC. The claimed ASIC-resistance of the Lyra2REv2 algorithm comes from the fact that \( T, C, \) and \( k \) can be increased easily if necessary and that the chain of hashing algorithms itself can be modified (as is the case with the newer Lyra2REv3 algorithm).

The high-level datapath of the proposed PL implementation of the simplified Lyra2 algorithm used in Lyra2REv2 is shown in Fig. 4, where the duplex construction with its state, round, and XOR input block can be clearly distinguished. The memory matrix \( M \) is mapped to a block RAM (BRAM). To reduce the complexity of the multiplexer (MUX) at the input of the duplex, the BRAM also contains constant vectors of \( b \) bits used during the bootstrapping and setup phases, i.e., an all-zero vector and the \( pad(params) \) vector.

As mentioned in Sections II-C and III, the round function \( f \) of the Lyra2 algorithm is an arrangement of BLAKE G-functions. Fig. 5 shows the hardware architecture of BLAKE’s G-function, where all signals are 64 bits wide. Lyra2 uses the BLAKE2b variation, i.e., \( m = 64, R_1 = 32, R_2 = 24, R_3 = 16, \) and \( R_4 = 63 \) (cf. Algorithm 1). Furthermore, the CM21 and CM21+1 inputs are not used, thus the corresponding adders are omitted in the implementation of the round function for Lyra2 presented in this work.

In the following, we first describe a version of the hardware architecture of the simplified Lyra2 core described in this work, where each round of the \( f \) function is executed in a single clock cycle (CC). We then describe how this basic architecture can be improved through pipelining.

A. Basic Iterative Architecture

The basic iterative Lyra2 architecture requires 68 CCS per hash: 24 for the bootstrapping phase, 16 each for the setup and wandering phases, and 12 for the wrap-up phase.

1) Bootstrapping Phase: During the bootstrapping phase, the duplex processes two 512-bit input blocks from \( pad(pwd || pwd || params) \) using a full-round absorb. In Lyra2REv2, \( pwd = cube_{out} \), with \( cube_{out} \) being the output of the first CubeHash instance, i.e., the previous algorithm in the
chain. Thus, as shown in Fig. 4, the \((pwd||pwd)\) vector is one of the inputs to the MUX of the duplex. On the other hand, the \(\text{pad}(\text{params})\) vector is fed into the sponge by loading it on \(q_a\) while simultaneously loading the all-zero vector on \(q_b\). Both constants are stored at known addresses in the BRAM, and are absorbed in a separate 12-round bootstrap state. During bootstrapping, the duplex only receives an input vector in the first round. Hence, for subsequent rounds, \(q_a\) and \(q_b\) output the all-zero vector, and their sum is passed to the duplex via its input MUX.

2) Setup Phase: The setup phase is split into three distinct phases for convenience, namely Setup0, Setup1, and Setup2, which correspond to Lines 6–8, Lines 9–11, and Lines 12–20 of Algorithm 2, respectively. Similarly to the bootstrapping phase, the setup phase uses the all-zero vector stored in the BRAM. In the Setup0 state, the squeezes input an empty message into the duplex and directly write the duplex output to the BRAM. To achieve that, the all-zero vector is output on \(q_a\), \(q_b\), and \(q_c\). Setup1 reads the all-zero vector on \(q_b\), but a specific vector from the BRAM on \(q_a\). Setup2 reads two vectors from \(q_a\) and \(q_b\). Both the duplex output and the rotated duplex output are XOR'd with two other vectors from the BRAM, requiring the two XOR blocks in parallel as illustrated in Fig. 4. On the control path, counters keep track of the various rows \((\text{row}^0, \text{row}^1, \text{prev}^1)\) and their corresponding columns to generate read and write addresses for the RAM.

3) Wandering Phase: The input to the duplex in the wandering phase is always the word-wise addition of two RAM cells. Both XOR blocks connected to the duplex output are used. As mentioned in the algorithmic description of the wandering phase in Section III-C, the pseudorandom and deterministic rows used in this phase can collide. In hardware, this special case requires the output of one XOR block to be input to the other, while the write port of the first XOR block needs to be disabled to prevent write collisions on the RAM.

4) Wrap-Up Phase: During the wrap-up phase, one RAM cell is input into the sponge and then processed using a full-round absorb. For the following squeeze, the requested hashed-output length \(k\) is lower than the bitrate \(b\), i.e., the duplex state directly provides the output hash.

B. Memory Matrix

In the wandering phase, up to two RAM cells need to be written and three RAM cells need to be read per CC. These operations cannot be spread over multiple CCs without negatively affecting the overall throughput of the design. Therefore, we use standard true-dual-port BRAMs along with multipumping and replication techniques [26] in order to implement the required functionality. Replication provides extra read ports by physically replicating the BRAM while connecting the write ports to keep the two copies coherent. Multipumping operates the BRAM at double the clock frequency of the surrounding logic, which, together with replication, effectively provides four read ports and two write ports. A \(b = 768\)-bit wide BRAM with true-dual-port functionality can be implemented using \(21 \times 36K\) and one \(18K\) PL BRAM primitives, which are \(21 \times 36\) and 18 bits wide, respectively. In total, the Lyra2 core then uses \(42 \times 36K + 2 \times 18K = 1548\) Kbits of BRAM.

C. Pipelined Architecture

Pipelining the BLAKE2b round function can greatly reduce the delay of the critical path. Recall that the round function consists of an arrangement of G-functions, whose architecture is illustrated in Fig. 5. In the basic iterative version described above, the critical path extends from the RAM read ports to the RAM write ports and contains eight sequential 64-bit adders in the round function. Dividing these sequential adders into eight pipeline stages greatly increases the achievable clock frequency, with only a minimal increase to resource usage due to the additional registers required. Each hash that is concurrently being processed in the pipeline needs its own memory. However, extra RAM-based memory is readily available since the current Lyra2REv2 parameters result in a RAM depth much shallower than that of the PL BRAMs. With adequate scheduling, concurrent hashes write to the same BRAMs in distinct CCs. While read ports \(q_a\) and \(q_c\) feed the duplex, \(q_c\) and \(q_d\) feed the XORs with duplex outputs. When pipelining the round function, \(q_c\) and \(q_d\) therefore need to be delayed by as many CCs as there are pipeline stages. The extra read port that is unused in the basic architecture allows delaying the control path for \(q_d\) rather than using a delayed version of \(q_a\), avoiding a long chain of 768-bit registers. Eight pipeline stages in the round increase the latency to 544 CCs per hash. On the other hand, the pipeline can process eight hashes concurrently, i.e., one hash is output every 68 CCs on average. Finally, the logic depth reduction, from eight sequential 64-bit adders to a single one, more than doubles the achievable clock frequency, which in turn significantly increases the overall hashing throughput of the pipelined architecture.

D. Programmable Logic Implementation of Lyra2MOD

A PL implementation of the Lyra2MOD algorithm can be based on the pipelined architecture of the simplified Lyra2 algorithm as described in Section IV-C, with appropriate changes to support the modified wandering phase explained in Section III-E. Fig. 6 shows the hardware implementation of the row selection during the wandering phase for both the simplified Lyra2 (Lyra2REv2) and Lyra2MOD (Lyra2REv3) algorithms. Specifically, Fig. 6(a) shows that in the simplified Lyra2 algorithm, the row is selected simply based on the 2 least-significant bits of the state (cf. line 23 of Algorithm 2). On the other hand, the row selection in Lyra2MOD is much
more involved (cf. lines 24–26 of Algorithm 2). Thus, as shown in Fig. 6(b), Lyra2MOD requires the addition of multiplexers and memory to store the new instance variable. The instance-variable memory is initialized to all zeros during the bootstrap phase. Finally, note that in the 8-stage pipelined architecture, instance and row\(^1\) need to be stored for every hash in the pipeline using small \(8 \times 4\) bits and \(8 \times 2\) bits RAMs, respectively. After implementation, verification, and synthesis of Lyra2MOD, it was found that the changes introduced have negligible impact in terms of resources. Furthermore, the critical path is unaffected as the new row-selection logic in Lyra2MOD translates to significantly fewer logic levels than that of the 64-bit adders on the datapath.

V. MPSOC IMPLEMENTATION OF A STANDALONE LYRA2REV2 MINER

In this section, we present an MPSoc-based architecture for the standalone Lyra2Rev2 miner, and the changes that would be required to support the Lyra2Rev3 chain. Specifically, we implement the computation-intensive part of the Lyra2Rev2 (or Lyra2Rev3) chained hashing algorithm on the PL along with supporting logic, and use the processing system (PS) capabilities of the MPSoc to run supporting software that is used to handle high-level cryptocurrency protocol tasks.

Fig. 7 shows the high-level architecture of the proposed standalone Lyra2Rev2 miner, where the supporting software on the PS side (left) provides the PL side (right) of the miner with the required data to start the search for a nonce that leads to a hash that meets the target threshold. In case of success, the supporting software reads back the winning nonce from the register file, regenerates the winning hash, and communicates the results to the network through the high-level cryptocurrency protocol.

In the following, the miner is described in more details. We first briefly describe the communication mechanism between the PS and the PL sides of the MPSoc. Then, we discuss the software on the PS. The next two sections describe the control logic, including nonce generation and threshold verification. Lastly, we discuss the hardware implementation of the mining algorithm on the PL side of the device including the hashing algorithms, other than simplified Lyra2 and Lyra2MOD that we have already described above.

A. Communications Between the Processing System and the Programmable Logic

Given the limited amount of data that transits between the PL and the PS, a flip-flop based register file is used. Table II shows the content of the register file and Fig. 8 provides a detailed view of the status and control registers. This allows the verification software to easily write 640-bit block headers, 256-bit target thresholds, and maximum nonces to the hardware miner, and to read back 32-bit nonces, while reading and writing status and control signals. As shown in Fig. 7, the register file is wrapped in an adapter to allow access through a memory-mapped 32-bit wide AXI4-Lite bus, which is clocked at 250 MHz.

B. Software on the Processing System

The verification software consists of a Linux driver and a userspace application running inside a custom embedded GNU/Linux distribution. The driver exposes the memory-mapped register file as an mmap() capable character device. Userspace applications can then use the character device to write block headers and interact with the PL side of the miner.

The userspace application is based on the existing cpuminer-multi [27] open-source mining software, which was enhanced by adding a new type of algorithm, namely lyra2rev-hw. This new algorithm communicates directly with the mining hardware on the PL side using the character device mentioned above. It writes the block header—which includes the starting nonce value—, the target threshold, and a maximum nonce value into the register file. Then, it asserts a bit in the control register to signal that new block data is available and starts to poll bits in the status register until either the winning-nonce-found bit is set or until the nonce-not-found bit is set. In the first case, the winning nonce is read back from the register file, the winning hash is regenerated and the results are communicated back to the network through the high-level cryptocurrency protocol. In the second case, the software proceeds with the next block header.

To ensure reliable and reproducible software builds, the Linux-based firmware and boot image are created using a

![Table II](image-url)

| Addr   | Register  |
|--------|-----------|
| 0x00   | Status    |
| 0x04   | Control   |
| 0x08   | Winning Nonce |
| 0x0C   | Target    |
| 0x28   | Threshold |
| 0x2C   | Block     |
| 0x78   | Header    |
| 0x7C   | Maximum Nonce |

Fig. 6. Hardware implementation of the row selection during the wandering phase for (a) the simplified Lyra2 and (b) Lyra2MOD. Clock signals are omitted for clarity.
The threshold-verification logic signals the output control FSM that the winning nonce was found. The output control FSM then reads the corresponding winning nonce from the metadata FIFO, asserts the winning-nonce-found bit in the status register, and writes the winning nonce to the register file. However, if the corresponding nonce read from the metadata FIFO does not produce a hash that meets the threshold and that nonce corresponds to the maximum value, this implies that the search is over. In that case, the output control FSM asserts the nonce-not-found bit in the status register.

### E. Chained Hashing Algorithm in Programmable Logic

Fig. 9 illustrates the hardware implementation of the Lyra2REv2 chained hashing algorithm, where each hash function has its dedicated scheduler, and is bounded by FIFOs. The number of instances of each hash function varies, as it is chosen depending on their respective maximum clock frequency and throughput in hashes per second with the goal to balance the processing pipeline. More details are provided in Section VI, but the number of instances per hashing algorithm is selected in order to maximize the overall mining algorithm throughput. This section provides details about the PL implementation of the Lyra2REv2 hashing chain.

Reference implementations for the SHA-3 candidates that are optimized for various performance metrics are publicly available. In particular, a research team at the George Mason University (GMU) described a methodology to compare the hardware performance of fourteen round-two candidates, including all of those utilized in Lyra2REv2 [15], and they also provide the source code for their implementations [29]. We used the GMU throughput-per-area-optimized designs as starting points for some of the implementations of these hashing cores used in this work.

The Lyra2REv2 chain passes only 256-bit inputs between the algorithms in the chain, while all of the SHA-3 candidates were required to support arbitrary input lengths. Generally, this results in some functionality that does not appear and allows for heavy optimizations. Also, the implementations from GMU include interfaces to communicate with software, accounting for such things as endianness and serialization at the output, which are not required for the custom mining chain. As such,
we only re-used some main computational blocks of the GMU implementations and always customized the control path. This greatly simplifies the control flow for these algorithms and could often also introduce optimizations for the computational datapath. More details are provided for individual hashing cores in the following.

1) FIFOs: The hashing cores have different nominal frequencies and throughputs. Firstly, FIFOs are used to normalize data transfers between hashing cores with different throughput, by properly asserting the forward- and back-pressure signals. Secondly, since the hashing cores also have various operating frequencies, asynchronous FIFOs are used to safely transfer data from one clock domain to another. The forward and back-pressure signals are individually set to match the internal pipelined architecture of each hashing core.

2) Schedulers: While the FIFOs are necessary to interface hashing algorithms operating at different frequencies, data schedulers—one per hashing step in the chain—are needed to balance throughput between cores with varying execution times. For example, an upstream hashing core producing an output hash every 192 CCs will inherently starve a downstream core that can accept new data every 68 CCs. To address this limitation, in this example the upstream core would be replicated 3 times and the read/write operation of each core would be scheduled to produce a hash every 64 CCs.

The scheduler consists of a state machine that monitors the upstream and downstream FIFO back-pressure signals and that tracks each hashing core computation. Schedulers have knowledge of the execution time and pipeline depth of the hashing cores they are associated to. Given this information, the scheduler will assert the ready signal of the next available core, in a round-robin fashion, when the upstream FIFO has enough data to sustain the hashing core internal pipeline and the downstream FIFO has enough space to receive new data. Subsequently, when a core finishes its computations, the resulting hash is written to the downstream FIFO.

3) BLAKE: Like the round function in the sponge of Lyra2 which is based on BLAKE2b, the round function of BLAKE is given by an arrangement of G-functions. The G-functions themselves differ from the one of Algorithm 1, with different constants for the rotations and with the insertion of additional adders. We adapted the BLAKE2b round implementation for Lyra2 to implement the BLAKE algorithm.

Consider Fig. 5, which shows the hardware architecture of BLAKE’s G-function that updates 4 out of 16 state words, with all signals being m bits wide. In the Lyra2REv2 and Lyra2REv3 algorithms, the BLAKE hash function is for m = 32 bits, and uses the constants $R_1 = 16$, $R_2 = 12$, $R_3 = 8$, and $R_4 = 7$. The inputs $CM_{2i}$ and $CM_{2i+1}$ take the value of a round-dependent permutation of a message block $M_n$ and constant $C_o$. Notably, these inputs are excluded when the G-function is implemented together with the sponge, because an interface to inject message blocks into the state is already present in the functions $H_{absorb}$ and $H_{duplex}$.

BLAKE hashes a 512-bit message in 14 rounds. In our architecture, which is optimized for high throughput per area, the rounds are fully unrolled and form 14 pipeline stages. The round-dependent permutation can then be designed using only routing resources, rather than requiring a complex block that must be able to output each of the 14 permutations based on a round counter. Furthermore, analogous to Lyra2, the sequential adders within the round are divided into pipeline stages to allow for a higher operating clock frequency of the core. Since the 32-bit adders of BLAKE feature shorter carry chains than the 64-bit adders of Lyra2, only four pipeline stages are implemented within a BLAKE round. In total, the BLAKE architecture forms a 56-stage pipeline that concurrently processes 56 different message blocks. Contrary to the other cores in the Lyra2REv2 chain that pass 256-bit values, the BLAKE core, at the head of the chain, takes 640-bit block headers as input. Each block header is therefore split into two message blocks, and the BLAKE implementation can then, on average, output one hash every 2 CCs.

4) Keccak: Keccak, which introduced the concept of a sponge, is very efficiently implementable in hardware, which is one of the main reasons it won the SHA-3 competition. While Lyra2 uses a sponge with the BLAKE2b round function, Keccak defines its own family of round functions called $Keccak-f\{w\}$, with $w$ being one of seven values for the sponge permutation width. Lyra2REv2 uses an instance of $Keccak-f\{1600\}$, with $b + c = 1088 + 512$, the permutation applied in 24 rounds and $l = 256$ bits of output hash length. We use a custom sponge implementation with its corresponding control logic, along with the $Keccak-f$ round function from GMU. Executing one round per clock cycle, the Keccak implementation can then output one hash every 24 CCs.

5) CubeHash: Each CubeHash round is simple, but it is applied many times. CubeHash in Lyra2REv2 does 16 initialization rounds and a total of 176 finalization rounds. Each round takes a single CC so that a total of 192 CCs are required to compute one hash. The difference between initialization and finalization rounds amounts to flipping a
single bit of the state and is trivial to implement in hardware. We re-use the CubeHash round function from GMU, and implement round-serial control logic to output one hash every 192 CCs.

6) Skein: Skein is based on the Threefish tweakable block cipher [9], and uses the unique block iteration (UBI) chaining mode for hashing, as illustrated in Fig. 10. For the Lyra2REv2 algorithm, all inputs of the first UBI block are constant, hence it can be pre-computed as an initialization value. In normal operation of Skein, for an arbitrary length input message, there is an iterative implementation of the UBI block, where the last round is slightly different as it inputs the constant zero instead of a message. However, for Skein as used in Lyra2REv2, there is an equal number of hashing rounds (taking message inputs) and finalization rounds (taking zero-inputs). It is useful to unroll and pipeline the remaining two UBI blocks. With one of its input as a constant, a significant portion of the logic in the UBI block that corresponds to the finalization round can be removed. Furthermore, when using two distinct UBI blocks, the key schedule of the first block is independent of the message input, and it can be pre-computed and stored in a read-only memory. Within each UBI block, Skein transforms the input using 72 Threefish rounds. Every 8 rounds have a similar structure, and they are implemented as a single pipelined block, which is applied 9 consecutive times. Finally, the above Skein implementation can output, on average, one hash every 9 CCs.

7) Blue Midnight Wish: The implementation of BMW is derived from that of GMU, where the control logic has been completely replaced. BMW in Lyra2REv2 takes a 256-bit input and only has a single hash round followed by a finalization round for this input length. Because BMW implements fewer rounds, the round function itself is inherently more complex. For example, one of the functions in the round, $f_1$, implements 16 sequential 32-bit adders that each take 17 addition operands. To improve on the achievable clock frequency of the GMU design, the round is implemented as 18 pipelined stages. Each message passes once through the pipeline for the hash round and once for the finalization round, such that, on average, the BMW implementation outputs one hash at every 2 CC.

F. MPSoC Implementation of Lyra2REv3

A potential MPSoC implementation of a Lyra2REv3 miner would be very similar to that of the Lyra2REv2 miner described previously. The required modifications consist of the removal of the Keccak-256 and Skein-256 blocks, the replacement of the simplified Lyra2 core with the new Lyra2MOD block described in Section IV-D, and the re-arrangement of the hashing chain as shown in Fig. 2. On the PS side, the verification software would need to be modified to use Lyra2REv3, which is also supported by cpuminer-multi.

VI. IMPLEMENTATION RESULTS

In this section, we provide implementation results for a full standalone Lyra2REv2 miner, notably using the simplified Lyra2 core described in this work. To the best of our knowledge, there are no other FPGA-based implementations of simplified Lyra2 cores or for Lyra2REv2 miners in the open literature. For this reason, we can unfortunately not provide detailed comparative FPGA/MPSoC implementation results, but we provide a comparison with a GPU and a commercially available FPGA-based Lyra2REv2 miner.

A. Lyra2REv2 Miner

The Lyra2REv2 miner was implemented on a Xilinx ZCU102 Evaluation Kit, which is based on the Xilinx Zynq UltraScale+ 9EG (ZU9EG) MPSoC. The PL of the ZU9EG MPSoC contains a total of 34,260 configurable logic blocks (CLBs) with 274,080 look-up tables (LUTs), 548,160 registers, and 32.1 Mbits of BRAM. The PS of the ZU9EG MPSoC contains four ARM Cortex-A53 cores clocked at 1.2 GHz. The functionality of the Lyra2REv2 chain was verified against test vectors generated using cpuminer-multi.

The power-consumption estimation was obtained using Xilinx’s Vivado Power Estimator tool, where the timing constraints are those required for the operating frequencies of Table IV, the switching activity is obtained by way of simulation [30] with the miner processing input vectors generated using cpuminer-multi [27], and the post-fitted design provided to the tool meets all timing constraints.

Table III shows the throughput metrics for the individual hashing cores. Due to the different hashing core architectures, we use a total of 5 clock domains, namely, 100 MHz for the BLAKE and BMW cores, 375 MHz for Skein and Keccak, 250 MHz for CubeHash, and 225 MHz and 450 MHz for Lyra2 and its multi-pumped RAM blocks, respectively. Clock-domain crossings are done over the asynchronous FIFOs. From Table III, it can be observed that both the execution time and the resulting individual throughput vary significantly among the hashing cores, thus making it challenging to perfectly balance the Lyra2REv2 chain. The bottom half of Table III provides the number of cores per hashing step that are used in the Lyra2REv2 chain, which result in a relatively balanced pipeline that is limited by the 31.25 MHash/s combined throughput of the Keccak and CubeHash cores. It should be noted that there is a total of 48 instances of the CubeHash core as there are two CubeHash steps in the chain (cf. Fig. 9).

Table IV shows the post-fitting area results of the proposed Lyra2REv2 miner. Specifically, the table shows the average

\[1\] We note that the VHDL code and relevant scripts for the simplified Lyra2 core are publicly available at https://github.com/Michielvb/lyra2-hw.
TABLE III
THROUGHPUT METRICS FOR THE INDIVIDUAL HASHING CORES FOR THE XILINX ZYNQ ULTRASCALE+ MPSoC 9EG.

| Metrics          | BLAKE | Keccak | CubeHash | Lyra2 | Skein | BMW |
|------------------|-------|--------|----------|-------|-------|-----|
| Frequency (MHz)  | 100   | 375    | 250      | 225   | 375   | 100 |
| Exec. time (CCs/Hash) | 2     | 24     | 192      | 68    | 9     | 2   |
| T/P (MHz/Hash/s) | 50.00 | 15.63  | 1.30     | 3.31  | 41.67 | 50.00 |

Combined

| # Cores/Step | 1 | 2 | 24 | 10 | 1 | 1 |
|-------------|---|---|----|----|---|---|
| T/P (MHz/Hash/s) | 50.00 | 31.25 | 31.25 | 33.01 | 41.67 | 50.00 |

TABLE IV
POST-FITTING AREA RESULTS OF THE STANDALONE LYRA2REv2 MINER FOR THE XILINX ZYNQ ULTRASCALE+ MPSoC 9EG. THE AVERAGE INDIVIDUAL RESULTS FOR EACH HASHING CORE ARE PROVIDED AND THE TOTAL FOR ALL COMBINED INSTANCES OF A CORE IS GIVEN IN PARENTHESES.

| Resources          | BLAKE | Keccak | CubeHash | Lyra2 | Skein | BMW |
|--------------------|-------|--------|----------|-------|-------|-----|
| Area (CLBs)        | 4417  | 436    | 254      | 12176 | 2062  | 2073 |
| LUTs               | 25229 | 2924   | 1762     | 84553 | 6138  | 12973 |
| Registers          | 37213 | 2013   | 1319     | 63302 | 8321  | 13579 |
| RAM (kbits)        | 0     | 0      | 0        | 0     | 0     | 0    |

| | Total |
|---|-------|
| Area (CLBs) | 4417 (4417) |
| LUTs | 25229 (25229) |
| Registers | 37213 (37213) |
| RAM (kbits) | 0 (0) |

TABLE V
COMPARISON WITH A GPU IMPLEMENTATION AND A COMMERCIALLY AVAILABLE FPGA MINER.

| Implementation | NVIDIA Titan Xp | Hash Altcoin BlackMiner F1+ | Xilinx Zynq UltraScale+ 9EG |
|----------------|-----------------|-------------------------------|-------------------------------|
| T/P (MHz/Hash/s) | 63.09 | 324 | 31.25 |
| Power (W)       | 215   | 543  | 25   |
| En.-Eff. (µJ/Hash) | 3.41 | 1.68 | 0.80 |

individual area results for each hashing core and the total amount for all combined instances of a core in parenthesis. The “Others” column shows the resource utilization of all blocks except the Lyra2REv2 chain on the PL side of Fig. 7. Finally, the “Total” column is the total resource utilization for the complete miner. The total CLB count is less than the sum of the individual CLBs because some CLBs are shared across components. We observe that the 48 CubeHash instances require the most PL CLB and LUT resources, followed closely by the 10 Lyra2 instances. Especially Keccak, on the other hand, is much more hardware efficient.

Table V shows the post-fitting power consumption results of the proposed standalone Lyra2REv2 miner. The Lyra2REv2 miner consumes 24.93 W, which leads to an energy efficiency of 0.80 µJ/Hash at a throughput of 31.25 MHash/s.

B. Comparison with a GPU and a Commercial FPGA Miner

Table V shows a performance comparison of the work described in this paper against a Lyra2REv2 miner running on a (non-overlocked) NVIDIA Titan Xp GPU and on the Hash Altcoin BlackMiner F1+ commercial multi-FPGA miner [31], which features 18 parallel Xilinx Kintex 7 (XC7K325T) FPGAs. The power consumption of the BlackMiner F1+ has been measured and found to be 543 W when mining a Lyra2REv2-based cryptocurrency [32]. For the GPU, we use version 390.48 of the NVIDIA drivers for Linux and version 2.3.1 of the ccminer software [33] compiled from scratch with version 9.1.85 of the CUDA compilation tools. The ccminer intensity option was set to 22 (out of 25), which is the largest supported value before the GPU memory runs out. All remaining parameters of the NVIDIA drivers and of the ccminer tool have their default values. We set ccminer up to mine MonaCoin using Lyra2REv2 on the zergpool.com mining pool.2 The power and hash rates reported in Table V are average values that are provided directly by the ccminer software.

We observe that the proposed FPGA-based Lyra2REv2 miner is estimated to be 4.3 times more energy efficient than the GPU-based miner. Moreover, the FPGA-based Lyra2REv2 miner is also estimated to be 2.1 times more energy efficient than the BlackMiner F1+. Also note that the BlackMiner F1+ is a multi-FPGA miner and that our FPGA-based Lyra2REv2 miner achieves a 1.74 times higher throughput than the average throughput per FPGA of the BlackMiner F1+. However, due to a lack of details on the implementation of the BlackMiner F1+, it is difficult to assess whether the improved energy efficiency and throughput are due to a better implementation of the various hashing cores or simply due to a difference in the employed FPGAs. It should also be noted that the BlackMiner F1+ and our FPGA-based Lyra2REv2 miner are standalone devices, while the power we report for the GPU-based miner does not include the computer required to host the GPU.

VII. Conclusion

This paper, we presented the first FPGA-based implementation of a standalone miner for Lyra2REv2, which is an ASIC-resistant hashing algorithm employed by several cryptocurrencies. To this end, we also presented the first implementation of the simplified Lyra2 hashing algorithm used by Lyra2REv2 in the open literature. The key to achieve a good throughput and energy efficiency for Lyra2 is to efficiently map the memory matrix to programmable logic (PL) RAM blocks and to pipeline the BLAKE2b round function. With regard

2Note that all mining rewards obtained during testing were directly sent to Vertcoin to the Tip Jar wallet of the Vertcoin Developers (VnFHNCy5Aq7v7zq5W9UK9wfdOL7mRPWZK), who are also the developers of Lyra2REv2 and Lyra2REv3.
to the whole miner, there are two key ingredients. The first one is to minimize communications between software and hardware by implementing nonce generation and threshold verification in hardware. The second one is to optimize the throughput per area of each core in the chain while at the same time finding a good balance between the links, under the constraint of the total amount of resources available. As a result, the proposed Lyra2REv2 FPGA-based miner has an estimated energy efficiency of 0.80 μJ/Hash at a throughput of 31.25 MHash/s, which is 4.3 and 2.1 times better than an NVIDIA Titan Xp GPU and a commercial FPGA-based miner, respectively. At the same time, the proposed FPGA-based miner is easily reconfigurable so that it can be adapted to future versions of Lyra2RE which may be introduced to deter ASIC-based miners. Furthermore, with trivial changes to our software, our infrastructure could be reused to mine other cryptocurrencies by swapping cores in the chain.

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