A 0.75 V reference clamping sense amplifier for low-power high-density ReRAM with dynamic pre-charge technique

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Abstract There are two major challenges in developing the sensing circuit for ReRAM in deep submicron technologies, including: 1) the reduced sensing margin (SM) due to the lowered supply voltage (VDD); 2) the degraded read access pass yield caused by the increased process-voltage-temperature (PVT) variations. A Reference Clamping Sense Amplifier (RC-CSA) with Amplifier Assisted load PMOS and Dynamic Pre-charge circuit is proposed to deal with these two challenges. Simulation results show that the RC-CSA is able to provide over 200 mV SM with VDD down to 0.55 V. Overall, RC-CSA is very suitable for low-VDD and high-density applications.

Keywords: ReRAM, sense amplifier, sensing margin, low-VDD, PVT variations

Classification: Integrated circuits

1. Introduction

Resistive RAM (ReRAM) is a promising candidate among emerging memory devices due to its fast operation, good endurance, and the compatibility with CMOS back-end-of-line (BEOL) process [1]. However, there are several critical challenges in its periphery circuit design. Firstly, sensing margin (SM) becomes very sensitive to process-voltage-temperature (PVT) variations [2]. As the process technology scaling down, it is difficult to ensure a reliable SM [3]. Secondly, sensing speed is degraded due to the huge parasitic capacitance in bit-line (BL). The huge capacitance is caused by the increasing number of cells integrated in one BL for the purpose of high-density storage [4]. In addition, low-VDD operation is another challenge attributing to the requirements for heat dissipation and energy efficiency in embedded system [5].

To overcome PVT variations and capacitive load in BL, many large-capacity non-volatile memories employ current-mode sense amplifiers (CSA) to achieve faster sensing than those using voltage-mode sense amplifiers (VSA) [6, 7, 8, 9]. However, conventional CSAs are incapable of achieving low-VDD sensing for the reduced SM and the degraded sensing speed. Time-Differential SA (TDSC-SA) and Split-Path SA (SP-SA) are proposed to double the SM [10, 11, 12], however, they suffer from longer sensing time. Body biasing technique (BB-SA) has been introduced to provide faster sensing and to alleviate the limitation in VDD [13, 14], but the enhancement is finitely. Tunable reference voltage was employed to provide an asymmetric and large SM [15, 16], but the additional current mirror may bring larger offset.

This study proposes a low-VDD sensing scheme enabling ReRAM to be sensed under lower VDD with faster sensing, as well as better tolerance to not only PVT variations but also Bit-line (BL) parasitic capacitance compared to conventional SAs. What’s more, the proposed sensing scheme has enhancements in both the thermal reliability and the power consumption. Such improvements are achieved by the idea of Amplifier-assisted load PMOS (AAP) and Dynamic Pre-charge Circuit (DPC).

The rest of this paper is organized as follows: Section 2 discusses the background of the low-VDD sensing for ReRAM. Section 3 describes the proposed low-VDD sensing scheme. Section 4 explains the details and the key points in the RC-CSA design. Section 5 compares the performance and reliability of RC-CSA to other three SAs [10, 14, 17]. Finally, section 6 draws conclusions.

2. Background and related works

2.1 One transistor one ReRAM cell

One Transistor One ReRAM (1T1R) cell as shown in Fig. 1(a) is capable of three operations: SET, RESET and READ. The SET operation changes the ReRAM from high-resistive state (HRS) to low-resistive state (LRS) by applying a SET voltage ($V_{\text{SET}}$) to the BL and 0 V to the Source-line (SL). The RESET operation changes the ReRAM from LRS to HRS by applying a RESET voltage ($V_{\text{RESET}}$) to SL and 0 V to the BL. During READ operation, sensing current $I_{\text{Data}}$ is generated by applying read voltage ($V_{\text{read}}$) to BL and 0 V to SL. Besides, VDD is applied to WL for access to ReRAM during such operations [18].

2.2 Conventional sense amplifiers

The conventional sense amplifier (SA) shown in Fig. 1(b) includes a data branch and a reference generator, which consists of degeneration PMOS transistors (P3, P4), load PMOS transistors (P1, P2) and dynamic clamp NMOS...
transistors (N1, N2) and amplifiers (A1, A2). The path consists of N1, N3, P1, P3 and R\text{Data} is the data branch, and the other path consisting of N2, N4, P2, P4 associated with Ref-cell is the reference branch. Here, R\text{Data} is the cell to be sensed. The Ref-cell, as shown in Fig. 1(c), is applied to create a precise reference current (I\text{Ref}) [19, 20]. The dynamic clamp NMOS (N1/N2) clamps the read voltage (V_{BL}/V_{DBL}) to V_{read}. Furthermore, it also improves the sensing speed by isolating the large parasitic capacitance from Data (Ref) node to BL (DBL) [21].

During the sensing operation, the current difference (\Delta I_{0,1}) between the data (I_{Data0,1}) and the reference (I_{Ref}):

\[ \Delta I_{0,1} = |I_{Data0,1} - I_{Ref}| \]  

(1)

is converted into voltage difference (\Delta V_{0,1}) by the load PMOS pair (P1, P2). The conversion from \Delta I_{0,1} to \Delta V_{0,1} is given by:

\[ SM = \Delta V_{0,1} = |V_{Data0,1} - V_{Ref}| = \Delta I_{0,1} \times R_{load} \]  

(2)

Where \Delta V_{0,1} is also known as the sensing margin (SM), V_{Data0,1} is the output voltage of the Data node for LRS/HRS, R_{load} is the small-signal resistance of the load PMOS.

However, as shown in Fig. 2, the SM of the CON-SA under low-VDD is deficient, which is resulted from a huge Voltage-Headroom (VHR) caused by the diode-connected P2 (VHR_{P2}). VHR_{P2} is determined by the threshold voltage (V_{TH,P2}) and overdrive voltage (V_{io}) of P2, as shown in (4). The VHR_{P2} induces a large voltage drop, so that V_{Ref} is too low to be disguised with V_{Data0}, as shown in (5–6).

\[ V_{HR_{P2}} = |V_{TH,P2}| + V_{io} \]  

(3)

\[ V_{Ref} = \text{VDD} - V_{SD,P4} - V_{HR_{P2}} \]  

(4)

\[ V_{Ref} = \text{VDD} - V_{SD,P4} - |V_{TH,P2}| - V_{sd} \]  

(5)

where V_{SD,P4} represents the source to drain voltage of P4.

Recently, Body-Biasing-SA is proposed to enlarge SM by increasing the voltage difference between source and bulk (V_{SB}) of P1/P2. After that, \[|V_{TH,P2}|\] reduces due to the rise of V_{SB} and further leads to a smaller VHR_{P2} [14, 22]:

\[ |V_{TH}| = |V_{TH0}| + \sqrt{2\varphi_F} - \gamma |2\varphi_F + V_{SB}| \]  

(6)

Where 2\varphi_F is surface potential, \gamma is bulk-effect coefficient and V_{TH0} is the threshold voltage for V_{SB} = 0. The BB-SA can compress \[|V_{TH,P2}|\] to a certain degree, but the SM is still unsatisfactory.

2.3 PVT variations effect

Once the operation of sensing circuit is finished, the two output voltages, V_{Data} and V_{Ref} enter into a latch for the production of digital signal (0 or 1) [23]. Ideally, the latch should magnify the voltage difference (\Delta V_{R}) between V_{Data} and V_{Ref} correctly. However, offset voltage exists in the sensing circuit and latch (V_{OS}), hence \Delta V_{R} must be higher than V_{OS}. The statistical distributions of \Delta V_{0,1} and V_{OS} caused by variation can be modeled as Gaussian distribution, consequently the read access pass yield (RAPY_{CELL,01}) in terms of the mean and standard deviation of \Delta V_{0,1} and V_{OS} can be expressed as follows [24]:

\[ RAPY_{CELL,01} = \frac{\mu_{\Delta V_{0,1}} \times \mu_{V_{os}}}{\sqrt{\sigma_{\Delta V_{0,1}}^2 + \sigma_{V_{os}}^2}} \]  

(7)

Where \mu_{\Delta V_{0,1}} (\mu_{V_{os}}) is the mean of \Delta V_{0,1} (V_{OS}), \sigma_{\Delta V_{0,1}} (\sigma_{V_{OS}}) is the standard deviation of \Delta V_{0,1} (V_{OS}), RAPY_{CELL} is defined as the smaller one between RAPY_{CELL1} and RAPY_{CELL0}. The minimum acceptable RAPY_{CELL} is 6 sigma, which guarantees 96.7% read yield in 32-Mb macro [17].

3. Proposed reference clamping current mode SA

For the achievement of the low-VDD sensing capability while maintaining fast sensing speed as well as high PVT variations tolerance, this work proposes a Reference-Clamping Current mode Sense Amplifier (RC-CSA) that can tolerate large BL parasitic and thermal drift. The RC-CSA and submodule are exhibited in Fig. 3.

3.1 Concept of the amplifier assisted load PMOS

The Amplifier Assisted load PMOS (AAP) shown in Fig. 3 introduces a negative feedback: when reference voltage V_{Ref} is lower than V_{Clamp}, V_{P} will be dropped down by A_{2}, further leading to a larger I_{OS,P2} to pull up V_{Ref}; Contrarily, if V_{Ref} is higher than V_{Clamp}, A_{2} will pull up V_{P}, causing a decrease in V_{Ref}. Eventually, V_{Ref} will be clamped to V_{Clamp}. Such process indicates that the influences of PVT variations can be suppressed by A_{2}.

The main advantage of AAP is that VHR_{P2} is eliminated and a tunable V_{Ref} is achieved by just adjusting V_{Clamp}. Therefore, V_{Ref} can be fixed to the middle of V_{Data0} and V_{Data1} exactly. As a result, a significant}
in SM is imported due to the symmetrical $\Delta V_0$ and $\Delta V_1$ [15, 16].

In addition, the delay time is compressed without trade off in SM. That is due to the time constant in Ref node ($\tau_{\text{ref}}$) is deceased by $A_2$, and a smaller $\tau'_{\text{ref}}$ means a shorter delay time [25]:

$$\tau_{\text{ref}} = \frac{C_{\text{ref}}}{g_{m,p2}}$$

$$\tau'_{\text{ref}} = \frac{C_{\text{ref}}}{G_2 * g_{m,p2}} = \frac{\tau_{\text{ref}}}{G_2}$$

Where $G_2$ is the gain of $A_2$, $g_{m,p2}$ is transconductance of P2, $C_{\text{ref}}$ is the capacitance exists in Ref node and $\tau_{\text{ref}}$ is the time constant in Ref node of CON-SA.

Besides on, the body of the P1 and P2 are connected to Ref and Data respectively, for enlargement in SM. When an HRS cell is accessed, $V_{\text{data}1}$ will be higher than $V_{\text{Ref}}$, on the basis of Eq. (6), $[V_{\text{TH,P1}}]$ will be smaller than $[V_{\text{TH,P2}}]$ and further elevate $V_{\text{data}1}$. On the contrary, $V_{\text{data}0}$ will further drop when an LRS cell is accessed [14].

3.2 Concept of the dynamic pre-charge circuit

Dynamic Pre-charge circuit (DPC) is applied in RC-CSA as well for both quickly pre-charge and faster sensing speed. The proposed DPC is controlled by EQ signal: when EQ is activated, P5 turns off and N5 turns on for the link of the pre-charge PMOS (P3, P4) with $A_2$, P6 also turns on for the equalization of $V_{\text{Data}}$ and $V_{\text{Ref}}$. During this time, pre-charge PMOS (P3, P4) and load PMOS (P1, P2) are connected in parallel to provide strong pre-charge current ($I_{\text{pre}}$) for upraising $V_{\text{DBL}}/V_{\text{BL}}$ to $V_{\text{read}}$:

$$I_{\text{pre}} = I_{P1}/P2 + I_{P3}/P4$$

3.3 Circuit diagram and operation

The timing diagram of the proposed RC-CSA is shown in Fig. 4. The sensing operation of the RC-CSA is divided into three phases: pre-charge (S1), evaluation (S2), and latch (S3). EN and EQ are enabled in S1, therefore P1~P4 work together to provide pre-charge current ($I_{\text{pre}}$) for the quickly pulling up of DBL and BL to $V_{\text{read}}$. Contribute to $A_2$, $V_{\text{Ref}}$ and $V_{\text{Data}}$ are pre-charged to $V_{\text{Clamp}}$ ultimately. During S2, EQ is disabled then N5 and P6 are turned off, meanwhile P5 is activated to disable P3~P4, therefore Amplifier Assisted load PMOS (AAP) can provide an accurate conversion from $\Delta V_0$ to $\Delta V_1$. Finally, the difference between $V_{\text{data}}$ and $V_{\text{Ref}}$ ($\Delta V_{0,1}$) is magnified to digital signal (0 or 1) when CLK is enabled in S3.

4. Design method for the RC-CSA

It is critical to choose a reasonable $V_{\text{read}}$ and $V_{\text{Clamp}}$. $V_{\text{read}}$ decides the voltage to be applied on the ReRAM cell during sensing, although a higher $V_{\text{read}}$ is helpful to obtain faster sensing speed by larger $I_{\text{data}}$, it may induce read disturbance [3]. Here, $V_{\text{read}}$ is set to 220 mV for the tradeoff between performance and reliability. Once $V_{\text{read}}$ is determined, the range of $V_{\text{data}}$ can be confirmed by:

$$V_{\text{data0,min}} \geq V_{\text{read}} \quad (11)$$

$$V_{\text{data1,max}} \leq V_{\text{DD}} \quad (12)$$

Consequently,

$$V_{\text{Clamp}} = \frac{V_{\text{read}} + V_{\text{DD}}}{2} \quad (13)$$
is selected for the balance of $\Delta V_0$ and $\Delta V_1$ to get a maximal $\text{RAPY}_{\text{CELL}}$.

Amplifiers ($A_1, A_2$) and the latch are also important to the performance of the RC-CSA. In the consideration of response time and power consumption, single-stage-structure is implemented for both $A_1$ and $A_2$ as shown in Fig. 5. In the meantime, a voltage-type latch with input voltage ranging from GND to VDD is chosen to match with the large output range in $V_{\text{data}}$ [26, 27], schematic of the latch is exhibited in Fig. 3(c). The sizing of transistors used in RC-CSA are all shown in Table I.

Table I. Sizing of transistors in RC-CSA

| Transistors | Sizing (µm) | Transistors | Sizing (µm) |
|-------------|-------------|-------------|-------------|
| P1/P2       | 2/0.2       | AP1/AP2     | 3/0.2       |
| P3/P4       | 3/0.04      | AP3         | 1/0.04      |
| P5/P6       | 0.5/0.04    | AP4         | 0.5/0.1    |
| N1/N2       | 4/0.1       | AP5         | 2/0.1       |
| N5          | 0.5/0.04    | AN1/AN2     | 1/0.3       |
| P7/P8/P10/P11 | 0.3/0.04 | AP6/AP7     | 1.2/0.8     |
| P9          | 0.6/0.04    | AN3/AN4/AN7 | 2/0.1       |
| N6/N7/N9/N10 | 0.2/0.04  | AN5         | 1/0.04     |
| N8          | 0.4/0.04    | AN6         | 0.5/0.1     |

5. Simulation result and comparison

SPICE Monte Carlo simulations are performed using in UMC 40 nm PDK tools to evaluate the RC-CSA. The variation and mismatch of all MOSFETs used in RC-CSA are taken into concern, which has been listed in Table I. The typical HRS and LRS resistance of ReRAM are chosen to be 100 KΩ and 10 KΩ, and the standard derivation are 15% and 2%, respectively [28, 29]. VDD of 0.75 V is chosen for energy saving. Besides on, a capacitor of 1024 fF is assumed in BL,DBL, which is equivalent to 1024 cells with 1 fF loading for each cell [30]. For comparison, the previous techniques such as [10, 14, 17] are also simulated in the 40 nm SOI technology with the same ReRAM model, amplifiers and latch. MC simulation of 1000 trials are used to calculate $\text{RAPY}_{\text{CELL}}$ in each condition.

5.1 Enlargement in sensing margin

Fig. 6 shows the distribution of $V_{\text{Ref}}$ and the SM according to CON-SA and RC-CSA. In the CON-SA case $V_{\text{Ref}}$ is close to $V_{\text{Data}}$, which lead to an insufficient SM and unacceptable read yield. In the RC-CSA case, the reduced $V_{HR_{22}}$ ensures a lower supply voltage. In addition, $V_{\text{Ref}}$ can be adjusted and clamped by $A_2$, which enhances SM and read yield observably. Furthermore, enlargement in SM and read yield will strengthen the robustness against global process variations.

5.2 Improvement in low-VDD compatibility

Fig. 7 plots the sensing time and read yield as functions of VDD in four SAs, the sensing time and read yield of RC-CSA is superior to other three SAs distinctly under any VDD condition, which can be attributed to the eliminated $V_{HR_{22}}$ by the AAP technique. RC-CSA can even obtain a $\text{RAPY}_{\text{CELL}}$ of 6.1 sigma with 9.5 ns sensing time under 0.55 V VDD, while the best of other three SAs could only manage a $\text{RAPY}_{\text{CELL}}$ of 5.1 sigma with 9.8 ns sensing time under 0.75 V VDD. Such results indicate that RC-CSA is adequate for low-VDD applications.

5.3 Enhancement in thermal reliability

Monte Carlo simulations are also performed under different temperature conditions to evaluate the thermal reliability of four SAs as shown in Fig. 8. The $V_{\text{Ref}}$ generated by AAP is not sensitive to thermal, leading to an excellent performance from ~40°C to 120°C. The minimum $\text{RAPY}_{\text{CELL}}$ of RC-CSA is 7.5 sigma, providing a 99.9% read yield in 32-Mb macro. Such results reveal that the proposed RC-CSA is liberated from thermal drift, and shows a strong robustness against temperature variations.

5.4 Improvement in drive capability

To verify the improvement of RC-CSA’s drive capability,
different Monte Carlo simulations are performed from 256 to 4096 cells per BL/DBL as illustrated in Fig. 9. With the increment in BL load, all four SAs have evident degradation in reliability and sensing speed. Nevertheless, RC-CSA still obtain a $\text{RAPY}_{\text{CELL}}$ of 6.5 sigma with 11.7 ns access time when there are 4096 cells per BL/DBL, which is owning to two factors: Firstly, the AAP strengthen the sensitivity to sensing current and cut off the settling time distinctly. Secondly, the sensing speed is accelerated by DPC obviously. A powerful driven capability means that more cells can be integrated in one BL, which results in higher area utilization.

5.5 Comparison in area and power consumption

The area overhead due to the additional techniques is only 1.5% when the subarray size is 1024 × 8 as exhibited by the layout in Fig. 10. It will further reduce as subarray’s size increases, considering that the proposed RC-CSA is able to drive a BL with 2048 or 4096 cells.

The power dissipation of RC-CSA and CON-SA are 379 fJ/bit and 398 fJ/bit. The enhancement of RC-CSA is resulted from the shorter access time.

Table II summarizes the performance comparisons among RC-CSA with prior works [10, 14, 17].

6. Conclusion

This paper presents a Reference Clamping Sense Amplifier (RC-CSA) with Amplifier Assisted load PMOS (AAP) and Dynamic Pre-charge Circuit (DPC). AAP is capable to achieve low-VDD and high PVT variations tolerance. DPC provides an optimized initial state for a faster sensing speed. The proposed RC-CSA can achieve 99.9% read yield (7.5 sigma) for 32-Mb macro as well as 28% acceleration in sensing speed under 0.75 V VDD. In addition, the RC-CSA is adequate to ensure 96.7% read yield with 0.55 V VDD or 4096 cells existing in one BL. Such results prove that the RC-CSA has a strong robustness against PVT variations and is capable for low-VDD as well as high-density applications.

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