Development of an analog read-out channel for time projection chambers

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Abstract. The development of an analog read-out channel for time projection chambers (TPC) is presented both in schematic and layout. Structure of the channel consists of a preamplifier, fourth order shaper and differential buffer. The channel operates with positive and negative polarities of input charge. The prototype has the following features: dynamic range of 100 fC for both polarities, 20 mv/fC of sensitivity for differential output, peaking time – 160 ns, ENC - <1000e at 40 pF of source capacitance. The presented channel was designed and verified in the CMOS UMC MMRF 180 nm process. The results of post layout simulation are presented.

1. Introduction

Multipurpose detector (MPD) is the key experiment on Nuclotron-based Ion Collider facility (NICA). The MPD time projection chamber (TPC) is the main tracking detector of the central barrel.

The TPC readout system is based on Multi-Wire Proportional Chambers (MWPC) with cathode readout pads. Image charges are induced on an array of pads and are recorded as a function of time. The image charge is measured by a preamplifier/shaper/ waveform digitizer system. For each track segment, the drift time provides a coordinate along the TPC axial line, while the induced signals on the pad provide the coordinates in the plane of the MWPC. The charge induced on the pads is shared between several adjacent pads, so the original track position can be reconstructed to a small fraction of pad width.

The front-end electronics has to read out the charge collected by about 80000 pads located in the readout chambers at the TPC end caps [1]. The main requirements to the front-end electronics are listed in table 1.

| Table 1. Requirements to the front-end electronics. |
|-----------------------------------------------|
| Number of channels | 80000 |
| Signal/Noise ratio | 20/1 |
| Polarity | Pos/Neg |
| Linear range, fC | 100 |
| Detector capacitance (Cd), pF | 40 |
| ENC, e | 1000 @ Cd=40pF |
| Sensitivity, mV/fC | 20 |
| Peaking time (Tp), ns | 160 |
| Shaping order | 4 |
| Power consumption, mW | 10 |
2. Channel structure

The channel consist of preamplifier, forth order shaper and noninverting buffer. The structure is presented on figure 1.

![Figure 1. Structure of the channel](image)

Several preamplifier architectures were simulated, such as telescopic and folded cascode ones with \textit{n}- and \textit{p}-type input transistor. The folded cascode architecture with \textit{n}-type input transistor was chosen due to better dynamic range, signal/noise ratio and speed. The preamplifier operates with both positive and negative polarities. To increase open loop gain, the additional gain boosting circuit is used [3]. The feedback capacitor was chosen to provide correct signal of preamplifier for positive and negative polarities of input charge. The feedback capacitance $C_f$ is 500 fF, and it is discharged by 1 M\(\Omega\) resistor $R_f$. Thus the preamplifier gain is set to 2 mV/fC, and its dynamic range is up to 100 fC. The rise time of preamplifier output signal is 25 ns at 40 pF of $C_d$. The schematic of the preamplifier is presented in figure 2 (biasing is not shown).

![Figure 2. CSA schematic](image)
Shaper is made of two stages of 2nd order filters. The first stage of shaper has similar to CSA folded cascode architecture. It has second order of shaping, based on T-bridge low pass filter scheme. At the shaper output the pulse has a long negative undershoot. Its width and amplitude depends on the time constant of CSA and filter time constant. The undershoot can be eliminated by applying the pole-zero cancellation circuit. The shaper output signal with pole-zero cancellation circuit can be estimated by equation 1 [3].

\[
V_{\text{out}}(s) = \frac{Q_{\text{in}}}{C_f} \times \frac{1}{s+\frac{1}{C_f R_f}} \times \frac{s^2 + \frac{1}{C R_p z}}{s^2 + \frac{1}{C(R_p z|R)}} \times \left(\frac{1}{s C R} + 1\right)^4,
\]

where \(Q_{\text{in}}\) – input charge, \(C\) and \(R\) – capacitor and resistor of differentiator. The long time constant \(\tau\) can be cancelled by adding an extra resistor \(R_{pz}\) if the condition \(C R_f = C R_{pz}\) is fulfilled. To prevent current flowing through P-z resistor, DC voltage of shaper was made the same as in preamplifier.

The second stage of shaper makes differential output signal from single ended input signal. To adjust baseline, common mode feedback was implemented [4]. It establishes common-mode voltage at the output of shaper. The adjustment is carried by external voltage. Peaking time of the channel is 160 ns. Equivalent noise charge (ENC) does not exceed 1000 e.

Because of two polarities of input signal, high gain can not be reached by using only CSA and shaper. To increase gain of the channel, output stage was designed. It based on noninverting differential amplifier. Output stage has baseline adjustment for both positive and negative shoulders of differential signal. The sensitivity of the channel is 10 mV/\(\mu\)C.

3. Layout

The channel was designed for 180 nm CMOS process of UMC (Taiwan). Layout of the channel is presented on figure 3. The die size is 900*100 \(\mu\)m².

![Figure 3. Layout of the channel](image)

4. Simulation

Parasitic elements were extracted from layout. Postlayout simulation results are presented in figures 4, 5.
The output CSA response has the following parameters: rise time – 25ns, fall time – 1500ns. Peaking time is 160ns. Simulation results are shown in table 2.

| Table 2. Channel parameters |
|-----------------------------|
| Technology                  | CMOS UMC 180nm MMRF       |
| Voltage supply, V           | 1.8                       |
| Polarity                    | Pos/Neg                   |
| Linear range, fC            | 100                       |
| Detector capacitance (Cd), pF | 40                        |
| ENC, e                      | 900 @ Cd = 40 pF          |
| Sensitivity, mV/fC          | 20                        |
| Peaking time (Tp), ns       | 160                       |
| Shaping order               | 4                         |
| Power consumption, mW       | 7                         |
| Input transistor geometry, W*L | 2000μm * 360nm            |

5. Conclusion
The development of the analog front-end channel for the time projection chamber of MPD experiment is presented. The ASIC was designed by means of the 0.18 um CMOS MMRF process of UMC. The designed channel has the following parameters: dynamic range of 100fC, ENC of 900 e at Cd=40pF,
peaking time is 160 ns. A power consumption of the channel is 7 mW. The die size is $900\times100 \ \mu m^2$.

Multichannel development, consisting of 32 channels is already ongoing.

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