Connection Pruning for Deep Spiking Neural Networks with On-Chip Learning

Thao N.N. Nguyen  
National University of Singapore  
Singapore  
thaonnnguyen@u.nus.edu

Bharadwaj Veeravalli  
National University of Singapore  
Singapore  
elebv@nus.edu.sg

Xuanyao Fong  
National University of Singapore  
Singapore  
kelvin.xy.fong@nus.edu.sg

ABSTRACT

Long training time hinders the potential of the deep, large-scale Spiking Neural Network (SNN) with the on-chip learning capability to be realized on the embedded systems hardware. Our work proposes a novel connection pruning approach that can be applied during the on-chip Spike Timing Dependent Plasticity (STDP)-based learning to optimize the learning time and the network connectivity of the deep SNN. We applied our approach to a deep SNN with the Time To First Spike (TTFS) coding and has successfully achieved 2.1x speed-up and 64% energy savings in the on-chip learning and reduced the network connectivity by 92.83%, without incurring any accuracy loss. Moreover, the connectivity reduction results in 2.83x speed-up and 78.24% energy savings in the inference. Evaluation of our proposed approach on the Field Programmable Gate Array (FPGA) platform revealed 0.56% power overhead was needed to implement the pruning algorithm.

CCS CONCEPTS
• Computing methodologies → Bio-inspired approaches; • Computer systems organization → Neural networks.

KEYWORDS
Connection Pruning, Spiking Neural Networks, On-Chip Learning, Hardware Accelerator

1 INTRODUCTION

Spiking Neural Network (SNN) has been increasingly used in the energy-aware real-time applications on the embedded systems platforms [1, 9, 27]. Due to its event-driven nature, SNN has the potential to be more energy-efficient than the Artificial Neural Network (ANN). However, the SNN architectures that achieve the high accuracy are usually deep and large, consisting of multiple layers and thousands of neurons and connections [5, 9, 12, 19]. For example, the SNN architecture proposed in [5] consists of 6 layers with more than 14,500 neurons and 29,000 connections, and achieved an accuracy of 99.14% on the MNIST dataset. The authors of [19] implemented an SNN based on the VGG-16 architecture [26], which consists of more than 138 million connections, and achieved an accuracy of 65.19% on the ImageNet dataset. The large-scale SNNs require long computation time and large amount of hardware resources, which limits their potential to be realized on the embedded systems platforms [23, 30]. Therefore, we are motivated to explore the techniques to compress the SNN to optimize the computation time, hardware resources, and energy consumption on the neuromorphic hardware. Our work aims to improve both the learning and the inference time of the SNN while minimizing the loss in the accuracy.

There are two common approaches to convert the continuous inputs to the spike events: rate-based coding and temporal coding. In the rate-based coding, the input value is encoded into the spike frequency. An input that has a large value is converted to a series of spike events that occur frequently. On the other hand, in the temporal coding, the input value is encoded into the spike timing, and each neuron spikes at most once for every input. An input that has a large value is converted to a spike event that occurs early. As compared to the rate-based coding, the temporal coding consumes less energy as a fewer number of spikes are generated [20]. In the temporal coding, the input information can be encoded into the relative order (rank order coding) or the latency (TTFS coding) of the spikes. The TTFS coding has been used in many recent works, such as the ones in [12, 13, 17], to solve challenging real-world problems. Therefore, our work focuses on developing a connection pruning algorithm for the SNN with the TTFS coding, which is more energy-efficient than the rate-based coding.

Connection pruning is a compression technique that has been applied to ANN [10, 15] and SNN [3, 4, 11, 14, 18, 23–25, 29] to reduce the network complexity and energy consumption. It has been shown that more than half of the connections in a well-performing neural network can be removed with minimal impact on the classification accuracy [11, 15]. The connection pruning can be performed either on a pre-trained network [3, 23] or during the network learning [18, 24, 25, 29]. The authors of [23] have proposed a heuristic connection pruning algorithm for the pre-trained SNN, in which the connection weights are obtained by converting from those of an ANN. The connection pruning is triggered periodically during the inference stage, based on the neuron parameters such as spike rate, membrane potential, and connectivity. Although this approach has efficiently improved the number of operations and hardware energy during the inference stage, it cannot be applied to the applications
that require the on-chip learning capability on hardware [1, 21, 27]. In addition, the work in [23] focuses on the SNN with the rate-based coding, in which a neuron spikes multiple times during the feed-forward computation of an input image. The spike rate indicates the activity of the neurons and varies greatly among the neurons in the network. In this case, it can be used as a pruning parameter to remove a higher percentage of connections from the less active neurons. However, in the TTFS coding, each neuron spikes at most once in the feed-forward computation. Consequently, the spike rate does not vary as much as in the rate-based coding and cannot be used as a pruning parameter. For this reason, the works in [23] and [24, 25, 29], which depend on the spike rate of the neurons to prune the connections, are not applicable to the SNN with the energy-efficient TTFS coding. Therefore, we proposed a connection pruning approach that is applicable to the energy-efficient TTFS coding. In addition, our approach can be applied during the STDP-based learning to support the applications that require the on-chip learning capability.

Previously, the authors of [18] have proposed an algorithm that skips the membrane potential update when the connection weight is below a threshold during the STDP-based learning. The connection is not eliminated from the network; it can still participate in the STDP-based learning and has a chance to be strengthened in the future. Completely eliminating the connections may lead to pre-mature pruning (as these connections may be strengthened later during the STDP-based learning) and cause accuracy degradation. However, it helps to reduce not only the number of membrane potential updates but also the number of weight updates during the STDP-based learning. Therefore, we are motivated to develop a connection pruning approach that is capable of eliminating the connections completely during the STDP-based learning while minimizing the accuracy loss.

In this work, we propose a novel connection pruning approach to prune the SNN with the TTFS coding during the on-chip STDP-based learning. As will be discussed in Section 6, our approach can improve the learning time by 2.1x, reduce the network connectivity by 92.83%, and save 64% energy consumption during the on-chip learning without causing accuracy degradation. As compared to our baseline (without pruning), we achieved 2.83x speed-up and 78.24% reduction in inference time and energy consumption, respectively. Furthermore, our hardware implementation for the connection pruning incurs as little as 0.56% overhead in the power consumption as compared to our baseline hardware implementation with the pruning units removed. Crucially, our proposed connection pruning approach can be applied during the on-chip STDP-based learning for deep SNN with the TTFS coding. Note that it is more challenging to apply the connection pruning on a deep SNN than on a one-layer SNN as the learning errors may propagate through the network layers, causing more spuriousness in the deep layers. It is also more challenging to compress the SNN with the TTFS coding as compared to the rate-based coding. In the TTFS coding, there are few spikes emitted, as one neuron emits at most one spike. Removing the connections, which causes the number of spikes to decrease, may lead to insufficiency of spikes to activate the spike activities in the deep layers.

2 PRELIMINARIES

Figure 1: An example of the potential accumulation in the postsynaptic neuron \( m \) connected to three presynaptic neurons \( n_1, n_2, \) and \( n_3 \). The connection weights are \( w_{m1}, w_{m2}, \) and \( w_{m3} \) respectively. When there is a spike from one of the presynaptic neurons, the membrane potential \( V_m \) of neuron \( m \) is increased by the corresponding weight. When \( V_m \) exceeds the firing threshold \( V_{th} \), neuron \( m \) emits a postsynaptic spike.

In SNN, the inputs are discrete spike events. When a spike event arrives at a neuron, the corresponding synaptic weight is accumulated in the membrane potential of the neuron. In our work, the potential accumulation follows the Integrate and Fire (IF) model [6], formulated in the following equation:

\[
v_i(t) = v_i(t-1) + \sum_j w_{j,i}s_j(t-1)
\]

where

\[
s_i(t) = \begin{cases} 
1 & \text{if neuron } i \text{ spikes at time } t \\
0 & \text{otherwise}
\end{cases}
\]

\( v_i(t) \) and \( s_i(t) \) are the membrane potential and postsynaptic spike of neuron \( i \) at time \( t \), \( w_{j,i} \) is the synaptic weight between neuron \( i \) and neuron \( j \). The overview of this membrane potential accumulation is illustrated in Figure 1. As soon as the membrane potential exceeds the firing threshold, the neuron fires a postsynaptic spike and inhibits the other neurons that are close to it in the network.

The STDP-based learning algorithm in SNN is performed based on the correlation between the presynaptic spike and postsynaptic spike of a connection. If the postsynaptic spike occurs within a small time window from the presynaptic spike, the two spikes are considered correlated and the connection is strengthened. This process is called Long Term Potentiation (LTP). Otherwise, the two spikes are considered uncorrelated and the connection is weakened. This process is called Long Term Depression (LTD) [28]. In our work, we applied a hardware-friendly STDP-based learning algorithm, as proposed in the work in [12]. In this algorithm, the synaptic weights are updated based on the following Equation:

\[
\Delta w = \begin{cases} 
-a^+w_{ij}(1-w_{ij}) & \text{if } t_j - t_i \leq 0 \\
-a^-w_{ij}(1-w_{ij}) & \text{otherwise}
\end{cases}
\]
3 PROPOSED CONNECTION PRUNING APPROACH

In order to compress the SNN and reduce the on-chip STDP-based learning time, we propose a connection pruning approach consisting of two stages: (i) dynamic pruning during the on-chip STDP-based learning in every layer and (ii) post-learning pruning after each layer has learned, as shown in Figure 2. Note that both of these stages are performed during the on-chip STDP-based learning.

3.1 Dynamic Pruning During The On-chip STDP-Based Learning

In the dynamic pruning stage, the connection pruning is performed after every \( k \) iterations during the on-chip STDP-based learning in each layer, based on two parameters: (i) weight update history, \( h \), of the synaptic connection and (ii) time of postsynaptic spike, \( t_{\text{post}} \). In the following, we will explain these parameters and present the details of our dynamic pruning approach.

3.1.1 Weight Update History. The weight update history, \( h \), is defined in the following equation:

\[
h = \frac{d}{w}
\]

where \( d \) is the number of times the LTD is performed on the connection, or the number of times the connection weight is decreased, in \( k \) learning iterations. \( w \) is the weight value at the time of pruning. The goal is to prune the connections having weights that are (i) small and (ii) decreasing steeply throughout a number of learning iterations. Note that the connection weights of the SNN emulated in our work are in the range \([0, 1]\). The intuition is that if a connection weight, which is in the range \([0, 1]\), has been decreasing steeply in a time period and has reached a small value, it will likely continue to decrease until it approaches zero. Therefore, we propose to prune these connections early to reduce the number of membrane potential updates and learning computations in the future iterations. For example, in Figure 3a, which shows the learning progress of selected weights during the on-chip STDP-based learning performed on our hardware implementation, weights \( w_2 \) and \( w_3 \) decrease steeply to a small value (less than 0.1) from iteration 2000 to 2500 and 1500 to 2000, respectively. In the later iterations, these weights contribute little to the spiking activities and will approach zero eventually. Consequently, \( w_2 \) can be pruned at iteration 2000 and \( w_3 \) can be pruned at iteration 2500, as shown in Figure 3b. Note that having the weight value in the denominator helps to reduce the chance of pre-mature pruning, in which the connection is pruned when it still contributes non-negligibly to the spiking activities.

3.1.2 Time of Postsynaptic Spike. In addition to the weight update history, our proposed pruning approach considers the synaptic competition during the on-chip STDP-based learning to formulate the pruning decision. The connection weights that are decreased during a strong synaptic competition should be less likely to be

Figure 2: Overview of our two-stage connection pruning approach.

Figure 3: Weight values of selected connections throughout the iterations of the on-chip STDP-based learning performed on our hardware implementation (a) without connection pruning (b) with connection pruning.
presynaptic neurons and a postsynaptic neuron. (a) $s_{\text{post}}$ spikes earlier, more connection weights are decreased; (b) $s_{\text{post}}$ spikes later, fewer connection weights are decreased.

Figure 4: Examples of the spiking activities of four presynaptic neurons $s_1, s_2, s_3, s_4$ and a postsynaptic neuron $s_{\text{post}}$. In our implementation of the on-chip STDP-based learning, the connection weights are increased if the presynaptic neurons spike before the postsynaptic neurons; otherwise, the connection weights are decreased, as described in Section 2. If there are many large connection weights, few spike events are needed to cause the membrane potential of the postsynaptic neuron to exceed the firing threshold. Hence, only the most competitive connections that have the largest weight values and carry the earliest presynaptic spikes will be able to contribute to the spiking of the postsynaptic neuron. Figure 4a shows an example to illustrate this scenario. When the postsynaptic spike, $s_{\text{post}}$, is emitted early, it is only the presynaptic spikes $s_1$ and $s_3$ that were early enough to contribute to $s_{\text{post}}$ and their connection weights will be increased. Contrarily, although $s_2$ is relatively early as compared to $s_4$ and its connection weight may be large, it was not able to contribute to $s_{\text{post}}$. Consequently, the connection weight associated with $s_2$ will be decreased. On the other hand, if $s_{\text{post}}$ is emitted later, as shown in Figure 4b, $s_2$ will be able to contribute to $s_{\text{post}}$ and its connection weight will be increased. Therefore, the weight decrements in the former scenario (Figure 4a) should be weighted less than the weight decrements in the latter scenario (Figure 4b) in the connection pruning decision.

The strong synaptic competition, as explained above, may happen in the early iterations in the on-chip STDP-based learning on our hardware, as shown in Figure 3a. We initialized the connection weights to follow the normal distribution in the range of (0, 1) with the mean being skewed at 0.8, following the work in [22]. This is to encourage the spiking activities and to emphasize the most dominant presynaptic spikes and connections in the early iterations of the learning. The connections that have smaller weights or carry less dominant presynaptic spikes will have their weights decreased. However, these connections still have a chance to have their weights increased in a later learning iteration, when many of the other connections are weakened and the postsynaptic neurons do not spike as early as before, as shown in weight $w_1$ in Figure 3a. Therefore, the time of postsynaptic spikes, $t_{\text{post}}$, helps to avoid pruning these connections in the early learning iterations when the synaptic competition is strong.

3.1.3 The Dynamic Pruning Approach. The proposed dynamic pruning approach combines $h$ and $t_{\text{post}}$ into a pruning parameter $P$:

$$P = h \ast t_{\text{post}}$$

Combining equations (4) and (5), we have:

$$P = \frac{d}{w} \ast t_{\text{post}}$$

$P$ is evaluated for every connection in every $k$ iterations of the on-chip STDP-based learning. If $P$ is greater than a pre-defined threshold $\alpha$, the connection is pruned. This dynamic pruning stage is performed during the on-chip STDP-based learning in each layer. After the learning is finished, we proceed to the post-learning pruning stage, which we will describe next.

3.2 Post-Learning Pruning

Our post-learning pruning approach is performed after the learning in one layer has finished, before proceeding to the next layer, as shown in Figure 2. In the post-learning pruning stage, all the connections that have the weights less than a threshold, $\beta$, are eliminated. Note that although this stage is performed after the learning in a layer, it is still within the on-chip learning process of the SNN. It differs from the existing pruning approaches on the pre-trained networks as it can affect the learning in the next layer. Overly aggressive pruning of the preceding layer will lead to learning errors in the next, causing losses in the classification accuracy.

4 EVALUATION HARDWARE ARCHITECTURE

We designed an event-driven hardware architecture that incorporates our proposed connection pruning approach to reduce the on-chip learning time and the network connectivity for SNN, as shown in Figure 5. The overall flow of our hardware architecture is as
follows. In every time step, the Controller receives the spike events and forwards them to the Processing Elements (PEs). The PEs compute the membrane potentials and update the Potential Memory. At the end of the time step, the PEs compares each membrane potential in the Potential Memory with a pre-defined firing threshold. If the membrane potential of a neuron exceeds the firing threshold, the PE writes the corresponding neuron ID to the Spike Memory. Finally, the Controller activates the STDP unit to perform the weight updates based on the STDP-based learning algorithm that was described in Section 2. During the learning, the STDP unit records the decrements of the weight values of each connection in the Decrement Track Memory.

The connection pruning is performed in the Prune Unit in every \(k\) iterations. After the STDP unit finishes updating the connection weights for the current time step, the Prune unit evaluates the pruning criteria for each connection weight (described in Section 3). If the pruning criteria is met, the corresponding connection weight is set to zero in the Weight Memory. The pruning components incur little overheads in the resources and power consumption in our hardware implementation which we will discuss in the following sections.

5 EXPERIMENTAL SETUP

This section describes our experimental setup to evaluate our proposed connection pruning approach and hardware architecture. We will first present the hardware platform on which our hardware architecture was implemented, followed by the dataset and the SNN network parameters used in our experiments.

5.1 Hardware Platform

Our hardware architecture was implemented on the Zynq-7000 Zedboard (XC7Z020) using Verilog. The hardware resources and power consumption were estimated by Xilinx Vivado 2018.3 [8]. Our hardware implementation of the connection pruning incurs less than 3.52% overheads in the LUTs and FFs and approximately 8.7% overheads in the BRAM consumption as compared to our baseline hardware implementation (with the Prune Unit and the Decrement Track Memory removed). In addition, 11 DSP slices were used in the implementation of the connection pruning, which is 5% of the DSP slices available on the board. The power consumption was increased by 0.56% as compared to our baseline hardware implementation (no pruning). These overheads are reported based on the post-implementation estimation generated by Xilinx Vivado 2018.3. Our hardware implementation was run at the clock frequency 100 MHz.

5.2 Dataset and Network Configuration

Our connection pruning approach was evaluated on the Caltech 101 dataset [7]. The training set consists of 396 images. The test set consists of 396 images. Our hardware implementation of the SNN was based on [12] and [22]. The SNN implemented on our hardware consists of three convolutional-pooling layers. The kernels of the three convolutional layers are of size 5x5x4, 17x17x20, and 5x5x20 (width x height x depth). In between the convolutional layers, the downsampling was performed with window sizes 7x7 and 5x5, respectively. Our connection pruning approach was applied to the convolutional layers. Following to the work in [12], the images were pre-processed using a Difference of Gaussians (DoG) filter, followed by the SNN emulated on our hardware implementation, and classified using a Support Vector Machine (SVM). Note that our work does not focus on improving this model but developing a connection pruning algorithm to reduce the network complexity of the SNN architecture. The effects of our connection pruning approach will be discussed in the following section.

6 RESULTS AND DISCUSSION

The performance of our connection pruning approach was evaluated based on the following four metrics: (i) the number of connections reduced in the network, (ii) the time speed-up, (iii) the energy saved, and (iv) the classification accuracy. In this section, we will discuss the trade-offs between these metrics. In addition, the individual effects achieved by each of the stages: (i) dynamic pruning and (ii) post-learning pruning in our two-staged connection pruning approach will be analysed. Finally, we will discuss the impacts of connection pruning on the network behaviours in the inference stage. We will demonstrate that our connection pruning approach successfully eliminates a significant number of connections during the on-chip STDP-based learning, which helps to reduce the time and energy in both the learning and the inference stages, without incurring any accuracy loss.

6.1 Connectivity Reduction vs. Accuracy

Our proposed connection pruning approach helps to eliminate 92.83% connections in the network without incurring any loss in the classification accuracy, as presented in Figure 6. This is consistent with the result in [11] that more than 90% of the connections can be eliminated after one million iterations of the STDP-based learning, regardless of the network size. However, in the work in [11], the connections are eliminated after a large number of iterations (one million iterations). Our connection pruning approach eliminates the connections early to save the on-chip learning time while preserving the accuracy. Different trade-offs between the

Figure 6: Connectivity reduction and accuracy trade-offs. The connectivity reduction was computed as \(n_{\text{pruned}}/n_{\text{total}}\), where \(n_{\text{pruned}}\) is the number of connections being pruned and \(n_{\text{total}}\) is the total number of connections in the network.
number of connections eliminated and the accuracy loss are presented in Figure 6. The number of connections in the network can be reduced by 92.83% without incurring any loss in the accuracy. Moreover, when the accuracy is allowed to fall within 1.2%, the network can be compressed by 92.9%. When up to 1.8% loss in the accuracy is allowed, the network connectivity can be reduced by 93.35%. In addition, when the accuracy loss is maintained within 2%, the connectivity can be reduced by up to 95.07%. The proposed connection pruning algorithm, which does not cause any loss in the classification accuracy, helps to reduce the number of connections to 9.7 times-55 million times fewer than other SNN implementations in the existing works, as shown in Table 1. Note our work does not aim to achieve the highest accuracy but a balance between the accuracy and the network complexity, which has significant impacts on the response time and the energy consumption on embedded systems platforms. In the case our connection pruning algorithm is performed off-chip (no on-chip learning is needed), it can help to reduce the number of entries in the Weight Memory by 92.83% as compared to our baseline (the SNN described in Section 5.2).

### 6.2 Improvements in Learning Time and Energy Consumption

The speed-up in the on-chip STDP-based learning time depends on (i) the number of connections being pruned in the network and (ii) the earliness of the pruning during the on-chip learning. Our connection pruning approach helps to speed-up the on-chip learning time by 2.1x without incurring any loss in the classification accuracy, as shown in Figure 7. In addition, when the accuracy loss is up to 1.2%, the learning time is improved by 2.14x. Furthermore, the learning time can be improved by up to 2.26x and 2.31x when the accuracy is allowed to fall within 1.8% and 2%, respectively. In addition to the learning time, the energy consumption during the STDP-based learning is also improved as a result of the network compression. In our experiments, the energy saving is estimated based on the number of operations reduced, similar to the related work in [18]. As shown in Figure 7, the energy consumption is reduced by 64-69.62% with 0-2% loss in the accuracy. The improvements on the learning time and the energy consumption were attributed to the two stages in our connection pruning approach: dynamic pruning and post-learning pruning, which we will analyse in the following.

![Figure 7: Trade-offs between learning time, energy consumption, and classification accuracy of the SNN emulated on our hardware implementation. The learning time speed-up and energy reduction are computed as $\frac{t_{\text{pruned}}}{t_{\text{unpruned}}}$ and $(1 - \frac{E_{\text{pruned}}}{E_{\text{unpruned}}}) \times 100$, respectively. $t_{\text{pruned}}$ and $E_{\text{pruned}}$ are the learning time with and without the connection pruning, $E_{\text{unpruned}}$ and $E_{\text{unpruned}}$ are the energy consumption in the learning with and without pruning.](image)

#### Table 1: Classification accuracy achieved on the Caltech-101 (Face/Motorbike) dataset.

| SNN Architecture | [16] | [17] | [12] | [13] | [31] | Our Work |
|------------------|------|------|------|------|------|----------|
| Learning Algorithm | STDP | Reward-modulated STDP | STDP | Back-propagation | Back-propagation | STDP |
| Platform | GPU | GPU | STDP | Back-propagation | STDP | STDP |
| # Learnable Parameters | 25,488 | 23,120 | 25,480 | 160,008 | >110 M | 2,383 |
| On-Chip Learning on Embedded Hardware | No | No | No | No | No | Yes |
| Accuracy | 97.6% | 98.9% | 99.1% | 99.2% | 99.5% | 95.7% |

#### Table 2: Impacts of dynamic pruning and post-learning pruning when applied individually and when combined together in our two-staged connection pruning approach.

| Connectivity Reduction | Dynamic Pruning | Post-Learning Pruning | Combined Approach |
|------------------------|-----------------|-----------------------|--------------------|
| Learning Time Speed-up | 2x | 1.78x | 2.1x |
| Energy Reduction | 62% | 48% | 64% |

#### 6.3 Dynamic Pruning vs. Post-Learning Pruning

Each of the two stages: (i) dynamic pruning and (ii) post-learning pruning in our connection pruning approach has its own effects on the network connectivity and the learning time. While the dynamic pruning is performed periodically during the learning in each layer, the post-learning pruning is performed after the learning in the layer has finished, as illustrated in Figure 2. Therefore, the dynamic pruning can eliminate the connections earlier than
the post-learning pruning. When the two approaches are applied separately, the dynamic pruning achieves a higher learning time speed-up and energy reduction, as shown in Table 2. However, the connectivity reduction achieved by the dynamic pruning is less than the post-learning pruning, as shown in Table 2. The reason is that during the learning, the network needs to maintain sufficient connections to generate the spike events in order to stimulate the STDP-based weight updates. On the other hand, after the learning in the layer has finished, the weights can be pruned without the concerns of the learning activities. Our connection pruning approach combines the dynamic pruning and the post-learning pruning to achieve the high learning time speed-up, high energy saving and significant connectivity reduction.

6.4 Impact on Inference Stage
The network compression during the STDP-based learning significantly reduces the response time and energy consumption in the inference stage. As shown in Figure 9, the inference time on our hardware implementation is speeded-up by 2.83-3.1x when 92.83-95% of the connections in the network are eliminated. In addition, the energy consumption is reduced by 78.24-81.47% as compared to our baseline without pruning. Meanwhile, the number of spikes generated in the inference is preserved at 95% compared to the SNN trained without the connection pruning. Figure 8 shows the feature maps of different images in the Caltech 101 dataset in different convolutional layers. The first convolutional layer extracts the edges in the images while the deeper layers observe more abstract features. The feature maps obtained in the SNN trained with the connection pruning (Figure 8b) are similar to the ones obtained in the SNN trained without the connection pruning (Figure 8a). This demonstrates that our connection pruning approach does not significantly affect the network behaviours in the inference. Therefore, the classification accuracy was preserved.

6.5 Comparison with Existing Works
Prior to our work, there have been approaches that eliminate the weak connections and dormant neurons in the well-trained spiking networks [3, 23]. However, these works are not applicable during the on-chip learning, when the weight values have not converged. This limits the potential of these works to be applied to the applications that require frequent online learning [1, 21, 27]. On the other hand, the approaches in [14, 18, 25] and our work eliminate the connections during the on-chip learning. While the works in [14, 25] focus on the SNN with the rate-based coding, our work proposes a connection pruning approach for the SNN with the TTFS coding,
which is more energy-efficient [20]. Note that it is more challenging to eliminate the connections for the SNN with the TTFS coding, as the spike activities are sparser than the rate-based coding. The connection pruning may cause the number of spikes to drop drastically, causing the shortage of spike activities to trigger the weight updates in the STDP-based learning. In addition, our connection pruning approach was evaluated on a deep SNN, consisting of three convolutional layers, while the works in [2, 18, 25] was applied to the SNNs consisting of one layer. It is more challenging to eliminate the connections during the STDP-based learning in a deep SNN as compared to an SNN with a single layer. In the deep SNN, the errors caused by the overly aggressive pruning in a layer will be carried to the following layers and may eventually increase accuracy loss.

7 CONCLUSIONS
In this paper, we have proposed a novel connection pruning approach to be applied during the on-chip STDP-based learning for SNN, in which the spikes are encoded using TTFS. Our main contributions are three-fold. First, we proposed a novel connection pruning approach that helps to compress the network and speed-up the on-chip learning time on embedded systems hardware. Our connection pruning approach was evaluated on a deep convolutional SNN and achieved the compression of 92.83% without incurring any loss in the classification accuracy. Second, evaluation on the FPGA platform showed that the on-chip learning time was reduced by 2.1x and the inference time was reduced by 2.83x as compared to our baseline with the connection pruning turned off. Moreover, the energy consumption was reduced by 64% in the on-chip learning and 78.24% in the inference as compared to the baseline. The hardware implementation of the connection pruning incurs 0.56% power overhead as compared to our hardware implementation with the pruning units removed. Third, while most of the existing works perform the compression on a well-trained network, our connection pruning approach can be applied during the on-chip STDP-based learning. In addition, our approach is applicable to the SNN with the TTFS coding while most of the existing works focus on the SNN with the rate-based coding, which consumes more energy. In the future, our approach can be combined with various device-level optimizations to further reduce the delay, hardware resources, and energy consumption of SNN implementations on embedded systems platforms.

ACKNOWLEDGMENTS
This work is supported in part by the NUS Start-up Grant, in part by the Ministry of Education (Singapore) Academic Research Fund (Tier 1), and in part by the A*STAR Programmatic Research Grant (SpOT-LITE).

REFERENCES
[1] Anton Akusok, Kaj-Mikael Björk, Leonardo Espinosa Leal, Yoan Miche, Renjie Hu, et al. 2019. Spiking networks for improved cognitive abilities on the spinnaker many-core neuromorphic system. Front. Neurosci. 13 (2019), 434.
[2] Peter U Diehl, Daniel Neil, Jonathan Binns, Matthew Cook, Shih-Chii Liu, and Michael Pfeiffer. 2015. Fast-classifying, high-accuracy spiking deep networks through weight and threshold balancing. In Proc. IJCNN, IEEE, 1–8.
[3] Eiji Komemjrot. 1996. Type I membranes, phase resetting curves, and synchrony. Neural Comp. 8, 5 (1996), 979–1001.
[4] Rufin Van Rullen and Simon J Thorpe. 2001. Rate coding versus temporal order regularization. arXiv preprint arXiv:1911.08623 (2019).
[5] Peter U Diehl, Daniel Neil, Jonathan Binns, Matthew Cook, Shih-Chii Liu, and Michael Pfeiffer. 2015. Fast-classifying, high-accuracy spiking deep networks through weight and threshold balancing. In Proc. IJCNN, IEEE, 1–8.
[6] Tom Feist. 2012. Vivado design suite. White Paper 5 (2012), 30.
[7] Xuchen Guan and Lingfei Mo. 2020. Unsupervised conditional reflex learning based on convolutional spiking neural network and reward modulation. IEEE Access 8 (2020), 17673–17690.
[8] Babak Hassibi and David G Stork. 1993. Second order derivatives for network pruning: Optimal brain surgeon. In Proc. NIPS. 164–171.
[9] Xavier Guzzetti, Jan Eriksson, François Grize, Marco Tomassini, and Alessandro EP Villa. 2005. Dynamics of pruning in simulated large-scale spiking neural networks. Biosystems 79, 1-3 (2005), 11–20.
[10] Jianwei Han, Rola Fergus, and Pietro Perona. 2004. Learning generative visual models from few training examples: An incremental bayesian approach tested on 101 object categories. In Proc. CVPR, 178–178.
[11] Suchow Huang, Lingfei Mo, and Yuan Xie. 2019. Comprehensive snn compression using admm optimization and activity regularization. arXiv preprint arXiv:1911.08623 (2019).
[12] Jiajun Huang, Cheng-Yang Kung, Gaurav Datta, Maunder Pedram, and Peter A Beere1. 2021. Spike-Threshold: Towards Energy-Efficient Deep Spiking Neural Networks by Limiting Spiking Activity via Attention-Guided Compression. In Proc. WACV. 3953–3962.
[13] Nitin Rathi, Priyadarshini Panda, and Kaushik Roy. 2018. Deep spiking convolutional neural network trained with unsupervised spike-timing-dependent plasticity. IEEE Trans. Cogn. Dev. Syst. 11, 3 (2018), 384–394.
[14] Nitin Rathi, Priyadarshini Panda, and Kaushik Roy. 2018. STDP-based pruning of connections and weight quantization in spiking neural networks for energy-efficient inference. IEEE Trans. Comput.-Aided Design Integr. Circuits Syst. 38, 4 (2019), 660–677.
[15] Milad Mozafari, Saeed Reza Kheradpisheh, Timothée Masquelier, Abbas Nowzari-Dalini, and Mohammad Ganjtabesh. 2018. First-spike-based visual categorization using reward-modulated STDP. IEEE Trans. Neural Netw. Learn. Syst. 29, 12 (2018), 6178–6190.
[16] Javier Iglesias, Jan Eriksson, François Grize, Marco Tomassini, and Alessandro EP Villa. 2005. Dynamics of pruning in simulated large-scale spiking neural networks. Biosystems 79, 1-3 (2005), 11–20.
[17] Bard Ermentrout. 1996. Type I membranes, phase resetting curves, and synchrony. Neural Comp. 8, 5 (1996), 979–1001.
[18] Runchun M Wang, Chetan S Thakur, and André van Schaik. 2018. An FPGA-based counts based low complexity SNN architecture with binary synapse. Trans. Biomed. Circuits Syst. 13, 6 (2019), 1664–1677.
[19] Malu Zhang, Jiadong Wang, Burin Amornpaisannon, Zhixuan Zhang, VPK Thrift, and Yuan Xie. 2019. Comprehensive snn compression using admm optimization and activity regularization. arXiv preprint arXiv:1911.08623 (2019).
[20] Rufin Van Rullen and Simon J Thorpe. 2001. Rate coding versus temporal order regularization. arXiv preprint arXiv:1911.08623 (2019).
[21] Xucheng Peng and Liu Cong. 2020. Rectified Linear Postsynaptic Potential Function for Backpropagation Learning: Learning Deep Neural Networks on the Fly. In Proc. ICASSP, IEEE, 8524–8528.
[22] Doyen Sahoo, Quang Pham, Jing Lu, and Steven CH Hoi. 2018. Neuroinspired unsupervised learning and pruning with subquantum CBRAM arrays. Nat. Commun. 9, 1 (2018), 1–11.
[23] Yuan Xie and Yuan Xie. 2019. Comprehensive snn compression using admm optimization and activity regularization. arXiv preprint arXiv:1911.08623 (2019).
[24] Sen Song, Kenneth D Miller, and Larry F Abbott. 2000. Competitive Hebbian learning through spike-timing-dependent synaptic plasticity. Nat. Neurosci. 3, 9 (2000), 919–926.
[25] Huyoung Tang, Jeetacep Kim, Hyoeonseong Kim, and Jongun Park. 2019. Spike Counts Based Low Complexity SNN Architecture With Binary Synapse. IEEE Trans. Biomed. Circuits Syst. 13, 6 (2019), 1664–1677.
[26] Runchun M Wang, Chetan S Thakur, and André van Schaik. 2018. An FPGA-based counts based low complexity SNN architecture with binary synapse. Trans. Biomed. Circuits Syst. 13, 6 (2019), 1664–1677.
[27] Malu Zhang, Jiadong Wang, Burin Amornpaisannon, Zhixuan Zhang, VPK Thrift, and Yuan Xie. 2019. Comprehensive snn compression using admm optimization and activity regularization. arXiv preprint arXiv:1911.08623 (2019).
[28] Huyoung Tang, Jeetacep Kim, Hyoeonseong Kim, and Jongun Park. 2019. Spike Counts Based Low Complexity SNN Architecture With Binary Synapse. IEEE Trans. Biomed. Circuits Syst. 13, 6 (2019), 1664–1677.