Hardware Implementation of Neural Self-Interference Cancellation

Yann Kurzo, Andreas Toftegaard Kristensen, Andreas Burg, Member, IEEE, 
Alexios Balatsoukas-Stimming, Member, IEEE

Abstract—In-band full-duplex systems can transmit and receive information simultaneously and on the same frequency band. However, due to the strong self-interference caused by the transmitter to its own receiver, the use of non-linear digital self-interference cancellation is essential. In this work, we describe a hardware architecture for a neural network-based non-linear self-interference (SI) canceller and we compare it with our own hardware implementation of a conventional polynomial based SI canceller. Our results show that, for the same SI cancellation performance, the neural network canceller has an 8.1× smaller area and requires 7.7× less power than the polynomial canceller. Moreover, the neural network canceller can achieve 7 dB more SI cancellation while still being 1.2× smaller than the polynomial canceller and only requiring 1.3× more power. These results show that NN-based methods applied to communications are not only useful from a performance perspective, but can also lead to order-of-magnitude implementation complexity reductions.

I. INTRODUCTION

In-band full-duplex (FD) communications have for long been considered to be impractical due to the strong self-interference (SI) caused by the transmitter to its own receiver. However, recent work on the topic (e.g., [2], [3], [4]) has demonstrated that it is, in fact, possible to achieve sufficient SI cancellation (SIC) to make FD systems viable. Typically, SIC is performed in both the radio frequency (RF) domain and the digital domain to cancel the SI signal down to the level of the receiver noise floor. There are several RF cancellation methods, that can be broadly categorized into passive RF cancellation and active RF cancellation. Some form of RF cancellation is generally necessary to avoid saturating the analog front-end of the receiver. Passive RF cancellation can be obtained by using, e.g., circulators, directional antennas, beamforming, polarization, or shielding [5]. Active RF cancellation is commonly implemented by transforming the transmitted RF signal appropriately to emulate the SI channel using analog components and subtracting the resulting SIC signal from the received SI signal [3]. Alternatively, an additional transmitter can be used to generate the SIC signal from the transmitted baseband samples.

However, a residual SI signal is typically still present at the receiver after RF cancellation has been performed. This residual SI signal can, in principle, be easily canceled in the digital domain, since it is caused by a known transmitted signal. Unfortunately, in practice, several transceiver non-linearities distort the SI signal. Some examples of non-linearities include baseband non-linearities (e.g., digital-to-analog converter (DAC) and analog-to-digital converter (ADC)) [6], IQ imbalance [6, 7], phase-noise [8, 9], and power amplifier (PA) non-linearities [6, 7, 10, 11]. These effects need to be taken into account using intricate polynomial models to cancel the SI to the level of the receiver noise floor. These polynomial models perform well in practice, but their implementation complexity grows rapidly with the maximum considered non-linearity order. Principal component analysis (PCA) is an effective complexity reduction technique that can identify the most significant non-linearity terms in a parallel Hammerstein model [11]. However, with PCA-based methods, the transmitted digital baseband samples need to be multiplied with a transformation matrix to generate the SIC signal, thus introducing additional complexity. Moreover, whenever the SI channel changes, the high-complexity PCA operation needs to be re-run. To the best of our knowledge, no hardware implementation of a polynomial SI canceller has been reported in the open literature to date. Only the work of [12] has made a step in this direction, since the authors considered quantization aspects of polynomial SI cancellers.

In the past few years, there has been renewed interest in the use of neural networks (NNs) to augment or replace a range of signal processing tasks in communications systems [13], [14], [15], [16], [17], [18]. NNs are particularly well-suited to tackle non-linear signal processing problems, where traditional model-based algorithms are unavailable or too complex for analytical treatment. However, NN-based solutions can also be used in cases where traditional model-based algorithms suffer from prohibitively high implementation complexity. For example, NNs have been used to successfully perform digital predistortion (DPD) in wireless systems [19], [20], non-linear leakage cancellation in FDD transceivers [21], as well as optical fiber non-linearity compensation [22]. NNs have also been used for non-linear SIC in full-duplex communications [23], [24], [25] and it was shown in [23] that they can achieve similar SIC performance with a state-of-the-art polynomial SIC model, but with much lower complexity.

The communications subsystems of embedded devices are
Contribution: In this work, we present a hardware implementation of the SIC method proposed in [23] to quantify and translate the computational complexity gains over the state-of-the-art polynomial based model of [11] into real-world hardware resource utilization gains. Contrary to [11], [23], we use a more realistic and well-defined measurement setup that results in a completely new and more challenging dataset with more non-linear content. Since, to the best of our knowledge, no polynomial SI canceller implementations have been reported in the literature, we also present a hardware architecture for a reference polynomial SI canceller. We note that this hardware architecture can also be used for other related applications such as digital predistortion and leakage cancellation in FDD transceivers. We provide FPGA and ASIC implementation results that clearly demonstrate the significant gains with respect to the polynomial SI canceller that can be achieved by an NN-based SI canceller in terms of resource utilization, throughput, and energy efficiency.

Outline: The remainder of this paper is organized as follows. Section III provides background on full-duplex communications and digital SIC using polynomial cancellers, while Section IV describes how SIC can be achieved using NNs. In Section V we describe our proposed NN-based SI canceller hardware architecture and, in Section VI we describe our proposed baseline polynomial-based SI canceller hardware architecture. In Section VII we compare the performance and the complexity of a conventional polynomial SI canceller with the NN-based SI cancellers. In Section VII we also provide FPGA and ASIC implementation results. Finally, Section VIII concludes this paper.

II. CONVENTIONAL DIGITAL SELF-INTERFERENCE CANCELLATION

Fig. 1 shows a block diagram of a full-duplex transceiver. On the transmitter side, the digital baseband samples $x[n] \in \mathbb{C}$, where $n$ is the sample index, are converted to an analog signal using a DAC, up-converted to a carrier frequency $f_c$ using an IQ mixer, amplified using a power amplifier (PA), and filtered using a bandpass (BP) filter. The transmitted signal leaks to the receiver through an SI channel $h_{SI}$ and is then filtered using a BP filter, amplified using an LNA, downconverted using an IQ mixer, and digitized using an ADC. The SI channel, $h_{SI}$, also models the passive RF SIC. An RF cancellation signal is subtracted from the received SI signal at some point before the LNA to avoid saturating the receiver. Since the transmitter and the receiver are co-located, they share a common local oscillator (LO) signal to minimize the effect of phase noise on the SI signal [9].

If we assume, for simplicity of exposition, that there is no signal-of-interest from a remote node and no thermal noise, then the received signal $y[n]$ in Fig. 1 consists only of the residual SI signal after RF SIC has been performed. We denote the received signal in this special case by $y_{SI}[n]$. The goal of digital SIC is to reproduce an accurate copy of $y_{SI}[n]$, denoted by $\hat{y}_{SI}[n]$, based on samples of the transmitted baseband signal $x[n]$. This signal is then subtracted from $y[n]$ so that the residual SI signal is $y_{SI}[n] - \hat{y}_{SI}[n]$. If $y_{SI}[n]$ is reconstructed perfectly, then the SI can be canceled entirely and $y_{SI}[n] - \hat{y}_{SI}[n] = 0$. In practice, as discussed previously, due to the presence of thermal noise and transceiver
non-linearities, perfect SIC is difficult to achieve. The SIC performance $C_{db}$ is typically evaluated as:

$$C_{db} = 10 \log_{10} \left( \frac{\sum_{n} |y_{SI}[n]|^2}{\sum_{n} |y_{SI}[n] - \hat{y}_{SI}[n]|^2} \right).$$  \hspace{1cm} (1)

A. Linear Self-Interference Cancellation

Linear SIC is the simplest form of SIC that ignores all non-linear effects of the various components in Fig. 1. The linear SIC signal is constructed as $\hat{y}_{SI}[n]$:

$$\hat{y}_{SI}[n] = \sum_{l=0}^{L-1} \hat{h}[l]x[n - l],$$  \hspace{1cm} (2)

where $\hat{h}[l] \in \mathbb{C}$, $l \in \{0, \ldots, L - 1\}$, models the SI channel, $h_{SI}$, and any other memory effect in the transceiver chain. The parameters $\hat{h}[l]$ can be obtained from training samples either in a one-shot fashion using standard least-squares (LS) estimation or adaptively using an iterative version of the LS estimation algorithm, such as least mean squares (LMS) or recursive least squares (RLS).

B. Polynomial Non-Linear Self-Interference Cancellation

Each active component in the transceiver model shown in Fig. 1 is generally a dynamic non-linear system. This means that linear cancellation alone is, in most cases, not accurate enough to cancel a sufficiently large fraction of the SI signal. It has been shown that the transmitter IQ imbalance and the PA non-linearities typically dominate all remaining non-linearities [10], [11]. This is true in particular when the transmitter and receiver chains use the same local oscillator signal for upconversion, as shown in Fig. 1, so that the effect of phase noise becomes negligible [9]. As such, the SIC signal $\hat{y}_{SI}[n]$ can be constructed as [10], [11]:

$$\hat{y}_{SI}[n] = \sum_{p=1}^{P} \sum_{q=0}^{L-1} \sum_{l=0}^{P-1} \hat{h}_{p,q}[l]x[n - l]^q x^n - l]^{p-q},$$  \hspace{1cm} (3)

where $\hat{h}_{p,q}[l] \in \mathbb{C}$ and only odd values for $p$ are considered because even harmonics typically lie out-of-band and are filtered out by the transmitter and receiver BP filters. The model in (3) is linear with respect to the parameters $\hat{h}_{p,q}[l]$, and therefore, similarly to linear SI estimation, the parameters $\hat{h}_{p,q}[l]$ can be estimated based on training samples using some variant of the LS estimation algorithm. The basis functions of the polynomial model in (3) are defined as:

$$BF_{p,q}(x) = x^p(x^*)^{p-q}. \hspace{1cm} (4)$$

The number of distinct basis functions in (3) is [11]:

$$N_{BF} = \frac{L}{4} (P + 1) (P + 3). \hspace{1cm} (5)$$

Using (4), the expression for $\hat{y}[n]$ in (3) can be re-written in a more compact form:

$$\hat{y}_{SI}[n] = \sum_{p=1}^{P} \sum_{q=0}^{L-1} \sum_{l=0}^{P-1} \hat{h}_{p,q}[l] BF_{p,q} (x[n - l]) .$$  \hspace{1cm} (6)

We note that linear cancellation is a special case of the polynomial model in (6) when only considering the single term for $p = 1$ and $q = 1$.

C. Computational Complexity

A multiplication between two complex numbers $x_1 = a + jb$ and $x_2 = c + jd$ can be performed in a straightforward manner as $x_1 x_2 = (ac - bd) + j(ad + bc)$. This requires two real-valued additions and four real-valued multiplications. However, it is also possible to first compute $s_1 = ac$, $s_2 = bd$, and $s_3 = (a + b)(c + d)$ so that $x_1 x_2 = (s_1 - s_2) + j(s_3 - s_1 - s_2)$. This requires five real-valued additions and three real-valued multiplications. Since hardware multipliers are typically significantly more complex than hardware adders, we assume the latter method is used to minimize the number of multipliers. Thus, it can directly be deduced from (2) that the total number of real-valued multiplications and additions that are required by the linear SI canceller is:

$$N_{ADD,lin} = 7L - 2, \hspace{1cm} (7)$$

$$N_{MUL,lin} = 3L. \hspace{1cm} (8)$$

Moreover, if we ignore the computation of the basis functions for simplicity the total number of real-valued multiplications and additions that are required by the polynomial SI canceller (which also includes the linear cancellation term) is [23]:

$$N_{ADD, poly} = \frac{7}{4} L (P + 1) (P + 3) - 2, \hspace{1cm} (9)$$

$$N_{MUL, poly} = \frac{3}{4} L (P + 1) (P + 3). \hspace{1cm} (10)$$

We note that the expression for $N_{ADD, poly}$ in our previous work [23] erroneously ignored the five real-valued additions that are required to implement each complex multiplication. As such, the actual complexity of the polynomial canceller is even higher than that reported in [23].

III. NEURAL NETWORK NON-LINEAR DIGITAL SELF-INTERFERENCE CANCELLATION

Polynomial SIC models such as (6) work well in practice but are often highly redundant in the sense that many of the $\hat{h}_{p,q}[l]$ parameters are very close to zero. NN-based SIC cancellers, on the other hand, can extract the essence of the non-linear structure of the SI signal from training data, which often significantly reduces the complexity of the SIC model [23]. A challenge when using NN cancellers is that the NN training process is inherently noisy due to the use of mini-batches for gradient estimation, which makes it difficult to achieve a very accurate reconstruction of the SI signal [25]. To overcome this problem, [23] used a NN to reconstruct only a particular part of the SI signal, while using conventional linear cancellation for the remainder of the SI. Specifically, in [23] the SI signal was conceptually decomposed into a linear component and a non-linear component:

$$y_{SI}[n] = y_{SI linear}[n] + y_{SI non}[n]. \hspace{1cm} (11)$$

1 We note that this simplification is justified in Section V.
The outputs of the first hidden layer neurons are given by:
\[
\hat{y}_{\text{SI,linear}}[n] = \sum_{l=0}^{L-1} \hat{h}[l] x[n-l].
\]  
(12)

The parameters \( \hat{h}[l] \) are obtained using LS estimation while considering the substantially weaker signal \( \hat{y}_{\text{SI,linear}}[n] \) as noise. The linear SIC signal is then subtracted from the SI signal to obtain:
\[
\hat{y}_{\text{SI,nl}}[n] \approx y_{\text{SI}}[n] - \hat{y}_{\text{SI,linear}}[n].
\]  
(13)

The task of the NN is limited to reconstructing \( \hat{y}_{\text{SI,nl}}[n] \) based on the appropriate \( x[n] \) samples.

As is common practice when training NNs, we normalize the input and output training samples so that \( x[n] \) and \( \hat{y}_{\text{SI,nl}}[n] \) have unit variance (i.e., the variance of the real part and the variance of the imaginary part are both equal to 0.5) and zero mean. To perform SIC on the test data, the output of the NN is denormalized using the mean and variance estimated based on the training data.

A. Neural Network Structure

Due to the universal approximation theorem [31], a feedforward NN with one hidden layer, as depicted in Fig. 2, is sufficient to reconstruct the non-linear SI signal. While the work of [23] only considered feedforward NNs with one hidden layer, it is possible to use any NN architecture to generate \( \hat{y}_{\text{SI,nl}}[n] \). In particular, [23] employed a deep feedforward NN and showed that using many layers with few neurons per layer can have significant computational complexity advantages with respect to a shallow NN SI canceller that uses a single layer with more neurons. In all cases and as shown in Fig. 2, the cancellation NNs have \( 2L \) input nodes, which correspond to the real and imaginary parts of the \( L \) delayed versions of \( x[n] \), and two output nodes, which correspond to the real and imaginary parts of the target \( \hat{y}_{\text{SI,nl}}[n] \) sample. In the following, we denote the number of hidden layers by \( N_l \) and the number of hidden nodes per layer \( N_h \). Let the vector \( l_0 \) contain the \( 2L \) inputs to the NN:
\[
l_0 = [\Re\{x[n]\} \ \Im\{x[n]\} \ldots \Re\{x[n-L+1]\} \ \Im\{x[n-L+1]\}]^T.
\]  
(14)

The outputs of the first hidden layer neurons are given by:
\[
l_1 = f_1 (W_1 l_0 + b_1),
\]  
(15)

where \( W_1 \) is an \( N_h \times 2L \) matrix containing the hidden layer weights, \( b_1 \) is an \( N_h \times 1 \) vector containing the hidden layer biases, and \( f_1(\cdot) \) is the (vectorized) non-linear activation function used in the first hidden layer. The outputs of the neurons in the hidden layers \( 1 < l \leq N_l \) are:
\[
l_{l+1} = f_{l} (W_l l_{l-1} + b_l),
\]  
(16)

where \( W_l \) is an \( N_h \times N_h \) matrix containing the hidden layer weights, \( b_l \) is an \( N_h \times 1 \) vector containing the hidden layer biases, and \( f_{l}(\cdot) \) is the (vectorized) non-linear activation function used in hidden layer \( l \). Finally, the outputs of the output layer neurons are given by:
\[
l_{N_l+1} = f_{N_l+1} (W_{N_l+1} l_{N_l} + b_{N_l+1}),
\]  
(17)

where \( W_{N_l+1} \) is a \( 2 \times N_h \) matrix containing the output layer weights, \( b_{N_l+1} \) is a \( 2 \times 1 \) vector containing the output layer biases, and \( f_{N_l+1}(\cdot) \) is the activation function used in the output layer. As can be seen in Fig. 2 for \( l_{N_l+1} \) we have:
\[
l_{N_l+1} = [\Re\{y_{\text{lin}}[n]\}] \ \Im\{y_{\text{lin}}[n]\}]^T.
\]  
(18)

The goal of the NN is to minimize the mean squared error between the expected NN output and the actual NN output:
\[
\text{MSE} = \frac{1}{N} \sum_{n=0}^{N-1} (\Re\{\hat{y}_{\text{SI,nl}}[n]\] - \Re\{\hat{y}_{\text{SI,nl}}[n]\}^T
\]  
+ \frac{1}{N} \sum_{n=0}^{N-1} (\Im\{\hat{y}_{\text{SI,nl}}[n]\] - \Im\{\hat{y}_{\text{SI,nl}}[n]\}^T,  
(19)

where \( N \) is the total number of training samples. The MSE in (19) is minimized by choosing appropriate values for \( W_l, b_l, l \in \{1, \ldots, N_l + 1\} \), using back-propagation [32].

B. Computational Complexity

Let us assume that the NN uses the popular ReLU activation function in the hidden layers (which has similar complexity to a real-valued addition (i.e., \( f_l = \text{ReLU}(x) = \max(0, x) \)), \( l \in \{1, \ldots, N_l\} \)) and a linear activation function in the output layer (i.e., \( f_{N_l+1}(x) = x \)). Then, the number of real-valued multiplications and additions that are required by an NN canceller with a single hidden layer and \( N_h \) hidden neurons is \( 2^3 \):
\[
N_{\text{ADD,NN}} = (2L + 3)N_h + 7L, \]  
(20)
\[
N_{\text{MUL,NN}} = (2L + 2)N_h + 3L, \]  
(21)

where the second term in both expressions comes from the linear SI canceller that is required for the NN SI canceller to work. Moreover, two additions are required to add the output of the linear SI canceller with the output of the NN canceller. For the more general NN described in [23] with \( N_l \) hidden layers with \( N_h \) neurons each, (20)-(21) can be generalized to:
\[
N_{\text{ADD,NN}} = (2L + 3 + (N_l - 1)(N_l + 1))N_h + 7L, \]  
(22)
\[
N_{\text{MUL,NN}} = (2L + 2 + (N_l - 1)N_h)N_h + 3L. \]  
(23)

We note that these two additions were not included in [23], but we include them here for the sake of accuracy.
IV. NEURAL NETWORK CANCELLER HARDWARE ARCHITECTURE

In this section, we describe a generic hardware architecture that can be used to implement both the shallow NN-based SI canceller of [23] and deeper NN-based SI cancellers such as the ones described in [25]. We first provide an overview of the architecture, which is followed by a more detailed explanation of each component. In Fig. 3, we show the high-level architecture of a general NN-based canceller. The set of baseband samples \( \{x[n], \ldots, x[n-L+1]\} \) is given as an input to a linear SI canceller and a NN-based SI canceller. These two SI cancellers operate in parallel to generate the linear and non-linear cancellation signals, respectively, which are then added (after the denormalization step for the NN) to produce the cancellation signal \( \hat{g}_{NN}[n] \).

A. Macro-Pipeline Architecture

As shown in the example of Fig. 4 in our architecture, the canceller NN layers are mapped to macro-pipeline stages. Each macro-pipeline stage requires several clock cycles to compute its outputs and it can start its computations as soon as valid outputs from the previous macro-pipeline stage become available. Due to the high-throughput requirements of the SIC task, we instantiate one macro-pipeline stage for each layer in the NN that is used for cancellation.

Let \( NE_l \) denote the number of neurons in layer \( l \). We note that \( NE_0 = 2L \), \( NE_{N_l+1} = 2 \), and \( NE_l = N_h \) for all hidden layers \( l \in \{1, \ldots, NE_l\} \). The goal of a macro-pipeline stage is to compute \( I_l \) using expressions of the form (15)-(17). Each element \( j \in \{0, \ldots, NE_l-1\} \) of \( I_l \) can be computed as:

\[
I_l[j] = f_l \left( b_l[j] + \sum_{i=0}^{NE_{l-1}-1} W_l[i,j]I_{l-1}[i] \right) .
\]

The architecture of each macro-pipeline stage is shown in more detail in Fig. 5. More specifically, each macro-pipeline stage contains an input interface, an array of \( N_{PE} \) processing elements (PEs), a weights-and-biases memory, a control unit, and an output interface. We note that for simplicity, all weights, biases, and partial sums have a common bit-width of \( Q \) bits and saturation is used in case of an overflow. More sophisticated quantization schemes are possible, but they are beyond the scope of this work.

The \( N_{PE} \) PEs, whose internal structure is shown in Fig. 6, can be used to compute (24) over multiple clock cycles using one of two possible schedules. In the neuron-by-neuron (NBN) schedule, neurons are processed sequentially and each of the \( N_{PE} \) PEs computes a part of the sum in (24) for a given neuron \( j \). In the input-by-input (IBI) schedule, the inputs of layer \( l \) (i.e., \( I_{l-1} \)) are processed sequentially and the \( N_{PE} \) PEs update the sum in (24) with the term \( W[i,j]I_{l-1}[i] \) for \( N_{PE} \) distinct neurons in parallel. As an NBN macro-pipeline stage generates neuron output values sequentially, the optimal accelerator structure consists of an NBN macro-pipeline stage always being followed by an IBI macro-pipeline stage, allowing the IBI stage to start performing computations once the output of the first neuron of the preceding NBN stage has been computed. Once all inputs have been processed by the IBI stage, it immediately outputs multiple values to the NBN stage which follows it. Having an NBN stage after another NBN stage means that the second NBN stage would have to wait for all outputs of the previous stage to be generated before any processing can take place, and having an IBI stage followed by another IBI stage would mean that the second IBI stage cannot start processing before the first IBI stage has processed all its inputs. This structure of NBN and IBI stages, connected in an alternating fashion, masks a significant part of the latency and reduces the number of interconnects between two consecutive macro-pipeline stages. Since the exact architecture of each macro-pipeline stage depends on the processing schedule, we describe the details of the corresponding architectures separately in the next two sections.

B. Neuron-by-Neuron Macro-Pipeline Architecture

1) Input Interface: The input interface consists of \( N_{PE} \) multiplexers, which route each of the \( NE_l-1 \) elements of \( I_{l-1} \) to the correct PE.

2) Processing Elements: In the NBN schedule, each PE is only associated with a single neuron, and therefore only a single partial sum needs to be stored in each PE. Thus, the PEs are simple multiply-and-accumulate (MAC) units and the memory shown in Fig. 6 is, in fact, a single \( Q \)-bit register.

3) Control Unit: The main tasks of the control unit are to distribute the computations to the PEs and to stall the computations when no valid inputs are available or when the following macro-pipeline stage is not ready to accept new inputs. The computations are dispatched to the PEs as follows. When \( N_{PE} \leq NE_{l-1} \), all \( N_{PE} \) PEs are used to process a single neuron at a time and \( \frac{NE_{l-1}}{N_{PE}} \) clock cycles are required to process all neurons. When \( N_{PE} > NE_{l-1} \), we constrain \( N_{PE} \) so that \( N_{PE} = k \cdot NE_{l-1}, \quad k \in \mathbb{N} \), and hence \( k \) neurons are
processed in parallel and \( \frac{\text{NE}_{l-1}}{\text{NE}_{l-1}} N_{\text{PE}} \) clock cycles are required to
process all neurons.

4) Weight and Bias Memories: The weight and bias mem-
ories for layer \( l \) are used to store \( W_l \) and \( b_l \) and they can be
written externally to re-configure the NN canceller. The weights are organized in a memory that is \( N_{\text{PE}} Q \) bits wide
so that all PEs can be provided with data in parallel. A single word of the weight memory contains \( N_{\text{PE}} \) weight values
per neuron. Thus the PEs are provided with data for \( k \) different neurons. The bias memory, on the other hand, has a-bit-width of \( k Q \) bits.

5) Output Interface: The output interface adds the partial
sums from the \( N_{\text{PE}} \) PEs using an adder tree, it adds the
weights and biases, and it applies the non-linear activation function \( f_l \) to each of the \( k \) neurons that are being processed
in parallel. A register is added between the PEs and the
output interface to reduce the critical path of the architecture.
Moreover, the output interface forwards the outputs of the
\( k \) neurons that are processed in parallel to the next macro-
pipeline stage.

6) Latency: In the remainder of this work, we select \( N_{\text{PE}} \)
carefully so that both \( \frac{\text{NE}_{l-1}}{\text{NE}_{l-1}} N_{\text{PE}} \) and \( \frac{\text{NE}_{l-1}}{\text{NE}_{l-1}} N_{\text{PE}} \) are integers. With
this setting, an NBN macro-pipeline stage requires
\[
L_l = \frac{\text{NE}_l \text{NE}_{l-1}}{N_{\text{PE}}} + 1,
\] (25)
clock cycles to produce all outputs of NN layer \( l \). However,
one full set of outputs for a NN layer is actually produced
every \( \frac{\text{NE}_l \text{NE}_{l-1}}{N_{\text{PE}}} \) clock cycles, so that the throughput of the NBN macro-pipeline stage in samples per clock cycle is
\[
T_l = \frac{N_{\text{PE}}}{\text{NE}_l \text{NE}_{l-1}}.
\] (26)
Moreover, the first \( k \) outputs of an NBN macro-pipeline stage
become available after
\[
L_{l, \text{first}} = \left[ \frac{\text{NE}_{l-1}}{N_{\text{PE}}} \right] + 1,
\] (27)
clock cycles. Therefore, a potential IBI macro-pipeline stage
that follows can already start its computations after the \( L_{l, \text{first}} \)
clock cycles and that only \( k \leq \text{NE}_l \) outputs need to be
forwarded to the next stage at a time.

C. Input-by-Input Macro-Pipeline Architecture

1) Input & Output Interfaces: The input and output inter-
faces of the IBI macro-pipeline stage are similar to that of the
NBN macro-pipeline stage. The main difference is that the IBI
output interface forwards the outputs of all \( \text{NE}_l \) neurons that
are processed in parallel to the next macro-pipeline stage.

2) Processing Elements: In the IBI schedule, each PE can be
associated with multiple neurons. Therefore, several partial
sums may need to be stored in each PE. Thus, the PEs are
MAC units and the memory shown in Fig. 6 has \( \frac{\text{NE}_l}{N_{\text{PE}}} \) \( Q \) bits.

3) Control Unit: In the IBI schedule, when \( N_{\text{PE}} \leq \text{NE}_l \),
all \( N_{\text{PE}} \) PEs are used to update the \( \text{NE}_l \) neurons of layer \( l \)
sequentially with a new input value \( I[i] \) and \( \text{NE}_{l-1} \) \( \frac{\text{NE}_l}{N_{\text{PE}}} \) clock cycles are required to process all neurons. When \( N_{\text{PE}} > \text{NE}_l \),
we constrain \( N_{\text{PE}} \) so that \( N_{\text{PE}} = k \text{NE}_l \), \( k \in \mathbb{N} \), and \( k \) inputs
are processed in parallel. Hence, \( \frac{\text{NE}_l \text{NE}_{l-1}}{N_{\text{PE}}} \) clock cycles are
required to process all neurons.

4) Weight and Bias Memories: The weight and bias mem-
ories are similar to those of the NBN macro-pipeline stage.
A single word of the weight memory contains \( N_{\text{PE}} \) weights
per neuron. The bias memory has a bit-width of \( \text{NE}_l Q \) bits in the IBI macro-pipeline stage. All
memories support external writes to re-configure the canceller.

5) Latency: Similarly to the NBN schedule, we choose \( N_{\text{PE}} \)
carefully so that both \( \frac{\text{NE}_l}{N_{\text{PE}}} \) and \( \frac{\text{NE}_{l-1}}{N_{\text{PE}}} \) are always integers.
Then, the latency and the throughput are
\[
L_l = \frac{\text{NE}_l \text{NE}_{l-1}}{N_{\text{PE}}} + 1,
\] (28)
clock cycles and
\[
T_l = \frac{N_{\text{PE}}}{\text{NE}_l \text{NE}_{l-1}},
\] (29)
samples per clock cycle, respectively. Moreover, since all
\( \text{NE}_l \) outputs of an IBI macro-pipeline stage become available
simultaneously, the number of clock cycles until the first
output is identical to \( L_l \) and also given by
\[
L_{l, \text{first}} = \frac{\text{NE}_l \text{NE}_{l-1}}{N_{\text{PE}}} + 1,
\] (30)
clock cycles.

D. Overall Neural Network Canceller Architecture

The overall NN architecture consists of \( N_l \) macro-pipeline
stages with pipeline registers added between them. The first
hidden layer uses an NBN macro-pipeline stage and the second
hidden layer (or the output layer when \( N_l = 1 \)) uses an
IBI macro-pipeline stage. Further layers use NBN and IBI
macro-pipeline stages in an alternating fashion as previously
discussed. The \( \text{NE}_0 = 2L \) inputs \( I_0 \) of the first NBN macro-
pipeline stage that implements the computations of the first

**Fig. 5. Block diagram of the macro-pipeline stage architecture [1].**

**Fig. 6. Detailed view of the PE architecture that is used by both the NBN and the IBI macro-pipeline stages [1].**
hidden layer are assumed to all be available in parallel. The number of PEs instantiated for layer \( l \) is denoted by \( N_{\text{PE},l} \). The computations for the linear canceller are done in parallel with the NN by instatiating a standard complex FIR filter with \( N_{\text{PE},\text{linear}} \) complex-valued PEs. The latency of the linear canceller in clock cycles

\[
\mathcal{L}_{\text{linear}} = \left[ \frac{L}{N_{\text{PE},\text{linear}}} \right].
\]  

(31)

Since the linear canceller is not pipelined, it holds that \( T_{\text{linear}} = \frac{1}{\mathcal{L}_{\text{linear}}} \). The throughput of the overall NN canceller architecture is:

\[
T = \min \left\{ T_{\text{linear}}, \min_{i \in \{1, \ldots, N_l+1\}} T_i \right\}.
\]  

(32)

Since it is typically not very costly in terms of resources to ensure that \( T_{\text{linear}} \geq T_i, \ i \in \{1, \ldots, N_l+1\} \), in practice \( T \) is usually limited by \( \min_i T_i \). As opposed to the throughput, the latency of the overall NN canceller is more complicated to derive in general. However, in the special case where the number of PEs for each layer \( l \) is chosen such that no stalling happens and \( N_l + 1 \) is even, the latency can be calculated as:

\[
\mathcal{L} = \max \left\{ \mathcal{L}_{\text{linear}}, \sum_{i=1}^{(N_l+1)/2} \left( \mathcal{L}_{2i-1,\text{first}} + \mathcal{L}_{2i} \right) \right\},
\]  

(33)

where the odd-indexed terms in the summation correspond to NBN macro-pipeline stages and the even terms correspond to IBI macro-pipeline stages. Finally, we note that the denormalization step shown in Fig. 3 is constrained to scaling with powers of two, which can be implemented efficiently with simple shifting operations, both during training and during inference.

V. POLYNOMIAL CANCELLER HARDWARE ARCHITECTURE

Since, to the best of our knowledge, there are no published implementations of polynomial SI cancellers in the literature, we provide our own optimized reference implementation. Our polynomial SI canceller architecture, which is shown in Fig. 7, is largely based on the NN architecture since the main computational tasks of the two cancellers are very similar (i.e., computation of weighted sums). The main differences are that the input interface also computes the basis functions, that \( N_{\text{CPE}} \) complex PEs (CPEs) are used to perform computations on complex values, and that there is only a single macro-pipeline stage. In the remainder of this section, we explain how the basis functions can be computed efficiently and we describe the polynomial SI canceller in more detail.

---

Algorithm 1 Dynamic programming computation of basis functions \( BF_{p,q}(x[n]) \)

1: \textbf{Input:} \( x[n] \)
2: \textbf{Outputs:} \( BF_{p,q}(x[n]) \) for \( p \in \{1,3,\ldots,P\}, \ q \in \{0,\ldots,p\} \)
3: \( BF_{0,0}(x[n]) \leftarrow (x[n])^* \)
4: \( BF_{1,0}(x[n]) \leftarrow x[n] \)
5: \textbf{for} \( p \in \{2,3,\ldots,P\} \) \textbf{do}
6: \textbf{for} \( q \in \{1,2,\ldots,p\} \) \textbf{do}
7: \( BF_{p,q}(x[n]) \leftarrow x[n]BF_{p-2,q-2}(x[n]) \)
8: \textbf{end for}
9: \textbf{end for}

A. Basis Function Computation

The computation of the \( N_{\text{BF}} \) basis functions in (4) for each cancellation sample seems like a cumbersome task. Fortunately, we can show that the basis functions have a number of properties that enable their efficient computation. First, significant basis function re-use is possible. In particular, after \( \hat{y}_{SI}[n-1] \) has been computed based on \( BF_{p,q}(x[n-1-l]), \ l \in \{0,\ldots,L-1\}, \ p \in \{1,3,\ldots,P\}, \ q \in \{0,\ldots,p\} \), the basis functions for \( l \in \{0,\ldots,L-2\} \) can be stored and re-used for the computation of \( \hat{y}_{SI}[n] \). As such, the only new basis functions that need to be computed for \( \hat{y}_{SI}[n] \) are \( BF_{p,q}(x[n]), \ p \in \{1,3,\ldots,P\}, \ q \in \{0,\ldots,p\} \). This requires \( \frac{L-1}{4}(P+1)(P+3) \) memory elements, but reduces the number of basis functions that need to be computed by a factor of \( L \) from \( \frac{L}{4}(P+1)(P+3) \) to \( \frac{1}{4}(P+1)(P+3) \). Moreover, the following proposition shows two additional properties of the basis functions.

**Proposition 1:** For the basis functions in (4), it holds that:

1) \( BF_{p,q}(x) = (BF_{p-p,q-2}(x))^* \)
2) \( BF_{p,q}(x) = x^qBF_{p-2,q-2}(x) \)

**Proof:** Both properties follow from the definition of the basis function in (4). Specifically, for 1) we have:

\[
BF_{p,q}(x) = x^q(x^*)^{p-q} = (x^{p-q}(x^*)^{p-(p-q)})^* = (BF_{p-p,q}(x))^*,
\]

and for 2) we have:

\[
BF_{p,q}(x) = x^q(x^*)^{p-q} = x^{2q-2}(x^*)^{p-2-(q-2)} = x^{2q}BF_{p-2,q-2}(x).
\]

Property 1) enables a computation reduction by a factor of two since for every \( p \in \{1,3,\ldots,P\} \), it is sufficient to compute \( BF_{p,q}(x) \) only for \( q \in \{1,2,\ldots,p\} \) and the remaining basis functions for \( q \in \{0,\ldots,p-1\} \) can be obtained by simple conjugation. Moreover, property 2) reveals an efficient dynamic programming (DP) method to compute the basis functions for \( x[n] \), which is shown in Algorithm 1. Algorithm 1 requires one multiplication to pre-compute \( (x[n])^2 \) and \( \frac{1}{4}(P+1)(P+3)-2 \) multiplications for all executions of line 7. The conjugation in line 8 does not require any multiplications as it is a simple sign change of the imaginary part of.
\( \text{BF}_{p,q}(x) \). As such, the total number of multiplications to compute the basis functions for a baseband sample \( x[n] \) is:

\[
N_{\text{MUL,BF}} = \frac{1}{8} (P + 1)(P + 3) - 1. \tag{36}
\]

One downside of the DP approach is that only the inner loop in Algorithm 1 can be parallelized. However, in most typical applications we have \( P \leq 9 \), so that the outer loop in Algorithm 1 is executed very few times. We note that, due to the efficiency of Algorithm 1, \( N_{\text{MUL,BF}} \) is significantly smaller than \( N_{\text{MUL,poly}} \), which justifies ignoring the multiplications of the basis function computations in (10) for simplicity.

### B. Polynomial Canceller Architecture

We use a high-level structure that is similar to the NN-based cancellers in Fig. 3 in the sense that linear cancellation is done in parallel to non-linear cancellation and the polynomial SI canceller focuses only on the non-linear part of the SI signal. Since most of the SI signal is linear, removing the linear term separately significantly reduces the dynamic range of the values within the polynomial SI canceller, which in turn allows us to reduce the common quantization bit-width \( Q \) for the real and the imaginary parts of the involved quantities.

1) **Input & Output Interfaces:** The input interface consists of \( N_{\text{CPE}} \) multiplexers, which route each of the \( N_{\text{BF}} \) BFs to the correct CPE to compute parts of the sum in (36). As mentioned previously, the input interface also computes the BFs using \( N_{\text{CPE,BF}} \) CPEs. Since only the inner loop in Algorithm 1 can be parallelized, it is reasonable to constrain \( N_{\text{CPE,BF}} \) so that:

\[
N_{\text{CPE,BF}} \leq P + \frac{3}{2}. \tag{37}
\]

The number of clock cycles to compute all new BFs based on \( x[n] \) with \( N_{\text{CPE,BF}} \) PEs is:

\[
L_{\text{BF,new}} = 1 + \sum_{p=3}^{P} \frac{p + 1}{2N_{\text{CPE,BF}}},
\]

where one clock cycle is used to pre-compute \( x^2 \) and the result (as well as \( x^4 \)) are stored in two \( 2Q \)-bit registers. The \( \frac{p+1}{2} \) \((P + 1)(P + 3)\) BFs that are re-used are stored in a circular buffer. The output interface consists of an adder tree for the partial sums stored in the \( N_{\text{CPE}} \) CPEs to produce the final result.

2) **Complex Processing Elements:** The \( N_{\text{CPE}} \) CPEs are complex MAC units with a \( Q \)-bit register to store partial sums. The complex MAC units are implemented using three real-valued multipliers and five real-valued adders.

3) **Control Unit:** Similarly to the NN-based canceller, the main tasks of the control unit are to distribute the computations to the CPEs and to stall the computations when no valid inputs are available. The control unit schedules the operation so that the CPEs first compute the terms of (6) that are based on BFs that are already available in the circular buffer. In the meantime, the input interface computes the \( \frac{1}{2} (P + 1)(P + 3) \) BFs that depend on the new sample \( x[n] \).

4) **Parameter Memory:** The parameter memory is used to store the complex-valued \( \hat{h}_{p,q} \) parameters of the polynomial canceller. The memory contains \( \frac{N_{\text{BF}}}{N_{\text{CPE}}} \) words that are \( 2QN_{\text{CPE}} \) bits wide so that all \( N_{\text{CPE}} \) CPEs can be provided with the parameters in parallel. The parameter memory can be written to externally to re-configure the polynomial canceller.

5) **Latency:** The terms of (6) that are based on BFs and are available in the circular buffer can be computed in parallel to the computation of the new BFs that are based on \( x[n] \), masking a part of the latency of the computation of (6) or the new BFs (whichever is greater). The latency of computing the terms of (6) for the BFs available in the circular buffer is:

\[
L_{\text{BF,old}} = \left[ \frac{L - 1}{L} \right] \frac{N_{\text{BF}}}{N_{\text{CPE}}}.
\]

Then, it can be shown that the overall latency of the polynomial canceller is given by:

\[
L_{\text{poly}} = \begin{cases} 
\left[ \frac{N_{\text{BF}}}{N_{\text{CPE}}} \right] + 1, & L_{\text{BF,old}} \geq L_{\text{BF,new}}, \\
L_{\text{BF,new}} + \left[ \frac{1}{L} \frac{N_{\text{BF}}}{N_{\text{CPE}}} \right] + 1, & L_{\text{BF,old}} < L_{\text{BF,new}},
\end{cases}
\]

where one clock cycle is required by the adder tree in the output interface to produce the final output. Since a pipeline register is inserted before the adder tree of the output interface, the throughput of the polynomial SI canceller, measured in samples per clock cycle, is given by:

\[
T_{\text{poly}} = \frac{1}{L_{\text{poly}} - 1}. \tag{40}
\]

### VI. SELF-INTERFERENCE CANCELLATION RESULTS

In this section, we compare the polynomial SI canceller with the NN-based SI cancellers in terms of their SIC performance and their complexity. To this end, we first describe our full-duplex testbed and the employed dataset in detail. Then, we provide a high-level performance and complexity comparison of the polynomial SI canceller with the NN SI canceller.

A. **Full-Duplex Testbed**

A picture of our full-duplex testbed is shown in Fig. 8. Our full-duplex testbed that is used to generate the dataset in
this section is based on the National Instruments PXI platform [33] with a National Instruments NI-5791 RF card [34]. The NI-5791 RF card is used for both transmission and reception. The transmitter and the receiver are configured to use the same local RF oscillator for up-conversion and down-conversion, respectively. The built-in IQ imbalance compensation is disabled to be consistent with commercial off-the-shelf transceivers. The NI-5791 RF card uses a 16-bit Texas Instruments DAC3482 DAC [35] and a 14-bit Texas Instruments ADS4246 ADC [36]. As the NI-5791 RF card has a relatively low maximum output power of 10 dBm, we use an external Skyworks SE2576L PA [37]. We use a MECA CS-2.500 circulator [38] to provide approximately 15 dB of isolation between the transmitter and the receiver. Since we do not have access to an active RF canceller, we emulate the active RF cancellation using a 50 dB attenuator before the receiver input of the NI-5791 RF card. We note that this is a feasible amount of active RF cancellation, which even the very first RF cancellers were able to achieve [4]. The model number, gain, and noise figure of the receiver LNA are not stated explicitly in [34], but the overall receiver noise figure is guaranteed to be less than 8 dB at a frequency of 2 GHz.

B. Full-Duplex Dataset

The transmitted signal is a 20 MHz QPSK-modulated OFDM signal with 2048 carriers and a peak-to-average power ratio (PAPR) of 13 dB. The output power of the NI-5791 RF card is experimentally set so that the Skyworks SE2576L PA operates at its 1 dB compression point, namely at an output power of approximately 32 dBm [37]. The RF carrier frequency is set to 2.45 GHz and the sampling rate of the receiver is set to 80 MHz so that we oversample the OFDM signal by a factor of 4. The dataset contains 20,480 time-domain SI baseband samples, out of which 90% is used for training and 10% for the evaluation of the SIC performance. For NN training, we use a mini-batch size of $B = 32$ and the Adam optimizer [39] with a learning rate of $\lambda = 0.004$.

One important issue is to ensure that our dataset is not obtained in a regime where we are limited by transmitter or receiver quantization noise. The 16-bit DAC has a dynamic range of approximately $96$ dBm, which puts the transmitter quantization noise at approximately $-64$ dBm for a $32$ dBm transmit power. The $65$ dB of total isolation between the transmitter and the receiver attenuates all components of the signal equally. Thus, the transmitter quantization noise power at the receiver is approximately $-129$ dBm, which is well below the $-95$ dBm thermal noise power (25 $^\circ$C, 80 MHz bandwidth). The power at the LNA input is $-45.6$ dBm and the reference level of the receiver is set at its lowest supported value of $-27$ dBm. The 14-bit DAC has a dynamic range of approximately $84$ dBm. As such, the receiver quantization noise floor is located at approximately $-111$ dBm, which is also well below the thermal noise power.

C. Comparison Setup

The complexity expressions for the polynomial SI canceller in (9)–(10) and the NN SI cancellers in (22)–(23) cannot be compared directly because they contain different sets of parameters and they have different SIC performance. Thus, we choose to compare two pairs of points in the design space of the polynomial and the NN cancellers:

1) A pair of points where the polynomial and the NN cancellers achieve their maximum respective SIC performance (peak-performance).

2) A pair of points where the polynomial and the NN cancellers have approximately the same SIC performance (equi-performance).

The comparison points are selected as follows. First, we evaluate the SIC performance of the polynomial canceller for various combinations of $L$ and $P$. Then, we find the maximum SIC performance $C_{\text{max, poly}}$ and we select the combination of $L$ and $P$ that results in the smallest number of multiplications according to (10) and has SIC performance at most $1$ dB lower than the maximum SIC performance. The back-off of $1$ dB is allowed because as $L$ and $P$ are increased there are severely diminishing returns in terms of the SIC performance and we want to ensure that a reasonable complexity-performance trade-off point is selected to be fair to the polynomial canceller. This gives the peak-performance point for the polynomial canceller. For the peak-performance point of the NN canceller, we follow the same procedure for various values of $L$, $N_k$, and $N_l$ and using (23) for the complexity evaluation. For the equi-performance point of the NN canceller, we select the NN with the smallest number of multiplications that achieves SIC performance greater than or equal to $C_{\text{max, poly}}$.

In Fig. 9, we show two heatmaps for the SIC performance and the number of multiplications for the polynomial canceller.

![Fig. 9. SIC performance and number of multiplications for the polynomial canceller as a function of the channel length $L$ and the maximum power $P$. The selected canceller with $L = 3$ and $P = 7$ is marked with yellow circles.](image-url)
with \( L \in \{2, 3, \ldots, 10\} \) and \( P \in \{3, 5, 7, 9\} \). As shown in Fig. 9b, there is only a marginal difference in performance between the different polynomial cancellers, whereas the complexity quickly grows, as shown in Fig. 9b. The maximum achievable SIC is 31.3 dB and the lowest complexity model that comes within 1 dB of this maximum uses \( L = 3 \) and \( P = 7 \) and achieves a SIC of 30.5 dB (shown in Fig. 9b with a circle). In Fig. 10, we show two heatmaps for the SIC performance and the number of multiplications for NN cancellers with \( L \in \{2, 4, \ldots, 10\} \), \( N_h \in \{6, 8, \ldots, 40\} \), and \( N_I = 1 \), which were trained for 50 epochs. We note that we also explored several architectures of deeper NNs (i.e., \( N_I > 1 \)), but the shallow NN always achieved the same SIC performance with lower complexity. The equi-performance NN has \( L = 2, N_h = 8 \), and achieves a SIC of 32.3 dB (shown in Fig. 10 with yellow circles). The peak-performance NN has \( L = 4, N_h = 34 \), and a SIC performance 37.6 dB (shown in Fig. 10 with black circles). We summarize the above selection in Table I, where we also show the complexity of the SI cancellers in terms of the number of real-valued multiplications and additions given by (9)-(10) and (22)-(23).

| Cancellation (dB) | Polynomial | Equi NN | Peak NN |
|-------------------|------------|---------|---------|
| \( L \)           | 3          | 2       | 4       |
| \( P \)           | 7          | n/a     | n/a     |
| \( N_0 \)         | n/a        | 1       | 1       |
| \( N_h \)         | n/a        | 8       | 34      |
| Real Add.         | 418        | 82      | 428     |
| Real Mult.        | 180        | 60      | 364     |

![Fig. 10. SIC performance and number of multiplications for the NN canceller as a function of the channel length \( L \) and the number of neurons \( N_h \) with \( N_I = 1 \). The equi-performance NN canceller with \( L = 2 \) and \( N_h = 8 \) and the peak-performance NN canceller with \( L = 4 \) and \( N_h = 34 \) are marked with yellow and black circles, respectively.](image)

Fig. 11. Comparison of the SIC performance of polynomial and NN-based cancellers. The pre-digital-cancellation SI signal and the receiver thermal noise floor are also shown for comparison. Active RF cancellation is emulated using a 50 dB attenuator at the receiver.

D. Self-Interference Cancellation Performance Comparison

In Fig. 11, we show the power spectral density (PSD) of the received SI signal \( y_s[n] \) before any SIC is performed, the PSD of the received signal when no transmission takes place (i.e., the effective noise floor of the receiver), as well as the PSDs of the SI signals after linear SIC and non-linear SIC with the polynomial and NN-based cancellers shown in Table I. We observe that using the polynomial canceller or the equi-performance NN canceller results in a residual SI signal that is approximately 9 dB above the receiver noise floor. While both cancellers achieve the same SIC performance, the PSDs of the residual SI signals are significantly different. In particular, the polynomial canceller does not model and, hence, can not cancel the carrier leakage around the DC tone, but it achieves a better SIC performance for the remaining in-band signal than the equi-performance NN canceller. The peak-performance NN canceller, on the other hand, can cancel the SI down to approximately 2.5 dB from the receiver noise floor. This clearly shows that there are non-linear effects that cannot be modeled adequately by the polynomial canceller.

In Fig. 12, we show the training convergence behavior for the non-linear cancellation part of the two NN cancellers. The linear cancellation is in both cases approximately 19 dB, making the non-linear SIC directly comparable. We observe that the equi-performance NN achieves its maximum performance on the test set after 9 epochs, while the peak-performance NN requires more than 20 epochs to achieve its maximum performance on the test set. Moreover, we observe that both...
NN cancellers have similar performance on the training and test sets, meaning that there are no obvious overfitting issues. We note that in this work, we focus on the complexity of the inference part for both the polynomial canceller and the NN-based cancellers. However, the complexity of the training part is an important issue that should also be carefully considered, even though training is typically required much less often than inference.

VII. HARDWARE IMPLEMENTATION RESULTS

In this section, we present a comparison of FPGA and ASIC implementation results for the polynomial SI canceller and the NN-based SI cancellers.

A. Comparison Setup

To perform a meaningful comparison of FPGA and ASIC implementation results, the quantization bit-width $Q$ for the different cancellers needs to be selected to individually minimize the implementation complexity while keeping the performance of the SI cancellers as close as possible to their floating-point equivalents. In Fig. 12, we show the cancellation performance for the polynomial SI canceller and the NN SI cancellers as a function of the quantization bit-width $Q$. We observe that both NN SI cancellers generally require a lower quantization bit-width $Q$ compared to the polynomial SI canceller to achieve SIC performance comparable to the floating-point performance.

Moreover, for the hardware implementation results presented in this section, we choose $Q = 16$ for the equi-performance NN canceller, $Q = 18$ for the peak-performance NN canceller, and $Q = 25$ for the polynomial SI canceller, as this choice leads to effectively identical SIC performance as the corresponding floating-point implementations for all cancellers. We note that the peak performance NN SI canceller requires one additional integer bit compared to the equi-performance NN SI canceller, due to larger absolute output values in the hidden layer. For the equi-performance NN canceller, we set $N_{PE,1} = 8$ and $N_{PE,2} = 4$ so that $T_1 = T_2 = 1/4$. With this setting, the macro-pipeline is perfectly balanced and one SI cancellation sample is produced every 4 clock cycles.

Furthermore, $N_{CPE, linear} = 1$ CPEs are instantiated for the NN SI canceller to ensure that the linear cancellation step can be completed in the same number of cycles. For the peak-performance NN canceller, we set $N_{PE} = 40$ for the hidden layer and $N_{PE} = 10$ for the output layer so that the throughput for both layers is $T = 1/7$. Again, we use $N_{CPE, linear} = 1$ for the linear canceller. The equi-performance NN canceller thus requires a total of 12 PEs and the peak-performance NN canceller requires a total 50 PEs, and both require only 1 CPE for the linear canceller. Finally, for the polynomial canceller, we use $N_{CPE} = 10$ complex PEs. We use relatively high parallelization because our cancellers need to achieve a throughput at least equal to the 80 Msamples/s sampling frequency that is used in our dataset.

B. FPGA Implementation Results

In Table II, we show place-and-route (PAR) results on a Xilinx Virtex-7 XC7VX485 (speed grade -2) FPGA, which contains a total of 75.9k slices, 303.6k LUTs, 607.2k flip-flops, and 2.8k DSP slices. A clock frequency target of 100 MHz is used for all cancellers.

We observe that the equi-performance NN canceller has the smallest resource utilization of all considered cancellers, while the peak-performance NN canceller has a similar resource utilization to the polynomial canceller, while providing approximately 7 dB better SIC performance. Moreover, the equi-performance NN canceller and the peak-performance NN canceller have a 95% and 5% higher throughput than the polynomial SI canceller. However, when implemented on an FPGA, none of the considered SI cancellers can achieve the 80 Msamples/s throughput that is required by the considered application.

C. ASIC Implementation Results

In Table III, we present ASIC implementation results for the polynomial SI canceller and the two NN SI cancellers using a 28 nm FD-SOI technology. We use typical-typical corners, a
0.9 V operating voltage, and a 25°C operating temperature. The polynomial canceller and the peak-performance canceller were synthesized, placed, and routed for a target frequency of 400 MHz and 1 GHz, respectively. However, for the power results, all cancellers are operated at a frequency that results in a throughput of exactly 80 Msamples/s, i.e., 560 MHz for the polynomial canceller and the peak-performance NN canceller, and 320 MHz for the equi-performance NN canceller. Moreover, post-PAR simulations are used both to verify the design and to accurately estimate the switching activity.

We observe that the equi-performance NN canceller requires a significant 8.1× less area and 7.7× less power than the polynomial canceller. We note that the absolute latency of the equi-performance NN canceller is 0.9 ns higher than the polynomial canceller and requires slightly more (1.3×) power. However, it should be noted that the peak-performance NN canceller also has an approximately 7 dB better SIC performance than the polynomial canceller.

VIII. CONCLUSION

In this paper, we presented a high-throughput hardware architecture for an NN-based SIC scheme for full-duplex radios. We also presented, to the best of our knowledge, the first efficient hardware architecture for polynomial SIC in the literature, which we used as a comparison baseline for the NN-based SI cancellers. Our implementation results show that the NN SI cancellers have significantly lower computational complexity than a conventional polynomial SI canceller, which translates into substantial area and energy savings when the schemes are implemented in hardware. Specifically, for the same SIC performance, an ASIC implementation of a NN-based SI canceller has up to 8.1× and 7.7× better hardware efficiency and energy efficiency when compared to a conventional polynomial SI canceller.

REFERENCES

[1] Y. Kurzo, A. Burg, and A. Balatsoukas-Stimming, “Design and implementation of a neural network aided self-interference cancellation scheme for full-duplex radios,” in Asilomar Conf. on Signals, Systems and Computers, Oct. 2018, pp. 589–593.

[2] M. Jain, J. I. Choi, T. Kim, D. Bharadia, S. Seth, K. Srinivasan, P. Levis, S. Katti, and P. Sinha, “Practical, real-time, full duplex wireless,” in Int. Conf. on Mobile Computing and Networking, ACM, 2011, pp. 301–312.

[3] M. Duarte, C. Dick, and A. Sabharwal, “Experiment-driven characterization of full-duplex wireless systems,” in IEEE Trans. Wireless Commun., vol. 11, no. 12, Dec. 2012, pp. 4296–4307.

[4] D. Bharadia, E. McMilin, and S. Katti, “Full duplex radios,” in ACM SIGCOMM, 2013, pp. 375–386.

[5] E. Everett, A. Sahai, and A. Sabharwal, “Passive self-interference suppression for full-duplex infrastructure nodes,” IEEE Trans. Wireless Commun., vol. 13, no. 2, pp. 680–694, Feb. 2014.

[6] A. Balatsoukas-Stimming, A. C. M. Austin, P. Belanovic, and A. Burg., “Baseband and RF hardware impairments in full-duplex wireless systems: experimental characterisation and suppression,” EURASIP J. on Wireless Commun. and Netw., vol. 2015, no. 142, 2015.

[7] D. Korpi, L. Anttila, V. Syrjala, and M. Valkama, “Wideband digital self-interference cancellation in direct-conversion full-duplex transceivers,” IEEE J. Sel. Areas Commun., vol. 32, no. 9, pp. 1674–1687, Sep. 2014.

[8] A. Sahai, G. Patel, C. Dick, and A. Sabharwal, “On the impact of phase noise on active cancelation in wireless full-duplex,” IEEE Trans. Veh. Technol., vol. 62, no. 9, pp. 4494–4510, Nov. 2013.

[9] V. Syrjala, M. Valkama, L. Anttila, T. Riihonen, and D. Korpi, “Analysis of oscillator phase-noise effects on self-interference cancellation in full-duplex OFDM radio transceivers,” IEEE Trans. Wireless Commun., vol. 13, no. 6, pp. 2977–2990, June 2014.

[10] L. Anttila, D. Korpi, E. Antonio-Rodriguez, R. Wichman, and M. Valkama, “Modeling and efficient cancellation of nonlinear self-interference in MIMO full-duplex transceivers,” in IEEE Globecom Workshops, 2014, pp. 777–783.

[11] D. Korpi, L. Anttila, and M. Valkama, “Nonlinear self-interference cancellation in MIMO full-duplex transceivers under crosstalk,” EURASIP J. on Wireless Commun. and Netw., vol. 2017, no. 1, p. 24, Feb. 2017.

[12] P. P. Campo, D. Korpi, L. Anttila, and M. Valkama, “Nonlinear digital cancellation in full-duplex devices using spline-based Hammerstein model,” in IEEE Globecom Workshops, Dec. 2018.

[13] T. O’Shea and J. Hoydus, “An introduction to deep learning for the physical layer,” IEEE Trans. Cogn. Commun. and Networking, vol. 3, no. 4, pp. 563–575, Dec. 2017.

[14] T. Wang, C. Wen, H. Wang, F. Gao, T. Jiang, and S. Jin, “Deep learning for wireless physical layer: Opportunities and challenges,” China Communications, vol. 14, no. 11, pp. 92–111, Nov. 2017.

[15] Q. Mao, F. Hu, and Q. Hao, “Deep learning for intelligent wireless networks: A comprehensive survey,” IEEE Comm. Surveys Tutorials, vol. 20, no. 4, pp. 2595–2621, Fourth Quarter 2018.

[16] D. Gunduz, P. de Kerret, N. D. Sidiropoulos, D. Gesbert, C. Murthy, and M. van der Schara, “Machine learning in the air,” Apr. 2019. [Online]. Available: https://arxiv.org/abs/1904.12385

[17] Z. Qin, H. Ye, G. Y. Li, and B.-H. F. Juang, “Deep learning in physical layer communications,” IEEE Wireless Commun., vol. 26, no. 2, Apr. 2019.

[18] A. Balatsoukas-Stimming and C. Studer, “Deep unfolding for communications systems: A survey and some new directions,” in IEEE Workshop on Sig. Proc. Systems (SiPS), Oct. 2019.

[19] C. Tarver, L. Jiang, A. Sezifit, and J. Cavallaro, “Neural network DPD
via backpropagation through a neural network model of the PA," in Asilomar Conf. on Signals, Systems and Computers, Nov. 2019.

[20] R. Hongyo, Y. Egashira, T. M. Hone, and K. Yamaguchi, “Deep neural network-based digital predistorter for Doherty power amplifiers,” IEEE Microwave and Wireless Comp. Letters, vol. 29, no. 2, pp. 146–148, Feb. 2019.

[21] O. Ploder, O. Lang, T. Paireder, and M. Huemer, “An adaptive machine learning-based approach for the cancellation of second-order-intermodulation distortions in 4G/5G transceivers,” in IEEE Vehicular Technology Conf. (VTC2019-Fall), Sep. 2019.

[22] C. Häger and H. D. Pfister, “Nonlinear interference mitigation via deep neural networks,” in Optical Fiber Commun. Conf. and Exposition (OFC), Mar. 2018, pp. 1–3.

[23] A. Balatsoukas-Stimming, “Non-linear digital self-interference cancellation for in-band full-duplex radios using neural networks,” in IEEE Int. Workshop on Signal Proc. Advances in Wireless Commun. (SPAWC), Jun. 2018, pp. 1–5.

[24] H. Guo, J. Xu, S. Zhu, and S. Wu, “Realtime software defined self-interference cancellation based on machine learning for in-band full-duplex wireless communications,” in Int. Conf. on Computing, Networking and Commun. (ICNC), Mar. 2018, pp. 779–783.

[25] A. T. Kristensen, A. Burg, and A. Balatsoukas-Stimming, “Advanced machine learning techniques for self-interference cancellation in full-duplex radios,” in Asilomar Conf. on Signals, Systems and Computers, Nov. 2019.

[26] C. Zhang, P. Li, G. Sun, Y. Guan, B. Xiao, and J. Cong, “Optimizing FPGA-based accelerator design for deep convolutional neural networks,” in ACM/SIGDA Int. Symp. on Field-Programmable Gate Arrays, Feb. 2015, pp. 161–170.

[27] Y. Chen, T. Krishna, J. S. Emer, and V. Sze, “Eyeiss: An energy-efficient reconfigurable accelerator for deep convolutional neural networks,” IEEE J. of Solid-State Circuits, vol. 52, no. 1, pp. 127–138, Jan. 2017.

[28] F. A. Aoudia and J. Hoydis, “Towards hardware implementation of neural network-based communication algorithms,” in IEEE Int. Workshop on Signal Proc. Advances in Wireless Commun. (SPAWC), Jul. 2019.

[29] I. Wodiany and A. Pop, “Low-precision neural network decoding of polar codes,” in IEEE Int. Workshop on Signal Proc. Advances in Wireless Commun. (SPAWC), Sep. 2019.

[30] C. Tarver, A. Balatsoukas-Stimming, and J. Cavallaro, “Design and implementation of a neural network based predistorter for enhanced mobile broadband,” in IEEE Int. Workshop on Signal Processing Systems (SPS), Oct. 2019.

[31] K. Hörnli, “Approximation capabilities of multilayer feedforward networks,” Neural Networks, vol. 4, no. 2, pp. 251–257, 1991.

[32] D. E. Rumelhart, G. E. Hinton, and R. J. Williams, “Learning representations by back-propagating errors,” Nature, vol. 323, pp. 533–536, Oct. 1986.

[33] “National Instruments PXI Systems.” [Online]. Available: https://www.ni.com/ni-pxi

[34] “National Instruments NI-5791 RF Adapter Module for FlexRIO.” [Online]. Available: https://www.ni.com/ni-pxi

[35] “Texas Instruments DAC3482 Dual-Channel, 16-Bit, 1.25-GSPS, 1x-16x Interpolating Digital-to-Analog Converter (DAC).” [Online]. Available: http://www.ti.com/product/DAC3482

[36] “Texas Instruments ADS4246 Dual-Channel, 16-Bit, 160-MSPS Analog-to-Digital Converter (ADC).” [Online]. Available: http://www.ti.com/product/ADS4246

[37] “Skyworks SE2576L.” [Online]. Available: https://www.skyworksinc.com/en/products/amplifiers/SE2576L

[38] “MECA CS-2.500.” [Online]. Available: http://www.e-meca.com/Circulator:cs-2-500

[39] D. P. Kingma and J. Ba, “Adam: A method for stochastic optimization,” in Int. Conf. for Learning Representations (ICLR), May 2015.

Yann Kurzo received the B.Sc. degree from the Haute école d’ingénierie et d’architecture (HEIA-FR) in 2014 and the M.Sc. degree in Electrical Engineering from the École polytechnique fédérale de Lausanne (EPFL) in 2018. He is currently a Digital Design Engineer at ON Semiconductor in Marín, Switzerland.

Andreas Tofftegaard Kristensen (Student Member, IEEE) was born in Hillerød, Denmark, in 1994. He received his B.Sc. degree in Electrical Engineering in 2017 and his M.Sc. degree (hons) in Computer Science and Engineering in 2019, both from the Technical University of Denmark. He is currently pursuing a Ph.D. degree in Electrical Engineering under the supervision of Prof. Andreas Burg in the Telecommunications Circuits Laboratory at EPFL, Switzerland. His research interests include vital-sign detection using commodity WiFi routers, full-duplex self-interference cancellation, and custom hardware architectures for neural networks.

Andreas Burg (Member, IEEE) was born in Munich, Germany, in 1975. He received the Dipl.-Ing. degree from the Swiss Federal Institute of Technology (ETH) Zurich, Switzerland, in 2000, and the Dr. sc. techn. degree from the Integrated Systems Laboratory, ETH Zurich, in 2006. In 1998, he worked at Siemens Semiconductors, San Jose, CA, USA. During his doctoral studies, he worked at Bell Labs Wireless Research for one year. From 2006 to 2007, he was a Post-Doctoral Researcher with the Integrated Systems Laboratory and with the Communication Theory Group, ETH Zurich. In 2007, he co-founded Celestrius, an ETH-spinoff in the field of MIMO wireless communication, where he was responsible for the ASIC development as the Director for VLSI. In January 2009, he joined ETH Zurich as a SNF Assistant Professor and as the Head of the Signal Processing Circuits and Systems Group, Integrated Systems Laboratory. In January 2011, he joined the Ecole polytechnique fédérale de Lausanne (EPFL), where he is leading the Telecommunications Circuits Laboratory. He was promoted to Associate Professor with tenure in June 2018. Dr. Burg is a member of the EURASIP SAT SPDC, the IEEE TC-DISPS, and the CAS-VSATC. He has served on the TPC of various conferences on signal processing, communications, and VLSI. He was a TPC Co-Chair for VLSI-SoC 2012 and ESSCIRC 2016 and SIPS 2017. He was the General Chair of ISLPED 2019. He served as an Editor for the IEEE Transaction of Circuits and Systems in 2013 and on the Editorial Board of the Springer Microelectronics Journal. He is currently an Editor of the Springer Journal on Signal Processing Systems, MDPI Journal on Low Power Electronics and Applications, and the IEEE Transactions on Very Large Scale Integration (VLSI) Systems.

Alexios Balatsoukas-Stimming (Member, IEEE) received the Diploma and M.Sc. degrees in electronics and computer engineering from the Technical University of Crete, Chania, Greece, in 2010 and 2012, respectively, and the Ph.D. degree in computer and communications sciences from the Ecole polytechnique fédérale de Lausanne (EPFL), Switzerland, in 2016. He then spent one year at the European Laboratory for Particle Physics (CERN) as a Marie Skłodowska-Curie Post-Doctoral Fellow. He was a Post-Doctoral Researcher with the Telecommunications Circuits Laboratory, EPFL, from 2018 to 2019. He is currently an Assistant Professor with the Eindhoven University of Technology, The Netherlands. His research interests include VLSI circuits for signal processing and communications, error correction coding theory and practice, as well applications of machine learning to signal processing for communications.