Quantum Computational Advantage via 60-Qubit 24-Cycle Random Circuit Sampling

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To ensure a long-term quantum computational advantage, the quantum hardware should be upgraded to withstand the competition of continuously improved classical algorithms and hardwares. Here, we demonstrate a superconducting quantum computing system Zuchongzhi 2.1, which has 66 qubits in a two-dimensional array in a tunable coupler platform. The readout fidelity of Zuchongzhi 2.1 is considerably improved to an average of 97.74%. The more powerful quantum processor enables us to achieve larger-scale random quantum circuit sampling, with a system scale of up to 60 qubits and 24 cycles. The achieved sampling task is about 6 orders of magnitude more difficult than that of Sycamore [Nature 574, 505 (2019)] in the classic simulation, and 3 orders of magnitude more difficult than the sampling task on Zuchongzhi 2.0 [arXiv:2106.14734 (2021)]. The time consumption of classically simulating random circuit sampling experiment using state-of-the-art classical algorithm and supercomputer is extended to tens of thousands of years (about $4.8 \times 10^4$ years), while Zuchongzhi 2.1 only takes about 4.2 hours, thereby significantly enhancing the quantum computational advantage.

INTRODUCTION

Quantum computers are emerging with the promise of solving certain computational tasks exponentially faster than the current classical computers [1, 2]. Limited by the development of quantum hardwares, quantum computing has been at the stage of small-scale demonstrations for several decades in the past [3]. Recently, thanks to the significant progress in superconducting and photonic platforms, the long-anticipated milestone of quantum computational advantage or supremacy [4–7] has been achieved by using the quantum processors Sycamore [8], Jiuchang [9, 10], and Zuchongzhi [11] successively. These quantum processors with dozens of qubits reveal remarkable potential for quantum computing to offer new capabilities for near-term applications in the noisy intermediate scale quantum (NISQ) area, such as quantum simulation [12–25], quantum machine learning [26–32], and cloud quantum computing [33–38].

Nonetheless, quantum computational advantage will be a long-term competition between classical simulation and quantum devices, rather than being a one-off experimental demonstration. During the past two years, the classical simulation algorithms keep evolving [39–46]. In particular, it is estimated in Ref. [40] that simulating Sycamore’s 53-qubit and 20-cycle circuit sampling only takes about 19 days on Summit, and the exact amplitudes for 2 million correlated bitstrings were computed in 5 days by using only 60 GPUs in a recent work [41], in comparison with 10,000 years as estimated in the original paper [8]. Additionally, since calculating and storing the evolution of the entire state-space of the 53 qubits in random circuit sampling is still possible [39], there is a sample-size-dependent loophole in the Google’s Sycamore experiment. The development of classical algorithms and hardwares is almost about to overturn the quantum computational advantage that Sycamore has achieved. Thus, the quantum hardware needs to be continuously upgraded to maintain the quantum computational advantage. Such a long-term competition will also provide an important diagnose to benchmark the quantum computing system which is useful for eventually realizing fault-tolerant quantum computing.

In this work, a new 66-qubit two-dimensional superconducting quantum processor, called Zuchongzhi 2.1, is designed and fabricated. Compared to Zuchongzhi 2.0 [11], the readout performance of Zuchongzhi 2.1 is greatly improved to an average fidelity of 97.74%, while the single-qubit gate and the two-qubit gate have an average fidelity of 99.84% and 99.40%, respectively. Based on this state-of-the-art quantum processor, the random quantum circuit sampling with a system size up to 60 qubits and 24 cycles is realized experimentally. As estimated, the classical computational cost of simulating our sample task is about 6 orders of magnitude and 5000 times higher than that of the hardest tasks on the Sycamore [8] and
Our experiment extended the classical simulation time of random circuit sampling experiment to tens of thousands of years, even using the state-of-the-art classical supercomputers.

**FIG. 1. Device schematic of the Zuchongzhi 2.1 quantum processor.** (a) The Zuchongzhi 2.1 quantum processor is composed of two sapphire chips combined by flip-chip technique, one of which has 66 qubits and 110 couplers, and the other carries all the control lines. (b) Simplified circuit schematic of the qubit, coupler and readout. The coupler marked in red in the left panel is not working properly, which can only provide fixed coupling with a coupling strength of about 7.5 MHz.

**Zuchongzhi 2.1 —— AN UPGRADED HIGH-PERFORMANCE QUANTUM PROCESSOR**

**60-QUBIT RANDOM CIRCUIT SAMPLING**

After the basic calibration, we implement random quantum circuit sampling to characterize the overall performance of the quantum processor, and measure the degree of quantum computational advantage. The gate sequence of our random quantum circuit is shown in Fig. 3(a). Each cycle consists of a layer of single-qubit gates randomly selected from set \{\sqrt{X}, \sqrt{Y}, \sqrt{W}\} and applied to all qubits, followed by a layer of two-qubit iSWAP-like gates. The two-qubit gates in each two-qubit gate layer are applied according to a specified pattern, labeled by A, B, C, and D, and the layer is implemented to realize fast tuning of the coupling strength \(g\) continually from \(\sim +5\) MHz to \(\sim -50\) MHz. Except for a unfunctional coupler (see Fig. 1(b)), the remaining 66 qubits and 109 couplers on the quantum processor function properly, among which 60 qubits are selected for random quantum circuit sampling experiment.

Compared with previous work [11], Zuchongzhi 2.1 mainly upgrades the performance of readout. Specifically, the coupler frequency at turn-off point is significantly higher than the readout frequency, so that we don’t need to reset the qubit frequency when performing measurement. After calibrating and optimizing the readout, the average single-qubit state readout error of the selected 60 qubits can reach \(e_r = 2.26\%\) (Fig. 2(a)). Among them, the highest readout fidelity reach 99.1%. The huge improvement in readout performance plays a key role in our realization of larger and deeper random quantum circuit sampling.

The procedures of calibration and optimization of single-qubit and two-qubit gate are similar to Zuchongzhi 2.0 [11]. In order to achieve parallel execution of gates, all the couplers are turned off when single-qubit gates are applied to isolate each qubit, and the required couplers are turned on only when two-qubit gates are implemented. The two-qubit gate implemented in our experiment is iSWAP-like gate [8], for the purpose of random circuit sampling. The matrix form of iSWAP-like gate is:

\[
\begin{pmatrix}
1 & 0 & 0 & 0 \\
0 & e^{i(\Delta_+ + \Delta_-) \cos \theta} & -ie^{i(\Delta_+ - \Delta_-) \sin \theta} & 0 \\
0 & -ie^{i(\Delta_+ + \Delta_-) \sin \theta} & e^{i(\Delta_- - \Delta_+) \cos \theta} & 0 \\
0 & 0 & 0 & e^{i(2\Delta_+ - \phi)}
\end{pmatrix}
\]

where the five parameters \(\{\theta, \phi, \Delta_+, \Delta_-, \Delta_{\text{off}}\}\) are obtained by two-qubit gate cross-entropy benchmarking (XEB) [5, 50] fitting. The use of a stronger coupling strength (\(~14\) MHz) than that (\(~10\) MHz in 2.0) increases the duration of iSWAP-like gate is shortened from \(\sim 32\) ns to \(\sim 24\) ns. The performance of quantum gates is characterized by parallel XEB, yielding the average pauli errors of 0.16\% (Fig. 2(b)) and 0.60\% (Fig. 2(c)) for single-qubit gates and two-qubit gates, respectively, in the case of all gates are applied simultaneously.

**Zuchongzhi 2.1** is an upgraded version of the same generation of Zuchongzhi 2.0 [11] (Zuchongzhi 1.0 is used in Ref. [23]). Zuchongzhi 2.1 is designed and fabricated as a \(11 \times 6\) two-dimensional rectangular superconducting qubit array composed of 66 Transmon qubits [47] (see Fig. 1). Except for the qubits at the boundary, each qubit has four tunable couplers to couple to its nearest neighboring qubits [48], where the coupler is also a Transmon qubit, whose frequency several GHz higher than that of the data qubits [49]. All the qubits and couplers are fabricated on a sapphire chip, and all the control lines are fabricated on another sapphire chip. These two separate sapphire chips are then stacked together with the indium bump flip-chip technique. Each qubit has a microwave drive line and a fast flux-bias line to realize full control, including state excitation and qubit frequency modulation. Each coupler is controlled by a magnetic flux bias line, to realize fast tuning of the coupling strength \(g\) continually from \(\sim +5\) MHz to \(\sim -50\) MHz.
FIG. 2. Readout, single-qubit gate and two-qubit gate performance of the selected 60 qubits. (a) and (b) are the readout error $e_r$ and single-qubit gate pauli error $e_1$ for these 60 qubits, respectively. (c) The two qubit gate pauli error $e_2$ of the 99 two-qubit gates used. The errors are measured when operating all qubits simultaneously. The average errors of readout and quantum gates are also given in each subgraph.

FIG. 3. 60-qubit random quantum circuit, 4-patch calibration, and results of circuit with 15-60 qubits and 10-cycle. (a) In the processor structure topology diagram, the circles represent qubits, and the discarded qubits are marked with a shaded colour. The single-qubit gates in the random quantum circuit are chosen randomly from the set of $\{\sqrt{X}, \sqrt{Y}, \sqrt{W}\}$. The orange, blue, green, and red lines represent the two-qubit gates of the four patterns A, B, C, and D respectively. (b) We divide the circuit into 4 patches as shown, and optimize the parameters of iSWAP gates in each patch. (c) The XEB fidelities of circuit with 15-60 qubits and 10-cycle before and after 4-patch calibration. Each data point, including the results from full circuit, patch circuit, and elided circuit, is an average over nine quantum circuit instances. The predicted fidelity result is shown as a black line labeled by “Estimated”, which is calculated from a simple multiplication of individual operation. The gray line labeled by “Fitting” is the exponential fit of the fidelities before 4-patch calibration. Whether it’s before or after 4-patch calibration, the fidelities of the patch and elided circuits are in good agreement with those of the full circuit. And after the 4-patch calibration, the fidelity of each circuit can be significantly improved, and is highly consistent with the predicted fidelity.

In general, the verification of large-scale random quantum circuit is done through two variant circuits, named patch circuit and elided circuit, which are designed by removing a slice of two-qubit gates and only a fraction of the gates between the patches, respectively. As the first step of the experiment, we first evaluate whether these two verification methods are applicable on this quantum processor. We implement these two variant circuits and full version of the circuits ranging from 15 qubits to 60 qubits with 10 cycles, and calculate the linear XEB fidelities $F_{XEB}$ of the respective output bitstrings. Experimental results (see Fig. 3(c)) show that the average ratio of patch circuit and elided circuit fidelities to full circuit fidelity are 1.09 and 1.13, indicating the effectiveness of these two verification circuits.

However, the fidelity of all circuits appears lower than the predicted fidelity calculated from a simple multiplication of individual operations. This is due to the additional error...
FIG. 4. Experimental results of random quantum circuits in the quantum computational advantage regime. (a) Results of random quantum circuits with 60 qubits and 12-24 cycles. Each data point denotes the average fidelity of the patch or elided circuit over 12 distinct quantum circuit instances, as an estimate of the fidelity of the full circuit. The error bar denotes three standard deviations. For each 60-qubit 24-cycle circuit instance, about 70 million bitstrings are sampled in 4.2 hours (1 million samples per 210 seconds). (b), (c), (d), and (e) show the fidelity of each individual 16-cycle, 20-cycle, 22-cycle, and 22-cycle elided circuit instance, respectively. The band corresponding to ±σ_{\text{mean}}, which is the mean statistical error bar of the 12 instances.

caused by our control method. In Zuchongzhi 2.1, the coupler and qubit are placed at their original frequencies most of the time, and then detuned to the idle frequencies within a few microseconds before and during the experiment, and finally detuned back to their original frequencies after the readout pulse ends (Zuchongzhi 2.0 uses DC pulse to keep the qubit and coupler at the idle frequencies all the time.). The distortion of the square pulse causes qubit frequency and coupling strength continuously change slightly during the operation time. To mitigate this effect, the square pulses on the qubit are calibrated. However, the calibration of square pulses on coupler is not performed, due to the frequency of the couplers is too high. This causes the parameters of iSWAP-like gate obtained by the two-qubit XEB to be slightly inaccurate for shallow circuits.

We develop a new calibration method, called 4-patch calibration, to search the optimal parameters of the iSWAP-like gate, based on the original gate parameters obtained by the two-qubit XEB. We divide the full circuit into 4 non-overlapping patches, which nevertheless covers all the iSWAP gates. Then we sample the bitstrings of the 4 patch circuits separately, and use the sampled bitstrings as the training set b_{\text{train}}. For each patch, we use a gradient-based machine learning to optimize the parameters of the iSWAP gates it contains. Specifically, we consider the set $\gamma = \{\gamma_1, ..., \gamma_{n_g}\}$ as trainable parameters, where $\gamma_i = (\theta^i, \phi^i, \Delta^i, \Delta^{\text{off}}_i)$ is the parameters of i-th iSWAP gate, and $n_g$ is the total number of iSWAP gates in this patch. By minimizing the loss function

$$\text{Loss}_{\text{XEB}}(\gamma, b_{\text{train}}) = 1 - F_{\text{XEB}}(\gamma, b_{\text{train}}),$$

using the BFGS optimizer, we are able to find the optimal parameters of each iSWAP for this patch, where $F_{\text{XEB}}(\gamma, b_{\text{train}})$ is the linear XEB fidelity of chosen patch. All these trained parameters of all the iSWAP gates are obtained. After 4-patch calibration, we re-calculate the XEB fidelities of all of the circuits in Fig. 3(c) using the the optimized two-qubit gate parameters. Results show that all of these fidelities have been greatly improved and match the predicted fidelities quite well (see Fig. 3(c)), indicating that the optimized parameters have adaptability to different quantum circuits. Furthermore, The behavior of two variant circuits are more consistent with full circuits, where the the average ratio of patch circuit and elided circuit fidelities to full circuit fidelity are improved to 1.05 and 1.07, respectively. Since the circuit is split into 4 patches for training, our 4-patch calibration method can be efficiently implemented on the classical computer. For larger circuits, our method can easily be modified into n-patch calibration to maintain its efficiency.

We sample the output bitstrings of 60-qubit full, patch, and elided circuits with increasing depth from 12 to 24 cycles, and employ patch and elided circuits to estimate the performance of full circuit. At each system size, a total of 12 randomly generated circuit instances are executed. Figure 4(a) shows the XEB fidelities of patch and elided circuits. For the largest circuit with 60 qubits and 24 cycles, we collect approximately
TABLE I. The runtime of tensor network algorithm for different circuits on Summit. The classical simulation consumption estimation of the random quantum circuit sampling experiment on the Sycamore, Zuchongzhi 2.0, and Zuchongzhi 2.1 processors are provided. FPOs is the abbreviation for the number of floating point operations, QPU is the abbreviation for quantum processing unit.

| Processor       | Circuit       | Fidelity | # of bitstrings | FPOs (a perfect sample) | FPOs (circuit) | Runtime on Summit | Runtime on QPU | ClassicalRuntime | QuantumRuntime |
|-----------------|---------------|----------|-----------------|-------------------------|----------------|--------------------|-----------------|-----------------|-----------------|
| Sycamore [8]    | 53-qubit 20-cycle | 0.224%   | $3.0 \times 10^9$ | $1.63 \times 10^{28}$  | $1.10 \times 10^{24}$ | 15.9 days          | 600s           | $2.29 \times 10^4$ |                |
| Zuchongzhi 2.0 [11] | 56-qubit 20-cycle | 0.0662%  | $1.9 \times 10^7$ | $1.65 \times 10^{20}$  | $2.08 \times 10^{24}$ | 8.2 years          | 1.2h            | $6.02 \times 10^4$ |                |
| Zuchongzhi 2.1  | 60-qubit 22-cycle  | 0.0758%  | $1.5 \times 10^7$ | $1.06 \times 10^{22}$  | $1.21 \times 10^{26}$ | 4.8 $\times 10^2$ years | 1h             | $4.21 \times 10^6$ |                |
| Zuchongzhi 2.1  | 60-qubit 24-cycle  | 0.0366%  | $7.0 \times 10^7$ | $4.68 \times 10^{23}$  | $1.2 \times 10^{28}$  | $4.8 \times 10^4$ years | 4.2h           | 9.93 $\times 10^7$ |                |

7.0 $\times 10^7$ bitstrings for each circuit instance, and the combined linear XEB fidelity of these 12 elided circuit instances are calculated as $F_{\text{XEB}} = (3.66 \pm 0.345) \times 10^{-4}$. Thus, with high statistical significance ($> 10\sigma$), the null hypothesis of uniform sampling ($F_{\text{XEB}} = 0$) is rejected.

**COMPUTATIONAL COST ESTIMATION**

We employ the state-of-the-art classical algorithm, tensor network algorithm [40–46], to estimate the classical computational cost of our largest circuit with 60 qubits and 24 cycles. The number of floating point operations to generate one perfect sample from the 60-qubit 24-cycle random circuit are estimated as $1.63 \times 10^{38}$ by the python package cotengra [51] (see Supplemental Material for details). Thus, it would cost a total of $1.10 \times 10^{22}$ floating point operations to reproduce the same results of this hardest circuit ($7.0 \times 10^7$ bitstrings, 0.0366% fidelity) using classical computer. Table I also shows the extrapolated run times for Sycamore’s 53-qubit 20-cycle circuit [8] and Zuchongzhi 2.0’s 56-qubit 20-cycle circuit using tensor network algorithm.

As shown in Table I, using the tensor network algorithm, the classical computational cost of our sample task with 60-qubit and 24-cycle is about 6 orders of magnitude and 5000 times higher than that of the hardest tasks on the Sycamore and Zuchongzhi 2.0 processor [11], respectively. The random circuit sampling task with 60-qubit and 24-cycles, achieved by Zuchongzhi 2.1 in 4.2 hours, would cost Summit 48,000 years to simulate.

**CONCLUSION**

In conclusion, the high-performance superconducting quantum computing system Zuchongzhi 2.1 has achieved a larger-scale random quantum circuit sampling with 60-qubit and 24-cycle, yielding a Hilbert space dimension up to $2^{90}$. Compared with Zuchongzhi 2.0, our sampling task is about 5000 times more difficult in classical simulation, thus the quantum computational advantage has been significantly enhanced. Our future work would be to investigate the practical applications of random quantum circuits on NISQ devices, such as certified random bits [52], error correction [53], and hydrodynamics simulation [54], beyond the abstract sampling task.

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Supplemental Material for
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Since most of the methods of calibration and result analysis have been provided in the Ref. [1] of Zuchongzhi 2.0, in this supplemental material, we will list the relevant results of Zuchongzhi 2.1 without describing too many details about the method. Interested readers may refer to the Ref. [1] for more details about the method used.

I. QUANTUM PROCESSOR

Our device is a 66-qubit superconducting programmable quantum processor, consisting of 66 Transmon qubits [2] and 110 tunable couplers [3], which is similar to Zuchongzhi 2.0 [1]. Each qubit is inductively coupled to a control line for both XY and Z control, and capacitively coupled to a separate XY and Z control, and capacitively coupled to a separate bandpass filter [4, 5] for fast and high fidelity readout. Each qubit is tunably coupled to one of its nearest neighbor qubits with a coupler which can tune coupling strength from $\sim +5$ MHz to $\sim -50$ MHz, except for the coupler between qubit $Q_{22}$ and $Q_{15}$ which does not work well. With the tunable coupler, we can tune off the qubit-qubit coupling when qubit at idle, and tune on the coupling when performing two-qubit gates. The coupling strength we used to perform two-qubit gates is about $-14$ MHz. Steps of fabrication are same with Zuchongzhi 2.0, which will not be described here.

II. EXPERIMENTAL WIRING

The experimental wiring setup for qubit/coupler control and frequency-multiplexed readout of cryogenic system and the configuration of room temperature electronics are same with the setup of Zuchongzhi 2.0 [1]. The room temperature electronics used in this experiment includes 330 DAC channels, 11 ADC channels, 11 DC channels and 32 microwave source channels. All experiments are performed in a dilution refrigerator at base temperature of 20 mK with a magnetic field shield.

III. GATE PERFORMANCE AND READOUT

A. Basic calibration on 66 qubits

The basic calibration steps of the processor are also the same with Zuchongzhi 2.0, all 66 qubits, 110 couplers, 66 readout resonators and 11 JPAs are involved in this process. One can see more details about the procedure in Ref [1]. The maximum frequencies $f_{\text{max}}$ of the all 66 qubits are shown in Fig. S3. The coupler between qubit $Q_{22}$ and $Q_{15}$ does not work properly, so there are 109 couplers which we can use to tune the coupling strength between near-neighbor qubits in this processor.

B. Fine-tune on 60 qubits

For technical and theory reasons, we select 60 qubits in the device and set other qubits’ frequencies far away from these qubits to avoid residual coupling. We then perform accurate calibration on these 60 qubits. After fine measurement of $T_1$ and XY crosstalk, we preliminary set a suitable idle frequency distribution. However, we find that the $T_1$ performance at idle frequency may change significantly during the experiment. Thus, we quickly measure these qubits’ $T_1$ and $T_2$ near idle frequencies in parallel and then adjust the idle frequency distribution if the coherence performance of qubits decreases.
1. Readout Calibration

All selected qubits are placed at idle frequencies during measurement. Readout fidelity of each qubit is measured after qubits are prepared at $|0\rangle, \ldots, |0\rangle$ or $|1\rangle, \ldots, |1\rangle$. To reduce the influence of energy relaxation and enhance the effective lifetime, we drive the qubits into $|2\rangle$ from $|1\rangle$ before readout [6]. By applying this technology, we can achieve average readout fidelity of 97.74%. To evaluate the performance of joint readout, we randomly prepare the qubits states $|s_1, s_2, \ldots, s_{60}\rangle$, where $s_i = 0$ or 1, and measure these randomly states to obtain the average joint readout fidelity, corresponding to 0.2304.

2. Single-Qubit Gate Calibration

Couplers and qubits are placed at their original frequencies at most time and then detuned to idle frequencies several microseconds before and during the experiment and finally detuned back to their original frequencies after the readout pulses end. Due to this control method, we find qubit frequency and coupling strength may vary slightly during the operation time, which may reduce the following single-qubit gate fidelity. To mitigate this effect, we measure the qubit frequency variation and then calibrate the square pulse. In Fig. S1, we show our ramsey test pulse to measure $z$ control pulse distortion and the phase before (after) calibration. After this calibration, we measure the single-qubit gate fidelity for isolated operation and simultaneous operation by cross-entropy benchmarking(XEB) [7], see Table S1. The difference between isolated fidelity and simultaneous fidelity is caused by XY crosstalk and residual coupling strength.

![Z control pulse distortion calibration](image1)

**FIG. S1.** Z control pulse distortion calibration. a, Pulse sequence of the $z$ control pulse distortion calibration. b, Phase before calibration. c, Phase after calibration.

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**FIG. S2.** Single-qubit gates XEB and readout errors. a, Integrated histograms of single-qubit gates Pauli error $e_i$. The dotted line represent isolated results, and the line represent simultaneous results. b, Integrated histograms of readout errors $e_{i|0}$ and $e_{i|1}$.

3. Two-Qubit Gate Calibration

iSWAP-like gates [7] are used in our experiment, which are realized by tuning two near-neighbor qubits into resonance. The procedures of calibration and optimizing are similar to Zuchongzhi 2.0 which we briefly illustrate here again. First, we set the total duration time of iSWAP-like gates to $24\mu s$ after considering the effect of the leakage to non-computational basis. To realize swap angles close to $\pi/2$, we delicately calibrate the coupling strength and detuning of two near-neighbor qubits.

After calibration of iSWAP-like gates parameters, we use XEB [7] to benchmark the gate performance. Through optimize the five parameters $\{\theta, \phi, \Delta_+, \Delta_-, \Delta_{\text{off}}\}$, as described in the main text, overall fidelities of XEB are obtained Fig. 2(main). We also analyze the error of speckle purity benchmarking(SPB) [7] which is shown in Fig. S4(b). Considering the effects of two-level-system(TLS), pulse distortion, decoherence and the residual coupling between nearest-neighbor qubits when simultaneous manipulating two-qubit gates in a specific pattern, we obtain an optimized resonance frequency configuration of all 99 two-qubit gates in four different patterns, as exhibited in Fig. S4(a).

After calibration and optimization, we compare two-qubit gates performance in the isolated and simultaneous situations. As illustrated in Fig. S6(a), the XEB error is close to SPB error in both cases which means our control error is small. The difference is that the SPB error is larger when simultane-
ously manipulate two-qubit gates which mainly caused from the residual coupling strength. Partial parameters of all 99 iSwap-like gates are shown in Fig. S6(b), the average swap angle and conditional phase are 90 degrees and 10 degrees separately.

### C. 4-patch calibration

Till now the parameters of all the iSWAP-like gates are calibrated using two-qubit XEB. As stated in the main text and section III (B2), the distortion of the square pulse will cause qubit frequency and coupling strength continuously change slightly during the operation time. However, the square pulses on coupler are not calibrated. Due to that the iSWAP-like gate parameters obtained by two-qubit XEB is fitted using 10-500 cycles circuits, the iSWAP-like gate parameters is slightly inaccurate for shallow circuits.

To optimize the XEB fidelity for the shallow and full circuits, it may be helpful to directly calibrate the iSWAP-like gate on the whole system level with shallow cycle. For such a purpose, we will minimize the loss function

\[
\text{Loss}_{\text{XEB}}(\vec{\theta}, b_{\text{train}}) = 1 - F_{\text{XEB}}(\vec{\theta}, b_{\text{train}}).
\]

(S1)

Here \(\vec{\theta}\) is a list of tunable parameters of all the iSWAP-like gates, \(b_{\text{train}}\) is a training dataset which is generated experimentally before hand, \(F_{\text{XEB}}\) is the cross-entropy fidelity. We note

**FIG. S3.** Average 2D \(T_1\) and qubit maximum frequency of 66 qubits.

**FIG. S4.** The qubit resonance frequencies and Purity error distribution of 99 couplers.
FIG. S5. Typical distribution of selected 60-qubits.
TABLE S1. Summary of system parameters.

| Parameters                                | Mean     | Median   | Stdev. | Figure |
|-------------------------------------------|----------|----------|--------|--------|
| Qubit maximum frequency (GHz)             | 5.094    | 5.099    | 0.129  | Fig. S3|
| Qubit idle frequency (GHz)                | 4.921    | 4.926    | 0.082  | Fig. S5|
| Readout drive frequency (GHz)             | 6.397    | 6.409    | 0.097  | Fig. S5|
| Qubit anharmonicity (MHz)                 | -246.6   | -245.3   | 4.9    | Fig. S5|
| \(T_1\) at idle frequency (\(\mu s\))    | 26.5     | 26.5     | 5.3    | Fig. S5|
| \(T_2^*\) at idle frequency (\(\mu s\))  | 3.4      | 2.9      | 2.1    | Fig. S5|
| Readout \(|0\rangle\) isolated / simultaneous (%) | 1.36 / 1.48 | 1.20 / 1.35 | 0.55 / 0.63 | Fig. S2|
| Readout \(|1\rangle\) isolated / simultaneous (%) | 3.22 / 3.03 | 3.02 / 2.93 | 1.03 / 0.91 | Fig. S2|
| 1Q XEB \(e_1\) isolated / simultaneous (%) | 0.15 / 0.16 | 0.14 / 0.16 | 0.05 / 0.04 | Fig. S2|
| 1Q XEB \(e_1\) purity isolated / simultaneous (%) | 0.12 / 0.13 | 0.11 / 0.12 | 0.03 / 0.04 | Fig. S2|
| 2Q XEB \(e_2\) isolated / simultaneous (%) | 0.048 / 0.060 | 0.40 / 0.52 | 0.31 / 0.30 | Fig. S6|
| 2Q XEB \(e_2\) purity isolated / simultaneous (%) | 0.42 / 0.51 | 0.35 / 0.44 | 0.23 / 0.24 | Fig. S6|

FIG. S6. Two-qubits gates XEB and parameters. a, Integrated histograms of two-qubit gates Pauli error \(e_2\). The dotted line represent isolated results, and the line represent simultaneous results. b, Integrated histograms of two control parameters \(\theta\) and \(\phi\).

FIG. S7. Two-qubit crossentropy benchmarking (XEB) on a pair of qubits.
FIG. S8. **4-patch calibration and experimental results.** (a) We divide the circuit into 4 patches as shown, and optimize the parameters of iSWAP gates in each patch. (c) The XEB fidelities of circuit with 15-60 qubits and 10-cycle before and after 4-patch calibration.

FIG. S9. **Parameters of iSWAP-like gates before and after 4-patch calibration**

**IV. RANDOM QUANTUM CIRCUITS**

In the random quantum circuit, single-qubit gates are chosen randomly from \{\sqrt{X}, \sqrt{Y}, \sqrt{W}\}, the two-qubit gates are implemented in the sequence of ABCDCDAB, where A, B, C and D are 4 different patterns. The random quantum circuit for 60-qubit and 24-cycle is constructed using the method in Ref. [1], and the four patterns for two-qubit gates are shown in Fig. S10. For the 60-qubit 22-cycle circuit, the sequence for two-qubit gates are set as (ABCDCDAB)*2+ABCD+CB, to ensure the difficulty of classical simulation.

**V. XEB RESULT ANALYSIS**

For a set of bitstrings \{q_i\}, we estimate the linear XEB fidelity from the ideal probabilities \{p_i = p_s(q_i)\} as

\[ F_i = \langle Dp \rangle - 1 \]  

(S2)

Firstly, we compare the XEB results of patch circuits and elided circuits with full circuits to check the efficacy of circuit performance estimation method. Fig. S11 shows the XEB results measured by full, patch and elided circuit of systems from 15 to 60 qubits with 10 cycles. The average ratio of patch circuit and elided circuit fidelity to full circuit fidelity are 1.05 and 1.07, both with a standard deviation of 6%.

We then check the probability distribution of our samples against the theoretical PDF

\[ P_l(x|\hat{F}_l) = (\hat{F}_l x + (1-\hat{F}_l))e^{-x} \]  

(S3)

where \( x \equiv Dp \) is bitstring probability scaled by the dimension \( D \). For elided circuit with 60 qubits and 24 cycles, we show the result of one circuit instance in Fig. S12. Kolmogorov-Smirnov test is performed to quantify the consistency of experimental data distribution with theoretical curve. Taking one circuit instance for example, the K-S test result is \( p = 0.77 \) for hypothesis \( F = \hat{F} \) while \( p = 8.0 \times 10^{-4} \) for hypothesis \( F = 0 \).

The statistical uncertainty of XEB is estimated with formula

\[ \hat{\sigma}_{F_i} = D\sqrt{\text{Var}(p)/N_s} \]  

(S4)
VI. CLASSICAL SIMULATION

In this section, two state-of-the-art classical algorithms, tensor network contraction algorithm (abbreviated as TNC, a single-amplitude algorithm) and Schrödinger-Feynman algorithm (abbreviated as SFA, a full-amplitude algorithm), are used to estimate the classical computational cost of our random quantum circuit. Compared with SFA, TNC is more ef-

FIG. S10. **Coupler activation patterns for 60 qubits.** Coupler activation pattern for 60 qubits that determines which qubits are allowed to interact simultaneously in a cycle.

![Coupler activation patterns for 60 qubits](image)

FIG. S11. **Performance of patch circuits and elided circuits.** Patch, elided and full circuit XEB fidelity from 15 to 60 qubits with 10 cycles. Each data point is averaged over 9 quantum circuit instances.

![Performance of patch circuits and elided circuits](image)

FIG. S12. **Distribution of bitstring probabilities from a 60-qubit 24-cycle circuit.** The theoretical curve $P_{\text{th}}(x|\hat{F}_l)$ is computed with the experimental XEB fidelity and scaled by the number of samples $N_\text{s} = 7 \times 10^7$.

![Distribution of bitstring probabilities](image)

FIG. S13. **Fidelity distribution of bootstrap samples.** The samples of a 60-qubit 24-cycle elided circuit are bootstrapped 2500 times. Calculated fidelities distribution is shown with a gaussian fit.

![Fidelity distribution of bootstrap samples](image)

We check the formula with bootstrap method. For a 60-qubit 24-cycle elided circuit, the statistical uncertainty of XEB is $1.20, 1.19, 1.21 \times 10^{-4}$ for the estimating formula, bootstrap and gaussian fit. The fidelity distribution of 2500 bootstrap samples with Gaussian fit are shown in Fig. S13.

Then we use inverse-variance weighting to estimate the fidelity and statistical uncertainty of all twelve 60-qubit and 24-cycle elided circuits. The result is $\hat{F}_l = (3.66 \pm 0.35) \times 10^{-4}$, indicating great consistency with the theoretical statistical uncertainty $3.5 \times 10^{-4}$.
cient for this system size, so the results of TNC are present in the main text as the estimation of classical computational cost.

A. Tensor network contraction

The cost of TNC algorithm can be estimated by the python package cotengra. When using this package, we leave 21 out of the 60 qubits as open, set the size of the largest intermediate tensor as $2^{30}$, and the optimizer kahypar is chosen. For the 60-qubit random quantum circuit with 22 cycles and 24 cycles, the number of floating point operations to generate one perfect sample are estimated as $1.06 \times 10^{22}$ and $4.68 \times 10^{23}$, respectively, by repeating the procedure about 100 times (see Fig. S14).

![FIG. S14. Probability distributions of the number of floating point operations for contraction of (a) 60-qubit 22-cycle circuit and (b) 60-qubit 24-cycle circuit.](image)

As estimated in Ref. [8], it would cost 833.75s to generate one perfect sample for a tensor network with $6.66 \times 10^{18}$ contraction cost using Summit. Thus, it would cost $(4.68 \times 10^{23}) \times (7.0 \times 10^{7}) \times (3.66 \times 10^{-4}) \times 833.75s = 4.8 \times 10^{4}$ years to reproduce the same results as the 53-qubit 20-cycle circuit in Ref. [7] and our 60-qubit 24-cycle circuit using Summit.

B. Schrödinger-Feynman algorithm

For the 60-qubit random quantum circuit with 22 cycles and 24 cycles, the promising cuts for SFA are shown in Fig. S15. We use the same simulator and server in Ref. [1] to estimate the cost of SFA. The results are shown in Table S2 (For the sake of comparison, we also list the estimation for Sycamore and ZuChongzhi 2.0’s circuits).

![FIG. S15. optimal cut for (a) 60-qubit circuit with 22 cycles and 60-qubit circuit with 24 cycles, respectively.](image)

![FIG. S16. Cumulative probability distribution of $|\delta_\theta|$ for iSWAP-like gates. $|\delta_\theta|$ has an average around 0.054 and the speedup of SFA is less than an order.](image)

![FIG. S17. Classical speedup given by the imbalance gates. We assume all iSWAP-like gates deviate from $\pi/2$ by the same $\delta_\theta$ and calculate the speedup with given $g$ and $F$. Left: speedup with varied fidelity $F$ and fixed $g = 54$. Right: speedup with varied $g$ and fixed $F = 0.0366\%$.](image)

| Processor          | # of qubits | cycle | fidelity | run time (years) |
|--------------------|-------------|-------|----------|------------------|
| Sycamore           | 53          | 20    | 0.224%   | 1.332            |
| ZuChongzhi 2.0     | 56          | 20    | 0.0662%  | 8.612,623        |
| ZuChongzhi 2.1     | 60          | 22    | 0.0738%  | 6.4 \times 10^9  |
| ZuChongzhi 2.1     | 60          | 24    | 0.0366%  | 1.2 \times 10^2  |

TABLE S2. Run times of SFA using 7,630,848 CPU cores (the most powerful supercomputer Fugaku has a total of 7,630,848 cores).
We did not consider the DCD formation in our estimation. The DCD formation appears three times in the 60-qubit 22-cycle and 24-cycle circuits. In addition, the balanced iSWAP-like gate in our experiment has $\theta \approx \pi/2$ and $\phi \approx \pi/18$. Deviation of $\theta$ and $\phi$ from the expected values results in imbalanced gates, which can accelerate the simulation with SFA. We calculate classical simulation speedup for imbalanced gates using the method introduced in Ref. [1, 7]. Assuming the imbalanced gates in our experiments is in the form of iSWAP-like($\pi/2 \pm \delta\theta$, $\phi \approx \pi/18$). We show the distribution of $|\delta\theta|$ in Fig. S16. In the experiments, $|\delta\theta|$ has an average 0.054 radians. For 60-qubit 24-cycle circuits, we have XEB fidelity $F = 0.0366\%$ and the number of decomposed iSWAP-like gates $g = 54$ in SFA. The speedup resulted from imbalanced gates is shown in Fig. S17. We can conjecture that the classical speedup in our experiment is less than an order.

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