Surface code compilation via edge-disjoint paths

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Abstract

We provide an efficient algorithm to compile quantum circuits for fault-tolerant execution. We target surface codes, which form a 2D grid of logical qubits with nearest-neighbor logical operations. Embedding an input circuit’s qubits in surface codes can result in long-range two-qubit operations across the grid. We show how to prepare many long-range Bell pairs on qubits connected by edge-disjoint paths of ancillas in constant depth that can be used to perform these long-range operations. This forms one core part of our Edge-Disjoint Paths Compilation (EDPC) algorithm, by easily performing many parallel long-range Clifford operations in constant depth. It also allows us to establish a connection between surface code compilation and several well-studied edge-disjoint paths problems. Similar techniques allow us to perform non-Clifford single-qubit rotations far from magic state distillation factories. In this case, we can easily find the maximum set of paths by a max-flow reduction, which forms the other major part of EDPC. EDPC has the best asymptotic worst-case performance guarantees on the circuit depth for compiling parallel operations when compared to related compilation methods based on swaps and network coding. EDPC also shows a quadratic depth improvement over sequential Pauli-based compilation for parallel rotations requiring magic resources. We implement EDPC and find significantly improved performance for circuits built from parallel CNOTs, and for circuits which implement the multi-controlled X gate C²NOT.
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1 Introduction

Quantum hardware will always be somewhat faulty and subject to decoherence, due to inevitable fabrication imperfections and the impossibility of completely isolating physical systems. For large computations it becomes a certainty that faults will occur among the many qubits and operations involved. \textit{Fault-tolerant quantum computation} (FTQC) can be implemented despite this by encoding the information in a quantum error correcting code and applying logical operations which are carefully designed to process the encoded information with an acceptably low effective error rate.

The surface code \cite{Kit03; BK98} provides a promising approach to implement FTQC. Firstly, it can be implemented using geometrically local operations on a patch of qubits in a 2D grid, which is the natural setting for many hardware platforms including superconducting \cite{Fow+12; Cha+20a} and Majorana \cite{Kar+17} qubits. Secondly, the logical qubits it encodes remain protected even for relatively high noise rates, with a threshold of around 1\% \cite{WFH11}. Thirdly, a sufficiently general set of elementary logical operations can be performed fault tolerantly on qubits encoded in the surface code using \textit{lattice surgery} \cite{Hor+12}. By tiling the plane with surface code patches, a 2D grid of logical qubits is formed, where the elementary operations are geometrically local; see Figure 1. When combined with magic state distillation \cite{BK05} these operations become universal for quantum computing. Indeed this approach, which we will refer to as the \textit{surface code architecture}, is seen as among the most promising by many research groups and companies working in quantum computing \cite{Fow+12; Cha+20b; YK17; FC16}.

In this work, we seek to minimize the resources required to fault-tolerantly implement a quantum algorithm using the surface code architecture, which we will refer to as the \textit{surface code compilation problem}. For concreteness, we will assume that the input quantum algorithm is expressed as a quantum circuit composed of preparations and destructive measurements of individual qubits in the Z or X basis, controlled-not (\texttt{cnot}), Pauli-X, -Y, and -Z, Hadamard (\texttt{H}), Phase (\texttt{S}) and \texttt{T} gates. Our results can be easily generalized to broader classes of input quantum circuits. The output is the quantum algorithm executed using the elementary logical surface code operations shown in Figure 1. Ultimately, we would like to minimize the \textit{physical space-time cost}, which is the product of the number of physical qubits and the time required to run an algorithm. To avoid implementation details, we instead minimize the more abstract \textit{logical space-time cost}, which is the number of logical qubits (the circuit width) multiplied by the number of logical time steps (the circuit depth) of the algorithm expressed in elementary surface code operations. The logical and physical space-time costs are expected to be 1-to-1 and monotonically related (see Appendix B), such that minimizing the former should minimize the latter.

A well-established approach to implement surface code compilation is known as sequential Pauli-based computation \cite{Lit19}, where non-Clifford operations are implemented by injection using Pauli measurements, and Clifford operations are conjugated through the circuit until the end. The circuit that is run in this approach then consists of a sequence of high-weight Pauli measurements which
Figure 1: Logical qubits (light and dark gray patches) encoded in the surface code form a 2D grid. The elementary operations can be applied on any lattice translations of those shown. Their times in units of surface code logical time steps are as follows. 0 logical time steps: Single-qubit preparation in the \( X \) basis (i), and the \( Z \) basis (ii). Destructive single-qubit measurement, which moves the patch outside of the code space, in the \( X \) basis (iii), and the \( Z \) basis (iv) take 0 steps. 1 logical time step: Two-qubit measurement of \( XX \) (v) and \( ZZ \) (vi). A move of a logical qubit from one patch to an unused patch (vii). Two-qubit preparation (viii) and destructive measurement (ix) in the Bell basis. 3 logical time steps: A Hadamard gate, which uses three ancilla patches (x). See Appendix A for further details.

can have overlapping support leading them to be measured one after the other. For large input circuits this can be problematic because highly parallel input circuits can become serialized with prohibitive runtimes.

A major challenge to solve the surface code compilation problem is that quantum algorithms typically involve operations between logical qubits that are far apart when laid out in a 2D grid. One approach to deal with a long-range gate is to swap logical qubits around until the pair of interacting qubits are next to one-another [CSU19]. However, this can result in a deep circuit, see Figure 2a. A more efficient approach is to create long-range entanglement by producing Bell pairs, which for example can be used to implement a long-range CNOT with a constant-depth circuit [Bri+98; LO17; Jav+17] (see Figure 2b). Both of these approaches can be implemented with the elementary operations of the surface code.

Moreover, algorithms typically consist of many long-range operations that can ideally be performed in parallel. For swap-based approaches, this can be done by considering a permutation of the logical qubits which is implemented by a sequence of swaps [Lao+18; Mur+19; ZW19]. Finding these SWAP circuits reduces to a routing problem on graphs [CSU19; SHT19]. There are efficient algorithms that solve this problem for certain families of graphs [ACG94; CSU19], but finding a minimal depth solution is NP-hard in general [BR17]. Alternatively, linear network coding can be used to prepare many long-range pairs in constant depth [LOW10; Kob+09; Kob+11; SLI12; HPE19; BH20], and then these Bell
pairs can be used to implement operations on pairs of distant qubits. But a major barrier for using linear network coding is the lack of known efficient algorithms to find linear network codes.

In this paper, we provide a solution to the surface code compilation problem which generalizes the use of entanglement for long-range CNOTs discussed above to the implementation of many long-range operations in parallel. In particular, we propose the Edge-Disjoint Paths Compilation (EDPC) algorithm, which is a computationally efficient classical algorithm tailored to the elementary operations of the surface code architecture. We find evidence that our EDPC algorithm significantly outperforms other approaches by performing a detailed cost analysis for the execution of a set of quantum circuits benchmarks.

EDPC reduces the problem of executing quantum circuits to problems in graph theory. Logical qubits correspond to graph vertices, and there is an edge between qubits if elementary surface code operations can be applied between them. We show how to perform multiple long-range CNOTs in constant depth along a set of edge-disjoint paths (EDP) in the graph. In other words, long-range CNOTs can be performed simultaneously, in one round, if their controls and targets are connected by edge-disjoint paths. This leads to the well-studied problem of finding maximum EDP sets [Kle96]. The ability to perform long-range CNOTs along with the elementary operations allows compilation of Clifford operations. We also give a construction for EDP sets that are asymptotically optimal in the depth of worst-case sets of independent CNOTs.

The final operations that complete our gate set for universal quantum compu-
Table 1: A comparison in the depth of surface code compilation algorithms (that use $\Theta(n)$ space) for various input circuits of width $n$. We compare the worst-case performance for a single long-range CNOT gate, for CNOT circuits with $n/2$ parallel CNOT gates, and for $k$ rotations, with $k \in \mathbb{N}$, that need to be performed at the boundary.
mentary operations of the surface code with a low logical space-time cost. In Appendix A we give an overview of the surface code and justify the resource costs of the elementary operations shown in Figure 1. The initial quantum algorithm is assumed to be expressed as a circuit diagram involving preparations and measurements of individual qubits in the computational basis, controlled-not (CNOT), Pauli-X, -Y, and -Z, Hadamard (H), Phase (S) and T gates. In this section we build and calculate the cost of some key circuit components from the elementary surface code operations in Figure 1. The contents of this section are reproductions or straightforward extensions of previously-known circuits.

2.1 Single-qubit operations

Some of the operations of the input circuit can be implemented directly with elementary surface code operations, namely the preparation and measurement of individual qubits in the measurement basis, and the Hadamard gate (provided three neighboring ancillary patches are available as ancillas, see Figure 1). Pauli operations do not need to be implemented at all since they can be commuted through Clifford gates and arbitrary Pauli gates [Kni05] and can therefore be tracked classically and merged with the final measurements. For this reason, while we occasionally explicitly provide the Pauli corrections where instructive, we often show equivalence of two circuits only up to Pauli corrections. The remaining single-qubit operations in the input circuit, namely the S and T gates, can be implemented using magic states and is addressed in Section 4.

2.2 Local CNOT and SWAP gates

An important circuit component is the CNOT gate, which can be implemented as shown in Figure 3a [ZBL08]. The qubits involved in this example are stored in adjacent patches, i.e., it is local. Another useful operation is a SWAP of a pair of qubits stored in nearby patches. The surface code’s move operation shown in Figure 1 gives a straightforward way to implement this as shown in Figure 3b. With these implementations, the CNOT requires one ancilla, while SWAP requires two. Both are depth 2.

2.3 Long-range CNOT using SWAP gates

Typical input circuits for surface code compilation will involve CNOT operations on pairs of qubits that are far apart after layout. A very intuitive approach to apply a long-range CNOT(q1, q2) gate is shown in Figure 4. This involves making use of SWAP gates to first move the qubits q1 and q2 so that they are near one another, and then use the local CNOT gate in Figure 3a. Let the path \( P = v_1 v_2 \ldots v_k \), for \( k \in \mathbb{N} \), where \( v_1 = q_1 \) and \( v_k = q_2 \). As each swap has depth 2, we get a circuit of depth \( 2\left\lceil \frac{k-1}{2} \right\rceil \) since we can perform swaps on either end simultaneously. Afterwards, the two qubits are adjacent and we simply perform a CNOT in depth 2.
A cnot gate can be implemented in depth 2 using ZZ and XX joint measurements with a $|+\rangle$ ancilla state, followed by classically controlled Pauli corrections. The swap gate can be implemented using four move operations and two ancillas in depth 2.

A non-local cnot can be implemented using swaps which takes depth $2\lceil\frac{k-1}{2}\rceil$ using a zig-zag of ancilla patches along the path $P$ of length $k$. The figure shows the case when $k$ is odd and SWAPs depth is $2(k - 1)$. The patches on the path can store other logical information, which will simply be moved during the swap gates. The patches adjacent to the path are ancillas which are used to implemented the swap gates.

A lower bound on the depth it takes to perform a long-range cnot gate using swaps is proportional to the length of the shortest $q_1$-$q_2$ path. To move a qubit $k$ patches using SWAPS takes depth exactly $2k$. Therefore, to move control and target to the middle of the shortest path connecting them, it must take time proportional to at least half the length of the path.

2.4 Long-range CNOT using a Bell pair

A circuit component that we make extensive use of in this paper is the long-range CNOT using a Bell pair [LO17]. This allows us to apply CNOTs in depth 2 between any pair of qubits (provided there is a path of ancilla qubits which connects them).

To understand the construction, we first show in Figure 5a how to prepare a longer-range Bell pair from two Bell pairs. By iterating this construction one can form a circuit to prepare a long-range Bell pair at the ends of any path of adjacent ancilla patches in depth 2. Next, we show in Figure 5b how to implement a CNOT operation between qubits stored in patches neighboring a
Preparing a longer-range Bell pair

A long-range CNOT can be implemented in depth 2 by first preparing a Bell pair. (a) Joining Bell pairs with Bell measurements. This can be iterated to form a long-range Bell pair along any path of ancillas in depth 2. (b) A Bell pair can be used to apply a CNOT. (c,d) The first and second steps of a depth-2 circuit that implements a CNOT between a pair of patches at the end of a path of ancilla patches by preparing and consuming a Bell pair.

Figure 5: A long-range CNOT can be implemented in depth 2 by first preparing a Bell pair. (a) Joining Bell pairs with Bell measurements. This can be iterated to form a long-range Bell pair along any path of ancillas in depth 2. (b) A Bell pair can be used to apply a CNOT. (c,d) The first and second steps of a depth-2 circuit that implements a CNOT between a pair of patches at the end of a path of ancilla patches by preparing and consuming a Bell pair.

3 Parallel long-range CNOTs using Bell pairs

Here, we generalize the use of Bell pairs from the setting of compiling an individual non-local CNOT gate into surface code operations to the setting in which a set of parallel non-local CNOT gates are compiled. In Figure 1 and the circuit components in Section 2, ancilla qubits are used to perform some operations on data qubits. To consider the compilation on large sets of qubits,
we must specify the location of data and ancilla qubits: here we assume a 1 data to 3 ancilla qubit ratio, as illustrated in Figure 7.

In Section 3.1 we discuss some relevant background on sets of vertex-disjoint paths (VDP) and sets of edge-disjoint paths (EDP) in graphs. Then in Section 3.2 we define the VDP subroutine and the EDP subroutine that apply parallel CNOT gates at the ends of a particular type of VDP or EDP set. In Section 3.3, we show how to use the EDP subroutine to compile more general CNOT circuits and prove bounds on the performance of this approach.

3.1 Vertex-disjoint paths (VDP) and edge-disjoint paths (EDP)

In Section 2.4 we saw that a long-range CNOT could be implemented with the use of a Bell pair produced with a path of ancilla qubits connecting the control and target of the CNOT. A barrier to implement multiple CNOTs simultaneously can arise when an ancilla resides in the paths associated with multiple different CNOTs. This motivates us to review some relevant theoretical background concerning sets of paths on graphs.

Given a graph $G$, a set of paths $P$ is said to be a vertex-disjoint-path (VDP) set if no pair of paths in $P$ share a vertex, and an edge-disjoint-path (EDP) set if no pair of paths in $P$ share an edge. Note that a set of vertex-disjoint paths is also edge-disjoint. Further consider a set of terminal pairs $T = \{(s_1, t_1), \ldots, (s_k, t_k)\}$ for terminals $s_i, t_i \in V(G)$, the vertices of $G$, and $i \in [k]$. We then say that a set of paths $P$ is a VDP set for $T$ (respectively an EDP set for $T$) if $P$ is a VDP set (respectively an EDP set), and each path in $P$ connects a distinct pair in $T$. These path sets do not necessarily connect all pairs in $T$. In what follows, we pay special attention to the square grid graph (see Figure 9a). The grid graph is relevant for qubits in the surface code as shown in Figure 1, where the vertices correspond to code patches and edge connect vertices associated with adjacent patches.

The problems of finding a maximum (cardinality) VDP set for $T$ or a maximum EDP set for $T$ have been well-studied and there are known efficient algorithms capable of finding approximate solutions to each. Unfortunately, on grids it is particularly hard to approximate the maximum VDP set. In particular, for $N := |V(G)|$ there exist terminal sets for which no efficient algorithm can find an approximate solution to within a $2^{O(\log^{1-\epsilon} N)}$ factor of the maximum set size for any $\epsilon > 0$, unless $\text{NP} \subseteq \text{RTIME}(N^{\text{poly log } N})$ [CKN18]. However, efficient algorithms are available if one is willing to accept a looser approximation to the optimal solution. For example, a simple greedy algorithm is an $O(\sqrt{N})$-approximation algorithm for finding the maximum VDP set [KS04; KT06a], i.e., it produces a VDP set to within an $O(\sqrt{N})$ multiplicative factor of the optimal solution for any graph, not just the grid. For grids, the best efficient algorithm

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1Later we will consider a modification of the square grid graph because our algorithms require some further restrictions on the paths, for example preventing them from passing through those vertices associated with data qubits. It is unclear if all of the results in this section also apply for these modified graphs.
that is known is an $\tilde{O}(N^{1/4})$-approximation algorithm [CK15], where $\tilde{O}(\cdot)$ hides logarithmic factors of $O(\cdot)$.

The situation is better for approximation algorithms of the maximum EDP set: There is a $\Theta(\sqrt{N})$-approximation algorithm [CKS06] for any graph, and on grids Aumann and Rabani [AR95] showed an $O(\log N)$-approximation algorithm that was later improved to an $O(1)$-approximation algorithm [KT95; Kle96]. In practice, these algorithms can be technical to implement and can have large constant prefactors in their solutions that can be prohibitive for the instance sizes that we consider. A simple greedy algorithm forms a $O(\sqrt{N})$-approximation algorithm [KS04] for finding a maximum EDP set on the two-dimensional grid and does not suffer from the constant prefactors of the asymptotically superior alternatives. The dominant runtime complexity of this greedy algorithm is mainly in finding shortest paths for each terminal pair, giving a $O(|T| N \log N)$ runtime upper bound by Dijkstra’s algorithm$^2$.

It is informative to consider the comparative size of the maximum EDP and VDP sets for the same terminal set $T$. Since any VDP set is also an EDP set, the size of the maximum VDP set for $T$ cannot be larger than the maximum EDP set for $T$. Moreover, one can construct some cases of $T$ on the grid [Kle96] in which the maximum EDP set is a factor $\sqrt{N}$ larger than the maximum VDP set [Kle96]. For example, consider the set of terminal pairs $T = \{(i, 1), (L, i) \mid i \in [L]\}$ of an $L \times L$ grid graph, where vertex $(i, j)$ denotes the vertex in row $i$ and column $j$. All terminals can be connected by edge-disjoint paths but the maximum VDP set is of size one.

In Section 3.2, we show that both VDP and EDP sets for $T$ can be used to form constant-depth compilation subroutines for disjoint cnot circuits. Ultimately, as will become clear in Section 3.2, each path in the EDP or VDP sets for $T$ allows us to implement one more cnot gate in parallel by a compilation subroutine. In this work, we focus on EDPs rather than VDPs for two main reasons. Firstly, as mentioned above, better approximation algorithms exist for finding maximum EDP sets than for finding maximum VDP sets on the grid. Although, in practice, we make use of the greedy $O(\sqrt{N})$-approximation algorithm for finding maximum EDP sets in this work. Secondly, as was also mentioned above, the maximum EDP set is at least as large as the maximum VDP set.

An important open problem that could ultimately influence the performance of the surface code compilation algorithm we present in this work is whether an alternative approximation algorithm for finding maximum EDP sets can be used that performs better in practical instances.

### 3.2 Long-range cnot subroutines using VDP and EDP

Here we present one of our main technical contributions, namely a description of how to implement a set of long-range cnots at the end of VDP and EDP

$^2$It may be possible to improve the runtime by using a decremental dynamic all-pair shortest path algorithm; it may be quicker to maintain a data structure for all shortest paths that can quickly be updated when edges are removed.
sets using surface code operations. This is central to our overall surface code compilation algorithm presented in Section 5.

Consider the $L \times L$ square grid graph $G$ (see Figure 9a), which consists of vertices $V(G) = [L] \times [L]$, for $[L] := \{1, \ldots, L\}$ and undirected edges

$$E(G) = \{(i,j), (i,j+1) \mid i \in [L], j \in [L-1]\} \cup \{(i,j), (i+1,j) \mid i \in [L-1], j \in [L]\}. \quad (1)$$

Here, vertices correspond to qubits stored in surface code patches, and edges connect qubits on adjacent patches (see Figure 1). We color the vertices of $G$ with three colors: black, grey, and white (see Figure 7). All vertices with both even row and even column index are colored black and correspond to data qubits (where data qubits correspond to qubits in the input circuit). The vertices (corresponding to ancilla qubits) with both odd row and odd column index are colored white, and all remaining vertices are colored grey. This gives us a $1 : 3$ data qubit to ancilla qubit ratio. We set $n$ to equal the number of black vertices, i.e., the number of data qubits.

Due to the designation of some vertices as data qubits and others as ancilla vertices in our layout, and due to the asymmetry of two-qubit operations along horizontal and vertical edges in Figure 1, we add some restrictions to the paths we consider. We define an operator path to be a path $P = v_1v_2 \ldots v_k$, for $k \in \mathbb{N}$, such that $v_1$ and $v_k$ correspond to data qubits and its interior $v_2 \ldots v_{k-1}$ are all ancilla qubits. Moreover, $v_1$ to $v_2$ must be a vertical edge, and $v_{k-1}$ to $v_k$ must be a horizontal edge. Then an operator VDP (resp. EDP) set is a set of vertex-disjoint (resp. edge-disjoint) operator paths. In addition, we require that the ends of the paths in the operator EDP set do not overlap. With the coloring assignments of the grid graph $G$, it is easy to see that the first and last vertex of an operator path are colored black. In what follows, we show how we can implement CNOTs between the data qubits at the ends of the paths in an operator VDP (EDP) set in constant depth.

First consider an operator VDP set $P$. It is straightforward to see that we can simultaneously apply long-range CNOTs along each $P \in P$ as in Figure 5 in depth 2. We call this the vertex-disjoint paths subroutine (VDP subroutine).

Now consider an operator EDP set $P$. An EDP set can have intersecting paths, and the ancilla qubits at intersections appear in multiple paths, preventing us from simultaneously producing Bell pairs at their ends. We circumvent this by producing Bell pairs across a path in two stages by splitting the path into segments; see Figure 6. We will show that $P$ can be fragmented into two VDP sets $P_1$ and $P_2$ that, together, form $P$. More precisely, each path $P \in P$ can be built by composing paths contained in $P_1$ and $P_2$ such that each path in either $P_1$ or $P_2$ appears in precisely one path in $P$. We say that the paths in $P_1$ and $P_2$ are segments of paths in $P$. This forms the basis of the edge-disjoint paths subroutine (EDP subroutine), which is presented in Algorithm 3.1 and illustrated with an example in Figure 7.

We show the following Lemma, which restricts the adjacency of crossing vertices. As will become clear later, the adjacent crossing vertices impose systems
of constraints on fragmenting $\mathcal{P}$, and their restricted adjacency of any operator EDP set ensures a fragmentation into two VDP sets always exists.

**Lemma 3.1.** Given an operator EDP set $\mathcal{P}$, a crossing vertex is a vertex contained in more than one path in $\mathcal{P}$. Let the set of crossing vertices be $V_c$, then the induced subgraph $G[V_c]$ contains only three kinds of connected components:

1. **Isolated vertices.**

2. **A horizontal path,** where each vertex $(i, j)$ in the connected component can only be adjacent to $(i - 1, j)$ and $(i + 1, j)$.

3. **A vertical path,** where each vertex $(i, j)$ in the connected component can only be adjacent to $(i, j - 1)$ and $(i, j + 1)$.

**Proof.** We consider all possible colors of a vertex $(i, j)$ in a connected component of $G[V_c]$. Black vertices cannot be crossing vertices by definition of an operator EDP set so cannot be contained in $V_c$. It is then easy to see that white vertices in $V_c$ satisfy the Lemma.

Therefore, the only relevant case is when $(i, j)$ is a grey vertex. The vertices $(i + 1, j)$ and $(i, j + 1)$ are white and $(i + 1, j + 1)$ is black. We show that these
The EDP subroutine implements a set of parallel CNOTs connected by an operator EDP set. We assume a qubit ratio of 1 to 3 of data (black) to ancilla (gray and white). (a) The input to the EDP subroutine is a set of CNOTs and an associated EDP set. (b) We fragment the EDP set into two VDP sets consisting of segments of the original paths, and implement the compiled circuit over two depth-2 stages, one for each of these sets. (c) During the first stage we prepare a Bell pair between the ends of the segments in the first VDP set. (d) During the second stage we perform joint Bell measurements between the ends of segments in the second VDP set, producing long-range Bell pairs on ancillas adjacent to the control and target of each CNOT. Then, long-range CNOTs can easily be applied by using the long-range Bell pairs (Section 2.4). See Figures 6 and 8 for further details of the long-range operations used here.
Figure 8: Detailed implementation of the steps in Figure 7. For each segment that is scheduled in phase 1, we use (b) and (c); and for each subpath that is scheduled in phase 2, we use (d) and (e). In (d) variables $x_0$ and $z_0$ equal to the total parity of all long-range Bell measurements applied during stage 2 on the CNOT path. Each of these operations takes depth 2. (d) and (e) share the variables $a$ and $c$. 
Algorithm 3.1: **EDP subroutine**: to apply CNOTs to the data qubits at the endpoints of a set of edge-disjoint paths $P$, where the interior of each path is supported on ancilla qubits. The depth is at most 4.

**Input**: An operator EDP set $P$

1. $P_1, P_2 \leftarrow$ fragment $P$ in two VDP sets of segments // **Theorem 3.2**

2. **for** segment $P \in P_1$:
   3. **if** $P$ connects two data qubits **then**
   4. **execute** long-range CNOT along $P$
   5. **else**
   6. **execute** phase 1 operation along $P$ (Figure 6a, or 8b, or 8c)

7. **for** segment $P \in P_2$:
   8. **if** $P$ connects two data qubits **then**
   9. **execute** long-range CNOT along $P$
  10. **else**
  11. **execute** phase 2 operation along $P$ (Figure 6b, or 8d, or 8c)

We now prove that $P$ can be fragmented.

**Theorem 3.2.** We can fragment an operator EDP set $P$ to produce vertex-disjoint sets of segments $P_1$ and $P_2$. If $P$ is vertex-disjoint, then $P_1 = P$ and $P_2 = \emptyset$.

**Proof.** We assign edges for inclusion in segments in $P_1$ or $P_2$ by an edge labelling $l(e): E(G) \to \{1, 2\}$. Given a labelling of all edges $e$ in the paths of $P$, we can assign edges $l(e) = b$ to segments in $P_b$. Therefore, given a labelling of all edges in paths in $P$, it is easy to construct $P_1$ and $P_2$. We now label all edge in the paths in $P$ and prove that their labelling guarantees the vertex-disjointness property of $P_1$ and $P_2$.

We constrain the labeling around every crossing vertex $v$ so that the VDP property is satisfied. Clearly, $v$ is contained in the interior of exactly two paths, $P_1$ and $P_2$. Let $v$ be contained in edges $e_1$ and $e'_1$ of $P_1$, and edges $e_2$ and $e'_2$ of $P_2$, then we impose the constraints

\begin{align*}
l(e_1) &= l(e'_1) \\
l(e_2) &= l(e'_2) \\
l(e_1) &\neq l(e_2)
\end{align*}
guaranteeing the vertex-disjointness of segments at \( v \) since a segment of \( P_1 \) must span both \( e_1 \) and \( e'_1 \), and a segment of \( P_2 \) must span both \( e_2 \) and \( e'_2 \) with a different label.

We show there always exists a feasible solution given these constraints. If we consider the graph \( G[V_c] \) induced by crossing vertices \( V_c \), then we see that every connected component in \( G[V_c] \) gives a system of constraints. The adjacency of \( G[V_c] \), by Lemma 3.1, is such that each system has one degree of freedom, which we decide arbitrarily.

Finally, for every vertex-disjoint path \( P \in \mathcal{P} \), assign \( l(e) = 1 \) to all edges \( e \) in \( P \). All remaining edges can be labeled arbitrarily.

The depth of a CNOT circuit produced by the EDP subroutine for an operator EDP set \( \mathcal{P} \) is at most 4. If \( \mathcal{P} \) happens to be vertex-disjoint, then the depth is 2 since all paths are assigned to phase 1 by Theorem 3.2.

### 3.3 Compiling parallel CNOT circuits with the EDP subroutine

In this section we consider how to compile input parallel CNOT circuits using the EDP subroutine. We define the terminal pairs \( T \subseteq V(G) \times V(G) \) to be the pairs of control and target qubits for each CNOT gate in the parallel CNOT circuit. To use the EDP subroutine, we need to find operator EDP sets \( \mathcal{P}_1, \ldots, \mathcal{P}_k \) that connect all terminal pairs in \( T \). We will refer to any such set \( \{\mathcal{P}_1, \ldots, \mathcal{P}_k\} \) as a \( T \)-operator set. The depth of the compiled implementation is minimized when the size \( k \) of the \( T \)-operator set is minimized.

There are reasons to believe that the compilation strategy for parallel CNOT-circuits formed by finding a minimal \( T \)-operator set and applying the EDP subroutine should produce low-depth output circuits. For sparse input circuits, i.e. those with a small number of CNOTs, one can expect a small \( T \)-operator set to exist, giving a low depth output. On the other hand, we now prove that there are dense CNOT circuits for which the EDP subroutine with a minimal size \( T \)-operator set produces a compiled circuit with optimal depth (up to a constant multiplicative factor).

**Theorem 3.3.** Let a parallel input CNOT circuit with corresponding terminal pairs \( T \) be given, and let the \( n \) qubits of the input circuit be embedded in a grid among \( 3n \) ancilla qubits according to the layout in Figure 7. For simplicity, we assume \( n \) is both even and the square of an integer. We can find a \( T \)-operator set of size at most \( 2\sqrt{n} - 1 \) in polynomial time.

**Proof.** For each CNOT we construct an operator path and argue that all such paths can be grouped into \( O(\sqrt{n}) \) disjoint EDP sets. For simplicity, in the following, we specify paths by a sequence of key vertices, with each consecutive pair of key vertices connected by the shortest path (which is a horizontal or a vertical line).

We now construct an operator path for each CNOT, where the associated control vertex is \( v = (v_x, v_y) \in V(G) \) and the target vertex is \( u = (u_x, u_y) \in \).
We can always form an operator path to connect $u$ and $v$ given by the following sequence of five key vertices $v$, $(v_x, v_y - 1)$, $(u_x - 1, v_y - 1)$, $(u_x - 1, u_y)$, $u$. This path consists of one vertical end segment, one horizontal interior segment, one vertical interior segment, and finally a horizontal end segment.

Having assigned a path to each CNOT, we now show that any of these operator paths can share an edge with at most $2(\sqrt{n} - 1)$ of the other paths. Since the operator paths have distinct endpoints, two different paths cannot share an edge on either of their end segments $v$, $(v_x, v_y - 1)$ and on $(u_x - 1, u_y)$, $u$. Therefore pairs of these operator paths can only share an edge on their interior segments. The horizontal interior segment of the operator path from $v$ to $u$ can share an edge with at most $\sqrt{n} - 1$ other paths. To see this, consider an operator path from $v' = (v'_x, v'_y) \in V(G)$ to $u' = (u'_x, u'_y) \in V(G)$ that shares at least one horizontal edge with the operator path from $v$ to $u$. Explicitly, that means the segment $(v_x, v_y - 1)$, $(u_x - 1, v_y - 1)$ shares an edge with the segment $(v'_x, v'_y - 1)$, $(u'_x - 1, v'_y - 1)$, which implies that $v_y = v'_y$. Since the terminals are unique, there can only be $\sqrt{n} - 1$ other CNOTs with the control sharing the $v_y$ coordinate. An analogous argument applies for vertical segments, such that the operator path from $u$ to $v$ can share an edge with at most $2(\sqrt{n} - 1)$ other operator paths.

Let us construct a graph $H$ where each vertex represents an operator path as constructed above. We connect two vertices in $H$ if the associated paths share an edge. Every vertex in $H$ has degree at most $2(\sqrt{n} - 1)$, therefore, $H$ is $(2\sqrt{n} - 1)$-colorable using the (polynomial time) greedy coloring algorithm. We construct a $T$-operator set of size $2\sqrt{n} - 1$ by grouping the paths associated with each color in a set of edge-disjoint paths.

We now show a general lower bound on compiling parallel CNOT circuits to the surface code architecture. Our strategy will be to consider a parallel CNOT circuit with control data qubits in an area with small boundary that generates an amount of entanglement across the boundary proportional to the area for a given initial state. However, each elementary surface code operation is local such that only those operations acting at the boundary can increase the entanglement across it. The depth of any implementation of the CNOT circuit is then lower bounded by the entanglement that it generates over the boundary size [DBT21; Bap+22].

**Theorem 3.4.** Consider a surface code architecture of $n$ data qubits embedded in a grid where all ancilla qubits are in the $|0\rangle$ state. For any positive integer $k \leq n/2$, there exists a parallel CNOT circuit of $k$ CNOT gates with associated terminal pairs $T$ that needs depth $\Omega(\sqrt{k})$ to be implemented on the surface code architecture.

**Proof.** Consider a CNOT circuit with terminal pairs $T$ with control qubits on data vertices in a square region, $V_L$, and target qubits on vertices outside $V_L$. We initialize the $2k$ data qubits associated with $T$ to a product state $|+\rangle^k|0\rangle^k$, with $|+\rangle$ on control qubits and $|0\rangle$ on target qubits (the remaining data qubits are initialized in an arbitrary product state and ignored). After applying the
CNOT circuit, we obtain $k$ Bell pairs. Therefore, the (von Neumann) entropy of the reduced state of the data qubits in $V_L$ has increased from 0 to $k$.

Consider a circuit $C$ of depth $d$ that implements the parallel CNOT circuit. Any elementary operation of the surface code acting only within $V_L$ or within $\bar{V}_L := V(G) \setminus V_L$ or classical communication (together, LOCC) cannot increase the entropy of the state on $V_L$. Moreover, as we show below, each elementary operation that acts both on $V_L$ and on $\bar{V}_L$ can increase the entropy by at most a constant 4. We can therefore upper bound the increase in entropy due to $C$ by $4d$ times the number of vertices adjacent to $V_L$, which is proportional to $\sqrt{k}$. To attain the $k$ increase in entropy, we therefore need that $d = \Omega(\sqrt{k})$.

We now bound the increase in entropy of any elementary operations acting on $V_L$ and $\bar{V}_L$ to at most 4. All such elementary operations are built from a single XX or a ZZ measurements and single qubit operations Appendix A, which cannot increase the entropy. It is possible to implement XX and ZZ measurements acting on $V_L$ and $\bar{V}_L$ using two CNOTs and operations acting only within $V_L$ or within $\bar{V}_L$. The increase in entropy in $V_L$ by a CNOT operation is bounded by 2 [Ben+03, Lemma 1]. Therefore, XX measurements, ZZ measurements, and indeed any elementary operation of the surface code can increase the entropy by at most 4.

In practice, it can be difficult to find minimal-size $T$-operator sets. However, when the minimal size $T$-operator set is $k$, in the following theorem we show that a $T$-operator set $\{P_1, \ldots, P_l\}$ with size at most $l = O(k \log |T|)$ can be found by a greedy algorithm that finds iteratively finds the maximum operator EDP set for remaining terminals in $T$.

**Theorem 3.5.** On the grid of $n$ vertices, the greedy algorithm for finding $T$-operator sets repeats the following two steps, for $i = 1, \ldots$, until there are no more terminal pairs to connect:

1. find a maximum operator EDP set $P_i$,
2. remove all terminal pairs in $P_i$ from $T$.

The set $\{P_1, \ldots, P_k\}$ is a $T$-operator set and is an $O(\log |T|)$-approximation algorithm for finding minimum-size $T$-operator sets.

**Proof.** We base our proof on [AR95]. Assume that the minimum-size $T$-operator set is $\{Q_1, \ldots, Q_K\}$ for some size $K$. Then there is an operator EDP set $Q_i$, for $i \in [K]$, such that $|Q_i| \geq |T|/K$. Therefore, the number of unconnected terminal pairs is reduced by at least a factor $(1 - 1/K)$ each iteration and it will require at most $O(K \log |T|)$ iterations to connect all terminal pairs [Joh74].

To make use of Theorem 3.5 we would ideally like to have an algorithm to find maximum operator EDP sets on the grid, however the efficient algorithms we discussed in Section 3.1 fall short of this in two ways. Firstly they find EDP sets rather than operator EDP sets, and secondly they provide approximate maximum sets rather than maximum sets. Fortunately, we find an equivalence
between operator EDP sets on the grid and EDP sets on a graph that we call the $\mathcal{T}$-operator graph (see Figure 9b). The $\mathcal{T}$-operator graph is a copy of the grid graph but with all vertices corresponding to control qubits in $\mathcal{T}$ only having vertical outgoing edges, and with all vertices corresponding to target qubits in $\mathcal{T}$ only having horizontal incoming edges, and all remaining vertices corresponding to data qubits are removed. An EDP set for terminal pairs $\mathcal{T}$ on the $\mathcal{T}$-operator graph is an operator EDP set on the grid. It is easy to see that a maximum operator EDP set for $\mathcal{T}$ on the grid is equivalent to a maximum EDP set for $\mathcal{T}$ on the $\mathcal{T}$-operator graph. Using an approximation algorithm for finding the maximum operator EDP set also still gives approximation guarantees for minimizing the $\mathcal{T}$-operator set, as shown in the following Corollary.

**Corollary 3.6.** The greedy algorithm for finding minimum $\mathcal{T}$-operator sets, but with a $\kappa$-approximation algorithm for finding maximum operator EDP sets, gives an $O(\kappa \log |\mathcal{T}|)$-approximation algorithm for finding minimum $\mathcal{T}$-operator sets.

**Proof.** We modify the proof of Theorem 3.5 such that every iteration we connect a $(1 - \kappa/K)$ fraction of unconnected terminal pairs using the $\kappa$-approximation algorithm for finding maximum operator EDP sets. Therefore we obtain a $O(\kappa \log |\mathcal{T}|)$-approximation algorithm for finding minimum $\mathcal{T}$-operator sets. □

The equivalence between operator EDP sets on the grid and EDP sets on the $\mathcal{T}$-operator graph motivates us to seek an efficient algorithm to find approximate maximum EDP sets on the $\mathcal{T}$-operator graph as a key part of our EDPC algorithm. The algorithms we discussed in Section 3.1 come close to doing this, but some of them are intended for finding approximate maximum EDP sets on the grid rather than on the $\mathcal{T}$-operator graph and even if they are adapted, the guarantees of the size of the approximate minimum EDP sets they produce...
Algorithm 3.2: Bounded $\mathcal{T}$-operator set algorithm: An approximation algorithm for minimizing the $\mathcal{T}$-operator set size that combines the theoretical guarantees from Theorem 3.3 with pragmatic performance using the greedy algorithm of Theorem 3.5.

| Input |
|-------|
| $\mathcal{T}$ terminal pairs |

| 1 | $Q_1 \leftarrow$ the $\mathcal{T}$-operator set given by Theorem 3.3 for $\mathcal{T}$ |
| 2 | $Q_2 \leftarrow \emptyset$ |
| 3 | while $\mathcal{T} \neq \emptyset$: // Greedy apx. minimum-size $\mathcal{T}$-operator set |
| 4 | $P \leftarrow$ approximately maximize operator EDP set using greedy EDP algorithm [KS04] on operator graph |
| 5 | remove connected terminal pairs in $P$ from $\mathcal{T}$ |
| 6 | $Q_2 \leftarrow Q_2 \cup \{P\}$ |
| 7 | return minimum-size set between $Q_1$ and $Q_2$ |

may not apply in the case of the $\mathcal{T}$-operator graph. The algorithms described in Refs. [AR95; KT95] for finding approximate maximum EDP sets on the grid do not directly apply to the operator graph. While it seems straightforward to adapt the $O(\log n)$-approximation algorithm [AR95], the algorithms in [AR95; KT95] are complex to implement and have large constant-factor overheads, which can make them impractical on small instance sizes.

In EDPC, we instead combine the theoretical worst-case bounds of Theorem 3.3 with the pragmatic performance of a greedy approach, which does not have a large constant overhead, in Algorithm 3.2. By Theorem 3.4 this gives us asymptotically tight performance in the worst-case. The runtime of this algorithm is dominated by $O(|\mathcal{T}|)$ iterations of approximately maximizing the operator EDP set in time $O(|\mathcal{T}| n \log n)$. We leave it as an open question to find better approximation algorithms for finding maximum operator EDP sets that give improved performance outside the worst-case and that may also improve the runtime since less iterations over $\mathcal{T}$ are required.

4 Remote rotations with magic states

Thus far we have discussed the surface code compilation of all the input circuit operations listed in Section 1 except for the single-qubit rotation gates $S = Z(\pi/4)$ and $T = Z(\pi/8)$. In this section we design a subroutine for the compilation of parallel rotation circuits. The $S$ and $T$ gates can be implemented by using specially prepared magic states $|S\rangle$ and $|T\rangle$, respectively. Magic states can be prepared using a highly-optimized process known as magic state distillation [Kni04], which distills many faulty magic states that are easy to prepare into fewer robust states. Still, producing both $|S\rangle$ and $|T\rangle$ involves considerable overhead. The $|S\rangle$ state is used to apply the $S$-gate in a ‘catalytic’ fashion, whereby the state $|S\rangle$ is returned afterwards. On the other hand, the state $|T\rangle$ is consumed to apply the $T$-gate. The reason for this distinction is rooted in the
Figure 10: We assume the capability of performing $S$ and $T$ gates at the boundary qubits (red) where it is easy for us to supply the requisite $S$ and $T$ magic states. We can then execute $S$ or $T$ gates in the $Z$ or $X$ basis for our circuit by using long range CNOTS and the circuits in Figure 10b. For example, to execute $S$ or $T$ on qubits G3, E7 and HTH on G7, we apply long-range CNOTs between pairs (G3,G1), (E7,A7), (A5,G7) and then execute $S$ or $T$ on G1, A7, HTH on A5. We can continue applying other Clifford gates to qubits G3, E7, and G7 right after performing the long-range CNOT, without waiting for the $Z$ correction, since we can propagate the correction through Clifford operations.

In this work, we do not address the mechanism by which magic states are produced, but instead assume that these states are provided at specific locations where they can be used to implement gates. More specifically, we assume rotation gates $S$ and $T$ (and also Clifford variations of these such as $X(\pi/8) = T_x$ and $X(\pi/4) = S_x$) can be applied as a resource on specific ancilla qubits $B \subseteq V(G)$ at the boundary of a large array of logical qubits (Figure 10a). This will allow sufficient space outside the boundary where highly-optimized magic state distillation and synthesis circuits can be implemented. Because a large number of magic states are used in the computation, we consider having magic state distillation adjacent to and concurrent with computation we are concerned with in this paper to be a reasonable allocation of resources.

We need a technique to apply remote rotations to data qubits which can be far from the boundary making use of the rotations that can be performed at the boundary. We make use of the property that any $Z$ rotation (including $T$ or $S$) has the same action when applied to either qubit in the state $\alpha|00\rangle + \beta|11\rangle$. In particular, these two qubits need not be close to one another, so we can apply $Z$ rotations remotely. A similar notion holds for $X$-rotations (including $T_x = HTH$ or $S_x = HSH$) and $\alpha|++\rangle + \beta|--\rangle$. Given a qubit $q$ that needs to perform a $Z$ rotation requiring a magic state, we apply a remote $Z$-rotation (Figure 10b): by
performing a long-range CNOT\((q, q')\) to a boundary ancilla \(q' \in B\) prepared in \(|0\rangle\). Therefore we can apply the \(Z\) rotation remotely and use an \(X\) measurement on \(q'\) to collapse the state back to one logical qubit. Similarly, for a qubit \(q\) that needs to perform an \(X\) rotation requiring a magic state, we apply a long-range CNOT\((q', q)\) to an ancilla \(q'\) prepared in \(|+\rangle\) on the boundary, giving

\[
\text{CNOT}|+\rangle(\alpha|+\rangle + \beta|--\rangle) = \alpha|++\rangle + \beta|--\rangle. \tag{5}
\]

Therefore we apply the \(X\) rotation remotely and collapse the state back by a single-qubit \(Z\) measurement of \(q'\).

The task of compiling a parallel rotation circuit therefore reduces to applying a set of CNOT gates from the boundary to the sites of the rotation gates. This can be achieved by finding an appropriate EDP set and running the EDP subroutine of Algorithm 3.1. Compared to the task of finding an EDP set for parallel CNOT gates of Section 3, there is one simplifying condition here: Any boundary qubit can be used for each CNOT when applying remote rotations. As we explain below, we can find the maximum EDP set for the compilation of remote rotations by solving the following (unit) MAX FLOW problem [KT06b].

**Definition 4.1 (MAX FLOW).** Given a directed graph \(G\) and source and sink vertices \(s, t \in V\), we wish to find a flow for all edges of \(G\), \(f(e): E(G) \to \mathbb{R}\), that is skew symmetric, \(f((u, v)) = -f((v, u))\), and, for \(v \in V(G) \setminus \{s, t\}\), must respect the constraints

\[
f(e) \leq 1 \tag{6}
\]

and

\[
\sum_{u:(v, u) \in E(G)} f((v, u)) = 0 \tag{7}
\]

such that the outgoing source flow \(|f| := \sum_{(s, u) \in E(G)} f((s, u))\) is maximized.

To understand why this yields a maximum EDP, we first point out that a solution for which \(f\) has binary values provides an EDP set by building paths from those edges \(e\) for which \(f(e) = 1\). Moreover, this EDP set must be maximum, because a larger EDP set would imply a larger flow than \(f\), which is the maximum flow by definition. Indeed the Ford-Fulkerson algorithm [FF56] solves MAX FLOW in runtime bounded by \(O(|E(G)||f|)\) and finds flow values \(f(e) \in \{0, 1\}\) on all \(e \in E(G)\) because of the unit capacity constraints, \(f(e) \leq 1\). Therefore, \(f\) corresponds to a maximum EDP set [KT06b, Section 7.6].

The **remote rotation subroutine** (Algorithm 4.1) executes a set of parallel single-qubit rotations. Each iteration can be performed in depth 4 using the EDP subroutine. On the surface code architecture, we can give strong guarantees on the number of iterations required to execute a set of parallel rotations by the MAX FLOW to min-cut equivalence.

**Theorem 4.2.** The remote rotation subroutine executes all rotations in \(G_m\) in depth \(O(\sqrt{|\mathcal{G}_m|})\).
Algorithm 4.1: Remote rotation subroutine: executes parallel single qubit rotations that require magic states at the boundary by a MAX FLOW reduction. Using the EDP subroutine (Algorithm 3.1), we can perform remote rotations (Figure 10) on each set of qubits connected to the boundary by $P$ in depth 4.

**Input**: Connectivity graph $G$ with vertices corresponding to boundary qubits $B \subseteq V(G)$ and a set of parallel rotations $G_m$

1. function $\text{max\_rotations}(G_m)$:
2. $W \leftarrow$ vertices associated with qubits in $G_m$
3. create virtual vertices $s$ and $t$
4. $G' = (V(G) \cup \{s, t\}, E(G) \cup \{(s, s') \mid s' \in W\} \cup \{(t', t) \mid t' \in B\})$
5. $f \leftarrow$ solve MAX FLOW on $G'$ using the Ford-Fulkerson algorithm
6. $P \leftarrow$ construct edge-disjoint set of $s$–$t$ paths from $f$
7. return $P$ with $s$ and $t$ removed from each $P \in P$
8. while $G_m$ is not empty:
9. $P \leftarrow \text{max\_rotations}(G_m)$
10. execute remote rotations at boundary with EDP subroutine given $P$
11. remove executed rotations from $G_m$

**Proof.** The function $\text{max\_rotations}(G_m)$ that is a part of the remote rotation subroutine finds a maximum flow connecting the data qubits performing rotations to the boundary where every additional unit of flow is one more rotation executed. This maximum flow is equal to the minimum edge-cut separating the data qubits from the boundary [FF56]. The boundary of a rectangle containing $|G_m|$ vertices on the grid is of size $\Omega(\sqrt{|G_m|})$, giving a minimum cut size of $\Omega(\sqrt{|G_m|})$. Thus, at most $O(\sqrt{|G_m|})$ iterations of the while loop in the remote rotation subroutine are necessary to implement all remote rotations, as claimed.

We bound the runtime of the remote remote rotation subroutine by $O(n^2 \sqrt{|G_m|})$ as follows: At most $O(\sqrt{|G_m|})$ iteration of the while loop are necessary (see proof of Theorem 4.2). Each iteration, the call to $\text{max\_rotations}(G_m)$ is dominated by solving a MAX FLOW instance using the Ford-Fulkerson algorithm [FF56], which has a runtime bounded by $O(n^2)$.

One could consider a number of generalizations and variations of this compilation subroutine for parallel rotation circuits. For instance, when the number of rotation gates is small, it may be useful to find VDP sets rather than EDP sets so that the VDP subroutine rather than the EDP subroutine can be applied. There is a different reduction to MAX FLOW in this case which can be obtained by replacing each vertex with two vertices, one with incoming edge and one with outgoing edges, connected by a directed edge with capacity 1. This guarantees only one flow can pass through every vertex.

Although we do not consider other single-qubit rotations in our input circuit for compilation, it is worth noting that any single-qubit rotation gate $Z(\theta)$ can be approximately synthesized to arbitrary precision [RS16] using $|S\rangle$ and $|T\rangle$. 

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Algorithm 5.1: EDPC: a surface code compilation algorithm for any circuit $C = g_1 \ldots g_\ell$. An operation $g_i$ is available if it has not been executed and all operations $g_j$ with overlapping support, for $j < i$, are executed.

| Input | Circuit $C$ with Paulis commuted to the end and merged with measurement |
|-------|------------------------------------------------------------------------|
| 1     | while available operations in $C$ :                                    |
| 2     | execute all available state preparation, measurement, and Hadamard    |
| 3     | run remote rotation subroutine on available rotations                  |
| 4     | $T \leftarrow$ terminal pairs associated with available CNOTs         |
| 5     | $Q \leftarrow$ run bounded $T$-operator set Algorithm 3.2 on $T$        |
| 6     | for $P \in Q$ :                                                        |
| 7     | | run EDP subroutine (Algorithm 3.1) on $P$                            |

states along with the surface code operations shown in Figure 1. The approach used to apply $S$ and $T$ gates shown in Figure 10a can also be used to apply any rotation $Z(\theta)$ within the grid of surface codes by synthesizing the rotation at the boundary. However, if one considers more general rotations in the input circuit, the time needed for synthesis at the boundary will need to be accounted for and accommodated by other aspects of the overall surface code compilation algorithm. Another extension that can be considered is if multi-qubit diagonal gates are allowed in the input circuit. We show how $X$ and $Z$ rotations generalize to multi-qubit diagonal gates in Appendix D, although we do not use this in our surface code compilation algorithm.

5 EDPC surface code compilation algorithm

In this section we construct the EDPC algorithm for compiling universal input circuits into surface code operations by combining subroutines Algorithm 3.1 and Algorithm 4.1 for compiling long-range CNOTs and $Z/X$ rotations respectively. First we provide a more formal definition of surface code compilation:

Definition 5.1 (Surface code compilation). Consider an input quantum circuit of operations $C = g_1 g_2 \ldots g_\ell$, which is a list of length $\ell$ of operations $g_i$ for $i \in [\ell]$, consisting of: state preparation in $X$ or $Z$ basis; the single-qubit operators $X$, $Y$, $Z$, $H$, $S$, $T$, $S_x = HSH$, $T_x = HTH$; CNOT operations; and $X$, $Z$-measurements. Then a surface code compilation produces an equivalent output circuit $O$ in terms of surface code operations (Figure 1) on a grid of surface codes with $S$, $T$, $S_x$, and $T_x$ rotations applied only at the grid’s boundary.

The surface code compilation algorithm EDPC (Algorithm 5.1) combines the bounded $T$-operator set algorithm for parallel CNOTs with the remote rotation subroutine. Note that the input circuit is considered to be a sequence of operations rather than a series of time steps that specify the
operations in each time step, such that \( l \) is the number of operations of the input circuit, not the depth.

We bound the classical runtime of EDPC given an input circuit with depth \( D \) acting on \( n \) qubits. It is useful to note that each of the \( D \) layers of the input circuit can be decomposed into a set of parallel rotations followed by a set of parallel cNOTs, each acting on at most \( n \) qubits. Recall that the remote rotation subroutine has a runtime bounded by \( O(n^{2.5}) \), whereas compiling a set of parallel cNOTs has a runtime of at most \( O(n^3 \log n) \). Thus, EDPC has a runtime bounded by \( O(Dn^3 \log n) \).

Circuits compiled by EDPC can be bounded in depth as listed in Table 1. Our claim for a single cNOT is trivial. Theorems 3.3 and 3.4 show that parallel cNOT circuits are compiled to a depth of \( \Theta(\sqrt{n}) \), and Theorem 4.2 shows that \( k \) parallel rotations are compiled to a depth of \( O(\sqrt{k}) \). It is then easy to see that a circuit of depth \( D \) compiles to a circuit of depth at most \( O(D\sqrt{n}) \). If we assume a remote rotation must be performed for each rotation requiring magic states at the boundary (in particular, it requires a long-range cNOT as in EDPC), then Theorem 3.4 shows an \( \Omega(\sqrt{k}) \) lower bound on the depth to apply \( k \) cNOT operations with the boundary.

There are various modifications of EDPC that are worth considering. Firstly, the bounded \( T \)-operator set algorithm (Algorithm 3.2) can be improved by better algorithms for finding maximum operator EDP sets. Secondly, the requirement to execute all available gates before moving on to the next set could be relaxed. This could increase the number of long-range gates that are performed in parallel but would require careful scheduling with Hadamard gate execution, which may block some paths. Lastly, EDPC leans heavily on finding operator EDP paths and the EDP subroutine, but a similar surface code compilation algorithm could be constructed from operator VDP paths and the VDP subroutine instead. We believe that larger maximum EDP sets allows EDPC to apply more gates simultaneously (see Section 3.1), and more so if algorithms for approximation maximum operator EDP sets can adopted from EDP approximation algorithms [AR95; KT95]. Both of these features can give asymptotic improvements at only a 2\times depth increase over the VDP subroutine. However, it is not difficult to construct instances where a VDP-based approach would give a lower depth, motivating a more nuanced trade-off between our EDP-based approach and a VDP-based approach.

6 Comparison of EDPC with existing approaches

In this section, we compare EDPC with other approaches in the literature. We first mention some of the features and short-comings of the well-established approach of Pauli-based computation Section 6.1. Then we address a more recently proposed compilation approach based on network coding in Section 6.2. In Section 6.3 we specify a SWAP-based compilation algorithm [CSU19] and use this as a benchmark for numerical studies of the performance of an implementation of EDPC in Section 6.4.
6.1 Surface code compilation by Pauli-based computation

One well-established surface code compilation approach is known as Pauli-based computation, which is described in [Lit19]. For an algorithm expressed in terms of Clifford and $T$ gates, Pauli-based computation first involves re-expressing the algorithm as a sequence of joint multi-qubit Pauli measurements along with additional ancilla qubits prepared in $T$ states. This re-expressed circuit has no Clifford operations, and the circuit depth can be straightforwardly deduced from the input circuit since each $T$ gate results in two [CC21] joint Pauli measurements. This re-expression of the circuit essentially comes from first replacing each $T$ gate by a small gate teleportation circuit consisting of an ancilla in a $T$ state and a two-qubit joint Pauli measurement, and then commuting all Clifford operations to the end of the circuit. The main advantage of the Pauli-based computation approach is that all Cliffords are removed from the input circuit, resulting in no cost for $\text{cnot}$ circuits in Table 1.

That said, this approach has a major drawback. When a Clifford circuit is commuted through a two-qubit joint Pauli measurement, it is transformed into Pauli measurements which can have support on all logical qubits. Therefore, the resulting circuit may contain measurements with large overlapping support that need to be performed sequentially (even when the $T$ gates in the input circuit were acting on disjoint qubits during the same time step). The sequential nature of the joint measurements causes a fixed rate of $T$-state consumption that does not grow with the number of logical qubits and results in a $\Theta(k)$ depth for $k$ parallel rotations, as listed in Table 1. The depth for parallel rotations is significantly higher than EDPC and could lead to a larger space-time cost for circuits with many $T$ gates per time step.

A modified version of this Pauli-based computation compilation algorithm can be used to implement more $T$ gates in parallel [Lit19, Section 5.1]. However, as highlighted in [CC21, Section V.A], this results in a significant increase of total logical space-time cost when compared to the standard Pauli-based computation compilation algorithm, even when disregarding the increased $T$-factory costs that would be needed to achieve a higher $T$ state production rate.

In contrast with Pauli-based computation, one of our goals when designing the EDPC algorithm was to maintain the parallelism present in the input circuit, such that input circuits with higher numbers of $T$ gates per time step are compiled to circuits with a higher $T$-state consumption rate.

6.2 Surface code compilation by network coding

Another approach to surface code compilation, based on the field known as linear network coding [Ahl+00], can be built from the framework put forward in Beaudrap and Herbert [BH20]. Similar to our EDPC algorithm, the essential

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3In the scheme presented in [Lit19] only one joint Pauli measurement is needed per $T$ gate, but additional features are required of the surface code such as twist defects which were avoided in [CC21], and which we have avoided in this paper.
idea in this compilation scheme is to generate sets of Bell pairs in order to implement operations acting on pairs of distant qubits.

In the abstract setting of network coding [LL04], one is given a directed graph $G_{NC}$ and a set of terminal pairs $\mathcal{T} = \{(s_1, t_1), \ldots, (s_k, t_k)\}$ for source terminals $s_i \in V(G_{NC})$ and target terminals $t_i \in V(G_{NC})$ for $i \in [k]$. Messages are passed through edges according to a linear rule. Namely, the value of the message associated with an edge is given as a specific linear combination of the values of those edges which are directed at the edge's head. One can consider the task of “designing a linear network code” by specifying the linear function at each edge in the graph such that when any messages are input via the source vertices $s_1, \ldots, s_k$, then those same messages are copied over to the corresponding output via the target vertices $t_1, \ldots, t_k$.

A number of works have considered how linear network coding theory can be applied to the quantum setting [LOW10; Kob+09; Kob+11; SLI12; HPE19]. Beaudrap and Herbert [BH20] gives a construction for a constant-depth circuit to generate Bell pairs across the terminal pairs $\mathcal{T}$ on a set of ancilla qubits corresponding to the vertices of $G_{NC}$ with CNOTs allowed on the edges of $G_{NC}$. This is similar to, but not precisely the same scenario as we consider for surface code compilation in this paper since the basic operations are CNOTs rather than the elementary operations of the surface code, and since only ancilla qubits are considered without any data qubits. However, it should be quite straightforward to modify the approach in Beaudrap and Herbert [BH20] to form a surface code compilation algorithm. For example, one could use a layout similar to that which we use for EDPC in Figure 7, with $G_{NC}$ corresponding to a connected subset of ancilla qubits among a set of data qubits. The Bell pairs produced by the linear network coding approach could then be used to compile long-range operations between data qubits.

In such a network coding based compilation algorithm, the task of compiling an input circuit into surface code operations would largely rely on subroutines for (1) identifying $\mathcal{T}$ to implement the circuit’s long-range gates, and (2) designing a linear network code for $\mathcal{T}$. A major barrier to forming a usable compilation algorithm with linear network coding is that we are unaware of the existence of any efficient algorithm to design linear network codes, or even to identify if a given terminal pair set admits any linear network code. Even if such a linear network code can be found efficiently, there exist sets $\mathcal{T}$ for which network coding cannot provide a depth advantage over EDPC.

Any surface code compilation algorithm of CNOT circuits with $k$ parallel CNOTs, including EDPC and algorithms using network coding, is lower bounded in the worst case by Theorem 3.4 to a depth of $\Omega(\sqrt{k})$. This bound is loose when $k$ is superconstant and sublinear in $n$ since EDPC has a trivial upper bound of $O(k)$ and a bound of $O(\sqrt{n})$ by Theorem 3.3 on the compiled circuit depth. Therefore, it remains an open question whether network coding can give an advantage for the compiled circuit depth for such $k$. 

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On a rotated $L_1 \times L_2$ grid (here, $4 \times 5$), we can implement an odd-even pattern of swaps on data qubits (gray) using ancillas (white). Row-wise and column-wise swaps used in swap routing on a grid [ACG94] can be modified as shown above so that ancilla used for swaps do not overlap. Therefore, any arbitrary permutation on a rotated grid of can be implemented in space-time $4(L_1 + 1) + 2(L_2 + 1)$.

6.3 Surface code compilation by swap

Here we specify a swap-based compilation algorithm, stated in Algorithm 6.1, which we use to benchmark our EDPC against in Section 6.4. We assume the 1-to-1 ancilla-to-data qubit ratio as illustrated in Figure 11. This is more qubit-efficient than the 3-to-1 ratio we use for EDPC, and it allows the swap gadget in Figure 3b to be implemented between diagonally neighboring data qubits.

The first step of the swap-based compilation algorithm is to assign each of the input circuit’s qubits to a data qubit in the layout. Then, the gates in the input circuit are collected together into sets of disjoint gates. Before each set of gates, a permutation built from swap-gates is applied, which re-positions the qubits so that the gates in the set can be applied locally. We assume that the available local operations are the same as for our EDPC algorithm. In particular, we assume that the rotation gates ($S$, $T$, $S_x$ and $T_x$) can only be implemented at the boundary and that other single-qubit operations are performed as described in Section 2.1. One exception is that we make the simplifying assumption that the Hadamard can be performed without the need of three ancilla patches to simplify our analysis — this assumption could lead to an underestimate of the resources required for this swap-based compilation algorithm.

There are two main components of our swap-based algorithm which remain to be specified: how the permutations are implemented, and how we choose to separate the input circuit into a sequence of sets of disjoint gates. To permute the positions of data qubits, sequences of SWAP operations are used. Any permutation of the $n$ vertices in a square grid can be achieved in at most $3\sqrt{n}$ rounds of
Algorithm 6.1: **SWAP compilation**: We construct an algorithm based on the *greedy depth* mapper algorithm from [CSU19]. Let us implicitly define \( \text{route}(\pi) \), for mapping \( \pi \), which finds a SWAP circuit for implementing partial permutations [CSU19]. We can compute the required partial permutation from the current mapping of qubits, and the given future mapping \( \pi \).

**Input**: A circuit \( C \) with all Paulis commuted to the end and merged with measurement

1. **function** \( \text{cost}(\text{mapping } \pi, \text{vertices } v_1, v_2) \):
2.     **return** depth and edge attaining
3.     \[ \min_{e \in \mathcal{M}} \text{depth}(\text{route}(\pi + \{v_1 \mapsto e_1, v_2 \mapsto e_2\})) \]
4. **while** available gates in \( C \):
5.     \( G \leftarrow \) available gates in \( C \)
6.     execute all Hadamards and measurements in \( G \)
7.     \( G \leftarrow \) surface code grid graph
8.     \( \pi \leftarrow \) empty mapping of \( V(G) \rightarrow V(G) \)
9.     \[ \text{// Start modification for operations requiring magic states} \]
10.     Set \( B \subseteq V(G) \) as the set of boundary vertices
11.    \( G_m \leftarrow \{g \in G \mid g \text{ is } S, T, S_x, T_x\} \)
12.   **while** \( G_m \neq \emptyset \) and \( B \neq \emptyset \):
13.     \( g \leftarrow \) pop random gate from \( G_m \)
14.     \( \pi \leftarrow \pi + \{v \mapsto u\} \), for closest \( u \in B \) to \( v \)
15.     remove \( u \) from \( B \) and \( G \)
16.   \[ \text{// End modification} \]
17.  \( \mathcal{M} \leftarrow \) maximum matching of \( G \)
18.  \( G_c = \{g \in G \mid g \text{ is } \text{CNOT}\} \)
19. **while** \( G_c \neq \emptyset \) and \( \mathcal{M} \neq \emptyset \):
20.    \( g^*, e^* \leftarrow \max_{g \in G_c} \text{cost}(\pi + \{v_1 \mapsto e_1, v_2 \mapsto e_2\}) \) for \( v_1, v_2 \)
21.    current location of \( g \)
22.    \( \pi \leftarrow \pi + \{v_1 \mapsto e_1, v_2 \mapsto e_2\} \), for \( v_1, v_2 \) current location of \( g^* \)
23.    remove \( g^* \) from \( G_c \)
24.    remove \( e^* \) from \( \mathcal{M} \)
25. **execute** the SWAPS found by \( \text{route}(\pi) \)
26. **execute** gates on qubits mapped by \( \pi \) since they are now local
nearest-neighbor swaps [SHT19]. To do this involves three stages, with the first and third stages each involving rounds of swap-gates within rows only, and the second stage involving rounds of swap-gates within columns only. A round of swap-gates within either rows only or within columns only are implemented with surface code operations as shown in Figure 11. This immediately shows that this approach is asymptotically tight for parallel circuits because the depth of a swap-based approach is lower bounded by the $\sqrt{n}$ diameter of the architecture grid for one long-range CNOT or rotation gate from the center of the grid. Therefore a parallel input circuit is compiled by the swap-based algorithm to an output circuit with depth $\Theta(\sqrt{n})$, including all the examples in Table 1.

There is considerable freedom in how to collect together gates from the input circuit into sets of disjoint gates. In our implementation in Algorithm 6.1, we use the greedy depth mapper algorithm from [CSU19], with a small modification to ensure that $S$ and $T$ gates are performed at the boundary. This algorithm also incorporates some further optimizations as described in [CSU19], including a partial mapping of qubits to locations, leaving the remaining qubits to go anywhere in an attempt to minimize the swap circuit depth.

6.4 Numerical results

Here we numerically compare the performance of EDPC with the swap-based compilation algorithm (Algorithm 6.1) when applied to a number of different input circuits. Note that our implementation of the EDPC compilation algorithm here differs slightly from that given in Algorithm 5.1, by greedily executing CNOTs earlier where possible. See Appendix E for details of the implementation.

Our first input circuit example consists of random parallel CNOT circuits of different gate densities. The density $n_{\text{CNOT}}$ of a circuit is how many of the data qubits are involved in a CNOT gate in any such set. Therefore, $n_{\text{CNOT}} = 0.1n$ means that 10% of all qubits ($n$) are performing a CNOT gate in each set. For each data point, we sample 10 random circuits and plot the mean space-time cost in Figure 12 with the standard error of the mean in the shaded region. The runtime of the swap protocol was bounded by 2 days, which was insufficient for larger instances of these random circuits at high densities.

We also consider a more structured input circuit, namely implementing half of a multi-controlled-$X$ gate, $C^k\text{NOT}$. We consider decompositions of $C^k\text{NOT}$ for $k$ integer powers of 2, but only compile the first half of the circuit, given in Figure 13a. A $T$-efficient implementation of $C^k\text{NOT}$ uses measurement and feedback for uncomputation [Jon13], which are not captured in our model (see Section 7). We plot the space-time cost of compiling the half $C^k\text{NOT}$ in Figure 13b. We see that the dependence on the number of qubits $k$ is worse for swap-based compilation, and results in a larger space-time cost starting at 64 qubits. Unfortunately, the swap-based compilation is quite slow: we ran the algorithm for at most 3 days and 9 hours at each data point and were only able to obtain results up to 128 qubits. However, the data we were able to obtain indicates a cross-over for compiling $C^k\text{NOT}$ circuits. The swap-based compilation has better space-time performance for small instances, while EDPC has a better
Figure 12: Space-time cost of a randomly sampled set of disjoint CNOTs with standard error of the mean (shaded region) compiled to the surface code using EDPC and swap compilation. We generate 10 random circuits for each number of qubits \( n \) consisting of a set of disjoint CNOTs of varying density; the number of randomly selected qubits involved in a CNOT is given by \( n_{\text{CNOT}} \). At all densities we see improved performance and scaling using EDPC.

space-time performance for compiling large \( c^k \text{NOT} \) circuits.

7 Conclusion

In this paper, we have introduced the EDPC algorithm for the compilation of input quantum circuits into operations which can be implemented fault-tolerantly with the surface code. The heart of this algorithm lies in the EDP subroutine, which can implement both sets of parallel long-range CNOT gates and sets of parallel rotations in constant depth using existing efficient graph algorithms to find sets of edge-disjoint paths. EDPC has advantages over other compilation approaches including Pauli-based computation, network coding based compilation, and SWAP-based compilation. We numerically find that EDPC significantly outperforms SWAP-based circuit compilation in the space-time cost.
Figure 13: We compare the space-time cost of compiling a $T$-gate optimized circuit decomposition for a half $c^k$NOT circuit to the surface code using EDPC and swap compilation. We see in the log-log plot (b) that dependence of the space-time cost on $n$ gives a higher scaling dependence in the case of swap compilation than EDPC. This results in a lower space-time cost for EDPC starting from 64 qubits.

of random CNOT circuits for a broad range of instances, and for larger $c^k$NOT gates. However, many details of EDPC can be improved, as it is only a first step towards using long-range operations for surface code compilation.

EDPC requires sets of constrained edge-disjoint paths, which we call operator paths and run almost entirely along ancilla qubits. Better algorithms for finding maximum sets of edge-disjoint operator paths could improve EDPC. It seems likely that an $O(\log n)$-approximation algorithm for finding maximum EDP sets on grids [AR95] can be modified to give an algorithm for finding maximum sets of edge-disjoint operator paths on grids. A polylogarithmic approximation algorithm for this task would imply an approximation algorithm for minimizing the depth, up to a polylogarithmic factor, of compiling parallel CNOTs using the EDP subroutine. In practice, it is, however, also important to find approximation algorithms with reasonable constant prefactors.

The runtime complexity of EDPC for an input circuit of depth $D$ acting on $n$ qubits is $O(Dn^3 \log n)$. This is significantly faster than the swap-based compilation in Section 6.3, which was found to be $O(Dn^5)$ in Childs, Schoute, and Unsal [CSU19]. We found that our implementation of the swap-based compilation implementation runtime is much slower than that of EDPC on small instances, and found that the swap-based algorithm had impractically long runtimes when applied to circuits beyond a few hundred qubits, the regime of large-scale applications of quantum algorithms [Rei17; GE21]. Potential ways to further improve EDPC’s runtime include using a dynamical decremental all-pair shortest path algorithm in the greedy approximation of the maximum
EDP set, or by finding faster and better approximation algorithms for finding the maximum set of edge-disjoint operator paths.

Any diagonal gates in the $Z$ (or $X$) basis can be performed remotely on the boundary, including CCZ gates [GF19] (see Appendix D). Therefore, our results on applying $Z(\theta)$ rotations can be extended to diagonal gates, which will benefit circuit depth.

Even with the capability to perform long-range operations it may still be helpful to localize the quantum information on some part of the architecture such as by permuting the data qubits. In particular, the size of the EDP set is bounded above by the minimum edge cut separating the terminals. Therefore, it may be beneficial to first redistribute quantum information where it is needed to ensure large EDP solutions exist. It is straightforward to construct a long-range move of a data qubit to an ancilla in depth 2 from a long-range CNOT, by performing the CNOT targeting a $|0\rangle$ ancilla state and measuring the source in the $X$ basis up to Pauli corrections. It also is straightforward to adapt the EDP subroutine to perform sets of these long-range moves along operator paths, now ending at the ancilla, in depth 4. The depth to permute only a few qubits a long distance can be improved significantly by this technique. For example, a SWAP of the two corners of an $L \times L$ grid architecture takes $O(1)$ depth using long-range moves, as opposed to $\Omega(L)$ depth using conventional SWAPs. It remains an open question how to trade off permuting data qubits (using SWAPs or long-range moves) and directly using long-range CNOTs.

We have assumed that classical feedback is not present in the input circuit for clarity of presentation. EDPC can readily be extended to the setting of classical feedback in the input circuit to form a “just-in-time” surface code compilation algorithm. To do so, a larger computation would be broken up into a sequence of circuit executions without classical feedback, where prior measurement results specify the next circuit to compile and execute.

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Figure 14: (a) A $d = 5$ surface code patch implemented in a grid of data physical qubits (black disks), and ancilla physical qubits (white disks). Error correction is implemented with single-qubit operations and CNOT between pairs of qubits connected by a dashed edge. $Z$ and $X$ type stabilizers are associated with alternating red and blue faces. (b) A decoding graph that is defined by associating an edge with each qubit and a vertex for each stabilizer. If stabilizers are measured perfectly, $Z$ errors on data qubits (marked in red) can be corrected by finding a minimum weight matching (green edges) of vertices associated with unsatisfied $X$ stabilizers (yellow disks).

### A Surface code architecture

Here we review some basic details of the surface code focusing on the elementary logical operations shown in Figure 1. This is intended as a high-level overview to provide some intuition of how the logical operations in Figure 1 arise and what their resource costs are. For more thorough reviews of surface codes see Refs. [Bom13; Fow+12; Bro+17].

To implement the surface code, we assume physical qubits are laid out on the vertices of a 2D grid, with nearest-neighbor interactions allowed. For concreteness, we will describe here an implementation of lattice surgery with the rotated surface code with half-moon boundary [LR14], although our EDPC algorithm can use other implementations. A single surface code patch encodes a single logical qubit in $2d^2 - 1$ physical qubits, where the odd parameter $d$ is known as the code distance which corresponds to the level of noise protection; see Figure 14(a). For clarity, within this section of the appendix we refer to physical qubits and logical qubits explicitly, however in other sections we often drop the word “logical” when referring to logical qubits for brevity.

We designate every odd physical qubit as a data physical qubit in the patch, and every even physical qubit as an ancilla physical qubit to facilitate a stabilizer measurement; see Figure 14(a). The code space of a surface code consists of those states of the data physical qubits which are simultaneous $+1$ eigenstates of the set of stabilizer generators. The stabilizer generators can be associated
with faces and are either $X \otimes X \otimes X \otimes X$ or $Z \otimes Z \otimes Z \otimes Z$ operators for the bulk (interior) of the code or $X \otimes X$ or $Z \otimes Z$ operators on the boundary. We can see that the logical $Z$ operator, $Z_L$, defined as any path of single-qubit $Z$ operators on physical qubits connecting the rough boundaries, commutes with all stabilizers. Similarly, the logical $X$ operator, $X_L$, is a path of $X$ operators connecting the smooth boundaries.

For quantum error correction, it is necessary to repeatedly measure stabilizer generators. Stabilizer generators can be measured by running small circuits consisting of the preparation of the ancilla physical qubit, CNOTs between the ancilla physical qubit and the data physical qubits, followed by measurement of the ancilla physical qubit. Error correction can be performed by associating qubits with edges and stabilizer generators with vertices of a so-called decoding graph; see Figure 14b. A classical algorithm known as a decoder is used to infer a set of edges (specifying the support of the $X$ or $Z$ correction) given a subset of vertices (corresponding to unsatisfied $Z$ or $X$ stabilizers, that is stabilizer generators with measurement outcome -1). Figure 14b shows an example of this in the setting of perfect stabilizer measurements, although this can be generalized to handle faulty measurements by repeating measurements.

Logical operations can be implemented fault-tolerantly on logical qubits encoded in surface codes. For example, a destructive logical $X$ measurement of a patch is implemented by measuring all data qubits in the $X$ basis, and then using a decoder to process the physical outcomes and reliably identify the logical measurement outcome. Another important logical operation is the non-destructive measurement of a logical joint Pauli operator using an approach known as lattice surgery [Hor+12] as shown in Figure 15a. To simplify lattice surgery by lining up the boundary stabilizers of neighboring patches, we consider a tiling of the plane using two versions of distance $d$ surface code patches as shown in Figure 15b which forms a grid of logical qubits. Logical $Z_L \otimes Z_L$ can be measured between vertical neighbor patches while $X_L \otimes X_L$ can be measured between horizontal neighbor patches.

The allowed fault-tolerant logical operations that we assume throughout the paper and the resources they require are listed in Figure 1. These are largely based on the rules specified in [Lit19]. Here we justify the resource requirements for the logical operations in Figure 1 not covered in [Lit19] on a distance-$d$ surface code. For space analysis, we work in units of full surface code patches such that if any qubits from a patch are needed to implement an operation the full patch is counted. We show how to implement the operations in terms of more elementary Pauli measurements. The move operation can be implemented in depth 1 with the target qubit as ancilla, as shown in Figure 16. The Hadamard can be implemented in depth three with three ancilla patched along with the move operation as shown in Figure 17. Finally, Bell measurement and preparation can be implemented in depth 1 as shown in Figure 18.

It is worth mentioning that there is considerable freedom in the detailed choice and implementation of the surface code which could have an impact on the space-time cost of logical operations, both at the physical level but also in some cases at the logical level. For example the Hadamard could be performed
Figure 15: (a) A logical $Z_L \otimes Z_L$ measurement is performed by lattice surgery in the following steps: (i) Stop measuring the weight-two stabilizers along the horizontal boundary between the patches. (ii) Reliably measure the bulk faces for a single vertically-extended patch. Note that $Z_L \otimes Z_L$ can be inferred from the product of the outcomes of the newly measured red faces. This temporarily merges the patches to form a single extended surface code patch. (iii) Reliably measure once more the weight-two faces along the horizontal boundary between the patches. This separates the pair of patches. (b) Two types of patches tile the plane, with $Z_L \otimes Z_L$ measurements possible between vertically neighboring patches, and $X_L \otimes X_L$ measurements possible between horizontally neighboring patches.

Figure 16: The move operation can be implemented in depth 1 by local and neighboring Pauli measurements. A horizontal move can be implemented by preparing a single-qubit patch in $|0\rangle$, applying joint $XX$ measurement, and then measuring the original patch in the $Z$ basis (up to Pauli corrections). The vertical move follows from applying a Hadamard to the source qubit $|\phi\rangle$ and a Hadamard on the output. Simplifying the circuit gives the right-hand side in the Figure, with a $ZZ$ measurement that is available vertically.
Figure 17: Implementation of a Hadamard operation in depth 3 with three ancilla patches. (a) A transverse Hadamard is applied in depth 0 to each physical data qubit, which switches the arrangement of $X$ and $Z$ stabilizer generators compared to the standard configuration. (b) The patch is extended in depth 1 so that a segment of the standard boundary type is introduced on the right. (c) The patch is shrunk into a standard surface code patch of the form of the top-left corner of the region (see Figure 15b) in depth 1, but with its location shifted by a (code distance) $d$-independent amount. This allows us to shift the patch into the top-left corner in 0 depth (not shown). Then we move the logical qubit to the bottom-left corner in depth 1.

\[
\begin{align*}
\begin{pmatrix}
B \\
B
\end{pmatrix}
= & \begin{pmatrix}
Z & X \\
Z & Z
\end{pmatrix} \begin{pmatrix}
X & Z \\
Z & Z
\end{pmatrix} \\
= & \begin{pmatrix}
X & Z \\
Z & Z
\end{pmatrix} \begin{pmatrix}
X & Z \\
Z & Z
\end{pmatrix} \\
\end{align*}
\] 

$|00\rangle + |11\rangle$

(a) Bell pair preparation

\[
\begin{align*}
\begin{pmatrix}
B \\
B
\end{pmatrix}
= & \begin{pmatrix}
Z & X \\
Z & Z
\end{pmatrix} \begin{pmatrix}
X & Z \\
Z & Z
\end{pmatrix} \\
= & \begin{pmatrix}
X & Z \\
Z & Z
\end{pmatrix} \begin{pmatrix}
X & Z \\
Z & Z
\end{pmatrix} \\
x = & x_1 \oplus x_2 \\
z = & z_1 \oplus z_2
\end{align*}
\] 

(b) Bell measurement

Figure 18: We can implement Bell preparation and measurement in terms of single and two-qubit Pauli measurements in depth 1 as given in Figure 18 [Lit19]. (a) A Bell pair can be prepare from a (horizontal) joint $XX$ measurement of $|00\rangle$ or a (vertical) joint $ZZ$ measurement of $|++\rangle$, up to Pauli corrections. (b) A destructive Bell measurement can be implemented by a joint $XX$ measurement followed by individual $Z$ basis measurements, or by a joint $ZZ$ measurement followed by individual $X$ basis measurements.
using just one logical ancilla patch if each patch was padded with extra qubits. We do not explore these alternatives here, but note that our EDPC algorithm can still be applied if these alternatives are used.

B Logical space time cost as a proxy for physical space time cost

Here we provide a justification for our use of logical space time cost as a proxy for physical space time cost. As we have seen in Figure 1 and Appendix A, logical operations implemented with the surface code require physical time that scales as \(d\) and physical space that scales as \(d^2\). For a logical circuit written in terms of a total of \(A_{\text{logical}}\) elementary logical operations implemented using surface codes of distance \(d\), the physical space-time cost \(A_{\text{physical}}\) is approximately

\[
A_{\text{physical}} \sim A_{\text{logical}} d^3.
\]  

(8)

The probability of any of these elementary operations resulting in a logical failure scales as \(p_{\text{fail}} \sim (p/p^*)^{d/2}\), where the fixed system parameters are the physical error rate \(p\), and the fault-tolerant threshold for the surface code \(p^*\). Moreover, we assume \(p_{\text{fail}} \sim 1/A_{\text{logical}}\) to ensure that the logical circuit is reliable with as small a code distance as possible. This suggests that the code distance behaves as

\[
d \sim \frac{2 \log A_{\text{logical}}}{\log p^* - \log p}.
\]

(9)

Therefore we see that the physical and logical space time costs are monotonically related, i.e.,

\[
A_{\text{physical}} \sim A_{\text{logical}} (\log A_{\text{logical}})^3.
\]

(10)

C cnot via Bell operations

We list more variations of the standard cnot gate (Figure 3a) that use intermediate Bell preparation and measurements on ancillas in Figure 19. By choosing the right subcircuit, we see that the long-range operations in Figure 8 implement a cnot gate.

D Remote execution of diagonal gates

A gate \(D\) diagonal on \(k\) source qubits in the computational basis can be executed on \(k\) ancilla by first entangling these ancilla qubits using cnots. We call this remote execution. Let the computational basis be \(|\ell\rangle\), for \(\ell \in [2^k]\), then \(D|\ell\rangle = \exp(i\phi_\ell)|\ell\rangle\). We saw one use for remote gates in applying rotations at the boundary requiring magic states (Section 4).

We execute \(D\) remotely as follows (see Figure 20). First, we initialize the ancilla in the state \(|0\rangle^\otimes k\). Let the source qubits be in some pure state \(\sum_\ell \alpha_\ell |\ell\rangle\),
Figure 19: Various implementations of a CNOT gate with intermediate ancilla qubits and Bell operations. In particular, we are able to apply the control and the target either before (green) or after (teal) Bell preparation and measurement steps, while keeping the depth at 2.

(a) CNOT via Bell preparation

(b) CNOT via Bell measure

(c) CNOT with control first

(d) CNOT with target first

Figure 20: (a) Any $k$-qubit gate diagonal in the computational basis can be remotely executed on $k$ dedicated ancilla by first using CNOTs. We use this technique to apply remote $Z(\theta)$ rotations (Figure 10b) with magic states at the boundary. (b) Similarly, gates diagonal in the Hadamard basis also have a remote implementation. Since the Pauli corrections can be commuted through Clifford circuits, Clifford circuits can be executed immediately after executing the CNOT operations with no need to wait on the remote operations.
for $\alpha_\ell \in \mathbb{C}$. then we apply $k$ transversal CNOT gates controlled on source qubits so that the overall state becomes $\sum_\ell \alpha_\ell |\ell\rangle \otimes |\ell\rangle$. We now apply $D$ to the ancilla instead

$$(1 \otimes D) \sum_\ell \alpha_\ell |\ell\rangle \otimes |\ell\rangle = \sum_\ell \alpha_\ell \exp(i\phi_\ell) |\ell\rangle \otimes |\ell\rangle.$$ (11)

We now disentangle the ancilla by measuring them in the $X$ basis. Let the measurement give outcomes $x \in \{0, 1\}^k$, then the state on the source qubits is mapped to

$$\sum_\ell \alpha_\ell \exp(i\phi_\ell)(-1)^{(x, \ell)} |\ell\rangle,$$ (12)

where $(x, \ell)$ is the inner product modulo 2 between $x$ and the binary representation of $\ell$. Applying a $Z$ correction to each qubit $j \in [k]$ controlled on measurement result $x_j$ maps the state to $\sum_\ell \alpha_\ell \exp(i\phi_\ell)$ as required.

This technique can be extended to any unitary operator $U$ since it can be unitarily diagonalized as $U = VDV^\dagger$ by the spectral theorem, for $V$ unitary and $D$ diagonal operators. A particularly simple case are unitary operators that are diagonal in the Hadamard basis, where $V = H^\otimes k$. We write $U = H^\otimes k DH^\otimes k$ on the source qubits and apply remote execution of $D$ using our techniques above. We then simplify the circuit to obtain Figure 20b.

## E EDPC implementation

Here we provide Algorithm E.1, which specifies the implementation of EDPC used for our numerical results presented in Section 6.4, here called EDPCI for clarity. EDPCI differs slightly from EDPC (Section 5) and we will highlight the differences. Up until Line 7 in Algorithm E.1, EDPCI is the same as EDPC. Then, EDPCI greedily attempts to execute long-range CNOTs earlier than would occur in EDPC. In particular, EDPC only executes CNOTs after all available rotations have been executed, whereas EDPCI finds a set $P_c$ on Line 9 such that $P_c \cup P_m$ forms an EDP set. Now EDPCI concurrently executes long-range CNOTs using any edges left over from remote rotations. Moreover, we note that EDPC uses the bounded $T$-operator set algorithm (Algorithm 3.2) to execute a parallel CNOT circuit, which additionally finds a bounded $T$-operator set $Q_1$ on Line 1, whereas EDPCI only finds $Q_2$ from the bounded $T$-operator set algorithm if given a parallel CNOT circuit. As a consequence of this difference, while a parallel input CNOT circuit is guaranteed to compile to an output circuit upper bounded by $O(\sqrt{n})$, EDPCI does not have this guarantee.
**Algorithm E.1: EDPC implementation**:
The EDPC algorithm (Algorithm 5.1) differs from our implementation in that it greedily tries to execute CNOTs earlier.

**Input**: Circuit $C$ with Paulis commuted to the end and merged with measurement

1. while available operations in $C$:
   2. execute all available state preparation, measurement, and Hadamard
   3. $G_m \leftarrow \{ \text{available operations } g \in C \mid g \text{ is } S, T, S_x, \text{ or } T_x \}$
   4. $G_c \leftarrow \{ \text{available operations } g \in C \mid g \text{ is CNOT} \}$
   5. while $G_m \cup G_c \neq \emptyset$:
      6. $P \leftarrow \text{surface code grid graph}$
      7. $P_m \leftarrow \text{max_rotations}(G_m)$ // see Algorithm 4.1
      8. remove edges in each $P \in P_m$ from $G$
      9. $P_c \leftarrow \text{approximate max operator EDP set on } G$ with $G_c$
      10. execute concurrent remote rotations along $P_m$ and long-range CNOTs along $P_c$ using EDP subroutine
      11. remove executed rotations from $G_m$ and CNOTs from $G_c$