Implementation of Phase Shifted Carrier Modulation Technique for Cascaded Five-Level Inverter Using FPGA

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Abstract. This paper presents the development of Xilinx Field Programmable Gate Array (FPGA) to control single phase Cascaded Multilevel Inverter (MLI). FPGA realizes high speed switching and attains a high over sampling rate. The FPGA provide eight control signals for five level output voltage using Phase Shifted Carrier (PSC) modulation technique. All the function modules of the designed program was implemented using Very High Speed Integrated Circuit Hardware Description Language (VHDL) and Xilinx ISE 9.2i software was employed as a simulation and compiler tool. The proposed strategy can provide a wide range of rms output voltage by varying the modulation index. The simulation of the system was carried out by Matlab/Simulink. Simulation and experimental results are provided.

1. Introduction
In recent years, MLIs have been considered as energy converters in several applications. They are more profitable than conventional three-level converters because they can minimize the harmonic content of the fundamental wave by increasing the number of stages. The Flying Capacitor, Neutral Point Clamped, and the Cascaded H-bridge inverter, are the most studied and commercialized topologies. The Cascaded H-Bridge, also known as Multi-cell converter, topology is the most popular one; for simple controllability and its modular structure [1].

MLIs are mainly controlled with Multicarrier Modulation Techniques (MMT) to synthesize the output voltage and to decrease THD. In these techniques, one of sinusoidal signal is compared with each carries to determine the switched signals for the inverters [2]. MMTs are arrangement of two types depending on the type of carrier arrangement: Level Shifted (LSC- MMT) and Phase Shifted (PSC- MMT). In LS- MMT, all carrier signals are level-shifted (i.e. vertically shifted), which involves Phase Disposition (PD- MMT), Phase Opposition Disposition (POD- MMT) and Alternative Phase Opposition Disposition (APOD- MMT). Whereas PSC- MMT, all the triangular carrier signals are horizontally disposed [3, 4] as shown in figure 1.

![Figure 1. Multicarrier modulation techniques](image-url)
PSC- MMT is the best usual scheme for the cascaded MLI. In addition to PSC- MMT, it is better than LSC- MMT in terms of harmonic content and DC voltage utilization factor [5]. Different types of digital controllers as Microcontroller [6], Digital Signal Processors (DSPs) [7], Complex Programmable Logic Device (CPLD) [8], and Arduino [9] are used for generation of modulating signals for MLIs. In this work, FPGA was chosen for the experimental execution as a control circuit is owing to its very high computation speed, parallelism feature, and flexibility, which can produce accurate control signals.

2. Cascaded H-Bridge Inverter
The cascaded-MLI composed of series joining of identical single-phase H-bridge converters with isolated DC supply (as shown in figure 2), which may be obtained from batteries, or renewable energy sources as fuel cells, or solar cells [10].

![Figure 2. Circuit diagram of cascaded-MLI](image)

With Nth number of H-bridge inverter, the number of the level (L) of the o/p terminal voltage \( V_o \) equal to \((2N + 1)\). Thus the instantaneous o/p terminal voltage \( V_o(t) \) equal to summation of the instantaneous o/p terminal voltage of each H-bridge inverter (i.e. o/p voltage of first H-bridge \( V_{o1}(t) \), second \( V_{o2}(t) \), until o/p voltage of Nth H-bridge \( V_{oN}(t) \)) which can be presented as:

\[
V_o(t) = V_{o1}(t) + V_{o2}(t) + \ldots \ldots + V_{oN}(t)
\]  

3. PSC Modulation Technique
The PSC-MMT method uses numerous triangular carrier signals equal to \((K = L - 1)\), keeping only one modulating sine wave signal. In general, triangular carrier waves are equal frequency and have same peak - to - peak amplitude; on the other hand, there is a phase shift \( \phi_c \) equal to \(\frac{2\pi}{K}\) between carrier waves.

So; four triangular carrier waves (C1, C2, C3, and C4) are necessary for five level inverter with phase displacements angle equal to 90° between any two adjacent carriers as shown in figure 3. The reference waveform Ref is located at zero reference and continuously for comparison with carrier waves.

![Figure 3. PSC- Modulation Technique](image)
If the Ref is greater than a C1, C2, C3, and C4 carrier waves, then the semiconductor power switch conforming to that carrier is switched ON. Otherwise, it turned OFF [3]. The triggering pulses produced from PSC-MMT are all the time symmetrical to each other is it through various value of modulation index, whereas it becomes an asymmetrical in LSC-MMT in case of under-modulation. Therefore, both stress and losses are similarly distributed among the components of the converter. So PSC-MMT can be considered better than LSC-MMT for cascaded-MLI [4, 11].

4. Simulation Circuit
To verify the proposed cascaded five level inverter, a simulation model is implemented via Matlab/Simulink tool as shown in figure below.

![Simulation circuit of five level inverter](image)

**Figure 4. Simulation circuit of five level inverter**

5. Proposed VHDL Control Program:
After simulation in MATLAB Simulink System, the inverter was validated based on the FPGA environment. In the present scheme, the triggering signals for power device switches in five level inverter are directly produced using a software program coded with VHDL and downloaded in Xilinx Spartan 3E XC3S500E starter kit FPGA [12]. The main program has five parts as following:

5.1. Reference Wave Generator Block:
The single sine reference wave generation is realized by activation the Sine Look-Up Table (which is available in Xilinx CORE Generator). The Sine module accepts an unsigned input value α (3 to 10 bits for Block ROM) and produces two’s complement outputs of SINE (α) (4 to 32 bits). The user controls the input α width and output SINE width values. Equation (2) defines the relationship between the integer input angle α supplied to the core and the actual radian angle (θ).

\[ \theta = \alpha \frac{2\pi}{2^m} \text{ radians} \]  

(2)

Where: \( m \) is α width.

To generate a sine reference wave, the input data (α) in Sine module will be integer, coming from a programmable up counter, which will contain the different values of the discretized sine wave input α (0 to 2π). In order to adjust the frequency of sine reference wave:

- A clock divider based on Digital Frequency Synthesizer (DFS) unit is used to divide the clock frequency of the FPGA which equals to 50 MHz to produce clock frequency (f_c) which is used here according to.
The reference frequency ($f_r$) has a relationship with the clock frequency ($f_{clk}$) and the $\alpha$ width ($m$), could be expressed as:

$$f_r = \frac{f_{clk}}{2m} \quad (4)$$

The frequency of the sine reference wave ($f_r$) has been decided to operate at (50 Hz), the clock frequency ($f_{clk}$) is (409.836 KHz) ((50 MHz) divided by (122), and the $\alpha$ width ($m = 13$-bits) as shown in figure 5.

The peak value of the sine reference wave ($A_r$) depends on the width bit ($r$) of the output of a sine reference wave (sine $\alpha$) according to equation (5).

$$A_r = \frac{2^r}{4} \quad (5)$$

Figure 5. Proposed sine wave generator

5.2. Multicarrier Wave Generator Block

Each one of the multicarrier waves is generated using up/down counters, which is incremented and decremented until the maximum value and the minimum value of the carrier wave is reached respectively with taking in the consideration the phase shifting between each other.

- As seen in figure 3, there is a phase angle between the carrier waves; these angles are produced in the software by starting each counter of each carrier wave with different value and different direction (Upward or Downward).

- The carrier frequency ($f_c$) has a relationship with the $f_{clk}$ and the up/down counter bit resolution ($n$) which can be expressed as:

$$f_c = \frac{f_{clk}}{2^{(n+1)+1}} \quad (6)$$

- As in generation the sine reference waveform, the DFS unit is used to multiply the main clock frequency (50 MHz) by the ratio of ($\frac{19}{29}$) to generate ($f_{clk}$) equal to (32.75 MHz). Thus, with $n = 12$ and $f_{clk} = 32.75$ MHz; the carrier frequency ($f_c$) equal to (4 KHz).

- The peak amplitude of the triangular carrier wave ($A_c$) depends on the bit size of the up/down counter ($n$), according to the following equation:

$$A_c = 2^{(n-1)} - 1 \quad (7)$$

5.3. Modulation Index ($M$) Control Block

Modulation index is a significant parameter used to control the amplitude of the fundamental o/p voltage of DC-AC inverters. The ratio of amplitude of the sine reference wave ($A_r$), to the triangular carrier wave ($A_c$) is known as the Modulation index ($M$), as shown in equation (8).

$$M = \frac{A_r}{A_c} \quad (8)$$
The amplitude of the triangular carrier wave \( (A_c) \) is generally kept constant, so, controlling the amplitude of the sine reference wave \( (A_r) \) gives a variation of the M. The multiplier used for multiplying the values of the sine reference wave \( (\text{sine } \alpha) \) which are stored in an internal block ROM \( (r = 10\text{-bits}) \) with modulation index controller \( (\text{M-Controller} = 3\text{-bits}) \) to get a variation in the sine reference wave amplitude resulting in a variation of the M. The value of the M-Controller can be adjusted by using three slide switches (are already existing on the FPGA kit).

### 5.4. Comparators Block

The triangular carrier waves \( (C1, C2, C3, \text{and } C4) \) are to be compared with the multiplied sine reference wave \( (\text{Ref}) \) (output data from the multipliers) by using a four-digital comparators. The digital comparator output is logic one if the magnitude of the reference wave is greater than the magnitude of the carrier wave; else its output is logic zero. The comparator outputs negated to create the complement signals) of each value to trigger the lower power switches of the MLI.

### 5.5. Dead Zone Time Block

The turn off time of power switches is typically longer than its turn on time, and, thus a proper dead time should be included between the upper and lower gating signals to prevent simultaneous conduction of the switches on the same leg. In the same time date time causes distortion of the output voltage and reduces its amplitude. In this work he dead time for is \( (4 \text{ micro-sec}) \).

Figure 6 represents the RTL-Schematic of the proposed VHDL code. Figure 7 shows the simulation test bench waveform of the ISE software environment of eight gate signals of the five level inverter.

### 6. Experimental Results

A prototype setup of a five level inverter has been built for validation the theoretical and simulation analysis. Xilinx Spartan 3E controller (FPGA) is chosen as a controller. The eight TLP350 optocoupler inserted between FPGA card and the MOSFET power switches of the MLI. TLP350 involves of an infrared Light Emitting Diode (LED) optically coupled to an integrated high gain, high speed photo-detector integrated circuit chip as shown in figure 8. the benefits of each one of these optocoupler; provide isolation between the Power MOSFET bridge and the FPGA card in addition to provide amplified gate control signals to IRFP460 Power MOSFETs. A photograph of the experimental MLI is given in figure 9.
Figure 8. Gate drive circuit based on TLP 350 Optocoupler

Figure 9. Experimental circuit of MLI

Figure 10 shows the experimental o/p voltage waveform, simulation o/p voltage with its spectrum analysis, and load current waveform also with its spectrum analysis. These results of designed five level inverter are taken with different value of modulation index with R-L load, R=30 (Ω), L=10 (mH), output frequency $f_c$ = 50 (Hz). The frequency of the triangle carrier waveform was chosen as 4 kHz.

(a) Modulation index equal to 0.375
Figure 10. Experimental inverter output voltage waveform, load current with their spectrum analysis at various modulation indexes.
The lowest harmonics appear as sidebands centred on harmonic order equal to \(((K \cdot M_f), (2K \cdot M_f), (3K \cdot M_f)\), and so on). Where, \(K\)th is the number of carrier waves, and \(M_f\) is the ratio between the carrier and reference frequency.

\[
M_f = \frac{f_c}{f_r}
\]

Therefore, in the work, four triangle carrier waves with frequency equal to 4 KHz, the harmonics appear at side bands of 16 KHz. Thus, the number of level of the output voltage is decreased with decrease the amplitude the modulation index; when the modulation index decrees lower than 0.5 the number of level will equal to three instead of five. In addition to the amplitude of the THD decrease with decreasing the modulation index.

7. Conclusions:
- FPGA digital control switching patterns based on PSC-MMT are adopted and experimentally applied to the cascaded two H-Bridge MLI switches to generate five level o/p voltages. This inverter is confirmed by simulation and experimental results.
- Wide range variation of modulation index is obtained (i.e. the pulses are still produced even in the event of the under-modulation condition. So, a higher reliability is realizable with PSC-MMT as compared with LSC-MMT).
- The FPGA reduces complexity, computation time required to define the switching pulses for inverter. It can easily increase the range of modulation.
- Employing MLI instead of traditional (3-level) inverters improves quality o/p voltage waveform shapes, reduces its harmonic content and thus reduced the amplitude of output THD with higher fundamental component amplitude and voltage stress on semiconductors switches, especially the THD of the load current approximately equal to 1 which conceder low value.
- In future work; single-phase inverter PSC modulation technique with higher number of levels can be adopted, in addition to three-phase MLI technique can be implemented.

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