Characterization and Modelling of Gate Length Impact on the Transient Negative Capacitance Induced Control of Short Channel Effect in Ferroelectric Fin-FETS

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Abstract —This paper reports for the first time an intricate analysis of gate length dependence of the transient negative capacitance induced pruning of the short-channel effects in hafnium zirconium oxide based ferroelectric fin-FET devices. We have fabricated devices with 10nm thick hafnium zirconium oxide based ferroelectric Fin-FETs with fin width of 20nm and 25nm. The gate lengths are varied as 50nm, 70nm, 80nm and 150nm and transient negative capacitance induced alleviation of short channel effect in terms of subthreshold slope improvement have been analyzed and modelled. Further study has been conducted by simulating double gate ferroelectric FinFETs with channel lengths ranging from 25nm to 100nm using TCAD. The results show that ferroelectricity significantly reduces subthreshold swing and the impact is found to be significantly feister in short channel devices than long channel ones, which demonstrates the tremendous advantage of using ferroelectric gate stack for scaled MOSFETs. Further a compact analytical formulation is developed to quantify sub-threshold swing improvement for short channel devices.

Index Terms — analytical model, DIBL, ferroelectric, FinFET, negative capacitance, short channel effect, subthreshold swing.

I. INTRODUCTION

THE recent progress in the research of CMOS-compatible ferroelectric hafnium zirconium oxide (HZO) has paved the way for implementation of next generation ferroelectric memory[1,2] along with this, the advent of the research in the field of differential negative capacitance (NC) in HZO can also assist in subjugating the “Boltzmann Tyranny” for advanced logic devices[3]. Amidst a numerous research on the impact of negative capacitance and the reliability issues associated with them [4-8], the topic of negative capacitance has been a matter of dissension amongst the scientific community. The origin of additional steepness beyond 60mV/dec in ferroelectric traditional field effect transistors has been described by divergent physical phenomena by different groups. The origin was first ascribed to the quasi-static negative capacitance (QS-NC) concept, which used single-domain landau formalism for ferroelectric switching to predict the plausible existence of negative capacitance in ferroelectric FET [9-18].

This work was jointly supported by the Ministry of Science and Technology (Taiwan) grant MOST-108-2634-F-006-08 and is part of research work by MOST’s AI Biomedical Research Center.

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The red curve in Fig.1(a). depicts the switching path required for attaining the QS-NC region, where presence of more than one domain is interdicted.

Apart from this, the interfacial dielectric layer also plays a pivotal role to impel the ferroelectric layer into the QS-NC state [9]. As, it is evident from the Fig.1(b), that QS-NC region lies within a thermodynamically unstable region in Gibbs’ free energy curve for ferroelectric. Therefore, an additional matching interfacial dielectric layer is required to artificially steer the single-domain ferroelectric layer in the negative capacitance region. Apart from this, the random distribution of phase and trapping-detrapping phenomena in HZO infuses additional obscurity along with requisite of fabricating devices with a single-domain to attain QS-NC state. Therefore, obtaining QS-NC hysteresis free MOSFET is pretty abstruse in real scenario.

Although, some recent developments on the direct observation of the negative capacitance in some literatures have also reinforced the existence of “S” along with plausible “modus operandi” to drive the ferroelectric thin film into QS-NC state [19,20]. However, some explanations regarding single domain “S” curve extraction remains iff. Therefore, some recent researches enunciate their dubious notion towards experimental procedures of these researches and the existence of QS-NC, providing us with some alternative explanations of non-linearity incited dynamic snap-back effect, about the origin of
such steepness in ferroelectric FETs [21-25]. Nevertheless, none of the above researches could furnish adequate proof to falsify the antagonistic theory.

In this paper, we focus on the impact of transient negative capacitance (TNC) on FinFETs, where the presence of multidomains does not impede the ferroelectric film from attending differential negative capacitance region during its switching [26-30]. The TNC is a consequence of switching rate mismatch between free charge in metal plate and bound charge in ferroelectric layer [26]. Although there have been several researches corroborating the direct correlation between transient negative capacitance with the negative curvature of Gibbs’ free energy of ferroelectric materials [19,20], but it has been shown that modified Preisach model of ferroelectric switching can also accurately capture this phenomenon [28]. Although this paper does not discard the existence of QC-NC in single domain ferroelectric crystals, but the pivotal point of this work is to corroborate the effect of the TNC in multidomain ferroelectric crystals on the subthreshold swing improvement and establish direct correlation of subthreshold slope improvement with the device gate length. Therefore, we have also simulated the capacitance vs voltage characteristics to extract the voltage range where, TNC is prevailing. This extraction is important to predict the impact of TNC induced suppression of short channel effect. We have found that, albeit the QC-NC region is thermodynamically unstable and abstruse to realize in fabricated devices, the TNC is dominant in most of our fabricated devices, leading to about 31% of devices showing subthreshold slope less than 60mV/dec in reverse sweep. 99% of devices exhibited ferroelectric dominant switching (MW>0).

The paper is divided into seven sections. In the section-II we discuss about the fabrication and characterization of HZO based ferroelectric capacitors. Section-III have been dedicated towards fabrication procedures of HZO based FE-FinFETs, which has been followed by the discussion of electrical characterization of fabricated devices in section-IV. In section-V we focus of explaining the experimental data by means of TCAD simulation and analytical modelling. Section-VI predicts about the impact on the device performance ferroelectric layer thickness scaling for different technology nodes. The last part of this paper is dedicated to draw conclusion of this work.

II. FABRICATION AND CHARACTERIZATION OF HZO BASED FERROELECTRIC CAPACITORS

We have fabricated the ferroelectric capacitors with 10nm thick HZO and the experimental data obtained from the fabricated devices are used for conducting TCAD simulation of transient negative capacitance Fin-FET (TNC-FinFET) using Preisach model of hysteresis. The capacitors are fabricated using an n+ silicon wafer. Thermal oxidation was performed to germinate a 2nm-thick interfacial layer of silicon-dioxide(SiO$_2$) on top of n+ Si wafer to prevent the charge carriers from silicon to get trapped into the intrinsic defect sites in HZO. The bottom and top TiN electrode have been deposited by physical vapour deposition (PVD) method. The HZO layer was deposited by atomic layer deposition (ALD) method. Post deposition of top TiN metal the whole stack was subjected to rapid thermal annealing (RTA) at 700°C for 30 seconds. Finally, the capacitors are patterned and etched with an active area of 10000 µm$^2$. Fig. 2.(a) and Fig.2.(b). shows the schematic of the capacitor and TEM micrograph of the capacitor. The elemental composition has been shown by the EDS analysis in Fig.2.(c).

The fabricated capacitors were subjected to triangular waveform of 10KHz frequency and 6V peak to peak voltage. The polarization response under this applied voltage was captured by radiant technology precision multi-ferroic measurement system.

![Fig.3.](image) (a) Measured polarization vs voltage(P-V) curve and (b) corresponding capacitance vs voltage curve shows the position of coercive voltage around 1V and the remnant polarization ($P_r$) of 20µC/cm$^2$ and the saturation polarization ($P_s$) as 40µC/cm$^2$. (c) capacitor structure for TCAD simulation. (d) Capacitance vs voltage(C-V) characteristics obtained from TCAD simulation.

Fig.3.(a), shows the measured polarization vs applied voltage curve(P-V) and Fig.(b), shows the corresponding capacitance vs voltage(C-V) curve. The extracted values of coercive voltage, remnant polarization and saturation polarization were used for conducting transient TCAD simulation to unravel the
capacitance response of HZO with changing electric field. The Preisach multi-domain model was adopted for describing the physics of ferroelectric layer instead of landau formalism during the TCAD simulation.

The primary aim for conducting TCAD simulation for the ferroelectric capacitor was to perceive the region where, transient negative capacitance effect is effective in the ferroelectric-dielectric stack. The parameter values for ferroelectric layer was obtained from the experimentally calibrated P-V and C-V curve as shown in Fig.4(a) and Fig.3(b) where the coercive field ($E_c$) and remnant polarization ($P_r$) was given by, $E_c=1MV/cm$ and $P_r=20 \mu C/cm^2$.

Fig. 4(a) shows the schematic of the gate stack and Fig.4(b) illustrates the equivalent circuit of the ferroelectric gate-stack used for TCAD simulation. Usually, in double-gate FinFET (DG-FinFET) the body is very thin. Since the thin body region is typically fully depleted, it is reasonable to assume $C_{dep}$ to be zero. Thus, total gate capacitance ($C_{total}$) is modeled with:

$$\frac{1}{C_{total}} = \frac{1}{C_{FE}} + \frac{1}{C_{MOS}}$$  \hspace{1cm} (1)

Therefore, a simulation experiment specifically for extracting $C_{FE}$ is designed according to (1). $C_{FE}$ is obtained by extrapolation provided that multiple data points for $C_{total}$ and $C_{MOS}$ are available. We kept the thickness of FE layer fixed, while varying the interfacial oxide layer’s thickness ($T_{ox}$) to be 4nm and 5nm, respectively, in order to modulate $C_{MOS}$. Fig. 4(c) shows the resulting C-V characteristics and Fig. 4(d) shows the extracted value of ferroelectric capacitance ($C_{FE}$). One can contemplate from Fig.4(d) that before reaching to the negative capacitance region, the capacitor traverses through a region of singularity, which is resulted from the “polarization catastrophe” mentioned by Feynman [35]. The negative capacitance region is laid out from -2V to 0.25V. In the next section we shall focus onto the impact of this transient negative capacitance for ameliorating the short-channel effects and its correlation with device dimensions.

III. FABRICATION OF FE-FINFET

TNC-FinFET with a 10nm HZO layer as ferroelectric stack is fabricated on silicon on insulator (SOI) wafers using gate first process. Standard cleaning of SOI wafer is performed at first to trim the silicon layer down to 30nm. E-beam lithography is used during each fabrication step to maintain the uniformity and achieve high accuracy in terms of dimensions of the devices. We have fabricated devices with fin width 20nm and 25nm. The gate lengths are varied as 50nm, 70nm, 80nm and 150nm. We used two steps annealing for crystallization of HZO and diffusion of source-drain dopants. RTA is performed for obtaining the ferroelectric phase in HZO and microwave annealing (MWA) was performed to diffuse the dopants after ion implantation.

Fig.5(a) shows the process flow for fabricating the FE-FinFET devices. Fig.5(b) shows the TEM micrograph and Fig.5(c) shows the EDS analysis of our devices.
IV. CHARACTERIZATION AND MODELLING OF FE-FINFET

The electrical characterization of the fabricated devices was done by B1500A semiconductor characterization module. N-type devices were subjected to slowly varying gate voltage from -1V to 3V in both forward and in reverse direction. The drain voltage was kept at a constant value of 100mV. The counterclockwise (CCW) swing of drain current vs gate voltage (I_{d}-V_{g}) curve is attributed to ferroelectric dominant switching. The threshold voltage was extracted by constant current method at 200nA.

Fig.6(a) shows the I_{d}-V_{g} curve of an N-type FinFET with HZO as ferroelectric stack in gate stack. The CCW swing manifests FE dominant switching in the device. The S.S vs I_{d} curve in Fig.6(b) shows the existence of S.S<60mV/dec over four decades. It should be noted that S.S is less than 60mV/dec mostly during reverse sweep. The subthreshold region was considered to be extant from 100pA to 200nA to obtilerate the impact of gate current in the subthreshold slope, which has a maximum value around 10pA in our fabricated devices. Fig.6(c) shows the minimum S.S vs hysteresis trend. The minimum S.S was calculated as a point wise S.S above 100pA and below 200nA. The cluster of points having S.S less than 60mV/dec increases with increasing hysteresis, evincing a direct correlation between ferroelectric switching and S.S. Fig.6(d) shows the gate length dependence of S.S. It is evident from the figure that average value of S.S increases with increasing gate length. In the following section we shall divulge our focus into analyzing this trend with TCAD simulation and modelling.

Fig.6. (a) Id-Vg characteristics showing counterclockwise swing proves that the device is ferroelectric dominant. (b) The S.S vs I_{d} curve shows that subthreshold slope stays below 60mV/dec for four decades. (c) MW vs S.S curve shows that the subthreshold slope goes below 60mV/dec mostly during reverse sweep. (d) The box plot shows that the impact of TNC is more stout in short channel devices.

V. TCAD SIMULATION AND MODELLING

In this section TCAD simulation is explored to analyze and fathom the impact of scaling observed in the previous section of TNC FinFET. We have used double-gate FinFET (DG-FinFET) structure for this purpose. The device structure has been shown in Fig.7(a). and the Fig.7(b) shows the device parameters considered for TCAD simulation. The I_{d}-V_{g} characteristics shown in Fig.7(c) shows excellent reduction of off current, leading to mitigation of threshold voltage roll-off. Fig.7(d) illustrates the trend that the SS improvement becomes more significant as the gate length become shorter. For instance, The SS improvement at channel length of 25 nm is as much as 54.67%. Such observation is akin to the experimental result shown in Fig.6(d).

We would like to further develop an analytical model to quantitatively explain the above phenomenon. The TNC in the gate-stack amplifies the internal gate voltage to improve device performance. This amplification ratio is given by [24]:

\[
A_{V} = \frac{\mathcal{N}_{MOS}}{\mathcal{N}_{G}} = \frac{|C_{FE}|}{|C_{MOS}| - C_{MOS}(C_{d})} \quad (2)
\]

The value of C_{MOS} is influenced by the drain induced barrier lowering (DIBL) effect, which is translated to SS improvement. The focus in [24] is on drain biasing effect, whereas we focus on channel length dependence in this study.

The effect of drain-side electric field coupling can be modelled with a DIBL capacitance, C_d which degrades conventional FET device performance. On the other hand, C_d may improve NC gate-stack capacitance matching. In mathematically terms, the DIBL capacitance is expressed as follows in Eq. (3), based on a simplified version of BSIM-CMG sub-threshold swing degradation model [25]:

\[
C_{d} = \frac{0.5}{\cosh(DVT_{d})^{-1}} \quad (C_{dSC}) \quad (3)
\]
As $L_g$ scales down, according to Eq. (3), DIBL effect becomes more severe since $C_d$ increases. This leads to a larger value of $C_{MOS}$. Consequently, the $C_{MOS}$ value would approach $|C_{FE}|$. As a result, the denominator in Eq. (2) becomes smaller, and $A_V$ increases. The larger $A_V$ also translates to better SS, as can be seen from the following expressions for the relationship between SS and $A_V$ [24]:

$$SS_{\text{FinFET}} = 60\text{mV/dec} \left(1 + \frac{C_d}{C_{ox}}\right)$$

$$SS_{\text{NC-FinFET}} = SS_{\text{FinFET}} \times \frac{\partial V_G}{\partial V_{MOS}} = SS_{\text{FinFET}} \times A_V^{-1}$$

According to Eqs. (4) and (5), the SS improvement for NCFETs over regular FinFETs is determined by $A_V$. This explains the more significant SS improvement at shorter $L_g$ where $A_V$ becomes larger due to larger drain coupling capacitance, $C_d$. The parameters DVT and CDSC in Eq. (3) are calibrated through fitting to TCAD-simulated SS v.s. $L_g$ characteristics, as shown in Fig. 3. The value of DVT is found to be $1.292 \times 10^{-4}$, whereas CDSC is $1.292 \times 10^{-18}$ F. Eq. (5) is able to accurately predict SS degradation with and without ferroelectric effects. This validates the correctness of our analytical model and sub-circuit concept.

It is important to note that according to Eq. (2), the improvement of SS is based on the assumption that $C_{MOS}$ does not exceed $|C_{FE}|$, which is true throughout this study.

![Simple equivalent capacitance network model to take into account DIBL effect.](image)

Fig. 8. Simple equivalent capacitance network model to take into account DIBL effect.

VI. COMPACT MODELING AND SCALING PREDICTION

To anticipate the trend of NCFET technology scaling we have performed a Spice simulation using Verilog-A model and PTM technologies. Predictive Technology Model (PTM) [36] provides a set of BSIM-CMG [37] based transistor models to anticipate FinFET transistor characteristics at 20nm, 16nm, 14nm, 10nm and 7nm. We connect the calibrated FE capacitor Verilog-A model [38] to the gate terminals of PTM-based FinFET model and perform transient SPICE simulation to estimate NCFET device characteristics at various technology nodes.

As shown in Fig. 9, a minimum-SS point exists for each FE thickness. Also, the FE thickness is expected to scale with technology. As a consequence, the availability of thin FE films is important. The specific optimum point depends on the matching of transistor and FE capacitances. Therefore, even though the SS values shown here are not very low, further transistor design for capacitance matching will help reach an optimal SS.

![NCFET technology scaling prediction using compact model.](image)

Fig. 9. NCFET technology scaling prediction using compact model.

CONCLUSION

We have fabricated ferroelectric FETs to fathom the existence of transient negative capacitance in multidomain ferroelectric stack. Approximately 31% of the fabricated devices display S.S less than $60\text{mV/dec}$, corroborating that traversing through quasi-static “S” path is not necessary to attain differential negative capacitance. The impact of negative capacitance is feistier in small channel devices, which has also been successfully confirmed by TCAD simulation. The subthreshold swing improvement for short channel FinFETs is found to be more significant than long channel ones, due to improved capacitance matching by the larger drain-side coupling capacitor. Analytical model has been developed to prove the electrostatics improvement via gate voltage amplification from ferroelectric gate stack. We have also used PTM-based compact model to anticipate the impact of FE film thickness scaling, which necessitates quality FE thin films.

ACKNOWLEDGEMENT

We are grateful to Taiwan Semiconductor Research Institute for nanofabrication facilities and services, and Dr. Wen-Jay Lee and Nan-Yow Chen of National Center for High-Performance Computing for helpful suggestions on AI computation.

REFERENCES

[1] Darsen Lu, Sourav De, Mohammad Aftab Baig, Bo-Han Qiu and Yao-Jen Lee, “Computationally efficient compact model for ferroelectric field-effect transistors to simulate the online training of neural networks” Accepted Manuscript online 11 June 2020 IOP Publishing Ltd.

[2] S. De et al., “Tri-Gate Ferroelectric FET Characterization and Modelling for Online Training of Neural Networks at Room Temperature and 233K,” 2020 Device Research Conference (DRC), Columbus, OH, USA, 2020, pp. 1-2, doi: 10.1109/DRC50226.2020.9135186.

[3] Salahuddin and S. Datta, “Can the subthreshold swing in a classical FET be lowered below $60\text{mV/decade}?”,” IEEE 2008 International Electron Devices Meeting, p. 1-4, 2008 DOI:10.1109/IEDM.2008.4796789.

[4] C. K. Dabhi, S. S. Parihar, A. Dasgupta and Y. S. Chauhan, “Compact Modeling of Negative-Capacitance FDSOI FETs for Circuit...
Simulations," in IEEE Transactions on Electron Devices, vol. 67, no. 7, pp. 2710-2716, July 2020, doi: 10.1109/TED.2020.2994018.

[8] H. Amrouch et al., "Impact of Variabilization on Processor Performance in Negative Capacitance FinFET Technology," in IEEE Transactions on Circuits and Systems I: Regular Papers, doi: 10.1109/TCAS.I.2020.2990672.

[9] G. Bajpai et al., "Impact of Radiation on Negative Capacitance FinFET," 2020 IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA, 2020, pp. 1-5, doi: 10.1109/IRPS45951.2020.9129165.

[10] D. Prakash, A. Gupta, G. Palwa, J. Henkel, Y. S. Chauhan and H. Amrouch, "Impact of Interface Traps Induced Degradation on Negative Capacitance FinFET," 2020 4th IEEE Electron Devices Technology & Manufacturing Conference (EDTM), Penang, Malaysia, 2020, pp. 1-4, doi: 10.1109/EDMT47692.2020.9118008.

[11] A. D. Gaidhani, G. Palwa, A. Verma and Y. S. Chauhan, "Gate-Induced Drain Leakage in Negative Capacitance FinFETs," in IEEE Transactions on Electron Devices, vol. 67, no. 3, pp. 802-809, March 2020, doi: 10.1109/TED.2020.2967463.

[12] S. Salauhuddin, "Negative capacitance in a ferroelectric-dielectric heterostructure for ultra-low-power computing," In: Spintronics V. International Society for Optics and Photonics, p. 846111, 2012, DOI: 10.1117/12.933587.

[13] M. H. Lee, Y. T. Wei, K. Y. Chu, J. J. Huang, C. W. Chen, C. C. Cheng, M. X. Y. Chen, Y. S. Chen, L. H. Lee, M. Tsai, "Steep slope and near non-hysteresis of FETs with antiferroelectric-like HfZO for low-power electronics," IEEE Electron Device Letters, vol. 36, p. 294-296, 2015, DOI: 10.1109/LED.2015.2402517.

[14] P.-C. Chiu and V. P.-H. Hu, "Analysis of subthreshold swing and internal voltage amplification for hysteresis-free negative capacitance FinFETs," IEEE 2017 Electron Devices Technology and Manufacturing Conference (EDMT), Penang, Malaysia, 2017, DOI: 10.1109/EDMT.2017.8079886.

[15] E. Ko, J. W. Lee and C. Shin, "Negative Capacitance FinFET With Sub-20-mV/decade Subthreshold Slope and Minimal Hysteresis of 0.48 V," in IEEE Electron Device Letters, vol. 38, no. 4, pp. 418-421, April 2017, doi: 10.1109/LED.2017.2672967.

[16] C. Hu, S. Salauhuddin, C.-L. Lin, and A. Khan, "0.2 V adiabatic NC-FinFET with 0.6 mV/µm 1 ON and 0.1 mV/µm 1 OFF," IEEE 73rd Device Research Conference (DRC), p. 9-40, 2015, DOI: 10.1109/DRC.2015.717554.

[17] K. S. Li, P. G. Chen, T. Y. Lai, C. H. Lin, C. C. Cheng, C. C. Chen, Y. J. Wei, Y. F. Hou, M. H. Liao, M. H. Lee, M. C. Chen, M. J. Sheih, W. K. Yeh, F. L. Yang, S. Salauhuddin, C. Hu, "Sub-60mV-swing negative-capacitance FinFET without hysteresis," in IEEE International Electron Devices Meeting (IEDM), p. 22.6.1-22.6.4, 2015, DOI: 10.1109/IEDM.2015.7497539.

[18] J. Zhou et al., "Ferroelectric Negative Capacitance GeSn PFETs With Sub-20 mV/decade Subthreshold Swing," in IEEE Electron Device Letters, vol. 38, no. 8, pp. 1157-1160, Aug. 2017, doi:10.1109/LED.2017.2714178.

[19] Si, M., Su, C., Jiang, C. et al. Steep-slope hysteresis-free negative capacitance MoS2 transistors. Nature Nanotech. 13, 24–28 (2018). https://doi.org/10.1038/s41565-017-0010.

[20] J. Zhou et al., "Ferroelectric HfZrO5 Ge and GeSn PMOSFETs with Sub-50 mV/decade subthreshold swing, negligible hysteresis, and improved Ids," 2016 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, 2016, pp. 12.2.1-12.2.4, doi: 10.1109/IEDM.2016.7838401.

[21] P. Sharma et al., "Impact of total and partial dipole switching on the switching slope of gate-fast negative capacitance FETs with ferroelectric hafnium zirconium oxide gate stack," 2017 Symposium on VLSI Technology, Kyoto, Japan, 2017, pp. 7154-7155, doi: 10.23919/VLSIT.2017.7998160.

[22] Hoffmann M, Fenger FP, Herzig M, et al. Unveiling the double-well energy landscape in a ferroelectric layer. Nature. 2019;565(7740):464-467. doi:10.1038/s41586-018-0854-z.

[23] Khan, A., Chatterjee, K., Wang, B. et al. Negative capacitance in a ferroelectric capacitor. Nature Mater 14, 182–186 (2015). https://doi.org/10.1038/nmat4148.

[24] Song, S., Kim, Y., Park, M. et al. Alternative interpretations for decreasing voltage with increasing charge in ferroelectric capacitors. Sci Rep 6, 20825 (2016). https://doi.org/10.1038/srep20825.

[25] J. Van Houdt and P. Roussel, "Physical Model for the Steep Subthreshold Slope in Ferroelectric FETs," in IEEE Electron Device Letters, vol. 39, no. 6, pp. 877-880, June 2018, doi: 10.1109/LED.2018.2829604.