A 1.9 nW, Sub-1 V, 542 pA/V linear Bulk-Driven OTA with 154 dB CMRR for Bio-Sensing Applications

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Abstract: In this paper, a new technique for improvement on the DC voltage gain, while keeping the high-linearity in symmetrical operational transconductance amplifier (OTA) bulk-driven (BD) topology is proposed. These features are achieved by alloying two topological solutions: enhanced forward-body-biasing self-cascode current mirror, and source degeneration. The proposed concept is demonstrated through simulations with typical process parameters and Monte Carlo analysis on nominal transistors of the CMOS TSMC 180 nm node. Results indicate that the proposed OTA can achieve a very small transconductance, only 542 pA/V while keeping a voltage gain higher than 60 dB, 150 dB CMRR, and high linearity of 475 mVpp (1% THD), consuming only 1.9 nW for a supply voltage of 0.6 V. This set of features allows the proposed OTA to be an attractive solution for implementing OTA-C filters for the analog front-ends in wearable devices and bio-sensing.

Keywords: bulk-driven OTA; transconductor; self-cascode mirror

1. Introduction

The effort to develop implantable or bio-sensing battery-less biomedical instrumentation systems has been continuously challenging analog designers because of the intensified constraints arising from CMOS scaling [1–3]. Topological solutions for endowing operational transconductance amplifiers (OTAs) to process µV signals with common-mode swings in the range of tens of volts, allied to features like ultra-low power consumption, low-noise, enhanced linearity, high common-mode rejection ratio (CMRR), tiny silicon footprint, and large common-mode range (CMR) are frequently pursued by the analog circuit designers [4–18].

As a basic block in analog front-ends (AFE’s) for biosensing, the OTA-C filter with large time constants is among the most important applications for OTAs with reduced transconductance [19]. Such circuits when used in implantable/wearable biomedical applications have their design challenged by the restricted-sized on-chip integrated capacitors. In order to decrease the size of such filters, OTAs must output a very small transconductance in the order of a few nA/V, which is achieved with very low biasing currents [20] at the cost of the OTA linearity.

Among the typical OTA design techniques to increase linearity is the use of non-unity gain current mirrors [21–23] to allow higher biasing currents and maintain a low transconductance. Another well-known technique that is used to improve both OTA linearity and input signal voltage swing is the bulk-driven differential pair [1,24–29]. Unlike the gate-driven OTA topologies, the bulk-driven OTAs outputs are an alternative for a relatively lower transconductance [20,30]. In this case, the main drawback of this approach is a poor DC voltage gain, which can be improved by using several techniques [25]. An interesting and widely employed technique relies on a self-cascode topology known...
as trapezoidal or composite transistor [31–34]. Additionally, an improvement for the self-cascode transistor association was proposed in [13,35–37] allowing to increase voltage gain and decrease area usage. Therefore, in this paper, we propose a new symmetrical bulk-driven OTA topology that takes the advantages of previously described techniques, i.e., the combination of the topology presented by [23], with a bulk-driven differential pair [24], and the bulk-driven active source degeneration linearization technique adapted from [1,38]. Besides the employed combination of techniques in the OTA topology, we propose an innovative improved self-cascode current mirror (ISCCM) which is based on [35,37].

This paper is organized as follows: Section 2 describes current mirror topologies made of rectangular transistor arrays (composite transistor). The improved self-cascode current mirror that sources the proposed OTA is introduced. Section 3 presents the bulk-driven symmetrical OTAs topologies. Simulations and comparisons among the proposed BD topology, the conventional bulk-driven, and state-of-art transconductors are shown in Section 4. Finally, Section 5 presents the conclusions.

2. Current Mirrors

Current mirrors are the essential component of CMOS OTAs, and their output impedance improvement leads to OTAs with superior voltage gain and common-mode rejection. Implementing current mirrors with series-parallel associations of transistors is a design solution that allows for high current gain, reduced area usage, and less process variability compared to parallel-only current mirrors [22]. This technique was employed by [23] to achieve very low transconductance OTAs without sacrificing linearity and process variability tolerance [13,14]. Since the output transistor array has a large equivalent channel length ($L_{eq}$), the output current $I_o$ is less dependent on the output voltage $V_{out}$ variation.

Rectangular transistor arrays as illustrated in Figure 1 can be considered understood as a single transistor [31] with a higher output impedance [2,23,39]. The rectangular array, shown in Figure 1, is an $m$ by $n$ matrix of single transistors composed of $m$ parallel columns of $n$ series single transistors. The rectangular equivalent transistor aspect ratio $S_{eq-R}$ is a function of the single transistor aspect ratio $S_u$, as shown in Equation (1). The total gate area of the rectangular array is $A_T = (mn)A_u$, where $A_u$ is the gate area of the single transistor.

$$S_{eq-R} = \frac{W_{eq}}{L_{eq}} = \frac{mW_u}{nL_u} = \frac{m}{n}S_u. \quad (1)$$

Figure 2 represents an N-type improved composite transistor. It consists of a series connection of two independently forward-body-biased N-type MOS transistors $M_{N1}$ and $M_{N2}$, as first proposed in [35], and described in detail in [13,14,37], by using the ACM (advanced compact model) all-region transistor model [40].

![Figure 1. Rectangular 1\times m : n transistor array.](image)
The improved composite transistor equivalent aspect ratio $S_{eq}$ is defined as:

$$S_{eq} = \frac{S_{N1} \cdot \beta S_{N2}}{S_{N1} + \beta S_{N2}} = \frac{\beta k}{\beta k + 1} \cdot S_{N1}$$  \hspace{1cm} (2)

where

$$\beta \approx e^{\frac{(n-1)\Delta V_B}{n\phi_T}}$$  \hspace{1cm} (3)

represents a correction factor for the current drain $I_D$ definition due to the difference between the body-bias of the series transistors $M_{N2}$ and $M_{N1}$ $\Delta V_B = V_{B2} - V_{B1}$, assuming the transistors are operating in weak inversion, and

$$k = \frac{S_{N2}}{S_{N1}}$$  \hspace{1cm} (4)

is the ratio between transistors $M_{N1}$ and $M_{N2}$ and physical aspect ratios $S_{N1}$ and $S_{N2}$. Figure 3a shows the conventional current mirror (CM). The ratio between transistors $M_{1B}$ and $M_{1A}$ aspect ratios $S_{1A}$ and $S_{1B}$ define the current mirror gain $A_I = S_{1B} / S_{1A}$ and attenuation $1/A_I$. In order to have a better matching for non-unity current gain, the current mirror transistors should be replaced with rectangular transistor arrays [22].

A higher current attenuation is achieved by combining parallel transistor arrays at the current mirror input, and series transistor arrays at the output. This scheme is a desirable feature for ultra-low transconductance OTAs [21,23], as it provides transconductance attenuation without decreasing linearity.

The typical cascode current mirror is a variation of the Wilson current mirror first proposed by [41]. The topology increases the output impedance in order to decrease the output current gain error. On the other hand, its drawback is a lower output voltage swing, which will be solved by the proposed current mirror as follows.

An alternative topology to a typical cascode, is the self-biased self-cascode current mirror (SCCM), first proposed by [42], which uses composite transistor arrays in a trapezoidal shape, which are equivalent to single transistors with increased output impedance. The trapezoidal geometry means that the top composite transistors, i.e., those related to drain portion must have a greater aspect ratio than the bottom transistors, i.e., corresponding to source portion, so this kind of composite transistor can be made by arranging their drain transistors in an array connected to a series array corresponding to source transistors (the smaller base of the trapezoid) [43]. This topology is recommended for low input currents and unity current mirror gain, but it is not appropriate for higher currents or very large current gains, since it would require a very large area. Nevertheless, the trapezoidal current mirror can still use the parallel-series technique for current attenuation [21,22] by replacing the output series transistor array with a trapezoidal transistor array, as shown in Figure 3b. This is possible because there is no need for trapezoidal arrays at the mirror input for non-unity gains.
Figure 3. Self-biased current mirrors: (a) conventional current mirror with rectangular transistor arrays (CM) [22], (b) trapezoidal output current mirror (SCCM) [42], and (c) improved self-cascode current mirror (ISCCM).

By taking (2), $\beta = 1$, and since $M_{1B}$ and $M_{2B}$ bulk terminals are connected to each other, the current gain $A_I$ can be expressed as

$$A_I = \left( \frac{S_{2B}}{S_{1B} + S_{2B}} \right) \cdot \frac{S_{1B}}{S_{1A}}$$

(5)

For $S_{2B} \gg S_{1B}$, the SCCM current gain is approximately $S_{1B}/S_{1A}$, as in the conventional parallel-series current mirror. However, this current mirror has a relatively larger output resistance, consequently, it is more tolerant to output voltage variation.

The SCCM output resistance can be further increased by independently forward-body-biasing transistors $M_{1B}$ and $M_{2B}$ by connecting their shared gate terminals to their shared bulk-terminals [37], as shown in Figure 3c. In its turn, the $k$ factor is increased by a $\beta$ factor function of the bulk-to-source voltage $V_{BS2}$, accordingly to (3), and hence the gain of the current mirror, $A_I$ is defined as

$$A_I = \frac{S_{1B} \cdot \beta S_{2B}}{S_{1B} + \beta S_{2B}} \cdot \frac{S_{1A} + \beta S_{2A}}{S_{1A} \cdot \beta S_{2A}} = \left( \frac{S_{1A} + \beta S_{2A}}{S_{1B} + \beta S_{2B}} \cdot \frac{S_{2B}}{S_{2A}} \right) \cdot \frac{S_{1B}}{S_{1A}}$$

(6)

Again, considering a high value of $\beta$, the current gain $A_I$ is approximately $S_{1B}/S_{1A}$.

For proof of concept, the above current mirrors were designed for the TSMC 180 nm technology and simulated for typical process parameters and room temperature. Table 1 summarizes the transistor arrays dimensions for each circuit.

First, by considering a fixed 1.6 nA input current $I_{in}$ and an output voltage $V_o$ sweeping from 0 to 600 mV, Figure 4a shows the output current mirrors. According to the transistor arrays dimensions, the conventional rectangular parallel-series current mirror (CM) should attenuate the input current by a $16 \times$ factor, and provide a 100 pA current. However, due to non-ideal behavior, it outputs about 125 nA, which is close to $13 \times$ attenuation. The self-cascode current mirror (SCCM) behaves similarly to CM, as $S_{2B} = 16 \times S_{1B}$. The improved self-cascode current mirror (ISCCM) has a slightly smaller attenuation, close to $12 \times$. The
main difference between these current mirrors is the output resistance $R_o = 1/(dI_o/dV_o)$, shown in Figure 4b. At the saturation region, the SCCM $R_o$ is much higher than CM, while the ISCCM is more than one order of magnitude higher.

Table 1. Transistor sizes (Figure 3).

| Mirror | Size (m × (M:N) × W/L) | Size (m × (M:N) × W/L) |
|--------|-------------------------|-------------------------|
| RCM    | $M_{1A}$ 4 × (4:1) × 1.0 μm/8.0 μm | $M_{1B}$ 4 × (1:4) × 1.0 μm/8.0 μm |
| TCM    | $M_{1A}$ 4 × (4:1) × 1.0 μm/8.0 μm | $M_{1B}$ 4 × (1:4) × 1.0 μm/8.0 μm |
|        | $M_{2B}$ 4 × (4:1) × 1.0 μm/8.0 μm |                           |
| ISCCM  | $M_{1A}$ 4 × (4:1) × 1.0 μm/8.0 μm | $M_{1B}$ 4 × (1:4) × 1.0 μm/8.0 μm |
|        | $M_{2A}$ 4 × (4:1) × 1.0 μm/8.0 μm | $M_{2B}$ 4 × (4:1) × 1.0 μm/8.0 μm |

![Figure 4](image-url)

**Figure 4.** Current mirrors comparison: (a) output current × output voltage, and (b) output resistance × output voltage for $I_{in} = 1.6$ nA.

Nonetheless, the ISCCM is not perfect. Figure 5 shows the current attenuation $1/A_1$ as a function of the input current $I_{in}$. As can be seen, the current attenuation is practically constant for the CM and SCCM, but it varies for the ISCCM, as the $\beta$ is indirectly a function of the input current.

![Figure 5](image-url)

**Figure 5.** Current mirrors attenuation as a function of input current for $V_{out} = 0.3$ V.

The ISCCM differential bulk voltage is defined as $\Delta V_B = V_{BS2} = V_{in} - V_{DS1}$. As the input current $I_{in}$ increases exponentially, $V_{in}$ increases linearly, as shown in Figure 6a. For 1 nA input, $\Delta V_B$ is approximately 100 mV. As $V_{BS2}$ is always positive, the transistors $M_{2A}$ and $M_{2B}$ are forward-body-biased. In spite of that, the drain current $I_D$ is orders of magnitude higher than $I_B$ (see Figure 6b), so $I_{in} \approx I_D$. 
Figure 6. Improved self-cascode current mirror: (a) $V_{in}$ and $V_{DS1}$ voltages × input current, and (b) drain ($I_D$) and bulk currents ($I_B$) × input current.

3. Bulk-Driven Symmetrical Operational Transconductance Amplifiers

Bulk-driven OTA topologies as illustrated in Figure 7 take advantage of the transistor bulk terminal of the differential pair to achieve higher transconductance linearity and input range rather than conventional gate-driven topologies [25,28].

The intrinsic drawback of this scheme is the reduced transconductance due to its equivalent gate-driven OTA, hence, a lower DC voltage gain. Nonetheless, biomedical applications frequently involve slow varying quantities and the supposed disadvantage, i.e., the very-low transconductance turns beneficial as analog signal filters with very low cut-off frequencies using relatively small-sized integrated capacitors are essential. Moreover, the lower voltage gain can be addressed with techniques such as positive feedback [25], cascode gain stages [44], and transistor arrays [31,45].
Figure 7b shows the proposed topology which relies on the conventional symmetrical OTA shown in Figure 7a with a key aspect. The current mirrors are built by improved self-cascode configuration [36], according to Figure 3c. This scheme allows increasing the OTA DC voltage gain as also the CMRR. Further, in this work, the conventional BD-OTA (see Figure 7b) makes use of the same active source degeneration technique [1,38,46] employed in the input differential pair to keep fair comparisons between the topologies.

To describe the topology behavior, we use the ACM transistor model (more details in [47]), hence the BD-OTA topology can be explained as follows: the transconductance $G_{\text{mb}}$ is a function of the differential pair transconductance $g_{\text{mb1}}$, the source degeneration factor $a$ [46], and the current mirror factor $N$, as defined by (7). The differential pair transconductance $g_{\text{mb1}}$, defined by (8) and is attenuated relative to the gate-driven OTA by a factor of $(n - 1)$.  

$$G_{\text{mb}} = \frac{g_{\text{mb1}}}{aN},$$  

$$g_{\text{mb1}} \approx \frac{n - 1}{n} g_{\text{ms1}} \approx \frac{n - 1}{n} \frac{I_S}{\phi_I} \left( \sqrt{1 + i_f} - 1 \right).$$  

Another advantage of the bulk-driven topology over the gate-driven approach is the reduced minimum supply voltage needed for operation, since the differential pair transistors $M_{1A-B}$ and source degeneration transistors $M_{2A-B}$ gate terminals are connected to the ground instead of to the input signal voltages, which has a typical common-mode voltage of half the supply voltage. It is worth noting that, in order to $M_{1A-B}$ operate in the saturation region, $V_{GS1}$ should be greater than the sum of $V_{GS4}$ and $V_{DSAT1}$, which is achieved by assuring that $i_f1$ is sufficiently greater than $i_f4$ [38,46].

The differential pair is composed of the transistors $M_{1A-B}$, and the active source degeneration transistors $M_{2A-B}$. The ratio between the differential pair and the source degeneration transistor aspect ratios $S_1/S_2$ is 4 for the earlier explained reasons and is achieved by using rectangular transistor arrays with the same area. The ratio between the differential pair and the tail current source transistors aspect ratios $S_1/S_3$ is sixteen, consequently, since the drain currents are the same, the ratio of their forward inversion level $i_f1/i_f3$ is also 16. The current mirrors use the series-parallel technique [23] to achieve a $16 \times$ current attenuation.

As sketched in Figure 7, the conventional BD-OTA, and the proposed one differs because of their body biasing and their current mirror schemes according to Figure 7a,b, respectively. Both the designed conventional and proposed OTAs are composed of the same transistors with the same dimensions. The transistors’ sizes of both topologies are summarized in Table 2.

### Table 2. Transistor sizes (Figure 7).

| Trans. | Size (m × (M:N) × W/L) | Trans. | Size (m × (M:N) × W/L) |
|--------|-------------------------|--------|-------------------------|
| $M_{1A-B}$ | $4 \times (1:4) \times 3.0 \mu m/8.0 \mu m$ | $M_{2A-B}$ | $2 \times (1:8) \times 3.0 \mu m/8.0 \mu m$ |
| $M_{3A-B}$ | $4 \times (1:4) \times 3.0 \mu m/8.0 \mu m$ | $M_{3C-E}$ | $4 \times (1:4) \times 3.0 \mu m/8.0 \mu m$ |
| $M_{4A-B}$ | $4 \times (1:4) \times 3.0 \mu m/8.0 \mu m$ | $M_{4C-D}$ | $4 \times (1:4) \times 3.0 \mu m/8.0 \mu m$ |
| $M_{5A-B}$ | $4 \times (1:4) \times 3.0 \mu m/8.0 \mu m$ | $M_{5C-E}$ | $4 \times (1:4) \times 3.0 \mu m/8.0 \mu m$ |
| $M_{6A-B}$ | $4 \times (1:4) \times 3.0 \mu m/8.0 \mu m$ | $M_{6C-D}$ | $4 \times (1:4) \times 3.0 \mu m/8.0 \mu m$ |

Figure 8 illustrates the layout of the conventional and the proposed BD-OTA. It is possible to observe a very small difference between both topologies, with the tiny occupied area of only 0.00867 mm$^2$ and 0.0143 mm$^2$, for conventional BD-OTA and the proposed BD-OTA, respectively.
Figure 8. Layout designs of the BD-OTAs. (a) Conventional BD-OTA layout. (b) Proposed BD-OTA layout.

4. Simulation Results

In this section, the post-layout simulation results referring to a TSMC 180 nm CMOS process for the conventional BD-OTA, and the proposed one, are reported. The circuits are considered to operate under the same conditions, i.e., 27 °C temperature, $V_{DD}$ equal to 0.6 V, $I_{bias}$ equal to 100 pA, besides the typical process parameters. Characteristics from both OTAs were obtained by simulating the four testbenches shown in Figure 9. Figure 9a shows the integrator test bench used in the AC and DC simulations. This scheme allows the evaluation and comparison of DC open-loop gain, as also the gain-bandwidth product (GBW) of each OTA version. Then, Figure 10a shows the open-loop gain AC simulation results, and Figure 10b shows the DC simulation results.

It can be noted that the use of improved mirrors increases DC gain without changing considerably the gain-bandwidth product of the OTA versions using the same differential pair, as they are biased with the same current. As expected, the proposed BD OTA with the enhanced mirror has lower transconductance, while keeping higher gain and the same linearity than the typical BD topology.

Figure 9. Cont.
As the power supply rejection ratio (PSRR) is equal to the OTAs DC gain, there is a unity gain voltage between supply and output voltages. The common-mode rejection ratio (CMRR) is inherently increased by the use of improved mirrors, as the current source transistors also use improved self-biased cascode configuration. The CMRR and PSRR can be noted in Figure 10c,d, respectively. Table 3 summarizes the AC simulation results.

**Table 3. Integrator simulation results summary.**

|                      | Conventional BD-OTA | Proposed BD-OTA |
|----------------------|----------------------|-----------------|
| DC gain (dB)         | 44.5                 | 64.2            |
| CMRR (dB)            | 114                  | 154             |
| PSRR (dB)            | 88.7                 | 124             |
| GBW (Hz)             | 78.47                | 83.14           |

**Figure 9. OTA testbenches.** (a) OTA-C integrator. (b) Transconductor (Symmetrical). (c) Transconductor (asymmetrical). (d) OTA-C low-pass filter. (e) Unity gain buffer.

**Figure 10. Integrator test bench simulation results.** (a) AC voltage gain transfer function. (b) DC voltage gain transfer function. (c) AC CMRR transfer function. (d) AC PSRR transfer function.
Figure 9c shows the testbench used in the DC simulations to compare the transconductance linearity of each OTA version. Figure 11a–c show, respectively, the output current, transconductance, and transconductance error for the conventional BD-OTA and for the proposed one.

![Graphs showing output current, transconductance, and transconductance error](image)

**Figure 11.** Transconductor testbench simulation results. (a) Output current. (b) Transconductance. (c) Transconductance error. (d) Normalized transconductance.

Table 4 summarizes the transconductance and impedance simulation results for $I_{\text{bias}}$ equal to 100 pA. Notice that BD OTAs have finite DC input impedances ($1/G_i$) as large as their output impedances ($1/G_o$), which reduces considerably the effectiveness of the gain improving technique in practical use, where the OTAs are cascaded in OTA-C filters.

**Table 4.** BD-OTAs DC results.

|                | Conventional BD-OTA | Proposed BD-OTA |
|----------------|---------------------|-----------------|
| $G_i$ (fA V$^{-1}$) | 77.3                | 78.1            |
| $G_m$ (pA V$^{-1}$) | 506                  | 542             |
| $G_o$ (fA V$^{-1}$) | 3024.5               | 311.6           |
| $A_v$ ($G_m/G_o$) | 167.3               | 1739.4          |

In Figure 11d, the transconductance normalized with respect to the supply voltage $V_{\text{DD}}$ is shown. It is possible to notice that both OTA versions work properly from a minimum $V_{\text{DD}}$ of about 300 mV, which is feasible for implants and wearable biomedical trends. Unlike conventional gate-driven OTA topologies, which are limited by the minimum common-mode input voltage $V_{\text{cmi}}$, and in which frequently are set to half $V_{\text{DD}}$ to allow the current source transistors to operate in saturation, according to mentioned this limitation is mitigated in BD topologies. Besides the mentioned aspects, it is worth noticing that the
minimum operational voltage, $V_{DD}$, is directly influenced by the current source, and the
differential pair transistors channel inversion, hence which are themselves a function of the
bias current, i.e., $I_{bias}$. In this way, a higher biasing current would result in a larger linear
input range and greater transconductance, on the other hand, also a higher minimum $V_{DD}$.

Figures 12a,b and 13a,b show the nominal output current and its resulting transcon-
ductance for symmetrical and asymmetrical input voltage, according to the testbenches
shown in Figure 9b,c, respectively. For the asymmetrical test, the inverting input is kept
constant at $V_{cm} = V_{DD}/2$, so $-300 < \Delta V_{in} < 300$ mV, while, for the symmetrical input,
both OTA inputs are at $V_{cm}$ for $V_{in} = 0$ V, and the differential input voltage excursion is
doubled to $-600 < \Delta V_{in} < 600$ mV. Moreover, for the asymmetrical testbench, the common
mode input voltage $V_{cm}$ varies with the input voltage $V_{in}$, so $V_{cm} = V_{in}/2 + V_{cm}$. For the
symmetrical testbench, $V_{cm}$ is constant, as the average of the inverting and non-inverting
input voltages are the same. It can be noticed, for both cases, that as the biasing current
$I_{bias}$ increases, the transconductance $G_m$ increases almost proportionally.

![Figure 12](image1.png)

**Figure 12.** Output current $I_o$ for (a) symmetrical, and (b) asymmetrical input voltage $V_{in}$, as a function
of $I_{bias}$.

![Figure 13](image2.png)

**Figure 13.** Nominal transconductance $G_m$ for (a) symmetrical, and (b) asymmetrical input voltage
$V_{in}$, as a function of $I_{bias}$.

For a better comparison, for different biasing currents, the transconductances were
normalized for $\Delta V_{in} = 0$, as shown in Figure 14a,b. It is clear for the asymmetrical
input that the error is larger for $\Delta V_{in} < 0$. This happens for two reasons: the parasitic
substrate current at the differential pair is extremely non-linear and the common-mode
input voltage goes above the limit for $I_{bias} = 10$ nA. For symmetrical input, the resulting
$G_m$ is also symmetrical and the range is twice as high. It can also be noted that the shape
of the curve changes as the current increases, which is expected, as the differential pair inversion increases.

\[ G_{m} \text{ (Normalized)} \]

\[ V_{in} \text{ [mV]} \]

\[ -500 \quad -250 \quad 0 \quad 250 \quad 500 \]

\[ 0.6 \quad 0.7 \quad 0.8 \quad 0.9 \quad 1.0 \quad 1.1 \quad 1.2 \]

(a)

\[ V_{in} \text{ [mV]} \]

\[ -400 \quad -200 \quad 0 \quad 200 \quad 400 \]

\[ 0.6 \quad 0.7 \quad 0.8 \quad 0.9 \quad 1.0 \quad 1.1 \quad 1.2 \]

(b)

**Figure 14.** Normalized transconductance \( G_{m} \) for (a) symmetrical, and (b) asymmetrical input voltage \( V_{in} \), as a function of \( I_{bias} \).

It is also important to notice that for single-ended OTA applications, normally, the input is not symmetrical. This is the case with most OTA-C filters, such as those based on integrators and active loads, as depicted in the test benches shown in Figure 9a,d. For wider range and linearity, the single-ended OTA should be converted to its fully differential version, which needs extra biasing circuits for its output common-mode definition.

As previously explained, the parasitic input current is one of the causes of transconductance asymmetry. This parasitic current is shown in Figure 15a, and is a function of the input voltage and biasing current. There is a single point where the input current is zero, which happens when the differential pair PMOS transistor bulk-terminal voltage is equal to its source-terminal voltage. For input voltages below this point, the transistor is forward-body-biased and the parasitic current grows exponentially. For voltages above this point, the parasitic current is almost constant, consequently, the input conductance is very small. Figure 15b shows the OTA output current for both inputs at \( V_{DD}/2 \) and the output sweeping from 0 to 600 mV. As can be seen, the output current, even considering that the current mirrors attenuate the differential pair output current, is considerably larger than the parasitic current for a large range.

\[ I_{in} \] (a)

\[ I_{o} \] (b)

**Figure 15.** Nominal (a) input current \( I_{in} \times \) input voltage \( V_{in} \), and (b) output current \( I_{o} \times \) output voltage \( V_{o} \), as a function of \( I_{bias} \).

The input and output conductances can be derived from the input and output currents, as shown in Figure 16a,b, respectively. It is worth noting that for OTA-C filter applications, the OTA outputs terminals will be connected to other OTAs input terminals. The main
advantage of the proposed improved self-cascode current mirror is to decrease the output conductance as it increases the output resistance. If the input conductance of the subsequent stage is greater than the output conductance, the technique effectiveness is reduced.

![Input Conductance Graph](image1)

![Output Conductance Graph](image2)

**Figure 16.** Normalized (a) input conductance $G_{ii}$, and (b) output conductance $G_o$ as a function of $I_{bias}$.

In order to compare the linearity OTAs, the unity gain low-pass OTA-C filter testbench shown in Figure 9d was used in DC and transient simulations. Figure 17a,b show, respectively, the DC transfer functions, transient, and the total harmonic distortion (THD) for both OTAs. It is possible to observe that the BD OTAs have almost the same full input range. Figure 17b shows the total harmonic distortion versus input plotted as a function of input signal amplitude. For both OTAs, one can observe that THD is lower for smaller signal amplitudes. They exhibit approximately the same amount of distortion of 0.07% as a result of a 300 mV amplitude input signal at 100 mHz. As the input voltage amplitude increases, the proposed OTA reaches $\approx 1\%$ THD ($-39.8$ dB), SNR equal to 56.6 dB for a $V_{in-pp} = 405$ mV at 100 mHz signal.

![Transfer Functions Graph](image3)

![Total Harmonic Distortion Graph](image4)

**Figure 17.** Low-pass testbench simulation results. (a) Transfer functions. (b) Total harmonic distortion.

Figure 18 shows the input-referred noise (IRN) for both OTA versions configured as a unit-gain buffer. Since both OTA versions have the same transistor dimensions, differing only by the adopted current mirror topology, there is a slight difference in IRN of conventional BD-OTA and the proposed one. The IRN in the proposed topology is equal to $246 \mu V_{RMS}$, and $237 \mu V_{RMS}$ in the other, both obtained by integrating noise from 10 mHz–1 kHz.
By using the transconductor (Figure 9c) and low-pass filter (Figure 9d) testbenches, 500 runs of Monte Carlo have been carried out for evaluation of transconductance and offset voltage, respectively. Figure 19a,b show the results for the Monte Carlo process and mismatch analysis of the proposed BD-OTA. These results are summarized in Table 5. On this basis, it is possible to conclude that the proposed BD-OTA besides a lower transconductance feature, has a considerably less input voltage offset than the conventional BD-OTA.

Table 5. Monte Carlo simulation results.

|                | Conventional BD-OTA | Proposed BD-OTA |
|----------------|---------------------|-----------------|
| \( G_m \) \( \bar{x} \) (pA/V) | 506.6              | 546.58          |
| \( G_m \) \( \sigma \) (pA/V) | 7.61               | 7.56            |
| \( G_m \) \( \sigma / \mu \) (%) | 1.5                | 1.38            |
| \( V_{os} \) \( \bar{x} \) (\( \mu \)V) | 429.8              | 61.47           |
| \( V_{os} \) \( \sigma \) (mV) | 3.16               | 3.15            |

Table 6 compares the performance of the proposed OTA with the state-of-art low-transconductance OTAs. The previous work proposed by us [48] presented a 450 pA/V OTA with small power consumption but lower gain, CMRR, and PSRR, despite being based on non-unitary current gain through the splitting current technique, it achieved a poorer performance with respect to the present work. In [49], a low-transconductance amplifier has been proposed based on the channel-length-modulation effect (Early effect). This solution
shows a high IRN. Such an IRN is 3x smaller in the proposed topology while keeping lower transconductance, power consumption, and higher CMRR as also PSRR features. The OTA proposed by [28] is similar to the conventional OTA presented in this work. The difference is in the rectangular arrays used to increase the gain and in no linearization technique employed. Another low-$G_m$ topology presented by [50] uses a linearization technique that relies on a combination of source degeneration with an active attenuator. Despite the valuable linearity and gain achieved, the power consumption, and transconductance may not be suitable to the constraints of biomedical implants or bio-sensing operations. The architecture proposed by [51] is another channel length modulated OTA which contains the same V-I conversion scheme as presented in [49] but requires a higher supply voltage.

| Feature                      | This Work (S) | [48] (S) | [49] (M) | [28] (M) | [50] (M) | [51] (M) |
|------------------------------|---------------|----------|----------|----------|----------|----------|
| Year                         | 2021          | 2021     | 2020     | 2014     | 2014     | 2009     |
| Tech. (nm)                   | 180           | 180      | 180      | 130      | 350      | 350      |
| Supply (V)                   | 0.6           | 1        | 1        | 0.25     | 5        | 5        |
| $G_m$ (nA/V)                 | 0.542         | 0.45     | 0.62–6.28| 22       | 39.5–367.2| 0.03–25,000|
| $A_v$ (dB)                   | 64            | 37       | -        | -        | 52.3–64.7| -        |
| Power (µW)                   | 0.0019        | 0.032    | 0.028–0.270| 0.01   | 160      | <300     |
| CMRR (dB)                    | 154           | 56       | 56       | -        | >44.8    | >80      |
| PSRR (dB)                    | 124           | 36       | 47       | -        | -        | >80      |
| GBW (Hz)                     | 83.14         | 6.9      | -        | -        | -        | -        |
| $V_{os}$ (mV)                | 0.06 ± 3.15   | ±20      | 25–50    | ±10.82   | -        | -        |
| IRN (µVRMS)                  | 246           | -        | 760      | 100      | -        | 635      |
| Linear range sym. input ($V_{pp}$) | 0.475 | 0.3 | 2 | - | 2 | 2.6 |
| THD (%) @ input ($V_{pp}$)   | 100.475       | 100.3    | 0.18@2  | 0.53@0.1| 0.13@2  | <1@2.6 |
| SNR (dB) @ THD (%)           | 54.8@1        | -        | 59.3@0.47| 66.5@0.13| 62@1    | -        |
| Layout area (mm²)            | 0.0143        | -        | 0.027    | 0.053    | 0.006   | 0.046    |

THD @ $V_{in} = 250$ mVpp, (M): Measured, (S): Simulated.

5. Conclusions

The paper presented a bulk-driven symmetrical OTA based on a self-cascode current mirror with source degeneration to provide a high-gain, high linearity, and low-$G_m$ topology. The proposed low-$G_m$ topology shown a valuable performance that is suitable for new biomedical IC applications. In particular, the new topology achieved the lowest power consumption compared with the state-of-art topologies, in addition to high gain, linearity, low transconductance, and IRN. Moreover, the circuit obtained the highest CMRR and high PSRR, which turns the proposed OTA into an interesting topology as a basic block for OTA-C filters.

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Abbreviations

The following abbreviations are used in this manuscript:

- ACM: Advanced Compact Model
- BD: Bulk-driven
- CMOS: Complementary Metal-Oxide Semiconductor
- CM: Current Mirror
- CMR: Common-Mode Range
- CMRR: Common-Mode Rejection Ratio
- GBW: Gain–Bandwidth Product
- OTA: Operational Transconductance Amplifier
- SCCM: Self-Cascode Current Mirror
- IRF: Equivalent Input Referred Noise
- ISCCM: Improved Self-Cascode Current Mirror
- PSRR: Power Supply Rejection Ratio
- SNR: Signal-to-Noise Ratio
- THD: Total Harmonic Distortion

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