A system design approach toward integrated cryogenic quantum control systems

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Abstract—In this paper, we provide a system level perspective on the design of control electronics for large scale quantum systems. Quantum computing systems with high-fidelity control and readout, coherent coupling, calibrated gates, and reconfigurable circuits with low error rates are expected to have superior quantum volumes. Cryogenic CMOS plays a crucial role in the realization of scalable quantum computers, by minimizing the feature size, lowering the cost, power consumption, and implementing low latency error correction. Our approach toward achieving scalable feedback based control systems includes the design of memory based arbitrary waveform generators (AWG's), wide band radio frequency analog to digital converters, integrated amplifier chain, and state discriminators that can be synchronized with gate sequences. Digitally assisted designs, when implemented in an advanced CMOS node such as 7 nm can reap the benefits of low power due to scaling. A qubit readout chain demands several amplification stages before the digitizer. We propose the co-integration of our in-house developed InP HEMT LNAs with CMOS LNA stages to achieve the required gain at the digitizer input with minimal area. Our approach using high impedance matching between the HEMT LNA and the cryogenic CMOS receiver can relax the design constraints of an inverter-based CMOS LNA, paving the way toward a fully integrated qubit readout chain. The qubit state discriminator consists of a digital signal processor that computes the qubit state from the digitizer output and a pre-determined threshold. The proposed system realizes feedback-based optimal control for error mitigation and reduction of the required data rate through the serial interface to room temperature electronics.

Index Terms—Quantum control electronics, cryogenic CMOS, spin qubit systems, optimal control, error mitigation, quantum error correction, qubit state detector, integrated readout chain.

I. INTRODUCTION

The architecture of any solid state-based quantum computation scheme, requires a platform of coherent physical qubits, strong tunable coupling with high fidelity control and readout system, together with error correction schemes to realize fault tolerant logical operations [1]-[2]. The quantum computing stack consists of different layers, that can be broadly classified into quantum hardware layer, quantum control layer and the application layer. Quantum hardware layer contains the qubits and its ancillary elements to realize quantum gates. The control layer is responsible for the control and readout of quantum gates, by facilitating the integration and scalability of the overall system. The control layer also contains gate sequencing and error correction logic, hosted on a general-purpose processor at room temperature, whose main function is to sequence and orchestrate the execution of quantum algorithms. The applications layer translates real-world problems into quantum algorithms, hosted on a server or may use the quantum serverless approach from IBM [3].

The focus of this work is to analyze the system level requirements of control systems for large-scale quantum computers with 1000 physical qubits and above. The performance of a quantum computer depends upon several factors, such as the number of physical qubits, the number of gates that can be applied, the connectivity of the device, and the number of operations that can be run in parallel [4]. Realization of fault-tolerant quantum computers requires error correction by expanding the Hilbert space of logical qubits, which in turn requires coherent operation of many physical qubits [2]. The control and readout circuitry design, therefore, must explore ways to achieve dense integration and synchronized operation.

The proposed integrated control layer, Fig.1a can deliver optimized control and readout signals, while reducing the cabling overhead in large scale quantum computing systems. It holds the potential for co-integration with high density qubit platforms such as spin systems (Fig.1b), provided the thermal loading, noise and crosstalk criteria are satisfied. Power consumption has been, by far, the most important figure of merit concerning cryogenic CMOS circuit design. We propose to shift the focus towards other important metrics such as feature size, low noise, synchronous operation, generation of low jitter clocks, and signal integrity. We introduce low power design strategies for cryogenic control systems, to facilitate signal processing within the cryostat and to reduce the data rate through serial links to room temperature, thus achieving low power through scaling offered by advanced CMOS nodes.

A major challenge in the design of an integrated control and readout system is to minimize the decoherence caused due to coupling of the quantum processor to the external environment. It has been shown that thermal loading leads to qubit dephasing and reduced relaxation times [5]-[8]. Considerable effort has been made to isolate qubits from thermal radiation, by proper thermalization of the cables and other components such as attenuators and filters in the cryostat. To suppress thermal noise, filters are employed whose stop-bands lie well outside the frequency range of qubits and their readout circuitry. To reduce the infrared coupling, blocking filters have been proposed [7]-[8]. Despite these measures, other noise sources such as 1/f noise from the control electronics can affect the qubit coherence times. It has been shown that these effects can be mitigated by using optimized control signals [9]-[10].
II. QUANTUM CONTROL SYSTEM ARCHITECTURE

The current state of the art quantum control systems use rack mounted equipments or FPGA boards with off the shelf components to generate the required set of control and readout signals. The control signals are sent through attenuators to achieve the required levels of amplitude, of the order of tens of millivolts for spin qubits [15]. The qubit readout, on the other hand requires several amplification stages, including quantum limited amplifiers, HEMT LNAs and CMOS amplifiers to boost the signal amplitude from microvolts to hundreds of millivolts required for state discrimination. The main requirements of a generic quantum control system are:

1. Generate arbitrary waveforms (eg: 2-20 GHz for spin qubits [13] and 4-8 GHz for dispersive readout at the required amplitude, phase, pulse width with acceptable signal integrity, noise, and jitter.
2. Amplify, digitize and process the readout signals from the quantum processor to determine the state of qubits and perform parity-based error correction.
3. Generate reference clocks, bias voltages and currents for different blocks within the system, while adhering to the known specifications.
4. A task scheduler to orchestrate the sequences applied to the qubit gates, the control and readout signals, the optimal position of the measurement window, recalibration and data transfer.
5. Fault detection mechanism
6. Reliability with respect to environmental changes
7. Timing and synchronization requirements

A. Rapid power ON/OFF

The quantum control hardware puts forth hard real-time requirements on the synchronization among FPGA devices and digital logic with complex clocking schemes. The clock tree is designed with reference to the system clock in the order of 100 MHz. On board phase locked loops can be used to generate high frequency clocking for blocks such as RF DAC (eg: 5 GHz reference) and ADC (eg: 500 MHz Nyquist rate). A “sync” pulse must be propagated to each logical control unit shown in Fig.1a to ensure synchronous operation of waveform generators and receiver sampling. The timing block with counters generates and propagates synchronous trigger pulses to the scheduler finite state machine (FSM), that initiates the operation of control and readout blocks. Periodic monitoring of logical qubit controller is required to ensure that the system stays in sync mode. The timing diagram of a logical controller SoC is shown in Fig.2a.

B. Control chain

The digital architecture of a sequencer system on chip Fig.2a receives commands through serial links and decodes the instructions with parameters for gate control sequences. The control signal amplitude, pulse shape, phase and duration are stored in a waveform memory. Using direct digital synthesis, arbitrary waveforms are generated using a fixed frequency reference clock. An alternate approach for power reduction uses analog mixers and local oscillators (LO) to up convert the IF signals to GHz frequency range as required by the qubit hardware [11]-[14]. Since LO phase noise not only limits the signal to noise ratio but also demands additional phase rotation capabilities at the receiver, we propose to use direct digital synthesis approach using an RF DAC. Depending upon the frequency multiplexing ratio for control signals, the power budget per qubit can be calculated.

C. Readout chain

Quantum computing systems have stringent requirements such as 99.9% on readout fidelity of the qubit state. Our targeted spin systems employ dispersive readout schemes, owing to their minimal device overhead and synergy with super conducting systems. We propose a fully integrated readout chain with RF A/D converters as qubit digitizers with an integrated amplifier front-end and a digital signal processor back-end for qubit state discrimination as shown in Fig.1c. Co-integration of CMOS low noise amplifiers with in-house developed InP HEMT LNA offer several benefits. From simulation shown in Fig.1c we infer that shifting the impedance matching to 50 Ω from 50 Ω results in 10 dB increase in the gain of an inverter-based CMOS LNA while yielding 10× reduction in power reported in table I. The simulated characteristics of single stage LNA is reported in table II. The inverter based three stage CMOS LNA characteristics with 500 Ω input impedance provides the required gain of 60 dB gain and a bandwidth of 5.8 GHz post layout in 5 nm FinFET technology.

### TABLE I: Inverter with resistive feedback ($R_F$) single stage LNA design parameters in 5 nm FinFET technology

| $I/p$ impedance | $FET_1$ size | $FET_2$ size | $R_F$ | Power |
|-----------------|--------------|--------------|-------|-------|
| 50 Ω            | 800 fins     | 600 fins     | 0.497 kΩ | 12.91 mW |
| 500 Ω           | 80 fins      | 60 fins      | 5.30 kΩ  | 1.42 mW  |

### TABLE II: Simulated single stage CMOS LNA characteristics

| Bandwidth | Gain | Noise Figure | Power |
|-----------|------|--------------|-------|
| 11.5 GHz  | 29.5 dB | <3 dB        | 1.42 mW |
powered OFF during a given instruction cycle. This could potentially mitigate qubit dephasing induced by extensive operation of the control circuitry. A built-in rapid power ON capability achieves power saving when compared to the current state of the art systems that are powered ON throughout the entire control and measurement cycle. Furthermore, by reducing the ON time, CMOS circuits can be designed with more relaxed electromigration (EM) constraints and optimized with respect to additional parasitic capacitance, which would be required to fulfill the EM specs with longer power ON times. The risk of supply noise during power ON and how it affects the gate fidelity needs to be estimated.

**B. Optimal measurement window from qubit calibration data**

Power consumption of CMOS circuits is directly proportional to their operation time. Reducing the operational time of the readout logic by using an optimized timing window derived from qubit calibration curve as illustrated in Fig. 1 enables low power operation. The efficient measurement window for a given qubit group can be computed periodically by recalibration as shown in Fig. 2a and 2b. It can be used to enable clock or power gating for digital and mixed signal blocks to achieve low power operation. A digitally synthesized qubit state discriminator based on weighted multiply and accumulate logic, consumes only 54.6 $\mu$W of power with clock gating using optimized measurement window, as opposed to 256 $\mu$W without clock gating.

**C. Data reduction using low latency error correction and optimized feedback-based control**

Latency requirements on error correction hardware is expected to play a crucial role in large scale systems. The fidelity of fast qubit gates can be increased by optimized control pulses in a closed-loop fashion [9]-[10]. Low latency error correction logic at cryogenic temperature will help to generate optimized control signals using direct digital synthesis at GHz frequency range enabling faster gates.

**D. Multiplexing**

Digital to analog converters with 2-20 GHz bandwidth and sufficient spurious free dynamic range can be used to generate control signals for multiple qubits in the current research environment [13]. The control of multiple qubits using frequency division multiple access (FDMA) has been proposed to reduce the cabling bottleneck due to scaling, however, this can be proven inefficient in some systems employing cross-resonant gates [14]. The real merits of using FDMA as opposed to 1:1 qubit to control circuit ratio for large scale error corrected systems needs in-depth evaluation. Frequency multiplexing may be favorable for dispersive readout, where RF signal bandwidth is within 4-8 GHz.
CONCLUSIONS AND OUTLOOK

A study on the design of an integrated control system for quantum computers is reported. The proposed architecture uses digitally assisted RF AWG and RF ADC designs, with techniques to enable an integrated amplification chain and qubit state discriminator. The reported method eliminates the need of noisy local oscillators and analog mixers, while reaping the benefits of scaling in advanced CMOS nodes. It enables real time equalization and re-calibration to compensate drift due to changes in the cryostat cabling. Moreover, an optimized timing window can be derived to minimize the power consumption of readout circuitry. The proposed architecture supports cryogenic digital signal processing, leading to fully integrated, feedback-based optimized cryogenic control systems. In the near term, it is expected that the control hardware evolves with changing qubit hardware specifications. Therefore, it is desirable to have a high level of programmability at low cost and compactness.

In the long-term, the features of subcomponents must be optimized, and their operating temperature must be defined in the interest of signal integrity, noise, and power consumption. Digital signal processing capabilities and state discrimination at cryogenic temperature is crucial to reduce the required data rate on serial links to room temperature. The versatility offered by the presented approach is desirable to accommodate evolving spin qubit specifications and to overcome the memory requirement, which is one of the biggest challenges of cryogenic CMOS systems. The discussed architecture also offers a solution for realizing large scale control systems with synchronized operation of multiple gates with inserted correction gates and the generation of their timing sequences.

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