Effect of Threshold Switching Selectors on One-Selector One-Resistor Crossbar Arrays

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ABSTRACT: In this paper, the influence of selector on the performance of 1S1R crossbar array memory is focused. First, a read-write circuit is designed based on the 1S1R cell model, which is a Verilog-A physical model built by our research team in the former work. Then, the parameters of selector (Vth, Vhold, RS-on, RS-off, NL) with different array sizes are calculated and analyzed. Different from the influence of selector on 1S1R cell, the read/write margin and read/write power consumption of the 1S1R crossbar array are impacted by selector significantly. Selectors with large Vth improve the write margin, but too large Vth reduce the read margin. The ON-resistance of the selector affects the read power consumption more than the OFF-resistance of the selector does, and the larger nonlinearity improves the overall performance of the crossbar array. Finally, this new 1S1R crossbar array memory is compared with 1R crossbar array memory and the result proved that the optimized memory can reduce the leakage current and power consumption to the large extent.

1. INTRODUCTION
Resistive Random Access Memory (RRAM) is considered as one of the next generations of non-volatile memory technology. It mainly uses High Resistance Status (HRS) and Low Resistance Status (LRS) as storage units and can be switched back and forth [1-3]. It is commonly used in crossbar arrays to achieve high density storage due to simple Metal-Insulation-Metal (MIM) structure and compatibility with CMOS technology.

However, there is a leakage current in the RRAM crossbar array using ohmic law Resistance Switching Elements (RSE), which will result in reading errors. In order to solve this problem, this paper proposed a series connection with each RSE in in a one-selector one-resistor (1S1R) cell to suppress the leakage current from unselected cells [4-6].

Some papers have presented the influence of selector characteristics on the performance of some crossbar arrays [7-10]. In the literature [7], Y. Li extracted threshold voltage (Vth) and holding voltage (Vhold) and obtained their variation distribution expressions to explore the influence of 32× 32 1S1R crossbar array on reading and writing processes under different bias schemes. The parameters of the selector in this literature were more specific, but the influence of its other parameters was not discussed in the literature, and the crossbar array is too small for high-density storage. L.Zhang [9] studied the influence of threshold switch (TS) selector characteristics on the performance of the whole 1S1R crossbar array, and simulated SPICE circuit by a top-down method. The literature shows that the Vth and the ON-state resistance (Rs-on) were important selector parameters, and the performance of crossbar array could be affected by TS selector parameters in multiple ways. However, SPICE model was used for 1S1R in the literature, which was characterized by complex construction, slow simulation speed, poor flexibility, so it could not be reused arbitrarily. SPICE modules are more difficult to describe high-level functions and behaviors than Verilog-A modules.
A single 1S1R model is tested in Section 2 of this paper. In the previous work, we built a 1S1R model based on Verilog-A language [11], which can more accurately reflect the influence of relevant parameters of selector on the performance of memory cell. A read-write circuit is designed for 1S1R crossbar array and simulated in Section 3. And in Section 4, a more detailed analysis of how the parameters of selector influence the memory performance is carried out. And finally a conclusion is presented in Section 5.

2. ANALYSIS OF A SINGLE 1S1R MODULE

The RRAM model published by H. Li [12] is adopted. As shown in Figure 1a, RRAM can realize the conversion between HRS and LRS when opposite voltage is applied, where the $V_{SET}\approx 1.844V$, $V_{RESET}\approx 1.1V$, and the high and low resistance status ratio is approximately $10^3$. However, the current of RRAM is still relatively high in HRS. Therefore, the selector model is introduced from the 1S1R model. And Poole-Frenkel is used to explain the I-V relationship of the selector in HRS, which is

$$I = \frac{V}{\beta} \cdot \exp\left(\frac{V - V_{OP}}{\alpha}\right).$$

(1)

where $V_{op}$ refers to the operating voltage, $\alpha$ and $\beta$ are fitting parameters. In LRS, the resistance of the selector basically remains unchanged, so a fixed resistance value $R_s$ is used to describe the I-V relationship of selector in LRS, which is

$$I = \frac{V}{R_s}.$$ 

(2)

The simulation result of 1S1R module is shown in Figure 1b. Before the forward voltage reaches the $V_{th}$, Selector remains HRS, and after it reaches $V_{th}$, the selector is turned on. When the voltage is less than $V_{hold}$, the selector is turned off again. So the main parameters of the threshold switch selector are: threshold voltage $V_{th1}$, $V_{th2}$, holding voltage $V_{hold1}$, $V_{hold2}$, Off-State Resistance($R_{s-off}$), On-State Resistance($R_{s-on}$), nonlinearity (NL). Nonlinearity is a measure of a selector's ability to calibrate under program or readout conditions. As can be seen from Figure 1c, the 1S1R model reduces the current in the LRS compared to the RRAM model, which will greatly reduce the power consumption during reading.

Figure 1 (a) I-V characteristics of single RRAM, (b) I-V characteristics of single 1S1R, (c) RRAM vs 1S1R.
3. CIRCUIT CONSTRUCTION AND SIMULATION

The schematic of crossbar array is shown in Figure 2. The 1S1R module is formed at the intersection of the word line (WL) and the bit line (BL). The worst data pattern depends on the operation being performed as well as on the state of the addressed cell, as summarized in Table I. The line resistance is set to 10 $\Omega$.

A 1/2 bias method is adopted. We mainly analyze the performance of the crossbar array from the following three perspectives: read margin (RM), write margin (WM) and read power (Pr).

- **Read Margin (RM)**, which is a worst case measure of the separation between the sensed-out on-states and off-status levels. Typically, a current-based definition is adopted for the RM:

$$RM = \frac{I_{\text{sense(on)}} - I_{\text{sense(off)}}}{I_{\text{sense(on)}}} \cdot 100\%.$$  (3)

Where $I_{\text{sense(on)}}$ is the readout current sensed on the selected bit-line for reading on state. $I_{\text{sense(off)}}$ is the readout current sensed on the selected bit-line for reading off state.

- **Write margin (WM)**, which is a worst case measure of the access voltage transfer to the selected cell. Commonly, a voltage-based definition is employed for the WM:

$$WM = \frac{V_{\text{SEL}}}{V_{\text{applied}}} = \frac{V_{\text{SEL}}}{V_{\text{BLS}} - V_{\text{WLS}}} \cdot 100\%.$$  (4)

Where $V_{\text{SEL}}$ is the voltage on the selected cell, $V_{\text{applied}}$ is the applied voltage, $V_{\text{BLS}}$ and $V_{\text{WLS}}$ is the voltage on the bit line and word line.

- **Read POWER (PR)**, which is the total power consumed by the crossbar array during read operations.

$$PR = P_{\text{select}} + P_{\text{half-select}} + P_{\text{no-select}}.$$  (5)

Where $P_{\text{select}}$, $P_{\text{half-select}}$, $P_{\text{no-select}}$ is the power consumption of selected cell, half-selected cells and no-selected cells.

Figure 2. Simulation of crossbar array. SEL: selected cell. WLHS: WL half-selected cell. BLHS: BL half-selected cell. NS: no-selected cell. WLS: selected WL. BLS: selected BL. WLNS: WL unselected. BLNS: BL unselected. $R_{\text{wire}} = 10\Omega$ / cell.

| SET   | RESET  | READ HRS | READ LRS |
|-------|--------|----------|----------|

Table 1. Worst Case Data Pattern
Figure 3 shows the simulation results of 1S1R module in the read-write circuit. The voltage drop in BL and WL is showed in figure 3a and figure 3b, and the change of current in 1S1R module is shown in figure 3c.

Figure 4a, an increase in $V_{\text{th}1}$ results in an increase in the minimum read voltage. However, since the reset voltage is about -1.1V, when the $V_{\text{th}1}$ is greater than 1V, the required minimum read voltage is also greater than 1V, which is very close to the reset voltage and can cause serious reading errors. So $V_{\text{th}1}$ is limited to 1V to ensure that the read voltage cannot change the state of the memory. As shown in figure 4b, the power consumption of reading will increase as $V_{\text{th}1}$ increases. The larger $V_{\text{th}1}$ is, the greater the read voltage is required to turn on the selector. However, higher read voltages will inevitably increase power consumption, and higher read voltages may cause half selected and unselected cells to be turned on incorrectly. In crossbar arrays, the power consumption is mainly affected by other half-selected or unselected cells. Therefore, with the increase of the size of the crossbar array, if the selector cannot control the half-selected cells and the unselected cells not being turned off, the increase of power consumption will become more obvious and rapid. As shown in figure 4c, $V_{\text{th}1}$ has little impact on reading margin. According to the reading margin formula Eq.(3), with the increase of $V_{\text{th}1}$, the on-state current and off-state current of selector change in the same trend.

4. RESULTS AND DISCUSSION
In figure 4a, an increase in $V_{\text{th}1}$ results in an increase in the minimum read voltage. However, since the reset voltage is about -1.1V, when the $V_{\text{th}1}$ is greater than 1V, the required minimum read voltage is also greater than 1V, which is very close to the reset voltage and can cause serious reading errors. So $V_{\text{th}1}$ is limited to 1V to ensure that the read voltage cannot change the state of the memory. As shown in figure 4b, the power consumption of reading will increase as $V_{\text{th}1}$ increases. The larger $V_{\text{th}1}$ is, the greater the read voltage is required to turn on the selector. However, higher read voltages will inevitably increase power consumption, and higher read voltages may cause half selected and unselected cells to be turned on incorrectly. In crossbar arrays, the power consumption is mainly affected by other half-selected or unselected cells. Therefore, with the increase of the size of the crossbar array, if the selector cannot control the half-selected cells and the unselected cells not being turned off, the increase of power consumption will become more obvious and rapid. As shown in figure 4c, $V_{\text{th}1}$ has little impact on reading margin. According to the reading margin formula Eq.(3), with the increase of $V_{\text{th}1}$, the on-state current and off-state current of selector change in the same trend.

Figure 4. Relationship between read performance and $V_{\text{th}}$ of selector, including: a minimum read voltage, b read power consumption, c read margin.
However, $V_{th}$ has little impact on reading margin. In figure 5, $V_{th}$ has a great influence on writing margin and its power consumption. On the whole, small $V_{th}$ makes the half-selected or unselected cells subdivide a certain voltage of the selected cell, reducing writing margin. And writing power increases as more and more half-selected and unselected cells are opened.

Figure 5 The effect of $V_{th}$ on write margin

In conclusion, we hope that $V_{th}$ can be as small as possible in reading operation and as large as possible in writing operation. Therefore, based on the limit of reading voltage mentioned earlier, the $V_{th}$ is set between 0.8V and 1.0V.

$V_{\text{hold1}}$ refers to the minimum voltage that keeps selector open, and it generally changes correspondingly with the change of the threshold voltage of selector. The $V_{\text{hold}}$ slightly lower than the $V_{th}$ is enough, so the $V_{\text{hold1}}$ is set between 0.7V and 0.9V. The reverse $V_{\text{d2}}$ and $V_{\text{hold2}}$ methods are similar, and will not be further elaborated.

As shown in figure 6a, in the x-coordinate direction, with the increase of the size of the crossbar array, more and more unselected or semi-selected units are opened, and the power consumption of the crossbar array increases. In the y-coordinate direction, the power consumption decreases as the $R_{\text{off}}$ increases. However, the power consumption will not be significantly reduced when the $R_{\text{off}}$ increases to a certain degree. The resistance is sufficient to suppress the leakage current. As the $R_{\text{off}}$ continues to increase, the reading performance will not be further improved.

In addition, as shown in figure 6b, the $R_{\text{off}}$ has little influence on the applied voltage.

Figure 6 Effect of off-state resistance on (a) read power (b) Applied voltage in different array size
As illustrated in figure 7a, read margin greatly decreases with the $R_{\text{on}}$ increasing. The large $R_{\text{on}}$ causes the selector share too much voltage when the 1S1R is turned on. The partial pressure on RRAM is not enough which cause RRAM module cannot set or reset correctly. So the read margin of the overall crossbar array has dropped significantly. In figure 7b, increasing the $R_{\text{on}}$ slightly affect the power consumption. However, the power is known to be driven by OFF-current of half-selected or unselected cells rather than ON-current of the selected one. Under ideal conditions, half-selected or unselected selectors are all in OFF-state, so larger $R_{\text{off}}$ will consumes less power rather than $R_{\text{on}}$. In general, the $R_{\text{on}}$ affects the read margin more, and the $R_{\text{off}}$ affects the read power consumption more.

So the $R_{\text{off}}$ is set to $1E7\,\Omega$ and the $R_{\text{on}}$ is set to $100\,\Omega$.

According to the mathematical formula (1), NL is closely related to operating voltage ($V_{\text{op}}$). In order to reduce the variable parameters for simplicity, in order to simplify the variable parameters, the array size is fixed to 256*256. As shown in figure 8, $V_{\text{op}}$ has little effect on reading margin, but it can be greatly improved by NL because the large NL increases the current difference of the $R_{\text{off}}$ and $R_{\text{on}}$. The reading window is increased, so RM will be significantly improved. The NL also indicates the current-limiting capability of a selector, namely the higher the non-linearity, the stronger the current-limiting capability. However, since the nonlinear of our mathematical model is affected by the $V_{\text{op}}$, and the nonlinear cannot be indefinitely increased according to the actual physical meaning, the nonlinear is set to between $10^4$ and $10^5$.

After the parameter values of 1S1R module are determined, the module is applied to the crossbar
array. The current of all the half-selected and unselected cells is added. As shown in figure 9, compared with 1R crossbar array, the leakage current of 1S1R crossbar array is obviously reduced, and its corresponding power consumption is also greatly reduced.

![Fig. 9 Leakage current in RRAM crossbar array and 1S1R crossbar array](image)

5. CONCLUSION

In this paper, a Verilog-A model of 1S1R is proposed, and the model is applied to the crossbar array to adjust various parameters of the selector through the performance of the crossbar array. It is found that the larger the $V_{th}$ is, the better the writing performance will be, and the smaller the $V_{th}$ is, the better the reading performance will be. Compared with $R_{off}$, $R_{on}$ has a greater influence on read power, and the greater the nonlinear coefficient is, the better the overall performance of crossbar array will be. These performance changes provide the direction for determining parameters and make our model more complete. And it also indicates that our model can be adjusted accordingly for any RRAM model.

ACKNOWLEDGEMENTS

This work was supported by the National Natural Science Foundation of China (Grant No. 61874001), and University Natural Science Research Project of Anhui Province (Grant number KJ2019A0014).

REFERENCES

[1]. R. Waser and M. Aono, Nat. Mater. 6, 833 (2007).
[2]. M.J. Lee, C.B.Lee, D.Lee, S.R.Lee, M.Chang, J.H.Hur, Y.B.Kim, C.J.Kim, D.H.Seo, S. Nat. Mater. 10, 625-630 (2011).
[3]. Z.S. Tang, Y.Q. Chi, L. Fang, R.L. Liu, X. Yi, J. Nanosci. Nanotechnol. 14, 1494-1507 (2014).
[4]. S.Yu, H.Y. Chen, B.Gao, J.Kang, H.S.P. Wong, ACS Nano. 7, 2320-2325 (2013).
[5]. L. Zhang et al, IEEE Electron Device Lett., 35, 199-201 (2014).
[6]. Liping Fu et al. Modern Physics Letters B, 34, 2050115, (2020).
[7]. Y.J.Li et al. Chin. Phys. B, 27, 118502, (2018).
[8]. S.Kim, K.D.Kim, S.I, Choo, Solid-State Electronics 114, 80, (2015).
[9]. L.Q.Zhang et al. IEEE Transactions On Electron Devices 62, 3250, (2015).
[10]. R. Mandapati et al. IEEE Transactions On Nanotechnology 12, 1178 (2013).
[11]. Y.H.Dai, M.Qi, F.Tao, A new one-selector one-resistorVerilog-A model for circuit simulation, 2019 International Conference on Communication, Network and Artificial Intelligence (CNAL), 27-29 December, Guangzhou, China.
[12]. H. Li et al. IEEE Electron Device Letters, 35, 211 (2013).