A Compact Rectifier Design Method Utilizing Harmonics

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Abstract: This paper proposes a compact rectifier design method for utilizing harmonics. Based on total reflection generated by pure reactance loads at the second harmonic (2nd) and open circuit at the third harmonic (3rd), a compact DC-pass filter is designed to effectively utilize the 2nd and 3rd harmonics excited by the rectifying diode. The amplitudes of the harmonics can be controlled by adjusting the input impedances of the DC-pass filter at harmonics. A prototype operating at 5.8 GHz fundamental frequency is implemented and measured to validate the scenario. When the input power is 18.3 dBm, the measured rectifying efficiency is 71.3%, while the 2nd and the 3rd harmonic amplitudes are −2.4 dBm and 0.1 dBm respectively. This method could also be extended to design a rectifier only utilizing the 2nd or the 3rd harmonic.

Keywords: microwave power transmission; rectifier; harmonics utilization; DC-pass filter; rectifying efficiency

1. Introduction

Microwave power transmission (MPT) transmits power from one point to another [1] or to multiple points [2] through free space. MPT technology has become one of the most promising power supply methods for electronic devices, such as mobile terminals [3], wireless sensor networks [4], and drones [5]. In a MPT system, the rectifier, converting the microwave power into the direct-current (DC) power, is a key component. The rectifying diode works in the nonlinear state of large-signal and produces the high-order harmonics. Generally, to lessen the influence of the harmonics and obtain high rectifying efficiency, there are two design methods. One is re-rectifying harmonic for recycling [6,7], another is harmonic controlling by using class-F [8] and class-F$^{-1}$ [9].

In recent years, Guo.et al. proposed to use the 3rd harmonic for antenna beam alignment of the MPT system [10,11]. In [10], a hybrid coupler was suggested to transfer the input power for rectification and utilize the 3rd harmonic to the isolation port for antenna beam alignment. In [11], a ring-shaped coupler directed the 3rd harmonic to the input port and was radiated through a dual-frequency antenna. However, the couplers make the rectifiers complicated and necessitate having large sizes. The separate 2nd harmonic utilization path was employed in [12], but this method also had a large size. The 2nd harmonic is used as the pilot signal for the retrodirective system in [13]. Although the rectifier utilized the 2nd harmonic without extra devices and complicated structure, the rectifying efficiency was only 42.5%.

Based on a specially designed DC-pass filter, this paper presents a compact rectifier design method for utilizing harmonics while maintaining high rectifying efficiency. Table 1 summarizes the comparison between the proposed rectifier and the published literatures. The proposed rectifier design method can utilize the 2nd and the 3rd harmonics simultaneously without an extra coupler or a separate harmonic utilization path, and the rectifying efficiency is above 70%. The amplitudes of the utilized harmonics can be controlled conveniently by designing the DC-pass filter to meet the communication system demand.
Furthermore, the rectifier design method of only utilizing the 2nd or the 3rd harmonic is also analyzed.

### Table 1. Comparison with the prior design methods.

| Ref  | Frequency (GHz) | Input Power (dBm) | Harmonic Type | Harmonic Amplitude (dBm) | Efficiency (%) | Implementation Type | Size (λ₀ × λ₀) | Method          |
|------|-----------------|-------------------|---------------|--------------------------|----------------|---------------------|----------------|-----------------|
| [10] | 2.45            | 6                 | 3rd           | -22                      | 76%            | Microstrip and lumped component | 1.16 × 1.32 | coupler         |
| [11] | 2.45            | 18                | 3rd           | -17.2                    | 70.6%          | Microstrip and lumped component | 1.28 × 1.52 | coupler         |
| [12] | 0.915           | 15                | 2nd           | -2                       | 71%            | Lumped component       | 0.07 × 0.17 | separate harmonic utilization path |
| [13] | 2.45            | 10.7              | 2nd           | -4.1                     | 42.5%          | Microstrip             | N.A.          | N.A.            |
| This work | 5.8            | 18.3              | 2nd and 3rd   | -2.4 and 0.1             | 71.3%          | Microstrip             | 0.69 × 1.38 | DC-pass filter |

λ₀ is the guided wavelength in substrate.

### 2. Design and Simulation

#### 2.1. Principle

The block diagram of the rectifier is shown in Figure 1. It consists of an input impedance matching network, a shunt diode, a DC-pass filter, and a load. The input impedance of the diode \( Z_{in} \) is the parallel connection of \( Z_F \) and \( Z_D \):

\[
Z_{in} = Z_F \parallel Z_D
\]  

(1)

where \( Z_F \) is the input impedance of the DC-pass filter and \( Z_D \) is the diode impedance. The rectifier can utilize different harmonics by designing the \( Z_F \) at the specific harmonics. Table 2 shows the input impedances of the DC-pass filter in different harmonic utilization states.

\[Z_{F,2f_0} = jX \text{ or } +\infty\]  

(3)

\[Z_{F,3f_0} = jX \text{ or } +\infty\]  

(4)

where \( jX \) is pure reactance and \(+\infty\) means open circuit state. The rectifier has two special features. Firstly, the DC-pass filter keeps total reflection at \( f_D, 2f_0, \) and \( 3f_0, \) and only the DC component is transmitted to the load. Secondly, by adjusting the input impedances of the DC-pass filter (\( jX \)) at \( 2f_0 \) and \( 3f_0 \), the amplitudes of the harmonics can be controlled to meet the demand of the communication system.
Table 2. The input impedances of the DC-pass filter in different harmonic utilization states.

| The Type of Harmonic Utilization | $Z_{F, 2f_0}$ (Ω) | $Z_{F, 3f_0}$ (Ω) |
|----------------------------------|-------------------|------------------|
| 2nd and 3rd                     | jX or +∞          | jX or +∞         |
| 2nd                             | jX or +∞          | 0                |
| 3rd                             | 0                 | jX or +∞         |

The impedance matching design of the rectifier includes the input impedance matching network and the DC-pass filter. The former one is to match the input impedance of the diode to 50 Ω at the fundamental frequency. The latter one is to utilize the 2nd and 3rd harmonics simultaneously. By designing the input impedance matching network and the DC-pass filter, the fundamental wave from the source will enter the diode to be rectified, while the 2nd and 3rd harmonics excited by the diode will be utilized towards the source direction. It should be noticed that the harmonics have influence on the rectifying efficiency, so it is necessary to make a trade-off between the rectifying efficiency and the harmonic amplitude in practical application, which means the input impedance of the harmonics are not matched perfectly.

(2) Only utilizing the 2nd or 3rd harmonic: When the input impedances of the DC-pass filter are short circuit at $3f_0$ and pure reactance or open circuit at $f_0$, $2f_0$, the input impedance of the diode will be short circuit at $3f_0$ and the 3rd harmonic will be fully reflected back into the diode for rectifying repetitively. Meanwhile, by designing the input impedance matching network and the DC-pass filter, the input impedance of the diode at $f_0$ can be matched, and the rectifier can utilize the 2nd harmonic. The design method of utilizing the 3rd harmonic is similar to that of the 2nd harmonic. The input impedance of the DC-pass filter should be short circuit at $2f_0$, and pure reactance or open circuit at $f_0$, $3f_0$.

2.2. Simulation

A rectifier is designed to verify the proposed design scenario, which utilizes both the 2nd and the 3rd harmonics simultaneously. The operation fundamental frequency is 5.8 GHz. A Schottky diode MA4E1317 is chosen as the rectifying diode, which has a series resistance $R_s$ of 4 Ω, a zero bias junction capacitance $C_j0$ of 0.02 pF, and a reverse breakdown voltage $V_b$ of 7 V. The material F4B-M with a thickness of 0.8 mm is employed as the printed circuit board (PCB) substrate. The substrate has a relative dielectric constant of 2.65 and a loss tangent of 0.001.

The structure of the proposed rectifier is shown in Figure 2 and is simulated under Advanced Designed System (ADS) software. The π-type stub acts as the input impedance matching network. The π-type stub is used because it has more adjustable variables. The DC-pass filter consists of five open stubs. Stubs $l_5$–$l_9$ correspond to the quarter guided wavelength at fundamental, 2nd, 4th, and 6th harmonic. The length of stub $l_6$ is quarter guided wavelength at fundamental, so the input impedance of stubs $l_6$–$l_{11}$ is short circuit at fundamental and the 3rd harmonic. Since the length of stub $l_5$ is also quarter guided wavelength at fundamental, the input impedance of the DC-pass filter is open circuit at fundamental and the 3rd harmonic. Stub $l_{10}$ functions to adjust the input impedance of the DC-pass filter at the 2nd harmonic. Thus, the input impedance of the DC-pass filter is open circuit at the fundamental and the 3rd harmonic, and $-jZ_c/\tan(4\pi \times l_{10}/\lambda_g)$ at the 2nd harmonic, respectively. $Z_c$ is the characteristic impedance of the microstrip line, and $\lambda_g$ is the guided wavelength of the microstrip line at 5.8 GHz. Figure 3 shows the position of the input impedance of the DC-pass filter on the Smith Chart when the length of stub $l_{10}$ varies from 0 to $\lambda_g/4$. By jointly optimizing the π-type stub and the DC-pass filter, the design goal can be met.
the guided wavelength of the microstrip line at 5.8 GHz. Figure 3 shows the position of the input impedance of the DC-pass filter on the Smith Chart when the length of stub $l_{10}$ varies from 0 to $\lambda_g/4$. By jointly optimizing the $\pi$-type stub and the DC-pass filter, the design goal can be met.

**Figure 2.** The schematic of the rectifier utilizing the 2nd and 3rd harmonic: $l_1 = 4.7$ mm, $l_2 = 4.7$ mm, $l_3 = 4.2$ mm, $l_4 = 8.3$ mm, $l_5 = 9.2$ mm, $l_6 = 9.2$ mm, $l_7 = 4.5$ mm, $l_8 = 2.2$ mm, $l_9 = 1.5$ mm, $l_{10} = 4.8$ mm, $l_{11} = 4.5$ mm, $w_1 = 1.7$ mm, $w_2 = 0.55$ mm, $w_3 = 1.5$ mm, $w_4 = 0.5$ mm, $w_5 = 1$ mm, $w_6 = 1$ mm, $w_7 = 1$ mm, $w_8 = 1$ mm, $w_9 = 1$ mm, $w_{10} = 1$ mm, $w_1 = 1$ mm.

**Figure 3.** For different length of the stub $l_{10}$: the position of the input impedance of the DC-pass filter in the Smith Chart.
Adjusting the length of stub $l_{10}$ can affect the amplitudes of the 2nd and 3rd harmonic simultaneously. Since the harmonics ($2f_0 + f_0 = 3f_0$, $3f_0 - f_0 = 2f_0$) are mixed with the fundamental in the diode, the amplitude of the 2nd harmonic has a tight relationship with that of the 3rd harmonic. By adjusting the input impedance of the DC-pass filter (j$X$) (the length of stub $l_{10}$) at the 2nd harmonic, the amplitude of the 2nd harmonic will change. Meanwhile, the 3rd harmonic is also affected by the amplitude of the 2nd harmonic even if the input impedance of the DC-pass filter maintains open circuit at the 3rd harmonic. Therefore, the amplitudes of the 2nd and 3rd harmonics can be controlled simultaneously by adjusting the length of $l_{10}$.

The harmonic amplitude varying with the length of the stub $l_{10}$ at 18 dBm input power is shown in Figure 4. When the length of the stub $l_{10}$ varies between $0\sim3\lambda/g/20$ (0~5 mm), the amplitude of the 2nd harmonic is lower than that of the 3rd one. The 2nd harmonic is reflected back into the diode and mixed with the fundamental, which might excite the new 3rd harmonic and increases its amplitude. When the length of the stub $l_{10}$ varies between $3\lambda/g/20\sim5\lambda/g/5$ (5~7 mm), the amplitude of the 2nd harmonic is higher. Since the propagation loss of the 3rd harmonic is greater than that of the 2nd one in free space, the 3rd harmonic should be higher than the 2nd one when utilizing both of them simultaneously. Therefore, the length of the stub $l_{10}$ is selected as $2\lambda/g/15$ (4.8 mm), and the input impedance of the DC-pass filter at the 2nd harmonic is $j9$ Ω. In this case, the 2nd and 3rd harmonics amplitudes are $−1.2$ dBm and $1.3$ dBm respectively.

![Figure 4](image-url) Simulated harmonic amplitude with the length of the stub $l_{10}$ at 18 dBm input power.

Figure 5 analyzes the rectifying efficiency and harmonic amplitude of different rectifier at different input power. Figure 5a–c have different circuit layouts and the main difference between them is the input impedances of the DC-pass filter at harmonics. The layouts of them are all realized through π-type stub and the DC-pass filter composed of five open stubs, but their sizes are different to realize different harmonic utilize states. Figure 5d is the convention harmonic suppression rectifier, and the simulation results are described here for comparison with Figure 5a–c.

Figure 5a shows the performances of the rectifier utilizing both the 2nd and 3rd harmonics. When the input power is 18 dBm, the 2nd and 3rd harmonic amplitudes are $−1.2$ dBm and $1.3$ dBm, respectively, and the rectifying efficiency is 72%.
Figure 5. Simulated rectifying efficiency and the harmonic amplitude of different rectifiers at different input powers: (a) the rectifier utilizing both the 2nd and 3rd harmonics; (b) the rectifier utilizing the 2nd harmonic; (c) the rectifier utilizing the 3rd harmonic; (d) the harmonic suppression rectifier.

Figure 5b shows the simulated result of the rectifier utilizing the 2nd harmonic. When the input power is 18 dBm, the 2nd and 3rd harmonic amplitudes are 7.4 dBm and −35 dBm, respectively, and the rectifying efficiency is 71.2%. The 3rd harmonic is almost totally reflected back into the diode, and only the 2nd harmonic is utilized. Figure 5c demonstrates the simulated result of the rectifier utilizing the 3rd harmonic. The 2nd and 3rd harmonic amplitudes are −28.3 dBm and 7.3 dBm, respectively, and the rectifying efficiency is 72%. Figure 5d presents the simulated result of the harmonic suppression rectifier. The 2nd and 3rd harmonic amplitudes are −41 dBm and −31 dBm, respectively, and the highest rectifying efficiency is 77%. The rectifying efficiencies of these four rectifiers are all higher than 70%. The specific circuits can be selected by the demands of the practical applications. Since the amplitude of the fourth harmonic is much smaller than that of the 2nd and 3rd harmonic, the fourth harmonic is not discussed here. The input power of the rectifiers (18 dBm) can be applied for long-distance high-power microwave power transmission systems, such as drones. The proposed design method is still applicable when the diode is selected for medium and low power.

3. Experimental Validation

The proposed rectifier utilizing both the 2nd and 3rd harmonics was fabricated and measured. Figure 6 shows the schematic diagram of the measurement system. The signal source is Keysight E8257D, and the microwave power from the signal source is shunted by a coupler (the coupling degree is 20 dB). One way feeds the rectifier, while another way feeds the power meter to observe the input power of the rectifier. The spectrum analyzer is used to measure the amplitudes of the utilized harmonics.
Harmonic amplitude varying with the input power is shown in Figure 7a. When the input power varies from 10 to 18.3 dBm, the measured amplitude of the 2nd harmonic varies from −10.6 to −2.4 dBm, and the 3rd harmonic varies from −8.3 to 0.1 dBm. Compared with the simulated results, the amplitudes of the 2nd and 3rd harmonics reduce about 1.5 dB and 1.4 dB, respectively. The difference between simulation and measurement may be caused by the errors of the SPICE model, the permittivity, and loss tangents of the substrate at the 2nd and 3rd harmonics.

Figure 6. The schematic diagram of the rectifier efficiency measurement system.

Figure 7. The measured and simulated result of the rectifier utilizing the 2nd and 3rd harmonics: (a) the measured and simulated harmonic amplitude varies with input power; (b) the measured and simulated rectifying efficiency varies with input power; (c) the measured and simulated rectifying efficiency varies with the load; (d) the measured and simulated output voltage varies with input power.
The measured rectifying efficiency is calculated by

\[ \eta = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{V_L^2}{R_L \cdot P_{\text{in}}} \] (5)

where \( R_L \) is the load value, \( V_L \) is the DC output voltage across the load which can be read by a multimeter, and \( P_{\text{in}} \) is the input power of the rectifier.

The measured rectifying efficiency varies with the input power and is shown in Figure 7b. The rectifying efficiency increases as the input power increases. When the input power increases from 10 to 18.3 dBm, the rectifying efficiency is greater than 50% and reaches the highest value of 71.3% at 18.3 dBm. When the input power is greater than 18.3 dBm, the output DC voltage approaches the reverse breakdown voltage of the diode, and the efficiency drops rapidly. Figure 7c shows the measured rectifying efficiency versus the load, and the peak rectifying efficiency is obtained at 350 \( \Omega \). Figure 7d shows the measured output DC voltage at different input power, and the maximum output voltage is about 4.5 V.

4. Conclusions

In this paper, a compact rectifier design method for utilizing harmonics is proposed, analyzed, and verified. By specifically designing the input impedances of the DC-pass filter at harmonics, the rectifier can work in different harmonic utilization states for different application. The rectifier can realize a compact structure and high rectifying efficiency by the proposed design method, which could be applied in mobile terminals, wireless sensor networks, and drones for wireless power supply.

The authors acknowledge the financial support of the National Natural Science Foundation of China under Grant 61931009.

Author Contributions: X.Q. and G.H. conceived and designed the experiments; X.Q. performed the experiments; X.Q. and X.Y. analyzed the data; X.Y. and S.G. contributed reagents/materials/analysis tools; X.Q., G.H. and X.Y. wrote the paper. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by National Natural Science Foundation of China: 61931009.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The data presented in this study are openly available.

Conflicts of Interest: The authors declare no conflict of interest.

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