Random telegraph noise from resonant tunnelling at low temperatures

Zuo Li1, Moïse Sotto1, Fayong Liu1, Muhammad Khaled Husain1, Hiroyuki Yoshimoto2, Yoshitaka Sasago2, Digh Hisamoto2, Isao Tomita3, Yoshishige Tsuchiya3 & Shinichi Saito1

The Random Telegraph Noise (RTN) in an advanced Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is considered to be triggered by just one electron or one hole, and its importance is recognised upon the aggressive scaling. However, the detailed nature of the charge trap remains to be investigated due to the difficulty to find out the exact device, which shows the RTN feature over statistical variations. Here, we show the RTN can be observed from virtually all devices at low temperatures, and provide a methodology to enable a systematic way to identify the bias conditions to observe the RTN. We found that the RTN was observed at the verge of the Coulomb blockade in the stability diagram of a parasitic Single-Hole-Transistor (SHT), and we have successfully identified the locations of the charge traps by measuring the bias dependence of the RTN.

Charge traps in advanced Silicon (Si) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) have been used for many important applications in semiconductor industries. For example, a Metal-Oxide-Nitride-Oxide-Semiconductor (MONOS) memory device has an advantage on a long retention time at high temperatures, which is suitable for an integrated microprocessor in a vehicle. An interface trap is also useful to extend the current plateau in a single electron pump at low temperatures, which is a promising candidate for a redefinition of ampere to establish a new current standard based on an elementary charge in quantum metrology. On the other hand, charge traps also affect reliability problems, such as Random Telegraph Noise (RTN) and Negative Bias Temperature Instabilities (NBTI), causing failures of Static Random Access Memory (SRAM) cells and degradations of long term performance. In particular, the impact of RTN is getting more important with the scaling, since the variations in an atomic level can affect the drain current in sub-20 nm MOSFETs.

RTN is coming from the carrier trapping and de-trapping processes through charge traps at the gate insulator/Si interface, which are intrinsic quantum processes. Quantum effects are not negligible in advanced MOSFETs, since the gate insulator is as thin as 1 nm, and the direct tunnelling currents from the channel into the traps are expected due to enhanced coupling. Previously, the most of the works on RTN were based on measurements at room temperatures, which was difficult to identify the quantum energy levels of charge traps. By measuring the MOSFETs at low temperatures, it is easier to observe various quantum effects.

In our previous study, we have found current peaks at low temperatures in advanced Si MOSFETs, but the mechanism of the peaks was not elucidated. In this study, we characterised the peaks in time domain, and found that the current peaks are related to RTN. The bias conditions to observe the current peaks have been clarified from the stability diagram of the associated with a parasitic Single-Hole-Transistor (SHT) at low temperatures. We also studied the bias dependence of RTN to identify the possible origin of charge traps.

Current Peaks in the Stability Diagram
The device was measured at 2 K, and the fundamental characteristics are shown in the supplementary information. From the stability diagram, open diamonds were observed in the stability diagram of the device, as shown in Fig. 1(a), which implies that several quantum dots in series were responsible for $I_d$ in the subthreshold regime. The quantum dots might be coming from the remote surface roughness coming from Poly-Si grains. At the edge of Coulomb diamonds, we have observed current peaks in the stability diagram, which were previously

1Sustainable Electronics Technologies, Department of Electronics and Computer Science, Faculty of Physical Science and Engineering, University of Southampton, Southampton, UK. 2Research and Development Group, Hitachi, Ltd., 1-280 Higashikoigakubo, Kokubunji, Tokyo, 185-8601, Japan. Correspondence and requests for materials should be addressed to S.S. (email: S.Saito@soton.ac.uk)

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reported in our studies on MOSFETs at low temperatures. The regime where current peaks can be observed formed a border at the edge of Coulomb diamonds. Particularly, the density of current peaks was much higher at some narrow bias conditions. We mark one of them as HT. The extended view of stability diagram in HT regime is shown in Fig. 1(b).

**Quantum Probabilities of the Trap States**

We measured the time domain characteristics of $I_d$ at the bias conditions near the current peaks, and observed RTN. One example of the measurement results, which was measured at $V_g$ of $-640$ mV and $V_d$ of $-13.5$ mV, is shown in Fig. 2(a). Two types of RTN could be identified, which were named as RTN1 and RTN2, as shown in Fig. 2(a). RTN1 has larger amplitude and longer average switching time, while RTN2 has smaller amplitude and shorter average switching time. The long switching time and high amplitude imply that the trap corresponding to RTN1 is a deep oxide trap, while RTN2 might come from the shallow interface trap in the SiON/substrate interface. We could roughly estimate the amplitude of RTN1 by estimating the number of carriers inside the channel. The regime where current peaks can be observed (negative differential conductance) was shown. (Figure 1.) Shows the stability diagram of the MOSFET at 2 K.

From Fig. 3(a), $I_d$ was more likely to be in the high current state if $|V_d|$ was large, and a sharp transition of the preferred $I_d$ state can be observed near $V_g$ of $-640$ mV. This sharp transition showed that the occupancy of the trap, which is revealed from $P_{\text{h}}$ and $P_{\text{l}}$, was modulated by $V_g$. This implies the charge trap corresponding to RTN1 is located in the SiON layer. The high current state was only observable at $V_d$ of $-13$ mV and $-13.5$ mV.

**Nature of the trap**

We will investigate on the probability of finding $I_d$ at the high current State ($P_{\text{h}}$) or the low current state ($P_{\text{l}}$) shown in Fig. 2(b) to identify the nature of the charge trap. The way to extract $P_{\text{h}}$ and $P_{\text{l}}$ is shown in the method. The dependence of $P_{\text{h}}$ and $P_{\text{l}}$ on $V_g$ and $V_d$ are shown in Fig. 3(a) and (b), respectively.

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**Figure 1.** Bias condition to observe current peaks. (a) Shows the stability diagram of the $p$ MOSFET at 2 K. The regime where current peaks can be observed (negative differential conductance) was shown. (b) Shows the extended view of HT region and the bias conditions where RTNs were measured.
accroding to Fig. 3(b), which implies the presence of resonant tunnelling in the channel due to the narrow bias window of $V_d$. The $V_g$ and $V_d$ dependence of RTN1 amplitude were shown in Fig. 3(c) and (d), respectively. We can see that the amplitude of RTN1 almost has no dependence on both $V_g$ and $V_d$. Since the dependence of $I_d$ on $V_g$ is non-linear, as shown in supplementary information, RTN1 is unlikely to have come from the impact of the shift of threshold voltage caused by carrier trapping/de-trapping. Otherwise, if the shift of threshold voltage was constant, the amplitude of RTN1 will have dependence on $V_g$ and $V_d$, which was not what we observed in Fig. 3(c). We could use a similar method to investigate the characteristics of RTN2. The dependence of RTN2 on biases was complex, which implies RTN2 came from a shallow trap near SiON/substrate interface. The dependence of RTN2 on biases is shown in Supplementary information.

The position of the single hole is determined by the wavefunction of single hole in the charge trap. Different positions of the single hole in the charge trap show different impact on the $I_d$. Therefore, the wavefunction of the single hole in this charge trap resulted in an extra noise in $I_d$. In order to understand the wavefunction of the
single hole as shown in Fig. 2(d) and (f), we must study its bias dependence. We will study the noise coming from wavefunction in order to understand its dependence on biases. The differential current, $\Delta I$, is defined as

$$\Delta I = I_d(t + 1) - I_d(t),$$

where $t$ is time with the unit of second. The dependence of its probability distribution on $V_g$ and $V_d$ are shown in Fig. 4(a) and (b), respectively. The standard deviation of $\Delta I$ was extracted by fitting the distribution of $\Delta I$ with the Gaussian distribution function.

The probability distribution of $\Delta I$ had very weak dependence on $V_g$, as shown in Fig. 4(a), while it showed more significant dependence on $V_d$, as shown in Fig. 4(b). Since the change of $I_d$ is similar between Fig. 4(a) and (b), the fact that $\Delta I$ shows more significant dependence on $V_d$ implies that the coupling between the quantum dot and energy level created by charge trap was mainly modulated by $V_d$. We observe that the standard deviation of probability distribution showed a peak value if $V_d$ was at $-13.5$ mV, as shown in Fig. 4(b). This reveals that the wavefunction of the single hole in the channel became the broadest at this bias condition, which implies that the strongest correlation between two energy levels in the channel at this bias condition. This is also in agreement with the assumption of resonant tunnelling. The resonant level is likely to have originated from the charge traps. The Johnson noise of this system was calculated to be $\sim 20$ fA/√Hz and the background noise of the system was $4$ pA in a bandwidth of 5 Hz, which were both much smaller than the noise coming from wavefunction.

**Two Traps RTN**

We could use lag plots to study the correlation behaviour of $I_d$ and the fractal nature of the two charge traps. The lag plot of $I_d$ with the time lag, $\Delta t$, of 1 s, 10 s and 100 s, were shown in Fig. 5(a),(b) and (c). When $\Delta t$ was 1 s, we could observe strong correlation behaviour, as shown in Fig. 5(a). The fractal shape of the lag plot is diagonal, which reveals the strong positive autocorrelation behaviour of $I_d$ in this time scale. When $\Delta t$ was increased to 10 s, the shape of lag plot remained diagonal, but become rectangular within each small area, as shown in Fig. 5(b). This reveals the lost of $I_d$ correlation behaviour regarding RTN2. When $\Delta t$ was further
increased to 100 s, the fractal shape of lag plot became rectangular in both large and small area, as shown in Fig. 5(c). This reveals that the correlation behaviour of $I_d$ almost disappeared in this time scale.

**Discussion**

In the previous sections, we discussed about the characteristics of charge traps. Based on the experimental data, we found that the RTN1 is coming from the opening/closing of a resonant level in the device channel, and the carrier trapping/de-trapping process have originated from the tunnelling process between the Poly-Si gate and charge trap in the SiON layer. The lag plot clearly shows the correlation behaviour and fractal nature of the two charge traps. We also observed the crossover between RTN and 1/f noise, which was previously reported to be observed in magnetic nanodot system\(^4\), as shown in the Supplementary information.

Based on the information shown above, we could establish a physical model to describe the RTN1, as shown in Fig. 6. A schematic 3-D diagram of the device and its physical model is shown in Fig. 6(a). Two quantum dots in series, marked as QD1 and QD2, were responsible for the drain current. The series quantum dots have presum-ably originated from the remote surface roughness caused by Poly-Si grains. We simulated the stability diagram of the series quantum dots system based on the master equations\(^4\),\(^6\),\(^7\), which is explained in detail in method part. The parameters are summarised in the supplementary information. The simulated stability diagram is shown in Fig. 6(b), which is roughly in agreement with the experimental data obtained in Fig. 1(a). The simulation result of stability diagram for individual QD1 and QD2 have been summarised in Supplementary information.

The trap corresponding to RTN1 is located in the SiON layer. Considering the $V_g$ dependence, the charge trapping/de-trapping process has likely originated from the tunnelling of carriers between the poly-Si gate and the trap inside the SiON, as shown in Fig. 6(c). If $|V_g|$ is decreased, the tunnelling barrier between the hole in the poly-Si gate and the energy level in the gate oxide becomes lower, and the trap was easier to be occupied. This corresponds to the trend observed in Fig. 3(a).

The different current states can be explained by the opening/closing of the resonant level\(^4\),\(^8\)–\(^10\) in the channel created by the charge trap. Due to the strong $V_g$ dependence, the resonant level should be close to the drain reservoir. We address the resonant level to be located in the tunnelling barrier between QD2 and the drain reservoir. As a result, the resonant level is strongly coupled with QD2. Due to the relatively much larger distance between the resonant level and QD1, the coupling between the resonant level and QD1 is much weaker than the coupling between the resonant level and QD2, and therefore can be neglected.

**Figure 4.** The dependence of experimental parameters on wavefunction broadening. (a) and (b) Shows the dependence of wave function broadening on $V_g$ and $V_d$, respectively. The $V_g$ and $V_d$ dependence on standard deviation of the corresponding Gaussian wave function, $\sigma$, is shown in subfigures inside (a) and (b), respectively.

**Figure 5.** Fractal nature of the charge traps. The lag plot of $I_d$ with different time lag shows fracture nature of charge traps. (a–c) Shows the correlation behaviour of $I_d$ if time lag was 1 s, 10 s and 100 s, respectively.
A schematic diagram of the potential profile across the channel is shown in Fig. 6(d). If no single hole occupies the charge trap, it was not neutral. Since the Poly-Si gate behaves like a metal, the trap generates mirror charge in the Poly-Si gate. As a result, the trap and the corresponding mirror charge forms an electric dipole. The electric dipole therefore forms a potential well for the single hole in the channel. Under certain bias conditions, the energy level inside this potential well is aligned with the energy level in the QD2. Under that circumstance, resonant tunnelling is observed and the tunnelling barrier between QD2 and drain reservoir is made more transparent. As a result, $I_d$ will increase, therefore we can observe the high current state. If the charge trap is occupied by a single hole, the charge trap will become neutral, and no resonant level will be found in the channel. Under this condition, the tunnelling barrier therefore becomes less transparent, and we can only observe the low current state. This model, which is based on resonant tunnelling, could explain the reason for the narrow $V_g$ and $V_d$ bias condition to observe RTN. Since the resonant level is in the channel, it is therefore more significantly modulated by $V_g$. Besides, the transmission coefficient and wavefunction were mainly influenced by the $V_d$, which explains the fact that the wavefunction was mainly affected by $V_d$, as shown in Fig. 4.
We can estimate the position of charge trap based on the depth of the resonant energy level. From the simplicity point of view, since RTN1 is only observed in the HT regime at the edge of Coulomb diamond, the depth of the potential well, \( \Delta V \), is assumed to be 13.5 mV. We could estimate the distance between trap and Poly-Si/SiON interface, \( d \), from

\[
e\Delta V = \frac{2e^2d}{4\pi\varepsilon_0\varepsilon_{\text{eff}}^2}.
\]

(3)

From Equation (3), we can roughly estimate \( d \) to be \( \sim 0.2 \) nm. This is on the same magnitude with the lattice constant of SiON. This estimation should be correct in magnitude, and is in agreement assuming that the charge trap is located on the top side of SiON. As a result, we think a charge trap located near the Poly-Si/SiON interface, which was presumably a boron ion coming from the ion implantation process, is responsible for the resonant level in the channel.

In conclusion, we successfully demonstrate that we could identify the nature of the trap by measuring the RTN and investigating its bias dependence at low temperatures. We could estimate the position of the trap from the experimental data. Our research demonstrate a way to study the characteristics of charge trap systematically, and will pave the way for scientists to understand the detailed nature of the RTN.

**Methods**

**Sample and experiments.** The device we measured was a standard bulk-Si \( p \)-type MOSFET (\( p \) MOSFET), fabricated by a standard 65nm-node technology. The channel of the \( p \) MOSFET was 10 \( \mu \)m wide and 75 nm long. Wide-channel devices were chosen to increase the chance to find charge traps. The gate was made of highly-doped poly-crystalline silicon (Poly-Si). The gate oxide was made of SiON, with the equivalent oxide thickness of 2.4 nm. The MOSFET was fabricated by a standard 65nm-node technology. The channel of the MOSFET was wire-bonded with Aluminium wire onto a chip carrier. Then the MOSFET was put into a cryostat, with the maximum capability to control temperatures down to 2 K. The MOSFET was measured by a B1500A with high resolution current module. The value of current at each bias was obtained after averaging over \( 10^5 \) sampling taken with the duration of 2 \( \mu \)s for each point. The background noise was less than 4pA, in a bandwidth of 5Hz.

**Data analysis.** The probability to observe high current state and low current state in Figs 2 and 3 are determined by fitting the experimental data with Gaussian distribution functions. The amplitude of RTN is determined by the difference of the peaks. The probability of each state is determined by integrating the corresponding probability distribution function over the current. For example, if the probability distribution function corresponding to the high current state in Fig. 2 is \( P_h(I_d) \), and the probability distribution function corresponding to the low current state in Fig. 2 is \( P_l(I_d) \), then \( P_h \) and \( P_l \) are determined from

\[
P_h = \frac{\int_{-\infty}^{\infty} P_h(I_d)dI_d}{\int_{-\infty}^{\infty} P_h(I_d)dI_d + \int_{-\infty}^{\infty} P_l(I_d)dI_d},
\]

(4)

and

\[
P_l = \frac{\int_{-\infty}^{\infty} P_l(I_d)dI_d}{\int_{-\infty}^{\infty} P_h(I_d)dI_d + \int_{-\infty}^{\infty} P_l(I_d)dI_d},
\]

(5)

which correspond to the shaded areas (magenta and blue, respectively) in Fig. 2(b).

**Simulation of Quantum Dots.** In semiconductor quantum dots, the single particle energy spacing is comparable to the charging energy. Therefore, the Hamiltonian of the system does not simply depend on the charging energy, and the effect of single particle spacing must be considered. In order to simulate the quantum dots in a simple way, we used mesoscopic capacitor model, with different effective coupling capacitances in different hole states, as an approximation.

Assuming the gate capacitance, drain capacitance, and source capacitance when \( n \) holes occupy the quantum dots are \( C_g(n) \), \( C_d(n) \) and \( C_s(n) \) respectively. Considering the circumstance when one less hole occupies the quantum dot, the change in free energy when a hole tunnels out through the electrode drain, \( \Delta F_d^\pm(n) \), or tunnels out through the electrode source, \( \Delta F_s^\pm(n) \), can be expressed as

\[
\Delta F_d^\pm(n) = F_d(n-1) - F_d(n) = -(n-1/2)e^2 - e[C_g(n) + C_d(n)]V_d - C_g(n)V_d^2,
\]

(6)

and

\[
\Delta F_s^\pm(n) = F_s(n-1) - F_s(n) = -(n-1/2)e^2 + e[C_g(n)V_d + C_d(n)V_d^2],
\]

(7)

We could easily obtain the expression of \( \Delta F_d^\pm(n) = F_d(n + 1) - F_d(n) \), and \( \Delta F_s^\pm(n) = F_s(n + 1) - F_s(n) \) from Eqs (6) and (7). Therefore, using Fermi’s golden rule, the tunnelling rate through the drain and source can be expressed as
\[
\Gamma^\pm_0(n) = \frac{1}{R_e e^2} \left[ -\frac{\Delta F^\pm_0(n)}{k_B T} \right]
\]  

and

\[
\Gamma^\pm_s(n) = \frac{1}{R_e e^2} \left[ -\frac{\Delta F^\pm_s(n)}{k_B T} \right]
\]

The master equation can be expressed as

\[
\frac{\partial p(n, t)}{\partial t} = p(n + 1)[\Gamma^+_0(n + 1) + \Gamma^-_0(n + 1)] - p(n)[\Gamma^+_s(n) + \Gamma^-_s(n)].
\]

In the steady state, the probability is not associated with time, so

\[
\frac{\partial p(n, t)}{\partial t} = 0.
\]

The drain current is therefore expressed as

\[
I = e \sum_{n=-\infty}^{n=\infty} p(n)[\Gamma^+_s(n) - \Gamma^-_s(n)].
\]

We solve the equations listed above using extracted parameters to simulate the characteristics of drain current and differential conductance in series quantum dots system. The effect of inversion layer when \(V_g\) is near the threshold voltage is considered in the simulation.

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Author Contributions

H.Y., Y.S., and D.H. fabricated the MOSFET device and discussed results. Z.L., M.S., F.L., M.K.H., I.T., Y.T. and S.S. have contributed for measurements and analysed experimental results.

Additional Information

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