Development of an SDBC-MMCC-Based DSTATCOM for Real-Time Single-Phase Load Compensation in Three-Phase Power Distribution Systems

Wei-Neng Chang 1,* and Ching-Huan Liao 2

1 Department of Electrical Engineering, Chang Gung University, 259 Wen-Hwa 1st Road, Kwei-Shan Dist., Tao-Yuan City 333, Taiwan
2 National Chung-Shan Institute of Science and Technology, 486, 6th Neighborhood, Sec. Jia’an, Zhongzheng Road, Longtan Dist., Tao-Yuan City 325, Taiwan; howardliao05@gmail.com
* Correspondence: nchang@mail.cgu.edu.tw; Tel.: +886-3-211-8800

Received: 31 August 2019; Accepted: 5 December 2019; Published: 10 December 2019

Abstract: This paper proposes a newly developed single-delta bridge-cell, modular multilevel cascade converter (SDBC-MMCC)-based distribution-level static synchronous compensator (DSTATCOM) for single-phase load compensation in three-phase, three-wire electric power distribution systems. Each main circuit arm of the DSTATCOM uses a modular multilevel cascade converter based on full-H-bridge (FHB) cells. The three main DSTATCOM arms are delta-connected to allow phase-independent operations for phase balancing and unity power factor correction of the single-phase load in three-phase, three-wire electric power distribution systems. By using the symmetrical components method, a feedforward compensation algorithm was employed for the DSTATCOM. A simulation of the DSTATCOM was performed for functioning verification. Finally, a hardware test system was built by using a multi-DSP-based control system. The test results verified the effectiveness of the proposed SDBC-MMCC-based DSTATCOM in single-phase load compensation.

Keywords: DSTATCOM; full-H-bridge converter; phase balancing; power factor correction; SDBC-MMCC; single-phase load compensation

1. Introduction

In a three-phase electric power distribution system, a large power capacity of single-phase load (e.g., an electrical railway traction system) absorbs unbalanced (negative-sequence) load current and reactive power. The unbalanced load current produces an unbalanced voltage drop on the electric power distribution line. The resulting unbalanced voltage affects other sensitive loads connected to the distribution system. For example, AC rotary machines will induce extra losses, and rectifier loads will generate ripples in their DC links. Moreover, the unbalanced current will disturb the normal operation of an electric power generator. To keep good power quality, the unbalanced current from the single-phase load should be improved [1,2].

Traditionally, the delta connection of passive inductive/capacitive reactances, also known as a “Steinmetz compensator”, was employed for single-phase load compensations in three-phase power systems [3–5]. The operation principle of the Steinmetz compensator has been used in many applications of unbalanced load compensations [6]. Presently, static var compensators (SVC) are widely used in the load compensations of high-power, single-phase traction systems [7–9]. The thyristor-controlled reactor with fixed capacitor (TCR–FC) type of SVC is applied in these traction systems. A drawback of the TCR–FC type of SVC is that it demands large space for installation. Two-level converters can also...
be used for single-phase load compensations in three-phase power systems \[10–12\]. However, the power ratings of two-level converters are limited.

Recently, static synchronous compensators (STATCOMs) have been introduced as the next-generation shunt compensators \[13–16\]. Compared to traditional SVCs, STATCOMs have quicker response times, more compact structures, wider compensation ranges, and smaller installation space demand. Therefore, distribution-level static synchronous compensators (DSTATCOMs) are highly suitable for unbalanced load compensations in modern three-phase electric power distribution systems. Various types of converters can be employed to construct the main circuit of a DSTATCOM. Due to lower voltage stress and modular structure, single-delta bridge-cell, modular multilevel cascade converters (SDBC-MMCCs) are very suitable for the main circuits of DSTATCOMs in high-voltage and high-power applications \[17–20\]. Hence, the SDBC-MMCC-based DSTATCOMs can replace the SVCs in single-phase load compensations.

In this paper, a new concept of applying an SDBC-MMCC-based DSTATCOM for real-time single-phase load compensation in a three-phase, three-wire power distribution system is proposed. Applications of multilevel full-H-bridge (FHB) converters and staircase modulation in the DSTATCOM main circuit can achieve high-efficiency operation in practical applications. A feedforward compensation algorithm derived from the symmetrical components method was designed for the DSTATCOM, which was constructed using the MATLAB/Simulink program for preliminary verification. Finally, a hardware prototype test system was built using a multi-TMS320F2812 digital signal processor (DSP)-based control system. Experimental results show that the proposed SDBC-MMCC-based DSTATCOM has a rapid response and a satisfactory compensation effect. This paper is a further development of the SDBC-MMCC-based DSTATCOM for three-phase unbalanced load compensation that we previously described \[21\]. In single-phase load compensation, the control algorithm of the DSTACOM is more compact, and the sizing of the DSTATCOM is more precisely defined.

2. DSTATCOM Load Compensation Algorithm

Figure 1 illustrates the study system for deriving the DSTATCOM compensation algorithm. A shunt type of DSTATCOM is installed for the on-site single-phase load compensation. The feedforward compensation algorithm detects the load power parameters, \(P_{ab}^L\) and \(Q_{ab}^L\), and sends three reactive power compensation commands, \(Q_{ab,bc,ca}^{ST}\), to the DSTATCOM’s main circuit arms. The three DSTATCOM arms independently regulate their reactive power inputs, then the synthesized DSTATCOM line current compensates the unbalanced single-phase load current. Consequently, the source currents are balanced with a unity power factor. Using the symmetrical components method, we derived the feedforward compensation algorithm. Figure 2 shows the phase-sequence circuits of Figure 1.

![Figure 1](image-url)  
**Figure 1.** Three-phase, three-wire power distribution system with single-phase load and distribution-level static synchronous compensator (DSTATCOM).
Equation (1) expresses the line voltage of the load bus illustrated in Figure 1, where $V_{ll}$ represents the line voltage. The phase-a load current is shown in Equation (2), in which the relationship of $(V_{ab})^i V_a = p_{ab}^L - jQ_{ab}^L$ is used. The symmetrical components of the load current are then calculated using Equation (3).

$$\bar{V}_{ab} = \bar{V}_{an} - \bar{V}_{bn} = V_{ll} \angle 30^\circ$$  
$$\bar{I}_a = \frac{1}{V_{ll} \angle 30^\circ}(p_{ab}^L - jQ_{ab}^L)$$  
$$\begin{bmatrix} \bar{I}_0 \\ \bar{I}_1 \\ \bar{I}_2 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1a^2 & a & 1 \end{bmatrix} \begin{bmatrix} \bar{I}_a \\ -\bar{I}_a \\ 0 \end{bmatrix}$$  

Equation (3) can be rewritten as rectangular forms, as indicated in Equations (4) and (5). The zero-sequence component of the load current is zero. Equation (6) gives the three arm currents of the DSTATCOM, where the relationship of $V^* \cdot I = P - jQ$ is used. Equation (7) shows the DSTATCOM line currents. Using the symmetrical components transformation in Equation (8), Equation (9) shows the symmetrical components of the DSTATCOM line current in terms of the reactive power flows of the three DSTATCOM arms. For a DSTATCOM with a delta-connected main circuit, the zero-sequence current, $I_{0}^{\text{ST}}$, in Equation (8) is zero.

$$I_1 = \frac{1}{\sqrt{3}V_{ll}^\circ} \left(p_{ab}^L - jQ_{ab}^L\right) = \frac{p_{ab}^L}{\sqrt{3}V_{ll}^\circ} - \frac{jQ_{ab}^L}{\sqrt{3}V_{ll}^\circ}$$  
$$= \text{Re}\left(I_1^1\right) + j\text{Im}\left(I_1^1\right)$$  

$$I_2 = \frac{1}{\sqrt{3}V_{ll}^\circ} \left(\frac{\sqrt{3}}{2}p_{ab}^L + \frac{\sqrt{3}}{2}Q_{ab}^L\right) + j\frac{1}{\sqrt{3}V_{ll}^\circ} \left(\frac{\sqrt{3}}{2}p_{ab}^L - \frac{1}{2}Q_{ab}^L\right)$$  
$$= \text{Re}\left(I_2^2\right) + j\text{Im}\left(I_2^2\right)$$  

$$\begin{bmatrix} I_a^{\text{ST}} \\ I_b^{\text{ST}} \\ I_c^{\text{ST}} \end{bmatrix} = \begin{bmatrix} \bar{I}_a^{\text{ST}} & \bar{I}_b^{\text{ST}} & \bar{I}_c^{\text{ST}} \\ -\bar{I}_b^{\text{ST}} & \bar{I}_c^{\text{ST}} & -\bar{I}_a^{\text{ST}} \\ \bar{I}_c^{\text{ST}} & -\bar{I}_a^{\text{ST}} & \bar{I}_b^{\text{ST}} \end{bmatrix}$$  

$$\begin{bmatrix} I_0^{\text{ST}} \\ I_1^{\text{ST}} \\ I_2^{\text{ST}} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} I_a^{\text{ST}} \\ I_b^{\text{ST}} \\ I_c^{\text{ST}} \end{bmatrix}, \ a = 120^\circ$$  

$$I_1^{\text{ST}} = -\frac{j}{\sqrt{3}V_{ca}^\circ} \left(Q_{ab}^{\text{ST}} + Q_{bc}^{\text{ST}} + Q_{ca}^{\text{ST}}\right)$$  
$$I_2^{\text{ST}} = \frac{1}{\sqrt{3}V_{ll}^\circ} \left(\sqrt{3}Q_{ab}^{\text{ST}} - \sqrt{3}Q_{ca}^{\text{ST}}\right) + j\frac{1}{\sqrt{3}V_{ll}^\circ} \left(-\frac{1}{2}Q_{ab}^{\text{ST}} + Q_{bc}^{\text{ST}} - \frac{1}{2}Q_{ca}^{\text{ST}}\right)$$  

![Figure 2. Phase-sequence circuits of Figure 1.](image-url)
As shown in Figure 2, for the single-phase load compensation, the DSTATCOM should compensate the entire negative-sequence component and imaginary part of the positive-sequence component currents generated by the single-phase load, as revealed in Equation (10) [21,22]. The source current only supplies the real part of the positive-sequence load current. As a result, with the assistance of the DSTATCOM compensation, the source current is balanced with a unity power factor.

\[ I_{1S}^{ST} + \text{Im}\{I_{1c}\} = 0, I_{2S}^{ST} + I_{2c} = 0 \]  
(10)

Finally, combining Equations (4), (5) and (9), (10), we obtained the required load compensation algorithm of each DSTATCOM arm for real-time single-phase load compensation, as indicated by Equation (11). The DSTATCOM is treated as a reactive power load. Hence, much like a traditional SVC, the DSTATCOM can easily compensate the unbalanced load currents generated by the single-phase load, as revealed in Equation (10) [21,22]. The source current consists of an internal voltage source, \( V_{ll} \), modulated by a seven-level, cascade full-H-bridge converter and a commutation reactor, \( X_{ST} \). In this study, each DSTATCOM arm is equivalent to a purely reactive load, which can be inductive or capacitive, is independently controlled by the compensation algorithm in Equation (11). By using power calculation definitions, \( P = (\int_{t} i \cdot v \, dt)/T \) and \( Q = (\int_{t} i \cdot v(\pi/2) \, dt)/T \), in the time domain, Equation (12) shows another version of Equation (11) for the DSTATCOM, where \( T \) is the period of the fundamental frequency. Equation (12) can easily be digitized and implemented in a digital controller. Finally, Equation (13) shows the three-phase source current with DSTATCOM compensation.

\[
\begin{align*}
Q_{ab}^{ST*} &= -Q_{ab}^L \\
Q_{bc}^{ST*} &= -P_{ab}^L/\sqrt{3} \\
Q_{ca}^{ST*} &= P_{ab}^L/\sqrt{3} \\
Q_{abche}^{ST} &= -1/\sqrt{3}T \int_{t} (i_{ab}^c - v_{ab}^c) \, dt \\
Q_{bche}^{ST} &= -1/\sqrt{3}T \int_{t} (i_{bc}^c - v_{bc}^c) \, dt \\
Q_{cahe}^{ST} &= -1/\sqrt{3}T \int_{t} (i_{ca}^c - v_{ca}^c) \, dt
\end{align*}
\]

\[
\begin{bmatrix}
I_{aS}^l \\
I_{bS}^l \\
I_{cS}^l
\end{bmatrix}
= \begin{bmatrix}
1 & 1 & 1 \\
1 & a^2 & a \\
1 & a & a^2
\end{bmatrix}
\begin{bmatrix}
I_{aS}^0 \\
I_{bS}^1 \\
I_{cS}^1
\end{bmatrix}
= \begin{bmatrix}
1 & 1 & 1 \\
1 & a^2 & a \\
1 & a & a^2
\end{bmatrix}
\begin{bmatrix}
0 & \sqrt{3}V_{ll}^L/\phi_0^l \\
P_{ab}^L/\sqrt{3}V_{ll}^L\phi_{-120}^l \\
P_{ab}^L/\sqrt{3}V_{ll}^L\phi_{120}^l
\end{bmatrix}
\]

3. DSTATCOM Main Circuit

Figure 3 shows a three-phase power distribution system, a single-phase load, and the proposed seven-level, SDBC-MMCC-based DSTATCOM as the test system in the paper. Each STATCOM arm consists of an internal voltage source, \( V_{ST} \), modulated by a seven-level, cascade full-H-bridge converter and a commutation reactor, \( X_{ST} \). In this study, each DSTATCOM arm is equivalent to a purely reactive power load.

The reactive power flows of these three DSTATCOM arms are regulated independently for the single-phase load compensation. The power inputs of each DSTATCOM arm in Figure 3 are expressed in Equations (14) and (15), respectively. An indirect phasor-domain power angle regulation method is used for the reactive power control in the DSTATCOM. For a reactive power demand, the DSTATCOM controller regulates the power angle, \( \delta_{ST} \), to absorb or release the active power from the power source according to Equation (14). The active power flow charges or discharges the DC-link capacitors and then regulates the DC-link voltages. Finally, the cascaded DC-link voltages synthesize the internal voltage, \( V_{ST} \), then the DSTATCOM absorbs capacitive or inductive reactive power according to Equation (15). When the reactive power response is completed, the power angle returns to near-zero values. With the delta-connected main circuit, the three DSTATCOM arms achieve phase-independent operation. Hence, much like a traditional SVC, the DSTATCOM can easily compensate the unbalanced load current and correct the power factor caused by a single-phase load.
A typical staircase modulation scheme, depicted in Figure 4, enables the DSTATCOM main circuit to operate with high efficiency. Each level and internal voltage waveform of the DSTATCOM arm \( a-b \) in Figure 3 are also shown [21]. The internal voltage \( v^{ST} \) shows a staircase waveform. The three switching angles, \( \theta_1-\theta_3 \), should be determined to minimize the harmonics generated. The internal voltage \( v^{ST} \) in Figure 4 can be represented as a Fourier series, as detailed in Equation (16), where \( n \) is the harmonic order (\( n = 1, 3, 5, 7, \ldots \)). Ideally, the harmonic order contains only odd-order components. Equation (17) shows the harmonic components in Equation (16).

\[
p^{ST} = \frac{V^{ST}V^L}{X^{ST}} \sin \delta^{ST} \tag{14}
\]

\[
Q^{ST} = \frac{V^L(V^L - V^{ST} \cos \delta^{ST})}{X^{ST}} \tag{15}
\]

\[
v^{ST}(\omega t) = \frac{4V^{dc}}{\pi} \sum_n \left[ \cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3) \right] \frac{\sin(n \delta_{ab})}{n} \theta_1 < \theta_2 < \theta_3 < 90^\circ, n = 1, 3, 5, 7, \ldots \tag{16}
\]

\[
H(n) = \frac{4V^{dc}}{n\pi} \left[ \cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3) \right] \tag{17}
\]
In Equation (17), setting $n = 1$ produces the fundamental component $H(1)$, which consists of the DC-link voltage $V_{dc}$ and three switching angles, $\theta_1 - \theta_3$. The fundamental component $H(1)$ is used for the reactive power regulation. To eliminate the specified harmonic orders, a harmonic-minimizing method is used [23]. Assigning $H(1) = 3V_{dc}$ for the fundamental-component modulation and setting $H(5) = H(7) = 0$ for the 5th and 7th orders’ harmonic cancellation produces Equation (18). Subsequently, solving Equation (18) results in the required switching angles, namely, $\theta_1 = 11.68^\circ$, $\theta_2 = 31.18^\circ$, $\theta_3 = 58.58^\circ$.

$$\begin{align*}
\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) &= 3\pi/4 \\
\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) &= 0 \\
\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) &= 0
\end{align*}$$

(18)

Figure 5 depicts the functional block diagram of the DSTATCOM controller proposed in this paper. As noted, the control algorithm using Equation (11) calculates the required reactive power values for Equation (11) and the reactive power inputs of the three DSTATCOM arms in real time. The DSTATCOM controller in Figure 5 requires a fast power detection scheme. Figure 6 schematizes the fast calculation method of active and reactive powers that applies control compensation in real time. The DSTATCOM controller in Figure 5 completes the single-phase load compensation independently, as shown in Equation (19). The three output commands of the PID controllers, $\delta_{ST_{ab}}, \delta_{ST_{bc}}, \delta_{ST_{ca}}$ generate the gating signals, as shown in Figure 4 for these switching elements in the three DSTATCOM arms. With the proposed controller shown in Figure 5, the DSTATCOM completes the single-phase load compensation in real time. The DSTATCOM controller in Figure 5 requires a fast power detection method. Figure 6 schematizes the fast calculation method of active and reactive powers that applies the single-phase $\alpha - \beta$ reference axis method. Applying this fast calculation results in the load power values for Equation (11) and the reactive power inputs of the three DSTATCOM arms in real time.

$$\delta_{ST_{ab,bc,ca}} = K_p \Delta Q_{ST_{ab,bc,ca}} + K_i \int \Delta Q_{ST_{ab,bc,ca}} dt + K_d \frac{d}{dt} \Delta Q_{ST_{ab,bc,ca}}$$

(19)
4. Simulation Verification

Figure 7 shows the simulation system, which was developed in the MATLAB/Simulink program for a preliminary verification of the proposed DSTATCOM. A single-phase inductive load was used in the testing. First, the DSTATCOM main circuit was built according to Figure 3. In the simulation, the switch (SW) in Figure 7 was closed at \( t = 0.605 \) s to make a step response caused by the single-phase load. With the setting, the transient and steady-state performances of the DSTATCOM compensation were observed from the simulation results. Appendix A lists the system parameters.

Figures 8 and 9 are the simulation results. Figure 8a shows the transient load current response. With the assistance of the DSTATCOM, the three-phase source current was corrected to be balanced with a unity power factor, as shown in Figure 8b. Figure 8c depicts the synthesized line current of the DSTATCOM.

Figures 9a–e reveal other DSTATCOM responses in the single-phase load compensation for reference. When the single-phase load was switched in, the three DSTATCOM arms changed to phase-independent operation, as shown in Figure 9a,b. Figure 9c–e reveal other DSTATCOM responses in the single-phase load compensation for reference.

The simulation results in Figures 8 and 9 clearly indicate that the proposed DSTATCOM discussed in this paper is suitable for single-phase load compensation. It is also observed that the unbalanced operation of the three DSTATCOM arms produce high-order harmonic currents. The harmonic currents tend to flow into the system and aggravate the electric power quality. An adequate front-end filter can be installed to lessen the harmonic current pollution. Increasing the cascade numbers of the FHB cells in the DSTATCOM main circuit can markedly reduce the high-order harmonic currents.
Figure 8. DSTATCOM compensation response. (a) Three-phase load current ($i_{L_a}$); (b) Three-phase source current ($i_{S_b}$); (c) Line current of DSTATCOM ($i_{ST_c}$); (d) Power ($P_{ST_a}$, $Q_{ST_a}$) to the single-phase load; (e) Power ($P_{3o}$, $Q_{3o}$) from the source.

Figure 10 shows the steady-state power flow with the DSTATCOM compensation. It can be observed that the DSTATCOM offers a path to rearrange the power flow for single-phase load compensation.
The simulation results in Figures 8 and 9 clearly indicate that the proposed DSTATCOM discussed in this paper is suitable for single-phase load compensation. It is also observed that the unbalanced operation of the three DSTATCOM arms produce high-order harmonic currents. The harmonic currents tend to flow into the system and aggravate the electric power quality. An adequate front-end filter can be installed to lessen the harmonic current pollution. Increasing the cascade numbers of the FHB cells in the DSTATCOM main circuit can markedly reduce the high-order harmonic currents.

Figure 10 shows the steady-state power flow with the DSTATCOM compensation. It can be observed that the DSTATCOM offers a path to rearrange the power flow for single-phase load compensation.

---

### Table 1: Power Flow Data

| Time (s) | \( P_{\text{L}} \) (kW) | \( Q_{\text{L}} \) (kVar) |
|---------|----------------|----------------|
| 0.58    | 0.0            | -0.5           |
| 0.6     | 0.0            | -0.6           |
| 0.62    | 0.0            | -1.0           |
| 0.64    | 0.0            | 0.5            |
| 0.66    | 0.0            | 1.0            |
| 0.68    | 0.0            | 0.5            |
| 0.70    | 0.0            | -0.5           |

---

**Figure 8.** DSTATCOM compensation response. (a) Three-phase load current \( i_{\text{abc}} \); (b) Three-phase source current \( i_{\text{Sabc}} \); (c) Line current of DSTATCOM \( i_{\text{STabc}} \); (d) Power \( P_{\phi}, Q_{\phi} \) to the single-phase load; (e) Power \( P_{\phi}^3, Q_{\phi}^3 \) from the source.

---

**Figure 9.** DSTATCOM compensation response. (a) Internal voltage \( v_{\text{STabc}} \); (b) Current \( i_{\text{STabc}} \); (c) Compensation command \( Q_{\phi}^*, \phi \); (d) Power angle command \( \delta_{\phi}^* \); (e) DC-link voltages of full-H-bridge (FHB) cells.
5. Hardware Experimental Results

Figure 11 shows the hardware prototype test system constructed in the laboratory, and Appendix B lists the system parameters used. A single-phase load was used for verification testing in the physical experiment. The SDBC-MMCC-based DSTATCOM main circuit had a seven-level, transformerless configuration with a delta connection. In the hardware implementation of the DSTATCOM main circuit, insulated-gate bipolar transistors (IGBTs) were used. The DSTATCOM controller was a multi-TMS320F2812 DSP-based system with a sampling time of 0.52 ms to digitize the three PID controllers in Figure 5. The control program in the multi-DSP-based controller was first developed in C language on a host PC. The execution file was downloaded to the multi-DSP-based controller through Joint Test Action Group (JTAG) data links. Two multi-channel digital scopes were employed to record the transient responses of the DSTATCOM. During the DSTATCOM operation, some selected on-line calculation results in the controller were sent to the host PC for further evaluation.

Figure 11. Functional block diagram of the DSTATCOM hardware prototype test system.
Figures 12 and 13 reveal the hardware experimental results. Figure 12 shows the current responses with DSTATCOM compensation. In Figure 12a, the switching-in of the single-phase load created an unbalanced operation. The single-phase load operation requires active power with a lagging power factor. Figure 12b illustrates the source current response; the phase-a-to-ground voltage waveform was recorded at the same time for reference. With the real-time compensation of the DSTATCOM, the source current was corrected very quickly to be balanced with a unity power factor. Figure 12c shows the transient response of the synthesized DSTATCOM line current in the compensation. Table 1 records the steady-state DSTATCOM compensation result in Figure 12. The transient compensation result in the hardware test.

\[
I_{UR} = \frac{\max(|I_a - I_{avg}|, |I_b - I_{avg}|, |I_c - I_{avg}|)}{I_{avg}} \times 100\% \quad (20)
\]

Figure 12. Transient responses with DSTATCOM compensation. (a) Single-phase load current (\(I_{a,b,c}^L\)); (b) Source current (\(I_{a,b,c}^S\)); (c) DSTATCOM line current (\(I_{a,b,c}^{ST}\)).

Table 1. DSTATCOM compensation result in the hardware test.

|        | \(I_{a,b,c}^L\) | \(I_{a,b,c}^S\) | \(I_{a,b,c}^{ST}\) | \(I_{UR}^L (%)\) | \(I_{UR}^S (%)\) |
|--------|----------------|----------------|-----------------|----------------|----------------|
| Load   | 6.46           | 6.43           | 0               | 100%           | 3.26%          |
| Source | 4.1            | 3.85           | 4.0             | 3.26%          | 3.26%          |
DSTATCOM line currents, as shown in Figures 13b,c. However, high-order harmonic currents were 
unavoidably generated in the three DSTATCOM arms.

The hardware experimental results verified that the proposed SDBC-MMCC-based DSTATCOM 
is suitable for real-time phase balancing and power factor correction of single-phase loads in three-
phase, three-wire power distribution systems.

Figure 13. Transient responses of the DSTATCOM. (a) Internal voltage ($v_{ST\,ab\,bc\,ca}$); (b) Arm current ($i_{ST\,ab\,bc\,ca}$); (c) Arm a-b voltage and current ($v_{ST\,ab\,} \cdot i_{ST\,ab}$); (d) Compensation command ($Q_{ST\,ab\,bc\,ca}$); (e) DC-link voltages ($V_{dc\,ab\,1,2,3}$, $V_{dc\,bc1,2,3}$, $V_{dc\,ca1,2,3}$).

Figure 13 shows other responses in the DSTATCOM main circuit. The three DSTATCOM arms 
changed to phase-independent operation when the single-phase load was switched in. The physical 
test results agreed with the simulation results presented in Figure 9. The transient compensation
response of the DSTATCOM was quite fast. The delta-connected DSTATCOM main circuit and the harmonics-minimizing method eliminated the specified harmonic components in the synthesized DSTATCOM line currents, as shown in Figure 13b,c. However, high-order harmonic currents were unavoidably generated in the three DSTATCOM arms.

The hardware experimental results verified that the proposed SDBC-MMCC-based DSTATCOM is suitable for real-time phase balancing and power factor correction of single-phase loads in three-phase, three-wire power distribution systems.

6. Conclusion

In a three-phase, three-wire electric power distribution system, a newly designed SDBC-MMCC-based DSTATCOM employing staircase modulation and an indirect phasor-domain power angle regulation method for real-time single-phase load compensation was studied. An effective feedforward compensation algorithm was proposed for the DSTATCOM. The computer simulation results showed that the function of the proposed DSTATCOM was quite satisfactory. Finally, a hardware test system was built for functional verification. The proposed DSTATCOM showed a fast transient response and a satisfactory steady-state compensation effect. However, the simulation and experimental results also revealed that unbalanced operation of the DSTATCOM induced unbalanced harmonic currents in the three DSTATCOM arms. Thus, in practical applications, harmonic filters should be installed to enhance the electric power quality. Increasing the cascade numbers of the FHB cells in each DSTATCOM main circuit arm can also reduce undesired harmonic currents.

Author Contributions: W.-N.C. conceived this paper and composed the study system; C.-H.L. conducted the theoretical study, computer simulation, and hardware implementation; all authors wrote the paper.

Funding: The financial support from the Ministry of Science and Technology (MOST), Taiwan, is acknowledged.

Acknowledgments: Valuable comments and discussions from the reviewers are appreciated.

Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

General:
\[ P \] active power
\[ Q \] reactive power
\[ v \] instantaneous voltage
\[ i \] instantaneous current
\[ \delta \] power angle
\[ V \] voltage phasor
\[ I \] current phasor
\[ C \] dc-link capacitor
\[ X \] reactance
\[ \text{Re} \] real part
\[ \text{Im} \] imaginary part

Superscripts:
\[ S \] power source
\[ L \] load
\[ ll \] line to line
\[ ST \] DSTATCOM
\[ ST^* \] DSTATCOM command
\[ dc \] dc link
\[ * \] complex conjugate

Subscripts:
\[ 3\phi \] three-phase
\[ 1\phi \] single-phase
\[ 0, 1, 2 \] Zero, positive, negative sequences
Appendix A. Simulation System Parameters

System side:

\[ V_{fl}^S = 110V, f_s = 60Hz, X_{\alpha,\beta} = 0.1\Omega, Z_{ab}^l = 15 + j5.655\Omega \]

DSTATCOM side:

\[ C_{ab,1,2,3} = C_{bc,1,2,3} = C_{ca,1,2,3} = 3,300\mu F, X_{ST,ab,\beta,ca}^S = 3.77\Omega, \theta_1 = 11.68^\circ, \theta_2 = 31.18^\circ, \theta_3 = 58.58^\circ, K_p = 1.0, K_i = 0.65, K_D = 0.0007 \]

Appendix B. Experimental System Parameters

System side:

\[ V_{fl}^S = 110V, f_s = 60Hz, X_{\alpha,\beta} = 0.1\Omega, Z_{ab}^l = 15 + j5.655\Omega \]

DSTATCOM side:

\[ C_{ab,1,2,3} = C_{bc,1,2,3} = C_{ca,1,2,3} = 3,300\mu F, X_{ST,ab,\beta,ca}^S = 3.77\Omega, \theta_1 = 11.68^\circ, \theta_2 = 31.18^\circ, \theta_3 = 58.58^\circ, K_p = 0.8, K_i = 0.65, K_D = 0.0007 \]

References

1. Grünbaum, R.; Hasler, J.P.; Thorvaldsson, B. FACTS: Powerful means for dynamic load balancing and voltage support of AC traction feeders. In Proceedings of the 2001 IEEE Porto Power Tech Conference, Porto, Portugal, 10–13 September 2001; pp. 1–6.
2. Dugan, R.C.; McGranaghan, M.F.; Santos, S.; Beaty, H.W. Electrical Power Systems Quality; McGraw-Hill: New York, NY, USA, 2002.
3. Todeschini, G.; Emanuel, A.E.; Ferrero, A.; Morando, A.P. A poynting vector approach to the study of the Steinmetz compensator. IEEE Trans. Power Deliv. 2007, 22, 1830–1833. [CrossRef]
4. Sainz, L.; Pedra, J.; Caro, M. Steinmetz circuit influence on the electric system harmonic response. IEEE Trans. Power Deliv. 2005, 20, 1143–1150. [CrossRef]
5. Sainz, L.; Monjo, I.; Riera, S.; Pedra, J. Study of the Steinmetz circuit influence on AC traction system resonance. IEEE Trans. Power Deliv. 2012, 27, 2295–2303. [CrossRef]
6. Miller, T.J.E. Reactive Power Control in Electric System; Wiley & Sons: New York, NY, USA, 1982.
7. Grünbaum, R. FACTS for dynamic load balancing and voltage support in rail traction. In Proceedings of the IEEE 2007 European Conference on Power Electronics and Applications, Aalborg, Denmark, 2–5 September 2007; pp. 1–6.
8. Grünbaum, R. SVC for the channel tunnel rail link: Providing flexibility and power quality in rail traction. In Proceedings of the IEE Seminar on Power—It’s a Quality Thing, London, UK, 16 February 2005.
9. Wang, H.; Liu, Y.; Yan, K.; Fu, Y.S.; Zhang, C.H. Analysis of static var compensators installed in different positions in electric railways. IET Electr. Syst. Transp. 2015, 5, 129–134. [CrossRef]
10. Singh, B.; Sharma, S. Stand-alone single-phase power generation employing a three-phase isolated asynchronous generator. IEEE Trans. Ind. Appl. 2012, 48, 2414–2423. [CrossRef]
11. Ladoux, P.; Raimondo, G.; Caron, H.; Marino, P. Chopper-controlled Steinmetz circuit for voltage balancing in railway substations. IEEE Power Electron. 2013, 28, 5813–5822. [CrossRef]
12. Wu, J.C.; Wang, Y.H. Three-phase to single-phase power-conversion system. IEEE Trans. Power Electron. 2011, 26, 453–461. [CrossRef]
13. Gultekin, B.; Gercek, C.O.; Atalik, T.; Deniz, M.; Bicer, N.; Ermis, M.; Kose, K.N.; Ermis, C.; Koc, E.; Cadirci, I.; et al. Design and implementation of a 154 kV, ±50 MVar transmission STATCOM based on 21-level cascaded multilevel converter. IEEE Trans. Ind. Appl. 2012, 48, 1030–1045. [CrossRef]
14. Milanovic, J.V.; Zhang, Y. Modeling of FACTS devices for voltage sag mitigation studies in large power systems. IEEE Trans. Power Deliv. 2010, 25, 3044–3052. [CrossRef]
15. Peng, F.Z.; Wei, Q.; Dong, C. Recent advances in multilevel converter/inverter topologies and applications. In Proceedings of the IPEC conference, Sapporo, Japan, 21–24 June 2010; pp. 492–501.
16. Ghosh, A.; Ledwich, G. Power Quality Enhancement Using Custom Power Devices; Kulwer Academic Publishers: London, UK, 2002.
17. Akagi, H. Classification, terminology, and application of the modular multilevel cascade converter (MMCC). *IEEE Trans. Power Electron.* 2011, 26, 3119–3130. [CrossRef]

18. Peng, F.Z.; Wang, J. A universal STATCOM with delta-connected cascade multilevel inverter. In Proceedings of the Power Electronics Specialists Conference, Aachen, Germany, 20–25 June 2004; pp. 3529–3533.

19. Hagiwara, M.; Maeda, R.; Akagi, H. Negative-sequence reactive-power control by a PWM STATCOM based on a modular multilevel cascade converter (MMCC-SDBC). *IEEE Trans. Ind. Appl.* 2012, 48, 720–729. [CrossRef]

20. Wu, P.H.; Chen, H.C.; Chang, Y.T.; Cheng, P.T. Delta-connected cascaded H-bridge converter application in unbalanced load compensation. *IEEE Trans. Ind. Appl.* 2017, 53, 1254–1262. [CrossRef]

21. Chang, W.N.; Liao, C.H. Design and Implementation of a STATCOM based on a multilevel FHB converter with delta-connected configuration for unbalanced load compensation. *Energies* 2017, 10, 921. [CrossRef]

22. Lee, S.Y.; Wu, C.J.; Chang, W.N. A compact algorithm for three-phase three-wire system reactive power compensation and load balancing. In Proceedings of the 1995 International Conference on Energy Management and Power Delivery EMPD’95, 21–23 November 1995; pp. 63–70.

23. Liu, Y.; Hong, H.; Huang, A.Q. Real-time calculation of switching angles minimizing THD for multilevel inverters with step modulation. *IEEE Trans. Ind. Electron.* 2009, 56, 285–293. [CrossRef]