A Low-Voltage Hybrid CMOS-Memristor-Based Wideband Class-AB Amplifier for Portable Electronic Device Applications

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This paper presents a low-voltage high-gain wideband three-stage true-class-AB amplifier. This is realized in the 0.18 μm CMOS process. The three-stage class-AB amplifier is proposed based on a compensation topology called nested Miller compensation along with a memristor to get pole-zero cancellation, which arises beyond the unity gain frequency. The circuit is implemented without the need for extra components as transistors, resistors, and capacitors, thus saving the complexity of the circuit and power consumption. The circuit is designed to operate with a supply voltage of ±1 V along with a bias current of 175 μA. The simulation results indicate that this proposed amplifier is capable of driving wide range of resistive and capacitive loads, furthermore capable of maintaining a phase margin of more than 60°. The total compensation capacitor is 2 pF, which is much lesser as compared to pseudo- and true-class AB amplifier, which implies a reduction in area. Simulation results show that the unity gain frequency of the proposed class-AB amplifier is 136.7 MHz, which is much higher as compared to the counterpart topologies. The major advantage associated with this work is a very high bandwidth attained without affecting the gain of the amplifier.

1. Introduction

Recently, the real bottleneck for analog circuits is to make them operate at reduced supply voltage; at the same time, it is desired that there should not be any degradation in its performance. The modern-day mixed-signal chip is a very unfriendly environment for analog circuits such as operational amplifiers, where the power supply is very often corrupted. This directly results in the performance degradation of the circuit which fails the chip. Hence, it is high time to develop low-voltage analog circuits to attain sufficient gain, bandwidth, and stability at lower technology nodes. It is evident that class AB amplifiers are low-voltage compatible, and our work aims to further enhance the low-voltage compatibilities of class AB amplifiers. Class AB operational amplifiers [1–6] with high slew rate, low-power dissipation, and as they can cause output current ample greater than the whole bias current in the output point, make them most suitable for portable electronic devices such as audio amplifiers, light emitting diodes, motor drivers, and liquid crystal display drivers [7].

As the channel length of the MOSFET goes on decreasing, consequently, there is a fall in supply voltage, which aid in to decrease in the gain of the single-stage amplifier. Hence, the finest technique to increase the gain is to employ cascading amplifiers in which the overall gain will be the product of the gain of every stage. But as we go on increasing the number of stages, stability becomes the major issue. To
overcome these stability issues, advanced compensation techniques are used such as Ahuja compensation, nested Miller compensation [8], and reverse nested Miller compensation [9].

This paper is structured as follows. Analysis and design of the pseudo- and true-class-AB amplifier along with its advantages and disadvantages are presented in Section 2. The theory of memristor is presented in Section 3. The
proposed circuit along with its compensation technique and stability analysis is presented in Section 4. Simulation results along with a comparison study with the proposed class-AB amplifier are presented in Section 5. Finally, in Section 6, our work is concluded.

2. Three-Stage Pseudo- and True-Class-AB Amplifier

Figure 1 shows the schematic of the pseudoclass AB amplifier [10]. The first stage of the circuit is essentially a simple differential amplifier, followed by two common source amplifiers. The first common source amplifier which is formed by (M6 and M7) provides negative gain, whereas the second common source amplifier made by (M8 and M11) provides positive gain. There is a feed-forward path from V1 to transistor M10, which is responsible for establishing the push-pull action in the amplifier. The last stage comprises an NMOS designed by transistors M9 and M11. For instance, the increase in input voltage V_{in+} results in the rise in the current of the transistors M1 and M2 consequences of the fall of the voltage at node V1. Consequently, the current at transistors M6 and M10 increases; as the transistor M2 can sink the bias current, the voltage at node V2 rises. The PMOS transistor M10 forms a feed-forward path beginning node V1 toward the output. So, as the V_{in+} rises, the amplifier supplies an enormous source current to the load. On the other hand, if V_{in-} rises, then the voltage at node V1 is augmented, and the voltage at node V2 falls for the occurrence of inverting common source amplifier. The rise in voltage of transistors M6 and M11 results in the rise of sinking current, through the output of the transistor M9. As a result of which, the quiescent current rises with the rise in the output sinking current causing of loss.
in the current efficiency and power. Hence, the amplifier is named as pseudoclass-AB amplifier.

It is important to note that the maximum sinking current is restricted by supply voltage, whereas the source current is independent of the supply voltage.

The compensation scheme used in the pseudoclass AB amplifier is reverse nested Miller compensation. Later that is in Figure 2, a gate to drain feedback resistor is employed between the second-stage amplifier [11], which in turn cancels out the gain of the first common source amplifier and aids in stirring the pole at the gate terminal of the second-stage common source amplifier to a higher frequency.

3. Theory of Memristor

A memristor is a passive circuit element that is used to control and restore the amount of current that has flowed through it in terms of accumulation of charge. Memristors have several distinct characteristics unlike some other elements, such as the ability to rebuild their prior value without the usage of electricity. Relied on the electric charge going across the circuit, the memristance value alters. The resistivity of the two-terminal component gets impacted by factors such as the duration, amplitude, and direction of the applied voltage. The memristor emits dynamic negative resistance by memorizing its last resistance value generated when the power is turned off until the voltage is switched on again. A new modern solid-state memory was born which operates solely on the change of resistance state yielding nonvolatility and creating an opportunity for the realization of innovative circuits. The primary advantages of memristor include nonvolatility, energy efficiency, CMOS compatibility, and fast switching speed. Memristor finds its application ranging from nonvolatile memory to neuro-morphic computing as it covers both digital and analog domains [12].

The memristor for circuit analysis can be defined mathematically as:

\[ v = R(w)i, \]  \hspace{1cm} (1)

\[ \frac{dw}{dt} = f(w, i), \]  \hspace{1cm} (2)

where \( w \) is the state variable of the device and \( R \) is generalized resistance. \( R \) and \( f \) are the explicit functions of time. The entire resistance of the memristor is recognized by the two variable resistors connected in series, where the resistances are assumed for the complete length of the device. The total voltage across the memristor can be computed as

\[ V(t) = \left( \frac{R_{on} w(t)}{D} + R_{off} \left( 1 - \frac{w(t)}{D} \right) \right) i(t). \]  \hspace{1cm} (3)

Here, some conventions are made: ohmic conductance, ions drift linearly in a uniform field, and average mobility of ions is \( \mu_v \).

\[ \frac{dw(t)}{dt} = \mu_v \left( \frac{R_{on}}{D} \right) i(t). \]  \hspace{1cm} (4)

Then, \( w(t) \) can be expressed as

\[ w(t) = \mu_v \left( \frac{R_{on}}{D} \right) q(t). \]  \hspace{1cm} (5)

By inserting Equation (5) in Equation (3), the memristance of the device can be expressed as

\[ m(q) = R_{off} \left( 1 - \frac{\mu_v R_{on}}{D^2} q(t) \right). \]  \hspace{1cm} (6)
A memristor is a three-dimensional stacked composition. It consists of a TiO$_2$ layer arranged in between the bottom and top electrodes, namely, Pt and Au which are characterized as oxygen ion blocking electrodes. In addition, the Titania switching layer is divided into two categories: one is stoichiometric TiO$_2$ and another one is the nonstoichiometric TiO$_2$ as shown in Figure 3. A concentration gradient is formed due to the deficiency in the oxygen vacancies. As an impact of positive bias, there is a momentum of oxygen ions to the nonstoichiometric Titania region from the stoichiometric Titania region, and in the switching layer, the oxygen vacancies will spread rapidly over a broad region, allowing the conductance of the memristor to enhance, causing the device to SET at a lower resistance. The inversion of the bias potential results in the oxygen ions returning to the stoichiometric region, causing the device to be RESET at higher resistance.

4. Proposed Class-AB Amplifier

Figure 4 represents the schematic of the proposed three-stage true-class-AB amplifier. The first block is made up of an NMOS differential pair (M$_1$-M$_2$) with a current mirror load (M$_3$-M$_4$). (M$_8$-M$_9$ and M$_{10}$-M$_{11}$) are all taken together to act as a single noninverting stage. Finally, the output stage is designed by an inverting common source amplifier (M$_{12}$ and M$_{13}$). The feed-forward stage is made up of a PMOS device M$_{13}$ acting as an active load for the last stage. It is the basic feature of the class AB amplifier that all the internal transistors have low quiescent current, but the output stage has huge sourcing and sinking ability. When there is an increase in voltage $V_{in+}$, the current through the transistor M$_1$ and M$_2$ rises, resulting in a fall in voltage at node $V_1$. As a result, the current through the transistors M$_8$ and M$_{12}$ increases. Since M$_9$ can sink only the bias current, there is a rise in voltage at node $V_2$ but the current at node M$_{10}$ is limited to their respective bias currents. So, the voltage at node $V_2$ to fall in voltage at node $V_1$. The transistors are limited to their respective transconductance. The voltage at the output causes the amplifier to deliver source current as $V_{in-}$ rises. On the other hand, if $V_{in-}$ is increased, it makes the transistor M$_{12}$ off.

4.1. Nested Miller Compensation. The suggested construction, depicted in Figure 5, is discussed in detail since the RHP zero diminishes the bandwidth of the NMC amplifier and devalues its stability. The feed forwarded transconductance stage ($g_{mp}$) is employed to eradicate the feed-forward small amount of current through $C_{c1}$ at the high frequency range and to enhance the amplifier’s optimum output transconductance. It should be recognized that under this topology, $g_{mp}$ is designed to be higher than $g_{m3}$. Furthermore, as with the 2-stage Miller compensating amplifier, a nulling resistor ($R_m$) is required to negate the RHP zero.

The third stage, together with the feed-forward stage, comprises a push-pull output stage. If extra control circuitry is installed, the output stage can be converted to a class-AB type. Here, $g_{m3}$ can be considered equivalent to $g_{m3}$ to double the GBW because of the reason that the quiescent currents of the PMOS, as well as NMOS are the similar. The size of the PMOS is tripled to account for the fluctuation of the mobility carriers. $C_{c3}$, which regulates the GBW, could be lowered to acquire a bigger GBW, if a PM less than that of 60 degrees is not essential in some situations.

4.2. Stability Analysis. The small signal equivalent of the modified class-AB amplifier is shown in Figure 6. The first stage is having transconductance of $g_{m1}$ and the second stage which is a combination of two inverting amplifiers is having transconductance $g_{m2}$, and the third stage is $g_{m3}$. The feed-forward path is having transconductance $g_{mf}$. The corresponding impedance concerning ground at the respective nodes $V_1$, $V_2$, and the output node $V_{out}$ is $R_i/C_1$, $R_f/C_2$, and $R_{out}/C_{out}$, respectively. The overall gain of the proposed class-AB amplifier is approximately the product of their respective individual gains of the corresponding stages and is given by

$$A_V = g_{m1}R_{o1}g_{m2}R_{o2}g_{m3}R_{o3},$$

Figure 7: Pole/zero location of the proposed circuit (not to scale).
Figure 8: Simulated (a) magnitude and (b) phase plot of the proposed three-stage true-class-AB amplifier, driving 25 pF//1 kΩ, 100 pF//10 kΩ, and 200 pF//1 MΩ.
The stability of nested Miller compensation with feedforward transconductance and a nulling resistor amplifier is insensitive towards the variation in the circuit parameters as the stability depends on the ratio of transconductance and capacitor.

5. Simulation Results

Figure 7 shows the different pole and zero locations of the proposed circuit. From the pole/zero values in Hz (i.e., poles locations are $-4.575 \times 10^4$, $-1.540 \times 10^7$, $-1.742 \times 10^8$, and $-9.125 \times 10^8$, and zero location is $-2.01 \times 10^7$), these values were obtained during the simulation process from the Cadence® software with Virtuoso tool using 180 nm CMOS technology. The proposed circuit contains four left hand part poles and one left hand part zeros. Table 1 summarizes the poles and zeros values. The zeros located at higher frequencies are not taken into consideration due to their negligible effect on stability.

The effectiveness of the proposed class-AB amplifier is realized by employing nested Miller compensation, and it is found to be comparable with its counterparts when it is simulated using a 0.18 $\mu$m CMOS process. It is even observed that the amplifier consistently provides a phase margin greater than 60°, for a wide range of loads, which is a parallel combination of resistor $(500 \Omega - 1 M \Omega)$ and capacitor $(1-200 pF)$. The amplifier is made to drive various loads of $200 pF//1 M \Omega$, $100 pF//10 K \Omega$, and $25 pF//1 K \Omega$ as shown in Figure 8, then its gain and phase margin are inferred.

Table 2 gives the summary of the ac simulation carried out for three amplifiers driving a load of 25 pF//1 KΩ.

6. Conclusion

A simple compensation technique, i.e., nested Miller compensation, along with a memristor, have been presented in this work. The proposed class-AB amplifier operates with a low supply and simple bias circuit. The proposed class-AB amplifier was simulated in a 0.18 $\mu$m CMOS process, and simulation results were comparable with true and pseudoclass AB amplifier in accordance to phase margin, common-mode rejection ratio, gain and slew rate, unit gain frequency, and third harmonic distortion. The proposed circuit, if implemented physically in portable devices, would have definitely strive the hunger in terms of area and power as compared to its counterpart.

Table 2: Performance comparison of amplifiers in Figures 1–3. Driving a load of 25 pF//1 KΩ.

| Technology            | Pseudoclass-AB | True-class-AB | Proposed true-class-AB |
|-----------------------|---------------|---------------|------------------------|
| $R_{OUT}$             | $500 \Omega - 1 M \Omega$ | $500 \Omega - 1 M \Omega$ | $500 \Omega - 1 M \Omega$ |
| $C_{OUT}$             | 1 pF-200 pF   | 1 pF-200 pF   | 1 pF-200 pF            |
| DC gain (dB)          | 67.3          | 63.4          | 70.5                   |
| Unit gain frequency (MHz) | 2.6           | 4.9           | 136.7                  |
| Phase margin (deg)    | 99            | 83            | 69.2                   |
| Gain margin (dB)      | 30            | 15            | 7                      |
| CMRR @ DC (dB)        | 71            | 80            | 83                     |
| THD (dB)              | -45.7         | -47.1         | $-15 \text{dB} @ V_{out} = 1.6 \text{Vpp}$ |
| Slew rate (V/μs)      | 1.3           | 2.7           | 175                    |

The data used to support the findings of this study are included within the article.

Conflicts of Interest

The authors declare that there is no conflict of interest regarding the publication of this article.

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