Special Topic: Topological Insulators

Topological insulating phase in commonly used semiconductors

Kai Chang

Interface polarization between commonly used semiconductors provides a possible method to drive commonly used semiconductors into their topological insulating phase.

Topological insulators (TIs) have attracted interest over recent years, with properties such as an insulating bulk region, robust metallic edges or surface modes and topological excitations. They have potential applications ranging from spintronic devices to quantum computation [1–8]. Despite recent progress, topological insulating materials are still limited by the narrow band gaps of the materials that contain heavy atoms, such as HgTe [4, 5], Bi\textsubscript{2}X\textsubscript{3} (X = Se, Te, ...) [6–9]. However, these materials are very different from conventional semiconductors in both their structures and properties, and are difficult to integrate into current electronic devices that are based on well-developed semiconductor fabrication technologies.

Although the quantum spin Hall effect is predicted to occur in graphene [3], the main obstacle in its occurrence is the weak intrinsic spin–orbit interactions (SOIs) of carbon atoms. Instead of searching for new TI materials with exotic structures and chemical elements, another route is to drive commonly used semiconductors into their TI states using intrinsic electric fields and strain. This approach is difficult because most of the commonly used semiconductors, such as Si, Ge and GaAs, possess sizable band gaps and do not have strong enough SOIs.

Commonly used semiconductors, such as Si, Ge and GaAs, possess sizable band gaps ranging from 0.8 to 1.4 eV. Thus, a large electric field is required to close the band gap and invert the conduction and valence bands. Such a large electric field cannot be generated by utilizing the gate technique. Recent technical advances in atomic-scale synthesis have made it possible to fabricate high-quality semiconductor heterostructures. Recently, a new method to explore the topological insulating phase in semiconductors that utilizes the strong piezoelectric effect at a GaN/InN interface has been proposed [10]. The strain between these materials resulted in a large polarization and electric field across the interface. This large electric field not only inverted the conduction and valence bands, but also generated a strong Rashba SOI, eventually driving the system into its topological insulating phase. However, a strong strain (~10%) in this system induced defects, vacancies and dislocations in the samples. The density of these defects rapidly increased as the thickness of the InN layers increased, making the sample growth and fabrication challenging. To overcome this obstacle, the realization of TIs in commonly used lattice-matched semiconductors is required.

Commonly used semiconductors, such as Si, Ge and GaAs, possess sizable band gaps ranging from 0.8 to 1.4 eV. Thus, a large electric field is required to close the band gap and invert the conduction and valence bands. Such a large electric field cannot be generated by utilizing the gate technique. Recent technical advances in atomic-scale synthesis have made it possible to fabricate high-quality semiconductor heterostructures. Recently, a new method to explore the topological insulating phase in semiconductors that utilizes the strong piezoelectric effect at a GaN/InN interface has been proposed [10]. The strain between these materials resulted in a large polarization and electric field across the interface. This large electric field not only inverted the conduction and valence bands, but also generated a strong Rashba SOI, eventually driving the system into its topological insulating phase. However, a strong strain (~10%) in this system induced defects, vacancies and dislocations in the samples. The density of these defects rapidly increased as the thickness of the InN layers increased, making the sample growth and fabrication challenging. To overcome this obstacle, the realization of TIs in commonly used lattice-matched semiconductors is required.

A schematic diagram of the proposed semiconductor quantum well (QW) structure is shown in Fig. 1a with its atomic configuration, which was grown along the (1 1 1) polar direction. The lattice constants for the GaAs and Ge materials were 5.655 Å and 5.657 Å, respectively. This lattice match made it possible to grow GaAs/Ge/GaAs QWs coherently. A large electric field was induced in the Ge layer. In the GaAs/Ge/GaAs QW, one of the
interfaces consisted of As–Ge bonds and the other consisted of Ga–Ge bonds. Each As atom contains five electrons, whereas each Ga atom contains only three electrons. Thus, the charges were transferred from the As–Ge side to the Ga–Ge side of the interface, and an electric field was created and exerted on the Ge layer. The electric field shifted the electron and hole states to the left and right sides of the QW and reduced the difference in their energies (band gap), eventually inverting their order. In addition, the electric field also induced a considerably large Rashba SOI. When the Ge film was thicker than four monolayers, the Ge layer was driven into its topological insulating phase [11].

Both Ge and GaAs are important materials for microelectronic and optoelectronic device applications. Recently, Ge/GaAs heterostructures formed by epitaxy have paved the way to heterostructure-based devices that make use of band gap offsets, quantum size effects and band structure modifications with electric fields. Ge/GaAs quantum structures have promise to dramatically increase the mobility required for power saving electronics [12]. Ge/GaAs interfaces with exceedingly small lattice mismatches have many advantages over strained interfaces. The Ge layers grown on GaAs substrates have been studied previously because of their widespread applications in solar cells, metal–oxide–semiconductor field-effect transistors, millimeter-wave mixer diodes, temperature sensors, and photodetectors.

Ge is a well-known indirect band gap semiconductor with a valence band maximum (VBM) at the \( \Gamma \) point and a conduction band minimum (CBM) at the \( L \) point. While growing a heterojunction along the \( (1 1 1) \) direction, the symmetry was broken and the bands were folded along the \( \Gamma – L \) direction (see Fig. 1b). As a result, the CBM at the \( L \) points in the bulk Ge was folded to the \( \Gamma \) point and the Ge thin layers that were grown in the \( (1 1 1) \) direction had a direct gap at \( \Gamma \). This nontrivial band folding led to a strong coupling between the electron and the hole states, which is essential for the TI transition.

The driving force to decrease the band gap was the strong electric field, imposed by the charges located at the two interfaces in the GaAs/Ge/GaAs QW (see Fig. 1c). The strength of the electric field decreased with an increasing thickness of the Ge layer, because of the charge transfer from the Ga–Ge interface to the As–Ge interface, which weakened the driving force toward band inversion. A slight tensile strain also helped to drive the system into band inversion. This slight tensile strain was realized by either doping through introducing In atoms into the GaAs host material, bending the sample, or by growing the heterostructures on substrates with larger lattices. The compressive and tensile strains provided us with an effective way to control the TI transition. The TI transition was shown by the existence of the helical edge states (see Fig. 1d).

SOIs are essential for the transition to a topological insulating phase. The intrinsic SOIs in both Ge and GaAs were not strong enough to create TI states. The large electric field at the interface induced a considerably large Rashba SOI splitting of the electron and hole states (\( \sim 2–15 \) meV). A Rashba SOI of this magnitude usually occurs only in systems containing heavier atoms.

The presence of the TI state in ultrathin Ge layers has potential to advance the application of this new quantum state in existing electronic and optoelectronic devices. GaAs/Ge/GaAs structures are ready to be integrated with conventional semiconductors that are extensively used in electronic devices [12].

ACKNOWLEDGEMENTS

This work was supported by a National Natural Science Foundation of China (NSFC) grant no. 10934007 and grant no. 2011CB922204 from the Ministry of Science and Technology (MoST) of China.

Kai Chang
SKLSM, Institute of Semiconductors, Chinese Academy of Sciences, China
E-mail: kchang@semi.ac.cn

REFERENCES

1. Hasan, MZ and Kane, CL. Rev Mod Phys 2010; 82: 3045–67.
2. Qi, XL and Zhang, SC. Rev Mod Phys 2011; 83: 1057–110.
3. Kane, CL and Mele, EJ. Phys Rev Lett 2005; 95: 146802.
4. Bernevig, BA, Hughes, TL and Zhang, SC. Science 2006; 314: 1757–61.
5. Konig, M., Wiedmann, S and Br"{u}ne, C et al. Science 2007; 318. 766–70.
6. Fu, L, Kane, CL and Mele, EJ. Phys Rev Lett 2007; 98: 106803.
7. Hsieh, D., Qian, D and Wray, L et al. Nature 2008; 452: 970–4.
8. Xia, Y., Qian, D and Hsieh, D et al. Nature Phys 2009; 5: 398–402.
9. Chen, YL., Analysis, JG and Chu, JH et al. Science 2009; 325: 178–81.
10. Miao, MS, Yan, Q, Van de Walle, CG, Lou, WK, Li, LL and Chang, K. Phys Rev Lett 2012; 109: 186803.
11. Zhang, D, Lou, WK, Miao, MS, Zhang, SC and Chang, K. Phys Rev Lett 2013; 111: 156402.
12. Pillarisetty, R. Nature 2011; 479: 324–8.