Effects of Memristors on Fully Differential Transimpedance Amplifier Performance

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Abstract—The progress of the Internet of Things (IoT) technologies and applications requires the efficient low power circuits and architectures to maintain and improve the performance of the increasingly growing data processing systems. Memristive circuits and substitution of energy-consuming devices with memristors is a promising solution to reduce on-chip area and power dissipation of the architectures. In this paper, we proposed a CMOS-memristive fully differential transimpedance amplifier and assess the impact of memristors on the amplifier performance. The fully differential amplifiers were simulated using 180nm CMOS technology and have 5.3-23MHz bandwidths and 2.3-5.7kΩ transimpedance gains with a 1pF load. We compare the memristor based amplifier with conventional architecture. The gain, frequency response, linear range, power consumption, area, total harmonic distortion and performance variations with temperature are reported.

Index Terms—transimpedance amplifier, fully differential, memristor, IoT, 180nm CMOS.

I. INTRODUCTION

Communication between various devices is the principal idea of the IoT [1], [2] and the progress of transceivers plays a major role in the IoT development [1], [3], [4]. Amplifier is a fundamental element in any analog circuit for IoT applications, and a majority of transceivers include transimpedance amplifiers (TIA) [3], [5], [6], [7], [8]. IoT systems require low power devices and circuits with small on-chip area, and ability to tolerate temperature variations [1], [9], [10]. There are several research works attempting to fulfill these requirements in TIAs [11], [12], [13], [14]. However, the energy efficient amplifiers that can be used for large scale IoT applications is still an open problem [2].

In this paper, we proposed the energy efficient memristor-based TIA design that can be used for large scale IoT architectures. The use of memristors in various architectures has proven the to be efficient for the reduction of on-chip area and power consumption, comparing to the conventional CMOS-based designs [1], [2], [10], [15]. This paper compares the conventional TIA design shown in [5] and proposed CMOS-memristive modification, where one resistor, two CMOS transistors are replaced by memristors.

The rest of the paper is organized as follows. In Section II, mathematical analysis is conducted to find the expected value of the transimpedance gain in first and second designs. In Section III, gains, frequency responses, linear ranges, power consumptions, total harmonic distortions and performance variations with temperature are reported for all four designs. Section IV discusses differences between the presented designs and Section V concludes the paper.

II. PROPOSED DESIGN AND GAIN CALCULATION

The schematics of fully differential TIA is presented in Fig. 1 [5]. We propose to replace resistor R1, and transistors M6 and M9 with memristors, which allows to reduce the on-chip area and power dissipation, and does not deteriorate the functionality of the circuit.

In this amplifier, current $I_G$ is represented by Eq. 1 where $r_{ds13}$ is the drain to source resistance of transistor M13 and $V_O$, which is the gate voltage of M2, equals to $V_{dd} - I_G R_1$. 

$$I_G = \frac{V_{dd}}{R_1 + r_{ds13}}$$

The drain current of M2 is represented by $I_O$, which is replicated by current mirror built by M9-M12. The two other current mirrors, M13-M14 and M15-M16, replicate $I_G$, which is added to $I_O$ and is a drain current of M1. In case of M3 and M4, input currents $I_{in+}$ and $I_{in-}$ are added to $I_O$ respectively.

For correct operation transistors M1-M4 operate in active region, shown by Eq.2-5, where transistors M1-M4 have the same geometrical parameters and are all NMOS transistors, and $V_{ds}$ is the same to ensure the ideal matching condition.

$$I_{D1} = I_O + I_G = \mu N C_{ox} \frac{W}{L} V_{ds} (V_{dd} - V_T - \frac{n_N}{2} V_{ds})$$

$$I_{D2} = I_O = \mu N C_{ox} \frac{W}{L} V_{ds} (V_O - V_T - \frac{n_N}{2} V_{ds})$$

$$I_{D3} = I_O + I_{in+} = \mu N C_{ox} \frac{W}{L} V_{ds} (V_{out+} - V_T - \frac{n_N}{2} V_{ds})$$

$$I_{D4} = I_O + I_{in-} = \mu N C_{ox} \frac{W}{L} V_{ds} (V_{out-} - V_T - \frac{n_N}{2} V_{ds})$$

Equation 6 is a result of subtracting Eq.3 from Eq.4.

$$I_{in+} = \mu N C_{ox} \frac{W}{L} V_{ds} (V_{out+} - V_O) \quad (6)$$

Equation 7 is obtained by subtracting Eq.3 from Eq.2.

$$I_G = \mu N C_{ox} \frac{W}{L} V_{ds} (V_{dd} - V_O) \quad (7)$$

Equation 8 is obtained by subtracting Eq.2 from Eq.1.
Equation 8 is derived by dividing Eq.6 by Eq.7, and similar for Eq.9.

\[
\frac{I_{in}}{I_G} = \frac{V_{out} - V_O}{V_{dd} - V_O} \quad (8)
\]

\[
\frac{I_{in}^-}{I_G} = \frac{V_{out}^- - V_O}{V_{dd} - V_O} \quad (9)
\]

Eq.10 can be obtained by rearranging Eq.8-9, where \( I_G \) and \( R_1 \) is determined by Eq.11.

\[
V_{out}^+ - V_{out}^- = V_{dd} - V_O \left( I_{in}^+ - I_{in}^- \right) \quad (10)
\]

\[
R_1 = \frac{V_{out}^+ - V_{out}^-}{I_{in}^+ - I_{in}^-} = \frac{V_{out}}{I_{in}} \quad (11)
\]

In our design, we replace R1, M6 and M9 by memristors, and the analysis from Eq.11 is useful to determine \( R_{off} \) (Eq.12).

\[
R_{off} = R_1 = \frac{V_{out}^+ - V_{out}^-}{I_{in}^+ - I_{in}^-} = \frac{V_{out}}{I_{in}} \quad (12)
\]

As memristors are programmed to have OFF state resistance \( R_{off} \) equal to 10kΩ, the substitution of M6 and M9 does not have effect on the above calculations.

### III. SIMULATION RESULTS

The simulations are performed using 180nm CMOS model for transistors and HP memristor [16]. We simulated four different designs. In the first design, we simulate the original circuit proposed in [5] for 180nm CMOS technology with \( V_{DD} = 1.8V \). The sizes of the transistors are shown in Table I. Fig. 2 shows that the range of inputs for which the amplifier has a constant gain (linear range) is from -140µA to 60µA for both \( I_{in}^+ \) and \( I_{in}^- \). Fig. 3 shows that the system has a 6MHz bandwidth and has a constant gain of 5.2kΩ throughout the passband. Fig. 4 shows their variation with temperature. Fig. 5 shows the total harmonic distortion for 1MHz sinusoidal input currents from 0 to 70µA. TIA has 1mV offset in output. The power dissipation is 1396µW. The on-chip area of this design is 2541µm².

In the second design, memristors U1, U2 and U3 are substituted for R1, M6 and M9, respectively. The design with memristors is shown in Fig. 6. Memristors are programmed to operate in OFF state, where their resistance is equal to 10kΩ. Lengths and widths of transistors were kept the same as in [5] and are summarized in Table I. Fig. 7 shows that the linear range of this design has been shortened and is now from -15µA to 80µA. Fig. 8 shows that the system has a constant gain of 5.7kΩ and a 5.3MHz bandwidth. Fig. 9 shows that in comparison with the first design, gain variation with temperature is considerably smaller. Fig. 10 shows the total harmonic distortion with respect to input current. One can notice that this design has a linear increase THD in contrast to exponential one in the case of the first design. The output offset is 0mV. Power dissipation has been decreased to 1154µW. This design occupies 2182.4µm². This reduction of area was possible...
due to substitution of resistor R1 and transistors M6 and M9 by memristors, where the latter are assumed to have 45nm×90nm dimensions [17].

The third design is without memristors but has length and width of each transistor decreased by the factor of 5, which is summarized in Table II. As can be seen in Fig. 11 the linear range of this design has been increased; it is now from -270µA to 180µA for both inputs. Fig. 12 shows that the system has a constant gain of 2.3kΩ and a 23MHz bandwidth. Fig. 13 shows their variation with temperature. From Fig. 14 it can be seen that THD of this design is considerably smaller than in previous designs. However, changes in geometric parameters have introduced a significant offset of 73mV in the output. Furthermore, the power dissipation has heavily grown to 2316µW. On the other hand, shortening of transistors’ widths and lengths allowed a drastic decrease of the on-chip area from 2541µm² in the first design to 203.1µm².

The fourth design is the third design with memristors U1-U3 substituted instead of R1, M6 and M9. Fig. 15 shows that the linear range is from -15µA to 150µA for both inputs. From Fig. 16 the gain is 3.6kΩ and the bandwidth is 11.3MHz. Fig. 17 proves that gain variation with temperature
is smaller in designs with memristors. Fig. 18 shows that total harmonic distortion of this design is higher than in the third one, but it grows at a lower pace. The substitution of memristors has completely removed the output offset. In addition, it decreased the power dissipation to 1177 $\mu W$.

Moreover, the on-chip area has been further reduced to 169.6 $\mu m^2$.

**IV. DISCUSSION**

Due to their small on-chip area and low power dissipation, memristors reduce the on-chip area and power dissipation.

Table II summarizes main performance characteristics of all four designs.

Gains of all four designs significantly diverge from the theoretical value of $10k\Omega$. Considerable impact to this mismatch is from unequal drain to source voltage drop in transistors M1-M4. It was assumed that these drops would be the same, but simulation results show that they were different. From the simulation results one can notice that application of memristors in the circuit has positive effects on gain, output offset and power dissipation. The total harmonic distortion is higher for lower input currents but it does not grow as much with increasing input as in the designs without memristors.

However, frequency response analysis shows that bandwidth decreases when the memristors are introduced in the design. Temperature variation analysis shows that in all cases bandwidth alterations are insignificant and gain deviations are considerably smaller in the memristor based design.
Fig. 11. Output voltage $V_{OUT}$ versus input current $I_{IN}$. Modified geometric parameters, transistor only case

Fig. 12. Frequency response. Modified geometric parameters, transistor only case

Fig. 13. Gain variation with temperature. Modified geometric parameters, transistor only case

Fig. 14. Total Harmonic Distortion (THD) over $I_{IN}$. Modified geometric parameters, transistor only case

Fig. 15. Output voltage $V_{OUT}$ versus input current $I_{IN}$. Modified geometric parameters, memristors added case

Fig. 16. Frequency response. Modified geometric parameters, memristors added case
TABLE III
Performance characteristics

| Design                                                                 | Linear range | Gain | Bandwidth | Power | Area    |
|----------------------------------------------------------------------|--------------|------|-----------|-------|---------|
| Original circuit [5] with 180nm CMOS transistors                     | -140μA to 60μA | 5.2KΩ | 6MHz      | 1390μW | 2514μm² |
| Memristor-based design with replaced R1, M6 and M9                   | -15μA to 80μA  | 5.7KΩ | 3.5MHz    | 1154μW | 2182.4μm² |
| Original design with decreased transistor size                       | -270μA to 180μA | 2.3KΩ | 23MHz     | 2316μW | 203.1μm² |
| Memristor-based design with decreases transistor size                | -15μA to 150μA  | 3.6KΩ | 11.3MHz   | 1177μW | 1154μm²  |

![Fig. 17. Gain variation with temperature. Modified geometric parameters, memristors added case](image1)

![Fig. 18. Total Harmonic Distortion (THD) over I_{IN}. Modified geometric parameters, memristors added case](image2)

V. CONCLUSION

Four designs which are based on [5] were compared and contrasted in terms of gain, frequency response, linear range, power consumption, area, total harmonic distortion and performance variations with temperature. To conclude, if fully differential feature is not required, designs with memristors give many advantages over the designs without them.

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