Influence of substrate-induced thermal stress on the superconducting properties of V$_3$Si thin films

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Thin films of superconducting V$_3$Si were prepared by means of RF sputtering from a compound V$_3$Si target at room temperature onto sapphire and oxide-coated silicon wafers, followed by rapid thermal processing under secondary vacuum. The superconducting properties of the films thus produced are found to improve with annealing temperature, which is ascribed to a reduction of defects in the polycrystalline layer. Critical temperatures ($T_c$) up to 15.3 K were demonstrated after thermal processing, compared to less than 1 K after deposition. The $T_c$ was found to always be lower on the silicon wafers, by an average 1.9(3) K for the annealed samples. This difference, as well as a broadening of the superconducting transitions, is nearly independent of the annealing conditions. In-situ XRD measurements reveal that the silicide layer becomes strained upon heating due to a mismatch between the thermal expansion of the substrate and that of V$_3$Si. Taking into account the volume reduction due to crystallization, this mismatch is initially larger on sapphire, though stress relaxation allows the silicide layer to be in a relatively unstrained state after cooling. On oxidized silicon however, no clear evidence of relaxation upon cooling is observed, and the V$_3$Si ends up with an out-of-plane strain of 0.3% at room temperature. This strain increases as the sample is cooled down to cryogenic temperatures, though the deformation of the polycrystalline layer is expected to be highly inhomogeneous. Taking into account also the reported occurrence of a Martensitic transition just above the critical temperature, this extrapolated strain distribution is found to closely match an existing model of the strain dependence of A-15 superconducting compounds.

I. INTRODUCTION

Self-aligned silicides have long been the technology of choice for contacting CMOS transistors, as they offer low specific resistance, a reliable process, and often a silicidation-tunable Schottky barrier height. Though recent efforts have focused mainly on nickel and nickel-platinum silicides, numerous other transition metals have been studied for this application, each often presenting its own advantages.

As the downscaling progressed and requirements shifted, these specific advantages have often meant that material preferences shifted, most recently as Ni(Pt)Si superseded CoSi$_2$. Now, with the end of Moore’s law in sight and interest in beyond-CMOS technologies rising, such demands may shift once more. One area of investigation is superconducting computing, which offers lower power requirements for large-scale operation and, most prominently, provides a platform for quantum computing. The central element of such technologies is the Josephson junction, traditionally made by joining two superconductors with an insulating barrier, across which superconducting carriers can tunnel. Because transport through such insulators cannot be modulated by applying a voltage, gates typically rely on tuning the interference between two nearby junctions with magnetic fields. Such magnetic tuning has the disadvantages that the fields from nearby gates may affect each other, and that it effectively doubles the number of junctions that need to be patterned. A different approach returns to the mature CMOS process, drawing on existing designs and fabrication expertise to create Josephson field effect transistors (JoFETs). In such devices, superconducting silicides offer high-quality contacts to a semiconducting channel, allowing the superconducting transport to be tuned by a gate voltage.

In addition to most of the usual material properties desired of silicides for regular transistors, superconducting behavior is now of central importance.

Not all silicides are superconducting, and those that are have widely different critical temperatures ($T_c$’s) at which superconductivity appears. PtSi and CoSi$_2$ for example, which are relatively mature in terms of integration, offer values of around 1.0 and 1.4 K, whereas the less developed V$_3$Si can be superconducting up to 17 K. A high $T_c$ is desirable as it relaxes the cryogenic requirements for operation, but it also directly relates to the strength with which superconducting electrons bind to each other. This can be quantified by the energy gap $\Delta$ (not to be confused with the semiconducting band gap), which in general relates to the critical temperature through $\Delta = k_B T_c$. To illustrate, while PtSi has a superconducting band gap of 70–150 meV depending on the film thickness, that of V$_3$Si is in the range of 2.2–2.8 meV. A higher critical temperature therefore means that the electron pairs are harder to break apart as they traverse the semiconducting channel, and coherent transport between the contacts is easier to establish. It also implies a shorter coherence length, around 7 nm for V$_3$Si, making the superconducting behavior near an interface more sensitive to the quality of the surface, and thus imposing more stringent requirements on the fabrication.

Besides the critical temperature, other properties such as the Schottky barrier height to silicon, mismatches with the channel in effective mass and lattice parameter, and the ability to reliably form high-quality films are important in selecting a silicide for Josephson field effect transistors.

Though V$_3$Si offers the highest known critical temperature of any silicide that the authors are aware of, relatively little is known about its integration into CMOS devices. Motivated by
this scarcity in the literature, we aim to understand the formation of thin films and their behavior at cryogenic temperatures. The focus in this study is the apparent influence of the substrate on the superconducting properties of the thin film, which seems not to be related to the qualities of the film itself. Analysis of changes in the out-of-plane lattice parameter induced during and after thermal processing suggests that the residual strain is substrate-dependent, and strongly affects the critical temperature.

II. V₃Si DEPOSITION AND THERMAL PROCESSING

Among vanadium silicides predicted by the V/Si phase diagram, only V₃Si₂ and V₃Si form in thin-film conditions (few nm to µm). Since the reaction of pure vanadium and silicon usually leads to the undesired compound V₃Si₂, it is necessary to modify the conventional self-aligned process of metal deposition followed by a combination of thermal processing and selective etch. Four approaches were considered to select the V₃Si phase: (i) deposition of pure vanadium on SiO₂, (ii) deposition of V on O-doped Si, (iii) sequential sputtering of V and Si in the right stoichiometry, and (iv) direct sputtering of V₃Si from a compound target. The first two rely on the presence of oxygen to prevent the VSi₂ phase, possibly by slowing the diffusion of Si and so selecting V as the dominant diffusing species. At one extreme, V was deposited on relatively thick SiO₂ layers, which would reliably form V₃Si at the interface, with VOₓ accumulating on the surface. Similar results could be obtained at much lower oxygen concentrations, when the metal was deposited on oxygen-doped amorphous or crystalline silicon. Either technique has the disadvantage of necessitating the selective removal of an oxide layer, and likely leaving residual oxygen contamination in the silicon. The latter would affect the contact resistance, and could impair device performance at cryogenic temperatures by providing parasitic two-level systems. Instead of adding reaction inhibitors that prevent the formation of VSi₂, the nucleation of V₃Si can be aided by providing the right local concentration of the respective elements. Both sequential sputtering of Si and V and deposition from a compound V₃Si target have been shown to be effective to this end. We have opted for this last method, which can ensure continuity to lower film thicknesses than sequential sputtering, and requires only a single target slot in the deposition tool. The clear downside of this process is that while with the salicide process the silicon is only provided by the contact openings connected to the channel, it is now present across the entire surface, and hence the silicidation no longer occurs only locally. It is possible to address this issue with appropriate process modifications.

The V₃Si target had a measured silicon content of 22.7(2) at.% (WDXRF) to 25.7 at.% (supplier data), which may differ from the Si concentration in the deposited layer by 1 at.%. Conflicting reports exist on the impact of a deviation from Si:V stoichiometry on the critical temperature: a reduction in Si content from 25 to 20% has been observed to reduce the critical temperature by 6 K, while others report that a ±20% change in Si content produced hardly any change of $T_c$.

It has been argued elsewhere that while the chemical composition itself is unimportant, any changes in the lattice parameter that it induces may cause large reductions in $T_c$. The V₃Si films were deposited on substrates using RF magnetron sputtering equipment. The pressure, Ar flow and RF power were optimized to obtain the desired V₃Si stoichiometry of the films. During the film deposition, the Ar pressure was maintained at $2.5 \times 10^{-2}$ mbar with Ar flow of 50 sccm. The RF sputtering power was 200 W for all samples. Substrates were in rotation and translation movement during deposition. The thicknesses of the films were determined by an X-ray reflectivity (XRR) method (D8Fabline).

Though previous investigations on sputtering from a compound V₃Si target used heated substrates, in the current study the chuck was at room temperature (not intentionally heated), so that the heating step could be examined separately. The lower deposition temperature led to a relatively higher resistivity of 180(10) µΩcm of the as-deposited layers. Subsequent rapid thermal processing (RTP) occurred under secondary vacuum at different temperatures during two minutes in a Jipelec furnace, with a 20 °C/min ramp rate. Three types of wafers were used as substrate: silicon with 20 nm of thermal SiO₂, HF-cleaned silicon, and sapphire. The V₃Si showed no sign of reacting with the sapphire and SiO₂-coated silicon wafers during a later annealing, though VSi₂ formation occurred on the cleaned Si substrates. In this report we focus on samples where V₃Si was the only silicide phase present.

III. LOW-TEMPERATURE MEASUREMENTS

After deposition, the V₃Si layers were amorphous, with no discernible peaks of the compound present in its XRD diffractogram. This is reflected in its superconducting properties, as the critical temperature was only 0.9 K and 1.2 K on the sili-

![FIG. 1. The critical temperature ($T_c$) of a 200 nm thin film of V₃Si is plotted versus the temperature at which the sample was annealed, with error bars indicating the temperatures at which the sample retained 10% and 90% of the normal-state resistance. Inset: resistance measurements on selected samples, showing sharp drops to zero as they become superconducting. Measurements on as-deposited samples for both substrates are shown with open symbols.](image-url)
Influence of substrate-induced thermal stress on the superconducting properties of V$_3$Si thin films

Counts
Critical temperature ($\bullet$)

While the Si pieces were 20 RRR on some of these pieces, it could straightforwardly be explained by a faster critical temperature due to the substrate cannot be explained this figure shows that there is a clear development of this ratio and sapphire substrates, respectively. Heating the layers promotes crystallization, and the critical temperature improves markedly, approaching that of bulk samples to within 2 K as the annealing temperature was increased to 900 °C. This is illustrated in the main graph of Fig. 1, where each point represents a sample with 200 nm of V$_3$Si that was annealed at the indicated temperature. The continuing upward trend at the higher end of the annealing temperature scale suggests that further improvements in $T_C$ could straightforwardly be achieved.

The rise in critical temperature due to annealing can be attributed to the elimination of scattering centers as the material becomes more ordered and the density of defects is reduced. This can be quantified by the residual resistance ratio $\text{RRR} = R_{260K}/R_{20K}$, where the reference temperature of 260 K is chosen such that data is available for all samples. The electron-electron and electron-phonon interactions that dominate the resistance of a metal at room temperature are strongly suppressed as the material is cooled down. The scattering rate on impurities and defects is temperature-independent however, and is therefore the only contribution that remains, hence providing the residual resistance. Improvements in superconducting properties are associated with larger resistance ratios, illustrated by the strong relationship in Fig. 2. The inset in this figure shows that there is a clear development of this ratio as the annealing temperature is increased, which is nearly independent of the sample substrate.

When plotted both against the annealing temperature and the residual resistance ratio, a clear offset in $T_C$ of 1.9(3) K (Fig. 1) and 1.8(2) K (Fig. 2) is visible between the samples with Si and sapphire substrates. This relative reduction of the critical temperature due to the substrate cannot be explained by different concentrations of impurities or defects, as in this case the points in Fig. 2 would be expected to fall onto a single line. Since the sapphire samples were smaller (10 $\times$ 5 mm$^2$, while the Si pieces were 20 $\times$ 20 mm$^2$), the modestly higher RRR on some of these pieces could be explained by a faster thermalization during the annealing. This cannot, however, account for any of the difference between sapphire and silicon in the relation between RRR and $T_C$. The substrate therefore appears to affect the superconducting behavior of the V$_3$Si without necessarily altering the dynamics of the silicide formation. The superconducting transitions on the sapphire substrate are also sharper, with an average transition width $T_{90\%} - T_{10\%}$ of 3.0(7) % of the critical temperature, while that on the silicon substrate is 6.2(7) %. This suggests that in addition to improving the average superconducting behavior of the material, the sapphire substrate also reduces local variations, causing the material to be more homogeneous at low temperatures.

IV. IN-SITU XRD ANALYSIS

One sample of each substrate with 200 nm of V$_3$Si was heated in steps of 50 °C up to 600 °C and then in steps of 20 °C to 1000 °C. The temperature was held constant after each step for around 15 minutes, and an out-of-plane $\theta$-2$\theta$ XRD scan was performed. After the samples cooled down to 30 °C, a final measurement was taken. Even when the constituent elements are already intermixed, it is not expected that they would form the silicide phase unless sufficient thermal energy is supplied to stimulate atomic movement and bond formation, and to overcome the barrier posed by the surface energy of a newly formed crystallite. This thermal activation of the formation is demonstrated by the absence of any peaks in the scans up to 450°C. Three peaks of the cubic A15 V$_3$Si phase at 38.0° (200), 42.7° (210) and 47.1° (211) become visible on both substrates at 500°C, each becoming sharper and moving to smaller angles as the temperature is increased. Individual scans at 550, 780 and 1000 °C are shown in Fig. 3, while the shift in peak positions with temperature is made more explicit in Fig. 4. The shift of the peaks to smaller angles is explained by the thermal expansion of the V$_3$Si, and is affected by strain imposed by the substrate, which expands at a different rate. Using the Scherrer equation, it is possible to estimate the

FIG. 2. Residual-resistance ratio (RRR), here defined as the ratio of the resistances at 260 to that at 20 K, increases with annealing temperature for both substrates, indicating a reduction in defect density or clustering of impurities.

FIG. 3. Selected $\theta$-2$\theta$ curves measured at 550, 780 and 1000 °C, reference peak positions of the (200), (210) and (211) planes are indicated by black lines.
crystallite size from the full width at half maximum of each of the three peaks. In the top panel of Fig. 4, a weighted average (weighted by peak area) of these three values is shown for each temperature, showing a continued crystal growth during the measurement.

Though there is no one-to-one correspondence between the crystallinity observed at a given temperature during the in-situ experiment and that obtained after thermal processing for two minutes at that same temperature, the general relationship is assumed to hold. The improvements in resistance ratio and critical temperature with increasing RTP temperature as shown in Figs. 1 and 2 can thus likely be attributed at least in part to enhanced crystallinity. This does not mean, however, that the differences in superconducting properties between the two substrates can also be explained by the quality of the material. If the sapphire substrate were to better promote \( V_3Si \) growth, one would expect to see both larger grains and a higher degree of texture. We found no sign of either. The grain size developed at a similar rate on sapphire and oxidized silicon, and no significant difference between the two substrates was observed in the distribution of crystal orientations. The films are preferentially oriented along the \( <210> \) direction on both substrates. Nor did any of the three analyzed peaks exhibit growth relative to the others while the temperature was increased, as would be expected in the case of epitaxial alignment. The differences in superconducting behavior between the two substrates therefore cannot be ascribed to a relative improvement in crystallinity on the sapphire substrate.

The dependence on temperature of the \( V_3Si \) peak positions was used to calculate the out-of-plane expansion of the crystals. In Fig. 5, the change in lattice parameter relative to a PDF reference value is shown. The parameter was calculated from each of the three peaks, after which an average value was taken. This average was weighted by the relative peak areas to account for the larger uncertainty in the position of the smaller peaks. An offset between the expansions on silicon and sapphire is immediately apparent, as well as a sudden reduction in volume on both substrates between 660 and 700 °C. The latter is attributed to a plastic deformation of the crystal as strain is relaxed that was built up during the transition from the initial amorphous phase to the more efficiently packed crystal phase.

On the sapphire substrate the rate at which grains expand out of plane is found to depend on their orientation: the grains that are tilted with respect to the horizontal substrate, represented by the (210) and (211) peaks, expand at a higher rate. On silicon, however, each peak gives the same expansion rate. This is illustrated by the bar graph inset in Fig. 5, where each bar represents the average linear thermal expansion coefficient of grains oriented along the indicated Miller indices, calculated with a linear regression on peak positions obtained between 700 and 1000 °C. The fact that the expansion rate depends on the orientation on the sapphire substrate, while it does not on silicon, can be explained by sapphire’s larger thermal expansion coefficient. When taking into account the volume reduction due to the crystallization of the initially amorphous layer, the \( V_3Si \) likely has an effective expansion rate similar to that of the silicon substrate, so that little thermal stress will occur. The situation is different on sapphire, which expands faster and so imposes an in-plane tensile strain on the silicide layer. Sapphire has a room-temperature thermal expansion coefficient of \( 5.0 \times 10^{-6} \) K\(^{-1}\) orthogonal to the c-axis, which is the in-plane direction of our substrates, while that of silicon is \( 2.6 \times 10^{-6} \) K\(^{-1}\) in all directions. Meanwhile, monocrystalline \( V_3Si \) has an expansion rate of \( 7.5 \times 10^{-6} \) K\(^{-1}\) at room temperature.

Crystals with their main lattice planes aligned normal to the substrate can minimize the change to their unit cell volume by compensating for the in-plane expansion with a reduction in the out-of-plane lattice parameter. As a result, the (200) peaks in the \( \theta-2\theta \) scans exhibit a smaller thermal expansion coefficient on sapphire than on silicon. When crystals are tilted with respect to the imposed strain, however, they will either undergo a shearing deformation or see a change in their unit cell volume, both of which are energetically unfavorable. The more misaligned a grain is, the harder it therefore is to compensate for in-plane tensile strain by out-of-plane contraction, which explains why those oriented along the \( <211> \) axis have a larger out-of-plane thermal expansion coefficient than the \( <210> \) grains, which in turn expand faster than those oriented \( <200> \).

Two more XRD scans were performed after the samples were cooled down to room temperature, visible on the bottom-left of Fig. 5. Residual strain is present in the \( V_3Si \) on the silicon substrate, as the out-of-plane lattice parameter is -0.3%
Testardi and coworkers developed a thermodynamic model in the 1970’s that describes the general dependence of the critical temperature of A-15 superconductors on strain. A second-order expansion in strain coefficients $\varepsilon_i$ was proposed, where the coefficients were determined using sound velocity and specific heat measurements. Given a $6 \times 1$ strain matrix $\varepsilon$, this dependence was given as

$$T_c(\varepsilon) - T_c(0) = \sum_i T_{ii} \varepsilon_i + \frac{1}{2} \sum_i \sum_j \Delta_{ij} \varepsilon_i \varepsilon_j.$$  

(1)

In the case of V$_3$Si it was found that $\Delta_{11} = -24 \times 10^4$ K, $\Delta_{12} = -5 \times 10^4$ K, $\Delta_{44} = -1 \times 10^4$ K, and $|\Gamma| < 50$ K, with all other $\Delta_{ij} = 0$.

If the volume remains constant, as it is reported to do precisely, then equal strains $\varepsilon_2 = \varepsilon_3$ applied along the two in-plane axes are associated with an out-of-plane strain $\varepsilon_1$ of twice their magnitude (assuming $\varepsilon_i \ll 1$):

$$\varepsilon = \left( \varepsilon_1, -\frac{\varepsilon_1}{2}, -\frac{\varepsilon_1}{2}, 0, 0, 0 \right), \quad \text{with} \quad \varepsilon_1 = \frac{2}{3} \left( \frac{c}{a} - 1 \right).$$  

(2)

This means that only the terms with $i, j = 1, 2, 3$ need to be kept in eq. (1), which simplifies to

$$T_c(\varepsilon) - T_c(0) = \frac{3}{4} \varepsilon_1^2 \left( \Delta_{11} - \Delta_{12} \right).$$  

(3)

The coefficients $\Delta_{11}$ and $\Delta_{12}$ in this expression were originally determined for bulk samples, while the current study considers thin films. To compare results, it is necessary to first estimate the strain in the V$_3$Si layers at the critical temperature, which can be done by extrapolating from the strain measured at room-temperature.

For those crystals that have one of the cubic axes oriented vertically, we assume that the measured deviations in the room-temperature out-of-plane lattice parameters shown in Fig. 5 correspond to such a tetragonal deformation. Their values are $\varepsilon_1 = 0.2(4) \times 10^{-3}$ and $\varepsilon_1 = -3.3(1) \times 10^{-3}$ on sapphire and silicon, respectively. The thermal contractions of the substrate materials and V$_3$Si down to cryogenic temperatures have been determined previously. Taking these into account as the samples cool from room temperature to the critical temperature of V$_3$Si, listed in Table I, we find the following estimates for the strain at $T_c$:

$$\varepsilon_1^{\text{sapphire}} = -0.9(5) \times 10^{-3}, \quad \varepsilon_1^{\text{silicon}} = -5.2(2) \times 10^{-3}.$$  

(4)

When used in eq. (3), these values correspond to reductions in the critical temperature between 0 and 0.3 K on sapphire, and between 3.5 and 4.2 K on silicon, compared to unstrained bulk V$_3$Si. Conversely, a reduction in $T_c$ of 1.9(3) K would in the case of a purely tetragonal deformation be associated with an out-of-plane strain of $3.7(3) \times 10^{-3}$. The behavior of the polycrystalline layer during cooling is more complex, however, than a uniform strained contraction, since not all grains have one of the cubic axes aligned vertically. Differently oriented grains could exhibit different modes of deformation in response to an in-plane tension, and the picture is complicated by an unpredictable degree of tetragonal deformation prevalent in A-15 superconductors.

A Martensitic tetragonal deformation is observed in most, though not all, monocrystalline samples of V$_3$Si and is associated with a strain up to $\varepsilon_1 = -2 \varepsilon_{2,3} = 1.7 \times 10^{-3}$, where...
TABLE I. The estimated contractions of sapphire\textsuperscript{12}, silicon\textsuperscript{43} and V\textsubscript{3}Si\textsuperscript{15,44} from 300 to 16 K (valid both in-plane and out-of-plane), and the induced out-of-plane expansion of V\textsubscript{3}Si.

| Material   | Contraction Relative to V\textsubscript{3}Si | Induced $\Delta t$ |
|------------|---------------------------------------------|-------------------|
| Sapphire   | $-6.2(8) \times 10^{-4}$                    | $-1.2(3) \times 10^{-3}$ |
| Silicon    | $-2.3(2) \times 10^{-4}$                    | $-1.9(2) \times 10^{-3}$ |
| V\textsubscript{3}Si | $-1.2(1) \times 10^{-3}$                    | — |

the unit cell contracts along two axes while it expands along the other, generally referred to as the $a = b$ and $c$ axes. It should be noted that those samples where the transformation did not occur were found to have lower resistance ratios $R_{300K}/R_{20.5K}$ than those where it did\textsuperscript{41}. It is likely that this deformation occurs to some degree in strained polycrystalline samples as well, with the axes of expansion necessarily misaligned. The larger reduction in $T_c$ on silicon is due to an in-plane tensile strain. Therefore, grains where the expanding $c$-axis of the Martensitic transition is close to in-plane, the critical temperature would be further reduced. In others, the Martensitic deformation and the strain imposed by the substrate could partially compensate each other, where the compensation would be maximal when the $c$-axis points out of plane. The smaller relative reduction in $T_c$ on silicon than would be expected from the extrapolation of the measured room-temperature out-of-plane lattice parameters suggests that for a large share of the grains the Martensitic deformation compensates for the thermal stress. This implies that the substrate-induced strain selects a preferential axis for the Martensitic transition, such that the total deformation from a cubic crystal is minimized. The dependence of the critical temperature on the orientation of the grains also provides a mechanism for the observed broadening of the superconducting transitions on the silicon substrate, as discussed earlier in section III.

Grains that are tilted relative to the vertical axis cannot accommodate the imposed strain with only a tetragonal deformation, and need to undergo a combination of volume change, plastic deformation and shearing. The first two are unlikely to contribute much, since V\textsubscript{3}Si tends to preserve its unit cell volume\textsuperscript{41}, and the reversibility of the tetragonal deformation\textsuperscript{15} suggests that no plastic changes should occur. Shearing is more likely to take place considering the strong reduction in the restoring force for shear deformation at low temperatures\textsuperscript{30}. However, since $\Delta_{14} \ll \Delta_{11} - \Delta_{12}$, this is expected to contribute less to the broadening of the superconducting transitions than the misalignment of the $c$-axes of the Martensitic deformations of different grains in the polycrystalline film.

VI. CONCLUSION

Vanadium silicide is found to have a lower superconducting critical temperature on silicon substrates than it does on sapphire, a difference that cannot be straightforwardly ascribed to improvements in purity or crystallinity. In-situ XRD analysis during heating and cooling of as-deposited samples revealed that the thin films respond strongly to thermal expansion mismatches with the substrate, leaving the material relatively strained on silicon when cooled down after crystallization. This imposed strain is increased upon cooling to cryogenic temperatures, and is assumed to depend strongly on grain orientation due to the near vanishing of the shearing restoration force at low temperatures and the expected presence of a Martensitic transition just above $T_c$. The observed reduction in critical temperature, as well as the broadening of the superconducting transitions, due to this inhomogeneous strain is well explained by an existing thermodynamic model for the A-15 superconducting compounds.

Strain thus offers a pathway to critical temperature modulation of this class of superconductors. It may be relaxed by prolonged heating, in which case it is predicted to increase the critical temperature of V\textsubscript{3}Si and V\textsubscript{3}Ga thin films, and decrease that of V\textsubscript{3}Ge\textsuperscript{30}. The engineering of local strain has previously been demonstrated on the scale of a few tens of nanometers\textsuperscript{46,47}, an approach that could also be used to compensate for the stresses introduced by silicidation\textsuperscript{48}, or to spatially vary the superconducting properties of these materials.

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