Impacts of material parameters on breakdown voltage and location for power MOSFETs

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Received: 16 June 2022 / Accepted: 7 July 2022 / Published online: 25 July 2022
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Abstract
To improve the electrical performance of power devices, materials used in fabrication need to be analyzed and optimized. By numerical simulations, we reveal that the breakdown voltage (BV) and location of a lateral diffused MOS power device simultaneously depend also on trench oxide permittivity. For a given device geometry, while the trench oxide permittivity with a certain value leads to a maximal BV, a smaller (larger) value causes electrical breakdown in the Si drift channel around the bottom (top) of the trench. This trend remains the same when Si is replaced by SiC. Our study implies that any by-product reducing the trench permittivity during trench filling should be avoided.

Keywords: Permittivity · Breakdown · Lateral diffused MOS

1 Introduction
Trench process has been widely used in semiconductor fabrication, such as shallow trench isolation, tall fin, and lateral trench formations. The latter has to be optimized to achieve better electrical performance in terms of a higher BV and a lower specific on-resistance of a lateral diffused MOS (LDMOS) power device [1–3].

Following the trench formation and oxidation remedy at the etched Si surface, the trench is refilled with oxide (normally SiO₂ with an ideal relative permittivity value \(\varepsilon_{\text{ox}}\) of 3.9) by chemical vapor deposition (CVD) [4, 5]. In CVD process, the temperature, pressure and precursors significantly affect the permittivity of the trench oxide. The value can be smaller than ideal \(\varepsilon_{\text{ox}}\) due to sloppy microstructures and incorporation of hydrogen and carbon atoms [6]. On the other hand, the presence of nitrogen and other metallic elements in the trench oxide will result in a larger value of \(\varepsilon_{\text{ox}}\) [7]. However, the impact of permittivity of the trench oxide on the LDMOS is rarely discussed [8].

A larger bandgap \(E_G\) of the host semiconductor for a power device theoretically guarantees a higher BV. However, a semiconductor with a wider \(E_G\) normally possesses a lower relative permittivity \(\varepsilon_s\), which may unfortunately enhance the electric field. However, the influence of these two semiconductor parameters on power devices is still unrevealed in detail.

Therefore, we investigate the correlation between material (both semiconductor and oxide) permittivity and electrical breakdown of LDMOS power devices by using a technology computer-aided design (TCAD) simulator. We quantitatively discuss the impacts of a larger \(E_G\) and a smaller \(\varepsilon_s\) on BV as well.

2 Simulation approach
The simulated Si LDMOS device is shown in Fig. 1a, and its electrical characteristics is calculated by solving Poisson and hydrodynamic equations self-consistently with Fermi statistics and an initial temperature set at 300 K [9]. Carrier mobility is modeled with concerns of high field saturation, impurity and surface roughness scattering. Carrier generation and recombination are considered by including Auger, avalanche, doping-dependent and field-enhanced Shockley–Read–Hall (SRH) models. And default parameters of these models for Si are used in simulations.
Both carrier and lattice temperatures can theoretically rise because energy of carriers increases due to electric field acceleration and then relaxes to the lattice via scattering. This phenomenon is likely to lead to different temperatures between the carrier and lattice in a power device. Compared to drift–diffusion formulism, hydrodynamic model is able to take nonequilibrium effects into account [10]. Particularly, avalanche model requires carrier and local lattice temperatures for accurate predictions [11]. As a consequence, besides including hydrodynamic transport model, carrier temperature is also coupled to high field saturation, SRH and avalanche models in the simulations.

3 Results and discussion

3.1 Simulations with default Si parameters

Figure 2 shows the $I_{DS}-V_{DS}$ curves of the LDMOS devices with default Si parameters and different $\varepsilon_{ox}$. All curves almost fall on top of each other when $V_{DS} < 70$ V, which implies that the on-resistance is hardly affected by different trench oxide $\varepsilon_{ox}$.

This is attributed to the fact that the current flow is not confined at the trench interfaces. The abrupt increase of the drain current can be clearly observed when the drain voltage reaches a certain value for each LDMOS device. After BV extraction from Fig. 2, the correlation between BV and trench oxide $\varepsilon_{ox}$ is presented by the black squares in Fig. 3. With the maximal at $\varepsilon_{ox} = 3$, the BV drops rapidly with increasing and decreasing $\varepsilon_{ox}$. Compared to the BV at $\varepsilon_{ox} = 3$, BV value drops by 24.6%, 2.2% and 12.3% at $\varepsilon_{ox} = 2$, 3.9 and 5, respectively. This result strongly suggests strict fabrication control of the trench oxide deposition.

Figure 4 displays the electric field (E) and electrostatic potential contour corresponding to the simulations in Fig. 2 at BVs. With $\varepsilon_{ox} = 1$, $V_{DS}$ drops along the U-shaped lightly doped drift region and the maximum E around the trench corner can be observed, where the avalanche breakdown happens. With $\varepsilon_{ox} = 3$, thanks to the reduced surface field (RESURF) effect [12], more even distribution of $V_{DS}$ drops between the top and bottom corners of the trench is achieved, accounting for the maximal BV in Figs. 2 and 3. With further increasing $\varepsilon_{ox}$, the enhanced electrical coupling between the source and drain is directly via the top of trench oxide, concentrating $V_{DS}$ drop, augmenting the E around the top corner of the trench and reducing VB.

3.2 Simulations with modified Si parameters

With Si default parameters in simulations, the maximal BV takes place at $\varepsilon_{ox} = 3$ as shown in Figs. 2 and 3. It may be
worthy to study whether this result can be influenced by changing Si parameters to wide-bandgap material ones. To make the study more transparent, we decouple the impacts on these default and modified Si parameters, the BVs of the LDMOS devices are exhibited in Fig. 3. With a constant $E_G$ although a lower $\epsilon_s$ of a wide bandgap material tends to counteract the BV improvement.

4 Conclusion

By numerical simulations, we reveal that the breakdown voltage (BV) and location of a lateral diffused MOS power device simultaneously depend on trench oxide permittivity. For a given device geometry, while trench oxide permittivity of around 4 leads to a maximal BV, a smaller (larger) permittivity value causes breakdown in the Si drift channel around the bottom (top) of the trench. Our study implies that any by-product reducing the trench permittivity during trench filling should be avoided.

Acknowledgements This work is financially supported by the Young Scholar Fellowship Program from Ministry of Science and Technology, Taiwan, under Grant MOST 110-2636-E-006-004.

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