Efficient Analog CAM Design

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Abstract—Content Addressable Memories (CAMs) are considered a key-enabler for in-memory computing (IMC). IMC shows order of magnitude improvement in energy efficiency and throughput compared to traditional computing techniques. Recently, analog CAMs (aCAMs) were proposed as a means to improve storage density and energy efficiency. In this work, we propose two new aCAM cells to improve data encoding and robustness as compared to existing aCAM cells. We propose a methodology to choose the margin and interval width for data encoding. In addition, we perform a comprehensive comparison against prior work in terms of the number of intervals, noise sensitivity, dynamic range, energy, latency, area, and probability of failure.

Index Terms—Analog CAM (aCAM), In-Memory Computing, Memristor, TCAM, ReRAM, Content Addressable Memory.

I. INTRODUCTION

On account of the imminent barrier to Moore’s law in CMOS technology, also known as the power wall, revolutionary approaches for systems integration are needed. The quest for more advanced novel nanoelectronics with low-power functionality and dense reconfigurable electronics integration has brought up a promising element: the memristor. As a prospective candidate, the memristor has substantial advantages, such as inexpensive manufacturing, ultrahigh density, non-volatility, low power, and most importantly CMOS compatibility, which allows the advancement of Moore’s Law beyond the present silicon roadmap horizons [1]. Memristors are programmable and exhibit a controllable hysteresis during operation making them a viable candidate for a vast majority of applications [2]. These include non-volatile processors, highly programmable and self-adaptable analog/digital electronics, in-memory compute, resistive nanocomputing architectures, and synaptic neuromorphic networks [1].

More recently, associative and approximate computing using resistive memory based Ternary Content Addressable Memory (TCAM) is becoming increasingly popular. Content Addressable Memories (CAM) are storage devices that can be searched in a parallel manner to match the input data and return the address of the matching content. While CAMs require an exact match to the input, Ternary CAMs stand out as an extension where partial searches are possible, as they allow “don’t care” conditions on parts of the searched data [3]. The highly parallel in-memory operation of the TCAM results in very high throughput compare operations at low latency, leading to commercial success in different applications including network routing [4], [5], real-time network traffic monitoring [6], and access control lists (ACLs) [7]. Such architecture styles, though immensely useful, struggle with high power consumption and low density when implemented in standard CMOS technology. Various memristor-based TCAM design options have been proposed to tackle these concerns, benefiting from their non-volatility and high packing density. Nevertheless, in most memristor-based CAM designs, the memristor encodes only binary states, and its highly tunable analog conductance is not utilized.

Accordingly, the memristor-based analog CAM (aCAM) was proposed to leverage the tunable conductance of memristive devices to store a range of values in each cell [8]. Cells can cover overlapping wide ranges or small discrete ranges. This allows to compare an analog or encoded multi-bit input to the stored range to decide on a match or a mismatch and thus enhances memory storage capability. Given the aCAM’s ability to store wide intervals of continuous levels, new search functionalities in the analog domain are possible [8]. This along with multi-bit capabilities offer improved memory densities along with reduced power [8], which in turn allows the use of aCAMs for more generic applications. These applications include associative computing [9]–[12] which benefit from these properties as it usually suffers from limited memory densities and high power consumption of traditional CAMs. Furthermore, in aCAM, joint intervals may result in a larger number of possible non-mutually exclusive states. Multi-bit CAM cells (MCAM) can also be implemented using other switching devices such as NAND Flash [13]. A recent study [14] compared different types of switching devices including memristors, phase change, magnetorsistors, and FeFET devices. Memristor devices stood out in many key properties such as the maximum number of distinguishable states, switching speed, endurance, and retention, thereby qualifying them as good candidates for aCAM applications. More recently, the authors in [15]–[18] introduced HfO$_2$ based Ferroelectric field-effect transistors (FeFET) aCAM and MCAM cells where FeFETs were used due to improved compactness, multi-level programmability, and density. They demonstrated the ability to encode 2-3 bits, i.e., up to 8 levels, with some overlap between adjacent levels in the presence of variability [15].

Our study is oriented towards the memristor based analog CAMs analog CAMs with single data search lines and programmable analog/multi-bit intervals [8]. Fig. 1 shows the structure of the memristor based aCAM cell proposed in [8]. It consists of two voltage divider subcircuits: (1) the lower bound subcircuit (LBS) and (2) the upper bound subcircuit (UBS).
applications. In this paper, we propose two new aCAM cell designs with improved gain capabilities. We compare these designs along with a switch based cell [8] in terms of different design metrics. We further develop an interval building algorithm for aCAM cells that draws boundaries, i.e., margins, between discrete intervals to ensure proper operation and guard against noise and process variations.

The contributions of this paper can be summarized in the following:

- We propose two new aCAM cell designs: the 10T2M and 8T2M aCAM cells and explore the improvements in the gain and other design metrics in comparison to the 4T2M2S cell proposed in [8].
- For purposes of multi-bit storage, we develop an interval building algorithm to determine the memristor configurations that result in a maximum number of discrete intervals while maintaining conservative margins between the intervals to ensure proper differentiation between match and mismatch and ensure operation in the presence of noise and/or process variations. We relied on SPICE simulations for interval building and validation. We also relied on heuristics to determine a desired number of intervals the configurations that maximize the dynamic margin, the match line difference between the full match and 1-mismatch scenarios.
- We compare the different designs in terms of key metrics such as the maximum number of intervals, dynamic range, latency, fail probability, energy, and area. Our studied memristor based CAMs proved the ability to encode up to 4 bits of storage and a maximum of 17 intervals for the 8T2M cell and 24 intervals for 10T2M with 5-10x lower latency than the 4T2M2S design. The latter enabled 6 distinguishable intervals at the same noise guarding level (10% \(V_{DD}\)) and up to 31 intervals at low noise guarding levels (2% \(V_{DD}\)).
- Finally, we study the behavior of the proposed aCAM cells under variability and process variation considerations.

The remainder of the paper is organized as follows: Section II discusses the aCAM concept, operation, and the circuit realization that has been proposed in [8]. Section III introduces two new circuit realizations for the aCAM and discusses the designs along with a switch based cell [8]. Section IV examines the margin methodology and the algorithms implemented for interval building and figure of merit analysis. Section V presents the simulation results and a comparative analysis of the different circuit designs. Finally, section VI concludes the work.

II. ACAM CELL DESIGN AND ANALYSIS

A. 6T2M aCAM cell Overview

Similar to current CAM setups, the search operation in the 6T2M design starts by precharging the ML to a high logic level, and the ML stays high (match) only when the search input is within the bounds determined by the two subcircuits, otherwise, ML discharges through transistors T1 and/or T2, thereby leading to a low logic level (mismatch) on the ML. Thus, a match occurs when both gate voltages of transistors
T1 and T2, $V_{G1}$ and $V_{G2}$, respectively, are smaller than the threshold voltage, thereby keeping the transistor channels in a high resistance state.

**Lower and Upper Bound Subcircuits:** as shown in Fig. 1 the LBS consists of a resistor-based inverter comprising a transistor and a series-connected memristor M1, which generates the gate voltage $V_{G1}$ for T1 to embody the aCAM cell’s lower bound LB match threshold. The value of this match threshold is configured by tuning the memristor conductance in the resistor-based inverter circuit. When an applied input voltage $V_{DL}$ is larger than this match threshold, a small voltage will build on G1 and yield a match due to the fact that T1 will remain off. The upper bound of the search range, UB, is configured similarly with an independent voltage divider using memristor M2 and an inverter to control the gate voltage $V_{G2}$ of the second pull-down transistor T2 (Fig. 1). As a result, the cell yields a match and keeps ML high only when $V_{DL}$ is within a certain range set by the resistance values for memristors $R_{LB}$ and $R_{UB}$.

Table I summarizes the match/mismatch states based on $V_{G1}$ and $V_{G2}$ values in an ideal framework. Fig. 3 represents the LBS and UBS voltage transfer characteristics (VTC) for $V_G$ versus $V_{DL}$. As such, we can rely on such curves to determine the lower and upper bounds for a given pair of M1 and M2 resistances, respectively, based on the $V_{DL}$ values that result in $V_{G1} = V_{in}$ and $V_{G2} = V_{in}$. For example, for the simulated VTC curves in Fig. 3, the range: [LB, UB] = [0.255, 0.374]V can be obtained for $R_{LB} = 619 K\Omega$ and $R_{UB} = 63.1 K\Omega$.

**B. Cell Conductance Sensitivity**

In [8], it was stated that when the word length is long enough, sensing errors and/or changes in the accepted search range of an aCAM cell are likely to occur. This is because the cell conductance, $G$, is related to current leakages through the pull-down transistors, whose gates are controlled by $V_{DL}$. So if $G$ is continuous with respect to $V_{DL}$ ($G = f(V_{DL})$), the higher $\partial G_T/\partial V_{DL}$ at the boundary of interval, the better the capability to store more accurate ranges and accordingly more bits of discrete levels. $\partial G_T/\partial V_{DL}$ can be best defined as:

$$\frac{\partial G_T}{\partial V_{DL}} = (\alpha S_s)^{-1}$$  \hspace{1cm} (1)

where $\alpha = \frac{\partial V_{DL}}{\partial G} = (1/gain)$, and $S_s$ is the subthreshold swing slope of the transistor. So for better sensitivity, we need lower $S_s$ and higher gain, i.e., steeper $V_G$ vs $V_{DL}$ VTC slopes, as shown in Fig. 3.

**III. PROPOSED aCAM DESIGN ALTERNATIVES**

In this section, we present new aCAM cell designs that improve the conductance sensitivity in (Eq. (1)) and hence the word length and memory storing capabilities through...
improving the gain as opposed to the 4T2M2S cell that relies on enhancing subthreshold swing. We focus on improving $\frac{\partial V_G}{\partial V_{DL}}$ for the LBS design which demonstrates lower gains compared to $\frac{\partial V_G}{\partial V_{DL}}$ in the UBS design as can be inferred from the VTC curves in Fig. 3 where the UBS VTC shows steeper transitions. To enhance the sensitivity of the LB curves and obtain steeper lower bounds (better sensitivity), we propose two new LBS designs. Note that the UBS remains unchanged.

A. 10T2M aCAM Cell

We first study inserting a simple non-inverting buffer composed of two inverters before T1 to maintain the same functionality, while boosting gain (albeit at a cost of area) as illustrated in Fig. 5. Fig. 6 (a) illustrates the enhancement in the slopes of the LBS, as compared to that of the initial 6T2M circuit (Fig. 3 (a)), as they became much steeper. This results in up to 40 times improvement in the gain (at low conductance) compared to the 6T2M design (Fig. 7).

B. 8T2M aCAM cell

A more compact version can be introduced by replacing T1 with a PMOS transistor preceded by an inverter as illustrated in Fig. 8. We studied the VTC curves ($V_{G1}$ vs $V_{DL}$) as well as the gain in Fig. 6 (b) and 7 respectively, for the 8T2M cell. We record up to 6 times improvement in the gain for this new design in comparison to the 6T2M cell. Note that for the 8T2M, for a LB match, T1 (PMOS) must be off; hence, $V_{G1}$ must be high, $V_{G1} > V_{PC} - |V_{tp}|$, where $V_{PC}$ is the ML pre-charge voltage. Table II summarizes the match/mismatch states criteria for the 8T2M cell in an ideal framework. In addition, Some examples of transient signals of reading the three cells are shown in detail in the Supplementary materials (Fig. 3).

IV. INTERVAL BUILDING AND MARGINING

Herein, we develop an interval building algorithm that determines the proper memristor configurations in order to maximize the number of aCAM discrete intervals without sacrificing functionality while guarding against noise and process variations.
A. aCAM Row

Each aCAM cell creates a pull-down (up) path to the ML based on its state: match or mismatch. Thus, the cell is associated with a corresponding effective resistance, and hence channel conductances of transistors (or switching memristors) involved.

The effective match and mismatch resistances of an aCAM cell are

\[ R_{fm} = 0.5 R_{on} \]

\[ R_{1mm} = R_{on}/R_{off} \approx R_{on}, \]

where \( R_{on} \) and \( R_{off} \) are the on and off resistances of the pull-down transistor for the 10T2M and 8T2M cells, and the effective resistances for the 4T2M2S cell. As several cells are connected on the same ML in a row, just like digital CAMs, a row ML outputs “high” (“low” for 4T2M2S circuit) when all the cells in the row match. This represents a full match state (fm). A mismatch state incorporates charging (discharging for 4T2M2S) the ML. We typically optimize the design to properly differentiate between the fm and the one mismatch (1mm) being the weakest mismatch case as shown in Fig. 9.

The search range for one cell is affected by other cells in a row. Subthreshold current leakages via the ML pull-down transistors usually restrict the maximum length of CAM words and the number of bits held by each cell. Given \( N \) cells per row, the fm and 1mm effective resistances, \( R_{fm} \) and \( R_{1mm} \), respectively, of the aCAM row can be defined as follows:

\[ R_{fm} = \frac{R_{on}}{N} \]

\[ R_{1mm} = \frac{R_{on}R_{mm}}{R_{on} + (N-1)R_{mm}} \]

The design is robust when operating in conditions that enable differentiation between \( R_{1mm} \) and \( R_{fm} \). This can be either achieved by choosing sparse discrete levels, or by relying on designs whose effective resistance or conductance demonstrate high sensitivity to changes in \( V_{DL} \). This is in coherence with the requirement in section II-B.

B. Margining Overview

As stated in [8], the memristor configurations can be used to allow the array to store “continuous ranges of value”, or “discrete levels”. In the context of our work, we are interested in identifying memristor configurations for discrete levels. Based on this, we assume that the array cells may be storing discrete values for purposes of multi-bit storage. We determine basic definitions for discrete level programming given in Table III.

Our objective is to identify functional levels \( \{D_i\} \), and their corresponding programmable values, \( R_{L,B_i} \) and \( R_{U,B_i} \), that maximize the potential of a given design without sacrificing accuracy and functionality. Particularly, the intervals must allow for proper differentiation between full-match and one mismatch states, i.e., differentiating between \( R_{fm} \) and \( R_{1mm} \). This can be achieved when \( R_m \geq R_{mm} \), and the ideal set \( \{D_i\} \) allows for large \( R_{mm} \) during match for minimal leakages, and small \( R_m \) of the mismatching cells for fast evaluations during mismatch and proper separation.

In the simplest form, to determine the stored intervals, we can assume a cutoff voltage equal to the threshold voltage of the transistors (e.g., \( V_{th} = 0.4 = V_{DD}/2 \)). Thus, for a given pair of \( R_{LB} \) and \( R_{UB} \) resistances, the LB and UB of the stored interval are defined as the \( V_{DL} \) values that result in \( V_{G1} = V_{DD}/2 \) and \( V_{G2} = V_{DD}/2 \), respectively, as explained in section II-A. However, this eliminates the differentiation between the effective \( R_m \) and \( R_{mm} \). Furthermore, the designs can be subject to noise and/or process variations and this can affect their operation.

To guarantee proper functionality in terms of the ability to differentiate between match and mismatch scenarios and to guard against noise and process variations, we devise the following. Instead of relying on a single cutoff level to build the intervals, we rely on two cutoff levels, as will be explained next, that result in margins between the intervals. These margins help us restrict to specific levels the outputs of the LB and UB subcircuits, which in turn are inputs to the devices that discharge the match line and hence help maintain reasonable effective \( R_m \) and \( R_{mm} \). This guarantees (1) better dynamic ranges and better responses. As such, uncertainties are minimized and a matching value for one interval results in a proper mismatch for another. It also (2) guards against noise and process variations. For the latter, we incorporate Monte Carlo analysis for forbidden region construction to secure proper functionality for non-nominal cells with process variations.

Definitions: To build the intervals with proper margins, we rely on the following terms that are key for our interval building algorithm as summarized in Table III and illustrated in Fig. 10. In Fig. 10, the figure presents a sketch for the lower bound and upper bound subcircuit output responses \( V_{G1}V_{DL} \) and \( V_{G2}V_{DL} \) respectively for an arbitrary \( R_{LB} \) and \( R_{UB} \); output nodes \( G_1 \) and \( G_2 \) feed the switches that will charge or discharge the match line.

| \( \eta \) | number of discrete voltage levels; e.g., \( \eta = 8 \) represents 3-bit storage in the cell |
| --- | --- |
| \( D_i \) | represents the \( i^{th} \) discrete voltage level; \( D_i \in [0, V_{DD}] \) |
| \( R_{L,B_i} \) | represents LB subcircuit memristor value corresponding to the \( i^{th} \) discrete voltage level \( D_i \) |
| \( R_{U,B_i} \) | represents UB subcircuit memristor value corresponding to the \( i^{th} \) discrete voltage level \( D_i \) |
| \( Cell_i \) | cell that is programmed using \( R_{L,B_i} \) and \( R_{U,B_i} \) |
The list of terms starts with the two subcircuit output cutoff levels that will be used for the interval building: $V_{Gi\text{lo}}$ and $V_{Gi\text{hi}}$, as presented next along with some other definitions.

1) $V_{Gi\text{lo}}$: represents the desired subcircuit output response low voltage levels as a percentage of $V_{DD}$ for proper match. E.g., $V_{Gi\text{lo}} = 0.1 * V_{DD}$. 

2) $V_{Gi\text{hi}}$: represents the desired subcircuit output response high voltage levels as a percentage of $V_{DD}$ for proper mismatch. E.g., $V_{Gi\text{hi}} = 0.9 * V_{DD}$. 

3) $LB_{io}$: corresponds to $V_{DL}$ value that results in $V_{G1} = V_{Gi\text{lo}}$ for the LB circuit. 

4) $LB_{hi}$: corresponds to $V_{DL}$ value that results in $V_{G1} = V_{Gi\text{hi}}$ for the LB circuit. 

5) $UB_{lo}$: corresponds to $V_{DL}$ value that results in $V_{G2} = V_{Gi\text{lo}}$ for the UB circuit. 

6) $UB_{hi}$: corresponds to $V_{DL}$ value that results in $V_{G2} = V_{Gi\text{hi}}$ for the UB circuit. 

7) $[LB_{io}, UB_{io}]$: Match interval boundaries guarantee $V_{G1}$ and $V_{G2}$ values to be low enough for interval match. This ensures better matches and leaves room or noise guarding. 

8) $FR(R_{LB}) = [LB_{hi}, LB_{io}]$: Lower forbidden region boundary guarantees $V_{G1}$ output to be high enough for inputs from lower intervals. This ensures better mismatches and leaves room for noise. 

9) $FR(R_{UB}) = [UB_{lo}, UB_{hi}]$: Upper forbidden region boundary guarantees $V_{G2}$ output to be high enough for inputs from higher intervals. This ensures better mismatches.

**Interval match mismatch requirements:** The corresponding matching levels $\{V_{DL}\}$ must be restricted within values $[LB, UB] = [LB_{io}, UB_{io}]$. This results in low enough $V_{G1}$ and $V_{G2}$ such that the switches are off and the defined matching interval is associated with large $R_{on}$ for a given matched cell. As such, we define the discrete level, $D$, associated with a given pair $(R_{LB}, R_{UB})$ for a given cell to be according to:

$$D = \frac{LB_{lo} + UB_{lo}}{2}$$  \hfill (3)

We also have forbidden regions, as defined in items (8) and (9) above, surrounding a given predefined interval $[LB_i, UB_i]$. No other interval can start within those forbidden regions. Hence, with this requirement for given input $D_j$, ($j \neq i$), the cell is guaranteed to operate in strong mismatch state. As such, the forbidden regions for a given cell encompass the $V_{DL}$ values that result in $V_{G1\text{lo}} < V_{G1\text{hi}} < V_{G1\text{lo}}$. $V_{DL}$ beyond the forbidden regions will result in proper turning on the switches of the cell.

**C. Interval Defining Algorithm**

Depending on the requirements set for $V_{Gi\text{lo}}$ and $V_{Gi\text{hi}}$, the number of feasible intervals within a given range can vary. Relaxed requirements result in increased number of intervals, however, this can be limiting in terms of the array size. In fact, the authors in [8] demonstrate that the aCAM cell can support up to 20 discrete levels for an array of 512x64 columns. They also state that the number of discrete levels will vary based on the size of the array and particularly the number of columns in the arrays.

In what follows, we present an interval defining algorithm as function of $V_{Gi\text{lo}}$ and $V_{Gi\text{hi}}$, that, given a range of memristor values, determines for a given design the maximum number of discrete intervals of width=W that can be stored in an aCAM cell along with their corresponding memristor configurations while maintaining a predefined conservative margin between the intervals to ensure proper operation. This will be used to study and compare the different designs subject to a set of critical performance metrics in terms of latency, leakage, and encode capability as function of the array size. The algorithm can be best defined as follows. It is split into two phases:

1) **Preparatory Phase:** Its objective is to identify for each memristor value a corresponding bound values. These values will be useful in the next phase to determine the intervals. Hence, we first generate the LBS and UBS VTC, i.e. $V_{G1}(R_{LB}, V_{DL})$ and $V_{G2}(R_{UB}, V_{DL})$ curves, by sweeping UB and LB subcircuits for different $R$ and $V_{DL}$ values similar to Fig. [3]. We capture from the VTC curves for each $R_{LB}$ and $R_{UB}$ value the corresponding $LB_{io(hi)}$ and $UB_{io(hi)}$ values. Fig. [11] presents the corresponding plots that demonstrate the trend of the different bounds as function of the memristor values. Hereon, we use two look-up-tables to store the resistance and corresponding bounds as triplets as $LUT_{LB} = \{(R_{LB}, LB_{lo(hi)})\}$ and $LUT_{UB} = \{(R_{UB}, UB_{lo(hi)})\}$. These tables are sorted by the resistance values in decreasing order.
2) Building the intervals Phase:

Algorithm 1 presents the pseudo-code for building the intervals. The basics are as follows. The first interval LB is determined based on the lowest possible lower bound value. For a given LBlo value, the corresponding UBlo is determined based on a predefined interval width W, and the corresponding RLB and RUB values are determined from the LUTs. To determine the next interval, hereon, while guaranteeing that forbidden regions do not intersect with the chosen intervals, Eq. (4b) must hold. For our purposes, we enforced the conservative requirement presented in Eq. (4b) as illustrated in Fig. 12. As such, we derive LBhi for the next interval from UBhi from the previous one. The corresponding LBlo and RLB can be determined accordingly from the LUTs, and UBlo, hi and RUB can be determined as stated earlier:

\[ UB^{(i)}_lo \leq UB^{(i)}_hi, \quad LB^{(i+1)}_hi \leq LB^{(i+1)}_lo \quad (4a) \]
\[ UB^{(i)}_lo = LB^{(i+1)}_hi \quad (4b) \]

The intervals are built in a similar manner for the 8T2M circuit since the UBS does not change. As for the LBS, since the PMOS is an active low device, we exchange LBlo and LBhi so that the matching levels \[ V_{DL} \] are now restricted within values \[ \{ LB, UB \} = \{ LB_hi, UB_lo \} \], and the forbidden region becomes: \[ \{ LB_lo, LB_hi \} \cup \{ UB_lo, UB_hi \} \] as illustrated in Fig. 13. For generic non-symmetrical values for \( V_{G_{lo}} \) and \( V_{G_{hi}} \), we rely on \[ 1 - \frac{V_{G_{lo}}}{V_{DD}}, 1 - \frac{V_{G_{hi}}}{V_{DD}} \].

D. Figure of Merit

In order to have a fair comparison between the different circuits, we define a Figure of Merit, FOM, which is a function of the following three important metrics:

- Latency time, \( T \), which is the sampling time at which we measure the match line voltage \( V_{ML} \).
- Number of desired intervals, \( \kappa \), where \( 2 \leq \kappa \leq \eta \) and \( \eta \) is defined by the algorithm.
- Dynamic Range, \( DR \), is the maximum possible separation between the full match and 1-mismatch cases for one combination of \( (level, N, T) \), as shown in Fig. 14 where \( level \) refers to the defined ranges of \( V_{G_{lo, hi}} \). \( N \) represents the number of cells per row. The dynamic range measurements accommodate for the multiple stored memristor values for the 6T2M circuit.

![Fig. 11. The different bounds plotted as function of the corresponding memristor values for the 6T2M circuit.](image)

![Algorithm 1: Interval building pseudo-code](image)

![Fig. 12. Interval building relies on the lookup tables and forbidden regions to identify the next interval.](image)
Hence, to find the DR for all possible intervals \( \eta \), we proceed as follows. A cell storing value \( D_i \) will result in a match when the input is \( D_i \) and a mismatch at all other input states \( \{ D_j \} \), \( j \neq i \) values where \( i, j \in [1, \eta] \). For each \( D_i \), we measure the ML value for the full-match case, \( V_{fm_i} \). For the 1-mismatch case, we choose the closest \( D_j \) values. Hence, we measure ML for two scenarios: a lower bound mismatch case, \( V_{LBmm_i} \), where the mismatch cell is storing \( D_j \) at \( j = i - 1 \), and an upper bound mismatching cell case, \( V_{UBmm_i} \), where the mismatch cell is storing \( D_j \) at \( j = i + 1 \). Assuming that a full-match maintains ML high, the dynamic range can be defined as follows:

\[
DR = \min\{\{V_{fm}\}\} - \max\{\{V_{LBmm}\} \cup \{V_{UBmm}\}\}
\]  

(5)

The data was monotonic and for a desired number of intervals \( \kappa \in [2, \eta] \), we relied on a heuristic to find best \( DR_\kappa = \max\{DR\} \) for all possible combinations of \( \kappa \) intervals. Hence, the Figure of Merit (FOM) for a given \( (level, N, \kappa) \) and a desired operating range for the sampling time \( T \) is defined as follows:

\[
FOM(level, N, \kappa) = \frac{\max\{DR_\kappa\}}{T}
\]  

(6)

E. Variability Considerations

For a given cell with a targeted \( R_{LB} \) and \( R_{UB} \) pair, the lower bound and upper bound will vary in the presence of process variations, and accordingly, the same cell with the same \( R \) will behave differently. Thus, in this section, our objective is to evaluate the impact of process variations on the intervals and the overall performance of the design. For the different cell instances with the same \( R \) values to match, we need to compensate for the variability in the interval building by an additional guard band. To do so, we redefined the lower and upper bounds to include variability based marginalizing as shown in Fig. 15.

For purposes of illustration, we rely here on the most conservative 3 sigma bounds. We later generalize and test the performance when guarding for less conservative bounds of the general form of \( \pm m\sigma \), where the multiplier \( m \in [0; 3] \). In the new marginalization, each \( R_{LB} \) is associated with a range of values for \( LB_{lo} \) between \( LB_{lo}^{m\sigma} \) and \( LB_{hi}^{m\sigma} \) where

\[
LB_{lo}^{m\sigma} = \mu_{LB_{lo}} + m\sigma_{LB_{lo}}
\]

and the mean and standard deviation, \( \mu_{LB_{lo}} \) and \( \sigma_{LB_{lo}} \), of \( LB_{lo} \) are obtained from Monte Carlo simulations on the lower bound circuit for the targeted response low voltage level, \( V_{Gllo} \). The same applies for \( LB_{hi}^{m\sigma} \). Similarly, each \( R_{UB} \) is associated with a value for \( UB_{lo}^{m\sigma} \) and \( UB_{hi}^{m\sigma} \) that are derived in a similar fashion using Monte Carlo simulations. Thus, according to Table IV, we get the new interval bounds as: \( \{LB_{lo}^{m\sigma}, UB_{lo}^{m\sigma}\} \).

The interval building code in Algorithm 1 will search for the next resistor using the newly derived curves \( \{ (R_{LB}, LB_{lo}^{m\sigma}), (R_{LB}, LB_{hi}^{m\sigma}), (R_{UB}, UB_{lo}^{m\sigma}), (R_{UB}, UB_{hi}^{m\sigma}) \} \), to obtain the desired intervals.

V. RESULTS AND ANALYSIS

In this section, we perform a comparative analysis of the 10T2M, 8T2M, and 4T2M2S designs in terms of the FOM analysis, energy, dynamic range, latency, and variability implications.

A. Experimental Setup

We performed our simulations in HSPICE. We relied on predictive technology models for 45nm high-k/metal gate CMOS devices [20] to study the design metrics and build the different LUTs. Similar to the assumptions in [8], we set the transistor threshold voltage \( V_{th} = 0.4V \). We also set \( V_{DD} = 0.8V \). We used the threshold switching model
described in [21]. To derive the intervals and dynamic ranges, we implemented our algorithms using MATLAB [22]. For our designs, we assumed Redox based devices [8]; hence, the aCAM comprised of 1T1R branches with a resistance range for $R_{LB/UB} \in [5K\Omega, 2.5M\Omega]$. For our simulations, we adopted a linear memristor model, similar to [8], [23], because we are only reading and not programming the devices in our experiments. The design space parameters are set as follows. For DC sweeps to develop the LUTs, we set $V_{DL} \in [0.1, V_{DD}]$. For building the intervals, we set the interval width $W = 10mV$. We also set $N \in \{16, 32, 64\}$. Finally, we examined the interval building capabilities at different levels of $[V_{Glo}, V_{Ghi}] = V_{DD}*[p_{lo}, p_{hi}]$ values. For the 10T2M and 8T2M designs, we chose $p_{lo} - p_{hi} = 10 - 90\%$ to represent strong operation for match and mismatch, $10 - 50\%$ to represent strong match and slow mismatch. Intermediate levels such as $30 - 70\%$ and $40 - 60\%$ represent weaker match and mismatch but increased number of intervals. For the 4T2M2S, we opted for tighter ranges $40 - 60\%, 45 - 55\%, 48 - 52\%$ and $49 - 51\%$ due to the steep subthreshold swing of the TS switch.

### B. FOM

For different applications, the necessary number of intervals will differ, so we studied the $FOM$ for different $\kappa$, $N$, and level values for the different circuits. $T = [0.5-10]ns$ for the 10T2M design, 8T2M circuit, and the 4T2M2S design. Note, that for the 4T2M2S, the DR improved for larger sampling time but this had implications on the figure of merit. In fact, both the 10T2M and the 8T2M provide better DR results at reasonably small sampling times (less than $1ns$), unlike the 4T2M2S design which yields wider DR at higher time. As such, we report for each pair $(N, \kappa)$ and level the corresponding $FOM$ values as illustrated in Fig. 17 for the different cells.

As we can see, there is a trade-off for the three designs between the $FOM$ and $\kappa$. This is attributed to the fact that larger $\kappa$ are subject to more ML costraints as illustrated in Fig. 14 and hence typically result in lower DRs. The overall pool of intervals to choose amongst is also affected by the level chosen to operate at. For instance, stricter level ranges such as the $10 - 90\%$ and the $10 - 50\%$ for the 10T2M and 8T2M designs and the $40 - 60\%$ and $45 - 55\%$ for the 4T2M2S design provide higher DR at the cost of less number of intervals. Relaxed levels, however, result in lower DR values but yield more intervals. For example, 31 intervals are attainable for the 4T2M2S design for the level $49 - 51\%$. Finally, it is worth noting, 4T2M2S uses the low gain LB and UB circuits, and thus it has lower number of intervals at $40 - 60\%$ compared to the other two designs, however, due to the fact that the TS has high subthreshold swing, we can further push operation to tighter level ranges and attain higher number of intervals.

### C. Variability Analysis

To account for the implications of variability, we apply process variations to the device threshold voltages, such that the NMOS devices are subject to $3\sigma_{vt}$ of $\sim 50mV$ variation. We scale the PMOS device threshold voltage variations according to the device widths. We generated the intervals for $m \in [1; 3]$ mimicking tight and relaxed margin constraints. For each $m$ value, we performed 1000 Monte Carlo SPICE simulations for
the different cells subject to random variations. Fig. [16] shows the maximum number of achievable intervals $\eta$ that we can get for different design levels for the three circuits as we vary the multiplier $m$. It is clear that as we move towards the more conservative scenarios (more guarding against failure), we obtain fewer intervals. In general, the 4T2M2S design yields the highest number of intervals. In the following section, we introduce a summary table where we comment on the overall performance of the three designs and compare the implications of variability on the probability of fail.

D. Corner Analysis

Aside from random variations, we also explore the impact of the corner analysis on the different designs. We thus studied five corners where the threshold voltages of NMOS and PMOS transistors were skewed by \( \pm 10\% \). For purposes of our results, TT refers to the typical corners, SF refers to slow NMOS and Fast PMOS and so on. Our simulations show a slight change of \( \pm 2 \) intervals in the number of intervals for a given cell at different corners as illustrated in Table [V] for \( 40-60\% \) margins. Other design margins results are reported in the Supplementary Tables I, II, and III, with the FS corner yielding the highest number of intervals and depending on the level the SF offering the lowest number of intervals.

E. Comparative Analysis

Table [VI] summarizes the results for the three cell designs using 45nm PTM. We chose the level \( 40 - 60\% \) as the basis of our comparisons since it is common among the three circuits, and we set the number of cells per row to 16. To properly assess the designs, we evaluated each of the following metrics subject to a fixed set of constraints. Thus, for purposes of the dynamic range comparisons, we fixed the time at which we read $V_{ML}$ to \( 1ns \), and the number of intervals equal to $\kappa = 3$, and we reported the best dynamic range for each design. For the latency, we also set $\kappa = 3$, and we identified it as the smallest time at which we achieve a DR of \( 100mV \). As for the energy dissipation, we fixed the evaluation time to \( 1ns \) and reported the average energy for the full mismatch case, while choosing the three intervals that give the best DR for each design.

For the 10T2M and the 8T2M circuits, the energy comprises pre-charge and evaluate energies, with the evaluate energy being mainly driven by the voltage-divider circuits of the resistor-based inverters. For the 4T2M2S, the dissipated energy comprises the evaluate energy that is mainly composed of the voltage dividers’ energy and the energy needed to charge the ML upon mismatch. A more detailed energy analysis showing the full match, one lower bound mismatch, and full mismatch energies for each of the three intervals is present in Supplementary Tables IV, V, and VI. We note that the energy consumption rises as the memristance values decrease due to more leakages for the voltage divider circuits. For the same resistance range, the compare energy is almost the same for the different designs. For the intervals that provided the maximum dynamic range, the 8T2M followed by the 10T2M consumed lower energies compared to the 4T2M2S. The same experiments were repeated using 65nm TSMC technology [24], and similar trends were reported as illustrated in Supplementary Table XIV. As for the area, Table VI presents the estimated active area for the different designs. The 10T2M consumes most area with 4T2M2S requiring additional area due to the presence of the switches. The details of the area estimation are presented in Supplementary Section 5.

In order to assess impact of variability on the different designs, we study their respective failure probabilities. For each design, we choose the maximum multiplier value that results in 3 intervals ($m = 2.5$ for the 10T2M circuit, $m = 2$ for the 8T2M circuit, and $m = 1.5$ for the 4T2M2S circuit). Here, we fixed $T = 0.5ns$. To estimate the failure probability, we performed 1000 Monte Carlo SPICE simulations for a row of 16 aCAM cells subject to threshold voltage variations with $3\sigma_{vt}$ of 50mV. We measured $V_{ML}$ for fm, 1LBmm and 1UBmm cases for the different intervals for each Monte Carlo run. Then, we identified the best reference voltage value $V_{ref}$ that provides the best separation between the match and mismatch scenarios in the presence of variability. For the 10T2M and 8T2M designs, we counted a simulation with a match value that is below $V_{ref}$ as a match fail, and a simulation with a mismatch value that is above $V_{ref}$ as a mismatch fail. The opposite holds for the 4T2M2S circuit. We defined the failure probability based on the number of match and mismatch fails obtained from the simulations for all the intervals. Supplementary Tables VII, VIII, and IX show the fail probabilities at different sampling times for the 10T2M, 8T2M, and 4T2M2S aCAM designs, respectively. Table [VI] presents the fail probabilities for the three designs at the 40-60% level and $T=0.5ns$; $V_{ref}$ = 100, 408 and 123mV for the 10T2M, 8T2M and 4T2M2S designs, respectively.

As far as the specific metrics studied in Table [VI] overall, we observe that the 10T2M stands as a viable solution as applicable to the specified metrics combined in terms of BER, DR, latency and energy. The 8T2M maintained the lowest energy consumption, and best latency with a good BER. We
channel resistance of transistor is divided into $M$ partitions, each having parasitic interconnect parasitics, where the row (column) interconnect resistance values depend on data presented in Supplementary Reference [4] and [23]. Without loss of generality, we performed a thorough analysis on the impact of these assumptions on the 10T2M cell for all the different levels and $m$ values. Supplementary Table X presents these results in terms of the number of intervals and $P_f$. We note that with the application of the proposed algorithms, we only noted a slight impact on the results in the presence of this variability.

**G. Impact of Array Parasitics and Signal Timing**

The latency simulations in Table VI did not fully incorporate the array interconnect parasitics. Herein, we study the effect of the array size on the performance of the aCAM in the presence of parasitic effects. As such, we considered the 10T2M, 8T2M and 4T2M2S aCAM array with different numbers of rows and columns, and replicated the latency analysis for the specific sets of three intervals studied in Table VI, targeting the cells maintaining a dynamic range of partitions involved for a specific cell depends on the cell location (row number and column number). As discussed in Supplementary Note 9, the effect of row parasitics becomes negligible when we set the proper timing requirements for the early arrival of signal $V_{DL}$ as recommended in [8] for the 6T2M cell. As such, we take into consideration the array parasitic effects and accommodate for an early arrival of $V_{DL}$ signal to compensate for the delay of the parasitic network. We set $V_{DL}$ to arrive earlier than $V_{SLhi}$ by $5\tau$, where $\tau$ represents the expected RC time constant of the interconnect network feeding $V_{DL}$ to the inputs of the aCAM cell. Table VII presents the summary of the latency simulations for the farthest row ($N=512$ in this example) as function of the number of columns.

Furthermore, we studied the impact of parasitics, $r = 1\Omega$ and $c = 1fF$, on the response of the cell as function of the farthest row in a 4T2M2S aCAM array with two columns. We swept $V_{DL}$ and studied $V_{ML}$ response with respect to the input $V_{DL}$, measured at 4ns. We varied the number of rows $N \in \{8, 16, 32, 64, 128, 256, 512\}$. Without loss of generality, the cells have a match interval $[LB, UB] = [0.37, 0.47][V]$, corresponding to resistances $[R_{LB}, R_{UB}] = [112.7, 20.9][k\Omega]$. By setting $V_{DL}$ to arrive earlier than $V_{SLhi}$ by $5\tau$, ML evaluates properly for up to 512 rows, as illustrated in Fig. 18. In addition, Supplementary Figure 7 analyzes the impact of $V_{DL}$ timing with respect to $V_{SLhi}$ on the ML response.

**VI. CONCLUSIONS**

In this paper, we proposed two new analog CAM cell designs, the 10T2M and the 8T2M circuits, in an attempt to improve the functionality of the aCAM. We developed the algorithms needed for interval building and Figure of Merit analysis. We performed a comprehensive comparison amongst three different aCAM cell designs: the 10T2M, the 8T2M, and the 4T2M2S aCAM cells and explored the improvements in the gain in comparison to previous work in [8]. We also studied...
the behavior of the aCAM with variability considerations. The different designs were assessed in terms of key metrics such as the dynamic range, latency, energy, area, maximum number of intervals, and fail probability. The obtained results show a trade-off among the three designs for the different metrics. As such, depending on the desired application, an appropriate aCAM cell design should be adopted.

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