Abstract—Polar codes have been selected as the channel coding scheme for control channel in the fifth generation (5G) communication system thanks to their capacity achieving characteristics. However, the traditional polar codes support only codes constructed by binary $(2 \times 2)$ kernel which limits the code lengths to powers of 2. Multi-kernel polar codes are proposed to achieve flexible block length. In this paper, the first combinational decoder for multi-kernel polar codes based on successive cancellation algorithm is proposed. The proposed decoder can decode pure-binary and binary-ternary $(3 \times 3)$ mixed polar codes. The architecture is rate-flexible with the capability of online rate assignment and supports any kernel sequences. The FPGA implementation results reveal that for a code of length $N = 48$, the coded throughput of 812.1 Mbps can be achieved.

Index Terms—Polar code, successive cancellation decoder, multi-kernel, error correcting codes, hardware implementation.

I. INTRODUCTION

POLAR codes have been subjected to growing attention due to their capability to achieve symmetric channel capacity of binary-input discrete memoryless channels at infinite code length $[1]–[3]$. During the last decade, researchers have extensively improved polar codes in terms of error-correction performance for finite-length codes, decoding latency under successive cancellation (SC) algorithm, complexity and power. This effort paved the way for polar codes to be adapted in the 3GPP fifth generation new radio (5G-NR) wireless communication standard [4].

However, the majority of current research works have concentrated on polar codes constructed by binary kernels $(2 \times 2$ polarization matrix) also known as Arikan’s kernel [1]. The lengths of polar codes are therefore restricted to powers of 2. The 5G framework demands various code lengths and code rates. The rate-matching schemes [5], [6] are proposed to address this limitation. However, a priori performance and optimality evaluation of these methods are hard. Multi-kernel (MK) polar codes $[7]–[9]$ offer flexible code lengths with the same computational complexity as Arikan’s polar codes by employing kernels with variable dimensions. It is shown in [8] that MK polar codes outperform similar codes constructed by puncturing and shortening methods in terms of error-correction performance.

Several architectures have been proposed for decoding Arikan’s polar codes. Recently, an architecture for implementing MK polar codes constructed from binary and ternary $(3 \times 3)$ kernels have been proposed in [10] by adapting the architecture of Arikan’s codes in [11] to MK codes. The work in [12] proposed a MK architecture to reduce the latency of the MK polar codes. However, the coded throughput is not promising. Also, two mentioned MK decoders need different memory interfaces for binary and ternary stages which adds to the complexity of the memory system.

In this paper, we propose an architecture based on the SC algorithm targeting high-throughput MK polar codes with low power consumption. The recursive and feed-forward structure of the SC algorithm makes use of pure combinational logic possible to implement the decoder’s functions. The operation frequency of combinational decoders is lower than that of the sequential counterparts. However, they are capable of decoding an entire codeword in only one clock cycle resulting in considerable reduction in dynamic power with reference to sequential decoders. The proposed architecture features an online rate assignment mechanism for a given block length and it can decode pure-binary and binary-ternary mixed kernels. Since pure-ternary codes generate odd block lengths, they are out of our interest. An FPGA implementation is conducted to validate the architecture and the results are compared to the state-of-the-art MK decoders.

The remainder of this paper is organized as follows. A background on polar codes is presented in section II. Section III details the code construction method, the proposed decoder’s architecture and complexity analysis. The implementation results and comparison to previous works are summarized in section IV. Finally, section V concludes this work.

II. POLAR CODES

A polar code of length $N$ carrying $K$ bits of information is denoted by $PC(N, K)$ and the code rate is computed as $R = \frac{K}{N}$. The set of $K$ information bits are called information set $(I)$ and the set of remaining $N - K$ bits are called frozen set $(F)$ which are set to 0. Arikan proposed channel polarization phenomenon [1] to transform the physical channel $W$ into $N$ individual virtual channels $W_{i}^{N} (1 \leq i \leq N)$ with relative increased or decreased reliabilities. The reliability of each channel approaches either 0 (completely unreliable) or 1 (completely reliable) as the code lengths approaches infinity. The individual reliable channels can be designated by Bhattacharya parameters [1].

A binary polar code can be constructed through a linear transformation expressed as $x = uG$. Here $x$ is the encoded stream, $u$ is a N-bit input vector to the encoder constructed by message and frozen data placement into reliable and...
unreliable positions, respectively. Finally, $G = T_2^2 \otimes \ldots \otimes T_2^n$ is the binary generator matrix constructed by the $n$-th Kronecker product of Arikan’s kernel $T_2 = [1 \ 1 \ 0 \ 1]$. Obviously, $G$ is defined in a recursive way where a binary polar code of length $N$ is generated by concatenating two codes of length $N/2$.

### A. MK Polar Codes

Utilizing $T_2$ as the generator matrix bounds the block lengths of polar codes to powers of 2. However, using the LDPC WiMax codestrengths [13] as guideline reveals that the code lengths constructed by non-binary kernels are needed. Most of the desired code lengths can be obtained using only one or few non-binary kernels. In order to construct a block code as $N = n_0 \times n_1 \times \ldots \times n_k$ with $n_i$s being not necessarily individual prime numbers, a series of Kronecker products between different kernels can form the generator matrix as $G \triangleq T_{n_0} \otimes T_{n_1} \otimes \ldots \otimes T_{n_k}$, where $T_{n_i}$s are squared matrices.

Each distinctive prime number can be considered as a kernel, however the least complete and most practical kernels are binary and ternary (defined as $T_3 = [1 \ 0 \ 1 \ 0 \ 1 \ 1 \ 8]$) kernels. It is shown in [14] that $T_3$ offers polarization optimality, although it has a lower polarization exponent than $T_2$. In this paper, we investigate codes constructed by pure-binary and any combination of binary and ternary kernels. The pure-ternary kernels are not of our interest since they generate an odd block length.

The block length and the generator matrix for the polar codes presented in this paper can be formulated as $N = 2^{n_1} \cdot 3^{n_2}$ and $G = \otimes_{i=0}^{n_2} T_k$, where $n, m \in \mathbb{N}$. Defining the number of terms in the generator matrix as $M = m + n$ with $M \in [1, 10]$, the increased length flexibility offered by MK polar codes is outlined in Table I. The bold values indicate codes with possible use cases in $5G$ polar codes.

| $N$ | 2 | 4 | 8 | 16 | 32 | 64 | 128 | 256 | 512 | 1024 |
|-----|---|---|---|----|----|----|-----|-----|-----|------|
| 2   | 4 | 8 | 16 | 32 | 64 | 128 | 256 | 512 | 1024 |
| 3   | 6 | 12 | 24 | 48 | 96 | 192 | 384 | 768 | 1536 |
| 9   | 18 | 36 | 72 | 144 | 288 | 576 | 1152 | 2304 |
| 27  | 54 | 108 | 216 | 432 | 864 | 1728 | 3456 |
| 81  | 162 | 324 | 648 | 1296 | 2592 | 5184 |
| 243 | 486 | 972 | 1944 | 3888 | 7776 |
| 729 | 1458 | 2916 | 5832 | 11664 |
| 2187 | 4374 | 8748 | 17496 |
| 6561 | 13122 | 26244 |
| 19682 | 39366 |
| 59048 |

Table I: List of block lengths attainable by MK codes using $T_2$, $T_3$.

#### B. MK Successive-Cancellation Decoding

Arikan [11] proposed the SC algorithm to decode polar codes. MK polar codes can be decoded using the same algorithm. Fig. 2(b) depicts the decoder tree corresponding to the Tanner graph of Fig. 1(a). The channel’s soft information $(\alpha_{\nu})$ called log-likelihood ratios (LLRs) enter the tree from the root. To estimate a codeword, the soft information needs to propagate to the tree and visit all the leaves in a sequential way with the condition of visiting the left node first. Three functions are needed to traverse the tree. For a given binary node $\nu$, $\alpha_{\nu i}$ is the function required to travel to the left branch which can be estimated as

$$
\alpha^b_{\nu i}[i] = sgn(\alpha_{\nu i}[i], \alpha_{\nu i}[i + 2(\lambda - 1)]) \min(|\alpha_{\nu i}[i]|, |\alpha_{\nu i}[i + 2(\lambda - 1)]|)
$$

where $i \in \{0 \div 2(\lambda - 1) - 1\}$. The node $\nu$ can compute the LLR vector to be sent to the right branch when the hard decisions $(\beta^b_{\nu i})$ from the left branch are available.

$$
\alpha^b_{\nu i}[i] = (1 - 2\beta^b_{\nu i}[i]) \alpha_{\nu i}[2i] + \alpha_{\nu i}[2i + 1] \text{ for } i \in \{0 \div 2(\lambda - 1) - 1\}
$$

where $\beta^b_{\nu i}$ is the LLR of the right branch. The codeword at node $\nu$ called $\beta^b$ can be generated by combining at node $\nu$ when the hard decision bits of the right branch are available.

$$
[\beta^b_{\nu i}], [\beta^b_{\nu i + 2(\lambda - 1)}] = [\beta^b_{\nu i} \oplus \beta^b_{\nu i + 2(\lambda - 1)}], [\beta^b_{\nu i}], [\beta^b_{\nu i + 2(\lambda - 1)}], [\beta^b_{\nu i + 2(\lambda - 1)}].
$$

The hard decisions on a leaf node can be estimated as

$$
\beta_v = \begin{cases} h(\alpha_v), & \text{if } v \in I, \\ 0, & \text{if } v \notin I, \text{ and } h(x) = \begin{cases} 0, & \text{if } x \geq 0, \\ 1, & \text{otherwise}. \end{cases} \end{cases}
$$

We define $f^b$, $g^b$ and $C^b$, respectively, as shown in Fig. 1(b). The message passing criterion for a ternary node needs defining four functions. For a given node $\nu$ located at level $\lambda$ in a pure-ternary polar code, the decoding functions for traveling to the left, middle and right branches are shown by $\alpha_{\nu l}$, $\alpha_{\nu m}$ and $\alpha_{\nu r}$, respectively. For $i \in \{0 \div 3\lambda - 1\}$ the $\alpha_{\nu i}$ is calculated as

$$
\alpha^l_{\nu i}[i] = sgn(\alpha_{\nu i}[i], \alpha_{\nu i}[i + 2(\lambda - 1)], \alpha_{\nu i}[i + 2\lambda]) \min(|\alpha_{\nu i}[i]|, |\alpha_{\nu i}[i + 2(\lambda - 1)]|, |\alpha_{\nu i}[i + 2\lambda]|).
$$

When the hard decisions from the left branch $(\beta^b_{\nu l})$ are computed, the LLRs can be proceed to the middle branch by

$$
\alpha^m_{\nu i}[i] = (1 - 2\beta^b_{\nu i}[i]) \alpha[i] + f^b(\alpha[i + 2(\lambda - 1)] + \alpha[i + 2\lambda])
$$

Fig. 1. a) Encoder graph and b) decoder tree of a MK polar code of size $N = 6$ with $G = T_2 \otimes T_3$. 

![Decoder Tree Example](image-url)
Finally, having $\beta^t_{\nu}$ and hard decisions from the middle branch ($\beta^t_{v_t}$), the LLR vector can travel to the right branch using

$$\alpha_{v_r}[i] = (1-2\beta^t_{v_t}[i])\alpha[i+2^{(\lambda-1)}] + (1-2\beta^t_{v_t}[i] \otimes \beta^t_{v_r}[i])\alpha[i+2^{\lambda}] .$$

The hard decisions at node $\nu$ can be combined as

$$[\beta^t_{i}, \beta^t_{i+2^{(\lambda-1)}}, \beta^t_{i+2^{\lambda}}] = [\beta^{pt}_i \oplus \beta^{pt}_i, \beta^{pt}_i \oplus \beta^{pt}_i, \beta^{pt}_i \oplus \beta^{pt}_i] .$$

As illustrated in Fig. 1(b), we define (5), (6), (7) and (8) as $f^t$, $g^t_1$, $g^t_2$ and $C^t$, respectively. Finally, a binary sign function ($s(x)$) and a frozen bit indicator vector ($a$) will be used in the following sections which are defined as

$$s(x) = \begin{cases} 0, & \text{if } g \geq 0, \\ 1, & \text{otherwise} \end{cases}, \quad a_i = \begin{cases} 0, & \text{if } i \in F, \\ 1, & \text{if } i \in Z. \end{cases}$$

III. MK codes: Construction and Architecture

A. Code Construction

In this paper, we use the method proposed in [8] since it yields substantial error-correction performance compared to puncturing [15] and shortening [16] methods. Fig. 2 plots the error-correction performance of MK polar code of $PC(72, 36)$ with $G = T_2 \otimes T_2 \otimes T_2 \otimes T_3$. Obviously, it considerably outperforms punctured and shortened codes constructed by a mother code of $N' = 128$. The MK codes can be constructed by arbitrary kernel orders. However, they feature different error-correction performances since the Kronecker product is not commutative. Presently, no theoretical way is identified to find the best kernel order and simulations need to be conducted to find the kernel order with the best error-correction performance. In this paper, we use the method proposed in [9] to obtain the kernel orders. We use the LDPC WiMAX code lengths [13] as our guideline which suggests that the desired MK block lengths can be obtained by employing a few non-binary kernels. Thus we focus on MK codes constructed by only one ternary kernel. This is also important in terms of hardware complexity analysis as will be explained in the following sections. The error-correction performance of such codes with block lengths lower than 1024 is illustrated in Fig. [3]

The complexity of MK decoding is lower than that of the puncturing and shortening methods. This is due to the fact that MK polar codes employ a smaller Tanner graph with respect to puncturing and shortening methods which use a mother code of size $N' = 2^{[\log_2 N]}$ which determines the code’s complexity. The overall number of LLR computations can be defined as a complexity metric for the sake of comparison. Let $s$ be the number of stages in the code’s Tanner graph which is identical to the number of kernels used in the code construction. The complexity metric of MK and puncturing/shortening methods can be calculated as $N \times s$ and $N'^{\log_2 N'}$, respectively. Fig. 4 illustrates the complexity reduction of MK method with respect to puncturing and shortening methods for various code lengths. It can be seen that reported MK codes offer at least 32.5% lower LLR computational complexity with respect to punctured/shortened codes.

B. Proposed Decoder Architecture

The SC decoder can be implemented by purely combinational logic since no loops are included in the algorithm. Therefore, there are no memory elements between the input and output stages. The main objective of combinational implementation is to achieve a high throughput. In this section, we first explain the implementation method of belief propagation functions. Then the overall architecture of the proposed mixed-kernel polar codes will be detailed.

1) Belief Propagation functions: To implement the combinational functions, $Q$ bits are used to represent the channel observation LLRs in sign-magnitude representation (similar to [17] and [18]) to prevent conversions between different representations. The $f^b$ and $f^t$ functions can be directly implemented by (4) and (5), respectively, using comparators and multiplexers. The precomputation method in [19] is used to implement the $g^b$, $g^t_1$ and $g^t_2$ functions.
Fig. 4. The complexity gain of MK method versus puncturing and shortening method using the defined complexity metric.

The decision logic serves as the basic building block of the decoder. Using the construction method in [9], we observed that all codes of this paper’s interest has no ternary kernel located at stage zero ($s = 0$ in Fig. 1(b)). Therefore, there is no need to use a ternary kernel in the decision logic considering the fact that they consume considerable resources. Thus we can use the method proposed in [17] to estimate the binary odd-indexed leaves as

$$
\hat{u}_{2i+1} = \begin{cases} 
0 & \text{if } a_{2i+1} = 0, \\
\lambda_1 & \text{if } a_{2i+1} = 1 \text{ and } |\lambda_1| \geq |\lambda_0| \\
\lambda_0 \oplus \hat{u}_{2i} & \text{otherwise,} 
\end{cases}
$$

(10)

where $\lambda_0$ and $\lambda_1$ are the input LLRs to the $g^b$ function.

2) Overall architecture: In this section, we first present an improved architecture for the Arikan’s combinational decoder proposed in [17]. Then an SC decoding architecture for mixed-kernel polar codes will be proposed. Fig. 5 illustrates the generalized improved combinational architecture of a decoder of size $N$ constructed by Arikan’s kernels based on the conventional architecture proposed in [17]. In the conventional architecture, a decoder of size $N = 4$ is used as the basic building block. However, we use a decoder of size $N = 2$ to increase the code length flexibility. The modified decoder is constructed by two Arikan’s decoders of size $N/2$ glued by one $f^b$, one $g^b$, and one combine logic of size $N/2$. The combine logic of size $N/2$ is used to substitute the encoder of size $N/2$ in the conventional architecture. This modification leads to significantly decreasing the number of XOR gates. For instance, for a polar code of size $N = 32$, the number of XOR gates is decreased by $42.3\%$.

The proposed combinational architecture of a ternary stage of a MK polar code of size $N$ is depicted in Fig. 6. It is composed of three decoders of size $N/3$ and one $f^b$, one $g^b_1$, one $g^b_2$, and two combine logics of size $N/3$ as the glue logic. The basic building block in this case is also a decoder of size $N = 2$.

As a result of recursive structure of the SC algorithm, the architecture of a MK decoder of size $N = 6$ can be constructed by two combinational decoders of size $N = 2$ and $N = 3$. The last kernel which is used for polarizing the nodes located at stage zero ($s = 0$ in Fig. 1(b)) known as decision logic serves as the basic building block of the MK decoder. Fig. 7 portrays a mixed-kernel architecture for a polar code of size $N = 6$ with $G = T_3 \otimes T_2$. Registers are not shown here to prevent congestion. Since the last kernel in the kernel sequence is $T_2$, a binary decision making circuitry is used as the basic building block of this decoder. Given $T_3$ as the next kernel, the glue logic includes two binary combine logics ($C^b$), one $f^b$, one $g^b_1$ and one $g^b_2$. In order to get the codeword estimate at the root of the tree, we use a ternary combine function ($C^t$).
Solving the recursion equation of (12) gives $g^c = \text{number of comparators (method in [9] suggests for the majority of such codes. The number is located at the root of the Tanner graph as the construction}

The Arikan’s and proposed combinational architectures consume $N \times (Q + 2)$ register bits to store the input LLRs ($N \times Q$), estimated codeword ($N$) and frozen pattern bits ($N$). As it is shown in Fig. 5, Fig. 6 and Fig. 7, no synchronous logic elements (registers or RAM) are integrated between the input and output registers in the combinational decoders. This feature results in power efficiency and saving processing time. The hardware complexity is also decreased by removing the RAM routers and in result lowering the long read/write latencies. The decoder has one clock cycle latency since it generates the decision vector one clock after receiving the input LLRs. The critical path is equal to the delay of the logic between the input and output registers.

**C. Hardware Complexity Analysis**

In this section, the complexity of the proposed architecture will be investigated. It is shown in [17] that the total number of basic building blocks of a combinational Arikan’s decoder of size $N$ can be computed as

$$c^b_N + s^b_N + r^b_N = N(\frac{3}{2}(\log_2 N) - 1) \approx N\log_2 N,$$  \hspace{1cm} (11)$$

where $c^b_N$ and $s^b_N$ denote the number of comparators used in implementing $f^b$ and the decision logic, respectively, and $r^b_N$ represents the total number of adders and subtractors used in implementing $g^b$. A general complexity analysis of MK codes is not possible since it depends on the number and location of different kernels in the kernel sequence. However, in this paper we calculate the complexity of MK codes with only one ternary kernel since they construct the most important block lengths. We assume the most complex scenario where the ternary kernel is located at the root of the Tanner graph as the construction method in [9] suggests for the majority of such codes. The number of comparators ($c^M^K_N$) used for implementing $f^t$ and $g^t_1$ equals $c^M^K = N$. Therefore, a decoder of size $N$ has the recursive relationship of

$$c^M^K_N = 3c^M^K_{N-1} + N = 3(2c^M^K_{N-2} + \frac{N}{6}) + N = ...$$  \hspace{1cm} (12)$$

Solving the recursion equation of (12) gives

$$c^M^K_N = N(\log_2 N - 4.17).$$  \hspace{1cm} (13)$$

The number of comparators used in the decision logic for $N = 2$ is $s^b_2 = 1$. Thus we can calculate the number of comparators in decision logic for MK case as $s^M^K_N = \frac{N}{2}$. Finally, the total number of adders and subtractors ($r^M^K_N$) can be computed as

$$r^M^K_N = 6c^M^K_{N-1} + \frac{4}{3}N = N(log_2 N - 1.25).$$  \hspace{1cm} (14)$$

Thus the number of basic logic blocks of the MK decoder can be estimated as

$$c^M^K_N + s^M^K_N + r^M^K_N = N(2\log_2 N - 4.92) \approx N\log_2 N.$$  \hspace{1cm} (15)$$

Which shows that the decoder’s complexity is roughly $N\log_2 N$.

**IV. IMPLEMENTATION RESULTS AND ANALYSIS**

All polar codes of this paper are implemented by VHDL coding in Xilinx Vivado 2019.1 environment. Logic synthesis, technology mapping, and place and route are preformed to validate the design. Random codewords are generated by a software program and then transferred to the decoder. We use $Q = 5$ bits to quantize the LLRs. Fig. 8 illustrates that the quantization performance loss is negligible for $PC(192,96)$.

**A. FPGA Utilization**

The FPGA utilization of the proposed MK decoders of size $N = 48$ and $N = 64$ along with that of a decoder of size $N = 64$ proposed in [17] are reported in Table II. Comparing to [17], the proposed decoder consumes 29.3% lower LUTs. This is due to the modifications on the encoding circuitry in sub-decoders which results in using substantially lower XOR gates. The registers are mainly used for small logic circuits and fetching the RAM outputs. The proposed decoder consumes 5.8% higher registers. This difference stems from register duplication to address the target clock frequency. Finally, both decoders consume the same amount of RAM since $N \times (Q+2)$ bits of RAM are needed.

**B. Throughput**

The coded throughput of MK polar codes can be calculated as $T_c = N \cdot f$ similar to the binary case. The flexibility and scalability of the proposed decoder is evaluated by implementing different codes with different kernel orders. The coded throughput of various polar codes under different conditions are summarized in Table III. It can be observed that the proposed MK polar code of size $N = 48$ achieves 22, 4% higher coded throughput with respect to combinational shortend code of the same size constructed by a mother code of $N' = 64$. Comparing to [10], our proposed MK decoder

**TABLE II**

| Decoder | Block Length | Kernel Order | LUTs | Registers | RAM (bits) |
|---------|--------------|--------------|------|-----------|------------|
| This work | 48 | {3, 2, 2, 2, 2} | 2385 | 387 | 336 |
| This work | 64 | {2, 2, 2, 2, 2, 2} | 3626 | 415 | 448 |
| [17] | 64 | {2, 2, 2, 2, 2, 2} | 5126 | 392 | 448 |

*Fig. 7. The combinational MK polar decoder for $N = 6$ and $G = T_3 \otimes T_2$.***
increases the throughput by 88.5% for a polar code of length $N = 48$. The coded throughput of the proposed MK decoder of size $N = 64$ gains 4% higher throughput with respect to its Arikan’s counterpart in [17].

V. CONCLUSION

A combinatorial MK polar decoder with high-throughput has been implemented on FPGA. The proposed architecture offers flexible code rate. A complexity analysis is conducted and FPGA utilization for the target block lengths is reported. The implementation results reveal that the proposed architecture achieves the coded throughput of 812.1 Mbps for a code of size $N = 48$.

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TABLE III

CODED THROUGHPUT COMPARISON OF VARIOUS POLAR CODES

| Length | Block | 48   | 64   | 64   |
|--------|-------|------|------|------|
| MK     | (MK)  | 812.1| 663.45| 884.6| 850.7|
| MK short. | (Arikan) | 850.7| 850.7| 850.7| 850.7|

Fig. 8. The error-correction performance of MK code of PC(192, 96) comparing to puncturing and shortening methods.