**Benchmarking a Probabilistic Coprocessor**

Jan Kaiser, Rishi Jaiswal, Behtash Behin-Aein, and Supriyo Datta

1) Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, 47906 USA
2) Ludwig Computing, 516 Northwestern Ave, West Lafayette, IN, 47906 USA

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Computation in the past decades has been driven by deterministic computers based on classical deterministic bits. Recently, alternative computing paradigms and domain-based computing like quantum computing and probabilistic computing have gained traction. While quantum computers based on q-bits utilize quantum effects to advance computation, probabilistic computers based on probabilistic (p-)bits are naturally suited to solve problems that require large amount of random numbers utilized in Monte Carlo and Markov Chain Monte Carlo algorithms. These Monte Carlo techniques are used to solve important problems in the fields of optimization, numerical integration or sampling from probability distributions. However, to efficiently implement Monte Carlo algorithms the generation of random numbers is crucial. In this paper, we present and benchmark a probabilistic coprocessor based on p-bits that are naturally suited to solve these problems. We present multiple examples and project that a nanomagnetic implementation of our probabilistic coprocessor can outperform classical CPU and GPU implementations by multiple orders of magnitude.

**I. INTRODUCTION**

Due to the slowing down of Moore’s law, unconventional computing approaches that move algorithms closer to physics are of great current interest. One promising field is that of probabilistic computing which has achieved wide spread attention. One form of probabilistic computing inspired by Feynman makes use of a compact probabilistic (p-)bit that can fast and efficiently generate random numbers at a area footprint of only 3 transistors and 1 stochastic magnetic tunnel junction (s-MTJ). In comparison, CMOS alternatives require 1000+ transistors to perform a similar functionality. These p-bits can be utilized to compactly implement new and existing algorithms following Monte Carlo methods. Monte Carlo methods are easy to understand, easy to implement and allow embarrassingly parallel computation. Markov Chain Monte Carlo algorithms are very powerful and have been named as part of the top 10 algorithms of the 20th century. They have the property that the random number generator (RNG) is crucial for the overall computation and can be the bottleneck since other mathematically heavy parts of data processing is readily addressed by with today’s GPUs, resistive crossbars or by pipelining.

In this paper, we propose and benchmark a probabilistic coprocessor that is naturally suited to address a wide range of tasks that require a large amount of random numbers. The architecture is designed to make the most use out of parallel RNG units that could be implemented with stochastic MTJ based p-bits on an integrated chip. For each problem, we emulate the probabilistic coprocessor with a Field Programmable Gate Array (FPGA) and project the performance of an integrated p-computer using a nanomagnetic implementations. We compare the coprocessor with conventional CPU and GPU platforms using state-of-the-art software implementations. We show that the p-computer emulation can achieve 1-3 orders of magnitude improvement when compared to CPU and GPU implementations whereas the projected p-computer can achieve another 2-3 order of magnitude improvement for each problem when compared to the emulation.

The paper is structured as follows. First, we introduce the probabilistic coprocessor architecture and show how it could be implemented in an integrated circuit using MTJ-based p-bits. We then demonstrate the advantage of parallelization on the simple problem of estimating \( \pi \). Then we demonstrate the p-computer on an example of uncertainty classification and Bayesian networks. Consequently, we show that Markov Chain Monte Carlo techniques can be implemented as well and show the performance on the Knapsack optimization problem.

**II. ARCHITECTURE OF THE PROBABILISTIC COPROCESSOR**

The probabilistic coprocessor is shown in Fig. 1 which describes the general architecture that can solve a wide variety of problems that can be address with probabilistic computing. The random number generator (RNG) block is responsible for fast generation of random numbers which could be implemented in an integrated circuit using the 1 s-MTJ and 3 transistor based p-bits (see section II A for more details). The processing of the generated random numbers is performed by the Kernel which will be adapted depending on the problem. The N-bit RNG and Kernel block is copied in order to run multiple operations in parallel. The data processing is pipelined as much as possible in order to make use of fast RNGs. The processed data is collected in the yellow data collector block. We note that for usual computational pipelines the input is dependent on other processes. Here, since

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\(^{a)}\text{Electronic mail: kaiser32@purdue.edu}\)
the input into the pipeline is the RNG, we can make full use of pipelining without waiting for the data processing of other processes to finish. In the methods section, the \textit{p-computer} emulation is described in detail.

![Diagram of Probabilistic Coprocessor](image)

**FIG. 1. Structure of Probabilistic coprocessor:** \textit{N-bit RNG} and \textit{Kernel} blocks can have parallel units for problems that benefit from it. For \textit{N-bit RNG} blocks, s-MTJ based p-bit arrays can be utilized.

### A. Hardware implementation for \textit{N-bit RNG} block

As hardware implementation for the \textit{N-bit RNG} block in the architecture in Fig. 1, an array of compact hardware p-bits\textsuperscript{9} consisting of just 3 transistors and 1 stochastic MTJ can be utilized whereas CMOS alternatives like linear-feedback shift registers (LFSRs) would require 1000+ transistors. We note that the p-bits can supply tunable random numbers whereas simple LFSRs would require additional hardware in the form of lookup tables (LUTs) to generate tunable random numbers\textsuperscript{13}. The p-bit design was first proposed by Camsari et al.\textsuperscript{9} and analyzed by Hassan et al.\textsuperscript{14,15} The overall power consumption of one hardware p-bit is around 20\,\mu W which is orders of magnitude better than CMOS alternatives\textsuperscript{10}. Another advantage of this compact RNG-source is that it is based on stochastic MTJs which can operate at nanosecond speeds which has been shown theoretically as well as experimentally\textsuperscript{16–19}. The random number generation of the p-bit design can be tuned with the input voltage at the gate of the NMOS-transistor \(V_{IN}\) and has a bipolar output voltage \(V_{OUT} = \pm V_{DD}/2\). The average of the binary bitstream of the p-bit can be described by \(\langle V_{OUT} \rangle \approx V_{DD}/2 \cdot \tanh(V_{IN}/V_0)\) where \(V_0\) is a material dependent reference voltage. This tunability is important for problems with feedback (compare section III B 1) since the proposal distribution is dependent on the current configuration of the system. For cases where the proposed configuration must be close to the current p-bit state vector, all p-bits can be biased to the current configuration and only have a small probability to generate a perturbed state.

### III. BENCHMARKING THE PROBABILISTIC COPROCESSOR

In this section, we address several problems with the probabilistic coprocessor. We compare the time to solution of our \textit{p-computer} emulation and \textit{p-computer} projection with the performance on CPU and GPU for every problem.

Broadly, there are two classes of Monte Carlo algorithms: simple Monte Carlo algorithms that perform direct sampling and Markov Chain Monte Carlo techniques. Both require many random numbers, however, Markov Chain Monte Carlo also requires feedback from \textit{Kernel} back to \textit{N-bit RNG} (see black arrow in Fig. 1).

#### A. Basic Monte Carlo techniques

The advantage of basic Monte Carlo techniques is that they are easy to parallelize and do not require convergence. The standard error is given by \(e_r = \sigma/\sqrt{N_S}\) and the solution accuracy improves proportional to \(1/\sqrt{N_S}\). As mentioned in the introduction the RNG generation can be the bottleneck since the mathematically heavy part is readily addressed by GPUs, resistive crossbars or by pipelining\textsuperscript{20}. Hence, the very rapid random number generation of \textit{p-computers} can be fully utilized. In our \textit{p-computer} emulation, we use pipelining to increase the data processing rate but other approaches are valid.

#### 1. Monte Carlo integration

One main advantage of the Monte Carlo calculation is that it can be straight-forwardly parallelized. Monte Carlo integration is especially advantageous to use for problems with many dimensions where it scales better than deterministic numerical integration techniques\textsuperscript{21}. To illustrate this point we demonstrate numerical integration on a simple example of calculating \(\pi\) by randomly drawing coordinates from a square as shown in Fig. 3 a).
To understand the procedure, we consider the Monte Carlo approach to estimating the value of π. The idea is to randomly generate points within a unit square and count the proportion of them that fall within a quarter circle of radius 1. This proportion is then used to approximate the value of π.

The accuracy of the estimation is shown in Fig. 3 d). For the π problem the standard deviation σ of the standard error is given by $\sigma = \sqrt{\frac{1}{N} \left(1 - \frac{\pi}{4}\right)/4}$. The main advantage of the p-computer compared to CPU and GPU is that the number of parallel blocks $N_p$ is much higher. We note, however, that in a fully pipelined design, some setup time $t_{su}$ is required to fill the pipeline. However, in this paper the pipeline stage number is small $t_{su} \ll TTS$ and $t_{su}$ can be neglected.

We note that this is just a simple example of Monte Carlo integration and other deterministic approaches to calculate π are superior. However, for integrals with many dimensions, Monte Carlo integration has better scaling than conventional methods such as trapezoidal and Simpson’s rule.

2. Uncertainty quantification

Fig. 4 shows uncertainty quantification using our probabilistic coprocessor. One way of quantifying uncertainty is to use Bootstrap resampling. Given a limited dataset, this resampling technique can be used to make a statement about the sampling error of dataset without making assumptions about the underlying distribution. The Bootstrap technique redraws from the limited dataset with replacement and checks if the parameters like mean or standard deviation change significantly for each resampled distribution. We note note that the ideal Bootstrapping becomes intractable quickly due to the large number of possible redraws which makes Monte Carlo techniques necessary.

Here, we use a dataset for A/B testing containing 1174 mothers and the birth weight of their babies that are classified into two groups: smoker and non-smokers. This results in a linear relationship between numbers of samples and the time to solution:

$$TTS = \frac{N_S}{f_{clk} \cdot N_p}$$

where $N_S$ is the number of samples, $f_{clk}$ the clock frequency and $N_p = 2800$ the number of parallel blocks. Eq. 1 is general for all Basic Monte Carlo in this section. The accuracy of the π estimation is shown in Fig. 3 d). For the π problem the standard deviation $\sigma$ of the standard error is given by $\sigma = \sqrt{\pi(1 - \pi/4)/4}$. The main advantage of the p-computer compared to CPU and GPU is that the number of parallel blocks $N_p$ is much higher. We note, however, that in a fully pipelined design, some setup time $t_{su}$ is required to fill the pipeline. However, in this paper the pipeline stage number is small $t_{su} \ll TTS$ and $t_{su}$ can be neglected.

To quantify if the birth weight is influenced by the fact that the mothers smoked during pregnancy, bootstrap resampling can be utilized. The overall implemented structure on for the p-computer emulation is shown in Fig. 4 a) where the Kernel is adapted to collect the histogram for the difference of the means. Here, instead of reading one number, 64 values for 64 bins are read out. In order to be able to collect statistics for multiple datasets the bin width and bin position for the bootstrapped distribution can be sent to the p-computer after implementation of the design. The TTS of the Bootstrap resampling is plotted for different total number of samples and compared to CPU and GPU. In addition, the projection of the p-computer with increased number of parallel blocks is plotted in Fig 4 b). It can be clearly seen that the p-computer emulation performs much better than CPU and GPU implementation. The overall behavior can be described by Eq. 1. Note that the parallelization in this example is done by having $N_p = 1500$ blocks shown in Fig. 4 a) and the mean is calculated serially. In principle, it is possible to have parallelization in both mean calculations which would increase the advantage when comparing the execution to CPU and GPU.

The difference of the means is plotted in a histogram for A/B testing containing 1174 mothers and the birth weight of their babies that are classified into two groups: smoker and non-smokers. This results in a linear relationship between numbers of samples and the time to solution.

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3. Bayesian networks

Bayesian networks can be mapped to the p-computer as shown in Fig. 5 a). Here, multiple N-bit RNG and Kernel are put in series to represent different layers of a Bayesian network. Every node of the Bayesian network can be represented by a tunable 1-bit RNG or p-bit\textsuperscript{25}. As an example we use the genetic relatedness in a family tree\textsuperscript{20–27}. The relatedness of two family members can directly be extracted from the network by measuring the correlation of the two corresponding p-bits. The absolute values of the correlation are shown in Fig. 5 b) for a family tree with 7 generations starting with 64 nodes in the first layer down to 1 node in layer 7. At total 127 members of the family tree are represented in the p-bit network. Every network is copied 10 times so that we emulated a network of 1270 p-bits total. Again the error of the correlation goes down \( \sim 1/\sqrt{N_S} \) using this method. Compared to deterministic algorithms, the advantage of a probabilistic computer is that during integration,

\[
P_A(x_A) = \int dx_B P(x_A, x_B),
\]

observed variables \( x_A \) can directly be measured without integrating over unobserved variables \( x_B \) as noted by Feynman\textsuperscript{7}.

The Bayesian network implemented on the emulated p-computer is benchmarked against the same algorithm run on CPU in Fig. 5 c). Compared to CPU we see around 2 orders of magnitude improvement and expect further improvement for the projected p-computer utilizing some parallelization techniques can be utilized to increase performance like partitioning the random variables into independent groups, multiple-try Metropolis\textsuperscript{30,31} or parallel tempering\textsuperscript{32,33}.

An important class of problems that can be readily addressed are optimization problems like finding the ground state of an Ising Model or the Knapsack problem. These problems are NP-hard which means that it takes exponential amount of resources to compute a solution. However, Monte Carlo algorithms utilizing random numbers can find approximate solution faster than the deterministic counterpart. To show that our probabilistic coprocessor can be used to solve problems like these, we use it to solve the Knapsack problem.

1. 0-1 Knapsack problem

The Knapsack problem is a famous difficult optimization problem. It can be mapped to problems like financial modeling, inventory management, resource allocation or

![FIG. 5. Bayesian network with probabilistic coprocessor:](image)

![FIG. 4. Bootstrap resampling:](image)
yield management. Given \( N \) items where each item has a given weight \( W \) and value \( V \), the goal is to find a configuration \( x = \max_i \left[ \sum_i V_i x_i \right] \) where \( \sum_i W_i x_i \leq C \) with capacity \( C \). To utilize the parallel RNG to the fullest we have implemented a pipeline that accepts new proposals every clock cycle as shown in Fig. 6 a) even if the \textit{Kernel} needs more than one clock cycle to propagate a new proposal. This approach is similar to multiple-try Metropolis. Each proposal uses the current state at a starting point and changes the state of 2 items at random. The generated proposal is then send into the pipeline and the new weight and value is calculated by making use of the fact that only the 2 flipped item’s weight and value are changed. If the weight value is smaller or equal to the maximum allowed weight, the new state is propagated to the accept/reject block where it is weighted by an exponential function and compared to the last accepted state. If accepted the current state is updated.

\[ TTS(N) = T_{run} \frac{\log(0.01)}{\log(1 - p_s)}, \]

where \( p_s \) is the probability of finding an acceptable solution when running the algorithm for a time \( T_{run} \). We define a success as finding a configuration that has a value that is larger than 99% of the ideal solution value. The emulated p-computer uses 10 different Markov Chains in parallel which decreases the TTS for smaller problem sizes (compare orange solid line to grey dashed line). The running time \( T_{run} \) is given by \( T_{run} = N_S \cdot \text{clock} \) for the p-computer emulation and as CPU running time for CPU. For the MCMC scheme we use a simulated annealing approach where the temperature is reduced exponentially by a factor of two every \( N_S/10 \) samples. To find the best annealing schedule for every problem size \( N \), we varied the number of total samples \( N_S = 2^x \cdot 10 \) with \( x = 1, 2, \ldots 20 \) and plotted the minimum TTS in Fig. 6 b). For each item property, we randomly draw a value \( V_i \) and weight \( W_i \) between 0 and 1000. As capacity we use \( C = \sum_{i=0}^{N} W_i / 2 \) for all problem sizes.

Fig. 6 b) shows that p-computer outperforms the dynamic programming algorithm on both CPU and GPU and is also about 1-2 orders faster than the MCMC implementation on CPU. The p-computer emulation is, however, outperformed by the special deterministic \textit{combo} algorithm developed by Pisinger and colleagues. We note that the MCMC approach is much more general than this specific algorithm. In addition, the algorithm on the probabilistic computer could be further improved for example by adding parallel tempering.

\[ \text{FIG. 6. Knapsack problem: a) p-computer emulation on sampling block of p-computer: LFSRs generate random numbers and the following logic is used to calculate the mean of a given Bootstrap sample, subtract both groups and collect the data in a histogram. b) Time to solution vs. problem size \( N \) for different platforms (CPU, GPU and p-computer) and different algorithms (DP, MCMC, Pisinger).} \]

In conclusion, we have benchmarked a probabilistic co-processor emulated on FPGA for multiple Monte Carlo applications. We show that the coprocessor can outperform conventional platforms by multiple orders of magnitude. We project that an integrated chip based on stochastic MTJs could show even better improvement in power consumption and speed.

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\[ ^1 Goto, H., Tatsumura, K. & Dixon, A. R. Combinatorial optimization by simulating adiabatic bifurcations in nonlinear Hamiltonian systems. Science Advances \textbf{5}, eaav3272 (2019). \]

\[ ^2 Aramon, M. \textit{et al.} Physics-Inspired Optimization for Quadratic Unconstrained Problems Using a Digital Annealer. Frontiers in Physics \textbf{7} (2019). \]
V. METHODS

For CPU benchmarks we used a Intel(R) Xeon(R) @ 2.3GHz CPU using C++ implementations. GPU results were obtained on a Tesla T4 @ 1.59GHz GPU using CUDA or Tensorflow platforms. For CPU, we note that interfaces like OpenMP can be utilized to run the Monte Carlo approach on multiple CPU cores. Here, we did not utilize any multi-processor interfaces for the CPU benchmarks. In general, the number of FPGA integration cores can be much larger than the typical number of CPU or GPU cores.

A. Emulated p-computer implementation

As FPGA hardware, a Xilinx Virtex Ultrascale+ xcux9p-flgb2104-2-i provided via Amazon Web Services F1 cloud-accessible EC2 compute instances is utilized. The logical organization of the FPGA is shown in Fig. 7. The problem parameters can be sent from the Linux userspace to the p-computer through the PCIe interface. For control signals, the AXI-Lite bus for direct register access is utilized. The results from the p-computer operation shown in Fig. 1 is sent to the on-chip DDR4 memory using an AXI interconnect interface. The data can then be read out from the DDR4 and send to the Linux Userspace through PCIe using direct memory access (DMA). For each data point the time stamp is saved in order to be able to extract the execution time of the emulated p-computer accurately.

References:

1. Yamamoto, K. et al. 7.3 STATICA: A 512-Spin 0.25M-Weight Full-Digital Annealing Processor with a Near-Memory All-Spin-Updates-at-Once Architecture for Combinatorial Optimization with Complete Spin-Spin Interactions. In 2020 IEEE International Solid-State Circuits Conference - (ISSCC), 138–140 (IEEE, San Francisco, CA, USA, 2020).
2. Yamaoka, M. et al. 24.3 20k-spin Ising chip for combinational optimization problem with CMOS annealing. In 2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, 1–3 (2015).
3. Ahmed, I., Chiu, P.-W. & Kim, C. H. A Probabilistic Self-Annealing Compute Fabric Based on 560 Hexagonally Coupled Ring Oscillators for Solving Combinatorial Optimization Problems. In 2020 IEEE Symposium on VLSI Circuits, 1–2 (IEEE, Honolulu, HI, USA, 2020).
4. Patel, S., Chen, L., Canoza, P. & Salahuddin, S. Ising Model Optimization Problems on a FPGA Accelerated Restricted Boltzmann Machine. arXiv:2008.04436 [physics] (2020).
5. Feynman, R. Physical computing with computers. Int. J. Theor. Phys 21 (1982).
6. Camsari, K. Y., Faria, R., Sutton, B. M. & Datta, S. Stochastic p-Bits for Invertible Logic. Physical Review X 7 (2017).
7. Camsari, K. Y., Salahuddin, S. & Datta, S. Implementing p-bits with Embedded MTJ. IEEE Electron Device Letters 38, 1767–1770 (2017).
8. Borders, W. A. et al. Integer factorization using stochastic magnetic tunnel junctions. Nature 573, 390–393 (2019).
9. Cipra, B. A. The Best of the 20th Century: Editors Name Top 10 Algorithms. SIAM News 33, 1–2 (2000).
10. Nguyen, H. Gpu Gems 3 (Addison-Wesley Professional, 2007), first edn.
11. Sutton, B. et al. Autonomous Probabilistic Coprocessing with Petalips per Second. IEEE Access 1–2 (2020).
12. Hassan, O., Faria, R., Camsari, K. Y., Sun, J. Z. & Datta, S. Low-Barrier Magnet Design for Efficient Hardware Binary Stochastic Neurons. IEEE Magnetics Letters 10, 1–2 (2019).
13. Hassan, O., Datta, S. & Camsari, K. Y. Quantitative Evaluation of Hardware Binary Stochastic Neurons. Physical Review Applied 15, 064046 (2021).
14. Kaiser, J. et al. Subnanosecond Fluctuations in Low-Barrier Nanomagnets. Physical Review Applied 12, 054056 (2019).
15. Safranski, C. et al. Demonstration of Nanosecond Operation in Stochastic Magnetic Tunnel Junctions. Nano Letters 21, 2040–2045 (2021).
16. Hayakawa, K. et al. Nanosecond Random Telegraph Noise in In-Plane Magnetic Tunnel Junctions. Physical Review Letters 126, 117202 (2021).
17. Kanai, S., Hayakawa, K., Ohno, H. & Fukami, S. Theory of relaxation time of stochastic nanomagnets. Physical Review B 103, 094423 (2021).
18. Kogge, P. M. The Architecture of Pipelined Computers (CRC press, 1981).
19. Joseph, A. Markov Chain Monte Carlo Methods in Quantum Field Theories: A Modern Primer (Springer Nature, 2020).
20. Efron, B. & Tibshirani, R. J. An Introduction to the Bootstrap (CRC Press, 1994).
21. Efron, B. Second thoughts on the bootstrap. Statistical science 135–140 (2003).
22. https://github.com/dataciencetrain/defa-2018sp-public/tree/master/textbook.
23. Faria, R., Camsari, K. Y. & Datta, S. Implementing Bayesian networks with embedded stochastic MRAM. AIP Advances 8, 045101 (2018).
24. Camsari, K. Y., Sutton, B. M. & Datta, S. P-bits for probabilistic spin logic. Applied Physics Reviews 6, 011305 (2019).
25. Faria, R., Kaiser, J., Camsari, K. Y. & Datta, S. Hardware Design for Autonomous Bayesian Networks. Frontiers in Computational Neuroscience 15 (2021).
26. Metropolis, N., Rosenbluth, A. W., Rosenbluth, M. N., Teller, A. H. & Teller, E. Equation of State Calculations by Fast Computing Machines. The Journal of Chemical Physics 21, 1087–1092 (1953).
27. Hastings, W. K. Monte Carlo sampling methods using Markov chains and their applications. Biometrika 57, 97–109 (1970).
28. Byrd, J., Jarvis, S. & Blahut, A. Reducing the run-time of MCMC programs by multithreading on SMP architectures. 1–8 (2008).
29. Liu, J. S., Liang, F. & Wong, W. H. The Multiple-Try Method and Local Optimization in Metropolis Sampling. Journal of the American Statistical Association 95, 121–134 (2000).
30. Swendsen, R. & Wang, J.-S. Replica Monte Carlo Simulation of Spin-Glasses. Physical review letters 57, 2607–2609 (1986).
31. Earl, D. J. & Deem, M. W. Parallel tempering: Theory, applications, and new perspectives. Physical Chemistry Chemical Physics 7, 3910–3916 (2005).
32. Pisinger, D. A minimal algorithm for the multiple-choice knapsack problem. European Journal of Operational Research 83, 394–410 (1995).
33. Martello, S., Pisinger, D. & Toth, P. Dynamic Programming and Strong Bounds for the 0-1 Knapsack Problem. Management Science 45, 414–424 (1999).
34. Ronnow, T. F. et al. Defining and detecting quantum speedup. Science 345, 420–424 (2014).
35. McMahon, P. L. et al. A fully programmable 100-spin coherent Ising machine with all-to-all connections. Science 354, 614–617 (2016).
36. Kellerer, H., Pferschy, U. & Pisinger, D. Knapsack Problems (2004).
FIG. 7. Logical Organization and Memory Map of the FPGA used to emulate the p-computer: The p-computer is connected to the AWS userspace through PCI Express interface (PCIe). The data generated by the p-computer is saved on the DDR4 on-chip memory.