Enhanced Performance of a DVR using Mixed Cascaded Multilevel Inverter

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Abstract
This proposed paper studies the design and performance of a new ’Dynamic voltage restorer’ (DVR) using a new hybrid 7 level PWM inverter. The new multilevel inverter is a combination of the capacitor clamped and the cascaded H-bridge type multilevel inverters. This new topology provides different levels of output voltages and high modularity. In the paper, the sag or swell are detected in a transmission line and the voltage is injected from the multilevel inverter through a boost transformer. Simulation results in matlab show that the performance of the new mixed multicell inverter is better than the traditional MLIs and normal inverters with the advantages like absence of the filter.

1. Multilevel Inverters
Multilevel inverters have become a very important aspect in the industries which have the capability of operating at high power using the medium voltage rated switches. The multilevel inverters traditionally are three types,

i) Neutral clamped MLI
ii) Capacitor clamped MLI
iii) Cascaded H-bridge MLI

These all traditional inverters have their own advantages and disadvantages. Using the advantages of these traditional inverters, a new topology is designed combining the flying capacitor and cascaded H-bridge which reduces the use of number of switches and gives a better performance. The new topology is named as mixed cascaded multi-level inverter(MCI).

The neutral clamped MLI has an advantage of higher efficiency at the fundamental frequencies in switching, but it requires a very high number of switches which will in turn reduce the overall efficiency. It requires (N-1) switches and (N-1)(N-2) clamping diodes for a N level output. In the case of a capacitor clamped MLI, we have the advantage of higher switching redundancies but it suffers from the disadvantage of the necessity of pre-charging of the balancing capacitors. This topology requires (N-1) switches and (N-1) balancing capacitors. The cascaded H-bridge MLI is a very simple and it is modular which makes it very easy to design. This topology of the MLI has the disadvantage of the requirement of separate DC source for each cell of the inverter. This requires (N-1)/2 modules for N levels where one module have 4 switches.

2. Dynamic Voltage Restorer (DVR)
Voltage disturbances in a power transmission line are the most common problems in a power system. These are because of the symmetrical or unsymmetrical faults of the system. The unsymmetrical faults constitute the line-ground, double line ground, line to line fault etc. the symmetrical fault is three line fault. The most probable
disturbances are voltage sag, voltage swell, harmonics, flickers. These disturbances can cause adverse effects on the sensitive loads in industries and domestic side. The voltage sag is a fall in the voltage level from 10% to 90% of its nominal value. Voltage swell is a momentary increase in the value of the line voltage.

Dynamic voltage restorer is a power-electronic device which is used to inject a dynamically controlled voltage into the transmission line for the compensation of the sag or swell of a system\(^2\). The basic DVR schematic diagram is given in the Figure 1. The storage unit is a battery or a DC source. The DVR will work independent of the type of fault, with the reference acquired from the control strategy used in the system. There are many types of control strategies like PID, fuzzy logic, PLL and many other systems for the voltage disturbance detection in the transmission line. The strategy used in this paper is PLL based magnitude comparison method. We are supposed to generate the magnitude of the phase voltage in per unit value and compare with a unit magnitude and the resultant signal is given as a reference to the inverter. Normally a inverter is used to convert the DC to AC supply in the compensation of the disturbances. In this paper we are designing a new multilevel inverter to inject the voltages in the system.

3. Mixed Cascaded Multilevel Inverter

Taking the advantages and disadvantages of the traditional multilevel inverters, we design a new topology which will be a combination of two types of MLIS. The use of a single source and variable switching possibilities of a capacitor clamped inverter and modular setting of the cascaded inverter are combined together and a hybrid multilevel inverter is formed. This new model will provide a higher number of voltage levels using less number of switches\(^6\).

The proposed model is a 7-level inverter which contains 3 cells of capacitor clamped MLI connected in series with a cell of cascaded H-bridge MLI. The capacitor clamped gives a 4 level output including 0v for a DC voltage and the output is given as input to cascaded H-bridge MLI which gives +ve and –ve output for the input which gives 7-level output for the given DC supply. The proposed mixed cascaded multilevel inverter (MCML) is given the Figure 2. We can observe that the 3 cells of capacitor clamped are connected in series with the H bridge inverter. The levels of output obtained in the MCML are \(V, 2V/3, V/3, 0, -V/3, 2V/3, -V\) for a DC supply of \(V\) volts.

The PWM circuit which is used for firing the inverter is given in the Figure 3. The reference signal of one phase voltage is taken and compared with 3 carriers using a technique similar to POD pwm. The resultant pulses are given to the capacitor clamped MLI. These pulses switch the IGBTs giving different levels of voltages in the output. The output waveforms of the MCML is given in the Figure 4.
4. Proposed DVR Model

The DVR model which is designed uses the new multilevel inverter in place of a normal inverter which will test the performance and working of the mixed cascaded multilevel inverter. The control strategy is shown in the Figure 5. The phase voltages are taken from the three phase voltage measurement and given to the control block. The PLL block is used to generate the magnitudes per each phase which are compared with the unit function to give a resultant signal. This is converted to sinusoidal signal which is in phase with the corresponding line. This signal is given to the MCML as the reference input for the PWM generation. This turns on the inverter when there is a fault occurred in the line. The sag or swell is detected and the reference signal is given to the MCML and this inverter injects the required voltage to the line through a boost transformer.

The main circuit diagram of the DVR system using the proposed multilevel inverter is shown as in the Figure 8. The voltage from each phase is compensated using three single phase mixed cascaded multilevel inverters. The signals are processed by sending them to PLL blocks and magnitude comparison and conversion into a sine wave. The error magnitude is adjusted using a proportional controller.

5. Simulation and Results

The proposed DVR model is simulated and tested for a L-G fault in the transmission line. For this, a power system model is created with two different loads. The 13KV output from the generation point is stepped up to 115KV using the power transformers. This is stepped down to 11KV at the distribution end. A 3 phase fault block is used to generate a L-G fault in the first phase. A DC source of 5.5KV is used for the supply to inverter. The total output is boosted up in a 1:2 transformer and supplied to the line. For the designed system, a LC filter is used with the specifications of inductance L at 10mH and capacitance C at 20uF.

The fault occurs at a time interval between 0.2 sec to 0.4 sec. Due to the L-G fault, the voltage in A phase becomes zero i.e a sag and the other two phases suffer with a swell. The per unit value of the voltages are taken in the control block and the proportional controller is set for a value K=0.9 for this case. The error signals are generated and this error is given as a reference to the PWM circuit. The specifications used in this model are given in the table 1. The input or the source side voltage during the fault is given in Figure 6. The reference signals which are the output of control block are given in the Figure 8. This signals are the reference of the MCML which will inject the required amount of voltage for the compensation of fault. The table shows the specifications used in the model.

The inverter output for the A phase is given in the Figure 9. The final compensated load side voltage is

| Sl no | Specification          | Value       |
|-------|------------------------|-------------|
| 1     | Supply voltage         | 13KV        |
| 2     | DC source voltage      | 5.5KV       |
| 3     | L,C filter values      | 10mH,20uF   |
| 4     | Load R,L               | 100hm,1mH   |
| 5     | Proportional gain,Kp   | 0.9         |
| 6     | Carrier frequency      | 2500 hz     |
| 7     | Fault                  | L-G         |
Figure 6. Voltage at the source side.

Figure 7. Proposed DVR circuit.

Figure 8. Reference signals to the PWM.

Figure 9. Output of multilevel inverter at phase A.

Figure 10. Compensated load side voltage waveform.

given in the Figure 10. The other two phases also have the similar outputs according to their reference signals given. As shown in the Figure 7, the controller of DVR is sending the input pulses for PWM of the MCML.

6. Conclusion

The design of a new DVR model using the mixed cascaded multilevel inverter (MCML) instead of the conventional inverters or the traditional multilevel inverters is successfully completed and the results show that the compensation of the DVR is working efficiently. The advantage of using the MCML in the DVR is that it has a reduced number of switches when compared to the traditional multilevel inverters and at the same time, it reduces the requirement of the size of capacitor as we can get the near sinusoidal voltages unlike the conventional inverters which produce the rectangular voltage outputs with harmonics. The compensated voltages are well below the tolerance levels of disturbances of the loads which ensure us the continuous supply of power even at fault conditions.
7. References

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