The LHCb Muon Upgrade

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ABSTRACT: The LHCb collaboration is currently working on the upgrade of the experiment to allow, after 2019, an efficient data collection while running at an instantaneous luminosity of $2 \times 10^{33} \text{ cm}^{-2}\text{s}^{-1}$. The upgrade will allow 40 MHz detector readout, and events will be selected by means of a very flexible software-based trigger. The muon system will be upgraded in two phases. In the first phase, the off-detector readout electronics will be redesigned to allow complete event readout at 40 MHz. Also, part of the channel logical-ORs, used to reduce the total readout channel count, will be removed to reduce dead time in critical regions. In a second phase, higher-granularity detectors will replace the ones installed in highly irradiated regions, to guarantee efficient muon system performances in the upgrade data taking conditions.

KEYWORDS: Data acquisition circuits; Control and monitor systems online; Wire chambers (MWPC, Thin-gap chambers, drift chambers, drift tubes, proportional chambers etc); Micropattern gaseous detectors (MSGC, GEM, THGEM, RETHGEM, MHSP, MICROPIC, MICROMEGAS, InGrid, etc)

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1 Introduction

The muon readout electronics [1] convert the analogue signal extracted from detector physical pads into logical channels (essentially X and Y strips), which are input to the L0 muon trigger algorithm. The present architecture is shown in figure 1.

The analogue signals are amplified, shaped and discriminated by means of a custom ASIC named CARIOCA [2]. The digital outputs of the CARIOCAs are combined in logical-OR both on the front-end boards (via another custom ASIC, the DIALOG [3]) and in the Intermediate Boards (IB) [4] to generate the logical channels. The logical channels are processed in the Off Detector Electronics (ODE) system [4], based on the custom SYNC chip [5], where they are synchronized with the master LHCb clock and grouped in the Trigger Unit (TU). These data are serialized with GOL chips [6] and sent to the level-zero muon (L0 muon) trigger processor at a rate of 40 MHz by means of optical interfaces. The arrival time of each channel with respect to the bunch crossing is measured through a 4-bits TDC with a resolution of about 1.5. The data are buffered in internal memories and, if a positive answer is received from the L0 muon trigger processor, they are sent to TELL1 [7] at a maximum rate of 1 MHz. The TDC information is of fundamental importance to synchronize all the readout channels and ensure the required time resolution of the whole muon system [1]. The front-end chips (CARIOCA and DIALOG) are controlled via the Service Board (SB) system [8], which also implements a pulsing system (PDM), used to synchronize and to time
align the detector. Both ODE and SB systems rely on the TFC system [9] from which they receive the master clock, the synchronization signals and the L0 commands. A CANBus based ELMB board [10] is used for the ECS interface [11].

This architecture, although well matched to current operation, is not suited to the requirements of the upgrade. Drawbacks include the obsolescence of certain components, the lack of flexibility to match the future running conditions, the TDC information extracted at only 1 MHz rate and the necessity to maintain (emulate) the present TFC and ECS systems. To address these concerns, while also optimising manpower, effort and costs, it has been decided:

- to replace the ODE, the SB and the PDM with new electronic boards, maintaining the present crates and power supply system;
- to maintain the present front-end electronics and the IB system whose replacement would otherwise require a complete disassembly of chambers and cables.

This new electronics must be electrically and mechanically compatible with the existing system in order to guarantee a simple and fast replacement. It will have to use the new GBT [12] and Versatile Link [13] components to implement the trigger, DAQ, TFC and ECS interfaces and to be fully compliant with the LHCb upgraded electronics specifications. Finally the upgraded electronics, maintaining the present functionalities, will also have to:

- allow the TDC readout at a rate of 40 MHz;
- eventually allow for an increase in channel granularity, achieved through either IB boards and/or new chambers;
- minimize the number of readout links to allow a possible trigger implementation in the TELL40 [14].

**Figure 1.** Present muon system electronics architecture.
2 The new readout architecture

A new Off Detector Electronics board (nODE) will replace the present ODE board and will be mechanically and electrically compatible with the current electronics. The nODE will have up to 192 input channels and will be based on a new rad-tolerant custom ASIC, the nSYNC, which will integrate all the required functionalities (clock synchronization, BX alignment, trigger hits production, time measurements, histogram capability, buffers). The nSYNC will also handle the zero suppression algorithm for the TDC data and the interfaces to the data acquisition and TFC/ECS systems. Such interfaces will be based on the GBT and Versatile Link components to guarantee full compatibility with the new electronic systems foreseen for the LHCb upgrade.

The so-called DAQ interface must allow a unidirectional data transfer of the binary hits information to the corresponding TELL40 boards, where also the new muon Low-Level Trigger (LLT) will be implemented. The hit map of the channels must be sent at a rate of 40 MHz (bunch per bunch) with minimum data latency and without any kind of zero suppression or data truncation. All the logical channels belonging to the same trigger unit (TU) will be grouped in a single data frame and will be sent to the trigger processor on the same link (each link can transmit more than one TU).

The so-called TDC interface must allow a unidirectional data transfer of the TDC information to the TELL40 boards. The TDC data need to be zero suppressed and formatted before transmission to optimize the number of required links. The elaboration and transmission time is not fixed and it fluctuates in each bunch crossing depending on the detector occupancy. Therefore, pipeline stages and buffers will be implemented and data truncation is foreseen.

Obviously the zero suppressed TDC data require a geographic addressing to be identified. This information is indeed contained in the hits map that is also used for the trigger purposes. Therefore, in order to avoid duplicating such information, the hits map will be used both for trigger algorithm and for TDC data address decoding. Such a choice allows an optimization of the bandwidth usage and a reduction in the number of links.

To measure the arrival time of the signals in the bunch crossing period, a 4-bits TDC with a resolution of about 1.5 ns will be used. To be consistent with the hits transmission, the TDC data will be send out using 2 links per board with the GBTx in WideBus mode (16 bits for header and 96 bits for data). A data encoding without error correction capability is usable also for TDC data because such information is typically used for time alignment and data integrity is not an issue. A maximum sustainable detector occupancy of 25% can be reached.

The TFC/ECS interface will be implemented with a dedicated full duplex link per board. It will use a GBTx in transceiver mode which acts as master and distributes the main clock to the other GBTx and to the nSYNC chips. The TFC commands will be received and decoded by each nSYNC chip. The master GBTx also provides the local ECS interface via a GBT-SCA chip. The ECS interface will be used to configure the electronics components of the board, to monitor their status and to download the time histograms. Figure 2 shows a block scheme of the nODE board.

To match the future run conditions in term of higher granularity and occupancy, the nODE will be compatible with the present IB board. In such a way a simple replacement of an IB with a nODE board will reduce the logical channels dimension and their occupancy. This is equivalent to the increase of detector granularity and has as drawback the increase in number of logical channels.
to be sent to the trigger system. The nODE architecture will also be compatible with any future higher granularity chambers if the present logical pad dimension will be maintained.

The nSYNC will be the core of the new Off Detector Electronics Boards (nODE). It will receive the data coming from the detectors, synchronizing them with the bunch-crossing identification number (BXid) and sending the binary information of the hits (that will also be used by the muon trigger) and the time information to the TELL40s. Data will be transmitted by interfacing the nSYNC to the GBTx. The nSYNC will have 32 input channels from which it will receive the LVDS data from the front-end electronics and from the IB system. Each channel will be equipped with a 4-bits TDC to measure the phase of incoming signals with respect to the LHCb master clock. The TDC information will be used internally to build a histogram of the incoming signal phase in order to perform the so-called fine-time synchronization that is crucial for achieving the required muon system efficiency. The histograms will be read back through the ECS interface. The TDC data will pass through the data flow together with the related hits information. These complex data will then be synchronized with respect to the BXid using a 12-bits internal counter. The TFC information will come from a GBTx housed in the nODE board. This information will be decoded inside the nSYNC. A block diagram of the nSYNC ASIC is shown in figure 2. After the proper BXid assignment to the complex data set, a Frame Header will be generated according to the requirements of the “Electronics Architecture of the LHCb Upgrade” specification document [15]. The Frame Header and the binary hit information will be sent, via a GBT interface, to the TELL40 recording the binary muon hits information, where also the muon LLT will be implemented. Using this information, the TDC data will be zero-suppressed (ZS) to reduce the required bandwidth. The Frame Header and the ZS TDC data will then be sent to the TELL40 recording the muon hits time via another GBT interface. Some programmable buffers are foreseen before the two GBT interfaces to guarantee the synchronization between data coming from different nSYNC. The nSYNC chip will be configured and controlled through ECS using a standard interface such as I2C or SPI. All the registers inside will be triple-voted and the configuration register will also have an automatic refresh system.

Figure 2. Block diagram of the nODE (left) and of the nSYNC ASIC (right).
3 The new control and pulsing systems

The current Muon Front-End Control (MuFEC) electronics is based on two custom boards, the Service Board (SB) and the Pulse Distribution Module (PDM), that communicate between themselves through a custom backplane. They are used to control, monitor and test every single channel of the detector front-end electronics. The MuFEC allows the threshold and the counter registers of every single channel to be accessed, playing a fundamental role in the noise measurement and in the threshold adjustment of the whole muon system. The MuFEC, together with the ODE boards, is also essential in detector time alignment, a procedure needed to achieve the required system efficiency. This is performed by injecting calibration pulses at a specific bunch crossing, allowing the delay calibration of every single muon detector channel. The PDM receives four CAN ports and distributes them to the SBs through the custom backplane. The programmable components of the boards are based on microcontrollers and flash memory technologies, which are fully radiation tolerant. The current system use a total of 600 microcontrollers. Each microcontroller performs well defined tasks when specific commands are received via CANbus. The timing information are received from the TFC system via a TTCrx chip and are used to broadcast timing signals to the full muon system.

The new MuFEC, while maintaining the original architecture of the system for what concerns crate allocation and module partitions, will use the GBTx and Versatile Link components to implement a TFC interface compliant with the new standard foreseen in the LHCb upgrade. Such an interface will not only allow the broadcasting of trigger and timing information, but will also provide a fast bidirectional data link for the experimental control system. An additional radiation hard chip named the GBT-SCA will be interfaced to the GBTx to control the I²C lines to the front-end boards. The new system will be built using three new components:

- a new PDM (nPDM) board based on the GBTx and GBT-SCA chips;
- a new SB (nSB) board mainly based on the GBT-SCA and a radiation tolerant Actel FPGA (based on flash technology) to provide some external logic; a new backplane to dispatch the communications channels (e-link) from the nPDM to the nSB boards.

The block diagrams of the nPDM and the nSB are shown in figure 3. The replacement of the CANbus with a faster data link will allow the removal of the local intelligence (the microcontrollers) from the control boards, and all system operations will be performed directly via software. The MuFEC upgrade will largely benefit from the new timing and fast control architecture developed within the LHCb collaboration for the upgrade, avoiding the use of obsolete components.

4 New detectors for Phase 2 upgrade

As already mentioned above, the muon system will be initially modified by replacing the off-detector electronics with new electronics compliant with the 40 MHz readout rate through TELL40. Only in a successive phase [16] higher readout granularity detectors will be installed in the central regions of the first stations, to overcome the efficiency losses due to the increase of detector deadtime caused by the higher luminosities, and to use detector technologies that can operate reliably in these highly irradiated regions, where detector ageing will become an issue.
The main objectives of this LHCb muon system phase 2 upgrade are the construction of new high granularity detectors for the inner regions (R1 and R2) of the first two muon stations and their electronics. The baseline detectors currently foreseen are anode-pad triple-GEM detectors for the R1 regions and cathode-pad MWPCs for the R2 regions. These detector technologies, according to the experience acquired during the LHC Run 1, appear to be promising solutions, both from the point of view of their rate capability [17] and their radiation hardness [18]. These detectors will have high-granularity pad readout to reduce the particle rate on each physical readout channel, in order to overcome the efficiency losses due to increased dead-time when operating in upgrade conditions. However the new readout granularity will remain compatible with the current muon detector projective layout, to allow the operation of the LLT without major modifications. New high-granularity MWPCs will be equipped with the current CARDIAC front-end boards based on the CARIOCA and the DIALOG chips. The very high channel density needed in R1 will require the development of a new highly-integrated front-end ASIC. To simplify the installation and the readout of these new high-granularity Triple-GEM detectors special readout boards will be developed. These boards, in addition to the new front-end electronics, will also be equipped with nSYNC chips to implement the nODE functionalities and will be directly readout via optical links.

This second phase of the upgrade has its basis on the R&D programmes foreseen for the period 2014-2019. New high-granularity detector prototypes and the required front-end electronics will be developed, new gas mixtures will be studied and extensive ageing tests will be performed.

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