HF-Release of Sacrificial Layers in CMOS-integrated MOEMS structures

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Abstract. In this paper we will present details of the release process of SiO$_2$ sacrificial layers we use within a multi-level MOEMS process developed by IPMS. Using such sacrificial layers gain a lot of benefits necessary for the production of high-end MOEMS devices like high surface quality and great surface planarity. However the HF-release of the sacrificial layer can be connected with specific issues. We present, which mechanisms are involved in the release process and how knowing them, can be the key for an optimized performance of the device. More-over we will present how to protect the CMOS backplane of our devices from unwanted HF attack during the release.

1. Introduction
The IPMS develops various types of Spatial light modulators (SLM), a kind of MOEMS [1], [2]. Applications for SLMs are high speed pattern generators for DUV lithography, for mask inspection, for wave front correction in adaptive optics and for projection systems. Each of these applications requires special material properties and structures especially for the parts of actuator suspension and mirrors and IPMS offers a wide range of possibilities to serve these purposes. SLMs with only small deflections can be fabricated using small air gaps and thicker spring. If higher deflection is required, the gap has to be increased. However in such case softer and thus mostly thinner hinges are needed to counteract the weaker electrostatic force at a given maximal drive voltage of the CMOS. Such MOEMS often use a reinforcement level additionally to the hinge and to the mirror level to fulfil the requirements on the device. A scheme and an exemplary image of such a three-level MOEMS are shown in figure 1 and 2.

The fabrication of most of our SLM is done on customized CMOS backplanes. For a successful integration of the MOEMS structure on the CMOS the use of SiO$_2$ as sacrificial layer is most promising. To obtain full movability of our mirrors, sacrificial layers, which provide low surface roughness and good homogeneity of thickness, are necessary. For our preparation process we use undoped SiO$_2$ as sacrificial layer material, which is deposited by plasma-enhanced chemical vapour deposition (PECVD) using Tetraethylorthosilicate (TEOS) as precursor material. A subsequent treatment by chemical-mechanical polishing (CMP) is performed to define the final actuator gap height and obtain a smooth and plain surface for the subsequent mirror deposition. The final release is performed by using gas-phase etch with hydrogen fluoride (HF) [3]. Most of the metal structures contain Aluminium based alloys, which are used to prepare soft hinges, reinforcements and high reflective mirrors. Details about the used materials and the preparation process can be found in [4].
2. HF-Release kinetics

2.1. Release mechanisms

A major topic one has to take into account using sacrificial layers is the etch kinetics of the release process. It is essential to know how fast the etching is done and which mechanisms lead to the specific etching fronts. From this information it is possible to adjust the duration of etching to the given MOEMS structures and the sacrificial volume, so an optimal processing refine of the device can be provided. Appearance of under-exposing to HF would lead to remaining oxide. In such a case e.g. if these remains connect movable structures, mirror deflection to its full extend would fail. On the other hand over-exposure can cause shortcomings, too. Especially metal surfaces are sensitive to corrosion by either the HF itself or water vapour occurring during the reaction chain of the etching. Keeping the release time on a low limit would also minimize risk and amount of corrosion of the open metal parts in the structure.

Unfortunately the movement of the etch front is not isotropic into the sacrificial volume over the full time of the release. We could observe three different mechanisms, which determine the actual shape of the etch front at a given time for a specific MOEMS design. The different mechanisms of etch front movement are shown in figure 3.

For our devices, the etch process starts in the slits between the mirrors. At the beginning the etch front moves with an isotropic manner into the SiO$_2$ forming the shape shown in subfigure 3A. However shortly after beginning, two anisotropic mechanisms become important and disturb the isotropic shape. The first one is the so called “topology based” (figure 3B) and is caused by the structure placed under the etched SiO$_2$, especially by filled vias. Long time before the etching front hits this structure, the etching velocity into the vertical direction increases. The reason for this behaviour is not fully understood but we assume that it is correlated with the behaviour during via filling. Since the growth of the oxide layer is not uniform from the bottom and the sidewalls, during the CVD several zones of growth exist and their fronts will meet at a certain point. In the worst case this can lead to voids inside the via but most probably provides areas with deviating density or stoichiometry, which not only exist inside the via but also above and slightly aside them, due to a low reduction of the different properties. Such disturbed areas show different etching sensitivity compared to the surrounding material on top of unstructured parts of the MOEMS. One example of this mechanism is shown in figure 4. One can see that the shape of the underlying hinge structure is patterned into the SiO$_2$, even though there is still an oxide layer with a thickness of approximately 200 nm on top of the spring.

While the first anisotropic mechanism is dominant in the vertical direction, the second one, which is called the “interface layer etch”, is more prominent in the horizontal one. As shown in the layout in
figure 3C, there is an oxide/oxide interface within the sacrificial layer. During the preparation of the device, the bottom oxide layer acts as stop for the etching of the hinge layer. The etching process influences the surface of this bottom layer in several ways although the exact reaction flow is still not fully understood. Our etching gas is a mixture of Cl₂ and BCl₃. Usually resist reacts with Chlorine in molecular as in elemental form to vinyl-like polymers, which are deposited on the surface. Usually, they should be removed during a subsequent cleaning, but residues are possible. A second process is a two-step reaction of the SiO₂ itself. Firstly it is reduced to Si by BCl₃ forming BOCl and finally reacts with Chlorine to SiCl₄ [5]. From all this reactions it can be assumed, but is not yet proven, that in the interface of two sacrificial layers there are phases of polymers, BOCl, Si or SiCl₄, which can change the interface properties of both layers or react with HF or later reaction products during the release and thus change the release kinetics at interfaces. The consequence is that along the interface of the two oxide layers, the release is faster than it is inside of each layer. The etching front of the interface layer etch has typically a wedge-like shape as shown in figure 3C, which – like the topology based etch – deviates strongly from the isotropic behaviour. In consequence one has to investigate the actual kinetics for each individual design to provide the best release process since the ratio of surface areas to sacrificial volume as well as the structure shape is very individual for different MOEMS designs.

![Figure 3](image3.jpg)

**Figure 3.** Schematic (left) and representative SEM images (right) of the release processes. (A) Isotropic Etch, (B) topology based etch, (C) interface layers etch.

![Figure 4](image4.jpg)

**Figure 4.** SEM image taken in oblique view showing the topology based etch on top of the hinge structures without deposited mirrors (inset).

The actual kinetics comes into account for the etching of the mirror array of the device. However, a big part of the device outside the mirror array has no significant topology but offers a high open area. Etching of the sacrificial layer in this area therefore takes more time. Even if the mirrors are completely released and fully movable, it is possible, that SiO₂ is still remaining on the device as it is shown schematically in figure 5. This remaining SiO₂ can possibly cause charging effects, which could have a negative influence on the operation of the device.

![Figure 5](image5.jpg)

**Figure 5.** Schematic top view on an SLM device. In contrast to the bond pad and the mirror array area, the outer chip area (black dotted area) does not have any surface topology and etching rate is lower. As a consequence SiO₂ can partly remain on the surface.
2.2. Residues

Another issue, which becomes important with the release kinetics, are residues from the sacrificial layer, which remain after the release process. Their shape can be string-like as shown in figure 6 or also tend to be canvas-like depending on the actual release kinetics. Often the residues contain carbon, probably from the TEOS, together with fluorine, oxygen and maybe boron and small amounts of other elements as can be measured using EDX as seen in figure 7. Since they are not solved in HF or later plasma treatments, they may stay in the device even for later operation. At this point, they may affect general performance or functionality in terms of restriction of single mirrors. We assume, that they agglomerate at the border, at which two etching fronts meet in the later release process. By changing the shape of the structure under the mirror one can influence the velocity and shape as well as possible numbers and direction of movement for etching fronts at a certain point. A very popular method to decrease the HF release duration is to use additional holes in the mirror. Having an optimized number and arrangement of these release holes can significantly change the release kinetics and consequently the position, where possible residues occur. Even though IPMS has developed several remedies to solve the residue issue afterwards the release process, avoiding it by pushing residues from crucial to non-crucial positions is the most promising one and provides a significant increase of the performance of the SLM device.

![Figure 6. SEM-image of a typical residue on the mirror backside taken after the HF release.](image1)

![Figure 7. Analysis of a mirror backside affected by residues by energy dispersive X-ray spectroscopy. The full spectrum is shown as black line, while the red bars are calculated as the difference between an affected and an unaffected area.](image2)

2.3. Protection of the CMOS

Although the use of SiO₂ as sacrificial layer material has many benefits for the MOEMS part of the device, it can be unfavourable for the CMOS part. Since SiO₂ is also used for insulating layers inside the CMOS, these layers have to be protected during the release process. Therefore an effective barrier layer between the top electrode layer and the inter-layer dielectrics is necessary. From different possible materials, which are HF inert and electrical insulating [6], [7], we chose Al₂O₃ as best suited for our needs. Since it showed less defects and better coverage, Al₂O₃ prepared by atomic layer deposition (ALD) is superior to sputtered one. Devices prepared with an etch stop from ALD-Al₂O₃ did not show any hint of etching attack to the CMOS from MOEMS side. As shown in figure 8, the USG underneath the Al₂O₃-layer still exists without visible damage, while the air gap is fully released.
3. Summary
We presented details of how SiO₂ is used as sacrificial layer material in our fabrication process for multi-level MOEMS devices. After a brief introduction to the layout and the used preparation techniques, the HF release kinetics was investigated. It was shown, that isotropic etching is only one mechanism at the very beginning of the release process, while the later process is dominated by two anisotropic mechanisms caused by topology and interfaces. However the release kinetics has a significant impact on the occurrence and position of residues, still present under the mirror after the HF release. Since they can affect the movability of the mirrors, it is proposed to use and optimize the etch kinetics with respect to each individual MOEMS design for a better performance of the device.

As a second goal we presented effective methods to protect the CMOS backplane during the release by using an ALD-Al₂O₃ etching barrier underneath the address electrode and a double-seal ring made of metal on the edges of the diced chip.

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