Studying the Effect of Stray Capacitance on the Measurement Accuracy of the CVT Based on the Boundary Element Method

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1.Introduction

The Capacitor Voltage Transformer (CVT) has high dielectric strength, fast transient response, wide dynamic range, low power consumption, and nonferromagnetic resonance with power systems. It also can reduce the head steepness of lightning shock and be used as a coupling capacitor for the power carrier communication [1-4]. Thus, it is widely applied in power systems from 35 to 1000 kV. Especially, in the high voltage of 110 kV and above, its market share is over 90%. The measurement accuracy of CVT is one of the key parameters for ensuring the safe and stable operation of the power system. The IEC-60044-5:2004 standard defines the measurement accuracy classes of a single-phase CVT are 0.2, 0.5, 1.0, and 3.0 [5]. It means that, for the highest class 0.2, the measurement accuracy of CVT, which is generally equivalent to the voltage difference ratio (VDR), must be below 0.2%. Stray capacitance affects the performance of high-voltage devices seriously, such as voltage dividers, insulator strings, modular power supplies, and measuring instruments [6]. Thus, it must be considered in the design of high-voltage devices. The stray capacitances of the CVT to ground and other charged parts play an important role in causing the VDR of the CVT [7]. Especially for the CVT applied in the ultra-high-voltage level, the effect of stray capacitance on its VDR is more serious [8]. For instance, the VDR of CVT which applied in the 750 kV power system caused by the stray capacitor is larger than 0.2% [9]. It exceeds the requirement of class 0.2. Therefore, it is urgent to study the influence of stray capacitance on the VDR of CVT and explore solutions to reduce the adverse effect of stray capacitance, so as to ensure the safe and stable operation of the power system.
In recent years, various works have already been carried out for studying the effect of stray capacitance on the electric performance of a high-voltage device. The stray capacitor and the impulse voltage distributions of the HVDC converter valve are calculated by the field-circuit coupling method [10]. The difference between the calculated and experimental voltages is less than 0.1%. Some researchers study the influence of stray capacitance on the voltage distribution of the insulator string [11–13]. The results show that stray capacitance caused the inhomogeneous distribution of insulator string voltage. The electric stress on the insulator close to the power line is obviously higher than that close to the tower. A grading ring [14] and metal electrodes [15] can homogenize the voltage distribution effectively. The stray capacitance can also affect the voltage distribution of breaks for the multibreak vacuum circuit breaker [16, 17]. For a three-break circuit breaker, the partial voltage of high-voltage break exceeds 60% due to the effect of stray capacitance of the low-voltage break to ground. It may result in the breaking failure for the short current. Paralleling capacitances across breaks can improve the uniformity of break voltage distribution effectively. The effects of the stray capacitor on the performance of a high-voltage arrestor are studied in [18–20]. J. Li et al. [18] calculated the stray capacitance, total leakage current, resistive leakage current, and phase angle difference of arresters by the finite-element method. The interphase interference from stray capacitance can be eliminated by the iterative algorithm based on the resistance-capacitance network model. He et al. [20] analysed the electric potential distribution of the 1000-kV MOV based on an idea of field-circuit combination, i.e., the 3D finite-element method and circuit-analytic method. The nonuniform coefficient of potential distribution can be reduced to within ±5% by installing the grading ring and parallel capacitors.

But, up to now, there are few studies about the effect of stray capacitance on the CVT. For the CVT applied in the 750-kV voltage level and above, the stray capacitance of the CVT to the high-voltage terminal increases the VDR of the CVT more than 0.1% [21]. Installation of a grading ring for a new UHV equipotential shielding CVT can improve the voltage distribution and compensate for the adverse effect caused by stray capacitance [3]. Furthermore, the rated bulk capacitances of this UHV CVT are derived under the interference of stray capacitances [7]. They are much less than those of the traditional CVT without a grading ring for the same accuracy class. The research results can reduce the manufacturing difficulty and cost. The measurement precision of the CVT is affected by stray capacitance and temperature [22]. It can be reduced to 0.1% by choosing large bulk capacitances and resistances with low temperature coefficient. The influence of stray capacitance on the VDR of the CVT is analysed by the field-circuit coupling method with the assumption of the homogenous distribution of stray capacitance [2, 23]. However, the distribution of stray capacitance is inhomogenous in fact. The abovementioned analysis results are not accurate. Reference [24] reviews the calculation methods of the stray capacitance of the CVT, but due to the complex structure of the CVT, it is a failure to solve the stray capacitance by the surface charge method.

Although great progress has been made for the research of the CVT, it is still hard to analyse the effect of stray capacitance on the VDR of the CVT accurately and quantitatively due to the complex configuration of the CVT [25], the difficulty in the experimental measurement of stray capacitance directly [26], and the variation of stray capacitance with the installation location of the CVT [27].

The purpose of this paper is to present a new calculation method of stray capacitance and further analyse the effect of stray capacitance on the VDR of the CVT. In this context, a model based on the boundary element method (BEM) is established to calculate the stray capacitance of the capacitance voltage divider (CVD). The voltage distribution of the CVD is obtained by the equivalent circuit model of the CVD. The reliability of the method is confirmed by comparing the calculated voltage with experimental measured results. Then, the effect of stray capacitance on the VDR of the CVT is analysed. Finally, the structure and parameters of the shield are optimized to further reduce the VDR of the CVT. The research results can contribute to design the high-precision CVT more efficiently.

2. Structure and Operation Principle of the CVT

Currently, the most widely applied of CVT in the power system has a column structure as shown in Figure 1. It consists of two parts: a capacitance voltage divider (CVD) and electromagnetic unit (EMU).

The CVD is mainly composed of a high-voltage capacitor, a medium-voltage capacitor, an external metal expander, and a porcelain insulator. Both of the high- and medium-voltage capacitors consist of dozens or hundreds of capacitance units in series. Each capacitance unit is made of aluminum foil and insulating film which are stacked together and immersed in insulating oil [28–32]. The CVD converts a primary high voltage into a medium voltage ranging from 10–25 kV as the input voltage of the EMU. The EMU is made up of a compensation reactor, a medium-voltage transformer, and a damper. It is used to convert the medium voltage, i.e., the output voltage of the CVD, into a standard secondary voltage as the inputs of power meters and relay protection devices.

In general, the total VDR of the CVT depends on the CVD, EMU, the temperature shift, power frequency variation, and proximity effects. Among them, it is believed that the CVD and EMU are the main factors [7]. The EMU is poured in an aluminum alloy box as a whole, so it is hardly affected by the external electromagnetic interference (EMI). However, the CVD does not have any electromagnetic shield. It is easily affected by EMI. Therefore, in this paper, it is reasonable to ignore the EMU and only take the effect of the CVD on the VDR of the CVT into account. The VDR of the CVD is assumed to be approximately equal to that of the CVT. Besides, the VDR of the CVD depends mainly on the bulk capacitance, the stray capacitance of the CVD to ground and the high-voltage terminal [33–36]. Thus, in order to analyze the effect of stray capacitance on the VDR of the CVD, it is necessary to calculate the stray capacitance of the CVD accurately first.
3. Calculation of Stray Capacitance and Voltage Distribution

3.1. Calculation of Stray Capacitance Based on the BEM.
Firstly, the CVD is divided into \( n \) capacitance units. Then, the electric potential and the quantity of surface charges on unit \( i \) are set as \( \phi_i \) and \( Q_i \), \( i = 1, 2, 3, \ldots, n \), respectively. The low-voltage terminal of the CVD is usually connected to ground directly or via a drain coil with negligible impedance at rated frequency. So, it is assumed as the reference ground with 0 V electric potential. The surface charge, electric potential, and capacitance of all units satisfied the following relationship:

\[
\begin{bmatrix}
Q_1 \\
Q_2 \\
\vdots \\
Q_n
\end{bmatrix} =
\begin{bmatrix}
-C_{11} & -C_{12} & \cdots & -C_{1n} \\
-C_{21} & C_{22} & \cdots & -C_{2n} \\
\vdots & \vdots & \ddots & \vdots \\
-C_{n1} & -C_{n2} & \cdots & C_{nn}
\end{bmatrix}
\begin{bmatrix}
\phi_1 \\
\phi_2 \\
\vdots \\
\phi_n
\end{bmatrix}
\]

(1)

The abbreviation of equation (1) is \( Q = C \Phi \), where \( Q \) and \( \Phi \) are the column vectors of surface charge and electric potential of all units, respectively. \( C \) is the capacitance coefficient matrix of the CVD. The off-diagonal element \( C_{ij} \) or \( C_{ji} \) \((i, j = 1, \ldots, n, i \neq j)\) is the mutual capacitance of unit \( i \) to unit \( j \).

The diagonal element \( C_{ii} \) is the sum of the stray capacitance of unit \( i \) to ground \( C_{ig} \) and the mutual capacitances of unit \( i \) to other units. Hence,

\[
C_{ig} = C_{ii} - \sum_{j=1}^{n} C_{ij} \,(i \neq j)
\]

(2)

The absolute value of the element in the first column of matrix \( C \), i.e., \( C_{1i} \) \((i = 2, 3, \ldots, n, i \neq 1)\), is the stray capacitance of unit \( i \) to the high-voltage terminal.

The main calculation methods of electrostatic field are the finite-element method (FEM) and the BEM. The BEM describes the mathematical and physical problems with boundary integral equations and solves them by the discrete technique of the FEM. It has higher accuracy than the FEM [37, 38]. Hence, this article adopted the BEM to calculate the stray capacitance of the CVD.

Firstly, the electric potentials of unit \( i \) and other units were assumed to be 1 V and 0 V, respectively. From equation (1), if the total quantity of surface charges on each unit was known, the elements in column \( i \) of \( C \) can be obtained. In this case,

\[
C_{ij} = Q_j, \quad j = 1, 2, \ldots, n.
\]

(3)

Secondly, the lateral surface of all capacitance units were divided into \( m \) patches. The total charges on each unit were assumed to be scattered homogeneously on its patches. Hence, the electric potential \( \phi_k \) at the center position \( x_k \) of patch \( k \) \((k = 1, 2, \ldots, m)\) is as follows:

\[
\phi_k = \phi_{ko} + \phi_{kl}
\]

where \( \phi_{ko} \) and \( \phi_{kl} \) are the electric potentials at point \( x_k \) generated by the charges on patch \( k \) and patch \( l \) \((l = 1, 2, \ldots, m \text{ and } l \neq k)\), respectively.

\[
\phi_{ko} = \frac{0.2821 \sigma_k}{\varepsilon_0 \sqrt{A_k}} = \frac{0.2821}{\varepsilon_0 \sqrt{A_k}} q_k,
\]

(5)

where \( \varepsilon_0 \) is the vacuum permittivity, \( A_k \) is the area of patch \( k \), and \( \sigma_k \) and \( q_k \) are the density and quantity of charges on patch \( k \), respectively.
Referring to equation (7), the charges on each patch of other units was set to be 1 V and 0 V, respectively.

For all patches, equation (6) can be rewritten in the following matrix form:

\[ pq = \varphi, \]

where \( p \) is a parameter matrix \((m \times m)\), \( q \) is the column vector \((m \times 1)\) of the quantity of charges on all patches, and \( \varphi \) is the column vector \((m \times 1)\) of the electric potential of all patches.

Then, the electric potential of all patches of unit \( i \) and that of other units was set to be 1 V and 0 V, respectively. Referring to equation (7), the charges on each patch \( q_k \) can be obtained. Next, substituting \( q_k \) into equation (3), the elements in column \( i \) of \( C \) were obtained as follows:

\[ C_{ji} = Q_j = \sum_{k \neq j} q_k, \quad j = 1, 2, \ldots n. \]

By repeating the abovementioned processes, the capacitance coefficient matrix \( C \) can be solved. Then, the stray capacitances of units to ground and the high-voltage terminal were obtained correspondingly.

In Section 3.2. Calculation of Voltage Distribution of the CVD. After obtaining the stray capacitance, the voltage distribution of the CVD was calculated in this part. Each capacitance unit was regarded as a voltage node. The electric potential of the node at the high-voltage terminal was assumed to be \( U_1 \), and the low-voltage terminal was grounded directly. Taking the stray capacitance of units to ground and the high-voltage terminal into account, the equivalent circuit of the CVD was obtained, as shown in Figure 2. Here, \( C_i \) is the capacitance of unit \( i \), \( C_{ih} \) is the stray capacitance of unit \( i \) to ground, and \( C_{sh} \) is the stray capacitance of unit \( i \) to the high-voltage terminal, and it replaced the parameter \( C_{1i} \) in Section 3.3.

The node voltage equation of the CVD is as follows:

\[ Y_B U = I, \]

where \( U \) is the node voltage column vector, \( U = [U_1, U_2, \ldots, U_n]^T \). \( I \) is the current column vector, \( I = [I_1, I_2, \ldots, I_n]^T \).

From Figure 2, any element \( I_i \) of \( I \) can be derived:

\[ I_i = \begin{cases} I_i, & i = 1, \\ j\omega[(U_{i-1} - U_i)C_{i-1} + (U_1 - U_i)C_{ih}], & i = 2, 3 \ldots n. \end{cases} \]

Also, the node admittance matrix \( Y_B \) can also be derived:

\[
Y_B = \begin{bmatrix}
-y_{11} + y_{12} + \sum_{j=2}^{n} y_{1j} & -y_{12} & \cdots & -y_{1n} \\
-y_{21} & -y_{22} + y_{2j} & \cdots & -y_{2n} \\
\vdots & \ddots & \ddots & \vdots \\
-y_{n1} & \cdots & -y_{nn} + y_{nj} & -y_{nn}
\end{bmatrix},
\]

where \( y_{ni} \) is the self-admittance of unit \( n \), \( y_{ni} = j\omega C_{ni}, \omega = 100\pi \).

\( y_{nh} \) is the admittance of unit \( n \) to the high-voltage terminal, \( y_{nh} = j\omega C_{nh} \). \( y_{ng} \) is the admittance of unit \( n \) to ground, \( y_{ng} = j\omega C_{ng} \).

Substituting equations (10) and (11) into equation (9), the column vector of node voltage \( U \) was solved, and then, the voltage distribution of the CVD was obtained correspondingly.

3.3. Method Verification. The previous two sections presented the calculation method for the stray capacitance and the voltage distribution of the CVD. Next, we verify the proposed method by comparing the calculated result with the experimentally measured result.

The experimental schematic diagram of CVD voltage measurement is shown in Figure 3. \( U_1 \), the high-power-frequency input voltage of the CVT, is generated by using a frequency series resonance device, \( U_i \) is the power grid voltage, \( T_1 \) is the excitation transformer, \( U \) is the output voltage of \( T_1 \), \( R \) is the current limiting resistor, and \( L_1 \) is the adjustable reactor. The output voltage of the CVD is measured by using the voltage transformer calibrator.

The test platform of the CVT is shown in Figure 4. The voltage transformer calibrator model is PT101 with the following parameters: the measuring accuracy is up to 0.002%, and the measuring range is 0–60 kV. The frequency series resonance device model is MEXB-108. Its main structure and electrical parameters are as follows: the input voltage of the excitation transformer is 400 V, the output voltage is 6 kV, and \( L_1 \) is an adjustable reactor with an adjustable range of 0–110 H. \( C_f \) is a series resonant capacitance with 1000 pF. The test CVT model is TYD110/0.01H. Its main structure and electrical parameters are as follows: the height of the CVD is 1.15 m, the output voltage of the CVD must be within the range of 15 kV to 25 kV to prevent damage to the insulation of the EMU, thus the adjustable position of the medium-voltage tap from ground is 0.162 m to 0.253 m (default position is 0.24 m), the average radius of...
the CVD is 0.30 m, the CVD is made up of 50 capacitance units in series (i.e., \( n = 50 \)), and its total capacitance value is 10000 pF (where the high-voltage capacitor \( C_1 = 12574 \) pF and medium-voltage capacitor \( C_2 = 48853 \) pF).

When \( U_1 = 110 \) kV and the total number of patches of all units \( m = 1000 \), the voltage distribution of the test CVD is calculated and shown in Figure 5. Adjusting the position of the middle-voltage tap, the measured voltages at four different positions are also illustrated in Figure 5.

The comparison of calculated voltages, measured voltages, and their maximum deviation rates at four different positions is shown in Table 1. The measured voltage is the average value of six measurements. When the measurement number is six and the confidence probability is 0.95, the measurement uncertainty is \( 1.5 \times 10^{-3} \) kV. As can be seen from Table 1, at the default position of the medium-voltage tap, the calculated and measured voltages are 22.459 kV and 22.461 \pm 1.5 \times 10^{-3} \) kV, respectively. The maximum voltage difference is 0.0034 kV, and the deviation rate of voltage is as low as 0.0015%. For the four selected measurement positions, the maximum deviation rate of voltage is only 0.021%, and the average deviation rate of voltage is as low as 0.015%. Therefore, the method proposed in this paper had high accuracy, and it is suitable for calculating the stray capacitance and the voltage distribution of the CVD.

4. Results and Discussion

4.1. Effect of Stray Capacitance on Voltage Distribution and VDR of the CVD. Figure 6 presents the stray capacitances of each unit to ground and the high-voltage terminal. As we can see from this, from the high-voltage terminal to ground, \( C_g \) increases rapidly from 28 pF to 123 pF and \( C_h \) decreases...
slowly from 56 pF to 8 pF. Near the low-voltage terminal, $C_g$ is much larger than $C_h$. But, near the high-voltage terminal, the difference between $C_g$ and $C_h$ is not obvious. This may result in the inhomogeneous distribution of CVD voltage.

The voltage drop on each capacitance unit of the test CVD is illustrated in Figure 7.

As shown in Figure 7, the voltage drop on the capacitance unit of the test CVD is not uniform. From the high-voltage terminal to the low-voltage terminal, it decreases rapidly from 2.36 kV to 2.12 kV. This is mainly attributed to the large $C_g$ near the low-voltage terminal.

The expression of VDR is as follows [2]:

$$ VDR = \frac{K_N U_{\text{out}} - U_1}{U_1} \times 100\% $$  (12)

where $U_{\text{out}}$ is the output voltage of the CVD and $K_N$ is the ideal partial voltage ratio of the CVD.

$U_{\text{out}}$ can be changed by adjusting the position of the medium-voltage tap. Within the adjustable range of the medium-voltage tap (0.162 m to 0.253 m from ground), the VDR of the CVD is shown in Figure 8. As we can see, the VDR reduces linearly from 0.292% to 0.273% with the increase of the medium-voltage tap position. At the default position of the medium-voltage tap, the VDR is 0.276%. Although the VDR of the CVD can be reduced by adjusting the position of the medium-voltage tap, it is still higher than the requirement of class 0.2 which specified in the IEC-60044-5:2004 standard.

### 4.2. Effect of the Shield on the VDR of the CVD

As stated above, due to the effect of stray capacitance, the VDR of the test CVD exceeded the requirement of class 0.2 even adjusting the position of the medium-voltage tap. Some studies indicate that the metal shield and grading ring can compensate for the effect of stray capacitance, improve the distribution of electric field, and boost the voltage endurance and insulation strength of the high-voltage apparatus accordingly [14,15,39]. In this section, we analyze the effect of the shield on the VDR of the test CVD and optimize the structure parameters of the shield to reduce VDR further.

Three types of shield are designed for the test CVT in this study. They are A type (only one shield installed on the high-voltage terminal), B type (only one shield installed on the low-voltage terminal), and C type (two shields installed on both of the high- and low-voltage terminals), as shown in Figure 9. $L$ and $l$ are the lengths of the shield on the high- and low-voltage terminal, respectively. $D$ and $d$ are the distances from the shield on the high- and low-voltage terminal to the axis of the CVD, respectively. The default parameters of the shield are $L = 230$ mm, $D = 75$ mm, $l = 430$ mm, and $d = 100$ mm. The shields are metallic cylindrical layers made of copper, and their thickness is 2 mm.

Figure 10 illustrates the effects of the shield with default parameters on the voltage distribution and VDR of the CVD. It is shown that, for all of the CVDs with the shield, the voltage distributions are more uniform and VDR is smaller than the CVD without shield. Among the three types of

| Position (m) | Measured voltage (kV) | Calculated voltage (kV) | Maximum deviation rate of voltage (%) |
|-------------|----------------------|------------------------|--------------------------------------|
| 0.18        | 16.840 ± 1.5 × 10^{-3} | 16.842                 | 0.021                                |
| 0.20        | 18.706 ± 1.5 × 10^{-3} | 18.707                 | 0.013                                |
| 0.22        | 20.582 ± 1.5 × 10^{-3} | 20.581                 | 0.012                                |
| 0.24        | 22.461 ± 1.5 × 10^{-3} | 22.459                 | 0.015                                |

### Table 1: Comparison of calculated and measured voltages at four different medium-voltage tap positions.
Figure 7: Voltage drop on each capacitance unit of the test CVD.

Figure 8: VDR of the CVD at different medium-voltage tap positions. The "+" and "-" before the value on the vertical axis represent the positive deviation and the negative deviation, respectively.

Figure 9: Three types of shield.
Figure 10: Effect of the shield type on the voltage drop and VDR of the CVD. (a) Voltage drop. (b) VDR.

Figure 11: Effect of shield parameters on VDR. (a) $L$ varies from 100 mm to 500 mm, $D = 75$ mm, $l = 430$ mm, and $d = 100$ mm. (b) $D$ varies from 50 mm to 200 mm, $L = 240$ mm, $l = 430$ mm, and $d = 100$ mm. (c) $l$ varies from 100 mm to 500 mm, $L = 240$ mm, $D = 100$ mm, and $d = 100$ mm. (d) $d$ varies from 50 mm to 200 mm, $L = 240$ mm, $D = 100$ mm, and $l = 320$ mm.
shield, the C-type shield is the best choice. As shown in Figure 10(a), the voltage drop on the capacitance unit of the CVD with the C-type shield is the most uniform. Specifically, the maximum voltage drop reduces from 2.31 kV (A type) to 2.24 kV (C type) while the minimum voltage drop increases from 2.12 kV (A type) to 2.16 kV (C type). In addition, Figure 10(b) shows that, for the CVD with a C-type shield, its VDR is the smallest. For instance, the VDR decreases from 0.261% (A type) to 0.192% (C type) at the default position of the medium-voltage tap. As we can also see from Figure 10(b), the VDR of the CVD with a C-type shield varies from 0.204% to 0.191% within the adjusting range of the medium-voltage tap position. Moreover, the VDR is less than 0.2% within the range of 0.20 m to 0.25 m from ground. It satisfies the requirement of class 0.2. But, it does not have an adequate margin.

To reduce the VDR of the CVD further, the optimization of structure parameters of the C-type shield is performed. Due to the internal insulation requirement and technology limitations of the CVT, the adjustable ranges of $L$ and $l$ are limited within 100~500 mm, $D$ and $d$ are limited within 50~200 mm.

The minimum VDR is the optimization goal. The optimization strategy is to optimize one of the parameters $L$, $D$, $l$, and $d$ in turn. During each optimization, the previous optimization results are used as default parameters, and the unoptimized parameters are defaults. The optimization results of parameters are shown in Figure 11.

As can be seen from Figure 11, all parameters $L$, $D$, $l$, and $d$ affect the VDR of the CVD. But, compared with $D$ and $L$, the effects of $l$ and $d$ are more obvious. Specifically, from Figure 11(a), when $L$ varies from 100 mm to 500 mm, other parameters are defaults, the minimum VDR = 0.18%, and here, $L = 240$ mm. As shown in Figure 11(b), when $D$ varies from 50 mm to 200 mm, $L = 240$ mm; meanwhile, other parameters are defaults, the minimum VDR = 0.165%, and here, $D = 100$ mm. As illustrated in Figure 11(c), when $l$ varies from 100 mm to 500 mm, $L = 240$ mm and $D = 100$ mm; while other parameters are defaults, the minimum VDR = 0.12%, and here, $l = 320$ mm. As shown in Figure 11(d), when $d$ varies from 50 mm to 200 mm, $L = 240$ mm, $D = 100$ mm, and $l = 320$ mm, the minimum VDR = 0.08%, and here, $d = 150$ mm.

According to the analysis mentioned above, the optimization of parameters for the C-type shield improves VDR greatly. The VDR of the CVD was reduced from about 0.2% before optimization to only 0.08% after optimization. Compared with the requirement of class 0.2 (0.2%), it has an adequate margin.

5. Conclusions and Future Work

This paper proposed a method based on the boundary element method and the equivalent circuit of the CVD to calculate the stray capacitance and voltage distribution of the CVD. Then the effect of stray capacitance on the VDR of the CVD was studied. At last, the structure and parameters of the shield were optimized to reduce the VDR of the CVT further. The following conclusions can be drawn:

1. The proposed method has high precision. The average deviation rate between calculated voltage and experimental measured voltage was only 0.015%. It is a useful and reliable tool for the calculation of stray capacitance and the voltage distribution of the CVD.

2. For the test CVT, although its VDR was reduced from 0.292% to 0.273% by adjusting the position of the medium-voltage tap, it still did not satisfy the requirement of class 0.2.

3. All of the three types of shield reduced the VDR of the CVD effectively, in particular the C-type shield. After the optimization of structure parameters for the C-type shield, the VDR was reduced from about 0.2% to only 0.08%. The optimization results of shield parameters were $L = 240$ mm, $D = 100$ mm, $l = 320$ mm, and $d = 150$ mm.

The research work in this paper can be used as a reference for studying the effect of stray capacitance on the performance of the CVD and is helpful to the optimal design of a high-precision CVT. However, the measurement accuracy of the CVT is affected by numerous and complex factors, and only the key factor of stray capacitance was considered in this paper. In future, we will focus on the effects of other factors on the measurement accuracy of the CVT, such as the phase-to-phase interference, the dielectric loss of the capacitor unit, the temperature shift, and the variation of power frequency.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

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