Towards a full integration of vertically aligned silicon nanowires in MEMS using silane as a precursor

G Gadea\(^1\), A Morata\(^1\), J D Santos\(^1\), D Dávila\(^1,2,3\), C Calaza\(^2\), M Salleras\(^2\), L Fonseca\(^2\) and A Tarancón\(^1\)

\(^1\) Catalonia Institute for Energy Research (IREC), Jardins de les Dones de Negre 1, 08930 Sant Adrià de Besòs, Barcelona, Spain
\(^2\) IMB-CNM (CSIC), Institute of Microelectronics of Barcelona, Campus UAB, 08193 Bellaterra, Barcelona, Spain
\(^3\) ETHZ, Micro and Nanosystems, Department of Mechanical and Process Engineering, Tannenstrasse 3, 8092 Zurich, Switzerland

E-mail: atarancon@irec.cat

Received 7 December 2014, revised 3 March 2015
Accepted for publication 18 March 2015
Published 23 April 2015

Abstract
Silicon nanowires present outstanding properties for electronics, energy, and environmental monitoring applications. However, their integration into microelectromechanical systems (MEMS) is a major issue so far due to low compatibility with mainstream technology, which complicates patterning and controlled morphology. This work addresses the growth of (111) aligned silicon nanowire arrays fully integrated into standard MEMS processing by means of the chemical vapor deposition–vapor liquid solid method (CVD–VLS) using silane as a precursor. A reinterpretation of the galvanic displacement method is presented for selectively depositing gold nanoparticles of controlled size and shape. Moreover, a comprehensive analysis of the effects of synthesis temperature and pressure on the growth rate and alignment of nanowires is presented for the most common silicon precursor, i.e., silane. Compared with previously reported protocols, the redefined galvanic displacement together with a silane-based CVD–VLS growth methodology provides a more standard and low-temperature (<650 °C) synthesis scheme and a compatible route to reliably grow Si nanowires in MEMS for advanced applications.

Online supplementary data available from stacks.iop.org/NANO/26/195302/mmedia

Keywords: silicon, nanowires, silane, gold, aligned, integration

1. Introduction

Lately, semiconductor nanowires have been attracting a great deal of interest due to their exceptional electronic, mechanical, photonic, electrochemical, and thermal properties, which make them potentially suitable for a wide range of applications such as field effect transistors [1–3]; chemical sensors [4–6]; optoelectronics [7–9]; energy storage [10–12]; and photovoltaic, piezoelectric, and thermoelectric power harvesting systems [13–18]. Nevertheless, it is frequently difficult to access these nanostructures to take advantage of their properties. Microtechnology makes it possible to bridge the gap between the macroscale and the nanoscale. Microelectromechanical systems (MEMS) are able to incorporate and exploit nanometric structures to produce a functional output for different applications. Since microtechnology batch production techniques are silicon based, much attention has
been paid to silicon nanowires due to their potential compatibility and integrability, not to mention their remarkable properties and the high availability of silicon precursors [19–25]. The method chosen for growing and integrating nanowires into a microelectronic device must fit properly in the entire fabrication process and not damage or compromise its functionality. Although many attempts have been made, a simple method that is fully compatible with current mainstream technology has not been developed so far.

Bottom-up integration of silicon nanowires usually involves (i) a selective deposition of metallic seeds for catalytic action and proper patterning and (ii) a growth process based on exposure to a silicon precursor gas [26]. Among other seeds, gold is the most commonly used mainly because of its high silicon solubility and low Au–Si system eutectic point (363 °C), which allow growth at temperatures from 400 to 900 °C [27]. The seed deposition method is an important step because it determines the size of the nanowires and the position where they will grow. Galvanic displacement has been proposed as a simple selective technique for metal thin film generation on silicon or other metal semiconductor substrates [28–44]. This versatile technique consists of simply immersing (dipping) the solid substrate into a noble metal precursor bath so that a redox reaction takes place, dissolving the substrate and precipitating the metal at the solid–liquid interphase. This fast, spontaneous reaction occurs exclusively at conducting or semiconducting surfaces, which makes it possible to selectively deposit metal on a surface with the help of oxide or nitride insulating masks. An adaptation of this technique, so-called microemulsion galvanic displacement, has been developed for depositing gold on silicon. By adding a surfactant and an organic immiscible solvent to the aqueous dipping solution, micelles containing the metal precursor are formed. This makes it possible to obtain not continuous films, but arrays of gold nanoparticles of controlled size and density on exposed silicon surfaces by means of a simple dipping procedure [34]. These nanoparticles act as seeds for the epitaxial growth of nanowires in the presence of adequate precursors through the so-called vapor liquid solid (VLS) mechanism that takes place in a chemical vapor deposition (CVD) reactor typically employed in the microelectronics industry [26, 45].

Another advantage of the galvanic displacement method compared with other techniques used to selectively define VLS seeds, like photolithography and microcontact printing [46, 47], is its capability to conformally cover a surface. This makes it possible to cover uneven surfaces or structures with the high aspect ratio usually present in MEMS. Combined with CVD–VLS, growth on walls or micro-trenches permits the in-plane fabrication of high-density arrays of horizontally aligned nanowires. When growing between two walls, double clamped nanowires are formed with epitaxial junctions on both sides, thus providing mechanically strong and electrically conductive connections [48–50]. These good-quality contacts between two separated regions make it possible to access the electrical properties of the nanowires, overcoming a typical difficulty of devices that use a non-planar architecture [18].

Thus, the combination of microemulsion galvanic displacement with CVD–VLS synthesis constitutes a useful route for implementing nanowires monolithically into microelectronic devices while controlling their properties, including the diameter and density, which are the key aspects for the performance of most nanoware-based devices. A few works have recently been devoted to using this combination for growing (111) aligned silicon nanowires by using silicon tetrachloride as a precursor [35, 42], including one by the authors reporting the first integration of Si NWs in a thermoelectric microgenerator [18]. However, a lack of knowledge of the formation mechanism of gold nanoparticles and, therefore, poor reproducibility of the size and density of seeds strongly limits the applicability of this methodology in mass production applications. In addition, the use of silicon tetrachloride represents an important limitation since this is not a mainstream precursor in microelectronics and necessitates an elevated growth temperature (>800 °C), which is hard to compatibilize with typical MEMS fabrication.

In this work, the galvanic displacement and CVD–VLS methods have been employed to grow vertically aligned arrays of silicon nanowires on silicon substrates using silane as the precursor. A comprehensive study of the formation and tailoring of seed micropatterns generated by galvanic displacement is presented together with the effect of the most important growth parameters for fine-tuning the morphology of the nanowires. The use of silane allows reduction of the growth temperature while using a mainstream technology. The most salient factors in the deposition–growth process are described, stressing the influence of crucial steps to achieve a reproducible, robust method for the integration of morphology-controlled silicon nanowires in microdevices.

2. Experimental setup

2.1. Galvanic displacement

Polished 1 cm² silicon chips exposing a (111) crystal plane were used as a substrate. First the chips were immersed for 5 min in hydrofluoric acid (HF) 5% w/w to remove the native oxide. The chips were then rinsed with deionized water and isopropanol and dried with compressed nitrogen. Afterwards, they were dipped in gold microemulsions.

The gold microemulsions were prepared by mixing an aqueous solution with an organic phase. The aqueous solution consisted of deionized water with 0.01 M NaAuCl₄ and 0.2 M HF, whereas the organic phase consisted of n-heptane with 0.33 M sodium bis(2-ethylhexyl) sulfosuccinate (AOT, a surfactant). Upon mixing these two phases, reverse micelles were formed with a size controlled by the so-called R parameter [34]:

$$ R = \frac{[\text{H}_2\text{O}]}{[\text{AOT}]} $$

(1)

where [H₂O] and [AOT] are the total concentrations of water and AOT in the solution, respectively. Note that the amount of gold present in the microemulsion is directly proportional

2
to \( R \). The two phases were mixed in different volume proportions so as to prepare microemulsions with \( R \) values of 21, 84, and 168, with aqueous to organic phase volume ratios of 1:8, 1:2, and 1:1 respectively. Once prepared, these solutions were immersed in an ultrasonic bath for 30 min.

The deposition was performed in recently sonicated microemulsion. The deposition time \( (t_{\text{dep}}) \) was varied in the range from 30 s to 30 min to analyze its effect on the gold deposit.

Following each deposition, the chips were immersed in three subsequent cleaning baths of acetone, deionized water, and isopropanol and dried with compressed nitrogen. Then the samples were annealed in air at 400 °C for 30 min to remove the remaining surfactant, with both heating and cooling ramps of 20 °C min\(^{-1}\). Thermogravimetry experiments (not shown here) revealed that most of the AOT is removed when samples are annealed under these conditions.

Occasionally, the chips were cleaned with acetone at 45 °C and organic etchant solution (consisting of a 3:1 volume mixture of concentrated sulphuric acid hydrogen peroxide) after galvanic displacement to observe the effects of removing AOT by means other than heating.

### 2.2. Nanowire growth in a CVD system

Prior to nanowire growth, the gold-seeded chips were immersed in HF 5% w/w for 5 min to remove the thermal oxide that could have been formed during the annealing process. The chips were then rinsed with deionized water and isopropanol and dried with compressed nitrogen. After HF cleaning the chips were transferred into a tubular CVD reactor (EasyTube® 3000 from FirstNano) for silicon nanowire growth using silane as the precursor. The reactor was brought to growth conditions in a hydrogen atmosphere. Hydrochloric acid was flowed for 5 min before the injection of silane and maintained during growth to prevent structural defects derived from gold segregation [51]. The nanowires were grown at pressures from 2.5 to 20 Torr and temperatures from 520 to 725 °C for growth periods (i.e., periods of exposure to silane) from 15 to 60 min. The flow rates employed during growth were 1000, 15, and 150 sccm for hydrogen, hydrochloric acid, and diluted silane (10% in hydrogen), respectively.

### 2.3. Characterization

Scanning Electron Microscopy (SEM) images were obtained using a Carl Zeiss Auriga 60 microscope to characterize the samples at different stages (gold seeds and silicon nanowires). Energy-dispersive x-ray spectroscopy (EDX) (Oxford Instruments X-Max) was occasionally used to determine the sample composition and analyze regions of interest.

Gold nanoparticle size, density (nanoparticles \( \mu \text{m}^{-2} \)), and shape were determined by processing top-view SEM images of the seed chips. ImageJ software was used to statistically analyze the samples [52]. The particles were adjusted to ellipses, and each one was assigned a size (defined as the diameter of a circular particle with the same area would have) and an aspect ratio (defined as the major axis divided by the minor axis). With the distribution data, mean area-weighted values of size and aspect ratio were assigned to each sample. The value of dispersion following the size is the standard deviation of the distribution.

The length and diameter of the grown nanowires were determined by SEM image processing as well. Mean values and standard deviations were calculated by measuring at least 20 nanowires of each representative cross-section image (i.e., sections with the nanowires within the image plane). Measurements of nanowire diameters were performed at the midpoint of the wire length. Densities (nanowires \( \mu \text{m}^{-2} \)) were determined by examining samples from a top view and counting only vertical nanowires.

A Carl Zeiss Libra 120 kV transmission electron microscope (TEM) was employed for imaging nanowires and obtaining electron diffraction patterns to study their structure and crystallinity. The nanowires were extracted from their substrates by sonication in ethanol at 40 °C for 15 min and dispersed in a TEM copper/graphite grid.

To study the crystallinity of the gold deposited on silicon substrates by galvanic displacement during a thermal annealing process, an x-ray diffraction (XRD) experiment was performed with a Bruker AXS D8 Advance diffractometer, with Cu Kα radiation (\( \lambda = 1.5406 \text{ Å} \)). The system was equipped with an Anton Paar XRK 900 high-temperature chamber for \( \textit{in situ} \) XRD measurements. Two theta measurements were performed at different temperature steps in the range of 30–80 °C. The chamber was heated from 25 to 400 °C at 20 °C min\(^{-1}\), with a stabilization dwell of 30 min, and cooled back to 25 °C at 20 °C min\(^{-1}\).

### 3. Results and discussion

#### 3.1. Gold seeding by microemulsion galvanic displacement

##### 3.1.1. Gold seed size control

Figure 1 shows SEM images of seed patterns obtained by galvanic displacement and calcination when changing two parameters, namely, \( R \) (i.e., gold amount in the microemulsion) and dipping time \( (t_{\text{dep}}) \). SEM–EDX mapping (not presented here) confirmed that bright particles were associated with gold deposition onto silicon. Homogeneous dispersions along the chip surface with particle dimensions ranging from 10 to 600 nm were observed. It is clear from the figure that increasing both the \( R \) value and \( t_{\text{dep}} \) results in growth of the particle size.

Figure 2(a) shows the size of the deposited seed particles as a function of \( R \) for a fixed dipping time of 30 s. The same plot includes values reported for similar deposition conditions obtained by Magagnini et al [34] and Gao et al [35]. An increase in mean size and statistical dispersion (error bars) with \( R \) is observed to be in good agreement with results reported in the literature. There is a certain degree of discrepancy, possibly due to the different methodology employed to calculate particle size, namely, XRD (Magagnini et al) and statistical analysis of SEM images (this work, Gao et al).
Figure 1. Top view of gold nanoparticles over \( \langle 111 \rangle \) silicon chips. Samples were prepared by dipping in microemulsions with different \( R \) values during different dipping times \( (t_{\text{dip}}) \), specified at top and left.

Figure 2. (a) Size variation of particles deposited by means of galvanic displacement with parameter \( R = [\text{H}_2\text{O}]/[\text{AOT}] \), which is proportional to the gold amount present in the microemulsion. Data from Magagnin et al [34] and Gao et al [35] are shown for comparison. The dipping time \( (t_{\text{dip}}) \) is 30 s in all cases. (b) Size variation of particles deposited by means of galvanic displacement with \( t_{\text{dip}} \) for various \( R \) values shown in the legend. Dips of 30 s, 5 min, and 30 min were performed. The error bars show the standard deviation of the distributions. The dotted lines are guides for the eye.
Figure 2(b) gathers the statistical data obtained from the samples in figure 1, showing particle size variation with \( t_{\text{dip}} \) and \( R \). A great increase in mean particle size and standard deviation is clearly observed for longer dippings and higher values of \( R \).

The strong effect of the dipping time suggests that control of the size and shape does not depend only on the nature of the microemulsion, i.e., the \( R \) parameter, as suggested by Magagnin et al. [34]. According to this reference, the origin of the formation of a nanoparticle is a single primitive micelle attached to the silicon substrate, so the final size is not dependent on the dipping time. Our results are more compatible with a mechanism involving multiple-layer deposition of micelles, with time controlling the final particle size.

3.1.2. Particle formation mechanism from galvanic displacement deposition of gold. Figure 3 presents SEM images from a sample with \( R=168 \) and \( t_{\text{dip}}=30 \) s before and after calcination at 400 °C. Before calcination, the gold deposit over the silicon forms a disordered pattern in which individual particles cannot be distinguished (figure 3(a)). As better appreciated in the inset this pattern is a dense, rough film comprising agglomerated crystallites with sizes of tens of nanometers. Possible organic residues remaining from galvanic displacement did not affect gold film imaging (see supplementary information). On the other hand, well-defined particles are visible after sample calcination (figure 3(b)); they are much larger, with a smoothed surface.

The results observed in figure 3 suggest that particle formation is driven by a thin film dewetting process. During galvanic displacement, a disordered thin film of gold is deposited over the silicon chip. During calcination, when the film is heated to 400 °C, a reduction in the total surface energy leads to the generation of particles and smooth patterns.

To confirm this mechanism, several \( R=168 \) samples were annealed at different temperatures (figure 4). As the annealing temperature was increased, the film passed from a dense pattern (figure 4(a)) to a bicontinuous pierced one (figure 4(b)); the latter evolved to a pattern of elongated particles (figures 4(c) and (d)), which eventually became elliptical particles at 400 °C (figure 4(e)).

XRD analysis of the samples during a heating ramp to 400 °C shows that galvanically displaced gold on silicon presents crystallinity before, during, and after the annealing process. Moreover, crystallite size increases throughout the process. This crystallinity increase is retained after the sample is cooled back to room conditions (see supplementary information).

As expected for a dewetting process, the higher the temperature, the faster the process, and thus the closer will be the particles to their final equilibrium (spherical) shape [53]. This confirms the mechanism proposed here of the formation of nanoparticles from the galvanic displacement of gold. In a 400 °C annealing the dewetting process starts well below the eutectic point of the silicon–gold system (363 °C) and ends beyond it. Thus, there is an initial phase of solid-state dewetting (ruled by gold surface self-diffusion) and a second phase of liquid-state dewetting (controlled by fluid film hydrodynamics) [54]. Although solid-state dewetting of dense gold films (sputtered or evaporated) is typically observed at
higher temperatures and higher annealing times [55], in this case it can be noticed under milder conditions (250–350 °C, figures 4(b)–(d)). This is thought to happen due to the high surface provided by the rough pattern of the dewetted film (figure 3(a)), which greatly enhances the kinetics of the process.

To emulate the sample state just before the nanowire growth takes place inside the CVD, different samples were treated with an additional annealing step at 600 °C and 2.5 Torr in hydrogen during 30 min, with the same heating ramp used during the growth process. No changes were observed with respect to figures 1–3, calcinated at 400 °C. This indicates that, during the calcinations, once the eutectic is formed (at T > 363 °C), the particles quickly adopt their final shape (due to the fast nature of liquid-state dewetting) and do not further evolve. Thus, the presented images show the particles as they are prior to silane exposure within the CVD reactor.

Summarizing, contrary to previously reported explanations [34], we propose that micelles in solution allow size control not only by serving as individual scaffolds for the particles to grow inside but rather by acting as a dispersant agent for the gold precursor. Microemulsion galvanic displacement allows the deposition of a rough, high-surface gold pattern over exposed silicon surfaces, the thickness of which increases with \( t_{\text{dip}} \) and \( R \). Upon dewetting—which is also thought to take place thanks to the good degree of dispersion —thicker films give rise to larger particles [53], thus enabling control over the size distribution.

### 3.1.3. Gold seed aspect ratio and density control

Figure 5 shows the dependence of density (particles per \( \mu \text{m}^2 \)) and aspect ratio of the seed particles of figure 1 on \( R \) and \( t_{\text{dip}} \). The aspect ratio was calculated by dividing the major axis by the minor axis of the ellipse that was adjusted to each particle. As \( R \) or \( t_{\text{dip}} \) (i.e., the deposited film thickness) increases, the density dramatically decreases and the aspect ratio increases. Both parameters are fairly homogeneous along the computed particles. (Standard deviations of the measures are <5% in all cases.)

In a dewetting process, the final particle density is known to decrease with increasing initial film thickness. Greater thickness also implies slower dewetting kinetics, i.e., higher annealing times required for the sample to pass from figures 4(a) to (e) [53]. For the same time and annealing temperature, thicker films will therefore present higher aspect ratio particles (far from their final shape). In extreme cases, the pattern will even look bicontinuous, such as in figures 4(b)–(c). The trends shown in figure 5 are then as expected for the dewetting of a film with increasing thickness, which further confirms the results previously discussed; i.e., higher \( R \) and dipping times lead to the deposition of thicker gold films that subsequently dewet during calcination.

### 3.2. VLS silicon nanowire growth by CVD

#### 3.2.1. Gold seed influence

Figure 6 shows SEM images of nanowires grown under the same conditions on different patterned gold samples with \( R = 21 \), \( R = 84 \), and \( R = 168 \) (\( t_{\text{dip}} = 30 \text{ s in all cases} \)). This dipping time was chosen to obtain nanowire diameters in the vicinity of 100 nm. Table 1 displays statistical data extracted from SEM images, showing the relationship of \( R \) to the dimensions and density of the resultant seeds and nanowires. It can be seen that when the value of \( R \) is increased (i.e., when the gold seed size is increased), better-quality arrays are obtained since their density, length, and degree of alignment in the \( \langle 111 \rangle \) direction also increase. TEM analysis confirmed the crystallinity and alignment of the nanowires in the \( \langle 111 \rangle \) direction and revealed hemispherical gold particles at the tips (see supplementary information). Treating the sample with hydrofluoric acid prior to loading it into the CVD was found to be necessary for growing aligned nanowires (see supplementary information).

As typically reported for nanowires grown by the VLS mechanism, their diameters are larger than those of the
original seeds. The reason is that the seeds expand when they become a droplet of gold–silicon alloy since they must incorporate the volume corresponding to the infiltrated silicon \[56\]. As seen in previous works the proportional diameter increase is higher with small particles because they reach a higher degree of supersaturation during the VLS process \[57, 58\].

The striking difference between the density of the gold seeds on the substrate (\(\sim 100\) nanoparticles \(\mu m^{-2}\)) and the corresponding vertically aligned nanowires (\(\sim 1\) nanowire \(\mu m^{-2}\)) is due mainly to two effects: (i) a kinetic hindrance renders seeds with sizes below a certain critical diameter unable to grow nanowires in the conditions employed; (ii) the dependence of the diameter on the direction of growth means that only the largest seeds are able to promote \(\langle 111\rangle\) (i.e., vertical) nanowires. Therefore, decreasing \(R\) has two opposing effects regarding aligned nanowire density: an increase in the number of potential nanowires per unit area due to the increase in seed density but a decrease in the probability of each seed giving rise to a vertical nanowire due to its smaller size, which implies higher kinetic hindrance and lower \(\langle 111\rangle\) growth direction preference.

The decrease in average length and density with small nanowire diameters has been previously reported and explained as being due to surface energy issues: small diameters imply a higher surface-derived energy barrier (Gibbs–Thomson effect), which lowers the growth speed. At very small sizes (very high nucleation barriers), this growth can even be kinetically blocked, which explains the decrease in density \[58, 59\]. In addition, when the nanowire diameter is small, there is higher relative importance of the lateral faces, and other preferential directions for growing appear, with the \(\langle 111\rangle\) family not being the most probable anymore. This fact explains the loss in verticality as proposed by Schmidt et al \[60\].

### 3.2.2. Growth time and growth rate

Figure 7 plots the lengths of the nanowires in samples with \(R=168\) and
\[ t_{\text{dip}} = 30 \text{s} \] at fixed pressure and temperature while varying the growth time \( t_g \) (i.e., time of exposure to silane). SEM images (supplementary information) show that the nanowires vary only in length, maintaining the good degree of alignment shown in figure 6(c). The length of the wires increases linearly with \( t_g \). The nanowires within all samples are fairly homogeneous in length, with standard deviations <5%, as expected for an \( R = 168 \) sample (see table 1). For this reason, standard deviation is not considered and thus not shown in the plots of length and growth rate in this work.

The negative intercept of the adjusted linear fit can be associated with an initial step in which no growth occurs. As proposed by Schmid et al this so-called nucleation time is thought to be the time that the liquid alloy droplet needs to be exposed to silane before reaching critical supersaturation and starting VLS growth [46]. In our case, the small value of the latter (\( \sim 100 \) s) under the most unfavorable conditions (i.e., large seeds and low silane pressure) produces a minimal influence on the growth rate values (less than 5%).

### 3.3. Growth pressure effect on verticality

Figure 8 shows nanowires grown in samples with \( R = 168 \) and \( t_{\text{dip}} = 30 \) s at fixed temperature and growth time and at different pressures. In figure 9, the corresponding growth rate is displayed as a function of silane partial pressure. Silane partial pressure (silane pressure for short) is assessed instead of the total pressure because it makes it possible to compare reference data and it has been reported as the parameter influencing the growth rate [56]. Mean nanowire diameter values are plotted as a function of silane pressure in figure 10(a).

As the silane pressure increases, the growth rate increases linearly (figure 9) and the wire alignment in the \( \{111\} \) directions decreases (figure 8). The experimental growth rate values are in fair agreement with data from other works, being perhaps slightly higher than expected. Nanowire diameter does not seem to follow a clear trend with pressure, having a wide distribution from 50 to 140 nm and a mean value of \( \sim 100 \) nm, as expected for a sample with \( R = 168 \) (see table 1).

The decrease in the wire alignment in the vertical \( \{111\} \) direction with increasing pressure is in agreement with the results of Lugstein et al and Schmid et al, who reported other preferred growth directions and increasing kinks with increasing total pressure and silane partial pressure [56, 61]. The linear dependence of the growth rate on pressure as determined herein, which suggests the existence of a first-order dependence of the growth rate on silane partial pressure, has been previously reported by several authors [46, 63–65].

### 3.4. Growth temperature influence

Figure 11 shows nanowires grown in samples with \( R = 168 \) and \( t_{\text{dip}} = 30 \) s at fixed pressure and growth time and at different growth temperatures. Figure 12 shows the corresponding growth rate as a function of temperature. Values
from other works are included for comparison. The mean nanowire diameter variation with temperature under these conditions is plotted in Figure 10(b).

As seen in Figures 10–12, nanowire diameter, \( \langle 111 \rangle \) alignment, and growth rate increase with increasing growth temperature. The growth rate values agree with the reference data shown in Figure 12(a). The Arrhenius representation (Figure 12(b)) reveals a thermally activated process with an activation energy of 15.3 ± 0.7 kcal mol\(^{-1}\). This value is consistent with data from references [46, 62, 66], wherein values of 14.3, 17.7, and 19 kcal mol\(^{-1}\), respectively, were obtained.

In Figure 11, the quality and the homogeneity of the nanowires grown at 630–725 °C and 2.5 Torr and with an \( R = 168 \) substrate can be appreciated. According to the observed tendencies, even better alignment could be expected at lower silane pressures and with larger gold seeds. The high degree of alignment seen in the inset in Figure 11(d) and in the TEM analysis (see supplementary information) confirms the epitaxial nature of the growth. The density of the vertical nanowires calculated from a top-view image of the 725 °C sample is approximately 1 nanowire/\( \mu m^2 \), i.e., four times lower than that obtained from growing at 600 °C (Table 1).

Although the diameter of grown nanowires does not seem to be affected by silane partial pressure, it is clearly affected by temperature, increasing from 65 ± 18 nm at 520 °C to 204 ± 60 nm at 725 °C (Figure 10). This is consistent with results from D Kwak et al., who also noticed an increase in nanowire diameter with temperature but not with pressure [65]. These authors also reported a decrease in nanowire density and thus suggested that these effects could be explained by the coalescence of either gold–silicon eutectic droplets during heating or silicon nanowires at an early stage of growth. In the present work, both effects were observed as well, but no agglomeration was seen when annealing gold nanoparticle substrates at 600 °C in hydrogen (see section 3.1.2). For this reason, it is probable that thickening is triggered by exposure to silane. If this is the case, the increase in diameter would be driven by the coalescence of early-stage nanowires rather than gold–silicon alloy droplets.

Finally, a tangle of silicon deposit close to the substrate surface was observed in Figures 11(c)–(d). This layer—or rather a primal form of it—is actually present in all samples, but it grows thicker with the amount of silicon deposited, and thus it could be clearly appreciated only under these fast growth conditions. Although removing this layer may not be trivial (its formation is thought to be linked to galvanic-displacement-seeded VLS nanowires; see supplementary information), it may not even be necessary since its presence does not seem to disturb the growth of aligned nanowires to a severe degree.

4. Conclusions

Vertically aligned silicon nanowires were obtained by combining microemulsion galvanic displacement with gold-catalyzed CVD–VLS synthesis using silane as the precursor. Both methods were systematically studied in order to gain control of the morphology of the obtained nanowires (i.e., length, diameter, and alignment), with emphasis on the most critical steps.

The size, shape, and density of the gold nanoparticles prepared by microemulsion galvanic displacement were found to be dependent not only on the microemulsion, as previously reported in the literature, but also on the deposition time and posterior annealing. By changing these parameters, particle sizes ranging from 10 to 600 nm with densities from 25 to 1000 particles \( \mu m^2 \) were obtained. A mechanism of particle formation has been proposed based on a dispersive gold deposition followed by dewetting. This mechanism explains the trends of particle size, density, and roundness with all the studied parameters, as well as the pattern evolution of the samples annealed at different temperatures.

Regarding the CVD–VLS process, a comprehensive study at different growth temperatures (520–725 °C) and
silane partial pressures (2.5 mTorr–256 mTorr) was undertaken. Aligned silicon nanowires with diameters (controlled by those of the gold seeds) between 25 and 200 nm and lengths from 2 to 30 μm were grown. The resultant density of the ⟨111⟩ aligned grown nanowires was strongly dependent on seed particle size, increasing along with it. Treating the sample with hydrofluoric acid prior to loading it into the CVD was necessary for growing aligned nanowires. Nanowire length increases linearly with growth time, and nucleation time was found to be insignificant for our growth conditions. The growth rate is strongly dependent on pressure and temperature in the studied ranges, increasing with both of them and varying from 100 to 1600 nm min⁻¹. The growth rate follows a linear tendency with silane partial pressure and an exponential tendency with temperature, with an activation energy of 15.3 ± 0.7 kcal mol⁻¹. The growth rate and activation energy values are in fair agreement with other published works, where similar conditions were used. The diameter of the grown nanowires was not affected by silane pressure but was indeed affected by growth temperature. A tangled layer of silicon was observed to grow close to the substrate, especially in high-temperature growths. Alignment of nanowires toward the ⟨111⟩ direction increased with decreasing silane pressure and increasing temperature. Fairly aligned nanowires were obtained at 600–700 °C and at 2.5–128 mTorr of silane partial pressure. In these conditions, the nanowires exhibited mean diameters in the range 100–200 nm and a density of approximately 1 nanowire μm⁻².

The present work offers the required guidelines for rendering microemulsion galvanic displacement linked to the CVD–VLS technique a reproducible and robust methodology.
suitable for the integration of controlled nanowires into MEMS. The possibility of patterning, contacting, and finely controlling the size and morphology of silicon nanowires together with the use of silane as a silicon precursor opens the possibility of employing mainstream technology for the mass production of advanced devices based on this fascinating and abundant nanomaterial.

Acknowledgments

This work was financially supported by the 7th Framework program under the project SiNERGY (FP7-NMP-SMALL-2013-604169) and by the European Regional Development Funds (ERDF, FEDER Programa 2007–2013 Competitivitat de Catalunya).

References

[1] Zhu H, Li Q, Yuan H, Baumgart H, Ioannou D E and Richter C A 2012 Self-aligned multi-channel silicon nanowire field-effect transistors Solid State Electron. 78 92–6
[2] Yao Z, Sun W, Li W, Yang H, Li J and Gu C 2012 Dual-gate field effect transistor based on ZnO nanowire with high-K gate dielectrics Microelectron. Eng. 98 343–6
[3] Cha H Y, Wu H, Chandrashekhar M, Choi Y C, Chae S, Koley G and Spencer M G 2006 Fabrication and characterization of pre-aligned gallium nitride nanowire field-effect transistors Nanotechnology 17 1264–71
[4] Lu N, Gao A, Dai P, Li T, Wang Y, Gao X, Song S, Fan C and Wang Y 2013 Ultra-sensitive nucleic acids detection with electrical nanosensors based on CMOS-compatible silicon nanowire field-effect transistors Methods 63 212–8
[5] Son J Y, Lim S J, Cho J H, Seong W K and Kim H 2008 Synthesis of horizontally aligned ZnO nanowires localized at terrace edges and application for high sensitivity gas sensor Appl. Phys. Lett. 93 053109
[6] Shen Y, Yamazaki T, Liu Z, Meng D and Kikuta T 2009 Hydrogen sensors made of undoped and Pt-doped SnO2 nanowires J. Alloys Compd. 488 L21–5
[7] Han S, Jin W, Zhang D, Tang T, Li C, Liu X, Liu Z, Lei B and Zhou C 2004 Photoconduction studies on GaN nanowire transistors under UV and polarized UV illumination Chem. Phys. Lett. 389 176–80
[8] Chen K J, Hung F Y, Chang S J and Young S J 2009 Optoelectronic characteristics of UV photodetector based on ZnO nanowire thin films J. Alloys Compd. 479 674–7
[9] Konenkamp R, Word R C and Schlegel C 2004 Vertical nanowire light-emitting diode Appl. Phys. Lett. 85 6004
[10] Li L et al 2014 One-dimension MnCo2O4 nanowire arrays for electrochemical energy storage Electrochim. Acta 116 467–74
[11] Chan C K, Peng H, Liu G, McIlwrath K, Zhang X F, Huggins R A and Cui Y 2008 High-performance lithium battery anodes using silicon nanowires Nat. Nanotechnology 3 31–5
[12] Pan H, Luo J, Sun H, Feng Y, Poh C and Lin J 2006 Hydrogen storage of ZnO and Mg doped ZnO nanowires Nanotechnology 17 2963–7
[13] Rao H A, Wu W Q, Liu Y and Xu Y F 2014 CdS/CdSe co-sensitized vertically aligned anatase TiO2 nanowire arrays for efficient solar cells Nano Energy 8 1–8
[14] Garnett E C and Yang P 2008 Silicon nanowire radial p-n junction solar cells J. Am. Chem. Soc. 130 9224–5
[15] Liu J, Fei P, Zhou J, Tummala R and Wang Z L 2008 Toward high output-power nanogenerator Appl. Phys. Lett. 92 173105
[16] Zhu G, Yang R, Wang S and Wang Z L 2010 Flexible high-output nanogenerator based on lateral ZnO nanowire array Nano Lett. 10 3151–5
[17] Wang W, Jia F, Huang Q and Zhang J 2005 A new type of low power thermoelctric micro-generator fabricated by nanowire array thermoelctric material Microelectron. Eng. 77 223–9
[18] Dávila D, Tarancón A, Calaza C, Salleras M, Fernández-Regúlez M, S Paulo A and Fonseca L 2012 Monolithically integrated thermoelctric energy harvester based on silicon integrated nanowire arrays for powering micro/nanodevices Nano Energy 1 812–9
[19] Peng K, Wang X and Lee S-T 2008 Silicon nanowire array photoelectrochemical solar cells Appl. Phys. Lett. 92 163103
dependence of growth rate and delay in growth Appl. Phys. Lett. 96 133109

[63] Lew K K and Redwing J M 2003 Growth characteristics of silicon nanowires synthesized by vapor–liquid–solid growth in nanoporous alumina templates J. Cryst. Growth 254 14–22

[64] Bootsma G A and Gassen H J 1971 A quantitative study on the growth of silicon whiskers from silane and germanium from germane J. Cryst. Growth 10 223–34

[65] Kwak D W, Cho H Y and Yang W C 2007 Dimensional evolution of silicon nanowires synthesized by Au–Si island-catalyzed chemical vapor deposition Physica E 37 153–7

[66] Latu-Romain L, Mouchet C, Cayron C, Rouviere E and Simonato J P 2008 Growth parameters and shape specific synthesis of silicon nanowires by the VLS method J. Nanopart. Res. 10 1287–91

[67] Lugstein A, Steinmair M, Hyun Y J, Hauer G, Pongratz P and Bertagnolli E 2008 Pressure-induced orientation control of the growth of epitaxial silicon nanowires Nano Lett. 8 2310–4

[68] Morin C, Kohen D, Tileli V, Faucherand P, Levis M, Brioude A, Salem B, Baron T and Perraud S 2011 Patterned growth of high aspect ratio silicon wire arrays at moderate temperature J. Cryst. Growth 321 151–6

[69] Vincent L, Boukhicha R, Gardès C, Renard C, Yam V, Fossard F, Patriarche G and Bouchier D 2011 Faceting mechanisms of Si nanowires and gold spreading J. Mater. Sci. 47 1609–13