An Efficient Partial Sums Generator for Constituent Code based Successive Cancellation Decoding of Polar Codes

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Abstract—This paper proposes the architecture of partial sum generator for constituent codes based polar code decoder. Constituent codes based polar code decoder has the advantage of low latency. However, no purposefully designed partial sum generator design exists that can yield desired timing for the decoder. We first derive the mathematical presentation with the partial sums set $\beta^*$ which is corresponding to each constituent codes. From this, we concoct a shift-register based partial sum generator. Next, the overall architecture and design details are described, and the overhead compared with conventional partial sum generator is evaluated. Finally, the implementation results with both ASIC and FPGA technology and relevant discussions are presented.

I. INTRODUCTION

Recently, polar code [1] has received increasing attentions because it is the first code which provably achieves the channel capacity. Its low-complexity encoding and decoding schemes make it very promising for practical application. There are three widely known algorithms for polar codes decoding. E. Arikan in [1] presents a successive cancellation (SC) algorithm which can successively accomplish decoding with recursive cancellation. I. Tal [2] makes the SC algorithm more competitive by exploring more paths among the codewords tree; this method is referred as list successive cancellation (LSC). Also, N. Hussami et al. in [3] shows that the belief propagation (BP) method is referred as list successive cancellation (LSC). Also, Arikan in [1] presents a successive cancellation (SC) algorithm which is corresponding to each constituent codes. From this, we concoct a shift-register based partial sum generator. Next, the overall architecture and design details are described, and the overhead compared with conventional partial sum generator is evaluated. Finally, the implementation results with both ASIC and FPGA technology and relevant discussions are presented.

Although many efforts have been made for BP decoder [4], [5] and [6], the BP decoding still suffers from the problem of high computing complexity. Thus, SC and LSC attract more studies especially on their hardware architecture [7] [8] [9] [10] [11] [12]. SC decoding is based on the architecture [7] [8] [9] [10] [11] [12]. SC decoding can be regarded as a binary tree traversal as successful cancellation to estimate channels.

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described in Fig. 1. The number of bits of one node in stage $m (m = 0, 1, 2, \ldots \log_2 n)$ is equal to $2^m$. $\alpha$ stands for the soft reliability value, typically is log-likelihood ratio (LLR). Each left and right child nodes can calculate the LLR for current node via $f$ and $g$ functions, respectively [7]. However, in order to solve $g$ function, a feedback $\beta_i$ from left child of the same parent node is needed. This kind of feedback is called partial sum. At stage 0, $\beta$ of a frozen node is always zero, and for information bit its value is calculated by threshold detection of the soft reliability according to

$$\beta = h(\alpha) = \begin{cases} 
0, & \text{if } \alpha \geq 0 \\
1, & \text{otherwise}
\end{cases} \quad (1)$$

At intermediate stages, $\beta$ can be recursively calculated by

$$\beta[i] = \{ \beta[i] \oplus \beta[i] \text{ if } i \leq N^m / 2 \} \quad (2)$$

B. Constituent codes based SC decoding

SC decoding generally suffers from the high latency due to its inherent serial property. The processing of obtaining the partial sum from each node significantly constrains the decoding speed. Thus, in order to reduce the latency caused by partial sum calculation, constituent code based SC decoding has been proposed [7], [13]. By finding some certain patterns in the source code, some part of the codeword and their corresponding partial sums can be estimated immediately without traversal. This method significantly reduces the partial-sum-constrained latency. $N^0$, $N^1$, $N^{SPC}$ and $N^{REP}$ are the four commonest constituent code.

$N^0$ and $N^1$ only contain either frozen bits or information bits, respectively. For $N^0$ codes, we can set the corresponding partial sums to 0 immediately. For $N^1$ node, the partial sums can be directly determined via threshold detection Eq. 1. $N^{SPC}$ and $N^{REP}$ contain both frozen bits and information bits. In the $N^{SPC}$ codes, only the first bit is frozen. It makes the length $n$ constituent codes as a rate $(n - 1)/n$ single parity check (SPC) code. This kind of code can be decoded by performing parity check with the least reliable bit. Typically it is the one with the minimum absolute value of LLR. In the $N^{REP}$ codes, only the last bit is information bit. In this case, all the corresponding partial sums should be the same since they all are the reflection of the last information bit. Thus, the decoding algorithm starts by summing all input LLRs and the partial sums are calculated by performing the hard detection to the final summary. Fig. 2 shows an example of how constituent code can simplify the SC decoding tree. According to T. Che’s implementation of constituent code based SC decoder [19], the latency of length $n$ constituent code can be reduced from $2n - 2$ to 1. $\log_2 n + 1$ and $\log_2 n$ for $N^0$, $N^1$, $N^{SPC}$ and $N^{REP}$ codes, respectively. In order to further optimize the performance constituent codes based decoder, a specific designed PSG for it is very necessary.

C. Shift-register-based partial sums generator

Among all the aforementioned PSGs design, shift-register-based PSG (SR-PSG) has a better performance in terms of both the timing and hardware complexity. For length $n$ polar decoder, it consists of $n$ registers and some other simple combination logic. Along with the estimation of each $\hat{u}_i$, the registers perform shift calculation and the partial sums can be obtained from their corresponding register. Its architecture is illustrated in Fig. 3. This architecture is built according to the following rule:

$$\begin{aligned}
R_0 &\leftarrow \hat{u}_i \cdot c_{i,0} \\
R_k &\leftarrow R_{k-1} \oplus (\hat{u}_i \cdot c_{i,k}), \quad \text{if } k \geq 0
\end{aligned} \quad (3)$$

where $\cdot$ and $\oplus$ stand for and exclusive-or operation, respectively. In Fig. 3 $R_0$ means the 0th register, $\hat{u}_i$ means the $i$th estimated bit, $\beta_{i,j}$ means the $j$th partial sum in stage $i$. $c_{i,k}$ means the $k$th row and $i$th column in the generate matrix $G$. The matrix generation unit is able to generate $c_{i,k}$ with very simple logic. The SC decoder consists of many basic computation parts called processing unit (PU). Each partial sum needs to be feed into the corresponding PU. The shift register based architecture can guarantee that all partial sum required by a PU are all generated in the same register, which can avoid any extra routing logic in the circuit.

Such architecture is able to receive the estimated bit and update the corresponding partial sum by every valid cycle,
which is highly consistent with SC decoding processing. However, this architecture is not suitable for constituent codes based SC decoder since some partial sums are obtained directly instead of calculating from estimated bits. Thus, a PSG for constituent codes based SC decoder should have the capability to generate the new partial sums from either the directly got intermediate partial sums or the estimated bits, and to maintain the coherence of them.

### III. Proposed Design

In this section, we first derive the mathematical presentation of constituent code based partial sum from Eq. (3). Then, the overall hardware architecture and subsequent design details are presented.

#### A. Mathematical Presentation

![Fig. 4. (a) Elements shift in generation matrix, and (b) diagonal cycle-shift in generation matrix](image)

For a length $n$ constituent code, its corresponding estimated bits and partial sums are denoted as $\hat{u}_{i,n-1}, \ldots, \hat{u}_i^c$ and $\beta_0^c, \ldots, \beta_{n-1}^c$, respectively. All the $\beta^c$ are obtained at the same time. For those bits that do not belong to any constituent codes, we still have to calculate their corresponding partial sums according to Eq. (3). Thus, if we still want to keep consistency between directly calculated intermediate partial sums and the one-by-one-estimated bits, we need to derive the mathematical presentation with $\beta^c$ from Eq. (3).

For $k \geq n$ and $k \in [a \cdot n, (a + 1) \cdot n - 1]$, $a = 1, 2, \ldots$, according to Eq. (3), we have

$$R_k = R_{k-1} \oplus (\hat{u}_i^c \cdot c_{i,k})$$

$$= R_{k-2} \oplus (\hat{u}_i^{c-1} \cdot c_{i-1,k-1}) \oplus (\hat{u}_i^c \cdot c_{i,k})$$

$$\cdots$$

$$= R_{k-n} \oplus [\hat{u}_{i,n-1}^c, \ldots, \hat{u}_i^c] \begin{bmatrix} c_{i-n+1,k-n+1} \\ \vdots \\ c_{i,k} \end{bmatrix}.$$ (4)

As we know, $c_{i,k}$ is the element of generation matrix $G$ which is the Kronecker power of $F = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$. Combine this property with our observation on the matrix, we conduct the following rule which is also noted in Fig. 4(a)

$$\begin{bmatrix} c_{i-n+1,k-n+1} \\ \vdots \\ c_{i,k} \end{bmatrix} = \begin{bmatrix} c_{i-n+1,(a+1)\cdot n-(k \ mod \ n)-1} \\ \vdots \\ c_{i,(a+1)\cdot n-(k \ mod \ n)-1} \end{bmatrix}.$$ (5)

According to the definition of generation matrix and concept of constituent code, when $c_{i,k} = 0$, the right part of Eq. (5) is equal to a all zero vector, and when $c_{i,k} = 1$ the right part of Eq. (5) is equal to the $(n - (k \ mod \ n) - 1)$th column in the generation matrix for length $n$ polar code. According to the definition of partial sum and Eq. (2), we get

$$[\hat{u}_{i,n+1}^c, \ldots, \hat{u}_i^c] \cdot [c_{i,n+1,p(k)}, \ldots, c_{i,p(k)}]^T = \beta_p(k)$$ (6)

where $p(k) = (n - (k \ mod \ n) - 1)$.

Now we apply the above observation back to Eq. (4). We define the vector $R_a = [R_{a,n}, \ldots, R_{a,n-1}]$ and $c_{i,a} = [c_{i,a,n}, \ldots, c_{i,a,n-1}]$ for $k \in [a \cdot n, (a + 1) \cdot n - 1]$, $a = 1, 2, \ldots$. We also define the vectors $\hat{u}_i^c = [\hat{u}_{i,n+1}^c, \ldots, \hat{u}_i^c]$ and $\beta^c = [\beta_0^c, \ldots, \beta_{n-1}^c]$. Then, we have

$$R_a = [R_{a,n}, \ldots, R_{a,n-1}]$$

$$= [R_{a-1,n}, \ldots, R_{a-1,n-1}] \oplus \begin{bmatrix} c_{i,n+1,a \cdot n+n+1} & \ldots & c_{i,n+1,a \cdot n} \\ \vdots & \ddots & \vdots \\ c_{i,a,n} & \ldots & c_{i,a,n-1} \end{bmatrix}$$

$$= [R_{a-1,n}, \ldots, R_{a-1,n-1}] \oplus \begin{bmatrix} \hat{u}_i^c \\ \vdots \\ \hat{u}_{i,p(a+1)}^c, \ldots, \hat{u}_i^c \end{bmatrix} \begin{bmatrix} c_{i,n+1,p(a+1)} & \ldots & c_{i,n+1,p(a+n-1)} \\ \vdots & \ddots & \vdots \\ c_{i,p(a+n-1)} & \ldots & c_{i,p(a+n-1)} \end{bmatrix}$$

$$= \bigg\{ \begin{array}{ll} 0, & \text{if } c_{i,a} = 0 \\ R_{a-1} \oplus \beta^c, & \text{if } c_{i,a} = 1 \end{array} \bigg\}.$$ (7)

For the consistent with Eq. (3), we rewrite Eq. (7) as follow:

$$R_a = R_{a-1} \oplus (\beta^c \& c_{i,a})$$ (8)

where $\&$ stands for the bit-wise and operation.

For $0 \leq k < n$, similar to Eq. (4), we have

$$R_k = [\hat{u}_{i-k,n}, \ldots, \hat{u}_i^c] \cdot [c_{i-k,0}, \ldots, c_{i,k}]$$ (9)

According to the definition of $G$ and constituent codes, we can conduct that for any length $n$ constituent codes, the first $n$ columns of its corresponding rows in $G$ should also be a generation matrix $G_n$ for length $n$ polar code. As described in Fig. 4(b) the diagonal cycle shift is same as each correspond column, and consider the $G_n$ is a lower triangular matrix, we get

$$[c_{i-n+1,k-n+1}, \ldots, c_{i-k,0}, \ldots, c_{i,k}]^T$$

$$= [c_{i-n+1,n-1-k}, \ldots, c_{i,n-k}]^T$$

$$= [0, \ldots, 0, c_{i-k-n+1-k}, \ldots, c_{i,n-k}]^T.$$ (10)

Thus, Eq. (9) can be rewritten as:

$$R_k = [\hat{u}_{i-k,n}, \ldots, \hat{u}_i^c] \cdot [c_{i-k,0}, \ldots, c_{i,k}]^T$$

$$= [\hat{u}_{i-n+1}, \ldots, \hat{u}_i^c] \cdot [0, \ldots, 0, c_{i-k,0}, \ldots, c_{i,k}]^T$$

$$= [\hat{u}_{i-n+1}, \ldots, \hat{u}_i^c] \cdot [c_{i-n+1,k-n+1}, \ldots, c_{i,n-k}]^T$$

$$= \beta_{n-k}^c.$$ (11)
has specific corresponding PU from each stage. They need constituent code based polar code. We can see each register by a re-configurable memory device like RAM for flexibility. Design complexity and hardware resource. It can be replaced code, it’s unnecessary to build an online generator for that. the constituent code. Due to the irregularity of the constituent code, where the generation matrix, where the inputs values to the right registers. The second difference is the shift function. According to Eq (12), instead of just shifting by one bit, the shifter should have the capability to shift n-bit where n is the length of constituent code. According to the definition of constituent code, n should be the any power of 2. Thus, A specific design (2^m−1)-bit shifter is proposed. The control signals for both the muxing networking and shifter are from the Control Signal Generator(CSG) with simple logic. The last difference is matrix generation unit. For each constituent code, its corresponding c_{i,j} should be the ith row of the generation matrix, where i is the index of the last bit in the constituent code. Due to the irregularity of the constituent code, it’s unnecessary to build an online generator for that. Thus, a pre-calculated ROM is placed. It is a trade-off between design complexity and hardware resource. It can be replaced by a re-configurable memory device like RAM for flexibility.

Fig. 6 shows an example of partial sum routing for 8 bit constituent code based polar code. We can see each register has specific corresponding PU from each stage. They need the multiplexing networking to route the partial sums to the each right register. For length n polar code, there are log_2 n stages in the decoder and n/2 registers in the SR-CB-PSG. If the multiplexing networking is built from the basic 2-bit MUX, each register is assigned an identical MUXs networking made by (log_2 n − 1) MUXs. All the networkings share the same control signal. According to its architecture, the control signals are the direct binary mapping of its stage index. In total, n/2 · (log_2 n − 1) MUXs are needed. Since the multiplexer networking needs to wait each PU finish computing to get the valid inputs, it is on the critical path of the decoder. Thus, it causes additional \( \lceil \log_2 \log_2 n \rceil \cdot \Delta(MUX) \) delay, where \( \Delta(MUX) \) is the delay for a single MUX.

For the (2^m−1) shifter, we proposed a barrel-shifter-based architecture. For length n polar code, m ≤ (log_2 n − 1). The shifter performs logic right shift. For k < n, where k is the index of the register and n is the length of the current constituent code, zeros are added to the left. For k ≥ n, we do shift. Those behaviors satisfy the first and second in Eq (12).

Fig. 7 shows an example of (2^m−1) shifter for 16-bit polar code decoder. All the MUXs in the same row can shall the same control signal. Those signals are generated by a k to 2^k decoder, where k = \( \lceil \log_2 \log_2 n \rceil \) for length n polar code. For length n polar code, there are (n/2−1)·(log_2 n − 1) MUXs are needed for the shifter. Since the shifter can start shift data without waiting PU to finish computing, it is not on the critical path. Thus, it should not deteriorate the timing performance of the decoder at all.

### IV. Implementation Results and Discussions
To the best of our knowledge, the proposed design is the first PSG design especially design for constituent codes based SC decoder. Thus, there is no reference design we can directly compare with. In this section, we list all the results we have and presents some relevant discussions.

| Table I. Critical Path Comparison |
|-----------------------------------|
| SR-PSG [14] | Proposed |
| Critical Path | \( \Delta(AND) + \Delta(XOR) \) | \( [\log_2 \log_2 N] \cdot \Delta(MUX) + \Delta(AND) + \Delta(XOR) \) |

Table I shows the critical path comparison between proposed PSG and the PSG in [14]. We can tell the delay overhead comes from the muxing network. Ideally, the maximum frequency of constituent codes based SC decoder is lower than that of conventional SC decoder. However, after taking the latency reduction into account, as shown in Table I.
constituent codes based SC decoder is able to achieve much higher throughput. The conventional SC decoder is referred from [9] which is the lowest latency conventional SC decoder to the best of our knowledge.

Table III shows the resource consumption estimation of proposed SR-CB-PSG for length $n$ polar code decoder and the comparison with other two conventional PSG. The most resource consumption part is the MUX since it used in both multiplexer networking and shifter. The estimation for the ROM size is based on the average calculation since the decoding latency changes along with the code rate.

| TABLE III. RESOURCE COMPARISON |
|--------------------------------|
| resource &                | proposed | [4]  | [8]  |
| DFF                     | $n/2$    | $n$  | $(n^2 - 4)/12$ |
| MUX                     | $(n - 1) \cdot (\log n - 1)$ | $n - 2$ | $n - 2$ |
| XOR                     | $n/2 - 1$ | $n/2 - 2$ | $n/2 - 1$ |
| AND                     | $n/2$    | $n/2$ | -       |
| ROM(bit)                | $n^2/10$ (average) | - | - |

The proposed design can be targeted on either ASIC or FPGA. We synthesized both with Nangate FreePDK 45nm process and on Xilinx Kintex-7 FPGA KC705 Evaluation board. Table IV shows the hardware resource of SR-CB-PSG for 1024 code length polar code decoder on both of them.

| TABLE IV. HARDWARE RESOURCE OF SR-CB-PSG FOR 1024 CODE LENGTH POLAR CODE DECODER |
|--------------------------------|
| Hardware Resource               | XC7K325T-2FFG900C FPGA | nanagate 45nm |
| slice LUTs                      | 1569 (<1%)               | 1569 µm$^2$  |
| slice RAMs                      | 512 (<1%)                |                 |
| area                            |                           |                 |

Noticeably, the architecture we discussed in this paper is based on the consideration for the worst case, which is that the maximum length of constituent codes could be $n/2$. However, for practical application, the maximum length of constituent is fix for certain code rate and usually cannot approach $n/2$. For those case, the logic of both the multiplexer networking and shifter could be even simpler, which will result in a better timing and silicon area performance.

V. CONCLUSION

This paper proposed an efficient PSG hardware design for constituent code based SC decoder. Conventional PSG is not compatible with the constituent code based SC decoder. This is because that the conventional one is only capable of taking estimated bit one by one but the constituent code based decoder is generated the intermediate partial sum directly. To solve this problem, we first derive the mathematical presentation for constituent code based PSG from the SR-PSG for conventional SC decoder. Then, the overall hardware architecture and design details are proposed. Finally, the implementation result with both VLSI and FPGA technology are presented, and the relevant discussions are carried out.

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