Top-Gated Carbon Nanotube FETs from Quantum Simulations: Comparison with Experiments

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Abstract—We present quantum simulations of carbon nanotube field-effect transistors (CNT-FETs) based on top-gated architectures and compare to electrical characterization on devices with 15 nm channel lengths. A non-equilibrium Green’s function (NEGF) quantum transport method coupled with a $k \cdot \vec{p}$ description of the electronic structure is demonstrated to achieve excellent agreement with the reported experimental data. Factors influencing the electrostatic control of the channel are investigated and reveal that detailed modeling of the electrostatics and the electronic band structure of the CNT is required to achieve quantitative agreement with experiment.

I. INTRODUCTION

Recent reports for CNT-FETs indicate performance targets for sub-5 nm technologies can be met [1]. In that work, electrical characterization and simulation for top-gated CNT-FETs is presented in which a long standing issue with nucleating high-$\kappa$ oxides on CNTs is overcome by deposition of an interfacial layer dielectric (ILX). Their CNT-FETs exhibit subthreshold swing values down to 65 mV/dec at 15 nm gate length while complying with gate leakage targets.

Due to difficulties in applying simple capacitance models commonly employed to describe Si CMOS operation and the need to consider various tunneling mechanisms, an approach combining detailed electrostatic modeling of the transistor geometry combined with a quantum treatment of charge transport and electronic structure are applied to determine current-voltage (IV) characteristics. Different approaches to the electrostatic modeling as well as an investigation of the electronic band structure are presented and related to subthreshold properties. The technology computer aided (TCAD) simulator QSim describes in detail the properties of these transistors without the requirement for high performance computing resources or long simulation times [2].

II. SIMULATION METHODOLOGY

A coupled mode-space non-equilibrium Green function (NEGF) solver is applied employing a $k \cdot \vec{p}$ electronic Hamiltonian capable of simulating the properties of CNT-FETs arranged in arbitrary 3D geometries. The QSim software package enables fast simulations of CNT-FETs including quantum mechanical treatment of elastic and inelastic phonon scattering. We validate our method by reproducing the experimentally measured transfer characteristics of devices fabricated as described in ref. [1]; we simulate top-gated devices based on (16,0) CNTs with 15 nm gate lengths and dimensions shown in fig. [1].

III. RESULTS

The transfer characteristics for the fabricated devices were measured at saturation $V_{DS} = 0.50$ V and in the linear $V_{DS} = 0.05$ V regions. Comparison of experimental measurements with three simulation schemes are shown in fig. [2] (a) a device without a back gate electrode having an intrinsic channel and chemically doped source/drain (S/D) extensions attached to ohmic contacts; (b) a similar device with a junctionless chemical doping scheme, and (c) a device employing electrostatic doping realised through a back-gate electrode with Schottky contacts on both ends of S/D extensions. Device (a) represents a commonly employed scheme for transistor simulations, while (b) and (c) describe configurations that are designed to increasingly match the actual experimental configuration. While all schemes are able to describe sub-$V_T$ swing degradation with increasing drain-source bias, simulations using chemical doping schemes are observed to predict better sub-$V_T$ performance. The model including electrostatic effects arising from the inclusion of back-gate electrode and metallic S/D contacts results in average sub-$V_T$ characteristics that closely track experimental results for both the linear and saturation regions. We note that although subthreshold swing values extracted from experimental data exhibit values below 80 mV/dec in some portions of the sub-$V_T$ characteristics, the values reported in fig. [2] correspond to averages over three orders of magnitude in current.

Figure [3] shows the local density of states and energy-resolved current at both leads for a state in the subthreshold region using simulation scheme (c). Current injected into the device at the source side shows two peaks corresponding to thermionic transport and source-to-drain tunnelling; although electronic occupations are significantly larger around the source Fermi level (zero of energy in Figure [3], the tunnelling barrier imposed at the channel results in both peaks exhibiting similar magnitude in the steady-state solution. As carriers travel through the CNT and interact with phonon modes both peaks become broadened and a new peak emerges through the drain extension due the availability of states at lower energies. After travelling the length of the drain extension most charge carriers have participated in phonon emission processes, as current reaching the drain electrode exhibits a
largest contribution at lower energies than available in the source extension.

Figure 4 compares extracted sub-$V_T$ swing values at each gate bias for simulated CNT-FETs with ILX thicknesses of 1.25 nm and 0.35 nm following the gate oxide description in ref. [1]. Our model estimates that a such a reduction in ILX thickness results in an improvement of around 10 mV/dec across the entire subthreshold region.

IV. CONCLUSION

CNT-FETs present excellent electrical characteristics for sub-5 nm technologies. However, details of their processing and their gate geometries require detailed electrostatic simulations to realistically capture physics behind their operation. Furthermore, features specific to the band structure of CNTs benefit from more advance treatments of the electronics structure. Phonon scattering and tunnelling mechanisms readily described within $\vec{k} \cdot \vec{p}$ enable quantitative predictions to be made at low computational effort.

To provide a validated treatment of the IV characteristics for the CNT-FET measured in ref. [1], a model including an explicit back gate to accurately model the electrostatics responsible for gate control of the channel was compared against more conventional simulation schemes. Finally, investigation of the ILX thickness reveals that if the seed layer thickness for the high-$\kappa$ gate oxide can be controlled, substantial improvements in subthreshold swing can be achieved.

REFERENCES

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[2] We use the EOLAS proprietary TCAD tool Q*. https://eolasdesigns.com, Jan 2021.