Dark current in monolithic extended-SWIR GeSn PIN photodetectors

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The monolithic integration of extended short-wave infrared (e-SWIR) photodetectors (PDs) on silicon is highly sought-after to implement manufacturable, cost-effective sensing and imaging technologies. With this perspective, GeSn PIN PDs have been the subject of extensive investigations because of their bandgap tunability and silicon compatibility. However, due to growth defects, these PDs suffer a relatively high dark current density as compared to commercial III-V PDs. Herein, we elucidate the mechanisms governing the dark current in 2.6 μm GeSn PDs at a Sn content of 10 at.%. It was found that in the temperature range of 293 K – 363 K and at low bias, the diffusion and Shockley-Read-Hall (SRH) leakage mechanisms dominate the dark current in small diameter (20 μm) devices, while combined SRH and trap assisted tunneling (TAT) leakage mechanisms are prominent in larger diameter (160 μm) devices. However, at high reverse bias, TAT leakage mechanism becomes dominant regardless of the operating temperature and device size. The effective non-radiative carrier lifetime in these devices was found to reach ~300 – 400 ps at low bias. Owing to TAT leakage current, however, this lifetime reduces progressively as the bias increases.

GeSn semiconductors have been attracting a great deal of interest because of the flexibility they offer to engineer the lattice parameter and the bandgap energy and directness. In recent years, silicon-integrated GeSn photodetectors (PDs) were demonstrated showing a room temperature performance close to that of commercial PbSe detectors at wavelengths reaching 3 μm. However, GeSn semiconductors are inherently metastable and typically exhibit a compositional gradient and a large compressive strain resulting from the lattice-mismatched growth on Ge/Si substrates. As a matter of fact, GeSn PDs suffer high dark leakage current, which can be orders of magnitude higher than that of extended-InGaAs PDs. For instance, at a wavelength cutoff of 2.5 μm GeSn PIN diodes display dark current density of ~10 A/cm², whereas in commercial InGaAs PIN PDs this density is typically on the order of 1 mA/cm². This reduces the performance of GeSn PDs by limiting the detectivity and the noise equivalent power, thus hindering their use in optical communication applications where low dark current PDs are required. High performance, cost-effective e-SWIR detectors operating at room temperature at wavelengths above 2 μm are also coveted for time-resolved spectroscopy, surveillance, autonomous vehicles, and imaging through scattering media such as snow, haze, and fog.

The lattice mismatch between Ge and GeSn layers creates misfits and threading dislocations, which are the main reason for the high dark current. However, studies of the dominating leakage mechanisms and the non-radiative carrier lifetime in GeSn PIN photodetectors remain conspicuously missing in literature despite their crucial importance to the development of all-group IV e-SWIR technologies. In this vein, herein dark current analysis is performed for epitaxial PIN GeSn PD devices at 10 at.% Sn content in the i-layer corresponding to a wavelength cutoff of 2.6 μm. For device diameters between 20 μm to 160 μm, it was found that bulk leakage rather than surface leakage is dominating the dark current, especially as the device diameter increases. Temperature-dependent dark current measurements were analyzed to estimate the activation energies as a function of the reverse bias. It was found that, for the small diameter device, diffusion dominates at low reverse bias, whereas trap assisted tunnel (TAT) leakage mechanism dominates at high bias. The latter is also the case for the large diameter device, but at low reverse bias Shockley-Read-Hall (SRH) leakage becomes the prevalent mechanism. Using capacitance-voltage measurements, the effective non-radiative carrier lifetime estimated at low bias was found in the 300 – 400 ps range, which decreases as high bias due TAT leakage dominating the dark current.

FIG. 1. Material growth and characterization. (a) TEM image showing the CVD grown PIN stack on top of GeSn and Ge-VS buffer layers. (b) XRD 2θ−ω scan confirming the high crystalline quality of GeSn PIN stack. (c) APT concentration profiles of different elements across the GeSn stack showing the width of the i-layer to be 300 nm. (d) Calculated 8 × 8 k·p band lineup (at 300 K) for the whole Ge VS/GeSn stack including the PIN layers.
In a low-pressure chemical vapor deposition (CVD) reactor, a 1.5 µm Ge virtual substrate (VS) was grown on a 4-inch Si (100) wafer. Afterward, GeSn multi-layer buffer with step-wise Sn content increase was grown on Ge VS to engineer the lattice constant to allow for the growth of PIN GeSn heterostructure at the desired Sn composition and lattice strain. A cross-sectional transmission electron micrograph (TEM) is displayed in Fig. 1(a) showing the heterostructure indicating a total thickness of 960 nm. Threading dislocations are observed in the Ge VS/GeSn buffer layers and p-GeSn, however, no extended defects are observed in the i-GeSn and n-GeSn, at the TEM imaging scale. This is likely because of the nucleation and propagation of threading dislocations are suppressed and the gliding of misfit dislocation is promted instead at the interface of GeSn buffer layers underneath the PIN heterostructure.

X-ray diffraction spectroscopy (XRD) 2θ − ω scans around the (004) XRD order were performed to further investigate the crystalline quality of as-grown GeSn multi-layer stack, as shown in Fig. 1(b). The Ge-VS peak is detected at 60.06°, while the signal at smaller angles relates to the GeSn stack. The n-GeSn/i-GeSn/p-GeSn peaks are observed at 64.51°, 64.76° and 65.08°, respectively. Since there are four GeSn buffer layers, the layers # 1 – 2 have a peak around 65.31° and the layers # 3 – 4 are observed around 64.94°. The reported peak at 65.8° associated with severe Sn segregation and precipitation is not observed thus confirming the absence of Sn clusters, in agreement with the atom probe tomography data (APT) measurements discussed below. The high intensity narrow n-GeSn/i-GeSn peaks indicates the high crystalline quality of these layers in line with TEM analysis. To determine the Sn content and investigate the p- and n-doping concentrations, three-dimensional atom-by-atom APT mapping was performed, as shown in Fig. 1(c). Although the small difference in atomic mass between As and Ge atoms makes decoupling As from Ge signal in APT challenging, a clear As profile is visible in the top GeSn layer with a background signal across the heterostructure. The Sn incorporation is controlled by a 10°C-step temperature reduction during growth resulting in uniform compositions of 5 at.% (#1), 6 at.% (#2), 8 at.% (#3), and 9 at.% (#4). Owing to the relatively slow B incorporation in GeSn lattice, the Sn content in the p-GeSn layer decreases from 9 to 8 at.% with broader interface. Conversely, the Sn content increases by 1 at.% in n-Ge0.885Sn0.115 (Fig. 1(c)), which stands in sharp contrast to earlier observations, where As doping was reported to reduce the incorporation of Sn.

Since both strain and composition influence the GeSn bandstructure, the eight-band k · p model with the envelope function approximation was optimized using the empirical parameters extracted from Fig. 1(a-c) to calculate the band lineup of the whole stack, as depicted in Fig. 1(d). It is noteworthy that the n-Ge0.885Sn0.115 and i-Ge0.894Sn0.106 layers have direct bandgaps of 0.512 eV and 0.541 eV, respectively. The p-Ge0.924Sn0.076 layer displays an indirect bandgap of 0.575 eV. It is also noted that the tensile strain in the n-layer has reduced the bandgap energy as compared to the i-layer which possesses less Sn content.

PIN PDs were fabricated with various mesa diameters following a top-down processing flow. Fig. 2(a) illustrates the device design. To reduce the contact parasitic capacitance and isolate each device from its neighboring ones, the fabrication process started with chlorine ICP etch down to Ge-VS. Subsequently, Another chlorine etch in the shape of circular bumps was subsequently performed down to the p-layer. The fabricated devices have varying mesa diameters of 20, 24, 32, 40, 80, 120, and 160 µm. To reduce surface defects, the etched sidewall was passivated using chemical treatment in HCl : HF (1:1) for 10 seconds followed by a PECVD deposited thick SiO2 layer. Using BOE wet etch, openings were made in the SiO2 layer for the p- and n-contacts followed by Ti/Au contacts deposition using e-beam vaporization, as schematically shown in Fig. 2(a).

First, the IV curves of GeSn PIN PDs at different diameters in dark were investigated. As displayed in Fig. 2b, a rectification ratio of 10^2 is recorded at 0.5 V for the 20 µm device, which indicates the relatively high quality of the GeSn PIN layers. As the diameter size increases, the reverse dark current increases monotonically, which is expected because of the increased active area of the device. However, when the dark current density is plotted as a function of the applied bias, the reverse dark current densities overlap on each other regardless of the device diameter, which is indicative of the low surface.
current leakage as the active area reduces from 160 µm to just 20 µm, as shown in Fig. 3(c). It is worth mentioning that the low dark current and applied bias would significantly increase the detectivity of these devices compared to photoconductive (PC) devices that suffer from high dark current and high noise. This would allow PIN devices to work without the need for lock-in technique to extract the photocurrent signal, which is relevant for practical applications. Owing to the importance of the dark current in shaping the performance of a PD, in-depth investigations of the underlying processes are of compelling importance. In this vein, systematic studies of the temperature-dependent dark current, activation energy, and leakage mechanisms are performed. One way to separate the contributions of the bulk leakage from the surface leakage is to fit the dark current density \( J_{\text{dark}} \) as a function of the inverse of the device diameter (\( D \)) using:

\[
J_{\text{dark}} = J_{\text{bulk}} + 4 \frac{J_{\text{surf}}}{D},
\]

where \( J_{\text{surf}} \) is the surface leakage current density. Figure 2(d) shows the linear fit for \( J_{\text{dark}} \) at reverse bias of 1 V and the value of the \( J_{\text{bulk}} \) is 6.5 A/cm² which is 3 orders of magnitude higher than the \( J_{\text{surf}} \) of 2 mA/cm² indicating the effective passivation of these PIN PDs. Thus, only the bulk leakage current is considered in the following analysis as it is the dominating component.

In Figs. 3(a) and 3(b), the dark current is plotted for the smallest and largest devices as a function of the applied bias acquired at different temperatures in the 293 - 363 K range with 10 K increments. At low bias (< 0.5 V), it is noticeable that the rise in temperature yields a remarkable increase in the dark current in the small device as compared to the large one. However, at high bias (> 0.5 V) the dark current at various temperatures becomes practically identical regardless of the device size. The following analysis elucidates this behavior.

Based on the temperature-dependent studies, the dominant leakage mechanisms underlying the dark current are identified, and their activation energies are estimated. According to PL measurements (not shown) the effective bandgap for the GeSn device is 0.52 eV (2.4 µm)\(^{12}\). Generally, the dark current generation in PIN device is attributed to three main mechanisms\(^{18,27}\): (1) diffusion leakage current due to the minority carriers at the edges of the depletion region, which corresponds to an activation energy (\( E_a \)) close to the bandgap energy (\( \sim 0.52 \) eV); (2) SRH leakage current caused by the generation of carriers from the deep level defect states with the corresponding activation energy of about half of the bandgap energy \( \sim 0.26 \) eV; and (3) TAT leakage current, which is more pronounced under a significantly high reverse bias, and the associated activation energy is typically smaller than that of SRH (\( \sim 0.26 \) eV). Given the relatively low reverse bias applied to these GeSn PDs and the very high bias typically required for the band-to-band tunneling, the contribution of the latter is neglected under our conditions. Consequently, the dark current can be expressed as:

\[
I_{\text{dark}} = I_{\text{diff}} + I_{\text{SRH}} + I_{\text{TAT}},
\]

where \( I_{\text{diff}} \), \( I_{\text{SRH}} \), and \( I_{\text{TAT}} \) are the diffusion, SRH, and TAT dark current components, respectively. Since the \( I_{\text{TAT}} \) depends on the trap density of the bulk material, it can be expressed as \( I_{\text{TAT}} = \Gamma I_{\text{SRH}} \), where \( \Gamma \) is the simulated electric field enhancement factor, which is proportional to the average electric field inside the junction\(^{28,29}\).

The total leakage dark current can be expressed as\(^{30}\):
The diffusion length is longer than the depletion region in these devices, it is important to estimate the effective carrier current for small device sizes or temperature. This is due to the relative importance of surface defects as compared to the small ones.

The Arrhenius plot of $\ln(I_{\text{dark}}/T^{1.5})$ as function of $1/kT$ for various bias values of 1, 0.8, 0.6, 0.4, and 0.2 V is shown in Figs. 3(c) and 3(d). It can be inferred from this plot that the curves become more linear as the bias increases for the small size device, which indicates a change in the leakage current mechanism, as discussed below.

For $qV >> kT$, the activation energy is the slope of these curves. The obtained values are plotted as a function of the applied bias for the two sets of devices in Figs. 3(e) and 3(f). Two different regimes emerge from this analysis. First, at low bias < 0.5 V, for the small diameter device $E_a$ significantly increases with temperature to reach $\sim 0.5$ eV at 0.2 V. This indicates that the diffusion leakage current is dominating at high T, while the TAT current dominates at low temperature, where $E_a < E_g/2$. However, for the large diameter device $E_a \sim 0.26$ eV (i.e., $E_g/2$) is obtained at high temperature indicating that the SRH generation mechanism is dominating the leakage current. At low temperature, the TAT dominates the dark current. This is most likely because the large active area devices contain a higher absolute amount of dislocations and defects as compared to the small ones. Second, at high bias > 0.5 V, the $E_a << E_g/2$ indicate that TAT is dominating the leakage current regardless of the device size or temperature. This is due to the relatively thin i-layer of these GeSn PDs such as only 1 V is sufficient to fully deplete it and enforce a high tunneling current.

To further clarify the leakage processes in these PIN devices, it is important to estimate the effective carrier lifetime $\tau_{\text{eff}}$. The latter is obtained assuming that the diffusion length is longer than the depletion region and by differentiating the dark current by the depletion width ($W$) as

$$\frac{dJ_{\text{dark}}}{dW} \approx \frac{q n_i \tau_{\text{eff}}}{W},$$

where $n_i$ is the intrinsic carrier concentration in the i-layer. It is relevant to evaluate the dependence of $\tau_{\text{eff}}$ on the bias and device size when TAT is not the dominant mechanism. Based on MOS capacitor measurements, the estimated carrier concentration in the unintentionally doped as-grown GeSn thin films is $n_i = 1.05 \times 10^{17}$ cm$^{-3}$ at room temperature. To determine the $W$, capacitance-voltage measurements (CV) were performed for all devices and the depletion width was determined as $W = \epsilon A/C$, where $A$ is the active device area and $\epsilon$ is the dielectric permittivity of GeSn. The depletion width is assumed to be independent of the device diameter. As shown in Fig. 4(a), the capacitance rapidly drops close to 0 V then slowly decreases as the reverse bias increases. The W extracted from the capacitance curve shows a continuous increase and exceeds 200 nm at 0.7 V beyond which the capacitance values are depressed because of the significant TAT leakage. Knowing $W$, $\tau_{\text{eff}}$ is determined from Eq. (3) as displayed in Fig. 4(b) showing $\tau_{\text{eff}}$ as a function of the applied bias up to 0.7 V for both small and large devices at $T = 293$ K. It can be inferred from the figure that, regardless of the device size, $\tau_{\text{eff}}$ decreases as the bias increases. Note that the activation energies in Figs. 3(e) and 3(f) are $\ll E_g/2$. This indicates that TAT leakage dominates the dark current at room temperature, which explains the small values of $\tau_{\text{eff}}$ across the whole bias range. At a low bias < 0.5 V, owing to the increased bulk defects in the large device and the increased importance of surface defects in the small device, and that $\Gamma$ depends on the electric field, the small device has slightly larger $\tau_{\text{eff}}$. Conversely, at a high bias > 0.5 V the large device exhibits a slightly higher $\tau_{\text{eff}}$. This is because the electric field has greater influence on the small device surface as the bias increases. However, this surface effect remains rather minor.

In summary, the dark current characteristics of vertical PIN GeSn PDs was investigated. The various leakage mechanisms dominating the dark current were elucidated and their behavior as a function of bias, device dimension, and operating temperature were discussed. Additionally, the effective non-radiative carrier lifetime was found to exceed 300 ps at low bias and decreases monotonically as the bias increases due to TAT leakage. Understanding and controlling the dark current is of paramount importance to pave the way to improve GeSn e-SWIR PDs and adopte their use in optical and data communication, LIDAR, and biochemical sensing applications.

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Data availability. The data that support the findings of this study are available from the corresponding author upon reasonable request.

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