Analysis and Calibration of SAR ADC

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Abstract—This paper presents the effect of capacitor mismatch on the weights of binary and split SAR ADC. It proposes matrix formulation to calculate the nodal voltages for N-section split SAR ADC. Second part of the paper proposes a new weight estimation methodology.

Index Terms—successive-approximation register (SAR), analog-to-digital converter (ADC), weight estimation, histogram, calibration, least-mean square estimation.

I. INTRODUCTION

Many emerging applications require low power, high precision, integrated analog to digital capability, example monitoring of bio-signals in medical instrumentation. SAR is well suited and it offers a good compromise in the trade offs among sampling rate, power, dynamic range and die area. Capacitor mismatch and parasitic capacitors associated with the attenuation capacitor is main source of non-linearity of the SAR ADC. If we combine the output bits with the actual weight instead of ideal weight, linearity of the SAR ADC will improve.

This paper takes a two step approach in order to determine the actual weight of the SAR ADC. The first stage is the estimation of the transition point of the ADC followed by weight estimation. A sinusoidal signal is digitized at sampling rate which is asynchronous to the input. The relative number of occurrences of the distinct digital output code is termed as code density. The code density data is used to compute all the transition points of the ADC. The optimum weight is the product of $R^{-1}$ and P where the $R^{-1}$ and P matrices can be calculated from the transition point.

This paper consists of five sections, Section 2 presents the mathematical model of the SAR ADC in terms of DAC Capacitors, Section 3 details the proposed weight estimation methodology, Section 4 explains the modified methodology where an exponential input is used in place of sinusoidal input and Section 5 draws the conclusion.

II. MATHEMATICAL MODEL OF SAR ADC

SAR ADC converts analog signals to digital based on binary search algorithms except the target value is not always compared to the middle value. In general binary SAR ADC, input voltage is compared to a voltage which depends on the previous cycle SAR ADC output. Capacitive SAR ADC consists of binary weighted capacitors whose bottom plate voltage is controlled by SAR Logic (previous bit cycle output stored in the series of D Flip Flop) and generated top plate voltage ( after charge conservation ) is compared to the input voltage. In the SAR operation, output of the SAR Logic is high during sampling, MSB toggles depending on the comparator output during the second cycle, followed by lower bits till LSB.

A. Binary SAR

A $N$ bit binary SAR consist of $N + 1$ capacitors i.e. $C_0$, $C_1 = C_0$, $C_2 = 2C_0$,..., $C_N = 2^{N-1}C_0$ as shown in Fig. 1. In the first cycle, $V_{in}$ is applied at the bottom plate and ground at the top plate of the capacitor which results in total charge stored $Q_i = V_{in} \sum_{i=0}^{N} C_i$. Effective weight of the MSB is calculated by connecting the bottom plate of $C_N$ capacitor to high voltage and the bottom plate of the rest of the capacitor to ground. Charge conservation is applied to calculate $V_x$ in terms of $V_{in}$ where $V_x$ is the top plate voltage.

$$Q_f = C_N(V_{DD} - V_x) + C_{N-1}(0 - V_x) + \ldots + C_0(0 - V_x) \quad (1)$$
$$Q_f = C_NV_{DD} - V_x \sum_{i=0}^{i=N} C_i = Q_i \quad (2)$$
$$V_x = -V_{in} + V_{DD} \frac{C_N}{\sum_{i=0}^{i=N} C_i} \quad (3)$$

The effective weight corresponding to the MSB is $C_N/\sum_{i=0}^{i=N} C_i$ as captured in the above equation. Similarly we can generalise the weight corresponding to the $b_k$ bit as $C_{k}/\sum_{i=0}^{i=N} C_i$ using induction. In an ideal binary weighted SAR ADC, capacitors are binary weighted which results in $2^{-i}$ weights. Due to the capacitor mismatch, the weights of the SAR ADC are non-integer power’s of 2 which results in repeated and missing code.

In an example of 6-bit binary SAR ADC where an actual MSB capacitor is 20% smaller than the ideal MSB capacitor, full scale of the SAR ADC is given by $0 - V_{DD}(1 - C_u/\sum C_i)$ is less compared to Ideal full scale $0 - V_{DD}(1 - 1/2^N)$. N-bit ADC output is converted into ADC decimal output by multiplying with weight. Histogram of the decimal output is plotted by dividing using $2^N$ bin. If ideal weights are used for an non-ideal ADC, decimal output
will start from the 0<sup>th</sup> till the 2<sup>N</sup> − 1<sup>th</sup> bin but some bins will be missing or repeated which result in distortion in the output spectrum. Instead of ideal weights, actual weights are multiplied to the ADC output code, there will be no missing bin but the last few bins will be empty.

Let’s take an example of 6-bit binary SAR ADC with capacitors $C_0, 1.9C_0, 1.9^2C_0, 1.9^3C_0, 1.9^4C_0$ and $1.9^5C_0$. If the SAR ADC Digital Codes are combined with Ideal Weights, 13 missing codes are seen at multiple location in the SAR ADC histogram as shown in figure [4]. But if we combine the SAR ADC Output with Actual Weight, no. of missing codes decreases as shown in figure [5]. Hence the improvement in the SNR of the SAR ADC.

### B. Split SAR

Weights of N-bit Split SAR ADC can be expressed in terms of DAC Capacitor similar to N-bit binary ADC. Weights are large and complex formulae involving DAC capacitor for more than 2-section SAR ADC. Instead of expressing the weights in terms of DAC capacitors, weights can be computed numerically. Paper proposes a method in which each phase of the SAR ADC can be expressed as a matrix equation. Matrices are solved for nodal voltages. Consider a 6-bit 2-section SAR ADC separated by a bridge capacitor $C_{B1}$ with
more significant section consisting of capacitors $C_{1,3}, C_{1,2},$ and $C_{1,1}$ and lesser significant section consisting of capacitors $C_{2,3}, C_{2,2},$ and $C_{2,1}$. The bridge capacitor $C_{B1}$ is associated with left plate parasitic capacitor $C_{LP1}$ and right plate parasitic capacitor $C_{RP1}$. In the sampling phase, node voltage $V_1$ is grounded and $V_{in}$ is applied at the bottom plate of the DAC capacitor. A node voltage vector $V_{K-1,1}$ for K-section ADC is calculated from the charge conservation equation $A_{K-1,K-1}V_{K-1,1} = Q_{K-1,1}$ applied at $K-1$ nodes. For 2-section ADC, matrices $A$ and $Q$ are given by

$$A_{1,1} = C_{LP1} + C_{B1} + \sum_{i=1}^{3} C_{2,i}$$  \hspace{1cm} (4)

$$Q_{1,1} = V_{in} \sum_{i=1}^{3} C_{2,i}$$ \hspace{1cm} (5)

For 3-section SAR ADC,

$$A_{1,1} = \sum_{i=1}^{3} C_{3,i} + C_{B2} + C_{LP2}$$ \hspace{1cm} (6)

$$A_{1,2} = -C_{B2}, A = A^{T}$$ \hspace{1cm} (7)

$$A_{2,2} = C_{B2} + C_{RP2} + \sum_{i=1}^{3} C_{2,i} + C_{LP1} + C_{B1}$$ \hspace{1cm} (8)

$$Q^{T} = [V_{in} \sum_{i=1}^{3} C_{3,i} \ V_{in} \sum_{i=1}^{3} C_{2,i}]$$ \hspace{1cm} (9)

Matrices $A$ and $Q$ can be generalised for N bit Split SAR where each section resolves $P_i$ bits such that $\sum_{i=1}^{K} P_i = N$. On applying charge conservation at each node except the node closest to the comparator in the $\phi_1$ phase, node voltage $V_2, V_3, \ldots$ and $V_K$ can be calculated as a solution to the matrices equation.

$$A_{i,j} = \begin{cases} C_{B_{K+1-i}} + C_{RP_{K+1-i}} + \sum_{i=1}^{i=p_{K+1-i}} C_{K+1-i,i} + C_{LP_{K+1-i}} + C_{B_{K+1}}, & i = j \\ C_{K+1-i,i} + C_{LP_{K-i}} + C_{B_{K-i}}, & i = j \\ -C_{B_{K-i}}, & i = j + 1 \\ -C_{B_{K+1-i}}, & i = j + 1 \\ 0, & \text{otherwise} \end{cases}$$ \hspace{1cm} (10)

$$[A]_{K-1,K-1} = \begin{bmatrix} V_{K} \\ V_{K-1} \\ \vdots \\ V_{2} \\ V_{1} \end{bmatrix} = \begin{bmatrix} V_{in} \sum_{i=1}^{i=p_{K}} C_{K,i} \\ V_{in} \sum_{i=1}^{i=p_{K-1}} C_{K-1,i} \\ \vdots \\ V_{in} \sum_{i=1}^{i=p_{2}} C_{2,i} \end{bmatrix}$$ \hspace{1cm} (11)

Total charge stored on the capacitors in the section closest to the comparator

$$Q_i = -C_{B1} V_2 - V_{in} \sum_{i=1}^{i=p_{1}} C_{1,i}$$ \hspace{1cm} (12)

In the $\phi_2$ phase, the node voltage vector $V^{T} = [V_{K} V_{K-1} \ldots V_{1}]$ is a solution of charge conservation equation $B_{K,K}V_{K,1} = S_{K,1}$. For 2-section SAR ADC,

$$B_{1,1} = \sum_{i=1}^{3} C_{2,i} + C_{LP1} + C_{B1}$$ \hspace{1cm} (13)

$$B_{1,2} = -C_{B1}, B = B^{T}$$ \hspace{1cm} (14)

$$B_{2,2} = C_{RP1} + C_{B1} + \sum_{i=1}^{3} C_{1,i}$$ \hspace{1cm} (15)
For 3-section SAR ADC,

\[
S_T = \left[ \sum_{i=1}^{3} D_{2,i}C_{2,i} + \sum_{i=1}^{3} D_{1,i}C_{1,i} + Q_i \right]
\]

(16)

1) Effect of the Bottom Plate Parasitic Capacitor: If we consider only the effect of the bottom plate parasitic capacitor i.e. rest of the capacitors are assumed ideal, bottom plate capacitor \( C_X \) decreases the weight \( W_1, W_2, \) and \( W_3 \) from ideal and increases \( W_4, W_5, \) and \( W_6 \) from ideal. Maximum deviation in the difference of decimal equivalent of the neighbouring ADC Digital Code will be observed when all the lower bits of the lesser significant section turns off and first bit of the more significant turns on, and if the deviation \( \delta_1 - \delta_2 - \delta_3 + \delta_4 \) (total deviation is positive as the first three deviations is negative) exceeds the 1 LSB, we will observe repeated code in the transfer characteristic. If we make the bridge capacitor \( C_B \approx 1.2C_B \), deviation in the weights \( W_1, W_2, \ldots, W_5 \) and \( W_6 \) decreases. Hence there will be lesser repeated codes in the transfer characteristics.

Let’s consider the case which has the maximum probability of repeated codes (LSB bits \( b_i \), \( 1 \leq i < j \)) turns off and MSB \( b_j \) turns on, change in the decimal output is \( W_j - W_0 - W_1 - \ldots - W_{j-1} \). If \( \delta_i \) is the deviation of the weight \( W_i \) from the ideal, total deviation of the decimal output form the ideal is \( \sum \delta_i \). If the total deviation is greater than 1 LSB i.e. \( C_0/\sum C_i \), we observe repeated code in the transfer characteristic and if the total deviation is smaller than 1 LSB, we observe missing code in the transfer characteristic. In the case of repeated or missing code, the quantization noise exceeds the \( \Delta^2/12 \) which decreases the resolution of the quantizer. In the weight estimation technique, we combine the binary output of the ADCs with actual weights instead of ideal weights in order to restore the SNR of the ADC. Missing code can be corrected by the above technique where as repeated code can not be corrected as there is information loss. In order to prevent repeated code, \( C_j \leq \sum_{i=j-1}^{n=0} C_i \). So if we keep \( C_j \leq \sum_{i=j-1}^{n=0} C_i \), there is no repeated code in the transfer characteristics.

III. Weight Estimation Methodology

ADC Calibration methodology consists of the Transition Point Estimation (TPE) stage which estimates the transition point of the ADC Transfer Characteristic and Weight Estimation (WE) stage uses the estimated transition point to calculate the weight of the ADC.

Due to capacitor mismatch, weight of the SAR ADC deviate from the ideal value \( 1/2^i \) where \( i = 0, 1, \ldots, N-1 \) where N is the ADC resolution, resulting in deterioration of the SNR (Signal to Noise Ratio). SNR of the ADC Output can be restored if we combine the ADC output bit with actual weights \( W_i = C_i/C_T \) instead of ideal weights.

\[
D_{out} = \sum_{i=0}^{N-1} d_i W_i
\]

(27)

In order to maximise the SNR of the ADC, quantization noise has to be minimised. If \( V_{in} \) is input to the ADC, \( x^T = [d_0 d_1 d_2 \ldots d_{N-1}] \) is the output code and \( w^T = [W_0 W_1 W_2 \ldots W_{N-1}] \) is the weight with which output code are combined, the quantization error is given by the following equation

\[
e[n] = V_{in} - w^T x
\]

(28)
We can apply Weiner filter approach to obtain optimum weight. In Weiner filter, the performance function (or the quantization noise) which is mean squared error function given by

$$Q = E[e[n]^2] = E((V_{in} - w^tx)(V_{in} - w^tx)^t)$$  \hspace{1cm} (29)

has single global minimum.

$$= E(V_{in}^2) + w^tE(xx^t)w - 2w^tE{xV_{in}}$$  \hspace{1cm} (30)

$$= E(V_{in}^2) + w^tRw - 2w^tp$$

$$W_{opt} = R^{-1}p$$  \hspace{1cm} (31)

where $$R_{N\times N} = E[xx^t]$$ and $$p_{N\times 1} = E[xV_{in}]$$

A. Modified Iterative Technique

Wiener’s optimum weight $$W_{opt} = R^{-1}p$$ involves $$R^{-1}$$ term which is computation intensive term especially in high resolution ADC. We can convert optimum weight to iterative weight update which does not involve the $$R^{-1}$$ term.

$$W_{i+1} = W_{i} - 2\mu[RW_{i} - p]$$  \hspace{1cm} (32)

where, $$\mu$$ is the learning rate.

B. R and p matrix Calculation

R matrix depends on the probability of the output code. If we use a deterministic signal (as the input signal) during calibration phase, we can determine the probability of the output code. Hence the R matrix. For a ramp input, probability density function of the output code will be uniform. Probability of the output code is calculated from the histogram bin height i.e. $$H(i)/N_t$$ . We need a Transition Point Estimator(TPE) stage to calculate the voltage $$V_a$$ and $$V_b$$ which are required to calculate the p matrix, according to the equation [38]

$$R = E[xx^t] = \sum_{i=0}^{2^N-1} x_i x_i^t p(x_i) = \sum_{i=0}^{2^N-1} x_i x_i^t \frac{H(i)}{N_T}$$  \hspace{1cm} (33)

where H(i) is the histogram bin height and $$N_T$$ is the sum of the bin height.

$$\sum_{i=0}^{2^N-1} x_i x_i^t \int_{V_a}^{V_b} p(V) dV$$  \hspace{1cm} (34)

where p(V) is the probability distribution, $$V_b$$ and $$V_a$$ is the transition point corresponding to $$x_i$$th code.

$$= \sum_{i=0}^{2^N-1} x_i x_i^t \frac{V_b - V_a}{FS}$$  \hspace{1cm} (35)

where FS is the input full scale of the ADC.

$$p = E[xV_{in}] = \sum_{i=0}^{2^N-1} x_i \int_{V_a}^{V_b} p(V) dV$$  \hspace{1cm} (36)

by quantization noise) which is mean squared error function given

$$E(xx^T) = \frac{1}{4} \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} + \frac{1}{4} \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} + \frac{1}{4} \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} + \frac{1}{4} \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} = \frac{1}{16} \begin{pmatrix} 4 & 0 & 0 & 0 \\ 0 & 4 & 0 & 0 \\ 0 & 0 & 4 & 0 \\ 0 & 0 & 0 & 4 \end{pmatrix}$$  \hspace{1cm} (37)

on assuming p(V) has a uniform distribution.

The simplest TPE stage is a ramp input (Full scale from $$V_{SS}$$ to $$V_{DD}$$) followed by histogram generator. The relative width of the step (corresponding to the $$i_{th}$$ code) in the ADC Transfer characteristic is given by $$w_i = (V_{DD} - V_{SS})H(i)/N_t$$ where $$H(i)$$ is the histogram bin height of the $$i_{th}$$ code and $$N_t$$ is the sum of bin heights. Transition point is given by following points $$V_{SS}, V_{SS} + wido, V_{SS} + wid1, ..., V_{DD}$$ where $$wid_0, wid_1$$, and $$wid_{2N-1}$$ are the widths of the 0, 1, ..., $$2^N-1$$ code respectively as shown in the figure [9]

Let’s take an example of 2 bit ideal and input full scale from $$-V_{ref}$$ to $$V_{ref}$$ ADC. Output code (x) can take 4 possible output.

$$x = \{ 0, 0, 1, 1 \}$$  \hspace{1cm} (38)

Since each code $$x_i$$ is equi-probable $$p(x_i) = 1/4$$.

$$E(xx^T) = \begin{pmatrix} E(d_0,d_0) & E(d_0,d_1) \\ E(d_1,d_0) & E(d_1,d_1) \end{pmatrix}$$  \hspace{1cm} (39)

$$d_0^2 = 1$$ as $$d_0 = 1$$ for 2 out of 4 cases, $$d_1^2 = 1$$ as $$d_1 = 1$$ for 2 out of 4 cases and $$d_0,d_1 = 1$$ as $$d_0 = d_1 = 1$$ for 1 out of 4 cases.

C. 6-Bit Non Ideal SAR ADC

Let’s take an example 6-Bit SAR of Capacitor DAC where $$C_1 = 0.8702C_0$$, $$C_2 = 1.6966C_0$$, $$C_3 = 3.1123C_0$$, $$C_4 = 6.6471C_0$$, $$C_5 = 13.2740C_0$$ and $$C_6 = 22.3398C_0$$. Histogram of the Output Decimal of the ADC using ideal weight is given by Fig. 10. We can observe missing code aggregated at the centre of the histogram. We take $$R = E[yy^T]$$ where $$y_{\times 1} = [x_{6\times 1}]^T$$ and $$p_{\times 1} = E[y_{\times 1}V_{in}]$$. We have added extra one bit so that weight Vector contains 6 weights and weight offset. Matrix R and p such that

\[
R = \begin{bmatrix}
0.918 & 0.412 & 0.492 & 0.401 & 0.402 & 0.497 \\
0.412 & 0.939 & 0.505 & 0.407 & 0.409 & 0.511 \\
0.492 & 0.505 & 0.990 & 0.412 & 0.414 & 0.557 \\
0.401 & 0.407 & 0.412 & 0.893 & 0.839 & 0.523 \\
0.402 & 0.409 & 0.414 & 0.351 & 0.894 & 0.524 \\
0.497 & 0.511 & 0.557 & 0.523 & 0.524 & 1.066 \\
0.918 & 0.939 & 0.990 & 0.893 & 0.894 & 1.066 \\
\end{bmatrix}
\]
**Fig. 10:** Histogram of Output Decimal of 6-Bit SAR ADC with Ideal Weight

**Fig. 11:** Histogram of Output Decimal of 6-Bit SAR ADC with Actual Weight

\[ P(V_a, V_b) = \frac{1}{\pi} \left( \sin^{-1} \left( \frac{V_b - V_o}{A} \right) - \sin^{-1} \left( \frac{V_a - V_o}{A} \right) \right) \]  

(44)

On applying the below formulae to the above equation and replacing \( P(V_a, V_b) = \frac{H}{N_T} \)

\[ \cos (\alpha - \beta) = \cos (\alpha) \cos (\beta) + \sin (\alpha) \sin (\beta) \]  

(45)

we get,

\[ V_b = V_a \cos \left( \frac{\pi H(i)}{N_T} \right) + \sin \left( \frac{\pi H(i)}{N_T} \right) \sqrt{A^2 - V_a^2} \]  

(46)

If the input full scale range of the ADC is from -A to A and \( V_a = -A \), we can get

\[ V_b = -A \cos \left( \frac{\pi H(i)}{N_T} \right) \]  

(47)

Recursively, we can write transition voltage \( V_i \) in terms of cumulative histogram CH(i)

\[ V_i = -A \cos \left( \frac{\pi CH(i)}{N_T} \right) \]  

(48)

Hence we can write transition point \( V_i \) using ADC output histogram of the input sinusoidal signal.

**E. Simulation Result**

Figure 12 shows the number of input samples of the linear ramp required for N-bit SAR ADC (with 5% deviation in sampling capacitor) to achieve approximately 6n+2 SNR after correction. No of samples required to estimate the Transition Point with desired accuracy increases with increase in the resolution of the ADC.

15 is the histogram of the output sine signal of 7 bit ADC (largest capacitor of the CDAC is 0.8 of the ideal capacitor).

### IV. CONSIDERING THE INPUT HARMONICS

Generating pure sinusoidal wave is difficult compared to square wave. Exponential rising and falling signal can be used as the replacement to pure sinusoidal signal. Fig. 14 shows

\[ V_{out} = A + (V_1 - A)e^{-\frac{t}{RC}}, \quad 0 \leq t \leq T \]  

(49)
Fig. 13: (a) Histogram with LMS Optimum Weight (b) Spectrum of sine output with Optimum weight (c) Histogram with Ideal Weight (d) Spectrum of sine output with Ideal Weight

![Image](https://via.placeholder.com/150)

Fig. 14: Exponential Signal

\[ V_{out} = V_2 e^{-\frac{(t-T)}{RC}}, T \leq t \leq 2T \]  

(50)

where

\[ V_1 = \frac{Ae^{-T/RC}(1-e^{-T/RC})}{1-e^{-2T/RC}} \]  

(51)

\[ V_2 = \frac{A(1-e^{-T/RC})}{1-e^{-2T/RC}} \]  

(52)

Fig. 15: Effect of RC time constant on the Output Voltage

![Image](https://via.placeholder.com/150)

Fig. 16: Effect of RC time constant on the probability density of the Output

![Image](https://via.placeholder.com/150)

Fig. 17: Effect of time constant on the SNR

![Image](https://via.placeholder.com/150)

The equation

\[ p(y) = \frac{p(x_1)}{dx_1} + \frac{p(x_2)}{dx_2} \]  

(53)

On integrating the above equation, we get

\[ p(V_b, V_a) = \frac{\tau}{2T} \ln \left[ \frac{A|V_a|^{-1} - 1}{A|V_b|^{-1} - 1} \right] \]  

(54)

\[ V_b = \frac{A}{1 + (A|V_a|^{-1} - 1)e^{-2T/\tau}p(V_b, V_a)} \]  

(55)

where \( p(V_b, V_a) = \frac{H_a}{N_t} \)

B. Simulation Result

Fig. 17 shows the effect of time constant on the SNR of the ADC. SNR can recovered through this calibration at only optimum time constant. If the time constant is small, no of sample which will lie between 0 and VDD is very small compared to samples at VDD and VSS. Hence the transition point estimator will not have enough samples to predict the transition point correctly. If the time constant is large, output signal will not be full scale so transition point near to VDD and ground can not be determined.

Fig 18 shows the Histogram of the decimal output of a Non Ideal 6-Bit ADC with ideal weights. Actual Weight is estimated by using \( W_{opt} = R^{-1}p \) where \( R \) and \( p \) matrix are
Fig. 18: Histogram of the Decimal Output of Non-ideal ADC

Fig. 19: Histogram of the Decimal Output of Non-ideal ADC after correction calculated using transition point estimator. Fig 19 shows the histogram of the decimal output with estimated weights.

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