Valley-Spin Hall Effect-Based Nonvolatile Memory With Exchange-Coupling-Enabled Electrical Isolation of Read and Write Paths

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ABSTRACT Valley-spin hall (VSH) effect in monolayer WSe$_2$ has been shown to exhibit highly beneficial features for nonvolatile memory (NVM) design. Key advantages of VSH-based magnetic random access memory (VSH-MRAM) over spin orbit torque (SOT)-MRAM include access transistor-less compact bit-cell and low-power switching of perpendicular magnetic anisotropy (PMA) magnets. Nevertheless, large device resistance in the read path ($R_S$) due to low mobility of WSe$_2$ and Schottky contacts deteriorates sense margin (SM), offsetting the benefits of VSH-MRAM. To address this limitation, we propose another flavor of VSH-MRAM that (while inheriting most of the benefits of VSH-MRAM) achieves lower $R_S$ in the read path by electrically isolating the read and write terminals. This is enabled by coupling VSH with electrically isolated but magnetically coupled PMA magnets via interlayer exchange coupling. Designing the proposed devices using object-oriented micromagnetic framework (OOMMF) simulation, we ensure the robustness of the exchange-coupled PMA system under process variations. To maintain a compact memory footprint, we share the read access transistor across multiple bit-cells. Compared with the existing VSH-MRAMs, our design achieves 39%–42% and 36%–46% reduction in read time and energy, respectively, along with $1.1 \times$–$1.3 \times$ larger SM at a comparable area. This comes at the cost of $1.7 \times$ and $2.0 \times$ increase in write time and energy, respectively. Thus, the proposed design is suitable for applications in which reads are more dominant than writes.

INDEX TERMS Exchange coupling, monolayer transition metal dichalcogenide (TMD), nonvolatile memories (NVMs), perpendicular magnetic anisotropy (PMA), valley-spin hall (VSH) effect.

I. INTRODUCTION

WITH the recent explosive growth in highly data-centric applications such as the Internet of Things and artificial intelligence, high storage capacity along with low-power computing in memories has become more crucial than ever. Although conventional CMOS-based memories have brought great prosperity to the semiconductor industry to date enabling high-performance computing, increasing leakage energy and low cell density hinder them from sustaining their benefits in the deep submicrometer regime [1]. To tackle such issues, emerging nonvolatile memories (NVMs) such as phase change memory (PCM), resistive random access memory (RRAM), ferroelectric (FE) memories, and spin-based magnetic RAMs (MRAMs) are being extensively explored [1].

Among the emerging NVMs, spin transfer torque (STT)-MRAM has demonstrated the highest endurance with comparable performance ($>10^{12}$ cycles of endurance and <10 ns write time), is CMOS compatible [1], [2], and, hence, is considered to be one of the most promising NVMs [3]. In addition to the fast operation, high endurance, and nonvolatility, it also exhibits distinct advantages over CMOS memories such as low standby power and high density. However, its high write current density flowing through a magnetic tunnel junction (MTJ) causes critical design conflicts leading to high write power and time-dependent breakdown of the tunneling oxide in the MTJ. Moreover, low distinguishability between two binary states (measured by tunneling magneto-resistance, or TMR) aggravates the design challenges, putting questions on the wider adaptability of STT-MRAM in advanced applications [2], [3].

To address some of the issues of STT-MRAM, spin orbit torque (SOT)-MRAM has been proposed following the discovery of the giant spin hall (GSH) effect in heavy metals (e.g., Pt, Ta, and W) [4], [5], [6]. SOT-MRAM (also named “GSH-MRAM”) has separate write and read paths (see Fig. 1(a)). Write path through a metal leads to a substantial reduction in the write power. Besides, the separation between
write and read paths in SOT-MRAM mitigates the reliability issues [7]. However, these benefits come at the cost of higher area due to the need for multiple access transistors per bit-cell (see Fig. 1(b) and (c)) [7], [8]. A technique based on sharing the read access transistor alleviates some area overhead [9], but has some write issues as the read and write paths are not completely electrically isolated. Another limitation of GSH-MRAM is that its field-free operation relies on in-plane magnetic anisotropy (IMA) which is inferior to perpendicular magnetic anisotropy (PMA) in the context of write efficiency. Coupling the GSH effect with PMA typically requires an external magnetic field leading to design overheads [10]. Some schemes have been introduced to avert an external magnetic field such as interplay of STT and SOT [11], [12], structural asymmetry [13], and interlayer exchange coupling [14]. However, such designs have their own overheads. For example, the design in [14] still relies on IMA-based design, and the read path is not completely isolated from the write path.

Valley-spin hall (VSH) effect in 2-D transition metal dichalcogenides (TMDs) can potentially be a key for implementing an energy-efficient PMA-based spintronic memory [15]. VSH effect enables field-free PMA switching even with higher spin injection efficiency with valley hall angle ($\theta_{\text{SH}}$) as large as 1 at room temperature [16], significantly reducing the write power. Additionally, as we previously proposed in [15], the VSH-MRAM (see Fig. 1(d)) utilizes an integrated back-gate to control the charge and spin currents in 2-D TMD channel. This leads to an access transistor-less compact bit-cell (see Fig. 1(e) and (f)). However, large channel resistance due to low mobility of monolayer WSe$_2$ and source/drain Schottky contacts results in large series resistance ($R_S$) in the read path, deteriorating the memory sense margin (SM).

Motivated by this, we propose VSH-based spintronic memories that not only inherit the appealing features of existing VSH-MRAM but also attain lower $R_S$ by electrically isolating the read and write paths (EIRW). We name the proposed memories EIRW-VSH MRAMs. Low $R_S$ is achieved by designing electrically isolated but magnetically coupled PMA magnets via interlayer exchange coupling [17]. Previously, we had explored a similar structure in the context of nonvolatile flip-flop design [18]; here, we utilize EIRW-VSH for memory design by appropriately optimizing the device for NVM applications and carrying out device-array co-design to achieve optimal energy-performance-area trade-offs. The key contributions of this article are as follows.

1) We propose single-ended and differential nonvolatile spintronic memories utilizing the VSH effect in monolayer WSe$_2$, which feature: 1) out-of-plane spin generation that can be coupled with PMA magnets; 2) integrated back-gate for spin current control during write; 3) EIRW via exchange coupling between PMA magnets; and 4) shared read access transistor for compact array design.

2) We investigate the impact of process variations on the exchange coupling between PMA magnets and the functionality of the proposed memories.

3) We explore the implications of shared read access transistor for both single-ended and differential EIRW-VSH MRAMs, advancing the study in [9] (which focused on single-ended memories).

4) We analyze the benefits and trade-offs of the EIRW at device and array levels, and conduct a detailed comparison with previously proposed VSH-MRAM.

5) We benchmark memory characteristics with SRAM and emerging spin-based NVMs.

II. VSH DEVICES WITH EXCHANGE-COUPLED-ENABLED EIRW

A. STRUCTURE AND OPERATION

As proposed in our earlier work [18], the EIRW in VSH devices is achieved by utilizing the exchange coupling between PMA free layers (FLs). In contrast to [18] where the device was designed with a small energy barrier ($E_B$) of FLs (suitable for nonvolatile flip-flops), here, the exchange-coupled PMA FLs are optimized to have $E_B$ of $\sim 50 kT$ to ensure a large memory lifetime (> 10 years). Moreover, since a low device footprint is of paramount importance in memory design, we optimize the FLs to have smaller dimension compared with [18] while maintaining $\sim 50 kT$ energy barrier. For this, we use a different set of parameters to obtain saturation magnetization ($M_S$) [19] and uniaxial anisotropy density ($K_U$) [20] which are suitable for memory design with larger $E_B$ (see Table 1). Employing these parameters, we propose and optimize two flavors of memory devices: single-ended EIRW-VSH and differential DEIRW-VSH (see Fig. 2(a) and (b), respectively).

The proposed EIRW-VSH devices are designed to exploit the VSH effect in monolayer WSe$_2$. They include a spin...
TABLE 1. Parameters for micromagnetic (OOMMF) and HSPICE simulation.

| Parameter                              | VSH-MRAM | EIRW-VSH MRAM |
|---------------------------------------|----------|---------------|
| Thickness of Single FL [nm]           | 1.3      | 1.3           |
| Volume of Single FL [nm³]             | $(1/4)\times30\times30\times1.3$ | $(1/4)\times21\times21\times1.3$ |
| Thickness of MgO [nm]                 | 1.2      | 1.1           |
| Saturation Magnetization, $M_s$        | 1257.3 [19] | 1257.3 [19]  |
| Uniaxial Anisotropy Density, $K_u$ [erg/cm²] | 2.3×10⁴ [20] | 2.3×10⁴ [20] |
| Damping Coefficient, $\alpha$         | 0.008 [27] | 0.008 [27]   |
| Gyromagnetic Ratio, $\gamma$          | 17.6     | 17.6          |
| Energy Barrier, $E_b$ [kT]             | -50      | -50           |
| Exchange Stiffness, $\delta$ [pJ/m]   | 13       | 13            |
| Exchange Coupling Strength, $J_{xx}$ [mJ/m²] | -        | 0.35 [17]    |
| Resistivity of Ta [KΩ-mm]              | -        | 2 [21]        |

generator, which has a p-type monolayer WSe₂ channel and one or two arms. The devices are designed with a single arm for single-ended read functionality (EIRW-VSH; Fig. 2(a)) or with two arms for a differential read (DEIRW-VSH; Fig. 2(b)). The WSe₂ channel and arms have an integrated back-gate that controls the flow of charge current ($I_C$) in the channel and in turn, spin current ($I_S$) in the arms (which is generated due to the VSH effect). The $I_S$ interacts with FLs, FL₁Ws, which are in direct contact with WSe₂. FL on each arm is a 1.3-nm CoFeB layer with a perpendicular magnetic easy axis in the z-direction. A structure of Ta (0.7 nm)/FeCo-oxide (1.1 nm)/Ta (0.7 nm)/CoFeB (1.3 nm) is formed on top of FL₁W to ferromagnetically couple FL₁W with the top CoFeB FL (FL₉) via interlayer exchange coupling with [17]. An MTJ is formed on top, having FL₉ as its FL. A Read path is formed between nodes R₁ and R₂ (through MTJ) by extending the upper Ta layer in the stack. Note, the read path is completely electrically isolated from the WSe₂ channel (or Write path). Therefore, the proposed devices achieve an EIRW utilizing the exchange coupling between PMA FLs (i.e., FL₁W and FL₉). In terms of conducting properties, thin film Ta has lower resistivity (2 kΩ-nm [21]) than monolayer WSe₂, thus leading to low $R_S$ in our designs compared with VSH-MRAMs [15].

A Write path is formed between source (S) and drain (D) contacts. When $I_C$ (or $I_{WRITE}$) flows between S and D in the y-direction (see Fig. 2), spin currents with opposite out-of-plane spin polarization ($I_{S\uparrow}/I_{S\downarrow}$) are induced to flow along x-axis. Induced $I_{S\uparrow}$ ($I_{S\downarrow}$) switches FL₁W upward (downward) by exerting spin torque. Note that the EIRW-VSH device holds either $I_{S\uparrow}$ or $I_{S\downarrow}$ along the arm. In contrast, the DEIRW-VSH device has both $I_{S\uparrow}$ and $I_{S\downarrow}$ in the two arms, leading to complementary storage of the bit information in the two FL₁W-S (see Fig. 2(c) and (d), respectively). Then, FL₉ is switched by interlayer exchange field generated from the corresponding FL₁W. Thus, $I_C$ in WSe₂ leads to $I_{S\uparrow}/I_{S\downarrow}$, which, in turn, set the MTJ state to be in P- or AP-state via the combination of spin torque and interlayer exchange coupling. The state of the MTJ depends on the direction of the current ($I_C$ or $I_{WRITE}$): in case of DEIRW-VSH device, when $I_C$ flows in $+y$-direction, $I_{S\uparrow}$ ($I_{S\downarrow}$) is generated in $+x$ ($-x$)-direction, and FL₁W (FL₉₁) switches upward (downward). This switches FL₁R₂ upward and FL₁R₁ downward via exchange coupling, encoding P and AP states in MTJs on the right and left arms, respectively (the magnetization of pinned layer in MTJ is in $+\hat{z}$). In the EIRW-VSH device, $I_C$ flowing in the $+y$-direction induces $I_{S\uparrow}$ in the $+x$-direction, setting the MTJ to be in P-state. The opposite happens if the $I_C$ direction is reversed.

Before we end this section, let us briefly discuss the present status of the experimental efforts in exploring the VSH effect. Hung et al. [16], [22] experimentally demonstrated the spinlocked VSH effect in 2-D TMDs using nonlocal measurement and detected out-of-plane spins in 2-D WSe₂ using permalloy (Py) ferromagnetic contact [22]. Moreover, they showed that out-of-plane spin polarity in monolayer WSe₂ depends on the current direction, which supports the idea of Write in the proposed devices. However, a direct interaction between 2-D TMDs and PMA magnets or VSH-driven SOT (employed in this and previous works [15], [18] based on the expectation from the physics of PMA magnetization switching) needs further experimental exploration.

**B. SIMULATION FRAMEWORK**

A simulation framework (see Fig. 3) is established to evaluate the proposed EIRW-VSH devices and arrays and to compare them with VSH-MRAM-based designs [15]. First, we build a 2-D FET model that self-consistently captures 2-D electrostatics and charge transport in p-type WSe₂ channel. The drain current (or charge current, $I_C$) is calculated using the extracted mobility of monolayer WSe₂ [18] and contact resistance ($R_C$) at S/D side [23]. Calibration with the experiment of the drain current is in the inset of 2-D FET model (details on the experiment of WSe₂ FET in [18]). Since both VSH-MRAMs and EIRW-VSH devices exploit the VSH effect in WSe₂, the 2-D FET model is used for all designs.

For the proposed EIRW-VSH devices, $I_C$ (as a function of $V_G$ and $V_D$ of the device), is delivered to object-oriented micromagnetic framework (OOMMF) [24] simulation to investigate the implication of current-induced SOT on the coupled PMA FLs (recall the “Write” operation). To capture the VSH effect-driven spin torque, we use an existing “Xf_STT” class in OOMMF and modify the equations of STT [25] for our memory device structure (dimensions in Fig. 2 and Table 1). We also use a “TwoSurfaceExchange”
class to integrate the Ruderman–Kittel–Kasuya–Yosida (RKKY)-style exchange coupling (coupling strength, $J_{EX}$) between PMA FLs (FL$_W$ and FL$_R$). We use $J_{EX} = 0.35$ ml/m$^2$ as reported in the experiments in [17]. The uniaxial anisotropy ($K_U$) and exchange stiffness ($A$) which are related to the intra-exchange energy of PMA FLs, are considered. For OOMMF simulation, we choose cell sizes (or mesh sizes) as 1, 1, and 1.3 nm (x, y, and z), and the magnetic parameters used in the simulation are listed in Table 1. The switching time of the coupled PMA system (as the result of VSH) obtained from OOMMF simulation is provided to HSPICE simulation for array-level analysis. The MTJ resistance which is involved in the read operation (details in Section III-B) is obtained from Non-Equilibrium Green Function (NEGF) equations, as detailed in [26], and used to develop a Verilog-A model for HSPICE simulations. For baseline VSH-MRAMs, we follow the simulation process outlined in [15].

C. DEVICE CHARACTERISTICS

As mentioned earlier, the proposed (D)EIRW-VSH devices are re-designed from our previous work [18] for evaluation and comparison with (D)VSH-MRAMs [15]. We perform isothermal stability ($\Delta = E_g/k_BT$) analysis between the designs. In the baseline (D)VSH-MRAMs, the single FL is designed to have $\Delta \sim 50$. In contrast, each FL in (D)EIRW-VSH devices is designed to have smaller $\Delta$ but $\Delta \sim 50$ as a whole system (i.e., exchange-coupled FL$_W$ and FL$_R$). This is achieved by maintaining the same thickness but different diameters of a single FL in two designs (see Table 1 for details). This results in a smaller area footprint in our proposed designs compared with (D)VSH-MRAMs, which will be discussed in Section III. The thickness of MTJ oxide (i.e., MgO) is optimized separately for each device to maximize the SM which will be discussed shortly. Specifically, due to the lower $R_3$ in (D)EIRW-VSH devices, the optimal MgO thickness is lower than (D)VSH devices (see Table 1). For both designs, we ensure the SM to be greater than zero even with a 10% variation in MgO thickness which secures robust read.

1) READ

For read, the exchange-coupling-enabled EIRW in (D)EIRW-VSH devices is favorable because of the following two aspects.

1) The high $R_1$ along the WSe$_2$ channel found in the (D)VSH-MRAMs is averted in (D)EIRW-VSH devices, resulting in higher SM (see Fig. 4(a)). For single-ended designs (i.e., VSH-MRAM and EIRW-VSH device), SM is calculated as $(I_p - I_{AP})/2$ where $I_p$ and $I_{AP}$ denote $I_{READ}$ flowing through P- and AP-state MTJs, respectively. For differential designs (i.e., DVSH-MRAM and DEIRW-VSH device), SM is calculated as $I_p - I_{AP}$. Due to the low $R_1$ in the read path and thus larger $I_{READ}$, (D)EIRW-VSH devices exhibit $1.9\times$ improved SM compared with (D)VSH-MRAMs in the entire range of $V_{READ}$ considered in Fig. 4(a).

2) Second, the exchange coupling between FL$_W$ and FL$_R$ in (D)EIRW-VSH devices can be beneficial for lowering the read disturbance. The disturbance is attributed to the fact that $I_{READ}$ flowing through an MTJ can exert STT and disturb the MTJ state (see Figs. 1(d) and 2). Given the read current direction, the AP-state of MTJ is vulnerable to this disturbance and can switch from AP to P state (for both the baseline and proposed designs). However, the critical current ($I_{CR}$) above which such undesired switching occurs is higher in (D)EIRW-VSH devices ($I_{CR} = 20.3 \mu A$) compared with (D)VSH-MRAMs ($I_{CR} = 15.5 \mu A$). This is because FL$_W$ generates an effective field (due to exchange coupling) that opposes the switching of FL$_R$ and helps in lowering the disturbance due to $I_{READ}$. However, as the $I_{READ}$ is also higher due to the low $R_1$ in (D)EIRW-VSH devices, read disturb margin (RDM), which is defined as $(I_{CR} - I_{AP})/I_{CR} \times 100$, is slightly lower for the proposed devices at the same $V_{READ}$ (see Fig. 4(b)). This reduction in RDM is much smaller compared with the SM improvements discussed earlier. Therefore, at $\sim$iso-RDM of $\sim$80% (see Fig. 4(c)), it is observed that SM in (D)EIRW-VSH devices is $1.9\times$ larger.

D. IMPACT OF PROCESS VARIATIONS ON EXCHANGE COUPLING

We also examine the implication of potential process variations on write performance (i.e., switching time of the exchange-coupled PMA magnets). Albeit such a study was performed in our earlier work in the context of nonvolatile flip-flops [18], the FLs re-designed for memories with a

FIGURE 4. Device-level analysis of (D)EIRW-VSH devices compared with (D)VSH-MRAMs: (a) SM and (b) RDM versus read voltage ($V_{READ}$), (c) $1.9\times$ enhancement in SM is achieved at $\sim$iso-RDM of $\sim$80%, and (d) write latency versus write current.
higher $E_B$ in this article require a separate analysis to understand their resilience to possible process variations. As shown in Fig. 5(a) (inset), we consider horizontal misalignment between FL$_W$ and FL$_R$, and reduction in exchange coupling strength ($J_{EX}$) as the process variation factors. The misalignment is swept from 0% to 50% as to the diameter of FL ($D_{MTJ}$), and the exchange coupling strength is reduced to 40%–100% of its original value ($J_{EX \_EXPT}$) reported in the experiment [17]. Here, 0% of misalignment and 100% of $J_{EX \_EXPT}$ (i.e., $J_{EX} = J_{EX \_EXPT}$) is the nominal scenario. Even with misalignment as large as 20% and reduction in $J_{EX \_EXPT}$ by 40% (i.e., $J_{EX} = 0.6 \times J_{EX \_EXPT}$; Fig. 5(b)), we observe a successful switching, with the switching time of the exchange-coupled PMA system remaining similar to the nominal case (see Fig. 5(a)). Moreover, a reduction in $J_{EX \_EXPT}$ by 50% (i.e., $J_{EX} = 0.5 \times J_{EX \_EXPT}$) leads to only a 1.5% increase in switching time for 20% misalignment. For larger misalignment values, which are unlikely to occur, we observe that switching of FL$_R$ via exchange coupling is still attainable as long as $J_{EX}$ remains greater than 40% of the experimental value. However, we notice switching failures in FL$_R$ (when FL$_W$ is reversed by the VSH effect) for reduction in $J_{EX \_EXPT}$ by 70% (i.e., $J_{EX} = 0.3 \times J_{EX \_EXPT}$). Therefore, we conclude that exchange-coupled PMA FLs are resilient to the potential process variations without significantly degenerating their performance keeping large margins in both the misalignment and $J_{EX}$ variation.

### III. (D)EIRW-VSH DEVICE-BASED MEMORY ARRAYS

#### A. DESIGN OF MEMORY ARRAYS BASED ON (D)EIRW-VSH DEVICES WITH SHARED READ ACCESS TRANSISTOR

Utilizing the proposed (D)EIRW-VSH devices, we design single-ended and differential memory arrays (see Fig. 6) with 256 rows and 256 columns. As the read path in the proposed (D)EIRW-VSH devices is formed along the MTJ and Ta layer, a read access transistor is required to control the access to the designated bit-cells during read and to avoid the sneak current through the unaccessed cells. However, having the read access transistor per bit-cell can lead to a large area penalty in our proposed designs compared with the (D)VSH-MRAMs. Therefore, for array design, we adopt a scheme proposed previously by us in [9] for GSH-MRAMs where bit-cells belonging to the same word share the read access transistor as shown in Fig. 6. Note, in [9], the read and write paths are not completely isolated, which can cause write issues/overheads in GSH-MRAMs. However, due to the complete EIRW in our proposed devices such issues are eliminated, and the read path can be optimized solely considering the read requirements. Moreover, the analysis in [9] only considers single-ended design. In this work, we also investigate the sharing of the read access transistor for a differential design. Specifically, for DEIRW-VSH MRAM, the read access transistor is connected to both the true and complementary MTJs of the bit-cells belonging to a word. During read, we access 64 bit-cells (considering a 64-bit word) by asserting the shared read access transistor. Therefore, the read access transistor is shared with 64 MTJs for EIRW-MRAMs and 128 MTJs for DEIRW-MRAMs. The access transistor is an n-type FinFET with its gate connected to read-word-line (RWL). Node $R_1$ of each bit-cell (see Fig. 2) is connected to the drain of the shared read access transistor. Sense-lines, SL (and SLB) are connected to node $R_2$ along the extended Ta layer in the MTJ stack of (D)EIRW-VSH devices and are shared along the column. With this arrangement, read current ($I_{READ}$) through each bit-cell can be read individually on SL (and SLB). However, sharing the read access transistor in a word alters the read operation as...
the MTJs of 64 bit-cells are connected in parallel, and the total resistance affects the current flowing through the shared read access transistor (details will be discussed shortly). The increase in area due to the shared read access transistor is also discussed later in this section.

Similar to [15], an access transistor in the write path is not required in our array designs (see Fig. 6). This is because the back-gate of each bit-cell (i.e., (D)EIRW-VSH MRAMs) has the control of on and off states of the (D)EIRW-VSH devices (see details in Section II-A and [15]) and thus, can be directly connected to write-word-line (WWL). The source and drain of each cell are connected to bit-line (BL) and BL-bar (BLB), respectively, which are shared along the cells in the same column. The details of operation are discussed in Section III-B with bias conditions presented in Table 2.

**B. (D)EIRW-VSH MRAM MEMORY ARRAY OPERATION**

1) **WRITE**

To write, we access the selected bit-cell by applying 0 V to the corresponding WWL (recall that the proposed memory device is p-type). Then, complementary biasing (i.e., \( V_{DD}/0 \)) is applied to BL and BLB to flow \( I_{WRITE} \) in the bit-cell. Note, depending on the BL/BLB biasing, \( I_{S1}/I_{S2} \) will flow and encode Boolean logic into the MTJs in each bit-cell, as discussed earlier. For the single-ended array (see Fig. 6(a)), if BL and BLB are driven to \( V_{DD} \) and 0, respectively, \( I_{WRITE} \) flows from source to drain, generating \( I_{S1} \) to the right arm (due to the VSH effect) and switching FL-W upward (for more details, see Fig. 2). As FL-W and FL-R are magnetically coupled, FL-R also switches upward, encoding “P” in the MTJ (i.e., logic “1” in the bit-cell). Encoding “AP” (or logic “0”) also can be done by applying 0 and \( V_{DD} \) to BL and BLB, respectively. For differential array (see Fig. 6(b)), the write mechanism is similar except the differential encoding in one device is possible. This is because the generated \( I_{S1} \) and \( I_{S2} \) flow in the opposite direction (Fig. 2 for more details), and store “P” and “AP” in MTJs located in two arms of the DEIRW-VSH MRAM. It is noted that, to avoid the sneak current paths, WWL, BL, and BLB are driven to \( V_{DD} \) for unaccessed cells (hold condition) [15].

2) **READ**

To read the stored bits of an accessed cell, we enable the read path by applying \( V_{DD} \) on RWL and \( V_{READ} \) on SLs (and SLBs in case of DEIRW-VSH MRAM). We simultaneously read 64 bit-cells of the accessed word. Sharing the read access transistor among the bit-cells belonging to the same word has important read implications, especially in a single-ended array. Each MTJ in a bit-cell exhibits two levels of resistance, high- and low-resistance state (\( R_{AP} \) and \( R_{P} \), respectively), with \( R_{P} < R_{AP} \). Therefore, when the 64 MTJs are connected to the read access transistor in parallel, the bit pattern stored, e.g., the number of cells storing logic “1/0” (P/AP-state), affects the equivalent resistance and controls the amount of currents flowing through the shared read access transistor and also, through the SL. To explain this, let us first consider a case where “N” and “64-N” cells are storing logic “1” and “0,” i.e., “N” and “64-N” MTJs are in P- and AP-state, respectively (see Fig. 7(a)). The voltage at node x \( (V_x) \) is dictated by N. Now, if the number of cells storing logic “1” \( (N) \) increases, the equivalent resistance of all the MTJs decreases and thus, \( V_x \) increases. This results in the decrease of voltage drop across the MTJs, reducing both \( I_P \) and \( I_{AP} \). Thus, \( I_{READ} \) in the single-ended array is the function of the number of cells storing logic “1,” as shown in Fig. 7(c).

Although we simultaneously read a word, each bit-cell can be sensed independently by reading \( I_{READ} \) through each SL, which runs along the column and is connected to the current sense amplifier (CSA) in the reference circuit (see Fig. 7(b)). Two reference MTJs (in P- and AP-state each) are employed in the reference circuit and also share the same read access transistor with the 64 bit-cells. By doing so, the reference current \( I_{REF} = (I_P + I_{AP})/2 \) for single-ended array flowing through the reference MTJs can track the number of cells storing logic “1” in the word (see Fig. 7(c)). The \( I_{READ} \) (either \( I_P \) or \( I_{AP} \)) from each bit-cell is compared with \( I_{REF} \) and the output of the CSA yields the stored bit-information. Fig. 7(c) shows \( I_{READ} \) versus the number of cells storing logic “1” in single-ended array based on EIRW-VSH MRAM. As explained earlier, both \( I_P \) and \( I_{AP} \) decrease as the number of cells storing logic “1” increases. Here, the SM of cells storing logic “1” and “0” are calculated as \( I_{P - I_{REF}} \) and \( I_{REF - I_{AP}} \), respectively.

For the differential array designed with DEIRW-VSH MRAM, the number of cells storing “1” in a word is fixed to 64 regardless of the bit stored in each cell. This is because each differential cell holds both P- and AP-MTJs. Therefore, \( I_{READ} \) is constant irrespective of bit pattern stored in the accessed word (see Fig. 7(d)). It is noted that in the case of the proposed differential array, the reference MTJs are not necessary as SL and SLB in a cell can be compared to determine the output (i.e., bit information of the cell). Here, SM is calculated as \( I_{P - I_{AP}} \).

Note, it is important to consider the pitch-matching of the proposed bit-cells with the CSA. Since the EIRW bit-cells have the layout width of \( >2 \) metal pitch (single-ended) or \( >4 \) metal pitch (differential), the CSA needs to be laid out so as to either: 1) match its layout width with that of the bit-cell or 2) share the CSA among the bits of different words in a row by using a column multiplexer before the CSA.

![FIGURE 7](image-url)
sizes. Also, the results are compared with those of baseline trade-off and 2) time and energy analysis with various array comprehensive array-level analysis, including 1) SM and area reduction in EIRW is favorable to read performance in array designs, \( \sim 2.1 \times \) path of (D)EIRW-VSH MRAMs leads to 1.9 \% for single-ended and differential, respectively) is not severe even at \( N \) of 50. It is important to note that there exists a trade-off between SM and area (see Figs. 8(e) and 9(a)). Depending on the system requirements and target specification, \( N_{\text{FIN,SHARED}} \) can be tuned for the required sensing robustness with a comparable or slight increase in area.

Second, the exchange coupling between FLs helps in reducing read disturbance (see Section II-C for more details). Given that (D)EIRW-VSH MRAM exhibits higher \( I_{\text{CR}} \) than (D)VSH-MRAM due to the exchange coupling, (D)EIRW-VSH MRAM array shows 1.2\( \times \)–1.3\( \times \) higher RDM than (D)VSH-MRAM (see Fig. 9(b)). Although increasing the size of the shared read access transistor leads to the reduction in RDM due to larger \( I_{\text{READ}} \), RDM of (D)EIRW-VSH MRAM remains 1.1\( \times \) higher than (D)VSH-MRAM even at \( N_{\text{FIN,SHARED}} = 50 \).

2) Write/Read Time and Energy
Fig. 10(a)–(d) show write/read time and energy comparison of the proposed (D)EIRW-VSH MRAM arrays with the baseline (D)VSH-MRAM arrays. Read time and energy (RT and RE) are lowered in the proposed (D)EIRW-VSH MRAM arrays due to small \( R_S \) in the read path and compact array design by virtue of the shared read access transistor. (D)EIRW-VSH MRAM arrays exhibit 39\%–42\% reduction in RT, and 36\%–46\% reduction in RE compared with the (D)VSH-MRAM-based arrays. However, exchange coupling in the proposed designs leads to 67\% and 66\% increase in write time (WT) for single-ended and differential arrays (array size = 256 \times 256 and \( N_{\text{FIN,SHARED}} = 20 \)). As the write energy (WE) is proportional to WT, the increased WT leads to a 95\% and 96\% increase in WE for single-ended and differential arrays, respectively.

We further investigate the effect of array size on write and read performance (see Fig. 10(e)–(l)). Write/read time and energy are calculated with the various array sizes from 256 \times 256 to 1024 \times 1024, and normalized to (D)VSH-MRAM arrays with an array size of 256 \times 256. For write, increasing the array size reduces the WT and WE penalties in the proposed designs (i.e., reduction in the ratio of WT(E)\( \text{(D)EIRW}/\text{WT(E)}\)\( \text{(D)VSH} \)) as the contribution of FL switching time diminishes with the increase in

C. LAYOUT
We also perform the layout analysis based on scalable \( \lambda \)-based rules [28], where \( \lambda \) is half the minimum feature size (\( F \)) associated with technology. We consider gate and metal pitches corresponding to 7 nm technology [29]. Fig. 8 shows the layout comparison for a word. As shown in Fig. 8(b) and (d), the proposed arrays include the area of the shared read access transistor, leading to an increase in total width compared with (D)VSH-MRAM arrays. However, due to the smaller MTJ dimension (recall from Section II-A and Table 1), bit-cell height is smaller in the proposed arrays, compensating for the increase in width. Therefore, the increase in the area (see Fig. 8(e)) in single-ended EIRW-VSH MRAM array is less than 1\% compared with the VSH-MRAM array for \( N_{\text{FIN,SHARED}} \) of 20. For differential arrays, DEIRW-VSH MRAM array exhibits 1\% reduction in the area compared with the DVSH-MRAM array at the same \( N_{\text{FIN,SHARED}} \). Although the area overhead grows as the size of the read access transistor increases, the area increase (12\% and 7\% for single-ended and differential, respectively) is not severe even at \( N_{\text{FIN,SHARED}} = 50 \).

D. ARRAY-LEVEL ANALYSIS
In Section II-C, device analysis shows that low \( R_S \) in the read path of (D)EIRW-VSH MRAMs leads to 1.9\( \times \) improvement in SM at RDM of \( \sim 80\% \). Hence, exchange-coupling-enabled EIRW is favorable to read performance in array designs, including enhancement of SM and RDM, and reduction in read time and energy. However, this comes at the cost of higher write time and energy. In the following, we describe a comprehensive array-level analysis, including 1) SM and area trade-off and 2) time and energy analysis with various array sizes. Also, the results are compared with those of baseline (D)VSH-MRAM arrays.
metal-line-charging time/energy. For read, the read time and energy improvements are further enhanced as the array size is increased. Our results show RT and RE reduction of up to 47%–50% and 46%–50%, respectively, compared with (D)VSH-MRAM for a 1024×1024 array. This is because the effect of low R_S in the proposed designs is manifested to a larger extent in larger arrays as the SL RC delay becomes more dominant for larger array sizes (due to an increase in the SL capacitance).

3) BENCHMARKING WITH OTHER MEMORIES

In Fig. 11, we benchmark the memory metrics with SRAM, and emerging spin-based NVMs such as STT-MRAM [2], (D)GSH-MRAMs [7], [8], and (D)VSH-MRAMs [15]. Values of RT, RE, WT, WE, and area are obtained in a 1024×1024 array and normalized with respect to SRAM. SM is normalized to that of STT-MRAM as the SRAM employs voltage-based sensing while emerging spin-based NVMs use current-based sensing. For WE and RE, 30% cache utilization [30] is considered for all designs. Therefore, SRAM cache expends the leakage energy with the remaining 70% of idle time, whereas emerging NVMs do not (i.e., zero leakage). Among the current-based designs, the proposed (D)EIRW-VSH MRAMs show the lowest RT and RE. RE of the proposed designs is comparable to that of SRAM. Despite the write cost in the proposed MRAMs, WT and WE are lower than STT-MRAM. Compared with (D)GSH-MRAMs, WE is smaller in our designs. Furthermore, (D)EIRW-VSH MRAMs exhibit considerable area reduction compared with other memory solutions. However, these benefits come at the cost of lower SM (but also improved RT and RE) compared with STT- and GSH-MRAMs.

To summarize the benchmarking results, the WT associated with the switching of ferromagnets is limited to be in nano-second range, which makes it challenging for the proposed designs to surpass the SRAM performance. However, the major advantage of the proposed devices with respect to SRAM is their compactness and nonvolatility (yielding zero standby leakage). Therefore, for large memory capacities, the energy/area benefits of the proposed memories would be more prominent. If the material/device development (e.g., mobility of WSe2 and contact resistance at S/D contacts) is guided toward the right direction, this may help in achieving faster FM switching and thus lower write time and energy. The larger current obtained from the improved WSe2 mobility and contact resistance could also promote faster read and thus, improvement in the read time and energy.

IV. CONCLUSION

The previously proposed VSH-MRAMs are known for their compact layout and energy-efficient PMA-based write without the assistance of external magnetic field, but the high series resistance in read path degrades the memory SM. To mitigate this issue, we propose VSH-based nonvolatile spintronic devices featuring EIRW (EIRW-VSH devices) enabled by exchange coupling between FLs. Since the large series resistance is averted in our proposed designs, we observe a 1.9× improvement in SM at ~iso-RDM of ~80% at the device level compared with the previously proposed VSH devices. However, this comes at the cost of write efficiency as the exchange coupling between FLs increases write latency by 1.7× in the proposed devices. We also explore array design for the proposed EIRW-VSH MRAMs employing a shared read access transistor for every word. With comparable area, the proposed memory arrays achieve 39%–42% and 36%–46% reduction in read time and energy, respectively, along with 1.1×–1.3× larger SM compared with VSH-MRAM-based arrays, but at the cost of 1.7× and 2.0× write time and energy. We also observe that increasing the array size can further enhance the improvement in the aforementioned read performance and mitigate the cost of write efficiency in our design. Thus, the proposed EIRW-VSH design is suitable for applications in which reads are more dominant than writes, while the baseline VSH design may be more suitable for applications that require frequent writes.

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