Two-dimensional MoSi$_2$N$_4$: An Excellent 2D Semiconductor for Field-Effect Transistors

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Abstract—We report the performance of field-effect transistors (FETs), comprised of mono-layer of recently synthesized layered two-dimensional MoSi$_2$N$_4$ as channel material, using the first principles quantum transport simulations. The devices’ performance is assessed as per the International Roadmap for Devices and Systems (IRDS) 2020 roadmap for the year 2034 and compared to advanced silicon-based FETs, carbon nanotube-based FETs, and other promising two-dimensional materials based FETs. Finally, we estimate the figure of merits of a combinational and a sequential logic circuit based on our double gate devices and benchmark against promising alternative logic technologies. The performance of our devices and circuits based on them are encouraging, and competitive to other logic alternatives.

Index Terms—Field-effect transistors (FETs), Density functional Theory (DFT), Maximally-localised Wannier functions (MLWF), Non-equilibrium Greens function (NEGF), Quantum Transport (QT), Mono-layer (ML).

I. INTRODUCTION

THE two-dimensional (2D) semiconductors are promising channel materials for future technology nodes, owing to the ultrathin thickness (< 1 nm), no surface dangling bonds, and sharp turn-on of the density of states (DOS) at band edges [1]–[4]. In the last five years, there has been remarkable progress on synthesizing novel 2D semiconductors and several promising device concepts [5]–[7] have been demonstrated based on them. Also, the shortest MoS$_2$ transistor with 1 nm gate length has been fabricated, which shows a near-ideal sub-threshold swing of $\sim 65$ mV/decade and an ON/OFF current ratio of $\sim 10^6$ [8].

The 2D semiconductors materials library has been enriched due to their bulk, arranged in layered form, in which intralayers bonds are strong covalent bonds and weak Van der Walls (vdW) force connects inter-layers. Advanced experimental techniques have been used to isolate their layers from bulk. But, most bulk materials are non-layered (strong covalent bonds are strong covalent bonds and weak Van der Walls force connects inter-layers). Thus, the exfoliation process cannot create their 2D structure. Recently, Silicon has been introduced as a passivating during the CVD growth of non-layered molybdenum nitride (MoN$_2$) [9]. This process results in the growth of the centimeter-scale film of layered 2D MoSi$_2$N$_4$.

Mono-layer (ML) MoSi$_2$N$_4$ has excellent mechanical, electronic, optical, and thermal properties [9]–[13]. It is also a promising photocatalyst for water splitting and CO$_2$ reduction [10], [12]. It has been shown that ML-MoS$_2$N$_4$ has excellent stability (far better than other 2D semiconductors), using phonon, molecular dynamics (MD) calculations, and experimental testing. Even it can be handled, processed, and stored without any protective environment, unlike black phosphorus (In ambient conditions, black phosphorus (BP) can be easily etched due to chemical degradation [14]) and MoS$_2$ (In moist air below 373 K, its surface starts oxidizing [15]). The Young’s modulus and breaking strength for ML-MoS$_2$N$_4$ are $\sim 479$ GPa and $\sim 49$ GPa, respectively. These values are more than double of ML-MoS$_2$. ML-MoS$_2$N$_4$ is an indirect band gap semiconductor with the experimental band gap value of 1.94 eV. Its elastic constant is $\sim 4$ times of ML-MoS$_2$, and the carrier mobilities in it are $\sim 4$ times and $\sim 4$-6 times of ML-MoS$_2$ (the most widely studied 2D material for FETs application [8], [16]–[28]). Its lattice thermal conductivities [11], [12] are approximately 1.6 times silicon (Si) and much higher than other widely known 2D semiconductors [29]–[31] (ML-MoS$_2$, As, Sb, silicene and, ML-BP), but much lower than graphene [29], [32]. The high lattice thermal conductivity of ML-MoS$_2$N$_4$ ensures a high rate of heat removal through nano-electronic devices comprised of this material. Its optical transmittance is high ($\sim 97\%$) and comparable to graphene. The metal contacts to the ML of MoSi$_2$N$_4$ show exceptional physical properties with a large Schottky barrier height slope parameter, outperforming most other 2D semiconductors. CMOS compatible metals (Sc and Ti) also show excellent ohmic contact to ML-MoS$_2$N$_4$ with zero interfacial tunneling barrier [33], [34]. Overall, Mono-layer MoSi$_2$N$_4$ is an excellent semiconductor for logic applications. However, there is a need to investigate the transport properties of FETs based on ML-MoS$_2$N$_4$, and performance of integrated circuits (ICs) comprised of MoSi$_2$N$_4$ FETs.

Here, we exploit the capabilities of maximally localized Wannier functions (MLWFs) [35]–[37] to model electronic structure of ML-MoS$_2$N$_4$ and generate tight-binding (TB) like Hamiltonian for the targeted device dimensions. Next, we compute transport properties of n- and p-type devices based on this ML by solving coupled Poisson and Schrödinger equations in non-equilibrium Green’s functions (NEGF) formalism. We assess the performance of MoSi$_2$N$_4$ based FETs as per the requirements of International Roadmap for Devices and Systems (IRDS) 2020 roadmap for the year 2034 and compared to advanced silicon-based FETs, carbon nanotube-based FETs, and other promising two-dimensional materials based FETs. Finally, we estimate the figure of merits of a combinational and a sequential logic circuit based on our double gate devices and benchmark against promising alternative logic technologies. The performance of our devices and circuits based on them are encouraging, and competitive to other logic alternatives.
The channel length scalability of devices is also studied with their switching performance. Finally, the figure of merits (FOMs) of a combinational circuit (32-bit adder) and a sequential circuit (ALU) are estimated and benchmarked against promising logic technologies (CMOS and beyond-CMOS).

II. Computational Methods

Vienna Ab initio Simulation Package (VASP) [39], a tool based on DFT, is used to relax the atomic positions and calculate the electronic structure of ML-MoSi$_2$N$_4$. The Projector Augmented Wave (PAW) [40] pseudopotentials with plane-wave basis set are used for DFT calculations. The generalized gradient approximation (GGA) developed by Perdew-Burke-Ernzerhof (PBE) [41] is used to consider exchange and correlation effects. The energy cutoff of 400 eV is used for the plane-wave basis set, and the Brillouin zone integrations are performed using $12 \times 12 \times 1$ k-mesh.

The obtained Bloch/plane-wave states from DFT calculations are mapped to MLWFs using the Wannier90 suite of codes [42]. The obtained TB-like Hamiltonian in MLWF basis is used to construct the Hamiltonian for targeted device dimensions. In the transverse direction (channel width direction), periodic boundary condition (PBC) is considered with 30 uniform wave-vector samples. The constructed device Hamiltonian is used as input to solve coupled Schrödinger and Poisson equations in Non-equilibrium Green’s functions (NEGF) formalism [43]–[46]. Additional computational details are described in Appendix.

III. Results

A. Structural and Electrical Properties of ML-MoSi$_2$N$_4$

The two dimensional periodic replication of one Mo, two Si, and four N atoms, packed in honeycomb lattice, generate the ML of MoSi$_2$N$_4$ (see Fig. 1 (a) and (b)). This ML can be viewed as MoN$_2$ (2H – MoS$_2$ like structure) sandwiched between two buckled honeycomb SiN layers (see Fig. 1 (b)). The optimized lattice constant is $a(= b) \sim 2.90$ Å and the thickness of ML is $\sim 7.01$ Å. The optimized structural parameters agree well with the literature [10], [47], [48].

The electronic band structure of MoSi$_2$N$_4$ is plotted along with the high symmetry points (Γ–X–S–Y–Γ–S) in the orthogonal Brillouin zone (BZ). Figure. 2 (c) shows the BZ associated with hexagonal cell and orthogonal cell. Figure. 2 shows the band structure of MoSi$_2$N$_4$ obtained from DFT and MLWF-TB Hamiltonian. The band structure from MLWF-TB Hamiltonian shows a good match with DFT near VBM and CBM. It is an indirect band gap semiconductor with the conduction band maxima (CBM) lies in the way from Γ to X (equivalent to K in hexagonal BZ) and valence band maxima (VBM) at Γ. The curvature of CBM and VBM are isotropic, but the curvature of CBM is larger than the curvature of VBM. Hence, larger effective mass for holes ($m_h^*$) than electrons ($m_e^*$) i.e., $m_h^* > m_e^*$ (see Table I).

B. Device Structure and Electrical Characteristics

The Single gate (SG) and double-gate (DG) devices, using ML of MoSi$_2$N$_4$ as channel material, are investigated. Figure. 3 (a) and 3 (b) show the schematic of SG and DG devices, respectively. The geometrical parameters of the devices are gate length ($L_G$), channel length ($L_{Ch}$), source/drain extension...
Fig. 3: Schematic of (a) single gate (SG) and (b) double gate (DG) FETs. BOX layer and gate oxides are SiO₂, of thickness \( t_{\text{box}} \) and \( t_{\text{ox}} \), respectively, \( L_G \), \( L_{\text{UL}} \), and \( L_{\text{ch}} (= L_G + 2\times L_{\text{UL}}) \) are gate length, underlap length, and channel length, respectively. \( L_{S/D} \) is source/drain extension length. The source and drain are heavily doped with donors/acceptors for n-p-type devices. This doping results in the energy degeneracy of 50 meV.

\( L_{S/D} \), underlap length (UL), and oxide thickness \( (t_{\text{ox}}) \). For SG, \( t_{\text{box}} \) is BOX layer thickness with \( t_{\text{box}} = 10 \) nm. Silicon dioxide (SiO₂) is used as gate oxide and BOX layer. This work aims to assess the intrinsic performance of FETs based on the mono-layer of MoSi₂N₄. Hence, the S/channel/D doping used in the device simulations are n+/undoped (intrinsic)/n+ and p+/undoped (intrinsic)/p+ for n- and p-type devices, respectively. The S/D is doped such that the Fermi level is 50 meV above/below the conduction/valence band for n-FET/p-FET. The metal gate work function is tuned to get \( I_{\text{ds}} \) \( \sim 10^{-2} \, \mu\text{A}/\mu\text{m} \) (say it OFF-current \( (I_{\text{OFF}}) \) at \( V_{gs} = 0 \) V for all the simulated devices.

We start the investigation by simulating SG and DG devices with \( L_{\text{ch}} (= L_G) = 12 \) nm, equivalent oxide thickness (EOT) \( = 0.60 \) nm, and \( V_{DD} = 50 \) V. The source-to-drain tunneling is negligible for the devices with \( L_{\text{ch}} = 12 \) nm, and the band-to-band tunneling is negligible due to the high value of band gap in this ML. These device parameters are considered according to IRDS 2020 roadmap for the year 2034. According to the roadmap, the expected channel materials are germanium (Ge) and 2D materials, and the expected devices are 2D materials based devices and FeFETs for the year 2034 [38]. Figure [4] shows the transfer characteristics for n-FETs and p-FETs. In both types, DG configuration shows a steeper sub-threshold slope (SS) and higher \( I_{\text{ON}} \) than SG.

The SS for thermionic current is proportional to \( 1 + C_q/C_{\text{OX}} \) [49], where \( C_q \) is quantum capacitance and \( C_{\text{OX}} \) is oxide capacitance. For DG configuration, oxide capacitance is double than SG, hence DG devices show better SS than SG for \( L_{\text{ch}} = 12 \) nm. The stepper SS and higher value of \( C_{\text{OX}} \) in DG ensure higher \( \partial I_{ds}/\partial V_{gs} \) and higher mobile carrier concentration, respectively than SG, hence higher \( I_{\text{ON}} \) than SG. Defects and series parasitics resistance from contacts and S/D access regions are not included in our simulations, usually limiting the device’s performance.

1) Channel length Scaling: The channel length scaling is performed to study the scalability and immunity to source-to-drain tunneling (SDT) of ML-MoSi₂N₄ based FETs. The SDT plays a significant role in deteriorating device performance at short channel lengths. It is more severe for the low effective mass carriers than high effective mass, as the tunneling probability is proportional to \( \exp(−\sqrt{m^*}) \). Figures [5] (a), (b), (c), and (d) show the transfer characteristics of DG n-FET, DG p-FET, SG n-FET, and SG p-FET, respectively for various channel lengths \( L_{\text{ch}} = 12, 8, 5, 3 \) nm.

The impact of SDT is more for n-type devices than p-type because the curvature of CBM is greater than VBM. In DG, the device is more immune to SDT than SG as DG shows better gate controllability than SG. Hence, DG devices are more scalable than SG. The best scalable device is DG p-FET, and it can be scaled down to 5 nm. At \( L_{\text{ch}} = 5 \) nm, DG p-FET show SS \( \sim 65 \) and \( I_{\text{ON}}/I_{\text{OFF}} > 3 \times 10^4 \) for LP applications; For HP applications, it shows SS \( \sim 67 \) mV/decade and \( I_{\text{ON}}/I_{\text{OFF}} > 10^4 \).

Figure [6] shows the output characteristics of DG n-FET and p-FET with \( L_{\text{ch}} = 5 \) nm. Figure [7] shows \( I_{\text{ON}} \) and SS of n-FET and p-FET for various \( L_{\text{ch}} \) at three different values of \( I_{\text{OFF}} \). Also, for a full assessment of DG devices at short channel lengths, DIBL is estimated from the change in threshold voltage \( (V_{th}) \) obtained by varying \( V_{ds} \) from \( V_{low} = 50 \) mV to \( V_{DD} \). Figures [8] (a) and (b) show the variations of SS and DIBL with \( L_{\text{ch}} \), respectively. Figure [9] shows the variation of \( I_{\text{ON}} \) vs. \( L_{\text{ch}} \) for DG n- and p-FETs based on

| \( \alpha (\text{A}) \) | \( b (\text{A}) \) | \( E_{\text{CG}} (\text{eV}) \) | \( m_p^* \) | \( m_n^* \) | \( \Gamma / \Gamma^\text{-X} \) | \( \text{VBM/CBM} \) |
|---|---|---|---|---|---|---|
| MoSi₂N₄ | 2.90 | 7.01 | 1.842 | 0.478 | 1.184 | VBM/CBM |
ML-MoSi$_2$N$_4$ and other promising 2D materials. For both types, the ML-BP FETs show the highest $I_{ON}$ among others (the data is not shown in the figure). But, the stability of BP remains the primary concern. For n-type devices: (1) For $L_{Ch} > 5$ nm, ML-As, and ML-Bi$_2$O$_2$Se have high $I_{ON}$ than ML-MoSi$_2$N$_4$. However, the preparation of As can produce toxic arsenic trioxide, making its fabrication more complex, other than stability issue. ML-Bi$_2$O$_2$Se shows good environmental stability. But the short-channel effects are more in ML-As and ML-Bi$_2$O$_2$Se than ML-MoSi$_2$N$_4$. (2) ML-InSe shows the lower value of $I_{ON}$ than ML-MoSi$_2$N$_4$ and the $I_{ON}$ difference increases as we go below 5 nm channel length. However, compelling surface oxidation in InSe deteriorates mobility and causes uncontrollable current hysteresis in InSe FETs. (3) The ML-MoSi$_2$N$_4$ shows superior ON-state current than ML-MoS$_2$ FETs. For p-type devices: (1) Except InSe, the MoSi$_2$N$_4$ shows superior ON-state current than others for $L_{Ch} < 5$ nm.

(2) The $I_{ON}$ for ML-MoSi$_2$N$_4$ is very close to ML-Bi$_2$O$_2$Se and superior to others for $L_{Ch} > 5$ nm. BL-Bi$_2$O$_2$Se suffers from high leakage current due to small bandgap ($E_G \sim 0.18$ eV), and $I_{ON}$ is much lower than ML-MoSi$_2$N$_4$ for both n- and p-type devices.

2) Switching Performance of FETs: The delay and power dissipation product (PDP) are crucial figures of merit (FOMs) for logic applications. They determine switching speed and switching energy (energy per switching event), respectively. Figure. 10 (a) and (b) show the delay [$\tau = (Q_{ON} - Q_{OFF})/I_{ON}$] and PDP [=$(Q_{ON} - Q_{OFF})V_{DD}$] vs $L_{Ch}$, respectively for DG FETs. These switching parameters for advance Si FETs (Si FinFETs and Si Nanowire FETs) and carbon nanotube (CNT) FETs are also shown in Fig. 10. For MoSi$_2$N$_4$ FETs with $L_{Ch} = 3, 5, 8, 12$ nm, $\tau$ and PDP lies in range 0.022 – 0.082 ps and 7.33 – 51.7 aJ/$\mu$m, respectively. Overall, MoSi$_2$N$_4$ FETs switch faster with lower switching energy than advance Si FETs (0.22 – 0.48 ps, 55 – 182 aJ/$\mu$m) and CNT FETs.
Fig. 9: ON current vs $L_{Ch}$ for DG (a) n-FET and (b) p-FET devices. The data for several promising 2D materials [56]–[59] based DG devices, obtained from first-principle calculations ($I_{OFF} = 10^{-1} \mu A/ \mu m$), are also shown in same plot for comparison.

Fig. 10: (a) $\tau$ and (b) PDP vs $L_{Ch}$ for MoSi$_2$N$_4$ FETs. (c) Benchmarking of MoSi$_2$N$_4$ FETs against promising 2D materials based FETs. The performance of 1nm-$L_G$ MoS$_2$ FET is also shown for comparison.

Fig. 11: Comparison of (a) PDP vs $\tau$ and (b) active power vs standby power for a 32-bit adder based on ML-MoSi$_2$N$_4$ FETs against other promising logic technologies [60].

$\tau$ is varied from (0.046–0.184 ps, 26–58 aJ/\mu m). It is worth to notice that the theoretical limit on delay for non-tunneling barrier controlled binary logic switch is 0.04 ps [63]. Our non-tunneling devices ($L_{Ch} = 8 \text{ nm and 12 nm}$) have $\tau$ in the range 0.041–0.082 ps.

The switching performance of DG MoSi$_2$N$_4$ based FETs ($L_{Ch} = 12 \text{ nm}$) is benchmarked against other promising 2D materials based DG FETs [52], [56]–[58]. Other than 1 nm-MoS$_2$ FET, the channel length of other 2D materials based FETs are in the range 7–9 nm. The five best performing devices are BP armchair direction (AD) n-FET, InSe n-FET, InSe p-FET, MoSi$_2$N$_4$ n-FET, and MoSi$_2$N$_4$ p-FET, these have energy-delay product (EDP = PDP $\times \tau$) $< (4 \times 10^{-30} \text{ Js}/\mu \text{m})$. The BP armchair direction (AD) n-FET has best switching speed among these, followed by InSe n-FET, InSe p-FET, MoSi$_2$N$_4$ n-FET, and MoSi$_2$N$_4$ p-FET. The MoS$_2$ 1nm-$L_G$ FETs have lower switching energy than others, but p-FET and n-FET are $\sim 23$ times and $\sim 212$ times slower than MoSi$_2$N$_4$ p-FET, respectively. The EDP of our devices are close to high performing InSe p-FET ($2.64 \times 10^{-30} \text{ Js}/\mu \text{m}$) and BP AD n-FET ($2.15 \times 10^{-30} \text{ Js}/\mu \text{m}$). The best performing device is InSe n-FET with approximately one third EDP than our devices, and EDP of BP zigzag (ZZ) n-FET is approximately three times than our devices. Others (Bi$_2$O$_2$Se and MoS$_2$) have EDP ($25$–$603 \times 10^{-30} \text{ Js}/\mu \text{m}$) far from MoSi$_2$N$_4$ FETs. All the devices have $I_{OFF} = 10^{-1} \mu A/ \mu m$.

3) FOMs of 32-bit Adder and ALU: The FOMs of a combinational (32-bit adder) and a sequential logic circuit (32-bit ALU) based on MoSi$_2$N$_4$ FETs are estimated, using the methodology of [60]. The n- and p-type DG MoSi$_2$N$_4$ FETs with $L_{Ch} = 12 \text{ nm}$ are considered, and are sized to deliver same current. The 15 nm metal half pitch and 60 nm contacted gate pitch are taken, which results in interconnect capacitance ($C_{ic}$) = 0.0378 $\text{F}$ and interconnect delay ($t_{ic}$) = 0.1891 ps for $I_{OFF} = 10^{-1} \mu A/ \mu m$ (HP applications).
Using these data, the $\tau$ and PDP are calculated for inverter with fan-out of four ($\tau \times$ PDP $= 0.3984 \text{ps} \times 21.0382 \text{aJ}$), NAND gate with fan-in of four ($0.6379 \text{ps} \times 19.4914 \text{aJ}$), 32-bit adder ($111.32 \times 10^2 \text{ps} \times 21.1885 \times 10^3 \text{aJ}$), and ALU ($267.41 \text{ps} \times 2.2136 \times 10^4 \text{aJ}$) comprised of MoS$_2$N$_4$ FETs. Figure 11 (a) and 12 (a) show $\tau$ vs PDP for 32-bit adder and ALU, respectively based of MoS$_2$N$_4$ and other spintronics and electronics logic devices (these data are taken from [67]). The spintronics devices (ASL, CSL, MEMTJ, mLgic, CoMET, and SWD) based adder and ALU switch slower and consumes more energy than electronics devices. Among electronics devices, switching speed of MoS$_2$N$_4$ based adder and ALU is comparable to CMOS HP and ThinFET (WTe$_2$/SnSe$_2$ heterojunction interlayer TFET), but the switching energy of MoS$_2$N$_4$ is one order less than CMOS HP and comparable to TFET devices (ThinFET and GaSb/InAs heterojunction TFET). Further, we characterize the power consumption parameters of adder and ALU. Figures 11 (b) and 12 (b) show the standby power vs. active power for adder and ALU comprised of MoS$_2$N$_4$ FETs and other promising electronic devices. The standby power and active power of the circuits consisting of MoS$_2$N$_4$ devices are close to CMOS HP and more than TFET devices (ThinFET and GaSb/InAs heterojunction TFET).

IV. CONCLUSION

Two-dimensional semiconductors are promising candidates as a channel of next-generation electronic devices. In recent years, a new 2D semiconductor with the formula MoS$_2$N$_4$ has been discovered and gaining attention owing to its excellent physical and electronic properties. In this work, the performance of FETs based on recently discovered ML-MoS$_2$N$_4$ is assessed, using the first principles based quantum transport simulations. The upper-performance limit is reported, as the transport is assumed to be ballistic in nature. The scalability and impact of source-to-drain tunneling are investigated by physical and electronic properties. In this work, the performance is estimated as per the IRDS roadmap for the year 2034. The key FOMs for logic switches are calculated and benchmarked against other promising 2D materials-based FETs. It is found that the switching parameters of double-gate devices are better than advanced Si-FETs and CNT-based FETs. Finally, we calculate the FOMs of a combinational and a sequential logic circuit based on our double gate devices and benchmark against CMOS and beyond-CMOS logic technologies. The performance of 32-bit adder and ALU are promising among other alternative logic technologies.

APPENDIX

At each bias ($V_{gs}$, $V_{ds}$), the transmission coefficient can be expressed as,

$$T(E, k, V_{gs}, V_{ds}) = \text{Trace}[\Gamma S G^R(\Gamma_D G^A)],$$  \hspace{1cm} (1)
\(I_{ds}(V_{gs}, V_{ds}) = \frac{e}{\hbar} \int_{-\infty}^{\infty} \sum_k T(E, k, V_{gs}, V_{ds}) \left[f(E - \mu_s) - f(E - \mu_d)\right]dE\),

where, \(e\) is the electron charge, \(\hbar\) is the reduced Planck constant, \(T(E, k, V_{gs}, V_{ds}) = \sum_k T(E, k, V_{gs}, V_{ds})\) is the transmission coefficient at Energy \(E\) for a given bias \((V_{gs}, V_{ds})\), \(\mu_{s/d}\) is the chemical potential at source/drain, and \(f(E - \mu_{s/d})\) is the Fermi-Dirac distribution function at source/drain.

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