A Model Study of an All-Digital, Discrete-Time and Embedded Linear Regulator

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Abstract— With an increasing number of power-states, finer-grained power management and larger dynamic ranges of digital circuits, the integration of compact, scalable linear-regulators embedded deep within logic blocks has become important. While analog linear-regulators have traditionally been used in digital ICs, the need for digitally implementable designs that can be synthesized and embedded in digital functional units for ultra-fine grained power management has emerged. This paper presents the circuit design and control models of an all-digital, discrete-time linear regulator and explores the parametric design space for transient response time and loop stability.

Index Terms— discrete time digital linear regulator, low drop-out (LDO), limit-cycle oscillations, on-chip power delivery, transient modeling.

I. INTRODUCTION

With the growing need for higher energy efficiency in digital systems-on-chip (SoCs) and microprocessors, power management has emerged as a major design constraint. Both DC-DC conversion and voltage regulation continue to be actively researched for efficiency, compactness and faster response to provide ultra-fine grain spatio-temporal power management. On-chip power delivery networks are implemented in a hierarchical manner, combining slower and more efficient switching regulators with faster and less efficient linear regulators, to address power “hotspots” across multiple-voltage domains and wide dynamic operation [1]. Traditional low drop-out (LDO) regulators have been analog in nature and employ a high-gain error amplifier to provide regulation. They provide high bandwidth, low ripple, fast response times and high power supply rejection (PSR) [2], [3]. However, the use of analog design principles do not allow operation at low input and control voltages and are difficult to integrate as collaterals embedded deep within a digital functional unit. This has inspired the design of digital implementations of LDOs [4]-[7] targeted for digital load circuits. The rationale behind such designs is to convert the control section of an LDO into a digitally implementable circuit which is easier to integrate in scaled nodes. Secondly, it allows the designer to replicate and distribute such regulators in larger numbers on the die to provide ultra-fine grained

spatio-temporal power management.

Digitally implementable LDOs are implemented using either (i) continuous-time [4], [6] or (ii) discrete-time control. Discrete-time control [5], [7] uses a master clock that synchronizes all the data movement in the control portion of the regulator. This paper builds on top of [7] and provides an in-depth analysis of the discrete-time all-digital LDO, taking into account both the transient and steady state operations. The key contributions of this brief are:

1. Development of a z-domain control model of the LDO illustrating the relationship between key design parameters and transient response.
2. Development of a steady state model for assessment of limit cycle oscillations in the LDO.
3. Design space exploration of the LDO for performance, power efficiency and stability.

II. DESIGN OF DISCRETE-TIME ALL-DIGITAL LDO

Before presenting the model study of the digital LDO, let us explore the key design elements that have been proposed in [7] (Fig. 1). Design and simulations were performed using the IBM 130nm LP process. The regulated (or output) voltage ($V_{\text{OUT}}$) is synchronously sampled by a single-bit comparator which provides a binary ($V_{\text{REF}}>V_{\text{OUT}}$ or $V_{\text{OUT}}>V_{\text{REF}}$) signal. The comparator output (which in essence represents a 1-bit ADC) controls a programmable barrel shifter with parallel outputs to switch ON (or OFF) the power MOSFETs.

A. Comparator and shift stages

As proposed in [7], a single bit comparator provides a compact and efficient design. A clocked sense amplifier based topology is employed [8]. It obviates the need for constant bias current...
of a clock-less comparator. During the negative phase of the clock, the output is pre-charged to V_{DD}. At the positive clock edge, the faster discharging node resets the discharging process of the other one and the comparator output results in 1 if V_{IN} < V_{REF} or 0 if V_{IN} > V_{REF}. The decision is latched using an SR latch. A bi-directional barrel shifter takes input from the comparator and turns on/off a fixed number of power MOS devices using a thermometer code through a barrel shifter. It is set using a register programmable gain. In the present implementation, the shift register is 128 bits wide. A programmable gain of \{+3,+2,+1,-1,-2,-3\} is implemented through two levels of multiplexing. At the \textit{n}th barrel shifter output, the first level MUX takes \textit{A}_n, \textit{A}_{n-2} and \textit{A}_{n+2} as input to produce one of the intermediate values (\textit{B}_n) for the next level of MUXes. This allows a shift of \{0, +2, or -2\}. The other inputs on the second MUX levels are \textit{B}_{n+1} and \textit{B}_{n+1} which allow an additional \{+1, -1, or 0\} shifts, thus realizing the whole range of programmable gain as depicted in Fig. 2.

### B. Power PMOS Array

A total of 128 equally sized PMOS devices are connected as pass devices to regulate the output voltage. The exact size of each PMOS is dictated by the underlying process technology, the target voltage range and the load current specifications. In the current design, the PMOS array has a total area of 51.2 \mu m and is capable of delivering a maximum of 3.5 mA at a nominal output voltage of 0.7 V from a supply voltage of 1 V. The resistance offered by digital load circuit (\textit{R}_L) and the on-chip capacitance at the output from the grid, including all the parasitic and on-chip decoupling capacitances (\textit{C}_L), account for the total load. A grid and load capacitance of 1nF [6] has been assumed. The design can be fully integrated without the need for external capacitors.

## III. HYBRID CONTROL MODEL FOR THE REGULATOR

Small signal dynamics are modeled in the \(Z\)-domain to account for the all-digital control. The synchronous comparator can be represented by a subtraction followed by an impulse voltage sampler running at the clock frequency (\textit{F}_c). It gives a unit-less discrete time error sample at time \(nT\), as:

\[
\text{e}^* = V_{\text{REF}}(nT) - V_{\text{OUT}}(nT)
\]  

where \(T=1/F_c\). At every clock cycle the error is either +1 or -1 and in steady state it represents a bang-bang control. The barrel shifter acts as a perfect discrete time integrator as shown in Fig. 3. The output of the shifter, which is a thermometer coded digital word, \(D(nT)\), represents the number of PMOS devices that are on at any time instant, \(nT\). This discrete integration in the form of a difference equation is:

\[
D(nT) = D((n-1)T) + K_{\text{FORWARD}}e((n-1)T)
\]

(2)

The digital word is applied after a single cycle clock delay following synchronous operation of the LDO. \(K_{\text{FORWARD}}\) is the forward gain and is adjusted by setting the step-size in the barrel shifter \{+3,+2,+1,0,-1,-2,-3\}. From (2) we obtain:

\[
D(z)=K_{\text{FORWARD}}z^{-1}e(z)
\]

(3)

The output of the shifter interfaces with a continuous time plant (load circuit) through a zero order hold (ZOH). Direct transformation is employed to convert s-domain transfer function to \(Z\)-domain giving (4).

\[
P(z) = \frac{\text{OUT}(1-e^{-\text{F}_iT})}{\text{F}_i} \frac{1}{z-e^{-\text{F}_iT}}
\]

(4)

The load pole is at \(\text{F}_i = \frac{1}{(\text{R}_L \text{R}_{\text{PMOS}}) \text{C}_L}\) and \(\text{K}_{\text{OUT}}\) is the gain in the plant transfer function. \(\text{K}_{\text{OUT}}\) is proportional to \(I_{\text{PMOS}}\) and can be expressed as:

\[
\text{K}_{\text{OUT}} = \text{K}_{\text{DC}} I_{\text{PMOS}}
\]

(5)

Where \(I_{\text{PMOS}}\) is the current of a single ‘ON’ PMOS and is equal for equally sized PMOS devices in the array and \(\text{K}_{\text{DC}}\) is a DC proportionality constant. Thus using (3), (4) and (5) the open loop forward path transfer function of the digital LDO is written in the \(Z\)-domain as

\[
G(z) = \frac{K_{\text{FORWARD}}K_{\text{DC}}I_{\text{PMOS}}(1-e^{-\text{F}_iT})}{\text{F}_i} \frac{1}{(z-1)(z-e^{-\text{F}_iT})}
\]

(6)

This represents a second order system. The pole at (1,0) on the unit circle comes from the digital integration (equivalent to a single tap IIR filter) whereas, the second pole at \(e^{\text{F}_iT}\) is function of both load (\(\text{F}_i\)) and sampling frequency (\(\text{F}_c\)). Using unity feedback, the overall closed loop transfer function of the digital LDO in \(Z\)-domain is:

\[
H(z)=\frac{K}{z^2-(1+e^{-\text{F}_iT})z+e^{-\text{F}_iT}}
\]

(7)

where the open loop gain \(K = \frac{K_{\text{FORWARD}}K_{\text{DC}}I_{\text{PMOS}}(1-e^{-\text{F}_iT})}{\text{F}_i}\). Root locus of the closed loop poles as the open loop gain (\(K\)) increases as shown in Fig. 4a for two different load conditions. Similar to second order continuous time systems, the current system may also become oscillatory and can exhibit instability for high values of \(K\).

### A. Comparison of transient model and simulation

In this sub-section, we establish the notion of stability in digital LDOs and specify different parameters which affect its transient performance. Obtaining phase margin (PM) through Bode plots is not feasible in perfect integration systems like in
a digital LDO [9]. Therefore, PM is approximated in time domain. Given the percentage overshoot ($\delta$), the damping factor ($\zeta$) of the system is calculated using:

$$\zeta = \frac{\delta}{\sqrt{1 - \delta^2}}$$  \hspace{1cm} (8)

Then PM is given as $\zeta \times 100$. This approximation works well for second order systems to check for any potential instability at the boundary specifications. Fig. 4b shows changing PM for different load conditions of LDO obtained through HSPICE simulations. Increasing the open loop gain ($K$) moves the closed loop poles on the locus decreasing PM as shown in the Fig. 4. This establishes an upper bound on $K$ which can be ascertained through the model for a given $F_i$ and $F_s$. The two control knobs which a designer can exercise to change $K$ are the barrel shifter gain, $K_{\text{FORWARD}}$ and the $I_{\text{PMOS}}$. The size of each PMOS in the array is dictated by the load current specification during design time. During run-time $K_{\text{FORWARD}}$ can be used as a control parameter for variable proportional gain in the forward path. Fig. 5 illustrates the movement of the system poles and corresponding performance improvement as $K_{\text{FORWARD}}$ is increased. Change of $F_i$ brings the open loop output pole closer to the integrator pole, thus decreasing the PM. Hence, even with a low value of $K$, the designer can obtain faster transient response at an increased $F_i$. Step response for similar load conditions and $K_{\text{FORWARD}}$ but increased $F_i$ are compared in Fig. 6a. A 5X increase in $F_i$ is simulated for a load step of 1.5 mA from 0.9 to 2.4 mA. It shows over a 6X decrease in the rise time, from 0 V to within 5% of 700 mV, of regulated output voltage. Correspondingly, we see a change in the position of open loop poles for increasing values of $F_i$ as verified by the $z$-plane pole-zero plots in Fig. 6(b-d).

From HSPICE simulations we note that a 3X change in $K_{\text{FORWARD}}$ can achieve the same improvement in the transient response as a 2.5X increase in $F_i$ (comparing Figs. 5 and 6). While $K_{\text{FORWARD}}$ determines the position of the closed loop poles on the root locus, $F_i$ changes the position of one of the open loop poles and can thus actuate a faster transient response.

IV. STEADY STATE REGULATOR MODEL

Although the linear small signal models, as described in Section III allow us to qualitatively and quantitatively analyze the transient response and stability criteria in digital LDOs, such models fail to comprehend the steady-state behavior, in particular the role of limit cycle oscillations. Limit cycle oscillations are observed in digital LDOs [5] because of the hard quantization at the comparator input. Further, the delay between the sampling instant and the time of actuation through the PMOS devices plays a critical role in this regard.

A nonlinear sampled feedback system is proposed to capture this behavior (Fig. 7). The comparator in the feedback loop exhibits the transfer characteristics of an ideal relay with zero dead-time. All other components take the same form as presented in Section III. Such a system with a hard nonlinearity i.e., an ideal relay, shows limit cycle oscillations and lends itself to be analyzed in terms of describing functions [10]. At every positive clock edge, the comparator (or relay) will turn on or off a PMOS giving a periodic output. For example, a sequence $\{+1 +1 -1 -1 -1\}$ exhibits a limit cycle and will be referred to as a mode-3 oscillation. Here mode refers to the number of switching power PMOSes in steady state. Any other explicit delays in the loop can also be
incorporated in the following holistic analyses.

Following Fig. 7, let us determine the condition for mode-n to exist. In a limit cycle, the input to the relay, x(t), is sinusoidal. At y(t), ‘n’ PMOS devices switch in a single cycle of frequency ω₁/2n and satisfies mode-n. Each sample at y(t) is separated by a maximum of (360/2n)° for mode-n. If one of the sampling instants is assumed to be at the origin then the following is the necessary criteria for mode-n to exist.

\[
x(t) = A \sin \left( \frac{\omega_1}{2n} t + \phi \right); \quad 0 < \phi < \frac{180^\circ}{n}
\]

where A is the amplitude of the ripple and ϕ is the phase term with respect to an assumed origin of x(t). y*(t) samples the relay output, y(t). The fundamental component of these samples is advanced by (180/2n)°. If each sample y*(t) is of amplitude D then [y*(t)] is:

\[
[y^*(t)] = \frac{2D}{\omega_1} n^T \quad \frac{y(t) \sin \left( \frac{\omega_1}{2n} t + 180^\circ \right)}{2n} dt
\]

This integration is solved as a summation of impulses in one cycle. It should only include one of the two endpoint samples. From [10], the sampled describing function is given as:

\[
N(A, \phi) = \frac{\text{phasor representation of fundamental component of } y^*(t)}{\text{phasor representation of } x(t)}
\]

Then for mode-n it reduces to:

\[
N(A, \phi) = \frac{2D}{\omega_1} n^T \quad y(t) \sin \left( \frac{\omega_1}{2n} t + 180^\circ \right) dt
\]

The sinusoidal response function for the linear part is given by

\[
L(j\omega) = H(j\omega)Z(j\omega)S(j\omega)
\]

Here S gives the discrete integration and the clock cycle delay. Z represents the ZOH followed by H as the load frequency response. L(j\omega) is evaluated at the oscillation frequency of \( \omega = \omega_1/2n \) which simplifies to:

\[
L\left(j\frac{\omega_1}{2n}\right) = \frac{1 - e^{-j(\frac{\omega_1}{2n})T}(e^{-j(\frac{\omega_1}{2n})T} - 1)}{1 - e^{-j(\frac{\omega_1}{2n})T}(e^{-j(\frac{\omega_1}{2n})T} - 1)}
\]

For a limit cycle to exist, according to the Nyquist criterion

\[
N(A, \phi)L\left(j\frac{\omega_1}{2n}\right) = -1 = 1 - 1Z - 180^\circ \quad 0 < \phi < \frac{180^\circ}{n}
\]

Comparing the phase terms in (15) and applying the inequality gives the bounds of \( F_s^{\pm}_{F_1} \) for which mode-n can exist.

Similarly, all the necessary bounds of relevant modes can be calculated for the proposed LDO by evaluating (15) within the phase constraints. Loop gain also needs to be greater than 0 dB to achieve the sufficient conditions for a given mode to exist. Loop gain is numerically computed through simulations and model calibration. We note a good corroboration of the proposed model with simulations. Control propagation delay in the loop and any delay in the output voltage grid are negligible compared to the clock frequency (typically 10-100 MHz). Similar necessary conditions for different modes can be found following the same analysis. Fig. 8 summarizes the results for the given design.

V. PARAMETRIC DESIGN TRADE-OFFS AND OPTIMIZATIONS

From the control model described in section III and the steady state model described in section IV, it becomes clear that the choice of F_s plays a major role in ascertaining both the stability and performance of a digital LDO. Further, as F_s increases the mode of limit-cycle oscillation also increases.

The delay of one clock cycle in the baseline design (see Fig. 7) can be reduced by changing the clocking mechanism. If the comparator samples on the positive clock edge and the barrel shifter updates its output at the following negative edge then the transport delay reduces to half of a clock cycle. Following a procedure similar to that of Section IV, we can determine the bounds on the limit cycle modes for a given F_s/F_1. We note a reduction of the limit cycle mode at iso-F_s/F_1. The results from the proposed model and simulations are summarized in Fig. 9.
A design space exploration is carried out for optimally designing a practical digital LDO. An exponential reduction in the rise time \( T_r \) is achieved for higher values of \( F_s/F_L \) with diminishing returns as \( F_s/F_L \) approaches 20. Current efficiency decreases linearly with increasing \( F_s \), but drops exponentially as \( F_s/F_L \) ratio approaches 20. HSPICE simulation results for dual edge LDO are summarized in Fig. 10a, where the current consumed by the LDO’s control logic increases from 2\( \mu \)A to 10\( \mu \)A as \( F_s/F_L \) increases from 2 to 17. In the same span, \( T_r \) improves by more than 600\%. An optimal trade-off between power consumption and transient performance is obtained when \( F_s/F_L \) ranges from values of 5 to 10. On the other hand, \( F_s \) has a non-monotonic effect on the output voltage ripple. Increasing \( F_s \) tends to reduce the output ripple as the load capacitor performs better filtering of the steady state oscillations. However, it increases the mode of limit cycle oscillations. Thus the net output ripple is a resultant of these two effects. For lower values of \( F_s/F_L \), an exponential decrease in the output voltage ripple is first obtained and it tends to flatten out as \( F_s/F_L \) becomes higher. A large increase in the ripple is obtained when the mode increases. Fig. 10b illustrates the simulated output ripple as a function of \( F_s/F_L \) for a particular design instance showing a non-monotonic behavior. Thus we note that for an optimal design, it is necessary to select \( F_s \) to match \( F_L \) for some specification of the output ripple. As a rule of thumb, \( F_s/F_L \) in the range of 5 to 10 provides maximum performance gain while maintaining output ripple and power efficiency.

In summary, we note that the optimal trade-offs of transient rise time, power consumption and output voltage ripple is obtained when \( F_s \) is 5 to 10 times higher than the value of \( F_L \). Therefore, \( F_s \) should track \( F_L \) for optimal performance. As the output load current (and hence \( F_s \)) changes, a worst case or an adaptive design [7] principle can be employed. In light load conditions, a low \( F_s \) can optimize power consumption and still provide regulation. The upper bound on \( F_s \) is determined by the transient response time and conditions for stability. The design space (\( K_{\text{forward}} \) vs \( F_s/F_L \)) shown in Fig. 11 illustrates the regions of stable operation and the iso-\( T_r \) contours.

VI. CONCLUSION

An all-digital discrete time LDO for fine-grained power management of digital circuits is described in this paper. Theoretical models for analyzing the transient and steady state response of the LDO are corroborated with HSPICE simulations using a commercial process design kit. The role of the design topologies and parameters like clock frequency, dual clock edge triggering, barrel shifter based open-loop variable gain have been explored and shown to provide the designer with control over the transient and steady-state performance. A sampling clock frequency which is 5X-10X of the load pole frequency has been shown to provide an optimal trade-off among performance, power and steady-state output ripple.

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