Retraction

Retraction: Performance of CH-DVR during Phase Angle Jump and Fault Riding (J. Phys.: Conf. Ser. 1916 012011)

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[1] Cabanac G, Labbé C and Magazinov A 2021 arXiv:2107.06751v1

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Performance of CH-DVR during Phase Angle Jump and Fault Riding

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Abstract. In this paper, a seven-level cascaded H-Bridge dynamic voltage restorer (CHDVR) is proposed to mitigate power quality issues in the power system that are causing severe problems both in industrial and commercial sectors which may sometimes lead to interruption of power. To improve the voltage quality, many series compensators are being used in which DVR is one best solution wherein in many cases phase angle jump is not considered during the initial stage of compensation which influences the power quality. In this paper voltage Phase Angle Jump (PAJ) is taken into consideration to improve voltage quality using DVR. Moreover, Fault riding capability (FRC) is also considered along with phase jump to progress overall execution of the power system. The control strategy adopted is worked out for several sag cases and the analysis is validated using results acquired from MATLAB/SIMULINK 2019 platform.

1. Introduction
Consumption of power is increasing day by day with the growing population and the usage of equipment working with power. For reliable operation of equipment at the consumer end, the Power system should be free from power quality issues like voltage sags, low power factor, voltage transients, and so on. To overcome the issues in power system, power electronics as an advanced technology plays an important role in sustainability and good efficiency [1]. In finding the best technologies to overcome the power quality issues, different types of series compensators are to be installed in the power grid [2]. One diplomat application among many is the dynamic voltage restorer (DVR). It is a static var device having applications in a range of transmission and distribution systems [3-4].

The typical layout of DVR mainly consists of a voltage source converter, an energy storage system, a coupling transformer, and an output filter [5]. DVR is connected in series with the point of common coupling (PCC) between the source and the load.

Under normal operation i.e., during the healthy conditions, the DVR remains in standby mode and during the increase or decrease of voltage from supply to its minimal value, the DVR controller injects the voltage into PCC accordingly.

The proposed system uses a cascaded H-Bridge inverter which proved its performance when compared to the other two basic multilevel inverter topologies. The structure and operation of the
inverter are presented in [6-7]. Here 7 level topology is implemented which uses 3 separate DC sources and 3 H-Bridges with 4 switches in each H-Bridge.

This paper mainly aims with the compensation of sag in the of the power system for improving quality of voltage for sensitive loads with the help of proposed CHDVR by considering Phase Angle Jump (PAJ)and also Fault Riding Capability (FRC) and adopting a mathematical model of the proposed system. The obtained results are validated using MATLAB-2019(a)/ SIMULINK Environment.

2. CH-DVR Topology

The CH-DVR topology is based on a Multilevel inverter and is shown in Figure 1.

![Figure 1. Topology of CHDVR system.](image)

I. Conventional Method

Case (i): The depth of voltage sag percentage \( K_{sag} \) should have the relation as in Equations (1) and (2)

\[
K_{sag} \leq 1 - \cos(\theta_L) \\
K_{sag} = \left( \frac{V_{Lref} - V_L}{V_{Lref}} \right) 
\]

where \( \theta_L \) gives load power factor angle, \( V_{Lref} \) gives load voltage reference value, \( V_S \) and \( V_L' \) represents the grid side rated voltage and the voltage with sag. The \( V_{DVRf} \) is at right angles to \( I_L' \) shown in Figure 2(a). Phase angle RMS value of \( V_{DVRf} \) are given as in Equations (3) and (4)

\[
\theta_{DVR} = \pi - \arccos \left[ \frac{(V_S' + (V_{DVRf})^2 - (V_L')^2)}{2V_S'V_{DVRf}} \right] 
\]

The Phasor \( V_L \) is the voltage before sag and \( V_L' \) is the load voltage after the sag [8].The Phase angle jump exists, even if the DVR safeguard the sensitive load in opposition for sag in voltages of the grid with the help of energy–improved procedures which is as shown in 2(a).

An improved technique is proposed in [9] to correct the PAJ on load voltage as shown in 2(b) which is represented by a blue colored curve. Figure 3 shows the Active (real) power representation of DVR model in voltage rectification state
Figure 2. Phasor Diagram of Voltage rectification state (a) Reactive power rectification. (b) Improved system with a smooth changeover when Ksag<1- cos(θL). (c) Improved system for a smooth changeover when Ksag>1- cos(θL).

Phase Angle RMS value of $V_{DVRi}$ is given as in Equations (5) and (6)

$$V_{DVRi} = \sqrt{(V_{presag})^2 + (V_s^2)^2 - 2V_{presag}V_s\cos(\sigma)}$$

$$\theta_{DVRi} = -\left\{ \pi - \arccos \left( \frac{(V_{DVRi})^2 + (V_s')^2 - (V_{presag})^2}{2V_sV_{DVRi}} \right) \right\}$$

Figure 3. Active (real) power representation of DVR model in voltage rectification state. (a) Ksag>1 - cos(θL). (b) Ksag ≤ 1 - cos(θL).

In the transition stage, DVR consumes a definite amount of non-reactive power from the side of the DC link which is shown in the blue line.

Case (ii): If the voltage sag is $V_s'$ with Ksag>1 - cos(θL), here correction of sag with non-active power is not feasible. With the lowest active power injection, in order to attain voltage compensation, $V_s'$ has to follow the direction of $I_L'$. Now, the RMS value of $V_{DVRf}$ can be obtained as in Equations (7)

$$V_{DVRf} = \sqrt{(V_s')^2 + (V_s')^2 - 2(V_s')(V_s')\cos(\theta_f)}$$

Here, the DVR consumes a certain amount of non-zero active power in a steady-state and is shown with red-colored line.
II. Adapted Energy Recovery Principle:

1) Adapted Energy Recovery Principle of Operation: In this stage, DVR will guarantee the load side voltage quality with the phase jump improvement not only in the initial and later stages but also retrieves voltage of DC link very quickly.

![Vector diagram for DVR workable recovery](image)

**Figure 4.** Vector diagram for DVR workable recovery. (a) when $K_{sag} < 1 - \cos(\theta_L)$. (b) With a flexible changeover when $K_{sag} > 1 - \cos(\theta_L)$.

After overcoming the disturbances, the voltage of the system reaches the usual point where $V_s' = V_{presag}$ and $\sigma = 0$. By the injection of instantaneous voltage $V_{inj}$ as shown in Figure 4(a), the phase angle jump can be avoided after elimination of fault which is dependent on the change in the voltage rectification state.

In the recovery state, the injected voltage satisfies the relation as in Equations (8-11)

$$V_{presag} + V_{inj} = V_L$$

(8)

From Figure 4, the $\alpha_r$ can be written as

$$\alpha_r = \begin{cases} 
\theta_L + \sigma & \text{if } K_{sag} > 1 - \cos(\theta_L) \\
\theta_L + \theta_{DVRf} + \pi/2 - \sigma & \text{if } K_{sag} \leq 1 - \cos(\theta_L) 
\end{cases}$$

(9)

Now the RMS value of the injected voltage is given as

$$V_{inj} = \sqrt{\left(V_L'\right)^2 + \left(V_{presag}\right)^2 - 2\left(V_L\right)\left(V_{presag}\right)\cos(\alpha_r)}$$

(10)

From initial to the final operating point, Mode 2 transition is given as

$$\theta_{trans} = \theta_f + \Delta_2(\theta)$$

(11)

$V_L'$ reaches final place like $V_{presag}$ after flat mutation which is presented in Figure 4(b).

2) Self-Recovery Principle of Operation: During $\Delta_2$, DVR will work as a positive capacitive load and is used in DVR energy recovery. The amplitude of $V_L$ is the same as $V_s$ as shown in Figure 5 and the DVR injects voltage $V_{inj}$. Here, the self-recovery of the energy of the DC link can be noticed. The active power supplied is given by Equation (12)

$$P_m = V_s I_s \cos(\phi - \alpha) - V_L I_L \cos(\theta)$$

(12)
Figure 5. The vector diagram of the smooth switching for the preliminary state of self-recovery.

Here, the active power which is supplied depends upon the value of $\alpha$. By taking $V_L'$, $V_{\text{presag}}$ as 1 p.u. and $\alpha_{\text{max}} = \theta_i$, it is clear that the DVR absorbs higher power and is given by Equations (13), (14) and (15)

$$P_{\text{max}} = S_L \left[ 1 - \cos (\theta_i) \right]$$

(13)

The injected phase angle of voltage and magnitude are given as

$$\gamma = \pi - \frac{1}{2} (\pi - \alpha_s) = \frac{1}{2} (\pi + \alpha_s)$$

(14)

$$V_{ij} = \sqrt{V_L^2 + V_s^2 - 2V_LV_s \cos (\theta_i)}$$

(15)

3) Advanced Energy Self-recovery Principle of Operation:

Here, the important thing is to obtain the energy recovery by handling the voltage of the DC link close to the recommended value along with bringing the DVR to the highest operating end for obtaining smooth access. The total switching process is represented in Figure 5. The complete operation representing DVR inside the energy recovery state is explained in 3 modes:

Mode 1: When $V_{\text{SC}} > V_{\text{SCmin}}$, the operation of energy self-recovery be disabled with the power generated by the DVR is very small after the disappearance of sag. By which mode 2 is enabled with smooth changeover as represented in Figure 6 with a black-colored line shown from $t_1$ till $t_2$.

Mode 2: When $V_{\text{SC}} < V_{\text{SCmin}}$, the operation of energy self-recovery is enabled by which controller retain the working of DVR at the recovery operation initial point after the voltage sag disappears and is remained same until $V_{\text{SC}} > V_{\text{SCref}}$. By which mode 2 is enabled with smooth changeover as represented in Figure 6 with red-colored line from $t_3$ till $t_6$.

Mode 3: In the general case, by the smooth changeover of mode 3, energy self-recovery operation is launched to restore the DC link voltage. Until $V_{\text{SC}} > V_{\text{SCref}}$, the DVR is remained to work at the maximum operating point of the recovery stage, and hence entered the smooth changeover mode 2 which is represented in Figure 6 with a blue-colored line from $t_3$ till $t_6$. 
3 Control Scheme and Parameter Selection

i) Control scheme: A new type of cascaded inverters is also proposed for better reliability of the system [10]. A lot of research has been done on the control schemes of CH-DVR [11].

Figure 7 shows the proposed control system. To understand the voltage rectification, injected voltage reference angle is to be calculated and is done by the phase calculation block to calculate the angles \( \theta_{DVRf} \) and \( \theta_{DVRi} \). Similarly to understand the energy self-recovery stage, \( \gamma \) is to be calculated.

Using a stationary reference frame, the DVR reference voltage \( V_{DVRref} \) or \( V_{Injref} \) are compared through the predefined voltage. To track \( V_{DVRref} \) or \( V_{Injref} \) precisely, PI controller is proposed.

ii) Parameter Selection:

Cascaded H-Bridge inverter design:

By using the PWM technique, the switches in CH-DVR should satisfy the relation as in Equations (16-22)

\[
V_{DVRref} = \sqrt{(V_{x})^2 - (V_{L} \cos \theta_{x})^2} \\
N_P \geq \frac{(V_{L})}{I_L}
\]

(16)

(17)

Now, the rated voltage of DC-link with each inverter level \( V_{DCH} \) should be

\[
\frac{V_{DVR}}{n} \leq V_{DCH} \leq N_P V_r
\]

(18)

The overall minutest capability in the switching mechanism can be deduced as
\[ S_{\text{max, overall}} = n N_{\text{max}} N_{\text{Pmax}} V_r I_r \geq V_{\text{DVR}} I_L \]  \hspace{1cm} (19)

So, one can say that the capability in the switching mechanism depended on \( V_r \) and \( I_r \) and can be changed by changing turns-ratio \( k \), \( N_{\text{S min}} \) and \( N_{\text{P min}} \).

Ride-through capability:
The active (real) power injected by the CH-DVR, when the voltage sag is assumed as \( V_{\text{SAG}} \) in pu without phase angle jump is given by
\[ P_{\text{DVR}} = -\frac{C_{\text{dc}} u_{\text{dc}} du_{\text{dc}}}{dt} = \sqrt{3} V_L \cos \phi (1-V_{\text{SAG}}) \]  \hspace{1cm} (20)

If \( T_{\text{sag}} \) is the duration of voltage sag, the supplied energy by CH-DVR is
\[ W_{\text{sup}} = \int_{t_s}^{t_s+T_{\text{sag}}} (-C_{\text{dc}} u_{\text{dc}} du_{\text{dc}}) dt = \int_{t_s}^{t_s+T_{\text{sag}}} P_{\text{DVR}} (1-V_{\text{SAG}}) dt \]  \hspace{1cm} (21)

LC design:
Apart from the high switching frequency of the cascaded H-Bridge MLI, there exist many higher harmonic components close to the equivalent switching frequency. For compensating them, a LC-based filter is proposed by taking \( \rho = (0.5 \sim 0.8) R_L \) as given
\[ L_f = \frac{\rho^2}{2 \pi f_c} \]
\[ C_f = \frac{L}{\rho^2} = \frac{1}{2 \pi f_c \rho} \]  \hspace{1cm} (22)

Where \( R_L \) is given as
\[ R_L = \frac{3 V_{\text{DC}}^2}{P_{\text{DVR}}} \]  \hspace{1cm} (23)

4 Results and Discussion

A single-phase CH-DVR topology is simulated in MATLAB/SIMULINK and the execution of the anticipated control scheme is verified for different values of sag by taking sample time as 20 µs.

Figure 8 shows the output in the voltage rectification stage. Here during 0.2~0.3s, the voltage of the system reduces to 0.8 p.u. which shows that with possible switching control, the DVR can smoothly go through and out the state of least energy rectification, which guarantees the minor Phase Jump towards the voltage of the load.

![Figure 8. Voltage rectification during K sag value is 0.8 p.u.](image)

Figures 9-11 shows the self-recovery stage of CH-DVR which is initiated at 0.40 s. The values of \( V_{\text{DC}} \) and \( V_{\text{DVR max}} \) are set at 300V and 250V respectively.
Figure 9. CH-DVR in self-recovery

Figure 10. Preliminary flexible handover in optimal energy self-recovery state.

Figure 11. CH-DVR Performance. From top to the bottom: (a) the source voltage $V_s$, (b) the voltage of load $V_L$, (c) the voltage of secondary $V_{DVR}$, (d) the current of the load $I_L$. 

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5. Conclusion
In this paper, a CH-DVR system is presented with a mathematical model which deals with different sag voltages and energy self-recovery. The proposed system will enhance the quality of voltage of sensitive loads by safeguarding them during the sag in the grid voltage against phase angle jump. Moreover, the Fault riding capability of DVR is also presented. To observe the helpfulness of the presented model, simulation results of DVR are verified under various cases.

References
[1] Santhoshi. B. K., Mohanasundaram. K. & Kumar. L. A., ANN – based dynamic control and energy management of inverter and battery in a grid-tied hybrid renewable power system fed throughwitched Z-source converter. ElectrEng (2021).
[2] P. T. Cheng, C. C. Huang, C. C. Pan, and S. Bhattacharya, Design and implementation of a series voltage sag compensator under practical utility conditions, IEEE Trans. Indus. Applica., vol. 39, no. 3, pp. 844-853, May/Jun. 2003.
[3] F. M. Mahdianpoor, R. A. Hooshmand, and M. Ataei, A new approach to multifunctional dynamic voltage restorer implementation for emergency control in distribution systems, IEEE Trans. Power Del., vol. 26, no. 26, pp. 882-890, Apr. 2011.
[4] N. H. Woodley, L. Morgan, and A. Sundaram, “Experience with an inverter-based dynamic voltage restorer,” IEEE Trans. Power Del., vol. 14, no. 3, pp. 1181-1186, Jul. 1999.
[5] A. Moghassemi, S. Padmanaban, Dynamic voltage restorer (DVR): a comprehensive review of topologies, power converters, control methods, and modified configurations, Energies, vol. 13, no. 16: 4152, 2020.
[6] Y. T. R. Palleswari; S. S. R. SarathbabuDuuvvuri, State Estimation for Cascaded Hybrid Multi-level Inverter Fed Induction Motor Drive Using Derivative-free Extended Kalman Filter, 2018 8th IEEE India International Conference on Power Electronics (IICPE).
[7] Haldorai, A. Ramu, and S. Murugan, Social Aware Cognitive Radio Networks, Social Network Analytics for Contemporary Business Organizations, pp. 188–202. doi:10.4018/978-1-5225-5097-6.ch010
[8] R. Arulmurugan and H. Anandakumar, Region-based seed point cell segmentation and detection for biomedical image analysis, International Journal of Biomedical Engineering and Technology, vol. 27, no. 4, p. 273, 2018.
[9] C. Meyer, R. W. Doncker, X. W. Li, and F. Blaabjerg, Optimized control strategy for a medium-voltage DVR—theoretical investigations and experimental results, IEEE Transactions on Power Electronics, vol. 23, no. 6, pp. 2746–2754, Nov. 2008.
[10] S. Pengwei, C. C. Liang, L. Jih-sheng, and L. Chuang, Cascade dual-buck full bridge inverter with hybrid PWM technique, in Proc. 2012 17th Annual APEC, Orlando, FL, 2012, pp. 113-119.
[11] H. K. Al-Hadidi, A. M. Golc, and D. A. Jacobson, A novel configuration for a cascade inverter-based dynamic voltage restorer with reduced energy storage requirements, IEEE Trans. Power Del., vol. 23, no. 2, pp. 881-888, Apr. 2008.