Performance Enhancement in N₂ Plasma Modified AlGaN/AlN/GaN MOS-HEMT Using HfAlOₓ Gate Dielectric with Γ-Shaped Gate Engineering

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Abstract: In this paper, we have demonstrated the optimized device performance in the Γ-shaped gate AlGaN/AlN/GaN metal oxide semiconductor high electron mobility transistor (MOS-HEMT) by incorporating aluminum into atomic layer deposited (ALD) HfO₂ and comparing it with the commonly used HfO₂ gate dielectric with the N₂ surface plasma treatment. The inclusion of Al in the HfO₂ increased the crystalline temperature (∼1000 °C) of hafnium aluminate (HfAIOₓ) and kept the material in the amorphous stage even at very high annealing temperature (>800 °C), which subsequently improved the device performance. The gate leakage current (I_{G}) was significantly reduced with the increasing post deposition annealing (PDA) temperature from 300 to 600 °C in HfAIOₓ-based MOS-HEMT, compared to the HfO₂-based device. In comparison with HfO₂ gate dielectric, the interface state density (D_{it}) can be reduced significantly using HfAlOₓ due to the effective passivation of the dangling bond. The greater band offset of the HfAIOₓ than HfO₂ reduces the tunneling current through the gate dielectric at room temperature (RT), which resulted in the lower I_{G} in Γ-gate HfAIOₓ MOS-HEMT. Moreover, I_{C} was reduced more than one order of magnitude in HfAIOₓ MOS-HEMT by the N₂ surface plasma treatment, due to reduction of N₂ vacancies which were created by ICP dry etching. The N₂ plasma treated Γ-shaped gate HfAIOₓ-based MOS-HEMT exhibited a decent performance with I_{DMAX} of 870 mA/mm, G_{DMAX} of 118 mS/mm, threshold voltage (V_{TH}) of −3.55 V, higher I_{ON}/I_{OFF} ratio of approximately 1.8 × 10⁹, subthreshold slope (SS) of 90 mV/dec, and a high V_{BR} of 195 V with reduced gate leakage current of 1.3 × 10⁻¹⁰ A/mm.

Keywords: AlGaN/AlN/GaN; MOS-HEMT; HfAIOₓ; HfO₂; interface trap density; post-deposition annealing (PDA); Γ-shaped gate; flicker noise

1. Introduction

In recent years, the wide band gap semiconductors have been widely used in high power electronic applications due to its high power density and high power conversion efficiency [1]. As of today, the AlGaN/GaN based high electron mobility transistors (HEMTs) are the most promising devices for high power and high frequency applications due to their unique properties such as wide band gap (3.4 eV of GaN), large breakdown field (>3 MV/cm), high density of two-dimensional electron gas (2 DEG) (∼10¹⁵/cm²), low intrinsic carrier density, and high saturation velocity (∼2 × 10⁶ cm²/V·s) [2–5]. Due to the safety and power saving concerns, the recessed gate GaN-based HEMTs are desirable to realize the normally-off operation [6]. However, Ki-Sik et al. and Zhe et al. reported that the electron transport characteristics could be seriously affected by the interface states in fully recessed HEMTs, due to the completely etched AlGaN barrier layer [7,8].

In order to avoid the degradation of the transport characteristics of the carrier the partially recessed GaN HEMT structure was proposed [9]. The Cl₂-based inductive coupled...
plasma (ICP) dry etching has been widely used, to realize the partially recessed-gate structure. However, the gate recess process induced the trap states in the device, leading to the severe gate leakage, worse current collapse, and very low breakdown voltage ($V_{BR}$) [6,10]. Baik et al. reported that the N$_2$ plasma treatment could effectively improve the surface morphology and ohmic contacts in GaN HEMTs by reducing the N$_2$ vacancies, created by ICP dry etching [11].

In addition to the N$_2$ surface treatment, to reduce the gate leakage current significantly, the metal oxide semiconductor high electron mobility transistor (MOS-HEMT) with an insulating dielectric have also been widely investigated. Numerous gate dielectrics have been experimented, such as SiO$_2$ [12], AlN [13], Al$_2$O$_3$ [14], MgCaO [15], HfO$_2$ [16], ZrO$_2$ [17], TiO$_2$ [18], etc. The dielectric layer not only can suppress the gate leakage current, but also can be used as a passivation layer to suppress the current collapse phenomenon [19]. Among the many used dielectrics, HfO$_2$-based MOS-HEMTs can achieve much more efficient electrostatic control due to their high dielectric constant ($k$). However, due to the insufficient barrier height, the HfO$_2$-based GaN MOS-HEMT suffers from a high gate leakage current, which subsequently deteriorates the device performance [20]. Thus, to reduce the gate leakage current without the reduction of gate controllability, the HfO$_2$-based stack gate dielectric layer such as HfO$_2$/Y$_2$O$_3$ [21], HfO$_2$/Al$_2$O$_3$ [16], HfO$_2$/AlN [22] or Hf-ternary oxide HfSiO$_x$ [20], HfZrO [23], etc. have also been investigated. However, owing to the lower crystalline temperature, e.g., Y$_2$O$_3$ (~<425 °C) [24] and HfZrO (500–550 °C) [25], the respective MOS-HEMT might not be applicable in a high temperature.

A previous study has shown that the inclusion of Al into HfO$_2$ could improve the interface properties and reduce the gate leakage current in hafnium aluminate (HfAlO$_x$)-based MOS-HEMTs [26,27]. HfO$_2$ provides a high dielectric constant ($k$ ~ 25) but poor conduction band offset to GaN (~1.51 eV), while Al$_2$O$_3$ offers a larger conduction band offset to GaN (~1.96 eV) but it has a relatively lower dielectric constant ($k$ ~ 9) [27]. To improve the channel controllability a high-k material is preferred, whereas a large conduction band offset is required to reduce the gate leakage current. In addition, a high temperature sustainability is much more important for a high power application. Since the phase change from amorphous to crystalline will rise to the leakage current, the crystalline temperature of HfO$_2$ (~400 °C) is much lower than Al$_2$O$_3$ (~900 °C) [27]. Previous reports also suggested that the HfO$_2$ suffers severely from the interface state and border state densities than Al$_2$O$_3$, which affects the device performances significantly [26,28]. Thus, by incorporation of Al into HfO$_2$ the thermal stability of the ternary compound, i.e., HfAlO$_x$ could be improved significantly.

The crystallization temperature of HfAlO$_x$ could give rise to ~1000 °C with 45.5% of Al [26]. The conduction band offset of HfAlO$_x$ is also much higher (~1.61 eV) [27], with a high dielectric constant ($k$~14) [29]. Moreover, due to the incorporation of Al, the interface state density is effectively reduced with the passivation of the dangling bond in HfAlO$_x$, which helps the improvement in the device performance significantly [30]. To date, the direct observation of the enhancement of device performance in HfAlO$_x$-based MOS-HEMTs with N$_2$ surface plasma modulation using the $\Gamma$- shaped gate structure, has not yet been investigated.

With this aim in mind, in this work, we have demonstrated the improvement of device performance in $\Gamma$-gate AlGaN/AlN/GaN MOS-HEMT with the Al doped HfO$_2$ gate dielectric and N$_2$ surface plasma modulation. The inclusion of Al into HfO$_2$ increased the crystalline temperature of HfAlO$_x$, which reduced the gate leakage current at a high PDA temperature (~600 °C). The interface state density of HfAlO$_x$ MOS-HEMT is reduced nearly one order of magnitude, which improved the hysteresis behaviour of the device. Moreover, the use of gate field plate (FP) increased the breakdown voltage ($V_{BR}$) of the device. The N$_2$ plasma treated $\Gamma$-shaped gate HfAlO$_x$-based MOS-HEMT exhibited a decent performance with $I_{PMAX}$ of 870 mA/mm, $G_{MMMAX}$ of 118 mS/mm, threshold voltage ($V_{TH}$) of ~3.55 V, higher $I_{ON}/I_{OFF}$ ratio of approximately $1.8 \times 10^9$, subthreshold slope (SS) of 90 mV/dec, and a $V_{BR}$ of 195 V with the reduced gate leakage current of $1.3 \times 10^{-10}$ A/mm.
2. Materials and Methods

The AlGaN/AlN/GaN-epitaxy was grown on a 6-inch low resistive (111) Si substrate by the metal organic chemical vapour deposition (MOCVD) system. The epitaxial layer consists of a 5.5 µm GaN buffer layer, a 200 nm GaN channel layer, a 1 nm AlN layer and a 25 nm Al$_{0.23}$Ga$_{0.77}$N barrier layer, and a 2 nm GaN cap layer. The measured Hall mobility, sheet carrier concentration, and sheet resistance were found to be 1800 cm$^2$/V·s, $8 \times 10^{12}$ cm$^{-2}$, and 434 Ω/□, respectively.

To achieve the device isolation the mesa etching was employed by using the inductive coupled plasma reactive ion etching (ICP-RIE) system under the Cl$_2$/BCl$_3$ environment. After that, the source and drain regions were defined using UV-photolithography, followed by Ti/Al/Ni/Au (25/150/30/120 nm) metal stacks were deposited by the electron beam (e-beam) evaporation system. Then, the rapid thermal annealing (RTA) took place at 875 °C for 45 s in N$_2$ ambient to ensure the good ohmic contact. After that, the gate recess area was defined by the ELS-7500 EX electron beam lithography (EBL) system. Subsequently, the GaN and AlGaN layers under the gate were partially recessed while using low power ICP-RIE. After that, the N$_2$ plasma treatment was done by RF-sputter and the sample was transferred to the atomic layer deposition (ALD) chamber (Picosun) to deposit the gate dielectric. The 10 nm thick hafnium aluminate (HfAlO$_X$) was deposited as the gate dielectric by ALD at 250 °C. As for the 10 nm HfAlO$_X$ deposition, three cycles of Al$_2$O$_3$ were first deposited, then four cycles of HfO$_2$, and one cycle of Al$_2$O$_3$ were cyclically deposited until the total thickness of 10 nm. Then, the sample was coated with an electron resist and baked at 180 °C for 7.5 min. After that, the Γ-shaped gate region was defined by the e-beam lithography system. Finally, the Ni/Au (80/100 nm) gate metal stack was deposited by the e-gun evaporator. In addition, (i) the Γ-shaped gate MOS-HEMT with the HfO$_2$ gate dielectric, (ii) Γ-shaped gate HEMT, and (iii) non-recessed HEMT (C-HEMT) were also fabricated following the same process as the control samples. In addition, to examine the high temperature sustainability of HfAlO$_X$, the MOS-HEMTs were fabricated with three different post deposition annealing (PDA) temperatures, i.e., 300, 600, and 800 °C for 1 min, and compared with HfO$_2$ MOS-HEMT. The schematic of the AlGaN/AlN/GaN Γ-shaped gate MOS-HEMT is shown in Figure 1a. All the devices were fabricated with the same gate length ($L_G = 0.5$ µm) and $L_{GD}/L_{SD}$ (2/2 µm).
3. Results and Discussion

Figure 1a–i shows the typical transmission electron microscope (TEM, JEM-2010 Electron Microscope; JEOL Co. 200 KV) images of the HfO₂- and HfAlOₓ-based MOS-HEMT. Without the intermixing of layers, a quite smooth oxide/GaN interface was observed. In order to compare the thermal stability of HfO₂ and HfAlOₓ, the PDA was done at 300 °C and 600 °C for 1 min and the characteristics were analyzed. Figure 1b,c shows the TEM images of the Γ-gate HfO₂ and HfAlOₓ MOS-HEMTs with the PDA at 300 °C. It was noticed that the gate dielectrics were in amorphous stage, i.e., no crystalline lattice fringes were found after the PDA at 300 °C. From Figure 1d, it can be observed that the amorphous phase of HfO₂ was changed to polycrystalline with the increasing annealing temperature from 300 to 600 °C. In addition, the selected area diffraction pattern (SADP) was used to analyze the details of the crystal diffraction by TEM, as shown in Figure 1e. Some diffraction peaks were found in the 600 °C annealed HfO₂ MOS-HEMT. As the AlGaN is a single crystal, thus, the diffraction ring is about the HfO₂ crystallization.

On the other hand, from Figure 1f,g it can be clearly understood that the HfAlOₓ was still in the amorphous stage at 600 °C. No diffraction peak was found in the SADP image, which further proved the aforementioned statement. In order to further analyze the thermal stability of HfAlOₓ, the material was annealed at 800 °C for 1 min. The TEM and SADF images proved that HfAlOₓ was still amorphous, as shown in Figure 1h,i.
results revealed that the crystallization temperature of HfO$_2$ was improved to a great extent by the incorporation of Al. Figure 1j shows the energy-dispersive X-ray spectroscopy (EDX) measurement with a line scan mode of HfAlO$_X$ film. It can be observed that the Hf and Al atoms are distributed uniformly. The ratio between Al and Hf in HfAlO$_X$ is about 1:2.

Figure 2a,b shows the gate leakage ($I_G$) characteristics of HfO$_2$- and HfAlO$_X$-based MOS-HEMTs with different PDA temperatures. The gate leakage current of HfO$_2$ MOS-HEMT was increased approximately two orders of magnitude with the increasing annealing temperature to 600 °C, as shown in Figure 2a. As the TEM images confirmed that the HfO$_2$ phase changes from amorphous to polycrystalline with the increasing PDA temperature, thus the additional high leakage path along the grain boundaries through the poly crystalline dielectrics increased $I_G$ with the PDA temperature [26]. The $I_G$ values ($@V_G = -12$ V) were found to be approximately $10^{-7}$ and $10^{-8}$ A/mm ($10^{-9}$ A/mm) orders of magnitude for $\Gamma$-gate HfO$_2$ MOS-HEMTs with 600 and 300 °C PDA (w/o PDA). From Figure 2b, it can be observed that the $I_G$ values were decreased about two orders of magnitude with the increasing annealing temperature from 300 to 600 °C in HfAlO$_X$ MOS-HEMTs. The decreased trap density with the increasing annealing temperature might be one possible reason for the reduction in the leakage current [26]. The $I_G$ ($@V_G = -12$ V) was increased from $10^{-9}$ to $10^{-8}$ mA/mm, when the temperature raised from room temperature (RT) to 300 °C, and then the gate leakage was reduced approximately to $10^{-10}$ mA/mm, with further increments of the PDA temperature to 600 °C. At a higher temperature, the growth of SiO$_2$ at the interface resulted in the reduction in $I_G$ [26].

![Figure 2. Comparison of gate leakage characteristics of (a) $\Gamma$-gate HfO$_2$ MOS-HEMT and (b) $\Gamma$-gate HfAlO$_X$ MOS-HEMT with the PDA at 300 and 600 °C and without the PDA.](image)

In order to analyze the effects of nitrogen (N$_2$) plasma treatment after ICP etching, on the gate leakage current, the $I_G$–$V_G$ characteristics were calibrated from $\Gamma$-gate HEMT and HfAlO$_X$ MOS-HEMTs with and without the N$_2$ plasma treatment, as shown in Figure 3a,b. It can be clearly observed that the gate leakage current was reduced more than one order of magnitude in $\Gamma$-gate HfAlO$_X$ MOS-HEMTs, whereas the $I_G$ was reduced approximately two orders of magnitude in the $\Gamma$-gate partially recessed HEMT by the N$_2$ plasma treatment. The N$_2$ vacancies, created by ICP dry etching, could be filled by the nitrogen radicals generated from the pure N$_2$ plasma. In addition, reducing the dangling bonds by forming Ga-N bonds resulted in activating the surface, which correspondingly reduced the gate leakage current [31].

The typical drain current-voltage characteristics of the $\Gamma$-gate HEMT- $\tau$, HfO$_2$-, HfAlO$_X$- based MOS-HEMT, and non-recessed HEMT is shown in Figure 4. The maximum drain currents ($I_{\text{D MAX}}$) of the HfAlO$_X$ ($@V_G = 5$ V) and HfO$_2$ ($@V_G = 4$ V) based MOS-HEMTs were found to be 870 and 775 mA/mm, respectively. Whereas, $I_{\text{D MAX}}$ values ($@V_G = 1$ V) were found to be 570 and 520 mA/mm for the recessed and non-recessed HEMT, respectively, which is comparatively much lower than $\Gamma$-gate MOS-HEMT. Owing to the large gate leakage current, the HEMTs were not biased with the high gate voltage [32]. Hence-
forth, due to the insertion of the gate dielectrics the gate leakage current can be effectively suppressed, which resulted in the improvement of the \(I_{\text{DMAX}}\) in the MOS-HEMT.

**Figure 3.** Comparison of gate leakage characteristics of (a) \(\Gamma\)-gate HEMT and (b) \(\Gamma\)-gate HfAlO\(_X\) MOS-HEMT with and without the N\(_2\) surface plasma treatment.

**Figure 4.** Comparison of drain current-voltage (\(I_D-V_D\)) characteristics of (a) \(\Gamma\)-gate HEMT (with the N\(_2\) plasma treatment) and non-recessed HEMT (w/o the N\(_2\) plasma treatment) and (b) \(\Gamma\)-gate HfO\(_2\) and HfAlO\(_X\) MOS-HEMT with the N\(_2\) plasma treatment.

To understand the gate controllability of the N\(_2\)-plasma treated \(\Gamma\)-gate HEMT-, HfO\(_2\)-, and HfAlO\(_X\)-based MOS-HEMT and C-HEMT, the transfer characteristics were calibrated at \(V_D = 4\) V, as shown in Figure 5. The threshold voltage \((V_{\text{TH}})\) is defined as the gate bias intercept point of the linear extrapolation of \(I_D\) at peak transconductance \((G_{\text{MMAX}})\) [33]. The threshold voltages were found to be \(-3.55\), \(-3.41\), and \(-3.55\) V for \(\Gamma\)-gate HEMT-, HfO\(_2\)-, and HfAlO\(_X\)-based MOS-HEMT, respectively. In comparison, the \(V_{\text{TH}}\) of the non-recessed HEMT was found to be \(-4.9\) V. The partially gate recessed and the use of field plate structure resulted in the positive shifting of \(V_{\text{TH}}\) in \(\Gamma\)-gate HEMT and MOS-HEMTs. The maximum transconductances were found to be 139, 116, and 118 mS/mm for the partially recessed HEMT-, HfO\(_2\)-, and HfAlO\(_X\)-based MOS-HEMT, respectively. The insertion of the gate dielectric layer, increased the distance between the gate and 2DEG channel. Therefore, the controllability of the gate is decreased which resulted in the reduction of the transconductance. The \(G_{\text{MMAX}}\) was found to be 114 mS/mm for the non-recessed HEMT.

**Figure 6a** shows the subthreshold characteristics as a function of the gate voltage (@ \(V_D = 4\) V) for \(\Gamma\)-gate HEMT-, HfO\(_2\)-, and HfAlO\(_X\)-based MOS-HEMT with the N\(_2\)-plasma treatment, and non-recessed HEMT. From Figure 6a, it is clearly observed that the subthreshold drain leakage current was decreased more than two orders of magnitude in the HfAlO\(_X\)-based MOS-HEMT, than the \(\Gamma\)-shaped gate HEMT. The HfAlO\(_X\) gate dielectric
improved the metal/semiconductor junction which subsequently reduced the drain leakage current. The subthreshold drain leakage current is dominated by the reverse biased gate leakage current ($I_G$) in the off-state [34]. Thus, the reduction of the reverse biased gate leakage current in the MOS-HEMT, resulted in the decrement of the subthreshold drain leakage current, as shown in Figure 6a.

Figure 5. Comparison of transfer characteristics ($I_D-V_G$) (@ $V_D = 4$ V) of (a) Γ-gate HEMT (with the N$_2$ plasma treatment) and non-recessed HEMT (w/o the N$_2$ plasma treatment) and (b) Γ-gate HfO$_2$ and HfAlO$_X$ MOS-HEMT with the N$_2$ plasma treatment.

Figure 6. Comparison of (a) subthreshold (@ $V_D = 4$ V) and gate leakage ($I_G-V_G$) characteristics of Γ-gate HEMT and Γ-gate HfO$_2$ and HfAlO$_X$ MOS-HEMT with the N$_2$ plasma treatment and non-recessed HEMT (w/o the N$_2$ plasma treatment). (b) Hysteresis characteristics of (@$V_D = 4$ V) Γ-gate HfO$_2$ and HfAlO$_X$ MOS-HEMT with the N$_2$ plasma treatment.

The subthreshold swing (SS) also depends on the $I_G$. To understand the gate controllability, the SS values were extracted for different devices from Figure 6a. The SS values were found to be 101, 86, and 90 mV/dec for the N$_2$-plasma treated partially recessed HEMT-, HfO$_2$-, and HfAlO$_X$-based MOS-HEMT, respectively. The current ON/OFF ratio ($I_{ON}/I_{OFF}$) of the aforementioned devices were found to be $2.9 \times 10^6$, $2.3 \times 10^8$, and $1.8 \times 10^9$, respectively. The SS and $I_{ON}/I_{OFF}$ were found to be 110 mV/dec and 1.04 $\times 10^6$, respectively for the non-recessed HEMT.

The reduction of the off-state gate leakage current is important in GaN HEMTs for their application in the electrical circuit. In general, it is also important to achieve a low flicker noise and low power consumption. The reversed and forward gate leakage I-V characteristics of the N$_2$-plasma treated Γ-gate HEMT-, HfO$_2$-, and HfAlO$_X$-based MOS-HEMT, respectively. The current ON/OFF ratio ($I_{ON}/I_{OFF}$) of the aforementioned devices were found to be $2.9 \times 10^6$, $2.3 \times 10^8$, and $1.8 \times 10^9$, respectively. The SS and $I_{ON}/I_{OFF}$ were found to be 110 mV/dec and 1.04 $\times 10^6$, respectively for the non-recessed HEMT.

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1.5 \times 10^{-7}, 1.7 \times 10^{-9}, and, 1.3 \times 10^{-10} \text{ A/mm} for the N_2-plasma treated \Gamma-gate HEMT-, HfO_2-, HfAlO_X-based MOS-HEMT. In particular, the HfAlO_X-based device exhibited the lowest \text{I}_G among all the devices. Due to the inclusion of Al in HfO_2, the band gap increased from \sim 5.8 \text{ eV} to greater than 6.5 \text{ eV} for HfAlO_X with \sim 50\% of Al, which is consistent with the large band gap of Al_2O_3 (\sim 8.1 \text{ eV}) [26]. The greater band offset of the HfAlO_X than HfO_2, effectively reduced the tunneling current which results in the reduction of the gate leakage current [26]. It can also be noted that the forward leakage current (@ V_G = 5 \text{ V}) also reduced more than three orders of magnitude in the HfAlO_X-based MOS-HEMT than the other devices, due to the large band offset. In comparison with the other devices, for C-HEMT without FP and the N_2 surface treatment, the \text{I}_G was found to be approximately (@ V_G = -12 \text{ V}) 3.7 \times 10^{-7} \text{ A/mm}.

To understand the hysteresis behavior of the gate dielectrics, the double sweep sub-threshold transfer characteristics of \Gamma-gate HfO_2 and HfAlO_X MOS-HEMT were measured, as shown in Figure 6b. It is clearly seen that the HfAlO_X-based MOS-HEMT (\sim 150 \text{ mV}) exhibited a much smaller hysteresis than the HfO_2-based devices (\sim 484 \text{ mV}). With the inclusion of Al into HfO_2 the interface state density was reduced due to the effective passivation of the dangling bonds in HfAlO_X than HfO_2 [30]. The incorporation of Al into HfO_2 also reduced the border traps which resulted in the reduction of hysteresis in HfAlO_X [26].

The off-state breakdown characteristics of different devices is shown in Figure 7. The breakdown voltages were found to be 107, 145, and 195 \text{ V} for the \Gamma-gate HEMT-, HfO_2-, and HfAlO_X-based MOS-HEMT, respectively. The defect states caused by ICP dry etching increased the gate leakage, resulting in the significant reduction of the breakdown voltage (V_{BR}) in the \Gamma-gate HEMT. As discussed earlier, due to the inclusion of Al into HfO_2 the \Gamma-gate/HfAlO_X interface was improved with a greater dangling bond passivation with the increased band gap and reduced \text{I}_G, which resulted in a much higher V_{BR} in the HfAlO_X-based MOS-HEMT compared to the HfO_2-based device.

![Figure 7](image-url)

**Figure 7.** Comparison of breakdown voltage characteristics of \Gamma-gate HEMT, HfO_2, and HfAlO_X MOS-HEMT with the N_2 plasma treatment.

The current collapse is an important issue for the electrical performance of AlGaN/GaN HEMTs, due to the electron trapping at the AlGaN surface states between the gate and the drain the current collapse occurred [31]. To investigate the effectiveness of the HfAlO_X gate dielectric with the field plate structure on the current degradation, the gate lag measurements were employed. Figure 8a–c shows the drain current response of the \Gamma-gate HEMT-, HfO_2-, and HfAlO_X-based MOS-HEMT with the field plate structure. The pulse width is 500 \mu\text{s} and the pulse period is 50 \text{ ms}. From the observations, it was clearly revealed that the current collapse phenomenon was effectively suppressed with the gate dielectric in the partially recessed MOS-HEMT. The drain-source current collapse was improved in the HfAlO_X-based MOS-HEMT to 4\% (@\text{V}_D = 8 \text{ V}, \text{V}_G = 0 \text{ V}), while for the HfO_2-based MOS-HEMT and partially-recessed HEMT it was found to be approximately 13\% and 18\%, respectively.
respectively. Most of the surface states presented at the source-drain access regions might have been passivated with the combined effects of the N₂ plasma treatment and HfAlOₓ surface passivation with the application of the gate field plate.

![Figure 8. Comparison of pulsed \(I_D-V_D\) characteristics of (a) \(\Gamma\)-shaped gate HEMT, (b) HfO₂, and (c) HfAlOₓ MOS-HEMT with the N₂ plasma treatment.](image)

In order to understand the reduction of trap states of \(\Gamma\)-gate HfO₂ and HfAlOₓ-based MOS-HEMTs, the capacitance-voltage (C-V) measurements were done for the devices at different frequencies, as shown in Figure 9a. The interface state densities (\(D_{it}\)) were extracted from the previously reported formula [35] to be \(1.8 \times 10^{12}\) and \(7.1 \times 10^{12}\) eV⁻¹·cm⁻² for the HfAlOₓ- and HfO₂-based MOS-HEMTs, respectively. In addition, the interface quality between the gate dielectric and the GaN layer could also be evaluated from the frequency dependent C-V measurement shown in Figure 9a. The interval of the C-V curve improved to 60 mV from 130 mV for the HfAlOₓ device, indicating the excellent interface quality between the gate dielectric and GaN layer [36,37].

![Figure 9. Comparison of (a) C-V characteristics of \(\Gamma\)-gate HfO₂ and HfAlOₓ MOS-HEMT at different frequencies and (b) flicker noise characteristics of \(\Gamma\)-gate HEMT, HfO₂, and HfAlOₓ MOS-HEMT with the N₂ plasma treatment.](image)

Low-frequency noise measurements are an effective method for studying the electron trapping and de-trapping behaviour. Figure 9b shows the low-frequency noise characteristics, measured at \(V_{DS} = 2.9\) V and \(V_{GS} = -3.9\) V, with frequencies ranging from 10 to 100 kHz, for the \(\Gamma\)-gate HEMT\_\(\Gamma\), HfO₂\_\(\Gamma\), and HfAlOₓ-based MOS-HEMT. In the noise characteristics, the variation of noise current density \(S_{ID}(\text{A}^2/\text{Hz})\) with the frequency was measured. The \(1/f\)-noise characteristics are directly related to the presence of the electron trap and de-trapping between the 2DEG channels and the traps presented in the GaN buffer layer [38]. It was observed that \(S_{ID}\) of the \(\Gamma\)-gate MOS-HEMT was more than one order lower than the partially recessed HEMT. The gate dielectrics significantly reduced the gate leakage currents and passivated the S/D access region, which subsequently improved the interface quality, as discussed earlier. Consequently, the insertion of gate dielectric layer can suppress the flicker noise. In particular, due to the better interface quality with the
lower interface density, the noise current density was found one order lower in HfAlOx-based MOS-HEMT (~10^{-12} A^2/Hz) than the HfO2-based device (10^{-10} A^2/Hz) at a low frequency. Table 1 shows the comparison of the N2 plasma treated HfAlOx MOS-HEMT and non-recessed HEMT. Table 2 shows the comparison of electrical performances of HfAlOx-based MOS-HEMT with different Al2O3 and HfO2-based MOS-HEMTs. The performance is comparable with the previous reports.

Table 1. Comparison of N2 plasma treated HfAlOx-based MOS-HEMT and C-HEMT w/o the N2 plasma treatment.

| Parameters | Non-Recessed HEMT | Partially-Recessed HEMT | Partially-Recessed MOS-HEMT | Partially-Recessed HfAlOx MOS-HEMT |
|------------|--------------------|-------------------------|-----------------------------|----------------------------------|
| I_DMAX (mA/mm) | 520 (V_G = 1 V) | 570 (V_G = 1 V) | 775 (V_G = 4 V) | 870 (V_G = 5 V) |
| V_TH (V) | -4.9 | -3.55 | -3.41 | -3.55 |
| G_MAX (mS/mm) @ V_D = 4 V | 114 | 139 | 116 | 118 |
| SS (mV/dec) | 110 | 101 | 86 | 90 |
| I_C (A/mm) @V_G =-12 V | 3.7 x 10^{-7} | 1.5 x 10^{-7} | 1.7 x 10^{-9} | 1.3 x 10^{-10} |
| Current collapse (%) | - | 13 | 13 | 4 |
| D_th (eV^{-1}·cm^{-2}) | - | 2.1 x 10^{13} | 7.1 x 10^{12} | 1.8 x 10^{12} |
| Hysteresis (ΔV) (V) | - | 0.48 | 0.15 | |
| V_BR (V) | - | 107 | 145 | 195 |

Table 2. Comparison of Electrical performances of HfAlOx-based MOS-HEMT with Al2O3 and HfO2 MOS-HEMT.

| Parameters | Ref. [21] | Ref. [23] | Ref. [39] | Ref. [40] | Ref. [41] | This Work |
|------------|-----------|-----------|-----------|-----------|-----------|-----------|
| Epi structure | GaN/AlGaN/GaN | GaN/AlGaN/AlN/AlGaN | AlInN/AlN/GaN | GaN/AlGaN/GaN | GaN/AlGaN/GaN | GaN/AlGaN/GaN |
| L_G (μm) | 1 | 5 | 0.2 | 50 | 1.5 | 0.5 |
| Dielectric materials | HfO2/Y2O3 | HfZrO2 | Al2O3 | Al2O3 | Al2O3 | HfAlOx |
| Dielectric Thickness (nm) | 12/1 | 20 | 5 | 50 | 20 | 10 |
| G_MAX (mS/mm) @V_D = 0.05 V | 600 | 705 | 1150 | -160 | 300 | 870 |
| SS (mV/dec) | 70 | 85 | - | - | 74 | 90 |
| I_C (A/mm) @V_G =-9 V | 10^{-10} | 10^{-7} | A/mm | 10^{-4} A/mm | 10^{-3} A/mm | 10^{-11} A/mm |
| Current collapse (%) | - | <9% | - | - | - | - |
| D_th (cm^{-2}·eV^{-1}) | 10^{12} | 1.1 x 10^{9} | - | - | - | 1.8 x 10^{12} |

4. Conclusions

In summary, we have demonstrated the comparative study of N2 plasma treated HfAlOx-based MOS-HEMT with HfO2 and HfAlOx as gate dielectrics. The off-state gate leakage current was significantly reduced with the increasing PDA treatment from 300 to 600 °C in the HfAlOx-based MOS-HEMT compared to the HfO2-based devices. Due to the inclusion of Al into HfO2, the crystallization temperature was significantly improved to ~1000 °C of HfAlOx. Moreover, due to the higher conduction band offset of HfAlOx to GaN (~1.61 eV), the gate leakage current was effectively reduced in HfAlOx MOS-HEMT even at the higher temperature. The interface state density of HfAlOx MOS-HEMT was effectively reduced compared to the HfO2 device, due to the effective passivation of the dangling bonds, which subsequently improved the hysteresis and current collapse characteristics. Due to the reduction of N2 vacancies, created by ICP dry etching, the gate leakage current was reduced more than one order of magnitude by the N2 surface plasma treatment. The D_th values were improved to 1.8 x 10^{12} eV^{-1}·cm^{-2} from 7.1 x 10^{12} eV^{-1}·cm^{-2} for HfAlOx MOS-HEMT than HfO2 MOS-HEMT. The N2 plasma treated HfAlOx-based MOS-HEMT exhibited a decent performance with I_DMAX of 870 mA/mm, G_MAX of 118 mS/mm, threshold voltage (V_TH) of ~3.55 V, higher I_ON/I_OFF ratio of approximately 1.8 x 10^{9}, subthreshold slope (SS) of 90 mV/dec, a V_BR of 195 V with reduced current collapse of 4%, and gate leakage current of 1.3 x 10^{-10} A/mm.
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