A series-connected asymmetrical PWM half-bridge three-level converter with reduced circulating current

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Abstract A novel three-level (TL) converter topology is proposed in this paper. The primary side of the proposed converter consists of two asymmetric half-bridge inverters, which are connected in series. The rectifier stage is composed of two parallel full-bridge rectifiers (FBR) which use the same diodes as the common current path. The asymmetrical-PWM control is employed to regulate output voltage. Compared with the traditional TL converters, the circulating current can be significantly reduced. Moreover, all the switches can achieve ZVS performance with a small leakage inductor over wide load range. The parallel connection of the two FBR also helps to reduce the current ripple of the filter inductor, leading to high efficiency over wide load range, reduced circulating current and low filter requirement. The parallel connection of the two FBR also helps to reduce the current ripple of the filter inductor, leading to high efficiency over wide load range, reduced circulating current and low filter requirement.

Keywords: three level, zero-voltage-switching, circulating current, reduced filter size

1. Introduction

The traditional three-level (TL) converter is designed to achieve the feature of high input voltage and high efficiency with zero voltage switching (ZVS) operation, which makes it well suited for medium-to-high-power applications. The traditional TL converter is shown in Fig. 1. The voltage stresses of the switches in the primary side are clamped to the half of input voltage [1, 2, 3, 4, 5]. However, there are also some drawbacks in the traditional TL converter. First, the primary circulating current causes significant conduction loss at heavy loads, which greatly reduces the efficiency of the converter. Moreover, the ZVS condition of lagging-leg switches is hard to achieve at light loads. The ringing of the secondary voltage needs extra clamping diodes in the primary side, which increases the volume of the converter.

To overcome the aforementioned drawbacks of the traditional TL converter, many studies have been conducted. For the traditional TL converter, the ZVS of lagging-leg is determined by the energy stored in the leakage inductor of the transformer. In order to extend the ZVS range of traditional TL converter, a resonant inductor and two clamping diodes are added to the converter’s primary side [6]. The resonant inductor can provide more energy for the lagging-leg to achieve ZVS condition at light loads. However, large inductor in the primary side can also cause more duty-cycle loss and a high voltage spike across the rectifier which needs clamping diodes to eliminate. To improve the ZVS conditions of the lagging-leg, the TL converters with exchanging the position of the resonant inductance and the transformer is proposed in [7, 8]. However, the circulating current in the primary side is increased. A series of new TL converters with auxiliary circuits is proposed to extend the ZVS range of TL converter [9, 10, 11]. Although these converters can achieve ZVS operation at light loads, extra components also bring more conduction loss and are not suitable for high density design. Some DC/DC converters extend the ZVS range by connecting two half bridge cells in the primary side [12, 13, 14]. The two half bridges are connected in series to form the TL circuit without any extra auxiliary circuits.

The load-dependent circulating current is one of the major reasons for the conduction loss in TL converter. The circulating current passes through the converter’s power train during the non-duty cycle period while no energy is transmitted to the output. The TL converters with zero-Voltage and Zero-Current-Switching (ZVZCS) operation is a good way to reduce the circulating current. Some DC/DC converters eliminate circulating current by adding auxiliary circuits to the primary side. The auxiliary circuits absorb the energy stored in the leakage inductance during the freewheeling period, which can make the current decay to zero in the primary side [15, 16, 17, 18]. The TL converters in [19, 20, 21, 22, 23, 24] adds clamping circuits and coupling inductor in the secondary side to eliminate circulating current.

However, the auxiliary circuits also increase the voltage rating of rectifier diodes. In these converters, the leading-leg switches adopt MOSFETs, and IGBT is used as the lagging-leg switches. Although ZCS technique can significantly reduce the tail current of the IGBTs, the maximum switching frequency of the IGBTs limits the magnetic components and space-constrained design. The converters in [24, 25, 26, 27, 28, 29, 30] use two half bridges to form the TL structure. Although it can eliminate the circulating current, in the primary side auxiliary circuit is also added to limit the ringing of the rectifiers.

In this paper, a novel TL DC/DC converter with wide ZVS range, reduced circulating current and low filter requirement is proposed. Fig. 2 shows the circuit diagram of proposed converter. As shown in Fig. 2, the proposed converter is composed of two asymmetric half-bridge (AHB) inverters...
AHB-1 and AHB-2 in series. The phase shift angle of AHB-1 and AHB-2 is 180°, and the converter changes the duty-cycle of upper switch in the AHB to regulate its output voltage. At the rectifier stage, two full-bridge-rectifier (FBR) are placed in parallel to provide low current ripple. Because two FBR use the common current path, there are only five diodes used to compose the rectifier stage. The circulating current in the primary side is reduced by the asymmetrical-PWM control and all switches can achieve ZVS conditions at light loads without any extra auxiliary circuits. Moreover, the rectifier stage can reduce the current ripple of output filter inductor. The transformers in the proposed converter share the output power equally, and there are only five diodes in the secondary part. Therefore, the transformers in the proposed converter are easy to design, and high density can be achieved.

The performance of the proposed converter is verified by an experimental prototype with 480-600 Vdc input, 96Vdc/12A output. Experimental results show that the proposed converter can achieve higher conversion efficiency than the traditional TL converter.

2. Operational principle

Fig. 3 shows the key current and voltage operating waveforms of the proposed converter in the steady state. The proposed converter is composed of two AHB converters in series. The duty cycle of Q1 is complementary to that of Q3 and the phase-shift of two AHB converters is 180°. The output voltage is regulated by adjusting the duty cycle of Q1 and Q3. In order to simplify the theoretical analysis, the following assumptions are made: (1) the magnetizing inductances of T1 and T2 are large enough and the ripple of the magnetizing inductor current is neglected. The magnetizing inductor current is considered as mean value; (2) the leakage inductances of T1 and T2 are same and equal to Lk; (3) the output filter inductors Lp is large enough to be considered as constant current source of Io; (4) the blocking capacitor is large enough to be considered as constant voltage source of 0.5DVin.

There are 18 states in one switching period, which can be divided into two half periods, t0~t9 and t9~t18. Due to the symmetry of the circuit structure, only the first half period is introduced in this paper. The operations in the other half period are the same as t0~t9 except for the direction of powering path. The corresponding operation circuits during t0~t9 are shown in Fig. 4.

Mode 1 [t0~t1]: The time t0 is the moment when D1 and D2 finish their commutation. During this mode, Q1, Q4, D1 and D3 are in the on-state. The power is transferred from the input to the output through Q1, T1, D1 and D3.

Mode 2 [t1~t2]: At time t1, Q1 is turned off. The junction capacitances of Q1 and Q3 are linearly charged and discharged by a constant current source of (nIo + ILM). The primary voltage of T1 Vp1(t) linearly drops off until it goes down to 0V at t2. Then, D2 starts to conduct, and the commutation between D1 and D2 starts.

Mode 3 [t2~t3]: At time t2, Vs1 goes down to zero and the secondary winding of T1 is short-circuited. The primary part of proposed converter gets into resonant state, and the primary winding current ip1 is decreased simultaneously. The energy stored in the leakage inductances Lk starts to charge and discharge the junction capacitances of Q1 and Q3. VAO continues to drop off and it falls down to zero at t3. Then, the resonant state is over. The key voltage and current are calculated as follows:

\[ i_{p1}(t) = (nI_o + I_{LM})\cos\sqrt{\frac{1}{2L_kC}}(t - t_2) \] (1)

\[ V_{AO}(t) = 0.5DV_{in} - \sqrt{\frac{L_k}{2C}}(nI_o + I_{LM})\sin\sqrt{\frac{1}{2L_kC}}(t - t_2) \] (2)
Mode 4 \([t_3 \sim t_5]\): At time \(t_3\), the resonance in the primary side of the proposed converter is completed. The drain-source voltage of \(Q_3\) reaches zero and \(i_{p1}\) flows through the body diode of \(Q_3\). Thus, \(Q_3\) can be turned on with ZVS after this moment. \(i_{p1}\) continually decreases due to the existence of \(0.5DV_{in}\) and it goes down to \(I_{Lm}\) at \(t_4\), the commutation between \(D_1\) and \(D_2\) is completed.

Mode 5 \([t_4 \sim t_5]\): During this mode, the primary current for \(T_1\) is remained at \(I_{Lm}\), and it is remained at \(-nI_o + I_{Lm}\) for \(T_2\).

Mode 6 \([t_5 \sim t_6]\): Mode 6 begins when \(Q_3\) is turned off at \(t_5\). The primary current for \(T_2\) starts to drop off and the commutation between \(D_1\) and \(D_2\) starts. During this mode, the resonance of \(L_4\), \(C_{oss2}\) and \(C_{oss1}\) occurs in the primary side and \(i_{p2}\) decreases with a sinusoidal waveform. \(V_{p2}\) goes down to zero at \(t_6\) and the commutation between \(D_2\) and \(D_3\) starts. \(V_B\) and \(i_{p2}\) in this mode are expressed as:

\[
V_B(t) = (nI_o + I_{Lm}) \sqrt{\frac{L_k}{C}} \sin \frac{1}{2L_kC} (t - t_5) \quad (3)
\]

\[
i_{p2}(t) = -(nI_o + I_{Lm}) \cos \frac{1}{2L_kC} (t - t_5) \quad (4)
\]

Mode 7 \([t_6 \sim t_7]\): The secondary winding of \(T_2\) is short-circuited during this mode. The energy stored in the leakage inductor \(L_k\) starts to charge and discharge the junction capacitances in the primary side. The midpoint voltage \(V_B\) continues to increase and it reaches to \(0.5DV_{in}\) at \(t_7\). Then, the resonance in the primary side of the converter is completed. The key voltage and current are calculated as follows:

\[
V_B(t) = i_{p2}(t_6) \sqrt{\frac{L_k}{2C}} \sin \frac{1}{2L_kC} (t - t_6) + DV_{in} \quad (5)
\]

\[
i_{p2}(t) = -\sqrt{\left(nI_o + I_{Lm}\right)^2 - \frac{L_k}{C_{oss}} - D^2} \cdot V_{in} \cos \frac{1}{2L_kC} (t - t_6) \quad (6)
\]

Mode 8 \([t_7 \sim t_8]\): At time \(t_7\), the midpoint voltage \(V_B\) reaches to \(0.5DV_{in}\), and then \(Q_2\) can be turned on with ZVS condition. \(i_{p2}\) continues to decrease and it drops to zero at \(t_8\), the commutation between \(D_4\) and \(D_5\) is completed.

Mode 9 \([t_8 \sim t_9]\): At time \(t_8\), \(i_{p2}\) is equal to zero and \(D_5\) is naturally turned off. During this mode, \(i_{p2}\) continues to decrease until it is equal to \(-i_{p1}\) at time \(t_9\). The commutation between \(D_2\) and \(D_3\) is completed. \(t_9\) is the end of one-half cycle of the whole switching period, and the operations in the other half cycle are the same as \(t_0 \sim t_9\) except for the direction of powering path.

3. Performance comparison

A. Voltage Conversion Ratio

The durations of ZVS transition can be ignored since they are very narrow. The simplified waveforms of rectifier output voltage can be shown as in Fig. 5.

The output voltage is equal to the average voltage of rectifier. In addition, the conversion ratio of the proposed converter and TL converter can be expressed as:

\[
G_{pro}(D) = V_o/nV_{in} = \left[3D - 2D^2\right] \quad (7)
\]

\[
G_{tr}(D) = V_o/nV_{in} = 0.5D \quad (8)
\]

Compared with the traditional TL converter, the rectifier voltage is nonzero and the proposed converter can transfer the power to the output in the whole switching period. Therefore, the current ripple can be greatly reduced. Fig. 6 shows the curves of conversion ratio of the above two topologies. As we can see in the Fig. 6, the conversion ratio of the proposed converter is higher than traditional TL converter.
Therefore, the proposed converter can have less turns of secondary winding, which is benefit to improve the efficiency especially for the applications with high output current and low output voltage.

B. ZVS Condition

Fig. 7 shows the simplified equivalent circuit of the ZVS process. For the proposed converter, two half-bridges are connected in series, and their ZVS conditions are the same. As described in the Section 2, the ZVS of upper switches (Q1 and Q2) is achieved in two phases. At first, the junction capacitance is charged by the energy in the output inductor and magnetic inductance. Then, the energy used to charge the junction capacitance is supplied by the leakage inductor $L_k$. Therefore, the constraints can be expressed as:

$$\frac{1}{2} L_k [(1.5 - D) n I_o] \geq C_{oss} D^2 V_{in}^2$$  (9)

The ZVS operation of lower switches (Q3 and Q4) is also achieved in two phases. In Mode 6, the current of AHB-2 is decreased with a sinusoidal waveform, actually $L_k$ also release energy to charge the junction capacitor at this period. And in the second phase, the energy used to junction capacitor are all supplied by $L_k$. Therefore, soft switching condition is that the energy in the leakage inductor must be greater than the energy needed to charge and discharge the junction capacitor. The constraints can be expressed as:

$$\frac{1}{2} L_k [(n I_o + I_{Lm})^2 - \frac{L_k}{C_{oss}} - 4 D^2 \cdot V_{in}^2] \geq C_{oss} \cdot (1 - 2D)^2 V_{in}^2$$  (10)

As seen in (10), the current of magnetizing inductor is benefit to realize the ZVS operation. Therefore, the assistent current of $L_m$ in can achieve ZVS operation over a wide load range.

C. Current ripple of the filter inductor

The current ripple of output filter inductor is calculated based on the rectified voltage. In the traditional TL converter, the rectifier voltage is zero during the freewheeling interval, and the power from the primary side cannot be transferred to the output side. The current ripple in the traditional TL converter is expressed as:

$$\Delta I = \frac{D \cdot n V_{in}}{f_s \cdot L_o} (2 - 0.5D)$$  (11)

However, for the proposed converter, the rectifier voltage is nonzero and the primary power can be transferred to the outside in the whole switching period. Thus, the current ripple can be greatly reduced. The current ripple in proposed converter is calculated as:

$$\Delta I = \frac{D \cdot n V_{in}}{f_s \cdot L_o} (1 - 3D + 2D^2)$$  (12)

Fig. 8 shows the current ripple of the output filter inductor in function of duty-cycle at $L_o = 120 \mu H$. It can be noted from Fig. 8 that the current ripple of the proposed converter is much smaller than that of traditional TL converter.

4. Experimental results

An experimental prototype was built to verify the operational principle, advantages and performances of the proposed converter. The specifications of the experimental prototype are shown in Table I.

Fig. 9 shows the gate signal, primary voltage and primary current of AHB-1 and AHB-2 at $V_{in} = 600 \text{V}$ and $I_o = 12 \text{A}$. As shown in Fig. 8(a) and Fig. 8(b), it is obvious that the working state of AHB-1 and AHB-2 is consistent. And the circulating current during the freewheeling period is greatly reduced. Fig. 10 shows the waveforms of proposed converter with maximum and minimum $V_{in}$. Because the small leakage inductor of proposed converter, the duty-cycle loss is reduced. The experimental waveforms of the prototype coincide well with the theory waveforms in Fig. 3.

Fig. 11 shows the ZVS condition of the proposed converter under different load conditions. The experimental
waveforms confirm that the primary switches are operated with soft-switching characteristic under a wide range of load conditions. Fig.12 shows the experimental efficiency of the traditional TL converter and proposed converter at $V_{in}=600V$. The curves show that the proposed converter obtains higher conversion efficiency than the traditional TL converter since its wide ZVS range and reduced circulating current.

5. Conclusion

This paper proposed a series-connected asymmetrical half-bridge TL converter. The rectifier stage uses only five diodes as full-bridge rectification due to the common current path in the secondary-side of the converter. In this paper, the analysis of converter is provided to show that the circulating current is greatly reduced, and all the switches can achieve ZVS conditions over a wide load range. The two transformers share the load power equally, therefore they are easy to design. The rectifier stage uses only five diodes but the conduction loss of the diodes is not increased. Moreover, the conduction loss in the primary side of proposed converter is lower than that of the traditional TL converter. Finally, the experiment prototype converter is built to demonstrate the performance of the proposed converter and the experimental waveforms well support the theoretical analysis.

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