Quantum Point Contact Transistor and Ballistic Field-Effect Transistors

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Abstract. We report the experimental results and theoretical understanding of the Quantum Point Contact Transistor - a fully ballistic one-dimensional (1D) Field-Effect Transistor (FET). Experimentally obtained voltage gain greater than 1 in our Quantum-Point-Contact transistors at 4.2 K can be explained with the help of an analytical modeling based on the Landauer-Büttiker approach in mesoscopic physics: the lowest 1D subband and the band gap play the key role in increasing its transconductance, especially by reducing its output conductance, and thus achieving a voltage gain higher than 1. This work provides a general basis for devising future ballistic FETs and the quantum limits found in this work may be used to estimate normalized transconductance and channel resistance in future two-dimensional (2D) ballistic FETs.

1. Introduction

It has long been a hope to devise a FET operating in the ballistic regime. Presently, thanks to remarkable theoretical and experimental progress in mesoscopic physics, ballistic Field-effect devices are routinely achievable [1]. Among them, the most investigated mesoscopic device is a nearly perfect 1D (one Dimensional) quantum ballistic conductor also called QPC (Quantum Point Contact), which is realized by split-gate constrictions on a high mobility 2DEG (Two-Dimensional Electron Gas) [2]. For turning such 1D device into real ballistic FETs as building blocks - switches - for digital integrated circuits, the key point is to obtain a voltage gain greater than 1.

Terminologically, a transistor is an electronic device having the ability to amplify electrical signals. Generally, there are three different gains, i.e., current, voltage or power gain. We will show that any field-effect device can have a current gain but not necessarily a voltage gain or a power gain. For a FET, important gains are the voltage gain and the power gain. This can easily be understood if we consider, for example, a large number of identical FET switches in a logic circuit: in that case, the required input (gate-source) voltage swing $\delta V_{gs}$ for setting a switch to two distinguishable states must be smaller than the deliverable output (drain-source) voltage $\delta V_{ds}$ of the preceding one. This is why $\delta V_{ds}/\delta V_{gs}>1$ is essential for the building blocks of any sequential information processing. And in addition, a power gain is necessary for ensuring the fan-out capability.

Suppose that the FET to be investigated is with an almost perfect gate, i.e., without DC leakage current, so the gate impedance has only an imaginary part with a value of $1/(2\pi f C_g)$ ($f$ is the operation frequency and $C_g$ is the input gate capacitance). The gate leakage current can be written as
\[ \delta I_{ds} = (2\pi f C_g) \delta V_{gs} \]  

The variation of the drain-source current \( I_{ds} \) can be expressed from the transconductance definition \( g_m = \frac{\delta I_{ds}}{\delta V_{gs}} \).

Current gain can be written as

\[
\frac{\delta I_{ds}}{\delta I_{gs}} = \frac{g_m \delta V_{gs}}{(2\pi f C_g) \delta V_{gs}} = \frac{g_m}{2\pi f C_g} .
\]

By defining the current cutoff frequency \( f_T = \frac{g_m}{2\pi C_g} \), we have

\[
\frac{\delta I_{ds}}{\delta I_{gs}} = \frac{f_T}{f}.
\]

When \( f < f_T \), we have \( \frac{\delta I_{ds}}{\delta I_{gs}} > 1 \).

The voltage gain can be expressed by

\[
\frac{\delta V_{ds}}{\delta V_{gs}} = \frac{\delta I_{ds}}{\delta I_{gs}} \frac{g_d}{g_m} = \frac{g_m}{g_d} \frac{\delta I_{ds}}{\delta I_{gs}} \frac{2\pi f C_g}{g_d},
\]

where \( g_d \) is the output conductance and is defined by \( g_d = \frac{\partial I_{ds}}{\partial V_{ds}} \).

We define the critical frequency \( f_C = \frac{g_d}{2\pi C_g} \), the voltage gain can then be expressed by

\[
\frac{\delta V_{ds}}{\delta V_{gs}} = \frac{\delta I_{ds}}{\delta I_{gs}} \frac{f}{f_C}.
\]

So in the condition of \( f < f_C \), a current gain \( > 1 \) cannot ensure a voltage gain \( > 1 \). Only in the frequency range \( f_C < f < f_T \), the current gain \( > 1 \) can guarantee the voltage gain \( > 1 \). If \( g_d \) and \( g_m \) values are close, this frequency range remains narrow.

Inversely, when \( f < f_C \),

\[
\frac{\delta I_{ds}}{\delta I_{gs}} = \frac{\delta V_{ds}}{\delta V_{gs}} \frac{f}{f_C}. 
\]

Thus a voltage gain \( > 1 \) can ensure a current gain \( > 1 \) except for the frequency range \( f_C < f < f_T \).

The power gain is defined by

\[
\frac{\delta V_{ds} \delta I_{ds}}{\delta V_{gs} \delta I_{gs}} = \left( \frac{\delta V_{ds}}{\delta V_{gs}} \right)^2 \frac{g_d}{2\pi f C_g} = \left( \frac{\delta I_{ds}}{\delta I_{gs}} \right)^2 \frac{f}{f_C},
\]

or

\[
\frac{\delta V_{ds} \delta I_{ds}}{\delta V_{gs} \delta I_{gs}} = \left( \frac{\delta I_{ds}}{\delta I_{gs}} \right)^2 \frac{2\pi f C_g}{g_d} = \left( \frac{\delta I_{ds}}{\delta I_{gs}} \right)^2 \frac{f}{f_C}. \]

When \( f < f_C \), a current gain cannot ensure a power gain while a voltage gain can.

So the most important gain for a FET is the voltage gain. The maximum (or intrinsic) voltage gain can be measured by using two main FET parameters, the transconductance \( g_m \) and the output conductance \( g_d \); in which case the gain reads \( g_m/g_d \). Therefore, to realize a ballistic FET becomes basically how to increase \( g_m \) and decrease \( g_d \).

2. Experimental results and analytical simulation

The 1D quantum ballistic conductor device illustrated in Figure 1a consists of source and drain ohmic contacts and a Schottky split-gate that forms a 1D channel in a high electron mobility 2DEG. Experimentally, the 2DEG is obtained in a modulation doped AlGaAs/GaAs heterojunction grown by molecular beam epitaxy. In order to have a high control efficiency of the split-gate and 1D subbands
with large energy separation, the AlGaAs/GaAs interface is placed close to the surface, 35 nm deep, and a narrow gap of about 45 nm for the split-gate is realized by electron beam lithography (see Figure 1b). The electron density and mobility of the used 2DEG are, respectively, $5.7 \times 10^{15} \text{ m}^{-2}$ and 93 m$^2$/Vs at 4.2 K. The corresponding electron mean free path of 11 µm guarantees that the transport is fully ballistic across the QPC.

![Figure 1.](image)

(a) Schematic illustration of the QPC device, which consists of a source “S”, a drain “D” and a split-gate “G”. In this work, the source is the reference voltage. The grey sheet represents the surface of the heterojunction and the yellow sheet indicates the 2DEG with a 1D channel constricted by the voltage biased split-gate. (b) Scanning electron microscope image of the QPC. The metallic split-gate (light grey) is deposited on the surface of the AlGaAs/GaAs heterojunction (dark grey).

We plot measured $I_{ds}-V_{gs}$ characteristics as a function of $V_{ds}$ at 4.2 K in Figure 2a. Step-like variations of $I_{ds}$ can be clearly found, and the corresponding $g_{m}-V_{gs}$ characteristics (symbols) are shown in Figure 3a, with $g_{m}$ peaks when $V_{gs}$ is biased at around $P1$ and $P2$. Measured $I_{ds}-V_{ds}$ characteristics as a function of $V_{gs}$ at 4.2 K are shown in Figure 2b, and the corresponding $g_{d}-V_{ds}$ characteristics (symbols) in Figure 3b, which clearly show that the needed $V_{ds}$ bias for reaching a non-linearity in the $I_{ds}-V_{ds}$ characteristics depends on $V_{gs}$. Under the bias condition of $V_{ds}<15$ mV, $V_{gs}$ must be less than about -60 mV.

![Figure 2.](image)

(a) Measured $I_{ds}-V_{gs}$ characteristics as a function of $V_{ds}$. (b) Measured $I_{ds}-V_{ds}$ characteristics as a function of $V_{gs}$. All measurements are performed at 4.2 K.

Straightforwardly, the voltage gain of our device can be deduced by the ratio of $g_{m}$ to $g_{d}$. Based on the results in Figures 3a and 3b, we plot in Figure 3c the map of the experimental voltage gain as a function of $V_{gs}$ and $V_{ds}$ with white and black contour lines indicating the voltage-gain value $g_{m}/g_{d}=1$ and 0.1, respectively. $g_{m}/g_{d}$ values from 1 to as high as 5 are found on the left of the white contour line. Between the white and black contour lines, $g_{m}/g_{d}$ varies from 1 to 0.1. For the rest of the area, $g_{m}/g_{d}$ remains below 0.1. It clearly appears that when $V_{gs}$ is biased around $P1$, the voltage gain is higher than 1 for appropriate $V_{ds}$. As an example, for the working point indicated with the red circle in Figures 2 and 3 under the fixed bias condition of $V_{gs}=-90$ mV, $V_{ds}=7$ mV and $I_{ds}=0.18$ µA, $g_{m}=20$ µS, $g_{d}=10$ µS and a voltage gain of 2 can be reached with a power consumption of only 1.3 nW.

In order to prove that our device operates in the ballistic regime, an analytical simulation has been performed based on the Landauer-Büttiker formalism in the ballistic regime [1]. The details of the
analytical modeling can be found in the reference [3]. Indeed, the complex characteristics (symbols) of $g_m-V_{gs}$ and $g_d-V_{ds}$ in Figure 3 can be nearly perfectly simulated (lines). The good agreement between the experimental and theoretical results confirms therefore that our device actually works in the ballistic regime.

Figure 3. (a) $g_m-V_{gs}$ characteristics based on measured $I_{ds}-V_{gs}$ (symbols) and by analytical simulation (lines). (b) $g_d-V_{ds}$ characteristics based on measured $I_{ds}-V_{ds}$ (symbols) and by analytical simulation (lines). (c) Voltage gain deduced from the experimental data as a function of $V_{gs}$ and $V_{ds}$. The right column indicates different colours in relation to $g_m/g_d$ values.

For a better understanding, the energy diagram of our device in the ballistic regime is illustrated in Figure 4a, which is represented by two 2DEG reservoirs of the source and the drain with the electrochemical potentials $\mu_s$ and $\mu_d$, respectively, and 1D subbands by the QPC with $E_n$, the energy of the bottom of the nth 1D subband. Here a simplified description is used, $\mu_s$ is kept as the reference voltage, $E_n$ can be modulated by $V_{gs}$ of the split-gate with a capacitance coupling and $\mu_d$ is directly controlled by $V_{ds}$ with $\mu_d = \mu_s - eV_{ds}$. Basic features of $g_m-V_{gs}$ and $g_d-V_{ds}$ in Figure 3 can be explained by relative positions of $\mu_s$, $E_n$ and $\mu_d$ as shown in Figures 4b and c.

Figure 4. (a) Schematic illustration of the energy diagrams of the QPC device in the ballistic regime. (b) Energy diagram illustrating $E_1$ set between $\mu_s$ and $\mu_d$. (c) Energy diagram illustrating $E_2$ set between $\mu_s$ and $\mu_d$.

For $g_m$, first (second) $g_m$ peaks in Figure 3a with $V_{gs}$ bias at $P1$ ($P2$) correspond to the band diagram in the Figure 4b (4c), i.e., $g_m$ peaks can be found when $E_n$ is set around middle between $\mu_s$ and $\mu_d$. Interestingly, the lowest 1D subband can produce the highest $g_m$ peaks under low drain bias of $V_{ds} < 15$ mV.

For $g_d$, low $g_d$ can be obtained (see the curve $C1$ in the Figure 3b) when $V_{gs}$ is set around $P1$ (corresponding to the band diagram Figure 4b). $g_d$ decreases with the increase of $V_{ds}$. This is due to the fact that when $\mu_d$ is below $E_1$ or $\mu_d$ enters into the band-gap, any increase of $V_{ds}$ cannot produce an additional electron injection, so $g_d$ decreases rapidly. The bias condition of $V_{gs}$ at around $P1$ is favorable for obtaining a voltage gain greater than 1. However, when $V_{gs}$ is set around $P2$, which corresponds to the energy diagram Figure 4c, $g_d$ of the curve $C2$ in the Figure 3b is large. With the decrease of $\mu_d$ (under low $V_{ds}$ condition of < 15 mV), additional electron injection is allowed for $\mu_d$ from $E_2$ down to just above $E_1$ (Figure 4c), and $g_d$ of the curve $C2$ (Figure 3b) remains almost constant. This bias condition of $V_{gs}$ around $P2$ leads to a $g_d$ that stays larger than $g_m$. 
Consequently, voltage gain can be obtained when \( V_{gs} \) is biased around \( P1 \), i.e., when the lowest 1D subband \( E_1 \) is set around \( \mu_s \). \( g_d \) can be reduced efficiently by lowering \( \mu_d \), since \( \mu_d \) enters into the band gap even with a small \( V_{ds} \). By contrast, when \( V_{gs} \) is set around \( P2 \) or \( E_2 \) is set around \( \mu_s \), under the same \( V_{ds} \) as for \( V_{gs} \) biased at \( P1 \), \( g_d \) is too high to obtain a voltage gain. Probably much high \( V_{ds} \) is needed to put \( \mu_d \) into the band gap and then to realize a voltage gain higher than 1.

3. Discussion and conclusion

In order to assess the QPC transistor performance, various electrical parameters can be expressed by the normalized ones with the actual channel width. For the working point as indicated by the red cycle in Figures 2 and 3 with \( V_{gs} \) set at \( P1 \), the corresponded channel width is equal to or less than half Fermi wavelength \( \lambda_F/2 \) according to the wave guide concept for the 1D ballistic conductor [2]. By using the 2DEG density \( n \) in this work, \( \lambda_F/2 \) is \((\pi/2n)^{1/2}=16.6 \) nm. So we have a normalized transconductance as high as 1.2 S/mm and a current density of only 10.8 mA/mm. The corresponded channel conductance \( g_{do} \) at \( V_{ds} \approx 0 \) V is 38 \( \mu \)S (see Figure 3b C1), so the normalized channel resistance is 0.43 \( \Omega \)mm. Comparing to current FETs, these values show that the 1D ballistic FET can be a promising device for low-power electronics.

More generally in a 1D ballistic FET, as shown above, under relative low drain voltage only the lowest subband must be used to ensure the voltage gain greater than 1, i.e., \( E_1 \) must be set around \( \mu_s \). Based on the Landauer-Büttker formalism [3], the maximum obtainable transconductance with the lowest 1D subband is \( g_{m,\max}=2e^2/h=77.5 \mu \)S. The corresponded initial channel resistance (at \( V_{ds} \approx 0 \) V) is \( R_o=1/g_{do}=h/e^2=25.8 \Omega \). Since the Fermi wavelength depends on the 2DEG density \( n \), normalized transconductance and normalized channel resistance are \( g_{m,\max}/(\lambda_F/2) \) and \( R_o \times (\lambda_F/2) \), respectively. These two parameters as a function of the 2DEG density are reported in Figure 5, and these values from the 1D ballistic FET can be used to assess the performance of 2D ballistic FETs.

![Figure 5. Normalized maximum transconductance and channel resistance of the 1D ballistic FET.](image)

In conclusion, the experimental and simulated results of the QPC transistor make clear the functioning of a ballistic FET. The injection of the ballistic electrons from the source reservoir is controlled by a gate induced subband or quantum barrier. The lowest subband can be used to produce the largest variation in charge density and thus the highest transconductance. In order to obtain a high voltage gain or a low output conductance in the ballistic regime, the key point is to realize the nonlinearity in the drain current-voltage relationship. This can only be accomplished with the help of the band gap, i.e., when the electrochemical potential of the drain is biased below the energy of the bottom of the lowest subband.

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References

[1] Datta S 1997 *Electronic Transport in Mesoscopic Systems* (Cambridge: Cambridge Univ. Press.)

[2] van Wees B, van Houton H, Beenaker C, Williamson J, Kouwenhoven L, van der Marel D and Foxon C 1988 *Phys. Rev. Lett.* 60 848

Wharam D, Thornton T, Newbury R, Pepper M, Ahmed H, Frost J, Peacock D H D, Ritchie D and Jones G 1988 *J. Phys. C* 21 L209

[3] Grémion E, Niepce D, Cavanna A, Gennser U and Jin Y 2010 *Appl. Phys. Lett.* 97 233505