Atomic transistors based on seamless lateral metal-semiconductor junctions with a sub-1-nm transfer length

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The edge-to-edge connected metal-semiconductor junction (MSJ) for two-dimensional (2D) transistors has the potential to reduce the contact length while improving the performance of the devices. However, typical 2D materials are thermally and chemically unstable, which impedes the reproducible achievement of high-quality edge contacts. Here we present a scalable synthetic strategy to fabricate low-resistance edge contacts to atomic transistors using a thermally stable 2D metal, PtTe2. The use of PtTe2 as an epitaxial template enables the lateral growth of monolayer MoS2 to achieve a PtTe2-MoS2 MSJ with the thinnest possible, seamless atomic interface. The synthesized lateral heterojunction enables the reduced dimensions of Schottky barriers and enhanced carrier injection compared to counterparts composed of a vertical 3D metal contact. Furthermore, facile position-selected growth of PtTe2-MoS2 MSJ arrays using conventional lithography can facilitate the design of device layouts with high processability, while providing low contact resistance and ultrashort transfer length on wafer scales.

The scaling of the dimensions of electronic components is essential to increase the density of devices in an integrated chip (IC)1,2. To fulfill industrial requirements, the transistors in ICs must have both ultra-short physical lengths of the gate (L < ~12 nm) and contact (Lc, which should be smaller than the required tightest metal pitch, ~16 nm) by 20341,3. In this respect, two-dimensional (2D) van der Waals (vdW) materials have emerged because of their higher carrier mobility and superior electrostatic controllability at the atomically thin limit12 to achieve channel scaling for future nanoelectronics. However, fundamental limitations in producing ultra-scaled, low-resistance contact electrodes for 2D semiconductors (e.g., transition metal dichalcogenides (TMDs))13-14 using a conventional 3D metal contact limit the switching performance of transistor. For example, the deposition of the 3D metal contact onto 2D semiconducting TMDs typically yields a disorder-rich interface at the metal-semiconductor junction (MSJ), resulting in high contact resistance (Rc)13-14. Furthermore, the resultant 3D/2D MSJs have inevitably long transfer length (LT) of charge carriers (e.g., LT > ~50-200 nm)9,10, which leads to an exponential increase in Rc with the reduction in the contact size if Lc is smaller than LT (i.e., Lc < LT), prohibiting prospective contact scaling.

To avoid the problems associated with conventional vertical contact, pioneering works on the use of edge-to-edge connected lateral 3D-2D (or 2D-2D) MSJs have been conducted15-17. It has a directly metalized junction with strong hybridization, and the absence of atomic discontinuities or defects at the lateral MSJs facilitates superior contact between the 2D semiconducting TMDs and metal electrodes (i.e., smaller Rc)13,14. Furthermore, using a lateral MSJ has a significant advantage in lowering the LT because the carriers are only injected...
through the few-atom-thick interface (i.e., $L_T$ decreases to a few nm). Thus, the lateral MSJ-based transistor performs excellently even if $L_T$ is reduced to the sub-nm range. However, owing to the general thermal and chemical instability of TMDs, practical techniques for controlling heterogeneous integration are highly challenging. Only proof-of-concept has been demonstrated\cite{4.56,4.57} thereby failing to achieve high yield and high device density. For instance, obtaining a uniform contact by lithographic techniques requires that the 2D semiconductors be protected against oxidizing conditions using a passivation layer (e.g., hexagonal boron nitride)\cite{4.11,4.13}, or in-situ etching prior to edge metallization\cite{4.1}.

Chemical vapor deposition (CVD) of TMD-based 2D-2D MSJ heterostructures lacks the control of spatial locations\cite{4.12,4.13,4.14}, and their active layer is inevitably degraded by thermal budget effect because the synthesis of 2D semiconductors along the edge of 2D vdW metals are still at the embryonic stage of development. Although graphene has been widely studied for low-resistance contacts with 2D semiconductors\cite{4.16,4.17}, the large lattice mismatch between graphene and the 2D semiconductor, along with the polymer-based residues incorporated into the assemblies during the graphene-transfer processes, commonly hinder the production of edge-contacted in-plane 2D-2D MSJs and limit the performance of the contacts\cite{4.18,4.19}. Recent studies have demonstrated significant advances towards fabricating lateral 2D-2D MSJs using irregularly-formed flakes of 2D vdW metals, Mo$_2$C and VS$_2$\cite{4.20,4.21}. However, for the approach to be practical and scalable, limitations in terms of the reproducibility of conformal MSJ patterns with sub-1-nm $L_T$ on a large scale and low $R_t$ through the suggested approach need to be addressed. Therefore, in the long term, it is vital to develop a groundbreaking technique for fabricating a 2D vdW metal with high stability and processability that can offer a substantial degree of freedom in the device architecture.

Here, we demonstrate the formation of synthetic edge contacts consisting of metallic 2D vdW PtTe$_2$ crystals with high thermal stability and the facile position-selected growth of conformal lateral 2D-2D MSJ patterns using conventional lithography. We investigated the high thermal stability of PtTe$_2$ under ultrahigh vacuum (UHV) (which maintained its intrinsic surface property up to $\sim$825 °C) and succeeded in obtaining edge-directed PtTe$_2$-MoS$_2$ lateral heterojunctions by using two-step CVD. The resultant epitaxially grown lateral MSJ sustained almost ideal stoichiometry without the development of thermally induced voids or the production of mixed alloys. The monolayer MoS$_2$ MSJ transistors with PtTe$_2$ edge contacts exhibited superior n-type carrier transport compared to those with 3D vertical contacts, attributed to both the reduced thermionic emission at the Schottky barrier and the lack of interfacial defects. Additionally, the position-controlled growth of PtTe$_2$ and subsequent chemical assembly to MoS$_2$ allowed us to obtain 2D TMD-based synthetic edge contact arrays on a large scale. The patterned MSJ showed ultralow contact resistivity (>1.7 $\Omega \cdot \mu$m$^2$), which is almost one order of magnitude smaller than those of typical 3D top contact electrodes ($10^{10}$ to $10^{13}$ $\Omega \cdot \mu$m$^2$), along with a significantly short $L_T$ (~0.7 nm), indicating the potential of PtTe$_2$ for affording drastically miniaturized high-quality metal contacts to atomic transistors.

**Results**

**Synthetic strategy for high-quality, edge-contact MSJ**

To produce electronic-grade edge contacts, we developed a synthesis method for lateral MSJs that ensures high-quality MoS$_2$ as a channel material. Many previous studies on lateral MSJs prepared using CVD rely on the growth of 2D metals after the preparation of 2D semiconductors because typical 2D semiconductors (e.g., WS$_2$, MoSe$_2$) require a relatively high growth temperature ($700$–$800$ °C) compared to vdW metals (e.g., $\sim$600 °C for NbS$_2$ or VSe$_2$)\cite{4.22,4.23}. However, this sequence for two-step CVD can thermal degrade 2D semiconductors, substantially lowering the performance of resultant device because of the increased chalcogen vacancies of the channel\cite{4.24}. Instead, we developed a technique to create a 2D semiconductor (i.e., MoS$_2$) after preparing 2D metal (i.e., PtTe$_2$) to produce a high-quality semiconducting 2D sheet in the lateral MSJ (Fig. 1a, b).

As an efficient edge contact metal for MoS$_2$, we selected one of 2D metallic TMDs, PtTe$_2$, because it exhibits many attractive features as potential n-type metal contacts for 2D semiconductors. For example, the theoretical work function (WF) of few-layered PtTe$_2$ (WF; ~4.56–4.57 eV)\cite{4.25} is one of the smallest among those reported for chemically synthesizable metallic TMDs\cite{4.32,4.33} (Supplementary Fig. 1), and its electrical conductivity ($>10^6$ S/m) has shown to be the highest among 2D metals\cite{4.36,4.37}. However, the simultaneous achievement of large-area production of high-quality stoichiometric, metallic TMD thin films with thermal stability remains challenging, mainly because of the difficulties in incorporating Te and low environmental stability during thermal CVD\cite{4.38,4.39}. Furthermore, guaranteeing the thermal stability of the 2D metal is essential for our two-step CVD process because PtTe$_2$ must resist the thermal procedure required for synthesizing MoS$_2$ while maintaining excellent quality. In this regard, no success has been achieved yet for 2D-2D lateral heterojunctions based on 2D tellurides.

Since Te vacancies substantially reduce the Gibbs free energy for the adsorption of ambient gas and cause structural instability\cite{4.30}, the growth of high-quality PtTe$_2$ is essential to ensure its stability to some extent. Thus, we synthesized the PtTe$_2$ crystals using the eutectic solidification method\cite{4.40,4.41}, where the pre-deposited Pt precursor reacted with liquefied Te at 700 °C (Fig. 1a). The resultant PtTe$_2$ formed single crystals with a highly stoichiometric nature (Supplementary Fig. 2). As our synthetic methods do not require an oxide precursor, no oxygen-metal bonds, which often become reactive sites and cause poor stability, were formed\cite{4.42}. In addition, the PtTe$_2$ crystals maintained their high-quality structures with Te terminations even after exposure to air for up to ~3 h, as indicated by TEM analysis (Supplementary Fig. 3). The WF of PtTe$_2$ (~4.65 eV), characterized by ultraviolet photoelectron spectroscopy (UPS), was comparable to the computed value\cite{4.43} (Supplementary Fig. 2h), satisfying the basic requirement of an efficient n-type contact for the MoS$_2$ transistor, considering its band structure (Supplementary Fig. 1).

To evaluate the thermal stability of the as-synthesized PtTe$_2$, the crystal was annealed under UHV conditions (~$10^{-10}$ Torr) at temperatures between $T$ = 500–1000 °C for 1 h. The Raman spectra obtained are shown in Fig. 1c. The as-grown PtTe$_2$ and the UHV-annealed crystals heated to 900 °C showed comparable Raman in-plane $E_g$ (~110 cm$^{-1}$) and out-of-plane $A_{1g}$ (~156 cm$^{-1}$) vibrational modes of PtTe$_2$ (black dashed line in Fig. 1c). Remarkably, only annealing above ~1000 °C altered the peak positions and their intensities, demonstrating the high thermal stability of the PtTe$_2$. The thermal stability is an intrinsic property independent of the thickness and degree of structure order, as evaluated by X-ray photoelectron spectrum (XPS) and UPS (Supplementary Fig. 4). The surface properties of PtTe$_2$ start to change above the $T$ of ~825 °C, which is far beyond the limitations of metallic TMDs (e.g., WTe$_2$, MoTe$_2$, TaS$_2$, and 1T-MoS$_2$) measured under vacuum or in an Ar atmosphere\cite{4.30–4.32}. In addition, low electrical resistivity of PtTe$_2$ ($\rho$ = 0.37 $\Omega \cdot$cm; Supplementary Fig. 5a, b), even lower than other few-layered metallic TMDs\cite{4.33–4.36,4.37–4.39} ($\rho$ = 0.5–100 $\Omega \cdot$cm), shows promise for a robust electrode that may prevent thermal stress as summarized in Fig. 1d.

Following the synthesis of thermal-stable PtTe$_2$ multilayers, a monolayer of MoS$_2$ was formed laterally along the edge of the PtTe$_2$ by CVD at ~700 °C (Fig. 1b). Compared to the edge, the atomically pristine, dangling-bond-free surface of a 2D crystal typically possesses fewer surface defects and minimal MoS$_2$ nucleation. Density functional theory (DFT) simulations were performed to investigate the selective nucleation of MoS$_2$ on the edges of PtTe$_2$. Adsorption energy
calculations reveal that there was preferential adsorption and subsequent nucleation of MoS$_2$ at the PtTe$_2$ edge. For instance, the MoS$_2$ monomer exhibited a lower adsorption energy of $-3.6$ eV at the PtTe$_2$ edge compared to $-2.7$ eV on the PtTe$_2$ basal plane (Supplementary Fig. 6). These findings are consistent with those of previous reports on the two-step CVD of 2D heterostructures, where in the adsorption energy of 2D TMDs at the edge of a 2D crystal was lower than that on the 2D basal plane.$^{19,40}$ The low occurrence of MoS$_2$ nucleation on the PtTe$_2$ surface is attributed to the higher adsorption energy of MoS$_2$ nuclei on the basal plane. In our experiments, we significantly lowered the mass flux of precursors through the source-contact geometry and use of a MoO$_x$ thin-film precursor significantly reduced the opportunities for nucleation (Supplementary Note 1). The attachment of adatoms or atomic clusters of MoS$_2$ by heterogeneous nucleation was allowed only at the edge of PtTe$_2$. The introduction of a higher mass flux would thus increase the possibility of producing more
nucleations and trigger the synthesis of randomly distributed multilayer MoS₂ on the structures.

Attributed to the edge-mediated growth mode, the MoS₂ crystals were observed exclusively along the PtTe₂ edges as shown in false-colored scanning electron microscopy (SEM) images (inset of Fig. 1b and Supplementary Fig. 7). The Raman signals at the interface of MSJ demonstrated the Raman signals of PtTe₂ with the characteristic peak positions, while the MoS₂ features of E₂g (∼384 cm⁻¹) and A₁g (∼407 cm⁻¹) modes also existed (Fig. 1e). Most of the MoS₂ attached to PtTe₂ was a monolayer with a uniform thickness of ∼0.7 nm, as shown in the AFM image and height profile (Fig. 1f). XPS analysis of the heterostructures was used to reveal the surface compositions and chemistries (Fig. 1g, h). Hence, the coincident binding energy of MoS₂ connected to PtTe₂ and that of the bare flakes suggests that the present growth mode conferred the intrinsic surface properties of the 2D semiconductor layer (i.e., MoS₂), as we experimentally demonstrated in the case of Ti/MoS₂ (gray, Fig. 1g). Hence, the coincident binding energy of MoS₂ connected to PtTe₂ and that of the bare flakes suggests that the present growth mode conferred the intrinsic surface properties of the 2D semiconductor layer (i.e., MoS₂), as we experimentally demonstrated in the case of Ti/MoS₂ (gray, Fig. 1g). Hence, the coincident binding energy of MoS₂ connected to PtTe₂ and that of the bare flakes suggests that the present growth mode conferred the intrinsic surface properties of the 2D semiconductor layer (i.e., MoS₂), as we experimentally demonstrated in the case of Ti/MoS₂ (gray, Fig. 1g).

We performed DFT calculations to understand the formation mechanism of defect-free interface in the lateral PtTe₂-MoS₂ MSJ (Supplementary Fig. 12). The calculated relative energies (∆E) of the possible intermediates (i.e., MoO₃ and S adsorbents) attached to the PtTe₂ edge indicated the relative stability of each atomic structure during the epitaxial growth of MoS₂ (Supplementary Table 2). We found that reactive gas-phase S atoms were bonded to MoO₆ precursor attached to the edge of PtTe₂ (∆E < −2.88 eV), and that O in MoO₃ tended to desorb as it reacted with additional S by forming SO₂(g) because of the consequent exothermic processes. A similar repeated reduction process for MoO₃ resulted in the formation of the most stable MoS₂ structure because of the substantial energy relative to the initial structure (∆E = −19.49 eV). Furthermore, each periodic interfacial cell comprised four PtTe₂ and five MoS₂ unit cells to minimize the lattice mismatch at the heterojunction (Supplementary Fig. 13). The lattice mismatch between PtTe₂ and MoS₂ was −18% when each unit cell of PtTe₂ was matched to a unit cell of MoS₂ in a one-to-one ratio according to the equation ∆a = (a₁ − a₂)/a₂, where a₁ (3.25 ± 0.05 Å) and a₂ (3.96 ± 0.05 Å) are the in-plane lattice constants of MoS₂ and PtTe₂, respectively (Supplementary Fig. 13a). In comparison, adjusting the number of unit cells on the interface to a five-to-four ratio of PtTe₂ and MoS₂ resulted in a smaller mismatch between the materials (−3%). STEM analysis also validated our heterostructure with consistently matched periodic cells along the <100> direction, indicating a (semi)-coherent interface (Supplementary Fig. 13b–d). Given this smaller interfacial cell mismatch (−3%), we calculated the most stable atomic structure for the heterostructure using DFT and the multicell model, as depicted in Supplementary Fig. 13b, c. The Pt-S and Mo-Te covalent bonds formed at the interface, resulting in strong orbital interactions between the atoms at the heterojunction.

High-performance monolayer MoS₂ FETs with PtTe₂ edge contact

We now shift our focus to the electrical characterization of the edge-contacted 2D-2D MSJ field-effect transistors (FETs). After the definition of MoS₂ channels by the reactive ion etching process, PtTe₂-flake-connected MoS₂ MSJ FETs were fabricated by Ti/Au (10/70 nm) contact pad deposition on PtTe₂. The Ti/Au layer was also deposited on the other side of the MoS₂ channel to produce an asymmetrical contacted MoS₂ channel with a fixed width (W) and length (L) for comparison with the MoS₂-Ti vertical junction (Fig. 2a, b). The gate bias was applied through the 300-nm-thick SiO₂ dielectric layer for this measurement. Because the reverse-biased contact (source) causes most of the voltage drop and dominates the transistor behavior in n-type MoS₂ MSJ FETs, the source (either Ti or PtTe₂) determines the performance of a FET with asymmetric contacts. This allows the electrical properties of the barrier to be systematically evaluated by controlling the interface. We selected Ti as the counterpart to PtTe₂ because it is the most widely used contact and has a low WF of ∼4.33 eV, which is even smaller than that of PtTe₂ (∼4.60-4.65 eV in Fig. 1g).

Figure 2g shows a representative transfer characterization (Iₜ–Vₜ) of the MSJs where the electrons were injected from the PtTe₂ edge (red) and the vertical Ti contact (blue). In addition to the output curve (Supplementary Fig. 14a), the on-state current (Iₘₜ) of PtTe₂-MoS₂ (∼4.0 μA/μm) was twice that of Ti-MoS₂ (∼1.8 μA/μm). The two-terminal field-effect mobility (μₑ) was also increased to ∼9.7 cm²V⁻¹s⁻¹ by injection of charge carriers from PtTe₂ compared to Ti (∼7.0 cm²V⁻¹s⁻¹) for the same channel (−3.5 ± 1.3 cm²V⁻¹s⁻¹ and −1.6 ± 0.9 cm²V⁻¹s⁻¹ on average for more than 10 devices with PtTe₂ and Ti asymmetric contacts, respectively; and the averaged values are demonstrated in Fig. 2h). We found a slight negative shift of the on-state current (Iₜ) because the reduced Rₛ and SBH caused the transistor easier to switch on (note that we could not observe an obvious doping effect on the in the XPS (Fig. 1g, h) and...
Raman spectra (Fig. 1e) after lateral epitaxy of PtTe2. The performance enhancement was also confirmed for the MoS2 FET with symmetric contact geometry (i.e., PtTe2/MoS2/PtTe2; Supplementary Figs. 1b–e). It showed a $\mu_{E2}$ of $-15.8 \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$, higher than those from asymmetrically contacted FET, which again verifies the influence of the resistance of the FET components related to Ti.

High-energy deposition of a 3D metal typically degrades the surface of monolayer MoS2 by forming sulfur vacancies and promoting atomic diffusion at MoS2 surfaces (i.e., forming interfacial defects of MoS2, Supplementary Figs. 1c–e). These processes increase the $R_{\text{vdW}}$ and contact resistivity ($\rho_{\text{c}}$) by forming localized states as depicted in the contact components in Fig. 2c, 2f, and 2i. In addition, the established gap states can shift the charge neutrality, pinning the Fermi level to the mid-gap of MoS2, which can significantly impact the Schottky barrier height (SBH) of the MoS2 surface (i.e., absence of $R_{\text{vdW}}$). According to Sze’s model, the Fermi level pinning (FLP) enhances increases with the density of interfacial traps ($\rho_{\text{c}}$) and sheet resistance ($R_{\text{sh}}$) of MoS2. In contrast, the PtTe2/MoS2 heterostructure has a cleaner interface that prevents further metallization on the MoS2 surface (i.e., absence of $R_{\text{vdW}}$) and the reduced BW can improve carrier injection through the edge (Fig. 2c, d). The absence of $R_{\text{vdW}}$ and the metal contact pad (i.e., Ti/Au in Fig. 2a), the contribution of the SBH of PtTe2-MoS2 MSJ (red) and Ti/MoS2 (blue) as a function of $V_g$ showing the low SBH of 38.5 meV at the flat band voltage. Inset: representative Arrhenius plot ($\ln(I_{ds}/T)$ vs. $1/TK$) of PtTe2-MoS2 heterojunction with different $V_g$. Comparison of the SBH of few-layer MoS2 based MSJ FETs with 3D top contacts (Ti, Cr, Ag, Au, and Pd; solid) and with 2D lateral contacts (Mo2C, and graphene; open). The extracted SBHs of PtTe2-MoS2 (red) and Ti/MoS2 (blue) are indicated by colored symbols. Plots of the strength of Fermi-level pinning ($\phi_{\text{FEP}}$) are shown as solid lines in order to compare the mechanism of formation of the SBHs.

High-performance edge-contacted PtTe2-MoS2 metal-semiconductor junction (MSJ) field-effect transistors (FETs). a–h Monolayer MoS2 FETs with asymmetric contact injection from PtTe2 lateral epitaxial contact and from vertical Ti, characterized at room temperature. a Schematic and (b) optical microscopy image of a device with asymmetric Ti/Au and PtTe2 electrodes contacted to a monolayer MoS2 (white dashed lines) with a defined channel width (W) and length (L). c, e Cross-sectional illustrations of resistance networks of monolayer MoS2-based MSJ with (c) asymmetrically positioned PtTe2 lateral contact and (e) top-contact with Ti/Au. Metalization of MoS2 can degrade both the contact resistivity ($\rho_{\text{c}}$) and sheet resistance ($R_{\text{sh}}$) of MoS2. In contrast, the PtTe2/MoS2 heterostructure has simpler contact geometry (i.e., PtTe2 lateral epitaxial contact and from vertical Ti (blue). The error bars indicate the standard deviations from each device set.

Summary of the thermionic barrier heights ($\phi_{\text{FEP}}$) of the PtTe2-MoS2 heterojunction with different $V_g$. The extracted barrier heights ($\phi_{\text{FEP}}$) of PtTe2-MoS2 (red) and Ti/MoS2 (blue) are indicated by colored symbols. Plots of the strength of Fermi-level pinning ($\phi_{\text{FEP}}$) are shown as solid lines in order to compare the mechanism of formation of the SBHs.

3D metal and 2D semiconductor can also produce an additional tunneling barrier ($T_{\text{vdW}}$), although Ti/MoS2 may possess a narrower $T_{\text{vdW}}$ than other 3D metals/MoS2 because of the strong hybridization. In contrast, the PtTe2-MoS2 MSJ developed herein has a clearer interface that prevents further metallization on the MoS2 surface (i.e., absence of $R_{\text{vdW}}$), leading to simple contact components only related to the edge (Fig. 2c, d). The absence of $T_{\text{vdW}}$ and the reduced BW can improve carrier injection through the edge of PtTe2. Notably, despite the presence of a vdW gap between PtTe2 and the metal contact pad (i.e., Ti/Au in Fig. 2a), the contribution of $R_{\text{vdW}}$ in the Ti/PtTe2 interface ($-0.12$–$0.23 \text{ k}\Omega\mu\text{m}$) of the MoS2-based MSJ system was insignificant ($<0.13\%$; Supplementary Fig. 16). Furthermore, the estimated $R_{\text{vdW}}$ of the Ti/PtTe2 interface is almost the lowest value that can be obtained in a 3D metal/vdW metal interfacial system (Supplementary Table 3) and is even smaller than that obtained with the most widely used vdW metal (graphene).

To gain insight into the physical characteristic associated with carrier transport through the barriers, the thermionic barrier heights ($\phi_{\text{Th}}$) of the monolayer MoS2 MSJ FETs with symmetric contacts of PtTe2 and Ti were calculated by electrical characterization at low temperatures (Fig. 2i, j and Supplementary Fig. 17). This allowed us to extract the SBHs at the interface by fitting the Arrhenius plot to the thermionic
emission model:\cit{46}:

\[ I_d = \frac{AA' T^{3/2}}{h} \exp \left( - \frac{q \phi_n}{k_B T} \right) \left[ \exp \left( \frac{q \phi_n}{k_B T} \right) - 1 \right] \]  \hspace{1cm} (1)

Here, \( T \) is the junction area, and \( A' \) is the effective Richardson–Boltzmann constant. According to Eq. (1), the \( \phi_n \) can be extracted from the slope of the Arrhenius plot (inset of Fig. 2i), resulting in \( \phi_n \) as a function of \( V_g \) (Fig. 2i). Interestingly, the \( \phi_n \) for PtTe2-contacted MSJ at the flat band voltage \( (V_{FB}) \) was found to be a substantially small value of \( \sim 35.9 \pm 9.8 \) meV (average of four devices), with fewer interfacial defects\(^{10,13,50,52} \), hence, the SBHs can follow the Schottky-Mott limit through the formation of a metal-induced gap state (MIGS)\(^{13} \), is less significant. Figure 3a shows a representative Raman spectrum of the as-synthesized PtTe2 thin film, which is vital for achieving scalable, mass production of PtTe2 electrodes in any desired shapes (Fig. 3b). The electrical characterization by the four-point probe method showed that the \( R_{on} \) of the as-synthesized PtTe2 thin film was \( H \)-dependent due to the greater carrier scattering as \( H \) decreased (Fig. 3c). The \( R_{on} \) values of the developed PtTe2 samples were lower than those previously reported for CVD-grown films\(^{43} \), and comparable to those of single-crystalline flakes\(^{37} \), indicating the atomic displacements of Te (which begins to resemble the electrical properties of Pt, as noted in caption of Supplementary Fig. 4).

Subsequent conducted thermal CVD of MoS2 induces lateral epitaxy of monolayer MoS2 from the edge of the arranged PtTe2 patterns (Fig. 3e). A key to achieving a fully stitched MoS2 thin film between the PtTe2 crystals (instead of small flakes) is the extension of the growth time while decreasing the deposition rate via delicate control of the atomic flux. A higher growth temperature (\( >730^\circ C \)) and extensive precursors (for MoOx and S) resulted in multilayer MoS2 and allowed MoS2/PtTe2 structures due to the island growth mode, whereas the layer-by-layer growth mode was enabled by the opposite manner. Figure 3f shows a representative Raman spectrum of the heterojunction, which shows the vibrational modes of each layered crystal. The Raman peaks for MoS2 in the flakes and at the interface did not differ significantly (e.g., the energy difference between \( E_2g \) and \( A_{1g} \) peaks \( \sim 19 \) cm\(^{-1} \)), suggesting the growth of monolayer MoS2. The HAADF-STEM image (Fig. 3g) and its indexed diffractionogram (Fig. 3h) confirm epitaxial alignment between monolayer MoS2 and PtTe2. The STEM-EDS and corresponding (inverse) FFT study also verified the formation of a well-stitched lateral heterojunction comprising high-quality atomic layers (Supplementary Fig. 20). We did not find any significant differences from the bare MoS2 flake in the XPS characterization of MoS2 grown along the PtTe2 array (Supplementary Figs. 8c, d).

### Spatial arrangement of synthetic edge contacts

As the ultimate approach for demonstrating the advantage of PtTe2 with respect to material processing, we eventually controlled the spatial arrangement of the synthetic edge contacts at the microscopic level (Fig. 3a). Powder-based tellurization was used to transform the Pt patterns prepared by conventional photolithography into PtTe2 patterns at a low temperature of \( \sim 400^\circ C \) (heated using Pt instead of PtO\(_N\), which can assure high quality of the resultant PtTe2)\(^{38} \). Remarkably, the patterns were successfully manufactured on a 2-inch SiO\(_2\)/Si wafer, which is vital for achieving scalable, mass production of PtTe2 electrodes in any desired shapes (Fig. 3b). The electrical characterization by the four-point probe method showed that the \( R_{on} \) of the as-synthesized PtTe2 thin film was \( H \)-dependent due to the greater carrier scattering as \( H \) decreased (Fig. 3c). The \( R_{on} \) values of the developed PtTe2 samples were lower than those previously reported for CVD-grown films\(^{43} \), and comparable to those of single-crystalline flakes\(^{37} \), suggesting that the developed films are of high quality. We found that the XPS-extracted stoichiometries for 4-nm-thick PtTe2 were almost perfect (at.% ratio of Te/Pt = 2) independent on the thermal stress up to \( T > 825^\circ C \) (Fig. 3d), suggesting the high quality and thermal stability of the film (similar to the case for single crystals in Fig. 1). The \( R_{on} \) of the PtTe2 thin film was also \( 450 \) \( \Omega \) sq for the samples annealed below \( 800^\circ C \). However, it suddenly changed as \( T \) reached \( 850^\circ C \) (\( R_{on} = 208 \) \( \Omega \) sq), indicating the atomic displacements of Te (which begins to resemble the electrical properties of Pt, as noted in caption of Supplementary Fig. 4).

Arrays of FETs composed of edge-contacted MoS2 MSJs were fabricated and operated by using an \( \text{A}_2\text{O}_3 \) back-gate dielectric (Fig. 4a). Analysis of the output and transfer characteristics (Fig. 4b, c) showed that the monolayer MoS2 FETs with PtTe2 symmetric contacts exhibited a maximum \( \mu_{FE} \) value of \( \sim 17.9 \) cm\(^2\) V\(^{-1}\) s\(^{-1} \) (average), \( \mu_{FE} \) of up to \( \sim 3.4 \) \( \mu \)A/\( \mu \)m\(^2\) and \( \mu_{FE} \) of up to \( \sim 10^4 \) \( \mu \)A/\( \mu \)m\(^2\), which are much higher than those fabricated using vertical Ti contacts on monolayer MoS2 FETs with the same device geometries (channel \( L \) and \( W \)). We repeatedly observed performance enhancement for a large number of devices (\( >15 \)), where the \( \mu_{FE} \) of the Ti/MoS2 FET was \( \sim 0.4 \pm 0.3 \) cm\(^2\) V\(^{-1}\) s\(^{-1} \) and \( \mu_{FE} \) of the PtTe2/MoS2 FETs was \( \sim 0.2 \pm 0.1 \) \( \mu \)A/\( \mu \)m. It is worth noting that, considering their \( L \) and \( W \) values, the \( \mu_{FE} \) value of the MoS2 FETs with PtTe2 edge contacts were either comparable or even higher than those of previously reported devices with various 3D edges (e.g., Sc\(^{2+} \), Ti\(^{3+} \), Au\(^{3+} \)).
and Mn) or 2D lateral contacts (e.g., graphene (Gr.), and VS2) (Supplementary Figs. 21a–c).

To determine whether the μT of a device was severely underestimated because of the contact property, we extracted the intrinsic mobility (μ0) of more than 30 different devices using the Y-function method (Supplementary Fig. 22). The μ0 value is typically free from underestimation due to Rf and provides a better indication of the intrinsic performance. The averaged μ0 value in our PtTe2-MoS2 MSJ FETs was calculated to be ~11.1 ± 4.5 cm2 V−1 s−1, which is almost comparable to the μT value (~10.6 ± 2.9 cm2 V−1 s−1) calculated using the transconductance (gms = bL/VT). The insignificant difference between μT and μ0 (~4.5%) implies the presence of a minor contact barrier at the edge interface.

Notably, by using a MSJ fabricated with transfer length method (TLM) patterns, we could determine the Rf values of the monolayer MoS2 FETs with PtTe2 edge contact (Fig. 4e, f). The TLM-driven Rf reached ~168 ± 127 kΩμm when a carrier density (n2D) of ~9 × 1012 cm−2 was attained, which was largely induced by a Vg of ~−19 V. This Rf value is ~25 times lower than that of its counterpart using Ti (~4,285 ± 1,959 kΩμm) in Fig. 4f. We note that the demonstration of Rf as a function of n2D (= Cox(Vg−Vth)/q) helps compare devices because n2D includes information on the threshold voltage (Vth) that can be varied by channel doping, the gate dielectric layer, and the interfacial trap density of the substrate. The Rf was also calculated using the Y-function method (Fig. 4g and Supplementary Fig. 22), where the minimum Rf of the device was ~18 kΩμm (~113 ± 60 kΩμm, on average) and ~2,562 kΩμm (~12,443 ± 8,406 kΩμm) for PtTe2 and MoS2, respectively. The average Rf values were comparable to those extracted from the TLM, demonstrating the reliability of the characterization methods. The low Rf obtained with PtTe2 allowed the FETs to outperform the Ti/MoS2 MSJ FETs (Fig. 4b–d).

The significantly low TLM-driven Rf at the monolayer-thick interface (e.g., Lc = 0.7 nm) of the spatially-arranged PtTe2-MoS2 MSJ suggests that the contact length (Lc) can be further scaled without an increase in Rf (Fig. 4h), as an advantage. For 3D top contacts, Rf increases as the Lc decreases below the Lc because current crowding becomes severe, according to the transmission line model expressed as Rf = √LcRsh ⋅ cot(Lc/Lc) and μc = (Rf ⋅ Lc)2 the specific contact resistivity (Supplementary Fig. 23). Thus, there have been tremendous efforts (i.e., insertion of an interlayer, chemical doping, and metal deposition under UHV conditions) to achieve immunity of Rf to Lc scaling by lowering both μc and Lc (right panel in...
Fig. 4 | Electrical transport studies of the edge-contacted PtTe2-MoS2 MSJ FETs array. a Schematic showing monolayer MoS2 FETs with patterned PtTe2 edge contacts (upper) and vertical Ti contacts (lower). The transfer length (Lt) of the carrier and physically attained contact length (Lc) are schematically demonstrated. b Representative Lc-Vc characteristics of monolayer MoS2 FET with symmetric PtTe2 and Ti contact electrodes depending on Vg. c Lc-Vc characteristics of corresponding devices on linear (symbols: right) and logarithmic scale (lines; left). d Average Rc and Lc of different FETs (>15 devices) contacted to PtTe2 (red) or Ti (blue). The error bars indicate the standard deviations of each measurement set. e Determination of contact resistance (Rc) of MSJs with different compositions using (e, f) TLM and (g) Y-function method. e TLM plot showing total resistance normalization by contact width (RW) as a function of L. The y-intercept yields the 2Rc in units of Ωμm. Inset shows OM image of MoS2 (purple-like) grown between edges of PtTe2 patterned for TLM. f) TLM-derived Rc of PtTe2-MoS2 MSJ FETs approaching \(-168 \pm 127\) kΩμm when the carrier density (n2D) of \(-9 \times 10^{12}\) cm\(^{-2}\) was largely induced by Vg (red circles), which is significantly lower than that of Ti/MoS2 (\(4.26 \pm 1.99\) kΩμm, blue squares). Solid lines specify curves fitted to the relation of Rc, depending on the n2D (Rc = n2D\(^{−0.7}\)). g Histograms of Rc for PtTe2-MoS2 (left) and Ti/MoS2 MSJ FETs (right) extracted by the Y-function method (Supplementary Fig. 22). The lowest Rc of PtTe2-MoS2, obtained in this study was \(-18.2\) kΩμm and the average value reached \(-13.0 \pm 0.3\) kΩμm. h Benchmark specific contact resistivity (ρc) and Lt of synthetic PtTe2 contacts. The experimental data from MoS2 FETs with lateral graphene contact (Gr\(^{16,19}\)), 3D edge contacts (Ti\(^{18}\), Ni\(^{12}\), Au\(^{10}\), Ag\(^{9}\), and Mn\(^{13}\)), and top contacts (Ti\(^{18}\), Ni\(^{12}\), Au\(^{10}\), Ag\(^{9}\), and Mn\(^{13}\)) are demonstrated. The colored symbols are the extracted data for PtTe2 (red stars) and Ti (blue circle) in this work. For fair comparison, the data are sorted by ρc extraction methods, i.e., four-point probe (open), TLM (solid), and Y-function (half-open symbol).

Discussion

We report here a spatially-controlled, reproducible preparation of metallic vdW PtTe2 crystals as a lateral edge contact with semi-conducting monolayer MoS2. The high-quality stoichiometric PtTe2 retained its surface properties even after CVD at the high temperature of \(-750°C\) under UHV conditions. The edge of thermally stable PtTe2 provides nucleation sites for the subsequently grown 2D semiconductor without noticeable thermal degradation, resulting in in-plane lateral MSJs without substantial interfacial issues such as alloying or void-like defects. Therefore, the PtTe2-MoS2 MSJ may have a simple resistance network and displays superior n-type carrier transport through the short and narrow thermoionic barriers, enabling the higher performance of the FET compared to that composed of vertical 3D contacts. This approach also provides a more scalable way to produce an arrangement of lateral heterostructures in a dimension-controlled manner, where the contact properties could be evaluated by using the TLM patterns consisting of the lateral MSJ. The substantially small contact resistivities achieved through the atomically thin edge suggest that the developed contact scheme has the potential for scaling the contact length for miniaturized 2D electronics.

Our work on the synthesized edge-contact MSJ arrays offers benefits in terms of scalability for both material synthesis and device fabrication. The edge contact between 2D (or 3D) metals and 2D semiconductors should be developed and evaluated based on CVD-grown 2D layers to investigate its practical potential for semiconductor technology in the future. However, almost all investigations on lateral MoS2-based MSJs have drawbacks in terms of reproducibility.

Fig. 4h). However, the achievement of a small Lt (< tens of nanometers) together with low ρc is inherently challenging for 3D top contacts\(^{30}\). Instead, the edge contact can prospectively afford a negligible Lt because carrier transport occurs strictly through the interface of the edge\(^{31,33}\) as depicted in Fig. 4a. We summarize the device performances of MoS2 FETs with 3D edge\(^{29,32,33,35,36}\) or 2D lateral contacts\(^{14,33,35,36}\) (Supplementary Table 5). Although a direct comparison of the contact properties with our device is inappropriate because of the differences in the Lf values, MoS2 channel thicknesses, and Rc-extraction methods (see Supplementary Note 3 for more details), the developed PtTe2-MoS2 MSJ had a significantly low ρc (as low as \(-11.7\) Ωμm\(^{-1}\)) and Lt = 0.7 nm, which is the lowest value among those reported for few-layer MoS2 FETS with 2D lateral graphene\(^{32,33}\), or 3D edge (Ti\(^{+}\), Ni\(^{+}\), Au\(^{+}\), Sc\(^{+}\), and Mn\(^{+}\)) contacts (see the left panel in Fig. 4h and Supplementary Fig. 21d), thus promising the realization of ultralow Rf in L-casted transistors for next-generation 2D nanoelectronics. We propose that even further reduction of Rt and SBH is possible in our PtTe2 edge contact by achieving a multilayer lateral 2D-2D MSJ heterostructure, which can be attributed to the effectively screened interfacial traps from the substrates\(^{31,32}\), the downshift of the conduction band edge in multilayer MoS2\(^{27}\), and the weaker current crowding at the thicker heterointerface\(^{10,13}\). Moreover, the use of high-dielectric oxides (e.g., HfO\(_2\), Sb\(_2\)O\(_5\), Sr\(_2\)TiO\(_3\)) passivation layers (e.g., BN), and top-gate structures, which were already applied in the previous edge-contact FETS\(^{31,32,35,36}\), can also improve the performance of our device, which can be due to the suppressed charge scattering and trapped states from surrounding disorders\(^{26,28}\).
or the achievement of pure edge contact (Supplementary Table 4). In this regard, our strategy based on direct growth of a large-area 2D metal on a dielectric substrate followed by MoS2 epitaxy has considerable advantages over other methods using 2D metals such as Mo5C2 and graphene13-15,16 formed by mechanical exfoliation of single crystal and/or transfer of CVD-grown layers. More importantly, the realization of edge contacts with the L1 between 0.01 M NaCl promoter solution was pipetted on the corner of the substrate because the unreacted Te was vaporized and sucked out toward the vacuum pump.

In addition, the construction of TLM patterns using a TMD-based synthetic edge contact provides assurance by permitting a better systematic analysis. Because of the complexity of realizing a lateral MSJ, it is difficult to achieve reproducible data from multiple devices and to perform statistical computations for Rc. Investigating Rc of edge-contact MSJs using TLM pattern proves particularly challenging because of channel-to-channel variations and deficiencies in integration scalability. Many of the studies on lateral MSJ rely on the four-point measurements10,13-15,16 or Y-function methods15-17 for Rc extraction, which can be inaccurate compared with the TLM (Supplementary Note 3). Therefore, together with the reproducibility of our 2D material system, the statistical analysis of the Rc values extracted by TLM and the Y-function method in this study can provide better insights into the electrical features of 2D-2D edge contacts.

Methods

Growth of PtTe2 flakes

The growth of multilayer PtTe2 single crystals was conducted using a conventional horizontal furnace system, in which the Te-Pt precursors on a SiO2/Si substrate were placed inside the center of the chamber. To prepare the precursor sample, a Pt thin film precursor (~2 nm, 99.9% purity pellet) was deposited using an e-beam evaporator (Temescal FC-2000), and then 0.1 g of Te powder was introduced manually to cover up the thin film. The reactant was then heated to ~700 °C (at a heating rate of ~50 °C/min) under a pressure of ~0.1 Torr using H2 (10 sccm) as the carrier gas. After maintaining a growth temperature of ~700 °C for 1 min, the furnace was naturally cooled to room temperature. We succeeded in synthesizing PtTe2 directly on top of the SiO2/Si substrate because the unreacted Te was vaporized and sucked out toward the vacuum pump.

Preparation of patterned PtTe2 thin films

The pre-deposited, poly-crystalline Pt thin film (~1 nm) on the SiO2/Si substrate and Te powder (~0.1 g) inside a quartz boat were placed in a horizontal furnace ~1 cm apart. Under low pressure (0.1 Torr) at ~400 °C, the evaporated Te vapor reacts with the Pt precursor, resulting in a homogenous, uniform PtTe2 layer with a thickness of ~4 nm. The thickness of the as-grown thin film could be controlled by modulating the Pt precursor’s thickness. For position-controllability, the shape of any desired pattern was defined using photolithography (MIDAS MDA-400S) with a photoresist with an undercut profile. To de

Synthesis of MoS2 along the edge of PtTe2

The MoS2 flakes were synthesized using MoO3 thin film (~1 nm-thick on a 1 cm2 SiO2/Si substrate, evaporated using an e-beam evaporator) and S powder as precursors in atmospheric-pressure two-zone CVD with Ar/H2 as the carrier gas. To promote the nucleation of MoS2, ~1 μL of a 0.01 M NaCl promoter solution was pipetted on the corner of the oxide thin film on the substrate. Then, the NaCl solution was baked at ~100 °C to evaporate the water entirely. The formerly prepared PtTe2 multilayers on the substrate were placed face to face on top of the MoS2 film prepared with NaCl. This metal oxide/PtTe2 sample was placed at the center of the heat zone of the furnace, with the S-powder-containing boat loaded upstream of the CVD furnace. Under an Ar/H2 ratio of 70/20 sccm, the system was steadily heated to ~700 °C. At a growth temperature of ~700 °C, S vapor was introduced because the powder was heated at ~200 °C just before reaching the growth temperature and then maintained constantly for a growth time of ~10 min. The as-synthesized PtTe2 sample was stored in a chamber under UHV atmosphere (~10^-10 Torr) immediately after synthesis, and the air exposure time of PtTe2 until the subsequent CVD process was ~5 min.

Structural characterization

The morphological investigation was conducted using an SEM (Hitachi S-4800 or SU8220) equipped with high- and low-angle BSE detectors. Micro-Raman measurements were performed with a 532 nm laser (Thermo Scientific DXR2 Raman Microscope) configured for wave-number precision of ±0.066 cm^-1. XRD patterns were captured using a Bruker AXS DS instrument with a Cu Kα source. AFM images were recorded on a Bruker Dimension AFM operating in tapping mode. High-resolution STEM images, SAED patterns, EDS were obtained using an aberration-corrected FEI Titan G2 60-300 equipped at an acceleration voltage of 200 kV. Images were subtracted by Wiener filter. EELS was performed using a Gatan Quantum 965 dual EELS system with an energy resolution of 1.0 eV under an acceleration voltage of 200 kV. Specimens for cross-section TEM analysis were prepared by focused ion beam (FEI Helios Nanolab 450HP). XPS and UPS measurements were performed using an ESCALAB 250Xi system (Thermo Fisher K-alpha) equipped with an Al Kα source under UHV conditions. The calibration of the XPS was performed by the alignment of the C 1s spectrum (whose binding energy is 284.5 eV).

DFT calculation

We constructed a × × × × × 1 PtTe2 supercell with vacuum along the b and c directions to model a PtTe2 single layer strap with an edge having 50% Te coverage. We performed geometry optimization based on DFT calculations using the supercell and the Vienna ab initio software package (VASP) code. We employed the projector-augmented-wave (PAW) method18,55,56 and the Perdew-Burke-Enzerhof (PBE) functional17 using a plane-wave basis set with an energy cutoff of 500 eV. The k-points were sampled using a × × × × 1 Monkhorst-Pack mesh19, and the spin-orbit coupling effect was also included.

Electrical device fabrication and measurements

To define the device channel, the shape of the channel layer was defined by e-beam lithography (NBL and NB3), and then a reactive ion etching process was conducted using SF6 and O2 plasma. The etched structures were transferred to a dielectric layer on highly p-doped Si, which can be used as the back-gate. For instance, the single-crystalline PtTe2-MoS2 MSJ was transferred to a 300-nm-thick SiO2 layer, whereas the conformally grown array was transferred to a 50-nm-thick Al2O3 layer. The well-connected heterointerface between PtTe2 and MoS2 confirmed through TEM analysis (Figs. 1j and 3g), proves that the wet transfer method utilizing a polymeric supporting layer did not affect the edge contact of the samples. The SiO2 layer was dry-oxidized in a furnace (KHD-306) with ±3% uniformity, and the Al2O3 dielectric layer was prepared by atomic layer deposition (Lucida, D100), being deposited within ±2% uniformity along the wafer. Ti/Au (~10–100 nm, respectively) contacts and pads were then deposited using e-beam lithography and an e-beam evaporator. Electrical characterizations at different temperatures (138-300 K) were performed using a Keithley 4200-SCS detector in a cryogenic probe station (Lakeshore CRX-4K) under a high vacuum (≈10^-10). The μFe of the FETs on the Al2O3 dielectric insulator were determined by measuring the gate oxide capacitance per unit area (Cox) of Al2O3 via C-V analysis of the metal-insulator-semiconductor structure (e.g., Pt/Al2O3/Si), where the DC voltage was swept from ~5 to 10 V, while an AC voltage with an amplitude of ~100 mV and frequency of ~20 kHz was applied. The
calculated $C_{\text{ox}}$ in the accumulation region was 0.164 ± 0.001 μF cm$^{-2}$ (average of ten devices), which corresponds to an equivalent oxide thickness of ~117.9 nm.

**Data availability**

Relevant data supporting the key findings of this study are available within the article and the Supplementary Information file. All raw data generated during the current study are available from the corresponding authors upon request.

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Author contributions
S.S. prepared materials and performed most of the experiments with assistance from J.Y., S.J., C.L., J.W., Y.S., D.J.; A.Y. and Z.L. conducted the (S)TEM characterizations; J.-K.H. and S.K.M. conducted the DFT calculations; S.S. and S.-Y.K. wrote the manuscript with the input of all other authors; all authors discussed the results and commented on the manuscript; S.-Y.K. supervised the project.

Competing interests
The authors declare no competing interests.

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