The charge islands SOI LDMOS with back-side etching technology

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Abstract. The charge islands SOI LDMOS with Back-side Etching technology structure is proposed. The new structure features the equally spaced charge islands of the upper LDMOS and a back-side etched structure of the lower LDMOS. A series of equidistant high concentration N⁺ regions are formed at the upper SOI LDMOS by the ion implanting method. The breakdown voltage of the device is improved due to dielectric field enhancement and the interaction of charges. The results show that the breakdown voltage is increased from 210V to 615V (192.8% enhanced), compared to the conventional LDMOS. The on-resistance of the as-studied stacked SOI LDMOS reduces from 48.2 Ω·mm² to 37.23 Ω·mm² comparing with conventional charge islands device, leading to a reduction ratio of 22.7%.

1. Introduction
Silicon-on-insulator (SOI) is a wide-used technique for high power integrated circuit (IC) because of its effective isolation, low leakage current and high breakdown voltage (BV) properties. However, the vertical breakdown limits to the high BV for SOI LDMOS. Many SOI LDMOS devices have been carried out [1–4] to solve the low BV and high high on-resistance(R_on) problems. Some new structures based on ENDF (enhanced dielectric layer field) have been developed to efficiently increase the BV via self-adaptive interface charges, such as using Variable-k Buried Layer [5–7], super junction [8] and Floating Metal Rings [9, 10]. Moreover, the Reduced Surface Field (RESURF) method can simultaneously improve the BV and reduce the R_on based on charge compensation effect in recent years [11–15].

In this paper, the charge islands SOI LDMOS with back-side etching technology structure is proposed. Based on the charge-induction effect, the vertical electric field is increased. The doping concentration in drift region is increased due to triple-RESURF effect. Thus the BV is improved and the R_on is decreased.

2. Structure and mechanism
Figure 1 gives a schematic diagram of the stacked SOI LDMOS (SS-LDMOS) with equidistant charge islands and back-side etched. A series of equidistant high concentration N⁺ regions at the upper SOI LDMOS are formed by ion implanting, and the lower LDMOS is realized by a back-side etching technology. N_d and L_d represent the doping concentration and the length of the drift region, respectively. t_0 and t_1 are the thickness of the bottom buried oxide(BOX) and top BOX. H, W and D are the height, width and spacing of the N⁺ region, respectively. t_S1 and t_S2 represent the upper and lower LDMOS silicon layer, respectively.
Figure 1. Schematic diagram of the cross section of (a) the proposed SS-LDMOS structure and (b) the charge distribution.

When the drift region of the device is depleted on the off-state, benefiting from the charge-induction effect, numerous electrons and holes will be induced and accumulated respectively at the two interfaces of the top BOX as shown in figure 1 (b). The N⁺ charge islands prevent the lateral electric field from extracting holes with the help of Coulomb Force. There is no vertical electric field in bottom BOX and the substrate is using back-side etching technology. Based on the boundary condition of top BOX and bottom BOX, the top BOX electric field $E_1$ of the SS-LDMOS increases from $\frac{\varepsilon_r E_s}{\varepsilon_1}$ to $\frac{(\varepsilon_r E_s + \sigma_{\text{inv}})}{\varepsilon_1}$ compared with the conventional SOI LDMOS. The $E_s$ and $Q_{\text{inv}}$ represent the electric field of SOI layer and the inversion charge density between two charge islands, respectively.

The BV of SS-LDMOS is expressed by

$$BV = 0.5t_s \varepsilon_1 E_s + \frac{\varepsilon_r}{\varepsilon_1} E_s t_1 + \frac{q t_s \sigma_{\text{inv}}}{\varepsilon_1}$$

where $\delta_{\text{n}}$ defines the characteristic charge density of a N⁺ cell. The detailed parameters of the device are listed in Table 1.

Table 1. Device parameters in the simulation.

| Device parameters | SS-LDMOS | Con-LDMOS | CI-LDMOS |
|-------------------|----------|-----------|----------|
| Drift length, $L_d$ | 40~70µm | 50~70µm | 40~70µm |
| Thickness of SOI layer, $t_{S1}, t_{S2}$ | 5 µm | 5 µm | 5 µm |
| Concentration of P-top | $2\times10^{16}~5\times10^{16}$ cm$^{-3}$ | - | $2\times10^{16}~5\times10^{16}$ cm$^{-3}$ |
| Height of charge islands, $H$ | 0.25~0.75µm | - | 0.25~1µm |
| Spacing of charge islands, $D$ | 1.5~2.5µm | - | 0.25~0.75µm |
| Width of charge islands, $W$ | 0.25~0.75µm | - | 0.25~0.75µm |

3. Results and discussion

Figure 2 shows the surface electric fields distribution of the three LDMOSs. The surface electric field of the SS-LDMOS structure is obtained at $y=7.001$ µm. It is seen from that the surface electric field in the drift region of the SS-LDMOS is greatly improved about $9\times10^4$ V/cm compared with the conventional LDMOS (Con-LDMOS), yielding to an increase of the BV. The electric field of top BOX⋯
is enhanced based on self-adaptive interface charges, which improves the distribution of the surface electric field in the drift region. The inserts show the optimized equipotential contours of Con-LDMOS, conventional charge island LDMOS (CI-LDMOS) and SS-LDMOS. The equipotential lines of the SS-LDMOS structure are very dense and uniformly distributed along the horizontal direction, however, the equipotential lines of the Con-LDMOS are concentrated on both ends of the source and drain areas. Furthermore, the SS-LDMOS and CI-LDMOS structured devices have a higher BV than the Con-LDMOS because of top BOX field enhancement from the induced interface charges.

Figure 2. Surface electric field distribution at breakdown for three LDMOSs.

Figure 3. Vertical electric field and potential distribution at breakdown under the drain for Con-LDMOS, CI-LDMOS and SS-LDMOS.

Figure 3 is the vertical electric field and potential distributions breaking down at the drain. The electric field of the top BOX increases from 90 V/µm of the Con-LDMOS to 538 V/µm of the SS-LDMOS, and the BV is 210 and 615V, respectively. The voltage drop of the top BOX of the SS-LDMOS is more than 87%, while this value is only 45% for the Con-LDMOS. The induced interface charges can effectively enhance electric field in top BOX and the top BOX plays a major role for sustaining vertical voltage to prevent premature breakdown in the silicon layer.
Figure 4. Influence of the Charge island height, width and spacing on the BV for the SS-LDMOS.

Figure 4 (a) shows the relationship between the doping concentration $N_d$ and the surface BV with different charge islands heights. The BV exhibits a close dependent relationship with the heights of the charge islands. When the charge islands height is 0.5 µm, the BV is the largest and the drift concentration is about $7 \times 10^{14} \text{cm}^{-3}$. When the charge islands height is 0.25 µm, the BV is the smallest and the drift concentration is about $1.4 \times 10^{15} \text{cm}^{-3}$. Figure 4 (b) gives the relationship between the BV and charge islands spacing $D$ for the SS-LDMOS, from which it can be seen that spacing of the charge islands has an optimal value, in which the BV is the largest. By contrast to the related figures when the charge islands width is 0.5µm and the spacing is 2µm, the BV reaches to 615V.

Process flow for the fabrication of the proposed SS-LDMOS device in figure 5. As it is shown in figure 5 (a), the starting material is a p-type SIMOX silicon wafer. The P+ is implanted to form P-top and P-well in figure 5 (b). Steps (c) is to form the gate oxide. Steps (d) is impurity implantation and annealing to form the contact regions. The N-drift is prepared by Si epitaxy in figure 5 (e). The remaining steps for forming the SS-LDMOS are: (f) the Arsenic implantation to form the N+ region in N-drift (g) CVD process (h) forming the electrodes and front passivation (i) substrate back-etching process and back passivation process.
Figure 5. Feasible key fabrication steps for forming the SS-LDMOS.

4. Conclusions

The charge islands SOI LDMOS with Back-side Etching technology structure is proposed. The structure consists two LDMOSs stacking up and down. The equally spaced charge islands are introduced into the upper LDMOS and a back-side etched structure is used in lower LDMOS. The results reveals that the BV increased from 210 V to 615 V, compared with the Con-LDMOS, leading to an increase rate of 192.8%. In addition, the SS-LDMOS reduced the $R_{ON}$ by 22.7% from 48.2 Ω·mm$^2$ to 37.23 Ω·mm$^2$ in comparison with the CI-LDMOS.

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References

[1] Wang Y, Bao M, Tian, Wang Y F, Yu C, hao and Cao F 2017 An improved SOI LDMOS with buried field plate Superlattices Microstruct. 111 340–9
[2] Li W, Zheng Z, Wang Z, Li P, Fu X, He Z, Liu F, Yang F, Xiang F and Liu L 2017 A novel P-channel SOI LDMOS structure with non-depletion potential-clamped layer Chinese Phys. B 26 17701
[3] Zhang W, Zhang B, Qiao M, Li Z, Luo X and Li Z 2017 Optimization and New Structure of Superjunction with Isolator Layer IEEE Trans. Electron Devices 64 217–23
[4] Qi L, Le L, Haiou L and Fabi Z 2017 A New Modulating Electric Field Structure with Homo-type Fixed Interface Charges
[5] Qi L, Pingjiang H, Haiou L, Nianjiong Y, Fabi Z and Yonghe C 2016 A New High
Voltage DPSOI Structure with Variable- k Buried Layer 3–6

[6] Luo X, Zhang B and Li Z 2007 A new structure and its analytical model for the electric field and breakdown voltage of SOI high voltage device with variable- k dielectric buried layer Solid. State. Electron. 51 493–9

[7] Luo X, Wang Y, Yao G, Lei L, Zhang B and Li Z 2010 Partial SOI power LDMOS with a variable low- k dielectric buried layer and a buried P-layer ICSICT-2010 - 2010 10th IEEE Int. Conf. Solid-State Integr. Circuit Technol. Proc. 31 2061–3

[8] Wei J, Luo X, Zhang Y, Li P, Zhou K, Li Z, Lei D, He F and Zhang B 2015 Accumulation-mode high voltage SOI LDMOS with ultralow specific on-resistance Proc. Int. Symp. Power Semicond. Devices ICs 2015-June 185–8

[9] Fujishima N, Saito M, Kitamura A, Urano Y, Tada G and Tsuruta Y 2001 A 700V lateral power MOSFET with narrow gap double metal field plates realizing low on-resistance and long-term stability of performance 13th Int. Symp. Power Semicond. Devices ICs (ISPSD’01), June 4, 2001 - June 7, 2001 255–8

[10] Korec J and Gerlach W 1993 Influence of Interconnections onto the Breakdown Voltage of Planar High-Voltage p-n Junctions IEEE Trans. Electron Devices 40 439–47

[11] Hossain Z and Fulton J 2002 Double-resurf 700V N-channel LDMOS with Best-in-class On-resistance 137–40

[12] Zhang J, Guo Y F, Pan D Z, Yang K M, Lian X J and Yao J F 2018 Effective Doping Concentration Theory: A New Physical Insight for the Double-RESURF Lateral Power Devices on SOI Substrate IEEE Trans. Electron Devices 65 648–54

[13] Optic U and Computation F 1995 Detection and estimation using optic flow computation Image (Rochester, N.Y.) 1529–31

[14] Luo X, Zhang B, Li Z, Guo Y, Tang X and Liu Y 2007 A novel 700-V SOI LDMOS with double-sided trench IEEE Electron Device Lett. 28 422–4

[15] Wu L J, Hu S D, Zhang B and Li Z J 2011 Novel high-voltage power device based on self-adaptive interface charge Chinese Phys. B 20 2–9