Room-temperature quantum cascade laser packaged module at ∼8 µm designed for high-frequency response

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A high-speed, room-temperature quantum cascade laser packaged module emitting at 8.14 µm is presented. The cavity length of the laser is as small as 0.5 mm, and the threshold current at 298 K is 110 mA. A matching printed circuit board is inserted into the packaged module to reduce the RC constant. As a result, the rectification response of packaged module is relatively flat up to 2 GHz and the −3 dB cut-off frequency is increased from 0.9 to 2.2 GHz.

Introduction: High-speed quantum cascade lasers (QCLs) are important for mid-infrared free-space optical communication (FSOC) because of their small size, low power consumption, and high modulation speed. QCLs emitting in long-wave infrared (LWIR) are especially attractive because of lower attenuation in the atmosphere [1]. Due to their intrinsic high-speed response the modulation bandwidth of QCLs can theoretically achieve 100 GHz level [2], but is usually limited by electric parasitic in practice. Several different device structures are applied to improve the modulation speed of LWIR QCLs. QCLs emitting at 8 µm using chalcogenide glass as insulating layer response flat up to roughly 7 GHz at 20 K [3]. An almost flat frequency response up to 14 GHz at 77 K was obtained for QCLs embedded into the microstrip line [4]. However, there are few reports on high-speed LWIR QCLs working at room temperature, especially with the packaged module.

Some previous studies [3, 5, 6] focused on reducing the parasitic capacitance of QCLs; however, the differential resistance of QCLs also contributes to the RC constant and thus influences the high-frequency performance. In this letter, we presented a packaged high-speed QCL module with improving high-frequency performance without changing the device structure.

Design and fabrication: The QCL wafer used in this experiment was grown on an n-doped (Si, 2 × 1017 cm−3) InP substrate by solid-source molecular beam epitaxy (MBE) based on a bound-to-continuum structure [7]. The laser chip was prepared as a semi-insulating InP (SI-InP, Fe-doped) buried heterostructure device with a ridge width of 8 µm. The ridge waveguide was deep etched (∼9 µm) using wet chemical etching and then the SI-InP was regrown thick enough (∼7 µm) on both sides of the ridge by metal–organic chemical vapor deposition (MOCVD) to reduce the parasitic capacitance. Next, a 450-nm thick gold layer was electrodeposited to improve the heat dissipation. After substrate thinning, contact metal deposition, and annealing, the wafer was cleaved into 0.5-mm-thick gold layer was electroplated to improve the heat dissipation. After substrate thinning, contact metal deposition, and annealing, the wafer was cleaved into 0.5-mm-long laser bars. Such a short cavity length is expected to reduce parasitic capacitance, and thus improve modulation bandwidth. At the same time, short cavity lowers electric power consumption. To reduce mirror losses, the back facet of the QCL was coated with high reflective film of ZrO2/Ti/Au/Ti/Al2O3 for reflectivity about 100%, and the front facet coated with Al2O3/Ge/Al2O3/Ge for reflectivity about 92%. Finally, the prepared QCL chip was mounted epi-layer side down on a specially designed SiC ceramic heat sink to reduce electric parasites.

The module is based on a high-heat-load (HHL) package with a matching printed circuit board (PCB) and a Sub-Miniature Version A (SMA) connector for transmitting radio frequency (RF) signals, as shown in Figure 1. The RF signal is injected from the SMA connector and the DC current from the pins on the opposite side. They are then combined on the matching PCB and sent to the QCL chip. In a sense, the matching PCB behaves like a bias tee, where the DC current and the RF signal are combined. A thermoelectric cooler (TEC) and a temperature sensor are used for temperature control. The electrical circuit schematic diagram of the module is shown in Figure 2. The values of C1, C2, and C3 are all 11 nF in this experiment but each of them can also be larger. C2 and C3 are used to block direct current (DC) and can be seen as short circuits to RF signal. The role of R1 and R3 is to increase the −3 dB cut-off frequency, and C1 can also filter the noise from the DC current source. R3 should match the impedance of the module to the RF source impedance RRF, so R3 = RRF. The simplified small-signal model of a QCL is consistent with a differential resistor RQCL and a parasitic capacitance CQCL in parallel [3], in which only the current flowing through RQCL contributes to the light emission. After injecting the radio frequency (RF) signal the RF current flowing through RQCL (IRF,QCL) will be:

\[ I_{RF, QCL}(\omega) = \frac{2}{1 + \left( j \omega C_{QCL} + R_{QCL} \right)^{-1}} \left( \frac{1}{R_{RF}} \right) \]  

\[
(1)
\]  

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where $P_{RF}$ is the setting output power of RF source. Let $I_{RF,QCL}(\omega_{-3\,dB}) = \frac{1}{2} I_{RF,QCL}(0)$ and then it can be calculated that the

$$\omega_{-3\,dB} = \left( \frac{1}{R_{QCL}} + \frac{1}{R_1} \right) \cdot \frac{1}{C_{QCL}} \quad (2)$$

After adding the PCB, the absolute value of impedance of $C_1 (~0.14 \Omega$ at 100 MHz) is much smaller than $R_1$, which can be approximated as a short circuit, so $R_1$ is equivalently connected in parallel with $R_{QCL}$, which reduces the RC constant of the whole packaged module to $(\frac{1}{R_{QCL}} + \frac{1}{R_1} + \frac{1}{R_s}) C_{QCL}$. After injecting the RF signal, the RF current flowing through $R_{QCL}$ ($I_{RF,QCL}$) will be

$$I_{RF,QCL}(\omega) = \frac{2}{1 + (R_s + R_1) \left( \frac{j \omega C_{QCL}}{R_{QCL}} + \frac{1}{R_{QCL}} \right)} \cdot \frac{\sqrt{P_{RF} R_s}}{R_{QCL}} \quad (3)$$

and the $-3 \,dB$ cut-off frequency is

$$\omega_{-3\,dB} = \left( \frac{1}{R_{QCL}} + \frac{1}{R_s + R_1} + \frac{1}{R_1} \right) \cdot \frac{1}{C_{QCL}} \quad (4)$$

Though smaller $R_1$ results in higher $-3 \,dB$ cut-off frequency and smaller DC voltage drop on $R_1$, it also causes smaller RF current going through $R_{QCL}$ at low frequency. As a compromise, $R_1$ can be selected close to $R_{QCL}$.

Experiments and discussion: Figure 3 shows the continuous-wave (CW) power–current–voltage (P–I–V) characteristics of the QCL bare chip and the packaged module. The inset shows emission spectra of the packaged module at a temperature of 298 K. According to the P–I–V characteristic curve of the bare chip, it can be calculated that the differential resistance above the threshold current is about 19 $\Omega$. At 298 K and when DC current is 120 mA, the emission wavelength of the bare chip is about 8.14 $\mu$m. The test results show that the rectification response of packaged module is relatively flat up to 2 GHz and the $-3 \,dB$ cut-off frequency is about 2.2 GHz, while that of the bare chip is about 0.9 $\Omega$. The deviation of the test result from the simulation result may be caused by the non-ideality of leads connected to the QCL and of the components on the PCB.

Conclusion: We have demonstrated a high-speed QCL module with a CW emitting wavelength of 8.14 $\mu$m and a CW output optical power about 2 mW at 298 K. The RC constant is reduced by inserting a matching printed circuit, and the $-3 \,dB$ cut-off frequency is increased from about 2.2 GHz to about 0.9 GHz. A test module has been used in the test are: the RF source setting output power is 0 dBm, the amplitude of the RF signal is modulated at 1021 Hz, and the DC current is 120 mA. For the testing circuit of the packaged module, the input of the lock-in amplifier is connected in parallel with $C_1$ whose absolute value of impedance to the rectified signal ($\sim 14.2 \,k\Omega$ at 101 Hz) is much greater than $R_1 + R_{QCL}$, so $C_1$ will have little impact on the rectified signal. It should be noted that the rectified voltage $V_{\text{rect}}$ is proportional to the square of the RF current ($I_{RF,QCL}$ or $I_{RF,QCL}$) flowing through $R_{QCL}$ [8], i.e.

$$V_{\text{rect}} \propto I_{RF,QCL}^2 \quad (5)$$

Figure 4 shows the measured microwave rectification voltage and corresponding simulation results of bare chip and packaged module, each of which is normalized. The simulation results are calculated according to Equations (1), (3) and (5). The parameters used in the simulation are: $C_{QCL} = 10 \,pF$, $R_s = 50 \,\Omega$, $R_{QCL} = 19 \,\Omega$, $R_1 = 21.5 \,\Omega$, and $R_2 = 39.2 \,\Omega$. The simulation results show that the $-3 \,dB$ cut-off frequency of the bare chip is about 1.1 GHz, and the packaged module is about 1.7 GHz, which are consistent with Equations (2) and (4), respectively.

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