Single-Stage Quadrature LMVs

Nam-Jin Oh
Departement of Electronic Engineering, Korea National University of Transportation, Chungju, Korea

ABSTRACT
This paper proposes three kinds of single stage RF front-end, called quadrature LMVs (QLMVs), by merging LNA, single-balanced mixer, and quadrature voltage-controlled oscillator (VCO) exploiting a series LC (SLC) network. The low intermediate frequency (IF) or baseband signal near dc can be directly sensed at the drain nodes of the VCO switching transistors by adding a simple resistor-capacitor (RC) low-pass filter (LPF). Using a 65 nm CMOS technology, the proposed QLMVs are designed. Oscillating at around 2.4 GHz band, the proposed QLMVs achieve the phase noise below $-107$ dB/Hz at 1 MHz offset frequency. The simulated voltage conversion gain is larger than 30 dB. The double-side band (DSB) noise figure (NF) of the proposed QLMVs is below 10 dB. The QLMVs consume less than 0.51 mW dc power from a 1-V supply.

Copyright © 2018 Institute of Advanced Engineering and Science.
All rights reserved.

1. INTRODUCTION
Low power, low-voltage, and highly integrated circuits are always the main topics for integrated circuit design, especially very important for mobile wireless communication systems due to the limitation of battery life. Single stage circuits combining mixer and oscillator have been designed for the purpose of a higher degree of integration and reducing power consumption. For highly integrated low-power receiver front-end, a current reuse technique is typically chosen across different functional blocks. A popular method is cascading the mixer on top of the input stage of the low-noise amplifier (LNA), while less frequent is stacking mixer and voltage-controlled oscillator (VCO) [1-5].

![Figure 1](image-url)

Figure 1. (a) Receiver RF front-end and (b) quadrature signal generation with two differential VCOs

A conventional VCO with a current source can be considered as a mixer when a RF signal is applied...
to the input port of the current source. For the conventional VCO, the down-converted IF signal at the VCO output is negligible due to the low impedance at the low frequency. If a series resonator is employed, the impedance is high at the low frequency and the IF signal can be recovered without any signal loss [6].

As shown in Figure 1(a), the direct conversion architecture generally requires accurate quadrature LO signals which can be generated by several methods such as combining VCO and poly-phase filter, VCO at double frequency followed by flip-flops, and the quadrature VCO (QVCO). The QVCO is the popular topology to achieve low phase noise (PN) using LC-tuned resonator. As shown in Figure 1(b), the direct connection followed by a cross connection of two differential VCOs forces to oscillate in quadrature. There are several QVCO topologies reported. The most common QVCO is called parallel QVCO (P-QVCO) which couples two VCOs in quadrature with parallel coupling transistors. Another method is called S-QVCO which couples two VCOs in a cascode-like way [7]. While the P-QVCO has low phase and amplitude errors, it has rather poor phase noise performance. On the contrary, the S-QVCO exhibits good phase noise performance with good quadrature accuracy. The third method is to couple two VCOs through the body terminals (or back-gate) of the VCO core transistors [8]. The back-gate coupled QVCO (BG-QVCO) has low phase noise compared to P-QVCO and S-QVCO. However, the BG-QVCO has larger phase and amplitude errors compared to P-QVCO and S-QVCO.

In this paper, several quadrature LMVs are proposed combining LNA, mixer, and QVCO. By exploiting a series LC (SLC) network instead of a parallel LC (PLC) network, the low frequency IF or baseband quadrature signal can be directly extracted from the drain outputs of the QVCOs. This paper is organized as follows. In Section II, the traditional LC tank oscillator is described as a mixer, and a detailed analysis for the proposed quadrature LMV (QLMV) is given. In Section III, an experimental performance is given based on simulation using 65 nm CMOS technology. Finally, a conclusion is given.

2. CIRCUIT DESIGN OF QLMVs

A conventional LC tank oscillator, as shown in Figure 2, performs the mixing process since an RF signal in the VCO bias current is down-converted by the switching transistors. Also, by the same mechanism, the dc current of $M_{cs}$ is up-converted to the LO frequency. The bandpass characteristic of the PLC resonator responds to the fundamental frequency in the current waveform and rejects higher order harmonics with a differential VCO output voltage.

$$V_{LO} = \frac{4I_{CS}R_{L}}{\pi}.$$  \hspace{1cm} (1)

With the complete switching is assumed for the $M_{sw1}$ and $M_{sw2}$, the current at the VCO output port is given by

$$i_p(t) = \frac{4I_{CS}}{\pi} \cos \omega_{LO}t + \frac{2}{\pi} g_m v_{gs} \cos(\omega_{LO} - \omega_{RF}) t + ...$$  \hspace{1cm} (2)

where $I_{CS}$ and $g_m$ are the dc current and transconductance of the current source $M_{CS}$, respectively [9]. The first term in (2) is the LO component of the VCO. The low frequency IF signal (the 2nd term) is severely attenuated since the inductor of the PLC tank is short at around dc. Also, the high frequency component (the 3rd term) is attenuated by the PLC tank. Attempting to sense the down-converted component at the VCO...
output unavoidably degrades the VCO phase noise [2]. One possible solution is to exploit the SLC network for the VCO to extract both LO and IF signals [6]. Figure 3(a) shows a SLC VCO where the coupling capacitor \( C_{\text{cpl}} \) and the inductor \( 2L \) form a SLC network. At the LO frequency, Figure 3(a) is a NMOS and PMOS cross coupled complementary VCO. When an RF signal is applied to the input of the transconductance stage, the topology with the resistance and PMOS cross-coupled load is exactly the same as the single-balanced mixer since the coupling capacitor \( C_{\text{cpl}} \) is open at IF frequency. In Figure 3(a), the current source can be modified as an LNA. The RC low-pass filter attenuates the LO component of the VCO at the drain nodes while somewhat degrading the phase noise performance.

\[
R_{\text{out}} = \frac{1}{g_{mp}} \parallel R_L = \frac{R_L}{g_{mp}R_L - 1}
\]

where \( g_{mp} \) is the transconductance of the cross coupled PMOS transistor. In (3), it can be seen that the load resistance can be maximized when \( R_L \) equals \( 1/g_{mp} \).

Figure 4 shows the simulated voltage gain with and without the PMOS load. As shown in Figure 4(a), the maximum voltage gain is limited by the resistor load with different bias current since the resistor consumes the voltage headroom. On the contrary, the voltage gain with the cross coupled PMOS load can be significantly enhanced by canceling the load resistance with negative resistance of the PMOS transistor as shown in Figure 4(b) and Figure 4(c).

Also, the noise figure (NF) of the mixer can be improved with the increased gain as shown in Figure 5. The simulation result shows that about 6 dB NF improvement is achieved with the PMOS active load at higher offset frequencies. The single balanced SLC VCO in Figure 3 can be designed to generate quadrature signals while performing the frequency mixing.

Figure 6 shows several topologies for quadrature signal generation using two VCOs [7, 8]. Figure 6(a) shows the P-QVCO in which two VCOs are coupled through the parallel transistor \( M_{\text{cpl}} \). The parallel transistor contributes large phase noise to the output. Figure 6(b) shows the S-QVCO in which two VCOs are coupled through the series coupling transistor in a cascode-like fashion. The S-QVCO displays an
excellent phase noise performance. The other method is called BG-QVCO in which the two VCOs are coupled through the body terminal (or back-gate) of the switching transistor. The BG-QVCO also shows an excellent phase noise behavior. In terms of phase and amplitude errors of QVCO, the simulation result shows that the BG-QVCO has large phase and amplitude errors compared to P-QVCO and S-QVCO.

Figure 4. Simulated voltage gain (a) load resistor only, (b) load resistor added with PMOS active load, and (c) the signal swing comparison with and without PMOS load.

Figure 5. Simulated double sideband (DSB) noise figure of the single balanced mixer with and without the PMOS load.
Several QLMVs are proposed in Figure 7 based on the QVCO topologies in Figure 6. Each QLMV has the same merits and demerits of each QVCO in Figure 6. The LNA part in Figure 7 is designed by adding a small size extra capacitor between the gate and source of the current source transistor, which enables to apply a power-constrained simultaneous noise input matching (PCSNIM) technique for low-power design [10], [11].

Figure 8 shows the small-signal equivalent circuit of the LNA in Figure 7(d). The noise mean-squared gate induced noise current is given by

\[ \overline{i_{ng}^2} = 4kT\delta g \Delta f \]  

(4)

Where

\[ g_s = \frac{\omega^2 C_g^2}{\delta g_{d0}} \]  

(5)

In (4), \( k \) is the Boltzmann constant, \( T \) is the absolute temperature, \( \delta \) is a constant with value of 4/3 in long-channel devices, \( C_g \) is the gate-source parasitic capacitance of the RF input transistor, \( g_{d0} \) is the drain-source conductance at zero drain-source voltage, and \( \Delta f \) is the bandwidth, respectively. Since the gate induced noise current has a correlation with the drain channel noise current, its correlation coefficient is given by

\[ c = \frac{i_{ng}^* i_{nd}}{\sqrt{i_{ng}^2 i_{nd}^2}} \approx -0.395 \]  

(6)

The noise factor \( F \) and noise parameters (noise resistance \( R_n \), optimum noise impedance \( Z_{opt} \), and minimum noise factor \( F_{min} \)) are given by
\[
F = 1 + \frac{1}{g_{\text{m}}R_s} \left[ \frac{\psi_{\text{dr}}}{1 - \omega^2C_{\text{c},L_s} (L_s + L_c) \left( 1 - \alpha \left| \delta \sqrt{5\gamma} \right| \right)} + (\omega C_{\text{c},R_s} \delta)^2 \left( 1 - \alpha \left| \delta \sqrt{5\gamma} \right| \right) \right] \right]
\]

(7)

\[
R_s = \frac{\gamma}{\alpha} \cdot \frac{1}{g_{\text{m}}}
\]

(8)

\[
Z_{\text{opt}} = \frac{\alpha \left( \frac{1}{\sqrt{5\gamma}} |\delta| \right)}{\alpha C_{\text{c},c} \left( \frac{1}{\sqrt{5\gamma}} |\delta| \right)} - j \alpha L_s
\]

(9)

\[
F_{\text{min}} = 1 + \frac{2}{\sqrt{\alpha}} \left[ \frac{1}{\omega} \left( 1 - |\delta| \right) \right]
\]

(10)

where \( \gamma \) is unity at zero \( V_{\text{DS}} \) and 2/3 in saturation mode transistor operation with long channel devices, \( \alpha = g_m/g_{\text{dr}} \) is unity for long channel devices and decreases as the channel length decreases. \( C = C_{\text{c},c} + C_{\text{c},s} \), and \( \omega_{\gamma} \) is the cutoff frequency and is equal to \( g_m/C_{\text{c},c} \), respectively.

The input impedance \( Z_{\text{in}} \) of the LNA is given by

\[
Z_{\text{in}} = \frac{S_{\text{m}}L_s + \frac{1}{j \omega C_s} + j \alpha L_s}{C_s}
\]

(11)

Figure 7. Proposed QLMVs. (a) P-QVCO LMV, (b) S-QVCO LMV, (c) BG-QVCO LMV, and (d) LPF and LNA

For the circuit shown in Figure 8, the condition for simultaneous noise and input matching can be satisfied when
Comparing (9) and (11), the condition that satisfy (12) is given by

\[
\frac{\alpha}{\omega C_{ex}} \left\{ \frac{\alpha^2 \delta}{5\gamma} (1-|k|^2) + \left( \frac{C}{C_{ex}} - \alpha |k| \sqrt{\frac{\delta}{5\gamma}} \right)^2 \right\} = R_s
\]

(13)

\[
\frac{\left( C - \alpha |k| \sqrt{\frac{\delta}{5\gamma}} \right)}{\omega C_{ex}} \left\{ \frac{\alpha^2 \delta}{5\gamma} (1-|k|^2) + \left( \frac{C}{C_{ex}} - \alpha |k| \sqrt{\frac{\delta}{5\gamma}} \right)^2 \right\} - \omega L_s = \omega L_s
\]

(14)

\[
\frac{g_{mL}sL_s}{C_c} = R_s
\]

(15)

\[
\frac{1}{\omega C_c} - \alpha L_s = \omega L_s
\]

(16)

From (13) and (15), the source degeneration inductor can be approximated by

\[
L_s \approx \frac{\alpha}{\omega \omega \omega C_c} \left\{ \frac{\delta}{5\gamma} (1-|k|^2) \right\}
\]

(17)

Assuming $\delta/\gamma$ is nearly constant which is about 2, $\alpha$ is less than unity, and $|k|=0.395$ for the short channel transistors [9].

Figure 8. Small-signal equivalent circuit of the LNA

3. PERFORMANCE OF THE PROPOSED QLMVs

A symmetric inductor is used to have a higher quality (Q) factor (Q=12.5 at 2.4 GHz) to have a better phase noise performance. The ac coupling capacitor $C_{cpl}$ is implemented with metal-insulator-metal (MIM) capacitor. The tuning range is varied with the MOS varactors. The transistors $M_{cpl}$ and $M_{sw,n}$ in Figure 6 are set to have the same size for fair comparison. The width of the switching transistors is 32 $\mu$m with the minimum channel length of 60 nm. The size of $C_{ex}$, $L_s$ and $L_s$ are chosen following the PCSNIM technique to match the signal source impedance of 50 ohm. The value of $C_{ex}$ is about 80 fF. Figure 9(a) shows the frequency domain analysis of the LO and IF output of the S-QVCO LMV. Figure 9(b) shows the signal swing at the RF input and IF output when $-80$ dBm RF input signal is applied. The voltage conversion gain is about 32 dB. Figure 10(a) shows the phase noise performance of the proposed QLMVs. The S-QVCO LMV
has better phase noise performance compared to other two QLMVs. It has the phase noise of –68.2 dBc/Hz, –92.4 dBc/Hz, and –113.2 dBc/Hz at 10 kHz, 100 kHz, and 1 MHz offset frequency, respectively. The frequency tuning range of S-QVCO LMV is from 2.33 GHz to 2.42 GHz.

As shown in Figure 10(b), the double sideband noise figure \( NF_{DSB} \) of the S-QVCO LMV is lower at low offset frequencies less than 0.1 MHz and higher at high offset frequencies larger than 0.1 MHz compared to other two QLMVs. The \( NF_{DSB} \) of the S-QVCO is about 9.6 dB at 1 MHz offset frequency. Table I summarizes the performance of the proposed QLMVs. To simulate the phase and amplitude errors, 0.1% tank inductor mismatch is assumed. Even though the P-QVCO LMV has the lowest phase and amplitude errors, it has inferior phase noise performance since the parallel coupling transistor contributes large phase noise. While the BG-QVCO LMV has good phase noise performance, it has large phase and amplitude errors. The S-QVCO LMV has the lowest phase noise performance and power consumption with moderate phase and amplitude errors. From the simulation results, the proposed QLMVs are expected to be successfully integrated for the direct conversion receiver such as Global Positioning System (GPS), satellite communication receiver [12], medical body area network, and cable TV (CATV) set-top box while consuming low power with just one integrated block.
Table 1. Summary of Performance of QLMVs

|                        | S-QVCO LMV | P-QVCO LMV | BG-QVCO LMV |
|------------------------|------------|------------|-------------|
| fosc(GHz)              | 2.37       | 2.48       | 2.56        |
| Phase error(°)         | 0.54       | 0.01       | 4.23        |
| Amplitude error(dB)    | 0.16       | 0.07       | 0.14        |
| Pf2(pW)                | 313        | 510        | 414         |
| Voltage gain(dB)       | 32         | 53         | 40          |
| PN@1MHz(dBc/Hz)        | -113.2     | -107.6     | -110.2      |
| NF@1MHz(dB)            | 9.59       | 7.22       | 7.44        |

*Phase and amplitude errors are simulated assuming 0.1% tank inductor mismatch.

4. CONCLUSION

By utilizing a series LC resonator, this paper proposes fully integrated RF front-end QLMVs by merging LNA, single-balanced mixer, and quadrature VCO. The proposed QLMVs are designed and simulated using 65 nm TSMC CMOS technology. The proposed QLMVs can be easily integrated on a chip, and applied for low-power high-performance direct conversion RF front-end receiver.

REFERENCES

[1] T.-P. Wang, C.-C. Chang, R.-C. Liu et al. “A low-power oscillator mixer in 0.18-μm CMOS technology,” *IEEE Transactions on Microwave Theory and Techniques*, 2006; 54(1); 88-95.

[2] A. Liscidini, A. Mazzanti, R. Tonietto, L. Vandi, P. Andreani, and R. Castello, “Single-stage low-power quadrature RF receiver front-end: The LMV cell,” *IEEE J. Solid-State Circuits*, 2006; 41(12); 2832-2841.

[3] F. Behbahani et al. “A 27-mW GPS radio in 0.35 μm CMOS,” IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers. 2002; 398-399.

[4] J. van der Tang and D. Kasperkowitz, “A 0.9–2.2 GHz monolithic quadrature mixer oscillator for direct-conversion satellite receivers,” IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, 1997; 88-89.

[5] Nam-Jin Oh, “A single-stage low-power double-balanced mixer merged with LNA and VCO,” *International Journal of Electrical and Computer Engineering (AJECE)*, 2017; 7(1); 152-159.

[6] Nam-Jin Oh, “A Single-Stage Low-Power RF Receiver Front-end: Series-Resonator based LMV cell,” *IETE Technical Review*, 2015; 32(1); 61-69.

[7] P. Andreani, A. Bonfanti, and C. Samori. “Analysis and design of a 1.8-GHz CMOS LC quadrature VCO,” *IEEE J. Solid-State Circuits*, 2002; 37(12); 1737-1747.

[8] H.-R. Kim, C.-Y. Cha, S.-M. Oh et al., “A very low-power quadrature VCO with back-gate coupling,” *IEEE J. Solid-State Circuits*, 2004; 39(6); 952-955.

[9] T. H. Lee, “The Design of CMOS Radio-Frequency Circuits,” Cambridge, U. K.: Cambridge Univ. Press, 1999.

[10] T.-K. Nguyen, C.-H. Kim, G.-K. Ihm et al., “CMOS low-noise amplifier design optimization techniques,” *IEEE Trans. Microw. Theory Tech.*, 2004; 52(5); pp. 1433-1442.

[11] Nam-Jin Oh, “Corrections to ‘CMOS low-noise amplifier design optimization techniques,” *IEEE Trans. Microw. Theory Tech.*, 2007; 55(6); 1255.

[12] T.-V. Hoi, N. T. Lanh, N. X. Truong et al., “Design of a front-end for satellite receiver,” *International Journal of Electrical and Computer Engineering (AJECE)*, 2016; 6(5); 2282-2290.

BIOGRAPHY OF THE AUTHOR

Nam-Jin Oh received the B.S. degree in physics from Hanyang University, Seoul, Korea, in 1992, the M.S. degree in electrical engineering from North Carolina State University, Raleigh, NC, USA, in 1999, and the Ph.D. degree from the Korea Advanced Institute of Science and Technology–IT Convergence Campus (KAIST–ICC) (formerly the Information and Communications University), Daejeon, Korea, in 2006. From 1992 to 1997, he was with LG Corporate Institute of Technology, Seoul, Korea. From 1999 to 2001, he was with Samsung Electronics, Suwon, Korea. From 2006 to 2007, he was with Auto-ID Lab., Fudan University, China, as a post-doctor. He joined the department of Electronic Engineering, Korea National University of Transportation (formerly Chungju National University), Korea, in 2007, where he is currently an associate professor. His research interests are focused on analog and mixed-signal integrated circuits, digital integrated circuits, system level behavioral simulation of wireless communications, and device modeling of CMOS active and passive circuits.