Design of 3-D quantum-dot cellular automata adders

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Abstract: A three-dimensional (3-D) QCA architecture is proposed in this express. The design of a 3-D quantum-dot cellular automata (QCA) full adder based on 3-D inverters and majority gates is presented and compared with its 2-D counterparts. The 3-D adder uses over 46\% less cells and occupies 40\% less area compared with the best 2-D design. The proposed 3-D QCA architecture offers an additional dimension for computation, which is not available in current CMOS technology.

Keywords: quantum-dot cellular automata, three dimensional, adder, majority logic

Classification: Electron devices, circuits, and systems

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1 Introduction

Quantum-dot cellular automata (QCA) [1, 2] technology offers significant advantages over CMOS technology in terms of higher density, faster speed and very low
power dissipation. To date, digital circuit design in QCA has focused on two-dimensional (2-D) QCA architecture [2, 3, 4]. However, recently 3-D integrated circuits [5] have attracted attention as they are expected to provide advantages of enhanced integration, more interconnection flexibility and reduced global wire length. QCA, by using field coupled cells, prefers local interconnections and could therefore significantly benefit from 3-D architectures. A 3-D architecture can be designed by using vias as connections between layers. Vias can be realized either by physical wires, as proposed for 3-D CMOS circuits [5] or by the QCA cells interacting with each other in the vertical direction, which is similar to a multi-layer crossover as used in QCADesigner [6]. The latter one is a better choice, as the cell vias can be used for both computation and communication.

In this express, a 3-D QCA adder is proposed based on the interaction of neighboring QCA cells in the vertical direction, which can perform logical computation in three dimensions with 3-D majority gates and inverters.

2 3-D QCA basic gates

The two fundamental logical building blocks in QCA are majority gates and inverters. A conventional QCA inverter (INV) can be easily designed with two diagonal cells as shown in Fig. 1(a). A 3-D inverter gate can be designed with two neighboring cells in a vertical direction with an appropriate distance between them [7]. The two nearest-neighbor cells are polarized to opposite states due to the vertical Coulombic repulsion, as shown in Fig. 1(b). The 3-D inverters can also be used as the vias between two QCA layers.

![Fig. 1. QCA inverters: (a) 2-D inverter; (b) 3-D inverter.](image)

The conventional 2-D QCA majority gate is shown in Fig. 2(a). Its functionality can be expressed as follows:

\[ M_{1L}(A, B, C) = AB + AC + BC \]  

(1)

The subscript of \( M_{1L} \) indicates that one layer is used. By using the vertical Coulombic interaction between neighbor cells, three types of 3-D majority gates can be derived. Note that the strength of the Coulomb interactions in both the vertical neighbor cells and the lateral neighbor cells are the same.

\[ M_{3L1}(A, B, C) = M_{1L}(\tilde{A}, B, C) = \tilde{A}B + \tilde{A}C + BC \]  

(2)

where the subscript of \( M_{3L1} \) indicates two layers are used with one input from layer 1. Similarly, by using the output in the layer 2 as shown in Fig. 2(c), a 3-D majority gate, \( M_{2L1} \), can be expressed by \( M_{1L} \) as follows:
\[ M_{2L2}(A, B, C) = \tilde{M}_{1L}(A, B, C) = M_{1L}(\tilde{A}, \tilde{B}, \tilde{C}) = \tilde{A}\tilde{B} + \tilde{A}\tilde{C} + \tilde{B}\tilde{C} \]  

(3)

where the subscript of \( M_{2L2} \) indicates two layers are used with its output in layer 2. Another 3-D majority gate, \( M_{3L} \), is shown in Fig. 2(d), which uses three layers with one input A from layer 1 and the output in layer 3. The relationship between \( M_{3L} \) and \( M_{1L} \) is:

\[ M_{3L}(A, B, C) = M_{1L}(\tilde{A}, \tilde{B}, \tilde{C}) = A\tilde{B} + A\tilde{C} + \tilde{B}\tilde{C} \]  

(4)

where the subscript of \( M_{3L} \) indicates three layers is used. The relationships between the three 3-D majority gates are listed as follows:

\[ M_{2L1}(A, B, C) = M_{2L2}(A, \tilde{B}, \tilde{C}) \]  

(5)

\[ M_{2L2}(A, B, C) = M_{3L}(\tilde{A}, B, C) \]  

(6)

\[ M_{3L}(A, B, C) = \tilde{M}_{2L1}(A, B, C) \]  

(7)

Fig. 2. QCA majority gates: (a) \( M_{1L} \): a 2-D conventional QCA majority gate using one layer; (b) \( M_{2L1} \): a 3-D QCA majority gate using two layers with one input from layer 1; (c) \( M_{2L2} \): a 3-D QCA majority gate using two layers with its output in layer 2; (d) \( M_{3L} \): a 3-D QCA majority gate using three layers.

3 3-D QCA 1-bit full adder design

A full adder can be designed in QCA with three 2-D majority gates [8]. The adder is defined as follows.

Inputs: operand bits \( a \) and \( b \), carry-in bit \( c_i \);

Outputs: sum bit \( s \), carry-out bit \( c_o \).

\[ s = abc_i + \tilde{a}\tilde{b}c_i + \tilde{a}b\tilde{c}_i + ab\tilde{c}_i = M_{1L}(M_{1L}(a, b, \tilde{c}_i), c_i, \tilde{c}_o) \]  

(8)

\[ c_o = ab + ac_i + bc_i = M_{1L}(a, b, c_i) \]  

(9)

A 3-D QCA full adder can be designed by using the proposed 3-D gates. One possible design is derived as follows:

\[ s = M_{1L}(M_{3L}(a, \tilde{b}, c_i), c_i, \tilde{c}_o) \]  

(10)

\[ c_o = M_{1L}(a, b, c_i) = \tilde{M}_{2L2}(a, b, c_i) \]  

(11)
The 3-D layout of the 1-bit full adder with \( a = 1 \), \( b = 0 \), and \( c_i = 1 \) is shown in Fig. 3. The clocking can be performed by conventional methods in each 2-D layer as used in [3] and the cells used as vias can be arranged in the same clocking zone.

The proposed 3-D adder is compared with its 2-D counterparts [8, 9], as shown in Table I. Cells for all designs are assumed to have a height of 18 nm and a width of 18 nm while the quantum dots have a diameter of 5 nm (same as the assumptions of [9]). Further, the cells are placed on a grid with a cell center-to-center distance of 20 nm. Although the proposed 3-D adder uses more inverters than the 2-D adder II [9] as shown in the table, the proposed 3-D architecture can save cell count and area much more than that incurred by additional inverters used in the 3-D adder, which is further illustrated in Fig. 4 and Fig. 5.

From Fig. 4, it can be seen that the proposed 3-D adder saves more than 100 cells compared with the conventional 2-D adder I. Furthermore, it uses about half as many cells as the best 2-D design to date [9]. The area comparison of 2-D and 3-D adders is shown in Fig. 5. It is clear that the area of proposed 3-D adder can be reduced by over 40% compared with both 2-D designs. The comparison results confirm that the proposed 3-D QCA adder is an area-efficient and cost-effective design.
4 Conclusion

A 3-D QCA architecture is proposed for implementation with 3-D inverters and majority gates. An efficient 3-D full adder is shown with over 46% less cells and 40% less area compared with its best 2-D counterpart. The proposed 3-D QCA architecture can perform the computation in three dimensions. Therefore, even higher integration density of QCA circuits is achievable.

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