Optimizing PWM Control for Efficiency and Reduction of False Turn-On Events in Synchronous Buck GaN Converters

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ABSTRACT
Half-bridge GaN power converters are susceptible to false turn-on events, which can lead to shoot-through and potentially device-damaging currents. There are three main parameters that can be adjusted in PWM schemes to reduce the likelihood of false turn-on events: negative gate bias, gate resistance, and deadtime. However, these PWM parameters also affect converter efficiency in the inverse way, meaning less false turn-on events must be balanced with lowered efficiency. The novelty of this paper is to investigate the trade-off between reducing GaN false turn-on events (by reducing the transient peak of gate to source voltage) and maximizing the power converter efficiency, which has not been done in prior work. This paper investigates this trade-off using a synchronous buck converter over numerous operating points with variation of the three key PWM parameters. Six converter scenarios are considered with input voltage of 200/400V, switching frequency of 50/100kHz, and output power of 500W/1kW. For each scenario, negative gate bias is set to $-4.4\,\text{V}$ and $-5\,\text{V}$, gate on-resistance is set to $10\,\Omega$ and $12.5\,\Omega$, and deadtime is varied at 60ns, 80ns, and 110ns. The results are organized into Pareto plots to find optimal points for efficiency and reduction of false turn-on events. The experimental results show that a further negative gate bias ($-5\,\text{V}$) most significantly reduces the false turn-on voltage peak and still achieves very high efficiency with appropriate selection of gate resistance and deadtime.

INDEX TERMS
DC–DC power converters, gallium nitride, energy efficiency, reliability.

I. INTRODUCTION
Due to having low losses and the capability of attaining very high switching frequencies, gallium nitride (GaN) switching devices are excellent options for power converters requiring high efficiency and low volume. A market study in [1] predicts that GaN power converters will show an annual growth rate of almost 30% in the coming years. Since their inception in the late 1970s, the GaN-HEMT structure had been mainly used in RF applications; however, in 2009, Efficient Power Conversion developed the first enhancement mode GaN on silicon (Si) FETs as power MOSFETs. The HEMT structure demonstrates an unusually high electron mobility with two-dimensional electron gas in the region of an aluminum gallium nitride (AlGaN) layer and GaN heterostructure interface [2]. Thus, even though the GaN-HEMT structure is fabricated on a Si substrate, it is quite different than a standard MOSFET device structure [2]. Among the available wide bandgap devices for power conversion, silicon carbide (SiC) and GaN, GaN has the highest electron mobility, saturated electron velocity, energy gap, and electric field breakdown limit, which are the prime reasons for the focus on GaN technology for low-to-mid levels of power conversion [3], [4].

However, along with the benefits of new GaN devices comes new design challenges, such as false turn-on events and threshold voltage instability. One main concern is the reliability of GaN devices especially in half-bridge circuits due to issues like sustained gate voltage ringing which can lead to false turn-on. False turn-on is problematic because it can increase switching losses and cause a short across the two switches in a half-bridge circuit, potentially allowing device-damaging currents to flow. This restricts the reliability of the converter and can affect the performance of the whole power converter.

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Instabilities like false turn-on occur in GaN devices because of very high dV/dt rates and related voltage oscillations during switching transients, due to the small internal capacitances, combined with the fact that the gate threshold voltage is relatively low, and is thus easy to exceed [5]–[7]. Table 1 shows how typical GaN devices have lower gate threshold voltages compared to conventional Si MOSFETs and SiC devices. This comparison shows typical values for the three different device types, where the data has been collected over wide voltage and current ratings from different manufacturers. The low threshold voltage and maximum Vgs for GaN makes gate driver design challenging because there is a very narrow band of allowable voltages.

In [6], three of the most prominent types of instabilities in synchronous half-bridge circuits are explained, including an analysis based on a second-order transfer function using positive feedback and Barkhausen criteria. The first type of instability arises due to distortion in the PWM signal whereas the other two arise because of turn-on and turn-off induced oscillations on account of high dV/dt and dI/dt transitions. Reference [7] uses a negative conductance oscillator to suppress these self-sustained oscillations and clearly highlights for both SiC and GaN that half-bridge circuits can have severe instability issues, especially for GaN due to its device structure and very fast switching times.

Though soft switching reduces the voltage ringing and crosstalk [8], [9], it requires a more complicated circuit and control algorithm. In the typical synchronous buck converter, the low-side synchronous switch turns on at ZVS since reverse conduction occurs during the deadtime before the switch is turned on. However, the high-side switch operates with hard-switching, and when it turns on with high dV/dt, the voltage oscillations affect the low-side switch, potentially raising the low-side switch gate-to-source voltage above the threshold voltage when the switch should be off. Thus, it is desirable to study how the challenges of GaN can be mitigated in the simple and widely used synchronous buck converter. This paper focuses on investigating and developing a PWM switching scheme that reduces false turn-on events by varying all three of the critical PWM parameters: gate resistance, negative gate bias, and deadtime. Though much prior work has analyzed GaN device performance, none has focused on a quantitative investigation of the trade-off between reducing the risk of false turn-on and achieving high converter efficiency. The proposed investigation uses the whole converter in full operation while varying all three of the critical PWM parameters: gate resistance, negative gate bias, and deadtime. Though much prior work has analyzed GaN device performance, none has focused on a quantitative investigation of the trade-off between reliability and efficiency. For example, Refs. [6], [7] investigate how to mitigate false turn-on events by altering gate resistance, but do not quantify the effects on efficiency. Reference [10] focuses on mitigating false turn-on by varying gate resistance and negative bias, but only considers converter operation up to 50 V and does not quantify the effect on efficiency. References [11]–[14] focus on reducing oscillations and mitigating crosstalk by varying gate resistance, but only perform the double pulse test (which cannot account for heating effects) and do not focus on efficiency. Reference [17] considers both gate resistance and negative bias in investigating the switching

| Device Type (Rating Range) | Manufacturers | Vth,nom (V) | Vth,typ (V) | Vgs,max (V) |
|---------------------------|--------------|------------|------------|------------|
| MOSFET (100V/600V)       | Vishay, Infineon | 3          | 3.5        | 20         |
| SiC (200V/650V)          | Semikron, Cree | 2.5        | 3          | 18-25      |
| GaN (100V/650V)          | GaNsystems, EPC, Transform | 1.1        | 1.7        | 6-10       |

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transient and threshold voltage instability, but does not focus on false turn-on events or efficiency. Dynamic on-resistance is investigated in [21], [27], and [28]. Furthermore, [29] and [30] investigate bootstrap capacitor behavior and designing gate drive respectively varies gate resistance and deadtime only without any relation to efficiency by performing full converter test. In [31] switch voltage slew rate is investigated, which is related to false turn-on events, but only variation in gate resistance is considered, and efficiency is not discussed in detail. Finally, [32] and [33] discuss the model to reduce false turn-on events based on non-linear capacitance and parasitic inductances, but focus only on gate resistance and negative bias PWM parameters, and do not consider efficiency as only double pulse tests are used.

The novelty of this paper is that there is no earlier work which endorses an effective PWM strategy for half-bridge eGaN-HEMTs circuits, which can relate to both false turn-on issues and power converter efficiency with a variation in all the three critical PWM parameters: gate resistance, negative bias and deadtime. In this investigation, the trade-off between converter reliability (i.e., false turn-on from voltage oscillations) and efficiency is thoroughly analyzed in order to recommend ideal PWM strategies. Section II describes the fundamental problem of instability of GaN in half-bridge circuits, Section III presents an analysis of how the PWM scheme affects false turn-on and efficiency, and Section IV presents the experimental results and discussion. Finally, Section V concludes the paper.

II. INSTABILITY IN HALF BRIDGE GaN CIRCUITS
The half-bridge synchronous buck GaN topology poses larger instability concerns than a single switch because the characteristics of one device affects the other during on and off transients. Fig. 1 shows false turn-on in the low-side GaN device in a synchronous buck converter. The root cause of the false turn-on is that after the low-side switch has turned off and the deadtime has passed, the high-side switch turns on. When this occurs, the voltage across the low-side switch rises very quickly. $C_{ds_l}$ is charged, which results in $C_{gd_l}$ and $C_{gs_l}$ being charged as well. The displacement current from the high $dv/dt$ flows through $C_{gd_l}$ to the gate node, and then some of this current flow through $C_{gs_l}$. Due to the Miller Effect, enough displacement current may flow such that $V_{Cgs_l}$ exceeds the gate threshold voltage, hence the term Miller Turn-On.

Furthermore, with the high $di/dt$, a voltage is created across the common-source inductance, which increases the effective $V_{gs}$, pushing the gate-source voltage closer to the threshold voltage. In general, the fast-switching transients of GaN combined with the low device capacitances, the capacitive coupling between the high-side and low-side devices in the half-bridge configuration, and the inevitable parasitic inductances create voltage oscillations during the switching transient period.

Fig. 2 (a) shows the displacement current paths in the low-side switch (in blue) that result from the high $dv/dt$ event of the high-side switch turning on while the low-side switch is off. In this case, the off-state gate voltage is shown as zero, meaning a negative gate bias is not used. This current can result in the charging of $C_{gs}$ above the threshold voltage. Current will also flow in the red path through the gate driver, and the value of this current will depend on the impedance of the gate drive circuit, including the off resistance, $R_{g,off}$. By using KCL,

$$i_{Cgd} = i_{Cgs} + i_{R_{g,off}} \quad (1)$$

Thus, $R_{g,off}$ should have a low value to minimize the displacement current flowing through $C_{gs}$. This is one way of providing Miller compensation [25], [26]. Thus, in this paper, $R_{g,off}$ is kept at a constant low value (2 $\Omega$).
Fig. 2(b) shows another, generally more effective approach for Miller compensation, which is to use a negative gate bias during the off time of the device [34]. The negative gate voltage bias charges $C_{gs}$ to a negative voltage, which adds immunity to false turn-on because this negative voltage partially cancels out the positive voltage generated across the common source inductance during the high $di/dt$ event. Thus, the effective $V_{gs}$ oscillations during the high-side switch turn-on transient will have a lower peak voltage, reducing the chance for false turn-on.

However, since using a lower negative gate bias voltage also increases device reverse conduction losses during the deadtime, this paper performs an in-depth investigation of negative gate bias values considering converter efficiency.

### III. PWM STRATEGY

This paper investigates three critical aspects of an effective PWM to balance converter efficiency with a reduction of false turn-on events in the synchronous buck converter: gate turn-on resistance ($R_{g,on}$), negative gate bias, and dead time selection.

#### A. GATE TURN-ON RESISTANCE

Since it is the turn-on of the high-side switch which causes the high $dv/dt$ across the low-side switch and thus induces the gate oscillations leading to false turn-on, this paper investigates the effect of changing $R_{g,on}$ of both switches. With a larger $R_{g,on}$, the high-side switch will turn on more slowly, inducing a lower $dv/dt$ across the low-side switch. Furthermore, a larger $R_{g,on}$ in the low-side switch gate drive circuit will add more damping to the resulting oscillations from the switch internal capacitances and the circuit stray inductances.

Thus, it is clear that a larger $R_{g,on}$ will reduce the chances of false turn-on events. However, a larger $R_{g,on}$ will also increase turn-on switching losses in both devices due to a slower turn-on event and thus a larger overlap of voltage and current during the turn-on transition.

This paper will quantify these benefits and drawbacks of using a larger $R_{g,on}$ by considering 10 $\Omega$ and 12.5 $\Omega$ values for $R_{g,on}$. The 10 $\Omega$ value is selected because it is the default recommended value by GaN Systems for use with the evaluation board [35]. The value of 12.5 $\Omega$ is selected as a 25% increase from the default value to aim to still achieve high converter efficiency while dampening switching oscillations.

#### B. NEGATIVE BIAS

Using a negative gate bias during the off-time is a well-known method to reduce false turn-on events [10]–[15], though the negative bias must be kept within a safe operating area such as higher than $-10 \, \text{V}$ to prevent device damage and significant gate threshold instability. As discussed, the negative bias lowers the $V_{gs,1}$ false turn-on peak voltage as it partially cancels out with the positive voltage generated across the common-source inductance during the high $di/dt$ event. However, a negative gate bias also increases reverse conduction losses. Though GaN devices do not contain a body diode, they can conduct reverse current through the main channel when off, similar to a body diode. A lower negative gate bias will increase the voltage drop across the switch while in the reverse conduction mode, $V_{sd,rev\_cond}$, increasing losses [35]. Equation (2) describes this reverse conduction power loss that is proportional to $V_{sd,rev\_cond}$, which is in turn a function of the negative gate bias, $V_{gs,off}$. In (2), $I_{sd}$ is the reverse conducting current, $t_{dead}$ is the deadtime, and $f_{sw}$ is the switching frequency.

$$P_{loss,rev\_cond} = V_{sd,rev\_cond}(V_{gs,off}) \cdot I_{sd} \cdot 2t_{dead}/f_{sw}$$  \hspace{1cm} (2)

Thus, a moderate negative gate bias of around $-3 \, \text{V}$ is often recommended to minimize the extra losses associated with this reverse conduction characteristic [34], [35]. This paper will quantify the benefits and drawbacks of using further negative gate biases of $-4.4 \, \text{V}$ and $-5 \, \text{V}$ on both false turn-on likelihood and converter efficiency.

#### C. DEAD TIME

The selection of the deadtime affects converter efficiency and false turn-on events. With a longer deadtime, the low-side switch will conduct in the reverse direction for a longer period of time in each switching cycle and these losses will also be dependent on the negative gate bias [3], as shown in (2). However, a longer deadtime will leave more time for intrinsic capacitances in the switch to completely discharge before the high-side switch turns on, and thus can reduce false turn-on voltage oscillations. The lower limit on a desirable deadtime is that which allows the low-side synchronous switch to turn on at ZVS, as operating without ZVS would decrease efficiency. Equation (3) shows the calculation of this limit [36]–[38], as the deadtime must be long enough to allow the current flowing through the switch, $I_{out}$, to discharge the effective device output capacitance, $C_{o(\text{effective})}$, to discharge $V_{ds}$ from $V_{in}$ to zero.

$$t_{dead} \geq \frac{C_{o(\text{effective})}V_{in}}{I_{out}}$$  \hspace{1cm} (3)

However, modelling $C_{o(\text{effective})}$ during the switching transient has always been an issue as the C-V curve follows a nonlinear relationship. The most conventional ways are to consider energy-related and time-related output capacitances. $C_{o(\text{er})}$ is the capacitance which gives the same stored energy as output capacitance $C_{oss}$ while $V_{ds}$ increases from zero to $V_{in}$ based on the principle of conservation of energy, and $C_{o(tr)}$ is the capacitance which gives the same charging time as $C_{oss}$ while $V_{ds}$ increase from zero to $V_{in}$. Choosing the maximum of $C_{o(tr)}$ and $C_{o(\text{er})}$ gives a reasonable approximation of $C_{o(\text{effective})}$ as shown in (4).

$$C_{o(\text{effective})} = \max(C_{o(\text{er})}, C_{o(tr)})$$  \hspace{1cm} (4)

The GS66516T datasheet gives the values of $C_{o(\text{er})} = 207 \, \text{pF}$ and $C_{o(tr)} = 335 \, \text{pF}$, meaning $C_{o(\text{effective})}$ should be 335 pF. This research investigates three combinations of $V_{in}$ and $I_{out}$...
TABLE 2. Experimental setup parameters.

| Parameter                  | Value       |
|----------------------------|-------------|
| DC input voltage           | 200, 400 V  |
| DC load output             | 5, 10 A     |
| Switching frequency        | 50, 100 kHz |
| Duty cycle                 | 50%         |
| Power inductor             | 2 × 60 µH   |
| Input/output capacitor     | 20 µF       |
| Gate turn-on resistance    | 10, 12.5 Ω  |
| Gate turn-off resistance   | 2 Ω         |
| Negative bias              | -4.4, -5.0 V|
| Deadtime                   | 60, 80, 110 ns|

IV. EXPERIMENTAL RESULTS AND DISCUSSION

The experimental circuit is a synchronous buck converter, as shown in Fig. 4. The circuit uses GaN Systems’ GS665MB-EVB evaluation board [35] with GS66516T 650V/60A rated devices and ACPL-346 gate drivers. The devices use ultra-low inductance packaging, and a dedicated source sense connection is used on the PCB to minimize the gate loop inductance. Table 2 summarizes the experimental setup parameters. Two CWS high frequency power inductors of 60 µH each are used in series along with a 20 µF output capacitor.

Fig. 5 shows the whole experimental setup whereas Fig. 6 shows a closer view of the buck converter and the measurement probes. In Fig. 5, the experimental setup includes a Sorensen SGX programmable DC power supply and a Chroma 63804 programmable AC/DC electronic load, which is used to maintain either a constant 5 A load current (for tests with 400 V and 200 V input voltage) or a constant 10 A load current (for tests with 200 V input voltage). The Tektronix MSO54 4-channel 500 MHz mixed signal oscilloscope is used. The high-side switch Vgs and Vds are measured with TMDP0200 differential probes with 200 MHz bandwidth. The low-side switch Vgs is measured with the
FIGURE 7. (a) Voltage and current switching waveforms for $V_{in} = 400V$, $R_{g,\text{on}} = 10\ \Omega$, $V_{gs,\text{off}} = -5\ V$, (b) Zoomed-in view of low-side switch turn-on, (c) Zoomed-in view of low-side switch turn-off.

ISOVu 500 MHz probe (tripod) as shown in Fig. 6. The low-side switch current is measured with the TCP0020 current probe with 50 MHz bandwidth.

FIGURE 8. $V_{gs,\text{low}}$ measurements for $V_{in} = 400V$ and $f_{sw} = 100\ kHz$ for four different test cases of negative bias and $R_{g,\text{on}}$ (a) zoomed out (top) (b) zoomed-in (bottom).

The bipolar gate drive signal is produced using a 5-11V DC/DC converter which generates a dc rail that is split into positive and negative terminals. The positive terminal is set by a Zener regulator circuit which has an RC divider branch coupled to it. The output of the DC/DC converter is fed into the isolated ACPL-P346 gate driver which drives the high and low eGaN-HEMTs separately. The Zener regulator provides a particular bipolar PWM signal so that two different bipolar PWM signals $+6.2/-4.4V$ and $+5.6/-5V$ can be generated.

Fig. 7 (a) shows the measured switching waveforms of the circuit for $V_{in} = 400\ V$, $f_{sw} = 100\ kHz$, $R_{g,\text{on}} = 10\ \Omega$, and $V_{gs,\text{off}} = -5\ V$. Fig. 7 (b) and (c) show zoomed-in version of the turn-on and turn-off transitions for the low-side switch. In Fig. 7 (c), it can be seen that when the low-side switch has turned off and the high-side switch turns on, $V_{gs,\text{low}}$ has a voltage oscillation peak of 19.5 V, well above the typical threshold voltage of 1.7 V. Also, in Fig. 7 (b), when the high-side switch has turned off and the low-side switch turns on, $V_{gs,\text{high}}$ oscillations are not significant. This result shows that the low-side switch is the primary concern for false turn-on
events and agrees with findings [13], [14]. The rate of rise of the voltage of the low-side switch is primarily determined by the turn-on speed of the high-side switch, which is dependent on $R_{g_{on}}$.

Table 3 shows how the drain-to-source $dv/dt$ of the low-side switch varies with $V_{in}$, $R_{g_{on}}$, $V_{gs,off}$, and $t_{dead}$ for 100 kHz switching frequency at 200 and 400 V input and at 1 kW output power. For $V_{in} = 200$ V, $R_{g_{on}} = 10$ Ω produces an average $dV_{ds-low}/dt$ of 27.7 V/ns and $R_{g_{on}} = 12.5$ Ω produces an average $dV_{ds-low}/dt$ of 25.7 V/ns. For $V_{in} = 400$ V, $R_{g_{on}} = 10$ Ω produces an average $dV_{ds-low}/dt$ of 49.8 V/ns and $R_{g_{on}} = 12.5$ Ω produces an average $dV_{ds-low}/dt$ of 45.8 V/ns.

Fig. 8 shows the $V_{gs,low}$ waveforms for $V_{in} = 400$ V, $f_{sw} = 100$ kHz, $I_{load} = 5$ A, and $t_{dead} = 80$ ns for four different test cases of negative gate bias and $R_{g_{on}}$ after the low-side switch is turned off and when the high-side switch is turned on (after the deadline). The peak $V_{gs,low}$ voltage value during this time is selected as a metric to measure the likelihood of a false turn-on event occurring. Fig. 8 shows that the $-4.4$ V gate bias leads to a higher $V_{gs,low}$ peak for both $R_{g_{on}}$ values tested, and that this peak is well over the nominal threshold voltage of 1.7 V. However, the $-5$ V gate bias reduces these oscillation peaks.

Fig. 9 summarizes the efficiency results for all six test cases. Increasing the deadline (within the selected range) had the smallest effect on efficiency for all cases. Increasing the negative gate bias from $-4.4$ V to $-5$ V (solid lines to dashed lines) causes a moderate drop in efficiency.

Fig. 10 presents the results in Pareto plots such that the lower left corner is the optimal operating point of high efficiency and low false turn-on peak voltage. Thus, it combines the efficiency results with measured peak $V_{gs}$ values of the low-side switch measured at the moment when
the high-side switch turns on, i.e., after the low-side switch has turned off and the dead time has passed.

Fig. 10 shows that for the 200 V test at both 500 W and 1 kW power levels, increasing the deadtime makes little difference in peak $V_{gs,\text{low}}$ (less than 1 V), but lowers efficiency, so is not recommended. Thus, the minimum deadtime of 60 ns is recommended for 200 V operation at either power level or switching frequency. For the 200 V cases, lowering $V_{gs,\text{off}}$ from $-4.4$ V to $-5$ V has the largest influence on reducing the false turn-on peak voltage, and thus on reducing the potential for false turn-on events. Increasing $R_{g,\text{on}}$ to 12.5 $\Omega$ (blue lines vs. red lines) slows down the switch transition at turn-on, increasing turn-on switching losses, and leading to lower efficiency compared to $R_{g,\text{on}} = 10 \Omega$. These results show that the value of $R_{g,\text{on}}$ has a relatively large influence on efficiency, compared to the effects of increasing deadtime or negative bias. By keeping deadtime low (at 60 ns) it is possible to achieve very high efficiency even at the lower negative gate bias of $-5$ V, despite the larger reverse conduction losses. The highest efficiency is obtained with 60 ns deadtime, $R_{g,\text{on}} = 10 \Omega$, and $V_{gs,\text{off}} = -4.4$ V.

It can be seen in Fig. 10 that at 200 V and at both power levels, the average reduction in peak $V_{gs,\text{low}}$ by using $V_{gs,\text{off}} = -5$ V is 6 to 7 V. For the 200V/500W case (Fig. 10(a) and (b)) all tests with $V_{gs,\text{off}} = -4.4$ V (square markers: all deadtimes, both $R_{g,\text{on}}$ values) had peak $V_{gs,\text{low}}$ values over 6 V, meaning over the device threshold voltage, and instead using $V_{gs,\text{off}} = -5$ V lowered all peak $V_{gs,\text{low}}$ Values to below the threshold voltage (circle markers). For 200 V at both power levels, using higher $R_{g,\text{on}} = 12.5 \Omega$ (compared to 10 $\Omega$) makes little difference in peak $V_{gs,\text{low}}$, but reduces efficiency by about 1%, and is thus not recommended. Thus, $R_{g,\text{on}} = 10 \Omega$ is recommended. Overall, for 200 V operation, to achieve a good balance of
The experimental results show that, as expected, switching frequency does not play a major role in determining the dV/dt slewing rate (which impacts stability), as evidenced by the similar Vgs peak voltages at both 50 kHz and 100 kHz for the same other conditions. Thus, the general findings of this paper are applicable to lower and higher switching frequencies commonly used in power converters.

V. CONCLUSION AND FUTURE WORK

The novelty of this paper is that it investigates the tradeoffs between reducing GaN false turn-on events and achieving high power converter efficiency, which has not been covered in prior work. The proposed investigational method includes varying all three main PWM parameters (gate resistance, negative bias, and deadtime) over a wide range of operating points in a synchronous GaN-based buck converter (where false turn-on is a more prevalent issue compared to other topologies). Reliability is estimated based on the measured peak gate voltage oscillation that occurs on the low-side switch while the high-side switch is turning on. Overall, for 200V operation, to achieve a good balance of reliability and efficiency, it is recommended to use Vgs,off = −5 V, Rg,off = 10 Ω, and deadtime = 60 ns. At the lower power level (500 W), this PWM strategy completely removes any risk of false turn-on, as the peak gate voltage oscillation is below the device threshold voltage. Overall, for 400V operation, if reliability is of the highest concern, it is recommended to use Vgs,off = −5 V, Rg,off = 10 Ω, and deadtime =110 ns. If it is most important to have a good balance between reliability and efficiency, the recommended PWM strategy is Vgs,off = −5 V, Rg,off = 12.5 Ω, and deadtime = 110 ns. In summary, the use of a further negative gate bias of Vgs,off = −5 V was found to be an important part of an ideal PWM strategy balancing efficiency and reliability, and thus it is recommended that engineers should consider using more negative gate biases to −4 V than the commonly recommended −3 to −4 V.

Future work will include expanding the investigation to other converter topologies. Furthermore, active gate drivers will be investigated to further reduce the chances of false turn-on events by damping the gate oscillations.

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