Phase-locked subdivision method of digital signal based on FPGA

Han Hou 1,2,a, Guohua Cao 1,2,b*, Hongchang Ding 1,2,c, Kun Li1,2,d, Aijia Wang 1,e
1Mechanical Engineering, Changchun University of Science and Technology, Changchun, Jilin, China
2Changchun University of Science and Technology Chongqing Research Institute, Chongqing 401135, hgcelikun@163.com China
aemail: eric_houyz@163.com, cemail: dinghc@cust.edu.cn,
dhgelikun@163.com@163.com, email: aijia_wang2020@163.com
*Corresponding: bemail: caogh@cust.edu.cn

Abstract. In order to improve the accuracy and real-time performance of the subdivision signal expression result of the photoelectric encoder in the signal dynamic measurement process, a phase-locked subdivision method of digital signal based on FPGA is proposed. The open-loop structure is used to realize the large-range detection of the grating measurement system, and the fractional frequency division method is used to realize the subdivision function of the grating moiré signal. In order to verify the effectiveness of the design, we compare the analog signal subdivision with the traditional digital phase-locked subdivision method. The experimental results show that the digital phase-locked subdivision algorithm designed in this paper can be used in the high-frequency moiré signal frequency and rate of change. The subdivision function is realized under the following conditions, which can be better applied to dynamic measurement occasions.

1. Introduction

Moiré grating is an important component of grating sensors in grating rulers and photoelectric encoders. It is widely used in precision measurement fields such as optical engineering precision measurement, aerospace, military measurement, etc[1-2][3], used to achieve linear displacement measurement and circular accurate measurement of arc angular displacement.

At present, there are three subdivision methods for moiré grating signals: mechanical subdivision methods, optical subdivision methods and electronic subdivision methods. Among them, the electronic subdivision method has the advantages of high subdivision accuracy and high system integration, and is widely used in the field of detection.

At present, many scholars have done a lot of work on the research of grating moiré signal subdivision. In 2008, the American Astronomical Observatory proposed an adaptive period error compensation method for Heidhain photoelectric encoder[4], which realizes the compensation of various errors of the grating signal. The disadvantage of this method is that it requires a large number of high-order matrices. Calculation, causing the system to run slowly; Sun proposed a triangular signal integral compensation method for Moiré delta interpolation error [5], in the process of experimental testing, the error compensation system reduces the interpolation error to ⅓ of the original error; Chen Ran from Changchun University of Science and Technology and others proposed a subdivision error
compensation method based on BP neural network[6]. From the perspective of compensation effect, this error compensation method reduces the original error from 20" to less than 2"; By determining the subdivision multiplication of the input signal, a corresponding look-up table is established in the FPGA. The voltage-controlled oscillator finds the division factor based on the geology and outputs the multiplication correction. Signal, the experiment proves that this method can achieve 200 times subdivision. However, when the frequency range of the input signal is relatively high, the required look-up table occupies high logic resources of the FPGA, and the logic operation is difficult [7].

In view of the above-mentioned scholars’ shortcomings in the study of subdivision errors, this paper proposes an improved digital phase-locked subdivision method for digital subdivision of moiré grating dynamic signals, by completing the circuit development of the digital subdivision algorithm on the FPGA platform. The experimental results show that the improved digital phase-locked frequency multiplication and subdivision method can effectively realize the moiré grating signal subdivision function in the dynamic measurement process.

2. Principle of phase-locked subdivision of grating moiré signal

2.1. Principle of grating moiré signal

![Moiré grating measurement system](image)

The Moiré grating measurement system is mainly composed of light source, optical system, indicating grating, grating code disc and photoelectric receiver as shown in the figure. We define the grating moiré signal :

\[ u(x) = U_m \sin \theta(x) \]  

Among them: \( U_m \) is the amplitude of the input signal, \( \theta \) is the phase value of the grating moiré signal, and \( \theta = 2\pi \theta / W \) is the grating distance \( W \) from the \( \theta \), and \( x \) is the grating displacement.

2.2. Principle of digital phase-locked subdivision

The principle of digital phase-locked subdivision mainly includes a phase detector, a loop filter, a numerically controlled pressure cavity oscillator, and a frequency divider.

When the frequency of the input signal \( x(n) \) is \( f_i \), the signal frequency \( f_o \) of the system output signal \( y(n) \) can be expressed as:

\[ f_o = Nf_i \]  

Among them, \( N \) is the subdivision frequency.

The phase difference between the phase detector detection signal \( x(n) \) and the frequency divider
feedback signal $b(n)$ is the output square wave pulse signal $p'(n)$. Under normal circumstances, the square wave pulse signal $p(n)$ is input into the digital loop filter, and the output signal is:

$$p'(n) = h(n) \otimes p(n)$$  \hspace{1cm} (3)

$h(n)$ is the impulse response function of the digital loop filter $p'(n)$; the pulse width of $p'(n)$ is $p'$.

The output signal $p'(n)$ of the loop filter is the output signal of the numerically controlled oscillator, and its size will affect the frequency $f_o$ of the output signal $y(n)$ of the numerically controlled oscillator:

$$f_o = Nf_i + K_o P_i = f_c + K_o P_i$$  \hspace{1cm} (4)

$K_o$ represents the gain amplitude of the numerically controlled oscillator; $f_c = Nf_i$ is the core frequency of the numerically controlled oscillator. After the output signal $y(n)$ of the system passes through the $N$ frequency divider, the result is fed back to the input end of the system, thus forming a closed-loop control structure. The frequency of the feedback signal $b(n)$ of the system is expressed as:

$$f_o = f_i \frac{1}{N}$$  \hspace{1cm} (5)

Normally, when the input signal frequency is relatively stable, through closed-loop feedback adjustment, the phase difference between the input signal and the feedback loop signal can be close to 0, that is, $p' = 0$. When the system loop is relatively stable, the output signal $y(n)$ is close to the center frequency $f_c$ of the system. From equation (4), the system can complete the subdivision function of $N$ times.

From the analysis of system functions, although the photoelectric closed-loop structure can achieve better subdivision effects when the input signal is relatively stable, the loop lock requires more complicated calculations, longer execution time, and bandwidth setting of the loop filter. It will affect the frequency bandwidth of the input signal to a certain extent. Therefore, it is difficult for the traditional digital phase-locked frequency multiplication and subdivision method to output the grating moiré signal to a larger range of the moiré grating measurement system, and it has a higher impact on the precision of the phase-locked subdivision in the high-frequency domain.

3. Algorithm of improved phase-locked subdivision

In response to the problems raised in the previous article, the open-loop structure is used to achieve the improvement of the digital phase-locked frequency multiplication and subdivision method. The principle structure is shown in the figure:

![Fig.2 Modified digital phase locked subdivision](image)
In the dynamic detection process of the Moiré grating error, when the input signal $x(n)$ frequency $f_i$ continuously changes, since the input signal quantization value and the subdivision multiple are both integers, the clock division factor will appear non-integer. The method of fractional frequency division is adopted to realize the subdivision of the phase-locked loop.

The fractional frequency division algorithm divides the frequency of $f_{clk}$ according to the integer frequency keyword $M, M+1$ to achieve subdivision. According to formula (4), the integer frequency keyword $M$ can be defined as:

$$
M = \text{int}\left(\frac{y'(n)}{N}\right)
$$

$$
M \leq C = \frac{y'(n)}{N} \leq M + 1
$$

According to the input signal frequency quantization value $y'(n)$ and the digital subdivision multiple $N$, we can get the integer frequency key characters $M$ and $M+1$ that match the input signal frequency and frequency, so that the corresponding frequency expression can be obtained:

$$
\begin{align}
M &= \text{int}\left(\frac{y'(n)}{N}\right) \\
M &\leq C = \frac{y'(n)}{N} \leq M + 1
\end{align}
$$

When the frequency $f_i$ of the input signal $x(n)$ continuously changes, the size of $T_i$ will also change, but the output frequency of the frequency divider is too single, and it is difficult to ensure that a complete signal cycle $T_i$ is completed within $N$ cycles. In the $T_i$ time range, $k_1$ period $f_M$ signals and $k_2$ period $f_{M+1}$ signals are output, and $k_1 + k_2 = N$.

$$
T_M = \frac{1}{f_M}, \quad T_{M+1} = \frac{1}{f_{M+1}}
$$

express the above process as the following formula:

$$
k_1M + k_2(M + 1) = y(n)
$$

From the results after sorting, all variables are taken as integers here, so by limiting the value of $M, M+1, k_1, k_2$, the $N$ times subdivision of the input signal at any frequency can be completed. Realize the equivalent effect of fractional frequency division under different input signals.

4. FPGA implementation of phase-locked subdivision method

In order to ensure the real-time and rapidity of the digital subdivision circuit. The overall circuit block diagram of the moiré signal subdivision processing based on the improved digital phase-locked subdivision method is shown in Fig.3.

![Fig.3 Optimize the principle of digital phase-locked subdivision circuit](image-url)
The digital subdivision system is mainly divided into two parts, the preprocessing circuit and the FPGA processing module. Among them, the preprocessing module includes two parts: digital signal sampling and analog-to-digital conversion, which are used to collect and amplify the output signal of the moiré grating; in the FPGA processing module, the quantization parameter solving module uses the edge detection and counting device to process the input signal to obtain the quantized value \( y'(n) \).

In order to effectively improve the dynamic detection capability of the detection system, the quantization parameter solving module uses the parallel structure of FPGA to solve the \( M, M+1, k_1, k_2 \) in the system parameters. This method can effectively reduce the clock delay in the system output module.

\[
\begin{align*}
    k_1M + k_2(M+1) &= y'(n) \\
    k_1 + k_2 &= N \\
    k_2 &= y'(n) - NM
\end{align*}
\]

Bringing (9) into the equation, we can simplify:

\[
k_2 = \text{mod}(y'(n), N)
\]

In order to reduce the system delay problem in the process of parameter solving, while comparing \( k_1 \) and \( k_2 \), the \( N/2 \) value can be obtained by shifting. Then through the comparator, compare the size relationship between \( k_1 \), \( k_2 \) and \( N/2 \), so as to determine the value of the number of output groups.

5. Experiment and data analysis

In order to verify the effectiveness of the optimized digital phase-locked frequency multiplication and subdivision method, we use the dynamic subdivision circuit of the FPGA chip to verify the experimental design. The FPGA development board chooses ALTERA's DE2-115 to implement the error compensation algorithm.

In this article, we choose the traditional digital phase-locked frequency multiplication method as the reference object. Set the experimental conditions as \( N = 16 \), \( f_i = 0.5MHz \), \( f_{ch} = 200MHz \), and use the traditional digital phase-locked frequency multiplication subdivision algorithm and the optimized digital phase-locked frequency multiplication subdivision algorithm in the dynamic subdivision circuit. The experimental parameters are shown in the following table:

| Table 1 | Comparison of algorithm parameters before and after optimization |
|---------|---------------------------------------------------------------|
| Function parameter | Traditional phase-locked subdivision | Optimize phase-lock subdivision |
| Maximum input frequency \((f_{max}/MHz)\) | 0.58 | 0.92 |
| Maximum input frequency change rate \((df_{max}/MHz:s^{-1})\) | 0 | 3230 |
| Loop locking time \((ns)\) | 28446 | 10 |
| LE | 75 | 463 |

From the analysis of the table data, it can be seen that the traditional digital phase-locked frequency multiplication and subdivision method can only subdivide the signal frequency within the fluctuation range of the center frequency. In the optimized digital phase-locked frequency multiplication and
subdivision method, when $f_i = 0.5 \text{MHz}$, $\max = 3032 \text{MHz} / s$, and the output delay only needs 10ns. It can be seen that the optimized digital phase-locked frequency multiplication has the characteristics of high frequency adaptability, high calculation efficiency, and high signal output accuracy. In terms of hardware resource occupancy, the optimized logic algorithm occupies less resources and performs more efficiently.

6. Conclusion

This paper proposes an optimized digital phase-locked subdivision method, and analyzes the effect of the decimal frequency division algorithm on system error reduction. A digital phase-locked subdivision circuit based on FPGA is proposed to optimize the circuit design of the flip-book solving module. The experimental results can show that the improved digital phase-locked frequency multiplication and subdivision method can subdivide the moiré grating signals in different frequency states. Compared with the traditional digital phase-locked frequency multiplication and subdivision method, the improved digital lock The phase doubling frequency subdivision method has a significant improvement in accuracy and computational efficiency in terms of realizing the signal subdivision function.

Acknowledgments

This research was funded by the Major National Scientific Instrument and Equipment Development Project of China (Grant NO. 2017YFF0105304) and the Key Research and Development Project of Science and Technology Development Plan of Jilin Provincial of China (NO. 20200401117GX).

Reference

[1] HUANG Y, XUE Z, QIAO D. Study on the performance of self-calibration angle encoder [C]. Proceedings of the SPIE, 2016, 9684:96840.
[2] CHEN G. Improving the angle measurement accuracy of circular grating [J]. Review of Scientific Instruments, 2020, 91(6):065108.
[3] GUO R, LUO F Y, YOU Y P. Interpolation method of frequency-discrimination Moiré fringe [J]. Modern Electronics Technique, 2013, 36(1):99-101+104.
[4] Warner M, Krabbendam V, Schumacher G. Adaptive periodic error correction for Heidenhain tape encoders[J]. Proceedings of SPIE, 2008, 7012: 70123N.
[5] Feng Yingqiao, Wan Qiuhua, Sun Ying, Yang Shouwang, Zhao Changhai. The interpolation error correction of the photoelectric signal of approximate triangular wave Moire fringe[J]. Acta Optica Sinica, 2013, 33(08): 114-118.
[6] CHEN G. Improving the angle measurement accuracy of circular grating [J]. Review of Scientific Instruments, 2020, 91(6):065108.
[7] GUO Y M, CUI J L, LIU X Y, et al. Interpolation method of phase-locking Moire fringe [J]. Journal of Harbin Institute of Technology, 2007, 39(9): 1496-1498.