Low-Resolution Horizontal and Vertical Layered Mutual Information Maximizing LDPC Decoding

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Abstract—We investigate iterative low-resolution message-passing algorithms for quasi-cyclic LDPC codes with horizontal and vertical layered schedules. Coarse quantization and layered scheduling are highly relevant for hardware implementations to reduce the bit width of messages and the number of decoding iterations. As a novelty, this paper compares the two scheduling variants in combination with mutual information maximizing compression operations in variable and check nodes. We evaluate the complexity and error rate performance for various configurations. Dedicated hardware architectures for regular quasi-cyclic LDPC decoders are derived on a conceptual level. The hardware-resource estimates confirm that most of the complexity lies within the routing network operations. Our simulations reveal similar error rate performance for both layered schedules but a slightly lower average iteration count for the horizontal decoder.

I. INTRODUCTION

Mutual information maximizing low-density parity-check (LDPC) decoders have recently been shown to outperform conventional algorithms when using coarse resolutions for the messages exchanged between variable and check nodes [1]–[3]. Yet, only a few works address decoding with a layered schedule [4]–[6], which is of great practical relevance as it can halve the number of required decoding iterations compared to the flooding scheme [7], [8]. In particular we are not aware of results on comparing horizontal and vertical scheduling in combination with mutual information maximizing decoders.

The horizontal scheme defines layers of check nodes that are fully updated, as shown in Fig. 1 [7]. Between the layer updates, all variable nodes are partially updated, improving the reliability information for the next layers within one iteration. In contrast, the vertical scheme defines layers of variable nodes that are fully updated, as shown in Fig. 1 [8]. Between the layer updates, all check nodes are partially updated.

This work investigates the two scheduling methods where compression operations are performed in each update under preservation of relevant information. The compression aims at reducing the message passing complexity and the memory footprint for caching messages between iterations.

In mutual information maximizing decoding several implementations for the node updates exist [4]. In this work we restrict ourselves to two-input operations that can be realized with standard components such as adders or comparators. In [2] a variable node with small single-input reconstruction tables, adders and non-uniform threshold quantization was shown to maximize the mutual information within a single node update. It was revealed in [9] that restriction to uniform quantization allows significant complexity savings at nearly no performance loss. For the check node, solutions with non-uniform and uniform threshold quantization exist as well [2], [9]. Another check node implementation with slightly reduced performance but further complexity savings is the minimum approximation update [9], [10]. The performance loss can be reduced when performing a check node aware variable node design as proposed in [11].

The paper is organized as follows. Section II describes the design of mutual information maximizing horizontal and vertical layered decoding. In section III the complexity for routing network and node update implementations are discussed. Section IV evaluates the error rate performance.

II. DESIGN OF QUANTIZED LAYERED DECODING

An LDPC encoder maps the information bits \( u \in \{0, 1\}^K \) to code bits \( b \in \{0, 1\}^N \) satisfying \( Hb = 0 \) where the parity check matrix \( H \in \{0, 1\}^{M \times N} \) defines \( M \) parity checks. Throughout the paper we assume a symmetrically quantized additive-white Gaussian noise (AWGN) channel with binary phase shift keying (BPSK) modulation. The quantization is designed to maximize the mutual information between the code bits \( b \) and the \( w_{c,h} \)-bit channel messages \( t^{ch} \in \mathbb{F}_{2^c}^N \) [1].

All quantized messages use a symmetric sign-magnitude alphabet \( \mathbb{T}_c = \{-2^{t-1}, \ldots, -1, +1, \ldots, +2^{t-1}\} \), whose elements are sorted by the underlying log-likelihood ratio (LLR) \( L(b|t) = \log p(b=0|t)/p(b=1|t) \). In the decoder we perform...
iterative message passing between variable and check nodes
over a routing network. To avoid routing congestion many
applications make use of quasi-cyclic (QC) LDPC codes
with a structured parity check matrix shown in Fig. 1. The
parity check matrix is fully defined by its base matrix
H \in \{-1, \ldots, Z\}^{N/Z \times M/Z} with lifting size Z: The lifting
procedure replaces each element h_{ij} with a cyclically shifted
identity matrix I(h_{ij}) \in \{0, 1\}^{Z \times Z} if h_{ij} \geq 0 and by a zero
matrix 0 \in \{0\}^{Z \times Z} if h_{ij} = -1 [4]. In this paper we restrict
ourselves to regular LDPC codes with h_{ij} \geq 0 where N/Z
and M/Z equal the check and variable node degrees d_c
and d_v. The structure can be exploited to define horizontal or
vertical layers, as highlighted in Fig. 1 where d_v = 2 and d_c = 3.
Next, the design of horizontal or vertical decoders is described,
where we use discrete density evolution to track probability
distributions of messages [1].

A. Horizontal Layered Decoding

One iteration in horizontal (or row-) layered decoding is
characterized by d_v layer updates. For each layer l \in L = \{0, \ldots, d_v - 1\}
we perform Z full check node and N
partial variable node updates. Fig. 2 depicts a single unrolled
iteration of the decoding procedure.

1) Full Check Node Updates: We denote the set of variable
nodes adjacent to check node \( z \in \{0, \ldots, Z - 1\} \) in layer l as

\[ V_{l,z} = \{ iZ + (z + h_{il} \mod Z) \} : i \in \{0, \ldots, d_c - 1\} \].

Each check node obtains extrinsic information for the variables
through the parity check equation \( b_n = \bigoplus_{i \in V_{l,z} \setminus \{n\}} b_{n_i} \).
For each connected variable node \( n \in V_{l,z} \), the mutual
information maximizing check node update yields a w-bit output message
\( t_{l,n}^c = Q^c(y_{l,n}^c) \in T_w \) with

\[ y_{l,n}^c = \prod_{n_i \in V_{l,z} \setminus \{n\}} \text{sgn}(t_{l,n_i}^v) \sum_{n_i \in V_{l,z} \setminus \{n\}} |\phi_c(t_{l,n_i}^v)|, \quad (1) \]

In (1), \( |\phi_c(t_l^v)| = \log \tanh L(b_l | t_l^v) \) is a reconstruction function,
implemented by a small lookup table [2], [9]. The threshold
quantization \( Q^c \) poses as an information bottleneck (IB) setup
where \( y_{l,n}^c, b_n \) and \( t_{l,n}^c \) are considered as the realizations of the
observed, relevant and compressed random variables, Y_l, B and T_l,
respectively, with the objective \( \max_{Q^c} I(B; T_l) \) [1].
Significant complexity can be saved by making uniform quantization
as proposed in [9]. Alternatively, the minimum approximation update [4] yields

\[ t_{l,n}^c = \prod_{n_i \in V_{l,z} \setminus \{n\}} \text{sgn}(t_{l,n_i}^v) \min_{n_i \in V_{l,z} \setminus \{n\}} |t_{l,n_i}^v|, \quad (2) \]

2) Partial Variable Node Update: For \( n \in \{0, \ldots, N - 1\} \) the
mutual information maximizing partial variable node update in
layer l yields a w-bit output message \( t_{l+1,n}^v = Q^v(y_{l+1,n}^v) \in T_w \) with
iterative or recursive computation

\[ y_{l+1,n}^v = \phi_v(t_{l,n}^v) + \sum_{l \in C \setminus \{l+1\}} \phi_c(t_{l,n}^c) + L(b_n), \quad (3) \]

In (3), \( \phi_v(t_{l,n}^v) = L(t|b_n) = \log p(t|b=0)/p(t|b=1) \) is a reconstruction
function that can be implemented by small lookup tables and
\( L(b_n) = \log p(b_n=0/b_n=1) \) is the a priori LLR.
Note, that the index (de)increment \( l+1 \) is modulo \( |L| \).
For the recursive update, we initialize \( y_{0,n}^v = \phi_v(t_{0,n}^v) \) in the first
decoder iteration. Again, the non-uniform threshold quantization
\( Q^v \) poses as an IB setup. A layer-specific design with
low-complexity uniform threshold quantization is restricted to the
iterative computation in (3) which allows rescaling
of \( y^v \) [9]. As shown in [11] for the flooding schedule, a check node
aware design of \( Q^v \) may improve the performance also for
the horizontal schedule.

B. Vertical Layered Decoding

One iteration in vertical (or column-) layered decoding is
characterized by \( d_c \) layer updates. For each layer \( l \in L = \{0, \ldots, d_c - 1\} \) we perform M
partial check node and Z full variable node updates. Fig. 4 depicts
a single unrolled iteration of the decoding procedure. In the first iteration we perform updates according to the flooding schedule with full
check and variable node updates.

1) Partial Check Node Updates: For \( m \in \{0, \ldots, M - 1\} \) the
mutual information maximizing partial check node update in
layer l yields a w-bit output message \( t_{l,m}^c = Q^c(y_{l,m}^c) \in T_w \) with
iterative or recursive computation

\[ y_{l,m}^c = \prod_{l \in C \setminus \{l\}} \text{sgn}(t_{l,m}^v) \sum_{l \in C \setminus \{l\}} |\phi_c(t_{l,m}^v)| \]

Equation (5) can be implemented with good accuracy using
the three-minimum approximation proposed in [12].

2) Full Variable Node Update: We denote the set of check
nodes adjacent to variable node \( z \in \{0, \ldots, Z - 1\} \) in layer l as

\[ C_{l,z} = \{ iZ + (z - h_{zl} \mod Z) \} : i \in \{0, \ldots, d_v - 1\} \].

For each connected check node \( m \in C_{l,z} \), the mutual
information maximizing variable node update yields a w-bit output message
\( t_{l,m}^v = Q^v(y_{l,m}^v) \in T_w \) with

\[ y_{l,m}^v = \phi_v(t_{l,z+1,m}^c) + \sum_{m_i \in C_{l,z} \setminus \{m\}} \phi_c(t_{l,m_i}^c) + L(b_{z+1}), \quad (6) \]

III. COMPLEXITY ANALYSIS

A. Routing Network Complexity

For hardware implementations, the unrolled horizontal and
vertical decoding graphs in Fig. 2 and Fig. 4 can be reorganized
to avoid routing congestion. In case of the horizontal schedule, Fig. 3a places the variable and check nodes such that only parallel wires occur. The long parallel wires can be avoided by making use of the third dimension. In Fig. 3b,
of the partial variable node update (3). The APP message passing is more efficient if the bit width of $y^v_i$ is smaller than the combined bit width of $t^v_i$ and $t^v_{i+1}$. The horizontal APP unrolled decoding graph is depicted in Fig. 6a. The variable and check node units are located closely without intermediate shifter as shown in Fig. 6b. Thus, using the minimum approximation allows to save memory by reconstructing $t^v_{i+1}$ from the first and second minimum (+index) of the previous iteration. Instead of storing $d_v(w−1)$ bits we only have $\lceil\log_2(d_v)\rceil+2(w−1)$ bits for the magnitudes. From (4) we also can derive a modified APP message passing for the vertical schedule, but without further memory savings.

C. Node Update Complexity

Several options exist to implement the full and partial node update under a horizontal and vertical schedule. Table II gives an overview about the options for check node (CN) and variable node (VN). The update with non-uniform quantization was shown to achieve highest mutual information
...iteration-dependent reconstruction complexity. The 6-bit reconstructions entail 7-bit adder units leading to 8-bit APP (MIM) decoders.

The last column counts the usage of reconstruction functions $\phi^c$ and $\phi^v$ which translate a $w$-bit message to a higher resolution $w'$-bit representation value. Note, that in uniform quantization [9] the translation involves a scaling, such that the quantization can be achieved with a clipping and bit shifting operation. Thus, no comparisons or memory for storing the thresholds are required as in non-uniform quantization. One disadvantage of the uniform approach is that for every partial update all extrinsic inputs have to be rescaled and processed which is not very practical for high node degrees. The authors of [14] observed that enforcing non-varying translation tables among consecutive layer updates causes only minor degradation. In a similar way the rescaling issue might be relaxed also for the uniform quantization. In the following we focus on low-complexity configurations.

D. Decoder Complexity

Next, we aim to estimate the overall decoder resources including node computations, message transfers and memory demand for various practical mutual information maximizing (MIM) decoders.

Fig. 6: APP message passing.

TABLE II: Node complexity depending on check node degree $d_c$, variable node $d_v$ and exchanged message resolution $w$.

| node type     | additions | comparisons | translations |
|---------------|-----------|-------------|--------------|
| full          | CN        | VN          |              |
| non-uniform [2] | $2d_c - 2$ | $d_v(w - 1)$ | $d_v$        |
| uniform [9]   | $2d_c - 2$ | 0           | $d_v - 2$    |
| min [10]      | 0         | $d_v + \log_2(d_c) - 2$ | 0            |
| partial       | CN        | VN          |              |
| non-uniform [2] | $2d_v - 1$ | $d_v(w - 1)$ | $d_v + 1$    |
| 3-min [12]    | $d_v - 1$ | 0           | $d_v - 2$    |
| uniform       | $d_v - 1$ | 0           | 0            |

TABLE III: Gate count per addition/comparison [15].

| Decoder label | CN ops. [gates] | VN ops. [gates] | Network Total [gates] | Memory [bits] |
|---------------|-----------------|-----------------|-----------------------|---------------|
| MIM-H         | 11.2            | > 70            | 240                   | 321           |
| MIM-HA        | 30              | 58.3            | 180                   | 268           |
| MIM-V         | 11.2            | 58.3            | 180                   | 250           |
| OMSQ-H        | 18.5            | 60              | 230                   | 319           |
| OMSQ-HA       | 45              | 50              | 240                   | 335           |
| OMSQ-V        | 18.5            | 50              | 240                   | 309           |

TABLE IV: Decoder complexity per edge in one iteration.

1) Configurations: For the horizontal layered decoder MIM-H we use a full check node update with minimum approximation and the partial variable node with uniform quantization. The decoder MIM-HA uses the APP message-passing schedule. For the vertical decoder MIM-V we select the partial check node update with 3-minimum approximation [12] and full variable node with uniform quantization [9]. The flooding decoder MIM-F performs full updates for check and variable nodes. As a benchmark we consider the quantized offset-min-sum algorithm (OMSQ) decoder for flooding, horizontal-standard, horizontal-APP and vertical schedule [8]. The check node uses a slightly more complex minimum approximation with offset operation.

The complexity for the addition and comparisons reported in Table III assumes a $k$-bit ripple-carry adder with $5$ gates for each of the $k$ full-adders. This adder can be considered as a lower bound with minimum area but high delay [15].

The MIM decoders use $w$-3-bit messages and $w'$=6-bit reconstructions. For the OMSQ decoder we consider $w$=4 bits. In the complexity analysis and simulations we use a high rate code with $Z=512$, $d_v=3$ and $d_c=18$ [4]:

$$H = \begin{bmatrix} 0 & 0 & 1 & 0 & 1 & \cdots & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 & 0 & \cdots & 1 & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots & \vdots & \vdots \\ 1 & 0 & 0 & 0 & 0 & \cdots & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & \cdots & 0 & 0 & 0 \\ \end{bmatrix}$$

(7)

2) Evaluation: In Table IV the highest gate counts are related to the barrel-shifting routing network, which confirms that LDPC decoding is a data transfer dominated application, raising demand for low-resolutions.

The OMSQ decoders require $w$=4-bit messages since the representation levels cannot change across the iterations. But, the constant 4-bit levels also lead to $\log_2(d_c 2^w)$=6-bit APP messages in the variable nodes. Therefore, under an APP message passing schedule, only 6 bits for OMSQ-HA instead of 2-4 bits for OMSQ-H must be transferred.

The MIM decoders focus on reducing the resolution of messages under standard message passing. The reconstruction operation enables iteration-specific representation levels for the variable node update. Every reconstruction table consists of $2^{w-1}$ $w'-1$-bit values under a symmetric sign-magnitude format [9]. It can be observed in [11] that only the high reliable magnitude level involve a non-linear translation. To keep the Table IV less complicated, we have not included the iteration-dependent reconstruction complexity. The 6-bit reconstructions entail 7-bit adder units leading to 8-bit APP...
messages. Therefore, we have a larger routing network for MIM-HA compared to MIM-H. Further, the uniform quantization with bit shifting involves a rescaling of the APP message. On the other hand, APP message passing reduces the memory demand from 2 to 1.5 bits, as discussed in section III-B.

In the MIM-V decoder the uniform quantization is more efficient when fully updating the variable nodes. It avoids additional translations for internal rescaling of all extrinsic inputs that would be required in every partial update [9]. Moreover, all check node messages can use the same reconstruction table. On the other hand, the 3-min check node updates are more complex. The flooding decoders have the lowest node complexity by relying only on full node updates, however, they require twice the number of iterations compared to layered decoders [4].

IV. PERFORMANCE INVESTIGATION

In Fig. 7 we evaluate the bit error rate performance for the high-rate \( R = 5/6 \) QC LDPC code (7) with a maximum of 10 iterations including results for high-resolution belief propagation (BP). Compared to 4-bit OMSQ-H, we observe gains of 0.1 dB in case of 4-bit, 0.04 dB for 3-bit and a degradation of 0.16 dB for 2-bit MIM decoding. The horizontal and vertical decoder lead to very similar performance. In Fig. 8, the vertical schedule requires 14% more average decoding iterations (under early termination with the APP hard decision) compared to the 4-bit horizontal MIM decoder. Reducing the resolution from \( w = 3 \) to 2 bits increases the average iteration count by 40% at \( E_b/N_0 = 4.0 \text{ dB} \), as highlighted. However, this is compensated with a smaller routing network which involves only 120 instead of 180 gates (Table IV).

V. CONCLUSIONS

We compared horizontal and vertical layered decoding with mutual information maximizing node updates for regular quasi-cyclic LDPC codes. A complexity analysis revealed that barrel shifting constitutes a major part of the decoder. Decreasing bit width reduces shifting complexity but increases the average iteration count. Our results suggest less complexity for horizontal scheduling since we observed fewer average iterations. However, the schedule selection may depend on other important characteristics, like achievable clock frequency, required chip area or energy consumption. The evaluation of those metrics demands hardware implementations.

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