Electron transport of WS$_2$ transistors in a hexagonal boron nitride dielectric environment

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We present the first study of the intrinsic electrical properties of WS$_2$ transistors fabricated with two different dielectric environments WS$_2$ on SiO$_2$ and WS$_2$ on h-BN/SiO$_2$, respectively. A comparative analysis of the electrical characteristics of multiple transistors fabricated from natural and synthetic WS$_2$ with various thicknesses from single- up to four-layers and over a wide temperature range from 300 K down to 4.2 K shows that disorder intrinsic to WS$_2$ is currently the limiting factor of the electrical properties of this material. These results shed light on the role played by extrinsic factors such as charge traps in the oxide dielectric thought to be the cause for the commonly observed small values of charge carrier mobility in transition metal dichalcogenides.

The emerging class of atomically thin semiconducting materials formed by transition metal dichalcogenides (TMDCs) is showing a plethora of complementary properties to those of graphene that are of interest to fundamental and applied research. These materials are uniquely suited to study the superconducting phase transition in the extreme two-dimensional limit inherent to atomically thin systems. At the same time TMDCs have a band gap which is essential for transistor applications and which could enable a new class of atomically thin photo-transistors. For example WS$_2$ has a direct band gap of 2 eV in single layer form and has already shown great promise as a flexible transistor with field effect mobilities comparable to the best liquid crystals and on/off ratio of the current exceeding $10^6$. Understanding the limiting factors of the electrical properties of TMDCs is an open quest and a stepping stone for accessing novel physics in these systems.

The typical values of charge carrier mobility measured in thin WS$_2$ flakes are always much lower than those measured in bulk material. This behaviour has been interpreted as due to defect states in the SiO$_2$ substrate leading to the localization of charge carriers in TMDCs and a small charge carrier mobility. To probe the intrinsic electrical properties of TMDCs it would be necessary to measure electrical transport in either suspended structures or in transistors fabricated on clean substrates with fewer impurities than typically present in SiO$_2$. An ideal choice for such a substrate is hexagonal boron nitride, which is a preferred substrate for high quality graphene transistors since it has a very low concentration of charge scattering impurities and is atomically flat. To date such a study has not yet been conducted and the consequent lack of knowledge is limiting the potential impact of TMDCs on fundamental and applied research. Furthermore most of the studies conducted so far have been limited to just MoS$_2$, while other TMDCs such as WS$_2$ have not yet received much attention, whereas they might be better suited than MoS$_2$ for a given application.

Here we present the first study of the electrical properties in WS$_2$ transistors fabricated on different dielectrics (i.e. SiO$_2$ and h-BN/SiO$_2$) and using synthetic as well as natural WS$_2$. The comparative analysis of the electrical characteristics of these transistors studied in the temperature range from 300 K down to 4.2 K shows that in all cases electrical transport takes place via hopping conduction through localized states. At low temperature ($T < 20$ K) we observe peaks of the conductance as a function of back-gate voltage and source-drain bias due to inelastic tunnelling in the impurity states with sub-gap energy. These results show that intrinsic disorder rather than extrinsic factors such as defect states in the oxide dielectric is limiting the electrical properties of WS$_2$ and more generally TMDCs.
Results

Thin flakes of WS₂ were obtained by mechanical exfoliation of flakes from synthetic crystals onto p-doped Si/SiO₂ substrate that serves as a back gate (for natural WS₂ see supporting information). Thin flakes are first identified with the aid of optical microscopy and their thickness is subsequently determined by atomic force microscopy (AFM) and Raman spectroscopy. The fabrication of WS₂ transistors on h-BN and subsequent encapsulation in h-BN are first identified with the aid of optical microscopy and their thickness is independently measured with AFM, see Fig. 1e. Finally, upon increasing the number of WS₂ layers the position of the 2LAM and E₁²g(Γ) peaks redshift monotonically, whereas the A₁g(Γ) peak blue shifts as previously shown, see Figure 1f.

Having established a reliable procedure to identify the layer number of WS₂ flakes we now turn to investigate the electrical transport properties of this material. The source-drain current vs. bias voltage characteristics (I-V) of WS₂ transistor devices are always highly nonlinear and upon performing current-bias annealing, a linear I-V around zero voltage bias is attained (see Figure 2a and supplementary information). Owing to the difference in work function between WS₂ and Cr, a Schottky barrier of about 100 meV has to be expected at this interface when no-gate voltage is applied. The observed bias-annealing changes in the I-V and the large values of voltage bias at

![Figure 1](https://example.com/figure1.png)

**Figure 1** (a) shows an AFM measurement of a bilayer WS₂, the scale bar corresponds to 500 nm. The dashed areas labeled by A and B enclose the step edge at the SiO₂-bilayer WS₂ and the fold in the WS₂ flake respectively. The corresponding histograms of the measured heights in A and B are shown in (b). (c) shows the evolution of the shape and position of the Raman peaks of WS₂ as the number of layers is increased from single layer to bulk. (d) is a plot of the Raman spectra for bulk WS₂ and a fit to three Lorentzians corresponding to the 2LAM(M) and A₁g(Γ) peaks, see main text. (e) shows the measured wavenumber shift (Δν) between 2LAM(M) and A₁g(Γ) plotted for 30 flakes with different layer number. (f) summarizes the measured Raman shift for 2LAM(M), E₁²g(Γ) and A₁g(Γ) as a function of layer number.
after bias-annealing. A large voltage bias as shown in Figure 2a. In the following we only consider the analysis of electrical transport measurements in devices after bias-annealing.

Figure 2(b–d) show the room temperature field effect transistor (FET) transfer characteristics, that is the gate voltage (V_g) dependence of the conductivity (σ), for monolayer WS_2 on SiO_2 (Figure 2b), four-layer WS_2 sample on a SiO_2 (Figure 2c) and four-layer WS_2 sample on a h-BN/SiO_2 (Figure 2d). In all cases we observe that the conductivity has a large on-off ratio typical of semiconducting materials, with a finite threshold voltage. However we find that the field effect mobility (μ) is always larger in WS_2 on h-BN than in WS_2 on SiO_2 (0.23 cm^2 V^-1 s^-1) for 1L-WS_2/SiO_2, 17 cm^2 V^-1 s^-1 for 4L-WS_2/SiO_2 and ~80 cm^2 V^-1 s^-1 for 4L-WS_2/h-BN/SiO_2 in Figure 2(b–d)). A large hysteresis is also present in σ(V_g) for WS_2 on SiO_2 but is fully suppressed when WS_2 is on h-BN/SiO_2. Similar hysteresis in I-V have also been reported in graphene and is commonly attributed to dopants present in the SiO_2 dielectric.

Discussion

For all the measured devices we find that the temperature dependence of σ(V_g) shows a pronounced suppression of the value of σ upon lowering the temperature as expected for a semiconducting material, see Figure 3a. In these devices we apply a large enough value of gate voltage such that the charge carriers are directly injected from the metal contacts into the conduction band of WS_2. In this limit the relevant energy scale dominating the temperature dependence of the zero-bias resistance is the difference between the Fermi energy and the conduction band edge of the n-doped semiconductor (i.e. WS_2). A plot of σ as a function of T^-1 at V_g = 60.5 V reveals that from 260 K down to 100 K the conduction takes place by thermally activated charge carriers, i.e. σ(T) = σ_0 exp(-E_a/2k_B T) with E_a the activation energy and k_B the Boltzman constant. The values of E_a estimated from a fit of σ(T) for 50 V < V_g < 60 V are in the range 0.109 eV < E_a < 0.113 eV and change linearly with V_g, see inset in Figure 3b. These values of δE are compatible with the voltage bias range over which non-linear 1-V are measured (see blue curve in Figure 2a) suggesting that δE is the energy from the Fermi level to the conduction band edge (E_c), i.e. δE = E_c - E_F which is also much larger than the Schottky barrier height (∼100 meV).

The smooth dependence of δE on V_g demonstrates that for sub-gap energies the Fermi level can be continuously tuned by means of a gate voltage throughout the defect induced states. To estimate the density of defect states we consider the equivalent gate capacitance of these WS_2 transistors that is the series of the gate oxide capacitance (C_{ox}) and defect states capacitance (C_d), i.e. -dE/dV_g = 1.5 × 10^{-4} e V = C_{ox}/C_d. Knowing that the oxide capacitance per unit area is C_{ox} = 0.12 μF cm^-2 = 1.2 × 10^{-4} Fm^-2 we find C_d = 0.8 Fm^-2 = qD(E), where q is the unit of charge and D(E) is the density of defect states which we estimate to be 3.12 × 10^{19} J^-1 m^-3.

The dominant role of disorder induced states with sub-gap energies becomes fully apparent when considering a fit of the low temperature σ(T) in logarithmic scale in terms of T^-p with p critical exponent, see Figure 3c. This study reveals that p = 1/3 gives the best fit stemming for non-interacting Mott variable range hopping (11,14,19) σ = σ_0 exp(-T_0/T)^{1/3} where T_0 is the hopping parameter and is related to the density of localised states existing within the forbidden gap and the electron wavefunction size ξ by the following relation T_0 = 13.8/k_B D(E)_ξ^{1/3}. The extracted values for the hopping parameter T_0 at each different gate voltage are plotted in Figure 3(d) along with the conductance at T = 4.2 K. This comparative plot shows a clear correlation between the hopping parameter and the conductance whereby peaks in conductance correspond to very low values of
T0. Furthermore T0 is found to fluctuate from \( <100 \text{ K} \) to \( <4000 \text{ K} \) in a small gate range (from \( V_g = 50.5 \text{ V} \) to 52 V, corresponding to an energy window of just 0.25 meV). Consequently the estimated localization radius in WS2 increases from 1.8 nm to 17 nm. These observations indicate that the sub-gap impurities states have peaks of narrow energy band-widths dominating electrical transport for sub-gap energies.

Another prominent feature evident in the temperature dependence of \( s(V_g) \) is the emergence of peaks for \( T, <100 \text{ K} \) with decreasing amplitude for \( T, >20 \text{ K} \), see Figure 3a. At the same time the differential conductance as a function of source-drain bias and gate voltage at \( T = 4.2 \text{ K} \) (Figure 4a) shows that these peaks shift their position as a function of voltage bias. These observations suggest that charge transport at sub-gap energies occurs through inhomogeneous charge puddles and localized states in WS2. Since we observe a similar \( s(V_g) \) behaviour in a variety of samples independently of (1) the WS2 flakes aspect ratio, (2) the WS2 layer number and (3) the dielectric environment (WS2/BN/SiO2, see supplementary information) we conclude that the localized states dominating electrical transport in WS2 at sub-gap energies are intrinsic to the WS2 and not extrinsic such as defect states in the dielectric.

To estimate the localization radius (\( \xi \)) we consider electrical transport measurements of a representative 4L-WS2 in which the peaks of \( \sigma(V_g) \) are spaced by an average gate voltage \( \langle V_g \rangle \approx 1.13 \text{ V} \) corresponding to 0.17 meV, see bottom graph in Figure 4. In this device the peaks of \( \sigma \) at fixed \( V_g \) as a function of source-drain bias (V) are spaced by an \( \langle V \rangle \approx 11 \text{ mV} \), which for a channel length of 350 nm corresponds to a threshold electric field \( E_T = 3.14 \times 10^4 \text{ V/m} \). This value of \( E_T \) together with the observed average peak separation of 0.17 meV gives a localization region of diameter \( 2\xi = 5.4 \text{ nm} \) which is consistent with the extracted value of the localization radius \( \xi \) from the analysis conducted on the temperature dependence of \( \sigma(V_g) \).

**Figure 3** | (a) shows a representative plot of \( s(V_g) \) for a 4L-WS2 in the gate range 50 V to 65 V. (b) Typical temperature dependence of the conductivity plotted in terms of the activation energy relation (this curve is taken at \( V_g = 60.5 \text{ V} \)). The inset is a plot of the extracted activation energy for different gate voltages, each point corresponds to an average over 0.2 V gate voltage. (c) shows the same data as in (b) but plotted in terms of 2D Mott variable range hopping relation. (d) The conductivity at 4.2 K plotted alongside the hopping parameter \( T_0 \). A strong correlation between the two is observed: i.e. peaks in conductance correspond to low values of \( T_0 \).

\( T_0 \) is found to fluctuate from \( \approx100 \text{ K} \) to \( \approx4000 \text{ K} \) in a small gate range (from \( V_g = 50.5 \text{ V} \) to 52 V, corresponding to an energy window of just 0.25 meV). Consequently the estimated localization radius in WS2 increases from 1.8 nm to 17 nm. These observations indicate that the sub-gap impurities states have peaks of narrow energy band-widths dominating electrical transport for sub-gap energies.

**Figure 4** | The top colour map shows the measured differential conductance plotted against gate voltage and source drain at \( T = 4.2 \text{ K} \) for the same representative 4L-WS2 on h-BN discussed in Figure 3. The bottom plot is a graph of the conductivity at \( T = 4.2 \text{ K} \) while the inset is a graph of five differential conductance curves plotted from \( V_g = 61.52 \text{ V} \) up to 62 V highlighted by the dashed lines A and B respectively and in steps of 96 mV of gate voltage.
Finally we note that Coulomb blockade cannot account for the observed peaks of $\sigma(V_g)$. Indeed, if we assume a charging energy in our devices of $E_c \sim 40$–50 meV estimated directly from the stability diagram shown in Figure 4, we extract a diameter $d \sim e^{2}/4\kappa_{\text{eff}}E_c \sim 20$–40 nm for the confining regions ($\kappa = 1.610^{-13} \text{C}, \kappa_\text{eff} = 8.8510^{-13} \text{F/m}$ and $\kappa_* = (\kappa_{\text{vac}} + \kappa_{\text{BN}})/2 = 2.5$ with the dielectric constant for vacuum and BN $\kappa_{\text{vac}} = 1$ and $\kappa_{\text{BN}} = 4$). Given the dimensions of the conductive WS$_2$ channel, our devices would consist of 100–1000 charging regions (i.e. length $\times$ width)/$d = (350 \text{ nm} \times 1500 \text{ nm})/d$). The stability diagram of such an array of charging islands would consist of many overlapping Coulomb diamonds which are not observed in our measurements. An indication of the underlying physical process originating these peaks of $\sigma(V_g)$ is given by the temperature dependence of $\sigma(V_g)$ presented in Figure 3a: we always observe that the amplitude of the peaks decreases upon lowering the temperature. This behaviour has been previously reported in other semiconducting systems and it is a fingerprint of inelastic tunnelling which in WS$_2$ occurs through the sub-gap impurity states. In summary we have presented the first systematic study of the intrinsic electrical properties of thin WS$_2$ flakes. By comparing the $I$–$V_g$ of transistors fabricated using two different dielectric environments (i.e. (1) WS$_2$ on SiO$_2$ and (2) WS$_2$ on h-BN/SiO$_2$) we find that hopping through localized states dominate electrical transport over a wide temperature range ($T < 100 \text{ K}$). This intrinsic disorder has a finite density of states at sub-gap energies which contribute with inelastic tunnelling to electrical transport. These results demonstrate the dominant role played by intrinsic disorder over extrinsic factors such as defect states in the oxide dielectric as a limiting factor of the electrical properties of WS$_2$.

**Methods**

**Materials.** Synthetic WS$_2$ was purchased from Lowerfriction.com.

**Measurement techniques.** The Raman spectra where measured with a Renishaw spectrometer using an excitation laser with a wavelength of 532 nm, focused to a spot size of 1.5 μm diameter and 1 mW incident power. These measurements were performed in air and at room temperature.

**Electrical measurements.** The electrical transport measurements were performed in constant voltage configuration with excitation voltage smaller than $k_B T$, with $k_B$ Boltzmann constant. The differential conductance was measured using the lock-in technique.

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