A Novel Coplanar Based Adder Logic Design Using QCA

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Abstract. Now a days, VLSI is a one of the top most technology are used in the field of electronics communication. It is used to create an integrated circuit by merging million of MOS transistor into a single chip. In VLSI, most of the transistors are design in micro scale level. Now a days people will want all materials are in compact size. So, it is necessary to design a circuit in nanoscale level. In the field of VLSI, CMOS technologies are used for designing a integrated circuit (IC) chips. But in CMOS, size that are used to designing a circuit is in micro scale level. So researcher is introducing new nanotechnology that new technology is called QCA technology. Logic function gate is a one of the fundamental components to design an any circuit in electronics communication. In this paper, novel coplanar approach to designing an efficient QCA based 4-bit full adder using XOR/XNOR logic gate is proposed. QCA Designer Version 2.0.3 simulation tools are used in this proposed method. Performance is analysed and verified to determine the capabilities of proposed full adder.

1. Introduction
Adder has a major role in designing a digital circuit. It is not only to perform in arithmetic operations but it also performs in logical operation. Adder is a building block for designing a microprocessor and digital signal processing chips. A full adder means adding more than two bits. Recently, VLSI is one of the most used technology in the electronics communication field. It creates IC chips with million numbers of transistors. CMOS technologies are used to constructing integrated circuit in VLSI. But, a size that is used in CMOS technologies for designing a circuit is the microscale level.

Due to physical limits in CMOS technologies, they cannot able to extend their size up to nanoscale. To conquer this issue, researchers proposed new nanotechnology ideas. The new idea has proposed by recent time researchers named efficient Quantum-Dot Cellular Automata (QCA) which is new nanotechnology. QCA nanotechnology is a replaceable approach to CMOS technology with many additional features. Recently this technology becomes one of the top six emerging technologies. QCA is one of the concepts of novel digital technologies. This novel digital technology results in low energy consumption and excessive density. In QCA, binary information is not encoded as ‘0’ and ‘1’. But it encodes binary states as charge configuration. Binary state ‘0’ is representing by ‘+1’, which means positive charge configuration. Binary state ‘1’ is represented by ‘-1’, which means a negative charge configuration.
The fundamental elements of QCA are QCA cell or quantum cell. In each corner of the QCA cell, quantum dots are located. Totally 4 quantum dots in each QCA cell. Every quantum cell has two additional free electrons. When columbic repulsion takes place between the cells two electrons are placed in quantum cell diagonally opposite to each other. QCA cells have two possible polarization configuration each one will denote the binary state ‘0’ or ‘1’. Due to the columbic repulsion binary information can easily move from input to output of QCA cell.

This paper objective is to overcome the CMOS physical limits and design a QCA based coplanar QCA XOR/XNOR full adder circuits with minimum cost. To exhibit the functionality and capabilities of the proposed XOR logic gates and 4-bit full adder architecture, performance is evaluated and analysed.

2. Related work
Jadav Chandra Das, al., (2019) proposed a even parity checker based on QCA technology. It is a Error Detection Circuit for nanocommunication Network. Hamid Reza, al., (2019) proposed a Multilayer QCA RCA circuit. This RCA circuit has 0.17µm² area and 125 cells. Y.Adelinaet,al.,(2019) proposed a novel XOR gate. Proposed model are compatible with QCA gates within nanoscale for combinational circuit. Moslem Balali, al., (2018) developed an adder circuit using QCA nanotechnology. Created RCA circuit has 0.3µm² area and 209 cell counts and postponement of circuit is 1.23 number of clock cycles. ImanEdrisiArani, al., (2018) proposed a serial-parallel Multiplier in QCA nanotechnology. Multiplier circuit has 31 cells count and area of 0.03µm². The delay of this circuit is 0.5 cycles Marciano.et.al., (2016) proposed a clocking scheme USE. This clocking scheme is universal, scalable, efficient and easily manufacturable.

3. System implementation
In this paper, the proposed method introduce QCA based 4-bit full adder using an XOR gate. XOR/XNOR logic gates are preferred over other circuits because they reduce the complexity of the circuit. Why this paper used XOR gate for the implementation of the full adder? Because it is easy to calculate adder logic sum and carry. There are two types of wire crossing methods that are used in QCA nanotechnology. QCA cells are aligned properly and they do not interact with each other in the coplanar crossover wiring method. Coplanar crossover is preferred for designing a complex circuit in QCA nanotechnology. In developed circuit cell size has been reduced and the complexity also reduced. The designed full adder comprises a minimum number of logic gates, which minimize the latency and cell count.
The proposed schematic diagram for the XOR gate has appeared in Figure 3. In this diagram input contribution of the gate is A and B. P1, P2 are the polarisation inputs of the gate. Based on the enable input it either acts as an XOR gate or XNOR gate.

Mathematical expression of full adder is given by cell count.

\[
\text{Adder logic sum} = A'(B \oplus C) + A(B \oplus C)'
\]  

(1)

Adder logic sum is expressed with ex-or operation of all three inputs. And Adder logic carryout is expressed in terms of previous stages of inputs.

4. Simulation results & discussion

QCA designer version 2.0.3 simulation tools are used to implementing and simulating the proposed method. QCA designer is a powerful CAD capabilities tools. It allows the designer quickly to design a layout and simulate the circuit construct with ‘n’ number of QCA cells. Figure 5(a) and 5(b) demonstrate the XOR/XNOR logic gate simulation results.
Figure 5(a). Simulation result for XOR logic.

Figure 5(a) illustrates the simulation results of the output XOR gate logic function. The polarisation inputs (P1 P2) are ‘01’ in binary, and then it performs the XOR operation. Contribution to the logic gate XOR is applied and yield of the corresponding gate is checked. Similarly, if A=0 and B=1, then C=1 is the output. According to inputs A and B of the XOR gate, their corresponding output will be evaluated.

Figure 5(b). Simulation result for XNOR logic.

Figure 5(b) illustrates the special gate XNOR logic style and its simulated output for various input combination. The polarisation inputs (P1 P2) are ‘10’ in binary, and then it performs the XNOR operation. If inputs of XNOR are A=1 and B=0, then C=0 is the output. Similarly, if A=1 and B=1, then C=1 is the output. According to inputs A and B, their corresponding output will be evaluated. Figure 6 shows the input sequence of adder logic and figure 7 shows the output sequence of adder logic. There is a total of 32 inputs/outputs combination for 4-bit adder logic. The first sixteen inputs and their outputs are related to carry-in is low. The remaining sixteen inputs and their outputs are
related to carry-in is high. Adder logic sum has 4-bit. If carry-in is low, then the first 8 carry-out are low and the remaining 8 carry-out are high. If carry-in is high, then the first 8 carry-out are high and the remaining 8 carry-out are low. Adder logic outputs are simulated and verified for all possible inputs combination.

**Figure 6.** Input sequence of proposed full adder for 4-bit.

**Figure 7.** Output sequence of proposed 4-bit full adder.

**Table 1.** compare the parameters between existing and proposed method.

| Work            | Gate Count | Cell count | Area µm² | Latency (ns) |
|-----------------|------------|------------|----------|--------------|
| A. M. Chabi et al | 4          | 29         | 0.03     | 0.75         |
| S. Sheikhfaal et al | 3          | 32         | 0.25     | 1            |
5. Conclusion

This paper first designed for full adder addition for 1 bit and then the addition of 4 bits using the coplanar approach in QCA technology. The proposed adder logic requires 0.009µm² of space and has a delay of 0.5(ns). Adder logic designed with the help of QCA design requires less space in size compared to an existing method. Due to lower latency in the proposed method cell count is less. This work has been proved an efficient programmable circuit. Using this proposed XOR/XNOR logic gate, we will design more complex circuits in future.

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