Design of Low Voltage CMOS OTA Using Bulk-Driven Technique

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Abstract

Background/Objectives: The main objective was to design a CMOS Operational Transconductance Amplifier (OTA) for biomedical applications and high speed transmission with an operating voltage 0.4 V. Methods/Statistical Analysis: In this paper we have proposed an OTA using bulk driven technique. The transistors are working in weak-inversion. The design was simulated using conventional transistors. The technique employed was source degeneration technique with positive feedback for enhancement of the transconductance. Findings: The proposed OTA obtains a DC gain (Ao) of 26 dB, a Gain-Bandwidth Product (GBW) of 750 MHz, Slew Rate (SR) of 3.7 V/µs, a Phase Margin (PM) of 98°, DC offset of 2.2 mV and a power dissipation of 250 µW under no load condition. The proposed OTA is simulated in 90-nm CMOS technology using Cadence EDA software. Voltage to current (V/I) convertor based on proposed OTA is also simulated in 90-nm CMOS technology. The simulated results confirm rail to rail operation with the transconductance of 26 µS and bandwidth upto 40 MHz. The overall power consumption is also very less which makes it useful for low power portable applications. Applications/Improvements: The OTA proposed in this paper can be employed in low power biomedical and sensor applications. The gain could be increased for the proposed OTA as it is less and could be enhanced.

Keywords: Low Voltage, Operational Transconductance Amplifier, Source Degeneration, Sub-threshold

1. Introduction

Aggressive scaling of the CMOS circuits, the most widely used remedy to decrease the dissipation of power is by reducing the operating voltage to values less than 1 V. CMOS circuits working in weak-inversion are best for low power applications as they have good $\frac{g_{mb}}{I}$ ratio and have very good efficiency. On the other hand, due to device scaling the operating voltage and the threshold voltage are reduced resulting in reduction of the intrinsic gain. Amplifiers operating at very low supply voltages are best for bio-medical and sensor applications where energy can be harvested from its environment. In biomedical devices such as ambulatory heart detectors and hearing aids very low power consumption is used to increase the battery life. There is equal importance for low voltage and lower power operation in portable applications as low voltage operation enables the use of lesser of batteries thereby being advantageous for size and weight considerations and the battery life gets improved by low power consumption. For low voltage the main idea is to make the circuit operate in the weak inversion region. There are various approaches like floating gate approach, self-cascode structures. The utilization of bulk-driven differential pair might beat a few requirements forced by supply voltages in situations where its operating voltage is of the same request as the threshold voltages. Recent publications which are using this technique has provided dependable low voltage power amplifiers. Although huge difficulty for this technique is the reduction in $\frac{g_{mb}}{gm}$ ratio in the CMOS technologies, there are some drawbacks of the bulk-driven technique like the value of gmb will be 5–8 times smaller than the value of gm and very large parasitic capacitance on the bulk and high input referred noise. Therefore, we represent a differential pair operating in sub-threshold region using bulk-driven technique.

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as one possible solution to contend with the $g_{mb} = g_m$ ratio reduction by upgrading the transconductance and enhancing the unity gain frequency ($f_T$) as well as the open loop gain without increasing the power consumption. The principle of the bulk-driven technique is that the input is given on the body that is less than the threshold voltage and a voltage is being set on the gate terminal so as to form a channel. The thickness of the depletion zone i.e. the conduction channel is affected by the bulk voltage. A bulk-driven symmetrical OTA operating in weak inversion can result in both reduced power consumption and high linearity. The utilization of this technique makes it conceivable to design low-voltage OpAmps with very large value of input CMRR and low power dissipation on the CMOS technologies. The proposed OTA can be implemented in low power applications with a correct voltage to current conversion which has been discussed.

In this paper we have used conventional transistors as compared to the halo implanted transistors. The proposed OTA using bulk driven technique is simulated with improved various parameters such as slew rate, the effective transconductance, input referred noise, phase margin, as well as improvement in other OpAmp performance parameters.

In section 2 a brief on the basic theory of the bulk driven technique and weak inversion operation is mentioned. In section 3 details of the proposed OTA are described and results are demonstrated and discussed in section 4 of the proposed OTA. In section 5, an application approach is simulated using the proposed OTA. Section 6 concludes the paper.

2. Basic Theory of the Bulk-driven Technique and Weak Inversion Operation

Bulk-driven MOSFET was first adopted in. While designing an OTA while adopting the bulk-driven technique the most significant stage is the input stage. In this technique, a fixed voltage is associated with the gate terminal and the input is given into the bulk terminal as shown in Figure 1. With the zero-bias voltage on the bulk terminal the transistors are in weak inversion. The two fundamental favorable circumstances of utilizing the bulk-driven system are that the bulk-driven differential sets in an OpAmp and incredibly enhances the transconductance and the threshold voltage of the transistor vanishes and both negative and positive bias voltages ($V_{BS}$) are conceivable. Whereas there are a couple of downsides to this technique when contrasted with the gate driven method, for example, little transconductance due to the less input capacitance of the depletion layer and larger parasitic capacitance to the mass which diminishes the $f_T$. Due to the smaller transconductance the device will have high input referred noise. By setting the input signals on the substrate instead of gate terminals the input differential pair will results in large input CMRR of the OpAmp. The enhancement in the transconductance is determined by the positive feedback.

The drain current $I_{DS}$ of the MOS transistor operating in weak inversion is dependent on a channel diffusion current that can be expressed as

$$ I_{DS} = \alpha \exp \left( \frac{qV_{GS}}{nkT} \right) \exp\left[ \frac{q(n-1)V_{BS}}{nkT} \right] $$

Where $n$ is the slope factor in weak inversion, which can be defined as $1+g_{mb}/g_m$, it is in fact not a consistent variable but rather a component of the process parameters and substrate biasing. This gives fundamental further point in expected transconductance in these circuits. The transistor will be operating when $V_{DS} > 3kT/q$. This paper presents simulated results only of an improvement in the transconductance for input differential pair. The transconductance of the pair is defined as

$$ Gm = \frac{I_o}{V_m} $$

Where $I_o$ is the output current and $V_m$ is the input voltage. As the CMOS scaling is done, the ratio of $g_{mb}$ and $g_m$ decreases, however the improvement element $(n+1)/(n-1)$ ratio increments demonstrating the overall transconductance will increment with scaling.

Figure 1. Bulk-driven nMOS.
3. Proposed Bulk-driven OTA Circuit

Circuit diagram of the proposed bulk-driven OTA circuit is shown in Figure 2. The proposed OTA consists with two differential pairs. The input signal is given on the body of the PMOS in the first differential pair. It consists of four p-type transistors. The four transistors are represented as \( M_{1a}, M_{1b}, M_{2a}, M_{2b} \). The transistors \( M_{1a} \) and \( M_{2a} \) are identical, whereas the \( M_{1b} \) and \( M_{2b} \) are also identical. The drains of the \( M_{1b} \) and \( M_{2b} \) are connected to the other differential pair. The reference current \( (I_{REF}) \) is given as 500 µA. Moreover, the slew rate to the amplifier is determined by the reference current. The main objective of the proposed OTA is that all the transistors should work in the weak inversion region. The circuit has an operating voltage of 0.4 V. Two identical transistors \( M_3 \) and \( M_4 \) are the PMOS transistors used as active loads and they are divided into four PMOS. Higher swing results in the expansion in the DC shift. The compensation circuit consists of a capacitor of 100F. The capacitor \( C_c \) is placed before the final stage. It is basically an on-chip amplifier. The Bandwidth of the proposed OTA is significantly very large, which therefore leads to higher Gain Bandwidth product (GBW). The frequency should be high for the design of OTA. The phase margin of the proposed OTA is 98°.

4. Simulation Results

The transient response with an operating frequency of 100Hz is shown in Figure 3, 10-mVpp input to only the inverting input terminal. The rise time is about 10 ns. Figure 4 shows the simulated bode diagrams for proposed OTA in this paper. The output impedance is independent of the bulk-driven differential pair and change in open loop gain. The unity gain frequency is dependent to the change in transconductance. But there are other parameters which are having good value. The reference current is 500 µA with the power supply of 0.4 V, allowing all the transistors operating in weak inversion.

Figure 5 demonstrates the change on the output current with change in the temperature. The simulated results verify that there is an increase in the output current as the temperature is increasing. At \( T = 0^\circ \) the output current increases and becomes constant when the input voltage is 0.4 V. At \( T = 20^\circ \) the output current increases and decreases when voltage is 0.5 V. Current variation is shown with change in temperature. The PSRR performance is also

![Figure 2. Circuit diagram of the proposed operational transconductance amplifier.](image)

![Figure 3. Transient response of the OTA.](image)

![Figure 4. Simulated bode diagrams for the proposed bulk-driven OTA.](image)
simulated when the conditions are VDD = 0.4 V and no load condition. The simulated result is shown in Figure 6. The proposed OTA achieves a PSRR of 54.5 dB at low frequencies whereas the roll-off frequency is ~100 Hz.

Table 1 lists the performance comparisons between the proposed OTA and previous publications. The analysis is done by using Cadence tool. The PSRR of the proposed OTA is ~54.5 dB at 100 Hz. The value of PSRR reduces at high frequencies. The circuit is having high PSRR due to the output capacitance. The value of the PSRR is dependent to the output capacitance. Due to the value of biasing current, high slew rate of the proposed OTA is achieved. The equation (1) shows the pole frequency expression of this proposed OTA is calculated by

$$f_{nd} = \frac{gm6}{2\pi CL}$$  \hspace{1cm} (3)

5. V-I Convertor by using Bulk-driven OTA Circuit

Figure 7 shows the simplest configuration of a V-I converter. The design is made out of a voltage divider which is buffered before the V-I converter. Rail to rail input voltage divider is present before the V-I converter which helps in attenuation of the input voltage. The proposed V-I converter is thereby essentially consist of cascaded structure. Functioning involves the input voltage V_in being propagated to the OTA voltage follower with the input-output voltage being rail to rail. A modular circuit can be set only with cascode configuration so that in the second phase the cascode transistors can enhance the current being copied and increase output resistance. The voltage divider formed
6. Conclusion

The low voltage OTA employed in this paper using bulk-driven input differential pair is presented. The circuit is simulated in 90-nm standard CMOS process using Cadence EDA software. Source degeneration with the positive feedback in a differential pair was the methodology utilized to enhance the transconductance and the slew rate. The difference in transconductance, the execution features of the OpAmp, for example, slew rate, UGBW, GBW are all upgraded. The GBW of the OpAmp is 750 MHz and the slew rate is 3.7 V/μsec while achieving a PSRR of ~55 dB with a 0–100-kHz frequency range. The power consumption is 250 µW and a value of 0.4 V for operating voltage making this OpAmp very useful in high speed transmission and biomedical applications.

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Table 2. V-I convertor performance comparisons

| Design Parameters | (12), 1999 | (10), 2007 | (11), 2011 | (13), 2012 | This Work 2015 |
|-------------------|------------|-----------|-----------|-----------|----------------|
| CMOS Technology   | 1.2 μm     | 0.5 μm    | 0.18 μm   | 0.18 μm   | 90 nm         |
| Supply Voltage    | 3 V        | 1.5 V     | 1 V       | 1.2 V     | 0.4 V         |
| Transconductance  | 20 μS      | 10 μS     | 100 μS    | 12.5 μS   | 26 μS         |
| Input Range       | 0–2.8 V    | 0–3 V     | 0–1 V     | 0–1.19 V  | 0–1 V         |
| Bandwidth         | n.a        | 90 MHz    | 39.2 MHz  | 5.2 MHz   | 40 MHz        |
| Input referred noise | n.a    | 1.78 μV/√Hz | n.a    | 341.6 μV/√Hz | 2.4 μV/√Hz |
| Power consumption | 310 μW     | 3000 μW   | 730 μW    | 75 μW     | 350 μW        |
| FoM               | n.a        | 30 MHz/mW | 54 MHz/mW | 69 MHz/mW | 190 MHz/mW    |

Table 2. shows V-I convertor performance and compared with previously published V-I converters.

The voltage is buffered to $V_A = V_{in2} = αV_{out1} = αV_{in}$. Then, the generated current $I_1 = \frac{α}{R_s} V_{in}$. The FoM from can be expressed as

$$\text{FoM} = \frac{V_{in}}{VDD} \times BW / Power$$

Publications published recently which are peak to peak V-I converters derived by implementing the input terminals with passive resistors.

Figure 7. V-I convertor using bulk-driven OTA.
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