Impedance Design of Excitation Lines in Adiabatic Quantum-Flux-Parametron Logic Using InductEx

Naoki Takeuchi, Member, IEEE, Hideo Suzuki, Member, IEEE, Coenrad J. Fourie, Senior Member, IEEE, and Nobuyuki Yoshikawa, Senior Member, IEEE

Abstract—The adiabatic quantum-flux-parametron (AQFP) is an energy-efficient superconductor logic family that utilizes adiabatic switching. AQFP gates are powered and clocked by ac excitation current; thus, to operate AQFP circuits at high clock frequencies, it is required to carefully design the characteristic impedance of excitation lines (especially, above AQFP gates) so that the microwave excitation current can propagate without reflections in the entire circuit. In the present study, we design the characteristic impedance of the excitation line using InductEx, which is a three-dimensional parameter extractor for superconductor devices. We adjust the width of an excitation line using InductEx such that the characteristic impedance is maintained at 50 Ω even above an AQFP gate. Then, we fabricate test circuits to verify the impedance of the excitation line. We measure the impedance using time domain reflectometry (TDR). We also measure the S parameters of the excitation line to investigate the maximum possible clock frequency. Our experimental results indicate that the characteristic impedance of the excitation line agrees well with the design value even above AQFP gates, and that clock frequencies beyond 5 GHz are possible in large-scale AQFP circuits.

Index Terms—Adiabatic logic, quantum flux parametron, impedance calculation.

I. INTRODUCTION

SUPERCONDUCTOR logic families [1]–[4] are crucial for achieving cryogenic information systems, such as energy-efficient microprocessors [5], [6], single-photon image sensors [7], [8], and quantum computers [9], [10]. We have been investigating adiabatic quantum-flux-parametron (AQFP) logic [11], which is an adiabatic logic family based on the quantum flux parametron (QFP) [12], [13]. AQFP circuits can operate with an energy dissipation of approximately $10^{-21}$ J per Josephson junction [14] by using underdamped high-critical-current-density Josephson junctions, which maximize the benefit of adiabatic switching [15], [16]. We have designed and demonstrated various AQFP circuits, such as a microprocessor [6], a cryogenic detector interface [8], and a stochastic problem solver [17].

To conduct adiabatic switching, the potential energy of an AQFP gate is modulated between a single-well shape and a double-well shape by applying an ac excitation current. This means that all AQFP gates, including both combinational and sequential circuits, must be powered and clocked by the excitation current. Furthermore, unlike complementary metal–oxide–semiconductor (CMOS) logic, AQFP gates must be clocked in the order of logic operation with moderate clock skews. We have proposed clocking schemes for AQFP logic [18], [19] to appropriately distribute the excitation current in the entire AQFP circuit, whereby we have demonstrated small-to-medium-scale AQFP circuits at GHz-range clock frequencies [14], [19]. To apply the above clock schemes to large-scale AQFP circuits at high clock frequencies, it is required to carefully design the characteristic impedance of excitation lines (i.e., clock paths) so that the microwave excitation current is applied equally to each AQFP gate without standing waves. However, it has been difficult to design the impedance of excitation lines precisely because the physical structure of excitation lines is too complicated to allow theoretical estimation of the impedance; a part of an excitation line is placed above AQFP gates and thus cannot be treated as a simple microstrip line, as will be shown later. Note that the impedance of a simple microstrip line can be analytically estimated [20], [21], and that microstrip and strip lines are used for interconnection in RSFQ circuits [22].

In this paper, we precisely design the impedance of excitation lines using InductEx [23], which is a three-dimensional inductance extractor for superconductor devices. Recently, characteristic impedance calculation capability was added to InductEx [24], which simultaneously calculates the magnetoquasistatic inductance, with the inclusion of kinetic inductance, and the electroquasistatic capacitance, with the inclusion of multiple dielectric layers. We adjust the width of an excitation line using InductEx such that the characteristic impedance is maintained at 50 Ω even above an AQFP gate. Then, we fabricate test circuits to verify the impedance of the designed excitation line. We measure the impedance using time domain reflectometry (TDR) [25]. We also measure the S parameters of the excitation line to investigate the maximum possible clock frequency.

Manuscript received November 27, 2020; revised January 18, 2021; accepted February 1, 2021. Date of publication February 9, 2021; date of current version March 9, 2021. This work was supported by KAKENHI under Grants 18H01493 and 19H05614 from the Japan Society for the Promotion of Science (JSPS).

(Corresponding author: Naoki Takeuchi.)

Naoki Takeuchi and Hideo Suzuki are with the Institute of Advanced Sciences, Yokohama National University, Hodogaya, Yokohama 240-8501, Japan (e-mail: takeuchi-naoki-kx@ynu.ac.jp; suzuh@ynu.ac.jp).

Coenrad J. Fourie is with the Department of Electrical and Computer Engineering, Stellenbosch University, Stellenbosch 7602, South Africa (e-mail: coenrad@sun.ac.za).

Nobuyuki Yoshikawa is with the Institute of Advanced Sciences, Yokohama National University, Hodogaya, Yokohama 240-8501, Japan, and also with the Department of Electrical and Computer Engineering, Yokohama National University, Hodogaya, Yokohama 240-8501, Japan (e-mail: nyoshi@ynu.ac.jp).

Coenrad J. Fourie is with the Department of Electrical and Computer Engineering, Stellenbosch University, Stellenbosch 7602, South Africa (e-mail: coenrad@sun.ac.za).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TASC.2021.3058080.

Digital Object Identifier 10.1109/TASC.2021.3058080

1051-8223 © 2021 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See https://www.ieee.org/publications/rights/index.html for more information.
II. IMPEDANCE DESIGN

Fig. 1(a) illustrates an AQFP buffer, which is one of the most fundamental logic gates in AQFP logic, and Fig. 1(b) shows typical waveforms for the buffer. The buffer is in the form of an rf superconducting quantum interference device (SQUID) whose Josephson junction is replaced with a dc SQUID (J1-L1-L2-J2). The excitation current \( I_x \) modulates the critical current of the dc-SQUID, i.e., the potential energy shape of the buffer. A dc offset current \( I_d \) applies an offset flux of 0.5\( \Phi_0 \) for four-phase clocking [18], where \( \Phi_0 \) is the flux quantum. While \( I_x \) increases, either J1 or J2 switches depending on the polarity of the input current \( I_{in} \). Consequently, the state current \( I_{st} \), which represents the logic state of the buffer, appears through the load inductor \( L_q \). A positive \( I_{st} \) represents a logic 1, whereas a negative \( I_{st} \) represents a logic 0. A signal transformer composed of \( L_q \) and \( L_{out} \) is included to facilitate logic negation; while the AQFP gate shown in Fig. 1(a) operates as a buffer for a positive \( k_{out} \), it operates as an inverter for a negative \( k_{out} \).

Since an AQFP gate is powered and clocked by \( I_x \) as shown in Fig. 1, the operating frequency (clock frequency) of an AQFP gate is equal to the frequency of \( I_x \). Therefore, the characteristic impedance \( Z_0 \) of the excitation line \( L_x \) should be carefully designed such that \( I_x \) can propagate through \( L_x \) without reflections even at GHz-range clock frequencies. Fig. 2(a) shows the physical layout of an AQFP buffer designed for the AIST 10 kA/cm\(^2\) Nb high-speed standard process (HSTP) [18], whose dimensions are 20 \( \mu \text{m} \) (width) by 40 \( \mu \text{m} \) (height). The HSTP includes four Nb layers (M1 through M4), where M1 is used for ground planes and Josephson junctions are formed between M2 and M3. Here, we calculate \( Z_0 \) using InductEx and adjust the line width of \( L_x \) such that \( Z_0 \) becomes 50 \( \Omega \). One difficulty in impedance calculation using InductEx is that the current version of InductEx cannot handle non-planarized processes such as HSTP, due to modeling limitations when the surface model for capacitance calculation is generated. As shown in Fig. 2(a), part of \( L_x \) (in M4) is placed above inductors \( L_1 \) and \( L_2 \) (in M3); thus, the distance \( d \) between \( L_x \) and the ground plane (in M1) is different for segments A and B. Consequently, the impedance (i.e., inductance and capacitance) of \( L_2 \) in segment A and that in segment B separately, and then calculate \( Z_0 \) from the total inductance and capacitance in segments A and B. Fig. 2(b) shows the physical model used to calculate the impedance in segment A, where \( L_x \) is a microstrip line placed above \( L_1 \) and \( L_2 \) with \( d = 1.6 \mu \text{m} \). The Josephson junctions (J1 and J2) are replaced with ground contacts (GC1 and GC2) because \( L_1 \) and \( L_2 \) are connected to the ground plane via J1 and J2. InductEx yields the inductance between ports P1 and P2 as well as the capacitance between the microstrip line \( L_{st} \) and ground. Fig. 2(c) shows the physical model for segment B, where \( L_x \) is a simple microstrip line with \( d = 1.2 \mu \text{m} \). Using the physical models shown in Figs. 2(b) and (c), we calculate \( Z_0 \) and adjust the line width of \( L_x \), where the relative permittivity of SiO\(_2\) layers between Nb layers is set to 3.9. We found that \( Z_0 \) becomes approximately 50 \( \Omega \) when the line width is 1.5 \( \mu \text{m} \); the inductance and capacitance with regard to \( L_{st} \) in segment A are 5.10 pH and 2.33 fF, respectively, and those in segment B are 1.80 pH and 0.501 fF, respectively, which results in a \( Z_0 \) of 49.4 \( \Omega \) and a phase velocity \( v_p \) of 1.43 \( \times 10^8 \) m/s. It should be noted that \( v_p \) is lower than that of a simple 50-\( \Omega \) microstrip line with \( d = 1.2 \mu \text{m} \) (2.4 \( \mu \text{m} \)) and that the phase velocity is lower than that of a simple microstrip line with \( d = 1.2 \mu \text{m} \) (1.63 \( \times 10^8 \) m/s). This is because \( L_1 \) and \( L_2 \) are connected to the ground plane, so that the capacitance between \( L_x \) and the ground plane increases in segment A. Meanwhile, inductance decreases slightly in segment A; the inductance per
unit length in segment A is 0.34 pH/μm, whereas that in segment B is 0.36 pH/μm.

### III. Experiments

We measure $Z_0$ to verify the calculation results obtained using InductEx. Fig. 3(a) illustrates the experimental setup used to measure $Z_0$ through TDR. An array of AQFP buffers are coupled to a long meandering excitation line, which is represented by a transmission line rather than lumped inductors. A step generator (Tektronix, SD-24) applies an incident pulse with a short rise time to the excitation line, and then reflected pulses appear where the characteristic impedance changes. A sampling oscilloscope (Tektronix, 11801) samples the resultant wave of the incident and reflected pulses, thereby measuring $Z_0$. It should be noted that a large reflected pulse appears at the end of the excitation line because of the open end. This makes it easy to measure both $Z_0$ and $v_p$, as will be shown later. We also measure the S parameters of the excitation line to determine the maximum operating frequency. Fig. 3(b) illustrates the experimental setup used to measure the S parameters. As with Fig. 3(a), an array of AQFP buffers are coupled to a long meandering excitation line. Both input and output ports are terminated by a vector network analyzer (VNA) (Keysight, P9374A). The VNA measures the transmission loss ($S_{21}$) and reflection loss ($S_{11}$) of the excitation line. Fig. 4 shows a micrograph of the chip including the circuits under test (CUTs) for the TDR and S parameter measurements. This chip was fabricated through HSTP with a $5 \times 5$ mm die, including five CUTs (CUT 1 through CUT 5). CUT 1 through CUT 3 are for the TDR measurement and correspond to the schematic in Fig. 3(a). The length of the excitation line ($l$) varies between CUT 1 through CUT 3: $l$ = 15 mm, 30 mm, and 45 mm for CUT 1 through CUT 3, respectively. CUT 4 is a through line used as a reference in the S parameter measurement. CUT 5 is for the S parameter measurement and corresponds to the schematic in Fig. 3(b) with $l$ = 15 mm. The inset shows part of an AQFP buffer array, where the physical layout of each buffer is the same as that shown in Fig. 2(a).

We conducted experiments using a wide-bandwidth cryoprobe at 4.2 K in liquid He. Fig. 5(a) shows the TDR measurement results for CUT 1 through CUT 3. The blue, green, and red solid lines are the voltage signals for, respectively, CUT 1, CUT 2, and CUT 3. The amplitude of the incident pulse ($V_0 = 0.250$ V) corresponds to 50 Ω, and the voltage difference $ΔV$ from $V_0$ represents the characteristic impedance of the CUTs. The sharp rises at the edges of the voltage signals represent the reflected pulses at the open ends, and the fluctuations between 85.8 ns and 86.0 ns represent impedance changes due to the pads on the chip. Thus, the voltage signal between 86.0 ps and the rise at the edge represents $Z_0$ of the excitation line. Fig. 5(a) shows that $ΔV$ for the excitation line is 6.49 mV, which is an average between 86.24 ns and 86.44 ns for CUT 3. Therefore, $Z_0 = (1 + ρ)/(1 − ρ) × 50 = 52.7$ Ω, where $ρ = ΔV/V_0 = 0.0260$. The measured $Z_0$ agrees well with the simulation result (49.4 Ω). The slight discrepancy may have arisen because the impedance calculation using InductEx does not take into account the shrinkage in the line width of $L_x$ (typically, approximately 0.1 μm). We also measured $v_p$ based on Fig. 5(a). The difference in the timing of the rising edges in the voltage signals ($t_1$ through $t_3$) is attributed to the difference in the excitation line length ($Δl$); thus, this time difference corresponds to $2Δl/v_p$, where the coefficient 2 is for the round-trip length. Fig. 5(b) shows the timing of the rising
edges as a function of the round-trip length of an excitation line ($2l$), where the solid line represents the linear regression given by $\alpha \times 2l + \beta$ ($\alpha = 7.38$ ps/mm, $\beta = 86.0$ ps). Consequently, $v_p$ is given by $1/\alpha = 1.35 \times 10^8$ m/s, which agrees well with the simulation result ($1.43 \times 10^8$ m/s).

Fig. 6 shows the measurement results of $S_{21}$ and $S_{11}$ for CUT 4 and CUT 5. The blue dashed lines are the results for CUT 4, and the red solid lines are for CUT 5. Since CUT 4 is a through line, the $S$ parameters for CUT 4 represent the frequency response of the cryoprobe used in the experiment. Fig. 6(a) shows that $S_{21}$ for CUT 5 is almost the same as that for CUT 4 up to approximately 6 GHz. Figs. 6(a) and (b) show that for CUT 5 there is no clear dip in $S_{21}$ or peak in $S_{11}$ at the resonant frequency ($v_p/2l = 4.5$ GHz). The above measurement results indicate that a microwave excitation current can propagate along a long excitation line above AQFP buffers without significant reflections, and that high clock frequencies are possible in large-scale AQFP circuits. The measurement results also validate piecewise impedance calculation with InductEx, and the applicability of quasistatic calculation of characteristic impedance in superconductor integrated circuit layouts at frequencies far below the gap frequency.

IV. CONCLUSION

We designed the characteristic impedance of the excitation line in an AQFP buffer using InductEx so that the microwave excitation current can propagate in a large-scale AQFP circuit without reflections. We verified that the characteristic impedance of the excitation line agrees well with the design value in the TDR experiment. We also found that a microwave excitation current can propagate along a long excitation line without significant reflections in the $S$ parameter measurement. It is noteworthy that the excitation line design for the buffer is applicable to other logic gates because in AQFP logic the physical layout design of all logic gates is based on that of a buffer [26]. Our measurement results demonstrated that a microwave excitation current can propagate appropriately in a large-scale AQFP circuit with the help of impedance design using InductEx.

ACKNOWLEDGMENT

The circuits were fabricated in the Clean Room for Analog-digital superconductivity (CRAVITY) of the National Institute of Advanced Industrial Science and Technology (AIST). The authors thank K. Jackman for his valuable contributions.
REFERENCES

[1] K. K. Likharev and V. K. Semenov, “RSFQ logic/memory family: A new Josephson-junction technology for sub-terahertz-clock-frequency digital systems,” IEEE Trans. Appl. Supercond., vol. 1, no. 1, pp. 3–28, Mar. 1991.

[2] O. A. Mukhanov, “Energy-efficient single flux quantum technology,” IEEE Trans. Appl. Supercond., vol. 21, no. 3, pp. 760–769, Jun. 2011.

[3] Q. P. Herr, A. Y. Herr, O. T. Oberg, and A. G. Ioannidis, “Ultra-low-power superconductor logic,” J. Appl. Phys., vol. 109, no. 10, 2011, Art. no. 103903.

[4] M. Tanaka, M. Ito, A. Kitayama, T. Kouketsu, and A. Fujimaki, “18-GHz, 4.0-aJ/bit operation of ultra-low-energy rapid single-flux-quantum shift registers,” Jpn. J. Appl. Phys., vol. 51, May 2012, Art. no. 053102.

[5] Y. Ando, R. Sato, M. Tanaka, K. Takagi, N. Takagi, and A. Fujimaki, “Design and demonstration of an 8-bit bit-serial RSFQ microprocessor: CORE e4,” IEEE Trans. Appl. Supercond., vol. 26, no. 5, Aug. 2016, Art. no. 1301205.

[6] C. L. Ayala, T. Tanaka, R. Saito, M. Nozoe, N. Takeuchi, and N. Yoshikawa, “MANA: A monolithic adiabatic iNtegration architecture microprocessor using 1.4aJ/op superconductor Josephson junction devices,” in Proc. IEEE Symp. VLSI Circuits, 2020, pp. 1–2.

[7] S. Miyajima, M. Yabuno, S. Miki, T. Yamashita, and H. Terai, “High-time-resolved 64-channel single-flux quantum-based address encoder integrated with a multi-pixel superconducting nanowire single-photon detector,” Opt. Exp., vol. 26, no. 22, Oct. 2018, Art. no. 29045.

[8] N. Takeuchi et al., “Scalable readout interface for superconducting nanowire single-photon detectors using AQFP and RSFQ logic families,” Opt. Exp., vol. 28, no. 11, May 2020, Art. no. 15824.

[9] M. W. Johnson et al., “A scalable control system for a superconducting adiabatic quantum optimization processor,” Supercond. Sci. Technol., vol. 23, no. 6, Jun. 2010, Art. no. 065004.

[10] E. Leonard et al., “Digital coherent control of a superconducting qubit,” Phys. Rev. Appl., vol. 11, no. 1, 2019, Art. no. 014009.

[11] N. Takeuchi, D. Ozawa, Y. Yamanashi, and N. Yoshikawa, “An adiabatic quantum flux parametron as an ultra-low-power logic device,” Supercond. Sci. Technol., vol. 26, no. 3, Mar. 2013, Art. no. 035010.

[12] K. Loe and E. Goto, “Analysis of flux input and output Josephson pair device,” IEEE Trans. Magn., vol. MAG-21, no. 2, pp. 884–887, Mar. 1985.

[13] M. Hosoya et al., “Quantum flux parametron: A single quantum flux device for josephson supercomputer,” IEEE Trans. Appl. Supercond., vol. 1, no. 2, pp. 77–89, Jun. 1991.

[14] N. Takeuchi, T. Yamae, C. L. Ayala, H. Suzuki, and N. Yoshikawa, “An adiabatic superconductor 8-bit adder with 24kJ/T energy dissipation per junction,” Appl. Phys. Lett., vol. 114, no. 4, Jan. 2019, Art. no. 042602.

[15] K. Likharev, “Dynamics of some single flux quantum devices: I. Parametric quantumtron,” IEEE Trans. Magn., vol. 13, no. 1, pp. 242–244, Jan. 1977.

[16] J. G. Koller and W. C. Athas, “Adiabatic switching, low energy computing, and the physics of storing and erasing information,” in Workshop Phys. Computation, 1992, pp. 267–270.

[17] N. Takeuchi, M. Aono, and N. Yoshikawa, “Superconductor amoeba-inspired problem solvers for combinatorial optimization,” Phys. Rev. Appl., vol. 11, no. 4, Apr. 2019, Art. no. 044069.

[18] N. Takeuchi et al., “Adiabatic quantum-flux-parametron cell library designed using a 10 kA cm−2 niobium fabrication process,” Supercond. Sci. Technol., vol. 30, no. 3, Mar. 2017, Art. no. 035002.

[19] N. Takeuchi, M. Nozoe, Y. He, and N. Yoshikawa, “Low-latency adiabatic superconductor logic using delay-line clocking,” Appl. Phys. Lett., vol. 115, no. 7, Aug. 2019, Art. no. 072601.

[20] W. H. Chang, “The inductance of a superconducting strip transmission line,” J. Appl. Phys., vol. 50, no. 12, pp. 8129–8134, Dec. 1979.

[21] T. Van Duzer and C. W. Turner, Principles of Superconductive Devices and Circuits, NJ: Prentice Hall PTR, 1999.

[22] K. Takagi et al., “SFQ propagation properties in passive transmission lines based on a 10-Nb-layer structure,” IEEE Trans. Appl. Supercond., vol. 19, no. 3, pp. 617–620, Jun. 2009.

[23] C. J. Fourie, “Full-gate verification of superconducting integrated circuit layouts with InductEx,” IEEE Trans. Appl. Supercond., vol. 25, no. 1, Feb. 2015, Art. no. 1300209.

[24] C. J. Fourie, “Electronic design automation tools for superconducting circuits,” J. Phys. Conf. Ser., vol. 1590, no. 1, Jul. 2020, Art. no. 012040.

[25] Tektronix, Inc., “TDR impedance measurements: A foundation for signal integrity,” 2008. [Online]. Available: https://www.tek.com/document/fact-sheet/tdr-impedance-measurements-foundation-signal-integrity

[26] N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, “Adiabatic quantum-flux-parametron cell library adopting minimalist design,” J. Appl. Phys., vol. 117, no. 17, 2015, Art. no. 173912.