A real-time ultra-low light color imaging system based on FPGA

Wang Hua1,2,*, Bian He2, Yang Lei1,2, Zhang Hui1,2, Cao Jianzhong2
1University of Chinese Academy of Sciences, Beijing 100049, China
2Xi’an Institute of Optics and Precision Mechanics of Chinese Academy of Sciences, Xi’an, Shaanxi 710119, China

*Corresponding author:wanghua@opt.ac.cn

Abstract. This article shows a low light color image acquisition system. The core components of the system are the Fairchild’s SCMOS image sensor CIS1910F1111 and XILINX’s Artix-7 XC7A100T-2CSG324I FPGA, the remarkable advantage of the system is that it can obtain better color imaging effect under lower illumination environment, and the image noise is much less than other similar products. Based on the excellent imaging performance of the image detector, a high performance real-time low-light level color imaging system is developed. This imaging system can obtain the characteristic information of the targets under ultra-low illuminance environment, including the details, colors and so on. The hardware of the low light level imaging system mainly contains a color SCMOS image sensor and a FPGA, a driving circuit of a combination of DDR3, the ultra-low noise power conversion circuit and a Camera-Link and a 3G-SDI interface circuits. The SCMOS chip is used for photoelectric conversion of the shot scene and the FPGA is used for the control of the whole imaging system, image acquisition and image processing, etc. The FPGA software system consists of SCMOS initialize configuration and timing control module, automatic exposure control module, real-time color image processing module, imaging tone mapping module, image denoising module and image enhancement module. The automatic exposure control (AEC) module adaptively adjusts the average gray value of the region of interest. The module automatically calculates the exposure time and gain value of the next frame according to the current frame image data value. The real-time color image processing module includes color restoration, automatic white balance and color spaces conversion, etc. The image denoising module uses the advanced real-time guide-filter algorithm. The image tone mapping module and enhancement module are proposed based on an improved automatic threshold logarithmic and enhancement algorithm. Combining the hardware and FPGA soft algorithm with excellent performance, the imaging results show that the system can get good color image effect of the ultra-low light level about 10^{-2}lx.

Keywords: imaging system, real-time, ultra-low light.
1. Introduction
With the development of imaging technology, people need more and more low-light color imaging equipment. For low-light color imaging system, the performance of image detector directly affects the imaging effect of the whole imaging system, such as the lowest detectable environmental illumination and image signal-to-noise ratio. Existing visible light image detectors can be divided into CCD and CMOS. The advantages of CCD image detectors are high detection sensitivity, low noise and high dynamic range. However, CCD image detectors have high power consumption and complex circuit. CMOS image sensors offer many advantages for imaging system. Some of these advantages include: high MTF, high reliability, small size, low weight, day night color imaging [1], etc. Although CMOS image detector has the advantages of high integration, low power consumption and high readout frequency, its deficiencies in readout noise, dynamic range and detection sensitivity limit its applications at a higher level. In recent years, the development of SCMOS has made up for the deficiency of traditional CMOS image detectors to some extent. SCMOS image detectors have higher detection sensitivity and lower readout noise, showing their excellent performance in low-light imaging.

In recent years, low-level light color imaging system based on SCMOS has been widely used in industrial detection, safety protection, mobile night vision, auto driving and other fields. However, only relying on the low light level performance of SCMOS can not meet the needs of users for low light level imaging performance, especially for the acquisition of color information in low-light environment. This requires image enhancement by image processing algorithms to obtain better imaging effects. The low - level light color imaging system based on SCMOS is composed of hardware circuit and software algorithm, both of which have the same status. In order to get more target color and detail information in low light environment, we can work in two ways. In the design of hardware circuit, full consideration of the influence of power supply noise on the image sensor of SCMOS can help to obtain a cleaner original image data. In addition, refrigeration technology of the sensor also can reduce the image noise to a certain extent and improve the signal-to-noise ratio. In the software design, we can improve the image quality through image enhancement, image denoising, image sharpening and other technologies.

2. Hardware Design
There are three circuit boards in the imaging system. The closest one to the lens is the imaging board, which contains Fairchild's SCMOS chip and its peripheral drive circuit and the low noise power supply conversion circuit. This board realizes photoelectric conversion of the scene and output of the digital image data. The second circuit board is the system control and signal processing board, it contains a core processor – the FPGA, two pieces of DDR3 data cache chips, and one piece of configuration Flash. This FPGA is the Xilinx's A7 series ARTIX-7 XC7A100T-2CSG324I, it can be programmed according to different functional requirements and camera parameters control. The data cache chip is Micron's DDR3, which is used to cache the image data. The Flash chip is also selected from Micron's SPI Flash to cache the camera's FPGA configuration data. The last one is the interface board, which contains a camera link interface, a standard 3G-SDI interface and a UART communication interface. The main function of this circuit board is to output the image data to the host computer or monitor. These three boards are interconnected by inter-board connectors. The imaging system is powered by 5V DC power supply, and then the 5V DC power supply is converted into various low-voltage power supplies by the dc-dc module. After the system is powered on, FPGA automatically loads the program from flash through SPI interface. FPGA configures the internal registers of image sensor through JTAG interface, and configures DAC to generate SCMOS bias powers. Under the control of driving timing, SCMOS successively exposes and outputs the digital image data. FPGA receives the image data and carries out a series of image processing before sending it to the image display and acquisition system through the Camera Link and 3G-SDI port.

The hardware block diagram of the low-light color imaging system is shown in figure 1:
For the low-light imaging circuit, the power supply circuit of the sensor is particularly important, because the signal is weak under low-light conditions, so it is easy to be submerged by the noise. Therefore, the cleaner the bias power, the better chance we have of getting a good image.

The CIS1910F requires many bias power supplies, and these power supplies have strict requirements for noise. The specific power requirements of CIS1910F are listed in Table 1 [2].

Table 1. The specific power requirements of CIS1910F

| Parameter      | Voltage(unit:V) | Current(unit:mA) | Ripple       |
|----------------|-----------------|------------------|--------------|
| AVDD           | 3.3             | 90               | < 1mV RMS    |
| AVDD_PIX       | 3.3             | 10               | < 100 µV RMS |
| AVDD_RST1      | 2.77            | 1                | < 10 µV RMS  |
| AVDD_RST2      | 3.0             | 1                | < 10 µV RMS  |
| DVDD           | 1.8             | 160              | < 25 mV RMS  |
| DVDD_IO        | 1.8             | 65               | < 1 mV RMS   |
| VTX1_POS       | 3.3             | 80               | < 1 mV RMS   |
| VTX2_POS       | 3.3             | 80               | < 1 mV RMS   |
| VTX1_NEG       | -0.4            | 80               | < 100µV RMS  |
| VTX2_NEG       | -0.4            | 80               | < 1 mV RMS   |

As can be seen from Table 1, the sensor has very strict requirements on the RMS noise of the power supplies. For the power supply with larger working current and general RMS noise requirements, we use LDO chip for conversion, while for the bias power supply with small current, we use DAC and low noise operational amplifier for the design.

3. System Software Design
The main function of the software system is to control the the working state and mode of all components in the whole system, generate the driving sequence of SCMOS, collect the image data and process the image, and finally output the processed image. The software system consists of SCMOS initialize configuration and timing control module, automatic exposure control module, color image processing module, image denoising module, imaging tone mapping module and image enhancement module.
3.1. SCMOS driver
The SCMOS driver module contains two sub-modules: the SCMOS initialization configuration module and SCMOS drive timing generate module. The initialization configuration module of SCMOS completes the initialization configuration of internal registers of SCMOS image sensor through JTAG interface at the end of the sensor reset, there are forty-eight 32-bit registers in the sensor. By configuring these registers, the working parameters of image sensor can be set, such as exposure time, gain value, shutter mode, image window area and so on. In addition to image sensor register initialization configuration function, the module is also responsible for SCMOS bias power configuration and control. The configuration and control of bias power supply is realized by configuring the internal register value of DAC. By setting appropriate register parameters, we can easily obtain high-quality and high-precision bias voltage, which is very important for the normal operation of SCMOS. The direct interface between FPGA and DAC chip is SPI interface, including CS, SCK and DIN three signals. It is worth noting that when CS is low, the data DIN is written into register on the rising edge of SCK [3].

The timing generate module generates the timing waveform required for the operation of SCMOS, including exposure trigger, charge transfer and data selective readout signals. By controlling the working time sequence of the image sensor, we can control the working mode of the sensor, the working frame rate, the reading time of the effective frame and so on.

3.2. Data cache
Because the SCMOS outputs parallel image data through the top and bottom channels at the same time, in order to obtain a complete image, the lower half of the image data needs to be cached and then read out according to the prescribed image format to form a standard video stream. The image data cache chip uses DDR3, so the module also includes DDR3 for initialization and read-write control.
3.3. Color image process

The color image processing module includes color restoration, automatic white balance, color space conversion, image denoising, image enhancement, gamma correction and other algorithms. The color restoration module converts the original bayer data of sensor into color images, and the automatic white balance module automatically adjusts the color according to the color temperature, so as to achieve the most suitable color effect for human eyes. The image denoising, image enhancement and gamma correction modules are all designed to achieve better imaging effects under low light conditions. The image denoising algorithm is optimized by fast guided filtering and the image enhancement method is the dual-platform histogram algorithm. The main idea of dual platform histogram image enhancement based on FPGA is as follows [4]:

1. Calculate the histogram data of the input image when the image data is valid.
2. Adjust the statistical histogram data according to the set upper and lower thresholds [5] [6]:

\[
P(k) = \begin{cases} 
T_A, & p(k) > T_H \\
T_L, & T_H < p(k) < T_L \\
0, & 0 < p(k) < T_L \\
0 & p(k) = 0 
\end{cases}
\]

(1)

Where \(p(k)\) is the original statistical histogram and \(P(k)\) is the adjusted histogram.

3.4. Automatic exposure control (AEC)

Automatic exposure control module is based on grayscale statistics to calculate exposure time and digital gain. The basic idea of the AEC algorithm is to divide an image into 25 regions, and the average gray value of each region is counted in turn. Then different weight values are given according to the distance between each region and the center of the image, and the average gray value of each region and the weight are normalized to get the average gray value of the whole image. By comparing the difference between the average gray level of the current image and the expected gray level, the exposure time and gain value of the next frame image are dynamically adjusted until the average gray level of the image reaches the expected gray value. Finally, the values of the exposure time and gain value registers are reconfigured on the falling edge of the frame valid signal via the JTAG interface.

4. Experimental Results

The low-light color SCMOS imaging system captures 1080p@50Hz image data in real time, and image data is output and displayed via the Camera-Link interface and 3G-SDI interface and the image data can be collected by computer software.

The original low light level color image and the low light level color image after image enhancement are shown in Figure 3. Through the experiment results, we can see that image enhancement can make the details of the image more obvious, and the image display effect is better.

![Figure 3. Experimental results under 0.03lx illumination.](image-url)
5. Conclusion
The imaging results show that the low-light imaging system can capture 1080p@50Hz video image data in real time and the image can be displayed and captured by Camera Link and 3G-SDI. The design can be used for low illumination CMOS image acquisition and the imaging results show that the system can get good color image effect of the ultra-low light level about 10^-lx.

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