The Blockchain Based Auditor on Secret key Life Cycle in Reconfigurable Platform

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Abstract—The growing sophistication of cyber attacks, vulnerabilities in high computing systems and increasing dependency on cryptography to protect our digital data make it more important to keep secret keys safe and secure. Few major issues on secret keys like incorrect use of keys, inappropriate storage of keys, inadequate protection of keys, insecure movement of keys, lack of audit logging, insider threats and non-destruction of keys can compromise the whole security system dangerously. In this article, we have proposed and implemented an isolated secret key memory which can log life cycle of secret keys cryptographically using blockchain (BC) technology. We have also implemented a special custom bus interconnect which receives custom crypto instruction from Processing Element (PE). During the execution of crypto instructions, the architecture assures that secret key will never come in the processor area and the movement of secret keys to various crypto core is recorded cryptographically after the proper authentication process controlled by proposed hardware based BC. To the best of our knowledge, this is the first work which uses blockchain based solution to address the issues of the life cycle of the secret keys in hardware platform. The additional cost of resource usage and timing complexity we spent to implement the proposed idea is very nominal. We have used Xilinx Vivado EDA tool and Artix 7 FPGA board.

Index Terms—Blockchain, FPGA, Key Memory, Secret Key Life Cycle

I. INTRODUCTION

The security of a crypto system depends on three primary keys. **Symmetric Key**: is used to encrypt bulk data in symmetric key algorithms like AES, TDES, DES etc. **Private Keys**: of public-private key pair used in Asymmetric Key Cryptography such as RSA, Diffie Helmen etc. Private key is used for signature generation and key exchange process. **Hash Key**: is used to check integrity and authenticity of transactions and data with algorithms like SHA-3. Increasing volume of secret key and data protected by those keys makes the cryptographic key management relevant in current research trend [1]. There are several threats causes compromised key. In this article we have discussed about few major threats.

A. Storage

In many sense, processor based architectures are flexible but it can be exposed to software threats like cache attack [2], bus snooping [3], memory disclosure attack [4] etc. hence the storage of secret keys should be separated form software area and it should be isolated from any physical connection of processor.

B. Insecure Movement

A security processor allows key movements between several cores like Key Memory, RNG, Hash, Symmetric Key and Asymmetric Key core. All these key movement to the key memory and from the key memory should be authenticated and secured. These transactions of key mainly suffers two issues. A. The buses used for these movements can be snooped by software attacks. B. The request of key can be issued from some compromised IP placed inside the architecture. To overcome attack-A the most effective solutions are bus encryption [3], or partition of software area from these buses [5]. Attack-B can be prevented by verifying the signature of the requestee IP. To the best of our knowledge we did not find any similar solution in hardware platform.

C. Non-destruction

Once the signature of requestee IP is verified, the key should be released to the proper destination. Except the pre-master key, other keys should be destroyed securely. This removal of key should be logged cryptographically and should non-traceable.

D. Audit Logging

The secret keys of a security processor is the most sensitive data. The creation, deletion and the movement of secret key should be logged and audited cryptographically otherwise it will be difficult to identify a compromise for forensic investigation.

E. Incorrect use of keys

The generated master keys are for specific purposes. Hash core can not use encryption key and vice versa. If the keys are used for something else, the proper protection action should be taken. The main contribution of this article are stated below:

- This article proposes a security processor architecture which is partitioned in three separated areas such as processor area, crypto area, and confidential area. This architecture assures that secret key memory is isolated form processor area.
- The architecture proposes a blockchain based auditor to monitor secret key lifecycles. The architecture prevents insecure movement, unauthorized key request, non-destruction issued and incorrect use of keys.
The proposed security processor can execute 21 custom crypto instructions as shown in Table II. In this architecture we have partitioned three areas such as (i) processor area, (II) crypto area and (iii) confidential area. The whole architectural details is stated in [6]. The partitioned and isolated confidential area to store secret keys assures that the secret key never come in the processor area because the processor area is very much vulnerable for various software threats. The main contribution of the proposed article is to add a special private blockchain to audit the movement of secret keys. Each secret key movement is authenticated and registered graphically. To adopt blockchain, we have designed the data path controller (DPC), custom bus interconnect (CBI), buffer and a Signature Checker (SC) core. The architecture can execute 21 crypto instructions divided in 5 categories as shown in Table II. All these proposed instructions are executed by DPC and CBI. As instructed by the TLS white paper [7], the architecture processes instructions for pre – master key generation, master key generation, hash and encryption process. For the proposed blockchain process, we have created a new category named as common purpose. The details of other instructions are not described because of page restriction. It is to be noted that blockchain data is written in main memory which can be accessed by the PE.

A. Custom Bus Interconnect

The proposed custom bus interconnect (CBI) is a junction through which various crypto cores and the buffer which is created as gateway of Master Key Memory (MKM) can communicate. Various paths of crypto cores and buffer are controlled by 4 bits input and 4 bit output addresses. Input-output address pins are controlled by data path controller (DPC) IP. In our current version of design, we have 4 inputs coming from buffer, output of hash, output of RNG and output of RSA. The 5 outputs of CBI are connected with buffer, key of AES, key of hash and key of RSA block. The synchronization signals of input cores and output cores are also taken care of by CBI. The fig. 1 shows the synchronization signals such as RNG_done, Buff(rd), Hash_done, Buff_rdy, Hash_key_rdy and En_key_rdy. The CBI is combination of MUX and DE-MUX where MUX’s output is connected with DEMUX’s input. The input address and output address pins are the selecting inputs of MUX and DE-MUX respectively.

B. Data Path Controller

The proposed data path controller (DPC) is a slave IP of PE. The PE can send 21 instructions by Application Peripheral Interface (API) call for various crypto operations of TLS protocol. The data path controller maintains a control word register to execute the 21 instructions as shown in Table II. The PE can communicate DPC by AXI bus through PE bus interconnect. In the current version of hardware, DPC has 16 bits control word to control various crypto cores placed in the crypto area. The data path and binaries for all proposed instructions are shown in II. As shown in fig. 2 the 11th bit is set to logic 1 to enable the custom bus interconnect, otherwise it will be logic 0 to disable the said interconnect. The 16th to 13th bits are used to select the input address. If the input address is 0000, RNG will be selected. It will be 0001, 0010 and 0011 to select Buff, Hash and PubEn core respectively. The 12th and 9th bit is to address outputs. The output address will be 0000, 0001, 0010, 0011 and 0100 to select the Buff, Hash_Key, En_key, Hash_In and Pub_en_in core. The 6th to 1st bit of control word register (CWR) are used to enable different hardware blocks such as RSA, RNG, Hash, Enc, MKM and Buff. The PE directly can write to CWR to control the data path of the hardwares placed in the crypto area.

C. Buffer

The proposed buffer is a gateway to write or read keys to the MKM. This buffer can accommodate data, timestamp from timer IP, pre – hash from Signature Checker, read/write operation, signature of data and the system status. The
TABLE I: Comparison Results

| #  | key storage | Incorrect use | Insecure movement | Destruction | Audit log |
|----|-------------|---------------|-------------------|-------------|-----------|
| Proposed key memory | × | × | × | ✓ | ✓ |
| 2011 key memory | ✓ | ✓ | ✓ | × | |
| 2010 key memory | ✓ | ✓ | ✓ | × | |
| 2018 key memory | ✓ | ✓ | ✓ | × | |
| 2019 main memory | ✓ | ✓ | ✓ | × | |
| 2009 main memory | ✓ | × | ✓ | × | |
| 2015 cache memory | ✓ | ✓ | ✓ | × | |
| 2007 main memory | ✓ | ✓ | ✓ | × | |

✓ possible, × not possible

system status comes from the enable and ready ports and ready ports of all the existing IPs including crypto cores. Instruction-1 writes 384 bit random number from RNG to the data portion of Buffer. Similarly instruction 9, 17 and 18 can write 512 bit data from KECCAK and 1024 bits from RSA respectively.

D. Signature Checker

The Signature Checker (SC) consists two main parts such as KECCAK hash and RSA block to verify signature of the IPs requested to read or write to MKM. This IP receives the signature from buffer. The signature is the encrypted hash of data. The SC first decrypt it by the RSA block with the public key of requestee IP. The requestee IP is addressed by the source IP address available in CWR. After that SC gets the hash of data. The data is already available in the buffer. If the hash of buffer data is matched with the decrypted data by RSA then the requested transaction will be granted by SC.

III. IMPLEMENTATION & RESULTS

The proposed architecture is implemented in Artix-7 (csg324-100)FPGA using Vivado Tool. The additional hardwares added to the original architecture to protect the keys form major threats as stated in Table I are SC, buffer and the CBI. The signature checker consist of a KECCAK and RSA-1024 which cost 4188 and 31008 slices respectively. The base architecture without blockchain consumes 50k logic cells. The architecture with blockchain to protect severe key threats consumes 95k logic cells which is around 45% of the total logic cells available in Artix-7 FPGA. As shown in Table II articles 5, 8 and 6 proposed dedicated secret key memories which are completely isolated from processor area to prevent software threats but this architecture does not prevent incorrect use, insecure movement and non-destructions issues of keys. If any spoofing IPs or dishonest probes already exist inside the architectures of 5, 8 and 6 and try to read secret key stored in dedicated key memory, the system will allow the key transaction to those malicious nodes. Though the dedicated key memories proposed in these article are physically isolated but can not prevent said incorrect and insecure movement of secret keys. Articles 5, 8 and 6 do not have any facility to investigate the key movement and to prevent non-destruction issue. Amazon Web Server [9] is one of the most recent software based key management architecture which can audit and investigate tracking of secret keys, but it cannot prevent the insecure movement and incorrect use of key. It does not have any signature checking facility on the key request. In our architecture we have introduced dedicated secret key memory which is physically isolated from processor area. Any read write operation on this secret key memory named as Master Key Memory (MKM) is blockchain based. We have observed the usual operations on MKM are related with RNG, HASH, and AES block. The Public and Private keys of all these crypto IPs are already generated in offline by an automatic script during the RTL development. The pre master key is generated by RNG which needs to be written in MKM through buffer as shown in Table II instructions 2, 3, and 17 to 21. Instruction 2 writes random number generated by RNG into buffer. The buffer also stores the public keys of RNG (Source IP) and MKM (Destination). The buffer includes timestamp form TIMER IP, and stores all the current status of Done and Enable pin of available IPs in the proposed design. The instructions 17 to 21 generate signature of the write operation on MKM by RNG.
This signature will also be stored in buffer. This signature will be verified by the Signature Checker IP placed inside Confidential Area as stated in fig. 5. If the signature is matched then the pre master key generated by RNG will be written in MKM, otherwise the transaction will be discarded form the buffer. The other read write requests on MKM are (i) read pre master key by HASH to generate master key (Instruction 7 and 10), (ii) write master keys in MKM (Instruction 9 and 10), (iii) read master key form MKM by hash (Instruction 14 and 15) and (iv) read master key form MKM by AES (Instruction 11 and 13). All these read write operations follows Instruction 17 and 21 for authentic checking of the requestee. The verification process of signature checker IP using the buffer data with system status, timestamp, signature and the pre hash prevents incorrect use and insecure movement of keys. The MKM also delete the keys which are already read to address non-destruction issue. The partitioned memory for secret keys prevents software attacks. The timing diagram of instruction 17, 18 and 19, 20 is shown in fig. 4 and fig. 5 respectively. Table III shows the trade off of latency and resource usage with security features.

**TABLE III: Summery of Trade-off**

| Feature | Role | SW attacks | Prevent crypto instructions | Prevent insecure movement & incorrect use of keys | Audit log for security processor |
|---------|------|------------|-------------------------------|-----------------------------------------------|---------------------------------|
| BRAM    | 0×0 | 0×0        | 0×0                          | 0×0                                          | 0×0                             |
| Clock   | 2×2 | 2×2        | 2×2                          | 2×2                                          | 2×2                             |
| SDRAM   | 20×2 | 20×2 | 20×2                          | 20×2                                         | 20×2                            |

This article proposes a hardware blockchain with a partitioned and dedicated secret key memory which prevents most of the software attacks, insecure key movement, incorrect use, non-destruction use secret key. Apart from this, if breach of keys occurs in the system, the hardware blockchain can investigate previous key transactions. To the best of our knowledge, the FPGA based blockchain to prevent threats stated in Table I is never explored. The additional hardware adopted for blockchain is very nominal in-terms of resource usage and throughput.

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