Increasing Flash Memory Lifetime by Dynamic Voltage Allocation for Constant Mutual Information

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Abstract—The read channel in Flash memory systems degrades over time because the Fowler-Nordheim tunneling used to apply charge to the floating gate eventually compromises the integrity of the cell because of tunnel oxide degradation. While degradation is commonly measured in the number of program/erase cycles experienced by a cell, the degradation is proportional to the number of electrons forced into the floating gate and later released by the erasing process. By managing the amount of charge written to the floating gate to maintain a constant read-channel mutual information, Flash lifetime can be extended. This paper proposes an overall system approach based on information theory to extend the lifetime of a flash memory device. Using the instantaneous storage capacity of a noisy flash memory channel, our approach allocates the read voltage of flash cell dynamically as it wears out gradually over time. A practical estimation of the instantaneous capacity is also proposed based on soft information via multiple reads of the memory cells.

I. INTRODUCTION

Flash memory is ubiquitous on our keychain, in our super-thin laptop, and in the racks of enterprise storage data centers. Unfortunately, Flash memory reliability degrades over time as a function of the amount of charge that is written into and subsequently erased from the memory cell. This degradation (called “wear-out”) can be understood as a time-varying noise whose variance increases with the number of electrons forced into and out of the floating gate by Fowler-Nordheim tunneling. Wear-out becomes worse as the storage density (bits per memory cell) is increased by using denser constellations to store more information. The reliability and lifetime problems associated with these new, higher-density Flash memories have driven research into the use of LDPC codes to improve performance.

Fig. 1 illustrates the device structure of a NAND flash memory cell (i.e., a floating-gate transistor). To store information, a charge level is written to the cell by adding a specified amount of charge to the floating gate through Fowler-Nordheim tunneling by applying a relatively large voltage to the control gate. Actually, charge is written to the floating gate incrementally with feedback, carefully approaching the desired level from below.

To read a memory cell, the charge level written to the floating gate is detected by applying a specified word-line voltage to the control gate and comparing the transistor drain current to a threshold by a sense amp comparator. If the drain current is above the threshold, the charge written to the floating gate was sufficient to prevent the applied word-line voltage from turning on the transistor. The sense amp comparator only provides one bit of information about the charge level present in the floating gate.

The word-line voltage required to turn on a particular transistor is called the threshold voltage. We refer to the variation of threshold voltage from its intended value as the read channel noise. The threshold voltage can vary from its intended value for a variety of reasons. For example, the floating gate can be overcharged during the write operation, the floating gate can lose charge due to leakage in the retention period, or the floating gate can receive extra charge when nearby cells are written.

This paper presents an approach that dynamically scales the amount of charge for each level (i.e. the word-line voltage thresholds for each level) to maintain a constant mutual information over the lifetime of the device. The motivation is to increase lifetime by carefully managing the precious resource of total charge written to the cell. Our approach utilizes read-channel state information that could be provided by variable-precision decoding. Our approach maintains the simplicity of a constant instantaneous storage capacity of the device over its useful lifetime.

The rest of the paper is organized as follows: Sec. II introduces the Flash memory channel model used in this paper. Sec. III presents the main ideas of our dynamic voltage allocation and the numerical results. Sec. IV discusses practical
techniques to estimate the distribution of the actual Flash memory cell using multiple reads. Finally Sec. VIII concludes the paper.

II. FLASH MEMORY CHANNEL MODEL

This section introduces a tractable but also realistic model for Flash memory channel. Following the general approach of [3]–[7] with respect to the case of limited magnitude asymmetric errors, we first design a reasonable noise model and then seek the best possible system for that model. We draw heavily upon the extensive prior theoretical investigations and experimental studies in the semiconductor device research community [8]–[16] to capture the critical components of the time-varying and input-dependent characteristics of NAND Flash memory cells. Our model makes explicit the dependence of the wear-out and retention noise on the total amount of charge written to and subsequently erased from the memory cell. We model the NAND Flash memory cell data storage process as

\[ y = x + n_p + n_w + n_r, \]  

where \( x \) is the threshold voltage level intended to be written to the cell and \( y \) is the threshold voltage when the cell is read. The three noise components in our model are the programming noise \( n_p \), the wear-out noise \( n_w \), and the retention noise \( n_r \), which is described in detail below. Wear-out and retention noise depend explicitly on accumulated charge.

Fig. 2 shows the contributions from each type of noise. We do not include cell-to-cell interference through parasitic capacitive coupling [17] in our model because cell-to-cell interference is a data-dependent process that can be partially mitigated by equalization and pre-distortion [18], [19]. However, the approach can be extended to handle an additional noise term reflecting residual cell-to-cell interference.

A. Programming noise

The programming noise \( n_p \) represents memory cell threshold voltage variation immediately after a brand new cell has been written. The programming noise is approximately Gaussian, but the variance is input-dependent [10], [14]. Letting \( x_i \) be the \( i \)-th voltage level of a Flash cell, our model is given as

\[ f_{N_p}(n_p) = \begin{cases} \mathcal{N}(0, \sigma_p^2) & \text{if } x = x_i, i > 1, \\ \mathcal{N}(0, \sigma_c^2) & \text{if } x = x_1, \end{cases} \]

where \( \sigma_c > \sigma_p \). In other words, the erased state \( x_1 \) has a larger noise variance.

B. Wear-out noise

Flash memory program/erase (P/E) cycling causes damage (i.e., wear-out) to the tunnel oxide of Flash memory cells in the form of charge trapping in the oxide and interface states [8], [11], [20], [21]. The memory cell wear-out caused by P/E cycling is proportional to the number of electrons tunneling through the gate oxide that is further proportional to the programmed threshold voltage level. Memory cell damage caused by P/E cycling is a function of the accumulated programmed threshold voltages over these P/E cycles [21].

Let \( V_c \) denote the voltage of the erased state, \( V^{(j)}_p \) denote the voltage of programmed state during the \( j \)-th P/E cycle, and \( N \) denote the total number of P/E cycles. Define the voltage accumulated over \( N \) writes as

\[ V_{acc} = \sum_{j=1}^{N} (V^{(j)}_p - V_c). \]

Based upon the discussion and measurement results presented in [13], [22], we model the wear-out noise \( n_w \) in [11] as a Laplace \((0, \lambda)\) distribution with density \( f(n_w) = \frac{\lambda}{2} e^{-\lambda n_w} \) with \( \lambda = C_w + A_w \cdot (V_{acc}/V_{max})^{k_1} \) where constants \( C_w, A_w \) and \( k_1 \) are technology dependent with typical values around \( 1.26 \times 10^{-3}, 1.80 \times 10^{-2} \) and 0.62, respectively.

C. Retention noise

Retention noise \( n_r \) models the degradation of the threshold voltage integrity due to charge leakage after it is written. Interface trap recovery and electron detrapping [24]–[26] gradually reduce memory cell threshold voltages. The degradation becomes worse as \( V_{acc} \) becomes larger. Based upon the discussion and measurement results in [11], [24], the noise \( n_r \) in [11] approximately follows a Gaussian distribution \( \mathcal{N}(\mu_r, \sigma_r^2) \), where the parameters \( \mu_r \) and \( \sigma_r \) are both time-varying and voltage-dependent. Our model has mean \( \mu_r \) given as

\[ \mu_r = -x \ln \left( 1 + \frac{t}{t_0} \right) \frac{A_r}{V_{max}} \left( \frac{V_{acc}}{V_{max}} \right)^{k_1} + B_r \left( \frac{V_{acc}}{V_{max}} \right)^{k_2}, \]

and the variance \( \sigma_r^2 \) given as

\[ \sigma_r^2 = 0.1 x \ln \left( 1 + \frac{t}{t_0} \right) \frac{A_r}{V_{max}} \left( \frac{V_{acc}}{V_{max}} \right)^{k_1} + B_r \left( \frac{V_{acc}}{V_{max}} \right)^{k_2}, \]

where \( x \) is the target threshold voltage being programmed into the memory cell. The exponents \( k_1 \) and \( k_2 \) depend on the
Our model channel has been studied in the context of multiple-user communication with time-varying parameters. A similar channel model has been chosen to be of use during its “after life”, but the goal is to delay this as long as possible. We use information theory to dynamically tune the voltage levels and variable rate coding to decrease the rate as the instantaneous capacity decreases. However, both USB drives and enterprise storage applications tend to assume that the instantaneous storage capacity remains constant over the lifetime of the device.

Our approach recognizes that the device needs to maintain a specified instantaneous storage capacity and designs the system to maximize the lifetime over which that capacity is maintained. This does not preclude the use of variable-rate coding to allow the device to be of use during its “after life”, but the goal is to delay this as long as possible. We use information theory to dynamically tune the voltage levels to maintain only the needed margin, minimizing \( V_{acc} \). This achieves a longer average lifetime. The extremely large margin common in the beginning of a cell’s life is not needed (since the LDPC code is in place) and that excess margin comes at the cost of a shorter lifetime.

To illustrate this, take a Flash chip with 4-level cells as in Fig. 2 and a rate-8/9 error correction code as an example. Suppose the needed margin of 0.12 bits requires the instantaneous capacity to be above 1.9 bits. For this example, the technology-dependent parameters are chosen as follows: \( A_w = 1.8 \times 10^{-4}, C_w = 1.26 \times 10^{-3}, A_r = 7.0 \times 10^{-4}, B_r = 4.76 \times 10^{-3}, V_{max} = 16 \). The voltage levels are set to be \( \{2.8, 5.2, 6.4, 7.86\} \). The time constant is set to \( t_0 = 1 \) in units of hours. The state-dependent Gaussian noise variances are chosen to be \( \sigma_p = 0.05 \) and \( \sigma_r = 0.35 \).

For a retention time of 1 year (\( t = 8760 \) hours), the red curve in Fig. 3 is the baseline for fixed voltage levels over the lifetime. The baseline voltage levels are chosen such that the instantaneous capacity drops to 1.9 bits at a typical lifetime of 3000 P/E cycles for a 4-level Flash cell. Fig. 3 also shows the instantaneous capacity using our dynamic voltage level.
Our dynamic-voltage-level approach determines at regular (though infrequent) intervals how much to increase the voltage levels. At each channel assessment period, we can numerically solve the general optimization problem of where to place the least growth in levels. At each channel assessment period, we can numerically solve the general optimization problem of where to place the least growth in levels.

IV. ASSESSMENT OF WEAR-OUT AND RETENTION NOISE

Fig. 4. \( \alpha \) vs. P/E cycle at 1 year retention time.

Approach. The voltage levels are scaled by a single parameter \( \alpha \), adjusted after every 100 P/E cycles to attain instantaneous capacity of 1.92 bits (slightly higher than the threshold to provide extra margin) until the voltage levels become the same as our baseline (\( \alpha = 1 \)). This single parameter scheme improves the lifetime from 3000 to 5400 P/E cycles: an 80% improvement in this example.

Fig. 4 compares \( \alpha \) as a function of P/E cycles between the varying level scheme and the baseline. The initial \( \alpha \) is set to 0.28 and as the device wears out, \( \alpha \) is gradually increased to match the desired mutual information margin every 100 P/E cycles. As illustrated in Fig. 4 the lifetime improvement is significant since a brand new Flash cell only needs 28% of the fixed voltage levels to achieve sufficient amount of instantaneous capacity. Fixed voltage levels waste 70% of the early voltage, needlessly damaging the Flash cell. We emphasize that this is only an initial illustration. Investigation of a variety of ways to improve performance further including optimizing the frequency of charge level adjustment and more carefully optimizing each of the charge levels is ongoing work.

Fig. 5. Histogram of 9000 Flash cells with threshold voltage distributions and memory-sensing word-line voltages as shown in Fig. 3 available in Flash memory utilizing multiple reads to obtain soft information for decoding LDPC codes.

Figs. 5 (a) and (b) indicate that the degree of wear-out faced by a page in Flash memory can be estimated from such a histogram with enough accuracy to support the dynamic voltage level approach. We note that in [30] the author uses a similar histogram approach to estimate the threshold voltage distribution for the purpose of choosing the best possible quantization thresholds according to [29]. In [30], twelve histogram bins were sufficient to estimate with high precision the means and variances of a mixture of four Gaussians. Thus, the method of distribution estimation from the histogram is sound.

While information theoretic analysis provides the foundation for this approach, our implementation is practical. The histogram is generated immediately after a write to avoid confusion with retention loss effects. Then, whether and how much to increase voltage levels can be determined as a function of how many threshold voltages are outside of the “correct” bins. This approach can be applied on a block-by-block basis so that constant mutual information can be maintained despite the large variations that have been observed between blocks.

The histogram approach can also identify and largely mitigate the mean-shift portion of retention loss. Comparing Figs. 5 (b) and (c) shows the mean shift due to retention loss as a left-shift of the most populated bins, which affects LDPC decoding. This was also observed in [30], where a second cycle of memory sensing follows the histogram-estimated means and variances to obtain optimal limited-precision soft information. We explore an alternative approach that uses the obtained histogram to adjust how likelihood ratios are assigned to the
histogram bins.

The example of Figs. 2 and 5 only considered three quantization thresholds between two adjacent storage levels for simplicity. Commercial NAND Flash memory chips already support more levels. The Samsung 21nm 2 bits/cell chip can support six quantization thresholds between two adjacent storage states [31]. Thus we are confident that the mechanism for generating sufficiently rich histograms will exist as a matter of course in future Flash memory systems.

V. Conclusion

Using information theory, we have introduced a novel dynamic voltage allocation method to increase the lifetime of a Flash storage device. A channel model based on voltage-dependent Gaussian noise and Laplace noise is used to demonstrate the numerical results, our idea is applicable to general Flash memory channel model. For the parameters chosen in this paper, the dynamic voltage allocation almost doubles the lifetime of a 4-level Flash memory cell. We expect additional lifetime extension for a general Flash memory channel model.

In order to obtain the (approximate) mutual information of the Flash memory channel, the noise distribution must be available. We propose estimating the noise distribution by using the quantized soft information obtained during the page-reading process, which is an emerging feature in modern Flash memory devices.

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