Abstract

Difficulties in obtaining high-performance p-type transistors and gate insulator charge-trapping effects present two major challenges for III-V complementary metal-oxide semiconductor (CMOS) electronics. We report a p-GaAs nanowire metal-semiconductor field-effect transistor (MESFET) that eliminates the need for a gate insulator by exploiting the Schottky barrier at the metal-GaAs interface. Our device beats the best-performing p-GaSb nanowire metal-oxide-semiconductor field effect transistor (MOSFET), giving a typical sub-threshold swing of 62 mV/dec, within 4% of the thermal limit, on-off ratio $\sim 10^5$, on-resistance $\sim 700$ kΩ, contact resistance $\sim 30$ kΩ, peak transconductance $1.2 \ \mu$S/μm and high-fidelity ac operation at frequencies up to
10 kHz. The device consists of a GaAs nanowire with an undoped core and heavily Be-doped shell. We carefully etch back the nanowire at the gate locations to obtain Schottky-barrier insulated gates whilst leaving the doped shell intact at the contacts to obtain low contact resistance. Our device opens a path to all-GaAs nanowire MESFET complementary circuits with simplified fabrication and improved performance.

**Keywords:** nanowire, transistor, MESFET, Schottky gate, p-GaAs

Modern integrated circuits are heavily reliant on complementary circuit architectures featuring both $p$-type and $n$-type transistors to minimise power consumption. Continued miniaturisation spurred the development of nanowire CMOS, at first using carbon nanotubes and Si nanowires, and more recently focussing on III-V nanowires integrated on Si towards achieving high performance at low cost. Progress for $n$-type III-V nanowire transistors has fared better than for $p$-type. Near-thermal limit gating has been obtained for $n$-InP, $n$-InGaAs, and $n$-AlGaAs/GaAs nanowires, with integration on Si substrates and GHz operation also demonstrated. Several significant challenges have impeded progress on the $p$-type counterparts including lower intrinsic carrier mobility and difficulties in the growth, doping and fabrication of high quality gates and ohmic contacts.

Candidate materials for $p$-type III-V nanowire transistors include GaSb, GaAs, InAs, InGaAs, InP and InSb. The In-based materials are hard to deploy and often ambipolar because the $p$-type doping needs to compete against sub-surface electron accumulation arising from surface-state pinning of the surface Fermi energy at the conduction band edge and/or a relatively small band-gap. GaSb is more favourable for $p$-type nanowire transistors because it is intrinsically $p$-type due to native antisite defects. Dey et al. reported a single InAs/GaSb nanowire CMOS inverter circuit featuring a horizontally-oriented GaSb $p$-MOSFET with sub-threshold swing $S = 400$ mV/dec, peak transconductance $g_m = 3.4 \, \mu S/\mu m$, on-off ratio $\sim 10^{18}$, on-resistance $R_{on} > 1.2 \, M\Omega$ and operation frequency up to 10 kHz without significant fidelity loss. Babadi et al. obtained improved $R_{on} \sim 26 \, k\Omega$ from a GaSb nanowire with moderate Zn doping albeit with some loss in sub-
threshold swing (820 mV/dec). Vertical p-GaSb MOSFET arrays have since been developed towards scale-up and applications;\textsuperscript{21,22} we will return to these later. A complexity with using GaSb nanowires is the need to grow on GaAs or InAs stems to achieve high quality and yield.\textsuperscript{23}

Figure 1: Device Structure. a Schematic diagram and b Scanning electron micrograph of our p-GaAs nanowire MESFET structure. It features a \( \sim 120 \) nm diameter GaAs nanowire with an undoped core (light green in a) and a nominally 30 nm thick Be-doped shell (dark green). The nominal shell acceptor density \( N_A = 1.5 \times 10^{19} \) cm\(^{-3}\). The nanowire is thinned near the middle of its length via a lithographically patterned wet-etch to facilitate Schottky-gating as described in the text. The device has three electrodes (yellow): source (S), drain (D) and a Schottky-gate (G). The typical gate length for our devices is 600 – 750 nm. The scale bar in b represents 1 \( \mu \)m.

Here we report on the development of a p-GaAs nanowire metal-semiconductor field-effect transistor (MESFET) with sub-threshold swing \( S = 62 \) mV/dec, normalised peak transconductance \( g_m = 1.2 \mu S/\mu \)m, on-off ratio \( 10^{5} \), on-resistance as low as 715 k\( \Omega \), contact resistance \( \sim 30 \) k\( \Omega \), a field-effect hole mobility \( \sim 5 \) cm\(^2\)/Vs and high-fidelity operation at frequencies up to 10 kHz. Two notable aspects of GaAs nanowires are the capacity for
direct self-catalysed growth, including on Si substrates, and surface-states that pin the surface Fermi energy to mid-gap giving metal-semiconductor interfaces with a substantial Schottky barrier, typically \( \sim 0.5 \text{ eV} \). The latter can be both an advantage and a disadvantage. On the positive side, it enables us to make Schottky gates. This simplifies the device processing as the gates become self-insulating, removing the need for an added insulator layer, e.g., \( \text{Al}_2\text{O}_3 \) or \( \text{HfO}_2 \). The disadvantage is the difficulty involved in achieving low-resistance ohmic contacts to \( p \)-GaAs nanowires. Low resistance contacts (\( \sim 30 \text{ k}\Omega \)) can be achieved using GaAs nanowires with a heavily Be-doped shell, however, such heavy doping means conventional metal-oxide gating fails. Here we demonstrate that this problem can be overcome by carefully etching the nanowire to reduce the local Be-doping density at the locations where gates are patterned prior to depositing gate metal directly on the nanowire surface. Our approach provides both strong, low-leakage gating and low contact resistance simultaneously. It opens a path to high performance \( p \)-GaAs nanowire transistors without oxide gate-insulators, which entail substantial issues with charge trapping and gate hysteresis. Our \( p \)-GaAs nanowire MESFETs could potentially be paired with \( n \)-InGaAs, \( n \)-GaAs or \( n \)-AlGaAs/GaAs MESFETs to produce high-performance oxide-free complementary circuit architectures.

A controlled near-monolayer accuracy etch for GaAs nanowires

Figure 1 shows a schematic of the \( p \)-GaAs nanowire MESFET structure and a scanning electron micrograph of a completed device. The nanowire is grown as an undoped core with a heavily Be-doped shell (see Methods for full details), however, this does not mean the Be-dopants remain confined to the shell alone. Be has a high diffusion constant in GaAs, which means significant amounts of the Be diffuse into the otherwise-undoped core. The result is a roughly constant doping density in the shell and a monotonically decreasing doping density moving into the core; for a much higher doping density than we use, this can result in a fully doped core. This aspect of the doping profile is crucial to properly understanding our device. It also underpins our ability to make devices with high repeatability and yield given a well-engineered nanowire.
Figure 2: Controlled etching of the Be-doped nanowire shell. Scanning electron micrographs of a GaAs nanowire etched with 1 : 1 : 250 H$_3$PO$_4$:H$_2$O$_2$:H$_2$O for a self-aligned etch using the source/drain contacts as etch mask and b patterned etch with PMMA resist etch mask demonstrating issues with metal-assisted etching for this process. Both scale bars represent 1 µm. c Plot of etched region diameter $\phi$ vs etch time $t_{etch}$ for the 1 : 1 : 250 H$_3$PO$_4$:H$_2$O$_2$:H$_2$O etchant solution on a GaAs nanowire without source/drain contacts.
etch process. We leave the shell intact at the source and drain contacts as shown in Fig. 1 to minimise the contact resistance. The key is then to thin the nanowire and thereby reduce the doping level at the gate location just enough for the channel to become electrostatically gateable in the region where the gates are placed. This requires a careful balance – etch insufficiently and the gate either fails to function and/or leaks current to the nanowire; etch too much and the on-resistance become undesirably high and the on-off ratio falls.

Note that it is vital that some doping remains in the etched region to counteract the GaAs surface-states, which pin the Fermi energy at mid-gap, and then provide the free holes required to achieve conduction through the etched channel segment. The gate-etch is thus administered completely ignoring the location of the core-shell boundary. Indeed, for our optimum devices below, we completely etch the shell and somewhat into the core.

We used a phosphoric acid etch \( 1 : 1 : 250 \, \text{H}_3\text{PO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O} \), inspired by Mori and Watanabe’s work on slow etching of GaAs wafers for microwave devices to obtain a highly-controllable nanowire gate-etch without deleterious effects. We made attempts with other etchants, e.g., sulfur-oleylamine, which has previously shown near-monolayer etch control for III-Vs, but only the phosphoric acid etchant proved compatible with other aspects of nanowire device fabrication (see Supplementary Information for further discussion). We note that a two-step digital etch process could also be applied; it may provide more precision than our \( \text{H}_3\text{PO}_4 \) etch but our 30–50 nm etch depth may also make it a high time-cost option.

With this in mind, one could suggest using a thinner shell and increasing the doping density to avoid loss in contact performance. The issue here is that this drives dopant diffusion into the core, as discussed above, requiring a deeper gate-etch to achieve a functional doping level at the gated segment. This defeats the purpose of thinning the shell in the first place.

An important consideration when performing the gate-etch for a GaAs nanowire MESFET is the stage where the etch is performed. The simplest option is to pattern the source and drain contacts first and use these as a mask for a ‘self-aligned’ gate-etch. The outcome is shown in Fig. 2a, where the nanowire etches much faster local to the contact edges than
near the middle, presumably due to metal-assisted etching. This is supported by the fact that the nanowire segment off to the left in Fig. 2a, which was also exposed to the etchant, is not as heavily etched. We avoided this problem by performing the etch prior to contact deposition, using EBL-patterned polymethylmethacrylate (PMMA) resist as the etch mask. This gives the more even gate-etch shown in Fig. 2b, and was the etch process used to obtain the device shown in Fig. 1b. The fact that the nanowire is sitting on a substrate may slightly reduce the etch rate at the bottom of the nanowire, which could produce a slight inhomogeneity in doping density on this side. We do not expect this effect to be substantial given the same issue did not adversely affect our earlier horizontal wrap-gate nanowire devices, where a similar wet-etch was administered, or appear to be detrimental to the performance of the devices made here. This issue would be eliminated entirely in the vertical orientation preferred for applications.

Figure 3: p-GaAs nanowire MESFET dc performance. a Source-drain current $I_{sd}$ vs source-drain bias $V_{sd}$ at four different top-gate voltages $V_{tg} = +0$ V (solid blue), +0.5 V (dashed green), +1.0 V (dotted red) and +1.5 V (thick black) for a p-GaAs MESFET with 40 s gate-etch at temperature $T = 300$ K. b/c $I_{sd}$ vs top-gate voltage $V_{tg}$ at b $T = 300$ K and c $T = 4$ K with sweep to positive $V_{tg}$ (solid) and return to $V_{tg} = 0$ V (dashed) both shown. The thermal limit sub-threshold swings at $T = 300$ K (59.6 mV/dec) and $T = 4$ K (0.8 mV/dec) are shown as the dashed black line in b and the dot-dashed black line in c for reference. The gate-voltage separation between up- and down-sweeps at the sub-threshold midpoint $I_{sd} = 10^{-10}$ A is 80 mV for b and 40 mV for c. The apparent hysteresis in the off-state for b and c is an experimental artefact explained in the Supplementary Information.

Figure 2c shows a plot of the etched segment diameter $\phi$ versus etch time $t_{etch}$ for the
phosphoric acid etch. The diameter was measured by post-etch scanning electron microscopy, with results averaged over 24 separate nanowires for each $t_{etch}$. The etch is well controlled for $t_{etch} < 100$ s. At longer $t_{etch}$ the nanowire becomes sufficiently thin that the etch acts anisotropically, producing breaks and substantial thickness variations. The long $t_{etch}$ behaviour is not problematic since we only aim to slightly thin the nanowire and this requires significantly less than $t_{etch} = 100$ s. Some readers may note a slight gradient change to the linear trend in Fig. 2c at approximately 30 s. Given a nominal shell thickness of 30 nm and a typical etch rate of 1.1 nm/s, this likely arises from the etch crossing the core-shell boundary.

![Figure 4: p-GaAs nanowire MESFET ac performance. a-c Plots of applied gate voltage $V_g$ (blue/top panel) and source-drain current $I_{sd}$ (red/bottom panel) vs time $t$ for gate drive frequencies $f$ of a 100 Hz, b 1 kHz and c 10 kHz. d Source-drain current $I_{sd}$ vs gate voltage $V_g$ for increasing $V_g$ (red) and decreasing $V_g$ (green) demonstrating the minimal gate hysteresis in this device for $f = 100$ Hz operation (n.b. hysteresis is sufficiently small that the green trace is hidden by the red trace in Fig. 5d).](image)

Obtaining high-performance $p$-GaAs nanowire MESFETs with controlled gate-segment etching The challenge in the fabrication is to identify the appropriate $t_{etch}$ needed
to optimise electrical performance. Optimum performance was obtained for $t_{\text{etch}} = 40$ s, yielding the electrical characteristics in Fig. 3. Figure 3a shows $I_{sd}$ versus $V_{sd}$ at four different top-gate voltages $V_{tg}$. The $I_{sd}$ versus $V_{sd}$ characteristic is relatively linear for $V_{tg} = 0$ V, with slope corresponding to an unbiased channel resistance $R_{on} \sim 700$ kΩ. The typical contact resistance at $T = 300$ K for these nanowires is $29 \pm 15$ kΩ. An increasingly positive $V_{tg}$ results in reduced $I_{sd}$ at a given $V_{sd}$, as expected for a p-MESFET, without severe degradation in source-drain characteristics. Figure 3b shows $I_{sd}$ versus $V_{tg}$ at $V_{sd} = 100$ mV at $T = 300$ K. We obtain remarkably strong gating with a sub-threshold swing of $62 \pm 7$ mV/dec at $T = 300$ K. This is within 4% of the room-temperature thermal limit of $59.6$ mV/dec, which is indicated by the black dashed line in Fig. 3b for comparison. The $T = 300$ K data has on-off ratio $10^{5.1}$, threshold voltage $V_{th} = +1.3$ V and relatively low hysteresis; the up and down traces in Fig. 3b are separated by only 80 mV in $V_{tg}$ at $I_{sd} = 10^{-10}$ A. We will comment further on normalised on-current, peak transconductance and field-effect mobility in our benchmarking comparison to other devices below.

**Potential for studying hole-based quantum devices** Our device architecture may also be useful for quantum device applications. A concern is that gate-etch might cause conduction to freeze-out before sufficiently low temperature for observing quantum effects is attained. To test this we repeated the $I_{sd}$ versus $V_{tg}$ characterisation after cooling to $T = 4$ K, as shown in Fig. 3c. The on-resistance increases slightly to $R_{on} \sim 1.6$ MΩ consistent with the etched channel segment being non-metallic. Strong gating is retained but the sub-threshold swing of $15 \pm 7$ mV/dec is not as close to the respective thermal limit ($0.8$ mV/dec at $T = 4$ K – black dot-dashed line in Fig. 3c for comparison). This is a positive outcome for quantum device applications, as very steep gate response makes it harder to control/study quantum effects, e.g., 1D conductance quantization\cite{46-48} and can increase noise as smaller gate voltage fluctuations give a stronger effect. The on-off ratio at $T = 4$ K remains high ($10^{4.6}$) and the threshold voltage $V_{th} = +1.1$ V shifts slightly closer to zero, consistent with reduced ionized dopant density due to freeze-out. The hysteresis is
also improved significantly upon cooling. Optimisation of the gate-etch for quantum device applications will be subject of a separate study.

Comparison of performance with $p$-GaSb nanowire MOSFETs The most notable competitor for our devices is the $p$-GaSb nanowire MOSFET, which is the current device of choice for complementary architectures featuring III-V nanowires. We will make this comparison in two stages. First we will compare to horizontally-oriented single nanowire devices to make a direct ‘like-for-like’ performance comparison. We will then benchmark against more recently developed vertical nanowire array devices to consider prospects for scale-up and applications.

Dey et al.\textsuperscript{19} previously reported single InAs/GaSb nanowire CMOS inverter oriented horizontally on a SiO$_2$-on-Si substrate. Their $p$-GaSb MOSFET featured a nanowire with diameter 65 nm and a gate length of \~500 nm, giving sub-threshold swing $S = 400$ mV/dec, peak transconductance $g_m = 3.4 \mu S/\mu m$, on-off ratio \~$10^{1.8}$ and a normalised on-resistance $R_{on,n} = 212 \Omega$.mm at room temperature. Babadi et al.\textsuperscript{20} improved $R_{on,n}$ to 3.9 $\Omega$.mm by moderate doping with Zn coupled with a reduced gate length of 200 nm. This improved the peak transconductance to $g_m = 80 \mu S/\mu m$ but also led to a significantly reduced sub-threshold swing of 820 mV/dec.\textsuperscript{20} A measurement of hole mobility was not provided in Dey et al.\textsuperscript{19} but Babadi et al.\textsuperscript{20} obtained a peak hole mobility of 153 cm$^2$/Vs.

Our sub-threshold swing of 62 mV/dec significantly surpasses that obtained by Dey et al. and Babadi et al. above. Our peak transconductance $g_m = 1.3 \mu S/\mu m$ (normalised to channel circumference) is comparable with that obtained by Dey et al.\textsuperscript{19} Our normalised on-resistance is 137 $\Omega$.mm, which is 65% lower than the device reported by Dey et al. but \~35 times higher than Babadi et al.\textsuperscript{20} Improvement in our normalised on-resistance should be possible by reducing the channel length and/or increasing the shell doping density to improve the contact resistance and then compensating with increased gate-etch depth to maintain gate-performance. The hole mobility is challenging to calculate for our device due to the absence of an oxide, but we can provide a reasonable estimate. The gate insulator in
our device is the depletion region at the GaAs surface arising from surface states. Casadei et al.\textsuperscript{37} calculate the surface depletion width as a function of doping density for nanowire radii of 40 nm and 100 nm. They obtain a depletion width of 7 nm for our acceptor density $N_A = 1.5 \times 10^{19} \text{ cm}^{-3}$ with negligible radii dependence, i.e., the depletion width values as a function of radii converge at high $N_A$.\textsuperscript{37} To obtain the top-gate capacitance we use a coaxial-capacitor model and reduce the resulting capacitance by 20% to account for the gate not covering the bottom of the nanowire where it sits on the substrate. Assuming the standard value for GaAs dielectric constant of 12.9 and the measured gate-length of 650 nm for the device with $t_{etch} = 40$ s, we obtain a gate capacitance of 1.8 fF. This in turn gives a hole mobility of 5.6 cm$^2$/Vs. This is lower than the mobility obtained by Babadi et al.\textsuperscript{20} from devices with less than a third of the gate-length and much lower on-resistance. More competitive mobilities are probably attainable for $p$-GaAs MESFETs with some optimisation of our design.

Figure 4 shows the frequency response of our $t_{etch} = 40$ s $p$-GaAs MESFET. A square-wave top-gate voltage $V_{tg}$ (blue trace/top panels) is applied at frequency $f = 100$ Hz, 1 kHz and 10 kHz producing a square-wave source-drain current $I_{sd}$ response (red trace/bottom panels) in each case. The fidelity for our device remains excellent up to 10 kHz, where the leading edge begins to evolve a slight rounding. The high-frequency fidelity loss does not arise from the device acting as a low-pass filter – the 1.8 fF gate capacitance estimated above combined with the 715 kΩ channel resistance gives a roll-off frequency of 123 MHz. That said, radio-frequency operation is well-known to require careful capacitance management of the device and external circuit, and is commonly achieved for nanowire transistors by moving to vertical nanowire array structures.\textsuperscript{6,13} The fidelity loss we see likely arises from a mixture of instrument/circuit limitations and some gate-semiconductor interface effects; there will inevitably be some GaAs native oxide at the gate interface because the processing is not carried out in a fully oxygen-free environment. Charge trapping by oxide at gate interfaces is a well-known contributor to gate hysteresis in nanowire transistors.\textsuperscript{31–33} The
data in Fig. 3b indicates low hysteresis under dc operation; this performance is retained under ac conditions also. Figure 4d shows the device response to a triangle-wave $V_{tg}$ signal between 0.0 and +0.5 V at $f = 100$ Hz with the up-sweep to +0.5 V data in green and the down-sweep data in red. Up and down sweeps are separated by a constant offset at higher frequencies (see Supplementary Fig. S3). We attribute this to a displacement current induced by the high gate-sweep rate. Regarding benchmarking of the frequency performance against $p$-GaSb, Dey et al.\textsuperscript{19} only present characteristics for their inverter and not their $p$-GaSb MOSFET alone unfortunately. However, their inverter frequency response will be limited by the slowest component, which is inevitably the $p$-GaSb MOSFET, giving some indication of its performance. The frequency performance of our $p$-GaAs MESFET appears at least as good by this comparison – a more conclusive benchmarking would require a careful comparative study beyond the scope of the current work.

A notable aspect of our devices is the low gate leakage current despite the lack of an oxide gate insulator. We obtain gate leakage current $I_{tg} < 50$ pA over the entire operating range for devices with $t_{etch} = 40$ s. The gate-etch is essential to obtaining low gate leakage; for $t_{etch} = 0$ s we get $I_{tg} \sim 10$ nA at $V_{tg} = +2$ V (see Supplementary Fig. S4), as expected, since in this instance the heavy shell doping makes the metal gate electrode into an ohmic contact.\textsuperscript{49} For $t_{etch} > 40$ s we get 100% yield of leakage-free gates albeit with reduced gate performance – Data obtained for $t_{etch} = 50$ s and 60 s corresponding to Figs. 3 and 4 is presented in Supplementary Figs. S5 – 8 to demonstrate this. At $t_{etch} = 40$ s we get excellent performance but the yield of leakage-free gates is only $\sim 70\%$ and drops sharply for shorter etch times. This makes $t_{etch} = 40$ s optimum on both performance and yield-to-performance measures, however, this would naturally vary for different growth conditions and require optimisation on a growth-batch basis. This performance compares very well to other single nanowire MESFETs, for example, Noborisaka et al.\textsuperscript{35} report leakage currents between 1 and 700 pA for a $n$-InGaAs device, Fortuna & Li\textsuperscript{34} report 20 pA to 30 nA for a $n$-GaAs device, and Liu et al.\textsuperscript{50} report $10 – 20$ pA for a $p$-Zn$_3$P$_2$ device.
Prospects for scale-up Development for practical applications tends to focus on vertical nanowire arrays over horizontal single nanowire devices for reasons of higher current carrying capacity, improved gate coupling and scalability, and capacitance management for high-frequency operation. A key aspect in vertical array devices is that the gate-length is no longer constrained by lithography and instead controlled by layer thicknesses during processing, facilitating scaling to sub-100 nm gate length. This pathway has already been taken for \textit{p}-\textit{GaSb}, with the single horizontal nanowire devices of Dey et al. and Babadi et al. translated into vertical nanowire array structures by, e.g., Svensson et al. and Jönsson et al. The nanowire III-V CMOS on Si inverter structures by Jönsson et al. represent the state-of-the-art in the field and feature a \textit{p}-\textit{GaSb} device containing an array of 144 nanowires with 350 nm pitch, 40 nm diameter and 70 nm gate length. These transistors give sub-threshold swing 273 mV/dec, normalised on-resistance 5.9 Ω.mm and peak transconductance 74 µS/µm. The on-resistance and peak transconductance are superior, as one would expect for an array. Our sub-threshold swing is better, but we have to acknowledge that this metric is often compromised slightly in array structures by wire-to-wire variations. Benchmarking on ac operation is difficult because such data is limited for \textit{p}-\textit{GaSb} array transistors. Svensson et al. demonstrate ac operation of an inverter featuring \textit{n}-\textit{InAs} and \textit{p}-\textit{GaSb} vertical nanowire array transistors at 1 kHz with good fidelity but report significant distortion at higher frequencies due to parasitic capacitance issues. These issues are more related to the vertical nanowire array layout than the nanowire channel itself; at this point the only comment we can make is that our \textit{p}-\textit{GaAs} nanowire performance does not indicate that scale-up to arrays for high frequency operation would be obviously problematic.

Potential for complementary GaAs nanowire MESFET circuits Looking forwards, an interesting consideration is the scope for complementary circuits featuring only (In,Al)GaAs nanowire MESFETs, which would require an \textit{n}-channel device to complement the \textit{p}-\textit{GaAs} design we present here. We see several alternatives. The first is a pure GaAs implementation. Fortuna and Li reported a \textit{n}-\textit{GaAs} nanowire MESFET featuring a nanowire
grown epitaxially along the surface of a (100)GaAs substrate. Their device gave strong electronic performance with sub-threshold swing $S = 150$ mV/dec, on-off ratio $\sim 10^2$ and low contact resistance $R_c \sim 40$ kΩ. Noborisaka et al.\textsuperscript{35} reported an $n$-InGaAs nanowire MESFET with sub-threshold swing $S = 200$ mV/dec, on-off ratio $\sim 10^3$ and low channel resistance $R_{on} \sim 100$ kΩ. More recently, Morkötter et al.\textsuperscript{11} demonstrated a delta-doped GaAs-AlGaAs core-shell nanowire $n$-MESFET with $S = 70$ mV/dec, on-off ratio exceeding $10^4$ and $R_c \sim 30$ kΩ. With the latter, complementary circuits could be made on Si substrates using ‘pick and place’ micro-manipulation techniques. An exciting alternative would be to grow the GaAs nanowires directly on Si by template-assisted selective epitaxy,\textsuperscript{51} although a challenge here would be doping of separate GaAs nanowires to be deterministically $n$– or $p$-type.

We demonstrated a $p$-GaAs nanowire MESFET with strong electronic performance by taking a GaAs nanowire with an undoped core and heavily Be-doped shell and carefully etching the nanowire at the gate location to enable a Schottky-gate without compromising on contact resistance. We obtain a sub-threshold swing of $62 \pm 7$ mV/dec, within 4% of the room-temperature thermal limit, on-off ratio $\sim 10^5$, on-resistance $\sim 700$ kΩ and typical contact resistance $\sim 30$ kΩ. Accounting for nanowire diameter, we obtain a normalised on-resistance of $137 \, \Omega \cdot \text{mm}$ and peak transconductance of $g_m = 1.3 \, \mu \text{S} / \mu \text{m}$. We estimate a field-effect hole mobility of $\sim 5 \, \text{cm}^2 / \text{Vs}$ for our device. Our overall single MESFET performance is competitive with that obtained for single horizontal $p$-GaSb nanowire MOSFETs,\textsuperscript{19,20} and suggests that scale-up to vertical nanowire transistor arrays may lead to devices that could potentially compete well with $p$-GaSb vertical nanowire array transistors.\textsuperscript{21,22} Our $p$-GaAs MESFETs show good square-wave fidelity for frequencies up to 10 kHz, comparable to single horizontal $p$-GaSb nanowire MOSFETs.\textsuperscript{19} The ability to eliminate the gate oxide in our device results in strong gating and reduced issues with charge-trapping effects, e.g., gate hysteresis. Our $p$-GaAs MESFETs show strong potential for combination with high-performance $n$-type (In,Al)GaAs MESFETs\textsuperscript{11,34,35} towards nanowire complementary circuit
applications, perhaps even ultimately integrated monolithically on Si using templated epitaxy techniques.\textsuperscript{51}

Methods

The GaAs nanowires were self-catalysed\textsuperscript{52} and grown by molecular beam epitaxy on (111)Si.\textsuperscript{37} The undoped core was grown at 630°C using As\textsubscript{4} and a V/III flux ratio of 60 for 30 – 45 min. The Be-doped shell was grown at 465°C using As\textsubscript{2} and a V/III ratio of 150 for 30 min, giving nanowires with shell acceptor density \( N_A = 1.5 \times 10^{19} \) cm\(^{-3} \), diameter 120 ± 20 nm and length 5 – 7 \( \mu \)m. These nanowires are the highest doping density from earlier work on contacts to \( p \)-GaAs nanowires.\textsuperscript{28} The nanowires are pure zincblende crystal phase but may have short wurtzite segments at the ends;\textsuperscript{26} these wurtzite segments will be buried under the source/drain contacts. Nanowires were dry-transferred to a pre-patterned HfO\textsubscript{2}/SiO\textsubscript{2}-coated \( n^+ \)-Si substrate for device fabrication. The heavily-doped substrate was used as a global back-gate for control studies. The source and drain contacts were defined by electron-beam lithography (EBL) and thermal evaporation of 200 nm of 1 : 99 Be:Au alloy (ACI alloys) and were not thermally annealed.\textsuperscript{28} The thin GaAs native oxide was removed at the contact interfaces by a 30 s etch in 10% HCl solution immediately prior to contact deposition. The 20/180 nm Ti/Au gate electrode was formed in a separate round of EBL and metal deposition. Electrical measurements were performed at temperature \( T = 300 \) K in ambient atmosphere and at \( T = 4 \) K by immersion in liquid helium. The source-drain current \( I_{sd} \) was measured using a Keithley 6517A electrometer for the dc measurements in Fig. 3 and using a Femto DLP-CA-200 pre-amplifier connected to a National Instruments USB-6216 data acquisition system for the ac measurements in Fig. 4. Keithley K2410 voltage sources supplied the source-drain voltage \( V_{sd} \), top-gate voltage \( V_{tg} \) and back-gate voltage \( V_{bg} \) (back-gate used in control studies only) for the dc measurements. In the ac measurements \( V_{tg} \) was instead supplied from a Stanford Research Systems DS345 signal generator.

Supporting Information. Additional fabrication details and electrical data, as well as a discussion of attempts with sulfur-oleylamine etchant. This material is available free of
charge via the Internet at [http://pubs.acs.org](http://pubs.acs.org).

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References

(1) Chandrakasan, A.P., Sheng, S. and Brodersen, R.W., Low-power CMOS digital design. *IEEE Journal of Solid-state Circuits* **27**, 473-484 (1992).

(2) ITRS International Technology Working Groups. *International Technology Roadmap for Semiconductors* 2015 edition. Available at [http://www.itrs.net](http://www.itrs.net) (2015).

(3) Lu, W. and Lieber, C.M., Nanoelectronics from the bottom up. *Nature Materials* **6**, 841-850 (2007).

(4) Barraud, S., Lapras, V., Previtali, B., Samson, M.P., Lacord, J., Martinie, S., Jaud, M.-A., Athanasiou, S., Triozon, F., Rozeau, O., Hartmann, J.M., Vizioz, C., Comboroure, C., Andrieu, F., Barbé, J.C., Vinet, M. and Ernst, T., Performance and design considerations for gate-all-around stacked-NanoWires FETs, Proceedings of the 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, pp. 29.2.1-29.2.4, (2017).

(5) Mertens, H., Ritzenthaler, R., Pena, V., Santoro, G., Kenis, K., Schulze, A., Litta, E.D., Chew, S.A., Devriendt, K., Chiarella, T., Demuynck, S., Yakimets, D., Jang, D., Spessot, A., Eneman, G., Dangol, A., Lagrain, P., Bender, H., Sun, S., Korolik, M.,
Kioussis, D., Kim, M., Bu, K.-H., Chen, S.C., Cogorno, M., Devrajan, J., Machillot, J., Yoshida, N., Kim, N., Barla, K., Mocuta, D. and Horiguchi, N., Vertically stacked gate-all-around Si nanowire transistors: Key Process Optimizations and Ring Oscillator Demonstration, Proceedings of the 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, pp. 37.4.1-37.4.4, (2017).

(6) Wernersson, L.-E., Thelander, C., Lind, E. and Samuelson, L., III-V nanowires – Extending a narrowing road. *Proceedings of the IEEE* **98**, 2047-2060 (2010).

(7) del Alamo, J.A., Nanometre-scale electronics with III-V compound semiconductors. *Nature* **479**, 317-323 (2011).

(8) Riel, H., Wernersson, L.-E., Hong, M. and del Alamo, J.A., III-V compound semiconductor transistors – from planar to nanowire structures. *MRS Bulletin* **39**, 668-677 (2014).

(9) del Alamo, J.A., Antoniadis, D.A., Lin, J., Lu, W., Vardi, A, and Zhao, X., Nanometer-scale III-V MOSFETs. *J. Electron. Dev. Soc.* **4**, 205-214 (2016).

(10) Tomioka, K., Yoshimura, M. and Fukui, T., A III-V nanowire channel on silicon for high-performance vertical transistors. *Nature* **488**, 189-192 (2012).

(11) Morkötter, S., Jeon, N., Rudolph, D., Loitsch, B., Spirkoska, D., Hoffmann, E., Döblinger, M., Matich, S., Finley, J.J., Lauhon, L.J., Abstreiter, G. and Koblmüller, G., Demonstration of confined electron gas and steep-slope behavior in delta-doped GaAs-AlGaAs core-shell nanowire transistors. *Nano Letters* **15**, 3295-3302 (2015).

(12) Schmid, H., Borg, M., Moselund, K., Cignac, L., Breslin, C.M., Bruley, J., Cutaia, D. and Riel, H., Template-assisted selective epitaxy of III-V nanoscale devices for co-planar heterogeneous integration with Si. *Applied Physics Letters* **106**, 233101 (2015).

(13) Johansson, S., Memisevic, E., Wernersson, L.-E. and Lind, E., High-frequency gate-all-
around vertical InAs nanowire MOSFETs on Si substrates. *IEEE Electron Device Letters* **35**, 518-520 (2014).

(14) Sørensen, B.S., Aagesen, M., Sørensen, C.B., Lindelof, P.E., Martinez, K.L. and Nygård, J., Ambipolar transistor behavior in $p$-doped InAs nanowires grown by molecular beam epitaxy. *Applied Physics Letters* **92**, 012119 (2008).

(15) Storm, K., Nylund, G., Börgstrom, M.T., Wallentin, J., Fasth, C., Thelander, C. and Samuelson, L., Gate-induced Fermi level tuing in InP nanowires at efficiency close to the thermal limit. *Nano Letters* **11**, 1127-1130 (2011).

(16) Nilsson, H.A., Caroff, P., Thelander, C., Lind, E., Karlström, O. and Wernersson, L.-E., Temperature dependent properties of InSb and InAs nanowire field-effect transistors. *Applied Physics Letters* **96**, 153505 (2010).

(17) Ling, C.C., Lui, M.K., Ma, S.K., Chen, X.D., Fung, S. and Beling, C.D., Nature of the acceptor responsible for $p$-type conduction in liquid encapsulated Czochralski-grown undoped gallium antimonide. *Applied Physics Letters* **85**, 384-386 (2004).

(18) Virkkala, V., Havu, V., Tuomisto, F. and Puska, M.J., Native point defect energetics in GaSb: Enabling $p$-type conductivity in undoped GaSb. *Physical Review B* **86**, 144101 (2012).

(19) Dey, A.W., Svensson, J., Borg, B.M., Ek, M. and Wernersson, L.-E., Single InAs/GaSb nanowire low-power CMOS inverter. *Nano Letters* **12**, 5593-5597 (2012).

(20) Babadi, A.S., Svensson, J., Lind, E. and Wernersson, L.-E., Impact of doping and diameter on the electrical properties of GaSb nanowires. *Applied Physics Letters* **110**, 053502 (2017).

(21) Svensson, J., Dey, A.W., Jacobsson, D. and Wernersson, L.-E., III-V nanowire com-
plementary metal-oxide semiconductor transistors monolithically integrated on Si. *Nano Letters* 15, 7898-7904 (2015).

(22) Jönsson, A., Svensson, J. and Wernersson, L.-E., A self-aligned gate-last process applied to All-III-V CMOS on Si. *IEEE Electron Dev. Lett.* 39, 935-938 (2018).

(23) Borg, B.M. and Wernersson, L.-E., Synthesis and properties of antimonide nanowires. *Nanotechnology* 24, 202001 (2013).

(24) Yang, Z.-X., Yip, S., Li, D., Han, N., Dong, G., Liang, X., Shu, L., Hung, T.F., Mo, X. and Ho, J.C., Approaching the hole mobility limit of GaSb nanowires. *ACS Nano* 9, 9268-9275 (2015).

(25) Fontcuberta i Morral, A., Colombo, C., Abstreiter, G., Arbiol, J. and Morante, J.R., Nucleation mechanism of gallium-assisted molecular beam epitaxy growth of gallium arsenide nanowires. *Appl. Phys. Lett.* 92 063112 (2008).

(26) Krogstrup, P., Popovitz-Biro, R., Johnson, E., Madsen, M., Nygård, J. and Shtrikman, H., Structural phase control in self-catalyzed growth of GaAs nanowires on silicon(111). *Nano Letters* 10, 4475-4482 (2010).

(27) Waldrop, J.R., Schottky-barrier height of ideal metal contacts to GaAs. *Appl. Phys. Lett.* 44, 1002-1004 (1984).

(28) Ullah, A.R., Gluschke, J.G., Krogstrup, P., Sørensen, C.B., Nygård, J. and Micolich, A.P., Towards low-dimensional hole systems in Be-doped GaAs nanowires. *Nanotechnology* 28, 134005 (2017).

(29) Ullah, A.R., Carrad, D.J., Krogstrup, P., Nygård, J. and Micolich, A.P., Near-thermal limit gating in heavily doped III-V semiconductor nanowires using polymer electrolytes. *Phys. Rev. Materials* 2, 025601 (2018).
(30) Carrad, D.J., Mostert, A.B., Ullah, A.R., Burke, A.M., Joyce, H.J., Tan, H.H., Jagadish, C., Kroghstrup, P., Nygård, J., Meredith, P. and Micolich, A.P., Hybrid nanowire ion-to-electron transducers for integrated bioelectronic circuitry. *Nano Lett.* **17**, 827-833 (2017).

(31) Dayeh, S.A., Soci, C., Yu, P.K.L., Yu, E.T. and Wang, D., Influence of surface states on the extraction of transport parameters from InAs nanowire field effect transistors. *Appl. Phys. Lett.* **90**, 162112 (2007).

(32) Roddaro, S., Nilsson, K., Astromskas, G., Samuelson, L., Wernersson, L.-E., Karlström, O. and Wacker, A., InAs nanowire metal-oxide-semiconductor capacitors. *Appl. Phys. Lett.* **92**, 253509 (2008).

(33) Holloway, G.W., Song, Y., Haapamaki, C.M., LaPierre, R.R. and Baugh, J., Trapped charge dynamics in InAs nanowires. *J. Appl. Phys.* **113**, 024511 (2013).

(34) Fortuna, S.A. and Li, X., GaAs MESFET with a high-mobility self-assembled planar nanowire channel. *IEEE Electron Device Letters* **30**, 593-595 (2009).

(35) Noborisaka, J., Sato, T., Motohisa, J., Hara, S., Tomioka, K. and Fukui, T., Electrical characteristics of InGaAs nanowire-top-gate field-effect transistors by selective-area metal organic vapor phase epitaxy. *Jpn. J. Appl. Phys.* **46**, 7562-7568 (2007).

(36) Ilegems, M., Beryllium doping and diffusion in molecular-beam epitaxy of GaAs and Al$_x$Ga$_{1-x}$As. *J. Appl. Phys.* **48**, 1278-1287 (1977).

(37) Casadei, A., Kroghstrup, P., Heiss, M., Röhr, J.A., Colombo, C., Ruelle, T., Upadhyay, S., Sørensen, C.B., Nygård, J. and Fontcuberta i Morral, A., Doping incorporation paths in catalyst-free Be-doped GaAs nanowires. *Applied Physics Letters* **102**, 013117 (2013).

(38) Koren, E., Hyun, J.K. Givan, U., Hemesath, E.R., Lauhon, L.J. and Rosenwaks, Y.,
Obtaining uniform dopant distributions in VLS-grown Si nanowires. *Nano Lett.* **11**, 183-187 (2011).

(39) Mori, Y. and Watanabe, N., A new etching solution system, $\text{H}_3\text{PO}_4-\text{H}_2\text{O}_2-\text{H}_2\text{O}$, for GaAs and its kinetics. *J. Electrochem. Soc.* **125**, 1510-1514 (1978).

(40) Naureen, S., Shahid, N., Sanatinia, R. and Anand, S., Top-down fabrication of high quality III-V nanostructures by monolayer controlled sculpting and simultaneous passivation. *Adv. Funct. Mater.* **23**, 1620-1627 (2013).

(41) Lu, W., Zhao, X., Choi, D., El Kazzi, S. and del Alamo, J., Alcohol-based digital etch for III-V vertical nanowires with sub-10 nm diameter. *IEEE Electron Device Letters* **38**, 548-551 (2017).

(42) Kane, B.E., Pfeiffer, L.N., West, K.W. and Harnett, C.K., Variable density high mobility two-dimensional electron and hole gases in a gated GaAs/Al$_x$Ga$_{1-x}$As heterostructure. *Appl. Phys. Lett.* **63**, 2132-2134 (1993).

(43) DeJarld, M., Shin, J.C., Chern, W., Chanda, D., Balasundaram, K., Rogers, J.A. and Li, X., Formation of high aspect ratio GaAs nanostructures with metal-assisted chemical etching. *Nano Letters* **11**, 5259-5263 (2011).

(44) Storm, K., Nylund, G., Samuelson, L. and Micolich, A.P., Realizing lateral wrap-gate nanowire FETs: Controlling gate length with chemistry rather than lithography. *Nano Lett.* **12**, 1-6 (2012).

(45) Burke, A.M., Carrad, D.J., Gluschke, J.G., Storm, K., Fahlvik Svensson, S., Linke, H., Samuelson, L. and Micolich, A.P., InAs nanowire transistors with multiple, independent wrap-gate segments. *Nano Lett.* **15**, 2836-2843 (2015).

(46) van Weperen, I., Plissard, S.R., Bakkers, E.P.A.M., Frolov, S.M. and Kouwenhoven, L.P., Quantized conductance in an InSb nanowire. *Nano Lett.* **13**, 387-391 (2013).
(47) Heedt, S., Prost, W., Schubert, J., Grützmacher, D. and Schäpers, Th., Ballistic transport and exchange interaction in InAs nanowire quantum point contacts. *Nano Lett.* **16**, 3116-3123 (2016).

(48) Irber, D.M., Seidl, J., Carrad, D.J., Becker, J., Jeon, N., Loitsch, B., Winnerl, J., Matich, S., Döblinger, M., Tang, Y., Morkötter, S., Abstreiter, G., Finley, J.J., Grayson, M, Lauhon, L.J. and Köblmuller, G., Quantum transport and sub-band structure of modulation-doped GaAs/AlAs core-superlattice nanowires. *Nano Lett.* **17**, 4886-4893 (2017).

(49) Baca, A.G., Ren, F., Zolper, J.C., Briggs, R.D. and Pearton, S.J., A survey of ohmic contacts to III-V compound semiconductors. *Thin Solid Films* **308-309**, 599-606 (1997).

(50) Liu, C., Dai, L., Ma, R.M., Yang, W.Q. and Qin, G.G., \textit{p}-Zn$_3$P$_2$ single nanowire metal-semiconductor field-effect transistors. *J. Appl. Phys.* **104**, 034302 (2008).

(51) Knoedler, M., Bologna, N., Schmid, H., Borg, M., Moselund, K.E., Wirths, S., Rossell, M.D. and Riel, H., Observation of twin-free GaAs nanowire growth using template-assisted selective epitaxy. *Cryst. Growth Des.* **17**, 6297-6302 (2017).

(52) Colombo, C., Spirkoska, D., Frimmer, M., Abstreiter, G. and Fontcuberta i Morral, A., Ga-assisted catalyst-free growth mechanism of GaAs nanowires by molecular beam epitaxy. *Physical Review B* **77**, 155326 (2008).