Junction Temperature Measurement Method for Thermal Resistance Testing of SiC MOSFET Module

Hao Guo¹, Chunsheng Guo¹,b*, Lei Wei¹, Yunong Liu¹
¹Faculty of Information Technology, Beijing University of Technology, Beijing China
²Email: guohao_guohao_1@126.com, b*email: guocs@bjut.edu.cn

ABSTRACT: The internal anti-parallel Schottky barrier diode threshold voltage of SiC metal-oxide-semiconductor field-effect transistor (MOSFET) modules is less than that of their body diodes, which prevents the use of the body diode voltage drop to measure junction temperature. In this paper, a thermal resistance test of the SiC MOSFET module is proposed based on the on-state voltage drop as a temperature-sensitive electrical parameter. Measurements are performed with the method and its feasibility evaluated. The on-state voltage drop temperature sensitivity under different gate voltages and the repeatability of the on-state voltage drop parameters before and after electric power heating in the thermal resistance tests are studied. The on-state voltage drop is measured under a high gate voltage and the accuracy of junction temperature measurement improves when the grid voltage remains the same during heating and measurement.

1. Introduction

Compared with traditional Si-based power devices, SiC-based power devices have the advantages of a wide band gap, high thermal conductivity, and high breakdown field strength [1]. These devices are suitable for high temperature, high frequency, and high power operating conditions. There are many potential applications of these devices in power electronic circuits for rail transit, electric vehicles, and aerospace [2]. The reliability and service life of SiC-based devices have drawn considerable attention, and junction temperature and thermal resistance are key parameters in studies of the reliability of semiconductor devices. Therefore, junction temperature measurements and thermal resistance measurement techniques are important issues in the research of SiC-based power devices.

Currently, there are three main methods for measuring the junction temperature of semiconductor devices: physical contact, infrared [3], and electrical methods. Among these, electrical methods are considered to be most promising for assessing junction temperature [4]. In research on thermal resistance testing of SiC metal-oxide-semiconductor field-effect transistor (MOSFET) modules to date, the electrical method has been used to measure junction temperature. In the literature [5], a forward voltage drop of the anti-parallel SiC Schottky barrier diode (SBD) in Silicon carbide MOSFET modules traces a cooling curve, which allows the junction temperature to be calculated through the Cauer model; however, this method is not suitable for junction temperature measurements of SiC MOSFET modules. There are two types of SiC MOSFET modules. Those with SiC MOSFETs connected in parallel in the module and those with SiC MOSFET connected in parallel with SiC SBDs. Among these, the body diode voltage drop can be used as a temperature-sensitive electrical parameter to measure the temperature of the first module and the second module block has an internal SiC SBD anti-parallel connected with the SiC MOSFET. The threshold voltage is lower than the body diode threshold voltage. Hence, the body diode voltage drop cannot be measured by the module junction temperature measurement and it is necessary to use the SiC MOSFET conduction voltage drop as a temperature-
sensitive electrical parameter to measure the temperature of this type of module.

Therefore, here a method is proposed to directly and accurately measure the junction temperature of SiC MOSFETs in thermal resistance measurements. On the basis of existing research that compares body diode voltage drop [6] and on-state voltage drop [7] as temperature-sensitive electrical parameters, the reliability and feasibility of using these two parameters in temperature measurements of SiC MOSFET modules are examined. Moreover, interfacial state traps at the interface of SiC and SiO2, SiC MOSFET devices pose problems such as device threshold voltage drift and gate oxide degradation. Therefore, when the electrical method is used for temperature measurements, the electrical parameters are affected by grid defects, causing problems such as drift and poor stability. Therefore, in this paper, the on-state voltage drop temperature sensitivity under different gate voltages and the reliability of the on-state voltage drop parameters after electric power heating in thermal resistance tests are examined. Temperature-sensitive electrical parameters can be measured more accurately by SiC MOSFET module thermal resistance testing.

2. Junction temperature measurement based on body diode voltage drop $V_{SD}$

In the MOSFET structure, there is a parasitic reverse PN junction, i.e., a parasitic body diode. The $V_{SD}$ is a classic temperature-sensitive electrical parameter and is widely used in Si MOSFET temperature measurements and thermal resistance testing. Therefore, this parameter can also be used as a temperature-sensitive electrical parameter in SiC MOSFETs. The body diode voltage drop measurement requires gate-source reverse bias and $V_{SD}$ to be measured under conditions that avoid self-heating with the drain-source passing a small measurement current $I_M$. Unlike Si MOSFETs, SiC MOSFET gate defects influence the measured $V_{SD}$ when the gate is suspended or a different gate-source reverse bias voltage is applied; however, this parameter has good linearity and sensitivity ($\sim 2.3 \text{ mV/°C}$) under certain gate-source reverse bias voltage. The temperature calibration curve is shown in Figure 1.

Current SiC MOSFET modules are divided into two types namely those that have only SiC MOSFETs in parallel in the module and modules composed of SiC MOSFETs and SiC SBDs in parallel. However, the temperature-sensitive electrical parameter temperature measurement is only applicable to the first type of module. The threshold voltage of the parasitic body diode of the SiC MOSFET is in the range of 2–3.5 V and the threshold voltage of the SBD is between 0.7–1.5 V. Therefore, the SBD will lead to conduction during temperature measurements and the voltage drop of the parasitic body diode cannot be measured. A structural diagram and the current trends when the temperature-sensitive electrical parameter is used for temperature measurements are shown in Figure 2.

3. Junction temperature measurement based on SiC MOSFET on-state voltage drop

For the module composed of SiC MOSFET and SiC SBD in parallel, it is impossible to apply a small drain-source reverse measurement current $I_M$ to measure $V_{SD}$ under the condition of gate-source reverse bias. Therefore, the forward parameter turn-on voltage $V_{DS}$ of the SiC MOSFET needs to be selected as the temperature-sensitive electrical parameter. However, the temperature sensitivity of $V_{DS}$ depends...
on the on-resistance. For MOSFET devices, the main part of the on-resistance $R_{DS,on}$ can be divided into the channel resistance $R_{ch}$ and the remaining body resistance $R_S$. Among these, $R_S$ includes the source contact resistance $R_{CS}$, JFET zone resistance $R_{JEFT}$, and drift zone resistance $R_D$.

1. **Channel resistance $R_{ch}$**

The channel resistance $R_{ch}$ can be expressed as

$$R_{ch} = \frac{\mu n C_{OX} Z}{L_{ch}} (V_{GS} - V_T),$$

where $\mu_n$ is the effective mobility of inversion channel electrons, $L_{ch}$ is the channel length, $Z$ is the width of the channel in the direction perpendicular to the cell section, $C_{OX}$ is the gate oxide capacitance per unit area, $V_T$ is the threshold voltage, and $V_{GS}$ is the gate source voltage.

When the device temperature changes and the effective gate drive voltage $V_{GS} - V_T$ is the same, the channel resistance $R_{ch}$ of the MOSFET at each temperature is inversely proportional to the effective mobility of channel electrons $\mu_n$, and the mobility increases with the increase of temperature. Therefore, the channel resistance $R_{ch}$ has a negative correlation with temperature.

2. **Body resistance $R_S$**

In a device with a relatively high withstand voltage, the impurity concentration of the epitaxial layer is low and the thickness is much greater, and the drift region resistance $R_D$ accounts for the main part of the bulk resistance $R_S$. Owing to the high critical breakdown field strength and high temperature resistance of SiC materials, SiC MOSFETs are often high-voltage devices; hence, the drift region resistance $R_D$ of SiC MOSFETs accounts for the main part of $R_S$ as the device temperature increases because $R_D$ increases at higher temperatures. As a result, the bulk resistance $R_S$ also increases at high temperatures [8]. Therefore, the body resistance $R_S$ is positively correlated with temperature.

Notably, $R_{ch}$ and $R_S$ have completely opposite temperature sensitivities in that $R_S$ is positively correlated with temperature, and $R_{ch}$ is negatively correlated with temperature. Furthermore, the proportions of $R_{DS,on}$ of $R_{ch}$ and $R_S$ are also different under different gate voltages. Therefore, the different ratios of $R_{DS,on}$ and different gate voltages have different effects on the temperature sensitivity. Under a low gate voltage, $R_{ch}$ is the main negatively correlating temperature sensitivity coefficient. Under a high gate voltage, $R_S$ makes the greatest contribution and is a positive correlation temperature sensitivity coefficient. Therefore, $V_{DS}$ under a low gate voltage and $V_{DS}$ under a high gate voltage will be discussed as the temperature-sensitive electrical parameters. Low and high gate voltages are defined by measuring the transfer curve at different temperatures (Figure 3). When $V_{GS}$ is less than 11 V, higher temperatures are associated with a greater current, i.e., the low gate voltage region. When $V_{GS}$ is higher than 14 V, higher temperatures lead to lower current, i.e., the high gate voltage region.

![Figure 3. Transfer curves](image1)

![Figure 4. Output curves](image2)

3.1. **High gate voltage on-state voltage drop $V_{DS}$**

When selecting $V_{DS}$ under a high gate voltage as the temperature-sensitive electrical parameter, to ensure that $V_{DS}$ is all determined by $R_S$, $V_{GS} = 18$ V is selected as the test condition. When selecting this
temperature-sensitive electrical parameter, it is also necessary to consider whether defects of the gate oxide layer of the SiC MOSFET will affect the junction temperature measurements in the thermal resistance tests. In commonly used thermal resistance testing, when measuring thermal resistance, it is necessary to apply power to the device for electrical heating when the device is on. During the heating process, VGS needs to be applied to the device to enable conduction through the device (IDS). Therefore, it is necessary to study whether changes to VGS and IDS during the heating process will affect VDS measured during the temperature measurement process.

To simulate the influence of the heating process, different VGS values were applied for 1 min before the junction temperature measurement and different effects on the VDS measurement during the temperature measurement process were studied. As shown in Figure 5, the heating VGS and the measured VGS were consistent with minimal variation. Therefore, when measuring the influence of the heating current on the temperature measurements, VGS = 18 V, which had the least influence was selected for the experiments and applied for 1 min and at different IDS to avoid self-heating. The influence on the measurement of VDS is shown in Figure 6. Different values of IDS did not notably affect the VDS measurements (within 0.1 mV). The above results indicate that the heating VGS and measured VGS should be kept stable during the temperature measurement. Furthermore, to avoid the influence of error when measuring the temperature calibration curve, it is also necessary to apply the same VGS for 1 min before measuring the VDS at each temperature, selecting a gate voltage VGS = 18 V, and measuring VDS from IDS to avoid self-heating. The temperature calibration curve is shown in Figure 7, which has good linearity but poor sensitivity (IDS = 500 mA, 0.02 mV/°C). However, the sensitivity of this method is poor at low temperature and small IDS. Better sensitivity would require measurements at high temperature and a larger IDS. However, a larger IDS may increase the temperature during the temperature measurement, increasing the error. Therefore, when using this method more accurate temperature measurements are achieved under short pulses and high IDS.

Figure 5. Influence of different VGS values on VDS
Figure 6. Influence of different IDS values on VDS
3.2. Low gate voltage on-state voltage drop \( V_{DS} \)

When selecting \( V_{DS} \) as the temperature-sensitive electrical parameter under a low gate voltage, to ensure that \( V_{DS} \) is determined by \( R_{ch} \), select \( V_{GS} = 6 \) V as the test condition. Under the grid voltage \( V_{GS} = 6 \) V, select the leakage-source current \( I_{DS} \) to avoid self-heating. The \( V_{DS} \) calibration curve of the \( I_{DS} \) measurement is shown in Figure 8. The linearity and the sensitivity (\( I_{DS} = 150 \) mA, \(-0.2 \) mV/°C) measured under these conditions are better than those when \( V_{DS} \) is measured under the high gate voltage conditions. When measuring the junction temperature under high gate voltage, it is necessary to ensure that \( V_{GS} \) during heating is the same as that during the temperature measurement. However, when a low gate voltage \( V_{DS} \) is selected as the temperature-sensitive electrical parameter, the heating current is very low because the MOSFET is not completely turned-on during heating; hence, the heating time will be relatively long. Moreover, when heating under a low gate voltage, the temperature sensitivity is negatively correlated such that a higher temperature has a greater current passing through, which might lead to the device burning out.

4. Conclusion

For two modules with different structures \( V_{SD} \) is selected as the temperature-sensitive electrical parameter for temperature measurements of the module with only MOSFETs in parallel, giving better linearity, sensitivity, and feasibility. The \( V_{DS} \) measured under low and high gate voltages were selected as temperature-sensitive electrical parameters of the internal parallel SiC SBD module. The measurement of \( V_{DS} \) under a high gate voltage is the most suitable temperature-sensitive electrical parameter for this type of module. In the resistance testing \( V_{GS} \) must be the same when the device is heated and when the temperature is measured. However, it is necessary to determine a calibration curve and measure at high temperature and higher \( I_{DS} \) to obtain better sensitivity. Thermal resistance and junction temperature measurements of SiC MOSFET modules at high temperature and high current, will be examined in future work.

References

[1] Millán J, Godignon P, Perpiñà X, et al. A survey of wide bandgap power semiconductor devices[J]. IEEE Transactions on Power Electronics, 2014, 29(5):2155-2163.
[2] Sheng Kuang, Guo Qing, Zhang Junming, et al. Development and prospect of SiC power devices in power grid[J]. Proceedings of the CSEE, 2012, 32(30):1-7(in Chinese).
[3] Zarebski J, Gorecki K. The electrothermal large-signal model of power MOS transistors for SPICE. IEEE Transactions on Power Electronics, 2010, 25(5): 1265–1274.
[4] Baker N, Liserre M, Dupont L, et al. Improved reliability of power modules: a review of online
junction temperature measurement methods[J]. IEEE Industrial Electronics Magazine, 2014, 8(3): 17-27.

[5] Zheng Shuai, Du Xiong, Zhang Jun, et al. Measurement of thermal parameters of SiC MOSFET modules with cooling curves[J]. Proceedings of the CSEE, 2020, 40(6): 1759-1769(in Chinese).

[6] Herold C, Sun J, Seidel P, et al. Power cycling methods for SiC MOSFETs[C]//29th International Symposium on Power Semiconductor Devices and ICs. Sapporo, Japan: IEEE, 2017.

[7] Griffo A, Wang J, Colombage K, et al. Real-time measurement of temperature sensitive electrical parameters in SiC power MOSFETs[J]. IEEE Transactions on Industrial Electronics, 2018, 65(3): 2663-2671.

[8] Hull B, Allen S, Gajewski D, et al. Reliability and stability of SiC power MOSFET and Next-Generation SiC MOSFET [C]. IEEE Workshop on Wide Bandgap Power Devices and Applications(WiPDA). Knoxville, TN, 2014: 139-142.