Design of Second-Order Multifunction Filter IC Based on Current Feedback Amplifiers with Independent Voltage Gain Control

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ABSTRACT This paper presents the integrated circuit (IC) design and implementation of the voltage-mode (VM) second-order gain-controlled multifunction filter (GMF), which consists of three current feedback amplifiers (CFAs), two grounded capacitors and four resistors. The design and implementation of the chip are based on a 0.18 μm process technology, and offers the attractive advantages of high efficiency, high reliability, low voltage, low power consumption, small size and good performance. The VM-GMF chip implements low-pass (LP), inverting band-pass (IBP) and band-stop (BS) filtering functions, and can independently control the gain of LP, IBP and BS filtering functions. The chip operates with a wide input voltage of 1.2 Vpp at ±0.9 V supply voltage, and has a figure-of-merit (FOM) of 66.7%. The on-chip measured input power at 1-dB compression point (IP1dB) is about 7.5 dBm with good linearity and the measured power dissipation (PD) is 5.4 mW with low voltage and low power consumption. The measured phase noise (PN) at an offset frequency of 1 kHz is −100.61 dBc/Hz. The measured value of the third-order intermodulation distortion (IMD3) is −57.38 dBc and the third-order intercept point (TOI) is 21.77 dBm. Simulations and on-chip experimental measurements demonstrate the theoretical analysis of the proposed VM-GMF.

INDEX TERMS Integrated circuit, chip design, filter, voltage-mode, analog circuit.

I. INTRODUCTION

IC has the advantages of high efficiency, low voltage, low power consumption, small size, high system integration, high reliability, light weight, few leads, few solder joints, long life, and good performance. It is not only widely used in consumer electronic products, but also widely used in sensing, communication, remote control and other fields. Analog circuit designs based on various active components for VM filters have been extensively studied [1]–[27], but none of them can be fully implemented on a single chip. The techniques of [1]–[27] use only circuit simulations and/or commercial ICs such as LT1228 [5], LM13700 [6], AD844 [2], [4], [7]–[27] measurements to verify the designed circuits. To verify circuit characteristics using an existing commercial IC, the supply voltage of the circuit must conform to the commercial IC datasheet, and additional passive components need to be added. The low-voltage and low-power characteristics of the circuit [1]–[27] cannot be verified in this way, nor can a full custom chip design be integrated. Hence, the techniques of [1]–[27] cannot provide low-voltage, low-power technology, nor can they integrated all the active and passive components used in circuit design into a single chip. One of the active components, the CFA, uses the commercial IC AD844 to design analog circuits [7]–[15], but these circuits cannot simultaneously implement the three VM filtering transfer functions. Although CFA-based circuits can simultaneously have at least three VM filtering transfer functions [16]–[27], the entire circuit for each design configuration still cannot be integrated into a single chip.

Recently, a new on-chip VM second-order multifunction filter was reported in [28]. The circuit in [28] can synthesize three VM filtering transfer functions, but the gains of their transfer functions cannot be controlled independently. In order to overcome the drawbacks in [28], the paper proposes a new VM CFA-based second-order GMF IC. The proposed VM-GMF has independent gain control capability for VM LP, IBP...
and BS filtering transfer functions. The VM-GMF design offers the following advantages: (i) simultaneous implementation of LP, IBP, and BS filtering transfer functions, (ii) independent adjustment of the filter passband gain, (iii) orthogonal adjustment of the filter bandwidth (BW) and quality factor (Q), (iv) features of one high-input impedance and three low-output impedances suitable for VM cascading, and (v) utilization of two grounded capacitors and four resistors as the smallest passive elements for realizing the VM multifunction filter with independent gain controllable. Table 1 presents the comparison of the proposed VM-GMF with the previously proposed VM multifunction CFA-based circuits. In Table 1, the proposed VM-GMF satisfies all the main advantages (i) to (v) above. From the survey of CFA-based literature in [7]–[27], none of the studies attempted to implement VM filters on a single chip. Although the VM CFA-based second-order multifunction filter circuits in [16]–[27] can be implemented with the commercial IC AD844AN, they are still not integrated into a single chip. Regarding the recent study in [28], the gains of the three filter responses interact to affect the Q of the filter. In other words, the gains of the three filter responses of [28] cannot be independently controlled without affecting the Q and angular pole frequency (ωp) of the filter parameters. In this paper, the authors propose a new synthesis method for second-order multifunction filter IC with independent voltage gain control. Without any additional voltage amplifiers, the new circuit design has independent gain control of the filter responses without affecting the parameters of Q and ωp. This independently adjustable gain characteristic can effectively reduce mutual interference between filter parameters when designing circuit systems, simplify the complexity of circuit design, and make the system easy to operate. Compared to [28], the new synthesis and design filter adds the advantage of independent voltage gain control to avoid interferences between filter parameters, and still enjoys all the main features of [28]. Despite the same value of FOM = 66.7% measured in the time domain, the chip still has up to input amplitude of ±1.2 Vpp at ±0.9 V power supply. Moreover, the proposed circuit has better P1dB, TOI and IMD3 performance compared to [28]. These advantages are not considered in the commonly used FOM. Based on the proposed filter with independent voltage gain control capability and better P1dB, TOI and IMD3 values, the proposed filter outperforms the previous filter in [28].

In wireless communication systems, the distance between the receiver and the transmitter affects the attenuation or amplification of the signal. This paper presents a new synthesis and design method for a second-order multifunction filter with on-chip implementation and experimental measurements. The filter implements LP, IBP and BS simultaneously with independent voltage gain control. The proposed circuit design does not require any additional voltage amplifiers and has independent gain control over the filter response without affecting the Q and ωp parameters, which can effectively reduce the chip area and power consumption. Adders and subtractors should be added to achieve high-pass and all-pass filter responses. The proposed second-order VM-GMF has been simulated using HSpice under the Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 μm process model. In addition, the proposed VM-GMF circuit is fabricated by TSMC 0.18 μm process technology, and the experimental results prove that the chip meets the requirements of the LP, IBP and BS filtering transfer functions.

| Performance factor | [17] | [18] | [19] | [20] | [21] | [22] | [23] | [24] | [25] | [26] | [27] | [28] | This work |
|---------------------|------|------|------|------|------|------|------|------|------|------|------|------|-----------|
| Number of CFA active components | 3 | 3 | 3 | 4 | 3 | 4 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| Number of passive elements | 5 | 7 | 6 | 8 | 5 | 6 | 10 | 5 | 6 | 5 | 5 | 6 | 6 |
| Use of only grounded capacitors | yes | no | yes | yes | no | yes | no | yes | yes | yes | yes | yes | yes |
| Simultaneous operation of various types of filters | 3 | 3 | 3 | 3 | 4 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| Constraints of passive element values | no | no | no | no | yes | no | no | yes | no | no | no | no | no |
| High-input and low-output impedances | no | yes | yes | yes | no | yes | yes | yes | yes | yes | yes | yes | yes |
| Orthogonal tuning of bandwidth and quality factor | no | yes | yes | no | no | yes | yes | no | yes | no | yes | yes | yes |
| Independent tuning of three passband gains | yes | no | no | yes | no | no | yes | no | no | no | no | no | yes |
| Technology | AD844 | AD844 | AD844 | AD844 | AD844 | AD844 | AD844 | AD844 | AD844 | AD844 | AD844 | AD844 | Chip |
| Voltage supply | ±12 V | ±6 V | ±6 V | ±6 V | ±6 V | ±6 V | ±6 V | ±6 V | ±0.9 V | ±0.9 V | ±0.9 V | ±0.9 V | ±0.9 V |
II. CIRCUIT DESCRIPTION

A. BASIC CONCEPT OF CFA

As a current-mode active component, the CFA is a versatile four-terminal analog building block, and its circuit symbol and complementary metal-oxide semiconductor (CMOS) implementation of the CFA are shown in Figs. 1a and 1b, respectively. In Fig. 1b, the CMOS implementation of the CFA is equivalent to a second-generation current conveyor with a voltage buffer, and the terminal relationship of the CFA can be modeled as [28]

\[
\begin{bmatrix}
I_Y \\
I_X \\
I_Z
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 \\
1 & 0 & 0 \\
0 & 1 & 0
\end{bmatrix}
\begin{bmatrix}
V_Y \\
V_X \\
V_Z
\end{bmatrix}, \quad \text{and } V_W = V_Z
\]

(1)

FIGURE 1. Symbol and CMOS structure of CFA. (a) Circuit symbol. (b) CMOS implementation.

B. ANALYTICAL SYNTHESIS METHOD OF VM-GMF MULTIFUNCTION FILTER

To illustrate the analytical synthesis method of VM-GMF, the resulting BS filtering transfer function is considered as:

\[
\frac{V_{BS}}{V_m} = \frac{H_o(s^2 + \frac{1}{ab})}{s^2 + \frac{1}{b} + \frac{1}{ab}}
\]

(2)

where \(a\) and \(b\) are the lossless integrator time constants, \(H_o\) is the BS filtering passband gain, \(V_m\) is the input signal of the VM second-order multifunction filter, and \(V_{BS}\) is one of the output signals of the VM second-order multifunction filter. Rearranging (2) and dividing by \(s^2\) gives

\[
(1 + \frac{1}{sb} + \frac{1}{s^2ab})V_{BS} = H_o(1 + \frac{1}{s^2ab})V_m
\]

(3)

Rearranging (3) to get

\[
V_{BS} = H_oV_m + \frac{1}{sb}V_m - \frac{1}{sb}V_{BS} - \frac{1}{s^2ab}V_{BS}
\]

(4)

Rearranging (4), yields

\[
V_{BS} = H_oV_m + \frac{1}{sb}(-V_{BS} + \frac{1}{sa}(H_oV_m - V_{BS}))
\]

(5)

Let

\[
V_{LP} = \frac{1}{sa}(H_oV_m - V_{BS})
\]

(6)

Then, (5) simplifies to

\[
V_{BS} = H_oV_m + \frac{1}{sa}(-V_{BS} + V_{LP})
\]

(7)

The output voltage \(V_{IBP}\) is

\[
V_{IBP} = \frac{1}{sb}(-V_{BS} + V_{LP})
\]

(8)

Therefore, (7) can be rewritten as

\[
V_{BS} = H_oV_m + V_{IBP}
\]

(9)

Substituting (9) into (6), the output voltage \(V_{LP}\) is

\[
V_{LP} = -\frac{1}{sa}V_{IBP}
\]

(10)

Equations (8), (9) and (10) of \(V_{IBP}\), \(V_{BS}\), and \(V_{LP}\) can be used to express the input-output relationship matrix of the VM multifunction filter as follows.
Using (11), two IBP and LP filtering transfer functions can be derived as

\[
\frac{V_{IBP}}{V_\text{in}} = \frac{-H_o \left( \frac{1}{s b} \right)}{s^2 + s + \frac{1}{a b}} \quad (12)
\]

\[
\frac{V_{LP}}{V_\text{in}} = \frac{H_o \left( \frac{1}{a b} \right)}{s^2 + s + \frac{1}{a b}} \quad (13)
\]

According to (8), (9) and (10), the block diagram of the analytical synthesis method for LP, IBP and BS filtering transfer functions is obtained, as shown in Fig. 2.

![Fig. 2. Block diagram of the synthesis VM-GMF based on two lossless integrator loops.](image)

C. VM-GMF MULTIFUNCTION FILTER REALIZATION

According to Fig. 2 and the input–output matrix form of (11), the minimal implementation of the integrator is using one capacitor and one resistor, and the minimal implementation ratio of the voltage passband gain for independent controlled voltage signal is using two resistors. Therefore, the lossless integrator time constants and the voltage passband gain \(a, b\) and \(H_o\) in Fig. 2 as

\[
a = C_1 R_1, \quad b = C_2 R_2, \quad \text{and} \quad H_o = \frac{R_3}{R_4} \quad (14)
\]

Taking (14) and substituting it into (2), (12) and (13), the LP, IBP and BS filtering transfer functions of the VM-GMF multifunction filter are obtained.

\[
\frac{V_{LP}}{V_\text{in}} = \frac{R_3}{R_4} \left( -\frac{1}{s C_2 R_2 R_3} \right), \quad H_{LP} = \frac{R_3}{R_4} \quad (15)
\]

\[
\frac{V_{IBP}}{V_\text{in}} = \frac{R_3}{R_4} \left( \frac{s^2 + 1}{C_2 R_2 + C_2 C_2 R_2} \right), \quad H_{IBP} = \frac{R_3}{R_4} \quad (16)
\]

\[
\frac{V_{BS}}{V_\text{in}} = \frac{R_3}{R_4} \left( \frac{s^2 + 1}{C_2 R_2 + C_2 C_2 R_2} \right), \quad H_{BS} = \frac{R_3}{R_4} \quad (17)
\]

The \(\omega_o, BW\) and \(Q\) of filter can be obtained as

\[
\omega_o = \sqrt{\frac{1}{C_2 C_2 R_2 R_2}} \quad (18)
\]

\[
\frac{\omega_o}{Q} = \frac{1}{C_2 R_2} \quad (19)
\]

\[
Q = \sqrt{\frac{C_2 R_2}{C_2 R_2}} \quad (20)
\]

Based on Fig. 2, the proposed VM-GMF multifunction filter is shown in Fig. 3. The circuit consists of three CFAs, two grounded capacitors and four resistors as the minimal passive elements to achieve the VM-GMF multifunction filter. In Fig. 3, the proposed VM-GMF multifunction filter with one high-input impedance and three low-output impedences is synthesized based on Fig. 2 and the input–output matrix form of (11). Routine analysis of the proposed VM-GMF multifunction filter in Fig. 3 yields the same LP, IBP and BS filtering transfer functions as given in (15), (16) and (17). The parameters \(\omega_o, \omega_o/Q\) and \(Q\) of the VM-GMF are also given in (18), (19) and (20), respectively. Examining (15) to (20), the voltage passband-gain of each \(H_{LP}, H_{IBP}\) and \(H_{BS}\) allows independent control of each transfer function gain without affecting the parameters \(\omega_o, \omega_o/Q\) and \(Q\) of the VM-GMF. Therefore, the circuit has the ability to independently control the voltage gain of LP, IBP and BS filtering transfer functions.

![Fig. 3. The proposed multifunction filter with independent tuning of passband gain.](image)
III. SIMULATION AND CHIP MEASUREMENTS

In order to obtain a pole frequency of $f_o = 568$ kHz at $Q = 1$, the passive elements of two capacitors and four resistors were set equal to 14 pF and 20 kΩ, respectively. In an electronic design automation cloud system provided by the Taiwan Semiconductor Research Institute, pre- and post-layout simulations of the proposed VM-GMF configuration were performed using cadence’s virtuoso tool to validate the theoretical analysis. The CMOS transistor aspect ratio (length/width) of the CFA in Fig. 1b is taken as 0.4µm/75µm for M1—M16, 0.8µm/13µm for M17—M20, and 0.4µm/26µm for M21—M28. In Fig. 1b, the supply voltages were $V_{DD} = -V_{SS} = 0.9$ V and the bias voltages were $V_{BI} = 0.6$ V and $V_{Z} = 0.3$ V.

To verify the performance of the CFA active component, two basic analytical simulations were performed on the DC and AC characteristics of the CFA voltages at the Y, X, Z and W terminals. Figure 4 shows the DC characteristic relationship between the voltages at Y, X, Z, and W when a 5 kΩ resistance to ground is used at each of the X and Z terminals, and the voltage at Y is swept from −0.9 V to 0.9 V. In Figure 4, the dynamic range (DR) of the input is −0.8 V to 0.8 V with maximum error of approximately 0.02 V. Figure 5 shows the AC characteristic relationship between the voltages at Y, X, Z, and W using a 5 kΩ ground resistance at the X and Z terminals, and the Y input voltage is AC = 1 V. In Figure 5, the frequency domain simulated −3 dB frequencies for the X, Z, and W terminals are approximately 378 MHz, 409 MHz, and 431 MHz, respectively, so the available −3 dB range for the CFA active component is approximately 378 MHz. To verify the gain adjustable range of the CFA in the frequency domain, a 5 kΩ resistor is connected between the X terminal of the CFA and ground, and AC = 1 V is applied to the Y terminal of the CFA. The Z terminal resistance of the CFA is varied to 5 kΩ, 10 kΩ, 20 kΩ, and 30 kΩ to obtain voltage gain of 0 dB, 6 dB, 12 dB, and 15.56 dB at the Z terminal, respectively. Figure 6 shows the simulation results of the CFA-based voltage amplifier at different gain values. In Figure 6, the simulated gains at the Z terminal of the CFA-based voltage amplifier are about −0.05 dB, 5.92 dB, 11.8 dB, and 15.3 dB. When the gain of the CFA-based amplifier circuit is increased to approximately 15.3 dB, the available bandwidth without gain loss is approximately 7.8 MHz.

![FIGURE 4. DC analysis simulation characteristics of CFA between Y, X, Z, and W terminal voltages.](image)

![FIGURE 5. AC analysis simulation characteristics of CFA between Y, X, Z, and W terminal voltages.](image)

![FIGURE 6. Frequency response of the CFA-based voltage amplifier with different values of gain.](image)
simulated $f_0$ and errors of the proposed circuit compared to the theoretical values.

To verify the gain of the filter, the filter gain can be independently controlled without affecting the parameters $f_0$ and $Q$, and two equal resistors $R_1 = R_2 = 20 \, \text{k}\Omega$ and two equal capacitors $C_1 = C_2 = 14 \, \text{pF}$ were set to obtain $f_0 = 568.4 \, \text{kHz}$ and $Q = 1$. Figures 10 to 12 show that when $R_4 = 20 \, \text{k}\Omega$ is fixed, and $R_3$ is given as $20 \, \text{k}\Omega$, $40 \, \text{k}\Omega$, $80 \, \text{k}\Omega$, and $120 \, \text{k}\Omega$ respectively, the filter gain can be independently controlled without affecting the parameters of $f_0$ and $Q$ to obtain $0 \, \text{dB}$, $6 \, \text{dB}$, $12 \, \text{dB}$, $15.56 \, \text{dB}$.

### Table 2. The simulated $f_0$ and its error of the proposed circuit.

| Transfer function | Ideal pole frequency (kHz) | Simulated pole frequency (kHz) | Error (%) |
|-------------------|----------------------------|---------------------------------|-----------|
| LP                | 568.4                      | 574.1                           | 0.98      |
|                   | 1136.8                     | 1148.1                          | 0.99      |
|                   | 2273.6                     | 2312                            | 1.23      |
|                   | 3789.4                     | 3908.4                          | 3.1       |
| IBP               | 568.4                      | 574.1                           | 1.01      |
|                   | 1136.8                     | 1148.1                          | 0.99      |
|                   | 2273.6                     | 2312                            | 1.23      |
|                   | 3789.4                     | 3908.4                          | 3.1       |
| BS                | 1136.8                     | 1148.1                          | 0.99      |
|                   | 2273.6                     | 2312                            | 1.23      |
|                   | 3789.4                     | 3908.4                          | 3.1       |

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To evaluate the variation of process parameters, five simulation corners in typical-fast (TT), fast-fast (FF), slow-slow (SS), fast-slow (FS) and slow-fast (SF) modes were performed. Figures 13 to 15 show the simulated response of amplitude versus frequency for the filter with five corner variations. Table 3 shows the simulated $f_0$ and errors for the five corner modes of the filter compared to the theoretical value of $f_0 = 568.4$ kHz.

| Transfer function | Simulated $f_0$ (kHz) | Errors (%) |
|-------------------|-----------------------|------------|
|                  | TT                    | SS         | FF | SF | FS |
| LP                | 574                   | 568        | 607 | 603 | 564 | 0.98 | -0.07 | 6.79 | 6.08 | -0.77 |
| IBP               | 574                   | 564        | 584 | 581 | 562 | 0.98 | -0.77 | 2.74 | 2.21 | -1.12 |
| BS                | 565                   | 560        | 581 | 576 | 557 | -0.59 | -1.47 | 2.21 | 1.33 | -2.00 |

Post-layout simulations of the proposed VM-GMF configuration were also carried out. The completed layout of the entire schematic allows viewing of parasitic effects, including all parasitic capacitances and resistances in the layout. By performing post-layout simulation, the accuracy of VM-GMF designed chip can be predicted. Figure 16 shows the VM-GMF micrograph and layout. Design rule checks and layout versus schematic can verify potential errors and net mismatches between schematic and layout, as well as complete wafers of VM-GMF chip fabricated using TSMC 0.18 μm process technology. In Fig. 16, the core layout of the pad less VM-GMF chip is 490.6 x 461.5 μm², and the layout cell of the CMOS implemented CFA is 265.4 x 103.9 μm². Figure 17 illustrates the on-chip measurement printed circuit board (PCB) constructed for on-chip measurement of the VM-GMF. Figure 18 illustrates the photograph of the experimental setup.
To validate the feasibility of the VM-GMF structure shown in Fig. 3, chip performance evaluations in the time domain, frequency domain, total harmonic distortion (THD), PD, IMD3, TOI, IP1dB, and PN analysis were investigated. Figures 19 to 21 show the time domain on-chip measurements of the LP, IBP and BS responses at 568 kHz pole frequency to test the input dynamic range of the proposed VM-GMF chip, respectively. Table 4 summarizes the on-chip measurements of voltage and phase errors between the input and output at a pole frequency of 568 kHz.
FIGURE 21. BS time-domain on-chip measurements of input and output waveforms at 568 kHz pole frequency. (a) Input 400m Vpp, (b) Input 800m Vpp.

Table 4. On-chip measurements of voltage and phase errors between the input and output at a pole frequency of 568 kHz.

| Transfer function | Input voltage | Output voltage | Voltage loss | Ideal pole phase | Measured pole phase | Phase difference error |
|-------------------|---------------|----------------|--------------|------------------|---------------------|------------------------|
| LP                | 400m          | 380m           | 20m          | -90°             | -89.9°              | 0.1°                   |
|                   | 800m          | 752m           | 48m          | -90°             | -89.74°             | 0.26°                  |
| IBP               | 400m          | 392m           | 8m           | -180°            | -177.6°             | -2.4°                  |
|                   | 800m          | 752m           | 48m          | -180°            | -177.1°             | -2.9°                  |
| BS                | 400m          | 40m            | 0m           | 0°               | '46.86'°            | '46.86'°               |
|                   | 800m          | 80m            | 80m          | 0°               | '29.16'°            | '29.16'°               |

Note: For the band-stop filter, the ideal output amplitude must be completely filtered out at the pole frequency, so the measured phase information at pole frequency is inaccurate.

Figures 22 to 24 show the frequency-domain on-chip measurements of the LP, IBP, and BS responses, respectively, which were derived and used as additional measurement traces for the Matlab theoretical analysis, as described in (15), (16) and (17). Figures 25 to 27 show the comparison between the Matlab theory, HSpice simulations, and on-chip measurements for the LP, IBP and BS responses. Table 5 summarizes the on-chip voltage transfer function measurements for gain and phase responses. These results confirm the good performance of the VM-GMF design and implementation.
FIGURE 25. LP response results based on Matlab theory, HSpice simulation and on-chip measurements.

FIGURE 26. IBP response results based on Matlab theory, HSpice simulation and on-chip measurements.

FIGURE 27. BS response results based on Matlab theory, HSpice simulation and on-chip measurements.

Table 5. On-chip measurements of LP, IBP and BS voltage gain and phase responses.

| Transfer function | Ideal pole phase | Ideal pole frequency | Measured pole frequency | Pole frequency error | Gain loss |
|-------------------|------------------|----------------------|-------------------------|---------------------|----------|
| LP                | −90°             | 568 kHz              | 584.7 kHz               | 16.7 kHz            | 0.87 dB  |
| IBP               | −180°            | 568 kHz              | 576.9 kHz               | 8.9 kHz             | 0.53 dB  |
| BS                | 0°               | 568 kHz              | 569.5 kHz               | 1.5 kHz             | +21.18 dB|

Note: For the bandstop filter, the desired output amplitude must be completely filtered at the pole frequency, so the observed gain measurement at the pole frequency can be used to determine how much gain is not filtered out.

To evaluate the maximum allowable distortion output voltage swing, the IBP output spectrum was measured on-chip for input voltages range from 200 mVpp to 1.2 Vpp. Figures 28 to 38 show the measured on-chip IBP output spectra over an input voltage range from 200 mVpp to 1.2 Vpp, respectively. From the tables in Figs. 28 to 38, THD can be calculated. Figure 39 shows the results of the THD analysis of the IBP output spectrum. Figure 40 shows the maximum allowable distortion output voltage swing of the IBP output waveform with a THD calculation of 3.3% when the input voltage is 1.2 Vpp. Figure 41 shows the PN analysis of the IBP response when the input voltage is 1.2 Vpp. As shown in Figs. 28 to 41, the design VM-GMF has a wide input voltage range from 200 mVpp to 1.2 Vpp and a low PN of −100.61 dBc/Hz at offset frequency 1 kHz. Figure 42 shows the IP1dB analysis of the IBP response. As shown in Fig. 42, the on-chip measured IP1dB is about 7.5 dBm with good linearity. Figure 43 shows a two-tone test of the IBPF voltage response through intermodulation characterization. In Fig. 43, two closely spaced tones, f1 = 567 kHz and f2 = 569 kHz, are used with equal input amplitudes of 0.35 Vpp. The measured value of the IMD3 is −57.38 dBc and the TOI point is 21.77 dBm.
FIGURE 29. IBP output spectrum results when input voltage as 300 mVpp.

FIGURE 30. IBP output spectrum results when input voltage as 400 mVpp.

FIGURE 31. IBP output spectrum results when input voltage as 500 mVpp.

FIGURE 32. IBP output spectrum results when input voltage as 600 mVpp.

FIGURE 33. IBP output spectrum results when input voltage as 700 mVpp.

FIGURE 34. IBP output spectrum results when input voltage as 800 mVpp.

FIGURE 35. IBP output spectrum results when input voltage as 900 mVpp.

FIGURE 36. IBP output spectrum results when input voltage as 1 Vpp.
The FOM of the VM second-order filter has defined as [28, 29]

\[
\text{FOM} = 100 \times \left( \frac{V_{in}}{V_{dd}} \right) \% \tag{21}
\]

where the \( V_{in}/V_{dd} \) ratio is the ratio of the input voltage signal to the power supply voltage. As shown in Figs. 39 and 40, the FOM of the VM-GFM chip is calculated to be 66.7%. As shown in Figure 43, the DR is defined as the difference spectrum in the two-tone test of the IBP response for each 0.35 \( V_{pp} \) input voltage signal. The measured DR is approximately 57 dB, the measured PD is 5.4 mW, and the simulated filter BW is approximately 2.2 MHz. Based on
IV. CONCLUSIONS

On-chip implementation and experimental measurements of the VM-GMF are presented in this paper. The VM-GMF design enjoys the following advantages: (i) it can implement LP, IBP and BS filtering transfer functions simultaneously, (ii) it can independent tuning of the filter passband gains, (iii) it can orthogonal tuning of the filter BW and Q, (iv) it has one high-input impedance and three low-output impedances and can be easily cascadable, and (v) it uses two grounded capacitors and four resistors as the minimal passive elements to achieve the VM multifunction filter with controllable gain. The design and implementation of the chip offers the attractive advantages of high efficiency, high reliability, low voltage, low power consumption, small size and good performance. The design VM-GMF has a wide input voltage ranges and the maximum allowable distortion output voltage swing of the IBP output waveform with a THD calculation of 3.3% when the input voltage is 1.2 V_{pp}. The on-chip measured IP1dB is about 7.5 dBm with good linearity, and the measured PD is 5.4 mW with low voltage and low power consumption. The measured PN at an offset frequency of 1 kHz is −100.61 dBc/Hz. The measured value of the IMD3 is −57.38 dBc and the TOI is 21.77 dBm. These results confirm the good performance of the VM-GMF design and implementation.

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