2 ps Time-to-Digital Converter for Frequency Synthesis in 55 nm CMOS Technology

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Abstract. This paper presents a 2-ps time-to-digital converter (TDC) in 55 nm CMOS technology for all-digital phased-locked loop (ADPLL) system. Innovative inverter delay chain and Vernier delay chain cascade structure is adopted in the TDC to expand the measurement range while ensuring high resolution, so as to meet the wideband application requirements. Time window technology is employed to reduce circuit working frequency to save power by extracting single rising/falling edge of clock signal. Multiplexing technology is exploited to further reduce the power consumption by reusing the rising/falling edge detection delay chain of the first-level TDC, and also the time deviation detection circuit and resolution scaling factor detection circuit of the second-level TDC. The TDC features a differential nonlinearity (DNL) of 0.31 least significant bits (LSB) and an integral nonlinearity (INL) of 0.62 LSB, with a total current consumption of 4 mA from a 1.2 V supply voltage.

1. Introduction

The time-to-digital converter (TDC) can convert the phase difference between the reference clock (FREF) and the digitally-controlled oscillator (DCO) feedback signal (HCLK) into a digital signal, using the resulting digital signal to control the oscillation frequency of DCO, which makes it possible to achieve the all-digital phase-locked loop (ADPLL). Actually, TDC has been used earlier in particle physics, high-energy physics and other fields requiring accurate time interval measurement for more than 20 years, and other applications including time of flight measurement, testing instruments such as digital oscilloscope and logic analyzer [1]. But the use of TDC in ADPLLs has only grown in popularity in recent years. It turns out that with the continuous development of CMOS technology, the channel length of MOS tube is decreasing, and the intrinsic gain of amplifier is also declining. At the same time, the decrease of the power supply voltage reduces the design margin of the analog circuits, thus the usage of some circuit structures to improve the performance of the analog circuits is limited. Meanwhile, due to the progress of process, the delay and power consumption of digital gate circuits are decreasing, so the performance and power consumption of time and digital domain circuits are constantly improving. This allows for higher resolution and better linearity in time and digital domain. Compared with traditional analog circuits, time and digital domain circuits will have better performance in the future. Therefore, the performance of TDC will also improve along with the progress of process, and it will inherit the characteristics of short design cycle and strong portability of...
digital circuits. However, as in any case where a digital circuit is substituted for an analog one, the TDC generates quantization noise, which determines the in-band phase noise of the PLL. The improvement of the resolution of TDC can significantly reduce the in-band phase noise of PLL. Besides resolution, sampling rate, measurement range and linearity are also important performance indexes of TDC.

In recent years, in order to achieve high performance, TDC with various structures emerge endlessly, and can mainly be divided into Nyquist TDC and oversampling TDC. Nyquist TDC is often used to achieve a higher resolution with high sampling rate by obtaining a delay time lower than the minimum inverter delay under a particular process. However, the in-chip mismatch of advanced processes becomes more serious, which will worsen the resolution and linearity of TDC. Although mismatch can be reduced by increasing the size of MOS tube, power consumption and chip area will increase at the same time, which is contrary to the trend of process evolution. Oversampling TDC can reshape the mismatch and achieve a large measurement range and high resolution. However, oversampling TDC is vulnerable to the time skew error caused by leakage current and charge sharing, which will worsen its performance, regardless of its complex structure, limited bandwidth and large power consumption. Overall, TDC has been realized in a variety of ways and structures, such as: Vernier-delay line TDC [2], gated-ring-oscillator (GRO) TDC [3], Vernier-ring TDC [4], delay-lock loop (DLL) based TDC [5], coarse-fine TDC [6], digital-to-time-converter (DTC)-assisted TDC [7], time amplifier based TDC (TA-TDC) [8], delta-sigma TDC [9], and TDC optimized with other digital processing techniques [10].

In this paper, a two-level coarse-fine TDC implemented in SMIC 55nm CMOS technology is demonstrated, featuring a resolution of 2 ps and a measurement range of more than 2 ns. The paper is organized as follows: the architecture of the proposed coarse-fine TDC is demonstrated in Section II. The implementation of critical building blocks of the TDC is described in Section III. The simulation results are shown in Section IV and the conclusion is drawn in Section V.

2. Two-level TDC architecture
The architecture of the two-level coarse-fine TDC employed in this design is shown in Figure 1. The proposed TDC is mainly composed of core quantization unit, including first-stage quantization unit, intermediate-stage time-deviation-selection unit and second-stage quantization unit, and decoding unit, including pseudo-thermometer to binary decoder and periodic normalization unit. The timing sequence diagram of the TDC is presented in Figure 2. The time deviation $DT_r$ is the distance between the rising edge of $FREF$ and the later nearest rising edge of $HCLK$, which is generated by the coarse quantization of the first-stage TDC, and the time deviation $dt_r$ is generated by the fine quantization of the second-stage TDC. Then, the accurate time deviation $Dt_r$ between the rising edge of $FREF$ and the later nearest rising edge of $HCLK$ can be obtained by making a difference between $DT_r$ and $dt_r$ according to certain rules. Similarly, the accurate time deviation $Dt_f$ between the rising stage of $FREF$ and the later nearest falling stage of $HCLK$ can be obtained by making a difference between $DT_f$ and $dt_f$ according to certain rules. Specifically, the relationship between the time deviation $DT_{r(f)}, dt_{r(f)}$ and $Dt_{r(f)}$ is as follows,

$$Dt_{r(f)} = DT_{r(f)} * K_{res} - dt_{r(f)}$$  \hspace{1cm} (1)

where $K_{res}$ is the two-level resolution ratio factor.

3. Two-level TDC circuit
3.1. Core quantization unit
The core quantization unit of the TDC adopts two-level structure, thus achieving the requirements of high resolution and large measurement range at the same time. The first stage is based on buffer delay chain, with a resolution of 48 ps and 48 delay units, while the second stage is based on Vernier delay chain, with a resolution of 2 ps and 32 delay units.
The block diagram of the first stage quantization unit realizing rising and falling edge detection simultaneously is demonstrated in Figure 3. As shown in the diagram, FREF is delayed through the buffer delay chain, and the nearest rising edge DH_out and falling edge DL_out of HCLK later than the rising edge of FREF are extracted through rising and falling edge flip-flop separately. Afterwards, DH_out and DL_out are utilized to sample the delayed FREF signal so as to digitize the time difference between DCO output and FREF signal. The main advantage of this structure is no need of high-speed delay chain with high power consumption, compared with traditional structure where HCLK is regarded as the delayed signal. The resolution of the first stage quantization unit is determined by the buffer delay $t_{buf1}$, and the whole delay time of the delay chain should cover at least one DCO period with some additional margin for PVT variation. DH(L)_out and FREF-delayed signal $D<k>$ would subsequently be send to the intermediate-stage time-deviation-selection circuit.

![Figure 1](image-url)  
Figure 1. Architecture of the two-level coarse-fine TDC.

![Figure 2](image-url)  
Figure 2. Timing sequence diagram of the TDC.

![Figure 3](image-url)  
Figure 3. Block diagram of the first-level quantization unit realizing rising and falling edge detection simultaneously.
The block diagram of the second stage quantization unit based on Vernier delay chain is presented in Figure 4. The basic characteristic of the structure is to carry out the timing comparison and quantization of two signals through two delay chains with close resolution, thus getting the ability to overcome the process constraints to achieve a higher resolution which is the unit delay difference between the two delay chains, expressed as $t_{buf3} - t_{buf2}$.

Besides, the second stage quantization unit is reused in the design for the quantization of a partly same delay chain as the first stage quantization unit to get the ratio factor $K_{res}$. The selection of the output signal of the intermediate-stage time-deviation-selection circuit or the duplicate chain signal is implemented with the gate control unit, including two 2:1 MUXs controlled by $FREF$. When $FREF$ is high, the output signals of the intermediate-stage time-deviation-selection circuit enter the second stage; when $FREF$ is low, the duplicate delay chain signals enter the second stage. In other words, the measurement of time interval of data signal is in the high state of reference signal, while the measurement of ratio factor is in the low state of reference signal, which not only avoids the conflict of signals, but also effectively multiplexes the second-level quantization circuit. Moreover, after the direct decoding of the ratio factor, an average is made to reduce the error caused by the influence of PVT deviation and too small measurement interval, so that the ratio factor is more accurate.

3.2. Intermediate-Stage Time-Deviation-Selection Circuit

The main function of the intermediate-stage time-deviation-selection circuit is to extract the most recently delayed $FREF$ signal after $DH(L)_{out}$ and $DH(L)_{out}$ signal and send them to the second stage for time interval quantization. The transition module between the two TDC stages is very critical as the transmission process may introduce some time deviation, resulting in quantization deviation, because of the transmission delay of the transition module.

The block diagram and the time sequence diagram of the time-deviation-selection unit are shown in Figure 5. Firstly, a SEL-signal generator is required, which is obtained through the analysis of the first-level quantization results, that is, at the time of the first transformation from 1 to 0, the gate value is 1, and the rest states are 0, so that the delayed $FREF$ signal of which the rising edge firstly exceeds the rising edge of $DH(L)_{out}$ is extracted. Next, a delay chain should be placed after $D<k>$ and $DH(L)_{out}$, mainly in order to make the signal reach the 48:1 MUX after SEL signal is effective, so as to achieve the correct gating function. Finally, the multipath selection of $D<k>$ and $DH(L)_{out}$, which is the key module of the transition unit, determines the magnitude of the introduced time deviation and the effectiveness of the gate unit. It is necessary to simultaneously measure the delayed $FREF$ signal $D<47:1>$ and $DH(L)_{out}$ signal with the same delay, thus a 48:1 MUX is needed here.

The core block diagram of the 48:1 MUX is presented in Figure 6. In order to make effective $D<k>$ and $DH(L)_{out}$ go through the same delay and reduce the introduced time deviation, dummy circuit is adopted in the design to ensure that $DH(L)_{out}$ will experience the same delay after passing through
the dummy 48:1 MUX. And referring to $D^{<k>}$, the gating signal is generated by the SEL-signal generator, while the gating signal related to $DH(L)_{out}$ is set to some constant to let $DH(L)_{out}$ pass through directly.

![Diagram](image)

Figure 5. (a) Block diagram and (b) time sequence diagram of the time-deviation-selection unit.

![Diagram](image)

Figure 6. Core block diagram of the 48:1 MUX.

3.3. Periodic Normalization Unit

Although the two-level resolution ratio factor $K_{res}$ of the two stages quantization units can be estimated by the simulation results, the factor would fluctuate to a certain extent due to PVT influence. Therefore, the data signal period is necessary to be normalized with a periodic normalization unit, which is reused with the second stage quantization unit, as shown in Figure 7. It is required to obtain a second-level quantization result of the first-level quantization interval, namely the value of the first transformation of the second-level quantization result when FREF is in low state. The formula of the ratio factor $K_{res}$ can be expressed as below:

$$K_{res} = \frac{t_{buf1}}{t_{buf2} - t_{buf3}}$$

(2)

4. Results and comparisons

Implemented using SMIC 55 nm CMOS process, the layout of the proposed two-level TDC is shown in Figure 8. The total size including all the pads is $0.95 \times 0.78$ mm$^2$ and the core area occupies $0.36 \times 0.32$ mm$^2$. The TDC layout based on buffer and Vernier delay chain is considered as follows: firstly, the layout of the intermediate-stage time-deviation-selection circuit should be implemented symmetrically as far as possible, and the surrounding environment should be symmetric too, so that the path that each data goes through would be as similar as possible, so as to have the same delay time;
secondly, for the same clock, clock synchronization needs to be achieved by entering the clock port of each D flip-flop through a clock tree with the same path length. The total current consumption of the TDC is 4 mA under a 1.2 V supply voltage.

The simulation is carried out using an external $f_{\text{REF}}=50$ MHz frequency reference clock $F_{\text{REF}}$ and a $f_0=4-8$ GHz high-speed clock $H_{\text{CLK}}$ generated by voltage-controlled oscillator (VCO). The simulation results show that the proposed TDC can normally cover a measurement range of 2.2 ns with a resolution of about 2 ps. The differential non-linearity (DNL) is blow 0.31 least significant bit (LSB) and the integral non-linearity (INL) is blow 0.62 LSB, as shown in Figure 9. The TDC resolution versus process and temperature is displayed in Figure 10. The distribution is relatively tight as the resolution varies within $\pm0.5$ ps between weak and strong process and a temperature range of -45~+125℃. Table I compares the proposed TDC system with current state-of-the-art TDCs in CMOS technology. The simulation results show that the proposed TDC can functional well and is possessed of large measurement range and high resolution with high linearity and low power consumption.

![Figure 7. Periodic normalization unit reused with second-level quantization unit.](image1)

![Figure 8. Layout of the two-level TDC (0.95×0.78 mm2).](image2)
5. Conclusion

In this paper, a two-level coarse fine TDC in 55 nm CMOS technology is presented for wideband ADPLL application. The first-stage TDC adopts the inverter delay chain, which has a lower resolution while meeting the measurement range requirement, and the second-stage TDC adopts the Vernier delay chain, which has a higher resolution and meets the accuracy requirement, thus giving consideration to both high precision and wide measurement range. Time window technology and circuit multiplexing technology are also employed in the proposed TDC to reduce the circuit power.
consumption and the amount of circuit components. With all the performance figures, power consumption and size, the proposed architecture is suitable for wideband ADPLL application.

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References
[1] R. B. Staszewski, S. Vemulapalli, P. Vallur, J. Wallberg and P. T. Balsara. (2006) 1.3 V 20 ps time-to-digital converter for frequency synthesis in 90-nm CMOS. *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 3, pp. 220-224.
[2] S. Henzler, S. Koepppe, D. Lorenz, W. Kamp, R. Kuenemund and D. Schmitt-Landsiedel. (2008) A Local Passive Time Interpolation Concept for Variation-Tolerant High-Resolution Time-to-Digital Conversion. *IEEE Journal of Solid-State Circuits*, vol. 43, no. 7, pp. 1666-1676.
[3] M. Z. Straayer and M. H. Perrott. (2009) A Multi-Path Gated Ring Oscillator TDC With First-Order Noise Shaping. *IEEE Journal of Solid-State Circuits*, vol. 44, no. 4, pp. 1089-1098.
[4] J. Yu, F. F. Dai and R. C. Jaeger. (2010) A 12-Bit Vernier Ring Time-to-Digital Converter in 0.13 µm CMOS Technology. *IEEE Journal of Solid-State Circuits*, vol. 45, no. 4, pp. 830-842.
[5] M. Zanuso, P. Madoglio, S. Levantino, C. Samori and A. L. Lacaita. (2010) Time-to-Digital Converter for Frequency Synthesis Based on a Digital Bang-Bang DLL. *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 3, pp. 548-555.
[6] M. Lee, M. E. Heidari and A. A. Abidi. (2009) A Low-Noise Wideband Digital Phase-Locked Loop Based on a Coarse–Fine Time-to-Digital Converter With Subpicosecond Resolution. *IEEE Journal of Solid-State Circuits*, vol. 44, no. 10, pp. 2808-2816.
[7] V. K. Chillara. (2014) 9.8 An 860µW 2.1-to-2.7GHz all-digital PLL-based frequency modulator with a DTC-assisted snapshot TDC for WPAN (Bluetooth Smart and ZigBee) applications. *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, San Francisco, CA, pp. 172-173.
[8] A. Elkholy, T. Anand, W. Choi, A. Elshazly and P. K. Hanumolu. (2015) A 3.7 mW Low-Noise Wide-Bandwidth 4.5 GHz Digital Fractional-N PLL Using Time Amplifier-Based TDC. *IEEE Journal of Solid-State Circuits*, vol. 50, no. 4, pp. 867-881.
[9] Y. Wu, M. Shahmohammadi, Y. Chen, P. Lu and R. B. Staszewski. (2017) A 3.5–6.8-GHz Wide-Bandwidth DTC-Assisted Fractional-N All-Digital PLL With a MASH ΔΣ-TDC for Low In-Band Phase Noise. *IEEE Journal of Solid-State Circuits*, vol. 52, no. 7, pp. 1885-1903.
[10] A. Ximenes, G. Vlachogiannakis and R. B. Staszewski. (2017) An Ultracompact 9.4–14.8-GHz Transformer-Based Fractional-N All-Digital PLL in 40-nm CMOS. *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 11, pp. 4241-4254.