3.3-mA 2.8-GHz bufferless LC oscillator directly driving a 10-mm on-chip clock distribution line

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Abstract A bufferless LC oscillator can potentially offer an attractive solution for low-power, high-speed clock distribution due to the absence of repeaters on the clock distribution line and utilization of LC resonance. However, conventional bufferless LC oscillators suffer from a fundamental tradeoff between the frequency and power consumption due to their high-frequency sensitivity. In this paper, we have introduced a low-frequency sensitivity bufferless LC oscillator that is directly connected to a 10-mm on-chip clock distribution line in the TSMC 0.18-µm 1-Poly 6-Metal CMOS technology. The core area of the LC oscillator is only 270 × 280 µm². The measurement results show that a 2.8-GHz oscillation frequency, 3.3-mA current consumption, and −112.8 dBc/Hz phase noise at 1 MHz offset can be achieved.

Keywords: LC-oscillator, clock distribution, transmission line

Classification: Integrated circuits

1. Introduction

1.1 Background

High-speed clock distribution design has increasingly become important in determining the overall performance of VLSI systems as it is associated with the highest power consumption. A large portion (40%–70%) of the total power can be dissipated in microprocessors due to the high swing rate and large capacitance [1, 2, 3]. The effects of the number of inverter-based repeaters on the clock distribution line with increasing frequency and chip area in recent digital systems have gained prominence due to the following reasons. First, a huge amount of power is dissipated due to the large voltage swing level (usually 0 to Vdd). Second, a high-frequency operation is difficult owing to the high voltage swing level. Third, the Vdd sensitivity, known as the power supply rejection ratio, is very high. A bufferless clock distribution can offer an attractive solution to overcome the above stated limitations. However, the fundamental tradeoff between the oscillation frequency and power consumption, as determined by Eq. (1) and (2), presents a practical problem when such a bufferless structure is applied to a conventional LC oscillator. In Eq. (1) and (2), f, Ls, CDo, Rs, and Rp represent the oscillation frequency, series inductance, frequency tuning capacitance, series resistance, and equivalent parallel resistance, respectively as shown in Fig. 1.

\[ f_0 = \frac{1}{2\pi\sqrt{LsCDo}} \]  
\[ I \propto \frac{1}{R_p} \left( R_p \approx \omega LsQ, \quad Q = \frac{\omega Ls}{Rs} \right) \]

1.2 Previous work

Many works have been investigated for low-power resonant clock distribution [4, 5, 6, 7, 8, 9, 10, 11, 12, 13]. A 1.5-GHz bufferless LC oscillator introduced by Mesgarzadeh et al. [4, 5] achieved an ~57% lower clock power as compared to a conventional repeater-based LC oscillator. However, this has not resolved the fundamental tradeoff between the oscillation frequency and power consumption as the circuit structure is based on the conventional LC oscillator shown in Fig. 1. This makes operation at even higher frequencies difficult due to the very small inductor value.

1.3 Objectives and scope of this study

We have previously proposed a theory on the low-frequency sensitivity bufferless LC oscillators [6] to overcome the tradeoffs associated with conventional LC oscillators. In this paper, we present an experimental implementation of the previously proposed LC oscillator with the following conditions. A differential signaling configuration in a 10-mm line is used for the clock distribution line as shown in Fig. 2. Such a structure is commonly used in high-speed serial links that require the highest chip frequency [14, 15, 16, 17]. However in this case, the 10-mm line has been organized to function as a meander line due to the limited chip area. A length of 10 mm allows the consideration of huge chips such as microprocessors [1]. The TSMC 0.18-µm 1-poly, 6-metal CMOS process was used for the fabrication due to the limited options available in our laboratory. A 2.8-GHz target frequency was selected as the maximum frequency in the worst case scenario at FO = 4 (Fan Out) is ~3-GHz for a 0.18-µm fabrication process. This measurement based approach not only establishes the
low-frequency sensitivity feature but also shows the effects of the transmission line on the LC oscillator. This paper is organized as follows. A brief introduction on our proposed bufferless LC oscillator is described in Section 2, while the test chip implementation is detailed in Section 3. The measurement results and analysis along with the main conclusions are described in Sections 4 and 5, respectively.

2. Low-frequency sensitive bufferless LC oscillator

Fig. 3(a) and (b) show the conventional and proposed LC oscillators [6], respectively. Fig. 3(b) indicates that the LC tank is shared between the tuning capacitor oscillators [6], respectively. Fig. 3(b) shows that the impedance $Z_{cs}$ can be expressed by Eq. (3). The solution of Eq. (3) for a denominator equal to 0 is the oscillation frequency $f_{p1}$. The output swing $V_{OUT}$ can be obtained using Eq. (2). Table I shows the theoretical differences between the conventional and proposed LC oscillators. Fig. 4(a) and (b) show the oscillation frequency $f_{p1}$ and output swing $V_{OUT}$. The figures clearly show that the proposed structure has a lower frequency and voltage swing sensitivity with an increase in the output loading $C_L$ as compared to the conventional structure.

$Z_{cs} = \frac{j\omega(L_1 + L_2 - \omega^2L_1L_2C_L)}{1 - \omega^2L_1C_L - \omega^2C_D(L_1 + L_2 - \omega^2L_1L_2C_L)}$ (3)

3. Test chip implementation

Fig. 5 and 6 show the structure of the fabricated circuit and photograph of the chip. The circuit has an 8-shaped differential inductor [18, 19, 20, 21, 22, 23, 24] with $L = 2.86$ nH and $\alpha_{TAP} = 0.5$. The LC oscillator has a core area of only $270 \times 280 \mu\text{m}^2$. The 10-mm on-chip clock distribution line is organized by the meander line using a thick metal layer (M6), and width and space of 2 $\mu$m each taking into consideration the limited chip area and resistive loss. The differential signal obtained after clock distribution is buffered using a 5-stage FO = 2 current-mode logic and finally output with an impedance of 50 $\Omega$ to the PAD for the purposes of measurement.

4. Measurement results and analysis

4.1 Measurement setup

The measurements from the proposed bufferless LC oscil-
Gain of LNA (39.5 dB) has been deducted from the measurement results for the oscillation frequency $f_{\text{osc}}$ and single-ended output swing $V_{\text{OUTP}}$. A comparison is made between the $RC$ and $RLC$ models for the simulation results to investigate whether the effects of the transmission line should be taken into consideration. In this study, the Cadence Assura-RCX and Integrand Software, Inc. EMX models for the simulation results are used. The transmission line length to achieve a higher voltage swing in the far end is not terminated ($=$ open). The wavelength is 50 mm for a relative dielectric constant $\varepsilon_r = 4$. There is a phase change of $\sim 144$ degrees when the reflection-wave returns to the near end. The S11 Smith chart of the 10-mm transmission line shown in Fig. 8 also indicates the expected trend. Thus, the swing of the standing-wave signal becomes much smaller than that of the $RC$ model. However, a significant error still exists between the measurement and $RLC$ model. We believe that the convolution process from the $s$-parameter to the time-domain is the source of this error as this is strongly dependent on the simulation tool. Next, the figure-of-merit (FoM) expressed in Eq. (4) and (5) is compared with the results shown in Table III. It can be seen from Table III that the FoMa of [28] and FoM of [30] have much better performance as compared to the results from our study, which might be due to the following reasons. First, the major difference with respect to the FoMa of [28] results from the inductor area. Our inductor has a simple 2D structure whereas [28] has a stacked 3D structure. Second, there are two major differences with respect to the FoM of [30], namely the circuit structure and capacitive loading. Our circuit structure only has Nch whereas [30] has both the Pch and Nch. This results in a power consumption difference of around 3 dB due to the improved trans-conductance. Next, the capacitive loading in our study is around 2.5 pF while it was only 0.5 pF in [30], which results in a difference of $\sim 6$ dB. Thus, the FoM of [30] is fundamentally 9 dB better than that seen in our study. However, a further improvement (minimum 10 dB) is necessary to be comparable with other state-of-the-art structures. Some solutions to achieve this are as follows: (1) The use of both the Pch and Nch from [30] to improve the trans-conductance and subsequently the power consumption. (2) The selection of an appropriate transmission line length to achieve a higher voltage swing in the standing wave mode. (3) The selection of a frequency greater than 2.8 GHz with advanced technology to improve the $Q$ of the $LC$ oscillator.

### 4.2 Measurement and simulation results

Table II shows a comparison between the measurement and simulation results for the oscillation frequency $f_{\text{osc}}$ and single-ended output swing $V_{\text{OUTP}}$. A comparison is made between the $RC$ and $RLC$ models for the simulation results to investigate whether the effects of the transmission line should be taken into consideration. In this study, the Cadence Assura-RCX and Integrand Software, Inc. EMX models for the simulation results are used. The transmission line length to achieve a higher voltage swing in the far end is not terminated ($=$ open). The wavelength is 50 mm for a relative dielectric constant $\varepsilon_r = 4$. There is a phase change of $\sim 144$ degrees when the reflection-wave returns to the near end. The S11 Smith chart of the 10-mm transmission line shown in Fig. 8 also indicates the expected trend. Thus, the swing of the standing-wave signal becomes much smaller than that of the $RC$ model. However, a significant error still exists between the measurement and $RLC$ model. We believe that the convolution process from the $s$-parameter to the time-domain is the source of this error as this is strongly dependent on the simulation tool. Next, the figure-of-merit (FoM) expressed in Eq. (4) and (5) is compared with the results shown in Table III. It can be seen from Table III that the FoMa of [28] and FoM of [30] have much better performance as compared to the results from our study, which might be due to the following reasons. First, the major difference with respect to the FoMa of [28] results from the inductor area. Our inductor has a simple 2D structure whereas [28] has a stacked 3D structure. Second, there are two major differences with respect to the FoM of [30], namely the circuit structure and capacitive loading. Our circuit structure only has Nch whereas [30] has both the Pch and Nch. This results in a power consumption difference of around 3 dB due to the improved trans-conductance. Next, the capacitive loading in our study is around 2.5 pF while it was only 0.5 pF in [30], which results in a difference of $\sim 6$ dB. Thus, the FoM of [30] is fundamentally 9 dB better than that seen in our study. However, a further improvement (minimum 10 dB) is necessary to be comparable with other state-of-the-art structures. Some solutions to achieve this are as follows: (1) The use of both the Pch and Nch from [30] to improve the trans-conductance and subsequently the power consumption. (2) The selection of an appropriate transmission line length to achieve a higher voltage swing in the standing wave mode. (3) The selection of a frequency greater than 2.8 GHz with advanced technology to improve the $Q$ of the $LC$ oscillator.

| Parameters | Measurement | Simulation ($RC$) | Simulation ($RLC$) |
|------------|-------------|-------------------|-------------------|
| $f_{\text{osc}}$ | 2.83 GHz | 2.54 GHz | 2.74 GHz |
| $V_{\text{OUTP}}$ | -61.7 dBm | 3.7 dBm | -20.6 dBm |

**Condition:** $V_{\text{DD}} = V_{\text{AG}} = 1.8 \text{ V}$

Gain of LNA (39.5 dB) has been deducted from $V_{\text{OUTP}}$.  

### 4.3 Analysis

The measurement and simulation results will be analyzed in this section. First, the $RLC$ model shows a better match with respect to the oscillation frequency as compared to the $RC$ model. This indicates that the parasitic inductance cannot be ignored considering the transmission line effect. The $RLC$ model has a higher oscillation frequency as compared to the $RC$ model as the parasitic inductance cancels out the parasitic capacitance to a certain extent. Second, the $RLC$ model shows a better match for the output swing as compared to the $RC$ model. This indicates that the transmission line effects cannot be ignored as also seen in the case of the oscillation frequency [25, 26, 27]. The much smaller output swing of the $RLC$ model as compared to that of the $RC$ model can be intuitively explained as follows. Our test chip operates at a frequency of around 3 GHz and has a 10-mm length. A reflection wave is produced as the far end is not terminated ($=$ open). The wavelength is 50 mm for a relative dielectric constant $\varepsilon_r = 4$. There is a phase change of $\sim 144$ degrees when the reflection-wave returns to the near end. The S11 Smith chart of the 10-mm transmission line shown in Fig. 8 also indicates the expected trend. Thus, the swing of the standing-wave signal becomes much smaller than that of the $RC$ model. However, a significant error still exists between the measurement and $RLC$ model. We believe that the convolution process from the $s$-parameter to the time-domain is the source of this error as this is strongly dependent on the simulation tool. Next, the figure-of-merit (FoM) expressed in Eq. (4) and (5) is compared with the results shown in Table III. It can be seen from Table III that the FoMa of [28] and FoM of [30] have much better performance as compared to the results from our study, which might be due to the following reasons. First, the major difference with respect to the FoMa of [28] results from the inductor area. Our inductor has a simple 2D structure whereas [28] has a stacked 3D structure. Second, there are two major differences with respect to the FoM of [30], namely the circuit structure and capacitive loading. Our circuit structure only has Nch whereas [30] has both the Pch and Nch. This results in a power consumption difference of around 3 dB due to the improved trans-conductance. Next, the capacitive loading in our study is around 2.5 pF while it was only 0.5 pF in [30], which results in a difference of $\sim 6$ dB. Thus, the FoM of [30] is fundamentally 9 dB better than that seen in our study. However, a further improvement (minimum 10 dB) is necessary to be comparable with other state-of-the-art structures. Some solutions to achieve this are as follows: (1) The use of both the Pch and Nch from [30] to improve the trans-conductance and subsequently the power consumption. (2) The selection of an appropriate transmission line length to achieve a higher voltage swing in the standing wave mode. (3) The selection of a frequency greater than 2.8 GHz with advanced technology to improve the $Q$ of the $LC$ oscillator.

![Image](image-url)
Area only power, high-frequency system can be realized by selecting the long transmission line is directly connected. A low-frequency system also found that the standing wave mode is generated when the sensitivity feature enables high-speed operation even in small mm on-chip clock distribution line. The low-frequency system is directly connected to a 10-mm transmission line (input: 50Ω, output: open).

Table III. Comparison results for the FoM and FoMA from various studies.

| Tech [nm] | [28] | [29] | [30] | [31] | This work |
|-----------|------|------|------|------|-----------|
| 65 | 180 | 130 | 55 | 180 |
| Area [μm²] | 484 | 1260 | 6955 | 5976 | 7560 |
| Ω | 50 |
| L(Δf) [dBc/Hz] | −110 | −116 | −120.6 | −100.5 | −112.8 |
| f₀ [GHz] | 21 | 5.32 | 5.29 | 80 | 2.83 |
| Δf [MHz] | 10 | 1 | 1 | 1 | 1 |
| P_{dc} [mW] | 1.92 | 5.71 | 1.98 | 18 | 5.94 |
| FoM [dBc/Hz] | −173.6 | −183.0 | −192.1 | −186.0 | −174.1 |
| FoMa [dBc/Hz] | −206.8 | −181.9 | −193.7 | −188.2 | −185.3 |

\[
\text{FoM} = L(\Delta f) - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{dc}}{1 \text{ mW}}\right) \\
\text{FoMa} = \text{FoM} + 10\log\left(\frac{\text{Area}}{1 \text{ mm}^2}\right) 
\]

Here,

- \(f_0\): oscillation frequency
- \(\Delta f\): offset frequency
- \(P_{dc}\): power consumption
- \(L(\Delta f)\): phase noise at \(\Delta f\)

5. Conclusion

In this paper, we introduced a low-frequency sensitivity bufferless LC oscillator that is directly connected to a 10-mm on-chip clock distribution line. The low-frequency sensitivity feature enables high-speed operation even in the case of heavy capacitive loading. In addition, it was also found that the standing wave mode is generated when the long transmission line is directly connected. A low-power, high-frequency system can be realized by selecting an appropriate transmission line length and frequency. The test chip has been fabricated using the TSMC 1-poly, 6-metal CMOS technology with an oscillator core area of only 270 × 280 μm². The measurement results demonstrate that a 2.83-GHz frequency, 3.3-mA current consumption, and −112.8 dBc/Hz phase noise at 1-MHz offset can be achieved.

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Fig. 8. The S11 smith chart of the 10-mm transmission line (input: 50Ω, output: open).
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