Investigation on electrical properties in silicon p-n junction diode with thermal diffusion variation for solar cell applications

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Abstract Diodes were fabricated on n-type silicon substrate using thermal diffusion method. Samples were diffused with boron to make a p-n junction diode at different thermal diffusion temperature such as 700 ºC, 800 ºC and 900 ºC. Time taken for heated the samples were varied with 60 minutes, 90 minutes and 120 minutes. The effect on electrical properties of p-n junction silicon diode through variation thermal diffusion temperatures and times were measured using two and four point probe. The electrical measurement (I-V) results show that samples heated at 900 ºC temperature for 120 minutes diffusion produced the lowest sheet resistance and resistivity which are $1.50 \times 10^7 \, \Omega/\square$ and $1.65 \times 10^2 \, \Omega\text{-cm}$, respectively as compared to others. On the other hand, the highest current value was obtained 54.60 mA when the supply voltage at 10 V. Thus, this indicates that samples heated at 900 ºC with 120 minutes annealing was having higher concentration by having better resistivity and sheet resistance as compared to samples with lower diffusion temperature and annealing time. Hence, it show that samples with this parameter have potential to be applied for production of n-type silicon solar cells that aiming for having better electrical performance.

1. Introduction

Last few decades due to the environmental problems and energy crisis [1], emerging of green technology industry has grown tremendously. One of the alternative green technology industry is energy conversion device namely Photovoltaic (PV) or solar cell which is used to convert the energy from the sun or light into electricity. Nowadays, large portion of commercial silicon solar cell development comprises the usage of p-type silicon as a substrate [2]. This is because p-type silicon solar cell has the well-established fabrication PV technology [2]. However, this commercial p-type silicon solar cell suffers with the issue of light induced degradation (LID) which have affected device efficiency performance. The LID is related to boron-oxygen (B-O) complexes formed the metastable defect with decreases minority carrier generated by effect of light [3, 4]. Thus, this condition will affected the device performance with reduction of conversion efficiency [3, 4].

In order to resolve the reduction conversion efficiency performance in p-type silicon solar cell and also producing a cost effective device, researchers [1-9] have subsequently give great attention in development of n-type silicon solar cell because of the advantages it can offers compared to than that
p-type substrate. It has been reported [3, 5, 6, 7] that n-type silicon having longer diffusion length hence having higher tolerance to any metal impurities [3, 5, 6, 7]. It also does not contain any boron-oxide pairs [3, 6, 8] which considered as origin of LID. As a result, n-type silicon solar cell can potentially maintain the efficiency performance without degradation during illumination of light. However, n-type crystalline silicon substrate is still a new route in PV technology with the aim of having high-efficiency and cost-effective modules as compared to the established p-type silicon technology. By knowing the boron doping profile into n-type silicon, results of boron dopant profile can be optimized [6] hence can be applied for manufacturing of n-type silicon solar cell. Based on the above issue, this research was conducted and focused on fabrication of p-n junction diode using n-type crystalline silicon as a substrate. This is to investigate the effect on electrical properties of silicon p-n junction diode with thermal diffusion variation such as temperature and time. By identifying the potential diffusion parameter (temperature and time) thus effect of LID can be reduced and enhance the device electrical conversion performance.

2. Experimental details

Figure 1 shows the cross-sectional of p-n junction diode that have been fabricated in this research. The overall device mask pattern is 15 mm x 15 mm, with the opening window for boron to be doped is 15 mm x 2 mm and 15 mm x 4 mm for metal contact. The fabrication process of a diode takes place by using 0.5 μm thick bare n-type silicon as a substrate. Silicon dioxide, SiO₂ was thermally grown for 1 hour using furnace tube at above 1000 °C temperature as it can produce high quality barrier or dielectric. Boron was diffused into n-type substrate on the selected window using thermal diffusion process with boron dopant source for producing the p-n junction. Different samples were annealed at 700 °C, 800 °C and 900 °C diffusion temperatures. Each of the samples were heated at different diffusion time with 60 minutes, 90 minutes and 120 minutes. Aluminium was deposited using Physical Vapour Deposition (PVD) for the metal contact, thus device electrical performance (I-V) can be investigated. Along the fabrication process, the sample was inspect thoroughly with measuring the thickness using FILMETRICS, resistivity and sheet resistance using four-point probe before electrical measurement (I-V) of p-n junction diode can be determined.

3. Results and Discussions

Each of material have its own resistivity ρ, which contributed to device performance such as series resistance, capacitance and threshold voltage. The resistivity ρ, is the electrical resistance per unit length and per unit of cross-sectional area. On the other hand, for diffuse layers, resistivity is the strong function of depth. Thus, the sheet resistance $R_{sh} = \rho / t$ is commonly used to calculate with having unit ohm per square ($\Omega/\square$), which can be thought of as depth integral of the dopant atom density regardless of its vertical spatial doping density variation [12]. Measurement on resistivity and sheet resistance after boron diffusion have taken place in order to investigating the device performance using four point probe. This is because the diffusion process will modified the wafer resistivity. In this research, firstly mapping technique have been used to measure the uniformity and thickness of SiO₂
using FIlMETRICS. The samples were measured at nine different places on the surface wafer. It can be observed that, after thermal annealing process the grey silicon wafer changes into bluish colour covered all over the wafer indicating that SiO$_2$ have been uniformly growth on the sample. In this case, the average SiO$_2$ thickness is 0.5 µm after 1 hour annealing. Next, effect of device performance after boron diffusion process is investigate using four point probe. Results were discussed in subsection 3.1 and 3.2.

3.1 Sheet resistance & resistivity at thermal diffusion variation.

Figure 2 and figure 3 show the graph of sheet resistance and resistivity that having variation thermal diffusion temperatures at 700 ºC, 800 ºC and 900 ºC. The samples also varies at diffusion times with 60 minutes, 90 minutes and 120 minutes. Figure 2 shows sample that diffused at 900 ºC with 60 minutes having sheet resistance $1.7 \times 10^7 \, \Omega/\square$, whereas at 120 minutes diffusion it decreases into $1.5 \times 10^7 \, \Omega/\square$. The reduction of samples resistivity can also be observed on the resistivity versus time graph in figure 3. For example sample at 900 ºC with 60 minutes diffusion having resistivity $1.9 \times 10^2 \, \Omega\cdot cm$, while at 120 minutes time diffusion the sample resistivity reduced into $1.65 \times 10^2$. It can be concluded form graph figure 2 and 3, the value of samples sheet resistance and resistivity decreased when the temperature and time for thermal diffusion increased. This trend is agree with the theory where diffusion process will modified sample resistivity hence enhance the performance by having lower resistance [11]. It is also expected that higher temperatures produced higher doping concentration thus improve the performances of devices.

![Fig. 2 Sheet resistance of p-n junction diode at different diffusion temperatures and times.](image-url)
3.2 I-V measurement of p-n junction diode
Figure 4 show results samples heated at 700 °C at different diffusion times which are 60 minutes, 90 minutes and 120 minutes. Sample annealed at 700 °C for 120 minutes have the higher value of current than other wafers as expected. It produces 24.6 mA of current value in 10 V of voltage value. It follows with wafer at 700 °C for 90 minutes which produces 20.4 mA of current value and 18.9 mA of value current for the wafer at 700 °C for 60 minutes.
Three samples were diffused at different times (60 minutes, 90 minutes and 120 minutes) at 800°C temperature. Results in figure 5 shows that, all samples having not much different current value and the pattern of the graph was similar to each other. It is expected during this temperature, the diffused samples started to activated hence affected to the graph behavior of a p-n junction diode. The higher current value at 33.80 mA for sample heated for 120 minutes. Then, followed by sample with 90 minutes which is 32.70 mA and lastly sample heated for 60 minutes with lower current value which is 31.17 mA.

![I-V Diodes Characteristic](image)

Fig. 5 I-V diode characteristic for samples at 800 °C temperature.

Figure 6 show results annealed at 900 °C of diffusion temperature with different times. As expected, the higher current value was produced by wafer with temperature 900 °C in 120 minutes which is 54.60 mA. Then, followed by samples heated for 90 minutes and 60 minutes with currents values 43 mA and 36.9 mA, respectively. The trend of p-n junction diode can clearly observed on the graph.
In comparison between the different diffusion temperatures (700 °C, 800 °C and 900 °C) and times (60 minutes, 90 minutes and 120 minutes) samples annealed at 900 °C temperature for 120 minutes produced better performances as compared to the others with highest current value which is 54.60 mA and smoother I-V curve as shown in figure 7. It is believed samples with higher concentration have low resistivity value and sheet resistance values as discussed above. For I-V measurement, current produced by all samples at different temperatures and times were in milliamperes (mA) which satisfied with the theory values. Thus, indicates that samples were successfully fabricated in this research by showing the p-n diodes characteristics. It can also be concluded, the higher electrical conductivity gives better performance of the devices. Hence, this diffusion temperature and times can potentially to be used in further investigation for manufacturing the n-type silicon solar cell application.

Fig. 6 I-V diode characteristic for samples at 900 °C temperature.
4. Conclusions
This research presents the effect on electrical properties in silicon p-n junction diode with thermal diffusion variation. A p-n junction diode with boron doped into n-type silicon substrate has been successfully fabricated using thermal diffusion method with solid dopant source. In this process, the effect different diffusion temperature (700 °C, 800 °C, and 900 °C) and different diffusion time (60 minutes, 90 minutes and 120 minutes) were studied. Results showed the potential diffusion temperature and time of boron doping was at 900 °C for 120 minutes. This is because samples produced low sheet resistance and resistivity which are 1.50x10⁷ Ω/□ and 1.65x10² Ω-cm, respectively. Based on the results, the low sheet resistance and resistivity will be able to produces higher electrical conductivity [12]. Meanwhile, for I-V measurement sample diffused at 900 °C for 120 minutes having the highest current value with 54.60 mA at 10 V as compared to others. It clearly shows that by having longer diffusion time with higher temperature better performance can be achieved. In conclusion, the highest doping concentration and highest electrical conductivity can improve the performance of p-n junction and potentially to be applied for manufacturing of n-type silicon solar cell.

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References
[1] K. W. J. Barnham, M. Mazzer and B. Clive, “Resolving the energy crisis: nuclear or photovoltaics”, Nature Materials, pp.161 – 164, 2006, doi: 10.1038/nmat1604
[2] M. A. Green, K. Emery, Y. Hishikawa, W. Warta and E. D. Dunlop, “Solar cell efficiency tables (version 41)”, Prog. Photovolt: Res. Appl. Vol. 21, pp. 1–11, 2013

[3] C. Xiao, D. Yang, X. Yu, R. Wang and D. Que, “Analysis of the photovoltaic properties of n-type compensated silicon solar cells with the Al-alloyed emitter”, Journal of Alloy and Compound, vol. 561, pp. 28-32, 2013

[4] F. Rougieux, C. Samundsett, K. C. Fong, A. Fell, P. Zheng, D. Macdonald, J. Degoulang, R. Einhaus and M. Forster, “High efficiency UMG silicon solar cells: impact of compensation on cell parameters”, Prog. Photovolt: Res. Appl., 2015

[5] J. Benick, B. Hoex, M. C. M. van de Sanden, W. M. M. Kessels, O. Schultz and S. W. Glunz, “High efficiency n-type Si solar cells on Al2O3-passivated boron emitters” Appl. Phys. Lett. Vol. 92, 253504, 2008

[6] E-Y. Kim and J. Kim “Effects of the Boron-Doped p+ Emitter on the Efficiency of the n-Type Silicon Solar Cell” Advance in Material Science and Engineering, 974507, 2013

[7] U. Gangopadhyay, S. Roy, S. Garain, S. Jana and S. Das “Comparative simulation study between n-type and p-type Silicon Solar Cells and the variation of efficiency of n-type Solar Cell by the application of passivation layer with different thickness using AFORS HET and PC1D”, IOSR Journal of Engineering, vol. 2, Issue: 8, pp. 41-48, 2012

[8] S. W. Glunz, S. Rein, J. Y. Lee, and W. Warta, “Minority carrier lifetime degradation in borondoped Czochralski silicon”, Journal of Applied Physic, vol. 90, no. 5, 2001

[9] A. Rahman and S. H. Lee “Advancement in N-type Base Crystalline Silicon Solar Cells and Their Emergence in the Photovoltaic Industry”, The Scientific World Journal, pp.1-13, 2013

[10] J. Bullock, P. Zheng, Q. Jeangros, M. Tosun, M. Hettick, C. M. Sutter-Fella, Y. Wan, T. Allen, D. Yan, D. Macdonald, S. D. Wolf, A. Hessler-Wyser, A. Cuevas and A. Javey, “Lithium Fluoride Based Electron Contacts for High Efficiency n-Type Crystalline Silicon Solar Cells”, Advance Energy Material, 2016

[11] S. Li, Y. Gao, R. Fan, D. Li and D. Yang, "Room-Temperature Near-Infrared Electroluminescence from Boron-Diffused Silicon P-N Junction Diodes", Front. Mater., vol. 2, 2015

[12] Dieter K. Schroder; Semiconductor Material and Device Characterization, 3rd Ed.; John Wiley; 2006.