Research Toward a Heterogeneously Integrated InGaN Laser on Silicon

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A heterogeneously integrated InGaN laser diode (LD) on Si is proposed as a path toward visible wavelength photonic integrated circuits (PICs) on Si. Herein, InGaN films are vertically stacked on a TiO$_2$ waveguide (WG) fabricated on a Si wafer by bonding. In the light propagation direction, it is composed of a hybrid InGaN/TiO$_2$ section, a TiO$_2$ WG, an adiabatic taper, and mirrors that can form a cavity. As the refractive index of GaN is well matched with that of TiO$_2$, the optical transverse mode extends to both the GaN and TiO$_2$ in a hybrid mode. Modes between a hybrid InGaN/TiO$_2$ and a pure TiO$_2$ WG can transfer with an adiabatic taper structure. The coupling loss is calculated to be less than 0.5 dB with fairly short taper length of 78 μm and tip width of 200 nm. GaN substrate removal and bonding are critical fabrication steps of this LD and PIC. The substrate removal is successfully done by photoelectrochemical etching. Although direct bonding of GaN wafers with thermal oxide on Si is successful, GaN epitaxial wafers are more difficult. An implication and remedy of this is discussed in terms of surface roughness of GaN epitaxial film.

1. Introduction

Over the past two decades, Si has been demonstrated as a photonic platform and is now in high volume production. The optical transparency and high refractive index contrast with cladding material SiO$_2$ make Si particularly suited for standard telecommunication bands such as O-band (1260–1360 nm) and C-band (1530–1565 nm), achieving dense integration of photonic integrated circuits (PICs). Various photonic components as well as PICs have been demonstrated using a silicon-on-insulator (SOI) wafer, including modulators, photodetectors, grating couplers (GCs), distributed Bragg reflection (DBR) mirrors, loop mirrors, phased array, and large-scale integrated on-chip photonic–electronic systems. Si PICs, however, had suffered from a lack of an efficient electrically pumped light source due to the indirect gap of Si. There have been several attempts to bond a discrete III–V laser diode (LD) to Si PICs but this approach requires a precise alignment and has limited scalability. This issue has been solved by a heterogeneously integrated Si laser where unprocessed III–V material is bonded to Si waveguide (WG) fabricated on the SOI wafer. In this platform, optical gain is provided by the III–V material due to evanescent coupling to Si WG, whereas a laser cavity can be formed inside the Si WG. As the propagation loss of a Si WG is much lower than that of III–V counterpart, the total quality factor (Q) of heterogeneous III–V/Si resonators can be increased by replacing lossy III–V WG with low loss Si WG, thereby improving the coherence of semiconductor laser. More importantly, multiple III–V dies bonded to Si wafer can be processed lithographically simultaneously, so that no critical bonding alignment is required, allowing for high volume production of Si photonics transceivers for data center markets. Well-established Si processing and testing capability on larger wafers can be utilized to reduce the cost while improving the reliability of PICs. The other benefit of heterogeneous integration is to use the well-established device library of Si photonics to provide additional functionality, such as surface emission, wavelength tunability, narrower line width, and beam steering.

The aforementioned success of the heterogeneous integration at telecommunication wavelengths can be extended into the visible light region with InGaN PICs on Si. Instead of Si WGs, the WG may comprise Si$_3$N$_4$ or TiO$_2$ that is transparent in visible light region. The ultralow propagation loss of Si$_3$N$_4$ WG and corresponding high Q ring resonator have been demonstrated, but Si$_3$N$_4$ has a lower refractive index than GaN, so that the mode is predominantly confined in the GaN region. Therefore, it would be challenging to transfer mode between a hybrid InGaN/Si$_3$N$_4$ section and Si$_3$N$_4$ WG with an adiabatic taper structure. In contrast, TiO$_2$ has a comparable refractive index with GaN, so that it is straightforward to transfer the mode between a hybrid InGaN/TiO$_2$ section and pure TiO$_2$ WG with the adiabatic
taper structure. Therefore, TiO$_2$ is chosen as a WG material. An evanescent coupling is, however, more critical at a shorter wavelengths, for an evanescent tail is thinner at shorter wavelengths, as is shown by Equation (1).

$$E \propto e^{i \frac{2\pi}{\lambda} n_{eff} \frac{d}{2}}$$

(1)

where $E$ is the field amplitude at a distance, $d$, from the core-cladding interface, $\lambda$ is the wavelength, $n_{eff}$ is the effective index of the mode, and $n_q$ is the refractive index of the cladding.

With this in mind, here, we first calculate the optical transverse mode in a heterogeneously integrated GaN/TiO$_2$ LD and confirm that it extends both to GaN and TiO$_2$ regions. We then design an adiabatic taper structure that can transfer the mode between a hybrid GaN/TiO$_2$ section and a pure TiO$_2$ WG with a low coupling loss by eigenmode expansion (EME) solver, confirmed by finite difference time domain (FDTD) solver, but with some discrepancies. We have then developed four primary technologies to fabricate heterogeneously integrated InGaN/ TiO$_2$ LD such as TiO$_2$ WG, edge emitting InGaN LD with topside n-contact, GaN substrate removal, and direct bonding of GaN with Si by plasma activation.

2. Design of a Heterogeneously Integrated InGaN/TiO$_2$ LD

Figure 1a shows a schematic of a heterogeneously integrated InGaN/TiO$_2$ LD that is composed of a hybrid InGaN/TiO$_2$ section, an adiabatic taper structure, DBR mirrors, and a GC. The adiabatic taper structure can transfer a mode between a hybrid InGaN/TiO$_2$ section and pure TiO$_2$ WG with a low coupling loss by eigenmode expansion (EME) solver, confirmed by finite difference time domain (FDTD) solver, but with some discrepancies. We have then developed four primary technologies to fabricate heterogeneously integrated InGaN/TiO$_2$ LD such as TiO$_2$ WG, edge emitting InGaN LD with topside n-contact, GaN substrate removal, and direct bonding of GaN with Si by plasma activation.

2.1. Fundamental Transverse Electric Mode of a Heterogeneous InGaN/TiO$_2$ Section

Figure 1b shows a schematic cross-sectional structure of a hybrid InGaN/TiO$_2$ section of heterogeneously integrated LD. The InGaN layer stack structure adopted here is a University of California Santa Barbara (UCSB) standard LD structure except for the thickness of GaN n-cladding layer.\cite{20} We set the thickness of the n-cladding layer as 100 nm to satisfy both sufficient electrical conductivity of the n-cladding layers and an efficient coupling between InGaN and TiO$_2$ WGs. Dispersion of refractive index for In$_x$Ga$_{1-x}$N and Al$_x$Ga$_{1-x}$N alloys as well as the relation of bandgap with alloy molar fraction $x$ is deduced from Bergmann and Casey.\cite{21} whereas the dispersion of refractive index of TiO$_2$ is taken from Siebke et al.\cite{22} Figure 1c shows a fundamental transverse electric (TE) mode of a hybrid InGaN/TiO$_2$ section with 1000 nm of TiO$_2$ rib width for $\lambda$ of 450 nm. $\Gamma$ of MQWs is 1.9%, whereas $\Gamma$ of TiO$_2$ WG is 28%.

![Figure 1](image-url)
TiO₂ WG is reduced to 500 nm, Γ of MQWs and TiO₂ WG is 2.5% and 9.3%, respectively. This shows that Γ can be tuned with the width of TiO₂ WG, which is an important feature of the heterogeneous platform to engineer the modal profile.

2.2. Adiabatic InGaN/TiO₂ Taper

Figure 2 shows a schematic adiabatic InGaN/TiO₂ taper structure. Upper layers from GaN p-cladding to MQW active layer constitute an upper taper structure, whereas the bottom n-layers such as InGaN guiding and GaN cladding layers constitute a lower taper structure. Double-sectioned tapers instead of straight tapers are used to shorten the taper length. A rib width of GaN is 2 μm, whereas both tip widths are 200 nm. The width of TiO₂ WG is 500 nm. Importantly, this can be fabricated by a KrF excimer laser stepper. Based on this structure, EME is performed, and various taper lengths including 38, 78, and 116 μm turned out to have low coupling loss. From the perspective of low loss mode transfer, longer taper is better. The longer taper, however, has unpumped MQW region due to inefficient injection of carriers toward the tip of taper, leading to absorption. In this regard, we assume 78 μm taper length is well balanced, sufficiently long for low loss mode transfer and short for avoiding unpumped region. Table 1 shows a table of square of scattering matrix for the 78 μm long taper obtained with EME solver where “1” stands for a fundamental TE mode of port 1, whereas “2” for fundamental TE mode of port 2. The taper is composed of 56 μm long upper and 21 μm long lower tapers with a separation of 1 μm. The coupling loss is very low, 0.14 dB for either direction while reflection at each port is extremely low <50 dB. Here, a straight TiO₂ WG is used but the use of tapered TiO₂ WG would be advantageous for shorter taper and lower coupling loss.[23] Figure 3 shows a cross-sectional xz field profile, showing smooth mode transfer.

The EME solver is an efficient way to design and optimized long tapers because of the low computational time. Here, FDTD (Lumerical FDTD solution) is used to confirm the validity of EME results. Table 1 shows a table of square of scattering matrix for the 78 μm long taper with FDTD solver. Basically, similar results are obtained, but there are some quantitative discrepancies. First, the reflection at each port is higher compared with EME results. The coupling losses that occur when a fundamental TE mode is transferred from port 1 to port 2 (S₂₁²)

![Figure 2](image1.jpg)

**Figure 2.** A schematic adiabatic InGaN/TiO₂ taper structure. A rib width of GaN is 2 μm, whereas both tip widths for upper and lower taper are 200 nm. The width of TiO₂ WG is 500 nm.

![Figure 3](image2.jpg)

**Figure 3.** A cross-sectional xz field profile of 78 μm long adiabatic InGaN/TiO₂ taper for λ of 450 nm. a) Mode transfer simulated by EME solver. b) Mode transfer from port 1 to 2 and c) mode transfer from port 2 to 1 simulated by FDTD.

| EME | 1 | 2 |
|-----|---|---|
| 1   | −79 dB (1.35 × 10⁻⁴) | −0.14 dB (0.968) |
| 2   | −0.14 dB (0.968) | −50 dB (9.79 × 10⁻⁴) |

| FDTD | 1 | 2 |
|------|---|---|
| 1    | −60 dB (1.10 × 10⁻⁴) | −0.43 dB (0.906) |
| 2    | −0.42 dB (0.906) | −41 dB (7.23 × 10⁻⁴) |

a¹: fundamental TE mode of port 1; b²: fundamental TE mode of port 2.
or from port 2 to port 1 ($S_{12}^2$) are slightly higher, 0.42–0.43 dB, compared with EME results. But, the total transmission is high in either directions: transmission from port 1 to port 2 ($T_{21}$) = 0.11 dB; transmission from port 2 to port 1 ($T_{12}$) = 0.28 dB. This difference between total transmission and coupling loss corresponds to the generation of higher order modes. Figure 4a shows reflection at each port ($S_{11}^2$, $S_{22}^2$), whereas Figure 4b shows coupling loss ($S_{11}^2$ and $S_{12}^2$) and total transmission ($T_{21}$ and $T_{12}$) for various total taper lengths (38, 78, and 116 µm). Here, the 38 µm-long taper is composed of 16 µm long upper and 21 µm long lower tapers with a separation of 1 µm, whereas the 116 µm-long taper is composed of 84 µm long upper and 31 µm long lower tapers with a separation of 1 µm. As taper length is longer, reflection at port 1 is kept low, but reflection at port 2 becomes lower with taper length. Obviously, reflection at the taper should be minimized because the cavity should be formed by DBR mirrors, not by the tapers, so that longer taper is preferred in this regard. The coupling losses are comparably low for 38 and 78 µm, but drops for 116 µm. But this would be a sort of tuning problem. Indeed the coupling loss is resumed to be 0.49–0.50 dB at wavelength of 440 nm. Therefore, lower coupling loss would be achieved by squeezing the taper length slightly from 116 µm. Figure 3b,c shows cross-sectional $xz$ field profile simulated by FDTD solver for light propagating from port 1 to 2 and from port 2 to 1, respectively. The field profiles are almost the same, but it would be intriguing to see subtle difference depending on light-propagating direction. Light is smoothly introduced through TiO$_2$ WG and bouncing in a hybrid GaN/TiO$_2$ section for light propagation from port 1 to 2 (Figure 3b) while vice versa for light propagation in an opposite direction (Figure 3c).

3. Fabrication of Heterogeneously Integrated InGaN/TiO$_2$ LD

There are two approaches to integrate III–V LDs on Si, direct growth or bonding. Recently, electrically injected InGaN LD directly grown on Si has been successfully demonstrated, which is intriguing from the perspective of cost reduction but has suffered from a short lifetime due to significant level of threading dislocations (TDs).$^{[24]}$ The status of GaAs LDs epitaxially grown on Si is more advanced, but TDs still limit the lifetime.$^{[25]}$ In contrast, the bonding approach has solved the reliability issue of InP LDs on Si, demonstrating stable operation at a temperature of 80 ºC and a current of 180 mA for more than 19 000 h,$^{[26]}$ because there are virtually no TDs in InP material when grown on a native substrate. Low temperature bonding does not introduce additional TDs or any damages due to the difference of coefficient of thermal expansion (CTE). In addition, the InGaN LD grown on Si uses a very thick buffer layer, more than 1 µm, to overcome large lattice mismatch or large difference of CTE, resulting in a very weak evanescent coupling between InGaN and TiO$_2$ WGs. This is particularly relevant at shorter wavelength as discussed earlier. Therefore, bonding approach is used in this article.

The entire fabrication process of heterogeneously integrated InGaN/TiO$_2$ LD is as follows. First, an InGaN epitaxial layer grown on GaN wafer is bonded to a carrier wafer. This is followed by a photoelectrochemical (PEC) undercut etch in a KOH solution by shining filtered LED light, such that carriers are predominantly generated in a sacrificial InGaN MQW with an active MQW protected by dielectric film.$^{[26]}$ After the GaN substrate is removed, the InGaN films on the carrier wafer are bonded to a TiO$_2$ WG fabricated on a Si wafer. Then, the carrier wafer is removed, followed by GaN processing by lithography to make the LD. The bonding-twice approach is a prerequisite to make a carrier spreading layer n-GaN, for the bonding-once approach requires a p-GaN carrier spreading layer, which increases the series resistance of the LD significantly.

The fabrication process can be broken up into four primary technologies: TiO$_2$ WG fabrication, semipolar GaN (202 $\bar{1}$) edge emitting LD on GaN with topside n-contacts, bonding of GaN with the WG fabricated on a Si and GaN substrate removal by PEC undercut etch. A choice of GaN crystalline plane is relevant to the PEC etch. Semipolar GaN (202 $\bar{1}$) that we have chosen is just 15° off from $m$-plane that shows smooth etched surface, so that (202 $\bar{1}$) would show less rough etched surface compared with $c$-plane. In addition, (202 $\bar{1}$) is suitable for longer wavelength lasing, which is favorable to reduce the propagation loss of the WG both in terms of material loss and scattering at a WG interface.
3.1. Fabrication of TiO₂ WG

TiO₂ was sputtered by a gas mixture of Ar and O₂ to deposit TiO₂ film, followed by rapid thermal annealing (RTA) at 400 °C for 15 min. Spectroscopic ellipsometry (Woolam) shows that the TiO₂ film has high refractive index comparable with effective refractive index of typical InGaN LD stack while maintaining a low extinction coefficient: n = 2.57; k = 0 at λ of 450 nm (mean squared error = 8.102). The TiO₂ WG was lithographically patterned by a KrF excimer laser stepper and fabricated by inductively coupled plasma (ICP) etch using CHF₃. Although the propagation loss of TiO₂ WG has not been measured yet, heterogeneous platform could engineer the modal profile to minimize the loss due to TiO₂ WG, as is discussed earlier, even if the propagation loss of TiO₂ WG were high.

3.2. Fabrication of Edge-Emitting InGaN LD with Topside n-Contact

An epitaxial structure optimized for edge-emitting LD was grown by atmospheric pressure metal organic chemical vapor deposition on freestanding (202idi) bulk GaN substrates (Mitsubishi Chemical). The LD structure consisted of 1.2 μm n-GaN, a 65 nm In₀.₀₇Ga₀.₉₃N n-guiding layer, two quantum well (QW) active layers consisting of 4 nm InGaN wells and 7 nm GaN barriers, a 10 nm p-AlₓGa₀.₉₋ₓN electron blocking layer (EBL), a 65 nm p-In₀.₀₇Ga₀.₉₃N guiding layer, 650 nm of p-GaN cladding, and an 20 nm p⁺⁺-GaN contact layer. The reason to use two QW active layers is to reduce the threshold current. Heat dissipation of heterogeneously integrated LDs may be impeded by thermal oxide, so that lower current injection is preferred to suppress heat generation. Experimental results have shown that the threshold current decreases as the number of QWs decreased from 4 to 2 and increased for single QW, probably due to reduced modal gain. It should be also noted that lasing of heterogeneously integrated InP/Si LD can be observed up to 150 °C despite the presence of SiO₂ that seemingly impedes heat transfer from the LD region to a Si substrate.

The backside of heterogeneously integrated LDs is occupied by SiO₂ and Si, so that topside n-contacts should be used instead of backside n-contact. For the fabrication of edge-emitting LD with topside n-contact, ridges were defined by a reactive ion etch (RIE), immediately followed SiO₂ deposition, allowing for a subsequent self-aligned lift-off process. Pd/Au p-contacts were deposited by electron beam evaporation and lift-off. A via for access to n-layer was fabricated by ICP to etch down to n-GaN cladding layer. Ti/Al/Ni/Au n-contacts were deposited by electron beam evaporation and lift-off. RTA at 300 °C was performed for n-contact. Ti/Au contact pads were deposited by electron beam evaporation and lift-off. Facets were formed by chemically assisted ion beam etch (CAIBE) in an Oxford ion mill and no facet coating is performed. The rib widths ranged from 2 to 5 μm, and the cavity length ranged from 600 to 1200 μm. The light–current–voltage (LIV) curve was taken under pulsed operation at room temperature, and the emission spectra was recorded using an optical fiber to couple light into a spectrometer (Ocean Optics).

Figure 5a,b shows LIV curve and emission spectrum of edge-emitting LD with 2.5 μm wide rib and 900 μm long cavity. The threshold current density (Jth) and threshold voltage (Vth) were 2.6 kA cm⁻² and 5.8 V, respectively, under pulsed operation with a temporal width of 500 ns and frequency of 10 kHz (duty cycle of 0.5%). The slope was 0.62 W A⁻¹ for both ends and output power of more than 300 mW is obtained at a current of 1000 mA from one end. The emission spectrum was measured at 200 mA (3.5 × Jth) and a lasing wavelength was 447 nm.

It should be noted that no heavily doped n-layer for n-contact is inserted and lower temperature n-contact anneal are performed compared with the previous 450 °C anneal. If heavy doping were done for the entire GaN cladding layer, carrier transport properties would deteriorate due to presence of a high concentration of Si dopants. Therefore, we have to insert very thin heavily doped n-layer, for instance, 20 nm. It would be, however, difficult to etch stop at the thin heavily doped n-layer due to spatial variation of etch depth. The other thing is that, in the heterogeneous integration, whatever the bonding is used, a CTE mismatch is always an issue. Higher temperature processing would adversely affect the device, for example, cracking or peeling off. For this reason, lower temperature during bonding and postprocessing steps is preferred, typically less than 300 °C from results for InP/Si platform. Table 2 shows linear CTEs of materials used

Figure 5a,b shows LIV curve and b) emission spectrum of edge-emitting LD with 2.5 μm wide rib and 900 μm long cavity. The threshold current density (Jth) and threshold voltage (Vth) were 2.6 kA cm⁻² and 5.8 V, respectively, under pulsed operation. The emission spectrum was measured at 200 mA (3.5 × Jth) and a lasing wavelength was 447 nm.
for heterogeneously integrated InGaN/TiO$_2$ and InP/Si LD. Note that linear CTE of GaN is in $c$-direction\(^a\),\(^b\) whereas CTE of TiO$_2$ is an average value for rutile TiO$_2$ in $a$- and $c$-direction. This data suggest that since a linear CTE of TiO$_2$ may be somewhat high, processing temperature of GaN after bonding should be less than 300 °C. Despite these two modifications from UCSB standard fabrication recipe, low threshold current density and threshold voltage are achieved.

3.3. GaN Substrate Removal

The sample structure to test GaN substrate removal consisted of 500 nm GaN, sacrificial three QW layer consisting of 3 nm In$_{0.12}$Ga$_{0.88}$N wells and 7 nm GaN barriers, 50 nm n-GaN, 15 nm n-$\alpha$-Al$_{0.3}$Ga$_{0.7}$N and 1 µm n-GaN. We planned to perform PEC undercut etch followed by PEC top-down etch to smoothen the etched surface. The n-$\alpha$-Al$_{0.3}$Ga$_{0.7}$N acts as an etch stop layer for PEC top-down etch, but we end up only performing PEC undercut etch here.

The PEC undercut etch of sacrificial MQW proceeds in a lateral direction, so that a whole substrate removal would be impractical. Therefore, rectangular mesas were formed by ICP etch to expose sacrificial MQW. A Ti/Au metal was deposited by electron beam evaporation and lift-off, leaving PEC cathode and pad on the mesa. Using a carrier wafer such as glass or sapphire, Ti/Au was deposited by electron beam evaporation, and In/Au was deposited by thermal evaporation. A flip-chip bonding of the GaN wafer with the carrier wafer using Au-In solid-liquid interdiffusion (SLID) bonding was performed at 200 °C using a graphite-bonding fixture. PEC undercut etch of sacrificial MQW was performed in a 1 m KOH solution with illumination of an LED array ($\lambda$ = 405 nm).

Figure 6a shows an optical micrograph of the GaN film bonded on carrier wafer, in this case, a glass. GaN substrate removal was successful, and 220 µm wide and 1200 µm long rectangular mesas were observed. Unfortunately, the etched surface was rough (arithmetic mean roughness $R_a$ = 6.17 nm for 2 × 2 µm scan of atomic force microscope [AFM]), impeding direct bonding. The etched surface roughness, however, should be reduced significantly by ice bath etch, $R_a < 1$ nm, as is reported recently.\(^c\) Also, subsequent top-down etch with an AlGaN etch stop layer would improve the surface morphology further.

InAu SLID bonding is used here to consider its resistance to harsh conditions of PEC etch such as soaking in strong base and ultraviolet (UV) light irradiation, but organic adhesive may be better for lower temperature bonding and detachment of carrier wafer as long as it is tolerant to PEC etch.

3.4. Direct Bonding

For direct bonding, either a semipolar GaN (202 $\bar{1}$) free standing wafer or a GaN epitaxial wafer was used. The GaN epitaxial wafer has the same epitaxial layer stacking structure as the one used for GaN substrate removal. A wet thermal oxidation of Si wafer was performed, forming 1 µm-thick thermal oxide. Both GaN wafers and Si with thermal oxide were activated by oxygen plasma (EVG 810). The pieces were then placed in contact, leading to a spontaneous bonding, followed by thermal annealing at 200–300 °C using a graphite-bonding fixture.

Direct bonding of GaN wafer with thermal oxide on Si is going well, but the GaN epitaxial wafers fail to bond even after multiple trials. A surface roughness of the GaN epitaxial wafer observed by AFM is very low, $R_a = 0.177$ nm, for 2 × 2 µm scan. This can meet the criterion of microroughness imposed by EVG, a supplier of bonding machine, to obtain excellent bonding results: $R_a < 0.5$ nm for 2 × 2 µm scan. But there are other EVG criteria such as total thickness variation (TTV) and bow. These figures, basically, stand for height variation that takes place in long distance as opposed to microroughness, namely, height fluctuation in short distance. Our speculation is that even though microroughness is low, longer-range height variation of the GaN epitaxial wafer would be large. Based on this consideration, wide AFM scans were performed. Figure 7a shows the scan size dependence of surface roughness $R_a$ for GaN wafer and GaN epitaxial wafer observed by AFM. It should be noted that wafer bowing is corrected to extract the microroughness. As we increase the scan size, the surface roughness of the GaN epitaxial wafer is evidently increased and exceeds 1 nm for 50 × 50 µm scan, whereas the surface roughness of GaN wafer is kept low. Indeed, there seems to be several micrometer-scale undulation along $c$-plane, as shown in Figure 7b. This may prevent direct bonding. The similar morphology and surface roughness have been observed for n-type GaN films grown on off-axis substrate from $m$-plane toward [0001] direction.\(^d\)

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\(^a\)Linear CTE of GaN in $c$-direction; \(^b\)Average linear CTE of rutile TiO$_2$.

| Material        | InGaN/TiO$_2$ CTE | InP/Sl CTE | CTE  |
|-----------------|-------------------|------------|------|
| GaN\(^{27}\)   | 2.6\(^c\)         | InP\(^{28}\) | 4.6  |
| TiO$_2$\(^{29}\) | 6.4\(^c\)         | Si\(^{30}\) | 2.618|
| SiO$_2$\(^{31}\) | 0.55              | SiO$_2$    | 0.55 |
| Si              | 2.618             | Si         | 2.618|

**Table 2.** A table of linear CTEs of materials used for heterogeneously integrated InGaN/TiO$_2$ LD and InP/Si LD.
Polishing might be necessary for direct bonding but only small amount of polishing is allowed or precise thickness control with tens nanometer-scale accuracy is needed for our device, making this approach challenging. In addition, thermal oxide on Si wafer is used in this work instead of TiO$_2$/thermal oxide/Si because thermal oxide should meet all the EVG criteria for bonding such as microroughness, bow, and TTV and ideal for a test bonding. But in reality, the surface roughness of TiO$_2$ would be another concern. In this regard, polymer-based adhesive bonding may be practical alternative because it is more tolerant to the roughness of bonding surface.\cite{34}

![Figure 7. a) Surface roughness $R_a$ for GaN wafer and GaN epitaxial wafer observed by AFM plotted against scan size. b) AFM image in 20 $\times$ 20 $\mu$m scan.](image)

4. Conclusions

A heterogeneously integrated InGaN/TiO$_2$ LD is proposed for GaN PIC on Si, wherein InGaN films are vertically stacked on a TiO$_2$ WG by bonding. Due to the high refractive index of TiO$_2$, comparable with GaN, the optical transverse mode extends to both the GaN and TiO$_2$ in a hybrid mode. Mode transfer between a hybrid InGaN/TiO$_2$ section and a pure TiO$_2$ WG can be achieved with an adiabatic taper structure. The coupling losses are calculated to be 0.14 dB and 0.42–0.43 dB for EME and FDTD solver, respectively, with fairly short taper length of 78 $\mu$m and tip width of 200 nm, which can be fabricated by a KrF excimer laser stepper. Four primary technologies including TiO$_2$ WG, edge-emitting InGaN LD with topside n-contact, GaN substrate removal, and bonding of GaN with Si need to be established for realizing heterogeneously integrated InGaN/TiO$_2$ LD. The former two are straightforward. Although it would be nontrivial task to fabricate low loss TiO$_2$ WG due to shorter wavelength, the WG loss would not be an issue at an early stage of development because the heterogeneous platform can engineer the modal profile and minimize the effect of propagation loss of TiO$_2$ WG if it is significant. Good performance of the semipolar GaN LD with topside n-contact such as low threshold current density and high output power have been demonstrated with modifications from the previous recipe to be compatible with the heterogeneous platform. The GaN substrate removal is successfully done by the PEC undercut etch. Although it is rough, the etched surface morphology would be improved by ice bath PEC etch. Furthermore, successful direct bonding of GaN wafer with thermal oxide on Si by plasma activation has been demonstrated. Altogether, we are now working toward the development of the heterogeneously integrated GaN/TiO$_2$ LD on Si.

**Acknowledgements**

The authors acknowledge the use of computational facilities purchased with funds from the National Science Foundation (CNS-1725797) and administered by the Center for Scientific Computing (CSC). CSC was supported by the California NanoSystems Institute and the Materials Research Science and Engineering Center (MRSEC, NSF DMR 1720256) at UC Santa Barbara. The authors thank Warren Jin for assistance with FDTD.

**Conflict of Interest**

The authors declare no conflict of interest.

**Keywords**

heterogeneous integration, InGaN, photonic integrated circuits, Si photonics

Received: September 18, 2019
Revised: November 18, 2019
Published online: December 29, 2019

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