Recovering single precision accuracy from Tensor Cores while surpassing the FP32 theoretical peak performance

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Abstract

Tensor Core is a mixed-precision matrix-matrix multiplication unit on NVIDIA GPUs with a theoretical peak performance of more than 300 TFlop/s on Ampere architectures. Tensor Cores were developed in response to the high demand of dense matrix multiplication from machine learning. However, many applications in scientific computing such as preconditioners for iterative solvers and low-precision Fourier transforms can exploit these Tensor Cores. To compute a matrix multiplication on Tensor Cores, we need to convert input matrices to half-precision, which results in loss of accuracy. To avoid this, we can keep the mantissa loss in the conversion using additional half-precision variables and use them for correcting the accuracy of matrix-matrix multiplication. Even with this correction, the use of Tensor Cores yields higher throughput compared to FP32 SIMT Cores. Nevertheless, the correcting capability of this method alone is limited, and the resulting accuracy cannot match that of a matrix multiplication on FP32 SIMT Cores. We address this problem and develop a high accuracy, high performance, and low power consumption matrix-matrix multiplication implementation using Tensor Cores, which exactly matches the accuracy of FP32 SIMT Cores while achieving superior throughput. The implementation is based on NVIDIA’s CUTLASS. We found that the key to achieving this accuracy is how to deal with the rounding inside Tensor Cores and underflow probability during the correction computation. Our implementation achieves 51TFlop/s for a limited exponent range using FP16 Tensor Cores and 33TFlop/s for full exponent range of FP32 using TF32 Tensor Cores on NVIDIA A100 GPUs, which outperforms the theoretical FP32 SIMT Core peak performance of 19.5TFlop/s.

Introduction

In order to meet the increasing demand of dense matrix-matrix multiplication from the machine learning community, processors with specialized computing units for matrix multiplication are being developed by numerous vendors. For instance, Google Tensor Processing Unit (TPU) \cite{15}, Intel Ponte Vecchio \cite{13}, IBM POWER10 \cite{12}, Preferred Networks MN-Core \cite{24} and NVIDIA GPUs, all have special arithmetic units for low-precision matrix-matrix multiplication. The NVIDIA Tensor Core is a mixed-precision matrix-matrix multiplication unit on NVIDIA GPUs and its theoretical peak performance is more than 300 TFlop/s on the latest Ampere architecture \cite{20}. Tensor Cores compute a matrix-matrix multiplication of two FP16 (IEEE 754 binary16) matrices in full-precision and accumulate in FP32 (IEEE 754 binary32). This results in higher accuracy in matrix-matrix multiplication compared to FP16 computing units. This capability to perform fast matrix multiplication can be used not only by machine learning applications, but also scientific computing applications and middleware that support both communities. Haidar \cite{11} uses Tensor
Cores within a mixed-precision iterative refinement solver in order to exploit the speed of Tensor Cores while recovering the accuracy through refinement. This method can be applied to recover full FP64 (IEEE binary64) accuracy and is currently used in MAGMA\(^1\) and NVIDIA’s cuSOLVER implementation.\(^2\) Tensor Cores can also be used for sparse matrix multiplication in graph analytics, breadth-first search, multigrid methods, etc \(^30\). Furthermore, Tensor Cores have also been used for reduction/scan operations in Monte Carlo methods, sort algorithms, etc \(^3, 5, 9\).

There have been several efforts to analyze the internal behavior of Tensor Cores. Jia et al. and Raihan et al. analyze how Tensor Core assembly instructions divide the input matrices, and the order they compute multiplications of the subdivided matrices \(^14, 25\). There have also been studies on how Tensor Cores support subnormal numbers and use RZ (Round toward Zero) \(^6\). Others have performed error analysis of Tensor Cores, where the theoretical error bound of mixed-precision block FMA computation is analyzed and compared to the actual error of Tensor Cores \(^1\). Studies on error correction have also been proposed. We have mentioned earlier that the conversion of input matrices to FP16 results in a loss of accuracy. To address this problem, Mukunoki et al. uses the Ozaki scheme \(^23\) on Tensor Cores \(^18\). Using this method, it is possible to achieve single precision or even double precision accuracy on Tensor Cores. This method is able to perform matrix-matrix multiplication in FP64 faster than the cuBLAS DGEMM on GPUs with limited FP64 support such as the NVIDIA GeForce series. However, this method is slower when it comes to FP32, and is much slower than the cuBLAS SGEMM on any GPU. This method is also not competitive for FP64 matrix multiplication when compared to cuBLAS DGEMM on NVIDIA Tesla series GPUs.

For single-precision matrix-matrix multiplication, Markidis et al. propose a method to improve the accuracy of Tensor Core computation by using auxiliary FP16 variables to account for the truncated bits \(^17\). Markidis’ method and its extensions are used for FFT \(^27\), QR Factorization \(^22\), and quantum-based molecular dynamics simulations \(^8\). However, the use of auxiliary FP16 variables alone is not sufficient to fully recover the FP32 accuracy. Feng et al. propose an improvement to Markidis’ method, which uses a better rounding mode during the truncation to FP16 \(^7\). However, they are still not able to match the accuracy of SGEMM with their error correction method. We consider that there might be some technical errors in their paper. First, they do not take into account the implicit bit in IEEE 754 floating-point numbers. For example, they claim that FP16 has 10 mantissa bits so two FP16 numbers have a total of 20 mantissa bits. However, with the implicit bit the total is actually \((10 + 1) × 2 − 1 = 21\) bits. This inaccurate description also causes some confusion during their description of the rounding they propose. Second, their method truncates a single-precision value \(x\) to a half-precision \(x_{hi}\) and stores the remaining value \(x − x_{hi}\) to \(x_{lo}\). They propose to decide the rounding of \(x_{hi}\) by looking at the 21st bit of mantissa of \(x\), but if we consider the implicit bit, they should be looking at the 22nd bit. Furthermore, \(x_{hi}\) will always store the first 10 bits when truncating, but \(x_{lo}\) does not always store the next 10 bits. This means that always looking at the same bit to decide the rounding of \(x_{hi}\) will not result in the round-split method they intend to perform. Therefore, their mantissa length analysis applied on Markidis’ method (Truncate-Split) and their method (Round-Split; EGEMM-TC) might be incorrect. In the end, Feng et al. are not able to achieve an accuracy that exactly matches SGEMM \(^7\).

Another important advantage of matrix-matrix multiplication unit is energy consumption. For instance, the top supercomputer listed (June 2021) in the Top500 –Fugaku–, requires 30MW of power to achieve 442 PFlop/s FP64 performance, and Exascale systems are predicted to consume even more power. If we look at the Green500 list, the top systems are equipped with matrix-matrix multiplication hardware such as MN-Core, and NVIDIA A100. This reflects the energy efficiency of matrix-matrix multiplication hardware. The power consumption of GPUs have been analyzed at the Parallel Thread Execution (PTX) level, middleware level, and application level. Sakamoto et al. measured the effect of low-precision computing

\(^1\)https://developer.nvidia.com/magma
\(^2\)cusolverIRSRefinement_t section of cuSOLVER Documentation https://docs.nvidia.com/cuda/cusolver/
on power consumption of the ICCG method in their earthquake simulation [26]. Guo et al. performed a CUDA PTX instruction level power analysis [10].

We envision that in the future a majority of applications will adopt mixed precision. In this scenario, there will be variables that will be computed in FP64, FP32, and FP16. For instance, the work by [4] uses three precisions during the iterative refinement and the LU is done in FP32, which calls an single-precision matrix-matrix multiplication. Furthermore, while the current quantum computer simulation using tensor network contraction uses single-precision matrix-matrix multiplication, it has been also investigated that which part of computing precision is sensitive to the result [16]. In recent year, the real machines of quantum computer have been developed and tried to be shown quantum supremacy, that they compute certain tasks that (classical) supercomputers are not be able to compute in realistic time. Moreover, since they have low power consumption [2], energy efficiency is becoming an important metric when evaluating quantum supremacy. For instance, qFlex is a quantum computer simulator based on tensor network contraction using single-precision complex matrix-matrix multiplication, where the power consumption of each component was reported during its simulation on Summit V100 GPUs [28]. Although they have considered to use FP16 and Tensor Cores in their simulation, they decided not to use it since FP16 has less exponent than FP32 and insufficient to use.

In this paper, we improve upon the existing error correction methods for matrix-multiplication on Tensor Cores by [17] and [7]. The two main causes of error in existing work are:

1. The rounding inside Tensor Cores is done with round-to-zero by default, which causes a large error even when accumulating in FP32.

2. The high probability of underflow and gradual underflow in the error correction computation.

We address these problems and evaluate against four other existing methods; Markidis’ method, Feng’s method, cuBLAS SGEMM using FP32 SIMT Core, and cuBLAS SGEMM over Tensor Cores. These results are shown in Figure 1. Although, we implemented the method described in Feng’s work, we were not able to reproduce the accuracy shown in the paper [7]. We also reduce the computational complexity compared to Markidis’s method and Feng’s method. Furthermore, we provide our SGEMM implementation using NVIDIA CUTLASS.\textsuperscript{3} We evaluate the performance of our method in Figure 2. Our method surpasses the FP32 theoretical peak performance, while achieving the same error as FP32.

Our contributions can be summarized as follows:

- We theoretically calculate the expectation of the mantissa length and experimentally evaluate the effect of this mantissa length. As a result, we find that the mantissa loss is not the main cause of error during matrix-matrix multiplication in Markidis’ method.

- We evaluate the effect of rounding inside Tensor Cores, and find that this is one of the main causes of error. We reduce the effect of these rounding errors by accumulating outside of the Tensor Cores, and improve the matrix multiplication accuracy to exactly match that of CUDA FP32 SIMT Cores.

- We also apply scaling to reduce the underflow probability. As a result, our method can deal with a wider range of values compared to Feng’s and Markidis’ method. Furthermore, we use the TF32 [20] data type, which is available on Ampere architectures, and confirm that it can represent nearly the entire FP32 exponent range.

- We remove one of the three error-correction terms, and reduce the amount of computation on Tensor Cores to 75% without loss of any accuracy.

\textsuperscript{3}https://github.com/enp1s0/cutlass
Figure 1: Accuracy comparison of matrix multiplication $A \times B$ of our method, Feng’s method[7], Markidis’ method[17], cuBLAS SGEMM using FP32 SIMT Cores, and cuBLAS SGEMM using Tensor Cores. Input matrices $A \in \mathbb{FP32}^{16 \times k}$ and $B \in \mathbb{FP32}^{k \times 16}$ are initialized with random numbers generated from a uniform distribution $(-1, 1)$. The error is calculated by Eq. (7).

- We include these modifications to NVIDIA CUTLASS and evaluate the matrix-matrix multiplication accuracy, computational throughput, and power consumption. Our implementation shows higher performance and lower power consumption compared to cuBLAS SGEMM on FP32 SIMT Cores while retaining the same accuracy.

**Background**

**Rounding**

The rounding of floating-point numbers is the key to understanding the present contribution, so we will first describe the different types of rounding. Let us consider a floating-point value with $\ell$ mantissa bits, and the cases where it is rounded to $n$ bits.

$$m = \underbrace{m_{\ell-1}m_{\ell-2}\cdots m_{\ell-n}}_{n \text{ bit}} \underbrace{m_{\ell-n-1} \cdots m_0}_{\ell \text{ bit}}$$

The different rounding modes described below are defined by a combination of two basic operations; rounding-up and rounding-down (truncation). Rounding-up adds 1 to $m_{\ell-1}m_{\ell-2}\cdots m_{\ell-n}$, while rounding-down does nothing to $m_{\ell-1}m_{\ell-2}\cdots m_{\ell-n}$. In this paper, we use three types of rounding modes:

**Round to Nearest; ties to even (RN)**

1) Truncate when $m_{\ell-n-1}$ equals 0.
2) When $m_{\ell-n-1}$ equals 1:
   a) Round-up when at least one of $m_{\ell-n-2}, \ldots, m_0$ is 1.
   b) Truncate or round up so that $m_{\ell-n}$ becomes 0 when all of $m_{\ell-n-2}, \ldots, m_0$ are 0 (Ties to even).
Figure 2: Performance comparison of our method in TF32 and FP16, cuBLAS SGEMM and the FP32 theoretical peak. Our methods compute the single-precision matrix-matrix multiplication with the same accuracy as cuBLAS SGEMM.

Round to Nearest; ties to Away from zero (RNA)
1) Truncate when \( m_{l-n-1} \) equals 0.
2) Round-up when \( m_{l-n-1} \) equals 1.

Round toward Zero (RZ)
Always truncate.

We show the number line representation of RN, RNA and RZ in Figure 3.

**Tensor Cores**

**Programming interface**

NVIDIA provides the WMMA API for using Tensor Cores in CUDA/C++. When using the WMMA API, the input matrices (in FP16) are copied to a register array called “Fragments” using a WMMA API function. A pseudocode for computing matrix-matrix multiplication \( C \leftarrow A \times B \) on Tensor Cores using WMMA API is shown in Code 1. In this pseudocode, we divide the input matrices into sub-matrices and compute matrix-matrix multiplications on them. The functions \texttt{fill\_fragment}, \texttt{load\_matrix\_sync}, \texttt{mma\_sync}, \texttt{mma\_sync} and \texttt{store\_matrix\_sync} in the pseudocode are part of the WMMA API. The flow of computation is as follows:

1. Initialize a fragment \( \text{frag\_c} \) for accumulating the resulting matrices using \texttt{fill\_fragment} function.
2. Load sub-matrices of \( A, B \) from memory to fragments \( \text{frag\_a}, \text{frag\_b} \) using the \texttt{load\_matrix\_sync} function.
3. Compute the matrix-matrix multiplication of \( \text{frag\_a}, \text{frag\_b} \) and accumulate to \( \text{frag\_c} \) using the \texttt{mma\_sync} function.
4. Store the sub-matrix of \( C \) from the fragment \( \text{frag\_c} \) to memory.
Figure 3: The roundings we use in this paper.

```
__device__ void matmul(mem_c, mem_a[K], mem_b[K]) {
  fragment frag_a, frag_b, frag_c;
  shared_mem_fp16 smem_a, smem_b;
  // 1: Initialize an accumulator fragment
  fill_fragment(frag_c, 0.f);
  for (k=0;k<K;k++) {
    // Convert subdivided matrix to FP16
    smem_a = toFP16(mem_a[k]);
    smem_b = toFP16(mem_b[k]);
    // 2: Load subdivided matrices to fragments
    load_matrix_sync(frag_a, smem_a, ...);
    load_matrix_sync(frag_b, smem_b, ...);
    // 3: Compute matrix–matrix multiplication
    // and accumulation on Tensor Cores
    mma_sync(frag_c, frag_a, frag_b, frag_c);
  }
  // 4: Store result to memory
  store_matrix_sync(mem_c, frag_c, ...);
}
```

Code 1: A simple matrix-matrix multiplication pseudocode on Tensor Cores using WMMA API.

**Fragment mapping and PTX Instructions**

The functions load_matrix_sync and store_matrix_sync, map the memory index of the input matrix elements to the fragment index. We can analyze this mapping and use it for reducing the memory footprint. Our wmma_extension library provides functions for that purpose. For instance, computing matrix-vector multiplication without unnecessary memory footprint, and loading/storing fragments with custom operations for each element.

There are two types of PTX instructions: wmma and mma. The wmma instructions provide finer control compared to the mma instruction, such as loading fragments using wmma.load, computing matrix-matrix multiplication accumulation using wmma.mma, and storing fragments using wmma.store. However, we chose to use the mma due to the more efficient register usage compared to wmma.

When we use wmma instructions, each element in matrices A and B is kept by two elements inside the
fragments on threads in a warp. On the other hand, for \texttt{mma} each element of the input matrices is kept by only one element of the fragments on threads in a warp without duplication. To use \texttt{mma}, we need to map the memory and the fragment manually since the load and store instructions for \texttt{mma} do not exist. This map for \texttt{mma} is available in the NVIDIA Toolkit Documentation\textsuperscript{4}.

**Single-precision matrix-matrix multiplication using error correction technique on Tensor Cores**

As we mentioned previously, in order to use Tensor Cores for single-precision matrix-matrix multiplication we need to convert the input matrices to FP16 which introduces a truncation error. Markidis et al. propose a method to correct this truncation error by keeping the mantissa loss in additional FP16 variables and using them for correcting the accuracy of matrix-matrix multiplication [17].

\[
\begin{align*}
\mathbf{A}_{F16} & \leftarrow \text{toFP16}(\mathbf{A}_{F32}) \\
\Delta \mathbf{A}_{F16} & \leftarrow \text{toFP16}(\mathbf{A}_{F32} - \text{toFP32}(\mathbf{A}_{F16})) \\
\mathbf{B}_{F16} & \leftarrow \text{toFP16}(\mathbf{B}_{F32}) \\
\Delta \mathbf{B}_{F16} & \leftarrow \text{toFP16}(\mathbf{B}_{F32} - \text{toFP32}(\mathbf{B}_{F16})) \\
\hat{\mathbf{C}}_{F32} & \leftarrow \mathbf{A}_{F16}\mathbf{B}_{F16} + \Delta \mathbf{A}_{F16}\mathbf{B}_{F16} + \Delta \mathbf{A}_{F16}\Delta \mathbf{B}_{F16}
\end{align*}
\]

\texttt{Code 2: A simple pseudocode example of Markidis’ error correction method}

\textsuperscript{4}Warp Level Matrix Multiply-Accumulate Instructions section in PTX ISA Chapter \url{https://docs.nvidia.com/cuda/parallel-thread-execution/}
We show the accuracy of Markidis’ method in Figure 1. To evaluate the accuracy, we compute the relative residual using the following equation.

\[
\text{RelativeResidual} = \frac{||C_{FP64} - C_{Target}||_F}{||C_{FP64}||_F},
\]

where the \( || \cdot ||_F \) is the Frobenius norm. We compute the reference matrix-matrix multiplication \( C_{FP64} = \text{toFP64}(A_{FP32}) \cdot \text{toFP64}(B_{FP32}) \) in FP64.

From Figure 1 we see that, Markidis’ method is more accurate than the Tensor Core without error correction for smaller matrix sizes. However, we found that RZ rounding inside Tensor Cores accumulates errors faster than the RN of FP32 SIMT Cores, and the accuracy catches up to the Tensor Core as the matrix size becomes larger. Feng et al. propose to reduce the mantissa loss in Eqs. (3) and (5) by using the sign bit as an extra mantissa bit [7]. However, our experiments could not show any advantage by faithfully reproducing what is described in their paper.

Error investigation and improvements

Expectation of mantissa length

We can write Eqs. (2) and (3) and Eqs. (4) and (5) for each element as

\[
v_{F16} \leftarrow \text{toFP16}(v_{F32}) \quad \text{(8)}
\]

\[
\Delta v_{F16} \leftarrow \text{toFP16}(v_{F32} - \text{toFP32}(v_{F16})) \quad \text{(9)}
\]

The input element \( v_{F32} \) is approximated by \( v_{F16} + \Delta v_{F16} \). The mantissa length of FP32 is 23 + 1 = 24 bit, including an implicit 1 bit, and the FP16 is 10 + 1 = 11 bit. Thus \( v_{F16} + \Delta v_{F16} \) cannot represent the full mantissa of \( v_{F32} \). In this section, we calculate the expectation of the mantissa length kept by Eqs. (8) and (9).

We express the mantissa bit of \( v_{F32} \) as \( m_{22}m_{21} \cdots m_0 \) from MSB without the implicit 1 bit, and the rounding during the conversion to FP16 is RN, which is the default in CUDA. In this case, \( m_{13} \cdots m_0 \) bits decide whether we round-up in Eq. (8). We show the mantissa length kept by Eqs. (8) and (9) and its probability of occurrence in the case of \( m_{13} \cdots m_0 \) in Table 1. This probability is calculated under Assumption 1 for the mantissa part of floating-point numbers as follows.

**Assumption 1** Each bit of the mantissa is 1 with probability \( \frac{1}{2} \), and each bit is statistically independent

It follows that the expectation of the mantissa length is 22.75 bits out of the FP32 mantissa length of 23 bits. Furthermore, when we use RNA for rounding during the FP16 conversion in Eqs. (8) and (9), the values of \( v_{F16} \) and \( \Delta v_{F16} \) are different from RN. However, the mantissa length and its probability of occurrence are the same as RN, and the expectation of mantissa length is 22.75 bits.

To evaluate the effect of this 22.75 bits of mantissa, we evaluate the accuracy of FP32 matrix-matrix multiplication by truncating the Least Significant Bit (LSB) of the mantissa of input matrices. The expectation of the mantissa length during this operation is 22.5 bits under Assumption 1, which is shorter than 22.75 bits. We show the accuracy comparison between this truncation and Markidis’ method in Figure 4, and see that the accuracy of Markidis’ method is worse than this method despite the higher expectation of mantissa length. In conclusion, the mantissa loss is not the main cause of error during matrix-matrix multiplication on Tensor Cores.

Although the mantissa length of FP16 is 10 + 1 = 11 bits and two FP16s can keep only 22 bits of mantissa per 23 + 1 = 24 bits of FP32 mantissa, the expectation of the mantissa length is 22.75 + 1 = 23.75 bits. The reason for this can be explained as follows:
When the last $n$ bits of mantissa are 0, the mantissa length to keep is $23 + 1 - n$ bits per 24 bits. We can keep the full mantissa when $n \geq 2$.

When $l_0$ is greater than or equal to 2, the mantissa length kept by $\Delta v_{\text{F16}}$ is less than or equal to 10. Therefore, we can keep the full mantissa.

Rounding-up can be performed during the conversion in Eq. (8) when $l_0 = 0$. It keeps more mantissa compared to RZ. It follows that $|v_{\text{FP16}}| < |v_{\text{FP32}}|$ when rounding-up. And the signs of $\Delta v_{\text{F16}}$ and $v_{\text{FP32}}$ are different because $v_{\text{FP16}}$ and $v_{\text{FP32}}$ have the same sign. Let us consider the following example.

The mantissa of $v_{\text{FP32}}$ is represented by a $23 + 1 = 24$ bit integer shown in Eq. (10).

$$I_{\text{FP32}} = + \begin{array}{llllll}
10000000000' & 0000000000' & 11
\end{array}$$  \hspace{3cm} (10)

| $l_0$ | $m_{13}$ | $m_{12}$ | $m_{11}$ | $m_1$ | $m_0$ | len | prob |
|-------|---------|---------|---------|-------|-------|------|------|
| $\geq 2$ | * | 0 | 0 | * | * | 23 | 1/4 |
| $= 1$ | * | 0 | 1 | * | 0 | 23 | 1/8 |
| * | 0 | 1 | * | 1 | 22 | 1/8 |
| $= 0$ | * | 1 | 0 | * | 0 | 23 | 1/8 |
| * | 1 | 1 | * | * | 23 | 1/4 |

Table 1: The mantissa length kept by $v_{\text{F16}}$ and $\Delta v_{\text{F16}}$ (len), the probability of occurrence (prob) when RN is performed during the FP16 conversion in Eqs. (8) and (9). $m_{22}m_{21} \cdots m_0$ represents the 23 bits of FP32 mantissa, and the probability is calculated under Assumption 1. The length $l_0$ is the number of consecutive zeros from $m_{12}$ towards the LSB. The mark "*" means it does not matter if it is 0 or 1.
\begin{table}[h]
\centering
\begin{tabular}{ccccccc}
\hline
$l_0$ & $m_{13}$ & $m_{12}$ & $m_{11}$ & $m_1$ & $m_0$ & len & prob \\
\hline
\geq 3 & * & 0 & 0 & * & * & 23 & 1/4 \\
= 2 & * & 0 & 1 & * & 0 & 23 & 1/8 \\
& * & 0 & 1 & * & 1 & 22 & 1/8 \\
= 1 & * & 1 & * & 0 & 1 & 22 & 1/8 \\
& * & 1 & * & 0 & 0 & 23 & 1/8 \\
\hline
\end{tabular}
\caption{The mantissa length kept by $v_{F16}$ and $\Delta v_{F16}$ (len), the probability of occurrence (prob) when RZ is performed during the FP16 conversion in Eqs. (8) and (9). $m_{22}m_{21}\cdots m_0$ represents the 23 bits of FP32 mantissa, and the probability is calculated under Assumption 1. $l_0$ is the number of consecutive zeros from $m_{12}$ toward LSB. The mark "*" means it does not matter if it is 0 or 1.}
\end{table}

The $I_{FP32}$ is kept by two $10 + 1 = 11$ bit integers $I_{FP16}$ and $\Delta I_{FP16}$ using RZ.

\[
I_{FP16} = + \underbrace{10000000000}_{11\text{bit}}'
\]
\[
\Delta I_{FP16} = + \underbrace{10000000000}_{11\text{bit}}'
\]
\[
Loss = + \underbrace{11}_{2\text{bit}}
\]

In this case, 2 bits of mantissa loss occurs. On the other hand, when we use RN instead of RZ, only 1 bit of mantissa loss occurs.

\[
I_{FP16} = + \underbrace{10000000001}_{11\text{bit}}'
\]
\[
\Delta I_{FP16} = - \underbrace{0111111111}_{11\text{bit}}'0
\]
\[
Loss = + \underbrace{1}_{1\text{bit}}
\]

This is because we need fewer bits to keep $n$ bits of an integer $a$ when $a > 2^{n-1}$, if we keep $2^n - a$ instead of $a$.

We also calculate the expectation of the mantissa length when we use RZ in Eqs. (8) and (9). We show the mantissa length and its probability of occurrence in Table 2. The expectation of the mantissa length is 22.25 bits.

**Avoiding RZ during Tensor Core accumulation**

The accumulator inside Tensor Cores has at least 2 extra bits of mantissa and RZ is used for rounding [6]. It follows that RZ is performed in the accumulator `frag.c` in every $k$ iteration in Code 2. We evaluate the effect of this RZ for the matrix-matrix multiplication using Markidis’ method using the mixed-precision matrix-matrix multiplication function `mmarn` and `mma_rz` that perform similar operations with Tensor Cores. Both functions compute the matrix-matrix multiplication as follows

\[
D_{F32} \leftarrow A_{F16} \times B_{F16} + C_{F32}.
\]
The multiplication of each element is computed in FP32 and accumulation in FP64. We truncate the mantissa of the accumulator to keep them in 25 bit after every element accumulation. The difference between these two functions is that the mma_rn performs RN for rounding after the addition of C_{F32} in Eq. (11), while the mma_rz performs RZ in the same way as Tensor Cores do.

We use mma_rz and mma_rn, instead of Tensor Cores, to compute a single-precision matrix-matrix multiplication using Markidis’ method and evaluate the accuracy. The results are shown in Figure 5. While the accuracy using mma_rn is the same as FP32 SIMT Core, the one using mma_rz is the same as Markidis’ method. Therefore, we conclude that performing RZ in the accumulator after addition to C_{F32} in Eq. (11) causes the accuracy loss in Markidis’ method.

To avoid the RZ and improve the accuracy, we compute the addition to C_{F32} in Eq. (11) outside of the Tensor Cores. We show the flow of our proposed method, and compare it against the standard process presented in Figure 6. We input a zero matrix to the Tensor Cores and compute the addition shown in Eq. (11) outside of the Tensor Cores using FP32 SIMT Cores which performs RN for rounding. By using this technique, the accuracy of the single-precision matrix-matrix multiplication using Markidis’ method improves to the same accuracy as FP32 SIMT Cores, as shown in Figure 1. On the other hand, this technique requires more registers to keep a zero matrix, additional process for making the zero matrix, and extra addition operations on FP32 SIMT Cores compared to Markidis’ method.

Reducing the underflow and gradual underflow probability in Δv_{F16} computations

The probabilities of underflow and gradual underflow in subtracting two values are high when their absolute values are close. This is shown in Eq. (9). We calculate the probabilities for each exponent value of v_{F32} and improve Eq. (9) to reduce the underflow. To calculate these probabilities, we first define some constant values, the exponent bias of FP16 b_{F16} = 15, and the mantissa length of FP16 l_{F16} = 10 and FP32 l_{F32} = 23. To simplify the calculation, we assume that RZ is used in toFP16 in Eqs. (8) and (9) while RN is used otherwise. Under this assumption, the first 10 bits of the mantissa of v_{F32} are kept by v_{F16}, and the 10 bits from (l_{F16} + l_0)th bit are kept by Δv_{F16} shown in Figure 7. Therefore, the exponent value of Δv_{F16} is smaller than the v_{F32} by l_0 + l_{F16} + 1, the last 1 is the length of the implicit bit of the mantissa. We
Figure 6: The flow of computation to avoid RZ inside Tensor Cores, which affects the accuracy of Markidis’ error correction method. **Left:** Standard usage of Tensor Cores via WMMA API. In this case, RZ is performed on the accumulator $C_{FP32}$ directly. **Right:** Our method for avoiding the RZ. We accumulate the result of the matrix-matrix multiplication $A_{F16} \times B_{F16}$ to $C_{F32}$ outside of Tensor Cores using FP32 SIMT Cores.

calculate the probabilities using this fact into consideration. We also define the exponent value of $v_{F32}$ as $e_v$ including exponent bias, where $v_{F32}$ is represented as follows,

$$v_{F32} = 1.m_{22}m_{21} \cdots m_0 \times 2^{e_v}$$  \hspace{1cm} (12)

First, we calculate $P_{u+gu}(e_v)$, the probability at which gradual underflow occurs. When normalized, the smallest number that can be expressed in FP16 is $2^{-b_{F16}+1}$. Therefore, the condition for underflow or gradual underflow in Eq. (9) can be represented as

$$e_v - (l_0 + l_{F16} + 1) < -b_{F16} + 1$$

$$\Rightarrow e_v - l_{F16} + b_{F16} - 2 < l_0.$$  \hspace{1cm} (13)

We define the probability $P(l_0 = n)$ such that $l_0$ equals to $n$ under the assumption 1 as

$$P(l_0 = n) = \begin{cases} 
0 & (n < 0) \\
\left(\frac{1}{2}\right)^{n+1} & (0 \leq n < l_{F32} - l_{F16}) \\
\left(\frac{1}{2}\right)^{l_{F32} - l_{F16}} & (n = l_{F32} - l_{F16}) 
\end{cases}$$  \hspace{1cm} (14)
Then, by using $P(l_0 = n)$, we calculate the desired probability $P_{u+gu}(e_v)$ as

$$P_{u+gu}(e_v) = \sum_{l = (e_v - l_{F16} + b_{F16} - 2)+1}^{l_{F32} - l_{F16}} P(l_0 = l).$$  \hspace{1cm} (15)$$

Next, we calculate $P_u(e_v)$, the probability where only underflow occurs. Without normalization, the smallest number that can be expressed by FP16 is $2^{-(b_{F16} + l_{F16})+1}$. Therefore, the condition at which underflow occurs can be expressed as

$$e_v - (l_0 + l_{F16} + 1) < -(b_{F16} + l_{F16}) + 1$$
$$\Rightarrow e_v + b_{F16} - 2 < l_0$$  \hspace{1cm} (16)$$

Using $P(l_0 = n)$ in the same way as $P_{u+gu}(e_v)$, we can calculate the desired probability $P_u(e_v)$ as

$$P_u(e_v) = \sum_{l = (e_v + b_{F16} - 2)+1}^{l_{F32} - l_{F16}} P(l_0 = l).$$  \hspace{1cm} (17)$$

In Figure 8, we show the theoretical $P_{u+gu}(e_v)$ and $P_u(e_v)$ calculated by Eq. (15) and Eq. (17) respectively, along with the experimental values aggregated on GPUs. We find that gradual underflow occurs in Eq. (9) even if $v_{F32}$ is around $10^6$.

To reduce these probabilities, we add $l_{F16} + 1 = 11$ to the exponent of the result of subtraction in Eq. (9) by multiplying $2^{11}$,

$$\Delta v_{F16} \leftarrow \text{toFP16} \left( (v_{F32} - \text{toFP32}(v_{F16})) \times 2^{11} \right)$$  \hspace{1cm} (18)$$

This process does not affect the mantissa. In this paper, we refer to the method that keeps $v_{F32}$ in Eqs. (8) and (18) as halfhalf, and the method in Eqs. (8) and (9) as Markidis’ halfhalf. The single-precision
matrix-matrix multiplication using halfhalf can be written as

\[
\begin{align*}
A_{F16} & \leftarrow \text{toFP16}(A_{F32}) \\
\Delta A_{F16} & \leftarrow \text{toFP16}((A_{F32} - \text{toFP32}(A_{F16})) \times 2^{11}) \\
B_{F16} & \leftarrow \text{toFP16}(B_{F32}) \\
\Delta B_{F16} & \leftarrow \text{toFP16}((B_{F32} - \text{toFP32}(B_{F16})) \times 2^{11}) \\
\hat{C}_{F32} & \leftarrow A_{F16}B_{F16} \\
& \quad + (\Delta A_{F16}B_{F16} + A_{F16}\Delta B_{F16})/2^{11} \\
& \quad + (\Delta A_{F16}\Delta B_{F16})/2^{22}
\end{align*}
\]

CUDA provides a data type called TF32 (Tensor Float) which has 8 bits of exponent and 10 bits of mantissa as the input type of Tensor Cores in Ampere architectures. Because the exponent length is the same as FP32, we can keep a wider exponent range compared to FP16. We use the TF32 instead of FP16 in Eqs. (8) and (9) and we refer to this method as \texttt{tf32tf32}. Currently, we can use RNA and RZ for rounding when converting FP32 to TF32. We use RNA because it keeps more mantissa compared to RZ, as we have shown in the Section Expectation of mantissa length. We show the comparison of representation accuracy and exponent range in Figure 9.

Removing negligible error correction

The absolute value of each element in \(\Delta^{(2)} = \Delta A_{F16}\Delta B_{F16}\) is at least \(2^{22}\) times smaller than \(\Delta^{(0)} = A_{F16}B_{F16}\). When two floating-point values are added, the mantissa of the value with the smaller exponent is shifted to align the exponent of the two values. Therefore, when computing \(\Delta^{(0)} + \Delta^{(2)}\), the shifting size is at least 22 bits in each element. This means that each \(\Delta^{(2)}\) element at most affects the mantissa LSB in each \(\Delta^{(0)}\) element since the mantissa length of FP32 is 23 bit and the correction capability is negligible.
Thus, we ignore this term and replace Eq. (23) with Eq. (24).

\[
\hat{C}_{\text{F32}} \leftarrow A_{\text{F16}}B_{\text{F16}} + (\Delta A_{\text{F16}}B_{\text{F16}} + A_{\text{F16}}\Delta B_{\text{F16}}) / 2^{11}
\]

Eq. (24) reduces the computation on Tensor Cores by 3/4.

**Incorporating our method into CUTLASS**

NVIDIA CUTLASS\(^5\) is an open-source CUDA C++ matrix-matrix multiplication template library that has hierarchical memory blocking strategies and computing primitives. We use CUTLASS version 2.5 as a base implementation and include our techniques for: avoiding RZ after the addition of \(C_{\text{F32}}\) in Eq. (11), reducing the underflow and gradual underflow probabilities, while ignoring negligible correction terms. We develop two types of implementations: \texttt{cutlass\_halfhalf} and \texttt{cutlass\_tf32tf32}. We use the \texttt{mma.sync.aligned.m16n8k8} PTX instruction, which computes matmul-(16, 8, 8) and addition using FP16 Tensor Cores. We call this implementation \texttt{cutlass\_halfhalf}. For using TF32 Tensor Cores, we use a PTX instruction which computes the same size of matrix-matrix multiplication and addition as the FP16 and we call this implementation \texttt{cutlass\_tf32tf32}. We only add the code for the error correction and use the original CUTLASS code for other parts of the computation, such as loading matrix data from global memory to shared memory. Therefore, our implementation can compute any matrix-matrix multiplication size as long as CUTLASS supports it.

The avoiding of RZ is only applied to \(A_{\text{F16}}B_{\text{F16}}\) in Eq. (24) and it is not applied to \(\Delta A_{\text{F16}}B_{\text{F16}} + A_{\text{F16}}\Delta B_{\text{F16}}\). This allows us to reduce the required registers and computations. We show an example using FP16 Tensor Cores in Code 3. Furthermore, we show a simple example of a single-precision matrix-matrix multiplication using Markidis’ and our methods. In this figure, we process \(A_{\text{FP32}}^{(0)} A_{\text{FP32}}^{(1)} B_{\text{FP32}}^{(0)} B_{\text{FP32}}^{(1)}\) using FP16 Tensor Cores.

---

1. void matmul (...) {
2.    fragment frag_a, frag_b, frag_c;

\(^5\)https://github.com/NVIDIA/cutlass
Figure 10: The comparison of Markidis’ method (top) and our method (bottom) to carry out single-precision matrix-matrix multiplication $A^{(0)}_{FP32} A^{(1)}_{FP32}$ $B^{(0)}_{FP32} B^{(1)}_{FP32}$. The matrices $A_{FP16}^{(·)}$, $\Delta A_{FP16}^{(·)}$, $B_{FP16}^{(·)}$, $\Delta B_{FP16}^{(·)}$ in Markidis’ method are calculated by Eqs. (2)-(5), and in our method by Eqs. (19)-(22).
fragment frag_da, frag_db, frag_dc;
fragment frag_tmp;
shared_mem_fp16 smem_a, smem_b;
shared_mem_fp16 smem_da, smem_db;

// Initialize accumulator fragments
fill_fragment(frag_c, 0.f);
fill_fragment(frag_dc, 0.f);
for (k=0; k<K; k++) {
  // Compute eq (19), (21)
  smem_a=toFP16(mem_a[k])
  smem_b=toFP16(mem_b[k])
  load_matrix_sync(frag_a, smem_a);
  load_matrix_sync(frag_b, smem_b);
  // Compute eq (20), (22)
  smem_da=toFP16((mem_a[k]−toFP32(smem_a)*2048)
  smem_db=toFP16((mem_b[k]−toFP32(smem_b)*2048)
  load_matrix_sync(frag_da, smem_da);
  load_matrix_sync(frag_db, smem_db);
  // Compute a part of eq (24)
  mma_sync(frag_da, frag_db, frag_da, frag_db);
  // Initialize a temporal accumulator fragment
  fill_fragment(frag_tmp, 0.f);
  mma_sync(frag_tmp, frag_a, frag_b, frag_tmp);
  for (i=0; i<frag_c.num_elements; i++) {
    // Accumulation using FP32 SIMT Core
    frag_c.x[i] += frag_tmp.x[i];
  }
  // Compute a part of eq (24)
  for (i=0; i<frag_c.num_elements; i++) {
    frag_c.x[i] += frag_dc.x[i]/2048;
  }
  // Store result to memory
  store_matrix_sync(mem_c, frag_c);
}

Code 3: Pseudocode including our improvements for computing single-precision matrix-matrix multiplication with error correction using FP16 Tensor Cores.

In our actual implementation, which is more complex than the simple example shown in Code 3, we don’t store $A_{F16}, B_{F16}$ and $\Delta A_{F16}, \Delta B_{F16}$ explicitly to the shared memory in order to reduce the memory footprint. Instead, we load $A_{F32}, B_{F32}$ from the shared memory, compute Eq. (19)-(22) on the registers, and store them to the fragments directly.

Parameter tuning of CUTLASS

The CUTLASS library has some template parameters to determine the blocking size of each memory layer, the number of software pipeline stages, etc. We searched the parameters for achieving the highest throughput for each input matrix size using a grid search. We used Weights&Biases’ sweeps for searching the optimal parameters efficiently. We show the parameter search space in Table 3. The total number of all parameter combinations is 3,456 and we filter them with the following set of rules.

- At least, one of $w_m > b_m$, $w_n > b_n$, and $w_k > b_k$ is satisfied. This is because the size of thread-block level blocking must be larger than the warp level.

6https://wandb.ai/site
Parameter Values Description

| Parameter | Values                  | Description                                      |
|-----------|-------------------------|--------------------------------------------------|
| bm, bn, bk| 16, 32, 64, 128, for respectively | The size of thread block level blocking. Each thread block computes matmul-(bm, bn, bk). |
| wm, wn, wk| 16, 32, 64, 128, for respectively | The size of warp level blocking. Each warp computes matmul-(wm, wn, wk). |
| stages    | 3, 4                    | The number of software pipelines.                |

Table 3: The parameter space for grid search when optimizing the computing performance of CUTLASS.

| Implementation | TensorCore | Error Correction |
|----------------|------------|------------------|
| cutlass_tf32tf32 | TF32-TC    | YES              |
| cutlass_fp16fp16  | FP16-TC    | YES              |
| cublas_tf32tc     | TF32-TC    | NO               |
| cublas_fp16tc     | FP16-TC    | NO               |
| cublas_simt(FP32) | Not used   | NO               |

Table 4: The list of implementations we use to evaluate our proposed methods. The implementations named cutlass_XX are our implementation, and cublas_XX are reference implementations.

- The size of the shared memory required exceeds its capacity.
- The error calculated by Eq. (7) is larger than the threshold (even if the compilation is successful). At this point, we set 0.1 as the threshold and we checked experimentally that this value holds for all cases.

Through this automatic filtering process, we were able to reduce the number of parameter combinations for cutlass_halfhalf to 202, and for cutlass_tf32tf to 200.

**Experiment details**

We compare the accuracy, throughput, and power consumption of our implementations. The list of implementations we used are summarized in Table 4.

**Accuracy evaluation**

We input single-precision matrices for each implementation and calculate the error following Eq. (7). We compute matrix-matrix multiplication 8 times with different random seeds and average the error of each of them. The order of addition is changed by the template parameters of CUTLASS, which slightly affects the error. We use the worst values in the grid search as the error. We use NVIDIA A100 40GB SXM4 and CUDA version 11.3.

In this section, we evaluate the effect of the exponent range and its pattern.

**Effect of the exponent range of input matrices**

As we mentioned in the previous section, the exponent range of halfhalf is narrower than FP32 as shown in Figure 9. To evaluate this effect on the matrix-matrix multiplication accuracy, we input the matrices with
Figure 11: The effect of the exponent range on the accuracy of matrix-matrix multiplication $A_F \times B_F$.

**Type 1**: All elements in both $A_F$ and $B_F$ are represented with high precision in halfhalf.

**Type 2**: All elements in either $A_F$ or $B_F$ are represented with high precision, while the others are lower precision for smaller values in halfhalf.

**Type 3**: All elements of both $A_F$ and $B_F$ are lower precision for smaller values in halfhalf.

**Type 4**: At least one of $A_F$ or $B_F$ is all zero in halfhalf because they are out-of-range.

Various exponent ranges and evaluate the accuracy. We define a single-precision matrix set $\text{exp Rand}(a, b)$ ($a, b \in \mathbb{Z}$) so that the exponent of each element of a matrix in it is generated from a uniform distribution $[a, b]$ and the mantissa is generated from a uniform distribution $[0, 2^{23} - 1]$.

$$
e \leftarrow \text{UniformRandInt}[a, b]$$

$$m \leftarrow \text{UniformRandFP32}[1, 2]$$

$$s \leftarrow \text{UniformRandInt}[0, 1]$$

$$(i, j)\text{-element} \leftarrow (2s - 1) \times 2^e \times m \quad (25)$$

In this evaluation, we use three types of input matrices as follows:

**exp Rand(−15, 14)**

All elements are in range of $(10^{-5}, 10^5)$, and represented by our halfhalf with high precision as shown in Figure 9.

**exp Rand(−35, −15)**

All elements are in range of $(10^{-11}, 10^{-4})$, and represented by our halfhalf with lower precision for smaller values as shown in Figure 9.

**exp Rand(−100, −35)**

All elements are in range of $(10^{-31}, 10^{-10})$. The halfhalf can’t represent this range of numbers.

We initialize the input matrices $A_{FP}$ and $B_{FP}$ with the above three patterns, respectively, and compute the matrix-matrix multiplication $A_{FP}B_{FP}$. We show the accuracy for the following combinations:

**Type 1**

Both $A_{FP}$ and $B_{FP}$ are $\text{exp Rand}(-15, 14)$.

**Type 2**

One of $A_{FP}$ or $B_{FP}$ is $\text{exp Rand}(-15, 14)$ and the other one is $\text{exp Rand}(-100, -35)$.

**Type 3**

Both $A_{FP}$ and $B_{FP}$ are $\text{exp Rand}(-35, -15)$. 

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Figure 12: Visualization of the exponent pattern of the input matrices $A_{FP32}$, $B_{FP32}$. We use randtlr, spatial, cauchy as $B_{FP32}$, and urand(0,1), exp_rand(-15, 0) as $A_{FP32}$.

Type 4

At least one of $A_{FP32}$ or $B_{FP32}$ is $\text{exp\_rand}(-100, -35)$.

The outcome of this experiment is shown in Figure 11. We can see that cutlass_tf32tf32 computes matrix-matrix accuracy with the same accuracy as FP32 SIMT in all cases. On the other hand, although cutlass_halfhalf computes in the same accuracy with FP32 SIMT in case Type 1, the loss of accuracy occurs in Type 2 and 3, and cutlass_halfhalf is not able to perform in case Type 4. Therefore, if all elements in the matrix have very small exponents, we need to carry out additional scaling before matrix-matrix multiplication is performed.

Effect of exponent patterns of the input matrices

In real-world computations, matrices have various exponent patterns. STARS-H\textsuperscript{7} was originally developed for the evaluation of hierarchical low-rank approximation methods, and covers various dense matrix patterns in real applications. We generate three types of input matrix $A_{F32}$ using STARS-H as follows:

\textsuperscript{7}https://github.com/ecrc/stars-h
**Accuracy**

- **High**
- **Low**

**Implementaiton**
- `cutlass_halfhalf`
- `cutlass_tf32tf32`
- `cublas_simt`
- `cublas_fp16tc`
- `cublas_tf32tc`

**Performance**

| Implementation | Accuracy | Performance [TFlop/s] |
|----------------|----------|----------------------|
| `cutlass_halfhalf` | **High** | A100: 150, RTX A6000: 120, GeForce RTX 3090: 90 |
| `cutlass_tf32tf32` | **Low**  | A100: 20, RTX A6000: 15, GeForce RTX 3090: 10 |
| `cublas_simt` | **High** | A100: 120, RTX A6000: 90, GeForce RTX 3090: 60 |
| `cublas_fp16tc` | **Low**  | A100: 20, RTX A6000: 15, GeForce RTX 3090: 10 |
| `cublas_tf32tc` | **Low**  | A100: 20, RTX A6000: 15, GeForce RTX 3090: 10 |

**Randtlr**

Random synthetic TLR (Tile Low-Rank) matrix.

**Spatial**

Exponential kernel for spatial statistics.

**Cauchy**

Cauchy matrix.

And as input matrix $B_{F32}$, we use two types of input matrix as follows:

**Urand** $(-1, 1)$

Random matrix from a uniform distribution (-1, 1).

**Exp Rand** $(-15, 0)$

Random matrix generated by Eq. (25).

We show a sample of exponent patterns of these matrices in Figure 12 and the accuracy of matrix-matrix multiplication $A_{F32}B_{F16}$ in Figure 13.

Although the accuracy of `cutlass_halfhalf` and `cutlass_tf32tf32` are better than `cublas_simt` in some matrix sizes, this likely due to the order of addition, and not because of our error correction method. Thus, we conclude that the accuracy of `cutlass_halfhalf` and `cutlass_tf32tf32` are the same as cuBLAS SGEMM, for various patterns of exponent values in the matrix.

**Performance evaluation**

We calculate the Flop/s for matmul-($m, m, m$) by dividing $2m^3$ with the computing time $s$ [sec]. The performance on NVIDIA A100, RTX A6000, and GeForce RTX 3090 is shown in Figure 14. The specifications of the host machine: for each GPU are:
|                | FP16-TC [TFlop/s] | TF32-TC [TFlop/s] | FP32 [TFlop/s] |
|----------------|-------------------|------------------|--------------|
| A100           | 312               | 156              | 19.5         |
| RTX A6000      | 309.6             | 154.8            | 38.7         |
| RTX 3090       | 142               | 71               | 35.58        |

|                | Bandwidth [GB/s] | L1 Cache [KB/SM] | L2 Cache [MB] |
|----------------|------------------|------------------|--------------|
| A100           | 1555             | 164              | 40           |
| RTX A6000      | 768              | 128              | 6            |
| RTX 3090       | 932              | 128              | 6            |

Table 5: The GPU specifications used in our evaluation [21, 20, 19].

NVIDIA A100 (40GB, SXM4)
AMD EPYC 7742, 1 TB of DDR4 Memory (3200 MT/s)

NVIDIA RTX A6000
AMD EPYC 7302, 256 GB of DDR4 Memory (3200 MT/s)

NVIDIA GeForce RTX 3090
AMD EPYC 7402, 512 GB of DDR4 Memory (3200 MT/s)

On the NVIDIA A100, cutlass\_halfhalf and cutlass\_tf32\_tf32 are faster than cublas\_simt for all matrix sizes. Furthermore, they are faster than the theoretical peak performance of FP32. The performance of cutlass\_halfhalf achieves 51 TFlop/s and cutlass\_tf32\_tf32 achieves 33 TFlop/s at maximum peak. The theoretical peak performance of FP16 Tensor Core and TF32 Tensor Core on NVIDIA A100 is 312 TFlop/s and 156 TFlop/s respectively [20]. Therefore, the theoretical upper limit of our method is 312/3 = 104 TFlop/s for cutlass\_halfhalf and 156/3 = 52 TFlop/s for cutlass\_tf32\_tf32 since we need three times more computation for the error correction as shown in Eq. (24). Thus, the ratio against the theoretical peak is 49% for cutlass\_halfhalf and 63% for cutlass\_tf32\_tf32. For the evaluation on the other GPUs, although cutlass\_halfhalf is faster than cublas\_simt for all matrix sizes, cutlass\_tf32\_tf32 is slower than cublas\_simt in some cases. We show the specifications of each GPU in Table 5. The theoretical peak performance of cutlass\_tf32\_tf32 on RTX3090, which is 71/3 = 23.7 TFlop/s, is lower than FP32, which is 35.58 TFlop/s. The GA102 architecture, which RTX 3090 and A6000 are equipped with, can execute FP32 operations on the datapath for integer operations. And the theoretical peak performance of FP32 shown in Table 5 is calculated as a sum of FP32 datapath and integer datapath performance. Therefore, if the performance of cuBLAS on RTX 3090 is improved by using this feature more, it might be impossible for cutlass\_tf32\_tf32 to outperform the cuBLAS SGEMM. Furthermore, we show a roofline performance analysis[29] on NVIDIA A100 in Figure 15. Our implementations do not reach the theoretical peak performance and memory bandwidth. Therefore, we acknowledge that there is still room for improvement in the implementation.

The power consumption evaluation

We calculate the power consumption per matrix-matrix multiplication using the best CUTLASS template parameters (Figure 16). We use NVML (NVIDIA Management Library) to monitor the power consumption every 0.02 sec and aggregate the data\(^8\). To obtain enough data for the evaluation, we compute a sequence

\(^8\)https://github.com/enp1s0/gpu_monitor
Figure 15: Roofline performance analysis for maximum and minimum execution. The theoretical peak performances of cutlass_fp16fp16 and cutlass_tf32tf32 are approximated by dividing the peak performance of Tensor Cores by 3.

Figure 16: The evaluation of power consumption on NVIDIA A100, RTX A6000, and GeForce RTX 3090 for matmul-\((m, n, k)\). The solid lines show single-precision matrix-matrix multiplication in FP32 accuracy (high accuracy) while the dashed lines are for FP16 accuracy (low accuracy).
of matrix-matrix multiplication for at least 2 sec. We evaluate the power consumption on NVIDIA A100, RTX A6000, and GeForce RTX 3090.

Similar to the computational throughput in the previous section, the power consumption of cutlass_halfhalf and cutlass_tf32tf32 on NVIDIA A100 is lower than cublas_sint for all matrices. The performance-per-power-consumption of cutlass_halfhalf achieves 121 GFlops/W and cutlass_tf32tf32 achieves 80.9 GFlops/W at maximum peak while cublas_sint is 67.0 GFlops/W. Although the power consumption of cutlass_halfhalf is also lower than cublas_sint on the other GPUs for all matrices, cutlass_tf32tf32 is higher than cublas_sint for some matrices. The power consumption and computing time are proportional in many cases.

Summary of experiments

We show the summary of the experiments in Table 6. For cutlass_tf32tf32 on A100, we are able to perform single-precision matrix-matrix multiplication faster than cuBLAS SGEMM, while retaining the exact same accuracy. For cutlass_halfhalf, although the exponent range it can handle is limited, it computes single-precision matrix-matrix multiplication faster than cuBLAS with lower power consumption on all three GPUs.

Conclusion

In this paper, we improve upon the error correction methods proposed by Markidis et al. and Feng et al. for matrix-matrix multiplication on Tensor Cores. To the extent of our knowledge, this is the first time the accuracy of GEMM on Tensor Cores has matched the accuracy of cuBLAS SGEMM through error correction while outperforming the FP32 theoretical peak performance. We use CUTLASS as the base for our implementation, and reach approximately 56% of the theoretical peak performance on NVIDIA A100.

We also perform a thorough analysis of the expected error caused by different rounding modes. We calculate the expectation of mantissa length kept in our method under an i.i.d. assumption of mantissa bits and prove that the loss in mantissa length is not the main cause of error in the previous work by Markidis et al. and Feng et al.. To improve the accuracy, we avoid the RZ rounding performed inside Tensor Cores and reduce the underflow and gradual underflow probabilities. Furthermore, we reduce the amount of computation during the error correction by ignoring the last term between the differences.

As a result, our implementation computes single-precision matrix-matrix multiplication with the same accuracy as cuBLAS SGEMM while exceeding the throughput of cuBLAS SGEMM, and also exceeding the theoretical peak performance of FP32 on NVIDIA A100. Our implementation also consumes lower power compared to cuBLAS SGEMM.

| Implementation    | Accuracy            | Computing Performance | Power Consumption |
|-------------------|---------------------|-----------------------|--------------------|
|                   |                     | A100                  | Other GPUs        |
|                   |                     | Faster (Max: 33TFlop/s) | Case-by-case Lower |
|                   |                     | Faster (Max: 51TFlop/s) | Faster Lower Lower |

Table 6: Comparison between our implementations and cuBLAS single-precision matrix-matrix multiplication.
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References

[1] Pierre Blanchard, Nicholas J. Higham, Florent Lopez, Theo Mary, and Srikara Pranesh. Mixed Precision Block Fused Multiply-Add: Error Analysis and Application to GPU Tensor Cores. *SIAM Journal on Scientific Computing*, 42(3):C124–C141, January 2020. Publisher: Society for Industrial and Applied Mathematics.

[2] Keith A. Britt, Fahd A. Mohiyaddin, and Travis S. Humble. Quantum Accelerators for High-Performance Computing Systems. *2017 IEEE International Conference on Rebooting Computing (ICRC)*, pages 1–7, November 2017. arXiv: 1712.01423.

[3] R. Carrasco, R. Vega, and C. A. Navarro. Analyzing GPU Tensor Core Potential for Fast Reductions. In *2018 37th International Conference of the Chilean Computer Science Society (SCCC)*, pages 1–6, November 2018. ISSN: 1522-4902.

[4] Erin Carson and Nicholas J. Higham. Accelerating the Solution of Linear Systems by Iterative Refinement in Three Precisions. *SIAM Journal on Scientific Computing*, 40(2):A817–A847, January 2018. Publisher: Society for Industrial and Applied Mathematics.

[5] Abdul Dakkak, Cheng Li, Jinjun Xiong, Isaac Gelado, and Wen-mei Hwu. Accelerating reduction and scan using tensor core units. In *Proceedings of the ACM International Conference on Supercomputing*, ICS ’19, pages 46–57, New York, NY, USA, June 2019. Association for Computing Machinery.

[6] Massimiliano Fasi, Nicholas J. Higham, Mantas Mikaitis, and Srikara Pranesh. Numerical Behavior of the NVIDIA Tensor Cores, April 2020. Issue: 2020.10 Number: 2020.10.

[7] Boyuan Feng, Yuke Wang, Guoyang Chen, Weifeng Zhang, Yuan Xie, and Yufei Ding. EGEMM-TC: accelerating scientific computing on tensor cores with extended precision. In *Proceedings of the 26th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, PPoPP ’21, pages 278–291, New York, NY, USA, February 2021. Association for Computing Machinery.

[8] Joshua Finkelstein, Justin S. Smith, Susan M. Mniszewski, Kipton Barros, Christian F. A. Negre, Emanuel H. Rubensson, and Anders M. N. Niklasson. Quantum-based Molecular Dynamics Simulations using Tensor Cores. arXiv:2107.02737 [physics, physics:quant-ph], July 2021. arXiv: 2107.02737 version: 1.

[9] J. S. Firoz, A. Li, J. Li, and K. Barker. On the Feasibility of Using Reduced-Precision Tensor Core Operations for Graph Analytics. In *2020 IEEE High Performance Extreme Computing Conference (HPEC)*, pages 1–7, September 2020. ISSN: 2643-1971.

[10] Chu Guo, Youwei Zhao, and He-Liang Huang. Verifying Random Quantum Circuits with Arbitrary Geometry Using Tensor Network States Algorithm. *Physical Review Letters*, 126(7):070502, February 2021. Publisher: American Physical Society.
[11] A. Haidar, S. Tomov, J. Dongarra, and N. J. Higham. Harnessing GPU Tensor Cores for Fast FP16 Arithmetic to Speed up Mixed-Precision Iterative Refinement Solvers. In SC18: International Conference for High Performance Computing, Networking, Storage and Analysis, pages 603–613, November 2018.

[12] IBM. IBM Power Systems Announces POWER10 Processor. https://www.ibm.com/blogs/systems/ibm-power-systems-announces-power10-processor/, 2020.

[13] Intel. Ponte Vecchio. https://download.intel.com/newsroom/2021/client-computing/intel-architecture-day-2021-presentation.pdf, 2021.

[14] Zhe Jia, Marco Maggioni, Benjamin Staiger, and Daniele P. Scarpazza. Dissecting the NVIDIA Volta GPU Architecture via Microbenchmarking. arXiv:1804.06826 [cs], April 2018. arXiv: 1804.06826.

[15] Norman P. Jouppi, Cliff Young, Nishant Patil, and et al. In-Datacenter Performance Analysis of a Tensor Processing Unit. In Proceedings of the 44th Annual International Symposium on Computer Architecture, ISCA ’17, pages 1–12, New York, NY, USA, June 2017. Association for Computing Machinery.

[16] Yong (Alexander) Liu, Xin (Lucy) Liu, Fang (Nancy) Li, Haohuan Fu, Yuling Yang, Jiawei Song, Pengpeng Zhao, Zhen Wang, Dajia Peng, Huarong Chen, Chu Guo, Heliang Huang, Wenzhao Wu, and Dexun Chen. Closing the "quantum supremacy" gap: achieving real-time simulation of a random quantum circuit using a new Sunway supercomputer. In Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis, SC ’21, pages 1–12, New York, NY, USA, November 2021. Association for Computing Machinery.

[17] Stefano Markidis, Steven Wei Der Chien, Erwin Laure, Ivy Bo Peng, and Jeffrey S. Vetter. NVIDIA Tensor Core Programmability, Performance & Precision. arXiv:1803.04014 [cs], March 2018.

[18] Daichi Mukunoki, Katsuhisa Ozaki, Takeshi Ogita, and Toshiyuki Imamura. DGEMM Using Tensor Cores, and Its Accurate and Reproducible Versions. In High Performance Computing, Lecture Notes in Computer Science, pages 230–248, Cham, 2020. Springer International Publishing.

[19] NVIDIA. NVIDIA A100 TENSOR CORE GPU. https://images.nvidia.com/aem-dam/en-zz/Solutions/data-center/nvidia-ampere-architecture-whitepaper.pdf, 2020.

[20] NVIDIA. NVIDIA AMPERE GA102 GPU Architecture V1. https://images.nvidia.com/aem-dam/en-zz/Solutions/geforce/ampere/pdf/NVIDIA-ampere-GA102-GPU-Architecture-Whitepaper-V1.pdf, 2020.

[21] NVIDIA. NVIDIA AMPERE GA102 GPU Architecture V2. https://www.nvidia.com/content/PDF/nvidia-ampere-ga-102-gpu-architecture-whitepaper-v2.pdf, 2020.

[22] Hiroyuki Ootomo and Rio Yokota. Randomized SVD on Tensor Cores. ISC High Performance, Research poster, June 2020.

[23] Katsuhisa Ozaki, Takeshi Ogita, Shin’ichi Oishi, and Siegfried M. Rump. Error-free transformations of matrix multiplication by using fast routines of matrix multiplication and its applications. Numerical Algorithms, 59(1):95–118, January 2012.

[24] Preferred Networks. MN-Core - Accelerator for Deep Learning. https://projects.preferred.jp/mn-core/en/, 2018.
[25] Md Aamir Raihan, Negar Goli, and Tor Aamodt. Modeling Deep Learning Accelerator Enabled GPUs. arXiv:1811.08309 [cs], February 2019. arXiv: 1811.08309.

[26] Ryuichi Sakamoto, Masaaki Kondo, Kohei Fujita, Tsuyoshi Ichimura, and Kengo Nakajima. The Effectiveness of Low-Precision Floating Arithmetic on Numerical Codes: A Case Study on Power Consumption. pages 199–206, January 2020.

[27] A. Sorna, X. Cheng, E. D’Azevedo, K. Won, and S. Tomov. Optimizing the Fast Fourier Transform Using Mixed Precision on Tensor Core Hardware. In 2018 IEEE 25th International Conference on High Performance Computing Workshops (HiPCW), pages 3–7, December 2018.

[28] Benjamin Villalonga, Dmitry Lyakh, Sergio Boixo, Hartmut Neven, Travis S. Humble, Rupak Biswas, Eleanor G. Rieffel, Alan Ho, and Salvatore Mandrù. Establishing the quantum supremacy frontier with a 281 Pflop/s simulation. Quantum Science and Technology, 5(3):034003, April 2020. Publisher: IOP Publishing.

[29] Samuel Williams, Andrew Waterman, and David Patterson. Roofline: an insightful visual performance model for multicore architectures. Communications of the ACM, 52(4):65–76, April 2009.

[30] Orestis Zachariadis, Nitin Satpute, Juan Gómez-Luna, and Joaquín Olivares. Accelerating sparse matrix–matrix multiplication with GPU Tensor Cores. Computers & Electrical Engineering, 88:106848, December 2020.