Design and analysis of a three stage CMOS op-amp using indirect feedback compensation

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Abstract. With the rapid change in CMOS technology, the scaling has resulted in faster transistors. But the rate of decrease in threshold voltage is too low. The intrinsic gains from the transistors is diminishing and hence the open-loop gain. This led to paths for the techniques like vertical stacking which is not well suited for low power designs and has constraints on swing. Thus, horizontal cascading must be used to achieve higher gains for the op-amp at lower VDD. This paper presents a simple three stage class A op-amp using Indirect Feedback Compensation. The op-amp has been designed and simulated at 180nm process and it produces an open-loop gain of 84.7db, 45.65MHz unity gain frequency, 89˚ phase margin and 14.45V/μSec SR and it is capable to drive a 30pF load.

1. INTRODUCTION

Since its invention op-amp includes many interesting and useful design techniques so that its study is still in practice. op-amps have being used in power management ICs, data converters, filters, sensors, regulators etc. Most of the applications are made by employing op-amp circuits in negative feedback, which also helps to achieve stability. With the continued scaling in technology node, transition frequency is high and results in faster transistors. But the transconductance, output resistance and hence the intrinsic gain (gm*ro) of transistor is decreased. With scaling in supply voltage, low-power circuits should reduce thermal dissipation with the trend in miniaturization [14]. As a result, gain of the analog systems decreasing consistently with the scaling. One obvious solution is cascoding, which is a vertical stacking of devices. The problem with stacking is there will be a swing limit and is not suited for low voltage design [3]. In order to overcome this, we must go with horizontal cascading. The process variations become significant with scaling leading to random offsets [1], [2]. Scaling also affects the linearity and accuracy of analog systems. The DC gain of individual stages must be increased to compensate the effect of scaling on accuracy. Thus, to meet the gain requirements of op-amp at nano-scale process, multi-stage op-amp topologies have become important [6]. However, the multistage op-amp suffers from the closed loop stability and bandwidth reduction due to increasing the number of frequency poles [5]. This paper is arranged in such a way that section 2 contains the need for frequency compensation, where a detailed analysis of compensation in two stage op-amp is explained. Section 3 contains three stage op-amp, section 4 contains proposed circuit, section 5 contains the design methodology followed by results and conclusion.

2. NEED FOR COMPENSATIONS

It is noted that system with single pole (corner frequency) is inherently stable. Without the compensation capacitor (Cc) op-amp will oscillate and hence the system is unstable, and it is observed
that phase margin is negative. In a two-stage op-amp without Cc, there will be poles present in the same frequency range in the left-hand plane (LHP) only. If all poles are in LHP then the system must be stable, but if there are multiple poles at the same location in LHP then also it will lead to instability. So, the poles in same frequency range also comes under this case and lead to unstable system. We need to split these poles such that one becomes dominant and other is a non-dominant pole. Then the system will behave like single pole system which is inherently stable [7]. Dominant pole is the one which has frequency approximately minimum of 5 times than the non-dominant pole frequency.

![Figure 1. Conventional two stage op-amp](image)

To achieve this, we use a compensation capacitor between the two stages i.e., from output of first stage to the output of second stage. After keeping this Cc, poles will split but a zero will form in the RHP. The location of Zero has nothing to do with the stability. But the obtained phase margin is significantly low. To overcome this, we keep a resistor in series to Cc. We need large value of Cc for pole splitting and to get higher unity gain frequency. But having large Cc will lead to larger area so we will take the advantage of miller effect, by keeping over the second stage i.e., from second stage input to output. The small value of CC will save layout area [11]. This method of maintaining enough phase margin is called Frequency Compensation technique [13]. The op-amp with this kind of configuration is called as Miller op-amp. Op-amps with higher gain will have phase margin of more than 45 degrees, even though the op-amp is non-compensated. But for op-amps with lower gain, the phase margin is lower than 45 degrees and there is chance of less stable. Hence, op-amps with high gain are easy to compensate and the op-amps with low closed loop gain are difficult to compensate for ensuring stability. So, frequency compensation is very much mandatory to stabilize closed loop 3 stage op-amps as well. In this paper, Indirect Feedback Compensation [4] is used where the compensation current is feedback indirectly from output node to internal high impedance node [13].

| Table 1. Design Parameters |
|----------------------------|
| Transistor | Geometry |
| M0         | 6/0.5    |
| M1, M2     | 3/0.5    |
| M3, M4     | 7/0.5    |
| M5         | 45/0.25  |
| M6         | 19/0.25  |
| M7         | 6/0.5    |

Table 1 provides the sizes of transistors that were used in designing the conventional 2 stage op-amp.
The sizes are given in μm/μm.

3. THREE STAGE OP-AMP

The conventional two stage op-amp circuit shown in figure 1 is suffering with asymmetrical slew rate. It is having a large positive slew rate (SR+) but negative slew rate (SR-) is less. Three stage op-amp is at least a third order system with a minimum of 3 poles and 2 Zeros. The block diagram of generalized three stage op-amp using Indirect Feedback Compensation is shown below in figure 2. The indirect current fed back from node 3 to internal high impedance node in the first stage through CC2 is given by $i_{C2}$ and current from node 2 to other high impedance node through CC1 is given by $i_{C1}$. 

![Figure 2. Block diagram of three stage op-amp](image)

For the above block diagram, the small signal model is shown below (figure 3).

![Figure 3. Small signal model of block diagram](image)

By applying nodal analysis at all the 3 nodes, we got 3 equations as follows:

\[
g_{m1}V_s + v_1sC_1 + \frac{v_2}{1 + sC_1R_1} - \frac{v_{out}}{1 + sC_2R_2} = 0
\]  

\[
-g_{m2}V_1 + v_2sC_2 + \frac{v_2}{1 + sC_1R_1} + \frac{v_2}{R_2} = 0
\]  

\[
g_{m3}V_2 + v_{out}sC_3 + \frac{v_{out}}{1 + sC_2R_2} + \frac{v_3}{R_3} = 0
\]

On solving these equations, we generalized the transfer function as follows:
Numerator is of the 2nd order with positive coefficients there will be two zeros in the LHP. The Zeros are located at

\[ z_1 = -\frac{1}{R_{C1}C_{G1}} \]

\[ z_2 = -\frac{1}{R_{C2}C_{C2}} \]

Denominator in the transfer function is of 5th order with positive coefficients indicating that there will be 5 poles in the LHP. If \( P_1 \) is the dominant pole i.e. magnitude of \( P_1 \) is very large than the magnitude of the other poles so that \( P_1 \) is located nearer to the origin. The dominant real pole is given as

\[ P_1 \approx \frac{1}{g_{m2}R_2g_{m2}R_1C_{C2}} \]

The unity gain frequency is approximately given by

\[ f_{un} = \frac{|P_1|A_v}{2\pi} \approx \frac{g_{m1}}{2\pi C_{C2}} \]

Slew rate was calculated as the ratio of drain current of M0 and Cc2 i.e. \( SR = \frac{I_{DM0}}{C C2} \) where \( IDM0 \) is the tail current coming from the transistor below the differential pair in the first stage.

### 4. PROPOSED CIRCUIT

![Proposed Three Stage Op-amp using Indirect Feedback Compensation](image)

**Figure 4.** Proposed Three Stage Op-amp using Indirect Feedback Compensation

The proposed three stage op-amp is shown in figure 4. The problem with conventional 2 stage op-amp is output node of first stage is connected to second stage output with a capacitor in between them. Because of this, unity gain frequency and phase margin are less. The idea here is disconnecting the
direct path from third stage output node and first stage output node which enhanced the unity gain frequency and phase margin. The differential pair with split length transistors is employed as first stage. In order to create the internal high impedance node, split length transistors have been used in input differential pair. Due to split length configuration, either M1A or M1B will be linear or cut-off but not in saturation. Hence low impedance node X is being formed. It is observed that 2nd stage must be a high bandwidth stage right hand plane zero reduces phase margin. Also, it is evident that 2nd stage must be a high bandwidth stage. So, here cascode amplifier with cascode load is used as 2nd stage. Finally, to meet the swing requirements at the output common source is used. The major problem in multi-stage amplifiers is Loading Effect. This effect is taken care by connecting the output node to gate terminal of next stage.

The circuit consists of two resistors Rc1 & Rc2 and two capacitors Cc1 & Cc2. As mentioned above the split length transistors created low impedance nodes X and Y. Current flows from third stage output node to low impedance node through Rc2 and Cc2. Similarly, one more current flow from second stage output to node X through Rc1 and Cc1. These two currents are reflected at the internal high impedance node Z in the first stage. From node Z it is given to second stage. Here the Rc2 and Cc2 are not connected directly to the first stage output node, which is the high impedance node the phase margin and unity gain frequency are improved as there is no RHP Zero. With the fact that most of the bio-medical applications require high gain and low power amplifiers with minimal chipset area [10]

Transistor sizes for the proposed circuit is shown in Table 2

| Transistor | Geometry |
|------------|----------|
| M1A, M1B, M2A, M2B | 5/2 |
| M3, M4, M5, M6 | 5/0.5 |
| M7 | 5.5/0.5 |
| M8, M9 | 6/0.5 |
| M0, M10 | 2.5/0.5 |

The above table provides the sizes of transistors that were used in designing the conventional 2 stage op-amp. The sizes are given in μm/μm.

### 5. DESIGN METHODOLOGY

Here we try to present the design procedure by considering that we are given with specifications

1. Begin with the specifications like open loop gain (AOL), Unity-gain frequency, Slew Rate, Phase Margin, maximum Power dissipation and VDD
2. From the maximum power dissipation and slew rate decide the bias current (in case of conventional 2 stage Op-amp) if bias current is used for biasing.
3. Distribute the required gain across all the individual stages.
4. Overdriven is chosen such that gate to source voltage, transition frequency and intrinsic gain of MOSFET are set
5. Choose a value for gm1 and gm2 is chosen based on desired phase margin
6. Choose CC2= gm1/(2π*fun)
7. Choose CC1 and gm3 such that pole-zero doublets (if any) are outside fun.
8. Finally simulate the design for transient and frequency response. If phase margin needs to be improved, then go back to step 5
6. RESULT

The comparison of various three stage op-amps is shown below in table 3. From [9], the phase margin should be a minimum of 45˚ before the implementation of closed loop configuration. Here we obtained a PM of 89˚. There was no effect of Rck and Cck on gain. Before using the op-amp in closed loop configuration, it should have enough high gain and here we obtained a gain of 84.70 dB. In its recent applications CMOS op-amp with large dynamic range and higher unity gain frequency are required [12]. The unity gain frequency indicates the speed of the system, 35.65 MHz was achieved.

The quality of the system was given by figure of merit. Higher figure of merit indicates the better performance of the system. In this work, small signal figure of merit (FOMS) and large signal figure of merit (FOML) were compared based on the following equations.

\[
\text{FOMS} = \frac{\text{fun} \times \text{CL}}{\text{power}}
\]

\[
\text{FOML} = \frac{\text{SR} \times \text{CL}}{\text{power}}
\]

Table 3. Comparison of various op-amps

|     | CL (\text{pF}) | AOL (dB) | PM fun (˚) (MHz) | SR (V/\mu\text{Sec}) | Power FOMS \(\left(\frac{\text{MHz}\times\text{pF}}{\text{mW}}\right)\) | FOML \(\left(\frac{\text{pF} \times V}{\mu\text{Sec} \times \text{mW}}\right)\) |
|-----|----------------|----------|------------------|-----------------------|-------------------------------------------------|-------------------------------------------------|
| 2 Stage | 5              | 56.52    | 56.49.45         | 9.67                  | 0.328 753.81                                    | 147.40                                         |
| NMC [9] | 25             | 80.73    | 74 17.83         | 7.6                   | 0.789 564.95                                    | 261.76                                         |
| RNIC [8] | 15             | 73.45    | 83 28.02         | 7.12                  | 0.68 618.10                                     | 157.10                                         |
| Pseudo [15] | 20             | 83.89    | 70.8 40.68       | 9.19                  | 1.28 635.63                                     | 143.60                                         |
| This work | 30             | 84.70    | 80.9 45.6        | 14.4                  | 0.81 845.37                                     | 535.19                                         |

7. CONCLUSION

A simple 3 stage class A op-amp using Indirect feedback compensation has been analysed and presented. The indirect feedback compensation was practically implemented, and it is a superior technique for the compensation of op-amps. It resulted in faster op-amps. This technique can be applied to multi-stage fully differential op-amps as well. Op-amps using split length transistors is well suited for low-voltage designs.

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