DNNFuser: Transformer as a Generalized Mapper for Fusion in DNN Accelerators

Sheng-Chun Kao*  
Georgia Institute of Technology  
Atlanta, GA  
felix@gatech.edu

Xiaoyu Huang*  
Georgia Institute of Technology  
Atlanta, GA  
xhuang394@gatech.edu

Tushar Krishna  
Georgia Institute of Technology  
Atlanta, GA  
tushar@ece.gatech.edu

ABSTRACT
Dataflow/mapping decides the compute and energy efficiency of DNN accelerators. Many mappers have been proposed to tackle the intra-layer map-space. However, mappers for inter-layer map-space (aka layer-fusion map-space), have been rarely discussed. In this work, we propose a mapper, DNNFuser, specifically focusing on this layer-fusion map-space. While existing SOTA DNN mapping explorations rely on search-based mappers, this is the first work, to the best of our knowledge, to propose a one-shot inference-based mapper. We leverage Transformer as our DNN architecture to learn layer-fusion optimization as a sequence modeling problem. Further, the trained DNNFuser can generalize its knowledge and infer new solutions for unseen conditions. Within one inference pass, DNNFuser can infer solutions with compatible performance to the ones found by a highly optimized search-based mapper while being 66x-127x faster.

CCS CONCEPTS
- Computer systems organization → Data flow architectures;  
- Computing methodologies → Reinforcement learning.

KEYWORDS
RL, Transformer, Transfer Learning, Dataflow, DNN Accelerator

1 INTRODUCTION
Accelerators for Deep Neural Network (DNN) models are commonplace today across the system stacks from cloud clusters [13] to edge devices [5, 6, 22]. For computation and energy efficiency, different dataflows/mappings [5, 22] have been proposed to optimize the data movement and compute utilization inside DNN accelerators. Many mappers have been proposed to automate this mapping optimization problem [9, 11, 15].

The conventional map-space of SOTA DNN mappers follows the assumptions of layer-by-layer execution in DNN accelerators [5, 9, 15]. Each layer of DNNs is mapped onto the accelerator sequentially and iteratively. The output activations are streamed out to the off-chip memory. Upon completion, those activations as inputs of the next layer are streamed back to on-chip buffer and computation units. This scheme often introduces a large number of off-chip memory accesses. With the increasing interest in high-resolution image processing or long-sequence language models, these off-chip access overheads start to stick out. Some prior researchers [1, 16, 32] have shown that a rarely explored mapping dimension could potentially ameliorate this off-chip access challenge –inter-layer dataflow (or so-called layer fusion).

Instead of sticking to layer-by-layer execution, layer fusion opens the discussion of mapping multiple layers to the DNN accelerators simultaneously to leverage the immediate data reuse of intermediate activations. Fused-layer CNN [1], TGPA [32], and FLAT [16] showcased huge potential benefits, however relying on their manual-designed layer fusion strategies. While many mappers are proposed to automate the search in intra-layer map-space, automated mappers for the layer fusion map-space have been rarely discussed.

In this paper, we propose DNNFuser, which is a Transformer-based mapper targeting the map-space of DNN layer-fusion. DNNFuser is an orthogonal work to existing intra-layer mappers [9, 11, 15]. We envision the proposed framework being further combined with the existing SOTA intra-layer mappers (as part of future work) to harvest and jointly explore both axes of performance improvement. We summarize the key technical innovations within DNNFuser as follows:

i) Layer-fusion Map space. DNNFuser is one of the first automated mappers to target the layer-fusion map-space while most prior work focuses on intra-layer map-spaces [9, 11, 15].

ii) Transformer-based Mapper. To the best of our knowledge, DNNFuser is the first mapper for DNN accelerators leveraging Transformer pre-training. The key feature is: once the mapper is trained, it could produce a mapping strategy at inference-time, i.e., no additional search process is needed. Many existing DNN mappers rely on optimization methods such as genetic algorithm (GA) [15], Bayesian Optimization (BO) [33], Mixed-Integer-Programming (MIP) [11], or RLs [34], which work well but require large search time. A recent work [9] shows gradient-based surrogate model could reduce the search time, however, a search process is still needed. In this work, we model the layer-fusion mapping optimization as a sequence modeling problem and leverage the Transformer as our underlying DNN architecture.

iii) Generalizability. We show that DNNFuser can generalize its knowledge to unseen HW conditions. In our study, we train DNNFuser to produce an optimized mapping that can condition on the current available on-chip buffer in the DNN accelerator. Note that the available on-chip buffer could vary since other small kernels could be running concurrently and occupying some portion of the on-chip buffer. Whenever the HW constraint (on-chip buffer) changes, the mapping needs to be updated, which means another search process for the search-based methods. In contrast, for DNNFuser, we can produce a new mapping at inference time.

iv) Transfer Learning. DNNFuser can be trained on several DNN workloads and serve as a general mapper. We show that the trained general mapper can execute transfer learning on a new DNN workload with only a few epochs of fine-tuning, demonstrating a strong sign of transferable generalized knowledge.

*Both authors contributed equally to this research.
2 BACKGROUND ON DNN ACCELERATORS

DNN accelerator design points often can be described with two parts: HW resources and the mapping strategy.

Hardware Resources. Spatial DNN accelerators [5] comprise an array of processing elements (PEs) (Fig. 1). Each PE has a MAC to compute partial sums and a scratchpad to store weights, activations, and partial sums. The accelerators also house a shared on-chip (global) buffer to pre-fetch activations and weights from off-chip memory for the next tile of computation that will be mapped over the PEs. Networks-on-Chip (NoCs) are used to distribute data from the on-chip buffer to PEs, collect the partial or full outputs, and write them back to the on-chip buffer.

Intra-layer Mapping. Conventionally, we use mapping/dataflow to refer to intra-layer mapping [5, 15], which includes (1) tiling (how tensors are sliced, stored, and fetched across the memory hierarchy), (2) ordering (the order in which loop computations are performed), (3) parallelism (how compute is mapped across PEs in space), and (4) clustering (how to compute/buffer are structured into a hierarchy of levels). These form a search space as large as $O(10^{24})$ [15], which is not feasible for exhaustive search. Hence there is a wide array of works on searching through this map-space [9, 11, 15, 34].

Inter-layer Mapping: Layer Fusion. Inter-layer mapping (layer fusion) is an orthogonal map-space to intra-layer mapping. It decides a special tiling dimension across multiple dependent DNN layers. The layer fusion map-space grows exponentially with the number of layers in a DNN workload. For example, if we allow 64 tiling choices per layer (which we use in our evaluations), for an 18 layers DNNs such as Resnet18 [8], the map-space will become as large as $64^{18} = O(10^{32})$. With deeper DNN workloads such as Resnet50, Mobilenet-V2, and Mnasnet, the map-space grows to the order of $O(10^{90})$. In this map-space, prior works introduced manually-tuned fusion strategies [1, 16, 32], and no prior mappers, to the best of our knowledge, search this space automatically.

3 PROBLEM FORMULATION

In the DNN accelerator, the on-chip buffer is often limited and not able to stage the full output activation. The key idea of layer fusion is that, rather than streaming back the full output activation to the off-chip memory like in [9, 11, 15], we stage “partial” output activation on-chip to exploit data locality and thus boost data reuse.

Practitioners start to use “micro-batching” as the go-to strategy. With micro-batching, we will divide a batch of activations into multiple micro-batches. In practice, we search for the largest acceptable micro-batch size that allows us to stage all intermediate activations on-chip, which becomes the most naive micro-batching strategy. However, this naive strategy cannot maximize the reuse opportunity. Different layers produce different sizes of output activations, and a naive unified micro-batch size could leave the on-chip buffer under-utilized.

A more sophisticated layer-wise micro-batching strategy is needed to maximize the on-chip buffer utilization, minimize off-chip access, and finally improve the runtime (latency or throughput) performance.

We call a layer-wise micro-batching strategy — layer fusion strategy, since it is essentially dividing DNN layers into multiple fused-layers. For example, in Fig. 2 we have a layer fusion strategy for a 5-layer DNN workload. The strategy dictates the output micro-batch sizes of each layer, where the first value represents the input micro-batch size. We use “-1” to represent a signal to synchronize and stream data back to off-chip memory before proceeding to the next layer. This synchronization divides the dataflow into two groups of fused-layers, as shown in Fig. 2(b). The groups of fused-layers will be executed sequentially, as shown in Fig. 2(c). Fig. 2(a) shows a snapshot when the accelerator is executing fused-layer group-0. For an N layer DNN workload, the layer fusion strategy is represented as follows:

$$Strategy = [mB_0, mB_1, ..., mB_N]$$

where $mB_i$ is the micro-batch size of layer i. To search for the optimum the micro-batching (layer fusion) strategy, the problem formulation is as follows:

Problem formulation: Given a DNN workload, batch size, and available on-chip memory, produce a layer-fusion strategy that optimizes the end-to-end latency or throughput performance.

4 DNNFUSER

We propose DNNFuser, a pre-trained Transformer-based mapper for layer fusion optimization for DNN workloads. DNNFuser, with a fully trained model, features the ability to infer an optimized mapping for different HW conditions at inference time. As shown in Fig. 3, DNNFuser takes in the input of a workload (a DNN model and its batch size), HW parameters (number of PEs, on-chip BW, off-chip BW), and an HW condition (requesting on-chip buffer usage), and outputs an optimized mapping.

4.1 Motivation for using RLs and Transformers

The key objective is to train a generative model (a decoder model, or an encoder-decoder model where encoder can take in the condition) so that it can serve as a mapper while not incurring any search process. DNNs have been proven repeatedly to have some amount of “knowledge generalization” ability. Deep RLs (DRLs) become one of the best testimonies of this “generalizability”. Even though the number of possible frames (or states) in RL environments, such as Atari games and OpenAI gym, is often too large to be fully enumerated (similar challenge as in our layer fusion map-space), a

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1Layer fusion means we fuse the computation of two or more layers/operators together and map them onto the accelerator simultaneously so that their activations are staged on-chip and reused immediately.
Layer-Fusion strategy: \([mB_0 = 2, mB_1 = 2, mB_2 = 4, mB_3 = -1, mB_4 = 3, mB_5 = 3]\)

**Figure 2:** A layer-fusion mapping example on a 5-layer DNN model. (a) The hardware implication, (b) the introduced two group of fused-layer, and (c) the execution steps of each group.

well-trained DRL can play well in those environments and generalize its knowledge to states never seen before. This motivates us to take advantage of DRL in our layer fusion problem.

However, DRLs are also known for their “unstableness”, as they rely on NNs to learn the “connection” of each state itself in a long trajectory while also suffering from the delayed reward and vanishing gradient problems (which is even more challenging in our layer fusion problem (discussed in detail in Section 4.4.1)), and are also sensitive to the case-by-case setting of discount rate [3]. Transformers, meanwhile, are known for their powerful ability to make customized “connections” by attention mechanisms [31] even in long-sequence scenarios. Recent research [2, 3, 23] shows that learning RL problems with a Transformer is promising and “stable” because it can automatically learn how to attend to previous states and also avoid the discount rate problem.

Therefore, we decide to formulate layer fusion into an RL problem for the potential “generalizability” and utilize Transformers to learn the formulated RL problem for its “stability”.

### 4.2 Formulating Layer Fusion into RL Problem

We model a micro-batching decision for a layer in the DNN workload as one time-step in the RL environment. For an N layers DNN, the agent (DNNFuser) would go through N+1 time-steps, visiting N+1 states, making N+1 actions, and receiving N+1 rewards, before it receives a “done” signal and complete one trajectory.
Action. The action at time-step \( t \) is the micro-batch size of layer-\( t \) (\( mb_t \)), also note as \( a_t (\text{mb}_{t}) \).

State. We formulate a state at time-step \( t \) as follow,

\[
s_t = [K_t, C_t, Y_t, X_t, R_t, S_t, \bar{M}, P_{a_{t-1}}]
\]

(2)

The first 6 dimensions are the tensor shape of the current DNN layer. We use the 6-loop notation of CONV layer (other types of layers can also be mapped and represented with these 6-loop notations). \( K_t, C_t \) are output and input channels. \( Y_t, X_t \) are height and width of activations. \( R_t, S_t \) are height and width of weight kernels. \( \bar{M} \) is given as the currently available memory (normalized by the batch size). \( P_{a_{t-1}} \) designates the runtime performance (latency or throughput) after a series of actions: \( [a_0, ..., a_{t-1}] \). For example at time-step-0, where no previous actions have been made, \( P_0 \) will be the runtime performance before any layer fusion strategy is performed. At time-step-1, \( P_{a_0} \) is the runtime performance when we only apply layer fusion strategy to the first layer, and so on.

4.3 Transformers for RL-based Layer-Fusion Problem

Reinforcement learning is often noted as harder to converge, higher variance in the result, and unstable in training. Thus, there remains a long-lasting hope of converting RL into a supervised learning problem. Recently, an array of works [2, 3, 23] leverage Transformers to model off-line reinforcement learning and achieve SOTA performance in many typical RL tasks. Leveraging similar taxonomy, we convert our RL-based layer fusion formulation into a Transformer-based supervised learning problem as follows.

4.3.1 Formulation. We convert RL state transition into a sequence like a sentence in language models (similar to [2, 3, 23]). One trajectory of state transition is a sequence of reward, state, action pair, \([(r_0, s_0, a_0), ..., (r_N, s_N, a_N)]\), with \( N \) being the number of layers of the targeting DNN models. The Transformer will take this sequence as input and generate a prediction for the next action, \( \hat{a}_t \), as shown in Fig. 3. For supervised learning, the loss is taken as the Mean Square Error between the predicted action, \( \hat{a}_t \), and the actual action, \( a_t \), for \( t \in [0, 1, ..., N] \).

4.3.2 Discussion. There is two high-level intuition for why this formulation is specifically useful in our problem.

- 1) Sparse and distant reward. The correlation between action and reward is often sparse and distant in the layer fusion scenario. The optimal micro-batch and the corresponding impact on the overall memory usage for the current layer often do not depend closely on the last action (last micro-batch decision), but those several time-steps back. The transformer is expected to efficiently deal with the long-sequence scenario and excavate the relation between each action pair, near and far.

- 2) The attention layer in the Transformer is capable of finding shortcuts between individual trajectories [3]. This means that our DNNFuser can find paths that are missing from the dataset, and more specific to our layer-fusion scenario, some peak memory usages that it has never seen.

4.3.3 Conditional Reward. Rather than the common practice of taking only state or state-action pairs to generate a policy in traditional RLs [19, 20], we take the full reward-state-action pair as inputs as previously described. The benefit is that the reward is now exposed as input at the inference phase Fig. 3), which opens the opportunity to control the output (mapping solution) by the “desired” reward. This technique is also leveraged in [3].

We use “requesting/conditioning on-chip memory usage” as the conditioning (desired) reward (noted as \( r_\text{c} \)). This formulation brings three benefits:

- 1) The current available on-chip memory sizes are known parameters, therefore we could use it as a reasonable condition.

- 2) The heuristics tell that a layer fusion strategy that maximizes the on-chip memory usage often achieves better runtime performance. Therefore, we can expect a high-performance solution if conditioning on the total available memory.

- 3) By setting memory usage as a condition, it also set up a potential use case of generalizing to unseen memory sizes, discussed later in Section 4.6.
4.4 Training Data Collections

4.4.1 Imitation Learning and Teacher Model. An DNN learning trick, “imitation learning”, is found useful in training Transformers [2, 3, 23]. “Imitation learning” could be imitating and learning 1) from self previous experiences as used in related works [2, 3, 23] or 2) from another well-trained teacher model, which we use in this work and find it critical for Transformers to learn well in our layer fusion problem.

In previous work, such as Decision Transformer (DT) [3], the “imitation learning” dataset is collected by an RL agent sampling in the targeting Atari or OpenAI environment. However, we find that popular RL algorithms, including Advantage Actor-Critic (A2C) [20] and Deep Deterministic Policy Gradient (DDPG) [19], suffer from inefficient sampling when interacting with the layer fusion map-space, and their trajectories are therefore inefficient demonstrations for “imitation learning”.

We observe that, unlike Atari or OpenAI with smooth state transitions, in our mapping problem, state transits abruptly between two consecutive time-steps (e.g., the state includes information of current layer shape, which does not have deducible relation to the layer shape in next state), and that the variance is detrimental to the convergence of the mentioned RL algorithms. Thus, rather than letting the agent (our model) explore in the environment itself to collect “experiences”, which is particularly inefficient in this case, we decide to use a teacher model, with some prior knowledge, to demonstrate directly some good trajectories. Next, we will discuss the details of our teacher model.

4.4.2 Developed Teacher Model: G-Sampler. Gamma [15] is one of the SOTA intra-layer mappers for DNN accelerators. We extended Gamma to support inter-layer layer-fusion map-space and found it several orders of magnitude better in performance than other optimization methods such as A2C [20], PSO [17], DE [25], and so on [7, 10, 19, 24, 29], which we show in our evaluations (Section 5.2). We use the developed extended Gamma as our teach model and call it — G-Sampler. We use G-Sampler to search for optimal layer-fusion strategy given different on-chip buffer sizes.

Note that we empirically found that G-Sampler works well as a layer fusion mapper, which beats many optimization methods. However, G-Sampler is still a search-based method, which is inevitably slower than most of the inference-based DNN models. Therefore, G-Sampler only serves as a training data generator, which samples several good solutions (trajectories) in the layer-fusion environment (Fig. 3). DNNFuser, as a student, learns from these demonstrations and generalizes the knowledge to learn to generate optimized mapping at inference time.

4.5 Model Training and Inference

4.5.1 Training. With all the above-mentioned preparation and setup, we can now train our model. As shown in Fig. 3, the steps are as follows. 1) Data collection with teacher model. We take G-Sampler and ask it to search for several (4-10) sets of optimized mapping in different conditions (on-chip memory sizes). 2) Formulating into RL state transition. We take those solutions, which is a sequence of actions in RL terminology, and decorate them with the state and reward information to make it a state transition trajectory. These decorated trajectories will be stored in the replay buffer (essentially a place to house the training dataset). 3) Model training. We sample the training data from the replay buffer and train our model in an “imitation learning” fashion.

4.5.2 Inference. At inference time, the model takes in a conditioning reward, which is the conditioning on-chip buffer usage, and generates a sequence of actions as a solution in an auto-regressive manner. The actual on-chip buffer usage of the solution adheres to the desired condition.

4.6 Generalization and Transfer Learning

4.6.1 Generalization. After training, DNNFuser can work on not only the seen conditions (on-chip buffer sizes) but also some unseen conditions. For example, we can train DNNFuser with some conditioning on-chip buffer sizes, such as 16, 32, 48, and 64 MB, and it could generalize its knowledge to the unseen interpolated buffer sizes between 16-64MB. For example, if the available buffer sizes in the HW suddenly change from 32MB to 28MB because some amount of buffer is occupied by other small procedures. We do not need to re-train the model (or launch a new search as we will need in a traditional search-based method). We can simply do another inference with 28MB as the new condition, and DNNFuser with its generalized knowledge could infer a solution.

4.6.2 Transfer Learning. DNNFuser can be trained on one or several common DNN workloads and serve as a pre-trained model for transfer learning. For a new DNN workload, we can take this general model and fine-tune it on the new workload. The fine-tuning process only takes a few epochs to converge since the generalized knowledge in DNNFuser can be transferred and utilized in the new workload. Empirically, we find that fine-tuning process requires only 10% of the training epoch compared to training from scratches, and can achieve compatible or better performance than a training-from-scratch model.

5 EVALUATION

5.1 Setup

Workload. We experiment on several common DNN workloads, including VGG16 [28], Resnet18 [15], Resnet50 [8], Mnasnet [30], and Mobilenet-V2 [27].

Accelerator Assumption. We experiment on the DNN accelerator configurations of 1024 PEs, on-chip buffer sizes of 64 MB, off-chip memory BW of 900GB/s, on-chip memory BW of 9000GB/s, and frequency of 1GHz, which is similar to [5, 13]. We set this as our underlying DNN accelerator modeled by our cost model.

Cost Model. We built an analytical cost model to model the effect of layer fusion in DNN accelerators. The cost model focuses on modeling interactions between layers and assumes the ideal performance for intra-layer map-space, which can already be achieved by existing intra-layer mappers [9, 15]. The cost model takes in a DNN workload, the number of PEs, on-chip memory size, on-chip and off-chip memory bandwidths (BW), and a layer fusion strategy, and returns its runtime performance and peak memory usage. The built cost model is validated against MAESTRO [18], which is in turn validated against real chip performance.
Baseline Mapping. Our baseline mapping, no-fusion mapping, is the best possible mapping without exploring layer fusion map-space (i.e., the most ideal mapping in intra-layer map-space), representing mapping that can be found by existing SOTA mappers [9, 11, 15]. To compare the effectiveness of the different searching algorithms for this fusion strategy search problem, we compute the speedup of the solution proposed by each searching algorithm (a fusion-based mapping) to the baseline mapping (no-fusion mapping).

Baseline Search Methods. Among optimization methods, we compare with many widely used ones as our baseline search methods for the inter-layer mapping, including Particle Swarm Optimization (PSO), Covariance matrix adaptation evolution strategy (CMA-ES), Differential Evolution (DE), Test-based population-size adaptation (TBPSA) and standard GA (stdGA), whose implementations are from nevergrad [26] by Facebook. We also implement an RL method A2C [20]. We allow all of them to have sampling budgets of 2K.

Baseline Sequence Model. DNNFuser is a Transformer-based sequence models. To show the effectiveness of Transformer as the sequence model for this problem, We also implement an RNN-based sequence-to-sequence model (Seq2Seq) as a baseline sequence model. The Seq2Seq is made of a LSTM with 2 layers of fully connected layers and 128 hidden dimension in each encoder and decoder.

Performance Metric. To fairly compare the effectiveness of optimization methods, we compare the achieved speedup of their layer-fusion solutions over the baseline mapping.

Implementation Details of G-Sampler. G-Sampler, our developed search method (Section 4.4.2), has a population size of 40 and runs for 50 generations, which also ends at a sampling budget of 2K as baselines do.

Implementation Detail of DNNFuser. DNNFuser is made of three transformer blocks, two heads, and a hidden dimension size of 128. We train the model for 100K epochs.

5.2 Comparisons with Baselines

First of all, the sampling efficiency\(^3\) of the optimization algorithms will decide the quality of the found solutions. In this experiment, the constraint is the on-chip memory usage, and the objective is to minimize the latency. Many baseline methods such as PSO, CMA, DE, and so on, cannot meet the on-chip memory usage constraint. Note that their memory usage is larger than 20MB (or 40MB at the bottom half the table) in Table 1. Therefore their solution is invalid, and we mark the invalid solution as N/A. They cannot find valid solution within the given 2K sampling budget. Given "enough" sampling budget, they will eventually limit the latency and not achieve the speedup target. However, 2K sampling budget already take them 1-2 hours. The need of more sampling budget and more hours makes these baseline methods not ideal for this problem.

A2C can successfully find a valid solution within the sampling budget. However, it takes around 5 hours, and its solution ends up worse than the baseline mapping, i.e., speedup smaller than 1.0.

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Table 1: Performance comparisons of different optimization methods on VGG16 workload with two different cases of on-chip memory constraints. The speedup is the latency of the found mapping by each search algorithm to the latency of the baseline mapping (described in Section 5.1). All the experiments run on a 4-core Intel Xeon CPU with a Nvidia GTX 1070 GPU.

| Algorithm | Case-1 | Case-2 |
|-----------|--------|--------|
| On-chip Memory constraint 20M, Batch size 64 | On-chip Memory constraint 40M, Batch size 128 |
| PSO       | N/A    | 102.76 | N/A    | 255.3 |
| CMA       | N/A    | 186.25 | 91.42  |
| DE        | N/A    | 114.0  | 104.74 |
| TBPSA     | N/A    | 153.34 | 106.20 |
| stdGA     | N/A    | 139.69 | 151.74 |
| A2C       | 0.98   | 2.26   | 293.81 |
| G-Sampler | 1.19   | 16.46  | 0.66   |
| Seq2Seq   | 1.05   | 16.06  | 0.01   |
| DNNFuser  | 1.20   | 19.27  | 0.01   |

Table 2: Speedup performance of DNNFuser (DF) and Seq2Seq (S2S) on unseen conditioning memory usage (20, 25, 30, 35, 40, and 45MB). DNNFuser is only trained on conditioning memory usage of 16, 32, 48, and 64MB.

| Model (Batch=64) | VGG16 | Resnet18 |
|------------------|-------|----------|
| Cond. Mem. Usage (MB) | DF   | S2S | DF | S2S | DF | S2S |
|------------------|------|-----|----|-----|----|-----|
| 20               | 1.20 | 1.04| 1.19| 1.27| 1.32| 1.37|
| 25               | 1.20 | 1.04| 2.18| 1.27| 1.32| 1.34|
| 30               | 1.16 | 1.83| 1.86| 2.31| 1.56| 1.53|
| 35               | 1.88 | 1.85| 2.14| 2.31| 1.56| 1.53|
| 40               | 1.97 | 1.86| 2.17| 2.68| 1.56| 2.88|
| 45               | 1.97 | 2.02| 2.30| 2.68| 1.56| 2.95|

Next we discuss the choice of sequence model in our framework, it could be the Transformer-based DNNFuser or an RNN-based Seq2Seq model. For both sequence models, we leverage the G-Sampler to generate the examples (training data for the sequence models). G-Sampler itself can converge within around 1.3 mins and achieve 1.19x and 2.06x speedup over the baseline mapping. As for the sequence model, we could observe that both DNNFuser and Seq2Seq can perform well in our framework in terms of search time and achieved speedup. However, DNNFuser can constantly find better solution, achieving more speedup than Seq2Seq. DNNFuser takes around 0.6-1.3 mins for searching and achieves 1.19x and 2.06x speedup over the baseline mapping. DNNFuser can find the

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\(^3\)The performance improvement over number of samples.
We train DNNFuser on VGG16 and Resnet18 respectively, using the memory condition of on-chip memory usages of 16, 32, 48, and 64MB. Without re-training, DNNFuser can directly generalize its knowledge to unseen HW conditions and infer corresponding solutions, the memory condition of 20, 25, 30, 35, 40, and 45, as shown in Table 2. Note that all of these conditions are unseen for the trained DNNFuser, and they are the interpolation of the range of memory condition (16 - 64MB) that DNNFuser is trained on\(^a\). With only one inference, DNNFuser and Seq2Seq can both find solutions with compatible performance to G-Sampler while G-Sampler is running full-search. Among DNNFuser and Seq2Seq, we can observe their performance is compatible on VGG16. However, on Resnet18 DNNFuser is a clear win. It is because Resnet18 forms a longer sequence, and DNNFuser (a Transformer-based model) performs better than Seq2Seq (a RNN-based model) at longer sequence tasks.

5.3 Generalizing to Unseen HW Condition

We train DNNFuser on VGG16 and Resnet18 respectively, using the memory condition of on-chip memory usages of 16, 32, 48, and 64MB. Without re-training, DNNFuser can directly generalize its knowledge to unseen HW conditions and infer corresponding solutions, the memory condition of 20, 25, 30, 35, 40, and 45, as shown in Table 2. Note that all of these conditions are unseen for the trained DNNFuser, and they are the interpolation of the range of memory condition (16 - 64MB) that DNNFuser is trained on\(^a\). With only one inference, DNNFuser and Seq2Seq can both find solutions with compatible performance to G-Sampler while G-Sampler is running full-search. Among DNNFuser and Seq2Seq, we can observe their performance is compatible on VGG16. However, on Resnet18 DNNFuser is a clear win. It is because Resnet18 forms a longer sequence, and DNNFuser (a Transformer-based model) performs better than Seq2Seq (a RNN-based model) at longer sequence tasks.

| Layer ID | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|----------|---|---|---|---|---|---|---|---|---|
| DNNFuser | 42 | -1 | 30 | 27 | -1 | 30 | -1 | 30 | -1 |
| G-Sampler | 64 | -1 | 36 | -1 | 64 | -1 | -1 | 25 | -1 |

5.4 Transfer Learning

To demonstrate the ability to execute transfer learning, we train DNNFuser on both VGG16 and Resnet18 to form a pre-trained general model. Then we use this general model to execute transfer learning on new DNN workloads: Resnet50, Mobilenet-V2, and Mnasnet. We fine-tune on new workloads (Transfer-DFs) with only 10% of the training epochs compared to training-from-scratch (Direct-DFs). As shown in Table 3, with only 10% of training epochs, Transfer-DFs can achieve compatible performance with G-Sampler and better performance than Direct-DFs (looking at some edge cases where Direct-DFs fail (N/A)). This tells that prior knowledge gained from pre-training actually increases the training speed and quality, which is especially important when training large DNN workloads such as Resnet50, Mobilenet-V2, or Mnasnet, which would otherwise require more training data. I.e., Direct-DFs need more teacher demonstrations from the Teacher model than Transfer-DFs. This observation showcases the usefulness of transfer learning—with a pre-trained general model of DNNFuser, we can learn new workloads faster and better.

5.5 Analysis of Found Solutions

In Fig. 4, we show one of the solutions found by DNNFuser and G-Sampler on ResNet18 with batch size 64 conditioning on memory size of 20MB. Values represent the micro-batch size of each layer, with LayerID 0 being the input to LayerID 1.

![Figure 4: The layer-fusion mapping found by DNNFuser and G-Sampler on ResNet18 with batch size 64 conditioning on memory size of 20MB.](image)

6 RELATED WORK

DNN Mapper. There are many DNN mapper proposals utilizing different optimization methods, such as simulated annealing in TVM [4], RL in FlexTensor [34] and ConfuciuX [14], Mixed Integer Programming in CoSA [11], domain-specific GA in GAMMA [15], gradient-based surrogate model in MindMapping [9], and many others. However, 1) all the previously mentioned prior arts are mappers for intra-layer map-space while DNNFuser is a mapper for the less explored inter-layer map-space, and 2) they are search-based methods while DNNFuser is an inference-based method.

Layer-Fusion. Some compiler works also study “Operator-Fusion” such as [12, 21], however, we want to clarify that “Operator-Fusion” usually fuses CONV or MatMul layer with element-wise operators such as ReLU but not several CONVs, FCs, or MatMul as we refer to by “Layer-Fusion”. “Layer-Fusion” has more complexity and is therefore often discussed in the context of inter-layer dataflow or mapping. Layer fusion is an orthogonal map-space to intra-layer mapping where most DNN mapper focuses on. Some recent works have looked into this map-space such as fused-layer CNN [1], TGPA [32], and FLAT [16] and demonstrate the huge potential performance improvement by leveraging this one additional mapping dimension in DNN mapping. However, the previously mentioned prior arts focus on proposing a hand-tuned layer fusion strategy for the considered use-cases. In contrast, DNNFuser is a mapper which can work on different use-cases automatically.

\(^a\)We leave the extrapolation as future work.
Transformers for RL Problems. Adapting RLs as sequence modeling problems has not been notably successful until some recent works, such as Decision Transformer [3]. Further applications showcase its vitality. Boustati et. al. [2] examined and discovered some significant potentials in transfer learning, and [23] by DeepMind developed the idea further to human-AI interaction. This work, to the best of our knowledge, is the first work using a transformer with RL formulation to tackle DNN mapping problem.

7 CONCLUSION

We propose a mapper, DNNFuser, for Layer-Fusion map-space, featuring its ability to find a solution at inference time, much faster compared to the best existing search-based mappers with comparable performance. DNNFuser can also generalize to unseen conditions and do transfer learning on a new DNN workload.

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