Preparation of flat surfaces on silicon carbide substrate using electron beam processing

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Abstract. Electron beam processing of 6H-SiC{0001} surfaces is studied. Initial substrates contain polishing scratches on (0001) face and rough surface of (000-1) face specially developed by KOH etching which are eliminated by electron beam processing. Processing is carried out in vacuum of 0.1 mTorr, energy about of 69 kJ, and background temperature of 1100 K in presence of 1-30 µm thick silicon film on the substrates. Atomic force microscopy images show near atomically flat surfaces which roughness decreases in 22-23 times for (000-1) and 1.5-2.0 times for (0001), respectively. Root-mean square value of processed surfaces are 0.27-0.30 nm for 5×5 μm² scan area. The steps (height of 0.5-1.0 nm) between the terraces (length of 500 nm) correspond to a height of 2-4 Si-C bilayers. The obtained changing of roughness factor also indicates a decrease of real surface area of the faces during electron beam processing.

1. Introduction
The key parameter to achieve quality epilayers and device structures on silicon carbide (SiC) substrate is quality of the surface prior to epitaxy. Commercially available SiC wafers have a large number of scratches and a residual subsurface defects or damaged layer [1-4]. This layer induced by mechanical impacts of abrasive particles during grinding and rough polishing is not eliminated even by chemical-mechanical polishing (CMP). Prior to epitaxial growth and device fabrication it is necessary to remove damaged layer and decrease surface roughness. It is known that finishing of silicon carbide is very difficult owing to its high hardness and chemical resistance. In recent years, several preparation techniques based on CMP are proposed to eliminate the damaged layer [2-4]. These are methods included surface modification and soft abrasive polishing. However, this approach does not exclude mechanical action and, accordingly, the residual layer is not completely removed. Moreover SiC polishing processes cannot be the same for each polytype, orientation and doping levels and has to be tuned to reach surface quality [1]. These drawbacks result in necessity to develop additional damage-free finishing processing technique for SiC wafers.

More promising, not only for epitaxy but also for graphene obtaining, non-mechanical approach to polish SiC is thermal surface modification [5-7]. And the thermal source can be vacuum annealing [7], laser and low-energy electron beams [5,6]. The perspective of the latter has been shown by previously received results [5,6,8]. After upgrade of the equipment, refining of production tools aimed at expanding the temperature range of processing, it became possible to carry out experimental studies of SiC polishing.

In this work we investigated surface preparation technique of 6H-SiC substrates by electron beam processing.
2. Experiments
The 6H-SiC substrates used for the study are Lely crystals doped to density of about \((\text{Nd-Na}) 10^{17} \text{ cm}^{-3}\). We use \{0001\} faces as samples: as-polished (0001) face and chemical etched (000-1) face. The latter samples were etched in molten potassium hydroxide (KOH) for 35 minutes to obtain “initial” increased surface roughness. Then all samples were cleaned according to standard RCA cleaning procedure and coated by 1-30 µm thick silicon layers in order to remove damage layer by electron beam activated dissolution. The technique is based on SiC dissolution mechanism in a pure Si melt [9] and presented with experimental methodic and processing conditions in [6,10]. We also gives physical-mathematical model designed to investigation of temperature distribution and melt lifetime in the structure during processing in [11]. The electron beam processing was carried out in vacuum of 0.1 mTorr, energy about of 69 kJ, and background temperature of 1100 K. After processing Si layer was removed in HNO_3:HF (3:1) solution. Measurements on the surfaces were made using Solver P47 Pro (NT-MDT, Russia) atomic force microscope in tapping mode.

3. Results and discussion
The surface morphology and profiles of \{0001\} faces for as-received or initial and electron beam processed samples are shown in Fig.1. Fig.2. The values of its roughness parameters: peak-to-peak \((R_y)\), ten point height \((R_z)\), average height \((H_a)\), average roughness \((R_a)\), root-mean-square \((R_q)\) roughness, surface skewness \((R_{sk})\) and coefficient of kurtosis \((R_k)\) are summarized in Table 1.

![AFM images](https://via.placeholder.com/150)

Figure 1(a-c). AFM images (a,b) of the (000-1) 6H-SiC substrate (a) KOH etched, (b) electron beam processed, and the corresponding profiles (c) to (a) – shading in gray, (b) – black line
Figure 2(a-c). AFM images (a,b) of the (0001) 6H-SiC substrate (a) as-received, (b) electron beam processed, and the corresponding profiles (c) to (a) – shading in gray, (b) – black line

Table 1. Effect of electron beam processing on surface roughness of {0001} 6H-SiC substrate

| Parameter | (000-1) face | (0001) face |
|-----------|-------------|-------------|
|           | KOH etched  | Processed   | As-received | Processed   |
| Ry, nm    | 52.67±1.88  | 2.27±0.24   | 4.61±0.52   | 2.04±0.21   |
| Rz, nm    | 26.02±0.89  | 1.14±0.11   | 2.35±0.28   | 1.05±0.12   |
| Ha, nm    | 16.63±1.38  | 1.19±0.19   | 2.02±0.55   | 1.01±0.10   |
| Ra, nm    | 5.09±0.60   | 0.21±0.02   | 0.39±0.09   | 0.23±0.06   |
| Rq, nm    | 6.67±0.60   | 0.27±0.02   | 0.53±0.12   | 0.30±0.06   |
| Rs,k, -   | 0.91±0.17   | −0.02±0.08  | 0.91±0.41   | 0.27±0.05   |
| Rk, -     | 2.34±1.63   | 0.21±0.09   | 3.83±0.50   | 0.63±0.41   |
| D, -      | <2.37>      | <2.13>      | <2.29>      | <2.21>      |
| Fr, -     | <7.78>      | <1.95>      | <4.99>      | <3.2>       |
As seen in figures and table, the roughness values of initial and as-received samples decreased by processing in about of 22-23 times for (000-1) and 1.5-2 times for (0001), respectively. The RMS values of both type processed samples are 0.27-0.30 nm for area of $5 \times 5 \mu m^2$. Surface skewness and kurtosis were changed from nonzero (asymmetric distribution) for initial surfaces to zero value (symmetric narrow distribution), which corresponds to normal and leptokurtic distribution. This behavior confirms the surface profile became more uniform. The steps (height of 0.5-1.0 nm) which can be seen between the terraces (length of 500 nm) correspond to a height of 2-4 Si-C bilayers [12]. The obtained changing of fractal dimension ($D$) and roughness factor ($Fr$, see Table 1) also indicates a decrease of real surface area of the faces during electron beam processing.

Processing conditions were chosen on the basis of the model [11] so as to ensure the proper thickness of the molten silicon, its temperature and dissolution time. The melt thickness at a fixed temperature determines the limit of the soluble thickness of the substrate (damaged layer). In our experiment, the thickness of the removed layer correlates with the average height ($Ha$) value and was from 1 to 15 nm.

4. Conclusion

In this paper electron beam processing of the (0001) and (000-1) faces of 6H-SiC has been presented. Surface roughness of the samples have been decreased in 1.5-20 times to 0.27-0.30 nm for RMS values. The steps of 0.5-1.0 nm in height (2-4 Si-C bilayers) and terraces up to 500 nm in length were found. The obtained changing of calculated roughness factor showed a significant decrease of real surface area of the faces during processing that indicates dissolution processes of substrate material.

Thus, electron beam processing of silicon carbide covered by silicon initiating a dissolution processes, has been allowed to produce formation of a clean, near-atomically flat surfaces of the substrates with removal of the damaged layer. This technique could be considered as a superfinsihing damage-free polishing complementary to standard chemical-mechanical process.

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