High-frequency performance of scaled carbon nanotube array field-effect transistors

Mathias Steiner¹,a), Michael Engel²,³, Yu-Ming Lin¹, Yanqing Wu¹, Keith Jenkins¹, Damon B. Farmer¹, Jefford J. Humes⁴, Nathan L. Yoder⁴, Jung-Woo T. Seo⁵, Alexander A. Green⁵, Mark C. Hersam⁵, Ralph Krupke²,³,⁶, and Phaedon Avouris¹,b)

¹ IBM Thomas J. Watson Research Center, Yorktown Heights, New York 10598, USA

² Institute of Nanotechnology, Karlsruhe Institute of Technology, 76021 Karlsruhe, Germany

³ DFG Center for Functional Nanostructures (CFN), 76028 Karlsruhe, Germany

⁴ NanoIntegris Inc., Skokie, IL 60077, USA

⁵ Department of Materials Science and Engineering and Department of Chemistry, Northwestern University, Evanston, IL 60208, USA

⁶ Institut für Materialwissenschaft, Technische Universität Darmstadt, 64287 Darmstadt, Germany

a) Electronic mail: msteine@us.ibm.com
b) Electronic mail: avouris@us.ibm.com
Abstract:

We report the radio-frequency performance of carbon nanotube array transistors that have been realized through the aligned assembly of highly separated, semiconducting carbon nanotubes on a fully scalable device platform. At a gate length of 100 nm, we observe output current saturation and obtain as-measured, extrinsic current gain and power gain cut-off frequencies, respectively, of 7 GHz and 15 GHz. While the extrinsic current gain is comparable to the state-of-the-art the extrinsic power gain is improved. The de-embedded, intrinsic current gain and power gain cut-off frequencies of 153 GHz and 30 GHz are the highest values experimentally achieved to date. We analyze the consistency of DC and AC performance parameters and discuss the requirements for future applications of carbon nanotube array transistors in high-frequency electronics.
Field-effect transistors made of semiconducting carbon nanotubes (CNTs) have excellent electrical DC characteristics and have been explored as possible successors to their silicon counterparts. Knowledge of their AC characteristics is, however, limited. For transistors made of a single CNT, because of the large impedance mismatch with the measurement system, such studies are extremely difficult and, ultimately, their output current is not sufficient for technological applications. In order to deploy CNTs in high-frequency electronics it is necessary to use an array. Nevertheless, there are problems associated with their separation, their aligned assembly at high densities, scaling of device dimensions, and minimization of device parasitics.

In this Letter, we introduce a scalable, planar device platform that enables the electric-field driven, in situ assembly of aligned CNT arrays from solution. We characterize field-effect transistors made of those arrays by means of electrical transport measurements in the DC and AC domain. Furthermore, we investigate the consistency of the experimental results and discuss the requirements for future applications of CNT array transistors in high-frequency electronics.

We produced CNT array field-effect transistors based on centrifugation-enriched solutions containing 99.6% semiconducting carbon nanotubes having an average diameter of 1.5 nm. A planar device platform with embedded electrodes allows for the controlled scaling of channel length, gate length, gate dielectric thickness, and contact length (see Fig. 1). Electron beam lithography with poly(methyl methacrylate) (PMMA) as the resist was used for all the patterning. In a first step, the device layout and alignment markers were patterned into the PMMA on top of highly resistive Si coated with a SiO2 layer having a thickness of 1µm, see Fig. 1(a). The pattern was transferred
into the underlying SiO$_2$ with a combination of reactive ion etching and wet chemical etching using buffered oxide etch, see Fig. 1(b). The resulting etch depth was 50 nm. The metal stack consisting of 5nm Ti, 45nm Au, and 1nm Ti was then sequentially evaporated on top of the structure. After lift-off in acetone, we obtained a planar device platform with embedded metal electrodes as shown in Fig. 1(c), thus avoiding performance degradation due to bending of the CNTs. In the next step, a gate dielectric layer made of 10nm HfO$_2$ ($\kappa=13$) grown by atomic layer deposition at 125°C was locally deposited through a PMMA mask window followed by lift off processing, see Fig. 1(d). We then assembled aligned CNT arrays having a density of $D=50\mu m^{-1}$ from an aqueous CNT solution by using low-frequency dielectrophoresis$^{15}$: a droplet (~30µl) of diluted CNT suspension (0.5µg/ml) was placed on the device structure while an alternating voltage ($V_{pp}=4V, f=300kHz$) was applied between the deposition electrode pairs for 10 minutes as schematically indicated in Fig. 1(e). The CNT solution was then replaced with de-ionized water and the surface was dried with a stream of $N_2$, see Fig. 1(f). We note that the CNTs do not make physical contact with the deposition electrodes underneath the dielectric. This way, material issues associated with heat dissipation during dielectrophoresis, such as electro-migration, are avoided. The device fabrication was completed by patterning source and drain contacts and evaporation of 0.5nm Ti, 40nm Pd, and 20nm Au, see Fig. 1(g). The (first-layer) deposition electrodes below the gate dielectric layer and the actual (second-layer) source and drain contacts of the device were shorted in order to reduce parasitic capacitances. Scanning electron microscopy images of the CNT array transistor are shown in Fig. 1(h).
Fig. 2 shows the DC electrical characterization of the CNT array transistor. The device exhibits a current density of $I_d = 50\mu A/\mu m$ and a transconductance of $g_m = \Delta I_d / \Delta V_g = 15 \mu S/\mu m$ at a gate length of $L_g = 100\text{nm}$. Most importantly, current saturation is observed in the output characteristics of the device; see Fig. 2(b). Accordingly, the output conductance $g_d = \Delta I_d / \Delta V_d$ drops to zero at a drain bias of $V_d = -2V$.

We determined the high-frequency performance of the CNT array transistors by measuring the scattering (S) parameters (see supplementary material). From this, we obtained the short circuit current gain cut-off frequency ($f_T$) and the maximum frequency of oscillation ($f_{\text{MAX}}$) as shown in Fig. 3(a). These frequencies characterize the highest frequencies at which electrical signals are propagated in the transistor and electrical power gain is achieved, respectively. The as-measured, extrinsic current gain $|h_{21}|$ of the CNT array transistor shows the expected -20dB/decade roll-off with an extrinsic cut-off frequency of $f_T^{\text{ext}} = 7\text{GHz}$ which is comparable to the state-of-the-art$^{10,12}$. Both the extrinsic unilateral power gain (U) and the extrinsic maximum available power gain (MAG) become 0dB at $f_{\text{MAX}}^{\text{ext}} = 15\text{GHz}$ which constitutes an improvement with respect to the state-of-the-art$^{10,12}$.

The performance of scaled high-frequency transistors is typically deteriorated by parasitic resistances and parasitic capacitances$^{16}$. While the extrinsic AC performance of a transistor is meaningful in the context of circuit design and integration, the intrinsic AC performance reveals the electrical transport properties of the channel material itself. The determination of the intrinsic transistor performance is routinely accomplished by de-
embedding techniques\textsuperscript{17,18} that have been widely adopted for characterizing electronic devices made of bulk semiconductors, as well as low-dimensional materials. The intrinsic AC cut-off frequency \( f_{T}^{\text{int}} \) is proportional to the DC transconductance \( g_{m} \) of the transistor and can be expressed by\textsuperscript{13}:

\[
f_{T}^{\text{int}} = \frac{g_{m}}{2\pi C_{g}}.
\]  

This expression allows for testing the consistency between the AC and DC measurements and constitutes an appropriate figure of merit to compare the performance potential of different semiconducting channel materials for high-frequency applications\textsuperscript{13}.

We use a de-embedding procedure based on “open” and “short” reference structures to determine the intrinsic high-frequency performance of the CNT array transistor (see supplementary material). Based on the extrinsic results shown in Fig. 3(a), we obtain an intrinsic current gain cut-off frequency \( f_{T}^{\text{int}} = 153\text{GHz} \) and an intrinsic power gain cut-off frequency \( f_{\text{MAX}}^{\text{int}} = 30\text{GHz} \) for \( L_{g} = 100\text{nm} \), see Fig. 3(b). The results demonstrate that the advancements made with respect to CNT separation, alignment and device scaling result in the highest intrinsic high-frequency CNT transistor performance reported so far.

We now investigate the consistency of the electrical transport measurements (DC and AC) and calculate the theoretical gate capacitance \( C_{g}^{\text{theo}} \) of an evenly spaced array of CNTs with density \( D \), which is given by\textsuperscript{19}:

\[
C_{g}^{\text{theo}} = D \left\{ \frac{1}{2\pi \varepsilon_{r} \varepsilon_{0}} \ln \left( \frac{\sinh (2\pi r D)}{\pi r D} \right) + \frac{1}{C_{q}} \right\}^{-1},
\]  

where \( C_{q} = 4 \cdot 10^{-10} \text{F} \cdot \text{m}^{-1} \) is the quantum capacitance of a CNT and \( r = 0.75\text{nm} \) is the average CNT radius. As in our experiments, the gate dielectric is HfO\textsubscript{2} having a thickness
\( t = 10\text{nm} \) and we assume a relative permittivity \( \varepsilon_r = (13+1)/2 \) to account for the fact that the CNTs are located at the HfO\(_2\)/air interface. By using a CNT density of \( D = 50\mu\text{m}^{-1} \), we obtain \( C_{g}^{\text{theo}} = 0.0013\text{pF} \). In Fig. 4(a), we plot the experimental \( f_T^{\text{int}} \)-values as function of the associated \( g_m \)-values for four different devices with \( L_g = 100\text{nm} \). By fitting Eq. (1) to the data, we obtain an experimental gate capacitance of \( C_g^{\text{exp}} = (0.0013 \pm 0.0001)\text{pF} \) which is in agreement with the calculated \( C_{g}^{\text{theo}} \)-value.

Furthermore, by using the experimental DC-value \( g_m = 15\mu\text{S/\mu m} \) and \( C_g^{\text{exp}} = C_{g}^{\text{theo}} = 0.0013\text{pF} \) in Eq. (1), we obtain \( f_T^{\text{int}} = 153\text{GHz} \), which is in agreement with the result of the S-parameter measurement, see Fig. 3(b).

We now analyze the intrinsic power gain cut-off frequency \( f_{\text{MAX}}^{\text{int}} \) which we relate to \( f_T^{\text{int}} \) in the following way\(^{13} \):

\[
f_{\text{MAX}}^{\text{int}} = \frac{f_T^{\text{int}}}{2\sqrt{g_d (R_{p,s} + R_g)} + 2\pi f_T^{\text{int}} C_{p,gd} R_g}.
\]

(3)

Here, \( R_{p,s} \) is the parasitic source resistance (\( R_{p,s} \approx 0.5R_{\text{device}} = 250\Omega \) in the present case), \( R_g = 45\Omega \) is the gate resistance, and \( C_{p,gd} \approx \frac{2}{3} \cdot C_{\text{gate}} = 0.03\text{pF} \) is the parasitic gate-to-drain capacitance that is estimated based on the geometric gate capacitance of the device, \( C_{\text{gate}} \). By using the experimental values \( g_d = 25\mu\text{S/\mu m} \) and \( f_T^{\text{int}} = 153\text{GHz} \) in Eq. (3), we obtain \( f_{\text{MAX}}^{\text{int}} = 55\text{GHz} \). In the case where we use \( C_{p,gd} = 0.13\text{pF} \), we are able to reproduce the experimental value \( f_{\text{MAX}}^{\text{int}} = 30\text{GHz} \) obtained by the S-parameter measurement, see Fig. 3(b). This relatively high \( C_{p,gd} \)-value of 0.13pF can be understood by considering the presence of the deposition electrodes in the device (see Fig. 1) which are not
accounted for in the conservative estimate $C_{p,gd} = \frac{2}{3} C_{\text{gate}}$. This analysis validates the consistency of the electrical transport measurements and shows the good correlation between the experimental AC parameters $f_T^{\text{int}}$ and $f_{\text{MAX}}^{\text{int}}$ and the measured DC parameters $g_m$ and $g_d$.

Finally, we discuss important technical requirements for future applications of CNT array transistors in high-frequency electronics. A key issue that needs to be addressed is the high contact resistance of CNTs in the solution-processed array. Based on our DC measurements, we estimate that the contact resistance of a single CNT can be as high as 500kΩ which is 50 times larger than the values achieved with single, as grown CNTs\textsuperscript{20}. This is likely due to incomplete removal of residual surfactant surrounding the CNTs. Lowering the resistance of the CNT-metal contacts would benefit both intrinsic and extrinsic device performance.

Significant performance improvements could be realized through device design and scaling over the course of this study. In Fig. 4(b), we plot the maximum intrinsic $f_T$-values that we obtained with different device concepts while maintaining the quality of CNT solutions at a high level of electronic separation (<1% metallic carbon nanotube admixture). Shortcomings of our previous top-gated and back-gated device concepts involved limited scalability, excessive gate leakage, and performance-degrading chemical treatment and bending of CNTs. The device concept reported here has overcome those limitations and holds great potential for further scaling and performance improvements. Implementing the manufacturing principle on a flexible plastic substrate as discussed in reference 21 could enable high-frequency applications that are not possible with state-of-the-art thin film transistor technology.
Further enhancements in performance are expected in transistors made of CNT solutions having a higher selectivity with respect to their diameter and, ultimately, with solutions containing only a single CNT chiral species\textsuperscript{22,23,24}, which may allow the application of such devices in logic circuits. Nevertheless, operation in analog radiofrequency circuitry\textsuperscript{8} is conceivable with the CNT solutions used in this study. In this respect, we note that our DC measurements indicate a self gain of the order $g_m/g_d \approx 10$ and further optimization is certainly possible. We point out, however, that the large-scale assembly of dense and aligned arrays of solution-processed CNTs remains a major challenge.

As compared to high-frequency transistors made of graphene\textsuperscript{25}, the presence of a band-gap in CNTs and the current saturation at shorter gate lengths suggest the possibility of higher power gain and lower standby power consumption.

**Acknowledgment**

We acknowledge discussions with A. D. Franklin, W. Haensch, S. O. Koswatta, and A. Valdes-Garcia (all IBM T. J. Watson Research Center) and thank J. J. Bucchignano, B. A. Ek, and G. P. Wright (IBM T. J. Watson Research Center) for expert technical assistance. M.C.H. acknowledges support by the National Science Foundation (DMR-1006391 and DMR-1121262) and the Nanoelectronics Research Initiative. N.L.Y. acknowledges support by the Office of Naval Research (ONR), grant # N00014-11-C-0135.
FIG. 1. Solution-assisted manufacturing of scaled carbon nanotube array transistors. (a-g) Schematic illustrations of the manufacturing steps for obtaining a planar device with embedded gate electrodes [labeled g in (e),(g)] and deposition electrodes [labeled a in (e),(f)]. In (g), source (s) and drain (d) electrodes of the transistor are also indicated. (h) Scanning electron microscope image of the dual channel device having a channel width of 2x20µm. (Inset) Magnified and colorized scanning electron microscopy image of the transistor channel showing 3 parallel carbon nanotubes (highlighted by red arrows) bridging the gated region (gray color) between source and drain electrodes (golden color).
FIG. 2. Electrical DC characteristics of the carbon nanotube array transistor. (a) Measured electrical $I_d$-$V_g$ transfer characteristics (black lines) and transconductance $g_m$ (red squares). (b) Measured electrical $I_d$-$V_d$ output characteristics (black lines) and output conductance $g_d$ (blue squares). The magnitude of the electrical parameters $V_d$, $V_g$ in the respective voltage sweeps are indicated on top.
FIG. 3. Electrical AC characteristics of the carbon nanotube array transistor. (a) The as-measured, extrinsic short-circuit current gain ($h_{21}$, red squares) shows -20dB/decade roll-off (black line: $1/f$-fit) and becomes 0dB at the current gain cut-off frequency $f_T$. The extrinsic, maximum available power gain (MAG, blue rings) and the extrinsic, unilateral power gain (U, green circles) becomes 0dB at the maximum frequency of oscillation, $f_{MAX}$. (b) Intrinsic short-circuit current gain ($h_{21}$, red squares; black line: $1/f$-fit), intrinsic maximum available power gain (MAG, blue rings), and intrinsic unilateral power gain (U, green circles). The measurement was performed at $V_{d}=-2V$, $V_{g}=-2V$. 
FIG. 4. (a) Plot of the measured transconductance $g_m$ (red squares) as function of the experimental, intrinsic current gain cut-off frequency $f_T$ for four different carbon nanotube array transistors with gate length of $L_g = 100\text{nm}$. A linear fit (black line) delivers the experimental value of the gate capacitance $C_g^{\text{exp}}$ that is also indicated. (b) Highest intrinsic cut-off frequency $f_T$ achieved (black circles) versus number of experimental iteration. The vertical lines separate the iteration steps that are based on different device (gate) concepts. In the device schematics, the gate electrodes are visualized in red color, source and drain electrodes are shown in blue color.
References

1. P. Avouris, Phys. Today 62, 34 (2009).
2. J. Appenzeller and D. J. Frank, Appl. Phys. Lett. 84, 1771 (2004).
3. S. Li, Z. Yu, S.-F. Yen, W. C. Tang, and P. J. Burke, Nano Lett. 4, 753 (2004).
4. S. Rosenblatt, H. Lin, V. Sazonova, S. Tiwari, and P. L. McEuen, Appl. Phys. Lett. 87, 153111 (2005).
5. A. A. Pesetski, J. E. Baumgardner, E. Folk, J. X. Przybysz, J. D. Adam, and H. Zhang, Appl. Phys. Lett. 88, 113103 (2006).
6. L. Nougaret, G. Dambrine, S. Lepilliet, H. Happy, N. Chimot, V. Derycke, and J. P. Bourgoin, Appl. Phys. Lett. 96, 042109 (2010).
7. E. D. Cobas, S. M. Anlage, and M. S. Fuhrer, IEEE Transactions on Microwave Theory and Techniques 59, 2726 (2011).
8. C. Kocabas, H.-S. Kim, T. Banks, J. A. Rogers, A. A. Pesetski, J. E. Baumgardner, S. V. Krishnaswamy, and H. Zhang, Proc. Nat. Acad. Sci. 105, 1405 (2008).
9. C. Kocabas, S. Dunham, Q. Cao, K. Cimino, X. Ho, H.-S. Kim, D. Dawson, J. Payne, M. Stuenkel, H. Zhang, T. Banks, M. Feng, Rotkin, S. V., and J. A. Rogers, Nano Lett. 9, 1937 (2009).
10. L. Nougaret, H. Happy, G. Dambrine, V. Derycke, J. P. Bourgoin, A. A. Green, and M. C. Hersam, App. Phys. Lett. 94, 243505 (2009).
11. C. Wang, A. Badmaev, A. Jooyaie, M. Bao, K. L. Wang, K. Galatsis, and C. Zhou, ACS Nano 5, 4169 (2011).
M. Schroter, P. Kolev, D. Wang, M. Eron, S. Lin, N. Samarakone, M. Bronikowski, Z. Yu, P. Sampat, P. Syams, S. McKernan, Microwave Symposium Digest (MTT), 2011 IEEE MTT-S International, 1 (2011).

C. Rutherglen, D. Jain, and P. Burke, Nat. Nanotechnol. 4, 811 (2009).

M. S. Arnold, A. A. Green, J. F. Hulvat, S. I. Stupp, and M. C. Hersam, Nat. Nanotechnol. 1, 60 (2006).

R. Krupke, F. Hennrich, H. B. Weber, D. Beckmann, O. Hampe, S. Malik, M. M. Kappes, and H. v. Loehneysen, Appl. Phys. A: Mat. Sci. & Proc. 76, 397 (2003).

F. Schwierz and J. J. Liou, Solid-State Electronics 51, 1079 (2007).

H. Cho and D. E. Burk, IEEE Trans. Electron. Dev. 38, 1371 (1991).

M. C. A. M. Koolen, J. A. M. Geelen, and M. P. J. G. Versleijen, IEEE Proceedings of the 1991 Bipolar Circuits and Technology Meeting, 188 (1991).

Q. Cao, M. Xia, C. Kocabas, M. Shim, J. A. Rogers, and S. V. Rotkin, Appl. Phys. Lett. 90, 023516 (2007).

A. D. Franklin and Z. Chen, Nat. Nanotechnol. 5, 858 (2010).

N. Chimot, V. Derycke, M. F. Goffman, J. P. Bourgoin, H. Happy, and G. Dambrine, Appl. Phys. Lett. 91, 153111 (2007).

N. Stuerzl, F. Hennrich, S. Lebedkin, and M. M. Kappes, J. Phys. Chem. C 113, 14628 (2009).

H. Liu, D. Nishide, T. Tanaka, and H. Kataura, Nat. Commun. 2, 309 (2011).

A. A. Green and M. C. Hersam, Advanced Materials 23, 2185 (2011).

F. Schwierz, Nat. Nanotechnol. 5, 487 (2010).
Supplementary Material

High-frequency performance of scaled carbon nanotube array field-effect transistors

Mathias Steiner\textsuperscript{1,a)}, Michael Engel\textsuperscript{2,3}, Yu-Ming Lin\textsuperscript{1}, Yanqing Wu\textsuperscript{1}, Keith Jenkins\textsuperscript{1}, Damon B. Farmer\textsuperscript{1}, Jefford J. Humes\textsuperscript{4}, Nathan L. Yoder\textsuperscript{4}, Jung-Woo T. Seo\textsuperscript{5}, Alexander A. Green\textsuperscript{5}, Mark C. Hersam\textsuperscript{5}, Ralph Krupke\textsuperscript{2,3,6}, and Phaedon Avouris\textsuperscript{1,b)"

\textsuperscript{1} IBM Thomas J. Watson Research Center, Yorktown Heights, New York 10598, USA

\textsuperscript{2} Institute of Nanotechnology, Karlsruhe Institute of Technology, 76021 Karlsruhe, Germany

\textsuperscript{3} DFG Center for Functional Nanostructures (CFN), 76028 Karlsruhe, Germany

\textsuperscript{4} NanoIntegris Inc., Skokie, IL 60077, USA

\textsuperscript{5} Department of Materials Science and Engineering and Department of Chemistry, Northwestern University, Evanston, IL 60208, USA

\textsuperscript{6} Institut für Materialwissenschaft, Technische Universität Darmstadt, 64287 Darmstadt, Germany

\textsuperscript{a) Electronic mail: msteine@us.ibm.com
\textsuperscript{b) Electronic mail: avouris@us.ibm.com}
**Electrical transport measurements**

The DC characterization of the semiconducting carbon nanotube (CNT) array transistors was performed in a probe station (LakeShore FWP6) under N\textsubscript{2} flow using a semiconductor parameter analyzer (Agilent B1500A Semiconductor Device Analyzer) and ground-signal-ground coplanar probes (GGB Industries). For high-frequency measurements the probe station was evacuated to a base pressure below 10\textsuperscript{-5} mTorr. The high-frequency performance of the transistors was obtained by measuring the scattering (S) parameters using a network analyzer (Agilent E8364C PNA Microwave Network Analyzer). DC voltages at the gate and drain contacts were applied through bias tees using the same semiconductor parameter analyzer.

The intrinsic high-frequency performance was obtained by using a de-embedding procedure based on “open” and “short” reference structures, similar to the method described in references S1 and S2. The “open” reference structure was identical to the active transistor except for the absence of CNTs in the device channel. The short circuit current gain $|h_{21}|$ was determined from the S parameters by using

$$h_{21} = \frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}}.$$  \hspace{1cm} (I)

The current gain cut-off frequency $f_T$ is defined as the frequency at which $|h_{21}|$ is equal to 0dB.
The maximum available power gain (MAG) was derived from the S parameters by using

\[ \text{MAG} = \left| \frac{S_{21}}{S_{12}} \left( K - \sqrt{K^2 - 1} \right) \right|. \]  

(II)

where \( K \) is the stability factor expressed by

\[ K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}S_{21}|} \quad \text{and} \quad \Delta = S_{11}S_{22} - S_{12}S_{21}. \]  

(III)

The unilateral power gain (U) was determined from the S parameters by using

\[ U = \frac{|S_{21} - 1|^2}{2K \left| \frac{S_{21}}{S_{12}} \right| - 2 \text{Re} \left( \frac{S_{21}}{S_{12}} \right)}. \]  

(IV)

Both MAG and U were converted into the dB-scale \((10 \cdot \log |\text{MAG}|)\). The maximum frequency of oscillation \( f_{\text{MAX}} \) is defined as the frequency at which U (MAG) equals 0dB.

References

S1 H. Cho and D. E. Burk, IEEE Trans. Electron. Dev. 38, 1371 (1991).

S2 M. C. A. M. Koolen, J. A. M. Geelen, and M. P. J. G. Versleijen, IEEE Proceedings of the 1991 Bipolar Circuits and Technology Meeting, 188 (1991).