Principle of constructing flat designs of electronic circuit diagrams considering forbidden figures

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Abstract. The problem of designing double-sided printed circuit boards in the form of synthesis of flat structures of electronic circuit diagrams at the design stage is considered. The aim of the work is to arrange the connections on two sides of the printed circuit board without jumpers, which facilitates the conditions for routes to any tracer of modern design programs. The main drawback of all the algorithms used is the principle of sequential and fragmented viewing of the commutation space incorporated in them. To solve this problem, it is necessary to use the graph theoretical method, rather than the topographic method, where priority is given to the metric aspect of the problem. The graph theoretical method involves preliminary stratification of the graph on two sides of the printed circuit board and analysis of the planarity of the graph circuit with subsequent elimination of jumpers, assigning a conflict link of the route to the back of the circuit board.

1. Introduction
Designing single-sided (SPCBs) or double-sided printed circuit boards (DPCBs) without jumpers is one of the most difficult tasks at the stage of structural design. The task in this formulation is especially relevant for onboard electronic circuit diagrams made with the help of surface mounting technology, where, for example, because of a metal heat sink or ceramic base, the structure of the compounds is possible in only one or two layers.

To solve it, many different algorithms [1] [2] [3] have been proposed, however, none of them can practically implement the tactics and strategies of a human developer. The main drawback of all the algorithms used is the principle of sequential and fragmented viewing of the commutation space incorporated in them. The complexity of the synthesis algorithms for such structures is also due to the need to consider a large number of different requirements related to the specifics of their manufacture and the features of the developed structural and technological solution.

2. The theoretical part
Let us consider the classic approach to the development of SPCBs and DPCBs, using electroradioelements (ERE)s with strict logic of functioning. Initially, a schematic electrical diagram is developed, and then a design is created by solving the problems of placing EREs and wiring on the assembly field. This approach has developed historically since each ERE outlet carries its own functional significance.
Based on the analysis carried out in [4], to solve this problem we will use the graph theoretical method, which involves graph planarizing for SPCB and graph stratifying into two sides for DPCB and a preliminary analysis of the graph planarity of the scheme with a subsequent elimination of intersections, assigning the conflicting track link to the reverse side of the printed circuit board.

The main task of creating the topology of ERE lead connection diagram is the need to arrange the connections on the plane without intersections, which facilitates wiring conditions for any tracer of modern design programs.

Among the graph planarity criteria, the most famous is the Pontryagin-Kuratovsky criterion [5].

The task of wiring of the outputs of elements in the circuit is to synthesize the circuit graph that does not contain subgraphs of homeomorphic $G_5$ or $G_{3,3}$.

In [4], a graph planarization algorithm is presented based on finding forbidden figures and transferring them from the forbidden class to the allowed class.

The main requirement for computer-aided design systems for flat designs of electronic circuits in the form of printed circuit boards with various number of layers is to provide 100% wiring efficiency, which is understood as the ratio of the number of realized connections on one layer to the total number of connections.

In this paper, it is proposed to design a DPCB with high efficiency of wiring by solving the problem of stratification of the initial graph diagram and constructing a flat graph diagram both on the ERE installation side and on the reverse side of the board — the solder side, excluding forbidden figures by the Potryagin–Kuratovsky theorem [5]. The stratification problem is the problem of coloring a graph in two colors, the solution of which is based on Koenig’s theorem, which defines a forbidden figure in the form of odd length cycles.

Let us consider the solution to the problem of stratification of the original graph-scheme’s edges on the two sides of the printed circuit board in the form of the problem of coloring the graph-scheme in two colors using the Kening theorem. A graph is two-color if and only if it does not contain cycles of odd length [4].

The algorithm for stratification of edges on two sides.

1. Search for forbidden figures (cycles of odd length).
2. Construction of the semantic table.
3. Finding the minimum coverage of table rows with columns. If all rows in the table are covered by at least one column, go to point 7. Otherwise, go to point 4.
4. Finding the components of the forbidden figure to bring the original model to an interpretable form.
5. Removing components from the source graph based on the semantic table of minimum coverage.
6. Transition to point 1.
7. The obtained minimum coverage is the optimum solution; removing these components (signatures) transfers forbidden figures to the allowed class, that is, forms a two-color graph.
8. The end of the algorithm.

Let us consider an example of converting the graph presented in Figure 1 into a two-color graph. Quality functional - minimum of removed edges.
Let us find all forbidden figures - these are cycles of odd length. We build a semantic table (Table 1), in which the rows reflect the forbidden figures, and the columns represent the components (edges) of these figures.

Table 1. Forbidden figures

| Z.F. | Edges | 12 | 13 | 15 | 16 | 25 | 28 | 34 | 36 | 38 | 46 | 57 | 78 |
|------|-------|----|----|----|----|----|----|----|----|----|----|----|----|
| 1251 |       | 1  | 1  |    |    |    |    |    |    |    |    |    |    |
| 1361 |       | 1  | 1  |    |    |    |    |    |    |    |    |    |    |
| 3463 |       | 1  | 1  | 1  |    |    |    |    |    |    |    |    |    |
| 138751 |     | 1  | 1  |    | 1  |    |    |    |    |    |    |    |    |
| 16387521 | | 1  | 1  | 1  | 1  |    |    |    |    |    |    |    |    |
| 283152 |       | 1  | 1  | 1  | 1  |    |    |    |    |    |    |    |    |
| 163821 |       | 1  | 1  | 1  | 1  | 1  |    |    |    |    |    |    |    |
| 16438751 | | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |    |    |    |    |

The minimum coverage of rows by the first table’s columns indicates which components of the forbidden figure should be changed when the original model is brought to an interpreted form. This component is edge 38. Removing this edge (Figure 2) leads to the beginning of the algorithm and the construction of the second table (Table 2). Similarly, to the first table, there is also a component with minimal column coverage of rows (edge 15). Removing this edge (Figure 3) leads to the beginning of the algorithm and the construction of the third table (Table 3). The minimum coverage in the last table (edge 36) leads to the optimum solution - a two-color graph (Figure 4).

Figure 2. Graph after component removal.

Thus, edges 38, 15, 36 translate forbidden figures (cycles of odd length) into the class of allowed ones, and the original graph into a two-color graph. This process is much less time consuming than the process of actual generation of all equivalent structures in the search for a minimum solution by known approaches [3].

When designing double-sided printed circuit boards, a methodology was developed for constructing planar graphs and stratifying the graph into two sides of the printed circuit board with a decrease in the number of unseparated edges.

Table 2. Forbidden figures (part 2)

| Z.F. | Edges | 12 | 13 | 15 | 16 | 25 | 28 | 34 | 36 | 38 | 46 | 57 | 78 |
|------|-------|----|----|----|----|----|----|----|----|----|----|----|----|
| 1251 |       | 1  | 1  | 1  |    |    |    |    |    |    |    |    |    |
| 1361 |       | 1  | 1  |    | 1  |    |    |    |    |    |    |    |    |
| 3463 |       | 1  | 1  | 1  |    |    |    |    |    |    |    |    |    |
| 157821 |     | 1  | 1  | 1  | 1  | 1  |    |    |    |    |    |    |    |
Figure 3. Initial graph after the next component removal.

Table 3 Forbidden figures (part 3)

| Edges   | 13 | 16 | 34 | 36 | 46 |
|---------|----|----|----|----|----|
| Z.F.    |    |    |    |    |    |
| 1361    | 1  | 1  | 1  |    |    |
| 3463    |    | 1  | 1  | 1  |    |

Figure 4. Resulting graph on the solder side.

Figure 5. Resulting graph from ERE installation side.

The main criterion for the effectiveness of constructing planar structures is 100% wiring between structural elements in one or more layers. Estimating the results of the synthesis of flat structures of electronic circuits constructed using the developed model and algorithm, we used the DipTrace and Altium Designer (P-CAD) modern software package with specialized software to conduct the wiring experiment. A comparative analysis of the presented wiring results (possibility of 100% wiring) of the applied CAE systems obtained ‘Before’ (without planarization) and ‘After’ (planarization) using the proposed planarization approach of the original graphs for designing flat structures of electronic circuits enables to increase the efficiency of wiring by an average of 2-5%.

3. Conclusions
When designing double-sided printed circuit boards, a methodology was developed for constructing planar graphs and stratifying the graph into two sides of the printed circuit board with a decrease in the number of unseparated edges.

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