Improvement of Electrical Performance in Heterostructure Junctionless TFET Based on Dual Material Gate

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Received: 1 November 2019; Accepted: 19 December 2019; Published: 23 December 2019

Abstract: In this paper, a dual metallic material gate heterostructure junctionless tunnel field-effect transistor (DMMG-HJLTFET) is proposed and investigated. We use the Si/SiGe heterostructure at the source/channel interface to improve the band to band tunneling (BTBT) rate, and introduce a sandwich stack (GaAs/Si/GaAs) at the drain region to suppress the OFF-state current and ambipolar current. Simultaneously, to further decrease ambipolar current, the gate electrode is divided into three parts namely auxiliary gate (M1), control gate (M2), and tunnel gate (M3) with workfunctions $\Phi_{M1}$, $\Phi_{M2}$ and $\Phi_{M3}$, respectively, where $\Phi_{M1} = \Phi_{M3} < \Phi_{M2}$. Simulation results indicate that DMMG-HJLTFET provides superior performance in terms of logic and analog/RF as compared with other possible combinations, the ON-state current of the DMMG-HJLTFET increases up to $9.04 \times 10^{-6}$ A/µm, and the maximum $g_{m}$ (which determine the analog performance of devices) of DMMG-HJLTFET is $1.11 \times 10^{-5}$ S/µm at 1.0 V drain-to-source voltage ($V_{ds}$). Meanwhile, RF performance of devices depends on the cut-off frequency ($f_{T}$) and gain bandwidth (GBW), and DMMG-HJLTFET could achieve a maximum $f_{T}$ of 5.84 GHz, and a maximum GBW of 0.39 GHz, respectively.

Keywords: gate material engineering; band-to-band tunneling (BTBT); a sandwich stack structure (GaAs/Si/GaAs); dual material gate heterostructure junctionless TFET (DMMG-HJLTFET)

1. Introduction

The mechanism of conventional metal oxide semiconductor field effect transistors (MOSFETs) is thermal electron emission, so the continuous scaling of conventional MOS device is extremely difficult in nanoscale circuit because of a great many reasons, such as, VDD scaling of MOSFETs is no longer viable, OFF-state current dramatically increases and short channel effects (SCE) is severely aggravated, and a limitation of 60 mV/Dec subthreshold swing (SS) can’t be broken [1,2]. In order to overcome these issues, different types of structure have been investigated in recent years, among them, tunnel field effect transistor (TFET) [3,4] is a selective candidate for future low power applications due to its complementary MOS (CMOS) process compatibility and scalability, which employs band-to-band mechanism and is not influenced by the short channel effect, moreover, it can break the SS limit of 60 mV/Dec, and the leakage current is small under the OFF-state condition [5–7]. However, there are also inherent disadvantages in TFETs, the most serious problems are small ON-state current and large miller capacitance. To address these issues, a lot of novel structures of TFETs are proposed [8–19]. As a whole, most of TFETs reported in recent years adopt different doping concentration in channel and active regions to form heavily doped abrupt junction at tunneling interface, which leads to a complex fabrication processes and a high thermal budget, what’s more,
introduction of high-density layer at source/channel junction and Gaussian doping in drain region also find difficulty during fabrication process and it’s easy to be influenced by random dopant fluctuations (RDFs) [20–23].

To avoid the above issues in TFETs, the junctionless tunneling field effect transistor (JLTFET) [24–30] is proposed, which uses a uniformly high-doping concentration in source, channel, and drain region, wherein the doping concentration and type of channel are consistent with source and drain. Therefore, junctionless tunnel field-effect transistor (JLTFET) is immune to random dopant fluctuations (RDFs) [31], while complex fabrication processes and high thermal budgets in JLTFET manufacturing can be effectively avoided by the charge plasma concept. Still, low ON-state current remains the problem in junctionless TFETs due to the presence of a barrier between source and channel. As we know, TFETs use a heavily doped source and a lightly doped channel to make the distance between the source valance band and the channel conduction band as short as possible, so that band to band tunneling from source valance band to channel conduction band will occur at source/channel interface, that is to say, a heavily doped degenerate source is required in TFETs to make the working mechanism of this structure change from hot electron emission to band to band tunneling. In this paper, different doping regions in the uniform doping device are achieved via the charge plasma concept. In this paper, a dual material gate heterostructure junctionless TFET (DMMG-HJLTFET) is proposed and investigated, in which we adopt a uniform doping concentration and a corresponding P⁺-N⁺-I-N⁺ structure can be realized via the charge plasma concept with appropriate work function for polar gate (PG) and control gate (CG). The PG is located at the source region and has a larger work function than CG for inducing a P⁺ source while CG is located at the middle for inducing intrinsic channel. We use Si/SiGe heterostructure at the source/channel interface to improve band to band tunneling (BTBT) rate. Meanwhile, a sandwich stack structure (GaAs/Si/GaAs) at the drain region is introduced to suppress the OFF-state current and ambipolar current. Moreover, based on the gate-engineered concept, the gate electrode is divided into three parts in DMMG-HJLTFET so that the ON-state current and the OFF-state current can be further improved. Si-based integrated circuits are most extensive in nowadays, so DMMG-HJLTFET using Si and SiGe as heterojunction at source/channel interface is proposed. And in order to match the current and performance with the DMGE-HJLTFET in [22], a sandwich stack structure (GaAs/Si/GaAs) in drain region is used in our new design. Through a comprehensive analysis, the DC and AC characteristics of this structure are comparable to DMGE-HJLTFET, and better than similar devices without gate engineering and sandwich structure, whose comparison will be shown in Table 2.

The details will be discussed in following sections: Section 2 describes the device structure and parameters. Section 3 includes the properties of the structure and the optimization process. Section 4 summarizes the article and makes some relevant statements.

2. Methods

Figure 1a shows the device structure of conventional JLTFET, in which the PG is located at the source region and has a larger work function than CG for inducing a P⁺ source while CG is located at the middle for inducing intrinsic channel, and a heavily doping is considered in silicon body with concentration of $1 \times 10^{19}$ cm⁻³, resulting in a junctionless P⁺-N⁺-I-N⁺ structure with appropriate workfunctions for PG and CG by charge plasma concept. Compared with conventional JLTFET, the difference of heterostructure junctionless tunnel field-effect transistor (HJLTFET) is that ON-state current can be improved by heterojunction at source/channel interface, as shown in Figure 1b. Based on conventional HJLTFET, DMMG-HJLTFET still uses Si/SiGe heterostructure at the source/channel interface and introduces a sandwich stack structure (GaAs/Si/GaAs) at drain region to suppress OFF-state current and ambipolar current, moreover, the gate electrode is divided into three parts namely auxiliary gate (M1), control gate (M2), and tunnel gate (M3) with workfunctions $\Phi_{M1}$, $\Phi_{M2}$ and $\Phi_{M3}$, respectively, where $\Phi_{M1} = \Phi_{M3} < \Phi_{M2}$, as shown in Figure 1c. As a result, the DMMG-HJLTFET has a larger ON-state current and lower OFF-state current than JLTFET and HJLTFET, so it is possible
to be applied to low power integrated circuit. Table 1 shows the fundamental geometrical parameters of the different devices.

![Cross-sectional view of (a) JLTFET; (b) HJLTFET; (c) DMMG-HJLTFET.](image)

**Table 1.** The fundamental geometrical parameters of the different devices.

| Parameter Name                  | JLTFET | HJLTFET | DMMG-HJLTFET |
|---------------------------------|--------|---------|--------------|
| Length of source (L_s/nm)       | 20     | 20      | 20           |
| Length of channel (L_ch/nm)     | 20     | 20      | 20           |
| Length of drain (L_d/nm)        | 20     | 20      | 20           |
| Length of gap (L_ga/nm)         | 5      | 5       | 5            |
| Thickness of SiO2 and HfO2 (T_OX/nm) | 2  | 2       | 2            |
| Thickness of the silicon body (T_si/nm) | 5  | 5       | 5            |
| Thickness of the Si (T_s/nm) in sandwich stack | 3  | 3       | 3            |
| Length of auxiliary gate (L_1/nm) | 7      |         |              |
| Length of control gate (L_2/nm) |        | 10      |              |
| Length of tunnel gate (L_3/nm)  |        | 3       |              |
| Work function of polarity gate (Φ_PG/eV) | 5.9 | 5.9     | 5.9          |
| Work function of control gate (Φ_CC/eV) | 4.6 | 4.6    | 4.6          |
| Work function of auxiliary gate (Φ_M1/eV) | 4.1 |         | 4.1          |
| Work function of tunnel gate (Φ_M3/eV) |         |         | 4.1          |
| N-type doping concentration (N_C/cm^{-3}) | 1 × 10^{19} | 1 × 10^{19} | 1 × 10^{19} |

All the simulations are carried out in Silvaco Atlas 5.20.2.R [32–35]. The nonlocal BTBT model (BBT.NONLOCAL) is used to take into account the spatial variation of the energy bands and the nonlocal generation of electrons and holes. Because of the presence of highly doped channel, Shockley-Read-Hall related to concentration (CONSRH) is used for accounting the minority carrier recombination effects, at the same time, Fermi Statistics (FERMI) and band gap narrowing (BGN) model are also activated to reduce the carrier concentration in the simulation. Moreover, quantum confinement effects due to the increased doping levels and thinner gate oxide in the channel distinctly influence the device...
characteristics, so quantum confinement model given by Hansch (HANSCHQM) is also considered in our simulation. Furthermore, tunneling of electrons from the valence band to the conduction band through trap or defect states and phonon assisted tunneling effects of indirect band gap semiconductors can have an important effect on the current, in order to involve these effects, the Schenk model for trap Assisted tunneling (SCHENK.TUNN) and band to band tunneling model given by Schenk (SCHENK.BBT) are also included.

3. Results and Discussion

3.1. The Operating Mechanism of DMMG-HJLTFET

A basic analytical formulation for band to band tunneling probability \( T(E) \) is shown in Equation (1):

\[
T(E) \propto \left(-\frac{4 \sqrt{2m^*E_g^2}}{3|\hbar|E_g + \Delta\Phi}\right) \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}}} \Delta\Phi
\]

where \( m^* \) is the effective carrier mass, \( E_g \) is the bandgap, \( \Delta\Phi \) is the energy range over which tunneling can take place, and \( t_{ox}, t_{si}, \varepsilon_{ox}, \varepsilon_{si} \) are the oxide and silicon film thickness and dielectric constants, respectively. As can be seen from the above formulation that small \( m^* \) and small \( E_g \) in source region is required in the source region, and appropriate materials need to be selected in source/channel interface to ensure the appropriate \( \Delta\Phi \).

Based on theoretical analysis, we propose a dual material gate heterostructure junctionless TFET (DMMG-HJLTFET) in this paper.

The physical mechanism of DMMG-HJLTFET is explained in Figures 2a–d and 3a,b. Figure 2a,b shows the BTBT rate of electron and hole of DMMG-HJLTFET when \( V_{ds} = 1 \text{ V} \). It is obvious that BTBT occurs at source and channel interface, and the rate of BTBT increases significantly due to heterojunction between source and channel. Figure 2c shows the electric field distribution when \( V_{gs} = 2.0 \text{ V} \) and \( V_{ds} = 1.0 \text{ V} \), it is not difficult to find that the value of electric field is markedly improved near heterojunction between source and channel interface. Figure 2d shows the total current density of DMMG-HJLTFET when \( V_{gs} = 2.0 \text{ V} \) and \( V_{ds} = 1.0 \text{ V} \), as can be seen from the Figure 2d, the current mainly flows in the middle region of this device, introducing the sandwich stack structure (GaAs/Si/GaAs) for DMMG-HJLTFET not only guarantees the large ON-state current, but also guarantees the small OFF-state current, which benefits from combining the advantages of silicon and GaAs.
Figure 2. (a) Nonlocal band to band tunneling (BTBT) rate of electron; (b) nonlocal band to band tunneling (BTBT) rate of hole; (c) electric field distribution in DMMG-HJLTFET; (d) total current density of DMMG-HJLTFET.

Figure 3. (a) The energy band diagram of JLTFET, HJLTFET and DMMG-HJLTFET at the device surface region; (b) The energy band diagram of DMMG-HJLTFET at the device middle region.

The comparative analysis among devices JLTFET, HJLTFET and DMMG-HJLTFET for the energy band diagram at the device surface is shown in Figure 3a. From observing this figure, it is not difficult to find that the conduction band and valance band of HJLTFET and DMMG-HJLTFET in the tunneling region are very close to each other, resulting in the tunneling distance of both devices being much smaller than that of JLTFET, this is because both devices employ germanium as their source and a heterojunction is introduced at the channel/source interface, which leads to the tunneling possibilities and ON-state current of HJLTFET and DMMG-HJLTFET being much larger than that of JLTFET. Moreover, the difference in DMMG-HJLTFET is that the gate electrode is divided into three parts namely auxiliary gate (M1), control gate (M2), and tunnel gate (M3), with workfunctions Φ_{M1}, Φ_{M2} and Φ_{M3}, which further improves the tunneling possibilities at channel/source interface and produces an extra barrier height at channel/drain interface in DMMG-HJLTFET. Together with sandwich stack structure (GaAs/Si/GaAs), divided gate electrode obviously increases the ON-state current and decreases the OFF-state current of DMMG-HJLTFET. Figure 3b shows the energy band diagram of JLTFET, HJLTFET and DMMG-HJLTFET at the middle region of the device, as can be seen from this figure, the variation of energy band of source region at the middle is similar to Figure 3a, however, variation of energy band of channel and drain region is very different to Figure 3a. The reason for this is that the extra barrier introduced by divided gate electrode only exists in the surface region of DMMG-HJLTFET.

3.2. The Input Characteristics

The log scale and linear scale transfer characteristics of JLTFET, HJLTFET and DMMG-HJLTFET are illustrated in Figure 4a. It is very clear that DMMG-HJLTFET can generate a higher current
than HJLTFET and JLTFT, the ON-state current of DMMG-HJLTFET is $1.01 \times 10^{-5}$ A/\(\mu\)m when \(V_{GS} = 2.0\) V and \(V_{DS} = 1.0\) V, however, the corresponding ON-state currents of JLTFT and HJLTFET are only $3.82 \times 10^{-6}$ A/\(\mu\)m and $7.21 \times 10^{-7}$ A/\(\mu\)m, respectively. Moreover, the OFF-state current of DMMG-HJLTFET is much smaller than that of JLTFT and HJLTFET due to a sandwich stack structure (GaAs/Si/GaAs) is introduced at the drain region, which ensures a small OFF-state current in DMMG-HJLTFET on account of large forbidden band width of GaAs.

The transconductance \((g_m)\) is an important parameter to evaluate the analog performance of devices. It can be calculated by first derivative of drain current \((I_{ds})\) with respect to \(V_{GS}\), Equation (2) is the formula of \(g_m\):

\[
g_m = \frac{dI_{ds}}{dV_{GS}} \tag{2}
\]

Figure 4b shows the transconductance characteristics of JLTFT, HJLTFET and DMMG-HJLTFET. Transconductance of DMMG-HJLTFET increases observably compared with JLTFT and HJLTFET. The maximum transconductance of DMMG-HJLTFET is $1.26 \times 10^{-5}$ S/\(\mu\)m, while the maximum transconductance of JLTFT and HJLTFET are $1.22 \times 10^{-6}$ S/\(\mu\)m and $5.76 \times 10^{-6}$ S/\(\mu\)m.

Including Figure 4a, b, a comparison of the three devices is presented in Table 2. According to Table 2, the value of \(I_{on}/I_{off}\) ratio of DMMG-HJLTFET can be reached at $1.56 \times 10^{13}$, while the \(I_{on}/I_{off}\) ratio of JLTFT and HJLTFET are only $5.3 \times 10^{8}$ and $1.34 \times 10^{9}$, respectively. Moreover, average subthreshold swing(SS) of DMMG-HJLTFET is $52 \text{ mV/Dec}$ extracted from \(V_{min}\) to \(V_t\) (\(V_{min}\) is the gate voltage at which drain current equals to Ioff, the gate voltage at which the drain current becomes $1 \times 10^{8}$ A/\(\mu\)m is taken as the threshold voltage \(V_t\)) under \(V_{DS} = 1.0\) V.

|                      | \(I_{on}\) (A/\(\mu\)m) | \(I_{off}\) (A/\(\mu\)m) | \(I_{on}/I_{off}\) | \(g_m\) (S/\(\mu\)m) | SS (mV/Dec) |
|----------------------|-------------------------|--------------------------|-------------------|-------------------|-------------|
| JLTFT                | $7.21 \times 10^{-2}$   | $1.36 \times 10^{-15}$   | $5.3 \times 10^{8}$ | $1.22 \times 10^{-6}$ | 122         |
| HJLTFET              | $3.82 \times 10^{-6}$   | $2.84 \times 10^{-15}$   | $1.34 \times 10^{9}$ | $5.76 \times 10^{-6}$ | 88.2        |
| DMMG-HJLTFET         | $1.01 \times 10^{-5}$   | $6.5 \times 10^{-19}$    | $1.56 \times 10^{13}$ | $1.26 \times 10^{-5}$ | 52          |

3.3. The Output Characteristics

Figure 5a indicates the output characteristics of JLTFT, HJLTFET and DMMG-HJLTFET at \(V_{GS} = 1\) V, it can be seen clearly that JLTFT shows worse saturation performance under this simulation condition, meanwhile, the maximum ON-state current of JLTFT is only $2.35 \times 10^{-10}$ A/\(\mu\)m. While HJLTFET and DMMG-HJLTFET have better saturation performance, and the maximum ON-state currents of HJLTFET and DMMG-HJLTFET are $3.01 \times 10^{-8}$ A/\(\mu\)m and $8.32 \times 10^{-7}$ A/\(\mu\)m, respectively.
when channel doping concentration increases from 1 \times 10^{18} \text{ cm}^{-3} to 1 \times 10^{19} \text{ cm}^{-3}.

Moreover, the ON-state current of DMMG-HJLTFT increases while the OFF-state current of DMMG-HJLTFT always remains at the order of 10^{-13} \text{ A/} \mu\text{m}, as a result, the ratio of Ion/Ioff keeps at level of 10^{13} with increase of channel doping concentration as shown in inserted small figure at Figure 6b. Therefore, channel doping concentration is selected as 1 \times 10^{19} \text{ cm}^{-3} in order to obtain a maximal ON-state current.

The output transconductance ($g_{ds}$) is also an important parameter to evaluate the analog performance of devices, and it can be calculated by Equation (3):

$$g_{ds} = \frac{dI_{ds}}{dV_{DS}}$$

(3)

Figure 5b shows the output conductance ($g_{ds}$) characteristics of JLTFET, HJLTFT and DMMG-HJLTFT at $V_{gs} = 1$ V. As can be seen from the Figure 5b, output conductance of DMMG-HJLTFT is greater than that of JLTFET and HJLTFT from 0.2 V to 1.0 V $V_{ds}$, and maximum output conductance of DMMG-HJLTFT is 1.99 \times 10^{-6} \text{ S/} \mu\text{m} when $V_{ds} = 0.74$ V. However, the maximum output conductance of JLTFET is 1.73 \times 10^{-6} \text{ S/} \mu\text{m} when $V_{ds} = 0.6$ V, and the maximum output conductance of HJLTFT is 9.86 \times 10^{-8} \text{ S/} \mu\text{m} when $V_{ds} = 0.52$ V.

### 3.4. Effect of Device Sizes on the Transfer Characteristics

Figure 6a shows the impact of channel doping concentration on transfer characteristics. As shown in this figure, the ON-state current of DMMG-HJLTFT stays at the order of 10^{-6} \text{ A/} \mu\text{m} at $V_{ds} = 2$ V when channel doping concentration increases from 1 \times 10^{18} \text{ cm}^{-3} to 1 \times 10^{19} \text{ cm}^{-3}.

Moreover, the ON-state current of DMMG-HJLTFT increases while the OFF-state current of DMMG-HJLTFT always remains at the order of 10^{-18} \text{ A/} \mu\text{m}, as a result, the ratio of Ion/Ioff keeps at level of 10^{13} with increase of channel doping concentration as shown in inserted small figure at Figure 6b. Therefore, channel doping concentration is selected as 1 \times 10^{19} \text{ cm}^{-3} in order to obtain a maximal ON-state current.

Figure 7a shows the impact of polar gate work function ($\Phi_{PC}$) on transfer characteristics with keeping $\Phi_{M1} = \Phi_{M3} = 4.1$ eV and keeping $\Phi_{M2} = 4.6$ eV. As can be seen clearly from the Figure 7a appropriate selection of polar gate work function is required to achieve higher ON-state current, the
appropriate selection of polar gate work function is required to obtain higher ratio of electric field and band diagram with keeping... ΦM2=3.8eV

Electric Field (V/cm)
Distance (nm)
source channel drain

Figure 7. (a) Simulated log scale and linear scale transfer characteristics of DMMG-HJLTFT with different polar gate work function (ΦPG); (b) the variation of energy band with different polar gate work function (ΦPG).

We mentioned above that the gate electrode is divided into three parts namely auxiliary gate (M1), control gate (M2), and tunnel gate (M3) with work functions ΦM1, ΦM2 and ΦM3, respectively, where ΦM1 = ΦM3 < ΦM2.

Figure 8a–d shows the impact of control gate work function (ΦM2) on transfer characteristics, electric field and band diagram with keeping ΦM1 = ΦM3 = 4.1 eV and ΦPG = 5.9 eV. As depicted in Figure 8a, the selection of control gate work function is very important to obtain higher ratio of Ion/Ioff, the ON-state current and the OFF-state current of DMMG-HJLTFT decrease with the increase of control gate work function. The variation of electric field is shown in Figure 8b, it is very clear that value of electric field in channel region increases with the decrease of control gate work function, which makes the surface potential under control gate increase and the energy band bend severely in this region, as shown in Figure 8c,d shows the energy band diagram in OFF-state, where it is observed that tunneling barrier height increases with the increase of control gate work function in the channel region. As a result, the overall performance of the DMMG-HJLTFT is significantly affected by the control gate work function, and the optimal value of the control gate work function is chosen as 4.6 eV.

Figure 7. Cont.
Figure 8. (a) Simulated log scale and linear scale transfer characteristics of DMMG-HJLTFT with different control gate work function ($\Phi_{M2}$); (b) the distribution of electric field at the surface with different control gate work function ($\Phi_{M2}$); (c) the variation of ON-state energy band with different control gate work function ($\Phi_{M2}$); (d) the variation of OFF-state energy band with different control gate work function ($\Phi_{M2}$).

Figure 9a–d shows the impact of auxiliary gate work function ($\Phi_{M1}$) and tunnel gate work function ($\Phi_{M3}$) on transfer characteristics, surface potential, electric field and band diagram with keeping $\Phi_{M2} = 4.6$ eV and $\Phi_{PC} = 5.9$ eV. It can be found through the observation of Figure 9a that the ON-state current of DMMG-HJLTFT decreases and the OFF-state current of DMMG-HJLTFT increases with the increase of auxiliary gate work function, i.e., appropriate selection for auxiliary gate work function should be small in terms of ON-state current. At the same time, the surface potential and electric field are also markedly influenced by auxiliary gate work function, as shown in Figure 9b,c, it can be notified that the DMMG-HJLTFT exhibits higher surface potential and electric field at the position of M1 and M3 with small auxiliary gate work function, which helps M1 suppress the ambipolar leakage current and reduce hot carrier effects (HCEs) by diminishing lateral electric field at drain/channel interface together with SiO2 near the drain and helps M3 improve the ON-state current by increasing the tunneling probability at source/channel interface, as a result, a higher tunneling rate at the source/channel interface and higher barrier height at drain/channel interface are introduced simultaneously, as shown in Figure 9d. So, auxiliary gate work function should be small in terms of ON-state current and OFF-state current, and the auxiliary gate work function should be large in terms of barrier height at drain/channel interface. All things considered, the optimal value of auxiliary gate work function is chosen as 4.1 eV.
As we know, the frequency characteristics of the integrated circuits is profoundly affected by parasitic capacitances of devices, so it is very necessary to research the capacitance of DMMG-HJLTFET. Apparently, the characteristics of $C_{gg}$ (gate capacitance), $C_{gs}$ (capacitance of gate to source), and $C_{gd}$ (capacitance of gate to drain) are of great significance to evaluate the frequency performance of DMMG-HJLTFET. Meanwhile, the ON-state current of DMMG-HJLTFET increases visibly when $T_S$ varies from 4 nm to 1 nm, the reason is that thickness of GaAs in sandwich stack structure $(GaAs/Si/GaAs)$ increases from 0.5 nm to 3 nm when $T_S$ decreases from 4 nm to 1 nm, which improves the electric field distribution at the surface of DMMG-HJLTFET, as shown in Figure 10b. It is not difficult to find that electric field of channel region increases and electric field of drain region decreases when $T_S$ increases from 1 nm to 4 nm, which enhances the lateral electric field at drain/channel interface and improves the tunneling probability at source/channel interface. The reason for the improvement of the ON-state current and electric field distribution in Figure 10a,b is that GaAs is a direct bandgap semiconductor while Si is an indirect bandgap semiconductor, the bandgap width of GaAs is larger than that of Si, and the electron mobility of GaAs is much higher than that of Si.

3.5. Performance Comparison in Terms of Analog/RF Figure of Merits

Figure 10a shows the impact of the thickness of silicon ($T_S$) in a sandwich stack structure $(GaAs/Si/GaAs)$ on transfer characteristics. It can be seen clearly from the Figure 10a, the ON-state current of DMMG-HJLTFET is minimal when $T_S = 5$ nm, this is because DMMG-HJLTFET is converted into HJLTFET when $T_S = 5$ nm, the current level of this condition is consistent with HJLTFET mentioned previous section. Meanwhile, the ON-state current of DMMG-HJLTFET increases visibly when $T_S$ varies from 4 nm to 1 nm, the reason is that thickness of GaAs in sandwich stack structure $(GaAs/Si/GaAs)$ increases from 0.5 nm to 3 nm when $T_S$ decreases from 4 nm to 1 nm, which improves the electric field distribution at the surface of DMMG-HJLTFET, as shown in Figure 10b. It is not difficult to find that electric field of channel region increases and electric field of drain region decreases when $T_S$ increases from 1 nm to 4 nm, which enhances the lateral electric field at drain/channel interface and improves the tunneling probability at source/channel interface. The reason for the improvement of the ON-state current and electric field distribution in Figure 10a,b is that GaAs is a direct bandgap semiconductor while Si is an indirect bandgap semiconductor, the bandgap width of GaAs is larger than that of Si, and the electron mobility of GaAs is much higher than that of Si.
Cgd (capacitance of gate to drain) are of great significance to evaluate the frequency characteristics and analog application ability of devices. Figure 11a–c show the capacitance of JLTFET, HJLTFT and DM-HJLTF versus Vgs under Vds = 1 V. In Figure 11a–c, the trend of the capacitance curve versus Vgs is similar, Cgs is very small in three devices due to the existence of polar gate which separates control gate electrode far from source electrode and, as a result, the coupling of control gate electrode and source electrode is relatively slight, so the curve of Cgg and Cgd is highly coincident, and Cgg is mainly determined by Cgd. Figure 11d shows the comparison of Cgg of JLTFET, HJLTFT and DMMG-HJLTFT, Cgg of JLTFET and HJLTFT remain at a small value when Vgs < Vds and increase rapidly with the increasing Vgs when Vgs > Vds, as shown in Figure 11d, while Cgg of DMMG-HJLTFT remains at a small value when Vgs < 0.5 Vds and increases rapidly with the increasing Vgs when Vgs > 0.5 Vds on account of divided gate electrode, moreover, Cgg of DMMG-HJLTFT is much less than that of JLTFET and HJLTFT due to the hetero dielectric adopted under the control gate.

Based on the above capacitance changes, we discuss the cut-off frequency (fT) and gain bandwidth (GBW). Both of them are the important evaluation indicators for RF performance, and as shown in Equation (4), cut-off frequency (fT) can be expressed as ratio of gm to Cgg [36]:

\[
f_T = \frac{g_m}{2\pi C_{gs} \sqrt{1 + \frac{2 C_{gd}}{C_{gs}}}} \approx \frac{g_m}{2\pi (C_{gs} + C_{gd})} = \frac{g_m}{2\pi C_{gs}}
\]

(4)

The GBW can be expressed as a ratio of \(g_m\) to \(C_{gd}\) for the DC gain value equal to 10, as shown in Equation (5) [37,38]:

\[
\text{GBW} = \frac{g_m}{2\pi 10 C_{gd}}
\]

(5)
Figure 12a,b shows the characteristic curves of the $f_T$ and GBW of JLTFET, HJLTFT and DMMG-HJLTFT. Further, benefiting from large transconductance induced by structural innovation, the DMMG-HJLTFT could achieve a maximum $f_T$ of 9.17 GHz at $V_{gs} = 1.4$ V, and a maximum GBW of 0.17 GHz at $V_{gs} = 1.2$ V, respectively. However, maximum $f_T$ of JLTFET and HJLTFT are only 1.01 GHz at $V_{gs} = 2.0$ V and 3.74 GHz at $V_{gs} = 1.6$ V, and maximum GBW of JLTFET and HJLTFT are only 0.005 GHz and 0.09 GHz at $V_{gs} = 1.1$ V.

**Figure 12.** (a) The cut-off frequency ($f_T$) characteristic curves of JLTFET, HJLTFT and DMMG-HJLTFT; (b) the gain bandwidth (GBW) characteristic curves of JLTFET, HJLTFT and DMMG-HJLTFT.

4. Conclusions

In this paper, a dual material gate heterostructure junctionless TFET(DMMG-HJLTFT) is constructed and researched to improve the performance of JLTFET and HJLTFT. To enhance the on-state current and suppress the OFF-state current, Si/SiGe heterostructure at the source/channel interface and sandwich stack structure (GaAs/Si/GaAs) at drain region are introduced. Simultaneously, based on the gate engineered concept, the corresponding electrode is divided into three parts to further increase the tunneling barrier width at the drain/channel interface and the tunneling probabilities at source/channel interface. In our work, the effects of the device sizes, doping concentration and work function on the performance of the DMMG-HJLTFT are researched systematically to optimize the overall device performance. Simulation results indicate that DMMG-HJLTFT provides superior performance in terms of logic and analog/RF performance as compared with JLTFET and HJLTFT, the ON-state current of DMMG-HJLTFT increases up to $1.01 \times 10^{-5}$ A/μm, and the maximum $g_m$ of DMMG-HJLTFT is $1.26 \times 10^{-5}$ S/μm at $V_{ds} = 1.0$ V, meanwhile, DMMG-HJLTFT could achieve a maximum $f_T$ of 9.17 GHz at $V_{gs} = 1.4$ V and a maximum GBW of 0.17 GHz at $V_{gs} = 1.2$ V, respectively. So, DMMG-HJLTFT may be one of the alternative devices for the next generation of low power applications.

**Author Contributions:** Conceptualization, H.L., T.H., W.L., S.C., S.W., and H.X.; methodology, H.X. and T.H.; software, H.X. and W.L.; validation, H.L., and H.X.; formal analysis, H.X.; investigation, H.X.; resources, H.X; data curation, H.X.; writing—original draft preparation, H.X.; writing—review and editing, H.X.; visualization, H.X.; supervision, H.X.; project administration, H.L.; funding acquisition, H.L. All authors have read and agreed to the published version of the manuscript.

**Funding:** This research was funded by National Natural Science Foundation of China (Grant No. U1866212) and in part by Foundation for Fundamental Research of China (Grant No. JSZL2016110B003) and Major Fundamental Research Program of Shaanxi (Grant No. 2017ZDJC-26) and Innovation Foundation of Radiation Application (Grant No. KFZC2018040206).

**Conflicts of Interest:** The authors declare no conflict of interest.

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