Simulation of Gate Leakage Current of AlGaN/GaN HEMTs: Effects of the Gate Edges and Self-Heating

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The gate leakage current ($I_{G}$) of AlGaN/GaN high electron mobility transistors (HEMTs) at various ambient temperatures is simulated by considering its mechanism as domination of trap-assisted tunneling (TAT) and Poole-Frenkel (PF) emission for low electric field in the AlGaN barrier, and domination of Fowler–Nordheim (FN) tunneling for high electric field in the AlGaN barrier. Two bias cases are studied: $V_{GS}$ (gate voltage) variation while $V_{DS}$ (drain voltage) is constant with $V_{GS} = 0$ V with self-heating. For the first case, FN tunneling current mainly concentrates near the gate edges and so it is not changed with the gate length. While PF emission and TAT current do not show big variation along the gate, they are affected by the gate length and show higher values for longer gate. For the second case, with $V_{DS}$ increasing the elevated device temperature caused by self-heating obviously increases PF emission and also increases $I_{G}$ because PF emission is the dominant mechanism of $I_{G}$. With $V_{DS}$ further increasing, although the higher device temperature presents, $I_{G}$ is not affected by the self-heating because the temperature-independent FN tunneling becomes the dominant mechanism of $I_{G}$.

The AlGaN surface has negative piezoelectric and spontaneous polarization charge, while the AlGaN/GaN interface has correspondent positive charge. Large amount of donor-like traps concurrently exist on the AlGaN surface and the 2DEG in the channel comes from ionization of the donor-like traps. The AlGaN surface negative charge is partially or even completely neutralized by positive charge from ionization of the donor-like traps. For the case that the AlGaN surface negative charge is partially neutralized, nonzero electric field should present in the AlGaN barrier which should lead to nonzero leakage current from the channel to the gate. To make total zero leakage current when $V_{GS}$ and $V_{DS}$ equal to zero, forward current from the gate to the channel namely trap-assisted tunneling current ($J_{TAT}$) was proposed, which has form similar to the thermionic emission and can be expressed as

$$J_{TAT} = J_0 \exp \left[ \frac{\left( q (V_{GS} - V_0) \right)}{\eta k T} - 1 \right] \tag{1}$$

where $J_0$, $V_0$, and $\eta$ are parameters used to fit the experimental data, and $q$ is the fundamental electronic charge, $k$ is Boltzmann constant, and $T$ is temperature. As aforementioned statement, $J_{TAT}$ is considered in RLEF. For the first studied case of high $V_{GS}$ ($V_{GS} = 0$ V), $V_{GS}$ is approximated as constant along the gate and so Equation 1 can be directly used. For the second studied case of low $V_{DS}$ ($V_{DS} = 0$ V), $V_{DS}$ along the gate is not a constant and so more derivations are needed. Because of low value of $V_{DS}$, it can be approximated as linearly distributes in the channel between the source and drain contact, i.e., the electric field is constant in the channel. Therefore, the potential difference between any position of the gate contact and the source contact ($V_{Gx}$) can be expressed as $V_{Gx} = -V_{DS} (L_{SG} + L_{LG} + L_{LG} + L_{GD})$, where $L_{SG}$, $L_{LG}$, and $L_{GD}$ represent the distance of source-gate contact, gate length, and distance of gate-drain contact, respectively. $L_{LG}$ is a variable denoting the position along the gate. $L_{SG} = 0$ and $L_{GD} = L_G$ denote the position of source-side and drain-side gate edge, respectively. Then $V_{Gx}$ in Equation 1 should be replaced as $V_{Gx} = V_{GS}$. As a result, $J_{TAT}$ does not uniformly distribute along the gate.
PF emission means the electron emission from the trap also by thermal activation but with a lowered trap depth induced by the coulomb interaction, i.e., the emission rate is enhanced by the electric field. The current density \( J_{PF} \) induced by the PF emission is expressed as

\[
J_{PF} = C_{PF} E \exp \left[ -\frac{q(\phi_b - \sqrt{E/\pi \varepsilon_s})}{kT} \right],
\]  

where \( C_{PF} \) is a constant, \( E \) is the electric field across the barrier, \( \phi_b \) is the barrier height for the electron emission from the trap state, \( \varepsilon_s \) is the permittivity of vacuum, and \( \varepsilon \) is the relative permittivity of AlGaN at high frequencies. Equation 2 can be rearranged as

\[
\ln(J_{PF}/E) = m(T)\sqrt{E} + b(T),
\]

where

\[
m(T) = \frac{q}{kT} \sqrt{\frac{q}{\pi \varepsilon_s}},
\]
\[
c(T) = -\frac{q\phi_b}{kT} + \ln(C_{PF}).
\]

From Equation 3 \( \ln(J_{PF}/E) \) should be a linear function of \( \sqrt{E} \), and \( \varepsilon_s \) as well as \( \phi_b \) can be extracted from \( m(T) \) and \( c(T) \). For the gate contact with large area, the leakage current near the gate edges is negligible. \( J_{PF} \) can be calculated as \( J_{PF}(A) \) (PF is the leakage current caused by PF emission and \( A \) is the gate contact area), then the above approach can be adopted to extract \( \varepsilon_s \) as well as \( \phi_b \). But for the devices studied in this paper, the leakage current near the gate edges is significant so that \( J_{PF} \) cannot be simply calculated as \( J_{PF}(A) \) and therefore \( \varepsilon_s \) as well as \( \phi_b \) cannot be extracted by the above approach.

For AlGaN/GaN HEMTs, FN tunneling means the electron in the gate metal tunnels through a triangular barrier to the AlGaN conduction band, expressed as

\[
J_{FN} = A E^2 \exp \left( -\frac{8\pi\sqrt{2m_s(q\phi_b)}}{3q\hbar E} \right),
\]

where \( A \) is a constant, \( m_s \) is the effective electron mass, \( \phi_b \) is the Schottky barrier height, and \( h \) is Planck constant. At last, as aforementioned illustration, \( J_G \) is constituted by \( J_{ITAT}, J_{PF}, \) and \( J_{FN} \), and it is calculated as

\[
J_G = J_{ITAT} + J_{PF} + J_{FN}
\]

Note that the leakage current \( I_G \), \( I_{ITAT}, I_{PF}, \) and \( I_{FN} \) are integral of the leakage current density \( J_G \), \( J_{ITAT}, J_{PF}, \) and \( J_{FN} \) along the gate metal/AlGaN interface, respectively.

In principle, direction of \( E \) should be vertical to the gate metal/AlGaN interface and \( E \) should be constant across the AlGaN barrier in the expressions of \( J_{ITAT} \) and \( J_{FN} \). The following approximations are adopted in our simulations. Although in the barrier near the gate edges significant horizontal component of electric field \( E_x \) is presented, it is much lower than the vertical component \( E_z \). In the other areas of the barrier, \( E_z \) is negligible. Especially, if the gate metal and AlGaN are considered as ideal metal and ideal dielectric, respectively, then the boundary conditions of Poisson equation determine that \( E \) at the gate metal/AlGaN interface has only \( E_z \) but no \( E_x \), i.e., the direction of \( E \) is vertical to the interface. Therefore, \( E \) can be replaced by \( E_z \) for calculations of \( J_{ITAT} \) and \( J_{FN} \). As stated before, \( J_{ITAT} \) is considered in RLEF, in which \( E \), across the AlGaN barrier can be approximated as constant. So \( E \), at the gate metal/AlGaN interface is used for \( J_{ITAT} \) calculation. \( J_{FN} \) is considered in RHEF and it mainly concentrates near the gate edges (see more illustrations in the next section) where \( E \) does not keep constant. However, considering the tunneling barrier near the gate edges is very thin due to the relative high value of \( E_z \), it can be approximated as triangular barrier and then \( E \), can be calculated as \( \phi_b/L \), where \( L \) is the thickness of the tunneling barrier (see Figure 1).

\( E \) (replaced by \( E_z \) and \( T \) (the lattice temperature) needed for calculations of \( J_{ITAT}, J_{PF}, \) and \( J_{FN} \) are obtained by numerical simulations with the FEM software COMSOL, in which the traditional semiconductor equations including Poisson equation, current continuity equation, and thermal conduction equation are simultaneously solved by numerical method. Details of the equations and solving procedure can be found in Refs. 13 and 14. The self-heating effect is included in the simulation for the device under \( V_{DS} > 0 \) (\( V_{GS} = 0 \) V) and it is influenced by the device power consumption. \( T \) is determined by the device self-heating and ambient temperature. Calculations of \( J_{ITAT}, J_{PF}, \) and \( J_{FN} \) do not address the electron temperature and so here the hot electron effect is not considered.

The devices studied have epitaxial layers of 22 nm Al_{0.29}Ga_{0.71}N barrier and 1.4 µm GaN buffer grown on 400 µm 4H-SiC substrate by metal-organic chemical vapor deposition. Inductive coupled plasma etch was performed for electrical isolation. Ohmic contacts and gate electrode were formed of Ti/Al/Ni/Au (20/120/40/80 nm) and Ni/Al (20/200 nm) layers by E-beam evaporation, respectively. A 100 nm Si, N_x passivation layer was deposited by plasma enhanced chemical vapor deposition. The studied two devices have geometries of

\[
egin{align*}
L_{GD} & = 2.2 \mu m, \quad L_{G} = 0.7 \text{ and } 3 \mu m, \quad L_{GD} = 4.7 \mu m, \text{ and two fingers with each } 50 \mu m \\
\end{align*}
\]

results under vacuum conditions at different ambient temperatures by HP/Agilent 4156C semiconductor parameter analyzer and a Janis probe station.

Results and Discussion

Figure 3 shows simulated \( I_G, I_{ITAT}, I_{PF}, \) and \( I_{FN} \) as a function of \( V_{GS} \) (\( V_{DS} = 0 \) V) at the ambient temperatures of 350 K (Figure 3a) and 500 K (Figure 3b). Experimental \( I_G \) is also shown for a comparison. In the simulations, the reasonable parameters of \( \varepsilon_s = 10, \ m_s = 0.222 \ m_0, \ \phi_b = 0.6 \ eV, \) and \( \phi_F = 1.2 \ eV \) were selected. \( \phi_t = 0.6 \) eV is higher than the value of 0.3 eV reported in Ref. 1. This difference would be explained that the continuum of states formed by the dislocations may be influenced by the material properties and the device processing, which therefore may lead to uncertainty of \( \phi_b \) for different devices. As shown in Figure 3a, with \( V_{GS} \) decreasing from 0 to around −4.5 V the temperature-dependent \( I_{ITAT} \) and \( I_{PF} \) dominate \( I_G \), and this
is the reason that higher ambient temperature leads to higher \( I_G \) (Figure 3b). With \( V_{GS} \) further decreasing to \(-6 \) V, temperature-independent \( I_{FN} \) becomes the dominant component of \( I_G \). As a result, \( I_G \) will not affected by the ambient temperature. In order to deeply analyze the mechanism of \( I_G \), the distribution of \( E_y \) (Figure 3c), \( J_{TFAT} \), \( J_{PF} \), and \( J_{FN} \) (Figure 3d) along the gate metal/AlGaN interface from source- to drain-contact for \( V_{GS} = -3 \) V and \(-6 \) V are solely shown. \( E_y \) near the gate edges continuously increases with \( V_{GS} \) deceasing, while \( E_y \) in the other areas of the interface saturates after \( V_{GS} \) lower than the threshold voltage, which is a result from the depletion of 2DEG in the channel. Correspondingly, \( J_{PF} \) and \( J_{FN} \) show higher values near the gate edges than that in other areas. \( J_{FN} \) is very sensitive to \( E_y \), and so it shows pronounced variation along the interface. For \( V_{GS} = -3 \) V, \( J_{PF} \) along the whole interface is higher than \( J_{FN} \) and so \( I_{PF} \) is the dominant component of \( I_G \). For \( V_{GS} = -6 \) V, \( J_{FN} \) becomes higher than \( J_{PF} \) near the gate edges, as a result \( J_{FN} \) becomes the dominant component of \( I_G \).

The saturate \( E_y \) far from the gate edges is not high enough to cause obvious \( I_{FN} \), meaning \( I_{FN} \) mainly concentrates near the gate edges.

To investigate how \( I_G \) is influenced by \( L_G \), \( I_G \) for another device with \( L_G = 3 \) \( \mu \)m is also simulated and compared with \( L_G = 0.7 \) \( \mu \)m. Under the same \( V_{GS} \), \( E_y \) (Figure 4b) and also \( J_{PF} \) as well as \( J_{FN} \) (Figure 4c) have almost same distributions along the gate metal/AlGaN interface for different \( L_G \). Although the same distributions of \( J_{PF} \), \( I_{PF} \) shows higher value for \( L_G = 3 \) um than that for \( L_G = 0.7 \) um because of the larger gate area for longer \( L_G \) (Figure 4a). However, due to the concentration of \( J_{FN} \) near the gate edges, \( I_{FN} \) have same values for the different \( L_G \). Therefore, for the high \( V_{GS} \), device with longer \( L_G \) should have higher \( I_G \) because \( J_{TFAT} \) and \( J_{PF} \) are the dominant components of \( I_G \). While for low \( V_{GS} \), \( I_G \) should be \( L_G \)-independent because \( I_{FN} \) becomes the dominant component of \( I_G \).

We have studied \( I_G \) for the device under \( V_{GS} < 0 \) V (\( V_{GS} = 0 \) V) without self-heating. In the following, \( I_G \) for the device under \( V_{DS} > 0 \) V (\( V_{GS} = 0 \) V) with self-heating will be studied. \( J_{TFAT} \) is temperature-independent and \( I_{TFAT} \) is considered only for low \( V_{DS} \) to which the self-heating is negligible. So only the simulated \( I_{TFAT} \) with and without self-heating are compared as shown in the Figures 5a and 5b. For \( 5 \) V < \( V_{DS} < 15 \) V, the elevated device temperature exhibiting the maximum value at the drain-side gate edge (Figure 5c) caused by the self-heating significantly increases \( I_{PF} \) and also \( I_G \) since \( I_{PF} \) is the dominant component of \( I_G \). This increase of \( I_G \) is more obvious for

**Figure 3.** Simulated \( I_G \), \( I_{TFAT} \), \( I_{PF} \), and \( I_{FN} \) variation with \( V_{GS} \) (\( V_{DS} = 0 \) V) at the ambient temperatures of 350 K (a) and 500 K (b), and simulated distributions of \( E_y \) (c), \( J_{PF} \), and \( J_{FN} \) (d) along the gate metal/AlGaN interface from the source- to drain- side at the ambient temperature of 350 K for the device with \( L_G = 0.7 \) \( \mu \)m. Experimental \( I_G \) is also shown for a comparison. Because \( J_{TFAT} \) is considered only for high \( V_{GS} \), it is not shown in (d) for low \( V_{GS} = -3 \) V and \(-6 \) V.

**Figure 4.** Simulated \( I_G \), \( I_{TFAT} \), \( I_{PF} \), and \( I_{FN} \) variation with \( V_{GS} \) (\( V_{DS} = 0 \) V) (a), and simulated distributions of \( E_y \) (b), \( J_{PF} \), and \( J_{FN} \) (c) along the gate metal/AlGaN interface from the source- to drain- side at the ambient temperature of 500 K for the device with \( L_G = 0.7 \) and 3 \( \mu \)m. Note that some curves are overlapped and they are distinguished by solid lines (\( L_G = 3 \) \( \mu \)m) and dash lines (\( L_G = 0.7 \) \( \mu \)m) for all of the graphs. Experimental \( I_G \) (red circle) in (a) for \( L_G = 3 \) \( \mu \)m is also shown for a comparison.
the device at low ambient temperature of 350 K. The SiC substrate of the studied device has high thermal conductivity. For the other two common Si and sapphire substrates having lower thermal conductivity compared to SiC, impact of the device self-heating on $I_G$ should be more significant. For $V_{DS} > 15$ V, although stronger self-heating is presented, but it has no effect on $I_G$ because $I_{FN}$ becomes the dominant component of $I_G$. Figure 5d shows the distributions of $J_{PP}$ and $J_{FN}$ near the gate metal/AlGaN interface. Due to the pinch-off of the drain current, $E_y$ near the drain-side gate edge is much higher than that in other areas of the interface. Similar to the aforementioned illustration, for the high $V_{DS} = 20$ V $J_{FN}$ is higher than $J_{PP}$ near the drain-side gate edge and it mainly concentrates there.

In the following, we will illustrate that the simulations of $I_G$ are consistent with the reported experimental work about the increased $I_G$ for the degraded device. Mizuno et al.\textsuperscript{15} illustrated that the plasma treatment before gate metal evaporation can reduce the positive charge locates in the vicinity of the AlGaN surface, meaning the electric field near the gate is reduced which therefore reduces the gate tunneling current. The increased $I_G$ for the degraded device could be attributed to two main aspects: one aspect is that the hot electrons can trigger traps in the device illustrated by Meneghesso et al.,\textsuperscript{16} this effect is more obvious especially for the device operation in semi-on state in which the hot electrons have both high energy and high density; another aspect is that, when the device operation under high $V_{DS}$ and low $V_{GS}$ with high electric field appearing at the drain-side gate edge, because of the piezoelectric property of AlGaN/GaN, high inverse piezoelectric stress may cause pits/cracks (mechanical failure) at the drain-side gate edge where large amount of traps should locate.\textsuperscript{17} Overall, the device degradation regarding to the increase of $I_G$ was attributed to the increased traps caused by the hot electrons and pits/cracks. In our work, TAT, PF emission, and FN tunneling are considered for the simulations of $I_G$. It is straight that increased traps should enhance the traps-based TAT and PF emission current. Additionally, increased traps can deplete the 2DEG in the channel and thus increases the electric field in the barrier, which finally increases TAT, PF emission, and also FN tunneling current. Therefore, our simulations of $I_G$ are consistent with the reported experimental results.

Conclusions

$I_G$ of AlGaN/GaN HEMTs considered as summation of $I_{TAT}$, $I_{PF}$, and $I_{FN}$ is simulated and compared to the experimental data. The TAT and PF emission are dominant mechanisms for low electric field in the AlGaN barrier, while FN tunneling is the dominant mechanism for high electric field in the AlGaN barrier. $I_{TAT}$ and $I_{PF}$ can be influenced by $E_y$, while $I_{FN}$ is $E_y$-independent due to the concentration of $I_{FN}$ near the gate edges. For the device at small values of $V_{DS} > 0$ V ($V_{GS} = 0$ V) with obvious power consumption, the self-heating can significantly increases $I_{PF}$ and also $I_G$ because $I_{PF}$ is the dominant component of $I_G$. While for the device under high $V_{DS}$, the self-heating has no influence on $I_G$ because temperature-independent $I_{FN}$ becomes the dominant component of $I_G$.

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Figure 5. Simulated $I_G$, $I_{TAT}$, $I_{PF}$, and $I_{FN}$ variation with $V_{DS}$ ($V_{GS} = 0$ V) at the ambient temperatures of 350 K (a) and 500 K (b), and simulated distributions of $E_y$ (left axis in (c)) and the maximum device temperature (right axis in (c)), $J_{PF}$, and $J_{FN}$ (d) along the gate metal/AlGaN interface from the source- to drain-side for the device with $L_G = 0.7$ μm. The simulations of temperature-dependent $I_{PF}$ with and without self-heating are compared in (b). Because temperature-dependent $I_{TAT}$ is considered only for low $V_{DS}$ (the self-heating is negligible), simulations of $I_{TAT}$ with and without self-heating are not compared in (b).
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