Influence of wet etching in KOH on defects in silicon nanowires formed by cryogenic dry etching

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Abstract. The work is devoted to exploration of arrays of vertical aligned silicon nanowires (SiNWs) obtained by cryogenic dry etching in ICP mode with height of 4.5–5.5 μm and aspect ratio of 7. It was shown that geometry of nanowires has crucial influence on rate of wet etching in KOH since it is higher for 3D objects than for planar wafer, and the diameter should be the same along the nanowire for controlled wet etching. Wet etching in 4% KOH solution during 30 s allowed to save array of uniformity vertical aligned SiNWs with height of 4 μm and diameter of 500 nm. Such treatment reduced concentration of defects detected by deep-level transient spectroscopy, particularly, it drops as minimum in two times for deep level with $E_a=0.68-0.74$ eV placed near to surface of wafer.

1. Introduction
Nowadays, there is movement from classical planar solar cells to structures with layers of low dimension, which allow to vary the geometry and electronic properties of the materials. For example, vertically aligned silicon nanostructures (nanowires, nanorods) can enhance the absorption of solar radiation and can be used for fabrication of double-junction since it allows the use of cheap silicon wafers and technologies of the silicon industry as the most developed in micro- and nanoelectronics. Recently, it was experimentally demonstrated for microcrystalline silicon solar cells grown on silicon nanowires (SiNWs) [1,2]. However, its effective development is hampered by the imperfection of the applied technologies like metal-assisted chemical etching of silicon wafer or vapour-liquid-crystal for the fabrication of nanowires due to defect formation from trace of metal catalysts [3–5]. Recently, SiNWs are formed by new method of dry etching of silicon wafer in inductively-coupled plasma (ICP) at cryogenic temperature [6]. Unlike classical reactive ion etching (RIE) this method led only to partially amorphisation of thin surface layer without degradation of bulk properties in silicon wafer [7]. However, influence of cryogenic etching process on properties of SiNWs were not studied in details unlike planar wafer. Therefore, this work is devoted to exploration defect formation in array of SiNWs by capacitance methods, and research of post-etch treatment to suppress it.

2. Experimental details
Firstly, layer of SiO₂ 400 nm thick was deposited by chemical vapour deposition on (100) silicon wafer (2–7 Ω·cm) using Oxford Plasma Lab System 100 setup. Then wafers were covered by latex spheres with 1 μm diameter using spin-coater. Further, spheres size was decreased by dry etching in oxygen plasma in Oxford Plasma Lab ICP 380 setup, layers of SiO₂ was dry etched in atmosphere of CHF₃ in
RIE mode down to wafer to form SiO\(_2\) mask resisting to cryogenic etching. Finally, wafers was dry etched in mixture of SF\(_6\)/O\(_2\) in ICP mode at -140 °C during 3.5 and 4.5 minutes. SEM images of fabricated structures are presented in figure 1. In result, we obtained uniform array of SiNWs with diameter of 700 nm and height of 4.5 μm for 3.5 min etch, and with 600 nm and 5.5 μm, respectively, for 4.5 min of etching. Note that the SiO\(_2\) layer was not etched and practically did not decrease, which confirms its resistance to cryogenic etching and it is suitable for use as a mask. However, diameter of SiNWs decreases in their upper part, especially, it is noticeably for sample with higher etching time where it leads to appearance of inverted pyramids, and their shape is like an hourglass. Such behavior change geometry of nanowires, and it can complicate next operations as wet etching, deposition of layers or metals etc. Then, all samples were cleared in HF solution to remove remnants of spheres and SiO\(_2\) layer.

The morphology of wafer with array of SiNWs were characterized by using scanning electron microscopy (SEM) (SUPRA 25 Zeiss). Metal contacts were evaporated in BOC Edwards Auto500 setup for fabrication of structures with Schottky barrier for further electrophysical measurements. Standard I–V curves were measured using a Keithley 2400 source-meter. Capacitance-voltage characteristics were performed using a precision E4980A Keysight (former Agilent) LCR-meter at 100 kHz at 300 K. Capacitance deep-level transient spectroscopy were done using an automated installation based on a Boonton-7200B capacitance bridge in the temperature range of 80-360 K to study interface in different area of wafers and its defect properties [8].

![Figure 1. SEM images of arrays of silicon nanowires obtained by cryogenic etching during 3.5 min (a) and 4.5 min (b).](image-url)

### 3. Results and discussion

As noted before, defects appear in surface layer of 50 nm thick after dry cryogenic etching due to plasma influence, but it was also showed that wet etching in KOH leads to recovery of lifetimes in silicon wafer [7]. Furthermore, post-KOH dipping is used an effective method to improve properties of SiNWs fabricated by MACE [9,10]. Here, the sample after dry etching of 4.5 minutes was taken to explore influence of wet etching on geometry of SiNW’s array. SEM images for different etching conditions are presented in figure 2. Firstly, the sample was etched at conditions equal to experiments with planar wafer: in 20% KOH solution during 60 s (see figure 2a). In result, wafer relief significantly changed: SiNWs became very thin and almost disappeared, and surface was covered by pyramids that is not unacceptable for further double-junction solar cell fabrication. For this reason, 4% KOH was used to slow down the chemical reaction, and also sample was etched during 30 s, 60 s and 180 s. The etching during 30 s allowed to save structure of SiNWs arrays, but their form is changed: height decreased down to 2-3 μm, and upper part became rough and spiky (see figure 2b). Subsequent increase to 60 s led to further destruction of nanowires (diameter and height reduction), and after 180 s they are totally etched (see figure 2d).
Figure 2. SEM images of arrays of silicon nanowires obtained by cryogenic etching during 4.5 min, after wet etching in 20% KOH during 60 s and in 4% KOH during 30 s (b), 60 s (c) and 180 s (d).

Therefore, sample with array of SiNWs obtained after dry etching during 3.5 minutes (see figure 1a) was wet etched in 4% KOH during 30 s, and its SEM images are presented in figure 3. In result, relief of SiNW’s array and their geometry was much better saved than in previous sample, but their height and diameter decreased to 4 μm and 500 nm, respectively. Consequently, rate etch is strongly depend on geometry of sample: it is higher for 3D objects than for planar one, and variation of shape uniformity leads to acceleration of etching. It acts in total side surface, and when NWs have shape as hourglass the area with the smallest diameter is etched firstly leading to their break, the top surface becomes like peak, and cylindrical geometry is lost. So parameters optimization of dry etching should be focused on ideal geometry of SiNWs since it has crucial influence on wet etching. Nevertheless, suggested treatment in 4% during 30 s allowed to etch possible defective surface and save array of SiNWs so below its influence on defects was studied below for sample obtained by dry etching during 3.5 minutes.
Figure 3. SEM images of array of silicon nanowires obtained by cryogenic etching during 3.5 min after wet etching in 4% KOH during 30 s.

Then, ohmic contact was formed to bottom side of wafer by plasma-enhanced atomic layer deposition of highly n-doped GaP layer 20 nm thick [11,12] with subsequent deposition of indium. Further, Schottky barrier was formed to SiNWs by evaporation of gold through mask with holes with a diameter of 0.5 mm. SEM image of sample after wet etching and Schottky barrier formation are presented in figure 4. As shown, metal fully covered side and top surfaces of NWs and area on the bottom between them so it allowed to explore whole surface of wafer obtained by cryogenic etching.

Figure 4. SEM images of array of silicon nanowires obtained by cryogenic etching during 3.5 min without (a) and with (b) wet etching in KOH with evaporated gold.

Measurements of current-voltage characteristics for both samples show classical view for Schottky diode: exponential behavior at forward bias voltages and constant low current at reverse ones, even it is lower for wet etched sample (see figure 5a). Further, capacitance-voltage characteristics were obtained at 100 kHz and 300 K (see figure 5b), and profile of concentration of free charge carriers were estimated (in inset). Curves are almost the same at all range, and concentration ($N_{CV}=1\times10^{15}$ cm$^{-3}$) exactly corresponds to the doping concentration of the silicon wafer (2-7 Ω·cm). Due to low concentration, NWs are depleted even at zero voltage since gold cover total side surface and its diameter is less 700 nm. Therefore, space charge region penetrates inside the bulk wafer at reverse bias voltage so defect characterization inside SiNWs or in interface Au/n-Si can be reached only by applying of forward bias voltage allowing to flatten bands and fill defect levels in this regions.
Figure 5. Current-voltage (a) and capacitance-voltage characteristics (b) of sample with array of SiNWs. In inset – concentration profiling.

In this case, DLTS measurements were carefully performed at the following conditions: $V_{\text{ini}}= 0 \, \text{V}$, $V_{\text{pulse}}=+2 \, \text{V}$, $t_{\text{pulse}}=50 \, \text{ms}$ to explore possible defects near to interface Au/n-Si. Nevertheless, technique was also applied to explore defects in the depth of wafer at the following conditions: $V_{\text{ini}}= -4 \, \text{V}$, $V_{\text{pulse}}=+4 \, \text{V}$, $t_{\text{pulse}}=50 \, \text{ms}$. DLTS spectra for rate window of $20 \, \text{s}^{-1}$ obtained for both modes are shown in figure 6.

![Figure 6](image)

Figure 6. DLTS spectra for rate window of $20 \, \text{s}^{-1}$ for initial (a) and etched (b) in KOH samples for different modes.

Firstly, when reverse bias voltage is applied there is only one high-temperature peak related to defect level with abnormally high activation energy, but its concentration lower than $1 \times 10^{12} \, \text{cm}^{-3}$, and its response almost disappeared in sample after KOH etching. Secondly, for mode with forward bias voltage during the filling pulse, there is series high peak in range of 240-360 K that corresponds to response from defect level with an activation energy $E_a=0.68-0.74 \, \text{eV}$, capture-cross section of $\sigma_T=1 \times 10^{-15} \, \text{cm}^2$ and concentration $N_T=2 \times 10^{12} \, \text{cm}^{-3}$ estimated from equation for point-like defect, but due to broadened peak on curve more realistic case is extended defects near surface of silicon. However, after etching in KOH amplitude of peak dropped in two times so defect concentration also decreased as minimum in two times. Therefore, additional wet etching in 4% KOH solution during 30 s led to lower defect concentration in array of SiNWs obtained by cryogenic etching.

4. Conclusion

In result, arrays of vertical aligned silicon nanowires (SiNWs) obtained by cryogenic dry etching in ICP mode with height of 4.5-5.5 μm and aspect ratio of 7 were explored. It was shown that geometry of nanowires has crucial influence on rate of wet etching in KOH since it is higher for 3D objects than for planar wafer, and the diameter should be the same along the nanowire for controlled wet etching. Wet etching in 4% KOH solution during 30 s allow to save array of uniformity vertical aligned SiNWs with height of 4 μm and diameter of 500 nm. Such treatment reduced concentration of defects, particularly, it drops as minimum in two times for deep level with $E_a=0.68-0.74 \, \text{eV}$ placed near to surface of wafer.

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