Abstract—Present-day quantum computers suffer from various noises or errors such as, gate error, relaxation, dephasing, readout error, and crosstalk. Besides, they offer a limited number of qubits with restrictive connectivity. Therefore, quantum programs running these computers face resilience issues and low output fidelities. The noise in the cloud-based access of quantum computers also introduce new modes of security and privacy issues. Furthermore, quantum computers face several threat models from insider and outsider adversaries including input tampering, program misallocation, fault injection, Reverse Engineering (RE) and Cloning. This paper provides an overview of various assets embedded in quantum computers and programs, vulnerabilities and attack models and the relation between resilience and security. We also cover countermeasures against the reliability and security issues and present future outlook for security of quantum computing.

Index Terms—Quantum Computing, Security, Privacy, Resilience, Fault Injection, Reverse Engineering.

I. INTRODUCTION

Quantum computing is a paradigm-shifting technology that can revolutionize fields like drug discovery, chemistry [1], machine learning [2], and optimization. Quantum computing is evolving rapidly from a theoretical concept to the experimental demonstration of quantum advantage [3]. Various vendors like IBM [4], Amazon [5], and Microsoft [6] are offering cloud-based access to physical quantum computers. Several physical hardware are being developed by IBM, Pasqal, Rigetti, Xandau and Google. Software packages such as, Qiskit, Cirq, Orqesstra, and Forest are also available to design, optimize, and execute quantum algorithms. With progress on hardware and software, quantum computing is poised to meet the scalability requirements to solve practical size problems.

The work is supported by National Science Foundation (NSF) (CNS-1722557, CCF-1718474, OIA-2040667, DGE-1723687 and DGE-1821766) and seed grants from Penn State Institute for Computational and Data Sciences (ICDS) and Huck Institute of the Life Sciences.

We acknowledge the use of IBM Quantum services for this work. The views expressed are those of the authors, and do not reflect the official policy or position of IBM or the IBM Quantum team.

However, present-day quantum computers suffer from several challenges which include a small number of qubits, restrictive connectivity, and limited native instructions. Besides, the qubits are error-prone and have short lifetimes. Quantum circuits are affected by these errors and generate low-quality outputs. Therefore, noise-resilient methods are of paramount importance. These devices are often termed as noisy intermediate-scale quantum (NISQ) computers [7]. Apart from engineering better qubits, several other independent approaches like parameter optimization in variational algorithms, noise-aware mapping, and scheduling are pursued to make quantum programs resilient to noise. For example, parameterized quantum circuits (PQCs) are proposed for variational algorithms and machine learning [8]–[10]. Resilience of a variational algorithm, namely, quantum approximate optimization algorithm (QAOA) under noise, and compilation techniques to achieve better resilience have been studied in [11]–[15]. The resiliency of various quantum factoring algorithms have been investigated in [16]. A hybrid quantum-classical approach is proposed [17] to counteract noise in NISQ based true random number generator. The above approaches achieve noise resiliency through parameter optimization. Besides parameter optimization, various software techniques like mapping and scheduling are being explored that aim to minimize the number of SWAPs for communication [18], allocation of gates to less noisy qubits [19]–[21], reducing crosstalk through intelligent scheduling [22], or blend outputs of different mappings to sanitize errors [23]. In general, the methods try to improve the performance of quantum algorithms by mitigating numerous errors.

In addition to resilience issues, NISQ devices and the cloud model of quantum computing can be susceptible to many security and privacy challenges. For example, quantum circuits can be treated as intellectual properties (IP). An untrusted software chain or server can steal data and computation and cause undue loss to users. Besides, hardware architectures.
with 1000 qubits are projected in less than 5-years. Such scale makes multi-tenant computing [24] lucrative in quantum clouds as it can increase device utilization and commercial gains. However, multi-tenant access to quantum hardware can lead to fault injection [25] and data-leakage attacks [26]. Moreover, malicious entities at the cloud-end can allocate inferior hardware and/or report incorrect error rates. Running on inferior devices or qubits can lead to low program fidelity.

In this paper, we (i) review various challenges and security vulnerabilities in NISQ computers; (ii) review various resilience techniques proposed in the literature to mitigate errors; and (iii) discuss attack models, countermeasures, and security opportunities relevant to NISQ architectures.

In the remaining of the paper: Section II presents the challenges and security vulnerabilities present in devices. Section III describes attack models demonstrated in NISQ devices. Section IV reviews various error mitigation methods for noise resilient performance. Section V presents several countermeasures to thwart attacks. Section VI describes security opportunity in terms of true random number generator (TRNG). Section VII presents the future outlook on resilience and security of quantum computers. Finally, Section VIII draws conclusion.

II. CHALLENGES AND VULNERABILITIES

A. Qubit lifetime and errors

Quantum bits or qubits on NISQ devices suffer from a short lifetime and erroneous gate and measurement operations. A short qubit lifetime entails a spontaneous loss of qubit state (saved data) which is called decoherence. For example, a qubit in state $|1\rangle$ interacts with the environment, spontaneously loses energy, and ends up with state $|0\rangle$. This phenomenon is known as relaxation. Another qubit lifetime issue is dephasing where a qubit state loses its phase information. Relaxation and dephasing are quantified by gate error rate and measurement error rate, respectively.

Moreover, crosstalk errors can be present in the device due to which two parallel gate operations can experience increased gate error. In [27], the authors presented multiple sources of classical crosstalk that can be present in Transmon-based quantum computers such as, traditional electromagnetic (EM) crosstalk between microwave lines, stray on-chip EM fields, etc. On a high level, the signal intended to control one qubit can disturb another independent qubit. For example, in [28] the authors demonstrate one such case where control fields (magnetic flux) used to operate qubits affect unaddressed qubits. The work in [29] reported that including crosstalk in quantum circuit simulation could lead to more accurate results. It establishes crosstalk as a prevailing source of error in NISQ devices. Finally, all the errors (decoherence, gate error, measurement error, and crosstalk) show temporal variation.

B. Limited native gates

A quantum program or circuit can be constructed with any high-level quantum gate (any reversible gate can be a quantum gate). However, the NISQ devices support only a few native gates. For example, there are 4 single-qubit gates (‘id’, ‘rz’, ‘sx’, and ‘x’) and only 1 two-qubit gate (‘cx’) in IBM machines. Any high-level gate is decomposed to the native gates of the hardware. The decomposition step increases the number of gate counts and run-time of the circuit. Increased gate count and run-time adversely affect circuit performance due to short qubit lifetime and gate error.

C. Coupling constraint

NISQ devices, especially quantum computers based on superconducting qubits, have limited connectivity between qubits known as coupling constraint. The limited connectivity prevents 2 qubit gates between any two arbitrary qubits. A compiler needs to add additional SWAP operations to satisfy the coupling constraint. Fig. 2a shows the coupling graph of an IBM quantum computer where we cannot perform a CNOT (CX) gate directly between Q1 and Q4 as they are not connected. One option is to swap Q1 and Q2 so that the data of Q1 moves to Q2. Now, the CX can be applied between Q2 and Q4 as they are connected. A SWAP operation
D. Cloud-based access

Quantum computing is far from becoming a personal commodity due to cost and needs for ultra-cold temperature [30], [31], shielded environment, and complex wiring for control. Therefore, cloud-based access to quantum computers is the logical path forward where the hardware is hosted in a remote location. In addition to hardware, high-performance quantum simulators also need cloud offerings as personal computers can hit memory limit while simulating a reasonably large circuit.

Quantum computing in the cloud is growing at a tremendous rate in the past few years. IBM is providing free access to its quantum processors and simulators through the cloud (IBM Quantum Experience). Rigetti, another quantum computing vendor, started a similar service named Quantum Cloud Service or QCS (which is now retired and moved to AWS Braket and Azure Quantum). Companies such as, Microsoft, Google, Amazon, D-Wave, Xanadu, IonQ, etc. are also providing various services for quantum computing in the cloud.

With cloud offering being the only option, various security and privacy issues can emerge. For example, a malicious entity on the cloud-end can assign an inferior hardware [32] or report incorrect error-rates [33] (discussed in Section 11 as “scheduler attacks”). Besides, a rogue element in the cloud can steal the structure and/or the output of a quantum program which can be intellectual properties (IPs). For example, a company can invest substantial time and money to design a quantum algorithm to solve a difficult problem (e.g., drug discovery). These make it lucrative for an adversary to observe the submitted quantum programs and steal information.

E. Problem encoding

The construction of a quantum circuit can reveal sensitive information about the problem. We discuss one such vulnerability using a combinatorial problem MaxCut which involves dividing a graph into two parts so that the maximum number of edges is cut. Such problems can be formulated using the spin-glass/Ising model. Fig. 2 (right) shows the quantum approximate optimization algorithm (QAOA) circuit for the problem graph in Fig. 2 (left). Here, each edge in the graph is represented by a CNOT-rotation-CNOT gate in the circuit. Therefore, one can infer the problem graph just by looking at the circuit. Besides MaxCut, many Quadratic Unconstrained Binary Optimization (QUBO) problems fall under this category.

F. Need for untrusted compilers

One of the important aspects of quantum circuit compilation is to optimize the circuit for improved circuit depth and reduced gate count. Several 3rd party compilers are evolving that offer optimization at faster compilation time even for large quantum circuits [18], [34]. The following factors will motivate the quantum circuit designers to avail the untrusted 3rd party compilation services: (a) success of quantum circuit since the optimized circuit is essential to obtain meaningful results from NISQ computers. A poorly optimized circuit will produce random outputs even if it is functionally identical; (b) lack of trusted compilers that have caught up with the latest advancements in optimization; (c) availability of efficient but untrusted 3rd party compilers [18], [24], [34] that are being developed to optimize depth and gate count compared to trusted compilers. These compilers can be hosted on either the local machines by the 3rd party or on the cloud service providers to launch, (i) cloning-counterfeiting, where the quantum circuit can be stolen or reproduced; and (ii) Reverse Engineering (RE), where the sensitive aspects of the quantum circuit could be extracted.

G. Application oriented vulnerabilities: quantum machine learning

Quantum machine learning (QML) is an emerging field that aims to develop quantum algorithms to perform conventional generative/discriminative machine learning tasks (e.g., classification, regression, etc.) [2], [9], [10], [35]. An extremely high-dimensional classical data can be loaded into a few qubits using methods like amplitude encoding [36]. For example, 2^n classical features can be encoded as the amplitudes of different basis states in an n-qubit system. Therefore, QML has been explored with to provide an advantage over the existing

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**Fig. 2:** (a) The coupling map of ibmq_5_yorktown. (b) A SWAP gate is inserted to satisfy coupling constraint as Q1 and Q4 are not connected.

**Fig. 3:** (left) An example graph for MaxCut (right) QAOA circuit for finding MaxCut of the graph on the left.
Recent research on QML has uncovered several performance bottlenecks. The work in [37] revealed that the training landscape in parameterized quantum circuits might have vanishing gradients. These locations of vanishing gradients are referred to as barren plateaus in the literature. Once stuck in a barren plateau, gradient-based optimization methods (e.g., stochastic gradient descent) may not be able to move further to train the network. In [38], the authors showed that quantum-noise could also induce barren plateaus in the PQC training landscape. In [39], the authors demonstrated that the temporal variation in quantum-noise can affect the reliability of a quantum classifier. In [40], the authors demonstrated that a small amount of perturbation in the input data is enough to induce misclassification in a trained quantum classifier. As the required perturbation scales inversely with the dimension, a small perturbation is sufficient to induce misclassification in high-dimensional quantum classifiers. An adversary can exploit these performance bottlenecks or vulnerabilities to attack QML applications. Several attacks have been demonstrated already in recent academic studies [25, 41].

III. ATTACK MODELS

A. Security attacks

1) Crosstalk induced fault injection: Crosstalk error can be exploited to launch fault-injection attacks in a multi-tenant computing (MTC) environment where two or more quantum programs may run simultaneously on a different set of physical qubits. MTC is economically enticing as it maximizes hardware resource usage and profit. Fault-injection in the computation process may have substantial socio-economical significance. For example, a deterministic fault in the weather forecast or optimal power grid topology calculation can provide undue financial/political advantage to the adversary. The attack model from [25] assumes that the adversary can run his/her program in the same hardware as one or more victim programs. A conceptual diagram is given in Fig. 4. They assume that the adversary, (i) will know the public information e.g., coupling map of the hardware; (ii) may also be aware of the crosstalk values between various qubits by running crosstalk characterization experiments such as, idle tomography and simultaneous randomized benchmarking on the qubits before the attack. The authors demonstrated the attack using both simulation and experiments. They picked a 3-qubit Grover search as the victim program and repeated CNOT drive as the adversary program. The results, collected from ibmq_5_yorktown (ibmqx2) a Canary processor, (Fig. 5) show that the correct output probability of the Grover search falls drastically (i.e., becomes indistinguishable) after a certain number of CNOTs in the adversary circuit.

2) Scheduler attacks: Quantum circuits are sent to quantum hardware via a cloud-based provider which allocates the hardware for the circuit. Here, the user has no visibility on the hardware that is being allocated. In [32], the authors propose a new attack model where the user is allocated an inferior quantum hardware instead of the desired one. Moreover, even if the desired quantum hardware is allocated, the scheduling policy for the queue of quantum circuits is another aspect that should be taken into consideration. The queue of quantum programs on the cloud side is usually long, with the main goal of maximizing throughput for cost reduction and better scientific exploration. The scheduling policy of the hardware is usually provided by the vendor for program allocation to hardware. In Fig. 6, two users U1 and U2 request for hardware A which is better compared to hardware B in terms of characteristics like error rates and fidelity. First U1 sends the request to the cloud service, and cloud service allocates hardware A to U1. However, when U2 requests for hardware B, the cloud service could make U2 either wait or allocate hardware B, which is of inferior quality. If the latter happens, U2 will suffer from incorrect results due to inferior hardware and may also end up paying more.

A variant of the scheduler attack is discussed in [33] where the scheduler allocates the requested device however, a rogue employee in the quantum computing company can be the attacker. He/she can alter the reported error-rate data so that an inferior qubit (with a larger error rate) is reported as a superior qubit (with a smaller error rate). When a user requests or a compiler allocates physical qubits, they (user or compiler) can unknowingly select inferior quality qubits to run the circuit. Therefore, the user circuit will experience heightened errors and sub-optimal output. The authors state that the success of the attack depends on the variation of the error rates of
the underlying hardware and the failure model applied to determine the mapping policy. An attack can be triggered if there is a significant variation in the qubit error rates.

3) Attacks on QML: Similar to the attack models on classical ML algorithms, attacks on QML can be categorized from three dimensions- (i) timing i.e., if the attack take place during training or inference; (ii) information i.e., the type of information that is available to the attacker e.g., knowledge of the internals of the QML model/algorithm (white-box attacks) or access to the inputs/outputs of the QML model only (black-box attacks); and (iii) goals i.e., the objectives of the attacker e.g., force misclassification for certain inputs (targeted attacks) or affect the overall reliability of a model (non-targeted attacks).

In [25], the authors demonstrated a non-targeted/reliability attack where an attacker induces noise to a victim’s quantum classifier (during inference) through crosstalk in a MTC environment. It increased the misclassification rate of the classifier significantly. In [41], the authors demonstrated ways to generate adversarial samples for a QML image classifier (noisy inputs that are misclassified by the classifier) in both white-box and black-box setup. The additional noise acted as a unitary that modifies the input state to the classifier. However, using such adversarial samples to perform actual attacks is an open research question.

Fig. 6: Scheduler attack model [32]

B. Privacy attacks

1) Readout sensing: The readout error in a quantum computer is state-dependent which means state |1⟩ and |0⟩ experience asymmetric bit-flip probabilities. Besides, the asymmetry extends beyond a single qubit. For example, if 2 qubits are read, then 4 possible states - |00⟩, |01⟩, |10⟩, and |11⟩ - will show asymmetric bit-flip probabilities. Therefore, if the two qubits belong to two different programs each, one adversary and another victim, the adversary can sense the state of the victim just by reading his/her qubit. The work in [26] demonstrated that an adversary can exploit readout error and infer another user’s output by reading his/her qubit.

The authors provide experimental results that show the adversary output distribution is glaringly different for victim qubit being |0⟩ and |1⟩. The sensing attack involves two steps, (i) the adversary collects reference signatures from a device by running circuits on both qubits, (ii) the adversary reads only his/her qubit and compares it with the reference signature using a statistical distance (Jensen-Shannon Distance). If the collected signature is statistically closer to reference signature |1⟩ than |0⟩ then it is inferred as |1⟩ and vice-versa. The authors report an inferring accuracy of 96% from experiments.

C. Vulnerabilities in reversible circuits

Quantum Circuits are based on reversible logic. There are several works on the security of reversible circuits [42–45]. In [45], an IP/IC piracy attack for reversible circuits was presented along with countermeasures. A target Boolean logic function can be converted into a reversible circuit using synthesis such as, quantum multiple-valued decision Diagrams (QMDD), binary decision diagram (BDD), etc. The synthesis step adds ancillary lines on the input side and garbage lines on the output side of the logical function. Reversible circuits have a certain level of inherent privacy as an adversary needs to know which are ancillary and garbage lines and values of ancillary bit to identify the functionality. However, the synthesis approach can leave “telltale” signs that help an adversary to locate ancillary and garbage lines. The adversary can exploit these left-over signs to launch an attack which entails knowing the embedded functionality of the circuit. In [44], the authors consider the end-user to be untrusted along with the foundry. They show that an end-user can launch piracy and reverse engineering attacks with access to a netlist and a functional chip.

IV. RESILIENCE TECHNIQUES

A. Depth optimal qubit mapping and routing

As mentioned in Section II-C, additional SWAP gates, that are necessary to satisfy coupling constraint, are detrimental for circuit performance. Thus, it is desired to keep the SWAP gates to a minimum. As the problem is NP-complete [46], researchers often resort to heuristic techniques to make it scalable.

In [18], the authors exploited A* search to find a depth-optimal version of the NN-compliant circuit. They defined a cost function $f(x) = g(x) + h(x) + l(x)$ where $g(x)$ is the path cost, $h(x)$ is the heuristic cost, and $l(x)$ is the look-ahead cost. The algorithm takes one layer of the circuit. The physical qubits used in the circuit and their neighbors are considered for SWAP insertion. For each possible SWAP, a heuristic cost $h(x)$ is computed. The cost is the new distance between qubits after adding the SWAP (adding a SWAP usually minimizes the distance). Besides, adding a SWAP affects future layers. The lookahead cost $l(x)$ accounts for this. The SWAP with the lowest $f(x)$ is selected as the candidate SWAP, and the search continues.

The proposal in [47] argues that not all candidate qubits (used physical qubits in the circuit and their neighbors) have the same priority in the SWAP insertion decision. They only consider qubits used in the particular layer and their neighbors. This reduced set of qubits curtails the number of SWAPs to be checked, decreasing the search time in large quantum circuits.
significantly. Many other works exist [34], [46], [48]–[54] on mapping and routing based on heuristic and exact methods.

B. Noise-aware mapping

Gate error rates vary among qubits in real devices i.e., some qubits are better (less erroneous) to perform computations than others. This observation has led to several noise-aware mapping techniques [19]–[21]. The main idea is to prioritize less erroneous qubits to perform the majority of the gates. In [19], the authors first proposed leveraging qubit-to-qubit variation to improve the program success rate. They proposed variation-aware qubit allocation (VQA) and variation-aware qubit movement (VQM) policies. In VQA, a set of physical qubits are picked to maximize their cumulative connectivity strength. The cumulative coupling strength is defined as the sum of success probabilities of all coupling links between the qubit and its neighbors. Its strength reflects two things: (i) a qubit is connected to more neighbors which is beneficial for optimal routing (less SWAP), and (b) the 2-qubit operations between the qubit and its neighbors will be less erroneous. Besides, the VQM policy ensures that the compiler will pick a routing path that uses fewer erroneous links.

In [20], the authors started with a depth optimal NN-compliant version of the circuit using an algorithms as in [18] and searched for an isomorphic sub-graph from the device coupling graph with best program fidelity. The method contained the depth of the circuit (beneficial to counteract qubit lifetime issue) while finding better qubits and links to run the program. In [21], the authors used satisfiability-modulo-theorem (SMT) to make qubit allocation and movement decisions while keeping error rate variations in mind. They also included readout error in their allocation decision besides gate error. Their weighted approach provided users with the flexibility to prioritize between gate and measurement errors.

C. Crosstalk mitigation

The classical version of the crosstalk arises when two gates, due to crosstalk, gate errors of two parallel gates can increase compared to isolated error rates. In [22], the authors conducted extensive experiments on several IBM devices to characterize crosstalk using simultaneous randomized benchmarking (SRB) [55]. They had two key observations: (i) not all couplings are susceptible to crosstalk i.e., crosstalk between some couplings is negligible whereas some couplings can experience a 2X-3X increase in error rates due to crosstalk, and (ii) crosstalk becomes negligible after 1-hop distance.

On the basis of crosstalk characterization results, the authors proposed a gate scheduling technique to minimize crosstalk. The core idea involved serializing the parallel gates at the cost of increased program depth (run-time) and hence, decoherence. The authors devised an SMT-based scheduler (XtalkSched) to compare the reduction in crosstalk error and increase in decoherence error due to gate serialization. Then, the scheduler only serialized gates that provided an overall reduction in error from these two conflicting conditions. Up to 5.6X improvement in program fidelity has been reported due to crosstalk-aware scheduling.

Another work in [56] proposed dynamic assignment of qubit frequency to minimize crosstalk. Qubits are frequency addressable. If two neighboring qubits have sufficiently different operating frequencies, they will be less susceptible to crosstalk from another. However, the qubit operating frequency range is small which causes frequency crowding. The authors presented a software solution to solve the frequency crowding issue and to dynamically allocate separate frequencies to neighboring qubits. They report 13.3X improvement in program success rate on average compared to gate serialization technique. The authors note that the solution is applicable to frequency tunable qubits.

D. Readout error mitigation

Once a quantum circuit completes execution, its final state is measured. In the superconducting quantum hardware from IBM, a single-qubit measurement is done by (i) running the readout pulse on the readout channel of the qubit, and (ii) recording the corresponding signal, which measures the energy state of the qubit, on the acquire channel. The signal recorded during the entire acquire duration is summed to generate a single complex value which is then plotted in an I-Q plane where |0⟩ and |1⟩ are supposed to show distinct clusters. Currently, IBM uses a linear classifier to classify the measured state (|0⟩ or |1⟩) from the imaginary and the real components of the complex value. The classifier is trained using a synthetic dataset. To generate this dataset, the qubit is prepared in the |0⟩ and |1⟩ state multiple times followed by measurement operations. The real and imaginary components associated with each measurement are used as the input features to the classifier. The actual states are used as the labels.

In [57], the authors showed that the linear classifier suffers from non-uniform measurement errors. Especially, the error magnifies when the actual state is closer towards |1⟩. This is partly due to the significant overlap zone between the |0⟩ and |1⟩ states created by the linear decision boundary. To circumvent this issue, the authors proposed two non-linear classifiers (based on circular and elliptical decision boundaries) and trained them to minimize the variance in measurement errors across different states. The authors reported a noticeable reduction in the variance of the errors over the linear classifier.

Another measurement calibration technique is available through IBM’s Qiskit tool kit. In this method, bit-flip probabilities of various states are computed by running circuits with known outputs. Then, an output distribution is compensated with the knowledge of bit-flip probabilities to get a measurement error calibrated result. This method gives excellent results for circuits with a smaller number of qubits. However, for a larger number of qubits, it requires a prohibitively large number of circuits (2^N circuits for N qubits) to generate the measurement calibration matrix.

There are a few works on readout error mitigation using detector tomography [58], [59].
E. Leveraging extended native gates

Most quantum computers offer only a single 2-qubit gate. For example, CNOT gate in IBM’s superconducting qubits, Mølmer–Sørensen gate in IonQ’s trapped-ion qubits, etc. However, new hardware is emerging which supports multiple 2-qubit gates [60]–[62]. An extended native gate set can make the gate decomposition step more efficient. In [60], the authors note that a SWAP can be decomposed using two gates (1 CZ + 1 iSWAP) when both CZ and iSWAP gates are available as native instructions. If only CZ or only iSWAP is available as the native gate, it takes 3 CZ/iSWAP to decompose a SWAP. Therefore, an extended gate set can significantly reduce the gate count from SWAP insertions in NISQ architectures with limited connectivity. For a test case on QAOA circuits, they report ≈30% reduction in gate depth leveraging the extended gate set. In general, reducing gate count is desired to minimize decoherence and gate error for better resilience.

F. Leveraging program structure – QAOA

General-purpose quantum compilers apply generic rules to optimize any given quantum program. They do not take into account program-specific details for aggressive optimization. In [12]–[14], the authors presented algorithm-specific compilation methodologies for QAOA which is a promising near-term algorithm. In QAOA, the ZZ-interactions (can be implemented with 2 CNOTs and 1 RZ operation as in Fig. 3) within a level are commutative [13]. In other words, these operations can be re-ordered without affecting the output state of the circuit. Parallelization of the ZZ-operations using binary bin-packing algorithm (Instruction Parallelization - IP), repeated compilation of QAOA-circuits with re-ordered layers guided by a branch-and-bound optimization heuristic (Iterative Compilation), layer-by-layer circuit construction and compilation prioritizing operations that require less SWAPs (Incremental Compilation - IC) or can be executed more reliably (Variation-aware Incremental Compilation - VIC) are proposed in [13]. They also developed heuristics to manipulate QAOA-circuit properties to perform intelligent initial qubit allocation (Qubit Allocation and Initial Mapping - QAIM/ Variation-aware Qubit Placement - VQP). These suite of techniques achieved ≈53% reduction in circuit depth, ≈23% reduction in gate-count, and ≈63% improvement in estimated success probability of QAOA-circuits over the existing state-of-the-art techniques. They also demonstrated ≈26% improvement in performance on a real IBM device. Similar techniques can be developed for other near-term quantum algorithms to maximize performance and resource utilization.

G. Error inclusive training of Quantum ML models

The training of the quantum classifier leverages a quantum-classical hybrid loop where a PQC generates an output distribution, and a classical optimizer updates the parameters of the PQC based on the output to minimize a cost function (minimize loss during the training phase). The authors in [39] noted that if the training is performed including noise in the PQC, the quantum classifier shows more resilient performance.
to the quantum hardware. The parameters of QuPUF and the output given by the hardware act as the challenge-response pair respectively. For each hardware, the authors accumulate different challenge-response pairs. The assumption here is that each hardware will generate unique challenge-response pairs due to every hardware’s unique characteristics like single-qubit error rates, CNOT error rates, decoherence time, and dephasing time. They propose two models of QuPUF namely, Hadamard gate-based QuPUF and decoherence-based QuPUF (Fig. 9(a) and (b)) as described below.

**Hadamard gate-based QuPUF:** The Hadamard gate-based QuPUF uses the biasing of the probability of the qubits towards either 0 state or 1 state to generate the response. The reason for such biasing could be gate error (usually small for single-qubit gates) or readout error (typically large). At the start, all the qubit states are initialized to a zero state. They are then put in a superposition state using the Hadamard gate, and then the qubits are measured. Ideally, the output should be 50% probability for both the states. But that won’t be the actual case due to the errors and would be biased towards either 1 state or 0 state which would act as a unique device signature.

**Decoherence-based QuPUF:** The decoherence-based QuPUF relies on the decoherence times of the qubits to give output. The qubits are initialized to 0 state and then flipped to 1 state using a not gate. The qubits are then allowed to decohere down from 1 state to 0 state by the use of idle gates, which do no operation and simply pass time. In other words, the qubits are excited to a higher state and allowed to decohere down to 0 state. The decoherence of qubits will effectively act as the unique device signature.

\[
\begin{align*}
\text{(a)} & \quad \begin{array}{c}
Y \\
H \\
H \\
Y \\
\end{array} \\
\text{(b)} & \quad \begin{array}{c}
X \\
H \\
H \\
X \\
\end{array}
\end{align*}
\]

Fig. 9: Proposed QuPUFs: (a) Hadamard gate-based QuPUF; (b) decoherence-based QuPUF. The tunable rotation has been added for resilience.

3) **Tracking changes in error rates:** To detect unexpected changes in error-rates attack, the authors in [33] proposed monitoring quantum circuit errors using test points. They proposed three different types of tests: (i) classical test, (ii) superposition test, and (iii) un-compute test. A user needs to know the expected output to detect any changes in error rates. However, the user does not know output beforehand, otherwise the problem would become trivial. Besides, he/she cannot always resort to simulation since that is computationally expensive. Therefore, the tests are carefully chosen so that the user has knowledge about output. For example, the output of an un-compute test should be the initial state it started with. Two copies of a circuit with test points are run on two isomorphic sub-graphs of the device. The outputs are compared to check if the relative error rates are satisfied. If there is an anomaly, unexpected changes in compile-time information (error rates) are detected.

**B. Privacy attacks**

1) **Obfuscation using dummy gate:** As mentioned in Section II-D, the quantum circuit can be an IP. In [63], the authors proposed adding *dummy gates* in a circuit to obfuscate the circuit from an untrusted compiler. The objective is to hide the true functionality of the circuit from the untrusted compiler. The adversary needs to identify and remove the dummy gates from an obfuscated circuit to extract the original circuit. This is a computationally hard problem since any gate can be a potential dummy gate. Any attempt to reuse the circuit without removing the dummy gates will result in corrupted or severely degraded performance. Fig. 10 conceptually shows the idea with a quantum circuit. The original circuit is divided into layers first. Then, inside each layer possible dummy SWAP insertion locations are identified. For example, if a layer has 3 free qubits, there are \( \binom{3}{2} = 3 \) choices for dummy SWAP gates. Therefore, there can be numerous SWAP insertion locations. However, only one dummy SWAP will be inserted in the original circuit and sent to the untrusted compiler.

The aim is to insert a dummy SWAP that will cause significant degradation in the output. The authors first ran exhaustive simulations with a set of test circuits and studied the impact of dummy SWAP insertion at each possible location. From the study, they developed a heuristic to find out an optimal SWAP insertion location. The heuristic tracks several features such as, the number of control qubits in the path from the SWAP to a measure qubit and calculates a score for the position. On the basis of the score, the optimal SWAP candidate is selected.

2) **Blind quantum computation:** Researchers considered protecting the privacy of quantum computation from compromised or malicious servers from an information-theoretic standpoint. The umbrella term for such line of research is *blind quantum computation* (BQC) [64]. Several theoretical protocols [65]–[67] have emerged which allows a client to perform a computation on a server such that the server cannot learn any information about the client’s input, output, and computation. Recently classical homomorphic encryption for quantum circuits has been proposed [67]. The scheme allows a client to both hide data and performs computation on the hidden data. A review of the BQC protocols is presented in [68]. Although the theory for BQC is well researched, the physical implementations of such protocols are under-examined. A few works on physical implementations of BQC has been cited in [68].

There is a recent work [69] on watermarking of quantum circuits. It includes a secret signature during the decomposition phase to watermark the IP [69].

C. **Securing reversible circuits**

To circumvent the IC/IP piracy attack in [45], the authors presented two approaches. The first (naive) approach adds
Fig. 10: Attack model proposed in [63]. The quantum circuit is sent by the user to the untrusted compiler, where the adversary can steal the IP or reverse engineer the circuit. Logic obfuscation is proposed as countermeasure.

Fig. 11: Overview and simplified flow of proposed methods for finding optimal gate parameter for the TRNG application.

extra (dummy) ancillary and garbage lines pre-synthesis. After the synthesis step, more ancillary and garbage lines will be added. The attack can identify only ancillary and garbage lines added post-synthesis, not the pre-synthesis ones. Thus, the first approach obfuscates the embedded functionality. However, adding extra lines pre-synthesis increases the hardware overhead. To optimize the cost, they propose a second approach where reversible gates are added to the circuit in a judicious manner so that after synthesis the “telltale” signs are removed keeping the logical functionality intact.

To prevent piracy and reverse engineering from the end-use, the authors proposed logic locking [44]. In particular, they chose SFLL-HD0, a variant of stripped functionality logic locking (SFLL) to secure the circuit. The logic locking block consists of 3 sub-blocks: functionally stripped circuit (FSC), restore unit/comparator, and restore signal/XOR. The FSC is formed by either adding or replacing a few logic gates. It inverts the output bit for one protected input pattern (PIP). The comparator/restore unit compares a key and the primary input to generate a restore signal. The key is saved in a tamper-proof memory. Finally, the XOR unit will revert the inverted output depending on the restore signal. The scheme protects against removal and SAT attacks.

VI. SECURITY OPPORTUNITY: TRNG

Quantum superposition property can be used to generate true random numbers. However, various noise sources, especially readout error, induce bias in the random bit generation. The authors in [17] proposed gate parameter optimization to compensate for this bias and to generate high quality true random numbers.

1) Hardware-in-the-loop approach: In this approach (Figure 11), a real quantum computer starts with an initial gate parameter and generates a bitstream. A classical optimizer calculates the 1/0 ratio from the stream and tries to minimize an objective function: $f = (1 - \text{ratio})^2$ by optimizing the gate parameter. The loop continues until an optimal parameter value is found which ensures a 1/0 ratio of 1.0 ± tolerance. Due to temporal variation, the optimal parameter varies with time and from device-to-device. Thus, the hardware-in-the-loop has to be invoked each time for each device which is tedious.

2) Machine learning based approach: In this approach, a statistical model (k-nearest neighbor regression) was trained to predict the gate parameter. First, the training data set is generated by running simulations in a noisy quantum circuit simulator. In the simulation, single qubit gate error, T1-relaxation time, and readout error are varied, and optimal gate parameter is computed for each combination. At the beginning, 3 qubit parameters - the gate error, T1-relaxation time, and readout error - are fed into the model, and the model outputs an optimal gate parameter. The true random number generator then starts with the parameter. This method avoids the slow classical optimizer-quantum hardware loop and quickly finds the optimal parameter.

3) Combined machine learning and hardware-in-the-loop approach: In this approach, the previous two methods are combined to leverage the best of two approaches. First, the statistical model generates a near-optimal parameter. Next, the hardware-in-the-loop starts from that parameter and finds
the final (more) optimal parameter. As the optimization loop starts from a near-optimal point, the loop converges faster than random initialization.

VII. FUTURE OUTLOOK

Quantum computers and the quantum workload possess several assets that could be lucrative targets for the adversaries to launch tampering, Denial-of-Service (DoS) attacks and/or to steal information. Quantum computers also come with several vulnerabilities including crosstalk and other noise sources, unencrypted netlist and sensitivity to noise, to name a few. Similar to classical computing, the security of quantum computing is intertwined with resilience. The presence of quantum computers in cloud and active usage are unlocking several new security and privacy threat vectors. The security of quantum computing requires an immediate attention to uncover various vulnerabilities and attack vectors so that proper defenses can be developed before the wide spread usage of this exotic and powerful technology.

VIII. CONCLUSIONS

In this paper, we review the challenges in NISQ devices. We discuss the state-of-the-art resilience techniques for addressing the challenges. We provide a survey of the security and privacy issues and their countermeasures in quantum computing. Finally, we discuss a projection into the future. As quantum computing matures and becomes ubiquitous, it will be more lucrative to attackers. Now is an opportune time to study the vulnerabilities and design safeguards for a resilient and secure future of quantum computing.

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