Third ArchEdge Workshop: Exploring the Design Space of Efficient Deep Neural Networks

Invited paper§

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Abstract—This paper gives an overview of our ongoing work on the design space exploration of efficient deep neural networks (DNNs). Specifically, we cover two aspects: (1) static architecture design efficiency and (2) dynamic model execution efficiency. For static architecture design, different from existing “end-to-end” hardware modeling assumptions, we conduct “full-stack” profiling at the GPU core level to identify better accuracy-latency trade-offs for DNN designs. For dynamic model execution, different from prior work that tackles model redundancy at the DNN-channels level, we explore a new dimension of DNN feature map redundancy to be dynamically traversed at runtime. Last, we highlight several open questions that are poised to draw research attention in the next few years.

I. INTRODUCTION

This paper summarizes our latest explorations in the design space of efficient DNNs. Specifically, we cover two complementary aspects: (a) static architecture design efficiency and (b) dynamic model execution efficiency.

A. Static Architecture Design Efficiency

Recent AutoML techniques, such as Neural Architecture Search (NAS), aim to automate the design of DNNs [11–13]. Due to the considerable search cost required to traverse the DNN design space, early approaches can take thousands of GPU hours to select the final model candidates [4]. To this end, in the context of hardware-constrained DNNs, previous work has significantly improved the search efficiency thanks to hardware performance models (e.g., DNN FLOPs, energy consumption, latency, etc.) which allow the AutoML algorithm to efficiently traverse the design space in a hardware-aware manner [5–7], by quickly discarding DNNs that violate the hardware constraints of the target platform.

Hardware-aware AutoML algorithms resort to certain ineffective performance interpretations with respect to the underlying hardware. On the one hand, early AutoML methods [8] use FLOPs as a general performance indicator, yet recent works demonstrate a mismatch between FLOPs and hardware metrics [9–12]. Nevertheless, this mismatch has been discussed mainly through empirical results and is not comprehensively analyzed. On the other hand, while recent methods replace FLOPs with predictive models (e.g., latency, power consumption), they rely on “end-to-end” profiling, which is either limited to discrete design choices (e.g., 50%, 100% channels) [13] or follows a look-up table-based manner [7].

To this end, we present a comprehensive “full-stack” profiling analysis that dives into individual GPU cores/threads to examine the intrinsic mechanisms of DNN execution [14]. As a key contribution, we shed light into the “GPU tail” effect as root cause of FLOPs-latency mismatch and GPU under-utilization. Based on our findings, we revisit the DNN design configuration choices of state-of-the-art AutoML methodologies to eliminate the tail effect, enabling larger, more accurate DNN designs at no latency cost. Hence, our method concretely improves accuracy-latency trade-offs, such as 27% latency and 4% accuracy improvements on top of SOTA DNN pruning and NAS methods. Moreover, we extend our profiling finding across different GPU configurations.

Discussion - Future work: while our investigation is employed as a fine-tuning (local search) step on top of SOTA designs, our findings can be flexibly incorporated into other AutoML methods. That is, a direction for future work is to revisit the predictive-models of existing single- and multi-path NAS works [15, 16] to further improve the accuracy-latency trade-offs by traversing the design space in a “tail effect”-aware fashion. Moreover, our methodology focuses on eliminating “tail effects” at the DNN design level, but improvements from alleviating GPU under-utilization can be realized at other design levels, as shown by novel scheduling- and computational flow-level explorations [17, 18].

Next, we hope that our findings could inspire researchers to revisit design-space assumptions, by allowing to identify hardware-optimal DNN candidates while eliminating sub-optimal ones. For example, our channel-level analysis reveals a discrete set of DNN channel configurations [14] with optimal GPU utilization, which could potentially reduce the number of candidates by 10× as opposed to traversing a continuous channel-number space, e.g., on top of existing channel-pruning methods [19, 20]. Last, an interesting direction would be to investigate the severity of similar under-utilization beyond GPUs, especially in the context of hardware accelerators and co-design NAS methodologies [21].
B. Dynamic Model Execution Efficiency

Dynamic execution methods aim at selecting between “switchable” DNN components at runtime [22]–[26]. The key insight behind these works is to improve the overall model efficiency by adaptively selecting and executing (a subset of) the model based on the input characteristics [27]. In our work, we extend this intuition across a new model redundancy dimension, namely dynamic feature map redundancy [28]. Specifically, we show that feature redundancy exists at the spatial dimensions of DNN convolutions, which allows us to formulate a dynamic pruning methodology in both channel- and spatial-wise dimensions. Our proposed method can greatly reduce the model computation with up to 54.5% FLOPs reduction and negligible accuracy drop on various image-classification DNNs.

Discussion - Future work: Drawing inspiration from our analysis on the FLOPs-latency mismatch, we highlight that when implemented naively, merely pruning convolution weights at the spatial level does not translate to latency savings. To this end, we postulate that advances in sparse DNN operators will be essential to support dynamic-sparse execution, as recently shown with CUDA implementations for dynamic convolutions [29].

II. CONCLUSION

In this paper, we summarize a set of novel efficiency optimization angles for DNN design in both static architecture design and dynamic model execution. New potential advantages can be attained by integrating the proposed new perspectives to current optimization methods.

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