Resonance Suppression Method for Grid-Connected Converter With LCL Filter Under Discontinuous PWM

HYEON-SIK KIM (Member, IEEE), AND SEUNG-KI SUL (Fellow, IEEE)

Corresponding author: Hyeon-Sik Kim (hyeonsik@gachon.ac.kr)

This work was supported in part by the Gachon University Research Fund of 2020 under Grant GCU-202008460002, and in part by the National Research Foundation of Korea (NRF) through Korean Government (Ministry of Science and ICT) under Grant NRF-2021R1F1A1051924.

ABSTRACT This paper presents a resonance suppression method that reduces current oscillation incurred by the LCL-filtered grid-connected converter’s discontinuous PWM (DPWM). First, the cause of LCL resonance is analyzed with an aspect of frequency and time domain for DPWM scheme. Then, voltage references are manipulated to decrease the resonance problem. In the proposed method, pole voltage references at the edge of offset voltage are slightly adjusted to reduce the current oscillation. In addition, a perturb and observe (P&O) technique is adopted to search the magnitude of an edge voltage. Through the simulation and experimental tests, the current oscillation is dramatically reduced while keeping the advantages of DPWM scheme. The proposed method can minimize the switching frequency under the grid harmonics regulation.

INDEX TERMS Discontinuous PWM (DPWM), grid-connected converter, LCL resonance, active damping, search algorithm.

I. INTRODUCTION

Voltage source converters (VSCs) have largely penetrated electric power grids to interface renewable energy sources (RES), distributed generations (DG), and energy storage systems (ESS). A passive filter is installed for grid-connected converter systems to minimize high-frequency harmonics incurred by a pulse-width modulation (PWM) of the converter. Compared to the simple inductive (L) filter, the inductive-capacitive-inductive (LCL) filter has better harmonic attenuation performance, which not only minimizes the size, weight, and cost of the filter inductor but also improves the dynamics of the system [1], [2]. However, the resonance of LCL filter could cause unexpected current harmonics to the grid and even instability of the converter itself.

Various damping algorithms have been proposed to suppress LCL resonance. In general, existing literature can be classified into two groups: passive damping [3]–[5] and active damping methods [6]–[15]. Passive damping methods are quite simple and robust; however, they result in additional losses at a damping resistor. In addition, they reduce the filter attenuation ratio at PWM switching frequency. As an alternative, active damping methods have been proposed to simulate virtual damping resistors. They pass resonant frequency by adding an additional feedback loop to the current controller, which minimizes the losses on the filter. In [10]–[12], a digital delay due to sampling and computation was modeled to ensure the robustness of active damping methods. In [13]–[15], a resonance interaction between paralleled converters was analyzed to maintain system stability. These researches alleviate inherent resonant characteristics of LCL filters where the harmonic source exists. However, they were only focused on a current controller’s stability analysis coupled with a damping algorithm, where the converter is assumed as an ideal voltage source. Thus, they did not consider a resonance problem provoked by PWM schemes of the converter and harmonic source itself.

In respect to the PWM scheme, it is essential to minimize power losses under the stringent regulation of grid standards. Current harmonics incurred by the PWM switching are subject to harmonic regulations such as IEEE 519 or BDEW [16], [17]. They describe maximum allowable harmonic currents at each harmonic number. In the worst case,
the maximum harmonic current is 0.3 % of the rated current for harmonic numbers higher than 35 [16]. Therefore, \(LCL\) filter should be designed and damped to satisfy the harmonic regulation where harmonic spectra of PWM methods are carefully considered.

In [18], the impacts of PWM methods were analyzed based on power loss and power density for two-level three-phase converter with \(LCL\) filter. 60° discontinuous PWM (DPWM) has better performance compared with continuous PWM (CPWM) in most aspects, i.e., lower total power losses while keeping the harmonic standard. Not only semiconductor losses but also core loss of the filter inductor and cooling conditions are analyzed to optimize the weight of \(LCL\) filter. However, it did not consider a current oscillation provoked by abrupt changes of an offset voltage.

In [19] and [20], the resonance problem from DPWM was discussed through a frequency domain analysis. The low-order harmonics under a half of the switching frequency were triggered when the offset voltage is abruptly changed. These moments are generated every 60° in the conventional DPWM. As an alternative, a hybrid PWM method mixed with DPWM and CPWM was proposed to alleviate the cause of the resonance problem. In [21], an adaptive DPWM method was proposed to increase the ratio of CPWM to DPWM when the modulation index (MI) is low. It could be regarded as one of the hybrid PWM methods. However, the hybrid PWM methods in [19]–[21] increases switching losses compared to DPWM method because the region of CPWM is inserted to minimize the harmonics.

In this paper, the resonance problem incurred by DPWM is analyzed through \(LCL\) filter modeling in the frequency domain and harmonic spectra analysis according to the modulation schemes. Then, voltage references are modified to suppress the current oscillation while maintaining the merits of DPWM scheme. In the proposed method, the voltage references at the edges of offset voltage are moved closer to the optimal point by applying a perturb and observe (P&O) algorithm. Moreover, practical implementations and gain settings are analyzed to improve the performance of the proposed algorithms. The effectiveness of the proposed method is verified with the simulation and experimental results. Compared to the previous research work [22], the implementation and gain setting processes are clearly described. Besides, simulation and experimental results are added to clarify the effectiveness of the proposed method.

II. ANALYSIS OF RESONANCE PROBLEM

A. \(LCL\) FILTER MODELING

Fig. 1 shows the circuit topology of a grid-connected converter with \(LCL\) filter. \(L_{fc}, L_{g} \equiv L_{fg} + L_{grid}\), and \(C_{f}\) represent a converter-side inductance, a grid-side inductance, and a filter capacitance, respectively. The filter admittances from converter voltage, \(v_{conv}\), to converter current, \(i_{conv}\), and to grid current, \(i_{grid}\), are defined by the following equations, respectively:

\[
Y_{cc}(s) = \frac{i_{conv}(s)}{v_{conv}(s)} = \frac{L_{g} C f s^2 + 1}{L_{fg} L_{g} C f s^3 + (L_{fc} + L_{g}) s} = \frac{1}{L_{fc}} \left( \frac{s^2 + \omega_{LC}^2}{s^3 + \omega_{res}^2} \right),
\]

\[
Y_{gc}(s) = \frac{i_{grid}(s)}{v_{conv}(s)} = \frac{1}{L_{fg} L_{g} C f s^3 + (L_{fc} + L_{g}) s} = \frac{1}{L_{fg} + L_{g} s} \left( \frac{s^2 + \omega_{res}^2}{s^2 + \omega_{res}^2} \right),
\]

where \(\omega_{res} = 2 \pi f_{res} = \sqrt{\frac{1}{L_{fg} L_{g} C f}}\), and \(\omega_{LC} = 2 \pi f_{LC} = \sqrt{\frac{1}{L_{fg} L_{g} C f}}\). Here, \(f_{res}\) is the resonant frequency of \(LCL\) filter and \(f_{LC}\) is the LC resonant frequency of grid-side.

Fig. 2 depicts the frequency response of the filter admittances where \(LCL\) filter parameters are given in Table 1. \(Y_{gc}\) has 20 dB/dec of attenuation rate in a low frequency range, i.e., \(-20\) dB/dec for \(f < f_{res}\), and \(60\) dB/dec attenuation rate in a high frequency range, i.e., \(-60\) dB/dec for \(f > f_{res}\). The magnitude of \(Y_{gc}\), \(|Y_{gc}(s)|\), becomes very large at the resonant frequency, \(f_{res}\). This result means that voltage harmonics around \(f_{res}\) can provoke large current oscillation and violate the harmonic regulation. Thus, \(f_{res}\) should be far
where $m$ and $n$ are carrier and baseband integer indices, respectively [23].

Fig. 3 shows the pole voltage references, PWM waveforms and harmonic spectra of alpha-phase voltage, defined as $v_{\alpha1}$, when MI and $f_{sw}$ are set to 0.9 and 7.2 kHz, respectively. Here, MI is defined as the ratio between a fundamental component of the phase voltage, $v_{\alpha1}$, and a half of dc-link voltage as follows:

$$MI = \frac{v_{\alpha1}}{0.5V_{dc}}. \quad (4)$$

As shown in Fig. 3(a), the offset voltage of CPWM, $v^*_{\alpha1}$ (CPWM), which is equivalent to SVPWM [24], is defined as

$$v^*_{\alpha1} \text{(CPWM)} = -0.5(v^*_{\text{max}} + v^*_{\text{min}}), \quad (5)$$

where $v^*_{\text{max}}$, $v^*_{\text{min}}$ represent the maximum and minimum pole voltage reference, respectively.

The offset voltage of DPWM, $v^*_{\alpha1}$ (DPWM), is defined as follows as shown in Fig. 3(b).

$$v^*_{\alpha1} \text{(DPWM)} = \begin{cases} +0.5V_{dc} - v^*_{\text{max}} \equiv v^*_{\alpha1, \text{pos}}, & (v^*_{\text{max}} + v^*_{\text{min}} \geq 0) \\ -0.5V_{dc} - v^*_{\text{min}} \equiv v^*_{\alpha1, \text{neg}}, & (v^*_{\text{max}} + v^*_{\text{min}} < 0). \end{cases} \quad (6)$$

Harmonic spectra of $v_{\alpha1}$ in Fig. 3 show that DPWM has larger and widespread sideband harmonics near $f_{sw}$ compared with CPWM. In this case, the sideband harmonics of $f_{sw}$ and resonant frequency band near $f_{\text{res}}$ can be overlapped, which would provoke severe harmonic oscillation [20].

An effective $f_{sw}$ of DPWM is two-thirds of that of CPWM, and the switching loss of DPWM is almost half of that of CPWM owing to no switching at near maximum current. Thus, $f_{sw}$ of DPWM can increase up to twice that of CPWM under the given limitation of the switching loss depending on a power factor angle [25], [26]. However, in spite of increasing $f_{sw}$, sideband harmonics around $f_{sw}$ conspicuously increase when DPWM is applied. Therefore, $v_{\alpha1}$ harmonics near $f_{\text{res}}$ should be avoided by changing PWM schemes or revising control algorithms.

When DPWM is applied, $v^*_{\alpha1}$ abruptly changes from $v^*_{\alpha1, \text{pos}}$ to $v^*_{\alpha1, \text{neg}}$ or vice versa, 6 times per an electrical period. Fig. 3(b) shows that a pulse width of $v^*_{\alpha1}$ abruptly varies at rising and falling edge of $v^*_{\alpha1}$ contrary to the case of SVPWM in Fig. 3(a), which induces more sideband harmonics around $f_{\text{res}}$. In the aspect of time domain, it could be comprehended that the harmonic oscillation occurs at each $v^*_{\alpha1}$ edge, triggering the oscillation not only in converter currents but also in grid currents. Consequently, the grid currents start to oscillate at an interval of 60° for DPWM and that cannot be easily suppressed with the conventional methods for the grid-connected converter with LCL filter.

**III. PROPOSED RESONANCE SUPPRESSION METHOD**

**A. CONCEPT OF PROPOSED METHOD**

To suppress the harmonic oscillation incurred by DPWM, $v_{\alpha1}$ harmonics near $f_{\text{res}}$ should be avoided. $v_{\alpha1}$ spectra are

![FIGURE 3. Pole voltage references, PWM waveforms, and harmonic spectra of $v_{\alpha1}$ when MI = 0.9, $f_{sw}$ = 7.2 kHz. (a) CPWM. (b) DPWM.](image-url)
determined by pole voltage references, $v_{abcn}^*$, which means that $v_{abcn}^*$ can be modified to change $v_{har}$ near $f_{res}$. The pole voltage references, $v_{abcn}^*$, is the sum of phase voltage references, $v_{abcs}^*$, and offset voltage reference, $v_{sn}^*$. Here, $v_{abcs}^*$ is set up by $d-q$ voltage references, $v_{dq}^*$, which is the output of the current controller. On the other hand, $v_{sn}^*$ is determined by the PWM method. The PWM method can be changed to suppress sideband harmonics near $f_{res}$ as mentioned previously [19]–[21]. However, the modification of $v_{sn}^*$ is not desirable because a transition from DPWM to other PWMs would degrade the system’s efficiency due to increased switching loss. Thus, the focus is on modifying $v_{dq}^*$ to suppress the harmonic oscillation while the current controller operates without interruption.

Fig. 4(a) shows the traces of $d-q$ voltage references in a stationary reference frame, $v_{dq}^*$, at a steady-state under the conventional current controller. The magnitude of $v_{dq}^*$ remains constant at the instant of $v_{sn}^*$ edge because the bandwidth of the current controller is too low to catch up with the current harmonics near $f_{res}$. $f_{res}$ is about one-third of $f_{sw}$, i.e., a few kHz, in the case of the $LCL$-filtered converter to satisfy the harmonic regulation. It is far from the current controller bandwidth, usually set to a few hundred Hz, e.g., 200 Hz. To damp the $LCL$ resonance, a feedforward voltage, $\alpha_{peak} v_{dq}^*$, can be added or subtracted at the output of the current controller as shown in Fig. 4(b). Since the dominant voltage harmonics, i.e., $v_{har}$ near $f_{res}$, are induced at $v_{sn}^*$ edge, the feedforward voltage is applied at the edge of $v_{sn}^*$ in the direction of damping the resonance. The feedforward voltage before the edge of $v_{sn}^*$ is compensated after the edge of $v_{sn}^*$ to maintain $v_{dq}^*$ on the average.

Fig. 5 shows the conceptual relationship between the ratio of the feedforward voltage, $\alpha_{peak}$, and the magnitude of harmonic currents represented by THD$_i$. Here, THD$_i$ is the total harmonic distortion of $i_{grid}$, and $\alpha_{opt}$ represents the optimal $\alpha_{peak}$ to minimize the harmonic distortion at $v_{sn}^*$ edge. The correlation between THD$_i$ and $\alpha_{peak}$ varies depending on the operating conditions such as the filter admittance and the harmonic spectra of PWM. Thus, it is difficult to find an analytical solution for $\alpha_{opt}$ in real-time due to heavy computational burden.

The harmonic spectra of PWM are the function of MI and $f_{sw}$, which are influenced by disturbances such as a converter nonlinearity [27], [28], and a sensor accu-
racy [29]. In addition, the filter characteristics are affected by the manufacturing tolerance and grid impedance variation. Thus, a searching algorithm would be a practical solution to find $\alpha_{\text{opt}}$ in real-time. As a result, the proposed method combines the searching algorithm instead of the premade LUT.

Fig. 6 shows the harmonic spectra of $v_{\text{sa}}$ when MI and $f_{\text{sw}}$ are set to 0.9 and 7.2 kHz, respectively. The low-order harmonics up to 50-th are zoomed in to distinguish $v_{\text{har}}$ components near $f_{\text{res}}$. There are $v_{\text{har}}$ components near $f_{\text{res}}$ owing to the widespread sideband harmonics of DPWM as shown in Fig. 6(a). It can be suppressed by changing $\alpha_{\text{peak}}$ while maintaining DPWM. Fig. 6(b) reveals that low-order harmonics are minimized by setting $\alpha_{\text{peak}}$ to $-0.04$, close to $\alpha_{\text{opt}}$. In this case, low-order harmonics owing to DPWM are reduced by almost one-third by adding the feedforward voltage at the edge of $v_{\text{sn}}^*$. Active damping algorithms, e.g., filter capacitor current- or voltage- feedback-based algorithms [6]–[8], are insufficient to suppress the resonance incurred by DPWM because the damping performance is limited by a sampling noise and digital delay. These algorithms reduce the current harmonics after $v_{\text{sn}}^*$ edge have passed by adding the virtual damping resistors. It cannot eliminate a root cause of the $LCL$ resonance, i.e., $v_{\text{har}}$ near $f_{\text{res}}$, which triggers the harmonic oscillation at each $v_{\text{sn}}^*$ edge. However, it can suppress the harmonics provoked by other causes such as grid harmonics and other converters. Thus, the active damping algorithms can be utilized in conjunction with the proposed method to enhance the system stability under a weak grid condition.

**B. IMPLEMENTATION OF PROPOSED METHOD**

To realize the proposed method, the edge of offset voltage, $v_{\text{sn}}^*$ edge, should be detected in advance and the feedforward voltage, $\alpha_{\text{peak}} v_{\text{ds}}^*$, added at each edge of the offset voltage. Moreover, the optimal $\alpha_{\text{peak}}$, defined as $\alpha_{\text{opt}}$, is searched in real-time to minimize the resonance incurred by DPWM. Thus, $v_{\text{sn}}^*$ edge detection and $\alpha_{\text{opt}}$ searching algorithms should be processed at each calculation point.

Fig. 7 shows the flowchart of the proposed $v_{\text{sn}}^*$ edge detection algorithm. First, the voltage reference angles at present and the next operating point, $\theta_{\text{v}}$ and $\theta_{\text{v,pre}}$, are calculated by an arctangent function as shown below, respectively.

$$\theta_{\text{v}} = \text{atan2}(v_{qs}^*, v_{ds}^*),$$

$$\theta_{\text{v,pre}} = \theta_{\text{v}} + \omega_{\text{grid}} T_{\text{samp}},$$

where $\text{atan2}(v_{qs}^*, v_{ds}^*)$ returns the four-quadrant arctangent of $v_{\text{dq}}^*$ in the range of $[-\pi, \pi]$.

Here, $\theta_{\text{v,pre}}$ is predicted under the assumption of steady-state condition. On the basis of $\theta_{\text{v}}$ and $\theta_{\text{v,pre}}$, each status of $v_{\text{sn}}^*[n]$ and $v_{\text{sn}}^*[n + 1]$, equivalent to $k_0$ and $k_{0,\text{pre}}$, is decided. When $k_0 = 0; v_{\text{sn}}^* = v_{\text{sn, pos}}$, and when $k_0 = 1; v_{\text{sn}}^* = v_{\text{sn, neg}}$ as defined in (6). Then, positive and negative edges of $v_{\text{sn}}^*$ are distinguished by the difference of $k_{0,\text{pre}}$ and $k_0$, $k_{\text{edge}}$, as follows:

$$k_{\text{edge}} = k_{0,\text{pre}} - k_0.$$ (9)

Consequently, $k_{\text{edge}}$ is utilized to detect the edge of $v_{\text{sn}}^*$.
widely utilized for a maximum power point tracking (MPPT) algorithm in photovoltaic applications due to ease of implementation. The basic principle is to perturb $\alpha_{\text{peak}}$ and observe a current error, $i_{\text{err}}$, where $i_{\text{err}}$ is measured twice and compared to track down $\alpha_{\text{opt}}$.

Fig. 8 shows the flowchart of the proposed $\alpha_{\text{peak}}$ P&O algorithm. First, $i_{\text{err}}$ was extracted until the number of $v_{\text{sn}}$ edge is sufficient to minimize the effects of other disturbances in $i_{\text{err}}$ observation part. $i_{\text{err}}$ is simply extracted from the current error terms in the current controller at the steady-state condition, i.e., the error between current references and sensed currents. Otherwise, a current observer could predict the converter current without the effects of PWM harmonics [8], $i_{\text{err}}$ is calculated from the sum of the squared current error, where the current error is the difference between actual and predicted currents. $i_{\text{err}}$ is accumulated until the number of $k_{\text{edge}}$, defined as $k_{\text{edge\_cnt}}$, is equal to $k_{\text{max}}$. The duration of $i_{\text{err}}(t)$ calculation is $120^\circ \cdot k_{\text{max}}$.

The direction of $\alpha_{\text{peak}}$ is then determined by comparing a measured $i_{\text{err}}$ in $\alpha_{\text{peak}}$ perturbation part. The principle of $\alpha_{\text{peak}}$ perturbation part is as follows: If measured $i_{\text{err}}$, $i_{\text{err}}(t)$, is less than $i_{\text{err}}$ measured at one sample before, $i_{\text{err}}(t - 1)$, $\alpha_{\text{peak}}$ keeps the present moving direction, i.e., the direction of $\Delta \alpha_{\text{peak}} = \alpha_{\text{peak}}(t) - \alpha_{\text{peak}}(t - 1)$. Otherwise, $\alpha_{\text{peak}}$ changes to the opposite direction of $\Delta \alpha_{\text{peak}}$. It can be shortly implemented by comparing $\Delta \alpha_{\text{peak}}$ with $\Delta i_{\text{err}}$. As follows:

$$\alpha_{\text{peak}}(t + 1) = \begin{cases} \alpha_{\text{peak}}(t) - \varepsilon_{\text{peak}}, & (\Delta \alpha_{\text{peak}} \cdot \Delta i_{\text{err}} \geq 0) \\ \alpha_{\text{peak}}(t) + \varepsilon_{\text{peak}}, & (\Delta \alpha_{\text{peak}} \cdot \Delta i_{\text{err}} < 0) \end{cases}$$

where $\varepsilon_{\text{peak}}$ is a perturbation step size of $\alpha_{\text{peak}}$.

As a result, $\alpha_{\text{peak}}$ is updated and directly applied at the next $v_{\text{sn}}$ edge.

Fig. 9 shows the overall control block diagram of the proposed method. First, $k_{\text{edge}}$ is extracted by the $v_{\text{sn}}$ edge detection algorithm. Then, $\alpha_{\text{peak}}$ is calculated based on the P&O algorithm. $k_{\text{edge}}$ and $\alpha_{\text{peak}}$ are utilized to modify the output voltages of the current controller, $v_{dq\_CC}^*$. Finally, $d-q$ voltage references, $v_{dq}^*$, are revised as follows after the proposed algorithms are applied.

$$v_{dq}^* = (1 + k_{\text{edge}} \alpha_{\text{peak}})v_{dq\_CC}^*.$$  

$\alpha_{\text{peak}}$ is limited within a voltage hexagon at a stationary reference frame, which is a physical limit of PWM. If $v_{dq}^*$ is out of the hexagon boundary, then the voltage should be adjusted at the boundary of the hexagon. This means that the range of $\alpha_{\text{peak}}$ is naturally set within the dc-link voltage.

### C. GAIN SETTING IN PROPOSED METHOD

The tuning factors of the proposed method are $k_{\text{max}}$ and $\varepsilon_{\text{peak}}$. Disturbances such as converter nonlinearity and grid harmonics influence the current error, $i_{\text{err}}$. They provoke undesirable fluctuations of $\alpha_{\text{peak}}$. Thus, $k_{\text{max}}$ can be increased to make the P&O algorithm more robust to the disturbances. However, the dynamic response gets sluggish as $k_{\text{max}}$ becomes larger. To minimize the effects of a current unbalance in the three-phase system, $k_{\text{max}}$ is set in multiples of three, i.e., $k_{\text{max}} = 3n$. In this case, $\alpha_{\text{peak}}$ is updated at an interval of $360^\circ \cdot n$.

Likewise, small $\varepsilon_{\text{peak}}$ minimizes the oscillation of $\alpha_{\text{peak}}$, enhancing the steady-state performance owing to its small perturbation. However, small $\varepsilon_{\text{peak}}$ slows down the transient response under abrupt changes of the operating condition such as current reference and grid voltage variations. Thus, $k_{\text{max}}$ and $\varepsilon_{\text{peak}}$ should be adjusted considering both dynamic responses in the transients and oscillatory responses in the steady states. Otherwise, a dynamic step size can be applied to improve the performances of the proposed method further.

The proposed method can be applied for whole MI ranges where the range of $\alpha_{\text{peak}}$ is limited owing to its voltage margin as aforementioned. However, this is not a concern because the oscillation caused by DPWM decreases as MI increases. In other words, the effects of $v_{\text{sn}}$ jumps are reduced under high MI operation, which lessens the $LCL$ resonance. In any case, $\alpha_{\text{peak}}$ is converged to $\alpha_{\text{opt}}$ by the proposed P&O algorithm within the physical voltage limit.

### IV. SIMULATION RESULTS

In the simulation, the performances can be evaluated under ideal conditions without the effects of noise and disturbance. The grid-connected converter with $LCL$ filter in Fig. 1 was simulated in MATLAB/Simulink with PLECS. System parameters were set as Table I, and a grid inductance, in Fig. 1 was simulated in MATLAB/Simulink with PLECS. In this case, $f_{\text{res}}$ was located at 2.03 kHz, near 34$\text{th}$ harmonics. The gains of the proposed method, $k_{\text{max}}$ and $\varepsilon_{\text{peak}}$, were set to 3 and 0.0005, respectively.

Fig. 10 shows the waveforms and harmonic spectra of $\alpha$-phase grid current, $i_{\text{grid\_av}}$, at the rated current and unity power factor conditions, i.e., $P^* = 5$ kW and $Q^* = 0$ kW.
where the dc-link voltage, $V_{dc}$, was set to 400 V. Fig 9(a) shows that the resonance occurs when DPWM is applied. Current oscillations are provoked when $v_{abcn}^*$ is abruptly changed, i.e., at $v_{sn}$ edges. The current harmonics exceeds the grid regulation near $f_{res}$ band, i.e., 0.3 % of the rated current in the case of IEEE 519. After applying
the proposed method, harmonics near $f_{\text{res}}$ are remarkably decreased as shown in Fig. 10(b), satisfying the regulation while still maintaining DPWM. It means that the effective $f_{\text{sw}}$ can be reduced by adopting DPWM with the proposed method.

Fig. 11 shows the simulation results when $P^*$, $Q^*$ and $V_{dc}$ were set to 5 kW, 0 kW, and 360 V, respectively. The dc-link voltage decreased by 10% when compared to the case of Fig. 10, reducing the effects of $v_{in}^*$ jumps at $v_{in}^*$ edges. As shown in Fig. 11(a), the current harmonics near $f_{\text{res}}$ exceed the grid regulation when DPWM is applied even under the reduced dc-link voltage, i.e., high MI operation. However, the current oscillations are decreased and satisfy the regulation by applying the proposed method as shown in Fig. 11(b).

Fig. 12 shows the current and voltage waveforms under $P^*$ transients from $+5$ kW to $-5$ kW when the proposed method was applied. The proposed method can rapidly suppress the current oscillations during $P^*$ variations where the resonance effects are remarkably reduced within a half cycle. It means that $\alpha_{\text{peak}}$ set by the P&O algorithm is quite effective even under transient conditions because MI is not significantly changed in the grid-connected converter. Moreover,
V. EXPERIMENTAL RESULTS

The proposed and conventional methods were conducted in a 5-kW converter system with LCL filter as shown in Fig. 13, where the system configurations are identical with the circuit diagram in Fig. 1. All control algorithms were implemented in a digital signal processor (DSP), TMS320F28335. System parameters and controller gains of the experiment were identical to those of the simulation. The dead time was set to 2 µs, and \( V_{dc} \) was changed by a dc power supply. In addition, the three-phase grid was emulated by a programmable ac power source.

Fig. 14 shows the experimental results during the steady-state operation, the same condition as those in Fig. 10. In contrast to the simulation results, low-order harmonics such as 5th and 7th are provoked by the converter nonlinearity. In Fig. 14(a), where DPWM is applied, there are harmonics near \( f_{res} \) due to the transition of \( v_{sn}^* \). Without the proposed method, the harmonic distortion occurs at the edge of \( v_{sn}^* \). It shows that the harmonic regulation cannot be achieved under \( v_{sn}^* \) jumps as shown in the harmonic spectra of \( i_{grid,a} \).

Thanks to the proposed method, the harmonic oscillations are significantly suppressed by shifting \( v_{abcn}^* \) at the edge of \( v_{sn}^* \) as shown in Fig. 14(b).

Fig. 15 shows the experimental results under the same condition as those in Fig. 11. Similar to the case of Fig. 14(a), the harmonic distortion occurs at each \( v_{sn}^* \) edge by DPWM as shown in Fig. 15(a). The current harmonics near \( f_{res} \) are slightly decreased by internal resistances of the LCL filter compared with those in the simulation. However, the internal resistances are not sufficient to satisfy the harmonic regulation. After applying the proposed method, harmonic oscillation incurred by DPWM is significantly reduced as shown in Fig. 15(b). It satisfies the harmonic regulation by applying
the proposed method without adding the damping resistor or increasing the switching frequency.

Fig. 16 shows the performance under $V_{dc}$ transients from 400 V to 350 V. It shows that the proposed method can suppress LCL resonance even under rapid $V_{dc}$ variations, i.e., MI variations. $\alpha_{\text{peak}}$ is slowly converged to $\alpha_{\text{opt}}$ under MI variations by applying the P&O algorithm. However, the variation of MI is restricted within certain ranges for the grid-connected converter. In addition, $V_{dc}$ is slowly changed in practical applications. Thus, the P&O algorithm can be an effective solution to search $\alpha_{\text{opt}}$ in real-time where $\alpha_{\text{opt}}$ varies slightly depending on the operating conditions.

VI. CONCLUSION
This paper analyzes the resonance problem incurred by DPWM for the grid-connected converter with LCL filter. In this paper, the resonance problem is dealt with the frequency and time domain analysis. The root cause of LCL resonance is interpreted as abrupt changes of the offset voltage. Thus, the voltage references near the edge of offset voltage is modified to minimize the current oscillation while preserving the merits of DPWM scheme. In the proposed method, the pole voltage references at the $v^{*}_{\text{in}}$ edge are move closer to the optimal point. It becomes possible to implement the $v^{*}_{\text{sn}}$ edge detection and $\alpha_{\text{opt}}$ searching algorithms. The performance of the proposed method has been verified with various simulation and experimental results. The current oscillation at $v^{*}_{\text{sn}}$ edges is conspicuously reduced through the proposed method, minimizing the effective switching frequency of PWM converter under the satisfaction of the grid harmonics regulation.

REFERENCES
[1] M. Liserre, F. Blaabjerg, and S. Hansen, “Design and control of an LCL-filter-based three-phase active rectifier,” IEEE Trans. Ind. Appl., vol. 41, no. 5, pp. 1281–1291, Sep./Oct. 2005.
[2] K. Jalili and S. Bernet, “Design of LCL filters of active-front-end two-level voltage-source converters,” IEEE Trans. Ind. Electron., vol. 56, no. 5, pp. 1674–1689, May 2009.
[3] R. Peña-Alzola, M. Liserre, F. Blaabjerg, R. Sebastián, I. Dannenh, and F. W. Fuchs, “Analysis of the passive damping losses in LCL-filter based grid converters,” IEEE Trans. Power Electron., vol. 28, no. 6, pp. 2642–2666, Jun. 2013.
[4] R. N. Beres, X. Wang, F. Blaabjerg, M. Liserre, and C. L. Bak, “Optimal design of high-order passive-damped filters for grid-connected applications,” IEEE Trans. Power Electron., vol. 31, no. 4, pp. 2083–2098, Mar. 2016.
[5] D. Solati-Akbaran, K. G. Khajeh, and F. Zare, “A novel filter design method for grid-tied inverter,” IEEE Trans. Power Electron., vol. 36, no. 5, pp. 5473–5485, May 2021.
[6] J. Dannenh, M. Liserre, and F. W. Fuchs, “Filter-based active damping of voltage source converters with LCL filter,” IEEE Trans. Ind. Electron., vol. 58, no. 8, pp. 3623–3633, Aug. 2011.
[7] S. G. Parker, B. P. McGrath, and D. G. Holmes, “Regions of active damping control for LCL filters,” IEEE Trans. Ind. Appl., vol. 50, no. 1, pp. 424–432, Jan./Feb. 2014.
[8] V. Miskovic, V. Blasko, T. M. Jahns, A. H. C. Smith, and C. Romensko, “Observer-based active damping of LCL resonance in grid-connected voltage source converters,” IEEE Trans. Ind. Appl., vol. 50, no. 6, pp. 3977–3985, Apr. 2014.
[9] W. Yao, Y. Yang, X. Zhang, F. Blaabjerg, and P. C. Loh, “Design and analysis of robust active damping for LCL filters using digital notch filters,” IEEE Trans. Power Electron., vol. 32, no. 3, pp. 2360–2375, Mar. 2017.
[10] M. Lu, X. Wang, P. C. Loh, F. Blaabjerg, and T. Dragicevic, “Graphical evaluation of time-delay compensation techniques for digitally controlled converters,” IEEE Trans. Power Electron., vol. 33, no. 3, pp. 2601–2614, Mar. 2018.
[11] E. Rodriguez-Diaz, F. D. Freijedo, J. C. Vasquez, and J. M. Guerrero, “Analysis and comparison of notch filter and capacitor voltage feedforward active damping techniques for LCL grid-connected converters,” IEEE Trans. Power Electron., vol. 34, no. 4, pp. 3958–3972, Apr. 2019.
[12] F. Zheng, W. Wu, B. Chen, and E. Koutroulis, “An optimized parameter design method for passivity-based control in a LCL-filtered grid-connected inverter,” IEEE Access, vol. 8, pp. 189878–189890, 2020.
[13] M. Lu, X. Wang, P. C. Loh, and F. Blaabjerg, “Resonance interaction of multiparallel grid-connected inverters with LCL filter,” IEEE Trans. Power Electron., vol. 32, no. 2, pp. 894–899, Feb. 2017.
[14] H. Bai, X. Wang, and F. Blaabjerg, “Passivity enhancement in renewable energy source based power plant with paralleled grid-connected VSIs,” IEEE Trans. Ind. Appl., vol. 53, no. 4, pp. 3793–3802, Jul. 2017.
[15] K.-B. Park, F. D. Kieferndorf, U. Drofenik, S. Pettersson, and F. Canales, “Optimization of LCL filter with integrated intercell transformer for two-interleaved high-power grid-tied converters,” IEEE Trans. Power Electron., vol. 35, no. 3, pp. 2317–2333, Mar. 2020.
[16] IEEE Recommended Practices and Requirements for Harmonic in Electrical Power Systems, IEEE Standard 519, 2014.
[17] Technical Guideline Generating Plants Connected to the Medium-Voltage Network, BDEW MW Guideline, 2008.
[18] K. B. Park, F. D. Kieferndorf, U. Drofenik, S. Pettersson, and F. Canales, “Weight minimization of LCL filters for high-power converters: Impact of PWM method on power loss and power density,” IEEE Trans. Ind. Appl., vol. 53, no. 3, pp. 2282–2296, May/Jun. 2017.
[19] J.-H. Park and K.-B. Lee, “Improved DPWM scheme for improvement of grid current quality in a large-scale grid-connected inverter system with a LCL-filter,” in Proc. IEEE Conf. Energy Convers. (CENCON), Oct. 2015, pp. 343–348.
[20] J.-H. Park and K.-B. Lee, “Performance improvement for reduction of resonance in a grid-connected inverter system using an improved DPWM method,” Energies, vol. 11, no. 1, p. 113, Jan. 2018.
[21] F. Liu, K. Xin, and Y. Liu, “An adaptive discontinuous pulse width modulation (DPWM) method for three phase inverter,” in Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC), Mar. 2017, pp. 1467–1472.
[22] H.-S. Kim and S.-K. Sul, “Voltage reference modification scheme for resonance suppression in LCL-filtered inverters with discontinuous PWM method,” in Proc. Int. Power Electron. Conf. (IPEC-Nagoya-ECCE.Asia), May 2018, pp. 521–527.
[23] D. G. Holmes and T. A. Lipo, Pulse Width Modulation for Power Converters: Principles and Practice, New York, NY, USA: Wiley, 2003.
[24] D.-W. Chung and S.-K. Sul, “Minimum-loss strategy for three-phase PWM rectifier,” IEEE Trans. Power Electron., vol. 41, no. 3, pp. 517–526, Jun. 1999.
[25] A. M. Hava, R. J. Kerkman, and T. A. Lipo, “A high-performance generalized discontinuous PWM algorithm,” IEEE Trans. Ind. Appl., vol. 34, no. 5, pp. 1059–1071, Sep. 1998.
[26] Z. Zhang and L. Xu, “Dead-time compensation of inverters considering snubber and parasitic capacitance,” IEEE Trans. Power Electron., vol. 29, no. 6, pp. 3179–3187, Jun. 2014.
[27] Y. Yang, K. Zhou, H. Wang, and F. Blaabjerg, “Analysis and mitigation of dead-time harmonics in the single-phase full-bridge PWM converter with repetitive controllers,” IEEE Trans. Ind. Appl., vol. 54, no. 5, pp. 3534–3534, Apr. 2018.
[28] M. Kim, S.-K. Sul, and J. Lee, “Compensation of current measurement error for current-controlled PMSM drives,” IEEE Trans. Ind. Appl., vol. 50, no. 5, pp. 3365–3373, Sep. 2014.
[29] T. Esram and P. L. Chapman, “Comparison of photovoltaic array maximum power point tracking techniques,” IEEE Trans. Energy Convers., vol. 22, no. 2, pp. 439–449, Jun. 2007.
[30] M. A. G. de Brito, L. Galotto, L. P. Sampaio, G. E. de Azevedo e Melo, and C. A. Canesin, “Evaluation of the main MPPT techniques for photovoltaic applications,” IEEE Trans. Ind. Electron., vol. 60, no. 3, pp. 1156–1167, Mar. 2013.
HYEON-SIK KIM (Member, IEEE) was born in Busan, South Korea, in 1988. He received the B.S. and Ph.D. degrees in electrical and computer engineering from Seoul National University, Seoul, South Korea, in 2013 and 2019, respectively.

From 2019 to 2021, he was a Principal Research Engineer with Hyundai Mobis, South Korea. Since 2021, he has been with Gachon University, Seongnam, South Korea, where he is currently an Assistant Professor. His research interests include electric machine drives, electric/hybrid vehicles, and power electronic systems in various applications. He was a recipient of the 2015 Industrial Power Converter Committee (IPCC) First Prize Paper Award from the IEEE Industrial Application Society.

SEUNG-KI SUL (Fellow, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 1980, 1983, and 1986, respectively.

From 1986 to 1988, he was an Associate Researcher with the Department of Electrical and Computer Engineering, University of Wisconsin-Madison, Madison, WI, USA. From 1988 to 1990, he was a Principal Research Engineer with LG Industrial Systems Company, South Korea. Since 1991, he has been a member of the Faculty with the School of the Electrical and Computer Engineering, Seoul National University, where he is currently a Professor. He has authored or coauthored more than 150 IEEE journal articles and a total of more than 340 international conference papers in the area of power electronics. His current research interests include position sensorless control of electrical machines, electric/hybrid vehicles and ship drives, and power-converter circuits based on SiC MOSFET.

Dr. Sul was a recipient of the 2015 IEEE TRANSACTIONS 1st and 2nd Paper Awards on Industrial Application, simultaneously. He was also a recipient of the 2016 Outstanding Achievement Award of the IEEE Industrial Application Society and the 2017 Newell Award sponsored by the IEEE Power Electronics Society. He was the Program Chair of the IEEE Power Electronics Specialists Conference, in 2006, the General Chair of the IEEE International Conference on Power Electronics, and ECCE-Asia, in 2011. In 2015, he was the President of The Korean Institute of Power Electronics (KIPE). From 2011 to 2014, he was the Editor-in-Chief of the Journal of Power Electronics (KIPE), which is an SCIE-registered journal, Seoul.