TimingCamouflage+: Netlist Security Enhancement with Unconventional Timing
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Abstract—With recent advances in reverse engineering, attackers can reconstruct a netlist to counterfeit chips by opening the die and scanning all layers of authentic chips. This relatively easy counterfeiting is made possible by the use of the standard simple clocking scheme, where all combinational blocks function within one clock period, so that a netlist of combinational logic gates and flip-flops is sufficient to duplicate a design. In this paper, we propose to invalidate the assumption that a netlist completely represents the function of a circuit with unconventional timing. With the introduced wave-pipelining paths, attackers have to capture gate and interconnect delays during reverse engineering, or to test a huge number of combinational paths to identify the wave-pipelining paths. To hinder the test-based attack, we construct false paths with wave-pipelining to increase the counterfeiting challenge. Experimental results confirm that wave-pipelining true paths and false paths can be constructed in benchmark circuits successfully with only a negligible cost, thus thwarting the potential attack techniques.

I. INTRODUCTION

A major IC (Integrated Circuit) counterfeiting threat is the illegal production of chips by a third party with a netlist reverse engineered from authentic chips. In reverse engineering, authentic chips are delayed and imaged to identify logic gates, flip-flops, and their connections to reconstruct a netlist. Because the recognized netlist carries all necessary design information, this reverse engineering flow allows counterfeiters to reproduce authentic chips with much freedom.

Several techniques have been proposed to thwart reverse engineering attacks on authentic chips. The first method is IC camouflaging which tries to prevent the netlist from being recognized easily [2]. In [3] transistors are manipulated with a stealthy doping technique during manufacturing so that they function differently than they appear. In [4], the layouts of different cells are designed to be identical, leading to difficulty in interpreting the functionality of a netlist. The work in [5]–[7] mixes real and dummy contacts to camouflage standard cells so that they cannot be recognized by reverse engineering. The method in [8] explores netlist obfuscation by iterative logic fanin cone analysis at circuit level. In addition, the method in [9] introduces a quantitative security criterion and proposes camouflaging techniques with a low-overhead cell library and an AND-tree structure to strengthen netlist security. The functionality of a given design is perturbed in [10] by applying a simple transformation and a separate camouflaged block is used to recover the functionality. Moreover, the method in [11] creates logic loops by adding dummy wires and gates to obfuscate the circuit topology. However, nearly all these camouflaging methods can be deobfuscated by attacks based on Boolean Satisfiability (SAT) [12]–[14].

The second method to thwart reverse engineering is logic locking, which inserts additional logic gates, e.g., XOR/XNOR in [15], [16], AND/OR in [17], MUX in [18] and look-up tables (LUTs) in [19], into the netlist. These components can only activate the correct function of the circuit with a given key. This method is expanded in [20] to incorporate delay information into the locking mechanism. Furthermore, logic locking can be performed at sequential level to prevent the circuit from entering working states without a valid key [21]. Recently, logic locking has been applied to protect parametric behavior of circuits, e.g., pipelined processors [22], GPUs [23] and analog circuits [24]. The method in [22] adds meaningless clock cycles to camouflage a design, where only correct keys allow a high timing performance. However, various attack methods, e.g., SAT attack [25], removal attack [26] and bypass attack [27] can potentially recognize the correct keys.

Beyond the techniques described above, other methods, e.g., watermarking [28], metering [29] and split manufacturing [30], [31], can also be applied against counterfeiting. But the purpose of these methods is primarily to prevent overproduction and they need to be adapted properly to counter reverse engineering.

The existing methods of circuit protection either make the netlist more difficult to be recognized, or make the correct behavior of the circuit dependent on additional input information even after the netlist is recognized. In this paper, we propose a new perspective to counter counterfeiting based on reverse engineering. Our contributions are as follows.

- A new dimension of IC camouflaging is proposed to secure circuit netlists by integrating unconventional timing information. A camouflaged netlist thus only works correctly with a given set of timing information, which, however, is difficult to be recognized exactly by reverse engineering.
- To integrate unconventional timing into a netlist, wave-pipelining paths are constructed in some parts of a circuit. To prevent the exposure of these paths resulting from clustering, the retiming technique is deployed to spread them across a circuit by blocking the paths not related to wave-pipelining construction.
• With the retiming technique, the area overhead to construct wave-pipelining paths can also be reduced, since paths not related to wave-pipelining construction are maintained as single-period to avoid unnecessary delay insertion.

• A camouflaged netlist with wave-pipelining only contains normal logic gates, so that it is challenging for attackers to isolate and then identify the locations of wave-pipelining. An attack method based on path delay test to locate the camouflaged wave-pipelining paths would require a large number of test vectors.

• The introduced wave-pipelining false paths obstruct the test-based counterfeiting methods further, because some paths that are originally testable are camouflaged as false paths in the netlist.

• The proposed method is fully compatible with other security techniques introduced previously, so that they can be combined together to strengthen netlist security at circuit level.

The rest of this paper is organized as follows. In Section II, we explain the motivation and the basic idea of the proposed method. In Section III, we provide a detailed description of the wave-pipelining technique. In Section IV, we analyze potential attack techniques to identify or circumvent wave-pipelining paths introduced into the circuit. We also discuss the limitations of these techniques and propose countermeasures to thwart the attack attempts. We describe the implementation details to construct wave-pipelining paths in Section V. Experimental results are reported in Section VI. Conclusions are drawn in Section VII.

II. MOTIVATION AND BASIC CONCEPT

Digital circuits rely on their structures to define their functions. A netlist is usually sufficient to reproduce a correctly working circuit. To prevent the netlist from being recognized by reverse engineering, techniques from physical level to netlist level can be applied to camouflage the logic. These methods, however, are still confined within the conventional single-period clocking timing model, so that attackers only need to recognize the netlist correctly.

In the conventional clocking timing model, all the paths in a combinational block operate within one clock period. We call them single-period clocking paths. Figure 1(a) shows an example of a conventional sequential circuit with three flip-flops F1, F2 and F3. The data switching activities at internal points A, B, C and D in this circuit are illustrated in Figure 1(b). We assume that data are latched into flip-flops at the rising clock edge. At time 0, the input data of F1 is transferred to its output and becomes stable after \( t_{eq} \), the clock-to-q delay of F1, shown as data\(_{a_1}\). It travels further through the logic gates and reaches B, shown as data\(_{b_1}\) in Fig. 1(b). Although the data at B is stable far before the next rising clock at time T, it is still blocked at F2 until the arrival of the next rising clock edge to be transferred to the output of F2. At this clock edge, the second data wave is injected onto the path from A to B by F1 and starts to propagate. In this way, combinational logic blocks are isolated by flip-flops and data waves are pipelined to propagate through the logic blocks in the conventional digital design.

A side effect of the sequential isolation with flip-flops above is that the netlist carries all logic information. This simplification allows attackers to counterfeit chips relatively easily, because they only need to recognize the logic types of gates, flip-flops, and interconnect connections with reverse engineering.

To thwart the potential netlist attack attempt described above, we propose to invalidate the conventional timing model in the circuit under protection. For example, we can remove the flip-flop in the middle of Fig. 1(a) to construct the circuit structure shown in Fig. 2(a). The switching activities of the internal signals in Fig. 2(a) are illustrated in Fig. 2(b). At two consecutive rising clock edges, F1 injects data\(_{a_1}\) and data\(_{a_2}\) onto the combinational path, respectively. Therefore, two data waves at A are always separated by one clock period. Since no flip-flop blocks the propagation of data\(_{b_1}\), it passes through C directly and reaches D after traveling through the inverter and OR gate. Once the data at D becomes stable as data\(_{d_1}\), it waits to be latched by F3 while the second data wave is propagating. To avoid that data\(_{d_1}\) is flushed by the following data waves, the delays of all the combinational paths passing through B and C, including those between F1
and F3, must be larger than one clock period. Otherwise, the change of the data at D triggered by the second data wave data \( d_{2} \) happens before the next rising clock edge, so that the previous data \( d_{1} \) waiting at the input of F3 cannot be latched correctly. The result of flip-flop removal is that two data waves propagate along the path without a flip-flop separating them. This technique is called wave-pipelining (WP) and has previously been investigated for circuit optimization as in, e.g., [32]–[35].

With wave-pipelining paths, the function of the circuit depends on both its structure and the timing information of combinational paths. If attackers obtain a netlist as in Fig. 2(a), they need to determine whether these paths are single-period clocking paths or wave-pipelining paths. If attackers assume the former and process the netlist using a standard EDA flow, the circuit loses synchronization, because the data at the input of F3 is latched one clock period earlier than in the original design. If attackers want to determine whether it is the latter case, additional effort is required to extract the timing information for each combinational path in the circuit.

Though attackers may have access to the standard cell library, e.g., through a third-party IP vendor, it is still very hard to obtain accurate interconnect/RC parasitics by delaying authentic chips, due to unknown process parameters, challenges in 3D RC extraction, and switching-window-dependent crosstalk-induced delay variations, etc. In any case, the more accurate the original timing information should be recognized from delayed chips, the harder and more expensive it becomes to reproduce a design. Therefore, this unconventional timing concept has a potential to open up a new dimension of netlist security and can be combined with the existing camouflaging techniques, e.g., through dopant-level camouflage [3], or dummy contact insertion [5]–[7].

III. WAVE-PIPELining CONSTRAINTS

A wave-pipelining path such as the one in Fig. 2(a) allows two data waves to propagate on the path simultaneously. Since the second data wave must not catch the first one, special timing constraints should be imposed for this path.

When creating wave-pipelining paths, a flip-flop in Fig. 2(a) is removed to construct the circuit in Fig. 2(a). In practice, this operation may lead to many paths with wave-pipelining, because any combinational path through B and C becomes a new wave-pipelining path. When the setup time \( t_{su} \) and the hold time \( t_{h} \) of the flip-flop are considered, all these paths \( P \) should meet two constraints. First, the delay \( d_{p} \) of a path should be \( t_{h} \) larger than the clock period \( T \). Otherwise, the second wave arrives at the flip-flop too early and thus disturbs the latching process of the first wave. Second, the delay of the path should be \( t_{su} \) smaller than \( 2T \) to guarantee that the data is latched by F3 correctly. The timing constraints for all these paths can be written as

\[
d_{p} \geq T + t_{h}, \forall p \in P \iff \min_{p \in P} (d_{p} - t_{h}) \geq T \tag{1}
\]

\[
d_{p} \leq 2T - t_{su}, \forall p \in P \iff \max_{p \in P} (d_{p} + t_{su}) \leq 2T. \tag{2}
\]

If all the wave-pipelining paths meet the two constraints (1) and (2), the wave-pipelining version of the circuit after a flip-flop is removed is functionally equivalent to the original circuit.

IV. POTENTIAL ATTACKS AND COUNTERMEASURES

The proposed camouflage technique with wave-pipelining secures netlists with timing information at sequential level. This new technique may face potential attacks. We analyze some of these attacks in this section, though their experimental attempt is not covered in this manuscript. In the assumed attack model, the available information includes a netlist recognized by reverse engineering and estimated delays of logic gates as well as interconnects with an inaccuracy factor \( \tau \). The objective of the attack is to identify on which combinational paths in the netlist wave-pipelining is applied.

1) First Attack Technique – Delay Estimation

In this method, the delays of all the gates and interconnects are measured while the netlist is reverse engineered. Using the measured delays, path delays can be estimated from the netlist. Since the delays of wave-pipelining paths are between \( T \) and \( 2T \) as defined in (1) and (2), these paths can therefore be identified. The challenge of this attack technique is that it is difficult to extract accurate gate and interconnect delays just from reverse engineering, due to the inaccuracy in delaying authentic chips described in Section II. Assume that the real delay of a path is \( d \), including setup time of a flip-flop, and the delay recognition technique suffers an inaccuracy factor \( \tau (0 < \tau < 1) \). Consequently, this path delay can be any value in the range \([((1-\tau)d, (1+\tau)d)]\). If the upper bound of an estimated delay is smaller than \( T \), this path is definitely a single-period clocking path. If the lower bound of an estimated delay is larger than \( T \), the path is definitely a wave-pipelining path. However, if no such clear decision can be made with the estimated delay, namely,

\[
(1-\tau)d \leq T \leq (1+\tau)d \tag{3}
\]

this path can only be considered as suspicious of wave-pipelining. In the following, we call the range \([(1-\tau)d, (1+\tau)d)]\) the gray region for a path with delay \( d \). In reality, a well-optimized design contains a huge number of critical paths with delays close to the clock period \( T \), so that their gray regions often surround \( T \). When constructing wave-pipelining paths in the proposed method, we also guarantee that their delays are in the gray region to counter this attack technique.

2) Second Attack Technique – Testing Delays

With the estimated delays, attackers can actually narrow down the number of potential wave-pipelining paths, because paths with estimated delays definitely smaller or larger than \( T \) can be screened out. The second attack technique is thus to test the delays of the remaining suspicious paths using authentic chips from the market. With the netlist recognized, it is not difficult to determine test vectors to trigger the remaining suspicious paths. Since the only information of interest is whether a path delay is larger than \( T \), only one delay test for each path is required.

To prevent all suspicious paths from being tested as described above, we introduce a countermeasure to create unsensitizable paths with wave-pipelining. When we construct wave-pipelining paths by removing flip-flops, we prefer the paths that, viewed directly with the conventional single-period
clocking model, are false paths, which cannot be sensitized by any test vector.

**Definition 1.** False Path: A combinational path which cannot be activated in functional mode or tested due to controlling signals from other paths \([36], [37]\).

**Definition 2.** Wave-Pipelining False Path (WP False Path): A combinational path with wave pipelining that is a false path when viewed with the conventional single-period clocking model.

**Definition 3.** Wave-Pipelining True Path (WP True Path): A combinational path with wave pipelining that is a true path when viewed with the conventional single-period clocking model.

Wave-pipelining false paths have two data waves propagating along them when the circuit is operating, but they are false paths when the netlist is examined assuming the conventional single-period clocking model. An example of a wave-pipelining false path is shown in Fig. 3, which is a snippet of the s298 circuit from the ISCAS89 benchmark set. When the flip-flop in the middle is removed, the dashed path becomes a wave-pipelining path. If attackers view it as a single-period clocking path in the extracted netlist, this dashed path is also a false path. In this case, a signal switching at the beginning of the dashed path never reaches the final flip-flop. If the signal \(v_2\) has a value ‘1’, which is the controlling signal to an OR gate, it blocks the signal switching along the dashed path at the last OR gate; If the signal \(v_2\) has a value ‘0’, it blocks the signal switching along the dashed path at the AND gate right away. Consequently, the dashed path cannot be triggered for delay test and attackers have no way to differentiate it from all the other false paths in the original circuit, which may contribute up to 75% of all the combinational paths in real circuits \([38]\).

3) Third Attack Technique – Logic Simulation

Since the delays of false paths cannot be tested, brute-force logic simulation could be applied to differentiate the camouflaged false paths from real false paths. In this method, each false path that cannot be excluded by delay screening in the first step can be assumed to be a real false path or a wave-pipelining false path, so that attackers have to verify which assumption is correct for this false path with simulations. Assuming the number of such paths is \(n\). If each path in \(n\) can be a real false path or a wave-pipelining false path, then \(2^n\) simulations of the complete circuit have to be performed to check which combination is correct. In theory, this method can eventually find the correct combination of real false paths and wave-pipelining false paths. However, it is still impractical because of the unaffordable simulation time due to the large number of false paths in the original design \([36], [38]\), e.g., 728262 for s13207 in the ISCAS89 benchmark set, and the long runtime for a full simulation of the complete circuit.

4) Fourth Attack Technique – Sizing False Paths

In this method, all false paths in the circuit are considered as wave-pipelining paths and logic gates are sized so that delays of all these paths meet the constraints \([1]\) and \([2]\).
gates can be replaced with high $V_i$ counterparts to enlarge their delays. Consequently, attackers cannot determine the locations of wave-pipelining paths according to the number of logic gates.

7) Seventh Attack Technique – SAT-based Attack

In the SAT-based attack methods, e.g., [14, 43], it is assumed that attackers have full access to the scan chain, so that they can apply input test vectors and observe the outputs with the authentic chips. With various sets of input and output observations, the SAT-based attack can determine the locations of wave-pipelining paths that match all input and output observations. In fact, wave-pipelining true paths can be screened out with this method, since these paths can be triggered with the at-speed testing. However, the constructed wave-pipelining false paths cannot be triggered for delay test if they are considered to work within one clock period. If attackers try to activate such paths with two consecutive data waves, all the side-inputs of the wave-pipelining false paths should be set to non-controlling values in two consecutive clock cycles. For example, $v_2$ in Fig. 3 is one of the side-inputs of the dashed wave-pipelining false path. It should be set to 1 in the first clock cycle to allow a signal switching through the AND gate. In the second clock cycle, it should be set to 0 so that the signal switching can pass through the OR gate. These requirements might be met by tracing logic blocks between two flip-flop stages before F1. The traced logic blocks should be set to appropriate values so that all the side-inputs ensure the activation of the wave-pipelining false paths. However, this method requires drastic changes in the existing testing platform. In addition, the delays of original false paths in the circuits might be larger than the given clock period since they are ignored during timing analysis. By triggering the conflicting logic with two clock cycles, these paths can also be activated with two consecutive data waves, so that the constructed wave-pipelining false paths can be concealed. Furthermore, TimingCamouflage+ can be combined with other existing methods such as scan chain encryption [44, 45], to further increase the difficulty of activating wave-pipelining paths.

To differentiate wave-pipelining false paths from original false paths with SAT-based attacks, the whole circuit can be considered as a black box, where only the data at the primary inputs and the primary outputs of the design can be observed. Since identifying wave-pipelining false paths requires to determine where the flip-flops are removed, attackers can first collect connections between gates along all suspicious false paths and then determine where to re-insert flip-flops to recover the original circuit without wave-pipelining. To identify the correct combinations of inserting flip-flops, SAT-based attacks search iteratively for discriminating input sequences at the primary inputs. Each discriminating input sequence eliminates one or more combinations of inserting flip-flops. The iteration continues until only the correct combination of inserting flip-flops remains. In [46, 47], similar attacks have been attempted onto sequential circuits, and it has been demonstrated that it is not possible to decamouflage relatively large sequential circuits even with smaller numbers of keys compared with TimingCamouflage+. Furthermore, TimingCamouflage+ actually introduces a new dimension in netlist camouflaging. Therefore, it can also be combined with other security methods, e.g., Anti-SAT logic locking [48, 49], to counter SAT-based attacks together.

Recently, a Satisfiability Modulo Theory (SMT)-based attack method is proposed to enhance SAT-based attack with theory and graph solvers [50]. However, it is assumed that all combinational paths work within one clock period. This assumption does not hold in TimingCamouflage+, where the intentionally constructed wave-pipelining paths have delays larger than one clock period. To extract correct timing constraints of such wave-pipelining paths, their locations have to be identified, which requires much effort as discussed above.

V. WAVE-PIPELINING CONSTRUCTION

When constructing wave-pipelining paths in a circuit while maintaining its original function, we need to guarantee that the constructed paths meet the timing constraints (1) and (2). To counter the attack techniques discussed in Section IV, the constructed paths should meet the constraint (3), so that they cannot be verified easily. Furthermore, the wave-pipelining paths should contain false paths when viewed as single-period clocking paths. The wave-pipelining construction problem can thus be formulated as follows.

**Inputs:** Original optimized design; gate and interconnect delays; the given clock period $T$; the delay recognition inaccuracy factor $\tau$ ($0 < \tau < 1$); the required number of wave-pipelining false and true paths $n_{wpf}$, $n_{wpt}$; distance threshold $d_{IS}$.

**Outputs:** A revised design containing at least $n_{wpf}$ wave-pipelining false paths and $n_{wpt}$ wave-pipelining true paths, where $n_{wpf}$ and $n_{wpt}$ are user-defined parameters. These wave-pipelining paths should meet the timing constraints (1) and (2) as well as the gray region requirement (3).

**Objectives:** The original function of the circuit should be maintained; the original design should be kept unchanged as much as possible; the increased resource usage should be as little as possible; the physical distances between the constructed wave-pipelining paths should be as far as possible to prevent the exposure of these paths resulting from clustering.

When constructing wave-pipelining paths, we incorporate PVT (Process, Voltage and Temperature) variations by allowing path delays to deviate from their original values. Specifically, delays of longest paths are enlarged to $(1+\delta)$ times of the original values. On the contrary, delays of shortest paths are reduced to $(1-\delta)$ times of the original values. The value of $\delta$ should be determined by designers according to the corresponding manufacturing technology. With this setting, the constructed wave-pipelining paths should still work correctly under PVT variations.

A. Work flow of wave-pipelining construction

The major steps to construct wave-pipelining paths are shown in Fig. 4. Wave-pipelining paths can potentially be constructed at a flip-flop connected to paths with large delays, so that timing constraints (1) and (2) of such paths can be satisfied easily. Therefore, we sort all flip-flops in a circuit in a decreasing order according to the sum of the maximum delays.
of their incoming and outgoing paths as described above. In addition, wave-pipelining construction might be challenging at those flip-flops with a large number of incoming and outgoing paths, because a huge number of wave-pipelining paths can appear when the flip-flop is removed. To guarantee all these wave-pipelining paths to meet the timing constraints (1) and (2) is difficult, because these constraints require that all the path delays should be within the range of \( T \) and \( 2T \) simultaneously. Therefore, such flip-flops with large numbers of incoming and outgoing paths should be filtered out. Since traversing all incoming and outgoing paths of a flip-flop to acquire their numbers is time-consuming, we use the numbers of source and sink flip-flops of a flip-flop to indicate the difficulty in constructing wave-pipelining paths. Therefore, flip-flops with the number of source or sink flip-flops larger than a given threshold are filtered out to accelerate the construction.

After sorting and filtering flip-flops, for each remaining flip-flop \( f_i \), we check whether there are wave-pipelining false paths that can be formed from single-period true paths on the left and on the right of \( f_i \) (L7). The number of such paths is stored in \( n_f \). If wave-pipelining false paths cannot be formed at \( f_i \), the function construct_WP_paths\((f_i, T, \tau)\) is used to construct such paths eventually with the combinational logic leaving from and arriving at it. The identified logic gates are also expanded to include all the gates reachable from them, because sizing the logic gates on the wave-pipelining paths also affects delays of paths through the expanded gates. All these gates are denoted together as a set \( G \). The details of this construction will be explained later.

As shown in Fig. 2(a), for a wave-pipelining path, the flip-flop at the beginning of the path and the flip-flop at the end of the path should not be removed from the circuit during constructing of further wave-pipelining paths. Otherwise, paths with more than 2 waves may appear, requiring more complex timing constraints. These fanin and fanout flip-flops are inserted into the set \( F_w \) (L10) and all the flip-flops tracked by \( F_w \) cannot be considered as candidates to construct wave-pipelining paths. In addition, the physical distance between the

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### Algorithm

| Step | Description |
|------|-------------|
| L1   | Input: netlist, delay information, \( T, \tau, n_{wpf}, n_{wpt}, dist \), construct wave-pipelining true paths similar to L5–L15. |
| L2   | Sort all flip-flops \( F \) in a decreasing order; |
| L3   | Filter \( F \rightarrow F_i \) using the number of source/sink flip-flops; |
| L4   | For \( i = 1 \) to \( |F_i| \) do |
| L5   | If a flip-flop \( f_i \) \( \notin F_w \) then |
|      | \( n_f = \text{check\_WP\_false\_paths}(f_i, T, \tau) \); |
|      | If \( n_f > 0 \) then |
|      | If construct\_WP\_paths\((f_i, T, \tau)\) is false, go to L5; |
|      | \( F_w \leftarrow f_i \); |
|      | If \( (DIS(f_i, f_j)) < dist \) then \( f_i \) and \( f_j \) are other flip-flops |
|      | \( n_{wpt} = n_{wpf} - n_f \); |
|      | If \( n_{wpt} \leq 0 \) then break; |
|      | end |
|      | end |
| L6   | end |
| L7   | Construct wave-pipelining true paths similar to L5–L15. |

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![Figure 5: The number of paths on each side of \( f_i \) is limited to 500. Wave-pipelining paths should be large to prevent the exposure resulting from the clustering of such paths. We use the distances between flip-flops to represent the distances between wave-pipelining paths. Therefore, a flip-flop \( f_j \) whose distance to \( f_i \) that is currently used to construct wave-pipelining is smaller than \( dist \) cannot be a candidate for wave-pipelining, so that it is inserted into the set \( F_w \).](image-url)
C. Retiming to facilitate wave-pipelining construction

With the false path checking method described above, we can check whether wave-pipelining false paths can be formed from the selected single-period true paths on the left and right of flip-flop $ff_i$. If such wave-pipelining false paths can be formed, we mark the original single-period clocking true paths forming them as relevant paths. Other single-period clocking paths are called irrelevant paths. An example of the relevant and irrelevant paths is shown in Fig. 6(a). To construct wave-pipelining with relevant paths, the flip-flop $ff_i$ in the middle can be removed. Unfortunately, the removal of $ff_i$ makes all the paths connected with it wave-pipelining. Since many short paths may exist on the left and on the right of $ff_i$, connecting them by removing $ff_i$ directly generates many paths whose delays are too small to meet the lower bound of the wave-pipelining constraint (1). In addition, the removal of the flip-flop leads to a clustering of wave-pipelining paths, which are vulnerable to be identified by attackers. Fig. 6(a) illustrates a construction example, where a wave-pipelining false path is formed from the relevant paths after $ff_i$ is removed. However, the irrelevant paths on the left and the right of $ff_i$ lead to unnecessary wave-pipelining generation. To deal with the challenges, we try to maintain the irrelevant paths on the left and right of $ff_i$ to be single-period as much as possible.

To maintain the irrelevant paths as single-period clocking paths, we apply the retiming technique [54] to block these paths with flip-flops. Retiming transforms the structure of a circuit by moving the locations of flip-flops while preserving the function of this circuit. This concept is illustrated in Fig. 6(b), where the flip-flop $ff_i$ is moved to the left of the OR gate. To maintain the original structure of the circuit, a flip-flop is inserted at each input of the OR gate.

The concept of retiming can be explained using Fig. 6. To apply this technique, we use $g \in G$ to represent a combinational gate and a net $e \in E$ to represent the net connecting the output of a combinational gate and an input of another combinational gate. The delays from the input pins of a gate to its output pin are different, due to the internal structure of the gate. Therefore, these delays should be set individually according to the corresponding lookup table. Since the input pins of a gate appear along different combinational paths, we use $d^p_{eg}$ to represent the pin-to-pin delay for gate $g$ along the path $p$. Interconnect delays can be modeled as extra nodes between nets, similar to combinational gates. Each net $e_{g_i,g_j}$ between gates $g_i$ and $g_j$ has a weight $w(e_{g_i,g_j})$ to represent the number of flip-flops along the connection. Assume that between two gates $g_i$ and $g_j$, there is a path $p$. The propagation delay of this path is equal to the sum of the delays of the gates on the path, expressed as follows:

$$d(p) = \sum_{k=1}^{n} d^p_{eg_k}$$  \hspace{1cm} (4)

where $n$ is the number of gates on the path. Furthermore, the weight of a path $p$, representing the total number of flip-flops on the path, is defined as the sum of the weights of the nets along the path, expressed as:

$$w(p) = \sum_{k=1}^{n-1} w(e_{eg_k})$$  \hspace{1cm} (5)

The goal of retiming is to find an assignment of an integer $r(g)$ for each gate $g$ to transform a circuit to another functionally equivalent circuit. $r(g)$ defines how many flip-flops are moved from the output of a gate to its inputs. In Fig. 7(a), the combinational gate is retimed by -1 if the flip-flops at its inputs are moved to its output. In this case, the integer $r(g)$ of the gate is equal to -1. On the contrary, the integer $r(g)$ of the gate is 1, if the flip-flop at its output is moved to its inputs.

After retiming, the number of flip-flops on a net between gates $g_i$ and $g_j$ is written as $w_{r}(e_{g_i,g_j}) = w(e_{g_i,g_j}) + r(g_j) - r(g_i)$. Two retiming cases are shown in Fig. 7(b). In the first case 1, the flip-flop at the output of $g_j$ is moved to its inputs, so that the number of flip-flops between $g_i$ and $g_j$ can be derived as $w_{r}(e_{g_i,g_j}) = w(e_{g_i,g_j}) + r(g_j) - r(g_i) = 0 + 1 - 0 = 1$. In the second case 2, the flip-flops at the inputs of $g_j$ are moved to its output further, so that the number of flip-flops between $g_i$ and $g_j$ is increased to $w_{r}(e_{g_i,g_j}) = w(e_{g_i,g_j}) + r(g_j) - r(g_i) = 0 + 1 - (-1) = 2$. For a legal retiming, the retimed weight $w_{r}(e_{g_i,g_j})$ must be non-negative. To meet a given clock period $T$ for a retimed circuit, any path $p$ with a delay larger than the given clock period $T$ should have a retimed weight $w_{r}(p)$ larger than 0 to guarantee there is a
The output of this gate, denoted as $g_j$, from a flip-flop travels through the longest path and arrives at the latest and the earliest arrival times at the output of a flip-flop, $d_j$. Therefore, it is not straightforward to determine the optimal locations to apply retiming to construct wave-pipelining. To enlarge the delays of these paths to meet the lower requirement (3), all the other wave-pipelining paths resulting from the removal of $ff_j$ are also guaranteed, because the arrival times of other paths are bounded between them.

Since we do not know at which location the retiming should be performed to construct wave-pipelining paths, a variable $y_{g_i, g_j}$ is assigned for each net $e_{g_i, g_j}$ to indicate whether the retimed flip-flop on this net can be removed, with $y_{g_i, g_j} = 1$ to indicate that the retimed flip-flop is removed and vice versa. If there is no retimed flip-flop on $e_{g_i, g_j}$, $y_{g_i, g_j}$ should be set to 0. Consequently, the relation between $y_{g_i, g_j}$ and the number of retimed flip-flops $w_r(e_{g_i, g_j})$ on this net can be established as follows:

$$y_{g_i, g_j} \leq w_r(e_{g_i, g_j}).$$

With this setting, three representative cases for a net between gates $g_i$ and $g_j$ should be examined, as shown in Fig. 10.

**Case 1:** The net from gate $g_i$ to gate $g_j$ has the retimed weight $w_r(e_{g_i, g_j}) = w(e_{g_i, g_j}) + r(g_j) - r(g_i) = 1$, and thus a retimed flip-flop $ff_{k}$ exists along this net. The retimed flip-flop is not removed, denoted as $y_{e_{g_i, g_j}} = 0$.

**Case 2:** The net from gate $g_i$ to gate $g_j$ has the retimed weight $w_r(e_{g_i, g_j}) = w(e_{g_i, g_j}) + r(g_j) - r(g_i) = 1$, but the flip-flop is removed, denoted as $y_{e_{g_i, g_j}} = 1$.

**Case 3:** The net from gate $g_i$ to gate $g_j$ does not have a retimed flip-flop, $w_r(e_{g_i, g_j}) = 0$. In this case, the data at the output of $g_i$ passes through $g_j$ directly.

When removing flip-flops combined with retiming, each of the cases above can happen. We let the solver determine which case actually happens during wave-pipelining construction. After this construction, no flip-flop should appear on the relevant paths. Consequently, if there is a retimed flip-flop on a net along a relevant path $w_r(e_{g_i, g_j}) = 1$, this flip-flop should be removed, so that $y_{e_{g_i, g_j}} = 1$. Accordingly, the following constraints should be met:

$$w_r(e_{g_i, g_j}) = y_{e_{g_i, g_j}}, \quad \forall e_{g_i, g_j} \in E$$

**Detailed timing constraints of each case are explained in Appendix.**

**Figure 8:** Removal of flip-flops together with retiming. (a) $ff_j$ is removed for wave-pipelining construction. (b) Wave-pipelining paths can be constructed from the relevant paths and a small number of irrelevant paths after the retimed flip-flop $ff_j$ is removed.

**Figure 9:** The latest and the earliest arrival times of $g_j$. The net from gate $g_j$ is the minimum delay with which the data from a flip-flop travels through the shortest path and arrives at the output of this gate, denoted as $s_{g_j} = \min\{d_1, d_2, d_3\}$. To tolerate PVT variations, For the wave-pipelining paths after a flip-flop is removed, shown in Fig. 8(b), if the latest and the earliest arrival times at points A, B, C satisfy the timing constraints (1)–(2) and the gray region requirement (3), all the other wave-pipelining paths resulting from the removal of $ff_j$ are also guaranteed, because the arrival times of other paths are bounded between them.

**Figure 10:** Removal of a retimed flip-flop.
We thus formulate the wave-pipelining construction problem as follows

\[
\text{Minimize} \quad \alpha \sum_{g \in G} \xi_g - \beta \sum_{g \in G} \sum_{i=1}^{n_g} d_i^g + \gamma \sum_{g \in G} r(g)(\# \text{input of } g - \# \text{output of } g) 
\]

Subject to

(6) and gray region constraints

Case 1 constraints, if \( w_r(e_{g_i,g_j}) + y_{e_{g_i},g_j} = 1 \)

Case 2 constraints, if \( w_r(e_{g_i,g_j}) + y_{e_{g_i},g_j} = 2 \)

Case 3 constraints, if \( w_r(e_{g_i,g_j}) + y_{e_{g_i},g_j} = 0 \)

where \( \xi_g \) is introduced to enlarge the delay of wave-pipelining paths, which can be implemented by lengthening interconnects. \( d_i^g \) is the delay from the \( i \)th input pin to the output pin of gate \( g \). \( n_g \) is the number of input pins for \( g \). \( r(g)(\# \text{input of } g - \# \text{output of } g) \) represents the increased number of retimed flip-flops. \( \alpha, \beta \) and \( \gamma \) are constants with \( \alpha \geq \gamma \geq \beta \) to prevent the exposure of wave-pipelining resulting from lengthened interconnects and suppress area overhead by more retimed flip-flops and gate sizing. The conditional constraints (12)–(10) can be converted into linear constraints as described in [55].

Since only one flip-flop is used to construct wave-pipelining at a time and other flip-flops are kept in the circuit as shown in Fig.8(b), the part of a circuit around this flip-flop for wave-pipelining construction is not large. Therefore, we solve (9)–(10) directly with an ILP solver to construct wave-pipelining.

E. Wave-pipelining construction with duplication combined with retiming

The wave-pipelining construction by applying the removal of flip-flops combined with retiming described above might not be achieved successfully for a flip-flop \( ff_j \), due to the circuit structure and the restriction on the area overhead incurred by lengthening interconnects, so that the ILP formulation (9)–(10) may return no solution. To solve this problem, retiming is first applied to block irrelevant paths as much as possible and the circuit is duplicated in part to bypass such paths further to facilitate wave-pipelining construction. To implement the first step, the variable \( y_c \), which indicates whether the retimed flip-flop on a net is removed, should be set to 0 for all nets in a circuit to guarantee that all paths are still single-period. The original flip-flop \( ff_i \) should be moved to its left side to block irrelevant paths as much as possible with the formulation (9)–(10), as shown in Fig.11(a). This leftward movement of flip-flops leads to fewer logic gates to be duplicated, as shown in Fig.11(b).

In the second step, after retiming, we duplicate the logic in the circuit and size the gates and lengthen interconnects so that the delays of all wave-pipelining paths meet timing constraints (1)–(3) as illustrated in Fig.11(b). In the duplicated circuit on the right of retimed flip-flops, we only keep the flip-flops at which wave-pipelining paths terminate. The other flip-flops stay in the original circuit. Afterwards, we delete the logic gates backwards to remove those gates that do not drive any flip-flop to reduce resource usage. When duplicating the logic on the left of \( ff_j \), however, we need to keep all the logic gates to maintain the correct function of the circuit.

In the duplicated logic in Fig.11(b), we do not duplicate flip-flops. Therefore, all combinational paths in the duplicated logic are wave-pipelining paths and their delays should meet the timing constraints (1)–(3). To meet these constraints, we size the gates and lengthen interconnects in the duplicated logic with an ILP formulation. For example, in Fig.11(b), we assume the latest and the earliest arrival times at the output of the inverter in the duplicated circuit as \( \tau_{g_i} \) and \( \xi_{g_j} \). Similarly, we assume the latest and the earliest arrival times at the output of the AND gate in the duplicated circuit as \( \tau_{g_i} \) and \( \xi_{g_j} \). Furthermore, the delay from an input pin to the output pin of the AND gate along the path \( p \) traveling through the inverter is written as \( d_{g_j}^p \). With these definitions, the arrival times between the inverter and the AND gate can be written as

\[
\tau_{g_j} \geq \tau_{g_i} + \xi_{g_i} + d_{g_j}^p \\
\xi_{g_j} \leq \tau_{g_i} + \xi_{g_i} + d_{g_j}^p .
\]

(13)

(14)

To reduce the number of duplicated gates, we try to connect the output pins of logic gates in the duplicated logic to the original gates as much as possible, as illustrated in Fig.11(b). In the original logic, the latest and the earliest arrival times are constants. Assume that the arrival times at the output of the inverter in the original circuit are \( \tau_{g_i}^E \) and \( \xi_{g_i}^E \), and a 0-1 variable \( p_i \) indicates whether the output pin in the duplicated logic should be driven by the original logic. We can then extend the constraints (13)–(14) as

\[
\tau_{g_j} \geq \tau_{g_i}^E + d_{g_j}^p + \xi_{g_i} - p_i M \\
\tau_{g_j} \geq \tau_{g_i}^E + d_{g_j}^p + \xi_{g_i} - (1 - p_i) M \\
\xi_{g_j} \leq \tau_{g_i}^E + d_{g_j}^p + \xi_{g_i} + p_i M \]

(15)

(16)

(17)

(18)

where \( M \) is a very large positive constant used to transform the conditional constraints to linear constraints [56]. In either case when an output pin in the duplicated logic is connected or disconnected with the original logic, only two constraints
In (15)–(18) are valid.

In the description above, we allow a path delay to be extended with lengthening interconnects. However, we try to keep the delay incurred by interconnects as small as possible. In addition, we try to reduce the overall area overhead when implementing wave-pipelining. Therefore, we formulate the construction problem as

\[
\begin{align*}
\text{minimize} & \quad \alpha \sum_{g \in G} \xi_g - \beta \sum_{g \in G} \sum_{i=1}^{n_g} d_{ij} - \gamma \sum_{i \in I} p_i \\
\text{subject to} & \quad \gamma \geq \gamma \geq \beta \quad \text{to prevent the exposure of wave-pipelining resulting from lengthened interconnects and duplicated gates and suppress area overhead by gate sizing. In this setting, the effectiveness of camouflaging is more important than incurred delay.} \quad \text{(19)}
\end{align*}
\]

where \(\alpha \geq \gamma \geq \beta\) are larger than 100 for \(n_{wpf}\) are larger than 100 for the wave-pipelining false path construction, so that wave-pipelining circuits from the ISCAS89 benchmark set. The number of flip-flops and the number of logic gates are shown in the columns \(n_s\) and \(n_g\) in Table I, respectively. The benchmark circuits were sized using a 45 nm library. We set the timing margin \(\delta\) to 0.15 to tolerate PVT variations and the inaccuracy factor \(\tau\) of delay estimation of attackers to 0.2. To simplify the delay models, input slew and output loads are set to constant values. However, TimingCamouflage+ is independent of delay characterization and can work with any delay model. We used Gurobi [55] to solve the optimization problems.

The results of wave-pipelining path construction are shown in Table I. The column \(n_{wppt}\) shows the numbers of wave-pipelining true paths whose delays are in the gray region. These paths are used to testable paths are single-period and avoid the expensive test procedure. The column \(n_s\) shows the numbers of single-period clocking true paths whose delays meet the gray region requirement. When attackers try to detect the locations of wave-pipelining paths, these true paths need to be tested to determine whether their delays are actually larger or smaller than \(T\). The column \(\sum wpt n_{wpf} + n_t\), is the total number ofuspicious true paths that are required to be tested.

The column \(n_{wpf}\) shows the numbers of wave-pipelining false paths whose delays are in the gray region. In the experiments, we set the target numbers of wave-pipelining true and false paths both to 100 and the threshold distance \(d_{\text{disp}}\) between the flip-flops in the first line of Fig. 4 to construct wave-pipelining true and false paths to 10 times of the minimum distance between all pairs of flip-flops. We executed the construction of wave-pipelining true and false paths shown in Fig. 4 repeatedly using the method described in Section V-D and Section V-E. When we constructed wave-pipelining false paths, we also found wave-pipelining true paths in the circuit and vice versa. Consequently, the numbers of these paths shown in the columns \(n_{wppt}\) and \(n_{wpf}\) are larger than 100 for many test cases except s4863 and s1238. In s4863 there is no wave-pipelining false path and in s1238 the number of wave-pipelining paths is very small due to the limited sizes of these two circuits. In all large test cases, however, wave-pipelining paths have been constructed successfully. In practice, as the circuit size increases, more path candidates become available for the wave-pipelining false path construction, so that wave-pipelining false paths can always be constructed successfully.

The column \(n_f\) shows the number of suspicious single-period clocking false paths. Since their delays meet the gray region requirement.

| Circuit | \(n_s\) | \(n_g\) | \(n_{wppt}\) | \(n_{wpf}\) | \(n_t\) | Cost | Runtime |
|---------|----------|----------|----------------|----------------|----------|------|--------|
| s35932  | 1728     | 16065    | 579            | 80213          | 80792    | 715  | 130802 | 481.8 |
| s38584  | 1452     | 19253    | 420            | 202647         | 203067   | 2486 | 722378 | 736.2 |
| s38417  | 1636     | 22179    | 8369           | 637091         | 645460   | 9837 | 594078 | 643.8 |
| s15850  | 534      | 9772     | 1932           | 1693510        | 1695442  | 606  | 20999926 | 21000532 |
| s13207  | 669      | 7951     | 7830           | 2949311        | 302361   | 13410| 728262 | 223.4 |
| s9234   | 228      | 5597     | 282            | 5710           | 5992     | 1349 | 154825 | 362.3 |
| s5378   | 179      | 2799     | 844            | 8465           | 9309     | 706  | 467    | 114.9 |
| s4863   | 104      | 2342     | 300            | 359663         | 359963   | 0    | 70432413 | 3564.7 |
| s1423   | 74       | 657      | 278            | 7997           | 8275     | 272  | 5698   | 19.3  |
| s1238   | 18       | 508      | 4              | 381            | 385      | 2    | 849    | 0.8   |

VI. EXPERIMENTAL RESULTS

TimingCamouflage+ was implemented in C++ and tested using a 3.20 GHz CPU. We demonstrate the results using
region requirement \( \xi \), these paths are suspicious wave-pipelining false paths for attackers. The total suspicious wave-pipelining false paths are shown in \( n'_f = n_{wpp} + n_f \). To determine whether a false path is wave-pipelining or not from a huge number of suspicious paths, much effort is required as explained in Section IV since these false paths cannot be triggered for delay test.

The column \( n_p \) shows the equivalent number of inserted delays in the unit of the delay of a buffer by lengthening interconnects to enlarge wave-pipelining path delays. Since the number of inserted delays does not increase with respect to circuit size, the area cost for constructing wave-pipelining paths is negligible in relatively large circuits.

In the experiments, we constrained the inserted delay \( \xi_g \) incurred by lengthening interconnects to be no larger than the delay of three buffers for each net. With this constraint, the removal of flip-flops combined with retiming in Section V-D can only be achieved in s15850 to construct wave-pipelining paths. In the remaining circuits, this method cannot construct wave-pipelining successfully, since a few short paths still require much delay insertion to meet the timing constraint of wave-pipelining. However, the number of such paths is very small, confirmed by the total delays inserted as shown in column \( n_p \). In this case, circuit duplication combined with retiming is applied as described in Section V-E. The column \( n_d \) in Table I shows the number of logic gates duplicated to construct wave-pipelining. Since we only inserted wave-pipelining paths at a limited number of locations, generally the number of duplicated gates does not increase with respect to circuit size.

To construct wave-pipelining paths, retiming might cause an increase of the number of flip-flops, shown in column \( n_r \). This increase and the corresponding area overhead are still negligible. The last column \( t_r \) in Table I shows the runtime of TimingCamouflage+, which is acceptable because wave-pipelining construction is a one-time effort.

We also applied TimingCamouflage+ in two practical circuits, vga_lcd and pci_bridge32, from TAU 2013 variation-aware timing analysis contest. In both circuits, wave-pipelining false and true paths can be constructed successfully. Specifically, in vga_lcd, 169 wave-pipelining true paths and 138 wave-pipelining false paths were constructed with 25 inserted buffers, 60 duplicated gates and 5 more retimed flip-flops. In pci_bridge32, 206 wave-pipelining true paths and 1162 wave-pipelining false paths were constructed with 18 inserted buffers, 43 duplicated gates and 2 more retimed flip-flops.

When constructing wave-pipelining paths by lengthening interconnects, we constrained the interconnect delay \( \xi_g \) inserted before a gate \( g \). Fig. 12 shows the changes of the numbers of duplicated gates when the interconnect delays are relaxed. It is clear that with the increase of delays inserted before a gate \( g \), the number of duplicated gates required to construct wave-pipelining paths is decreased in three circuits. When the allowable number of delay units reaches 9, no circuit duplication is required for all these circuits. In s15850, duplicated gates are not even required to construct the wave-pipelining paths when the allowable number of delay units is larger than or equal to 3, due to the efficiency of the removal of flip-flops combined with retiming in Section V-D. For s38584 and s35932, the removal of flip-flops combined with retiming cannot be achieved successfully due to circuit structures. Therefore, the numbers of duplicated gates are not reduced.

In the wave-pipelining construction formulation (19)–(20), we maximize the number of output pins that can be driven by the original circuit as illustrated in Fig. 11(b). Consequently, the number of logic gates in the duplicated circuit can be reduced. Fig. 13 compares the numbers of gates in the originally duplicated circuit before the removed flip-flop in Fig. 11 and the number of gates after reduction by using the original circuit. In all test cases, the numbers of duplicated gates were reduced significantly.

In the experiments, we also simulated the gate sizing attack on the netlist as discussed in Section IV. The basic idea was that all false paths with delays falling in the gray region were treated as wave-pipelining paths and their delays were sized to meet (1)–(2). The results of this simulated attack are shown in Fig. 14, where the first bar shows the number of false paths we used to simulate the attack. The second bar shows the number of false paths that were not sized successfully. Even with such a small number of false paths from the huge set of false paths in the original circuit, no sizing attack succeeded.

TimingCamouflage in [1] uses the same timing concept to camouflage the netlists. However, it constructs wave-pipelining paths with duplicated gates without applying the retiming
itself does not carry all design information anymore, the secure circuit netlists against counterfeiting. Since a netlist is clear that TimingCamouflage+ outperforms TimingCamouflage in [1]. The comparison of computation time with TimingCamouflage+ are also smaller than those with TimingCamouflage in [1], except for s38417, in which the number of duplicated gates was constrained to be no larger than three. TimingCamouflage in [1] fails to construct the wave-pipelining paths in s1238, s4863, s15850 and s35932, as shown in Fig. 15. In the other cases, the numbers of duplicated gates with TimingCamouflage+ are also smaller than those with TimingCamouflage in [1], except for s38417, in which the number of duplicated gates is slightly larger in TimingCamouflage+. The comparison of inserted delay units are shown in Fig. 16 where the numbers with TimingCamouflage+ are consistently smaller in all test cases than with [1]. The comparison of overhead to construct wave-pipelining paths are shown in Fig. 17 where the area overhead with TimingCamouflage+ is smaller than that with TimingCamouflage in [1], except for s38417. For s1238, s4863, s15850 and s35932, wave-pipelining paths cannot be constructed successfully with TimingCamouflage with the maximum numbers of inserted delay units to be no larger than three. The power consumption is roughly proportional to the area overhead.

In TimingCamouflage+, the construction of wave-pipelining paths is accelerated by sorting and filtering flip-flops described in Section V-A. Consequently, the runtime is reduced significantly. The comparison of computation time with TimingCamouflage [1] is shown in Fig. 18. From this comparison, it is clear that TimingCamouflage+ outperforms TimingCamouflage in [1] in efficiency.

VII. CONCLUSION

In this paper, we have proposed TimingCamouflage+ to secure circuit netlists against counterfeiting. Since a netlist itself does not carry all design information anymore, the difficulty of attack has increased significantly due to additional test cost and the introduced wave-pipelining false paths. TimingCamouflage+ opens up a new dimension of netlist camouflage at circuit level, and it is fully compatible with other previous counterfeiting methods so that they can be combined together to strengthen netlist security. Future work includes experimental attempts of the attacks discussed in Section IV and the combination of the proposed camouflage method with other existing methods. Advanced timing concepts can be embedded into the netlist to enhance circuit security [57]–[61].

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Wave-pipelining Construction for TimingCamouflage+ (Appendix to [R1])

Case 1: The net from gate $g_i$ to gate $g_j$ has the retimed weight $w_r(\{e_{g_i,g_j}\}) = w(e_{g_i,g_j}) + v(r(g_j)) - r(g_i) = 1$, and thus a retimed flip-flop $f_k$ exists along this net. The retimed flip-flop is not removed, denoted as $y_{e_{g_i,g_j}} = 0$.

In this case, the circuit can operate with a given clock period $T$, if setup and hold time constraints can be satisfied, expressed as follows

$$\bar{\varsigma}_{g_i} + t_{su} \leq T$$

$$\varsigma_{g_j} \geq t_h$$

where (21) represents that the latest arrival time at $g_i$ should be stable $t_{su}$ before a rising clock edge. The earliest arrival time $\bar{\varsigma}_{g_i}$ should be larger than $t_h$ as shown in (22), so that the data can be latched by the flip-flop $f_k$, reliably.

The latest and the earliest arrival times at gate $g_j$ after the retimed flip-flop is passed through are expressed as follows

$$\bar{\varsigma}_{g_j} = t_{eq} + \xi_{g_j} + d_{g_j}$$

$$\varsigma_{g_j} \leq t_{eq} + \xi_{g_j} + d_{g_j}$$

where $t_{eq}$ is the clock-to-q delay of the flip-flop. $\xi_{g_j}$ is introduced to enlarge the delay of wave-pipelining paths, which can be implemented by lengthening interconnects, $d_{g_j}$ represents the delay from the input pin to the output pin of $g_j$ which is set individually for each input of $g_j$.

To guarantee that data traveling from $f_k$ and $f_k$ are latched by $f_k$, correctly, the latest and the earliest arrival times at $g_j$ should satisfy the following constraints

$$\bar{\varsigma}_{g_j} + t_{su} \leq T$$

$$\varsigma_{g_j} \geq t_h$$

where $\bar{\varsigma}_{g_j}$ and $\varsigma_{g_j}$ can be replaced by (23–24), so that (25–26) can be converted as follows

$$t_{eq} + \xi_{g_j} + d_{g_j} + t_{su} \leq T$$

$$t_{eq} + \xi_{g_j} + d_{g_j} \geq t_h.$$  

Case 2: The net from gate $g_i$ to gate $g_j$ has the retimed weight $w_r(\{e_{g_i,g_j}\}) = w(e_{g_i,g_j}) + v(r(g_j)) - r(g_i) = 1$, but the flip-flop is removed, denoted as $y_{e_{g_i,g_j}} = 1$.

In this case, wave-pipelining paths can be constructed between the fanin flip-flops and $f_k$, as in Fig. 10. After $f_k$, the data coming from the fanin flip-flops pass the removal point directly and travel through the gate $g_j$ afterwards. The data should arrive at $f_k$ after the first rising clock edge and before the second rising clock edge to guarantee it is latched correctly [R2]. With respect to wave-pipelining, the arrival times at $g_j$ should satisfy the following constraints

$$\bar{\varsigma}_{g_j} + t_{su} \leq 2T$$

$$\varsigma_{g_j} - t_h \geq T.$$  

Since the retimed flip-flop on the net between $g_i$ and $g_j$ is removed, the data at the output of $g_i$ travels through $g_j$ directly. Therefore, the relations between their arrival times are established as follows

$$\bar{\varsigma}_{g_j} \geq \bar{\varsigma}_{g_i} + \xi_{g_j} + d_{g_j}$$

$$\varsigma_{g_j} \leq \varsigma_{g_i} + \xi_{g_j} + d_{g_j}.$$  

By replacing $\bar{\varsigma}_{g_j}$ and $\varsigma_{g_j}$ by (31–32), (29–30) can be converted as follows

$$\bar{\varsigma}_{g_i} + \xi_{g_j} + d_{g_j} + t_{su} \leq 2T$$

and thus

$$\bar{\varsigma}_{g_i} + \xi_{g_j} + d_{g_j} - t_h \geq T.$$  

where $\bar{\varsigma}_{g_i}$ is removed in Fig. 10 should satisfy the constraints (25–26). To guarantee that the data from wave-pipelining and single-period paths are latched correctly at $f_k$, the latest arrival times at $g_j$, $\max\{\bar{\varsigma}_{g_j} + \xi_{g_j} + d_{g_j} - T, t_{eq} + \xi_{g_j} + d_{g_j}\}$, and the earliest arrival times at $g_j$, $\min\{\varsigma_{g_i} + \xi_{g_j} + d_{g_j} - T, t_{eq} + \xi_{g_j} + d_{g_j}\}$, should satisfy the following constraints

$$\bar{\varsigma}_{g_j} + \xi_{g_j} + d_{g_j} - T, t_{eq} + \xi_{g_j} + d_{g_j} \leq t_{su} \leq T$$

$$\min\{\bar{\varsigma}_{g_j} + \xi_{g_j} + d_{g_j} - T, t_{eq} + \xi_{g_j} + d_{g_j}\} \geq t_h.$$  

The wave-pipelining constraints in (31–32) for all constructed paths are met by guaranteeing the longest and the shortest constructed paths as wave-pipelining with (37–38). In addition, all constructed wave-pipelining paths should also meet the gray region constraint, so attackers cannot determine whether they are wave-pipelining or simple critical paths [R3]. For example, the wave-pipelining paths from fanin flip-flops to $f_k$, after $f_k$ is removed in Fig. 10 should satisfy the gray region constraint. To achieve this goal, with respect to wave-pipelining, the arrival times at $g_j$ should meet the following constraints

$$(1 - \tau)\bar{\varsigma}_{g_j} \leq T \leq (1 + \tau)\varsigma_{g_j}$$

where the $\bar{\varsigma}_{g_j}$ and $\varsigma_{g_j}$ can be replaced by those in (31–32), to convert (39) as follows

$$\bar{\varsigma}_{g_j} + \xi_{g_j} + d_{g_j} \leq T \leq (1 + \tau)(\bar{\varsigma}_{g_j} + \xi_{g_j} + d_{g_j}).$$  

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