Transferring data between two points is very essential in digital systems and the accuracy of the transferred data is important for some critical applications. However, errors during the transmission of data are very common in these systems. RRNS is mostly used in parallel processing environments because of its ability to increase the robustness of information passing between computer processors. This paper presents some results on multiple error detection and correction based on the Redundant Residue Number System (RRNS). The Mixed Radix Conversion (MRC) was incorporated with the Hamming Distance (HD) as a joint technique in the detection and correction of multiple bits errors. In the proposed method, it is possible to detect the exact locations of multiple bits errors and correct them using minimum hardware. An area-delay comparison analysis was done and compared with the other best-known result, which revealed that, the proposed scheme has a considerable improvement in speed by up to 68% and tends to require about 81% less hardware resources, which proves the efficiency of the proposed scheme in terms of delay and area requirements.
Multiple Bits Error Detection and Correction in RRNS Architecture using the MRC and HD Techniques

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Index Terms

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Keywords
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