Germanium electrostatic quantum dot with integrated charge detector in an MOS structure

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ABSTRACT

We report the fabrication and characterization of an electrostatic quantum dot in pure Germanium with an integrated charge measurement transistor. The device uses the Al₂O₃/Germanium interface for the confinement of carriers in the Germanium and an hybrid design with an electron quantum dot and hole transistor for the charge detection. The hole transistor, using with NiGe source and drain contacts, despite the modest low temperature carrier mobility of 450 cm²/Vs, has shown a sensitivity to the dot electric potential sufficient to detect single charges tunneling in and out of the quantum dot. The device is realized with a two level gate stack, with the top level used to attract electrons and the lower one to define the electron confinement potential and accumulate the hole transistor. The possibility to improve the device operation using an Al₂O₃/SiGe/Ge multilayer for the confinement of electrons at a smoother interface is discussed.

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Introduction

Electrons in Silicon and Germanium share the possibility to reach long spin coherence time enabled by the natural abundance of spinless nuclei and the possibility of isotope purification. While research is now focused on Silicon devices for technological advantages of this material system, Germanium based devices would have properties already recognized in the past\(^1\) that would solve some issues currently open in Silicon devices, so that the initial development efforts would be justified. The use of Germanium rich heterostructures was initially proposed for the peculiar possibilities allowed by conduction band engineering. Bulk Silicon, Germanium and any alloy of these two materials have two local conduction band minima in the \(\Delta\) and in the \(L\) crystallographic direction. Electrons in either minimum have properties, such as effective mass and Landé g-factor, substantially different, but such values are only marginally dependent on the alloy composition: as a consequence in any SiGe substrate or thin film the electronic properties are set by which conduction band local minimum is at the absolute minimum energy [\(^2\)]. The band profile is affected not only by the alloy composition, but also by the strain involved in the growth of Silicon-Germanium heterostructures. The unique property found in germanium rich heterostructures, and in particular in SiGe films grown on pure Germanium substrates, is that when the Silicon content in the epilayer is larger than 15 or 30% (depending if \((100)\) or \((111)\) substrate orientation is considered) the strain pushes the energy of the \(X\) valley at the absolute energy minimum [\(^1,3\)]. Consequently thin films where either the \(L\) or the \(X\) valley is the absolute minimum, and thus where electrons can have very different physical properties, can be grown on each other. Besides, the \(L\) valley minimum, that is the absolute minimum in Germanium like materials, has advantageous properties deriving from its symmetry properties. This minimum has a 4-fold degeneracy in the bulk, with the energy ellipsoids aligned along the \((111)\) directions. Owing to the fact that the effective mass is larger in the \((111)\) direction, the degeneracy is completely lifted in a 2D confinement structure, provided that the confinement is obtained in a plane normal to the \((111)\) direction: this is in contrast to what happens in Silicon based devices where a 2-fold degeneracy is left. Besides the in-plane mass in Germanium is smaller than in Silicon (0.082\(\times m_0\) vs 0.19\(\times m_0\) for Si and 0.063\(\times m_0\) for GaAs) allowing a larger quantum dot size, and consequently relaxing the technological requirements.

A type I alignment of the conduction and valence bands is predicted at the SiGe/Ge interface and a 55meV conduction band offset has been recently measured at the Si\(0.11\)Ge\(0.89\)/Ge interface on a (100) substrate [\(^3,4\)]. In a similar band structure it would be in principle possible to confine electrons in the Germanium substrate, but the limited barrier height requires a more complex device design. The semiconductor/dielectric interface can be a valid alternative to confine the charge carriers and quantum dot devices based on MOS structures are today being successfully realized in Silicon [\(^5,6\)]. The improvements reported on the Germanium/high-\(k\)
dielectric interface \cite{7} suggest the possibility to transfer the Silicon device design to Germanium. However the operation at very low temperature poses new difficulties that haven't been addressed in Germanium MOS devices yet, namely the realization of low temperature MOSFETs. The integration of a transistor functioning as a highly sensitive electrometer is necessary to detect the charge confined in the quantum dot, and perform the readout of the spin state through projective measurements that have been largely proven in GaAs \cite{8} and recently in Silicon \cite{9} based devices. The operation of MOS devices should not in principle be modified at low temperature, however the freeze-out of the dopants in non degenerately doped source and drain wells and the presence of energy barriers from the S-D metal to the transistor channel, that may be shallow enough to not hinder the operation at room temperature, can easily lead to failure when the device is cooled down to liquid helium temperature or lower. Virtually every metal on Germanium shows a Fermi level pinned close to the valence band \cite{10} rendering necessary a very large doping to enable carrier tunneling through the Schottky barrier. At the same time dopants in Germanium show large diffusivity and lower solid solubility \cite{11} compared to Silicon, making it difficult to reach the required high doping density. Methods suggested recently to reduce the effective barrier height at the metal-semiconductor interface \cite{12,13} didn't provide the needed improvement for operation at 4 K or below, so that failure of \textit{n}-type MOSFETs realized during the initial phases of this work was routinely observed. On the other hand the alignment of the metal level close to the Germanium valence band is favorable to the injection of holes and thus the formation of \textit{p}-MOS devices. The possibility to use hole, rather than electron, qubits has been recently studied \cite{14,15,16} as a way to reduce the influence of the nuclear spins on the spin coherence time, in particular in AlGaAs based devices, using the peculiarity of the hole wavefunction that goes to zero at the nuclei sites. This wouldn’t however be advantageous in Germanium and Silicon based devices, where isotope purification allows the complete elimination of nuclear spins. For group IV materials electrons still represent the preferred choice for the quantum information storage, allowing the use of ESR for spin rotation, having a lower in-plane mass and possibly achieving longer coherence time in semiconductors with spinless nuclei. Consequently we designed and realized a hybrid device where a \textit{p}-type transistor is electrostatically coupled to an electron quantum dot to detect the confined charge.
**Device design**

The device here reported is an MOS structure with a 2 level gate stack. The device architecture already used in Silicon MOS quantum dots [5] has been adapted for the use of carriers of opposite sign in the quantum dot and the measurement channel. The mid level gate, besides depleting the 2DEG and forming the quantum dot, is used to accumulate the transistor channel, while the top level gate is positively biased to attract electrons. The transistor gate is shaped with a small constriction (W/L= 70nm/100nm) constituting the high sensitivity region. Next to this a set of 4 gates, represented in Fig 1c, is used to shape the electron potential well. The two gates indicated as $V_b$ form an adjustable tunnel barrier to the electron reservoir, while the $V_p$ gates are used to tune the energy level in the quantum dot. The entire area represented in figure 1c is covered by the positively biased top gate, not reproduced in the picture, used to attract the electrons.

To optimize and validate the gates design we simulated the device operation with a procedure similar to what described in [17]. In Fig 1d we report the surface charge density calculated when both the hole channel and the electrons in the quantum dot are accumulated. Besides showing the formation a quantum dot for electrons closely coupled to the hole transistor this picture evidences the formation, in the area where no mid-level gates are present, of a 2DEG acting as an electron reservoir for the quantum dot. An n-type ohmic contact used to inject electrons in

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**Fig1:** a) Schematic cross-section of the device here reported. b) Gate structure of the quantum dot device, with S1, S2, D1, D2 indicating the ohmic contacts, and the gray area the mid-level gates. The top gate covers the entire device and is not represented. c) SEM image of the device in the area delimited by the dashed square in fig 1b. The arrow indicates the region where the hole current flows. d) Simulated surface charge density at typical operation condition for the formation of an electron quantum dot
this 2DEG would have less stringent requirements compared to the source and drain contacts of the transistors, so that the technological difficulties previously discussed wouldn't play a major role: indeed during the operation electrons are exchanged between the QD and the reservoir, leaving the total accumulated charge in the 2DEG constant. Even a very large contact resistance for the n-type contact would thus be tolerable: for example a $10^{12}$ $\Omega$ contact resistance would still allow accumulating the 2DEG over a $100 \times 100$ $\mu$m$^2$ area device in tens of milliseconds. Besides, even if no ohmic contacts are available, other non ideal effects such as interface defects or band-to-band tunneling may favor the promotion of electrons in conduction band, and more reliable results would be obtained accumulating the 2DEG at room temperature before cool down or generating the electrons by light absorption.

**Fabrication and characterization**

The device previously described was realized on a (100) non-intentionally doped germanium substrate. After standard cleaning procedure, Nickel was deposited on the ohmic contact regions and NiGe was formed via annealing at 400 $^\circ$C for 4 min in N$_2$ atmosphere. Next we deposited the first gate layer consisting of 44 nm Al$_2$O$_3$ by atomic layer deposition at 200 $^\circ$C. The mid level gates were defined by e-beam lithography and deposition of Ti/Au. The second gate dielectric was a stack of 44nm Al$_2$O$_3$ and 100nm SiO$_2$. The extra SiO$_2$ layer was added to reduce the capacitance of quantum dot to the top gate, increasing the charging energy and the electrometer sensitivity. Finally the top gate was defined by optical lithography and deposition of Ti/Al.

![Figure 2: Hole mobility and density measured as a function of the gate voltage at 0.37 K in a gated Hall bar device](image-url)
Device testing was performed in a $^3$He refrigerator at a base temperature of 0.37K. The performances of the hole transistor were first measured on a gated Hall bar device. At the base temperature we found that the source and drain contacts consistently maintained their ohmic behavior. The curve of Hall density vs. gate bias shows a good linear behavior. The minimum density we could measure on Hall bar was $1.2 \times 10^{12} \text{ h}^+ / \text{cm}^2$ that is evidence of a large trapping of carriers not contributing to the conduction. We also observe an increase of the threshold voltage from 4.2 to 0.37 K, further evidencing the presence of a large density of non mobile carriers. Finally, the mobility vs. gate voltage curve, reported in fig. 2, showed a peak value of 450 cm$^2$/Vs. These evidences show that the 2DHG properties are mainly influenced by the interface scattering: this is not surprising considering that our dielectric consists of Al$_2$O$_3$ deposited on the free germanium surface without use of interface layers or in situ surface cleaning.

Moving on to the properties of the charge detector, reported in figure 3a, even though the ohmic contacts constantly showed ohmic characteristics, the drain current vs. gate voltage ($I_d-V_g$) curves on this device didn't present a smooth linear behavior close to threshold, but several peaks and valley characteristic of the Coulomb blockade regime that evolved to a linear characteristic when the gate was made more negative. While the transistor gate was not

![Graph showing Drain current vs. Gate voltage and Id vs. Top gate voltage](image)

**Fig3:** a) Source-Drain current vs. Gate voltage through the charge measurement transistor evidencing a coulomb blockade regime at low gate overdrive. The straight line is computed with the threshold voltages measured on the Hall bar, a mobility of 450 cm$^2$/Vs and the geometric aspect ratio of the transistor gate. b) $I_d$ vs. top gate voltage measure near threshold showing a clear single hole transistor behavior.
shaped to form a quantum dot, this characteristic is not surprising, as potential fluctuations at the Al$_2$O$_3$/Ge interface caused from interface defects or charges in the oxide can lead to the formation of isolated potential minima that can be screened when a sufficient density of holes is accumulated. Finer I-V curves, reported in Fig 3b, measured close to threshold confirmed a behavior typical of a quantum dot in the Coulomb Blockade regime. In this case the channel potential is controlled via the top gate: considering that only in the region of the constriction the field lines from the top gate can penetrate under the transistor gate, we conclude that the non linearity is due to the transport through the small constriction rather than to the contacts or the leads.

Tuning the transistor in the quantum dot regime would allow the maximum sensitivity to the neighboring charges. However, as evidenced by both 2-gate scans and by stability diagrams, not reported here, the conduction is obtained through a random distribution of multiple quantum dots: in such condition is was hard to achieve the needed stability of the sensitivity. Instead we worked at larger bias where a smoother and stable I$_d$-V$_g$ characteristic was obtained. The transistor sensitivity reported in figure 4a, defined as the derivative of the S-D current to the V$_b$ bias and measured at a 1 mV source-drain voltage and 20 mV$_{rms}$ modulation of V$_b$, evidences a still non linear, but reproducible, response of the transistor. The average measured sensitivity is

![Image](https://via.placeholder.com/150)

**Fig4:** a) transistor sensitivity to the barrier gate bias (dI$_{sd}$/dV$_b$) as a function of V$_g$. b) transistor sensitivity (dI$_{sd}$/dV$_b$) as a function of V$_p$. The dips marked are evidence of single electrons entering/leaving the dot driven by the modulation of V$_b$. c) 2D scan of the sensitivity vs. V$_p$ and V$_s$. The dotted line is a eye guide representing a slope of 1V/V, corresponding to and equivalent electrostatic coupling of the electrons to V$_p$ and V$_b$ gates.
1.3 \times 10^{10} \text{ A/V with peaks up to } 3 \times 10^9 \text{ A/V. The sensitivity is about one order of magnitude lower compared to what reported for similar Si based devices}^5 \text{ and can be attributed to the lower hole mobility that requires higher charge density in the channel to obtain comparable source-drain resistance.}

When the plunger gate is swept the same oscillations on the sensitivity curves are observed with a longer period as required from the weaker coupling of this gate to the channel. Superposed to these curves are sharp deeps evidenced in Fig. 4b that are signature of single electrons tunneling in and out of the quantum dot, coherently driven from the modulation of \(V_b\). To confirm that the switching events can be attributed to charge in the quantum dot, rather than to defects in other positions of the device, we observe the shift of the peaks as a function of the two quantum dot gates, \(V_s\) and \(V_b\). These data are reported in Fig. 4c where the dotted line represents the slope of 1 V/V. This slope confirms the comparable coupling strength of the charge to the two set of gates, compatible with the position of the charge inside the quantum dot region.

Integrating the dip in the trace in Fig 4b we can extract the change of source-drain current after the addition/subtraction of one electron to the quantum dot that, in the highest sensitivity region, corresponds to a current step of \(1.1 \times 10^{-11} \text{ A}\). This is obtained for a total current \(I_{sd} = 3.5 \times 10^{-9} \text{ A}\) and source-drain bias \(V_{sd} = 1 \text{ mV}\). At 0.37 K the main noise source in these conditions is the shot noise, giving a maximum theoretical speed for the detection of single tunneling events of \(10^5 \text{ Hz}\).

The instabilities measured in the 2D scans evidence the presence of trapped charges in the quantum dot, expected given the nature of the Ge/Al\(_2\)O\(_3\) interface, and limit the ability to consistently control the charge accumulated in the quantum dot in a limited range of \(V_p\) and \(V_b\). Much work has been lately focused on the improvement of the Germanium/dielectric interface, but data on the low temperature mobility of electrons at such interfaces is still lacking. As an alternative approach to the improvement of the device we suggest the use of the SiGe/Ge interface for the confinement of electrons. The possibility to confine electrons in Si\(_x\)Ge\(_{1-x}\)/Ge heterostructures with \(x \approx 0.1\) is limited by the relatively small energy barrier available, just 55 meV. However electrons in Germanium have a fairly large longitudinal transverse effective mass, which is the relevant one for tunneling through this kind of barrier if the heterostructure is grown on (111) substrates, so that a sufficiently long confinement of electrons can be obtained, provided that the transverse electric field is limited. This requirement means that the hetero-interface is adequate for the confinement of the few electrons in the quantum dot but not for the accumulation of the 2DEG of the reservoir or the 2DHG of the electrometer channel.

A schematic cross-section of a possible device using both the Al\(_2\)O\(_3\)/SiGe and the SiGe/Ge interface, realized on a Al\(_2\)O\(_3\)/SiGe/Ge multilayer, is reported in figure 5: the high energy barrier...
at the Al₂O₃/SiGe interface is used to confine the 2DHG, that doesn’t require high interface quality, while the electrons in the quantum dot requiring a smooth and well controlled confinement potential would be at the SiGe/Ge interface. A 2DEG, acting as an electrons reservoir, would be formed at both the Al₂O₃/SiGe and at the SiGe/Ge interface. Electrodes are provided so that the more mobile electrons at the lower interface would have a smaller energy barrier to the quantum dot, so that this layer would be the one actually used for the electron reservoir. The quantum dot potential is set with a metal electrode in contact with the SiGe surface, so that electrons eventually tunneling through the barrier can be collected without

![Diagram](image1)

**Fig 5.** a) Schematic cross-section of a quantum dot device realized on a SiGe-Ge heterostructure with integrated charge sensor. The 2DHG and the electron in the quantum dot lay on two different planes of the device. The Quantum dot electrode is directly in contact with the SiGe surface in order to collect the electrons possibly tunneling through the barrier.
b) Simulation of the device. The color in the Ge and SiGe layers encodes the carrier surface density (positive numbers indicate a hole channel, while negative are referred to electrons) while the iso-curves indicate the conduction band energy, with 10 meV steps. The electron wavefunction is obtained solving the Schrödinger equation in the potential well formed in the quantum dot region.
modifying the potential of the electron trap. In fig 5b we report a simulation of the potential profile. The large transverse mass of electrons in Germanium makes this approach a viable solution. In the design reported the barrier to confine electrons is triangular with an electric field of $2.2 \times 10^6$ V/m. Through a WKB approximation, using an effective barrier height of 50meV, we can estimate an average confinement time larger than one hour, large enough that it won’t be the limit factor on the complexity of the spin manipulation that can be executed in such a device.

**Conclusions**

Concluding, we have shown for the first time the formation of an electron quantum dot in pure Germanium using an Al$_2$O$_3$/Ge MOS structure with an integrated readout channel. We designed a device employing a p-type transistor to detect the electron charge in the quantum dot: this design has allowed overcoming the technological difficulties encountered in the realization of low temperature Germanium n-MOSFETs and added no complexity to the device fabrication. While the low hole mobility of 450 cm$^2$/Vs, caused by the use of the Al$_2$O$_3$/Ge interface, reduced the transistor current and sensitivity, we were able to detect the displacement of single electrons charges driven by the modulation of one of the quantum dot gates. Control of the quantum dot potential with the two sets of gates confirmed that the charge detected was confined in the quantum dot defined by the electrodes. Instability observed in the 2-gates scans suggest that charges are trapped at the Al$_2$O$_3$/Ge interface causing non repeatable modifications of the quantum dot potential during the experiments, limiting the control on the quantum dot charge. The low interface quality can be acceptable for the charge detection transistor, where defects can be screened by a larger carrier density and the penalty on the mobility and sensitivity doesn't hinder the detection of single charges. However the electrons in the quantum dot will require a cleaner interface to allow better control of the quantum dot potential: we suggest the use of a three layer structure consisting of Al$_2$O$_3$/SiGe/Ge. The large barrier at the Al$_2$O$_3$/SiGe interface is used for the accumulation of the charge measurement transistor, while the electrons that are accumulated with a lower surface density are confined at the SiGe/Ge interface. A proper device design can limit the electric field in the SiGe barrier over the quantum dot, ensuring a confinement time much longer than the time required for electron spin manipulations.

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