**Single-Switch High Step-Up Zeta Converter Based on Coat Circuit**

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**ABSTRACT** By the negative influence of parasitic parameters from the components, the voltage step-up capacity of basic dc-dc converters is limited at extremely high duty cycle. Which makes the traditional dc-dc converters are difficult to be applied to renewable energy generation systems such as fuel cell and photovoltaic (PV) systems. In this study, a single-switch high step-up Zeta converter is proposed based on the basic Zeta converter and corresponding coat circuit. By using the coat circuit, the proposed converter not only can achieve higher voltage gain, but also acquire lower voltage stress on the semiconductor devices. Therefore, the devices with lower conduction resistances can be used to improve the efficiency. Furthermore, the coat circuit is composed of passive components, which does not change the continuous output current characteristic of the basic Zeta converter. And the proposed converter has only one active switch, the drive and control circuits are simple. The operation principle and the performance analysis of the proposed Zeta converter are described in detail, and a 300 W closed-loop experimental prototype has been developed for verification.

**INDEX TERMS** Zeta converter, single-switch, high voltage gain, low voltage stress, dc-dc converter.

**I. INTRODUCTION**

With the exacerbation of a series of global problems such as the greenhouse effect and environmental pollution, the grid-connected generation systems of renewable energy such as PV and fuel cell systems have been rapidly developed and deployed [1]–[6]. Thus, the research interests in advanced dc-dc converters to obtain high voltage gain is ever-increasing. The isolated dc-dc converters can easily obtain the capacity of high voltage step-up by changing the turn ratio of transformers [7], [8]. However, the use of transformers would increase the total cost and volume of the converters. And the isolated converters are preferred when electrical isolation is required. The voltage gain of the cascade converters is the product of the gain of each stage structure, and the ability of high voltage step-up can be easily achieved [9]–[11]. But the efficiency of the system would decrease with multi-stage energy transformation, and there are some problems in the stability of the multi-stage structures. The utilization of coupled inductor is another widely used method to obtain high voltage gain in dc-dc converters [12], [13]. However, the leakage inductor would lead to high voltage stress of semiconductor devices. And some appropriate snubber circuits are needed to absorb the voltage spike caused by leakage inductor, which increases the complexity of the system. The high voltage gain converters with switched capacitor structures have some basic disadvantages such as complex driving circuit and many active switches [14]–[16]. In [17]–[19], some high voltage gain converters have been presented based on various voltage multipliers. By using the voltage multipliers, the voltage gain of these converters can be significantly increased and the voltage stress across switching devices would be effectively reduced.

Although each type of aforementioned converters has its advantages, most of them are derived from the conventional boost converter, which makes above converters can only achieve voltage step-up, without the capability of voltage step-down. Therefore, these converters are difficult to be applied in some applications with the requirement of a wide voltage gain for both step-up and step-down [20]–[22].
By introducing the voltage multipliers into the conventional buck-boost converter, the converter presented in [23] can obtain higher voltage gain and has the ability of voltage step-down. And the voltage stress across active switch in this converter can be decreased. Similarly, a single-switch high voltage gain dc-dc Zeta-derived converter has been proposed in [24]. But the voltage gain is limited, which is only twice that of the basic buck-boost converters. In [25], a negative output high step-up buck-boost converter has been proposed. The converter can be derived a wider voltage gain than the classical buck-boost converter. And the control and drive circuits are consistent with the conventional buck-boost converter though the converter has two active switches. Analogously, A single-switch buck-boost converter with high voltage gain has been presented in [26]. In [27], a non-isolated single-switch cascaded converter has been proposed. The converter can obtain a wider output voltage, and its voltage gain is the square of the classical buck-boost converter. However, the voltage stress across semiconductor components of the above three converters is correspondingly higher. Moreover, the aforementioned converters have the common drawback that the circuit structures are not easy to expand, which limits the capability of voltage step-up.

For further improving the voltage gain of classical buck-boost converters, some expandable converters have been proposed in [28]–[30]. Compared to the classical buck-boost converter, the converter presented in [28] can improve the voltage gain with lower voltage stress on the devices by using the scalable voltage multipliers. A family of non-isolated dc-dc converters have been proposed in [29] based on the switched capacitor structures. By using different switched-capacitor structures, the converters can achieve the capability of voltage step-up and step-down with a low duty cycle and have a low energy loss in the magnetic field. However, the efficiency of the converter will decrease, and the volume of the heatsink will increase when using many active switches. A family of coat circuits that are suitable for traditional dc-dc converters is proposed in [30] to improve the voltage gain, where the Cuk converter has been analysed in detail as an example.

In the present investigation, a Zeta converter with coat circuit is proposed and analysed in detail. The operation principle and performance analysis of the presented Zeta converter are described in the sections II and III of this study, respectively. The correctness of the mathematical analysis and the dynamic performance of the system are verified by a 300 W closed-loop experiment prototype in Section IV. And the concluding remarks are proposed in Section V.

II. OPERATION PRINCIPLE OF THE PROPOSED ZETA CONVERTER

The general structure of the proposed Zeta converter, which contains \( n \) basic cells, is shown in Fig. 1(a). According to the actual application requirements, the number of the basic cells of the presented converter can be appropriately adjusted. The topology of the presented Zeta converter with a single basic cell is illustrated Fig. 1(b). And the analysis of the operation principle in this study is adopted the topology shown in Fig. 1(b).

The results can be readily generalized to the configuration with more basic cells. To simplify the analysis process of the proposed converter, some assumptions are considered as follows:

1) The capacitances of all capacitors are supposed assumed to be large enough that the effects of voltage ripple across them are negligible.
2) All devices are assumed to be ideal, i.e. the influence of parasitic parameters is negligible.

The proposed Zeta converter can be operated in the discontinuous conduction mode (DCM) and the continuous conduction mode (CCM) according to different load conditions [31]. When working in CCM, the converter has two switching modes over a single switching period \( T_s \), and the main operating waveforms are plotted in Fig. 2. The specific working modes are as follows:

**Stage 1\([t_0,t_1]\):** The equivalent circuit of stage 1 is presented in Fig. 3(a). In this stage, diodes \( D_1 \) and \( D_{11} \) are turned off, and main switch \( S_1 \) is turned on. The voltage source constitutes three loops, which are: first, the voltage source charges the inductor \( L_1 \) through the main switch \( S_1 \) to form a loop, second, the source charges the inductor \( L_2 \) and capacitor \( C_2 \) to form a loop with the capacitor \( C_1 \), and finally charges the inductor \( L_{11} \) and capacitor \( C_{12} \) through the capacitor \( C_1 \) and capacitor \( C_{11} \) to form a loop and powers the load. In this interval, the inductor currents \( i_{L1}, i_{L2}, \) and \( i_{L11} \) all...
Based on the above analysis of the operation principle, and applying the principle of voltage-second balance of inductors, the voltage equations can be derived by (2).

\[ \begin{align*}
  u_{L1} & = u_{in} \\
  u_{L2} & = u_{in} - u_{C2} + u_{C1} \\
  u_{L11} & = u_{in} - u_{C12} + u_{C1} + u_{C11}
\end{align*} \]  

Equation (4) gives the expression for the output voltage. Therefore, the voltage gain \( M \) can be calculated by:

\[ M = \frac{u_o}{u_{in}} = \frac{2D}{1-D} \]  

where \( m \in [1, n] \).

Equation (7) states that the voltage gain \( M \) of the presented Zeta converter can be adjusted by changing the quantities of \( L_1, L_2, \) and \( L_{11} \), it can be derived from (1) and (2).

\[ \begin{align*}
  u_{in} \cdot D & = u_{C1} \cdot (1-D) \\
  (u_{in} - u_{C2} + u_{C1}) \cdot D & = u_{C11} \cdot (1-D) = u_{C2} \cdot (1-D) \\
  (u_{in} - u_{C12} + u_{C1} + u_{C11}) \cdot D & = \\
  (u_{C12} - u_{C11}) \cdot (1-D) & = (u_{C12} - u_{C2}) \cdot (1-D) 
\end{align*} \]  

Rewriting (3) one obtains:

\[ \begin{align*}
  u_{C1} & = u_{C11} = u_{C2} = \frac{D \cdot u_{in}}{1-D} \\
  u_{o} & = u_{C12} = \frac{2D \cdot u_{in}}{1-D}
\end{align*} \]  

The single-cell proposed Zeta converter can be generalized to contain \( n \) basic cells, i.e.

\[ \begin{align*}
  u_{Cm2} & = \frac{u_{in} \cdot (m+1)D}{1-D} \\
  u_{C1} & = u_{C2} = u_{Cm1} = \frac{u_{in} \cdot D}{1-D} \\
  u_{o} & = u_{Cm2} = \frac{u_{in} \cdot (n+1)D}{1-D}
\end{align*} \]  

III. PERFORMANCE ANALYSIS

A. VOLTAGE GAIN

Based on the above analysis of the operation principle, and applying the principle of voltage-second balance of inductors and capacitors, the voltages across them are slightly increased, and the capacitors \( C_2 \) and \( C_1 \) are charged that the voltages across them are slightly increased. Then the voltage equations of inductors \( L_1, L_2, \) and \( L_{11} \) in this stage can be expressed as:

\[ \begin{align*}
  u_{L1} & = u_{in} \\
  u_{L2} & = u_{in} - u_{C2} + u_{C1} \\
  u_{L11} & = u_{in} - u_{C12} + u_{C1} + u_{C11}
\end{align*} \]  

Equation (7) states that the voltage gain \( M \) of the presented Zeta converter can be adjusted by changing the quantities of
basic cells.

\[ u_0 = \frac{R \cdot (D \cdot u_{in} - (1 - D) \cdot V_D)}{\frac{1}{n+1} \left( R + R_{L1} + \sum_{i=1}^{n} R_{L1} \right) + \frac{(n+1)D^2}{1-D} \cdot R_{L1} + \frac{(n+1)D}{1-D} \cdot R_{on}} \]  

(8)

When considering the voltage drops and the equivalent resistances of the components, the output voltage of the proposed Zeta converter using \( n \) basic cells can be obtained (see (8)).

Where \( V_D \) represents the voltage drop of diodes, \( R_{on} \) is the main switch equivalent resistance, \( R \) is the load resistance, and \( R_{L1}, R_{L2}, R_{L11}, R_{L21}, \ldots, R_{L1n} \) are the equivalent resistances of the corresponding inductors.

**B. STRESS ANALYSIS OF THE COMPONENTS**

As presented in Fig. 2, the voltage stresses across the diodes \( D1, D11 \) and the main switch \( S1 \) are denoted as \( u_{D1}, u_{D11}, \) and \( u_{S1} \), respectively. According to (4), \( u_{D1}, u_{D11}, \) and \( u_{S1} \) are:

\[
\begin{align*}
    u_{D1} &= u_{in} + u_{C1} = \frac{u_0}{2D} \\
    u_{D11} &= u_{in} + u_{C1} + u_{C11} = \frac{u_0}{2D} \\
    u_{S1} &= u_{in} + u_{C1} = \frac{u_0}{2D}
\end{align*}
\]

(9)

According to (6), the voltage stresses across the main switch can be generalized to the case that contains \( n \) basic cells, i.e.

\[
\begin{align*}
    u_{D1} &= u_{Dm1} = \frac{u_0}{(n+1)D}, \quad m \in [1, n] \\
    u_{S1} &= \frac{u_0}{(n+1)D}
\end{align*}
\]

(10)

To simplify the analysis for the current stress, the ripple of the output current \( i_0 \) can also be ignored, and its average value is marked as \( I_o \). The inductors current ripples are ignored, and the currents \( I_{L1}, I_{L2}, \) and \( I_{L11} \) of the inductors \( L1, L2, \) and \( L11 \) are denoted by \( I_l1, I_l2, \) and \( I_{l11}, \) respectively. The average currents \( I_{D1} \) and \( I_{D11} \) of the diodes \( D1, D11 \) are denoted as \( I_{D1} \) and \( I_{D11}, \) respectively. According to the capacitor charge balance of \( C1, C2, C11, \) and \( C12, \) we have:

\[
\begin{align*}
    (I_{L2} + I_{L11}) \cdot D &= I_{l1} \cdot (1 - D) \\
    I_{L2} \cdot D &= I_{D11} - I_{L2} \cdot (1 - D) \\
    I_{L11} \cdot D &= I_{D11} - I_{L11} \cdot (1 - D) \\
    I_{L11} - I_0 &= 0
\end{align*}
\]

(11)

Based on (11), the average current values of the inductors \( L1, L2 \) and \( L11 \), and diodes \( D11, D1 \) is obtained:

\[
\begin{align*}
    I_{L1} &= (I_{L2} + I_{L11}) \cdot \frac{D}{1 - D} = I_0 \cdot \frac{2D}{1 - D} \\
    I_{L2} &= I_{L11} = I_{D1} = I_{D11} = I_0
\end{align*}
\]

(12)

Based on Fig. 3(a), the main switch current stress is written as:

\[
    I_{S1} = D \cdot i_{S1} = D \cdot (I_{L1} + I_{L2} + I_{L11}) = I_0 \cdot \frac{2D}{1 - D}
\]

(13)

When the proposed converter is extended to the configuration with \( n \) basic cells, the average current values of the switches, the inductors, and the diodes can be calculated by (14).

\[
\begin{align*}
    I_{S1} &= \frac{(n+1)D}{1 - D} \cdot I_0 \\
    I_{D1} &= I_{Dm1} = I_0 \\
    I_{L1} &= \frac{(n+1)D}{1 - D} \cdot I_0 \\
    I_{L2} &= I_{Lm1} = I_0 \\
    & \quad m \in [1, n]
\end{align*}
\]

(14)

**C. DCM AND BOUNDARY CONDITION**

As the load power decreases, the average currents of the inductors \( L1, L2, \) and \( L11 \) decrease accordingly. However, the current ripple peak-to-peak values of the inductors do not change according to (1)-(4). Therefore, when the output current drops to a certain value, the analysis of the presented Zeta converter will enter DCM. When working in DCM, the proposed Zeta converter is divided into five stages in a single switching period. The analysis of the stage 2\((t1-t2)\) and stage 3\((t2-t3)\) in DCM is the same as that stage 1 and stage 2 in CCM, respectively. And Fig. 4 and Fig. 5 show the main waveforms and the equivalent circuits in DCM, respectively.

Fig. 5(a) shows the equivalent circuit of stage 1\((t0-t1)\). During this stage, the inductor \( L1 \) starts to be charged and the inductors \( L2 \) and \( L11 \) are discharged in reverse after the main switch \( S1 \) is turned on. This interval in this stage, the capacitors \( C1 \) and \( C11 \) are charged, the capacitors \( C2 \) and \( C12 \) are discharged, and the diodes \( D1 \) and \( D11 \) are turned off. The process would finish when the currents \( I_{l1} \) and \( I_{l11} \) reach zero at the time \( t1 \) which is plotted in Fig. 4. The equivalent circuit of stage 4\((t3-t4)\) is illustrated Fig. 5(b). During this period, the inductors \( L2 \) and \( L11 \) start to be charged in reverse after the currents \( I_{l1} \)
When diodes are working in the on-state, we have:
\[ i_{D1} + i_{D11} = i_{L1} + i_{L2} + i_{L11} \]  
(17)

Based on the capacitor charge balance of capacitors \( C_1, C_{11}, C_2 \) and \( C_{12} \), the average current values of the diodes \( D_1 \) and \( D_{11} \) are calculated by:
\[
I_{D1} = I_{D11} = I_o = \frac{u_0}{R_L} 
\]  
(18)

Next, the total average current \( I_D \) of the diodes \( D_1 \) and \( D_{11} \) are:
\[
I_D = I_{D1} + I_{D11} = 2\frac{u_0}{R_L} 
\]  
(19)

The sum of the peak currents of diodes \( D_1 \) and \( D_{11} \) is marked as \( i_{D-\text{peak}} \). According to Fig. 4, \( I_D \) can be calculated as:
\[
I_D = I_{D1} + I_{D11} = \frac{1}{2} \times D_M \times i_{D-\text{peak}} 
\]  
(20)

The sum of peak currents of inductors \( L_1, L_2 \) and \( L_{11} \) is denoted as \( i_{L-\text{peak}} \). Based on (17), it can be derived that \( i_{D-\text{peak}} \) is equal to \( i_{L-\text{peak}} \), and \( i_{D-\text{peak}} \) can be written as:
\[
i_{D-\text{peak}} = i_{L-\text{peak}} = i_{L1-\text{peak}} + i_{L2-\text{peak}} + i_{L11-\text{peak}} 
\]  
(21)

where
\[
1 = \frac{1}{L}_{\text{eq}} = \frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_{11}} 
\]  
(22)

Based on (20) and (21), \( I_D \) can be derived as:
\[
I_D = \frac{1}{2} \cdot D_M \times i_{D-\text{peak}} = \frac{u_{\text{in}} \cdot D_M \cdot D \cdot T_S}{2L_{\text{eq}}} 
\]  
(23)

By using (16), (19), and (23), \( D_M \) can be eliminated. The voltage gain \( M_{\text{DCM}} \) thus can be derived and written as:
\[
M_{\text{DCM}} = \frac{u_0}{u_{\text{in}}} = D \cdot \sqrt{\frac{R_L \cdot T_S}{2L_{\text{eq}}}} 
\]  
(24)

Here, a dimensionless coefficient \( \tau \) is defined as:
\[
\tau = \frac{R_L \cdot T_S}{2L_{\text{eq}}} 
\]  
(25)

Substitute (25) into (24), equation (24) can be rewritten as:
\[
M_{\text{DCM}} = D \cdot \sqrt{\frac{1}{\tau_n}} 
\]  
(26)

When the proposed Zeta converter is extended to contain \( n \) basic cells, the generalized voltage gain of the presented converter working in DCM can be calculated as:
\[
M_{\text{DCM}} = \frac{u_0}{u_{\text{in}}} = D \cdot \sqrt{\frac{1}{\tau_n}} 
\]  
(27)

where
\[
\tau_n = \frac{R_L \cdot T_S}{2L_{\text{eq}}} 
\]  
(28)
FIGURE 6. Curves of voltage gain versus duty cycle.

FIGURE 7. Curve of boundary coefficient $\tau_B$ versus duty cycle.

Fig. 6 illustrates the curves between voltage gain and duty cycle for the presented Zeta converter with two basic cells. When working in DCM with various $\tau$, the voltage gain $M_{DCM}$ increases as $\tau$ increases.

The voltage gain in CCM is identical with that in DCM, with the proposed Zeta converter operating in the boundary conduction mode. According to (5) and (26), the boundary coefficient $\tau_B$ can be calculated as:

$$\tau_B = \frac{4}{(1 - D)^2}$$  \hspace{1cm} (29)

The curve between boundary coefficient $\tau_B$ and duty cycle of the proposed Zeta converter with one basic cell is illustrated in Fig. 7. When $\tau < \tau_B$, the proposed Zeta converter operates in CCM. On the contrary, the proposed Zeta converter works in DCM if $\tau > \tau_B$.

Similarly, the boundary coefficient $\tau_{Bn}$ of the proposed Zeta converter contains $n$ basic cells is expressed as:

$$\tau_{Bn} = \frac{(1 + n)^2}{(1 - D)^2}$$  \hspace{1cm} (30)

D. COMPARISON

Based on some classical converters such as buck-boost, boost, and Zeta converters, some dc-dc converters with high voltage conversion ration have been proposed in [20]–[30]. The performance comparison between the proposed Zeta converter, some of these converters, and the traditional Zeta converter is presented in Table 1. Fig. 8 illustrates the relationship between voltage gain and duty cycle for the proposed Zeta converter, the converters presented in [24], [27], the Zeta-derived converter proposed in [29], and traditional Zeta converter. Comparing with conventional Zeta converter, the proposed Zeta converter and the others have the advantages of lower voltage stress on the semiconductor devices and higher voltage gain. When the presented Zeta converter contains a single basic cell, the voltage gain is equal to that of the converter proposed in [24]. And the total number of devices used by the proposed converter is the same as that in [24]. Comparing with the proposed Zeta converter with two basic cells, the converter proposed in [27] can obtain a wider range of output voltage. However, in [27], the voltage stress across the devices is even higher. Furthermore, the converters presented in [24], [27] have a common disadvantage that their circuit structures are not expandable, and thus their voltage gains are difficult to be extended. Compared to the converters in [29], the presented Zeta converter can achieve higher voltage gain when using the same number of expandable cells. Moreover, the proposed Zeta converter uses only a single active switch and the voltage stress on devices is lower compared to the converters in [29]. This means the overall loss as well as the volume of the heatsink can be reduced for the presented converter.

E. SYSTEM MODEL AND CONTROL STRATEGY

As presented in Fig. 9, according to the circuit averaging method described in [32], the averaged switching model that
contains two basic cells is derived to obtain the dynamic characteristics of the proposed Zeta converter. The symbol (*) in (31) and (32) represents small perturbation of the parameters in the model. In Fig. 9, \( T_p \) represents the primary winding of the transformer, and \( T_{S1}, T_{S2}, \) and \( T_{S3} \) are the secondary windings of corresponding transformers (the transformer windings represent the dynamic ratio relationship between the active switch and the diodes in this model).

\[
\begin{align*}
\mathbf{i}_1 &= \frac{I_{D1}}{D} \cdot \hat{d}(t) \\
\mathbf{i}_2 &= \frac{I_{D11}}{D} \cdot \hat{d}(t) \\
\mathbf{i}_3 &= \frac{I_{D21}}{D} \cdot \hat{d}(t) \\
\mathbf{u}_1 &= \frac{U_{in}}{D} \cdot \hat{d}(t) \\
\langle \mathbf{i}_j(t) \rangle_{T_S} &= \hat{i}_j(t) + I_j \\
\langle \mathbf{u}_C(t) \rangle_{T_S} &= \hat{u}_C(t) + U_{C_i} \\
\langle \mathbf{u}_n(t) \rangle_{T_S} &= \hat{u}_n(t) + U_{in} \\
\langle \mathbf{u}_o(t) \rangle_{T_S} &= \hat{u}_o(t) + U_o \\
d(t) &= \hat{d}(t) + D
\end{align*}
\]

In equation (33), \( C_i \) is \( C_1, C_2, C_{11}, C_{12} \) or \( C_{21} \), and \( L_j \) is \( L_1, L_2, L_{11} \) or \( L_{21} \).

The block diagram of the double-loop control strategy based on current of inductor \( L_1 \) and output voltage is illustrated in Fig. 10. Compared to the control strategy of single voltage loop, the dual-loop control strategy with the output voltage and the inductor current has the advantages of excellent anti-noise effect, fast response speed and controllable input current, and it has been widely used for dc-dc converters.

IV. EXPERIMENTAL VERIFICATION

A closed-loop experimental prototype of the proposed Zeta converter that contains two basic cells was built to verify the correctness of the above analysis mentioned in the previous sections. Table 2 presents the experimental parameters of the prototype. And the recorded experimental waveforms are illustrated in Figs. 11-15.

### TABLE 1. Comparison of the proposed Zeta converter with other topologies.

| Topology             | Proposed Converter | Converter in [24] | Converter in [27] | Zeta-derived converter in [29] | Traditional Zeta converter |
|----------------------|--------------------|-------------------|-------------------|-------------------------------|-----------------------------|
| Voltage gain         | \( \frac{1}{1-D} \) \(
| Max voltage stress   | \( \frac{u_o}{(n+1)D} \) \(
| Max voltage stress   | \( \frac{u_o}{(n+1)D} \) \( \frac{u_o}{2D} \) \( \frac{u_o}{D^2} \) \( \frac{(n-1)D}{D} \) \( \frac{u_o}{D} \) \)
| Number of diodes     | \( n+1 \) \( 2 \) \( 5 \) \( n \) \( 1 \)
| Number of inductors  | \( 2n+1 \) \( 3 \) \( 3 \) \( 2 \) \( 2 \)
| Number of switches   | \( 1 \) \( 1 \) \( 1 \) \( 2n-1 \) \( 1 \)
| Number of capacitors | \( 2n+2 \) \( 4 \) \( 3 \) \( n+1 \) \( 2 \)
| Total                | \( 4n+6 \) \( 10 \) \( 12 \) \( 4n+2 \) \( 6 \)

### TABLE 2. Parameters of the experimental prototype.

| Parameter          | Values          |
|--------------------|-----------------|
| Switching frequency (\( f_s \)) | 100kHz |
| Diodes (\( D_1, D_{11}, D_{12} \)) | IGBT12S60C |
| Switch (\( S_1 \)) | IRFB4332 |
| Inductors          | \( L_o, L_{11}, \) and \( L_{21} \) |
| Capacitors         | \( C_o, C_{11}, C_{12}, C_{21}, \) and \( C_{22} \) |
| Output power (\( P_o \)) | 300 W |
| Input voltage (\( u_i \)) | 48 V |
| Output voltage (\( u_o \)) | 400 V |

### FIGURE 10. Double-loop control strategy diagram for the proposed Zeta converter.

The \( u_{gs}, u_{in}, u_{i1} \) and \( u_o \) shown in Fig. 11 represent the waveforms of the driving voltage, the input voltage, the voltage stress across active switch, and the output voltage, respectively. When the duty cycle is about 74%, the output voltage is approximately 400 V, which is consistent with the analysis of (7).

The current waveforms for inductors \( L_1, L_{11}, L_2, \) and \( L_{21} \) are illustrated in Fig. 12, where the average current of inductor \( L_1 \) is near 6.25 A, while the average currents of inductors \( L_{11}, L_2 \) and \( L_{21} \) are all approximately 0.75 A, which complies with the theoretical calculation.
B. Zhu et al.: Single-Switch High Step-Up Zeta Converter Based on Coat Circuit

FIGURE 11. Waveforms of the driving voltage, input voltage, voltage across the active switch $S_1$ and output voltage.

FIGURE 12. Waveforms of the inductor currents.

FIGURE 13. Waveforms of the voltage across the diodes.

Fig. 13 illustrates the voltage waveforms across diodes $D_1$, $D_{11}$, and $D_{21}$, while the voltages $u_{D_1}$, $u_{D_{11}}$, and $u_{D_{21}}$ are all around 181 V that represent the voltage stress across diodes $D_1$, $D_{11}$, and $D_{21}$ respectively. The voltage stress $u_{S_1}$ across active switch is also about 181 V. The above results of voltage stresses are the same as that obtained from (10).

The waveforms of voltages across the capacitors $C_{1}$, $C_{11}$, $C_{21}$, $C_{2}$, $C_{12}$, and $C_{22}$ are shown in Fig. 14. As shown in Fig. 14(a), $u_{C_1}$, $u_{C_{11}}$, and $u_{C_{12}}$ are all approximately 133 V. In the Fig. 14(b), $u_{C_{21}}$ is about 133 V, $u_{C_{12}}$ is about 266 V, and $u_{C_{22}}$ is about 400 V. The above results of voltages across capacitors are also consistent with that obtained from (6).

Furthermore, Fig. 15 shows the waveforms of the dynamic performance testing of the prototype. Fig. 15(a) and Fig. 15(b) illustrate the experimental waveforms of the input voltage, output voltage and AC value of output voltage with the input voltage jumping from 48 V to 58 V and jumping from 58 V to 48 V, respectively. The results show that the change in power supply has a response process of approximately 9ms and the output voltage hardly changes with input voltage jumping. The experimental waveforms of the output voltage, output current, input voltage, and AC value of output voltage when the load resistor changes from 533 Ω to 400 Ω and changes from 400 Ω to 533 Ω are illustrated in Fig. 15(c) and Fig. 15(d), respectively. As presented in Fig. 15(c), the output voltage drops slightly with the increase of output power and the amplitude of the fluctuation is about 10 V. In about 4ms, it reaches the rated value. Fig. 15(d) shows that the output voltage rises slightly with the decrease of output power and the fluctuation amplitude is about 10 V. In about 4ms, it also can reach the steady state. The waveforms of dynamic testing show that the dynamic response is fast and the voltage overshoot is small based on the designed closed-loop control scheme.

The efficiency the proposed Zeta converter prototype is plotted in Fig. 16 as functions of the output voltage and the output power. Fig. 16(a) illustrates the efficiency of the prototype under different output voltage conditions with 48 V input voltage. The converter can obtain the maximum efficiency 94.3% when the output voltage is 240 V. As presented in Fig. 16(b), the efficiency curve under different output powers is obtained when the load resistor is changed. The maximum
efficiency 94.2% of the converter can be reached when the output power is 240 W.

Fig. 17 shows the calculated loss at rated power of the experimental prototype. The overall loss of the prototype mainly consists of the loss of inductors, active switch and diodes, in which the loss of inductors is calculated about 7.13 W, the loss of active switch is calculated to be around 6.92 W and the loss of diodes is calculated approximately 3.38 W.
The relationship between the duty cycle \( (D) \) and the voltage gain \( (M) \) is illustrated in Fig. 18, where the blue curve is the theoretical voltage gain and the red curve shows the measured voltage gain of the experimental prototype. Obviously, the actual voltage gain from the experiment is close to the theoretical voltage gain when \( D \) is less than 0.8. On the contrary, when \( D \) is greater than 0.8, the results from the prototype are greatly affected by parasitic parameters, and the actual voltage gain of the proposed Zeta converter deviates largely from the theoretical values.

V. CONCLUSION

In this study, a single-switch high step-up Zeta converter is proposed by incorporating the “coat circuit” into the basic Zeta converter. The experimental results for a 300 W prototype show that the maximum efficiency is about 94.2\% with different load resistors. And the closed-loop system has been established to test the dynamic performance of the prototype. With the analysis and verification of the above sections, the proposed Zeta converter includes the following advantages:

1) Since the presented Zeta converter has only a single active switch, the driver and control circuit are uncomplicated to design and cost-effective to implement; 2) the number of basic cells can be adjusted based on the different applications; 3) the voltage gain of the proposed converter can be significantly improved compared to the traditional Zeta converter, which can avoid the extreme duty cycle. The characteristics thus show the proposed Zeta converter is suitable for the applications where a wide voltage conversion ratio is required.

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