Electrostatic Engineering Using Extreme Permittivity Materials for Ultra-Wide Bandgap Semiconductor Transistors

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Abstract—The performance of ultra-wide bandgap semiconductors like $\beta$-Ga$_2$O$_3$ is critically dependent on achieving high average electric fields within the active region of the device. In this article, we show that dielectrics like BaTiO$_3$ with extremely high dielectric constant can provide an efficient field management strategy by improving the uniformity of electric field profile within the gate–drain region of lateral field-effect transistors. Using this strategy, we achieved high average breakdown field of 1.5 and 4 MV/cm at gate–drain spacing ($L_{gd}$) of 6 and 0.5 $\mu$m, respectively in $\beta$-Ga$_2$O$_3$, at a high channel sheet charge density of $1.6 \times 10^{14}$ cm$^{-2}$. The high channel charge density along with the high breakdown field enabled a record power figure of merit ($V^2_{br}/R_{ON}$) of 376 MW/cm$^2$ at a gate–drain spacing of 3 $\mu$m.

Index Terms—Barium titanate, breakdown, gallium oxide, high-$k$, power figure of merit.

I. INTRODUCTION

LOW loss power switching devices were mostly based on Si until the introduction of wide bandgap semiconductors like SiC (3.2 eV and $F_{br} = 2.5$ MV/cm) and GaN (3.4 eV and $F_{br} = 3$ MV/cm). The larger breakdown field in these semiconductors offered the possibility of shrinking the drift region thickness for the same breakdown voltage resulting in lower on resistance ($R_{ON}$). This improvement in performance is well described by the power figure of merit [1] ($PFOM = \epsilon \mu F^2_{br}$), where $\epsilon$, $\mu$, and $F_{br}$ represent dielectric permittivity, carrier mobility, and breakdown field strength, respectively.

With a theoretical breakdown field strength (8 MV/cm) [2] much higher than GaN and SiC, $\beta$-Ga$_2$O$_3$ offers a new material platform for improving the performance metrics of high voltage devices. In addition to the large breakdown field strength, the availability of bulk substrates grown from melt [3] makes $\beta$-Ga$_2$O$_3$ highly attractive. High-quality epilayers have already been demonstrated using a variety of growth techniques like molecular beam epitaxy (MBE) [4], metal organic chemical vapor deposition (MOCVD) [5], halide vapor phase epitaxy (HVPE) [6], and low pressure chemical vapor deposition (LPCVD) [7]. Background acceptor impurity concentration as low as $9.4 \times 10^{14}$ cm$^{-3}$ has been reported using MOCVD showing the quality of $\beta$-Ga$_2$O$_3$ epilayers that can be achieved [8].

High voltage $\beta$-Ga$_2$O$_3$ devices with excellent performance have already been demonstrated both in vertical and lateral geometry [9]–[11] but for these devices to compete with the current state of the art, it is essential to achieve the full breakdown field strength of $\beta$-Ga$_2$O$_3$ (8 MV/cm). However, this is challenging due to the lack of a suitable dielectric that can sustain electric fields significantly higher than 8 MV/cm. This leads to catastrophic failure of devices at much lower voltages due to dielectric breakdown. In addition, many of the traditional field termination structures which are used in Si and wide bandgap semiconductors such as guard rings [12] and junction termination extensions [13] cannot be utilized in $\beta$-Ga$_2$O$_3$ because of the absence of p-type doping.

The low room temperature mobility is another significant issue hampering the performance of $\beta$-Ga$_2$O$_3$-based devices [14]. The low mobility leads to high channel resistance which in turn affects $R_{ON}$. Improving the channel mobility is one approach to solving this problem, but since the intrinsic mobility in $\beta$-Ga$_2$O$_3$ is limited by polar optical phonon scattering [15], increasing the mobility beyond the theoretical limit may be difficult. An easier approach is to increase the charge density in the channel, especially in lateral field-effect transistors. Most of the high voltage lateral field effect transistors reported in $\beta$-Ga$_2$O$_3$ [9, p. 85], [16], [17] use low channel charge density ($<10^{13}$ cm$^{-2}$) leading to high $R_{ON}$ and low power figure of merit. Increasing the charge density is challenging since modulating higher channel charge density
between the gate and drain leads to larger peak electric fields, decreasing the breakdown voltage. Therefore, new field management strategies may be necessary to simultaneously achieve high breakdown voltage and high channel charge density.

In this article, the use of extreme-\(k\) gate dielectrics is shown to simultaneously achieve high sheet charge density in the channel and improve the average breakdown field, resulting in the improved power figure of merit. First, a detailed analysis is done on the electrostatics of an extreme-\(k\) dielectric/semiconductor heterojunction transistor using two-dimensional device simulation as well as analytical modeling. This is followed up with an experimental demonstration of the said electric field management in BaTiO\(_3/\beta\)-Ga\(_2\)O\(_3\) lateral field effect transistor.

II. 2-D DEVICE SIMULATION AND MODELING

We first define an extreme-\(k\) dielectric as an insulator with a dielectric constant above 100 (\(\varepsilon_b > 100\)). This definition is made to distinguish between extreme-\(k\) dielectrics and traditional high-\(k\) gate dielectrics like HfO\(_2\), whose dielectric constant is electrostatically insufficient in providing the electric field management discussed in this article. Extreme-\(k\) dielectrics include materials like BaTiO\(_3\), SrTiO\(_3\), and Ba(Zn\(_{0.33}\)Nb\(_{0.67}\))O\(_3\) which show extremely large dielectric constants. The effect of using an extreme-\(k\) gate dielectric in a lateral transistor has previously been studied using 2-D device simulations by Xia et al. [18]. Though the simulation was done for the specific case of BaTiO\(_3\) on BaSnO\(_3\), the electrostatics remains the same and therefore the simulations are valid in general. In the work, it was found that the slope of the electric field in the lateral \(x\)-direction [see Fig. 1(a)] reduces when the extreme-\(k\) gate dielectric is introduced improving the average electric field. The effects of additional device parameters, specifically the thickness of the extreme-\(k\) gate dielectric (\(t_b\)) and the channel sheet charge density (\(n_s\)) are discussed in this study.

Consider the lateral transistor structure shown in Fig. 1(a) consisting of a low-\(k\) semiconductor (\(\varepsilon_{ch}\)) with a channel sheet charge density of \(n_s\) (assumed to be a 2-D electron gas) and an extreme-\(k\) gate dielectric (\(\varepsilon_b\)) of thickness \(t_b\) on top. The extreme-\(k\) gate dielectric is assumed to be linear, meaning that the dielectric constant (\(\varepsilon_b\)) is independent of electric field. The 2-D device simulation in Silvaco Atlas software was used to extract both the \(x\)- and \(y\)-components of electric field along a lateral (\(x\)-direction) cutline in the low-\(k\) semiconductor, as shown in Fig. 1(a). Gate length (\(L_g\)) of 1 \(\mu\)m, gate–drain spacing (\(L_{gd}\)) of 3 \(\mu\)m, \(\varepsilon_{ch}\) of 10, and \(\varepsilon_b\) of 300 is assumed for the device. Fig. 1(c) shows the variation in the field profile (\(E_x, E_y\)) as a function of \(t_b\) at a reverse bias of 250 V. As \(t_b\) is increased from 20 to 140 nm, the slope in the \(x\) electric field decreases. This decrease in slope of \(E_x\) is accompanied by a decrease in the peak value of \(y\) electric field at the drain.
side edge of the gate. Fig. 1(d) also shows the effect of \( n_s \) on the electric field profile \( (E_x, E_y) \) showing the reverse trend. As \( n_s \) is increased in the channel, the slope in the \( x \) electric field increases, increasing the peak electric field. In addition, the peak value of \( y \) electric field also increases with increasing \( n_s \). Therefore, in addition to the dielectric constant of the extreme-\( k \) dielectric, its thickness and the channel sheet charge density also determine the electric field profile.

While simulations provide an accurate picture of the impact of parameters like dielectric thickness, \( t_b \), and sheet charge, \( n_s \), it is desirable to have a theoretical model to develop an intuitive understanding of the effects. To fully analyze an interface with dielectric discontinuity it is essential to estimate the polarization charges formed at the dielectric interfaces. Considering the same transistor design shown in Fig. 1(a) and assuming that the gate–drain depletion region \( (L_{\text{dep}}) \) supports a reverse bias \( V_{\text{bi}} \), the distribution of charges is as shown in Fig. 1(b), consisting of positive sheet charge of \( n_s \) in the channel and negative charge on the drain side edge of the gate. The depletion region is assumed to be a positive sheet of charge with density \( n_s \) that abruptly ends at \( x = L_{\text{dep}} \). The gate charge is approximated as a line of negative charge with charge density \( \lambda \) located at the corner of the gate as shown in Fig. 1(b). Since the total charge is conserved, we can write

\[
\lambda = qn_s L_{\text{dep}}.
\]

The presence of these charges leads to the formation of polarization charges on both interfaces of the extreme-\( k \) dielectric. The negative line of charge induces a positive sheet of polarization charge \( [\sigma_1(x)] \) at the \( A'-B' \) interface [Fig. 1(b)] and the positive sheet charge in the channel will induce a negative sheet charge \( [\sigma_2(x)] \) at the \( A-B \) interface as shown in Fig. 1(b). In this simple model we are neglecting the contribution to the \( y \) field along the \( A-B \) interface due to the negative line charge on the gate. This is a reasonable assumption to make especially far away from the gate (\( x \gg t_b \)). The polarization charge density \( \sigma \) in general at a dielectric interface can be estimated by using the following relation:

\[
\sigma = \varepsilon_o \chi E_y
\]

where \( \chi \) is the dielectric susceptibility \((\varepsilon - 1)\), and \( E_y \) is the net electric field in the \( y \)-direction at the interface. Therefore, the negative polarization charge density along \( A-B \) interface

\[
\sigma_2(x) = \varepsilon_o (\varepsilon_b - 1) \left( \frac{q n_s}{2 \varepsilon_o} - \frac{\sigma_2}{2 \varepsilon_o} + \frac{\sigma'}{2 \varepsilon_o} - \frac{\sigma'}{2 \varepsilon_o} \right).
\]

Giving

\[
\sigma_2 = \frac{(\varepsilon_b - 1)}{\varepsilon_b + 1} q n_s.
\]

In (3), \( \sigma' \) corresponds to the dielectric polarization charge within the low-\( k \) semiconductor as shown in Fig. 1(e). For extreme-\( k \) dielectrics \((\varepsilon_b > 100)\), the donor sheet of charge gets completely screened by \( \sigma_2 \) \((\sigma_2 \sim q n_s)\) as shown in (4). Therefore, along the top interface \( A'-B' \) we only need to consider the effect of the negative line of charge at the gate corner. For this, consider the example of a line of charge \( \lambda \) placed at a distance \( d \) away from an air dielectric interface as shown in Fig. 1(f). The special case of \( d = 0 \) ([19]) gives the solution to the required polarization charge density \( \sigma_1(x) \) along \( A'-B' \) giving

\[
\sigma_1(x) = qn_s L_{\text{dep}} \left( \frac{\varepsilon_b - 1}{\varepsilon_b + 1} \right) \delta(x)
\]

where \( \delta(x) \) is the Dirac delta function with peak at \( x = 0 \). Therefore, the polarization charge density along the \( A'-B' \) interface is 0 except at the gate corner. Now, consider a vertical line \( C-D \) at any position \( x \) through the extreme-\( k \) dielectric as shown in Fig. 1(b). Since there is an absence of free charge density within the dielectric, the electric field at any point along \( C-D \) obeys the Laplace equation

\[
\left( \frac{\partial E_y}{\partial y} \right)_{C-D} + \left( \frac{\partial E_x}{\partial x} \right)_{C-D} = 0.
\]

Due to the large dielectric constant of the extreme-\( k \) dielectric, \( E_y \) is much smaller in comparison to \( E_x \). Therefore, the voltage drop along any vertical line within the extreme-\( k \) dielectric may be neglected. The potential distribution and \( E_x \) within the dielectric can therefore be considered as only functions of \( x \) and independent of \( y \). Then along any vertical line \( C-D \) \([x = x_o = \text{constant}, \text{see Fig. 1(b)}] \)

\[
\left( \frac{\partial E_x}{\partial x} \right)_{C-D} = -\left( \frac{\partial E_y}{\partial x} \right)_{C-D} = \text{constant}.
\]

Therefore, the slope of the \( y \) electric field is a constant and can most generally be written as

\[
\left( \frac{\partial E_y}{\partial y} \right)_{C} = \frac{E_x(C) - E_x(D)}{t_b}
\]

Since the extreme-\( k \) dielectric contains zero free charge, we can again apply Laplace equation

\[
E_x(C) = \frac{\sigma_2(C)}{\varepsilon_o (\varepsilon_b - 1)} = \frac{q n_s}{\varepsilon_o (\varepsilon_b + 1)}
\]

and

\[
E_x(D) = \frac{\sigma_1(D)}{\varepsilon_o (\varepsilon_b - 1)} = \frac{q n_s L_{\text{dep}}}{\varepsilon_o (\varepsilon_b + 1)} \delta(x_o).
\]

Therefore, the slope of \( y \) electric field in the extreme-\( k \) dielectric at any position \( x \) along the \( A-B \) interface is given by

\[
\left( \frac{\partial E_y}{\partial y} \right)^{A-B} (x) = \frac{q n_s}{t_b \varepsilon_o (\varepsilon_b + 1)} (1 - L_{\text{dep}} \delta(x))
\]

Since the extreme-\( k \) dielectric contains zero free charge, we can apply Laplace equation

\[
\left( \frac{\partial E_x}{\partial x} \right)^{A-B} = 0
\]

giving

\[
\left( \frac{\partial E_x}{\partial x} \right)^{A-B} = -\frac{q n_s}{t_b \varepsilon_o (\varepsilon_b + 1)} (1 - L_{\text{dep}} \delta(x))
\]

Since the tangential component of electric field stays the same across the dielectric interface

\[
\left( \frac{\partial E_x}{\partial x} \right)^{A-B} = \left( \frac{\partial E_x}{\partial x} \right) = -\frac{q n_s}{t_b \varepsilon_o (\varepsilon_b + 1)} (1 - L_{\text{dep}} \delta(x))
\]
where \((\partial E_x)/(\partial x)\) represents the slope of the \(x\) electric field in the low-\(k\) semiconductor below the \(A-B\) interface. \(E_x\) can now be solved as

\[
E_x(x) = \frac{\int_{x}^{L_{dep}} \frac{q_n}{t_0 \epsilon_o(\epsilon_b + 1)} (1 - L_{dep}) d\delta(u)}{t_0 \epsilon_o(\epsilon_b + 1)}
\]

\[
= \frac{q_n}{t_0 \epsilon_o(\epsilon_b + 1)} (L_{dep} - x) - \frac{q_n L_{dep}}{t_0 \epsilon_o(\epsilon_b + 1)} \delta_{x=0}
\]

(15)

where \(\delta_{x=0}\) is the Kronecker delta function given by

\[
\delta_{x=0} = \begin{cases} 
1, & x = 0 \\
0, & x \neq 0.
\end{cases}
\]

The depletion length at any given reverse bias \(V_{dg}\) can be calculated by satisfying

\[
V_{dg} = \int_{0}^{L_{dep}} E_x(x, L_{dep}) dx.
\]

(16)

Fig. 1(g) and (h) shows the comparison of (15) and (16) with the corresponding values obtained from 2-D device simulations showing reasonable agreement. This simple model is thus able to predict the electric field profile in a lateral field effect transistor with an extreme dielectric interface. As is clear from (15), the dielectric constant, its thickness, and the sheet charge density determine the electric field profile within the gate–drain depletion region of the transistor. Therefore, using a thick extreme-\(k\) dielectric theoretically provides an alternate field management strategy by maintaining a smooth electric field profile between the gate and drain.

### III. Epitaxial Growth and Device Fabrication

To demonstrate the field management strategy using extreme-\(k\) dielectrics, we fabricated lateral metal–insulator–semiconductor field-effect transistors (MISFETs) on \(\beta\)-Ga\(_2\)O\(_3\) with BaTiO\(_3\) as the extreme-\(k\) gate dielectric. BaTiO\(_3\) was chosen due to the high dielectric constant and high breakdown field strength (>8 MV/cm) [20], [21]. MOCVD growth carried out in an Agnitron Agilis Research and Development Oxide Growth System was used to grow the \(\beta-(\text{Al}, \text{Ga}_{1-x})_2\text{O}_3/\text{Ga}_2\text{O}_3\) epilayer as shown in Fig. 2(a). Prior to the growth, the Fe-doped semi-insulating \(\beta\)-Ga\(_2\)O\(_3\)(010) substrates procured from Novel crystal technologies were rinsed using acetic acid, IPA, and DI water followed by 5-min dip in 10% HF. The epitaxial growth using MOCVD was performed at a substrate temperature of 880 °C using the precursors, trimethyl gallium (TEGa), trimethyl aluminum (TMAI), and oxygen for supplying Ga, Al, and O adatoms respectively. Ar was used as the carrier gas for supplying the precursors into the growth chamber. Si doping was carried out using silane (SiH\(_4\)) as the gas source balanced with Ar to achieve the required doping level. Further information on MOCVD growth of \(\beta\)-Ga\(_2\)O\(_3\) and \(\beta-(\text{Al}, \text{Ga}_{1-x})_2\text{O}_3\) can be found in [8] and [22]. The epitaxial structure as shown in Fig. 2(a) consists of a 500-nm unintentionally doped (UID) \(\beta\)-Ga\(_2\)O\(_3\) buffer layer which facilitates the spatial separation of the channel from the Fe (deep acceptor) doped substrate, reducing buffer related trapping issues [23]. The active part of the device consists of 30-nm Si-doped (5 × 10\(^{18}\) cm\(^{-3}\)—n-type) \(\beta\)-Ga\(_2\)O\(_3\) channel layer, a 5-nm Si-doped (5 × 10\(^{18}\) cm\(^{-3}\)) \(\beta-(\text{Al}, \text{Ga}_{0.73})_2\text{O}_3\) layer, and a 15-nm cap layer of UID \(\beta-(\text{Al}_{0.27}\text{Ga}_{0.73})_2\text{O}_3\) epitaxially grown on top of the buffer layer as shown in Fig. 2(a). Fig. 2(b) shows the expected band diagram of the device along a vertical cutline under the gate electrode using the band line up between BaTiO\(_3\) and \(\beta\)-Ga\(_2\)O\(_3\) reported in [24].

Source and drain regions were defined using optical lithography followed by Si ion implantation using ion energies ranging from 10 to 115 keV, to obtain a 100-nm box profile with concentration of 5 × 10\(^{19}\) cm\(^{-3}\) as shown in Fig. 2(c). Implant activation was carried out in a tube furnace in N\(_2\) ambient at a temperature of 900 °C for 30 min, similar to what has been reported previously [25]. Following the activation anneal, the \(\beta-(\text{Al}_{0.27}\text{Ga}_{0.73})_2\text{O}_3\) cap layer was etched away from the source and drain regions using BCl\(_3\)/-Ar-based dry etching. The dry etching step was followed by ohmic contact metallization using Ti/Au/Ni (40/50/50 nm) metal stack annealed at 470 °C in N\(_2\) ambient. The BaTiO\(_3\) gate dielectric was deposited postmetallization of ohmic contacts, using radio frequency (RF) sputtering. Sintered BaTiO\(_3\) (99.9% purity) procured from Kurt J. Lesker was used as a target for the deposition process with an applied RF power of 140 W. Ar and O\(_2\) were used to form the sputtering plasma with corresponding flow rates set to 20 and 2 sccm, respectively, and the chamber pressure maintained at 10 mtorr resulting in a deposition rate of 0.5 nm/min. A substrate temperature of 670 °C gave the best results in terms of the dielectric constant and was therefore used for the deposition.
thickness of the BaTiO₃ dielectric layer was measured using ellipsometry (woolam alpha-SE spectroscopic ellipsometer) giving a thickness of 73 nm (75 nm intended) and a high-frequency refractive index of 2.25. The deposition of the BaTiO₃ gate dielectric was followed by mesa isolation after which the gate metal stack (Ni/Au/Nil – 40/50/50 nm) was deposited to form the Schottky junction.

IV. DEVICE CHARACTERISTICS

Capacitance–voltage (C–V) and transfer length measurements (TLMs) were performed to estimate the effect of sputtering BaTiO₃ at high temperature (670 °C) on the channel charge density, mobility, and contact resistance by comparing these measurements predeposition and postdeposition of BaTiO₃. Sputtering involves deposition using high energy atomic species and can cause significant damage to the semiconductor surface [26]. C–V measurements (1 MHz) performed predielectric deposition show a total charge density of 1.8 × 10⁻¹³ cm⁻² in the channel as shown in Fig. 2(d). The C–V and the charge profile characteristics [inset, Fig. 2(d)] show the presence of additional charge in the buffer layer that remains undepleted even at a reverse bias of −20 V. The MOCVD grown buffer layer is expected to have an uninfluenced. The deposition of BaTiO₃ gate dielectric increases the sheet resistance of extreme-k gate dielectric. The measured devices span a gate–drain spacing from 0.5 to 6 μm. Fig. 3(a) and (b) shows the output characteristics of the fabricated BaTiO₃/β-Ga₂O₃ transistor with source–drain spacing (L₉d) of 1.5 and 7.2 μm, respectively. RₒN of 13.6 Ω · mm and max drain current (I₉d,max) of 359 mA/mm is obtained at L₉d = 1.5 μm. The low ON-resistance and high current density are attributed to the high channel charge density. I₉d,max of 359 mA/mm is also the highest reported in any epitaxially grown β-Ga₂O₃ lateral transistor device under dc conditions, and higher currents have only been obtained in β-Ga₂O₃ nanomembrane transistors transferred onto high thermal conductivity substrates like diamond and Si [30]–[32]. Fig. 3(c) and (d) shows the corresponding transfer characteristics for the same devices showing an on/off ratio of 10⁴−10⁵, which is reasonable considering the high charge density in the channel. Transistors which were fabricated by directly depositing the gate metal on the β-(Al₀.₂⁷Ga₀.₇₃)₂O₃ cap layer without BaTiO₃ gate dielectric could not be pinched off due to severe gate leakage. Hysteresis in the forward and backward sweep of the transfer curves is also observed suggesting the presence of interface states at the BaTiO₃/β-(Al₀.₂⁷Ga₀.₇₃)₂O₃ interface. This may be reduced in future devices by depositing a low-k dielectric like Al₂O₃ on the epilayer before the deposition of BaTiO₃. Fig. 3(e) shows the variation in measured on-resistance for devices with gate length (L₉g) of 0.7 μm. A sheet resistance of 5.5 kΩ/sq is also estimated from the slope of Fig. 3(e), which matches well with the TLM measurements performed postdeposition of BaTiO₃ [Fig. 2(e)].

Fig. 3(f) shows the variation in measured breakdown voltage (V₉bd) and the average breakdown field (F₉av) as a function of gate to drain spacing (L₉g). The three terminal breakdown voltage increases from 201 to 918 V as L₉g is increased from 0.5 to 6 μm, representing a change in F₉av [(V₉bd − V₉g)/L₉g] from 4 to 1.5 MV/cm. The average fields obtained in this work are comparable to those obtained in β-Ga₂O₃ field plated lateral devices with much lower channel sheet charge density [9], [16], [17], [29], [33] and therefore shows the effectiveness of extreme-k gate dielectric-based field management. F₉av versus L₉g plot [Fig. 3(f)] shows two distinct regions. For L₉g between 2 and 6 μm, there is a gradual increase in F₉av from 1.5 to 2.3 MV/cm. As shown in (13), the extreme-k dielectric only reduces the slope of electric field profile and does not make it flat. This results in smaller F₉av at larger L₉g. For L₉g between 1.5 and 0.5 μm, there is a much steeper increase in F₉av from 2.4 to 4 MV/cm. This is likely due to change from nonpunchthrough (L₉dep < L₉gd) to punchthrough breakdown (L₉dep = L₉gd), which provides much larger F₉av. Fig. 3(g) shows the reverse leakage current as a function of drain bias for the devices with L₉g = 3 and 6 μm, indicating that the gate leakage limits the breakdown performance. Simulated electric field profiles for the device with L₉g = 6 μm is shown in Fig. 3(h) along cut lines drawn under the gate [A–A’ in Fig. 2(a)] and through the β-(Al₀.₂⁷Ga₀.₇₃)₂O₃ cap layer [B–B’ in Fig. 2(a)]. Even though the BaTiO₃ extreme-k gate dielectric maintains a uniform electric field profile within the epilayer (peak value < 8 MV/cm), the peak electric field at the gate corner (within BaTiO₃) reaches a much larger value.
(9.5 MV/cm) resulting in increased gate leakage and eventual dielectric breakdown.

Fig. 3(i) shows the comparison of the performance of BaTiO3/β-Ga2O3 transistors with previous reported values in β-Ga2O3 lateral transistors in terms of the power figure of merit ($V_{br}^2/R_{ON}$) where $R_{ON}$ is the ON resistance normalized to the active area of the device ($L_{sd} \times W$). As shown, there is a small variation in the figure-of-merit performance of the measured devices but all of them lie above 147 MW/cm$^2$, with the best performing device, $L_{sd} = 4.2 \mu m$, $L_g = 0.7 \mu m$, and $L_{gd} = 3 \mu m$, showing a power figure of merit of 376 MW/cm$^2$ which is the highest reported value for any β-Ga2O3 transistor to the best of our knowledge. The extreme-k field management strategy using BaTiO3 as the gate dielectric has thus resulted in superior performance even in the absence of additional field termination structures like field plates.

V. CONCLUSION

We have shown that extreme-k insulators like BaTiO3 can provide efficient field management in lateral field effect transistors when used as gate dielectrics. The 2-D device simulations and analytical modeling considering polarization charges formed at the dielectric interfaces were done to theoretically understand the effect of introducing the extreme-k gate dielectric. The field management strategy was further experimentally investigated by fabricating BaTiO3/β-Ga2O3 MISFETs with high channel charge density of $1.6 \times 10^{13} \text{cm}^{-2}$. The fabricated devices showed excellent breakdown performance without any additional field termination structures like field plates, giving an average breakdown field of 1.5 MV/cm at $L_{gd} = 6 \mu m$ and 4 MV/cm at $L_{gd} = 0.5 \mu m$. The high average breakdown fields coupled with the high channel charge density enabled a record power figure of merit of 376 MW/cm$^2$ at a gate–drain spacing of 3 μm. The performance of these transistors in the future may be further improved by integrating additional field termination structures like field plates along with extreme-k gate dielectrics. The ideas developed here are relevant not just for β-Ga2O3, but also provide a framework for designing the next generation of semiconductor devices in RF and power electronics where higher average electric fields enable better efficiency, power density, and faster speed. The integration of extreme permittivity dielectrics based on perovskite oxides into conventional and wide bandgap semiconductors such as Si, GaAs, GaN, and SiC could enable unprecedented performance improvements in RF and power electronics devices.

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