SparkXD: A Framework for Resilient and Energy-Efficient Spiking Neural Network Inference using Approximate DRAM

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Abstract—Spiking Neural Networks (SNNs) have the potential for achieving low energy consumption due to their biologically sparse computation. Several studies have shown that the off-chip memory (DRAM) accesses are the most energy-consuming operations in SNN processing. However, state-of-the-art in SNN systems do not optimize the DRAM energy-per-access, thereby hindering achieving high energy-efficiency. To substantially minimize the DRAM energy-per-access, a key knob to reduce the DRAM supply voltage but this may lead to DRAM errors (i.e., the so-called approximate DRAM). Towards this, we propose SparkXD, a novel framework that provides a comprehensive conjoint solution for resilient and energy-efficient SNN inference using low-power DRAMs subjected to voltage-induced errors. The key mechanisms of SparkXD are: (1) improving the SNN error tolerance through fault-aware training that considers bit errors from approximate DRAM, (2) analyzing the error tolerance of the improved SNN model to find the maximum tolerable bit error rate (BER) that meets the targeted accuracy constraint, and (3) energy-efficient DRAM data mapping for the resilient SNN model that maps the weights in the appropriate DRAM location to minimize the DRAM access energy. Through these mechanisms, SparkXD mitigates the negative impact of DRAM (approximation) errors, and provides the required accuracy. The experimental results show that, for a target accuracy within 1% of the baseline design (i.e., SNN without DRAM errors), SparkXD reduces the DRAM energy by ca. 40% on average across different network sizes.

Index Terms—Spiking neural networks, SNNs, inference, resilience, energy, efficiency, approximate computing, DRAM, DRAM errors, error-tolerance.

I. INTRODUCTION

Spiking neural networks (SNNs) bear the potential of achieving low energy processing and high algorithmic performance because of their biological plausibility [1]. A large-sized SNN model is more desirable as it can achieve higher accuracy than the smaller ones. For instance, Fig. 1(a) shows that the 200MB-sized SNN model achieves 92% accuracy for MNIST, while the 1MB-sized SNN achieves only 75%. On the other hand, most of the SNN hardwares employ an on-chip memory of limited size, e.g., less than 100MB [2]–[4]. Therefore, running an SNN model, whose size is larger than the on-chip memory, on such a hardware needs excessive DRAM accesses. This problem is even more critical for Edge-AI applications where SNNs are deployed on low-cost embedded devices with a small-sized on-chip memory, leading to high DRAM energy consumption. This hinders (embedded) SNN hardwares from achieving further energy-efficiency gains, as the DRAM access energy is relatively higher than other operations (e.g., neuron computations). Previous work [5] observed that the memory access energy during inference is dominant, consuming ca. 50%-75% of the total energy across different hardware platforms, as also shown in Fig. 1(b). The challenging research question is: If and how can we reduce the DRAM access energy for the SNN inference, while maintaining the accuracy. The solution to this issue will enable efficient SNN inference for energy-constrained devices and their applications for IoT-Edge and Smart CPS (cyber physical systems).

A. State-of-the-Art and Their Limitations

To reduce the energy of SNN inference, the state-of-the-art works have proposed different techniques, and can be categorized as follows:

• Reduction of the SNN operations through weight pruning [6], stochastic neural operations [4], and neuron elimination [7]. These approaches can reduce the number of DRAM accesses required for SNN parameters.
• Quantization that reduces the possible representable values for a single weight [6] [7]. This approach decreases the amount of data (i.e., weights) to be stored in and fetched from DRAM.

Limitations: These state-of-the-art works mainly target reducing the number of accesses, but do not optimize the DRAM energy-per-access and approximations in DRAM that provide an additional knob to achieve high energy efficiency. Therefore, these works can potentially hinder the SNN inference system exploiting the full potential of DRAM energy saving. The goal should be jointly minimizing the energy-per-access as well as the number of accesses, leveraging approximations in DRAM to expose the full energy saving potential, while overcoming the adverse effects of the approximation-induced errors.

To address these limitations, we propose to employ approximate DRAM (i.e., DRAM with reduced supply voltage) with efficient DRAM mapping and error-tolerant SNN training to substantially reduce the DRAM energy in SNN inference systems while preserving their accuracy. Note, our approach can also be combined with the above-discussed state-of-the-art existing techniques to further improve the energy-efficiency of SNN inference. For instance, Fig. 1(a) shows the estimated DRAM energy benefits achieved by our proposed technique combined with the weight pruning.

To highlight the potential of approximate DRAM, we present an experimental case study in the following section.

B. Motivational Case Study and Key Challenges

We analyze (1) the DRAM access energy consumed by different DRAM access conditions (i.e., a row buffer hit, a row buffer miss, and a row buffer conflict), and (2) the dynamics of DRAM array voltage (Varray), for both the original and the approximate DRAM scenarios. In a row buffer hit, the requested data is already in the DRAM row buffer, and hence the data can be accessed directly. Meanwhile, a row buffer miss or conflict has to open the requested DRAM row before the data can be accessed. The detailed information of the different DRAM access conditions will be discussed in Section II-B1.

For the experimental setup, we use the LPDDR3-1600 4Gb DRAM configuration. We employ the DRAMPower simulator [8] to obtain the...
DRAM access energy, as it is widely used in memory and architecture communities and has been validated against real measurements. We also employ the DRAM circuit model from [10] and the SPICE simulator to study the dynamics of DRAM array voltage. The original DRAM is operated with a 1.35V supply voltage, while the approximate one with 1.025V. More details on the experimental setup are presented in Section V. From the experimental results presented in Figs. 2(b) and 2(d), we make the following key observations:

- The reduced DRAM voltage reduces the DRAM energy-per-access, across different DRAM access conditions, i.e., 31%-42% energy savings per access.
- The row buffer hit incurs the least energy consumption, compared to the row buffer miss and the row buffer conflict conditions. Therefore, the row buffer hit should be maximized to reduce the DRAM access energy.

Although employing the approximate DRAM can significantly reduce the DRAM energy-per-access, it reduces the DRAM reliability as the bit errors increase along with the decreased supply voltage (see Fig. 2(c)). These errors will consequently reduce the accuracy of the SNN as they alter the weight values in DRAM. Therefore, the key challenge is how to ensure high energy savings considering approximate DRAMs, while minimizing their negative impact on the SNN inference accuracy under the targeted accuracy constraints.

C. Our Novel Contributions

To overcome the above key challenges, we propose SparkXD framework that enables a resilient and energy-efficient Spiking neural network inference using approximate DRAM. To the best of our knowledge, this work is the first effort that exploits approximate DRAM for improving the energy-efficiency of SNNs while enabling their error-tolerant training. Following are the novel steps performed in the SparkXD framework (the overview is illustrated in Fig. 3):

1) Improving the SNN Error Tolerance, so that the SNN inference achieves high accuracy, even in the presence of bit errors in approximate DRAMs. It is done by incorporating the error profiles from the given approximate DRAM into the training.

2) Analyzing the Error Tolerance of the Improved SNN Model to find the maximum tolerable BER that can be applied to the SNN model, while meeting the targeted accuracy. It is done by adjusting the BER values, while checking whether the obtained accuracy meets the user-specified accuracy.

3) DRAM Mapping for the Improved SNN Model to maximize DRAM row buffer hit and optimize the DRAM access energy, by placing the synaptic weights into the appropriate DRAM partition (e.g., subarray) whose error profile meets the BER requirement.

Key Results: We evaluated SparkXD framework for (1) accuracy, using Python-based simulations on GPGPU and Embedded GPU, with the MNIST and the Fashion MNIST dataset and (2) DRAM access energy, using DRAMPower [8]. The experimental results show that, for a target accuracy within 1% of the baseline SNN system with accurate DRAM, SparkXD reduces the DRAM access energy by approximately 40% on average, across different network sizes.
to a specific bank and decoded into the row and column addresses. Data from the requested row are copied to the row buffer when the activation (ACT) command is issued. Then, data can be read from or written to a specific column in the activated row buffer when the read (RD) or write (WR) command is issued. There are different possible DRAM access conditions: a row buffer hit, a row buffer miss, and a row buffer conflict [4]. A row buffer hit happens if the requested row is already activated, and the requested data is already in the row buffer. Hence, the data can be accessed directly. If the requested row is not yet activated, then the condition is either a row buffer miss or conflict. A row buffer miss happens if there is no activated row, hence it needs to activate the requested row before accessing the data. A row buffer conflict happens if the requested row is not yet activated, but the row buffer is still occupied by another activated row. Hence, this condition needs to close the activated row using the precharging (PRE) command, before activating the requested row using the activation (ACT) command. Fig. 5(b) shows the DRAM commands (i.e., ACT, RD or WR, and PRE) and the corresponding timing parameters (i.e., tRCD: row address to column address delay, tRAS: row active time, and tRP: row precharge time).

Fig. 6. The dynamics of the DRAM V_array and the timing parameters. The weak cells (i.e., cells that fail when the DRAM parameters reduced), and the probability of an error in any weak cell.

- **Error Model-1**: The bit errors have a vertical distribution across the bitlines of a DRAM bank. The errors are modeled by considering (1) the weak cells in bitline B, and (2) the probability of an error in the weak cells of bitline B.

- **Error Model-2**: The bit errors have a horizontal distribution across the wordlines of a DRAM bank. The errors are modeled by considering (1) the weak cells in wordline W, and (2) the probability of an error in the weak cells of wordline W.

- **Error Model-3**: It is a data-dependent error model, i.e., profile of the bit errors follow a uniform random distribution that depends on the content of the DRAM cells. The errors are modeled by considering (1) the weak cells, (2) the probability of an error in the weak cells that contain a 1 value, and (3) the probability of an error in the weak cells that contain a 0 value.

In this work, we employ the DRAM Error Model-0, because: (1) it produces the errors with high similarity to the real approximate DRAM; (2) it provides a reasonable approximation of other error models, i.e., approximation of (a) error distribution across bitlines like Error Model-1, (b) error distribution across wordlines like Error Model-2, and (c) uniform random distribution like Error Model-3; and (3) it offers fast error injection by software. Previous work [15] also used the Error Model-0 majority due to the similar reasons.

### IV. SparkXD Framework

**A. Overview**

We propose the SparkXD framework to enable a resilient and energy-efficient SNN inference in the presence of voltage-induced DRAM errors. The detailed steps of SparkXD are shown in Fig. 7 which are explained in the subsequent sections.

1) **Improving the Error Tolerance of SNN Model (Section IV-B)**

   It makes the SNN inference achieves high accuracy, even in the presence of bit errors in DRAM. It is performed by incrementally increasing the BER from 0 to a defined maximum BER in the training process, while considering the error profile from the DRAM error model.

2) **Analyzing the Improved SNN Error Tolerance (Section IV-C)**

   The idea is to find the highest BER for the improved SNN model that fulfills the user-specified inference accuracy. It employs a linear search on the given BER values, while checking if the corresponding accuracy meets the targeted accuracy. If so, the associated BER value is selected as the solution candidate.

3) **DRAM Mapping for the Improved SNN (Section IV-D)**

   It aims at optimizing the DRAM access energy for the improved SNN model through the following ideas: (1) data are mapped in the appropriate DRAM partition (e.g., subarray), whose error rate meets the BER requirement; and (2) data are mapped in a way that maximizes the row buffer hits, while exploiting DRAM multi-bank burst feature.

**B. Improving the SNN Error Tolerance**

The bit errors in the SNN weights can degrade the accuracy, since they alter the weight values and deviate the classification to a different...
Fig. 7. The SparkXD framework with novel steps highlighted in blue boxes. Towards this, we improve the SNN error tolerance through a training process that incorporates the error profile of the approximate DRAM. The proposed training has the following key steps.

- **Step-1**: The bit errors are generated for different BER values, based on the different $V_{\text{supply}}$ values and the DRAM error model-0 that follows a uniform random distribution across a DRAM bank.

- **Step-2**: The generated bit errors are then injected into the locations in DRAM. Therefore, the bits of data (weights) stored in these locations will be flipped. Here, as the baseline DRAM mapping, the weights are mapped in subsequent address space in a DRAM bank to exploit the DRAM burst feature and achieve high throughput. If a DRAM bank is already filled, then the weights are mapped in the different banks of the same DRAM chip.

- **Step-3**: Afterwards, we include the bit errors in the training process by incrementally increasing the BER value from a minimum error rate to a maximum one (the error rates are defined in the Step-1, while the locations of bit errors are defined in Step-2). Furthermore, we increase the BER after each epoch of training by a user-defined increment value (e.g., the next error rate is 10x of the previous one). In this manner, the SNN is gradually trained to tolerate the bit errors from the lowest rate to the given maximum rate, thereby carefully improving the SNN error tolerance.

### C. Analyzing the Error Tolerance of the Improved SNN Model

The accuracy of SNN inference needs to be maintained within the user-specified accuracy, even in the presence of bit errors in the synaptic weights. Towards this, our SparkXD framework analyzes the error tolerance of the improved SNN model, to find the maximum tolerable BER that can be applied in the SNN systems. It performs a linear search on the different BER values, which are obtained from Section IV-B). It searches from a minimum error rate to a maximum one, while checking whether the corresponding accuracy meets the user-specified accuracy. The linear search can be employed, because we found that the SNN error-tolerance curve is generally decreasing as the BER increases (see Fig. 8). This technique ensures that bit errors whose rate is below or equal to the maximum tolerable BER, will not decrease the accuracy under the user-defined target. This technique is also beneficial for devising a resilient and energy-efficient DRAM mapping, which is discussed in Section IV-D.

To synergistically employ the techniques from Section IV-B and Section IV-C, we devise Algorithm 1 for improving and analyzing the SNN error tolerance.

### D. DRAM Mapping for the Improved SNN Model

The improved SNN model needs to be placed properly in DRAM to ensure that the trained weights are minimally affected by bit errors in DRAM, and hence the classification accuracy is maintained. Towards this, our SparkXD employs a DRAM mapping policy to properly map the SNN weights in DRAM, while optimizing the DRAM energy-per-access. The proposed DRAM mapping is illustrated in Fig. 9(a), and following are the key ideas.

- The weights are mapped in the appropriate DRAM partition (e.g., channel, rank, chip, bank, or subarray), whose error profile meets the BER requirement, i.e., error rate $\leq$ maximum tolerable BER (BERth). In this work, we consider the subarray-level granularity for our DRAM mapping, since such a granularity level allows us to exploit the following aspects.
  - The DRAM multi-bank burst feature, which is available in the commodity DRAMS, can be employed to increase the data throughput. Its timing diagram is illustrated in Fig. 9(b).
  - The subarray-level parallelism, which is available in new DRAM architectures (such as in [14]), can also be employed to increase the data throughput.

- The weights are mapped in a way to maximize row buffer hits and minimize row buffer conflicts, for optimizing the DRAM energy-per-access. The reason is that the row buffer hit incurs the least DRAM access energy than other access conditions, as suggested by our experiments in Fig. 2(b).

#### Algorithm 1 Improving and analyzing the SNN error tolerance

**INPUT**: (1) Baseline SNN: model ($model_0$), accuracy ($model_0$.acc); (2) DRAM error model ($DRAMerr$), BER: error rates ($rates$), number of error rates ($N_{rates}$), number of epoch ($N_{epoch}$); (3) Test dataset: samples ($S_{test}$), number of samples ($N_{test}$); (4) Target accuracy: lower bound (acc_bound)

**OUTPUT**: (1) Improved SNN: model ($model_1$), accuracy ($model_1$.acc); (2) Maximum tolerable BER ($BER_{th}$)

**BEGIN**

1: $model_{temp} = model_0$
2: for $i = 0$ to ($N_{rates} - 1$) do
3:  $error = DRAMerr(rates[i])$; // error generation
4:  $error = model_{temp}.err$; // error injection
5:  $p = 0$ to ($N_{epoch} - 1$) do
6:  $r = 0$ to ($N_{train} - 1$) do
7:  $s = 0$ to ($N_{test} - 1$) do
8:  $test_{model_{temp}}(S_{train}[r])$; // train
9:  $test_{model_{temp}}(S_{test}[s])$; // test
10: if $model_{1}.acc \geq (model_{0}.acc - acc\_bound)$ then
11:  $model_1 = model_{temp}$;
12:  $BER_{th} = rates[i]$;
13:  return $model_1$

**END**
be prioritized for storing the weights (shown in Algorithm 2 line 7). 
(2) To maximize the row buffer hits and exploit the multi-bank burst feature, the DRAM mapping sequence in each DRAM chip follows the following policy (shown in Algorithm 2 lines 3-8).

- **Step-1:** We prioritize to map the data in different columns of the same row, to maximize row buffer hits. If all columns in the same row are filled, then the remaining data is mapped to a target subarray in a different bank. 
- **Step-2:** If the target subarray in the target bank meets the BER requirement, the remaining data is mapped to this subarray like in **Step-1**. Otherwise, this subarray is not used and we move the target to a subarray in a different bank. Afterwards, we perform the **Step-2** again. If all columns in the same row of all banks are filled/unavailable or unsafe, then the remaining data is mapped to a different subarray in the target bank.  
- **Step-3:** In the target subarray, remaining data is mapped in the same fashion as in **Steps-1** and **2**. If all columns in the same row of all safe subarrays across all banks are filled, then the remaining data is mapped to a different row, and we perform **Steps-1** to **3**.  
- **Step-4:** If some data still remains, it is mapped to different chips, ranks, and channels respectively, using the **Steps-1** to **3**.

Algorithm 2 The proposed DRAM mapping

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INPUT: (1) DRAM (DRAM), number of channel-per-module (nch), number of rank-per-channel (nrank), number of chip-per-rank (nchp), number of bank-per-chip (nbank), number of subarray-per-bank (nsub), number of row-per-subarray (nrow), number of column-per-row (ncol); (2) Error rates of subarrays (subarray_rate); (3) Data (data);
OUTPUT: DRAM (DRAM);
BEGIN
Process:
1: for ch = 0 to (nch - 1) do 
2: for ra = 0 to (nsub - 1) do 
3: for cp = 0 to (nchp - 1) do 
4: for ro = 0 to (nrow - 1) do 
5: for su = 0 to (nsub - 1) do 
6: for ba = 0 to (nbank - 1) do 
7: if subarray_rate[ch, ra, cp, ba, su] ≤ BERth then 
8: for co = 0 to (ncol - 1) do 
9: DRAM(ch, ra, cp, ba, su, ro, co) ← data;
10: return DRAM;
END
```

V. EVALUATION METHODOLOGY

The experimental setup for evaluating our SparkXD framework is shown in Fig. [10]. Following are the details of the experimental setup.

Accuracy Evaluation: We use a Python-based simulation with FP32 precision that run on GPGPU (Nvidia RTX 2080 Ti and Embedded GPU (Nvidia Jetson Nano), to show the generality of our solution across different compute and memory capabilities. We use the MNIST and the Fashion MNIST, and employ the rate coding and the Poisson distribution for converting the input samples into spike trains. For comparison partner, we consider the baseline SNN model which is trained without considering DRAM errors. We also define the target accuracy to be within 1% of the baseline SNN with accurate DRAM. For network architecture, we employ the fully-connected SNN with different number of neurons: 400, 900, 1600, 2500, and 3600 (i.e., N400, N900, N1600, N2500, and N3600, respectively).

Error Generation and Injection: We generate bit errors based on the DRAM error model-0, and inject them into the locations in DRAM. Based on the DRAM mapping policy, the data bits that are stored in the locations with errors, will be flipped. For the baseline mapping, we place the weights in subsequent addresses in a DRAM bank. For the mapping in SparkXD, we use the proposed Algorithm 2.

DRAM Energy Evaluation: We employ the DRAM circuit model from [10] and the SPICE simulator to extract the DRAM parameters (e.g., V_{supply}, t_{RCD}, t_{RAS}, t_{RP}), while considering LPDDR3-1600 4Gb DRAM configuration which is representative for the main memory of energy-constrained embedded systems. The accurate DRAM is operated with 1.35V of V_{supply}, while the approximate one is operated within the range of 1.025V-1.325V. Afterwards, we use the state-of-the-art and cycle-accurate DRAMPower [8] that consider the extracted DRAM parameters, as well as the DRAM access traces and statistics for estimating the DRAM access energy.

VI. RESULTS AND DISCUSSIONS

A. Improvements of the SNN Error Tolerance

Fig. [11] presents the results of accuracy for the baseline SNN with accurate DRAM, the baseline SNN with approximate DRAM, and the improved SNN with approximate DRAM.

We observe that the baseline SNN with approximate DRAM suffers from the accuracy degradation, as compared to the baseline SNN with accurate DRAM. Here, the accuracy decreases as the error rate increases. The reason is that, the weight bits are corrupted (flipped) when they are stored in the approximate DRAM, and these weights are not trained to adapt with such bit flips. On the other hand, the improved SNN with approximate DRAM, can maintain the accuracy within 1% of the baseline SNN with accurate DRAM, across different error rates, different network sizes, and different datasets. The minimum target accuracy is shown by a dashed-line pointed by label-1 in Fig. [11]. The reason is that, the SparkXD incorporates the error profile from the approximate DRAM in the training process. In this manner, our SparkXD trains the weights to adapt to the presence of bit errors, and thereby improving the SNN error tolerance.

Furthermore, we observe the impact of bit error locations in DRAM. The locations of bit errors are distributed based on the locations of weak cells and generated from the Error Model-0. Here, we found that when the bit errors flip the most significant bits (MSBs) of weights, then they change the corresponding weight values and the accuracy may be decreased significantly, as shown by label-2 in Figs. [11]. On the other hand, when the bit errors flip the less significant bits of weights, then the errors may not significantly change the corresponding weight values and the accuracy is not much affected. Therefore, in general, how the bit errors are distributed in DRAM has impact on the accuracy of SNN inference.

B. DRAM Access Energy Savings

Fig. [12] presents the experimental results of the DRAM access energy for the baseline SNN with accurate DRAM and the improved SNN with approximate DRAM, across different V_{supply} values, different network sizes, and different datasets/workloads (the MNIST and the Fashion MNIST). These two workloads have similar DRAM access energy, since they have the similar number of weights and number of DRAM accesses for inference. The reduction of the V_{supply} to 1.325V, 1.25V, 1.175V, 1.1V, and 1.025V using our SparkXD, saves the DRAM energy by the 3.84%, 13.33%, 22.69%, 31.12%, 39.46% on average respectively, across different network sizes. For each network size, following are the detailed results when reducing the V_{supply} to 1.325V, 1.25V, 1.175V, 1.1V, and 1.025V.
Fig. 11. The accuracy of the baseline SNN with accurate DRAM, the baseline SNN with approximate DRAM, and the improved SNN with approximate DRAM, for (a) the MNIST and (b) the Fashion MNIST datasets, across different BER values and different network sizes.

VII. CONCLUSION

We propose a novel SparkXD framework to achieve resilient and energy-efficient SNN inference under approximate DRAM, through error-aware SNN training, SNN error-tolerance analysis, and error-aware DRAM mapping. SparkXD reduces the DRAM energy by ca. 40% on average, while maintaining the accuracy within 1% of the baseline SNN with accurate DRAM. Furthermore, our work would enable further studies on the resilient and energy-efficient SNN.

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