A 76-81 GHz CMOS mmW Quadrature Down-Conversion Mixer for Automotive Radar Applications

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Abstract This paper presents a mmW quadrature down-conversion mixer for 76-81 GHz automotive radar applications. A transformer-based gm-rethinking method and a new cascade inter-stage network are proposed to improve the gain of preamplifier. A pair of cross-coupled transistors are exploited to bleed dynamic current into mixer core to reduce noise figure while utilizing its negative resistance to improve conversion gain. The mixer is implemented in a 55-nm CMOS process and the measurement results show that the BW is 5.5 GHz, the peak gain is 4.1 dB with < 0.16 dB I/Q mismatch, the input P1dB is up to -6 dBm and the minimum noise figure (NF) is 19 dB while dissipating 40 mW of power. The achieved FOM is up to 0.02.

key words: CMOS, mmW, Transformer-based, GM-rethinking, Inter-stage network, Cross-coupled transistors, Bleed dynamic current

1. Introduction

The frequency-modulated continuous wave (FMCW) Radar is a key sensing module of advanced driver assistance systems (ADAS) and autonomous vehicles due to its detection capability of long range and robustness to environment variations, such as inclement weather and extreme lighting scenarios [1]. In the past, automotive radars are generally realized using GaAs and SiGe processes due to its higher level and also lower noise. However, with the widespread deployment of radars, the CMOS technology has become an charming choice in order to reduce cost and improve integration level [2, 3]. The CMOS FMCW radars have been widely studied [4–14] in recent years.

A typical automotive radar system is illustrated as Fig. 1. The local oscillator (LO) generates a LO signal whose frequency linearly and periodically changes with time. The continuous wave RF signal is transmitted through power amplifier (PA) and reflected after encountering obstacles. The receiver (RX) will receive the reflected signal and mix it with the LO signal to produce an intermediate frequency (IF) signal. Based on the IF frequency (Δf + and Δf −), we could calculate the obstacle distance through the transmission flight time and the moving speed by the Doppler effect. Also as shown in Fig. 1, the TX-to-RX feedthrough will require a highly-linear RX. The RX linearity is generally limited by the down-conversion mixer. Besides, the mixer should provide some gain to suppress noise contributions from successive building blocks, such as baselband amplifiers and ADC. How to realize a high linearity, high gain and low noise mmW mixer has become a research hotspot [15–25].

In [21], a 65-nm CMOS down-conversion mixer implements a -3 dBm input P1dB without dissipating power while only achieving -6 dB gain due to its passive topology. The sub-harmonic mixer shown in [22] provides a peak gain of 9 dB. However, it realizes a part of gain by the IF amplifier, which deteriorates the entire noise performance. The measured NFmin is larger than 22 dB. Reference [17] reports a mixer fabricated in 130 nm SiGe BiCMOS which achieves a peak gain of 14.5 dB and a NFmin of 6.3 dB. However, it realizes high gain and low noise with a deteriorated input P1dB of -24.5 dBm and high power consumption of 76 mW. This paper presents a CMOS quadrature down-conversion mixer operating at 76-81 GHz for automotive radar applications. A transformer-based gm-rethinking preamplifier is used to improve gain. A new interstage network to eliminate parasitic capacitance and the cross-coupled transistors for bleeding dynamic current are proposed to improve noise figure and conversion gain. The rest of the paper is organized as follows. Section 2 describes circuit design. Section 3 presents measurement results and Section 4 concludes this paper.

2. Circuit design

Fig. 2(a) shows schematic of the proposed preamplifier used in the mmW down-conversion mixer. In order to drive the
quadrate mixer, a passive power divider is utilized at the final stage of the preamplifier. The 3-D view of the power divider is shown in Fig. 2(b). It is made of the top copper layer (thickness is 3.3 μm) and the sub-top copper layer (0.9 μm) to provide high Q factor.

2.1 Transformer-based \( g_m \)-boosting preamplifier

As shown in Fig. 2(a), a transformer-based \( g_m \)-boosting method is designed to optimize the gain of the mmW preamplifier. The transformer-based \( g_m \)-boosting network consists of one primary coil and two secondary coils. Magnetic coupling between the primary coil and two secondary coils provides in-phase signals. Two secondary coils can provide anti-phase signals through crossing connection between the gate and the source of transistor, effectively improving \( g_m \) of the TM1 and TM2. Differential circuit could be equivalently analyzed in the single-ended and the differential ground is marked by gray color as shown in Fig. 2(a). The principle of transformer-based \( g_m \)-boosting could be analyzed as follows:

\[
V_g = \frac{M_1}{(L_1/L_2)Z_2(1 - k^2)s + L_1} \quad (1)
\]

\[
Z_2 = \frac{1}{sC_{gs}} + sL_3 + \frac{g_m \cdot L_3}{C_{gs}} \quad (2)
\]

where \( V_i \) is the RF input amplitude of preamplifier, \( V_g \) is the gate voltage of TM1, while \( L_1, L_2 \) and \( L_3 \) are self inductances of the primary coil and two secondary coils, respectively. \( M_1 \) and \( M_2 \) are mutual inductances between \( L_1 \) and \( L_3 \), and between \( L_1 \) and \( L_2 \), respectively, while \( k \) is the coupling coefficient. \( Z_2 \) is the input impedance looking into the gate of TM1 while ingoring neutralization capacitance. \( V_g \) and \( Z_2 \) will have similar forms with eqs. (1) and (2). For tight coupling, \( k \) is close to 1, the equivalent transconductance can be written as

\[
G_m = \frac{g_m \cdot V_g}{V_i} = \frac{M_1}{(L_1/L_2)Z_2(1 - k^2)s + L_1} + \frac{M_2}{(L_1/L_3)Z_3(1 - k^2)s + L_1} \cdot \frac{g_m = M_1 + M_2}{L_1} \cdot \frac{g_m}{3} \quad (3)
\]

Thus, \( g_m \) is boosted by \( (M_1 + M_2)/L_1 \) according to eq. (3). Fig. 3 shows simulated gain of two common source (CS) amplifiers. Comparing with the traditional topology, the \( g_m \)-boosting amplifier features 2.7 dB higher gain without extra power consumption. Layout and 3-D view of the input \( g_m \)-boosting transformer is illustrated as Fig. 2(b). The primary coil is made of the top copper layer (thickness is 3.3 μm) to guarantee a high Q factor. Two secondary coils are respectively made of the sub-top copper layer (0.9 μm) and the top aluminum layer (1.17 μm) to reduce parasitic coupling between two overlapping windings.

2.2 A new cascode inter-stage network

In mmW bands, the cascode inter-stage parasitic capacitance will significantly decrease amplifier gain. The \( \pi \)-type [26] and \( T \)-type [27] matching networks are two traditional methods to eliminate this parasitic effect. As shown in Fig. 4(a), a \( L_s \) and two parasitic capacitors of \( C_1 \) and \( C_2 \) can form a \( \pi \)-type matching network. Here, \( C_1 \) includes \( C_{gs7} \) and \( C_{sb7} \), while \( C_2 \) includes \( C_{db5} \) and \( C_{gd5} \). However, there is a big difference between the CG transistor input impedance of \( 1/g_m \) and the CS transistor output impedance of \( r_o \). It is difficult to match them through a single inductor of \( L_s \) because \( C_1 \) and \( C_2 \) are both parasitic capacitance whose value are usually not controllable. As shown in Fig. 4(a), the matching mechanism could be analyzed in the current domain. The CG transistor input impedance of \( 1/g_m \) will not affect resonating frequency but only lower the Q factor, the
output current of TM7 can be calculated as

\[ I_{out} = I_{in} \cdot \frac{1}{\frac{1}{1 + sC_2} \cdot \frac{g_m}{g_m + sC_1}} \]

(4)

when \( L_s \) and \( C_1 \) are resonating, the \( L \)-type impedance transforming network could change the CG transistor input impedance into

\[ Z_{in} = \frac{1}{g_m \cdot (1 + Q^2)} \]

(5)

where \( Q \) is the quality factor of LC-tank and mainly decided by the \( L_s \) inductor. If this inductor is lossless, the output current of TM7 can be written as

\[ I_{out} = I_{in} \cdot \frac{g_m}{g_m + sC_1} \]

(6)

However, the \( L_s \) inductor is lossy, and then the \( C_2 \) capacitor will shunt a part of \( I_{in} \). Fig. 4(b) shows a modified \( \pi \)-type inter-stage network. Through using a \( L_{p2} \) inductor to resonate with \( C_2 \), it will reduce the current wasted by \( C_2 \). Fig. 5 shows simulation results using different inter-stage networks. The blue curve represents a result corresponding to Fig. 4(a) and the red curve represents a result corresponding to Fig. 4(b). The Fig. 4(b) topology shows 1 dB higher gain than that of Fig. 4(a). In differential amplifier, the neutralization technology [28] is generally used to eliminate parasitic capacitance between gate and drain terminals as shown in Figs. 4(b). Thus, a \( C_2 \) only including \( C_{db5} \) is always much less than the \( C_1 \) including \( C_{gs7} \) and \( C_{eb7} \). To resonate with a small \( C_2 \), a large-sized inductor will cause layout design difficulty. For example, a \( L_{p2} \) of 400 pH is required when the \( TM_5 \) size is 12 \( \mu m \)/60 nm. The structure shown in Fig. 4(b) is more suitable for those large-sized power amplifiers. Based on the above analysis, \( C_2 \) is relatively small and ignored in the successive analysis. However, \( C_1 \) will still shunt a part of \( I_{in} \). Fig. 4(c) proposes a new inter-stage network to eliminate this parasitic capacitance of \( C_1 \). The resonating frequency consisting of \( L_s \), \( L_p \) and \( C_1 \) is calculated as

\[ \omega_0^2 = \frac{L_s + L_p}{L_pL_sC_1} \]

(7)

Comparing eqs. (9) and (10), we can find that the \( Z_2 \) is higher than the impedance of \( C_1 \), which effectively improves the current flowing into source terminal of TM7. As shown in Fig. 5, the Fig. 4(c) topology shows 1.8 dB higher gain than that using Fig. 4(a). Compared to a \( L_{p2} \) of 400 pH in Fig. 4(b), the employed \( L_p \) in Fig. 4(c) is only 75 pH.

2.3 Bleeding dynamic current into mixer core

Fig. 6(a) shows schematic and layout of the proposed active mixer. Comparing with the passive mixer, the active mixer generally features higher gain. Based on [29], the output noise current contributed by switch transistors could be written as

\[ i_{o,n} = V_n \cdot \frac{I}{\pi A} \]

(11)

where \( V_n \) represents the gate noise voltage of switch transistors and \( A \) is the amplitude of LO signal. Current bleeding method could effectively reduce noise caused by switch transistors in active mixer [30]. By injecting a fixed current into mixer core, the equivalent current passing through switch transistors decreases. This static bleeding current is implemented by two current sources, as shown in Fig. 6(c) by grey color. However, when the \( g_m \) decreases, which raises the input impedance seen into the source of switch transistors. As a result, the signal current shunted by parasitic capacitance increases, which finally causes a lower conversion gain. Fig. 7 shows the simulated conversion gain using various architectures. The pink curve represents the native mixer and the green curve represents the mixer with static current bleeding. The static current bleeding method deteriorates the conversion gain by 1.5 dB at 75 GHz. Because the
The single-ended impedance seen from X node to the right side is written as

\[ Z_X = \frac{-R_c/g_m}{R_e - 1/g_m} \]  

If \( 1/g_m \approx R_e \), the \( Z_X \) will be much larger than the \( R_e \), which effectively improve \( Q \) factor and more signal current will flow into switch transistors. As shown in Fig. 7, the blue curve shows the simulated gain with the parallel inductor while bleeding static current, the red curve represents the result only using the parallel inductor and the black curve shows the simulated result with the parallel inductor while bleeding dynamic current. Comparing with other structures, the method combinatorially using parallel inductor and bleeding dynamic current shows the highest conversion gain.

3. Measurement Results

The chip photograph of the proposed 76-81 GHz quadrature down-conversion mixer is shown in Fig. 8. The area is 1104 \( \mu \text{m} \times 595 \mu \text{m} \). The chip is measured by on-probe method and the GSG pitch is 100 \( \mu \text{m} \). The single-ended LO is converted into orthogonal signals through RC-CR poly-phase filter, after being amplified by a two-stage cascode amplifier, they are used to drive switch transistors of the mixer core. The LO orthogonal and differential precision is optimized at 77 GHz. The differential precision of I- and Q-paths are 2 and 2.7 degree, respectively. The orthogonal precision between I- and Q-path is 3.1 degree. The differential peak-to-peak amplitude is 850 mV in I-path, while 876 mV in Q-path. As shown in Fig. 9, the proposed down-conversion mixer realizes \(<-10 \text{ dB} \ S_{11} \) from 70 to 110 GHz. The conversion gain is measured by sweeping RF and LO frequency synchronously, while keeping the IF frequency be a constant value of 0.5 GHz. The measured peak gain with 50 \( \Omega \) IF load approaches 4.1 dB and the 3 dB bandwidth is up to 5.5 GHz with the maximum in-band I/Q gain mismatch of 0.16 dB. Fig. 10 shows the measured input-referred P1dB up to -6 dBm and Fig. 11 shows the measured NF. The NF is less than 23.5 dB when the IF is from 10 MHz to 5 GHz and the \( NF_{\text{min}} \)
Table I: Performance Summary and Comparison with the Prior CMOS mmW mixers.

| Ref. | Tech.          | Freq.(GHz) | Conversion Gain(dB) | IP1dB(dBm) | Noise Figure(dB) | PowerDC(mW) | FOM*** |
|------|----------------|------------|---------------------|------------|------------------|-------------|--------|
| [15]EL 14 | 90-nm CMOS | 75-85       | 1.5                 | -9         | 23.3             | 13          | 0.004  |
| [16]IMS 17 | 0.18-µm SiGe | 60         | 10                  | -23        | 18               | 39.6        | 0.0038 |
| [17]MWCL 14 | 0.13-µm SiGe | 76.8       | 14.5                | -24.5      | 6.3              | 76          | 0.0005 |
| [18]TDMR 16 | 65-nm CMOS | 65-75       | -1                  | -4         | N/A              | N/A         | N/A    |
| [19]IMS 19 | 90-nm CMOS | 57-67       | 3                   | -10        | N/A              | 12.7        | N/A    |
| [20]MWCL 17 | 90-nm CMOS | 57-66       | 8                   | -7.6       | 13               | 55          | 0.025  |
| This Work | 55-nm CMOS | 76-81       | 4.1                 | -6         | 19               | 20**       | 0.02   |

∗ Single path of I or Q; ∗∗ FOM=[Gain(abs):f0(GHz):IP1dB(mW)]/[PDC(mW)-NF(abs)].

Fig. 9: Measured S-parameters and conversion gain of the proposed 76-81 GHz quadrature down-conversion mixer.

Fig. 10: Measured input P1dB of the proposed down-conversion mixer.

Fig. 11: Measured noise figure of the proposed down-conversion mixer.

is 19 dB at 0.6 GHz. Table 1 summarizes the measured performance and compares it with the prior CMOS mmW down-conversion mixers published in recent years. The proposed down-conversion mixer compromises the noise, gain and linearity and achieves a competitive FOM.

4. Conclusion

A 76-81 GHz mmW quadrature down-mixer for automotive radars is implemented in a 55-nm CMOS technology. A transformer-based gm boosting technique and a novel cascode inter-stage network are proposed to improve the gain of the preamplifier without extra power consumption. In mixer design, we bleed dynamic current into mixer core while utilizing negative resistance effect to achieve gain improvement and noise reduction. A competitive FOM is finally realized.

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