A quadrature LO-generator using an external single-ended clock receiver for dual-band WLAN applications

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Abstract A low phase noise quadrature LO-generator for dual-band wireless local area network (WLAN) applications is presented. The quadrature LO-generator is composed of a clock receiver, a CML divider, and two quadrature dividers for the dual-band, respectively. A clock receiver converts the single-ended clock to a differential signal. Then a quadrature divider with a 25% duty cycle generates four quadrature signals for mixers. The split-grounded architecture and multiply ground pads decrease the inductive component of ground impedance as well as the ground bounce of the single-ended input. The phase noise is −143 dBc/Hz and −149 dBc/Hz at 1 MHz offset in the 2.4-GHz and 5-GHz bands, respectively.

Keywords: quadrature local oscillator (LO), clock receiver, single-ended, WLAN, quadrature frequency divider, dual-band

1. Introduction

Low IF (Intermediate frequency) quadrature architecture has been widely applied to WLAN transceivers, and quadrature signals are generally generated by a local oscillator (LO). Many papers reported quadrature LO circuits, such as a quadrature voltage-controlled oscillator (QVCO), a passive RC polyphase filter (PPF), an injection-locked ring oscillator (ILRO), and a divide-by-two circuit. References [1, 2, 3] adopted QVCO to generate quadrature signals, which were achieved by quadrature dividers or a single sideband (SSB) mixer. QVCO method reduced the requirement of frequency-tuning range, while sacrificed chip area due to required two LC oscillators. Furthermore, references [4, 5, 6, 7] generated quadrature LO by passive RC PPF, however, the phase error was more sensitive to PVT (process, supply, temperature) variations. Besides, references [8, 9, 10] presented ILROs, which were operated multiply mode of frequency division and the required frequency-tuning range was increased, while ILROs were vulnerable to PVT variation because of the narrow lock range, and phase noise was sensitive to the deviation of harmonic frequency and input frequency. Typical divide-by-two circuit generated quadrature wideband frequency, while it required high power consumption and resulted in higher phase error [10, 11, 12, 13].

To independently measure the performance of the quadrature LO-generator, the VCO is bypassed and an external clock source is used as the input. Consequently, a high-speed single-ended receiver is required. High-speed receivers have been broadly applied to inter-chip communication, such as multi-core processors [14], electrical/optical interconnect [15], memory interconnect [16, 17]. To satisfy the increasing demands for high data-rates, a high-performance receiver needs to be wideband, reliable, and energy-efficient [18, 19, 20].

This letter presents a high-speed clock receiver with the following functions: impedance matching, amplifying, single-ended to differential transforming, and configurable bypass. Furthermore, it provides wideband and low phase noise quadrature dividers, which are operated at 2.4-GHz and 5-GHz bands, respectively.

The letter is organized as follows. Section 2 describes the ground bounce of a single-ended input and an equivalent model of a bonding wire. Section 3 provides circuits of clock receiver, CML divider, and quadrature divider. Fabricated in 55 nm CMOS technology, the simulation results of the clock receiver and quadrature LO-generator are demonstrated in section 4. Finally, this work is summarized in section 5.

2. Model of the bonding wire

The passive mixers demand a quadrature clock of large voltage swings, whose 25% duty-cycle alleviates many issues, such as I/Q crosstalk, and unbalanced sideband gains, and noise contribution of the following stages [21, 22, 23].

Fig. 1 shows the quadrature LO-generator for WLAN applications. The clock receiver converts the external single-ended clock at 9.6–11.8 GHz to a differential output, which provides the input of the CML divider and the 5-GHz band quadrature divider, respectively. Then, the 2.4GHz quadrature divider generates quadrature LO after a CML (current mode logic) divider.

Power supplies and an external single-ended clock are transmitted to a chip by bonding wires, which connect a chip pad and a printed circuit board (PCB) pad. However, the high-speed signals incur more notable ground bounce due to bonding wire inductors and pad capacitors [24, 25, 26]. Furthermore, the ground bounce is equivalent to a common-mode noise and added to all signals shared the same reference ground [27, 28, 29].

The equivalent model of a bonding wire is shown in
Fig. 2. (a) Model of single bonding wire. (b) Model of a bonding wire with signal source.

As shown in Fig. 3 (a), a single-ended signal \(V\text{HF}\) at high speed incurs the ground bounce \(V\text{AVSS}\). As plotted in Fig. 3. (b), the low-frequency signal \(V\text{LF}\) is added to the ground bounce noise. Furthermore, a high-speed signal is significantly attenuated due to LC-filter loss. Although differential signals can overcome the common-mode noise, LC-filter loss is inevitable.

It is assumed that the number of ground bonding wires is \(n\), the number of input signal bonding wires is \(m\). \(R_S\) is the source impedance, and \(R_g\) is the off-chip ground impedance. To consider the input impedance of \(V_S\), let

\[
Z_X = \frac{1}{sL} + \frac{1}{sC_p} + \frac{1}{sR} = \frac{1}{sL} + \frac{1}{sC_p} + \frac{1}{sR} \quad (1)
\]

Compared to source clock \(V_S\), the input signal \(V_S\) is significantly attenuated due to the passive network. As the frequency of the \(V_S\) becomes higher, \(V\text{AVSS}\) approximates to \(V\text{IN}\), thus the amplitude of common-mode noise further increases.

\[
V_{\text{IN}} = V_S \left( \frac{R/n + sL/n + 1/(smC_p)}{R_s(smC_p)Z_X + n} + Z_X \right) \quad (2)
\]

\[
V_{\text{AVSS}} = V_S \left( \frac{R/n + sL/n}{R_s(smC_p)Z_X + n} + Z_X \right) \quad (3)
\]

As the frequency of the input signal increases, the ground bounce is more severe and \(V\text{AVSS}\) becomes larger.

The signal-to-ground ratio defines SGR, which reflects the frequency response of the amplitude of the signal-to-ground ratio. As shown in Fig. 4, SGR deteriorates with signal frequency increasing, even the amplitude of ground approximates to the signal around 10 GHz frequency, which the SGR decreases to 0dB. Significantly, as the number ratio of ground-to-signal bonding wires \(n/m\) increases, the SGR relatively increases. Therefore, to relax the effects of ground bounce, the inductive term \(sL\) and the resistive term \(R\) should be smaller. And an adequate number of ground pads is required.

3. Clock receiver and quadrature LO with 25% duty cycle

As shown in Fig. 1, the blocks of the dual-band Quadrature LO-
LO-Generator are presented. The clock receiver is shared by 5GHz Quadrature LO-Generator and 2GHz quadrature LO-Generator, which consists of a CML divider and a quadrature divider, and the 5GHz block merely includes a quadrature divider after the clock receiver.

### 3.1 Clock receiver

As shown in Fig. 5, the clock receiver provides impedance matching, amplifying, and single-ended to differential transforming.

Impedance matching network reuses bonding wires of packaging and inner matching network of LC passive network to achieve wideband frequency resonance. Amplifier adopts the RC feedback to broaden the matching bandwidth. The load of the amplifier is a transformer that converts the single-ended signal to the differential outputs, which provide high gain over the wideband.

![Fig. 5](image)

**Fig. 5** Circuit of single-ended clock receiver.

### 3.2 Quadrature divider

The quadrature divider uses two dynamic latches to generate quadrature phases. Fig. 6 is the quadrature divider circuit, which is based on the reference [30]. When CK\(_P\) is high, two pull-up transistors M\(_{11}\) and M\(_{12}\) are off, the outputs of V\(_{IP}\) and V\(_{IN}\) obtain low. Once CK\(_P\) turns low, V\(_{IP}\) is assumed to turn high, V\(_{IN}\) keeps low due to regenerative loops. In addition, V\(_{QP}\) and V\(_{QN}\) were low, otherwise it would violate the assumption of high V\(_{IP}\). When CK\(_N\) turns low, V\(_{QN}\) turns high and V\(_{QP}\) holds low due to M\(_3\) is on, respectively. Thus, four phases alternately turn high in two periods, and the quadrature outputs achieve the 25% duty cycle.

### 3.3 CML divider

The block of the 2.4-GHz band adopts a CML divider, and the 9.6-10GHz frequency of the external clock is divided-by-two before the 2.4GHz quadrature divider.

Fig. 7 presents the circuit of the CML divider, which is adapted to a high-speed signal. The CML divider is composed of two cross-coupled inverters, which merely use NMOS devices to provide moderate voltage swings and obtain faster state transitions, while it consumes more static power.

### 4. Simulation results

Fabricated in a 55 nm CMOS technology. The clock receiver, quadrature divider, and CML divider are operated at 1.5V, 1.5V, and 1.2V supplies, respectively, by the internal LDOs converting 3.3V supplies. The quadrature LO-generator consumes 11.81mW at the 2.4-GHz band, which includes 4.13mW of the CML divider and 7.68mW of the quadrature divider, as well as 12mW at the 5-GHz band, respectively. Fig. 8. (a)-(b) shows the layout of the clock receiver and the quadrature divider. The chip areas are 0.225 mm\(^2\) (including pads) and 0.03047 mm\(^2\), respectively. The total area is 0.286 mm\(^2\) (including pads).

#### 4.1 Clock receiver

Fig. 9 displays the S-parameters of the clock receiver, whose return loss is below -15dB at the band of 9.6 – 11.8 GHz. From single-ended input to the differential output, it achieves
7.8 - 12 dB gain, the clock receiver consumes much power to overcome the parasitic loss, such as LC-filter loss and ground bounce at the high-speed frequency.

Fig. 10 describes the transient waves of differential outputs of the clock receiver. VP and VN represent the differential outputs of the transformer. The passive network of bonding wire incurs notable power supply fluctuation, which is the common-mode noise, and the amplitude of the added noises in AVDD and AVSS are identical due to large decoupling capacitors. To suppress the common-mode noises, a transformer is used to isolate the clock receiver and dividers (including quadrature divider and CML divider, which are loads of the clock receiver), and the clock receiver adopts independent power supplies, which are different from the dividers. Therefore, the differential phases of VP to AVDD and VN to AVDD more approximate to 180°.

Table I summarizes the simulations of the clock receiver.

4.2 Quadrature divider

Fig. 11. (a)-(b) present I/Q transient waves of the quadrature generators at 2.4GHz and 5.8 GHz, respectively. Phase noises are shown in Fig. 12 at 2.4GHz and 5.8GHz frequencies. It is demonstrated that phase noises at 1MHz offset are −148.6dBc/Hz and −142.9dBc/Hz at 1MHz offset frequency.

Table II compares this work with previously reported quadrature LO-generators. The proposed quadrature LO-generator achieves the single-ended to the differential transforming of external VCO and low phase noise with a compact area of 0.235 mm².
5. Conclusion

A quadrature LO-generator is presented in this letter, which consists of a low phase noise clock receiver, CML divider, and two quadrature dividers. Converting a single-ended external clock at 9.6 – 11.8GHz to quadrature LO outputs for dual-band WLAN applications. It adopts three-stage architecture, multiple ground pads, and independent power/ground to decrease the ground bounce of a single-ended input at high-frequency. The circuit provides four-phased quadrature LO signals with a 25% duty cycle for TX and RX mixers, respectively. As a result, the quadrature LO-generator achieves phase noises of -148.6dBc/Hz and -142.9dBc/Hz at 1MHz offset in 2.4-GHz and 5-GHz bands, respectively.

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