Energy-delay performance of giant spin Hall effect switching for dense magnetic memory

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We show that the giant spin Hall effect (GSHE) magnetoresistive random access memory (MRAM) can enable better energy delay and voltage performance than MTJ spin torque devices at 10–30 nm scaled nanomagnet dimensions. We propose a dense bit cell composed of a folded electrode to enable scaling to sub-10 nm CMOS. We derive the energy-delay trajectory and energy-delay product of GSHE and MTJ devices with an energy minimum at the magnetic characteristic time. Optimized GSHE devices with PMA can enable low voltage (<0.1 V), scaled dimensions, and fast switching time (100 ps) at an average switching energy approaching 100 aJ/bit. © 2014 The Japan Society of Applied Physics

Fig. 1 (a) Three-terminal spin Hall memory device with spin Hall effect write electrode and MTJ-based readout. (b) Top view of the cell showing the orientation of the free layer magnet and the GSHE metal.

Fig. 1(a), where the magnet is oriented along the width of the GSHE electrode for appropriate spin injection. The magnetic cell is written by applying a charge current via the GSHE electrode, the direction of the magnetic writing is determined by the direction of the applied charge current. Positive currents (along +y) produce a spin injection current in the transport direction (along +z) and spins pointing to the +x-direction. The injected spin current in turn produces spin torque to align the magnet in the +x- or −x-direction. The transverse spin current \( I_x = I_w - I_s \) with spin direction \( \hat{\sigma} \) for a charge current \( I_x \) in the write electrode is given by

\[
I_s = P_{SH}(w, \lambda_{SF}, \theta_{GSHE}) \left( \hat{\sigma} \times I_w \right),
\]

where \( P_{SH} = (I_T - I_j)/(I_j + I_T) \) is the spin Hall injection efficiency (SHIE), which is the ratio of the magnitude of the transverse spin current to the lateral charge current, \( w \) is the width of the magnet, \( t \) is the thickness of the GSHE metal electrode, \( \lambda_{SF} \) is the spin flip length in the GSHE metal, and \( \theta_{GSHE} \) is the SHE angle for the GSHE metal to the FM1
interface. The injected spin angular momentum responsible for the spin torque is given by $S = n I_s / 2 e$.

We show that a novel 1T–1MTJ three-terminal SHE-MTJ bit cell with folded electrodes is appropriate for a scaled CMOS design with a unidirectional metal design rule. The proposed cell provides excellent cell density (1.5 P × 1.5 M4) with no penalty due to the three-terminal configuration. The proposed bit cell and integration scheme are shown in Fig. 2. The bit cell comprises an MTJ, a write transistor, and three terminals connected to BL\textsubscript{read} and BL\textsubscript{write}, and to the drain of the select transistor [Fig. 2(a)]. The charge current responsible for SHE passes from M2-BL\textsubscript{write} via the V2–M1–V1–M2 current path. The metal layer M2-SHE is selectively optimized for SHE injection efficiency. The metal layers M0/M2/M4 run parallel to enable differential read and write. Figure 2(b) shows a pseudodesign-rule-compliant bit cell laid out for scaled CMOS design rules of unidirectional metal lines$^{23}$ and close to uniform pitch to accommodate high-density routing.$^{23}$ The folded current path is described in Fig. 2(c), which shows the vertical stacking of three bit lines with no density loss. The via landing and alignment issues are identical to those of a traditional 1T–1MTJ cell in terms of similar design constraints. The cross section of the device along the MTJ (perpendicular to the gate direction) is shown in Fig. 2(d). MTJ occupies the vertical space for V3–M3–V4 with 100–200 nm space to accommodate a typical MTJ stack. Note that the traditional 1T–1MTJ STT device would be limited by the drive transistor sizing to accommodate the high resistance of the MTJs in scaled nodes, combined with the unidirectional design rules$^{22}$ and uniform pitch at low metal layers.$^{23}$ The 1T–1SHE device provides competitive density to a 2-terminal device.

We show that an effective spin injection efficiency $>100\%$ can be obtained using an optimum SHE electrode thickness for 30 nm nanomagnet width. We show the SHIE ratio of spin current injected to the charge current in the electrode as a function of electrode thickness (Fig. 3), which has an optimum value at 2–3 nm electrode thickness. The SHIE is given by

$$P_{\text{SHE}} = \frac{I_i}{I_s} = \frac{\pi w}{4 t} \theta_{\text{SHE}} \left[ 1 - \text{sech} \left( \frac{t}{\lambda_{\text{ef}}} \right) \right].$$  

In Fig. 3(a), we show the SHIE as a function of the thickness of the spin Hall metal electrode for a 30-nm-wide ($w$) free layer. In Fig. 2(b), we show SHE as a function of nanomagnet width. SHIE decreases monotonically with scaled magnet dimensions. However, SHE remains $>100\%$ for $\beta$-W even with highly scaled magnets. A higher SHE implies a lower required charge current with associated benefits in the control transistor areal footprint [Fig. 3(b)].

We show that the GSHE devices scale to operating voltages $<0.1$ V using an analytical scaling model for voltage and write delay of GSHE and MTJ memory devices. The analytical relationship connecting the switching time to the write voltage of a spin torque memory with critical voltage $v_c$ is given by

$$\tau = \frac{\tau_0 \ln(\pi/2\delta_0)}{v/v_c - 1},$$  

where

$$v_{\text{SHE}} = 8 \rho L \left[ \theta_{\text{SHE}} \left( 1 - \text{sech} \left( \frac{t}{\lambda_{\text{ef}}} \right) \right)^{\frac{1}{\pi L}} \right].$$

Here, $\delta_0 = \sqrt{k_B T / 2 E_0}$ is the effect of stochastic variation owing to thermal noise; $E_0 = (1/2)\mu_0 M_s H_s V$ is the thermal barrier of the magnet of volume $V$, saturation magnetization $M_s$, and anisotropy $H_a$, and $\tau_0 = M_s V / I_s P_{\mu S}$ is the characteristic time. $I_s$ is the critical current for spin-torque-induced magnetic switching. We have verified the validity of Eq. (3) via stochastic spin torque simulations of a nanomagnet. We compare the switching time and voltage relationship of the GSHE device with that of the MTJ with nominal device parameters for a nanomagnet with a 40 kT thermal barrier. We assumed in-plane magnets for this comparison. The assumed
material properties are shown in Fig. 4. From Fig. 4(a), we can see that the operating voltage range for MTJ devices is restricted to voltages higher than those for SHE owing to the high resistance of a magnetic tunnel junction device. Secondly, GSHE does not suffer from the polarization degradation due to voltage effects,\(^1\) which limit the peak injected currents and operating speed of MTJs to > 1 ns.

We derive the optimum electrode dimensions and relative switching energy of STT-MTJ and GSHE-MTJ devices for identical nanomagnet dynamics. For identical delay and critical currents, the relative switching energy of GSHE writing to STT-MTJ devices is

\[
\frac{E_{\text{she}}}{E_{\text{MTJ}}} = \left( \frac{P_{\text{MTJ}}}{R_{\text{MTJ}}} \right) \left( \frac{R_{\text{she}}}{P_{\text{she}}} \right) = \frac{2\rho_{\text{she}}}{\pi^2 u t_0 \rho_{\text{she}}^2 [1 - \text{sech}(t/\lambda_{\text{she}})]^2}. \tag{5}
\]

To understand dimensional scaling, the ratios of the energy required to switch using identical nanomagnets are plotted in Fig. 5. We note that the relative energy scales with the resistance of the write electrode and is inversely proportional to the square of the spin injection efficiency. For MTJ devices, the product \(R_{\text{MTJ}}/P_{\text{MTJ}}\) is fundamentally constrained, since reducing the tunneling resistance is coupled with reducing the spin polarization. However, this trade-off may be broken for GSHE devices if materials with high \(\theta_{\text{SHE}}\) and low resistivity \(\rho_{\text{SHE}}\) can be identified.\(^{15,18,19}\) The relative energy of GSHE as a function of the thickness of the GSHE electrode shows (Fig. 5) an optimum near \(t_0 = 3\lambda_{\text{eff}}\) with 10–100x improvement in relative energy over STT-based MTJs. The relative energy improvement is retained for highly scaled magnets of 10–20 nm widths using the optimum GSHE electrode geometry. The relative energy advantage is significantly higher for larger nanomagnet widths and may have implications for high-retention and robust microcontrollers with low density requirement.\(^{27}\)

We compare the energy delay (ExD) trajectories of GSHE and MTJ (GSHE-MTJ) devices for in-plane magnet switching as the applied write voltage is varied. The ExD trajectory (for in-plane switching) can be written as

\[
E(t) = R_{\text{write}}I_{\text{co}}^2 \left[ \tau + \frac{\tau_0}{2} \ln\left( \frac{\pi}{2\theta_0} \right) \right]^2 \rightarrow \frac{4}{\hbar^2} \frac{R_{\text{write}}}{P^2} \frac{1}{\tau} \left[ \tau + \frac{\tau_0}{2} \ln\left( \frac{\pi}{2\theta_0} \right) \right]^2, \tag{6}
\]

where \(R_{\text{write}}\) is the write resistance of the device (\(R_{\text{GSHE}}\) or \(R_{\text{MTJ-AP}}, R_{\text{MTJ-AP}}\)) and \(P\) is the spin current polarization \(P_{\text{GSHE}}\) or \(P_{\text{MTJ}}\). We also note that \(\tau_0 = M_sV_e/L\mu_{\text{H}}\) varies as the spin polarization varies for various GSHE metal electrodes (Fig. 3). The combined effect of spin Hall polarization, damping, and resistivity of the spin Hall electrodes is captured in Eq. (6) and plotted in Fig. 6(a). All the cases considered in Fig. 6(a) assuming a 30 × 60 nm magnet with a 40 kT thermal energy barrier and a 3.5 nm GSHE electrode thickness. The ExD trajectories of the devices are obtained assuming a voltage sweep from 0 to 0.7 V in accordance with the voltage restrictions of scaled CMOS.\(^{6}\) The ExD trajectory of the GSHE-MTJ devices broadly exhibits two operating regions: Region 1 where the ExD product is approximately constant (\(\tau_d < M_sV_e/L\mu_{\text{H}}\)) and Region 2 where the energy is proportional to the delay \(\tau_d > M_sV_e/L\mu_{\text{H}}\). The two regions are separated by energy minima at \(\tau_{\text{opt}} = M_sV_e/L\mu_{\text{H}}\), where the minimum switching energy is obtained for the spin torque devices. The ExD trajectory of the STT-MTJ devices is limited with a minimum delay of 1 ns for in-plane devices at 0.7 V maximum applied voltage; the switching energies for P–AP and AP–P are approximately 1 pJ/write. A design space exists to improve the ExD trajectory of the STT-MTJ devices by a judicious design of domain wall physics and the cancellation of out-of-plane demagnetization.\(^{28}\) In contrast, the ExD trajectory of the GSHE-MTJ (in-plane) devices enables us to obtain switching times as short as 20 ps (\(\beta-W\) with 0.7 V, 20 fJ/bit) or switching energies as small as 2 fJ (\(\beta-W\) with 0.1 V, 1.5 ns switching time).

Finally, we compare the energy delays of GSHE-MTJ and STT-MTJ devices for in-plane and perpendicular magnetic anisotropy (PMA). The spin orientation of the injected electrons using a planar GSHE electrode does not directly allow...
the switching of a PMA device [see Eq. (1)]. We note that an integrated solution for SHE-current-switching-scaled PMA devices remains an important and outstanding problem for VLSI applications of GSHE. However, alternative techniques may be feasible where a remnant dipole field\(^9,24,25\) or an exchange bias field\(^20\) is applied or asymmetric structures are realized\(^21\), such that a noncollinear spin torque can switch a PMA device. We hope that the scaling study presented here motivates this exploration. The ExD function of GSHE-MTJ and STT-MTJ switching with PMA is given by

\[
E(t) = \frac{R_{\text{write}} f_{\text{co}}}{2} \left[ \tau + \tau_0 \ln\left(\frac{\tau}{2\tau_0}\right) \right]^2.
\]

The effect of PMA on the switching ExD of GSHE-MTJ- and STT-MTJ-based devices is shown in Fig. 6(b). From Fig. 6(b), we can see that at 1 ns delay, the switching energy of the PMA-GSHE-MTJ device compared with that of the PMA-STT-MTJ device is reduced to 100 aJ/bit from 100 fJ/bit. Alternatively, PMA-GSHE-MTJ devices can be used to reduce the switching time to 10 ps. The PMA β-W design [red line with solid squares in Fig. 6(b)] corresponds to an ExD of 50 aJ/ns using an optimum geometry spin Hall electrode \(t_{\text{GSHE}} = 2.3 \text{ Åf}, P_{\text{GSHE}} \sim 170\%\) with \(30 \times 60 \text{ nm}^2\) magnets and a 40 kT thermal barrier representing a \(\geq 100\times\) improvement in ExD while operating under a low voltage of \(<0.1\) V. We have also verified that the high current density of the SHE device in the write electrode is below the electromigration threshold for short sections of wires, as given by the Blech-length effect.\(^26\) The expected critical \(J_{\text{fail}}\) \(\times\) length for ultra-short wire sections is expected to be above \(1 \text{ GA/cm}^2\).

In conclusion, we describe a dense SHE bit cell and study the voltage, spin injection, and ExD scaling of GSHE switching. We show that the spin injection efficiency of GSHE can exceed 100% even with highly scaled nanomagnets. We also identify the optimum electrode geometry for spin injection efficiency (to minimize the write current) and the optimum switching energy conditions. Using a voltage/energy-delay scaling relation for GSHE-MTJ devices, we show that GSHE devices enable a much lower ExD product (PMA: 50–100 aJ/ns, InP: 0.4–3 fJ/ns) than STT-MTJ devices enabling 100 aJ/switching with switching times as short as 10 ps at 0.1–0.4 V. We further note that an integrated solution for GSHE-PMA switching for scaled devices remains to be developed. GSHE (and giant spin–orbit current) devices represent a significant opportunity for the development and integration of CMOS-compatible spintronic memory and logic devices.

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1) I. Žutić, J. Fabian, and S. Das Sarma, Rev. Mod. Phys. 76, 323 (2004).
2) C. Chappert, A. Fert, and F. N. Van Dau, Nat. Mater. 6, 813 (2007).
3) A. Brataas, A. D. Kent, and H. Ohno, Nat. Mater. 11, 372 (2012).
4) D. E. Nikonov and I. A. Young, IEDM, 2012.
5) S. Manipatruni, D. E. Nikonov, and I. A. Young, IEEE Trans. Circuits Syst. I 59, 2801 (2012).
6) W. H. Butler, X. G. Zhang, T. C. Schultness, and J. M. MacLaren, Phys. Rev. B 63, 054416 (2001).
7) Web [http://www.irste.net/Links/2011FTRS/Home2011.htm].
8) I. M. Miron, K. Garello, G. Gaudin, P. Zernatten, M. V. Costache, S. Aufré, S. Bandiera, B. Rodmacq, A. Schuhl, and P. Gambardella, Nature 476, 189 (2011).
9) L. Q. Liu, C. F. Pai, Y. Li, H. W. Tseng, D. C. Ralph, and R. A. Buhrman, Science 336, 555 (2012).
10) C.-F. Pai, L. Liu, Y. Li, H. W. Tseng, D. C. Ralph, and R. A. Buhrman, Appl. Phys. Lett. 101, 122404 (2012).
11) T. Kimura, Y. Otani, T. Sato, S. Takakashi, and S. Maekawa, Phys. Rev. Lett. 158, 156601 (2007).
12) K. Ando, S. Takahashi, K. Harii, K. Sasaue, J. Jeda, S. Maekawa, and E. Saitoh, Phys. Rev. Lett. 101, 036601 (2008).
13) O. Mosendz, J. E. Pearson, F. Y. Fradin, G. E. W. Bauer, S. D. Bader, and A. Hoffmann, Phys. Rev. Lett. 104, 046601 (2010).
14) P. Laczkowsk i, J.-C. Rojas-Sánchez, W. Savero-Torres, H. Jaffrès, N. Reynen, C. Deranlot, L. Notin, C. Beigné, A. Marty, J.-P. Attatna, L. Vila, J.-M. George, and A. Fert, Appl. Phys. Lett. 104, 142403 (2014).
15) Y. Niimi, Y. Kawanishi, D. H. Wei, C. Deranlot, H. X. Yang, M. Chshiev, T. Valet, A. Fert, and Y. Otani, Phys. Rev. Lett. 158, 156602 (2012).
16) Y. M. Lee, J. Hayakawa, S. Ikek, F. Matsukura, and H. Ohno, Appl. Phys. Lett. 89, 042506 (2006).
17) C. Wang, Y. T. Cui, J. A. Katine, R. A. Buhrman, and D. C. Ralph, Nat. Phys. 7, 496 (2011).
18) M. Morota, Y. Niimi, K. Ohnishi, D. H. Wei, T. Tanaka, H. Kontani, T. Kimura, and Y. Otani, Phys. Rev. B 83, 174405 (2011).
19) M. Gradhand, D. V. Fedorov, P. Zahn, and I. Mertig, Phys. Rev. Lett. 105, 186403 (2010).
20) M. Belmeguenai, T. Devolder, and C. Chappert, J. Appl. Phys. 97, 083903 (2005).
21) G. Yu, P. Upadhyayana, Y. Fan, J. G. Alzate, W. Jiang, K. L. Wong, S. Takei, S. A. Bender, L. T. Chang, Y. Zhang, J. Yang, T. Wang. Y. Grover, P. Upadhyaya, P. Khalil, P. Amiri, and K. L. Wang, Nat. Nanotechnol., (2014).
22) D. Ingerly, A. Agrawal, R. Ascanbili, A. Blattner, M. Buehler, V. Chakarmambe, B. Choudhury, F. Cinnor, C. Ege, C. Gunpam, T. Glassman, R. Grover, P. Hentges, J. Hicks, D. Jones, A. Kandas, H. Khan, N. Lazo, K. Lee, H. Liu, A. Madhavan, R. McCaffrend, T. Mule, D. Parsons, P. Parthangal, S. Ranagur, D. Rao, J. Roosler, A. Schmitz, M. Sharma, J. Shin, V. Shusterman, N. Speer, P. Tiwari, G. Wang, P. Yashar, and K. Mistry, IEEE Int. Interconnect Technology Conf. (IITC), 2012, 1,3.
23) C.-H. Jan, U. Bhattacharya, R. Brain, S.-J. Choi, G. Curello, G. Gupta, W. Hafiez, M. Kang, M. Kang, K. Komey, T. Leo, N. Nidhi, L. Pan, J. Park, K. Phoa, A. Rahman, C. Staus, H. Tashiro, C. Tsai, P. Vandervoorn, L. Yang, K. Y. Yeh, and P. Bai, IEDM Tech. Dig., 2012, 3-1.
24) K. Garello, C. O. Auvi, M. Miron, O. Bouline, S. Aufré, P. Gambardella, and G. Gaudin, (2013) arXiv:1311.5586.
25) M. Cubukcu, O. Bouline, M. Drouard, K. Garello, C. O. Avci, I. M. Miron, J. Langer, B. Ocker, P. Gambardella, and G. Gaudin, (2014) arXiv:1311.5586.
26) D. Nee, F. Federspiel, V. Ginzult, O. Thomas, and P. Gergaud, IEEE Trans. Device Mater. Re却. 6, 175 (2006).
27) G. Kortuem, F. Kwast, D. Fitton, and V. Sundramoorthy, IEEE Internet Comput. 14, 44 (2010).
28) H. Zhao, B. Glass, P. K. Amiri, A. Lyle, Y. Zhang, Y.-J. Chen, G. Rowlands, P. Upadhyayana, Z. Zeng, J. A. Katine, J. Langer, R. Galatisis, H. Jiang, K. L. Wang, I. N. Krirovorov, and J.-P. Wang, Phys. D 45, 025001 (2012).