COMET: A Comprehensive Cluster Design Methodology for Distributed Deep Learning Training

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Abstract—Modern Deep Learning (DL) models have grown to sizes requiring massive clusters of specialized, high-end nodes to train. Designing such clusters to maximize both performance and utilization—to amortize their steep cost—is a challenging task requiring careful balance of compute, memory, and network resources. Moreover, a plethora of each model’s tuning knobs drastically affect the performance, with optimal values often depending on the underlying cluster’s characteristics, which necessitates a complex cluster-workload co-design process. To facilitate the design space exploration of such massive DL training clusters, we introduce COMET, a holistic cluster design methodology and workflow to jointly study the impact of parallelization strategies and key cluster resource provisioning on the performance of distributed DL training. We develop a step-by-step process to establish a reusable and flexible methodology, and demonstrate its application with case studies of training large models on cluster configurations of variable compute, memory, and network resources. Our case studies demonstrate COMET’s utility in identifying promising architectural optimization directions and guiding system designers in configuring key model and cluster parameters. To illustrate, cluster configuration comparisons identify performance differences of up to $7.7 \times$ and highlight performance optimization opportunities of up to $1.4 \times$ when employing memory expansion as an optimization technique.

I. INTRODUCTION

Modern Deep Learning (DL) workloads such as natural language processing [68], [78], drug discovery [19], [72], text-to-speech conversion [3], [60], [70], and personal recommendation engines [46], [83] are becoming increasingly pervasive and commercially important, forming the core components of many day-to-day applications and services deployed in datacenters. The rapid growth of these models has culminated in massive resource requirements (terabytes of memory, petaflops of compute) to train in a practical timeframe. Training is therefore conducted in a distributed fashion over massive clusters of high-end specialized accelerator nodes, such as GPUs or TPUs, connected over high-bandwidth networks [28], [44].

Fig. 1: Tunable cluster component parameters in COMET and value ranges evaluated in this paper.

Given the abundance of available compute (GPU, TPU, custom accelerator), network (Ethernet, InfiniBand, NVLink), and memory system (HBM, DRAM over DDR or CXL) technologies, as well as the steep cost of such clusters, designing them for maximum performance and efficiency is a challenge of high complexity and critical importance.

Optimizing a cluster for distributed DL training requires keen understanding of key model characteristics, training strategies, and hardware components. Maximizing efficiency not only requires carefully balancing the cluster’s compute, memory, and network characteristics, but also adjusting the model’s parallelization strategy to best suit those underlying hardware resources. Therefore, a holistic, end-to-end methodology is needed to analyze and understand the impact of different system components and training strategies on each cluster’s DL training performance and efficiency.

To address this need, we introduce the COMET methodology, which allows rapid joint exploration of cluster resource provisioning and training parallelization strategies. COMET includes a detailed workflow to break down a model into its layers, analyze its training behavior as a function of the employed parallelization strategy, and assess the impact of a cluster’s key resources on training performance and efficiency. COMET is a versatile tool that helps cluster designers determine the optimal resource provisioning balance for a set of target training algorithms. The methodology also enables researchers and technologists to study and quickly quantify the impact of emerging technologies or of any modification of a given component’s characteristics (e.g., per-node compute density, memory capacity or bandwidth, network bandwidth or latency, etc.) on distributed DL training performance and efficiency.

In summary, we make the following contributions:

- We construct the holistic COMET methodology to enable rapid design space co-exploration of model training parallelization strategies and key cluster resource parameters, to assess their joint impact on the performance of distributed DL training.
- We implement our methodology with a streamlined toolchain.
and showcase its utility with case studies using different large Deep Learning Recommendation Models (DLRM) and language (Transformer) models. 

- COMET helps system architects rapidly quantify the impact of various current and future accelerators, network capabilities, and memory system technologies on cluster performance and efficiency. We particularly emphasize the potential of memory expansion techniques (e.g., CXL-attached memory) as an understudied yet promising cluster design knob.

**Paper outline:** §II covers background and related work. §III details COMET’s methodology and §IV its implementation. §V demonstrates COMET’s utility with use cases and §VI concludes.

## II. Background and Related Work

### A. Distributed DL Parallelization Strategies

In recent years, we have witnessed tremendous growth in DL model sizes, with current largest models already trending in the 100s of billions or trillions of parameters [15], [38], [68]. Training models of such size requires tremendous computational and memory resources, only attainable on massive clusters with hundreds of (typically GPU-based) computing nodes. Given a cluster deployment, there is a range of parallelization strategies to choose for distributed DL training such as Data Parallelism (DP) [37], Model Parallelism (MP) [65], [66], Pipeline Parallelism (PP) [21], and more general parallelization strategies (e.g., expert parallelism [15]). COMET currently focuses on analyzing the effects of the two foundational parallelization strategies of MP and DP\(^1\), but its modular design allows future extension to model other strategies as well.

In MP training, the model is split across the nodes, hence each node holds a shard of the model, requiring frequent inter-node communication both during forward and backward propagation. In contrast, in DP training, each node holds the entire model and the training batch is shared across nodes. Inter-node communication is only required on backward propagation to reconcile weight updates across the multiple model copies. As a result, MP training generally requires more frequent synchronous inter-node communication, while DP training results in less frequent but more voluminous communication, which is easier to overlap with computations.

### B. Challenges in Distributed DL Training

The performance and efficiency of a cluster used in distributed DL training is dictated by a range of key parameters: per-node computational capability, memory capacity and bandwidth, and the inter-node network bandwidth. In addition to raw hardware capabilities, a training task’s performance is affected by the training task’s structure (i.e., the chosen parallelization strategy), as that affects the resulting workload characteristics and, consequently, how each cluster resource is being stressed. Limiting our scope to the two foundational MP and DP parallelization strategies, the chosen MP/DP balance for a given training task drastically affects the workload’s characteristics, bearing significant implications in the resulting computation/communication balance, per-node memory capacity requirements, and, ultimately, the distributed training’s performance and efficiency. Therefore, optimizing training performance requires holistic co-design of the parallelization strategy alongside the cluster’s memory, compute, and network resources. The COMET methodology enables composite studies where cluster resource provisioning strategies and parallelization strategies for a training task are jointly varied.

### C. Prior Work on Distributed DL Training

**DL training accelerator design.** A vast body of prior work focuses on optimizing the individual accelerator node (GPU or custom accelerator) [8], [9], [29], [33], [51], [52], [63]. However, node design in isolation does not capture cluster-scale effects during distributed training and can lead to resource imbalance and cluster under-utilization. Maximizing cluster-wide performance and utilization requires a holistic design approach that jointly considers the impact of compute, network, memory, and workload parallelization strategy.

**Cluster-scale DL training performance analysis.** Closer to our work, some prior work characterizes the performance of large-scale distributed training on current clusters. Jain et al. evaluate the performance of training ResNet and Inception models on different CPU and GPU architectures, as a function of batch size, node count, and threads per node [23]. Ren et al. analyze the distributed training performance of NLP and computer vision workloads leading-edge systems, providing insights into the collective communication kernels and the impact of node count scaling on overall training throughput [61]. Jeon et al. focus on multi-tenant GPU clusters hosting co-located DNN training workloads, study how locality-aware scheduling affects performance and utilization, and propose guidelines for improved cluster schedulers [25].

**Cluster communication performance optimizations.** Another family of work focuses on cluster communication performance, which is often a major performance determinant. Dong et al. propose an algorithm/system co-design methodology to improve training scalability, by alleviating network congestion with a congestion-less server architecture that uses novel communication collective algorithms and network topology [14]. Jiang et al. accelerate DNN training with a unified communication framework that dynamically adapts reduction collectives and parameter server tasks to best utilize CPU and bandwidth resources, and overlap communication latency [27]. Shah et al. and Sun et al. propose communication abstraction and improvised communication algorithms [64], [69].

**Memory system impact on training.** Memory system design and optimizations play a crucial role in the overall performance and efficiency of a distributed training cluster, as well as the cluster size required to train a given large model. Prior works such as Checkmate [24], ZeRO-DP [53], ZeRO-Offload [59],
and ZeRO-Infinity [54] focus on reducing the per-node memory footprint required to train large DL models.

**Training strategy auto-tuning frameworks.** Prior works on auto-tuning frameworks (Alpa [85], AutoDDL [7], Rhino [82], FlexFlow [26]) focus on identifying the optimal parallelization strategy using a combination of data, operator and communication patterns. These frameworks perform an exhaustive design space search to identify the optimal parallelization strategy for a given cluster. While auto-tuning frameworks predict the optimal parallelization strategy for a DL model training task on a specific cluster, COMET develops a generic methodology to jointly evaluate the performance of a training strategy on an arbitrary cluster at an earlier design stage: when a cluster’s architecture is still malleable, i.e., going under design considerations. Our goal is not to identify the best parallelization strategy for training a given DL model on an existing cluster, but rather to enable rapid design space exploration and evaluation of impact of various model parallelization strategies along with key architectural cluster design parameters. COMET currently does not automate the workload and cluster design space exploration. A future extension could add a frontend layer in the toolchain that automates generation of workload input files (representing different parallelization strategies) and cluster configurations (i.e., steps 2 and 5 in Fig. 5, described in §IV).

All aforementioned categories of prior work provide valuable insights to understand the performance characteristics of individual components of a large training cluster. However, a cluster design approach that jointly considers the training parallelization strategy along with the cluster’s key architectural parameters is essential to not only maximize performance and efficiency, but also identify the true impact any individual or combination of future changes will have on the metrics of interest. We, therefore, argue for a holistic cluster design methodology encapsulating: (i) the target model to be trained with the range of possible parallelization strategies, each node’s (ii) compute and (iii) memory subsystem, and (iv) the cluster’s network. Understanding these tradeoffs at scale is challenging, and we are not aware of a publicly available unified framework that allows researchers to perform such broad design space exploration quickly. **COMET is a methodology and toolchain that aims to fill that gap, facilitating rapid iterations of algorithm/hardware co-design for large-scale DL training.**

![Fig. 2: COMET methodology overview.](image)

![Fig. 3: Variation of per-node memory capacity requirements as a function of MP and DP degrees in a fixed-size cluster.](image)

### III. THE COMET METHODOLOGY

We design the COMET methodology to holistically evaluate a large-scale model’s training strategy on an arbitrary cluster and assess the best combination of training strategy and cluster resource balance to maximize training performance and/or cost efficiency. Fig. 2 shows a high-level overview of our methodology and this section details each of its steps.

#### A. Workload Modeling

The first step involves decomposing the model of interest into its layers, along with the number of operations and data movement requirements in each layer. We express each layer as a general matrix-matrix multiplication (GEMM) between input activations ($M \times K$) and weights ($K \times N$), producing an output matrix ($M \times N$). After decomposing the model into layers, we compute the number of parameters for the operand matrices of each layer. The total size of a model, in terms of number of parameters, is given by the sum of the weight matrices' (i.e., $K \times N$) elements [73]. Layers that cannot be encoded as GEMMs (e.g., embedding-lookups) are represented by their input/output operand sizes, total number of operations and data moved between memory and the compute unit.

#### B. Training Strategy Configuration

In this step, we determine the parallelization strategy for the selected model based on the model type and per-node memory capacity. Different strategies focus on optimizing training for different metrics such as throughput, compute utilization, inter-node communication, etc. The current version of COMET focuses on Data and Model parallelism (MP and DP—see §II-A). Given a target cluster size, we compute the per-node memory capacity requirement as a function of the selected degree of MP and DP in the cluster. We compute the per-node memory footprint to hold all the data (model, input/output matrices) required for the distributed DL training task. The model’s memory footprint is dictated by model states and activations. We compute the memory footprint required for each operand matrix based on its type (i.e., model weights or input/output activations), size of parameters, and the memory optimizations (e.g., ZeRO-DP, as explained later in Section §IV). For a cluster of size N, we start with the initial condition where all the nodes are within the MP dimension (i.e., $MP = N, DP = 1$) and, collectively, hold a single copy of the entire

2In this paper, the term “node” refers to one compute unit (e.g., a GPU, a CPU, a TPU, etc.).
model. Then we sweep the (MP, DP) degree to the other extreme (i.e., \( MP = 1, DP = N \)), considering all power-of-two combinations, with \( MP \times DP = N \).

Doubling the DP dimension implies halving the MP dimension, so half the number of nodes must hold an entire copy of the model. Consequently, the per-node memory capacity requirement doubles. To illustrate, Fig. 3 shows a cluster configured as two data-parallel node groups (\( DP = 2 \)) and each DP node group consisting of \( m \) nodes performing \( m \)-way model parallelism (\( MP = m \)), for a total node count \( N = 2m \). To contain a copy of the entire model of size \( C \) across each DP group’s \( m \) nodes, each node requires a minimum memory capacity \( P = \frac{C}{2m} \). Moving from a \( DP = 2, MP = m \) to a \( DP = 4, MP = \frac{m}{2} \) configuration doubles the per-node memory capacity requirement to \( 2P \), as each DP group of \( \frac{m}{2} \) nodes now hold the entire model \( C \). As a result, the cluster’s total memory capacity also doubles from \( 2mP \) to \( 4mP \).

The chosen (MP, DP) degree not only affects the memory requirement per node, but also results in different computation requirements and communication behavior. Therefore, for each (MP, DP) combination, we also derive the volume of per-node computation and inter-node communication.

### C. Distributed Training Time Estimation

The computation and communication requirements per layer for each (MP, DP) combination are fed into a performance model that estimates the model’s training time. The performance model estimates end-to-end training time as a function of the modeled cluster’s per-node compute capability, memory capacity and bandwidth, network bandwidth and topology.

A key design decision in COMET is opting for generality and breadth rather than detailed modeling of individual components, as our methodology is intended to enable rapid and scalable exploration of a vast design space, rather than highly accurate performance estimations. COMET’s goal is to allow gleaning performance trends as cluster parameters are varied both jointly and separately. Therefore, we chose to go with detailed analytical models for compute, memory, and network rather than be tied to any specific technology or component instance. Performance estimation for DL training models lends itself well to analytical modeling (as opposed to cycle-level simulation), as their computation, memory access, and communication patterns exhibit regularity typically absent from general workloads [5], [39]. By sweeping generic characteristics like TOPS, bandwidth, latency, COMET’s users may easily create proxies for specific components or technologies of interest, such as GPUs with different computational capabilities, memories with different capacity/bandwidth characteristics (e.g., HBM vs. DDR), or networks with different bandwidth/latency characteristics (e.g., InfiniBand vs. NVLink). Next, we describe how individual performance models are constructed and tied together in COMET.

#### Compute delay estimation

To produce compute-delay estimations independent of any compute node’s microarchitectural details, we employ a roofline model [49], [77]. In each case, the compute node of interest is represented by its peak performance (\( perf_{\text{peak}} \) in GFLOPS) and memory bandwidth.

![Fig. 4: Roofline model. Attainable performance shifts for the same OI, depending on available memory bandwidth.](image-url)
methodology’s utility and decouple the results of the conducted case studies from any specific compute unit’s microarchitectural characteristics.

2) Memory traffic estimation: Memory traffic is the cumulative number of bytes transferred between the main memory and compute unit while performing the desired functionality. For a hypothetical compute node with infinite on-chip buffer space, all operands can be fetched exactly once from the memory, resulting in a very high OI (cf. Eqn. (1)). However, every realistic compute unit’s limited on-chip buffer space can only hold a limited set of data operands. Therefore, a layer’s matrix operands must usually be fetched multiple times from the memory to complete the required operations, thereby lowering the resulting OI. We construct a linear model to better estimate the memory traffic for a GEMM operation on a compute node with an on-chip buffer of configurable size.

Consider a GEMM operation between two matrices of $U$ and $V$ bytes, generating an output matrix of $W$ bytes. We assume one of the input operands is tiled to fit in the on-chip buffer, and the other operand/output are streamed in/out of the compute node, respectively. For an on-chip buffer size of $S$ bytes, we estimate the memory traffic (in bytes) as $\min\{\Psi_1, \Psi_2\} + W$, where $\Psi_1 = \lceil U/S \rceil \times V + U$ and $\Psi_2 = \lceil V/S \rceil \times U + V$. In practice, for $U$ and $V >> S$, tiling the smaller operand results in less data movement (e.g., if $U < V$, $\Psi_1$ is the tiling method of choice, resulting in about $V - U$ less data movement).

An additional important architectural design knob we want to investigate with COMET is that of memory expansion, whereby the compute unit’s local memory (LM) is enhanced with a secondary level of memory, which we refer to as expanded memory (EM). Such a setting can be enabled by allowing the compute unit to directly access its host CPU’s memory, or by physically attaching additional memory over CXL [12], photonic links, or other (current or future) technology. Investigating such an option using CXL-attached memory (which offers considerably higher bandwidth per pin than DDR) for DL training is of particularly high relevance given the growing interest in deploying it as a new memory hierarchy component [18], [36], [40].

To investigate this system design option, we consider per-node memory expansion, with the available bandwidth as our sensitivity analysis knob. To model performance with such a hybrid memory system, we instrument our roofline model with the new memory system’s effective memory bandwidth ($bw_{\text{hybrid}}$), which depends on the fraction of data accessed from local/expanded memory ($data_{\text{LM}}/data_{\text{EM}}$) at the local/expanded memory’s bandwidth ($bw_{\text{LM}}/bw_{\text{EM}}$). We estimate the hybrid memory system’s effective bandwidth as:

$$bw_{\text{hybrid}} = \frac{\text{total data accessed}}{bw_{\text{LM}} \cdot data_{\text{LM}} + bw_{\text{EM}} \cdot data_{\text{EM}}} \quad (3)$$

To illustrate, accessing 240GB of data in a hybrid memory system with 80GB of LM, $bw_{\text{LM}} = 27B/s$, and $bw_{\text{EM}} = 17B/s$ results in $bw_{\text{hybrid}} = 1.2TB/s$. Using Eqn. (3), we can determine the cluster’s performance as a function of the bandwidth offered by the hypothetical memory expansion technique used.

3) Communication delay estimation: During the training process, nodes continuously exchange data. Their communication delay is dictated by the total communication volume, the aggregate network bandwidth available between the nodes, and the dynamic network utilization. In addition, depending on the training phase, the communication among the nodes may be blocking or non-blocking. In the forward-pass and input-gradient phases, communication is blocking along the model-parallel dimension; in the weight-gradient phase, communication is non-blocking across the data-parallel dimension. Blocking communication falls on the critical path of a training phase, while non-blocking communication can be (partially) overlapped with compute, thus ameliorating its impact on resulting training time. The combination of data movement volume, available network bandwidth, communication type, and concurrently performed computation, dictates how much of the occurring communication is exposed, affecting training time. Ultimately, for each layer, the total exposed communication delay determines whether the layer is compute- or communication-bound on a given system configuration.

4) Total training time estimation: Finally, we combine the per-layer compute delays (§III-C1) with each layer’s corresponding communication characteristics (data volume and communication type—§III-C3) to determine the degree of computation/communication overlap and derive the training time per iteration and, by extension, total training time.

Overall, COMET comprises an iterative training time estimation process as shown in Fig. 2. For each model, different training strategies are considered (cf. §III-B) and the training time is estimated as described in §III-C. The process is repeated for different cluster sizes, and compute, network, and memory parameters to guide the user’s selection of parallelization strategy and cluster resource provisioning to optimize for the target metric of merit—raw training performance, or training efficiency (i.e., training time relative to resources deployed).

IV. COMET IMPLEMENTATION

Fig. 5 shows the implementation of our toolchain implementing the COMET methodology. The toolchain’s frontend, in steps (1) and (2), generates parameters for the per-layer computation and communication requirements. These parameters are then fed into the toolchain’s backend, which models the resulting performance of the training task, as a function of the target cluster’s configuration (steps (3) and (4)).

A. DL Model Analysis

In step (1), we analyze the DL model of interest and break it down into its layers. Each layer is represented as a sequence of GEMMs of input activations, model parameters, and resulting output activation matrices. The size of each matrix dimension $M, K, N$ is derived from the model’s hyper-parameters and batch size. Depending on the model type, a set of fixed independent hyper-parameters form the model’s signature. For example, in case of Transformers, hidden-dimension, # layer-stacks, and # attention-heads characterize the model size. Then, based on the derived GEMM dimensions, we compute the total
number of model and activation parameters required for each layer. In addition, the size of each operand matrix (i.e., input activations, model parameters, and output matrices) per node is affected by the MP/DP degree.

**B. Parallelization Strategy**

In step (2), we select a parallelization strategy for the given workload, generate the corresponding workload input file and feed it to the performance simulator to estimate the distributed training time. In addition, the workload’s required memory footprint is computed by aggregating model parameters, optimizer states, gradients, residual states, and checkpoint-activations. The workload input file must describe the characteristics of each layer of the workload, which includes the number of floating-point operations, data volume (in bytes) moved between memory and compute, communication collective, and communication volume (in bytes). As per ZeRO-Infinity, we compute the total number of operations and matrix operands required in both forward (FP) and backward (i.e., input gradient (IG) and weight gradient (WG)) training phases.

As described in §III-C2, we estimate the bytes transferred between the processor and main memory for each layer in each training phase. Similarly, we estimate the total number of operations and matrix operands required for each layer in each training phase. Based on the parallelization scheme used for the workload, we also determine the communication collective and compute the communication volume required per layer in each training phase, as well as the required per-node memory footprint to fit the model states and working dataset.

We use ZeRO-DP (os+g) [53], a.k.a. ZeRO-2, to derive the per-node memory footprint of model-states. ZeRO-2 avoids replication of optimizer states and gradients on each node and distributes them across the data-parallel dimension to reduce the per-node memory footprint, while avoiding additional communication overhead. For residual states, we estimate the memory footprint as \# activation-parameters \times 2 bytes assuming fp16 activation parameters. We exclude the memory required for checkpoint activations in our per-node memory footprint estimate. Typically, in large models such as Transformer-1T, the memory footprint required to store the checkpoint activations is significantly larger than the intermediate activations and hence are offloaded to host memory. Therefore, during the training process, we only consider the Activation Working Memory [54], which is the memory required to hold the intermediate activations between two consecutive checkpoints.

As explained in §III-B, the parallelization strategy affects the required memory footprint per node. To illustrate with a concrete use case, Fig. 6 shows how the per-node memory footprint requirement changes for a Transformer-1T model on a fixed cluster size of 1024 nodes, as a function of different stages of ZeRO and a decreasing MP degree (the invariant being $DP \times MP = 1024$). In baseline (i.e., no ZeRO optimizations), the model footprint per node increases exponentially as the MP degree reduces. The same trend holds even with memory optimizations like ZeRO-2: although the growth is slower, the model footprint per node eventually exceeds the typical memory capacity of a single device, highlighting the value of MP to enable in-memory training of huge models. Among all the ZeRO-DP optimizations, ZeRO-3 stands out as it provides the lowest memory footprint per node and remains unaffected by MP reduction. However, ZeRO-3 incurs a $1.5 \times$ communication overhead compared to the baseline. Other approaches such as ZeRO-Offload and ZeRO-Infinity offload data and compute to the host machine resources to reduce the memory capacity pressure on accelerator nodes.

**C. Total Training Time Estimation**

As shown in Figure 5 step (3), COMET plugs into a cost model for training time estimation. We use the ASTRA-SIM simulator [57], [79] for this purpose. ASTRA-SIM is a discrete event-based simulator developed by Meta, Intel and Georgia Tech that can simulate distributed training for a variety of DL workloads. It accepts a workload configuration, topology description and system parameter file to simulate the distributed DL training on a target cluster, and outputs the end-to-end training time breakdown and resource utilization.

At a high level, ASTRA-SIM consists of a workload, system, and network layer. The workload layer is responsible for instantiating a model and scheduling training loops for simulation. The system layer provides the mechanisms for collective primitives and scheduling of communication tasks, similar to collective communication libraries like NCCL [47]. The network layer provides the topology interface via network APIs to support a fast analytical model [79] or detailed network simulation using Garnet [2] and NS3 [62].

An ASTRA-SIM workload configuration file describes the DL workload to be simulated, and consists of the compute...
time, communication collective, and the collective size for each layer of the workload. For each layer, ASTRA-SIM schedules the communication collectives and overlaps the communication delay with compute delay to estimate the total training time. ASTRA-SIM’s analytical network backend—used in our current COMET implementation—estimates the communication delay of an event based on the topology and network bandwidths specified in the configuration files. ASTRA-SIM supports multiple collective communication primitives and scheduling algorithms. The symmetric network topology of distributed training platforms and topology-aware collective communication algorithms minimize the network congestion, enabling the analytical network backend to accurately model the communication overhead [31], [55], [58], [79]. ASTRA-SIM’s runtime projections for 8–16 node clusters has been validated against real systems to be within 5% difference [79].

For COMET, we chose ASTRA-SIM as the cost model for training time estimation given its modular architecture for plug-and-play compute and communication models, and implementations of diverse collective communication algorithms and scheduling strategies. We integrated our workload and data movement models (§ III-C1 and III-C2) in ASTRA-SIM to enable modeling a range of compute units with hybrid memories (LM and EM). Using our added models and the data provided in the workload input file (operations and data size per layer), the compute delay per layer is estimated. ASTRA-SIM uses the compute delay, communication collectives and volume, the network topology, and system parameters provided to perform a training simulation and generates an end-to-end per-layer training-time breakdown for each training phase. It reports the compute and exposed (i.e., non-overlapped) communication times for each layer in the FP, IG, and WG phases.

For our design space exploration of parallelization strategies on a cluster of size \( N \), we sweep the degree of MP and DP such that always \( MP \times DP = N \). This emulates the effective increase in per-node memory capacity as MP decreases in favor of DP, as demonstrated in Fig. 6, and generates the corresponding workload input file for each (MP, DP) combination.

D. Cluster Parameter Reconfiguration

Finally, step 4 provides a set of knobs to perform sensitivity analysis by varying the key component parameters, which include the network topology, compute capability, as well as memory and network bandwidth and latency.

E. Iterative Modeling for Design Space Exploration

By iterating through steps 2 to 4 (§IV-B–§IV-D), we obtain the resulting training time for different system configurations and hardware parameters to identify the best combination of parallelization strategy and cluster resources. The target optimization metric may be raw performance or cost efficiency (i.e., performance relative to cluster’s provisioned resources).

V. CASE STUDIES

We now leverage COMET to evaluate cluster design decisions across multiple dimensions (cluster size and network, per-node memory and compute capability) in the context of large-scale Transformer and DLRM training. We first describe the models and the cluster we model as our baseline system (§V-A). We then evaluate the impact of different cluster configuration parameters using Transformer (§V-B) and DLRM (§V-C) models. §V-D employs COMET to compare a range of different clusters on a range of models. Finally, §V-E concludes with a summarizing overview of COMET’s versatility and quantification of the tool’s key strength of speed, enabling rapid design space explorations for distributed training tasks on large clusters.

A. Baseline Evaluation Setup and Workloads

Fig. 7 visualizes our baseline 1k-node DGX A100 [48] cluster with expanded memories and Table I summarizes the parameters used to model it in ASTRA-SIM. We evaluate training performance for Transformer and DLRM models, which represent the largest models currently deployed. Our evaluation predominantly focuses on the Transformer model due to its higher complexity and broader range of (MP, DP) training strategies (§V-B). Due to space constraints, we present a small subset of DLRM evaluation results in §V-C.

1) Transformer Model: Transformer-based language models are huge natural language processing models used extensively in language modeling, machine translation, text summarization, AI chatbots (e.g., ChatGPT), etc. Latest Transformer models comprise up to trillion parameters and must be trained over hundreds of high-end processing nodes in a distributed manner using multiple levels of parallelization [43], [66], despite advanced techniques employed reduce their required memory footprint [16], [53], [54].

A Transformer model comprises a stack of multiple encoder and decoder structures, each composed of multi-head attention layers followed by fully connected feed-forward and residual layers [73]. Each of the encoder and decoder stack

![Fig. 7: Cluster of 1024 A100 GPUs with expanded memories, grouped in 128 8-GPU pods. Link bandwidth is per direction.](image)

**TABLE I: Baseline NVIDIA DGX A100 system parameters.**

| Single-node Parameters (NVIDIA A100 GPU) |
|-----------------------------------------|
| **Peak Performance (perf_peak)**        | 624 TFLOPS (fp16) |
| **Local Memory Capacity / Bandwidth**   | 80 GB / 2039 GB/s |
| **On-chip SRAM size**                   | 40 MB |

| Cluster Parameters |
|-------------------|
| **Compute Pod**   | NVIDIA A100 DGX (8-GPU) |
| **Cluster Size**  | 1024 nodes (128 pods x 8 GPUs) |
| **Intra-pod Network BW per GPU**        | 300 GB/s / direction (NVLink Gen-3) |
| **Inter-pod Network BW per GPU**        | 31.25 GB/s / direction (InfiniBand) |
| **Physical Topology**                    | Hierarchical Switch |
| **Collectives Implementation**           | Logical Ring |
TABLE II: Transformer model layers and dimensions.

| Layer Type                     | #Stacks | \(N\) | \(K\) | \(d_{model}\) | \(d_{k}\) | \(d_{v}\) | \(d_{ff}\) |
|--------------------------------|---------|-------|-------|--------------|----------|----------|----------|
| Input Embedding                | 1       | \(b \times v\) | \(h \times d_{model}\) | \(d_{model}\) | \(h \times d_{k}\) | \(h \times d_{v}\) | \(d_{ff}\) |
| Layer Norm                     | Element-Wise Multi | N | \(b \times v\) | \(h \times d_{model}\) | \(h \times d_{k}\) | \(h \times d_{v}\) | \(d_{ff}\) |
| Query Projection (Q)           | GEMM    | N | \(b \times v\) | \(h \times d_{model}\) | \(h \times d_{k}\) | \(h \times d_{v}\) | \(d_{ff}\) |
| Key Projection (K)             | GEMM    | N | \(b \times v\) | \(h \times d_{model}\) | \(h \times d_{k}\) | \(h \times d_{v}\) | \(d_{ff}\) |
| Value Projection (V)           | GEMM    | N | \(b \times v\) | \(h \times d_{model}\) | \(h \times d_{k}\) | \(h \times d_{v}\) | \(d_{ff}\) |
| \(U = \text{softmax}(QK^T / \sqrt{d_k})\) | GEMM    | N | \(b \times v\) | \(h \times d_{model}\) | \(h \times d_{k}\) | \(h \times d_{v}\) | \(d_{ff}\) |
| \(Y = UV\)                    | GEMM    | N | \(b \times v\) | \(h \times d_{model}\) | \(h \times d_{k}\) | \(h \times d_{v}\) | \(d_{ff}\) |
| concat(Z = Y \_1, ..., Z_n)   | GEMM    | N | \(b \times v\) | \(h \times d_{model}\) | \(h \times d_{k}\) | \(h \times d_{v}\) | \(d_{ff}\) |
| Residual Addition Element-Wise Add | N | \(b \times v\) | \(h \times d_{model}\) | \(h \times d_{k}\) | \(h \times d_{v}\) | \(d_{ff}\) |
| Layer Norm                     | Element-Wise Multi | 1 | \(b \times v\) | \(h \times d_{model}\) | \(h \times d_{k}\) | \(h \times d_{v}\) | \(d_{ff}\) |
| \(I = G_{softmax}(U X_{a+k})\) | GEMM    | N | \(b \times v\) | \(h \times d_{model}\) | \(h \times d_{k}\) | \(h \times d_{v}\) | \(d_{ff}\) |
| \(Z = I \_1, ..., Z_n\)       | GEMM    | N | \(b \times v\) | \(h \times d_{model}\) | \(h \times d_{k}\) | \(h \times d_{v}\) | \(d_{ff}\) |
| Residual Addition Element-Wise Add | N | \(b \times v\) | \(h \times d_{model}\) | \(h \times d_{k}\) | \(h \times d_{v}\) | \(d_{ff}\) |
| Output Embedding               | Table update | 1 | \(b \times v\) | \(h \times d_{model}\) | \(h \times d_{k}\) | \(h \times d_{v}\) | \(d_{ff}\) |

Legend: \(d_{model}\): hidden dimension, \(b\): batch size, \(v\): sequence length, \(d_{k}\): key/value tensor dimension per attention head, \(d_{ff}\): portion of MLP layer per MP node, \(d_{vocab}\): chunk of total vocabulary per MP node.

takes input and output embeddings as inputs which map a sequence of symbols into a continuous representation. We model the Transformer-IT architecture and hybrid model & data parallelism approach as described in Megatron-LM [66]. Table II breaks down the Transformer-IT model into its layers, and summarizes each layer’s type and dimensions.

2) DLRM: DLRMs are among the largest deep learning models used widely for generating personalized content [11], [20], [45] (e.g., movie recommendations [17], [32], e-commerce catalogs [67], [75], [86]), comprising up to trillions of parameters. DLRM model contains large embedding tables that capture the latent space of user and product feature interaction. In each DLRM, inputs are classified into sparse and dense features which represent the categorical data and continuous features. While sparse features are used to look up the embedding tables, dense features are processed using a bottom stack of MLP layers. The result of embedding lookup and output of bottom MLP layers are combined and given as input to the top MLP layers which finally predict the probability of an event (such as click-rate) occurrence. We model the DLRM architecture and parallelization strategy as described by Rashidi et al. [56].

Unlike Transformer models that can be trained using a wide range of model versus data parallelism configuration points, the training structure for DLRMs is more rigid. DLRM follows a hybrid parallelization strategy where the bottom embedding layers are shared across multiple nodes and performs an all-to-all communication during forward and backward propagation while the MLP layers are replicated on each node in a data parallel fashion and perform an all-reduce during backward propagation. DLRM therefore does not offer the same MP/DP configuration knob we sweep for Transformer models.

B. Transformer Evaluation

A Transformer model can be trained via a wide range of parallelization strategies. We first evaluate the impact of different (MP, DP) parallelization strategies on that cluster’s performance and per-node memory requirements (§V-B1). We then demonstrate the impact of individually scaling the cluster’s per-node memory system (§V-B2), per-node compute capability (§V-B3), and network (§V-B4).

1) Parallelization Strategy Impact on Performance and Memory Requirements: We begin by sweeping (MP, DP) under the invariant \(MP \times DP = 1024\). In this section, training time estimations ignore per-GPU memory capacity constraints, assuming infinite per-node memory capacity accessible at the baseline system’s peak memory bandwidth.

Fig. 8a shows the training time breakdown and corresponding per-node memory footprint for several (MP, DP) configurations, assuming a constant memory bandwidth of 2039GB/s, irrespective of capacity. The total training time is a combination of compute delays and exposed communication delays (cf. §III-C4). The compute and exposed communication time is broken down into three components to indicate the three main phases in a training iteration: forward pass (FP), input gradients (IG), and weight gradients (WG). As MP decreases in favor of more DP groups, the required memory footprint per node increases; therefore, fitting the model in our baseline GPU’s 80GB memory requires an MP degree of 64 or higher.

Memory capacity requirements aside, the best-performing configuration is MP8_DP128, where the exposed communication in FP and IG phases, and the compute delay exhibit their lowest values. Note that WG communication (WG_Exp_Comm) is fully overlapped by the WG compute (WG_Compute) in every configuration, hence not visible. The configurations left of MP8_DP128 (higher MP) are communication bound due to the exposed blocking communication patterns in FP and IG phases across the MP dimension. In contrast, for configurations right of MP8_DP128 (lower MP), the effective model footprint per node grows as the model is distributed across fewer nodes per DPU, and hence becomes more memory bound resulting in higher compute delays dominating runtime, while barely any communication is exposed.

Fig. 8b better highlights the changing balance between compute and exposed communication time for the same (MP, DP) range. Under high MP degrees (e.g., MP64_DP16), training time is dominated by exposed communication time. As MP decreases in favor of increasing DP, the fraction of runtime spent on communication becomes negligible from MP8 onwards. MP8_DP128 is the optimal configuration because it strikes the best balance, effectively overlapping communication delays with compute, without getting into a memory-bandwidth-bound region that causes drastic compute time increase.

2) Effect of Memory System Design: Based on §V-B1’s results, the best-performing MP8_DP128 configuration requires ~250GB of memory to fit the model, exceeding the 80GB the NVIDIA A100 GPU baseline’s per-node memory capacity by \(3\times\). The best-performing configuration achievable under the 80GB memory constraint is MP64_DP16. The required capacity for MP8_DP128 could be achieved with a hybrid memory system, complementing the GPU’s HBM with a secondary DRAM-based memory that offers additional capacity, albeit accessible at lower bandwidth. As mentioned in §III-C2, such additional capacity could be provided by allowing the GPU to access its host CPU’s memory, or by attaching additional memory to the GPU over CXL [12] or other technology.

Fig. 9 shows the performance results normalized to MP64_DP16, the best-performing configuration of in-memory distributed training that is feasible without memory expansion.
(a) Breakdown of comp./comm. time & per-node memory footprint.

Fig. 8: Training runtime of Transformer-1T with varying MP/DP degree (norm. to best-performing MP8 DP128 config.).

(b) Exposed communication to compute ratio.

Fig. 9: Effect of memory bandwidth availability to the expanded memory system. The check-mark indicates the baseline configuration to which all the other values are normalized.

(cf. Fig. 8a). The heatmap’s x-axis shows the bandwidth to expanded memory, while the varying (MP, DP) degree on the y-axis is a proxy for the required capacity of that expanded memory (see memory requirements in Fig. 8a). MP64 DP16 and configurations with higher MP remain unaffected by the expanded memory’s bandwidth, as the dataset entirely fits in each node’s local memory, and configurations with MP higher than 256 are omitted, as they perform strictly worse.

The heatmap guides system architects in determining what memory expansion technology can be used to boost a cluster’s training performance, revealing the range of expanded memory characteristics that allow building a cluster with lower training time than the MP64 DP16 baseline. Conversely, the data can also be leveraged to derive the equally valuable information of memory technologies that would not be applicable.

We provide two illustrative examples derived from Fig. 9:

Ex. 1: The theoretically optimal MP8 DP128 configuration is achievable with a hybrid memory system offering at least $4.25 \times$ higher aggregate capacity than the baseline (cf. Fig. 8a), and outperforms the baseline if the expanded memory is accessible at a bandwidth of at least 500GB/s.

Ex. 2: A system architect considering CXL-attached memory can quickly deduce that, in order to benefit the given workload, the technology must be capable of delivering 500GB/s to 340GB of memory, at a minimum. In practice, that would require a memory device accessible over 32 lanes of CXL 3.0.

3) Effect of Per-node Compute Capability: The tremendous demand for DL training drives rapid evolution of the hardware used in clusters deployed for such purpose. COMET can be used to study the effect of per-node compute capability by scaling each node’s peak performance ($p_{max}$) to model hardware of different generations.

Fig. 10 shows the effect of per-node compute scaling on the MP8 DP128 configuration, assuming a memory system of varying $bw_{EM}$ as a function of $bw_{EM}$, and sufficient capacity to hold the model. At the highest $bw_{EM}$ of 2TB/s, halving compute capability—e.g., by replacing the baseline A100 with a lower-end GPU—increases the runtime by 50%, while doubling it reduces the runtime by 25%. Scaling compute further has diminishing returns, as training becomes communication bound. For lower memory bandwidth availability, the impact of compute capability scaling further diminishes due to the additional bottleneck of memory bandwidth. System designers can employ such studies to predict the impact of a next-generation GPU on a cluster’s overall performance.

4) Effect of Networking Capability: A cluster’s network bandwidth plays a critical role in the overall training time. Especially at higher MP configurations, training time is dominated by the exposed blocking communication patterns in forward and input gradient phases. In our modeled cluster, there is an intra-pod bandwidth to communicate with GPUs within a pod and a lower inter-pod bandwidth for communication across pods (see Table I). We use a Hierarchical Collective implementation [10], [58] in our evaluations, which first reduces data across GPUs of the same pod, followed by inter-pod

Fig. 10: Effect of node compute capability relative to baseline A100 GPU (MP8 DP128 configuration).
DP16 is majorly affected by network DP128 training is feasible, the network’s DP16. In each plot, we vary the two DP128 configuration, where the MP dimension is DP16 with an aggregate full duplex bandwidth of 331.25 GB/s which feature high intra-pod bandwidth. Halving intra-/inter-pod bandwidth (i.e., 284 GB/s intra-pod and 47.32 GB/s inter-pod). For lower/higher ratios, inter-/intra-pod network bandwidth becomes a bottleneck, respectively. In the case of compute-bound MP8 DP128, the MP dimension is

Fig. 11: Effect of network capabilities on cluster-scale performance. The check-mark indicates the baseline configuration to which all the other values are normalized. 300/31.25 GB/s is currently a typical NVLink/InfiniBand configuration.

reduction. Such local network bandwidth-aware collective optimization reduces the communication volume on the lower-bandwidth inter-pod links.

Fig. 11 shows the effect of both intra- and inter-pod network bandwidth scaling on training time for two different (MP, DP) configurations: the communication-bound MP64_DP16 and the compute-bound MP8_DP128. In each plot, we vary the two network bandwidths while keeping the compute and memory bandwidth constant to the baseline system’s values (Table I).

Unsurprisingly, MP64_DP16 is majorly affected by network bandwidth, as the MP dimension straddles several 8-node pods, which feature high intra-pod bandwidth. Halving intra-/inter-pod bandwidth results in a 48%/22% slowdown, respectively. On the contrary, doubling intra-/inter-pod bandwidth reduces runtime by 3%/18%, respectively, while doubling both reduces runtime by 27%. Evidently, the most effective network scaling scales bandwidth on both dimensions, while scaling only one dimension’s bandwidth provides reduced or marginal gains.

This effect is attributed to the mapping of the workload on the underlying cluster. The performance-critical all-reduce communication in forward and backward propagation is bottlenecked by both intra- and inter-pod links. Thus, increasing only one dimension’s capability yields limited gains (as the other dimension remains a bottleneck), while boosting the capabilities of both dimensions has an amplificatory effect. In contrast, when MP8_DP128 training is feasible, the network’s role is much less critical. Reducing both intra- and inter-pod bandwidth to 50% only degrades performance by 11%, while even increasing both by 4\times only boosts performance by 5%.

We conduct an additional experiment to focus on identifying the ideal balance of the bandwidth available at the two dimensions. Instead of varying the two values independently, as previously done in Fig. 11, Fig. 12 shows the performance trends when the available network bandwidth is re-distributed between intra-/inter-pod links, while its aggregate value always remains fixed. For the baseline MP64_DP16 configuration with an aggregate full duplex bandwidth of 331.25 GB/s per direction (300 GB/s intra-pod and 31.25GB/s inter-pod), we find an optimal bandwidth ratio of 1:6 between inter-/intra-pod network bandwidth (i.e., 284 GB/s intra-pod and 47.32 GB/s inter-pod). For lower/higher ratios, inter-/intra-pod network traffic becomes a bottleneck, respectively. In the case of compute-bound MP8_DP128, where the MP dimension is entirely contained within a pod, the performance-critical MP communication is entirely dictated by intra-pod bandwidth while the DP communication across the pods is affected by the inter-pod link bandwidth. Therefore, MP communication is not a bottleneck and performance is largely insensitive to the rebalanced bandwidth ratio. Performance starts dropping beyond 1:5 (i.e., with intra-pod bandwidth less than 276GB/s), as MP communication starts reappearing as a bottleneck. Overall, 1:6 inter-/intra-pod network bandwidth provisioning appears to be the ratio that best accommodates both training configurations, improving training time by up to 15% compared to the default 1:9.6 ratio.

System designers can use such analysis to determine the topology and interconnect technology to use (e.g., Ethernet, InfiniBand, NVLink), while balancing the resulting performance with the associated cost of the selected hardware resources.

C. DLRM Evaluation

We now briefly cover evaluation highlights for the training of a 1.2 trillion parameter DLRM, modeled as described in Table V of Rashidi et al. [56]. Fig. 13a shows the training
time breakdown for single DLRM instance and corresponding per-node memory footprint for different cluster sizes. Since the DLRM’s memory footprint is relatively smaller than §V-B’s Transformer-1T model, we start with a smaller cluster comprising only 8 pods of our baseline DGX cluster (64 GPUs in total). As the cluster’s size decreases, the exposed communication delay decreases at the cost of increased memory footprint per node required, resulting in a compute delay increase. However, the overall increase in training time is sublinear with the node count reduction, especially in the 64–16 range. Thus, memory expansion can not only be used to improve DLRM training efficiency, but also better performance for a training workload comprising several DLRM models. This is a common use case, as large corporations often need to train multiple DLRMs for different purposes [1], [42].

Fig. 13b evaluates the overall turnaround time of training 8 DLRMs on 64 GPU nodes as a function of available bandwidth to the expanded memory. While DLRM’s performance is more sensitive to memory bandwidth, results qualitatively match §V-B2’s takeaways. Performance improvement opportunities require memory expansion solutions delivering at least 75% additional memory capacity at 800GB/s; a 200GB expanded memory accessible at 1.5TB/s improves training time by 1.5×.

D. Comparative DL Training on Different Clusters

We conclude COMET’s utility demonstration by comparing 11 different DL training clusters, summarized in Table III: nine GPU-based clusters, a Google TPU v4, and a Tesla Dojo cluster. The general structure of the three cluster types is depicted in Fig. 14. Our goal is not to declare the “best” system—as they drastically differ in cost, node count, definition of a “node”, etc.—but to demonstrate the different behavior across three very dissimilar clusters when training the same huge model.

a) DGX cluster variants: We model three base 1024-GPU cluster variants—A, B, and C—with different resource (compute, memory, network) provisioning. We base each design on a major GPU model (V100, A100 and H100). All GPU cluster variants are organized in 16-GPU pods and feature a two-dimensional network like the one shown in Fig. 7. For each base cluster variant, we evaluate three memory systems—0, 1 and 2—with different characteristics, for a total of nine GPU cluster variants. Memory system 0 consists of only local GPU memory without any capacity expansion. Memory systems 1

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TABLE III: Per-node details of various cluster configurations.

| config | compute node | local bw (GB/s) | exp. bw (GB/s) | network (topology : bandwidth per node) |
|--------|--------------|----------------|---------------|-----------------------------------------|
|        | Peak TOPS   | local cap. (GB) | exp. cap. (GB) | two-level switch :                      |
| A0     | V100        | 125            | 80            | 0                                       |
| A1     |             | 900            | 150 GB/s intra-pod, 6.25 GB/s inter-pod |
| A2     |             | 201            | 1000          |
| B0     | A100        | 625            | 80            | 0                                       |
| B1     |             | 2039           | 300 GB/s intra-pod, 31.25 GB/s inter-pod |
| B2     |             | 201            | 1000          |
| C0     | H100        | 1979           | 80            | 0                                       |
| C1     |             | 3350           | 450 GB/s intra-pod, 62.5 GB/s inter-pod |
| C2     |             | 201            | 1000          |
| Dojo   | Tray        | 54,300         | 640           | 0                                       |
| TPU v4 | TPU         | 275            | 32            | 0                                       |
|        |             | 12000          | 1200          |
|        |             | 39             | 1200          |
|        |             | 3D torus : 6 × 48GB/s per direction |

*Although the V100 GPU features 32GB of memory, we model 80GB instead to keep the memory system configuration options of clusters A, B, and C aligned.
and 2 are hypothetical expanded memory systems accessible at 0.5TB/s and 1TB/s, respectively.

b) TPU v4 cluster: We model a TPU cluster of 4096 TPU-V4 chips connected in a 3D Torus topology with 48GB/s full duplex links. Each TPU features 32MB of on-chip SRAM, a 32GB HBM with a memory bandwidth of 1.2TB/s, and 275 TFLOPS peak performance [71].

c) Dojo cluster: We model a Dojo cluster of 64 nodes (“trays”), each comprising several training tiles and interface processors. Each node has 66GB of on-chip SRAM, 640GB of memory with a 16 TB/s bandwidth, and 54.3 PFLOPS peak performance. Given limited publicly available information, we model the network topology as a single logical switch delivering 1 TB/s of full duplex network bandwidth to each node [34].

Fig. 15 shows the speedup for DLRM and Transformer-1T across different cluster configurations. Every cluster except A0, B0, C0, and Dojo assumes per-node memory expansion with capacity and bandwidth characteristics listed in Table III. DLRM training is modeled as described in §V-C: Clusters A0, B0, and C0 use 64 nodes to run a single DLRM instance. A1, B1, and C1 leverage their expanded memory to train one DLRM per 16 nodes. Likewise, A2, B2, and C2 use 8 nodes per instance. The reported speedup for DLRM refers to training a total of 8 model instances. For Transformer-1T, speedup refers to training a single instance on the entire cluster. All reported speedups are normalized to cluster A0 as baseline.

Clusters A2, B2, and C2 benefit from their expanded memory at 1TB/s, delivering 1.8×, 2.6×, and 2.7× speedups, respectively, for DLRM. While clusters A1, B1, and C1 fare poorly for DLRM due to their lower bandwidth to expanded memory, B1 and C1 deliver a good speedup of 7.2× and 12.5×, respectively, for DLRM. Increasing expanded memory bandwidth to 1TB/s further improves speedup for Transformer-1T (e.g., to 14.3× for C2).

Cluster A2’s double bandwidth to expanded memory improves cluster A1’s DLRM performance by 1.64×. Due to the memory-bound nature of DLRM, memory bandwidth improvements are more critical than compute capacity or network bandwidth. On the other hand, Transformer-1T is more sensitive to the compute capacity and network bandwidth, and therefore low compute and network bandwidth drastically reduces speedup opportunities for clusters A1 and A2. Transformer-1T benefits from TPU’s large compute capacity and network bandwidth, but the DLRM suffers from its low memory capacity and local memory bandwidth. In contrast, Dojo significantly benefits both workloads due to large on-chip SRAM, memory capacity, and high network bandwidth.

Overall, among GPU cluster variants, there is no single optimal configuration for both Transformer-1T and DLRM, as different workloads are impacted differently. Disregarding any cost considerations, the best GPU cluster on average is C0, delivering a 7.7× speedup over the baseline A0 cluster. Memory expansion is an effective technique for all clusters when training Transformers, but only for the lowest-end cluster A on average, due to DLRM’s memory bandwidth sensitivity. This study demonstrates that, as one size does not fit all, system architects should evaluate a workload mix representative of the main use cases for the target cluster to determine the system configuration that best fits the ensemble.

E. COMET takeaways: versatility and speed

The extensive evaluation in § V-B and V-C demonstrates COMET’s versatility and the breadth of case studies it facilitates. We illustrated that COMET enables joint sensitivity analysis of the effect of node compute capability, memory system design, and network provisioning on cluster performance, facilitating balanced resource provisioning and identification of cost-reduction opportunities. COMET also allows rapid exploration and evaluation of memory system design on a cluster’s performance as a function of its capacity and bandwidth characteristics, helping system designers determine what existing technologies for memory expansion are viable to improve training performance, and gauge the impact of relevant future technologies.

While §V’s evaluation focused on demonstrating the utility and flexibility of the tool, an additional key strength of COMET is the short turnaround time of experiments, allowing researchers to rapidly glean performance trends. Once a target model is broken down into its layer-wise representation as specified in §III-A, exploring a broad design space is a matter of few hours. COMET’s methodology allows modeling different compute nodes, network topologies, memory bandwidths and parallelization strategies in an embarrassingly parallel fashion on commodity processors. To provide some concrete data points, generating the two memory bandwidth sensitivity heatmaps (Fig. 9 for Transformer-1T and Fig. 13b for DLRM) takes about 5 hours / 45 minutes, respectively, on a single 24-core Intel Xeon Silver server. Other analyses presented in the paper require comparable runtimes. Such rapid exploration
of a wide range of design choices is a valuable capability COMET contributes.

VI. CONCLUSION

We introduced COMET, a holistic, end-to-end methodology and workflow for rapid design space exploration of key parameters affecting the performance and efficiency of large-scale distributed DL training: the model’s parallelization strategy and provisioning of each of the cluster’s key resources. We demonstrated COMET’s utility with case studies on DLRM and Transformer models, deriving actionable cluster design hints for system designers, and identifying required bandwidth and capacity characteristics for emerging memory expansion techniques to have a positive impact on cluster performance on distributed DL training. COMET enables the evaluation of a wide spectrum of key cluster design parameters in a matter of few hours using very modest physical hardware resources.

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REFERENCES

[1] B. Acun, M. Murphy, X. Wang, J. Nie, C.-J. Wu, and K. Hazelwood, “Understanding training efficiency of deep learning recommendation models at scale,” in 2021 IEEE International Symposium on High-Performance Computer Architecture (HPCA), 2021, pp. 802–814.
[2] N. Agarwal, T. Krishna, L.-S. Peh, and N. K. Jha, “Garnet: A detailed on-chip network model inside a full-system simulator,” in Performance Analysis of Systems and Software, 2009. SPASIS 2009. IEEE International Symposium on, IEEE, 2009, pp. 33–42.
[3] D. Amodei, S. Ananthanarayan, R. Anubhai, J. Bai, E. Battenberg, C. Case, J. Casper, B. Catanaro, Q. Cheng, G. Chen, J. Chen, J. Chen, Z. Chen, M. Chrzanski, A. Coates, G. Diamos, K. Ding, N. Du, E. Elsen, J. Engel, W. Fang, L. Fan, C. Fougner, L. Gao, C. Gong, A. Hannun, T. Han, L. Johannes, B. Jiang, C. Ju, B. Jun, P. LeGresley, L. Lin, J. Liu, Y. Liu, W. Li, X. Li, D. Ma, S. Narang, A. Ng, S. Oriair, Y. Peng, R. Prenger, S. Qian, Z. Quan, J. Rainman, V. Rao, S. Satheesh, D. Sceattapun, S. Sengupta, K. Srinet, A. Sriram, H. Tang, L. Tang, C. Wang, J. Wang, K. Wang, Y. Wang, Z. Wang, Z. Wang, S. Wu, L. Wei, B. Xiao, W. Xie, X. Xie, D. Yogatama, B. Yuan, J. Zhan, and Z. Zhu, “Deep speech 2 : End-to-end speech recognition in english and mandarin,” in Proceedings of The 33rd International Conference on Machine Learning, ser. Proceedings of Machine Learning Research, vol. 48, New York, New York, USA, 20–22 Jun 2016, pp. 173–182. [Online]. Available: https://proceedings.mlr.press/v48/amodei16.html
[4] P. Belevich, Y. Zhao, S. Li, J. Choi, R. Varma, P. Damania, G. Chauhan, M. Yadav, P.-Y. Aquilanti, and S. Ranganatha, “Training a 1 Trillion Parameter Model With PyTorch Fully Sharded Data Parallel on AWS,” https://medium.com/pytorch/training-a-1-trillion-parameter-model-with-pytorch-fully-sharded-data-parallel-on-aws-3ae31aa96c6f, 2022. [Online; accessed 28-22 June2022].
[5] A. Castelló, M. Catalán, M. F. Dolz, J. I. Mestre, E. S. Quintana-Ortí, and J. Duato, “Performance modeling for distributed training of convolutional neural networks,” in 2021 29th Euromicro International Conference on Parallel, Distributed and Network-Based Processing (PDP), 2021, pp. 99–108.
Proceedings of the 28th International Conference on Architectural Support for Programming Languages and Operating Systems, 2023.

[41] T. Miao, Q. Wu, T. Liu, P. Cui, R. Ren, Z. Li, and G. Xie, “Md-roofline: A training performance analysis model for distributed deep learning,” in 2022 IEEE Symposium on Computers and Communications (ISCC), 2022, pp. 1–8.

[42] D. Mudigere, Y. Hao, J. Huang, Z. Jia, A. Tulloch, S. Sridharan, X. Liu, M. Ozdal, J. Nie, J. Park, L. Luo, J. A. Yang, L. Gao, D. Ivchenko, A. Basant, Y. Hu, J. Yang, E. K. Ardeastani, X. Wang, R. Komuravelli, C.-H. Chu, S. Yilmaz, H. Li, J. Qian, Z. Feng, Y. Ma, J. Yang, E. Wen, H. Li, L. Yang, C. Sun, W. Zhao, D. Melts, K. Dhulipala, K. Kishore, T. Graf, A. Eisenman, K. K. Matam, A. Gangidi, G. J. Chen, M. Krishnan, A. Nayak, K. Nair, B. Muthiah, M. khorasani, P. Bhattacharya, P. Lapukhov, M. Naumov, A. Mathews, L. Qiao, M. Smelyanskiy, B. Jia, and V. Rao, “Software-hardware co-design for fast and scalable training of deep learning recommendation models,” in Proceedings of the 49th Annual International Symposium on Computer Architecture, ser. ISCA ’22, New York, NY, USA, 2022, p. 993–1011. [Online]. Available: https://doi.org/10.1145/3470496.3535372

[43] D. Narayanan, M. Shoeybi, J. Casper, P. LeGresley, M. Patwary, V. Korthikanti, D. Vainbrand, P. Khashikin, J. Bernauer, B. Catanzaro et al., “Efficient large-scale language model training on gpu clusters using megatron-lm,” in Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis, 2021, pp. 1–15.

[44] D. Narayanan, M. Shoeybi, J. Casper, P. LeGresley, M. Patwary, V. Korthikanti, D. Vainbrand, P. Khashikin, J. Bernauer, B. Catanzaro, A. Parashar, P. Raina, Y.-H. Chen, V. A. Ying, A. Mukkara, M. Ott, S. Shleifer, M. Xu, P. Goyal, Q. Duval, and V. Caggiano, “Efficient large-scale language model training on GPU clusters using megatron-lm,” in International Conference for High Performance Computing, Networking, Storage and Analysis (SC), B. R. de Supinski, M. W. Hall, and T. Gamblin, Eds.

[45] M. Naumov, J. Kim, D. Mudigere, S. Sridharan, X. Wang, W. Zhao, S. Yilmaz, C. Kim, H. Yuen, M. Ozdal, K. Nair, I. Gao, B. Su, J. Yang, and M. Smelyanskiy, “Deep learning training in facebook data centers: Design of scale-up and scale-out systems,” CoRR, vol. abs/2003.09518, 2020. [Online]. Available: https://arxiv.org/abs/2003.09518

[46] M. Naumov, D. Mudigere, H. M. Shi, J. Huang, N. Sundaraman, J. Park, X. Wang, U. Gupta, C. Wu, A. G. Azzolini, D. Dzhulgakov, A. Mallevich, I. Cherniavskiy, Y. Li, R. Krishnamoorthi, A. Yu, V. Kondratenko, S. Pereira, X. Chen, W. Chen, V. Rao, B. Jia, L. Xiong, and M. Smelyanskiy, “Deep learning recommendation model for personalization and recommendation systems,” CoRR, vol. abs/1906.00091, 2019. [Online]. Available: http://arxiv.org/abs/1906.00091

[47] NVIDIA, “NVIDIA Collective Communication Library (NCCL),” https://docs.nvidia.com/en-us/nccl/

[48] NVIDIA, “Nvidia dgx a100,” Cloud & Data Center DGX A100, Aug 2022, https://images.nvidia.com/aem-dam/Solutions/Data-Center/nvidia-dgx-a100-80gb-datasheet.pdf.

[49] G. Ofenbeck, R. Steinmann, V. Caparros, D. G. Spampinato, and M. Puschel, “Applying the roofline model,” in 2014 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2014, pp. 76–85.

[50] M. Ott, S. Shleifer, M. Xu, P. Goyal, Q. Duval, and V. Caggiano, “Fully Sharded Data Parallel: faster AI training with fewer GPUs,” https://engineering.fb.com/2021/07/15/open-source/fdp/, 2021, accessed 28-June-2022.

[51] A. Parashar, P. Raina, Y. S. Shao, Y.-H. Chen, V. A. Ying, A. Mukkara, R. Venkatason, B. Khailany, S. W. Kreckler, and J. Eisen, “Timeloop: A systematic approach to dnn accelerator evaluation,” in 2019 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2019, pp. 304–315.

[52] E. Qin, A. Samajdar, H. Kwon, V. Nadella, S. Srinivasan, D. Das, B. Kaul, and T. Krishna, “Sigma: A sparse and irregular gemm accelerator with reconfigurable interconnects,” in Proceedings of the 28th International Conference on Architectural Support for Programming Languages and Operating Systems, 2023.

[53] S. Li, Y. Zhao, R. Varma, O. Salpekar, P. Noordhuis, T. Li, A. Paszke, J. Smith, B. Vaughan, P. Damanica, and S. Chintala, “Pytorch distributed: Experiences on accelerating data parallel training,” CoRR, vol. abs/2006.15704, 2020. [Online]. Available: https://arxiv.org/abs/2006.15704

[54] J. Lin, A. Yang, J. Bai, C. Zhou, L. Jiang, X. Jia, A. Wang, J. Zhang, Y. Li, W. Lin, J. Zhou, and H. Yang, “Ms-05t: A sharing-delinking paradigm for efficient multi-trillion parameter pretraining,” CoRR, vol. abs/2101.03888, 2021. [Online]. Available: https://arxiv.org/abs/2101.03888

[55] G. Lu, R. Chen, Y. Wang, Y. Zhou, R. Zhang, Z. Hu, Y. Miao, Z. Cai, L. Li, J. Leng, and M. Guo, “Distsim: A performance model of large-scale hybrid distributed dnn training,” 2023.

[56] H. A. Maruf, H. Wang, A. Dhanotia, J. Weiner, N. Agarwal, P. Bhatcharya, C. Petersen, M. Chowdhury, S. Kanaujia, and P. Chauhan, “Tpp: Transparent page placement for cxl-enabled tiered memory,” in
