I. INTRODUCTION

NOWADAYS most of the detectors used in positron emission tomography (PET) applications are based on pixelated detectors. Usually a high number of individual scintillator crystals are either coupled individually to a light sensor or sharing a fewer number of them. In both cases the spatial resolution is limited by the pixel size. The high degree of segmentation in those detectors strongly simplifies the task of locating gamma ray interaction although on the other hand small pixel size degrades energy resolution and time performance. Moreover the scalability of pixel based architecture requires a high cost in terms of material and manufacturing. Other solutions have been proposed in the past [1] based on bigger scintillation crystals where the light distribution sensed by an array of photodetectors was analyzed in order to obtain the gamma event characteristics. However the size and shape of the scintillator crystal cannot be fully customized and large area detectors (body PET scanners) are still difficult to build.

II. PETALO DETECTOR CONCEPT

PETALO (Positron Emission TOF Apparatus based on Liquid xenOn) detector makes use of liquid Xenon (LXe) as scintillation medium which not only offers interesting properties such as high scintillation yield (∼30k photons per 511 keV gamma) and fast time performance [2] but also allows to build custom size detectors suitable for large volume applications. Since LXe requires a cryogenic environment (cryostat) some parts of the detector must be compatible with low temperature operation. However most of the sensitive electronics can be placed in the vacuum space of the cryostat device thus avoiding the effects of cryogenic temperatures (see fig.1).

PETALO detector aims at capturing the light produced by the scintillation in LXe taking advantage of its uniform response and continuity. This strategy will lead to a geometrical distortion free behavior compared to other PET detectors.

In order to achieve the best characteristics, densely packed arrays of VUV sensitive SiPMS will be employed to meet LXe scintillation light wavelength requirements. The enhanced light collection capabilities of such structure will increase resolution performance of previous LXe based detectors [3]. Moreover the low temperatures inside the cryostat will make dark count rate effects neglectable. PETIT prototype, the first version of the PETALO detector, which is being built at the moment will be composed of a 17 cm height and 36 cm diameter ring with a fully instrumented outer face (fig.2). In later versions the height of the ring will be extended in order to further reduce border effects in the field of view (FOV).

In order to take advantage of the unique PETALO detector characteristics a read-out architecture must be designed to meet the following specifications: Electronics associated to detector (front-end and read-out itself) must be fully expandable in terms of detector size. Read-out scheme must be compatible with the non-segmented structure of the detector. Time of Flight (TOF) capabilities must be assured at the scanner level, that is to say front-end and read-out electronics should not degrade LXe time performance [2].
A. Brain PET case study

Continuous systems show a high spatial pileup probability as well as a much higher amount of information generated for an equivalent activity in the FOV. Light distribution for every gamma detected must be acquired and sent for further processing and coincidence analysis. PETALO design allows to extract more information from every event and eventually will implement Compton reconstruction algorithms in order to enhance overall detector sensitivity. However continuous medium detectors are more prone to pile up effects since more individual sensors get involved in every event. A typical brain PET application can be used as an example to show a worst case pileup probability as well as the total amount of information generated by the system. For the usual dose of FDG in such a PET scanner assuming the dimensions of PETIT prototype the pile up probability is shown in table I. On the other hand an approximate computation of the information generated is presented in table II for different implementation options. Although estimations show the feasibility of PETALO concept, the total data flow required through the readout system is high enough to require a new design approach in order to optimize the data link speeds as well as introduce data reduction or compression techniques in its first stages.

III. PETALO READ-OUT PROPOSAL

A front-end and read-out architecture has been proposed (fig. 3) to meet the stated requirements. Front-end section (FE) is based on TOFPET2 asics [4] which offer a good solution for early digitization of sensor outputs and timestamp generation with a CRT resolution close to that of the LXe. Each TOFPET2 is able to handle 64 SiPMs generating timestamps and integrated charge data for every channel individually. A certain number of TOFPETs are controlled by a first level (L1) readout board that manages their configuration and receives their output data. L1 main function is to reduce the amount of information generated by FE and send it to upper levels of the readout architecture. A second level (L2) readout board will finally group all the channel data with same timestamp and look for gamma event coincidences in order to build true detected events. In an initial stage of development L2 functionality can be carried out by a dedicated computer able to handle the resulting data bandwidth.

The output data flow from the detector shows statistical variations due to two dominant effects. The most important is the Poisson fluctuation in the event rate but also the analog to digital conversion (ADC) done at the FE level has a variable latency due to the usage Wilkinson ADC converters. In order to attenuate the data flow fluctuations a set of FIFO based memory buffers must be introduced between the different stages of the readout. The depth of these FIFOs along with the data link speeds in every point of the readout scheme are fundamental parameters for the design process. A data flow simulation test bench has been developed to get a realistic approximation for these values. The physics data generation is based on a GEANT simulation which uses the same event rate as the one obtained in the brain PET study. The detector architecture chosen for this simulation is a fully SiPM instrumented PETALO prototype with the same geometry specifications as the one used in the previous pile up study. A total number of 7680 SiPMs covering the inner face of the cylindrical volume of the detector are controlled by 120 TOFPET2 asics and 12 L1 (10 asics per L1) in this configuration. Behavioral data flow models with latency and timing specifications have been developed for all the elements and whole parametrized readout architecture has been simulated under different conditions using Python based SIMPY package [5] to get the required information.

Another key element of the PETALO readout concept is the synchronization scheme required to generate coherent timestamps at the FE level. Every TOFPET asic in the system needs to be synchronized within a 50 ps margin in order not to degrade the timing resolution of captured events. Synchronization links are deployed between L1 and L2 boards according to the same principles described in [6], that allow propagation of a common clock frequency and automatic correction of timestamps.

IV. READ-OUT SYSTEM DESIGN AND SIMULATION

In this section a description of the functionality and simulation results of every component in the readout architecture

| TABLE I | BRAIN PET ACTIVITY AND PILE-UP |
|---------|-------------------------------|
| TOTAL FDG dose | 240 [MBq] (peak) |
| Brain activity | 36 [MBq] (peak) |
| Detected Activity (100% efficiency) | 30.7E6 [γ/s] (peak) |
| Pile-up probability | 10.4 % |

| TABLE II | BRAIN PET INFORMATION GENERATION. (63 % DETECTION EFFICIENCY) |
|----------|---------------------------------------------------------------|
| Bits per channel | 46 |
| Bits per event | 1472 |
| Raw data rate (average) | 25.1 Gbit/s |
| Data rate for coincidence filtering integrated in readout | 5 Gbit/s |
| Data rate for coincidence and energy filtering integrated in readout | 0.7 Gbit/s |

Fig. 3. Read-out scheme.
will be presented. The simulation results are based in the brain PET study case shown in the previous section.

A. Front end modelization

A behavioral model for TOFPET asic has been developed based in its internal structure. Each input channel has a 4 depth analog FIFO, a Wilkinson ADC converter with a maximum latency of 5 microseconds and a time to digital converter (TDC) for timestamp generation. The output digital link of the device has been modeled with a speed of 32 Mevents/s which is lower than the maximum provided by the manufacturer specifications. Results for input analog FIFOs and maximum data latency in the FE stage are shown in figure 4 for a 50K events simulation.

B. L1 board modelization

First level readout boards (L1) must collect the information of FE stage and compose the pieces of the light distribution associated to each gamma event detected. Since each channel generates data with different arrival times to the L1 input, each L1 board must store a batch of data in a buffer that will have to be scanned continuously to build data frames with the same timestamp value. Once an event piece has been built, this information can be erased from the buffer so that new FE data can be stored. L1 input buffer has been sized through simulation to behave as a time window where all the information related to the same event is stored and no output information from FE is lost due to buffer overload. From the results in fig. 5 regarding maximum data frame length (integrated charge related data from the FE with the same timestamp) and maximum number of event pieces in the L1, the buffer size required is smaller than 50 kbits.

C. Data Compression

L1 output data link must operate at a speed of 2.2 Gbits/s for the required simulation conditions and its output FIFO must store a maximum of 60 data frames (54 kbits) (fig. 6). Although this size is affordable for any FPGA device, the output data link speed is quite high. Moreover the amount of data generated for 12 L1 would reach 25 Gbits/s for the storage system at the end of the readout. This link speed could be optimized if a compressor element is introduced in L1.

As explained in previous section, each data frame generated at the output of L1 has a single timestamp and belongs to the same event. Since that data frame composes a piece of the same gamma event, any image based compression techniques could be applied to reduce data at the output of L1. A single stage Haar-1 wavelet filter has been evaluated. This type of compressor extracts low spatial frequency and high spatial frequency components of the original image and uses a lower number of bits to quantize the later ones (10 bits / 4 bits) thus reducing the whole amount of data with a minimum loss in image quality. Simulations have been carried out to quantify the effect on spatial resolution of the detected events (fig. 7).
Fig. 6. L1 FIFO size simulation.

Fig. 7. Resolution loss due to compressor.

Fig. 8. Compressor effect on data frame length

V. CONCLUSIONS

A new readout concept has been introduced which is compatible with a fully continuous medium detector such as PETALO. The possible drawbacks associated with the amount of data generated as well as the required data link speeds along the system have been analyzed using a custom developed simulation test bench. Results show that the system is feasible however a fast compression technique has been also introduced in L1 to further reduce the data bandwidth requirements.

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and the results show a degradation in Z and PHI coordinates lower than 0.2 mm (FWHM).

The compression rate achieved with this simple filter is around 55%. However its performance profile (fig. 8) shows a higher compression factor for events which involve a higher number of SiPM channels, that is to say those that generate longer data frames and require more time to be transmitted. This fact has a strong impact on data link speed that can be reduced down to 480 Mbits/s for every L1 without data loss.