Analysis of energy consumption bounds in CMOS current-steering digital-to-analog converters

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Abstract
In this paper, an attempt to estimate energy consumption bounds versus signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) in CMOS current-steering digital-to-analog converters is presented. A theoretical analysis is derived, including the design corners for noise, speed and linearity for the mixed-signal domain. The study is validated by comparing the theoretical results with published measured data. As result it serves as a design reference to aim for minimum energy consumption. It is found that for an equivalent number of bits (ENOBs), the noise-bound grows at a rate of $2^{2\text{ENOB}}$, whereas the speed-bound increases by $2^{\text{ENOB}-2}$ and is dependent on device dimensions. Therefore, as the technology scales down, the noise bound will dominate, which is observed for an estimated SNR of about 40 dB in 65 nm CMOS process. The linearity bound is derived from an analysis based on the assumption of limited output impedance, where it is found to be dependent on the device dimensions and increase at a rate of $2^{\text{ENOB}-1}$. The observations show that it is possible to achieve less energy consumption in all the design corners for different SNR and SFDR specifications within the Nyquist frequency, $f_s/2$.

Keywords Digital-to-analog converter · CMOS · Current-steering · High-speed · Energy/Power consumption bounds

1 Introduction
Digital-to-analog converters (DACs) are essential building blocks in many applications, e.g., telecommunications, video systems, etc., as digital signals must be represented by an analog signal for further signal processing in the analog/RF domain. The introduction of wireless communication standards, such as 2G/3G/4G, has challenged DAC design to operate at higher sampling speeds and wider bandwidths yet with improved linearity and reduced power consumption. The continuous down-scaling of CMOS technologies with their reduced device dimensions and higher transit frequencies has enabled the design of DACs operating at lower power consumption and higher sampling speeds.

High-speed CMOS DACs operating with low power consumption have gained increasing attention due to the importance of prolonging battery life in portable devices as well as reducing overall power consumption in the wireless communication systems[1–3]. The ever-growing demand for wider bandwidths has pushed sampling frequencies into the multi-GHz domain at the cost of increased power consumption. Elaborate methods to improve DAC linearity to achieve spectral-efficient use of the radio frequency (RF) spectrum and high modulation schemes have also led to augmented power consumption. Published results over the past decade report linearities of SFDR > 65 dBc at sampling frequencies above 6 GHz [4–6].
With communication standards such as 5G and mm-Wave communications, a DAC operating at higher channel bandwidths with maintained linearity is required, in turn, increasing the design challenges to maintain low-power consumption [7]. However, not much about the actual required power consumption in high-speed DACs has been reported [8]. Acquiring knowledge of the energy limitations required to achieve a certain SNR, SFDR, and signal bandwidth is relevant to identify how much power savings can be obtained. The analysis presented in this paper addresses power and energy consumption concerns from a design point of view.

A CMOS binary-weighted DAC architecture is utilized as the base model for our investigations. It is regarded to be the less power-hungry solution due to its intrinsic simplicity in the data conversion process. Moreover, the current-steering topology is considered as it is one of the preferred options for high-speed DAC operation since it has no need for buffers and provides a simplistic architecture.

A generic current-steering DAC is illustrated in Fig. 1 showing its main building blocks. Our study starts with a noise-limited analysis as the fundamental bounding condition. Then, speed and linearity requirements are added and addressed to determine how they could influence the energy required to meet the SNR and SFDR specifications. Fundamental building blocks, including switching drivers, buffers, and timing circuits are included in the model, but we have omitted the digital signal processing parts and other conditional circuitry as they are too diverse and application specific. We discuss the implications of this assumption.

The paper is organized as follows: In Sect. 2 a derivation of the SNR taking the noise contributions into account is presented along with the power consumption for a differential CS DAC. In Sect. 3 an elaborated analysis considering the power and energy consumption bounds for noise, speed, and linearity is presented. In Sect. 4 additional design considerations with respect to the bias network, output impedance and load resistance are discussed. In Sect. 5, data from reported measurement results are compared with the data obtained from the analysis which validates and motivates the theoretical results. Finally, the paper is concluded in Sect. 6.

2 Preliminary notes

In this paper, energy and power consumption bounds aimed at CMOS current-steering DACs are derived. We utilize a differential N-bit structure and a unary current $I_u$ representing the least significant-bit (LSB). Each single-ended output is terminated by a resistive load $R_L$ as shown in

Fig. 1 Structural overview of a generic current-steering digital-to-analog converter (CS DAC)

Fig. 1. The analog supply voltage is $V_{AVDD}$. The full-scale current, $I_{FS}$, attained at the single-ended output is

$$I_{FS} = (2^N - 1) \cdot I_u$$

and the differential voltage swing at the output is

$$V_{sw,d} = 2 \cdot (2^N - 1) I_u R_L$$

The output swing is usually dictated and specified by the following blocks, like a power amplifier or mixer, dependent on the system architecture. Adjustments of the parameters $I_u$, $N$, and $R_L$ are then required to set the swing. Assuming a full-scale sinusoidal signal, the normalized output power delivered by the differential CS DAC in units of amperes$^2$ is

$$P_{\text{sig}} = \frac{I_{FS}^2}{\sqrt{2}}$$

Thermal noise will arise in both resistive loads, $R_L$, and inside the DAC itself and will be present at the output which will in turn determine the SNR as well as the ENOB. We have selected to bound the thermal noise such that its power equals the quantization noise power. The total noise power then equals the sum of the thermal noise power, $P_{Th}$, and the quantization noise power, $P_Q$, which can be expressed in units of amperes$^2$ as

$$P_{\text{noise}} = \frac{(2I_u)^2}{12} + \frac{(2I_u)^2}{12} = \frac{(2I_u)^2}{6}$$

The SNR is defined as the ratio between the signal and noise power and with (3) and (4) we get

$$\text{SNR} = \frac{P_{\text{sig}}}{P_{\text{noise}}} = \frac{3}{4} \cdot (2^N - 1)^2$$
where the supply voltage is \( V_{\text{AVDD}} = V_{\text{hr}} + V_{\text{swd}}/2 \), with \( V_{\text{hr}} \) as the voltage headroom to bias the analog circuits. Figure 2 shows the switch current cell (CC) with the stacked transistors \( M_{\text{sw}} \) and \( M_{\text{cs}} \) as the switch and current source transistors, respectively. As will be explained in Sect. 3, a reduction of the current \( I_u \) is limited by noise, speed and linearity requirements, whereas a reduction of \( V_{\text{hr}} \) depends on the number of stacked transistors. The simplest differential current cell consists of two stacked transistors, offering the lowest headroom, \( V_{\text{hr}} \) [9]. Transistor \( M_{\text{cs}} \) operates as a current source, and its effective voltage, \( V_{\text{eff,Mc}} \), is set to \( 2V_{\text{th,d}}/a \). To guarantee that the current source transistor \( M_{\text{cs}} \) operates in saturation, its drain-to-source voltage, \( V_{\text{ds,Mc}} \), is set to \( 2V_{\text{th,d}}/a \) with \( a > 0 \) and the voltage headroom can be written as:

\[
V_{\text{hr}} = (1 + \beta)V_{\text{eff,Mc}} = \beta V_{\text{eff,Mc}}
\]

(8)

with \( \beta = (1 + \alpha) \). For \( M_{\text{sw}} \) to operate in saturation, its drain voltage, \( V_{\text{d,Ms}} \), needs to satisfy \( V_{\text{d,Ms}} \geq V_{\text{gt,Ms}} \) where \( V_{\text{d,Ms}} = V_{\text{hr}} \) and \( V_{\text{gt,Ms}} = V_{\text{g,Ms}} - V_{\text{th,Ms}} \) with \( V_{\text{g,Ms}} = \text{the voltage at the gate of } M_{\text{sw}} \) with respect to ground, and \( V_{\text{th,Ms}} \) its threshold voltage, respectively. Substituting (8) into (7) and using \( V_{\text{AVDD}} = V_{\text{hr}} + V_{\text{swd}}/2 \), the analog power consumption becomes:

\[
P_{\text{DACa}} = (2^N - 1)(\beta V_{\text{eff,Mc}} + V_{\text{swd}}/2)I_u
\]

(9)

To minimize this expression, it is clear that \( I_u \) and \( V_{\text{eff,Mc}} \) should be minimized. In Sect. 3 we derive an expression to find the optimum \( V_{\text{eff,Mc}} \) for minimum \( P_{\text{DACa}} \) due to noise constraints.

\section{2.2 Digital domain}

In the DAC model in Fig. 1, the digital blocks consist of switch drivers, timing circuits and clock/data buffers. Timing circuits are needed to synchronize data, but at a cost of higher power consumption and area. The digital blocks in our analysis are mainly implemented with CMOS static logic [11]-[13], but it is noted that current-mode logic (CML) is also utilized in high-speed DACs [14]. It is well-known that digital power consumption equals [15]

\[
P_{\text{DACd}} = P_{\text{sw}} + P_{\text{sc}} + P_{\text{leak}} + P_{\text{sta}}
\]

(10)

with \( P_{\text{sw}}, P_{\text{sc}}, P_{\text{leak}}, \) and \( P_{\text{sta}} \) as switching, short-circuit, leakage and static power. In the model, rail-to-rail voltage swing and no use of pseudo-CMOS logic cancels the static component \( P_{\text{sta}} \). Also considering ideal data/clock transitions reduce \( P_{\text{sc}} \) to zero [16]. Albeit a potentially considerable factor in modern digital circuits, the leakage current \( P_{\text{leak}} \) is omitted from our analysis. As a result, \( P_{\text{sw}} \) remains in (10) and the \( P_{\text{DACd}} \) for an \( N \)-bit CS DAC is:

\[
P_{\text{DACd}} = (2^N - 1)V_{\text{VDVDD}}^2(2a_{01}C_d + C_{\text{clk}})f_s
\]

(11)

where \( a_{01} \) is the switching activity, i.e., the probability of a \( 0 \rightarrow 1 \) transition per clock cycle, \( C_d \) is the capacitance contribution from the timing circuits/switching drivers and data buffers, \( V_{\text{VDVDD}} \) is the digital supply voltage and \( C_{\text{clk}} \) originates from the clock buffers and due to that nature is scaled by \( a_{01} = 1 \).

\section{2.3 Mixed-signal domain}

Additional power dissipation comes from charging the gate capacitance, \( C_{g,\text{sw}} \), in the switch transistors (\( M_{\text{sw1,2}} \) in Fig. 2). The power consumption from the mixed-signal domain becomes [12, 17]

\[
P_{\text{DACm}} = a_{01}(2^N - 1)C_{g,\text{sw}}V_{\text{g,Ms}}^2f_s
\]

(12)
where \( C_{g,sw} = 2W_{sw}L_{sw}C_{ox}/3 + 2C_{g,ov} \), with \( C_{g,ov} \) as the overlap capacitance, and \( V_{g,M_{sw}} \), the voltage swing at the gate of \( M_{sw1,2} \).

### 2.4 DAC Power consumption

The total DAC power consumption, \( P_{DAC} \), is the sum of the power from the analog, digital and mixed-signal domains. In the worst-case scenario, when operating at the Nyquist rate with \( f_{s} = f_s/2 \) and \( s_{0} = 0.5 \), \( P_{DAC} \) can be approximated for \( N \geq 6 \) by,

\[
P_{DAC} \approx 2^{N-1} \left[ (2\beta V_{eff,M_{sw}} + V_{sw,d})I_{u} + 2V_{DD}^{2}C_{T}f_{s} \right]
\]

where \( C_{T} = C_{d}/2 + C_{g,sw}/2 + C_{ch} \), and \( V_{DD} = V_{g,M_{sw}} \).

### 3 Analog power bounds in CS DACs

We are now able to elaborate further on the expressions to find the optimum values that minimizes power consumption. Presented below is the analysis with respect to noise, speed, and linearity bounds.

#### 3.1 Noise-limited bound

To obtain a noise-limited bound, uncorrelated thermal noise contribution from the current source transistors and the single-ended load resistors, \( R_L \), are taken into consideration. Flicker noise from the current source transistors is omitted due to its relevance only at low frequencies. The thermal noise from the gate resistance, \( R_G \), is neglected as it is small [18]. For a CS DAC operating with a signal bandwidth \( \Delta f \) and a temperature \( T \), the power of the thermal noise in amperes\(^2\) is

\[
P_{Th} = 4k_{B}T \left( (2^{N} - 1)\gamma g_{m} + \frac{2}{R_L} \right) \Delta f
\]

with \( k_{B} \) and \( \gamma \) as the Boltzmann and technology excess noise constant, and \( g_m \) the transconductance of \( M_{cs} \) given by

\[
g_{m} = \frac{2I_{u}}{V_{eff,M_{cs}}} = \frac{2I_{u}}{V_{GS} - V_{th}}
\]

Substituting (15) into (14), the thermal noise power is

\[
P_{Th} = 8k_{B}T \left[ \left( (2^{N} - 1)\gamma \frac{I_{u}}{V_{eff,M_{cs}}} + \frac{1}{R_L} \right) \Delta f \right]
\]

Since \( P_{Th} \) is equal to the quantization noise power, it can also be expressed as

\[
P_{Th} = \frac{(2I_{u})^{2}}{12}
\]

Then (16) together with \( R_L = V_{sw,d}/2(2^{N} - 1)I_{u} \) yields

\[
\frac{(2I_{u})^{2}}{12} = \frac{8(2^{N} - 1)k_{B}T_{u}}{V_{sw,d}}(\gamma V + 2)\Delta f
\]

with \( V \) as the ratio \( V_{sw,d}/V_{eff,M_{cs}} \). Solving for \( I_{u} \) in (18) with \( \Delta f \) as the Nyquist bandwidth, \( f_s/2 \) a lower bound for \( I_{u} \) due to noise bounds is obtained and approximated for \( N \geq 6 \)

\[
I_{u,n} \approx \frac{12k_{B}T_{2}^{2}}{V_{sw,d}}(\gamma V + 2)f_s
\]

Substituting (19) into (9) gives

\[
P_{DAC,n} \approx \frac{6k_{B}T_{2}^{2}}{V_{sw,d}}(2\beta \gamma + 4\beta V^{-1} + \gamma V + 2)f_s
\]

For minimum \( P_{DAC} \) with respect to \( V_{eff,M_{cs}} \), we derive (20) and set to zero:

\[
\frac{\partial P_{DAC}}{\partial V_{eff,M_{cs}}} = \frac{6k_{B}T_{2}^{2}}{V_{sw,d}} \left( \frac{4\beta}{V_{sw,d}} - \frac{\gamma V_{sw,d}}{V_{eff,M_{cs}}^{2}} \right)f_s = 0
\]

Solving for \( V_{eff,M_{cs}} \) in (21), we get an expression for \( V_{eff,M_{cs}} \) that reaches a minimum \( P_{DAC,n} \) as

\[
\frac{4\beta}{V_{sw,d}} - \frac{\gamma V_{sw,d}}{V_{eff,M_{cs}}^{2}} \Rightarrow V_{eff,M_{cs}} = \sqrt{\frac{\gamma V_{sw,d}}{2}}
\]

Thus, \( V_{eff,M_{cs}} \) is a function of \( V_{sw,d} \), \( \beta \) and \( \gamma \). Since \( \beta = (1 + \alpha) \), with \( \alpha = V_{DS,M_{cs}}/V_{eff,M_{cs}} \), an expression that relates \( V_{eff,M_{cs}} \) and \( V_{DS,M_{sw}} \) is found by expanding (22) as

\[
V_{eff,M_{cs}}^{2} + V_{eff,M_{cs}}V_{ds,M_{sw}} - \frac{\gamma V_{sw,d}^{2}}{4} = 0
\]

Solving for \( V_{eff,M_{cs}} \) in (23), we get the following two roots

\[
r_{1,-}, r_{2+} = \frac{\sqrt{D}}{2}, D = V_{DS,M_{sw}}^{2} + \gamma V_{sw,d}^{2}
\]

Root \( r_{1,-} \) is discarded as it is negative. Using the expressions for \( V_{DS,M_{sw}} \) and \( V_{sw,d} \), the effective gate voltage \( V_{eff,M_{cs}} \) is calculated. The bound for \( P_{DAC} \) due to the noise-limited condition is derived by substituting (22) into (20), where we get

\[
P_{DAC,n} \approx 12k_{B}T_{2}^{2}\left( \sqrt{\beta \gamma + 1} \right)^{2} f_s
\]

### 3.2 Speed-limited bound

The speed of the DAC is limited by the response time of the complementary switching transistors, \( M_{sw1,2} \), and the settling time of the output signal. The switching speed is
related to the transit frequency, $f_T$, which for submicron CMOS processes now reaches beyond 100 GHz [19]. The settling time is determined by the load’s time constant $R_L C_L$, which also limits the output signal bandwidth to

$$BW = \frac{1}{2\pi R_L C_L} \quad (26)$$

From (26), minimizing $R_L C_L$ is necessary to achieve the highest bandwidth. $R_L$ is one of the design parameters, whereas $C_L$ is composed of all the capacitance present at the output node with respect to ground. Moreover, $C_L = (2^N - 1) C_t$, with $C_t$ as the drain-to-ground capacitance of the individual current cell as shown in Fig. 2.

Since $M_{sw1,2}$ are operating in saturation, $C_t$ is reduced to the diffusion capacitance, and is determined by the device dimensions and technology parameters. Assuming that the bandwidth equals the Nyquist bandwidth, $f_s/2$, and using (26), the sample frequency $f_s$ can be given in terms of $C_t$ by

$$f_s = \frac{1}{(2^N - 1) \pi R_L C_t} \quad (27)$$

To maximize $f_s$, this suggests utilizing the smallest $C_t$ given by the technology and minimum sized transistors should be used for $M_{sw1,2}$. The load resistance, $R_L$, can be reduced to increase $f_s$, at the cost of augmented $I_u$ and $P_{DAC}$ to maintain a fixed $V_{sw,d}$. Substituting for $R_L = V_{sw,d}/(2^N - 1) I_u$ in (27) and solving for $I_u$ from the speed bound, we get

$$I_{u,s} = \frac{\pi V_{sw,d} C_f f_s}{2} \quad (28)$$

For example, setting $V_{sw,d} = 1$ V and $C_t \sim 0.1$ fF, the currents $I_{u,s}$ and $I_{u,n}$ are normalized with respect to $f_s$ (GHz) and plotted versus the SNR in Fig. 3. A crossing point between $I_{u,s}/f_s$ and $I_{u,n}/f_s$ around an SNR of 45 dB is observed. For SNR < 45 dB ($N=8$), the minimum $I_u$ is dominated by the speed bound; and for SNR > 45 dB, the noise bound dominates.

If the sizes of $M_{sw1,2}$ are kept at a minimum for different magnitudes of current $I_{u,s}$, adjustments in the voltage headroom $V_{hr}$ must take place to counteract the additional voltage drop. This effectively alters the $V_{eff,M_u}$ and $\beta$. If instead $V_{hr}$ is chosen to be fixed, adjustments in the width of $M_{sw1,2}$, $W_{sw}$, are necessary. For the latter, and as a first-order approximation (without body-effect and channel-length modulation), $W_{sw}$, is sized according to

$$W_{sw} = I_{u,s} \left( \frac{L_{sw}}{KV_{eff,M_u}} \right) \quad (29)$$

where $K = \mu_n C_{ox}/2$ and $\mu_n$ is the electron mobility and $C_{ox}$ is the gate-oxide capacitance per unit area. It is worth noting that $C_t = C' + (W_{sw} + 2I_u) C_{j-sw}$ with $C'$ as the junction capacitance in F, $l$ the junction length in m, and $C_{j-sw}$ the sidewall capacitance in F/m. Consequently, $C_t$ becomes a function of $I_{u,s}$, and therefore another expression for $I_{u,s}$ can be derived after substituting (28) into (29) as

$$I_{u,s} = \frac{\pi K V_{sw,d} V_{eff,M_u} f_s}{2KV_{eff,M_u}^2 - \pi V_{sw,d} L_{sw} V_{eff,f_s} C_1} \quad (30)$$

with $C_0 = C' + 2C_{j-sw}$ and $C_1 = C_{j-sw}$. From (30), in order to have mathematical consistency and maintain $I_{u,s} > 0$, the inequality $2KV_{eff,M_u}^2 > \pi V_{sw,d} L_{sw} f_s C_1$ needs to be satisfied, which sets a bound for $f_s$ as

$$f_s < \frac{2KV_{eff,M_u}^2}{\pi V_{sw,d} L_{sw} C_1} \quad (31)$$

From (31), the maximum $f_s$ is proportional to $V_{eff,M_u}$, and $\mu_n$. On the contrary, a longer channel length $L_{sw}$ and $C_1$ reduces $f_s$. Nevertheless, from (27), to achieve maximum $BW$, minimum $C_t$ is required, suggesting the utilization of minimum sized $M_{sw1,2}$. Then, $P_{DAC}$ due to speed-limited conditions is obtained by substituting (28) into (9), which yields

$$P_{DAC,s} \approx 2N^2 \pi C_1 (2\beta V_{eff,M_u} V_{sw,d}^2 + V_{sw,d}^2) f_s \quad (32)$$

### 3.3 Linearity-limited bound

Sources of linearity degradation can be classified in terms of amplitude and timing errors [20, 21]. Part of the amplitude errors is due to current mismatch in the output currents and threshold voltages in the $M_{CS}$ transistors is related to process and temperature variations as well as
To counteract for process variations, the transistors are increased in size and placed with reduced dimensions and the spacing, \( D \), between MOS transistors as suggested by [22, 23]

\[
\sigma^2(DI) = \left\{ \begin{array}{l}
\frac{A_{j}^2}{WL} + \frac{S_p^2 D^2}{2} \\
\frac{4A_{VT}^2}{WL(V_{gs} - V_{th})^2}
\end{array} \right.
\]  

(33)

with \( A_{j} \), \( A_{VT} \) and \( S_p \) as process-dependent parameters.

To counteract for process variations, the transistors are increased in size and placed with reduced dimensions and the spacing, \( D \), between MOS transistors as suggested by [22, 23]. The output impedance reduces as the frequency of the signal reaches the Nyquist bandwidth. As an example, Fig. 2 shows the drain-to-ground parasitic capacitance in \( M_{cs} \), \( C_s \), at the common node \( V_s \), creating a pole which will be indicated in this section. Other CCs integrate more than one cascode transistor to augment the output impedance [24]. Initially, we limit ourselves to the single-stacked CC and no timing errors to treat the linearity-limited bound.

To analyze the linearity with respect to \( P_{DAC} \), the SFDR is taken for a differential DAC, which is expressed as [25, 26]

\[
SFDR = \left[ 1 - \frac{2}{\rho_G \cdot x} \left( \frac{1}{\rho_G \cdot x} + \sqrt{\frac{1}{(\rho_G \cdot x)^2} - 1} \right) \right]^2
\]

(34)

where \( x \) is the ratio between the AC amplitude, \( X_{AC} \), and the DC level, \( X_{DC} \), of the single-ended input signal. For a full-scaled signal we have \( X_{DC} = X_{AC} = 2^{N-1} \). Also, \( \rho_G \) in (34) is given by

\[
\rho_G = \frac{1}{1 + (|\rho_G| \cdot X_{DC})^{-1}}
\]

(35)

with \( \rho_G \) as the conductance ratio’s magnitude, \( \rho_G \), as

\[
|\rho_G| = \frac{R_L}{R_{out}} \cdot \sqrt{\frac{1 + (\omega R_{out} C_s)^2}{1 + (\omega R_{out} C_s)^2}}
\]

(36)

For a well-designed current source, \( \rho_G \) is close to zero and (34) approximates

\[
SFDR \approx \frac{16}{\rho_G^{16}}
\]

(37)

\[ |Z_{out}| \] of the chosen current cell can be modeled as [27]

\[
|Z_{out}| \approx \frac{1}{\sqrt{(R_{out}^{-2} + \omega^2 C_s^{-2})}}
\]

(38)

with \( \omega = 2\pi f_{sig} \) and \( R_{out} \) the output resistance. As a first-order approximation, \( R_{out} \) for the single-stacked CC is

\[
R_{out} \approx g_{m,s}_{sw} r_{0,sw} r_{0,cs} = \frac{2}{\lambda_{sw} \square_{cs} V_{eff, Msw} I_u}
\]

(39)

where \( g_{m,s}_{sw} = 2I_u/V_{eff, Msw} \), \( r_{0,sw} = 1/\lambda_{sw} I_u \) and \( r_{0,cs} = 1/\lambda_{cs} I_u \), with \( \lambda_{sw} \) and \( \lambda_{cs} \) as the channel modulation values, and \( g_{m,s}_{sw} \), \( r_{0,sw} \) the transconductance of \( M_{sw} \). The output impedance has a pole at \( 1/2\pi r_{0,cs} C_s \), \( \lambda_{cs} I_u/2\pi C_s \) and the frequency response of \( |Z_{out}| \) can be separated into the following regions \( f_{sig} \leq \lambda_{cs} I_u/2\pi C_s \), and \( \lambda_{cs} I_u/2\pi C_s < f_{sig} \).

These two cases are treated in more detail later in this section. Substituting for \( |Z_{out}| \) in (36), and solving for \( f_{sig} = f_s/2 \), with \( f_s \) as \( 1/2\pi R_{L} C_s \), \( |\rho_G| \) is reduced to

\[
|\rho_G| = \frac{1}{|Z_{out}|} \cdot \frac{R_L}{\sqrt{\frac{1}{1 + \left(\frac{f}{f_s}\right)^2}}}
\]

(40)

Solving for \( |\rho_G| \) in (28) for a full-scale input signal, and substituting for \( \rho_G = 2/\sqrt{SFDR} \), we get

\[
|\rho_G| = \frac{1}{2^{N-1} \cdot F(SFDR)}
\]

(41)

with \( F(SFDR) = \sqrt{SFDR}/2 - 1 \). Substituting (41) into (40) for \( |\rho_G| \) and solving for \( |Z_{out}| \) gives

\[
\frac{1}{|Z_{out}|} \cdot \frac{R_L}{2^{N-1} F(SFDR)} \Rightarrow |Z_{out}| = \frac{2^{N-1} F(SFDR) R_L}{\sqrt{2}}
\]

(42)

Since \( R_L = V_{sw,d}/(2^{N-1} I_u) \), (42) can also be given by

\[
|Z_{out}| \approx \frac{F(SFDR) V_{sw,d}}{2^{2N} |\rho_G|}
\]

(43)

From (43) it is seen that a reduction in \( |Z_{out}| \) is obtained either by reducing \( V_{sw,d} \) or increasing \( I_u \) at the cost of a higher power consumption. The unity current \( I_u \) is obtained from (43) as

\[
I_u = \frac{F(SFDR) V_{sw,d}}{2^{2N} |\rho_G|}
\]

(44)

and can be calculated from the SFDR and \( |Z_{out}| \) requirements. The output impedance \( |Z_{out}| \) is also a function of \( I_u \), see (39). Substituting (38) and (39) into (44), and utilizing \( H = F(SFDR) V_{sw,d}/2\sqrt{2} \) gives

\[
I_u = H \cdot \sqrt{\left(\frac{(\lambda_{sw} \lambda_{cs} V_{eff, Msw} I_u)^2}{4} + \omega^2 C_s^2 \right)}
\]

(45)

If \( f_{sig} \leq 1/2\pi r_{0,cs} C_s \), then (45) can be reduced to

\[
4 = \left( H \lambda_{sw} \lambda_{cs} V_{eff, Msw} \right)^2
\]

and the SFDR is obtained from the
product \( \lambda_{sw} \lambda_{cs} V_{eff,sw} \). This result does not depend on frequency nor \( I_u \). If \( f_{sig} > 1/2 \pi \lambda_{0,cs} C_x \), the term \( \omega^2 C_x^2 \) dominates and \( I_u \) can be expressed as
\[
I_u = \frac{\pi f_i C_x F(SFDR) V_{sw,d}}{\sqrt{2}} \tag{46}
\]

The pole, \( 1/2 \pi \lambda_{0,cs} C_x \), equals \( \lambda_{cs} I_u / 2 \pi C_x \), and is also a function of \( I_u \). A criteria to satisfy \( f_{sig} > 1/2 \pi \lambda_{0,cs} C_x \) is defined when operating at \( f_{sig} = f_i / 2 \) as
\[
I_u < \pi C_x f_s / \lambda_{cs} \tag{47}
\]

Substituting (46) into (47) yields
\[
F(SFDR) V_{sw,d} < \frac{1}{\lambda_{cs}} \tag{48}
\]

If (48) is satisfied, the pole is located at a frequency below Nyquist, which can be expressed as \( \lambda_{cs} I_u / 2 \pi C_x < f_s / 2 \). The linearity-limited power bound when satisfying (47) and \( f_{sig} = f_i / 2 \) is found after substituting (49) into (9) as
\[
P_{DAC,i} \approx \frac{2^{N-1} \pi F(SFDR) C_x \left( 2 \beta V_{eff,Mcs} V_{sw,d} + V_{sw,d}^2 \right) f_i}{\sqrt{2}} \tag{49}
\]

A similar analysis can be realized when adding a cascode transistor with \( M_{cs} \), as illustrated in Fig. 4a. The frequency response of \( Z_{out} \) is shown in Fig. 4b [12], and it is divided in two regions separated by the zero \( gm_{cas} / 2 \pi C_{cs} \). Thus, for \( f_{sig} > gm_{cas} / 2 \pi C_{cs} \), the pole becomes \( 1 / 2 \pi \lambda_{0,cs} C_x \), and \( V_{eff,Mcs} \) in (49) is substituted by \( V_{eff} \) instead.

The total power \( P_{DAC} \) is calculated taking the noise, speed and linearity requirements into account. For the noise and speed bounds, the SNR is taken into consideration. For the linearity bound, the SFDR is instead used.

### 4 Power consumption design considerations

In addition to the analysis presented above, other aspects concerning power consumption are treated in this section, including the bias network, output impedance, and load resistance.

#### 4.1 Bias network

The simplest bias network consists of a current mirror transistor connected at the gate of the current source transistors. However, long interconnections between the reference current mirror and the source transistors can lead to mismatch errors [28, 29]. Hence, a more elaborated bias network can be used with added power consumption. The noise contribution from the bias network is modeled in Fig. 5. The noise power spectral density from the bias network corresponds to the current source \( I_{n,bias} \). Also, the input-referred noise contribution of each current source \( i \) at its gate is model with a current source \( I_{n,i} \). Then, the total noise, \( I_{n,in} \), equals \( (2^N - 1)I_{n,i}^2 + I_{n,bias}^2 \). Then, the total power, \( P_{n+bias} \), is given by
\[
P_{n+bias} = 4 k_{B} T \left( 2^N - 1 \right) g_m (1 + \eta_{bias}) \tag{50}
\]

As shown in appendix, \( \eta_{bias} \) is inversely proportional to \( (\omega C_{bias})^2 \) with \( C_{bias} = (2^N - 1) C_{g,cs} + C_{parasitics} \). Then,
of $n_{\text{bias}}$ approximates to zero for high-speed and resolution and omitted from the analysis.

### 4.2 Current source output impedance

From (45), when operating at $f_{\text{sig}} \leq 1/2\pi r_{0,c5} C_s$, then $(\lambda_{\text{sw}} \lambda_{\text{cs}} V_{\text{eff,Msw}} H)^2 = 4$, which relates $\lambda_{\text{s}} = \lambda_{\text{sw}} \lambda_{\text{cs}}$ with respect to the SFDR, $V_{\text{eff,Msw}}$ and $V_{\text{sw,d}}$, by

$$\lambda_{\text{s}} = \frac{4 \sqrt{2}}{F(\text{SFDR}) V_{\text{eff,Msw}} V_{\text{sw,d}}} \quad (51)$$

In Fig. 6, $10 \lambda_{\text{s}}^{-1}$ is plotted versus the SFDR for $V_{\text{eff,Msw}} = 0.1$ V and $V_{\text{sw,d}} = 1$ V, where $10 \lambda_{\text{s}}^{-1}$ increases at a constant rate for an SFDR > 50 dBc with $\lambda_{\text{s}}$ expressed as

$$\lambda_{\text{s}} = \frac{k_{\text{ds}} (L_{\text{sw}} L_{\text{cs}})^{-1}}{4 \sqrt{V_{\text{DS,sw}} - V_{\text{eff,sw}} + \Phi_0} \sqrt{V_{\text{DS,cs}} - V_{\text{eff,cs}} + \Phi_0}} \quad (52)$$

with $k_{\text{ds}}$ and $\Phi_0$ as technology parameters, $L_{\text{sw}}$ and $L_{\text{cs}}$ as the channel length of $M_{\text{sw}}$ and $M_{\text{cs}}$. For reduced $V_{\text{hr}}$, we have $V_{\text{DS,sw}} = V_{\text{eff,Msw}}$ and $V_{\text{DS,cs}} = V_{\text{eff,Mcs}}$, simplifying (52) to

$$\lambda_{\text{s}} = \frac{k_{\text{ds}}^2}{4 L_{\text{sw}} L_{\text{cs}} \Phi_0} \quad (53)$$

To reduce $\lambda_{\text{s}}$, it is necessary to either increase $L_{\text{sw}}$ or $L_{\text{cs}}$. Increasing $L_{\text{sw}}$ to reach higher output impedance, augments the mixed-signal power consumption as suggested by (12) and reduces the bound for $f_s$ according to (31). Consequently, $L_{\text{sw}}$ remains with minimum size in the analysis, and $L_{\text{cs}}$ is sized instead to satisfy (51), without extra expense in power consumption. Further on, $L_{\text{cs}}$ is sized based upon mismatch specifications in the current sources as suggested by (33). Therefore; $L_{\text{cs}}$ should be taken from the maximum $L_{\text{cs}}$ from these two analyses.

### 4.3 Output load resistance

Another important design consideration has to do with the selection of $R_L$. Usually, an output resistance of 50 $\Omega$ is used to facilitate the matching of the output ports with other building blocks, e.g., reconstruction filters, RF baluns. If it is specified to achieve $V_{\text{sw,d}} = 1$ V, $I_u$ can be found as

$$I_u = \frac{V_{\text{sw,d}}}{2(2^N - 1) R_L} \quad (54)$$

From (54), it is shown that as $N$ is larger, $I_u$ decreases for a fixed $V_{\text{sw,d}}$ and $R_L$, which can compromise the SNR/SFDR as explained in Sect. 3. Another approach is to choose $I_u$ from the SNR, or SFDR requirements, and calculate an optimum $R_L$ instead. A matching network can be used between the DAC output and external building blocks to have impedance matching and maximum power transfer.

As an example, Fig. 7 plots the load resistance $R_L$ versus SNR according to the noise analysis at different sample frequencies $f_s$. The dash line corresponds to $R_L = 50$ $\Omega$, where we identify the crossing points with $f_s = 10$, 1 and 0.1 GHz for SNR of about 60, 70, 80 dB. For SNRs where $R_L \geq 50$ $\Omega$ from the noise bound curves, an $R_L = 50$ $\Omega$ can be utilized instead as it does not compromise the SNR. Beyond the crossing points with higher SNR, the $R_L$ must instead be chosen from the noise bound. A similar analysis can be done for the speed and linearity bounds.

### 5 Verification with measurement results

To validate the theoretical analysis, the energy bounds, including analog, digital and mixed-signal power domains, for the three different design corners, i.e., noise, speed and linearity, are plotted in Figs. 8, 9 and 10 along with published measurement results. The publications use various types of current-steering DACs in different CMOS technologies. Table 1 lists the design and technology parameters utilized in the analysis. The capacitance values are obtained from a 65-nm CMOS process. Minimum sized switch transistors are used, and therefore, a range of allowed $V_{\text{ds,Msw}}$ voltages is specified. Table 2 lists the drain-to-source $V_{\text{ds,Msw}}$ values for 100 and 400 mV as well as the calculation of $V_{\text{eff,Mcs}}/V_{\text{hr}}$, $\beta$, $V_{\text{hr}}$ and $V_{\text{AVDD}}$. Full-scale current and load resistance, $I_{\text{FS}}$ and $R_L$, are determined by the unary current, $I_u$, and consequently, are not listed in Table 1. The noise energy bounds are plotted for a temperature of 75 $^\circ$C.

Figure 8 presents the energy consumption versus the SNR for the noise and speed design corners. The noise
bound is presented for two design cases, $\beta_1$ and $\beta_2$, see Table 2. In Fig. 8, for SNR < 50 dB, the two noise plots $\beta_1$, $\beta_2$ and the speed bounds converge at energy levels above 0.1 pJ as the digital and mixed-signal energy consumption start to become more dominant. For SNR > 50 dB, the noise bound dominates due to the strong exponential dependency of the ENOB according to (25). As SNR gets larger, noise plots $\beta_1$ and $\beta_2$ diverge, making it possible to see the implication of different switch voltages within the $V_{ds,Msw}$ range.

With respect to the ENOB, the speed design corner, the digital and mixed-signal components grow at a rate of $2^{ENOB}$, whereas the analog grows at $2^{ENOB-2}$. The analog component is linearly dependent on $C_1$, and scales down as device dimensions decrease. Thus, the speed bound is predominately dominated by the digital and mixed-signal components and grows proportional to $2^{ENOB}$. In Fig. 8, we also see that the noise bound dominates. It grows at a rate of $2^{2ENOB}$, and from SNR = 60 dB we see how this component dominates the exponential curve. Comparing measurement data in terms of noise bounds, it is observed that the data points follow the behavior of the curves $\beta_1$, $\beta_2$ even for current-steering DACs implemented with current-mode logic (CML) [14, 33, 34], which suggests an agreement with the theory presented in Sect. 3.

Figs. 9 and 10 plot the linearity energy bound versus the SFDR for the $\beta_2$ case. Measurement data from 12- and 16-bit DACs are presented. The linearity energy bound scales with device dimensions as it is a function of the common-node capacitance, $C_{x}$, and as a result, this bound is plotted for different CMOS process nodes. Some of the DACs utilize enhancement techniques to improve the SFDR at the cost of extra power consumption. The distortion reported in the measurement data come also from timing and amplitude errors, and not only limited due to output impedance. Therefore, the plots presented should be considered as a reference for comparison purposes between the linearity bound and the published measurement data.

In Fig. 9, the linearity bounds for a 12-bit DAC implemented in a 0.18 μm and a 65 nm CMOS processes are plotted along with measurement results from published 12-bit DACs in 0.18 μm and 65 nm CMOS processes to have a fair comparison between the theory and measured data. From Fig. 9, as is expected, we see that the measured results indicate a higher energy consumption with respect to the presented linearity energy bounds. It is observed a gap of about less than an order of magnitude in the data.

![Fig 6](image1.png) Current source output impedance factor $10/\lambda_{m}$ vs SFDR for an output voltage swing, $V_{sw,d}$, of 1 V and an effective voltage in the switching transistor, $V_{eff,Msw}$, equal to 0.1 V

![Fig 7](image2.png) Load resistance value $R_L$ versus the SNR requirement for noise corner and constant output voltage swing of 1 V for different sampling frequencies, $f_s$, of 0.1, 1, and 10 GHz

### Table 1 Technology and Design Parameters

| Parameter                  | Variable  | Value  |
|----------------------------|-----------|--------|
| Digital supply voltage     | $V_{DD}$  | 1 V    |
| Differential output voltage| $V_{sw,d}$| 1 V    |
| CC common-node capacitance | $C_x$     | $\approx 2.0\times10^{-2}$ fF |
| CC output capacitance      | $C_f$     | $\approx 0.5\times10^{-3}$ fF |
| CC gate capacitance        | $C_{g,sw}$| $\approx 1.5\times10^{-3}$ fF |
| Capacitance of the digital blocks | $C_d + C_{cl}$ | $\approx 13\times10^{-4}$ fF |
| Technology excess noise constant | $\gamma$ | 1.5 |

### Table 2 $V_{eff,Mcs}$ Calculation From Different $V_{ds,Msw}$

| $V_{ds,Msw}$ | $V_{eff,Mcs}/V_s$ | $V_{he}$ | $\beta$ | $V_{AVDD}$ | Plot Ref |
|--------------|-------------------|----------|---------|------------|----------|
| 100 mV       | $\approx 565$ mV  | $\approx 665$ mV | 1.18    | $\approx 1.17$ V | $\beta_1$ |
| 400 mV       | $\approx 445$ mV  | $\approx 845$ mV | 1.90    | $\approx 1.35$ V | $\beta_2$ |
points [37] and [38], except for [39], which incorporates a delta-sigma-assisted pre-distortion scheme to compensate for current mismatch at the cost of increased power consumption. On the other hand, utilization of decoding logic in combination with randomization circuits in [37], and utilization of a thermometer decoder with delay equalizers along with master and slave latches in [38] elevate also the power dissipation.

Figure 10 plots the energy consumption bound for a 65 nm CMOS processes, and 16-bit DACs manufactured in the same process node. The measured data report a higher energy consumption in comparison with the linearity energy bound, where it is observed how the measured data follows the bound trend as the requirement in the SFDR increases. Both [40] and [41] incorporate signal processing, in turn, increasing the overall power consumption as observed between the measured data and the linearity bound when operating with a channel bandwidth of $f_s/2$.

6 Conclusions

A theoretical analysis was presented to derive the energy consumption bounds for the three design corners, including noise, speed, and linearity in CMOS current-steering DACs. From the study, the digital and mixed-signal power contributions for the different design corners are observed to be less significant as technology scales down because of smaller device dimensions and reduced parasitic capacitances. On the contrary, the analog energy bound for the noise corner does not scale with the device dimensions and dominates over the digital and mixed-signal power domains for $\text{SNR} > 50 \text{ dB}$. It is found that the analog energy bound is strongly dependent on the ENOB by $2^{2\text{ENOB}}$, which agrees with the trend observed in the measured data when plotting energy consumption versus SNR.
In summary, the noise energy bound sets a limit that remains at different CMOS processes. On the other hand, the analog bounds for speed and linearity are functions of the device dimensions and parasitic capacitances, and therefore, they scale with technology. An expression for the common-node voltage in the differential current cell structure to achieve minimum analog power consumption is also derived. The expression is found to depend on design and technological parameters, including the differential output voltage swing, the ratio between the common-mode voltage in the differential current cell and the drain-to-source voltage of the switch transistors, and the technological noise constant, $\gamma$.

As technology scales down, the noise energy bound takes over as the parasitic capacitances in the device are reduced, decreasing the energy bounds for speed and linearity. From the comparison with measured data, a narrow gap between the noise energy bound is observed, whereas for the speed energy bound, it becomes larger than one order of magnitude. For the linearity energy bound, there is still some margin with respect to the measured results, which suggests that it is possible to reach even lower energy consumption.

**Appendix**

This appendix elaborates on the noise contribution from the bias network presented in Sect. 4.1 In Fig. 5, the total noise at the current source gate $V_b$ is

$$\bar{I}_{n,\text{out}}^2 = (2^N - 1)\bar{I}_{n,M}^2 + \bar{I}_{n,\text{bias}}^2$$

(55)

where $\bar{I}_{n,M}$ is the input-referred current noise and $\bar{I}_{n,\text{bias}}$ the current noise from the bias network. The total current output-referred noise equals

$$\bar{I}_{n,\text{out}}^2 = \left[ (2^N - 1)\bar{I}_{n,M}^2 + \bar{I}_{n,\text{bias}}^2 \right] |Z_{\text{bias}}|^2 g_m^2$$

(56)

with $|Z_{\text{bias}}|^2 = R_{\text{bias}}^2 / \left[ 1 + (\alpha R_{\text{bias}} C_{\text{bias}})^2 \right]$, and $g_m$ the transconductance. Furthermore, $C_{\text{bias}}$ equals to $(2^N - 1)C_{\text{gate}} + C_{\text{parasitic}}$, with $C_{\text{gate}}$ as the gate capacitance, and $C_{\text{parasitic}}$, the parasitic capacitance of the bias metal network. $C_{\text{gate}}$ is proportional to the transistor area, $WL$, which is normally large due to mismatch considerations. The transistor noise current contribution in (56) is

$$\bar{I}_{n,M}^2 = \frac{V_{n,M}^2}{\bar{I}_{\text{bias}}^2}$$

(57)

Substituting (57) in (56) for $N \geq 6$, $\bar{I}_{n,\text{out}}^2$ approximates to

$$\bar{I}_{n,\text{out}}^2 \approx g_m^2 \left( 2^N V_{n,M}^2 + \bar{I}_{n,\text{bias}}^2 |Z_{\text{bias}}|^2 \right)$$

(58)

For $|Z_{\text{bias}}|^2$ in (58), the noise current can be rewritten as

$$\frac{\bar{I}_{n,\text{out}}^2}{\bar{I}_{n,M}^2} \approx \frac{2^N}{g_m^2} + \frac{\bar{I}_{n,\text{bias}}^2}{\bar{I}_{n,M}^2} \left[ R_{\text{bias}}^2 + (\alpha R_{\text{bias}} C_{\text{bias}})^2 \right]$$

(59)

The first term in (59) is the total noise contribution from the current sources as indicated in (14), whereas the second term is the noise coupled to the output from the bias network. The second term is inversely proportional to $(\alpha C_{\text{bias}})^2$. The factor $\eta_{\text{bias}}$ is introduced such that $\bar{I}_{n,\text{out}}^2 = \bar{I}_{n,M}^2(1 + \eta_{\text{bias}})$, with $\eta_{\text{bias}}$ as

$$\eta_{\text{bias}} = \frac{\bar{I}_{n,\text{bias}}^2}{\bar{I}_{n,M}^2} \frac{g_m^2 R_{\text{bias}}^2}{1 + (\alpha R_{\text{bias}} C_{\text{bias}})^2}$$

(60)

From this we see that if $(\alpha C_{\text{bias}})^2 \rightarrow \infty$, $\eta_{\text{bias}} \rightarrow 0$ and the noise component can be neglected from the analysis. Essentially, with proper decoupling, the noise from the bias network can be minimized.

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**Data availability statement** The datasets generated during and/or analysed during the current study are available in the Data Availability Set: (Energy/Power Bounds CMOS CS DACs) repository, http://urn.kb.se/resolve?urn:nbn:se:liu:diva-178137.

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