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Abstract—Voltage multipliers (VMs) are widely used in applications with high-voltage-gain rectifiers and dc/dc converters with the capability of increasing voltage conversion ratio. Currently, all the existing VM circuits are designed with two input-terminals, while optimal design on voltage conversion ratio and voltage stress on semiconductor devices of the converters with VMs can be achieved by varying the number of basic VM units. However, as the fixed number of its input-terminals and thus the current stress on semiconductor devices are not adjustable at the design stage, such circuits have limited applications in today’s high-power energy conversion systems. In order to address such drawbacks of the conventional VMs, a multiple input-terminal VM (MIVM) circuit is proposed in this paper. Analysis of the operation principles and the performance characteristics of the proposed MIVM circuit are presented in detail. As an example, the application of the MIVM with traditional boost converters is presented and discussed, and the efficacy of the theoretical analysis is validated experimentally.

Index Terms—Multiple input-terminal voltage multiplier (MIVM), high voltage gain, current stress, boost converter

I. INTRODUCTION

Voltage multiplier (VM) is a high-voltage-gain rectifier which is essentially a capacitor-diode network. The history of VM can be traced back to early last century, when the first VM, known as Cockcroft-Walton voltage multiplier (CW-VM) as shown in Fig. 1(a), was proposed in 1932 in order to generate positive ions of hydrogen with a voltage level up to 300 kV [1]. As shown in Fig. 1(b), another well-known VM called Dickson voltage multiplier (D-VM) was proposed in 1976 to meet the requirements of power ICs and EEPROMs [2-3]. The modeling and analysis of these two types of VM circuits were intensively studied and well-developed [4-7].

In recent years, due to the high demand for high-voltage-gain dc/dc converters in the applications such as fuel cell and photovoltaic power generations, various VM circuits have been proposed and used to integrate with conventional dc/dc converters, aiming to get a higher voltage conversion ratio. Two-phase interleaved boost converters have been used to integrate with D-VM in [8-9] and CW-VM in [10-12], respectively. Based on the CW-VM circuit, a high voltage conversion gain dc/dc converter with the common ground has been proposed in [13]. Bipolar D-VM has been used to work with different converters, such as the conventional boost converter [15] and the two-phase interleaved boost converter [16-17]. A generalized structure for high-voltage-gain dc/dc converter based on VM and the boost converter (including both non-isolated and isolated boost) has been developed in [18] as shown in Fig. 2. Similar to this generalized structure, some other topologies with various VM circuits have been proposed in [19-21]. Coupled inductors have been used to further improve the voltage conversion ratio of the converters in [22-24].

Fig. 1. Topologies of two traditional VM circuits: (a) CW-VM, (b) D-VM.

Fig. 2. Generalized structure of the converters combing two-phase interleaved boost converter and traditional VM circuits.

There are some salient advantages when combining VM
circuits with the conventional boost converters. First, the voltage conversion ratio of converters can be further increased, and the voltage stress on semiconductor components can be reduced significantly by changing the number of basic cells in VM circuit. Second, when VM is integrated with two-phase interleaved boost converter, the relationship between the two input-terminal currents are determined by the duty ratio of the two switches, and the two input-terminal currents can be equalized automatically when the duty ratio of switches is set equal. However, limited by the input terminal number of the traditional VM circuits, only two-phase interleaved boost converters can combine with the traditional VM circuits. In a certain working environment, the current stress of the components like inductors or switches cannot be decreased when the input terminal of the converters is fixed [8-21]. This makes it difficult for these converters to be used in high power/current applications, e.g., dc collection grids for offshore wind farms [25-27].

Based on the previous work [28], a multiple input-terminal voltage multiplier (MIVM) circuit is proposed in this paper. Operation principles and performance characteristics of the proposed MIVM circuit are discussed in Sections II and III respectively. Applications of the proposed MIVM to traditional non-isolated and isolated boost converters are presented in Section IV. Theoretical analysis of the proposed MIVM circuit is verified experimentally in Section V. The main findings are concluded in Section VI.

II. TOPOLOGY AND ANALYSIS OF THE PROPOSED MIVM

Fig. 3 (a) shows the topology of the proposed MIVM where the corresponding input-terminals and the basic VM cells are indicated. Both the number of VM cells and the number of input-terminals of the MIVM can be adjusted during the design of the circuit.

To demonstrate the working principle of MIVM, the proposed MIVM with four input terminals and two VM units has been analyzed, as shown in Fig. 3 (b). Moreover, the analysis results of the MIVM have also been generalized to arbitrary number of input-terminals and VM cells. The following assumptions are made to simplify the analysis:

1) All devices are ideal, and the effects of parasitic parameters are ignored;
2) The input voltage source $u_{in}$ is sinusoidal, i.e.,
   \[ u_{in}(t) = U_m \cdot \sin \omega t \]  
   (1)
3) The capacitances value of the capacitor connected to the load are large enough, so that the ripple of the output voltage can be ignored due to the fact that it is much smaller than that of the other capacitors in MIVM, i.e. $\Delta u_{in} < \Delta u_{Vm}$.
4) The capacitances value of all capacitors in MIVM circuit except those connected with the load are equal, as $C_{11}=C_{21}=C_{12}=C_{22}=C_{Vm}$.

Fig. 4 shows the key waveforms of the MIVM during one period of the supply sinusoidal voltage. According to the Ampere balance principle on the capacitors in MIVM, in steady state, it can be derived that the average currents of all diodes $I_{D11}, I_{D12}, \ldots, I_{D42}$ are denoted as $I_{D11}, I_{D21}, \ldots, I_{D42}$ respectively as:

\[ I_{D11} = I_{D21} = \ldots = I_{D42} = I_o \]  
   (2)

Furthermore, the basic ripple on the capacitors is defined as $\Delta u_{Vm}$:

\[ \Delta u_{Vm} = \frac{I_o}{f \cdot C_{Vm}} \]  
   (3)

Where $f$ is the frequency of the input voltage source.

Based on the above assumptions, the working process of the MIVM in Fig. 2(a) is given as follows:

**Mode 1** $[0-t_1, t_1-t_2, t_1+2\pi \text{m} ]$, Fig. 5(a): At this stage, all diodes are off. The voltages of all capacitors except $C_{41}$ and $C_{42}$ keep their values, and the load is powered by $C_{41}$ and $C_{42}$.

**Mode 2** $[t_1-t_2]$, Fig. 5(b): The time of $D_{22}$ is turned on is determined by the input voltage $u_{in}$ and the voltages of capacitors $C_{11}, C_{12}, C_{21}, C_{22}$. Before this mode, the voltages across $C_{11}$ and $C_{12}$ are both at their peak value which are denoted as $u_{c11_{max}}$ and $u_{c12_{max}}$ and the voltages across $C_{21}$ and $C_{22}$ are both at their valley value which are denoted as $u_{c21_{min}}$ and $u_{c22_{min}}$. When the sum of $u_{in}, u_{c11}$ and $u_{c12}$ is greater than the sum of $u_{c21}$ and $u_{c22}$, $D_{22}$ is turned on. There is another problem, that is, how to judge the peak and valley voltage of each
capacitor. Take C11 for example, its peak value is \( U_m \) which can be obtained from Fig. 4(i) when D11 is working in on state. The valley value of C11 is denoted as \( u_{c11-min} \), and it can be obtained by (4) where \( \Delta u_{c11} \) is the voltage ripple of C11.

\[
\Delta u_{c11} = u_{c11-max} - u_{c11-min} = U_m - \Delta u_{c11} \tag{4}
\]

When capacitor C11 is discharged, the current will flow through diodes D21 and D22, the voltage ripple of C11 can be obtained by (5). And the valley voltage of C11 can be obtained by (5). Similarly, the peak, valley and ripple voltage of all capacitors can be acquired as shown in Table I.

Table I

| Capacitors | Peak voltage | Valley voltage | Ripple voltage |
|------------|--------------|----------------|----------------|
| C11        | \( 2U_m \)  | \( U_m-2\Delta u_m \) | \( 2\Delta u_m \) |
| C21        | \( 2U_m \)  | \( U_m+4\Delta u_m \) | \( 2\Delta u_m \) |
| C31        | \( 3U_m \)  | \( U_m-6\Delta u_m \) | \( 2\Delta u_m \) |
| C41        | \( 4U_m \)  | \( U_m-8\Delta u_m \) | \( 2\Delta u_m \) |
| C51        | \( 4U_m \)  | \( U_m-7\Delta u_m \) | \( 2\Delta u_m \) |
| C61        | \( 4U_m \)  | \( U_m-9\Delta u_m \) | \( 2\Delta u_m \) |
| C71        | \( 4U_m \)  | \( U_m-9\Delta u_m \) | \( 2\Delta u_m \) |

Appreciably, when the input voltage reaches \( U_m+6\Delta u_m \) at \( t_1 \), D22 is turned on. During this mode, capacitors C21 and C22 are charged, C11 and C12 are discharged. And the voltage of C21 rises from \( 2U_m-4\Delta u_m \) to \( 2U_m+3.25\Delta u_m \), the voltage of C22 rises from \( 4U_m-8\Delta u_m \) to \( 4U_m+7.25\Delta u_m \), the voltage of C11 decreases from \( U_m \) to \( 0.75\Delta u_m \), the voltage of C12 decreases from \( 4U_m-6\Delta u_m \) to \( 4U_m+6.75\Delta u_m \). In order to simplify the analysis process of other modes, the conduction conditions of other diodes will not be analyzed.

**Mode 3** \([t_2-t_3]\), Fig. 5(c): At \( t_2 \), when the input voltage reaches \( U_m-3\Delta u_m \), D12 and D22 are turned on. During this mode, capacitors C21, C22, C41 and C42 are charged, while C11, C12, C31 and C32 are discharged. And the voltage of C21 rises from \( 2U_m-3.25\Delta u_m \) to \( 2U_m+3\Delta u_m \), the voltage of C22 rises from \( 4U_m-7.25\Delta u_m \) to \( 4U_m+7\Delta u_m \), the voltage of C11 decreases from \( U_m-0.75\Delta u_m \) to \( U_m+6\Delta u_m \), the voltage of C12 decreases from \( 4U_m-6\Delta u_m \) to \( 4U_m+7\Delta u_m \). The voltage of C31 and C32 decreases from \( 3U_m-4\Delta u_m \) to \( 3U_m+4.5\Delta u_m \), the voltage of C41 and C42 decreases from \( 4U_m-8\Delta u_m \) to \( 4U_m+8.5\Delta u_m \). The voltage of C11 and C12 increases, but the voltage ripple of C11 and C12 are much smaller than other capacitors, it can be approximately considered that their voltage remain unchanged at \( 4U_m-6\Delta u_m \) and \( 4U_m+9\Delta u_m \), respectively.

**Mode 4** \([t_3-t_4]\), Fig. 5(d): At \( t_3 \), when the input voltage reaches \( U_m-2\Delta u_m \), D31 and D32 are turned on. During this mode, capacitors C21, C41 and C42 are charged while C11, C12, C31 and C32 are discharged. And the voltage of C21 rises from \( 2U_m-3\Delta u_m \) to \( 2U_m-2.5\Delta u_m \), the voltage of C11 decreases from \( U_m-1.5\Delta u_m \) to \( U_m-1.5\Delta u_m \), the voltage of C31 decreases from \( 3U_m-4.5\Delta u_m \) to \( 3U_m-5\Delta u_m \), the voltage of C41 decreases from \( 4U_m-8\Delta u_m \) to \( 4U_m-9\Delta u_m \).

**Mode 5** \([t_4-t_5]\), Fig. 5(e): At \( t_4 \), when the input voltage reaches \( U_m+\Delta u_m \), D21 and D23 are turned on. During this mode, capacitors C21 and C41 are charged while C11 and C31 are discharged. And the voltage of C21 rises from \( 2U_m+2.5\Delta u_m \) to \( 2U_m+2\Delta u_m \), the voltage of C11 decreases from \( U_m+1\Delta u_m \) to \( U_m+0.5\Delta u_m \), the voltage of C31 decreases from \( 3U_m+5\Delta u_m \) to \( 3U_m+4.5\Delta u_m \), the voltage of C41 decreases from \( 4U_m+8\Delta u_m \) to \( 4U_m+7\Delta u_m \).

**Mode 6** \([t_6-t_7]\), Fig. 5(f): When the input voltage is decreased to \( -U_m-6\Delta u_m \) at \( t_6 \), D32 is turned on. During this mode, capacitors C31 and C32 are charged, C21 and C22 are discharged. And the voltage of C31 rises from \( 3U_m-6\Delta u_m \) to \( 3U_m+5.25\Delta u_m \), the voltage of C32 rises from \( 4U_m-9\Delta u_m \) to \( 4U_m+8.25\Delta u_m \), the voltage of C21 decreases from \( 2U_m-2\Delta u_m \) to \( 2U_m-2.75\Delta u_m \), the voltage of C22 decreases from \( 4U_m-7\Delta u_m \) to \( 4U_m+7.75\Delta u_m \).

**Mode 7** \([t_7-t_8]\), Fig. 5(g): When the input voltage is decreased to \( -U_m-3\Delta u_m \) at \( t_7 \), D31 and D32 are turned on. During this mode, capacitors C11, C12, C31 and C32 are charged, C21, C22 and C42 are discharged. And the voltage of C11 rises from \( U_m+2\Delta u_m \) to \( U_m+1.5\Delta u_m \), the voltage of C12 rises from \( 4U_m-7\Delta u_m \) to \( 4U_m-6.5\Delta u_m \), the voltage of C31 rises from \( 3U_m+5.25\Delta u_m \) to \( 3U_m+5\Delta u_m \), the voltage of C32 rises from \( 4U_m+8.25\Delta u_m \) to \( 4U_m+7.5\Delta u_m \), the voltage of C21 decreases from \( 2U_m-2.75\Delta u_m \) to \( 2U_m-3\Delta u_m \), the voltage of C22 decreases from \( 4U_m-7.75\Delta u_m \) to \( 4U_m-8\Delta u_m \).

**Mode 8** \([t_8-t_9]\), Fig. 5(h): When the input voltage is decreased to \( -U_m-2\Delta u_m \) at \( t_8 \), D21 and D31 are turned on. During this mode, capacitors C11, C12 and C31 are charged, C21, C41 and C42 are discharged. And the voltage of C11 rises from \( U_m+1.5\Delta u_m \) to \( U_m+1.5\Delta u_m \), the voltage of C12 rises from \( 4U_m-6.5\Delta u_m \) to \( 4U_m-6\Delta u_m \), the voltage of C31 rises from \( 3U_m+6\Delta u_m \) to \( 3U_m+5.5\Delta u_m \), the voltage of C32 rises from \( 4U_m+4.5\Delta u_m \) to \( 4U_m+3\Delta u_m \), the voltage of C21 decreases from \( 2U_m-3\Delta u_m \) to \( 2U_m-3.5\Delta u_m \).

**Mode 9** \([t_9-t_10]\), Fig. 5(i): When the input voltage is decreased to \( -U_m+\Delta u_m \) at \( t_9 \), D11 and D13 are turned on. During this mode, capacitors C11 and C31 are charged, and C21 and C41 are
discharged. And the voltage of $C_{31}$ rises from $U_m-\Delta u_{vm}$ to $U_m$.

![Equivalent circuits for different modes of the proposed MIVM](image)

The voltage of $C_{31}$ rises from $3U_m-4.5\Delta u_{vm}$ to $3U_m-4\Delta u_{vm}$, the voltage of $C_{21}$ decreases from $2U_m-3.5\Delta u_{vm}$ to $2U_m-4\Delta u_{vm}$. This state ends at $t_{10}$ when the input voltage decreases to its negative peak value $-U_{lim}$.

III. PERFORMANCE CHARACTERISTICS

Firstly, performance characteristics of the MIVM with four input-terminals and two VM cells have been analyzed, then the results have been extended to general form of the MIVM circuit as shown in Fig 3(a).

A. Current of Input-Terminal and Current Stress on Capacitors

In the positive half cycle of the input voltage source, the average current of each input-terminal can be obtained as (6). While in the negative half cycle, the average input-terminal current is given in (7).
\[
\begin{align*}
i_1 &= -i_2 = I_{D21} + I_{D22} + \ldots + I_{D2n} = n \cdot I_o \\
i_3 &= -i_4 = I_{D41} + I_{D42} + \ldots + I_{D4n} = n \cdot I_o \\
i_m &= -i_{m-1} = I_{Dm1} + I_{Dm2} + \ldots + I_{Dmn} = n \cdot I_o \\
i_j &= (-1)^{j+1} \cdot (m+1-j) \cdot I_o
\end{align*}
\]

Similarly, in the positive half cycle of the input voltage source, the average current of capacitors can be obtained as given in (9).

\[
\begin{align*}
i_{i1} &= i_{i3} = 2I_o \\
i_{i2} &= i_{i3} = I_o \\
i_{i4} &= i_{i4} = -2I_o \\
i_{i2} &= i_{i2} = -I_o \\
i_{i1} &= i_{i1} = -2I_o \\
i_{i2} &= i_{i2} = -I_o \\
i_{i4} &= i_{i4} = 2I_o \\
i_{i2} &= i_{i2} = I_o
\end{align*}
\]

While the proposed MIVM with \( m \) input-terminal and \( n \) VM cells, the average current of the input-terminals and capacitors can be obtained in (10)-(13).

In the positive half cycle of the input voltage source:

\[
\begin{align*}
i_1 &= -i_2 = I_{D21} + I_{D22} + \ldots + I_{D2n} = n \cdot I_o \\
i_3 &= -i_4 = I_{D41} + I_{D42} + \ldots + I_{D4n} = n \cdot I_o \\
i_m &= -i_{m-1} = I_{Dm1} + I_{Dm2} + \ldots + I_{Dmn} = n \cdot I_o \\
i_j &= (-1)^{j+1} \cdot (n+1-j) \cdot I_o
\end{align*}
\]

In the negative half cycle of the input voltage source:

\[
\begin{align*}
i_1 &= -i_m = -I_{D11} - I_{D12} - \ldots - I_{D2n} = -n \cdot I_o \\
i_3 &= -i_4 = -I_{D41} - I_{D42} - \ldots - I_{D4n} = -n \cdot I_o \\
i_m &= -i_{m-2} = -I_{D(m-1)1} - I_{D(m-1)2} - \ldots - I_{D(m-1)n} = -n \cdot I_o \\
i_j &= (-1)^j \cdot (n+1-j) \cdot I_o
\end{align*}
\]

where \( i \in \{1, \ldots, m\} \), \( j \in \{1, \ldots, n\} \).

### B. Voltage Gain Analysis

From table I, the output voltage can be obtained as:

\[
u_o = u_{d1} + u_{d2} = 8U_m - 15\Delta u_{cm}
\]

While the proposed MIVM with \( m \) input-terminal and \( n \) cells, the peak voltage across capacitors in the MIVM and the output voltage can be obtained by (15).

\[
\begin{align*}
u_{i1,\text{max}} &= i \cdot U_m - (i-1) \cdot \Delta u_{cm} \\
u_{ij,\text{max}} &= m \cdot U_m - \left\{ \frac{(2n-j+2)(j-1)(m-1)}{2} + (i-1)(n-j+1) \right\} \cdot \Delta u_{cm} \\
u_o &= mn \cdot U_m - \frac{(m-1)n(n+1)(2n+1)\Delta u_{cm}}{6}
\end{align*}
\]

### C. Voltage Stress of Diodes

As shown in Fig. 5, the voltage stresses of \( D_{11}, D_{11}, D_{12} \) and \( D_{32} \) reach their peak values at \( t_0 \), and the voltage stresses of \( D_{21}, D_{41}, D_{22} \) and \( D_{42} \) reach their peak values at \( t_{10} \). These peak values are denoted as \( u_{\text{vp}D_{11}}, u_{\text{vp}D_{21}}, u_{\text{vp}D_{31}}, u_{\text{vp}D_{41}}, u_{\text{vp}D_{12}}, u_{\text{vp}D_{22}}, u_{\text{vp}D_{32}} \) and \( u_{\text{vp}D_{42}} \) respectively:

\[
\begin{align*}
u_{\text{vp}D_{11}} &= 2U_o - 2\Delta u_{cm} \\
u_{\text{vp}D_{21}} &= u_{\text{vp}D_{31}} = 2U_m - 4\Delta u_{cm} \\
u_{\text{vp}D_{12}} &= u_{\text{vp}D_{42}} = 2U_m - 3\Delta u_{cm} \\
u_{\text{vp}D_{22}} &= u_{\text{vp}D_{32}} = 2U_m - 6\Delta u_{cm}
\end{align*}
\]

Generalizing above analysis to the circuit with \( m \) input-terminal and \( n \) VM cells yields the expressions of the peak values of \( D_{ij} \), i.e.

\[
\begin{align*}
u_{\text{vp}D_{ij}} &= u_{\text{vp}D_{mn}} = 2U_m - \left\{ \frac{(2n-j+1) \cdot j \cdot \Delta u_{cm}}{2} \right\} \\
u_{\text{vp}D_{ij}} &= 2 \cdot U_m - (2n-j+1) \cdot j \cdot \Delta u_{cm}, (i \neq 1, m; j \neq n)
\end{align*}
\]

### D. Comparison of the Proposed MIVM with Traditional CW-VM and D-VM

To simplify the comparison, all the results in Table II are presented without considering the influence of voltage ripple on capacitors. Traditional CW-VM and D-VM circuits can achieve high voltage conversion gain by increasing the number of basic VM cells. However, with the increase of VM cells, the current stress of capacitors in CW-VM circuit is increased (which will also affect the voltage conversion gain) and the voltage stress of capacitors in D-VM circuit is increased. For a given voltage conversion ratio, by adjusting the number of input-terminals, the proposed MIVM circuit can achieve a relatively lower current stress of capacitors than CW-VM circuit and a relatively lower voltage stress of capacitors than D-VM circuit. Obviously, the proposed MIVM has better design flexibility than traditional CW-VM and D-VM circuits. Moreover, it is also an important addition to the existing VM circuit family.

![Fig. 6. Combination of the Proposed MIVM and Boost converter.](image-url)
**TABLE II**

**COMPARISON OF THE PROPOSED MIVM WITH TRADITIONAL CW-VM AND D-VM.**

| Topology | Proposed MIVM | CW-VM | D-VM |
|----------|---------------|-------|------|
| Average current of capacitors during half period | \(i_{cij} = (n - j + 1) \cdot I_o\) | \(i_{cij} = \frac{(n - j + 2) \cdot I_o}{2}\), \(j\) is odd | \(i_{cij} = \frac{(n - j + 1) \cdot I_o}{2}\), \(j\) is even |
| Voltage stress of capacitors | \(u_{vpci,m} = i \cdot U_m\) | \(u_{vpci,m} = U_m\) | \(u_{vpci,m} = j \cdot U_m\) |
| Average current of diodes | \(I_o\) | \(I_o\) | \(I_o\) |
| Voltage stress of diodes | \(2U_m\) | \(2U_m\) | \(2U_m\) |
| Maximum output voltage | \(mnU_m\) | \(nU_m\) | \(nU_m\) |
| The number of diodes | \(mn\) | \(n\) | \(n\) |
| The number of capacitors | \(mn\) | \(n\) | \(n\) |

Note: the results in Table I are given under the following conditions: all devices are ideal, and ignoring the influence of voltage ripple on capacitors.

The corresponding circuit topology is shown in Fig. 6. By changing the number of input-phases of the converter proposed in Fig. 6, the current stress of the devices can be adjusted for different design requirements. Apparently, compared to the high step-up dc/dc converters with traditional D-VM and CW-VM circuits in [9-13], the design flexibility of the converter with the proposed MIVM is better. Detailed theoretical analysis and experimental results of the converter in Fig. 6 can be obtained in [25, 29].

**IV. EXPERIMENTAL RESULTS**

In order to verify the results derived from the presented theoretical analysis in section II and III, an experimental prototype of the proposed MIVM has been built and the specifications of this experimental prototype are given in Table III. Fig. 7 shows the test platform and experimental prototype.

**TABLE III**

**SPECIFICATIONS OF THE EXPERIMENTAL PROTOTYPE.**

| Parameter | Value |
|-----------|-------|
| Input voltage (peak) and frequency | 100V/1 kHz |
| Number of input phases and cells | \(m=4, n=2\) |
| Diodes | IDT12S60C |
| Capacitors in MIVMs | 10μF |
| Capacitors connected with load | 50μF |
| Load resistance | 6400Ω |

Experimental waveforms are shown in Fig. 8. The voltage waveforms across VM capacitors are shown in Figs. 8(a) and (b), and the RMS value of these voltages are: \(u_{c11} = 90.64V\), \(u_{c21} = 171.7V\), \(u_{c31} = 252.5V\), \(u_{c41} = 341.5V\), \(u_{c12} = 340.9V\), \(u_{c22} = 332.4V\), \(u_{c32} = 322.8V\), \(u_{c42} = 319V\). The voltage ripples of these capacitors are shown in Figs. 8(d) and (e), and \(\Delta u_{v_{vm}} = 9.2V\). It can be verified that the above measurements are consistent with that calculated using Table I. The waveform of the output voltage is shown in Fig. 8(e) and \(u_o = 658.6V\), and again it is consistent with that calculated from (14).

Fig. 7. Test platform and experimental prototype.
The proposed MIVM can be combined with the conventional VMs, optimized for various applications. Like the conventional VMs, the MIVM enjoys better design flexibility as the number of its input terminals can be increased. The accuracy of the theoretical analysis and the effectiveness of the proposed MIVM circuit have been verified experimentally.

V. CONCLUSION

A multi-input-terminal voltage multiplier (MIVM) circuit is proposed in this paper. Compared to the existing VM circuits, the MIVM enjoys better design flexibility as the number of its input terminals can be adjusted. As such, not only the voltage stress but also the current stress of the capacitors can be optimized for various applications. Like the conventional VMs, the proposed MIVM can be combined with the conventional dc/dc converters such as boost converter. Compared to the existing high step-up dc/dc converters that consist of VM and boost converter, not only the voltage conversion ratio and voltage stresses on devices are improved, but also the current stresses on switches and inductors can be decreased by selecting a greater number of input terminals.

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