Characterization of Oxide Trapping in SiC MOSFETs Under Positive Gate Bias

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This work was supported in part by the Suzhou Science and Technology program under Grant SYG201923; in part by the Key Program Special Fund in Xi’an Jiaotong-Liverpool University (XJTLU) under Grant KSF-T-07; and in part by XJTLU Research Development Fund under Grant PGRS1912003 and Grant RDF-20-02-62.

ABSTRACT SiC MOSFETs devices with double-trench dominate the market due to their low on-resistance. However, studies on its temperature-dependent properties are not comprehensive. This work uses fast I-V and static I-V techniques to explore the location of electrons trapped in the device under moderate gate stress. Threshold voltage instability ($V_{TH}$ hysteresis and $\Delta V_{TH}$) and on-resistance degradation ($\Delta R_{ON}$) are used to characterize oxide trapping. Although the observation method is different, it can be found that the $V_{TH}$ instability and $R_{ON}$ degradation increase linearly with logarithmic time over a wide time range from $100 \mu s$ to $10^4$ s, suggesting that the direct tunneling mechanism dominates the electrons trapping in the oxide near the SiO$_2$/SiC interface. The interface trap density is $3.8 \times 10^{12}$ cm$^{-2}$·eV$^{-1}$. In addition, a negative temperature dependence is shown in the test, and the fitting parameter $\gamma$ from 0.16 to 0.18 indicated that these traps are concentrated in the oxide layer. These traps’ energy level at 0.68 eV below the conduction band was obtained in the recovery phase through the Arrhenius plot.

INDEX TERMS Activation energy, fast I-V technique, MOSFETs, on-resistance degradation, positive-bias stress, silicon carbide, static I-V technique, threshold voltage instability.

I. INTRODUCTION

Silicon carbide (SiC) is considered a promising wide bandgap semiconductor material to supersede silicon for developing high-efficiency, high-power, and high-temperature electron devices [1]. In particular, SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) are expected to meet the growing demand for electrical power generation, distribution, and switching due to their high breakdown voltage, low conduction, and low switching loss capabilities [2], [3].

Studying the positive gate stress of SiC MOSFETs is crucial to circuit design. For example, SiC MOSFET is usually used as the DC circuit breaker in protection circuits, gated on for prolonged periods. The changed threshold voltage ($V_{TH}$) under positive gate bias would cause a response time delay of the faulty system [4]. $V_{TH}$ instability is generally characterized by threshold voltage shifts ($\Delta V_{TH}$) and hysteresis ($V_{TH}$ hysteresis). Besides the $V_{TH}$, the on-state drain-to-source resistance ($R_{DS(ON)}$ or $R_{ON}$) is an important parameter related to power loss.

Semiconductor manufacturers enthusiastically research device structures and optimize gate oxide to restrict $V_{TH}$ instability and alleviate the $R_{ON}$ degradation [4], [5], [6], [7]. Several papers have investigated the negative or positive temperature dependence of $V_{TH}$ instability and $R_{ON}$ degradation in planar structures [3], [8], [9], [10], yet few studies on the trap level of devices [8]. Meanwhile, very little is known about trench gate structure [7], [11]. Although some articles have observed that trench gate structures had larger $V_{TH}$
instability than planar gate structures under the same gate bias [12], [13]. Double trench devices dominate the market due to their low on-resistance. However, there is still a research gap on the temperature-dependent properties of the double trench structure. In this work, fast I-V and static I-V methods are used to investigate the \( V_{TH} \) instability and \( R_{ON} \) degradation over a wide time range from 100 \( \mu \)s to 10\(^5\) s under moderate stress voltages. The trap level and their distribution are analyzed and calculated. These results may help manufacturers to optimize the gate oxidation process and improve the threshold voltage stability of the device.

The organization of this article is shown below. Section II investigates the \( V_{TH} \) hysteresis and \( R_{ON} \) degradation with different ramp speeds, gate stress voltages, and stress times using the fast I-V technique. Section III investigates the device degradation under gate stress at high temperatures over a broad time scale using the static I-V technique. Section IV is the conclusion part.

II. FAST I-V EXPERIMENTAL PROCEDURE AND TEST RESULTS

The SiC MOSFETs studied in this work came from leading commercial manufacturers. From its datasheet, the device has a breakdown voltage of 1200 V and \( R_{DS(on)} \) of 105 m\( \Omega \), measured at \( V_{GS} \) = 18 V and \( I_D \) = 7.6 A at room temperature. The simplified structure of SiC MOSFETs with double trench is shown in Fig. 1. According to their technical report, the source trenches can effectively disperse the electric field at the bottom of the gate trench [14].

Fast I-V measurement relied on a parameter analyzer system involving Agilent DSO-X 2024A digital oscilloscope, Agilent E3647 DC power supply, Rigol DG 2041A pulse generator, and computer control program [15], [16]. A schematic experiment setup for fast I-V measurement is shown in Fig. 2 (a). Changeable square pulses were applied to the gate terminal of the devices under test (DUTs). The load resistance \( (R_L) \) of 10 \( \Omega \) was carefully selected for limiting resonance and a low off-state current. During DUT’s switching along the load line, the voltage waveforms of the gate \( (V_{GS(i)}) \) and drain \( (V_{DS(i)}) \) terminals were simultaneously recorded by the digital oscilloscope with the sampling rate of 50 M/s, as exhibited in Fig. 2 (b). A small \( V_{DD} \) of 0.5 V was selected to eliminate the current collapse and hot-electron effect [16]. It is worth mentioning that before the test, all terminals of the DUTs were grounded for 1 min to achieve a steady state by releasing the charges initially trapped in the MOS interface and oxide bulk. After the up-and-down ramping of each pulse, all terminals of the DUTs were grounded for 10 s to release the trapped charges to restore their initial state.

According to the schematic, time-dependent drain current \( I_D(t) \) and drain-to-source resistance \( R_{DS(i)} \) could be calculated using the following equations:

\[
I_D(t) = \frac{V_{DD} - V_{DS(i)}}{R_L} \tag{1}
\]

\[
R_{DS(i)} = \frac{V_{DS(i)} \cdot R_L}{V_{DD} - V_{DS(i)}} \tag{2}
\]

The calculated up (solid line)-/down (dotted line) ramp \( I_D(V_{GS}) \) and \( R_{DS} - V_{GS} \) curves are shown in Fig. 3 (a) and (b). In Fig. 3 (a), The \( V_{TH} \) hysteresis (pink-dotted-line) is defined as the gate voltage difference read at the up/down ramps when the drain voltage \( (V_{DS(i)}) \) is 0.3 V [17]. In Fig. 3 (b), \( R_{ON} \) is defined as the value of \( R_{DS} \) when \( V_{GS} = 6 \) V. \( \Delta R_{ON} \) is defined as the ratio of \( R_{ON} \) on the down-ramp to \( R_{ON} \) on the up-ramp [17].

It can be seen from Fig. 4 (a) and (b) that the ramping time \( t_{1/2} \) greatly influences the extraction of threshold voltage hysteresis and on-resistance. In Fig. 4 (c), the \( V_{GS} \) and on-resistances extracted from the up-ramp shift to the left as the ramp speed becomes faster. Furthermore, it was observed that the \( V_{GS} \) and on-resistances extracted by the down-ramp shift towards the right direction as the ramp speed become faster. Fig. 4 (d) shows that the \( V_{TH} \) hysteresis and \( \Delta R_{ON} \) increase with faster ramp speed. Moreover, a strong correlation between threshold voltage and on-resistance can be observed [7].

In the ramp region, the slow ramp speed will change the charge state close to the MOS interface. In this case,
FIGURE 3. (a): calculated \( I_D - V_{GS} \) curves at up-/down ramps. The ramp time \( t_r/f \) is 10 \( \mu \)s. (b): calculated \( R_{DS} - V_{GS} \) curves at up-/down ramps.

FIGURE 4. (a): \( I_D - V_{GS} \) and (b): \( R_{DS} - V_{GS} \) curves at different ramping times. (c): \( V_{GS} \) and \( R_{ON} \) extracted by up-/down-ramp (d): \( V_{TH} \) hysteresis and \( \Delta R_{ON} \) with different ramping times.

FIGURE 5. (a): \( I_D - V_{GS} \) and (b): \( R_{DS} - V_{GS} \) curves under different gate stresses. (c): \( V_{GS} \) and \( R_{ON} \) were extracted by up-/down-ramps under different gate stresses. (d): observed \( V_{TH} \) hysteresis and \( \Delta R_{ON} \) under different gate stresses.

The threshold voltage hysteresis is usually underestimated. In other words, faster ramp speed allows for more accurate observation of oxide traps near the interface because less charge state changes during the test [5], [6], [15], [18], and [19].

To achieve acceptable threshold voltage and transconductance, the gate oxide in SiC MOSFETs is usually thinner than its Si counterparts. However, it will lead to more severe degradation in the gate oxide because a higher electric field is applied [4], [18]. The gate stress voltage significantly influences the threshold voltage hysteresis and on-resistance, as shown in Fig. 5. In Fig. 5 (a), the \( V_{TH} \) hysteresis is more pronounced at larger stress voltages than at smaller stress voltages. In Fig. 5 (b), the degeneration of on-resistance is in the same pattern. It is further confirmed in Fig. 5 (c), where extracted \( V_{GS} \) and \( R_{ON} \) did not change significantly during the up-ramps with increasing gate stress compared with the down-ramps. This is because more oxide defects are filled at higher voltages. Fig. 5 (d) shows the \( V_{TH} \) hysteresis and \( \Delta R_{ON} \) observed under different gate biases using the fast I-V method.

Depending on the results in Fig. 4 and 5, an up-/down-ramp speed of 100 \( \mu \)s and moderate gate stress of 7 V is selected for the following short-term stress test. In Fig. 6, \( V_{TH} \), hysteresis, \( \Delta R_{ON} \), and maximum transconductance changes (\( \Delta G_{m,max}\% \)) are monitored during the 1 s stress time. The \( G_{m,max} \) is defined as the maximum value of \( \Delta I_D/\Delta V_{GS} \). The degradation of transconductance \( \Delta G_{m,max}\% \) is defined as the percentage of the \( G_{m,max} \) difference read at the up/down ramps divided by the \( G_{m,max} \) value of up-ramps.

Fig. 6 (a) and (b) show that \( V_{TH} \) hysteresis and \( R_{ON} \) degradation increase with stress time. In Fig. 6 (c), the extracted \( V_{GS} \), \( R_{ON} \), and \( G_{m,max} \) did not change significantly on the up-ramps but changed greatly with increasing stress time on the down-ramps. Fig. 6 (d) shows that \( V_{TH} \) hysteresis and \( \Delta R_{ON} \) increase linearly with logarithmic time [2], [6], [20], [21], [22], and the transconductance degradation \( \Delta G_{m,max}\% \) also increases with stress time.

Based on the direct tunneling model of charge transfer into MOS devices, it is assumed that the traps are randomly distributed in the oxide. The total charge transferred into the oxide trap follows a logarithmic time dependence [18], [23].
as described by the following equation:

\[ Q_{\text{NIOT}} \approx eN \left( \frac{t}{t_0} + \frac{\zeta}{2\beta} \ln \frac{t}{t_0} \right) \]  

(3)

Where \( Q_{\text{NIOT}} \) is the charge states in the near-interfacial oxide traps, \( N \) is oxide trap density, \( e \) is the electronic charge, \( \beta \) is the tunneling parameter, \( t_0 \) is the initial tunneling transition time, and \( \zeta \) is the Euler’s constant. It can be seen from the equation that trapped charge states increase linearly concerning the logarithm of stress time, which is consistent with the results shown in Fig. 6 (d).

It is suggested that the \( V_{\text{TH}} \) hysteresis and \( \Delta R_{\text{ON}} \) are attributed to the direct tunneling of channel electrons into as-grown oxide traps near the interface within 1 s bias time [6], [21]. As shown in Fig. 6 (c) and (d), the decrease in transconductance with stress time is more pronounced since transconductance is related to bulk traps in the oxide layer [24].

It can be predicted that more electrons would be trapped into the deeper oxide defects as stress time increases, causing more significant \( V_{\text{TH}} \) hysteresis and \( \Delta R_{\text{ON}} \).

### III. STATIC I-V EXPERIMENTAL PROCEDURE AND TEST RESULTS

In the previous section, we discussed the \( V_{\text{TH}} \) hysteresis and \( \Delta R_{\text{ON}} \) under short-term stress within 1 s; in this section, we will discuss the \( \Delta V_{\text{TH}} \) and \( \Delta R_{\text{ON}} \) under long-term stress within \( 10^4 \) s. The static I-V technique uses the measure-stress-measure (MSM) process, as illustrated in Fig. 7 (a). The MSM procedure consists of four steps: initial stabilization, I-V reference curves measurement, multiple stress-sense measurement, and recovery-sense measurement. The schematic experiment setup for static I-V measurement is shown in Fig. 7 (b). Due to the pulse width limitation of the pulse generator in the fast I-V technique, the MPSMU module of Agilent B1505A is used to generate long-term pulse width for stress periods and recovery periods. The maximum current level is limited to 60 mA to protect the parameter analyzer.

At the beginning of the test, four virgin devices were initialized by all terminals being grounded for 1 min. Then the DUTs were heated to elevated temperatures for 1 hour to stabilize the device package temperature. After that, I-V reference curves at elevated environment temperatures were performed with \( V_{\text{DS}} \) from 0 V to 7 V at \( V_{\text{DS}} = 0.1 \) V by Agilent B1505A, as displayed in Fig. 7 (c). The \( V_{\text{TH}} \) is defined as the gate voltage when the drain current reaches 0.1 mA. There are three temperature ranges from room temperature to 75 °C, to 100 °C, to 125 °C. Threshold voltage shifts are defined herein as the difference between the threshold voltage at different temperatures and the room temperature threshold voltage. It can be observed that in
For 10^4 alleviated Coulomb scattering effect [3], [26], [28], [29]. The threshold swing decreases at high temperatures due to the
from 1.31 \times 10^{11} to 2.41 \times 10^{11} with temperature from 25 °C to 125 °C, which is caused by the massive electron emission from the interface traps [25] and [27]. In Fig. 7 (d), the sub-threshold swing decreases at high temperatures due to the alleviated Coulomb scattering effect [3], [26], [28], [29].

In the stress period, 7 V gate bias was applied to the DUTs for 10^4 s with other terminals grounded. The stress process was interrupted at the mean logarithmic time. Transfer characteristic curves were performed in the negative orientation (VGS from 7 V to 0 V at VDS = 0.1 V) to monitor the VTH and RON [11]. The threshold voltage instability \( \Delta V_{TH} \) is defined as the difference in VTH before and after stress.

In the recovery period, the gate voltage of 0 V was applied to the DUTs for 10^4 s with other terminals grounded to release electrons that had been trapped in the MOS interface and bulk defects.

To obtain the capture/emission time constant and describe the distribution of defects in the oxide layer, the \( \Delta V_{TH} \) data in Fig. 8 (a) and (b) are fitted with the stretched exponential functions by using the following Equations (4) and (5), with the high R-square values between 0.95 to 0.99 (dash fitted line) [3], [26], [27].

\[
V_{TH\ hys(s)} = V_{TH\ hys(max)} \left[ 1 - \exp\left( -\frac{t_s}{\tau_s} \right)^{\gamma} \right] \tag{4}
\]

\[
V_{TH\ hys(r)} = V_{TH\ hys(ts,0)} \exp\left( -\frac{t_r}{\tau_r} \right)^{\gamma} \tag{5}
\]

\( V_{TH\ hys(max)} \) is related to the total trap density, \( V_{TH\ hys(ts,0)} \) is the non-recovered \( V_{TH\ hys} \) value, \( \gamma \) is related to the trap energy distribution, \( t_s/t_r \) is stress/recovery time, and \( \tau_s/\tau_r \) is the time constant of stress/recovery periods.

It can be found in Fig. 8 (a) that the time constant \( \tau_s \) increases from 10^3 to 10^2 as the temperature increases, leading to a negative activation energy of -0.52 eV, extracted in Fig. 10 (a). This may explain why the \( \Delta V_{TH} \) decreases with the elevated temperature, the same phenomenon observed in [3], [11]. In other words, during the high-temperature stress phase, the de-trapping is even more thermally activated than the trapping, caused by the emission time constant being shorter than their associated capture time [11].

In Fig. 8 (b), after removing the gate bias, we found the de-trapping in the recovery phase is accelerated by high temperatures, with the time constant \( \tau_r \) dropping from 10^9 s to 10^2 s with increased temperatures, leading to a trap level at 0.68 eV activation energy, extracted by Fig. 10 (b) in the Arrhenius plot.

Moreover, the trap energy distribution shows consistency in the stress and recovery phases, with the parameter \( \gamma \) from 0.16 to 0.18, as shown in Fig. 8 (a) and (b). This indicates that the trap energy distribution is concentrated in the gate oxide [3].

We also found that the \( \Delta V_{TH} \) increases linearly with logarithmic time (solid fitted line), the same as in Fig. 6 (d). It is suggested that channel electrons are trapped in the oxide defects near the interface [30], [31], [32].

In Fig. 9, the interface trap density \( D_{it} \) at room temperature is calculated by I-V subthreshold method [33], [34], [35]. The \( D_{it} \) increases exponentially near the conduction band edge. \( E_{CS} \) is the potential of the conduction band surface, and \( E_{t0} \) is the surface potential related to the trap level. At the \( E_{CS} - E_{T0} = 0.1 \) eV, the \( D_{it} \) is 3.8 \times 10^{12} cm^{-2} eV^{-1}.

The time evolution of \( \Delta R_{ON} \) during the stress and recovery process are shown in Fig. 11 (a) and (b), respectively. It can be found that the \( \Delta R_{ON} \) decreases with elevated temperature, which is consistent with the \( \Delta V_{TH} \) tendency in Fig. 8 (a). The \( \Delta R_{ON} \) also fits well with the stretched
TABLE 1. Interface trap density of SiC MOSFETs.

| Device        | Measurement method                  | Interface trap density $D_{iT}$ (cm$^{-2}$·eV$^{-1}$) | Ref. |
|---------------|-------------------------------------|------------------------------------------------------|------|
| Planar        | L-V subthreshold characteristics   | $5.8 \times 10^{-2}$                                 | [34]|
|               |                                     | $6.8 \times 10^{-2}$                                 |      |
|               |                                     | $9.3 \times 10^{-2}$                                 |      |
|               |                                     | $2 \times 10^{-13}$                                  | [33]|
| Unknown       |                                     | $5.4 \times 10^{-12}$                                | [35]|
| Planar        | C-V high-frequency characteristics  | $2.5 \times 10^{-12}$                                | [36]|
|               |                                     | $10^{-13}$                                            | [37]|
|               |                                     | $5 \times 10^{-11}$                                  | [38]|

TABLE 2. Trap level of commercial SiC MOSFETs.

| Device       | Methods                | Bias (V) | $T_s$(s) | $T_r$(s) | Trap level (eV) | Ref. |
|--------------|------------------------|----------|----------|----------|-----------------|------|
| Planar       | AC stress (10 kHz)     | 25       | $10^4$-$10^6$ | $1.2$ (stress) | [8] |
| Planar       | Cyclic gate bias       | 30       | $2 \times 10^8$ | $0.1$ (stress) | [39]|
| Unk.         | DC stress              | 15-20    | $10^{-13}$ | $1.04$-$1.14$ (stress) | [6] |
| Unk.         | Double ramp            | 15       | $5 \times 10^4$ | $10^4$-$10^5$ | $0.3$ (recovery) | [40]|
| Double-trench| DC stress              | 7        | $10^4$-$10^6$ | $10^4$-$10^5$ | $0.68$ (recovery) | This work|

IV. CONCLUSION

This work uses fast I-V and static I-V techniques to explore the oxide trapping mechanism under positive gate bias in the double-trench SiC MOSFETs.

By monitoring $V_{TH}$ hysteresis and $\Delta R_{ON}$ within 1 s stress time using the fast I-V technique, it was found that these two parameters are affected by ramp speed, bias voltage, and stress time. By monitoring the $\Delta V_{TH}$ and $\Delta R_{ON}$ within $10^4$ stress time using the static I-V technique, it was found that the $\Delta V_{TH}$ and $\Delta R_{ON}$ decreased with increasing temperature due to the activated de-trapping effect. Moreover, during the $10^4$ recovery time, the trap level at 0.68 eV below the conduction band is obtained, and these recoverable trap sites are concentrated in the oxide layer.

Although the observation method is different, it can be found that the instability of the threshold voltage and on-resistance increases linearly with logarithmic time regardless of the long or short stress time, indicating that direct tunneling dominates the electrons trapping in oxide near the interface. The interface trap density is $3.8 \times 10^{12}$ cm$^{-2}$·eV$^{-1}$.

Comparisons of $D_0$ and $E_a$ between the SiC MOSFETs with different structures are shown in Tables 1 and 2, respectively.

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