Here, we demonstrate the fabrication of a Cu-graphene heterostructure interconnect by the direct synthesis of graphene on a Cu interconnect with an enhanced performance. Multilayer graphene films were synthesized on Cu interconnect patterns using a liquid benzene or pyridine source at 400 °C by atmospheric pressure chemical vapor deposition (APCVD). The graphene-capped Cu interconnects showed lower resistivity, higher breakdown current density, and improved reliability compared with those of pure Cu interconnects. In addition, an increase in the carrier density of graphene by doping drastically enhanced the reliability of the graphene-capped interconnect with a mean time to failure of >10⁶ s at 100 °C under a continuous DC stress of 3 MA cm⁻². Furthermore, the graphene-capped Cu heterostructure exhibited enhanced electrical properties and reliability even if it was a damascene-patterned structure, which indicates compatibility with practical applications such as next-generation interconnect materials in CMOS back-end-of-line (BEOL).
RESULTS

Fabrication of Cu/Graphene heterostructure interconnects

We implemented oxygen-free APCVD at 400 °C using benzene and pyridine carbon sources to directly integrate multilayer graphene film into Cu interconnects. The types of interconnects with their components and synthesis conditions of graphene have been described (Supplementary Fig. 1) 13,14. Optical micrograph and scanning electron microscopy (SEM) images show that the Cu interconnect remained physically intact without any change in surface morphology (e.g., pore or dewetting regions), because the low-temperature process prevented thermal damage to the Cu (Fig. 1a and Supplementary Fig. 2). In addition, Cu grain size in interconnects was expanded by thermal annealing during the graphene synthesis process, which improved the electrical properties of the Cu interconnect (Supplementary Fig. 2). The schematic in Fig. 1a shows the Cu-graphene heterostructure formed by low-temperature CVD. Graphitic films on the surfaces of the Cu interconnect were observed in high-resolution transmission electron microscopy (HRTEM) images (Fig. 1b). Uniform multilayer graphene films were synthesized on the top, left, and right sides of the Cu interconnect (Fig. 1b). The thickness of the graphene films grown for 120 min was ~7 nm with the number of layers ranging from 20 to 22. Hence, this low-temperature CVD process is suitable for the fabrication of Cu-graphene heterostructure interconnects.

Representative graphene peaks such as the G and 2D bands were observed in the Raman spectra of the Cu/Graphene and Cu/N-graphene interconnects. Furthermore, an 2D/G of less than 0.5 with a broad 2D peak depicted the formation of a multilayer graphene film, which is consistent with the TEM images (Fig. 1c). The full-width at half-maximum (FWHM) of the 2D peak of undoped graphene and N-doped graphene synthesized using APCVD, which indicate a randomly rotated structure of c-axis, were ~62.9 and ~64.3, respectively. These values are lower than those of a graphene layer grown via ECR-CVD (~90.9) 10, graphene via PECVD (~71.1) 11, and amorphous carbon via ICP-CVD (~153.5) 12, which demonstrates the formation of higher crystalline graphene films layer on Cu interconnects (Supplementary Fig. 3) 15. By contrast, no graphene was detected in the as-fabricated Cu and annealed Cu interconnects, and the SiO2 region of substrate after graphene synthesis. This suggests the possibility that graphitic film formed during annealing can be excluded; it also suggests that annealing is only helpful in the synthesis of a uniform multilayer graphene film and in the improvement of the electrical properties of the Cu interconnect by increasing the grain size of the Cu surface 16. Hence, multilayer graphene films were selectively synthesized on Cu interconnect surfaces in the growth step of CVD at 400 °C (Fig. 1c). In addition, because the integration of CVD-grown graphene films is used in this study, uniform, inch-scale Cu-graphene heterostructure interconnects can be fabricated on one substrate. The Raman spectra of graphene measured in randomly selected Cu interconnects in nine different regions of a wafer (area of 1 inch²) exhibited excellent uniformity, which is...
significant for realizing large-area Cu-graphene-based interconnects (Supplementary Fig. 4).

Graphene synthesis on Cu interconnects via APCVD enables the thickness control of the graphitic coating layer as a function of the synthesis time. For a short synthesis time of 30 min, a thin graphene film of ~1.5 nm was formed on the Cu interconnects and the thickness of the graphitic film proportionally increased to ~7.35 nm as the synthesis time increased. The formation of continuous multilayer graphene films ranging from 4 to 21 layers grown for 30–120 min was observed in TEM images (Fig. 1d and Supplementary Fig. 5). Generally, the synthesis of graphene on Cu foil via LPCVD results in the formation of a monolayer graphene film as a result of the self-limiting effect of Cu induced by the low solubility of carbon. By contrast, for Cu interconnects fabricated by sputtering and annealing, it is possible for numerous nuclei of graphene to be initiated and a larger amount of carbon atoms to be absorbed on polycrystalline Cu, leading to the formation of multilayer graphene.

To compare the crystallinity of Cu, X-ray diffraction (XRD) patterns of the Cu foil and Cu interconnect were acquired. XRD revealed only a majority (111) grain orientation in the Cu foil, which may be responsible for the formation of the single-layer graphene owing to the low solubility of carbon in Cu. Meanwhile, the XRD patterns of polycrystalline Cu interconnect show major (111) and minor (200) grain orientations (Supplementary Fig. 6a). The HRTEM image of Cu foil reveals the presence of (111) lattice fringes with no grain boundaries. In addition, in the accompanying selected area electron diffraction (SAED) patterns, the ordered array of the clear bright diffraction spots indicates that the Cu foil is a single crystal with a face-centered cubic (FCC) structure (Supplementary Fig. 6b). By contrast, HRTEM image and SAED patterns of the Cu interconnect show the different orientations of atomic arrangements with grain boundaries and mix-ordered patterns, indicating polycrystalline Cu with numerous defects such as point defects and grain boundaries, which act as nucleation sites for graphene, owing to which multilayer graphene films were achieved (Supplementary Fig. 6c).

Furthermore, we synthesized an N-doped multilayer graphene film using pyridine at 400 °C to improve the electrical properties of interconnects by the doping effect. For comparison with the undoped-graphene-capping layer, the N-doped graphene film was synthesized with a similar thickness of graphene being grown on Cu/Graphene interconnects. In the TEM image, the thickness of the N-doped graphene film was confirmed to be ~7 nm with the number of layers being 20 (Fig. 2a). In addition, the presence of nitrogen was observed in electron energy loss spectroscopy (EELS) mapping. Red spots denoting nitrogen atoms are distributed over the entire graphene film, demonstrating the uniform doping of nitrogen atoms in graphene. The amount of nitrogen was estimated to be ~2.32 at.% based on atomic analysis of the EELS mapping data (Fig. 2b).

X-ray photoelectron spectroscopy (XPS) of the N-doped graphene was performed to detect the nitrogen in graphene. The survey spectrum of N-doped graphene showed carbon and nitrogen bonding peaks located at approximately 285 and 400 eV, respectively. The N 1s spectrum showed three nitrogen bonding components located at 398.0 (blue line), 400.9 (red line), and 402.5 eV (olive line), corresponding to pyridinic, graphitic, and oxidized nitrogen, respectively (Fig. 2c). By contrast, XPS data obtained for the undoped graphene grown using benzene showed carbon bonding peaks without any nitrogen (Supplementary Fig. 7). Therefore, the presence of nitrogen in graphene obtained from pyridine was confirmed. XPS quantitative analysis reveals that the amount of nitrogen in graphene was ~2.11 at.%, consistent with the EELS results. Raman spectroscopy of the pyridine-derived graphene was conducted to confirm the nitrogen doping effect in comparison with the undoped graphene because the positions of representative peaks such as G and 2D bands in Raman spectra shifted owing to electron or hole doping. Raman mapping analysis of pyridine-derived graphene film exhibited a G peak with a higher wavenumber and a 2D peak with a lower wavenumber as compared with those of undoped graphene, which is consistent with previous studies (Fig. 2d and Supplementary Fig. 8). Hence, the formation of a large-area, N-doped multilayer graphene film was demonstrated.

**Electrical properties of graphene-capped Cu interconnects**

The performance of graphene-capped Cu interconnects fabricated by the direct growth of graphene on Cu interconnects at 400 °C via APCVD was characterized and compared with Si3N4-capped Cu interconnects (Cu/Si3N4) without graphene to demonstrate the advantages of graphene. The annealed Cu interconnects showed
A resistivity ($\rho$) of 9.58 ± 0.12 $\mu$Ω cm and breakdown current density ($J_{BR}$) of 20.2 ± 0.7 MA cm$^{-2}$, which were superior to those of the as-fabricated Cu interconnect. The primary reason for this was the decrease in grain boundary scattering owing to increased grain size (Supplementary Fig. 2)\textsuperscript{11,24}. The integration of low-resistivity graphene on a Cu interconnect (Cu/Graphene) enhanced its performance. In addition, the $J_{BR}$ of the Cu/Graphene interconnect increased with the thickness of graphene and saturated up to ~7 nm (Supplementary Fig. 9)\textsuperscript{10}. A noticeable performance improvement was observed wherein $\rho$ was reduced to 9.29 ± 0.07 $\mu$Ω cm and $J_{BR}$ increased up to 23.3 ± 0.4 MA cm$^{-2}$ for the 7-nm-thick graphene heterostructure Cu interconnects (Fig. 3a and Supplementary Fig. 10a). By contrast, the insulating capping layer did not influence the electrical properties of Cu interconnects significantly. The Cu/Si$_3$N$_4$ interconnects showed a $\rho$ of 9.62 ± 0.13 $\mu$Ω cm and a $J_{BR}$ of 20.5 ± 0.8 MA cm$^{-2}$, similar to those of the Cu interconnects (Fig. 3a and Supplementary Fig. 10a). This demonstrated that the integration of a metallic graphene-capping layer with interconnects using the direct synthesis of graphene provides low-resistance and fast-current pathways as well as improvement of Cu crystal structure, leading to performance enhancement achieved in the form of a 3.1% increase in $\rho$ and 14.8% increase in $J_{BR}$ as compared with the pure Cu counterpart\textsuperscript{10,11,24}. The performance of graphene-capped Cu interconnects was further improved by doping with graphene. Pyridine-derived N-doped graphene exhibits a lower resistivity than that of benzene-derived undoped graphene because of a higher charge carrier density in graphene induced by additional electrons\textsuperscript{14,17}. Hence, Cu/N-graphene interconnects showed the lowest $\rho$ (9.25 ± 0.07 $\mu$Ω cm) and highest $J_{BR}$ (25.2 ± 0.4 MA cm$^{-2}$), indicating an improvement of 3.5% in $\rho$ and 24.1% in $J_{BR}$ as compared with those of the pure Cu interconnect (Fig. 3a and Supplementary Fig. 10).

The enhanced $J_{BR}$ of the graphene-capped Cu interconnects may be due to the graphene, which suppresses the EM and temperature increase in the Cu of heterostructure interconnects\textsuperscript{25}. SEM images show the void and breakdown points of the interconnects after electrical breakdown (Supplementary Fig. 11). Larger voids were observed in the graphene-capped Cu interconnects compared with those in the annealed Cu and Cu/Si$_3$N$_4$ interconnects. The breakdown of interconnects occurs as a result of elevated temperature produced by Joule heating. Hence, the higher Joule heat in Cu/Graphene and Cu/N-graphene interconnects at higher $J_{BR}$ induced a greater breakdown void. In addition, the breakdown points of the Cu/Graphene and Cu/N-graphene interconnects were shifted farther away from the electron injection contact electrode than those of the annealed Cu and the Cu/Si$_3$N$_4$ interconnects. This demonstrates that the graphene-capping layer mitigated the EM of Cu owing to an increased activation energy; these effects will be discussed later\textsuperscript{26,27}.

To gain deeper insight into the physical role of graphene in the improvement of electrical properties of graphene-capped Cu heterostructure interconnects, we calculated the resistivity of undoped and N-doped graphene film directly synthesized on Cu interconnect. Given that each graphene layer has uniform resistance and is electrically connected to the underlying Cu interconnect in parallel, the total resistivity of the heterostructure can be obtained by

\[
W_{Cu/Graphene} = \frac{t_{Cu/Graphene}}{t_{Cu/Graphene}} \cdot \frac{W_{Cu}}{P_{Cu/Graphene}} = \frac{W_{Cu}}{P_{Cu}} + \frac{t_{Cu/Graphene}}{t_{Graphene region 1}} + \frac{f_{Cu/Graphene} \cdot W_{Cu}}{P_{Graphene}} + \frac{t_{Graphene region 1}}{t_{Graphene region 3}}
\]

where $W_{Cu/Graphene} = W_{Graphene region 2} + W_{Graphene region 3}$ is the total width and $t_{Cu/Graphene} = t_{Cu} + t_{Graphene region 1}$ is the total thickness of the heterostructure. Then, the total cross-sectional area of the graphene overlayer is given by $W_{Cu/Graphene} + 2t_{Cu}f_{Graphene}$ because the thickness of graphene grown on the...
The entire Cu surface is almost uniform. Taking the 500-nm-width test Cu interconnects with 7-nm-thick graphene-capping layer as an example, where $\rho_{\text{Cu}}$ = 9.58 $\mu\Omega$ cm, $\rho_{\text{Cu/Graphene}}$ = 9.29 $\mu\Omega$ cm, and $\rho_{\text{Cu/N-graphene}}$ = 9.25 $\mu\Omega$ cm were acquired from measurements, the resistivity values of undoped and N-doped graphene layers were calculated to be 3.4 and 3.1 $\mu\Omega$ cm, respectively. This indicates that the graphene-capping layer strongly influences the electrical properties of the Cu-graphene heterostructure because $\rho_{\text{Cu/Graphene}}$ is less than $\rho_{\text{Cu}}$.

In addition, the power factor of interconnects was calculated to describe the relationship between the breakdown current density and resistivity:

$$J_{\text{max}} = A\rho^{-n}$$  

(2)

where $A$ is a fitting parameter and $n$ is a power factor. $A$ fit to the power law yielded $n$ values of 2.41 and 2.45 for annealed Cu and Cu/Si$_3$N$_4$, respectively. Surface scattering at the Cu/Si$_3$N$_4$ interface can lead to a significant degradation of interconnect performance. However, the resistivity, breakdown current density, and power factor of Cu/Si$_3$N$_4$ interconnects are similar to those of Cu interconnects, indicating that the Si$_3$N$_4$ capping layer does not affect the electrical properties of Cu interconnects$^{29}$. By contrast, the graphene-capped Cu interconnects showed lower $n$ values of 2.02 (Cu/Graphene) and 1.79 (Cu/N-graphene), indicating that the graphene-capping layer acts as the dominant current pathway in Cu-graphene heterostructures and, hence, enhances the performance of the interconnect (Fig. 3b and Supplementary Fig. 10b).

Thus, we confirmed the reliability of graphene-capped Cu interconnects by measuring the mean time to failure (MTTF) at 100 °C under a continuous DC stress of 3 and 10 MA cm$^{-2}$ and compared it with that of the Cu/Si$_3$N$_4$ interconnects because pure Cu interconnects without an oxygen barrier are readily oxidized above 100 °C (Supplementary Fig. 12)$^{30}$. The failure times for the Cu/Si$_3$N$_4$ interconnects were $\sim$200,000 s (3 MA cm$^{-2}$) and $\sim$18,000 s (10 MA cm$^{-2}$) because EM in Cu creates voids and increases the resistance of interconnects. By contrast, the undoped graphene-capped Cu interconnects had increased failure times of $\sim$400,000 s (3 MA cm$^{-2}$) and $\sim$74,000 s (10 MA cm$^{-2}$). Furthermore, N-doped graphene-capped Cu interconnects showed enhanced failure times of $\sim$1,390,000 s (3 MA cm$^{-2}$) and $\sim$120,000 s (10 MA cm$^{-2}$) (Fig. 3c, d). The graphene-capping on the Cu interconnects leads to lower electrical resistivity and higher thermal conductivity in the heterostructure interconnect owing to the high heat dissipation of graphene$^{31,32}$. In addition, C-Cu binding at the surface of the interconnect results in more stable and unmoved Cu atoms against electrical stress. Furthermore, an increase in the carrier density in graphene by doping drastically enhances the reliability of Cu/N-graphene interconnects with a failure time of $>10^6$ s under 100 °C and 3 MA cm$^{-2}$ DC stress. Hence, the EM is significantly mitigated by integrating the high conducting graphene layer on Cu, leading to enhanced reliability and thermal stability of the interconnects$^{12}$.

In addition, we implemented the fabrication of a Cu/N-graphene interconnect with a damascene-patterned structure for practical applications$^1$. A single damascene process was used to form Cu interconnect patterns to test the synthesis of the graphene (see Methods section for details). A selectively grown graphene-capping layer on a flat Cu surface was obtained without any physical changes (Fig. 4a-d). HRTEM image shows that the N-
doped graphene film was synthesized on the damascene-patternd Cu interconnect surface. The thickness of the graphene film was approximately 6.5 nm with 18 layers (Fig. 4b). In addition, Raman spectra and mapping image indicate that graphene was successfully synthesized on top of the Cu interconnects. In contrast to the detection of no graphene on the SiO2, the 2D contrast to the detection of no graphene on the SiO2, the 2D successfully synthesized on top of the Cu interconnects. In Raman spectra and mapping image indicate that graphene was then purged with argon. This process was repeated ve times to ensure graphene was formed from a decrease in ρ and an increase in Jbr and by the failure time. The Cu/N-graphene interconnect showed a ρ of 16.4 ± 0.2 μΩ cm and Jbr of 19.9 ± 0.6 MA cm−2, corresponding to an improvement of 4.1% and 21.3% over the pure Cu interconnect owing to a lower power factor (1.83) (Fig. 4e and Supplementary Fig. 13). In addition, the lifetimes of Cu/N-graphene interconnects as per the MTTF measurement were ~600,000 s (3 MA cm−2) and ~47,000 s (10 MA cm−2) longer than the ~73,000 s (3 MA cm−2) and ~8300 s (10 MA cm−2) for Cu/SlN4 (Fig. 4f). Thus, enhanced electrical properties and reliability were obtained by a graphene-capping layer even for a damascene-patternd structure.

DISCUSSION

We demonstrated the feasibility and benefits of graphene-capped Cu heterostructure interconnects by the direct synthesis of graphene films on Cu interconnects via APCVD at 400 °C while keeping the underlying Cu interconnect intact. The performance of the graphene-capped Cu interconnects in terms of resistivity, breakdown current density, and MTTF was enhanced as compared with those of pure Cu interconnects. Furthermore, the compatibility of the graphene-capped Cu heterostructure with the damascene-patternd structure was confirmed. This study is a significant step toward the direct fabrication of graphene-capped Cu interconnect during the manufacturing of future advanced interconnects for practical applications such as CMOS back-end-of-line (BEOL).

METHODS

Direct growth of graphene on Cu interconnects via APCVD

Cu interconnect patterns were fabricated on SiO2/Si substrates using photolithography followed by Cu sputtering. The width (w), thickness (t), and length (l) of the Cu interconnect line are 4 μm, 500 nm, and 100 μm, respectively. Then, it was loaded into the hot center of a quartz tube. Prior to graphene growth, the quartz tube was pumped down to ~10−6 Torr and then purged with argon. This process was repeated five times to flush the air contained in the quartz tube (residual oxygen concentration of 0%). After 200 sccm of Ar gas was supplied into the quartz tube, the pump was switched off, and the quartz tube was kept at ambient pressure. To increase the Cu grain size and ensure the removal of native oxide and a smooth Cu surface, the Cu interconnect was annealed at 750 °C for 30 min under a working pressure of 650 mTorr and an RF power of 30 W. As the excess Cu is removed by a chemical mechanical polishing (CMP) damascene-patterned Cu interconnect was formed. Its w, t, and l are 4 μm, 500 nm, and 100 μm, respectively, which is the same with Cu interconnect patterns. Cu/SlN4 and Cu/N-graphene interconnect with the damascene-patterned structure were fabricated by formation of SiN4 and N-doped graphene films on damascene patterned Cu interconnect.

Characterizations

The surface morphology, quality, uniformity and layers of graphene were characterized by optical microscopy (BK51, Olympus) and FESEM (JEOL JSM-750F). Raman spectroscopy (HR-320, 144 mW, λ = 532 nm, Horiba Jovin-Yvon). Estimations of the atomic compositions of the samples were obtained HRTEM images and EELS mapping in an image-aberration-corrected TEM (TITAN G2 60–300, FEI). XPS (AXIS Ultra DLD, Kratos Analytical) measurements were carried out using a monochromatic Al Kα X-ray source (1486.6 eV) to determine the chemical compositions and work function of the pristine and N-doped graphene films grown on Cu foil. The crystallinity of the Cu foils was evaluated by XRD (D/Max-2500, Rigaku). The electrical properties of interconnect were studied in air at room temperature using a high current source meter (Keithley 2430). The breakdown current density and resistivity of interconnects were estimated from I–V characteristic. The MTTF property was measured at 100 °C under continuous DC stress of 3 and 10 MA cm−2.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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AUTHOR CONTRIBUTIONS
M.S. and J.J. contributed equally. M.S. and M.H.H. conceived and designed the research. M.S. and J.J. performed most of the experiments including graphene synthesis, interconnect fabrication, characterization, and data analysis. J.J. and M.H.H. performed the optical, SEM, and Raman analysis. J.N. and J.Y.H. performed TEM analysis. Y.S. and B.H.L. performed the electrical characteristic measurements. M.S. wrote the manuscript. All authors discussed the results and commented on the manuscript.

COMPETING INTERESTS
The authors declare no competing interests.

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