GBTX emulator for development and special versions of
GBT-based readout chains

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ABSTRACT: The GBTX ASIC is a standard solution for providing fast control and data readout for radiation detectors used in HEP experiments. However, it is subject to export control restrictions due to the usage of radiation-hard technology. An FPGA-based GBTX emulator (GBTxEMU) has been developed to enable the development of GBT-based readout chains in countries where the original GBTX cannot be imported. Thanks to utilizing a slightly modified GBT-FPGA core, it maintains basic compatibility with standard GBT-based systems. The GBTxEMU also may be an interesting solution for developing GBT-based readout chains for less demanding experiments.

KEYWORDS: Data acquisition circuits, Front-end electronics for detector readout, Digital electronic circuits

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1 Introduction

The GBTX ASIC [1] is a standard solution for fast control and data readout for radiation detectors used in HEP experiments [2–5]. Together with the dedicated GBT-FPGA [3] core suitable for implementation in FPGA, it can be used for time-deterministic transmission of commands in the downlink direction and transmission of command responses and readout data in the uplink direction. For communication, a dedicated high-speed 4.8 Gb/s GBT Link protocol [6] is used. Connection to the Front-End ASICs is made via convenient SPI-Like E-Link interfaces.

Many readout systems have been created based on the GBTX [7–10]. For the STS and MUCH detectors in the CBM experiment, dedicated front-end ASICs [11] have been developed, together with a special HCTSP protocol [12] oriented on communication via AC-coupled links.

Unfortunately, the GBTX is not widely available. It is not a "custom of the shelf" (COTS) part. Additionally, due to the usage of the radiation-hard technology, it is subjected to export restrictions and unavailable in certain countries.

Therefore, in many international experiments, certain collaboration members cannot develop GBTX-based readouts in their countries. The usage of GBTX chips in all development sites also may not be justified from an economic point of view.

The GBTx emulator (GBTxEMU) board has been developed to eliminate the mentioned limitations.
2 Concept of the GBTxEMU board

The concept of the GBTxEMU board was based on a few assumptions:

- It should provide essential functionalities of the GBTX ASIC,
- It should be widely available (no export restrictions on components),
- It should be easily affordable (possibly based on cheap, mass-produced COTS components),

A relatively cheap commercial board from Trenz [13] TE0712 [14] with an Artix 7 FPGA was selected to fulfill the last two requirements. Of course, the GBTxEMU should emulate not the GBTX alone but the whole GBTX-based readout board. Therefore, the TE0712 board had to be supplemented with an additional baseboard equipped with necessary interfaces and other infrastructure. For example, obtaining the reference clock from the clock recovered from the GBT link requires a jitter cleaner.

The general concept of the GBTxEMU board is shown in Figure 1.

3 Hardware platforms for the GBTxEMU board

The first prototype of the GBTxEMU [15] (see Figure 2) used the TEBA0841-1 baseboard by Trenz [16], providing an SFP+ cage for the GBT Link transceiver and gold-pin header for E-link connections. Additionally, a 100 Mb/s DP83848 Ethernet PHY module [17] was connected.

The Si5338 clock generator, controlled by the FPGA, was used as a jitter cleaner in that version.

Experiences gathered with the first prototype were used to develop the first version of the GBTxEMU board (shown in Figure 3) in GSI. It is equipped with two SFP+ cages and the hardware jitter cleaner based on a Silabs Si5344 chip [19].

That version was equipped with the FMC connector enabling the use of FMC boards with various FEB connectors. Due to versatility, that version is a good solution for development and testing.

The GBTxEMU is also planned for use as a component of the GBT-based readout chain in the BM@N experiment [5, 20]. For that purpose, the second version of the GBTxEMU board (see Figure 4) was prepared. This version is designed in a Eurocard format. The E-Links are connected to the high-density Samtec connectors instead of the FMC connector for better space utilization.
Figure 2. The first prototype of GBTxEMU, based on TE0712 and TEBA0841 boards. Picture from the presentation [18].

Figure 3. The first version of the GBTxEMU board developed at GSI. On the left – the top side with the FMC equipped with ZIF connectors for FEBs. On the right – the bottom side with a TE0712-2 module.

Figure 4. The second version of the GBTxEMU developed at JINR in the Eurocard format and with high-density Samtec connectors for FEBs. The TE0712-2 module is covered with a heat sink.
4 Implementation of the GBTxEMU firmware

The block diagram of the GBTxEMU firmware is shown in Figure 5

![Block diagram of the GBTxEMU firmware](image)

**Figure 5.** Block diagram of the GBTxEMU firmware (based on [21]).

Because the main system clock is obtained by the jitter-cleaning of the clock recovered from the GBT Link it means that certain initialization must be done before the main clock is available. For that purpose the GBTxEMU is equipped with the J1B system controller using the additional “boot clock”\(^1\).

4.1 J1B system controller

Initialization of the GBTxEMU requires configuring the clock generator, the jitter cleaner, and the GTP transceivers. For that purpose, a simple synthesizable J1B CPU [22] was implemented. It is programmed in Forth [23] language. Due to good code density, despite relatively small 32 kB RAM, it may perform quite complex initialization routines. An example code that reads the board’s MAC address from a UNI/O FLASH memory [24] is shown in Listing 1.

The Forth language is considered to be difficult to learn but offers efficient possibilities of interactive work. It needs only a UART connection\(^2\) to the operator’s console. In the interactive mode, it is possible to create new procedures (called *words* in Forth) and execute them. Thence Forth may be a perfect debugging tool. The captured word definitions may also be compiled and put into the GBTxEMU configuration bitstream. The user-defined word *cold* is executed after the system starts.

4.2 GBTxEMU internal bus

Most functional blocks of the GBTxEMU are connected to the internal Wishbone bus. The bus is managed by the Address Generator for Wishbone (AGWB) system [4] which assigns the addresses

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\(^1\)The “boot clock” has a frequency of 10 MHz in the first batches of GBTxEMU and then it was replaced with 20 MHz.

\(^2\)It is also possible to emulate UART via JTAG. The J1B connected via JTAG-emulated UART is used in the KCU116_J1B project [25].
Listing 1: Example Forth code for the J1B, used to read the MAC address from the UNI/O FLASH memory.

for the internal registers, generates the VHDL code providing access to those registers, and generates
the software modules for Forth and Python, enabling convenient access to those registers via their
name. The address map may be automatically adjusted after modification of the register file.

The internal Wishbone bus has three masters. The first of them is J1B, described in the previous
section and used for initialization and debugging. The second is the IPbus [26] master, which may
control the GBTxEMU via the independent Ethernet interface (with 100 Mb/s or 1 Gb/s speed).
That requires that the board is initialized to the stage where the Ethernet connection is working.
Otherwise, it enables control and debugging using Python running on the computer, which is
more convenient than Forth. The third master is the controller based on the GBT-SC core [27].
This master provides the best emulation of GBTX because control commands and responses are
transmitted via the GBT link, just like in the case of the real GBTX.

4.3 The GBT-FPGA core

The GBT-FPGA core was developed by CERN [28]. It implements the essential GBTX function-
alities in an FPGA. The original implementation, however, does not support the Artix 7 FPGAs.
Therefore, certain modifications were necessary.

Adaptation of GBT-FPGA core was made based on a version prepared for Kintex 7 as it
was the most similar. The Artix 7 FPGAs use GTP transceivers [29], while Kintex 7 uses the
GTX transceivers [30]. The necessary modifications were related to different widths of the internal
datapath, internal clock frequencies, and configurations of the PLL blocks generating the transceiver
clock. The operation of GTP transceivers at 4.8 Gb/s (required for a standard GBT link) was achieved
successfully.
The Artix 7 FPGAs offer lower performance than Kintex 7. Despite this, it was possible to implement the forward error correction (FEC) in the downlink direction, which is essential for reliable transmission of control commands to front-end ASICs. Also, the optimized latency mode was possible in the downlink direction – it is necessary to synchronize the front-end ASICs. In the uplink direction, the ported GBT-FPGA provides standard latency transmission in the Widebus mode (without FEC).

4.4 Implementation of E-Links

The E-Link block is responsible for retrieving the appropriate bits from the downlink GBT frame and sending them serially via E-Links, and simultaneously for receiving the bits from the E-Links and storing them into the uplink GBT frame. The uplink direction is optimized for transmission of the hit data from the FEE ASIC. Hence, it is assumed that the uplink data are transmitted with a dual data rate (DDR). Because the downlink in the FEC mode used by the GBTxEMU delivers one 80-bit downlink frame every 25 ns, and the uplink in the Widebus mode accepts one 112-bit frame every 25 ns, the possible number of E-Links depends on the E-Link clock frequency $f_{\text{EL CLK}}$. It is limited by the number of bits available in the uplink frame and may be calculated according to the formula:

$$N_{\text{E-Links}} = \text{ceil} \left( \frac{112}{40 \text{ MHz}} \right).$$

Therefore, for E-Link clock frequency $f_{\text{EL CLK}} = 40$ MHz, the GBTxEMU may support up to 56 E-Links, while for $f_{\text{EL CLK}} = 80$ MHz only 28.

The original GBTX ASIC offers a possibility to control the phase of the generated E-Link clock and the delay of the input E-Link data. That enables adaptation to different values of the skew and length of the cable used for the FEE ASIC connection. In the GBTxEMU, the E-Link clock phase may be adjusted with a resolution of 78.125 ps using the MMCM block to produce the output clock. The input data from the E-Link are delivered through the IDELAYE2 blocks with run-time controllable delay (up to 2.496 ns with 78 ps resolution and with selectable clock edge) [21]. When used together, those functions enable reliable operation of the E-Links.

5 Current use and results

Different versions of the GBTxEMU have been used in test setups in WUT, GSI, and JINR (see Figure 6). The WUT setup is used mainly for development and testing purposes. In GSI, the GBTxEMU has been successfully used for debugging the port of the GBT-FPGA developed for the CRI readout board. The GBTxEMU provided extended diagnostics at the slave end of the GBT link. In JINR, the GBTxEMU is used to develop the readout chain for the BM@N. It is also planned to be used in its final version [5]. Of course, the FPGA-based design cannot assure radiation hardness. However, in situations where the highest throughput of E-Links is not needed, the board may be placed at some distance from the on-detector electronics, outside of a high magnetic field and radiation environment. The 10-meter length copper cable connection between the front-end electronics and GBTxEMU was proven to be stable in the BM@N STS project.
Figure 6. Three test setups equipped with GBTxEMU boards. On the left – the setup in GSI with 2 GBTxEMU v1 and two connected FEB-8 boards. In the center – the setup at WUT with a single GBTxEMU v1 and connected FEB-8 board. On the right – setup at JINR with a GBTxEMU v2 and connected BM@N STS FEB board.

6 Conclusions

The GBTX emulator (GBTxEMU) appeared to be a useful tool enabling the development of GBT-based readout systems in locations where the original GBTX ASIC cannot be used. It has also shown its potential at debugging the GBT links during porting of the GBT-FPGA IP core to the new FPGAs. The GBTxEMU may be used in special versions of the GBT-based readout chain, where radiation hardness is not essential. It may also be a basis for creating the GBT-controlled test setups for testing the FEE ASICs and modules connected via GBTX-compatible E-Links. The FPGA-based design is highly flexible, providing the end-users with the possibility to implement their own extensions.

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