Asymmetric SECE Piezoelectric Energy Harvester Under Weak Excitation

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ABSTRACT Piezoelectric energy harvesters (PEHs) are widely used to convert energy from a piezoelectric transducer into a stable DC form, which enables low-power IoT devices to have an unlimited operating life without using batteries. Under weak excitation conditions, however, the power-extraction efficiency of conventional PEHs is too low to provide power even to low-power IoT devices that requires low operation voltages less than 2 V. This paper proposes an asymmetric synchronous electric charge extraction (ASECE) scheme that improves the extraction efficiency of PEHs at low output voltages under weak excitation. The proposed ASECE is implemented using 0.18 \textmu m CMOS technology. The figure-of-merits (FOMs) of the proposed ASECE while operating under 2 V of output voltage are 7.14 and 6.24 at weak and strong excitations, respectively. The maximum FOM for various different excitation levels is observed to be as high as 7.7. The proposed ASECE is superior to prior art with respect to FOM, by at least 1.15 \times, 1.63 \times, and 2.21 \times under 2 V, 1 V, and 0.5 V outputs, respectively, under strong excitation.

INDEX TERMS Energy harvesting, piezoelectric devices, low power electronics, the Internet of Things.

I. INTRODUCTION

Battery-powered IoT devices have been widely used for embedded and remote sensors, but frequent replacement of their batteries due to limited lifetimes leads to higher operation and maintenance (O&M) costs. Energy harvesters eliminate the need for batteries, allow for unlimited operating lives, and thus lower O&M costs [1]–[5]. Among various energy sources, vibration-energy harvesting can utilize any mechanical vibration from common household goods, smart factories, vehicles, airplanes, constructions, and so on [6]–[10]. There are three main approaches regarding the implementations of a vibration-energy harvesters: electrostatic, electromagnetic, and piezoelectric. In-plane and out-of-plane capacitors produced using a micro-electro mechanical system (MEMS) can be used as electrostatic energy harvesters [11], but electrostatic potential is a lot higher than several tens of Volts that requires higher voltage switching devices and causes higher conduction losses. For periodically stressed applications, electromagnetic energy harvesters can be realized at the expense of bulky magnets and macro-scale coils [12]. Finally, piezoelectric energy harvesters (PEHs) are the simplest devices to fabricate, because their structural vibrations are directly converted to a voltage output without any additional complexity. In addition, PEHs can produce 3 to 30 times more power than their electrostatic or electromagnetic counterparts can at the compatible size [10], [13].

An example of a piezoelectric energy-harvesting system is shown in Fig. 1. Because the converted energy from the piezoelectric transducer (PT) is in a variable AC form, it cannot be directly used in most electronic devices requiring a stable DC supply voltage. When only a small amount of vibration energy is available, it is required to have a highly efficient PEH followed by a low-power IoT device using low operating voltage. These sensors indicate that an operating voltage of less than 2 V is widely used for low-power applications [14]–[21]. Inductor-based PEHs such as SSHI, SECE, and precharging SECE in [7], [8], [22]–[35]
are widely used for IoT devices. Recently, the sense-and-sat (SaS) scheme in [36] enhances the harvested power by maintaining the input near the maximum-power point at the expense of multiple switching in a cycle. In addition, the short-circuit synchronous electrical charge extraction (SC-SECE) in [37], phase-shift synchronous electrical charge extraction (PS-SECE) in [39], frequency tuning synchronous electrical charge extraction (FT-SECE) in [38], and conjugate impedance matching method in [40] have been developed for improving efficiency in wideband energy harvesting. However, the power extraction efficiency under weak excitation in the aforementioned PEHs is still too low to drive low-power IoT devices. In this paper, a highly efficient PEH that can operate under weak excitation conditions is proposed for low-power IoT devices with low operation voltage. The proposed PEH adopts the SECE method to obtain a constant output power regardless of the output voltage. Furthermore, the proposed method harvests, flips, and precharges energy only once in a cycle to maximize power under weak excitation.

II. CONVENTIONAL PEHS

In order to analyze and compare various PEHs simply, all the components are considered to be ideal without any loss. A conventional full bridge rectifier (FBR) in Fig. 2 is a basic approach to harvest energy from a PT modeled with an internal capacitance \( C_{PZ} \) and a sinusoidal input current \( i_{PZ} \), where the amplitude and frequency depend on the magnitude and period of the mechanical vibration, respectively. A FBR charges the output capacitor \( C_O \) according to the positive and negative input currents through two different paths. Assuming that the diode forward voltage is zero, \( i_{PZ} \) will charge \( C_{PZ} \) until \( v_{PZ} \) exceeds the rectified output voltage \( V_O \) for a positive half cycle. Once \( v_{PZ} \) exceeds \( V_O, i_{PZ} \) flows through the diodes and charges \( C_O \). For a negative half cycle of \( i_{PZ}, C_{PZ} \) is negatively charged until \( v_{PZ} \) exceeds \( V_O \). Subsequently, \( i_{PZ} \) charges \( C_O \) till the end of a negative half cycle. The maximum charge available in each half cycle is \( q_{PZ} \). The shaded area in the first period depicts the charge stored in \( C_{PZ} \), represented by \( q_{FB,lost} \), which is not delivered to the output. \( q_{PZ} \) and \( q_{FB,lost} \) can be defined by

\[
q_{PZ} = C_{PZ} V_{PP},
\]

\[
q_{FB,lost} = C_{PZ} (2V_O),
\]

where \( V_{PP} \) is the peak-to-peak open-circuit voltage of \( v_{PZ} \). Next, the harvested power of an FBR, \( P_{FB} \), can be defined as

\[
P_{FB} = E_H f_O = 2(q_{PZ} - q_{FB,lost}) V_O f_O = C_{PZ} (V_{PP} V_O - 2V_O^2) f_O.
\]

The maximum-power point can be found when \( V_O = 0.25 V_{PP} \). Therefore, the maximum \( P_{FB} \) becomes

\[
\text{max} (P_{FB}) = \frac{1}{4} C_{PZ} V_{PP}^2 f_O.
\]

To eliminate the charge lost in \( C_{PZ} \), inductor-based PEHs have been researched as shown in Fig. 3. A synchronized switch harvesting on inductor (SSHI) in Fig. 3(a) has been widely researched in [6], [22]–[25]. In phase 1 (harvest), \( q_{PZ} \) is fully delivered to \( C_O \) because \( v_{PZ} \) equals \( V_O \). Phase 2 (flip) is defined at the end of each half cycle, where \( S_P \) turns on and \( v_{PZ} \) is flipped to \(-V_O \) through an inductor \( L \). The operation in phase 3 is identical to that in phase 1, except that \( i_{PZ} \) is reversed. The harvested power of a SSHI, \( P_{SSHI} \), can then be defined as

\[
P_{SSHI} = 2q_{PZ} V_O f_O = 2C_{PZ} V_{PP} V_O f_O.
\]

Recently, a synchronized switch harvesting on capacitor (SSHC) has also been researched, wherein bulky inductors have been replaced with smaller capacitors [26]–[28]. As \( P_{SSHI} \) has a linear relationship with \( V_O \), it is not appropriate for low-voltage applications. Fig. 3(b) shows the process of synchronous electrical charge extraction (SECE), wherein the harvested power is not limited by the output voltage [7], [8], [29]–[31]. In phase 1 (store), \( q_{PZ} \) is stored in \( C_{PZ} \) to its positive direction. In phase 2 (harvest), at the end of each \( C_{PZ} \) to \( L \). The charge is then harvested to the output when \( v_{PZ} \) becomes zero by switching \( S_P \) off and \( S_S \) on. In phase 3, \( q_{PZ} \) is stored in \( C_{PZ} \) to its negative direction. The harvested power of an SECE, \( P_{SECE} \), can be defined as

\[
P_{SECE} = \frac{1}{2} C_{PZ} V_{PP}^2 f_O = C_{PZ} V_{PP}^2 f_O.
\]

The harvested power is four times larger than that of an FBR. To increase the harvested power of an SECE, the process of precharging SECE, as shown in Fig. 3(c), has been...
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FIGURE 3. Conventional PEHs (a) synchronized switch harvesting on inductor (SSHI), (b) synchronous electrical charge extraction (SECE), (c) precharging SECE.

FIGURE 4. (a) The circuit and (b) timing diagrams of the proposed ASECE.

Phases 1 and 3 are the same as those in an SECE. In phase 2 (harvest and precharge), \( S_S \) is switched on in order to harvest charge from \( C_PZ \) to \( C_O \) and to charge \( C_PZ \) to the precharged voltage value \( V_{PC} \) (or \(-V_{PC}\)) through \( L \) depending on the previous phase. The harvested power of a precharging SECE \( P_{PSECE} \) can be defined as

\[
P_{PSECE} = 2\left( \frac{1}{2} C_{PZ} (V_{PP} + V_{PC})^2 - \frac{1}{2} C_{PZ} V^2_{PC} \right) f_O
\]

where the power enhancement in a precharging SECE compared with that in an SECE is \( 2C_{PZ} V_{PP} V_{PC} f_O \).

\[
V_{PC} = V_{PP} + V_{PC} - 2V_O.
\]

where \( V_{PC} \) is \( V_{PC} \) at the previous half cycle. If \( V_{PP} = 2V_O \), \( V_{PC} \) can be saturated because \( V_{PC} = V_{PC} \). \( V_{PC} \) becomes smaller with the passage of time when \( V_{PP} < 2V_O \), which leads to a lower amount of power generation. In contrast, \( V_{PC} \) becomes larger when \( V_{PP} > 2V_O \), which may lead to problems due to overvoltage. To obtain a constant value of \( V_{PC} \), various alternatives have been researched [34], [35].

III. PROPOSED ASYMMETRIC SECE

A. BASIC IDEA

Fig. 4 shows the circuit and timing diagrams of the proposed asymmetric SECE (ASECE). Phase 1 (store) corresponds to storing energy to \( C_{PZ} \). \( i_PZ \) charges \( C_{PZ} \) to a positive value from the initially charged value \( V_{PZ} = V_{PP} + V_{PC} \). In phase 2 (precharge & harvest), at the end of the positive half cycle, \( S_P \) is on for precharging \( C_{PZ} \) until \( V_{PZ} \) reaches the preset value \(-V_{PC}\). The charged energy in \( C_{PZ} \) is transferred to \( L \). The rest of the energy stored in \( C_{PZ} \) is harvested by switching \( S_S \) on until the inductor current \( i_L \) becomes zero.

The operation in phase 3 (store) is similar to that in phase 1, except for the initially charged value of \( V_{PZ} = -V_{PC} \) and \( i_PZ \) in the opposite direction. In phase 4 (flip), at the end of the negative half cycle, switching on \( S_P \) allows for \( V_{PZ} \) to be flipped to the positive as \( V_{PZ} = V_{PP} + V_{PC} \). The harvested power of the proposed ASECE \( P_{ASECE} \) is defined as

\[
P_{ASECE} = \left( \frac{1}{2} C_{PZ} (2V_{PP} + V_{PC})^2 - \frac{1}{2} C_{PZ} V^2_{PC} \right) f_O = 2C_{PZ} V^2_{PP} f_O + 2C_{PZ} V_{PP} V_{PC} f_O,
\]

where the proposed ASECE extracts twice as much power as the SECE does, which can be observed from the first term of the equation. Moreover, the power is further increased by an amount corresponding to the second term of the equation, upon precharging \( C_{PZ} \).
B. CIRCUIT IMPLEMENTATION

Fig. 5 shows a block diagram of the proposed PEH. All switches are implemented using transmission gates controlled by a pre-configured sequence at each phase. To find the end of phases 1 and 3, the peak detector monitors detector (ZCD) sets the digital output $V_{ZCD}$ to a high value at the instant that the inductor current becomes zero, in phases 2 and 4. The control logic receives the output signals from each block and generates the switching signals $S_S$, $S_P$, and $S_{SP}$ for each phase.

The circuit and timing diagrams of the peak detector are shown in Fig. 6. The rectified voltage $v_{REC}$ is generated by $M_3$ and $M_4$ from $v_{PZ}^+$ and $v_{PZ}^-$. An AC current flows from $C_1$ to $R_1$ as $v_{REC}$ increases, making $V_-$ higher than $V_+$. $v_{REC}$ decreases after $v_{REC}$ reaches its peak value, resulting in $V_+ > V_-$. When $V_+$ exceeds $V_-$ by $V_H$, the hysteresis comparator $CMP_1$ sets the digital output $V_{PK}$ to be high. The peak detector is then reset by $S_{SP}$ immediately afterwards.

Fig. 7 shows the circuit and timing diagrams of ZCD. To place ZCD into sleep mode, reset signals $V_{R[0]}$ and $V_{R[1]}$ are set to be high in phases 1 and 3, respectively. When $v_{PZ}^+$ exceeds $v_{PZ}^-$, ZCD is enabled for phases 2 and 4 by making $V_{R[0]}$ and $V_{R[1]}$ low, respectively. If $i_L$ is larger than zero in phase 2, the on-resistance of $M_1$ depicted in Fig. 5 leads $v_{PZ}^+$ to become negative. Thus, the timing for $i_L = 0$ can be obtained at the condition $v_{PZ}^+ = 0$. In phase 4, the timing for $i_L = 0$ is detected in the same manner as the peak value of $v_{PZ}^+$ is determined in phase 1 from the peak detector. Tables 1 and 2 summarize and compare theoretical power harvested for various PEHs described in Section II under ideal conditions and the configurations with recent publications, respectively.

IV. SIMULATION RESULTS

Fig. 8 shows the simulated transient response of the proposed ASECE at the steady state. Phases 1 and 3 are operated over a positive and negative half cycle, respectively. These phases are slightly delayed because of hysteresis in the peak detector. In phase 2, $S_P$ and $S_S$ are switched on until $v_{PZ}^-$ reaches $V_{PC}$ and $i_L$ reaches zero, respectively. In phase 4, $v_{PZ}^-$ is flipped to $v_{PZ}^+$ during the period in which $S_P$ is switched on. Fig. 9 displays the simulated output power with varying $V_{PC}$, at various values of $V_{PP}$. The output power of the proposed ASECE increases as $V_{PC}$ or $V_{PP}$ increases. The normal operating voltage of the proposed ASECE is set to $|2V_{PP}+V_{PC}| \leq V_{MAX}$, where $V_{MAX}$ is the maximum operating voltage of each transistor. In order to maximize

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**TABLE 1.** Theoretical power harvested for various PEHs under ideal conditions.

| Method                  | Maximum Output Power |
|-------------------------|----------------------|
| FBR                     | $0.25C_{ref}V_{PP}f_0$ |
| SSSI [22]-[25]           | $2C_{ref}V_{PP}f_0$   |
| SECE [7], [8], [29]-[31] | $2C_{ref}V_{PP}f_0$   |
| Precharging SECE [32]-[35] | $C_{ref}V_{PP}f_0 + 2C_{ref}V_{PP}f_0$ |
| Proposed ASECE           | $2C_{ref}V_{PP}f_0 + 2C_{ref}V_{PP}f_0$ |

**TABLE 2.** Comparisons of operation for various PEHs.

| Method                  | Store | Flip | Precharge | Harvest |
|-------------------------|-------|------|-----------|---------|
| FBR                     | 0     | 0    | 0         | 2       |
| SSSI [22]-[25]           | 0     | 2    | 0         | 2       |
| SECE [7], [8], [29]-[31] | 2     | 0    | 0         | 2       |
| Precharging SECE [32]-[35] | 2     | 0    | 0         | 2       |
| SC-SECE [37]             | 2     | 0    | 0         | 2       |
| PS-SECE [38]             | 2     | 0    | 0         | 2       |
| FT-SECE [39]             | 2     | 0    | 0         | 2       |
| Conjugate Impedance [40] | 2     | 1    | 0         | 1       |
| Proposed ASECE           | 2     | 1    | 1         | 1       |
FIGURE 8. Simulated transient response of the proposed ASECE.

FIGURE 9. Simulated output power according to $V_{PC}$ at various values of $V_{PP}$.

The calculated FOM of the proposed ASECE is compared with that of the conventional PEHs under the ideal condition shown in Fig. 10(a), wherein the FOM in [36] is defined as

$$FOM = \frac{P_H}{0.25C_PZV_{PP}^2F_O}.$$  \hspace{1cm} (11)

As shown in Fig. 10(a), the FOM of the proposed ASECE is higher than that of the conventional PEHs under an output voltage of 2 V. The simulated FOM of the proposed ASECE, compared with that of conventional PEHs designed with the same process, is shown in Fig. 10(b). An FBR comprises a Schottky diode supplied by the CMOS process. The switches of an SECE and SSHI are designed to be the same size as that of the proposed ASECE. The FOM of the proposed ASECE maintains a value ranging from 12.6 to 14.2, which is higher than that of the conventional PEHs under an output voltage of 2 V.

V. EXPERIMENTAL RESULTS

Fig. 11 shows a microphotograph of the proposed ASECE. The proposed ASECE is fabricated using 0.18 $\mu$m CMOS technology, and it occupies an area of 0.12 mm$^2$. The experimental setup is shown in Fig. 12. A commercial PT (Mide PPA-1022) with a 0.9 g tip mass is placed on a shaker (Bruel & Kjaer type 4810) excited by a sine-wave signal. The signal, having a resonant frequency of the PT (85 Hz), is generated from a function generator and amplified by a power amplifier (Bruel & Kjaer type 2718). In Fig. 13, an accelerometer modeled BW 23204 is used for measuring $V_{PP}$ according to
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**FIGURE 13.** (a) Accelerometer, and (b) experimental results for $V_{pp}$ vs. acceleration.

**FIGURE 14.** Measured transient waveforms of the proposed ASECE during startup.

Various acceleration values based on the experimental setup. Fig. 14 shows the measured transient waveforms during the startup phase of the proposed ASECE. Because of the high extraction efficiency at a low voltage, the settling time is as low as 478 ms at an output voltage $V_O = 1.5$ V with $V_{PP}$, $V_{PC}$, $C_O$, and $R_L$ being 2.5 V, 2 V, 1 $\mu$F, and 550 k$\Omega$, respectively. Fig. 15 shows the measured input and switching waveforms of the proposed ASECE. As previously explained, $i_{PZ}$ is stored in $C_{PZ}$ during phases 1 and 3. In phase 2, the stored energy in phase 1 precharges $C_{PZ}$ to $V_{PC}$, and the remaining energy is harvested. In phase 4, the stored energy in phase 3 is flipped to $v_{PZ+}$. The detailed input and switching waveforms in phases 2 and 4 are shown in Fig. 16. In phase 2, $S_P$ is switched on until $v_{PZ-}$ reaches $V_{PC}$. In phase 4, $v_{PZ-}$ is flipped to $v_{PZ+}$, with $v_{PZ+}$ being slightly lower than $v_{PZ-}$ because of the conduction loss of the switching path.

Fig. 17 shows the measured output power of the proposed ASECE in weak and strong excitations, compared with that of an FBR fabricated on a separated chip. Under weak excitation, the value of the output power delivered is up to 0.57 $\mu$W at an output voltage of 0.4 V. In contrast, under strong excitation, the output power remains almost constant over the wide output range, with a peak value as high as 4.05 $\mu$W. The maximum FOM under an output voltage of 2 V is measured at various values of $V_{PP}$ and is depicted in Fig. 18. The FOM under weak excitation is considerably higher than that under strong excitation, with a peak value of 7.7 at $V_{PP} = 1.25$ V.

**FIGURE 15.** Measured input and switching waveforms of the proposed ASECE.

**FIGURE 16.** Measured input and switching waveforms of the proposed ASECE in (a) phase 2 and (b) phase 4.

Fig. 19 compares the measured FOM values of the proposed ASECE under strong excitation with the corresponding FOM values obtained from prior art. The maximum FOM value of the proposed ASECE for the output voltage under 2 V is 6.24. The proposed ASECE is superior to prior art under strong excitation. In Table 3, the proposed ASECE is compared with prior art with different topologies described in [18], [21], [28], and [31]. FOM values for three different conditions the proposed PEH is superior to prior art by at least $1.15 \times$ under an output of 2 V, $1.62 \times$ under an output of 1 V, and $2.21 \times$ under an output of 0.5 V. These results demonstrate that the proposed ASECE is more efficient than prior art under strong excitation.
TABLE 3. Performance comparison.

| Parameter       | [23] | [26] | [31] | [36] | This work |
|-----------------|------|------|------|------|-----------|
| Technology (µm) | 0.35 | 0.35 | 0.04 | 0.18 | 0.18      |
| Topology        | SSHI | SSHC | SECE | SaS  | ASECE     |
| Key Component   | L=1mH | C=45×8μF | L=2.2mH | L=1mH | L=1mH |
| PEH type        | MIDE | MIDE | MIDE | MIDE | MIDE |
| Self-Powered    | O    | X    | O    | X    | X        |
| Vp (V)          | 5    | 5    | 5.7  | N/A  | 2.5      |
| Cpe (nF)        | 20.8 | 45   | 43   | 7    | 7        |
| f0 (Hz)         | 226  | 92   | 75.4 | 85   | 85       |
| FOM (P0/Vp<2)   | 2.89 | 4.01 | 3.14 | 5.41 | 6.24     |
| FOM (P0/Vp<1)   | 1.48 | 1.77 | 2.8  | 3.82 | 6.21     |
| FOM (P0/Vp<0.5)| 0.67 | 1.02 | 1.52 | 2.75 | 6.08     |

(1) FOM = max(P0)/max(P0).
(2) Extracted from prior-art.

VI. CONCLUSION

A piezoelectric energy harvester with asymmetric SECE is proposed to achieve improved extraction efficiency, especially under conditions of low output voltage. Theoretically, the proposed ASECE extracts more power than conventional PEHs do. In order to measure the FOM, an FBR is fabricated using the same process as the proposed ASECE. The FOMs of the proposed ASECE with an output voltage of under 2 V are 7.14 and 6.24 under weak and strong excitations, respectively. The maximum FOM for various excitation levels is observed to be as high as 7.7. Compared with prior art, the proposed ASECE improves the FOM by more than 1.15×, 1.62×, and 2.21× under output voltages of 2, 1, and 0.5 V, respectively. Therefore, the proposed ASECE can be more practical compared with other PEHs when applied in low-power IoT devices.

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