LEVERAGING GPU BATCHING FOR SCALABLE NONLINEAR PROGRAMMING THROUGH MASSIVE LAGRANGIAN DECOMPOSITION∗

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Abstract. We present the implementation of a trust-region Newton algorithm ExaTron for bound-constrained nonlinear programming problems, fully running on multiple GPUs. Without data transfers between CPU and GPU, our implementation has achieved the elimination of a major performance bottleneck under a memory-bound situation, particularly when solving many small problems in batch. We discuss the design principles and implementation details for our kernel function and core operations. Different design choices are justified by numerical experiments. By using the application of distributed control of alternating current optimal power flow, where a large problem is decomposed into many smaller nonlinear programs using a Lagrangian approach, we demonstrate computational performance of ExaTron on the Summit supercomputer at Oak Ridge National Laboratory. Our numerical results show the linear scaling with respect to the batch size and the number of GPUs and more than 35 times speedup on 6 GPUs than on 40 CPUs available on a single node.

Key words. GPU optimization solver, second-order optimization method, decomposition

AMS subject classifications. 65K05, 90C06, 90C30, 90-04, 90-08

1. Introduction. Batch nonlinear programming refers to computing solutions of a batch of nonlinear programming problems that can be solved in parallel. The need for batch programming stems from distributed computing, which has been widely used to tackle large-scale optimization problems by the decomposition of the large problem into many smaller subproblems. In this case, the subproblems are solved in parallel at each iteration of the algorithm. Examples of distributed computing algorithms include Lagrangian-based decomposition algorithms, for example the alternating direction method of multipliers (ADMM) [6], and value function iteration of dynamic programming [7]. Structures amenable to such decomposition are embedded in many applications in the literature including network optimization (e.g., communication networks [31], electric grids [25], and water networks [35]), as well as stochastic optimization [19, 18] and multi-period optimization [17]. In these cases, the solution time highly depends on the time to solve each batch.

While graphics processing units (GPUs) have shown great success in accelerating the computation time of some batch operations, such as mini-batch training in machine learning and batched factorization [1, 14, 20] in linear algebra, little attention has been given to accelerating batched nonlinear programming using GPUs. Many studies have focused on solving a single medium to large optimization problem and leveraged GPUs to improve the computation time of the linear algebra only. For example, GPUs have been used to accelerate the solution of linear systems arising in convex optimization algorithms [30, 36, 37] and the KKT system of an augmented

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Lagrangian of nonlinear programming [9]. In [12], the authors have implemented some number of components of the L-BFGS-B algorithm\(^1\) on GPUs, however, the algorithm does not work fully on GPUs.

All the aforementioned work takes a hybrid approach; some part requires execution on CPUs and involves data transfers between CPUs and GPUs. Limited success in terms of outperforming CPUs has been observed on selected problems with these approaches. This situation is partly due to lack of a fast large-scale sparse symmetric indefinite linear system solver\(^2\) for GPUs, expensive data transfer cost, and the sequential nature of many optimization algorithms prohibiting full utilization of the parallel computation capability of GPUs. Such a linear solver is required because the system of equations (the KKT matrix) to be solved at each iteration of optimization algorithms is large, sparse, symmetric, and indefinite. In order to find a descent direction in this case, many optimization algorithms, such as Ipopt [43], perform inertia control which requires computation of the number of positive, negative, and zero eigenvalues. Recent experimental results [41] of Ipopt using a GPU-based linear solver SPRAL [11, 15] show limited success on dense problems only. In sparse cases, Ipopt with a GPU-based solver showed much slower performance than when it used CPU-based linear solvers.

In this paper we focus on batch nonlinear programming using GPUs, where we have a large number (e.g., tens of thousands) of problems in the batch. In this case, we employ a massive number of threads on GPUs to their full capacity to solve as many problems as possible in parallel so that we can maximize the throughput. Although individual solve of a problem might be still slower than CPUs, a vast number of parallel computations is expected to outperform CPUs in the case of a batched solve, even CPUs with multiple cores as demonstrated in section 6.

Special attention should be given to the kernel design and its implementation according to the problem size. When the size of problems in a batch is small, the algorithm becomes memory bound, therefore, data transfers between CPU and GPU could cause a significant cost. Reducing such transfers is a key to accelerating computation time. Also, due to the scarcity of available resources on the GPU hardware, kernel design should take into account factors leading to maximizing the throughput of the computation. We discuss these factors and present our kernel design scheme in section 4.

As a GPU solver for the individual solve of a problem in a batch, we implement a novel GPU-accelerated algorithm for bound-constrained nonlinear nonconvex optimization problems of the form:

\[
\text{minimize}_{x} \ f(x) \quad \text{subject to} \quad l \leq x \leq u,
\]

where \(x \in \mathbb{R}^d\) is the optimization variable and \(l, u \in \mathbb{R}^d \cup \{-\infty, \infty\}^d\) are respectively lower and upper bounds (allowing negative and positive infinite values). Bound constraints hold componentwise, and the objective function \(f : \mathbb{R}^d \to \mathbb{R}\) is a generic nonlinear nonconvex function. Bound-constrained problems play an important role as a building block to solve problems with more general constraints such as \(h(x) = 0\), where \(h\) is a linear or a nonlinear function.\(^3\) This is achieved by reformulating the

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\(^1\)This is a variant of the limited-memory Broyden–Fletcher–Goldfarb–Shanno (L-BFGS) for box-constrained nonlinear optimization [45].

\(^2\)Currently, Nvidia’s cuSOLVER [29] library supports only a dense version of symmetric indefinite linear solver.

\(^3\)General inequality constraints can be formulated as equality constraints by introducing slack variables, for example, \(g(x) \leq 0 \iff g(x) + s = 0, s \geq 0\).
given problem into a bound-constrained form by taking an augmented Lagrangian
\[ L_{\rho}(x; \lambda, \rho) := f(x) + \lambda^T h(x) + \frac{\rho}{2} \| h(x) \|^2 \]
and minimizing it with respect to \( x \), that is, \( \min_{l \leq x \leq u} L_{\rho}(x; \lambda, \rho) \). A sequence \( \{x_k\} \) is generated with each \( x_k \) corresponding to an approximate solution of the augmented Lagrangian problem, and under suitable assumptions [10, 26] the sequence converges to a solution of the original problem with an appropriate updating scheme for \((\lambda^k, \rho^k)\).

We demonstrate the computational performance of our algorithm by solving many nonlinear programming problems of (1.1) by leveraging GPU batching. We highlight that our numerical experiment cannot be performed by any existing solver. The solution of such nonlinear programming problems is required for the Lagrangian-based decomposition methods. For example, in our computational experiment, the decomposition of electric grid network results in 34,704 nonlinear programming sub-problems that need to be solved multiple times in the decomposition method. Our GPU-accelerated algorithm will be used to solve the nonlinear subproblems on multiple GPUs available on the Summit supercomputer at Oak Ridge National Laboratory. In addition, we implement the algorithm in Julia for the following reasons: portability, performance, and productivity. The portability is about removing the complicated process of setting compilation flags and linking proper libraries for each platform. A great productivity can also be achieved by Julia’s high-level operations (vs. low-level operations in C) while showing as fast performance as CUDA without requiring users to optimize the code [4].

Our batch nonlinear programming solver is extremely important in the new optimization algorithm paradigm that solves a large-scale optimization by various decomposition methods (e.g., [34, 44, 40]). In particular, our solver enables the scalable solution of large-scale nonlinear constrained optimization problem solely on GPUs. Recent advances on ADMM algorithms [39] enable us to have convergence guarantees even with nonconvex problems. This implies that for any given large-scale optimization problem we can decompose it into smaller subproblems via ADMM to the extent that will work well with our batch nonlinear programming solver on GPUs. Since other ADMM routines, such as consensus variable and multiplier updates, in general have a closed-form solution, they can be efficiently implemented on GPUs as well. Therefore, the entire ADMM algorithm can be implemented on GPUs. In subsection 6.1, we present such an ADMM example.

The contributions of this work can be summarized as follows:

- We develop the first bound-constrained nonlinear optimization solver, implemented fully on GPU without data transfer to or from CPU.
- The optimization solver, as well as the ADMM used for our experiment, has been implemented in Julia, which is portable to supercomputers such as Summit at Oak Ridge National Laboratory.
- We have investigated and profiled multiple GPU-centric design decisions, which we report in detail in section 4. Using the optimal choices for each algorithmic unit has allowed us to obtain a superior overall performance.
- By applying our approach to a distributed control of large-scale electric grid operations, we demonstrate that the solution time is significantly reduced by a factor of 9–35 on 6 GPUs (vs. 40 CPU cores) on Summit.
- We demonstrated the multi-GPU implementation by using direct GPU-GPU communication.

2. Background on GPU architecture. This section presents background on the GPU architecture with a focus mainly on the concepts and terminologies relevant
For GPU memory architectures, each device has its own memory hardware that is separate from the host (CPU) memory. Therefore, data transfers are needed when we want to copy data from the host to the device and vice versa. Similar to the CPU memory system, the GPU memory is hierarchical, based on data access speed, as illustrated in Figure 1(a). Basically, the higher the units are in the hierarchy, the faster they are for read and write operations. Registers are the fastest for read and write, L1 cache and shared memory are the next, and so on. We note that the L1 cache and shared memory (smem) share the same memory unit, and that we can determine how much space we allocate for each of them.

State-of-the-art GPU programming models (such as Nvidia CUDA, OpenCL, and oneAPI) implement the execution model based on single instruction, multiple threads (SIMT) that executes single instruction on multiple threads in lockstep. A kernel function is a small program that is used to execute instructions on GPUs. Once the kernel function is launched, the execution environment creates a grid of thread blocks, each of which consists of the same number of threads, as depicted in Figure 1(b).

Each GPU architecture consists of multiple streaming multiprocessors (SMs), each of which contains scheduler and cores for computation and registers and L1 cache/shared memory for storage. In particular, a SM schedules the execution of the instruction into warps, each of which typically consists of a set of 32 threads. The L1 cache and shared memory are shared by all the threads inside the same thread block to help them communicate with each other, whereas registers are allocated for each thread. Since these computational and storage resources on each SM are scarce, the number of thread blocks that can run in parallel on each SM is restricted depending on how many resources each thread block requires.

3. Overview of the ExaTron algorithm. In this section we describe a variant of the trust-region Newton algorithm TRON for bound-constrained, nonlinear non-convex optimization problems [23]. Our algorithmic variant ExaTron implements the complete Cholesky factorization for preconditioning, as opposed to the incomplete
factorization in the original algorithm [23], which is further discussed in subsection 4.3. Moreover, we present the core operations relevant to its implementation on GPUs.

Algorithm 3.1 summarizes the algorithmic steps of ExaTrON. It is an iterative Newton-based algorithm that requires evaluating the values of the objective function, its gradient, and Hessian at the current point at each iteration (in line 3). These values are used to formulate a second-order Taylor approximation of the given model at the current point $x^k$, $f(x) \approx \tilde{f}(x) := f(x_k) + \nabla f(x_k)(x-x_k) + \frac{1}{2}(x-x_k)^T \nabla^2 f(x_k)(x-x_k)$.

ExaTrON then computes a Newton direction for the approximation $\tilde{f}$ (or a descent direction following a negative curvature in the nonconvex case) within the trust-region, expecting that we may be able to reduce the actual objective function value by moving along that direction. These steps correspond to Line 3 through Line 10 of Algorithm 3.1.

ExaTrON computes a Newton direction by the following four steps: (i) Cauchy point computation (Line 4); (ii) identification of a subspace to optimize (Line 5); (iii) subspace optimization using a conjugate gradient step (Line 6); and (iv) projected line search (Line 10). The Cauchy point computation step performs the gradient projection to find a point with a sufficient reduction for the approximation $\tilde{f}$ in Line 4. The sufficient reduction of a Cauchy point is a key property to guarantee the global convergence of the procedure. Starting from the Cauchy point, we identify a subset of the variables to optimize further, which has been shown in [26, 23, 22] to result in a faster convergence rate (superlinear or even quadratic). The subset corresponds to the variables with their values being strictly within their bounds, denoted by $\mathcal{F}$ in Line 5. We then optimize the variables in the subset by using the trust-region based conjugate gradient method [38]. This involves the computation of a preconditioner $L$ [22] to accelerate the convergence of the conjugate gradient step. Convergence of the conjugate gradient step is reached when one of the following three conditions is satisfied: (i) $|\mathcal{F}|$ number of CG iterations has been taken; (ii) the current CG direction reaches the trust-region radius; and (iii) a negative curvature is detected. We note that condition (iii) allows us to move along a descent direction even if $\nabla^2 f(x^k)$ is
not positive definite [38]. Using the direction $w$ computed in Line 9, we perform a projected line search to find the next point with a sufficient reduction, as depicted in Line 10. The projected line search allows a rapid change of active sets, which further accelerates the convergence. Interested readers are referred to [23] for more details.

Figure 2 describes the core operations to implement Algorithm 3.1, with a mapping showing where those operations are used in it. The numbers in parentheses at the end of each operation correspond to the line numbers of Algorithm 3.1. ExATRON implements its entire algorithm on GPUs in a way that does not require data transfers between CPUs and GPUs, provided that evaluation functions are implemented on GPUs. This removes latency issues incurred by such data transfers and enables us to achieve a much faster performance than on CPUs as described in section 6.

4. Kernel design principles. This section discusses the six kernel design principles and optimization techniques that are considered for the efficient implementation of Algorithm 3.1 on GPU. The design choices made in this section are specific for a nonlinear programming problem with 32 variables or less, considering the computational experiment in section 6. Note, however, that for problems with a larger number of variables, we discuss alternative choices of each design principle.

4.1. Single kernel vs multiple kernels. Our choice of the kernel design in EXATRON is to use a single kernel function in order to maximize the algorithm throughput. The throughput can be maximized by promptly reassigning the resources on SMs to thread blocks used for the optimization problems. Moreover, with this design choice, a batch run can be easily implemented by launching the kernel with a grid of thread blocks, whose size is equal to the number of problems in the batch. Assigning a specific thread block to each problem is logical, because the thread blocks are independently used and scheduled in the single-kernel design. However, a potential caveat of this single-kernel approach is that a large number of live registers are required for a thread block, as the registers may need to save many states in different device functions during the kernel execution.

Alternatively, multiple kernels may be employed as an alternative design choice in order to avoid the high register usage issue. However, the multi-kernel design would involve frequent memory operations to copy the current algorithm state information from one kernel to the other, exacerbating memory-bound situations. Moreover, the implementation becomes more complicated with multiple kernel functions, because we need to track down each problem’s state outside of the kernel function. If the
same kernel function was used for different problems by employing multiple thread blocks, the throughput would be significantly degraded due to the potential wait time for reassigning problems to the kernel function.

4.2. Thread configuration. ExaTRON uses the single warp 1-dimensional thread configuration. Each thread block consists of a single warp of 32 threads with an 1-dimensional thread configuration. These threads naturally enable parallel operations on a vector of size up to 32. Since most of our operations are matrix-vector and vector-vector operations (described later in this section), such a 1-dimensional scheme fits well with our needs.

Since we perform factorization of a matrix of size \( n \times n \) in Algorithm 3.1, one might think that a 2-dimensional \( n \times n \) thread configuration may be more efficient, with each thread in charge of each element of a matrix. This configuration may be effective when we read or write the entire matrix: one line of code will do the work, such as \( B[tx, ty] \leftarrow A[tx, ty] \), where \( tx \) and \( ty \) are thread IDs in \( x \)- and \( y \)-coordinate, respectively.

However, the number of threads required for the 2-dimensional \( n \times n \) configuration is proportional to the square of the number of variables, limiting the throughput of ExaTRON on each multiprocessor significantly. As discussed in [1], for \( n = 16 \) we already need 256 threads for each thread block in this case. On the Nvidia’s Volta architecture [27], this implies that we can have at most 8 active thread blocks on each multiprocessor, since a maximum of 2,048 threads is allowed per multiprocessor. Since a maximum of 32 thread blocks is allowed on each multiprocessor, the maximum throughput can be reduced by a factor of 4 with this configuration.

Another issue with the 2-dimensional \( n \times n \) configuration is that instruction efficiency is expected to be much lower than the single warp 1-dimensional configuration. Among the core operations of ExaTRON (Figure 2), factorization and triangular solves are the most expensive. However, they factorize or solve a single column of size at most \( n \) at a time, which makes the remaining threads idle. Moreover, the synchronization burden increases because a thread-level synchronization should be performed to synchronize between warps instead of a lighter warp-level synchronization.

In Figure 3, we plot the computation time ratio between the 1-dimensional and 2-dimensional thread configurations obtained from running ExaTRON for a batch solve.
when a single warp was used in both cases for $n \leq 5$, the 2-dimensional configuration showed slightly faster computation time than did the 1-dimensional configuration. For $n \geq 6$, however, its computation time deteriorated sharply when it started to use more than a single warp; and it showed up to 9 times slower performance than the 1-dimensional configuration. A similar result was obtained in [1] for Cholesky, LU, and QR factorizations under the same two different thread configurations.

4.3. Cholesky factorization. We use the Cholesky factorization to compute a preconditioner $L$ for a dense Hessian matrix $A = \nabla^2 f(x)$. If $A$ is positive definite, the Cholesky factorization will give us a lower triangular factor $L$ such that $A = LL^T$. In this case, $\hat{A} = L^{-1}AL^{-T}$ becomes an identity matrix, and we can find a solution to $\hat{A}s = \hat{b}$ in just one conjugate gradient iteration. If $A$ is not positive definite, $L$ is computed for a diagonally perturbed matrix ($A + \alpha I$) for some $\alpha > 0$. Such a preconditioner is expected to have eigenvalues of $\hat{A}$ clustered so that we can find a solution in a few conjugate gradient iterations [22, 23, 26].

In contrast to the existing method [23], which implements an incomplete Cholesky factorization with sparse linear algebra, ExaTron implements a complete Cholesky factorization with dense linear algebra. The incomplete Cholesky factorization stores only a subset of the new nonzero entries generated during factorization because of storage limitation with sparse linear algebra. This may result in a less accurate preconditioner. In contrast, the complete Cholesky factorization stores all of the newly generated nonzero entries. Since we are dealing with small sparse Hessian matrices, storing them in a dense matrix does not induce any memory limitations on GPUs. Dense linear algebra computations combined with GPU’s SIMT capability may be as competitive as sparse linear algebra in this case as well. By storing all the newly generated nonzero entries, we will have a more accurate preconditioner than that of the incomplete Cholesky factorization, which could potentially lead to fewer conjugate gradient iterations.

By taking advantage of a small matrix, we store its entire elements in shared memory during factorization for efficient read/write operations on GPUs. In this case, we do not have to employ a blocking algorithm that stores a block of elements at a time and factorizes it for efficient data reuse. All the elements are already available in shared memory, and read/write operations on shared memory are much faster than on global memory. Therefore, we implement an unblocked version of Cholesky factorization; we factorize one column at a time without employing level 3 BLAS operations. A similar design choice was made in [1] for a batch of Cholesky factorizations of small matrices of size $n \leq 32$.

To further optimize the implementation, we have experimented with two representative Cholesky factorization algorithms [14, 20]: left-looking factorization and right-looking factorization. The left-looking factorization applies all the previous updates just before a column is factorized, called lazy update, whereas the right-looking

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4 We modified the hs45 problem from [13] to experiment with different numbers of variables. The problem is a bound-constrained nonlinear nonconvex problem with objective function $f(x) = 120 - \prod_{i=1}^{n} x_i$ and bounds $x_i \leq i$ for $i = 1, \ldots, n$. Hence, the optimal solution is $x_i^* = i$. In each batch, we generated the same 10,000 instances.

5 There are other methods to compute a preconditioner, such as LU factorization. However, Cholesky factorization exploits the symmetricity of the Hessian matrix, enabling two times faster computation time than LU factorization.

6 We note that because of the numerical limitation of finite precision of floating-point numbers, we determine $s$ is a solution to $\hat{A} s = \hat{b}$ if $\|\hat{A} s - \hat{b}\| \leq \epsilon$ for some small error tolerance $\epsilon > 0$. 

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factorization immediately applies the updates to the trailing submatrix right after a column is factorized. A theoretical analysis in [14] shows that the left-looking algorithm has a smaller number of read/write operations than that of the right-looking algorithm, thus making it more efficient under memory-bound situations.

Table 1 shows the average computation time of the left-looking and right-looking batched Cholesky factorizations over 10,000 randomly generated matrices for $1 \leq n \leq 32$. As expected from the analysis, the left-looking algorithm showed a faster performance than that of the right-looking algorithm. Hence, ExaTron uses by default the left-looking Cholesky factorization algorithm to compute a preconditioner.

Table 1: Average computation time of the left- and right-looking Cholesky factorizations.

| Factorization      | Time (ms) |
|--------------------|-----------|
| Left-looking       | 0.362     |
| Right-looking      | 0.437     |

4.4. Triangular solves. In the conjugate gradient step, we need to perform matrix-vector multiplications between a preconditioned matrix $\hat{A} = L^{-1}AL^{-T}$ and a vector $p$. This involves two triangular solves: 1) $L^Tz = p$ (backward substitution); and 2) $Lq = \tilde{z}$ (forward substitution), where $\tilde{z} = Az$.

Triangular solves are inherently memory bound because they have to sequentially access one column at a time with a simple arithmetic applied to each element of it. Moreover, the number of elements to access is diminishing as we move forward or backward in both forward and backward substitutions. Hence, at most $n$ threads are needed. In this case, we apply data parallelism as described in subsection 5.2, updating each element of a column in parallel.

Implementing the forward substitution is straightforward; however, the backward substitution involves the transpose of $L$, requiring a row-wise memory access with as many strides as the size of the matrix. Although we store the elements of $L$ in shared memory, this memory access pattern could cause bank conflicts. For example, when $n = 8$ and the shared memory has 32 banks, a 2-way bank conflict will occur: elements in the same row with column indices differing by 4 will be stored in the same bank as they are accessed at the same time by different threads.

To avoid bank conflicts, we store the elements for both $L$ and $L^T$ in the same matrix. Since $L$ is a lower triangular matrix stored in a dense matrix format, we could use its upper triangular part to store the elements of $L^T$. This would involve additional write operations for the subspace optimization step of Algorithm 3.1. But since the backward substitution is applied multiple times during the conjugate gradient iterations and we could avoid bank conflicts, we may obtain performance gain offsetting the cost of additional writes. A similar approach was applied in [14].

In Table 2 we present the average computation time of explicit and implicit backward substitutions over 10,000 randomly generated matrices. By explicit, we mean we save the transpose of $L$ in its upper triangular part explicitly, whereas we perform row-wise access in the case of implicit. The results demonstrate that saving the transpose $L^T$ explicitly yields a faster computation time.

4.5. Shared-memory management. In many parts of ExaTron, memory space is needed to share data between device functions and to store and reuse in-
Table 2: Average computation time of explicit and implicit triangular solve

| Backward substitution | Time (ms) |
|-----------------------|-----------|
| Explicit              | 0.875     |
| Implicit              | 1.408     |

termediate computation results. The current iterate $x^k$ is used by all components of ExaTron together with its lower and upper bounds. A preconditioner matrix is referred to in multiple places of ExaTron. We also need some number of vectors to store a Cauchy point and perform the conjugate gradient step.

One advantage of ExaTron’s algorithm is that it does not require dynamic memory allocation during its procedure. Therefore, we can predetermine the memory space needed for its computation for a given problem size $n$. For efficient data access and reuse, we use shared memory for such memory space.

Table 3 presents the effect of shared memory on the computation time of ExaTron over the batch of 10,000 nonlinear nonconvex problems used in subsection 4.2. With shared memory, ExaTron’s computation performance was about twice faster.\(^7\)

Table 3: Average computation time with/without using shared memory

| Data share              | Time (ms) |
|-------------------------|-----------|
| Shared memory           | 9.536     |
| No shared memory        | 16.293    |

Currently, the memory space allocated in shared memory for each thread block is proportional to the square of the problem size, $O(n^2)$. Since 96 KB of shared memory are available on recent GPU architectures, for small $n$ our shared-memory requirement is not a limiting factor for achieving high occupancy. For medium or larger size $n > 32$, however, it could become a limiting factor, and a different implementation may be needed to achieve higher occupancy in that case.

4.6. Register file management. ExaTron’s kernel invokes multiple device functions, and some of them are called in a nested way. This could increase the number of live registers significantly by accumulating the function calls in the nested call graph. When we compile ExaTron, the output of “ptxas -v” shows that our kernel function uses more than 100 registers. If we add another kernel on top of it (such as a kernel implementing an augmented Lagrangian algorithm), the number of registers could increase even more.

The use of a large number of registers potentially hinders achieving high occupancy. On the Volta architecture, the number of registers allowed per multiprocessor is 65,536. Assuming that each thread is using about 100 registers, the limit on the number of active thread blocks becomes 20.\(^8\) Therefore, the theoretical occupancy we could achieve is at most 31%.

\(^7\)As noted on page 17 of [27], the Volta architecture significantly improved L1 data cache performance, leading to much lower latency and higher bandwidth. When we do not use shared memory, frequently used data are cached in the L1 data cache.

\(^8\)The number was obtained from floor$(65536/(32 \times 100))$, 4 = 20 where we round down the result of the division to the multiple of 4, 4 being the warp allocation granularity.
To achieve higher occupancy, we need to reduce the number of registers down to where it stops improving performance. In general, there is a trade-off in restricting the number of registers. It may incur register spills to local memory, potentially slowing performance on data access. On the other hand, it could increase occupancy so that larger number of thread blocks could be executed simultaneously. We control the number of registers to use by specifying explicitly the compile option `maxregs`.

5. Other Implementation Details. We describe other implementation details to optimize the efficiency of the core operations on GPU. The implementation details considered in this section are independent to the problem size.

5.1. Register shuffling and warp-level synchronization. In some parts of ExaTRON, we need to compute an aggregation over a vector, such as a sum or a maximum of the vector elements, and broadcast the result back to threads. For example, a two-norm or a maximum-norm of a vector needs to be computed to check the violation of a trust region, \( \|x\|_2 \leq \delta \), or the convergence of the algorithm (measured by the maximum element of the projected gradient vector \( \|\nabla_{[l,u]} f(x)\|_\infty \leq \epsilon \)). Once we compute such a value, we need to broadcast it back to threads so that each thread can proceed to the next step.

![Diagram](image)

**Fig. 4**: Sharing values between threads in the same warp via register shuffling. `op` is a binary operator such as `+` or `max`.

For an efficient utilization of threads and a lightweight synchronization, we implement this type of aggregation using a register shuffling and a warp-level synchronization. The register shuffling refers to shared register values between threads in the same warp-through shuffling. For example, in order to compute \( \|x\|_2 = \sqrt{\sum_{i=1}^{n} x_i^2} \), each thread \( i \) for \( i \in \{1, \ldots, n\} \) computes \( x_i^2 \) first, and the values are summed up by using a register shuffling as shown in **Figure 4** for \( n = 8 \). The aggregated value is stored in the first thread, and we broadcast it back to all threads in the same warp using the register shuffling again. Similarly, computing a maximum is performed by replacing the `+` operator with `max`. Register shuffling routines include a warp-level synchronization such as `CUDA.sync_warp()`, which is lighter than a thread-level synchronization `CUDA.sync_threads()`. Also, the use of registers avoids the use of more expensive shared memory. All of these make it efficient to compute an aggregation and share data between threads in the same warp.

5.2. Data-level parallelism. Data-level parallelism (DLP) refers to applying the same instruction to multiple data in parallel. Arithmetic operations such as `axpy()`, `copy()`, and `scal()` can benefit from DLP by affecting one thread per element.
in a vector, replacing the use of a loop by a single line of code. For example, \( \text{axpy}() \) computes \( y \leftarrow y + ax \), where \( x \) and \( y \) are vectors of the same size and \( a \) is a scalar. Without the use of DLP, we have to loop around each element of those two vectors like for \( i=1:n \) \( y[i] = y[i] + a*x[i] \), where only a single thread works at a time. With DLP, this can be implemented as \( y[tid] = y[tid] + a*x[tid] \), where \( tid \) is a thread ID less than or equal to \( n \), utilizing \( n \) threads simultaneously. In a similar way, \textsc{ExaTron} makes use of DLP for other arithmetic operations whenever applicable.

5.3. **Instruction-level parallelism.** Within a thread, instruction-level parallelism (ILP) refers to the simultaneous execution of multiple instructions in a sequence of them that can be executed in any order. This depends on the compiler’s capability to detect such independent instructions.

An example of ILP in \textsc{ExaTron} can occur when we form a submatrix in step ii of the procedure. We extract and copy the rows and the columns of a Hessian matrix \( A \) corresponding to the free variables. This is implemented by assigning each thread to each free variable index—applying DLP—and having it copy the rows of \( A \) corresponding to that column. There are multiple rows to copy for each thread, and these copy instructions are independent of each other, making them a target to apply ILP: for thread \( j \) taking care of the \( j \)th free column, it copies elements \( A[i,j] \) for \( i \in R(j) \), with \( R(j) \) being the set of row indices to copy for column \( j \), and these copy instructions can be executed in any order.

6. **Computational Results.** In this section we demonstrate the performance of \textsc{ExaTron} using a distributed control application from the power system literature. In subsection 6.1 we briefly introduce an alternating current optimal power flow (ACOPF) and its distributed-computation method based on an alternating direction method of multipliers (ADMM). Subsections 6.2 and 6.3 describe the performance of \textsc{ExaTron} over single and multiple GPUs, respectively. We compare the performance of the GPU implementation of \textsc{ExaTron} with a CPU implementation in subsection 6.4.

The implementation of \textsc{ExaTron} is written in Julia, and the code is available at https://github.com/exanauts/ExaTron.jl. All experiments were performed on a compute node of the Summit supercomputer at Oak Ridge National Laboratory using Julia 1.6.0 [5] and CUDA.jl 2.6.1 [4]. Note, however, that our implementation is not limited to a single node. Each compute node of the Summit supercomputer has 2 sockets of POWER9 processors having 22 physical cores each, 512 GB of DRAM, and 6 NVIDIA Tesla V100 GPUs evenly distributed to each socket [21]. We note that the MPI communication between GPUs was implemented using a CUDA-aware MPI with the asynchronous send/receive routines. For CPUs, we used the scatter/gather routines. Our different use of the MPI routines is mainly because we found scatter/gather routines between GPUs were much slower than the asynchronous send/receive. We re-emphasize that \textsc{ExaTron} does not require transferring data between the CPU and GPU.

6.1. **Distributed control of ACOPF.** In electrical engineering, the optimal power flow problem [42] focuses on computing the optimal dispatch of active and reactive powers among a set of generators, while satisfying physical constraints such as voltage/generator limits, power balance, and transmission line limits. The power network is modeled as a undirected graph: generators are located on certain buses of the network. The active and reactive powers produced by the generators flow between buses via the transmission lines, so as to satisfy demand at each bus. The problem
corresponds to the ACOPF problem when the power flow is modeled by using alternating current. In that case, there exists an exact formulation that encapsulates the actual physical constraints, such as Ohm’s and Kirchhoff’s current laws. Computing an exact and efficient solution to the ACOPF problem has a practical application, since a small percentage increase in market efficiency leads to billions of dollars of cost savings per year \([8]\) for transmission operators.

Four representative variants of the ACOPF formulations exist: polar, rectangular, extended rectangular, and current-voltage formulations. Although their forms are different, they are equivalent between each other. In the following, we present the extended rectangular formulation using the notation in \([24]\):

\[
\begin{align*}
\text{minimize} & \quad f_{gi}(p_{gi}) \\
\text{subject to} & \quad p_{gi} \leq p_{gi} \leq \bar{p}_{gi}, \quad (g, i) \in \mathcal{G} \\
& \quad q_{gi} \leq q_{gi} \leq \bar{q}_{gi}, \quad (g, i) \in \mathcal{G} \\
& \quad \sqrt{q_{gi}^2 + p_{gi}^2} \leq \bar{s}_{ij}, \quad (i, j) \in \mathcal{L} \cup \mathcal{L}_t \\
& \quad (w^R_{ij})^2 + (w^I_{ij})^2 = w_{ij} w_j, \quad (i, j) \in \mathcal{L} \\
& \quad \bar{v}_i^2 \leq w_i \leq \bar{v}_i^2, \quad i \in \mathcal{B} \\
& \quad \tan(\theta^A_{ij}) w^R_{ij} \leq w^I_{ij} \leq \tan(\theta^A_{ij}) w^R_{ij}, \quad (i, j) \in \mathcal{L} \\
& \quad \sum_{(g, i) \in \mathcal{G}} p_{gi} - p^d_i = \sum_{j \in \mathcal{B}_i} p_{ij} + g_i^{ch} w_i, \quad i \in \mathcal{B} \\
& \quad \sum_{(g, i) \in \mathcal{G}} q_{gi} - q^d_i = \sum_{j \in \mathcal{B}_i} q_{ij} - b_i^{ch} w_i, \quad i \in \mathcal{B} \\
& \quad p_{ij} = g_{ij}^c w_i - g_{ij} w^R_{ij} + b_{ij} w^I_{ij}, \quad (i, j) \in \mathcal{L} \\
& \quad q_{ij} = b_{ij}^c w_i - b_{ij} w^R_{ij} - g_{ij} w^I_{ij}, \quad (i, j) \in \mathcal{L} \\
& \quad p_{ji} = g_{ji}^c w_j - g_{ji} w^R_{ij} - b_{ji} w^I_{ij}, \quad (i, j) \in \mathcal{L} \\
& \quad q_{ji} = b_{ji}^c w_j - b_{ji} w^R_{ij} + g_{ji} w^I_{ij}, \quad (i, j) \in \mathcal{L},
\end{align*}
\]

where \(\mathcal{G}, \mathcal{L}, \) and \(\mathcal{B}\) denote the set of generators, branches, and buses in the network, respectively. We use \((g, i) \in \mathcal{G}\) to represent that generator \(g\) is connected to bus \(i\).

For a branch \((i, j) \in \mathcal{L}, i\) is the “from” bus and \(j\) is the “to” bus in \((j, i) \in \mathcal{L}_t\). Formulation \((6.1)\) is a nonlinear nonconvex optimization problem, which is known to be computationally challenging; even verifying local optimality can be an NP-hard problem \([32]\). Hence, convergence is in general achieved at a point satisfying only second-order necessary optimality conditions \([26]\), and we are not interested in proving global optimality.

In order to efficiently solve large-scale ACOPFs, Mhanna et al. \([24]\) introduce a distributed control approach, where the problem is decomposed into components—generators, branches, and buses—by duplicating the variables linking different components. Then, the problem is solved by optimizing each component separately using an ADMM algorithm. One subproblem is associated with each component, resulting in a total number of subproblems equal to \((|\mathcal{G}| + |\mathcal{L}| + |\mathcal{B}|)\). At each ADMM iteration, the algorithm starts by solving the generator and branch subproblems in
parallel. Then, the bus subproblems are solved concurrently. Once all the subproblems are solved, the algorithm updates its Lagrange multipliers and moves to the next iteration.

One advantage of the algorithm introduced in [24] is that both the generator and the bus subproblems have a closed-form solution, so we do not have to employ a nonlinear optimization solver for them. However, the solutions of branch subproblems require to solve nonlinear nonconvex problems, each of which is formulated as (6.2) for branch \((i, j) \in L\):

\[
\begin{align*}
\min v_i, v_j, \theta_i, \theta_j & \quad \sum_{(l, m) \in ((i, j) \cup \{j, i\})} \left( \lambda_{pi,m}(p_{lm} - \tilde{p}_{lm}) + \lambda_{qi,m}(q_{lm} - \tilde{q}_{lm}) \\
+ \frac{\rho_{pi,m}}{2}(p_{lm} - \tilde{p}_{lm})^2 + \frac{\rho_{qi,m}}{2}(q_{lm} - \tilde{q}_{lm})^2 \right) \\
+ \sum_{l \in \{i, j\}} \left( \lambda_{w_l}(v_l^2 - \tilde{w}_l) + \lambda_{\theta_l}(\theta_l - \tilde{\theta}_l) \\
+ \frac{\rho_{w_l}}{2}(v_l^2 - \tilde{w}_l)^2 + \frac{\rho_{\theta_l}}{2}(\theta_l - \tilde{\theta}_l)^2 \right)
\end{align*}
\]

subject to

\[
\begin{align}
(6.2a) & \quad v_i \leq v_i \leq \bar{v}_i \\
(6.2b) & \quad v_j \leq v_j \leq \bar{v}_j \\
(6.2c) & \quad -2\pi \leq \theta_i, \theta_j \leq 2\pi,
\end{align}
\]

where the definition of \(p_{ij}, q_{ij}, p_{ji},\) and \(q_{ji}\) follows from (6.1i)–(6.1l) by plugging-in \(w_i = v_i^2, w_j = v_j^2, w_{ij}^0 = v_i v_j \cos(\theta_i - \theta_j),\) and \(w_{ij}^1 = v_i v_j \sin(\theta_i - \theta_j).\) Note that the objective of (6.2) is nonconvex.

| Data          | # Generators | # Branches | # Buses |
|---------------|--------------|------------|---------|
| 2868rte       | 600          | 3,808      | 2868    |
| 6515rte       | 1,389        | 9,037      | 6515    |
| 9241pegase    | 1,445        | 16,049     | 9,241   |
| 13659pegase   | 4,092        | 20,467     | 13,659  |
| 19402goc      | 971          | 34,704     | 19,402  |

We have implemented the ADMM algorithm fully on GPUs without data transfer to the CPU, and we use ExaTron to solve the branch subproblems at each ADMM iteration. The ADMM algorithm has also been written in Julia. We have experimented with our implementation in five large-scale examples from the MATPOWER [46] and PGLIB benchmark [3], where the first four of them were also used in the literature to test ADMM algorithm [24, 40]. Table 4 presents the data statistics of our test examples. We note that up to 34K nonlinear nonconvex problems are solved by ExaTron at each ADMM iteration.

6.2. Performance on a single GPU. Figure 5 depicts the average solution time of ExaTron for different sizes of batches of branch subproblems listed in Table 4.
The time on the y-axis is the average computation time in milliseconds taken by ExaTron to solve each batch within an ADMM iteration.

As illustrated in the figure, the performance of ExaTron generally scales linearly with respect to the batch size. This is expected since ExaTron solves the subproblems inside a batch in parallel, meaning that increasing the batch size would linearly increase its computation time as well. Moreover, all the subproblems share the same formulation (6.2), differing only by the parameter values.

We note that there are two main factors contributing to the computation time of a batch: (i) the number of subproblems per batch (i.e., batch size) and (ii) the average time for ExaTron to solve each subproblem in a batch. The latter is related to the level of difficulty of the subproblems in a batch. Although two batches are of the same size, one batch can show more computation time than the other if the subproblems in that batch are more difficult to solve than those in the other. In our case, the difficulty of batches was not significantly different from each other so ExaTron showed a linear scaling over them. However, this is not always the case, as demonstrated in subsection 6.3, where we present a load imbalance on multiple GPUs that was caused by different level of difficulties among batches.

Fig. 5: Performance of ExaTron on a single GPU

Fig. 6: Performance of ExaTron on multiple GPUs
6.3. Performance on multiple GPUs. We can achieve greater speedups of ExaTron by employing multiple GPUs. The GPU-aware message passing interface (MPI) with Nvidia’s GPUDirect supports direct GPU-GPU communication by allowing GPUs to directly send or receive data from and to the device memories, without staging through host memory. We employ such a GPU-aware MPI to communicate between GPUs that are connected via NVLink on Summit. We note that the MPI communication can become more expensive when we start to use more than 3 GPUs, since this involves cross-socket communications. This degradation of communication time will be observed in the experiments later in this section.

Figure 6 shows the speedup of ExaTron when we parallelize the computation across different GPUs (up to the 6 GPUs available on a node in the Summit supercomputer). Branch problems are evenly dispatched among 6 MPI processes in the order of branch indices, and the speedup is computed based on the timing of the root process. At each ADMM iteration, the root process distributes variable values over multiple GPUs, solves its own batch, and gathers variable values back from other GPUs. Therefore, the timing of the root process represents the synchronous time for all the MPI processes to finish their own solves, and communicate their solutions back to the root process.

As expected, we obtained a larger speedup as we increase the number of GPUs. In the case of 19402goc, it shows almost a perfect linear scaling: we obtained 5 times faster computation time when we used 6 GPUs. In general, a larger speedup is achieved for larger test instances, because the speedup is related to the maximum number, say $N$, of subproblems that a single GPU can solve in parallel. Therefore, the size of a batch divided by $N$ will determine the upper bound on the number of GPUs that we can benefit from employing them. This explains why the speedup is saturated for smaller batches, for example 2868rte and 6515rte. We also note that the slope of the changes of the speedup was slightly decreased when we used more than 3 GPUs. We think this is because of the increased communication cost for cross-socket communications.

In addition to the size of a batch, another factor contributing to the speedup is the load balance among GPUs. As we briefly discussed in subsection 6.2, the level of difficulty of problems affect the computation time of a batch. Although each GPU is assigned to a batch of the same size, the speedup may be degraded if the computational load is imbalanced in terms of the level of difficulty between GPUs. In our case, the level of difficulty of a batch is measured by its solution time on a GPU. Since the root process operates synchronously, some GPU may finish its computation much earlier than others, making it idle until all the other GPUs finish their work.

We quantify this load imbalance of our data using the metrics described in [33, 18] and present their values in Table 5. The percent imbalance of a problem instance $p$—where $p$ is divided into batches on GPUs in our case—at iteration $k$ is defined as

\[
\nu_{pk} := \left(\frac{t_{pk}^{\text{max}}}{\bar{t}_{pk}} - 1\right) \times 100%,
\]

where $t_{pk}^{\text{max}}$ and $\bar{t}_{pk}$ are the maximum and mean computation times of a batch among GPUs at iteration $k$. We define $\nu_p = \max_k \nu_{pk}$, $\nu_p = \min_k \nu_{pk}$, and $\nu_p^{\text{mean}} := \text{mean}_k \nu_{pk}$. Hence, a smaller $\nu_p^{\text{mean}}$ implies that the load is balanced better than the case with a larger $\nu_p^{\text{mean}}$.

Table 5 clearly shows that the workload of 19402goc among GPUs is much better balanced than the others, providing another insight into its superior speedup. We note that the load balance of 13659pegase is worse than that of 9241pegase. This
explains why 13659pegase shows a very small increase of the speedup compared to 9241pegase, although its size is about 25% larger than that of 9241pegase.

Table 5: Load imbalance metric values

| Data       | \( \nu_p \) | \( \nu''_p \) | \( \nu^{in}_p \) |
|------------|-------------|-------------|-----------------|
| 2868rte    | 481.58%     | 2.85%       | 46.76%          |
| 6515rte    | 480.88%     | 0.54%       | 37.02%          |
| 9241pegase | 475.48%     | 1.40%       | 32.79%          |
| 13659pegase| 469.64%     | 5.98%       | 45.76%          |
| 19402goc   | 469.79%     | 2.14%       | 9.04%           |

Fig. 7: Load imbalance among GPUs for 13659pegase

Figure 7 presents a verification of the load imbalance of 13659pegase problem. It depicts a heatmap where we sample 1,000 ADMM iterations for visibility and the value corresponds to the computation time in milliseconds of a batch that is assigned to each GPU. As we observe in the figure, the computation time of the second and the third GPU was almost twice more than the others throughout the iterations. An asynchronous solve combined with a load balancing scheme is our future research topic to alleviate this load imbalance issue.

6.4. Performance comparison: CPU vs GPU. We next compare the performance of ExaTron between a parallel CPU implementation and the GPU implementation. This experiment was run on a single Summit node with 6 GPUs and 40 CPUs. For the CPU run, we use the MPI library to implement the parallel communication between the CPU processes. Similar to the experiments for multiple GPUs in subsection 6.3, we measured the timing of the root process for CPUs that includes the cost for synchronizing distributed solves over the 40 cores.

Since ExaTron can operate in either CPU or GPU mode, the same ExaTron package was used to test the CPU implementation. We note that both modes implement the same algorithm described in Algorithm 3.1, hence the sequence of calling their functions is identical. The only differences are in the implementation
of such functions—especially functions listed in Figure 2—where we follow our kernel design principles described in section 4 for the GPU implementation.

In Figure 8, the computation time of the CPU implementation shows a linear increase of with respect to the batch size. However, the average computation time increases faster than that of the GPU implementation: the computation time of ExaTron on 6 GPUs is about 9–35 times faster than the CPU implementation using 40 cores. Most of the speedup relates to the GPU’s massive parallel computation capability.

7. Conclusion. Large-scale nonlinear programming can be tackled through Lagrangian decomposition. Such decomposition results in a batch of nonlinear programming problems to solve at each iteration of its algorithm. We have developed ExaTron for efficient batched nonlinear programming using GPUs. It implements a trust-region Newton algorithm for bound constrained nonlinear programming problems and works fully on GPUs without data transfers between CPU and GPU. This removes expensive data transfer cost which could be significant especially when the size of problems in the batch is small. We presented our design principles and implementation details for our kernel function for efficient utilization of GPUs. Experimental results over large-scale ACOPF problems decomposed into components through ADMM algorithm provided linear scaling of computation speed of ExaTron with respect to the batch size and the number of GPUs. On a single Summit node, the algorithm running on GPUs achieved more than 35 times speedup than on CPUs.

We conclude this paper by discussing several directions of future work. First of all, we plan to apply the ADMM algorithm with our GPU batch solver for solving multi-period multi-scenario optimal power flow problem. We found that only minor modifications are required to extend the current ADMM algorithm for solving the problem, while requiring more computing resources (i.e., multiple nodes and GPUs). Moreover, as we introduce more GPUs, a better design for MPI communication will be required. In particular, we have already observed that the computational load can be significantly imbalanced over multiple processes. Advanced asynchronous algorithms (e.g., [18]) will be required to alleviate the load imbalance.

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