Electromagnetic design methods in systems-on-chip: Integrated filters for wireless CMOS RFICs *(invited)*

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Abstract: We present general methods for designing on-chip CMOS passives and utilizing these integrated elements to design on-chip CMOS filters for wireless communications. These methods rely on full-wave electromagnetic numerical calculations that capture all the physics of the underlying foundry technologies. This is especially crucial for deep sub-micron CMOS technologies as it is important to capture the physical effects of finite (and mediocre) Q-factors limited by material losses and constraints on expensive die area, low self-resonance frequencies and dual parasitics that are particularly prevalent in deep sub-micron CMOS processes (65nm-0.18µm). We use these integrated elements in an ideal synthesis of a Bluetooth/WLAN pass-band filter in single-ended or differential architectures, and show the significant deviations of the on-chip filter response from the ideal one. We identify which elements in the filter circuit need to maximize their Q-factors and which Q-factors do not affect the filter performance. This saves die area, and predicts the FET parameters (especially transconductances) and negative-resistance FET topologies that have to be integrated in the filter to restore its performance.

1. Introduction
Filter synthesis and design is a very mature discipline [1] which still encompasses many novel areas of application. In each specific area, new physical properties of the technology realizing the filters may have to be considered and new methodologies accommodating and optimizing these properties may have to be invented and incorporated within the design cycle, see for example [2], [3], [4]. Standard CMOS technology is a demanding environment for designing integrated (on-Chip) microwave-frequency filters. Filter realization runs into several difficulties: For on-chip CMOS integration, compatible with low cost, die area is very expensive. Hence, a microstrip filter realization would end up with very large die areas. Alternatively, a filter realization containing many active elements could end up having substantial noise levels. In this paper we will present a promising filter realization that is “almost passive”. This means that the filter elements are on-chip lumped elements of maximum Q-factors realizing an ideal circuit topology. Deviations from the ideal behavior can be compensated through a complete high-frequency characterization of the integrated passives, an identification of the leading sources of the deviations per filter topology and the introduction of tuning and active elements compensating the leading sources of deviation. Even though we will illustrate the methods with a particular example, the procedures and models applying to the individual passives are quite general, and the design flow described here can be applied to any desired filter response.
2. Electromagnetic Design issues

In this paper we will choose the example of designing an on-chip CMOS pass-band filter of a 100MHz band centered at 2.45 GHz with high out-of-band rejection, appropriate for Bluetooth and WLAN devices. We will use design results on 0.18µm CMOS technology. To keep the discussion somewhat general, we will use representative properties of CMOS-integrated passives, rather than specific layouts. Throughout this paper we will rely on full-wave electromagnetic simulations for the analysis of relevant passives. In particular, we will use Method-of-Moments codes, that numerically solve the full set of Maxwell’s equations in the frequency domain, for arbitrary frequencies [5]. Since these appropriately convergent solutions, are the exact scattering solutions of the problem, they contain all the physics characterizing the underlying foundry technologies that affect the frequency response of the passive device. Four fundamental problems facing a passive filter design on CMOS technologies emerge:

1) Realizability on CMOS of ideal component values, following traditional ideal synthesis rules (e.g., Chebychev) for narrowband passband filters. Such syntheses yield excessively low shunt inductor values (0.1-0.2 nH), which are very hard to realize on CMOS reliably.

2) Physical loss coming from the metal loss of on-chip metal traces that have necessarily small cross sectional area. Further, a significant loss coming from the Si substrate itself.

3) Detuning coming from electromagnetic resonances at high frequencies. Each of the lumped elements involved is realized on-chip as a resonator, which can be described in circuit language as the “leading” lumped element the designer intended plus the “parasitic” elements coming from the integration. The leading element can always be found as the DC limit of the frequency-dependent impedance of the corresponding device realized on-chip. We will show that the parasitic elements can be found by modeling the input impedance or 2-port impedance matrix of the device as a resonator, i.e., from DC up to and including its self-resonance frequency. This is in contrast to extended current practices where such elements are fitted by frequency-dependent circuit models that only fit the impedance throughout a narrow band around the chosen operation frequency. The advantage of the broadband models we present is that all parasitic elements follow from these broadband models, and that these models are frequency-independent. This is essential for designing correctly integrated filters that cascade several of these on-chip elements, as parasitics interact differently at different frequencies of the filter operation and should be accounted globally in a frequency-independent, yet accurate, way.

4) Asymmetric response functions. This phenomenon is very pronounced on devices integrated in multi-layered CMOS technologies, because most 2-port passive devices are physically asymmetric between the two ports. This is because in CMOS the top metals are thicker than the bottom ones and the latter are closest to the substrate than the former and interact differently with it. Hence, $S_{11}(f)$ will be a very different function than $S_{22}(f)$, implying different parasitics, and a different circuit model for the device, according to whether one grounds port 1, port 2, or connects the device in series. This is in stark contrast to an off-chip passive device, where the two ports are electromagnetically symmetric.

We will illustrate each of these points within the limited space provided, summarizing along the way the basic dependence of the electromagnetic results that feed the four design areas mentioned above, on underlying CMOS technology features.

Regarding detuning/parasitics and port asymmetries (items 3 and 4 above), and as is evident from figure 1a, CMOS technology contains a variety of metal levels of different thickness and different proximity to the substrate and poly layers. These layers have substantially different properties than the low-loss dielectrics separating the upper metal layers. Therefore, metal-to-metal capacitance and loss through the substrate depends on the metal level(s) populated. This shows up in the design of single-ended inductors by the dramatic difference in the input impedance and self-resonance frequencies between the top and bottom ports in figure 1b, with the other port grounded. It also shows in the fact that differential inductors, such as the one shown in Figure 1c, despite the fact that their two ports are designed with a high degree of symmetry, develop a center ground that does not coincide with the mid-point of the total metal track length. This is due to the fact that geometrical symmetry of such
designs is never complete, since many signal paths are nested and interconnected by vertical vias from layer to layer. Symmetry-breaking due to metallization results in grounding center-taps that have to be located through accurate full-wave electromagnetic simulations.

Full-wave EM simulations are also indispensable for the accurate calculation of the self-resonant frequencies per port. This depends substantially on accurate calculation of the effects of the physical thickness of the metal traces, above and beyond a calculation of metal loss, which is usually done through a DC resistance and a frequency-dependent surface impedance. The reason is that tightly wound and vertically interconnected metal traces develop mutual capacitive coupling, very much dependent on the thickness, that reduces the self-resonance frequencies by 10% or more.

All these factors determine not only the self-resonant frequency but also the Q-factor as a function of frequency (Q-function), item 2 above. These physical parameters can actually be used as degrees of freedom to shape the Q-function at the design level, so that it reaches its maximum at the desired operating frequency, not near the (much larger) self-resonant frequency. As we show in figure 2b this is entirely possible and very desirable, especially for filter applications where we want inductors of maximum Q at the passband frequencies. To achieve such tailor-design of the Q-function, it is essential to rely on full-wave EM simulations, where all the physical parameters determining the Q-function are accounted for. In this report, we have used Method-of-Moment full-wave simulations with thick metal discretizations.

In figure 2a we show measurements of a 5 nH differential inductor. We plot the inductance function per port $i = 1,2$:

$$L_i(\omega) \equiv \text{Im}\left\{1 \over \omega(Y_{11} - Y_{12})\right\} \implies L_i = \lim_{\omega \to 0} L_i(\omega), \quad \omega = 2\pi f.$$  

We see excellent agreement between simulations and measurements, and between the two inductive functions, all the way up to self-resonance, indicating electromagnetic symmetry relative to the designed center-tap. In figure 2b we show the Q-functions of that inductor, specifically designed to peak at the range of 2.5-3.5 GHz, for use in a passband filter at 2.5 GHz. A maximum value of $Q=14$ is measured for the CMOS technology selected.

Another crucial issue for integrating such elements in an on-chip filter is the extraction of broadband circuit models correct up to the self-resonance frequencies of the elements. This is important because dual parasitics (capacitance for inductors and inductance for capacitors) should be correctly accounted for avoiding significant de-tuning of the filter, as we’ll show in the following section. We demonstrate that simple, irreducible circuit models are possible with the example of a single-ended inductor shown in figure 3. These correspond to the circuit model of figure 4a, and we see that the input impedance as a complex function of frequency can be fitted accurately from DC to self-resonance. Similar results hold for on-chip capacitors, using the circuit model of figure 4b. Obviously, when two or more ports are fed, slightly more complex circuit models are necessary. In general for $N$ ports, $N(N+1)$ real functions of frequency have to be fitted. However, the additions to the single-port topologies of figure 4 are based on extensions of these single-port circuits, capturing most of the physics of the technology.
3. A pass-band filter design example

In this section we summarize the design flow of a pass-band Bluetooth/WLAN filter integrated in 0.18\(\mu\)m technology. Figure 5a shows an ideal synthesis with CMOS-realizable elements terminated at high port impedances for insertion of the filter after high impedance stages. Similar synthesis is possible for 50-Ohm terminations. Figure 5b shows a differential version of the same filter, achieved by a 1:2 balun. In Figure 6a we show the response of the ideal filter, which meets or exceeds specifications for the performance of such filters, made out of discrete components on PCBs in Bluetooth/WLAN chipsets. The next step is to design the on-chip elements using full-wave EM analysis for capturing the parasitics and shaping the Q-function so that it peaks for frequencies at the

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Figure 2. (a) Measurement of \(L(\omega)_1\) and \(L(\omega)_2\) (solid lines) of a differential inductor calculated from ports 1, 2 to center-tap and a MoM EM simulation (diamonds). (b) Measured Q-factor, showing maximum values at frequencies of 2.5 – 3.5 GHz, much below the self-resonant frequency of 4.7 GHz.

Figure 3. (a) Measurement (m), broad-band (bb) and narrow-band (nb) circuit models for the inductance function of single-ended inductors. (b) Same as (a) for the real part of the input impedance.

Figure 4. Irreducible broad-band models of the single-ended (2nd port grounded) (a) inductor of Figure 3 (b) 4.7 pF capacitor self-resonating at 6 GHz.
passband. Then, from the EM simulations one extracts a broadband circuit model for each on-chip element as described above. This produces the schematic of figure 7a, which is an electromagnetically accurate CMOS version of the ideal design 5a. The response of 7a is shown in figure 6b. We observe that the on-chip passive filter has degenerated very badly relative to its ideal counterpart, due to the CMOS physics derived by the full-wave EM simulations and captured by the schematic of figure 7a. In particular, the filter is significantly detuned due to the dual parasitics, and the passband has degenerated to an unusable −25 dB.

The results of figures 6b and 7a are actually the end of the electromagnetic design cycle, which itself includes several cycles of convergence: Given a fixed die area, one can determine which inductors should have maximum Q-factors. Even though a-priori one would tend to treat all inductors equally, with respect to their losses, we will show that this is incorrect. Varying independently the resistors of the on-chip inductor equivalents, with the other elements of Figure 7a idealized, we show in Figs. 7b, 7c the filter response degradation for decreasing values of the series and shunt inductors respectively. Notice that a series inductor Q decrease to 10 drops the passband to the −2 dB level, which is acceptable in the industry, while the same decrease in the shunt inductor drops the passband to −19 dBs. Hence, for this topology, the shunt inductors have to have their Q’s maximized, while the series inductors can have a mediocre Q without much of a penalty, thus saving die area. With an accurate circuit description of the CMOS physics of the passives in place, we can derive negative-resistance FET topologies that cancel the loss of the shunt inductors only, as shown in Figure 7d.
Accurate values for the FET transconductances and other parameters also follow from the passive circuit, and are essential for the stable operation of the filter. The results in the end of the design cycle are shown in Figure 7e, where we observe an excellent reconstruction of the ideal filter response.

**References**

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