REAL-TIME DEEP LEARNING AT THE EDGE FOR SCALABLE RELIABILITY MODELING OF Si-MOSFET POWER ELECTRONICS CONVERTERS

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ABSTRACT

With the significant growth of advanced high-frequency power converters, on-line monitoring and active reliability assessment of power electronic devices are extremely crucial. This article presents a transformative approach, named Deep Learning Reliability Awareness of Converters at the Edge (Deep RACE), for real-time reliability modeling and prediction of high-frequency MOSFET power electronic converters. Deep RACE offers a holistic solution which comprises algorithm advances, and full system integration (from the cloud down to the edge node) to create a near real-time reliability awareness. On the algorithm side, this paper proposes a deep learning algorithmic solution based on stacked LSTM for collective reliability training and inference across collective MOSFET converters based on device resistance changes. Deep RACE also proposes an integrative edge-to-cloud solution to offer a scalable decentralized devices-specific reliability monitoring, awareness, and modeling. The MOSFET converters are IoT devices which have been empowered with edge real-time deep learning processing capabilities. The proposed Deep RACE solution has been prototyped and implemented through learning from MOSFET data set provided by NASA. Our experimental results show an average miss prediction of 8.9% over five different devices which is a much higher accuracy compared to well-known classical approaches (Kalman Filter, and Particle Filter). Deep RACE only requires 26ms processing time and 1.87W computing power on Edge IoT device.

1 Introduction

Power electronics systems are essential components of the energy-conversion process. It is expected by 2030, power converters will be used in 80% of applications in the generation, transmission, distribution, and consumer electronics [1]. Controllable power semiconductor devices play the most dominant role in the switching power converters. Operating at high current and voltage creates extreme stresses on the power devices, which often makes them the most susceptible...
components in the energy conversion process. Therefore, understanding, modeling and predicting the reliability models of the power converters are crucial for enabling emerging technologies and future applications such as electric vehicles, smart grids, and renewable energy.

Mathematically formulating and precise understanding of the physical degradation in high-frequency power converters is notoriously difficult, due to the system sophistication and many unknown non-deterministic variables. To solve this problem, a wide range of stochastical diagnostic and prognostics techniques have been proposed to address the reliability issues of a complex system in the design, fabrication, and maintenance process. The evaluation of these processes is beneficial to enable power convertors health management systems and resiliency for useful life estimation and reducing the risk of failures [2, 3]. Kalman filter and Bayesian calibration are two examples of classical time series modeling and prediction techniques. However, these approaches are often bounded to first-order models in isolation and are not able to bring the collective behavior of many devices with the same underlying physic to create an accurate algorithmic construct. Therefore, their prediction accuracy is very limited. Moreover, they have very limited scalability for emerging advanced technologies [4, 5].

Recent advances in deep learning open a new horizon toward smart and autonomous systems. Deep learning offers a scalable data-driven discriminative paradigm to understand, model and predict the behavior of complex systems by extracting the deep collective knowledge. With the new wave of the Internet-of-Things (IoT) and the feasibility of using the internet almost everywhere, there is a big chance for scalable device-specific real-time monitoring and analysis by pushing deep learning and advanced analytic computations from the cloud next to IoT devices (which also called edge computing) [6, 7]. In particular, the benefits of edge computing are much more pronounced for real-time reliability modeling and prediction of sophisticated physical and engineering systems such as power electronic converters.

This paper presents a transformative solution, which is called Deep learning Reliability Awareness of Converters at the Edge (Deep RACE)², for real-time reliability modeling and assessment of power semiconductor devices embedded into a wide range of smart power electronics systems. Deep RACE departs from classical learning and statistical modeling to deep learning based data analytics, combined with full system integration for scalable real-time reliability modeling and assessment. In this regard, it leverages the Long Short-Term Memory (LSTM) networks as a branch of Recurrent Neural Networks (RNN) to aggregate reliability across many power converters with similar underlying physics. Also, it offers real-time online assessment by selectively combining the aggregated training model with device-specific behaviors in the field.

To guarantee real-time scalable requirements, the Deep RACE presents an integrated cloud-edge platform in which, the cloud is responsible to aggregate different device reliability by training the LSTM network, while the inference is done at the edge next to the power devices. The interference at the edge (on-line) provides real-time feedback of the reliability modeling as well as active control and decision making for device proliferate. We have trained and implemented the proposed Deep RACE approach for five high-frequency MOSFET power converters. Our results demonstrate the Deep Race improves the misprediction by 1.98x and 1.77x compared to Kalman Filter and Particle Filter, respectively.

To the best of the author’s knowledge, Deep RACE is the first integrative solution for active reliability assessment of the high-frequency power converters based on real-time deep learning analytic. In this context, this paper moves beyond mainstream device modeling and traditional reliability analysis by combining advanced sensing solutions with cutting-edge deep learning and edge computing techniques. Although this paper primarily focuses on the reliability modeling of high-frequency MOSFETs, the proposed algorithmic construct and system level solution for real-time reliability and predictive maintenance can be extended to a wide range of semiconductor devices and engineering systems used in power conversion and smart energy systems.

The rest of this article is organized as the following: Section 2 briefly reviews the previous reliability approaches. Section 3 provides background on deep learning in particular deep RNN. Section 4 presents our proposed Deep RACE approach including LSTM-based machine learning and system-level integration for aggregated training and real-time inference. Section 5 presents the experimental results including comparison with existing approaches, and finally Section 6 concludes this article.

## 2 Related Work

This section briefly reviews the previous reliability approaches in power electronics, and discusses precursor identifier for power MOSFET degradations.

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²The Deep RACE is an open source project and its code is available at [https://github.com/TeCSAR-UNCC/Deep_RACE](https://github.com/TeCSAR-UNCC/Deep_RACE).
2.1 Reliability analysis/prediction in power electronics

The reliability approaches in power electronics systems have been developed in four broad categories: a) component level, b) damage accumulation, c) data analytics, and d) condition-based predictions. The first approach is not a prognostic-based since they consider the unit-to-unit difference and not the usage history [8, 9]. The second method offers more accurate tendency for an individual unit by using the accumulation of stress conditions over the time, although it needs experimental observation for the modeling [10, 11]. Data analytics focus on big-data mining for prediction based on the past usage history data and assign a predictive score as opposed to calculating a time to failure events [12, 13]. Lastly, condition-based prognostic methods rely on potential mode identifications and finding the root of the failure mechanism based on the individual behavior units of failure model physics[14, 15].

Several methods have been proposed for mean-life estimations like six sigma, fault tree analysis, state space, and filtering estimations [16, 17]. Due to increasing the large volume of data collected from smart devices, using the existing methodologies have some limitations on extracting the hidden patterns. Therefore, the necessity of applying deep learning algorithms for real-time system health monitoring is crucial. Few recent approaches have already demonstrated the significant benefits of deep learning based reliability monitoring and predictive maintenance in other engineering disciplines [18–20].

2.2 Precursor identifications in power MOSFET degradation

In the most comprehensive industry survey-based studies, power semiconductor devices (e.g., MOSFET) are responsible for at least more than 30% of the failures [21, 22]. The failure mechanisms in power MOSFET can be categorized into two extrinsic and intrinsic subcategories. The extrinsic failures include the transistor packaging issues and mainly summarized as a bond-wire lift, die solder detachment, and contact migration. Most of these studies verified that the bond-wire lift has a severe effect on the device failure over time [23, 24].

To evaluate device long-term reliability, the general approach is conducting an accelerated life test under power/thermal cycles, and continuously monitoring variations in electrical or mechanical parameters. Based on the most acceptable standards for device qualification in the industry, such as AEC-Q101 [25], and the state-of-the-art research, \( I_{ds(on)}, T_{j}, V_{th}, R_{th}, \) and \( R_{ds(on)} \) are the most common parameters for the device degradation tracking [8, 16, 26, 27]. \( I_{ds(on)} \), which refers to drain current at zero bias, can be used for early detection of die-level failures, \( T_{j} \) shows the device junction temperature and corresponds to thermal runaway failures, \( V_{th} \) shows the gate threshold voltage shifting, \( R_{th} \) is the thermal resistance of the device and represents device overheating mostly in the package level. Finally, \( R_{ds(on)} \) shows the device drain-source resistance, which represents both device degradation in the die and package level where inherently shows the device internal loss.

Fig. 1 illustrates the changes of \( R_{ds(on)} \) over time for five different MOSFET transistors (IRF520NPbf) extracted from the data set provided by NASA [28]. Although it may seem that these five transistors share a similar degradation pattern at the first observation, the deterioration pace and detailed behaviors are significantly varied across the devices with similar underlying physics. This is primarily due to diverse workloads, different environmental conditions, and varying manufacturing processes. In the next section, we discuss why the classical approaches are infertile to concurrently model the degradation of these five transistor devices. For the rest of this paper, we also consider these five data set to evaluate the performance of our proposed Deep RACE framework.

3 Motivation and RNN Background

In this section we explain the limitation of classical approaches for modeling of power device degradation. Then, we continue to elaborate more on vanilla RNN and its problem regarding modeling a complex time series data such as MOSFET \( \Delta R_{ds(on)} \) precursor.

3.1 Limitation of Classical Approaches

In the reliability-based prediction methods, the frequency of component failure is predicted based on a statistical model derived from acquired data in a laboratory environment or historical component usage if available. In a strict sense, these methods cannot be considered as prognostic methods due to unique unit-to-unit conditions and their specific usage history. Alongside, although theoretical approaches such as physics-of-failure [29] analysis are applied to identify the root of failure and drive the reliability model, these methods result in significant errors and are not applicable for unit-to-unit scenarios because of the complexity of power electronics systems and their operating conditions [16].

The other data-driven approaches, such as Kalman filter [30] and Bayesian calibration [13, 28], are predictive analytics which mostly focus on identifying the correlation of the experimental results, and the estimation of unknown variables.
and parameters. These techniques require an accurate failure model of a system to estimate the unknown mathematical parameters associated with a specific failure test; however, for new technologies, these methods cannot be effective due to the lack of precise failure model in the component as well as system level [15]. There is a high demand for solutions that address the algorithmic and system-level challenges for real-time scalable monitoring, modeling, and estimation of degradation behavior in power electronic transistors.

3.2 Recurrent Neural Networks

In contrast to classical approaches, this article proposes a holistic IoT system for hybrid condition-based prediction model which assesses the behavior of individual transistors based on both their usage history as inferred from sensed data and expected future load profiles. To achieve this, a data-driven model based on deep Recurrent Neural Network (RNN) is utilized at the edge, i.e. converter, for real-time device-specific reliability prediction and modeling; while the cloud infrastructure performs high-level metadata aggregation and analysis across many devices. At the time of Artificial Intelligence (AI) big-bang, we took advantages of a prominent model of RNN named LSTM to predict the transistor degradation. In our solution, the sensed resistance, and environment conditions will be sent to the cloud-side of the proposed framework to train and update the LSTM network models. Therefore, the models will be updated based on the current device operating condition.

The RNNs are a branch of neural networks specialized for analyzing and modeling complex time series. Following deep learning paradigm, RNNs need a fairly large dataset for training. The are very popular approach for natural language processing and object tracking over frames sequence. In a formalized RNN, sequence of data is notated by $X = [x_1 \ x_2 \ \ldots \ x_\tau]$ where $\tau$ is the number of input sequences. Fig. 2 formulates an RNN computation node, i.e. neuron, and its unrolling recurrent computation when $\tau = 4$. A neuron passes the information from the past to the current time by sharing the information and updating its cell state, $c$; therefore, this sharing process enables RNN to model a behavior of a time sequence. In a standard RNN cell with given input $X$, the cell output $Z = [z_1 \ z_2 \ \ldots \ z_\tau]$ is computed by Equations 1-4. In these equations, $\zeta(\cdot)$ and $\xi(\cdot)$ are nonlinear activation functions, $W_i$ is input weight, $W_c$ is the state cell weight, $W_o$ is the output weight, and $b_i$, $b_o$ are biases for input and output values, respectively.

$$i_t = W_i x_t + W_c c_{t-1} + b_i, \quad (1)$$
$$c_t = \zeta(i_t), \quad (2)$$
$$o_t = W_o c_t + b_o, \quad (3)$$
$$z_t = \xi(o_t). \quad (4)$$

Knowing $Y = [y_1 \ y_2 \ \ldots \ y_\tau]$ as the referenced output, the loss function is defined by (5). In (5), $L(z_t, y_t)$ can be considered as the squared error of a regression function or cross-entropy for the sake of classification. The ultimate goal
Unrolling

Figure 2: **Recurrent Neural Networks**: The schematic of standard RNN cell and its unrolling version for four input time sequence

of RNN learning is to minimize the cost function. This goal can be formalized by (6), which minimizes the introduced loss function by altering $\theta$, where $\theta$ is a network vector model which is described as: $\theta = [W_i \ W_c \ W_o \ b_i \ b_o \ c_0]$. 

$$L(Z, Y) = \sum_{t=1}^{T} L(z_t, y_t),$$

$$\arg\min_{\theta} L(z(\theta), Y).$$

Backpropagation through time (BPTT) is the mainstream approach to extract the proper weight factors of the RNNs to minimize the cost function across the trained data [31, 32]. For the vanilla RNN, a major issues associated with BPTT is the losing of cell sensitivity to the earliest inputs due to the chain of partial derivation. This phenomena is known as vanishing gradient problem and eventually prevents the network reaches to the earliest states in deep RNN [33]. More sophisticated versions of RNN network, such as LSTM cells, are proposed to address the sensitivity lost problem in the basic RNN networks. Based on that, in the next section, we describe our proposed reliability model based on the LSTM networks.

### 4 Deep Learning Reliability Awareness of Converters at the Edge (Deep RACE)

This section presents Deep RACE as an integrative framework of online real-time reliability awareness and modeling for power electronic devices. Deep RACE has two major aspects: (1) algorithmic principles for modeling the device reliability, and (2) system-level integration for real-time scalable reliability assessment. On the algorithm side, Deep RACE uses one of the major derivatives of RNN, called LSTM for aggregated training and device specific inference. On the system side, Deep RACE proposes an IoT-based edge-cloud computation platform which pushes the proposed LSTM-based reliability inference next to the individual power converters. In the following, we provide an in-depth explanation of both aspects.

#### 4.1 Algorithmic Constructs for Device Reliability Modeling

In this part, we first introduce the basics of LSTM cells for reliability modeling of power devices, and we continue to present our proposed reliability modeling network constructed out of the basic LSTM cells.

##### 4.1.1 Long Short-Term Memory Cells

For reliability modeling of power electronic converters, we propose using LSTM cells. In a nutshell, different deep neural networks recognize the patterns in two forms of spatial and temporal pattern depending on their structure. As an instance, Convolutional Neural Networks (CNN) are engineered in a form that they can distinguish spatial pattern, e.g. a dog or a face, existed in a picture. In the other hand, sequence data such as natural language data and time series, e.g. stock index have a temporal pattern that should be processed during a sequence of time. For our case, since we try to model $\Delta R_{ds(on)}$ data and it is intrinsically a time series, we leverage LSTM cells as the prominent version of RNN. The benefits of LSTM cells are in using the guided gates for selectivity remembering both short and long-term behaviors across many time series. The LSTM uses a subset of the cyclical node inside its cell known as “memory” in order to calculate the output based on the current input and its past status [34]. The LSTM selective memory sensitivity at large scale offers a systematic approach for reliability modeling of power electronic devices.

The LSTM cell contains three vectorized sigmoid ($\sigma$) functions, which each individual function operates as a gate and controls the flow of information passing through the cell — the input, output, and forget gates. Fig. 3 presents the internal structure of an LSTM cell. Each gate maps its input to $S = \{s_i | s_i \in [0, 1]\}$, where zero is a closed gate and
one means the gate is open. Moreover, the cell state (memory) is preserved by \( C \) as a candidate. The information of new candidates, which should be stored in the cell state, represented as \( \tilde{c} \).

\[
\begin{align*}
i_t &= \sigma(W_i \tilde{v}_t + b_i), \\
f_t &= \sigma(W_f \tilde{v}_t + b_f), \\
o_t &= \sigma(W_o \tilde{v}_t + b_o), \\
\tilde{c}_t &= \tanh(W_c \tilde{v}_t + b_c), \\
c_t &= f_t \odot \tilde{c}_t - 1 + i_t \odot \tilde{c}_t, \\
h_t &= o_t \odot \tanh(c_t).
\end{align*}
\]

With respect to LSTM cell visualization in Fig. 3, Equations 7-12 formulates the correlation between input and output per LSTM cell. In the equations, \( \tilde{v}_t = [\tilde{x}_t, \tilde{h}_{t-1}] \), \( \odot \) is Hadamard or element-wise matrix product, and \( \theta = [W_i, W_o, W_f, W_c, b_i, b_o, b_f, b_c, c_0] \) is the network model that should be trained. The input gate (7) decides what portion of current input with which degree should be stored in cell memory, while forget gate (8) chooses which portion of memory should be erased. In the other hand, new information, \( \tilde{c} \), will be mined by (10), and the cell memory will be updated by (11). Moreover, the output gate (9) decides which part of cell memory should affect the LSTM output at time \( t \), and finally the LSTM output value is calculated in (12).

### 4.1.2 LSTM-Based Device Training Network

LSTM-based neural network needs to be designed to properly reflect \( \Delta R_{ds(on)} \) propagation with enough depth to capture complex power converters behaviors, and thus learning deep behavioral patterns across many devices. A deep LSTM network should have sufficient depth to build up the progressive pattern recognition of sequential data in both coarse and fine grain directions.

As it mentioned in Section 2.2, we consider the trajectory resistance of drain-source of power MOSFET during ON time (i.e. \( \Delta R_{ds(on)} \)) as the precursor of device failure degradation. As \( \Delta R_{ds(on)} \) is intrinsically a time series, we design the model by using deep LSTM network, where the training is developed by aggregating data from different devices having the same technology. A batch of samples is created for each training iteration. Therefore, for predicting the next \( n \) samples of \( \Delta R_{ds(on)} \) based on the provided last input sequence \( \tau \), the batch should consist of \( \Delta R_{ds(on)} \) with the size of \( (\tau + n) \). Fig. 4 presents the batch tensor configuration per each iteration. The dimension of vector \( R_{\text{num}}^k \) is characterized based on the input size shown by \( k \), where \( n \) is the available devices for training, and \( t \) is the sequence. In order to prevent any sort of biases in training the LSTM, we selected randomly a vector sequence with the size of \( (\tau + n) \) from the \( \Delta R_{ds(on)} \) samples per each device. Increasing the number of devices, \( (m) \), per each batch helps the network to generalize the modeling of complex degradation properly, which results in higher accuracy of the predicted trajectory.
For designing of deep LSTM network, we need to also consider number of hidden layers. The number of hidden layer is the dimension of vectors generated in equations (7)-(12). The vector size can be changed by altering the weights and biases tensor shape defined in equations (7)-(10). Increasing the hidden layer is interpreted as increasing the “memory” size of the LSTM and its capacity to learn existing complex pattern in a signal.

At the same time, building a very deep LSTM network is not a viable solution due to lack of large data-set to trained all LSTM cells once at the same time. The BPTT often failed to train a large flat LSTMs network without any patriarchy. As the result, the alternative solution is stacking multiple LSTM networks (which called Stacked LSTM) to create more complex and deeper network with offering hierarchical modular layers over a very deep flat network. In our proposed network, we suggest developing a stacked LSTM to generalize the behavior complexity of power electronics convertor without the need for a very large data-set. As the result, number of stacked layers is the other parameter to increase the complexity of the LSTM network. Here, by stacking the cell up together in a way the $h_t$ of one cell is used as an input to its top adjacent cells. Fig. 5 shows an architecture of the deep LSTM network with the stacked layer size of $\ell$.

Since the output vector $h_t \in [-1, 1]$, we need to de-normalize the deep LSTM network output to actual system measurement. Therefore, a dense layer is added to the output of stacked LSTM to map $h_t$ to the predicted $\Delta R_{ds(on)}$ at the time $t$ as shown in Fig. 6. Based on modified deep LSTM structure, the network models are described as:
Algorithm 1: Training the deep LSTM network

Input: $X_{\text{training}}, Y_{\text{training}}, X_{\text{test}}, Y_{\text{test}}, \tau, m, n, \ell, k, \epsilon, c_{\text{th}}, t_{\text{max}}$

Output: $\theta_\lambda; 1 \leq \lambda \leq \ell, \theta_d$  

1. $\text{computation\_graph} \leftarrow \text{LSTM}(\text{hidden\_layer}, \ell)$  
2. $\text{error} \leftarrow \infty$  
3. $\text{min\_error} \leftarrow \infty$  
4. $j \leftarrow 0$
5. $\text{init\_rand}(\theta_\lambda, \lambda \in [1...\ell])$  
6. $\text{init\_rand}(\theta_d)$
7. while ($j \leq t_{\text{max}}$) or ($\text{error} \geq c_{\text{th}}$) do
8.  
9.  
10. $\text{error}_{\text{training}} \leftarrow \mathcal{L}(\Delta R_{\text{ds(on})}, Y_{\text{batch}})$
11.  
12.  
13.  
14.  
15.  
16.  
17.  
18.  
19.  
20. end while

$\theta_\lambda = [W_{\lambda_1}, W_{\lambda_2}, W_{\lambda_3}, b_{\lambda_1}, b_{\lambda_2}, b_{\lambda_3}, c_{\lambda_0}], 1 \leq \lambda \leq \ell$, and $\theta_d = [W_d, b_d]$, where $\ell$ is the stacked layer size. Each LSTM cell will be trained at the cloud, and network model will be transferred to the edge next to the transistor device for real-time prediction. Acquiring proper values for the LSTM network parameters can be done by exploring the design space in regard to system constraints (e.g., system accuracy, processing time, and power consumption) [35].

Figure 6: The proposed deep LSTM network model: A dense layer is added to the deep stacked LSTM to map $h_t$ to on-line measured $\Delta R_{\text{ds(on})}$ at time $t$.

4.2 Proposed IoT Framework

In this subsection, we explained the system integration to realize the proposed LSTM reliability modeling constructs through an IoT-based cloud-edge platform.

4.2.1 Data training and batch aggregation on the cloud

One key aspect of Deep RACE is an integrative cloud-edge system for scalable real-time reliability monitoring, assessment, and prediction. Fig. 7 shows the system architecture of Deep RACE based on the cloud-edge solution training on the cloud and real-time sensing and inference for reliability monitoring and health assessment on the edge nodes. The cloud is the centralized computing node for data aggregation and training of proposed LSTM algorithm across many power electronic transistors with similar underlying physics. The cloud stores the initial sampled dataset
(e.g., voltage, current, and device temperature) collected from devices under stress test for initial training. At the same time, it continuously receives new information and sample data from running devices for improving the accuracy of reliability modeling and prediction. The edge nodes are IoT devices which use local computing power to perform the real-time reliability monitoring, and prediction (deep learning inference). The edge nodes rely on the pre-trained models that have created during the training phase on the cloud.

Figure 7: The Deep RACE Framework: The proposed solution accumulates the knowledge of power transistor degradation model on the cloud-side by training the LSTM network, while real-time prediction and inference is accomplished on the edge side.

In this context, the edge nodes and cloud continuously interact and exchange information. The Edge nodes, while performing real-time reliability assessment, collect and update the cloud with the properties of the transistors for future training. The cloud also updates edge nodes with new reliability models (LSTM models) to increase the confidence interval of the prediction, and estimate the remaining useful life of the devices. To increase the confidence interval of the power MOSFET devices and the system operation, a predefined threshold $\Delta R_{t}$ can be defined based on system requirement. Once the error of predicted device resistance $\Delta R_{\text{DS(on)}}$ is greater than the $\Delta R_{t}$, the network models will be automatically updated through training the network on the cloud server.

Algorithm 1 describes the training procedure on the cloud side. The computation graph is the deep LSTM network structure. At first, the network models are initialized from a truncated normal distribution. $X_{\text{batch}}, Y_{\text{batch}}$ are generated based on the input size, input sequence, output sequence, and the number of devices. Next, computation graph predicts the $\Delta R_{\text{DS(on)}}$ according to its current network models and generated training batch. The models will be updated through the back-propagating error from the output of computation graph to its inputs.

During training phase of our proposed LSTM algorithm, and in general deep learning models, one major source of error would be over-fitting. In order to prevent the over-fitting problem, we have created a test batch ($x_{\text{test}}, y_{\text{test}}$) to predict $\Delta R_{\text{DS(on)}}$ of the test device based on the updated network model. Next, the test batch error will be compared against the previous error values and if it has the minimum value, the network model will be saved.

4.2.2 Real-time edge analysis

The edge converter has its own local controller equipped with an embedded SoC for the purpose of predicting the power transistor degradation. The $\mu$-controller unit is responsible of modulating the gate signals for the power converter control, and continuous monitoring of the voltage, current, and temperature of power converters. The sampled data also will be transferred to the cloud, which performs the reliability analysis (training phase) for each edge node. The SoC of the edge runs inference section of the deep LSTM, equations (7)-(12), and estimates the trajectory device resistance, $\Delta R_{\text{DS(on)}}$, based on the received trained network models from the cloud. Based on the predicted $\Delta R_{\text{DS(on)}}$, controller can leverage load-sharing [36] method through the system level control in modular converters or cascaded architectures in many applications such as distribution generation systems, data centers, and the electric vehicles in order to decrease the degradation pace until the appropriate action is taken.

Fig. 8 visualizes the scalability of Deep RACE when a new edge is added to the framework. At first, the edge node sends the voltage, current, and temperature samples to the cloud-side. The samples will be used for two purposes: (1) as training sets for the other nodes, and (2) as test sets in order to prevent over-fitting phenomenon during training process.
of the LSTM network. Then, network models will be sent back to the edge for the purpose of $\Delta R_{ds(on)}$ prediction. As more new devices added to the framework, the prediction error will be decreased as we demonstrated in the next section.

5 Experimental Results

The performance of proposed real-time reliability analysis was examined for training the data and applying the Deep RACE. This section describes the testing scenarios, the hardware setup, and the experimental results.

5.1 Experimental training of power transistors

On the cloud server, we used Intel Xeon CPU E5-2640 to train the deep LSTM network, where we initially modeled Si-power MOSFETs. The experimental data sets for both training and testing of the power MOSFET (IRF520NPbf) are provided from NASA dataset [28]. The Deep RACE predicts a new transistor degradation behavior based on the trained system without any prior knowledge in advance. In our experiment, the Deep RACE is trained to estimate the next 104 samples. For the application with higher window resolutions (i.e. higher output sequence), the network input sequence should also be increased to minimize the prediction error. Table 1 summarizes the deep LSTM network parameters. Based on the network configuration, we have also measured the training time on the cloud server. Table 2 summarizes the training time on the cloud side.

| Item | Parameter | Description | Value |
|------|-----------|-------------|-------|
| 1    | $k$       | Input size  | 1     |
| 2    | $\tau$    | Input sequence | 21    |
| 3    | $e_{th}$  | Error threshold | $5 \times 10^{-5}$ |
| 4    | $n$       | Output sequence | 104   |
| 5    | $i_{\text{max}}$ | Maximum iterations | 1000 |
| 6    | $\epsilon$ | Number of hidden layer | 64   |
| 7    | $\ell$    | Number of stacked layer | 4    |
| 8    | $m$       | Number of device for training | 4    |

Figure 8: The scalability of Deep RACE: As new edge is added to the framework, its extracted $\Delta R_{ds(on)}$ is transferred to the cloud to be used both as training data set (for other devices) and test data set to prevent over fitting problem.
We used Google TensorFlow framework to implement our stacked LSTM network model. Each LSTM cell is instantiated by calling `tensorflow.contrib.rnn.LSTMCell` function where the number of “hidden layer” is passed as an argument to this function. In the next step, an array consists of `LSTMCell` with the size of “stacked layer” is generated. Then, the array will be passed to the `tensorflow.contrib.rnn.MultiRNNCell` function to create the stacked LSTM network. The network unrolling is accomplished through `tensorflow.nn.dynamic_rnn` function. We defined Mean Square Error (MSE) (13) as an objective loss function, and used `tf.train.AdamOptimizer` method to minimize the function:

$$MSE = \frac{1}{n} \sum_{i=1}^{n} (y_i - z_i(\theta))^2,$$

where $z_i(\theta)$ is the predicted output trajectory from the Deep RACE, and $y_i$ is the actual measurement of the device resistance.

| Item | Description | Value |
|------|-------------|-------|
| 1    | Training size/Iteration | $m \times k(\tau + n) = 500$ |
| 2    | CPU Cores | 32 |
| 3    | GPUs | nVidia Tesla P100, and nVidia TITAN V |
| 4    | Elapsed time | 596 Seconds |

5.2 Edge Node Hardware Setup

We also developed a low-power edge computing system for real-time monitoring and reliability assessment. The edge computing node is based on nVidia TX2 board as the state-of-art embedded SoC with GPU compute units for edge device. As we explained, the inference part of Deep RACE is implemented on the edge, since the cloud is responsible for aggregated training of the proposed structure.

Fig. 9 shows the prototype of Deep RACE hardware realization at the edge. In this system, µ-controller controls the power converter, and the voltage, and current of the power semiconductor are captured and then transferred to the TX2 board for edge analysis. For the safety purpose, the automated supervisory control is designed for data collection from the switching converter and also protects the system operation if the power conversion deviates more than 5%.

Figure 9: **Experimental Verification**: The hardware realization of Deep RACE including the high-frequency power converter controller, and the SoC-TX2 for edge computation. The supervisory control is designed for the safety protection.

5.3 Reliability Modeling and Prediction

We created five different scenarios per each device in order to evaluate the scalability and robustness of Deep RACE. As an example, the trajectory resistance for Dev#5 is predicted based on learning degradation model from Dev#1 to Dev#4.
Then, recursively we reinitialized all network models from truncated normal distribution again, and we substituted the other devices to predict a new unknown transistor resistance variations from scratch. Therefore, the Deep RACE is challenged to predict a completely new and unknown device based on aggregating knowledge from other power devices at each scenario. We verified the system characteristics from acquired experimental results in two forms of MSE and error distribution. Table 3 shows prediction MSE of the selected devices. While the training process is performed in the cloud, we evaluated the prediction of the device resistance variation at the edge.

Fig. 10 illustrates the Deep RACE prediction performance for defined five scenarios and clarifies the scalability of the proposed algorithm. Although the apparatus behavior of each power device degradation looks similar, the microscopic observation of the transistors is different within the same time horizon. For an instance, the trained network for Dev#4 is expecting an exponential increment in the region of \( \Delta R_{ds(on)} > 0.02 \Omega \) based on aggregated training from Dev#1 to Dev#3, and Dev#5. This error can be further minimized through a new learning phase on the cloud.

Table 3: Prediction error for the power MOSFET transistors.

| Devices | #1   | #2   | #3   | #4   | #5   |
|---------|------|------|------|------|------|
| log(MSE)| -13.61 | -13.05 | -13.95 | -13.36 | -12.94 |

Figure 10: **Experimental results:** The resistance variation of given five power modules, which were predicted by Deep RACE method.

We also extracted the error distribution for five predicted devices by using:

\[
\text{Error}_{\text{diff}} = (y_i - z_i(\theta)),
\]

where \( z_i(\theta) \) is the predicted output trajectory from the Deep RACE, and \( y_i \) is the actual measurement of the device resistance (\( \Delta R_{ds(on)} \) in our model). Fig. 11 depicts that the average maximum error caused by Deep RACE method is less than 0.9%.

We extended our experiment to analyze the effect of training aggregation and scalability of multiple device data on accuracy of \( \Delta R_{ds(on)} \) prediction. In this case, we increased the number of devices per each batch during the training phase. Fig. 12 shows that MSE decreases with an exponential rate by increasing the number of devices in training batch. For each training set, we ran 1000 Monte-Carlo test for \( \Delta R_{ds(on)} \) prediction of three different devices, and
then the average of whole test sets is picked. These results indicate that our proposed approach can improve the prediction accuracy exponentially by increasing the edge node and power transistors through the life time of the system by accumulating knowledge about different device degradation during its usage, which demonstrates the scalability of our approach.

The region of $\Delta R_{ds(on)} < 0.02\Omega$ has linear behavior, therefore, the classical approaches (such as Kalman Filter, and Particle Filter) can predict the health state with higher accuracy; however, the prediction error increases after that for these methods. Since it is very crucial to detect the MOSFET resistance variation when $\Delta R_{ds(on)} \approx 0.05\Omega$, we calculated the average of error at the detection point ($\approx \Delta R_{5\%}$) for these methods by using (15):

$$\text{Error}_{\Delta R_{5\%}} = \frac{100}{m} \sum_{i=1}^{m} \frac{|\Delta R_{ds(on)_{mt5\%}} - (0.05)_{mt5\%}|}{(0.05)_{mt5\%}},$$  

(15)
where $m$ is the number of devices, $\Delta R_{ds(on)}$ is predicted value, and $t_{5\%}$ is the time when the first sensed value is 0.05Ω. The $\text{Error}_{\Delta R_{5\%}}$ results are summarized in Table 4. Our experiments indicate that the Deep RACE reduces the miss-prediction error at 0.05Ω by about 1.98x, 1.77x compared to Kalman Filter and Particle Filter, respectively.

| Method          | Kalman Filter [30] | Particle Filter [28] | Deep RACE |
|-----------------|---------------------|----------------------|-----------|
| Miss-prediction Error | 17.75%              | 15.85%               | 8.93%     |

### 5.4 Power consumption and processing time analysis

We also evaluated the power consumption and delay of the inference part of the network on embedded TX2 board. Table 5 summarizes the specification of embedded SoC. Since the TX2 has an embedded GPU, We considers two different scenarios to analyze the performance of Deep RACE. At first scenario, we set the tensorflow configuration to `device_count = {'GPU': 0}`, where no computation carried out at the embedded GPU, and in the second approach we made it ON. For the matrix size of 125 (input sequence + output sequence), it was observed that the CPU processed 3.2x faster than GPU for one device prediction. This performance degradation is because of data copying between CPU and GPU memory region – Note the DDR power consumption is higher for ‘GPU’: 1 scenario. In the other word, the amount of data is not enough for GPU to overlap the delay between data computation and movement. Increasing the number of devices that should be predicted per each edge node or increasing the prediction window resolution (output sequence) improves the performance for GPU since it carries out more computation than CPU per each data set. Table 6 summarizes the delay and power dissipation for two different cases.

| Module CPU | GPU CPU | DDR |
|-------------|---------|-----|
| Quad Cortex-A57 @ 2GHz | 256-core Pascal | 8GB LPDDR4 @ 1866MHz |
| Dual Denver2 @ 2GHz | @ 1300MHz |

| Module Power (W) | CPU | DDR | CPU+DDR | GPU Power (W) | DDR | GPU+DDR |
|------------------|-----|-----|---------|---------------|-----|---------|
| 1.07             | 0.80| 1.87 | | 0.166        | 0.90 | 1.06    |
| Delay (ms)       | 26  |     |         | 85            |     |         |

### 6 Conclusion and Future Work

This paper proposed a new solution as a collection of deep learning, edge, and cloud computing technologies to enable real-time high accuracy reliability modeling of high-frequency MOSFETs power converter devices. The proposed deep learning algorithm is based on LSTM algorithmic constructs for accumulating the degradation knowledge of different power MOSFET devices on the cloud server, and real-time inference at the edge. For the experimented results, we developed an entire integrated system of Deep RACE, including an embedded system system-on-chip implementation on nVidia SoC-TX2. The results demonstrated the real-time convergence of the system with about 8.9% miss prediction, with 26ms processing time.

In a broader perspective, the proposed research will have a fundamental contribution in the engineering of semiconductor devices and information processing by bringing recent advances in deep learning and edge computing for real-time predictive maintenance of emerging semiconductor devices. In this context, Deep RACE sets to move beyond mainstream device modeling and traditional reliability analysis (i.e. Weibull distributions, mean-time-to-failure, etc.) and looking to more applicable and accurate analytical tools through introducing advanced sensing solutions and combining it with cutting-edge deep learning techniques.
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