CIDAN: Computing in DRAM with Artificial Neurons

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Abstract—Numerous applications such as graph processing, cryptography, databases, bioinformatics, etc., involve the repeated evaluation of Boolean functions on large bit vectors. In-memory architectures which perform processing in memory (PIM) are tailored for such applications. This paper describes a different architecture for in-memory computation called CIDAN, that achieves a 3X improvement in performance and a 2X improvement in energy for a representative set of algorithms over the state-of-the-art in-memory architectures. CIDAN uses a new basic processing element called a TLPE, which comprises a threshold logic gate (TLG) (a.k.a. artificial neuron or perceptron). The implementation of a TLG within a TLPE is equivalent to a multi-input, edge-triggered flipflop that computes a subset of threshold functions of its inputs. The specific threshold function is selected on each cycle by enabling/disabling a subset of the weights associated with the threshold function, by using logic signals. In addition to the TLG, a TLPE realizes some non-threshold functions by a sequence of TLG evaluations. An equivalent CMOS implementation of a TLPE requires a substantially higher area and power. CIDAN has an array of TLPEs that is integrated with a DRAM, to allow fast evaluation of any one of its set of functions on large bit vectors. Results of running several common in-memory applications in graph processing and cryptography are presented.

Index Terms—Artificial neuron, Processing In-Memory, In-Memory Computing, Bulk Bitwise Operations, DRAM, Memory Wall, Memory Bandwidth, Energy

I. INTRODUCTION

The throughput of traditional Von Neumann architectures is severely limited by the bandwidth between CPU and memory due to the increasing gap in the performance of both the units. This well-known issue, often referred to as the "memory wall", degrades the throughput of many high bandwidth applications that rely on bulk bitwise operations such as machine learning [1], database management [2], encryption [3] etc. Over the last two decades, numerous researchers have proposed solutions to reduce the performance gap between the memory and the CPU. One category of solutions deals with improving the data bandwidth between memory and CPU. Examples of this category include double data rate (DDR) memory architectures and 3-D high bandwidth memory (HBM) architectures. While these solutions improve the throughput of the conventional memory, the greater improvement in CPU performance hasn’t diminished the memory-wall significantly. Another category of solutions involves increasing the size of the on-chip cache and introducing in-cache computations [4], [5]. However, this method is limited by the amount of cache memory that can be added to the CPU chip. The third category of solutions is commonly known as processing-in-memory (PIM) architectures [6], [7], [8]. The idea here is to perform some computation within the memory and not involve the CPU in these computations. This solution has the potential to exploit the maximum parallelism of access inside the memory and can accelerate a plethora of applications. PIM architectures can reduce the number of data transactions on the channel connecting the CPU and the off-chip memory. Accordingly, PIM is one of the best-known methods to bypass the communication bottleneck, i.e., memory wall problem between CPU and memory. PIM offers unique opportunities to improve the parallelism and throughput of rapidly increasing highly parallel applications. Hence, PIM is an active and growing area of research.

In general, PIM architectures can be classified as mixed-signal PIM (mPIM) and digital PIM (dPIM) architectures. The dPIM architectures can be further classified as internal PIM (iPIM) and external PIM (ePIM).

The mPIM architectures compute in the analog domain and convert the result into a digital value using an analog to digital converter (ADC). A few works representative of mPIM are [8], [9], [10]. mPIM architectures are based on either SRAM or non-volatile memories. They are extensively used for machine learning applications to perform multiply and accumulate (MAC) operations in parallel. mPIM architectures approximate the result as the accuracy depends on the precision of the ADC.

The iPIM architectures [6], [11], [12], [13] perform logic operations inside the memory array on one or two rows. iPIM architectures use internal DRAM operations with slight modifications to the memory array or the sense amplifier to achieve bitwise logic operation.

Due to the advancement in the memory technology to the 20nm node and the use 2.5D chip integration, a high bandwidth memory (HBM) has become possible. HBM uses bank-level parallelism to provide high bandwidth to the CPU. HBM has an even higher internal memory bandwidth which external PIM (ePIM) architectures exploit. The ePIM architectures embed digital logic outside the memory array but on the same die as the memory to use vast internal parallelism for machine learning applications. Recently DRAM makers SK-Hynix [7] and Samsung [14] introduce 16-bit floating-point processing units inside HBM. Though the existing PIM architectures can deliver much higher throughput as compared to the traditional CPU/GPU architectures [13], they suffer from either loss of precision (mPIM architectures), low energy efficiency or high area overhead (ePIM architectures), or low throughput on
complex operations (iPIM architectures).

This paper presents a different design of a PIM architecture, named CIDAN, which is a hybrid of the ePIM and iPIM designs. CIDAN introduces a new processing element, named threshold logic processing element (TLPE), that comprises of a threshold logic gate (TLG) (a.k.a artificial neurons or perceptron). A threshold function is a predicate involving a linear weighted arithmetic sum of its binary inputs. The implementation of a TLG within a TLPE is equivalent to a multi-input, edge-triggered flipflop that computes a subset of threshold functions of its inputs. The specific threshold function is selected on each cycle by enabling/disabling a subset of the weights associated with the threshold function, by logic signals. In addition to the TLG, a TLPE realizes some non-threshold functions by a sequence of TLG evaluations. CIDAN will be shown to substantially improve the energy efficiency and performance of state-of-the-art iPIM architectures. The main contributions of the paper are listed below:

- This paper demonstrates a novel integration of threshold gates (artificial neurons) in a DRAM architecture to perform bulk bit-wise operations such as NOT, (N)AND, (N)OR. This includes a novel structure for the threshold gate and its control circuit.
- An extensive comparison against the state-of-the-art PIM architectures is presented for several applications such as data encryption, graph processing, and DNA sequence mapping, which benefits immensely from the PIM architectures. Demonstrations include 3X improvement in latency and energy over state-of-the-art architectures.

II. BACKGROUND

A. DRAM: Architecture, Operation and Timing Parameters

The organization of DRAM in modern computers is shown in Figure 1. It consists of several levels of hierarchy. The lowest level of the hierarchy, which forms the building block of DRAM is called a bank. A bank contains a 2D array of memory cells, a row of sense amplifiers, a row decoder, and a column decoder. A collection of banks is contained in a DRAM chip. Memory banks in the chip share the I/O ports and an output buffer, and hence, only one bank per chip can be accessed at any given time. A group of DRAM chips is called a Dual-in-line memory module (DIMM). Additionally, a rank is a set of DRAM chips connected to the same chip select, which are therefore accessed simultaneously from a DIMM. When data needs to be fetched from the DRAM, the CPU communicates with the DRAM over a memory channel with a data bus that is generally 64 bits wide. Multiple DIMM’s can share a memory channel. Hence, a multiplexer is used to select the DIMM to provide data to the CPU over the memory channel. One rank of the DIMM provides data to fill the entire data bus. Note that all the DRAM chips in a rank operate simultaneously while reading or writing data.

A DRAM memory controller controls the CPU access to the DRAM and the data transfers between the DRAM and the CPU. Therefore, almost all the currently available in-memory architectures modify the technique used to access the data and extend the functionality of memory to perform logic operations. The controller issues a sequence of three commands to the DRAM: Activate (ACT), Read/Write (R/W), and Precharge (PRE), along with the memory address. The ACT command copies a row of data into the sense amplifiers through the corresponding bit-lines. Here, the array of sense amplifiers is called a row buffer as it holds the data until another row is activated in the bank. The READ/WRITE command reads/writes a subset of row buffer to/from the data bus by using a column decoder. After the data is read or written, the PRE command charges the bit-lines to VDD/2, so that the memory is ready for the next operation. After issuing a command, the DRAM controller has to wait for an adequate amount of time before it can issue the next command. Such restrictions imposed on the timing of issuing commands are known as timing constraints. Some of the key timing parameters are listed in Table I.

Due to the power budget, traditional DRAM architectures allow only four banks in a DRAM to be activated simultaneously, within a time frame of tFAW. The DRAM controller can issue two consecutive ACT commands to different banks separated by a time of tRRD. As a reference, a 1Gb DDR3-1600 RAM has tRRD = 7.5ns and tFAW = 30ns [15]. In Section III, the impact of these timing parameters on the delay in executing logic functions will be shown for the proposed processing-in-memory (PIM) architecture.

B. Prior Work on Logic Operations in DRAM (iPIM)

Currently available iPIM architectures such as Ambit [6] and ReDRAM [13] extend the operations of a standard DRAM
to perform logic operations. A representative diagram of Ambit operation on three rows is shown in Figure 2 (left). Its operation is as follows: DRAM commands (ACT, PRE, etc.) are issued to fetch the operands, perform the logic operation, and then write back the result. It operates simultaneously on three rows which are activated using a special row decoder using triple row activation (TRA) operation. When three rows are activated simultaneously i.e., WL_A, WL_B, and WL_C are turned ON, the capacitors are connected to the bit-line (BL). The charge in the capacitors used to store the values and the precharged BL (at \( \frac{V_{DD}}{2} \)) goes into the charge sharing phase until they stabilize to a voltage \( \frac{V_{DD}}{2} \pm \delta \). Using the resultant voltage at the end of the charge sharing phase, the sense amplifier computes the majority function by comparing this voltage against a reference and then driving BL to logic 0 or 1. Since the rows remain connected to the BL, the original data in the capacitors is lost and overwritten by the result value on BL. In the case of ReDRAM, two rows are activated (double row activation-DRA) at a time and they undergo the same charge sharing phase with the BL as in the case of Ambit. To prevent the loss of original data at end of TRA or DRA, both Ambit and ReDRAM reserve some rows called compute rows in the memory array to exclusively perform a logic operation. Hence, for every operation, the operands are fetched from the source rows to the compute rows by using the copying operation described in the work Row Clone [16]. A copy operation is carried out by a command sequence of ACT \( \rightarrow \) ACT \( \rightarrow \) PRE which takes 82.5ns in 1Gb DDR3-1600 [15]. In Ambit, all the 2-input operations such as AND, OR etc. are represented using a 3-input majority function.

![Fig. 2: Hardware architecture of Ambit (Left) and ReDRAM (Right).](image)

ReDRAM improves upon the work by Ambit, by reducing the number of rows that need to operate simultaneously to two. After the charge sharing phase, but only between two rows, a modified sense amplifier is used to perform the logic operation and write back the result. The modified sense amplifier is used to change the reference voltage and perform the logic operations, as opposed to the sense amplifier in Ambit that only uses a fixed reference voltage. In ReDRAM, the reference voltages are changed with the help of inverters of varying operating points. Each inverter enables the computation of a different logic function as shown in the Figure 3. A multiplexer is used to choose between one of the logic functions.

| A | B | Out 1 (\( \delta \)) | Out 2 (\( \frac{V_{DD}}{2} \)) | Out 3 (\( \frac{V_{DD}}{2} \)) |
|---|---|-----------------|-----------------|-----------------|
| 0 | 0 | 1               | 1               | 1               |
| 0 | 1 | 1/2             | 0               | 1               |
| 1 | 0 | 1/2             | 0               | 1               |
| 1 | 1 | 0               | 0               | 0               |

![Fig. 3: ReDRAM Inverters truth table for NOR2 and NAND2.](image)

ReDRAM and Ambit have a complete set of basic functions and can exploit full internal bank data width with a minimum area overhead. However, their shortcomings include:

- Ambit and ReDRAM rely on sharing charges between the storage capacitors and bit-lines for their operation. Due to the analog nature of the operation, the reliability of the operation may get affected under varying operating conditions.
- ReDRAM modifies the inverters in the sense amplifier to shift their switching points using transistors of varying threshold voltage at the design time. Hence, such a structure is vulnerable to process variations.
- Both the designs overwrite the source operands, because of which rows need to be copied before performing the logic operations. Such an operation reduces the overall throughput that can be achieved when performing the logic operations on bulk data.

### Key Advantages of CIDAN:

The proposed platform CIDAN improves the Ambit and ReDRAM iPIM architectures in four distinct ways.

1. Memory bank and its access protocol are not modified.
2. CIDAN does not need special sense amplifiers for its operation.
3. Only a single row in a bank is activated. Multiple operands are fetched from different banks within the four bank activation window.
4. The TLPE(s) connected to the DRAM do not rely on charge sharing over multiple rows and are essentially static logic gates. They are also reconfigured at run-time to realize different functions.

Further details are discussed in Section III.

### III. PROCESSING-IN-MEMORY PLATFORM

This section describes the architecture of CIDAN.

#### A. Threshold Logic function and Artificial Neurons

A Boolean function \( f(x_1, x_2, \cdots, x_n) \) is called a threshold function if there exist weights \( w_i \) for \( i = 1, 2, \cdots, n \) and a threshold \( T \) such that

\[
f(x_1, x_2, \cdots, x_n) = 1 \iff \sum_{i=1}^{n} w_i x_i \geq T,
\]

\(^1\) W.L.O.G. the weights \( w_i \) and threshold \( T \) can be integers [17].
where \( \sum \) denotes the arithmetic sum. Thus a threshold function can be represented as \((W,T) = [w_1, w_2, \ldots, w_n; T]\). An example of a threshold function is \(f(a, b, c, d) = ab \lor ac \lor ad \lor bc \lor ad\), with \([w_1, w_2, w_3, w_4; T] = [2, 1, 1, 1; 3]\). An extensive body of work exploring many theoretical and practical aspects of threshold logic can be found in [17].

Several implementations of threshold logic gates already exist in the literature [18] [19] [20]. These gates evaluate Equation 1 by directly comparing some electrical quantity such as charge, voltage, or current. For this paper, a variant of the threshold logic can be found in [17].

The addition operation using a single threshold gate is as shown in Figure 4. Assume that the \(i^{th}\) significant bit of operands \(A\) and \(B\) are being added, with the previous carry \(C[i]\) stored in L1. In the first cycle, carry \(C[i+1]\) is generated by computing the majority function of the operand bits \(A[i]\) and \(B[i]\) and the previous carry \(C[i]\). \(C[i+1]\) is stored in the latch L2 and is also fed back as an input to the threshold gate. In the second cycle, sum-bit \(S[i]\) is computed with the inputs \(C[i+1], A[i], B[i]\) and \(C[i]\) mapped to the weighted threshold function \([-2,1,1,1;T]\). Once the sum bit is generated, the data in latch L2 is copied to latch L1, so that \(C[i+1]\) is available for the adding next significant bits of operands \(A[i+1]\) and \(B[i+1]\).

**B. Threshold logic processing element (TLPE)**

Figure 5 shows the structure of a TLPE. It consists of one threshold gate to perform computations, two latches L1 and L2 to temporarily store the output, and four XOR gates to invert the signals from the banks. The threshold gate is designed to implement a subset of the threshold function \([-2,1,1,1;T]\), where \(T\) is selected during operation to be 1 or 2. The inputs to the processing element can be inverted using control signals \(C0-C3\) or optionally disabled using enable signals \(en_5\). The threshold and the remaining two inputs of the TLG are enabled or disabled by signals \(en_n\). All the control and enable signals are generated by an external controller discussed in section III-D. The TLPE is designed to perform basic logic operations (NOT, (N)OR, (N)AND, X(N)OR) and addition operation of 3 bits, which are the most commonly used operations for in-memory applications.

Logic operations which are threshold functions, i.e., (N)AND and (N)OR functions are performed in a single cycle by enabling the required inputs (I1-I3) of the TLPE, and choosing an appropriate threshold \(T\), as shown in Table III. Non-threshold functions such as XOR and XNOR operations are decomposed into two threshold functions and then scheduled on the TLPE over two cycles.

The addition operation using a single threshold gate is slightly more complicated. It is a bit-level operation that is implemented on the TLPE in the form of a schedule, as shown in Figure 6. Assume that the \(i^{th}\) significant bit of operands \(A\) and \(B\) are being added, with the previous carry \(C[i]\) stored in L1. In the first cycle, carry \(C[i+1]\) is generated by computing the majority function of the operand bits \(A[i]\) and \(B[i]\) and the previous carry \(C[i]\). \(C[i+1]\) is stored in the latch L2 and is also fed back as an input to the threshold gate. In the second cycle, sum-bit \(S[i]\) is computed with the inputs \(C[i+1], A[i], B[i]\) and \(C[i]\) mapped to the weighted threshold function \([-2,1,1,1;T]\). Once the sum bit is generated, the data in latch L2 is copied to latch L1, so that \(C[i+1]\) is available for the adding next significant bits of operands \(A[i+1]\) and \(B[i+1]\).
TABLE II: Power and area of functionally equivalent CMOS circuit normalized to TLPE (TLPE=1). The columns labeled M-Input-T and M-Input-X are implementations of threshold functions and XOR/XNOR functions for M= 2, 3, and 4.

| Power | Area |
|-------|------|
|       |      |
| CMOS  |      |
| 2-Input-T | 4.3x |
| 3-Input-T | 5.3x |
| 4-Input-T | 6.3x |
| 2-Input-X | 1.7x |
| 3-Input-X | 1.3x |
| 4-Input-X | 1.1x |
| 2-ADD  | 1.4x |
| 2-bit  | 1.9x |
| 3-bit  | 3.2x |
| 4-bit  | 4.0x |

Fig. 6: Schedule for addition operation on TLPE for 3-bits A_i, B_i, and C_i. Output is S_i and C_i+1.

TABLE III: Basic logic operations using threshold logic processing element. For demonstration, operands are I1 and I2.

| Function | Cycle number | Weights | T |
|----------|--------------|---------|---|
| NOT      | 1            | X ~I1    | 1 |
| AND      | 1            | X I1     | 2 |
| OR       | 1            | X I2     | 1 |
| NAND     | 1            | X ~I1 ~I2| 1 |
| NOR      | 1            | X ~I1 ~I2| 1 |
| XOR      | 2            | I1 ~I2   | 2 |
| XNOR     | 2            | I1 I2    | 2 |

Fig. 7: Threshold logic processing element array (TLPEA) connected to banks in a DRAM device.

Note that it is possible to realize all the functionality of a TLPE using conventional CMOS logic gates. Table II presents a comparison of a TLPE and its CMOS equivalent in terms of power and area. The CMOS implementation was obtained by jointly synthesizing all the functions including the selection logic. The columns labeled M-Input-T and M-Input-X are implementations of threshold functions and XOR/XNOR functions for M= 2, 3, and 4. 2-ADD is the implementation of 2-bit adder. The results demonstrate that TLPE is significantly lower in area and power than the corresponding CMOS equivalent. Note that an LUT could also be used, but this would be far worse than the custom CMOS implementation as it requires reprogramming on a cycle-by-cycle basis.

C. Top Level Architecture of CIDAN

Figure 7 shows the integration of the threshold logic processing element (TLPE) within the DRAM memory chip. An array of TLPE (TLPEA) of size N is connected to four banks in the memory chip, where N is the number of bits in a row of the bank latched into the sense amplifiers (BLSA). There is one TLPEA for a set of four banks in one DRAM chip. A TLPEA accepts N-bit input vectors B1, B2, B3 and B4 from all the four banks as shown in Figure 7. For bitwise operation in this work, at most two out of four banks are activated using a four-bank activation window (TFAW) to get the operands. Consequently, only two out of four inputs to the TLPE are enabled by external control signals. The output of the TLPE array TLPEA-OP is connected to the column decoder and write driver block as shown in the Figure 7. Using the control signals and the write drivers driven by the TLPEA-OP, the result of computations is written back to one of the four banks. During the computation phase, the column decoder selects all the bitlines of the selected bank. The data path of the PIM operations is orchestrated by the external controller described in section III-D.

D. System level integration and the Controller Design

CIDAN is used as a memory and as an external accelerator that is interfaced with the CPU. The design of CIDAN includes the addition of a special instruction to the CPU’s instruction set that specifies the data and operation in CIDAN. Whenever the CPU identifies a CIDAN instruction, it passes it to the CIDAN controller – a state machine that decodes the CIDAN instruction and generates DRAM commands and control signals to implement the bitwise operation in CIDAN. Extra bits are added to the CPU-memory bus to accommodate the control signals from the CIDAN controller. Extending the instruction set and utilizing the DRAM controller have several advantages. First, the operations in CIDAN can be directly triggered by the application instead of going through any other device API code which can cause additional overhead. Second, CIDAN’s memory can be accessed by the CPU directly which prevents copying data from CPU memory to the CIDAN memory as opposed to the memory of an FPGA. Finally, the on-chip
The CIDAN instruction is of the form, `bbop dest, src1, src2, func` where `bbop` specifies the CIDAN bulk bitwise operation, `dst` is the destination address, `src1` and `src2` are the source addresses and `func` is the logic function to be implemented in CIDAN. The instruction by default operates on a data of size equal to the CIDAN bank’s row. For the data spanning multiple rows, the instruction must be repeated in the application code with different row addresses. If the data is less than the row size, it is assumed that dummy data is padded to complete the row.

The sequence of commands generated by the controller for all the CIDAN operations is shown in Table IV. An operation is carried on the data present in the row address `i` and `j`. In CIDAN, `D_i` and `D_j` are read from bank `m` and `n` respectively and the result `D_o` is written to bank `o` row `r`. It should be noted that the consecutive activate commands in the case of CIDAN are issued to two different banks separated by `t_{RRD}` time (7.5ns) and in the case of the other PIM platforms, the consecutive activate commands are issued to the same bank separated by `t_{RAS}` time (35ns). It can be observed from Table IV that while prior PIM platforms take multiple AAP (82.5ns each) commands to execute simple AND/OR functions and the number of such commands increases many times for complex functions like XOR whereas the command sequence for CIDAN remains short and constant. The PIM platforms: GraphiDe [21] and SIMDRAM [22] build upon ReDRAM and for CIDAN, remains short and constant. The PIM platforms: GraphiDe [21] and SIMDRAM [22] build upon ReDRAM and Ambit respectively perform addition and report (7 AAP) and (6 AAP + 2 AP) commands for 1-bit addition respectively. Hence, the advantage of using CIDAN increases for complex functions.

### IV. Experimental Results

The performance and energy characteristics of CIDAN were evaluated using a combination of circuit-level and system-level simulations. The threshold gate used in the TLPE was evaluated for timing and proven for robustness using Monte Carlo simulations in TSMC 40nm LP technology. The TLPE was functionally verified using SPICE and its delay, energy, and area were extracted and scaled to the 45nm DRAM technology using [23]. Gem5 [24] was used for system-level simulation using these extracted values. Gem5 was integrated with Ramulator [25] – a DRAM simulator, to run the applications and obtain their performance statistics. The simulator DRAMPower [15] was used to evaluate the energy consumption.

#### A. Raw Performance and Energy

CIDAN was evaluated and compared against the existing iPIM architectures, i.e., ReDRAM [13] and Ambit [6] for raw performance and energy. Evaluations were conducted on all the platforms using custom benchmarks that execute bulk-bitwise operations NOT, AND, OR, and XOR on large bit-vectors of size 1 Mb, 2 Mb, and 4 Mb. A uniform memory configuration of 8 banks with a memory array size of 16384x1024x8 bits was used. In Table V, performance in terms of DRAM cycles required for each of the PIM platforms to execute each bitwise operation is presented. The data is normalized to the DRAM cycles taken by CIDAN.

#### Performance: As shown in Table V, ReDRAM requires about 3X more DRAM cycles than CIDAN to compute bitwise AND, OR, and XOR for different operand sizes. These improvements stem from the fact that CIDAN required far less internal DRAM operations than ReDRAM and any other PIM platform. CIDAN takes advantage of the four-bank activation window to activate two rows in different banks and has its operand ready in `t_{RRD} + t_{RCD}` time (22.5ns). In contrast, the ReDRAM and other PIM platforms must perform a series of row-initialization and row copy operations using AAP (82.5ns) to get the operands ready for computation. CIDAN performs the function in one or two clock cycles inside the TLPE and then writes the result to another bank. Precharge in CIDAN is shared by all open banks and helps to decrease the latency.
Whereas in ReDRAM and other PIM platforms, due to the series of ACT ACT PRE (AAP) operations, several clock cycles are needed to perform the operation and write the result.

**Energy:** Table [V] compares the energy needed for primitive operations on ReDRAM, Ambit and CIDAN. On average, CIDAN’s energy consumption is nearly half the energy of ReDRAM for bulk bitwise operations, and is significantly better than Ambit. Note that the values in Table [V] account for the fact that CIDAN activates more than one bank at a time, while ReDRAM and Ambit activate a single bank.

**B. Area Overhead**

The array of threshold processing elements (TLPEA) is added to the on-pitch area of the DRAM. Each TLPEA contains as many TLPE(s) as the number of bits in a memory bank’s row. One TLPEA is shared by four banks within a DRAM chip. Note that the area of one TLPE is 41 µm² as shown in the Table [II]. Therefore, for the DRAM configuration of 8 banks with 16384 rows, 1024x8 columns, the TLPEA occupies less than ~1% of the DRAM chip area.

V. APPLICATION-SPECIFIC ANALYSIS: CASE STUDY

The PIM platform CIDAN can accelerate the applications that make extensive use of bulk bit-wise operations on large bit vectors. Such applications are common in database management, graph processing, encryption, web search, bioinformatics, etc. In the following section, three algorithms have been chosen to demonstrate the performance and energy consumption of CIDAN. They are the Advanced Encryption Standard (AES), graph processing operations, and DNA sequence mapping. In these applications, most of the operations are bitwise operations on large vectors. We expect the improvements of CIDAN over ReDRAM and Ambit in these applications to be proportional to the number and ratio of different bitwise operations used in these applications.

**A. Advance Encryption Standard (AES)**

AES is a block cipher standard that encrypts and decrypts data with a unique key. It takes 16 bytes (128 bits) of data in a 4x4 matrix form as input and uses three different key lengths (128 bits, 192 bits, and 256 bits) to encrypt the data through a series of transformations using bitwise operations. Various stages in the AES algorithm are described in Figure 8. The encryption process takes place in multiple rounds of data transformation through stages shown in Figure 8. If the key length is equal to 128 bits, then there are 10 rounds, 12 rounds for 192 bits key, and 14 rounds for 256 bits key.

To accelerate the encryption process, the stages Mix Columns and Add Round keys are executed on the PIM platforms. These two stages consist of mainly bitwise XOR and AND operations. Add round keys and Mix column stages account for about 75% of the workload and we evaluate CIDAN, ReDRAM, and CPU with configuration as shown in Table [VI].

![AES](image)

**Fig. 8: AES CPU configuration used in the experiments.**

| Processor | x86, 4 cores, out-of-order, 2 Ghz |
|-----------|----------------------------------|
| L1 Cache  | 32 KB D-cache, 32 KB I-cache, LRU policy |
| L2 cache  | 256 KB, LRU policy, 64 B Cache line size |
| Main Memory | DDR3-1600, 1 channel, 1 rank, 8 banks |

The performance in terms of total clock cycles required for CPU, ReDRAM, and CIDAN are given in Table [VII] which shows that CIDAN achieves higher performance than ReDRAM and Ambit. Substantial improvements are gained from executing AES on CIDAN than on a CPU. The 75% of the workload which was offloaded to CIDAN is reduced by 40X. Similarly, the energy consumption of CIDAN is lowest among all the platforms and improves substantially over CPU.

**B. Graph Analysis**

Graphs are traditional data structures that can store data value and also represent the relationship among data. Graphs have been a popular choice to build social networks. Facebook, Google+, and many other social networks use graphs to maintain the information of their users. With the rapid growth in the size of social networks, graph processing has become difficult and slow on the traditional Von-Neumann architectures. For several graph operations, PIM architectures are better suited. One such graph processing application is called matching index.

Matching Index \( M_{ij} \) is the similarity between the two vertices \( V_i \) and \( V_j \) based upon the number of common neighbors shared by these vertices and is given by

\[
\frac{\sum \text{common neighbours}}{\sum \text{total number of neighbours}}.
\]

To perform a matching index operation in memory, graph partitioning and allocation on memory is required. We use METIS [26] algorithm to do balanced graph partitioning.

After mapping a graph in the form of adjacency matrices to CIDAN banks, the calculation of the number of common neighbors between two vertices \( V_i \) and \( V_j \) is just a bitwise AND operation between the two rows of \( V_i \) and \( V_j \) and the total number of neighbors is given by OR operation on the

| Latency (CIDAN = 1) | Energy (CIDAN = 1) |
|---------------------|---------------------|
| ReDRAM              | 1.15                |
| CPU                 | 4.04                |
|                     | 3.74                |

**TABLE VII: Latency and Energy comparison for executing AES on different platforms normalized to CIDAN.**
TABLE VIII: Social Network datasets.

| Dataset     | Nodes  | Edges   | Graph Information          |
|-------------|--------|---------|----------------------------|
| Facebook    | 4,039  | 88,234  | Social circles from Facebook|
| DBLP        | 317,080| 1,049,866| DBLP collaboration network  |
| Amazon      | 334,863| 925,872 | Amazon product network      |

TABLE IX: Latency and Energy comparison for executing Matching Index operation on different platforms normalized to CIDAN.

| Dataset | Latency (CIDAN = 1) | Energy (CIDAN = 1) |
|---------|---------------------|--------------------|
| ReDRAM  | 3.24                | 1.96               |
| Ambit   | 4.32                | 2.61               |

same two rows. The summation operation henceforth can be carried out in the CPU.

To evaluate CIDAN and other iPIM platforms, a memory bank configuration of 16384 rows and 1024 columns of 8 bits each is used. There are in total 8 memory banks which makes the total capacity of the memory to be 128 MB. We evaluate three Social Network data sets as shown in Table VIII.

In Table IX, the relative performance of the iPIM architectures for matching index operation on two vertices relative to CIDAN is shown. Based on the results, CIDAN is the fastest architecture because of the computation on the TLPEA and the elimination of several internal DRAM operations. CIDAN also achieves the highest energy efficiency as shown in Table IX. The non-iPIM architectures like CPU and GPU as shown in [13] consumes 21X (GPU) more energy than ReDRAM due to a large number of data transfers between computer unit and memory. It is also seen that both CPU and GPU spend most of the time waiting for the data to arrive in the compute unit to perform the operation.

C. DNA sequence mapping

DNA sequence mapping is an important application in bioinformatics which involves the pattern matching problem of a given DNA sequence to a large reference genome sequence. This problem can be solved as a string-matching problem by using the bit-vector algorithm [3] involving a large number of bitwise operations. Hence, such algorithms can easily be executed on PIM platforms for high throughput and energy efficiency. We implement and compare algorithm in [3] on CIDAN, ReDRAM and Ambit as shown in Table IX. The numbers in the table are normalized to that of CIDAN. ReDRAM and Ambit take about 3.14X and 4.35X more cycles respectively to execute the workload and consumes about 2.12X and 2.88X more energy, respectively.

TABLE X: Latency and Energy comparison for executing DNA sequence mapping algorithm [3] on different platforms normalized to CIDAN.

| Dataset | Latency (CIDAN = 1) | Energy (CIDAN = 1) |
|---------|---------------------|--------------------|
| ReDRAM  | 3.14                | 2.12               |
| Ambit   | 4.35                | 2.88               |

VI. Conclusion

In this paper, a novel processing-in-memory (PIM) architecture is presented, which uses highly reconfigurable and low-power threshold logic processing elements (TLPE). By using these elements, basic two-input bit-wise logic functions such as NOT, (N)AND, (N)OR, X(N)OR, etc. and full adder operation can be accelerated inside a DRAM to achieve higher performance than equivalent state-of-the-art architectures. CIDAN takes advantage of the four bank activation window and TLPE(s) to compute bit-wise logic operations in about 3x less time than the state-of-the-art ReDRAM. The simulation results for the AES encryption, graph processing operation, and DNA sequence mapping algorithm shows superior performance and energy over any other iPIM architecture.

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