Local-gated single-walled carbon nanotube field effect transistors assembled by AC dielectrophoresis

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Abstract

We present a simple and scalable technique for the fabrication of solution processed and local-gated carbon nanotube field effect transistors (CNT-FETs). The approach is based on the directed assembly of individual single-walled carbon nanotubes from dichloroethane via AC dielectrophoresis (DEP) onto pre-patterned source and drain electrodes with a local aluminum gate in the middle. Local-gated CNT-FET devices display superior performance compared to a global back gate with on–off ratios $>10^4$ and maximum subthreshold swings of 170 mV/dec.

The local bottom-gated DEP-assembled CNT-FETs will facilitate large-scale fabrication of complementary metal–oxide–semiconductor (CMOS) compatible nanoelectronic devices.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Carbon nanotube field effect transistors (CNT-FETs) have displayed exceptional electrical properties that are superior to those of the traditional silicon metal–oxide–semiconductor field effect transistor (MOSFET) without the problem of scaling down [1, 2]. Early fabrication techniques of CNT-FETs involved random placements of CNTs either on pre-patterned electrodes or by dispersing them on substrates, locating them with atomic force microscopy (AFM), and finally defining source and drain electrodes using electron beam lithography (EBL) [3]. In addition, most of these devices were often controlled by a global back gate because of its ease of processing. Such fabrication processes offer neither high throughput nor individual control of each CNT-FET necessary for parallel fabrication of nanoelectronic devices.

For large-scale fabrication of CNT-FET devices three conditions need to be satisfied: (i) separation of semiconducting and metallic carbon nanotubes must be realized, (ii) nanotubes need to be assembled at selected positions of the circuit with high yield, and (iii) each nanotube must be addressed individually with a local gate. While control over separation remains elusive, significant progress has been made in the directed assembly of CNT-FETs by patterning catalysts for the chemical vapor deposition (CVD) growth process and using a local top gate [4–7]. Although devices made from such techniques show the best performance so far, CVD requires the growth temperature to be 900°C, which is prohibitively high for current CMOS fabrication technologies. Other assembly techniques such as chemical and biological patterning [8, 9], flow assisted alignment [10], Langmuir–Blodgett assembly [11], bubble blown films [12], and contact printing [13] demonstrated for 1D nanostructures may also provide a route for large-scale fabrication of CNT-FETs.

Recently, AC dielectrophoresis (DEP) has been utilized for large-scale assembly of individual single-walled carbon nanotubes (SWNTs) or bundles at selected positions of the circuit [14–25]. In DEP, CNTs are assembled from solution using a non-uniform AC electric field. However, all DEP-assembled CNT-FETs reported in the literature used only a global back gate [14–19, 21, 22, 24]. Global back-gated devices give poor device performance due to inefficient gate coupling and contact-controlled operation. This means that when the back gate is active, it controls the Schottky barriers rather than the conducting channel itself, causing slow switching behavior [26]. In addition, a global back gate cannot...
address CNT-FETs individually, making integrated circuits out of the question.

Here we report on the fabrication and device characteristics of local bottom-gated DEP-assembled CNT-FETs. First, gold (Au) source and drain electrodes of 1 μm separation with a 100 nm wide aluminum (Al) gate electrode in the middle were fabricated with standard optical and electron beam lithography (EBL). Carbon nanotubes suspended in dichloroethane (DCE) were then assembled between source and drain electrodes via DEP. We find that both metallic and semiconducting nanotubes can be assembled and the centered aluminum gate does not affect the DEP assembly. We also show that the measured device performance, such as the subthreshold swing of a local-gated semiconducting nanotube FET, is superior compared to the global back-gated device, possibly due to channel-controlled operation. Local bottom-gated DEP-assembled CNT-FETs will facilitate large-scale fabrication of CNT-based integrated circuits and other nanoelectronic devices such as sensors.

2. Experimental details

Devices were fabricated on heavily doped silicon (Si) substrates capped with a thermally grown 250 nm thick SiO₂ layer. Figure 1 presents an illustration of the device fabrication procedure. The electrode patterns were fabricated by a combination of optical and electron beam lithography (EBL). First, large contact pads and electron beam markers were fabricated with optical lithography using double layer resists (LOR 3A/Shipley 1813), developing in CD26, followed by thermal evaporation of chromium (Cr) (5 nm) and Au (50 nm), and finally standard lift-off. Second, smaller-scale source and drain electrode patterns were defined with EBL using single-layer PMMA resists and then developing in (1:3) methyl isobutyl ketone:isopropyl alcohol (MIBK:IPA). After defining the patterns, 5 nm Cr and 20 nm Au were thermally deposited, followed by lift-off. The source and drain electrodes are chosen to be of tapered shape, as shown in figure 1(a), to maximize the electric field at the sharp edge and increase the chance of obtaining an individual SWNT connection during the DEP assembly. EBL was then implemented once again to define the Al gate patterns using single-layer PMMA resist and developing in MIBK:IPA following thermal deposition of 20–25 nm of Al and lift-off (figure 1(b)). The Al gate patterns had a partial overlap with selected gold contact pads defined earlier in order to apply a voltage to the local gate. The sample is finally treated in oxygen plasma for 10 min to ensure a good 2–3 nm thick aluminum oxide (Al₂O₃) layer.

The DEP assembly of a CNT shown in figure 1(c) was carried out as follows. A very small amount (∼0.3 μg) of highly purified HiPco-grown SWNTs (purchased as nanotube soot from Carbon Nanotechnologies Inc.) was ultrasonically dispersed in 5 ml of 1,2-dichloroethane for approximately 30 min. Immediately after the dispersion was complete, a small drop (∼8 μl) was cast onto a chip with 12 pairs of source–drain electrodes, each containing a 100 nm wide Al gate. An AC voltage of approximately 8 V_p-p at 1 MHz was applied with a function generator for 1–2 s to the electrode pair and then moved to the next pair in a probe station. It has been shown that when metallic posts are present in between source and drain electrodes they may influence the DEP assembly process for a CNT [18]. We have found that our gate electrode does not influence the ability to assemble CNTs between the 1 μm gap, possibly due to the Al₂O₃ insulating layer. We have studied other AC voltages and trapping times and find that larger voltages applied in shorted time periods give us more control over the ability to assemble an individual carbon nanotube or a small-diameter bundle. The AC voltage gives rise to a time-averaged dielectrophoretic force. For an elongated object it is given by

$$F_{\text{DEP}} \propto \varepsilon_m \text{Re}[K_f] V E_{\text{RMS}}^2, \quad K_f = \frac{\varepsilon_p - \varepsilon_m}{\varepsilon_p},$$

where \(\varepsilon_p\) and \(\varepsilon_m\) are the permittivity of the nanotube and solvent respectively, \(K_f\) is the Clausius–Mosotti factor, \(\sigma\) is the conductivity, and \(\omega = 2\pi f\) is the frequency of the applied AC voltage [27]. The induced dipole moment of the nanotube interacting with the strong electric field causes the nanotubes to move in a translational motion along the electric field gradient [23, 24]. Because of the strong dielectrophoretic force, the nanotubes are reproducibly aligned at the tips of the source and drain electrodes where the electric field is maximum. This is shown in figure 1(d), where we present a representative AFM image of one of our devices. After the trapping process is complete, the chip is rinsed with IPA and blow dried with nitrogen gas to remove any unwanted nanotubes or impurities in the suspension. Other groups have dispersed CNTs in aqueous sodium dodecyl sulfate (SDS) [14–20, 23], isopropyl alcohol.

![Figure 1](image-url)

**Figure 1.** Fabrication of the local-gated CNT-FET device. (a) Source (S)-drain (D) electrodes of 1 μm separation are patterned on heavily doped Si/SiO₂ substrates (250 nm thick oxide layer). (b) Local Al gate electrodes are patterned using EBL and a 2–3 nm thick Al₂O₃ is created by oxygen plasma treatment. (c) DEP assembly of a CNT. An AC voltage of 8 V_p-p is applied for 1–2 s to the source electrode with a function generator. (d) Resulting AFM image of a device showing that nanotubes are assembled at the tips.
3. Results and discussion

After the DEP assembly, electronic transport measurements were carried out in a probe station and ambient environment. Out of 115 devices that we have tested, we find that in $\sim$35% cases the electrodes were bridged with either an individual SWNT or a small-diameter CNT bundle determined by AFM measurements. The rest of the samples either have multiple connections or no connection at all. Here we focus on devices containing individual nanotubes or small bundles. The two-terminal resistance of our samples is usually in the range 1–10 MΩ. Our value of contact resistance is consistent with other DEP-assembled devices [14–25]; however, it is higher than that of top contact CVD-grown devices ($\sim$100 kΩ), where the nanotube is first grown by CVD on a substrate, made contact to, and then annealed. The contact resistance depends on several factors, such as work function of the metal being used, diameter of the nanotubes, surface properties, contact area and device geometry. From our observation of many AFM images, the DEP-assembled devices seem to be end-contacted (the nanotube’s end is connected to the electrode’s end). Therefore the contact area is very small. In addition, we used gold as a metal electrode, which gives a larger Schottky barrier at the metal–CNT interface. These may be a few reason for large contact resistance in our DEP-assembled devices. We are currently investigating ways of reducing the contact resistance such as using a palladium contact, post-deposition and annealing.

Before discussing local-gated devices, we first present the electronic characteristics of global back-gated devices. We used heavily doped Si substrates as a global back gate. Figure 2(a) shows the drain current ($I_{DS}$) as a function of back gate voltage ($V_{BG}$) of representative metallic and semiconducting devices for a fixed source drain voltage ($V_{DS}$) of 0.3 V. The metallic single-walled nanotubes (m-SWNTs) show weak modulation in $I_{DS}$ as a function of $V_{BG}$, whereas semiconducting single-walled nanotubes (s-SWNTs) show several orders of magnitude change in $I_{DS}$ as a function of $V_{BG}$. About half of the devices we examined for this study display p-type semiconducting behavior characterized by $V_{BG}$ following the DEP assembly. These devices displayed current on–off ratios $>10^4$ and subthreshold swings $S = [dV_G/d(\log I_D)]$ from 1000 to 2500 mV/dec. Other DEP-assembled CNT-FET devices reported in the literature also display similar device characteristics [14, 15, 17–19, 21, 22]. The other half of the devices we examined showed metallic behavior, where $\sim$30% of them were able to be transformed to become semiconducting via selective burning of m-SWNTs contained in the bundles [28]. To deplete carriers in the s-SWNTs, 10 V is applied to the $V_{BG}$ and then $V_{DS}$ is ramped up to approximately 10 V until the current starts to drop, as shown in figure 2(b), labeled 1 and 2. Some devices may be destroyed if further burning is done (usually the current will eventually drop to zero at voltages greater than 15 V). The $I_{DS}$–$V_{BG}$ characteristics are measured once again after each burning step and the procedure is repeated until a larger on–off ratio is observed. The final back gate voltage dependence is shown in figure 2(b)’s inset with an on–off ratio of $\sim$1000. Most of the devices that needed selective burning display lower on–off ratios compared to the as assembled semiconducting CNT-FETs. The fair performance can be attributed to the presence of metallic nanotubes still within the bundles between the electrodes, introducing more scattering into the transport.

Figure 3(a) presents characteristics of one of our local-gated device where we also present back-gated data of the same device for comparison. It can be clearly seen that the threshold voltage for the back gate is 10 V while for the local gate it is only 1 V, indicating an extremely better gate coupling for the local gate. Additionally, the back gate has a broad maximum subthreshold swing of $\sim$2230 mV/dec, whereas the local gate has a value of $\sim$170 mV/dec, demonstrating much faster switching behavior by the local gate. Figure 3(a)’s inset displays an expanded view of the local gate dependence,
clearly showing up to \( \sim 4 \) orders of magnitude change in \( I_{DS} \) for a small gate voltage range. The leakage current measured for our device is negligible (<1 pA for a voltage of \(-2 \) to \(+2 \) V applied to the local gate). Other local-gated devices that we have fabricated show similar FET response. Small values of the subthreshold swing and low threshold voltage are preferred in FETs for low power consumption and high-speed operation [5, 29]. In figure 3(b) we plot \( I_{DS} \) versus \( V_{DS} \) at different local gate voltages (0 to \(-1.4 \) V in steps of \( 0.2 \) V from top to bottom). These output characteristics are similar to typical p-MOSFET devices. From here we can calculate the transconductance in the saturation regime by taking \( g_m = \frac{dI_{DS}}{dV_g} \mid _{V_{GSS} = -1.6 \text{ V}} \) to be \( 0.3 \) \( \mu \)S. Normalized by the width of the nanotube (\( \sim 1.5 \) nm), we derive the normalized transconductance for the local gate of 200 \( S \) \( m^{-1} \), while for the back gate we derive a value of 3.3 \( S \) \( m^{-1} \). This also indicates better efficiency of the local aluminum gate. These local gate characteristics are superior to those of other DEP-assembled CNT-FETs [16] reported in the literature and comparable to those of some higher performance CNT-FET devices reported recently with \( Al_2O_3 \) gates [6, 29] and high-\( K \) dielectrics [5]. Table 1 gives a brief comparison of a few recently fabricated CNT-FETs along with the device presented here.

### Table 1. Comparison of a few recent CNT-FETs assembled by DEP and CVD techniques.

| Assembly  | Gate material  | Subthreshold Threshold | Reference |
|-----------|----------------|------------------------|-----------|
| DEP       | SiO\(_2\)/back gate | 1200 1.5 | [16] |
| CVD/ALD   | \( Al_2O_3 \)/local gate | 120 N/A | [29] |
| CVD       | SiO\(_2\)/back gate | 1000–2000 N/A | [5] |
| DEP       | \( Al_2O_3 \)/local gate | 170 1 | This work |

A possible reason for the fast switching behavior of our local-gated device may be due to channel-controlled operation [26]. There are two accepted sources of operation for CNT-FETs: (i) contact-controlled operation from the formation of Schottky barriers at the contacts [30] or (ii) channel-controlled operation [31] (typically for good ohmic contacted devices). For our local-gated device, the mechanism is channel controlled owing to the thin \( Al \) gate in the middle, which is relatively far away from the source and drain electrodes. When the \( Al \) gate is active its electric field cannot affect the contact between the nanotube electrodes. Thus, the switching will be due to the local gate controlling the channel and will not depend on whether the contact has a large Schottky barrier or if it is an ohmic contact. We are currently working on scaling down the gate length further to increase device performance.

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Figure 3. (a) Drain current versus local gate voltage and back gate voltage for comparison from the same device after DEP assembly. \( V_{DS} = 0.3 \) V for both curves. The local gate shows far better gate coupling. Inset: expanded plot of \( I_{DS} \) versus \( V_{LG} \) showing low threshold voltage and subthreshold swing. The gate leakage current is <1 pA. (b) Output characteristics, \( I_{DS} \) versus \( V_{DS} \) for different gate voltages up to the saturation regime.
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