VoxelCache: Accelerating Online Mapping in Robotics and 3D Reconstruction Tasks

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ABSTRACT

Real-time 3D mapping is a critical component in many important applications today including robotics, AR/VR, and 3D visualization. 3D mapping involves continuously fusing depth maps obtained from depth sensors in phones, robots, and autonomous vehicles into a single 3D representation model of the scene. Many important applications, e.g., global path planning and trajectory generation in micro aerial vehicles, require the construction of large maps at high resolutions. In this work, we identify mapping, i.e., construction and updates of 3D maps to be a critical bottleneck in these applications. The memory required and access times of these maps limit the size of the environment and the resolution with which the environment can be feasibly mapped, especially in resource constrained environments such as autonomous robot platforms and portable devices. To address this challenge, we propose VoxelCache: a hardware-software technique to accelerate map data access times in 3D mapping applications. We observe that mapping applications typically access voxels in the map that are spatially co-located to each other. We leverage this temporal locality in voxel accesses to cache indices to blocks of voxels to enable quick lookup and avoid expensive access times. We evaluate VoxelCache on popularly used mapping and reconstruction applications on both GPUs and CPUs. We demonstrate an average speedup of 1.47X (up to 1.66X) and 1.79X (up to 1.91X) on CPUs and GPUs respectively.

CCS CONCEPTS
- Computer systems organization → Robotics; Embedded systems; Other architectures;

KEYWORDS
Mapping, SLAM, reconstruction, caching, hardware acceleration

1 INTRODUCTION

3D mapping is an essential component in many important applications today, such as in autonomous robotics, AR/VR applications, and 3D reconstruction. Mapping involves the real-time construction of a representation (map) of the environment. This is typically done by continually processing and integrating distance information to objects in the scene that is obtained from sensors such as depth cameras and LiDAR. Mapping is an integral part of tasks such as SLAM (Simultaneous Localization and Mapping), which involves determining the location/pose of a mobile robot within the constructed map of the environment, and 3D reconstruction, which is used to construct and render 3D scenes/objects from 2D images. These tasks are deployed in a number of important applications. For example, augmented reality libraries for mobile phones like Google’s AR-Core [2] and Apple’s ARKit [1] use SLAM for motion and environment estimation. 3D Reconstruction is used for a number of visualization tasks, like 3D renderings of real estate floorplans for apartment rentals, and free viewpoint television, which enables interactively viewing large city models from different any viewpoints used for street view.

One common approach to represent the environment as a map is to use a voxel grid, in which the 3D space is discretized into a grid and each element of the grid (called a voxel) stores local information that characterizes that point in space. Typically, the distance to the closest occupied point in space is saved in each voxel, referred to as the Signed Distance Field (SDF) [31]. Mapping continually updates the information in each voxel by integrating the depth input information obtained from sensors with repeated calls to a map update routine. It is often necessary to have both fast map updates that can process high input frame rates and generating maps at high resolution (more voxels to represent a given region). For example, in robotics perception, faster updates allow for a faster control loop feedback which enables robust and agile maneuvering. In online scene reconstruction, a fast and high resolution map allows a more detailed render to be generated at a higher frame rate. In autonomous navigation, a higher resolution map would result in the application inferring finer details of its surroundings, enabling more optimized trajectories during path planning [16, 29, 30, 40, 41].

However, enabling fast map updates at very high resolutions is challenging, especially for mapping large environments. We find that a single map update takes anywhere from around 50ms to 500ms, depending on the required resolution of the map. This is due to both lengthy access latencies and a large number of accesses to voxel data per map update. Furthermore, higher map resolutions significantly increase the number of voxels required to be updated.
2 BACKGROUND AND MOTIVATION

2.1 Representation of Voxel Maps in Memory

A straightforward approach to store voxel data is to use a 3D array indexed by the spatial coordinate of the voxel [18, 37]. However, this approach is not scalable and becomes impractical for large maps or at high resolution as it requires a significant amount of memory for storage. For example, a 3D array to represent occupancy information for a relatively small 10m × 10m × 10m region with voxels of resolution 2cm would require 500MB.

Voxel hashing [28] provides an efficient way to store maps of large areas in a scalable manner while incurring low access/insertion latencies. Compared to a 3D array representation of voxels which densely represents both empty and occupied spaces, voxel hashing only allocates voxels for areas that are occupied. Unallocated voxels are considered to be empty making it highly scalable with respect to memory. Voxel hashing thus involves saving allocated blocks of voxels (of size n × n × n) that is indexed the coordinates of voxel block using a hash table. Mapping a large scene involves a number of allocations of blocks of voxels. A large block size would decrease the number of hash table entries needed, but would greatly increase the memory footprint occupied by the block. Since the target platforms for a number of SLAM/mapping and reconstruction frameworks are embedded systems which have constraints on memory and compute power, a large block size is generally not preferred. A block of dimensions 8 × 8 × 8 is usually chosen.

Octrees [15] are another popular approach for storing voxel information of large regions of the environment in memory. Octrees use a tree data structure to store voxel data in space. Each node in the tree corresponds to a cubic volume in 3D space. A node may contain 8 children, which represent 8 equal octants of the cube, or it may be a leaf node, which corresponds to an individual voxel. An access to a voxel involves traversing through the tree data structure starting from the root node to the leaf node. Since each access to a voxel requires a tree traversal, octrees incur a high access latency, making online mapping a lot more time-consuming compared to implementations using voxel hashing. However, some recent works on online mapping with octrees propose specialized implementations that achieve similar performance as implementations with voxel hashing [7, 24].

2.1.1 Voxel Data Structures. Voxel hashing [28] provides an efficient way to store maps of large areas in a scalable manner while incurring low access/insertion latencies. Compared to a 3D array representation of voxels which densely represents both empty and occupied spaces, voxel hashing only allocates voxels for areas that are occupied. Unallocated voxels are considered to be empty making it highly scalable with respect to memory. Voxel hashing thus involves saving allocated blocks of voxels (of size n × n × n) that is indexed the coordinates of voxel block using a hash table. Mapping a large scene involves a number of allocations of blocks of voxels. A large block size would decrease the number of hash table entries needed, but would greatly increase the memory footprint occupied by the block. Since the target platforms for a number of SLAM/mapping and reconstruction frameworks are embedded systems which have constraints on memory and compute power, a large block size is generally not preferred. A block of dimensions 8 × 8 × 8 is usually chosen.

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store the signed distance is the most commonly used approach in mapping literature [9, 13, 18, 22, 26, 32–35, 37, 38]. In this work, we mainly consider frameworks whose map construction maintains and updates signed distance information stored in voxel grids.

The map update routine receives depth measurement information of different points in space from either depth cameras / LiDAR or stereo vision cameras, and a pose estimate of the sensor from odometry measurements or external pose measurements as the input. Real time computation of true SDF from depth sensor measurements over a large volume is computationally expensive [18]. One common approach to obtain an approximate SDF is to compute the truncated signed distance field (TSDF) in which the point cloud captured by the sensor is first transformed from the camera’s coordinates to the global coordinates. Multiple rays are cast from the camera center to each point in the point cloud. The distance from each point to surrounding voxel centers along the ray up to a truncation distance is calculated and assigned to these voxels. Another approach to estimate an approximate SDF is to compute the Euclidean Signed Distance Field (ESDF) in which the distance from each occupied voxel center (closest voxel to each point in the point cloud captured by the sensor) to all neighboring voxels up to a clear radius is computed. These distances computed are used to update the signed distance of corresponding voxels.

2.2 Characterizing Mapping Overheads

Figure 1 illustrates how a voxel block pointer is retrieved from its coordinates by computing the hash function and iterating through a data-dependent sequence of load and key comparison operations. This is a high latency operation because of data-dependent memory accesses and the high branch mispredict rates in the control flow. A large number of these operations are performed at each map update leading to a significantly higher map update time. These operations form a significant portion of the overall map update time. An analysis of the contribution of this latency as a percentage of runtime and absolute number of accesses to the voxel hash table is shown in Figure 2. Note that in the case of inft-CPU, despite the relatively high number of accesses we observe a relatively smaller percentage of cycles contributing to the map update time. This is because inft-CPU uses a memoization scheme in software which caches the recently accessed block pointer at each hash table bucket. While reducing the number of hash table accesses, it incurs additional overhead for memoization at every access.

At higher resolutions, the number of accesses made at every update increases greatly, leading to a significant increase in map update time. On average, the map update time increases by 9X between grid sizes 0.15m and 0.05m.

![Figure 3: Normalized map update time with varying voxel grid size](image1)

Figure 3: Normalized map update time with varying voxel grid size

Figure 4 shows the number of accesses and the access time as a percentage of the overall scene integration time of Supereight [24], which uses an efficient octree implementation for the ICL-NUIM [14] living room traj2 dataset. We observe that the average number of accesses at smaller voxel grid sizes is up to $1.5 \times 10^6$, and the accesses take up to 40% of the scene integration time. In addition, a significant portion of the time taken for generating meshes using ray marching involves (up to 45%) voxel access times.

![Figure 4: Fraction of time attributed to octree voxel accesses in Supereight [24]](image2)

Figure 4: Fraction of time attributed to octree voxel accesses in Supereight [24]

2.3 Characterizing Key Access Patterns

Figure 5 shows the number of distinct voxel blocks accessed on average during a map update at a voxel resolution of 0.10m. On comparing this with the overall number of accesses during each map update step in Figure 2, we infer that there is massive reuse in accesses to voxel blocks. There are two sources that contribute to this reuse:

- A single update makes repeated accesses to the voxels in a small portion of the large scene. This is because a number of rays cast during raycast intersect the same blocks of voxels when estimating the TSDF. When computing the ESDF, voxels surrounding each point from a point cloud captured by the sensor are updated (refer to Section 2.1.2). Since these points (projected from a single depth image) are close by in space, there is a large degree of overlap between update regions of occupied voxels. As a result, the voxels in these overlapped regions are accessed multiple times during each map update.

- There is a large overlap in the blocks of voxels accessed in two consecutive updates, as it involves updating the SDF in the same portion of the scene.

To empirically verify repetitive key access patterns, we analyze the gaps between accesses to the same key (in terms of map accesses) and count the number of occurrences of each gap for the
9 mapping framework FIESTA [13]. Figure 6 shows the histogram of the gap distribution for accesses to the same blocks during a single map update at a voxel resolution of 0.1m. We observe that a large percentage of gaps between accesses to the same block occur within 150 accesses.

3 APPROACH

Our goal in this work is to enable fast map updates at higher resolutions, which is crucial for many important applications. To this end, we introduce VoxelCache, a hardware-software mechanism to enable fast map updates by speeding up voxel data retrieval latencies. The key idea of VoxelCache is to leverage temporal locality in accesses to the voxel map by caching the 3D coordinate of the voxel-block + voxel information pair. With hardware support for key-indexed lookup of voxel block pointers from the cache, we enable fast voxel data access. Figure 7 demonstrates the high level mechanism of VoxelCache. Voxel block pointers are indexed by its coordinates $k_x, k_y, k_z$ in space. On receiving a request to access voxel data from the block at coordinates $k_x, k_y, k_z$, VoxelCache performs a lookup for the corresponding block pointer in the cache and bypasses the costly execution path of voxel data access.

![Figure 7: VoxelCache lookup path: Each hash table access to the block pointer can be bypassed with a faster lookup](image)

We devise a scheme to make use of the existing L1D/L2 cache in CPUs and the L1D cache in GPUs as storage to cache key-block pointer pairs. We introduce a new storage mode which would allow application data to be stored in the cache alongside key-block pointers. We introduce changes to the cache controller to handle two different kinds of requests: virtual addresses and VoxelCache accesses. VoxelCache accesses handle the lookup/store operations of key-block pointer pairs in the cache. VoxelCache provides hardware primitives to store and lookup key-block index. Finally, we expose these primitive operations as ISA instructions accessible in software.

3.1 Design Overview

The cache holds two types of data: 1) cached voxel block data, and 2) virtual memory addressable data. We make the following design choices to handle accesses to voxel information and virtual-memory indexed data from the same cache:

First, we need to define how our key-value data is indexed and placed in the cache. We reserve $m$ ways of an $n$-way set associative cache for voxel block pointer data. Each line holds up to $3$ key-block pointer pairs, packed in a contiguous manner. Each key is associated with a pseudoaddress from which the set and tag of the reserved line is derived. The pseudoaddress is computed as:

$$ \text{pseudoaddress} = \text{hash function}(k) \% \text{NR} $$

(1)

where $\text{NR}$ is the number of reserved lines of the outermost reserved level of the cache hierarchy. The pseudoaddress determines which cache line a key-block pointer pair would belong to at each cache level. Note that this definition of the pseudoaddress ensures that keys packed in the same line do not get assigned to different lines in other levels of the cache hierarchy. The position of the key-block pointer pair within a cache line is determined at insert time: If there is an empty slot available, the key-block pointer is inserted into that position. If not, VoxelCache replaces the least recently used key-block pointer pair in the line with the new item.

Second, we need to define a replacement policy for the reserved lines to handle writes and evictions in the event of a cache miss or hit. When inserting key-block pointers, a tag and set index is computed for the pseudoaddress. If the tag is not found in the reserved lines in the cache, a cache miss is registered and the request is forwarded to higher levels of the hierarchy. If the tag exists among the reserved lines of the set, the key is compared against the keys in the cache line. The least recently used key-value pair in the line is replaced with the new key-value pair. We implement a write-through mechanism for all cache levels. On receiving a lookup operation, the cache controller looks up the line corresponding to the set and tag derived from the pseudoaddress of the key. If the tag exists among the reserved section but the key is not found, an invalid value is returned. If the tag is found, the corresponding value is returned and the line overwrites the line in the lower levels of the cache hierarchy. In the event where we encounter a cache miss at the outermost reserved section of the cache, we return an invalid value. Unlike a regular cache lookup, we do not forward this request to main memory.

Third, VoxelCache introduces voxcache_insert, voxcache_remove and voxcache_lookup instructions to the ISA. voxcache_insert inserts a VoxelCache store request, while voxcache_lookup inserts a VoxelCache load transaction request into the load store queue. These requests are handled by the cache controller which
performs the corresponding insert and lookup operations. In application code, voxcache_lookup is inserted before a voxel block access for lookup. If the lookup is unsuccessful, the application retrieves the voxel block pointer from the voxel data structure after which voxcache_insert is called.

### 3.2 VoxCache Inserts and Lookups

On receiving an insert or lookup or a remove transaction request for voxel block data, the requested key coordinates along with the computed pseudoaddress is inserted into the load-store queue of the core, as demonstrated in Figure 9. The cache controller picks up these attributes and derives the set index and tag for the cache level from the pseudoaddress. If the corresponding tag does not exist among the reserved lines, a cache miss is registered and the request is forwarded to higher levels of the cache. If the tag exists among the reserved lines of the set, the 16-byte key is compared against the keys in the cache line. For an voxcache_insert operation, the least recently used key-value pair in the line is replaced with the new key-value pair. For a voxcache_lookup operation, if the key is not found, an invalid value is returned. If the key is found, the corresponding value is returned and the line overwrites the line in the lower levels of the cache hierarchy.

### 3.3 VoxCache: Example Usage

Figure 8 shows an example on how VoxCache is placed in application code to retrieve block pointers. The pseudo code describes the wrapper function to retrieve block pointer corresponding to a requested key \( k \) using VoxCache. We first perform a lookup to search for the requested key. If the key is found, the block pointer is returned and we can bypass performing the expensive voxel data access. If we do not find the requested key in the cache, an invalid value is assigned to the block pointer and we do a voxel data structure lookup. After the voxel data access, we insert this key-block pointer pair in the cache for future lookups.

```plaintext
function GetBlkPtr(k : key_coordinates)
    blkptr ← voxcache_lookup(k)
    if IS_INVALID(blkptr) then
        blkptr ← HT_LOOKUP(k)
        voxcache_insert(k, blkptr)
    end if
    return blkptr
end function
```

Figure 8: VoxCache lookup algorithm to retrieve the requested block pointer

### 4 DETAILED DESIGN

In this section we provide a detailed description of the components of VoxCache, and describe their individual operation.

#### 4.1 VoxCache Data Indexing and Address Generation

We design VoxCache to handle key-block pointer data store and load requests similar to regular store and load operation with virtual memory addresses. We describe the changes to the core to handle data accesses to both cached block pointer data and regular virtual memory indexed data.

##### 4.1.1 Indexing Key-block Pointer Pairs

As outlined in Section 3.1, the cache holds key-block pointer pairs in lines of the cache separate from regular virtual address indexed data. To find the appropriate reserved cache line a key-block pointer pair should belong to, the cache controller would need to derive a set index and tag for a given key at each cache level. To this end, we associate each key with a VoxCache pseudoaddress (Eq. 1) from which the set index and the tag can be derived.

Since a single cache line can hold multiple key-block pointer pairs, a naive cache replacement policy evicts and inserts data at a key-block pointer element level. This would require defining a fine grained cache replacement policy which would become exceedingly complicated. To greatly simplify formulating a replacement policy, we make a design choice to index key-block pointer data that enables us to perform evictions and write backs at a cache line level similar to ordinary cache replacement policies. We therefore need to ensure that the cache is able to write back entire lines containing key-block pointer items at a time, without the need to derive locations to individual keys within the line. Therefore it is required that any two keys which derive the same set index and tag at one cache level derive set index and tag equal to each other at all levels of the cache. This criterion ensures that all key-block pointers within a cache line do not derive different set and tag bits at different levels of the cache. A pseudoaddress as defined in Eq. 1 ensures that any pair of keys packed in one line generate mutually equal set and tag bits at every reserved level of cache.

Figure 9: VoxCache issues memory load operations from the load store queue. The red regions of the cache indicate regions where key-block pointer data is stored.

##### 4.1.2 Addressing Modes

Under VoxCache, two types of data accesses are to be handled by the core: virtual memory load/stores and key-block pointer load/stores. We augment the core to handle both of these types of loads and stores. VoxCache queues key-block pointer requests to the load store queue alongside regular data indexed by virtual memory as shown in Figure 9. We categorize the type of access by associating each load/store with one of the two addressing modes: 1) the virtual address mode, which handles memory requests of data indexed by virtual addresses and 2) VoxCache mode, which looks up key-block pointer pairs stored in the cache. Each mode of access follow different cache replacement policies during lookup and insertion. An additional flag in each load
store queue entry specifies the addressing mode of our requested data. Note that using the load store queue for VoxelCache loads and stores allows leveraging memory disambiguation and store-load queue forwarding techniques supported by the processor leading to better performance.

4.2 Changes to the Cache Controller/Memory Pipeline

VoxelCache uses on-chip L1D/L2 cache to store key-block pointer pairs. The cache now holds two types of data: 1) key-block pointer data, and 2) regular virtual memory addressable data. We implement additional logic to support lookup and insert operations under VoxelCache, and make the following modifications to the cache controller.

4.2.1 Reserving cache lines in L1D/L2 cache. VoxelCache reserves cache lines in the L1D/L2 caches to store key-block pointer data. Any lookup or insert for a requested key requires VoxelCache to perform a search among the reserved lines of the cache. To indicate whether a line is reserved under VoxelCache or not, we introduce a 1 bit "mode" flag in the cache line state as shown in Figure 10. In an n-way set associative cache, the cache buffer is split into sets of lines with each set containing n cache lines. We implement a hardware primitive, reserve_cache_lines(m, level) to mark the first m lines among the n lines per set in the cache for voxel block caching. This primitive invalidates all marked lines of the cache, evicts the data and sets the "mode" flag in the cache state of each line.

4.2.2 Cache Line Format. We hold multiple key-block pointer pairs in each reserved cache line by contiguously packing key-block pointer bytes of data as depicted in Figure 10. Each key takes up 12 bytes (3D spatial coordinates of integers) and each block pointer takes up 8 bytes of space. For CPU caches with a 64 byte cache line, we pack 3 key-block pointer pairs in a reserved cache line (Figure 10a) whereas for GPU cache of size 128 kB, we pack 6 key block pointer pairs (Figure 10b). The position of a key-block pointer pair within the cache line is determined at insert time, where we follow a within-cache line insertion policy to determine the slot it would belong to. We choose an LRU policy to replace exist key-block data within each reserved cache line. To keep track of the least recently used item within the cache line, we introduce additional LRU-bits as part of the cache state.

(a) 64KB cache line in CPUs: 3 keys, block pointer indices are packed in each reserved line.

(b) 128KB cache line in GPUs: 6 keys, block pointer indices are packed in each reserved line.

Figure 10: VoxelCache reserved cache line format for storing keys in CPUs and GPUs. We add an additional flag 'mode' to the cache state.

4.3 Cache Replacement Policies under VoxelCache

We have separate cache replacement policies for the reserved and unreserved sections of the cache. For virtual memory loads and stores, a normal mode request is sent in the cache controller. Data accesses and evictions of cache lines for normal mode accesses is restricted to the unreserved line sections of the cache. The replacement policy for normal mode requests is identical to the cache replacement policy of the processor, with the constraint that write back and eviction operations only modify unreserved lines of the cache. We effectively trade off the number of lines of cache available to the process for faster accesses to the key-block pointer data. For reserved lines under VoxelCache, we need to define 2 cache replacement policies: Entire-line replacement policy and Within-line item replacement policy.

For key-block pointer loads and stores, the cache controller is restricted to only lookup the VoxelCache reserved lines in the cache. We now describe the entire-line level and within-line replacement policy in detail. The cache is said to have registered an entire-line-read-HIT when a VoxelCache load request for a key finds the corresponding set and tag among the reserved cache lines during lookup. If the requested key exists among the packed keys in the cache line, we register a within-line-read-HIT, otherwise we register a within-line-read-MISS. An entire-line-read-MISS is registered when the set and tag derived from the requested key is not found in the cache.

An entire-line-write-HIT is registered when a VoxelCache store request for a key finds its derived set and tag in the reserved lines of the cache. A within-line-write-HIT is when the key to be overwritten exists in the cache line. Otherwise a within-line-write-MISS is registered. A entire-line-write-MISS is registered when a VoxelCache store for a key does not find its tag bits in the set in the reserved section of the cache.

4.3.1 Entire Cache Line Replacement Policy. VoxelCache reserves cache lines in the L1D/L2 levels of the cache of CPUs, and in the L1D buffer of GPUs. Tables 1 and 2 outline the function of the cache controller in each possible scenario for CPUs and GPUs respectively.

For CPUs, on encountering an entire-line-read-MISS on L1D, the read request is forwarded to L2 cache. If we encounter an entire-line-read-MISS on L2, we return an invalid value. On encountering an entire-line-read-HIT in L1D or L2, The lookup then proceeds to look for the requested key within the line. If we encounter the entire-line-read-HIT at the L2 level, we implement a write back operation which copies the corresponding line into the L1D cache, as shown in Figure 11. For an entire-line-write-MISS in L1D, we forward the store request onto L2. On encountering an entire-line-write-HIT, we evict the least recently used reserved cache line in the set and insert the new key-block pointer data. An entire-line-write-HIT would invoke the within line replacement policy.

For GPUs, an entire-line-read-MISS from the L1D cache returns an invalid block pointer. We avoid forwarding VoxelCache requests to the L2 level for GPUs. An entire line read-HIT would search within the line for the requested key. On encountering an entire-line-write-MISS on L1D, we evict the least recently used line in the set and insert the new key-block pointer in the line. An entire-line-write-HIT would invoke the within line replacement policy.
Figure 11: The line corresponding to the key found on L2 cache is written through to L1D

Table 1: Read-Write replacement policy for VoxelCache requests for a CPU

| Read/Write | L1D        | L2               |
|------------|------------|------------------|
| Read hit   | Lookup within line | Writeback        |
| Read miss  | Forward to L2    | Return invalid   |
| Write hit  | Overwrite within line | Modified by writethrough |
| Write miss | Evict LRU line; Insert | Modified by writethrough |

Table 2: Cache line replacement policy for VoxelCache requests on a GPU

| Within Line Operation | L1D |
|-----------------------|-----|
| Read hit              | Lookup within line |
| Read miss             | Return invalid    |
| Write hit             | Overwrite block pointer |
| Write miss            | Evict; Write block pointer |

4.3.2 Within Cache Line Items Replacement Policy. A reserved cache line holds multiple key-block pointer items. During loads and stores, we replace the least recently used key-block pointer item present in the cache line. We make use of the within cache line LRU-bits in the cache state to find the least recently used key-block pointer pair within the cache line. These LRU-bits per line are updated each time an insert or lookup operation is performed. Table 3 describes the within line cache update policies in each scenario.

At load time, if the requested key exists in the cache line, the LRU-bits for the cache line are updated and the block pointer corresponding to the key is returned. If the requested key does not exist, an invalid value is returned. At insert time, a modified line along with the within-line LRU bits is written through to all the levels of the cache.

Table 3: Within line cache replacement policy

| Within-line read hit | Within Line Operation |
|----------------------|-----------------------|
|                      | Return data, update LRU bits |
| Within-line read miss| Return invalid value   |
| Within-line write hit| Update LRU bits        |
| Within-line write miss| Overwrite: Update LRU bits |

4.4 Software Interface: ISA Instructions

VoxelCache exposes 5 primitive operations as instructions to the ISA. These instructions control the configuration of the cache and perform accesses to key-block pointer pairs stored in the cache. A summary of their functionality is shown in Table 4. The reserve_cache_lines and unreserve_lines instructions are used to configure and modify cache state to toggle between VoxelCache mode and regular addressability mode. Instructions voxcache_lookup, voxcache_insert and voxcache_remove handle key-block pointer data load, store, or remove from the cache respectively.

Table 4: VoxelCache ISA Instructions

| ISA Instruction                  | Functionality                                                                 |
|---------------------------------|-------------------------------------------------------------------------------|
| reserve_cache_lines              | Invalidates first ways lines of all sets of cache in lvl1 of the memory hierarchy |
| voxcache_lookup state, rd1, rd2, r1 | Takes the 16 bytes of key from rd1, rd2 registers as inputs, outputs the value to r1, if found. |
| voxcache_remove status, rd1, rd2 | Takes the 16 bytes of the key entry from the rd1, rd2 and inserts invalid entry as its value. |
| voxcache_insert status, rd1, rd2, r1 | Takes the 16 byte key entry from rd1,rd2 and inserts the element into cache |
| unreserve_lines                  | Invalidates all VoxelCache reserved lines and changes mode of each line back to addressability mode |

- reserve_cache_lines(m, 1): Communicates to the cache controller to invalidate the first m lines of all sets of the cache at level 1, and set the reserved mode flag for each of the m lines.
- voxcache_lookup: Takes the key input from registers rd1, rd2 and inserts returns the value into output register r1, if found. If the corresponding value is not found, an invalid value is assigned to r1
- voxcache_insert: Derives the key from input registers rd1, rd2 and value from r1 and inserts a VoxelCache store request in the load store queue of the core, containing the pseudoaddress and the key coordinates.
- voxcache_remove: Derives the key input from registers rd1, rd2 and performs an insert operation with an invalid value.
- unreserve_lines: Returns to general mode of execution by invalidating all reserved lines in each set in the cache, and un-setting the reserved mode flag in the cache state of each line.

4.5 Example: VoxelCache Lookup Operation Walkthrough

In CPUs, load and store instructions are handled by virtual memory addresses produced by the address generation unit. In GPUs, each thread in a warp would issue load and store operations to global memory space by inserting requests to a per-SIMT memory access
queue of the load-store unit. We insert VoxelCache store and load operations in the respective load store queues of CPUs and GPUs. Here, we describe the execution of a VoxelCache load operation by the cache controller for CPUs.

Figure 12a and 12b describe a VoxelCache lookup where we reserve 1 way out of 4 and 2 ways out of 8 per set in L1D and L2 respectively, and the key is present at the L2 level. voxcache_lookup inserts a VoxelCache load request in the load store queue respectively. The core computes the pseudoaddress of the key from which the cache controller derives the set index and tag from this pseudoaddress for L1D cache. The set and tag derived from the pseudoaddress for L1D are used to find the corresponding line to look up. If the corresponding tag exists in the cache, it checks the cache line for the required key. If the key is found, the corresponding value is overwritten by the new block pointer.

If the tag is not found at the L1D level, the request is forwarded to L2. The set and tag are now derived for L2. If the corresponding tag exists here, the lookup now proceeds to compare against the keys within the line. Each key within the line is compared with the requested key. If found, this value is returned and line replaces lower level lines in the hierarchy. Otherwise, an invalid value is returned.

5 METHODOLOGY

We model and evaluate VoxelCache on CPUs using the sniper simulator [6]. Table 5 lists the specifications used. We reserve 1 way per set out of a 4-way set associative cache in L1D, and 2 ways per set out of an 8-way associative L2 cache for VoxelCache. For GPU workloads, we use GPGPUSim [21] to model a GPU with specifications mentioned in Table 6. We allocate 1 way out of the 4 ways per set in L1D for VoxelCache.

| CPU 3.6GHz Cascade-lake-like, OOO 4-wide dispatch window, 128-entry ROB; 32 entry LSQ |
| L1D + L1l Cache 32KB, 4 way LRU, 1 cycle; 64 Byte line; MSHR size: 10; stride prefetcher |
| L2 Cache 256KB, 8 way LRU, 4 cycle; 64 Byte line; MSHR size: 10; stride prefetcher |
| L3 Cache 1MB, 16 way LRU, 20 cycle; 64 Byte line; MSHR size: 64; stride prefetcher |
| DRAM 2-channel; 16-bank; open-row policy, 4GB DDR4 |

| Shader core 1.4GHz; 2 schedulers per SM |
| SM Resources 32768 Registers, 32KB Shared memory, 128KB L1D, 4 ways |
| DRAM 2-channel; 16-bank; open-row policy, 4GB DDR4 |

5.1 Workloads and Datasets

Outlined in Table 7 and Table 8 are the workloads and datasets used to run our experiments for CPUs and GPUs respectively. The EuRoC Machine hall dataset [5] is an RGB-D indoor dataset consisting of depth maps and images captured from motion across a large cluttered indoor industrial environment. The KITTI [11] sequence is an outdoor RGB-D dataset captured on driving a vehicle across a neighborhood. These datasets consist of data captured from motion over a relatively large area of space, where a voxel hashing implementation is required to keep track of the environment’s map in memory.

CPU workloads:

- voxblox: Voxblox [32] is a mapping framework for constructing truncated signed distance fields (TSDF) and Euclidean signed distance fields (ESDF) for MAV planning applications.
- infi-CPU: InfiniTAM [34] is a popular framework for large-scale 3D reconstruction with loop closure, built on top of KinectFusion [18].
- fiesta: FIESTA [13] is an efficient mapping system to compute the Euclidean Signed Distance Field (ESDF) map on the fly. The constructed map is used for online motion planning for aerial robotics.
- opchisl: OpenChisel [22] is a dense 3D reconstruction framework for mapping and localization, targeted for Google Tango mobile device.
VoxelCache: Accelerating Online Mapping in Robotics and 3D Reconstruction Tasks

- **c-blox**: c-blox [26] is a TSDF mapping library that is built on top of voxblox, designed for consistency for scalability in very large scale mapping.
- **supereight**: supereight [24] is a TSDF mapping library which uses an efficient octree implementation to store voxel data.

**GPU workloads:**
- **rfsn**: Refusion [33] is a GPU based fast 3D reconstruction and meshing framework that is designed to be robust to dynamic environments.
- **mhash**: Mesh hashing [9] proposes a framework to incrementally generate, update meshes online on the GPU from spatial hashed data structure.
- **inft-GPU**: GPU version of infiniTAM [34], for large scale mobile 3D reconstruction.

| Table 7: CPU Workload configuration |
|-------------------------------------|
| Workload  | Dataset                           |
|-----------|-----------------------------------|
| Voxblox [32] | KITTI Sequence 0027 [11]           |
| OpenChisel [22] | EuRoC Machine Hall Sequence 5 [5] |
| FIESTA [13] | KITTI Sequence 0027 [11]           |
| InfiniTAM [34] | EuRoC Machine Hall Sequence 5 [5] |
| c-blox [26] | KITTI Sequence 0027 [11]           |
| supereight [24] | ICL NUIM dataset [14]             |

| Table 8: GPU workload configuration |
|-------------------------------------|
| Workload  | Dataset                           |
|-----------|-----------------------------------|
| ReFusion [33] | KITTI Sequence 0027 [11]           |
| InfiniTAM [34] | EuRoC Machine Hall Sequence 5 [5] |
| MeshHashing [9] | KITTI Sequence 0027 [11]           |

6 EVALUATION

6.1 Speedup on Map Update

We measure the speedup on map update at different resolutions (at different voxel grid sizes). Depicted in Figure 13 are the speedups obtained at resolutions 5cm, 10cm and 15cm, where we observe average an speedup of 1.57X on CPU and 1.74X on GPU. We observe that we get higher speedups at higher resolutions. On average, at the highest resolution (5cm voxel grid size), we achieve a speedup of 1.45X on CPU and 1.78X on GPU. We conclude that VoxelCache can effectively improve map update times at different resolutions.

6.2 Energy Analysis

Figure 14a and 14b shows the energy savings of VoxelCache normalized to baseline on CPU and GPU workloads respectively at a voxel grid size of 0.05m. VoxelCache on average requires 22% less energy (up to 44%) on CPU and 9.5% (up to 14%) on GPU respectively. VoxelCache consumes less energy for mapping as a result of fewer accesses to DRAM by significantly reducing the number of hash resolutions required, which requires higher energy consumption and leads to longer runtime.

6.3 Comparison to Using a Fully Associative Buffer

We consider the case where we use an idealized fully associative buffer with an LRU replacement policy to store and lookup block pointers using keys and compare the cache miss rates with that of VoxelCache. Note that we count an access to VoxelCache as a hit if the requested voxel block is found in reserved cache lines at any level of the cache hierarchy.

Figure 15a shows the hit rate on using a fully associative buffer for lookups on CPU workloads, using workload configurations as mentioned in Table 7. We observe that the number of cache hits we receive saturates for a buffer size of around 400 elements. We
also observe that the performance benefit we achieve with a fully associative buffer which we achieve cache hit rates which compare closely to that of using VoxelCache. The hit rates for GPU workloads are as shown in Figure 15b. A cache hit is said to have registered when all threads of the warp encounter a cache hit.

With an access latency set to the same as the lookup times for L1D caches, the speedup achieved for a fully associative buffer storing key-value pointers is shown in Figure 16a for CPU workloads, and in Figure 16b for GPU workloads respectively. We achieve a speedup of 1.9x on InfiniTAM-GPU, 1.78x on mesh-hashing and 1.73x on ReFusion for a buffer size of 4096 elements.

6.4 Comparison to Hash Table Accelerator

Hash table accelerator [39] (HTA) enables fast access to hash table containers by proposing a special hash table storage format in memory. HTA packs hash table keys and values into cache-line sized elements which are stored as an array in memory. A key-value pair’s index in the array is derived from the result of a hash function applied on its key. Once a requested cache line is loaded into the cache, HTA is able to achieve fast access with hardware support for key lookup in CPU caches. HTA which uses the same replacement policies for all data used by the application. In contrast to this, our method reserves certain portion of the cache dedicated to key-voxel block pointers, leading to decoupling of map data and other data which our application uses during cache replacement. We compare our results for single threaded CPU workloads with our re-implementation of Flat-HTA, as described in [39]. We observe that on average, VoxelCache has an 8% higher speedup. The comparison between the speedups achieved between our method and with using HTA is shown in Figure 17.

Figure 15: Hit rates vs fully associative buffer size (number of key-block pointer pairs held)

(a) Hit rate vs buffer size observed for CPU workloads

(b) Hit rate vs buffer size observed for GPU workloads

Figure 16: Speedup observed on varying the fully associative buffer size

(a) Speedup on GPU applications

(b) Speedup on GPU applications

Figure 17: Comparing overall speedup between VoxelCache-cached key of CPU workloads vs HTA

We compare the heap allocated memory footprint of HTA and C++ standard library’s std::unordered_map at different load factors, shown in Figure 18. We observe that HTA would require 2X more memory when compared to the standard library implementation. This approach is thus impractical for large maps in resource-constrained edge devices, e.g., autonomous robots, drones or mobile devices. Our implementation is independent of underlying data structure to store voxel blocks, and enables fast accesses to reusable elements of the hash table regardless of the load factor.

6.5 VoxelCache with Octree Data Structures

VoxelCache caches a pointer to a $n \times n \times n$ block of voxels, and is independent of the data structure used for indexing the pointer to the blocks of voxels. Thus, we can use VoxelCache to optimize access latencies in any key-indexed data structure in applications that have a high degree of reuse of keys. In particular, the Supereight [24] project provides an efficient octree implementation.
that stores blocks of $8 \times 8 \times 8$ voxels as leaves in the octree instead of individual voxels as leaf nodes as an octree. We use VoxelCache to further optimize the access times to these blocks of voxels to improve mapping time in Supereight.

Figure 19 shows the speedup obtained on incorporating VoxelCache with supereight. We observe that VoxelCache enables faster scene integration (of up to $1.31 \times$) compared to the baseline implementation. We also note faster raycasting speedups of up to $1.41 \times$ on ray casting for mesh generation.

![Speedup on mapping update of Supereight with VoxelCache](image)

Figure 19: Speedup on mapping update of Supereight with VoxelCache

### 6.6 Overall Application Performance

VoxelCache enables efficient computation of high resolution (<5cm) signed distance field on voxels in large environments on the fly. We have evaluated the impact VoxelCache for the mapping update step alone in our results. To assess the impact of VoxelCache on the overall application, we present the average time taken by InfiniTAM to do iterative-closest-point (localization) and depth integration (mapping) per depth frame input. Table 10 and 9 show the results at resolutions 5cm and 2cm respectively. We observe that at a higher resolution, the time contribution of the mapping step increases significantly leading to overall application speedup ($1.24 \times$ and $1.31 \times$ on CPU and GPU respectively).

#### Table 9: Overall application impact of VoxelCache at voxel size 2cm

| VoxelCache | infT-CPU | infT-GPU |
|------------|---------|---------|
| Disabled   | 186 ms  | 2.69 ms |
| Enabled    | 150 ms  | 2.05 ms |

#### Table 10: Overall application impact of VoxelCache at voxel size 5cm

| VoxelCache | infT-CPU | infT-GPU |
|------------|---------|---------|
| Disabled   | 138 ms  | 2.11 ms |
| Enabled    | 127 ms  | 2.0 ms  |

### 6.7 VoxelCache Area Overhead

The primary area overhead incurred by VoxelCache comes from the additional 3 bits per line on CPUs for the LRU bits and cache state’s mode register introduced for each line of the cache. We evaluate the area overhead of VoxelCache using CACTI-6.5 [23]. In a 32nm node Intel Xeon CPU core, with a 32 KiB L1D, 256 KiB L2 and 1 MiB L3 Cache capacity, on having only the L1D and L2 buffers be able to reserve cache lines, VoxelCache incurs an area overhead of at most 0.098%.

### 7 RELATED WORK

To our knowledge, this is the first work that a) identifies map updates as a significant performance bottleneck and b) proposes a hardware-software mechanism to accelerate large-scale high resolution mapping in 3D reconstruction, SLAM, and robotics applications. Prior work in this area falls into three categories: 1) Faster voxel access methods with special special data structures; 2) Using compression data structures; and 3) Using a faster hash table container. In this section, we discuss each of these types of prior works, and discuss general acceleration techniques on mapping frameworks.

**Faster voxel access methods.** Fast accesses to voxel data could be achieved using special data structures, like b-trees [3, 27] that allow locality aware placement of voxels of close-by regions in memory, resulting in faster map construction [25, 36]. This approach is geared towards storage of large maps to have fewer data movements to and from permanent storage. However, the access times are only comparable to that of voxel hashing [25].

**Compressing voxel data structures.** Several prior works aim to reduce memory footprint while enabling fast access latencies. Octree based approaches [7, 15, 24, 38] allow memory efficient representation by compressing sparse regions of space. However, a tree lookup to access voxel data adds significant overhead leading to larger access times compared to voxel hashing [28].

**Fast voxel hash index.** Faster accesses to hash tables for voxel hashing can be achieved by decreasing the load factor of the hash table. This leads to fewer comparisons and less branching required for each hash table lookup. However, this increases the memory footprint making it infeasible to store larger scenes. For example, Google’s dense_hash_map provides faster accesses compared to C++ std::unordered_map but requires on average 4X the memory required. Hash Table Accelerator (HTA) [39] proposes a special hash table storage format in memory enabling fast accesses to hash table containers. HTA packs key-value pairs into cache-line sized elements stored as an array in memory, and indexed on the result of a hash function applied on its key. With hardware support to derive the HTA array index from the key, HTA is able to achieve faster hash table accesses in CPUs. However, HTA will only apply at low load factors, as each bucket can only accommodate keys and values into cacheline sized memory in DRAM, leading to higher memory use by the container. We compare quantitatively the results of VoxelCache with our implementation of HTA in Section 6.4. The above works trade off scalability of map representation for speed of accesses. Furthermore, HTA is not applicable to frameworks that use other data structures (e.g., octrees) to save voxel data.

**Accelerating Mapping and Reconstruction.** 3D mapping, SLAM and 3D reconstruction tasks consist of a number of common sub-problems like localization, scene integration, place recognition, loop closing, and meshing and rendering. Benchmarking tools to estimate contribution of individual sub-problems to the overall runtime for various SLAM projects have been developed [4, 17]. To speed up mapping in particular, a number of approaches have been proposed. One class of approaches use properties of TSDF updates to reduce the number of voxel accesses and updates that need to be done. For example, Flash fusion [12] stores a lookup table to the addresses of neighboring blocks of voxels to enable faster accesses when performing mesh extraction and TSDF fusion. It also proposes
a sampling technique to select only valid voxels which need to be accessed and (by discarding accesses to the blocks far away from the truncation distance). However, this would not speed up TSDF fusion in cases where the truncation distance is higher, in which case there are more accesses to the blocks in the camera view frustum. Hierarchical voxel block hashing [20], introduces a measure to have an adaptive voxel grid resolution in different parts in the environment, depending on detail. While this allows for a more memory efficient representation, it incurs a higher overhead leading to a lower map update rate. Compared to these approaches, VoxelCache is largely orthogonal and can be used in conjunction with these methods, and unlike these approaches VoxelCache is more generally applicable as it does not make any assumptions about the environment and is effective at any resolution.

8 CONCLUSION

In this paper we present VoxCache, a hardware-software mechanism to enable fast large scale mapping at high resolutions for SLAM and reconstruction applications. The key idea of our approach is to leverage temporal locality of in accesses to voxel blocks and cache voxel block pointers indexed by their coordinate in space in the cache. We provide hardware support to enable fast lookup of recently accessed voxel blocks from the cache given its key. With our approach, we demonstrate speeds of up to 1.45x on CPU and 1.78x on GPU on average for mapping frameworks at a high resolution.

REFERENCES

[1] [n. d.]. Apple Inc. ARKit. https://developer.apple.com/arkit/. Accessed: 2020-09-30.
[2] [n. d.]. Google Inc, AR Core. https://developers.google.com/ar/discover/. Accessed: 2020-09-30.
[3] [n. d.]. NVIDIA Inc, GVD. https://developer.nvidia.com/gvd. Accessed: 2020-09-30.
[4] Mihai Bujancz, Xuesong Shi, Matthew Spear, Pengpeng Zhao, Barry Lennox, and Mikel Luján. 2021. Robust SLAM Systems: Are We There Yet?. In 2021 IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS). https://doi.org/10.1109/IROS5116.2021.9636814
[5] Michael Burri, Janosch Nikolic, Pascal Cohl, Thomas Schneider, Jörn Rehder, Markus Achtelik, and Roland Y. Siegwart. 2016. The EuRoC micro aerial vehicle datasets. The International Journal of Robotics Research 35 (2016), 1157 – 1163.
[6] Trevor E. Carlson, Jorn Rehder, and Shahram Izadi. 2013. Scalable real-time volumetric surface reconstruction. ACM Transactions on Graphics (TOG) 32 (2013), 1 – 16.
[7] Angela Dai, Matthias Nießner, Michael Zollhöfer, Shahram Izadi, and Christian Theobalt. 2017. BundleFusion: real-time globally consistent 3D reconstruction using on-the-fly surface re-integration. ArXiv abs/1604.01093 (2017).
[8] Wei Dong, Jieqi Shi, Weiye Tang, Xin Wang, and Hongbin Zha. 2018. An Efficient Volumetric Mesh Representation for Real-Time Scene Reconstruction Using Spatial Hashing. 2018 IEEE International Conference on Robotics and Automation (ICRA) (2018), 6323 – 6330.
[9] Wei Dong, Jieqi Shi, Weiye Tang, Xin Wang, and Hongbin Zha. 2018. An Efficient Volumetric Mesh Representation for Real-Time Scene Reconstruction Using Spatial Hashing. 2018 IEEE International Conference on Robotics and Automation (ICRA) (2018), 6323 – 6330.
[10] Andreas Geiger, Philip Lenz, and Raquel Urtasun. 2012. Are we ready for autonomous driving? The KITTI vision benchmark suite. 2012 IEEE Conference on Computer Vision and Pattern Recognition (2012), 3354 – 3361.
[11] Lei Han and Lu Fang. 2018. FlashFusion: Real-time Globally Consistent Dense 3D Reconstruction using GPU Computing. In Robotics: Science and Systems.
[12] L. Han, Fei Gao, Boyu Zhou, and S. Shen. 2019. FIESTA: Fast Incremental Euclidean Distance Fields for Online Motion Planning of Aerial Robots. 2019 IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS) (2019), 4423 – 4430.
[13] Ankit Handa, Thomas Whelan, John B. McDonald, and Andrew J. Davison. 2014. A benchmark for RGB-D visual odometry, 3D reconstruction and SLAM. 2014 IEEE International Conference on Robotics and Automation (ICRA) (2014), 1524 – 1531.
[14] Xinmin Hornung, Kai M. Wurm, Maren Bennewitz, C. Stachniss, and Wolfram Burgard. 2013. OctoMap: an efficient probabilistic 3D mapping framework based on octrees. Autonomous Robots 34 (2013), 189 – 206.
[15] Jia Hu, Zhaowei Ma, Yifeng Niu, Wendi Tian, and Wenchao Yao. 2019. Real-Time Trajectory Replanning for Quadrotor Using OctoMap and Uniform B-Splines. In ICRA.
[16] Muhammad Huzafa, Rishi Desai, Samuel Grayson, Xutao Jiang, Ying Jing, Jae Lee, Fang Lu, Yihan Pang, Joseph Ravichandran, Finn Sinclair, Boyuan Tian, Hengzhi Yuan, Jeffrey Zhang, and Sarita V. Adve. 2021. Exploring Extended Reality with ILLIXR: A New Playground for Architecture Research. arXiv:2004.04643 [cs.DC]
[17] Shahram Izadi, David Kim, Omar Hilliges, David Molyneaux, Richard A. Newcombe, Pushmeet Kohli, Jamie Shotton, Steve Hodges, Dustin Freeman, Andrew J. Davison, and Andrew W. Fitzgibbon. 2011. KinectFusion: real-time 3D reconstruction and interaction using a moving depth camera. Proceedings of the 24th annual ACM symposium on User interface software and technology (2011).
[18] Olaf Kähler, Victor Adrian Prisacariu, and David William Murray. 2016. Real-Time Large-Scale Dense 3D Reconstruction with Loop Closure. In ECCV.
[19] Olaf Kähler, Victor Adrian Prisacariu, Julien P. C. Valentin, and David William Murray. 2016. Hierarchical Voxel Block Hashing for Efficient Integration of Depth Images. IEEE Robotics and Automation Letters 1 (2016), 192 – 197.
[20] Muhammad Khairi, Zhesheng Shen, Tor M. Aasland, and Timothy G. Rogers. 2020. Accel-Sim: An Extensible Simulation Framework for Validated GPU Modeling. In 2020 ACM/IEEE 47th Annual International Symposium on Computer Architecture (ISCA). 473 – 486. https://doi.org/10.1109/ISCA4697.2020.00047
[21] Matthew Klingensmith, Ivan Dryanovski, S. Sinha, and J. Xiao. 2015. Chisel: Real-Time Large Scale 3D Reconstruction Onboard a Mobile Device using Spatially Hashed Signed Distance Fields. In Robotics: Science and Systems.
[22] Sheng Li, Ke Chen, Jung Ho Ahn, Jay B. Brockman, and Norman P. Jouppi. 2015. CACTU: An Architecture-level modeling for SRAM-based structures with advanced leakage reduction techniques. 2015 IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS) (2015), 694 – 701.
[23] Robert Maier, Raphael Schaller, and Daniel Cremers. 2017. Efficient Online Surface Correction for Real-Time Large-Scale 3D Reconstruction. ArXiv abs/1709.03763 (2017).
[24] C. Mateo, J. Correas, and Y. Mezouar. 2020. Hierarchical, Dense and Dynamic 3D Reconstruction Based on VDB Data Structure for Robotic Manipulation Tasks. Frontiers in Robotics and AI (2020).
[25] Alexander Millane, Zachary Taylor, Helen Olenyukova, Juan Nieto, Roland Siegwart, and César Cadena. 2018. C-box: A Scalable and Consistent TSDF-based Dense Mapping Approach. In 2018 IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS) (2018).
[26] Ken Musesu. 2013. VDB: High-resolution sparse volumes with dynamic topology. ACM Trans. Graph. 32 (2013), 27:1 – 27:22.
[27] Matthias Nießner, Michael Zollhöfer, Shahram Izadi, and Marc Summinger. 2013. Real-Time 3D Reconstruction at Scale Using Voxel Hashing. ACM Trans. Graph. 32, 6, Article 169 (Nov. 2013). 11 pages. https://doi.org/10.1145/2508363.2508374
[28] Helen Olenyukova, Michael Burri, Zachary Taylor, Juan I. Nieto, Roland Y. Siegwart, and Enric Galceran. 2016. Continuous-time trajectory optimization for online online and offline planning. 2016. IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS) (2016), 5332 – 5339.
[29] Helen Olenyukova, Christian Lanegger, Zachary Taylor, Michael Pantic, Alexander Millane, Roland Y. Siegwart, and Juan I. Nieto. 2020. An open-source system for vision-based micro-aerial vehicle mapping, planning, and flight in cluttered environments. J. Field Robotics 37 (2020), 642 – 666.
[30] Helen Olenyukova, Alexander Millane, Zachary Taylor, Enric Galceran, Juan I. Nieto, and Roland Y. Siegwart. 2016. Signed Distance Fields: A Natural Representation for Both Mapping and Planning.
[31] Helen Olenyukova, Zachary Taylor, M. Fehr, R. Siegwart, and J. Nieto. 2017. Voxelbox: Incremental 3D Euclidean Signed Distance Fields for on-board MAV planning. 2017 IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS) (2017), 1366 – 1373.
[32] E. Palazzolo, J. Behley, Philipp Lottes, P. Giguière, and C. Stachniss. 2019. ReFusion: 3D Reconstruction in Dynamic Environments for RGB-D Cameras Exploiting Residuals. 2019 IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS) (2019), 7855 – 7862.
[33] V. Prisacariu, O. Kähler, S. Golodetz, Michael Sapientza, Tommaso Cavallari, Philip H. S. Torr, and D. W. Murray. 2017. InfiniTAM v3: A Framework for Large-Scale Dense Reconstruction with Loop Closure. ArXiv abs/1708.07083 (2017).
[34] Victor Reijgwart, A. Millane, Helen Olenyukova, R. Siegwart, Cesar Cadena, and J. Nieto. 2020. Voxgraph: Globally Consistent, Volumetric Mapping Using Signed Distance Function Submaps. IEEE Robotics and Automation Letters 5 (2020), 227 – 234.
[36] Ignacio Vizzo, Tiziano Guadagnino, Jens Behley, and C. Stachniss. 2022. VDB-Fusion: Flexible and Efficient TSDF Integration of Range Sensor Data. Sensors (Basel, Switzerland) 22 (2022).

[37] Thomas Whelan, Michael Kaess, Maurice F. Fallon, Hordur Johannsson, John J. Leonard, and John B. McDonald. 2012. Kintinuous: Spatially Extended KinectFusion. In AAAI 2012.

[38] Ming Zeng, Fukai Zhao, Jiaxiang Zheng, and Xinguo Liu. 2013. Octree-based fusion for realtime 3D reconstruction. Graph. Model. 75 (2013), 126–136.

[39] Guowei Zhang and Daniel Sánchez. 2018. Leveraging Hardware Caches for Memoization. IEEE Computer Architecture Letters 17 (2018), 59–63.

[40] Boyu Zhou, Fei Gao, Jie Pan, and Shaojie Shen. 2020. Robust Real-time UAV Replanning Using Guided Gradient-based Optimization and Topological Paths. 2020 IEEE International Conference on Robotics and Automation (ICRA) (2020), 1208–1214.

[41] Boyu Zhou, Jie Pan, Fei Gao, and Shaojie Shen. 2020. RAPTOR: Robust and Perception-aware Trajectory Replanning for Quadrotor Fast Flight. ArXiv abs/2007.03465 (2020).