Using the Automata Processor for Fast Pattern Recognition in High Energy Physics Experiments - A Proof of Concept

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Abstract

We explore the Micron Automata Processor (AP) as a suitable commodity technology that can address the growing computational needs of pattern recognition in High Energy Physics (HEP) experiments. A toy detector model is developed for which an electron track confirmation trigger based on the Micron AP serves as a test case. Although primarily meant for high speed text-based searches, we demonstrate a proof of concept for the use of the Micron AP in a HEP trigger application.

Keywords: Pattern Recognition, Tracking, Trigger, Finite Automata

1. Introduction

Pattern recognition occupies a central role in the reconstruction and analysis chains of practically all High Energy Physics (HEP) experiments. The ability to recognize a charged particle track from a pattern of detector "hits", for example, is extremely important because the trajectory of a particle carries crucial information on its properties and provides a powerful signature to isolate it from unwanted background. With the advent of electronic detectors and readout systems nearly 50 years ago [1], tasks, like the manual scanning of tracks, were transformed into computational problems. Such pattern recognition problems have grown more challenging with every new generation of experiment due to the trend towards more complex event topologies and higher particle densities. To cope with this trend, offline reconstruction applications have so far relied on the rough doubling of transistors in many-core architectures every two years (Moore’s Law), while online applications with real-time requirements have traditionally relied on custom hardware solutions. Unfortunately, Moore’s Law becomes less dependable as we enter a period of diminishing performance returns where power dissipation issues from leakage currents dominate as we approach the atomic scale [2]. On the other hand, custom hardware solutions often entail more technical risks and require more investments in manpower and capital.

In this paper, we take a different approach by exploring emerging commercial technologies designed to deal with the deluge of digital information in today’s data centered economies. One such technology is the Micron Automata Processor (AP) [3] which is specifically targeted at pattern matching applications like those in the Internet search industry and bioinformatics [4–6]. It is a direct hardware implementation of Non-deterministic Finite Automata (NFA) and can simultaneously apply thousands of rules to find patterns in data streams at a constant rate of 1 Gbps/chip. As a proof of concept to demonstrate its feasibility for HEP pattern finding applications, we develop a simple toy detector model typical of those found at modern hadron colliders and use the Micron AP to implement an electron track confirmation trigger.

2. The Automata Processor

2.1. Hardware Architecture

Because the Micron AP is based on a new and radical, non-von Neumann architecture, this section will provide a description of the hardware, focusing on aspects relevant to our evaluation.

2.1.1. A Memory-based Design

The Micron AP is derived from conventional SDRAM technology and its hardware architecture (see Figure 1) is conveniently understood in terms of a two-dimensional memory array. Each input byte on an 8-bit wide bus serves as a rule or address which is presented to an 8-to-2\textsuperscript{8} decoder that selects one out of 256 possible rows. A column of 256 cells in this array, together with additional logic for state information, comprises the basic building block of the AP known as a State Transition Element (STE). Any cell or combination of cells in an STE can be programmed to recognize any subset of 2\textsuperscript{8} possible values or symbols. When the address decoder selects a cell in an enabled column or STE, which is programmed to recognize its associated symbol, the stored value of “1” is output to indicate symbol recognition. This causes the STE output to change state and can be used to enable other downstream STEs. Multiple STEs, each programmed to recognize specific symbols, can be chained together to recognize patterns or strings of symbols. Such patterns need not be limited to ASCII strings and could just as well represent hit addresses associated with a particle trajectory.
in a tracking detector. The interconnections between the STEs is provided by the routing matrix structure, represented by the block at the bottom of Figure 1, which plays the role of the column address and decode operations.

Figure 1: The 2D memory array architecture of the Micron Automata Processor adapted from conventional SDRAM technology.

2.1.2. Reporting Pattern Matches

The Micron AP was specifically designed to perform high-speed pattern recognition. To be useful in this application, there must be an efficient way to tell whether pattern matches were found and provide details on these matches. To this end, any AP building block such as an STE, counter, or boolean can be configured to generate a signal known as a report event whenever it recognizes an input symbol. This way, the last element in a string of STEs programmed to recognize a sequence of symbols in an expression, can generate such a signal to indicate a matching pattern in the input data stream.

Figure 2: Reporting event vector readout architecture.

The portion of the AP architecture relevant to match reporting is shown in Figure 2. The AP is divided into 2 half cores, each of which has 3 output regions. Each region has a local storage area known as the output event memory with room for 1024 output event vectors (or report vectors) that are up to 1088 bits wide. Each vector has a 64-bit preamble used to indicate the offset from the start of the input data stream. The remaining 1024 bits are used to identify the element in the region that generated the report event. In this respect, the AP is unique because it provides both spatial and temporal information on the matches. The maximum number of reporting events per symbol cycle is therefore $2 \times 1088 \times 1024$ events/region/cycle = 6144 events/cycle. The compilation process will fail if the total number of reporting elements exceeds this number.

An output event vector is generated on every symbol cycle for which there was a report event in that region. Since each vector is associated with a symbol cycle, events occurring on the same cycle require a single vector while events on different cycles require separate vectors. When symbol processing completes, the vectors are transferred from each region’s output event memory to the output event buffer, where they can be read by external hardware.

2.1.3. Additional Latencies

Ideally, the total processing time would depend only on the number of input symbols. In reality, there are overheads tied to the internal memory transfers described above which introduce additional latencies. There is an overhead associated with transferring each vector from a region’s event memory to the output buffer. There is also a start-up overhead associated with transferring the first vector to the output buffer. Just to determine that a region is empty also incurs an overhead. The overhead due to transferring each vector depends on its size and can be reduced by configuring the AP to use smaller vectors.

2.2. Programming the Automata Processor

The Micron AP is programmed using tools provided in the AP Software Development Kit (SDK). The process begins by creating a human-readable representation of the automata which can be done through a graphical tool known as the AP Workbench. This representation is transformed into machine-readable form in the compilation step which involves optimization and placing and routing the automata elements onto the AP fabric. This produces a binary relocatable image that is loaded and executed on the AP hardware.

3. Proof of Principle: A Pixel-augmented Electron Confirmation Trigger

To investigate the feasibility of the Micron AP for HEP pattern recognition applications, we consider an electron confirmation trigger application where isolated high $p_T$ electrons are verified and confirmed in a hadron collider detector by matching energy clusters in an electromagnetic (EM) calorimeter with charged particle tracks in a pixel-based tracking detector. A simplified block diagram depicting the trigger hardware architecture is shown in Figure 3. Incoming pixel detector hit data are decomposed into the $R - \phi$ (bend plane) and $R - Z$ (non-bend
A trigger accept signal is required in time. If this condition is satisfied, a pair of reporting events (one from each view) that are correlated and fed into external logic that determines if there is at least one reporting event in each view are read out of each bank in terms of layer, face, module, ROC, and pixel row and column on the ROC. The entire pixel detector is immersed in a uniform solenoidal magnetic field oriented along the z-axis, resulting in charged particle trajectories that are curved in the $R - \phi$ (bend) view and straight in the $R - z$ (non-bend) view.

### Table 1: Toy pixel detector specifications.

| Layer | Radius (cm) | Faces | Modules | ROCs | Pixels ($\phi$) | Pixels ($z$) | Total pixels |
|-------|-------------|-------|---------|------|----------------|-------------|--------------|
| 1     | 2.99        | 12    | 96      | 1536 | 1920           | 3328        | 6389760      |
| 2     | 6.99        | 28    | 224     | 3584 | 4480           | 3328        | 14909440     |
| 3     | 10.98       | 44    | 352     | 5632 | 7040           | 3328        | 23429120     |
| 4     | 15.97       | 64    | 512     | 8192 | 10240          | 3328        | 34078720     |

Length of the toy pixel detector: 54.88 cm

#### 3.1. Toy Detector

For our proof-of-principle studies, we developed a toy detector model consisting of 4 concentric cylinders (layers) approximating the barrel portion of the CMS Phase-1 pixel detector [8]. The geometry and specifications of this model are described in Table 1. All pixels in the entire detector have dimensions measuring $165 \times 98 \mu m$ with the longer axis oriented along the beam axis ($z$). The pixels in each layer form a uniform grid laid out over the entire cylindrical surface. This means that the face of each pixel is really a cylindrical tube segment instead of a flat rectangular area. Each of the 4 detector layers are uniformly divided in azimuthal angle into faces or ladders that are parallel to the $z$-axis and run the entire length of the cylinder. Each ladder is divided in $z$ into 8 equal sections or modules. Each module is further subdivided into 2 rows (along azimuthal direction) by 8 columns (along $z$) of Read-Out-Chips (ROCs). Each ROC, in turn, consists of 80 rows by 52 columns of pixels. Pixels are uniquely identified using a cylindrical coordinate system ($R, \phi, z$), consisting of two orthogonal views which are projections onto the $R - \phi$ and $R - z$ planes. Pixel addresses or coordinates are encoded using the 16-bit and 14-bit data formats shown in Figure 4 for the $R - \phi$ and $R - z$ views, respectively. This format makes it convenient to specify any pixel in terms of layer, face, module, ROC, and pixel row and column on the ROC. Each ROI is divided into 72 overlapping azimuthal sectors, each measuring $25^\circ$ in $\phi$. In the $R - z$ view, layer 1 is divided into 32 equal sections in $z$ and each of layers 2, 3, & 4 into 16 equal sections in $z$. Taken together, the logical divisions in both views form cylindrical tube segments in each layer which we will refer to as tiles. An example of these tiles being used to define the ROIs for track searching is shown in Figure 6.

![Figure 3: Block diagram of Automata-Processor-based electron track confirmation trigger hardware.](image)

![Figure 4: Data encoding scheme for pixel addresses in the $R - \phi$ and $R - z$ views.](image)

For the purposes of defining the regions of interest (ROI) used in detector data readout and defining the pattern banks used by the automata processor (both discussed in more detail below), we divide the pixel detector into logical sections in the $R - \phi$ and $R - z$ views (see Figure 5). In the $R - \phi$ view, the detector is divided into 72 overlapping azimuthal sectors, each measuring $25^\circ$ in $\phi$. In the $R - z$ view, layer 1 is divided into 32 equal sections in $z$ and each of layers 2, 3, & 4 into 16 equal sections in $z$. Taken together, the logical divisions in both views form cylindrical tube segments in each layer which we will refer to as tiles. An example of these tiles being used to define the ROIs for track searching is shown in Figure 6.

Surrounding the pixel detector is a larger concentric cylinder representing the barrel portion of the EM calorimeter with a radius of 129 cm and eta coverage of $\pm 1.479$. We assume a single crystal barrel granularity of 180-fold in $\phi$ (half that of the CMS detector) and $2 \times 85$ fold in $\eta$.
Figure 5: The toy detector is divided into 72 overlapping sectors in the $R - \phi$ view. Examples of two such neighboring sectors, the 12th in red and the 13th in green, each measuring 25° are shown above. In the $R - z$ view, each layer is divided into equal sections in $z — 32$ for layer 1 and 16 for all other layers. Shown in blue, red, and green are examples of combinations of 4 sections (1 from each layer) forming roads of straight tracks originating from the luminous region and within the fiducial volume of the detector.

Figure 6: Two views of an event with 2 EM calorimeter clusters (one of which is represented by the yellow bar in (b)) above the threshold. The search for tracks associated with the clusters is done using only hits in the region-of-interest (ROI) defined by the 4 curved white tiles. There are 2 ROIs in the figure, each pointing at an EM cluster.
3.2. Simulated Events

Simulated events are generated with proton-proton collisions at 14 TeV center-of-mass energies using Pythia 6.4 [9] with CMS Tune Z2* [10] parameters. Each event consists of a $Z \rightarrow ee$ signal interaction overlaid with pileup interactions which are pure Monte-Carlo minimum bias interactions. The number of pileup interactions overlaid on each signal interaction is randomly chosen from a Poisson distribution. The positions of the primary interaction vertices along the $z$-axis are randomly selected from a Gaussian distribution centered at $z = 0$ cm with $\sigma_z = 5$ cm. For simplicity, the transverse positions of the primary vertices are always centered at $x = y = 0$ cm. Figure 7-a shows a 3D view of a simulated event consisting only of a single $Z \rightarrow ee$ signal interaction. Figure 7-b shows an event with a $Z \rightarrow ee$ interaction overlaid with 50 pileup interactions.

Starting from the production vertices, all particles are tracked through the toy detector model with a uniform 4T axial magnetic field. All unstable particles are allowed to decay randomly into a channel selected according to their branching fractions and with exponential decay length distributions based on their proper lifetime. Photons are converted into electron-positron pairs with the appropriate small opening angle distribution at a frequency determined by the pair production cross section (for both nuclear and electronic fields) in the material of the detector concentrated in the 4 pixel detector layers. We use a fictitious sensor module material with an effective $Z$ and density ($\rho$) determined from the various components of an actual CMS pixel sensor module. To keep things simple in this proof-of-concept investigation, no other physics processes such as multiple scattering and energy loss mechanisms are simulated. All charged particles traversing a pixel detector layer generate a single pixel hit for that layer with 100% efficiency. The address of the hit is determined from the coordinates of the intersection of the trajectory with the cylinder. In reality, a charged particle can produce a cluster of neighboring hits in a layer, which could lead to more fake tracks in the pattern recognition stage. This is not included in our simplified simulation. Because our selection criteria requires EM clusters to have $p_T \geq 5$ GeV, only electromagnetic particles (electrons and photons) above this threshold are propagated beyond layer 4 of the pixel detector to the EM calorimeter barrel. Upon reaching the calorimeter, the total energy of such an EM particle is deposited into the calorimeter crystal it intersects to generate an EM cluster.

Four different 1000-event samples were generated having Poisson means for the number of overlaid pileup interactions of $N = 50, 80, 110, & 140$. All four samples used the same set of $Z \rightarrow ee$ signal interactions.

4. Implementing the Track Finder on the Automata Processor

4.1. Basic Automata Network and Principle of Operation

The application of the automata processor as a fast pattern search engine is based on the idea of maintaining a database or dictionary of all possible patterns against which symbols in an input data stream are simultaneously compared for matches [11, 12]. The patterns in this dictionary can be all the possible words in a language or, in our case, all physically possible charged particle trajectories in a tracking detector. In our present case, each possible trajectory is defined by the addresses of 4 pixel hits representing the intersection of the trajectory with each layer of the detector. On the automata processor, each pattern of 4 pixel addresses representing a trajectory in the dictionary is associated with the automata network having the topology shown in Figure 8. As shown, this network consists of 9 columns of 2 STEs each. The pixel addresses are stored in the STE pairs labeled $L_x Lo$ and $L_x hi$ with $x=1,2,3,4$ denoting the detector layer. Since each STE only has 8 bits of symbol recognition
capability, the least and most significant bytes of each address are stored separately in $L_x lo$ and $L_x hi$, respectively. The STE pair to the left of each ($L_x lo, L_x hi$) pair acts as a latch that re-enables the $L_x lo$ STE on its right only on odd clock cycles. This ensures that pair of bytes denoting a pixel address are contiguous and can occur anywhere in the input data stream. The very first pair of STEs on the left of the figure imposes additional constraints for each pattern. Assuming that the very first symbol in an input data stream represents the energy of the EM cluster for which we are trying to find a track match, the STE labeled $ET$ requires this energy to be within the possible range for the stored track pattern. Below this, the STE labeled $Calo$ holds the address of the EM calorimeter crystal that trajectory intersects.

To illustrate the operation of this automata network, consider an input data stream from the detector, consisting of pixel hit addresses read out sequentially by layer, starting from the innermost. Assume that the very first symbol in the input data stream is an 8-bit number representing the EM calorimeter cluster energy and that the second symbol represents the address of the EM calorimeter crystal associated with the cluster. If the energy of the measured cluster falls within the range of the $ET$ STE, its output is enabled, thereby activating the $Calo$ STE. If the crystal address matches that in the $Calo$ STE, this STE enables its output and activates the $L1 lo$ STE. After this point, if a symbol anywhere in the data stream matches that in $L1 lo$, the output of this STE is enabled, activating $L1 hi$. If the immediately following symbol matches that in $L1 hi$, then $L2 lo$ is activated to wait for matching hits in the 2nd layer of the detector. On the other hand, if no match is found for $L1 hi$, we need to keep reactivating $L1 lo$ every other clock cycle until we find a layer 1 match. This is the purpose of the $OC_0a$ pair of STEs which reactivates $L1 lo$ on every odd clock cycle, re-initializing the search for the byte-pair representing the layer 1 hit. These steps are repeated for every detector layer until either 4 matching pixel hits are found or the input data stream is exhausted.

4.2. Generating the Dictionary or Pattern Banks

To generate the pattern banks, we use a single electron gun monte carlo event generator to produce all the possible tracks above $p_T = 5$ GeV. Figure 9 shows the process of generating these patterns for a given region of the detector. We simulate our pattern banks separately for the $R-\phi$ bend view and for the $R-z$ non-bend view [7]. For the $R-\phi$ view, the patterns are generated for each $\pm12.5$ degree $\phi$-sector described earlier in Section 3.1. For the $R-z$ view, we start with the same subdivisions along $z$ in each detector layer described in Section 3.1. We will refer to each division as a window. We take all possible combinations of 4 windows (one from each layer) forming roads containing straight lines originating from the luminous region and ending in the EM calorimeter barrel. Patterns are then generated for each road.

To generate the pattern banks, we use a single electron gun monte carlo event generator to produce all the possible tracks above $p_T = 5$ GeV. Figure 9 shows the process of generating these patterns for a given region of the detector. Electrons of both charges are generated and propagated through the toy detector model described in Section 3.1 generating pixel hits as they traverse each layer. Just as with our simulated $Z \rightarrow ee$ samples that are overlaid with pileup interactions, we do not simulate energy loss or multiple scattering when generating the pattern banks.
To keep the total number of patterns manageable, we use a resolution of 4 pixels for all detector layers in each view. There is a total of 72 pattern banks in the $R - \phi$ view with each bank having ~1163 unique track patterns. Due to the rotational symmetry of the ideal toy detector about the $z$ axis, each bank has an identical set of patterns modulo a rotation in $\phi$. One could, in principle, use a single bank to represent the entire detector in the $R - \phi$ view after the appropriate rotation is applied to the hits of a given sector. We chose not to do this since perfect rotational symmetry may not be present in a real detector. For the $R - z$ view, we consolidate all roads with a common layer 1 and layer 4 window into a single bank resulting in a total of 244 pattern banks. The average number of track patterns in each bank is ~4662. For the ideal toy detector, there is a mirror symmetry about the $x - y$ plane in this view. The set of track patterns in each half are identical modulo a translation in $z$. Again, we chose not to exploit this symmetry since it may not be present in a real detector.

These pattern banks are programmed into the automata processor using the C-API provided in the AP SDK. For each entry in a generated pattern bank, an instance of a macro representing the basic automata network shown in Figure 8 is created by substituting its parameters with the values associated with the current pattern. The resulting automata network containing all instances is then compiled into an object file that is loaded into the automata processor.

We can compile 2,496 instances of the macro shown in Figure 8 onto the current version of the AP chip. Without taking advantage of rotational or translational symmetries, this would require about 34 chips for the $R - \phi$ view and 456 chips for the $R - Z$ view. With the current AP boards that have 4 ranks of 8 chips each, this translates to about 1 board for the $R - \phi$ view and 14 boards for the $R - Z$ view.

4.3. Available Features and Capabilities and Possible Improvement

The simple automata network shown in Figure 8, requiring hits in all 4 layers of the detector, suffices for the present purpose of demonstrating a proof of principle. However, it is possible to design an automata-based algorithm that can deal with missing hits due to inefficiencies in a real detector. An automata network representing a track pattern allowing up to one missing hit in any layer is shown in Figure 10. In the general case when more than 1 missing hit is allowed, the total number of STEs representing a pattern is given by $N_{ste} = 2(2N_l + 2N_m - 3N_m - 1)$ where $N_l$ and $N_m$ are the number of detector layers and number of allowed missing hits, respectively. When there are no missing hits, the total number of STEs is simply $N_{ste} = 4N_l + 2$.

Another interesting feature of the AP is the STE’s ability to recognize a range of values instead of a specific one. This makes it possible to employ variable resolution patterns that offer a way to reduce the total number of patterns in a bank [13].

Lastly, the number of STE’s (18) in Figure 8 needed to represent a specific track pattern is largely due to the limited alphabet size of 8 bits. If our alphabet size were 16 bits, we could reduce the number of STEs by a factor of 3 to just 4 STEs representing the 4 hits plus two additional STEs for the calorimeter energy and position. This would reduce the total number of automata chips needed for our pattern banks.

5. Testing the AP-based Electron Confirmation Trigger with the Simulated Samples

To satisfy the requirements of the electron track trigger application described in Section 3, the AP must, first of all, be able to reconstruct tracks for electron/photons. Secondly, it must be able to accomplish this task within the available latency of the trigger [14]. This section will focus on its track finding ability. The next section will focus on its processing times.

5.1. Testing Procedure

For each of the simulated events described in Section 3.2, we check to see if there are EM calorimeter clusters. Selecting only EM clusters with $p_T > 5$ GeV, we then read out all the
In the R view that the latter knowledge is provided by an independent sub-
structure. The total number of simulated samples overlaid with a di-
sentinel (referred to as a trigger) to originate from the beam axis. The total number of
events and their breakdown into electrons and photons are shown in columns 2-4. Columns 5 and 6 show the number of
electron clusters and photon clusters, respectively, for which a matching track was found. The last three columns show the electron identification efficiency, photon rejection factor, and purity as defined in the text.

In this proof-of-principle study, we also assume single (double) crystal calorimeter resolution in the R view and precise knowledge of the interaction vertex associated with the Z signal. For the purposes of this study, we assume that the latter knowledge is provided by an independent sub-detector system such as an outer tracker based on silicon strips. In the R view, we first construct a straight line defined by the calorimeter cluster coordinates (center of the single crystal) and the primary interaction vertex. We then find the layer 1 and layer 4 windows this line intersects. Together with this pair, all layer 2 and layer 3 windows that form roads (see Section 4.2) with the pair are used to define the ROI extents in the R view. If such a ROI exists within the acceptance of the pixel detector, we will refer to the EM cluster plus primary vertex pair as reconstructable. All the pixel hits within the ROI defined this way are read out sequentially by layer starting with the innermost. The sequence of the hits within each layer in the data stream does not matter to the automata track finding algorithm. This data stream of pixel hits arranged by layer is appended to two 8-bit quantities, the first for the EM cluster energy and the second for the EM calorimeter crystal coordinate. The 8-bit stream is fed into the automata hardware containing the pattern banks corresponding to the ROI. This is done separately for the R and R views. In the hardware, all the instances of the macro represented by Figure 8 associated with the bank are simultaneously presented with the input data stream to generate reports in case of matches. A trigger accept is generated if matches are reported in both views on the same clock cycle.

### 5.2. Results for Electron Identification and Photon Rejection

All reconstructable EM clusters are required to have $p_T > 5$ GeV and to originate from the beam axis. The total number of EM clusters satisfying these criteria for each of the 1000-event simulated samples overlaid with a different number of pileup interactions are shown in the second column of Table 2. A breakdown of these numbers into those originating from electrons and those from photons is shown in the third and fourth columns. The fifth column of the table shows the number of electron clusters for which a matching track was found. The same number for photons is shown in the sixth column.

For this study, we define the electron identification efficiency as $e_\gamma = N_{EM}^{\gamma}/N_{EM}^{\gamma}$ and the photon rejection factor as $R_\gamma = N_{EM}^{e}/N_{EM}^{\gamma}$. $N_{EM}^{\gamma}$ and $N_{EM}^{e}$ are the number of reconstructable EM clusters originating from electrons and photons (columns 3 and 4 of Table 2), respectively, which satisfy the requirements described at the beginning of this section. $N_{EM}^{\gamma}$ and $N_{EM}^{e}$ are the corresponding numbers of EM clusters for which there is a matching track in the pixel detector (columns 5 and 6 of Table 2). The results for $e_\gamma$ and $R_\gamma$ are shown in the last two columns of Table 2. For all samples, we see that the AP algorithm correctly finds a matching track for every electron EM cluster satisfying our requirements. The fraction of photon EM clusters satisfying our requirements that are misidentified increases from 2% to 7% as the number of the pileup interactions in the sample, and hence detector occupancy, increases. The last column in Table 2 shows the purity $P_e = N_{EM}^{\gamma}/(N_{EM}^{\gamma} + N_{EM}^{e})$, which we define as the fraction of all EM clusters satisfying our track trigger requirements that originated from an electron.

### 6. Processing Time

The amount of time it takes the AP to find matching tracks in each view (which we will refer to as symbol processing time) depends only on the number of hits in the ROI. Because we are using 16-bit hits while the AP uses native 8-bit symbols, the total number of input symbols is twice the number of hits. Since one symbol is processed per AP clock cycle, the symbol processing time is simply equal to the number of input symbols. This time does not represent the total processing time since the match results in each view need to be read out of the AP chips and undergo further processing to find coincident matches in each view before making a trigger decision. This additional time includes (a) the internal data-transfer time within the AP to move the match results from the local event memories in the six output regions to the output event buffers (see Section 2.1.2), and (b) the external processing time in external logic to find coincident reports in both views. The internal transfer time depends on the size of the report vectors and their number in each.
of the six regions. In addition, there are overheads associated with determining a region to be empty and a startup overhead for reading the first vector. What we refer to as the external processing time includes the data-transfer time from the AP’s event output buffer to the external logic across the DDR3 interface. The symbol processing and internal data transfer will be collectively referred to as core processing since they both occur on the AP chip. The first subsection below will focus on the core processing followed by a second subsection devoted to the external processing.

6.1. Core Processing Time

To calculate the number of symbol processing cycles, we simply multiply the number of hits by two. For both views, we add an additional symbol cycle to process the 8-bit symbol representing the coordinates of the calorimeter crystal. For the R−φ view, we add one more symbol cycle to account for the 8-bit symbol representing the energy of the cluster.

As we explained earlier, two report events occurring on the same symbol cycle are saved in either the same or different event vectors depending on the output region they occurred in. As we also pointed out, it takes a finite number of symbol cycles to transfer each vector. Because of this, when calculating the internal data-transfer time, we randomly assign a report event to one of the six output regions. This assumes there is no correlation between the automata instances representing all the patterns in our bank and that they are uniformly distributed throughout the 6 regions. We use an event vector divisor of 2 to reduce the vector width to 512 bits and assign the appropriate number of symbol cycles to transfer a vector of this size. We also take into account the overheads associated with “reading” an empty region and transferring the first vector. The symbol processing times plus internal data-transfer times for each view are shown as a function of the simulated sample in Figure 11. For a symbol cycle of 7.5 ns, these translate to 1.29, 1.55, 1.85, and 2.15 µs, respectively, for the 50, 80, 110, and 140 pileup samples in the R−φ view. The corresponding times for the R−Z view are, respectively, 1.49, 1.94, 2.53, and 3.25 µs.

6.2. External Processing Time

After all detector hit data associated with an EM cluster are processed by the AP banks for the R−φ and R−Z views, the last step of our track finding algorithm requires checking for at least one pair of reporting events (one from each view) in which the R−Z event occurred one symbol cycle ahead of the R−φ event. This 1-cycle difference is due to the fact that the automaton representing a track in the R−Z view has one less STE than that for the R−φ view. This requirement does not guarantee a common source for both events, but those that do originate from the same track will necessarily exhibit this correlation in time, and this constraint can only help reduce fake rates.

To estimate the processing time associated with finding at least one pair of correlated reporting events, we implemented the Content Addressable Memory (CAM) reference design described in Reference [16] on a 100 MHz Xilinx Virtex-6 LX240T Field Programmable Gate Array (FPGA). Our studies are based on simulations done using the Xilinx ISE Design Suite. We assume that the report vectors can be read out of the Micron AP’s 8-bit wide bus at 1066 MHz. In our simulations, the 576-bit data (64-bit header + 512-bit reduced-size vector) associated with each vector is read out from the R−Z banks and the 64-bit header containing the temporal information is extracted and written into FPGA memory. Once the headers from all R−Z
Figure 12: The plots above show the number of cycles it takes an Intel Core i7 CPU to process the pixel track trigger algorithm described in Ref. [15]. Plots (a) & (b) show the number of CPU cycles for the single threaded and multithreaded cases, respectively, as a function of the simulated data samples. Dashed-line plots with upright triangular markers are obtained using only EM clusters for which no track match is found. Dashed-line plots with inverted triangular markers are obtained using only EM clusters that have at least one matching track. The solid-line plots and solid circular markers are obtained using all EM clusters. The cycles in these plots are measured using the Intel CPU’s time stamp counter.

7. Comparison with other Processor Architectures

In order to put the AP in better perspective, we compare it with other processor architectures. We implement the pixel-based tracking trigger algorithm described in Ref. [15] on a CPU and a GPU. For this algorithm, which is functionally equivalent to that used on the AP, we assume the same detector layout and parameters, apply the same energy threshold cuts, and look at an identical set of hits contained within a ROI defined in the same way.

The CPU and GPU results in Sections 7.1 and 7.2 are presented within the context of the electron confirmation trigger chosen to demonstrate our proof of concept. The relevant quantity in this case is the total amount of time it takes to process a single event (processing latency) and generate a trigger decision. In order to avoid dropping events, this must be less than the time available to temporarily store an event prior to a trigger decision, which is dictated by the limited size of the event buffers. For the CMS experiment, this available time is on the order of 10 $\mu$s. On the other hand, processing latencies are not as important for other applications like offline reconstruction or online triggers with sufficiently large event buffers. Although such applications may still demand high processing rates, they can easily be satisfied by the addition of more parallel execution units. In Section 7.3 we discuss the CPU performance with this latter case in mind by considering how many processing units (cores) can be used in parallel to achieve the same processing rate as the AP-based system. We do not do this for the GPU since it is much more difficult to determine and control the mapping of threads (and their organization into blocks) to the 15 streaming multiprocessors of 192 cores each, in order to define some processing unit that can be reliably scaled.

Similar approaches to track finding, based on matching patterns stored in a bank, have been implemented using CAMs or Associative Memories (AMs) on FPGAs and custom Application Specific Integrated Circuits (ASICs) [11, 12]. Since comparisons with such solutions provide a more level playing field than with CPUs and GPUs, we conclude this section by briefly describing a recent implementation of an CAM-based track finder on an FPGA and compare its capabilities with those of the AP.

7.1. CPU Comparison

We compile a single threaded C-version of the algorithm described in Ref. [15] using the Intel C compiler (v16.0.1). We then run it on a 3.3 GHz Intel Core i7 (5820K) processor using the same four simulated data samples. Using the Intel CPU’s time stamp counters, we measure the number of CPU cycles to
execute the trigger for each EM cluster and plot the mean as a function of the sample in Figure 12a with a solid line and solid circular markers. For a 0.3 ns CPU clock cycle, these results translate to 3.38, 7.60, 16.7, and 32.1 µs, respectively, for the 50, 80, 110, and 140 pileup samples.

The processing cycles are also shown separately for EM clusters with at least one matching track (dashed line with up-right triangular markers) and EM clusters with no matching tracks (dashed line with inverted triangular markers). Clusters with matching tracks require less processing time because the algorithm quits forming all possible combinations of 4 hits as soon as a matching track is found. The opposite is true for clusters with no matching tracks since the algorithm ends up attempting all possible combinations.

These results clearly exhibit a quadratic rise in processing times which increases by at least an order of magnitude in going from 50 to 140 pileup interactions. In contrast, the results in Figure 11 show that the AP processing times scale almost linearly as the number of pileup interactions in the samples is increased. The processing times increase only by less than a factor of 2× in going from 50 to 140 pileup interactions.

Using OpenMP, we created a multithreaded version of the code described above and compiled it with the same version of the Intel C compiler. The results for this multithreaded implementation on the Intel CPU described above, with 6 physical cores (12 logical cores because of Hyper-Threading), are shown in Figure 12b for the four simulated samples. This implementation runs the algorithm using 2 OpenMP threads on each of the 6 physical cores. The meanings of the markers and line types used in the plot are identical to those in Figure 12a. The average processing times are 5.23, 7.85, 11.7, and 17.5 µs, respectively, for the 50, 80, 110, and 140 pileup samples. The result for the 140 pileup sample is ~ 2× faster than the single threaded CPU result and ~ 5× slower than the AP result.

The plots in Figure 13 show the processing cycles as a function of the number of OpenMP threads for each simulated sample. These results show that using more threads becomes more advantageous as the number of hits (which increases with number of pileup interactions in the sample) that can be processed in parallel increases. However, as the plot for the 140 pileup sample indicates, using more cores only helps up to a certain point. Processing performance flattens out beyond 3 physical cores (6 threads) and begins to worsen when we exceed 2 threads per physical core (beyond 12 threads). Increasing the number of cores beyond a certain point has no effect in reducing the single-event processing time.

7.2. GPU Comparison

We also implemented the algorithm described in Ref. [15] on an nVidia Tesla K40c GPU (745 MHz) using nVidia’s CUDA programming environment. In this case, the loops over 4-layer hit combinations were unrolled using parallel thread blocks where each thread block dealt with one hit combination from Layers 1 and 4. Multiple threads in each block then dealt with Layer 2 and 3 hit combinations in parallel. The number of processing cycles as a function of sample for the GPU are shown in Figure 14. The processing cycles are measured using the host Intel CPU’s time stamp counter. The three different types of markers used have the same meaning as in Figure 12.
The GPU results do not show improvement over the CPU results, mainly because it is more complicated for the GPU to break out of a loop upon the first successful track match, or for it to skip to the next iteration of a loop through continue statements. This makes the execution time dependent on the slowest thread. The parallel capabilities of the GPU (with 2880 cores) are also not fully exploited by our test case where we have significantly reduced the combinatorics by considering only hits within the ROI. Furthermore, one must also take into account additional latencies associated with data transfers between the CPU and GPU, which contribute an additional > 91K CPU cycles (> 27 µs) to the total cycles (time). One place where the GPU does better, however, is on events in the tail of the execution time distributions of the CPU. Such events have little influence on the spread of the GPU distributions because the GPU excels at dealing with problems that have more massive parallelism.

The algorithm described in Ref. [15] used in the CPU/GPU comparisons above is functionally but not algorithmically equivalent to our automata-based track finder. Using regular expressions to represent hit patterns, we also implemented an algorithmically equivalent NFA-based solution on the same GPU used above. We measure ~ 10 seconds to execute the algorithm for each cluster which is about 6 orders of magnitude longer than on the AP.

7.3. Note on CPU Processing Rate

For applications in which the processing latency is irrelevant and only the processing rate matters, it is interesting to see how many CPU cores it takes to process events in parallel in order to match the rate of the AP-based system. Using the results for the sample overlaid with 140 pileup interactions and assuming that the $R - \phi$ and $R - Z$ views are done in parallel, the average single-event processing time (including the external processing time) for the AP-based system is 3.62 µs, which is equivalent to an event rate of approximately 276 kHz. Since the corresponding time on a single core of the Intel i7 CPU is 32.1 µs, it would require about 9 CPU cores to match the processing rate of an AP-based system consisting of 490 AP chips.

7.4. Associative Memories on an FPGA

Unlike ASICs, FPGAs are programmable, off-the-shelf devices and should offer a fair comparison with the AP. Reference [17] describes the development of a Pattern Recognition Associative Memory (PRAM) on modern FPGAs as part of Fermilab’s tracking trigger R&D program for the LHC experiments. The PRAM, which is based on CAMs, is implemented using a mid-range Xilinx Kintex UltraScale KU040. Up to 4,000 patterns, for a detector consisting of 6 layers with 15-bit hit addresses, were stored, consuming 78% of the FPGA resources [18]. The device was successfully operated at 250MHz with a fixed output latency of 7 clock cycles. It is also important to note that, in this design, hits from all 6 detector layers are presented simultaneously to the PRAM on 6 parallel 15-bit input buses, in contrast to the single 8-bit bus of the AP. The FPGA has an advantage over the AP in terms of maximum pattern capacity per chip and pattern finding speed. The advantage of the AP over the FPGA is in the ease with which it can be programmed using the Micron AP SDK.

8. Conclusion

We have demonstrated a proof-of-concept use of the Micron Automata Processor in an electron track confirmation trigger for HEP. Even the current, first version of this technology shows some promise for HEP trigger applications requiring low processing latencies. In the AP’s current form, CAM-based FPGA and ASIC implementations still surpass it in terms of pattern storage capacity and processing performance. It is clear that for specialized applications requiring the highest performance, such as the most demanding aspects of the lowest level trigger in a high-luminosity LHC environment, custom ASIC-based solutions may be the most sensible if not the only approach. However, the availability of an off-the-shelf, dedicated pattern matching engine that is easy to program and suitable for HEP applications, provides a new alternative for situations (e.g. less demanding triggers and offline reconstruction) in which custom or even FPGA-based solutions would not have been considered previously.

Compared with other commodity off-the-shelf solutions like CPUs and GPUs, the AP requires a factor of over two orders of magnitude fewer hardware cycles to perform our sample track finding application. With a clock cycle of 7.5 ns on the AP versus 0.3 ns on the CPU, this lower hardware cycle count translates into a processing latency of 3.64 µs on the AP that is ~ 5× lower than that of the multithreaded CPU implementation. Lower processing latencies are crucial for the online trigger application considered in this paper. On the other hand, if we disregard processing latency and pay attention only to processing rate, it requires only 9 CPU cores to achieve the same processing rate as an AP-based system consisting of 490 AP chips. Such requirements can be satisfied by a commodity server with dual 6-core CPUs.

When comparing the results, one must keep in mind that the Intel CPU used in this study is the 5th generation of a very mature technology. Pre-production evaluation versions of the AP are only becoming available now at the time of this writing. In our evaluation, we were also conservative in our choice of configurable parameters such as the size of the report vectors. Choosing a smaller size can further reduce the times associated with the internal transfer and readout of these vectors. Future versions of the AP may also incorporate larger alphabet sizes. Doubling the current symbol recognition capability from 8-bits to 16-bits, for example, will cut the time to process 16-bit hit addresses in our track finding algorithm in half. The possibility of such improvements, coupled with the results presented in this paper, suggest that this may be a promising technology worthy of more detailed consideration in real-world HEP pattern recognition applications. Lastly, this signifies the first use of this interesting technology to the recognition of visual patterns. It opens up a whole new realm which may even include image processing applications in fields like astronomy.
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