A fast TIADC calibration method for 5GSPS digital storage oscilloscope

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Abstract: Time-interleaved analog to digital convertor (TIADC) is widely used in engineering to increase the sample rate of acquisition system. However, the mismatches between sub-ADCs in TIADC system result in the distortion of sample output and decrease the sample performance. This paper focuses on the calibration of offset, gain and timing skew mismatches. A novel method based on statistical theory is proposed to estimate offset mismatch of each channel. This method can reduce the impact of noise on offset mismatch calibration. The amplitude of main spectrum is utilized to calibrate gain mismatch, and the average value of each sub-ADC is employed to calibrate timing skew mismatch. Meanwhile, gain mismatch and timing skew mismatch are calibrated by STPNM (Simplified Three Point Newton’s method). The proposed calibration method is implemented in a four-channel TIADC based digital storage oscilloscope whose sample rate is 5GSPS. The experiment results show that the impact of mismatches can be reduced effectively and the calibration can be finished in a short time because the convergence is very fast.

Keywords: TIADC, digital storage oscilloscope, Newton’s iteration, mismatch calibration.

Classification: Circuits and modules for electronic instrumentation

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1 Introduction

High speed and high resolution analog-to-digital converter (ADC) is a key building block in modern telecommunications and instrumentation [1]. In practice, the sampling rate and resolution of ADC are limited by the process technology of IC fabrication. Time-interleaving is an effective structure to increase the sampling rate of TIADC (Time-Interleaved ADC) beyond the process technology limit [2]. However, the performance of TIADC are significantly degraded by the mismatches among each ADC branch, such as offset, gain and timing skew mismatches [3, 4].

In the last few decades, numerous studies have attempted to estimate and compensate for the mismatch errors in TIADC. These studies have proposed different mismatch model and calibration method, and have pushed the development of researches on TIADC greatly. The impact of mismatches in TIADC has been researched in [2]-[4]. Some researches focus on the estimation of TIADC mismatches [5]-[6] and the digital compensation method of
TIADC mismatches [7]-[11]. The digital compensation methods include interpolation [7], multichannel filter [8], fraction delay filter [9]. However, if the mismatches is first estimated and then calibrated, because of the estimation accuracy and the compensation error of filter, there may be residual error after calibration. Therefore, adaptive calibration of TIADC mismatches is researched in [10]-[12]. In [10], a synthesis calibration method is proposed to calibrate the three mismatches together, but the partial derivative should be calculated in calibration, and cannot be realized easily in engineering. The method proposed in [11] employs a signal generator to calibrate mismatches. Although the calibration gets high accuracy, signal generator should be added in TIADC system.

In the application of instrumentation, TIADC is a core component of the sampling system in digital oscilloscope. In practice, the calibration is needed to capture signal accurately before measurement. Thus, the major requirement of calibration in this situation is fast. Besides, it is hoped that the calibration method can be implemented with no additional circuits added. Thus in this paper, we propose a fast TIADC calibration method for digital storage oscilloscope (DSO) using existing FPGA in DSO. Since offset, gain and timing skew mismatches are the leading causes of mismatch errors in TIADC, this paper focuses on compensation of these three mismatches. Fast calibration methods are proposed to mitigate the mismatch errors in a 4-channel 5GSPS TIADC based digital storage oscilloscope in this paper.

The contributions of this paper are summarized as follows. First, a novel method based on statistical theory has been proposed to estimate offset mismatch of each channel. This method uses histogram to represent the distribution of data and by setting a threshold to reduce the effect of unexpected phenomenon, like spike interference, inter symbol interference, power interference, etc. Second, a FFT-based calibration method is proposed to compensate for gain mismatch, which uses STPNW (Simplified Three Point Newton’s method). Third, we propose a fast method to compensate for timing skew mismatches which also utilizes the STPNW. The proposed methods are easier to implement in hardware, such as FPGA (Field Programmable Gate Array), and converge very fast.

The rest of this paper is organized as follows. In Section 2, a brief introduction of mismatches in TIADC and digital storage oscilloscope architecture are given. Section 3 gives the mathematical derivation of STPNM algorithm. In Section 4, the calibration method for offset, gain and timing skew are described. Section 5 presents the experiments results obtained from 5GSPS DSO system to validate the proposed method. Section 6 gives the conclusions of our work.

2 TIADC model and digital storage oscilloscope architecture

In this section, we derive a system model for TIADC to analyze the impact of offset, gain, and timing skew mismatches and give a description of digital storage oscilloscope architecture.
2.1 TIADC model
Time-interleaved architecture consists of \( M \) parallel ADCs operating in a time-interleaved manner. Each sub-ADC operates with a sampling frequency of \( f_s/M \) while the overall system has a sampling rate of \( f_s \). Ideally, each ADC should have same gain, offset and the input signal should be uniformly sampled. However, due to fabrication imperfection, mismatch errors will be introduced in TIADC system.

![Mismatch model of TIADC system.](image)

The system model are shown in Fig.1 where \( g_k \), \( o_k \) denote gain and offset of \( \text{ADC}_k \), and \( \Delta T_k \) represents the time deviation from ideal sampling instant. The output of the TIADC system can be represented as

\[
y[n] = \sum_{k=0}^{M-1} (g_k x(nMT_s + kT_s + \Delta T_k) + o_k) \tag{1}
\]

If the input signal is a sinusoidal, i.e. \( x(t) = A \sin(\Omega_0 t) \), the fourier transform of the TIADC output with overall sampling rate \( \Omega_s \) rad can be represented as [2]

\[
Y(j\Omega) = \frac{2\pi}{T_s} \sum_{k=-\infty}^{\infty} [\alpha[k] \delta(\Omega - \Omega_0 - k\frac{\Omega_s}{M}) - \alpha^{*}[M-k] \delta(\Omega + \Omega_0 - k\frac{\Omega_s}{M})] + \beta[k] \delta(\Omega - k\frac{\Omega_s}{M}) \tag{2}
\]

where

\[
\alpha[k] = \frac{A}{j2M} \sum_{l=0}^{M-1} g_k e^{-j\Omega_0 \Delta T_k} e^{-jkl\frac{2\pi}{M}} \tag{3}
\]

\[
\beta[k] = \frac{1}{M} \sum_{l=0}^{M-1} o_k e^{-jkl\frac{2\pi}{M}} \tag{4}
\]

2.2 Digital storage oscilloscope architecture
Fig. 2 shows the simplified block diagram of 5GSPS digital storage oscilloscope, which consists of analog channel, ADC, FPGA and digital signal processor (DSP), etc. The analog channel is utilized to amplify or attenuate
the input signal of DSO to adapt to the valid input range of ADC. It is shown that the analog channel includes operational amplifier (OA), digital step attenuator (DSA), etc. The part number of ADC is EV10AQ190 [13], whose sample rate is 5GSPS. The internal structure of this ADC is also shown in Fig. 2. It can be seen that EV10AQ190 is a four-channel TIADC composed of four ADC cores, and the offset, gain and sample phase can be adjusted independently. The sample data of ADC are transmitted to FPGA, and then received by ISERDESE which is a FPGA primitive of Xilinx company. Sample data are stored in FIFO (first in first out) of FPGA. Besides of data reception and storage, ADC control, DSP interface and time-base control are also implemented in FPGA. The DSP is the mainly control part of DSO. All hardware such as ADC, DSA and the modules in FPGA are controlled by DSP. The sample data stored in FIFO are transferred to DSP through DSP interface module, and then processed by DSP. These processes include decimation, interpolation and sample data to waveform conversion, etc. The graphic user interface is also realized in DSP.

3 Simplified Three Point Newton’s method (STPNM)

Newton’s method is a fast iterative method to find the roots of the function. In optimization problem, Newton’s method is applied to find the stationary point of the function. Supposing the function is \( f(x) \), the stationary point \( x_0 \) of \( f(x) \) satisfying \( f'(x_0) = 0 \).

The second Taylor expansion of \( f(x) \) near \( x_n \) is

\[
f(x_n + \Delta x) \approx f(x_n) + f'(x_n)\Delta x + \frac{1}{2} f''(x_n)\Delta x^2
\]  

where \( \Delta x \) is a small deviation from \( x_n \). The stationary point can be derived by setting the derivative of equation (5) with respect to \( \Delta x \) equal to zero, which can be written as

\[
\frac{df(x_n + \Delta x)}{d\Delta x} = f'(x_n) + f''(x_n)\Delta x = 0
\]  

Solving the equation, we can get

\[
\Delta x = -\frac{f'(x_n)}{f''(x_n)}
\]
Thus, by using the Newton’s method, one can get a better approximation of the stationary point which is

\[ x_{n+1} = x_n + \Delta x = x_n - \frac{f'(x_n)}{f''(x_n)} \]  

Our goal is to reduce the mismatch errors as much as possible, thus it is an optimization problem in essence. We can make use of Newton’s method to compensate for the mismatch errors. However, in practice, we don’t know the exact optimization function, so we cannot derive the first and second derivatives of the function directly. Thus we propose the STPNM to implement calibration. The algorithm is shown as follows.

Assuming there are three testing points \( x_1, x_2, x_3 \) satisfying \( x_1 < x_2 < x_3 \) and their corresponding function values are \( f(x_1), f(x_2), f(x_3) \) respectively. The first derivative of \( f(x) \) around \( x_2 \) can be estimated by

\[ f'(x_2) = \frac{f(x_1) - f(x_2)}{x_1 - x_2} \]  

And the first derivative of \( f(x) \) around \( x_3 \) is

\[ f'(x_3) = \frac{f(x_2) - f(x_3)}{x_2 - x_3} \]  

Thus, we can get the second derivative of \( f(x) \) around \( x_2 \) as

\[ f''(x_2) = \frac{f'(x_2) - f'(x_3)}{x_2 - x_3} = \frac{f(x_1) - f(x_2)}{(x_1 - x_2)(x_2 - x_3)} - \frac{f(x_2) - f(x_3)}{(x_2 - x_3)^2} \]  

Assuming \( x_3 - x_2 = x_2 - x_1 = \Delta x \), it can be derived that

\[ f''(x_2) = \frac{f(x_1) + f(x_3) - 2f(x_2)}{\Delta x^2} \]  

Then we can calculate a better approximation of the stationary point as given in (8).

The following section describes the calibration procedures for gain and timing skew mismatches which employ STPNM in detail.

4 Calibration method

4.1 Offset Error Calibration

In most previous offset calibration method, the offset value of each channel are derived by making an average of the sampled output of corresponding sub-ADCs. However, if determinate noise exists during the measurement, the estimated value deviates from the real offset mismatch. We will illustrate that as follows.

Let output of the \( k \)th \( (k = 0, \ldots, M - 1) \) sub-ADC be \( y_k(n) \) when there is no analog input, which can be expressed as

\[ y_k(n) = v_{k1}(n) + v_{k2}(n) \]  

where $v_{k1}(n)$ is the random noise and $v_{k2}(n)$ is the determinate noise. The random noise $v_{k1}(n)$ is caused by the thermal noise while the determinate noise may be caused by several unexpected phenomenon, like spike interference, inter symbol interference, power interference, etc.

Assuming $v_{k1}(n)$ is a White Gaussian Noise (WGN) with mean zero and standard deviation $\sigma_{k1}$. Suppose there are $N$ samples, the average of the $N$ sample points can be expressed as

$$y_{ka}(n) = \frac{1}{N} \sum_{n=1}^{N} (v_{k1}(n) + v_{k2}(n)) = \frac{1}{N} \sum_{n=1}^{N} v_{k1}(n) + v_{k2}(n)$$

(14)

The standard deviation of the average of $v_{k1}(n)$ is $\sigma_{ka} = \sigma_{k1}/\sqrt{N}$, which is decreased after average. However, due to the existence of determinate noise, there are second component appearing in the equation (14). This component is a fixed value and does not vary with average process thus it makes the output $y_{ka}(n)$ as a biased estimate of the offset value.

In this subsection, we propose a novel method based on the statistical theory. Since the determinate noise appears in a low probability, we can use the statistical theory to remove those noise so that we can get a better estimate of the offset value. The key procedure in our method is deriving the histogram of the TIADC output as shown in Figure 3.

![Fig. 3. Histogram of the TIADC sampled value.](image)

In Fig.3, the horizontal axis is the value of the sampled output while the horizontal axis is the number of times of the specific value. By eliminating the output sample with lowest probability according to the histogram, we can reduce the effect caused by the determinate noise $v_{k2}(n)$. In the proposed method, a threshold $T$ is chosen, which can be expressed as

$$N_k(l) = \begin{cases} 
N_k(l), & |N| \geq T \\
0, & |N| < T
\end{cases}$$

(15)

where $N_k(l)$ is the times of $k$th sub-ADC output value after average process and $l$ represents $l$th bin of the histogram. The estimated offset value of $k$th sub-ADC is hence given by

$$\hat{o}_k = \frac{\sum_{l=1}^{N} N_k(l)X(l)}{\sum_{l=1}^{N} N_k(l)}$$

(16)

where $X(l)$ is the $l$th bin offset value. Then we can eliminate the offset errors based on the estimated offset value using either digital or analog technique.
4.2 Gain Error Calibration

For a sinusoidal input signal, whose expression is

\[ x(t) = A \sin(\Omega_0 t + \phi) \]

(17)

Considering the gain, the offset and the timing skew errors in the \( k \)-th channel, we can get its expression in frequency domain

\[ X_k(j\Omega) = \frac{A\pi}{j} [\delta(\Omega - \Omega_0)e^{j\phi}e^{-j\Omega_0 T_k} - \delta(\Omega + \Omega_0)e^{-j\phi}e^{j\Omega_0 T_k} + 2\pi o_k\delta(\Omega)] \]

(18)

where \( X_k(j\Omega) \) is the continuous-time Fourier transform (CTFT) of \( x_k(t) \) in Fig.1.

Form Fig.1 and the principle of TIADC, the sampling impulse of TIADC is represented as

\[ P(t) = \sum_{n=-\infty}^{\infty} \delta(t - kT_s - nMT_s) \]

(19)

The Fourier transform of (20) is

\[ P(j\Omega) = \frac{2\pi}{MT_s} \sum_{n=-\infty}^{\infty} \delta(\frac{\Omega - n\Omega_s}{M})e^{-jn\frac{2\pi}{M}} \]

(20)

where \( \Omega_s = 2\pi/T_s \).

Thus the CTFT of output for \( k \)-th channel \( (y_k(t) = x_k(t) \times p(t)) \) is expressed as

\[ Y_k(j\Omega) = \frac{A\pi}{jMT_s} g_k \sum_{n=-\infty}^{\infty} [\delta(\Omega - \Omega_0 - n\Omega_s/M)e^{j\phi}e^{-j\Omega_0 T_k} \]

\[ - \delta(\Omega + \Omega_0 - n\Omega_s/M)e^{-j\phi}e^{j\Omega_0 T_k} + 2\pi o_k\delta(\Omega - n\Omega_s/M)e^{-jn\frac{2\pi}{M}}] \]

(21)

From (21), we know that the amplitude of spectrum at \( \Omega_0 \) is depended on the gain of \( k \)-th channel. If there is no gain mismatch, amplitude of spectrum at \( \Omega_0 \) for all channels will be equal, and it can be utilized as a criterion to calibrate gain mismatch. By making FFT of the samples from each channel, we can get \( M \) FFT spectrum with different magnitude. Choosing one channel as the reference channel. Then by multiplying a gain value to make other channel’s main spectrum identical to the reference channel.

The goal of gain mismatch calibration is to adjust the gain of each channel so that the main spectrum of various sub-ADCs can be matched. The adjustment method is based on the STPNM. The objective function \( f(x) \) can be defined as the square of the main spectrum difference value between adjust channel and reference channel.

We utilize channel 2 as an example to illustrate gain calibration process. First, we choose the initial value \( g_2 \) for ADC 2, and we can get the difference of main spectrum \( f(g_2) \) between the reference channel and channel 2 with input \( g_2 \). Second, by choosing the value of \( g_2 + \Delta g \), we get the function value \( f(g_2 + \Delta g) \) with input \( g_2 + \Delta g \). Third, by choosing the value of \( g_2 - \Delta g \), we get the function value \( f(g_2 - \Delta g) \) with input \( g_2 - \Delta g \). Fourth, we use the
equation (8) to find the better approximation of stationary point of function. Repeating the process until we find the value lower than the threshold we have set.

It should be noted that the spectrums must have the same standard, i.e. the number of points should be equal so that the magnitude of FFT can be compared, and should not be normalized.

4.3 Timing Skew Error Calibration

For a sinusoidal input signal shown in (17), the output of the \( k \)-th is

\[
y_k[n] = A g_k \sin(\Omega_0 ((nM + k)T_s + \Delta T_k) + \phi) + o_k
\]

If all mismatches is calibrated, i.e. \( g_k = 1, o_k = 0 \) and \( \Delta T_k = 0 \), (22) is rewritten as

\[
y_k[n] = A \sin(\Omega_0 ((nM + k)T_s) + \phi)
\]

Moreover, when the sample frequency of TIADC is equal to frequency of input signal, (22) is rewritten further as

\[
y_k[n] = A \sin(2\pi ((nM + k)) + \phi)
\]

Because the period of sinusoidal function is \( 2\pi \), the output for any \( k \) is equal. This demonstrates that when signal frequency is equal to sample frequency of TIADC, the sample output of each channel should be equal if there is no mismatch in TIADC. However, due to the existence of timing skew mismatch, the sample outputs of each channel are not same, which can be clearly seen from Fig.4. Therefore, we can compensate for timing skew mismatch using STPNM by adding appropriate time delay to make the sample outputs from each channel identical.

It should be noted that in the process of sampling, noise is unavoidable thus we need to take a consideration of the noise. We make an average of samples from each channel respectively and obtain average values of the signal. Then we can use the proposed method to calibrate the timing skew mismatch error.

![Fig. 4. Timing skew effects in a four channel TIADC system.](image)

Therefore, when gain and offset errors are calibrated, the average of each channel can be used as a criterion to calibrate timing skew error. If the aver-
age of each channel is equal, the calibration of timing skew error is finished. STPNM is also utilized in timing skew error calibration. The objective function $f(x)$ is defined as the square of the mean difference value between adjust channel and reference channel. The procedure of calibration is just similar as gain mismatch with $g$ replaced by $\Delta T$.

5 Experiment results

The proposed calibration method is implemented in 5GSPS DSO whose simplified diagram is shown in Fig. 2. The FFT and average process needed by proposed method are realized in FPGA. The statistic calculation for offset calibration is implemented in DSP. The adjust elements in ADC are employed to calibrate mismatches. The range for adjustment of offset, gain and phase is 40LSB, 10% and 15ps respectively. The step for adjustment of offset, gain and phase is 0.04LSB, 0.02% and 30fs respectively. The ADC provides registers controlled by SPI (serial peripheral interface) bus interface to adjust offset, gain and phase of each ADC core.

![Fig. 5. Sampled value of a 4-channel 5GSPS DSO with no input.](image)

In the proposed method, we need to estimate and calibrate offset mismatch errors firstly. Fig. 5 (a) and (b) shows the sampled value before and after offset calibration respectively. We use 1,200 points to get the histogram and eliminate the value with lowest times. Then we use weighted average algorithm to get the estimated offset value of each ADC core. The estimated values for four ADC core is 129.238, 127.728, 129.464 and 128.236 respectively. After the offset calibration, the mean value of each core becomes 129.383, 129.366, 129.082 and 129.1848 respectively. The offset mismatch have been considerably reduced by the proposed method.

After offset mismatch calibration, gain mismatch needed to be compensated. We adopted the 250MHz sinusoidal signal as the input. The DCW (Digital Control Word) value and the corresponding function value for ADC core B, C, D are represented in the Table I. The function $f(x)$ is chosen as square of main spectrum difference between calibrated channel and reference
channel. The threshold is set as 0.0025 in experiment. From the table, it can be seen that the STPNW converges after 2, 2 and 3 iterations for ADC core B, C and D respectively, which is fast compared to most iterative methods. The magnitude of main spectrums for four ADC cores after gain calibration are given as 81.70dB, 81.69dB, 81.71dB, and 81.70dB respectively. The main spectrum differences among each channel are no more than 0.01dB, thus the gain mismatch calibration achieves good performance.

Then we consider timing skew mismatch. At the start of timing skew calibration, the sample clock frequency is changed to 500MHz. This is because the bandwidth of our DSO is 1GHz. When the sample clock frequency is set to 500MHz, the sample frequency of whole ADC is 1GHz. Therefore, the set of TIADC system meets the demand that signal frequency is equal to sample frequency. After calibration, the sample clock is set to 2500MHz to recover the 5GSPS sample rate of DSO. In our DSO, the sample clock is generated by phase lock loop (PLL), whose part number is LMK04806. The frequency change is realized by changing the frequency division ratio, i.e. write control word to register in PLL by SPI control bus.

The DCW value and the corresponding function value for ADC core B, C, D are illustrated in the Table II. The function \( f(x) \) is chosen as square of mean value difference between calibrated channel and reference channel. The threshold is set as 0.05 in the experiment. From the table, it can be seen that the STPNW converges after 1, 6 and 2 iterations for ADC core B, C

### Table I. The DCW value and the corresponding function value for gain mismatch calibration

|       | DCW_B | \( f_B \) | DCW_C | \( f_C \) | DCW_D | \( f_D \) |
|-------|-------|---------|-------|---------|-------|---------|
| Initial | 512   | 0.0025  | 512   | 0.0196  | 512   | 0.0001  |
| 1st iteration | 506   | 0.0036  | 666   | 0.0196  | 537   | 0.0036  |
| 2nd iteration | 502   | 0.0025  | 613   | 0.0036  | 520   | 0.0004  |
| 3rd iteration | \( \_ \) | \( \_ \) | 600   | 0.0001  | \( \_ \) | \( \_ \) |

### Table II. The DCW value and the corresponding function value for time mismatch calibration

|       | DCW_B | \( f_B \) | DCW_C | \( f_C \) | DCW_D | \( f_D \) |
|-------|-------|---------|-------|---------|-------|---------|
| Initial | 512   | 0.0608  | 512   | 2.3654  | 512   | 1.5129  |
| 1st iteration | 554   | 0.0472  | 724   | 0.7895  | 729   | 1.9481  |
| 2nd iteration | \( \_ \) | \( \_ \) | 671   | 0.0653  | 626   | 0.0195  |
| 3rd iteration | \( \_ \) | \( \_ \) | 699   | 0.5171  | \( \_ \) | \( \_ \) |
| 4th iteration | \( \_ \) | \( \_ \) | 545   | 1.0541  | \( \_ \) | \( \_ \) |
| 5th iteration | \( \_ \) | \( \_ \) | 610   | 0.1103  | \( \_ \) | \( \_ \) |
| 6th iteration | \( \_ \) | \( \_ \) | 656   | 0.0382  | \( \_ \) | \( \_ \) |
and D respectively.

![Output spectra of a 4-channel 5GSPS TIADC in DSO with 1GHz input signal.](image)

Fig. 6. Output spectra of a 4-channel 5GSPS TIADC in DSO with 1GHz input signal.

The output spectrum of TIADC with 1GHz sinusoidal before and after offset, gain and timing skew mismatch calibrations are depicted in the Fig.6 (a) and (b). The offset, gain and time mismatch spurs are typically suppressed no longer visible above the noise floor. The SFDR after the calibration can be enhanced from 33.27 dBc to 52.66 dBc which shows the validity of the proposed algorithm.

6 Conclusion

In this paper, a fast TIADC calibration method for 5GSPS digital storage oscilloscope is proposed to compensate for offset, gain and timing skew mismatches. Offset mismatch is calibrated using weighted average algorithm based on statistical theory while gain and time mismatches are compensated by STPNM. The experiment results show that the impact of mismatches can be reduced substantially and the calibration can be finished in a short time because the convergence is very fast.

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