A New MRAM-based Process In-Memory Accelerator for Efficient Neural Network Training with Floating Point Precision

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Abstract—The excellent performance of modern deep neural networks (DNNs) comes at an often prohibitive training cost, limiting the rapid development of DNN innovations and raising various environmental concerns. To reduce the dominant data movement cost of training, process in-memory (PIM) has emerged as a promising solution as it alleviates the need to access DNN weights. However, state-of-the-art PIM based digital PIM accelerators employ either analog/mixed signal computing which has limited precision or digital computing based on a memory technology that supports limited logic functions and thus requires complicated procedure to realize floating point computation. In this paper, we propose a spin orbit torque magnetic random access memory (SOT-MRAM) based digital PIM accelerator that supports floating point precision. Specifically, this new accelerator features an innovative (1) SOT-MRAM cell, (2) full addition design, and (3) floating point computation. Experiment results show that the proposed SOT-MRAM PIM based DNN training accelerator can achieve 3.3\times, 1.8\times, and 2.5\times improvement in terms of energy, latency, and area, respectively, compared with a state-of-the-art PIM based DNN training accelerator.

Keywords—Process in-memory accelerators, efficient neural network training, spin orbit torque MRAM

1. Introduction

The recent record-breaking predictive performance achieved by deep neural networks (DNNs) motivates a tremendously growing demand to bring DNN-powered intelligence into numerous applications. However, the excellent performance of modern DNNs comes at an often prohibitive training cost due to the vast volume of training data and model parameters required. For example, one forward pass of ResNet50 \cite{1} requires 4 GFLOPs (FLOPs: floating point operations per second) of computation and training requires $10^{18}$ FLOPs, which takes 14 days on one state-of-the-art NVIDIA M40 GPU \cite{2}. As a result, training a state-of-the-art DNN model often demands considerable energy, along with the associated financial and environmental costs.

To address the time and energy dominant data movements of DNNs, process in-memory (PIM) based accelerators have emerged as a promising solution. While various PIM based accelerators have been developed for efficient DNN inference \cite{3}, \cite{4}, \cite{5}, PIM based accelerators for efficient training is less explored. Furthermore, state-of-the-art PIM based DNN training accelerators use either analog/mixed signal computing, which has limited precision \cite{5}, or digital computing using a memory technology that supports limited logic functions and thus requires complicated procedures to realize floating point computation \cite{6}.

In this paper, we propose a spin orbit torque magnetic random access memory (SOT-MRAM) based PIM accelerator that supports floating point computations which is often desirable in DNN training and features improved energy, time and area efficiency over state-of-the-art PIM accelerators for DNN training. The contribution of this paper can be summarized as follows:

- We develop a 1T-1R SOT-MRAM memory cell which features an improved balance between computation flexibility and memory density, favoring more efficient PIM accelerators.
- We propose a new full addition (FA) design that requires fewer computing steps to finish addition operations compared with the state-of-the-art design in \cite{6}.
- We develop efficient designs (reduced latency and energy) of the dominant floating point addition and multiplication for digital PIM accelerators, where the required latency and energy cost are analytically formulated.
- We integrate the aforementioned 1T-1R SOT-MRAM memory cell, new FA design, and efficient floating point computation to demonstrate a new SOT-MRAM PIM based DNN training accelerator.

2. Related Works and Background

**SOT-MRAM based Logic Functions.** SOT-MRAM is a type of non-volatile memory that stores data via resistance state (high or low) of Magnetic Tunnel Junctions (MTJ). Compared with other memory technologies, SOT-MRAM has advantages of (1) high memory cell density, (2) potentially infinite endurance, and (3) requiring low memory writing current \cite{7}, making it an attractive candidate for PIM accelerators. There have been several works exploring SOT-MRAM based PIM accelerators for DNN inference. The works \cite{8}, \cite{9} propose SOT-MRAM based inference accelerators for binary neural networks. The architecture in \cite{10} utilizes analog peripheral circuits to achieve multi-bit computation. However, most of the previous SOT-MRAM based PIM accelerators either support only single bit computations or are too complex to be used for DNN training.

A recent work \cite{11} introduces an efficient way to realize a complete set of Boolean logic functions, i.e., AND, OR, and XOR (see Figure 1) based on a single MTJ device, paving the way for SOT-MRAM based digital PIM accelerators.

**SOT-MRAM Memory Cells.** Figure 2 (a) and (b) show two typical SOT-MRAM cell designs \cite{11}. The 2T-1R cell in Figure 2 (a) consists of two transistors and one MTJ device. During a read operation, a small negative voltage is

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applied on RBL and a read current between the read bit-line (RBL) and source-line (SL) is generated, enabling the data stored in the MTJ to be read out. During a write operation, a high voltage and a positive voltage \( V_b \) are applied to the selected word-line (WL) and RBL, respectively, generating a current between the SL and the write bit-line (WBL) to enable writing the target data into the MTJ. The voltage applied on RBL determines whether the corresponding device’s resistance state can be switched. As a result, data can be written into different devices in the same row simultaneously. Compared to this 2T-1R cell, our proposed cell (see Figure 1 (c)) maintains its row-parallel writing flexibility, while having less transistors and higher memory density and write speed.

The memory cell in Figure 2 (b) consists of only a single MTJ device. During a write operation, the transistor at the target row and column are selected while all other transistors are set to be off, and either a zero or \( V_b \) is applied for each column depending on the desired data value to be written into the MTJ. During a read operation, the transistors for all of the columns of the selected row are activated while other transistors are set to be off, enabling all data stored in the selected row to be read out in parallel. While this single MTJ device cell has reduced parasitics and improved memory density, the current direction of all the cells in one row has to be changed simultaneously, requiring one extra step (as compared to the 2T-1R cell) for a write operation and thus limiting the computational latency of this single MTJ device cell as write operations dominate in the read/write process.

Available Boolean Functions vs. Computational complexity. Digital PIM accelerators’ computational complexity is closely related to the Boolean functions that can be implemented in the adopted memory technology. Specifically, if the memory technology can realize a complete set of Boolean functions, computational procedures will be simpler [6], [11], [12]; whereas more complicated procedures are required if only a limited set of Boolean functions can be implemented. As a concrete example, as the resistive random-access memory (ReRAM) in [6] supports only logic function NOR operations, it requires 13 steps of cell switch using a total of 12 cells for implementing 1-bit full addition (FA), while the same operation in SOT-MRAM based design requires only 5 steps of cell switch using a total of 4 cells [11]. Note that the 1-bit FA in [11] is not suitable for DNN training, because their design overwrites the original operands which are still needed later during training.

Floating Point Computation. It is well recognized that training with floating point precision favors high classification accuracy. Addition: among the standard procedures of performing floating point additions, it is naturally feasible to process all steps of different additions in parallel except for the step of aligning the two operands’ exponents. This is because different additions might require different shifted bits for their exponent alignment. To efficiently handling this step, FloatPIM [6] processes all the mantissas that require the same shifted amounts in parallel. Multiplication: similarly, the time/energy dominant step when performing floating point multiplication is the multiplication of the two operands’ mantissas. For efficiently handling this step, FloatPIM [6] processes input-weight multiplications in a row-wise parallel manner, which however involves writing a large amount of memory cells (e.g., 455 cells at one row for a 32-bit multiplication) in order to store the intermediate results. As writing into a memory cell can cost 100× higher energy than that of a NOR operation [6], new methods with much improved time/energy efficiency are needed.

3. The Proposed Digital PIM Accelerator

3.1. A New 1T-1R Memory Cell

Inspired by the advantages and disadvantages of the 2T-1R and single MTJ memory cells in [11] and in order to harvest the benefits of both, we propose a new 1T-1R memory cell as shown in Figure 2 (c) that consists of four control terminals. During both read and write operations, a high voltage (e.g., 0.7V in a 28nm technology) is applied to WL for turning on the selected transistor. During a read operation, RBL and SL are applied with a small negative voltage (e.g., -100mV) and connected to the ground, separately, resulting in a current flowing from SL to RBL (see the purple dash-line in Figure 2 (c)). Note that the negative voltage on RBL increases the current threshold to switch MTJs’ resistance state in order to avoid undesirable switches when reading data [7]. During a write operation, a positive voltage \( V_b \) (e.g., 600mV in [7]) or 0 is applied to RBL for controlling the threshold of current switching, while a positive or negative voltage is formed between WBL and SL.
to (1) generate the write current and (2) control the current direction. In this way, we can perform logic functions as shown in Figure 1 in the write process. For example, the computation of the OR operation is as follows: considering \( A = 1 \) (i.e., \( V_0 \) is applied to the top of SOT-MRAM), the write current flowing from SL to WBL (i.e., \( C = 1 \)) is larger than the threshold of current switching, leading to the MTJ’s switching to a high resistance state, i.e., \( B_{i+1}=1 \).

Compared with the existing SOT-MRAM based memory cells, the proposed memory cells feature increased memory density and improved read speed (e.g., over the 2T-1R cell in Figure 1), while maintaining the capability to control different cells within the same row which enables high computational flexibility and reduced computational latency.

3.2. A New FA for Digital PIM Accelerators

As discussed in Section 2, existing implementations of FA in digital PIM accelerators either require complicated procedures (and thus high energy/time cost) [6] or are not suitable for DNN training due to the overwriting of operands [11]. To this end, we propose a new FA design that addresses the limitation of prior works. Mathematically, 1-bit FA can be expressed as,

\[
S(R) = X \oplus Y \oplus Z \quad \quad (1)
\]

where \( X \) and \( Y \) are two operands, \( Z \) is the input carry, and \( Z' \) is the output carry. Figure 3 shows the required procedure: 1) Step 1 - \( X \), \( Y \), and \( Z \) are copied to corresponding MRAM caches of the same columns; 2) Step 2 - Both an XOR and AND operations between \( X \) and \( Y \) are performed in parallel to obtain \( X \oplus Y \) and \( XY \); 3) Step 3 - \( X \oplus Y \) is copied to the same row of and next to \( Z \), and an AND operation between \( Z \) and \( X \oplus Y \) is performed; and 4) Step 4 - an XOR operation between \( Z \) and \( X \oplus Y \) is performed in parallel with an OR operation between \( XY \) and \( Z(X \oplus Y) \). These four steps of read and write operations result in the sum \( S(R) \) and the new carry \( Z' \), while the value and location of \( X \) and \( Y \) are kept unchanged.

The aforementioned process can be performed using column-wise parallelism. Unlike [6], the operands and results in our design can be assigned to different columns. The MRAM cache can be reused in sequential 1-bit full additions for multi-bit additions. Specifically, our proposed FA requires 4 steps of read and write using a total of 4 memory cells, as compared to the required 13 equivalent steps using 12 memory cells in FloatPIM [6]. This improvement benefits from the: (1) available of complete Boolean \( \oplus \) and \( \land \) operations between \( Z \) and \( X \) in parallel to obtain \( X \); and (2) reuse of memory cells as cache and highly parallelable procedure.

3.3. Floating Point Computation

Addition. For handling the time/energy dominant exponent alignment, we adopt a similar “search” method as [6] (see Figure 2), as shown in Figure 3(a). Specifically, if the \( \text{input} \) bit matches with the stored bit, the read current from SL flows through the cell of a high resistance state and will be relatively low. Otherwise, the read current from SL flows through the cell of a low resistance state and will be relatively high. As a result, we can identify if the the \( \text{input} \) bit matches with stored \( \text{exp} \)’s (difference between two operands’ exponents) based on the current flowing from SL. Consider \( N_m \) bits for the mantissa and \( N_e \) bits for the exponents. Unlike FloatPIM which only supports bit-by-bit shifting and requires exponent-alignment latency and energy proportional to \( O(N_m^2) \) [6], the capability of shifting flexible bits thanks to the proposed 1T-1R cells enables an exponent-alignment latency and energy on the order of \( O(N_m) \). Specifically, the latency and energy of our proposed floating point addition are:

\[
T_{\text{add}} = (1 + 7N_e + 7N_m)T_{\text{read}} + (7N_e + 7N_m)T_{\text{write}} + 2(N_m + 2)T_{\text{search}}
\]

\[
E_{\text{add}} = (1 + 14N_e + 12N_m)E_{\text{read}} + (14N_e + 12N_m)E_{\text{write}} + 2(N_m + 2)E_{\text{search}}
\]

Multiplication. In a high-level, our proposed floating point multiplication (Figure 4 (b)) involves only shift-and-add operations for the dominant mantissa multiplications. Specifically, the multiplicand is multiplied with a single bit of multiplier, shifted, and added to previous intermediate results add multiplier’s bit times. The intermediate result of previous and current add are stored in two columns of cells, which will switch their roles in the next add operation. Other steps in multiplication are performed using column-wise AND, OR, and XOR operations in 1T-1R cells. The multiplication latency and energy costs are:

\[
T_{\text{mul}} = (2N_m^2 + 6.5N_m + 6N_e + 3)(T_{\text{read}} + T_{\text{write}})
\]

\[
E_{\text{mul}} = (4.5N_m^2 + 11.5N_m + 13.5N_e + 6.5)(E_{\text{read}} + E_{\text{write}})
\]
TABLE 1: Parameters of a SOT-MRAM cell [7]

| Parameter | Value     |
|-----------|-----------|
| \( R_{on} \) | 50 k\( \Omega \) |
| \( R_{off} \) | 100 k\( \Omega \) |
| \( V_{th} \) | 600 mV     |
| \( I_{write} \) | 65 \( \mu \)A |
| \( t_{switch} \) | 2.0 ns     |
| \( E_{switch} \) | 12.0 fJ    |

4. Experiment Results

4.1. Experimental Methodology and Setup

**Methodology:** To evaluate the effectiveness of the proposed ideas, we integrate the aforementioned 1T-1R SOT-MRAM memory cell, new FA, and efficient floating point computation to realize an SOT-MRAM based digital PIM accelerator for DNN training. For bench-marking the resulting accelerator in terms of DNN training performance, we first obtain (1) the energy consumption and latency per one bit memory write/read operation and per multiplication/addition calculation (MAC) of 32-bit floating point precision (commonly used for DNN training) and (2) the area of memory array and peripherals, separately; and then compare the training performance of our proposed accelerator with a state-of-the-art design, FloatPIM in [6] based on LeNet-type DNN model with 21,690 parameters of 32-bit floating point precision. Note that computations in both designs are performed with full precision, resulting in the same test accuracy after training.

**Setup:** To estimate the energy and latency cost per one bit memory write/read and the area in the proposed accelerator, we incorporate (1) basic SOT-MRAM cell parameters (see Table 1 from [7]) and (2) the current sense amplifier in [13] into the state-of-the-art simulator NVSim in [14]; while the energy and latency consumption per one bit memory write/read and the area of the FloatPIM accelerator is obtained from their paper [6]. For evaluating the accelerator performance, we adopt the same memory subarray size of 1024×1024 and hardware architecture as the FloatPIM baseline [6] for a fair comparison. The performance of both the proposed and FloatPIM accelerators are then obtained by designing a dedicated PIM accelerator simulator, the estimated performance of which is validated to be consistent with (<10% prediction accuracy) the reported performance in [6] under various conditions.

4.2. MAC with Floating Point Precision

Figure 5 evaluates the energy cost and latency of a MAC using the proposed 1T-1R cell, FA, and floating point addition and multiplication based on a 1024×1024 subarray. We can see that our MAC achieves a 3.3× lower energy cost and 1.8× lower latency compared with FloatPIM when finishing the same computation in the same size subarray, thanks to the facts that (1) the required fewer computing steps (i.e., read and write operations) to perform the same computation; and (2) compared with ReRAM in FloatPIM, the adopted SOT-MRAM requires a lower write current and thus a lower energy cost and latency for precharge. In addition, Figure 5 shows that cell switch latency dominates a MAC’s latency. Fortunately, ultra-fast switching SOT-MRAM developed recently [15] can potentially further reduce our MAC’s latency. Specifically, if we use the switch time in [15] to replace the current one, the MAC latency will be reduced by 56.7%.

4.3. Training with Floating Point Precision

Based on the simulation results of NVSim, we obtain the total energy cost, latency, and required area of training the LeNet model based on MNIST using the proposed digital PIM accelerator as benchmarked over FloatPIM in Figure 6. It is shown that our accelerator achieves a 2.5×, 1.8×, and 3.3× lower area, latency, and energy consumption, respectively, as compared to FloatPIM. This improved performance is resulted from the facts that (1) the fewer cells required to store intermediate results when performing the same computation as described in Section 3 and Figure 3; and (2) the higher design flexibility: unlike FloatPIM which requires the operands, intermediate results and the final result must be stored in the same row when performing addition or multiplication, memory cells in the proposed accelerator can be used to store intermediate results flexibly which maximizes cell reuse opportunities. Note that the improvement of the proposed accelerator’s energy efficiency and latency over FloatPIM is similar to that of a MAC, because computation dominates the total energy consumption and latency of small LeNet training.

5. Conclusion and future work

In this paper, we propose a SOT-MRAM based digital PIM accelerator for DNN training. Comparing to the pioneering work of ReRAM based digital PIM accelerator FloatPIM [6], our design achieves 3.3× higher energy efficiency, 1.8× lower latency, and 2.5× higher area efficiency. Future work will investigate the scalability of the proposed accelerator and evaluate the proposed design in larger DNN models and dataset.
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