ABSTRACT

We show that selecting a single data type (precision) for all values in Deep Neural Networks, even if that data type is different per layer, amounts to worst case design. Much shorter data types can be used if we target the common case by adjusting the precision at a much finer granularity. We propose Dynamic Precision Reduction (DPRed), where we group weights and activations and encode them using a precision specific to each group. The per group precisions are selected statically for the weights and dynamically by hardware for the activations. We exploit these precisions to reduce: 1) off-chip storage and off- and on-chip communication, and 2) execution time. DPRed compression reduces off-chip traffic to nearly 35% and 33% on average compared to no compression respectively for 16b and 8b models. This makes it possible to sustain higher performance for a given off-chip memory interface while also boosting energy efficiency. We also demonstrate designs where the time required to process each group of activations and/or weights scales proportionally to the precision they use for convolutional and fully-connected layers. This improves execution time and energy efficiency for both dense and sparse networks. We show the techniques work with 8-bit networks, where 1.82x and 2.81x speedups are achieved for two different hardware variants that take advantage of dynamic precision variability.

1. INTRODUCTION

Early successes in hardware acceleration for Deep Learning Neural Network (DNN) relied on exploiting its computation structure and the reuse in its access stream, e.g., [1][2][3]. Followup work identified and exploited various forms of informational inefficiency in DNNs such as ineffectual neurons [4][5], activations [4][6][5], ineffectual weights [7][5], an excess of precision [8][9][10][11][12][13][14][15], ineffectual activation bits [16], and hyper-parameter over-provisioning, e.g., [17][18]. Identifying additional forms of informational inefficiency is invaluable as it opens up additional opportunities for boosting execution time performance and energy efficiency which in turn support further innovation in DNN applications and design.

We highlight an overlooked informational inefficiency in the value stream of DNNs: the datatype/precision needed by most activations and weights is much shorter than that needed when considering the network as a whole or each of its layers individually. Additionally, the datatype needed by each activation varies considerably with the specific runtime input. In retrospect, the above observations are unsurprising: 1) by design, the expected per layer distribution of values, be it for weights or activations, is that most will be near zero and few will be of higher magnitude, and 2) the runtime values will obviously depend on the input.

Surprisingly, however, no hardware to date exploits the fine-grain precision variability of weights and activations fully. Some designs exploit profiled derived or quantized per layer precisions by: hardwiring the precision per layer [8], scaling voltage and frequency per layer [20], or supporting several data widths, e.g., [21][14] or the full spectrum of bit-widths [13]. These statically chosen per layer precisions must accommodate any possible input and for any activation and weight across a whole layer. We highlight that this design corresponds to a worst case precision analysis that exacerbates the importance of the exceedingly rare activation and weight values of large magnitude. We show that much higher potential for improvement exists if we tailor precision to target the common case instead. Specifically, the precision used at any given point of time needs to accommodate: 1) the activation values for the specific input at hand, and further 2) only the activation and weight values that are being processed concurrently. As a result the precision can vary with the input and could be adapted at a much finer granularity than the layer.

We demonstrate that, depending on how many activations and weights are processed together, the precision that they need can be lower than that identified through per layer pro-

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filing. We propose Dynamic Precision Reduction or DPRed (pronounced “Deep Red”) which adapts precision at a fine-granularity by grouping activations and weights and choosing a precision for each group separately. DPRed chooses precisions statically for the weights and dynamically for the activations. An accelerator that incorporates DPRed can use it to improve performance, reduce communication and storage needs, and ultimately improve energy efficiency over one that merely uses profile-derived per layer precisions. We make the following contributions:

1. We characterize the degree in which the data type needed by the weights and activations in DNNs varies when using groups much smaller than the layer and with the input.
2. We propose a DPRed hardware building block for compressing and decompressing groups of weights and activations off-chip thus reducing energy considerably and boosting the effective off-chip bandwidth. For weights the compression is done once as a pre-processing step. For activations, it is performed dynamically at the output of the previous layer. In both cases, the compressed data is decompressed on-the-fly when fetched from off-chip. This compression scheme reduces off-chip traffic to 38%. By comparison, using a fixed, profile precision reduces off-chip traffic to 50%. This building block is general and can be used with numerous accelerators.
3. We present DPRed Stripes (DStripes), an accelerator whose performance, communication and storage vary proportionally with the precision of activations at the granularity of a processing group. DStripes builds upon the Stripes accelerator [13] which exploits per-layer profile-derived precisions. A major advantage of DStripes is that the hardware changes it needs are modest yet the resulting performance, communication, storage, and energy efficiency improvements are anything but. For example, compared to a fixed-precision accelerator BASE (see Section 5.1) and for a configuration that performs 4K 16b × 16b multiplications per cycle, Stripes improves average performance and energy efficiency assuming everything fits on chip by 1.9 × and 1.32 × while DStripes improves them by 2.6 × and 1.84 × respectively.
4. We show that DStripes can also deliver benefits for pruned models (AlexNet, GoogleNet, ResNet50, and MobileNet) and that it delivers higher performance (on average 3.5 ×) than a similarly configured SCNN [3] (on average 1.9×). Moreover, we explain that DPRed is compatible with SCNN, and could be useful when processing larger inputs such as high-resolution images.
5. Like Stripes, DStripes accelerates computation only for convolutional layers which dominate execution time in many image related applications [2]. Since fully-connected layers are more prevalent in other applications [21] we present TARTAN (TRT), which enables DStripes to exploit precision variability also for these layers too. TRT is $P / \max(P_w, P_a)$ faster than Stripes and BASE where $P$ is the maximum precision supported in hardware, and $P_w$ and $P_a$ are the per group precisions for the weights and the activations respectively. TRT can be used independently of dynamic precision reduction. When combined with DStripes, TRT improves performance over BASE by 2.59× and 1.19× over the fixed-precision accelerator for a broader set of neural networks.

In 65nm DStripes requires less than 1% more area than Stripes. Adding TRT requires 26-51% more area depending on its configuration. Improvements with DStripes alone, or with DStripes combined with TRT far exceed those possible by scaling BASE to use the same area.

6. Since quantization has become more prevalent for certain classes of Deep Learning applications, we show that DPRed can deliver benefits even for 8b quantized networks. We show memory traffic reduction, performance and energy improvements for 8b configurations of DStripes and LOOM [22], a bit-serial design that exploits precisions for both weights and activations.

2. DYNAMIC PRECISION VARIABILITY

This section demonstrates that using per layer precisions for the activations is overly pessimistic. We demonstrate benefits for weights and activations in Section 6.

Figures 1a-1d show precision measurements for four convolutional layers — two from each of GoogleNet and SkimCaffe-ResNet50 [23] a weight pruned network. Similar trends were observed in other networks and layers. The measurements are over 5,000 randomly selected images from the IMAGENET dataset [24]. The graphs show the cumulative distribution of the precisions needed per group of activations for various group sizes ranging from 16 to 256, where each group uses the precision needed for its least favorable activation. Two vertical lines report the precisions when considering all activation values: 1) the profile-derived (“static”) over all sample images, and 2) the one that can be detected dynamically (“dynamic”) for one randomly selected sample image to illustrate that precisions also vary per input.

Figure 1e reports measurements for conv1, the first layer of GoogleNet. The profile-determined precision is 10 bits while for one specific image all values within the layer could be represented with just 7 bits, an improvement of 30% in precision length. The cumulative distribution of the precisions needed per group of 256 activations shows that further reduction in precision is possible. For example, about 80% of these groups require 6 bits only, and about 15% just 5 bits. Smaller group sizes further reduce the effective precision, however, the differences are modest. These results suggest that picking a precision for the whole layer exacerbates the importance of a few high-magnitude activations.

The first layer usually exhibits different value behavior than the rest since it processes the direct input to discover visual features whereas the inner layers tend to try to find correlations among features. Layer 5a-1x1 in Figure 1b shows more pronounced improvements in effective precision with the smaller group sizes. Figures 1c and 1d show that the behavior persists even in the sparse network. We include this measurement to demonstrate that dynamic precision variability is a phenomenon that is orthogonal to weight sparsity and thus of potential value to designs that target sparse neural networks.

Figure 1e compares (left Y-axis) the average effective precision with per layer profiling or with per value detection for weights and activations for additional models. These measurements are for 1000 randomly selected images from IMAGENET [24] for the image classification models [25, 26, 23, 27, 17, 28] and for 100 images from
CamVid [29] for SegNet [30] (segmentation), 100 and 10 inputs from Pascal VOC [31] respectively for YOLO V2 [32] (detection) and FCN8 [33] (segmentation), 10 images from CBSD68 [34] [35] [36], 10 inputs for LRCN [37] (denoising) and VDSR [38] (super-resolution), 500 inputs from WMT14 for Seq2Seq [39] (translation), 500 inputs from COCO [40] for LRCN [41] (captioning), and 500 inputs from Flickr8k [42] for Bi-Directional LSTM [43] (captioning). The measurements are across the whole network. It also reports the reduction in work (right Y-axis) for weights and activations when per-value precision is used. The results illustrate that selecting a single precision per layer grossly overestimates the precision needed for the common case.

Figure 1f reports the distribution of precisions needed for an 8b quantized GoogleNet. Three of the longer running layers are shown which are representative of the range of behaviors seen over all layers. For reduction and icp5_out1 more than 90% of the activations can be represented with 4 bits or less. For icp7_out0 more than 90% of the activations need 6 bits a 25% reduction over 8 bits. Section 6.6 shows that this behavior translates into significant memory and execution time benefits.

Generally, for all the networks studied the following were observed: 1) The activation precision needed varies, more so at the first layer, 2) for all layers the precisions needed at a finer than a layer granularity are shorter than those needed for the whole layer, and 3) only a small number of activation groups require the maximum precision needed for the layer as a whole. These results motivate incorporating dynamic precision reduction in hardware accelerators.

![Figure 1: Precision profiles for some conv. layers. (a)-(d) Average over multiple images. Multiple group sizes shown. "Dynamic" results for one sample image. (e) Average precisions and potential improvements for several networks. (f) Dynamic precision variability for three layers of an 8b quantized version of GoogleNet.](image)

Table 1: Average Per Layer Activation Precisions with DRed.

| Network | Effective Precision Per Layer | Reduction |
|---------|-------------------------------|-----------|
| AlexNet | 5.39-7.36-4.22-4.40-5.81      | 22.59%    |
| NIN     | 6.37-7.13-7.99-6.97-5.77      | 23.56%    |
| GoogleNet | 6.19-5.74-6.77-6.77-6.77-6.77 | 22.55%    |
| VGG_S   | 5.28-5.05-5.05-5.05-5.05      | 38.85%    |
| VGG_M   | 5.28-5.05-5.05-5.05-5.05      | 30.47%    |
| VGG_19  | 9.05-7.69-10.04-9.00-8.57     | 21.20%    |

Table 2: Average Per Layer Weight Precisions with DRed.

| Network | Effective Precision Per Layer | Reduction |
|---------|-------------------------------|-----------|
| AlexNet | 8.36-7.62-7.62-7.62-7.62      | 22.55%    |
| NIN     | 8.85-10.29-10.21-7.65-9.13    | 19.20%    |
| GoogleNet | 9.80-10.91-10.91-10.91-11.02  | 22.55%    |
| VGG_S   | 9.94-9.96-8.53-8.13-8.10      | 21.26%    |
| VGG_M   | 9.87-7.55-5.42-8.16-8.14      | 21.76%    |
| VGG_19  | 10.98-9.81-9.31-9.09-8.58     | 29.65%    |
3. REDUCING EFFECTIVE PRECISION

Tables 1 and 2 report the average precision DPRed achieves per layer which demonstrates that it can effectively reduce precisions. Due to space limitations we report results for a group size of 16 values along the channel dimension only. The effective precisions are fractional as they are averaged over all groups within the layer and weighted accordingly to their use at runtime.

4. REDUCING OFF-CHIP STORAGE AND COMMUNICATION

The bulk of energy in DNNs is expended by off- and on-chip memory accesses. Further, when on-chip storage is limited, off-chip bandwidth can easily be the bottleneck and more easily so for the fully-connected layers due to limited data reuse. Fortunately, the variable precision needs of activations and weights can be used to reduce the amount of storage and bandwidth needed on- and off-chip. Here we limit attention to the off-chip compression scheme.

Off-chip Memory Data Container: We encode weights and activations in groups of N values. We find that N = 16 offers a good balance between compression rate and metadata overhead. Figure 2a shows the in memory data container. For each group, we determine either statically (for weights) or dynamically (using the hardware unit of Figure 2c) at the output of the previous layer or at the input source for the first layer (for the activations) the precision in bits p_i, the group needs and store that as a prefix using 4 bits, followed by the 16 values each stored using p_i bits. In addition, to avoid storing zero values altogether, we use a 16b vector with one bit per original value to identify and store only the non-zero values off-chip. In total, this scheme requires 4 + 16 bits of metadata per group of 16 values. Uncompressed these 16 values occupy 256b so the metadata overhead is far less than the benefits obtained from compressing the values for typical cases. To simplify the hardware needed, the per-group memory container can be expanded so that in total it occupies a size that is a multiple of the memory interface (64b in our experiments).

Detecting the Per Group Precisions for Activations: Figure 2c shows how the hardware adjusts the precision at runtime for an example group of four 16b activations A_0 through A_3. It trims the unnecessary prefix bits by detecting the most significant bit position needed to represent all values within the group. The example activations can all be represented using just 12 bits as the highest bit position n_H a 1 appears is position 11. The hardware calculates 16 signals, one per bit position, each being the OR of the corresponding bit values across all four activations. The implementation uses OR trees to generate these signals. A “leading 1” detector identifies the most significant bit that has a 1, and reports its position in 4 bits. The same method can detect n_L – the trailing bit position needed to eliminate zero suffix bits. In practice, adjusting n_H dynamically resulted in a negligible reduction in effective precision of less than 0.4%; profiling effectively filters the less significant noisy bits which affect all activations regardless of magnitude [9]. Accordingly, we use the profile-derived n_L per layer. Since our networks used the ReLU all activation values are positive. The detector can be extended to handle negative values by converting them first to a sign-magnitude representation, and placing the sign at the rightmost (least significant) place. This is useful for weights and for networks that use activation functions that attenuate but not remove negative values [44, 45].

Memory Layout and Access Strategy: To minimize off-chip energy, we can size the on-chip memory buffers so that each weight and activation is accessed from off-chip once per layer [46]. In this case, the off-chip access stream is linear and contiguous and the different size of each container is no challenge. When the on-chip memory is not sufficiently large, we have to access some activations multiple times. The random access points can be easily identified at runtime when accessing them for the first time. Generally, for any given dataflow it will be possible to identify loop points either statically for the weights or dynamically for the activations and pre-record those in a small separate table.

Decompression/Compression: We use several decompression engines operating in parallel as per Figure 2c. As data is read from off-chip in chunks of 64b, the memory controller inspects the metadata header and distributes the data packets containing the values to the decompression engines each serving a different subset of the on-chip memory banks. The decompression engines expand the values to the format used in the on-chip memories and do so serially, one value at a time, avoiding the use of wide crossbars or shuffling networks. At the output of each layer, the output activations are assembled in groups in each bank and are encoded accordingly using the precision detected by the hardware of Figure 2c. The memory controller writes the resulting data containers as they become available.

Reducing On-Chip Communication: The precision reduction unit of Figure 2c can reduce communication when moving values on-chip as long as we use a bit-serial communication channel per value; values are trimmed just before the communication channel. A wide communication channel can be used to send multiple values concurrently.

Reducing On-Chip Storage: We can encode values in on-chip memory using the virtual column method of Judd et al., [47]. Values within the same precision group are spread over multiple virtual columns, one value per column. A separate virtual column is needed to specify the precision for each group. Evaluating this option is left for future work.

5. REDUCING EXECUTION TIME

The fine-grain precision requirement variability of the activations and weights can be used to also boost performance and energy efficiency. Specifically, this section presents DPRED Stripes or DStripes, an accelerator whose performance in convolutional layers scales proportionally with the inverse of the precision used for activations. DStripes is unique in that it adjusts the precision on-the-fly to meet the needs of only those activations that are currently being processed. Fortunately, DStripes can be implemented as a modest extension over the previously proposed Stripes [13]. Simplicity and low cost are major advantages for any new hardware proposal. We first review Stripes and an equivalent fixed-precision accelerator, and then explain the changes needed to enable dynamic precision reduction.
5.1 STRIPES and Bit-Parallel Accelerator

For clarity this discussion assumes the previously described configuration of a Stripes chip with 16 tiles, each processing 16 filters and 16 weights per filter and where the maximum precision is 16b. Each tile contains a grid of 16 Serial Inner-Product units (SIPs). Each SIP performs 16 1b × 16b multiplications followed by a reduction. The SIPs along the same column share the same group of 16 single-bit activations, while the SIPs along the same row share the same 16b weights, as each SIP produces an output activation corresponding to a different window. Each tile accepts 256 input activations and 256 × 16 = 4K weight bits per cycle, maintaining the same number of external wire connections as BASE. Before processing a layer Stripes expects software to specify the required precision, that is the positions of the most significant and of the least significant bits (MSB and LSB respectively), \( n_H \) and \( n_L \). Stripes uses this precision for all activations within the layer. Since Stripes processes 256 activations bit-serially over \( P_a \) cycles, it can ideally improve performance by 16/\( P_a \) over BASE. Data Reuse: Stripes further boosts data reuse in space and time: 1) each weight is reused across the 16 SIPs per row, and 2) weights are reused over the multiple cycles it takes to calculate their product with the corresponding activation bit-serially.

5.2 DPRed Stripes Architecture

The modest changes needed over Stripes to implement dynamic precision reduction are: 1) introducing a mechanism for detecting the precision needed per activation group, 2) adding a method of communicating the precision to the tiles, and 3) modifying the SIPs to appropriately handle starting the calculation per group at any \( n_H \) bit position. Precision Detection: Figure 3c shows the DStripes or-

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Figure 2: Using per group precisions to reduce off-chip memory bandwidth and storage.

Figure 3: (a) BASE Tile (b) STRIPES Tile (c) STRIPES: A Row of SIPs (d) DStripes
organization. A dispatcher reads a group of 256 activations from AM, however before communicating their values bit-serially, it first inspects them detecting the precision needed. It then communicates this precision as a 4-bit offset and as a single end of group signal. The precision is detected using the precision detection unit of Figure 5C.

To process an activation group, the dispatcher sends $H_n$ as the starting offset. The tiles decrement this offset every cycle. The dispatcher signals, using an end of group wire, the last cycle of processing for this group when the current offset becomes equal to $n_H$.

Granularity: The DStripes configurations we study detect precision for all 256 concurrently processed activations. Other arrangements are possible. For example, precision can be detected per group of 16 activations corresponding to SIPs along the same column.

Modified Serial Inner-Product Unit: The only modification needed to the SIP is the introduction of a shifter at the output of the adder tree. This shifter adjusts the adder tree output so that it can be accumulated with the running sum aligning it at the appropriate bit position. This is necessary since starting position varies per activation group.

### 5.3 Fully-Connected Layers

While Stripes and DStripes exploit precision variability for convolutional layers they do not do so for fully-connected layers. As a result, performance for fully-connected layers with Stripes and DStripes remains practically the same as that of BASE, but energy-efficiency suffers. This section motivates further extending Stripes and DStripes to exploit precision variability to boost performance and energy efficiency for fully-connected layers. We motivate this change by showing that: 1) indeed energy efficiency suffers in fully-connected layers (Section 5.3), and 2) precisions vary for weights in fully-connected layers (Section 5.3). The aforementioned results motivate the Tartan (TRT) extension that improves performance and energy efficiency for fully-connected layers and which complements Stripes and DStripes. For clarity this section presents TRT as an extension over Stripes.

While Stripes’s performance in fully-connected layers is virtually identical to BASE, its energy efficiency is on average 0.73× with very little variation across networks. While in image classification workloads fully-connected layers represent less than 10% of the overall execution time, in other applications this is not the case. Accordingly, it is desirable to improve energy efficiency for these layers as well.

The per layer precision profiles presented here were found via the methodology of Judd et al. [9]. For the image classification convolutional neural networks, Caffe [23] was used to measure how reducing the precision of each fully-connected layer affects the network’s overall top-1 prediction accuracy over 5000 images. The networks are taken from the Caffe Model Zoo [43] and are used as-is without retraining. For fully-connected layers precision exploration was limited to cases where both $P_w$ and $P_a$ are equal (the weight and activation precision ranges differ). For convolutional layers only the activation precision is adjusted since none of the designs we consider can further boost performance when reducing the weight precisions. While reducing the weight precision for convolutional layers can reduce their memory footprint [47], we do not explore this option in this evaluation. For NeuralTalk, we measure BLEU scores when compared with the ground truth. For Denoise, we measure PSNR, and define >99% accuracy as a drop of no more than 0.04dB.

Table 3 reports the resulting per layer precisions. The ideal speedup columns report the performance improvement that would be possible if execution time could be reduced proportionally with precision compared to a 16-bit bit-parallel baseline. For the fully-connected layers, the precisions required range from 8 to 10 bits and the potential for performance improvement is 1.64× on average. Given that the precision variability for fully-connected layers is relatively low (ranges from 8 to 11 bits) one may be tempted to conclude that an 11-bit BASE variant may be an appropriate compromise. However, given that the precision variability is much larger for the convolutional layers (range is 5 to 13 bits) the performance with a fixed precision datapath would be far below the ideal. Section 6 shows that the incremental cost of TRT over Stripes is well justified given the benefits.

#### 5.3.1 TARTAN

Unfortunately, since there is no weight reuse in fully-connected DStripes cannot reuse the same weight over multiple windows. In DStripes performance in fully-connected layers is limited by the number of cycles needed to load a different set of weights per SIP column [13]. TRT overcomes this limitation and boosts performance even for fully-connected layers by exploiting weight and activation precisions. We use Figure 4A to explain the concept behind TRT’s operation. The figure shows a row of SIPs (similar to Figure 3A) and focuses on the first weight input only. Whereas in Stripes the 16b weight input to the AND gates was coming directly from the WM connection here it is connected to a 16b Weight Register (WR). A multiplexer selects from where the WR can load its contents. The first option is to do so directly from the WM wires as in Stripes. This maintains the functionality needed for convolutions. An extra pipeline stage is needed to accommodate loading first to WR (stage 1) and then “multiplying” with the activation (stage 2). The

| Table 3: Per layer precision profiles needed to maintain the same accuracy as in the baseline. Ideal speedup with bit-serial processing of activations over a 16-bit bit-parallel baseline without dynamic adaptation. |
|-----------------------------------------------|-----------------------------------------------|
| Convolutional Layers                         |  100% Accuracy | Speedup |
| Network | Activation Precision in Bits | Ideal |  |
| AlexNet | 9-8-5-5-7 | 2.38 |  |
| VGG_S   | 7-8-9-7-9 | 2.04 |  |
| VGG_M   | 7-7-7-8-7 | 2.33 |  |
| VGG_I9  | 12-12-12-11-11-13-13-13-13-13-13-13-13-13-13-13-13-13-13-13 | 2.35 |  |
| NeuralTalk | 11 (all iterations) | 1.45 |  |
| Denoise | 12 (all layers) | 1.33 |  |
| Fully Connected Layers                        |  100% Accuracy | Speedup |
| Network | Act. & Weight Precision in Bits | Ideal |  |
| AlexNet | 10-9-9 | 1.66 |  |
| VGG_S   | 10-9-9 | 1.64 |  |
| VGG_M   | 10-9-9 | 1.64 |  |
| VGG_I9  | 10-9-9 | 1.63 |  |
| NeuralTalk | 11 (all iterations) | 1.45 |  |
| Denoise | 12 (all layers) | 1.33 |  |
second option is to load WR from the 16b Serial Weight Register (SWR). The SWR has a single input wire connection to the Weight Memory which is different per SIP. The first SIP in the row connects to wire 0 while the last to wire 15. SWR is a serial-load register and it can load a new weight value of \( p \) bits bit-serially over \( p \) cycles. Given that each SWR connects to a different Weight Memory wire, they can all concurrently load a different \( p \) bit weight value over the same \( p \) cycles. Each SIP can then copy its SWR held weight into its WR and proceed with processing the corresponding activations bit serially. Concurrently with processing the activations, the SWR can proceed to load the next set of weights. Accordingly, loading weights into the SWRs and processing the ones in the WRs form a two “stage” pipeline. The first “stage” of this pipeline requires \( P_w \) cycles to load a new set of weights since the weights are loaded bit-serially. The second “stage” of the pipeline requires \( P_o \) to process the current set of weights and activations since it multiplies activations bit-serially. As a result, it is the maximum precision of the weights or the activations that will dictate the number of cycles needed to process each group of activations.

Since there are 16 weights per SIP, the SWR and WR are implemented each as a vector of 16 16-bit subregisters. The remainder of this section explains how \( TRT \) processes convolutional and fully-connected layers. For clarity, in what follows the term \textit{brick} refers to a set of 16 elements of a 3D activation or weight array input which are contiguous along the \textit{channel} dimension, e.g., \( a(x,y,i) \ldots a(x,y,i+15) \). Bricks will be denoted by their origin element with a \( B \) subscript, e.g., \( a_B(x,y,i) \). The size of a brick is a design parameter.

**Convolutional Layers:** Processing is identical to \textit{Stripes} and starts by reading in parallel 256 weights from the Weight Memory as in \textit{Stripes}, and loading the 16 per SIP row weights in parallel to all SWRs in the row.

**Fully-Connected Layers:** Processing starts by loading bit-serially and in parallel over \( P_o \) cycles 4K weights into the 256 SWRs, 16 per SIP. Each SWR per row gets a different set of 16 weights as each sub-register is connected to one out of the 256 wires of the Weight Memory output bus for the SIP row (as in BASE there are 256 \( \times 16 = 4K \) wires). Once the weights have been loaded, each SIP copies its SWR to its SW and multiplication with the input activations can then proceed bit-serially over \( P_w \) cycles. Assuming that there are enough output activations so that a different output activation can be assigned to each SIP, the same input activation brick can be broadcast to all SIP columns. That is, each \( TRT \) tile processes one activation brick \( a_B(i) \) bit-serially to produce 16 output activation bricks \( o_B(i) \) through \( o_B(i \times 16) \), one per SIP column. Loading the next set of weights can be done in parallel with processing the current set, thus execution time is constrained by \( P_{max} = \max(P_w,P_o) \). Thus, a \( TRT \) tile produces 256 partial output activations every \( P_{max} \) cycles, a speedup of \( 16/P_{max} \) over BASE since a BASE tile always needs 16 cycles to do the same.

**Cascade Mode:** \( TRT \) is underutilized in fully-connected layer with less than 4K output activations. Some networks have layers with as little as 2K outputs. To avoid underutilization, the SIPs along each row are cascaded into a daisy-chain, where the output of one can feed into an input of the next via a multiplexer. This way, the computation of an output can be sliced over the SIPs along the same row: Each SIP processes only a portion of the input activations resulting into several partial output activations along the SIPs on the same row. Over the next \( np \) cycles, where \( np \) the number of slices used, the \( np \) partial outputs are added. The user can chose any number of slices up to 16, so that \( TRT \) can be fully utilized even when there are just 256 outputs.

**Other Layers:** \( TRT \) like \textit{Stripes} can process the additional layers needed by the studied networks. The tile includes hardware support for max pooling similar to \textit{Stripes}. An activation function unit is present at the output in order to apply nonlinear activations before writing back to AM.

**SIP and Other Components:** Figure 4 shows \( TRT \)’s SIP which multiplies 16 activation bits, one bit per activation, by 16 weights to produce an output activation. Two registers, a Serial Weight Register (SWR) and a Weight Register (WR), each contain 16 16-bit sub-registers. Each SWR sub-register is a shift register with a single bit connection to one of the weight bus wires that is used to read weights bit-serially for FCLs. Each WR sub-register can be parallel loaded from either the weight bus or the corresponding SWR sub-register to process convolutional or fully-connected layers respectively. The SIP includes 256 2-input AND gates that multiply the weights in the WR with the incoming activation bits, and a \( 16 \times 16 \) adder tree that sums the partial products. A final adder plus a shifter accumulate the adder tree results into the output register. A multiplexer at the first input of the adder tree implements the cascade mode supporting slicing the output activation computation along the SIPs of a single row. Each SIP also includes a comparator (max) to support max pooling layers. A shifter between the output of the adder tree and the input to the accumulator can be added to support DPRed.

As in \textit{Stripes} there is a central AM and 16 tiles. A \textit{Dispatcher} unit is tasked with reading input activations from AM always performing eDRAM-friendly wide accesses. It transposes each activation and communicates each a bit a time over the global interconnect. For convolutional layers the dispatcher has to maintain a pool of multiple activation bricks, each from different window, which may require fetching multiple rows from AM. However, since a new set
of windows is only needed every \( P_o \) cycles, the dispatcher can keep up for the layers studied. For fully-connected layers one activation brick is sufficient. A Reducer per tile is tasked with collecting the output activations and writing them to AM. Since output activations take multiple cycles to produce, there is sufficient bandwidth to sustain all 16 tiles.

**Coarser Bit Granularity Processing:** To improve TRT’s area and power efficiency, the number of activation bits processed at once can be adjusted at design time. Such designs need fewer SIPs and shorter wires. However, they forgo some of the performance potential as they force the activation precisions to be a multiple of the number of bits that they process per cycle.

### 5.4 DPRed Loom

Dynamic precision variability can also benefit Loom [22], an architecture that exploits precision variability both in activations and weights which is faster and more energy efficient than Stripes for smaller configurations. The original design, which uses per-layer precisions, can be extended utilizing the mechanism described in Section 5.2 to take advantage of per group precisions for both weights and activations.

### 6. EVALUATION

We first assume that all data fits on chip using the memory configuration of DaDianNao [2]. Having identified a reasonable compute configuration we then study restricted on-chip memory hierarchies and the effect of off-chip memory demonstrating that DPRed greatly helps with alleviating stalls due to off-chip accesses.

All accelerators were modeled using the same methodology for consistency. A custom cycle-accurate simulator models execution time. Computation was scheduled as described in Stripes to maximize energy efficiency for BASE [13]. To estimate power and area, all designs were synthesized with the Synopsys Design Compiler [49] for a TSMC 65nm library and laid out with Cadence Encounter. Circuit activity was captured with ModelSim and fed into Encounter for power estimation. All designs operate at 980 MHz. The SRAM activation buffers were modeled using CACTI [50]. The AM and WM eDRAM area and energy were modeled with Destiny [51]. Three design corner libraries were considered prior to layout. The typical case library was chosen for layout since bit-serial designs are affected less by the worst-case design corner. Accordingly, the relative benefits with DPRed over BASE are underestimated. DStripes and TRT improve energy efficiency and performance for all design corners.

Given that DStripes improves performance only for conv. layers, and that TRT performs identically to DStripes for conv layers while improving performance only for fully-connected layers, a different set of DNNs is used during the evaluation of the two techniques. For DStripes measurements were performed over a set of ImageNet Classification CNNs: AlexNet, GoogleNet, Nin, VGG_S, VGG_M, and VGG_19. For these networks conv. layers account for more than 90% of the execution time. For TRT the evaluation omits Nin and GoogleNet since the former has no fully-connected layers and their usage in the latter is not significant. Instead NeuralTalk [52] and Denoise [53] are included that are dominated by fully-connected layers. NeuralTalk uses long short-term memory to automatically generate image captions. Denoise is a 5-layer Multilayer Perceptron that implements image denoising aiming to reproduce the results of the state-of-the-art BM3D denoising algorithm [54].

#### 6.1 DStripes

**Performance:** Figure 5(a) shows the resulting speedup with DStripes alone and over the equivalently configured BASE and Stripes. Since DStripes improves performance only for conv. layers these measurements are restricted to conv. layers only. On average, dynamic precision reduction boosts performance over Stripes by 41% since DStripes proves 2.61× faster than BASE.

**Energy Efficiency:** As Table 4 shows DStripes greatly improves energy efficiency over BASE and Stripes. The dispatcher has to communicate less bits and the units have to perform fewer calculations. On average, compared to BASE, Stripes and DStripes are 1.84× and 1.38× more energy efficient respectively.

**Area:** In the interest of space, we omit the detailed area results here and present those for the combination of DStripes and TRT instead in the respective section. The overall area overhead of dynamic precision reduction is less than 1% over Stripes and as a result DStripes is 1.32× larger than BASE. Given that DStripes is 2.61× faster, the performance over area ratio is superlinear with DStripes. Utilizing 32% more area in BASE would at best increase performance proportionally. However, in practice the speedup will be a lot

![Figure 5: DStripes: Speedup over BASE in Convolutional Layers](image-url)
Table 4: Convolutional Layers: Energy Efficiency of DStripes vs. BASE and vs. Stripes (higher is better)

| Network  | vs. BASE | vs. Stripes |
|----------|----------|-------------|
| AlexNet  | 1.98     | 1.26        |
| NIN      | 1.68     | 1.27        |
| GoogleNet | 1.86    | 1.53        |
| VGG_M    | 2.22     | 1.40        |
| VGG_S    | 2.31     | 1.58        |
| VGG_19   | 1.20     | 1.24        |
| GEOMEAN  | 1.84     | 1.38        |

Table 5: Execution time and energy efficiency improvement with DStripes compared to BASE.

| Fully Connected Layers | Convolutional Layers |
|-----------------------|----------------------|
| Perf                  | Eff                  |
| AlexNet               | 1.61                 | 1.10                  | 2.81          | 1.28           |
| VGG_S                 | 1.61                 | 1.09                  | 3.26          | 1.49           |
| VGG_M                 | 1.61                 | 1.10                  | 3.15          | 1.44           |
| VGG_19                | 1.60                 | 1.09                  | 1.70          | 0.77           |
| Denoise               | 1.42                 | 1.01                  | -             | -              |
| geomean               | 1.52                 | 0.92                  | 2.65          | 1.21           |

6.2 Pruned Models

Pruning is sometimes possible and it converts several weights into zeros. Past work has exploited pruning to reduce work. Figure 5b compares the performance of DStripes and SCNN for a set of pruned models [23,27]. For both designs we assume infinite off-chip bandwidth giving an advantage to SCNN since DPRed reduces traffic more than zero compression. SCNN removes all products where the activation or the weight is zero. The reasons why DStripes outperforms SCNN are: 1) SCNN’s performance is limited by inter- and intra-tile fragmentation [5], while 2) DStripes targets all activations where the potential for work reduction is higher than the work reduction potential from targeting those values that are zero. However, Dynamic Precision Reduction is compatible with SCNN and we have experimented with replacing the bit-parallel multiply-accumulate units in SCNN with bit-serial units while increasing the number of tiles. Unfortunately, the benefits are limited since the higher tile count exacerbates inter-tile load imbalance. Addressing this imbalance is left for future work.

6.3 DStripes and TARTAN

Performance: We evaluate the combination of DStripes and TRT denoted as DStripes. Table 5 reports DStripes’s performance and energy efficiency relative to BASE for the precision profiles in Table 8 separately for fully-connected layers, convolutional layers, and the whole network. Denoiser has no convolutional layers. NeuralTalk uses a modified convolutional neural network (based on VGG_16 in this implementation) to recognize objects before the LSTM stage; we do not evaluate that phase as it is similar to the other image classifiers.

On fully-connected layers DStripes yields, on average, a speedup of 1.52×. For conv. layers DStripes improves performance by 2.65×. There are two main reasons DStripes does not reach the ideal speedup: dispatch overhead and under-utilization. During the initial Pc cycles the serial weight loading process prevents any useful products to be performed. This represents less than 2% for any given network, although it can be as high as 6% for the smallest layers. Underutilization can happen when the number of outputs is not a power of two or lower than 256.

Energy Efficiency As Table 5 reports, the average efficiency improvement with DStripes across all networks and layers is 1.19×. DStripes is more efficient than BASE for all layers. Overall, efficiency primarily comes from the reduction in effective computation due to reduced precisions. Furthermore, the amount of data that has to be transmitted from the WM and the traffic between the AM and the SIPs is decreased proportionally with the chosen precision.

Area: Table 6 reports the area breakdown of DStripes and BASE. Over the full chip, DStripes needs 1.51× the area compared to BASE while delivering on average a 2.59× speedup. Generally, performance would scale sublinearly with area for BASE due to underutilization.

Sensitivity to Precision Resolution: Table 7 reports performance for the DStripes variant of Section 5.3.3 that processes 2 bits per cycle in as half as many total SIPS. The previously quoted precisions are rounded up to the next multiple of two. This design always improves performance compared to BASE. Compared to the 1-bit DStripes performance is slightly lower, however this can be a good trade-off given the reduced cost and improved energy efficiency. Overall, there are two forces at work: There is performance potential lost due to rounding all precisions to an even number, and there is performance benefit by requiring less parallelism. The time needed to serially load the first bundle of weights is also reduced. The layout of DStripes’s 2-bit variant requires only 26.0% more area than BASE (Table 6) while improving energy efficiency in fully-connected layers by 1.24× on average (1.4× across all layer types).

6.4 Memory Hierarchy

We consider the effects of off-chip bandwidth and the effectiveness of DPRed for off-chip bandwidth amplification. We use 320KB of WM per tile which is sufficient so that DStripes can read each weight only once from off-chip and...
Figure 6: Offchip traffic reduction with compression schemes. Overhead for the compression metadata is reported as a percentage of the compressed traffic. The four rightmost models use per-layer precision aware 8-bit quantization.

Figure 7: Performance of DStripes with different memory technologies, off-chip compression schemes, and activation memory sizes for convolutional layers.

Figure 8: Performance of DStripes with different memory technologies and activation memory size for convolutional layers and fully connected layers.

Table 8: DStripes: Speedup over an 8-bit baseline in all layers with 8-bit quantization

| Name      | Rel. Perf. | Name      | Rel. Perf. |
|-----------|------------|-----------|------------|
| AlexNet   | 1.11       | AlexNet [26] | 1.62       |
| NiN       | 1.36       | GoogleNet | 1.54       |
| GoogleNet | 1.28       | BiLSTM    | 1.76       |
| VGG_M     | 1.15       | SegNet    | 2.50       |
| VGG_S     | 1.22       | geomean   | 1.82       |
| VGG_19    | 1.44       |           |            |
| ResNet50  | 1.39       |           |            |
| MobileNet | 1.47       |           |            |

Figure 9: LOOM: Comparison between static and dynamic precisions (with LPDDR4-4267)

per layer [46]. Figures [7] show the effect on the performance of DStripes for different on-chip AM sizes, compression schemes (x-axis), and off-chip memory technologies (stacked bars). We consider three compression schemes: 1) No Compression (NP), 2) precision-based using profile-derived per layer precisions (SP) [47], and 3) our per group precision-based (DP). Performance is normalized to the configuration where all activations fit on chip (INF) — the configurations used thus far. Figure [7] reports relative performance for the convolutional layers only, while Figure [8] reports relative performance for all layers.

Overall, the choice of external memory impacts performance significantly more than the choice of the on-chip AM. The results show that our compression scheme greatly boosts performance by reducing the impact of off-chip traffic. For the convolutional layers DStripes when used with our compression manages to maintain most its performance benefits even with 2 channels of DDR4-3200 memory. With HBM, which would be appropriate given the peak compute capability of this configuration, the performance is within 2% of the ideal. Off-chip memory is the bottleneck for fully-connected layers. However, using HBM or HBM2 preserves most of the overall benefits provided that our compression scheme is used. Finally, Figure [6] reports the relative off-chip traffic normalized to no compression (Base). Our compression scheme reduces traffic to 55% for GoogleNet, 60% for BiLSTM and to less than 40% for the remaining networks.

6.5 DPRed Loom

Figure [2] compares the performance of Loom when using dynamic vs. static per-layer precisions with a LPDDR4-4267 off-chip memory. We use the AM and WM memories suggested by Sharify et al. [22], processing 2048 weights.
Table 9: Area and power consumption of DStripesT normalized to BASE for 8-bit configuration

|                      | DStripesT (8-bit) | BASE (8-bit) |
|----------------------|-------------------|--------------|
| Normalized Total Area| 1.05 x            | 1.00 x       |
| Normalized Total Compute Area | 1.87 x | 1.00 x |
| Normalized Power     | 1.64 x            | 1.00 x       |

Table 10: LOOM: Speedup over an 8-bit baseline in all layers for 8-bit networks

| Name      | Rel. Perf. |
|-----------|------------|
| AlexNet [26] | 2.70       |
| Goog [26]  | 2.13       |
| BiLSTM     | 2.67       |
| SegNet     | 4.07       |
| GeoMean    | 2.81       |

and 256 activations concurrently bit-serially.

6.6 8-bit Quantization

Table 8 reports performance for 8b quantized models. We report results for two quantization approaches. The first two columns report results with the 8-bit quantized representation used in Tensorflow [11, 55]. This quantization uses 8 bits to specify arbitrary minimum and maximum limits per layer for the activations and the weights separately, and maps the 256 available 8-bit values linearly into the resulting interval. The second set of columns use precision aware quantization where quantization does not unnecessarily expand a range that can fit in less than 8b to the full 8b range. We perform an iso-area comparison only for the last set of models. That is, we scale the baseline’s compute resources to use at least as much area as that of DStripes; instead of 1.87x as per Table 9 we scale the area of the baseline compute units to 2x. We do not scale the memories since this does not provide a benefit in this evaluation, as all data fits on chip. In the time allotted we were able to quantize the four models shown which include a captioning LSTM and a segmentation CNN.

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7. RELATED WORK

Distributed Arithmetic (DA), which computes inner products bit-serially, has been used in the design of Digital Signal Processors [56], including designs with application-specific dynamic precision detection [57]. DA precomputes and stores in a table all combinations of coefficients. This is intractable for the weights of DNN as they are too many.

Pragmatic uses a similar organization to Stripes and thus DStripes but its performance on convolutional layers depends only on the non-zero activation bits [16]. DStripes can improve energy efficiency for Pragmatic by reducing the number of bits sent from off-chip memory and from AM to the tile. DStripes represents a different area vs. efficiency vs. performance trade-off than Pragmatic. The Efficient In-
et al., present an outlier aware accelerator design where a set of limited high-precision execution units are used to process those neurons that require them whereas the bulk of computations happen in lower precision units [15]. For this purpose, the weights are quantized and partitioned statically. DPRed works with any network whether quantized or not and adapts the precisions of both weights and activations. For this reason it could be beneficial even for the above reference accelerator.

8. CONCLUSION

We believe that dynamic precision reduction opens up several directions for future work including how to combine with other accelerator engines, how it can boost the efficiency of algorithms for pruning or for precision reduction or quantization of weights and of activations, and whether it can be exploited to accelerate training as well. The accelerators we proposed do not require any changes to the input network to deliver benefits. However, they do reward any advances in precision reduction including linear quantization and thus if deployed will provide an incentive for further innovation towards networks of extremely low precision.

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