Model Synthesis for Communication Traces of System-on-Chip Designs

Hao Zheng, Md Rubel Ahmed
U of South Florida, Tampa, FL
{haozheng,mdrubelahmed}@usf.edu

Parijat Mukherjee
Intel, Hillsboro, OR
parijat.mukherjee@intel.com

Mahesh C. Ketkar
Intel, Folsom, CA
mahesh.c.ketkar@intel.com

Jin Yang
Intel, Hillsboro, OR
jin.yang@intel.com

Abstract—Concise and abstract models of system-level behaviors are invaluable in design analysis, testing, and validation. In this paper, we consider the problem of inferring models from communication traces of system-on-chip (SoC) designs. The traces capture communications among different blocks of a SoC design in terms of messages exchanged. The extracted models characterize the system-level communication protocols governing how blocks exchange messages, and coordinate with each other to realize various system functions. In this paper, the above problem is formulated as a constraint satisfaction problem, which is then fed to a SMT solver. The solutions returned by the SMT solver are used to extract the models that accept the input traces. In the experiments, we demonstrate the proposed approach with traces collected from a transaction-level simulation model of a multicoresoC design and traces of a more detailed multicoresoC design developed in GEM5 environment.

Index Terms—specification mining, learning, system-on-chip

I. INTRODUCTION

Modern system-on-chip (SoC) designs integrate a large number of functional blocks procured from various sources. At runtime, these blocks communicate and coordinate with each other through intricate system-level protocols to implement various sophisticated functions. SoC executions are highly concurrent where a large number of system transactions following those protocols are often executed simultaneously. Experiences have shown that communications among different blocks are the major source of various design and runtime errors. In order to thoroughly verify the communication behavior of an SoC, well-defined and comprehensive protocol specifications are essential. However, in practice, such specifications are usually not available, ambiguous, incomplete, or even contain errors. They often become outdated and disconnected from the design implementation as the design progresses.

Many methods and approaches, e.g., [1]–[4], have been proposed to mine patterns or models from traces of various forms. They are inadequate to handle the SoC communication traces considered in this work. The existing methods extract patterns of events from a trace if those events show strong temporal dependencies. However, in communication traces as a result from concurrent executions of a large number of system transactions, events showing strong temporal dependencies may not be related according to the true dependencies in the ground truth specifications. In the next section, an example is used to elaborate this challenge. As a result, existing mining methods often generate a large number of patterns, many of which are not meaningful. Moreover, they may not be able to extract a model that includes all real valid patterns. Therefore, the extracted models can be large, not understandable, or even misleading.

To address the above challenge, this paper describes a method that can automatically infer reduced and concise models from communication traces of SoC designs obtained from simulation or emulation. These traces considered in this paper are sequences of messages exchanged among design blocks. Given an input trace, the model extraction is formulated as constraint satisfaction problem, which is then fed to an SMT solver. A model is constructed from solutions returned by the SMT solver. The extracted model characterizes the underlying system-level communication protocols that design blocks follow to generate the input trace.

The main contribution of this work is, to our best knowledge, the first method that can automatically and efficiently synthesize concise abstract models from system communication traces for SoC designs. What distinguishes this work from previous ones is that it targets traces generated from concurrently executing multiple system transactions, and aims to infer system-level protocols that govern the executions of those system transactions. As a result, it avoids finding patterns in the extracted models without true dependencies by incorporating readily available design information, thus leading to reduced and more understandable models. It is efficiently, and scalable to very long traces.

Related Work. Specification mining aims to extract patterns from various artifacts. A model based approach Synoptic [5] mines invariants from logs of sequential execution traces where concurrency is recorded in partial order. It then generates an FSM that satisfies the mined invariants. Perracotta [1] is another software execution log analysis tool that mines temporal API rules. It describes a chaining technique that can be used to find long sequential patterns. The work BaySpec [3] extracts LTL formulas from Bayesian networks trained with software traces. It requires traces to be clearly partitioned with respect to different functions. For mining hardware traces, the approaches presented in [6]–[10] mine assertions from either gate-level representations [6], or RTL models [7]–[11]. The work in [2] describes an assertion mining approach using episode mining from the simulation traces of transaction level
models. Those approaches often lack support for finding longer patterns, thus not able to find complex communication patterns involving multiple components.

Our work shares some similarities to the methods on software model synthesis. The aim of model synthesis is to identify a model from system execution traces such that the resulting model can accept the input traces. In [12], the deterministic finite automata inference based on the original evidence-driven state merging method [13] is extended and formulated as a graph coloring problem, which is then solved by a Boolean satisfiability solver. Recently, Trace2Model is introduced in [14] that learns non-deterministic finite automata (NFA) models from software execution traces using C bounded model checking technique. Similar work can also be found in [14]. The above approaches do not consider the concurrent nature of communication traces of SoC designs, and they rely on temporal dependencies discovered from traces to identify models. However, temporal dependencies are often not same as the true dependencies that our work aims to find.

II. BACKGROUND

System-level protocols are often represented as message flows in SoC architecture documents. Fig. 1 shows a very simple yet representative example of message flows for a multicore SoC design. This example specifies memory read operations for two CPUs via a shared cache. Message flows specify temporal relations for a set of messages. As shown in Fig. 1(a), each message is a tuple (src : dest : cmd) where the src denotes the originating component of the message while dest denotes the receiving component of the message. Field cmd denotes the operation to be performed at dest. For example, message (CPU0 : Cache : rd_req) is the read request from CPU_0 to Cache. Each message flow is associated with an unique start message to indicate initiation of an instance of such flow, and with one or multiple different end messages to indicate its completion. A flow may contain multiple branches describing different paths a system can execute such a flow. For example, the flow in Figure 1(b) has two branches specifying read operations in cases of cache hit or miss.

During the execution of an SoC design, instances of flows are executed concurrently. When a flow instance is executed along one of its paths, messages on that path are exchanged with runtime information, e.g. memory addresses. Typically, multiple instances of different flows that are executed concurrently are captured in the traces.

Definition 2.1: An SoC execution trace ρ is ρ = (ε₀, ε₁, . . . , εₙ) where εᵢ = {mᵢ₀, . . . , mᵢₖ} is a set of messages observed at time i, and mᵢⱼ is an message instance of some flow instance active at time i, for every mᵢⱼ ∈ εᵢ.

To simplify the presentation, hereafter flows (messages) and flow instances (message instances) are used interchangeably if their meanings are clear in the context.

An example trace from executing the flows in Figure 1 is

\[
\{(1, 3), 1, 2, 5, 1, 5, 6, 2, 4, 6, 2\}
\]

where the numbers in the trace are the message indices as shown in the Fig. 1(a). The idea of message sets helps to represent the outcomes of these concurrently executing flows. Note that the ordering of the messages in the same set of a trace is unknown. Given two messages mᵢ and mⱼ and a trace ρ, we define mᵢ <ᵢ ρ mⱼ, denoting that mᵢ occurs before mⱼ in ρ, if mᵢ ∈ εᵢ, mⱼ ∈ εⱼ, and i < j. For simplification, a set of a single message {m} is written as m. Moreover, a sequence of one message (m) is also written as m.

Given a trace as shown above, we aim to infer a model that characterizes the underlying message sequence protocols as shown in Fig. 1 to explain the generation of the trace. We use finite state automata to represent the extracted model.

Definition 2.2: A finite state automaton (FSA) is a tuple \( \mathcal{M} = (Q, q₀, \Sigma, F, \delta) \) where \( Q \) is a finite set of states, \( q₀ \in Q \) the initial state, \( \Sigma \) a finite set of symbols, \( F \subseteq Q \) the set of accepting states, and \( \delta : Q \times \Sigma \rightarrow Q \) the transition relation.

In our method, each symbol in \( \Sigma \) denotes an unique message found in the input trace, and \( F = \{q₀\} \). Given a FSA \( \mathcal{M} \), a flow execution scenario is defined as a set \( \mathcal{X} = \{(Mᵢ, qᵢ) \mid 1 \leq i \leq n\} \) where \( Mᵢ \) is the ith instance of \( \mathcal{M} \), and \( qᵢ \) is a current state of \( Mᵢ \). Suppose \( ρ \) is an input trace and \( \mathcal{M} \) is the model inferred from \( ρ \). Initially, all \( Mᵢ \) in \( \mathcal{X} \) are in \( q₀ \). Then, for every message \( m \) in \( ρ \) from the beginning, we can find an \( (Mᵢ, qᵢ) \in \mathcal{X} \) such that \( \Delta(qᵢ, m, qᵢ₊₁) \) holds for some state \( qᵢ₊₁ \in Q \). After accepting \( m \), we get a new execution scenario \( \mathcal{X}' \) with \( (Mᵢ, qᵢ) \) being replaced with \( (Mᵢ, qᵢ₊₁) \). At the end of the trace \( ρ \), the corresponding execution scenario is the same as the initial execution scenario. Multiple instances of the model \( \mathcal{M} \) in an execution scenario reflect the fact that the trace is the result from concurrent execution of multiple message flows when a SoC design runs.

The challenge of inferring models from communication traces as shown above is that such traces are results from executing many message flows concurrently, thus correlating messages correctly is very difficult. Note that (1, 5, 6, 2) and (3, 5, 6, 4) are two message flows specified in Fig. 1. Consider the trace (1, 3, 5, 6, 1, 3, 5, 6, 2, 4, 2, 4) resulting from executing the above message flows two times each in an interleaved manner. In this trace, messages 1 and 3 show strong temporal dependency, but they are actually unrelated. Existing methods fail to extract true message flows because they mostly rely on temporal dependencies to find interesting patterns. For
Algorithm 1: AutoModel

1: **Input**: A trace $\rho$
2: **Output**: a FSA $M$
3: Extract unique messages in $\rho$ into $M$;
4: Build the causality graph $G$ from $M$;
5: Generate $P$ the set of consistency constraints from $G$;
6: Get a solution $\text{sol}$ of $P$ using a SMT solver;
7: Derive a FSA $M$ from $\text{sol}$;

example, using Perracotta in [1] we can extract a sequential pattern $(1, 3, 5, 6)$, which is highly confusing. Fig. 2 shows the model produced using the method in [4]. Even though this model fits the trace perfectly, it contains message sequences that do not make sense with respect to the ground truth flows.

Note that the message flows in Fig. 1 specifies causality relations among messages in addition to their temporal relations. For example, when message (CPU_0 : Cache : rd_req) occurs, it causes either (Cache : CPU_0 : rd_resp) or (Cache : Mem : rd_req) to happen. Therefore, we define structural causality below based on the observation: any message in an SoC execution trace is an output of a component in reaction to a previous input message.

**Definition 2.3**: Message $m_j$ is *causal* to $m_i$, denoted as $\text{causal}(m_i, m_j)$, if $m_i.\text{src} = m_j.\text{dest}$.

The above causality is referred to as structural against the functional causality in the flow specifications. In our method, message sequences represented by the FSA model extracted from a trace are required to satisfy the structural causality relation for every two consecutive messages. With this requirement, sequence (1, 3, 2, 4) would not be extracted as a model of the above trace. Applying the structural causality relation during the model extraction process is straightforward as it only depends on basic structural information of a SoC design, which can be readily captured in messages.

III. MODEL SYNTHESIS

Algorithm 1 shows the outline of our method. It takes as an input a trace of messages $\rho$, and produces a FSA model $M$ such that executing $M$ in a certain way can lead to $\rho$ to be re-produced. This method involves three major steps, collecting messages and building a causality graph (lines 3-4), generating constraint problem $P$ from the causality graph (line 5), and extracting a model from $P$ (lines 6-7). These steps are explained in the following sections.

A. Building Causality Graph

Given an input trace $\rho$, it is scanned to collect all unique messages. A message is unique if at least one of its three attributes is different from all other messages already collected. Recall that each message flow is initiated with a start message, and completed with an end message. During the message collection process, start and end messages are also identified. Start and end messages can be identified from a trace as follows. A message $m$ is a start message if $m.\text{src} \neq m'.\text{dest}$ for all $m' < m$ in $\rho$. (2) A message is an end message if $m.\text{dest} \neq m'.\text{src}$ for all $m < m'$ in $\rho$. (3)

Scanning the trace from the beginning, we can find all start messages by checking condition (2). Similarly, all end messages can be found by scanning the trace from the end and checking condition (3).

Let all the collected messages be $M$, start messages $\text{Start} \subset M$, and end messages $\text{End} \subset M$. Next, we construct a causality graph from those messages, which captures all possible structural causalities among every pair of messages. A causality graph $G$ is a directed graph. It has a set of root nodes, each of which is labeled with a start message in $\text{Start}$, and a set of terminal nodes, each of which is labeled with a end message in $\text{End}$. The other nodes are labeled with messages that are not start or end messages.

Once the causality graph is constructed, the trace is scanned again to find the supports for nodes and edges. The support of a node is the number of instances of the labeled message in the trace. The edge support is the number of co-existences of messages at the head and tail nodes of that edge in the trace.

Consider the trace $\rho = (1, 3, 5, 6, 1, 3, 5, 6, 2, 4, 2, 4)$ as an example. The collected messages and the causality graph for this trace is shown in Figure 3. In the causality graph, numbers in blue are node supports, and numbers in red are edge supports. For example, we can find two instances of $(1, 5)$ in the above trace, therefore, the edge from node 1 to node 5 in the causality graph is labeled with 2.

B. Generating and Solving Consistency Constraints

The constructed causality contains potential models for the input trace, however, it also contains a lot of inconsistencies. Consider node 1 and all its outgoing edges. The node support is 2, and the total support of its outgoing edges is 6. This inconsistencies is due to the ambiguities when finding supports for edges. In this example, since we do not know what the other messages should be correlated with message 1, we consider all possibilities by finding supports for all binary...
sequences starting with message 1, i.e., (1,2), (1,4), and (1,5). As a result, message 1 is counted more times than it should be.

The goal of this step is to find a set of edge supports such that they are consistent with node supports. First, let \( x \rightarrow y \) denote an edge from node \( x \) to \( y \), and \( \text{sup}(\cdot) \) be the support of either a node or an edge. Additionally, let \( c(n \rightarrow n') \) be a variable about the support of \( n \rightarrow n' \). From the causality graph, we derive the following constraints.

1) For each node \( n \), and all its outgoing edges \( n \rightarrow n' \), create a constraint

\[
\text{sup}(n) = \sum_{n \rightarrow n'} c(n \rightarrow n')
\]

2) For each node \( n' \) and all its incoming edges \( n \rightarrow n' \), create a constraint

\[
\text{sup}(n') = \sum_{n \rightarrow n'} c(n \rightarrow n')
\]

3) For each edge \( n \rightarrow n' \), create a constraint

\[
0 \leq c(n \rightarrow n') \leq \text{sup}(n \rightarrow n')
\]

The first two constraints require consistencies between every node and its incoming and outgoing edges. The third constraint reflects the fact that it is unknown about the exact edge supports when scanning the trace for instances of an edge except it can be no more than the supports directly obtained from the trace.

### C. Deriving Model

After the constraint problem \( P \) is generated, it is fed into a constraint solver to find a solution. A solution \( sol \) of \( P \) is a set of edges in the causality graph \( G \) such that their supports are consistent with the node supports,

\[
\{(n \rightarrow m) \mid (n \rightarrow m) \in G, \text{ and } c(n \rightarrow m) > 0 \text{ in } sol\}.
\]

The solution can be visualized as a modified causality graph with the edge supports as returned from the solver. An example solution for the causality graph in Fig. 4 is shown in Fig. 4(a) and the corresponding FSA model is shown in Fig. 4(b). Note that in Fig. 4(a), edges from Fig. 4(b) with zero-supports in the solution are removed.

For a set of constraints \( P \) generated in the previous step, a large number of consistent solutions can be generated. Finding the minimal solution is NP-hard. Therefore, the goal of this step is to generate a reduced, not necessarily minimal, solution efficiently. In our method, we query the solver to return a set of solutions \( S = \{sol \mid sol \models P\} \). Then, for each solution \( sol \in S \), and for each edge \( (n \rightarrow m) \) with non-zero support in \( sol \), a new constraint is generated where its support is set to 0. After adding this constraint into the solver, if the solver becomes unjustifiable, \( sol \) is return as the candidate model. Otherwise, the above step repeats for the reduced solution \( sol' \).

At the end, from the set of reduced solutions, we select the one with the smallest number of edges with non-zero support, and return it to the user. The model extraction method is shown in Algorithm 2. The model in Fig. 4 shows an example model extracted using Algorithm 2. Note that sequence (1, 3) or (2, 4) is not included in the model.

After a reduced solution is returned as described above, a FSA can be constructed from it. This step is straightforward, and we skip its explanation.

### IV. Experimental Results

We collect ten message flows which are abstracted from system-level communication protocols used in real industry SoC designs. Each flow consists of a number of branches, resulting in a total number of 64 message sequences to specify various system communication scenarios such as cache-coherent memory accesses, upstream read/write, power management, etc. Although greatly simplified, these message flows capture essential communicating behaviors among typical components in a SoC design, including CPUs, caches, interconnect, memory controller, and peripheral devices, etc.
We implement a transaction-level simulation model where components in the model communicate with each other according to the protocols specified by these message flows. During simulation, each master component randomly initiates a message flow instance by generating a message, and sends it to the next component as specified. Since the message payloads are not considered in the message flows, they are not generated during the simulation, and each message only carries a command and the address of the destination component. In order to mimic the concurrent nature of modern SoC designs, the interconnect component of our simulation model is modeled as a switch network. This component model allows messages from a source to go to all other destinations as specified. In case when messages arriving from multiple sources simultaneously, they are interleaved using an internal arbiter before being sent out. All components run concurrently without global synchronization.

We simulate the model multiple times, collecting two sets of traces of different lengths. The first set of traces are generated when the model is restricted to only allow CPUs to initiate cache coherent downstream read flows while all other components are configured to only react to incoming messages. This set of traces are referred to as small. The second set of traces are generated with all components in the model are enabled to initiate message flows. This set of traces are referred to as large. For each configuration, we simulate the model three times. In each run, a limit is imposed on the number of instances of each flow allowed to be generated during simulation. We collect a total of six traces.

We implement the method described in this paper in Python. The SMT solver for solving the constraint problems in our method is the Python distribution of the Z3 solver [15]. We run our tool on the sets of collected traces, and the results are shown in Table I. The first two columns show the types and the number of unique messages in each type of traces. The third column shows the lengths of the traces in terms of the total number of messages included. The fourth column shows the number of states in the extracted FSA models, while the last column shows the runtime in seconds.

From Table I the runtime for handling each trace takes about 1 to 1.5 minutes, and it does not change much for traces of different lengths. This phenomenon can be explained as follows. The major portion of the total runtime (> 95%) is spent on the SMT solving, which is dependent on the sizes of the causality graphs in terms of the numbers of edges with non-zero support. The size of causality graphs depends on the number of unique messages in traces, and is much smaller than trace lengths. Additionally, causality graphs are relatively similar for traces of the same type. Therefore, solving constraint problems generated from such causality graphs incurs similar complexity, and its runtime performance is largely independent of trace lengths. This observation contrasts our method against previous work such as [4].

There are two other interesting observations from Table I. First, the runtime drops slightly for the traces of the same type; second, the runtime for the traces of different types is also similar. These observations seem to contradict to the above analysis. However, we believe these results are due to the nature of SMT solving. For traces of the same type, they are randomly generated, resulting different constraint problems. As a result, the initial sets of solutions generated are different. They would lead to different amount of runtime needed to reduce every one of those initial solutions. Overall, the runtime taken by invoking procedures in Algorithms 2 and 3 could be different for the traces of the same type. The above analysis can also explain why the runtime for traces of type Large is close to that for small traces.

We compare our method with Trace2Model described in [4]. It is similar to our method in that both try to synthesize FSA models to fit input traces by using some forms of constraint solving. However, Trace2Model does not consider concurrency nature of the traces as our method does, and it extracts a model only based on sequential dependencies in the traces. In experiments, we fix the size of the sliding window \( w \) in Trace2Model to 3 as suggested in [4]. Trace2Model suffers from considerably long run time when being applied to our traces, and it does complete even for the small traces after 30 minutes. Therefore, no results with Trace2Model are reported.

Experiments on a GEM5 Model. We develop a realistic system model in GEM5, and gather communication traces for a real-workload. This model, developed in Syscall Emulation (SE) mode, consists of four x86 TimingSimpleCPUs, each with private Level 1 (L1) data (64kB) and instruction (16kB) caches. There is a shared Level 2 (L2) cache of size 256kB. L1 and L2 caches are interfaced with a coherent bus that implements MOESI-like coherent protocol provided in GEM5. There are also a memory bus and a DDR3_1600_8x8 memory controller with a memory of 512MB. A high-level view of the simulation system is given in Figure 5.

| Traces | #Messages | Length | #States | Runtime |
|--------|-----------|--------|---------|---------|
| small  | 22        | 460    | 31      | 84      |
|        |           | 920    | 31      | 78      |
|        |           | 1840   | 31      | 70      |
| large  | 60        | 2180   | 92      | 75      |
|        |           | 4360   | 87      | 72      |
|        |           | 8720   | 100     | 62      |

**Fig. 5:** A quad-core simulation model developed in GEM5 System-Call Emulation mode.

**TABLE I:** Results from the simulation traces

![Simulation System Diagram](image-url)
Model synthesis for communication traces from highly concurrent SoC executions is very challenging. We describe a method that infers reduced and abstract models from such traces, and show that it is able to infer models efficiently, even for very long traces. The extracted models include meaningful information about system-level protocols implemented in the target SoC designs. We plan to enhance the method to allow user insights to be used easily to guide the search process.

Acknowledgment The research presented in this paper was partially supported by gifts from the Intel Corporation, and a grant from Cyber Florida.

REFERENCES

[1] Jinlin Yang, David Evans, Deepali Bhardwaj, Thirumalesh Bhat, and Manuvir Das. Perraccotta: Mining temporal api rules from imperfect traces. In Proceedings of the 28th International Conference on Software Engineering, ICSE ’06, pages 282–291, 2006.

[2] Lingyi Liu and Shobha Vasudevan. Automatic generation of system level assertions from transaction level models. Journal of Electronic Testing, 29(5):669–684, Oct 2013.

[3] Artur Mrowca, Martin Nocker, Sebastian Steinhorst, and Stephan Gün- nemann. Learning temporal specifications from imperfect traces using bayesian inference. In Proceedings of the 56th Annual Design Automation Conference 2019, DAC ’19, pages 99:1–99:6, 2019.

[4] Natasha Jeppu, Tom Melham, Daniel Kroening, and John O’Leary. Learning concise models from long execution traces. In DAC ’20, June 2020.

[5] Ivan Beschastnikh, Yurii Brun, Sigurd Schneider, Michael Sloan, and Michael D. Ernst. Leveraging existing instrumentation to automatically infer invariant-constrained models. In Proceedings of the 19th ACM SIGSOFT Symposium and the 13th European Conference on Foundations of Software Engineering, ESEC/FSE ’11, pages 267–277, 2011.

[6] Wenchao Li, Alessandro Forin, and Sanjit A. Seshia. Scalable specification mining for dynamic assertions mining on control signals. In Proceedings of the 47th Design Automation Conference, DAC ’10, pages 755–760, 2010.

[7] Samuel Hertz, David Sheridan, and Shobha Vasudevan. Mining hardware assertions with guidance from static analysis. Trans. Comp.-Aided Des. Integ. Cir. Sys., 32(6):952–965, June 2013.

[8] A. Danese, F. Filini, and G. Pravadelli. A time-window based approach for dynamic assertions mining on control signals. In 2015 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), pages 246–251, Oct 2015.

[9] Alessandro Danese, Tara Ghasempouri, and Graziano Pravadelli. Automatic extraction of assertions from execution traces of behavioural models. In Proceedings of the 2015 Design, Automation, & Test in Europe Conference & Exhibition, DATE ’15, pages 67–72, 2015.

[10] Alessandro Danese, Nicolò Dalla Riva, and Graziano Pravadelli. A-team: Automatic template-based assertion miner. In Proceedings of the 54th Annual Design Automation Conference 2017, pages 37:1–37:6, 2017.

[11] Po-Hsien Chang and Li.-C. Wang. Automatic assertion extraction via sequential data mining of simulation traces. In ASPDAC, pages 607–612, 2010.

[12] Marijn J. Heule and Sicco Verwer. Software model synthesis using satisfiability solvers. 18(4), 2013.

[13] Kevin J. Lang, Barak A. Pearlmutter, and Rodney A. Price. Results of the abadango one dfa learning competition and a new evidence-driven state merging algorithm. In ICGI, page 1–12, 1998.

[14] V. Ulyantsev and F. Tsarev. Extended finite-state machine induction using sat-solver. In ICMLAW, volume 2, pages 346–349, 2011.

[15] The Z3 Theorem Prover. https://github.com/Z3Prover/z3, 2020. Online; accessed 17 November 2020.
[16] Memory System in gem5. http://pages.cs.wisc.edu/~swilson/gem5-docs/gem5MemorySystem.html. Online; accessed November 16, 2020.