Design and Implementation of Quantum Dot Cellular Automata Based Irreversible and Reversible Logic Generator Block

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Abstract: Abstract: Quantum Dot Cellular Automata has attracted a lot of attention due to its extremely small feature size and ultra low power consumption. It is a possible alternative for transistor based technology. This paper presents the construction of Irreversible and reversible Logic Generator Block using quantum dot cellular automata. QCA based Irreversible and irreversible Logic generator block generates the logic of various devices like 1-Bit comparator, 1-Bit Half Adder, 1-Bit Half Subtractor, AND gate, XOR gate, NOR gate and XNOR gate. Proposed design of QCA based LGB is cost effective and easy to fabricate due to absence of wire crossings in irreversible LGB and no information loss in reversible LGB. This block can be made more efficient by using control lines. Depending on individual value on control line, logic of individual device will be generated. QCADesigner 2.0.3 tool is used for design and simulation of QCA based Logic Generator Block. Similarly here Reversible logic based Logic generator block is proposed which will be able to generate different logic. Area requirement of Reversible LGB is 85% less as compared to Irreversible LGB. Reversible logic provides ideally zero power dissipation that is no information loss is there.

Keywords: Arithmetic Logic Unit (ALU), Logic Generator Block (LGB), Reversible Logic, Dot Cellular automata (QCA).

1. INTRODUCTION
According to Moore’s law, the number of transistors on a unit area get double every 18 months [1]. The International Technology Roadmap for semiconductors (ITRS) projects that the scaling
of the CMOS technology will continue till 2019 [2]. Present transistor based technology faces consequences like leakage current, power dissipation, oxide thickness, electron migration in feature size reduction [3][4]. QCA technology solves the problem of interconnecting wires as coupling mechanism is done by Coulombic interaction. Unlike in CMOS, QCA approach permits high speed operation, ultra low power dissipation and avoids the problem of interconnect delay and information loss, which would drastically enhance the system performance. Proposed design of Logic Generator Block helps to generate multiple functions.

2. QCA BASICS

A. QCA Cell
QCA cell is comprised of four quantum dots in square structure. Quantum dot is made using GaAs / AlGaAs and Si/SiO$_2$ material system. Electrons repel each other hence they occupy two quantum dots which are in diagonally opposite direction. Electron can tunnel from one quantum dot to other. Thus it gives two stable states logic 0 i.e. polarization of -1 and logic 1 i.e. polarization of +1 as shown in Fig. 1. QCA is known as charge holder device by using a Coulombic repulsion method. Basic logic blocks like wire, Majority voter gate, inverter, and crossover wires are made using QCA cell.

B. QCA Wire
QCA wire is built using multiple number of QCA cells in which information transfers from one cell to adjacent cell because of electrostatic interaction between neighbouring cells. Depending upon the orientation of QCA cells two types of wires are available for the design of QCA circuits. Wire with 90° oriented QCA cell is shown in Fig. 2A and Second type of QCA wire with 45° oriented QCA cells is shown in fig. 2B. If wire is made using even number of 45° rotated cells as shown in fig. 2B, output will be complement of input. In contrast if odd number of 45° rotated cells are used, output will be same as input. QCA wire with different clock zones are used to obtain memory.

![Fig. 1 QCA Cell](image1)

![Fig. 2 (A). QCA Wire](image2)

![Fig. 2 (B). QCA Wire using 45° rotated cells](image3)
C. *QCA Clock*

The QCA cell itself is a storage cell, computing cell, and wire. A series of QCA cells act like a wire. The signal flow is controlled by clocks. As the main source of the synchronization, a clock plays a key role in the QCA circuit [6]. QCA clock is required in all the circuits to synchronize and control flow of information, the clock actually provides the power to run the circuit [7].

D. *QCA Wire Crossings*

Coplanar wire crossings and multilayer wire crossings are the two types of QCA wire Crossings. Crossing of two wires in one plane can be achieved by placing 90° binary wires in between 45° inverted wires as shown in fig. 3(A). The two signals are able to cross each other without interference since the wires of different orientation do not have any switch effect on each other [12]. Hence the kink energy is zero. From fig. 3(A) output YA is same as input A and YB is equal to B. Hence these two wires can be treated as two different signals.

Multilayer Wire Crossings has three different layers that is Main layer, Via layer and crossover layer. The cells are placed in multiple layers so that signals can pass properly in multiple layers using vertical interconnect [13]. Layout of Multilayer Wire Crossings is shown in Fig 3(B).

3. **BASICS OF REVERSIBLE LOGIC**

*Reversible Logic Gates*

The original inspiration was that reversible gates dissipate no heat [8]. Any reversible gate must have the same number of input and output bits. Reversible computation is achieved at a logical level by launching a one-to-one mapping between the input and output vectors in the logic circuit. Bennett showed that if a computation is carried out in reversible manner, kTln2 energy dissipation will not occur [9]. The quantum cost of any reversible gate is calculated by counting the number of 1x1 and 2x2 quantum gates requisite in its design. The quantum costs of reversible 1x1 and 2x2 gates are considered as unity [10]. Any reversible gate can be recognized using Controlled-V and Controlled-V + and the Feynman gate. Fig.4 shows reversible XOR gate which is also known as Feynman gate.

4. **PROPOSED WORK**

A. *QCA Based Logic Generator Block [14]*

Logic Generator Block using QCA is proposed in this paper. The block Schematic of LGB is shown in Fig.5.
Basic QCA logic gates like Majority Voter and Inverter are used for the implementation of LGB. The schematic and functionality of LGB is shown in fig. 6 and Table I respectively. Truth table of Logic Generator Block and its logical diagram is shown in Table III table IV.

As shown in fig.6, logic of 1-bit comparator, Half adder, Half Subtractor, XOR gate, XNOR gate, AND gate and NOR gate is generated using single block. Functions of all the devices/components which are available at the output of LGB are basic and required for almost all the digital applications like Arithmetic Logic Unit and in turn Nanoprocessors.

**TABLE I.** FUNCTIONAL TABLE OF LGB

| S.N. | Control Signal | Output of LGB |
|------|----------------|---------------|
| 1    | 0 0 0 0        | 1-Bit Half Adder |
| 2    | 0 0 0 1        | 1-Bit Half Subtractor |
| 3    | 0 1 1 0        | 1-Bit Comparator |
| 4    | 0 1 1 1        | XOR            |
| 5    | 1 0 0          | XNOR           |
| 6    | 1 0 1          | NOR            |
| 7    | 1 1 0          | AND            |
| 8    | 1 1 1          | Not Applicable |

Hences instead of implementing separate QCA layout for all these devices, it is beneficial to use LGB as the area required for LGB is less as compared to that of total area of the individual logic devices[8][9][10]. Equations of LGB is as below

**1-Bit Half Adder:**

\[
SUM = MV(MV(MV(A, B, 0), B, 0)) \cdot MV(MV(A, B, 1), 0, B, 1) \\
CARRY = MV(A, B, 0)
\]
1-Bit Half Subtractor:

\[
\begin{align*}
\text{DIFFERENCE} &= \text{NOR}(\text{NOR}(A, B, 0), B, 0), \text{NOR}(A, B, 1, 0, 0, 0) \\
\text{BORROW} &= \text{NOR}(\text{NOR}(A, B, 0), B, 0)
\end{align*}
\]

1-Bit Comparator:

\[
\begin{align*}
A < B &= \text{NOR}(\text{NOR}(A, B, 0), B, 0) \\
A = B &= \text{NOR}(\text{NOR}(A, B, 0), \text{NOR}(A, B, 1), 1) \\
A > B &= \text{NOR}(\text{NOR}(A, B, 1), 0, 0)
\end{align*}
\]

XOR Gate:

\[
\text{XOR} = \text{NOR}(\text{NOR}(A, B, 0), B, 0), \text{NOR}(A, B, 1, 0, 0, 0)
\]

XNOR gate:

\[
\text{XNOR} = \text{NOR}(\text{NOR}(A, B, 0), \text{NOR}(A, B, 1), 1)
\]

NOR Gate:

\[
\text{NOR} : \text{NOR}(A, B, 1) = A + B
\]

AND Gate:

\[
\text{AND} : \text{NOR}(A, B, 0) = A \cdot B
\]

B. Reversible Logic based Logic Generator Block

Reversible gate named XMS gate is proposed in this paper. XMS stands for XOR, Multiplexer and Sum.

Equations of Reversible XMS gate is,

\[
\begin{align*}
P &= A \oplus B \\
Q &= A \cdot B + A \cdot C \\
R &= B \oplus C
\end{align*}
\]

![Fig. 6.1 Block Diagram of Reversible XMS Gate](image)

Truth table of XMS gate is as shown in Table II

In Reversible logic gates power dissipation in almost zero i.e. there is no information loss. All the inputs are available at the output side. These types of gates are also used for the fault detection in the circuit if parity of inputs and outputs gets matched. In Future, Fault tolerant XMS gate can be designed.

| Inputs | Outputs |
|--------|---------|
| A | B | C | P | Q | R |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| S.N. | Control Signal | Output of Reversible LGB | Equation |
|------|----------------|--------------------------|----------|
| 1    | X X X         | P = Sum OF Full Adder    | $P = A \oplus B \oplus C$ |
| 2    | X X X         | Q=2:1 Multiplexer        | $Q = A \cdot \overline{B} + A \cdot C$ |
| 3    | X X X         | R= 2 input XOR Gate      | $R = B \oplus C$ |
| 4    | X X 1         | P = 2 Input XNOR Gate    | $P = A \oplus B$ |
| 5    | X X A         | Half Adder               | $R = A \oplus B$ |
| 6    | X 0 B         | Half Subtractor          | $Q = A \oplus B$ |
| 7    | X X 0         | 2 Input AND Gate         | $Q = A \cdot B$ |
| 8    | X 0           | 2 Input NOR Gate         | $Q = A + B$ |
| 9    | X 0 0         | Pass Logic               | $P = A, R = B$ |
| 10   | X 0           | Complement               | $X = \overline{A}$ |

This proposed gate will be working as a reversible logic generator by changing the inputs as shown in Table III.

5. RESULTS
Implementation of Logic Generator Block is shown in Fig.7,

![Fig.7 QCA Layout of Irreversible Logic Generator Block [14]](image_url)

Layout of XMS gate also known as reversible logic generator block and its simulation result is shown in Fig. 8 and Fig. 9 respectively.
Fig. 8 QCA Layout of Reversible Logic Generator Block

Fig. 9 Simulation Result of Reversible Logic Generator Block

6. PARAMETRIC ANALYSIS

| Parameters                              | QCA based Logic generator block | Reversible gate [XMS] based Logic generator block |
|-----------------------------------------|---------------------------------|--------------------------------------------------|
| No. of clock zones [Delay]              | 6                               | 7                                               |
| Total Number of cells [Complexity]      | 162                             | 204                                             |
| area                                    | 2916 nm²                        | 0.42µm²                                         |
| Simulation Time                         | 4 sec                           | 4 sec                                           |
| Total Number of QCA Gates               | 7 MV, 3 Inverters               | 7 MV, 2CMVMIN, 8Inverters                       |
| Number of wire crossings                 | Zero                            | 3                                               |
| Number of Logic functions generated     | 7                               | 10                                              |
CONCLUSION

Design and Simulation of Irreversible and Reversible Logic Generator Block is done using QCADesigner tool [11]. Functionality of both the LGBs is verified. Only one and half clock cycle is required for the generation of complete Irreversible design whereas 1.75 clock cycles are required for the implementation of reversible design, which results in fast circuit. Number of QCA gates required for the implementation of Irreversible LGB is 10 (7 MV and 3 Inverters) whereas for reversible LGB is 18 (3 CMVMIN, 7 MVs, 8 Inverters) QCA gates are required but using conventional method for the implementation all these logic devices 33 QCA gates are required (19 MV, 14 Inverter) So the proposed circuits are area efficient which can be used in Arithmetic logic unit and Nanoprocessors which may also be reversible ALU or Reversible nanoprocessors. Proposed Irreversible LGB circuits has zero wire crossings whereas 3 wire crossings are required for reversible LGB as shown in Table IV. Area required for designing reversible LGB is 85% less as compared to Irreversible LGB. Fabrication of this single layered device i.e. irreversible LGB is easy as compared to other existing multilayered arithmetic logic units and reversible LGB will be used for building the nanoprocessors with negligible power dissipation.

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