Self-oscillating isolated-buck (fly-buck) converter

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Abstract
This study presents a self-oscillating fly-buck converter. The primary objective of this research is to lower the final bill of materials cost of a fly-buck converter. The fly-buck converter is based on a relaxation self-oscillation circuit. The main transformer is updated with two additional auxiliary windings for positive feedback implementation. The turn ratios of these windings are estimated, and criteria for a stable oscillation mode are developed. A switching frequency formula is also provided. Furthermore, an example start-up circuit is proposed and calculated. Output voltage stabilisation is implemented and demonstrated to work with ±10% variations in input voltage. The experimental data and design procedure are presented along with a comparison of the proposed fly-buck converter against conventional fly-buck converters. The converter is optimised for maximum efficiency, with an efficiency of > 85% demonstrated at 20 W output power. The proposed self-oscillating circuit can also be implemented in a conventional synchronous buck converter. The Maxima software code for automated calculation of the converter is supplied as supplemental active media content.

1 INTRODUCTION

The fly-buck (isolated buck) converter is widely used as a simple solution to the provision of isolated power supply [1, 3–7]. It is simply a synchronous buck converter with additional windings coupled to the primary inductor providing isolated outputs (Figure 1). The fly-buck converter is extensively used as a gate drive power supply [2, 19], to provide biasing for analogue circuits and as a buck-boost converter as well as in other applications requiring multiple isolated outputs. Compared with other topologies, a fly-buck converter has the following advantages:

- The turn ratio of the windings determines the secondary voltages. This topology makes it possible to circumvent the use of an octocoupler because all the outputs are tightly coupled.
- The fly-buck converter has a primary non-isolated output, which can also be used on the primary side circuits.
- The fly-buck converter has few active components. Two switches work on the primary side, only one diode is present on each isolated output, and the maximum rated voltage of the primary switches is fixed to the maximum input voltage.
- The fly-buck converter always operates in a synchronous rectification mode, guaranteeing a continuous current mode (CCM). This further improves the load regulation characteristics of the fly-buck converter, as the output voltages are less dependent on the load and cross-regulation [20].

Originally, fly-buck converters were controlled via pulse width modulation (PWM) or constant on-time controllers, which require an integrated circuit (IC) ([8, 9]). This approach increases the bill of materials (BOM) cost of the entire converter.

Self-oscillating converters of different topologies are widely used in low-power converters because of their low cost. Examples can be found in the power supply systems of modern desktop computers, in which self-oscillating converters are used as an auxiliary power supply or stand-by converter. Another example are 1W/2W DC–DC converters with galvanic isolation based on the Royer converter or Baxandall’s resonant design [10, 11], which are commercially available from different manufacturers. The primary advantage of the self-oscillating converter family, as claimed by the power supply industry, is their low cost.

Most cost reduction methods cause efficiency degradation, and the final version of an optimised conventional fly-buck converter still includes an IC controller ([8, 9]) or a micro-controller, raising the cost. The proposed self-oscillating converter allows
for the implementation of an additional cost optimisation step: elimination of the IC controller.

In summary, the self-oscillating fly-buck converter has the following advantages:

- **Low cost** because the IC can be omitted from the BOM.
- **Input voltage levels** for the self-oscillating converter are much higher than for the currently available integrated solutions. For example, the proposed self-oscillating converter can be used as an off-line converter at a DC line voltage of \( \approx 350 \text{ V} \).
- **The self-oscillation converter** has smoother waveforms and low electromagnetic interference (EMI) emissions due to the properties of the oscillation mechanism, which permits circumventing the use of snubbers for ringing damping of the primary side switches.
- **The lifespan** of the self-oscillation circuit is increased due to the elimination of the IC. This calculation is based on the standard MIL-HDBK-217F [17].

The proposed converter might have some disadvantages:

- **Lower efficiency** and high losses in no-load conditions due to the high ripple current in the \( L_m \) inductance.
- **Possible high output voltage overshoot** because of the start-up circuit.

The goal of this research is to decrease the cost of fly-buck converters using a self-oscillation relaxation circuit. This approach makes it possible to circumvent the use of PWM controller ICs, yielding a simple design and a low-cost fly-buck converter. The following features of the proposed converter have been formulated to demonstrate the self-oscillating mechanism and dissimilarities from a conventional converter:

- The duty cycle must be different from 50% for versatility, enabling different applications.
- The output power level has to be \( \geq 20.0 \text{ W} \), which is a typical requirement for an auxiliary power supply for a fuel-cell controller board [18].

An external (non-integrated) switch control is required for versatility, facilitating maximal input voltages and output power levels.

The contributions of this study can be summarised as follows:

- A self-oscillating fly-buck converter is proposed that can operate at duty cycles other than 50%.
- The proposed converter can also be used as a self-oscillating buck converter because the buck converter can be considered as a specific case of the fly-buck converter.
- The equations and calculation procedure developed for the proposed converter are presented. The turn ratios for the windings have been estimated, and criteria for a stable oscillation mode have been developed. A switching frequency formula is also provided.
- The proposed design procedure can be used for any number of secondary outputs because neither equation includes the secondary voltage, and only the total output power is essential.
- The zero-voltage switching (ZVS) conditions calculated in this study can be applied in conventional fly-buck converter calculations.
- The equations can also be applied to other topologies based on the half-bridge self-oscillating circuit.
- Start-up and voltage stabilisation circuits are proposed and calculated.
- The Maxima software code for automated calculation of the converter is also supplied as supplemental active media content.

The subsequent sections describe the design stages and the calculation of the converter components, including the gate drive windings (Section 3.2) and the switching frequency calculation (Section 3.3). The criteria for stable oscillation and ZVS in the switches are presented in Section 3.1, and the optional output voltage stabilisation circuit is described in Section 3.5. An example of the start-up circuit is presented in Section 3.4, and the design procedure for the elements of the self-oscillating mechanism and the experimental validation are described in Section 4.

2  |  CONVERTER CIRCUIT AND OPERATION

2.1  |  Converter circuit development

Self-oscillating converters have long been used due to their simplicity and low cost [12, 13]. In self-oscillating converter circuits, positive feedback is utilised to create an oscillating mode of operation. A self-oscillating power supply can be constructed as a blocking power supply or as a self-relaxing power supply, and there are different types of self-oscillating power supplies described in the literature [12, 13]. Blocking converters are based on the saturation of the core of the main transformer,
while in a self-relaxing power supply the switches are blocked when voltages or currents in the passive components exponentially decay to a specific value. The fly-buck converter proposed in this study is based on a self-relaxing power supply.

A fly-buck converter can be modified into a self-oscillating converter using a half-bridge circuit. A comparison of the two converters and the converter development are illustrated in Figure 2. The B node of the half-bridge converter becomes the $V_{\text{out}1}$ node of the fly-buck converter. There are significant differences that must be considered:

- There is no capacitor divider in the fly-buck converter. The $V_{\text{out}1}$ node has zero potential at start up, and the bottom switch, Q2, cannot be used for start-up pulse generation.
- The Q1 and Q2 switches in the fly-buck converter determine the output voltage $V_{\text{out}1}$ and have different switch-on times. A conventional half-bridge converter (Figure 2(a)) typically operates with a duty cycle of close to 50%.
- The fly-buck converter has asymmetrical current waveforms for the Q1 and Q2 switches, which necessitates different conditions for ZVS and different stable oscillation criteria for these switches.

In the subsequent sections, the listed features are employed in the component calculations.

### 2.2 Converter circuit description

The proposed self-oscillating fly-buck converter is presented in Figure 3. It is a conventional fly-buck converter equipped with additional auxiliary windings $L_{\text{aux},Q1}$ and $L_{\text{aux},Q2}$ for the gate drive control. The windings are coupled to the main inductor $L_m$ such that they provide positive feedback for a self-oscillation mode. The turn ratios of the auxiliary windings are $1 : N_{Q1}$ and $1 : N_{Q2}$, and theoretically they may be different for the Q1 and Q2 switch gate circuits. The equivalent resistor-capacitor (RC) circuits that determine the on state time for each MOSFET are presented by networks $(R_{1Q1}, C_{1Q1}$ and $R_{2Q1})$ and $(R_{1Q2}, C_{1Q2}$ and $R_{2Q2})$. If their equivalent time constants are different for the Q1 and Q2 switches, the duty cycle can be regulated to the required voltages for the outputs. These RC circuits also regulate the switching frequency $F_{\text{sw}} = 1/T$ of the converter. Zener diodes $D_{z1}$-$D_{z2}$ have two important functions: First, they provide over-voltage protection for the gates of Q1 and Q2 during transient and start-up processes. Second, they fix the level of the gate voltage at the start of the on state such that the switch-on time is constant and dependent only on the parameters of the RC circuits and not on the input or output voltages. The Zener voltage on the $D_{z1}$-$D_{z2}$ diodes is denoted by the $V_{\text{zener}}$ parameter. The inductance $L_{\text{leak,}x}$ is the leakage inductance of the simplified model of the main transformer $T1$ reflected to the secondary side of the transformer. The current flowing through the primary winding of the transformer $T1$ is denoted by $i_1$, and the current flowing through the secondary winding is denoted by $i_2$. The currents in the Q1 and Q2 switches are denoted by $i_{Q1}$ and $i_{Q2}$, respectively, with positive directions selected as outlined in Figure 3 flowing into the drains of the MOSFETs. The magnetising current of the magnetising inductance $L_m$ is denoted by $i_{L_m}$.

The steady-state waveforms are presented in Figure 4. At the $t_0$ - $t_1$ interval, the Q1 switch is on and the Q2 switch is off, the D1 diode is blocked and power is delivered only to the primary
FIGURE 4 Main waveforms of the self-oscillating fly-buck converter

output $V_{out1}$. At the $t_1 - t_2$ interval, the Q1 switch is off and the Q2 switch is on, the D1 diode is open and power is delivered to all outputs. The duty cycle is equal to $D = \frac{t_1 - t_0}{T}$. The voltage at the primary output has the same expression as a conventional buck converter

$$V_{out1} = V_{in}D,$$  \hspace{1cm} (1)

where $V_{in}$ is the input voltage of the converter and $V_{out1}$ is the voltage at the primary non-isolated output. If the converter has $M$ number of outputs and $M - 1$ of them are galvanically isolated, the theoretical secondary voltages $V_{out2}, ..., V_{outM}$ can be derived as follows:

$$V_{out2} = V_{out1}N_{sec2}$$
$$V_{out3} = V_{out1}N_{sec3}$$
$$\vdots$$
$$V_{outM} = V_{out1}N_{secM}$$ \hspace{1cm} (2)

The actual output voltages may differ from the theoretical values due to non-ideal switches, leakage inductance and cross-regulation effects.

When the Q1 switch is on and the Q2 switch is off (moment $t_0$), there is a voltage ($V_{in} - V_{out}$) across the main inductor $L_m$. This voltage is transformed to voltage at the auxiliary winding $L_{aux,Q1}$ and is equal to

$$E_{1Q1} = (V_{in} - V_{out})N_{Q1}$$ \hspace{1cm} (3)

This voltage keeps the Q1 switch switched on until relaxation of the RC circuits ($R_{1Q1}, C_{1Q1}$ and $R_{2Q1}$) reduces the voltage at the gate to the MOSFET threshold $V_{th}$. At this moment ($t_1$), the Q1 switch turns off when the current flowing through it is equal to $I_{off,Q1}$. This current must be positive and sufficient to satisfy the ZVS condition for the voltage at node A to drop to zero, which turns on the Q2 switch. The voltage across $L_m$ then reverses polarity and becomes $-V_{out}$. This voltage is then transformed to a negative voltage across $L_{aux,Q1}$. The absolute value of the voltage can be expressed as follows:

$$E_{2Q1} = V_{out}N_{Q1}$$ \hspace{1cm} (4)

The gate of the Q1 switch rapidly jumps to a negative voltage. For the interval from $t_0$ to $t_1$, the voltage across $L_{aux,Q2}$ is negative, with an absolute value

$$E_{2Q2} = (V_{in} - V_{out})N_{Q2}$$ \hspace{1cm} (5)

From the moment $t_1$ when the Q1 switch is off, the gate of Q2 rapidly jumps to a positive voltage, the Q2 switch is on and a voltage $-V_{out}$ appears across the main inductor $L_m$. This voltage is transformed to voltage at the auxiliary winding $L_{aux,Q2}$ and is equal to

$$E_{1Q2} = V_{out}N_{Q2}$$ \hspace{1cm} (6)

This voltage keeps the Q2 switched on until relaxation of the RC circuits ($R_{1Q2}, C_{1Q2}$ and $R_{2Q2}$) reduces the voltage at the gate to the MOSFET threshold $V_{th}$. At this moment ($t_2 = T$), the Q2 switch turns off, the current flowing through it, which is equal to $I_{off,Q2}$. This current must be positive and sufficient to satisfy the ZVS condition for the voltage at node A to rise to $V_{in}$, switching on Q1. This cycle is then repeated with a period $T = \frac{1}{f_{sw}}$. 

$\quad$
3 | COMPONENT CALCULATIONS

This section presents component calculations related to the self-oscillating mode of operation. The selection of the power components is based on a methodology described in [4, 5, 14], and Figure 3 is used as the basis for further calculations. For further derivations, it is assumed that Q1 and Q2 are identical MOSFET switches with a small on-resistance, an input gate capacitance of $C_{\text{gs}}$, and an output drain-source capacitance of $C_{\text{oss}}$. The secondary side diodes (e.g. D1) are also assumed to be ideal diodes, with no switching losses and zero forward voltage drop.

3.1 | Stable oscillation criteria

For stable oscillations at the desired switching frequency and duty cycle, two conditions must be satisfied. First, when the Q1 switch is off, with a current $i_{\text{off,Q1}}$, the voltage at the node A (Figure 3) must drop rapidly from $V_{\text{in}}$ to a zero potential. Thus, the voltage across $L_m$ is reversed. Second, a similar process must occur when the Q2 switch is off, with a current $i_{\text{off,Q2}}$. At this moment, the voltage at node A must rapidly jump from zero potential to $V_{\text{in}}$. In sum, ZVS conditions must be satisfied for both the Q1 and Q2 switches. Hence, the following conditions must be met:

- The currents $i_{\text{off,Q1}}$ and $i_{\text{off,Q2}}$ must be positive for the Q1 switch and the Q2 switch, respectively. The positive directions of the Q1/Q2 currents are shown in Figure 3.
- The currents $i_{\text{off,Q1}}$ and $i_{\text{off,Q2}}$ must be large enough to change the potential at node A fast enough to meet the $\frac{dV}{dt}$ requirements. Thus, the transient process must be ended within a $\tau_\text{in}$ transition time.

It can be seen from Figure 4 that the leakage inductance $L_{\text{leak}}$ has a significant effect on the shape of the secondary current $i_2$ at the interval $t_1 - t_2$. The smaller the $L_{\text{leak}}$, the greater the peak current and the smaller the effective pulse width. In an extreme case, when the leakage inductance is $L_{\text{leak}} \rightarrow 0$, the current is $i_2(t_2) \rightarrow 0$ at the end of the cycle. This case is represented by a dashed line for $i_1$, $i_2$ and $i_{Q2}$ waveforms. Analysing these cases and waveforms, the main component that can be used to achieve ZVS and stable oscillations is the magnetising inductance $L_{\text{m}}$. Using the definitions in Figure 3 and the waveforms in Figure 4, the minimum value of $L_{\text{m}}$ can be found.

First, we consider the process of switching off Q1 at moment $t_1$. To charge and discharge the $C_{\text{oss}}$ capacitances of Q1 and Q2, the condition $i_{\text{off,Q1}} \geq 0$ must be met, and it can be rewritten as follows

$$i_{L_m}(t_1) > 0$$  \hfill (7)

This condition is always true, as it is for the conventional buck converter. The is because, in the buck converter, there is always a ripple current in the inductor $L_{\text{m}}$.

Second, we consider the process of switching off Q2 at moment $t_2$. To charge and discharge the $C_{\text{oss}}$ capacitances of Q1 and Q2, the condition $i_{\text{off,Q2}} \geq 0$ must also be met. The worst-case scenario for this condition is a small leakage inductance $L_{\text{leak}} \rightarrow 0$. In this case, the value of $i_{\text{off,Q2}}$ is equal to $-i_{\text{m}}(t_2)$. Thus, the conditions for ZVS and stable oscillations for switching off Q2 can be derived

$$i_{L_m}(t_2) < 0$$  \hfill (8)

Because $|i_{\text{m}}(t_2)| \leq |i_{\text{m}}(t_1)|$, the condition Equation (8) prevails for calculating the $L_{\text{m}}$ of the self-oscillating converter. Essentially, the physical ripples in the magnetising inductance must be large enough to turn off the Q2 switch while a positive current is flowing through the switch. For all outputs, the current $i_{\text{m}}$ is dependent on the magnetising inductance $L_{\text{m}}$ and the load condition. For a two-output fly-buck converter, the current $i_{L_m}(t_2)$ can be obtained as follows

$$i_{L_m}(t_2) = I_{\text{out1}} + I_{\text{out2}}N_{\text{sec}} - \frac{(V_{\text{in}} - V_{\text{out1}})}{2L_{\text{m}}}I_{\text{ON,Q1}}$$  \hfill (9)

where $I_{\text{out1}}$ is the steady state load current for the primary non-isolated output, and $I_{\text{out2}}$ is the steady state load current for the secondary isolated output. Time $t_{\text{ON,Q1}}$ is the on time of the Q1 switch, which is assumed to be fixed for the stabilisation method described in Section 3.5. Thus, the converter operates in a constant on-time mode. This offers some benefits, including good overload and short-circuit protection.

Using Equation (1) and (2), it is possible to modify Equation (9) as follows:

$$i_{L_m}(t_2) = \frac{I_{\text{out1}}V_{\text{out1}}}{V_{\text{out1}}} + \frac{I_{\text{out2}}V_{\text{out2}}}{V_{\text{out1}}} - \frac{(V_{\text{in}} - V_{\text{out1}})}{2L_{\text{m}}}I_{\text{ON,Q1}}$$  \hfill (10)

If the converter has $M$ number of outputs, Equation (10) can be generalised as follows:

$$i_{L_m}(t_2) = \sum_{i=1}^{M} I_{\text{out i}} \frac{V_{\text{out i}}}{V_{\text{out1}}} - \frac{(V_{\text{in}} - V_{\text{out1}})}{2L_{\text{m}}}I_{\text{ON,Q1}}$$  \hfill (11)

$$i_{L_m}(t_1) = \frac{P_{\text{tot}}}{V_{\text{out1}}} - \frac{(V_{\text{in}} - V_{\text{out1}})}{2L_{\text{m}}}I_{\text{ON,Q1}}$$  \hfill (12)

where $P_{\text{tot}}$ is the total output power of all primary and secondary outputs. Furthermore, a modified Equation (12) can be used to find the peak value of the magnetising inductance current for proper transformer design:

$$i_{L_m}(t_1) = \frac{P_{\text{tot}}}{V_{\text{out1}}} + \frac{(V_{\text{in}} - V_{\text{out1}})}{2L_{\text{m}}}I_{\text{ON,Q1}}$$  \hfill (13)

It can be seen from Equation (12) that the above expressions can be expanded not only for one isolated output but also for any multiple output configuration because there is no secondary voltage in the equation.
It is now possible to obtain the expression for the $L_{sw}$ condition that satisfies Equation (8)

$$L_{sw} < \frac{(V_{in} - V_{out1})V_{out1}}{2P_{tot}} t_{ON,Q1}$$  \hspace{1cm} (14)$$

Equation (14) can be used to determine the required minimum value for $L_{sw}$ inductance. This value guarantees that the current $i_{Q2}(t_2) > 0$ so that the voltage at node A increases before Q1 switches on. To limit the duration of the zero-voltage transition, the following equations can be used in place of Equations (8) and (14)

$$i_{sw}(t_2) < - \frac{2C_{oss}}{\tau_{tr}} V_{in}$$  \hspace{1cm} (15)$$

$$L_{sw} < \frac{(V_{in} - V_{out1})V_{out1}}{2P_{tot}} t_{ON,Q1} \left( \frac{2C_{oss} V_{in} V_{out1}}{P_{tot} \tau_{tr}} + 1 \right)$$  \hspace{1cm} (16)$$

where $C_{oss}$ is the output capacitance of the MOSFET switches, which can be found in the manufacturer’s datasheet. Parameter $\tau_{tr}$ is the required maximum voltage transition time at node A.

### 3.2 Gate drive windings

The additional windings, $L_{aux,Q1}$ and $L_{aux,Q2}$ (Figure 3), which provide positive feedback for the self-relaxation mode, should have the following features:

- The turn ratios with respect to the main inductor, $1 : N_{Q1}$ and $1 : N_{Q2}$, should be large enough to deliver voltage levels that reliably open switch Q1 and switch Q2. These voltages, $E_{1,Q1}$, $E_{2,Q1}$, $E_{1,Q2}$, and $E_{2,Q2}$ (Equation (3) and (4)), must exceed a specific level. In this case, the gate voltages reliably reach the $V_{zener}$ limit of the $D_{S2}$ diode for a wide range of converter input $V_{in}$ voltages and converter output $V_{out1}$ voltages. This also ensures that the switching frequency is predictable for all conditions and that there are no shot-through currents at the converter start up due to transients.
- The turn ratios $1 : N_{Q1}$ and $1 : N_{Q2}$ should not be too large to avoid high ohmic losses in the gate drive circuits.

The waveforms for the auxiliary windings and gate voltages are presented in Figure 4. It is assumed that the $V_{zener}$ and $V_{th}$ parameters are the same for the Q1 and Q2 channels. When one of the Q1 or Q2 switches turns on, the voltage at the gate must reach $V_{zener}$ in accordance with the conditions outlined earlier. The theoretical limit for this condition is when the threshold $V_{th}$ is close to $V_{zener}$. Voltage from the auxiliary windings reaching the gates of the switches passes through the resistive and capacitive dividers $R1/R2$ and $C1/C_{iss}$. Taking this into account, the condition for auxiliary winding voltages can be obtained as follows:

$$(E_{1,Q1} + E_{2,Q1}) \frac{R2_{Q1}}{R1_{Q1} + R2_{Q1}} \frac{C_{Q1}}{C_{Q1} + C_{iss}} \geq 2 V_{zener}$$  \hspace{1cm} (17)$$

$$(E_{1,Q2} + E_{2,Q2}) \frac{R2_{Q2}}{R1_{Q2} + R2_{Q2}} \frac{C_{Q2}}{C_{Q2} + C_{iss}} \geq 2 V_{zener}$$  \hspace{1cm} (18)$$

Using the corresponding values $E_{1,Q1}/Q2$ and $E_{2,Q1}/Q2$ from Equations (3) and (4), the conditions for the turn ratios can be derived:

$$N_{Q1} \geq \left( 1 + \frac{R1_{Q1}}{R2_{Q1}} \right) \left( 1 + \frac{C_{iss}}{C_{Q1}} \right) \frac{2 V_{zener}}{V_{in}}$$  \hspace{1cm} (19)$$

$$N_{Q2} \geq \left( 1 + \frac{R1_{Q2}}{R2_{Q2}} \right) \left( 1 + \frac{C_{iss}}{C_{Q2}} \right) \frac{2 V_{zener}}{V_{in}}$$  \hspace{1cm} (20)$$

It can be seen from Equations (19) and (20) that the turn ratios of the auxiliary windings must be calculated for the minimum input voltage, and they do not depend on other voltages or the duty cycle.

The turn ratios $1 : N_{Q1}$ and $1 : N_{Q2}$ defined by Equations (19) and (20) are minimum values that may be corrected due to the effect of the leakage inductance of the main transformer T1. In multi-winding transformers, the transformer model contains leakage inductances in series with each winding (T-model [15]). A schematic of the self-oscillating converter, with a full model of the transformer, is presented in Figure 5. In the model, the turn ratio $N_{sec2}$ represents the physical turn ratio of the transformer [15].

When the Q1 switch initially turns on, the leakage inductances $L_{leak,p}$ and $L_{leak,y}$ should be reset to zero current. Until they are reset, the voltage drop on $L_{leak,p}$ due to a high $di/dt$ can lower the voltages $E_{1,Q1}$ and $E_{2,Q2}$. The equivalent circuit during the reset of the leakage inductance is presented in Figure 6. The effects of the leakage inductance on the waveforms are shown in Figure 7.
In Figure 6, the Q2 switch has just been turned off, and the voltage at the node A rises from zero to $V_{in}$, but the secondary diode still conducts current. Thus, Equations (3) and (5) can now be corrected, assuming that $I_{\text{leak},p} \ll I_{\text{sec}} L_{\text{leak},S}/N_{\text{sec}}^2 \ll L_m$ and $V_{out2} \approx V_{out1} N_{\text{sec}}^2$.

$$E_{1, Q1} \approx \left( V_{in} \frac{I'_{\text{leak},S}}{L_{\text{leak},S}} - V_{out1} \right) N_{Q1}$$  \hspace{1cm} (21)$$

$$E_{2, Q2} \approx \left( V_{in} \frac{I'_{\text{leak},S}}{L_{\text{leak},S}} - V_{out1} \right) N_{Q2}$$  \hspace{1cm} (22)$$

where $I'_{\text{leak},S} = L_{\text{leak},S}/N_{\text{sec}}^2$. Equations (4) and (6) do not change.

For the Q1 switch to be turned on, the voltage at the gate must reach the $V_{th}$ threshold voltage. When the Q1 switch is turned on and the leakage inductance reset has been effected, the gate voltage increases to $V_{zener}$. Thus, Equations (17) and (18) must also be corrected:

$$\left( E_{1, Q1} + E_{2, Q1} \right) \frac{R_{2, Q1}}{R_{1, Q1} + R_{2, Q1}} \frac{C_{1, Q1}}{C_{1, Q1} + C_{\text{iss}}} \geq V_{zener} + V_{th}$$  \hspace{1cm} (23)$$

$$\left( E_{1, Q2} + E_{2, Q2} \right) \frac{R_{2, Q2}}{R_{1, Q2} + R_{2, Q2}} \frac{C_{1, Q2}}{C_{1, Q2} + C_{\text{iss}}} \geq V_{zener} + V_{th}$$  \hspace{1cm} (24)$$

Equations (19) and (20) can now be refined:

$$N_{Q1} \geq \left( 1 + \frac{R_{1, Q1}}{R_{2, Q1}} \right) \left( 1 + \frac{C_{\text{iss}}}{C_{1, Q1}} \right) \frac{V_{zener} + V_{th}}{V_{in}} \times \frac{I'_{\text{leak},S} + I_{\text{leak},p}}{I'_{\text{leak},S}}$$  \hspace{1cm} (25)$$

$$N_{Q2} \geq \left( 1 + \frac{R_{1, Q2}}{R_{2, Q2}} \right) \left( 1 + \frac{C_{\text{iss}}}{C_{1, Q2}} \right) \frac{V_{zener} + V_{th}}{V_{in}} \times \frac{I'_{\text{leak},S} + I_{\text{leak},p}}{I'_{\text{leak},S}}$$  \hspace{1cm} (26)$$

Thus, the final selection of turn ratios $1 : N_{Q1}$ and $1 : N_{Q2}$ should be the maximum value between Equations (19) and (25) and between Equations (20) and (26). The initial general recommendation is to choose the highest possible $V_{zener}$ voltage for the $D_{z1} - D_{z2}$ diodes. In this case, the turn ratios for the auxiliary windings should be sufficient for stable oscillations. Experimental corrections may be performed for these windings.

As can be seen from Equations (19), (20), (25) and (26), the recommended relation between resistances $R_1$ and $R_2$ can be obtained as follows:

$$R_{1, Q1} \ll R_{2, Q1} \hspace{1cm} R_{1, Q2} \ll R_{2, Q2}$$  \hspace{1cm} (27)$$

These conditions guarantee minimum turn ratios for $N_{Q1}$ and $N_{Q2}$ that are optimal for leakage inductance and losses in the gate drive circuits. These conditions are also consistent with
Switching frequency and duty cycle

low switching losses, for the reduction of which the lowest possible resistances R1,Q1 and R1,Q2 must be chosen. Another role of these resistors is limiting the current for charging and discharging capacitors C1,Q1 and C1,Q2. Therefore, the switching frequency and duty cycle are primarily determined by resistors R2,Q1 and R2,Q2 together with capacitors C1,Q1 and C1,Q2. The conditions for Equation (27) also make it possible to implement output voltage stabilisation by changing only one of the resistances (i.e. either R2,Q1 or R2,Q2), as demonstrated in Chapter 3.5.

The critical role of resistors R1,Q1 and R1,Q2 is to dampen the ringing caused by auxiliary winding leakage inductances \( L_{\text{leak,}Q1} \) and \( L_{\text{leak,}Q2} \) (Figure 5). Hence, resistance R1,Q1 and resistance R1,Q2 can be refined as follows:

\[
R_{1,Q1} = \sqrt{\frac{L_{\text{leak,}Q1}}{C_{\text{iss}}+C_{Q1}}}, \quad R_{1,Q2} = \sqrt{\frac{L_{\text{leak,}Q2}}{C_{\text{iss}}+C_{Q2}}} \quad (28)
\]

3.3 Switching frequency and duty cycle calculation

The gate voltage of switch Q1 and switch Q2 can be split into two intervals: \( t_{\text{zener,Q1}} \) and \( t_{\text{RC,Q1}} \) for the Q1 switch and \( t_{\text{zener,Q2}} \) and \( t_{\text{RC,Q2}} \) for the Q2 switch. The waveforms for the timing characteristic calculations are presented in Figure 4. The detailed gate drive RC circuit, including the gate input capacitance \( C_{\text{iss}} \), is shown in Figure 8.

The intervals \( t_{\text{zener,Q1}} \) and \( t_{\text{zener,Q2}} \) are periods during which voltages at the MOSFET gates are limited by the Zener diode voltage \( V_{\text{zener}} \), as described previously in Section 3.2.

The intervals \( t_{\text{RC,Q1}} \) and \( t_{\text{RC,Q2}} \) are relaxation times, during which voltages at the gates exponentially decays from \( V_{\text{zener}} \) voltage down to the MOSFET threshold voltage \( V_{\text{th}} \). Relaxation time constants for these processes are \( R2,Q1(C1,Q1+C_{\text{iss}}) \) and \( R2,Q2(C1,Q2+C_{\text{iss}}) \) for switch Q1 and switch Q2, respectively. For further derivations, conditions from Equation (27) are assumed.

If the turn ratios for the auxiliary windings have been chosen optimally, as outlined in Section 3.2 with Equation (19) and (20), the gate voltage only briefly remains at the \( V_{\text{zener}} \) limit. Thus, it is assumed that

\[
t_{\text{zener,Q1}} \ll t_{\text{RC,Q1}} \quad t_{\text{zener,Q2}} \ll t_{\text{RC,Q2}} \quad (29)
\]

Taking this into account, the on time for the MOSFETs Q1 and Q2 is predominantly determined by the time intervals \( t_{\text{RC,Q1}} \) and \( t_{\text{RC,Q2}} \)

\[
t_{\text{ON,Q1}} \approx t_{\text{RC,Q1}}, \quad t_{\text{ON,Q2}} \approx t_{\text{RC,Q2}} \quad (30)
\]

For these intervals, the voltage at the gates can be derived as the solution of a first-order differential equation. The general solution for such an equation is an exponential process with a constant relaxation time \( \tau \)

\[
V_{\text{gate}}(t) = A_1 + A_2 \exp \left( -\frac{t}{\tau} \right) \quad (31)
\]

The coefficients \( A_1 \) and \( A_2 \) can be derived from initial and infinity time conditions as \( A_1 = 0 \) and \( A_2 = V_{\text{zener}} \). Therefore, voltages at the gates for the intervals \( t_{\text{RC,Q1}} \) and \( t_{\text{RC,Q2}} \) can be obtained:

\[
V_{\text{gate,Q1}}(t) = V_{\text{zener}} \exp \left( -\frac{t}{R2,Q1(C1,Q1+C_{\text{iss}})} \right) \quad (32)
\]

\[
V_{\text{gate,Q2}}(t) = V_{\text{zener}} \exp \left( -\frac{t}{R2,Q2(C1,Q2+C_{\text{iss}})} \right) \quad (33)
\]

Knowing the threshold voltage \( V_{\text{th}} \), and taking into account Equation (30), the on time for the Q1 and Q2 switches can be obtained:

\[
t_{\text{ON,Q1}} \approx R2,Q1(C1,Q1+C_{\text{iss}}) \ln \left( \frac{V_{\text{zener}}}{V_{\text{th}}} \right) \quad (34)
\]

\[
t_{\text{ON,Q2}} \approx R2,Q2(C1,Q2+C_{\text{iss}}) \ln \left( \frac{V_{\text{zener}}}{V_{\text{th}}} \right) \quad (35)
\]

Now, the switching frequency and duty cycle can be derived:

\[
F_{\text{sw}} = \frac{1}{t_{\text{ON,Q1}} + t_{\text{ON,Q2}}} \approx \frac{1}{R2,Q1(C1,Q1+C_{\text{iss}}) + R2,Q2(C1,Q2+C_{\text{iss}})}
\]

\[
\times \left( \frac{1}{\ln \left( \frac{V_{\text{zener}}}{V_{\text{th}}} \right)} \right) \quad (36)
\]

\[
D = \frac{t_{\text{ON,Q1}}}{t_{\text{ON,Q1}} + t_{\text{ON,Q2}}} \approx \frac{1}{1 + \frac{R2,Q1(C1,Q1+C_{\text{iss}})}{R2,Q2(C1,Q2+C_{\text{iss}})}} \quad (37)
\]

The actual switching frequency will be less than the switching frequency calculated using Equation (36). This is due to the effect of resistors R1,Q1 and R1,Q2.

It is apparent that the switching frequency depends on the MOSFET gate-to-source threshold voltage \( V_{\text{th}} \) (Equation (36)). However, the duty cycle of the self-oscillating converter is not dependent on this parameter (Equation (37)).
output voltages are assumed to be stable from a long-term perspective.

3.4 Start-up circuit

As was mentioned in Chapter 2.1, unlike conventional half-bridge self-oscillating converters, the fly-buck converter cannot be started using the bottom switch Q2. This is because of the zero voltage during start up at the output $V_{out1}$ such that the $L_m$ inductor cannot be magnetised and zero potential is applied at node A (Figure 3). Accordingly, the start-up circuit must be modified. An example of such a circuit is presented in Figure 9.

The breakover voltage of the diac $D_{s1}$ $V_{diac} (V_{diac} < V_{in})$ and the values of $R_s$ and $C_s$ determine the converter start-up delay after the input voltage has been applied

$$t_{delay} = R_s C_s \ln \left( \frac{V_{in}}{V_{in} - V_{diac}} \right)$$  (38)

After the start-up process, when a pulsing voltage is applied to node A, the circuits $R_s$, $R_f$ and $Q_s$ reset the diac and keep it in this state while pulses are generated in node A. Thus, the following condition must also be satisfied to avoid activating the diac during normal operation:

$$t_{delay} \gg \frac{1}{f_{sw}}$$  (39)

Another limitation of the $R_s$ value is power dissipation within the resistance

$$P_{R_s} = \frac{V_{in}^2}{R_s}$$  (40)

The diac $D_{s1}$ can be replaced with an equivalent analogue circuit using two bipolar junction transistors (BJTs). An example of such a circuit is presented in Section 4.3.

For stable oscillations to be set, the duration of the $Q_s$ switch in state $t_{pulse}$ should be at least 5...10 switching periods, and it should be greater than the transient process period. The current pulse is injected in node A using resistor $R_{pulse}$. Voltage at the A node causes the Q1 switch to open initially for a determined on time $t_{ON,Q1}$ with the help of auxiliary winding $L_{aux,Q1}$. The current in inductance $L_m$ begins to rise from zero to a peak value $V_{in} L_m \frac{1}{t_{ON,Q1}}$. It is assumed that, at the beginning, the voltage on the primary output equals zero as a worst-case scenario: $V_{out1} = 0$. When the Q1 switch is turned off, the voltage at node A rapidly changes from $V_{in}$ to 0, so the Q2 switch reliably turns on with the help of auxiliary winding $L_{aux,Q2}$. For the second cycle of the Q1 switch turning on, the Q2 switch must turn off with a positive current flowing through it, similar to the condition described in Section 3.1. To satisfy this condition, the following inequalities can be obtained for the worst-case scenario at start up:

$$\frac{V_{in}}{R_{pulse}} \geq \frac{V_{in}}{I_{sw}} t_{ON,Q1}$$  (41)

Then, the maximum value of the resistor $R_{pulse}$ can be estimated:

$$R_{pulse} \leq \frac{I_{sw}}{t_{ON,Q1}}$$  (42)

This value is the initial resistance that guarantees the converter will be able to start at zero output power. The resistance $R_{pulse}$ and pulse duration $t_{pulse}$ also contribute to pre-charging the output $V_{out1}$, powering on switch Q2 during start up. However, a long $t_{pulse}$ time can cause output overshoot at converter start up. The resistance from Equation (42) must be tuned based on experimentation for the converter to start at the full range of voltages and loads.

Resistances $R_{s2} - R_{s3}, R_{s4} - R_{s5}$ and $R_{s6} - R_{s7}$ must be chosen for reliable opening and closing that correspond to transistors $Q_s1, Q_s2$ and $Q_s3$.

Pulse time $t_{pulse}$ is determined by the charge process of RC circuits $C_{s2}$ and $R_{s6} | R_{s7}$. Thus, capacitance $C_{s2}$ can be preliminarily estimated as follows:

$$C_{s2} = -\frac{(R_{s3} + R_{s2}) t_{pulse}}{R_{s2} R_{s3} ln \left( 1 - \frac{(R_{s3} + R_{s2}) V_{in}}{R_{s3} V_{BE}} \right)}$$  (43)

where $V_{BE} \approx 0.7$ V is the base-to-emitter voltage of BJT $Q_{s1}$.

3.5 Output voltage stabilisation

In most applications of the fly-buck converter, the primary output voltage $V_{out1}$ is stabilised. For the secondary voltages, the ratio from Equation (2) guarantees that the voltage $V_{out2}$ and others are also stabilised. This is one of the advantages of a fly-buck converter [4, 5, 8]. $V_{out1}$ voltage...
stabilisation can be implemented for the proposed self-oscillating converter.

Per Equations (34), (35) and (37), the duty cycle can be controlled in different ways. Changing one of the following parameters alters the duty cycle: $C_{Q_1}, C_{Q_2}, R_{2Q_1}$ and $R_{2Q_2}$. One of the simplest solutions (Figure 10) is based on equivalent $\mathcal{R}_2Q_2$ control and the gate control of switch $Q_2$, using the primary ground as a reference. This approach simplifies the circuit design and reduces the number of components required compared to other solutions. As shown in Figure 10, the circuit of the additional resistor $R_{3Q_2}$ and voltage source $V_{ctrl}$ is placed in parallel with resistor $R_{2Q_2}$. The voltage source $V_{ctrl}$ represents the output error amplifier of the feedback control circuit.

The gate voltage of the Q2 MOSFET can still be derived as a solution for a first-order differential equation, similar to Equation (31). Using the initial conditions, Equation (33), with respect to the voltage at the gate of Q2, can be modified as follows:

$$V_{gate,Q2}(t)$$

$$= V_{ctrl} \frac{R'_{2Q_2}}{R_{2Q_2} + R_{3Q_2}} + \left( V_{zener} - V_{ctrl} \frac{R'_{2Q_2}}{R_{2Q_2} + R_{3Q_2}} \right)$$

$$\times \exp \left( \frac{-t}{(C_{Q_2} + C_{iss}) \left( \frac{R_{2Q_2}R_{3Q_2}}{R_{2Q_2} + R_{3Q_2}} \right)} \right)$$

Now, the turn on time for the Q2 switch can be derived:

$$t_{ON,Q2} \approx \left( C_{Q_2} + C_{iss} \right) \left( \frac{R'_{2Q_2}R_{3Q_2}}{R_{2Q_2} + R_{3Q_2}} \right)$$

$$\times \ln \left( \frac{V_{zener} - V_{ctrl} \frac{R'_{2Q_2}}{R_{2Q_2} + R_{3Q_2}}}{V_{th} - V_{ctrl} \frac{R'_{2Q_2}}{R_{2Q_2} + R_{3Q_2}}} \right)$$

Analysing Equation (45), it is apparent that increasing $V_{ctrl}$ will cause an increase in the turn on time for the Q2 switch and a decrease in the duty cycle and output voltages. The following rationale facilitates determination of the $R_{3Q_2}$ value.

For practical application, when the relative change in the input voltage $\gamma = \frac{\Delta V_{in}}{V_{in}}$ is small, it is possible to choose a $R_{3Q_2}$ resistor with the following conditions:

$$\gamma \ll 1, \quad R_{3Q_2} \gg R_{2Q_2}$$

Using the equation for exact differentials, it is possible to derive for a function $f(x)$

$$\Delta f = \frac{\partial f}{\partial x} \Delta x$$

From Equation (47), the following requirements for variations in the turn on time for the Q2 switch can be obtained:

$$\gamma = \frac{\Delta V_{in}}{V_{in}} = \frac{\Delta D}{D} = (1 - D) \frac{\Delta t_{ON,Q2}}{t_{ON,Q2}}$$

$$\frac{\Delta t_{ON,Q2}}{t_{ON,Q2}} = \frac{\gamma}{1 - D} = \frac{\Delta V_{in}}{V_{in} - V_{out1}}$$

where $\Delta V_{in}$ is the variation in the input voltage compared to that in nominal conditions. Similarly, $\Delta D$ is the variation in the duty cycle, and $\Delta t_{ON,Q2}$ is the variation in the Q2 turn on time from the turn on time under nominal conditions.

Equation (45) can be rewritten in a shorter form as

$$f(x) = k \ln \left( \frac{a - x}{b - x} \right)$$

where

$$k = \left( C_{Q_2} + C_{iss} \right) \left( \frac{R'_{2Q_2}R_{3Q_2}}{R_{2Q_2} + R_{3Q_2}} \right)$$

$$a = V_{zener}$$

$$b = V_{th}$$

$$x = V_{ctrl} \frac{R'_{2Q_2}}{R_{2Q_2} + R_{3Q_2}}$$

From Equations (47) and (50)

$$\frac{\Delta f}{f} = \left( \frac{1}{b - x} - \frac{1}{a - x} \right) \frac{\Delta x}{\ln \left( \frac{x}{b - x} \right)}$$
From the assumption Equation (46), it is possible to assume that $a \gg x$ and $b \gg x$. Now, Equation (55) can be simplified as follows:

$$\Delta f \approx \left( \frac{1}{b} - \frac{1}{a} \right) \frac{\Delta x}{\ln \left( \frac{z}{b} \right)}$$  \hspace{1cm} (56)

This makes it possible to write the following expression for the relative variation in $Q_2$ turn on time:

$$\frac{\Delta t_{\text{ON},Q_2}}{t_{\text{ON},Q_2}} \approx \left( \frac{1}{V_{\text{th}} - V_{\text{zener}}} \right) \frac{1}{\ln \left( \frac{V_{\text{zener}}}{V_{\text{th}}} \right)} \times \left( \frac{\Delta V_{\text{ctrl}}}{R_2^{Q_2} + R_3^{Q_2}} \right),$$  \hspace{1cm} (57)

and using Equation (49), the relation between the resistors can be derived:

$$\frac{R_3^{Q_2}}{R_2^{Q_2}} \approx \left[ \frac{\Delta V_{\text{ctrl}}(V_{\text{in}} - V_{\text{out}})}{\Delta V_{\text{in}}} \right] \times \left( \frac{1}{V_{\text{th}} - V_{\text{zener}}} \right) \frac{1}{\ln \left( \frac{V_{\text{zener}}}{V_{\text{th}}} \right)} - 1,$$  \hspace{1cm} (58)

where $\Delta V_{\text{ctrl}}$ is the full voltage range of the control voltage $V_{\text{ctrl}}$.

It should be noted that the resistor $R_2^{Q_2}$ shown in Figure 10 is now different from the resistor $R_2^{Q_2}$ in Figure 3. To compare Equations (35) and (45), the relation

$$R_2^{Q_2} = \frac{R_2^{Q_2} R_3^{Q_2}}{R_2^{Q_2} + R_3^{Q_2}}$$  \hspace{1cm} (59)

can be obtained from the relaxation time, from a constant point of view. This will impact the design procedure described in Section 4.2.

Because the converter operates in a constant on time mode, the switching frequency is highest at the minimum input voltage. Thus the switching frequency increases when the input voltage rises.

### 4 | EXPERIMENT

#### 4.1 | Converter specifications

The converter specifications and parameters are presented in Table 1. This converter has three isolated outputs, with a total output power of 20 W. The output voltages are chosen in a manner that demonstrates the unsymmetrical operation of the switches $Q_1$ and $Q_2$ such that the duty cycle is $\approx 20\%$.

Before the prototype tests, the proposed self-oscillating converter was optimised for efficiency via simulation. The switching frequency can be optimised, and the SPICE simulation results are presented in the following figure:

Thus, a switching frequency of 50 kHz was adopted for the converters.

Components can also be selected for the self-oscillating converter in a more optimal manner. For example, ZVS conditions are naturally satisfied for $Q_1$ and $Q_2$ of the self-oscillating converter. However, for the $Q_1$ MOSFET, the turn off switching losses become dominant, as is apparent in the SPICE simulation on Figure 12. This means that the $Q_1$ MOSFET can be selected from cheaper alternatives with the same value as the merit parameter $R_{\text{on}} \cdot Q_{\text{tot}}$ but with a higher $R_{\text{on}}$ resistance than required for a conventional converter. IRF9956 MOSFETS were chosen for the $Q_1$ and $Q_2$ switches instead of the FDS8949 MOSFET typically used in a conventional converter.

| Parameter | Value |
|-----------|-------|
| Input voltage range, $V_{\text{in}}$ | 24.0 V ±10% |
| Output voltages and currents |
| $V_{\text{out}1}, I_{\text{out}1}$ | 5.0 V, 2.0 A |
| $V_{\text{out}2}, I_{\text{out}2}$ | 10.0 V, 0.5 A |
| $V_{\text{out}3}, I_{\text{out}3}$ | 10.0 V, 0.5 A |
| $V_{\text{out}4}, I_{\text{out}4}$ | 5.0 V, 0.05 A |
| Total output power, $P_{\text{tot}}$ | 20.0 W |
| Switching frequency, $F_{\text{sw}}$ | 50 kHz |
| MOSFETs $Q_1/Q_2$ output capacitance, $C_{\text{oss}}$ | 100 pF |
| MOSFETs $Q_1/Q_2$ gate input capacitance, $C_{\text{iss}}$ | 200 pF |
| Transition time at node $A$, $\tau_{\text{tr}}$ | 100 ns |
| Error amplifier output voltage range, $\Delta V_{\text{ctrl}}$ | 22.0 V |
| $D_{\text{z1}}-D_{\text{z2}}$ Zener voltage, $V_{\text{zener}}$ | 16.0 V |
| Threshold voltage of MOSFETs $Q_1/Q_2$, $V_{\text{th}}$ | 2.4 V |
| Delay time for the converter to start up, $t_{\text{delay}}$ | 10 ms |
| Duration of start-up pulse at node $A$, $t_{\text{pulse}}$ | 100 $\mu$s |
| Efficiency, $\eta$ | $\approx 0.9$ |
The following steps constitute the design procedure for the prototype specified in Table 1. It is assumed that the windings for secondary voltages are determined using Equation (2). The design procedure focuses on specific self-oscillation parameter calculations. All parameters must be calculated for minimum input voltage $V_{in,min}$.

1) **Calculation for constant on time for the Q1 switch**: For the selected switching frequency, the on time for the Q1 switch must be calculated for the minimum input voltage

$$t_{ON,Q1} = \frac{1}{F_{sw}} \frac{V_{out1}}{V'_{in,min}}$$  \hspace{1cm} (60)

which yields $t_{ON,Q1} = 4.6 \mu s$.

2) **Magnetising inductance selection**: Magnetising inductance $L_{sw}$ must be calculated for the minimum input voltage using Equation (16). The total power should include the total loss and be corrected using the estimated efficiency $\eta$: $(P_{in}/\eta)$, yielding

$$L_{sw} \leq 8.26 \mu H.$$  

3) **Gate resistor selection**: Resistors $R_{1,Q1}$ and $R_{1,Q2}$ are gate drive resistors, which determine the switching losses. It is recommended that they be $\leq 200 \, \Omega$. Thus, the following gate resistors can be adopted initially:

$$R_{1,Q1} = 22 \, \Omega, \quad R_{1,Q2} = 22 \, \Omega.$$  

These values may be corrected using Equation (42) in the experimental and tuning steps.

Resistors $R_{2,Q1}$ and $R_{2,Q2}$ in the worst-case scenario, have a square voltage with a peak voltage of $\pm V_{zener}$ (Figure 4). Thus, the lower limit for these resistances is determined by the power dissipation on $V_{zener}^2/R_{2,Q1}$ and $V_{zener}^2/R_{2,Q2}$. For general consideration, the lower $R_{2,Q1}$ and $R_{2,Q2}$, the higher $C_{1,Q1}$ and $C_{1,Q2}$ and the less the time characteristics are dependent on the $C_{iss}$ MOSFET parameter. Thus, for the 1206 case types, these values can be adopted:

$$R_{2,Q1} = 3.3 \, k\Omega, \quad R_{2,Q2} = 3.3 \, k\Omega.$$  

4) **Timing capacitor selection**: Capacitances $C_{1,Q1}$ and $C_{1,Q2}$ can be calculated by solving the system of Equations (1), (36) and (37), which yields

$$C_{1,Q1} = 540 \, pF, \quad C_{1,Q2} = 2.26 \, nF.$$  

5) **Additional windings turn ratio selection**: The turn ratios for auxiliary windings 1 : $N_{Q1}$ and 1 : $N_{Q2}$ must be calculated for the minimum input voltage. Equations (19) and (20) can be used initially, yielding

$$N_{Q1} = 2.09, \quad N_{Q2} = 1.66.$$  

The turn ratios can be calculated using Equations (25) and (26) if the transformer T1 can be measured for leakage inductance.

6) **Voltage stabilisation component selection**: If voltage stabilisation is required, the value $R_{2,Q2}$ should be corrected, and the resistor $R_{2,Q2}$ will transform to the $R'_{2,Q2}$, $R_{3,Q2}$, $V_{diac}$ circuit (Figure 10). Resistances $R'_{2,Q2}$, $R_{3,Q2}$ can be calculated by solving the system of Equations (58) and (59), which yields

$$R'_{2,Q2} = 3.4 \, k\Omega, \quad R_{3,Q2} = 113.2 \, k\Omega.$$  

7) **Start-up circuit calculations** (Figure 9): The system of Equations (38)–(40) must be solved to find $R_{tl}$ and $C_{tl}$. Choosing $V_{diac} \approx \frac{1}{2} V_{in}$ and losses for the $R_{1,Q1}$ resistor $P_{R1,Q1} = 0.025 \, W$ gives the following parameters:

$$V_{diac} = 12 \, V,$$

$$R_{1,Q1} = 18.7 \, k\Omega, \quad C_{1,Q1} = 77.3 \, nF.$$  

Resistance $R_{pulse}$ can be found using Equations (60) and (42):

$$R_{pulse} = 1.78 \, \Omega.$$  

The resistance $R_{pulse}$ must be tuned experimentally for the converter to start at the full range of voltages and load ranges. The $R_{pulse}$ resistor and switch Qs3 must withstand the short peak current $V_{in}/R_{pulse}$ at time $t_{pulse}$. If resistances $R_{2,Q1} = 10 \, k\Omega$ and $R_{2,Q2} = 10 \, k\Omega$ are selected, the capacitance $C_{s2}$ can be estimated using Equation (43):

$$C_{s2} = 298 \, nF.$$
It should be noted that the calculations in the procedure listed above and in Section 3 assume that the switches Q1 and Q2 and the diodes are ideal devices. For real components, the calculated characteristics may be different, and experimental tuning and modification of the converter might be required. The main correction will be for the $R_{Q2}$ value because of the assumptions made in Equations (56) and (57). The actual range of the control voltages $\Delta V_{ctrl}$ may be large and comparable to the input voltages, as in the example in Table 1.

Thus, the proposed design procedure can be used for any number of secondary outputs because neither equation includes a secondary voltage and only total output power matters.

### 4.3 Experimental data

A prototype of the self-oscillating converter with the characteristics listed in Table 1 has been constructed and compared with a conventional fly-buck converter based on the LTC3891 controller [9]. The full schematic diagram of the self-oscillating converter prototype is presented in Figure 13. The schematic includes all modifications in comparison with the values calculated above. The schematics for both converters can also be found in the supplemental active media. A picture of the prototype, with both converters mounted, is shown in Figure 14. Both converters have the same main power components, which are listed in Table 2. For the self-oscillating converter, the manufactured transformer T1 has been modified with additional windings, and the gap has been adjusted for the calculated $L_{m}$. For the converter based on the LTC3891 controller, the transformer has been altered, and it had a magnetising inductance of $L_{m} = 18.75 \mu H$.

![FIGURE 13](image1.png)

**FIGURE 13** Full schematic of the self-oscillating converter prototype

![FIGURE 14](image2.png)

**FIGURE 14** Prototype board with two converters populated: The top portion of the PCB is occupied by a conventional fly-buck converter, and the self-oscillating converter is placed on the bottom portion of the PCB

A conventional fly-buck converter based on the PWM controller would have more intelligent functionality, but many applications do not require a controller with such complex functionality. Self-oscillating fly-buck converters can be easily implemented with over-current protection using resettable fuses (polyfuses), which cost less than 0.1$ on the market. For

### Table 2 Main power components for conventional and self-oscillating converters

| Component          | Part number                                      |
|--------------------|--------------------------------------------------|
| $Q1$ and $Q2$ switches | FDS8949 (conventional)/ IRF9956 (self-oscillating) |
| Transformer T1      | ER28/14, Würth Elektronik 750811248              |
| Secondary side diodes | MBRS1100                        |
FIGURE 15  Waveforms of the gate voltage of the Q1 switch (CH2-blue), gate voltage of the Q2 switch (CH1-yellow) and voltage at the node A (CH3-magenta); $V_{in} = 21.6 \, V$

example, a component such as the 0ZCG0110FF2C from Bel Fuse can be used.

Waveforms at the gate signal of the MOSFETs Q1 and Q2, along with voltage at the node A, are presented in Figure 15–17 for different input voltages at full power.

A comparison of losses for the conventional and self-oscillating converters can be found in Figure 18. A comparison was performed after the EMI and common mode current spectrum were equalised for both converters by tuning the conventional converter. The self-oscillating converter has a lower efficiency, which is higher than 85%. This can be explained by the higher ripple current in the $L_{m}$ inductance and the Q1 and Q2 switches. This also can be seen in the full and no-load loss comparison. For the self-oscillating converter, the loss difference is relatively small.

Additionally, active losses are increased due to the gate voltage decaying to the MOSFET threshold voltage, and the on-resistance of the transistor becomes higher when the gate voltage approaches the threshold voltage. Active and switching losses may be decreased by implementing a gate driver IC between the RC circuit and the gate, but this solution will complicate the design and increase the cost of the converter. The gate driver IC requires a floating power supply. Depending on the application, it is still possible to implement such a solution. If the resistive load at the $V_{out1}$ output is always connected, the bootstrap circuit can be used [16].

There are differences in the values for some of the components corrected during prototype tuning. The following tuning steps were performed:

1) The resistances $R_{1Q1}$ and $R_{1Q2}$ were tuned to dampen the ringing caused by leakage inductances $L_{leak,Q1}$ and $L_{leak,Q2}$ (Figure 5).
2) The capacitance $C_{1Q1}$ was tuned to achieve the necessary $t_{ON,Q1}$ (Equation (60)).
3) The resistance $R_{2Q2}$ was tuned to achieve the required $V_{out1}$ voltage at the minimum input voltage $V_{in,min}$.
4) The resistance $R_{3Q2}$ was tuned to achieve the required $V_{out1}$ voltage for the full range of input voltages $V_{in} \pm \Delta V_{in}$.
5) The resistance $R_{pulse}$ was tuned for the converter to start up with the full range of loads.

The start up of the self-oscillating converter process is illustrated in Figure 19. As can be seen, there is a voltage overshoot at the $V_{out1}$ output at the beginning of the start-up process. This overshoot is caused by the initial current pulse through the resistor $R_{pulse}$. This current pulse charges the output capacitance on the output $V_{out1}$.

As in Figure 20, to improve emissions, for the conventional fly-buck converter, it was necessary to increase the gate resistances and additionally implement drain-source RCD snubbers to slow down $dV/dt$ and $dI/dt$. Thus, a comparison was performed after EMI and common mode current spectrum were equalised for both converters. This increased the power loss for the conventional converter; ultimately, the losses are comparable for both converters after all final optimisation and tuning (Figure 18).
A cost comparison and lifespan analysis can also be performed for conventional and self-oscillating converters. The cost comparison is based on the octopart.com resource and is presented in Figure 3. It was assumed that the transformer T1 has a price that is 10% higher for the self-oscillating converter. Thus, the cost difference is approximately equivalent to the price of the IC LTC3891.

The lifespan analysis was performed for conventional and self-oscillating converters using a method from the MIL-HDBK-217F NOTICE 2 reference [17]. The result is presented in Table 3. The increased ripple current and temperature for some of the components of the self-oscillating converter can increase the failure rate. However, for the conventional converter, there is an increased failure rate due to the high number of transistors and gates in the IC controller, in accordance with MIL-HDBK-217F NOTICE 2. Thus, the lifespan analysis shows that using the self-oscillating circuit and eliminating the IC controller could potentially increase the lifespan of the converter.

The following recommendations can be offered for improving converter characteristics. Based on the analysis and equations given in the paper, efficiency could be improved in the following ways:

- The MOSFETs must have the lowest possible gate capacitance $C_{iss}$. This will make it possible to use higher resistances in gate circuits, thus reducing losses.
- The switching frequency should be as low as possible and below 100 kHz. This will reduce switching losses in MOSFETs and in the transformer.
- The additional windings $L_{aux,Q1}$ and $L_{aux,Q2}$ for the main transformer should have good magnetic coupling to the primary winding. This will reduce turn ratios $1 : N_{Q1}$ and $1 : N_{Q2}$, so the losses in the gate circuits will be less; see Equations (25) and (26).
- Overshoot on the primary output can be reduced or even totally compensated by increasing the output capacitance $C_L1$ at this output.

The performance comparison of the presented converters is shown in Table 4.
5 | CONCLUSION

This study presents a self-oscillating fly-buck converter. The research focuses on the converter operation and presents the design procedure for self-oscillating-related components. Oscillations are created through positive feedback using additional auxiliary windings of the modified main transformer. A self-relaxation mode is provided by the relaxation of RC circuits, which turn off the switches and regulate the timing characteristics.

The following are the results and conclusions of this study:

- The self-oscillating fly-buck converter is presented. The proposed converter can operate at duty cycles other than 50%; around 20% in the presented prototype.
- Equations and a calculation procedure were developed for the proposed converter. Turn ratios for the windings have been estimated, and criteria for the stable oscillation mode have been developed. A switching frequency formula is also provided.
- The presented design procedure can be used for any number of secondary outputs because neither equation includes the secondary voltage, and only the total output power is important.
- ZVS conditions are calculated and can be used for conventional fly-buck converter calculations.
- Start-up and voltage stabilisation circuits are proposed and calculated.
- The proposed converter can also be used as a self-oscillating buck converter because the buck converter can be considered as a specific case of the fly-buck converter.
- Equations from the paper may also be used for other topologies based on the half-bridge self-oscillating circuit.
- The Maxima software code for automated calculation of the converter is also supplied as supplemental active content.

The proposed converter was compared with the conventional fly-buck converter. For this comparison, the self-oscillating converter was optimised for efficiency to demonstrate the control circuits and self-relaxation mechanism.

The proposed self-oscillating circuit demonstrated an efficiency higher than > 85% at 20 W of output power.

The cost difference between conventional converters and the proposed converter is equivalent to the cost of a PWM controller IC; thus, the goal of the research was achieved.

This study is supplemented with active media files, including a Maxima calculation file and schematics of the converters.

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SUPPORTING INFORMATION
Additional supporting information may be found online in the Supporting Information section at the end of the article.

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