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Abstract. 65-nm CMOS element of matching for content-addressable memory resilient to impact of single nuclear particles is proposed. Element includes upset-hardened STG DICE memory cell and XOR logical gate based on two tristate inverters. Transistors of the element are separated into two identical joint groups spaced on the chip by distance of more than 4 µm, which practically excludes the possibility of cell upset under impact of single nuclear particles. Designed element of matching is implemented in resilient to single event effects translation lookaside buffer of microprocessor.

1. Introduction

Content-addressable memory (CAM) [1] is used for parallel high performance processing of data streams. Elements of matching for content-addressable memory are conventionally designed on base of CMOS 6-transistor (6T) memory cells, which have increased sensitivity to the effects of single nuclear particles impact [2]. For today, there are a few upset-resilient designs of ternary content-addressable memory [3]-[4], however, they were not used in practice.

Fault-tolerant DICE (Dual Interlocked Cell) memory cells [5] were an effective decision, but with the technology scaling to 65 nm and less, they lost their advantages over 6T cells because of decreasing of distance between mutually sensitive nodes of the cell [6]. In STG DICE (Spaced Transistor Groups DICE) memory cells [7] the transistors are separated into two groups that are spaced on the chip, so the impact of single nuclear particle on only one group does not lead to a failure of the cell [8]. Device simulation results [9] and experimental results [7] proved an increased tolerance of STG DICE memory cells to single event effects compared to 6T and traditional DICE memory cells. In this work, the design of the element of matching for content-addressable memory based on STG DICE memory cell is proposed [10].

2. Structure of the element of matching

Element of matching includes STG DICE memory cell and the logical gate “Exclusive OR” (XOR), which consists of two tristate inverters TRInv 1 and TRInv 2. Figure 1 presents the scheme of the element of matching. Element of matching stores one bit of information and compare the stored bit with the sequence of bits from Input 1 and Input 2. Input 1 provides data in normal form, and Input 2 provides data in inverse form.

Bit of data is written to the STG DICE memory cell that have two steady states: ABCD = 0101 (storing of logical “0”) and ABCD = 1010 (storing of logical “1”). If a single nuclear particle impacts on only one group of STG DICE, the cell does not upsets, but only goes to one of the unsteady states:
ABCD = 1100, ABCD = 0011, ABCD = 1001, ABCD = 0110. The unsteady state of STG DICE is temporary, and the cell returns to its previous steady state after finishing of all transients.

Comparison of information bits is produced by the XOR gate. Output state of XOR gate is determined by the logical function:

$$Y_{\text{OUT}} = X_{\text{IN}1} \cdot X_{\text{AC}} + X_{\text{IN}2} \cdot X_{\text{BD}},$$

where $X_{\text{AC}} = X_A = X_C$ is the logical levels on the nodes A and C that are the same in steady state of STG DICE, $X_{\text{BD}} = X_B = X_D$ is the logical levels on the nodes B and D that are the same in steady state of STG DICE, $X_{\text{IN}1}$ is the normal logical level of input bit on Input 1; $X_{\text{IN}2} = nX_{\text{IN}1}$ is the inverse logical level of input bit on Input 2; $Y_{\text{OUT}}$ is the output logical level of XOR gate.

Transistors of element of matching are separated into two joint groups, every joint group includes one group of STG DICE memory cell and one tristate inverter (a half of XOR gate).

Figure 1. Schematic of element of matching based on STG DICE memory cell and XOR gate on two tristate inverters TRInv 1 and TRInv 2.

Transistors of element of matching are separated into two joint groups, every joint group includes one group of STG DICE memory cell and one tristate inverter (a half of XOR gate). Single nuclear particle impact on the transistors of XOR gate induces the noise pulse on the output of XOR [11]. Impact of particle with linear energy transfer on its track up to 40 MeV·cm²/mg can be simulated with

Figure 2. Node voltages of element of matching depending on time under the impact of current pulse on the output of element: (a) in steady state ABCD = 1010 of STG DICE; (b) in temporary unsteady state ABCD = 0011 of STG DICE. States of inputs: Input 1 = “1”, Input 2 = “0”.

\[a\]
the double-exponential current pulse [2] on the output of XOR gate. Figure 2a presents the output voltage of XOR depending on time under the impact of current pulse with rise time constant $\tau_R = 5$ ps and fall time constant $\tau_F = 50$ ps in steady state of STG DICE.

When transistors of one group of STG DICE collect an induced charge, the cell goes to the unsteady state, and the output of XOR gate goes to the high-impedance state or to the state with low-level output voltage $b \cdot V_{DD}$ [12]. Figure 2b presents the node voltages of element of matching depending on time when STG DICE goes to the unsteady state $ABCD = 0011$. Output voltage of element of matching takes on value $b \cdot V_{DD} = 170$ mV (dashed curve on figure 2b).

Placing the transistors of tristate inverter with the transistors of STG DICE group on the chip together in one joint group creates a possibility of simultaneous impact of induced charge on these transistors. In this case, the compensation of output noise pulse is possible. The output voltage of element of matching depending on time under the impact of current pulse on the output of element in unsteady state of the cell $ABCD = 0011$ is shown on figure 2b with the green curve. Simultaneous charge collecting by the transistors of STG DICE group and transistors of tristate inverter may lead to decreasing of output noise pulse amplitude.

3. Topology of the element of matching

Transistors of the element of matching are separated into two identical joint groups spaced on the chip. Basic variant of topology of two elements of matching is presented in figure 3. On the chip, area between two joint groups of every element is filled by one joint group of another neighboring element. This interleaving provides the distance between mutually sensitive nodes of every element of matching of more than 4 $\mu$m with minimum area overhead. The shaded areas on figure 3 are the drains of closed transistors of STG DICE memory cell in steady state $ABCD = 1010$.

Table 1 presents the parameters of element of matching designed with 65 nm CMOS technology, where $H_{J.G}$ and $W_{J.G}$ are the height and width of the joined group; $N_{TR}$ is the number of transistors in the joint group; $I_{OUT.LEAK}$ is the leakage current of the output of tristate inverter; $t_{DEL}$ is the delay of XOR gate output signal at the load capacitance of 2 fF. Table 2 presents the values of distances between mutually sensitive nodes of STG DICE memory cell in state $ABCD = 1010$. In inverse logical state $ABCD = 0101$ another couples of transistors are sensitive to particle impact, but the values of distances between them are the same. The interleaving of joint groups of neighboring elements provides the distance between mutually sensitive nodes of every element of more than 4 $\mu$m. It makes the element of matching resilient to impacts of single nuclear particles with linear energy transfer on its track up to 70 MeV-cm²/mg [11]. Guardian rings are placed along the boundary of p-bulk and n-well for protection against latch-up effect. Common for this technology parameters of topology are: the depth of p-bulk is 3 $\mu$m, p-bulk doping concentration is $10^{16}$ cm⁻³, device layers are Gaussian
doped with peak concentration of $2 \times 10^{18}$ cm$^{-3}$ on the 0.65 µm depth with boron for NMOS transistor and with arsenic for PMOS transistors in n-well.

**Table 1.** Parameters of one joint group of element of matching

| Parameter      | Value |
|----------------|-------|
| $N_{TR}$       | 10    |
| $W_{JG}$ (µm)  | 2.4   |
| $H_{JG}$ (µm)  | 2.45  |
| $I_{OUT\,LEAK}$ (pA) | 30-33 |
| $t_{DEL}$ (ps) | 20-25 |

**Table 2.** Distances between mutually sensitive transistors of STG DICE memory cell.

| Pair of transistors | Distance (µm) |
|---------------------|---------------|
| $N_A$–$N_C$         | 4.55          |
| $P_B$–$P_D$         | 4.55          |
| $P_B$–$N_C$         | 4.15          |
| $N_A$–$P_D$         | 5.15          |

### 4. Implementation in translation lookaside buffer

Presented element of matching is implemented in content-addressable memory block of translation lookaside buffer (TLB) of microprocessor [13]. Floorplan of designed TLB is presented in figure 4. The main functional blocks of TLB are: block of content-addressable memory (CAM), block of random access memory (RAM), block of read and write buffers (R/W BUF), block of input address decoder (DEC), block of output address encoder (ENCOD) and block providing control and synchronization signals (CONTROL). In presented TLB, capacity of CAM block is 64×47 bit and capacity of RAM block is 64×59 bit.

Table 3 presents the parameters of content-addressable memory block designed on base of proposed element of matching. Here H is the height of the block, W is the width of the block, S is the area of the block, $N_{TR}$ is the number of transistors in the block, $V_{DD}$ is the supply voltage, $F_{CLK}$ is the frequency of clock signal, $P_{WRITE}$, $P_{SEARCH}$, $P_{READ}$ are the power consumptions in write, search and read modes. Figure-of-merit (FOM) is the energy consumed in average by one bit of CAM block in one search operation.

**Table 3.** Parameters of CAM block of translation lookaside buffer.

| Parameter                  | Value           |
|----------------------------|-----------------|
| Capacity (bit)             | 64×47           |
| $H\times W$ (µm×µm)        | 303×158         |
| $S$ (mm$^2$)               | 0.048           |
| $N_{TR}$                   | 75136           |
| $V_{DD}$ (V)               | 1               |
| $F_{CLK}$ (GHz)            | 1               |
| $P_{WRITE}$ (mW)           | 17.9            |
| $P_{SEARCH}$ (mW)          | 27.5            |
| $P_{READ}$ (mW)            | 1.2             |
| **FOM** (fJ/bit/search)    | 12.6            |
5. Conclusion
The design of 65-nm CMOS element of matching for content-addressable memory based on upset-hardened STG DICE memory cell is proposed. Transistors of the element are separated into two identical joint groups, and interleaving of joint groups of neighboring elements provides spacing of STG DICE mutually sensitive nodes on the chip by distance of more than 4 µm. Proposed element of matching is implemented in translation lookaside buffer resilient to single event effects. Proposed design is promising for microprocessor systems with increased resistance to impacts of single nuclear particles.

6. References
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