Ultra-low-voltage-triggered Silicon Controlled Rectifier (ULVTSCR) ESD Protection Device for 1.2V/1.8V Application

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Abstract

High trigger voltage ($V_{t1}$) characteristic of silicon-controlled rectifier (SCR) device has limited its application in electrostatic discharge (ESD) protection of low voltage circuit, especially in advanced CMOS technologies. In this letter, an ultra-low-voltage-triggered SCR (ULVTSCR) is proposed to decrease the trigger voltage of the conventional SCR. The proposed device consists of an external NMOSs-string (ENMOSs-string), an internal NMOS (INMOS) with its gate controlled by the ENMOSs-string, and a main SCR triggered with the INMOS assistance. The ESD current-voltage characteristics of ULVTSCR has been measured with the transmission line pulsing (TLP) tester. The test results indicate that the proposed ULVTSCR possesses much lower $V_{t1}$ of ~ 5.03V as well as reduced area consumption compared to the existing optimization methods, making it highly suitable for the ESD protection for 1.2V/1.8V IO ports in CMOS technology. In addition, the impact of various critical dimensions of ULVTSCR have also been evaluated to further improve the ESD characteristics.

Background

Miniaturization of the CMOS technology makes it more difficult to provide electrostatic discharge (ESD) protection for integrated circuits (IC) due to the lower supply voltage and thinner gate oxide [1]. Grounded-gate NMOS (GGNMOS), one of the most commonly used ESD protection device in CMOS processes, is no longer attractive in advanced CMOS technologies because of its high trigger character and insufficient robustness [2–4]. A lateral silicon-controlled rectifier (LSCR) device can sustain a higher current with benefit from the strongly feedback effective between its parasitic n-p-n and p-n-p transistors. But the conventional LSCR device also has a higher trigger voltage ($V_{t1}$) and a deep snap-back I-V characteristic, which can not satisfy most of the ESD design widows. Thus, various designs have been proposed to improve the triggering characteristic of the LSCR [5, 6], such as the Modified Lateral SCR (MLSCR) [7, 8], the Low Triggered SCR (LVTSCR) [9–12], and the Diodes-string Triggered SCR (DTSCR) [13–20]. Among them, DTSCR is more suitable for lower supply voltage circuits as a value ESD protection device owing to its lower and adjustable trigger voltage [13]. However, the diodes of DTSCR are normally designed in a large area to ensure an acceptable voltage characteristic [19]. In the conventional DTSCR, the diodes-string was commonly designed with area ratio of 2:1 to its internal SCR, which has sharply increased the design costs. In addition, as the number of diodes increases, the parasitic Darlington effect of DTSCR will introduce enlarged leakage current of the device [20]. For providing more suitable ESD protections for the I/O ports of 1.2V/1.8V circuits, an ultra-low-voltage-triggered SCR (ULVTSCR) is first proposed in this letter. The proposed device has a more compact layout and avoids the Darlington effect compared to the conventional DTSCR.

Methods

The schematic cross-sectional view of the proposed ULVTSCR is shown in Fig. 1, and its equivalent circuit is demonstrated in Fig. 2. In ULVTSCR, like the conventional LVTSCR, an internal NMOS (INMOS) is embedded into PWELL with its drain setting cross NWELL and PWELL. Based on this, an external NMOS
(ENMOS) string is introduced, where the source of each ENMOS is connected to the gate and drain of the next, and the drain of the last ENMOS is connected to the gate of the INMOS for driving the INMOS to be turned on. Compared with the large area consumption of the diodes-string in DTSCR, the ENMOSs-string is designed with area ratio of only 1:5 to the internal SCR.

Once a positive ESD stress drops on the anode of ULVTSCR, the ENMOS string path will turn on first and prompt the channel of the INMOS conducting. Then, the current of INMOS will promote the parasitic transistors Q1 and Q2 to be turned on with the voltage on their emitter-base junctions increased to 0.7V respectively, thus triggering the SCR. Thanks to the much low threshold voltage ($V_{th}$) of each NMOS, the SCR can be triggered at a low voltage. Further, the $V_{t1}$ of the ULVTSCR can be adjusted by changing the number of the ENMOS from the ENMOSs-string.

### Experiments And Results

In this work, the proposed ULVTSCR devices are processed in a 65-nm CMOS logic technology. The layout of the basic ULVTSCR is shown in Fig. 3, where the width of its internal SCR ($W_{SCR}$) is 50 µm. The ENMOSs-string is set nearby the internal SCR and the distance between them is 8 µm (the minimum distance of the design rule). The width of each ENMOS ($W_{N}$) is 10 µm. To avoid the parasitic effects associated with the substrate, two P-type guard rings are employed around the ENMOSs-string and the internal SCR, respectively. The quasi-static $I-V$ characteristics of the proposed devices are measured using Hanwa TED-T5000 transmission line pulsing (TLP) tester with 10 ns rise time and 100 ns pulse width.

Four ULVTSCR devices containing different numbers ($N = 3, 4, 5, 6$) of ENMOSs are named ULVTSCR1, ULVTSCR2, ULVTSCR3, and ULVTSCR4, respectively. Measured TLP $I-V$ characteristics of four ULVTSCRs are compared in Fig. 4, as their specification and measurement results are listed in Table I. As expected, all devices operate with much low trigger voltages ($V_{t1}$) as well as high enough failure currents ($I_{t2}$). There are two trigger stages observed in turn-on processes of all devices. In ULVTSCR1, the first stage starts at ~1.92V due to the INMOS turned on driven by the trigger point (seen in Fig. 1.(a)), and the second stage is at ~5.65V due to the internal SCR triggering. Then, the voltage of ULVTSCR1 snap back to ~2.42V because of the positive feedback effect between Q1 and Q2. Subsequently, the SCR path dominates the ESD current conduction with a low resistance and achieves $I_{t2}$ of ~2.72A. When increases N from 3 to 6, the total $V_{th}$ of the ENMOSs tends to be doubled. On the one hand, the $V_{t1}$ has a decrease from ~5.65V to ~5.47V due to more current urged to the SCR path with the increased resistance of the ENMOSs-string. Notice that the $V_h$ and $I_{t2}$ of these devices basically keep the same. On the other hand, the $V_{on}$ of ULVTSCR2, ULVTSCR3 and ULVTSCR4 accordingly has been improved to ~2.80V, ~3.44V, and ~4.05V, respectively. Therefore, the proposed ULVTSCR structure is expected to provide effective ESD protections for different applications by adjust the number of its ENMOSs.

The leakage currents of four ULVTSCRs were measured by sweeping DC voltage from 0 to 1.8V at room temperature, as shown in Fig. 5. The results indicate that all ULVTSCRs possess acceptable nA-level leakage when biased DC voltage below 0.6A. As the the number of ENMOS increased, the leakage
characteristic will be optimized. For 1.8V applications, the ULVTSCR4 with 6 external NMOSs can be used. For 1.2V operations, the NMOS strings with 5 NMOSs is more suitable. More importantly, the leakage clamp capability might be further improved by increasing the number of the external NMOSs. But the number of ENMOSs needs special consideration with a trade-off between the area and leakage according to various applications.

In nanoscale CMOS processes, the epitaxy thickness is goes to thinner as the feature size scaling down, which will lead a higher sheet resistance for NWELL and PWELL. Therefore, increasing the distance (D1) from N+ active region to P+ active region in NWELL/PWELL can effectively enlarge the resistance of NWELL (PWELL). Figure 6 shows the measured TLP I-V characteristic of ULVTSCRs with four different D1. When increasing D1 from 0.5 µm to 4.0 µm, the $V_{t1}$ decreases by about 23% from ~ 6.92V to ~ 5.03V, and the trigger current is reduced from ~ 892 mA to ~ 467 mA. Moreover, the $I_{t2}$ also has an increase from ~ 2.72A to ~ 2.97A. These phenomenon can be attributed to more current branching into the SCR path as the INMOS path and N+/NWELL/PWELL/P+ diode path weakened by the enlarged $R_{NWELL}$ and $R_{PWELL}$.

Figure 7 illustrates that a larger length of the INMOS's gate D2 will lead to a significant increase in $V_h$ (from 2.42V to 3.69V) and an enhancement in holding current. This is because the increased base length of the Q2 will cause a decrease in the SCR current gain. Besides, the increased INMOS channel resistance will restrain current through the INOMS path, however, prompt more current to flow into the SCR path, which alleviates the so-called current concentration effect on INMOS, and further result in an improved $I_{t2}$ from 2.72A to 2.85A.

**Conclusions**

In this letter, a novel and improved low triggered ESD protection structure called ULVTSCR has been designed and fabricated in a 65-nm CMOS process. Unlike the huge area consumed diodes-string of DTSCR, in ULVTSCR, only 1/10 area is demanded for NMOSs-string with benefit from its stable voltage triggering characteristic. With adjustable $V_{on}$ and $V_t$ characteristics, the ULVTSCRs are suitable for 1.2V/1.8V circuits as valid ESD protection devices associated with acceptable nA-level leakages. Moreover, the proposed ULVTSCR is expected to be utilized in 2.5V or 3.3V power circuit ESD protection by improving its leakage characteristics.

**Abbreviations**

ESD: electrostatic discharge; IC:integrated circuits; GGNMOS:gate grounded NMOS; LSCR:lateral silicon controlled rectifier; MLSCR:modified lateral SCR; LVTSR:low voltage triggered SCR; ULVTSCR:ultra-low-voltage-triggered SCR; DTSCR:diodes-string triggered SCR; ENMOS:external NMOS; INMOS:internal NMOS; TLP:transmission line pulse; $V_{t1}$:trigger voltage; $V_h$:holding voltage; $I_{t2}$:failure current; $V_{th}$:threshold voltage.
Declarations

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Availability of Data and Materials

All data generated or analysed during this study are included in this published article.

Authors’ contributions

RbC generated the research idea, analyzed the data, and wrote the paper. FH, FbD, ZxL and XyF carried out the experiments and measurements. HxL and ZwL has given final approval of the version to be published. All authors read and approved the final manuscript.

Competing interests

The authors declare that they have no competing interests.

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Tables

Table 1: Specification and measurement results of the test ULVTSCRs

| Device name | Number of NMOS (N) | TLP Measurement Results |
|-------------|--------------------|------------------------|
|             |                    | $V_{on}$ (V) | $V_{th}$ (V) | $V_{h}$ (V) | $I_{f2}$ (A) |
| ULVTSCR1    | 3                  | 1.92        | 5.65        | 2.42       | 2.72       |
| ULVTSCR2    | 4                  | 2.80        | 5.51        | 2.50       | 2.71       |
| ULVTSCR3    | 5                  | 3.44        | 5.42        | 2.21       | 2.71       |
| ULVTSCR4    | 6                  | 4.05        | 5.47        | 2.35       | 2.73       |