Secure and Lightweight Strong PUF Challenge Obfuscation with Keyed Non-linear FSR

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Abstract—We propose a secure and lightweight key based challenge obfuscation for strong PUFs. Our architecture is designed to be resilient against learning attacks. Our obfuscation mechanism uses non-linear feedback shift registers (NLFSRs). Responses are directly provided to the user, without error correction or extra post-processing steps. We also discuss the cost of protecting our architecture against power analysis attacks with clock randomization, and Boolean masking. Security against learning attacks is assessed using avalanche criterion, and deep-neural network attacks. We designed a testchip in 65 nm CMOS. When compared to the baseline arbitor PUF implementation, the cost increase of our proposed architecture is 1.27x, and 2.2x when using clock randomization, and Boolean masking, respectively.

Index Terms—strong puf, nlfsr, obfuscation, power analysis

I. INTRODUCTION

Counterfeit integrated circuits (ICs) enter the supply chain from recycled, remarked, overproduced, cloned, or even out-of-spec, and defective parts [8]. Physical unclonable functions (PUFs) offer a mechanism to help prevent counterfeiting [6]. Unlike traditional identification alternatives, two authentic ICs using PUFs have very low probability of producing the same output, regardless of their programmed memory content. The ideal PUF design is lightweight [5], secure against modeling attacks [15], and produces high entropy responses that are chip unique, and stable over various environmental conditions.

Previous works used composition of strong PUFs to obfuscate the internal challenge, but resilience to learning attacks is ultimately limited by the stability of responses [16], [20], [25]. Error corrected strong PUFs require external helper data to cope with its large challenge space, but such alternative was shown to be insecure [4]. Recent works employ weak PUFs to generate an error corrected chip-unique secret, which is then used to obfuscate the external challenge [9], [12], [23]. The obfuscation algorithm must be lightweight, and secure against learning attacks. Moreover, manipulating external data (challenge) with sensitive information (secret key), requires counter-measures against power analysis attacks [11].

In this work we propose a secure and lightweight key based challenge obfuscation for strong PUFs. Our architecture is designed to be resistant against learning attacks, see Fig. 1. First, we XOR the external challenge with a secret key. The result is loaded into a non-linear feedback shift register (NLFSR), which is run for a number of cycles before the first evaluation (warm-up). The NLFSR state is then used as (obfuscated) challenge to evaluate the strong PUF. Responses are directly provided to the user—no error correction or post-processing is required. The secret key may be implemented with a one time programmable (OTP) flash, or a weak PUF.

Our key based challenge obfuscation architecture is designed to be resistant against learning attacks. We show that every bit of the obfuscated challenge meets the avalanche criterion [24]. We also performed deep-neural network (DNN) experiments with an arbiter PUF (APUF) enhanced by our obfuscation technique. The DNN model failed to obtain generalized knowledge despite of the well known APUF vulnerabilities.

The mitigation of side-channel attacks is crucial for any key based challenge obfuscation. If the key is extracted, the strong PUF is exposed to attackers. Protecting hardware implementations against power analysis attacks is costly, but effective [7], [18]. We made careful design choices in our obfuscation architecture, such that side-channel mitigation techniques have minimum impact in cost. We also discuss the implementation of a clock randomization counter-measure against power analysis attacks.

We designed a 65 nm CMOS testchip with an APUF enhanced by our proposed challenge obfuscation architecture. Our design was submitted for fabrication, and its register transfer level (RTL) code is publicly available [19]. We provide detailed post-layout area results that explore the trade-off between side-channel attack resilience and cost.

II. CHALLENGE OBFUSCATION

A. Non-linear Feedback Shift Register (NLFSR)

Non-linearity is a fundamental property for obfuscation algorithms. In the case of block ciphers, non-linear transformations are performed by substitution boxes (SBOXes). The implementation cost of SBOXes, however, is significant [21]. To
achieve lightweight non-linear challenge transformation, we use NLFSRs. NLFSRs are deterministic digital circuits capable of non-linear state transitions. Unlike their linear counterpart, NLFSRs lack a solid mathematical representation. The sequence length is found using brute force methods, therefore, maximum length NLFSRs hardly exceed $2^{21}$ [3].

Our NLFSR design is shown in Fig. 2. It uses a composition of two smaller NLFSRs, with 27 and 29 bits. Our feedback expressions have maximum length and were taken from [3]. A 56 bit challenge is obtained by concatenating the state of both NLFSRs. To make both states dependent of one another, we XOR the lowest significant bit of each NLFSR with the previous NLFSR state, running it for 56 cycles.

B. Evaluation Algorithm (no counter-measures)

The evaluation procedure for our proposed challenge obfuscation is listed in Algorithm 1. This algorithm is not yet protected against side-channel attacks. It assumes the secret key was read from OTP flash, or weak PUF. Both secret key and external challenge are 56 bits.

1) XOR key with ext. challenge, and load result to NLFSR
2) Run NLFSR for 112 cycles (for warm-up)
3) Run NLFSR for 56 cycles (flush state)
4) Evaluate strong PUF with NLFSR state as challenge
5) Output the 1 bit response (no post-processing)
6) If number of response bits is enough: return success
7) Otherwise: goto step 3

Algorithm 1 Evaluate external challenge using an implementation without side-channel attack counter-measures.

Assumptions: secret key has been read from OTP flash, or weak PUF. Both secret key and external challenge are 56 bits.

C. Secret Key Storage

The secret key storage may be implemented with one time programmable (OTP) flash, or weak PUF. Since uniqueness and unclonability properties are already provided by the strong PUF, using a weak PUF for secret key storage is possible, but adds extra complexity. One may argue that if a secret key is stored in flash, there is no need for a strong PUF. Such statement is inaccurate. For example, if the strong PUF is removed, over-produced chips (with blank OTP flash) can be programmed to behave alike any other device. That is not feasible when a strong PUFs is included in the design.

Other relevant considerations for both secret key storage options include protection against fault injection attacks, such as voltage glitches. Storing error correction data with the secret key, and performing multiple reads from memory for consistency checking was shown very effective in mitigating fault injections [22].

III. SIDE-CHANNEL ATTACK MITIGATION

The power consumption can be used to extract secret information from unprotected devices. In particular, manipulating external data (challenge) with sensitive information (secret key) is vulnerable to power analysis attacks [11]. This section discusses counter-measures to mitigate such risks.

A. Random Number Generator (RNG)

Random numbers are necessary to implement the counter-measures described in this section. Our pseudo random number generator (PRNG) is based on [18], and is shown in Fig.
3. It uses an LFSR and a cellular automata shift register (CASP), with outputs derived from their combined (XORed) state. The PRNG has three outputs, each of them generates a new random number every clock cycle. LFSR and CASR have maximum sequence length, with expressions taken from [17], and [2]. Because their cycle length is relatively prime, the total cycle length of the output is close to $2^{19}$. The seeding of LFSR/CASR states is performed using the available strong PUF. For that, we identify a challenge with unstable responses during enrollment, and store it in non-volatile memory. This challenge is repeatedly evaluated to generate random bits that initialize the LFSR/CASR states.

B. Clock Randomization

Power analysis attacks extract the key over a large number of recorded power traces. In each trace, the device manipulates distinct external data using the same key. The effectiveness of power attacks is higher when traces are aligned in time. The clock randomizer produces an irregular clock waveform, which will randomly skip clock edges. Our obfuscation architecture uses the randomized clock output. The circuit is shown in Fig. 3, and it may be seen as a conditional clock divider. The skip clock signal is derived from the 8 bit LFSR, therefore, the randomized clock waveform pattern repeats every 255 cycles, allowing authentication with predictable performance.

C. Boolean Masking of the NLFSRs

Boolean masking uses random numbers to split each value into two shares that are (ideally) uncorrelated to the original value. For example, the shared representation of $x$ is $(x_1, x_2)$, which are computed as $x_1 = x \oplus r$, and $x_2 = r$, where $r$ is a random number. The original value is recovered by XORing the shares, therefore, $x = x_1 \oplus x_2$. Physical probing of both shares is necessary to inspect the original data. When operations are performed with shared data, the power consumption is, in theory, uncorrelated to the data being processed. Moreover, if the secret key is stored in two shares, its plain-text value is never exposed.

Converting conventional single share circuits to operate with multiple shares of data differs for linear and non-linear operations. Linear operations, like XOR, shifts, and permutations, are simply applied to both shares without any changes. Non-linear operations, however, require a replacement circuit that will compute the shared outputs without disclosing the original value. We redesigned the NLFSRs described in section II-A to run using multiple shares. The resulting circuit is shown in Fig. 4. The number of state registers doubles to accommodate both shares of all values. Since XORs and shifts are linear operations, the NLFSR design remains mostly unchanged, except for the AND gates, which are replaced by their masked counterpart. The expression for the masked AND was taken from [1]. In fact, during the design of our challenge obfuscation architecture, we intentionally selected NLFSR expressions with a small number of non-linear gates to reduce the cost and complexity of masked implementations. For example, glitches are a well known source of information leakage in masked non-linear logic [13], but our original design has both AND inputs driven by registers—the best practice was already implemented.

Other design details include remasking the AND gate at every cycle, which is done by XORing fresh random numbers, $r_1$ and $r_2$, with both shares of the masked AND output. Remasking helps remove possible correlations between the original data and the shared values.

When the NLFSR warm-up cycles are completed, their shared state is XORed to obtain the unmasked, obfuscated challenge, necessary for evaluation. It is very important that this XOR operation is only performed after completion of all warm-up cycles. In other words, the XOR inputs must be gated during warm-up to avoid information leakage from the toggling XOR outputs.

D. Evaluation Algorithm (with counter-measures)

The evaluation procedure for the masked implementation is listed in Algorithm 2. Similarly to Algorithm 1, it assumes that the secret key was read from OTP flash, or weak PUF. However, the key is expected in two shares of 56 bits each.
Algorithm 2 Evaluate external challenge using an implementation with clock randomization, and Boolean masking.

Assumptions: secret key has been read from OTP flash, or weak PUF in two shares of 56 bits each. External challenge is 56 bits, with second share being all zeros.

1) Using the challenge with unstable responses, (serially) seed the PRNG with random numbers (8 + 11 = 19 bits)
2) Enable the clock randomizer
3) Using the PRNG output, (serially) seed the NLFSR with the same 56 bit random number in both shares
4) XOR the NLFSR content with the key, and load result back to NLFSR (for key remasking)
5) Run the NLFSR for 128 cycles (for time misalignment)
6) XOR ext. challenge with NLFSR, and load result back to NLFSR
7) Run the NLFSR for 112 cycles (for warm-up)
8) Run NLFSR for 56 cycles (flush state)
9) XOR the NLFSR shares and evaluate strong PUF with the unmasked state (obfuscated challenge)
10) Output the 1 bit response (no post-processing needed)
11) If number of response bits is enough: return success
12) Otherwise: goto step 8

First, the PRNG is seeded and the clock randomizer is enabled. The NLFSR is then seeded with random numbers from the PRNG. Both shares must be loaded with the same random number. The secret key is then XORed with the NLFSR state, which essentially performs a remasking operation of the key shares. Next, the NLFSR is run for 128 cycles to allow random delay insertion by the clock randomizer. The external challenge is then XORed with current NLFSR state, where the second share is considered all zeros. This will not leak information since the NLFSR content is already masked with fresh random numbers. The remaining steps are analogous to Algorithm 1, with the extra requirement of XORing the NLFSR shares to unmask the obfuscated challenge before each strong PUF evaluation.

IV. TESTCHIP IMPLEMENTATION

To accurately assess the effectiveness of our countermeasures against power analysis attacks, we designed a 65 nm CMOS testchip. Our design was submitted for fabrication, and the RTL code is publicly available [19]. Table I shows the post-layout area results for the three implementations included in the testchip. The number of instances, and area are listed for each implementation, and its components. Area for test logic is not reported. All implementations use 7 repeated evaluations for enhanced response stability [20]. The 56-APUF is a custom designed arbiter PUF with 56 delay stages, see [20] for APUF circuit details. The clock randomizer and CASR were split in two different design blocks. The placement of standard-cells and layout is shown in Fig. 5.

The 56-LFSR-APUF uses an APUF with challenge stored/unrolled by an LFSR. It represents the smallest viable authentication system that can be built using an arbiter PUF. It uses an area of 1583 ND2, which we define as our comparison baseline. The 56-NLFSR-APUF implements our challenge obfuscation architecture, without Boolean masking. Nevertheless, this implementation is not completely unprotected against side-channel attacks. It includes a clock randomizer instance, which represents 5% of the used area. The overall area of the 56-NLFSR-APUF implementation is 27% (1.27x) larger than the baseline. Finally, the 56-NLFSR-APUF (Masked) denotes the fully masked implementation, with clock randomization. The area for this implementation is 120% (2.2x) larger than the baseline. Results reported in [18] suggest that clock randomization alone delivers 2260x increase in resilience against power analysis attacks. An even greater increase, of 17330x, is achieved when clock randomization is combined with Boolean masking.

V. SECURITY ASSESSMENT

A. Avalanche Criterion

As defined in [24], if a cryptographic function is to satisfy the strict avalanche criterion (SAC), then, each output bit should change with a probability of one half, whenever a single input bit is complemented. We assess the avalanche criterion from the perspective of our obfuscation algorithm—input is the external challenge, and output is the NLFSR state after (112 + 56) cycles. Our experiment used 10000 unique external challenges, each of them was run twice, with a single toggled bit between runs. The secret key is randomized at the beginning and remains unchanged.
Fig. 6. Probability of change in NLFSR/LFSR state when a single bit of the external challenge changes.

Fig. 6 (a) and (b) show that toggling a single input bit causes a widespread (avalanche) effect in the NLFSR state, where each obfuscated challenge bit has an estimated 50% probability of changing. Same behavior was observed when other bit positions are toggled. For comparison, we replaced the NLFSR by a 56 bit linear feedback shift register (LFSR) of maximum sequence length (same as our baseline implementation discussed in section IV). The LFSR experiment also evaluates using a secret key, with output taken after (112 + 56) cycles. Results for the LFSR are reported in Fig. 6 (c) and (d), showing that the effects of a single toggled input bit on the final LFSR state are deterministic, that is, either 0%, or 100%. Therefore, LFSR based challenge obfuscation fails to meet the avalanche criterion.

B. DNN Attacks

Deep-neural networks (DNNs) are capable of learning complex PUF structures, without a mathematical model of the PUF being modelled. We performed experiments using a challenge obfuscated arbiter PUF, and a 12-layer DNN architecture similar to [10]. The input and output layers have 56, and 2 units, with 2000 units in hidden layers. The DNN was trained for 72 hours using 10 million CRPs, with a resulting accuracy equivalent to the PUF uniformity bias, which was 56% in our experiment. Therefore, the DNN model failed to obtain generalized learning on the challenge obfuscated arbiter PUF.

VI. CONCLUSION

We demonstrated the design of a lightweight key based challenge obfuscation for strong PUFs. We addressed security for both learning, and power analysis attacks. Future work shall use the fabricated testchip to assess the effectiveness of our side-channel attack counter-measures.

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