Low Power 130 nm CMOS Johnson Counter with Clock Gating Technique

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Abstract. In a very large scale integration (VLSI) of integrated circuit (IC) nowadays, digital circuit with low power design is the target of the IC designer. This is to prolong the battery life of the circuit especially if it is meant for wearable devices. In most of the digital circuits, counters are used widely and these counters consumed a lot of power. Therefore in this project the reduction of power consumption of Johnson Counter by using clock gating technique is presented. Johnson Counter is used extensively to generate particular data and shift the data synchronously as per the output sequence of the counter. To ensure the power consumption is reduced, a clock gating technique is incorporated to the Johnson Counter. This counter is implemented in Cadence software using 130 nm Complementary Metal Oxide Semiconductor (CMOS) technology. The design is observed by comparing the design of a 4 bit Johnson Counter using clock gating technique and another 4 bit Johnson Counter without using the clock gating technique. The result shows the power consumption of the Johnson Counter using the clock gating technique is 21.22 μW while the regular Johnson Counter consumed 67.09 μW. Thus the power consumption is reduced by about 68.3% when a clock gating technique is used.

1. Introduction

The circuitry and power consumption of digital system are increased day by day. More functions are integrated into electronic devices. This is achievable as technology is growing fast whereby chip size is getting reduces, speed become increases and device has become as small as possible. Since many tasks can be done in one time, power consumption has become an important part in design parameter. In a digital system, all arithmetic, logic and memory operations will be performed synchronously according to the system clock. Therefore, efficient design of sequential circuit is very important [1].

A Johnson Counter is a counter which provide data sequence and is used in many applications such as digital to analog (D/A) converter [2]. This counter provides a very specific loop synchronously which is very useful for other logic design [3]. Johnson Counter requires only a half number of flip-flops as compared to the conventional ring counter. Since the Johnson Counter is controlled synchronously by a clock, the circuit power consumption is very high. All the flip-flops in the counter will be triggered even though there is no change in the output of a certain flip-flop blocks. Thus to reduce the power consumption of the counter, clock gating technique is used to exclude those avoidable clock transitions at which no logic change is required by the block. By doing this process,
the power can be minimized for that sequential circuit [4]. Figure 1 shows the basic process of clock gating technique. It is a logic circuit that controlled the input of the clock to the sequential circuit.

![Clock gating logic](image)

Figure 1. Clock gating technique [2]

2. Clock Gating

Several methods and circuits have been proposed and designed by previous researchers in order to improve performance, achieve higher speeds and lower the power consumption of sequential circuits over the past decades [5-7]. However, there is still a challenge to provide a more low power consumption with the latest design for modern applications and with the advancement of small scale CMOS technology. This project is conducted in 130 nm CMOS technology to improve the power consumed by the Johnson Counter by incorporating a clock gating technique to govern the counter clock management system. With this, a greater device density, higher speed and low power consumption are obtained.

In clock gating technique the clock to the flip-flops in the Johnson Counter are coming from the master clock (clk) that is controlled according to equations given in equations (1) to (4). These equations are for 4 bit Johnson counter. Clock clk₁ and clk₂ are the clock master that had been divided by two and four respectively.

\[
\begin{align*}
C_{lkQ0} &= clk_f \cdot clk_{f1} \cdot clk_{f2} \\
C_{lkQ1} &= clk_f \cdot \overline{clk_{f1}} \cdot clk_{f2} \\
C_{lkQ2} &= clk_f \cdot clk_{f1} \cdot \overline{clk_{f2}} \\
C_{lkQ3} &= clk_f \cdot \overline{clk_{f1}} \cdot \overline{clk_{f2}}
\end{align*}
\]

3. The Designed Circuit

Two Johnson Counters are designed in this project by using Cadence EDA Tools. The first one is the conventional Johnson Counter and the other is the proposed Johnson Counter with the clock gating circuit. The operating supply of the circuits is 1.2 V which is smaller than other designs referred. Figure 2 and Figure 3 illustrate the conventional and proposed circuit of the Johnson Counter with clock gating technique designed in this project. A 4 bit Johnson Counter using J-K flip-flop is used in both designs. The four J-K flip-flops are used to shift the data synchronously according to the data sequence of Johnson Counter. The clock of conventional Johnson counter is not controlled in producing the output. As for the proposed Johnson counter, the flip flops will only get the clock pulse when they are needed to toggle the value stored in it. Otherwise the flip-flops are not triggered. Thus power consumption can be minimized by turning off the unused J-K flip flop.
Figure 2. The conventional Johnson Counter

Figure 3. The proposed Johnson Counter with clock gating technique

Figure 4 shows the schematic circuit of the conventional Jonson Counter designed using four J-K flip-flops, while Figure 5 shows the schematic circuit of the Johnson Counter with clock gating technique. The J-K flip-flop used in this design is in toggle mode and is built by using INVERTER and AND gates. The clock gating circuit is constructed also using a combination of INVERTER and AND gates according to the equations mentioned earlier to ensure the clock pulses to each of the flip-flop will be delivered only when it is required.
4. Result and Discussion

The Johnson Counter with clock gating technique circuit in Figure 6 was designed and simulated using Cadence with 130 nm technology and supply voltage of 1.2 V. The input for \( \text{clk}_{f2} \), \( \text{clk}_{f4} \) and master is connected with different pulse input. Figure 6 shows the simulated circuit with its input pulse and frequency.
4.1 Transient Analysis

Figure 7 shows the simulation result of the conventional counter while Figure 8 shows the simulation result of the counter with clock gating circuit. It is shown that the counter with clock gating technique is getting a pulse when it is needed to toggle the output. Each flip flop is receiving a controlled clock sequence generated by the combinational logic circuit, master clock and the available masking clocks. Hence the power consumption of the system can be controlled efficiently. From the simulation, the power consumption for conventional Johnson Counter circuit is 67.09 µW while the power consumption for Johnson Counter with clock gating technique circuit is 21.22 µW. There is a reduction around 31% or about 45.87 µW when clock gating technique is used.

Figure 6. Test bench circuit

Figure 7. Output waveform of conventional counter
4.2 Design Rule Check and Layout versus Schematic Test

Design Rule Check (DRC) is a physical design process to determine if the circuit layout drawn, satisfies a number of rules as defined by the semiconductor manufacturer. Figure 9 shows the layout for the proposed design and the result of the DRC for the layout is successful. The total physical area for the proposed analog multiplier is 129 $\mu$m².
The layout versus schematic (LVS) is done to verify whether the layout really representing the schematic circuit. In this test, a comparisons between the layout and schematic is done to check the circuit connectivity. The result from the LVS test has shown the schematic and layout are equivalent.

5. Conclusion

A 4 bit Johnson Counter with a clock gating technique are designed in this project. The clock gating technique is used as a method to reduce the power consumption of the Johnson Counter. The circuit is designed utilizing 1.2 V power supply using Cadence EDA tools with 130 nm CMOS technology. The simulation result shown that the clock gating systems is effective in reducing the power consumption if Johnson Counter.

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