Phase-Tunable Thermal Logic: Computation with Heat

Federico Paolucci\textsuperscript{1}, Giampiero Marchegiani\textsuperscript{1,2}, Elia Strambini\textsuperscript{1}, and Francesco Giazotto\textsuperscript{1}

\textsuperscript{1}NEST, Instituto Nanoscienze-CNR and Scuola Normale Superiore, I-56127 Pisa, Italy
\textsuperscript{2}Dipartimento di Fisica dell’Università di Pisa, Largo Pontecorvo 3, I-56127 Pisa, Italy

September 26, 2017

Boolean algebra, the branch of mathematics where variables can assume only true or false value, is the theoretical basis of classical computation. The analogy between Boolean operations and electronic switching circuits, highlighted by Shannon in 1938, paved the way to modern computation based on electronic devices. The grow of computational power of such devices, after an exciting exponential -Moore’s trend, is nowadays blocked by heat dissipation due to computational tasks, very demanding after the chips miniaturization. Heat is often a detrimental form of energy which increases the systems entropy decreasing the efficiency of logic operations. Here, we propose a physical system able to perform thermal logic operations by reversing the old heat-disorder epitome into a novel heat-order paradigm. We lay the foundations of heat computation by encoding logic state variables in temperature and introducing the thermal counterparts of electronic logic gates. Exploiting quantum effects in thermally biased Josephson junctions (JJs), we propound a possible realization of a functionally complete "dissipationless" logic. Our architecture ensures high operation stability and robustness with switching frequencies reaching the GHz.

The simplicity of Boolean algebra \cite{1} is one of the major motivations accounting for the development of classical computation during last century. The physical realization of mathematical operations defined in a binary environment \cite[i.e. 0 (false) and 1 (true)]{2,3,4} requires to employ systems where the variables can acquire only two stable values. Usually, this requirement is fulfilled through the use of electronic digital circuits implementing switching elements such as diodes and transistors \cite{2,3,4}. Modern devices entrain control systems able to perform logic operations without passing through electronic interfaces or external calculus apparatus \cite{5}. For this reason logic architectures taking advantage of different physical systems, such as: optics \cite{6}, fluidics \cite{7,8}, pneumatics \cite{9} and molecules \cite{10,11,12}, have been developed. What makes a calculation scheme appealing for technological applications is the operation speed. The most popular approach is quantum computation \cite{13}, where coherent quantum states exploit high-fidelity quantum bits (qubits) in order to implement computation algorithms \cite{12,13,14}.
Unfortunately, all logic architectures share one unescapable side effect: heat generation due to dissipation \[15\]-\[16\]-\[17\]. Even the most efficient computation architecture dissipates a minimum amount of heat estimated by Landauer fundamental limit \[18\]. Energy harvesting chases the storage and conversion of ambient energy into autonomous new functions. In this framework, recycling the already produced heat to perform logic operations would allow to recover part of lost power.

Here, we discuss the grounds of a thermal logic by constructing a functionally complete architecture \[19\] through the definition of thermal logic gates. The latter employ temperature as logic state variable which can acquire only two digital values: cold (logic state 0) and hot (logic state 1). A thermal logic device controls the energy flow between a reservoir and the output lead by means of a control mechanism (actuator) coupled to the input contacts. In such systems, the balance between the transmitted energy (which depends on the input temperatures configuration) and the power losses defines the output temperature (output logic state). The modulation of electron heat currents in solid-state nanostructures \[20\]-\[21\] can be realized in the framework of coherent caloritronics \[22\]-\[23\]-\[24\]-\[25\]. Heat currents are mastered by manipulating the superconducting quantum phases across thermally-biased Josephson junctions through the application of an external magnetic flux \[26\]-\[27\]-\[28\]-\[29\]. The latter can be generated by taking advantage of another quantum effect: thermoelectricity in temperature-biased normal metal-ferromagnetic insulator-superconductor \((N-FI-S)\) tunnel junctions \[30\]-\[31\]. In this Article, we show how the marriage of these two quantum effects develops a functionally complete thermal logic. The proposed structure guarantees full complementarity with low temperature electronic computating systems. In particular, the \(N-FI-S\) junctions allow to re-convert the thermal signals into electrical ones. As a consequence, the design of hybrid thermal/electrical systems (where areas of the circuit perform electrical computation and other thermal calculation) is possible. This possibility could pave the way to new computation concepts and architectures.

**Computation with Heat**

The three main operations of Boolean algebra \[1\] are: negation \((\text{NOT})\), conjunction \((\text{AND})\) and disjunction \((\text{OR})\). All the other operations can be obtained by a composition of them, i.e. they define a functionally complete logic. Figure 4a carries the essence of thermal logic: the distinctive shapes and the related truth tables of negation, conjunction and disjunction thermal logic gates are shown. For instance, the output temperature of a \(\text{NOT}\) thermal logic gate is 1 \((\text{hot})\) when the input is 0 \((\text{cold})\), vice versa. The specific value of the two logic states \(\text{cold}\) and \(\text{hot}\) only depends on the technology chosen to realize the architecture.

The most generic concept of thermal logic gate is a device with one or more binary temperature inputs that set the binary output. Such a system consists of one or more thermal inputs that control the heat current flowing through a valve connecting a power supply to an output contact, as schematized in Figure 1b. The steady-state output temperature of such general device \(T_C\), i.e. the result of the logic operation, derives from the balance between the output and loss heat currents. Therefore, it can be calculated by solving the following equation:

\[
\dot{Q}_{\text{OUT}}(T_A, T_B, T_P, T_C) - \dot{Q}_{\text{loss}}(T_A, T_B, T_P, T_C) = 0
\]

where \(\dot{Q}_{\text{OUT}}\) is the heat current flowing through the thermal valve, \(\dot{Q}_{\text{loss}}\) includes all the heat losses of the device, \(T_A\) and \(T_B\) are the input temperatures, and \(T_P\) is the power supply temperature (always kept at \(T_{\text{hot}}\)). Note that the type of implemented logic gate \((\text{OR}, \text{AND} \text{ or NOT})\) is exclusively defined by the structure of the actuators.

In solid state structures, phonons are the capital carriers exclusively of heat, while electrons carry both heat and charge. Since phonons are difficult to control, up to now the advancements in phononics \[32\] are less shattering than in electronics. Therefore, the use of phonons for thermal logic operations \[33\] is challenging. On the contrary, in coherent caloritronics \[22\]-\[23\]-\[24\]-\[26\]-\[27\]-\[28\]-\[29\] electron heat currents are precisely manipulated through the control of phases in superconducting mesoscopic circuits, such as superconducting quantum interferences devices \((\text{SQUIDs})\) \[20\]-\[21\] and superconducting quantum interreference proximity transistors \((\text{SQUIPTs})\) \[28\]. In such systems \((\text{i.e. metal thin nanostructures})\) the vanishing Kapitza resistance \[20\] ensures that the phonons of every element are completely thermalized with the substrate at a constant bath temperature \(T_{\text{bath}}\). At low temperatures \((\text{usually} \ T_{\text{bath}} < 1\text{K})\) the electron-phonon coupling is weak \[34\]. As a consequence, the electron and phonon ensembles are in thermal disequilibrium \((\text{i.e} \ T_e \neq T_{\text{ph}} \text{ with} \ T_e \text{ and} \ T_{\text{ph}} \text{ electron and phonon temperature, respectively})\) and the sum of the power losses due to the electron-phonon ther-
nal gradient in each element of the device $\dot{Q}_{c \rightarrow pb}$ is the principal cause of heat losses in the system ($\dot{Q}_{loss} = \sum_i \dot{Q}_{c \rightarrow pb,i}$).

Phase-Tunable Thermal Logic

An ideal logic architecture requires the input and output states to be identical variables (to allow for scalable networks) and fully decoupled (to avoid crosstalk).

Both requirements are fulfilled by the recently proposed first fully-thermal caloritronic device, the phase-tunable temperature amplifier (PTA) \cite{35}. It employs a thermal nano-valve (i.e. a temperature-biased SQUIPT \cite{28}) controlled by the magnetic flux $\Phi$ resulting from the closed-circuit current generated by a low temperature thermoelectric element (i.e. a $N-FI-S$ tunnel junction) \cite{30,31,38} closed by a superconducting coil. This inductive coupling guarantees an almost infinite input-to-output impedance making the PTA and ideal fully-thermal transistor when operated at unitary gain \cite{35}.

In the following we briefly introduce the temperature-biased SQUIPT and the $N-FI-S$ junction, and we show how the synergy between these two building blocks can be used to implement a functionally complete thermal logic architecture.

The SQUIPT is composed of a superconducting ring interrupted by a normal metal wire. The latter acquires a superconducting character through the superconducting proximity effect. A normal metal tunnel probe acting as output lead is coupled to the wire \cite{36}. A magnetic flux $\Phi$ threading the ring modulates the density of states (DOS) of the proximized wire \cite{39,40} and, as a consequence, the thermal conductance between the wire and the tunnel probe is periodic with the magnetic flux with period $\Phi = \Phi_0$ \cite{28}. In particular, the heat current is minimum (smaller than the power losses due to electron-phonon coupling) for $\Phi = 0$ (when the full superconducting minigap is developed in the wire DOS) and maximum for $\Phi = \Phi_0/2$ (when the wire shows a normal metal DOS). A detailed description of the thermal nano-valve (SQUIPT) can be found in the Methods section.

On the other hand, a thermoelectric effect can be generated by breaking the electron-hole symmetry in the DOS of a conductor. In a superconductor, this condition can be accomplished by Zeeman spin-splitting the DOS through an exchange field and spin-filtering the quasiparticles \cite{30}. Both the mechanisms can be provided by a single ferromagnetic insulator layer of a $N-FI-S$ junction. A temperature gradient between the normal metal and the superconductor produces a thermoelectric signal: an open circuit thermovoltage $V_T$ in the Seebeck regime or a closed circuit thermocurrent $I_T$ in the Peltier regime \cite{30,31,38}. A detailed description of the thermoelectric element can be found in the Methods.

The controlling system (actuator) is realized by shorting the thermoelectric element with a superconducting coil that inductively controls the thermal valve, as depicted in Figure 1b. This allows to design different "dissipationless" thermal logic

![Figure 2: NOT Logic Gate. a. Thermal schematic: an actuator (blue half-circumference) at input temperature $T_A$ controls through an normally open valve (red hourglass) the heat flow from the power supply (at temperature $T_{hot}$) to the output (at temperature $T_C$). The output ($\dot{Q}_{OUT}$) and loss ($\dot{Q}_{loss}$) thermal currents are shown. b. Schematic of the coherent caloritronic realization: thermoelectric elements are constituted of a metal (orange), a ferromagnetic insulator (gray) and a superconductor (blue). The blue spirals depict the superconducting coils $L_A$ and $L_O$. The SQUIPT is composed of a superconductor ring (red) interrupted by a metal wire (orange) tunnel-coupled to a metal probe (green) through a thin insulator (gray). c. Output temperature $T_C$ and output logic state $C$ versus the logic input configuration for $T_{cold} = T_{bath} = 100$ mK and $T_{hot} = 150$ mK. The output temperature $T_C$ for optimum (squares) and fluctuating (lines) input is shown.](image)
gates, because the energy used for the logic operation comes from otherwise lost power, and the dissipation in the actuation electric system is zero (the current flows in a superconducting coil).

Negation Logic Gate - NOT

The thermal inverter logic gate NOT can be in outline conceived as a normally open valve, as depicted in Figure 2a. In this way, when \( T_A = T_{cold} \) (input logic state 0) a thermal current flows through the valve and the output temperature is \( T_C = T_{hot} \) (output logic state 1). The energization of the actuator interrupts the flow of heat current from the power supply to the output lead and, as a consequence, the output temperature \( T_C \) lowers to \( T_C = T_{cold} = T_{bath} \) (output logic state 0). This can be realized by controlling a temperature-biased \( SQUIPT \) (thermal valve) through two \( N - FI - S \) junctions shorted by two coils: one connected to the input \( T_A \) while the other always kept at \( T_{hot} \) (see Figure 2b). The total magnetic flux threading the superconducting ring \( \Phi_{NOT}(T_A) \) is the sum of the contributions due to the opening \( \Phi_O \) and the input \( \Phi_A \) coil, and it takes the form:

\[
\Phi_{NOT}(T_A) = \Phi_O(T_{hot}) + \Phi_A(T_A) = M_O I_{T,O}(T_{hot}) + M_A I_{T,A}(T_A),
\]

(2)

where \( M_i \) (with \( i = O, A \)) is the mutual inductance between the superconducting ring and the opening \( L_O \) or input coil \( L_A \), and \( I_{T,i} \) is the thermocurrent generated by the opening or input thermoelectric element. The mutual inductance \( M_i \) is chosen in order to have maximum conduction through the valve when \( T_i = T_{hot} \), i.e. \( \Phi_i(T_{hot}) = \Phi_0/2 \) (with \( i = O, A \)). In summary, the behavior of the NOT thermal logic gate is expressed by the following system:

\[
\Phi_{NOT}(T_A) = \begin{cases} \Phi_0/2 + \Phi_0 & \text{if } T_A = T_{cold} \Rightarrow T_C = T_{hot} \\ \Phi_0/2 + \Phi_0 & \text{if } T_A = T_{hot} \Rightarrow T_C = T_{cold}. \end{cases}
\]

(3)

The opening coil \( L_O \) provides a constant contribution \( \Phi_0/2 \) to the flux. As consequence, when \( T_A = T_{cold} \) the input coil does not give any contribution to the total flux and the \( SQUIPT \) conducts \( (T_C = T_{hot}) \), while for \( T_A = T_{hot} \) the total flux is \( \Phi_{NOT} = \Phi_0 \) and the heat current through the valve is almost completely suppressed \( (T_C = T_{cold}) \).

In our setting, we define as logic state 0 the temperatures ranging from 100 to 105 mK (with optimum value \( T_{cold} = 100 \) mK) and logic state 1 the temperatures in the range 120 - 150 mK (with optimum value \( T_{hot} = 150 \) mK). In order to demonstrate the feasibility of our architecture we employ a Cu-EnS-Al tunnel-junction \( \Phi_0 \) as thermoelectric element and an Al-based \( SQUIPT \) with a Cu output electrode as thermal nano-valve \( \Phi_0 \). Further details on materials and geometry can be found elsewhere \( \Phi_0 \).

The output characteristic of the thermal inverter is shown in Figure 2c. For an ideal logic input 0 \( (T_A = 100 \text{ mK}) \) the output temperature is \( T_C = 142 \text{ mK} \), while for logic input 1 \( (T_A = 150 \text{ mK}) \) the output becomes \( T_C = 100 \text{ mK} \). Fluctuations on the order of 10% around the optimum input signal value produce variations of \( T_C \) that do not compromise the correct operation of the system as shown in the same figure.

Conjunction Logic Gate - AND

The thermal conjunction logic gate AND can be represented as a valve which is always closed, except when both actuators are energized \( (T_C = T_{hot} \text{ only if } T_A = T_B = T_{hot}) \), as depicted in Figure 3a. In the coherent caloritronic realization, the heat flow across a temperature-biased \( SQUIPT \) is modulated by means of the total magnetic flux \( \Phi_{AND}(T_A, T_B) \) generated by the coils \( L_A \) and \( L_B \) shorting two thermoelectric elements (input leads) at temperature \( T_A \) and \( T_B \). The total magnetic flux threading the superconducting ring is the sum of the contribution due to the two inputs \( (\Phi_A \text{ and } \Phi_B) \) and is given by:

\[
\Phi_{AND}(T_A, T_B) = \Phi_A(T_A) + \Phi_B(T_B) = M_A I_{T,A}(T_A) + M_B I_{T,B}(T_B),
\]

(4)

where \( M_i \) (with \( i = A, B \)) is the mutual inductance between the superconducting ring and the input coils \( L_i \), and \( I_{T,i} \) is the thermocurrent generated by the input thermoelectric elements. Both mutual inductances \( M_i \) are chosen in order to have \( \Phi_i(T_{hot}) = \Phi_0/4 \) (with \( i = A, B \)). As a consequence, the behavior of the AND thermal logic gate can be summarized by the following system:

\[
\Phi_{AND}(T_A, T_B) = \begin{cases} 0 + \Phi_0 & \text{if } T_A = T_{cold}, T_B = T_{cold} \Rightarrow T_C = T_{cold} \\ 0 + \Phi_0 & \text{if } T_A = T_{cold}, T_B = T_{hot} \Rightarrow T_C = T_{cold} \\ \Phi_0/2 + 0 & \text{if } T_A = T_{hot}, T_B = T_{cold} \Rightarrow T_C = T_{cold} \\ \Phi_0/2 + 0 & \text{if } T_A = T_{hot}, T_B = T_{hot} \Rightarrow T_C = T_{hot}. \end{cases}
\]

(5)

When \( T_A = T_B = T_{cold} \) [input logic state \( (A, B) = (0, 0) \)] the input coils do not generate any magnetic flux \( (\Phi_{AND} = 0) \), thereby the thermal conductance of the \( SQUIPT \) is almost zero \( (T_C = T_{cold}) \) (output logic state 0). If a single actuator is active, i.e. \( T_A = T_{hot} \) or \( T_B = T_{hot} \) with the other input at
Figure 3: AND Logic Gate. a, Thermal schematic: two actuators (blue half-circumferences) at input temperature $T_A$ and $T_B$ control through a valve (red hourglass) the heat flow between the power supply (at temperature $T_{hot}$) and the output (at temperature $T_C$). The output ($Q_{OUT}$) and loss ($Q_{loss}$) thermal currents are shown. b, Schematic of the coherent caloritronic realization: thermoelectric elements are constituted of a metal (orange), a ferromagnetic insulator (gray) and a superconductor (blue). The blue spirals depict the superconducting coils $L_A$ and $L_B$. The SQUIPT is composed of a superconductor ring (red) interrupted by a metal wire (orange) tunnel-coupled to a metal probe (green) through a thin insulator (gray). c, Output temperature $T_C$ and output logic state $C$ versus the logic input configuration for $T_{cold} = T_{bath} = 100$ mK and $T_{hot} = 150$ mK. The output temperature $T_C$ for optimum (squares) and fluctuating (lines) input is shown.

For the numerical demonstration of the behavior of the thermal conjunction we employ the same materials and geometry used for the NOT gate. Figure 3c illustrates the transfer characteristic of the AND logic gate. In the case of partially conducting SQUIPT [i.e. for $(A,B) = (1,0)$ or $(A,B) = (0,1)$], a small heat current flows from the power supply to the output electrode and the $T_C$ is slightly larger than for $(A,B) = (0,0)$. In all cases, the output temperature resides within the range of logic state 0 (100 – 105 mK), because the electron-phonon coupling is large enough to partially compensate the effect of the heat current reaching the output (see Methods).

Disjunction Logic Gate - OR

The working principle of the thermal disjunction logic gate OR is resumed in Figure 4a, where the parallel connection of two normally closed valves ($T_C = T_{cold}$ when $T_A = T_B = T_{hot}$) allows the heat flow from the power supply at temperature $T_P = T_{hot}$ to a common output electrode. The heating of at least one actuator ($T_A = T_{hot}$ and/or $T_B = T_{hot}$) opens a conduction channel to the output ($T_C = T_{hot}$). A possible practical realization is constituted of two SQUIPTs sharing the same output electrode, as schematized in Figure 4b. Each thermal nano-valve is controlled by the magnetic flux ($\Phi_A$ or $\Phi_B$) generated by a thermolectric element connected to the input electrode (at temperature $T_A$ or $T_B$). The magnetic flux $\Phi_{OR}$ effectively controlling the OR logic gate can be defined as:

$$\Phi_{OR}(T_A, T_B) = \Phi_A(T_A) \lor \Phi_B(T_B) = M_A I_{T,A}(T_A) \lor M_B I_{T,B}(T_B),$$

where $M_i$ (with $i = A, B$) is the mutual inductance between the superconducting ring and the input coil $L_i$, and $I_{T,i}$ is the thermocurrent generated by the
Figure 4: OR Logic Gate. a. Thermal schematic: two actuators (blue half-circumferences) at input temperature $T_A$ and $T_B$ control through two valves (red hourglasses) the heat flow from the power supply (at temperature $T_{hot}$) to the output (at temperature $T_C$). The output ($Q_{OUT}$) and loss ($Q_{loss}$) thermal currents are shown. b. Schematic of the coherent calorironic realization: thermolectric elements are constituted of a metal (orange), a ferromagnetic insulator (gray) and a superconductor (blue). The blue spirals depict the superconducting coils of the coherent caloritronic realization: thermoelectric elements are constituted of a metal (orange), a ferromagnetic insulator (gray) and a superconductor (blue). The blue spirals depict the superconducting coils $L_A$ and $L_B$. The $SQUIPT$s are composed of a superconductor ring (red) interrupted by a metal wire (orange) tunnel-coupled to a metal probe (green) through a thin insulator (gray). c. Output temperature $T_C$ and output logic state $C$ versus the logic input configuration for $T_{cold} = T_{hot} = 100 \text{ mK}$ and $T_{hot} = 150 \text{ mK}$. The output temperature $T_C$ for optimum (squares) and fluctuating (lines) input is shown.

input thermoelectric elements. The mutual inductance $M_i$ is chosen in order to have $\Phi_i(T_{hot}) = \Phi_i/2$ (with $i = A, B$). In summary, the $OR$ thermal logic gate works as follows:

$$\Phi_{OR}(T_A, T_B) = \begin{cases} 0 \lor 0 & \text{if } T_A = T_{cold}, \ T_B = T_{cold} \implies T_C = T_{cold} \\ 0 \lor 0 \lor 0 & \text{if } T_A = T_{cold}, \ T_B = T_{hot} \implies T_C = T_{hot} \\ 0 \lor 0 \lor 0 \lor 0 & \text{if } T_A = T_{hot}, \ T_B = T_{cold} \implies T_C = T_{hot} \\ 0 \lor 0 \lor 0 \lor 0 \lor 0 & \text{if } T_A = T_{hot}, \ T_B = T_{hot} \implies T_C = T_{hot} \end{cases}$$

(7)

For $T_A = T_B = T_{cold}$ [input logic state $(A, B) = (0, 0)$], both input coils do not generate any magnetic flux ($\Phi_{OR} = 0$), therefore both $SQUIPT$s are shut ($T_C = T_{cold}$) and the output logic state is 0. When at least one actuator is active, i.e. $T_A = T_{hot}$ or $T_B = T_{hot}$, there is heat flowing to the output electrode and $T_C = T_{hot}$ (output logic state 1).

The behavior of the thermal disjunction is numerically determined by employing the same materials and geometry used for negation and conjunction gates. The transfer characteristic of the $OR$ logic gate is resumed in Figure 4c. When only one actuator is energized [i.e. for $(A, B) = (1, 0)$ or $(A, B) = (0, 1)$], only the heat current flowing through one valve reaches the output electrode and the optimal output temperature is $T_C = 142 \text{ mK}$ (for further details see the Methods). In the case of $(A, B) = (1, 1)$, the thermal current flowing through both $SQUIPT$s arrive at the output; as a consequence, the output temperature is higher than in the previous cases ($T_C = 145 \text{ mK}$).

Operation temperature, speed, fan-out and compatibility

Temperature is the fundamental working parameter for phase-tunable thermal logic, because the grounding physical mechanisms of coherent caloritronics, such as electron-phonon coupling and superconducting pairing potential, strongly depend on both phonon and electron temperatures. For example, the working speed of such logic gates is limited by the thermalisation of the electrons with the lattice phonons, because typically the characteristic time constant of the inductive coupling is much shorter. Therefore, at first approximation, the logic
working speed depends on the threshold temperature $T_{\text{cold}} = T_{\text{bath}}$. In the limit of clean metals (employed as output electrode in our architecture) the electron-phonon relaxation time is given by \( 8 \):

$$\tau_{\text{e-ph}} = \frac{k_B v_F}{g \Sigma N_{\text{eff}} T_{\text{bath}}}$$

where $k_B$ is the Boltzmann constant, $v_F$ is the Fermi velocity, and $\Sigma$ is the electron-phonon coupling constant of the metal output lead. Therefore, the maximum operation frequency ($f = 1/\tau_{\text{e-ph}}$) is limited by the phonon temperature, as depicted in Figure 5a. For $T_{\text{cold}} = 100$ mK (which was used up to now), the operation frequency $f$ is limited to about 100 KHz. By employing superconductors with higher critical temperature, such as vanadium ($T_V = 5.38$K) and niobium ($T_{Nb} = 9.3$K), the operation temperature can be increased, and $f$ reaches values on the order of a few GHz.

Although we demonstrated a thermal logic architecture working at temperatures higher than 1 K (see Figure 5b), for logic state 1 the output temperature is drastically suppressed compared to $T_{\text{hot}}$, and the separation between $T_{\text{cold}}$ and $T_{\text{hot}}$ results to be very small (a few mK). We introduce the fan-out, namely the number of series logic gates properly working without the necessity of signal amplification (see the inset of Figure 5a). It is calculated by using the output heat of a device (in logic state 1) as input signal for the next logic gate until $T_C$ for state 1 resides in the correct temperature range. At high temperature every logic gate requires an amplification of the output signal, therefore the temperature amplifier becomes integral part of the device. On the contrary, at low temperatures the fan-out rises. For example, in the case of $T_{\text{cold}} = 100$ mK it is possible to connect, in principle, 3 devices before amplification.

Here, we have demonstrated the proof of principle of a new phase-tunable thermal logic by employing the simplest and most common geometry in hybrid nanostructures. However, the performances of our architecture (speed and fan-out) can be drastically improved by using only superconducting materials, because the thermal losses due electron-phonon coupling drastically decrease [34]. For instance, fully superconducting thermal memories working up to about 10 K at frequencies up to tens of GHz have been proposed [41]. In order to speed up our system and increase the fan-out, thermoeletric elements based on $S - FI - S'$ tunnel junctions (with $\Delta_S > \Delta_{S'}$) [42] and fully superconducting temperature-biased SQUIPTs [28] could be employed.

Finally, we would like to highlight that phase-tunable thermal logic could be used in synergy with other computation approaches. It can utilize the unavoidable heat generated by dissipation in other logic architectures in order to increase the total calculating capacity and to decrease the energy consumption. For instance, the employed materials and geometry are fully compatible with standard low temperature semiconductor-based technologies and quantum computation architectures. Therefore, phase-tunable thermal logic could represent a fertile field for the growth of new and more efficient combined computation systems.

Methods

Thermal valve - SQUIPT

Electronic thermal currents flowing from a power supply to an output electrode through a tunnel barrier are given by [34]:

$$Q_{\text{OUT}}(T_F, T_C) = \frac{2}{e^2 R_T} \int_0^\infty N_F(E) N_C(E) [f_0(E, T_F) - f_0(E, T_C)] E dE$$

where $T_{F/C}$ is the temperature of the power supply or the output lead, $e$ is the electron charge, $R_T$ is...
the normal state tunnel resistance, \( N_{PC} \) is the reduced DOS for the power supply or the output lead and \( f_0(E, T) = [1 + \exp(E/k_BT)]^{-1} \) is the Fermi distribution of the quasiparticles.

The thermal valve is a device which controls the flow of a heat current by opening and closing a passageway. The thermal current is modulated by tuning the DOS of (at least) one of the two electrodes [28]. For simplicity, in the following we assume an output electrode made of a normal metal with \( N_C(E) = 1 \) and we tune the DOS of the power supply electrode \( N_P(E) \). This can be realized by placing a normal metal wire in good electric contact with a superconducting ring (S). The superconducting properties acquired by the wire through the proximity effect [43] can be modulated by a magnetic flux \( \Phi \) threading the superconducting loop [39, 40, 41]. The DOS of the wire \( N_P = \text{Re} \left[ g^R \right] \) is the real part of the retarded Green’s function \( g^R \) [45] obtained by solving the one-dimensional Usadel equation [46]. In the limit of short junction (i.e. when \( E_{Th} = hDW_0/2 \gg \Delta_0 \)), where \( E_{Th} \) is the Thouless energy, \( h \) is the reduced Planck constant, \( D \) is the wire diffusion coefficient, \( l \) is the length of the wire and \( \Delta_0 \) is the zero-temperature superconducting energy gap (of the ring) the proximity effect is maximized, and the DOS can be explicitly written [28, 30]:

\[
N_P(E, \Phi) = \text{Re} \left[ \frac{E - iE_{Th} \gamma_s}{\sqrt{(E - iE_{Th} \gamma_s)^2 + (E_{Th} \gamma_f \cos \left( \frac{\gamma_s}{2} \right))^2}} \right].
\]

(10)

Above, \( \gamma = R_P/R_{int} \) is the transmissivity of the \( S - P \) contact (where \( R_P \) is the resistance of the metal wire and \( R_{int} \) the resistance of the \( S - P \) interface), \( g_S(E) = \frac{E + i\gamma_s}{\sqrt{(E + i\gamma_s)^2 - \Delta_S^2}} \) and \( f_S(E) = \frac{\Delta_S}{\sqrt{(E + i\gamma_s)^2 - \Delta_S^2}} \) are the coefficients of the phase-independent and phase-dependent parts of proximized DOS (where \( g_S \) is the Dynes broadening parameter [47] and \( \Delta_S \) is the BCS energy gap [48]), and \( \Phi_0 \approx 2.0678 \times 10^{-15} \) Wb is the magnetic flux quantum. The periodic behavior of \( N_C(E, \Phi) \) in the magnetic flux (with periodicity \( \Phi = \Phi_0 \)) results in a heat current \( \dot{Q}_{OUT}(T_P, T_C) \) with the same periodic dependence on \( \Phi \).

For a given supply temperature \( T_P \), the steady-state temperature of the output electrode \( T_C \) is obtained by solving the following energy balance equation:

\[
-\dot{Q}_{OUT}(T_P, T_C, \Phi) + Q_{-\text{ph},C}(T_C; T_{bath}) = 0.
\]

(11)

The electron-phonon coupling takes the form \( \dot{Q}_{\text{loss},C} = \dot{Q}_{-\text{ph},C}(T_C; T_{bath}) = \Sigma V (T^0_C - T_{bath}^n) \), where \( \Sigma \) is the electron-phonon coupling constant, \( V \) is the volume of the output electrode and the exponent \( n \) depends on the disorder of the system [44]. For metals, in the clean limit \( n = 5 \), while in the dirty limit \( n = 4.6 \) [28]. From Equation (11) descends that the temperature on the right side of the tunnel junction \( T_C \) inherits the same dependence on \( \Phi \) of \( N_C \) and \( \dot{Q}_{OUT} \) (i.e. \( T_C \) shows a minimum for \( \Phi = 0 \) and maximum around \( \Phi = \Phi_0/2 \)).

**Actuation system**

Since the nano-valve (SQUIP) is controlled by a magnetic field, it is necessary a temperature-to-flux conversion mechanism in the actuation system. This is realized by a thermoelectric element shorted by a superconducting coil.

Electron-hole asymmetry in the quasiparticle DOS is the key ingredient for thermoelectricity [37]. In superconductors it can be accomplished by spin-splitting the DOS through an exchange field \( h_{ex} \) and by selecting a specific spin species through the coupling of the superconductor to a spin-polarized element [30]. Both requirements are satisfied by a normal metal-ferromagnetic insulator-superconductor \((N - FI - S)\) junction, where the ferromagnetic element produces both the exchange field \( h_{ex} \) and the polarization \( P = (G^r_↑ - G^r_↓)/(G^r_↑ + G^r_↓) \) where \( G^r_↑ \) and \( G^r_↓ \) are the spin-up and spin-down conductances [49, 50]. For a superconductor thinner than the coherence length \( \xi_0 \), the spin-splitled DOS can be assumed to be spatially homogeneous [51] and written [52]:

\[
N_{r,i}(E) = \frac{1}{2} \text{Re} \left[ \frac{E + i\Gamma \pm h_{ex}}{\sqrt{(E + i\Gamma \pm h_{ex})^2 - \Delta_S^2}} \right],
\]

(12)

where \( E \) is the energy, \( \Gamma \) is the Dynes broadening parameter, and \( \Delta(T, h_{ex}) \) is the superconducting order parameter, which is calculated self-consistently from the BCS equation [52].

\[
\ln \left( \frac{\Delta_0}{\Delta_S} \right) = \int_0^{\hbar \omega_D} \frac{f_+(E, T) + f_-(E, T)}{\sqrt{E^2 + \Delta_S^2}} dE.
\]

(13)

Above, \( \Delta_0 \) is the zero-temperature superconducting gap, \( \omega_D \) is the Debye frequency of the superconductor and \( f_{\pm}(E, T) = [1 + \exp \{ (\sqrt{E^2 + \Delta_0^2 + h_{ex}}) / k_BT \}]^{-1} \) is the Fermi distribution of the spin-polarized electrons.

The thermocurrent originated by keeping \( N \) at a temperature \( T_A \) and the other two elements \((FI \text{ and } S)\) at the bath temperature \( T_{bath} \) takes the form:

\[
I_T(T_A, T_{bath}) = \frac{1}{eR_T} \int_{-\infty}^{\infty} N_e(E) \left[ (|f_N(E, T_A)| - f_S(E, T_{bath})) \right] dE,
\]

(14)

where \( R_T \) is the tunnel resistance in the normal state, \( N_{f,n} \) is the Fermi distribution of the metal or the superconductor. The resulting magnetic flux which threads the superconducting ring is:

\[
\Phi(T_A, T_{bath}) = M I_T(T_A, T_{bath}) = k\sqrt{T_A^{-1} T_{bath}^{-1}} I_T(T_A, T_{bath}),
\]

(15)
where $M$ is the mutual inductance, $k \leq 1$ is the coupling coefficient, $L_A$ is the inductance of the coil shorting the $N - FI - S$ junction and $L_S$ is the geometric inductance of the superconducting ring.

References

[1] Boole, G. An Investigation of the Laws of Thought on Which are Founded the Mathematical Theories of Logic and Probabilities, Dover Publications, New York, 1956.

[2] Balabanian, N. & Carlson B. Digital Logic Design Principles, John Wiley & Sons, New York, 2001.

[3] Shannon, C. D. A Symbolic Analysis of Relay and Switching Circuits, IEEE Trans. 57, 38-80, 1938.

[4] Bardeen, J. & Brattain, W. H. The Transistor, A Semi-Conductor Triode, Phys. Rev. 74, 230-231, 1948.

[5] Groisman, A., Enzelberger, M. & Quake, S. R. Microfluidic memory and control devices, Science 300, 955-958, 2003.

[6] Kitayama, K-I., Kimura, Y. & Seikai, S. Fiber-optic logic gate, Appl. Phys. Lett. 46, 317-319, 1984.

[7] Prakash, M. & Gershonfeld, N. Microfluidic Bubble Logic, Science 315, 832-835, 2007.

[8] Travagliati, M. et al. Interaction-free, automatic, on-chip fluid routing by surface acoustic waves, Lab on a chip 12, 2612-2624, 2012.

[9] Jensen, E. C., Grover, W. H. & Matheis R. A. Micropneumatic Digital Logic Structures for Integrated Microdevice Computation and Control, J. Microelectromech. Syst. 16, 1378-1385, 2007.

[10] Aviram, A. Molecules for Memory, Logic, and Amplification, J. Am. Chem. Soc. 110, 5687-5692, 1988.

[11] Ladd, T. D. et al. Quantum computers, Nature 464, 45-53, 2010.

[12] Deutsch, D. Quantum Theory, the Church-Turing Principle and the Universal Quantum Computer, Proc. R. Soc. A 400, 97-117, 1985.

[13] Debnath, S., Linke, N. M., Figgatt, C., Landsman, K. A., Wright, K. & Monroe, C. Demonstration of a small programmable quantum computer with atomic qubits, Nature 536, 63-66, 2016.

[14] Prando, G. Quantum computation: Towards on-chip qubits, Nat. Nanotech. 12, 6, 2017.

[15] Keyes, R. W. Physical limits of silicon transistors and circuits, Rep. Prog. Phys. 68, 2701-2746, 2005.

[16] Mannhart, J. & Schlom, D. G. Oxide Interfaces - An Opportunity for Electronics, Science 327, 1607-1611, 2010.

[17] Gibbs, J. W. Elementary principles in statistical mechanics, Scribner’s sons, New York, 1902.

[18] Landauer, R. Irreversibility and heat generated in the computing process, IBM J. of Research and Development 5, 183-191 , 1961.

[19] Enderton, H. B. A Mathematical Introduction to Logic, Academic Press, Cambridge, 2001.

[20] Giazotto, F. & Martinez-Pérez, M. J. The Josephson heat interferometer, Nature 492, 401-405, 2012.

[21] Martinez-Pérez, M. J., Solinas, P. & Giazotto, F. A quantum diffractor for thermal flux, Nature Commun. 5, 3579, 2014.

[22] Martinez-Pérez, M. J., Solinas, P. & Giazotto, F. Coherent Caloritronics in Josephson-Based Nanocircuits, J Low Temp Phys 175, 813-837, 2014.

[23] Meschke, M., Guichard, W. & Pekola, J. P. Single-mode heat conduction by photons, Nature 444, 187-190, 2006.

[24] Martinez-Pérez, M. J., Fornieri, A. & Giazotto, F. Rectification of electronic heat current by a hybrid thermal diode, Nat. Nanotech. 10, 303-307, 2015.

[25] Fornieri, A. & Giazotto, F. Towards phase-coherent caloritronics in superconducting circuits, Nat. Nanotech. 12, 2017.

[26] Martinez-Pérez, M. J. & Giazotto, F. Efficient phase-tunable Josephson thermal rectifier, Appl. Phys. Lett. 102, 182602, 2013.
[27] Fornieri, A., Blanc, C., Bosisio, R., D’Ambrosio, S. & Giazotto, F. Nanoscale phase engineering of thermal transport with a Josephson heat modulator, Nat. Nanotech. 11, 258-263, 2015.

[28] Strambini, E., Bergeret, F. S. & Giazotto, F. Proximity nanovalve with large phase-tunable thermal conductance, Appl. Phys. Lett. 105, 082601, 2014.

[29] Fornieri, A., Timossi, G., Bosisio, R., Solinas, P. & Giazotto, F. Negative differential thermal conductance and heat amplification in superconducting hybrid devices, Phys. Rev. B 93, 134508, 2016.

[30] Ozaeta, A., Virtanen, P., Bergeret, F. S. & Heikkilä, T. T. Predicted Very Large Thermoelectric Effect in Ferromagnet-Superconductor Junctions in the Presence of a Spin-Splitting Magnetic Field, Phys. Rev. Lett. 116, 097001, 2016.

[31] Kolenda, S., Wolf, M. J. & Beckmann, D. Observation of Thermoelectric Currents in High-Field Superconductor-Ferromagnet Tunnel Junctions, Phys. Rev. Lett. 112, 057001, 2016.

[32] Li, N., Ren, J., Wang, L., Zhang, G., Hänggi, P. & Li, B. Colloquium: Phononics: Manipulating heat flow with electronic analogs and beyond, Rev. Mod. Phys. 84, 1045-1066, 2012.

[33] Wang, L., & Li, B. Thermal Logic Gates: Computation with Phonons, Phys. Rev. Lett. 99, 177208, 2007.

[34] Giazotto, F., Heikkilä, T. T., Luukanen, A., Savin, A. M. & Pekola, J. P. Opportunities for mesoscopics in thermometry and refrigeration: Physics and applications, Rev. Mod. Phys. 78, 217-274, 2006.

[35] Paolucci, F., Marchegiani, G., Strambini, E. & Giazotto, F. Phase-Tunable Temperature Amplifier, EPL 118, 68004, 2017.

[36] Giazotto, F., Peltonen, J. T., Meschke, M. & Pekola, J. P. Superconducting quantum interference proximity transistor, Nat. Phys. 6, 254-259, 2010.

[37] Ashcroft, N. W. Mermin, D. N. Solid State Physics, (Saunders College, 1976).

[38] Giazotto, F., Solinas, P., Braggio, A. Bergeret, F. S. Ferromagnetic-Insulator-Based Superconducting Junctions as Sensitive electron Thermometers, Phys. Rev. Appl. 4, 044016, 2015.

[39] Petrashov, V. T., Antonov, V. N., Delsing, P. Claeson T. Phase Controlled Conductance of Mesoscopic Structures with Superconducting Mirrors, Phys. Rev. Lett.76, 5268, 1995.

[40] le Sueur, H., Joyez, P., Urbina, C. Esteve D. Phase Controlled Superconducting Proximity Effect Probed by Tunneling Spectroscopy, Phys. Rev. Lett.100, 197002, 2008.

[41] Guarcello, C., Solinas, P., Di Ventura, M. Giazotto, F. Hysteretic Superconducting Heat-Flux Quantum Modulator, Phys. Rev. Appl.7, 044021, 2017.

[42] Giazotto, F., Heikkilä, T. T., Bergeret, F. S. Very Large Thermophase in Ferromagnetic Josephson Junctions, Phys. Rev. Lett.114, 067001, 2015.

[43] Holm, R. & Meissner, W. Kontaktwiderstand zwischen Supraleitern und Nichtsupraleitern, Z. Phys. 74, 715-735, 1932.

[44] Meschke, M., Peltonen, J. T., Giazotto, F. Pekola, J. P. Tunnel spectroscopy of a proximity Josephson junction, Phys. Rev. B 84, 214514, 2011.

[45] Rammer, J. & Smith, H. Quantum field-theoretical methods in transport theory of metals, Rev. Mod. Phys. 58, 323-350, 1986.

[46] Usadel, K. D. Generalized Diffusion Equation for Superconducting Alloys, Phys. Rev. Lett. 25, 507-509, 1970.

[47] Dynes, R. C., Garno, J. P., Hertel, G. B., & Orlando, T. P. Tunneling Study of Superconductivity near the Metal-Insulator Transition, Phys. Rev. Lett. 53, 2437-2440, 1984.

[48] Tinkham, M. Introduction to Superconductivity, (McGraw-Hill, 1996).

[49] Moodera, J. S., Santos, T. S.& Nagahama, T. The phenomena of spin-filter tunnelling, J. Phys. Condens. Matter 19, 165202, 2007.

[50] Strambini, E., Golovach, V. N., De Simoni, G., Moodera, J. S., Bergeret, F. S. & Giazotto, F. Revealing the magnetic proximity effect in EuS/Al bilayers through superconduct-
ing tunneling spectroscopy, Phys. Rev. Mat. 00, 004400, 2017.

[51] Tokuyasu, T., Sauls, J. A. & Rainer, D. Proximity effect of a ferromagnetic insulator in contact with a superconductor, Phys. Rev. B 38, 8823-8833, 1988.

[52] Giazotto, F., & Taddei, F. Superconductors as spin sources for spintronics, Phys. Rev. B 77, 132501, 2008.

Acknowledgements

The authors thank A. Braggio for the useful discussions. The authors acknowledge the European Research Council under the European Unions Seventh Framework Programme (FP7/2007-2013)/ERC Grant No. 615187 - COMANCHE for partial financial support. The work of F.P. is funded by Tuscany Region under the FARFAS 2014 project SCIADRO. The work of E.S. is funded by a Marie Curie Individual Fellowship (MSCA-IFE-ST No. 660532-SuperMag).

Author contributions statement

F.P. and F.G. conceived the architecture, F.P., G.M. and E.S. developed the model, F.P wrote the manuscript. All authors reviewed the manuscript.

Additional information

The authors declare no competing financial interests.