A fixed latency ORBGRAND decoder architecture with LUT-aided error-pattern scheduling

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Abstract—Guessing Random Additive Noise Decoding (GRAND) is a universal decoding algorithm that has been recently proposed as a practical way to perform maximum likelihood decoding. It generates a sequence of possible error patterns and applies them to the received vector, checking if the result is a valid codeword. Ordered reliability bits GRAND (ORBGRAND) improves on GRAND by considering soft information received from the channel. Both GRAND and ORBGRAND have been implemented in hardware, focusing on average performance, sacrificing worst case throughput and latency. In this work, an improved pattern schedule for ORBGRAND is proposed. It provides > 0.5 dB gain over the standard schedule at a block error rate ≤ 10^{-5}, and outperforms more complex GRAND flavors with a fraction of the complexity. The proposed schedule is used within a novel code-agnostic decoder architecture: the decoder guarantees fixed high throughput and low latency, making it attractive for latency-constrained applications. It outperforms the worst-case performance of decoders by orders of magnitude, and outperforms many best-case figures. Decoding a code of length 128, it achieves a throughput of 79.21 Gb/s with 58.49 ns latency, yielding better energy efficiency and comparable area efficiency with respect to the state of the art.

Index Terms—Guessing Random Additive Noise Decoding (GRAND), Maximum Likelihood (ML), Ordered Reliability Bits GRAND (ORBGRAND), Decoder Architecture, VLSI, Low Latency, High Throughput

I. INTRODUCTION

Maximum Likelihood (ML) decoding is an optimal decoding approach that can be applied to virtually any code. It foresees the comparison of the vector to be decoded with all the possible codewords in the codebook, and the selection of the codeword that minimizes the error probability as the decoded vector. The complexity of ML decoding is very high, making it impractical for many applications.

Guessing Random Additive Noise Decoding (GRAND) [1] is a recently-proposed algorithm that can perform ML or near-ML decoding with limited complexity, and that can be used to decode any type of code. It has been shown to work well with short, high-rate codes. Unlike decoding algorithms that use the structure of the code to detect and correct errors in the received vector, GRAND attempts to guess the error pattern that was applied on the transmitted codeword. ML decoding is achieved by scheduling the attempted error patterns in descending order of likelihood: here lies the inherent challenge of GRAND decoding, that has led to various incarnations being proposed [2]–[4]. They evolve on the original premise by making use of soft information received from the channel to better infer the error-pattern schedule. Ordered Reliability Bits GRAND (ORBGRAND) [4] sorts the channel soft information in order of reliability, and schedules the error patterns based on their logistic weights. Thanks to its good trade-off between performance and complexity, it has attracted the interest of the research community, and improvements to ORBGRAND have been recently proposed [5], [6].

The attractiveness of GRAND-based algorithms has led to the proposal of decoder hardware implementations [7]–[9]. The standard GRAND is used in [7], [8], while [9] implements ORBGRAND. To limit the implementation complexity, the scheduled error patterns are constrained in terms of Hamming weight HW and, in case of [9], logistic weight LW as well. These decoders focus on average performance: they potentially require a large number of patterns to achieve good error-correction performance, but the decoding process is on average very short, since it is usually sufficient to attempt the decoding with few, highly-likely error patterns to obtain a valid codeword. These design choices lead to high average throughput and short average latency, but cause the worst case scenarios to have very bad performance. This is a noticeable hurdle towards the widespread acceptance of GRAND-based decoding, given the strict latency and demanding performance constraints of recent and upcoming communication standards, like the ultra-reliable low-latency scenario foreseen in the 5G standard [10]–[12].

In this work, the aforementioned problem is tackled on two sides. As a first step, the core issue of GRAND-based decoding of scheduling the error patterns in the most effective order is addressed. A high-performance error-pattern schedule is proposed, that enables ORBGRAND to provide its best error-correction performance in literature with a small maximum number of error patterns. This schedule further improves the performance of the one proposed in [5], through the addition of a number of empirically-observed highly likely patterns as the first ones attempted: it yields more than 0.5 dB gain over the original schedule [4] at a block error rate ≤ 10^{-5}. The proposed schedule can be easily used by any ORBGRAND decoder architecture in literature. Secondly, a code-agnostic decoder architecture is proposed, that can decode any binary linear code with code length ≤ N and code rate ≥ R_{min}. Enabled by the characteristics of the newly proposed schedule, it adopts a different paradigm than the architectures in literature, and guarantees a high fixed throughput and very low fixed latency. The variable number of patterns required to achieve successful decoding is leveraged to reduce power...
consumption instead of increasing average throughput. The decoder has been synthesized in 7 nm FinFET technology with various sets of design parameters, and shown to yield up to 79.21 Gb/s throughput and down to 40.58 ns latency.

The remainder of the paper is organized as follows. Section II introduces GRAND-based decoding and the relevant evolutions. The proposed error-pattern schedule is detailed in Section III and simulation results are presented. The decoder architecture is described in Section IV, whereas implementation results and comparison with the state of the art are presented in Section V. Finally, Section VI draws the conclusion.

II. PRELIMINARIES

Let us define a binary linear block code code \( \mathcal{C} \), identified by the \( k \times n \) generator matrix \( \mathbf{G} \) and the \((n-k) \times n\) parity check matrix \( \mathbf{H} \). Then, a source vector \( \mathbf{u} \) of \( k \) bits is encoded into a codeword \( \mathbf{x} \) of \( n \) bits through \( \mathbf{x} = \mathbf{u} \cdot \mathbf{G} \). The \( 2^n \) possible \( \mathbf{x} \) compose the codebook of \( \mathcal{C} \), for which the following is true:

\[
\forall \mathbf{x} \in \mathcal{C}, \mathbf{H} \cdot \mathbf{x}^T = \mathbf{0}
\]

where \( \mathbf{0} \) is the all-zero vector. Let \( \mathbf{x} \) be transmitted over a noisy channel; given the received soft-value vector \( \mathbf{y} \), the hard-decided vector inferred from \( \mathbf{y} \) can be expressed as \( \text{HD}(\mathbf{y}) = \mathbf{x} \oplus \mathbf{e} \), where \( \mathbf{e} \) is the error pattern applied by the channel. In case \( \mathbf{H} \cdot \text{HD}(\mathbf{y})^T = \mathbf{0} \), errors have been detected. In the remainder of this work, the elements of \( \mathbf{y} \) are supposed to be logarithmic likelihood ratios (LLRs).

The Guessing Random Additive Noise Decoding (GRAND) algorithm attempts to find the error pattern \( \mathbf{e} \) applied by the channel. After generating a test pattern \( \mathbf{e} \), it computes \( \text{HD}(\mathbf{y}) \oplus \mathbf{e} \). The codebook is queried by computing \( \mathbf{H} \cdot (\text{HD}(\mathbf{y}) \oplus \mathbf{e})^T \); in case the result is \( \mathbf{0} \), the decoding is successful, and vector \( \hat{\mathbf{y}} = \text{HD}(\mathbf{y}) \oplus \mathbf{e} \) is returned, otherwise a new \( \mathbf{e} \) is generated. These steps should be repeated until a valid codeword is found, GRAND with abandonment (GRANDAB, [1]) foresees the termination of the decoding process after a maximum amount of codebook queries \( Q_{max} \) has been performed.

To achieve ML decoding, the error patterns should be scheduled from the most probable to the least probable one. The scheduling of the error patterns is at the core of GRAND-based decoding design, and has a large impact on the algorithm error-correction performance. The optimal ordering for binary symmetric channels is based on the Hamming weight \( HW \) of \( \mathbf{e} \), but this schedule is strongly suboptimal for additive white Gaussian noise channels (AWGN). The Ordered Reliability Bits GRAND (ORBGRAND) [4] algorithm is a better suited option for complex channels. By making use of the soft information vector \( \mathbf{y} \) instead of \( \text{HD}(\mathbf{y}) \) only, it infers a refined error-pattern schedule. The elements of vector \( \mathbf{y} \) are sorted in ascending order of reliability, i.e. in ascending order of magnitude in case of LLRs, resulting in the index permutation \( \pi \) and the sorted vector \( \pi(\mathbf{y}) \). Error patterns \( \mathbf{e} \) are applied to \( \pi(\mathbf{y}) \) in ascending logistic weight order (LWO). Given the ordered vector \( \mathbf{v} = (v_0, \ldots, v_{HW-1}) \) containing the indices of the nonzero entries of \( \mathbf{e} \), and its length \( LW \) of \( \mathbf{e} \) can be computed as

\[
LW(\mathbf{e}) = \sum_{i=0}^{HW-1} (v_i + 1) .
\]

Error patterns with the same \( LW \) can be scheduled in any order. The syndrome calculation can be then performed in natural or permuted order:

\[
\mathbf{H} \cdot (\text{HD}(\mathbf{y}) \oplus \pi^{-1}(\mathbf{e}))^T, \\
\pi(\mathbf{H}) \cdot (\pi(\text{HD}(\mathbf{y})) \oplus \mathbf{e})^T,
\]

where \( \pi(\mathbf{H}) \) is the column-permuted \( \mathbf{H} \). In Section V the permuted order syndrome \( s = \pi(\mathbf{H}) \cdot z^T \) is used, where \( z = \pi(\text{HD}(\mathbf{y})) \oplus \mathbf{e} \).

GRAND-based decoding is universal, as it can be applied to any code. In the remainder of the paper, two particular code types are used as examples: Bose-Chaudhuri-Hocquenghem (BCH) codes [13] and polar codes [14]. BCH codes are widespread block codes used in a variety of practical applications, including communications, storage and cryptography. They feature a very flexible code design, that can cater to different error correction needs through the tuning of the code minimum distance. Polar codes are binary block codes based on the polarization property of their kernel matrix. They have been the object of intense research in the last decade, and they have been included in the 5G wireless communication standard [15]. For improved decoding performance, they are often concatenated to a cyclic redundancy check (CRC) code. In the remainder of this work, a BCH code with \( n = 127, k = 113 \) that can correct 2 errors is considered, and addressed as BCH(127,113,2). Its generator polynomial is \( g_c=0x7761 \) defined on GF(2\(^7\)), with a field generator polynomial \( g_f=0x91 \). The 5G standard \( n = 128, k = 105 \) polar code concatenated with an 11-bit CRC is used, and labeled PC(128,105)+CRC(11).

III. LUT-AIDED ERROR-PATTERN SCHEDULE

In [5], the improved logistic weight order (iLWO) schedule was proposed. It is an ordering of error patterns for ORBGRAND decoding that computes the weight of each error pattern \( \mathbf{e} \) as follows:

\[
iLW(\mathbf{e}) = \sum_{i=0}^{HW-1} (i + 1) \cdot (v_i + 1) ,
\]

where \( v \) has been defined for [2]. The iLWO resulting from the above iLW favors patterns with low \( HW \) and potentially high \( LW \) over patterns with low \( LW \) but high \( HW \). It follows the observation that at high enough signal-to-noise ratio (SNR), and thus low enough block error rate (BLER), high-\( HW \) patterns are less likely to lead to successful decoding, but LWO can schedule them with high priority. iLWO has been shown to yield substantial gains in error-correction performance with respect to LWO, it can be generated algorithmically, and it is parallelizable. However, it is an approximation of the sequence of error patterns that can be observed empirically on an AWGN channel, and as such it is suboptimal. To further
improve the error-correction performance of ORBGRAND and reduce its average number of queries \( Q \) given a maximum \( Q_{\text{max}} \), the look-up-table-aided (LUT-aided) error-pattern schedule is proposed here. It first attempts the decoding with \( Q_{\text{LUT}} \) empirically-observed error patterns stored in order of likelihood of occurrence, while the remaining \( Q_{\text{max}} - Q_{\text{LUT}} \) patterns are generated according to the preferred schedule, excluding the intersection with the set of the already selected \( Q_{\text{LUT}} \) patterns. Since iLWO currently yields the best error-correction performance and lowest average \( Q \) among the error-pattern schedules for ORBGRAND in literature, in the remainder of this work the LUT-aided iLWO is considered, and it is labeled LA-iLWO. Nevertheless, LUT-aided decoding is a general approach that can be paired with any other schedule if so desired, for example LWO \cite{9} or the \( HW \)-based schedule of GRAND \cite{1}. In the same way, LUT-aided schedules can be easily implemented in any practical ORBGRAND decoder \cite{9}, improving error-correction performance and speed.

Figure 1 plots the BLER and average number of queries \( Q \) for a BCH(127,113,2) code, decoded with various GRAND-based decoders, and with the soft-input type-II Chase decoder \cite{16} with 32 test patterns. The latter is a common choice for high-performance decoding of BCH codes. Simulations consider BPSK modulation over an AWGN channel. SGRAND \cite{3} with \( Q_{\text{max}} = 2^{14} \) achieves ML performance with this code at the observed SNRs, and it is plotted as a baseline. It can be seen that Chase-32 follows SGRAND closely in the considered SNR range. The blue curve with circular markers portrays the performance of ORBGRAND with the novel LA-iLWO schedule, \( Q_{\text{max}} = 2^{13} \), and \( Q_{\text{LUT}} = 512 \). To select the \( Q_{\text{LUT}} \) error patterns, the transmission of 128-bit vectors was simulated, and 10\(^{9} \) error events at SNR\(= 7 \) dB were observed, totaling around 2000 different error patterns on the sorted hard-decided vector \( \pi(\mathbf{HD}(\gamma)) \). The 512 ones occurring most frequently account for more than 99.85% of the total; their frequency of occurrence is monotonically descending, and each point of the curve counts more than 100 observations.

The selected \( Q_{\text{LUT}} \) patterns vary with the target SNR, albeit very gradually, and are expected to change in presence of different channel models. The remaining \( Q_{\text{max}} - Q_{\text{LUT}} = 7680 \) patterns are created according to iLWO, excluding the patterns already included in the first \( Q_{\text{LUT}} \). LA-iLWO is shown to yield a 0.15 dB gap from ML at BLER\(= 10^{-6} \), while outperforming both iLWO (0.05 dB gain) and LWO (0.4 dB gain) with the same \( Q_{\text{max}} \). At the same time, it matches the performance of list-GRAND (LGRAND, \cite{6}), that follows LWO and uses approximately \( 5 \times Q_{\text{max}} \), together with a more complex algorithm. iLWO is shown to also closely follow LGRAND as well, regardless of its lower complexity. At BLER\(= 10^{-7} \), the gain over LWO, iLWO and LGRAND increases. The average \( Q \) of LWO, iLWO and LA-iLWO are very close, with iLWO having lower \( Q \) than LWO, and LA-iLWO outperforming both at high enough SNR, whereas the high \( Q_{\text{max}} \) of LGRAND leads to substantially higher \( Q \).

Figure 2 shows BLER and average \( Q \) for a polar code PC(128,105) concatenated with an 11-bit cyclic redundancy check (CRC), both taken from the 5G standard \cite{15}. SGRAND, again plotted as a reference, requires \( Q_{\text{max}} = 2^{23} \) to achieve ML performance. Considering \( Q_{\text{max}} = 2^{13} \), LA-iLWO has a 0.65 dB gap from ML performance at BLER\(= 10^{-6} \). LA-iLWO and iLWO have almost the same performance, yielding a gain of more than 0.5 dB with respect to LWO; all three ORBGRAND schedules have very similar average \( Q \), with that of LA-iLWO being the lower of the three at high SNR. The gap between LA-iLWO and SGRAND reduces to 0.35 dB at BLER\(= 10^{-7} \). Increasing \( Q_{\text{max}} \) to \( 2^{17} \) makes LA-iLWO, iLWO, and LWO yield almost the same performance, while their average \( Q \) maintain the same trend observed for \( Q_{\text{max}} = 2^{13} \). This is due to the fact that as \( Q_{\text{max}} \) increases, the first \( Q_{\text{LUT}} \) patterns of LA-iLWO are eventually scheduled by iLWO as well, leading to similar BLER at a higher average \( Q \). Increasing \( Q_{\text{max}} \) allows also the suboptimal LWO to schedule patterns that were given a higher priority by both LA-iLWO and iLWO. The performance
of the widespread successive cancellation list decoder (SCL, \cite{17}) with a list size of 8, often considered the state-of-the-art decoder for 5G polar codes, is plotted as well. It can be seen that it matches the performance of LA-iLWO at lower SNR, while quickly converging towards that of SGRAND at higher SNR. It is worth noting that the LA-iLWO patterns used by LA-iLWO to decode a polar code in Figure 2 are the same ones used to decode a BCH code in Figure 1 since the error patterns depend on the code length but are independent from the encoding used, if any.

The maximum number of queries $Q_{\text{max}}$ is one of the main factors in determining the worst case latency of a GRAND-based decoder. By considering high-performance error-pattern schedules like LA-iLWO and iLWO, that schedule error patterns with high likelihood of occurrence earlier than LWO, ORBGRAND can achieve performance close to ML at lower SNR. It is worth noting that the ORBGRAND can achieve performance close to ML with a relatively small LUT. These schedules are thus well suited for practical implementation, as they can reduce latency, increase throughput and reduce power consumption of hardware decoders.

IV. DECODER ARCHITECTURE

GRAND-based decoder architectures in literature rely on the reuse of hardware resources for successive decoding attempts. This approach yields very short average latency and very high average throughput, but incurs dismal figures of merit in the worst case scenario. This drawback limits their appeal in practical applications where strict latency constraints are present. In this Section, a decoder architecture for ORBGRAND-based decoding that has a very high fixed throughput and a very short fixed latency is presented. In the spirit of GRAND-based algorithms, the decoder is code-agnostic: it can decode any type of binary linear code with code length $\leq N$ and with code rate $\geq 1/N$. The decoder is based on a highly-parallel, pipelined, feed-forward design; while the architecture is not tied to a particular error-pattern schedule, the decoder leverages the improved performance of LA-iLWO to limit $Q_{\text{max}}$. Figure 3 shows the proposed decoder architecture: it is divided into $T$ stages separated by registers, that are represented by gray rectangles.

A. Stage 0

The LLR vector $y$ is input in stage 0, each of the $N$ LLRs represented with sign and magnitude over $B$ bits. It is sorted by a bitonic sorter that uses $B-1$ bits for internal comparisons, i.e. the magnitude of each LLR, while also forwarding the sign bit of each LLR and its $\log_2 N$-bit index. Consequently, each of the $\log_2 N$ pipeline stages internal to the sorter are constituted of $(B + \log_2 N) \times N$ registers. Note that assuming BPSK modulation that maps 0 to +1 and 1 to −1, HD$(y)$ is equal to the vector of sign bits of $y$. The outputs of the sorter are the permuted vector of sign bits $\pi$(HD$(y)$) and the $N \times \log_2 N$ sorted vector of indices $\pi$, that can be used as a permutation vector to recover the natural order corrected vector $\hat{y}$ by one of the following stages. If a code with code length $n < N$ is to be decoded, the $n$ lowest indices of $\pi$ have to contain the valid LLRs. The magnitudes of the unused $N-n$ LLRs need to be set to $2^{B-1} - 1$, so that the sorter does not permute them, and their sign bits set to 0.

Parallel to the sorter, the $N$-bit vector containing the sign of each LLR HD$(y)$ is multiplied by the parity check matrix of the code $H$. The $H$ matrix is stored in a dedicated register matrix of dimension $(N-1) \times N$ (H memory in Figure 5). Since $H$ changes every time a new code is used, the $H$ memory needs to be programmable; to allow that, an $N$-bit input is used to overwrite the contents of the $H$ memory row-by-row after a code change. The $H \cdot \text{HD}(y)^\top$ product is performed for each row of $H$ in parallel, as shown in Figure 4 to compute the result of parity check $i$, bit HD$(y)_j$ with $0 \leq j < N$ is ANDed with $H_{i,j}$, and the $N$ resulting bits are XORed together to obtain the syndrome bit $s_i$. In case $s_i = 0$, $0 \leq i < N - 1$ then HD$(y)$ is already a valid codeword: it is forwarded to the following stages as the valid candidate in natural order $\hat{y}$, and the $\text{\texttt{vld}}$ flag is set to 1 by NORing all

![Fig. 2: BLER and average Q for PC(128,105)+CRC(11).](image-url)
bits of \( s \). The \( N - 1 \) rows of \( H \) allow for code rates as low as \( 1/N \), but in case a lower range of rates is foreseen, the matrix dimensions become \( (N(1 - R_{\text{min}})) \times N \), where \( R_{\text{min}} \) is the minimum code rate allowed by the system. Given a code rate \( r \geq R_{\text{min}} \) and a code length \( n \leq N \), the \( N - n \) rightmost columns and the \( N(1 - (r - R_{\text{min}})) \) lowermost rows of \( H \) need to be set to zero, so that the unused symbols are ignored in all the parity checks, and that all syndromes relative to unused parity checks are zero.

The columns of \( H \) are also permuted according to \( \pi \), the resulting \( \pi(H) \) being forwarded to the next stages, where it is used to verify if one of the vectors obtained through ORBGRAND in permuted order is a valid codeword.

In case \( \text{HD}(y) \) is a valid codeword, the decoding process has finished, and only \( \hat{y} = \text{HD}(y) \) and \( \hat{y}_{\text{old}} = 1 \) need to be forwarded to the following stages: consequently, all other registers between Stage 0 and 1 are not updated, reducing the dynamic power consumption. Moreover, as soon as \( \hat{y}_{\text{old}} = 1 \) is available, the sorting operation can be stopped, allowing to avoid the update of the last \( \log_2 N - 2 \) pipeline stages internal to the sorter and further save power. Unlike architectures like [9], where successful decoding with \( Q < Q_{\text{max}} \) allows to increase the average throughput, the proposed architecture uses the variable \( Q \) as a means to limit switching activity and reduce power consumption.

1) Sorter pruning: Depending on \( Q_{\text{max}}, N \), and the chosen pattern schedule, the bitonic sorter can be pruned without loss of error-correction performance and at undetectable cost in average \( Q \). Let us consider the parameters used in Section 4 for the decoder implementation (LA-iLWO, \( Q_{\text{max}} = 2^{13} \), \( Q_{\text{LUT}} = 512, N = 128 \)): with these conditions, while computing \( \pi(\text{HD}(y)) \oplus e \), the last \( N/2 \) entries of \( \pi(\text{HD}(y)) \) are flipped only by \( e \) with \( HW = 1 \). In fact, the scheduled error patterns with \( HW > 1 \) involve only the first \( N/2 \) positions of \( \pi(\text{HD}(y)) \). Consequently, any shuffling among the last \( N/2 \) positions will not have any impact on the error-correction capability of the decoder, at most changing the number of average queries \( Q \). The structure of a bitonic sorter foresees \( \log_2 N \) stages, each one with an additional set of compare-and-swap units [19]. The last stage, shown in Figure 3 for \( N = 16 \), performs \( \log_2 N \) consecutive sets of compare-and-swap. After the first set, the \( N/2 \) most reliable LLRs have been separated from the \( N/2 \) least reliable ones: the \( \log_2 N - 1 \) sets of compare-and-swap involving only the \( N/2 \) least reliable LLRs, highlighted in red in the figure, can be removed, as they would implement only an internal permutation. No change in in average \( Q \) could be detected via simulation using the pruned sorter.

B. Stage 1

After the decoder stage 0 has performed preliminary operations (checking if \( y \) represents a valid codeword, sorting the LLRs and providing \( \pi \)), stage 1 is where the core of GRAND-based decoding begins.

The LUT-aided schedule described in Section III requires the offline identification of the \( Q_{\text{LUT}} \) initial patterns, while the remaining \( Q_{\text{max}} - Q_{\text{LUT}} \) can be generated on-the-fly via LWO, iLWO, or any other schedule. Nevertheless, the pipelined nature of the proposed architecture demands that all \( Q_{\text{max}} \) error patterns are available at the same time, albeit in different pipeline stages. Consequently, all \( Q_{\text{max}} \) patterns are pre-generated and stored in dedicated memories; the \( Q_{\text{max}} \) patterns are divided among \( Q_{\text{max}}/Q_S \) decoder stages, with each stage attempting \( Q_S \) error patterns, starting with stage 1. A pattern memory stores \( Q_S \) binary vectors of \( N \) bits; each vector is a pattern \( e \) with a 1 at every position of the sorted hard-decision vector \( \pi(\text{HD}(y)) \) to be flipped. Much like the \( H \) memory in stage 0, the pattern memory is a \( Q_S \times N \) matrix of registers that can be programmed one row at a time. The storage of precomputed patterns enables the application of pattern schedules that cannot be easily generated algorithmically, like the first \( Q_{\text{LUT}} \) patterns of LA-iLWO, and removes the need to constrain the \( HW \) and \( LW \).
of patterns [9]. As the implementation cost of the pattern memories can grow quickly with $Q_{\text{max}}$, this solution suits well high-performance schedules like LA-iLWO, that rely on smaller $Q_{\text{max}}$.

All $Q_S$ patterns are XORed in parallel to $\pi(\text{HD}(y))$, returning the $Q_S \times N$ matrix $Z$, where $z_i = \pi(\text{HD}(y)) \oplus e_i$, $0 \leq i < Q_S$. Multiplying each vector $z_i$ to the permuted $H$ matrix $\pi(H)$, the syndrome matrix $S$ is obtained, each column $s_i$ the syndrome of $z_i$. If one of the syndromes is the all-zero vector, then one of the rows of $Z$ is a valid codeword, and the $z_{e\text{ld}}$ flag is set to 1 and forwarded to the next stage. Since the error patterns are ordered but they are applied in parallel, it is possible that more than one syndrome is zero; a priority selector forwards to the next stage the $z_i$ corresponding to the zero syndrome with the highest priority.

In case $z_{e\text{ld}}$ is risen, the pipeline registers for $\hat{y}$, $\pi(\text{HD}(y))$, $\pi(H)$ are not enabled, as a valid codeword was just found and the following stages do not need to continue the decoding. If $\hat{y}_{e\text{ld}} = 1$ at the input of stage 1, then a valid codeword was found at stage 0, and also the pipeline registers corresponding to $z$ and $\pi$ are disabled, while $\hat{y}$ is activated. In case no valid codeword was found at stage 0 and 1, then $\hat{y}_{e\text{ld}} = z_{e\text{ld}} = 0$, and the $z$ and $\hat{y}$ registers are disabled, while $\pi(\text{HD}(y))$, $\pi(H)$, and $\pi$ are enabled.

C. Stage 2 to $T-3$

The $T-4$ stages following stage 1 all have the same functionality, differing only by the contents of the pattern memory. Beside all of stage 1 operations, these stages also perform the inverse permutation of $z$ to obtain the natural order candidate codeword $\hat{y}$. If stage $t$ receives $z_{e\text{ld}} = 1$ as an input, a valid codeword in permuted order was identified at stage $t - 1$. The permutation $\pi$ is then used to perform $\hat{y} = \pi^{-1}(z)$ through $N$ to-1 demultiplexers, setting $\hat{y}_{e\text{ld}} = 1$ and forwarding only $\hat{y}$ to the following stages, while the other pipeline registers are not enabled.

D. Stage $T-2$ and $T-1$

Stage $T-2$ is the last one that includes a pattern memory, and thus the last where error correction can be attempted. As such, it maintains the functionality of the previous stage, but neither $\pi(\text{HD}(y))$ nor $\pi(H)$ can be forwarded to the last stage.

The last stage can only perform $\hat{y} = \pi^{-1}(z)$ if it receives $z_{e\text{ld}} = 1$, otherwise it outputs the received $\hat{y}$ and $\hat{y}_{e\text{ld}}$.

E. Latency and throughput

Given that the number of decoder stages $T$ is equal to $Q_{\text{max}}/Q_S + 2$, the decoding latency of the proposed decoder architecture in clock cycles can be computed as

$$L = \frac{Q_{\text{max}}}{Q_S} + 2 + \log_2 N,$$

where $\log_2 N$ is the latency introduced by the sorter in stage 0. The information throughput in bit/s is instead computed as

$$T = nrf,$$

where $n \leq N$ is the code length, $r \geq R_{\text{min}}$ is the code rate, and $f$ is the clock frequency at which the decoder is working. Unlike decoder architectures in literature, neither $L$ nor $T$ depend on the average $Q$.

V. IMPLEMENTATION

The decoder architecture proposed in Section [V] has been described in Verilog HDL and synthesized in TSMC 7 nm FinFET technology, using a typical corner; implementation results are reported in Table [II] along with state of the art decoders. The area and area efficiency of all solutions listed in these Tables have also been scaled to the 20 nm technology node using the scaling factors provided in [19]. The complexity of the designs and the distance between the native technology nodes involved makes it virtually impossible to have a fair comparison, and the scaled results should be considered as no more than order-of-magnitude approximations.

Table [I] showcases the implementation results for different combinations of decoder parameters, for a maximum code length $N = 128$ and $Q_{\text{max}} = 2^{13}$. Power estimations have been obtained annotating the decoder switching activity using realistic test vectors provided by the simulator: the reported figures consider a BCH(127,113,2) code decoded with OR-BRAND and the LA-iLWO schedule with $Q_{\text{LUT}} = 512$ patterns observed at SNR = 7 dB (BLER = $10^{-6}$). Nevertheless, the power is estimated at a target bit error rate of $10^{-5}$, the same conditions as [8], whose results are included in the Table. Implementation $A_{\text{BCH}}$ allows for the highest degree of code rate flexibility by instantiating an $H$ memory of size $(N - 1) \times N$. The high degree of internal parallelism inferred by $Q_S = 512$ leads to a very short latency of 25 clock cycles, however limiting the achievable frequency to $f = 616$ MHz, with an area occupation of 5.16 mm$^2$. The information throughput for the considered code is of 69.61 Gb/s. Since the

![Fig. 5: Last stage of an $N = 16$ bitonic sorter.](image-url)
### TABLE I: Proposed decoder implementation results versus [8], [20].

| Result type                      | This work | [8]a | [20]b |
|----------------------------------|-----------|------|-------|
| Technology [nm]                  |           |      |       |
| Synthesis                        | 7         | 7    | 7     |
| A_{BCH}                          | 512       | 512  | 256   |
| B.C.                             | 512       | 512  | 512   |
| C.t    | 8          | 8    | 8     |
| Area [mm²]                       | 616       | 616  | 701   |
| Area eff. [Gbps/mm²]             | 18.58     | 13.32| 14.58 |
| Area @ 20 nm [mm²]               | 5.16      | 3.70 | 4.05  |
| Supply [V]                       | 128       | 128  | 128   |
| LUT                              | 109       | 109  | 109   |
| r                                | 113/127   | 113/127| 113/127|
| Q_{max}                          | 21/3      | 21/3 | 21/3  |
| Q_{S}                            | 512       | 512  | 256   |
| T                                | 18        | 18   | 34    |
| Q_{LUT}                          | 512       | 512  | 512   |
| B                              | 8         | 8    | 8     |
| B.C.                             | 204.06 mW |      |       |
| W.C.                             | 277.66 mW |      |       |
| Power [mW]                       |           |      |       |
| Energy/bit [pJ/bit]              | 3.99      | 2.83 | 2.58  |

*a GRAND algorithm  
*b ne{128,127} only  
*c Modified type-II Chase algorithm with 4 test patterns  
*d Single code decoder for BCH(63,51,2)

The proposed architecture guarantees fixed latency and throughput, there is no difference between best case (B.C.) and worst case (W.C.) L and T. Power consumption at the observed SNR is 277.66 mW, dominated by leakage power. In fact, more than 54% of received vectors are valid codewords, thus requiring only partial activation of stage 0, while the vast majority of the remaining ones can be corrected in stage 1, with the activation rate of stage 2 being ≈ 0.3%. Thus, the switching activity in stages 2 to 17 is virtually null, greatly limiting the dynamic power of the decoder.

Implementation B maintains the same decoder parameters as A_{BCH} but reduces the size of the H memory, imposing R_{min} = 0.656, to enable a fairer comparison with [8]. This change of parameter is reflected on the size of all pipeline stages, on the complexity of the syndrome calculation circuit, and on the generation of \( \hat{y}_{old} \) (stage 0) and \( z_{old} \) (stage 1 to T-2); the total area occupation is reduced to 3.70 mm². The smaller H and the consequently simplified logic allows to reduce power consumption to 196.67 mW.

Implementation C instantiates smaller pattern memories, with \( Q_S = 256 \). This choice increases the number of decoder stages to \( T = 34 \), resulting in \( L = 41 \) clock cycles. Each stage has lower complexity than the \( Q_S = 512 \) case, thanks to the smaller pattern memory, syndrome calculation circuit, and z selection networks: the shorter critical path increases the achievable frequency to \( f = 701 \) MHz, and thus the throughput to \( T = 79.21 \) Gb/s. On the other hand, the higher \( T \) increases the total number of pipeline registers, that do not scale with \( Q_S \), leading to an overall area of 4.05 mm². While the smaller \( Q_S \) allows to have an even more granular stage activation rate than implementation A_{BCH} and B, the combined effects of the higher frequency and the more numerous pipeline stages bring the power consumption to 204.06 mW.

The flexibility granted by the implementation A_{BCH} comes at a cost in terms of area efficiency (\( \frac{\text{Area}}{\text{Power}} \)) and energy per bit (\( \frac{\text{Energy}}{\text{Bit}} \)), that are the lowest and highest among the three solutions, respectively. Reducing the size of H allows for 1.39× improvement in area efficiency and 1.41× reduction in energy per bit with respect to the fully-flexible implementation. The higher throughput of implementation C allows for an additional 1.04× factor in area efficiency and 1.10× energy per bit saving.

The work presented in [8] details a fabricated chip that implements the GRAND algorithm [1]. The generated test patterns are limited to those with \( HW \leq 3 \), and attempted in ascending \( HW \) order. Unlike the proposed architecture, the code length is not fully flexible, and can support only \( n =\{127,128\} \). The decoder in [8] has very low power consumption and a small area occupation. This is achieved
through small internal parallelism, time-sharing of resources, and low \( f \); these factors, together with the large \( Q_{\text{max}} \), also lead to low throughput and a great disparity between the B.C. and W.C. scenarios. The latency swings between 71 and 29,500 clock cycles, and the throughput can be as low as 0.004 bits/cycle. These metrics are independent of the technology node, and the proposed architecture yields lower latency and higher throughput than \([8]\). The low maximum throughput of \([8]\) (1.59 bits/cycle or 108 Mb/s) also impacts negatively the efficiency figures: even considering the results scaled to 20 nm and low \( f \) (4223 – 9300 Mb/s), instead of 5.75 dB used in Table I) allows for generally lower power consumption, since 84% of received vectors are valid in the case of a smaller \( r \) (16 \( \leq \) \( r \) 512), whereas LA-iLWO yields a lower throughput at 656 Mb/s due to the large number of codewords, and leads to an activation rate of stage 2 lower than that of \([8]\) (18% of the time on average).

The work in \([9]\] presents a decoder architecture for ORBGRAND decoding using a pruned LWO schedule. The results reported in Table II consider PC(128,105) + CRC(11) at a target BLER=10^{-7}. Implementation \( A_{\text{PC}} \) is structurally identical to \( A_{\text{BCH}} \), with updated power, throughput and efficiency due to the different code used, while implementation \( D \) and \( E \) have \( R_{\text{min}} \approx 0.75 \) instead of \( R_{\text{min}} \approx 0.656 \) used in \( B \) and \( C \). These are the same conditions of \([9]\), whose results are reported as well in the same table. The information throughput is lower than before, due to the polar code having a lower \( r \) than the BCH(127,113,2). The higher SNR (7.4 dB instead of 5.75 dB used in Table I) allows for generally lower power consumption, since 84% of received vectors are valid codewords, and leads to an activation rate of stage 2 lower than 0.001%. The higher \( R_{\text{min}} \) considered in implementation \( D \) and \( E \) reduces both area occupation and power consumption, and yield improved energy and area efficiency with respect to implementation \( B \) and \( C \).

The work in \([9]\] presents a decoder architecture for ORBGRAND decoding using a pruned LWO schedule. The results labeled under \([9]\) in Table I consider patterns with \( L W \leq 6 \) and the \( H W \) to 6, while those under \([9]\) consider patterns with \( L W \leq 96 \) and \( H W \leq 8 \), that result in \( Q_{\text{max}} \approx 1.77 \cdot 2^{16} \) and \( \approx 1.30 \cdot 2^{18} \), respectively. Under these conditions, the target BLER=10^{-7} is achieved around SNR= 8 dB, whereas LA-iLWO yields more than 0.5 dB gain with a substantially smaller \( Q_{\text{max}} \) at the same BLER. Much like \([8]\), the architectures in \([9]\) use
time-shared resources to limit complexity and sacrifice W.C. latency and throughput in favor of average measures. These decoders yield a 1-cycle B.C. latency and a B.C. throughput in bits/cycle as high as that of the proposed decoder, but the high $Q_{\text{max}}$ results in very long W.C. latency and extremely low W.C. throughput, orders of magnitude worse than those in A:\text{PC}, D, and E. Being the more heavily pruned of the two, and thus having the worst BLER, [9].1 yields very good area and energy efficiency. The [9].2 implementation, whose performance matches that of ORBGRAND with the standard LWO schedule, yields instead lower efficiencies.

An unrolled polar decoder architecture for the PC(128,64)+CRC(6) code implementing the SCL decoding algorithm with list size 8 is presented in [21], and its implementation results are reported in Table II. Similarly to the proposed decoder, the pipelined structure of [21] yields high throughput (equal to $N \cdot r$ bits/cycle) and low fixed latency, at the cost of large area occupation.

VI. CONCLUSION

In this work, the LUT-aided error-pattern schedule for ORBGRAND has been proposed. It schedules a number of empirically-observed, highly-likely error patterns before standard error patter generation. Coupled with the high-performance iLWO schedule, it achieves near-ML performance and the best error-correction performance in literature among ORBGRAND schedules, outperforming more complex GRAND-based decoding algorithms with a smaller number of maximum codebook queries. The proposed schedule can be easily implemented within decoder architectures in literature.

Making full use of the advantages of the LUT-aided iLWO schedule, a code-agnostic flexible decoder architecture has been proposed. It can decode any binary linear block code with code length and rate that fit within constraints set at design time. Unlike existing GRAND-based decoders, that focus on average performance sacrificing worst case performance, the proposed decoder guarantees fixed high throughput and low latency, making it an attractive choice for latency-constrained applications. The paradigm shift allows to use the average performance to reduce power consumption.

The proposed architecture has been implemented in 7 nm FinFET technology for various combinations of code and decoder parameters: its fixed throughput and latency outperform the worst-case performance of decoders in literature by orders of magnitude, and also outperform many best-case performance figures. Depending on implementation parameters, it can achieve a throughput of up to 79.21 Gb/s with 58.49 ns latency, and up to 69.61 Gb/s throughput with 40.58 ns latency, obtained during the decoding of a BCH code of length 127 and of a polar code of length 128, respectively. Given a maximum number number of error patterns, the decoder architecture can be tuned to distribute them among different decoding stages, striking different tradeoffs between power, area occupation, latency, and throughput.

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