Extended Off-Time Control for CRM Boost Converter Based on Piecewise Equivalent Capacitance Model

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ABSTRACT Valley-switching (VS) and zero-voltage switching (ZVS) improves overall efficiency in critical conduction mode (CRM) boost converters. To achieve VS/ZVS, off-time of the main switch is often extended to match the resonance period by circuit inductor and parasitic capacitors of switching components. In this article, a piecewise equivalent model for parasitic capacitors is proposed to derive analytical solutions of the resonant process, by which the numerical solutions of VS/ZVS time is calculated. To precisely achieve VS/ZVS in a boost converter, corresponding extended off-time based on the numerical solutions is implemented with an extended off-time (EOT) controller. The EOT controller makes the inductor volt-second unbalance in continuous conduction mode (CCM) operation during one switching cycle, leading to the convergence to CRM operation. The analytical and experimental results correct the results derived by conventional equivalent model for parasitic capacitors, which leads to deviated VS/ZVS boundary and wrongly calculated off-time. The proposed model and controller are verified in a non-synchronous CRM boost converter based on GaN high electron mobility transistor (HEMT) and SiC diode. With the derived extended off-time, a peak efficiency of 99.15% is achieved at output power level of 200W.

INDEX TERMS Critical conduction mode, parasitic capacitance, piecewise equivalent capacitance model, extended off-time control, boost converter.

I. INTRODUCTION

Converters under critical conduction mode (CRM) operation, which have potentials to degrade system order and achieve high efficiency, are widely used in low to medium power conditions, such as LED driver, power factor correction and on-board charger, [1]–[4]. To improve overall efficiency in non-synchronous boost converters operating in CRM, two sources of power loss are always considered: conduction loss and switching loss [5], [6]. With a certain power level and modulation strategy, conduction loss can be reduced by selecting devices with lower on-resistance or smaller voltage drop. Comparatively, reduction of switching loss requires corresponding control strategy or auxiliary circuit to minimize the voltage across switch at switching-on moment [7], [8]. Therefore, in addition to selecting components with lower on-resistance, valley switching (VS) and zero-voltage switching (ZVS) are vital approaches to improve overall efficiency for CRM boost converters.

To achieve VS/ZVS in non-synchronous boost converters, an extended off-time is often regulated delicately, which starts from zero-crossing point of inductor current and ends at the rising edge of switching-on signal. In this situation, the extended off-time should match the resonant time by circuit inductor and parasitic capacitors of switching components, which usually consist of diode junction capacitor \( C_j \) and output capacitor \( C_{\text{loss}} \) of the main switch. As shown in Fig. 1,
In order to precisely achieve VS/ZVS for a CRM converter, an analog zero current detection (ZCD) circuit is often used to locate the zero-crossing point of inductor current, which is the starting point of the resonant process. However, the resonant process only lasts several hundred nanoseconds, which means that the delay introduced by the ZCD circuit should be carefully considered. For examples, sampling resistor is used in ZCD circuit, where high speed comparator is required. To ensure a controllable VS/ZVS time, delay of each components is discussed in detail [22]. In [23], [24], the inductor current zero-crossing point is detected by secondary windings of the inductor. This method is easy to understand, but components in ZCD detection module may induce significant delay to the turn-on edge of main switch [25]. Furthermore, the detecting delay varies with input voltage, which make it complex to accurately locate the current zero-crossing point. From the aforementioned methods, analog ZCD module is indispensable for the implementation of CRM operation. However, an accurate ZCD module with matched speed could also increase the overall design complexity, cost and size, especially in high frequency applications.

In this article, a piecewise equivalent capacitance model for CRM boost converter is proposed to quantify the resonant process, based on which the optimal VS/ZVS time is derived. To simplify the non-linearity problem by $C_{\text{oss}}$ and $C_j$, the capacitor value is first divided into several intervals with respect to suitable voltage levels, where the capacitor value in each interval varies within a small range. Then, the equivalent capacitor value for each interval is calculated by a charge-based equivalent method. With capacitor values in each interval and the interval boundaries, analytical solutions of the resonant process are derived, which is the foundation to calculate the optimal VS/ZVS time. Comparatively, analytical solutions by the conventional constant capacitance model fail to match the resonant process in practice. To achieve VS/ZVS in a boost converter, the optimal VS/ZVS time is implemented in the extended off-time by an extended off-time (EOT) controller. The EOT controller makes the inductor volt-second unbalance in continuous conduction mode (CCM) operation during one switching cycle, leading to the convergence to CRM operation. Since it does not require ZCD module or current sensing, it is a sensorless approach. The derived VS/ZVS time and the proposed controller are verified in a boost prototype based on GaN HEMT and SiC diode.

This article is organized as follows: Section II discusses the conventional constant capacitance model for parasitic capacitors in non-synchronous CRM boost converter, and introduce the estimation method of equivalent capacitance under different conditions. In Section III, optimal VS/ZVS time is calculated according to the piecewise equivalent capacitance model. Furthermore, the VS/ZVS time is applied in the extended off-time with the proposed EOT controller. In Section IV, the derived VS/ZVS time and the proposed controller are verified by experimental results. Finally, a brief conclusion is given in Section V.
II. VS/ZVS REALIZATION IN NON-SYNCHRONOUS CRM BOOST CONVERTER WITH CONSTANT CAPACITANCE MODEL FOR PARASITIC CAPACITORS

VS/ZVS is often an indispensable approach to reduce the switching loss. For a non-synchronous CRM boost converter, to derive a proper VS/ZVS time, resonant process by circuit inductor and parasitic capacitors of switching components is often investigated. In the followings, the conventional constant capacitance model for the parasitic capacitors is introduced. This approach simplifies the analytical solutions of the resonant process, however, it ignores nonlinearity of the parasitic capacitors, where deviated VS/ZVS time is induced.

A. RESONANT PROCESS WITH CONSTANT CAPACITANCE MODEL

Basic topology of a non-synchronous boost circuit based on GaN HEMT and SiC diode is given in Fig. 2(a). Since the values of input and output capacitors in the circuit are much larger than that of the parasitic capacitors, the equivalent resonant circuit for boost circuit during VS/ZVS time is simplified to the topology in Fig. 2(b).

The current and voltage of the boost converter when VS and ZVS are achieved is given in Fig. 3(a) and Fig. 3(b). For an entire switching cycle, gate voltage \( v_{gs} \) keeps high from \( t_0 \) to \( t_1 \), where the inductor current rises from zero at \( t_0 \) and falls to zero at \( t_2 \). Finally, the circuit inductor resonates with parasitic capacitors from \( t_2 \) to \( t_3 \).

For VS situation shown in Fig. 3(a), \( v_{ds} \) during resonance is always higher than zero. The gate voltage \( v_{gs} \) turns high at the valley point of \( v_{ds} \), where the inductor current returns zero. For ZVS situation shown in Fig. 3(b), the resonant process ends at \( t_3 \), which is the zero-crossing point of \( v_{ds} \).

To derive the optimal VS/ZVS time, the resonant process should be fully investigated. Although the behaviors of the current and voltage are different for these two situations, their equivalent resonant topology remains the same. According to the equivalent circuit shown in Fig. 2(b), differential equations for drain-source voltage \( v_{ds} \) and inductor current \( i_L \) during the resonance are described as:

\[
L \frac{di_L(t)}{dt} = v_{in} - v_{ds}(t),
\]

\[
C_{oss}(v_{ds}) \frac{dv_{ds}(t)}{dt} = C_i(v_{ds}) \frac{dv_{ds}(t)}{dt} + i_L(t).
\]

To simplify the analysis of resonant duration, the two voltage-varying parasitic capacitors are equivalent to constant values based on the conventional constant capacitance method. Since voltage \( v_{ds} \) across the MOSFET satisfies

\[
v_{ds}(t_2) = v_0 \quad \text{and} \quad dv_{ds}(t_2)/dt = 0,
\]

equations (1) and (2) for \( v_{ds} \) and the inductor current \( i_L \) are derived as:

\[
i_L(t) = \frac{v_{in} - v_0}{Zr} \sin(\omega_r(t - t_2)),
\]

\[
v_{ds}(t) = \frac{v_{in} - (v_{in} - v_0) \cos(\omega_r(t - t_2))}{Zr},
\]

where \( Z_r = \sqrt{L/(C_{oss} + C_j)} \), \( \omega_r = 1/\sqrt{L(C_{oss} + C_j)} \), and \( t_2 \) is the beginning of the resonant process, as shown in Fig. 3(a) and Fig. 3(b). Thus, the capacitors during resonant process can be combined as one capacitor, which is \( C_{eq} = C_{oss} + C_j \).

B. SOLUTIONS FOR VS/ZVS TIME

With the resonant process equations (3) and (4), solutions for VS/ZVS time can be calculated.

For VS situation in Fig. 3(a), it is indicated by (4) that \( v_{ds} \) is positive definite when \( 2v_{in} > v_0 \). Therefore, VS can be achieved in half the resonant period, which is

\[
t_{VS} = \pi/\omega_r = \pi \sqrt{LC_{eq}}.
\]
For ZVS situation in Fig. 3(b), drain-source voltage $v_{ds}$ might reach a negative value when $2v_{in} < v_o$ according to (4). For a Si-based MOSFET, the negative value of $v_{ds}$ is clamped by the body diode. Comparatively, GaN HEMT is a kind of common power devices with a symmetric structure, without parasitic diodes and works upon two dimensional electron gas (2DEG) [26]. Similarly, the resonance voltage will be clamped to zero when $v_{eq}$ is higher than threshold voltage. Furthermore, no reverse recovery is induced owing to 2DEG conduction mechanism.

To investigate the optimal ZVS time $t_{zvs}$, the zero-crossing point of $v_{ds}$ is located by setting $v_{ds}(t_3) = 0$, which gives the minimum ZVS time as

$$t_{zvs, \min} > t_3 - t_2 = \frac{1}{\omega_r} \arccos\left(\frac{v_{in}}{v_{in} - v_o}\right). \quad (5)$$

After $t_3$, inductor current rises with a slope of $v_{in}/L$, the negative to positive zero-crossing point of $i_L$ is given by:

$$t_4 = t_3 + \frac{v_{in} - v_o}{\omega_r v_{in}} \sin\left(\omega_r (t_3 - t_2)\right). \quad (6)$$

Therefore, ZVS can be achieved from $t_3$ to $t_4$, where the GaN HEMT is reversely conducted.

Above analysis is based on the assumption that $C_{eq}$ is irrelevant to voltage level. However, both $C_{oss}$ and $C_j$ vary greatly with voltage. Since resonance period is directly related to capacitor value, this ignorance can lead to deviated results of the resonance behavior, such as VS/ZVS boundary and optimal VS/ZVS time. Furthermore, the beginning of the resonant process is often located by ZCD approach, whereas an accurate ZCD module with matched speed could increase overall design complexity, cost and size, especially in high frequency applications.

### III. PIECEWISE EQUIVALENT CAPACITANCE MODEL AND EOT CONTROL

In order to address aforementioned issues, a piecewise equivalent capacitance model is proposed to correct the optimal VS/ZVS time, which provides a reasonable explanation to the resonant behavior with nonlinear capacitors. The derived VS/ZVS time is implemented by an extended off-time (EOT) controller. It is a simple and effective approach to achieve CRM operation without ZCD module.

#### A. EOT CONTROL

Scheme of boost converter under EOT control is given in Fig. 4. Proportional-integral (PI) controller adjusts the reference current $i_{ref}$. The EOT controller makes the inductor volt-second unbalance in CCM operation during one switching cycle, leading to the convergence to CRM operation.

The EOT controller is described as

$$\begin{cases}
T_{on} = \frac{i_{ref} L}{v_{in}}, \\
T_{off} = \frac{i_{ref} L}{v_o} + t_{ext},
\end{cases} \quad (7)$$

where the extended off-time $t_{ext} = t_{rise} + t_{VS/ZVS}$, as shown in Fig. 5. The proposed approach can be applied to other basic topologies such as buck, buck-boost, SEPIC and Ćuk converter, as shown in TABLE 1, in which $L_1$ is the input inductor for SEPIC or Ćuk converter.

When the converter deviates to CCM operation, the inductor volt-second during one switching cycle satisfies

$$\frac{v_{in}}{L} T_{on} + \frac{v_{in} - v_o}{L} T_{off} = \frac{v_{in} - v_o}{i_{ref}} t_{ext} < 0. \quad (8)$$

Therefore, the inductor current is unbalanced during one switching cycle, which leads to a current decrease. Finally, owing to the unidirectional conduction characteristic of the diode, the converter converges to CRM operation in steady state.

In order to achieve VS/ZVS, $t_{ext}$ should be carefully considered, where $t_{VS/ZVS}$ is the VS/ZVS time, and $t_{rise}$ is
400V is given in Fig. 6(a). The rising time of \( v_{ds} \) at the falling edge of \( v_{gs} \), as shown in Fig. 5.

In the followings, a piecewise equivalent capacitance model is proposed to linearize the nonlinear capacitors in each interval. With the linearized capacitance, the optimal VS/ZVS time is derived by the analytical solutions of resonant process.

### B. PIEWISE EQUIVALENT CAPACITANCE MODEL

Considering the variations of equivalent capacitors, \( C_{eq}(v_{ds}) \) is a function of \( v_{ds} \). Resolving equations (1) and (2), a differential equation for \( v_{ds} \) during resonance is given by

\[
LC_{eq}(v_{ds}) \frac{d^2 v_{ds}(t)}{dt^2} + L \frac{dC_{eq}(v_{ds})}{dv_{ds}} \left( \frac{dv_{ds}(t)}{dt} \right)^2 + v_{ds}(t) = v_{in}.
\]

Obviously, (9) is a second-order nonlinear differential equation. Its analytical solution is hard to derive. Conventional method consumes that \( C_{eq}(v_{ds}) \) is a fixed value, which makes (9) a linear equation. It simplifies the analysis for the resonance behavior. However, the results can lead to mistake solutions of the resonant process.

To refine the resonant process, a piecewise equivalent capacitance model is introduced in the following.

In order to derive the accurate analytical solutions of (9), the nonlinear item, which is the second order differential term, should be eliminated. Considering the complexity and accuracy of the derivation process, the piecewise equivalent capacitance model for \( C_{oss} \) and \( C_j \) is proposed.

A piecewise equivalent capacitance example when \( V_o = 400V \) is given in Fig. 6(a). The \( C_{oss}(v_{ds}) \) is divided into three intervals. The \( n \)th interval boundaries are chosen from \( v_{in} \) to \( v_{in+1} \), where the capacitance in the boundary satisfies \( C_{oss}(v_{in+1}) = 2C_{oss}(v_{in}) \), \( n = 1,2,3,4 \). Comparatively, \( C_j(v_{ds}) \) drops rapidly to a small value after the resonance when voltage across the diode turns high. Since \( C_j \) is much smaller than \( C_{oss} \) in most situations, it is acceptable to divide \( C_j(v_{ds}) \) into two intervals, where the first interval boundary satisfies \( C_j(v_2) = 2C_j(v_1) \), as shown in Fig. 6(a).

For the entire resonance circuit, \( C_{eq} \) is acquired by combining \( C_{oss} \) with \( C_j \), as shown in Fig. 6(b). Finally, four intervals for \( C_{eq} \) with respect to different voltage levels are established, as shown in TABLE 2.

In order to derive analytical solutions of the resonant process, the equivalent capacitance of each interval is obtained by a charge-based equivalent method, which calculates the average capacitance for each interval. For voltage interval boundary with \( v_a \) and \( v_b \), the charge \( Q_c \) on capacitors satisfies:

\[
Q_C(v_a) - Q_C(v_b) = \int_{v_b}^{v_a} C(v)dv.
\]

Therefore, the equivalent capacitance is derived by

\[
C_{eq} = \frac{Q_C(v_a) - Q_C(v_b)}{v_a - v_b}.
\]

### C. NUMERICAL SOLUTIONS FOR \( t_{VS}/ZVS \) AND \( t_{ch} \)

1) NUMERICAL SOLUTIONS FOR \( T_{VS/ZVS} \)

Based on the equivalent capacitance and initial conditions of each interval, the analytical solutions for \( v_{ds} \) and \( i_L \) during the resonant process are derived. Resonant curves of \( v_{ds} \) and \( i_L \) at VS and ZVS situation are given in Fig. 7. For VS situation in Fig. 7(a), VS point is located by the valley value of \( v_{ds} \) or the zero-crossing point of \( i_L \). Comparatively, as shown in Fig. 7(b), there is a time range that ZVS can be achieved. Detail derivation process for \( t_{VS} \) and \( t_{ZVS} \) is given in the following.

Although the capacitors are voltage-varying, the resonance structure remains the same during VS/ZVS time, as shown in Fig. 2(b). Therefore, resonance behavior of each interval can be also described by (1) and (2), where the common solution of \( v_{ds} \) in each interval when \( v_{ds} > 0 \) is

\[
v_{ds}(t) = v_{in} + a_n \cos(\omega_n(t - t_n)) + b_n \sin(\omega_n(t - t_n)), \quad (12)
\]

where \( \omega_n = 1/\sqrt{L C_{eq,n}} \), \( n = 1,2,3,4 \). According to (2), \( i_L(t) \) in each interval is solved as

\[
i_L(t) = \frac{C_{eq,n}dv_{ds}(t)}{dt} = -a_n \omega_n C_{eq,n} \sin(\omega_n(t - t_n)) + b_n \omega_n C_{eq,n} \cos(\omega_n(t - t_n)). \quad (13)
\]

Derivation of \( a_n \) and \( b_n \) is based on the boundary conditions. By setting \( t = t_n \) in (12), \( a_n \) is derived as

\[
a_n = v_{ds}(t_n) - v_{in} - \frac{dv_{ds}(t_n)}{dt} \quad (14)
\]

Furthermore, \( b_n \) is derived by the current boundary condition. By setting \( t = t_n \), differentiating (12) gives

\[
dv_{ds}(t_n)/dt = b_n \omega_n. \quad (15)
\]

\[
\frac{dv_{ds}(t_n)}{dt} = \frac{i_L(t_n)}{\omega_n C_{eq,n}}.
\]
FIGURE 7. Resonant curves of $v_{ds}$ and $i_L$ when (a) VS and (b) ZVS are achieved.

Since inductor current keeps constant at the boundary of the $n$th and $(n-1)$th interval, the boundary current value is given by

$$i_L(t_n) = -a_{n-1} \omega_{n-1} C_{eq,n-1} \sin (\omega_{n-1} (t_n - t_{n-1})) + b_{n-1} \omega_{n-1} C_{eq,n-1} \cos (\omega_{n-1} (t_n - t_{n-1})).$$  \hspace{1cm} (16)

With analytical solutions of the resonant process, the VS point and the first ZVS point can be derived. When the valley value is above zero, VS is achieved at the valley point. When the valley value reaches below zero, ZVS is achieved starting from the first zero point of $v_{ds}$, which locates at $t_{ZVS1}$ shown in Fig. 7(b). After this point, the inductor current will rise up to zero with a slope rate of $v_{in}/L$, where the GaN HEMT is reversely conducted. Therefore, the negative-positive inductor current zero-crossing point $t_{ZVS2}$ is derived by

$$t_{ZVS2} = t_{ZVS1} + \frac{L_i(t_{ZVS1})}{v_{in}},$$  \hspace{1cm} (17)

where $t_{ext1}$ is acquired by solving (13) = 0. From $t_{ZVS1}$ to $t_{ZVS2}$, $v_{ds}$ can be regarded as zero, where ZVS is achieved.

FIGURE 8. Overall design process of optimal extended off-time.

2) NUMERICAL SOLUTIONS FOR $T_{CH}$

According to Fig. 5(b), charge balance of the equivalent capacitance during the conversion time gives

$$\int_0^{v_{in}} C_{eq}(v) \, dv = \int_0^{t_{rise}} i_{pk} \, dr.$$  \hspace{1cm} (18)

In general, a converter based on GaN HEMT and SiC diode provides a relatively high conversion speed of switching state, which makes $t_{ch}$ a much smaller value compared with $t_{VS/ZVS}$. Therefore, inductor current during $t_{ch}$ can be regarded as a current source during the charging time to parasitic capacitors.

Since $i_{pk} = T_{on} L / v_{in}$, $t_{ch}$ is derived by

$$t_{ch} = \frac{v_{in}}{T_{on} L} \int_0^{v_{in}} C_{eq}(v) \, dv.$$  \hspace{1cm} (19)

D. OVERALL DERIVATION PROCESS OF OPTIMAL EXTENDED OFF-TIME

Fig. 8 gives the overall calculation process for the extend off-time to achieve VS/ZVS. Firstly, the $C_{oss}$ and $C_j$ are divided into intervals with different voltage levels. The equivalent capacitance is calculated by the charge-based equivalent method based on (11). Then, analytical solutions of the resonant process are derived as (12) and (13), with which the optimal $t_{VS/ZVS}$ is obtained. Furthermore, $t_{ch}$ is calculated by (19). Combining $t_{VS/ZVS}$ and $t_{ch}$, the optimal $t_{ext}$ is derived to achieve VS/ZVS under EOT control.

E. SMALL SIGNAL MODELING

For stability analyses and compensator design, small signal model of boost converter with EOT control is given in the followings. In Fig. 9, $\{G_{vi}(s), G_{vg}(s), G_{vr}(s)\}$ are transfer functions from $i_{ref}$, $v_{in}$ and $R$ to the output voltage, respectively.

Under EOT control, the inductor current peak value is regulated to $i_{ref}$. Therefore, the output current average value of the boost converter is given by

$$i_{av} = \frac{i_{pk} T_{off}}{2(T_{on} + T_{off})} = \frac{i_{ref} T_{off}}{2(T_{on} + T_{off})}.$$  \hspace{1cm} (20)
Finally, small signal model of the system is derived as in Fig. 10.

The converter, the PI compensator is optimized as \( P = \frac{i_{\text{ref}}}{L} \) used to compensate the loop. Based on small-signal model of functions have the same pole with different gains.

Steps.

This indicates great stability toward input/output voltage is 32.5k rad/s, while the phase margin is 96.5 degrees.

According to Fig. 10, the cross-over frequency \( \omega_{\text{cross}} \) is 32.5k rad/s, while the phase margin is 96.5 degrees. This indicates great stability toward input/output voltage steps.

Differential functions of \( (20) \) and \( (22) \) are given by

\[
\begin{align*}
\dot{v}_o &= \frac{1}{sC}(i_{o,av} - \frac{v_o}{R}), \\
\dot{v}_{o,av} &= -\frac{i_{o,av}}{v_o}, \\
\dot{i}_{o,av} &= \frac{v_o}{v_{\text{in}}} - \frac{i_{o,av}}{2v_o}.
\end{align*}
\]

Finally, small signal model of the system is derived as

\[
\begin{align*}
\dot{v}_o &= G_{vi}(s)\dot{v}_{\text{ref}} + G_{vg}(s)v_{\text{in}} + G_{vf}(s)\dot{R}, \\
G_{vi}(s) &= \frac{v_o}{v_{\text{in}}}, \\
G_{vg}(s) &= \frac{1}{2v_o sRC + 2}, \\
G_{vf}(s) &= \frac{1}{R sRC + 2}.
\end{align*}
\]

The small signal model is first-order, and all transfer functions have the same pole with different gains.

In order to improve the system stability, a PI compensator is used to compensate the loop. Based on small-signal model of the converter, the PI compensator is optimized as \( P = 0.136 \) and \( I = 1936 \). Furthermore, the open-loop bode plot is given in Fig. 10.

IV. SIMULATIONS AND EXPERIMENTS

Simulations are carried out in MATLAB/Simulink to derive the curves of optimal VS/ZVS time versus \( v_{\text{in}} \) and \( v_o \). Specifications of the parasitic capacitors are obtained by datasheets of the experimental components. An experimental prototype, as shown in Fig. 11(b), is built to verify the proposed model and controller. Curves of the derived VS/ZVS time versus \( v_{\text{in}} \) and \( v_o \) based on piecewise equivalent capacitance model and constant capacitance model are given first. Then, comparisons of voltages and currents between analytical solution and experimental results are given to verify the effectiveness of proposed model and controller. Efficiency comparison is also given with respect to different voltage levels.

The curves of \( C_{\text{oss}} \) and \( C_j \) with respect to junction voltage is given in Fig. 1, where the main switching component is a GaN HEMT from GaNSystem (GS66508T) [9] and a SiC diode from ST (STPSC8H065) [10]. The SiC diode is used to match the switching frequency while eliminates the reverse recovery current.

Main specifications of the prototype are given in Table 3. Two ADC (LTC2314-14) modules are used to convert the analog values to digital signals. Digital value of input/output voltage are received and processed by a FPGA (Cyclone IV) board, as shown in Fig. 11(a). A 1µF capacitor (MP105J6241120) and a 0.1µF bypass capacitor are adopted as the output capacitor. The core material of inductor is PQ2016-3F36 from FERROXCUBE, which is suitable for operation frequency below 1MHz.

The input/output current and voltage and the efficiency are measured by power analyzer PA5000H. The measure range of input/output voltage is 300V/600V with absolute error of 0.01V. With a rated range of 5A current measurement board, the measure range of input/output current is set as 2.5A/1A with absolute error of 0.001A. The final efficiency measurement accuracy error provided by the power analyzer is 0.05%.
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FIGURE 12. Curves of VS/ZVS time versus \(v_{\text{in}}\) and \(v_{\text{o}}\) for VS/ZVS based on (a) piecewise equivalent capacitance model and (b) constant capacitance model.

FIGURE 13. Curves of \(t_{\text{ch}}\) versus \(v_{\text{in}}\) and \(v_{\text{o}}\).

A. \(t_{\text{ch}}\) AND \(t_{\text{VS/ZVS}}\)

Curves of optimal VS/ZVS time versus \(v_{\text{in}}\) and \(v_{\text{o}}\) based on piecewise equivalent capacitance model and constant capacitance model are given in Fig. 12(a) and Fig. 12 (b). Within all \(v_{\text{in}}\) and \(v_{\text{o}}\) range, \(t_{\text{VS/ZVS}}\) based on constant capacitance model is from 150ns to 410ns. However, it varies from 210ns to 490ns based on piecewise equivalent capacitance model, which shows considerable differences compared with that based on constant capacitance model. Furthermore, the VS/ZVS boundary is no longer \(2v_{\text{in}} = v_{\text{o}}\), as shown in Fig. 12 (a).

As shown in Fig. 13, curves of \(t_{\text{ch}}\) with \(v_{\text{in}}\) and \(v_{\text{o}}\) are plotted, where \(t_{\text{ch}}\) varies within 25ns. Adding \(t_{\text{ch}}\) to \(t_{\text{VS/ZVS}}\) gives \(t_{\text{ext}}\). With the derived extended off-time, experimental comparisons are given with respect to different capacitance equivalent method.

B. EFFECTIVENESS OF THE ANALYTICAL SOLUTIONS

In order to compare the effectiveness of the mentioned capacitance equivalent methods, experiments are given with respect to two output voltage levels at output power of 200W.

Under the proposed EOT control, the experimental prototype works at different voltage situations, where the currents and voltages are given in Fig. 14 and Fig. 15. As indicated in Section II, when \(2v_{\text{in}} = v_{\text{o}},\) ZVS should be achieved according to conventional constant capacitance model. However, when \(v_{\text{in}} = 200\text{V}\) and \(v_{\text{o}} = 400\text{V}\) shown in Fig. 14(a), the valley voltage is 20V, which means that the resonant process derivates from typical sinusoidal waveform. Fig. 14(b) gives the boundary condition of VS and ZVS, where \(v_{\text{in}} = 165\text{V}\) and \(v_{\text{o}} = 400\text{V}\). Fig. 14(c) gives a ZVS condition when \(v_{\text{in}} = 135\text{V}\) and \(v_{\text{o}} = 400\text{V}\). When \(v_{\text{in}} = 182\text{V}\) and \(v_{\text{o}} = 320\text{V}\) shown in Fig. 15(a), the valley voltage is 30V and the achieved \(t_{\text{VS}} = 310\text{ns}\). For conventional constant capacitance model, the VS/ZVS boundary satisfies \(2v_{\text{in}} = v_{\text{o}}\). However, Fig. 15 (b) gives the boundary condition of VS and ZVS, where \(v_{\text{in}} = 134\text{V}\) and \(v_{\text{o}} = 320\text{V}\). Fig. 15(c) gives a ZVS condition when \(v_{\text{in}} = 135\text{V}\) and \(v_{\text{o}} = 400\text{V}\). These figures show that the CRM operation at steady state is achieved with suitable \(t_{\text{ext}}\).

Furthermore, the achieved \(t_{\text{VS/ZVS}}\) is measured for the comparison with the calculated \(t_{\text{VS/ZVS}}\), as shown in TABLE 4. The calculated \(t_{\text{VS/ZVS}}\) based on piecewise equivalent capacitance model deviates from the experimental results within 5ns. In practice, errors within 5ns are accurate enough to achieve VS/ZVS. Comparatively, the calculated \(t_{\text{VS/ZVS}}\) based on the conventional constant capacitance model deviates from the experimental results within 72ns. Obviously, the results by conventional model has unacceptable accuracy for VS/ZVS.

C. EFFICIENCY COMPARISON AND LOSS BREAKDOWN

The accuracy of extended off-time directly affects the overall efficiency of the system. In the followings, efficiency comparisons are given with respect to \(t_{\text{ext}}\) by the proposed piecewise equivalent capacitance model and conventional constant capacitance model.

The efficiency comparisons at rated power of 200W is given in Fig. 16. The highest efficiency of 99.15% is achieved at a ZVS situation where \(v_{\text{in}} = 150\text{V}\) and \(v_{\text{o}} = 400\text{V}\.

| \(v_{\text{in}}\) | \(v_{\text{o}}\) | Experimental results | Proposed model (errors with experiments) | Conventional model (errors with experiments) |
|---|---|---|---|---|
| 400V | 200V | 320ns | 315ns (+6ms) | 252ns (+60ns) |
| 400V | 165V | 340ns | 342ns (+2ns) | 271ns (+69ns) |
| 400V | 135V | 375ns | 380ns (+5ns) | 303ns (+72ns) |
| 320V | 182V | 310ns | 307ns (+3ns) | 270ns (+40ns) |
| 320V | 134V | 355ns | 360ns (+5ns) | 287ns (+68ns) |
| 320V | 120V | 370ns | 374ns (+4ns) | 309ns (+61ns) |
Similar efficiency trend is achieved with respect to input voltage when \( v_o = 320V \) and \( v_o = 400V \), as shown in Fig. 16(a) and Fig. 16(b). When \( v_{in} > 160V \), VS is achieved. Although the valley voltage increases as \( v_{in} \) increases, the reduced efficiency with piecewise equivalent capacitance model (labeled as piecewise capacitance model) is always less than that with constant capacitance model. When \( v_{in} < 160V \), ZVS is achieved. However, the average input current increases as \( v_{in} \) decreases, which lead to higher conduction loss.
To quantify the changes of each losses, loss breakdown is given in Fig 17. It shows that higher switching frequency leads to higher switching loss under constant capacitance model (labeled as constant model), where additional switching loss of 0.848W is induced compared with piecewise equivalent capacitance model (labeled as piecewise model). When \( V_n \) reduces, the input current rises up, which induces higher inductor loss. This result indicates that switching loss can be greatly reduced with piecewise equivalent capacitance model, where the VS/ZVS is achieved. As a result, obvious overall efficiency improvement under piecewise model is achieved compared with that under constant capacitance model.

**V. CONCLUSION**

This article proposes a piecewise equivalent capacitance model to derive the analytical solutions of the resonance between inductor and parasitic capacitors in a CRM boost converter during VS/ZVS time. Compared with the conventional constant capacitance model, the proposed model can properly describe the resonance behaviour of parasitic capacitors. With the derived solutions, the optimal VS/ZVS time is calculated. This result is implemented in an extended off-time controller, which achieves CRM operation in a boost converter without ZCD module. Experimental results show that the VS/ZVS time calculated by the proposed model is accurate enough to achieve VS/ZVS in practice. As a result, a peak efficiency of 99.15% is achieved at power level of 200W and obvious overall efficiency improvement under piecewise model is achieved compared with that under constant capacitance model.

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