Electron conduction through quasi-one-dimensional indium atomic wires on silicon

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Electron conduction through quasi-one-dimensional (1D) indium atomic wires on silicon (the Si(111)-4\times1-In reconstruction) is clarified with the help of local structural analysis using scanning tunneling microscopy. The reconstruction has a conductance per square as high as 100 µS, with global conduction despite numerous surface steps. A complete growth of indium wires up to both the surface steps and the lithographically printed electrodes is essential for the macroscopic transport. The system exhibits a metal-insulator transition at 130 K, consistent with a recent ultraviolet photoemission study [H. W. Yeom, S. Takeda, E. Rotenberg, I. Matsuda, K. Horikoshi, J. Schaefer, C. M. Lee, S. D. Kevan, T. Ohta, T. Nagao, and S. Hasegawa, Phys. Rev. Lett. 82, 4898 (1999)].

The downsizing of microelectronics in pursuit of high density and high speed has brought them into the nanoscale regime in terms of their dimension. Suppose that the components of nanoelectronics, fabricated on a substrate, are further reduced in size to an extent that they are monatomically thin. These are nothing else than surface atomic structures, which often lead to reconstructions whose crystallographic and electronic properties are essentially distinct from their original bulk materials. Thus, understanding electron conduction properties of surface structures is of fundamental importance in the future nanoelectronics. In spite of its long history, interest in electron transport phenomena originating from well-defined surface reconstructions has been renewed only recently. To measure such conduction, two main difficulties must be overcome: 1) separating out conduction through the underlying subsurface space charge layer and 2) establishment of reliable electrical contacts to the atomic structures that are stable over a wide temperature range. Furthermore, as electron conduction through surface atomic structure is assumed to be grossly affected by defects, local structural analysis is essential to clarify their unambiguous transport properties.

In this paper an unprecedented combination of conductivity measurements and scanning tunneling microscopy clarifies electron transport properties of the Si(111)-4\times1-In reconstruction. This system is particularly interesting because it consists of quasi-one-dimensional (1D) indium wires on a silicon surface. We extract surface conduction through the comparison of two surface structures, one of which includes intentionally introduced defects. Indium atomic wire arrays have a global conductance per square as high as 100 µS despite numerous surface steps. A complete growth of atomic wires up to both the surface steps and the lithographically printed electrodes is found to be essential for conduction over macroscopic lengths. We find a metal-insulator transition at 130 K, consistent with a recent ultraviolet photoemission study [H. W. Yeom, S. Takeda, E. Rotenberg, I. Matsuda, K. Horikoshi, J. Schaefer, C. M. Lee, S. D. Kevan, T. Ohta, T. Nagao, and S. Hasegawa, Phys. Rev. Lett. 82, 4898 (1999)].

All experiments are performed under ultrahigh vacuum (UHV) conditions. Non-doped Si(111) (resistivity $\rho > 1000 \ \Omega \ \text{cm}$) is chosen as the substrate to minimize the electron conduction through the bulk. Tantalum, a typical refractory metal, is adopted as the electrode material to avoid diffusion during high temperature sample treatments. Two electrode pads separated by 1 mm are deposited beforehand on the sample with an electron beam evaporator (the inset of Fig. 1(b)). After load-
ing into the UHV chamber, the samples are cleaned by flashing at 1150 °C for 30 s. Indium is then deposited to a thickness of 1.8 monolayers (ML), followed by annealing around 450 °C for 5 minutes. This develops indium atomic wire arrays on a silicon surface (Si(111)-4×1-In reconstruction). The 4×1 reconstruction is confirmed over an extensive area by Low Energy Electron Diffraction (LEED). Local structures are observed with STM at room temperature, revealing defects in the wires, surface steps and domain boundaries. We find two classes of samples in terms of structural growth; I) complete and II) incomplete growth of indium atomic wires near the surface steps. Figures 1(a) and 1(c) show representative STM images respectively. After indium deposition, annealing at a temperature slightly higher than that required for complete growth strips off indium from the step edges. Thus, growth of the reconstruction at steps is controllable, and is homogeneous within the area of electron conduction.

Voltage-biased dc two-probe measurements are conducted after STM observation. Two spring-loaded gold-coated probes are pressed onto the electrodes to insure stable and reliable electrical contacts (the inset of Fig. 1(b)). The current-voltage (I−V) characteristics are linear for −1 V < V < 1 V over a wide temperature range, confirming the absence of a Schottky barrier at the electrode interfaces. The temperature dependence of conductivity is measured between room temperature and 6 K. No contamination is apparent in the STM images after the cooling cycles. The carriers in the bare silicon substrates are found to be quenched below 220 K. This allows the selective detection of electrical conduction originating from the surface structures: the possible conduction path is either the surface reconstruction or the underlying subsurface space charge layer.

We clarify electron conduction through the Si(111)-4×1-In reconstruction through the comparison of the two sample classes (I, II). Figure 1(b) shows the temperature dependence of conductivity (σ) of a representative class I sample (solid line) σ exhibits a broad maximum around 160 K with decreasing temperature, followed by a significant drop below 130 K. This drop indicates a dramatic change in the conduction mechanism. Complete growth of indium wires right up to the surface step (Fig. 1(a)) suggests that conduction is through both the surface reconstruction and the subsurface space charge layer in the class I samples. Destruction of the indium wires at steps edges should eliminate the surface conduction, leaving only the subsurface conduction. Figure 1(d) exemplifies the temperature dependence of conductivity of the class II samples. While the overall behavior is similar to that of the class I samples, the sudden decrease in σ below 130 K is absent. The value of σ above 130 K is also significantly lower than that of the class I samples (see the dashed line in Fig. 1(b) as an eye guide). This difference is not due to change in space charge layer conduction caused by different structural growth at steps, because this would lead to a rather uniform shift in σ across the entire temperature region. Thus we conclude that the gray region of Fig. 1(b) is the contribution from the surface atomic wires; the conductivity is approximately 100 μS. The sudden decrease in σ below 130 K is ascribed to a change in the surface conduction mechanism.

We confirm that the residual conductivity found in the class II samples (Fig. 1(d)) is the contribution of the subsurface space charge layer. The variation of σ can be well described by the equation

$$\sigma = C \exp(-E_g/k_BT)T^{-\alpha}$$

where C is a constant and $E_g$ and α are parameters. By curve fitting, one obtains $E_g = 39.7$ meV and α = 2.89. The fitting curve (dashed line in Fig. 1(d)) fully supports the experiment. The diagram of Fig. 1(d) (inset) illustrates the origin of these parameters. Because of the different Fermi levels between the surface Si(111)-4×1-In reconstruction and the silicon substrate, the silicon bands bend upwards near the surface. This induces hole carriers in the subsurface space charge layer. $E_g$ is attributed to the energy difference between the Fermi level and the upper bound of the silicon valence band near surface, representing the activation energy for holes. The term $T^{-\alpha}$ in equation (1) corresponds to the power-law $T$-dependence of the hole mobility. The value $E_g = 39.7$ meV is consistent with a previous report and the value α = 2.89 is close to α = 2.20, 2.42 for p- and

![FIG. 2: (a) An STM image of the sample with the Si(111)-4×1-In reconstruction in the first measurement. (b) An STM image of the sample in the second measurement. Inset: magnified image of an indium-induced defect. (c) The temperature dependence of conductivity of a sample with the Si(111)-4×1-In reconstruction in two consecutive measurements. Solid line: first measurement on the sample with a complete reconstruction (see (a)). Dashed line: second measurement on the sample with defects in the middle of the wires (see (b)). The difference between the two measurements is the contribution from the surface reconstruction (dotted-dashed line, five-times magnified).](image)
n-type silicons respectively. Once the band bending is determined, one can estimate the conductivity ($\sigma$) of the space charge layer using the reported silicon mobility. At room temperature, $\sigma$ is estimated to be 170 $\mu$S, consistent with the measured value 300 $\mu$S considering that the conductivity of the substrate (70 $\mu$S) is included at room temperature. Thus we conclude that the electron conduction in the class II samples is dominated by the subsurface space charge layer.

We have demonstrated electron conduction through surface reconstruction by intentionally destroying wires at steps, while their quantitative temperature dependence remains undetermined. To clarify this, we extract surface conduction by introducing defects in the middle of the wires on the same sample. A metal-insulator transition of this system is observed via transport experiments. First, a complete Si(111)-4x1-In reconstruction is formed with negligible defects (Fig. 2(a)). The conductivity $\sigma$ shows a significant decrease at 130 K (Fig. 2(c), solid line). After returning to room temperature, a small amount of indium (0.04 ML) is additionally deposited without any sample annealing. This process induces defects in the middle of the indium wires (Fig. 2(b)). In the second conductivity measurement (Fig. 2(c), dotted line), $\sigma$ is significantly decreased compared to the first above 130 K, while the two measurements collapse to a single curve below 130 K. Because electron conduction is suppressed by defects in the wires, the difference between the two (Fig. 2(c), dotted-dashed line) is the contribution of the surface reconstruction. It gradually decreases with decreasing temperature, followed by a sudden drop at 130 K. Below 120 K, conduction of the indium wires ceases, showing that the system is in the insulating phase.

Let us note that the electron transport phenomenon revealed here originates from the unique surface state of Si(111)-4x1-In reconstruction. A thin indium film on a silicon surface with bulk-like electronic states would not exhibit this change. The result is in agreement with a phase transition recently found by Yeom et al. They clarified that the system undergoes a transition around 130 K accompanied by gap opening at the Fermi level, leading to periodic modulation of lattices and charges below the transition temperature. Although its mechanism is still under debate, it is clear from our finding that the system undergoes a metal-insulator transition.

Although macroscopic surface electron conduction through steps and domain boundaries seems remarkable, this has been confirmed for the Si(111)-$\sqrt{3} \times \sqrt{3}$-Ag reconstruction in a similar configuration. The surface steps and domain boundaries may be the main sources of resistance in surface conduction, but the present experiment suggests that the conductivity is generally quite high as far as the surface reconstruction grows up to the steps. However, disruption of the reconstruction near steps can significantly enhance their resistance. This is possible if electron transfer between adjacent terraces is due to tunneling. In this case, only a small change in tunneling gap distance will lead to substantial enhancement of resistance.

One other factor significantly affects the global transport through the surface reconstruction: the electrode-indium wire interface. Figure 3 shows an STM image of the interface between the indium wires and a test tantalum pad. The surface reconstruction has grown up to the edge of the pad. FIG. 3: An STM image of the interface between the indium wires and a test tantalum pad. The surface reconstruction has grown up to the edge of the pad.

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13 Figure 1(a) contains another slightly thicker phase on the upper side of the step. This structure is different from the $\sqrt{7} \times \sqrt{3}$ reconstruction, and has been called ‘striped structure’. In addition, more defects in indium wires are visible in Fig. 1(c) than in Fig. 1(a).
14 Macroscopic electron conduction through the Si(111)-4×1-In is nearly isotropic despite its local 1D structure; domains with different wire directions coexist due to the three-fold symmetry of the reconstruction. The unit of surface conductivity is siemens (S), the same as that of conductance. This is because the conductance of a square sheet is independent of its size.
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