The power-delay product and its implication to CMOS Inverter

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Abstract. Due to power dissipation has always been a significant standard for low power VLSI design, as a parameter that could reflect both circuit power consumption and delay, Power-Delay Product is of great research value. This paper mainly explores the working principle of CMOS inverter, and the definition, and formation causes of PDP. Two experiments were designed based on LTspice for investigating the effect of width to length ratio of the channel of transistors and the stack approach on the propagation delay and dynamic dissipation of CMOS inverter. It is verified that the propagation delay of the inverter is just related to the ratio of the width of the channel between NMOS and PMOS transistors. It is also verified that the range of ratios of the width of the channel between two transistors which makes the propagation delay and PDP minimum is 2~4, and the stack approach could reduce the PDP in the CMOS inverter effectively.

1. Introduction

1.1. Research Background and Meaning
The processing power of chips doubles every two years, according to Moore's law, so the chip-fabrication technology has been advancing at a rapid pace. The Smaller size and faster computing speed have always been the goals of engineers in chip design. As VLSI technology is upgrading, not only the geometry of integrated circuits continues to shrink to the nanoscale, but the number of transistors per chip has also increased dramatically. However, the smaller size of the chip results in the channel length of a single Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) in the Integrated Circuit(IC) is reduced accordingly and the increase in power dissipation and an increase in the number of transistors may also lead to an increase in overall chip delay. Therefore, power consumption and delay time have been the top concerns of VLSI circuit design, for which Complementary Metal-Oxide-Semiconductor Transistor(CMOS) is the primary technology[1].

As the name implies, Power-Delay Product(PDP) is the product of power consumption and delay, which can reflect both parts of dynamic power dissipation and propagation delay of the system, it balances the performance and energy consumption and is mainly used to determine the performance of the digital integrated circuit. As a result, it is an extremely valuable research object in integrated circuit design, this paper will also discuss it based on conventional CMOS inverter.

1.2. Research Content of this paper
This paper is organized in this way: Section 2 describes the structure and working principle in CMOS inverter, and its transfer characteristics. Section 3 presents the definition, formation causes and
formula derivation of power consumption and propagation delay and the PDP, and two major methods for reducing the PDP in CMOS inverter. Section 4 illustrates experimental methodology with experimental contents and variables, and the experimental data. In the end, section 5 summarizes the research with its conclusion of the experiment and points out the weakness of this research.

2. Conventional CMOS Inverter

2.1. Structure and Working Principle of CMOS Inverter
CMOS inverter is one of the common basic circuits in CMOS logic gate circuits, and it is also an important unit of the integrated circuit to achieve complex logic functions. Fig.1 illustrates the conventional CMOS inverter circuit, and it consists of a pull down N-channel Metal Oxide Semiconductor (NMOS) and pull up P-channel Metal Oxide Semiconductor (PMOS), and the PMOS is connected to Voltage Drain Drain (VDD) and the NMOS is connected to the ground. CMOS logic is complementary. That means that the ideal state of two transistors at a time is that only one transistor will conduct, either pull up or pull down[2]. Therefore, the basic function of the inverter is to reverse the input signal and output it.

2.2. The Transfer Characteristic of CMOS Inverter
Fig.2 shows the realistic transfer characteristic of the inverter. It is obvious that when the transistor switches between fully on and fully off, the transistor will operate in the saturation region. When two transistors are simultaneously operating in the saturation zone, a large current will flow through the inverter since the two transistors are simultaneously conducting, which is the important reason for the dynamic dissipation of the inverter and will also affect its delay time.

3. Power-Delay Product in CMOS Inverter

3.1. Power Dissipation in CMOS Inverter
Power dissipation in the circuit is defined as the rate at which the energy is taken from the source and is converted to heat[3]. There are three main types of power consumption in CMOS circuits: leakage power, short circuit power, and dynamic power.

1) Leakage Power: The leakage power is static, and it is mainly determined by the current flowing through the channel when the transistor is off, which is generally very small[4].

The technique leakage power is given as:

\[ P_{\text{leakage}} = V_{DD} \sum_{i=1}^{n} I_{DS} \]  \hspace{1cm} (1)

Where \( I_{DS} \) is the current flowing through the channel in the \( i_{th} \) transistor.

2) Short Circuit Power: Short-circuit power refers to the power consumption caused by the current flowing through the NMOS and PMOS when these two thyristors switch and simultaneously conducting[7]. It can be limited by modifying the slope of the input signal. The short circuit power is known as:

\[ P_{\text{short-circuit}} = I_{\text{mean}} V_{DD} \]  \hspace{1cm} (2)
Where  $I_{\text{mean}}$ is the average short-circuit current.

3) Dynamic Power: Dynamic power is the dissipation caused by charging and discharging of a load capacitance when transistors switch, it is directly related to the power-delay product. Without considering the subthreshold current, dynamic power determines the inverter power consumption. The technique for dynamic power is specified by

$$P_{\text{dynamic}} = \kappa C_L V_{DD}^2 f$$

(3)

Where  $f$ is the clock frequency and  $\kappa$ is the node transition activity factor.

3.2. Propagation Delay in CMOS Inverter

1) Definition of Propagation Delay:

Propagation delay is defined as the time between the input signal becoming 50% VDD and the output signal becoming 50% VDD, therefore, it consists of two parts, low-to-high transition delay, and high-to-low transition delay. Fig.3 shows these two transition delays and the propagation delay can be expressed in the following formula that

$$t_{pd} = \frac{t_{pHL} + t_{pLH}}{2}$$

(4)

Where  $t_{pLH}$ is the low-to-high transition delay and  $t_{pHL}$ is the high-to-low transition delay.

2) Formation Causes of Propagation Delay: The propagation delay is caused by the presence of the load capacitance of the inverter. Taking the charging process of load capacitance as an example, its equivalent first-order circuit is shown in Fig.4. When the input signal is a step signal, according to the first-order circuit analysis method, it is easy to get the charge time of the load capacitance. The discharge time is known as

$$t_{pLH} = \ln(2) R_{\text{eq}} C_L = 0.69 R_{\text{eq}} C_L$$

(5)

Where  $R_{\text{eq}}$ is the equivalent resistance of PMOS. The derivation of  $t_{pHL}$ is the same as that of  $t_{pLH}$, so according to formula 4, the propagation delay is shown as

$$t_{pd} = 0.69 C_L \left( \frac{R_{\text{eqH}} + R_{\text{eqL}}}{2} \right)$$

(6)

3.3. The Definition and Derivation of Power-Delay Product

1) Definition: PDP is defined as the product of power and delay, it indicates the average energy consumed per switching event, so it is a fundamental parameter which is often used for measuring the quality and the performance of the CMOS process[3].

2) The Derivation of Formula: Fig.5 shows waveforms of the charging voltage at both ends of the capacitance and the charging current. According to the equivalent circuit diagram shown in Fig.4 and the first-order circuit analysis method, it is easy to obtain the stored energy on the capacitance during charging. The stored energy is shown as

$$E = \frac{1}{2} C_L V_{DD}^2$$

Figure 3. Low-to-high and high-to-low transition delays

Figure 4. The equivalent first-order circuit of load capacitance during charging
Figure 5. The curve of output voltage and charging current when a load capacitor is charged

(a) the charging voltage waveform, (b) the charging current waveform

According to the characteristics of the first-order circuit, the energy consumed by the resistance during the charging process of capacitance is equal to the energy stored in the capacitance. Therefore, according to the definition of PDP, it is easy to get its calculation formula, and it is specified by

\[ E_C = \int_0^{t_{frast}} i_{ppd}(t)v_{out}dt = \int_0^{t_{frast}} C_L \frac{dv_{out}}{dt}v_{out}dt = \frac{1}{2} C_L V_{DD}^2 \]

(7)

Where \( f_{frast} \) is the maximum switching frequency of a gate.

3.4. The Solutions to Reduce the PDP

Generally, the method of reducing PDP in CMOS inverter can be discussed from two aspects: adjusting transistor structure and optimizing circuit structure. The following sections focus on two solutions.

Solution from the Adjusting Transistor Structure: According to formula 8, the value of PDP is related to power supply voltage \( V_{DD} \), load capacitance \( C_L \) and propagation delay \( t_{pd} \). Due to the change of \( V_{DD} \) and \( C_L \) will affect both the dynamic dissipation and the propagation delay of the transistor, it is more convenient to consider the solution from the aspect of propagation delay.

The main method discussed is to change the width to length ratio of the transistor. Increasing the ratio of width to length of the transistor could reduce its resistance, thus reducing the charging and discharging time of the load capacitance and the propagation delay of the inverter. For consideration of the voltage transmission characteristics of inverters, the channel of PMOS is generally set wider so that its resistance matches the resistance of the pull-down NMOS to ensure that \( t_{pdd} \) and \( t_{pnh} \) are equal. It is generally required that the width of the channel of PMOS is 3~3.5 times that of NMOS.

Meanwhile, due to all transistors are connected in series between the VDD and Ground(GND), it forces the length of the inverter to increase.
4. Experimental Methodology

In this section, the experimental contents, the establishment of the experimental platform, the experimental variables, and the main measured experimental data of the two designed experiments are introduced respectively. And then the experimental results of delay and dynamic dissipation obtained in these experiments are displayed. The technological size of the experimental transistor was selected as 0.25\text{um}.

4.1. The Experimental Contents

According to the methods of PDP reduction mentioned at the end of section 3, two experiments are designed based on LTspice in this paper.

1) Experiment about the Width to Length Ratio of Transistors: To investigate the relationship between the width to length ratio and the propagation delay, and find out the appropriate range of this ratio that achieves the minimum delay, the channel length and width of the two transistors are initially set to 0.25\text{um} and 1.5\text{um}. Firstly, the width of the channel of NMOS is kept unchanged and the width to length ratios of the channel of PMOS are set to 4, 5, 6, 8, 10 respectively. Then, the two transmission delays and dynamic dissipation of the inverter after the simulation experiment were measured. Secondly, the width of the channel of PMOS is kept unchanged and the channel width to length ratios of NMOS are set to 4, 5, 6, 8, 10 respectively. Then, the same experimental data were recorded. Finally, the ratios between the width of the channel of PMOS and NMOS are set to 4:1, 3:1, 2:1, 1:1 respectively. Then, the same experimental data were recorded.

2) Experiment about the Stack Approach: To investigate the improvement effect of the stack approach on the PDP in the inverter, firstly the channel length and width of two PMOS transistors are set to 0.25\text{um} and 0.75\text{um} (W/L=3) and the channel length and width of two NMOS transistors are set to 0.25\text{um} and 0.375\text{um} (W/L=1.5). Then the two transmission delays and dynamic dissipation of the inverter after simulation were measured. Secondly, based on the experiment above, the channel width to length ratio of NMOS and PMOS and the ratios of the width of the channel between NMOS and PMOS were respectively changed to study the changes of propagation delay, dynamic dissipation, and PDP. The channel width to length ratios of NMOS are set to 1, 2, 3 respectively and the ratios between the width of the channel of PMOS and NMOS are set to 4:1, 3:1, 2:1, 1:1 respectively. Then the two transmission delays and dynamic dissipation of inverter at different situations were recorded respectively.

4.2. The Establishment of the Experimental Platform

Based on LTspice, two different experimental platforms were established in these experiments: the conventional CMOS inverter and the inverter using the stack approach as shown in Fig.7. The amplitude of power source VDD is set to 0.5V, and the input signal of the inverter is the ideal square wave signal, with the amplitude set at 0.5 V, the period set at 100ns, and the high potential duration set at 50ns. In this experiment, the dynamic consumption and delay of the inverter are measured within one signal period.
4.3. The Experimental Variable
In this experiment, the channel width of the transistor is selected as the sole experimental variable, and the channel length of the transistor is guaranteed to remain constant. The width to length ratio of the transistor is changed by adjusting the channel width of the transistor.

4.4. The Main Measured Experimental Data
1) Propagation delay: According to the definition of the propagation delay, it is measured from the trigger input edge reaching 50% of the supply voltage to the circuit output edge reaching 50% of the supply voltage in this experiment[5].

2) Dynamic dissipation: According to the features of dynamic dissipation, the average power dissipation of transistors in one switching event as the estimation of dynamic consumption[5].

4.5. Experiment Results
First need to statement, as shown in each table, most experimental data of propagation delays are negative. Because all transistors used in this experiment are ideal. When the transistors do not set the channel width and length, there is no propagation delay between the output signal and the input signal. So when the channel width of the transistor is adjusted, one of the and will always go down, so there will always be negative delay time. Therefore, this does not mean that the experimental data are wrong.

By observing the positive and negative signs of the sum of and the changing trend of propagation delay can be judged when the channel width of the transistor changes. If the sum of and is positive, the propagation delay of the inverter is increased, otherwise, the propagation delay is decreased.

To analyze the change of PDP clearly, this paper assumes that the initial propagation delay of the conventional inverter used in the experiment is 200ps, to ensure that all the propagation delays obtained in each experiment are positive.

1) The Result of Experiment about the Width to Length ratio of transistors: Table 1 shows the delay time and dynamic dissipation corresponding to the different width of the channel of PMOS. When the width of the channel of NMOS remains constant, with the increase of the width of the channel of PMOS, the value of increases, while that of decreases gradually. Meanwhile, when the ratio of PMOS and NMOS channel width is equal to 1, the delay time is the maximum, while when the ratio is less than or greater than 1, the delay time will decrease with the adjustment of the channel width of the transistor. And with the increase of the width of the channel of PMOS, the power consumption also increases, which is caused by the decrease of the equivalent resistance of the transistor. The variation trend of PDP is roughly the same as that of the propagation delay shown in Fig.8.

Table 2 shows the delay time and dynamic dissipation corresponding to the different width of the
channel of NMOS. When the width of the channel of PMOS remains constant, with the increase of the width of the channel of NMOS, the value of \( t_{\text{pLH}} \) increases gradually, while that of \( t_{\text{pHL}} \) decreases. With the increase of the width of the channel of NMOS, the power consumption also increases. The variation trend of PDP is roughly the same as that of the propagation delay shown in Fig. 9.

Table 1. Delay time and PDP with different widths of the channel of PMOS

| \( t_{\text{pLH}} \) (ps) | 4   | 5   | 6   | 8   | 10  |
|------------------------|-----|-----|-----|-----|-----|
|                        | 263.728 | 217.575 | 0.871 | -390.514 | -533.546 |

| \( t_{\text{pHL}} \) (ps) | -372.917 | -266.742 | 0.856 | 222.481 | 357.110 |

| Propagation Delay (ps) | 90.811 | 150.833 | 201.727 | 31.967 | 23.564 |

| Dynamic Dissipation (nW) | 21.424 | 23.001 | 29.639 | 43.387 | 49.098 |

| PDP (J) | 1.94 E-18 | 3.46 E-18 | 5.97 E-18 | 1.38 E-18 | 1.15 E-18 |

Table 2. Delay time and PDP with different widths of the channel of NMOS

| \( t_{\text{pLH}} \) (ps) | -458.713 | -229.597 | 0.871 | 224.362 | 358.923 |

| \( t_{\text{pHL}} \) (ps) | 255.909 | 217.121 | 0.856 | -304.878 | -534.356 |

| Propagation Delay (ps) | 1.178 | 187.524 | 201.727 | 119.484 | 24.567 |

| Dynamic Dissipation (nW) | 29.830 | 30.513 | 29.639 | 33.985 | 32.358 |

| PDP (J) | 3.51 E-20 | 5.72 E-18 | 5.97 E-18 | 4.06 E-18 | 7.94 E-19 |

Figure 8. The propagation delay and PDP with different widths of the channel of PMOS

Figure 9. The propagation delay and PDP with different widths of the channel of NMOS

Tables 3, 4, 5 show the delay time and dynamic dissipation corresponding to different ratios of NMOS and PMOS channel width when the NOMS channel length is changed. Propagation delay is rarely related to the ratio of channel width between PMOS and NMOS, however, the dynamic dissipation is different and the change rule is the same as described previously. And according to the data in these tables, when the ratio of NMOS and PMOS channel width is 3, and the ratio of NMOS...
and PMOS channel width which minimizes the propagation delay should range from 2 to 4. In this range, the PDP of the conventional inverter is also minimum.

Table 3. Delay time with different widths of the channel of PMOS (NMOS W/L=1)

|        | 1:1  | 2:1  | 3:1  | 4:1  |
|--------|------|------|------|------|
| \( t_{pLH} \) (ps) | 0.949 | -573.031 | -724.742 | -785.495 |
| \( t_{pHL} \) (ps) | 0.939 | 432.745 | 552.861 | 908.625 |
| Dynamic Delay (ps) | 201.888 | 59.714 | 28.119 | 323.13 |
| Dynamic Dissipation (nW) | 4.939 | 8.8259 | 9.796 | 11.762 |
| PDP (J) | 9.97E-19 | 5.27E-19 | 2.75E-19 | 3.80E-18 |

Table 4. Delay time with different widths of the channel of PMOS (NMOS W/L=2)

|        | 1:1  | 2:1  | 3:1  | 4:1  |
|--------|------|------|------|------|
| \( t_{pLH} \) (ps) | 0.949 | -573.031 | -724.742 | -785.495 |
| \( t_{pHL} \) (ps) | 0.939 | 432.745 | 552.861 | 908.625 |
| Dynamic Dissipation (nW) | 9.879 | 17.652 | 19.593 | 23.523 |

Table 5. Delay time with different widths of the channel of PMOS (NMOS W/L=3)

|        | 1:1  | 2:1  | 3:1  | 4:1  |
|--------|------|------|------|------|
| \( t_{pLH} \) (ps) | 0.949 | -573.031 | -724.742 | -785.495 |
| \( t_{pHL} \) (ps) | 0.939 | 432.745 | 552.861 | 908.625 |
| Dynamic Dissipation (nW) | 14.819 | 26.477 | 29.389 | 35.285 |

Figure 10. The propagation delay and PDP with different ratios of the width of the channel between PMOS and NMOS

2) The Result of Experiment about the Stack Approach: Table 6 shows the comparison of delay time and dynamic power dissipation between conventional inverter and inverter using the stack approach. When the ratio of the width of the channel between PMOS and NMOS is 6:3, the propagation delay of the inverter using the stack approach is greater than that of a conventional inverter. However, the dynamic dissipation of the inverter using the stack approach is far less than that of the conventional
inverter. It can be seen from Fig.10 that the PDP of the inverter using the stack approach is smaller than that of the conventional inverter, and it shrinks to about half that of the conventional inverter.

Table 6. The comparison of delay time and dynamic power dissipation between conventional inverter and inverter using the stack approach

|                      | Conventional Inverter | Inverter using the Stack Approach |
|----------------------|-----------------------|----------------------------------|
| $t_{PHL}$ (ps)       | -573.031              | -583.547                         |
| $t_{PLH}$ (ps)       | 432.745               | 483.599                          |
| Propagation Delay (ps)| 59.714                | 100.052                          |
| Dynamic Dissipation (nW)| 26.477              | 6.665                            |
| PDP (J)              | 1.58E-18              | 6.66E-19                         |

Figure 11. The comparison between traditional inverter and inverter using stack approach (a) The comparison of propagation delay, (b) The comparison of PDP

Table 7 shows the delay time and dynamic dissipation corresponding to different ratios of channel width between two PMOS transistors while their sum is constant. Obviously, with the increase of the ratios of channel width between two PMOS transistors, the delay time increases, and the dynamic dissipation decreases. It can be seen from Fig.12 that when the ratio of the width of two POMS channels is 4:2, the PDP of the inverter reaches the maximum.

Table 7. Delay time and dynamic dissipation with different ratios of the width of the channel between two PMOS transistors (PMOS: NMOS=6:3)

|                      | 3+3      | 3.5+2.5  | 4+2      | 4.5+1.5  |
|----------------------|----------|----------|----------|----------|
| $t_{PHL}$ (ps)       | -583.547 | -552.213 | -489.221 | -443.399 |
| $t_{PLH}$ (ps)       | 483.599  | 462.656  | 419.748  | 381.016  |
| Propagation Delay (ps)| 100.052  | 110.443  | 130.527  | 137.617  |
| Dynamic Dissipation (nW)| 6.665    | 6.543    | 6.120    | 5.121    |
| PDP (J)              | 6.66E-19 | 7.22E-19 | 7.98E-19 | 7.04E-19 |
Figure 12. The propagation delay and PDP with different ratios of the width of the channel between two PMOS transistors (P:N=6:3)

5. Conclusion

Based on CMOS inverter test results, the influence law of PMOS and NMOS channel width on propagation delay is firstly verified, the effects of those on the propagation delay of inverters are opposite. At the same time, the influence of transistor channel width on inverter dynamic dissipation is also obtained. The propagation delay and dynamic dissipation of the inverter are also investigated when the NMOS channel width to length ratio is different and the ratio of NMOS and PMOS channel width is different. It is found that the propagation delay of the inverter has nothing to do with the channel width to length ratio of each transistor, but depends on ratios of NMOS and PMOS channel width. And it is verified that when the ratios of NMOS and PMOS channel width is in the range from 2 to 4, the propagation delay and PDP of inverter might reach the minimum.

Meantime, the stack approach is adopted to change the circuit structure of the inverter, which effectively reduces the dynamic dissipation of inverter though delay time is sacrificed. In the case of little change of propagation delay, the PDP of the inverter using the stack approach is smaller than that of the conventional inverter, and the experimental results are achieved. It is also found that in the stack approach, when the sum of width to length ratios of the channel of two PMOS remains unchanged, but the ratios of the width of the channel between them change, the propagation delay will increase with the increase of the ratio of the width of the channel of the two PMOS transistors, and the dynamic dissipation will decrease. When the ratio of the width of the channel between two PMOS transistors is 2, the PDP of the inverter might reach the maximum, so this ratio should be avoided in the actual application of the stack approach in conventional CMOS inverter.

However, as the transistors used in this experiment are ideal components, the propagation delay and PDP in the inverter could not be accurately measured, and the changing trend of propagation delay and PDP are just compared relatively under different situations. Moreover, the ratio of the width of the channel of PMOS and NMOS which makes the propagation delay of inverter minimum is not accurately measured (its theoretical value is 2.4). This is left as future work.

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