Efficient FPGA implementation of high speed digital delay for wideband beamforming using parallel architectures

Gian Carlo Cardarilli¹, Luca Di Nunzio², Rocco Fazzolari³, Daniele Giardino⁴, Marco Matta⁵, Marco Re⁶, Sergio Spanò⁷, Lorenzo Simone⁸

¹,²,³,⁴,⁵,⁶,⁷University of Rome Tor Vergata, Via del Politecnico 1, 00133 Roma, Italy
⁸Thales Alenia Space Roma, Via Saccomuro 24-00131 Roma, Italy

ABSTRACT

In this paper, the authors present an FPGA implementation of a digital delay for beamforming applications. The digital delay is based on a Parallel Farrow Filter. Such architecture allows to reach a very high processing rate with wideband signals and it is suitable to be used with Time-Interleaved Analog to Digital Converters (TI-ADC). The proposed delay has been simulated in MATLAB, implemented on FPGA and characterized in terms of amplitude and phase response, maximum clock frequency and area.

Keywords:
Farrow filter
TI-ADC
Variable fractional delay
Wideband digital beamforming

Corresponding Author:
Luca Di Nunzio,
University of Rome Tor Vergata
Via del Politecnico 1, 00133 Roma Italy
Email: di.nunzio@ing.uniroma2.it

1. INTRODUCTION

The beamforming technique [1-5] is based on the combination of M different signals coming from M antennas. Such combination is obtained by delaying and summing the signals in order to produce additive interferences in some directions and destructive interferences in others.

In this application, the delay blocks represent a crucial element. When the beamforming involves narrowband signals, the delays can be realized with simple phase shifters, implemented with complex multipliers. Vice versa in case of wide-band signals, delay blocks must be implemented using more complex circuits [6-7]. A common solution consists in the use of fractional delay filters. These filters are able to generate delays, which are a fraction of the system clock cycle. In wideband applications, as for example wideband beamforming, the filters must comply with some specifications, namely:

a. Large bandwidth (ideally Nyquist frequency)
b. Reduced Magnitude ripple
c. Reduced Phase ripple
d. Ideally constant Group delay

These requirements can be easily met using the Weighted Least-Squares (WLS) method implemented with the Farrow architecture [8-13]. However, as the processing rate increases, e.g. more than 1 GHz, the hardware implementation could present some complications, for example the high sample rate that makes impossible the use of FPGAs. The reason is the impossibility of FPGAs to reach processing rates beyond the GHz. In fact, although modern Time-Interleaved ADCs [14-16] (TI-ADC) are able to provide wide-band signals with sample rates over the GHz, FPGAs are not able to process such signals without decimation and, consequently, without reducing the bandwidth of signals involved in processing [17, 18].
In this paper, the authors present an FPGA based digital delay for wideband digital beamforming. The proposed solution is able to reach preocessing rates compatible with actual TI-ADC. Such digital delay is based on Parallel FIR Filters which are used to compose a Parallel Farrow Filter.

2. RESEARCH METHOD

Farrow filters [19-21] represent the most common solution for the implementation of fractional delay filters. They are widely discussed in the literature and a detailed analysis is provided in [20]. In Figure 1 the block diagram of a Farrow filter is provided. The filter is composed of delay blocks, adders, multipliers (used for the selection of the delay entity) and M subfilters. Subfilters are represented in the figure with blocks named \( C_i(z) \) with \( 0 \leq i \leq M-1 \). As discussed in [3, 4], modern TI-ADCs for high speed/wide-band applications are usually composed of 2 or 4 ADC cores. Each core provides the output on a separate bus. All the cores work in parallel and the total sample rate of the ADC is the sum of the sample rates of the single cores.

In other words, the total sample rate is \( L \cdot f_{sa} \) where \( L \) is the number of cores and \( f_{sa} \) is the sample rate of each core. The idea of the proposed digital delay is to parallelize the Farrow architecture in order to process the incoming parallel data from the TI-ADC cores as shown in Figure 2. This is possible by parallelizing the sub-filters that compose the Farrow filter. The parallel architecture is based on polyphase filters banks [22, 23]. This technique allows to reduce the operating frequency by parallelizing the filters and, as consequence, could be used to reduce the system power consumption by acting on power supply [24].

To achieve such parallelization, we introduce a new polyphase architecture that we call Parallel-Polyphase. This architecture, differently from traditional polyphase architectures, is able to process data without any decimation and consequently without any bandwidth reduction.

Let's consider the impulse response \( c_i[n] \) of a generic sub-filter \( C_i \) composing the Farrow filter. In order to implement the architecture shown in Figure 2, each sub-filter must be parallelized by a factor equal to the number of TI-ADC available cores (Figure 2 shows the case of a TI-ADC composed by 4 cores). In the following, we get the equations for a generic parallel filter having \( L \) inputs and \( L \) outputs, where \( L \) is the number of the TI-ADC cores. We transform the discrete convolution of a classic SISO (Single Input, Single Output) FIR filter into a parallel convolution to model a MIMO (Multi-Input, Multi-Output) FIR Filter. A FIR filter is described by the discrete convolution:

\[
    y[n] = \sum_{i=0}^{N-1} x[n - i]c[i]
\]

where \( N \) is the length of the filter output and \( c[n] \) is the impulse response of \( C_i(z) \).
Applying a factor $L$ polyphase decomposition [25] to the output $y[n]$, we split the output in $L$ branches $y_k[n]$ with $k=0, 1, 2$ to $L-1$:

$$y_k[n] = y[Ln + k] = \sum_{i=0}^{N-1} x[Ln + k - i]c[i]$$

(2)

Note that each output $y_k[n]$ depends on every sample of the input sequence $x[n]$. Because TI-ADCs provide the inputs in parallel (each core has an independent bus), input $x[n]$ in the equation must also be parallelized. This is possible using a change of variables: $i=LM+l$ with $0 \leq l \leq L-1$ and $0 \leq m \leq M-1$ where $M$ is the length of the subfilters obtained by the polyphase decomposition of $c[n]$ [6]. The new equation of the model is shown in (3).

$$y_k[n] = \sum_{i=0}^{L-1} \sum_{m=0}^{M-1} x[Ln + (k - l) - Lm]c[LM + l]$$

(3)

(3) describes the $L$ outputs $y_k[n]$ in function of the $L$ inputs. In terms of Z transform we have:

$$Y_k(z^L) = \sum_{i=0}^{L-1} X_{K-i}(z^L) h_i(z^L)$$

(4)

where $Z[x[Ln + (k - l) - Lm]] = X_{K-i}(z^L)$ are the $L$ parallel inputs provided by the TI-ADC and $Z[c[LM + l]] = H_i(z^L)$ is the subfilter of $c[n]$. The term $X_{K-i}$ may have a negative subscript. For this reason, we consider $\beta=k-l$ and we rewrite $X_{L-1}$ with subscript between 0 and $L-1$:

$$X_\beta(z^L) = Z[x[Ln + \beta]] = Z[x[L(n-1)] + (L + \beta)] = X_{L+\beta}(z^L) z^{-L}$$

(5)

Consequently:

$$Y_k(z^L) = \sum_{i=0}^{k} X_{K-i}(z^L) h_i(z^L) + \sum_{i=k+1}^{L-1} X_{L+(k-i)}(z^L) h_i(z^L) z^{-L}$$

(6)

$$Y_{L-1}(z^L) = \sum_{i=0}^{L-1} X_{N-1}(z^L) h_i(z^L)$$
For example, choosing $L=4$, a generic filter $C_i(z)$ can be parallelized as shown in Figure 3. The polyphase sub-filters $H_i(z^L)$ are computed as shown in [6]. Note that the regularity of such architecture allows an easy scalability for any value of $L$.

![Figure 3. Parallel polyphase decomposition for L=4](image)

3. RESULTS AND DISCUSSION

The architecture of Figure 2 has been coded in VHDL and implemented on a XILINX XCVU9P-L2FLGA2104E FPGA [26]. After the hardware implementation, the digital delay has been tested injecting sinusoids at the input. Keeping a 16-bit resolution in the entire data-path (also inputs are represented with 16 bits) we obtain the following results:

a. Magnitude ripple < 0.2 dB.

b. Phase ripple < 2°.

c. Minimum delay 10 ps.

d. Maximum clock frequency (500 MHz)

The Farrow filter is composed by $M=5$ subfilters with a length of $N=11$. The maximum clock frequency of 500 MHz allows the reaching of 2 GSPS using 4 cores. In Figure 4 the magnitude and the phase error response in function of the delay are provided. Figure 5 shows examples of delay in the time domain.

| Resources | Utilization | Available | Utilization% |
|-----------|-------------|-----------|--------------|
| LUT       | 4,449       | 1,182,240 | 0.38%        |
| LUT RAM   | 784         | 591,840   | 0.13%        |
| FF        | 10,735      | 2,364,480 | 0.45%        |
| DSP       | 80          | 6,840     | 1.17%        |

Table 1. Resources utilization
4. CONCLUSION

In this paper, a digital delay for beamforming has been presented. The proposed digital delay is based on a parallel polyphase decomposition that can be easily implemented on FPGA or ASIC. Thanks to its regularity, this parallel polyphase decomposition can be easily generalized for any value of L. The introduced digital delay allows FPGAs to process wide-band signals without any decimation and consequently without any bandwidth reduction. We have shown an implementation’s example able to process a 2 GSPS signal using a TI-ADC with 4 cores and a 500 MHz clock frequency. The signals can be delayed of small quantities up to 10ps with Magnitude Ripple and Frequency Ripple respectively less than 0.2 dB and 2°.

REFERENCES

[1] Steyskal, Hans. “Digital Beamforming Antennas: An Introduction”. Microwave journal, 1987; 30 (1): pp. 10p between p 107 and 124
[2] R. Mucci, "A comparison of efficient beamforming algorithms," in IEEE Transactions on Acoustics, Speech, and Signal Processing, vol. 32, no. 3, pp. 548-558, June 1984.
[3] Malek, N.A., Khalifa, O.O., Abidin, Z.Z., Mohamad, S.Y., Abdul Rahman, N.A. Beam steering using the active element pattern of antenna array. Telkomnika (Telecommunication Computing Electronics and Control), 2018; 16(4): 1542-1550.
[4] M. Younis, C. Fischer and W. Wiesbeck, "Digital beamforming in SAR systems," in IEEE Transactions on Geoscience and Remote Sensing, vol. 41, no. 7, pp. 1735-1739, July 2003.
[5] D. E. Dudgeon, "Fundamentals of digital array processing," in Proceedings of the IEEE, vol. 65, no. 6, pp. 898-904, June 1977.
[6] Cardarilli G.C., Di Nunzio L., Fazzolari R., Re M., Ruffolo G., Bernocchi G. Analog chain calibration in Digital Beam-Forming applications. *ARPN Journal of Engineering and Applied Sciences*, 2018 13 (2), pp. 752-760.

[7] C. Cheung, R. Shah and M. Parker, “Time delay digital beamforming for wideband pulsed radar implementation,” *2013 IEEE International Symposium on Phased Array Systems and Technology*, Waltham, MA, USA, 2013, pp. 448-455.

[8] C. K. Chu and Yee-Hong Leung, “Further results on the WLS design of variable fractional delay filters,” *2012 6th International Conference on Processing and Communication Systems*, Gold Coast, QLD, 2012, pp. 1-7.

[9] T. Deng, “Symmetric Structures for Odd-Order Maximally Flat and Weighted-Least-Squares Variable Fractional-Delay Filters,” in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 12, pp. 2718-2732, Dec. 2007.

[10] Wu-Sheng Lu and Tian-Bo Deng, “An improved weighted least-squares design for variable fractional delay FIR filters,” in *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 8, pp. 1035-1040, Aug. 1999.

[11] Chien-Cheng Tseng, “Design of variable fractional delay allpass filter using weighted least squares method,” *2002 IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No.02CH37353)*, Phoenix-Scottsdale, AZ, USA, 2002, pp. V-V.

[12] S. Tahir, M. Elnamaky, M. A. Ashraf and K. Jamil, “Hardware implementation of digital beamforming network for Ultra Wide band signals using uniform linear arrays,” *The 2nd Middle East Conference on Antennas and Propagation*, Cairo, 2012, pp. 1-4.

[13] Cardarilli G.C., Di Nunzio L., Matta M., Re M., Silvestri F., Simone L., Spanò S. “Comparison and Implementation of Variable Fractional Delay Filters for Wideband Digital Beamforming”, Lecture Notes in Electrical Engineering, Article In Press 2019

[14] F. Harris, Xiaofei Chen, E. Venosa and F. A. N. Palmieri, “Two channel TI-ADC for communication signals,” *2011 IEEE 12th International Workshop on Signal Processing Advances in Wireless Communications*, San Francisco, CA, 2011, pp. 576-580.

[15] G. Manganaro and D. Robertson Interleaving ADCs: Unraveling the Mysteries https://www.analog.com/en/analog-dialogue/articles/interleaving-adcs

[16] *Interleaving ADCs for Higher Sample Rates* Literature Number: SNA1111 http://www.ti.com/lit/wp/sna1111/sna1111.pdf

[17] Cappello S., Cardarilli G.C., Di Nunzio L., Fazzolari R., Re M., Albicocco P. “Flexible channel extractor for wideband systems based on polyphase filter bank ”. *Journal of Theoretical and Applied Information Technology*, 2017; 95(16): 3841-3850.

[18] Cardarilli G.C., Di Nunzio L., Fazzolari R., Re M., Nannarelli A. “Power Efficient Digital Front-End for Cognitive Radio Systems”, Conference Record of the IEEE Asilomar Conference on Signals, Systems and Computers, 2018

[19] V. Valimaki and T. I. Laakso, "Principles of fractional delay filters," *2000 IEEE International Conference on Acoustics, Speech, and Signal Processing. Proceedings (Cat. No.00CH37100)*, Istanbul, Turkey, 2000, pp. 3870-3873 vol.6.

[20] Laakso T.I., Välimäki V., Karjalainen M., Laine U.K., “Splitting the unit: Delay tools for fractional delay filter design”. *IEEE Signal Processing Magazine*, 1996; 13(1), pp. 30-60.

[21] C. K. S. Pun, Y. C. Wu, S. C. Chan and K. L. Ho, "An efficient design or fractional-delay digital FIR filters using the Farrow structure," *Proceedings of the 11th IEEE Signal Processing Workshop on Statistical Signal Processing (Cat. No.01TH8563)*, Singapore, 2001, pp. 595-598.

[22] P. P. Vaidyanathan, "Multirate digital filters, filter banks, polyphase networks, and applications: a tutorial," in *Proceedings of the IEEE*, vol. 78, no. 1, pp. 56-93, Jan. 1990.

[23] Cardarilli, G.C., Di Nunzio, L., Fazzolari, R., Fereidountabar, A., Giuliani, F., Re, M., Simone, L. “Comparison of jamming excision methods for direct sequence/spread spectrum (DS/SS) modulated signal”, *Journal of Theoretical and Applied Information Technology*, 2017; 95(13): 2878-2888.

[24] Cardarilli, G.C., Di Nunzio, L., Fazzolari, R., Re, M., Silvestri, F., Spanò, S. “Energy consumption saving in embedded microprocessors using hardware accelerators”. *TEKOMNIKA (Telecommunication, Computing, Electronics and Control)*, (2018); 16(3): 1019-1026.

[25] Mitra S.K., and Yonghong K. Digital signal processing: a computer-based approach. Vol. 2. New York: McGraw-Hill, 2006.

[26] UltraScale Architecture Staying a Generation Ahead with an Extra Node of Value. https://www.xilinx.com/products/technology/ultrascale.html

Efficient FPGA implementation of high speed digital delay for wideband... (Gian Carlo Cardarilli)