Thickness Engineered Tunnel Field-Effect Transistors based on Phosphorene

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Thickness engineered tunneling field-effect transistors (TE-TFET) as a high performance ultra-scaled steep transistor is proposed. This device exploits a specific property of 2D materials: layer thickness dependent energy bandgap ($E_g$). Unlike the conventional hetero-junction TFETs, TE-TFET uses spatially varying layer thickness to form a hetero-junction. This offers advantages by avoiding the interface states and lattice mismatch problems. Furthermore, it boosts the ON-current to 1280 $\mu$A/$\mu$m for 15nm channel length. TE-TFET shows a channel length scalability down to 9nm with constant field scaling $E = V_{DD}/L_{ch} = 30$V/nm. Providing a higher ON current, phosphorene TE-TFET outperforms the homojunction phosphorene TFET and the TMD TFET in terms of extrinsic energy-delay product. In this work, the operation principles of TE-TFET and its performance sensitivity to the design parameters are investigated by the means of full-band atomistic quantum transport simulation.

I. INTRODUCTION

Since first experimental realization of $SS < 60$mV/dec\textsuperscript{1} in tunnel field-effect transistors (TFETs), these devices have been the main candidate for reduction of supply voltage $V_{DD}$ and energy consumption in electronic devices. TFETs lower the energy consumption of a transistor by removing the hot carrier injection from the source region of the transistor. However, TFETs have 2 main challenges: 1) small ON-current and 2) channel length scaling.

The small ON-current challenge of TFET is even more pronounced in the conventional CMOS channel materials, namely Si and Ge. These materials have an indirect gap which requires phonon assistance for band-to-band tunneling (BTBT). Si has also a large $E_g$ which further reduces $I_{ON}$. Smaller band gap channel materials such as Ge can improve the tunneling current and $I_{ON}$, however they also increase the $I_{OFF}$, hence degrade the $I_{ON}/I_{OFF}$ ratio\textsuperscript{2}. Previously, several designs have been proposed to increase the ON-current of TFETs such as 1) heterostructure channels \textsuperscript{3, 4}, 2) dielectric engineering \textsuperscript{5, 6} 3) internal polarization \textsuperscript{7}, and 4) 2D materials \textsuperscript{8–10}.

Heterostructure channels improve the performance of TFETs by using small Eg as source, Si as channel material to improve $I_{ON}$ while keeping $I_{OFF}$ small. Unfortunately, the large lattice mismatch \textsuperscript{11, 12} and interface states \textsuperscript{13–15} between the materials prevent the formation of an ideal heterojunction. Artificial heterojunctions based on a single channel material have been achieved in graphene by varying the width of graphene nanoribbon (GNR)\textsuperscript{16}. However, the edge roughness and device-to-device variations due to the lack of atomic level control in top down fabrication pose a big challenge for their technology development\textsuperscript{17–19}.

Novel 2D materials have interesting properties which can be used to provide artificial heterostructures. The bandgap of transition metal dichacogenides (TMDs), graphene and phosphorene depends on the layer thickness \textsuperscript{20–24}. In these materials, artificial heterojunctions can be achieved by spatially varying the layer thickness\textsuperscript{25}. Unlike the GNR heterojunctions where a sub-nanometer width control is required, a spatially varying layer thickness can be easily achieved with 2D material exfoliation.
and transfer techniques [26, 27]. Therefore, a thickness engineered TFET (TE-TFET) which exploits this spatially varying layer thickness technique is proposed in this letter. TE-TFET is designed to have a small $E_g$ in source and the channel near source and larger $E_g$ in the rest of device. TE-TFET can be applied to any material that has a band gap dependence on layer thickness. In this work, phosphorene is chosen as the channel material due to the fact that multi-layer phosphorene is direct gap material [28, 29] and its bandgap range includes the optimum bandgap of 1.2 $eV$ for TFET applications [30–32]. Although, the bandgap of TMD flakes depends on the flake thickness, only monolayer TMDs are direct gap materials.

A TE-TFET has several advantages: (1) Artificial heterojunction structure avoids the problems with lattice mismatch and interface states observed in a conventional heterojunction; (2) the ON-state current can be enhanced due to the small bandgap and small tunnel distance in source-channel interface; (3) the OFF-state current remains small because of the large $E_g$ barrier inside the channel.

The device structure of the TE-TFET based on phosphorene is shown in Fig. 1(a). The layer thickness and the length of the small band gap region inside the channel region are denoted by $L_{ext}$ and $T_{ext}$. The dependence of device performance on these design parameters and total channel length $L_{ch}$ will be discussed in details in section III. Finally, the capacitance voltage (CV) characteristics and energy delay product comparison with homojunction phosphorene TFET are discussed.

## II. SIMULATION DETAILS

The Hamiltonian of phosphorene is represented using a 10 band $sp^3d^5s^*$ second nearest neighbor tight binding model. The tight-binding parameters are well calibrated to match the band structure and effective mass from density function theory (DFT) HSE06 by the standard mapping method [33, 34]. Fig. 1(b) and Fig. 1(c) show the tight-binding bandstructure of 3L- and 1L-phosphorene, respectively. The Eg of phosphorene flakes with different number of layers are listed in Table 1. The relative permittivity for both in-plane $\epsilon_{in}$ and out-of-plane $\epsilon_{out}$ are taken from [35] and are also listed in Table 1. All the transport characteristics of the TE-TFET have been simulated using the self-consistent Poisson-Non Equilibrium Green’s Function (NEGF) method in the multi-scale [36] and multi-physics [37, 38] Nano-Electronic MOdeling (NEMO5) tool [39].

The default parameters of the TE-TFET device ($L_{ch}$, $L_{ext}$ and $T_{ext}$ shown in Fig. 1(a) are set to 12nm, 4nm and 3L respectively. $V_{DS}$ is 0.4V for $L_{ch}$ 12nm. Source and drain regions are doped with the doping level of $10^{20} cm^{-3}$. Equivalent oxide thickness (EOT) is set to 0.5nm. Constant field scaling $E = 30 V/nm$ is chosen for the device scaling, where $E = V_{DD}/L_{ch}$.

## III. RESULTS AND DISCUSSION

The transfer characteristics ($I_d - V_g$) of TE-TFET compared against 1L, 2L, and 3L phosphorene TFETs is shown in Fig. 2 All the $I_d - V_g$ curves, except the 3L-TFET, are shifted to have the same $I_{OFF}$ of $10^{-4} \mu A/\mu m$. The minimum current of 3L-TFET is $4.131 \mu A/\mu m$, which is larger than the required $I_{OFF}$ level. Hence, 3L phosphorene TFET is shifted by the same voltage shift as that of the TE-TFET.

Fig. 2 shows that TE-TFET has the advantages of both 3L and 1L homojunction TFETs: small $I_{OFF}$ of 1L-TFET and high ON-current of 3L-TFET. The $I_{ON}$ of about 700$\mu A/\mu m$ is achieved in TE-TFET with $V_{DD} = 0.4V$, which is 2 times larger than 2L-TFET. $I_{th}$, the current when SS becomes 60mV/dec [40], in TE-TFET is about 10$\mu A/\mu m$ which is larger by two orders compared to that of the best phosphorene TFET.

A comparison of TE-TFET against 3L-TFET in the ON-state and 1L-TFET in the OFF-state are shown in Fig. 3; the band diagrams along with energy resolved current of these devices are also plotted. At OFF state, as shown in Fig. 3(a) and b, TE-TFET has a larger barrier compared to the 3L-TFET which blocks the direct source-to-drain tunneling in the 1L section. TE-TFET thus achieves a small OFF-current. In the ON-state, shown in Fig. 3(c) and d, TE-TFET has a smaller tunnel distance compared to the 1L-TFET. Thus, TE-TFET

| Layer | 1 | 2 | 3 | 4 |
|-------|---|---|---|---|
| $E_g$(eV) | 1.390 | 0.803 | 0.570 | 0.481 |
| $\epsilon_{in}$ | 4.56 | 7.41 | 8.77 | 9.98 |
| $\epsilon_{out}$ | 1.36 | 1.52 | 1.80 | 2.04 |

**TABLE I. Phosphorene Parameters**

**FIG. 2.** The transfer characteristics of TE-TFET compared with different layer thickness TFET based on phosphorene.
FIG. 3. The band edges of (a) TE-TFET with 3L TFET at OFF state and (b) TE-TFET with 1L and 3L TFET at ON state aligned with the energy resolved current (c) and (d) respectively.

is able to achieve a higher ON-current compared to 1L-TFET due to the smaller tunnel distance at the source-channel interface. TE-TFET has $SS = 15\text{mV/dec}$ over four decades of drain current. In spite of high current levels in TE-TFET, its ON-current does not reach that of 3L-TFET due to the 1L barrier inside channel as shown in Fig. 3c and d.

The impact of device design parameters $T_{ext}$ and $L_{ext}$ on its performance is discussed for a TE-TFET with $L_{ch} = 12\text{nm}$. As shown in Fig. 4a, 4L, 3L and 2L flakes are used in the extension region of TE-TFET which translate into a bandgap of 0.481eV, 0.570eV and 0.803eV respectively. The ON-current can be improved from $700\,\mu\text{A/\mu m}$ to $800\,\mu\text{A/\mu m}$ by replacing 3L with 4L in the extension region. TE-TFET with 2L extension still achieves an ON-current similar to 3L, but its $I_{60}$ degrades by two orders of magnitude. Fig. 4b shows the impact of $L_{ext}$ on the performance of TE-TFET; by increasing $L_{ext}$ from 1nm to 2nm, the ON current improves by an order of magnitude. However, the performance saturates for $L_{ext}$ beyond 2nm (up to 4nm). This minimum value of $L_{ext}$ is because for the cases where $L_{ext}$ is too short, the tunneling in the ON-state does not occur completely in the small Eg region. Hence, a lower ON-current is achieved with $L_{ext}$ below 2nm.

The $I_{ON}/I_{OFF}$ ratio as a function of $T_{ext}$ and $L_{ext}$ for $L_{ch} = 12\text{nm}$ and $6\text{nm}$ is plotted in Fig. 4c. For the $6\text{nm}$ channel length with $V_{DS}$ of 0.2V (constant field scaling), the trend is similar to that of $L_{ch} = 12\text{nm}$. The OFF current of TE-TFET with $L_{ch} = 6\text{nm}$ increases beyond $10^{-4}\,\mu\text{A/\mu m}$ due to the fact that 1L barrier inside the channel is not long enough to block the leakage current. For a fair comparison, $I_{ON}$ is fixed to $10^{2}\,\mu\text{A/\mu m}$ for $L_{ext}$ study. It is worthwhile to mention that there is only a small range of $V_{GS}$ for $L_{ch} = 6\text{nm}$ in which the $SS$ is smaller than 60$m\text{V/dec}$.

Constant field scaling $E = 30\text{V/nm}$ of TE-TFETs is studied in this part ($E = V_{DD}/L_{ch}$). Fig. 4d shows that the $I_{ON}/I_{OFF}$ of TE-TFET is over 6 orders of magnitude for $L_{ch}$ above 9nm, however there is a noticeable increase in $I_{OFF}$ for the channel length of 6nm. Fig. 5a shows the impact of scaling on the total gate capacitance characteristics ($C-V_{GS}$). The gate capacitance is noticeably smaller than most TMD materials. This smaller capacitance originates from the smaller effective mass of phosphorene [31]. Unlike homojunctions, the CV curve of TE-TFET has a plateau region. This plateau in CV appears due to the strong density of states (DOS) modulation within the quantum well region. Fig. 5b illustrates the carrier density along the transport direction at the beginning and the end of the plateau region. In both
increase in DOS inside the 1L region and forms the plateau in the C-V curves. The length of the plateau region is different for different $L_{ch}$ since the carrier density is also influenced by the carrier injection from drain [41].

Compared to homojunction phosphorene TFETs [31], TE-TFETs exhibit higher ON-currents and slightly higher capacitances. These higher ON-currents translate to an improvement in 32 bit adder energy-delay product as shown in Fig. 6. The 32-bit adder energy-delay product is calculated using BCB 3.0 model [42] in which the parasitic capacitances are taken into account. The circuit parameters required in BCB model are taken from ITRS roadmap.

IV. CONCLUSION

In conclusion, thickness engineered tunneling field-effect transistor (TE-TFET) is proposed and evaluated in this work. By taking advantage of flake-thickness-dependent direct bandgap in phosphorene, an artificial heterostructure TFET can be achieved. The absence of interface, between different materials in artificial heterojunctions, allows TE-TFET to avoid the interface states and lattice mismatch problems observed in conventional heterojunction TFETs while providing similar boost in the ON-current of 1280 $\mu A/\mu m$ with a 15nm channel length. TE-TFETs are scalable down to 9nm with constant field scaling $E = V_{DD}/L_{ch} = 30$ V/nm. Offering higher ON-current, TE-TFETs outperform the best homojunction phosphorene TFETs and TMD TFETs in terms of circuit energy-delay product.

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