Performance evaluation of multiple (32 channels) sub-nanosecond TDC implemented in low-cost FPGA

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ABSTRACT: NA62 experiment Straw tracker frontend board serves as a gas-tight detector cover and integrates two CARIOCA chips, a low cost FPGA (Cyclon III, Altera) and a set of 400Mbit/s links to the backend. The FPGA houses 16 pairs of sub-nanosecond resolution TDCs with derandomizers and an output link serializer. Evaluation methods, including simulations, and performance results of the system in the lab and on a detector prototype are presented.

KEYWORDS: Front-end electronics for detector readout; Electronic detector readout concepts (gas, liquid); Data acquisition concepts
1 The detector

NA62 is a new Kaon experiment at the CERN SPS accelerator. The goal is to measure the very rare Kaon decay $K^+ \rightarrow \pi^+ \nu \bar{\nu}$ to make a decisive test of the Standard Model by extracting a 10% measurement of the CKM parameter $|V_{td}|$. The NA62 experiment is situated in the cavern TCC8 + ECN3 of the SPS North Area High Intensity Facility (NAHIF). The post decay tracker of NA62 is a STRAW tracker operating in vacuum [2].

The purpose of the STRAW Tracker is to measure the direction and momentum of secondary charged particles originating from the decay region with good accuracy. The spectrometer consists of four chambers intercepted in the middle by a high aperture dipole magnet providing a vertical B-field of 0.36T. Each chamber is equipped with 1792 straw tubes, which are arranged in four views providing measurements of four coordinates. The 2.1m long with 9.8 mm diameter tubes operate in vacuum at $1 \times 10^{-6}$ mbar and provide less than 130 um spatial tracking. Central tubes are expected to function at a 800 KHz particle rate, while the average for the whole detector is calculated at 60 KHz.

The frontend modularity is following straw smallest unit. There are 16 straws in the basic unit of gas distribution, high voltage and readout. Both starts and ends of signal must be recorded. The falling edge (end) of signal is the same for all straws seeing the same particle and can be used for time measurement validation or even as a crude time measurement. The rising edge (start) of the signal is used for precise drift time measurement and the track position is calculated through known r-t dependence.
2 The electronics

To cover the aforementioned requirements for the readout of few femto Coulomb pulses with sub-nanosecond precision for 7168 straws, an electronic board has been developed, following the modularity of 16 straws, measuring both rising and falling edges in separate TDCs.

The Straw tracker frontend board (figure 1) serves as a gas-tight detector cover and high voltage distributor, and integrates two CARIOCA chips, a low cost FPGA (Cyclon III, Altera) and a threshold setting DAC. The pulses are received by the CARIOCA chips (8 channels each) and after amplification, shaping and discrimination they are sent to the FPGA over LVDS links. The FPGA houses 32 sub-nanosecond resolution TDCs with derandomisers and an output link serializer. The FPGA also serves as the controller of functionality, DAC and communication with the backend. Data and commands are transferred over links with speed of 400 Mbps per twisted pair using CAT6 Ethernet cables.
3 Firmware

Four different clocks are generated by the same PLL and shared by all 32 TDCs on board (figure 2). Two clocks at 320 MHz with a phase difference of 90 degrees are connected to two different LVDS receivers sampling the inputs on rising and falling edges of the clocks (ALTERA megafuns). The bits from the receivers create a 16 bit edge detection register, clocked by a third clock of 80 MHz. Transitions are flagged and timestamped with a 5 bit word of 0.78 ns LSB, to get the basic coarse measuring time unit of 25 ns [4]. Words of 32 bits comprising of 18 bits of coarse timestamp and straw identity information along with 5 bits of fine measurement are pipelined in separate derandomisers (FIFOs) and then multiplexed into one output buffer. The output of the FIFO is first divided in four bytes and then serialized, 8b/10b encoded and sent at a maximum distance of 20 meters with CAT6 Ethernet cables.

4 Simulations and initial testing

In order to finalize the firmware and assess its performance, a number of different schemes were proposed. All were simulated using the Cadence simulator with timing and performance information provided by the Altera Quartus software. The final architecture was chosen only after differential non-linearity of less than 100 ps was confirmed. The next step of testing involved the creation of a dedicated test bench in the lab (including a waveform generator and an oscilloscope connected to the PC with a GPIB controller) to create timed LVDS signals, that were then input to an FPGA evaluation board (Cyclone III Started Kit Board, DEO-Nano Board) [3].

The results confirmed the expected performance for more than $10^4$ random measurements per bin (figure 3). The nominal TDC bin is 0.78 ns with differential non-linearity of 120 ps.

5 Test of the integrated system with injection of low charge on the real DAQ input

For the next test the cover prototype with the final version of the TDC firmware and with a full data acquisition chain was used. The cover was connected to a Straw Readout Board (SRB) from which data was sent to a Single board computer (SBC) through VME bus. Dedicated control software was developed using the ATLAS VME driver [5]. The system was used in the 2012 technical
Figure 4. TDC linearity of the full system with realistic charge pulse injection

Figure 5. Demonstration of the pulse reconstruction by scanning different thresholds

run [1], as well as for a dedicated test bench in the lab, to statistically enhance the knowledge and understanding of the system.

In this test bench, the software sends a start command to the SRB. This command is distributed both through the standard direction to be used for commands in the final system, as well as from the SRB as a trigger to a waveform generator. This process is deterministic and ensures a constant delay between the start of the counters on the TDCs and the triggering of the generator.

Different voltage pulses have been designed. Some intended to resemble in shape real electron clusters, as seen in simulations and before the discriminator of the CARIOCA via its analog output. Those are then triggered and sent to a bespoke board on the input of the cover to be attenuated and converted into a current function over a resistor. Alternatively square voltage pulses are converted into a delta charge function over a capacitor.

A number of different tests have been carried out with this setting. It has been possible to calculate the baseline and the sensitivity of the electronics and to calibrate the threshold for the reception of the pulses. Also, the fine time resolution of the TDC was measured by sending $10^4$ pulses every 0.5 ns within the 25 ns clock cycle.

The complete scan is on the figure 4, showing a regular bin size of 0.78 ns. A second test was performed to visualise the results and rule out the possibility of after pulses created by the CARIOCA shaper. In this case, for a set delay, the threshold of the CARIOCA discriminator sweeps a region of different charge thresholds, providing an image of one predesigned pulse, as received over time and after TDC reconstruction (figure 5).

6 Test with straw prototype: charge injection and cosmics

During the prototyping of the STRAW detector, a 64-straw prototype was built. This same prototype has been used in the past for different hardware and electronics tests in the lab or in test beam at CERN.
The first test on the prototype confirmed the results of the charge injection tests, with the charge being injected at the far end of one straw. This also provided useful information about the straw as a transmission line, in regard to attenuation and delay as well as about the integration of the electronics on the detector.

A new setting was required in order to acquire real particles, provided by the cosmic radiation. A scintillator couple was used for triggering and micromegas gaseous particle detectors were employed to provide precise tracking of cosmic particles. Dedicated software has been developed, to match triggering information with the read out. With this setting (figure 6), recording and reconstructing the trajectory of cosmic particles was made possible (figures 8 and 7).

7 Conclusions

The performance of the multiple sub-nanosecond TDC architecture has been measured at around 100 ps differential non-linearity. The architecture has been successfully integrated in the system, as shown by the measurements taken with full DAQ in various conditions. The design covers the specifications given. With the full system, 14236 different TDCs will be read out by the back end boards, with an average rate of 60,000 charged particles per second per straw, creating a bulk of data in the order of 15 Gbps.
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