Strain-Enhanced Mobility of Monolayer MoS$_2$

Isha M. Datye, Alwin Daus, Ryan W. Grady, Kevin Brenner, Sam Vaziri, and Eric Pop*

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ABSTRACT: Strain engineering is an important method for tuning the properties of semiconductors and has been used to improve the mobility of silicon transistors for several decades. Recently, theoretical studies have predicted that strain can also improve the mobility of two-dimensional (2D) semiconductors, e.g., by reducing intervalley scattering or lowering effective masses. Here, we experimentally show strain-enhanced electron mobility in monolayer MoS$_2$ transistors with uniaxial tensile strain, on flexible substrates. The on-state current and mobility are nearly doubled with tensile strain up to 0.7%, and devices return to their initial state after release of the strain. We also show a gate-voltage-dependent gauge factor up to 200 for monolayer MoS$_2$, which is higher than previous values reported for sub-1 nm thin piezoresistive films. These results demonstrate the importance of strain engineering 2D semiconductors for performance enhancements in integrated circuits, or for applications such as flexible strain sensors.

KEYWORDS: 2D materials, MoS$_2$ transistors, strain engineering, strain sensors, mobility

Transition metal dichalcogenides (TMDs), a class of two-dimensional (2D) layered materials, have gained interest for electronic and optoelectronic devices due to their atomically thin nature and pristine interfaces that, in theory, lack dangling bonds. MoS$_2$ is a promising TMD because it can be synthesized in single layers, it is relatively air-stable, and its band gap is nearly twice that of silicon, which is advantageous for low-power transistors. However, other electrical properties, such as on-state current, mobility, and contact resistance of MoS$_2$ and other TMD devices must be improved for them to compete with or complement existing technologies based on silicon. Several techniques have been used to experimentally improve TMD-based transistors, such as contact engineering, channel doping, defect healing, and interface engineering, while strain engineering has been theoretically predicted as an additional method to improve electrical performance.

Strain engineering was shown to improve the mobility of silicon metal oxide semiconductor field-effect transistors (MOSFETs) in the 1990s, and then commercialized with the 90 nm technology node. In practice, electron mobility in nMOS silicon FETs is increased by uniaxial tensile strain from silicon nitride encapsulation layers. In contrast, higher hole mobility in pMOS silicon FETs is achieved by uniaxial compressive strain imparted by selective growth of SiGe at the source and drain regions. Reduced electron effective mass and scattering due to band splitting in the conduction band, and reduced hole effective mass due to band warping in the valence band, lead to enhanced mobility with strain in silicon. Experimental and theoretical studies have shown that strain can also modify the band structure and phonon dispersion of 2D semiconductors based on TMDs. However, most strained TMD studies to date have focused on optical measurements (e.g., photoluminescence mapping of optical band gap changes with strain), and less attention has been paid to strain effects on electron and hole mobility, despite the enhancement predicted theoretically.

In this work, we study the effect of uniaxial tensile strain on the electrical performance of monolayer MoS$_2$ transistors on flexible substrates. We find the mobility and on-state current are nearly doubled with ~0.7% applied strain, reverting to their initial values when the strain is removed. This represents the largest enhancement of TMD mobility with externally applied strain to date, revealing that strain engineering could be just as important as defect- and contact-engineering for enhancing the performance of 2D transistors based on TMDs. We also show that these devices can be used as strain sensors with voltage-dependent gauge factors up to ~200, larger than most conventional strain sensors based on bulk materials and most 2D-based strain sensors.

We fabricate MoS$_2$ transistors with local back-gates on freestanding polyethylene naphthalate (PEN), a flexible and...
We apply strain to our MoS2 transistors using a two-point bending apparatus, by controlling the distance between the two ends of the substrate, as shown in Figure 2a. The strain can be estimated as $\varepsilon = \tau / (2R)$, where $\tau = 125 \mu m$ is the thickness of the PEN and $R$ is the radius of curvature of the bent substrate (see Figure 2b). The strain applied to the MoS2 is confirmed by Raman and photoluminescence (PL) spectroscopy, by monitoring the position of the in-plane E' peak at $\sim 384$ cm$^{-1}$ and the A exciton peak at $\sim 1.8$ eV, respectively. We note that we can only monitor changes in the MoS2 strain with bending; i.e., we cannot be sure if the transistor has built-in tensile or compressive strain from the transfer and fabrication process, because the Al2O3 gate dielectric can cause peak shifts in the MoS2 Raman spectra. Thus, all strain measurements below are reported relative to the as-fabricated devices in their flat, unstrained state.

Figure 2c shows the Raman spectra of the MoS2 device from Figure 1b without applied strain (blue) and with $\sim 0.7\%$ tensile strain (red). We perform Raman measurements on four locations across the device channel with similar results, but only include one representative spectrum at each strain level here for clarity. The E' peak clearly redshifts with $\sim 0.7\%$ applied tensile strain, and the average positions of the E' peaks without and with applied strain are $384.6 \pm 0.3$ and $383.0 \pm 0.2$ cm$^{-1}$, respectively. This corresponds to a peak shift of $\sim 2.3 \pm 0.2$ cm$^{-1}$/% strain, which is comparable to that of other studies. The cyan curve, representing the measurement after strain is released, matches very well with the initial 0% (blue) curve, indicating that the effects of strain are reversible. Figure S2 of Supporting Information Section 2 includes Raman peak position data for all devices measured and a short discussion of the smaller A$_1$ peak shifts.

Figure 2d displays the PL spectra of the MoS2 device from Figure 1b at 0% (blue), 0.4% (magenta), 0.6% (red), and back to 0% strain (cyan). As expected, the A exciton redshifts with tensile strain because of a decrease in the direct, optical band gap at the K point (see Figure 2e). The A exciton peak positions at 0%, 0.4%, 0.6%, and back to 0% strain are $1.810 \pm 0.006$, $1.790 \pm 0.004$, $1.772 \pm 0.004$, and $1.811 \pm 0.005$ eV, respectively, averaged over four measurements in the device channel. Therefore, the shift of the A exciton peak is $\sim 63 \pm 10$ meV/% strain. This is similar to that of other experimental studies demonstrating the PL of MoS2 with strain. The PL peak position data for all devices measured are included in Supporting Information Figure S3b.

Next, we perform electrical measurements of our devices as a function of strain. Our setup enables direct probing of transistors under strain (see Figure 2a) inside a vacuum probe station at $\sim 2 \times 10^{-5}$ Torr pressure. Figure 3a displays drain current vs gate voltage ($I_D - V_{GS}$) measurements of the MoS2 transistor shown in Figure 1b with applied tensile strain from 0% to 0.7%, and back to 0%. The on-state current rises with increasing strain and then returns to the initial (unstrained) level after strain release (cyan curve in Figure 3a). Thus, strain does not have a permanent effect on the device characteristics. The gate leakage currents remain low ($\sim 1.2$ nA) across all $V_{GS}$ and strain levels (see Supporting Information Figure S4). The drain current vs drain voltage ($I_D - V_{DS}$) measurements of the device at 0% (solid lines) and 0.7% strain (dotted lines) are displayed in Figure 3b at several $V_{GS}$ values. As before, we observe $I_D$ increasing with strain; for example, at $V_{GS} = 7$ V and $V_{DS} = 5$ V, the current doubles from $\sim 6 \mu A/\mu m$ to $\sim 12 \mu A/\mu m$ at 0.7% strain.

We estimate the field-effect mobility from the $I_D$ vs $V_{GS}$ curves in the linear operation regime, as $\mu_{FE} = (\partial I_D / \partial V_{GS})/L/(W/C_s V_{GS})$, where $C_s \approx 312$ nF/cm$^2$ is the capacitance per unit area of the gate oxide, extracted from capacitance–voltage measurements of Au–Al2O3–Au structures on the same sample as the MoS2 transistors, with and without strain (see Supporting Information Section 4). We note the threshold voltage ($V_T$) also changes with strain (see Figure 3a and Supporting Information Figure S11), suggesting that the electron density increases with the decreasing band gap under tensile strain. To account for shifts in $V_T$, we estimate $\mu_{FE}$ at the same carrier density $n \sim 1.1 \times 10^{13}$ cm$^{-2}$, where $n = (C_s q)/(V_{GS} - V_T - V_{DS}/2)$. We estimate $V_T$ with the linear extrapolation method, which uses the voltage intercept of a line fit to the $I_D$ vs $V_{GS}$ near the maximum transconductance $g_m = \partial I_D / \partial V_{GS}$. The transistor has $\mu_{FE} \approx 5.3$ cm$^2$ V$^{-1}$ s$^{-1}$ with 0% applied strain and $\mu_{FE} \approx 10.8$ cm$^2$ V$^{-1}$ s$^{-1}$ with 0.7% applied tensile strain. Therefore, we achieve a $\sim 2\times$ improvement in $\mu_{FE}$ at 0.7% tensile strain for this device, which is essentially the same as the increase in drive current observed in Figure 3b.

We measure 7 other transistors with lengths from $L = 2$ to 15 $\mu$m on the same substrate and perform electrical measurements with applied strain. To account for $V_T$ variation, we extract $\mu_{FE}$ at the same carrier density ($n \sim 1.1 \times 10^{13}$ cm$^{-2}$) and $I_D$ at the same $V_{GS} = 7$ V and $V_{DS} = 1$ V, plotting the
data for all devices in Figure 3c,d. These show \( \mu_{FE} \) and \( I_D \) normalized to their initial values without applied strain, with the data from all devices summarized by box plots. (Supporting Information Figure S6 shows the magnitudes of \( \Delta \) and \( I_D \) for each device, without normalizing them.) On average, \( \mu_{FE} \) increases by a factor of 1.85 ± 0.23, and \( I_D \) increases by a factor of 1.76 ± 0.18 with 0.7% applied tensile strain, compared to the initial values without applied strain. For the \( I_D \) comparison, we note that the threshold voltage variation is at most \( \delta V_T \approx 1 \) V, which is significantly smaller than the overdrive voltage \( V_{GS} - V_T \approx 8 \) V. Therefore, the \( \sim 12.5\% \) variation in electron density with \( \delta V_T \) cannot account for the nearly \( 2X \) increase in \( I_D \), which must come directly from the tensile strain applied.

Supporting Information Section 5 displays additional strain-dependent data as a function of channel length and at lower carrier density, with results largely consistent with the data presented in Figure 3. We also explored strain levels in excess of 0.7%; however, we generally observed a degradation of electrical device performance in such cases (see Supporting Information Section 6). We attribute this degradation to either worsened adhesion of the metal contact to the MoS$_2$ or to cracking of the metal lines or Al$_2$O$_3$ gate dielectric. "Slippage" of the MoS$_2$ along the substrate was ruled out because we observed the expected shift of the E' Raman peak at higher strain levels (Supporting Information Figure S13). In future work, higher strains could be achievable with metals that are more ductile and with gate oxides like HfO$_2$.

The improvements in current and mobility of our devices are expected to result from changes in the band structure with strain, as illustrated in Figure 2d,e. The direct band gap of monolayer MoS$_2$ at the K point decreases with tensile strain, seen as a redshift of the A exciton in Figure 2d. The next-lowest valley in the conduction band is at the Q point (approximately halfway along the T line between the Γ and K points), and the energy separation between the Q and K valleys (\( \Delta E_{Q\bar{K}} \)) has been predicted to increase when tensile strain is applied to MoS$_2$ (see Figure 2e), resulting in less electron intervalley scattering and therefore improved mobility. \( \sim 12-14 \) (\( \Delta E_{Q\bar{K}} \) for monolayer MoS$_2$, encased in quartz and WS$_2$ was experimentally estimated to be \( \sim 110 \) meV range for unstrained monolayer MoS$_2$ depending on the simulation approach used.\( \sim 12-14,41,45,46 \) Monolayer TMDs such as WS$_2$, WSe$_2$, MoSe$_2$, and MoTe$_2$ have smaller \( \Delta E_{Q\bar{K}} \); thus, one may expect a larger mobility improvement with strain in transistors based on these materials.\( \sim 13,46,47 \)

Tensile strain is also expected to change the curvatures of the conduction band valleys, leading to decreased electron effective mass.\( \sim 14,15,48,49 \) This is similar to the reduced electron effective mass with strain in silicon nMOS transistors, which leads to increased mobility.\( \sim 20,21 \) Applying tensile strain to 2D transistors has also been suggested to lower Schottky barriers at the source and drain contacts,\( \sim 33,30,51 \) potentially leading to lower contact resistance. However, because our devices have relatively long channels and our improvements in \( \mu_{FE} \) and \( I_D \) do not depend on channel length (see Supporting Information Figure S7), we expect the contribution of contact resistance in our measurements to be relatively small.\( \sim 52 \) Thus, we believe that the electrical performance improvements observed here are mostly related to electronic transport in the MoS$_2$ channel, i.e., lower intervalley scattering and effective mass.

We also consider the interaction of strain with defects in our MoS$_2$ channels. Electron transport in our MoS$_2$ channels is likely to occur in part by band-like transport, which is limited by scattering with phonons (e.g., intervalley\( \sim 12,13,43 \)), defects, or impurities, and in part by hopping-like transport between defect trap states.\( \sim 53 \) When strain is applied, the former benefits from lowering of the phonon-assisted intervalley scattering.
is the gauge factor (GF), defined as \( \frac{\Delta R}{R_0} \). The figure of merit used to characterize strain sensors is the initial resistance with 0% applied strain. We note that Figure 4d only displays GF values at 0% strain.

Figure 3. (a) Transfer characteristics \( I_D \) vs \( V_{GS} \) of the device from Figure 1b \( (W = 20 \mu m, L = 8 \mu m) \) at \( V_{DS} = 1 V \) and different levels of applied tensile strain \( \varepsilon \). Solid lines correspond to data plotted on a log scale (left y-axis), and dashed lines represent the same data plotted on a linear scale (right y-axis). (b) Output voltage characteristics \( I_D \) vs \( V_{DS} \) of the same device at 0% (solid) and 0.7% (dotted) applied tensile strain, for \( V_{GS} = 1 V \) (green), 3 V (magenta), and 7 V (dark blue). (c) Field-effect mobility \( \mu_{FE} \) normalized to the initial (unstrained) values for 8 devices as a function of applied strain, with box plots showing the median across devices (red points), first and third quartiles (blue box), and maximum and minimum (top and bottom horizontal lines, respectively). The cyan box plot corresponds to the measurement after strain is released. (d) \( I_D \) normalized to the initial (unstrained) values at different levels of strain, with box plots again showing the distribution of values across all devices. \( I_D \) values were extracted with \( V_{GS} = 7 V \) and \( V_{DS} = 1 V \). The cyan box plot again shows the measurement after strain is released.

Figure 4a shows the resistance \( \frac{R = V_{DS}/I_D}{R_0} \) vs \( V_{GS} \) curves for the device in Figure 1b from 0% to 0.7% applied tensile strain. Figure 4b illustrates \( \frac{\Delta R}{R_0} \) vs strain for several \( V_{GS} = -4.4, 0, 3, \) and 7 V. We find the largest change in resistance at \( V_{GS} = -4.4 V \), which corresponds to the subthreshold region of the transistor (see Figure 3a). Fitting a dashed line to the \( \frac{\Delta R}{R_0} \) vs strain at this \( V_{GS} \) yields an average GF \( \approx 150 \). Figure 4c shows the calculated GF as a function of \( V_{GS} \) for each strain level in Figure 4a. We observe a peak in GF at all strain levels around \( V_{GS} = -4.4 V \), with the maximum GF reaching \( \sim 200 \) for 0.4% tensile strain in this device. We performed similar measurements on 7 other devices with channel lengths between 2 and 15 µm, and we found an average maximum GF \( = 200 \) for these devices. The GF displays a stronger gate dependence below and near the threshold region \( V_{GS} < 0 \) where current is limited by hopping-like transport between defect trap states, recently shown to more weakly trap carriers when tensile strain is applied. The GF is nearly constant in the linear transistor regime \( V_{GS} > 0 \), also see Figure 3a) where the band-like transport and mobility dominate.

Figure 4d compares the best GF values obtained in this work to those found in the literature for MoS\(_2\) other 2D materials, silicon, and metals (of various thicknesses). Our GF for monolayer CVD-grown MoS\(_2\) is higher than the best GFs for monolayer and trilayer exfoliated MoS\(_2\), CVD-grown MoS\(_2\), other 2D materials (BP, InSe, and PtSe\(_2\)), and thin metal films. Comparably similar higher GFs have been found for bulk crystalline silicim and bilayer exfoliated MoS\(_2\), respectively. However, CVD-grown MoS\(_2\) is easier to integrate and more promising than bulk silicon or exfoliated MoS\(_2\) for large-area flexible and transparent sensors. We note that Figure 4d only displays GF calculated as \( \frac{\Delta I/I_0}{\Delta \varepsilon} \), though some studies calculate GF as \( \frac{\Delta I/I_0}{\Delta \varepsilon} \), where \( I \) is current, which artificially yields much larger GF. For example, using the latter definition with current instead of resistance, the maximum GF achieved by our devices would be \( \sim 5000 \) instead of \( \sim 200 \).
In summary, we studied the mobility enhancement of CVD-grown monolayer MoS$_2$ transistors with tensile strain, by bending devices on flexible PEN substrates. We found a 2-fold increase of mobility and current with tensile strain up to 0.7%, and a gauge factor (GF) up to $\sim 200$, which is the highest reported for sub-1 nm thin piezoresistive films. The improvements are attributed to changes in the band structure, including lower electron–phonon intervalley scattering and lower electron effective mass with tensile strain. These results achieve the largest mobility improvements of MoS$_2$ transistors with strain to date, pointing the way for performance enhancements in integrated 2D electronics, and for the use of this material in strain sensors on flexible substrates. For electronics on rigid substrates (i.e., integrated with silicon), strain could be induced with nitride or metal layers, or by growth on substrates with different thermal coefficients of expansion or lattice constants. Some approaches would have the additional advantage of inducing biaxial strain in the 2D material, which is expected to have a larger effect on the electrical properties than uniaxial strain.\(^{12,23,75}\)

### Figure 4.

(a) Resistance ($R$) vs $V_{GS}$ curves of the device in Figure 1b at $V_{DS} = 1$ V at different levels of applied strain ($\epsilon$). (b) $\Delta R/R_0$ vs strain at different gate voltages for the curves in panel a. (c) Gauge factor (GF = $(\Delta R/R_0)/\Delta \epsilon$) vs $V_{GS}$ for the different levels of strain. $\Delta \epsilon$ is always calculated with respect to 0% strain. The GF below approximately $-5$ V is uncertain when the measurable $I_D$ minimum is reached (see Figure 3a), suggesting that the peak GF obtained could be higher at lower voltages. (d) GF vs thickness for our best devices (shown as the blue square with error bars) in addition to various materials found in the literature, including CVD-grown MoS$_2$, exfoliated MoS$_2$, indium selenide (InSe), platinum selenide (PtSe$_2$), black phosphorus (BP), polycrystalline Si (poly-Si), crystalline Si (c-Si), and thin metal films. We note that the c-Si values are for bulk Si with thicknesses likely greater than 1 $\mu$m.

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**ASSOCIATED CONTENT**

**Supporting Information**

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.2c01707.

Device fabrication and MoS$_2$ transfer process, Raman and photoluminescence (PL) spectroscopy of devices with strain, current–voltage characteristics of MoS$_2$ transistors with strain, C–V characteristics of Au–Al$_2$O$_3$–Au capacitors with strain, mobility ($\mu_{FE}$) and drain current ($I_D$) as a function of strain, and degradation of devices at high levels of strain (PDF)

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**AUTHOR INFORMATION**

**Corresponding Author**

Eric Pop — Department of Electrical Engineering, Stanford University, Stanford, California 94305, United States; Department of Materials Science & Engineering and Precourt Institute for Energy, Stanford University, Stanford, California 94305, United States; orcid.org/0000-0003-0436-8534; Email: epop@stanford.edu

**Authors**

Isha M. Datye — Department of Electrical Engineering, Stanford University, Stanford, California 94305, United States; orcid.org/0000-0002-4409-2766

Alwin Daus — Department of Electrical Engineering, Stanford University, Stanford, California 94305, United States; Present Address: Chair for Electronic Devices, RWTH Aachen University, Aachen, 52074, Germany; orcid.org/0000-0001-7461-3756

Ryan W. Grady — Department of Electrical Engineering, Stanford University, Stanford, California 94305, United States; orcid.org/0000-0002-0457-5026

Kevin Brenner — Department of Electrical Engineering, Stanford University, Stanford, California 94305, United States; orcid.org/0000-0001-7461-3756

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The authors declare no competing financial interest.

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Supporting Information

Strain-Enhanced Mobility of Monolayer MoS$_2$

Isha M. Datye,$^1$ Alwin Daus,$^{1,2}$ Ryan W. Grady,$^1$ Kevin Brenner,$^{1,3}$ Sam Vaziri,$^1$ and Eric Pop$^{1,4,5,*}$

$^1$Department of Electrical Engineering, Stanford University, Stanford, CA 94305, USA
$^2$Present address: Chair for Electronic Devices, RWTH Aachen University, Aachen, 52074, Germany
$^3$Present address: Department of Electrical and Computer Engineering, Southern Methodist University, Dallas, TX 75275, USA
$^4$Department of Materials Science & Engineering, Stanford University, Stanford, CA 94305, USA
$^5$Precourt Institute for Energy, Stanford University, Stanford, CA 94305, USA

*Corresponding Author: epop@stanford.edu

1. Device fabrication and MoS$_2$ transfer process

1.1 Fabrication of monolayer (1L) MoS$_2$ transistors

The steps for fabricating our MoS$_2$ transistors on polyethylene naphthalate (PEN) substrates are described below. We include a schematic for each step of the process in Figure S1.

First, we pattern Cu (28 nm)/Au (5 nm) back-gates (BG) by optical lithography directly on the PEN (125 μm thick), and deposit them using electron-beam (e-beam) evaporation. We use Cu in contact with PEN because of its higher ductility than Au,$^1$ and we use a thin Au layer to encapsulate the Cu and limit its oxidation. We then deposit ~20 nm aluminum oxide (Al$_2$O$_3$) using atomic layer deposition (ALD) in a Savannah S200 from Cambridge Nanotech, with trimethyl aluminum (TMA) and H$_2$O as precursors for 200 cycles. We perform ALD at 130°C, which is within the thermal limitations of our PEN substrates.

The MoS$_2$ is grown by chemical vapor deposition (CVD) on separate SiO$_2$/Si substrates$^2$ (chips of approx. 1.5×2 cm) and transferred onto the Al$_2$O$_3$, as detailed in Section 1.2. Next, we pattern and e-beam evaporate Au (55 nm) to form the source and drain contacts to the transistors. The channel length of our transistors ranges from 2 to 15 μm, which is within the limits of optical lithography on PEN substrates. We also define and evaporate Ti (3 nm)/Cu (30 nm)/Au (5 nm) pads connected to the Au contacts for device probing. We note that before metal deposition of the pads, we etch the MoS$_2$ underneath this region to improve the adhesion of the metal to the PEN substrate. The MoS$_2$ is etched using O$_2$ plasma with 100 sccm O$_2$ at 150 mTorr at a power of 50 W for 45 seconds. Finally, the MoS$_2$ channel is patterned and etched into a rectangle to define the width of the transistor channel using the same etch conditions. We note that the fabrication processes outlined here do not damage the MoS$_2$ film or leave photoresist residue.$^3$
1.2 MoS₂ transfer process

We describe the steps used to transfer MoS₂ onto PEN substrates as follows.⁴

1. Place thin strips of tape (Nitto Denko RevAlpha series thermal release tape or Kapton) on all four edges of the chip with MoS₂ grown by CVD on SiO₂/Si.
2. Spin-coat 2% PMMA at 2500 rpm for 1 minute, and then bake for 45 seconds at 135°C.
3. Spin-coat polystyrene (PS) dissolved in toluene (PS/toluene 3 g/20 mL) at 2000 rpm for 1 minute, and then bake for 5 minutes at 85°C.
4. Remove the tape very carefully from edges of the chip.
5. Place MoS₂ sample with polymer support layers in a beaker of water. Agitate sample in water to cause delamination of MoS₂/polymer stack from growth substrate. Use tweezers to poke edges of the polymer stack to initiate delamination from substrate.
6. If MoS₂/polymer stack does not delaminate in water, place sample in a beaker of 1M NaOH for a few minutes to etch SiO₂ and promote delamination from the substrate. After the MoS₂/polymer stack begins to delaminate from the SiO₂/Si substrate, return the chip to a fresh beaker of water. Return to step 5 until the entire film has delaminated from the substrate.
7. After the MoS₂/polymer film has delaminated from the growth substrate, it will float on the water. Use the PEN to pick up the floating sample.
8. Carefully blow a N₂ gun perpendicular to the sample to remove water trapped between the MoS₂ and PEN.
9. Place the sample on a hot plate at 55°C for 5 minutes, then increase the temperature to 85°C and heat the sample for 5 minutes, and finally increase the temperature to 135°C. This gradual increase in temperature minimizes damage (e.g. bubbles and holes) to the MoS₂ film after the transfer. When the temperature reaches 135°C, remove the sample from the hot plate.
10. Place the obtained polymer/MoS₂/PEN stack in toluene for 12 hours to dissolve the PMMA and PS polymers. Rinse the sample in acetone and IPA after removing it from toluene.
2. Raman and photoluminescence (PL) spectroscopy of devices with strain

We use Raman and photoluminescence (PL) spectroscopy to confirm that the MoS$_2$ is under tensile strain, in addition to the visual inspections shown in Figure 2b of the main text.

Figure S2a-b below illustrates the E’ (in-plane) and A$_1'$ (out-of-plane) Raman peak positions for 10 devices, respectively. The data are presented as box plots for 0%, 0.7%, and back to 0% applied tensile strain. For each transistor, we averaged the Raman peak positions over ~5 spots across the channel. The average E’ peak positions across all 10 devices after device fabrication, with 0.7% strain, and after the strain is released are $384.6 \pm 0.1$ cm$^{-1}$, $382.8 \pm 0.4$ cm$^{-1}$, and $384.6 \pm 0.2$ cm$^{-1}$, respectively. This marks a $2.5 \pm 0.5$ cm$^{-1}$/% strain shifting rate of the E’ peak.

As expected, the shift of the A$_1'$ Raman peak (at ~403 cm$^{-1}$) is lower ($1.0 \pm 0.3$ cm$^{-1}$/% strain) than that of the E’ peak. This shift may be partially due to altered substrate interactions rather than purely a direct strain effect on the out-of-plane vibrations.\(^5\)

We note that some studies report peak splitting of the degenerate E’ Raman mode with tensile strain due to breaking the symmetry of the crystal.\(^6\)\(^7\) Our MoS$_2$ E’ peak did not exhibit such behavior, likely because the MoS$_2$ did not experience large enough strains.

We also perform PL spectroscopy on our samples to study the change in the optical band gap as a function of strain, with the A and B excitons schematically illustrated in Figure S3a. Figure S3b shows the position of the A exciton peak at 0%, 0.4%, 0.6%, and back to 0% strain. Each box plot represents data from 7 transistors, and for each transistor we averaged the peak position over 3 spots in the channel region. The average A exciton peak positions at 0% strain, 0.4% strain, 0.6% strain, and back to 0% strain are $1.813 \pm 0.004$ eV, $1.793 \pm 0.005$ eV, $1.773 \pm 0.005$ eV, and $1.814 \pm 0.005$ eV, respectively. We also point out that the PL peak intensity decreases slightly with increasing tensile strain (see Figures 2d-e in the main text), due to a narrowing of the indirect optical gap of monolayer MoS$_2$ between the $\Gamma$ (valence) and $K$ (conduction) points.\(^6\)\(^8\)

Figure S2. Box plots showing (a) E’ and (b) A$_1'$ Raman peak positions. The figures include data averaged from ~5 spots across the channels of all devices and show Raman peak positions before applying strain, with 0.7% strain, and after the strain returns to 0%.
We note that CVD-grown MoS$_2$ typically attains some built-in tensile strain during the growth process, due to the larger thermal coefficient of expansion (TCE) of MoS$_2$ compared to the underlying SiO$_2$.\textsuperscript{11} Transferring the MoS$_2$ to another substrate should release this built-in strain, so we expect that the MoS$_2$ is either unstrained or slightly compressively strained upon transfer to the PEN. However, the Raman and PL peak positions of unstrained MoS$_2$ are difficult to determine because these peaks are affected by many factors in addition to strain, such as doping and substrate interactions.\textsuperscript{5,11-13} Our MoS$_2$ is transferred onto Al$_2$O$_3$, which is known to cause peak shifts in the Raman and PL spectra of MoS$_2$.\textsuperscript{14} Therefore, we are unable to conclude whether our devices initially have any built-in tensile or compressive strain from the transfer and fabrication processes.

### 3. Current-voltage characteristics of MoS$_2$ transistors with strain

We perform electrical measurements with a Keithley 4200-SCS using Keithley Interactive Test Environment (KITE) software. Figure S4 shows the same $I_D$-$V_{GS}$ curves from Figure 3a of the main text but here includes the reverse sweep (dashed lines) in addition to the forward sweep (solid lines). The difference between the forward and reverse voltage sweep measurements points to hysteresis in the device, likely arising from electrostatic screening by H$_2$O and O$_2$ adsorbates trapped at the MoS$_2$-Al$_2$O$_3$ interface during the transfer process.\textsuperscript{15} The gate current ($I_G$) at different strain levels is depicted by the dotted lines and does not exceed 1.2 nA during any of the measurements, indicating that the leakage current through the gate dielectric remains low during all strain-dependent measurements.

The $I_D$-$V_{DS}$ measurements shown in Figure 3b of the main text include forward and backward voltage sweeps with no observable hysteresis, which also suggests that the traps are located at the MoS$_2$-Al$_2$O$_3$ interface or within the Al$_2$O$_3$, and are mainly affected by sweeping the gate voltage.
Figure S4. Measured $I_D$-$V_{GS}$ curves showing forward (solid) and backward (dashed lines) sweeps at different strain levels, for the same device shown in Figure 3a of the main text, with $W = 20 \, \mu m$, $L = 8 \, \mu m$, and $V_{DS} = 1 \, V$. The gate current ($I_G$) at different levels of strain is depicted by the dotted lines and does not exceed 1.2 nA for all measurements.

4. **C-V characteristics of Au-Al$_2$O$_3$-Au capacitors with strain**

We characterize the capacitance of the Al$_2$O$_3$ gate oxide using metal-oxide-metal structures (see Figure S5a for a top-view schematic) to enable more accurate estimation of field-effect mobility ($\mu_{FE}$). We verify that the capacitance does not change with strain, as shown in Figure S5b. We measure an oxide capacitance $C_{ox} \approx 312 \, \text{nF/cm}^2$, which we use in our calculation of $\mu_{FE}$. With ellipsometry, we estimate an Al$_2$O$_3$ thickness $t_{ox} \sim 20 \, \text{nm}$, which gives a relative dielectric constant $\varepsilon_{ox} \sim 7$ for our Al$_2$O$_3$, based on the equation $C_{ox} = \varepsilon_{ox} \varepsilon_0 / t_{ox}$, where $C_{ox}$ is normalized by the area of the Au electrode overlap and $\varepsilon_0 = 8.85 \times 10^{-14} \, \text{F/cm}$. The equivalent oxide thickness ($EOT = \varepsilon_{SiO2} t_{ox}/\varepsilon_{ox}$) of our Al$_2$O$_3$ film is $\sim 11 \, \text{nm}$. The alternating current (AC) frequency and voltage bias during the measurements are 20 kHz and 30 mV, respectively. 

Figure S5. (a) Schematic of Au-Al$_2$O$_3$-Au structure for capacitance-voltage measurements. (b) Capacitance-voltage measurements of an Au-Al$_2$O$_3$-Au test structure with and without 0.7% tensile strain. The capacitance is normalized by the area of the top and bottom Au electrode overlap.

5. **Mobility ($\mu_{FE}$) and drain current ($I_D$) as a function of tensile strain**

Figure S6a-b shows the magnitudes of $\mu_{FE}$ and $I_D$ as a function of strain, with each color corresponding to a different device. The data for 8 devices shown here correspond to the same data...
represented in box plots in Figure 3c-d of the main text. All values of $\mu_{FE}$ are extracted at the same carrier density $n \sim 1.1 \times 10^{13}$ cm$^{-2}$ and $V_{DS} = 1$ V, and all values of $I_D$ are extracted at $V_{GS} = 7$ V and $V_{DS} = 1$ V. The data points on the right side of each plot show $\mu_{FE}$ and $I_D$ after the strain is released back to 0%. We note that the unstrained mobilities are lower than in some other MoS$_2$ studies,$^{2,16}$ which we attribute to growth variations and partial degradation of the MoS$_2$ after transfer to the flexible substrates. We also perform strain-dependent electrical measurements on a different set of monolayer MoS$_2$ transistors with higher initial mobilities, which is discussed in Section 6.

Figure S6. (a) Mobility ($\mu_{FE}$) and (b) drain current ($I_D$) for 8 different devices at 0%, 0.4%, 0.6%, 0.7%, and back to 0% strain. Channel lengths of these devices are $L = 2$ to 15 $\mu$m, also see Figure S7.

Figure S7. (a) Normalized $\mu_{FE}$ and (b) normalized $I_D$ at 0.7% tensile strain as a function of channel length. The mobility and current are normalized to their unstrained values (subscript “0”).

We plot normalized $\mu_{FE}$ and $I_D$ at 0.7% strain as a function of $L = 2$ to 15 $\mu$m (see Figure S7a-b). There is no noticeable trend of mobility or current improvement with strain for different channel lengths, indicating that contact effects do not play a significant role across this range of channel lengths. Some theoretical studies have also predicted a directional (armchair vs. zigzag) dependence of MoS$_2$ mobility on strain.$^{17}$ However, the theoretical predictions are virtually indistinguishable at the lower strains applied in our work (<1%) and they are below our measurement sensitivity. In other words, we cannot conclude whether the variability observed in Figure S7 is due to applying strain along different crystallographic directions or (more likely) due to device and fabrication non-uniformity.
Figure S8a-b shows absolute and normalized $\mu_{FE}$ as a function of strain at a lower carrier density ($n \sim 4.8 \times 10^{12} \text{ cm}^{-2}$). The absolute and normalized $\mu_{FE}$ at lower $n$ are slightly lower than those at higher $n$ (see Figure S6a and Figure 3c in the main text), but the overall trends are similar.

![Figure S8](image)

**Figure S8.** (a) Mobility ($\mu_{FE}$) and (b) normalized mobility ($\mu_{FE}/\mu_{FE,0}$) for the same 8 devices as in Figure S6-S7, at 0%, 0.4%, 0.6%, 0.7%, and back to 0% tensile strain at a lower carrier density $n \sim 4.8 \times 10^{12} \text{ cm}^{-2}$. The $\mu_{FE}$ in (b) is normalized to the initial (unstrained) values, with the box plots showing the median across devices (red circles), first and third quartiles (blue box), and maximum and minimum (top and bottom lines, respectively). The red “+” symbols represent outliers in the data. The cyan box plot corresponds to the measurement after strain is released.

6. Degradation of devices at high levels of strain

At strain greater than 0.7%, we observe a degradation of mobility and current in all devices. Figure S9a depicts this decrease in mobility at 0.8% strain during the 1st measurement of a second set of devices. When the strain returns to 0%, the mobility decreases further. However, the 2nd measurement (Figure S9b) shows an increase in mobility when strain is again applied to the devices, though it is lower than the improvement in mobility observed in Figure S6. These results demonstrate that there is a “break-in” of the device when the strain exceeds 0.7%, resulting in a degradation in performance.

![Figure S9](image)

**Figure S9.** Field-effect mobility $\mu_{FE}$ as a function of larger tensile strain for devices on a different sample. Each color corresponds to a different device. (a) First measurement of devices at 0%, 0.8%, and back to 0% strain, showing a degradation in mobility. (b) Second measurement after device “break-in” at 0%, 0.8%, and back to 0% strain, this time showing an improvement in mobility at 0.8% strain, but lower mobility overall.
Figure S10. Current $I_D$ as a function of larger tensile strain for the same devices shown in Figure S9. Each color corresponds to a different device. (a) First measurement of devices at 0%, 0.8%, and back to 0% strain, showing a degradation in current. (b) Second measurement after device “break-in” at 0%, 0.8%, and back to 0% strain, this time showing an improvement in current at 0.8% strain.

Figure S10a-b shows the same trends of current $I_D$ at higher strain, i.e. an initial decrease in current with strain during the first measurement and subsequently an increase in current with strain during the second measurement. Once the strain is released the second time, $I_D$ and $\mu_{FE}$ return to the same levels as before the second measurement. We point out that the device measurements displayed in Figure S9 and Figure S10 have higher initial unstrained mobilities and drive currents than the device measurements shown in Figure S6, but we were unable to further improve the mobility with strain because of device break-in and degraded electrical performance at 0.8% strain.

Figure S11. $I_D$-$V_{GS}$ measurements at 0% and 0.3% strain for a transistor with $W = 20 \mu m$ and $L = 2 \mu m$ on a different sample. The mobility increases from $\sim 25 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ at 0% strain to $\sim 34 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ at 0.3% strain at $n \sim 7 \times 10^{12} \text{ cm}^{-2}$.

We also perform strain-dependent electrical measurements on a third set of monolayer MoS$_2$ transistors with higher initial mobilities ($\sim 15 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ to 35 cm$^2$V$^{-1}$s$^{-1}$). Transfer characteristics from one of these transistors are included in Figure S11. The mobility and current of these devices improve with $\sim 0.3\%$ strain, but the devices degrade at higher levels of strain (not shown). The mobility of the device in Figure S11 increases from $\sim 25 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ with 0% strain to $\sim 34 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ with 0.3% strain at $n \sim 7 \times 10^{12} \text{ cm}^{-2}$. 
We attribute the degradation in electrical performance at higher strains to cracking in the metal or Al₂O₃ gate dielectric, or worsened adhesion of the contact metal to the MoS₂. When strain greater than 1% is applied to the MoS₂ devices, we observe obvious cracks in the metal or Al₂O₃ layers (see Figure S12). Although we did not observe such cracks in the devices measured in Figures S9-S11, this could still be the source of device degradation. Raman measurements (see Figure S13) showing the expected shift in the E’ peak prove that the MoS₂ remains strained at 0.8%, and that the MoS₂ is not “slipping” against the substrate.

**Figure S12.** (a) Optical image of a device after >1% strain was applied. (b) Zoomed-in region showing fine cracks in the metal gate and/or the Al₂O₃ gate insulator under the MoS₂ channel. Small arrows point to the fine cracks.

**Figure S13.** Raman spectra at 0% and 0.8% tensile strain for one of the devices that degraded electrically at 0.8% strain. The data are depicted as symbols, and the fits using a superposition of Lorentzian and Gaussian peaks are displayed as solid curves. The redshift in the E’ peak shows that the MoS₂ is still strained (even after the electrical degradation of the transistor) and does not slip against the substrate.

7. **Supplementary References:**

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