A V-band Integrated Receiver Front-End Based on 0.15 μm GaAs pHEMT Process for Passive Millimeter-wave Imaging

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ABSTRACT The design, analysis, implementation and measurement of an integrated V-band receiver front-end based on 0.15 μm GaAs pHEMT process are presented in this paper. The front-end chip uses the super-heterodyne topology which consists of a low noise amplifier, an image reject mixer, and a multiply-by-four (×4) LO chain. In order to minimize the power consumed by LO chain, an active single-ended mixer is designed which requires extremely low LO power of -5 dBm. Meanwhile, the effect of signal coupling in the integrated chip is analyzed and solutions are proposed. By introducing appropriate filters into the circuit and optimizing the overall layout, the imbalance of in-phase and quadrature signals caused by unwanted coupling can be effectively mitigated, thus enhancing the image rejection of the chip. Probe and module tests are applied to the receiver front-end, and the measurement results reveal that the chip achieves -3 ± 0.7 dB conversion gain, 7 dB noise figure and more than 25 dB image rejection ratio in the RF frequency range of 52-56 GHz. Only one supply voltage of 3 V is required for the chip, and total power consumption is 312 mW. Moreover, with a continuously adjustable phase control of 360° and very broadband IF characteristics, the front-end chip is suitable for passive millimeter-wave imaging applications.

INDEX TERMS Integrated receiver front-end, V-band, low LO power, high image rejection, 0.15 μm GaAs pHEMT, passive millimeter-wave imaging.

I. INTRODUCTION Passive millimeter-wave imaging (PMWI) has been demonstrated as an effective technology for security screening due to its ability of detecting weapons hidden beneath clothing without generating harmful radiation [1, 2]. Compared with the existing Ka-band and W-band PMWI systems [3, 4], V-band imagers can achieve good performance of clothing penetration and spatial resolution with a moderate aperture, showing great potential in security applications. To reduce scanning time, security imagers generally perform electronic beam steering with compact linear or full two-dimensional receiver arrays [5]. Therefore, a low-cost and integrated receiver front-end is desired for the emerging V-band security imagers. In addition, the front-end for radiometer application should have flat gain and low noise figure (NF) in wide operation band, because these parameters directly determine the radiometric sensitivity. For our security imager that uses a joint technology of phased array and synthetic aperture [6], the main requirements for the receiver front-end are: 1) gain flatness better than ±1 dB and NF less than 8 dB within 4 GHz operation band, and 2) a continuously adjustable phase-control range of 360°.

Generally, both direct detection receiver and super-heterodyne receiver can be used for radiometers. The main attraction of the direct detection architecture is its low cost, small size, and low power consumption. However, radiometers usually suffer from various sources of degradations when using direct detection receivers, such as difficulty in amplification of millimeter-waves, gain fluctuation with phase shifting, and low detection sensitivity [7, 8]. In comparison, as the received millimeter-waves are down-converted to IF signals in super-heterodyne front-end,
signals are easily amplified and detected with high sensitivity at lower frequencies [9]. Despite more components, the monolithic microwave integrated circuit (MMIC) technology makes it possible to develop a fully integrated, highly compact super-heterodyne front-end. In the past few years, many MMIC receiver front-ends have been proposed in various semiconductor processes [10-12]. In general, GaAs and InP processes are adopted to obtain low NF and high gain at millimeter-wave band. Compared with the InP technology which can provide considerable gain at Terahertz [13], GaAs process is usually used for designing circuits below 100 GHz economically. In addition, SiGe and CMOS processes are emerging for realizing millimeter-wave MMICs recently [14-17]. Despite the high degree of integration and low power consumption, silicon-based technologies usually suffer from high noise due to the lossy dielectric, and the chip development cost is high.

Among the GaAs processes, 0.15 μm GaAs pHEMT process has a cut-off frequency of 88 GHz and exhibits reliable performance in previous designed Ka-band circuits [18-20]. However, few attempts have been made to adopt this process for circuits beyond 40 GHz due to the performance deterioration and inaccuracy of simulation models. One of the major difficulties in designing V-band super-heterodyne front-end with this process is the low gain of the transistor. To provide sufficient LO power for the mixer, large numbers of amplifiers are required in the LO chain, which greatly increase the power consumption of the chip. In addition, as many devices are integrated into a compact chip, the undesired signal coupling becomes significant, which would cause severe deterioration of image rejection due to the in-phase and quadrature imbalance. Hence, efforts have to be made to suppress the unwanted signal coupling. A representative work of V-band super-heterodyne receiver front-end based on 0.15 μm GaAs pHEMT process is presented by Gunnarsson et al. [21]. The method to reduce LO signal power is adopting a resistive single-ended image reject mixer (IRM) instead of the balanced topologies. As the LO power is 1 dBm, the receiver achieves 8 dB gain and 10.5 dB noise figure at 60 GHz with a power consumption of 990 mW. Besides, image rejection ratio (IRR) of 20 dB is obtained in 1.8 GHz bandwidth when providing a fixed LO signal. The receiver can well meet the requirement of communication but is not very desirable for radiometer application.

In this paper, a V-band super-heterodyne receiver front-end is designed for phased array radiometer application. The main contributions of this paper are summarized as follows.

1) We first demonstrate that 0.15 μm GaAs pHEMT process is a well promising technology for realization of V-band integrated radiometer receiver front-end. Within the RF frequency band of 52-56 GHz, the front-end achieves -34±0.7 dB conversion gain, 7 dB average noise figure, 360° continuously adjustable phase shifting, and more than 25 dB IRR. To the knowledge of the authors, the best results reported to date are reached for a V-band receiver front-end with very broadband IF characteristics in 4-10 GHz.

2) we propose a strategy that can reduce the power consumption of the receiver front-end based on 0.15 μm GaAs pHEMT process. By taking advantage of an active single-ended mixer without increasing extra power consumption, the LO drive power is reduced and fewer amplifiers are needed in the LO path.

3) The relationship between signal coupling and IRR is revealed, which provides a criterion for integrated front-ends design. By introducing a novel absorption band-pass filter into the LO path and designing a CPWG cross-over structure, the unwanted coupling signals are effectively suppressed, resulting in enhanced IRR.

4) Extensive range of simulations and experiments shows that the designed chip achieves suitable performance with respect to the PMMI application, which provides new insights for radiometer front-end design using low cut-off frequency and low cost processes.

II. INTEGRATED RECEIVER FRONT-END OVERVIEW

The block diagram of integrated receiver front-end is shown in Fig. 1. It consists of a low noise amplifier (LNA), an IRM, and a multiply-by-four LO chain which includes a drive amplifier, an analog phase shifter, a quadrupler and an absorption band-pass filter (ABF). Our previous work on real-time security imager (BHU-1024) has demonstrated that 4 GHz bandwidth is sufficient for measurement sensitivity [6]. In order to obtain relatively high gain with 0.15 μm GaAs pHEMT process, an operation frequency band of 52-56 GHz is selected for the receiver front-end. With a fixed LO signal of 48 GHz (12 GHz × 4), the RF signal is down converted into 4-8 GHz IF signals.

![FIGURE 1. Schematic of the integrated V-band receiver front-end.](image-url)
the image, because high Q filtering is practically difficult and area-consuming. But the IRM requires twice as many transistors and higher LO drive power. Our previous work on the double-balanced resistive mixer based on 0.15 μm GaAs process requires 10 dBm LO power. It is difficult to generate such a high-power signal at 48 GHz efficiently due to the low gain of this process. Consequently, a low LO power mixer is designed for the receiver front-end.

Since the receiver front-end is designed for phased array application, an analog phase shifter is added into the LO chain before the quadrupler. Compared with traditional phased array controlled by RF phase shifting, LO phase shifting can easily realize phase control of wideband RF signals, and alleviate the gain fluctuation with phase shifting. In addition, a band-pass filter is placed at the output of quadrupler to suppress the undesired harmonics.

III. LOW LO POWER IMAGE REJECT MIXER

The mixer is characterized as down converter from 52 to 56 GHz with respect to conversion loss and IRR. In order to reduce LO drive power, single-ended topology is applied to the mixer because it has the minimum number of transistors compared with balanced topologies. Meanwhile, by taking advantage of active FET mixer, the LO power can be further reduced.

FIGURE 2. Schematic of the image reject mixer.

The schematic of the designed IRM is shown in Fig. 2. It consists of two active mixers. The positive voltage is fed into the drain terminal of the transistor. Parallel resistor and capacitor network is connected to the source terminal to realize the self-bias structure. To obtain the in-phase and quadrature signals, a Lange coupler is used to split the RF signal and a power divider is adopted for LO splitting. This is because Lange coupler can provide low reflection of RF signal with the benefit of its structure even if there are some unpredictable deviations in the simulation models. In addition, Lange coupler is also used as a diplexer to isolate the LO and RF ports. In the mixer, the LO signal is fed into gate terminal where the time-varying transconductance is the dominate contributor to frequency conversion and the variation of other parameters is minimal. At the gate terminal, a high-pass filter is designed to suppress the leakage IF signal. Similarly, a low-pass filter is used at the drain terminal to provide over 20 dB suppression of RF and LO signals.

FIGURE 3. Simulated conversion gain of active and passive single-ended mixers under different Vgs.

Numerical optimization is implemented by Agilent Advanced Design System (ADS) to obtain the best conversion response and LO drive power. An active FET single-ended mixer is simulated at 54 GHz under different bias voltages (Vgs) when the positive supply voltage is set as 3 V, and the FET size is 2 × 50 μm. A passive FET single-ended mixer is also simulated for comparison. The required LO power is characterized by the input-referred 1 dB compression point. As shown in Fig. 3, with increase of the Vgs, conversion gain increases, but higher LO power is required. It suggests there is a compromise between the conversion gain and LO power. When the Vgs is ~0.7 V, the active mixer can operate with a low LO power of -5 dBm and realize a relatively low conversion loss of 10 dB. It can be also found that as opposed to the passive mixer which requires 5 dBm LO power, active topology has obviously reduced LO power and similar conversion gain. In addition,
the conversion gain versus transistor gate width (Ugw) is simulated when the finger number is 2 and the Vgs is -0.7 V. As shown in Fig. 4, the mixer shows significant rise in conversion gain when the gate width increases from 10 to 50 μm. With further increase of the gate width, improvement of conversion gain is very limited but higher LO power is required. Therefore, the $2 \times 50$ μm FET biased at -0.7 V is used for the mixer design.

A photograph of the designed IRM is shown in Fig. 5. With input and output GSG ports, the chip measures 2 mm × 1.5 mm. The mixer only consumes 0.7 mA current under 3 V power supply. Driven by a 48 GHz LO signal with -5 dBm power, the mixer has a flat conversion gain of -13 dB in 52-59 GHz, as shown in Fig. 6. The measured conversion gain is about 1 dB lower than simulation, which could be attributed to the larger resistive parasitism. In Fig. 7, measured conversion gain at 54 GHz is plotted as a function of LO power. It clearly shows that -5 dBm power is sufficient to drive the mixer. With further increase of LO power, the rise of conversion gain is very limited. Additionally, the mixer has a good balance performance of in-phase and quadrature signals. The amplitude imbalance is measured as 1 dB and the phase imbalance is lower than 5°.

FIGURE 5. Photograph of the image reject mixer.

FIGURE 6. Measured conversion gain of the IRM versus RF frequency.

IV. ANALYSIS AND SOLUTIONS FOR SIGNAL COUPLING

In the integrated circuit, one of the most critical problems is the undesired signal coupling. First, the single-ended topology used in the mixer has a low isolation between RF and LO ports. The LO signal leaked to RF port can be absorbed by the LNA which has an excellent output matching at 48 GHz. However, it is difficult to simultaneously suppress the leakage RF and image signals within a ultra-wideband at LO port. As a result, the reflected RF and image signals are in-phase separated by the power divider, leading to imbalance in the quadrature demodulation. To illustrate this phenomenon, the RF and image signals fed into the transistors of two branches are expressed as:

$$x_{RF/IM,1} = \cos(\omega t) + \Gamma \cos(\omega t + \theta)$$

$$x_{RF/IM,2} = \sin(\omega t) + \Gamma \cos(\omega t + \theta)$$

where $\omega$ is the frequency of RF or image signal. $\Gamma$ represents the normalized amplitude of the reflected signal from the LO port, which is twice as large as the isolation between transistor’s gate terminal and LO port. $\theta$ denotes the phase of the reflected signal.

There is another case that the balance performance of mixer can be affected. Because a cross-over of LO and IF path is inevitable in the integrated chip, a leakage LO signal will be coupled to one of mixer’s branch and cause in-phase and quadrature imbalance. In this case, the LO signals fed into the transistors of mixer can be expressed as:

$$x_{LO,1} = \sin(\omega_{LO} t)$$

$$x_{LO,2} = \sin(\omega_{LO} t) + K \sin(\omega_{LO} t + \theta)$$

where $\omega_{LO}$ denotes the frequency of LO signal. K and $\theta$ are normalized amplitude and phase of the leakage LO signal. Because the phase of the coupling signal is difficult to precisely control, the maximum amplitude and phase imbalance is calculated and shown in Fig. 8. It is obvious that the reflection of RF and image signals and LO leakage will reduce the balance performance of mixer significantly.

FIGURE 7. Measured conversion gain of the IRM versus LO power.
To illustrate the influence of signal coupling on image rejection clearly, the two cases discussed above are investigated separately. For the first case, the RF signal and its image that input to transistor $s$ can be defined as:

$$x_I = \sin(\omega_{RF}t) + \sin(\omega_{IM}t)$$

$$x_Q = \delta [\cos(\omega_{RF}t + \phi) + \cos(\omega_{IM}t + \phi)]$$

where $\omega_{RF}$ and $\omega_{IM}$ denote the frequencies of RF signal and its image. $\delta$ and $\phi$ are the amplitude and phase imbalance caused by reflection at LO port. The LO signal is defined as:

$$x_{LO, I} = x_{LO, Q} = \sin(\omega_{LO}t)$$

For the second case, the input signals are perfectly orthogonal which can be expressed as:

$$x_I = \sin(\omega_{RF}t) + \sin(\omega_{IM}t)$$

$$x_Q = \cos(\omega_{RF}t) + \cos(\omega_{IM}t)$$

while the in-phase LO signals are degenerated into:

$$x_{LO, I} = \sin(\omega_{LO}t)$$

$$x_{LO, Q} = \delta \sin(\omega_{LO}t + \phi)$$

where $\delta$ and $\phi$ are the amplitude and phase imbalance caused by LO leakage.

At the output of the mixer, I/Q signals are combined by a 90° hybrid. A same expression of the combined IF signal can be deduced for the two cases which is given as:

$$x_{IF} = x_{IF, RF} + x_{IF, IM}$$

$$= \frac{1}{2} \cos[(\omega_{RF} - \omega_{LO})t + \phi] + \delta \cos(\omega_{RF} - \omega_{LO})t + \phi$$

$$+ \frac{1}{2} \cos[(\omega_{LO} - \omega_{IM})t - \phi] - \frac{\delta}{2} \cos[(\omega_{LO} - \omega_{IM})t - \phi]$$

Then the IRR of the mixer can be calculated as:

$$\text{IRR} = \frac{P_{IF, RF}}{P_{IF, IM}} = 10 \log_{10}(\frac{1 + \delta^2 + 2\delta \cos \phi}{1 + \delta^2 - 2\delta \cos \phi})$$

The IRRs of the mixer for the two discussed cases are plotted in Fig. 9. For the designed mixer, the isolation between transistor’s gate and LO port is only 6 dB. If the RF and image signals are completely reflected at LO port, $\Gamma$ is -12 dB and only -11 dB IRR is obtained. To achieve more than 20 dB IRR, the reflection of RF and image signals has to be suppressed to lower than -20 dB. Therefore, we adopt an absorption band-pass filter at the mixer’s LO port.

The basis topology of the absorption band-pass filter is plotted in Fig. 10 (a), which contains two Lange coupler and two reflecting band-pass filter (RBF). The signal is input from port 1 and divided into two quadrature signals. Then the pass-band signals transmit through the RBFs and are combined in-phase by the output coupler. Meanwhile, the reflected stop-band signals are combined in opposite polarity at port 1 and absorbed by the resistor at port 3. Therefore, the
absorption bandwidth of the filter mainly depends on the Lange coupler, while the pass band is restricted by the RBF.

In order to absorb the leakage RF and image signals, a Lange coupler operating at 40-56 GHz is designed for the ABF. For the RBF, we adopt parallel-coupled micro-strips as resonators to obtain the required passband at 48 GHz. To further reduce the chip size, inductors realized by short stubs are added onto the coupled lines, such that the length of coupled line can be reduced to $\lambda/8$. In addition, two transmission zeros are introduced into the filter by taking advantage of the cross-coupling effect [22]. In this way, the unwanted harmonics of 36 GHz and 60 GHz are significantly suppressed. As shown in Fig. 11, the ABF has a pass band of 46-50 GHz with an insertion loss of 2.2 dB. The return loss lower than -14 dB is achieved in an ultra-wide band below 60 GHz.

![Graph showing IRRs of the IRM with ABF and RBF.](image)

**FIGURE 12.** IRRs of the IRM with ABF and RBF.

The proposed strategy is verified by comparing the IRRs of the mixer when ABF and RBF are used at the LO port. As shown in Fig. 12, the mixer achieves an IRR better than 29 dB over 6 GHz bandwidth when the ABF is used. In contrary, an RBF at LO port leads to a low IRR of 10 dB, which agrees well with the calculation results in Fig. 9. Simulation results show that the IRR degradation caused by poor isolation of mixer can be well solved by the ABF.

To obtain a high IRR for the integrated front-end, the suppression of LO leakage is also required. First, the crossover in LO and IF transmission path is designed using coplanar waveguide ground (CPWG), which can provide 23 dB isolation at 48 GHz. Besides, the bridging is taken place after the low-pass filter in the mixer. It can further suppress the LO signal leakage to transistor. Through above measures, the leakage coefficient $K$ is lower than -40 dB, introducing little impact on IRR.

V. MEASUREMENTS OF THE INTEGRATED RECEIVER FRONT-END

The main individual building blocks of the receiver front-end have been fabricated and measured previously. By using 4-stage common source amplifier with self-bias topology, the LNA achieves the gain of 14.9 $\pm$ 0.3 dB and NF of 3.5 dB in 51-57 GHz. With 3-stage buffer amplifier, the quadrupler generates 0 dBm LO signal at 48 GHz which meets the requirement of the mixer. The analog phase shifter is designed by using 4-stage distributed high-pass filters in which variable capacitors are realized by reverse-biased diodes. By properly choosing capacitance and inductance, the phase shifter provides $101^\circ$ phase shift at 12 GHz with a low insertion loss of 2 dB. To realize an optimized overall performance, ADS is used to design the integrated receiver front-end. Yield analysis is also performed to keep the circuit not sensitive to process variation. In simulation, yield variables are varied around the nominal values using the probability distribution functions provided by foundry, and then yield is estimated by counting the ratio of the number of designs that pass the performance specifications to the total number of designs. The summary of yield analysis for the proposed receiver front-end chip taken for 200 iterations is presented in Table I.

**TABLE I: YIELD ANALYSIS SPECIFICATIONS**

| Parameters          | Specifications | Yield |
|---------------------|----------------|-------|
| Conversion gain     | $>-2$ dB       | 94%   |
| NF                  | $<7.5$ dB      | 98%   |
| IRR                 | $>26$ dB       | 96%   |
| Phase shift range   | $>360^\circ$   | 100%  |

A photograph of the fabricated chip is given in Fig. 13. The chip size is 5 mm $\times$ 4 mm. For easily measurements, the receiver chip is assembled onto a test circuit supported by a metal platform. DC pads are connected to the PCB circuit through bonding wires. Coplanar GSG probes are applied for signal feeding and extraction. The nominal frequencies for RF, IF and LO are 52-56 GHz, 4-8 GHz and 48 GHz, respectively. As the input LO power is -15 dBm, the measured conversion gain of the chip is shown in Fig. 14. In the frequency band of 51-58 GHz, the measured conversion gain is -3 $\pm$ 0.7 dB with a peak value of -2.3 dB at 54 GHz. Meanwhile, it can be found that the measured conversion
gain is about 2 dB lower than the simulation results. The source of this discrepancy is not definitely known at this point but larger resistive parasitism is a possible cause. Besides, the higher ripple of the frequency response could originate from the noise picked up by the un-calibrated probe station.

The IRR of the receiver front-end is measured by assembling the die chip on a test module with an off-chip 90° hybrid. The off-chip 90° hybrid has ±2° phase imbalance and <0.6 dB amplitude imbalance in the frequency band of 4-8 GHz. In Fig. 15, the measured and simulated IRRs are plotted as a function of the IF frequency. By suppressing the unwanted signal coupling in the integrated circuit, more than 25 dB IRR is measured within a wide IF band range from 4 to 10 GHz. It can be noticed that a peak value appears at 6.5 GHz, which could be attributed to that the imbalance of I/Q signals happens to be compensated by the imperfect hybrid at this frequency. On average, the measured IRR agrees well with the simulation result and demonstrates the analysis in section IV.

The measured NF of the receiver MMIC are plotted in Fig. 16. At frequency of 52.5-58 GHz, NFs of I/Q channels are in the range of 6.5-8 dB, while a higher NF of 9.5 dB is measured at 52 GHz. For radiometer application, the noise figure can be further improved by adopting an off-chip pre-LNA.

Finally, phase shift range of the receiver is measured by using another receiver chip as reference. As shown in Fig. 17, the receiver achieves continuous phase shift of over 400° as the control voltage varies from 0 to 2 V.

The characteristics of the designed integrated receiver front-end are summarized in Table I. Meanwhile, the state-of-the-art works on V-band receiver front-end chip are also presented for comparison. From Table I, it can be noted that our design outperforms the front-end chip based on the same process, except for the conversion gain [17]. This is because our chip is designed for radiometer application, which puts more emphasis on NF and wideband performance. Obviously, the Si-based chips can achieve the most compact size and low power consumption. High gain and low NF can also be obtained using Si-based process with high cut-off frequency, but the manufacturing cost is high. Compared with the other reported works in Table I, our work exhibits better wideband characteristic with respect to IF bandwidth, gain flatness, IRR and NF.
VI. CONCLUSION
In this paper, a V-band integrated receiver front-end based on 0.15 μm GaAs pHEMT process is implemented to serve PMMI application. For the super-heterodyne receiver, a strategy to reduce power consumption is proposed by taking advantage of the active single-ended IRM driven by an extremely low LO power. Furthermore, the relationship between image rejection and signal coupling in the integrated circuit is analyzed and corresponding methods are proposed to improve the image rejection. The front-end chip demonstrates the desired performance of imaging radiometers, its RF and IF bandwidth, conversion gain, IRR, NF and phase shift are presented and discussed. Our future work is adopting this receiver chip to phased array radiometers for security imaging. Then the performance of the designed receiver front-end can be further verified in system level.

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