Design of Ka-band broadband low-noise amplifier using 100nm gate-length GaN on silicon technology

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Abstract. Due to the high breakdown voltage and better linearity of gallium nitride (GaN) high electron mobility transistor (HEMT), GaN based RF front-end is widely researched and studied. In this paper, a Ka-band cascode low-noise amplifier (LNA) designed with 100nm gate-length GaN-on-silicon technology is presented. With novel methods such as the introduction of high-pass filters and standing wave filtering capacitors, the LNA achieves a stable gain of 21-22.8dB and a noise figure (NF) of 0.9-1.3dB from 22GHz to 38GHz. The input and output return loss are better than -10dB in band of concern. This LNA occupies an area of 2.3mm x 0.9mm and consumes 265-mW DC power. Compared with silicon-on-insulator (SOI), indium phosphide (InP) and gallium arsenide (GaAs) LNAs, the proposed GaN LNA exhibits better performance of linearity, as well as competitive gain and NF.

1. Introduction

Recently, the fifth-generation (5G) communication technology is developing rapidly due to lower latency, higher data rates and improved link robustness [1]. Because of the substantial increase in communication frequency, the attenuation of electromagnetic waves in the air will be more serious than 4G communication, which places unprecedented requirements on the output power of the transmitter and the sensitivity of the receiver. Consequently, the phased-array [2-3] and Multi Input Multi Output (MIMO) [4-5] technology is widely used to improve the communication efficiency and distance. Nowadays, most of the phased-array transceivers are designed and fabricated by BiCMOS technology. IBM presented a 28GHz phased-array transceiver fabricated by 130nm SiGe BiCMOS technology in 2017 [6], that integrated 16 front-ends in single chip. Their measurements exhibited that the equivalent isotropic radiated power (EIRP) achieved 54dBm with four packaged integrated circuits (ICs). Nevertheless, limited by SiGe process, a single RF front-end in this phased-array can only provide saturated transmit power of about 17dBm and input-referred 1dB compression point of about -25dBm, which requires more antennas to achieve high-power beamforming. Therefore, as the gate length of GaN HEMT advances to 100nm or even 70nm, the millimeter wave RF front-end based on GaN technology become a new option in phased-array transceivers to achieve higher power, better linearity and lower noise figure. In this paper, we present a GaN based Ka-band low noise amplifier, exhibiting excellent anti-jamming ability and competitive gain and NF.
GaN is a wide bandgap (3.5eV) semiconductor with high electron saturation velocity ($2.7 \times 10^7$ cm/s) and high electric breakdown field (350V/μm) [7-8]. Therefore, the HEMT fabricated by GaN material shows excellent power and linearity performance. The related microwave effects measurements and model extraction of GaN device are presented in [9-10]. With the rapid development of 5G applications, GaN based high power amplifiers (HPA) are gradually being focused and tend to replace GaAs HPA. In the past 5 years, The K/Ka band HPAs have been designed using 100nm GaN-on-Si technology [11-12], achieving output power of over 38dBm and PAE of about 30%. As the scaling down and optimization of GaN devices, OMMIC company has commercialized 70nm GaN HEMT process, which provides $f_t$ of over 300GHz and $\text{NF}_{\text{min}}$ of 0.5dB at 30GHz. It can be seen that GaN technology is developing towards lower noise and ultra-high frequency.

For low noise applications, GaN technology has many advantages over GaAs and SOI, such as higher power tolerance capacity and better linearity. The stress experiments in [13-14] show that, GaN LNA is undamaged at 30dBm input power for 1 minute or 40dBm input pulse, which means GaN LNA can work in complex electromagnetic scenarios without a limiter in front of LNA. For NF and gain of GaN based LNA, several researches and applications have been reported and proved their competition. A GaN LNA named CGY2250UH/C1 developed by OMMIC company has been released. It can provide a gain of 20dB and NF of less than 1.5dB from 26GHz to 34GHz. Another ultra-wideband (18-56GHz) GaN LNA has been reported in [15] in 2020. This LNA provides a gain of 16-21.5dB and NF of 2.2-4.4dB across the band.

In this paper, the presented LNA is designed with OMMIC’s 100nm GaN-on-Silicon HEMT process, whose cost is lower than 100nm GaN-on-SiC technology but having comparative noise performance. The fabricated HEMT has the features of over 100GHz $f_t$ and 190GHz $f_{\text{max}}$, that is suitable for designing Ka-band LNAs. Figure 1 shows the cross section of the 100nm GaN HEMT. The asymmetric T-gate is far from the drain to increase breakdown voltage between drain and gate. The regrown source/drain reduces the parasitic access resistance to minimize the NF. Furthermore, the process provides two metal layers, two types of MIM capacitors (metal-nitride-metal and metal-SiO$_2$-metal), two types of resistors with different precision (accurate NiCr resistor and large volume active layer resistors), spiral inductor, Lange coupler and through substrate via hole for grounding.

![Figure 1. Cross section of the 100nm GaN-on-Silicon HEMT.](image)

For GaN LNAs that have been reported in the past few years, three or four stage common source structure was used [16-18]. The excessive matching networks easily occupy a larger chip area. The current negative feedback through a resistor to flat in-band gain will deteriorate NF, thereby limiting the bandwidth (over 30GHz). Additionally, the stability is only concerned within working band, which may cause self-oscillation at higher frequency(60GHz).
In this paper, the designed two-stage cascode LNA achieves a flat gain of 21-23dB and a competitive NF of less than 1.3dB from 22GHz to 38GHz through setting high pass filters in inter-stage matching network without a feedback resistor. The K factor of each stage is designed to be greater than 4 from 0 Hz to f_T Hz, and even under different bias. Moreover, benefit from less matching networks, this cascode LNA is 2.3mm x 0.9mm in chip size and consumes 265mW DC power.

2. Characteristics of 100nm GaN HEMT and analysis of LNA

2.1. The characteristics of 100nm GaN-on-Si HEMT
To employ the property of transistor, the characteristics such as transconductance, NF_{min}, breakdown voltage and threshold voltage are simulated in Agilent’s Advanced Design System (ADS). The accurate HEMT model according to the measurements is provided by OMMIC’s design kit. Figure 2 shows the transconductance simulation results. It can be seen that the transconductance reaches the maximum when V_g and V_d are set to -0.7V and 3V respectively, which can provide the highest small signal gain but consume a large DC power of 255mW. Therefore, the gate bias of less than -1v is more commonly used. Figure 3 shows the NF_{min} at different width of HEMT under a constant I_d. It shows that the transistor width from 4 x 15μm to 4 x 35μm shows similar noise characteristics, and larger width will worsen NF_{min} and DC power. Other simulations present that the breakdown voltage and threshold voltage are 30V and -1.8V respectively.

![Figure 2. gm scan under different bias.](image)

![Figure 3. NF_{min} scan under different width.](image)

2.2. Analysis of LNA
The topology of single-stage LNA with inductive source degeneration is shown in Figure 4(a), and the structure of multi-stage LNA is shown in Figure 4(b).

![Figure 4. LNA topology: (a) Topology of single-stage LNA with inductive source degeneration; (b) Structure of multi-stage LNA.](image)
2.2.1. Gain calculation. According to Figure 4(a), assuming that the reverse transmission characteristics are ignored, the available power gain of single-stage LNA can be expressed as Equations (1) and (2):

\[ G_T = G_i G_s G_L \]  
\[ G_o = |S_{21}|^2 \]

The \( G_s \) and \( G_L \) is the power gain of input and output matching networks respectively, and \( G_o \) is the power gain of the transistor. Under the condition of input and output matching, the \( G_s \) and \( G_L \) are equal to 1, and the gain of LNA reaches the maximum. In millimeter wave band, the \( G_o \) will decrease rapidly as the increase of frequency due to the parasitic capacitance, the reason will be explained in next section. Therefore, keeping \( G_s \) and \( G_L \) equal to 1 in whole working band may deteriorate the 3dB bandwidth of broadband LNA. The solution is to reduce the \( G_s \) and \( G_L \) at low frequency to keep a flat in-band gain. Furthermore, the matching network can be designed as a high-pass filter, keeping \( G_s \) and \( G_L \) equal to 1 at high frequency and less than 1 at low frequency, as shown in Figure 5.

![Figure 5. The method of keeping a flat in-band gain.](image)

2.3. Effective transconductance calculation

According to Figure 4(a), the effective transconductance of transistor can be expressed as Equation (3):

\[ g_{m,\text{eff}} = \frac{g_m}{1 + g_m s L_s + s C_{gs} (s L_s + s L_g + R_s)} \]  

When the inductors \( L_s \) and \( L_g \) resonate with capacitor \( C_{gs} \), the transconductance can be further simplified as Equation (4):

\[ |g_{m,\text{eff}}| = \frac{g_m}{2\omega R_s C_{gs}} \]

In terms of Equation (4), the \( \omega \) of denominator, explains why the gain of transistor is strongly frequency-independent and has a negative slop across the band, especially when an inductor is added to the source.

2.3.1. Input matching. According to Figure 4(a), the input impedance of LNA with inductive degeneration can be expressed as Equation (5):

\[ Z_{in} = \omega L_s + s (L_g + L_s) + \frac{1}{s C_{gs}} \]

The first part is real which can be adjusted to 50ohm by \( L_g \). The last two part is generated by two inductors and capacitor \( C_{gs} \). When resonating, the last two part will equal to 0 and achieve input matching. From another perspective, the phase of the standing wave on the gate can be shifted 180° by \( L_g \), so as to cancel the standing wave at the input port and achieve input matching.
2.3.2. Noise calculation of multi-stage LNA. According to Figure 4(b), the NF of multi-stage LNA can be calculated by Equation (6) [19], where $NF_{1-4}$ is the noise figure and $G_{1-3}$ is the gain of each stage.

$$NF = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \frac{NF_4 - 1}{G_1 G_2 G_3} + \cdots$$

(6)

From the equation, it can be seen that the NF of multi-stage amplifier is mainly determined by the $NF_1$ and $G_1$. Therefore, the design of first-stage amplifier is the most significant because it mainly determines the NF of whole LNA.

2.3.3. LNA structure. To meet a gain of over 20dB, common source (CS) LNA and cascode LNA are both available options [20-23]. Benefit from simpler structure, CS LNA can achieve lower NF. Nevertheless, the existence of Miller capacitance may cause potential instability and degraded gain at high frequency. Therefore, CS LNA usually needs more methods to suppress the gain for absolute stability. Moreover, due to the lower gain provided by single-stage LNA, CS LNA requires more cascading to achieve high gain, therefore occupying larger chip size. For cascode structure, the Miller capacitance can be cancelled through setting the same $V_{ds}$ and transistor width. The extra thermal noise introduced by cascode transistor can also be reduced by an inductor added to the source of cascode transistor. In comparison, the cascode LNA provides better overall performances in terms of bandwidth, noise figure, gain, linearity, power consumption and area.

3. LNA design

In order to obtain accurate simulation results, the LNA is designed with hybrid electromagnetic and HEMT model simulation in ADS. The passive part of LNA is simulated with electromagnetic (EM) simulation tool. The HEMT model provided by OMMIC’s design kit consists of small signal S parameter and noise data based on measurements.

3.1. Transistor width and bias selection

A two-stage cascode structure is used to provide a gain of over 20dB in Figure 6. Each HEMT uses 4 x 35 μm width to offset the Miller capacitance. The gate of transistor $M_1$ is biased at -1.1V and the gate of cascode transistor is biased at 2V through several Kohm resistors ($R_{g1}$ and $R_{g2}$). The drain of cascode transistor is biased at 6V to provide the same $V_{ds}$ for $M_1$ and $M_2$. The final layout of cascode LNA is shown in Figure 7.

Figure 6. Schematic of Ka-band broadband cascode LNA.
3.2. Low noise design
As mentioned previously, the first-stage amplifier mainly determines NF of whole LNA. Therefore, the design of input matching network is critical. We simplify the input matching network as much as possible because complicated structure brings excessive parasitic resistance which may worsen NF [24]. According to Figure 6, the TLs is introduced to the source of transistor to meet noise matching and conjugate matching simultaneously. The value of TLs needs to be carefully selected. Longer TLs can meet noise matching and conjugate matching more easily, but will degrade the gain of the first-stage amplifier, so that the noise generated by subsequent-stage cannot be suppressed. In contrast, shorter TLs achieves a higher gain but that may deteriorate the stability. Moreover, a quarter-wavelength stab with two decoupling capacitors (Cd and C2) is used for RF choke in input and output matching networks to reduce loss and isolate power noise.

3.3. Gain flatness design
It is not difficult to design a multi-stage Ka-band LNA with a gain of over 20dB using 100nm GaN HEMT, but a flat in-band gain is hard to guarantee. Due to the parasitic capacitance of HEMT, the gain will drop rapidly as the frequency increases. Therefore, the high pass filter is used to suppress the low-frequency gain and maintain the flatness, which is composed by TLd and C3 (Figure 6). The shunt high pass filter can filter out the small signal current at low frequency, so that the gain can be suppressed. When the gain at low frequency is suppressed, the stability of whole LNA is also improved. It is worth noting that this filter is not suitable for setting at the input or output matching network, because the standing wave generated by high pass filter will enter the source or load of LNA and deteriorate the return loss. Due to the isolation of transistor, setting it to the inter-stage matching network can avoid this situation. The simulation results of inter-stage matching network and cascode unit are shown in Figure 8.

Figure 7. Final layout of Ka-band broadband cascode LNA.

Figure 8. Gain of inter-stage matching network and cascode unit.
Furthermore, because the TL$ _d$ and C$ _3$ in inter-stage networks have the feature of poor RF choke effect, a lumped inductor L$ _d$ and C$ _d$ is additionally added to decouple the power. The power decoupling of each stage is very important, because the parasitic inductor from the probe or bonding wire will affect the impedance of matching networks, which may bring potential instability.

3.4. Stability design
To avoid potential instability, the K factor is simulated from 0 Hz to f$ _T$ instead of only working band. With a f$ _T$ of over 100GHz, the transistor still has a high gain at 60GHz. The reflections introduced by impedance mismatching may cause instability. Therefore, the shunt small capacitor C$ _3$ (Figure 6) between M$ _1$ and M$ _2$ is to ground the reflection wave for high frequency stability. At lower frequency (0-10GHz), R$ _1$ in series with decoupling capacitor C$ _2$ is to prevent direct parallel resonance between C$ _2$ and L$ _d$, because the resonance will put a huge load impedance to the drain and causes unstable gain.

3.5. Cascode unit design
The cascode unit contains a short stub TL$ _2$, capacitors C$ _3$ and C$ _4$ (Figure 6). The stub TL$ _2$ can suppress the noise from M$ _2$ because the parasitic inductor introduced by TL$ _2$ will reduce the gain of M$ _2$, so that the thermal noise generated by M$ _2$ won’t be amplified and flow into output. In addition, the parasitic capacitances from the drain of M$ _1$ and the source of M$ _2$ is the most critical reason for deteriorating the gain at high frequency. Therefore, TL$ _2$ is to resonate them to prevent gain degradation at higher frequency(30-40GHz). The capacitor C$ _4$ is added to divide the small signal voltage with C$ _{gs}$ of M$ _2$ and reduce the transconductance, which can improve the stability of whole LNA.

4. Layout and post-layout simulation
Figure 7 shows the final layout of cascode LNA. The bent microstrip lines is to reduce the chip area, and the width of metal at output is selected to be 30$ \mu$m in order to meet a larger current to pass. The final layout occupies an area of 2.3mm $\times$ 0.9mm.

The S parameter simulation results of two-stage cascode LNA are shown in Figure 9 and Figure 10. The simulated S$ _{11}$ and S$ _{22}$ are both lower than -10dB and the gain is about 21-22.8dB from 22GHz to 38GHz. The NF is 0.9-1.3dB across the band. Due to the Miller capacitance is cancelled and the parasitic capacitances between M$ _1$ and M$ _2$ (Figure 6) are resonated, the overall performances are better than common source structure.

![Figure 9. Return Loss simulation results.](image1)

![Figure 10. Gain and NF simulation results.](image2)

Figure 11 presents the K factor simulation result of this LNA from 0 GHz to 100 GHz. The K factor is better than 4 across the band, which proves the absolute stability. Figure 12 shows the harmonic simulation result. The OP1dB of cascode LNA achieves 18-21dBm due to a large bias on the drain, and the DC consumption is 265mW.
5. Conclusions
Since the GaN based RF front-end has great potential in power density, linearity and noise figure, a GaN based LNA is presented in this paper. With novel methods for gain flatness and stability, this cascode LNA achieves a flat gain of 21-22.8dB and a competitive NF of 0.9-1.3dB from 22GHz to 38GHz. The K factor is better than 4 from 0 GHz to 100 GHz. In addition, the presented LNA occupies an area of 2.3mm x 0.9mm and consumes 265mW DC power. The OP1dB achieves 18-21dBm, which demonstrates the excellent anti-jamming ability compared with GaAs and InP technology [25-27]. Table 1 shows the comparison with published works.

Table 1. Performance comparison with published works.

| Paper | Process | Structure | Frequency (GHz) | Gain (dB) | Noise Figure (dB) | OP1dB (dBm) | Area (mm²) |
|-------|---------|-----------|----------------|-----------|-------------------|------------|-----------|
| [16]  | GaN/0.1 | CS        | 18-31(MEA)     | 22-25     | 1.4               | 16-17      | 2.3       |
| [17]  | GaN/0.1 | CS        | 23-31(MEA)     | 25-29     | 2.2-2.8           | \           | 2.3       |
| [23]  | GaN/0.1 | Cascode   | 18-20(SIM)     | 35        | 1.4               | \          | 4.8       |
| [25]  | GaAs/0.1| CS        | 19-31(MEA)     | 29        | 2.1               | \          | 2         |
| [26]  | GaAs/0.1| CS        | 18-43(MEA)     | 21.6      | 1.8-2.7           | 11.5       | 2         |
| [27]  | InP/0.1 | CS        | 26-40(MEA)     | 21-23     | 1.5               | \          | 1.7       |
| This work | GaN/0.1 | Cascode   | 22-28(SIM)     | 21-22.8   | 0.9-1.3           | 18-21      | 2         |

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