A Homogeneous Processing Fabric for Matrix-Vector Multiplication and Associative Search Using Ferroelectric Time-Domain Compute-in-Memory

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Abstract—In this work, we propose a ferroelectric FET (FeFET) time-domain compute-in-memory (TD-CiM) array as a homogeneous processing fabric for binary multiplication-accumulation (MAC) and content addressable memory (CAM). We demonstrate that: i) the XOR/XNOR/AND logic function can be realized using a single cell composed of 2FeFETs connected in series; ii) a two-phase computation in an inverter chain with each stage featuring the XOR/AND cell to control the associated capacitor loading and the computation results of binary MAC and CAM are reflected in the chain output signal delay, illustrating full digital compatibility; iii) comprehensive theoretical and experimental validation of the proposed 2FeFET cell and inverter delay chains and their robustness against FeFET variation; iv) the homogeneous processing fabric is applied in hyperdimensional computing to show dynamic and fine-grain resource allocation to accommodate different tasks requiring varying demands over the binary MAC and CAM resources.

Index Terms—Ferroelectric FET, time-domain compute-in-memory, content addressable memory

I. INTRODUCTION

For the hardware acceleration of neural networks to support wide deployment of intelligent devices, different approaches have been proposed and studied. The commercialized digital processors and near-memory computing processors are have gained tremendous performance boost over the years through technology scaling [1]. The main challenge, however, for these computing platforms is the power-hungry and slow memory access, as summarized in Fig.1(a). Analog approaches, such as CiM, are proposed to address this issue by directly performing the computations inside the memory array, thus eliminating the data transfer bottleneck [1]–[5]. As the examples, the crossbar array is used to perform the MAC operation [2] to accelerate matrix-vector multiplication, and CAM designs have been used for parallel and efficient associative search [6]–[10]. Though these designs are promising, they still suffer from typical digital incompatibility and costly peripherals to convert signals between digital and analog domains.

TD-CiM is emerging as an alternative computing paradigm to address the challenges associated with the pure digital and analog processors [11]. Its core is a digital delay chain, whose delay is controlled in an analog fashion using memory cells. The computation results are reflected in the signal propagation delay, sensing which only needs digital techniques. TD-CiM is compact, energy-efficient, and compatible with digital circuits and associates with simple peripheral sensing circuitry. Recently, by leveraging compact, energy-efficient, and CMOS compatible HfO₂ based FeFETs, TD-CiM array is proposed [12], which is an inverter chain composed of N stages each embedding a FeFET device in the pull-down path, as shown in Fig.1(b). Such a design achieves remarkable energy-efficiency, while also has many unaddressed issues. Since the FeFETs participate in the signal propagation path as a tunable resistance, the final output delay is highly sensitive...
to the FeFET variation. In addition, the large ON/OFF ratio of FeFET can not be fully exploited for the output delay modulation as a FeFET exhibiting an OFF state may prevent the signal propagation, resulting in a computation failure. Therefore, the conductance range of FeFET that can be used in the design is limited. Moreover, with the FeFETs inside the signal transmission path, it is challenging to write FeFETs, especially in the array settings where inhibition bias schemes need to be applied. To address these issues, we propose a novel FeFET based TD-CiM where FeFETs are outside the signal propagation path, but rather controls the associated capacitor loading, as shown in Fig.1(c), thus regaining full digital compatibility and ease to operate.

![Fig. 2. (a) A homogeneous PE array that can function as both binary CAM (in gray) and MAC (in orange). It can be dynamically allocated to either CAM or MAC to adjust to various task workloads. (b) The proposed FeFET based TD-CiM to realize both binary CAM and MAC.](image)

In our proposed design, the FeFETs are outside the signal propagation path, and the 2FeFET AND/XOR cell stores binary values by leveraging the non-volatile memory property of FeFET, therefore, the design is robust against device variation, and maintains the signal propagation integrity. In addition, with access to the FeFETs source/drain, it is possible to program the FeFETs with write inhibition schemes [14], [15]. In the following, the 2FeFET cell implementing both the AND and XOR(XNOR) logic operation is introduced and validated in section II. Then the FeFET TD-CiM array using the 2FeFET cell is built and validated in section III and section IV, respectively. In section V the proposed FeFET TD-CiM is applied for hyperdimensional computing. Section VI concludes the paper.

II. 2FeFET Cell for XOR & AND Operation

In this work, FeFETs integrated on industrial 28nm high-$\kappa$ metal gate platform as shown in Fig.3(a) are demonstrated and used. The device features a gate stack of polysilicon/TiN/doped HfO$_2$/SiO$_2$/p-Si, and detailed process information can be found in [16]. When subjected to $\pm 4$V, 1$\mu$s write pulse, the FeFET will be set to the low-$V_{TH}$ state or the high-$V_{TH}$ state, respectively, as shown in Fig.3(b). For the tested 50 devices with a size $W/L=0.5\mu$m/$0.5\mu$m, a large memory window between the two states can still be obtained, indicating reasonable device variation control of FeFET [17].

Fig.3(c) and (d) show the operation principles of the 2FeFET cell structure to implement the XOR(XNOR) logic which is the key function in a CAM cell for match and mismatch conditions, respectively. The 2FeFETs are connected in series, forming a push-pull structure. By writing complementary states, i.e., low-$V_{TH}$ state and high-$V_{TH}$ state, into FeFETs to encode the stored information and then applying the search information on the search line (SL and $V_{SL}$), a match or mismatch between the stored information and applied search input can be determined. For example, for a cell storing bit "1", as shown in Fig.3(c), the upper and lower FeFETs are written to the low-$V_{TH}$ state and high-$V_{TH}$ state, respectively. Then a bit “0” is searched by applying $V_{DD}$/GND to SL/$V_{SL}$. In this way, due to the resistor divider formed by the two FeFETs, the internal node voltage, $V_{int}$, is given as

$$V_{int} = \frac{R_{HVT}}{R_{HVT} + R_{LVT}} V_{SL}$$

where the $R_{HVT}/R_{LVT}$ is the equivalent FeFET channel resistance for the high/low-$V_{TH}$ state. The internal node will be charged to a high voltage through the upper FeFET with low-$V_{TH}$, indicating a mismatch. On the other hand, flipping the search information to bit “1” corresponds to applying GND/$V_{DD}$ to SL/$V_{SL}$, as shown in Fig.3(d). In this case, the $V_{int}$ is given by

$$V_{int} = \frac{R_{LVT}}{R_{HVT} + R_{LVT}} V_{SL}$$
The internal node will be discharged to ground through the upper FeFET with low-$V_{TH}$, indicating a match. Similar analysis can be performed when the stored information changes to bit “0”, where the upper and lower FeFETs are written into the high-$V_{TH}$ state and low-$V_{TH}$ state, respectively. Based on this 2FeFET cell, XOR(XNOR) logic can be realized. To verify the cell operation, 2FeFET cell is constructed experimentally and characterized. Fig.3(e) and (f) show the $V_{int}$ as a function of applied read gate voltage, $V_{READ}$, during search when the cell stores bit “0” and “1”, respectively. When the cell stores bit “0” and a search input “1” is applied, as shown in Fig.3(e), the $V_{int}$ grows initially with the $V_{READ}$ and starts to decrease with continual increase of $V_{READ}$. This is because that to read out the the value stored in the FeFET, an appropriate $V_{READ}$ between the low-$V_{TH}$ and high-$V_{TH}$ is needed. When $V_{READ}$ is high enough such that even the FeFET storing the high-$V_{TH}$ state is turned ON, the $V_{int}$ starts to decrease with the $V_{READ}$. With an appropriate $V_{READ}$, e.g., $1V$, the $V_{int}$ for the match and mismatch scenarios are widely separated, even during the device variations among 17 measured cells. The robustness of the 2FeFET cell against device variation is another advantage, which will be further studied in section IV.

Using the same 2FeFET cell, the AND logic function can also be realized. In this case, the encoding of the stored information, which is one of the operands, remains the same as the XOR(XNOR) case by storing complementary $V_{TH}$ states into the two FeFETs. The other operand, i.e., the input voltages on the SL/$\overline{SL}$, however, are different from the XOR(XNOR) case. The input voltage is only applied on the SL while the $\overline{SL}$ is fixed at GND. Fig.3(g) shows all four scenarios corresponding to different combinations of the two operands. When bit “0” is stored, the lower FeFET is with the low-$V_{TH}$ state, and will discharge the internal node voltage upon the operation, irrespective of the input SL voltage. When the cell stores bit “1”, an input “0” causes the internal node voltage to discharge through the upper FeFET with the low-$V_{TH}$ state. The only scenario that will yield a high $V_{int}$ is when the cell stores “1” and input “1” is applied such that the $V_{int}$ is charged up through the upper FeFET with the low-$V_{TH}$ state. In this way, the AND logic is realized. The cell operations for the AND logic are also experimentally verified. Fig.3(h) and (i) show the transient waveform of $V_{int}$ for cell storing “1” and “0”, respectively. The results show that the $V_{int}$ is only high when the AND logic output is true and low otherwise, validating the AND logic operation. Note that the delay shown in the waveform is limited by the discrete measurement setup that is adopted and fully integrated cell is expected to operate much faster, which will be studied using SPICE simulation in section III.

III. PRINCIPLES OF FEFET TIME-DOMAIN CiM

By embedding the 2FeFET cell in section II into the array shown in Fig.1(c), the proposed FeFET based TD-CiM is realized. To understand the operation principles of the proposed FeFET TD-CiM, the buffer delay chains are first evaluated, as shown in Fig.4(a), which features the symmetric rising edge and falling edge delay. An input pulse is sent to the first stage and the corresponding output pulse thus has a delay, $T_{delay}$, with respect to the input pulse. In addition to the intrinsic delay of each buffer, $T_{intrinsic}$, $T_{delay}$ also contains the delay caused by the conditionally loaded capacitors for each stage. The capacitor loading occurs when the AND/XOR(XNOR) logic of the corresponding stage outputs a high $V_{int}$, which turns on the access transistor and activates the load capacitor. In this sense, $T_{delay}$ can be expressed as:

$$T_{delay} = N_{tot}T_{intrinsic} + N_{active}T_{C}$$

where the $N_{tot}$ and $N_{active}$ are the number of total stages and the active stages where the AND/XOR logic outputs “1”, respectively. $T_{C}$ is the additional delay incurred by the capacitor loading. Sensing the $T_{delay}$ allows to detect $N_{active}$, which reflects the outputs of the XOR(XNOR) and AND logic with in the stages, thus realizing the binary MAC and CAM operations, respectively.
To verify the working principles, a compact multi-domain FeFET model [18] and a 40nm MOSFET Predictive Technology Model (PTM) [19] with minimized transistor sizes have been adopted in the SPICE simulation. The load capacitor of each stage is set to 9ff unless explicitly mentioned. Fig 4(b) shows the transient waveform of a single buffer stage. When the $V_{int}=0V$, the associated load capacitor is deactivated and the delay between the output and input pulses is $T_{intrinsic}$. When the load capacitor is activated, the additional delay, $T_C$, caused by the load capacitor contributes to the total delay.

Fig.4(c) shows the $T_{delay}$ of 16 and 32 buffer stages with varying number of activated stages to evaluate the capability of a buffer chain in realizing the binary MAC/CAM operation. A linear dependence of $T_{delay}$ on the $N_{active}$ is validated, which is consistent with Eq. (3). Therefore, sensing the $T_{delay}$ allows to back calculate the $N_{active}$, thus realizing the binary MAC/CAM operation.

Building on the buffer delay chains, a denser solution using inverter chains is proposed, as shown in Fig 5. Without degrading the signal shapes during the signal propagation, a two-phase operation is proposed. In the phase I, as shown in Fig 5(a), all the odd stages AND/XOR cell output zero, thus disabling the odd stages capacitors. Then only the load capacitors of even stage participate in the computation, making the chain effectively a buffer chain. The rising edge delay of the output pulse compared with the input pulse is given by

$$T_{delay,r} = N_{tot} T_{intrinsic} + N_{active, even} T_C$$

where $N_{active, even}$ is the number of activated even stages. Similarly for the phase II, as shown in Fig 5(b), all the even stages are disabled and the total delay includes the delay contributed by the activated odd stages. To save energy, it is possible to apply a single input pulse propagation to perform the computation, where the rising and fall edges are sensed for computation in phase I and II, respectively. This requires the input pulse width to be larger than the phase I delay such that the signal propagation of phase I completes before the activated stages switch from even to odd, otherwise the phase I delay in Eq. (4) is not valid. In this way, the output falling edge delay with respect to the input pulse is given by

$$T_{delay,f} = N_{tot} T_{intrinsic} + N_{active, odd} T_C$$

where $N_{active, odd}$ is the number of activated odd stages. Then the total delay $T_{delay}$, i.e., the results for MAC/CAM function is obtained by adding the two phase delay results together.

$$T_{delay} = T_{delay,r} + T_{delay,f}$$

Fig. 5(c) shows the simulated rising and falling edge waveforms for phase I and II operations in an inverter chain with 32 stages. The evaluated delays for even and odd stages are shown in Fig. 5(d).
in Fig. 6(d). The linear delay increase with the number of activated stages and the total delay shows a similar dependence as the buffer chain shown in Fig. 6(c).

![Fig. 6: Experimental verification of the inverter chain based TD-CiM. (a) Experimental setup (e.g., 2x16 array). (b)/(c) Output transient waveforms for odd/even stages computation in a 32 stages inverter chain. (d) A linear dependence of the delay on the number of activated stages is observed, validating the TD-CiM operation. (e) Dependence of the delay time on the load capacitor size. The linear relationship is maintained for different capacitor sizes.](image)

### IV. Verification of FeFET TD-CiM

Fig. 6(a) shows the setup of a 2x16 inverter arrays using discrete inverters and load capacitors to experimentally validate the proposed FeFET TD-CiM. Fig. 6(b) and (c) show the transient waveforms of the falling and rising edges in an inverter chain with 32 stages. The falling edge is sensed to perform the computation associated with the odd stages while the rising edge is sensed to perform the computation associated with the even stages. Similar to the simulation results shown in Fig. 5(c), the delay of the falling or the rising edge increases with the number of activated odd or even stages. Evaluated delay results shown in Fig. 6(d) suggest the linear dependence of the total delay on the number of activated stages. In addition, different load capacitor sizes have been tested for an inverter chain with 8 stages, as shown in Fig. 5(c). The linear dependence of the total delay on the number of activated stages also holds for different load capacitor values. Note that these experimental results are intended for functionality verification. The speed and the load capacitors, due to the discrete measurement setup, are limited. It is expected that for fully integrated implementations, a much smaller capacitor can be used to improve the energy-efficiency and speed.

As mentioned in section III, the FeFET cell structure exhibits superior resilience against FeFET variations. This is because that as long as the resistance ratio between the high-$V_{\text{TH}}$ state and low-$V_{\text{TH}}$ state is large enough (e.g., >10), the internal node voltage, $V_{\text{int}}$, will reach closely to $V_{\text{DD}}$ or GND depending on the logic output. Here we further study the impact of the FeFET $V_{\text{TH}}$ variation on the delay chain operation through Monte Carlo simulations. We first verify the robustness of the 2FeFET cell by measuring the internal node voltage $V_{\text{int}}$ by 60 Monte Carlo runs assuming a $V_{\text{TH}}$ variation $\sigma V_{\text{TH}}$. Fig. 7(a) and (b) shows the $V_{\text{int}}$ as a function of the read gate voltage, $V_{\text{READ}}$, for the FeFETs with $\sigma V_{\text{TH}}$=0.12V and $\sigma V_{\text{TH}}$=0.2V, respectively, which is similar to the experimental results shown in Fig. 5(c) and (f). As shown, larger $\sigma V_{\text{TH}}$ enlarges the distribution of $V_{\text{int}}$. Fig. 7(c) summarizes the $V_{\text{int}}$ distributions upon $V_{\text{READ}}$ under different $\sigma V_{\text{TH}}$ values. Note that a fabricated FeFET with a size of W/L=500nm/500nm is experimentally measured to exhibit around 50 mV $\sigma V_{\text{TH}}$, which is far less than the assumed $\sigma V_{\text{TH}}$. Therefore, the 2FeFET cell output has superior robustness against the device variation. The impact of cell level variation on the accuracy of inverter chain operation is studied in Fig. 7(d), where 32, 64, and 128 stages are considered. When the FeFET $\sigma V_{\text{TH}}$ or the number of stages increases, the distribution of the inverter delay time becomes wider. Considering a sense margin of 100ps, the proposed FeFET TD-CiM is highly robust to the FeFET variation.

The energy and latency metrics of the proposed FeFET TD-CiM with respect to different load capacitor values varying from 10fF to 1280fF and different number of stages varying from 1 to 64 are illustrated in Fig. 7(e) and (f). The contour lines corresponding to a fixed energy consumption or latency are in the diagonal direction, indicating that the energy and delay are both proportional to the product of the load capacitor value and the number of activated stages (i.e., the total capacitance participating in the computation). Therefore a small load capacitor is preferred. However, the sensing circuitry, such as a counter, which is required to distinguish the small delay contributed by the small load capacitor, $T_C$, limits the lower bound of the load capacitor value. Moreover, the impact of the supply voltage, $V_{\text{DD}}$, on the array energy and delay metrics is investigated and shown in Fig. 7(g) and (h), respectively. It can be seen that the proposed array energy decreases and delay increases as the supply voltage scales down.

### V. Application of FeFET TD-CiM for Hyperdimensional Computing

As illustrated in Fig. 2, our proposed FeFET TD-CiM processing fabric can perform both binary MAC and CAM operations, thus allowing to adapt to different information processing tasks demanding different workloads of MAC and CAM. As a case study, we benchmark our design in the hyperdimensional computing (HDC) paradigm, as shown in Fig. 8. HDC emerges as an alternative paradigm that mimics the
critical brain dynamics for high-efficiency and noise-tolerant computation [21]. It is motivated by the observation that the human brain operates on high-dimensional data representations, and is robust against noise. As shown in Fig. 8(a), the HDC inference is composed of encoding module and similarity search module. This encoding method, inspired by the Radial Basis Function (RBF) kernel trick [22], considers the non-linear relation between the features during the encoding, and maps the input feature data points into high-dimensional space. Considering an encoding function that maps a feature vector \( F = \{V_1, V_2, \ldots, V_N\} \), with \( N \) features to a hypervector \( \vec{H} = \{H_1, H_2, \ldots, H_D\} \) with \( D \) dimensions (\( H_i \in \{0, 1\} \)). Each dimension of the encoded data is generated by calculating the matrix-vector multiplication of a feature vector with a base matrix \( \{\vec{B}_1, \vec{B}_2, \ldots, \vec{B}_N\} \), i.e., \( \vec{H} = \sum_{i \in N} V_i \times \vec{B}_i \), where \( \vec{B}_i \) is a randomly generated vector from a set \( \{0, 1\} \) with the same dimensionality of the feature vector \( \vec{H} \). The random vectors \( \{\vec{B}_1, \vec{B}_2, \ldots, \vec{B}_N\} \) can be generated once offline and then used for the rest of the inference task (\( \vec{B}_i \in \{0, 1\}^N \)), and the matrix-vector multiplication can be implemented by the MAC operation of the proposed TD-CiM array as shown in Fig 8(a). After the encoding, HDC superimposes together the encoded hypervectors corresponding to the same class of feature vectors to create a composite representation of a phenomenon of interest known as a “model hypervector”, which is then classified as an entry of the learned model.

During the inference, the HDC firstly encodes the input feature query to produce a query hypervector \( \vec{H} \) by performing the MAC operation. Parallel similarity search is then performed over the model hypervectors through an associative search operation. Such associative search, i.e., the accumulation XNOR function between the query hypervector and the stored class/model hypervectors, can be implemented by the CAM operation of the proposed TD-CiM array storing the learned model as shown in Fig 8(a). The similarity (\( \delta \)) between the query \( \vec{H} \) and all class/model hypervectors is computed to find out the class with the highest similarity to the query hypervector. In binary representation, Hamming distance is measured as the similarity metric, \( W \).

Using the same FeFET TD-CiM, the same chip can conduct dynamic fine-grain resource allocation of binary MAC and CAM for different tasks. We have designed and used a cycle-
accurate simulator based on PyTorch [26] which emulates the TD-CiM functionality during the HDC inference. Our tool receives the energy consumption and execution time of HDC key operations (i.e., binary MAC and CAM) using the proposed FeFET TD-CiM and then expands those values to compute the application-level energy consumption and time when searching each query. As shown in Fig.8(b), the breakdown of time and energy consumption when performing the speech, activity recognition and face detection demonstrates the varying demand of binary MAC and CAM. Fig.8(c) compares the energy consumption and execution time of the proposed TD-CiM for different applications compared to the GPU platform (GeForce RTX 3060 Ti GPU). It shows that our FeFET TD-CiM array in 32-stage configuration provides, on average 106× energy reduction and 63× speedup than GPU. Table I compares our proposed solution with other CiM solutions [11], [12], [23]–[25]. Due to the unique 2FeFET cell which can implement both the AND and XOR(XNOR) logic, our proposed FeFET TD-CiM allows fine-grain and highly flexible reconfigurability between the binary MAC and CAM functionalities using the same array. With the energy-efficiency of 8563 TOPS/W, the proposed FeFET based TD-CiM is a highly promising candidate processing fabric for various in-memory computing applications.

VI. CONCLUSION

In this work, we proposed a homogeneous processing fabric using FeFET based TD-CiM array that can support both the binary MAC and CAM. We have demonstrated the AND/XOR(XNOR) logic functionality of a 2FeFET cell and integrated such cells in a delay chain, which supports TD-CiM realization of binary MAC and CAM through a two-phase operation. Both theoretical and experimental validations are conducted and the robustness of the system against FeFET variation is demonstrated. We benchmark this FeFET TD-CiM processing fabric in the context of HDC, and show that our system can adapt to different tasks with varying demands over the binary MAC and CAM through dynamic resource allocation. Our proposed FeFET TD-CiM provides a promising CiM design with its versatility and high performance.

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