Status of a DEPFET pixel system for the ILC vertex detector

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We have developed a prototype system for the ILC vertex detector based on DEPFET pixels. The system operates a 128 × 64 matrix (with ~ 35 × 25 µm² large pixels) and uses two dedicated microchips, the SWITCHER II chip for matrix steering and the CURO II chip for readout. The system development has been driven by the final ILC requirements which above all demand a detector thinned to 50 µm and a row wise read out with line rates of 20 MHz and more. The targeted noise performance for the DEPFET technology is in the range of ENC=100 e⁻. The functionality of the system has been demonstrated using different radioactive sources in an energy range from 6 to 40 keV. In recent test beam experiments using 6 GeV electrons, a signal-to-noise ratio of S/N ~ 120 has been achieved with present sensors being 450 µm thick. For improved DEPFET systems using 50 µm thick sensors in future, a signal-to-noise of 40 is expected.

1. Introduction

The future International Linear Collider (ILC) will enter a new era of vertex detection. With the aimed impact parameter resolution of \( \sigma (d_0) = (3.9 \pm 7.8 / \sin \theta) \) µm precision physics will become possible which complements the discovery potential of the LHC machine. To achieve such outstanding performance, the ILC vertex detector requires a row wise operation where all sensor periphery is placed outside the sensitive area and detector layers that are thinned to 50 µm or even below. Furthermore, the emerging background rates due to the high luminosity beam necessitate the readout of the whole detector in 50 µs which translates into line rates of 20 MHz and more.

2. DEPFET technology for the ILC

One technological option presently discussed for the ILC vertex detector is the DEPFET concept. The basic principle of operation of the DEPFET is illustrated in figure 1. The DEPFET (abbreviated DEPleled Fie& Effect Transistor) combines in-pixel amplification and particle detection by embedding a FET in high-ohmic silicon material. The sensor is fully depleted due to sideways depletion from the backside contact and from the transistor channel jointly. The sideways depletion and additional implantations close to the detector front side form a laterally confined potential valley underneath the transistor channel. This potential valley is called internal gate, derived from the external gate of the transistor. Electrons generated by impinging radiation drift to the internal gate where they are collected. The potential of the internal gate changes due to the collected charge \( \Delta q \) and the transistor current is modulated according to \( \Delta I_D = g_m \cdot \Delta q \), where \( g_m \) is called the internal gain of the DEPFET transistor, equivalent to the transconductance of the external gate \( g_m \). Finally, the signal charge collected in the internal gate can be determined by measuring the device current. Since the readout of the device current does not affect the charge in the internal gate, it has to be removed from time to time. This is know as the clear of the device and is realized by an additional contact at the pixel fringe (not shown in figure 1). The main advantages of the DEPFET technology are the fully depleted bulk that is used for signal generation and the fact that charge collection is induced by an electric field.

Since the DEPFET concept relies on a backside contact to provide the fully depletion, new thinning concepts apart from the standard ones used in microchip industry need to be explored to fabricate thin DEPFETs. The present approach for thinning DEPFET modules is based on wafer bonding technology and anisotropic etching. The principle has been demonstrated by producing thin diode structures and will be combined with a large scale DEPFET pixel.

Figure 1: Cross section of a DEPFET pixel illustrating the basic principle of operation.

\[ \sigma (d_0) = (3.9 \pm 7.8 / \sin \theta) \text{ µm} \]
production in future. The radiation tolerance of the sensor against ionizing radiation has been shown up to a dose of 1 MRad using X-rays from a $^{60}$Co source.

A principle sketch of one ladder end proposed for a DEPFET ILC vertex detector is shown in figure 2. The sensitive area is thinned to 50 $\mu$m keeping a thicker frame ($\sim$ 300 $\mu$m) for mechanical stability and stiffening of the 100 mm long and 13 mm wide ladder. The steering chips for row selection and clearing strobes are situated at the longer side so that the detector is read out row wise to the ladder ends. There, readout chips are placed that process all matrix columns in parallel.

Concerning the readout of such a DEPFET ladder, new concepts have been explored as well [4]. Since the device signal of the DEPFET is a current, the most natural way is to adapt the signal processing queue to the current operation of the device. Therefore, current memory cells are used in the readout chip for temporal storage and processing of the signal current. The basic principle of operation of such a memory cell [5] is shown in figure 3. The cell operates as a dynamic current mirror, where transistor M1 works as the input and output stage depending on the setting of the different switches S1-S3. Apart from the fact that a direct signal processing without any current to voltage conversion is smart, additional advantages of operating in the current domain exist, upon the most important ones are:

- The voltage sampled at the gate of the transistor M1 in figure 3 is not directly proportional to the signal current. Hence, a higher dynamic range compared to a voltage sample and hold can be achieved. This is particularly important for emerging process technologies with reduced supply voltage.
- The subtraction of two values, as needed for pedestal subtraction, can be done very accurate and easily with currents.

3. The DEPFET pixel system

As an intermediate step towards a full scale ILC detector ladder, a prototype system using a $128 \times 64$ DEPFET pixel matrix has been developed. A schematic overview of the system is given in figure 4. It consists of three major parts: a USB-Board, a DAQ-Board and a Hybrid-Board. The USB-Board is based on USB 2.0 standard and provides the communication between the system and a PC. The Hybrid-Board hosts the DEPFET pixel matrix, the steering chips SWITCHER II, the readout chip CURO II and a pair of transimpedance amplifiers (I2U) that convert the current outputs of the CURO chip to voltage signals. The DAQ-Board carries two 14 bit ADCs for digitization and a SRAM for data storage. Integral part of the DAQ-Board is a SPARTAN 3 FPGA which provides the configuration of all chips in the system and manages the synchronization between the components during data acquisition. An external Protection-Board can be inserted to safeguard the power supply voltages. A photograph of the DEPFET system is shown in figure 5.

Figure 3 shows a close-up view of the chip assembly on the Hybrid-Board. The $128 \times 64$ pixel
DEPFET matrix is situated in the center. The steering strobes for the matrix are provided by two SWITCHER II chips located at both matrix sides. The SWITCHER II has been fabricated in an AMS high voltage process to provide a voltage range of up to 25 V, needed to operate some matrix designs. The present hybrid uses two steering chips to be very versatile in operating different matrix types. Recent measurements show that for some matrix designs only one steering chip is sufficient to take care of matrix steering and clearing.

At the bottom of the matrix the 128 channel readout chip CURO II is placed. This chip is fabricated in a 0.25 μm TSMC process. In addition, most of the design already uses radiation tolerant layout rules. It is therefore very likely that the readout chip sustains the radiation dose of 200 kRad expected after 5 years operation of the ILC. Whether the present chip already shows a suitable radiation tolerance or if the layout has to be improved further on will be studied in irradiation test.

One of the main features of the readout chip are on-chip pedestal subtraction and zero suppression. The zero suppression is performed by a scanner which scans the binary hit pattern in parallel. Standalone tests with the present CURO II chip show that the scanner finds up to two hits in a 128 channel hit pattern with rates of more than 100 MHz. This is much faster than needed to cope with the expected rates at the ILC.

4. Lab Measurements

The system has been used in the lab for X-ray detection in an energy range from 5.9 up to 44.23 keV. The capability of spatial detection of X-rays has been demonstrated using a 75 μm thick tungsten test chart with an engraved logo and several line structures having a pitch of 100, 75, 50 and 25 μm (from left to right, respectively). The radiogram of the ~2 x 3 mm$^2$ large test chart is shown in figure. The test chart has been placed on the backside of the detector and the system has been irradiated with a $^{55}$Fe source. The radiogram has been obtained by summing the pulse heights for pixels that contain a signal higher than five times their noise. Although no spatial reconstruction techniques have been applied to improve the spatial resolution, the 50 μm lines in the radiogram are clearly visible.
To determine the internal gain of the DEPFET device and to measure the linearity of the system, energy spectra have been taken for Rubidium (Rb), Molybdenum (Mo), Silver (Ag), Cadmium (Cd), Barium (Ba) and Terbium (Tb), provided by a variable X-ray source [11]. After performing a row-wise common mode correction\(^1\), clusters are reconstructed by identifying neighboring pixels, where every pixel contains a signal higher than five times its noise. In figure 8 the mean cluster signal as a function of the characteristic X-ray energy is shown. From the slope of the system response an internal gain of the DEPFET sensor of \( g_q = 282.6 \pm 3.3 \text{ pA/e}^- \) is extracted. The integral-non-linearity (INL) of the system is better than 0.8% for a dynamic range of 8500 e\(^-\). This range is large enough for the detection of about 2 MIPs in a 50 \( \mu \text{m} \) thin sensor device.

\(^1\)Subtraction of a mean value (common mode) from the pixel pedestal. The common mode is computed using the pedestals of each pixel of a row that contain no signal.

5. Beam Tests

The system has been tested for MIP detection in the 6 GeV electron test beam at the DESY synchrotron. The analysis of the data is done in the following way: After pedestal and common mode corrections, clusters are searched for. Seeds are identified with a threshold cut of 5 \( \sigma \). The seeds are combined with neighboring pixels if their signal is two times higher than the noise. The signal distribution for clusters containing a maximum of 3 \( \times \) 3 pixels is shown in figure 9. The observed most probable value of about 36000 e\(^-\) (1796 \pm 3 ADU) obtained by a landau fit complies with the expected MIP signal in a 450 \( \mu \text{m} \) silicon sensor material. The system noise extracted from the noise peak of the raw data spectrum is found to be 15.723 \pm 0.007 ADU. This combines to a signal-to-noise ratio of 114.2 \pm 0.2. The observed noise figure in the test beam (\( \sim 300 \text{ e}^- \)) is higher than the one achieved in the lab. It turned out that the connection node between readout chip and transimpedance amplifier is very sensitive for

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\begin{align*}
\text{Figure 7: Radiogram of a } 2 \times 3 \text{ mm}^2 \text{ tungsten test chart taken with } ^{55}\text{Fe}. \\
\text{Figure 8: Gain measurement of the DEPFET pixel system. The sensor response is plotted for different radioactive sources.} \\
\text{Figure 9: Signal distribution for clusters with up to } 3 \times 3 \text{ pixels.}
\end{align*}
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pick-up. Hence, the system noise depends on different operating parameters. A future version of the readout chip implementing either a transimpedance amplifier or a current mode ADC is expected to overcome this.

Figure 10 shows the cluster size distribution. The most probable cluster contains about 5 pixels only. The relatively small clusters are due to the fact that charge collection in the DEPFET is done by an electric field and not by thermal diffusion. Also shown in figure 10 is the cluster size distribution for inverse signals. This event distribution is obtained by inverting the signals and repeating the analysis. It is very likely that the inverted signals are due to out-of-time events.

Figure 11 shows the efficiency to find a track as a function of the seed cut. The purity defined as the ratio of found good clusters and all clusters is shown in figure 12 as a function of the seed cut. The main result of the efficiency and purity study is that an operation at almost 100 % purity and efficiency is achieved by choosing a seed cut of $5 - 7 \sigma$. Note, that this threshold corresponds to only $\sim 5\%$ of a MIP signal.

### 6. Conclusion and Outlook

A prototype system for the ILC vertex detector based on DEPFET pixels has been developed. The system has been successfully used for X-ray and MIP detection. The current benchmarks of the system are:

- Noise performance of about ENC=220e$^-$. 

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2Events that occur between the clear of the sensor and the pedestal measurement.
line rate of 2 MHz,

• $S/N \sim 120$ for MIPs using a 450 $\mu$m sensor.

Concerning position resolution, the present test beam data yields an upper limit of 5 $\mu$m dominated by multiple scattering effects. A more precise measurement will be performed in the high energy test beam at CERN in summer 2006.

To achieve the final ILC specifications the system still needs improvements. Most importantly, the line rate needs to be increased by a factor of 10. The single components of the systems have already been tested up to a line rate of more than 20 MHz, whereas their synchronization in the system needs further optimization. Moreover, the noise performance has to be improved by a factor of two. Based on calculations and the experience with the present system, we are very confident that this will be achieved with the next version of DEPFET sensors and readout chip.

As a next step, new generations of all system components are designed and fabricated. Large DEPFET matrices with up to $512 \times 512$ pixels are in production. The pixel size is reduced to $25 \times 25 \, \mu m^2$ and the internal gain of the sensor is optimized.

A new steering chip using a standard, low voltage process is designed. Some DEPFET designs having a so called cleargate structure can be cleared at much lower voltages than offered by the present steering chip. Hence, the use of a submicron process is possible here as well. This promises a much better radiation tolerance compared to the present chip using a high voltage technology.

A new generation of the readout chip is designed as well. Operating the system with a duty cycle as close as possible to the bunch timing of the accelerator (1:199) will reduce the total power consumption significantly. Hence, one of the most important conceptual extension of the readout chip will be a power down feature.

On a longer time scale, a major step is to combine the thinning technology with a DEPFET production in order to fabricate thin DEPFET sensors. Together with the aimed noise figure of ENC=100 e$^-$, a signal-to-noise ratio of 40 is expected for these thin devices.

References

[1] J. Kemmer, G. Lutz (1987): “New semiconductor concepts”, NIM A253, pp.356ff.
[2] L. Andricek et al. (2004): “Processing of ultra thin silicon sensors for future linear collider experiments”, IEEE TNS, vol.51 No.3, pp.1117-1120
[3] L. Andricek et al. (2006): “The MOS-type DEPFET Pixel Sensor for the ILC environment”, NIM A565, pp.165-171
[4] M. Trimpl et al. (2003): “A Fast Readout using Switched Current Techniques for a DEPFET-Pixel Vertex Detector at TESLA”, NIM A511, pp.257-264
[5] J.B. Hughes, N.C. Bird, I.C. Macbeth (1989): “Switched Currents - A New Technique for Analog Sampled-Data Signal Processing”, IEEE ISCAS (217), pp.1584-1587
[6] I. Peric (2004): “Design and Realization of Integrated Circuits for the Readout of Pixel Sensors in High-Energy Physics and Biomedical Imaging”, PhD thesis BONN-IR-2004-13, Bonn University
[7] C. Sandow et al.: “Clear-performance of linear DEPFET devices”, proceedings of the SDS 2005 conference to be published in NIMA
[8] M. Trimpl (2005): “Design of a current based readout chip and development of a DEPFET pixel prototype system for the ILC vertex detector”, PhD thesis BONN-IR-2005-08, Bonn University, http://hss.ub.uni-bonn.de/diss_online
[9] W. Snoeys et al. (2000): “Layout techniques to enhance the radiation tolerance of standard CMOS technologies demonstrated on a pixel detector readout chip”, NIM A439, pp.349-360
[10] M. Trimpl et al.: “Performance of a DEPFET pixel system for particle detection”, proceedings of the SDS 2005 conference to be published in NIMA
[11] Amersham, AMC 2084

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