E3NE: An End-to-End Framework for Accelerating Spiking Neural Networks with Emerging Neural Encoding on FPGAs

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Abstract—Compiler frameworks are crucial for the widespread use of FPGA-based deep learning accelerators. They allow researchers and developers, who are not familiar with hardware engineering, to harness the performance attained by domain-specific logic. There exists a variety of frameworks for conventional artificial neural networks. However, not much research effort has been put into the creation of frameworks optimized for spiking neural networks (SNNs). This new generation of neural networks becomes increasingly interesting for the deployment of AI on edge devices, which have tight power and resource constraints. Our end-to-end framework E3NE automates the generation of efficient SNN inference logic for FPGAs. Based on a PyTorch model and user parameters, it applies various optimizations and assesses trade-offs inherent to spike-based accelerators. Multiple levels of parallelism and the use of an emerging neural encoding scheme result in an efficiency superior to previous SNN hardware implementations. For a similar model, E3NE uses less than 50% of hardware resources and 20% less power, while reducing the latency by an order of magnitude. Furthermore, scalability and generality allowed the deployment of the large-scale SNN models AlexNet and VGG.

Index Terms—Spiking Neural Network, Neuromorphic Computing, Neural Encoding, Compiler Framework, FPGA

1 INTRODUCTION

With the growing interest in deploying machine learning models on embedded devices, the need for power-efficient algorithms with constrained computing resources arose. Spiking neural networks (SNNs) became a promising machine learning technique in edge-AI due to their high efficiency advantages over conventional artificial neural networks (ANNs). A human brain is estimated to consume a mere 20 Watts of power [1], making it orders of magnitude more efficient than modern machine learning hardware. Tapping onto the optimizations carried out by evolution, SNNs mimic biological processes which were discovered in experiments on nervous systems of mammals [2], [3]. It was observed that neurons generate electrical action potentials or spikes with a duration of around one millisecond each [4]. A certain sequence of spikes, a spike train, is used to transfer information between neurons [5].

To use the complex results of experimental observations for computational applications, models like the Hodgkin-Huxley model [6], the Izhikevich model [7] or the leaky integrate-and-fire model [8] described the neuron behavior mathematically. Furthermore, neural encoding schemes such as rate encoding [9] or temporal encoding [10] are used to convert real numbers into binary spike trains. Due to their characteristics with conventional ANNs, SNNs were coined the third generation of neural networks [11].

The characteristics of SNNs enable low-power applications. The binary encoding of information in the form of spike trains obviates the need for expensive multipliers in the data path. To fully exploit the advantages of SNNs, its deployment on dedicated hardware systems is necessary. Application-specific integrated circuits (ASICs) like TrueNorth [12] and SpiNNaker [13] are examples of adder-based neuromorphic devices which employ non-von Neumann architectures. Intel’s neuromorphic chips Loihi [14] and Loihi 2 [15] combine multiple general microprocessor cores with 128 neuron cores. Those core communicate among each other via spikes through a Network-on-Chip. User-programmable processes allow the implementation of both inference and online training. In addition, architectures for Field-Programmable Gate Arrays (FPGAs) have been proposed for accurate emulation of spiking neuron characteristics [16], [17]. FPGAs are known for their malleability, which can be beneficial in this emerging research field, where new discoveries are made frequently. FPGAs can also easily be adapted to a wide range of applications, depending the requirements regarding performance, power consumption, cost, etc. However, the development for FPGAs requires special knowledge on hardware architecture and device properties. While high-level synthesis is able to derive a hardware structure from software code, it still requires directives and might not support all the features one expects from a software compiler. Moreover, it also comes at the expense of performance drop since the automatically generated hardware might not be fully optimized for the application. Therefore, it is challenging to make efficient FPGA-based SNN accelerators accessible to scientists and developers in the fields of neuroscience and artificial intelligence.

In the early days of spiking neural networks, the fundamental principles where tested on very simple problems, such as binary classification [18], [19]. As SNN algorithms...
matured, larger models like VGG were used to tackle complex datasets such as CIFAR-10 or ImageNet [21]. Hardware accelerators, however, seem to lag behind software simulations, as past results were mostly reported on toy datasets such as MNIST. A potential reason for this scalability hurdle is the spike train length, which can reach into the thousands if the network model is large. On the one hand, that is necessary to avoid information loss and attain a high classification accuracy. On the other hand, it increases the runtime of the network and hence offsets the efficiency, making it less attractive to deploy on SNN hardware. Emerging neural encoding schemes found ways to compress the spike trains where information are represented inefficiently. This opens possibilities for shorter spike trains with greater information density. Hence accuracy can be retained at a high value.

In this paper, we present an End-to-End framework for accelerating spiking neural networks with Emerging Neural Encoding on FPGAs. E³NE enables the inference of SNN models to be deployed on almost arbitrarily-sized FPGAs. The framework builds upon efficient hand-crafted hardware blocks to execute the basic functions found in SNNs, including convolution and pooling. High performance is achieved by optimizing the instantiation and configuration of hardware blocks based on application requirements and hardware constraints. The framework employs a dynamic quantization scheme for the generation of spike trains and transformation of weights from a pre-trained SNN model. We provide open access to our GitHub repository 1 which contains source files of both the hardware and software tools for E³NE. Our contributions can be summarized as follows:

- The first end-to-end framework for spiking neural networks that is based on register-transfer level (RTL) hardware blocks.
- Optimization of data movement and logic utilization by maximizing the degree of parallelism in the generated hardware.
- Support for emerging neural encoding to increase inference throughput and accuracy.
- Outperforming of previous SNN hardware implementations with regard to accuracy, latency, power, and hardware resources.

The rest of the paper is organized as follows. Section 2 discusses existing compiler frameworks for FPGA-based machine learning hardware and reviews past implementations of SNN inference hardware. Section 3 introduces the basics of SNNs and neural encoding. We then describe the E³NE framework in Section 4 followed by the presentation of our experimental results in Section 5. Lastly, Section 6 concludes the paper.

2 RELATED WORK

Domain-specific design automation for neural network accelerators are crucial for the accessibility of fast FPGA hardware. Many previous works were presented to develop such compilers for traditional ANNs. Generally, they can be categorized into overlay-based solutions and dedicated hardware accelerators [21].

The former employs universal hardware, which is able to efficiently execute the operations involved in convolutional and fully-connected layers of a network. The overlay is supplied with data and instructions and passes the computation result back to the host. Multiple network architectures can potentially be supported without the need for reconfiguration of the FPGA. Angel-Eye [22], DNNVM [23], and DLA [24] are examples of overlay-based compilers. All of them employ parameters to control the parallelism of feature maps, input/output channels, etc., based on the number of available processing units, which in turn is constrained by on-chip hardware resources. A compiler maps convolution layers to those processing units by determining tiling parameters and generating instructions for data movement and execution schedule. Specific custom instruction sets have been developed for their accelerators. TVM [25] is a framework for the deployment of neural networks across a variety of architectures, including GPU and FPGA. A general matrix-multiply, together with appropriate buffers and memory blocks, is instantiated and controlled by an instruction fetch unit.

Ma et al. [26], on the other hand, use dedicated hardware blocks and configure them according to layer specifications. Their convolution modules have a fixed kernel size and stride. Those processing engines can be reused for layers with similar characteristics. Local configuration registers, which can be programmed during runtime, store information about the computation sequence. The proposed neural network compiler breaks down feature maps into tiles, which individually pass through a sophisticated sequence of diverse ANN operations.

While many design automation tools support conventional ANNs, there are only a few frameworks for their spiking counterparts. Due to the different computation paradigm, adapting an existing ANN framework would neglect important considerations about the time dimension. This has effects on the memory structure and access patterns. In addition, neural encoding, the update of neuron states, and spike train generation can be parts of the optimization process. Fang et al. [27] builds their hardware on top of a custom neural encoding scheme which utilizes the spike frequency as the information carrier. Their neuron model can hence be implemented as infinite impulse response filters, whose computation is efficiently implemented in digital signal processing (DSP) slices. Their compiler automatically determines bottlenecks in the computation flow and allocates more resources if the hardware platform permit. When dealing with pre-fabricated neuromorphic chips, the mapping of an SNN structure onto the fixed layout of neuron cores becomes another challenge. The LCompiler [28] is an SNN compiler for Loihi, which uses a greedy algorithm to iteratively optimize the mapping for power efficiency. With Lava [15], Intel recently announced a framework adopted for Loihi 2 and other neuromorphic platforms. Both BrainScaleS and SpiNNaker also come with their respective mapping algorithms [29, 30]. The previous examples show the advantage of neuromorphic systems on FPGA, where hardware is reconfigured to fit the network architecture, instead of vice versa.

In addition to the automated compiling tools, there are hardware implementations that take advantage of the

1. https://github.com/DanielGerlinghoff/radix-encoding
distinct properties of SNN. Minitaur [31] is an event-driven architecture, where every neuron is idle until a spike occurs at its input. Since spike trains are often sparse, this can lead to significant power efficiency improvement. Han et al. [32] use a hybrid approach for updating neurons. They iterate through the positions in the spike train in a sequential manner. Spikes at the same position are handled by an event queue. This improves the accuracy and hardware resources compared to Minitaur. However, both implementations only support fully-connected layers. In the realm of convolutional SNN accelerators, Ju et al. [33] introduce a two-dimensional array of convolution units, which reduces data movement by reusing input feature maps for multiple output feature maps. The simultaneous computation of multiple kernels and output channels reduces their runtime. However, their hardware design occupies many resources, making it difficult to be deployed on devices with small footprints. S2N [34], on the other hand, is a SIMD architecture with a high resource efficiency. The architecture was also evaluated on two-dimensional image datasets. Their work was implemented using high-level synthesis and the existing FINN framework for the acceleration of binary neural networks [35]. We will use existing SNN hardware implementations as a performance reference in the experiment section. Details on the low-level design of the hardware blocks, however, is not included in the scope of this paper.

3 Background

Spiking neural networks (SNN) are structurally similar to conventional neural networks. They consist of a sequence of layers through which information propagates. Each layer is either an array of neurons for fully-connected layers or a two-dimensional neuron feature map for convolution/pooling layers. At the neuron level, however, SNNs show inherently different characteristics from ANNs to achieve a greater resemblance of the biological processes found in human brains.

The primary method of communicating information between adjacent neurons in the spiking neural network is via spike trains instead of real values in traditional ANNs. Those are sequences \{s_0, s_1, ..., s_{T−1}\} of binary values \(s_t\) to indicate the presence (one) or absence (zero) of a spike event. Their length is denoted as \(T\), as in time steps. In contrast to ANNs, each SNN layer receives \(T\) inputs in a sequence before being able to move on to process the next input sample. If depicted as a loop hierarchy, as often done for ANN implementations, time steps are added as an additional loop (see Algorithm 3 in Section 4.2.3).

The generation of input spike trains from real values is an active research topic [35], [37]. With temporal encoding, the exact positions of spikes within the spike train relate to the represented value [38], [39]. The commonly used rate encoding sets the number of spike events over the length of the spike train proportional to the magnitude of the real value [40], [41]. This process, however, leads to severe information loss if the spike train length \(T\) is small, as only values in the range \([0, T]\) can be represented. Long spikes trains, on the other hand, require more time steps and hence increase the runtime. Previous publications used hundreds of time steps to maintain a high accuracy for large SNN models [20], [42]. Efficient neural encodings, such as [43], are able to significantly shorten spike trains to a length of less than ten. The compression of information is achieved by scaling the impact of spikes on the neurons depending on their position in the spike train. When choosing those scaling factors to be powers of two, a spike train is transformed to \{1s_0, 2s_1, ..., 2^{T−2}s_{T−2}, 2^{T−1}s_{T−1}\}. The impact of spikes on the neuron state doubles with every time step. That spike train is equivalent to the sequence of binary digits of a \(T\)-bit integer value, when read from least to most significant bit. That makes for a straightforward conversion between integers and efficient spike trains. The complexity is reduced to the selection of an appropriate method to quantize the real input values.

4 End-to-End Design Framework

This section describes E³NE in detail. First, we give an overview of the hardware library utilized by the framework. Then, we present the proposed compiler and corresponding optimization techniques. That covers the instantiation and configuration of processing modules, memory, and control instructions based on user input.

4.1 Hardware Block Library

The propagation of information in the form of binary spike trains comes with a significant advantage for hardware implementations. While ANNs rely on resource-expensive multiply-accumulate operations to determine the output value of a neuron, SNN can instead work with conditional accumulate operations. The arrival of a spike at any time step triggers the addition of a \(B\)-bit weight value to the current time step’s neuron state. In the absence of a spike, the neuron state remains unchanged. This enables us to employ arithmetic hardware blocks with a high energy and resource efficiency.

All hardware blocks are configured to adapt to the characteristics of the layers they compute. Thus, E³NE falls into the category of dedicated hardware accelerators. Processing modules for convolution and pooling can, however, be partially configured at runtime, allowing them to be reused
for multiple network layers. Two-dimensional processing modules are characterized by their number of rows $Y$ and number of columns $X$. The dimensions are fixed at the time of compilation, as is the supported kernel size, which is set to the dimension $Y$. At the same time, two degrees of freedom are provided by the hardware to allow various layers with an equal kernel size to be executed on the same processing modules. Firstly, the kernel stride can be set dynamically, provided that all desired stride values have been implemented in the hardware during compilation. Secondly, feature maps of different sizes can be computed by the same module. The exact calculation of all static and dynamic configuration parameters are covered in Section 4.2.1.

Our hardware design aims for extensive reuse of all hardware blocks, including both processing and memory modules. This resource efficiency leads to scalability in both directions, targeting both big and small FPGA devices. The data flow reflects this by sharing hardware among multiple layers. Figure 1 depicts a minimal implementation of our accelerator. Activation data is initially written into an activation memory block.ping. To compute a network layer, they are loaded into the processing module (blue arrows). That module can be any neural network operation, such as convolution, pooling and matrix-multiply. Weights are fetched as needed from a relevant weight memory block (yellow arrow). This example accommodates $L$ similar layers, each having a separate weight memory. Partial sums generated during processing are stored with high precision in the memory local to the processing module. The final output is written back to the pong block. The next layer can be executed without any additional hardware resources by reusing the processing module with a different set of weights, letting activations bounce between buffers ping and pong. Careful dimensioning of processing and memory modules by the compiler ensures that feature maps of varying size fit while maximizing hardware utilization.

An instruction decoder issues commands to memory and processing modules based on instruction words, which are stored in the local memory. Instructions are used to control the data flow and launch layer operations. Furthermore, they set configuration registers prior to starting a computation to adapt the modules to changes in the layer configuration. The sequence of instructions is unique to the network architecture and is generated by the compiler upfront.

The aforementioned principles hold true when scaling the hardware to support larger networks with a more complex architecture. With more types of layers in the network, additional specialized processing modules are necessary. A set of activation ping-pong buffers is added if both one- and two-dimensional features are handled, which is usually the case in convolutional neural networks. The instruction decoder remains the central controller for all hardware blocks.

4.2 Compilation Flow

The compiler’s task is to assemble the building blocks in the hardware library based on the user specification, such that the machine learning task can be efficiently executed. An overview of the compilation process is given in Figure 2. Compiler modules are shown in gray in the middle of the figure. We split the compilation into four sub-processes, each responsible to generate a certain part of the hardware architecture. Those sub-processes build upon each other, meaning that the sequence of execution was deliberately chosen. For example, instructions could not be generated without prior knowledge of processing and memory modules.

The user input is illustrated as green blocks in Figure 2 with green arrows indicating dependencies with compiler sub-processes. The starting point of the compilation is a neural network model, which was trained in the popular machine learning framework PyTorch [44]. The PyTorch model includes all hyper-parameters of the network, such as the architecture and layer specifications. It also contains the values of trained parameters, i.e., convolution kernels and weights for fully-connected layers. Design variables are used to constrain the hardware. Trade-offs between speed, accuracy, power and hardware resources can be achieved by adjusting variables such as resolution and parallelism. Input samples are usually stored in floating point format. The memory initialization sub-process converts them into spike trains so that they can be handled by the SNN accelerator.

Other than that, the hardware tools in blue are part of the compiler tool chain. The hardware library described earlier in Section 4.1 contains the available hardware blocks in the format of HDL files. The synthesis tool takes those together with configuration files obtained from the compiler sub-processes to generate a bitstream for the FPGA device. In the following sections, we will describe every compilation step and corresponding optimizations to achieve a high degree of parallelism and efficiency.

4.2.1 Processing Modules

The first step in the compilation process is to analyze the structure of the spiking neural network and derive the necessary processing modules (PMs) and their configurations. Each type of layer, i.e., convolution, pooling, or fully-connected layer, is computed with a dedicated PM. Through parallelism within modules, we optimize the hardware utilization for feature maps of different sizes. Parallelism between modules adjusts the computational performance. The outputs of this sub-process are configuration files with
parameters, such as the number and sizes of processing modules and routing information for different kernel strides and parallelism.

Configuration and Intra-Module Parallelism: Hardware blocks for two-dimensional operations, namely, convolution and pooling, are structurally alike and are defined by width $X$ and height $Y$. The latter is equal to the kernel size of the layer. With those dimensions being fixed in the hardware, at least one convolution/pooling module is instantiated for every kernel size occurring in the network. Algorithm 1 describes this in lines 1 and 2 by iterating over all kernel sizes in the network and instantiating the respective PMs.

Due to the reusability of hardware blocks, multiple layers can share processing modules, as long as their kernel sizes match. To avoid the need for tiling of feature maps, the width $X$ is set to the size of the largest feature map processed by the module. In Algorithm 1, $D_{out}^{(l)}$ stands for the dimension of an output channel in layer $l$. The first layer with a kernel size $K$ determines $X$, as expressed in lines 4 and 5. Figure 3 illustrates, how a processing module (green) moves across a feature map (gray) row-by-row starting at the first row. In case a), the size of the feature map matches the module and the hardware is fully utilized.

Due to pooling operations and convolution with a kernel stride greater than one, feature maps tend to vary greatly along the $X$ dimension of the processing module to increase utilization.

Algorithm 1 Generation of 2D Processing Modules

1: for all kernel sizes $K$ in the network do
2: instantiate processing module with $Y \leftarrow K$
3: for all layers $l$ with kernel size $K$ do
4: if first iteration then
5: $X \leftarrow D_{out}^{(l)}$
6: parallel channels $P^{(l)} \leftarrow \lfloor X/D_{out}^{(l)} \rfloor$
7: for $p \leftarrow 1$ to $P^{(l)}$ do $\triangleright$ index $(l)$ in loop omitted
8: $S_p \leftarrow \lfloor p * (D_{in} + \text{pad}) / \text{str} \rfloor$
9: $E_p \leftarrow S_p + D_{out} - 1$
10: create routing for $P^{(l)}$ parallel output channels
11: create routing for stride $\text{str}^{(l)}$

Each two-dimensional PM has potentially multiple settings for parallelism, as well as kernel stride. To allow the data flow to be adjusted dynamically during runtime, all settings have to be reflected in the hardware at the time of synthesis. Therefore, the compiler incorporates the necessary routing beforehand while configuring the hardware blocks (see Algorithm 1 line 10 & 11).

The one-dimensional processing module for fully-connected layers exhibits far less complexity compared to two-dimensional PMs. Configuration is limited to the number of parallel-computed output features. Since every operation requires a separate weight, the parallelism is bounded by the bandwidth of the memory used to store the weight values.

Inter-Module Parallelism: Depending on the use case of our SNN accelerator, different constraints for performance, power, and hardware resources exist. E²NE aims for high scalability to allow power and area efficient processing modules deployed on small and cost-effective FPGA devices. When higher performance is required, the inter-module parallelism can be realized by instantiating more than one processing module for each kernel size. The data flow is duplicated for all parallel PMs such that the output channels are computed concurrently. That is equivalent to unrolling the output channel loop as can be seen in Algorithm 1 line 3.

Through the design variables, the user can specify the number of parallel processing modules. In practice, however, only the duplication of convolution modules has a notable impact on the performance. For other PMs, the time to transfer data quickly exceeds the time spent on the actual computation. In this case, more memory bandwidth is necessary to achieve any further speed-up. The same limits apply to the convolution modules. However, due to the large amounts of computations involved in the convolution operation, this effect becomes obvious only with a larger number of parallel modules.

4.2.2 Memory and Initialization

The next two sub-processes of the compilation flow are related to the memory for activations and network parameters. Memory blocks are characterized by their width $W$ and height $H$. Our compiler sizes every memory module individually to minimize their resource consumption, while
ensuring the fit of the data to be stored. Therefore, the initialization sub-process is executed first. That also includes weight quantization and spike train generation as part of the neural encoding scheme. Important trade-offs in terms of accuracy, latency, and memory resources are made during that process.

**Weight Memory:** The PyTorch model holds the trained parameters of the convolution and fully-connected layers in floating point format. Quantization is needed before the weights can be used with our SNN accelerator. To minimize the information loss, E²NE employs a dynamic quantization scheme based on [45]. Specified by the user as a design variable, $B$ is the number of bits for the representation of weight and kernel values. This number is constant throughout the computation of the whole network. The range of weight and kernel values. This number is constant through.

The PyTorch model holds the trained weight values, however, might vary between layers. To pack out the computation of the whole network. The range of weight and kernel values. This number is constant through.

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During the third sub-process of the compilation, memory is reserved for both the weights and activations. During the first sub-process, the weights are quantized and packed into read-only memory blocks, which is sized according to the memory capacity, the compiler decides between them. That allows to read all values needed for the computation during a single clock cycle.

The second option for weight storage is chosen, if not all parameters fit into on-chip memory. They are initially written to the external memory. Before the execution of every layer, respective weights are loaded dynamically into a single block RAM in the FPGA device, from where they can be accessed just like the ROM. For the memory dimensions, the maximum values for $W$ and $H$ in Equation 3 over all layers are chosen.

**Activation Buffers:** Spike trains are encoded efficiently to reduce their length, as described in Section 3. Each position in the spike train corresponds to a binary digit of an $T$-bit integer number. Generating this $T$-bit integer follows the same dynamic quantization scheme as the weights. For every layer $l$, a scaling factor $R_{act}^{(l)}$ is computed with Equation 4. In contrast to the weights, which are fixed at the time of compilation, the magnitude of activations depends on the input given to the SNN model and is thus not strictly bounded. Instead, the maximum activation value $v_{act}^{(l)}$ is computed for every layer $l$ across all input samples of a representative dataset.

This ensures that typical network inputs can be represented by a spike train of length $T$ without the need for clamping after being scaled with $R_{act}^{(l)}$. Equation 5 expresses the generation of a spike train $S$ based on an input value $v_{act}^{(l)}$ and the scaling factor $R_{act}^{(l)}$ of the first layer. The operation \( \otimes_2 \) denotes the representation as binary digits.

The accumulation of integers require the result to be represented with a higher number of bits than the operands in order to avoid information loss. To prevent the bit width of activations to in the course of evaluating a model, the activations are requantized after every convolution or fully-connected layer to rectify the position of the radix point for the next layer. Partial sum value $v_{psum}^{(l)}$ is the high-precision result of the accumulation. Precision is reduced by a right-shift operation in Equation 6 such that the position of the radix point matches the activation scaling factor of layer $l + 1$. Trimming digits leads to numbers being rounded down, increasing the requantization error. Rounding to the nearest integer is achieved by a conditional add operation.

Spikes trains are stored in alternating buffers after being requantized. The sizes of those buffers are determined by simulating the network execution and recording the size required to store activations, as done in Algorithm 2 for two-dimensional feature maps. The buffer is expanded to at least the size required to store the respective feature maps. One row of binary spike activations is stored per memory address, requiring width $W$ to be at least of dimension

\[
W = K^2 \cdot B
\]

\[
H = C_{out} \cdot C_{in}
\]
Effort required. Optimization can be applied to reduce data layer types, which is the reason for the high computational solution layers have the deepest loop hierarchy among all for a convolution layer is shown in Algorithm 3. Convolution Loop Hierarchy and Instructions

Algorithm 3 Convolution Loop Hierarchy and Instructions

1: configure hardware
2: select of memory modules
3: for all output channels do \(\triangleright \) partially unrolled
4: for all time steps do \(\triangleright \) accumulating
5: for all input channels do \(\triangleright \) accumulating
6: reset
7: load kernels into PMs
8: load first activation row from ping
9: for all activation rows do
10: start processing \(\triangleright \) acc. & unr.
11: for all kernel rows do \(\triangleright \) acc. & unr.
12: for all kernel cols do \(\triangleright \) acc.
13: accumulate over the kernel
14: load next activation row from ping
15: wait for processing to finish
16: write partial sum
17: accumulate with previous input channels
18: requantize activations
19: write activations to buffer pong

The compiler follows the loop hierarchies when analyzing the network layer-by-layer and generates 32-bit instructions for every operation. Each instruction belongs to one of the four categories shown below. Instructions of different categories differ with respect to their function and format. Apart from the operation code, the available bits are used to indicate configuration parameters, wait conditions, etc. Figure 4 visualizes the anatomy of each instruction category. The full instruction set is described in Table 1 with the last column indicating the category of the instruction.

- Configuration of processing modules and memory
- Commands to launch computations and reset
- Memory operations for kernels and activations
- Wait for processes to complete

At the beginning of each convolution layer, the hardware is configured to the specifications of the layer. That includes setting the parallelism, stride, and scaling factors for requantization. Subsequently, it is selected from which memory to fetch the weights and which memory modules act as ping-pong buffers. For every input channel, the processing modules (PMs) involved in the current layer’s computation are reset and receive their respective kernel values. The processing is started separately for each activation row, after the data have been loaded from the buffer ping. An opportunity for parallel execution arises, when the processor stalls while the computation is ongoing. During that waiting

4.2.3 Instructions

Every action of the accelerator hardware is controlled by instructions. That includes the dynamic configuration of the aforementioned hardware blocks, data movement and launch of neural network operations. The sequence of instructions is derived for every layer from its loop hierarchy. That is an expression of the nested iterations taken over channels, feature maps, kernels, etc. Our loop hierarchy for a convolution layer is shown in Algorithm 3. Convolution layers have the deepest loop hierarchy among all layer types, which is the reason for the high computational effort required. Optimization can be applied to reduce data movement and necessary memory capacity, as done before for ANNs by [46], [47]. We interchanged loops such that accumulating (acc.) loops, like input channels and time steps, are executed before output channels, i.e., making them the inner loops. That reduces the memory footprint, since less high-precision partial sums have to be stored immediately.

Unrolling (unr.) is another loop optimization enabled by parallelism in hardware, as described earlier in Section 4.2.1. Since not all output channels are computed in parallel, the loop is only partially unrolled.

Fig. 4: Formats of each instruction category used by the processor.

\[ D_{in} \]. The height \( H \) depends additionally on the number of channels \( C_{in} \) and time steps \( T \). The target buffer changes between ping and pong after each layer.

Algorithm 2 Generation of 2D Ping-Pong Buffers

1: \((W_{ping}, H_{ping}) \leftarrow (0, 0)\)
2: \((W_{pong}, H_{pong}) \leftarrow (0, 0)\)
3: \(pp \leftarrow ping\)
4: for all layers \( l \) with dimension \( D_{in}^{(l)} \) and channels \( C_{in}^{(l)} \) do
5: \(\text{if } pp = ping \text{ then}\)
6: \(W_{ping} \leftarrow \text{max}(W_{ping}, D_{in}^{(l)})\)
7: \(H_{ping} \leftarrow \text{max}(H_{ping}, D_{in}^{(l)} * C_{in}^{(l)} * T)\)
8: \(pp \leftarrow pong\)
9: \(\text{else if } pp = pong \text{ then}\)
10: \(W_{pong} \leftarrow \text{max}(W_{pong}, D_{in}^{(l)})\)
11: \(H_{pong} \leftarrow \text{max}(H_{pong}, D_{in}^{(l)} * C_{in}^{(l)} * T)\)
12: \(pp \leftarrow ping\)
time, the next activation row is loaded. This engagement of multiple hardware circuits at the same time can shorten the runtime. Results of the convolution operation are written into a partial sum memory, where they are accumulated over all input channels. After all time steps have been processed, instructions are generated which requantize the output feature maps and write them back to buffer pong.

To avoid data hazards, our instruction decoder does not have multi-processing capabilities. We implemented a scalar processor without support for pipelining. Instructions in the processor-internal RAM are fetched one-by-one. In a typical neural network application, one can expect roughly 0.4 instructions per clock.

5 EXPERIMENTS

In this section, we explore how different settings of the compilation parameters affect the performance and efficiency of the spiking neural network inference. The experiments in Sections 5.1 to 5.4 are carried out on the MNIST dataset [48] using the LeNet-5 network [49]. MNIST consists of 60,000 training images and 10,000 test images of handwritten digits. It is a common dataset to verify SNN-related algorithms and hardware. LeNet is an early convolutional neural network designed to classify images of the MNIST dataset and hardware. LeNet has a homogeneous network architecture, because all convolution layers use a kernel size $K = 5$ and for all pooling layers $K = 2$. For that reason, the LeNet can be evaluated using only two processing modules (PMs) with $Y = 5$ and $Y = 2$ for convolution and pooling, respectively.

The width $X$ of the PMs is set according to size of the largest output feature map that they process. In that case, $X = 31$ for the convolution module and $X = 14$ for the pooling module. With 3-bit weights and a spike train length of $T = 4$, our LeNet SNN can achieve a reasonable accuracy of 99.09%. The weight quantization was carried out with the parameter $r = 3$ (see Equation 2), i.e., values in the range of three standard deviations can be represented by three bits without clamping.

By default, the compiler uses intra-module parallelism to increase the hardware utilization, as described in Section 4.2.1. In the case of LeNet, the convolution module is reused by all three convolution layers due to their equal kernel size. More than one output channel can be computed simultaneously for the second and third convolution layer. The output channel sizes of all two-dimensional layers are listed in Table 2. With the widths of the PMs fixed, the compiler determined the settings for intra-module parallelism as seen in the third column of that table. The smaller the output channel size, the more parallel channels can be placed in the PM. This does not affect the classification results and the accuracy, since the operations stay the same.

This experiment demonstrates the effect of intra-module parallelism. In Table 2, we compare the hardware utilization and runtime of each layer with and without parallel computing. In the second case, the PMs only compute one output channel at a time, as shown before in Figure 3 b). This negatively affects the hardware utilization of the last three layers. Even with parallelism, however, the placing along the width of the PM depends on the input channel size and padding (see Algorithm 1, line 8). This limits a further increase in hardware utilization.

More pronounced is the effect on the runtime. The total runtime of LeNet increases fourfold with intra-module parallelism disabled. It can be observed that especially convolution layers benefit. The runtime is almost inversely proportional to the degree of parallelism. In case of the last convolution layer, for example, using one instead of six parallel channels increases the runtime by 5.2 times. Pooling layers, on the other hand, only see a slight speedup when using parallel computing. Because the number of operations is significantly less compared to convolution layers, the data transfer has a larger impact on the runtime. For the same reason, we will apply inter-module parallelism in the next section to convolution layers only.

5.2 Inter-Module Parallelism

Through a design variable, the user can instruct the compiler to instantiate more than one convolution module for every kernel size. In contrast to intra-module parallelism, the objective is not to increase the utilization of existing hardware. Instead, additional hardware resources are required for inter-module parallelism. Those trade-offs are explored in this experiment. We use the same LeNet network architecture, compilation settings, and hardware platform as in the previous section. Intra-module parallelism is enabled by default.
TABLE 2: Intra-Module Parallelism (Intra-MP) of convolution and pooling layers in LeNet with an input image size of $32 \times 32$ pixels.

| Layer Size | Para. Util. [%] | Time [µs] | With Intra-MP | Util. [%] | Time [µs] | Without Intra-MP |
|------------|----------------|-----------|---------------|----------|-----------|-----------------|
|            |                |           | With Intra-MP |           |           | Without Intra-MP |
| 6C$^5$ 28  | 1              | 90        | 46            | 90       | 46        |                 |
| P2 14      | 1              | 100       | 13            | 100      | 13        |                 |
| 16C$^5$ 10 | 2              | 65        | 154           | 32       | 301       |                 |
| P2 5       | 2              | 71        | 10            | 36       | 12        |                 |
| 120C$^5$ 1 | 6              | 39        | 476           | 6        | 2464      |                 |
| Total      | 69             | 699       | 49            | 2836     |           |                 |

Fig. 5: Latency, power and hardware resources (lookup tables and flip-flops) when varying the number of parallel convolution modules from 1 through 10.

Various metrics are plotted in Figure 5 with dependence on the number of parallel convolution modules. The main goal of instantiating multiple modules is achieved as can be seen from the latency plot. The latency tends to decrease when more convolution modules are used. Compared to the baseline of one module (705 µs), the processing time is reduced to only 31% when using ten parallel modules (216 µs). One can observe a convergence of the latency values with a growing number of parallel modules. This is expected and in accordance with the Roofline model, which provides intuitive explanations for the limitations of hardware architectures [52]. In its essence, it assumes that hardware performance is limited either by the accelerator’s peak performance or the memory bandwidth. Ideal architectures reach a performance close to one of those limits. Whether the peak performance or the memory bandwidth is the bottleneck depends on the Computation-to-Communication (C/C) ratio. The time used for computation of the convolution operations decreases when using more parallel modules. The time spent on communication is roughly constant, since the same amount of data has to be moved between processing and memory modules. Hence, the C/C ratio of our SNN accelerator decreases, which leads to the application being memory bounded. This effect is visualized by the latency values, which converge to the communication time of around 200 µs. It can also be observed that the latency slightly increases between five & six and eight & nine parallel modules. In these cases, additional modules remain unutilized and lead to no reduction of the computation time. However, additional clock cycles are set aside to configure these additional hardware blocks, causing an increase in overall latency.

The plot of power values in Figure 5 shows the expected increase in power consumption with increasing number of instantiated hardware blocks. Interestingly, a larger increase in power goes together with a larger drop in latency and, vice versa, a smaller power increase coincides with no changes in latency. This correlation does not provide a definitive explanation to the cause and effect. However, we can reason that the dynamic power of additional modules is negligible when they are not utilized. Only the static power, which is consumed regardless of the module’s activity, causes the minor increase in overall power.

Hardware resources shown in Figure 5 are measured in terms of the number of 6-input lookup tables (LUTs) and flip-flops (FFs). A very linear behavior can be observed, with around 4900 additional LUTs and 4500 flip-flops for every added convolution module. The remaining hardware resources are shared mainly between a pooling module (200 LUTs, 500 FFs), a linear module (4800 LUTs, 2900 FFs), and the instruction decoder (500 LUTs, 200 FFs).

This experiment confirmed most of our expectations regarding the metrics for a variable number of parallel convolution modules. For high-performance applications, where hardware cost and power consumption are of less importance, a high degree of parallelism can be chosen. Embedded devices, which operate with a tight power budget, can execute the task with identical accuracy at the cost of a larger latency.

5.3 Instruction Parallelism

A naive compiler implementation would generate instructions in sequence, following the loop hierarchy of the network layers. This experiment analyzes the impact of reordering instructions such that multiple hardware circuits are utilized at the same time. Network architecture and hardware configuration is identical to the previous two experiments.

For every row of a two-dimensional feature map, a start instruction activates the processing module (see Algorithm 3, line 10). It needs no additional supervision by the instruction decoder until the activation row is fully processed. Hence, the processor stalls and waits for the computation to finish. In the case of LeNet, the waiting time without reordering equals eight clock cycles for convolution layers. The waiting time mainly depends on the number of kernel columns, whose loop is not unrolled and thus executed sequentially (see Algorithm 3, line 12). Our compiler makes the processor use those idle clock cycles for loading the next activation row. Since this process has a duration of two clock cycles, the idle time can be reduced to six cycles.

The influence of instruction parallelism on the latency varies depending on the number of convolution units, as can be observed from the measurements in Table 3. In case of a single convolution module, instruction parallelism reduces the latency by 11%. However, the effect decreases with more parallel convolution modules being deployed. Only 5% of latency reduction is achieved with eight modules. A potential reason is the overall decrease in the number of start and, therefore, wait instructions executed by the processor when parallelism is increased. That means, the
TABLE 3: Latency with and without instruction parallelism (IP) for various degree of inter-module parallelism (Inter-MP).

| Inter-MP | Without IP | With IP | Latency Reduction |
|----------|------------|---------|------------------|
|          | Latency [µs] |         |                  |
| 1        | 789        | 705     | 11%              |
| 2        | 471        | 429     | 9%               |
| 4        | 316        | 294     | 7%               |
| 8        | 252        | 240     | 5%               |

Fig. 6: Validation accuracy, latency and the size of activation memory dependent on the spike train length, i.e. number of time steps $T$.

Reducing the remaining waiting time by two clock cycles has a limited effect on the total latency. Put in terms of C/C ratio covered in the previous section, the improvement of computation time has a smaller effect when the communication time dominates the total runtime.

5.4 Spike Train Length

This experiment explores the relationship between spike train length and classification accuracy, which is a common trade-off in spiking neural networks. The spike train length was used interchangeably with the number time steps $T$ in Section 3, which indicates an additional impact on the execution time. The LeNet model and hardware settings are reused from the previous experiments. No inter-module parallelism is applied here.

Figure 6 shows the results for a spike train length ranging from two to eight. At the lower end of this range, the validation accuracy drops sharply to only 95.4%. This is a practical lower limit, since binary activation, i.e., $T = 1$, would lead to an unacceptable accuracy of less than 50%. The classification of the MNIST test images becomes more accurate as the spike trains become longer. Because longer spike trains can represent a wider range of activation values, the quantization error is reduced. On the upper end of the length range, we achieve a maximum accuracy of 99.28%. The curve flattens out towards the end and further lengthening of the spike trains would not lead to any accuracy gain due to the inherent limitations of the LeNet model.

Reaching the maximum accuracy with only eight time steps is made possible by efficient encoding. Because $2^T - 1$ values can be represented per spike train, the error caused by quantization after every layer is reduced exponentially when adding more time steps. In comparison, Fang et al. [27] needed nine time steps to reach an accuracy of approximately 99.2%. Our encoding attained the same accuracy with only five time steps, or around 55% of their spike train length.

Longer spike trains, however, lead to a linear increase in latency as can be seen in the lower plot of Figure 6. Time steps are processed in sequence by the hardware accelerator. Hence, more time passes until the classification result becomes available at the output. With the compilation settings used for this experiment, each additional time step leads to a latency increase of around 170 µs. Moreover, spike trains are stored in ping-pong buffers between layers. Their size needs to be adjusted to account for the additional data. The lengthening of spike trains increase the capacity of activation memory by increments of 7.6 kbits.

5.5 Performance Comparison and Scalability

The classification of the handwritten digits in the MNIST dataset was attempted before on SNN hardware. Table 4 compares those research efforts with regards to common metrics, such as accuracy, latency, power and hardware resources. Furthermore, a cross-platform comparison is provided, which demonstrates the performance of SNN hardware in relation to other popular machine learning architectures.

Ju et al. [33] employs a custom convolutional neural network (CNN) with 169k parameters. They can achieve 99.2% of accuracy. The reuse of hardware blocks, which are small, leads to a small area impact. They use 4x more flip-flops (FFs), which could be a consequence of using high-level synthesis in their compilation flow. Over-all, this comparison summarizes the advantages of E3NE. Optimizations and parallelism are applied to almost all subprocesses of the framework. Combined with the use of an efficient neural encoding scheme, that yields a remarkable reduction in latency and power, while maintaining a high level of accuracy. The reuse of hardware blocks, which themselves have small area requirements, leads to a small footprint suitable for deployment on low-cost FPGAs.
TABLE 4: Comparison among SNN hardware implementations with regards to performance and efficiency.

| Platform       | Dataset     | Network     | Accuracy [%] | Frequency [MHz] | Latency [µs] | Throughput [fps] | Power [W] | LUTs / FFs         |
|---------------|-------------|-------------|--------------|-----------------|-------------|-----------------|-----------|-------------------|
| Ju et al. [33] | MNIST       | CNN⁴        | 98.9         | 150             | 6110        | 164             | 4.6       | 107k / 67k        |
| Fang et al. [27] | MNIST      | CNN⁵        | 99.2         | 125             | 7530        | 2124            | 4.5       | 156k / 233k       |
| E3NE (this work) | MNIST   | CNN⁶        | 99.3         | 200             | 409         | 2445            | 3.6       | 41k / 36k         |
| E3NE          | MNIST      | LeNet-5     | 99.1         | 200             | 294         | 3400            | 3.4       | 27k / 24k         |
| E3NE          | CIFAR-10   | AlexNet     | 80.6         | 150             | 70k         | 14.3            | 4.7       | 48k / 50k         |
| CIFAR-100     | CNN⁷       | VGG-11      | 65.0         | 150             | 163k        | 6.1             | 5.0       | 88k / 84k         |
| RTX 5000      | CNN⁸       |             | —            | 1620            | 18k         | 864             | 61.2      | (GPU)             |
| i7-6700K      | CNN⁹       |             | 99.9         | 4000            | 252k        | 4               | 54        | (CPU)             |
| TrueNorth     | CNN⁶       |             | 99.4         | —*⁴             | 1000        | 1000            | 0.2       | (ASIC)            |
| Loihi         | CNN⁶       |             | 94.7         | 0.01            | 10k         | 97              | 0.24      | (ASIC)            |

1 28×28 – 64C5 – P2 – 64C5 – P2 – 256 – 10, 2 28×28 – 32C3 – P2 – 32C3 – P2 – 256 – 10, 3 32×32 – 16C5 – P2 – 8C3 – P2 – 100 – 10
4 Asynchronous event-based execution without a global clock

Our comparison is limited to SNN hardware which is able to handle convolutional layers, since they are used without exception in modern neural network architectures. The classification of MNIST images is, however, possible with fully-connected layers only. Three-layer networks were implemented by Minitaur [31] and Han et al. [32]. Their power consumption benefits form the simple network structure and the reduced computational effort. But accuracy was negatively impacted such that their result is not on par with the listed convolutional SNN implementations.

The advantages of custom SNN hardware deployed on FPGA becomes obvious, when compared with other computing platforms as done in Table 4. Nvidia RTX 5000 is a GPU widely used for deep learning applications. When presumably used with a large batch size, it can process over 800 images per second, but latency and power consumption are at least an order of magnitude higher than for E3NE. This support for batch parallelism is limited in CPUs, like the Intel i7-6700K, which affects both the latency and the throughput. TrueNorth by IBM [12] is a custom neuromorphic ASIC, which demonstrates the potential of SNN hardware when optimized for low power consumption. Its lack of malleability, however, inhibits the scalability and generality, as network models have to be specifically designed and trained to be compatible with the static architecture. Similarly, Intel’s Loihi chip imposes restrictions on the number of inputs of each neuron core, which requires a special adaptation and mapping of a network structure to the chip’s architecture [14].

As expected from a generic framework, E3NE can deploy a wide variety of convolutional SNN. That includes small models like LeNet, which has a relatively low number of 61k parameters. We used 3-bit weights and four time steps for activations in this experiment. That allows all data to be stored in on-chip memory, avoiding external DRAM access. That contributes to the comparably low energy consumption. Another power-saving factor is the small amount of logic resources required, even with four parallel convolution modules being used. In fact, a large amount of energy could be saved by deploying the accelerator on a much smaller FPGA device. When synthesized for an XC7U3P, the smallest part with the Xilinx Ultrascale+ architecture, a mere 1.2 W of power dissipation were reported. The inference of LeNet has accuracy of 99.09%, while processing 3400 images per second. On the other end of the spectrum, two larger networks AlexNet [51] and VGG-11 [50] were executed. The CIFAR datasets come closer to real-world image data, as they picture photographs of objects in their natural environment. That makes them considerably more challenging to classify than MNIST’s handwritten digits. Moreover, the CIFAR-100 dataset contains objects of 100 different classes. Understandably, the SNN models are significantly larger containing more than 23 million parameters each. Due to the increased complexity of both SNN model and dataset, six time steps and 6-bit weights are used to reach an acceptable accuracy. The quantity of parameters and layers influences the latency, which falls into the range of milliseconds for both AlexNet and VGG. Eight parallel convolution modules have been used to mitigate the relatively high runtime. To no surprise, this and the need for external memory accesses result in higher power and logic resources. Despite the large models, less hardware resources are used compared with [33] and [27], displaying the area efficiency and scalability of E3NE.

6 Conclusion
In this paper, we presented E3NE, an end-to-end framework for the inference of spiking neural networks with emerging neural encoding. It relies on an RTL hardware library, which contains area efficient processing modules for common SNN operations. Their capability to be dynamically reconfigured is exploited by the compiler, whose objective is an optimal utilization of the instantiated hardware for the sake of efficiency and performance. Both of those goals are also addressed by the emerging neural encoding scheme. We describe the technique to generate spike trains from real-valued input samples using dynamic quantization. The execution is controlled by a sequence of instructions, which is generated in accordance with the layers’ loop hierarchies. Through loop interchange and unrolling, we found a balance between processing speed and memory requirements. The reordering of instructions enabled parallelism on a macro-level, as two different segments of the logic were operating concurrently.
A variety of experiments demonstrated the impact of optimizations and trade-offs found in E3NE. Besides the importance of parallelism for hardware utilization, we observed how the spike train length affects the performance and accuracy. When compared with previous FPGA-based SNN accelerators, E3NE outperforms with respect to all metrics. Especially the superiority in terms of power and hardware resources allowed us to deploy larger SNN models on the FPGA accelerator.

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