Abstract—General Matrix Multiplication (GEMM) has a wide range of applications in scientific simulation and artificial intelligence. Although traditional libraries can achieve high performance on large regular-shaped GEMMs, which often behave not well on irregular-shaped GEMMs, which are often found in new algorithms and applications of high-performance computing (HPC). Due to energy efficiency constraints, low-power multi-core digital signal processors (DSPs) have become an alternative architecture in HPC systems. Targeting multi-core DSPs in FT-m7032, a prototype CPU-DSPs heterogeneous processor for HPC, an efficient implementation - ftIMM - for three types of irregular-shaped GEMMs is proposed. ftIMM supports automatic generation of assembly micro-kernels, two parallelization strategies, and auto-tuning of block sizes and parallelization strategies. The experiments show that ftIMM can get better performance than the traditional GEMM implementations on multi-core DSPs in FT-m7032, yielding on up to $7.2 \times$ performance improvement, when performing on irregular-shaped GEMMs. And ftIMM on multi-core DSPs can also far outperform the open source library on multi-core CPUs in FT-m7032, delivering up to $3.1 \times$ higher efficiency.

Index Terms—Matrix-matrix multiplication, Irregular-shaped matrix, DSPs, Performance optimization

I. INTRODUCTION

As a key routine of the Basic Linear Algebra Subroutines (BLAS) library, the general matrix-matrix multiplication (GEMM) has been extensively applied in various fields, such as scientific simulations, data analytic and deep learning. There are many well-known BLAS libraries [1]–[3], which provide highly optimized GEMMs for specific platforms. Unfortunately, the optimization has mainly focused on large regular-shaped matrices (where both dimensions of matrices are large and close to each other), which are the most common cases in the High Performance Linpack (HPL).

With the evolution of GEMM applications, the sizes and shapes of matrices involved in GEMM can often be notably changing when different algorithms and input data are carried out. In the field of scientific simulations, the application of Finite Element Method (FEM) in fluid dynamics generates many GEMMs working on small matrices [4]. In the field of traditional machine learning, the implementation of classical K-means clustering algorithm calculates the distance between many samples and multiple centroids by the means of GEMM [5], where the sizes of matrices are determined by the number of samples, centroids, and dimensions for each sample. For most datasets [6], [7], the number of samples are much bigger than the numbers of centroids and dimensions, which are usually small, so that the input matrices in K-means are irregular-shaped matrices where one dimension is much larger than the other [8]. In the field of deep learning, the general implementation of convolutional layers often transforms convolution operations into equivalent GEMM by means of image-to-column method (known as im2col) [9], [10]. One dimension of the matrix generated by im2col is equal to the product of the number, height and width of output images, and the other is dependent on the product of the number of channels, height and width of filters in convolutional layers. For the first layers of most Convolutional Neural Networks (CNNs) [11], [12], the former is much bigger than the latter. From the top to bottom layers in CNNs, the output images gradually become smaller, and the number of channels increases gradually, so the sizes and shapes of matrices in GEMM also varies greatly.

Recently, there have been many efforts focusing on the optimization of irregular-shaped GEMMs on GPUs and CPUs. Rivera and Chen et al. [8], [13], [14] proposed different algorithms for the optimization of irregular-shaped GEMMs with input matrices of various shapes on GPUs. Ernst [15] et al. described the implementation of real and complex irregular-shaped GEMMs on GPUs. Tang [16] et al. evaluated the performance of Tensor Core-based mixed-precision irregular-shaped GEMMs on GPUs. Yang et al. [17] first conducted the optimization for irregular-shaped GEMMs running on ARMv8 CPUs. Li et al. [18] proposes an auto-tuning framework for irregular-shaped GEMMs on CPUs with different architectures.

Due to the constraints of energy efficiency and power consumption, low-power embedded architectures have been introduced into the heterogeneous computing domain in high-performance computing, such as digital signal processors (DSPs) [19]–[21]. Compared to CPUs and GPUs, DSPs often features Very Long Instruction Word (VLIW) or vector cores without out-of-order execution. What’s more, cores in DSPs typically work on software managed on-chip memory, and integrates Direct Memory Access (DMA) engines for data transmission between on-chip software managed memory and off-chip main memory. As a result, existing optimizations for
GEMMs on CPUs and GPUs are not directly fit for GEMMs on DSPs. While the efficient implementations of regular-shaped GEMMs targeting DSPs have been intensively studied in [22]–[24], there are few works focusing on the optimization of irregular-shaped GEMM on DSPs.

FT-m7032 is one of the prototype CPU-DSPs heterogeneous processors explored by our university to accomplish general computing by means of DSPs. It integrates 16 ARMv8 CPU cores for running operating systems, and 4 multi-core general-computing DSP (GPDSP) clusters for providing maximum computing performance, detailed explained in Section II. Targeting multi-core DSPs (also called GPDSP clusters) in FT-m7032, this paper presents an efficient implementation for irregular-shaped GEMMs. To the best of our knowledge, this is the first work which optimizes irregular-shaped GEMMs on multi-core DSPs. The main contributions of this paper are as follows.

- We analyze problems and challenges of optimizing irregular-shaped matrices on multi-core DSPs in detail. It is found that various micro-kernels and parallelization methods are indispensable for irregular-shaped GEMMs to achieve high performance.
- We propose a new implementation (ftIMM) for three types of irregular-shaped GEMMs on multi-core DSPs in FT-m7032. ftIMM integrates various micro-kernels by the automatic generation of micro-kernels, provides different parallelization strategies, and can automatically choose the optimal block sizes and the parallelization strategy for irregular-shaped input matrices by dynamic adjusting.
- The experiments on FT-m7032 show that ftIMM can provide various auto-generated micro-kernels which can achieve close to theoretical performance. For three types of irregular-shaped GEMMs, ftIMM can achieve a speedup of up to 7.2 times against the traditional efficient GEMM implementations [23], [24]. Further, ftIMM on multi-core DSPs can get more than 3.1x improvement of efficiency compared with the OpenBLAS library [1] running on multi-core CPUs on FT-m7032.

II. FT-M7032 HETEROGENEOUS PROCESSOR

The FT-m7032 heterogeneous processor consists of one 16-core ARMv8 CPU and four GPDSP clusters, as shown in Fig. 1. The multi-core CPU is a simplified version of Phytium FT-2000plus Processor [25]–[27], and is chiefly responsible for process-level management and communication. The single-precision floating point peak performance of the multi-core CPU is 281.6 GFlops. Each GPDSP cluster includes eight DSP cores, which share 6 MB on-chip Global Shared Memory (GSM). All eight DSP cores and GSM in each cluster can communicate via an on-chip crossbar network, and the data coherency among them need to be maintained by software developers. The multi-core CPU and four GPDSP clusters share the same main memory space. The multi-core CPU can access the whole main space, but each GPDSP cluster can only access its own corresponding part with 42.6 GB/s hardware bandwidth. As the cache coherency among cores in the CPU is provided as in FT-2000plus, the cache data of CPU must be written back to the main memory before a function running on each GPDSP cluster starts, and be evicted after it finishes.

Each DSP core in each GPDSP cluster, based VLIW architecture, includes an instruction dispatch unit (IFU), a scalar processing unit (SPU), a vector processing unit (VPU) and a DMA engine, as shown in Fig. 2. IFU is designed to launch up to 11 instructions per cycle, which incorporate 5 scalar instructions and 6 vector instructions. SPU is used for instruction flow control and the scalar computation, and mainly consists of Scalar Processing Element (SPE) and 64 KB Scalar Memory (SM), which match five scalar instructions. VPU provides the main computing performance for each DSP core, including 768 KB Array Memory (AM) and 16 vector processing elements (VPE) working in a SIMD manner. Each VPE has 64 64-bit registers and three fused multiply-add (FMAC) units, one of which can deal with two FP32 multiply-add computation per cycle. In other words, the SIMD width for FP32 data type is 32 and each DSP core can provide a peak performance of 345.6 GFlops when working at 1.8 Ghz. AM can deliver up to 512 bytes per cycle to registers by means of two load-store vector units. Between SPU and VPU, data can be transferred through the broadcast instruction and shared registers. The DMA engine is utilized to transfer data between different levels of memories (i.e. main memory, GSM, and SM/AM).

III. MOTIVATION

A. Irregular-shaped GEMMS

This paper mainly involves the optimization of single precision GEMMs with irregular-shaped matrices on a GPDSP cluster of FT-m7032, where at least one of M and K is sufficiently large and N ≤ 96. In other word, for the three matrices (A, B and C) in GEMMs (C += A×B), at least one matrix is tall-and-skinny (i.e., the height is significantly larger than the width). Specifically, there are three types of matrix-matrix multiplications: the multiplication between a tall-and-
A. Algorithm 1: Traditional GEMM Implementation (TGEMM)

input : $A[M][K]$, $B[K][N]$
output: $C[M][N]$

1. Set $m_g = 512$, $k_g = 512$, $n_a = 96$ and $m_s = 6$
2. for $i = 0$: $m_g$: $M$ do
   3. for $j = 0$: $k_g$: $K$ do // Ping-pong
   4. DMA($A_{i,j}[m_g][k_g] \rightarrow A_{g}[m_g][k_g]$)
   5. for $t = 0$: $n_a$: $N$ do in parallel // Ping-pong
      6. DMA($B_{j,t}[k_g][n_a] \rightarrow B_{g}[k_g][n_a]$)
      7. DMA($C_{i,t}[m_g][n_a] \rightarrow C_{g}[m_g][n_a]$)
      8. for $ii = 0$: $m_s$: $m_g$ do // Ping-pong
      9. DMA($A_g[m_g][k_g] \rightarrow A_{s}[m_s][k_g]$)
     // Micro-kernel
    10. $C_{a}[m_s][n_a] = A_{s}[m_s][k_g] \times B_{s}[k_g][n_a]$
    11. DMA($C_{a}[m_s][n_a] \rightarrow C_{s,t}[m_s][n_a]$)

Algorithm 2: Implementation of Micro-Kernel in TGEMM

input : $A_s[m_s][k_g]$, $B_s[k_g][n_a]$
output: $C_a[m_s][n_a]$

1. Set $V = 32$, $v_n = (n_a + V - 1)/V$
2. VPU loads $C_a[m_s][n_a]$ to vector registers $V_{e,0:m_s,0:v_n}$
3. for $kk = 0$: $1$: $k_g$ do
   4. for $mm = 0$: $1$: $m_s$ do // hide the latency of FMAC units
      5. SPU loads $A_{s,m_m,k_k}$ to scalar register $R_{m_m}$
      6. SPU broadcasts $R_{m_m}$ to vector register $V_{a,m_m}$
      7. for $nn = 0$: $1$: $v_n$ do // map to FMAC1-3
      8. VPU loads $B_{s,k_k,m_m,n_n} \times V_{e,0:m_s,v_n}$ to vector register $V_{b,n_n}$
      9. $V_{c,m_m,n_n} = V_{a,m_m} \times V_{b,n_n}$
     10. VPU store $V_{e,0:m_s,0:v_n}$ back to $C_{a}[m_s][n_a]$
C. Analysis of Applying TGEMM to Irregular-shaped Matrices

As shown in [23], [24], TGEMM can get good performance on large regular-shaped matrices. However, there are several problems and challenges in the application of TGEMM to irregular-shaped matrices.

First of all, only a micro-kernel in TGEMM is supported so that the additional overhead will be incurred when performing on tall-and-skinny and small matrices by implicitly padding. For example, when \( N \) is smaller than \( n_a \), TGEMM still stores \( B_a \) in AM as a \( k_g \times n_a \) matrix so that the memory space of AM is wasted. Then, the maximum value of \( k_g \) will be limited, and the number of DMA operations for loading \( B \) into AM will be greatly increased. It also maybe introduces additional broadcast at most two FP32 scalars to two vectors per cycle bandwidth between SPU and VPU. In FT-m7032, SPU can parallelism, scalar and vector registers, and the broadcasting are wasted. Then, the maximum value of \( m \) and shapes of matrices, and the micro-kernels based on the strategy should be dynamically adjusted according to the sizes micro-kernels by automatic generation, where \( B \) and the number of DMA operations for loading \( B \) into AM can be improved.

Secondly, only the multi-core parallelization based on the \( N \) dimension is adopted in TGEMM so that it can not efficiently utilize multiple DSP cores when performing on irregular-shaped matrices where \( N \) is small. In order to take full advantage of all DSP cores in a GPDSP cluster, various parallelization strategies matched with the special shapes of matrices need to be introduced.

Finally, how to choose the optimal block sizes and parallelization strategy is a challenge when different micro-kernels and parallelization strategies can be available. In other words, in order to improve the efficiency of irregular-shaped GEMMs, the block sizes \( (m_g, k_g, n_a \text{ and } m_s, \text{ etc.}) \) and parallelization strategy should be dynamically adjusted according to the sizes and shapes of matrices, and the micro-kernels based on the dynamic block sizes \( (m_s \text{ and } n_a) \) are then auto-generated and called.

IV. DESIGN OF ftIMM

To efficiently handle three types of irregular-shaped matrix-matrix multiplications on multi-core DSPs described in Section III-A, this section proposes an efficient implementation: ftIMM. First, an automatic generation scheme of various assembly micro-kernels are designed to support matrices of various shapes in irregular-shaped GEMMs. Then we design the multi-core algorithm of irregular-shaped GEMMs with two parallelization strategies. Due to the special shapes of matrices in irregular-shaped GEMMs, we dynamically adjust the parallelization strategy and block sizes to make full use of multiple cores and reduce additional overhead.

A. Micro-Kernel Design and Generation

1) Design Principals: Our micro-kernel implementation aims to utilize three FMAC units in VPEs efficiently and minimize the cost of on-chip memory access (SM and AM). We achieve the target by making full use of the instruction-level parallelism, scalar and vector registers, and the broadcasting bandwidth between SPU and VPU. In FT-m7032, SPU can broadcast at most two FP32 scalars to two vectors per cycle owing to the instruction conflicts. VPU can load up to 128 FP32 data into 4 vector registers per cycle and perform up to three fused multiply-add operations of vectors per cycle. As a result, the bandwidth between VPEs and AM and the computation ability can meet the needs for the irregular-shaped GEMMs with \( N \leq 96 \), while the broadcasting bandwidth between SPU and VPU is likely to become a bottleneck of performance. It is very important to improve the parallelism of broadcast operations in the design and auto-generation of micro-kernels.

Based on the principals above, the general implementation of micro-kernels in ftIMM is proposed, shown in Algorithm 3. Compared with micro-kernels in TGEMM, there are three main differences. The first one is that ftIMM adds two loops (indexed by \( mu \) and \( ku \)) by loop tiling, which will be unrolled in the assembly implementation. The tiling sizes \( (m_u \text{ and } k_u) \) rely on how to make full use of three FMAC units in parallel and hide their latency, explained in Section IV-A2. The second one is that there is a reduction operation (Lines 12 - 13) in ftIMM when the tiling size \( k_u \) is greater than 1. The last one is that the loading operations are carried out according to the size of \( n_a \) by VPU so that the implicitly padding in TGEMM are no longer required and the space utilization efficiency of AM can be improved.

\[
\text{Algorithm 3: The Implementation of Micro-Kernel in ftIMM}
\]

\[
\begin{align*}
\text{input: } & A_s[m_s][k_a], B_a[k_a][n_a] \\
\text{output: } & C_a[m_s][n_a] \\
1 & \text{Set } V = 32, v_n = (n_a + V - 1)/V \\
2 & \text{for } mm = 0 : m_u : m_s \text{ do} \\
3 & \quad \text{VPU inits } V_{c,0,k_u,0,m_u,0,v_n} \text{ to zero} \\
4 & \quad \text{for } kk = 0 : k_u : k_a \text{ do} \\
5 & \quad \quad \text{for } mu = 0 : 1 : m_u \text{ do} \\
6 & \quad \quad \quad \text{for } ku = 0 : 1 : k_u \text{ do} \\
7 & \quad \quad \quad \quad \text{SPU loads } A_{s,mm+mu,ku,kk} \text{ to scalar register } R_{mu,ku} \\
8 & \quad \quad \quad \quad \text{SPU broadcasts } R_{mu,ku} \text{ to vector register } V_{a,mm,ku} \\
9 & \quad \quad \quad \quad \text{for } nn = 0 : 1 : v_n \text{ do} \\
10 & \quad \quad \quad \quad \text{VPU loads } B_a,ku,kk,nn \times V_{a,mm+1,kk,nn} \text{ to vector register } V_{b,ku,nn} \\
11 & \quad \quad \quad \quad \text{V}_{c,ku,mu,nn} = V_{a,mm,ku} \times V_{b,ku,nn} \\
12 & \quad \quad \quad \quad \text{for } ku = 1 : 1 : k_u \text{ do} \\
13 & \quad \quad \quad \quad \quad V_{c,0,m_u,0,v_n} = V_{c,ku,0,m_u,0,v_n} \\
14 & \quad \quad \quad \quad \text{VPU store } V_{c,0,m_u,0,v_n} \text{ back to } C_{a,m}[m_u][n_a].
\end{align*}
\]
The first is the case where $64 < n_a \leq 96$. As the same in TGGEMM, the parallelism in $n_a$ is mapped into three FMAC units in 16 VPEs. We use different schemes to hide latency of the FMAC units according to $m_a$. For the micro-kernel where $m_a$ is greater than the latency of FMAC instructions ($t_{fma}$), the tiling size $k_a$ is set to 1, and the $m_a$ can be as large as possible to hide the latency under the limitation of the total number of registers. For the micro-kernel where $m_a < t_{fma}$, $m_a$ is set to $n_a$ and $k_a$ is set to greater than 1 for hiding the latency $t_{fma}$.

The second is the case where $0 < n_a \leq 64$. For the case, the parallelism in $n_a$ is not sufficient for three FMAC units in 16 VPEs. In order to improve the utilization of FMAC units per cycle, the tiling size $k_a$ should be set to be greater than 1. At the same time, $m_a$ is also set to be as large as possible for hiding the latency of FMAC units. The generated assembly pipelines for the micro-kernels with different $m_a \geq t_{fma}$ based on the current instruction sets is shown in Table I, in which $t_{VLDMW}$ and $t_{SSR}$ represent the latency of the vector data loading instruction (i.e., VLDMW and VLDDW) and the jump instruction (i.e., SSR) respectively. All three FMAC units are filled, and all the operations are pipelined, such as scalar data loading (i.e., SLDH and SLDW), scalar data extending (i.e., SFEXT32L and SBALE2H), broadcasting (i.e., SVBCAST and SVBCAST2), vector data loading and fused multiply-add instructions (i.e., VFMULAS32).

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The second is the case where $0 < n_a \leq 64$. For the case, the parallelism in $n_a$ is not sufficient for three FMAC units in 16 VPEs. In order to improve the utilization of FMAC units per cycle, the tiling size $k_a$ should be set to be greater than 1. At the same time, $m_a$ is also set to be as large as possible for hiding the latency of FMAC units. The generated assembly pipelines for the micro-kernels with different $m_a \geq t_{fma}$ based on the current instruction sets is shown in Table I, in which $t_{VLDMW}$ and $t_{SSR}$ represent the latency of the vector data loading instruction (i.e., VLDMW and VLDDW) and the jump instruction (i.e., SSR) respectively. All three FMAC units are filled, and all the operations are pipelined, such as scalar data loading (i.e., SLDH and SLDW), scalar data extending (i.e., SFEXT32L and SBALE2H), broadcasting (i.e., SVBCAST and SVBCAST2), vector data loading and fused multiply-add instructions (i.e., VFMULAS32).

### Algorithm 4: Irregular-Shaped GEMM Implementation with Parallelization on M Dimension

**input**: $A[M][K]$, $B[K][N]$

**output**: $C[M][N]$

1. for $i = 0$: $n_g$: $N$ do
   2. for $j = 0$: $k_g$: $K$ do
      // Ping-pong
      3. $\text{DMA}(B_{ji}[k_g][n_g] \rightarrow B_{ij}[k_g][n_a])$
      4. for $t = 0$: $m_a$: $M$ do in parallel
         5. for $ii = 0$: $n_a$: $n_g$ do
            // Ping-pong
            6. $\text{DMA}(C_{i+ii}[m_a][n_a] \rightarrow C_{a}[m_a][n_a])$
            7. for $jj = 0$: $k_g$: $k_g$ do
               // Ping-pong
               8. $\text{DMA}(B_{gjj}[k_3][n_a] \rightarrow B_{a}[k_3][n_a])$
               9. for $tt = 0$: $m_a$: $m_a$ do
                  // Ping-pong
                  10. $\text{DMA}(A_{gtt+j+j}[m_a][k_3] \rightarrow A_{a}[m_a][k_3])$
                  $C_{a}[m_a][n_a] = A_{a}[m_a][k_3] \times B_{a}[k_3][n_a]$
                  11. $\text{DMA}(C_{a}[m_a][n_a] \rightarrow C_{i+ii}[m_a][n_a])$

2. Parallelization on K Dimension: The multi-core parallelization strategy based on $K$ dimension is shown in the Algorithm 5. Similar to the $M$-dimension-based parallelization strategy, this strategy uses a two-level DMA-based ping-pong scheme to implement matrix-matrix multiplication. First, in the $K$ dimension, based on the ping-pong method, perform the multiplication of the $m_a \times k_a$ sub-matrix of $A$ and the $k_a \times n_a$ sub-matrix of $B$. Based on ping-pong in the $M$ dimension, perform the multiplication of the $m_s \times k_s$ sub-matrix of $A$ and the $k_s \times n_s$ sub-matrix of $B$. We parallelize the loop of $K$ dimension and use GSM to cache the sub-matrix of $C$, and perform the reduction between multiple DSP cores based on GSM, which can effectively realize data reuse and reduce the memory access overhead caused by reduction. Besides, because the parallelization strategy based on $K$ dimension brings additional overhead of reduction, this strategy is suitable for the multiplication of irregular-shaped GEMM with both small sizes of $M$ and $N$ dimensions, and therefore we do not utilize ping-pong in the outermost loop.
C. Dynamic Adjusting

In the traditional implementation of GEMMs on multi-core DSPs, the block sizes are designed according to the hardware constraints and CMR, and both the block sizes and the parallelization strategy are fixed whatever the shapes of matrices are. For large-scale regular-shaped GEMMs, the method in TGEMM works well. But for irregular-shaped GEMMs, due to special shapes, fixed parallelization strategy with fixed block sizes cannot make full use of the computation ability, and too large block sizes bring additional computation and space overhead, so the parallelization strategy and block sizes need to be adjusted dynamically according to the shape of matrices.

First, we design the initial block sizes according to the hardware constraints and CMR. In the parallelization strategy based on the $M$ dimension, the following two types of data transfer between multi-level memories are considered, and the corresponding CMR is calculated.

1. The $k_g \times n_g$ sub-matrix of matrix $B$ is cached in GSM, the $m_a \times k_g$ sub-matrix of matrix $A$ is transferred between DDR and SM, and the $m_a \times n_g$ sub-matrix of matrix $C$ is transferred between DDR and AM. The CMR is shown in Eq. 1.

$$f_1 = \frac{2 \times m_a \times k_g \times n_g \times num_{core}}{num_{core} \times m_a \times (k_g + 2 \times n_g) + k_g \times n_g}$$ (1)

2. The $k_a \times n_a$ sub-matrix of matrix $B$ and $m_a \times n_a$ sub-matrix of matrix $C$ have been loaded to the AM, and the $m_a \times k_a$ sub-matrix of matrix $A$ is transferred between DDR and SM. The CMR is shown in Eq. 2.

$$f_2 = \frac{2 \times m_a \times k_a \times n_a \times num_{core}}{num_{core} \times m_a \times (k_a + 2 \times n_a) + k_a \times n_a}$$ (2)

Besides, when we design initial block sizes and adjust block sizes dynamically, we ensure the block size $k_g$ to be larger as much as possible because larger $k_g$ improves the reuse of the sub-matrix $C_g$ in AM which is loaded in line 6 of Algorithm 4. Considering the space limit of GSM, SM and AM, to maximize the CMR, we can obtain the initial optimal block sizes for single-precision floating-point GEMM. The block sizes are that $k_g = 5888$, $n_g = 96$, $m_a = 320$, $n_a = 96$, $k_a = 864$ and $m_a = 8$.  

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**TABLE I**

| Cycle | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|-------|---|---|---|---|---|---|---|---|
| Scalar Load&Store1 | SLDW | SLDW | SLDW | SLDW | SLDW | SLDW | SLDW | SLDW |
| Scalar MAC1 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 |
| SIEU | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 |
| Control unit | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 |

**TABLE II**

| Cycle | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|-------|---|---|---|---|---|---|---|---|
| Scalar Load&Store1 | SLDW | SLDW | SLDW | SLDW | SLDW | SLDW | SLDW | SLDW |
| Scalar MAC1 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 |
| SIEU | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 |
| Control unit | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 |

**TABLE III**

| Cycle | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|-------|---|---|---|---|---|---|---|---|
| Scalar Load&Store1 | SLDW | SLDW | SLDW | SLDW | SLDW | SLDW | SLDW | SLDW |
| Scalar MAC1 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 |
| SIEU | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 |
| Control unit | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 | VFMULAS32 |
Algorithm 5: Irregular-Shaped GEMM Implementation with Parallelization on K Dimension

**input**: Matrix $A[M][N]$, $B[K][M]$

**output**: Matrix $C[N][K]$

1. for $i = 0$: $m_g = M$
2. for $j = 0$: $n_g = N$
3. DMA($C_{ij}A[m_g][n_g] ightarrow C_g[m_g][n_g]$)
4. for $ii = 0$: $m_g = m_g$
5. for $jj = 0$: $n_g = n_g$
6. Init sub-matrix $C_a[m_a][n_a]$ to zero
7. for $t = 0$: $k_a = K$
8. // Ping-pong
9. DMA($B_{ij}A[t][k_a][n_a] ightarrow B_a[k_a][n_a]$)
10. for $u = 0$: $m_s = m_s$
11. // Ping-pong
12. DMA($A_{i+u}t[k_s][n_a] ightarrow\)
13. $A_{a}[m_a][n_a] + = A_{a}[m_a][k_a] \times B_{a}[k_a][n_a]$
14. Reduce sub-matrix $A_{a}[m_a][n_a]$ among multiple cores based on GSM, and store the reduction result back into $C_{i+i+j}[m_a][n_a]$

Similar to the parallelization based on the $M$ dimension, the initial block sizes of the parallelization based on the $K$ dimension can be obtained through CMR and hardware constraints. The CMR are shown in Eq. 3 and 4. The result is that $m_g = 1024, n_g = 512, m_a = 1024, n_a = 96, k_a = 512$ and $m_s = 14$.

$$f_3 = \frac{2 \times m_g \times k_a \times n_g \times num_{core}}{num_{core} \times k_a \times (m_g + n_g) + 2 \times m_g \times n_g} \quad (3)$$

$$f_4 = \frac{2 \times m_a \times k_a \times n_a \times num_{core}}{num_{core} \times k_a \times (m_a + n_a) + 2 \times m_a \times n_a} \quad (4)$$

After determining the initial block sizes, at runtime, ftIMM dynamically adjusts the parallelization strategy and block sizes based on the matrices sizes. For cases of multiplication between a tall-and-skinny matrix and a small matrix or multiplication between a large regular matrix and a tall-and-skinny matrix, in which $N \leq n_a$ and $M$ is large sufficiently, the parallelization strategy based on $M$ dimension is adopted. For the case of multiplication between a skinny-and-tall matrix and a tall-and-skinny matrix, in which $N \leq n_a$, $M$ is small enough and $K$ is large sufficiently, ftIMM chooses the parallelization strategy based on $K$ dimension which can utilize all cores in this case. Then the block sizes are adjusted based on the sizes of matrices and initial block sizes. For the case where the sizes are significantly smaller than the block sizes, ftIMM adjusts the block sizes to adapt to sizes of matrices, and increases the block size in the dimension selected for parallelization, to reduce additional computation and space overhead, and minimize memory access latency. Because micro-kernels with too small $m_s$ give lower performance than others, especially when $m_s \leq 6$, ftIMM ensures that $m_s \geq 6$ if $M$ is large enough during the adjusting of block sizes.

V. EXPERIMENT

A. Micro-Kernel Performance

We evaluate performance of auto-generated micro-kernels with single-precision workloads on two cases which are commonly used in the three types of irregular-shaped GEMMs. The first case is that $K$ is large sufficiently (i.e., $K = 512$) and micro-kernels of this case are used in the multiplication between a skinny-and-tall matrix and a tall-and-skinny matrix and the multiplication between a large regular matrix and a tall-and-skinny matrix. The second case is that $K$ is small enough (i.e., $K = 32$) which is used in the multiplication between a tall-and-skinny matrix and a small matrix. Because the size of $M$ is limited by the hardware constraints and the specific implementation of micro-kernels, the size of $M$ is different among the experiment of the two types of micro-kernels.

We first evaluate the performance of auto-generated micro-kernels where the size of $K$ is fixed at 512. The results are shown in Fig. 3(a), (b) and (c) in which $N = 96, 64, 32$ respectively. In these cases, the auto-generated micro-kernels achieve great performance. The highest is close to the theoretical upper bound, and the corresponding efficiency is up to 98.2%, 96.4% and 63.0% respectively. In Fig. 3(b), micro-kernels with $M = 8, 10$ give lower performance than the micro-kernel with $M = 6$ and the micro-kernel with $M = 14$ gives lower performance than the micro-kernel with $M = 12$. This is mainly because in the implementations for micro-kernels in which $32 < N \leq 64$, there are not enough parallel FMAC operations to fill up the pipelines of FMAC units if $M \mod 3 \neq 0$ and therefore micro-kernels with $M \mod 3 \neq 0$ give lower performance.

We also evaluate the performance of the micro-kernels in which the size of $K$ is small and the results are shown in Fig. 3(d), (e) and (f). The efficiency of cases in which $N = 96$ and $K = 32$ is up to 77.4% which is high enough though $K$ is too small. Besides, the efficiency for cases in which $N = 64$ and $N = 32$ can reach up to 65.4% and 46.6% which are close to or higher than the upper bound efficiency of micro-kernels in TGEMM respectively.

B. Single-Core Performance

The performance of ftIMM is first evaluated by performing three types of irregular-shaped GEMMs on single DSP core. The results are shown in Fig. 4. In all cases, ftIMM outperforms the traditional implementation TGEMM. For example, when $M \times N \times K = 20480 \times 32 \times 20480$, ftIMM gives 2.0× higher performance than TGEMM. The improvement is especially obvious for the case in which the size of $N$ dimension is much lower because of the optimized micro-kernels and dynamic adjusting. Specially, in (b) and (c), ftIMM gives lower performance in the case where $N = 80$ than in
the case where \( N = 64 \). This is because in the case where \( N = 80 \), block sizes, \( m_a, k_g \) and so on, are smaller than those in the case where \( N = 64 \) and the performance is affected by block sizes.

### C. Multi-core Performance

We also evaluate \( \text{ftIMM} \) by applying it to the three types of irregular-shaped GEMMs using multiple cores of a GPDSP cluster on FT-m7032. Inputs and outputs are both single-precision matrices. The results are shown in Fig. 5.

1) **Multiplication between a tall-and-skinny matrix and a small matrix:** Fig. 5(a) and (d) show the results on multiplication between a tall-and-skinny matrix and a small matrix on a GPDSP cluster. In Fig. 5(a), the size of the \( M \) dimension is set to \( 2^{16} \) which is large sufficiently. \( \text{ftIMM} \) achieves higher performance than \( \text{TGEMM} \), yielding up to \( 4.2 \times \) performance improvement. The performance improvement is due to the parallelization strategy which takes full advantage of multiple cores, the optimized micro-kernels and dynamic adjusting. \( \text{ftIMM} \) also demonstrates higher performance benefit for smaller \( N \) and \( K \) sizes. This is largely due to the optimized micro-kernels and dynamic adjusting. The maximum performance of \( \text{ftIMM} \) obtained with the roofline model is also shown in Fig. 5. \( \text{ftIMM} \) delivers up to 67.0\% of the maximum performance in the results. Because the performance of \( \text{ftIMM} \) on multiple cores is limited by the bandwidth and the actual bandwidth cannot reach the theoretical bandwidth which is used in the computation of roofline model, \( \text{ftIMM} \) cannot deliver maximum performance.

In Fig. 5(d), the sizes of \( K \) and \( N \) dimensions are set to 32. We can observe that the performance benefit tends to be more significant for larger size of the \( M \) dimension. For example, for GEMMs with \( M = 2^{22} \), \( \text{ftIMM} \) gives higher improvement than GEMMs with \( M = 2^{16} \). This is mainly because larger size of the \( M \) dimension makes it easier for \( \text{ftIMM} \) to improve the reuse of data and to deliver higher performance.

2) **Multiplication between a skinny-and-tall matrix and a tall-and-skinny matrix:** Fig. 5(b) and (e) show the performance on the multiplication between a skinny-and-tall matrix and a tall-and-skinny matrix on a GPDSP cluster. In Fig. 5(b), the size of \( K \) dimension is set to \( 2^{16} \). In Fig. 5(e), the sizes of \( M \) and \( N \) dimensions are set to 32. The results demonstrate that for these cases, \( \text{ftIMM} \) delivers up to \( 5.8 \times \) higher performance than \( \text{TGEMM} \). Though the parallelization strategy chosen in these cases brings additional overhead of reduction, \( \text{ftIMM} \) can take full advantages of multiple cores especially when \( M \) and \( N \) are much smaller than \( K \). We also observe that, because too small sizes of \( M \) and \( N \) dimensions cannot make full use of the computation ability and bandwidth, the performance is higher along with larger sizes of \( M \) and \( N \) dimensions.

3) **Multiplication between a large regular matrix and a tall-and-skinny matrix:** Fig. 5(c) and (f) show the results of the multiplication between a large regular matrix and a tall-and-skinny matrix on a GPDSP cluster. In Fig. 5(c), the sizes of the \( M \) and \( K \) dimensions are set to \( 20480 \). As can be seen from the results, \( \text{ftIMM} \) gives higher performance on this case, yielding up to \( 7.2 \times \) performance improvement. In Fig. 5(f), the size of the \( N \) dimension is set to 32. It is can be seen from the results that \( \text{ftIMM} \) and \( \text{TGEMM} \) both achieve higher performance in the computation of the third type of irregular-shaped GEMMs than the other types. It is because in the third type of irregular-shaped GEMMs, the micro-kernel can achieve higher performance with larger size of \( K \) dimension than others and additional overhead can be amortized more sufficiently. For cases in which \( M = K = 16384 \) or \( M = K = 20480 \), \( \text{ftIMM} \) gives lower performance than other
cases. This is because computation ability of used cores cannot be utilized sufficiently under the sizes of matrices and the corresponding block sizes.

4) Scalability: Fig. 6 shows the scalability of fitIMM on performing the three types of irregular-shaped GEMMs of $M \times N \times K = 2^{20} \times 32 \times 32$, $32 \times 32 \times 2^{20}$, and $20480 \times 32 \times 20480$. The vertical axis represents the speedup of fitIMM on multiple cores of a GPDSP cluster compared with on the single DSP core. It can be seen from the results that the performance of fitIMM increases with the number of DSP cores, while the scaling efficiency is not high. This is mainly because the algorithm is memory intensive and the performance is limited by the bandwidth when more DSP cores are used. Besides, among the three types of irregular-shaped GEMMs, for the case $M \times N \times K = 20480 \times 32 \times 20480$, the scalability of the proposed algorithm is worse than other cases. This is because the parallelization strategy based on K dimension is chosen for this case and the overhead of reduction among multiple cores increases with the increase of the number of cores.

D. Performance of Irregular-shaped GEMMs on CPU and GPDSP Cluster of FT-m7032

Though the open-source library LibShalom is optimized for irregular-shaped GEMMs on ARMv8 CPU, the available
version can not work on the case of $C = A \times B$. Therefore we compare the performance of ftIMM on a GPDSP cluster of FT-m7032 with the OpenBLAS-0.3.20, which is highly optimized for GEMM, on the 16-core ARMv8 CPU of FT-m7032 based on the same bandwidth. We evaluate the performance on the three types of irregular-shaped GEMMs and the results are shown in Fig. 7. We can observe that ftIMM delivers higher efficiency, which is the ratio of the achieved performance to the corresponding peak performance, on a GPDSP cluster than OpenBLAS on the multi-core CPU of FT-m7032 in most cases, yielding up to $3.1 \times$ improvement.

VI. CONCLUSION

We propose ftIMM, an efficient implementation for irregular-shaped matrix-matrix multiplication on multi-core DSPs of FT-m7032. We present an auto-generation scheme for building kernels of different sizes. Besides, we design the multi-core algorithm for irregular-shaped GEMMs with two parallelization strategies and the dynamic adjusting function. We evaluate ftIMM by applying it to irregular-shaped GEMMs on multi-core DSPs of FT-m7032 and compare it with the traditional implementation, which shows that ftIMM achieves higher performance for irregular-shaped GEMMs.

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