The growing interest for neuromorphic computing applications is driving a fundamental shift toward memory-centric computer architectures, enabling efficient machine learning and analysis of large data sets. Oxygen vacancy resistive random access memory (RRAM) is seen as a promising candidate for large capacity, nonvolatile memory technologies. This paper explores the potential of RRAM cells in cointegration with field-effect-transistor (MOSFET) selectors and nonvolatile resistive random access memory (RRAM) cells for future integration of a VNW-FET selector on the same nanowire, and we show improved RRAM performance when using an InAs VNW-FET selector.

Utilization of movement of oxygen vacancies in metallic oxides has accumulated a large interest, in part due to the simplistic material stack, and in part due to the demonstrated performance with energy efficient and high endurance switching up to 10^{12} cycles. The formation of an oxygen vacancy filament is accomplished by applying a large positive bias, $V_{\text{FORM}}$, on the top electrode (TE). For bipolar RRAM operation, the resistance is modulated by bipolar switching voltages, $V_{\text{RESET}}$ and $V_{\text{STOP}}$. For a successful switching cycle, the $V_{\text{RESET}}$ and $V_{\text{STOP}}$ occur below $V_{\text{STOP}}$. Changing the filament back and forth switches the cell between a low resistance state ($R_{\text{LRS}}$) and a high resistance state ($R_{\text{HRS}}$). This paper investigates bipolar oxygen vacancy RRAM cells consisting of a resistive switching interface of indium-tin-oxide (ITO) and hafnium-dioxide (HfO2) integrated on arrays of InAs VNWs. From an RRAM perspective, HfO2 is attractive in that it does not have any stable insulating substoichiometric oxides, which could interfere with the conservation of the number of vacancies.
during resistive switching,[11] and endurance values up to \(10^6\) have been demonstrated.[12] indium-tin-oxide-hafnium-dioxide (ITO-HfO\(_2\))-based RRAM shows low switching voltages, where material stacks of titanium-nitride (TiN)/HfO\(_2\)/ITO have been reported with bipolar resistive switching at below \(\pm 0.6\) V,[13,14] lower than what is reported for other typical stacks, for instance TiN/HfO\(_2\)/Ti/TiN.[15,16] A unique property of ITO-based RRAM is that it imposes a self-current-compliance due to the formation of a local Schottky barrier at the interface with the vacancy filament.[17] The barrier is likely formed due to the interstitial oxygen that is absorbed into the ITO is being complexed with the Sn, changing the Sn compensation from electronic to oxygen interstitial.[18] The barrier formation occurs during the SET process where the ruptured filament tip is reformed and oxygen is pushed into the TE. When increasing the positive \(V_{\text{STOP}}\), the oxygen interstitials go deeper into the ITO, and thus, \(V_{\text{RESET}}\) becomes more negative due to additional work of reversing the oxygen displacement.[17] The Schottky barrier allows for selector-less operation, but as we demonstrate, for low current switching, the distribution of switching voltages, as well as the resistive states, show a significantly larger spread without a selector.

For low power operation of large-scale RRAM arrays, an efficient selector is integral to reduce sneak path leakage and suppress degradation of the read and write pulses. MOSFET selectors offer precise control of the current compliance and support large current ON/OFF-ratios, high endurance, and bipolar conduction. Alternatively, self-rectifying diode selectors also offer large current ON/OFF ratios, and compared to MOSFETs, can be implemented with a low-complexity structure, however, with the drawbacks of unipolar conduction and relatively large voltage operation.[3,6] We incorporate InAs VNWs as VNW-FETs to offer the capability of driving RRAM cells at a large range of current levels while ensuring a minimal voltage drop over the selector. Nonetheless, our process technology is transferable, for example, to Si nanowires.[10–21] The VNW-RRAM cells are fabricated on a Si-substrate using NWs with a \(d_{\text{NW}}\) after the epitaxial growth of about 30 nm.[22] The subsequent RRAM fabrication process scheme is made fully compatible with the vertical gate-last process used for high performance MOSFETs, and in order to reduce the fabrication complexity, we demonstrate how the NW drain contact metal protector that is capped with TiN, used in the fabrication of asymmetrically etched high performance VNW-FETs, could consecutively be used as the RRAM BE.[23] In Figure 1a,b, scanning electron microscopy (SEM) images of the layout of a fabricated 4 × 4 cross-point array consisting of VNW-RRAM are shown. A cross-sectional SEM of an individual VNW-RRAM is shown in Figure 1c, where the TiN BE and the ITO TE are visible. The finalized VNW-RRAM area corresponds to 0.06 µm\(^2\) for a 400 nm vertical RRAM segment. The different fabrication steps are listed in Figure 1d, also showing illustrations of the VNW array after growth and after the two different metallization steps, respectively.

To evaluate the VNW-RRAM process yield, a complete 4 × 4 array is characterized electrically and the measured results are shown in Figure 2a, where a minimal and a median memory window of 21x and 107x are characterized, respectively, for all of the 16 RRAM cells in the same array for a \(V_{\text{STOP}}\) of \(\pm 1.5\) V. Without a selector, the \(R_{\text{LRS}}\) is determined by a combination of the current compliance imposed by the parameter analyzer, set at 10 µA during forming, and the self-current-compliance of the ITO-HfO\(_2\) interface.[24] To study the effect of instead having a selector imposing compliance, individual VNW-RRAM cells are characterized without (1R) and with a VNW-FET selector connected in series externally (ITISR). Distributions of \(V_{\text{SET}}\) and \(V_{\text{RESET}}\), and \(R_{\text{LRS}}\) and \(R_{\text{HRS}}\), for 100 switches are shown in Figure 2b,c, respectively, for both 1R and ITISR. With ITISR, it is possible to achieve a significantly smaller spread of both the \(R_{\text{LRS}}\) and \(R_{\text{HRS}}\) distributions. The distributions of the switching voltages also show significantly higher uniformity. For a 95% confidence interval, the SET and RESET occur below 0.6 V and above \(\sim 1.6\) V, respectively, for 1R, and below 0.4 V and above

![Figure 1](image-url)  
Figure 1. a,b) SEM image of the fabricated 4 × 4 cross-point nanowire array. The different top and bottom electrodes in the layout, TE and BE, respectively, are indexed 1–4. c) Cross-sectional SEM of a fabricated vertical nanowire RRAM with TiN BE and ITO TE. d) A process flow and illustrations of the different cross-point nanowire RRAM array fabrication steps.
−0.8 V, respectively, for IT1R. The median switching voltages and the largest determined switching voltages for the 1T1R configuration are 0.27/−0.27 V and 0.59/−0.93 V, respectively, for SET/RESET. For an RRAM cell measured in 1T1R configuration, 10 consecutive DC sweep cycles are shown in Figure 2d, and the resistance levels of 100 consecutive cycles are shown in Figure 2e, demonstrating the small switching voltages and consistent resistive states, respectively. To test the retention properties, a VNW-RRAM cell is demonstrated to hold both its high and its low resistive state for 10⁴ s at 125 °C, where the measurement is shown in Figure 2f. This is more than sufficient for nonvolatile storage, since holding its memory state for 10⁴ s at 85 °C corresponds to 10 years at room temperature.

To determine the feasibility of a full VNW-IT1R integration, the effect of the filament forming on the integrity of the selector device must be considered as well. The VNW-FETs will degrade if a too high bias (>1.5 V) is applied, and as such it is vital that the filament forming can be done at a sufficiently low applied voltage. Figure 3a shows the V_FORM scaling trend for a planar reference structure, via-hole RRAM cells, with the same material stack as for the VNW-RRAM.[25] At an average of 3.3 V, the V_FORM for the VNW-RRAM cells is found to be higher than for the Via-RRAM with the same oxide thickness, which can be expected as the area difference is about 100x.[16]

To test the impact on the VNW-FET of the forming procedure, a 45 nm in diameter, single nanowire VNW-FET selector, with a channel length (L_C) of 150–200 nm, is characterized before and after the forming procedure. The transfer and the output characteristics of the selector is shown before and after forming in Figure 3b,c, respectively. Even for a 4 V applied voltage pulse, no significant degradation is observed as the VNW-FET is only exposed to about 1.3 V due to voltage division between the forming RRAM and the selector. Noticeably, the lower conductance in saturation, as compared to the ON-resistance (R_ON) for low voltages, will reduce the voltage drop over the selector. However, to further improve the margin for the required high voltage tolerance of the transistor, it is possible to change the composition of the nanowire on the drain side to InGaAs, where VNW-FETs withstanding a drain–source voltage (V_DSS) of 1.5 V at multiple gate-source voltage (V_GS) points without degradation are demonstrated for a d_NW of 28 nm.[26] According to the oxide thickness trend in Figure 3a, scaling the switching oxide would also reduce the required voltage during forming. To maintain an achievable 100x R_HRS/R_LRS-ratio, it can be estimated that a 1.7 nm HfO_2 thickness is needed.[16] Reducing the RRAM cell area would allow for even further oxide scaling as the oxide leakage, and thus the highest achievable R_HRS, is proportional to the area.
The endurance of VNW-RRAM cells with VNW-FET selectors are measured using symmetrical 3 ms negative and positive triangle pulses, where the determined $V_{\text{SET}}$ as a function of the maximum pulse height, $V_{\text{STOP}}$, is plotted in Figure 3e. The relatively long pulses that we use are necessary in our present 1T1R measurement configuration as the VNW-FET selector is connected to the VNW-RRAM externally and probed separately, thus imposing a large capacitive load that limits the minimum undistorted pulse length in the circuit. As with the $V_{\text{RESET}} - V_{\text{STOP}}$ dependence,[17] explained by oxygen ions being transported deeper into the ITO during switching with larger applied voltages, we observe that the opposite trend is also true, that for a larger $V_{\text{STOP}}$ with negative TE polarity, the SET will occur at a larger voltage with positive TE polarity. The explanation is likely similar, that a larger negative $V_{\text{STOP}}$ will cause a larger displacement of the oxygen vacancies from the ruptured segment within the switching oxide, requiring a larger positive voltage to reverse. At current levels compatible with scaled integration (below 70 $\mu$A for an InAs VNW-FET with a $d_{\text{NW}}$ of 27 nm),[27] it is difficult to find stable switching voltages without a selector, and a soft failure typically occurs after a few hundred switches where the filament has to be SET or RESET with a larger voltage to be able to continue. For the endurance measurement, a 1T1R configuration with a $V_{\text{STOP}} = \pm 1.5$ V is chosen and the result of $10^6$ switches is shown in Figure 3f. It can be observed that the $R_{\text{HRS}}$ is somewhat degraded after $10^5$ pulses, however, at $10^6$, the $R_{\text{LRS}}/R_{\text{HRS}}$-ratio is still about 50x. Switching cycles with READ pulses after 100 and $10^6$ switches, respectively, are shown in Figure S1 in the Supporting Information. The volume of studies of HfO$_2$-ITO-RRAM-stacks are limited but demonstrate up to $10^8$ switching cycles, using down to 20 ns pulses, without the use of a selector but operated at about one or two orders of magnitude lower $R_{\text{LRS}}$ than what was used in our endurance measurements.[14,27] Operating at several hundreds of $\mu$A is, however, not compatible with scaled down selectors. Studies of selector-less ITO-HfO$_2$ RRAM with $R_{\text{LRS}}$ values similar to what was used for our endurance measurement have instead added dopants into the ITO in order to enhance the Schottky barrier formation and thus better constrict the conduction. The ITO studies with either Gd or Er dopants show endurances up to $10^6$ and $10^7$, receptively.[13,28] For a hybrid Static RAM (SRAM) and RRAM array integration, a minimum RRAM endurance of $10^5$ could be sufficient for up to 10 years of continuously running deep learning applications.[4]

For characterization of VNW-RRAM cells without a selector, shorter pulse widths are possible as the 1R configuration is not
limited by parasitic capacitances from the measurement setup. In Figure 4a, 5 consecutive switching cycles with ±1.0 V, 50 ns SET and RESET pulses are plotted on top of each other, and in Figure 4b, 5 consecutive SET pulses are shown. The increased width of the measured current pulse as compared to the applied voltage pulse is due to a 25 pF sampling capacitance of the parameter analyzer. Using the measured data it is possible to calculate the write energy. For 1 ms, 500 ns, and 50 ns pulses, the average SET energies for 5 consecutive pulses of each correspond to 1847, 24, and 0.49 pJ, respectively. The corresponding average RESET energies are 182, 1.1, and 0.11 pJ, respectively. SET pulses for 1 ms and 50 ns are shown in Figure S2 (Supporting Information). As the pulse width is reduced down to 50 ns, the current overshoot is reduced along with the consumed power. The average switching power for 50 ns pulses corresponds to 10 and 2 µW for the SET ($P_{SET}$) and RESET ($P_{RESET}$), respectively. The $P_{RESET}$ is lower than the $P_{SET}$ as once the RESET occurs, it will go into the $R_{HRS}$ and limit the conduction. The lower $P_{RESET}$ indicates that the $P_{SET}$ includes a current overshoot that could potentially be reduced with a shorter pulse, or by having a selector that limits the current. The SET energies are plotted versus the write time in Figure 4c, where they are benchmarked against other state-of-the-art resistive switching memory technologies.[8] We also include the best published ITO RRAM devices. From the benchmark we conclude that our technology is well positioned for future implementations of ultralow power cross-point memory arrays.

This paper presents a detailed evaluation of a vertical nanowire RRAM technology for high density, low power cross-point memory arrays compatible with high performance vertical nanowire transistor selectors. The vertical structure allows for cointegration of selector and RRAM, where a decoupling of the vertical dimension and the area footprint adds another degree of design optimization without impacting the integration area efficiency. The fabricated 0.06 µm² VNW-RRAM cells has an ultralow switching power of 10 µW that combined with a vertical implementation promises future dense and energy-efficient memory integration.

Supporting Information
Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest
The authors declare no conflict of interest.

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