Excellent potential of photo-electrochemical etching for fabricating high-aspect-ratio deep trenches in gallium nitride

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Received July 5, 2018; accepted July 27, 2018; published online August 10, 2018

Photo-electrochemical (PEC) etching was used to fabricate deep trench structures in a GaN-on-GaN epilayer grown on n-GaN substrates. A 50-nm-thick layer of Ti used for an etching mask was not removed even after etching to a depth of >30 µm. The width of the side etching was less than 1 µm with high accuracy. The aspect ratio (depth/width) of a 3.3-µm-wide trench with a PEC etching depth of 24.3 µm was 7.3. These results demonstrate the excellent potential of PEC etching for fabricating deep trenches in vertical GaN devices. © 2018 The Japan Society of Applied Physics

Allium nitride (GaN) power devices have recently attracted considerable attention as energy-saving solutions because of their advantages in terms of low specific on-resistance ($R_{on}$) coupled with a high breakdown voltage ($V_B$).1) These advantages arise from the high electron drift velocity and high breakdown field of GaN compared with those of Si or GaAs.2,3) In addition, superjunction (SJ) structures have been developed in power semiconductor devices in order to outperform the unipolar operating limits.3,4) In SJ structures, p/n columns are used instead of a unipolar drift layer. It has recently been demonstrated that SJ structures with 25-µm-deep trenches can be fabricated even in wide-band-gap semiconductors such as silicon carbide (SiC).5) As a technical aspect, it is necessary to fabricate deep trench structures in an n-type layer with an aspect ratio (depth/width) of more than 10, an aperture width of 1–2 µm, and backfilling regrowth of a p-type layer. In GaN, lateral SJ field-effect transistors (SJ-FETs) with a breakdown voltage >10 kV have been fabricated,6,7) and there is a theoretical report on GaN vertical SJ devices.8) However, there is no report on the actual fabrication of GaN vertical SJ devices, because it is difficult to achieve deep trench etching with backfilling regrowth. The backfilling regrowth of p-GaN might be possible by hydride vapor-phase epitaxy (HVPE), because the p-type conduction is reported to occur without Mg-activation annealing.9) On the other hand, there are no reports on the deep trench etching of GaN. Generally, GaN is etched by inductively coupled plasma-reactive ion etching (ICP-RIE),10,11) Unfortunately, however, plasma readily causes damage to GaN, and there is low etching selectivity between the GaN and the etching mask. The issue of plasma damage has recently been solved by neutral-beam etching (NBE) and atomic-layer etching (ALE) techniques.12,13) However, these techniques give low rates of etching owing to the low flux of the etching ion, and are therefore unsuitable for deep etching. Consequently, their application is limited to gate-recess etching for AlGaN/GaN high-electron-mobility transistors (HEMTs). Moreover, no deep reactive ion etching (DRIE) technique has been developed for GaN, although this method is well known in the Bosch process for Si etching in the through-silicon via (TSV) technology for 3D integration and in micro-electromechanical systems (MEMS).14,15)

We surmised that photo-electrochemical (PEC) etching might have the potential to provide an answer to the problems discussed above,15) because this technique has excellent etching selectivity against the etching mask and because it produces little side etching owing to the short hole lifetime of GaN. PEC etching has recently been applied to the mesa fabrication of GaN pn-junction diodes (PNDs) with high $V_B$ values.16) Furthermore, PEC etching produces greater yields of high-$V_B$ devices than does the dry etching of GaN-PNDs. Other applications of PEC etching include gate-recess etching for HEMTs17) and selective etching of n-GaN for n-contact layers in vertical-cavity surface-emitting lasers (VCSELs).18) In particular, PEC etching has many advantages from the viewpoint of preventing damage to fabricated products because it is a plasma-free process. Here, we report the use of PEC etching in fabricating deep trench structures in GaN-on-GaN epilayers with the structures of Schottky barrier diodes (SBDs) and PNDs grown by metal–organic vapor-phase epitaxy (MOVPE) on n-GaN substrates.

The two-inch free-standing GaN substrates used in this study were produced by our void-assisted separation (VAS) method.19,20) The free-standing VAS-GaN substrate had a dislocation density of about $2 \times 10^5$ to $5 \times 10^6$ cm$^{-2}$ uniformly spread over its surface. More details of the procedure can be found elsewhere.21) The epitaxial layers with SBD and PND structures were grown by MOVPE on n-GaN substrates. The SBDs consisted of an n-GaN layer with a nominal Si concentration of $1.5 \times 10^{16}$ cm$^{-3}$ and a thickness of 5.8 µm. The PNDs consisted of a Mg-doped ($2 \times 10^{20}$ cm$^{-3}$ with 20 nm thickness and $5 \times 10^{19}$ cm$^{-3}$ with 500 nm thickness) layer of GaN on an n$^-$-drift layer of Si-doped ($2 \times 10^{16}$ cm$^{-3}$ with 10 µm thickness) GaN. A 2-µm-thick n$^+$-interlayer was grown between the n$^-$-drift layer and the n-type GaN substrate. The PNDs were annealed at 850 °C for 30 min in N$_2$ to activate the Mg acceptors by removing adherent hydrogen atoms before the mask-patternning process. The etching mask was a 50-nm-thick layer of Ti produced by vacuum evaporation and the standard electron-beam lithography process with lift-off.

First, we confirmed the adhesion between Ti and the p-type layer of PNDs during PEC etching by using a dot pattern, because this interface is probably the weakest point in side etching owing to the existence of holes. Second, we used
line mask patterns for evaluating the trench aspect ratio and pattern fineness. The PEC-etched pattern was examined by optical microscopy and scanning electron microscopy (SEM).

Photo-assisted anodic oxidation is the basis of the PEC etching of GaN. GaN dissolves as Ga$^{3+}$ ions owing to the holes excited by UV irradiation at the anode of the GaN/electrolyte interface, where electrons flow out to the outside circuit. The Ga$^{3+}$ ions react with hydroxide ions (OH$^{-}$) in the electrolyte, resulting in the formation of Ga$_2$O$_3$. This dissolves in acid or base, so that an anodic oxidation process is the basis of the PEC etching of GaN. The etching depth $W_t$ is proportional to the total etching current, that is, PEC etching obeys a Faradic law.\(1,25\)

\[
W_t = \frac{M}{zF\rho} \int J \, dt
\]

Here, $M$ is the molecular weight of GaN, $z$ is the valence of the GaN dissolution reaction, $F$ is the Faraday constant, $\rho$ is the density of GaN, and $J$ is the etching current density. $J$ can be replaced by $J = J_{\text{out}}/(1 - A_{\text{mask}})$, where $J_{\text{out}}$ is the current density in the outside circuit normalized to the electrochemical cell size, and $A_{\text{mask}}$ is the area ratio of the etching mask. Here, $z$, which is the number of holes in the dissolution reaction of 1 mol of GaN, is the most important parameter because it determines the accuracy of the PEC etching depth. In comparison with the PEC etching of GaAs and InP,\(^{26}\) the valence in the PEC etching of GaN depends on the etching condition, similar to ZnSe.\(^{25}\)

The mechanism of the valence shift of the PEC etching of GaN has been discussed in detail from the viewpoint of reaction kinetics,\(^{15}\) that is, the ratio of the evolution of N$_2$ to that of O$_2$ changes at the anode. To obtain a smooth etched surface, the reaction rate should be limited by the [OH$^-$] supply. In other words, the PEC etching should be performed under a sufficient UV irradiation intensity. Additionally, it is preferable to apply a pulsed PEC etching sequence with a static electrolyte during anodic oxidation. Furthermore, the etching current, which is equivalent in electrochemical terms to the anodic current, should be low to prevent the electrolyte from being stirred by the intense evolution of N$_2$ and O$_2$ at the anode. A PEC etching rate of 24.9 nm/min, which is comparable to the rate of damage-free dry etching, gave a smooth etched surface. The highest PEC etching rate examined was 175.5 nm/min, but this gave a rough etched surface.

The PEC etching process is shown schematically in Fig. 1. The electrolyte was a 0.01 M NaOH aqueous solution containing 1% Triton X-100 [C$_{19}$H$_{40}$O$_{9}$H$_{4}$OH]$_{n}$–(1,1,3,3-tetramethylbutyl)phenyl–polyethylene glycol] used as a wetting agent to reduce the surface tension and to assist in bubble removal from the epi surface. A Pt counter electrode (CE) was used as the cathode. The anode was a GaN epi surface with a back ohmic contact of the substrate. The etching voltage ($V_{\text{ce}}$) of 1 V was biased between the GaN epi surface and the Pt CE. The UV illumination intensity was 9.0 mW/cm$^2$, provided by a Hg–Xe lamp at vertical incidence. The pulsed PEC mode was used, that is, the UV irradiation and etching voltage were applied simultaneously only during the PEC step. The duty ratio of the applied voltage was approximately 0.6. The typical etching current density was approximately 3 mA/cm$^2$ when the area ratio $A_{\text{mask}}$ of the etching mask was 0.09. Details of the PEC etching have been described elsewhere.\(^{15}\)

First, we demonstrated PEC etching with a circular 50-nm-thick Ti dot mask of 90 µm diameter. To demonstrate the potential of PEC etching in deep trench fabrication, PEC etching was conducted to an etching depth of more than 20 µm. Figure 2 shows SEM images of the PEC-etched GaN PNDs. The size of the etched region remained almost the same as that of the etching mask, even after etching to a depth of over 20 µm. Although it was difficult to exactly evaluate the residual thickness of Ti, the estimated etching selectivity against an etching mask of Ti was >400 (~20 µm/50 nm). As shown in Fig. 2, the width of side etching was less than 1 µm with high accuracy, because the hole excitation was limited on the bottom of the Ti-mask aperture area.\(^{22}\) These results revealed the excellent potential of PEC etching for fabricating deep trenches in vertical GaN devices. Figure 2(b) shows that no kinks were formed at the epi/sub interface, whereas Fig. 2(c) shows that the degree of side etching is low near the p–n interface. These are reasonable results from the viewpoint of hole lifetime. Hu et al. reported that the highest rate of recombination occurs near the p–n interface where $\tau_{\text{p}} = p_{\text{τ}_{\text{n}}}$; here, $n$ ($p$) is the electron (hole) concentration and $\tau_{\text{n}}$ ($\tau_{\text{p}}$) is the electron (hole) lifetime.\(^{27}\) The asymmetry of the side-etching width between the p- and n-type layers, as shown in Fig. 2(c), might be caused by the differences in band bending and/or the hole lifetime. The PEC-etched cylinder shape is independent of the crystallographic orientation; this also indicates that the width of side etching is determined by the hole lifetime. The PEC etching rate for the cylinder pattern was 25.1 nm/min, as estimated from the etching depth of 27.6 nm

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**Fig. 1.** Schematic representation of PEC etching method. The anode, cathode, and electrolyte were a GaN epi surface, a Pt counter electrode, and 0.01 M NaOH aqueous solution, respectively. Ti was used as the etching mask.
for three PEC cycles each of 66 s, and is comparable to that for ICP-RIE etching. It is also possible to employ a much higher etching rate if the roughness of the etched surface is unimportant as, for example, in wafer-dicing applications.

Figure 3 shows SEM images of the PEC-etched GaN SBDs with an etching depth of approximately 7.7 µm. The diameters of the circular cavities were designed to be 1, 5, 10, and 20 µm.

Figure 4 shows typical cross-sectional SEM images of the trench patterns produced by PEC etching, cleaved along the m-face. Remarkably, each trench had almost the same PEC etching depth of around 7.7 µm; in other words, the depth-etching rate in each pulsed step was controlled by changing the current density. Figure 5 shows the relationship between the PEC etching depth \( W_r \) and the trench aspect ratio. Unfortunately, there are only a few reports on the fabrication of GaN vertical trenches, including nanopillar fabrication by regrowth.22,28–31) Previously reported GaN trench depths were approximately 1–3 µm with aspect ratios of 1–3. We therefore used SiC trench structures fabricated by ICP-RIE as our reference structures.5,32,33) In Fig. 5, the solid, dashed, and dotted lines correspond to estimates of the aspect ratio of PEC etching based on \( W_r/(W_{mask} + 2W_{side-etching}) \), where \( W_{mask} \) is the width of the Ti etching mask and \( W_{side-etching} \) is the amount of side etching. The width of the side etching was assumed to be 0.7 µm from Fig. 2(c). The filled symbols are the experimental data, which are consistent with the estimated values. With short-width aperture masks, the PEC etching rate showed a decrease at an etching depth of about 30 µm, because the UV radiation appeared to have difficulty in reaching the bottom of these deep trenches. This indicates that a coherent UV light source would be preferable for deep PEC etching. As a matter of fact, from Fig. 5, these results indicate that PEC etching has excellent potential for three PEC cycles each of 66 s, and is comparable to that for ICP-RIE etching. It is also possible to employ a much higher etching rate if the roughness of the etched surface is unimportant as, for example, in wafer-dicing applications.
for deep trench etching. The maximum aspect ratio was 7.3, with a trench width of 3.3 µm at a PEC etching depth of 24.3 µm. This aspect ratio and the etching depth are comparable to the best results for SiC trenches fabricated by ICP-RIE, and they indicate the excellent potential of PEC etching not only in the fabrication of optical and electronic devices, but also in fabricating GaN-MEMS such as the through-via of wafers, diaphragms, microfluidic channels, and optical gratings.

In conclusion, we successfully fabricated vertical GaN trench structures by PEC etching with a Ti mask. The width of side etching was less than 1 µm with high accuracy. The aspect ratio of trenches fabricated by PEC etching was more than 7 at an etching depth in excess of 20 µm. These excellent results obtained with PEC etching open the door to the fabrication of cutting-edge GaN device structures such as SJ-FETs, the ridge fabrication of laser diodes, wafer-dicing, and GaN MEMS. We commit to sharing this convenient PEC etching technology with the GaN community as part of our responsibility as a supplier of GaN substrates.

Acknowledgments This research was supported by the Ministry of the Environment of Japan (see the online supplementary data at http://stacks.iop.org/APPL. The authors thank Mr. Kentaro Tamaki and Mr. Nakamura of Mitani Micronics Co., Ltd., for their GDS-file transform service to EB lithography format.

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