Electrostatic discharge attenuation test for the characterization of ESD protective materials

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Abstract. New experimental method has been developed to evaluate materials, tools, equipment and packaging used in the electronics production environment under Charged Device Model (CDM) type of electrostatic discharge (ESD) transients. The method is intended to characterize the ability of the material or object to attenuate ESD energy and peak discharge current when a charged device is discharged into the material under test. The test is supplementary for the standard quasi-static measurements of ESD control programs in the cases where standard measurements do not give sufficient information due to voltage non-linearity, complexity or shape of the material or object under test.

1. Introduction

Consumer demand is pushing semiconductor technology for increased performance and frequencies. To achieve the performance, technology have been scaled to below 100 nm line width and the density of circuits on a device has been increased. As a trade-off of the increased circuit performance, the devices have become more sensitive to electrostatic discharge (ESD) events since the late 1990s. The current trend, which is expected to continue, is circuit performance at the expense of ESD protection level [1]. The increased sensitivity of devices to ESD suggests that one should place more emphasis on reducing ESD exposure on the manufacturing floor to allow safe handling of electrostatic discharge sensitive devices (ESDS) during the manufacturing of electronics.

Safe handling of ESDS requires careful control of materials, tools, equipment and packaging used in the electronics production environment. To avoid Charged Device Model (CDM) types of ESD failures of devices due to an abrupt discharge of charged device or board assembly, all contacts to charged electronics during manufacturing and testing should be done by ESD protective materials having carefully controlled charge dissipation properties [2,3]. By the contact to such a material, the charge stored on the device or entire printed wiring board assembly can be discharged safely.

Material requirements given in the international standards for the protection of electronic devices from electrostatic phenomena (IEC 61340-5-1 [4] and ANSI/ESD S20.20 [5]) rely on quasi-static measures such as resistance, electrostatic charge, potential and electrostatic field. However, where a charged ESD sensitive device may make contact with a material, a very fast electrostatic discharge current can flow which has fast rise and fall times and short (nanosecond) duration. Static measurements may not correctly predict the material response under these dynamic events [6].
Mechanical structure and the shape of the material of an object may affect stray capacitance, resistance and inductance and voltage coefficients in the discharge path, cause frequency dependency and determine the wave shape and amplitude of the transients. In addition, static resistance measurements are often made with relative low voltages in comparison with initial potentials of real CDM discharge and, therefore, possible nonlinearities of current-voltage characteristics cannot be found with standard surface or volume resistance tests. As a result, undesired device failures may happen if a material used for the control of CDM type of ESD shows surface resistance in the electrostatic dissipative range during the standard quasi-static measurement but exhibits nearly metallic conductivity under a real ESD event.

In this paper we present a new experimental method that can be used to evaluate materials and objects (including tools, equipment, packaging) used in the electronics manufacturing environment under CDM type of transients. The method is intended to characterize the ability of ESD protective material or object to attenuate discharge energy and peak discharge current when a charged device is discharged into the material under test. The test method is developed as a supplementary material test for the standard quasi-static measurements of ESD control standards where charged ESD sensitive devices can contact the material or object and CDM ESD may be a threat.

2. Measurement method and setup
A simplified electrical circuit of the method is shown in Figure 1. It is an RLC-series circuit, simulating a charged device as an ESD source, in series with a grounded material under test. In the test, the capacitor \( C \) is charged to a high test voltage (e.g. 1000 V) and a discharge is obtained by bringing a test probe into contact with the material under test. The discharge waveform is measured by a current transformer connected to a fast oscilloscope.

![Figure 1. Simplified Charged Device Model kind of circuit for the ESD attenuation test of materials](image)

We have used the ESD source circuit parameters of \( C=20 \, \text{pF}, \ R=35 \, \Omega \) and \( L=70 \, \text{nH} \). The 20 pF capacitor simulates a very large device or rather a small printed wiring board assembly as an ESD source. In our setup the capacitor was simply an adjusted plate of a standard charged plate monitor [4]. The 35 \( \Omega \) series resistor is to simulate energy dissipation in the device, leading to potential device failure in a real world discharge, as well as to improve the repeatability of the discharge waveform. The 70 nH inductance is a measured stray inductance of the system. A minimum of 200 MHz bandwidth of oscilloscope and current transformer is required for correct measurements based on these parameters. Measurements in this paper were carried out with 20 GSa/s oscilloscope and 1 GHz current transformer. The RLC-values used are relevant to product areas of authors’ experience. For other products and processed, some other values for the circuit resistance, inductance and capacitance may be more relevant.
The energy dissipated in the resistance (of the simulated electronic device) is integrated from the measured current waveform. Measured discharge energy and current values with a material under test are compared to reference values measured using a metal reference object as the discharge drain, corresponding to the worst case of CDM ESD. As a result, ESD energy and peak current attenuation for the material or object under test are reported, see Table 1 for examples. From the verification standpoint, it is useful also to integrate the charge transferred in the discharge from the measured discharge waveform and to compare the result to the initial charge stored in the discharge circuit capacitor.

The method simulates a real world CDM discharge in the sense that the energy measured simulates the ESD energy which may lead to device damage in a similar real world discharge, and the measured peak discharge current is related to an internal voltage transient which may lead to breakdown of local dielectrics inside a device. In a material with high level of attenuation, majority of energy dissipation will safely happen in the material – not in the victim charged device.

3. Experimental tests

Electrostatic discharge attenuation tests presented in this paper include measurements done for electrostatically challenging materials and objects as well as for simple reference materials for verification purposes. The ESD voltage (i.e. voltage over the discharging capacitor) was 1000 V in all examples presented in the paper, corresponding to the charge transfer of 20 nC in a complete discharge. Examples of discharge current waveforms together with integrated energies dissipated on the resistor R are given in Fig. 2. More examples of peak discharge currents and dissipated energies in a 1000 V, 20 nC discharge are given in Table 1 for a variety of materials and objects, including a discharge to a grounded metal cylinder acting as the reference. All results are median values for 5-10 discharges. Standard point-to-point resistances, measured according to ref. [4], are given in the table for reference.

ESD attenuation tests with resistors (Table 1) were done for verification purposes because the energy dissipated in a discharge can be calculated also using basic electric circuit theory for the circuit given in Figure 1. Calculated energy dissipation in the 35 Ω resistance with the 10 kΩ discharge drain was \((20 \text{ nC})^2 / 2 \cdot 20 \text{ pF} \cdot (35 \Omega / 35 \Omega + 10 \text{ kΩ}) = 35 \text{ nJ in a 1000 V, 20 nC discharge corresponding to energy attenuation of 35 nJ / 10 \mu J = -25 dB.}

The calculated value is the same as the measured one.

| Sample                        | Rpp [kΩ] | Ip [A] | E [nJ] | Ip/Ip[Ref] [dB] | E/E[Ref] [dB] |
|-------------------------------|----------|--------|--------|-----------------|---------------|
| Soldering paste (100 μm)      | 1 000    | 9.2    | 4 600  | -2              | -2            |
| Pin of dissipative tester jig | <10      | 7.3    | 2 300  | -4              | -5            |
| Pin of insulating tester jig  | >10 G    | 2.7    | 170    | -14             | -17           |
| Dissipative rubber            | 100      | 0.13   | 0.62   | -40             | -41           |
| Resistor 1 kΩ                 | 1        | 1.2    | 350    | -20             | -13           |
| Resistor 10 kΩ                | 10       | 0.6    | 25     | -26             | -25           |
| Metal reference               | 0        | 12     | 7 400  | -               | -             |

The ESD attenuation shown in Fig. 2 (a) is an example of material for which the results of standard DC resistance measurement could lead to false feel of safety against CDM damage risks for devices assembled on the soldering paste of a board. The point-to-point resistance [4] for the 100 μm thick layer of paste was 1 GΩ measured at 100 V. The discharge attenuation test for the same sample done at 1000 V, however, suggests that the material is conductive giving low impedance path to ground during the discharge. The reason for the significant difference in the material response is the non-linearity of the material resistivity with voltage.
Figure 2. Examples of ESD discharge attenuation test waveforms for the discharge current and energy dissipated in the charged (simulated) device for 1000 V, 20 nC discharge: (a) discharge to about 100 µm thick soldering paste, (b) discharge to a metallic and isolated pin of insulating tester jig.

The other example in Fig. 2 (b) demonstrates the case where the object consists of two electrostatically very different materials: a metallic and isolated support pin in highly insulating matrix of tester jig. It is very difficult to predict the ESD safety of such a heterogeneous object against CDM ESD using standard measurement methods. The discharge attenuation test shows high peak discharge current, which could be of high risk for some devices, but, on the other hand, quite strong attenuation of discharge energy, which would mean ESD safety for the majority of devices.

The ESD attenuation test for peak discharge current and energy dissipation in a victim (simulated) device gives a good estimate on how well the material or object in contact with charged device or board assembly could attenuate the discharge to an acceptable, safe level. What is a safe level depends strongly on the ESD susceptibility of the device or board assembly in question.

4. Conclusions

Fast dynamic measurements are recommended to evaluate materials and objects which can be in contact with charged ESD sensitive components and could be involved in CDM ESD risk. Current standardized DC measurements can not be used alone to characterize ESD protective materials if the protection is based on prevention of high speed discharge in sensitive devices. Therefore, we have developed a new dynamic test method which gives essential information for the evaluation of materials and objects which can be in contact with CDM ESD sensitive components in electronics manufacturing environment.

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