Thermal activation and quantum field emission in a sketch-based oxide nanotransistor

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Abstract

We report direct measurements of the potential barriers and electronic coupling between nanowire segments within a sketch-based oxide nanotransistor (SketchFET) device. Near room temperature, switching is governed by thermal activation across a potential barrier controlled by the nanowire gate. Below $T = 150$ K, current flow is dominated by quantum field emission. Sharp maxima in the quantum field emission, observed at $T_{C1} = 65$ K and $T_{C2} = 25$ K, arise from dielectric anomalies occurring at structural phase transitions in the SrTiO$_3$ layer. This direct measurement of the source–drain and gate–drain energy barriers is crucial for the development of room-temperature logic and memory elements and low-temperature quantum devices.

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(Some figures in this article are in colour only in the electronic version)

1. Introduction

The interface between polar LaAlO$_3$ and non-polar SrTiO$_3$ exhibits a remarkable variety of electronic behavior [1] associated with the formation of an interfacial quasi-two-dimensional electron gas (q-2DEG) [2–8]. A sharp insulator-to-metal transition as a function of increasing LaAlO$_3$ thickness was observed [3], along with hysteretic switching between the metallic and insulating phases at a critical thickness of 3 unit cells (3 uc). Local switching of heterostructures consisting of 3 uc of LaAlO$_3$ grown on TiO$_2$-terminated SrTiO$_3$ (3 uc-LAO/STO) was subsequently reported [9]. A positive bias applied to a conductive atomic-force microscope (c-AFM) tip charges the top LaAlO$_3$ surface [10, 11], locally switching the interface to a conducting state; a negative bias discharges the top LaAlO$_3$ surface, locally restoring the insulating state. In a sense, the 3 uc-LAO/STO system can be regarded as an ultra-dense two-dimensional network of floating-gate field-effect transistors. The nanoscale writing and erasing can be regarded as a form of reversible modulation doping, using donors that are placed approximately one nanometer from the interface. By ‘sketching’ patterns of charge on the top LaAlO$_3$ surface, the LaAlO$_3$/SrTiO$_3$ interface conductance can be controlled with near-atomic spatial resolution [9]. Using this technique, a variety of structures and devices have been demonstrated at room temperature [12, 9, 10]. Among them, the sketch-based oxide nanotransistor (SketchFET) [10, 13] is especially interesting due to the small features with which they are constructed (as small as 2 nm).

The SketchFET results reported in [10] raise several questions that are relevant for future technological applications: What is the nature of the transistor action of the SketchFET? What is the depth of the electronic confinement potential between source and drain, and how is it modulated by the gate? What is the dominant carrier transport mechanism across these potential barriers? What role do the nanowires themselves play in governing transport in the device? A reliable method for determining these energy barriers and transport mechanisms is through temperature-dependent transport measurements. A convenient structure for quantifying these energy barriers is a SketchFET itself, since the electric field applied by source, drain and gate leads effectively tunes the energy profile and therefore can carry out examination in one more dimension.

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2. Experiment

Temperature-dependent experiments are performed in SketchFETs created from an oxide heterostructure consisting of 3.3 unit cells of LaAlO$_3$ grown on TiO$_2$-terminated SrTiO$_3$ substrates. The films were grown at the University of Augsburg by pulsed laser deposition using parameters that are described elsewhere [9, 10]. Ohmic contact with the interface is made with Ar ion etching followed by Au/Ti deposition. A comparison between two-probe and four-probe measurements [10] indicates that the contact resistance is orders of magnitude smaller than the c-AFM-written structures and can be neglected for the results described below. SketchFET structures are written at the interface between the two oxides using a c-AFM probe (figure 1(a)). Two SketchFET devices are created under nominally identical conditions with qualitatively reproduced characteristics observed. For consistency, results are shown for only one of them. The particular SketchFET device discussed here (figure 1(b)) consists of three nanowire sections: ‘source’, ‘drain’ and ‘gate’. Each nanowire is written with a tip bias $V_{\text{tip}} = +10 \, \text{V}$, which produces an approximately 16 nm wire width (figure S1 available at stacks.iop.org/Nano/21/475201/mmedia). A comparably sized potential barrier in the channel between the source and drain is created with $V_{\text{tip}} = -10 \, \text{V}$. The gate lead is oriented perpendicular to the barrier region and is separated from the channel by 50 nm.

Throughout the experiments, SketchFET devices were kept in the dark chamber of a closed-cycle refrigerator with a vacuum level on the order of $10^{-5}$ mbar or below.

3. Results and discussion

The gate-tuned drain current $I_D$ as a function of the source–drain voltage $V_{\text{SD}}$ ($I$–$V$ characteristics) of the SketchFET was measured at various temperatures ranging from room temperature (295 K) down to 15 K. The voltage sweeping rate was kept slow to eliminate the observation of capacitive or inductive reactance, and no noticeable hysteresis was observed comparing data taken during forward and backward voltage sweeps. Representative curves for three gate biases ($V_{\text{GD}}$) and three temperatures taken during a single slow cool-down are shown in figure 1(c). Subsequent experiments carried out at controlled temperatures or during a warm-up process verified the repeatability of the data under thermal cycling. In general, positive gate biases increase the source–drain conductance while negative biases suppress it. One qualitative interpretation is that the gate electrode is shifting the bottom of conduction band at the barrier region through the Fermi level and thereby
altering the carrier density, as with a standard field-effect transistor. At room temperature, the channel conductance near zero source–drain bias can be tuned by the gate over more than four orders of magnitude. Most of the I–V curves are purely odd functions of V_S, indicating that the field-tunable current flux is localized within the channel. At low temperatures and negative gate bias (V_GD = −2 V), an asymmetric I–V profile and slight negative differential resistance are observed (figure 1(c) (150, 20 K)) that is associated with the existence of leakage current from the gate lead [10].

Between room temperature and 150 K, the source–drain conductance decreases monotonically with decreasing temperature (figures 2(a) and (b)). Nanowires written by c-AFM without junctions typically exhibit a monotonically increasing conductance with decreasing temperature (figure S4a available at stacks.iop.org/Nano/21/475201/mmedia). Therefore, the potential barrier in the central junction of the SketchFET devices plays a dominant role in the decrease of the channel conductance. When the gate lead is also grounded, current measured at the drain can only flow from/to the source. Under these conditions, an unambiguous investigation of the barrier between the source and drain can be performed without the contribution of gate leakage current. Values of current flow into the drain when V_SD = 1 V and current flow out of the drain when V_SD = −1 V are comparable (figure 2(a)), indicating a generally symmetric potential profile along the channel between the source and drain.

Arrhenius plots of the drain current I_D as a function of temperature for various values of V_SD and V_GD are shown in figure 2(b). For a given V_GD, the temperature dependence of I_D reflects a thermal activation characteristic. The saturation of I_D at elevated temperatures can be accounted for by including the finite conductance of the source and drain nanowire leads which limits I_D when the thermal activation rate is high. Numerical fits using a simple equivalent-circuit model (figure S3 available at stacks.iop.org/Nano/21/475201/mmedia) produce good agreement with experimental results (figure 2(b)) using only a single fitting parameter for the lead conductance.

Figure 2(c) shows the extracted activation energies E_a for different source and gate biases. When a non-zero gate voltage is applied, gate leakage may also contribute to the drain current; however, due to the much wider barrier between gate and channel (figure 1(b)), this leakage current is negligibly small above 150 K. Therefore, the activation energies E_a extracted provide a reasonably accurate quantification of the potential barrier between the source and drain. The results show that the source–drain energy barrier can be reduced either by increasing the gate bias or the magnitude of the source bias. Varying the gate and source bias between ±2 V modulates the source–drain barrier by 0.5 eV, which is consistent with the 10^4 on–off ratio of the SketchFET device, limited by the finite conductance through the nanowire leads. We note that higher ratios are in principle achievable if the nanowire leads conductance is reduced appropriately.

When the source lead is grounded, only gate emitted/collection electrons contribute to the current measured at the drain. This leakage current is plotted as a function of temperature in figure 3(a) at different gate biases. In the thermally activated region above 200 K, the magnitude of drain current |I_D| is much larger for V_GD > 0 than for V_GD < 0. Activation energies E_a^+ = 0.39 eV and E_a^- = 0.53 eV are
Figure 3. Temperature dependence of gate leakage current. For $V_{GD} = 0$ V, current only flows between the gate and drain. (a) Gate–drain current $I_d$ versus temperature for $V_{GD} = 2.0, -2.0$ V. Maxima in $|I_d|$ are observed at two temperatures $T_{C1} = 65$ K and $T_{C2} = 25$ K for $V_{GD} = -2$ V. (b) Arrhenius plot of leakage current above 200 K at gate bias of 2 or $-2$ V. Difference in the extracted thermal activation energies indicates an asymmetry in the potential profile between the gate and the channel. ((c)–(e)) Finite element method simulation of electric field strength in the central junction area of the SketchFET for $V_{GD} = -2$ V and temperatures below (C), at (D) and above (E) a structural phase transition. Near $T = T_C$, a marked increase in field strength at the gate electrode greatly raises the electron field emission rate.

extracted from the Arrhenius plot for $V_{GD} \pm 2$ V, respectively (figure 3(b)). The difference in the activation energy signifies an asymmetric shape of the barrier between gate and drain. Below 200 K, the thermally activated leakage current decays below our measurement limit. For the positive gate bias $V_{GD} = 2$ V, the flow of electrons from drain to gate remains small down to the lowest temperature measured. For negative gate bias $V_{GD} = -2$ V, the flow of electrons from the gate exhibits two local maxima at $T_{C1} = 65$ K and $T_{C2} = 25$ K. We suggest that at low temperatures, the main contribution to the leakage current at $V_{GD} < 0$ is quantum tunneling via Fowler–Nordheim (FN) field emission. As will be discussed in detail below, the FN field emission is highly sensitive to the local electric field

$$\varepsilon = \begin{cases} T < T_C & \frac{T - T_C}{C} \\ T = T_C & C \\ T > T_C & \frac{2T_C - T}{C} \end{cases}$$

where $T_C$ is the Curie–Weiss temperature and $C$ is a constant. The electric field dependence $\varepsilon(T, E)$ in SrTiO$_3$ is readily estimated within the simplest LGD model (see supporting information and figure S2 available at stacks.iop.org/Nano/21/475201/mmedia). Using the calculated function $\varepsilon(T, E)$, the electric field strength over the 100 nm $\times$ 100 nm SketchFET area is calculated self-consistently at different temperatures using a finite element method (figures 3(c)–(e)). At transition temperatures $T_{C1}$ (paraelectric to ferroelastic) and $T_{C2}$ (ferroelastic to ferroelectric), the diverging and highly field-sensitive dielectric permittivity greatly improves the field
screening in the middle area between the gate, source and drain leads. As a consequence, the electric field $E$ is localized at the boundary of the gate lead with a significantly increased local intensity. The sharp increase in the electric field strength for negative $V_{GD}$ at $T \approx T_C$ greatly enhances the FN field emission rate $j \propto \Phi_1^2 \exp\left(-\frac{b}{\Phi_1^2 E^2}\right)$, where $\Phi$ is the work function of the emitter and $b$ is a constant [28]. For positive $V_{GD}$, the leakage current remains small because the drain lead, as the electron emitter, has significantly lower boundary field strength.

The low-temperature maxima in leakage current at $V_{GD} = -2 \text{ V}$ vanish when $V_{SD}$ changes sign from 1 to $-1 \text{ V}$ (figure 4(a)). This result can be explained by the decreased local field strength around the boundary of the gate lead (figures 4(b)–(d)). The sensitivity of the leakage current to the field strength near the emitter is a signature of FN field emission processes. Dielectric anomalies also show up in source–drain current (figure 4(e)) but coexist with a residual tail of the thermally activated current. Varying the source voltage changes the local field strength along the electron-emitting source lead, which tunes the local maxima’s intensity (figures 4(f)–(h)). Anomalies in conductance at the same temperatures are also observed in nanowire structures where the potential barriers within the nanowires are formed unintentionally (figure S4b available at stacks.iop.org/Nano/21/475201/mmedia). One potentially important contribution not considered here is that the electron mobility within...
the nanowires may experience similar anomalies, thus increasing the attempt rate for electron tunneling through the barrier [29]. A full quantitative picture would need to take into account (self-consistently) the sharp variation in the dielectric permittivity within the nanowires themselves. Such detailed analysis extends beyond the scope of this paper.

4. Conclusions

We have measured temperature-dependent transport in a nanoscale transistor (SketchFET), created at the 3 uc-LaAlO3/SrTiO3 interface using a rewritable c-AFM lithography technique. The SketchFET maintains its transistor functionality down to the lowest temperatures measured, \(T = 15\, \text{K}\). Between room temperature and 150 K, transport in SketchFET is dominated by thermal activation. Changing voltages applied to the gate and source electrodes within ±2 V can tune the channel activation energy from 0.1 to 0.6 eV. Our experimental observation of four orders of magnitude on-off ratio is limited by the source–drain lead resistance. Below 150 K, as thermal activation rate decays quickly with the lowering temperature, Fowler–Norheim quantum field emission starts to play an important role. Field emission current changes sensitively under different biasing conditions and is qualitatively well explained by the finite element simulation of the electric field distribution in SketchFET. Sharp peaks of field emission current are observed at 65 and 25 K, and are attributed to structural phase transitions in the SrTiO3. This investigation marks the first step in characterizing the energy landscape of oxide nanostructures, with implications for the performance of nanodevices at room temperature and at low temperatures.

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