Computationally efficient formulation of relay operator for Preisach hysteresis modeling

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Abstract—An algebraic expression for the Preisach hysteron, which is a non-ideal (delayed) relay operator, is formulated for a computationally efficient real-time implementation. This allows representing the classical scalar Preisach hysteresis model as a summation of a large number of weighted hysterons which computation can be accomplished in parallel. The latter makes possible an efficient FPGA or ASIC realization of the scalar Preisach hysteresis model that can be useful for multiple applications. The signal flow which specifies the model implementation is provided in form of the block diagram. The proposed computation of Preisach hysterons, aggregated to the entire Preisach hysteresis model, is evaluated numerically and on a real-time hardware platform.

Index Terms—Hysteresis, Preisach model, non-ideal relay, real-time computation, hysteron, nonlinear operator

I. INTRODUCTION

The scalar Preisach hysteresis (SPH) model is a universal mean for describing the rate-independent hysteresis phenomena with congruent loops and erasable, i.e. with wiping out property, memory, see e.g. [1] for details. The operator-based mathematical formalism of Preisach hysteresis model has been thoroughly studied and described in seminal works [1]–[4]. The definition of a Preisach hysteresis operator is general enough and a variety of formulations and implementations have been proposed in the literature, often depending on the application at hand and particular computation method yielding the hysteresis state and correspondingly output. A very common form of the SPH model, suitable for the fast real-time inversion and control, are the so-called Everett integrals, as used e.g. in works [5]–[7]. This form relies on the stored Everett integrals matrix, which is the measured realization of first-order reversal curves, and computes the hysteresis output by an explicit formula provided in [8], [9]. Using the space representation of Preisach plane, which is a well-known geometric interpretation of the Preisach model, and corresponding memory-line interface several schemes evaluate the output increment of the Preisach operator, see e.g. [10]. A related attempt of a continuous-time state-space formulation of the SPH model has been made in [11] and applied, with discrete-time, in the control in [12].

At the same time, the classical SPH model formulation, as in [13], is given by

$$f(t) = \int_{\alpha \geq \beta} \mu(\alpha, \beta) \gamma_{\alpha \beta} x(t) d\alpha d\beta,$$

where $x(t)$ is a piecewise-monotone input function and $\mu(\alpha, \beta)$ is an integrable nonnegative function defined over the $(\alpha, \beta)$ Preisach (half) plane with $\alpha \geq \beta$. The Preisach weighting function $\mu(\cdot)$, also denoted as Preisach density function, has a finite support (on the Preisach plane) within some triangle $T$ which is given by the hypotenuse $\alpha = \beta$ and the right angle at $(x_{\text{max}}, x_{\text{min}})$. Therefore, for a given input domain $[x_{\text{min}}, x_{\text{max}}]$ the Preisach density function $\mu(\alpha, \beta)$ with $(\alpha, \beta) \in T$ entirely parameterizes the Preisach hysteresis operator. The overall state of the Preisach hysteresis is determined by an infinite set of Preisach hysterons $\gamma_{\alpha \beta}$ which are the non-ideal relays with two discrete states $\gamma_{\alpha \beta} \in \{-1, +1\}$. Further mathematical properties of the Preisach hysteresis operator can be found e.g. in the works [13], [14].

While the discontinuous state transitions of a Preisach hysteron can be represented as in Fig. 1, the often used notation of the hysteron’s states is given by

$$y(t) = \gamma_{\alpha \beta} x(t) = \begin{cases} -1, & \text{if } x(t) \leq \beta, \\ +1, & \text{if } x(t) \geq \alpha, \\ y(t_0), & \text{if } \beta < x(\tau) < \alpha \quad \forall \tau \in [t_0, t]. \end{cases}$$

Therefore, the state of each hysteron is uniquely determined provided the initial sate at the time instant $t_0$ is given. From the practical, and thus application-related, point of view a computationally efficient and possibly real-time compatible realization of the total Preisach operator, and correspondingly single Preisach hysterons if required, can be a crucial factor when using the SPH model. Also in view of a finite memory implementation, when a non-parametric measure on the Preisach plane is assumed, an efficient storage of the hysteresis parameters is desirable along with the computation of hysteresis states. Recall that a non-parametric Preisach...
measure does not assume any analytic form of the Preisach density function and implements a discrete mesh (also denoted as grid) on the Preisach plane. A comparison of parametric and non-parametric identification of the Preisach hysteresis can be found in [15].

Apart from a fast real-time formulation of the SPH model and its inverse, reported e.g. in works [5]–[7], a parallelizm in processing (computing) a large number of elementar hysteresis operators, e.g. hysterons, can be highly efficient for multiple applications. Here the FPGA (Field Programmable Gate Array) and ASIC (Application-Specific Integrated Circuit) hardware solutions appear as well-promising when implementing a hysteresis model. This is quite naturale when neither sequential processor-based computations are required. The FPGA-based solutions of hysteresis computation and correspondingly control have been shown in [16], [17] for Krasonos’ skii-Pokrovskii and in [18] for Prandtl-Ishlinskii hysteresis operators. Among the real-time applications, the work [19] can be mentioned here, while the developed and VHDL (Very High Speed Integrated Circuit Hardware Description Language) implemented nonlinear hardware model of the power transformer included a real-time hysteresis computation.

The aim of this paper is to propose a computationally efficient formulation of a relay operator, i.e. Preisach hysteron, and thereupon based implementation of the SPH model. The main contribution is in deriving a rigorous algebraic form for (2) which allows a real-time execution of arbitrary input series and, above all, parallel processing of multiple hysterons. A low set of primitive operations required per hysteron – two summations, two sign operators, and two comparisons, plus one memory storage of the previous state – allow a FPGA-compatible implementation without any complex program routines. In the following, we describe in details the proposed formulation of the relay operator (2) and comment on the related entire SPH model in Section II. In Section III, a numerical evaluation is shown along with a hardware validation of the real-time computation. The latter is accomplished, in the first stage insofar, on the dSpace DSP (digital signal processor) platform at 2 kHz sampling rate. A relatively high but also limited, through the DSP operation memory capacity, number of hysterons \( N = 210 \) is assumed. The paper is concluded by a brief summery and discussion both provided in Section IV.

II. COMPUTATIONALLY EFFICIENT FORMULATION OF RELAY OPERATOR

In order to derive a computationally efficient algebraic expression for the non-ideal relay (further denoted as hysteron), as in Fig. 1, consider first the memoryless sign nonlinearities \( \text{sign}(x - \beta) \) and \( \text{sign}(x - \alpha) \) with \( \alpha > \beta \). Both represent the one-way switching behavior of a hysteron at thresholds \( \beta \) and \( \alpha \). The first one is for a monotonically decreasing input, i.e. \( dx/dt < 0 \), and the second one is for a monotonically increasing input, i.e. \( dx/dt > 0 \). When mapping both sign operators into the \((x, y)\) state diagram, see Fig. 2, one can recognize that the minimal state of both, i.e.

\[
\min \left[ \text{sign}(x - \beta), \text{sign}(x - \alpha) \right],
\]

describes the hysteron’s behavior on the interval \( x \in (-\infty, \beta) \cup (\alpha, \infty) \). For the interval between the threshold values, i.e. \( x \in [\beta, \alpha] \), the operator state remains undefined.

Further consider the interval \( x \in (\beta, \infty) \) for which the possible hysteron transitions can be represented as in Fig. 3. Here one can see that the recent state \( y \) depends not only on the recent input but equally on the previous state denoted by \( y(t-) \).

Since the switching condition is captured by \( \text{sign}(x - \alpha) \), the latter is to combine with the previous state, and that by the maximal value selection

\[
\max \left[ y(t-), \text{sign}(x - \alpha) \right].
\]

Now one can recognize that in order to complete the overall set of hysteron transitions, and correspondingly states, the subset (3) has to be combined with the \( \text{sign}(x - \beta) \) switch, here again by the minimal value selection, so that

\[
y(t) = \min \left[ \text{sign}(x - \beta), \max \left[ y(t-), \text{sign}(x - \alpha) \right] \right].
\]

Introducing the initial state

\[
y(t_0) = \begin{cases} 
\text{sign}(x(t_0)), & \text{if } x(t_0) \in (-\infty, \beta) \cup (\alpha, \infty), \\
[-1, +1], & \text{otherwise}. 
\end{cases}
\]

we obtain the overall input-output behavior of a hysteron, and that in the closed analytic form (4), (5). In view of a possible real-time implementation, the related signal flow can be represented by the block diagram as in Fig. 4. One can see that the proposed implementation requires solely 2 summation operators, 2 sign operators, and two comparators (max, min), plus an additional memory block for storage of the previous output state. For the parameterization of hysteron, the \( \alpha, \beta \), and \( y_0 \) values have to be stored. Further we note that in terms of incorporating the single hysterons into the

![Fig. 2. State transitions of sign operators at hysteron’s thresholds](image)

![Fig. 3. State transitions of \( \max[y(t-), \text{sign}(x - \alpha)] \) for \( x \in (\beta, \infty) \)](image)
Preisach hysteresis model each output \( y_i \), of the overall \( i \in \mathbb{N} \) hysterons, is subject to an additional gain \( W_i \). The latter is directly applicable at the output signal flow of Fig. 4.

Most important is the fact that the real-time computation of multiple hysterons does not require any sequentially executed program codes. Therefore a fully parallel (one-step) computation of a large number of single hysterons can be realized by means of e.g. FPGAs or ASICs, developed for a particular application. One can see that the summation

\[
f(t) = \sum_{i=1}^{N} W_i y_i(x(t), \alpha_i, \beta_i, y_i(t_0))
\]

of overall \( N \) weighted hysterons, all connected to the same input channel and executed in parallel, provides the entire Preisach hysteresis model. The latter is parameterized by the vectors of threshold values \( \alpha, \beta \in \mathbb{R}^{N \times 1} \) with \( \alpha \geq \beta \), initial states \( y_i(t_0) \in \mathbb{R}^{N \times 1} \) with \( y_i(t_0) \in [-1, +1] \), and hysteron weights \( W \in \mathbb{R}^{N \times 1} \) with \( W_i > 0 \). Furthermore, it is worth noting that the parallel real-time computation according to Fig. 4 and eq. (4) allows equally for further advanced features of the Preisach hysteresis model, like e.g. the direct recursive application. One can see that the summation

\[
f(t) = \sum_{i=1}^{N} W_i y_i(x(t), \alpha_i, \beta_i, y_i(t_0))
\]

provides a parallel processing of single hysterons but allows to prove the correctness of a real-time execution of hysteron’s implementation as in Fig. 4. The sampling rate is set to 2 kHz and the assumed number of hysterons is 210. The latter is limited by the available DSP operation memory and embedded compiler. First, a 1Hz sinusoidal input is proceeded during the 120 sec runtime. The recorded 120 major hysteresis loops are shown in Fig. 6 (a) over each other. Second, the white noise input which is low-pass (10 Hz cut-off frequency) filtered is proceeded during the 120 sec runtime. The recorded hysteresis trajectories are shown in Fig. 6 (b). Note that due to a large sporadic amplitude variations of the noise input series, the depicted (overlapping) trajectories are smoothing the hysteresis output steps, which are naturally related to the switching of single hysterons and clearly visible in Fig. 6 (a). Apart from that, the grey-shaded hysteresis area, inside of the major loop in Fig. 6 (b), discloses a correct response of implemented SPH model to a long-range random input sequence.

![Signal flow diagram of Preisach hysteron (non-ideal relay)](image)

III. NUMERICAL AND HARDWARE EVALUATION

The computation of SPH model, and that according to (4)–(6), is first evaluated within a numerical simulation (MATLAB/Simulink R2010b). A 80 × 80 mesh on the discretized Preisach plane is assumed which results in a total of 3240 hysterons. An uniform Preisach density function is assumed, for the sake of simplicity, that means the single weights of all hysterons have the same value. The latter is set so that the total co-domain is \( f(x) \in [-1, ..., 1] \). A monotonically decreasing sinusoidal input has been applied which results in a set of the nested minor hysteresis loops running towards the \((x, f)\) origin. The hysteresis loops recorded from the numerical simulation are shown in Fig. 5.

![Hysteresis loops of scalar Preisach hysteresis model (6) with 3240 hysterons computed for a monotonically decreasing sinusoidal input](image)

As next, we evaluate the real-time SPH model computation, according to (4)–(6), on the available DSP hardware platform dSpace DS1104CLP. Note that the latter does not provide a parallel processing of single hysterons but allows to prove the correctness of a real-time execution of hysteron’s implementation as in Fig. 4. The sampling rate is set to 2 kHz and the assumed number of hysterons is 210. The latter is limited by the available DSP operation memory and embedded compiler. First, a 1Hz sinusoidal input is proceeded during the 120 sec runtime. The recorded 120 major hysteresis loops are shown in Fig. 6 (a) over each other. Second, the white noise input which is low-pass (10 Hz cut-off frequency) filtered is proceeded during the 120 sec runtime. The recorded hysteresis trajectories are shown in Fig. 6 (b). Note that due to a large sporadic amplitude variations of the noise input series, the depicted (overlapping) trajectories are smoothing the hysteresis output steps, which are naturally related to the switching of single hysterons and clearly visible in Fig. 6 (a). Apart from that, the grey-shaded hysteresis area, inside of the major loop in Fig. 6 (b), discloses a correct response of implemented SPH model to a long-range random input sequence.

IV. SUMMARY AND DISCUSSION

A. Summary

A computationally efficient algebraic form of the Preisach hysterons, which is a non-ideal relay, has been proposed. This
allows applying a large number of hysterons, all executed (computed) in parallel, for a real-time implementation of the scalar Preisach hysteresis model. The proposed formulation utilizes a low number of primitive operations connected into a signal flow chart without any complex computational routines. This allows a direct FPGA or ASIC based hardware implementation which can be efficient for multiple applications. The proposed computation of hysterons, and thereupon assembled SPH model, has been evaluated in the numerical simulation and, additionally, on the DSP based real-time hardware. In perspective, the proposed solution is to be implemented and evaluated on a FPGA board using the intrinsic parallelism of computing a large number of hysterons.

B. Discussion

Theoretically, the single limitation posed on the usage of proposed method arises from the memory capacities of the low-end hardware platform at hand, i.e. FPGA or ASIC. The utilized min-, max-, and sign-operators constitute the simple comparators at the low-level. Additionally, two summation and one time-delay functional blocks are required per each hysteront unit. The time-delay block is a standard sample-and-hold element switched in a feedback manner. Therefore, the sampling time of computing a hysteron, and consequently all hysterons in parallel, is only double of the base sampling time of the hardware target. Apart from the summation block, with overall \( N \) input channels as in eq. (6), one common zero constant for the sign-related comparators and two common initial state constants \([-1,1]\] have to be recorded in a ROM memory. Furthermore, three additional constants have to be statically memorized (stored) per each hysteront block. These are the threshold and weight parameters.

The proposed method is suitable for a relatively large class of different applications, whenever a rate-independent Preisach hysteresis computation in real-time is required. One of the possible application fields is a hardware in the loop during the design, optimization, and fault detection or monitoring of the magnetic devices, see e.g. [22], [23] as potential examples. Another thinkable application is an online (recursive) identification of hysteresis behavior in a process, see e.g. [21]. Here the proposed method is easily extendable for a recursive scheme of parameter adaption. Finally the model-based control applications with hysteretic actuators, see e.g. [5], [12], [17], [18], [24], can generally benefit from the proposed fast computation, while various strategies of using the hysteresis model in control are thinkable.

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