Multi-Tensor Contraction for XEB Verification of Quantum Circuits

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The computational advantage of noisy quantum computers has been demonstrated by sampling the bitstrings of quantum random circuits. An important issue is how the performance of quantum devices could be quantified in the so-called “supremacy regime”. The standard approach is through the linear cross entropy benchmark (XEB), where the theoretical value of the probability is required for each bitstring. However, the computational cost of XEB grows exponentially. So far, random circuits of the 53-qubit Sycamore chip were verified up to 10 cycles of gates only; the XEB fidelities of deeper circuits were approximated with simplified circuits instead. Here we present a multi-tensor contraction algorithm for speeding up the calculations of XEB for quantum circuits, where the computational cost can be significantly reduced through some form of memoization. As a demonstration, we analyzed the experimental data of the 53-qubit Sycamore chip and obtained the exact values of the corresponding XEB fidelities up to 16 cycles using only moderate computing resources (few GPUs). If the algorithm was implemented on the Summit supercomputer, we estimate that for the supremacy (20 cycles) circuits, it would only cost 7.5 days, which is several orders of magnitude lower than previously estimated in the literature.

1 Introduction

Quantum computational supremacy [1, 2, 3] represents the status where a universal quantum computing device can accomplish a certain well-defined computational task much faster than any classical computer. In 2019 Google’s quantum team claimed that this goal was achieved [7]: their 53-qubit Sycamore superconducting chip produced one million samples per 200 seconds with fidelity up to 0.2% from some random quantum circuits with depth 20, while the same task of random circuit sampling with a classical supercomputer was predicted by the Google team to require as many as 10,000 years.

Afterwards, many attempts have been made in order to challenge [8, 9] Google’s claim by simulating the same quantum circuits with classical computers [10, 11, 12, 13]. The most popular approach so far is based on tensor network (TN) contractions; it is an important tool for classical simulations of large quantum systems [14], especially when the size of classical memory fails to cover the whole quantum state. Currently, state-of-the-art tensor network algorithms are often applied to estimate the expectation values of quantum observables [15], and evaluate single amplitudes or batches (i.e., a collection of bitstrings that share some fixed bits) of amplitudes for quantum circuits [16, 17, 10, 11]. The amplitudes can be obtained by directly contracting all indices in the TN, or by using slicing, also called variables projection [18, 10, 7, 19]. The latter is usually less efficient but reduces the required memory size and allows to perform the contraction in parallel.

In the context of random circuit $C$ simulation with TNs, previous works [17, 16, 20, 10, 11, 19] focused mostly on the efficiency in the evaluation of a single amplitude/probability $p_C(s) = |\langle s | C^\dagger 0^n \rangle|^2$ or one batch of amplitudes. For example, in [16] a batch of size $2^{37}$ is calculated for a universal random circuit of depth 23 in a 2D lattice of $8 \times 7$ qubits. Furthermore, the idea of using large batches in quantum simulations as a trade-off between the single-amplitude and the full-state simulators is discussed in [20].

1Let us note that there exists another popular approach to quantum supremacy called boson sampling [4, 5, 6], which is not considered in this paper.
The computational cost of calculating one batch of size $s$ using TN contractions is usually much smaller than the cost of calculating $s$ independent amplitudes. This significant cost reduction is because when we calculate the amplitudes in a batch we have a lot of common subexpressions that can be shared and reused during the contraction algorithm. It was shown very recently [19] that this general idea can also be used to reduce the cost of slicing.

However, in order to perform a full classical simulation of a quantum circuit $C$, or to verify the fidelity of the experimental output, one must also consider the problem on how multiple uncorrelated (batches of) amplitudes can be evaluated efficiently. Particularly, in Google’s experiment [7] the linear cross-entropy benchmarking (Linear XEB) was proposed as a tool for estimating the fidelity of random circuits. Explicitly, the linear XEB fidelity $F_{\text{XEB}}$ for a sequence of bitstrings $s_1, \ldots, s_k$, produced by the experiment is defined as

$$F_{\text{XEB}} \equiv \frac{2^n}{k} \sum_{i=1}^{k} p_C(s_i) - 1 . \quad (1)$$

In other words, for the verification task in random-circuit sampling, one needs to find the (theoretical) exact amplitudes for the random bitstrings produced in the experiments. At first sight, we may try to minimize the cost of calculations by choosing the batches covering as many as possible the experimental bitstrings. However, the problem is that the sampling size is too small, $k \ll 2^n$ ($\sim 10^6$ vs $2^{53}$ in Google’s experiment [7]), compared with the whole Hilbert space; one would often need to calculate almost all $k$ batches of amplitudes in practice. Apart from the verification task, we may also benefit [21] from finding multiple batches of amplitudes if we want to sample from a quantum circuit $C$ according to its output probability distribution $p_C(s)$ using the frugal rejection sampling method [22, 7].

On the other hand, a recent work [13] demonstrated spoofing of the Linear XEB test in the aforementioned Google’s experiment for the “supremacy circuit” (53 qubits, 20 cycles), with a single batch of amplitudes. Here spoofing means that, instead of running the actual simulation with a classical computer (i.e., output bitstrings according to the distribution of the actual quantum circuit), one produces bitstrings in a way just for passing the statistical test—the Linear XEB. We should note that despite the big difference between the simulation and spoofing tasks for random quantum circuits, the latter is also considered by some researchers to be a classically-hard problem [23], but in some special cases there exist polynomial-time algorithms [24].

In the current work, we develop a new set of tools for solving problems involving contraction of multiple tensor networks. The main feature of our approach is to assign a contraction tree [25, 26, 10] the contraction expression, where pre-calculated sub-expressions are invoked as much as possible. Moreover, a global cache is utilized to collect these values for speeding up multiple tensor contraction of different (batches of) amplitudes. As a result, this approach allows us to reduce the total computational cost by several orders of magnitude, compared to independent multiple runs of the tensor contraction. Furthermore, this approach is compatible with different TN contraction algorithms available in the literature [10, 11, 13]. Here our contraction algorithm is based on local transformations of contraction trees described in Appendix A.

The proposed algorithm was applied to verify the XEB fidelity of the (ABCD) supremacy circuits containing non-simplifiable tiling and sequence of quantum gates [27], where no more than 10 cycles of gates have been verified so far. For this reason, the Google team relied on simplified circuits (elided and patch) to indirectly estimate the Linear XEB of the supremacy circuits at higher depths.

Here, with our multi-tensor contraction algorithm, we have successfully verified all ABCD supremacy circuits with 12, 14, and 16 cycles using only moderate computing resources (few GPUs). Based on our results, we conclude that Google’s estimated XEB (based on simplified circuits) contains about 4% deviation. The data produced by our algorithm is available online [28]. If our algorithm was implemented on the Summit supercomputer, 16 cycles would only take 10 mins. Furthermore, we estimate that for verifying the 3 million bitstrings from the 20-cycles supremacy circuits, it would only require 7.5 days, which is several orders of magnitude lower than previously estimated (e.g. 79 years with the approach in Ref. [11]).

The rest of the paper is organized as follows. First, we briefly recall some standard definitions and notations related to tensor networks. Second, we discuss contraction trees and how to estimate their computational cost. After that, we describe our new efficient method for finding multiple amplitudes and batches of amplitudes, which can be used in combination with any TN based contraction algorithm. Finally, we demonstrate our experimental results on the verification task.

### 2 Definitions and notations

To get started, let us summarize the related concepts in TNs necessary for our discussion. Here a tensor of order $r$ is a multi-dimensional array $T[i_1, \ldots, i_r] \equiv T[i]$ with complex entries, where the indices $(i_1, \ldots, i_r) \equiv i$ are usually called legs, and the dimension of each leg is called its bond dimension. The shape of the tensor
where the sum is over all possible values of the legs

\[ T[i_1,\ldots,i_s] \] is the vector \((d_1,\ldots,d_r)\), where each \(d_j\) is the bond dimension of the tensor leg \(i_j; j = 1, r\). For example, a vector \(T[i_1]\) of length \(n\) is an order 1 tensor of shape \((n)\), and an \(m \times n\) matrix \(T[i_1,i_2]\) is an order 2 tensor of shape \((m,n)\).

Later, we would be interested in evaluating the summation of a collection of tensors \(T_1[i_1],\ldots,T_m[i_m]\) sharing some common legs,

\[
\text{sum} = \sum_{j_1,\ldots,j_s} T_1[i_1] \cdots T_m[i_m],
\]

where the sum is over all possible values of the legs \(j_1,\ldots,j_s\), which we call the closed legs. All the rest legs of the tensors \(T_1,\ldots,T_m\) are called open. As one can see, a tensor network is equivalent to the graphical representation of the summation.

Formally, it can be represented by a hypergraph \(\mathcal{N}\), where each tensor is denoted by a vertex, each leg is denoted by a hyperedge connecting all the related tensors. We call the sum (2) the result of contraction for \(\mathcal{N}\) denoted by \(\Sigma\mathcal{N}\). Furthermore, we also need to specify a subset \(\text{Op}(\mathcal{N})\) of open legs. For example, in Fig. 1(a) we have a tensor network \(\mathcal{N}\) that corresponds to the following sum:

\[
\sum_{i,j,k,l,m} T[i,j]S[i,k]U[j,k,m]Q[m,l]R[l,n],
\]

where the open leg \(n\) (shown in red) is not involved in the summation; therefore \(\text{Op}(\mathcal{N}) = \{n\}\). Note that tensor networks can be also viewed as factor graphs, which are widely used in the context of error-correcting codes and statistical inference [29, 30].

3 Tensor network contraction

For simplicity, in what follows, we shall consider only tensor networks that are represented by graphs, i.e. each leg connects at most two tensors, and it is open whenever it connects to only one tensor. However, all the algorithms described below also work for arbitrary tensor networks. Suppose we have a pair of tensors \(T[i_1,\ldots,i_n]\) and \(S[j_1,\ldots,j_m]\) in a tensor network \(\mathcal{N}\) and a total of \(q\) common closed legs in the set. We can define their contraction denoted by \(T*S\) as follows:

\[
T*S = \sum_{\text{closed legs}} T[i_1,\ldots,i_n] \cdot S[j_1,\ldots,j_m].
\]

In other words, the contraction of two tensors corresponds to merging the corresponding vertices in the tensor network. Note that we would omit the index \(\mathcal{N}\) if the tensor network is clear from the context and just write \(T*S\).

It is not hard to see that if a tensor network \(\mathcal{N}\) consists of tensors \(T_1,\ldots,T_n\), then the result of its contraction \(\Sigma\mathcal{N}\) does not depend on the way we order the tensors and use parentheses. For example, for the tensor network from Fig. 1(a) we can use the following expression:

\[
\Sigma\mathcal{N} = ((T*U)*S)*(R*Q).
\]

The same result can be obtained by any other expression that calculates \(\Sigma\mathcal{N}\), for example:

\[
\Sigma\mathcal{N} = ((Q*T)*(S*U))*R.
\]

However, from a practical point of view, a different contraction expression usually has different computational cost. This cost may be measured in the number of arithmetic floating-point operations such as addition and multiplication (FLOPs) and the number of tensor elements we read and write. Different contraction expressions also have different memory budgets. We can estimate from below the required memory size by the maximal size of intermediate results (i.e. the size of intermediate contractions) during the evaluation of the contraction expression. See Appendix A for more details on the contraction cost and memory size.

Each contraction expression can be naturally represented by a binary tree that is usually called the contraction tree [25, 26, 10]. In this tree, the leaves correspond to the tensors from the expression and the internal nodes to the contractions. For example, the tree in Fig. 1(b) corresponds to expression (5).

4 Multi-batch simulator

Before we proceed to our main algorithm, let us first introduce the concept of the contraction of multiple tensor networks. Note that both the computational complexity and the memory budget do not depend on the content of the tensors in the contraction tree. In fact, they only depend on the bond dimensions of the tensors \(T_1,\ldots,T_m\). Thus, it is helpful to consider formal expressions, where instead of some fixed tensors in the contraction expression we have variables \(X_1,\ldots,X_m\) that
denote arbitrary tensors of the same shapes as the tensors $T_1, \ldots, T_m$.

We can consider a contraction tree $\mathcal{T}$ with $m$ leaves also as a formal contraction expression $\mathcal{T}(X_1, \ldots, X_m)$. Hence we see that the contraction tree $\mathcal{T}$ is just a pictorial way to represent a formal contraction expression $\mathcal{T}(X_1, \ldots, X_m)$. Moreover, the subtrees $\mathcal{T}'$ of the contraction tree $\mathcal{T}$ for a contraction expression $\mathcal{T}(X_1, \ldots, X_m)$ represent its subexpressions $\mathcal{T}'(X_{p}, \ldots, X_{q})$. Hence in what follows we are going to identify formal contraction expressions and the corresponding contraction trees.

By a tensor network diagram we mean a tensor network $D$, where instead of fixed tensors $T_1, \ldots, T_m$ of some shapes we have variables $X_1, \ldots, X_m$ that correspond to arbitrary tensors of the same shapes. If we want to emphasize its variables, we denote a tensor network diagram as $D(X_1, \ldots, X_m)$. If we assign tensors $T_1, \ldots, T_m$ to the variables $X_1, \ldots, X_m$ we obtain the tensor network that we denote by $D(T_1, \ldots, T_m)$. The result of the contraction for this tensor network is denoted as $\Sigma D(T_1, \ldots, T_m)$. If $\mathcal{T}(X)$ is a contraction expression for $D$, then we can use it to perform this contraction, and obtain the result $\Sigma D(T_1, \ldots, T_m) = \mathcal{T}(T_1, \ldots, T_m)$.

In the literature, there are a number of algorithms [10, 11, 13] for optimizing contraction trees. In Appendix A we present our own optimization algorithm used to find contraction trees in this work. In all our experiments, we use a C++ implementation of this algorithm together with our own efficient library for TN contractions with GPU support.

In order to find $k$ different amplitudes (resp., batches), a common approach is just to run a single-amplitude (resp., single-batch) contraction algorithm $k$ times. However, this simple method is not efficient in the case when we need to find a large number (say $\sim 10^6$) of uncorrelated amplitudes or batches.

Below, we show that there exists a much more efficient way. If we are given a quantum circuit $C$, then we can convert it into a tensor network $\mathcal{N}_C$ in a standard way (see, for example, [20]). We also suppose that standard TN simplification techniques like gate fusion are already applied [31, 10]. This tensor network $\mathcal{N}_C$ has $n$ open legs, where $n$ is the number of qubits in our circuit (each open leg corresponds to one output qubit).

Let $D = D(X)$, $X = (X_1, \ldots, X_m)$, be the tensor network diagram for $\mathcal{N}_C$ with tensor variables $X_1, \ldots, X_m$, and $\mathcal{T}(X)$ is a contraction tree for $D(X)$. As it was already mentioned before, in a multi-amplitude simulation we find $k$ complex amplitudes $(s_i |0^n\rangle = \Sigma D(T^i); i = 1, \ldots, k$) for $k$ bitstrings $s_1, \ldots, s_k \in \{0, 1\}^n$. We can obtain this as the result of the contractions of $k$ tensor networks $D(T^1), \ldots, D(T^k)$, where each collection of tensors $T^i = (T^i_1, \ldots, T^i_m)$, $i = 1, \ldots, k$, corresponds to one bitstring $s_i$ (we assign its bits to the output legs of $\mathcal{N}_C$). If we have some contraction tree $\mathcal{T}(X) = \mathcal{T}(X_1, \ldots, X_m)$ for $D$, then we can use it to perform the contractions for our $k$ tensor networks $D(T^1), \ldots, D(T^k)$ and obtain:

$$\langle s_i | C | 0^n \rangle = \Sigma D(T^i); i = 1, \ldots, k.$$

If one needs to find multiple batches (each of $2^w$ amplitudes) we proceed in a similar way, but instead of the full contraction we do not contract $w$ legs that correspond to the non-fixed positions in each batch.

Hence we see that in a multi-amplitude and multi-batch simulation we evaluate the contraction expression $\mathcal{T}(X)$ on multiple collections of tensors $T^i = (T^i_1, \ldots, T^i_m)$, $i = 1, \ldots, k$. We call this multi-tensor contraction procedure since it produces $k$ tensors. The key observation is as follows: if one performs these $k$ contractions sequentially for $i = 1, 2, \ldots, k$, and we already evaluated some subexpression $\mathcal{T}'(X_p, \ldots, X_q)$ of $\mathcal{T}(X)$, then we can reuse the result next time when the values of the variables $X_p, X_{p+1}, \ldots, X_q$ are the same (see Fig. 2).

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{multi-tensor-contraction.png}
\caption{The main idea of the multi-tensor contraction: we can evaluate $\mathcal{T}'(X_p, \ldots, X_q)$ only once and reuse the result next time if the values of variables $X_p, \ldots, X_q$ are the same.}
\end{figure}

\section{Multi-tensor contraction algorithm}

Below we consider an algorithm for calculating $k$ contractions $\mathcal{T}(T^1), \ldots, \mathcal{T}(T^k)$ that stores the intermediate results of all its previous calls in a global cache $\mathcal{K}$. We further assume that $\mathcal{K}$ can be updated while the algorithm is running. The cache $\mathcal{K}$ can be implemented as a key lookup data structure. Here the key is a tuple $v = (T; T_1, \ldots, T_m)$, where $T = T(X_1, \ldots, X_m)$ is a contraction expression and $T_1, \ldots, T_m$ are the values of its variables $X_1, \ldots, X_m$. The value $\mathcal{K}(v)$ of the cache $\mathcal{K}$, corresponding to the key $v$, is equal to the result $\mathcal{T}(T_1, \ldots, T_m)$ of the expression $\mathcal{T}$ evaluation.
Algorithm 1: Multi-tensor contraction

\[ K := \emptyset \text{ (start with the empty global cache);} \]
for \( i := 1 \) to \( k \) do
\[
\text{Calculate } T(T^i) := \text{eval}(T, T^i, K);
\]
return \( T(T^1), \ldots, T(T^k) \);

on \( T_1, \ldots, T_m \). We also write \( K(v) = \text{null} \) if at the current stage we do not have the entry for the key \( v \) in the global cache \( K \).

Algorithm 1 shows the top level procedure that finds \( T(T^1), \ldots, T(T^k) \) for multiple collections of tensors \( T^i = (T^i_1, \ldots, T^i_m), i = 1, k \). We see that in this procedure we call \( k \) times the subprocedure \( \text{eval}(T, T, K) \), which, given the contraction tree \( T \), a collection of tensors \( T = (T_1, \ldots, T_m) \), and the intermediate results of the previous calls saved in \( K \), gives us \( T(T) \). Algorithm 2 shows a recursive definition of this subprocedure.

If we used this algorithm directly, then the cache size would be very big. However, one can significantly reduce it by reordering the collections of tensors \( T^1, \ldots, T^k \) in some special way, and deleting every cache entry \( K(v) \) immediately after the corresponding tensor was used for the last time. Let us describe how to achieve this. We assume that the variables \( X_1, \ldots, X_m \) from the top-level contraction expression \( T(X_1, \ldots, X_m) \) are enumerated according to their positions in \( T \). We also want to emphasize that each collection of tensors \( T^i = (T^i_1, \ldots, T^i_m) \) corresponds to an assignment of values to the variables \( X_1, \ldots, X_m \). Since we have \( k \) such collections each variable takes at most \( k \) different values, which we can enumerate for each \( X_j \), \( j = 1, m \). This allows us to put \( T^1, \ldots, T^k \) in the lexicographic order. To reduce the size of the cache \( K \) it can be split into the left and right parts \( K_L \) and \( K_R \) for storing the results of the left and right subexpressions in Algorithm 2, respectively. This splitting allows us to store in the left cache \( K_L \) at most one entry for each subexpression; and before we store \( K_L(T; T_1, \ldots, T_m) \), we can remove all keys \( (T; \ldots) \) from \( K_L \). The lexicographic ordering guarantees that the removed keys will not be used anymore.

To obtain a close-to-optimal contraction cost during the multi-tensor contraction we need to find a good contraction expression \( T \). The main characteristics that should be considered here are as follows:

1. Memory budget \( M = M(T) \), i.e., the amount of memory required for the simulation, including the cache size and memory for intermediate contraction results;
2. Computational complexity \( C = C(T) \), i.e., the number of floating-point operations (FLOPs), calculated as the sum of the complexities of all contractions in the contraction expression \( T \);

Algorithm 2: Procedure \( \text{eval}(T, T, K) \)

\[
\text{if } T = X_j \text{ then return } T_j; \]
\[
\text{Let } X_i, \ldots, X_m \text{ be the variables of } T; \]
\[
\text{if } K(T; T_{i_1}, \ldots, T_{i_k}) = \text{null} \text{ then} \]
\[
\text{Let } T = T_L \ast T_R; \]
\[
\text{// Recursively call itself on subtrees} \]
\[
U_L := \text{eval}(T_L, T, K); \]
\[
U_R := \text{eval}(T_R, T, K); \]
\[
\text{// perform the contraction operation} \]
\[
U := U_L \ast U_R; \]
\[
\text{// store the result } U \text{ to the cache } K \]
\[
K(T; T_{i_1}, \ldots, T_{i_k}) := U; \]
\[
\text{return } K(T; T_{i_1}, \ldots, T_{i_k}); \]

3. Parameter \( RW = RW(T) \), which is equal to the number of read-write operations from the memory for all contractions in the contraction expression \( T \).

The parameters \( C \) and \( RW \) should take into account how many times each subexpression is calculated in the worst case when we perform a multi-tensor contraction. For example, in the case of multi-amplitude simulation the complexity may depend on the number of calculated amplitudes. If we calculate \( 2^n \) amplitudes, and all the tensors in a subexpression \( T \) contain \( r \) legs corresponding to the circuit output, then this subexpression will be evaluated at most \( 2^{\min(r, m)} \) times. Some further details on the contraction expression optimization can be found in Appendices A, B, and C.

6 Verification of Google’s experiment

Using the described above multi-amplitude algorithm we verify Google’s results [7, 27] for up to 16 cycles using the samples (0.5M–2M samples per circuit) produced in Google’s experiment. We used 4 identical servers, each with the following configuration: 2 GPUs Tesla V100 with 16GB memory, \( 2 \times \) Intel(R) Xeon(R) Gold 6151 CPU 3.00GHz.

A link to the archive with the calculated amplitudes can be found here [28]. Based on this data we estimated the fidelity using the Linear XEB (see Table 1(a)). In Fig. 3 you can also see these fidelities for \( m = 12, 14, 16 \) together with the corresponding mean value and the standard deviation. As we can see, these results confirm the fidelities indirectly estimated in Google’s paper [7, 27].
Figure 3: The Linear XEB for all Google’s ABCD supremacy circuits for \(m = 12, 14, 16\). We show the \(\pm 5\sigma\) statistical error bars for each instance and the band corresponding to \(\pm \sigma\) around the mean fidelity, where \(\sigma = 1/\sqrt{k}\); \(k\) is the number of samples.

Table 1: (a) The linear XEB(%) of Google’s ABCD supremacy circuits for different number of cycles \(m = 12, 14, 16\); Google’s estimation of XEB is from [7, Table XI, Supplementary Information]. (b) The verification complexity of single amplitude (S) and multi-amplitude (M) simulators. The last column is the gain of the multi-amplitude simulator over multiple runs of the single amplitude simulator. The time is shown for one Tesla V100 16GB PCI-E. The number of FLOPs for each case is equal to \(2^m\) amplitudes. As we can see, the gain of \(S\) over \(M\) is the fidelity, \(f\) simulation on 1M cores with fidelity \(f\) [7, Table XI, Supplementary Information]. Here the factor \(f\) is because we assume that Summit is approximately equivalent to 5M cores. Let us note that this formula gives a slightly smaller qsimh running time estimate than the estimation from [7, Fig. S50, Supplementary Information].

We also verified all the EFGH circuits with 14 cycles and the number of qubits \(n < 53\). The results are shown in Fig. 4. We can see that the obtained XEB values (shown in red) are in good correspondence with the theoretical prediction (shown in green) from [7, Fig. 4].

The contraction cost of the verification task (the number of arithmetic operations with complex numbers) is the number of samples. As we can see, the gain of the multi-amplitude simulator over the multiple runs of the single-amplitude one is up to \(10^4\) in the hardest case \(m = 16\). In Table 2 we estimated the hypothetical running time of different algorithms for Summit supercomputer. For qsimh we used the formula \(0.2 \cdot \frac{1}{f} \cdot T_{sim}\); where \(f\) is the fidelity, \(T_{sim}\) is the running time of the qsimh simulation on 1M cores with fidelity \(f\) [7, Table XI, Supplementary Information]. Here the factor 0.2 is because we assume that Summit is approximately equivalent to 5M cores. Let us note that this formula gives a slightly smaller qsimh running time estimate than the estimation from [7, Fig. S50, Supplementary Information].

In the future we plan to verify some other cases as well. In fact, Table 2 shows that even in the case of \(m = 20\) cycles the verification of 3M samples can be done in several days on Summit supercomputer. We should note the running time of our algorithm depends on the maximal memory size required during the contraction. In all our estimations we assume that the GPU memory size is limited by 16GB. This is in a high contrast with the well known idea [9] to store all \(2^{53}\) amplitudes on hard drives. We also estimated that for modern GPUs with larger memory sizes, such as Tesla A100 80GB, it is possible to reduce the running time several times. Moreover, the third generation of tensor cores with better floating point precision, introduced recently in NVIDIA Ampere architecture, can improve the performance of our algorithm even further.

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Figure 4: The verification results for Google’s EFGH circuits with 14 cycles and the number of qubits $n < 53$. For each $n$ we found the Linear XEB for all 10 EFGH circuits (black dots) and calculated the corresponding mean value (red dots). The green curve shows the predicted XEB values from [7, FIG. 4].

![XEB fidelity vs number of qubits](chart.png)

Table 2: The estimated time on Summit supercomputer for different simulation algorithms possible to use for the verification of Google’s experiment: Google’s hybrid Shrödinger-Feynman (SFA) simulator qsimh (multi-amplitude, running time is scaled to 5M CPU cores) [7], Alibaba’s simulator [11, Table 1] (single-amplitude), and our TN contraction algorithm for single (S) and multiple (M) amplitudes. We assume that Summit has theoretical 400 PFlop/s single-precision ∼ 5M CPU cores with AVX-512. For all single-amplitude simulations the running time is multiplied by the number of samples.

| $m$ | #bitstrings | qsimh | Alibaba | Our(S) | Our(M) |
|-----|-------------|-------|---------|--------|--------|
| 12  | 0.5M        | 28 hours | 11 min | 5 min  | 14 sec |
| 14  | 0.5M        | 300 days | 73 min | 28 min | 1.1 min|
| 16  | 2M          | 133 years | 348 days | 66 days | 10 min |
| 18  | 2.5M        | 8,750 years | 4 years | 0.83 years | 1.4 hours |
| 20  | 3M          | 1,000,000 years | 66 days | 21 years | 7.5 days |

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A Contraction trees optimization

In this section we describe a new tensor contraction algorithm that finds contraction trees using local transformations.

When a tensor network is obtained from a quantum circuit, operating on qubits, all bond dimensions of the legs are equal to 2. In this case, the computational cost $C$ of elementary contraction operation (4) is easier to estimate: it involves $2^{r+r}$ multiplications and almost the same number of additions, where $r$ is the number of open legs in the result $T*S$. This is because we need to sum up $2^r$ terms and do it for all possible $2^r$ values of $r$ open legs.

On the other hand, the number of memory operations $RW$ is also an important parameter, since read/write operations of the tensors may become the bottleneck of the contraction in practice. As an estimation, let us consider the costs of reading the tensors $T$, $S$, and writing the result $T*S$. The total number of operations is simply $size(T) + size(S) + size(T*S)$, where $size(X)$ is the size of the tensor $X$, i.e. the product of all bond dimensions of its legs.

It is important to note that for the best overall performance of the contraction algorithm it is wise to take into account that the memory speed and the computation speed on particular hardware are not the same. Hence we need a parameter during our optimization algorithm that encodes the ratio of these two speeds. This optimization parameter is called the arithmetic intensity [33, Sec. 4.2.2]. We define it as the ratio of computational complexity (the number of elementary floating-point operations) to the number of memory read/write operations during the tensor contraction. For example, in GPU Tesla V100 this value is approximately equal to 16. Hence the arithmetic intensity is a device-dependent parameter, which is different for different hardware.

For optimization, we use the following objective function that tries to combine all the above characteristics:

$$f(T) := \beta \max \left( \log_2 \left( \frac{M}{M_{\text{max}}} \right), 0 \right) + \log_2(C + \alpha \cdot RW)$$

where $M_{\text{max}}$ is the upper limit on the memory size in Bytes (our memory budget); $\alpha$ is the arithmetic intensity; $\beta$ is the penalty factor for running out of memory, i.e., $\beta$ controls the weight of memory size in the objective function. If the memory budget is more important, we should increase the value of $\beta$.

To find a close-to-optimal contraction tree, we need an optimization algorithm that tries to minimize the objective function $f(T)$. In this work we use simulated annealing but any other local search algorithms such as hill climbing can be used as well (see [34, Chap. 4] for a review of local search methods). By a local search method here we mean a combinatorial optimization method that given an objective function $f : X \rightarrow \mathbb{R}$ on the search space $X$ of all possible states try to apply a small fixed number of local transformations $L = \{l_1, \ldots, l_n\}$ (each transformation $l_i$ is a function $l_i : X \rightarrow X$) starting usually from some random or predefined state $x_0 \in X$. Hence we obtain a sequence of states $x_0, x_1, \ldots, x_N$, where each next state $x_{i+1}$ is obtained from the previous state $x_i$ using one of the local transformations from the set $L$, i.e., $x_{i+1} = l(x_i)$ for some $l \in L$. The choice of the local transformation $l \in L$ on each individual step is usually governed by the gain

$$\Delta f(x_i, l) := f(x_i) - f(l(x_i))$$

that we obtain in terms of the objective function $f$. The local search usually stops when it reaches a state $x_N$ that cannot be improved locally (i.e., $\Delta f(x_i, l) < 0$ for all $l \in L$) or the maximal number of steps is reached. There are many other details on how a local search can be done. For example, in the simulated annealing method, we choose local transformations randomly with the probability that depends on the gain $\Delta f(x_i, l)$. At the same time, in the hill-climbing method, one can choose a local transformation deterministically in a greedy fashion (i.e., choose the local transformation which gives the best possible gain).

It can be easily checked that the contraction operation $T*S$ (as a binary operation on tensors) satis-
This way we need to find the contraction of the network such that all intermediate tensors are placed in the memory of the device on which the contraction is performed. In the end, we obtain the result of the entire network contraction.

In the proposed optimization methods it is very easy to take into account the implementation details by a slight modification of the objective function. We can use this to fine-tune the contraction tree and slicing obtained by other optimization methods to better fit some particular hardware and software. For example, if there is an efficiency profile for a given system, then we apply these two additional steps not very often, and the overall running time of our local search method is almost unchanged.

In a tensor network, several legs are fixed to reduce the memory size used by the contraction algorithm. We can fix some legs in the tensor network or to slicing. We propose the following slight modification to the above local search algorithm. We start with the empty list $S$ of legs used for slicing and every $K$ steps of the local search method we update $S$ by applying with probability $1/2$ one of the following two additional steps:

1. add to the list $S$ the leg that results in the best memory budget $M$ reduction;
2. remove the random leg from $S$.

Let us note that the objective function during our local search method requires only a local update on each step, and thus can be implemented very efficiently. However the same task for these two additional steps usually requires a global update of the objective function. Nevertheless if $K$ is quite big (e.g., $K = 10^3$), then we apply these two additional steps not very often, and the overall running time of our local search method is almost unchanged.

In a tensor network diagram (see Fig. 8(b)), in this tensor network diagram $D(X_0, \ldots, X_8)$, for simplicity, we denoted the legs by $T$. Figure 7: Slicing of the leg $v$.

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the numbers 0–7, and the open legs by the numbers 8–10.

If we fix three binary values \( s_1, s_2, s_3 \) of the output qubits (i.e., we fix the values of the open legs 8, 9, 10), then we fix the values \( T_0, \ldots, T_8 \) of all tensors variables \( X_0, \ldots, X_8 \) in the diagram \( D \), and the complex amplitude \( \langle s_1 s_2 s_3 \mid C \rangle \) for the bitstring \( s_1 s_2 s_3 \) is equal to the result of the contraction: \( \Sigma D(T_0, \ldots, T_8) = \Sigma D(T) \), where \( T = (T_0, \ldots, T_8) \).

Now suppose we want to find the complex amplitudes for the following 3-bit strings: 000, 011, 111. For example, to demonstrate our algorithm, we can use the following tree \( T \) given by the contraction expression:

\[
T(X_0, \ldots, X_8) = ((X_0 \otimes X_3) \ast (X_1 \otimes X_5)) \ast ((X_2 \otimes X_4) \ast (X_6 \otimes X_8)) \ast X_7
\]

for the quantum circuit \( C \). In order to find our \( k = 3 \) complex amplitudes \( \langle s_1 s_2 s_3 \mid C \rangle \) for the bitstrings \( s_1 s_2 s_3 \in \{000, 011, 111\} \) we need to find \( T(T^1), T(T^2), T(T^3) \), where each vector of tensors \( T^i = (T_0, \ldots, T_8), i = 1, 2, 3 \), corresponds to our three bit strings 000, 011, 111, respectively.

In Fig. 8(c) you can see the annotated contraction tree \( T \), where for each internal tree node that corresponds to a contraction we show the legs from 0–7 (we sum up over them in this contraction) and the open legs from 8–10 (the values of these legs are fixed when we fix the bitstring \( s_1 s_2 s_3 \)).

For the open legs, we also show their possible values. The number of these values shows us how many times we need to perform the contraction for this subtree. For example, for the subtree \( (X_0 \otimes X_3) \ast (X_1 \otimes X_5) \) we do not have open legs, hence we need to calculate it only once when we find \( T(T^1) \), and reuse the result in \( T(T^2), T(T^3) \). At the same time, for the subtree \( (X_2 \otimes X_4) \ast (X_6 \otimes X_8) \) we have two possible values (00 and 11) for open legs 9 and 10; hence we need to contract this subtree twice. However, if we used 3 times single-amplitude simulator we would need to contract each subtree three times.

C Details of Multi-tensor algorithm

Here we give a more detailed description of the multi-tensor algorithm where we want to evaluate a contraction expression \( T(X) \) on several tuples of tensors \( T^i = (T^i_1, \ldots, T^i_m), i = 1, \ldots, k \). Let us remind that in this algorithm we have two look-up data structures \( K_L \) and \( K_R \) that we call caches. Here the keys correspond to the subexpressions of the contraction expression \( T \), while the values in the cache \( K_L \) are tensor, and the values in the cache \( K_R \) are mappings from tuples of integers to tensors. Let us denote by \( K_R(v; t) \) the value of the mapping \( K_R(v) \) on the tuple of integers \( t \).

If we have a collection \( T = (T^i)_{i=1}^k \) of input arguments, then each variable \( X_j, j \in [m] \), in the contraction expression \( T(X_1, \ldots, X_m) \) takes finite number of different values. Let \( V_j \) be the collection of different tensors that the variable \( X_j \) can take, and consider \( n_j = |V_j|, V = (V_j)_{j=1}^m \). Hence, each tuple \( T^i \) is uniquely determined by the tuple of indices \( t^i \in \mathbb{N}^m \) such that \( t^i_j \in [n_j] \) and \( T^i_j = V_j[t^i_j] \) for all \( j \in [m] \).

The multi-tensor contraction procedure eval_all (Algorithm 3) takes the \( m \)-tuple \( V \) of sets of tensors, a set \( t \) of \( m \)-tuples of indices, and a contraction expression \( T \). It sorts the set \( t \) in the lexicographical order, creates caches \( K_L \) and \( K_R \), and sequentially for \( i = 1, \ldots, m \) calls procedure eval, which recursively evaluates (reusing temporary results stored in caches) the contraction expression \( T \) on one tuple of tensors defined by \( t^i \). The procedure eval_all returns the dictionary \( R \) where \( R(t^i) = T(t^i_1, \ldots, t^i_m) \). In the algorithm it is assumed that the variables of \( T \) are enumerated in the same order as they occur in \( T \).

By \(|t|\) we denote the number of elements in the set \( t \). If \( X_{j_1}, \ldots, X_{j_r} \) are the variables of the subexpression \( T' \) (if \( X_{j_i} \) occurs in \( T' \) earlier than \( X_{j_j} \)), then \( i < j \), then we will use the following notations:

\[
t_{T'} = (t^i_{j_1}, \ldots, t^i_{j_r}), \quad t_{T'} = (t_{T'})_{i=1}^{|t|}, \quad V_{T'} = (V_{j_1}, \ldots, V_{j_r}).
\]
Algorithm 3: Procedure eval_all(\(\mathcal{T}, V, t\))

```plaintext
// Initialize the caches \(K_L, K_R\) and the dictionary \(R\)
\(K_L := \emptyset, K_R := \emptyset, R := \emptyset;\)
Lexicographically sort \(t;\)
for \(i := 1\) to \(|t|\) do
\(R(t^i) := \text{eval}'(\mathcal{T}, V, t, i, i + 1, K_L, K_R);\)
return \(R;\)
```

Algorithm 4: Procedure eval'(\(\mathcal{T}, V, t, i, i'\), \(K_L, K_R\))

```plaintext
if \(\mathcal{T} = X_j\) then return \(V_j[t^i_j];\)
if \(i = 1\ or t^i_{T} \neq t^{i-1}_{T}\) then
Let \(\mathcal{T} = \mathcal{T}_L * \mathcal{T}_R;\)
if \(K_R(\mathcal{T}) = \emptyset\) then
// Call full multi-tensor contraction on the right subtree
\(K_R(\mathcal{T}) := \text{eval_all}(\mathcal{T}_R, V_{T_R}, t_{T_R});\)
// Recursive call on the left subtree
\(U_L :=\)
\(\text{eval}'(\mathcal{T}_L, V, t, i, i' | t^i_T = t^{i-1}_T\} + 1, K_L, K_R);\)
\(U_R := K_R(\mathcal{T}; t_{T_R});\)
// perform the contraction operation
\(U := U_L \ast U_R;\)
if \(i' = |t|\ and t^i_T = t^{i'}_{T}\) then
// Store the result in the cache to use it on the next step
\(K_L(\mathcal{T}) := U;\)
if \(i' > |t|\) then \(K_R(\mathcal{T}) = \emptyset;\)
return \(U;\)
else return \(K_L(\mathcal{T});\)
```

If \(\mathcal{T} = \mathcal{T}_L * \mathcal{T}_R\), then \(t^i_T = (t^i_{T_L}, t^i_{T_R})\) where \(t^i_{T}\) is some permutation of \(t^i_{T_R}\). Hence, if \(t^i_{T}\) is sorted lexicographically, then \(t^i_{T_L}\) is also sorted lexicographically, therefore in each call of \(\text{eval}'\) the set \(t^i_{T}\) is sorted lexicographically. Hence, the result of the evaluation of \(\mathcal{T}\) on the input tuple \(t^i_{T}\) should be stored in the cache only if \(t^i_{T} = t^j_{T}\) where \(j\) is the value of the parameter \(i\) in the next call of \(\text{eval}'\) for the subexpression \(\mathcal{T}\); otherwise \(j > i\) for all \(j \geq i\) and in this case we do not need to store the result in the cache \(K_L\). The parameter \(i\) for the root expression is equal to \(i + 1\) since the next call from \(\text{eval_all}\) will be with the parameter \(i + 1\). For the subexpression \(\mathcal{T}_L\) of the expression \(\mathcal{T} = \mathcal{T}_L * \mathcal{T}_R\) the parameter \(i\) is the first number after \(i\) for which the condition in the second line of Algorithm 4 is true (i.e. \(t^i_{T} \neq t^{i-1}_{T}\) or \(|t| + 1\) if this condition will be always false. Hence we get

\[i' = \min\{i' \mid i' > |t| or t^i_{T} \neq t^{i'}_{T}\} = \max\{i' \mid t^i_{T} = t^{i'}_{T}\} + 1.\]

**Complexity estimation.** For our optimization procedure we need to efficiently estimate the complexity and the memory used in Algorithm 4. Suppose we know the sets \(V_i\) and the number \(k\) of input tuples in \(\mathcal{T}\). Consider a subexpression \(\mathcal{T}'\) of \(\mathcal{T}\) and its variables \(X_{j_1}, \ldots, X_{j_s}\). This subexpression will be evaluated \(|t_{T'}|\) times. Since the variable \(X_{j_i}\) takes values from \(V_{j_i}\), it can take at most \(|V_{j_i}|\) different values. Hence the expression \(\mathcal{T}'\) will be evaluated at most

\[k_{T'} = \min\left(\prod_{j=1}^{s}\left|V_{j_i}\right|, k\right)\times.\]

Therefore, we can estimate the complexity recursively:

1. if \(\mathcal{T} = X_j\), then \(C(\mathcal{T}, k) = 0\) (in this case we do not perform the contraction)
2. otherwise \(\mathcal{T} = \mathcal{T}_L \ast \mathcal{T}_R\) and \(k_{T'} \leq \min(k_{T_L}k_{T_R}, k)\).

Thus, the values \(k_{T'}\) can be efficiently updated with the complexity \(O(1)\) after a local transformation of the contraction tree.

For the multi-tensor simulation, the contraction cost \(C\) depends not only on the contraction expression \(\mathcal{T}\) but also on the maximal number \(k\) of the input tensor tuples. The total contraction cost \(C(\mathcal{T}, k)\) can be estimated as follows:

1. if \(\mathcal{T} = X_j\), then \(C(\mathcal{T}, k) = 0\) (in this case we do not perform the contraction)
2. otherwise \(\mathcal{T} = \mathcal{T}_L \ast \mathcal{T}_R\), and we have

\[C(\mathcal{T}, k) = C(\mathcal{T}_L, k) + C(\mathcal{T}_R, k) + k_{T'}C(\mathcal{T})\]

where \(C(\mathcal{T})\) is the cost of the contraction in the root of \(\mathcal{T}\) (the contraction of the tensors \(T_L\) and \(T_R\)), which can be easily calculated from the set of legs of these tensors.

Note that \(k_{T'}\) depends only on the set of variables in the expression \(\mathcal{T}\) and does not depend on the evaluation order of the expression \(\mathcal{T}\). The complexity \(C(\mathcal{T}_L \ast \mathcal{T}_R)\) depends only on the set of output legs of the result of the evaluation of \(T_L\) and \(T_R\) and does not depend on the order of the evaluation of \(T_L\) and \(T_R\). Hence, when there are some local changes inside the subexpression \(\mathcal{T}\) the complexity gain can be recalculated locally.

When we apply a local transformation to \(\mathcal{T} = (T_1 \ast T_2) \ast T_3\) and obtain \(\mathcal{T}' = T_1 \ast (T_2 \ast T_3)\) the subtrees \(T_1, T_2, T_3\) remain the same. Taking into account the new subexpression \(T_2 \ast T_3\) and \(k_{T'} = k_{T'}\), the difference in the complexity can be calculated as follows:

\[C(\mathcal{T}, k) - C(\mathcal{T}', k) = k_{T_L}k_{T_3}C(T_1 \ast T_2) - k_{T_L}k_{T_3}C(T_2 \ast T_3) + k_{T'}(C(T) - C(T')).\]
Memory estimation. In the previous paragraph, we showed how we can locally recalculate the computational cost of the contraction after a local transformation in a contraction tree. However, it is much harder to recalculate the memory size. Below we propose a fast algorithm giving us a heuristic estimate $M(T, k)$ of the memory used in the contraction algorithm $\text{eval\_all}(T, V, t)$.

By $m(T)$ we denote the size of the contraction result for an expression $T$. Below we assume that the subexpression $T$ is evaluated exactly $k_T$ times and use the following observations for this case:

1. If $k_T = 1$, then $T$ is evaluated only once, and hence the cache is not used for storing the subexpression evaluation results.

2. If it is necessary, then the left and right subexpressions can be swapped without any changes in the complexity.

3. For each subexpression $T = T_L * T_R$ in the cache $K_L$ there is at most one entry, and in the cache $K_R$ there are all $k_{T_R}$ entries.

4. The total memory for the temporary results (excluding the caches) is approximately equal to $2 \max_{T' \subseteq T} m(T')$ (in the worst case usually a large tensor is contracted with a small tensor, and the result is again a large tensor of the same shape).

Taking into account the above observations, for an expression $T = T_L * T_R$ we define:

$$m_k(T) = k_T m(T),$$
$$m'(T) = \min(m_k(T_L) + m(T_R), m(T_L) + m_k(T_R)), $$
$$m''(T) = \min(m_k(T_L), m_k(T_R)), $$
$$m_K(T) = \begin{cases} 0 & \text{if } k_T = 1, \\ m'(T) & \text{if } \min(k_{T_L}, k_{T_R}) < k_T, \\ m''(T) & \text{if } k_{T_L} = k_{T_R} = k_T, \end{cases}$$

$$M(T, k) = \sum_{T' \subseteq T} m_K(T') + 2 \left( \sum_{T' \subseteq T} m^p(T') \right)^{1/p},$$

where $p \geq 1$ is the approximation parameter. Here we approximate the norm $\| \cdot \|_\infty$ by the norm $\| \cdot \|_p$ to make the target function smooth and locally updatable.

Note that this algorithm does not give the exact memory size. Instead, it calculates only an approximate value for the optimization procedure. To get the exact memory size one can run Algorithm 3 in an emulation mode, i.e., with a virtual memory allocator, which only calculates the memory size without any real memory allocation. One can also use dummy tensor contractions where only the tensor shapes are calculated.