Conceptual Improvisation on Low Power Mitigation for Domino Logic Systems using CHSK Domino Logic

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Abstract

Background/Objectives: In VLSI technology, the design provides low-power static random access to various applications and also performs with less energy and design implementation reduces the burden and also manages the delay. Methods/Statistical Analysis: The mixed domino high-speed circuit was designed with a wide domino logic circuit with a multiplexer. We propose a wide domino logic circuit of CHSK domino logic circuits to improve the performance of the parameters like Power, Delay, Unity Noise Gain, Power Delay Product and Robustness. Findings: The technique used in domino logic circuit designs and usage of higher order multiplexer of a modular design is presented and implemented by constructing a multiplexer. Simulation is done using Cadence CMOS process using Virtuoso tool. Application/Improvements: The proposed circuit improves unity noise gain, delay and power along with better performance as compared to Conditional Keeper and High Speed domino logic circuit of existing domino logic systems.

Keywords: Delay, Domino Logic, Keeper Circuit, Power, Unity Noise Gain and Power Delay Product.

1. Introduction

Nowadays, the logic circuit methodology is used for high performance in integrated circuit design. Dynamic logic of the device is exploiting from the static logic, which deliberate the information of capacitances in the circuit design. Logic Circuit is rapid access than the static in counterparts, toggle rate and power consumption. Based on trade-offs the consumption is defined and the toggle will be smaller in the logic circuit.

The methodology of dynamic design is distinguished usually when it refers to logic family like SOI design. In combinational or integrated logic circuit the clocked logic used in sequential logic circuit for synchronize transitions. To refer the memory device in logic circuit the dynamic terminology is used but not confuse with objectives. When compared to a logic circuit, the Domino logic requires less area and faster than the static CMOS logic. It is used in a high performance critical system such as microprocessor, multiplexer etc.

As the technology is scaled down, supply voltage is reduced which reduces the power consumption. The threshold voltage is also scaled to maintain the required performance. Low threshold voltage of the transistor, increase the sub-threshold and gate oxide leakage current. However, low threshold voltage makes the domino circuit to become more prone to input noises. These give the lowest of the delay and power, but have noise immunity. Circuits use more voltage at the source of the pull down network in the standby mode.

The main sources of noise signal in circuits are crosstalk, leakage current and supply noise. These noise signals reduce the robustness of the domino circuit. High leakage current discharges the dynamic node and make the logic failure of the domino circuit. Keeper provides immunity against noise and leakage current. Conventional method
to increases the robustness of the domino logic circuit is by upsizing the keeper ratio. The keeper ratio $K$ is defined, as the ratio of the current driving capability of the keeper transistor to the evaluation transistor $K = \frac{P^{(W/L)\text{keeper transistor}}}{n^{(W/L)\text{Evaluation Transistor}}}$.

Where $W$ and $L$ denote the Width and length size of a transistor, $p$ and $n$ are the mobilities of hole and electron, respectively. By increasing the value of $K$, it improves the robustness. Between the keeper and the pull down network it increases the conflict current which increases the short circuit power consumptions. The delay of the domino circuit is increased by upsizing of keeper has a tradeoff between speed and robustness $6,7$. So it increases the speed and power consumption of the domino circuit and it not a reliable solution.

Dynamic logic is harder to work for speeding process, there is no other choice than the domino logic system. Also difficulties in designing and verifying the circuit class and from this it become more sensitive to both clock skew and charges sharing among the domino logic. It is over two times faster than normal logic to compute logic by using fast N transistors and since Static logic uses slow P transistors it becomes slower. It has created a extensive interest owing to its CMOS power consumption needs and performance. It has lower switching threshold operations and lower input capacitance of the same output current, so it runs 1.5 times to 2 times faster than the static logic.

The remainder of the paper is organized as follows. Related surveys are discussed with the previous circuit techniques in section 2. The proposed circuits are explained in section 3 and the Simulation results and analysis are presented in section 4. Finally, concludes the proposed work in section 5.

## 2. Literature Survey

In this section the survey related to the domino circuits are discussed. It is widely used to achieve higher in speed, smaller in area and potentially lower power consumption in custom circuit design due to glitchfree-operation. Domino logic circuits can implement the circuit, which typically involves the conversion from the original binate logic network to a unite representation.

Domino circuits are more intricate than that of static circuit and the added difficulty is because it is monotonic in nature $8$. It can be mapped to a non-inverting function network, where logic inversions are needed and at either primary input and/or output it must performed $9$. The leakage power is reduced in Wallace tree multiplier by using full adders instead of half adder. Due to multiplexer operational mode the leakage power is relatively high. A logic circuit is designed to reduce more leakage power by implementing Wallace tree multiplier $10$.

High Speed Domino Logic (HS Domino) is similar to standard domino footless keeper except keeper is connected to the output through the CMOS transistor. In the evaluation phase, the keeper transistor will be OFF if the output of delayed clock is low. When any one input is high in circuit, dynamic node is discharged to the ground, keeper transistor remains OFF and the output is charged to high. After a delay of inverter, transistor is ON and again it becomes OFF. The contention current problem is solved by this circuit. Similarly, it maintains the dynamic node VDD against charge sharing and leakage $11$.

In Conditional-keeper Domino Logic (CKD), fixed keeper and conditional keeper are used. When a clock is low, dynamic node is charged to VDD, week keeper turns ON and other turns OFF. In the evaluation phase beginning the clock goes low to high and after a delay the keeper gets activated. If the dynamic node is high, then the conditional keeper turns ON. The conditional keeper improves noise immunity of the circuit. The noise immunity is maintained for high performance and better noise immunity by providing small contention current to the pull down network.

In paper $12$, proposed a technique that the diode is connected in series with the footer to enhance the robustness of the circuit. For improving the speed, current mirror is employed in the pull down network to increase the current evaluation. Simulation is done in 65nm technology for 64 bit input. When comparing to standard footless domino under the same delay it improves robustness by 17.7× and 10.6× as compared to conditional keeper domino.

In Noise Immunity Metric $13$ by applying the noise pulse the immunity of the domino circuit is measured. In static, the noise amplitude is same in output, but noise amplitude is varied based on the output. In this measurement, the noise pulse duration is kept 30ps (for 45nm technology). Unity noise gain is a comparison between the leakage and noise robustness. It provides same amplitude at the output. The UNG metric is given by $\text{UNG} = \{V_{\text{noise}}; V_{\text{noise}} = V_{\text{out}}\}$
Dynamic node of the footless domino circuit is very sensitive to noise. The dynamic node is discharged due to the noise signal. During evaluation phase dynamic node must be stable. By adding a transistor at the source of the pull down network it becomes footed domino logic circuit. It minimizes current leakage due to stacking effect at the cost of speed. For wide fan-in FDL circuit does not show more robustness. Several circuit techniques have been proposed in the literature such as High Speed Domino, the conditional keeper domino circuit etc\textsuperscript{14,15}. Main idea regarding these circuit designs to improve circuit performance and noise robustness.

The Filtered Switch Domino and Multi Dynamic Node Domino logic systems clocked logic is a design methodology in the combinatorial logic circuit. It can be two times faster than static logic because it has twice the thresholds higher, capacitive loading, and uses slow P transistors. Dynamic logic is harder to work with increased processing speed. Another conventional method is using high threshold voltage transistor at the expense of speed to improve robustness\textsuperscript{16,17}. To deal with these issues different techniques are proposed and High Speed and Conditional Keeper Domino logic are effective technique when compared to conventional footless domino logic. In this paper, new domino logic circuits are proposed with better performance than the existing system.

3. Proposed Work

In this section, the proposed domino logic circuit is proposed and designed to improve the speed, power consumption and to reduce noise immunity. The proposed modified circuit consists of same pull-up network. In order to improve the speed, the reset block of one or more additional transistor is connected in series. In the evaluation phase, the control input to the terminals plays a vital role in making the output to 0 V.

The domino logic circuit of High Speed with keeper contains the process by the combination of delayed clock and the output node. In the evaluation phase, the transistor turns off if the clock is high. So, the turning off process reduces in evaluation mode. The High Speed domino logic circuit is designed with the OR gate. For better speed the evaluation network turn on only if it high and its turn off once delay occur. The issues of the High Speed Domino logic are the improvement of noise on the stage of input and the dynamic nodes provides negative results by getting discharged. In order to overcome the challenges and to have better performances the High Speed domino logic circuit is needed to improve or redesign the circuit.

As well as, the domino logic of the Conditional Keeper circuit with keeper employ with the large as well as small keeper. This logic function process at the stage of pre-charge and it turns on the transistor pull up only if the clock is at low level. Also, it will be high in the beginning of the evaluation phase, so that the keeper and transistors will be off. In Conditional Keeper logic noise margin is improved in the circuit and delay of the circuit is increased by the inverters and the gate. In order to have improved and to reduce the delay and noise in the circuit the logic has to be reformed.

3.1 Proposed – High Speed Domino Logic Circuit

The domino logic of the High Speed technique is restructured to improve the performance and speed. In existing system the circuit is designed with the OR gate with keeper and without a keeper. It specifies the process of the work as mentioned in the survey. The proposed circuit is designed with multiplexer in order to show the performance with less power consumption and better performance.

The proposed High Speed domino logic schematic is shown in Figure 1. The processing steps are carried out...
with the existing technique and multiplexer was used to improve the performance. At the start of the evaluation phase, when clock mode is switched to high, PMOS will ON, so the keeper transistors will turn OFF. Again the PMOS will OFF after the delay for the inverters. If the output is high, then the dynamic node is discharged to ground and the NMOS transistor will remain OFF.

As well as if the dynamic node is higher, then the transistor is turned on and low the pull down network. However, since the transistor is disabled in the evaluation phase and the dynamic node is floating at the beginning itself. Without keeper the evaluation node will be discharged if there is noise in the inputs.

3.2 Proposed - Conditional Keeper Domino Logic Circuit

The Conditional Keeper domino logic is also like High Speed domino circuit restricted with a proposed circuit for better output with less immunity noise by the presence of multiplexer in the circuit. The schematic circuit of the conditional keeper is shown in Figure 2.

In the evaluation phase beginning, the dynamic node state is maintained by keeping the smaller keeper ON. Even after the inverter delay the dynamic node is still high, then the output goes low to turn ON it. The keeper transistor is sized larger to maintain the dynamic node state for the rest of the evaluation phase. However, it remains OFF if node is discharged to the ground. The fixed keeper and conditional keeper are powerful keeper supply. Dynamic node charge to VDD once the clock is Low.

In the beginning of the analysis section the clock is low to high. The conditional keeper improves noise immunity of the circuit. Weak keeper provides tiny conflict and current to the pull down network. This improves the circuit speed and it’s additionally decent to take care of the noise immunity throughout transistor Keeper.

3.3 Proposed - CHSK Domino Logic Circuit

From the proposed High Speed and Conditional Keeper domino logic circuit the performance of the circuit is improved. By combining the circuit, the performance of the circuit gets better. The schematic of the proposed combined circuit of proposed High Speed and Conditional Keeper domino logic is shown in Figure 3a. In this circuit the noise immunity is improved with high speed of the circuit and less power. By upsizing inverters delay the noise immunity is improved. For higher the noise immunity performance, the process is made to the dimensions of pull down network.
In the evaluation phase, the clock signal is assumed to be in the mode of standby only if it is low. As well as the devices of PMOS and the transistor will be turned off during the mode of precharge and the clock is swapped to high from low. The source voltage of the transistors will be decreased if the transistors are in off condition. The node becomes discharged by the on state of transistor gate. If the voltage of DC increased then the transistor gate source voltage will be decreased. By the effects of stacking the leakage current of sub threshold will decrease.

The proposed combined circuit without keeper is shown above in the Figure 3b. Unity noise gain is the important parameter for noise immunity measurement and noise pulse is given as input. In evaluating the immunity the pulse amplitude will be varied. The unity noise gain, power consumption and delay of power consumption are the parameter to normalize the value of domino circuit to show better performance of the circuit. The multiplication of the average power and the delay is defined as the Power Delay Product (PDP).

4. Simulation Results

In this section the analyses of the proposed work was simulated at an operating voltage of 0.7 Volts. The proposed circuits garbage input/output is consummate using the virtuoso tool of the cadence and the outputs are simulated. The purpose of the analysis is to set transient analysis of the domino logic to reduce the power consumption and noise immunity. Also define modes of operation and comparison of logic circuit with existing system to prove the efficiency and better performance. The comparison of delay of various domino logic for wide fan-in OR gates and proposed circuit with multiplexer are illustrated.
Here multiplexer is designed by current domino logic in proposed circuit. From the simulation results, by reducing the half of the dynamic power dissipation in the proposed work circuit is concluded that the total leakage power has been drastically reduced.

Figure 4 shows the analysis of the proposed High Speed domino logic circuit and the simulated results prove that the performance of the power, speed and noise immunity is better than the existing logic circuit. As well as the proposed Conditional Keeper domino logic is shown in Figure 5 which is the proposed combined circuit of High Speed and Conditional Keeper domino logic is called as CHSK Domino Logic circuit. The analysis of Proposed combined circuit – CHSK Domino Logic circuit is shown in Figure 6.

Table 1. Comparison of various domino logic circuits

| Domino Logic          | No of Transistors | Power(μw) | Delay(ns) | UNG(v) | PDP(μw∗ns)*10^{-3} |
|-----------------------|-------------------|-----------|-----------|--------|---------------------|
| Standard footless     | 36                | 286.41    | 27.807    | 0.2625 | 7.96                |
| FSD                   | 42                | 45.25     | 78.03     | 0.5293 | 3.530               |
| MDND                  | 46                | 58        | 77.54     | 0.4625 | 4.497               |
| MDFSD                 | 46                | 89        | 79.02     | 0.4259 | 7.032               |
| HS Domino             | 42                | 518.89    | 27.595    | 0.2619 | 14.318              |
| Conditional keeper    | 47                | 540.67    | 31.727    | 0.2773 | 17.153              |
| Proposed HS Domino   | 47                | 540.67    | 31.727    | 0.2773 | 17.153              |
| Proposed CK Domino   | 47                | 540.67    | 31.727    | 0.2773 | 17.153              |
| CHSK with Keeper      | 23                | 511.43    | 19.63     | 0.2526 | 10.039              |
| CHSK without Keeper   | 19                | 510.1     | 19.93     | 0.2719 | 10.166              |

The power consumption, delay process, PDP and noise immunity are evaluated from the analysis of the domino logic circuit. Figure 7 shows the analysis of transient of the combined circuit of CHSK domino logic. Table 1 shows the simulated results for various domino logic circuit comparison with the CHSK Domino Logic.

5. Conclusion

In the proposed domino logic circuit, the analysis of the circuit was carried out for the parameter like Power, Delay, Transistor count, Unity Noise Gain and Power Delay Product and those parameters are considered to compare the performances with the existing systems. From the analysis the proposed circuit increases the efficiency.
of the circuit with reduced delay and usage of number of transistors. The new circuit techniques are proposed with multiplexer and obtained better results when compared to the existing logic systems. By using these techniques, it produces a small potential at the source of the pull down network and also increases the robustness of the circuits.

6. References

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