A Novel Approach for Design and Investigation of Dual Material Stack Gate Oxide TFET using Oxide Strip Layer Mechanism

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Abstract In this paper, for the first time, we use a distinctive approach based on oxide strip layer in dual material stack gate oxide-tunnel field-effect transistor (DMSGO-OSL-TFET) to improve the DC, analog/RF, and linearity performance. For this, a stack gate oxide with workfunction is considered to enhance the ON-state current ($I_{ON}$) and reduce the ambipolar current ($I_{amb}$). For this case, the gate electrode is tri-segmented, named as tunnel gate ($M_1$), control gate ($M_2$) and auxiliary gate ($M_3$) with different gate lengths ($L_1, L_2, L_3$) and work functions ($\phi_1, \phi_2, \phi_3$), respectively. To maintain dual-work functionality, the possible combinations of these work functions are considered. Technology computer-aided design (TCAD) simulations are performed and noted that the workfunction combination ($\phi_1 = \phi_3 < \phi_2$) outperforms compared to other structures. Where $\phi_1$ on the source side is used to enhance the $I_{ON}$, while $\phi_3$ (equal to $\phi_1$) is used on the drain side to minimize the $I_{amb}$. To further enhance the device performance, a high-K oxide strip layer is considered on the drain side to suppress the ($I_{amb}$) whereas, a low-K oxide strip layer is used at the source junction to maximize the $I_{ON}$. Moreover, length of gate segments, oxide strip layer height, and thickness are optimized to achieve a better $I_{ON}$, switching ratio, subthreshold swing (SS) and reduce the ($I_{amb}$) which helps in the gain of device and design of analog/RF circuits. The proposed device as compared to dual material control gate-oxide strip layer-TFET (DMCG-OSL-TFET) shows improvement in $I_{ON}/I_{OFF}$ ($\sim 4.23$ times), 84 % increase in transconductance ($g_m$), 136 % increase in cut-off frequency ($f_T$), 126 % increase in gain bandwidth product (GBP), point subthreshold swing (15.8 mV/decade) and other significant improvements in linearity performance parameters such as $g_{m3}$, VIP3, IIP3, IMD3 making the proposed device useful for low power switching, analog/RF and linearity applications.

Keywords Dual material · Ambipolarity · oxide strip · Auxiliary gate · Control gate · Linearity

1 Introduction

MOSFETs are widely used for low power switching, analog/RF design, and wireless communication systems. To further improve the performance and increase the packing density, the dimensions of MOSFETs are aggressively down scaling [1]-[2]. Eventually, this leads to some major issues such as high $I_{OFF}$, high power dissipation, SCEs, and SS restriction of 60 mV/decade [3]-[4]. These challenges make conventional MOSFETs unfavourable for the future low power switching and analog/RF applications. To address the above problems, an alternative device structure based on quantum tunneling-FET (TFET) is considered to be one of the possible replacements of MOSFETs in low-power switching circuits due to lower ($I_{OFF}$), voltage scaling, steeper SS below 60 mV/decade and immunity to SCEs [5]-[7]. These features make TFETs more favorable for low-power energy-efficient circuits. However, the main issue of this device is inferior $I_{ON}$ and ambipolar behavior [8]. TFET can be used in digital complementary logic circuits and high-frequency applications if the ambipolar current is suppressed. Ambipolar current implies the flow of current for both positive and negative
$V_{GS}$ [9]. This happens as the tunneling junction is transferred from source to drain side by applying $V_{GS} < 0$ (in case of n-type TFET). Because of ambipolar current, SS degradation and the efficiency of the device for the complimentary digital logic circuits and high-frequency applications is limited [10]-[11].

The ON-current of the TFETs is inferior due to inadequate tunneling rate (BTBT) at the tunneling junction. In TFET, higher lateral electric field across the source junction is required to lower the tunneling barrier width. As per the Wentzel-Kramers-Brillouin method, the BTBT probability depends exponentially on the tunneling barrier width. As per the Wentzel-Kramers-Brillouin method, the BTBT probability depends exponentially on the tunneling barrier width. As per the Wentzel-Kramers-Brillouin method, the BTBT probability depends exponentially on the tunneling barrier width. As per the Wentzel-Kramers-Brillouin method, the BTBT probability depends exponentially on the tunneling barrier width. As per the Wentzel-Kramers-Brillouin method, the BTBT probability depends exponentially on the tunneling barrier width.

In recent literature, researchers have made numerous efforts and proposed different methods to suppress the ambipolar current, improve the DC, analog/RF and linearity performance. Raad et al. [12] proposed a TFET based on hetero dielectric and workfunction engineering (HGD-DW TFET) and reported an $I_{ON}$/$I_{OFF}$ ratio of (9.8×10$^{11}$), $g_m$ of 0.290 mS, $f_T$ as (~59.6 GHz). Kondekar et al. [13] proposed TFET based on electrically doping (ED-TFET) to enhance the analog and radio frequency performance and reported an $I_{ON}$/$I_{OFF}$ ratio of (~10$^{12}$), $g_m$ as 1.02 mS, $f_T$ of (190 GHz). Nigam et al. [14] proposed a charge plasma based TFET (DMCG-CPTFET) and obtained an $I_{ON}$/$I_{OFF}$ ratio of (~6×10$^{12}$), $I_{amb}$ as 1×10$^{-17}$ (A/µm), $f_T$ of (~28 GHz). Ashita et al. [15] investigated an inverted-C TFET (ICTFET) with SCOPs which provides both lateral and vertical tunneling to boost the ON current. The authors have reported $I_{ON}$/$I_{OFF}$ ratio of (4.5×10$^{9}$), SS of (48 mV/decade), $f_T$ of (1.19 GHz). Chandan et al. [16] proposed a metal strip based TFET (MS-ED-TFET) to overcome low switching ratio, SS and analog/RF performance and achieved an $I_{ON}$/$I_{OFF}$ of (8.92×10$^{8}$), SS of (8.07 mV/decade), $g_m$ of 0.007 mS, $f_T$ as (0.17 GHz). Shaikh et al. [17] presented a quadruple-gate TFET with drain engineering (DE-QG-TFET) and achieved an $I_{ON}$/$I_{OFF}$ ratio of (1.79×10$^{12}$), $f_T$ of (~34 GHz), $g_m$ of 0.261 mS, GBP of (3.9 GHz). Kumar et al. [18] proposed a stack-gate approach TFET with dual material (DMDODG-TFET) to and reported an $I_{ON}$/$I_{OFF}$ ratio of (5×10$^{11}$), SS of (~18.5 mV/decade), $f_T$ of (~8.8 GHz), $g_m$ of 0.09 mS. Joshi et al. [19] investigated an extended source TFET (ESDG-TFET) and reported an $I_{ON}$/$I_{OFF}$ of (2.57×10$^{12}$), SS of (12.24 mV/decade), $g_m$ of 0.238 mS, $f_T$ of (37.7 GHz).

To address the ON-current, ambipolarity issues, enhance the analog/RF and linearity parameters, in this work, a novel device structure named dual-material stack gate oxide-oxide strip layer TFET (DMSGO-OSL-TFET) is proposed. The ($\phi_3 < \phi_2$) workfunction and high-K oxide strip layer at the drain junction leads to an increased tunneling barrier width and reduced lateral electric field, as a result, ambipolar current reduces when negative $V_{GS}$ is applied. Similarly, ($\phi_1 < \phi_2$) work function and the low-K oxide strip layer at the source-channel junction reduces the tunneling width ($\lambda$) and increases the lateral electric field, which results in an improvement in tunneling current.

This paper is organised as follows: The structural and Simulation details of the device is discussed in section 2. Structural optimization details are presented in Section 3. DC, analog/RF and linearity performance is discussed in section 4. Lastly, the conclusions of this work is summarised in Section 5.

## 2 Device structure, parameters and simulation models

![Cross-sectional view of proposed DMSGO-OSL-TFET](image)

Fig. 1 Cross-sectional view of proposed DMSGO-OSL-TFET

The 2D structural view of the proposed DMSGO-OSL-TFET with oxide strip layers is illustrated in Fig. 1. Table 1 presents the device parameters and dimensions used in the simulation. The length of the stack gate is considered 50 nm with SiO$_2$ layer thickness of (0.8 nm) and HfO$_2$ oxide layer thickness of (1.2 nm) [18]. Further, the entire gate is split into three segments labelled as tunnel gate ($M_1$), control gate ($M_2$) and auxiliary gate ($M_3$) with lengths ($L_1$, $L_2$, $L_3$) and work functions ($\phi_1$, $\phi_2$, $\phi_3$) respectively. In the case of single-material stack gate oxide-oxide strip layer-TFET (SMSGO-OSL-TFET) the gate work functions ($\phi_1 = \phi_2$).
Table 1 Design parameters used in device simulation

| Parameters                        | DMCG-OSL-TFET | DMSGO-OSL-TFET |
|-----------------------------------|---------------|---------------|
| Gate Length (L<sub>G</sub>)       | 50 nm         | 50 nm         |
| SiO<sub>2</sub> thickness (T<sub>SiO<sub>2</sub></sub>) | 2 nm          | 0.8 nm        |
| HfO<sub>2</sub> thickness (T<sub>HfO<sub>2</sub></sub>) | -             | 1.2 nm        |
| Oxide strip thickness             | 2 nm          | 2 nm          |
| Oxide strip height                | 4 nm          | 4 nm          |
| Silicon film thickness (T<sub>Si</sub>) | 10 nm         | 10 nm         |
| Channel doping (N<sub>ch</sub>)    | 1×10<sup>17</sup> cm<sup>-3</sup> | 1×10<sup>17</sup> cm<sup>-3</sup> |
| Source doping (p type) (N<sub>S</sub>) | 1×10<sup>20</sup> cm<sup>-3</sup> | 1×10<sup>20</sup> cm<sup>-3</sup> |
| Drain doping (n type) (N<sub>D</sub>) | 5×10<sup>18</sup> cm<sup>-3</sup> | 5×10<sup>18</sup> cm<sup>-3</sup> |
| HfO<sub>2</sub> dielectric constant (K) | 25            | 25            |
| Tunnel gate Length (L<sub>1</sub>) | 10 nm         | 10 nm         |
| Control gate Length (L<sub>2</sub>) | 30 nm         | 30 nm         |
| Auxiliary gate Length (L<sub>3</sub>) | 10 nm         | 10 nm         |
| Tunnel gate workfunction (φ<sub>1</sub>) | 4.0 eV        | 4.0 eV        |
| Control gate workfunction (φ<sub>2</sub>) | 4.4 eV        | 4.4 eV        |
| Auxiliary gate workfunction (φ<sub>3</sub>) | 4.0 eV        | 4.0 eV        |

The control gate workfunction (φ<sub>2</sub>) is considered 4.4 eV corresponding to the metal molybdenum (Mo) (4.36 eV - 4.95 eV). The workfunctions (φ<sub>1</sub> and φ<sub>3</sub>) are considered 4.0 eV corresponding to metal aluminum (Al) (4.0 eV - 4.26 eV) [20]. In DMSGO-OSL-TFET without oxide strip layer, I<sub>ON</sub>/I<sub>OFF</sub> is noted as 2.25×10<sup>11</sup>. A low-K oxide strip layer is considered at the tunneling junction to increase the I<sub>ON</sub>. Whereas, a high-K oxide strip layer at the drain junction to lower the I<sub>OFF</sub>. Due to this, I<sub>ON</sub>/I<sub>OFF</sub> is noted as 2.83×10<sup>12</sup> in the proposed device using TCAD device simulator. The nonlocal BTBT model is considered which uses the Wentzel–Kramers–Brillouin method to measure tunneling probability across the junction. Shockley-Read-Hall model is enabled to consider minority carrier recombination effects for numerical solutions. Bandgap narrowing (BGN) model is used due to heavily doped concentrations in source and drain regions, FLDMOB mobility model is used to consider the velocity saturation effects because of lateral electric field. The simulation study carried out in this work uses a nonlocal BTBT model that is calibrated with the data reported in [8], which was previously calibrated, with the experimental data obtained from the fabricated device [21].

3 Results and discussion

3.1 Workfunction optimization Results

To align the band structure at the junctions and to modulate the carriers through the channel, the entire gate length in DMSGO-OSL-TFET is tri segmented known as tunnel gate (M<sub>1</sub>), control gate (M<sub>2</sub>), and auxiliary gate (M<sub>3</sub>) with workfunctions φ<sub>1</sub>, φ<sub>2</sub> and φ<sub>3</sub> respectively as illustrated in Fig. 1. By fixing (φ<sub>1</sub> and φ<sub>3</sub>) and changing (φ<sub>2</sub>), better switching ratio and minimum ambipolar current is observed for the combination (φ<sub>1</sub> = φ<sub>3</sub> < φ<sub>2</sub>) as illustrated in Fig. 3(a) and table 2. Fig. 3(b) and Fig. 3(c) shows ON-state and the OFF-state band diagrams of the proposed DMSGO-OSL-TFET by varying (φ<sub>2</sub>) and fixing (φ<sub>1</sub> = φ<sub>3</sub> = 4.0 eV). From the Fig. 3(c), it can be seen that tunneling width increases with an increase in (φ<sub>2</sub>). This results in band overlap decrease on the source side, which results in a decrease of tunneling current. Whereas the band overlap has been noted at the drain junction for (φ<sub>2</sub> > 4.4eV) and tunneling is observed in the OFF state, also (φ<sub>2</sub>) workfunction variation in the ON-state does not shows a significant change of the tunneling current until the workfunction (φ<sub>2</sub> = 4.4 eV). Also, a band overlap decrease is seen
for \((\phi_2 > 4.4 \text{ eV})\), which results in a decrease in ON current \((I_{ON})\) as shown in Fig. 3(a).

3.2 Oxide strip optimization results

To further improve \(I_{ON}\) and minimize the ambipolar current, optimized oxide strip layers are inserted at the source and drain junctions. Fig. 4(a) shows the comparative \(I_{DS-VGS}\) variation for different oxide strip materials in DMSGO-OSL-TFET. It was noted that the combination of low-K oxide strip (air) at the tunneling junction and high-K oxide strip \((HfO_2)\) at the drain-channel interface shows higher \(I_{ON}\) and minimum ambipolar current because of tunneling width and band alignment at the junction. Fig. 4(b) shows \(I_{DS-VGS}\) variation in DMSGO-OSL-TFET with oxide strip heights at the tunneling junction by fixing the oxide strip on the drain side. It has been noted that a strip of 4 nm height at the tunneling junction shows better \(I_{ON}\) because of higher electric field and decrease in tunneling width. Similarly, as shown in Fig. 4(c), fixing the height of low-K oxide strip and varying the high-K oxide strip, it was observed that at the drain channel junction, the oxide strip of 4 nm height shows minimum ambipolar current with a higher ratio of \(I_{ON}/I_{OFF}\). Fig. 4(d) shows the comparative \(I_{DS-VGS}\) characteristics in DMSGO-OSL-TFET for different oxide strip thickness. It was noted that oxide strip thickness of 2 nm at the tunneling junction shows better tunneling current \(I_{ON}\) and minimum ambipolar current due to the band alignment.

3.3 Gate length optimization

In this section, the gate segments of the proposed device is optimized. In this regard, Tables III–V shows the variations in \(I_{ON}, I_{OFF}, I_{amb}, I_{ON}/I_{OFF}\) for various combinations of \(L_1, L_2\) and \(L_3\). The optimization of \(L_3\) at constant \(L_1 = 10 \text{ nm}\) is shown in Table III. Further, the optimization of \(L_1\) at constant \(L_3 = 15 \text{ nm}\) is shown in Table IV. Table V shows the \(L_1\) and \(L_3\) variations at \(L_1 = L_3\). From this analysis, it has been noted that \(L_3 = 15 \text{ nm}\) performs better in terms of \(I_{ON}, I_{OFF}, I_{amb}\). However, \(L_1 = L_3 = 10 \text{ nm}\) shows

![Diagram](image-url)
Table 2 Impact of $\phi_2$ on $I_{ON}/I_{OFF}$ with ($\phi_1 = \phi_3$)

| $\phi_2$ | $I_{ON} (\lambda/\mu m)$ | $I_{OFF} (\lambda/\mu m)$ | $I_{ON}/I_{OFF}$ | $I_{amb} (\lambda/\mu m)$ |
|----------|-----------------------------|-----------------------------|-------------------|-----------------------------|
| 4.0 eV   | $1.36 \times 10^{-5}$       | $2.96 \times 10^{-13}$      | $4.58 \times 10^7$ | $3.58 \times 10^{-16}$      |
| 4.2 eV   | $1.23 \times 10^{-5}$       | $1.26 \times 10^{-15}$      | $9.79 \times 10^9$ | $3.70 \times 10^{-16}$      |
| 4.4 eV   | $1.02 \times 10^{-5}$       | $4.58 \times 10^{-17}$      | $2.23 \times 10^{12}$ | $3.76 \times 10^{-16}$      |
| 4.6 eV   | $8.11 \times 10^{-6}$       | $6.18 \times 10^{-17}$      | $1.31 \times 10^{12}$ | $3.79 \times 10^{-16}$      |
| 4.8 eV   | $5.36 \times 10^{-6}$       | $7.31 \times 10^{-17}$      | $7.33 \times 10^{10}$ | $3.80 \times 10^{-16}$      |

Fig. 4 Comparative optimization plots of (a) Oxide Strip layer materials (b) Low-K oxide strip layer height (c) high-K oxide strip layer height (d) oxide strip layer thickness by fixing heights in proposed device DMSGO-OSL-TFET.

better results in terms of $I_{ON}/I_{OFF}$ and is considered for further analysis.

For an optimized oxide strip layer shown in Fig. 1 based on ($\phi_1, \phi_2, \phi_3$) combinations, various structures for the device are formed, as presented in Table 6. Further, a comparative analysis among these devices is done in terms of their carrier concentration, band diagrams, tunneling rate, surface potential, electric field variation, and $I_{DS}-V_{GS}$ characteristics. For SMSGO-TFET, all the three workfunctions ($\phi_1, \phi_2, \phi_3$) of the gate material has been considered equal (4.4 eV). Fig. 5(a) shows the comparative carrier concentration variation with distance. Higher electron concentration is observed in the case of DMSGO-OSL-TFET, due to this a decrease in tunneling width and an increase in tunneling rate is observed as shown in Fig. 5(b) and Fig. 5(c). Further, an increase in surface potential is observed in DMSGO-OSL-TFET, shown in Fig. 5(d). Due to the oxide strip layer at the tunneling junction, maximum electric field is observed at this junction as shown in Fig. 5(e). Thus, maximum tunneling occurs in this region, as the BTBT rate ($G_{BTBT}$) at the tunneling junction depends on the electric field ($\varepsilon$) leads to an increase in BTBT rate as per the expression [22].

$$G_{BTBT} = A\varepsilon^\sigma \exp \left( -\frac{B}{\varepsilon} \right)$$  \hspace{1cm} (1)

Where A, B are constants which are related to the electron’s effective mass and the tunnelling probabil-
ity, ε is the electric field and σ is the transition constant. Further, the probability of tunneling of the carrier ($T_{WKB}$) at the tunneling barrier is analyzed by the approximation of Wentzel–Kramer–Brillouin (WKB) [23].

$$T_{WKB} \propto \exp \left[ -\frac{4\sqrt{2}\pi m^*}{\hbar} \frac{E_g^3}{3g(hE_g + \Delta \phi)} \right]$$  (2)

Where $m^*$ is the effective mass of an electron, q represents the electron charge, h represents Planck’s constant, $E_g$ is the effective bandgap, λ is the width of the tunneling barrier, and $\Delta \phi$ represents the energy overlap where the tunneling occurs. Therefore, as shown in Fig. 5(f), a significant increase in tunneling current is observed. Fig. 5 and Table 7 show that DMSGO-OSL-TFET performs better than other device structures.

### 4 DC, analog/RF and linearity performance

#### 4.1 DC characteristics

In this section, comparative DC characteristics of DMCG-TFET, DMSGO-OSL-TFET, and DMSGO-TFET have been analyzed. Because of the oxide strip layer, reduced $V_T$, an improved ON-state current, reduced ambipolar current, and a higher switching ratio ($2.83 \times 10^{12}$) was observed in DMSGO-OSL-TFET compared with DMCG-OSL-TFET due to decreased tunneling distance and improved lateral electric field across the tunneling junction. The electric field variation with distance is shown in Fig. 6(a), a higher electric field at the tunneling junction is noted in DMSGO-OSL-TFET, which decreases the tunneling barrier width as shown in Fig. 6(b). This results in a significant increase in drain current, as illustrated in Fig. 6(c). Fig. 6 and Table 8 shows that DMSGO-OSL-TFET performs better than the other structures. Fig. 6(d) shows the comparative output characteristics plot at $V_{GS} = 1$ V.

From the figure, it can be noted that the tunneling current $I_{DS}$ rises and then saturates because of velocity saturation as $V_{DS}$ increases from 0 to 0.8 V. The tunneling current does not change substantially from $V_{DS} = 0.8$ V onwards, so the current remains constant. Furthermore, due to the better coupling, increase in an electric field and decrease in tunneling barrier width, higher $I_{ON}$ is noted for DMSGO-OSL-TFET relative to DMCG-OSL-TFET with SiO$_2$ gate oxide.

### Table 3 $L_3$ Gate segment optimization at constant $L_1 = 10$ nm

| $L_3$ | $I_{ON}(\Lambda/\mu m)$ | $I_{OFF}(\Lambda/\mu m)$ | $I_{ON}/I_{OFF}$ | $I_{amb}(\Lambda/\mu m)$ |
|-------|-----------------|-----------------|-----------------|-----------------|
| 5 nm  | 1.51×10^{-4}   | 3.16×10^{-14}  | 4.78×10^{9}    | 4.09×10^{-13}  |
| 10 nm | 1.48×10^{-4}   | 5.23×10^{-17}  | 2.83×10^{12}   | 5.21×10^{-16}  |
| 15 nm | 1.59×10^{-4}   | 4.36×10^{-14}  | 3.65×10^{9}    | 3.65×10^{-16}  |
| 20 nm | 1.62×10^{-4}   | 6.21×10^{-14}  | 2.61×10^{9}    | 3.64×10^{-16}  |

### Table 4 $L_1$ Gate segment optimization at constant $L_3$ =15 nm

| $L_1$ | $I_{ON}(\Lambda/\mu m)$ | $I_{OFF}(\Lambda/\mu m)$ | $I_{ON}/I_{OFF}$ | $I_{amb}(\Lambda/\mu m)$ |
|-------|-----------------|-----------------|-----------------|-----------------|
| 5 nm  | 8.51×10^{-5}   | 3.24×10^{-17}  | 2.63×10^{12}   | 3.66×10^{-16}  |
| 10 nm | 1.59×10^{-4}   | 4.36×10^{-14}  | 3.65×10^{9}    | 3.66×10^{-16}  |
| 15 nm | 1.79×10^{-4}   | 1.86×10^{-11}  | 9.62×10^{6}    | 3.66×10^{-16}  |
| 20 nm | 1.88×10^{-4}   | 3.8×10^{-11}   | 4.96×10^{6}    | 3.66×10^{-16}  |

### Table 5 $L_1$ and $L_3$ Gate segments optimizations with $L_1 = L_3$

| $L_1$ | $I_{ON}(\Lambda/\mu m)$ | $I_{OFF}(\Lambda/\mu m)$ | $I_{ON}/I_{OFF}$ | $I_{amb}(\Lambda/\mu m)$ |
|-------|-----------------|-----------------|-----------------|-----------------|
| 5 nm  | 8.45×10^{-5}   | 9.01×10^{-17}  | 9.38×10^{11}   | 4.09×10^{-13}  |
| 10 nm | 1.48×10^{-4}   | 5.23×10^{-17}  | 2.83×10^{12}   | 5.21×10^{-16}  |
| 15 nm | 1.79×10^{-4}   | 1.86×10^{-11}  | 9.62×10^{6}    | 3.66×10^{-16}  |
| 20 nm | 1.97×10^{-4}   | 4.0×10^{-11}   | 4.91×10^{6}    | 4.91×10^{-16}  |

### Table 6 Possible devices with different work functions

| Possible device | $\phi_1$ | $\phi_2$ | $\phi_3$ |
|-----------------|---------|---------|---------|
| SMSGO-OSL-TFET  | 4.4 eV  | 4.4 eV  | 4.4 eV  |
| DMCG-OSL-TFET   | 4.0 eV  | 4.4 eV  | 4.4 eV  |
| DMSGO-OSL-TFET2 | 4.4 eV  | 4.4 eV  | 4.0 eV  |
| DMSGO-TFET      | 4.0 eV  | 4.4 eV  | 4.0 eV  |
4.2 Analog/RF Performance improvement

This section analyses the analog/RF parameters $g_m$, $g_{DS}$, $R_o$, $C_{gs}$, $C_{gd}$, $f_T$, TGF, Fmax, TFP, GBP and transit time. The transconductance ($g_m$) reflects the gain of the device, a larger $g_m$ makes the device useful for analog applications. Moreover, ($g_m$) plays an important role in attaining higher values of $f_T$ and GBP.

Fig. 7(a) shows the comparative variation of $g_m$ with $V_{GS}$ at $V_{DS} = 1$ V. The $g_m$ of DMSGO-OSL-TFET is noted to be maximum, because of an increase in tunneling current due to the low tunneling gate workfunction ($\phi_1$), and the presence of low-k oxide strip at the source junction shows more band bending and large electric field at the source junction in comparison to the other
Fig. 6 Comparative results of (a) Electric field variation (b) Band variation (c) $I_{DS}-V_{GS}$ characteristics (d) $I_{DS}-V_{DS}$ characteristics in DMCG-TFET, DMCG-OSL-TFET, DMSGO-TFET and DMSGO-OSL-TFET at ($V_{DS}=1.0\,V$, $V_{GS}=1.5\,V$).

| Parameters                  | SMSGO-OSL-TFET | DMSGO-OSL-TFET | DMSGO-OSL-TFET2 | DMSGO-OSL-TFET3 |
|-----------------------------|----------------|----------------|----------------|----------------|
| $I_{ON}$ ($A/\mu m$)        | $1.37 \times 10^{-5}$ | $1.41 \times 10^{-4}$ | $1.35 \times 10^{-5}$ | $1.48 \times 10^{-4}$ |
| $I_{OFF}$ ($A/\mu m$)       | $1.78 \times 10^{-16}$ | $1.788 \times 10^{-16}$ | $5.18 \times 10^{-17}$ | $5.22 \times 10^{-17}$ |
| $I_{ON}/I_{OFF}$            | $7.68 \times 10^{10}$ | $7.91 \times 10^{11}$ | $2.61 \times 10^{11}$ | $2.83 \times 10^{12}$ |
| $V_{TH}$ (V)                | 0.63            | 0.29            | 0.63            | 0.29            |
| $SS$ (mV/dec.)              | 32.7            | 17.3            | 28.7            | 15.8            |
| Electric field (MV/cm)      | $8.19 \times 10^{-4}$ | $9.79 \times 10^{-4}$ | $8.27 \times 10^{-4}$ | $1.01 \times 10^{-3}$ |
| $g_{m}$ ($s$)               | 5.15            | 5.55            | 5.16            | 5.56            |

structures. Further, it has been noted that because of an improvement in drain current, $g_{m}$ increases with $V_{GS}$ at first, then declines at a higher value of $V_{GS}$ due to degradation of mobility. Fig. 7(b) illustrates the comparative output conductance ($g_{DS}$) variation with the drain voltage ($V_{DS}$). Higher output conductance is preferred as it provides higher intrinsic gain. From the simulation results, higher output conductance has been noted in DMSGO-OSL-TFET due to the higher $\delta I_{DS}$ shown by DMSGO-OSL-TFET for the equal change in $\delta V_{DS}$. Fig. 7(c) shows the comparative $R_{O}$ variation with $V_{DS}$ for constant $V_{GS}$. It can be noted that lower $R_{O}$ is observed for DMSGO-OSL-TFET as $g_{DS}$ is higher. The variation of $C_{gs}$ and $C_{gd}$ obtained from small-signal ac analysis at 1MHz frequency is presented in Fig. 7(d) and Fig. 7(e). In DMCG-OSL-TFET, the minimum value of $C_{gs}$ is noted and in DMSGO-OSL-TFET, a significant increase of $C_{gd}$ is noted above $V_{GS}=0.85\,V$. Fig. 7(f) shows the comparative variation of $f_{T}$ with $V_{GS}$. It has been noted that, initially, $f_{T}$ increases with $V_{GS}$ due to an increase in $g_{m}$, then decreases with $V_{GS}$ after reaching the peak value due to an increase in $C_{gd}$ and decrease in $g_{m}$ due to mobility degradation. From the simulation results, a higher $f_{T}$
Fig. 7 Comparative performance of (a) $g_m$ (b) $g_{DS}$ (c) $R_O$ (d) $C_{gs}$ (e) $C_{gd}$ (f) $f_T$ in DMCG-TFET, DMCG-OSL-TFET, DMSGO-TFET and DMSGO-OSL-TFET

is obtained for DMSGO-OSL-TFET which shows that the proposed device structure is more favourable for radio frequency applications. The $f_T$ of the device is described as per the expression \[ f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \] (3)

The GBP is one of the crucial parameter for assessment of the radio frequency performance of the device, for a specified dc voltage gain of 10, it is calculated using the expression \[ GBP = \frac{g_m}{2\pi 10C_{gd}} \] (4)

The GBP variation with $V_{GS}$ is shown in Fig. 8(a). It can be seen that GBP initially increases as the gate voltage increases, but it decreases for higher gate voltages due to mobility degradation. In DMSGO-OSL-
TFET, due to $g_m$ and $C_{gd}$ at lower gate voltages, a high increase in GBP is observed. The TGF parameter indicates how efficiently the current reaches a certain transconductance value. Fig. 8(b) shows the TGF variation with $V_{GS}$. In DMSGO-OSL-TFET, higher TGF is observed at lower $V_{GS}$ and with increase in $V_{GS}$ it decreases as the variation in $I_{DS}$ is small. The TGF is obtained as follows

$$TGF = \left( \frac{g_m}{I_{DS}} \right)$$  \hspace{1cm} (5)\hspace{1cm}

Fig. 8(c) shows the variation of TFP with $V_{GS}$. It can be noted that DMSGO-OSL-TFET has higher TFP due to high $g_m$ and $f_T$. The TFP is obtained as follows

$$TFP = \left( \frac{g_m}{I_{DS}} \right) f_T$$  \hspace{1cm} (6)\hspace{1cm}

The variation in transit time ($\tau$) with $V_{GS}$ is illustrated in Fig. 8(d). It is the time taken by the carriers to move from the source side to the drain [20]. A decrease in the transit time is observed, with an increase in $V_{GS}$ due to an increase in $f_T$. Also, the minimum
transit time has been noted in DMSGO-OSL-TFET. The transit time ($\tau$) of the device is calculated using the expression

$$\tau = \frac{1}{2\pi 10f_T} \quad (7)$$

The maximum operating frequency ($f_{\text{max}}$) is another crucial parameter for a radio frequency performance analysis. It is calculated by using the equation

$$f_{\text{max}} = \sqrt{\frac{f_T}{8\pi C_{gd}R_{gd}}} \quad (8)$$

Here, $R_{gd}$ represents the gate resistance. Fig. 8(e) shows the $f_{\text{max}}$ variation with $V_{GS}$ at $V_{DS} = 1.0$ V. It has been

Fig. 9  Comparative performance of (a) $gm_2$ (b) $gm_3$ (c) VIP2 (d) VIP3 (e) IMD3 (f) IIP3 variation with $V_{GS}$ in DMCG-TFET, DMCG-OSL-TFET, DMSGO-TFET and DMSGO-OSL-TFET
shows the comparative variation of $g_m$ with $V_{DS}$ at $V_{DS} = 1.0$ V. A higher VIP2 needed for minimal distortion operation. Further, it can be noted that the VIP2 of DMSGO-OSL-TFET is higher than the other structures due to stack gate, dual gate and oxide strip. The higher VIP3 value indicates a more linear device. Fig. 9(d) shows the comparative VIP3 variation with $V_{GS}$ at $V_{DS} = 1.0$ V. It has been observed that VIP3 of DMSGO-OSL-TFET is higher than the other structures. IMD3 originates from the non-linearity characteristics of $I_{DS}-V_{GS}$ and seems to be a distorting signal in wireless systems. Devices with lower IMD3 values can have the ability to withstand higher signal distortion. Fig. 9(e) shows the comparative IMD3 variation with $V_{GS}$ at $V_{DS} = 1.0$ V. Further, IMD3 of DMCG-TFET is noted to be the smallest, indicating that the DMCG-TFET intermodulation distortion performance is the best of the above devices. The higher IIP3 value shows the device is more linear. Fig. 9(f) shows the comparative IIP3 variation with $V_{GS}$ at $V_{DS} = 1.0$ V, it has observed that the IIP3 of DMSGO-OSL-TFET is much higher than that of other devices.

### Table 8 Performance comparison of SiO$_2$ gate and stack gate TFET with and without oxide strip layers

| Parameters       | DMCG-TFET | DMCG-OSL-TFET | DMSGO-TFET | DMSGO-OSL-TFET |
|------------------|-----------|---------------|------------|----------------|
| $I_{ON}$ (A/µm)  | 5.02 x 10$^{-7}$ | 2.25 x 10$^{-5}$ | 1.03 x 10$^{-5}$ | 1.48 x 10$^{-4}$ |
| $I_{OFF}$ (A/µm) | 2.89 x 10$^{-17}$ | 3.36 x 10$^{-17}$ | 4.57 x 10$^{-17}$ | 5.22 x 10$^{-17}$ |
| $I_{ON}/I_{OFF}$ | 1.73 x 10$^{10}$ | 6.69 x 10$^{11}$ | 2.25 x 10$^{11}$ | 2.83 x 10$^{12}$ |
| $V_{TH}$ (V)     | 0.84      | 0.51          | 0.53        | 0.29           |
| SS (mV/decade)   | 29.4      | 17.9          | 31.4        | 15.8           |
| Electric field (MV/cm) | 5.01 | 5.01          | 4.51        | 3.56           |
| $g_m$ (S)        | 4.88 x 10$^{-5}$ | 5.49 x 10$^{-4}$ | 2.79 x 10$^{-4}$ | 1.01 x 10$^{-3}$ |
| $f_T$ (GHz)      | 5.34      | 81.6          | 20.8        | 193            |
| $f_{max}$ (GHZ)  | 56.6      | 383           | 172         | 525            |
| GBP (GHZ/V)      | 0.579     | 10.4          | 2.69        | 23.6           |
| VIP2 (V)         | 0.77      | 1.84          | 1.66        | 2.67           |
| VIP3 (V)         | 1.35      | 3.71          | 3.38        | 11.57          |
| IIP3 (dBm)       | -7.10     | 20.81         | 12.42       | 27.75          |
| IMD3 (dBm)       | -12.4     | -18.5         | -1.02       | 193            |

### Table 9 Performance comparison of proposed DMSGO-OSL-TFET with other devices

| Possible device | $I_{ON}/I_{OFF}$ | SS (mV/dec) | $g_m$(mS) | $f_T$ (GHz) |
|-----------------|------------------|-------------|-----------|-------------|
| HGD-DW TFET [12]| 9.8 x 10$^{11}$  | 18.5        | 0.290     | 59.6        |
| ED-TFET [13]    | ~ 1 x 10$^{12}$  | -           | 1.02      | 190         |
| DMCG-CPTFET [14]| ~ 6 x 10$^{12}$  | -           | -         | 28          |
| ICTFET [15]     | 4.5 x 10$^{9}$   | -           | -         | 1.19        |
| MS-ED-TFET [16] | 8.92 x 10$^{8}$  | 8.07        | 0.007     | 0.17        |
| DE-QG-TFET [17] | 1.79 x 10$^{12}$ | -           | 0.261     | 34          |
| DMDODG-TFET [18]| 5 x 10$^{11}$    | 18.5        | 0.09      | 8.8         |
| ESDG-TFET [19]  | 2.57 x 10$^{12}$ | 12.24       | 0.238     | 37.7        |
| Proposed work   | 2.83 x 10$^{12}$ | 15.8        | 1.01      | 193         |
5 Conlusion

The DMSGO-OSL-TFET with oxide strip layers at the drain and source junctions is proposed. The structural parameters like gate lengths ($L_1$, $L_2$, $L_3$), work functions ($\phi_1$, $\phi_2$, $\phi_3$), oxide strip height and thickness are optimized to achieve better switching ratio and reduce the ambipolar current. The performance of the proposed device is analyzed using TCAD device simulator. Finally, a comparative performance analysis of the proposed device is done with other device structures and noted the combination of low-K and high-K oxide strip layers at the source and drain junctions and workfunction combination ($\phi_1 = \phi_3 < \phi_2$) on the stack gate oxide in the proposed device shows significant improvements in $I_{ON}/I_{OFF}$, SS, $g_{m}$, $f_T$, $R_o$, transit time ($\tau$), GBP, TGF, TFP, $F_{max}$, VIP2, VIP3, IMD3 and IIP3 given in table 8. The performance of the proposed device is compared with the recent literature shown in table 9 which shows that the proposed device useful for low power switching, high frequency and linearity applications.

Author contributions:
1. Kaushal Nigam - Concept and methodology
2. Dharmender - Resource, simulation

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References
1. Kilchvyska V, Neve A, Vancaillie L, et al. (2003) Influence of device engineering on the analog and RF performances of SOI MOSFETs. IEEE Transactions on Electron Devices 50(3):577-588
2. Mohankumar N, Syamal B, Sarkar CK (2010) Influence of channel and gate engineering on the analog and RF performance of DG MOSFETs. IEEE Transactions on Electron Devices 57(4):820-826
3. Young KK (1989) Short-channel effect in fully-depleted SOI MOSFETs. IEEE Transactions on Electron Devices 36(2):399-402
4. Pal A, Sachid AB, Gossner H, Rao VR (2011) Insights into the design and optimization of tunnel-FET devices and circuits. IEEE Transactions on Electron Devices 58(4):1045-1053
5. Lee MJ, Choi WY (2012) Effects of device geometry on hetero-gate-dielectric tunneling field-effect transistors. IEEE Electron Device Letters 33(10):1459-1461
6. Choi WY, Park B, Lee JD, Liu TK (2007) Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec. IEEE Electron Device Letters 28(8):743-745
7. Boucart K, Ionescu AM (2007) Double gate tunnel FET with high k gate dielectric. IEEE Transactions on Electron Devices 54(7):1725-1733
8. Abhishek, Sharma D, Kumar YBN, Vasanthi MH (2016) Performance Enhancement of Novel InAs/Si Hetero Double-Gate Tunnel FET Using Gaussian Doping. IEEE Transactions on Electron Devices 63(1):288-295
9. Vijayavargiya V, Vishvakarma SK (2014) Effect of drain doping profile on double-gate tunnel field-effect transistor and its influence on device RF performance. IEEE Transactions on Nanotechnology 13(5):974-981
10. Sahay S, Kumar MJ (2015) Controlling the drain side tunneling width to reduce ambipolar current in tunnel FETs using heterodielectric BOX. IEEE Transactions on Electron Devices 62(11):3882-3886
11. Raad BR, Nigam K, Sharma D, Kondekar P (2016) Di-electric and work function engineered TFET for ambipolar suppression and RF performance enhancement. Electronics Letters 52(9):770-772
12. Kondekar PN, Nigam K, Pandey S, Sharma D (2017) Design and analysis of polarity controlled electrically doped tunnel FET with bandgap engineering for analog/RF applications. IEEE Transactions on Electron Devices 64(2):412-418
13. Nigam K, Pandey S, Kondekar P, Sharma D, Parte PK (2017) A Barrier Controlled Charge Plasma-Based TFET With Gate Engineering for Ambipolar Suppression and RF/Linearity Performance Improvement. IEEE Transactions on Electron Devices 64(6):2751–2757
14. Ashita, Loan SA, Rafat M (2018) A high-performance inverted-C tunnel junction FET with source-channel overlap pockets. IEEE Transactions on Electron Devices 65(2):763-768
15. Chandan BV, Gautami M, Nigam K, Sharma D, Tikkwal VA, Yadav S, Kumar S (2018) Impact of a Metal-strip on a Polarity-based Electrically Doped TFET for Improvement of DC and Analog/RF Performance. Journal of Computational Electronics 18(1):76-82
16. Shaikh MRU, Loan SA (2019) Drain-Engineered TFET With Fully Suppressed Ambipolarity for High-Frequency Application. IEEE Transactions on Electron Devices 66(4):1628-1634
17. Kumar S, Singh S, Nigam K, Tikkwal VA (2019) Dual material dual-oxide dual gate TFET for improvement in DC characteristics, analog/RF and linearity performance. Applied Physics A 125(5):3531-3538
18. Joshi T, Singh Y, Singh B (2020) Extended-Source Double-Gate Tunnel FET With Improved DC and Analog/RF Performance. IEEE Transactions on Electron Devices 67(4):1873-1879
19. Nigam K, Kondekar PN, Sharma D (2016) Approach for ambipolar behaviour suppression in tunnel FET by workfunction engineering. IET Micro and Nano Letters 11(8):460-464
20. Solomon PM, et al. (2004) Universal tunneling behavior in technologically relevant P/N junction diodes. Journal of Applied Physics 95(10):5800-5812

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References
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2. Mohankumar N, Syamal B, Sarkar CK (2010) Influence of channel and gate engineering on the analog and RF performance of DG MOSFETs. IEEE Transactions on Electron Devices 57(4):820-826
3. Young KK (1989) Short-channel effect in fully-depleted SOI MOSFETs. IEEE Transactions on Electron Devices 36(2):399-402
4. Pal A, Sachid AB, Gossner H, Rao VR (2011) Insights into the design and optimization of tunnel-FET devices and circuits. IEEE Transactions on Electron Devices 58(4):1045-1053
5. Lee MJ, Choi WY (2012) Effects of device geometry on hetero-gate-dielectric tunneling field-effect transistors. IEEE Electron Device Letters 33(10):1459-1461
6. Choi WY, Park B, Lee JD, Liu TK (2007) Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec. IEEE Electron Device Letters 28(8):743-745
7. Boucart K, Ionescu AM (2007) Double gate tunnel FET with high k gate dielectric. IEEE Transactions on Electron Devices 54(7):1725-1733
8. Abhishek, Sharma D, Kumar YBN, Vasanthi MH (2016) Performance Enhancement of Novel InAs/Si Hetero Double-Gate Tunnel FET Using Gaussian Doping. IEEE Transactions on Electron Devices 63(1):288-295
9. Vijayavargiya V, Vishvakarma SK (2014) Effect of drain doping profile on double-gate tunnel field-effect transistor and its influence on device RF performance. IEEE Transactions on Nanotechnology 13(5):974-981
10. Sahay S, Kumar MJ (2015) Controlling the drain side tunneling width to reduce ambipolar current in tunnel FETs using heterodielectric BOX. IEEE Transactions on Electron Devices 62(11):3882-3886
11. Raad BR, Nigam K, Sharma D, Kondekar P (2016) Di-electric and work function engineered TFET for ambipolar suppression and RF performance enhancement. Electronics Letters 52(9):770-772
12. Kondekar PN, Nigam K, Pandey S, Sharma D (2017) Design and analysis of polarity controlled electrically doped tunnel FET with bandgap engineering for analog/RF applications. IEEE Transactions on Electron Devices 64(2):412-418
13. Nigam K, Pandey S, Kondekar P, Sharma D, Parte PK (2017) A Barrier Controlled Charge Plasma-Based TFET With Gate Engineering for Ambipolar Suppression and RF/Linearity Performance Improvement. IEEE Transactions on Electron Devices 64(6):2751–2757
14. Ashita, Loan SA, Rafat M (2018) A high-performance inverted-C tunnel junction FET with source-channel overlap pockets. IEEE Transactions on Electron Devices 65(2):763-768
15. Chandan BV, Gautami M, Nigam K, Sharma D, Tikkwal VA, Yadav S, Kumar S (2018) Impact of a Metal-strip on a Polarity-based Electrically Doped TFET for Improvement of DC and Analog/RF Performance. Journal of Computational Electronics 18(1):76-82
16. Shaikh MRU, Loan SA (2019) Drain-Engineered TFET With Fully Suppressed Ambipolarity for High-Frequency Application. IEEE Transactions on Electron Devices 66(4):1628-1634
17. Kumar S, Singh S, Nigam K, Tikkwal VA (2019) Dual material dual-oxide dual gate TFET for improvement in DC characteristics, analog/RF and linearity performance. Applied Physics A 125(5):3531-3538
18. Joshi T, Singh Y, Singh B (2020) Extended-Source Double-Gate Tunnel FET With Improved DC and Analog/RF Performance. IEEE Transactions on Electron Devices 67(4):1873-1879
19. Nigam K, Kondekar PN, Sharma D (2016) Approach for ambipolar behaviour suppression in tunnel FET by workfunction engineering. IET Micro and Nano Letters 11(8):460-464
20. Solomon PM, et al. (2004) Universal tunneling behavior in technologically relevant P/N junction diodes. Journal of Applied Physics 95(10):5800-5812
22. Adell PC, Barnaby HJ, Schrimpf RD, Vermeire B (2007) Band-to-band tunneling (BBT) induced leakage current enhancement in irradiated fully depleted SOI devices. *IEEE Transactions on Nuclear Science* 54(6):2174-2180

23. Ionescu AM, Riel H (2011) Tunnel field-effect transistors as energy efficient electronic switches. *Nature* 479(7373):329-337

24. Nigam K, Kondekar PN, Sharma D (2016) DC characteristics and analog/RF performance of novel polarity control GaAs-Ge based tunnel field effect transistor. *Superlattices and Microstructures* 92:224-231

25. Ghosh P, Haldar S, Gupta RS, Gupta M (2012) An investigation of linearity performance and intermodulation distortion of GME CGT MOSFET for RFIC design. *IEEE Transactions on Electron Devices* 59(12):3263-3268

26. Zhijiong L, Hefei W, Ning A, Zhengyong Z (2015) A Tunnel Dielectric-Based Tunnel FET. *IEEE Electron Device Letters* 36(9):966-968