An Intelligent Low-Power Low-Cost Mobile Lab-On-Chip Yeast Cell Culture Platform

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ABSTRACT
Cells are the fundamental unit of life activities, and the basis of studying life phenomena. It is very important to observe the growth state of yeast cells for exploring the law of life movement, diagnosis and treatment of diseases, drug screening and so on. This study proposes a kind of intelligent low-cost portable cell culture platform using the microfluidic channel and the special machine learning circuit. The platform can independently complete the whole work of living cell culture and monitoring. For realizing the reusable and low-power deep learning circuit, a complement optimization neural network algorithm for hardware optimization and corresponding multi-clock-domain reusable multi-level precision neural network accelerator circuit were proposed, which can reduce the circuit area and power of convolution operation in all precisions by average 18.11% and 23.5% respectively. Besides, a dynamic multi-level precision control method based on the battery level is proposed to dynamically adjust the precision of machine learning operation, in order to balance the working time and segmentation accuracy of the culture platform. In addition, a microcolumns-based three-port input microfluidic structure was designed for better yeast culture effect. The experiment showed that the culture platform can realize yeast cell culture and achieve almost the same segmentation accuracy as the large biological laboratory with low-power and low-cost. Compared with the previous work, the cost of mass production was reduced by 88.95%, and the equipment volume was 27.1% smaller. At the same time, it can achieve the best balance of working time and working accuracy under the condition of limited power of equipment according to the needs of users.

INDEX TERMS
Microfluidic channel, yeast culture, portable cell culture platform, intelligent, low-power, lab-on-chip.

I. INTRODUCTION
Cell is the fundamental unit of life activity, is also the basis of the study of life phenomena, the status of the growth of living cells, to explore life movement rule and diagnosis and treatment of the disease, drug screening and so on all has the very vital significance, so as the basis of cell biology, cell culture technology occupies very important position in the field of biotechnology research [1], [2]. The yeast is a commonly used model organism in biology due to its simple growth requirements and genetic tractability [3]–[7]. And in a genetic study, phenotype study of yeast with the genetic mutations related to human genetic diseases has been a great help to improve the human disease diagnosis and treatment [8]–[12].

Nowadays, cell culture is expected to be finished in the laboratory with large and expensive equipment, which costs a lot and cannot leave the laboratory environment [13]. During the studies, massive images of yeast cells are generally captured with microscopes to observe the different cell structures and behaviors under mutation or different drug treatments. However, in general, the morphological analysis of yeast cells mainly depends on manual measurements by researchers, which is time-consuming and with personal subjectivity. Thus, an automatic and efficient yeast cell culture and analysis algorithm of yeast cells are required for the analysis of the yeast cell’s morphology and detailed structures. Therefore, the improvement of living cell culture equipment such as automation, miniaturization and portability has been the research focus. Low-cost portable living cell culture devices can remove the reliance on conventional cell incubators and reduce the risk of contamination during research. At the same
time, it is convenient for researchers to transport and save the experiment time.

Conventional cell culture techniques have changed little over the last several decades and essentially consist of growing cells on a homogeneous large surface (polystyrene or glass dishes or wells) immersed in a homogeneous bath. However, microfluidic introduces new ideas and methods [14]. Microfluidic devices of varying complexity are quickly gaining popularity in the field of cell biology [15], [16]. For chip of cell culture for a long time and high flux are the two basic requirements, the channel size of microfluidic chip in commonly dozens to hundreds of micrometers, and the cell of the same size, can from the space and time to precisely control of fluid, save a lot of reagents and cell, a traditional cell culture technology incomparable advantage [17]. Cell techniques on microfluidic chips have been widely used in single-cell detection [18], drug screening [19], cell analysis [20], [21] and other fields.

Although microfluidic reduces the cost and size of the cultural equipment, current analysis equipment mostly adopts lens set [22]–[24], which has problems such as high cost and difficulty in miniaturization, etc. however, the microfluidic lens-free scheme can be utilized to solve these problems.

Observation and tracking of traditional cell culture require manual operation by professionals, which cost a lot of labor and introduce the subjectivity of operators. However, artificial intelligence can well solve this problem, which has grown up to become a hot topic in this field. However, there continues to be a massive problem. Even though the fact that deep learning has become a heated topic in the field of the biological image, its computing needs to be based on servers or high-performance PC [25], [26], which greatly limits the portability and power consumption of the whole device. Therefore, it is better to have special circuits for concentrated learning, which can further miniaturize the equipment and reduce the costs of equipment. However, if the original inherent learning algorithm is directly used, the circuit scale will be too bulky, so the special optimization algorithm for hardware is needed to improve its cost performance efficiency [27]. The complementary optimization algorithm proposed in this paper had better hardware optimization efficiency.

At present, many portable devices [28] are fed by batteries. Owing to the limit of battery electric quantity, how to decrease the power consumption of devices to improve the use time of devices will be a key problem for portable cultivation devices. Contemporary technologies use servers or high-performance PC, which consume a lot of power and are not conducive to the long working hours of battery-powered portable devices. In addition, in the process of deep learning neural network operation, the precision of operation and the accuracy of results are a pair of parameters that must be balanced. High operation precision means high accuracy result and high cost, and vice versa. At the same time, the high-precision computing circuit also directly corresponds to the extraordinary power consumption, which directly leads to the shortened working time of the battery. However, the deep learning accelerator circuit in the current research is of fixed operational precision [29], which cannot be dynamically adjusted according to the battery power level to maximize the working time of the equipment. Therefore, a multi-precision multiplexing circuit structure based on the monitoring and dynamic adjustment of the battery power level is proposed to achieve the best balance between the accuracy of the monitoring and the working time of the battery.

Segmentation is very important for cell culture monitoring, while the neural network is proven very effective for segmentation [30], but the traditional network pursues precision and ignores the implementation cost, such as VGG [31], AlexNet [32]. Later, many studies began to reduce the network precision, such as DFP [33] BNN [34] XOR [35], and more [36], [37]. Although these methods were used to reduce the precision, but the effect will also decline obviously at the same time. High precision and high effect correspond to high cost and high-power consumption. For portable battery devices with limited power consumption, it is necessary to dynamically adjust the accuracy. It can balance the endurance and effect according to the maximum power of the device. And simple multi-level accuracy design is to design a set of circuits for each accuracy, which causes a lot of circuit waste. Therefore, a reusable multiprecision neural network structure was proposed.

In the calculation of the neural network, the convolution station accounts for the major part, therefore the optimization of the convolution operation can greatly reduce the cost and power consumption of the calculation circuit. Therefore, the complement optimization algorithm for hardware optimization is proposed to reduce the cost and power consumption of the neural network circuit

Our special contributions are as follows.

1) For the first time, a microfluidic lensless and special circuit platform for in vivo cell culture observation and analysis was built
2) In order to minimize the required low cost and low power consumption, a multi-level precision complement optimization algorithm for hardware implementation is proposed. The algorithm can maintain accuracy while minimizing the circuit area cost and power consumption
3) The circuit is designed for the algorithm. The circuit realizes multi-level precision operation and resource reuse to the greatest extent, and is implemented on FPGA
4) The dynamic precision switching control method is proposed, and the battery circuit monitoring circuit is designed to realize the dynamic precision selection
5) The microcolumns-based three-port input microfluidic structure and image acquisition module are designed to realize the culture of yeast cells and the image collection of living cell samples
6) A lite segmentation neural network structure was proposed for shortening the training time and reduced the complexity of the neural network

II. MATERIALS AND METHOD

This section introduces the microfluidic lensless living cell culture monitoring and analysis platform and the modules which consist of. The whole platform prototype is shown in Fig. 1.

The microfluidic lensless yeast culture monitor platform is composed of the following parts: microfluidic channel cultivation chip and image acquisition module, battery power level monitor module, FPGA multi-level precision deep learning accelerator module, liquid crystal display control module, and micropump. The voltage source in the prototype used to simulate different battery power supply voltage.

The specific working process of the microfluidic lensless yeast culture monitor platform is as follows:

1) Inject the yeast cell sample into the microfluidic culture pool through the micropump, and feed the yeast culture liquid media on two sides.

2) The image acquisition module collects images of samples in the microfluidic channel at intervals throughout the whole culture process, and sends the collected images to the FPGA deep learning accelerator module.

3) The battery power level monitor module consists of Analog-to-Digital Converter (ADC) and Micro Controller Unit (MCU) chip. The ADC converts the analog voltage signal into a digital signal in real-time, and sends the digital voltage value to MCU. Then the MCU analyzes the remaining power of the battery, and sends a precision-select signal to the FPGA deep learning accelerator module.

4) The FPGA deep learning accelerator module runs the segmentation neural network to segment the yeast culture image with the precision controlled by the MCU in the battery power level monitor module, and then completes the counting statistics.

5) The touch screen is a 7-inch HD screen with a surface capacitance touch layer, which is responsible for displaying the images in the microfluidic channel and...
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FIGURE 2. Lensless acquisition system and microfluidic chip.

statistical results and receiving user control throughout the yeast culture process.

A. IMAGE ACQUISITION MODULE AND MICROFLUIDIC CHANNEL CULTURE CHIP

The image acquisition module used a 1W yellow LED light source. The microfluidic chip was placed above the CMOS sensor closely for obtaining a better collection image of the yeast cell. The pixel size of the CMOS sensor is 1.4 µm, the effective pixel size is 2592 H × 1944 V (3.67 mm × 2.74 mm), the imaging FOV area is about 10.0 mm².

About yeast cell culture microfluidic channel chip, a microcolumns-based three-port input microfluidic structure was designed for better yeast culture effect. Specifically, the middle part of the three ports was inoculated with yeast samples, and the two ports at two sides are cell culture media input ports. After the injection of the yeast sample and culture media, the middle channel and the two side channels are connected through a microcolumn. The flow of injection is as follows, firstly, dilute the yeast sample with phosphate buffer saline (PBS) to eliminate the interference of other non-detection particle movements, and then use a micropump to inoculate the yeast into the intermediate culture pool at a uniform speed. The advantages of this structural design were as follows the structure can ensure that the bacteria in the intermediate culture pool are not disturbed by the flow of the culture medium as much as possible, and can effectively take away the metabolites of the yeast culture, which is beneficial to our collection and observation. The microfluidic channel structure is shown in Fig. 2.

The image acquisition system worked as follows:

1) Place the microfluidic chip in the lensless imaging acquisition area to ensure cleanliness.

2) After the yeast sample is diluted into the micropump, the inlet of the microfluidic chip is connected to the capillary tube, and the flow rate is controlled by the micropump controller to ensure uniform and stable outflow.

3) The yeast culture liquid media is passed into the two sides of the microfluidic channel chip, and diffuses freely into the culture area through the microcolumns of the middle culture pool and the channels at both sides.

B. MICROFLUIDIC CHANNEL CULTURE CHIP

The microfluidic channel chip for yeast cell culture was micron-sized and simulated the real environment in which microbial samples grow. The design of the micro-column array structure was adopted, and the two sides of the channel were passed into the culture solution, and the yeast sample was injected into the middle culture pool. This design used side channels to transport the culture liquid media, and the gap between the microcolumn arrays provided the conditions for the nutrients in the medium to diffuse into the culture chamber, ensuring the growth of the yeast cell.

Which can reduce the disturbance caused by the fluid, and provide nutrients to the yeast, and take away some of the yeast ’s metabolites which are good for yeast culture.

4) The CMOS sensor collected the culture image at intervals throughout the whole culture process.

Based on the above structure, the light source module structure is design with SolidWorks2016 software and 3D printed. For the microfluidic channel chip, the design software was AutoCAD 2018, and the manufacturing process polydimethylsiloxane (PDMS) and thin glass bonding were used to make microfluidic channel chip. The manufacturing process of the microfluidic channel chip is shown in Fig. 3.

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C. BATTERY POWER LEVEL MONITORING MODULE

The battery power level monitoring module consisted of the voltage ADC and MCU chip. The voltage ADC is connected to the battery to measure the remaining battery power, and convert the analog voltage value into a digital signal voltage, and then send it to the MCU for judging the power level of the battery. The MCU model is STM32F103ZET6, which
has a built-in 32-bit micro CPU which operated at 72MHz. The 12-bit analog-to-digital converter’s model is ADS1256, which can perform high-speed conversion of analog voltage to a digital value.

Currently, due to the complexity of the deep learning accelerator circuit and the huge consumption of hardware resources, the power consumption of the portable device is too large and the battery life is short. Therefore, a multi-precision deep learning accelerator circuit which can dynamically adjust the operation precision according to the battery power level was designed to achieve a good balance between performance and power consumption. In addition, the battery power level monitor was also necessary. The relationship between the voltage of the battery and the remaining power is that the voltage will gradually decrease with the passage of power, and the voltage value can well reflect the remaining power of the current battery pack [38].

The architecture of the battery power level monitor is shown in Fig. 4. The voltage ADC module detected the working voltage status of the battery pack, and converted the analog voltage signal into a digital voltage signal. Then, the digital signal was transmitted to the MCU. The MCU judged the battery power level according to the mapping table for voltage and electric quantity. After judging the battery power level, MCU judged the FPGA deep learning accelerator operation precision according to the mapping table for electric quantity and neural network precision. Finally, the precision select result was transmitted to the FPGA deep learning accelerator.

D. FPGA DEEP LEARNING ACCELERATOR

The selected model of the FPGA deep learning acceleration board was FACE-Z7100. The core board was based on the ZYNQ7100 chip and embedded with the high-performance CPU to support the Linux operating system. It had abundant programmable logic resources on-chip. Conducive to the implementation of the neural network acceleration algorithm.

The FPGA board consisted of an interface expansion board and a core board. The FPGA core board included FPGA chip and memory chips, which implemented all the circuit function. And the interface expansion board included different kinds of interfaces and debug pins. Therefore, the interface expansion board will be removed when minimization is needed.

E. PACKAGE DESIGN

To provide a mobile and inexpensive equipment, a minimal equipment package was designed. In the package, all the modules were packaged into a Cuboid outer shell. The package method is shown in Fig. 5. The size of the equipment package was 11*11.5*18cm.

III. COMPLEMENT CODE OPTIMIZATION ALGORITHM

In the process of yeast culture, the number of yeasts was monitored and counted by a convolution neural network. MAC arithmetic circuit is the key part of the convolution arithmetic circuit. In order to make the quantization convolution circuit more cost-effective, a booth multiplier-based complement code optimization (BCO) algorithm was proposed to facilitate the hardware implementation area.

The original radix-4 Booth multiplication algorithm is

\[ X \times Y = \sum_{n=0}^{\frac{N+1}{2}-1} (E_n \times Y \times 2^n) \]  

In equation (1), \( X \) denotes “multiplier”, \( Y \) denotes “multiplicand”, \( N \) denotes “precision bits number” (e.g. when accuracy is integer 8bit, \( N \) is 7), \( E_n \) denotes “partial product coefficient”, \( 2^{2n} \) denotes “left shift bits”.

The original radix-4 booth partial product encode is in Table 1.

| Input multiplier | Partial Product | Coefficient |
|------------------|-----------------|-------------|
| \( X_{3:1} \)    | \( X_2 \)       | \( X_{3:0} \) |
| 0                | 0               | 0           |
| 0                | 0               | 1           |
| 0                | 1               | 0           |
| 0                | 1               | 1           |
| 1                | 0               | 0           |
| 1                | 0               | 1           |
| 1                | 1               | 0           |
| 1                | 1               | 1           |

In the original radix-4 booth algorithm, negative \( E_n \) can be occur, and then the complement needs to be calculated for partial product accumulation.
TABLE 2. Optimized radix-4 booth partial product and circuit signals.

| Input multiplier | Partial Product | Circuit implementation |
|------------------|-----------------|------------------------|
| $X_{31:1}$ | $X_{21}$ | $X_{15}$ | $P_i$ | result | $\text{sign\_flag}$ | patch |
| 0 | 0 | 0 | 0 | $0 + (1 << (N+1)) - (1 << (N+1))$ | $\{1b1, N\cdot b0\}$ | 0 | $-(1 << (N+1))$ |
| 0 | 0 | 1 | Y | $Y + (1 << (N+1)) - (1 << (N+1))$ | $\{-Y[N-1], Y[N-1:0]\}$ | 0 | $-(1 << (N+1))$ |
| 0 | 1 | 0 | Y | $Y + (1 << (N+1)) - (1 << (N+1))$ | $\{-Y[N-1], Y[N-1:0]\}$ | 0 | $-(1 << (N+1))$ |
| 0 | 1 | 1 | $2Y + (1 << (N+1)) - (1 << (N+1))$ | $\{-Y[N-1], Y[N-1:0], b1\}$ | 0 | $-(1 << (N+1))$ |
| 1 | 0 | 0 | $-2Y + (1 << (N+1)) - (1 << (N+1))$ | $\{Y[N-1], -Y[N-1:0], b1\}$ | 1 | $-(1 << (N+1))$ |
| 1 | 0 | 1 | $-Y - (1 << (N+1)) + (1 << (N+1))$ | $\{Y[N-1], -Y[N-1:0]\}$ | 1 | $-(1 << (N+1))$ |
| 1 | 1 | 0 | $0 + (1 << (N+1)) - (1 << (N+1))$ | $\{1b1, N\cdot b0\}$ | 0 | $-(1 << (N+1))$ |
| 1 | 1 | 1 | 0 | $0 + (1 << (N+1)) - (1 << (N+1))$ | $\{1b1, N\cdot b0\}$ | 0 | $-(1 << (N+1))$ |

In our optimized algorithm, all partial products are added $1 \ll (N + 1)$ first, and the same value is subtracted in the last operation as a patch. By adding 1 to the highest bit, the partial product value is larger than the possible maximum negative number, so that all the partial products through the highest bit plus 1 can be guaranteed to be positive. Then we can make all the subsequent accumulative operations, when we need to expand the high bit number, without considering the negative number, we can directly make up for the high bit 0. The optimized algorithm and the signal implications of circuit implementation are described in Table 2.

The signal “result” denotes the result of adding the complement in advance, and does not include the operation of adding the complement. The calculation of “result” is

$$\text{result} = E_n \cdot Y + 1 \ll (N + 1) \quad (2)$$

The signal “sign_flag” denotes whether a complement plus 1 is needed in subsequent operations.

The signal "patch" is the patch value to be subtracted from the latter operation because $1 \ll (N + 1)$ is added to the former partial product operation.

Since $1 \ll (N + 1)$ is added to each partial product, after all the partial product accumulation, the patch formula for the final operation to be compensated is as follows.

$$X \cdot Y = \sum_{n=0}^{N+1-1} (E_n \cdot Y + 1 \ll (N + 1)) \cdot 2^{2n} - \sum_{n=0}^{N+1-1} ((1 \ll (N + 1)) \cdot 2^{2n}) \quad (3)$$

Therefore, in the case of integer 8bit (int8) precision, we need to subtract $16\cdot b5500$. The calculation is as follows.

$$X \cdot Y = \sum_{n=0}^{3} ((E_n \cdot Y + (1 \ll 8)) \cdot 2^{2n}) - 0x5500 \quad (4)$$

The above equation is the patch operation of an individual booth multiplier, the final real patch of int8 is the complement code of “-0x550000”.

Similarly, in the case of int16 precision, $N = 3$. The equation (3) can be rewritten as

$$X \cdot Y = \sum_{n=0}^{3} ((E_n \cdot Y + (1 \ll 8)) \cdot 2^{2n} - 0x5500) \quad (5)$$

The final real patch of int16 is the complement code of “-0x55550000”.

IV. DEDICATED CIRCUIT DESIGN

In this section, a dedicated circuit architecture was designed for the BCO algorithm. The circuit architecture is shown in Fig. 6.

The convolution neural network accelerator circuit has three main modules, convolution unit, ReLU unit and Max pooling unit. In the whole accelerator circuit, the convolution unit is responsible for convolution operation, and generating main power consumption and occupying the main circuit area of the whole accelerator circuit. ReLU unit is responsible for the ReLU activation operation, and the Max pooling unit is responsible for maximum pool operation.
The convolution unit consists of the multiply-accumulate (MAC) array and accumulation unit (ACCU). The structure of each MAC module is also shown in Fig. 6. The MAC consists of a booth process unit, a patch select unit, an exponent unit, and an adder.

The booth process unit is responsible for completing the proposed BCO booth multiplication, and the adder is responsible for adding the result of the booth process unit to the corresponding patch to complete a MAC operation. Detail structure of the booth process unit is shown in Fig. 7. The patch select unit is used to generate the patch according to the operation precision. The exponent unit is responsible for the exponent adding process when the precision is float-point 16bit (fp16).

Fig. 7 shows the detailed structure of the booth process unit. The booth process unit consists of eight base_booth_units, and it is a reusable booth multiplier structure with the maximum support of 16bit*16bit multiplication and the minimum support of 4bit*4bit multiplication. Each base_booth_unit is responsible for completing a basic booth table lookup operation. In order to avoid the subtraction operation when the table lookup result is negative, when the sign_flag is 1, the highest bit of the result data is reversed to a positive number. All the sign_flag generated from the base_booth_unit will be added to the final operation result through concat_unit and left_shift_unit. The booth lookup table (LUT) content is the booth table value of the BCO algorithm in Table 2.

The concat_unit is responsible for the data splicing operation between the operation result of this base_booth_unit and the sign_flag output by the adjacent lower bit base_booth_unit. Compared with the adder circuit, this data splicing operation consumes very little circuit resources.

The left_shift_unit is responsible for left shifting the sign_flag to the original bit position of the 3-bit multiplier in the booth lookup table operation. After the left_shift_unit, sign_flag can be spliced with the adjacent higher booth lookup table result in the concat_unit, in order to add the sign_flag introduced by the negative number inversion operation into the operation result.

The booth process unit is divided into three clock domains: clk_domain_4bit, clk_domain_8bit, and clk_domain_16bit. Each clock domain’s clock can be opened or closed in different precision. When the clock domain’s clock is off, the output clamp value is zero. The specific control method is as follow.

- When precision was int16 or fp16, all clock domains were opened.
When precision was int8 precision, clock_domain_4bit and clock_domain_8bit were opened, and clock_domain_16bit was closed.
When precision was int4 precision, clock_domain_4bit was opened and clock_domain_8bit and clock_domain_16bit were closed.

With this method, circuit multiplexing of multi-precision operation and power saving of different precision operation can be realized.

V. SEGMENTATION NEURAL NETWORK
Currently, in the medical field, classic U-Net is widely used in medical treatment [36]. In this study, based on the U-Net, a method of yeast cell segmentation based on the convolutional neural network was proposed. This neural network algorithm can use a large amount of data to learn the features of the yeast image to distinguish between yeast cell and background.

Due to the lower resolution of the images captured by the lensless system, it is necessary to fine-tune the U-Net structure so that it can effectively segment low-resolution images. Therefore, the improved network is called optimized U-net (OU-Net). The improved network structure shortens the training time and improves the segmentation accuracy.

In the U-Net structure, there were many network layers. However, the large number of convolution layers will cause overfitting. Therefore, the experiments were conducted for optimizing the convolution layer number. The segmentation accuracy test results of different layers are shown in Fig. 8. From the result, OU-net reduced the number of network layers to 5 layers.

In order to determine the size of the convolution kernel, experiments of different convolution kernel sizes were conducted. The segmentation accuracy tests of different convolution kernel sizes are shown in Fig. 9. Compared with the larger convolution kernel of U-Net, the smaller convolution kernel has better segmentation effect. At the same time, fewer convolution kernels also shorten the training time and reduced the complexity of the network. Therefore, a $3 \times 3$ convolution kernel is uniformly used in the OU-net structure.

The OU-Net structure is shown in Fig. 10. The network extracted 6 feature maps. For extracting more information from the image, 12 feature maps were extracted through Conv3. Then the network entered the up-convolution operation, and the up-convolution will fuse the multi-scale feature map together. The first up-convolution combined the features of Conv2 and Up1, and the second up-convolution combines the features of Conv1 and Up2. Among them, the activation function of each layer of convolution used the ReLU activation function to improve the training speed and high segmentation accuracy.

According to the test results, the proposed OU-Net network model can extract the features of low-resolution yeast cells collected by the image acquisition module to achieve the purpose of segmentation. And the segmentation accuracy was 97.44%. Compared to the U-Net network, the network parameters were greatly reduced. Besides fewer network parameters also shortened the training time and facilitated network transplantation. The segmentation effect diagram is shown in Fig. 11.
VI. RESULTS AND DISCUSSION

The experiment is divided into four parts. The first part is to observe the training process and confirm the normal operation of the training platform. The second part is the analysis of multi-level precision operation, including segmentation accuracy, power consumption analysis. The third part is the simulation of battery power based dynamic precision control. The fourth part is the comparison and analysis of the overall equipment cost size and weight.

A. YEAST CULTURE EXPERIMENT

As shown in the lensless sampling diagram below, it is the culture process of yeast in the culture system, and the shooting time is 4 hours and 8 hours respectively in the initial state. With the change of culture time, the cells gradually split and yeast gradually increased. This experiment shows that the proposed yeast cell culture platform can complete yeast cell culture in vivo.

B. ANALYSIS OF MULTI-LEVEL PRECISION OPERATION

In order to determine the influence of multi-level accuracy on the operation recognition rate, experiments with different accuracy recognition rate are arranged. Table 3 shows the accuracy at all precisions with the BCO algorithm. With the decrease of accuracy, the recognition rate is basically maintained at int8 and higher accuracy, and it is greatly reduced at int4.

There were many previous researches on yeast cell segmentation [39]–[41]. Different from our paper, these researches are based on the microscope, high-performance computer and large-scale laboratory equipment. In Table 4, the segmentation recognition rate of our study is compared with these previous works. The recognition rate of this paper is the same level as the works based on the microscope, high-performance computer and large laboratory equipment. This is a very exciting result, because our platform is miniaturized equipment with lensless sensing, and its cost and portability are much better than large laboratory equipment based on microscope and high-performance computer.

In order to clarify the effect of the complement optimization algorithm, the circuit area experiment and circuit power consumption experiment which are not used in different precision and required by complement optimization algorithm are arranged. The circuit comprehensive implementation is carried out on the design compiler of Synopsys, and the target library is 28nm. The area result is shown in the table below. In the area experiment, the BCO circuit area decreased by average 18.11% in all the precisions.

Then, the power consumption of the circuit is simulated on the Synopsys’ spyglass. First, the power consumption of a single multiplier is simulated. The power consumption results of a single multiplier are shown in Fig. 14. After using BCO algorithm, the power consumption of single multiplier decreased obviously An average of 24.77% area decreased in all precisions, and int8 and int16 decreased more significantly, with 32.84% and 32.53% respectively.

Then the power consumption of the whole convolution unit is shown in Fig. 15. From the power consumption experiment, the power consumption of the convolution unit circuit using the BCO algorithm is also significantly reduced when maintaining the accuracy. The average decrease percentage of all precision is 23.51%. Int16 is the most decreased precision, with a decrease ratio of 30.08%.

C. BATTERY POWER LEVEL BASED DYNAMIC PRECISION

In this part, the relationship among power, working time and segmentation accuracy corresponding to different precision are analyzed. Suppose a 3A battery’s electric quantity

| TABLE 3. Segmentation accuracy of different precisions. |
|--------------------------------------------------------|
| float32 | float16 | int16 | int8 | int4 |
| segmentation accuracy | 97.44% | 96.98% | 96.80% | 95.27% | 50.32% |
| accr_drop | - | 0.46% | 0.64% | 2.17% | 47.12% |

| TABLE 4. Accuracy comparison with previous works. |
|--------------------------------------------------|
| [39] | [40] | [41] | ours int16 | ours int8 |
| segmentation accuracy | 97.5% | 95.0% | 92.3% | 96.8% | 95.3% |

FIGURE 12. Yeast cell culture process (a) initial status (b) 4 hours later (c) 8 hours later.

FIGURE 13. Area and area drop of different precision.
is 1000mAh, and the DCDC conversion efficiency is 97% (a common conversion efficiency), and the circuit working voltage is 1V. The coefficient of efficiency (COE) is defined as:

\[ \text{CoE} = \left( \frac{\text{accuracy}^2}{\text{power}} \right) \times 10 \]

For example, the FoM of precision int8 is \((94.50\%)^2 / 0.016896w) \times 10 = 0.5372\).

From the results, int8 has the best FOM, which shows that the balance between accuracy and power consumption is best at precision int8.

Then we do experimental research on different battery power and operation precision gear setting strategies, among which the highest precision is fixed fp16 and the longest endurance is fixed int4.

Three dynamic precision modes are designed to meet the requirements of different customers. Table 5 shows the battery level based dynamic precision modes, the percentage value in the table is the battery electric level percentage.

The three dynamic precision modes are: high performance mode, high battery life mode and balance mode.

D. COST AND EQUIPMENT SIZE

The cost of equipment has an important impact on the promotion of the living cell culture platform, and the size and weight of the platform package are also the most important parameters for the portability of the equipment. Therefore, the cost, size and weight of our equipment are analyzed and compared with the previous works. The California University
algorithm dedicated circuit and dynamic precision control method were proposed. With the methods, the culture platform achieved a great balance between accuracy and battery duration. The area of the BCO algorithm circuit with all accuracy is reduced by 18.11% on average. The average power consumption of all accuracy is reduced by 23.51%. In addition, a microcolumns-based three-port input microfluidic structure was designed for better yeast culture effect, and the culture process was all in this microfluidic channel chip. Finally, a prototype platform was built, and this prototype can culture yeast cell and collect images and monitor them automatically and independently. The experiments show that the platform has reached the laboratory level. Compared with the Göröcs team’s work, the cost of mass production was reduced by 88.95%, and the equipment volume was 27.1% smaller. This study has proved the feasibility of miniaturization of cell culture equipment. Cell culture equipment can go out of the biological laboratory, which has greatly promoted the biological analysis ability and medical conditions in remote and arduous districts and the early detection of pollution and diseases in these districts.

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