Best CNTFET Ternary Adders?

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Abstract—The MUX implementation of ternary half adders and full adders using predecessor and successor functions lead to the most efficient implementation using the smallest transistor count. These designs are compared with the binary implementation of the corresponding half adders and full adders using the MUX technique or the typical complementary CMOS circuit style. The transistor count ratio between ternary and binary implementations is always greater than the information ratio \( \log_2(3)/\log_2(2) = 1.585 \) between ternary and binary wires.

I. INTRODUCTION

Many ternary half adders and full adders have been presented in the last decade. The most significant papers are [1], [2], [3], [4], [5], [6], [7]. In [8], we have compared different implementations of quaternary adders. The best quaternary one has been presented in [9]. It is based on the use of multiplexers. In this paper, we show that this approach also leads to the best implementation of ternary half and full adders. The design is based on CNTFET technology. This technology is far from being a mature technology. As of 2020, FinFET technology integrates millions of times more transistors than CNTFET technology. However, CNTFET has a big advantage for designing multivalued circuits. While it basically uses the typical CMOS circuit styles, the threshold levels of the different multivalued gates can be got by adjusting the diameter of each used transistor. This technology is used in this paper. We first present the MUX based design of the ternary half adder. Then we present the full adder design. These implementation are compared with the similar MUX based implementation and the conventional implementation of the binary versions.

II. TERNARY HALF ADDERS

Table I presents the truth table of the ternary half-adder. Ternary half adders and full adders have ternary inputs and outputs and binary carry inputs and outputs.

- Ternary values (0,1,2) corresponding to 0, \( V_{dd}/2 \) and \( V_{dd} \) voltage levels
- According to the circuit style that is used, the binary values may have levels 0 and \( V_{dd}/2 \) or 0 and \( V_{dd} \).

The technique used in [9] is based on multiplexers. In this approach, the carry signals are used as control inputs of MUX: they are never used as input values of these MUX. The binary levels are thus 0 and \( V_{dd} \). The corresponding binary values are 0 and 2.

Computation of the Half Adder SUM is processed by the following rules:
- When \( X = 0 \), SUM = Y
- When \( X = 1 \), SUM = \((Y+1) \mod (3)\). The corresponding circuit is called successor circuit.
- When \( X = 2 \), SUM = \((Y-1) \mod (3)\). The corresponding circuit is called predecessor circuit.
- According to \( X \), a ternary MUX provides the correct SUM output.

Threshold detectors circuits are implemented by the inverters NI and PI, according to Table 2. These inverters are generally called NTI and PTI, but this is confusing as they are binary inverters: the outputs are binary ones and they only have one threshold level. The only difference with typical binary inverters is the specific threshold levels. Assuming \( V_{dd} \), \( V_{dd}/2 \) and 0 ternary levels, the threshold levels are \( V_{dd}/4 \) and \( 3V_{dd}/4 \) when the threshold level of a binary inverter is \( V_{dd}/2 \). The NI and PI threshold levels are obtained by choosing the appropriate diameter for the different CNTFET transistors. They are shown in left part of Figure 1. The implementation of the ternary MUX is shown in right part of Figure 1.

Figure 2 presents the Successor and Predecessor circuits with two power supplies (\( V_{dd} \) and \( V_{dd}/2 \)). A, B, C, D outputs of NI and PI inverters control the different transistors: for each ternary input X, only one path is active between \( V_{dd} \) or \( V_{dd}/2 \) or ground and the corresponding output. The drawback of this approach is the supplementary power supply. Figure 3 presents the successor and predecessor circuits with only one power supply (\( V_{dd} \)). The intermediate level is got through a voltage

| Table I | Half Adder Truth Table |
|---------|------------------------|
| X/Y    | SUM | CARRY |
| 0/0    | 0   | 0     |
| 0/1    | 1   | 0     |
| 0/2    | 2   | 0     |
| 1/0    | 0   | 1     |
| 1/1    | 1   | 0     |
| 1/2    | 2   | 0     |
| 2/0    | 1   | 1     |

| Table II | NI and PI Binary Functions |
|----------|-----------------------------|
| NI      | 0 1 2 |
| PI      | 2 0 2 |
divider by using resistor-like transistors. The drawback of this approach is a static power dissipation when the output is 1.

![Fig. 1. Threshold detectors and ternary MUX (Ternary inputs and ternary control)](image)

Figure 4 presents the ternary half-adder circuit. The carry output is:
- When \( X = 0 \), \( C_{\text{out}} = 0 \)
- When \( X = 1 \), \( C_{\text{out}} = 1 \) if \( Y = 2 \) (\( \text{PI}(Y) = 2 \) according to Table 2)
- When \( X = 2 \), \( C_{\text{out}} = 1 \) if \( Y \geq 1 \) (\( \text{NI}(Y) = 2 \) according to Table 2)

Table III presents the transistor count for the half adders.

Table IV presents the transistor count for different ternary half adders proposed in the last ten years.

III. TERNARY FULL ADDERS

When \( C_{\text{in}} = 0 \), the full adder truth table was presented in Table 1 (half-adder). When \( C_{\text{in}} = 1 \), the truth table is given in Table V.

![Fig. 2. Successor and Predecessor Circuits (2 power supplies)](image)

![Fig. 3. Successor and Predecessor Circuits (1 power supply)](image)

![Fig. 4. Ternary Half Adder](image)

### Table III

| Technology | 2 PS | 1 PS |
|------------|------|------|
| Succ-Pred  | 8    | 14   |
| MUX        | 16   | 16   |
| PI-NI      | 16   | 16   |
| NOT        | 2    | 2    |
| **TOTAL**  | 42   | 48   |

Still using the MUX approach, the SUM output of the full adder is given by
- If \( C_{\text{in}} = 0 \), then \( \text{SUM}_{FA} = \text{SUM}_{HA} \) else \( \text{SUM}_{FA} = (\text{SUM}_{HA} + 1) \mod (3) \)

Another approach directly computes \( \text{SUM}_{FA} \) as a function of \( C_{\text{in}} \) and \( X \).
- When \( X = 0 \): if \( C_{\text{in}} = 0 \) then \( \text{SUM} = Y \) else \( \text{SUM} = (Y+1) \mod (3) \).
- When \( X = 1 \), if \( C_{\text{in}} = 0 \) then \( \text{SUM} = (Y+1) \mod (3) \) else \( \text{SUM} = (Y-1) \mod (3) \).
- When \( X = 2 \), if \( C_{\text{in}} = 0 \) then \( \text{SUM} = (Y-1) \mod (3) \) else \( \text{SUM} = Y \).

\( C_{\text{out1}} \) is the carry output when \( C_{\text{in}} = 1 \):
- When \( X = 0 \), \( C_{\text{out1}} = 1 \) if \( Y = 2 \) (\( \text{PI}(Y) = 2 \) according to Table 2)
- When \( X = 1 \), \( C_{\text{out1}} = 1 \) if \( Y \geq 1 \) (\( \text{NI}(Y) = 2 \) according to Table 2)
- When \( X = 2 \), \( C_{\text{out1}} = 1 \)

### Table IV

| Technology | 1   | 2   | 3   | 4   | New 2 PS | New 1 PS |
|------------|-----|-----|-----|-----|----------|----------|
| Transistor count | 136 | 112 | 112 | 85  | 42       | 48       |

### Table V

| X/Y | SUM | CARRY |
|-----|-----|-------|
| 0/0 | 0   | 0     |
| 0/1 | 1   | 0     |
| 1/0 | 0   | 0     |
| 1/1 | 1   | 1     |
| 2/0 | 1   | 1     |
| 2/1 | 1   | 1     |

![Screen capture of a document page with various diagrams and text content relating to ternary logic and circuit design, including figures and tables discussing threshold detectors, MUX, half-adder circuits, and adder design considerations.](image)
If $C_{in} = 0$ then $C_{outFA} = C_{outHA}$ else $C_{outFA} = C_{out1}$

**Fig. 5. Ternary Full Adder (version 1)**

**Fig. 6. Ternary Full Adder (version 2)**

Figure 5 and Figure 6 use two new different types of MUXes:
- MUXes with ternary inputs and binary control;
- MUXes with binary inputs and binary control.

Both types use the same typical MUX2 binary circuit (Figure 7)

**Fig. 7. Typical MUX2 with binary control**

**IV. COMPARING WITH BINARY ADDERS**

**A. Binary Half Adder**

Using the same MUX technique, the binary half-adder is shown in Figure 8. It uses 12 T. Permuting the MUX inputs and adding an output inverter would lead to 14 T with restored output levels. The transistor count is then the same as a typical conventional approach used in standard cell libraries [10], as shown in Figure 9.

**Fig. 8. Binary Half Adder (MUX technique)**

**B. Binary Full Adder**

With the MUX approach, the binary full adder is presented in Figure 10. It corresponds to the following rules:
- If $C_{in} = 0$ then $SUM_{FA} = X \oplus Y$ else $X \oplus Y$.
- XOR and NXOR functions are implemented using MUXes.
- If $C_{in} = 0$ then $C_{out} = X \cdot Y$ else $C_{out} = X + Y$.

The MUX based full adder has 30 T. A version with restored output levels would have 34 T. It could be outlined that

**Table VI**

| Carry | SUM V1 | SUM V2 | FA-V1 | FA-V2 |
|-------|--------|--------|-------|-------|
| 0     | 12     | 8      | 16    | 16    |
| MUX3  | 16     | 8      | 16    |       |
| MUX2  | 4      | 4      | 4     |       |
| PI-NI | 0      | 24     | 16    |       |
| NOT   | 6      | 2      | 2     |       |
| TOTAL | 26     | 50     | 46    | 76    | 72    |

**Table VII**

| Carry | SUM V1 | SUM V2 | FA-V1 | FA-V2 |
|-------|--------|--------|-------|-------|
| 0     | 21     | 14     | 14    |       |
| MUX3  | 16     | 8      | 16    |       |
| MUX2  | 4      | 4      | 4     |       |
| PI-NI | 0      | 24     | 16    |       |
| NOT   | 6      | 2      | 2     |       |
| TOTAL | 26     | 59     | 52    | 83    | 78    |

**Table VIII**

| Ternary Full Adder | Table | 5   | 6   | 7   | Proposed |
|--------------------|-------|-----|-----|-----|----------|
| TC (2 power supplies) | 106  | 132 | 72  |     |
| TC (1 power supply)  | 142  | 153 | 78  |     |
the MUX approach has more transistors than the typical conventional full adder with complementary CMOS shown in Figure 11. Many proposals using less than 28 T have been proposed in the literature.

Fig. 9. 14 T binary Half Adder)

Fig. 10. Binary Full Adder (MUX technique)

Fig. 11. 28 T binary Full Adder)

V. CONCLUSION

The proposed ternary half adders and full adders have less transistors than all the previously proposed ones. It seems that the MUX approach with successor and predecessor circuits is the best one to implement ternary arithmetic circuits. It looks like the transistor counts are close to the minimal possible value. The only valid comparison between ternary and binary circuit is based on the information ratio. According to Shannon theory of information, when N events have the same probability to occur, the corresponding amount of information is \( I = \log_2(N) \) bits (or Shannon). When \( N = 2 \), \( I = 1 \) bit. When \( N = 3 \), \( I = 1.585 \) bits. A ternary wire carries 1.585 times the amount of information of a binary one. This 1.585 information ratio must be used to compare binary and ternary circuits. For instance, an 8-bit binary adder can be compared to a 5-trit ternary adder as they process approximately the same amount of information. 8/5 is close to 1.585. The difference results from rounding issues. Considering the most conservative implementation of binary circuits, the transistor count ratio between ternary and binary half adder is 42/14 = 3 and 72/28 = 2.57 for the full adder when using two power supplies for the ternary case. With only one power supply, the ratios are respectively 48/14 = 3.4 and 78/28 = 2.8. Both ratios are greater than 1.585. It means that the best ternary implementation leads to more transistors, more chip area, more interconnects and more power dissipation than the corresponding conservative binary ones. These results are not surprising. 3 is not the best base for computation and multivalued circuits are restricted to a small niche.

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