Design of Optimized Radix-4 FFT Processor with Multiplier Sharing Method

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Abstract. To implement the parallel pipelined FFT architecture in OFDM applications. The OFDM has developed in wide band Digital communication. The radix4 algorithm can achieve to reduce the half computational steps compare than the radix2 algorithm and R4MDC is reduces the slices and power consumption than the single path delay feedback. It can be converted into real and imaginary values. To reduce the twiddle factor complexity by using the bit parallel multiplier. It can be exploits the constant twiddle factor when the twiddle factor multiplications in timing process. The changes can be appeared in multiplications so have to perform the TF at clock signals in two ways data path.

Keywords OFDM, FFT, MDC, BPM, SDF.

1. Introduction
In General, the FFT can make simple stand most effective optimizations when the number of samples to be transformed is an exact power of two, for which it can eliminate many unnecessary operations. The results of the FFT are the same with DFT, the only difference is that the algorithm usually runs much faster and less resources [1]. In algorithm terms, the DFT takes O(N²) arithmetic operations to be computed, whereas the FFT takes O(Nlog₂N) arithmetic operations. There are two basic DFT algorithm decimation in time and decimation in frequency [2-4]. This algorithm decomposes even and odd-indexed frequency samples

\[ X(2k) = \sum_{n=0}^{N-1} [x(n) W_N^{2nk}] \]

\[ = \sum_{n=0}^{N/2-1} [x(n) W_N^{2nk}] + \sum_{n=0}^{N/2-1} [x(n + n/2) W_N^{2k(n+N/2)}] \]

\[ = \sum_{n=0}^{N/2-1} [x(n) W_N^{2nk}] + \sum_{n=0}^{N/2-1} [x(n + n/2) W_N^{2kn}] \]

\[ \sum_{n=0}^{N/2-1} [(x(n) + x(n + N/2)) W_N^{kn}] \]
\[
X(2k+1) = \sum_{n=0}^{N/2-1} [x(n) + W_N^{N/2} x \left(n + \frac{N}{2}\right)] W_N^{(k+1)n}
\]

\[
X(4k_1 + l) = \sum_{k=0}^{N} [x(n) + x \left(n + \frac{N}{4}\right)] W_4^l + x \left(n + \frac{N}{2}\right) W_4^{2l} + (n + \frac{3N}{4}) W_4^{3l} W_N^{n l} W_4^{n k_1}
\]

\[l = 0, 1, 2, 3; k_1 = 0, 1, 2, 3 \cdots \frac{N}{4} - 1\]

FFT is a fastest method for finding DFT. There are many kind of algorithms and architecture available for FFT. This section will review commonly using algorithm and architectures. Decomposing the frequency samples in to 2 bins (one each for odd and even samples) gives the Radix-2 Algorithm. Increasing the number of bins to 4 gives the Radix-4 Algorithm.

Table 1.1 Twiddle factor multiplier required for Radix-4FFT

| Stage I    | Stage II                  |
|------------|---------------------------|
| \(W_{16}^0\) | 1                         |
| \(W_{16}^1\) | 0.9238-j0.3826            |
| \(W_{16}^2\) | 0.707-j0.707              |
| \(W_{16}^3\) | 0.3826-j0.9238            |
| \(W_{16}^4\) | -j                        |
| \(W_{16}^5\) | -0.3826-j0.707            |
| \(W_{16}^6\) | -0.707-j0.707             |
| \(W_{16}^7\) | -0.9238-j0.3826           |

Radix-4 FFT processor reduces half of the computational steps than Radix-2 FFT. Hence, Radix-4 FFT is preferred in this research work for alleviating the architectural performances of frequency modulation technique of OFDM system. The FFT architecture basically divided into the Two types. There is sequential processor, pipeline processor. Here using pipeline processor in R4MDC Multipath Delay Commutator (MDC) architecture reduces the hardware slices and power consumption of the FFT processors than Single Path Delay Feedback (SDF [3]). As shown in architecture of R4MDC, input data is shifted according to their appropriate delay positions. Commutator unit is used to re-arrange the one form of signals into another form of signal. On the other hand, Butterfly unit is used to add and subtract
the signed bit values. Appropriate delays are used to determine proper frequency response in appropriate
delay positions. If there is more number of samples are included in FFT processes, signal strength should
be increased while performing data communication. Due to merging the real and imaginary values of
complex input values, it is possible to reduce the half of the accumulation and subtract or units while
calculating FFT processes. [1] However, it requires more delay for exhibiting frequency transformation
process.

![Diagram of MDC Radix-2 Multi-path Delay Commutator](image)

**Figure 1. Architecture of MDC**

Radix-2 Multi-path Delay Commutator is the most classical approach for pipeline implementation of
radix-2 FFT algorithm. As shown in Fig.3.7, the input sequence has been broken into two parallel data
stream flowing forward, with correct distance between the data elements entering the butterfly scheduled
by proper delays. Both butterfly and multipliers are in 50% utilization. In certain applications like
Multiple-input Multiple-output (MIMO) Antenna systems, the first commutate at the input data stream
can be can replaced with 2 such commutates to keep the pipeline components 100% utilized. The
output data rate for this structure is twice the clock frequency and that is what makes it appealing for
high-speed applications [10-11].

Multiplication of twiddle factor value 0.707 requires 4 numbers of shifters and three number of adder to
perform multiplication.

![Bit parallel multiplication for twiddle factor 0.707](image)

**Figure 2. Bit parallel multiplication for twiddle factor 0.707**

Similarly, twiddle factor multiplication of 0.9238 and 0.3826 with constant input $x$ is illustrated in fig.
8 and fig. 9 respectively. Multiplication of twiddle factor value 0.9238 requires 5 numbers of shifters
and single adder to perform multiplication. Similarly, 0.3826 require two shifters and single adder to
perform multiplication. In this research work, we can realize these BPM based complex multiplier to
further reduce the hardware components. For the twiddle factor multiplication of 0.707, Equation (11)
can be further simplified based on taking common factor for reducing the number. Also equation (11)
can be write combinational circuit design is described. This technique allows reducing power
consumption, propagation delay and area of digital circuits while maintaining low complexity of logic design.

Figure 3. Bit parallel multiplication for twiddle factor 0.9238

Figure 4. Bit parallel multiplication for twiddle factor 0.3826

2. Architecture analysis and Design
As we mentioned in this section, the data flow structure of Radix-4 FFT has been illustrated in figure 2. Each stage of Radix-4 FFT performs two stage of Radix-2 FFT. For Radix-4, \( N = r^v = 4^v \) where \( v \) is number of stage and \( r \) is the radix of FFT [6].

Figure 5. Data Flow structure of 16 point Radix-4 FFT
\[ Y[K] = \sum_{n=0}^{N-1} y(n)W_N^{nk} + \sum_{n=N/4}^{N-1} y(n)W_N^{nk} + \sum_{n=N/2}^{N-1} y(n)W_N^{nk} + \sum_{n=3N/4}^{N-1} y(n)W_N^{nk} \]

\[ Y[K] = \sum_{n=0}^{N-1} y(n)W_N^{nk} + \sum_{n=0}^{N/4} y(n)W_N^{(n+N/4)k} + \sum_{n=N/4}^{N-1} y(n)W_N^{(n+N/2)k} + \sum_{n=3N/4}^{N-1} y(n+3N/4)W_N^{nk} \]

\[ Y[K] = \sum_{n=0}^{N-1} y(n)W_N^{nk} + W_N^{Nk/4} \sum_{n=0}^{N-1} y(n+N/4)W_N^{nk} + W_N^{Nk/2} \sum_{n=0}^{N-1} y(n+N/2)W_N^{nk} + W_N^{3Nk/4} \sum_{n=0}^{N-1} y(n+3N/4)W_N^{nk} \]

where the twiddle factor values are given as,

\[ W_N^{Nk/4} = \left[ \cos\left(\frac{2\pi}{4}\right) - j\sin\left(\frac{2\pi}{4}\right) \right]^k = (-j)^k \]  

\[ W_N^{Nk/2} = \left[ \cos\left(\frac{2\pi}{2}\right) - j\sin\left(\frac{2\pi}{2}\right) \right]^k = (-1)^k \]

\[ W_N^{3Nk/4} = \left[ \cos\left(\frac{2\pi*3}{4}\right) - j\sin\left(\frac{2\pi*3}{4}\right) \right]^k = (j)^k \]

Radix-4 FFT processor reduces half of the computational steps than Radix-2 FFT. Hence, Radix-4 FFT is preferred in this research work for alleviating the architectural performances of frequency modulation technique of OFDM system [7-10].

3. Simulation and Results

This OFDM application has been used in various categories of digital system in this design technologies in present state of developed implementation of power consumption is major problem in the design to overcome the disadvantage of the twiddle factor complexity, increase speed, increase speed. Simulation of Proposed Modified BPM based Radix-4 MDC FFT architecture has been illustrated in figure 5.1. As shown in Figure 6, to push the sequential inputs starting from 0+0i, 1+1i, 2+2i, and 3+3i ...63+63i in first 16 successful clock cycles. After 16 clock cycles, outputs are sequentially getting from designed Radix-4 MDC FFT.
Figure 6. shows the simulation result of the Radix4 16 point FFT

Figure 7. synthesis report in power summary

The figure 1.6 shows the synthesis report in Xilinx and gives the minimum period 22.04ns compare then the existing and the frequency in before and after clock is 23.24 computational delay is 23.241.

Figure 8. Area analyzer summary

Using the bit parallel multiplier it has the four no of adder and three no of shifters.it shows the area analysis report in Xilinx.and gives reduced slices and LUT compare existing in slices is 1299 and
proposed is 1025 have been reduced and LUT is 2193 into 1761 have been reduced. The XPower Analyser tool is used to measure the amount of power consumed during the operations. Here it used to calculate both the static and dynamic power. The power level can be increased or modified based on the switching activities of CMOS in hardware. So it’s necessary to choose the good SDK tool to implement this. The screen shots of power simulation is shown in Fig 5.3.

Fig 9 shows the output analysis of power consumption to compare than existing SDF architecture in reduced eight percentages. An RTL description is usually converted to a gate-level description of the circuit by a logic synthesis tool [11]. The synthesis results are then used by placement and routing tools to create physical layout. Logic tools may use a design's RTL description to verify its correctness. The RTL view of top level module is shown in Figure 10.

4. Conclusion
By using the FFT processor, the chip area reduced and speed is increased and frequency is achieved by reducing the computation stages. The proposed architecture provides low complexity, high speed and also reduces the chip area. In future this low complexity FFT processor will be used to implement in Radix-64 FFT. By using this processor is will reduces the Twiddle Factor multiplication complexity, speed and frequency is increased and reduction in power consumption are achieved. So this will be used in various research applications.
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