Improvement of Corrosion Process for Gate Commutated Thyristor Chips

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Abstract. In recent years, with the continuous development of installed grid capacity and renewable energy, DC power transmission and distribution technologies have developed rapidly. As one of the most important high power semiconductor devices, the integrated gate commutated thyristor (IGCT) has great potential in DC grid application. The gate-cathode blocking property is the key for device packaging and working. Based on the corrosion process of the GCT chip, two methods are proposed for improving the consistency of gate-cathode blocking voltage in this paper.

Introduction

With fast growing power generation capacity and evolving clean energy, DC transmission and distribution technologies have developed rapidly recent years, due to advantages such as large transport capacity, extra long-distance transportation and lower loss. Integrated gate commutated thyristor (IGCT) is a kind of fully controlled power electronic device and its excellent blocking voltage and high current turn-off capability make it suitable for high-capacity applications such as DC breakers[1, 2] and SVCs, etc. However, there are many important factors influencing the usage of IGCT, the properties between gate and cathode is one of them.

This paper analyzes and discusses the corrosion process of the GCT chip part of IGCT, and proposes two corrective methods from the aspects of process sequence and process operation based on process and device simulation results.

Process Introduction of Gate-Cathode Units

Figure 1 shows the schematic of the integrated gate commutated thyristor (IGCT), which consists of the GCT chip, the housing package and the gate drive circuit. The turn-off process of IGCT is shown in Figure 2[3], through the instant applied reverse voltage provided by the gate driver between gate and cathode, the cathode current is transferred to the gate. After this transformation, the device changes into an open-gate PNP transistor and turns off the current gradually.

![Figure 1. The schematic of an IGCT.](image)

To complete the transformation successfully, the PN junction between the gate and the cathode must withstand the reverse voltage applied by the external drive. Any PN junction unit with a lower
voltage than the given voltage will cause the whole device’s failure. However, if there’s any PN junction with a too high blocking voltage, then the doping around this area will do harm to the current commutation process[4]. As a result, it’s important to keep the consistency of the PN junction units throughout the device through fabrication process.

The structure diagram of a single cathode unit of the GCT chip is described in Figure 3. A cathode unit is composed of the N+ emitter region, the P+ base region, the moat shape[5], and the passivation layer between gate and cathode. Both the N+ emitter region and the P+ base region are fabricated by conventional doping diffusion method. And the passivation layers are composed of silicon dioxide and organic layer. The moat shape is performed by wet etching process, which determines the withstand voltage of the PN junction together with the N+ emitter region and the P+ base region.

Early papers discussed the gate-cathode blocking property based on small-sized devices (mainly 2-inch ones) [6, 7], but these papers did not discuss it in detail from the aspect of the fabrication process. As the size of the wafer grows, the number of gate-cathode units on the device increases, changing from tens of hundreds (2-inch) to thousands or ten thousand (4-inch and 6-inch). So the discussion on the consistency of the gate-cathode blocking property of the device is becoming more and more important.

**Improvement of Corrosion Process**

**Optimization of the Fabrication Process Sequence**

The optimization tries to reduce the lithography errors of the fabrication. To study the effect of the lithography errors, a sequence of simulations were made based on different lithography errors. The magnified views of the PN junctions at the sidewall or the bottom is shown in Figure 4, with the absolute doping profiles below the surface.
And the results are shown in Figure 5. When the PN junction is at different positions on the sidewall of the moat shape, the gate-cathode unit blocking voltage changes. And the changes are mainly decided by the P+ base region doping of junction below the sidewall surface. It should be noticed that when the position is near the bottom of the moat shape or at the bottom of the moat shape, the voltage changes little.

Usually there are two ways to realize the fabrication of gate-cathode units. For process sequence 1, the N+ emitter region is firstly fabricated and then the moat shape is etched, so there are two steps of lithography processes. And more random errors will appear between the two steps, so the junction asymmetry of the gate-cathode unit is more likely to occur, which causes the blocking voltage to deviate from the design level. As a result, the consistency of the gate-cathode unit blocking voltage becomes worse.

The improved way is to etch the moat shape after the pre-deposition of the impurities of the N+ emitter region, and then to diffuse the impurities at high temperature. Through the movement of the impurities in the silicon lattices, the symmetry of the gate-cathode unit is more easily realized. So the consistency of the gate-cathode unit blocking voltage will improve compared with process sequence 1.
Optimization of the Corrosion Operation Process

To make the moat shape, the traditional wet etching process is adopted. The main steps include the etching step in the etchant solution and the flushing step in the deionized water. After the etching step, it is necessary to transfer the wafers quickly into the deionized water for acid flushing to avoid extra local etching. However, not only the speed of transfer process but also the position of the wafers will cause extra local etching.

As shown in the Figure 8, when the cathode side (including the moat shape) of the wafer faces upwards during the transfer process, the acid drops accumulate at the corners of the moat shape easily and produce extra local corrosion, resulting in the micro pits at the corners. When the anode side of the wafer is placed upwards during the transfer process, the drops tend to fall down, keep the corners from getting extra corrosion.
To study the influences of these micro pits at the corner, different shapes of the gate-cathode units are created by Athena in Silvaco based on the fabrication process parameters. And then the gate-cathode blocking property sweeping is made. When the junction is at the micro pits, it can be seen from the results that the gate-cathode units with micro pits have higher blocking voltage, which means the lower doping in the P+ base region below the surface. Because of the random of the micro pits and the junction positions, there will be different doping in the P+ base region, which will do harm to the current commutation process of IGCT. And the fabrication should try to avoid this situation.

Figure 8. The comparison of different wafer positions during the corrosion process and the fabrication results.
(a: the cathode side faces upwards; b: the SEM of the sample when the cathode side faces upwards; c: the anode side faces upwards; d: the SEM of the sample when the anode side faces upwards)

Figure 9. Comparison of doping of gate-cathode units with different moat shapes.

115
Conclusion

In this paper, the consistency of the blocking voltage of gate-cathode units on the GCT chip is studied. The asymmetry of the gate-cathode junction and the micro pits at the corner of the moat shape will affect the blocking voltage obviously. Based on these problems, two methods are brought up to improve the gate-cathode unit blocking voltage distribution.

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