A 21.56 dBm Four-way Current-Combining Power Amplifier for Ka-band Applications in 65-nm CMOS

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Abstract This paper presents a four-way current-combining Ka-band power amplifier (PA) in 65-nm CMOS technology. A symmetrical transmission line based four-way current combiner, together with output transformers, is used to transfer the high load impedance (4*Z_L) to the desired Z_INT for each power unit cell. Besides, both inter-stage/input flexible matching transformers and the power splitter are optimized to improve the performance. Based on the methodology mentioned above, the power amplifier demonstrates a small-signal gain of about 24.12 dB, a saturated output power of 21.56 dBm, and a peak power-added efficiency of 27.3% at 35 GHz.

key words: Four-way current-combining, power amplifier, transmission line based combiner, flexible transformer

Classification: Microwave and millimeter wave devices, circuits, and hardware

1. Introduction

The demand for high data-rate wireless communication systems grows rapidly in these years [1,2,3,4]. Therefore millimeter-wave band circuits are popular in these decades because of the broad bandwidth [5]. System designs and circuit blocks for Ka-band (26.5 GHz-40 GHz) have been reported lately, such as Ka-band receiver or transceiver [4,5], power amplifier [6], and PLL [7]. Among these systems power amplifier (PA) is one of the most significant blocks. The output power of the power amplifier determines the communication distance of the system [2,8]. Due to the advantage of high-level integration and potentially low cost, CMOS technology is a good choice for millimeter-wave integrated circuits [9]. But the low breakdown voltage of the CMOS core device leads to a big challenge to provide higher output power in millimeter-wave frequency [10]. Therefore the power from a small MOSFET is limited. However, a large output transistor has low output impedance resulting in a high impedance transformation ratio with high insertion loss [10,11,12]. Circuits with large transistors are also sensitive to the device and interconnect parasitics. The big parasitic capacitance of the MOSFET and the gate interconnect resistance result in lower power gain and efficiency [13]. A popular way to overcome these problems and increase the output power is power combining [14,15,16,17,18], but the power combiner brings additional loss [13]. Transformer-based power combining is a popular and attractive way to implement silicon-based PA. Current-combining and voltage-combining are the two main ways for transformer-based power combining [18]. At millimeter-wave frequency, due to parasitic capacitance of the transformer windings, the imbalance problem of the voltage combiner will be severe when the PA using a single-ended output. Fortunately, the layout of the current-combining network can be symmetrical, thus the imbalance can be ignored compared to voltage combiner [9].

In this paper, we present a Ka-band four-way current-combining power amplifier with a symmetrical low loss transmission line based combiner. The transmission line based combiner has four nearly equal input impedance and the characteristic impedance of the transmission line is lower than 50 ohm for low loss and impedance matching. The output transformers and the combiner form the output matching network and transfer the load impedance (Z_L) to the desired optimal Z_opt for each differential pair. Both inter-stage/input flexible matching transformers and the power splitter are optimized to improve the performance. Leveraging the design methodologies mentioned above, the current-combining power amplifier delivers high output power and achieves high power-added efficiency (PAE).

2. Four-way current combiner, flexible matching transformer and input power splitter

Fig. 1(a) shows an ideal current-combining network that has a load of R_L. N symmetrical circuits combine their output power...
currents to generate high power. The voltage on $R_L$ is

$$V_L = (N \times I_N) \times R_L.$$  \hspace{1cm} (1)

The input impedance for each branch of the parallelled current-combining network is

$$Z_{IN} = \frac{V_L}{I_L} = \frac{(N \times I_N) \times R_L}{I_N} = N \times R_L.$$  \hspace{1cm} (2)

According to (2), the input impedance for each branch is $N$ times the load impedance, $R_L$. Considering a transformer-based $N$-way current-combining power amplifier illustrated in Fig. 1(b). The power amplifier consists of $N$ unit cells. Assuming the turn ratio of the transformer is $1:n$ and the coupling coefficient is unit, $V_0$ and $I_0$ are output voltage and current of the unit cell, respectively. $V_L$ and $I_L$ are the magnetically coupled voltage and current on load $R_L$. According to the relationship between voltage and current of an ideal transformer\[19\], we can get the result:

$$V_L = n \times V_0.$$  \hspace{1cm} (3)

and

$$I_L = N \times \frac{1}{n} \times I_0.$$  \hspace{1cm} (4)

where $N$ is the number of the unit cells. From equation (2)(3)(4), the impedance seen by each unit cell is:

$$Z_{opt} = \frac{V_0}{I_0} = \frac{1}{n^2} \times (N \times R_L).$$  \hspace{1cm} (5)

In a four-way current-combining power amplifier, the load seen by each unit cell is as high as $200\Omega$ if the load is a $50\Omega$ resistor. Usually, a matching network with a high impedance transformation ratio is required which results in high insertion loss. For a transformer-based current-combining power amplifier, according to (5), the turn ratio of the transformer must be high to get a low $Z_{opt}$. However, in this situation, one of the winding may be twice (or larger) the inductance of the other winding, which results in increased parasitic resistance and interwinding capacitance\[10\]. High parasitic resistance decreases the $Q$ factor of the winding and increases the insertion loss of the transformer. Parasitic capacitance also decreases the self-resonant frequency of the transformer. In this work, a symmetrical transmission line based combiner with low insertion loss is used to mitigate the high impedance transformation ratio concern. Fig. 2 shows the 3D view of the proposed four-way current combiner (a) and the whole output matching network with transformers (b). There are some advantages of this transmission line based combiner. Firstly, the ground plane of the transmission line not only provides a low-impedance path for the returning current but also minimizes the interaction of the signal with the substrate so that the substrate loss is minimized\[8\]. Secondly, the loss of the microstrip line is mainly due to the parasitic resistance of the signal line and the ground plane. In this work, the signal line is implemented by the top ultra-thick metal 9, and its line width is $12\mu m$. Ultra-thick metal and wide line width both decrease the resistance loss of the signal line. The ground plane formed by the bottom metal 1, metal 2, and metal 3 in parallel promotes its current handling capacity and reduces its ohmic loss. The transmission line characteristic impedance of this power combiner is about 32.36$\Omega$ at 35GHz. In this work, the transmission line based combiner, together with the output matching transformers, transfer the high load impedance($4 \times Z_L$) to the desired $Z_{opt}$ for each branch and combines four differential unit cells efficiently.

As shown in Figure 2, the power combiner has four input ports. Due to the symmetry of the layout, the power combiner obtains nearly equal input impedances ($Z_1$, $Z_2$, $Z_3$, $Z_4$) of its four input ports. At 35GHz, $Z_1= (14.78-j23.66)\Omega$, $Z_2= (14.80-j23.23)\Omega$, $Z_3= (14.91-j23.04)\Omega$, $Z_4= (14.82-j23.76)\Omega$. Fig. 2(b) shows the 3D view of the whole output matching network. Four transformers transfer
the input impedance of the combiner to Z_{opt1} for each PA unit cell, respectively. The output transformers, shown in Fig. 2(b), acting as baluns, transfer differential signals to single-ended signals. The primary winding (metal 9) and the secondary winding (metal 8 paralleled with metal 7) are stacked to increase the coupling coefficient which decreases the insertion loss of the transformer [11, 20]. But there is a certain misalignment between coils to reduce the parasitic interwinding capacitance, thereby increasing the self-resonant frequency of the transformer. In this design, Z_{opt1}=(17.21+j19.68)Ω, Z_{opt2}=(17.18+j19.56)Ω, Z_{opt3}=(17.15+j19.61)Ω, Z_{opt4}=(17.21+j19.71)Ω. at 35GHz, close to the optimal load impedance of the output transistors for maximum output power. The insertion loss of the whole output matching network is 1.7dB. Moreover, the characteristic impedance (Z0) of the transmission line may fluctuate due to process variations. To roughly evaluate the PA performance drift over the characteristic impedance variations, transmission lines with different characteristic impedance (around the designed Z0) are considered for the power combiner and the input splitter. Fig. 3(a) presents the average input impedance of different ports of the four-way current combiner with different Z0. Fig. 3(b) presents the average input impedance of different ports of the whole output matching network with different Z0. Compared to the four-way current combiner, characteristic impedance variations have little effect on the input impedance of the whole output matching network. The performance variations of the circuit from this fluctuation has been described in this paper later.

Fig. 4. 3D view of (a) interstage transformer and (b) input transformer.

Fig. 5. (a) 3D view of input splitter with input pad and (b) Power transfer gain magnitude and phase between input pad and the four output ports of the splitter.

The 3D view of the interstage transformer is shown in Fig. 4(a). The load impedance of interstage matching or input matching network is the input impedance of the transistors in the next stage. Usually, the bottleneck of the bandwidth for a power amplifier is at the interstage or input matching network because of their higher load impedance [2]. In a practical transformer matching network, the parasitic interwinding capacitance also results in a larger ripple in the band [21]. To decrease the ripple for a better bandwidth performance, the interstage and input matching networks are usually implemented by transformers with low coupling coefficient (low k) [2, 21, 22]. As illustrated in Fig. 4(a), the primary winding of the interstage transformer consists of two parts, part-line A and part-line B. Part-line A (L_A) is stacked with the secondary winding to obtain a higher coupling coefficient k1. Part-line B, series with part-line A, as a leakage inductor L_B, is used to achieve a nearly 2:1 turn ratio for matching. The coupling coefficient k between the whole primary and secondary winding is lower than k1 as explained in [2]:

$$k = k_1 \times \sqrt{\frac{L_A}{L_A + L_B}}.$$  

As mentioned above, a smaller k is required for the interstage transformer. In general, the role of part-line A is to provide a relatively high coupling coefficient, and the role of part-line B is to adjust the turn ratio and decrease the coupling coefficient. Therefore this structure is flexible and easy to be realized to get the turn ratio and the coupling coefficient required for interstage matching. For the input transformer, a relatively compact and area-saving structure is adopted, shown in Fig. 4(b). The primary winding is single-turn, and the secondary winding is double-turn. Both turns of the secondary winding are nested with the primary winding which can also increase the coupling coefficient and reduce the insertion loss of the transformer. The primary and secondary inductances (L_{pri}, L_{sec}) of the input transformer are 260 pH and 383 pH, respectively, with k of 0.52. For the inter-stage transformer, primary and secondary inductances are 229 pH and 108 pH, respectively, and the k is 0.34. Fig. 5(a) shows the 3D view of the input splitter with an input pad. Fig. 5(b) shows the gain amplitude and phase between the input pad and the four output ports of the splitter. The gain amplitude differences are smaller than 0.025dB and the phases are nearly equal.

3. Power amplifier design

Fig. 6 depicts the architecture of the proposed four-way current-combining Ka-band power amplifier and the PA unit cell. Each basic unity cell is a pseudo-differential NMOS pair with neutralization capacitors [23], as shown in Fig. 6(b). Each branch consists of two common source stages, biased in class AB. Impedance matching networks are mainly realized by transformers and transmission lines. Shunt resistors are inserted at the gate of both stages to help achieve impedance matching (R_g of 484Ω for the output stage and 1.481kΩ for the driver stage). Dimension of output stage transistor is
2×192 μm for each differential pair determined by the desired output power, while the driver stage is 2×64 μm for each differential pair to provide sufficient power gain and avoid compression. Typically, increasing the finger width results in the increase of the gate resistance and reduces the power gain[24]. On the other hand, increasing the number of fingers results in a large layout area and increases the parasitic capacitance. In this work, 6×32 fingers with finger width 1 μm for the output stage and 2×32 fingers with finger width 1 μm for the driver stage are used for better performance. The parasitic negative feedback caused by $C_{GD}$ between the gate and drain limits the power gain and reverse isolation, and potentially causes instability, especially in millimeter-wave frequency[16,25]. The neutralization capacitors ($C_{N}$) shown in Fig. 6(b) can be used to tackle these problems[16,23]. This technique provides an equivalent negative capacitance (-$C_{N}$) to cancel $C_{GD}$ for higher gain and better reverse isolation. A $C_{N}$ of about 61 fF implemented by a parallel-plate capacitor is selected for the power stage and the $K_{f}$ remains larger than 1 even when $C_{N}$ varies by 29.5% with a lossy transformer at power stage input. The $K_{f}$ of the power stage will improve considering the lossy on-chip output matching network[16]. For the driver stage, the neutralization capacitor is about 20.5 fF.

For common-mode signal, the feedback capacitance between gate and drain is increased from $2C_{GD}$ to $2 \times (C_{GD} + C_{N})$ which potentially degrades the common-mode stability[16,26]. Considering this condition, as shown in Fig. 6(a), a 250 Ω resistor $R_1$ is added in series with the center tap of the input and interstage transformers to suppress common mode oscillation as the case in [26]. The addition of $R_1$ has no severe impact on the output power and power gain in this work. Large resistor $R_2$ and capacitor $C_b$ are used to separate the dc and RF path.

4. Post-layout simulation results and discussion

The proposed power amplifier is designed in 65nm CMOS technology and the design prototype is shown in Fig. 7(a). Dimensions of the whole chip are 1.65 mm×1.494 mm including all pads, while the area of the core is about 1.646 mm$^2$. Fig. 7(b) shows the simulated S-parameters. The small-signal gain is 24.12 dB at 35 GHz, with a 1 dB bandwidth of 3.46 GHz from 32.76 GHz to 36.22 GHz. The 3 dB bandwidth is 6.38 GHz from 31.51 GHz to 37.89 GHz. The input reflection coefficient is lower than -10 dB from 32.82 GHz to 37.15 GHz and the output reflection coefficient is lower than -8 dB from 26 GHz to 47.22 GHz. Reverse isolation is better than -64 dB over the entire Ka-band. The stability factor $K_{f}$ is greater than 47 for all the frequencies. Large signal performance versus input power at 35 GHz is shown in Fig. 8(a). Under 1.1 V supply, the power amplifier achieves a 18.33 dBm OP1dB, while the Psat is about 21.56 dBm. Benefited from the high power gain and low loss output matching network, the maximum PAE is as high as 27.3% at 35 GHz. PAE at OP1dB is also as high as 13.6%. Fig. 8(b) shows the large-signal performance of the PA versus frequency. Fig. 9 depicts the performance variations of the circuit with different transmission line combiners and splitters due to the above-mentioned characteristic impedance drift. When the characteristic impedance changes in the range of 30.53 ~ 34.35 Ω, the maximum $\Delta S_{21}$ is about 0.51 dB in the range of 33 ~ 36 GHz, while the maximum $\Delta P_{sat}$ and $\Delta P_{AE_{MAX}}$ are about 0.25 dBm(21.51 ~ 21.76 dBm) and 0.36%(27.31 ~ 27.67%), respectively, at 35 GHz. Besides, various factors (for instance, the variation of antenna input impedance) impact the loading at the PA output which may degrade the performance of the power amplifier. To roughly estimate the performance drift over this loading variation, Fig. 10 shows the S-parameters and large-signal performance when PA load impedance (RL) changes in the range of 35 ~ 65 Ω. In these load situations, all of the corresponding peak $S_{21}$ are in the range of 23.86 ~ 24.55 dB. At 35 GHz, the $P_{sat}$ fluctuates between 21.24 ~ 21.61 dBm, while the peak PAE fluctuates between 25.92 ~ 27.75%. Therefore, the PA performance has no big differences in the different situations discussed above. Table I summarizes the performance of the designed amplifier and compares it with other state-of-the-art PAs in Ka-band. Thanks to the careful design of the four-way current power combiner, matching transformers, power splitter, and the proper transistor size, the outstanding

![Fig. 6. (a) The proposed four-way current-combining Ka-band power amplifier and (b) Differential common-source PA unit cell with neutralization capacitor.](image)

![Fig. 7. (a) Physical layout of the designed power amplifier and (b) Simulated S-parameters versus frequency.](image)
The performance of the power amplifier is achieved compared to the previously published CMOS power amplifiers around Ka-band.

Fig. 8. Simulated (a) gain, Pout and PAE against input power at 35 GHz and (b) Psat, P1dB, PAEmax and PAE@P1dB versus frequency.

Fig. 9. Simulated (a) S-parameters and (b) large-signal performance at 35GHz with different transmission line combiners and splitters due to characteristic impedance drift.

Fig. 10. Simulated (a) S-parameters and (b) large-signal performance at 35GHz when PA load impedance (RL) changes in the range of 35 to 65Ω.

5. Conclusion

A Ka-band four-way current-combining transformer-based power amplifier in 65-nm CMOS is designed. The transmission line based four-way current combiner and matching transformers are specially designed to improve performance. The amplifier achieves a 21.56 dBm Psat, a 24.12 dB small-signal gain, and a 27.3% maximum PAE under a 1.1 V supply. Leveraging the proposed design methodologies, the PA achieves a higher FoM than other CMOS state-of-the-art power amplifiers in Ka-band listed in Table I. However, the active area of the power amplifier is relatively large compared with those in other works, which should be also improved in future work. The four-way current power combiner presents a suitable way to transfer the high impedance caused by current-combining to a low impedance for each PA unit cell. Together with transformers, this work shows a suitable way to implement multiple way current-combining power amplifiers to obtain high output power in the millimeter-wave band.

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References

[1] Ericsson Mobility Report: The Need for Spectrum Harmonization (2016) https://www.ericsson.com/res/docs/2016/mobility-report/emr-june-2016-the-need-for-spectrum-harmonization.pdf.

[2] H. Jia, C. C. Prawoto, B. Chi, Z. Wang and C. P. Yue: “A Full Ka-Band Power Amplifier With 32.9% PAE and 15.3-dBm Power in 65-nm CMOS,” IEEE Transactions on Circuits and Systems I: Regular Papers 65 (2018) 2657 (DOI: 10.1109/TCSI.2018.2799983).

[3] M. Fujishima: “Recent trends and future prospective on millimeter-wave CMOS circuits,” IEICE Electron. Express 6 (2009) 721 (DOI:10.1587/eelex.6.721).

[4] Z. Li, J. Cao, Q. Li and Z. Wang: “A wideband Ka-band receiver front-end in 90-nm CMOS technology,” European Microwave Integrated Circuit Conference (2013) 5.

[5] B. Ding, S. Yuan, C. Zhao, L. Tao and T. Tian; "A Ka band FMCW Transceiver front-end with 2GHz bandwidth," IEEE/MTT-S International Microwave Symposium - IMS (2018) 887 (DOI: 10.1109/MWSYM.2018.8439346).

[6] C. Yu, J. Feng and D. Zhao: "A Ka-band 65-nm CMOS neutralized medium power amplifier for 5G phased-array applications," IEEE MTT-S International Wireless Symposium (IWS) (2018) 1 (DOI: 10.1109/IWEWS.2018.8400842).

[7] A. Agrawal and A. Natarajan: “A scalable 28 GHz coupled-PLL in 65 nm CMOS with single-wire synchronization for large-scale 5G mm-wave arrays,” IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers (2016) 38 (DOI: 10.1109/ISSCC.2016.7417895).
C. Chou, Y. Hsiao, Y. Wu, Y. Lin, C. Wu and H. B.Heydari, M.Bohsali, E. Adabi and A. M.Niknejad: “A 60 GHz Power Amplifier for D-band Applications in 40-nm CMOS,” IEEE Transactions on Microwave Theory and Techniques 60 (2012) 1365 (DOI: 10.1109/TMTT.2012.2187536).

[10] C. Chou, Y. Hsiao, Y. Wu, Y. Lin, C. Wu and H. Wang: “Design of a V-Band 20-dBm Wideband Power Amplifier Using Transformer-Based Radial Power Combining in 90-nm CMOS,” IEEE Transactions on Microwave Theory and Techniques 64 (2016) 4545 (DOI: 10.1109/TMTT.2016.2623781).

[11] I. Aoki, S. D. Kee, D. B. Rutledge and A. Hajimiri: “Distributed active transformer-a new power-combining and impedance-transformation technique,” IEEE Transactions on Microwave Theory and Techniques 50 (2002) 316 (DOI: 10.1109/22.981284).

[12] S. Pornpromlikit, J. Jeong, C. D. Presti, A. Scudeeri and P. M. Asbeck: “A Watt-Level Stacked-FET Linear Power Amplifier in Silicon-on-Insulator CMOS,” IEEE Transactions on Microwave Theory and Techniques 58 (2010) 57 (DOI: 10.1109/TMTT.2009.2036323).

[13] D. Simic and P. Reynaert: “A 14.8-dBm 20.3-dB Power Amplifier for D-band Applications in 40 nm CMOS,” IEEE Radio Frequency Integrated Circuits Symposium (RFIC) (2018) 232 (DOI: 10.1109/RFIC.2018.8428981).

[14] P. Reynaert and A. M. Niknejad: “Power combining techniques for RF and mm-wave CMOS power amplifiers,” IEEE Eur. Solid-State Circuits Conf. (ESSCIRC) (2007) 115 (DOI: 10.1109/ESSCIRC.2007.4430296).

[15] J. Chen and A. M. Niknejad: “A compact 1V 18.6dBm 60GHz power amplifier in 65 nm CMOS,” IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers (2011) 432 (DOI: 10.1109/ISSCC.2011.5746385).

[16] D. Zhao and P. Reynaert: “A 60-GHz dual-mode class AB power amplifier in 40-nm CMOS,” IEEE J. Solid-State Circuits 48 (2013) 2323 (DOI: 10.1109/JSSC.2013.2275662).

[17] J.-F. Yeh, Y.-F. Hsiao, J.-H. Tsai, and T.-W. Huang: “MMW ultracompact N-way transformer PAs using bowtie-radial architecture in 65-nm CMOS,” IEEE Microw. Compon. Lett 25 (2015) 460 (DOI: 10.1109/LMWC.2015.2427758).

[18] C. Tseng and Y. Wang: “A 60 GHz 19.6 dBm Power Amplifier With 18.3% PAE in 40 nm CMOS,” IEEE Microwave and Wireless Components Letters 25 (2015) 121 (DOI: 10.1109/LMWC.2014.2382682).

[19] Marian K.Kazimierczuk:High-Frequency Magnetic Components(Wiley, New York, 2009) 200.

[21] J. R. Long: “Monolithic transformers for silicon RF IC design,” IEEE Journal of Solid-State Circuits 35 (2000) 1368 (DOI: 10.1109/4.868049).

[22] M. Babaie, R. B. Staszewski, L. Galatro and M. Spitzhofer: “A wideband 60 GHz class-E/F2 power amplifier in 40nm CMOS,” IEEE Radio Frequency Integrated Circuits Symposium (RFIC) (2015) 215 (DOI: 10.1109/RFIC.2015.7337743).

[23] W. L. Chan and J. R. Long: “A 58–65 GHz neutralized CMOS power amplifier with PAE above 10% at 1-V supply,” IEEE J. Solid-State Circuits 45 (2010) 554 (DOI: 10.1109/JSSC.2009.2039274).

[24] B. Heydari, M. Bohsali, E. Adabi and A. M. Niknejad: “A 60 GHz Power Amplifier in 90nm CMOS Technology,” IEEE Custom Integrated Circuits Conference (2007) 769 (DOI: 10.1109/CICC.2007.4405843).

[25] D. Chen, et al.: “A wideband high efficiency V-band 65 nm CMOS power amplifier with neutralization and harmonic controlling,” IEICE Electron.Express 14 (2017) 20171110 (DOI: 10.1587/elex.14.20171110).

[26] N. Deferm, P. Reynaert: “Differential and common mode stability analysis of differential mm-wave CMOS amplifiers with capacitive neutralization,” Analog Integrated Circuits and Signal Processing 80.1 (2014) 1–12 (DOI: 10.1007/s10470-014-0295-2).

[27] Y. Chen, T. Tsai, J. Tsai and T. Huang: “Transformer-Based Predistortion Linearizer for High Linearity and High Modulation Efficiency in mm-Wave 5G CMOS Power Amplifiers,” IEEE Transactions on Microwave Theory and Techniques 67 (2019) 3074 (DOI: 10.1109/TMTT.2019.2914900).

[28] S. Shakib, H. Park, J. Dunworth, V. Aparin and K. Entesari: “A Highly Efficient and Linear Power Amplifier for 28-GHz 5G Phased Array Radios in 28-nm CMOS,” IEEE Journal of Solid-State Circuits 51 (2016) 3020 (DOI: 10.1109/JSSC.2016.2606584).

[29] K. Chiang, T. Tsai, I. Huang, J. Tsai and T. Huang: “A 27-GHz Transformer Based Power Amplifier with 513.8-mW/mm2 Output Power Density and 40.7% Peak PAE in 1V 28-nm CMOS,” IEEE MTT-S International Microwave Symposium (IMS) (2019) 1283 (DOI: 10.1109/MWSYM.2019.8700802).

[30] P. Indirayanti and P. Reynaert: ”A 32 GHz 20 dBm-PSAT transformer-based Doherty power amplifier for multi-Gb/s 5G applications in 28 nm bulk CMOS,” IEEE Radio Frequency Integrated Circuits Symposium (RFIC) (2017) 45 (DOI: 10.1109/RFIC.2017.7969013).