Impact of thinning the GaN buffer and interface layer on thermal and electrical performance in GaN-on-diamond electronic devices

Callum Middleton 1, Hareesh Chandrasekar 1, Manikant Singh 1, James W. Pomeroy 1, Michael J. Uren 1, Daniel Francis 2, and Martin Kubal 1

1 Centre for Device Thermography and Reliability, School of Physics, H H Wills Physics Laboratory, University of Bristol, Bristol BS8 1TL, United Kingdom
2 Element-Six Technologies, Santa Clara, CA 95054, United States of America
E-mail: CM1720@bristol.ac.uk

Received October 13, 2018; accepted November 25, 2018; published online January 31, 2019

We demonstrate that GaN-on-diamond technology with an ultra-thin GaN buffer and interface layer offers excellent thermal resistance alongside good electrical performance. Two device sets were investigated, one with 354 nm thick GaN buffer and 17 nm thick interface layers, the other with 700 nm thick GaN buffer and 36 nm thick interface layers. The samples demonstrate excellent thermal resistances of 9 ± 1 K/(W/mm) and 10.9 ± 0.5 K/(W/mm), respectively. Trade-offs between GaN buffer thickness and effective thermal boundary resistance are discussed demonstrating pathways for the advancement of GaN-on-diamond technology. IV measurements show low trapping and reduced thermal non-linearity in devices with ultra-thin GaN layers. © 2019 The Japan Society of Applied Physics

Gallium Nitride (GaN), by virtue of its wide bandgap, high breakdown field and high electron mobility is a key material for many electronic and optoelectronic devices. 1 While these properties allow GaN to sustain high voltages and fast switching speeds, they also result in a large power density in the device, creating the need for novel thermal management techniques. 2,3 Diamond, with the highest known bulk thermal conductivity, has been demonstrated to provide heat sinking superior to commonly used SiC substrates for GaN devices. 4,5 Thermal resistances as low as 10 K/(W/mm) have been demonstrated compared to 16 K/(W/mm) for GaN-on-SiC when comparing similar device architectures, as well as good RF performance and high mechanical stability of the interface. 6-8 This makes achievable 3 x greater areal power density when optimum gate pitches are chosen. 9

To fabricate GaN-on-diamond wafers, a GaN-on-Si wafer is used as starting material, after removal of the strain relief layers and original Si substrate, an interface layer, typically a dielectric such as silicon nitride, is deposited followed by the diamond growth. 8 The thermal resistances of the initial diamond seeding layer and the interface layer are critical for the optimization of the thermal resistance of GaN-on-diamond devices and are typically aggregated as an effective thermal boundary resistance (TBR eff). Whilst the interface layer’s large thermal resistance originates from its amorphous nature (its thermal conductivity is approximately 1 W m⁻¹ K⁻¹), phonon scattering at grain boundaries in the diamond seeding layer also reduce the phonon mean free path. Reducing the TBR eff is key for delivering the full capabilities of diamond as a heat spreader and improving heat extraction from devices. 9,10 TBR eff for GaN-on-diamond wafers shown in the literature are as low as 12 m²K GW⁻¹, and its value is approximately proportional to interface layer thickness. 8,9 Simulations have shown that the optimal GaN buffer thickness is dependent on the TBR eff at the GaN-diamond interface. 10 This work addresses the challenge of reducing device thermal resistance through reducing the GaN buffer thickness and the balance which needs to be struck with the TBR eff, DC and pulsed IV measurements shown here demonstrate that there is negligible device heating, and device performance is not strongly impacted by carrier trapping for ultra-thin GaN buffer layers. We also show for the first time that ultra-thin buffer layers reduce device temperature sensitivity.

The devices studied in this work originate from two four-inch GaN-on-diamond wafers, with the fabrication process described in Ref. 11. The first had a 700 nm thick GaN buffer and a 36 nm thick interface layer, and the other had a 354 nm thick GaN buffer with a 17 nm thick interface layer, both with an AlGaN barrier layer on top. Single-finger devices were studied, with standard ohmic and Schottky contacts, a SiN passivation, a W c of 50 μm, a L G of 1.5 μm, an L SG of 1 μm and a L GD of 7 μm. The gate contact is a gamma gate with a 1 μm overhang on the drain side.

Photoluminescence (PL) was used to determine the GaN channel surface temperature with a precision of approximately ±3 °C, at a distance 2 μm from the gate edge using a HeCd laser source (325 nm) with a laser spot size of less than 1 μm. A typical PL spectrum can be seen in Fig. 1. Bandgap emission energy varies following the modified Varshni equation

\[
E = E_0 - \frac{A T^2}{T + T_0} + \frac{1}{2} k_B T
\]

where \( E \) is the energy of the band-edge PL peak at a temperature \( T \), \( k_B \) is the Boltzmann constant and \( A \), \( E_0 \), and \( T_0 \) are empirical fitting parameters. 11,12 As the laser used is above bandgap, laser heating must be accounted for by measuring the PL energy at different laser powers and extrapolating to the case of zero laser power. 12,13 We note that whilst Raman thermography is typically used to measure channel temperature, 13 it was not possible in this instance due to the low signal from the thin GaN buffer and a high luminescence background from the diamond for the particular devices studied.

3D finite element simulations of the tested devices were performed using ANSYS. 14,15 To compare to the experimental data, Joule heating is applied over a 0.75 μm long area at the GaN top surface, adjacent to the gate edge on the drain side shown in Fig. 1. For the GaN a room temperature thermal conductivity of 160 W m⁻¹ K⁻¹ with a \( T^{-1.4} \) temperature dependence was used. For simplicity, the AlGaN barrier layer was not included in the thermal simulation. To account for the columnar growth structure of diamond, the diamond substrate was taken to consist of 5 separate layers whose...
thermal conductivities increase away from the interface as grain sizes increase. These layers start 1 μm thick and increase to 4, 10, 20 and finally 40 μm with thermal conductivities which are anisotropic and temperature dependent, taking data for the thermal conductivities from Refs. 7 and 15.

Devices on the 700 nm buffer sample and the 354 nm buffer sample were electrically tested under DC and pulsed IV conditions. Pulsed IV measurements were performed using a pulse width of 200 ns and a frequency of 1 kHz in unstressed (Vgs = 0 V, Vds = 0 V), gate stress (gate lag: Vgs = −6 V and Vds = 0 V), and gate and drain stress conditions (drain lag: Vgs = −6 V and Vds = 40 V).

Figure 2 shows the measured temperature determined from PL measurements, which corresponds to the temperature at the top of the GaN layer in the devices. The temperature change in the device at the measurement position for the 700 nm buffer layer device was 4.2 ± 0.2 K/(W/mm) compared to that of 2.61 ± 0.03 K/(W/mm) for the 354 nm buffer layer device. Finite element simulations were fitted to these experimental data, finding a TBR_{eff} of 20 m²K/GW for the 700 nm sample and 13 m²K/GW for the 354 nm sample, which is consistent with both the thinner interface layer in the latter sample and with values reported elsewhere. Both samples underwent identical growth procedures, meaning other factors such as differences in the diamond microstructure near the GaN-diamond interface caused by diamond growth conditions and the seeding method can be neglected.

Peak temperatures occur near the point of highest electric field in the devices which is at the gate edge on its drain side, although this part of the device is often obscured by a field plate as in the devices studied here. This is why, as demonstrated in Fig. 1, measurements were taken approximately 2 μm from the gate edge meaning peak temperatures and thermal resistances had to be determined from the measured temperatures using the finite element simulations, similar to approaches used elsewhere. For the 700 and 354 nm samples this gives thermal resistances of 10.0 ± 0.5 K/(W/mm) and 9 ± 1 K/(W/mm) respectively. Both these values are significantly improved with respect to the 16 K/(W/mm) reported in the literature for GaN-on-SiC, and are comparable to previously reported results for GaN-on-diamond of 10 K/(W/mm). Despite the difference in GaN buffer thickness and TBR_{eff} of the samples, both possess a similar thermal resistance. The difference in measured temperatures despite this similar thermal resistance implies the self-heating is more localized in the thinner sample. For a device with a higher TBR_{eff}, a thicker GaN layer is beneficial as this will allow lateral heat spreading prior to the heat reaching the interface layer, reducing heat flux density at the GaN-diamond interface. In this case the balance between heat spreading and TBR_{eff} reduction almost matches giving similar thermal resistance.

Results from finite element simulations depicted in Fig. 3 illustrate this for the two buffer layer thicknesses considered here. The lowest TBR_{eff} possible for a GaN-diamond interface is around 3 m²K/GW, found by the diffuse mismatch model. For TBR_{eff} values greater than 5–7 m²K/GW, the 700 nm GaN provides lower peak channel temperatures than...
for a thinner buffer layer, however for a lower $\text{TBR}_{\text{eff}}$ there is a benefit of using thinner buffer layers. This cross over point shifts to higher $\text{TBR}_{\text{eff}}$ with increased electrical power dissipation in the device due to increased heat flux at the interface.

Reducing the GaN buffer layer thickness therefore requires a reduction in $\text{TBR}_{\text{eff}}$ but provides an attractive pathway for improving GaN-on-diamond technology further beyond current state of the art, although the impact on the electrical performance must also be considered. Figure 4 illustrates a comparison between the DC and pulsed-$IV$ characteristics for representative devices on both samples. We see that there is limited reduction in $I_{\text{DSS}}$ between DC and pulsed-$IV$ measurements, indicating that the thermal droop associated with self-heating is small in both the samples. Interestingly, devices measured on the 700 nm GaN buffer sample exhibit a greater droop in $I_{\text{DSS}}$ at maximum drain voltage, 8% against 5%, for the thinner GaN buffer layer sample. This is consistent with the more localized self-heating in the latter sample, resulting in a smaller change in source and drain access resistances. Source resistance is the most temperature sensitive part of the device, so thinning the epitaxy provides a route to reduced thermally induced non-linearity.

Under gate lag stress, both samples show negligible change in ON resistance ($R_{\text{on}}$), with the 354 nm GaN buffer sample showing a small positive threshold voltage ($V_{\text{th}}$) shift of 180 mV with respect to the unstressed state, suggesting some minor electron trapping under the gate. The 700 nm sample showed no threshold shift, the absence of bulk trapping perhaps a consequence of the thicker buffer. Under drain lag stress the 354 nm GaN buffer sample shows negligible change in $R_{\text{on}}$ or further change in $V_{\text{th}}$, whereas the 700 nm sample shows a significant $R_{\text{on}}$ increase of 44%, and again a negligible $V_{\text{th}}$ shift. Given the small buffer trapping suggested by the gate lag measurements, the significant knee-walkout and increase in $R_{\text{on}}$ for the 700 nm sample is most likely to be associated with localized surface trapping of electrons in the vicinity of the gate edge.\(^\text{19}\) The reason for the drain lag difference between the two samples is unknown given that they had nominally identical processing. Encouragingly, the thinner GaN buffer layer device showed low knee-walkout and a manageable bulk trapping despite moving the GaN-diamond interface closer to the active channel region. These pulsed-$IV$ results are comparable to other reports for GaN-on-diamond devices,\(^\text{21}\) and suggest that there is little adverse impact on the device electrical properties when using thin GaN buffer and interface layers, illustrating great potential for further reduced thermal resistance GaN-on-diamond electronic devices.

The impact of reducing GaN buffer layer and interface layer thickness on the thermal characteristics of GaN-on-diamond devices was studied. The devices investigated demonstrate excellent thermal resistances, in particular for a device with a 354 nm thick GaN buffer layer which displayed a thermal resistance as low as 9 ± 1 K/(W/mm). This shows it is possible to create low thermal resistance stacks with ultra-thin GaN buffer layers which can potentially exceed the current state of the art, provided lower GaN-Diamond interface $\text{TBR}_{\text{eff}}$ material is also achieved. The comparison between DC and pulsed-$IV$ curves also showed that the thinner sample had less self-heating induced change in output conductance. This is a significant unreported benefit of an ultra-thin buffer, in that it localizes self-heating to the gate region and hence reduces the impact on the source resistance. This could give a major benefit in terms of reducing thermally generated device non-linearity. Future investigation into these devices could include analysis of how this more localized heating impacts the devices during RF operation.

**Acknowledgments**  We acknowledge financial support from the Engineering and Physical Science Research Council (EPSRC) through the programme grant GaN-DaME (EP/P00945X/1). CM’s PhD studentship is co-funded by the EPSRC Centre for Doctoral Training in Diamond Science and Technology (EP/L015315/1) and Element-Six Technologies. Data are available at the University of Bristol data repository, data.bris, at https://doi.org/10.5523/bris.10.5523/bris.id7obfjaiwa22/wlpj2j3tgm2aw.

1) B. J. Baliga, Semicond. Dev. Technol. 28, 074011 (2013).
2) M. Kuball and J. W. Pomeroy, IEEE Trans. Device Mater. Reliab. 16, 667 (2016).
3) G. Pavlidis, S. Pavlidis, E. R. Heller, E. A. Moore, R. Vetury, and S. Graham, IEEE Trans. Electron Devices 64, 78 (2017).
4) D. C. Dumka, T. M. Chou, J. L. Jimenez, D. M. Fanning, D. Francis, F. Faili, F. Ejeckam, M. Bernardoni, J. W. Pomeroy, and M. Kuball, Compound Semiconductor Integrated Circuit Symp. (CSICS) (IEEE, 2013, p. 1).
5) J. W. Pomeroy, M. Bernardoni, D. C. Dumka, D. M. Fanning, and M. Kuball, Appl. Phys. Lett. 104, 83513 (2014).
6) D. Liu, H. Sun, J. W. Pomeroy, D. Francis, F. Faili, J. D. Twitchen, and M. Kuball, Appl. Phys. Lett. 107, 251902 (2015).
7) J. Anaya, H. Sun, J. W. Pomeroy, and M. Kuball, IEEE ITherm, 2016, p. 1558.
8) H. Sun, R. B. Simon, J. W. Pomeroy, D. Francis, F. Faili, J. D. Twitchen, and M. Kuball, Appl. Phys. Lett. 106, 111906 (2015).
9) Y. Zhou et al., ACS Appl. Mater. Interfaces 9, 34416 (2017).
10) K. Park and C. Bayram, Appl. Phys. Lett. 109, 151904 (2016).
11) D. Francis, F. Faili, B. Babic, F. Ejeckam, A. Nurmikko, and H. Maris, Diam. Relat. Mater. 19, 329 (2010).
12) T. Batten, A. Manoi, M. J. Uren, T. Martin, and M. Kuball, J. Appl. Phys. 107, 074502 (2010).
13) N. Shigekawa, K. Onodera, and K. Shiojima, Jpn. J. Appl. Phys. 42, 2245 (2003).
14) ANSYS 18.1. Academic release (2017).
15) J. Anaya et al., Acta Mater. 103, 141 (2016).
16) D. Liu, D. Francis, F. Faili, C. Middleton, J. Anaya, J. W. Pomeroy, D. J. Twitchen, and M. Kuball, Scr. Mater. 128, 57 (2017).
17) M. Power, J. W. Pomeroy, Y. Otoki, T. Tanaka, J. Wada, M. Kuzuhara, W. Jantz, A. Souzis, and M. Kuball, Phys. Status Solidi A 212, 1 (2015).
18) Y. Won, J. Cho, D. Agonafer, M. Asheghi, and K. E. Goodson, IEEE Trans. Compon., Packag. Manuf. Technol. 5, 737 (2015).
19) C. Roff, J. Benedikt, P. J. Tasker, D. J. Wallis, K. D. Hilton, J. O. Maclean, G. D. Hayes, M. J. Uren, and T. Martin, IEEE Trans. Electron Devices 56, 13 (2009).