Non-Hysteretic Condition in Negative Capacitance Junctionless FETs

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Abstract—This paper analyzes the design space stability of negative capacitance double gate junctionless FETs (NCDG JLFET). Using analytical expressions derived from a charge-based model, we predict instability condition, hysteresis voltage, and critical thickness of the ferroelectric layers giving rise to the negative capacitance behavior. The impact of the technological parameters is investigated in order to ensure hysteresis-free operation. Finally, the stability of NCDG JLFET is predicted over a wide range of temperatures from 77 K to 400 K. This approach has been assessed with numerical TCAD simulations.

Index Terms—Charge-based model, double-gate junctionless FET, Negative capacitance, Instability, Hysteresis-free.

I. INTRODUCTION

Limitation to scaling is partly due to the source/drain (S/D) junctions in conventional metal-oxide-semiconductor field-effect transistors (MOSFET). Here is where junctionless field-effect transistors (JLFET) can help to overcome this technological challenge in the nanoscale FETs [1]. By essence, junctionless transistors (JLTs) are free from ultra-steep junctions implantations and thermal annealing for S/D dopant activation [1].

Nevertheless, the scaling of MOS devices still faces the issue of power consumption and off-state current ratio [2]. The reduction of the power supply voltage is always the best option to mitigate power dissipation, but at the expense of $I_{on}$ to $I_{off}$ current ratio degradation since the subthreshold swing (SS) of a FET is limited to the Maxwell-Boltzmann theoretical limit, i.e., 60 mV/dec at room temperature (RT).

Hence, the main parameter limiting the power supply voltage scaling in FETs is subthreshold swing (SS). It was proposed that replacing the conventional gate oxide with a stack made of an insulator and a ferroelectric material having a certain thickness could give rise to an effective negative capacitance (NC). Negative capacitance amplifies the impact of the gate voltage seen from the channel, resulting in a rapid variation of the current. [3]. This means that the SS could become lower than the Maxwell-Boltzmann theoretical limit [3][5].

However, ferroelectric material can be responsible for hysteresis which is inappropriate for logic applications [6]. An NC FET should operate in a non-hysteretic regime. This happens when the total energy of series capacitors (i.e. FE + MOS) satisfies stability conditions [3].

The behavior of a ferroelectric material was modelled by Ginzburg and Devonshire relying on the Landau theory of phase transitions [7].

In this context and following analytical models developed in [8][11], we propose to investigate in details the negative capacitance in Double-Gate junctionless FETs (DG JLFETs). In our previous work [11] we studied how the ferroelectric influences the current-voltage characteristics of a DG JLFET and predicted that, although NC in the junctionless FETs does not enhance the SS in the depletion region, swing in the moderate drain currents decreases and improves the overdrive voltage.

In this work, we will derive explicit relationships to predict the onset of instability, i.e, where the charge-voltage curve snaps back upon hysteresis, the critical thickness of the ferroelectric, and the hysteresis voltage.

II. MERGING DG JLFET WITH FERROELECTRIC

Using a ferroelectric in series with an insulating layer may, for a specific configuration, behave as a negative capacitance. If this happens, the body factor “m” becomes lower than unity, pushing the subthreshold swing (SS) below 60 mV/dec [4]. To model this behavior, the common approach is to consider the Gibb’s free energy $U$ of a ferroelectric with respect to the total polarization $P$ [11]. According to the Landau theory, the voltage drop across the ferroelectric $V_f$ is linked to the charge density of the ferroelectric $Q$ (per unit area) as follows

$$V_f = 2\alpha t_f Q + 4\beta t_f Q^3 + 6\gamma t_f Q^5.$$  (1)

where $\alpha$, $\beta$ and $\gamma$ are ferroelectric material constants. The properties of a ferroelectric are also be affected by the temperatur, which can be taken into account in the parameter $\alpha$, $\alpha = \alpha_0(T - T_c)$, where $T_c$ is the Curie temperature. In our paper, the Landau coefficients were extracted from the experimental data in [12]. Three-dimensional schematics of DG JLFET structure integrated with a ferroelectric layer are drawn in Fig. I. In order to provide the uniform electric field inside the ferroelectric layer, an embedded metallic layer is introduced between the insulator and the ferroelectric [5]. The potentials of the effective gate $V_{gate(eff)}$ and real gate $V_{gate}$ are related to the potential across the ferroelectric as follows

$$V_f = V_{gate} - V_{gate(eff)}.$$  (2)
Drain
Source
INsulator
Ferroelectric
Gate
Silicon channel
(a)
(b)
Fig. 1: (a) 3-D Schematic and (b) 2-D cross-section view of a symmetric double-gate JLFET with a ferroelectric layer in the gate stack.

A. DG JLFET core equations

An n-type long-channel symmetric double-gate JLFET with embedded ferroelectric is considered (see Fig. 1). In order to focus on the negative capacitance effect of the ferroelectric in a junctionless FET, we have ignored the short channel effects intentionally. The channel length, thickness, and width are \( L_g \), \( T_{sc} \) and \( W \) respectively. The channel doping density is \( N_D \). The gate oxide and ferroelectric thicknesses are \( t_{ox} \) and \( t_f \) respectively. Decreasing the gate voltage in an n-type JL FET makes its channel depleted from majority carriers and puts the device in OFF-state. On the other hand, increasing the gate voltage turns on the JL FET [13].

According to the charge-based model for symmetric DG JLFETs proposed in [8], [9], the effective gate potential \( V_{gate(\text{eff})} \) in depletion mode depends on the charge density in the semiconductor channel \( (Q_{sc} = Q_f + Q_m) \) as

\[
V_{gate(\text{eff})} = \Delta \phi_{ms} + V_{ch} - \frac{Q_{sc}}{2C_{ox}} + U_T \ln \left( \frac{N_D}{n_i} \right) + U_T \ln \left[ 1 - \left( \frac{Q_{sc}}{Q_f} \right)^2 \right] - \frac{Q_{sc}^2}{8C_{sc}Q_f},
\]

where \( n_i \) is the intrinsic carrier concentration, \( C_{ox} \) and \( C_{sc} = \epsilon_{si}/T_{sc} \) are the insulator and semiconductor capacitances, \( U_T = k_B T/q \) is the thermal voltage, \( V_{ch} \) is the quasi Fermi potential, \( \Delta \phi_{ms} \) is the metal - intrinsic semiconductor work function difference, \( Q_m \) is the total mobile charge and \( Q_f = qN_DT_{sc} \) is the fixed charge density in the channel . In accumulation mode, the effective gate voltage with respect to the charge density becomes (with \( \theta = 8\epsilon_{si}qN_DU_T \))

\[
V_{gate(\text{eff})} = \Delta \phi_{ms} + V_{ch} - \frac{Q_{sc}}{2C_{ox}} + U_T \ln \left( \frac{N_D}{n_i} \right) + U_T \ln \left( 1 + \frac{Q_{sc}^2}{\theta} \right). \tag{4}
\]

Using the drift-diffusion transport model, the drain current in the channel is given by

\[
I_{ds} = \mu W \left( -Q_m \frac{d\psi_s}{dx} + U_T \frac{dQ_m}{dx} \right) = -\mu W Q_m \frac{dV_{ch}}{dx}. \tag{5}
\]

where \( \mu \) is the free carrier mobility that we assume constant in this work. In depletion mode, \( dV_{ch} \) is obtained from (3) whereas in accumulation relation (4) is used instead. The drain current expressions are obtained from [8], [9].

B. DG JLFET with NC

To calculate the potential across the ferroelectric from relation (1), we need the total charge density in the channel. Explicit expressions of the total charge density in the ferroelectric for the JLFET operating either in depletion, accumulation, or hybrid modes obtain from ref [11].

The characteristics of the NCDG JLFET was analyzed and the analytical approach compared with TCAD. The 2-D electrostatics and transfer characteristics of the regular DG JLFET are simulated using TCAD SIVACO. On the other hand, the NCDG JLFET is simulated by a self-consistent solution of the charge-voltage characteristics of the ferroelectric obtained from Landau equation and the baseline DG JLFET obtained from TCAD. [11].

We consider a 1 \( \mu \)m channel length (to neglect short channel effects) and 1 nm oxide thickness. The channel thickness is 10 nm. The doping concentration is \( N_D = 10^{19} \text{cm}^{-3} \). Given that the relation between \( V_{gate(\text{eff})} \) and the ferroelectric total charge density \( Q \) is known, the next step is to introduce \( Q \) in (1) and use equation (2) to get the external gate voltage \( V_{gate} \) applied to the device.

Fig. 2 (a) displays the mobile charge density versus \( V_{gate} \) at low \( V_{DS} \) while varying \( t_f \). Fig. 2 (a) reveals that the slope increases when the ferroelectric thickness is increased, but above a critical value of \( t_f \), that we call the critical thickness \( t_{cr} \), the \( Q_m - V_{gate} \) curves snap back: the ferroelectric layer starts to exhibit hysteresis. This region is where the device becomes unstable.

III. CRITERIA FOR INSTABILITY IN LINEAR OPERATION

As mentioned in the previous section, increasing the thickness of ferroelectric increases the slope of the mobile charge density versus gate voltage dependence, see Fig. 2 (a). The onset of snapback happens when the first derivative of the charge density versus the gate voltage becomes infinite. We call it the instability point. According to Fig. 2 (a), this condition will happen twice, see points 1 and 2 in Fig. 2 (c) which is an illustration of \( Q_m - V_{gate} \). In this case, it means that the ferroelectric will experience some hysteresis, a feature that should be avoided for a correct operation of the NC JLFET. Non-hysteresis will appear when both locus merge...
into a single point, i.e. point 3. This figure resumess the three important points where the curve snaps back.

In addition, to see voltage amplification due to the negative capacitance, $V_f$ should be negative in relation (2). To find this condition, we first calculate the roots of relation (1) which are given by $Q = 0, Q = -\sqrt{\alpha/2\beta}$, and $Q = \sqrt{\alpha/2\beta}$. It is straightforward to draw the sign table of $V_f$ with respect to the roots, see Fig. [2] (b)). Based on this analysis, we can already draw some important conclusion: a negative value for $V_f$ can be obtained from Eq (1) when the total charge density in the ferroelectric material ($Q$) is either positive, or negative provided it is lower than $-\sqrt{\alpha/2\beta}$. Since this charge density is opposed to the charge in the silicon channel, $Q=Q_{sc}/2$, it means that negative capacitance can always take place in accumulation mode, but not necessarily in depletion mode i.e. that NC in depletion cannot be since you need technological values ($T_{sc}$=200 nm, $N_D=10^{19}$ cm$^{-3}$ or $T_{sc}$=10 nm, $N_D=2 \times 10^{20}$ cm$^{-3}$), but then the JL cannot be switched off [14]. This result was not expected and is a peculiarity of junctionless FET. This means that in a junctionless FET, the NC effect in the subthreshold region, precisely before the flat band condition, can only make a shift in the I-V characteristics. However, in the accumulation region, or we can say above the threshold, the swing can decrease to below the 60 mV/dec.

A. Instability Points

Given that we have two instability points, we have the following scenarios. The first is when 'instability 1' happens in depletion and 'instability 2' occurs in accumulation. The second is when both 'instability 1 and 2' arise in accumulation. The case where both instability points happen in depletion must be rejected. Hence, we conclude that an instability point 2 cannot happen in depletion.

1) Depletion Mode: Calculating the instability point in depletion mode needs to get the derivative of $V_{gate}$ respect to $Q_{sc}$ from equation (5). Introducing (1) and (2) in (3) and neglecting the coefficient gamma of $V_f$ in (1) gives

$$V_{gate} - (2\alpha f Q + 4\beta f Q^3) = \Delta \phi_{ms} + V_{ch} - \frac{Q_{sc}}{2C_{ox}}$$

$$+ U_T \ln \left( \frac{N_D}{mi} \right) + U_T \ln \left[ 1 - \left( \frac{Q_{sc}}{Q_f} \right)^2 \right] - \frac{Q_{sc}^2}{8C_{sc}Q_f},$$

where we can assume $Q \approx -Q_{sc}/2$ in lineal operation. To find the instability points we must find the roots of $dV_{gate}/dQ_{sc}$. This is given by a four degrees polynomial equation, $a_4 Q_{sc}^4 + a_3 Q_{sc}^3 + a_2 Q_{sc}^2 + a_1 Q_{sc} + a_0 = 0$, where $a_4 = -3\beta f/2$, $a_3 = -1/(4C_{sc}Q_f)$, $a_2 = 3\beta f Q_f^2/2 - \alpha f - 1/(2C_{ox})$, $a_1 = 2U_T + Q_f/(4C_{sc})$ and $a_0 = \alpha f Q_f^2 + Q_f^2/(2C_{ox})$. The only acceptable roots in depletion are given by (see Appendix I)

$$Q_{scD}(ins1) = -a_3 \frac{a_4}{a_4} + s - \frac{1}{2} \sqrt{-4s^2 - 2m - t},$$

where $m, l, s$ are defined in Appendix I. In addition, since the total charge density in depletion must be positive, neglecting $a_4, a_3$ and $a_2$ we end with a good approximation of the total charge density of the channel at the instability point.

2) Accumulation Mode: If instability happens in accumulation, we rely on the derivative of $V_{gate}$ versus $Q_{sc}$ based on (4). Substituting (1) and (2) in (4), still assuming that gamma is negligible and that in linear operation of mode $Q \approx -Q_{sc}/2$, we can write

$$V_{gate} = -\alpha f Q_{sc} - \beta f Q_{sc}^3/2 + \Delta \phi_{ms} + V_{ch} - \frac{Q_{sc}}{2C_{ox}}$$

$$+ U_T \ln \left( \frac{N_D}{mi} \right) + U_T \ln \left[ 1 + \frac{Q_{sc}^2}{Q_f} \right].$$

The instability point in the accumulation must satisfy $dV_{gate}/dQ_{sc} = 0$, leading to

$$b_4 Q_{sc}^4 + b_2 Q_{sc}^2 + b_1 Q_{sc} + b_0 = 0,$$

where $b_4 = -3\beta f/2, b_2 = -(1/(2C_{ox}) + \alpha f + 3\beta f/2), b_1 = 2U_T, \text{ and } b_0 = -\theta/(1/(2C_{ox}) + \alpha f)$. Solving this equation can be done by following the same analysis as for
the depletion mode (see Appendix I). The values predicting instability in accumulation mode are

$$Q_{scA(ins1)}^{scA(ins2)} = -\frac{b_3}{4b_4} \pm s - \frac{1}{2} \sqrt{-4s^2 - 2m \pm \frac{l}{s}}, \quad (10)$$

We introduce some approximation which gives the two values for the instability points in accumulation. When instability 1 happens in accumulation, neglecting $b_4$ gives the total charge density in the channel

$$Q_{scA(ins1)} \approx -b_1 - \sqrt{b_2^2 - 4b_0 b_2}. \quad (11)$$

Even neglecting $b_0$, the approximation is quite accurate.

When instability point 1 takes place in accumulation, it implicitly requires that the square root in (11) must be positive, imposing a key condition on the ferroelectric thickness, $t_f < (-c_1 + \sqrt{c_1^2 - 4c_2c_0})/2c_2$, where $c_2 = 3\theta/(4C_{ox}) + \alpha\theta/C_{ox}$. $c_0 = \theta/(4C_{ox}) - U_0^2$.

As mentioned, the instability point 2 always happens in accumulation where the total charge density in the channel is negative and hence can be approximated by neglecting $b_1$ and $b_0$.

The instability charge of points 1 and 2 versus the thickness of the ferroelectric film for different values of oxide thickness and channel doping has been plotted in Fig. 3(a), (b) respectively. As can be seen, decreasing the ferroelectric thickness causes instability points 1 and 2 to merge at point 3, and then the device operates in a non-hysteresis regime. On the other hand, increasing the oxide thickness and decreasing the channel doping lead to the non-hysteresis regime in a thicker ferroelectric film.

B. Hysteresis Voltage

When the ferroelectric thickness is increased, the difference in terms of voltage between the instability points 1 and 2 increases. We call this difference the hysteresis voltage ($V_H$) (see Fig. 2(b)). This hysteresis voltage ($V_H$) calculated for the NCDG JLFET is now calculated.

When both instability points happen in accumulation, $V_H$ becomes the difference of $V_{gate}$ in two instability points $Q_{scA(ins1)}$ and $Q_{scA(ins2)}$: 

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Fig. 3: The instability charge for (a) different oxide thickness and (b) different doping versus ferroelectric thickness. Hysteresis voltage for (c) different oxide thickness and (d) different doping versus ferroelectric thickness.
C. Critical Thickness

The critical thickness of the ferroelectric $t_{cr}$ is defined as the upper limit of the ferroelectric thickness where the device operates in the non-hysteresis regime. The $t_{cr}$ corresponds to locus 3 in Fig. 2(b) where instability points 1 and 2 are equal. Since instability point 2 will happen in accumulation, $t_{cr}$ must be obtained from (10), and should be real numbers. Therefore, if it goes to the non-hysteresis regime, (9) does not have real roots. According to the Appendix I, introducing the coefficients of (9) in (A.2), $t_{cr}$ is obtained from the cubic equation $d_3t_{cr}^3 + d_2t_{cr}^2 + d_1t_{cr} + d_0 = 0$ where $d_3 = (\alpha + 3\beta \theta)^2 - 27\alpha^2\beta\theta(\alpha + 3\beta \theta/2), d_2 = 3\alpha^2/(2C_{ox}) - 45\beta^2(\alpha + 3\beta \theta/4)/(2C_{ox}), d_1 = 3\alpha/(4C_{ox}^2) - 45\beta^2/(4C_{ox}^2) + 81\alpha U_f^2/2$ and $d_0 = 1/(2C_{ox})^3$.

The real root of the cubic equation gives the critical thickness of the ferroelectric in an NCDG JLFET which is obtained from Cardano’s formula

$$t_{cr} = \sqrt[3]{\frac{-A}{2} + \sqrt{\frac{A^2}{4} + \frac{B^3}{27}}} + \sqrt[3]{\frac{-A}{2} - \sqrt{\frac{A^2}{4} + \frac{B^3}{27}}} - C,$$

where $A = d_1/d_3 - d_2^2/(3d_3^2), B = 2d_2^3/(3d_3^3) - d_1d_2/(3d_3) + d_0/d_3, C = d_2, f_2, h_3$. In conclusion, as long as $t_f < t_{cr}$, the device works in the non-hysteresis regime.

D. Temperature Effect

The instability charge of points 1 and 2 versus the thickness of the ferroelectric film for different values of the temperature ranging from 77 to 400 K (note that the semiconductor is not degenerate at 77 K and Boltzmann statistics are still valid has been plotted in Fig. 4(a). It shows that increasing the temperature moves the non-hysteresis regime in a thicker ferroelectric film. The green lines in Fig. 4(a) represent $Q_{ins1,2}$ when FE is not a function of temperature which demonstrates that the semiconductor makes little changes with temperature, and most of the temperature dependence is expected to arise from the ferroelectric layer.

Hysteresis voltage versus the thickness of ferroelectric film for different values of the temperature has been plotted in Fig. 4(b). This figure show that the hysteresis voltage increases when temperature decreases. Fig. 4 shows $t_{cr}$ versus oxide thickness for different channel doping and different temperature. The results show that $t_{cr}$ has a linear dependency on $t_{ox}$ and is less sensitive to doping variations for lower temperatures.

IV. CONCLUSION

An analytical charge-based model for symmetric double-gate junctionless FETs with NC was developed. The model investigates the stability of an NCDG JLFET by proposing analytical expressions for the total charge density in the instability points. We proposed an explicit relationship for the critical thickness of the ferroelectric film, the thickness that determines hysteresis or non-hysteresis operation. The amount of hysteresis voltage, which is a measure of the hysteresis, has been given an analytical expression that depends explicitly on the device parameters. We also included the impact of the temperature on the JLFET with ferroelectric material from

![Fig. 4: (a) The instability charge and (b) Hysteresis voltage for the range of temperatures from 77 to 400 K versus ferroelectric thickness.](image)
Critical thickness $\phi$ and $s$ when the square root in $x$ becomes positive, $\Delta_1/2\sqrt{\Delta_0^3} \leq 1$. The lower limit gives the critical thickness of the ferroelectric, $\Delta_1 + 2\sqrt{\Delta_0^3} = 0$. This can be numerically solved. However, to simplify this, we assumethat $\Delta_0 \approx c^2$ and $\Delta_1 \approx 2c^3 + 27b^2e - 72ace$ leading to a polynomial equation

$$4c^3 + 27b^2e - 72ace = 0.$$  

**REFERENCES**

[1] C.-W. Lee, A. Aftzalian, N. D. Akhavan, R. Yan, I. Ferain, and J.-P. Colinge, “Junctionless multigate field-effect transistor,” *Applied Physics Letters*, vol. 94, no. 5, p. 053511, 2009.

[2] S. Takagi, T. Issawa, T. Tezuka, T. Numata, S. Nakahara, N. Hirashita, Y. Moriyama, K. Usuda, E. Toyoda, S. Dissanayake et al., “Carrier-transport-enhanced channel cmos for improved power consumption and performance,” *IEEE Transactions on Electron Devices*, vol. 55, no. 1, pp. 21–39, 2007.

[3] S. Salahuddin and S. Datta, “Use of negative capacitance to provide voltage amplification for low power nanoscale devices,” *Nano letters*, vol. 8, no. 2, pp. 405–410, 2008.

[4] G. A. Salvatore, D. Bouvet, and A. M. Ionescu, “Demonstration of subthreshold swing smaller than 60mv/decade in fe-fet with p (vdf-trfe)/sio 2 gate stack,” in *2008 IEEE International electron devices meeting*. IEEE, 2008, pp. 1–4.

[5] A. Rusu, G. A. Salvatore, D. Jiménez, and A. M. Ionescu, “Metal-ferroelectric-meta-oxide-semiconductor field effect transistor with sub-60mv/decade subthreshold swing and internal voltage amplification;” in *2010 International Electronic Devices Meeting*. IEEE, 2010, pp. 16–3.

[6] J. Jo and C. Shin, “Negative capacitance field effect transistor with hysterisis-free sub-60mv/decade switching;” *IEEE Electron Device Letters*, vol. 37, no. 3, pp. 245–248, 2016.

[7] L. D. Landau, “On the theory of phase transitions,” *Ukr. J. Phys.*, vol. 11, pp. 19–32, 1937.

[8] J.-M. Sallese, N. Chevillon, C. Lallement, B. Iniguez, and F. Prégaldiny, “Charge-based modeling of junctionless double-gate field-effect transitors,” *IEEE Transactions on Electron Devices*, vol. 58, no. 8, pp. 2628–2637, 2011.

[9] F. Jazaeri and J.-M. Sallese, *Modeling Nanowire and Double-Gate Junctionless Field-Effect Transistors*. Cambridge University Press, 2018.

[10] A. Rassekh, F. Jazaeri, M. Fathipour, and J.-M. Sallese, “Modeling interface charge traps in junctionless fets, including temperature effects,” *IEEE Transactions on Electron Devices*, vol. 66, no. 11, pp. 4653–4659, 2019.

[11] A. Rassekh, J.-M. Sallese, F. Jazaeri, M. Fathipour, and A. M. Ionescu, “Negative capacitance double-gate junctionless fets: A charge-based modeling investigation of swing, overdrive and short channel effect,” *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 939–947, 2020.

[12] M. Hoffmann, F. P. Fengler, M. Herzig, T. Mittmann, B. Max, U. Schroeder, R. Negrea, P. Lucian, S. Slesazeck, and T. Mikolajick, “Unveiling the double-well energy landscape in a ferroelectric layer;” *Nature*, vol. 565, no. 7740, p. 464, 2019.

[13] A. Rassekh and M. Fathipour, “A single-gate soi nanosheet junctionless transistor at 10-nm gate length: design guidelines and comparison with the conventional soi finfet;” *Journal of Computational Electronics*, pp. 1–9, 2020.

[14] F. Jazaeri, L. Barbout, and J.-M. Sallese, “Modeling and design space of junctionless symmetric dg mosfets with long channel;” *IEEE transactions on electron devices*, vol. 60, no. 7, pp. 2120–2127, 2013.