Abstract

We report on the design and performance of a mixed-signal application specific integrated circuit (ASIC) dedicated to avalanche photodiodes (APDs) in order to detect hard X-ray emissions in a wide energy band onboard the International Space Station. To realize wide-band detection from 20 keV to 1 MeV, we use Ce:GAGG scintillators, each coupled to an APD, with low-noise front-end electronics capable of achieving a minimum energy detection threshold of 20 keV.

The developed ASIC has the ability to read out 32-channel APD signals using 0.35 μm CMOS technology, and an analog amplifier at the input stage is designed to suppress the capacitive noise primarily arising from the large detector capacitance of the APDs. The ASIC achieves a performance of 2099 e− + 1.5 e−/pF at root mean square (RMS) with a wide 300 fC dynamic range. Coupling a reverse-type APD with a Ce:GAGG scintillator, we obtain an energy resolution of 6.7% (FWHM) at 662 keV and a minimum detectable energy of 20 keV at room temperature (20 °C). Furthermore, we examine the radiation

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tolerance for space applications by using a 90 MeV proton beam, confirming that the ASIC is free of single-event effects and can operate properly without serious degradation in analog and digital processing.

Keywords: ASIC, low-noise, X-rays, APD, radiation tolerance
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1. Introduction

Monitoring hard X-ray emissions from high-energy astronomical objects such as gamma-ray bursts (GRBs), supernovae, active galactic nuclei, black holes, and neutron star binaries plays an important role in their identification. In particular, observations in a wide energy band including hard X-rays are very crucial to identifying GRBs, because GRB emission ranges between a few keV to a few MeV [1]. In addition, GRBs are one of the most reliable counterparts for detectable gravitational wave (GW) sources such as GW150914 [2]. The detection of electromagnetic emission from GW sources would be critical for clarifying their origin by connecting them with known astronomical objects.

WF-MAXI [3] is a proposed mission on the International Space Station (ISS) to detect and localize X-ray transients, and is specifically designed to search the sky with a wide field of view (FoV). WF-MAXI has two scientific instruments: the Soft X-ray Large Solid Angle Camera, which is sensitive to the 0.7–10 keV band, and the Hard X-ray Monitor (HXM), which is sensitive to the 20 keV–1 MeV band. Both instruments have a very wide FoV of ∼25% of the entire sky. In particular, HXM is responsible for monitoring parts of the sky that other observatories do not cover in the hard X-ray band. HXM consists of a one-dimensional array of crystal scintillators (Ce-doped Gd₃Al₂Ga₃O₁₂; Ce:GAGG) coupled with avalanche photodiodes (APDs). By adopting an array structure combined with a coded mask or a passive shield around the scintillator array, HXM can localize X-ray transient sources to an accuracy of within a few degrees in one direction. If we use more than two sets of HXM with different angles, we can determine the two-dimensional source position. To realize this function, signals from each scintillator should be independently read out. As a consequence, analog front-end electronics are required for the HXM.

A primary objective of developing our application specific integrated circuit (ASIC) is to perform analog and digital signal processing on multiple APD signals, in order to measure energy spectra in a wide energy band between 20 keV–1 MeV. Thus, a wide dynamic range is needed for the ASIC, and the analog amplifier of the ASIC must have sufficiently low noise to detect low-energy X-ray photons at an energy of 20 keV. In addition, devices using a Complementary Metal Oxide Semiconductor (CMOS) in space applications, as in an in-orbit situation, radiation damage leads to serious issues, such as total dose effects and single event effects (SEEs). To ensure the in-orbit performance of our ASIC, the radiation tolerance should be evaluated.

Furthermore, to achieve a large detector effective area (∼100 cm²) using a 32-channel readout, each scintillator size should be ∼1×1×5 cm³ with large
APDs such as the S8664-55 (Hamamatsu: 0.5×0.5 cm$^2$ APD area and 1.0×1.0 cm$^2$ package area). In such a case, detector capacitance becomes ∼100 pF, where typically Si and CdTe detector capacitances are low and range from a few pF to 10 pF. Thus, to achieve our requirement, the series noise due to the large APD capacitance must be reduced when developing analog amplifiers in our ASIC.

In this paper, we report on a developed ASIC dedicated to APDs. Detailed specifications and the electrical design of the ASIC are described in Section 2 and the evaluated performance is shown in Section 3. Briefly, our ASIC achieves a performance comparable to the high-performance IDEAS ASIC (VA140) with low noise (1400 $e^-$ at a 100-pF load) and a wide dynamic range (200 fC) [4]. This creates a reasonable benchmark for ASICs with large detector capacitance for similar applications. The results of the ASICs’ tolerance to proton irradiation are presented in Section 4, and Section 5 concludes the paper.

2. Design of TT02APD32

2.1. Overview of TT02APD32

The TT02APD32 ASIC (henceforth TT02) is designed to read out 32 APD signal channels. Its main function is to condition the signal with a good signal-to-noise ratio and feed them into a Wilkinson-type analog-to-digital converter (ADC). The TT02 is fabricated based on the XFAB 0.35 µm CMOS technology with 4-metal and MIM (Metal-Insulator-Metal) options, and assembled in a ceramic package of 160 pins (QC-160360-WZ, KYOCERA). The electrical architecture of the TT02 utilizes a property of the Open IP project, which has amassed technologies and the development of several radiation detectors (e.g., [5]). In particular, since the large APD capacitance of ∼100 pF leads to a corresponding large capacitive noise, the TT02 implements an ingenious noise reduction scheme (see Section 2.5).

SEEs occur stochastically, and one of the most serious SEEs is the single event latch-up (SEL). In a CMOS structure, parasitic thyristors are formed due to the use of pMOS and nMOS transistors in a single silicon substrate. If a high-energy particle impacts the parasitic thyristor, the resulting large energy deposition generates many electrons and holes. Once the generated charge exceeds a critical limit in a certain region of the substrate, the thyristors activate, inducing an extremely large current into relevant circuits. Since its inherent positive feedback behavior (i.e., the large current lowers the threshold of the thyristor) causes thermal heating, it is never expected to automatically terminate until the power supply shuts down. Thus, the occurrence of SEL may result in the serious and permanent functional failure of ASICs, and can ultimately prevent a successful scientific mission. To improve the robustness of the TT02 against SEL, an epitaxial fabrication with p-type doping is used [6].

Figure 1 shows a photograph of the developed TT02 with a dimension of 4.8 × 8.4 mm$^2$. The specifications of the TT02 are shown in Table 1 and a schematic diagram of the TT02 is illustrated in Figure 2.
2.2. Analog processing

At an analog input, a charge sensitive amplifier (CSA) converts the input charge from the sensors or test pulse via \( C_{in} \) into a voltage through the feedback capacitance \( C_f \). The CSA output is directed into two paths: one, to a fast shaper with a peaking time of 0.5 µs, and the other to a slow shaper with a peaking time of 3 µs. Each signal channel is equipped with a pole-zero cancellation (PZC) circuit, which eliminates the long tail of the preamplifier output. The parameters for the PZC circuit are chosen to be

\[
R_f C_f = R_{pz} C_{pz} = R'_{pz} C'_{pz}.
\]

(1)

\( R_f, R_{pz}, \) and \( R'_{pz} \) employ transfer-gate-type transistors with the application of an adjustable gate voltage \( V_{GG} \). Thus, \( R_f \) could be modified from a few 100 MΩ to \( \sim \) GΩ by changing \( V_{GG} \). \( R_{pz} \) and \( R'_{pz} \) are configured as a parallel combination of replicated \( R_f \) so as to maintain the appropriate PZC requirement.

Since the PZC circuit does not include a time constant, the shaping amplifier is configured as a second-order low-pass filter, and the entire transfer function, including the PZC circuit, is equivalent to an ordinary CR–RC filter. The peaking time of the slow shaper is determined by a set of \( R_1, R_2, C_1, \) and \( C_2 \). To obtain critical damping in order to reduce undershooting of the output signal, the peaking time \( \tau_{peak,slow} = C_1 R_1 = 4 C_2 R_2 \) must be satisfied for the slow shaper. Similarly for the fast shaper, we impose \( \tau_{peak,fast} = C'_1 R'_1 = 4 C'_2 R'_2 \) on the peaking time. At the output stage of the slow shaper, the pulse height is acquired on a capacitor \( C_H \) at the timing of the HOLD signal, called the sample and hold (S/H).

Here, we adopt a current-mirror resistor circuit \( (R_1, R_2, R'_1 \) and \( R'_2) \) to obtain a specified large resistance as illustrated in Figure 3. The voltage difference between the IN/OUT nodes is converted into a current by the poly resistor sandwiched by two nMOS transistors. The circuit is configured to attenuate the current with the two stages of an asymmetric current mirror. As a result, the output current is substantially reduced to attain an effective resistance of a few MΩ. Another benefit of this resistor circuit is its high-Z input impedance. As a consequence, the amplifier located just before the resistor circuit does not feed any current. In addition, by feeding an adjustable constant current into the resistor, a coarse pedestal adjustment can be done.

Using a TSpice numerical simulation, we find that the stray capacitance around the current-mirror resistors distorts the waveform shape. To mitigate the pulse undershoot for the slow and fast shapers, the best choice for \( C_2 \) and \( C'_2 \) is found to be a very low capacitance (a few fF) where we utilize nMOS transistors because their gate capacitance is very low, although this apparently violates the critical damping condition.

2.3. Analog to digital conversion

The output signal from the fast shaper goes into two comparators. One is used for the trigger signal, and to conduct the S/H at the slow shaper after the elapse of the \( T_{HOLD} \) period. The other comparator detects very large signals
coming from the APD, which is employed to quickly restore the baseline of the shaper output, and to subsequently mitigate the dead time. The discharge is conducted by the “Release” signal, which shorts the capacitor $C_1$ or $C'_1$. We utilize a Wilkinson-type ADC that converts the pulse height to the digital channel value by counting the number of clocks for the ADC (ADCK) from the input of the START signal until the input of the STOP signal (i.e., during the $T_{ADC}$ period), where the STOP signal is generated when the RAMP signal exceeds the HOLD signal. The schematic view of the analog and digital processing for the ADC function is illustrated in Figure 4. The countable range for the ADC is 10 bits that are stored in digital registers.

2.4. Readout mode

For each event, the measured ADC values are output by two readout modes: FORCED and SPARSE. While in the FORCED mode, all ADC values for all 32 channels are output, and in the SPARSE mode several ADC values are output only for selected channels that have a larger ADC value than a certain threshold. Here, the SPARSE mode can be either analog or digital types, with the threshold levels determined by the analog voltage or the digital ADC value, respectively. Furthermore, the TT02 detects a common-mode noise as described in detail in Section 3.3. The ADC value of the measured common-mode noise can be read out for either mode.

By using the SPARSE mode, the amount of data is substantially reduced compared with the FORCED mode. Thus, adoption of the SPARSE mode is important for space applications because in many in-orbit situations the amount of onboard memory is highly limited.
Figure 2: Schematic diagram of the signal processing for the TT02APD32.

Figure 3: Current-mirror resistor employed as $R'_1$ and $R'_2$. A similar design is used for $R_1$ and $R_2$. By utilizing the asymmetric mirror ratio in a current-mirror pair and combining multiple pairs, a large resistor can be obtained. By feeding a constant current from PED+ to PED−, we can adjust the pedestal of the output signal. $V_L$ is a constant voltage source.
Table 1: Specification of the TT02APD32 (TT02)

| Specification                              | Value                          |
|-------------------------------------------|-------------------------------|
| Number of channels                        | 32                            |
| Dynamic range                             | 0 – 300 fC                    |
| Peaking time                               |                               |
| Fast shaper                               | 0.5 µs                        |
| Slow shaper                               | 3 µs                          |
| Integral non-linearity                    | 2.5%                          |
| Noise (RMS) at 100-pF load                | $2211 \pm 102 \ e^-$          |
| Detectability of common-mode noise        | >1 ADC channel                |
| Power supply                              | ±1.65 V                       |
| Power consumption                         | ∼100 mW                       |
| SEU cross-section (90% upper limit)        | <2.2 × $10^{-14}$ cm² bit⁻¹   |
| Radiation tolerance                       | >10.1 krad (101 Gy)           |

2.5. Input transistor of CSA

The designed CSA is illustrated in Figure 5 where a folded-cascode amplifier is adopted to obtain a high gain and large output swing. Since the APD’s capacitance is large ($C_D \sim 100$ pF), the capacitive noise is crucial for attaining a minimum detectable energy. To reduce the capacitive noise, the design of the input transistor of the CSA is key, and in the TT02, the noise power of the CSA is determined by the input transistor. The main contribution to capacitive noise power is a sum of the Johnson and flicker noise, which are proportional to $C_D^2/g_m \tau_{\text{peak}}$ and $C_D^2/A$, respectively, where $g_m$ is the transconductance of the input transistor and $A$ is the gate area of the input transistor ($A = WL$). $g_m$ is a function of the drain current $I_D$, the gate length $L$ and the gate width $W$.

While in the strong inversion approximation $g_m$ is proportional to $\sqrt{I_D W/L}$, the actual operation point is near the weak inversion. From the relation above, in order to reduce the capacitive noise power, larger $I_D$, larger $W$, and moderate $L$ for larger $A$ are required. In addition, a pMOS transistor is well-known to have a smaller noise than that of a nMOS transistor and we use a pMOS transistor as an input transistor. Since a single transistor cannot have large gate area $A$ and $I_D$, we use a number of pMOS transistors as an aggregated input transistor. Via numerical simulation using TSpice, we determined that $W = 8 \ \mu m$ and $L = 0.8 \ \mu m$ for the input transistor, and that in total 720 input transistors were required. The total $I_D$, gate capacitance and $g_m$ were estimated to be $793 \ \mu A$, $18 \ \text{pF}$, and $8.2 \ \text{mS}$, respectively.

2.6. Dual Interlock Cell

We adopt a master-slave flip-flop scheme to prevent malfunction due to distorted or noisy clock signals and stabilize the flip-flop’s output. Furthermore, a countermeasure is needed for a single event upset (SEU), which affects the correct behavior of flip-flops. If a high-energy particle impacts the CMOS circuits,
Figure 4: Schematic view of the analog and digital processing for measuring the pulse height. Details are mentioned in the text.

Figure 5: Analog electrical circuit of the CSA dedicated to APDs. A folded-cascode amplifier is adopted, where the gate length, gate width, and number of transistors are denoted as $L$, $W$, and $M$. $V_{H}$ and $V_{L}$ are constant voltage sources. The APD’s charge goes into $A_{IN}$ and the amplified voltage signal is output from $A_{OUT}$. 
the generated charge in the circuit accidentally activates the transistors, causing a bit inversion termed an SEU. Thus, an SEU event can significantly affect the ASIC operation when configured by control registers. To prevent SEUs from occurring, Dual Interlock Cell (DICE) circuits are implemented in the digital circuit of the TT02, as illustrated in Figure 6. By configuring a redundant dual structure, the original bit information is held even if one of the transistors in the DICE is accidentally activated. A similar DICE design has been widely used to protect ASICs from SEUs [7].

In addition, the TT02 can detect SEU events even if an SEU occurs in the TT02’s digital registers. The digital registers holding the configuration settings for the TT02’s signal processing are copied to separate registers, which are also DICE flip-flops as illustrated in Figure 7. The differences between the content on the shift register and the copy are detected by XOR gates, to be summed up in a wired-OR scheme. In addition to the prompt output of the SEU alert signal, the SEU bit is stored into the readback data of the configuration register or the ADC data.

2.7. Improvement from TT01

The TT02 is a revision of a previous ASIC, TT01APD32 (henceforth TT01, [8]). The TT01 has several problems and their related remedies in the TT02 are as follows:

- Tuning of the circuit parameters located around fast and slow shapers to suppress the degradation of the fast and slow waveforms (e.g., undershoot), as described in Section 2.2.

- Reduction of stray capacitances by analyzing the layout parasitic extraction and redesigning the schematic layout, alleviating distortion of the
Figure 7: Shift register implemented in the TT02 and capable of detecting an SEU event. Digital bit data are duplicated on a copy register. If an SEU event occurs and the original bit is inverted in a certain DICE, an XOR element activates a transistor with a wired-OR connection.

- Adding a new current source to independently adjust the constant voltages such as $V_L$ in the current-mirror resistor and 4-bit DAC (digital to analog converter) for coarse pedestal adjustment. Through this modification, we can tune the resistor values of $R_1$, $R_2$, $R_1'$ and $R_2'$ without any change of the pedestal DAC setting.

3. Performance

3.1. Waveform

For the TT01, a crucial problem is the degradation of the waveform of the fast and slow shapers, leading to lower pulse height, and more undershooting than expected, as shown in Figure 8. From our analysis of the layout parasitic extraction, we found that major stray capacitances are located amongst the fast/slow shapers and power/ground planes in the TT01. Thus, we redesigned the electrical schematic layout to reduce the stray capacitances when developing the TT02.

The improved TT02 waveforms are shown in Figure 8. The undershoots and low pulse heights of the TT01 are mitigated. Additionally, the significant upgrading of the pulse height for the fast shaper by a factor of $\sim$20% leads to an increase in the signal-to-noise ratio and a suppression of the noise level.
3.2. Linearity of signal

Here, we estimate the linearity performance between the input charge and output pulse. Figure 9 shows the linearity and its residual for a typical channel of the TT02, where the residual is defined as (obtained value – fitted value)/full scale. The obtained linearity performance shows that the residuals range from –2% to +0.5%. For small charge, the deviation from linear becomes larger because the fast shaper’s waveform rises more slowly in that range and the trigger signal is delayed. For larger charge, the deviation also increases, but this is instead due to a saturation of the pulse height. The linearity performance is also characterized by integral non-linearity (INL). The INL for the TT02 is estimated to be 2.5 %, which is comparable to other high-quality ASICs such as VA140 (< 3%) [4]. Furthermore, as described in Section 3.5, the energy resolution, which is mainly determined by the light yield of the scintillator (e.g., 54.7 % at 22 keV), is much larger than the systematic deviation due to the non-linearity. Thus, we conclude that the linearity performance of the TT02 is sufficient for spectroscopy.

3.3. Detectability of common-mode noise

The TT02 can detect common-mode noise by obtaining a median of the 32-channel ADC values. To estimate the common-mode noise properly, the pedestal levels for every channel should be the same while the original pedestal levels for each channel have some variation. To adjust the pedestal levels, we employ coarse 4-bit current DACs implemented in the resistor circuits $R_1$ and $R_1'$, and fine 5-bit voltage DACs consisting of a resistor and a variable current source located at the back-end of the fast and slow shapers, as illustrated in Figure 2.

Figure 10 (left) shows the pedestal distribution, with and without adjustment. We find that the pedestal adjustment is well-executed within ±2 ADC values. Here, the original pedestal distribution has a large variation up to 300 ch which corresponds to a ~ 200 mV offset voltage. Such a large offset voltage
is mainly caused by the $R_1$ feedback transistors as shown in Figure 2. Due to manufacturing variations, the two transistors that sandwich the poly resistor have different threshold voltages $V_{th}$, and several pairs of the current-mirror transistors are imbalanced. Additionally, the variation of $V_{GS}$ of the CSA input transistor also contributes an offset voltage via $R_{pz}$. These contributions conspire to create a large offset voltage, but a possible mitigation of the imbalance is to employ a common-centroid layout for the differential pair transistors and the current mirror.

We estimate the common-mode noise of test-pulse events in two ways. One is an offline procedure: in the FORCED readout mode, 32-channel ADC values are recorded for each event. By using all event data for every channel, the correction of the pedestal levels is very precisely executed by the software. By utilizing pedestal-corrected ADC values, we can estimate the offline common-mode noise. The other approach is an online procedure, which is relatively simple compared to the offline analysis. Pedestal variations are corrected only by the hardware adjustment. The median value for each event is stored in digital registers of the TT02 without any correction by the software, and the stored median is the “noise estimated by online hardware” which is available in both FORCED and SPARSE modes.

The estimated common-mode noises with the offline and online ways are shown in Figure 10 (right), and we find that these common-mode noises are in close agreement. The linear correlation coefficient is 0.73, with a probability of $\sim 10^{-165}$ that there is no correlation. This result indicates that even in operation of the SPARSE mode, we can properly estimate the common-mode noise. The offline method is more accurate in estimating the noise because the pedestal
correction can be executed precisely. However, it needs 32-channel data in the FORCED mode, and a reasonable estimate of the common-mode noise in the SPARSE mode can reduce the volume of flight data by an order of magnitude, which would be beneficial for a bus system.

We note that hereafter, every ADC value is represented with common-mode-noise subtracted. In laboratory experiments such as noise measurement or spectrum acquisition using radioisotopes, common-mode noise is suppressed well and the subtraction of the common-mode noise does not significantly affect our result. However, in the proton beam test, the ASIC was operated in a noisy environment with a large common-mode noise and we used the detection of the common-mode noise as described in Section 4.

3.4. Equivalent Noise Charge

We plot measurements of the equivalent noise charge (ENC) for the slow shapers of the TT02 in Figure 11. We find that the ENC value depends on the amount of input charge, which may be related to the ADC time period $T_{ADC}$ because shortening it by increasing the ADCK frequency gives lower ENC values, where the gradient of the RAMP signal is adjusted to keep the same ADC value with different ADCK frequencies. This might indicate that the $T_{ADC}$-dependence is caused by an accumulation of external noise in the HOLD signal during the $T_{ADC}$ period. To minimize this feature, we adopt a 60-MHz ADCK when obtaining energy spectra.

To detect low-energy photons around a minimum detectable energy of 20 keV, the ENC of the TT02 in the small input charge range (i.e., $\sim 0 \text{ fC}$) should be small with a target value of $\sim 2000 \text{ e}^-$, considering APD dark current of 3 nA at room temperature ($20^\circ\text{C}$). Figure 12 shows the measured ENC with different load capacitances at an input charge of 0 fC, where the 0-fC data
Figure 11: Input charge versus equivalent noise charge (ENC) with different ADCK frequencies. The load capacitance is 100 pF. In the higher frequency, a lower ENC is obtained.

can be obtained with a manual trigger mode without any charge input. The obtained ENC around a typical APD’s capacitance of 100 pF is $\sim2200 \ e^-$, which almost meets our requirement. We show the ENC distributions of the TT01 and TT02 in Figure 13. As mentioned in Section 3.1, while for the TT01 the stray capacitances distort the fast and slow shapers’ waveforms and degrade the signal-to-noise ratio, for the TT02 degradation of the waveforms is substantially reduced by redesigning the electrical layout, and we achieve a better ENC distribution in the TT02 by a factor of $\sim10\%$ compared with that of the TT01.

The obtained ENC is better than previous low-noise ASICs for APDs such as \cite{9} ($\sim3500 \ e^-$ at a 100-pF load), and the wide dynamic range (300 fC) is a significant feature. Thus, the dynamic range to the noise ratio (D/N) is a good barometer for evaluating the ASIC performance quantitatively. We summarize these characteristics to compare previously reported high-quality ASICs for APDs or similar use in Table 2, which indicates that the TT02 has performance comparable to the high-performance IDEAS ASIC (VA140).

3.5. Spectra

To detect X-ray photons up to 1 MeV, we adopt Ce:GAGG scintillators with a high density of 6.63 g cm$^{-3}$. If we choose a 10 mm thickness, $\sim20\%$ of 1 MeV photons can be efficiently detected. Furthermore, a 520 nm peak wavelength of Ce:GAGG matches well with the APDs and a large light yield of 57,000 photons MeV$^{-1}$ leads to a good energy resolution and lowers the minimum detectable energy. In addition, Ce:GAGG does not have any hygroscopic effects which makes handling easier compared with other hygroscopic scintillators such as Tl:CsI or Tl:NaI. Here, we use a Hamamatsu reverse-type APD (S8664-55 with
Figure 12: ENC distribution with different load capacitances. The best fitting linear function (solid line) is $2099 e^+ + 1.5 e^-/pF$. The measured data are taken from a channel which has a mean ENC as shown in Figure 13.

Figure 13: Equivalent noise charge distributions in TT02 = 2211 ± 102 (RMS). TT01 = 2393 ± 107 (RMS). The load capacitance is 100 pF.
Table 2: Comparison of the ASIC performance

|                | ENC [e−]* | Dynamic range [e−] | D/N |
|----------------|-----------|---------------------|-----|
| TT02 (this work) | 2200      | $1.87 \times 10^6$  | 850 |
| TIPPET08 [9]   | 3460      | $2.85 \times 10^5$  | 80  |
| CLEAR-PEM [10]| 1300†     | $2.71 \times 10^5$  | 210 |
| VA140 [4]      | 1400      | $1.25 \times 10^6$  | 890 |

*: 100-pF load
†: ENC was reported only at a 10-pF load.

an APD area of $5 \times 5 \text{mm}^2$) which is widely used as a scintillation detector [11], with its space use verified in small satellite projects [12, 13].

By using a Ce:GAGG scintillator of $10 \times 10 \times 50 \text{mm}^3$, a reverse-type APD of $5 \times 5 \text{mm}^2$ and the TT02, we obtained spectra from several radioactive sources such as $^{109}\text{Cd}$, $^{241}\text{Am}$, $^{133}\text{Ba}$, $^{57}\text{Co}$, $^{22}\text{Na}$ and $^{137}\text{Cs}$, measured at $20 \, ^\circ\text{C}$ and an avalanche gain of the APD at 100. The ADC channel and X-ray energy are linearly related, as shown in Figure 14. Here we show the representative spectra of $^{137}\text{Cs}$ (Figure 15) and $^{109}\text{Cd}$ (Figure 16). For the irradiation of $^{137}\text{Cs}$, a 32 keV line with an energy resolution of 41.6% (full width at half maximum: FWHM) is clearly detected, and the energy resolution at 662 keV is 6.7% (FWHM). To estimate the minimum detectable energy, we use the 22 keV line of $^{109}\text{Cd}$. Figure 16 shows the $^{109}\text{Cd}$ spectra obtained with the TT01 and TT02. While for the TT01 the 22-keV line is barely detected, for the TT02 it is clearly detected due to the improvement of the waveforms for fast and slow shapers with a larger signal-to-noise ratio. In particular, the improvement of the fast shaper’s waveform makes the contribution from the noise around 10 keV lower. Thus, we achieve the minimum detectable energy of 20 keV.

4. Radiation tolerance

To evaluate the radiation tolerance of the TT02, a proton irradiation test at 90 MeV was performed at the Wakasa Wan Energy Research Center in Fukui, Japan. We used 90 MeV protons because the cross section of the SEE for digital electrical elements rapidly increases from $\sim 10$ MeV and becomes saturated around 100 MeV [14, 15]. The proton beam is directly irradiated on the ASIC without any cover or cap, and every proton penetrates the ASIC because the proton range is $\sim 3.5 \text{ cm}$ in the Si medium, which is much longer than the thickness of the ASIC (<1 mm). The beam rate was $4.8 \times 10^7$ protons cm$^{-2}$ s$^{-1}$ with a duration of 2160 s. The total number of irradiated protons was $1.0 \times 10^{11}$ protons cm$^{-2}$, which corresponds to protons accumulated during 160 years in ISS orbit, where the in-orbit proton flux is calculated by the SPENVIS tool [16]. During the proton beam irradiation, we monitored the analog currents of $+1.65 \text{ V}$ and $-1.65 \text{ V}$, as shown in Figure 17. If SEL events were
Figure 14: Plot between ADC channel versus energy. The data points were obtained by measuring several radioactive sources such as $^{109}$Cd, $^{241}$Am, $^{133}$Ba, $^{57}$Co, $^{22}$Na and $^{137}$Cs. The dashed line represents the best-fit linear function.

Figure 15: Energy spectra of $^{137}$Cs measured with Ce:GAGG + a reverse-type APD (S8664-55) + TT02, measured at 20 °C. Obtained energy resolutions are 41.6% (FWHM) at 32 keV and 6.7% (FWHM) at 662 keV.
to occur in the TT02, the monitored currents would be expected to drastically increase. The result shows that the temporal variations of the analog currents are \(\sim 1\%\) and there is no sign of SEL events. In addition, after monitoring the SEU bit as illustrated in Figure 7, we did not obtain any SEU events during the proton irradiation. Considering that the TT02 has 1030-bit registers, the SEU cross-section of the TT02 is estimated to be \(\sigma_{\text{SEU}} < 2.2 \times 10^{-14}\) cm\(^2\) bit\(^{-1}\) (90% upper limit).

In the total dose effect, accumulation of charge occurs in the gate oxide, and continuing damage causes an increase of the leakage current and a shift in the voltage threshold of the transistors. The total dose of the proton irradiation is 10.1 krad (101 Gy), which corresponds to an in-orbit dose for \(\sim 10\) years because the typical dose rate in a low-earth orbit is roughly 1 krad year\(^{-1}\) (10 Gy year\(^{-1}\)). During the proton irradiation, test-pulse signals were continuously injected into the TT02. The ADC values of the test pulse gradually decreased by a factor of 10\%, while there was no significant difference between the measured pulse widths of the test-pulse events before and after the proton irradiation (1.11\(\pm\)0.05 ch versus 1.04\(\pm\)0.03 ch after the subtraction of the common-mode noise). Here, the measured pulse widths were affected by external noise, and before the subtraction of the common-mode noise we obtained original pulse widths of \(\sim 2.2\) ch. Thus, the detection of the common-mode noise as mentioned in Section 3.3 is useful for estimating and subtracting the external noise.

As shown in Figure 17, although the 10\% decrease of the pulse height after 10 years from launch slightly degrades the performance of the TT02, measured for example by an increase in the minimum detectable energy, this result indicates
that the total dose effect does not have a serious impact on the main functions of the TT02, considering that a typical mission life is $< 10$ years. Thus, we conclude that our developed ASIC has sufficient radiation tolerance for decadal-scale space applications, when protons are considered.

5. Conclusion

We have developed an analog and digital ASIC (TT02) dedicated to the readout of APDs combined with Ce:GAGG scintillators. By suppressing stray capacitances, the TT02 achieves a low-noise performance ($\sim 2200$ $e^-$) for a large detector capacitance of 100 pF with a wide dynamic range of 300 fC, and applications to spectroscopy from 20 keV to 1 MeV can be realized. The TT02 provides an excellent ability to detect common-mode noise with a sensitivity of $> 1$ ADC channel, which also enables a substantial reduction of the total amount of mission data by an order of magnitude. Through proton irradiation testing, we have demonstrated that the TT02 has a sufficient radiation tolerance for decadal-scale space use, and (1) is free of any SEE events such as SEL and SEU with $\sigma_{SEU} < 2.2 \times 10^{-14}$ cm$^2$ bit$^{-1}$ (90% upper limit), and (2) the total dose effect provides only a weak degradation (10%) for the spectroscopic applications of the TT02, while the primary functions work properly.

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