Layer transfer by controlled spalling

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Abstract
In this communication, we present what may be the simplest method yet devised for removing surface layers from brittle substrates. The process is called controlled spalling technology (CST) and works by depositing a tensile stressor layer on the surface of a substrate, introducing a crack near the edge of the substrate, and mechanically guiding the crack as a single fracture front across the surface. The entire process is performed at room-temperature using only common laboratory equipment. We present here, for the first time, the specific process conditions required for controlled spalling of Ge \langle 001 \rangle substrates using Ni as the stressor layer. We also illustrate the versatility of CST by removing completed CMOS circuits from a Si wafer and demonstrate functionality of the flexible circuits. Raman spectroscopy of spalled circuits with the Ni stressor intact indicates a residual compressive Si strain of 0.0029, in good agreement with the calculated value of 0.0022. Therefore, CST also permits new opportunities for strain engineering of nanoscale devices.

Online supplementary data available from stacks.iop.org/JPhysD/46/152002/mmedia
(Some figures may appear in colour only in the online journal)

1. Introduction
A number of ingenious layer release methods have been developed over the last few decades including Smart-cut [1], Eltran [2], epitaxial layer lift-off (ELO) [3] and their variants. These methods have allowed successful removal of a surface layer from one substrate material (primarily semiconductors) onto another substrate material by bonding thus enabling a variety of applications, such as silicon-on-insulator (SOI) for CMOS, 3D integration, optoelectronic devices, flexible electronics, to name a few. Despite their usefulness, all of these methods have the following shortcomings; (i) use of sophisticated and expensive equipment, (ii) modification of the substrate due to ion bombardment, high-temperature, or aggressive chemicals, (iii) limited options for removing partially or completely finished devices, and lastly (iv) these techniques are only applicable to a limited set of materials.

In this communication we describe a simple, cost-effective process for removing surface layers from essentially any brittle substrate without the previously described shortcomings. The process, called controlled spalling technology (CST) [4], is performed at room-temperature using inexpensive laboratory equipment and can be applied at nearly any point in the semiconductor manufacturing process; from ingots, to starting substrates, to completed devices. In previous work we have described the CST process in general, and characterized the physical and electrical properties of spalled GaAs/Ge photovoltaic structures [4]. In this work, we will describe the detailed experimental processing conditions for successful controlled spalling of Ge \langle 001 \rangle substrates using Ni as the stressor layer. We also present the measured fracture depth as a function of Ni thickness which enables control over the spalled layer thickness. Lastly, to illustrate the versatility of this technique, we then demonstrate the fabrication of flexible Si CMOS circuits as an example application and, for the
first time, characterize the residual strain present in these circuits.

2. Spalling mode fracture

It has been observed for decades that if a layer possessing tensile stress is deposited on the surface of a brittle substrate, often the layer would peel away from the surface and, in doing so, remove a portion of the substrate. This mode of fracture is referred to as substrate spalling. An analytical model of spalling was developed in the late 1980s [5, 6] which offered a direct and simple means of predicting critical loading conditions (film stress and thickness values) for which spalling fracture is possible as well as computing the equilibrium crack depth in the substrate. This unique mode of fracture results from the edge load created by the tensile stressor layer giving rise to a mixture of type I stress (opening mode) and type II stress (shear) which guides the crack to an equilibrium depth below the interface. An excellent review of mixed mode fracture is given in [7].

Nearly all research in spalling mode fracture has been conducted in an attempt to limit or suppress what is regarded as a mode of material failure. Recently it was demonstrated [8] that substrate spalling could be used as a means for fabricating thin Si substrates by depositing thick screen-printed metal (Al and Ag) pastes and annealing at 900 °C. The tensile stress in the metal layers increased upon cooling due to the coefficient of thermal expansion (CTE) mismatch between the metal and the Si, leading to spontaneous exfoliation of the surface.

The high temperature steps, required for creating the necessary stress, and the occurrence of spontaneous fracture upon cooling, severely limit the usefulness of the above approach. The high temperature prohibits layer spalling of prefabricated devices, and spontaneous fracture almost always leads to other competing modes of fracture, such as film cracking.

3. Controlled spalling technology

To make layer transfer by spalling as general and useful as possible, four basic elements need to be addressed; (i) the tensile stressor layer needs to be deposited with intrinsic stress in order to realize a low temperature process, (ii) since spontaneous spalling is not desired, a reliable crack-initiation strategy must be developed, (iii) a method is needed to mechanically control the subsurface crack propagation while suppressing parasitic fracture modes and (iv) a scheme is required for handling the spalled films once removed. Figure 1 shows an example of the controlled spalling process which satisfies the above four requirements and consists of the following steps; depositing a tensile stressor layer to a critical thickness, applying a flexible handle layer to the surface of the stressor, initiating a crack near the edge of the wafer, and mechanically guiding the fracture front across the substrate. Each step is described in more detail below.

4. Stressor layer deposition

Although a wide range of materials can be used as a stressor layer, Ni has proven to be convenient due to its low-cost, ease of deposition and high fracture toughness. The stress in the deposited Ni layer can be well-controlled using a dc Magnetron sputtering system by controlling the Ar gas pressure during deposition [9]. By adjusting the pressure from a few mT to tens of mT (the stable range of the system) the intrinsic tensile stress of the Ni can be tuned from around 300 MPa to 700 MPa, respectively. Electrodepositing Ni offers even more flexibility in stress control [10] with the advantage of lower cost. We have used both electroplating and sputtering interchangeably with similar results.

The role of the stressor layer is to provide sufficient loading to satisfy the condition for spalling, but not enough to cause spontaneous fracture. The various combinations of Ni thickness and stress that satisfy these conditions define the process window for CST. Figure 2(a) shows data points corresponding to various combinations of Ni stress and thickness that resulted in successful spalling of surface layers from 175 µm thick, 100 mm diameter Ge (0 0 1) wafers with approximately 4 µm Ga(In)As epitaxial surface layers. All these data are from sputtered Ni films and the reported stress values were established by measuring the radius of curvature on 500 µm thick, 100 mm diameter Si(1 1 1) monitor wafers and calculating film stress using a modified Stoney’s equation [11].

In figure 2(a), wafers that had Ni stress and thickness values in the subcritical region, could not be spalled at all. Therefore, the boundary of this region represents the critical loading condition for spalling of Ge (0 0 1) substrates and was calculated using the Suo and Hutchinson spalling model described in [6]. Experimentally, the critical loading data for Ge spalling follow the functional form of this model well, although the value of fracture toughness $K_{IC}$ required to match the data (0.4 MPa m$^{1/2}$) is about 25% lower than values obtained using indentation methods (0.53 MPa m$^{1/2}$) [12]. The upper boundary in figure 2(a) represents the combinations of Ni stress and thickness that tend to result in spontaneous spalling. This boundary is less fundamental and depends greatly on the
crack-initiation strategy used. An example computation of spalling parameters using the Suo and Hutchinson formalism [6] is shown in the online supplementary information section (stacks.iop.org/JPhysD/46/152002/mmedia).

The other role of the stressor layer is to establish the depth at which fracture occurs and therefore determines the thickness of the spalled layer. Figure 2(b) shows the measured relationship between the sputtered Ni thickness and the resulting thickness of the spalled Ge layer. These data also suggest the relationship between the Ni layer uniformity and the resulting spalled layer thickness uniformity. The error bars in figure 2(b) are a fixed value of ±2 μm originating from the ±1 μm precision of the digital micrometer used to measure the spalled films (including the 25 μm thick polyimide handle and stressor layers), in addition to the approximately ±1 μm variation in handle layer thickness. We observe a typical spalled layer thickness variation within the error of measurement over a 100 mm diameter wafer (data is shown in the online supplementary information section).

5. Crack Initiation

Because most of the materials that are attractive candidates for layer transfer are single crystal substrates, there are no pre-existing flaws or microcracks from which fracture can initiate. There are a number of “brute-force” crack-initiation methods available such as laser cutting, but this adds unnecessary complexity and cost to the process. The simplest method for creating a preferred crack-initiation region is to abruptly terminate the Ni film near the edge of the wafer. It is well-known [13, 14] that a discontinuous surface stressor layer creates a large strain gradient in the substrate near the free edge of the film. The nearly divergent nature of the stress fields near the film edge can result in peel σxz and shear σxμ stress in the GPa range within the substrate. When the handle layer is applied over the stressor layer and a small force is exerted near the edge, a crack is formed in the substrate at this high-stress region and propagated using the handle layer. The inset of figure 2(b) shows a cross-section SEM image of the crack-initiation region near the edge of a Ge(00 1) wafer. The image shows the original Ge surface, the location of crack initiation (where the free edge of the Ni layer was), and the depth at which fracture occurred (~7 μm below the surface).

6. Handle layer

The ability to mechanically fracture a thin layer from its host substrate without cracking or otherwise damaging the film requires that the crack initiates in a single location and propagates as a single crack front. The reason for this is that two or more intersecting fracture fronts almost always leads to film cracking. Also, the spalled film is under residual compressive stress due to the tensile Ni layer and capable of cracking if mishandled. A flexible handle layer attached to the surface of the stressor solves both problems of maintaining a singular fracture front, and permitting post-spall film handling. Due to the high curvature, the wafers in this work were held flat using a vacuum chuck after Ni deposition and prior to the application of the handle layer. We have used a variety of materials as handle layers and have found pressure sensitive tapes to be adequate and cost-effective. In the work presented here, a 25 μm thick polyimide tape was roll-applied onto the vacuum-chucked wafer and used as the handle layer. Spalling was then performed manually by gently (no noticeable force) pulling the handle layer upwards (roughly perpendicular to the wafer surface) while the wafer remained chucking to the vacuum table. In general, the addition of the handle layer to the surface of the stressor layer changes the loading conditions and thus the critical condition for spalling. As an extreme example, if a thick, rigid material is bonded to the surface of the stressor layer within the process window of figure 2(a), spalling becomes impossible. Most common polymer-based tape materials do not significantly affect the critical loading conditions provided that they are...
Figure 3. (a) Flexible SOI-based CMOS circuits formed by controlled spalling. These two 100 mm diameter flexible circuits were removed from the same 300 mm host wafer by depositing the Ni layer through a mask. The leftmost circuit in the image has the original handle and Ni layers attached to the surface, and the spalled Si has been removed rendering the underside of the devices visible through the remaining SiO₂ layer. In the flexible circuit shown on the right, the handle and stressor layers were removed revealing the original (Cu) surface. To provide mechanical support during handle and stressor layer removal, Al was first deposited on the SiO₂ layer followed by the application of a tape layer. (b) Cross-section transmission electron microscope (X-TEM) image of the flexible circuit with the stressor and handle layers still intact. The Pt was deposited on the underlying SiO₂ (BOX) layer during sample preparation. The Ti layer at the top of the image is the thin adhesion layer used before deposition of 6 μm Ni stressor layer. The image shows the aggressive dimensional scaling of the transistors in these circuits as well as the absence of any defects induced during removal. (c) Voltage versus time waveform from a 100 stage ring oscillator illustrates the retained functionality of complex integrated device arrays after CST. The measured delay per stage of 11.4 ps from the flexible circuit is similar to measurements taken from the rigid circuit before spalling.

7. Application to flexible circuits

Although layer separation by direct fracture may at first seem limited due to the presence of high stress fields and potential for material damage, we believe that this approach is by far the most versatile layer transfer technology yet devised. We have already demonstrated the preservation of material quality after spalling [4], and equivalence of electrical behaviour in defect-critical photovoltaic structures [15]. We present here another application of CST that further illustrates the versatility of a room-temperature layer transfer process by removing completed state-of-the-art CMOS circuits from a silicon wafer.

Figure 3(a) shows completed CMOS circuits fabricated on SOI substrates that have been removed, crack-free, from their host Si wafer using CST. Both 100 mm diameter circuits were removed from different regions of the same 300 mm diameter wafer by selectively depositing the Ni through a mask. CST was then performed and fracture occurred below the buried SiO₂ (BOX) layer leaving a ∼10 μm thick residual Si layer below the BOX layer. After chemically removing the residual Si layer, the entire backside of the circuit is visible through the remaining BOX layer (leftmost circuit in figure 3(a)).
from the reference Si and the thin Si in the circuit layer. The
removed in step (\(a\)) exposing the original (Cu) surface of the circuit.

To recover the original (front) surface of the circuit, an Al layer is first deposited on the BOX layer, followed by the application of flexible tape which serves as the new mechanical support layer. With the new support layer in place, the original handle layer can then be removed followed by chemical etching of the Ni stressor and Ti adhesion layers. This process flow is shown schematically in figure 4. The rightmost circuit in figure 3(a) is an example of a flexible circuit fabricated using CST with the original surface (Cu metallization) exposed.

A cross-sectional TEM image of the spalled circuit is shown in figure 3(b). As seen in the image, these state-of-the-art circuits feature a Si body thickness of only 6 nm, 30 nm transistor gate length and 100 nm device spacing. Also, no evidence of damage to the devices or metallization can be found in the TEM sample. The final flexible circuit shown in figure 3(a) (right) was then tested electrically and shown to have equivalent behaviour to the circuit before spalling. Shown in figure 3(c) is the voltage versus time data taken from a 100 stage ring oscillator on the flexible circuit. The delay per stage was measured to be 11.4 ps which was similar to the pre-spalled data. A more in-depth analysis of the electrical characteristics of flexible circuits fabricated in this manner can be found elsewhere [16].

As mentioned above, spalled substrate layers are under residual compressive stress due to the strain partitioning between the Ni stressor and the spalled film. As an example of this, a Si circuit layer was spalled and the Ni stressor layer was left intact on the surface. The residual Si was etched down to the BOX layer leaving the backside of the thin circuit exposed (similar to the leftmost circuit image in figure 3(a)). Raman spectroscopy was then used to measure the strain in the thin Si layer [17]. Figure 5 shows the Raman spectra (632 nm) from the reference Si and the thin Si in the circuit layer. The measured peak shift \(\Delta\omega\) of 2.4 cm\(^{-1}\) corresponds to an in-plane biaxial compressive strain \(\varepsilon_{xx}\) of approximately 0.0029. If we assume the Ni is fully relaxed after removal of the residual Si, and the thin remaining Si remains attached to the Ni (no slippage), then the theoretical strain can be calculated using:

\[
\Delta\varepsilon = \frac{\Delta\sigma_{\text{Ni}}}{M_{\text{Ni}}},
\]

with \(\Delta\varepsilon\) is the strain change in Si (and Ni), \(\Delta\sigma\) is the change in Ni stress and \(M_{\text{Ni}}\) is the biaxial modulus of the sputtered Ni film (275 GPa). The as-deposited Ni stress was approximately 600 MPa as measured on a Si monitor wafer, giving a calculated Si strain of 0.0022, in reasonable agreement with the Raman data. The ability to easily manipulate the strain state of the circuit after chip fabrication opens up new opportunities for optimizing performance in microelectronic circuits.

8. Concluding remarks

By mechanically controlling what was previously considered a material failure mode, we have been able to demonstrate a method for removing thin surface layers from brittle substrates that is highly simplified compared to pre-existing layer transfer methods. Using only common laboratory equipment, and performing layer transfer at room-temperature, CST can be applied to material systems that are difficult or impossible using ion-implant or epitaxial-based methods. It is also important to mention that all of the layer transfer work described in this communication was performed in a general laboratory environment; no cleanroom was required.

One challenge associated with CST originates from the residual stress and slight curvature that the layers possess after spalling. Processing of thin, stressed films requires the development of film handling strategies and equipment that may be specific to the application. These residual stresses, however, can also provide new opportunities for strain engineering nanoscale electronic devices such as Si CMOS circuits.

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**Figure 4.** Process flow used to fabricate flexible circuits using CST. In (a), the spall depth was approximately 10 \(\mu\)m below the buried SiO\(_2\) (BOX) layer. The residual Si layer was chemically etched (b) down to the BOX. In (c), a 2 \(\mu\)m thick Al layer was deposited on the BOX, followed by the application of a bottom tape ‘support’ layer. The PVC-based handle, Ni stressor and Ti adhesion layers were all removed in step (d) exposing the original (Cu) surface of the circuit.

**Figure 5.** Raman scattering using a 632 nm laser of a bulk Si reference (black) and the thin Si layer of the circuit measured through the exposed BOX layer (red). The Ni stressor is still intact on the opposite surface of the thin circuit resulting in a Si peak shift of 2.4 cm\(^{-1}\) to the right (compressive strain).
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