Research and design of digital unit for direct digital frequency synthesizer

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Abstract: The direct digital frequency synthesizer (DDS) is a new kind of all digital frequency synthesizer, which has fast frequency switching speed and high frequency resolution. It has been widely used in the field of signal processing. In this article, we analyze the basic principle of DDS and study several methods of phase-amplitude conversion. We use the method of searching ROM table for rough rotation and the optimized CORDIC algorithm based on excess-fours structure for fine rotation to achieve the phase to amplitude conversion. The power consumption and area of the fine rotation element are reduced with the preprocessing of the phrase. The output frequency is increased by using a 4-channel-interpolation structure. After the design is completed, we verify its correctness and evaluate its performance. The results show the phase-amplitude conversion algorithm meets the need of correctness and the DDS can work stably at 1GHz.

1. Introduction

With the rapid development of modern communication system and signal processing technology, people put forward higher requirements on the performance of signal source, which not only has higher accuracy and stability, but also can quickly complete the frequency switch. In 1971, the concept of direct digital frequency synthesizer has been proposed [1], which is based on digital circuit, synthesizing the required signals directly from the concept of phase quantization. DDS has the advantages of high frequency resolution, short frequency switching time, wide tuning bandwidth and low power consumption. It has been widely used in radar, communication system and quantum measurement and control [2].

In this paper, we analyze the basic principle of DDS and research several methods of phase to amplitude conversion technology. After considering the required power consumption and on-chip area, we choose the method of searching ROM table for rough rotation and an optimized CORDIC (Coordinated Rotation Digital Computer) arithmetic based on excess-fours structure [3] for fine rotation. By preprocessing the phase, the area and power consumption of the fine rotation element are reduced and a 4-channel-interpolation structure is adopted to raise the system clock frequency to 1GHz.

2. The basic principle of DDS

Figure 1 shows the basic structure of DDS, including a phase accumulator, a phase to amplitude converter, a digital-to-analog converter (DAC) and a low pass filter. Driven by the clock, the phase accumulator accumulates the frequency control word (Fword), and then adds the phase control word (Pword) to get the phase to be converted. Then the phase is fed into the phase-amplitude conversion
module to output the discrete sinusoidal signal and the DAC converts the discrete digital signal into a continuous analog signal to generate the stepped approximation of the sinusoidal signal. Finally, the continuous smooth sinusoidal waveform is obtained with a low-pass filter by filtering out the high frequency component.

![Figure 1. Schematic diagram of DDS](image)

3. Analysis of phase to amplitude conversion method

Phase to amplitude conversion logic is one of the key technologies in the DDS design. At present, the commonly used methods include searching lookup ROM table, piecewise polynomial approximation and angle decomposition, namely CORDIC algorithm [4].

Lookup table method is the most intuitive phase to amplitude conversion technology. Usually the high P bits of the phase accumulator are chosen as the address to the ROM table which stores the L bits amplitude value of the sinusoidal signal corresponding to $2^P$ phases, so the capacity of the ROM table is $2^P \times L$. Although many literatures [5,6] have proposed methods of compressing the ROM table, but the implementation of a high precision DDS still needs a large capacity of ROM, which will occupy a large amount of on-chip area. In the industry and academia, there are few cases completely using the structure of searching the lookup table to design a DDS.

The piecewise polynomial approximation method [7] divides the sinusoidal curve into several subintervals and approximates the sinusoidal value of each subinterval by polynomial with given coefficients. Its advantage is that it does not need to use a ROM, but higher precision sine value means higher order polynomials, which needs more multiplying units and puts forward higher requirements for the performance of the system.

As one of the angle decomposition methods, CORDIC algorithm is one of the most commonly used algorithms in DDS phase to amplitude conversion technology. Its characteristic is that it can approach the sine value of the target angle through iteration only by shifting and adding operations, which is very suitable for the implementation of very-large-scale integration (VLSI).

The principle of classical CORDIC is as follows: In the polar diagram, point $(x_0, y_0)$ rotates anticlockwise at angle $\theta$ to reach $(x_1, y_1)$ and through trigonometric transform, the result becomes to Eq. (1):

$$
\begin{bmatrix}
x_N \\
y_N
\end{bmatrix} =
\begin{bmatrix}
\cos \theta & -\sin \theta \\
\sin \theta & \cos \theta
\end{bmatrix}
\begin{bmatrix}
x_0 \\
y_0
\end{bmatrix} =
\cos \theta
\begin{bmatrix}
1 & -\tan \theta \\
\tan \theta & 1
\end{bmatrix}
\begin{bmatrix}
x_0 \\
y_0
\end{bmatrix}
$$

(1)

Hypothesize $x_0 = 1, y_0 = 0$, then the result becomes to Eq. (2):

$$
\begin{cases}
x_N = \cos \theta \\
y_N = \sin \theta
\end{cases}
$$

(2)

The rotation angle $\theta$ can be decomposed into the sum of multiple iterations of several small angles.
as Eq. (3):

\[
\theta = \sum_{i=0}^{i=N-1} \delta_i \cdot \theta_i
\]

\[
\delta_i = \{-1,+1\}, \theta_i = \tan^{-1} \frac{1}{2^i}
\]

Therefore \( x_n \), \( y_n \) can be represented by Eq. (4):

\[
\begin{bmatrix} x_n \\ y_n \end{bmatrix} = \prod_{i=0}^{i=N-1} \cos \theta_i \cdot \prod_{i=0}^{i=N-1} \begin{bmatrix} 1 & -\tan \delta_i \theta_i \\ \tan \delta_i \theta_i & 1 \end{bmatrix} \cdot \begin{bmatrix} x_0 \\ y_0 \end{bmatrix}
\]

\[
= K \cdot \prod_{i=0}^{i=N-1} \left( \delta_i 2^{-i} \right) \cdot \begin{bmatrix} x_0 \\ y_0 \end{bmatrix}
\]

\[
K = \prod_{i=0}^{i=N-1} \cos \left( \tan^{-1} \frac{1}{2^i} \right)
\approx 0.607253, N \to \infty
\]

The core of CORDIC algorithm is to make \( \theta_i = \tan^{-1}(1/2^i) \), turning each rotation into a simple addition and shift operation, which is ideal for hardware implementation. However, the traditional CORDIC algorithm needs to iterate many times to get a result and must judge the direction of rotation per iteration. Many literatures [3,8] have proposed an improved scheme for CORDIC algorithm.

4. Design and implementation of DDS

4.1. Phase accumulator module
Phase accumulator is one of the important components of DDS whose computation delay restricts the speed of DDS system to a great extent. Meanwhile, the number \( N \) of the accumulator determines the frequency resolution of the DDS, that is \( \Delta F = F_{clk}/2^N \). More precise frequency resolution requires more bits of adder but at the same time incurs higher latency. After comprehensive consideration, a 32-bit adder is selected as the phase accumulator in this paper to achieve a balance between the delay time and frequency resolution. If we directly use a common full adder to implement the 32-bit addition, it will bring a large delay to restrict the frequency of the clock as a result. Generally, a 8*4 bit Carry Look-ahead Adder (CLA) is used to implement the 32-bit addition. The approach of pipeline can indeed improve the clock frequency of the system, but it also means that it takes 8 clock cycles to get the result of addition, which seriously restricts the speed of frequency switching. Therefore, in this paper we finally choose the binary Kogge-Stone-structure adder as the phase accumulator. For the N-bit addition operation, it only needs \( \log_2 N \) steps to calculate the carry generation and carry propagation signal [9], which can greatly reduce the delay.
4.2. Phase to amplitude conversion module

The overall design of phase to amplitude conversion module is shown in Figure 2. We choose the method of searching the lookup ROM table for rough rotation and an optimized CORDIC arithmetic based on excess-fours structure for fine rotation. This paper’s phase word arrangement is shown in Fig. 3. The input phase is represented in binary and ranges from all 0 to all 1, representing 0 to $2\pi$. The high 19 bits are chosen to determine the output amplitude values. The 3 MSBs are selected for segment selected, the middle 7 bits are used for the lookup ROM table, the last 9 bits are used for 3 times fine rotation and the other LSBs are truncated. According to the symmetry of sine and cosine functions, the full periodic sine and cosine signals can be obtained only by calculating the interval from 0 to $\pi/4$. Its transformation mode is shown in Table 1 ($\theta$ represents $\psi[15:0]$).

| Octant $\psi[18:16]$ | Angle range       | Sine              | Cosine            |
|----------------------|-------------------|-------------------|-------------------|
| 000                  | $[0, \pi/4)$      | $\sin\theta$     | $\cos\theta$     |
| 001                  | $[\pi/4, \pi/2)$  | $\cos(\pi/4-\theta)$ | $\sin(\pi/4-\theta)$ |
| 010                  | $[\pi/2, 3\pi/4)$ | $\cos\theta$     | $-\sin\theta$    |
| 011                  | $[3\pi/4, \pi)$   | $\sin(\pi/4-\theta)$ | $-\cos(\pi/4-\theta)$ |
| 100                  | $[\pi, 5\pi/4)$   | $-\sin\theta$    | $-\cos\theta$    |
| 101                  | $[5\pi/4, 3\pi/2)$| $-\cos(\pi/4-\theta)$ | $-\sin(\pi/4-\theta)$ |
| 110                  | $[3\pi/2, 7\pi/4)$| $-\cos\theta$    | $\sin\theta$     |
| 111                  | $[7\pi/4, 2\pi)$  | $-\sin(\pi/4-\theta)$ | $\cos(\pi/4-\theta)$ |

The value of sine and cosine of the sum of $\psi[15:0]$ and pre-rotation quantity is stored in the lookup ROM table. We use the three-stage rotation structure to pre-rotate 3’b100 at each stage, so the total pre-rotation amount is 9’b100100100, namely 292. Therefore, the value stored in the lookup ROM table is as follows:

$$
\begin{align*}
  x &= \cos (2\pi (\psi[15:0] \times 2^9 + 292) / 2^{19}) \\
  y &= \sin (2\pi (\psi[15:0] \times 2^9 + 292) / 2^{19})
\end{align*}
$$

The relationship between the amount of rotation and the input is shown in Table 2.

| Rotation value input | Amount of rotation |
|----------------------|-------------------|
| 000                  | -4                |
| 001                  | -3                |
| 010                  | -2                |
| 011                  | -1                |
| 100                  | 0                 |
| 101                  | 1                 |
| 110                  | 2                 |
| 111                  | 3                 |
The ROM capacity of sine and cosine is both \(27 \times 16 = 4\) kb and the relationship between the amount of rotation and the input is shown in table 2. Compared with literature [3], there are two optimizations in saving power and area. One is that the product of \(\left(\frac{\pi}{4}\right) \cdot (X, Y)\) and \(\left(3\frac{\pi}{4}\right) \cdot (X, Y)\) is obtained from multiplication operation in real time while in literature [3], it is stored in the lookup ROM table. Therefore, the area is reduced even further. In this paper, we use the radix-4 booth algorithm partial product compression multiplier to implement multiplication, which can reduce the computation latency and the number of partial products. The second is that the rotation cell is simpler than that in literature [3], which means less power and area. In this paper, by preprocessing the angle of subsequent rotation in advance, there are only 8 kinds of rotation instances as shown in table 2, and it can further simplify the design of the rotating element. When \(\psi[16]=1\), the angle of rotation \(\phi[15:0]\) is \(16'b1111_1111_1111_1111-\psi[15:0]\), namely \(\pi/4-\theta'.\) In practical operation, it can be equivalently implemented as \(~\psi[15:0]\) and this can greatly reduce the delay. In literature [3] there are 24 kinds of rotation instances and it is guessed the rotation cell need to rotate -5 which can be decomposed into the sum of -8 and +3, and -8 can be treated as -1 in the higher rotate cell. As a result, the rotation cell is more complex and needs the circuit of judgment. Literature [10] has proposed some improvement on the excess-fours structure, but for the reason that it does not preprocessed the phrase, there are 48 kinds of rotation instances. Compared with the method in literature [10], the power consumption and area of the fine rotation element in this paper are reduced by 5.7% and 5.6% respectively. The algorithm of the first excess-fours rotation cell in this paper is shown in Eq. (6):

\[
\begin{bmatrix}
x_N \\
y_N
\end{bmatrix} = \begin{bmatrix}
1 & -\frac{\pi}{4} (4\phi[8] + 2\phi[7] + \phi[6] - 4) \times 2^{-12} \\
\frac{\pi}{4} (4\phi[8] + 2\phi[7] + \phi[6] - 4) \times 2^{-12} & 1
\end{bmatrix} \begin{bmatrix}
x_{\text{rom}} \\
y_{\text{rom}}
\end{bmatrix}
\] (6)

The remaining two rotation cells are similar to the first one.

After three fine rotations, output the sine and cosine values according to table 1. Compared with the traditional CORDIC algorithm, the method adopted in this paper has the following advantages: Firstly, we omit the judgement of the direction in each rotation. Secondly, the multiplication with the scaling factor \(K\) is eliminated. Thirdly, we reduce the number of rotations to \(N/3\) per \(N\) bits.

4.3. Linear phase interpolation structure

In this paper, we adopt a 4-channel-interpolated structure to improve the output frequency. To output signals of the same frequency, the clock frequency of the DDS with the interpolation structure is \(1/4\) of that of the traditional single-channel DDS. Its schematic diagram is shown in the Figure 4. The phase accumulator sets the input to 4 times the frequency control word i.e. \(4\omega\), to generate a phase value of \(\sum (4\omega)\) and get the phase \(2\omega\) by shifting and \(3\omega\) by addition. Then the sum of the phrase \(\sum (4\omega)-3\omega, \sum (4\omega)-2\omega, \sum (4\omega)-\omega, \sum (4\omega)\) and phrase control word \(\theta\) is sent to the phase-amplitude conversion module to generate a 4-way output signal. Finally, we use a clock with 4 times the frequency of that of the phrase accumulator to perform parallel series conversion and output sine and cosine signals in sequence.
5. Experimental Verification
The RTL code is simulated with ModelSim and the output data is written to a TXT file. Then, by comparing with the data obtained from simulation program, the results show that this component meets the need of correctness. After using the Design Compiler (DC) tools with our specific target library to synthesize, the system clock frequency can run stably at 1GHz.

6. Summary
In this paper, we analyze the basic principle of DDS and research several methods of phase to amplitude conversion technology. The adder with Kogge-Stone structure is adopted to implement the phase accumulator to reduce the latency and increase the clock frequency. We use the method of searching the lookup ROM table for rough rotation and the optimized CORDIC algorithm based on excess-fours structure for fine rotation to achieve the phase to amplitude conversion. By preprocessing the phase, we reduce the area and power consumption of the fine rotation element by 5.7% and 5.6% respectively. At the same time, a 4-channel-interpolation structure is adopted to increase the frequency of the output signal. Finally, the correctness of the phase to amplitude conversion algorithm is verified by simulation experiments and after using the Design Compiler tools to synthesize, the results show that the system clock frequency can run stably at 1GHz.

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