A 7.6-ns Delay Subthreshold Level-Shifter Leveraging a Composite Transistor and a Voltage-Controlled Current Source

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ABSTRACT A novel level shifter (LS) circuit that uses a new low-power approach based on a parasitic capacitance voltage controlled current source is presented to minimize the propagation delay (PD) and maximize the voltage conversion range. This new scheme uses a simplified circuit including a dependent current source, a composite transistor made of three interconnected n-channel MOSFETs (TnM), one CMOS input inverter, and one CMOS output buffer to provide a fast response time. The circuit utilizes the combined action of the equivalent parasitic capacitance of the TnM, the value of which changes dynamically according to the transient value of the input voltage, and the dependent current source to shift the input signal level up from subthreshold voltage levels to +3.0 V, with minimal delay and power consumption. The LS circuit fabricated in 0.35 µm CMOS technology occupies a silicon area of only 25 µm × 25 µm. The LS shows measured rising and falling PDs of, respectively, 4 and 11.2 ns. The measured results show that the presented circuit outperforms other solutions over a wide frequency range of 1 to 130 MHz. The fabricated circuit consumes a static power 31.5 pW and a dynamic power of 3.4 pJ per transition at 1 kHz, VDDL = 0.8 V, and a capacitive load of CL = 0.1 pF.

INDEX TERMS Level shifter, high-speed, subthreshold operation, equivalent parasitic capacitance, wide conversion range, low-power consumption.

I. INTRODUCTION Level shifters (LSs) are key circuits in numerous micro-electronic systems including systems-on-chip (SoCs) and complex system-in-package (SiP) devices [1], [2], [3], [4]. These circuits are used to translate one signal level to another, allowing signals to be properly transferred across different supply voltage domains [5], [6], [7]. High-performance telecommunication systems require high-speed LS circuits consuming as low power as possible. Low-power applications, such as peripheral modules for the Internet of Things or implantable medical devices, working at medium or low frequencies, often use subthreshold circuits to decrease static and dynamic power consumption [8], [9], [10]. Energy-efficient circuit designs using subthreshold operations are well suited for these applications that do
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FIGURE 1. Simplified level shifter circuit schematic: (a) basic structure of current source-based LS, (b) PD between input and output signals.

not require fast circuit operation [11], [12]. Hence, high-performance subthreshold LSs are necessary in these low-power applications [13], [14].

SoCs frequently use multiple voltage supply and signal levels inside their various building blocks [15], [16], [17], [18]. Using multiple technologies operating at various supply voltages within the same SiP can decrease fabrication cost and power consumption [19], [20], [21]. Emerging technologies using lower supply voltages are highly optimized to improve performance; hence, using them in SiP is advantageous but expensive [22], [23]. Therefore, reliable LS circuits support robust Technologies where higher supply voltages can cohabit with lower supply voltages to accommodate both high-speed high-performance, and low-power non-critical blocks within the same SiP [24], [25], [26], [27], [28], [29].

Fig. 1 (a) illustrates the basic structure of a conventional current mirror-based LS (CBLS). Different techniques and innovations have been proposed to improve the main parameters of CBLSs, including PD (Fig. 1(b)), static and dynamic power consumption, and dynamic conversion range [30], [31], [32], [33], [34], [35], [36], [37]. Such improved circuit has less contention than the latch-based LS [29]. However, it can exhibit a large static short-circuit current when the input pulse intensity is high (Fig. 1(a)), which can significantly increase the power consumption.

In [36], a logic error detection circuit for near-threshold operation is used to enhance the performance of CBLS as shown in Fig. 2 (a). In this schematic, the level shifting part includes M\textsubscript{P1}-M\textsubscript{P4}, M\textsubscript{N1}, and M\textsubscript{N2}, while the logic error detection part consists of M\textsubscript{P5}, M\textsubscript{P6}, and M\textsubscript{N3}-M\textsubscript{N5}. Although this LS was implemented in a CMOS 14-nm process using minimum transistor sizes, two-stage topology resulted in a rather long PD and narrow conversion range.

The CBLS reported in [38] (Fig. 2(b)) uses the n-type MOSFET M\textsubscript{N4} to minimize the static current. However, utilizing 15 transistors to implement the LS can result in a larger circuit area. This CBLS also uses a substantial amount of power, and the feedback loop increases the PD.

The CBLS presented in [39] uses a digital circuit based on error correction, as shown in Fig. 2(c), to overcome the limitations of conventional LSs. However, the presented LS suffers from significant contention in nodes OUT and Y. The contention is due to the superimposition of M\textsubscript{P6} with M\textsubscript{N8} at the output node on the right-hand side, and M\textsubscript{P1} with M\textsubscript{N3} on the left-hand side. The circuit in [39] also suffers from a similar problem like the LS circuit in [38]. The drawbacks associated with this topology are a long PD due to the feedback loop and a bulky area. Since the circuits shown in Figs. 2(b) and 2(c) operate as dual-stage circuits, their total speed is limited due to the resulting long PD.

In this paper, a novel subthreshold LS circuit based on a voltage controlled current source (VCCS) combined with the equivalent parasitic capacitance (C\textsubscript{p}) of three interconnected n-channel MOSFETs (TnM) is presented to shift the signal level up with a shorter PD, a wider conversion range, and a lower power consumption compared to other solutions. In our approach, a parasitic capacitor value C\textsubscript{p} varies according to the voltage drop across the TnM and the operating regions of the MOSFETs (i.e. triode or saturation mode), providing the LS circuit with minimal delay and power consumption for proper low-power operation in subthreshold region. It will be shown in the next sections that using the dynamic parasitic capacitor provided by the TnM at node V\textsubscript{A} (Fig. 3 (c)), compared to a single transistor, allows this LS design to operate in subthreshold region while providing the same delay and a wide conversion range compared to a LS working in strong inversion and consuming more power.

A low-power latch-based LS is presented in [40]. In this topology, the MOS transistors of M\textsubscript{P6} and M\textsubscript{P7} are added on the pull-up network in their diode configuration to mitigate any strong contention. However, this connection affects the swing of the circuit because the drain of M\textsubscript{N2} can only reach V\textsubscript{DDH} − |V\textsubscript{thp}|. In addition, the rise time of node D is decelerated due to the node connected transistors. Consequently, the propagation delay is increased. A latch-based structure associated with current limiter is presented in [41]. It is used to keep the current flowing during transitions to the minimum. The output is pulled down during transitions easily due to the limited current. In this LS circuit development, the diodes or isolation of gate is not obligatory. Furthermore, the current sources are switched off outside transition times. Consequently, the short-circuit static current is almost zero. The drawback of this circuit is that the buffer circuit input exposes the LS to noise by making the output signal floating high when the input pulse is low. A latch-based structure in which the delay elements and five series diode-connected MOSFETs create an intermediate supply voltage (V\textsubscript{IDD}) is presented in [42]. In this circuit, V\textsubscript{IDD} is lower than V\textsubscript{DDH} and is connected to pull up the network to reduce the drive strength. The circuit operation is highly challenging at low V\textsubscript{DDL} because a trade-off must be made between speed, area, and static power due to the delay element and the diode-connected transistors.

In this design, the current source supplies the needed current to the TnM within a given operating period, while
the TnM converts the obtained current from the VCCS to a voltage level greater than the input voltage level. A feedback mechanism is designed to provide the right amount of current to the TnM while keeping the LS in sleep mode after the transition times to minimize the total power consumption (TPC). The TnM provides fast charge/discharge due to its equivalent parasitic capacitance to minimize the PD. The combined action of the VCCS and the TnM also maximizes the conversion range (CR) compared to other LS circuit solutions.

The remaining sections of this article are organized as follows. The configuration and the operating principle of the proposed LS circuit are covered in Section II. The implementation of the circuit, mathematical discussion, and the post-layout simulation results are presented in Section III. The measured performance of the LS fabricated prototype is provided in Section IV. The results are discussed and compared to other solutions in Section V, followed by conclusions in Section VI.

II. PROPOSED LS ARCHITECTURE AND OPERATION

The proposed LS is constructed based on a current mirror structure, thus it benefits from the high impedance of its output node and good matching capability. A feedback network circuit is employed to control the current supplied to a modified current mirror-based LS (MCLS) (Fig. 3(a)). This area-efficient circuit block consists of a composite transistor including three interconnected MOSFETs providing level shifting and an equivalent parasitic capacitance $C_p$ at node $V_A$. In the simplified schematic of Fig. 3(c), when $IN = 1$, the VCCS charges $C_p$, which pushes $V_A$ upward. The charging of $C_p$ by VCCS provides a voltage ramp at node A. Then, the voltage $V_A$ is converted to $V_{DDH}$ through the output buffers (Fig. 3(a)).

In Fig. 3(a), the variable $V_A$ corresponds to the voltage of an important circuit node that is later used to produce the current source control voltage ($V_C$), as illustrated in Fig. 3(c). The voltage variation ($\Delta V_A$) is measured by the feedback network and converted into a current variation ($\Delta I_A$). Then, $\Delta I_A$ is subtracted from the main mirrored current “$I$”. Finally, the rest of the current ($I_1$) is delivered by the MCLS. Therefore, when $\Delta I_A = I$, the feedback network completely shuts the circuit down. Consequently, the average power consumption, corresponding to the area shown in green in Fig. 3(b) is saved and compared to a LS circuit without feedback.

Converting $V_A$ to $V_{DDH}$ using a buffer can consume as much power as the energy saved by the feedback mechanism, as shown in Fig. 3(b). A large equivalent parasitic capacitance is seen at node $V_A$ due to the TnM (Fig. 3(c)). The feedback network, therefore, must control the voltage $V_A$ at this critical node. The controlled charge/discharge of the large parasitic capacitance at node $V_A$ gradually shifts the level of the applied signal. Then, the output buffer (i.e. a chain of inverters) in the lower-strength nodes transforms the enhanced signal at node $V_A$ into $V_{DDH}$ with minimal contention. As explained in detail in Section III, the TnM provides a simplified topology designed to efficiently exploit the parasitic capacitance of the MOSFETs. Accordingly, this approach for converting the input signal into $V_{DDH}$, based on the TnM and the feedback network, significantly improves PD, TPC, and CR as compared to other implementations. Furthermore, the closed-loop negative feedback regulates the current delivered to the TnM to minimize any unnecessary power consumption.

The circuit operation is illustrated in Fig. 3(c). The voltage-controlled current source (VCCS) supplies a variable...
current to the TnM and produces a voltage $V_A$, which allows to generate the control voltage ($V_C$) of the feedback circuit. Finally, $V_A$ is amplified through two inverters to buffer the signal and to generate $V_{DDH}$. The design of the level shifter was summarized in a conference paper [7]. Compared to [7], this paper presents a detailed description of the design, and provide the measurement results obtained with the fabricated chip, which were not available in [7]. Detailed design explanations and a mathematical analysis of the circuit are also provided to fully cover the operation of the presented circuit. The measurement results obtained with the fabricated chip are discussed and the performance of our new level shifter design is compared with other solutions.

The advantages of the presented wide conversion range LS are summarized as follows:

1) A VCCS and a TnM are used to progressively increase the input signal level. Therefore, the opposition between the strong pull up and the weak pull down is completely removed, resulting in significant improvements in PD, CR, and TPC.

2) In contrast with the conventional current mirror-based LS, wherein the quiescent current limits the LS performance, the feedback used in this LS design permits the circuit to work only during a given time interval. When no input transition occurs, the LS is placed in stand-by mode, thereby significantly decreasing the leakage current and the static power.

3) Our topology uses only one effective stage to raise the signal intensity, rather than two or more, resulting in reduced propagation latency and complexity.

4) The presented circuit utilizes a large transistor on the low side of the current mirror to address the weak pull-down issue associated with the low $V_{DDL}$. This allows converting the low amplitude signal into a pulse of larger amplitude $V_{DDH}$. Consequently, this circuit is suitable for use in the subthreshold region.

5) The presented circuit uses fewer transistors compared with conventional CBLS circuit implementations, resulting in area saving.

III. CIRCUIT IMPLEMENTATION AND SIMULATION

A detailed description of the proposed LS circuit implementation is presented in Fig. 4(a). It consists of several subblocks, including a TnM, a feedback network, a VCCS, an input inverter, and an output buffer.

A. CIRCUIT DESCRIPTION

In the presented LS circuit (Fig. 4(a)), the input signal (IN) is applied to the n-channel MOSFET MN1, whereas the voltage $V_A$, which is in-phase with IN, is applied to the gates of MP1 and MP2 (p-type MOSFETs, superimposed with MN1 to cut off the static current). Accordingly, this circuit is allowed to operate only within the duration of the PD of the input signal to the output of the circuit. Otherwise, $V_A$ turns off MP1 and MP2 to avoid any current ($I_1$) flowing into the TnM and remains in idle mode. The role of the TnM composite MOSFET made of MN2, MN3, and MN4 is to shift the level of the input voltage upward by providing a dynamic equivalent capacitor, the value of which depends on the value of IN, charged by VCCS at node $V_A$. When $IN = "1"$, the VCCS charges $C_p$. When $IN = "0"$, the TnM discharges $C_p$ without the need for extra switches. In contrast to using a single transistor to charge $V_A$, this scheme provides a dynamic capacitor value at node $V_A$, the value of which depends on the operating region of MP2, MP4, MN2, MN3, and MN4. When $IN = "1"$, the voltage $V_A$ increases and puts MP2 and MP4 in the triode region while transistors MN2, MN3, and MN4 are in cut-off region. The value of $C_p$ is smaller in triode than in saturation, hence decreasing the dynamic power consumption and the delay. When $IN = "0"$, transistors MN1, MP2, and MP4 are in cut-off region and the voltage $V_A$ decreases. Consequently, MN2, MN3, and MN4 are put in the triode region, which also decreases the value of $C_p$ as compared to saturation mode, hence decreasing the dynamic power consumption and the delay [37].

The total gate capacitance of the MOSFET is given by $C_g = C_{OX}WL$ where W and L are, respectively, the width and the length of the MOSFET channel; and $C_{OX}$ is the parallel plate capacitance between the gate and the bulk (i.e., $C_{OX} = \varepsilon_{ox}/t_{ox}$). Parameters $\varepsilon_{ox}$ and $t_{ox}$ are, respectively, the silicon oxide permittivity and the oxide thickness. In the linear region (i.e. in triode), the values of the parasitic capacitances seen between the gate and the source (gate-source) and between the gate and the drain (gate-drain) of the MOSFET are dominant. Due to the existing conduction channel in this region, and are given by $C_{gs} = C_{gd} = C_{Ox}/2$ [40].

In the saturation region, the value of the gate-source parasitic capacitance is dominant and is given by $C_{gs} = 2C_{Ox}/3$ due to the channel pinch-off where the values of $C_{gd}$ and $C_{ds}$ are negligible [40]. In the presented LS, the TnM dynamically controls the value of the distributed parasitic capacitance $C_p$ according to the transient value of the input pulse (IN), when it is charged by VCCS and discharged through MN2, MN3, and MN4.

When IN is high, MN2, MN3, and MN4 turn off and the current flows through the p-channel transistors (MP2 and MP4) to charge the equivalent parasitic capacitance at node A. The voltage at node $V_A$ increases until MP1 and MP2 enter the triode and then the cutoff region. Consequently, the current ‘‘1’’ decreases. Eventually, the voltage at node $V_A$ is conveyed to $V_{DDH}$ by the output buffer. The circuit operation when IN = ‘‘1’’ is illustrated in Fig. 4(b).

The produced current from MN1 must be mirrored to the TnM in the proposed topology to shift up the output voltage. However, the current flowing into MP2 and MP4 depends on the $V_{SG}$ of MP2. The gate voltage of MP2 increases when $V_A$ increases gradually, whereas the drain voltage of MP2 decreases. Accordingly, $V_{SG}$ and $V_{SD}$ of, respectively, MP2 and MP4 decreases. The dependent current of the VCCS flows into TnM, leading to the increase of $V_A$ at node A. This way, $V_{SG}$ of MP2 and $V_{SD}$ of MP4, which corresponds
to \(V_C\) (Fig. 3(c)), create a well-controlled voltage that places MP2 and MP4 in the triode region and then turn them off, preventing any extra current to be delivered to the TnM. In addition, the value of \(C_p\) decreases when MP4 goes into the triode region and then into cutoff. Consequently, the dynamic power consumption decreases, and a minimum PD can be achieved.

In contrast, MN2, MN3, and MN4 turn off when \(IN = 0\)". Consequently, the available equivalent parasitic capacitance \(C_p\) seen at node A is discharged by the path provided by MN2 and MN3, through MN4. Thus, the voltage \(V_A\) rapidly discharges to nearly zero. The circuit returns to sleep mode when MN1 is turned off. The circuit operation for \(IN = 0\)" is illustrated in Fig. 4(c).

Indeed, when \(IN = 0\), MN2, MN3, and MN4 are designed to discharge \(C_p\) rapidly, in two different directions through the various \(R_{on}\) resistances of the MOSFETs with specific care to minimize the PD and to reduce the dynamic power consumption.

When \(IN = 0\), as shown in Fig. 4 (c), the input of MN2 and MN3 is equal to \(V_{DDL}\) while the voltage at node A, which was charged at the previous state (when \(IN = 1\)) is equal to \(V_{DDH} - V_{GMP2}\). Therefore, \(V_D\) voltages of MN2 and MN3 are equal to \(V_A\). Since \(V_{DS}\) of MN3 is fixed by the \(V_{GS}\) value of MN2 (\(V_{DSM3} = V_{DDL} - V_{GSN2}\)), \(V_{DS}\) of MN2 equals to \(V_{DSM2} = V_A - V_{DSM3}\). Most of \(V_A\) drop occurs across MN2 as \(V_{DSM2}\), thus MN2 is in saturation (\(V_{DSM2} > V_{thM2}\)), while MN3 is in triode due to the low voltage drop across its drain and source (\(V_{DSM3} = V_{DDL} - V_{GSN2}\)).

At the beginning, when \(IN = 0\), MN4 is turned off and all the discharge current (Fig. 4 (c)) passes through MN2 and MN3 (\(i_{discharge1}\)). Since the discharge current is high in the beginning, the voltage drop across \(V_{DSM3}\) is \(R_{onM3} \times i_{discharge1}\). The value of \(R_{onMN3} \times i_{discharge1}\) is greater than \(V_{thM4}\). In addition, a large enough voltage drop \(V_A\) across \(V_{DS}\) of MN4 provides the condition \(V_{DSM4} > V_{thM4}\) to turn MN4 on with the help of MN3. When MN4 is turned on, a low \(R_{on}\) is added in parallel with the \(R_{on}\) of MN2 and MN3. Thus, the total \(R_{on}\) provided by the two parallel discharge paths decreases, speeding up the discharge of \(C_p\) by \(i_{discharge2}\) in parallel with \(i_{discharge1}\) (Fig. 4 (c)). Consequently, the PD and the dynamic power consumption are decreased.

### Table 1. Transistor sizes of the proposed LS in Fig. 4.

| Parts            | Components          | Values (μm) |
|------------------|---------------------|-------------|
| Input inverter   | PMOS                | W/L=1.5/0.35 |
|                  | NMOS                | W/L=1.5/0.35 |
|                  | MN1                 | W/L=10/0.35 |
|                  | MP1                 | W/L=0.4/0.35 |
|                  | MP2                 | W/L=0.4/0.35 |
|                  | MP3                 | W/L=0.4/0.35 |
|                  | MP4                 | W/L=0.4/0.35 |
|                  | MN2                 | W/L=1.5/0.35 |
|                  | MN3                 | W/L=1.5/0.35 |
|                  | MN4                 | W/L=0.4/0.35 |
| Output buffer    | PMOS                | W/L=0.4/0.35 |
|                  | NMOS                | W/L=0.4/0.35 |

### B. TnM Circuit Analysis and Equivalent Capacitor

The circuit diagram of the TnM with all its parasitic capacitances, is illustrated in Fig. 5(a). The effective equivalent parasitic capacitance \(C_p\) at node “A” is the sum of the capacitance seen from the drain of the TnM (\(C_{eq-TnM}\) in Fig. 5 (a)), the drain of MP4 (\(C_{dMP4}\)), the gate of MP2, and the input capacitances of the output buffer (\(C_{eq-Buffer}\)). Thus, the total equivalent parasitic capacitor seen at node “A” is nonlinear and depends on the region of operation of the MOSFET. Fig. 5 (b) presents the simplified circuit of the output buffer and the schematic of an inverter with its parasitic, \(C_{dMP4}\), \(C_{eq-Buffer}\), \(C_{eq-MP2}\), and \(C_{eq-TnM}\) are detailed in (1). In the \(C_{eq-TnM}\), the \(C_{MN2}\) is the seen capacitor from the source of MN2. \(C_p\) is the summation of these capacitances.

\[
\begin{align*}
C_{dMP4} &= C_{dsMP4} + C_{dgMP4} \\
C_{eq-Buffer} &= C_{gsp} + C_{gdP} + C_{gdN} + C_{gsN} \\
C_{sM2} &= C_{gsM2} + C_{gdM3} + C_{dsM3} + C_{gsM4} \\
C_{eq-TnM} &= C_{dsM4} + C_{gdM4} + C_{gsM2} \\ &\quad + (C_{dsM2} \times C_{sM2} / (C_{dsM2} + C_{sM2}))
\end{align*}
\]
\[ C_{gMP2} = C_{g1MP2} + C_{g2MP2} \]
\[ C_P = C_{eq-TnM} + C_{eq-Buffer} + C_{dMP4} + C_{gMP2} \]  
\[ (1) \]

In general, post-layout simulations are necessary to obtain an accurate estimation of the total parasitic capacitance seen at a specific node. The circuit operation can be modeled based on the expression of a capacitance charged by a current source, as shown in Fig. 5(c). In this model, the voltage across the capacitance \( C_p \) is given by (2), where \( V \) is the voltage developed across capacitor \( C_p \) during the time interval \( T \), as shown in Fig. 5(d), and \( i_{CP} \) is the current flowing through \( C_P \).

\[ V = \frac{1}{C_P} \int_0^T i_{CP} \, dt \]  
\[ (2) \]

Simulation can be performed to precisely determine the value of the equivalent parasitic capacitance at node “A” in the circuit shown in Fig. 4(a).

In the proposed circuit, the capacitance value seen at node “A” can vary because the amount of current delivered to node “A” depends on the operating region of MP2 over different time intervals. When \( V_A \) is zero, MP1 and MP2 are in their saturation regions. Therefore, the values of \( C_P \) can be obtained from

\[ I = i_{SDMP2} \mu_P C_{OX} \frac{W}{2L} \left( V_{SGMP2} - |V_{thp}| \right) ^2 (1 + \lambda V_{SDMP2}) \]
\[ = C_P \frac{dV_A}{dt} \]  
\[ (3) \]

Expression (3) is valid only at startup. Afterward, when IN changes to “1”, the gate voltage of MP2 and the drain voltage of MP4 increase gradually, forcing MP2 to enter the triode region. Therefore, “\( i_{SDMP2} \)” in (3) is substituted by

\[ i_{SDMP2} = \mu_P C_{OX} \frac{W}{L} \left( (V_{SGMP2} - |V_{thp}|) V_{SDMP2} \right) - 0.5(V_{SDMP2})^2 \left( 1 + \lambda V_{SDMP2} \right) \]  
\[ (4) \]

Finally, MP2 enters the cutoff region, “\( i_{SDMP2} = 0 \)”, and the circuit shuts down when \( V_A \) further increases.

When \( IN = “1” \), the current delivered to the TnM by MP2 and MP4 follows three steps. In the beginning, the current is modeled by the equation of the drain current of MP2 when it is in the saturation region. Then, the current is modeled by the equation of the drain current of MP2 when it is in the linear region. Finally, the delivered current is equal to zero in the cutoff region of MP2. When \( IN = “0” \), MN2, MN3, and MN4 are activated to discharge the voltage of \( V_A \) through three steps corresponding to the operating regions of MN2, MN3, and MN4 (see a detailed description in the last paragraph of Section III A). During both transition times, when \( IN = “0” \) or \( IN = “1” \), MP2, MP4, and MN2-MN4 work through the three different regions in a short permitted operating time. In these three regions, the current delivered to the TnM first follows a second order equation as in (3), then a first order equation as in (4) follows, and finally \( I = 0 \), i.e. cut-off. Consequently, the current flowing through the TnM is a Gaussian waveform [43]:

\[ I_{TnM}(t) = \frac{1}{\sigma \sqrt{2\pi}} e^{-\frac{(t-t_0)^2}{2\sigma^2}} \]  
\[ (5) \]

where \( \sigma \) is standard deviation, \( m \) is mean value, and \( t \) represents the time. The amplitude of the current equals \( 1/\sigma \sqrt{2} \), and the operating time of the circuit equals approximately \( m/2 \). The LS circuit operation during the transition times and the transfer function of the output buffer are analyzed to derive the PD formula. \( V_O \) as a function of \( V_A \) (input of buffer voltage) is plotted in Fig. 5(e). In this voltage transfer characteristic, \( V_M \) is the switching threshold. Thus, the output of the presented LS changes when \( V_A \) reaches \( V_M \). Therefore, when \( IN = “1” \), to extract the rising PD \( (t_{pr}) \) from (2), we replace \( i_{CP}(t) \) by \( I_{TnM}(t) \) that is described by (5). In this way, (2) can be rearranged as follows where \( V = V_A \).

\[ V_A = \frac{1}{C_P} \int_0^T \frac{1}{\sigma \sqrt{2\pi}} e^{-\frac{(t-t_0)^2}{2\sigma^2}} \, dt \]  
\[ (6) \]
The proposed LS is allowed to work only during the PD; therefore, the integral bounds of (6) are from \( t_0 \) to \( t_0 + t_{pr} \), where \( t_0 \) indicates the exact start time of the LS input signal (IN) going up and \( t_0 + t_{pr} \) indicates the moment that \( V_A \) reaches \( V_M \). Thus, replacing \( V_A \) by \( V_M \) in (6) and evaluating this integral over the rising PD \( t_{pr} \) yields

\[
V_A = V_M = \frac{1}{C_P} \int_{t_0}^{t_0 + t_{pr}} \frac{1}{\sigma \sqrt{2\pi}} e^{-\frac{(t-t_0)^2}{2\sigma^2}} (t) \, dt
\]  
(7)

Which can be approximated using Simpson’s rule

\[
V_M = \frac{1}{C_P} \frac{(t_0 + t_{pr}) - t_0}{6} \left[ I_{ThM}(t_0) + 4I_{ThM} \left( \frac{2t_0 + t_{pr}}{2} \right) + I_{ThM}(t_0 + t_{pr}) \right]
\]  
(8)

Replacing \( dt \) by a time interval \( \Delta t \) in (3) yields

\[
\Delta t \cdot i_{SDMP2} = C_P \cdot \Delta V_A
\]  
(9)

where \( \Delta V_A \) is the variation of \( V_A \) over the time interval \( \Delta t \). The value of \( C_P \) is determined by

\[
C_P = \frac{\Delta t \cdot i_{SDMP2}}{\Delta V_A}
\]  
(10)

In (10), the value of \( i_{SDMP2} \) depends on the region of operation of MP2. \( i_{SDMP2} \) can be calculated using (3) when MP2 is in saturation and using (4) when it is in the triode region. The PD \( (t_p) \) is then derived as follows

\[
t_{pr} = \frac{6C_P V_M}{I_{ThM}(t_0) + 4I_{ThM} \left( \frac{2t_0 + t_{pr}}{2} \right) + I_{ThM}(t_0 + t_{pr})}
\]  
(11)

when IN goes down, MN1 is turned off and \( C_P \), which was charged at the previous step when IN = “1” starts to discharge through MN2, MN3, and MN4. Fig. 6 shows the equivalent circuit of the presented LS when IN = “0”. In this case, to extract the falling PD \( (t_{pf}) \), the equation of the discharging capacitor must be used. Based on Fig. 6,

\[
V_{C_P}(t) = V_A \cdot e^{-t/t_{pf}}
\]  
(12)

where \( R_{onT} \) equals \((R_{on2}+R_{on3})||R_{on4}(\text{Fig. 6}) \) and \( C_P \) is described by (10), while \( i_{SDMP2} \) is a discharging current, as illustrated in Fig. 6.

\[
C_P = \frac{\Delta t \cdot (i_{\text{discharge1}} + i_{\text{discharge2}})}{\Delta V_A}
\]  
(13)

In (12), the falling PD of \( t_{pf} \) equals the time interval between the input signal (IN), when it goes down, and the moment that \( V_{C_p}(t) \) decreases to reach \( V_M \). Therefore, by replacing \( V_{C_p}(t) \) with \( V_M \) in (12), \( t_{pf} \) is estimated by

\[
V_{C_P}(t) = V_M \Rightarrow e^{-t/t_{pf}} = \frac{V_M}{V_A} \Rightarrow -t_{pf} = R_{onT} \cdot C_P \cdot ln \left( \frac{V_M}{V_A} \right) \Rightarrow t_{pf}
\]

Finally, the PD is estimated by the average of \( t_{pr} \) and \( t_{pf} \) as follows

\[
t_p = \frac{t_{pr} + t_{pf}}{2}
\]  
(15)

C. SIMULATED PERFORMANCE

The simulation results of the proposed LS are shown in Fig. 7. It shows the input voltage of 0.6 V, the current “1” flowing through the TnM, the \( V_A \), which is gradually increasing, and the output voltage of 3.0 V with an operating frequency of 1 MHz. In the inset of Fig. 7, the PD of the rising edge is 1.99 ns. The current flows in the TnM only during a limited time interval within the PD, provides the current \( I \) with a Gaussian waveform (Fig. 7), which is an energy-optimal waveform [44], [45]. The figure also shows \( V_A \), which is controlled by the feedback network, increasing smoothly. The peak current flowing inside the TnM during the rising edge of the input/output pulses duration, is limited to 8.5 \( \mu \)A. The current in the rising edge is reduced by half due to the utilization of the feedback network, which minimizes any contention and speeds up the operation of the circuit, as shown by the limited duration of this current waveform.

Figs. 8 (a) and (b) show the simulated \( C_P \) and voltage \( V_A \) during the, respectively, rising and falling transitions in which, the LS circuit is permitted to work. In Fig. 8 (a), \( V_A \) is close to zero in the beginning placing MP2 and MP4 in the saturation region. At the same time, \( C_P \) exhibits its highest parasitic capacitance. When \( V_A \) gradually increases, the MP2 and MP4 go into the triode region which decreases the parasitic capacitance at node A. It should be noted that the gate-source / gate-drain parasitic capacitances of a MOSFET are dominant (other parasitic capacitances are negligible) and are given by \( C_{gs} = C_{gd} = C_O/2 \) in the triode region, and by \( C_{gs} = 2 \cdot C_O/3 \) in saturation, where \( C_O \) is the total gate capacitance of the MOSFET [40]. Thus, \( C_P \) follows a descending curve when the \( V_A \) increases when IN = “1”. As shown in Fig. 8 (a), \( C_P \) can vary from 30 fF to 7 fF when \( V_A \) increases from 0 V to 1.3 V.

Fig. 8 (b) shows the simulated \( C_P \) and \( V_A \) when IN goes down. In this case, the voltage \( V_A \) is around 1.35 V.
in the beginning assuming it was previously charged, the gate voltages of MN2 and MN3 are equal to $V_{DDL}$, which turns them on. As shown in Fig. 6, the TnM creates two different branches between $V_A$ and ground for discharging $C_p$ when $IN = "0"$, 1) through MN4, and 2) through MN2 and MN3 in series. In the beginning, $V_A$ is large placing MN4 and MN2 in the saturation region and thus significantly increasing the parasitic capacitance at node A. At this time, $C_p$ can be as high as 32 fF according to the simulation (Fig. 8 (b)). When $V_A$ decreases, the voltage across the TnM decreases, and consequently, MN4 and MN2 go into the triode region, decreasing the parasitic capacitance at node A. Then, when $IN = "0"$ and $V_A$ starts decreasing, $C_p$ decreases as shown in Fig. 8 (b). The value of $C_p$ varies from 32 fF to 5 fF when $V_A$ decreases from 1.4 V to 0.2 V for $IN = "0"$.

We compare the LS operation with a single transistor (Fig. 5 (f)) instead of using the TnM. Fig. 9 presents an input voltage of 0.6 V, a flowed current "$I"$ through a single transistor (replacing the TnM), a $V_A$ gradually increasing, and the output voltage of 3.0 V with an operating frequency of 1 MHz. In the inset of Fig. 9, the PD of the rising edge is 3.18 ns. In this setting, the simulated PD was 1.6 times longer than with the proposed LS circuit, which is using the TnM. The amplitude of the current is $I = 11 \, \mu A$, compared to $I = 8.5 \, \mu A$ when the TnM was used. To elaborate, when a single transistor is used instead of the TnM, the low side of the presented LS design (Fig. 4 (a)) performs like a conventional LS circuit (Fig. 1) that suffers from contention. Consequently, the power consumption and the PD of this LS increase compared to our solution, as simulated, and shown in Fig. 9. Figs. 10 (a) and (b) show the simulated $C_p$ and voltage $V_A$ during the, respectively, rising and the falling transitions in which the LS circuit (using a single transistor instead of the TnM) is permitted to work. In Fig. 10 (a), the input of the single transistor (used instead of the TnM) is "$0"$ and the single transistor is turned off. So, the variation of $C_p$ in node A depends on the parasitic capacitances of MP2 and MP4 (Fig. 4 (a)) where $C_p$ varies from 35 fF to 7 fF during the transition of the LS output from "$0"$ to "$1"$. During this transition, $V_A$ varies from 0.2 V to 1.5 V. When $IN = "1"$ the operation of the LS is independent of the parasitic capacitance of the low side of the LS. Therefore, the variation of $C_p$ and $V_A$ in Fig. 10 (a) and Fig. 8 (a) are the same.

Fig 10 (b) illustrates the simulated $C_p$ and $V_A$ when IN goes low. In this case, the input of the LS, which is using a single transistor rather than the TnM, is "$1"$ and the single transistor is turned on. Since $V_A$ has reached its maximum voltage after the previous step (IN = "$1"), it places MP2 and MP4 in their cutoff region. Therefore, $C_p$ depends on...
Figure 10. Simulated Cp and voltage of V_A when a single transistor is used instead of the TnM during the (a) rising (IN = "1") and (b) the falling.

The parasitic of a single transistor and is independent of the parasitic of MP2 and MP4. When V_A becomes large, the single transistor (i.e., MN2 in Fig. 1) is put in the saturation region, significantly increasing the parasitic capacitance at node A. At this time, C_p can be as high as 150 fF according to the simulation (Fig. 10 (b)). When V_A decreases, the voltage across the single transistor decreases, and consequently, the single transistor goes into the triode region, which decreases the parasitic capacitance at node A.

Then, when IN = “0” and V_A starts decreasing, C_p decreases as shown in Fig. 10 (b). The value of C_p varies from 150 fF to 5 fF when V_A decreases from 2.4 V to 1 V for IN = “0”. Comparing Fig. 10 (b) with the Fig. 8 (b), the equivalent parasitic capacitance at node A of the LS with the single transistor is greater than with the TnM, due to the generated contention in this node, which consequently increases the PD. When the PD increases, the voltage of V_A reaches V_M, showing that the variation of V_A (dV_A/dt) is slow.

The equivalent capacitance at node A is, therefore, large (C_p = I_{MP}/(dV_A/dt)), as shown in Fig. 10 (b).

Validating the operation of the proposed design against mismatch and process corners is critical because the current delivered to the TnM is closely related to V_{SG} and V_{SD} of MP2 and MP4. MP2 and MP4 shown in Fig. 4(a) are responsible for adjusting the current delivered to the TnM; hence, they must be designed and implemented to be resilient against process variations. The design is simulated for the typical case corner using typical NMOS and PMOS transistor parameters, V_{DDH} = 3 V, V_{DDL} = 1.6 V, capacitive load (C_L) = 100 fF, and an operating frequency of 1 MHz. The simulation yields a value of the PD (average of rising and falling PD) of 7.86 ns for the proposed LS. A worst-case simulation is performed to assess the effects of process variations. In the AMS design kit, “worst power” (WP) means “fast NMOS/fast PMOS” whereas, “worst speed” (WS) means “slow NMOS/slow PMOS”. The WP and WS represent the worst operating conditions due to process variations. The simulated values of the PD for the WP and WS cases are, respectively, 6.46 and 12.41 ns.

The WS case has the longest delay, while the WP yields the shortest delay. A Monte-Carlo simulation is performed for V_{DDH} = 3 V, V_{DDL} = 1.6 V, capacitive load (C_L) = 100 fF, and an operating frequency of 1 MHz to further examine the influence of process variations on the operation of the presented LS. The resulting PD and its log-normal distribution exhibiting variance of 0.105, mean PD (mu) of 7.92 ns, and standard deviation (sd) of 0.839 ns, are
The power consumption of the LS is also assessed to validate the operation of the proposed circuit against mismatch and process corners. The design is simulated for the typical case corner using typical NMOS and PMOS transistor parameters, \( V_{DDH} = 3 \text{ V}, V_{DDL} = 0.8 \text{ V}, \) capacitive load \((C_L) = 100 \text{ fF}, \) and an operating frequency of 1 kHz. The simulation yields a total power consumption of 1.89 nW for the proposed LS. A worst-case simulation is performed to assess the effects of process variations on power consumption. The simulated values of the power consumption for the WP and WS cases are, respectively, 12.16 and 1.56 nW. A Monte-Carlo simulation is performed for \( V_{DDH} = 3.0 \text{ V}, V_{DDL} = 0.8 \text{ V}, \) capacitive load \((C_L) = 100 \text{ fF}, \) and an operating frequency of 1 kHz to further examine the influence of process variations on the operation of the proposed LS. The resulting power consumption and its log-normal distribution of variance of 0.6, mean power consumption \((\mu)\) of 2.72 nW, and standard deviation \((\sigma)\) of 1.63 nW are presented in Fig. 11 (b).

**IV. EXPERIMENTAL RESULTS**

Fig. 12 shows the test setup used to perform the experimental validation of the fabricated LS circuit. As shown in the block diagram of Fig. 12 (a), a capacitive load is used to perform the measurement. A source measurement unit (SMU) with a resolution of 10 fA (KEYSIGHT-B2911A) is utilized to accurately measure the power consumption. Fig. 12 (b) shows the test equipment and the fabricated chip under test mounted on a custom printed circuit board (PCB). Fig. 12 (c) presents the enlarged view of one 10-pF capacitive load for the test. Fig. 12 (d) shows the screenshot of the oscilloscope and the measured input and output waveforms of the fabricated LS in parallel with amplitudes of 0.8V and 3.0 V, respectively. Fig. 12 (e) shows the enlarged view of the wire-bonded fabricated chip.

The presented LS circuit was fabricated in an AMS 0.35-\(\mu\)m CMOS process. A photograph of the fabricated chip prototype is shown in Fig. 13 (a). The fabricated LS occupies an area of \(25 \times 25 \mu \text{m}^2\). The performance of the fabricated LS is measured over a wide range of frequencies. The maximum operating frequency of the circuit is shown for different input signal amplitudes while \(V_{DDL}\) changes from 0.4 V to 2 V and \(V_{DDH} = 3 \text{ V}.\) The proposed LS successfully works up to 130 MHz (at \(V_{DDL} = 1.6 \text{ V}\)) as shown in Fig. 13 (b), while similar LS circuits are limited to 100 MHz, like in [37].
The total power consumption is another important parameter that must be considered. The measured power consumption of the fabricated LS circuit is presented in Fig. 14 (a) as a function of the frequency of the input pulse. Power consumption is measured experimentally for input signal amplitudes and VDDL of 0.6, 0.7, 0.8, 1.0, 1.4, and 1.8 V, a fixed VDDH = 3.0 V, and a capacitive load CL = 20 pF. The consumed power increases with the frequency of the input pulse. Except for the input inverter, which is supplied by VDDL, the other parts of the proposed LS circuit are supplied by VDDH, as shown in Fig. 4(a), and they consume the bulk of the power. VDDL is only connected to the input inverter that consumes a negligible amount of power. Accordingly, the measured power consumption shown in Fig. 14 (a) is the result of the product of VDDH and the current drained from VDDH measured by the SMU. Among the six measured curves, the highest power consumption variation occurs when the circuit converts the input signal with the lowest amplitude into 3 V (from 0.6 V to 3 V). While the lowest power consumption variation is obtained when the circuit converts the input signal with the highest amplitude into 3 V (from 1.8 V to 3 V). The circuit needs more power to provide a higher conversion gain. Since in all six measured curves presented in Fig. 14 (a) VDDH is fixed, the variation of the measured consumed power versus VDDL are close to each other.

The variation in power as a function of the input frequency over several values of VDDH (1.8, 2.0, 2.2, 2.4, 2.6, 2.8, and 3 V) is shown in Fig. 14 (b). The results are obtained for a fixed VDDL and a capacitive load CL = 20 pF. In this set of measured curves, the power consumption also increases with the frequency. Here, the highest measured power occurs at VDDH = 3 V while the lowest one is observed at VDDH = 1.8 V.

The measured consumed power variation of the LS circuit is presented in Fig. 14 (c) for different values of VDDL at VDDH = 3.0 V, capacitive load CL = 20 pF, and an operating frequency of 1 kHz. In this descending curve, when VDDL increases (i.e. the amplitude of the input signal increases), the implemented LS requires a lower amount of energy to convert the input signal to a signal with an amplitude of 3 V, because VDDH is fixed at 3 V. The total power consumption of the LS circuit versus VDDL for a fixed VDDL = 0.8 V, capacitive load CL = 20 pF, and an operating frequency of 1 kHz, is shown in Fig. 14 (d). The measured power consumption that is within a range of a few nW, increases with VDDL.

The static power consumption (PS) of the proposed LS circuit is measured for different input signal values. The PS measured for these DC input values, without applying any input pulse, is within a few pW. When the input of the LS is connected to GND ("0") or VDDL ("1"), the measured PS are, respectively, 31.5 and 260 pW. The power consumption...
versus capacitive load (C_L) at 1 kHz pulse shaped input, V_DD = 0.8 V, and V_DDH = 3 V is measured and presented in Fig. 15. In this measurement, C_L is changed from 0.1 pF to 100 nF and the power is measured at each step. As C_L increases, the power consumption increases.

The PD of the LS circuit is measured for an input pulse signal with a frequency of 1 MHz and a duty cycle of 50% while an inverter, integrated on the chip, is used as a load. As shown in Fig. 16 (a), the LS shows a rising PD of 4 ns and a falling PD of 11.2 ns (see Fig. 16 (b)). Thus, the average PD of the proposed LS after a transition is 7.6 ns.

Given that the PD is an essential parameter of any LS circuit, Figs. 16 (c) and (d) are provided to show the variation of the PD versus the voltage variation in VDDL and VDDH. The rising and falling PDs versus VDDL at a fixed VDDH = 3 V, and while using an integrated inverter as load, are presented in Fig. 16 (c). The PD, especially the rising edge delay for VDDL < 0.8 V, is long because of the larger conversion gain of the circuit when it is converting a low-amplitude signal into a high-amplitude signal of 3 V. The measured delay variation curve, especially the falling PD, is almost flat for VDDL > 0.8 V. The measured variations of the rising and falling PDs versus VDDH at fixed VDDL = 1.6 V, while an integrated inverter is used as load, are shown in Fig. 16 (d). In this figure, the PD is measured when the LS converts a pulse shaped signal with a 1.6 V amplitude into 3 V. In Fig. 16 (d), the PD of the circuit is almost flat, especially the rising PD, which shows that the circuit provides good performance at lower conversion gain (converting 1.6 to 3 V).

Designing circuits to work in subthreshold is essential for low-power budget applications, such as in biomedical implants [40], [46], [47], [48]. The results in Fig. 17 show that the operation of the circuit in subthreshold meets the requirements of high-performance operation due to the TnM and feedback network of the proposed LS (Fig. 4 (a)). Fig. 17 presents the measured waveforms of the implemented LS for an 80 mV and 50 kHz input pulse converted into a

**FIGURE 16.** Measured PD when an integrated inverter is used as load: (a) Rising edge at the output for a 1-MHz input pulse with an amplitude of 0.8V, and V_DDH = 3.0V (b) Falling edge at the output for a 1-MHz input pulse with amplitude of 0.8V, and V_DDH = 3.0V (c) Variation of rising and falling PD versus VDDL at V_DDH = 3.0 V, and (d) Variation of rising and falling PD versus V_DDH at VDDL = 1.6 V.
TABLE 2. Performance summary and comparison with other solutions.

| References | Range (V) | CMOS Process (nm) | Delay (ns) (@VDDL(V), fA(MHz)) | Ec (J) (@VDDL(V), fA(MHz)) | VDDL (V) | Pd (pW) | FoM1 (V/ns) | FoM2 (nW ns) | Res. |
|------------|-----------|-------------------|---------------------------------|-----------------------------|----------|---------|------------|-------------|------|
| [9], TVLSI’17 | 0.20-1.10 | 40                | 11.57 (@0.4, 1.0)             | 67.4f (@0.4, 1.0)          | 1.1      | 90.1    | 0.060      | 103         | Sim. |
| [34], TVLSI'15 | 0.10-1.0 | 90               | 16.60 (@0.2, 1.0)            | 77.0f (@0.2, 1.0)          | 1.0      | 8700    | 0.048      | 51.1        | Sim. |
| [35], TCAS-F17 | 0.33-1.80 | 180              | 29.0 (@0.4, 0.50)            | 61.5f (@0.4, 0.500)        | 1.8      | 330     | 0.048      | 44.0        | Meas.|
| [36], JSSC’21 | 0.32-1.20 | 14               | 8.30 (@0.5, 1.0)             | 0.1p (@0.8, 1.0)           | 1.2      | ---     | 0.064      | 230         | Meas.|
| [37], JSSC’12 | 0.40-3.0  | 350              | 15.0 (@0.8, 0.01)            | 5.8p (@0.4, 0.010)         | 3.0      | 230     | 0.146      | 30.9        | Meas.|
| [38], TVLSI’16 | 0.40-1.80 | 180              | 30.0 (@0.4, 1.0)             | 150.0f (@0.4, 1.0)         | 1.8      | 300     | 0.026      | 222         | Sim. |
| [47], Access’20 | 0.1-3.0   | 180-HV           | 14.37 (@0.4, 1.0)            | 84.32p (@0.4, 1.0)         | 3.0      | 2760    | 0.180      | 21.43       | Sim. |
| [48], Access’21 | 0.3-1.8   | 45nm             | 52.7 (@0.3, 1.0)             | 34.6p (@0.3, 1.0)          | 1.8      | ---     | 0.113      | 50.65       | Sim. |
| This work   | 0.08-3.0  | 350              | 7.60 (@0.1, 1.0)             | 3.4p (@0.8, 0.001)         | 3.0      | 31.5    | 0.184      | 3.67        | Meas.|

1Ec: Energy consumption; 2Pd: Static power consumption; FoM1=Range/delay.

3.0 V waveform. As can be seen, a clean 3 V pulse is extracted at the output of the presented LS circuit from a ultra-low amplitude input pulse. Therefore, the proposed LS provides a convenient interface between a weak signal and a digital processor.

V. DISCUSSION AND PERFORMANCE COMPARISON

The achieved experimental validation revealed that the utilization of the TnM remarkably improves the performance of the proposed LS. The TnM relies on the equivalent parasitic capacitances of the MOSFET utilized in the LS circuit. The feedback network prevents the LS circuit from consuming a large amount of power during the transitions. This minimizes the PD, enables operation in subthreshold, and minimizes static and dynamic power consumption. Table 2 summarizes and compares the performance of the presented LS circuit to other solutions. The experimental results show an improvement of approximately 8.5% of the PD as compared to [36], which uses a current mirror-based LS. In addition, the proposed circuit can successfully convert a pulse signal over a wide range of conversion (0.08-3 V) and with an amplitude as small as 80 mV into 3 V while working in subthreshold and consuming only 28 nW. Moreover, the measured maximum operating frequency of the fabricated circuit improved by 30% as compared to the other solutions. The static and dynamic power consumption is comparable with those of the recently published papers in this field. A reasonable criterion in the performance evaluation of a LS design is to measure the PD while the circuit is working over a given conversion range. Indeed, a larger conversion range results in longer PD. Therefore, a figure-of-merit (FoM1) is recommended to assess the performance of the PD over the conversion range. In our proposed LS, the PD of 7.6 ns is measured while the LS was converting a pulse with an amplitude of 1.6 V to a pulse with an amplitude of 3 V. Thus, a FoM1 = (3.0-1.6)/7.6 ns = 0.184 × 109 is achieved. With this FoM1, a larger value is the better. A second FoM2 is defined to compare the different LS designs together according to the trade-off between the power consumption (PC) and the PD (Delay). It is beneficial that a LS achieves the lowest PC for the shorter delay, while converting VDDL as low as possible. Therefore, in the defined FoM2, the VDDL, PC, and Delay appear at the numerator. Thus, a LS providing a smaller FoM2 would achieve a better performance. To facilitate comparison, FoM2 is normalized according to the VDDL employed in each circuit. The product of parameters PC and Delay is divided by the square of VDDL. As it can be seen in Table 2, our LS design has the lowest FoM2 of 3.67, suggesting that our design outperforms other solutions in terms of trade-off power consumption vs PD for a given VDDL.
VI. CONCLUSION

A new high-performance LS circuit topology is presented in this work. The presented current mirror-based structure offers a wide-range and fast LS conversion. Our design can convert subthreshold input signal levels to above-threshold levels with minimum PDs, leveraging the dynamic equivalent parasitic capacitance value of the TnM, which depends on the value of the transient input signal IN. The operation of the proposed circuit is efficient, especially in the case of contention on high-impedance nodes, owing to the utilization of a feedback network and a voltage controlled source (VCCS). An equivalent parasitic capacitance of three interconnected n-type MOSFETs (TnM) circuit is used to perform the level-shifting part of the LS in addition to forming two discharge paths for a Cp when IN = "0". The advantageous effect of this TnM minimizes the PD and dynamic power consumption. In addition, this approach enhances the conversion range as compared to the other mechanism. The measured performance of the test chip fabricated in a 0.35 μm AMS design process outperforms other compared solutions. The discussion and the measured performance of the presented LS illustrated the numerous advantages of this solution, namely wide conversion range, low power consumption, and short PD.

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REFERENCES

[1] G. Gagnon-Tarcotte, G. Bilodeau, O. Tsiakaka, and B. Gosselin, “Smart autonomous electro-optic platforms enabling innovative brain therapies,” IEEE Circuits Syst. Mag., vol. 20, no. 4, pp. 28–46, 4th Quart., 2020.
[2] M. Karimi, M. Ali, A. Hassan, M. Sawan, and B. Gosselin, “An active dead-time control circuit with timing elements for a 45-V input 1-MHz halfbridge converter,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 69, no. 1, pp. 30–41, Jan. 2022.
[3] M. Ali, A. Hassan, M. Honarparvar, M. Nabavi, Y. Audet, M. Sawan, and Y. Savaria, “A versatile SoCISP sensor interface for industrial applications: Implementation challenges,” IEEE Access, vol. 10, pp. 24540–24555, 2020.
[4] T. Datta-Chaudhuri, E. Smela, and P. A. Abshire, “System-on-chip considerations for heterogeneous integration of CMOS and fluidic bio-interfaces,” IEEE Trans. Biomed. Circuits Syst., vol. 10, no. 6, pp. 1129–1142, Dec. 2016.
[5] M. Fuzollahi, M. Karimi, and A. M. Sodagar, “A low-power generic biostimulator with arbitrary pulse shape based on a central control core,” IEEE Electron. Exp., vol. 30, no. 7, pp. 3964–3975, Jul. 2015.
[6] K. Keramatzadeh, A. Kiokojouri, M. S. Nahvi, Y. Khazaei, A. Feizi-Nejad, M. H. Maghami, R. Mohammadi, S. Nasiri, F. A. Boroumand, E. Namidi, M. Rezaei, A. Shojaei, J. Mirajafari-Zadeh, and A. M. Sodagar, “Wireless, miniaturized, semi-implantable electrocorticography microsystem validated in vivo,” Sci. Rep., vol. 10, no. 1, pp. 1–13, Dec. 2020.
[7] M. Karimi, M. Ali, A. Hassan, G. Weber-boisvert, A. Abuelnour, M. Sawan, and B. Gosselin, “A 1.99-ns 0.5-pJ wide frequency range level shifter with closed-loop negative feedback,” in Proc. 18th IEEE Int. New Circuits Syst. Conf. (NEWCAS), Jun. 2020, pp. 174–177.
[8] V. K. Lazarjan, A. B. Gashiti, M. Feshki, A. Garnier, and B. Gosselin, “Miniature fiber-spectrophotometer for real-time biomarkers detection,” IEEE Sensors J., vol. 21, no. 13, pp. 14822–14837, Jul. 2021.
[9] Z. Yong, X. Xiang, C. Chen, and J. Meng, “An energy-efficient and wide-range voltage level shifter with dual current mirror,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 25, no. 12, pp. 3534–3543, Dec. 2017.
[10] E. D. Manolov, “Design of CMOS analog circuits in subthreshold region of operation,” in Proc. IEEE 27th Int. Sci. Conf. Electron., Sep. 2018, pp. 1–4.
[11] C.-Y. Lu, C.-T. Chuang, S.-J. Jou, M.-H. Tu, Y.-P. Wu, C.-F. Huang, P.-C. Kan, H.-S. Huang, K.-D. Lee, and Y.-S. Kuo, “A 0.325 V, 600-kHz, 40-nm 72-kb 9T subthreshold SRAM with aligned boosted write wordline and negative write bitline write-assist,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 23, no. 5, pp. 958–962, May 2015.
[12] R. A. Robles and T. Harada, “A 0.6 V programmable frequency divider and digitally controlled oscillator for use in a digital PLL in the subthreshold region,” in Proc. 27th IEEE Int. Conf. Electron. Circuits Syst. (ICECS), Nov. 2020, pp. 1–4.
[13] A. Hasanbegovic and S. Aunet, “Low-power subthreshold to above threshold level shifter in 90 nm process,” in Proc. NORCHIP, Nov. 2009, pp. 1–4.
[14] N. Juteau and B. Gosselin, “Wearable wireless-enabled osimetric sphymnograph: A flexible ambulatory tool for blood pressure estimation,” IEEE Trans. Biomed. Circuits Syst., vol. 14, no. 6, pp. 1287–1298, Dec. 2020.
[15] M. Karimi, H. Jouaicha, F. Lelouche, P.-A. Bouchard, M. Sawan, and B. Gosselin, “6.78-MHz robust WPT system with inductive link bandwidth extended for cm-sized implantable medical devices,” in Proc. 42nd Annu. Int. Conf. IEEE Eng. Med. Biol. Sci. (EMBC), Jul. 2020, pp. 4196–4199.
[16] S. A. Mirbozorgi, E. Maghsoudloo, H. Bahrami, M. Sawan, and B. Gosselin, “Multi-resonator arrays for smart wireless power distribution: Comparison with experimental assessment,” IET Power Electron., vol. 13, no. 18, pp. 4183–4193, Dec. 2020.
[17] Y.-J. Huang, T.-H. Tzeng, T.-W. Lin, C.-W. Huang, P.-W. Yen, P.-H. Kuo, C.-T. Lin, and S.-S. Lu, “A self-powered CMOS reconfigurable multi-sensor SoC for biomedical applications,” IEEE J. Solid-State Circuits, vol. 49, no. 4, pp. 851–866, Apr. 2014.
[18] M. Karimi, M. Ali, M. Nabavi, A. Hassan, M. Amer, M. Sawan, and B. Gosselin, “A versatile non-overlapping signal generator for efficient power-converters operation,” in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), Oct. 2020, pp. 1–5.
[19] A. Dyck, M. Rosch, A. Tessmann, A. Lehther, M. Kuri, S. Wagner, B. Gashi, J. Schafer, and O. Ambacher, “A transmitter system-in-package at 300 GHz with an off-chip antenna and GaAs-based MIMCs,” IEEE Trans. Terahertz Sci. Technol., vol. 9, no. 3, pp. 335–344, May 2019.
[20] H.-R. Zhu, J.-B. Wang, Y.-F. Sun, X.-L. Wu, and J.-F. Mao, “A novel automatically designed EBG structure by improved GA for ultrawideband SSN mitigation of system in package,” IEEE Trans. Compon., Packag., Manuf. Technol., vol. 10, no. 1, pp. 123–133, Jan. 2020.
[21] K. Xu, B. Vaisband, G. Sizikov, X. Li, and E. G. Friedman, “Power noise and near-field EMI of high-current system-in-package with VR top and bottom placements,” IEEE Trans. Compon., Packag., Manuf. Technol., vol. 9, no. 4, pp. 712–718, Apr. 2019.
[22] J. Chang, Y.-H. Chen, G. Chan, H. Cheng, P.-S. Wang, Y. Lin, H. Fujiwara, R. Lee, H.-J. Liao, P.-W. Wang, G. Yeap, and Q. Li, “A 5 nm 135 Mb SRAM in EUV and high-mobility-channel FinFET technology with metal coupling and charge-sharing write-assist circuitry schemes for high-density and low-VMIN applications,” in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2020, pp. 238–240.
[23] J. Gao, K. Nair, N. Cao, D. Plass, E. Nelson, C. Hwang, G. Yeap, and Q. Li, “A 5 nm 135 Mbit DRAM macro for the POWER™ processor 32 MByte on-chip cache,” in Proc. IEEE Int. Solid State Circuits Conf. (ISSCC), Feb. 2020, pp. 1–5.
[24] B. Gosselin, “Multi-resonator arrays for smart wireless power distribution,” in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), Oct. 2020, pp. 1–5.
[25] M. Karimi, M. Ali, M. Nabavi, A. Hassan, M. Amer, M. Sawan, and B. Gosselin, “A versatile non-overlapping signal generator for efficient power-converters operation,” in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), May 2020.
[26] A. Hasanbegovic and S. Aunet, “Low-power subthreshold to above threshold level shifter in 90 nm process,” in Proc. NORCHIP, Nov. 2009, pp. 1–4.
[27] J.-S. Park, J.-W. Jung, H. Lee, D. Lee, S. Lee, H. Jung, S. Lee, S. Kwon, K. Jeong, J.-H. Song, S. Lim, and I. Kang, “A 6 K-MAC feature-map-sparsity-aware neural processing unit in 5 nm flagship mobile SoC,” in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2021, pp. 152–154.

[28] T. S. Kim, S. Lee, K. Lee, S. Shin, S. Jun, Y. Lee, S. Lee, H. Kang, C. Yim, Y. Lim, E. Moon, S. Lim, K. Jeong, and I. Kang, “An area and energy efficient 0.12 nJ/pixel 8 K 30 fps AV1 video decoder in 5 nm CMOS process,” in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2021, pp. 68–70.

[29] Q. Cai, Y. Ji, C. Ma, X. Li, T. Zhou, J. Zhao, and Y. Li, “An ultra-low-voltage energy-efficient dynamic fully-regenerative latch-based level-shift circuit with tunnel-PET & FinFET devices,” in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), May 2021, pp. 1–5.

[30] S.-C. Luo, C.-J. Huang, and Y.-H. Chu, “A wide-range level shifter using a modified Wilson current mirror hybrid buffer,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 61, no. 6, pp. 1656–1665, Jun. 2014.

[31] A. P. Chavan, “Ultra-low power, area efficient and high-speed voltage level shifter based on Wilson current mirror,” in Proc. IEEE Mysore Sub Sect. Int. Conf. (MysuruCon), Oct. 2021, pp. 109–113.

[32] K. Luo and J. Xiao, “A high-voltage dynamic level shifter with current mirror and augmented cross-coupling structure for high-side NMOS gate driver,” in Proc. IEEE 3rd Int. Conf. Electron. Technol. (ICTET), May 2020, pp. 330–333.

[33] S. Lütkeemeier and U. Ruckert, “A subthreshold to above-threshold level shifter comprising a Wilson current mirror,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 67, no. 12, pp. 321–325, Dec. 2020.

[34] M. Lanuzza, P. Corsonello, and S. Perri, “Fast and wide voltage conversion in multisupply voltage designs,” IEEE Trans. Very Large Scale Integ. (VLSI) Syst., vol. 23, no. 2, pp. 388–391, Feb. 2015.

[35] E. Maghsoudloo, M. Rezaei, M. Sawan, and B. Gosselin, “A high-speed and ultra-low-power subthreshold signal level shifter,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 64, no. 5, pp. 1164–1172, May 2017.

[36] H. Jeong, T.-H. Kim, C. N. Park, H. Kim, T. Song, and S.-O. Jung, “A wide-range static current-free current-mirror-based LS with logic error detection for near-threshold operation,” IEEE J. Solid-State Circuits, vol. 56, no. 2, pp. 554–565, Feb. 2021.

[37] Y. Osaki, T. Hirose, N. Kuroki, and M. Numa, “A low-power level shifter with logic error correction for extremely low-voltage digital CMOS LSIs,” IEEE J. Solid-State Circuits, vol. 47, no. 7, pp. 1776–1783, Jul. 2012.

[38] S. R. Hosseini, M. Saberi, and R. Lotfi, “A high-speed and power-efficient voltage level shifter for dual-supply applications,” IEEE Trans. Very Large Scale Integ. (VLSI) Syst., vol. 25, no. 3, pp. 1154–1158, Mar. 2017.

[39] H. Shao and C.-Y. Tsui, “A robust, input voltage adaptive and low energy consumption level converter for sub-threshold logic,” in Proc. 33rd Eur. Solid State Circuits Conf., Sep. 2007, p. 310–315.

[40] S. R. Hosseini, M. Saberi, and R. Lotfi, “A low-power subthreshold to above-threshold voltage level shifter,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 61, no. 10, pp. 753–757, Oct. 2014.

[41] S. Kabirpour and M. Jalali, “A low-power and high-speed voltage level shifter based on a regulated cross-coupled pull-up network,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 66, no. 6, pp. 909–913, Jun. 2019.

[42] A. Shapiro and E. G. Friedman, “Power efficient level shifter for 16 nm FinFET near threshold circuits,” IEEE Trans. Very Large Scale Integ. (VLSI) Syst., vol. 24, no. 2, pp. 774–778, Feb. 2016.

[43] B. Razavi, Design of Analog CMOS Integrated Circuits, 2001, New York, NY, USA: McGraw-Hill, 2017.

[44] S. Eichhoff and J. C. Jarvis, “An investigation of neural stimulation efficiency with Gaussian waveforms,” IEEE Trans. Neural Syst. Rehabil. Eng., vol. 28, no. 1, pp. 104–112, Jan. 2020.

[45] A. Wongsarnpigoon and W. M. Grill, “Genetic algorithm reveals energy-efficient waveforms for neural stimulation,” in Proc. Annu. Int. Conf. IEEE Eng. Med. Biol. Soc., Sep. 2009, pp. 634–637.

[46] M. N. Khiaar, E. Martianova, C. Borries, S. Martel, C. D. Proulx, Y. De Koninck, and B. Gosselin, “A wireless fiber photometry system based on a high-precision CMOS biosensor with embedded continuous-time ΣΔ modulation,” IEEE Trans. Biomed. Circuits Syst., vol. 12, no. 3, pp. 493–509, Jun. 2018.

[47] X. Chen, T. Zhou, J. Huang, G. Wang, and Y. Li, “A sub-100 mV ultra-low voltage level-shifter using current limiting cross-coupled technique for wide-range conversion to I/O voltage,” IEEE Access, vol. 8, pp. 145577–145585, 2020.

[48] C. Wang, Y. Ji, C. Ma, Q. Cai, L. Qi, and Y. Li, “An ultra-low-voltage level shifter with embedded re-configurable logic and time-borrowing latch technique,” IEEE Access, vol. 9, pp. 79904–79910, 2021.
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