Implementation of the deconvolution method for signal peak detection in read-out ASIC

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Abstract. An application of the deconvolution method for signal peak detection in read-out ASIC for GEM detectors is described. Instead of usage of the conventional analog or digital peak detector, deconvolution technique to define the signal maximum was studied. In this case the digital data coming from the ADC are processed by a digital filter that deconvolves according to the pre-determined transfer function of the analog channel. Such processing allows to identify the signal peak values and also to provide reasonable pileup rejection. That enables higher rates of the incoming signals and reduces the amount of lost data. Combined with the analog channel employing 10-bit 25 MHz sampling rate ADC and 250 ns time constant 2nd-order shaper, the designed deconvolution block maintains peak detection accuracy within 9 LSBs. Time resolution of peak separation is 4 ADC sampling intervals or 100 ns.

1. Introduction
One of the problems of signal processing in read-out ASICs is signal superimposition at high signal rates, resulting in a loss of amplitude information. In the conventional approaches an analog or digital peak detector are used to determine the signal maximum in analog channel. Signal maximum will determine with error at overlays and information about peak will loss. To resolve the issue, deconvolution method is proposed, which allows to separate the superimposed signals and determine their amplitudes.

Paper considers a popular nowadays approach in digitization of analog detector signals at the earliest stage and their further processing in digital domain [1,2]. As an example, it presents a classical analog front-end channel, consisting of charge sensitive amplifier, 250 ns time constant 2-nd order shaper, followed by 25 MSPS 10-bit ADC [3] and deconvolution filter and necessary digital signal processing block [1,2]. Analog channel was designed for read-out signals from GEM-detectors with detector capacitances up to 100 pF and signal amplitude up to 100 fCb.

2. Deconvolution method
Primarily, a delta impulse of detector current is converted by an analog part, having a transfer function H(s) as a convolution of an input signal. Further the shaper output signal is digitized by an ADC, producing the sequence of samples, which processed by deconvolution digital filter with the transfer function W(z). If \( W(z) = 1/H(s) \), deconvolution filter output will contain several non-zero samples.
with values proportional to the input signal amplitude [4,5,6]. The filter coefficients are calculated from the inverted transfer function W(z) of the analog channel.

Single non-zero sample at the output of the deconvolution filter will appear if the input signal peak time is synchronous with the ADC sample. Otherwise, the output of the deconvolution filter will be presented by two non-zero samples.

Figure 1 shows examples of the synchronous and asynchronous cases. For the asynchronous case, the peak value of the signal is the sum of the non-zero samples at the filter output.

![Figure 1. Deconvolution output with synchronous and asynchronous sampling.](image1)

If two pulses are overlapped, there will be two groups of non-zero samples at the deconvolution filter output. An example of the deconvolution output is shown in the figure 2. The implemented version the deconvolution filter has been realized using 4-samples window to separate two signals. The window width determines the resolution time of impulses pileup rejection of pulses.

Peak detector has to have a dead time defined by a shaper fall time. If this condition is not met, the shaper output will contain the sum of the current signal and the falling edge of the previous one. In this case, the calculated amplitude will be wrong. This limits the maximum channel signal rate.

![Figure 2. Deconvolution output for overlapped pulses.](image2)

The analog channel with the 250 ns time constant 2nd-order shaper has the output fall times of about 700 ns. The fall time defines the dead time of the peak detector.
The deconvolution filter allows to reduce the minimum interval between pulses with their correct separation. Using of the 4 samples resolution deconvolution method at 25 MSPS ADC provides 100 ns dead time, which allows to increase the channel signal rate up to 7 times.

3. Implementing of the deconvolution filter in the read-out ASIC
Deconvolution filter was implemented in the read-out ASIC, intended for GEM detectors having capacitance up to 100 pF. Figure 3 shows a fragment of the read-out chip structure with the deconvolution filter.

![Read-out chip structure fragment with the deconvolution filter](image)

Deconvolution filter was designed as the digital 4-order finite impulse response (FIR) filter. The signal passes through the analog channel. Then it is converted by the ADC into a sequence of samples at a frequency of 20-30 MHz and is processed by the 4th-order deconvolution FIR filter.

The filter output value is calculated using formula (1).

\[ w_i = W_0 - W_1 \times d_{i-1} + W_2 \times d_{i-2} - W_3 \times d_{i-3} + W_4 \times d_{i-4} \]  

(1)

where \( w_i \) – i-th deconvolution filter output value, \( d_k \) – k-th ADC sample, \( W_n \) - n-th coefficient of the polynomial transfer function W(z).

In order to tune the filter to both channel characteristics and detector capacitance, the filter coefficients are adjustable and loaded by a serial configuration (slow control) interface.

FIR filter output sequence of samples is read out over a high speed serial interface at 320 Mb/s. In the implemented version of the read-out ASIC the peak value of the input signal is calculated outside the ASIC.

Figure 4 shows the error of peak determination versus the amplitude of the incoming signal (as % of the maximum ADC output value). Line (a) represents the error for digital deconvolution filter and the line (b) – for digital peak detector. In both cases the design used the analog channel featuring 250 ns time constant 2nd-order shaper and 10-bit 25 MSPS ADC.

The error of the input signal peak determination equals 9 LSBS at the maximum amplitude of the incoming signal. Error decrease of the deconvolution method at low amplitudes is limited by the ADC code width, which decreases the accuracy of signal waveform determination. Due to this fact, the actual error exceeds theoretical one.

Deconvolution filter, as an ASIC building block, was developed and prototyped in the UMC CMOS MMRF 180 nm process. The filter block has area of 645,4x207,6 sq. um. The power dissipation equals to 7,28 mW at 80 MHz filter clock frequency.
4. Conclusion
The realization of the deconvolution method for signal peak detection in read-out ASIC for GEM detectors has been considered. Deconvolution filter with the analog channel were implemented in the UMC CMOS MMRF 180 nm process. The designed deconvolution filter allows to separate and restore the amplitudes of overlapped signals if the time interval between peaks is at least 4 ADC samples. This allows to reject signal pileups and increases the channel signal rate up to 7 times compared with conventional analog channel with the digital peak detector. The analog channel, used in the project, was featured by a 2-order shaper at a 250 ns time constant used and 25 MSPS ADC sampling rate.

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