Received 14 September 2022, accepted 17 October 2022, date of publication 4 November 2022, date of current version 9 November 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3219732

A 5LCHB Inverter for PV Transformerless Applications With Reduced Leakage Ground Current

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This work was supported in part by the Consejo Nacional de Ciencia y Tecnología (CONACYT), Convocatoria de Ciencia Basica o Ciencia de Frontera under Grant number 319541, and in part by the National Graduate Scholarship from CONACYT under Grant 774225.

ABSTRACT Transformerless inverters for photovoltaic systems are widely used as it features low cost, volume, and weight. Thus, in recent years, its study has been of great interest to the research community. In this paper a transformerless cascade multilevel inverter for photovoltaic applications with leakage ground current compensation capability is presented. The proposed solution involves a second-order LC output filter with a particular connection, which is referred to as the DC-link-tied LC output filter. This solution is aimed to deal with the leakage-ground current issue, regardless of the considered PWM strategy. The mathematical model of the system involving such a particular LC output passive filter configuration is presented, out of which, both the differential-mode and the common-mode models are obtained. These models are used to explain the leakage-ground current improvement of the proposed DC-link-tied LC output filter. This hardware solution is evaluated under different modulation schemes to contrast the converter output response and the leakage-ground current performance. Finally, simulation and experimental results are performed using a 1 kW academic prototype to assess the performance of the proposed DC-link-tied LC output filter used in a transformerless inverter application.

INDEX TERMS Leakage ground current, passive filters, PWM strategy, transformerless photovoltaic systems.

I. INTRODUCTION Transformerless photovoltaic (PV) systems are widely spread in the solar energy market due to their proficient characteristics like, on the one hand, high efficiency and power density, and on the other hand, low cost, volume, and weight [1], [2], [3]. However, leakage-ground current (LGC) is an important issue observed in non-isolated grid-tied PV inverters.

The associate editor coordinating the review of this manuscript and approving it for publication was Zhilei Yao.

The LGCs are also referred to as common mode currents (CMC), and these are generated after the interaction of a fluctuating common-mode voltage (CMV) source [4] and stray capacitances that make a path towards the ground. The CMV fluctuations, usually present in the conventional operation of a PV inverter, are mainly created by the switching sequences generated by the modulation scheme which can cause also electromagnetic compatibility (EMC) problems [5]. The literature reports several methods to deal with CMV that can be classified as follows: specific design of
the pulse width modulation (PWM) strategy, virtual-ground connection, control techniques, common-ground connection, passive filtering, and redesign of the topology [6], [7], [8], [9]. Among these, PWM strategies, passive filtering, common-ground connection and control methods result in attractive solutions because they avoid the modification of the converter structure reducing the implementation cost [10].

Among the PWM methods used to mitigate the LGC, [11] proposes a hybrid multicarrier PWM based on the in-phase disposition sinusoidal level-shifted PWM (IPDSLSPWM) technique, where the number of carrier signals is reduced to the half of that required in the phase opposite disposition (POD) technique. The LGC is compensated after the CMV is restricted to a low band limit. This method is also implemented in [12] and [13], where the switching states are carefully chosen to maintain a constant CMV. In [13], a modulation scheme is proposed with CMV fluctuations three times each half-cycle, where the LGC magnitude is close to the limit imposed by several international standards. In [14], a modulation scheme referred to as leakage current reduction PWM (LCPWM) for a nine-level cascaded H-Bridge (CHB) inverter is proposed, where the number of carrier signals is reduced from eight to four, and the LGC is reduced to 24 mA Rms. In [15], two improved PWM strategies for a single-phase cascade multilevel inverter are proposed, that allow a suitable distribution of power losses between modules. The utilization rate of power switches is balanced and the switching times are reduced leading to high efficiency. In [16], an analysis of the common-mode behavior considering the parasitic capacitors is presented, and a specific selection of the switching states using a phase-shifted PWM is proposed to reduce the leakage current in a CHB inverter. Moreover, a PWM improvement for a transformerless inverter with common-ground connection is presented in [17]. However, the PWM technique, in this case, is devoted to the improvement of the input current ripple since the common-ground connection reduces inherently the LGC magnitude.

Although PWM schemes have a good performance to deal with the LGC issue, these methods force the switching of power devices, which may deteriorate the overall efficiency and the distribution power losses. Passive filtering methods represent another proposal to deal with the LGC issue. In [18], two DC capacitors are used to connect a common-mode filter (CMF) to a virtual ground formed at the middle point of the split DC-link in a single-phase HB converter. This hardware modification alleviates the LGC and the common-mode electromagnetic interference noise on the AC side. In [19], DC-AC side capacitors and DC-AC common-mode chokes are connected to the DC-bus through the virtual-ground path in a multilevel CHB converter. The LGC is attenuated by limiting the current of the DC-AC capacitors. The concept of a virtual DC-bus is introduced in [20], where the LGC is mitigated after fixing the potential of the negative pole of the DC bus to the neutral point of the mains. This topology operates with conventional sinusoidal PWM strategies while inherently suppressing the LGC.

The present paper introduces a particular connection of the output LC filter referred to as the DC-link-tied LC output filter aimed to deal with the LGC in a single-phase Five-Level Cascade H-Bridge (SLCHB) inverter. This particular configuration has been specifically designed to compensate the LGC by avoiding its circulation through the ground path. The LC filter configuration was chosen considering that, from the circuit analysis, can create a low impedance path for the LGC circulation and can be also adapted to the configuration of the cascade multilevel inverter. Moreover, the mathematical filter analysis provides the common and differential mode models to determine the leakage current behavior. In addition, four multi-carrier PWM methods are used to evaluate the proposed solution and their effects on the CMC. Thus, the paper contributions are summarized as follows:

i) A CHB multilevel converter with a DC-link-tied LC output filter for a transformerless PVS application is proposed to face the LGC issue.

ii) The differential-mode model and the common-mode model are obtained and used to analyze and explain the behavior of the power inverter switching states under conventional PWM strategies.

iii) The equivalent circuits of both the differential-mode and the common-mode are obtained. These circuits are instrumental for better visualization of the inverter LGC behavior, as well as for the output filter design.

iv) An LGC performance comparison under different conventional PWM strategies is presented.

The rest of the paper has been organized as follows: in Section II, the CHB topology with the proposed DC-link-tied output filter is presented. Section III presents the system modeling and the analysis of the proposed system. Section IV derives the analysis of the conventional PWM strategies. Section V describes the laboratory implementation and shows the experimental results. Finally, concluding remarks are provided in Section VI.

II. PROPOSED TOPOLOGY

Figure 1 shows the simplified circuit of the SLCHB inverter topology comprising two cascaded H-bridge converters and the proposed DC-link-tied LC passive filter. This configuration is able to synthesize five voltage levels and deals with the LGC issue. The output filter includes four inductors (one per branch starting from points ε1 to ε4), two for the upper H-bridge, and two for the lower H-bridge. Besides, each inductor of each branch is connected to the DC-link terminals through capacitors in an unconventional connection. In particular, the inductors of the upper H-bridge are connected to the positive terminal of the DC-link via capacitors C1 and C2, while inductors of the lower H-bridge are connected to the negative terminal of the DC-link via capacitors C3 and C4. As explained later, this configuration avoids the LGC circulation towards the grid because the proposed circuit provides
an alternative low impedance path through the output passive filter before reaching the grid. Thus, $L_1$, $L_2$, $L_3$, $L_4$, and $C_1$, $C_2$, $C_3$, $C_4$ are the passive elements of the proposed LC output filter; for the analysis convenience, the DC-link in each cell has been split in two voltages referred as $v_{cDC1}$, $v_{cDC2}$ for cell one, and $v_{cDC3}$, $v_{cDC4}$ for cell two; $v_{c1}$ to $v_{c4}$ represent the voltages through the filter capacitors; $i_{l1}$ to $i_{l4}$, and $i_{c1}$ to $i_{c4}$, are the currents flowing through inductors of the filter (inverter side) and capacitors and finally $i_1$ and $i_2$ label the grid currents.

The circuit considers stray capacitances $C_{P1}$ to $C_{P4}$ connected at the positive and negative terminals of the DC-link of each converter. These stray capacitances are formed between the PV terminals and the corresponding grounded PV frame. Therefore, a path can be established from the PV ground reference to the grid neutral point $N$. This path is referred to as the ground path and has an associated impedance $R_{GC}$. As above mentioned, the LGC is mainly produced by high-frequency fluctuations of the CMV, which is connected to the ground path via the stray capacitors. Recall that, such a CMV is normally produced by the commutation of the power semiconductors after a given modulation scheme. Notice that, a leakage current flows through each stray capacitance, and thus the LGC is forced to recirculate inside the converter.

III. SYSTEM MODELLING AND ANALYSIS

The converter dynamics are described based on the electrical variables shown in Fig. 1. It should be noted that, to facilitate the modeling of the 5LCHB converter with the proposed LC structure, all the injected voltages produced by a branch are referred to as the virtual points $P_1$ and $P_2$, which divide each DC-link in two. Based on Kirchoff’s voltage and current laws, the following dynamical expressions are obtained:

$$
L_1 \ddot{i}_{l1} = -v_{C1} - \frac{v_{PV}}{2} + e_1,
$$

$$
L_2 \ddot{i}_{l2} = -v_{C2} - \frac{v_{PV}}{2} + e_2,
$$

$$
L_3 \ddot{i}_{l3} = \frac{v_{PV}}{2} + e_3 - v_{C3},
$$

$$
L_4 \ddot{i}_{l4} = \frac{v_{PV}}{2} + e_4 - v_{C4},
$$

$$
C_1 \ddot{v}_{c1} = i_{l1} - i_1,
$$

$$
C_2 \ddot{v}_{c2} + C_3 \ddot{v}_{c3} = i_{l2} + i_{l3},
$$

$$
C_4 \ddot{v}_{c4} = i_{l4} - i_2,
$$

$$
P_{C1} \ddot{v}_{CP1} + P_{C2} \ddot{v}_{CP2} + P_{C3} \ddot{v}_{CP3} + P_{C4} \ddot{v}_{CP4} = i_{GC},
$$

in addition, the following system restrictions are considered:

$$
v_{c1} = -v_{CP1} - R_{GC} i_{GC} + v_s,
$$

$$
v_{c2} - v_{c3} = -v_{CP1} + v_{CP4},
$$

$$
v_{c4} = -v_{CP4} - R_{GC} i_{GC},
$$

$$
v_{c1} - v_{c2} + v_{c3} - v_{c4} = v_s,
$$

$$
v_{CP1} - v_{CP2} = v_{PV},
$$

$$
v_{CP3} - v_{CP4} = v_{PV},
$$

$$
i_1 + i_2 = -i_{GC}.
$$

Besides, it is a common practice to assume that all filter inductors have the same values, i.e., $L_1 = L_2 = L_3 = L_4 = L_1$; as well as for all output filter capacitors, i.e., $C_1 = C_2 = C_3 = C_4 = C$. This simplifies the converter modeling without losing the essence of the analysis. Following this
same motivation, it is assumed that the stray capacitances of the PV panels at the positive and negative terminals have the same value, i.e., \( C_{P1} = C_{P2} = C_{P3} = C_{P4} = C_{P} \). Moreover, it is assumed that both PV panels exhibit the same voltage \( V_{PV} \).

**A. DIFFERENTIAL AND COMMON MODE MODELS**

The mathematical model of the proposed circuit described by expressions (1)-(8) can be transformed and split into differential and common mode parts based on the following definitions:

\[
\begin{align*}
\varepsilon_{DM} & \triangleq e_1 - e_2 + e_3 - e_4, \\
i_{DM} & \triangleq \frac{i_1 - i_2}{2}, \\
i_{LDM} & \triangleq \frac{i_{L1} - i_{L2} + i_{L3} - i_{L4}}{2}, \\
v_{CDM} & \triangleq \frac{v_{C1} - v_{C2} + v_{C3} - v_{C4}}{2}, \\
\varepsilon_{CM} & \triangleq \frac{e_1 + e_2 + e_3 + e_4}{2}, \\
i_{LCM} & \triangleq \frac{i_{L1} + i_{L2} + i_{L3} + i_{L4}}{2}, \\
v_{CPCM} & \triangleq \frac{v_{CP1} + v_{CP2} + v_{CP3} + v_{CP4}}{2}, \\
v_{CCM} & \triangleq \frac{v_{C1} + v_{C2} + v_{C3} + v_{C4}}{2}.
\end{align*}
\]

Out of the transformation of the above variables, considering the system dynamics from (1) to (8), and system restrictions from (9) to (15) the differential mode model (DMM) for the proposed circuit, in a most compact form, is described by

\[
2L \ddot{i}_{LDM} = \varepsilon_{DM} - v_S, \quad (24)
\]

\[
v_{CDM} = v_S, \quad (25)
\]

where \( \varepsilon_{DM} \) is the differential mode voltage (DMV) injected by the 5LCHB inverter; \( i_{LDM} \) is the total differential mode current (DMC), which represents the sum of the DMC of inductances of each H-bridge converter; \( v_{CDM} \) is referred to as the total DMV of the output filter capacitors, which represents the sum of DMVs established between corresponding capacitors on each H-bridge converter; and \( i_{DM} \) is the DMC on the grid side.

The common mode model (CMM) is given by

\[
\begin{align*}
\frac{L}{2} \ddot{i}_{LCM} & = \varepsilon_{CM} - v_{CCM}, \\
2Cv_{CCM} & = i_{LCM} + i_{GC}, \\
2C_Pv_{CPCM} & = i_{GC}, \\
i_{GC} & = \frac{v_S - v_{CCM} - v_{CPCM}}{2R_{GC}}.
\end{align*}
\]

where \( \varepsilon_{CM} \) is the total common-mode voltage (CMV) injected by the 5LCHB inverter; \( i_{LCM} \) is referred to as the total common-mode current (CMC) of inductances; \( v_{CCM} \) is the total CMV of the output filter capacitors, and \( v_{CPCM} \) is the total CMV of the stray capacitors.

The equivalent circuits for the DMM and CMM of the 5LCHB with the proposed passive filter are depicted in Fig. 2.
TABLE 1. All possible switching states for the 5LCHB inverter topology.

| $\sigma_{DM}$ | $S_{11}$ | $S_{12}$ | $S_{13}$ | $S_{14}$ | $S_{21}$ | $S_{22}$ | $S_{23}$ | $S_{24}$ | State |
|---------------|----------|----------|----------|----------|----------|----------|----------|----------|--------|
| 2$V_{PV}$     | 1 0 0 1 1 0 0 1 | St1      |
| $V_{PV}$      | 1 0 0 1 1 0 0 1 | St2      |
|               | 1 0 0 1 1 0 0 1 | St3      |
|               | 1 0 0 1 1 0 0 1 | St4      |
|               | 0 1 0 1 1 0 0 1 | St5      |
| 0 V           | 1 0 1 0 1 0 1 0 | St6      |
|               | 1 0 0 1 0 1 0 1 | St7      |
|               | 0 1 1 0 1 0 1 0 | St8      |
|               | 0 1 0 1 1 0 1 0 | St9      |
|               | 1 0 1 0 1 0 1 0 | St10     |
| $-V_{PV}$     | 0 1 1 0 0 1 0 1 | St11     |
|               | 0 1 0 1 0 1 0 1 | St12     |
|               | 0 1 1 0 1 0 1 0 | St13     |
|               | 1 0 1 0 0 1 0 1 | St14     |
| $-2V_{PV}$    | 0 1 1 0 0 1 0 1 | St15     |

FIGURE 3. Carriers disposition for (a) PSPWM, (b) IPD, (c) POD and (d) APOD to generate a five-level waveform.

considered. The gate signals for the 5LCHB are obtained after the comparison of the reference signal (a sinusoidal waveform at the grid frequency) against $n$ carriers, where $n$ depends on the number of voltage levels $m$ at the inverter output [22], [23], i.e., $n = m - 1$. Based on this, the phase-shift angle between carriers in the PSPWM method that cancels out all the harmonic content up to the $k$th carrier group must be computed as $\phi_{cr} = 360^\circ/(m - 1)$ or by $\phi_{cr} = 180^\circ/k$, where $k$ is the number of cells [26].

Table 1 collects all possible switching states for the 5LCHB to generate a five-level voltage waveform. Table 2 lists the particular switching states, from Table 1, used on each PWM technique. It is worth noting that the PSPWM method exhibits redundancies of switching states to generate the voltage levels $-V_{PV}$, 0 and $+V_{PV}$. This is in contrast to LSPWM methods that only use one switching state per voltage level.

A. THD ANALYSIS

To evaluate the THD versus the modulation index $m_a$, it is first considered the case without LGC compensation, i.e., without considering the DC-link-tied capacitor in the circuit of Fig. 1, instead, only a symmetric L output filter is considered. For this analysis, it is important to take into account the frequency index $m_f$ that plays an important role in the THD contribution. It is common practice to select $m_f$ as an odd integer; which allows harmonic reduction, while avoiding subharmonics due to the odd symmetry of the signal [24], [25].

Considering $f_m$ and $f_c$ as the reference and carrier frequency, the $m_a$, $m_{a,ps}$ and $m_{a,ls}$ are the modulation index for the PSPWM and LSPWM methods, respectively. For instance, $m_f = 167$ for a $f_{sw} = 10.02$ kHz ($f_{sw}$ is the switching frequency of the system) and $f_m = 60$ Hz is the grid frequency.

Fig. 4 depicts, in percentage, the output voltage THD ($\%THD_{e14}$) and grid side current THD ($\%THD_{i1}$) versus the modulation index $m_a$. Notice that, while the $\%THD_{e14}$ is similar in all PWM methods, the $\%THD_{i1}$ is better in the LSPWM method because the LGC contribution in the PSPWM is higher, which severely affects the $\%THD_{i1}$. In addition and implementing the LGC compensation, the $THD_{i1}$ of the PSPWM method becomes better than that of the LSPWM because the effective switching frequency of the inverter $f_{sw}$ in the PSPWM is $4 \times f_{sw}$ instead of $f_{sw}$ observed in LSPWM methods.

B. POWER LOSSES DISTRIBUTION ANALYSIS

This study considers that the 5LCHB is composed by four half-bridge IGBT modules, each module comprising 2 switches (module 1: $S_{11}$ and $S_{12}$; module 2: $S_{13}$ and $S_{14}$; module 3: $S_{21}$ and $S_{22}$; and module 4: $S_{23}$ and $S_{24}$), as shown in the electrical scheme of Fig. 1. Figure 5 shows, for every

TABLE 2. Particular switching states used on each PWM technique.

| $\sigma_{DM}$ | PSPWM | IPD | POD | APOD |
|---------------|-------|-----|-----|------|
| 2$V_{PV}$     | St1   | St1 | St1 | St1  |
| $V_{PV}$      | St2   | St5 | St5 | St5  |
|               | St3   | -   | -   | -    |
|               | St4   | -   | -   | -    |
|               | St5   | -   | -   | -    |
| 0 V           | St8   | St9 | St9 | St9  |
|               | St9   | -   | -   | -    |
|               | St10  | -   | -   | -    |
|               | St11  | -   | -   | -    |
| $-V_{PV}$     | St12  | St12| St12| St12 |
|               | St13  | -   | -   | -    |
|               | St14  | -   | -   | -    |
|               | St15  | -   | -   | -    |
| $-2V_{PV}$    | St16  | St16| St16| St16 |
PWM technique under study, the conduction and switching losses for each module (one bar per module) considering rated power. These results were obtained employing simulations using the Thermal Module of PSIM software, where the IGBT model is loaded using the curves of the datasheet provided by the manufacturer. The model constructed in this way provides a good approximation of the switching and conduction power losses of the IGBT and its anti-parallel diode. Note that, the power distribution losses are somehow balanced in the PSPWM, while the LSPWM techniques show bigger conduction losses than switching losses. Furthermore, according to Fig. 5, the PSPWM presents the biggest power losses affecting its overall efficiency. Table 3 summarizes and compares the main characteristics of the PWM methods under study.

![Figure 4](image1.png)

**FIGURE 4.** Percentage of THD against modulation index \( m_p \) for (a) the output voltage \( \% \text{THD}(e_{1n}) \), and (b) the grid current \( \% \text{THD}(i_1) \).

![Figure 5](image2.png)

**FIGURE 5.** Power losses distribution of (a) PSPWM, (b) IPD, (c) POD, and (d) APOD. The power losses are grouped in sets of 4 bars each, a bar per half-bridge module: (from left to right) module 1 to module 4.

**TABLE 3.** Comparison between the main characteristics of the PWM methods under study.

| Parameter                          | PSPWM                        | (LSPWM) IPD, POD, APOD |
|------------------------------------|------------------------------|-------------------------|
| Device switching frequency \( f_{sw} \) | \( f_{sw} = f_s \)          | Different \( \left( f_{sw}, (m-1) \right) \) |
| Device conduction period           | Same for all power switches  | Required                |
| Inverter frequency \( f_{inv} \)   | \( (m-1) f_{sw} \)          | \( f_{sw} \)            |
| Power losses distribution          | Similar in all power         | Conduction losses >     |
|                                    | semiconductors               | switching losses        |
|                                    | Q1 = Q4, Q2 = Q3             |                         |
| Power losses per module            | Same in all modules          | Different on each module|

V. EXPERIMENTAL RESULTS

The 5LCHB inverter with the proposed DC-link-tied LC filter has been tested in a 1 kW experimental prototype. The 5LCHB prototype has been built with four IGBT power modules SKM75GB1200 driven by SKHI22A-R modified gate drivers which can detect and indicate a module in fault, the fault can also be transmitted to other modules and a circuit has been also designed to receive the PWM signals via optic fibers. The modulation schemes are implemented in a control platform based on the TMS320F28335 DSP where a specific circuit was designed to emit the PWM signals via optic fibers.

Figure 6 depicts the experimental system setup. The stray capacitors \( C_{p1} \) to \( C_{p4} \) are emulated by MKP capacitors, which are connected to a resistor emulating the ground resistance in the ground current path. The experimental prototype parameters are summarized in Table 4. It should be noted that, the voltage at the input of the inverter is selected considering that the maximum voltage at the inverter output is the addition of the voltages at the input of each cell \( v_{PV} \) and considering the required voltage for power injection in a single-phase grid with 120 V RMS, then the selected voltage at the inverter output is 220 V. Moreover, the parasitic capacitance values \( C_{p1} \) to \( C_{p4} \) are chosen considering [21], where the parasitic capacitance value has been measured for different models of PV panels operating under different conditions and also considering [28], where a set of reference values are given. The \( R_{GC} \) value was set according to the average resistivity of soils and resistance of single rods (the most commonly used) which are described in [29]. Moreover, \( C_{DC1} \) and \( C_{DC2} \) are defined based on the energy required by the load, considering the current through them and the voltage supplied by the DC source in each cell. In fact, these capacitances were oversized to ensure suitable operation of the inverter since this issue is not a matter of study in this paper. Finally, the parameters for the proposed LC filter were selected considering the base values described in [30]. The evaluation tests consider the analysis of the switching pattern of each PWM method, time response, frequency response, and the efficiency comparative study of the PWM strategies.

Figures 7, 8 and 9 show, for the modulation schemes (LSPWM) IPD, POD and APOD, the inverter output voltage...
The five-level output voltage of the inverter $e_{DM}$ and the gate signals per semiconductor device $S_{11}$ to $S_{24}$. It can be observed that the switching pattern on each modulation technique is able to generate a five-level signal after the combination of the switching signals of each semiconductor device. Moreover, as a consequence of these commutation signals, the inverter output voltage displays a five-level voltage signal on every modulation scheme. Notice that, the semiconductors are only switched during a small period of time. This means that high efficiency of the 5LCHB inverter is expected out of these modulation techniques.

The five-level output voltage of the inverter $e_{DM}$ and the commutation signals for each semiconductor device $S_{11}$ to $S_{24}$ regarding PSPWM scheme are shown in Fig. 10. Notice that, the modulation scheme is able to generate a five-levels output voltage. However, the commutation signals show that the power semiconductors are switching during the complete fundamental period. This means that the conduction and commutation losses of the power converter are increased by employing this modulation scheme.

Figures 11, 12, 13 and 14 depict the steady-state responses of the IPD, POD and APOD schemes, respectively, in the case where the DC-link tied capacitors $C_1$, $C_2$, $C_3$, $C_4$ have been disconnected. Each figure shows (from top to bottom) the inverter output voltage $e_{DM}$, grid current $i_1$ and LGC $i_{GC}$. As above mentioned, the waveform of $i_{GC}$ depends on the CMV variations; hence, the $i_{GC}$ waveforms for the IPD, POD and APOD schemes are all similar, they all reach peaks close to 1.2 A. However, the PSPWM modulation shows an $i_{GC}$ with peaks of about 2 A, and with a different waveform due to the different switching patterns of the power devices. Moreover, the RMS value of current $i_{GC}$ is around 355 mA, 338 mA, and 364 mA for IPD, POD and APOD modulations techniques, respectively; whereas the RMS value for PSPWM is 1.22 A. These are all greater than the 300 mA imposed by the standard DIN VDE 0126-1-1 [31], [32], [33]. Moreover, this high LGC value propagates towards the grid currents causing a perceptible distortion in these currents.

Figure 15 depicts the transient responses of the grid currents $i_1$, $i_2$ and $i_{GC}$ under the IPD scheme after connection.
of the DC-link-tied capacitors $C_1, C_2, C_3, C_4$. Notice that, $i_{GC}$ is significantly reduced and, as a side effect, the passive filter guarantees good performance of the grid currents. As observed, a distortion appears at zero-crossings, however, this issue can be addressed by implementing the control loop. Figures 16 and 17 show the results for POD and APOD techniques, respectively. Notice that, similar results are obtained as those of the IPD scheme, that is, LGC mitigation is achieved together with properly filtered grid side currents. It should be remembered that the CMC, represented by the LGC, is propagated to the DMC to produce the actual grid side currents. Figure 18 presents the PSPWM scheme performance, where it is worth noticing the effectiveness of the proposed DC-link-tied LC filter at minimizing the $i_{GC}$, whose high-frequency components have been filtered out and their effect on the grid currents is minimized. As a result, after connecting the proposed DC-link-tied LC filter, a high-quality grid current waveform and a significant reduction of $i_{GC}$ are obtained no matter what PWM techniques are in use. The connection of the proposed DC-link-tied passive filter prevents the circulation of the $i_{GC}$ toward the electrical grid. That is, the filter forces the LGC to recirculate through the converter before reaching the electrical grid. As a side effect, the converter CMC increases, which may cause a slight reduction in the overall efficiency.

In the following, the steady state response for the PWM modulations applied to the 5LCHB with the overall proposed DC-link-tied LC filter is presented. Figure 19 (from top to bottom) shows the output voltage $e_{DM}$, grid side current $i_1$ and $i_{GC}$, which reveal that the LGC is effectively compensated. Although a residual $i_{GC}$ remains in the ground path, the RMS value of $i_{GC}$ is well below the limit and
Also a high-quality grid side current waveform is obtained. Similar experimental results were obtained for POD, APOD and PSPWM techniques. The results for the aforementioned PWM algorithms are shown in Figs. 20, 21 and 22, respectively.

In what follows, the frequency contents of the signals generated in the system composed by the converter and the DC-link-tied passive filter are analyzed. As expected, the frequency contents of the signals derived from level-shifted PWM methods are very similar among them, as observed in Figs. 23, 24 and 25. The harmonic content caused by these PWM methods is effectively compensated, out of which the THD for \( i_o \) is within the requirements for power injection. In addition, the dominant harmonics of the injected voltage \( e_{DM} \) appear as a side-band, around \( m_f \), which is defined as \( m_f = f_{sw}/f_g \). It is worth noticing that, in the PSPWM scheme, the dominant harmonics appear as a side-band centered around \( 4mf \). In consequence, the THD of the 5LCHB inverter output current is smaller in the PSPWM scheme than in the level-shifted methods as observed in Fig. 26.
TABLE 5. Summary results of the 5LCHB inverter with the proposed DC-link-tied LC filter.

| PWM method     | THD\textsubscript{v,DM} | THD\textsubscript{i1} | i\textsubscript{GC} w/o cap | i\textsubscript{GC} with cap | f\textsubscript{inv} | η\textsubscript{EURO} | η\textsubscript{CEC} | i\textsubscript{1} ripple |
|----------------|-------------------------|------------------------|----------------------------|-----------------------------|----------------------|----------------------|----------------------|------------------------|
| PSPWM          | 37.1%                   | 0.89%                  | 1.22 A\textsubscript{RMS}   | 29.3 mA\textsubscript{RMS}  | 40 kHz               | 92.17%               | 93.67%               | 19.89 mA               |
| (LSPWM) IPD    | 37.2%                   | 1.60%                  | 355 mA\textsubscript{RMS}   | 18.7 mA\textsubscript{RMS}  | 10 kHz               | 95.3%                | 96.51%               | 264.10 mA              |
| (LSPWM) POD    | 37.2%                   | 1.61%                  | 338 mA\textsubscript{RMS}   | 21.6 mA\textsubscript{RMS}  | 10 kHz               | 95.3%                | 96.51%               | 264.11 mA              |
| (LSPWM) APOD   | 37.2%                   | 1.61%                  | 364 mA\textsubscript{RMS}   | 20.6 mA\textsubscript{RMS}  | 10 kHz               | 95.3%                | 96.5%                | 264.11 mA              |

FIGURE 24. FFT inverter output voltage and grid side current for (LSPWM) POD with the proposed DC-link-tied LC filter.

FIGURE 25. FFT inverter output voltage and grid side current for (LSPWM) APOD with the proposed DC-link-tied LC filter.

FIGURE 26. FFT inverter output voltage and grid side current for PSPWM with the proposed DC-link-tied LC filter.

Next, a comparative efficiency study is performed. For this, the Thermal Module tool of PSIM has been used, which allows the calculation of the switching and conduction losses of the complete 5LCHB inverter structure. The simulation involves more realistic power devices, whose model is described based on information recuperated from the datasheet. The efficiency η of the 5LCHB inverter topology operating under each PWM method, in the power range of 50 W to 1 kW, is calculated as η = (P\textsubscript{in} − P\textsubscript{losses})/P\textsubscript{in}, where P\textsubscript{in} is the total power consumption on the DC side, and P\textsubscript{losses} represents the total power losses in all power switches of the 5LCHB inverter. The European efficiency (η\textsubscript{EURO}) and the California Energy Commission efficiency (η\textsubscript{CEC}) are used to take into consideration that the efficiency changes concerning the injected power level. The efficiency curves are depicted in Fig. 27. Notice that, the curves for the level-shifted PWM schemes show higher efficiency values than the PSPWM strategy because, in this latter, the power devices are switching continuously along the whole grid period. A summary of the above results is listed in Table 5, which considers as key parameters both the inverter output voltage and the grid side current THDs (THD\textsubscript{v}, THD\textsubscript{i1}) as well as the effective frequency under each PWM method, the LGC magnitude before and after the connection of the DC-link-tied capacitors (i\textsubscript{GC} without DC-link-tied capacitors, i\textsubscript{GC} with DC-link-tied capacitors) and the efficiencies η\textsubscript{EURO} and η\textsubscript{CEC}.

VI. CONCLUSION

This paper has focused on the study of a passive LC solution to suppress the common-mode current in a photovoltaic transformerless five-level cascade H-Bridge inverter. The proposed solution consists of a 5LCHB inverter plus a proposed specific connection of an LC output filter. This particular connection of the output filter has been referred to as a DC-link-tied filter. The proposed solution was assessed under four typical PWM strategies known as PSPWM, IPD, POD, and APOD obtaining a considerable reduction in the RMS values of the CMC well bellow of the 300 mA\textsubscript{RMS} [28]. For
the proposed solution, the common and differential mode models were derived to get a better description of the system operation. In particular, the common-mode model revealed the benefits of the proposed DC-link-tied filter structure, which forced the common mode current produced by the common mode voltage, to recirculate in the inverter before reaching the grid side connection, thus considerably reducing the leakage ground currents. The proposed system was evaluated in a 1 kW prototype under the four conventional multicarrier PWM strategies. The results showed that the highest RMS value of the leakage ground current was for the PSPWM strategy reaching a value of 29.3 mA, while the lowest value was for the IPD reaching a value of 18.7 mA. In conclusion, the 5LCHB inverter with the proposed DC-link-tied LC filter structure is suitable for transformerless applications, as it complies with the international regulation, which establishes a maximum of 300 mApkA for the leakage ground current. It was also shown that the $\eta_{CEC}$ for IPD, POD, and APOD was $\eta_{CEC} > 96\%$, while for the PSPWM strategy was $\eta_{CEC} > 93.5\%$. On the other hand, the $\eta_{IPD}$ for IPD, POD, and APOD was $\eta_{CEC} > 95\%$, while for the PSPWM strategy was $\eta_{IPD} > 92\%$ according to Table 5.

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