Abstract—Stereo matching is a critical task for robot navigation and autonomous vehicles, providing the depth estimation of surroundings. Among all stereo matching algorithms, Efficient Large-scale Stereo (ELAS) offers one of the best tradeoffs between efficiency and accuracy. However, due to the inherent iterative process and unpredictable memory access pattern, ELAS can only run at 1.5-3 fps on high-end CPUs and difficult to achieve real-time performance on low-power platforms. In this paper, we propose an energy-efficient architecture for real-time ELAS-based stereo matching on FPGA platform. Moreover, the original computational-intensive and irregular triangulation module is reformed in a regular manner with points interpolation, which is much more hardware-friendly. Optimizations, including memory management, parallelism, and pipelining, are further utilized to reduce memory footprint and improve throughput. Compared with Intel i7 CPU and the state-of-the-art CPU+FPGA implementation, our FPGA realization achieves up to 38.4× and 3.32× frame rate improvement, and up to 27.1× and 1.13× energy efficiency improvement, respectively.

I. INTRODUCTION
Stereo vision is a critical component in many computer vision applications, such as robot navigation, autonomous vehicles, augmented reality, and gesture recognition [1]. Especially, stereo vision provides the availability of depth estimation to abstract 3D scene structure from 2D images captured by two cameras. Accurate depth information is crucial for the safety of autonomous systems and serves as the prerequisite for following localization and motion planning [2].

Efficient Large-Scale Stereo (ELAS) [3] has recently attracted increasing attention and becomes one of the most accurate stereo matching algorithms. It overcomes the downsides of local matching methods that perform poorly on ambiguous surfaces and the downsides of global matching methods that require extensive computational efforts and high memory capacities. ELAS enables dense matching with small aggregation windows by reducing ambiguities on correspondences.

However, it has been shown that ELAS can only reach 1.5-3 fps speed on a high-end CPU [3]. Some intermediate steps in ELAS algorithm, such as the support points triangulation, involve a significant number of sequential, iterative, and condition processes with unpredictable memory accesses, posing great challenges for implementing ELAS on resource-constrained edge devices and limiting its application in latency and power-sensitive applications and autonomous cyber-physical systems [4], [5].

Some prior efforts have been made to accelerate ELAS on low-power platforms. [6] implements ELAS on an embedded FPGA-CPU SoC and achieves 17.3 fps on KITTI dataset [7] under 3 W power. [8] further introduces an ELAS-SGM (Semi Global Matching) combination approach and evaluates it on an FPGA-CPU platform, achieving 50 fps and 4.5 W power consumption on the KITTI dataset. However, both [6] and [8] accelerate only part of ELAS modules on FPGA and offload the triangulation and grid vector extraction computation on CPU during processing, which brings in higher power consumption and performance degradation.

In this paper, iELAS is proposed as a fully FPGA-based architecture of ELAS stereo vision system. The most time-consuming and iterative triangulation procedures are accelerated on FPGA by introducing an extra support points interpolation module, making it much more hardware-friendly (Sec. II-B). By utilizing parallelisms, pipelining, ping-pong storage mechanism, and several memory management techniques, all modules of iELAS are fully accelerated on an FPGA platform (Sec. III). Our design achieves up to 38.4× and 3.32× speedup over Intel i7 CPU and the state-of-the-art FPGA+Arm ELAS implementation [6], with 27.1× and 1.13× lower power consumption, respectively (Sec. IV).

The main contributions of this paper are as follows:

- A novel ELAS-based stereo vision hardware accelerator is proposed for real-time applications on energy-efficient FPGA platforms.
- An interpolated optimized support point extraction pattern is utilized to make ELAS algorithm much more hardware-friendly.
- Optimizations including memory management, parallelism, and pipelining are further exploited to save hardware resource consumption and improve throughput.

II. ALGORITHM FRAMEWORK
In this section, we present the original ELAS algorithm flow (Sec. II-A), and then propose an interpolated optimized ELAS algorithm to make it much more hardware-friendly (Sec. II-B).

A. Original ELAS Algorithm
ELAS algorithm is inspired by the observation that despite many stereo correspondences being highly ambiguous, some
can be robustly matched. It first establishes a prior over the disparity space by forming a triangulation on a set of correspondences whose estimation is simpler and comes with a higher degree of confidence. These correspondences provide a rough approximation of the scene geometry and guide the dense matching stage. ELAS is attractive since the slanted plane prior can be very efficiently implemented, and the dense depth estimation is fully decomposable over all pixels.

Fig. 1a demonstrates the overview of the ELAS algorithm. The detailed steps are described as follows:

**Descriptor Extraction.** The input stereo image pairs (left and right images) first pass through Sobel filters over the horizontal and vertical gradients to extract the descriptor information of each pixel.

**Support Point Extraction.** A set of sparse but confident correspondences (support points) is calculated using descriptor information over the full disparity range.

**Filtering.** By comparing support point values to neighbors within a window region, two types of obtained support points are removed. The implausible values that are inconsistent would respectively corrupt the representation are filtered out. The redundant values that are identical to neighbors in the same row or column and unnecessarily complicate the coarse representation are also removed.

**Disparity Computation.** The filtered support points are then used to guide the dense stereo matching in two separate ways. First, a slanted plane prior is constructed to approximate coarse scene geometry by using Delaunay triangulation. Second, a grid vector is created by pooling support points within a sub-region to make stereo matching more reliable.

**Post-processing.** ELAS uses post-processing techniques, such as gap interpolation, median filtering, to invalidate occluded pixels and further smooth the images.

### B. Interpolated Optimized ELAS Algorithm

In the original ELAS algorithm, the Delaunay triangulation module involves a significant number of speculations and random memory accesses, posing great challenges in FPGA acceleration. [6] chooses to offload triangulation computation to the CPU core, bringing higher power consumption and latency. To make Delaunay triangulation computing more hardware-friendly, we put forward a special way to interpolate support points and enable regular Delaunay triangulation procedures, which can be fully accelerated in the FPGA platform.

The interpolated ELAS algorithm flow is shown in Fig. 1b. After extracting support points, we add an interpolation module to derive a set of newly support points with fixed numbers and coordinations, which significantly facilitates the construction of slanted planes. The interpolation is performed using the disparity value of the support points within the neighborhood to fill the vacant positions. The detailed steps are as follows:

**Horizontal Interpolation.** For the position \( s \) to be interpolated, first search the support points in the horizontal direction within \((s - s_h, s + s_h)\) window. If there are support points \( (P_L, P_R) \) lying on both sides and their disparity values \(|D_{P_L} - D_{P_R}| \leq \epsilon\), then we use the mean of \( (D_{P_L}, D_{P_R}) \) to interpolate. If \(|D_{P_L} - D_{P_R}| > \epsilon\), then \( \min(D_{P_L}, D_{P_R}) \) will be chosen for interpolation.

**Vertical Interpolation.** If no support point pair \( (P_L, P_R) \) is found in the horizontal direction, then search in the vertical direction to find \( (P_T, P_B) \) and perform interpolation using the same method as step 1.

**Constant Interpolation.** If no support point pairs are found in both horizontal and vertical directions, then fill a constant disparity value \( C \) in the position \( s \).

Following this procedure, we present an example of support points interpolation in Fig. 2, where \( s_h = 5, \epsilon = 3, C = 0 \).

The accuracy of the proposed interpolated ELAS is evaluated on the New Tsukuba Stereo Dataset [9]. Fig. 3a visualize the support points obtained from the original ELAS algorithm, where different colors represent the ranges of different disparity values. Fig. 3b demonstrates the results after interpolation. It is well observed that the disparity ranges of interpolated support points align with the original set, but the coordinates...
of the new set of support points are much more regular. This regular pattern will significantly facilitate the following Delaunay triangulation procedure.

We further evaluate the disparity error across the whole image as:

\[ \text{Error} = \frac{1}{N} \sum \left| D_{\text{interpolated}} - D_{\text{real}} \right| \]

where \( D_{\text{interpolated}} \) is the calculated disparity value and \( D_{\text{real}} \) is the groundtruth disparity value.

Tab. I demonstrates the matching error rate under different lightning conditions. We can observe that the accuracy of our proposed interpolated ELAS algorithm surpasses the traditional ELAS algorithm in all scenarios.

III. HARDWARE ARCHITECTURE

In this section, we provide an overview of the proposed iELAS accelerator (Sec. III-A) as well as the detailed implementations of each module (Sec. III-B). Several leveraged optimization techniques are presented in Sec. III-C.

A. Hardware Architecture Overview

The overall architecture of the proposed ELAS-based accelerator, iELAS, is demonstrated in Fig. 4. It is fully accelerated on programmable logic of FPGA. The descriptor extractor is implemented to accelerate feature information extraction from input stereo image pairs. Support point extractor and dense matching blocks are responsible for disparity value calculation by leveraging interpolated support points. Several design traits, such as memory management, parallelism, and pipelining are proposed to improve throughput and save hardware resources.

B. Hardware Architecture of Each Compute Module

The detailed hardware architecture implementation of each compute module is described as follows.

Descriptor Extractor. This module is responsible for obtaining image pair’s descriptor information for further support points extraction and dense matching use. The input image pair is processed by 3x3 Sobel filter in both horizontal and vertical direction, and the pre-processed results are stored in Block RAM (BRAM) for further support points extraction and dense matching use. The Sobel filter is operated as:

\[ F_{3x3} = \begin{bmatrix} 1 & 0 & -1 \\ 2 & 0 & -2 \\ 1 & 0 & -1 \end{bmatrix} \begin{bmatrix} \text{win}_{11} & \text{win}_{12} & \text{win}_{13} \\ \text{win}_{21} & \text{win}_{22} & \text{win}_{23} \\ \text{win}_{31} & \text{win}_{32} & \text{win}_{33} \end{bmatrix} \]  

(2)

where \( \text{win}_{ij} \) is the pixel value of input images.

The descriptor extractor module is mainly composed of line buffers and register banks, as shown in Fig. 5. Since the image is fed row-wisely, the length of line buffers is the same as the image width. When the first pixel reaches \( \text{win}_{22} \) position, the extraction process will be triggered and the descriptor of current patch will be calculated. By performing Sobel filtering on \( w \times h \) image in this way, all descriptors will be extracted in \( (w+1) \) clock cycles, enabling real-time processing.

Support Point Extractor. This module extracts a sparse set of support points based on obtained descriptors in any \( 5 \times 5 \) window and generates disparity values with their coordinates. As shown in Fig. 6, a specific pixel descriptor \( (u, v) \) is selected in left image, and the energy cost function is calculated between \( (u, v) \) and each neighbor descriptors in right image. Next, a point in right image is selected and the same process is repeated. The pair with the minimum energy cost value will be considered as the matching pair, and the disparity value is computed accordingly. The results are stored in BRAM.

Filtering. This module removes both implausible and redundant values from disparity values. It consists of line buffers and register banks. The filtered results are sent to the grid vector module.

Grid Vector. The grid vector module takes the filtered disparity results as input. It aggregates them to limit the disparity values evaluated in the dense matching stage, which can improve the robustness of the system. The grid vector results are stored in BRAM for dense matching use.

Interpolator. This module performs disparity value interpolation horizontally and vertically within the neighbor of extracted support point, significantly facilitating the Delaunay triangulation implementation.

Delaunay Triangulator. It takes the interpolated support points as input and constructs a mesh that can approximate coarse scene geometry and guide the dense matching stage.
Fig. 7: Ping-pong memory management scheme.

C. Key Accelerator Design Traits

To reduce resources consumption and improve throughput, we use several optimization techniques in the iELAS design.

**BRAM Saving.** Original ELAS design requires high memory capacities. The descriptor of each pixel is concatenated to 128-bit, and 2400 BRAMs are needed for an image pair. To reduce memory consumption, we propose to directly store 8-bit intermediate results after Sobel filter, making descriptor concatenation task complete during support points extraction, which can achieve around 8× memory consumption reduction.

**Parallelism.** Considering both support point and descriptor extractions use 5×5 window, we choose to store every five rows in one BRAM, significantly facilitating the parallelism of support points extraction and dense matching. In this way, both modules can be finished within 17 ms, whereas they need 271.6 ms and 374.4 ms in the original design, respectively.

**Ping-pong Storage Mechanism.** To improve the throughput of iELAS, we adopt a ping-pong storage mechanism (Fig. 7). During processing, frame \( i + 1 \) will arrive before the process of frame \( i \) is finished in BRAM 1. To avoid potential data loss of frame \( i \), we store the information of frame \( i + 1 \) in BRAM 2 during the procedure. When frame \( i + 2 \) arrives, BRAM 1 has been released and ready for repeated use. This ping-pong mechanism can improve system’s throughput by almost 2×.

**Grid Vector Optimization.** Original ELAS design stores all 256 disparity values for grid vector computation. However, we notice that most of the support points are removed in the filtering module and cannot be fully utilized by the grid vector. By analyzing the accuracy and resource consumption under the different number of stored support points, we choose to store 20 disparity values of each pixel for grid vector, which can greatly save memory capacity without accuracy degradation.

IV. Evaluation Results

This section evaluates the hardware resource utilization (Sec. IV-A) and stereo matching accuracy (Sec. IV-B) of proposed iELAS accelerator, and demonstrates its advantages in performance and energy efficiency (Sec. IV-C).

A. Experiment setup

**Hardware Platform and Dataset.** The proposed iELAS accelerator is fully implemented on Virtex-7 VC707 FPGA, and evaluated on the New Tsukuba Stereo dataset and KITTI dataset with 640×480 and 1242×375 resolution, respectively.

**Resource Utilization.** Tab. II demonstrates the resource utilization of the proposed iELAS under two datasets. The FPGA device has 304K LUTs, 607K Flip-Flops, and 1030 BRAMs in total. Overall, the hardware architecture consumes 37.62% LUT, 9.62% Flip-Flop, and 48.70% BRAM on the New Tsukuba Stereo dataset and 47.71% LUT, 12.99% Flip-Flop, and 45.56% BRAM on KITTI dataset.

B. Accuracy Analysis

The accuracy of iELAS is measured by matching error which means the number of estimated disparities differing from ground truth (same method as [6]). As shown in Tab. III, comparing with software implementation (i7 CPU) and the state-of-the-art SoC implementation (FPGA+ARM) [6] on two datasets, iELAS can maintain similar matching accuracy after support points interpolation (under \( s_δ = 50, \epsilon = 15, C = 60 \)).

C. Performance Evaluation

**CPU Comparison.** Tab. IV compares the frame rate and power of iELAS and Intel i7 CPU. Compared with CPU, iELAS achieves 38.4× and 38.3× speedup with 27.1× and 26.5× energy efficiency improvement on New Tsukuba Stereo dataset and KITTI dataset, respectively.

**Existing Accelerator Comparison.** Tab. IV also compares iELAS with FPGA+Arm implementation [6]. Compared with [6], iELAS raises the performance by 3.27× and 3.32×, and improves energy efficiency by 1.13× and 1.07× for two datasets, respectively. This benefits from the fact that we achieve FPGA acceleration for all compute modules by leveraging support point interpolation, while [6] offloads Grid Vector and Delaunay Triangulation modules computation on Arm CPU and other modules on FPGA.

V. Conclusion

In this paper, an ELAS-based stereo vision system, iELAS, is proposed for real-time and energy-efficient applications and fully implemented on FPGA. The ELAS algorithm is reformulated as a regular pattern with support points interpolation for hardware-friendly implementation. All modules in ELAS are accelerated on FPGA to reduce the latency significantly.
The iELAS is also designed in a ping-pong storage pattern with other memory management techniques to further reduce memory footprint and improve the throughput. The evaluation results on the KITTI dataset have shown iELAS could achieve up to $3.32 \times$ and $38.4 \times$ speedup in frame rate, and $1.13 \times$ and $27.1 \times$ improvement in energy efficiency when compared to the state-of-the-art Arm+FPGA and Intel i7 CPU, respectively.

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REFERENCES

[1] Z. Wan, B. Yu, T. Y. Li, J. Tang, Y. Zhu, Y. Wang, A. Raychowdhury, and S. Liu, “A survey of fpga-based robotic computing,” arXiv preprint arXiv:2009.06034, 2020.

[2] Z. Wan, Y. Zhang, A. Raychowdhury, B. Yu, Y. Zhang, and S. Liu, “An energy-efficient quad-camera visual system for autonomous machines on fpga platform,” arXiv preprint arXiv:2104.00192, 2021.

[3] S. Krishnan, Z. Wan, K. Bharadwaj, P. Whatmough, A. Faust, G.-Y. Wei, D. Brooks, and V. J. Reddi, “The sky is not the limit: A visual performance model for cyber-physical co-design in autonomous machines,” IEEE Computer Architecture Letters, vol. 19, no. 1, pp. 38–42, 2020.

[4] S. Krishnan, Z. Wan, K. Bharadwaj, P. Whatmough, A. Faust, S. Newman, G.-Y. Wei, D. Brooks, and V. J. Reddi, “Machine learning-based automated design space exploration for autonomous aerial robots,” arXiv preprint arXiv:2102.02988, 2021.

[5] O. Rahnama, D. Frost, O. Miksik, and P. H. Torr, “Real-time dense stereo matching with elas on fpga-accelerated embedded devices,” IEEE Robotics and Automation Letters, vol. 3, no. 3, pp. 2008–2015, 2018.

[6] A. Geiger, P. Lenz, C. Stiller, and R. Urtasun, “Vision meets robotics: The kitti dataset,” The International Journal of Robotics Research, vol. 32, no. 11, pp. 1231–1237, 2013.

[7] O. Rahnama, T. Cavallari, S. Golodetz, A. Tonioni, T. Joy, L. Di Stefano, S. Walker, and P. H. Torr, “Real-time highly accurate dense depth on a power budget using an fpga-cpu hybrid soc,” IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 66, no. 5, pp. 773–777, 2019.

[8] S. Martull, M. Peris, and K. Fukui, “Realistic cg stereo image dataset with ground truth disparity maps,” in ICPR workshop TrakMark2012, vol. 111, pp. 117–118, 2012.