Photovoltaic-assisted self-Vth-cancellation CMOS rectifier for synergistic RF energy harvesting

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Abstract A highly efficient CMOS rectifier for RF energy harvesting has been developed (using 0.18-μm CMOS technology). To operate with high efficiency even under extremely low input power conditions, the voltage-doubler-based rectifier was implemented using an effective combination of self-Vth-cancellation (SVC) and photovoltaic (PV)-assisted techniques. In this rectifier, the threshold voltage (Vth) of the diode-connected MOSFET was compensated for by a DC bias voltage generated from not only the on-chip PV cells, but also from the output voltage of the rectifier itself. Therefore, the rectifier operated with high efficiency even under low input power conditions. Furthermore, a bias voltage limiter using simple pn diodes was adopted to regulate the excessive Vth compensation effectively and realize a high efficiency in the operation of the rectifier over a wide power range. The radio frequency to DC power conversion efficiency (PCE) of 30.8% was achieved at an input power level of ~15 dBm, a frequency of 1 GHz, an output load resistance of 10 kΩ, and a light irradiance of 10 mW/m².

Keywords: energy harvesting, radio waves, photovoltaic, power conversion efficiency, rectifier

Classification: Energy harvesting devices, circuits and modules

1. Introduction

Radio frequency (RF) energy harvesting has become significantly important in a wide range of applications such as Internet of Things (IoT) [1, 2], implantable biomedical devices [3, 4, 5, 6, 7], and radio frequency identification tags (RFIDs) [8, 9, 10, 11]. In these applications, RF energy harvesting is utilized as a form of wireless power transfer (WPT) for autonomous power supply. When harvesting energy, although multiple ambient energy sources including light, heat, vibration, and other such sources [12] exist at the same time and the same place, they are generally utilized exclusively, independent of one another. In order to effectively utilize multiple ambient energy sources, a “synergistic energy harvesting” concept, which utilizes multiple energy sources to compensate for the disadvantages inherent in the use of a single energy source, has been proposed [13].

Fig. 1 shows the concept of a common RF energy harvesting design and a synergistic RF energy harvesting design. In a common RF energy harvesting scheme (frame with red dashes), an antenna receives ambient radio waves, the matching network transfers the maximum power of the antenna to the rectifier, and the rectifier converts the RF signal to DC power. The DC power is stored in an energy storage device, or directly drives the load device. In this system, major challenges are the limited RF power and low RF to DC power conversion efficiency (PCE) of the rectifier under low input power conditions. A rectifier is a key component for efficient RF energy harvesting, under low input power conditions. Although a rectifier has been realized using diode-based topology [14], a diode-connected MOSFET is commonly used as a rectifying diode in CMOS technology. Fig. 2(a) shows a voltage doubler that is a typical rectifier utilizing CMOS technology. The PCE, which is a common figure of merit (FoM) for evaluating rectifiers, is expressed by the following equation [15].

$$\text{PCE} = \frac{P_{\text{OUT}}}{P_{\text{IN}}} = \frac{P_{\text{OUT}}}{P_{\text{OUT}} + P_{\text{LOSS}}} \geq \frac{V_{\text{DC}}}{V_{\text{DC}} + V_{\text{TO}}} \geq \frac{V_{\text{RF}} - V_{\text{TO}}}{V_{\text{RF}}},$$

where $P_{\text{OUT}}$, $P_{\text{IN}}$, $P_{\text{LOSS}}$, $V_{\text{DC}}$, $V_{\text{TO}}$, and $V_{\text{RF}}$ are the DC output power, the RF input power, the power loss of the rectifier, the DC output voltage, the turn-on voltage of the rectifying diode, and the peak voltage amplitude of the applied RF signal, respectively. In this case, the $V_{\text{TO}}$ in (1) is almost equal to the threshold voltage (Vth) of the MOSFET. Equation (1) shows that the PCE can be increased by decreasing the Vth of the MOSFET. Therefore, various Vth compensation techniques have been proposed [15, 16, 17, 18, 19, 20, 21, 22, 23, 24]. One example is the self-Vth-cancellation (SVC) scheme [15, 16] shown in Fig. 2(b). It is the same as the conventional voltage doubler except that gate electrodes of the nMOS and the pMOS are connected to $V_{\text{OUT}}$ and ground, respectively. It utilizes a self-compensation technique that compensates for the Vth of the MOSFET by the DC output voltage generated by the

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rectifier itself. Although a high PCE is obtained at medium input power, the PCE is not large enough under low input power conditions because the DC output voltage acting as a compensating voltage to lower the Vth is too low, whereas, under high input power conditions, the Vth is excessively compensated for by a high output voltage. In this condition, reverse leakage current, which was ignored in the previous simplified analysis of (1), increases significantly, resulting in increased diode loss and degraded PCE. Therefore, input power range having a high PCE is limited to a medium input power region.

A PV-assisted CMOS rectifier is proposed as an example of the “synergistic energy harvesting” concept [13, 22, 23, 24], shown in Fig. 1 with a solid blue line. Photovoltaic (PV) cells (solar cells) generate a DC voltage and compensate for the Vth of the MOSFET as shown in Fig. 2(c). Compared with a conventional voltage doubler, wherein nMOS gate and pMOS gate are directly connected to the ground and VOUT, respectively; on-chip PV cells consisting of pn diodes are inserted in the gate bias paths of diode-connected nMOS and pMOS transistors. The PCE of the PV-assisted CMOS rectifier improves over the entire input power range as compared with conventional voltage doubler. However, the Vth compensation is insufficient because the bias voltage generated by the PV cell is low under typical lighting conditions; hence, the achieved PCE is not sufficient. Although a series connection of two PV cells to increase the output voltage is possible [25], the two electrically isolated series connected PV cells that are required in this application cannot be integrated in the same substrate by conventional CMOS integrated circuit technologies.

In this study, we propose a photovoltaic-assisted self-Vth-cancellation CMOS rectifier [26]. We combine the SVC and PV-assist techniques to enhance the threshold voltage compensation. Additionally, a voltage limiter mechanism for regulating the excessive Vth compensation by the SVC scheme is presented, to equip the rectifier to operate over a wide power range.

The rest of the paper is organized as follows: Section 2 describes the proposed rectifier. The rectifier equipped with a voltage limiter for enhancing PCE over a wide power range is described in Section 3. Conclusions are provided in Section 4.

2. PV-assisted SVC CMOS rectifier

2.1 Circuit design

Fig. 3 shows the proposed PV-assisted SVC CMOS rectifier. This rectifier utilizes the Vth compensation technique to achieve high PCE under low input power conditions. The basic concept of the rectifier is based on the utilization of both the DC output voltage of the rectifier itself and the output voltage generated by the PV cell to bias the gates of rectifying MOSFETs. Based on the SVC CMOS rectifier [15, 16] shown in Fig. 2(b), wherein the gates of nMOS and pMOS are connected to the VOUT and the ground, on-chip PV cells consisting of simple pn diode are inserted in the gate bias paths of MOSFETs. When output voltage is low under low input power conditions, the Vth is compensated for by the PV cell; hence, the PCE of the PV-assisted SVC CMOS rectifier, even under low input power conditions, is greatly enhanced. The conventional PV cells for power generation require a large cell area, a high level of light irradiation, and maximum power point tracking (MPPT) mechanism. However, because the purpose of the PV cells in this rectifier application is not generating power, but bias voltage generation, a smaller cell area and lower level of light irradiation such as indoor light is sufficient, and the MPPT mechanism is not required. Because output of the PV cell is connected to the gate of MOSFET with extremely high impedance, it operates in an open-circuit condition and the photocurrent does not flow out of the PV cell. Incidentally, PV cells are inserted between the DC node and gate of the MOSFET, which is isolated from RF nodes such that the parasitic effect due to RF signal that causes power loss can be minimized. A test chip of PV-assisted SVC CMOS rectifier was designed and fabricated by 0.18-µm, 5-metal layer (ML) CMOS technology. The channel width and length of the nMOS were 3.6 µm and 0.18 µm, respectively, and those of the pMOS were 10.8 µm and 0.18 µm, respectively. Two PV cells for nMOS biasing and pMOS biasing were implemented on the same substrate as that of the rectifier, as shown in Fig. 4. For nMOS biasing, the PV cell consists of a p+ -diffusion/n-well/p-substrate structure as shown on the left. For pMOS biasing, the PV cell consists of a n+ -diffusion/p-well/deep-n-well/p-substrate structure using the triple well technology as shown on the right. A junction composed of the surface diffusion layer and underlying well acts as a PV cell for gate biasing. The p-well/deep-n-well junction is short-circuited and therefore can be ignored. These structures are required not only to electrically isolate them, but also to make the gate bias voltages generated by the PV cells
symmetrical [23]. Note that, in order to increase the bias voltage generated by the PV cells, a non-silicide technique is adopted to fabricate the PV cells [24]. The n-well/p-sub junction of the nMOS bias PV cell on the left of Fig. 4 is reverse biased and the photocurrent flows from the DC output node to the ground. However, because this photocurrent (in nA level) is much smaller than the output current (in μA level) of the rectifier, it does not affect the PCE of the rectifier. The size of the square surface diffusion layer of PV cells is $7 \times 7 \, \mu\text{m}^2$ on each side. The transistor area is covered by the top two metal layers (ML4 and ML5) for shading. Both coupling capacitor $C_C$ and output smoothing capacitor $C_S$ were designed to have a capacitance of 1.13 pF.

2.2 Measurement setup
The PCE was evaluated by on-wafer measurements. Measurements were carried out at an RF input frequency $f_{RF}$ of single-tone 1 GHz and an output load resistance $R_L$ of 10 kOhm using a vector network analyzer (VNA, Agilent N5242A) unless otherwise specified. Because target radio waves for energy harvesting were assumed to be in UHF bands, for example, the waves used in television broadcasting, a mobile phone and Wi-Fi, frequency of 1 GHz was chosen as a representative frequency. The PCE of the rectifier was calculated from the measured values using the following equation:

$$\text{PCE} = \frac{P_{\text{OUT}}}{P_{\text{IN}}} = \frac{V_{\text{OUT}}^2}{R_L P_{\text{SRC}} (1 - |S_{11}|^2)}, \quad (2)$$

where $V_{\text{OUT}}$, $P_{\text{SRC}}$, and $S_{11}$ are the output voltage of the rectifier, the source power supplied from the VNA, and the measured reflection coefficient, respectively. Although necessary in practical energy harvester design, the rectifier’s performance was measured without an input impedance matching network to measure the intrinsic performance of the proposed rectifier. Therefore, the PCE was evaluated not as a function of $P_{\text{SRC}}$ but as a function of $P_{\text{IN}}$. An LED lamp was used as the light source in order to simulate typical indoor lighting conditions. The irradiance of the LED lamp was controlled by a source meter (KEITHLEY 2400). The light irradiance $E$ was measured by a photo radiometer (Delta OHM HD2302) with an irradiance probe (LP471RAD).

2.3 Measurement results and discussion
Fig. 5 shows the measured PCE of the proposed rectifier in comparison with the previously reported rectifiers (voltage doubler, SVC [15, 16] and PV-assisted CMOS [13, 22, 23, 24]). Measurements were performed at a light irradiance $E$ of 10 mW/m$^2$. As shown in the Fig. 5, the PCE of the PV-assisted SVC rectifier was significantly improved over the input power range from $-25$ to $-15$ dBm. Specifically, the proposed rectifier achieved a peak PCE of 27.5% at an input power of $-16$ dBm. Incidentally, although the light irradiance in typical indoor conditions is about 3 W/m$^2$, a high PCE could be realized even under a very low light irradiation of 10 mW/m$^2$. However, the PCE of the proposed rectifier was degraded under high input power conditions because $V_{\text{th}}$ was excessively compensated for, and reverse leakage current increased as with the SVC scheme.

### PV-assisted SVC CMOS rectifier with bias voltage limiter

3.1 Circuit design
The weakness of the PV-assisted SVC CMOS rectifier described in section 2 is the degradation of the PCE under high input power conditions due to excessive $V_{\text{th}}$ compensation and the resulting increase in reverse leakage current. Therefore, if the excessive $V_{\text{th}}$ compensation is effectively regulated, a higher PCE can be expected even under high input power conditions. In other words, the rectifier will operate efficiently over a wide power range. Although highly efficient technologies over a wide power range have been proposed [27, 28, 29, 30, 31], the advanced version of the PV-assisted SVC CMOS rectifier innovatively adopts a gate bias voltage limiter mechanism consisting of a pn diode to appropriately regulate $V_{\text{th}}$ compensation. Fig. 6 shows the newly proposed PV-assisted SVC CMOS rectifier equipped with bias voltage limiters. Bias voltage limiters were added at two places: between the nMOS gate and ground, and between the pMOS gate and $V_{\text{OUT}}$. When $V_{\text{OUT}}$ increases due to an increase in $P_{\text{IN}}$ and the gate bias voltage becomes higher than the turn-on voltage of limiters, the photocurrent flows into the limiters and generates constant bias voltage limiting the excessive $V_{\text{th}}$ compensation. The current flowing through the limiters is supplied from the output of rectifier circuit, resulting in some amount of energy loss. However, because the PV cell is inserted in-series with the limiter, flowing current is actually a photocurrent (in pA level) that was much lower than the output current (in μA level) of the rectifier. Hence, there was no problem with the efficiency of the rectifier. The PV cell acts not only as a bias voltage generator but also as a current limiter to prevent useless current flowing from $V_{\text{OUT}}$ to ground. Although a voltage
3.2 1x and 2x limiter

In Fig. 8(a), the 1x limiter structure is shown. The 1x limiter for regulating nMOS bias voltage is composed of a $p^+$-diffusion/n-well/p-substrate structure, and the structure for regulating pMOS bias voltage is an $n^+$-diffusion/p-well/deep-n-well/p-substrate structure. The size of the square surface diffusion layer of the limiters was $7 \times 7 \mu m$. The transistor and limiter areas were covered by the top two metal layers (ML4 and ML5) for shading. Limiter structures are the same as PV cells except for the additional metal shading layers.

Fig. 8(b) presents the structure of the 2x limiter. The 2x limiters for nMOS is composed of an $n^+$-diffusion/p-well/deep-n-well/p-substrate and a $p^+$-diffusion/n-well/p-substrate structure. This structure was necessary to prevent the photocarriers generated in the non-shaded region from flowing into the voltage limiter pn junction area composed of the $n^+$-diffusion/p-well structure of the upper-side limiter. The photocarriers generated in the non-shaded region flow into the deep-n-well, but there is no problem with the operation of the limiter because the photocurrent is supplied from the output terminal of the rectifier. The 2x limiters for pMOS are composed of a series connection of two $n^+$-diffusion/p-well/deep-n-well/p-substrate structures. The size of the square surface diffusion layer of limiters was $7 \times 7 \mu m$. The transistor and limiter area were covered by the top two metal layers (ML4 and ML5) for shading.

The I-V characteristics of the limiters were first measured. Figs. 9(a) and 9(b) show measurement setups for the 1x and 2x limiters. In Fig. 9(a), the applied voltage of the $p^+$-diffusion was swept, and the flowing current was measured. In Fig. 9(b), $0.5 V$ was applied to the deep-n-well to emulate $V_{OUT}$, and the flowing current was measured by sweeping the p-well voltage. Measured I-V characteristics of the 1x and 2x limiter are shown in Fig. 10. These results show that the turn-on voltage of the limiter can be altered by connecting diodes in series. In other words, limiting voltage can be changed by the number of diode stages.

3.3 Measurement results and discussion

Fig. 11 shows the PCE measurement results of the PV-
assisted SVC CMOS rectifiers with the 1x and 2x limiters and without limiters. With the 1x limiter, there was no SVC effect, and it operated similar to the PV-assisted CMOS rectifier [13, 22, 23, 24]. The photocurrent generated by the PV cell flows into the limiter and the limiting voltage is determined by the I-V characteristics of the limiter; considering this fact, the same limiting voltage or bias voltage develops because the diode structure and I-V characteristics of the limiter are the same as that for PV cell used in the PV-assisted rectifier. Therefore, the PCE for rectifier with a 1x limiter is almost the same as that for the PV-assisted CMOS rectifier shown in Fig. 5. In other words, because the limiting voltage of the 1x limiter was too low, the SVC mechanism could not be activated. On the other hand, with the 2x limiter, because the excessive Vth compensation was effectively regulated, the PCE under high input power conditions significantly improved in comparison to the rectifier without a limiter. These results show that this rectifier realized a wide power range of high efficiency operation by adding the 2x limiter.

PCE measurement results of the PV-assisted SVC CMOS rectifier with the 2x limiter under various light irradiation conditions from 10 mW/m² to 25 W/m² are shown in Fig. 12. Because the bias voltage increased with an increase in the light irradiance and the Vth of the MOSFET was compensated to a greater extent, the PCE under low input power conditions significantly improved in comparison to the rectifier without a limiter. These results show that this rectifier realized a wide power range of high efficiency operation by adding the 2x limiter.

4. Conclusion

We developed a high efficiency PV-assisted SVC CMOS rectifier for synergistic RF energy harvesting. A DC bias voltage compensated for the Vth of diode-connected MOSFET. This bias voltage was generated from not only the on-chip PV cells, but also from the output voltage of the rectifier itself. The bias voltage enhances the efficiency of rectifier under low input power conditions. Moreover, the adoption of the 2x limiter regulates the excessive Vth compensation and improves the PCE over a wide power range. The PCE of the proposed rectifier attained a value of 30.8% at an input power of −15 dBm. Wide high-PCE range was also obtained.

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