Performance Characterization of Multi-threaded Graph Processing Applications on Intel Many-Integrated-Core Architecture

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Abstract—Intel Xeon Phi many-integrated-core (MIC) architectures usher in a new era of terascale integration. Among emerging killer applications, parallel graph processing has been a critical technique to analyze connected data. In this paper, we empirically evaluate various computing platforms including an Intel Xeon E5 CPU, a Nvidia GeForce GTX1070 GPU and an Xeon Phi 7210 processor codenamed Knights Landing (KNL) in the domain of parallel graph processing. We show that the KNL gains encouraging performance when processing graphs, so that it can become a promising solution to accelerating multi-threaded graph applications. We further characterize the impact of KNL architectural enhancements on the performance of a state-of-the-art graph framework. We have four key observations: 

1. Different graph applications require distinct numbers of threads to reach the peak performance. For the same application, various datasets need even different numbers of threads to achieve the best performance. 
2. Only a few graph applications benefit from the high bandwidth MCDRAM, while others favor the low latency DDR4 DRAM. 
3. Vector processing units executing AVX512 SIMD instructions on KNLs are underutilized when running the state-of-the-art graph framework. 
4. The sub-NUMA cache clustering node offering the lowest local memory access latency hurts the performance of graph benchmarks that are lack of NUMA awareness. At last, we suggest future works including system auto-tuning tools and graph framework optimizations to fully exploit the potential of KNL for parallel graph processing.

I. INTRODUCTION

In the age of big data, information explodes usually in the form of large scale graphs. To understand information better, graph processing has been an important technique to compute, analyze and visualize connected big data. Real-world large scale graphs include social networks, the Internet, transportation networks, citation graphs, biochemical networks and cognitive networks, which typically have millions of vertices and millions to billions of edges. Because of the huge graph size, it is natural for both industry and academia to develop parallel graph frameworks to accelerate graph processing on various hardware platforms. A large number of shared memory or distributed CPU frameworks, e.g., IBM System-G [30], Giraph [33], Pregel [28], Galois [31], PowerGraph [14] and GraphLab [27], have emerged for scalable in-memory graph processing. Recent research efforts also propose GPU frameworks such as VertexAPI2 [12], Medusa [47], LonestarGPU [5], CuSha [17] and Gunrock [42] to perform high throughput graph processing on GPUs.

For CPU frameworks, graphs can be partitioned, distributed and processed among different nodes [14], [27], [28], [38] by message passing schemes or computed locally on one shared memory node [30], [31]. Graph applications are notorious for their frequent communications between computations on each vertex or edge [14], [30], [31]. In a large scale cluster, the frequent communications are translated to huge volumes of messages across multiple nodes [27], [28], [38], seriously limiting the performance of graph processing. Even a single Mac-Mini SSD-based laptop can potentially outperform a medium scale cluster [21] for graph processing. In a shared memory multi-core processor node, the communications are interpreted to loads and stores in the memory hierarchy [30], [31]. When executing the Graph500 framework, the core efficiency in a shared memory node is averagely 100× higher than that in a cluster [37]. However, compared to GPUs, the computing throughput of graph frameworks on CPUs is still constrained by the limited number of cores.

GPU graph frameworks capture the inherent parallelism of graph processing by mapping and computing millions of vertices on thousands of GPU cores [30], [31]. Although graph applications exhibit irregular memory access patterns, frequent thread synchronizations and data dependent control flows [32], GPUs still substantially boost their performance over CPUs [12], [43]. However, the performance of graph processing on GPUs is sensitive to graph topologies. When traversing graphs with a huge diameter, GPUs are even slower than CPUs due to the lack of traversal parallelism [49]. Moreover, in some commercial applications, simple operations, like adding or deleting an edge in a graph, may cost a significant portion of the total application execution time [30], but it is difficult for GPUs to support such basic operations.

Recently, Intel Xeon Phi MIC processor emerges as a promising GPU alternative for parallel graph processing. In this paper, we focus on the performance characterization of multi-threaded graph applications on a second generation Intel Xeon Phi processor - KNL [36]. Our contributions are summarized as follows:

- We empirically evaluate a state-of-the-art graph framework on three hardware platforms: an Xeon E5 CPU, a GTX1070 GPU and a KNL processor. We show that the KNL demonstrates promising performance when running multi-threaded graph applications.
- We further characterize performance details of multi-threaded graph benchmarks on KNL. We measure and analyze the impact of KNL architectural enhancements such as many out-of-order (OoO) cores, simultaneous multithreading (SMT), cache clustering modes, vectorization processing units (VPUs) and 3D stacked MCDRAM on parallel graph processing. We have four key observa-
tions: ❶ Different graph applications require distinctive numbers of threads to achieve their best performance. For the same benchmark, various datasets ask for different numbers of threads to attain the shortest execution time. ❷ Only a few graph applications benefit from the high bandwidth MCDRAM, while others favor the low latency DDR4 DRAM. ❸ VPs executing AVX512 SIMD instructions on KNLs are underutilized when processing graphs. ❹ The sub-NUMA cache clustering mode offering the lowest local memory access latency actually hurts the performance of graph benchmarks that are lack of NUMA awareness.

• For future work, we suggest possible system auto-tuning tools and framework optimizations to fully exploit the potential of KNL for multi-threaded graph processing.

II. BACKGROUND AND MOTIVATION

A. Graph Processing Frameworks

The rapid and wide deployment of graph analytics in real-world diversifies graph applications. A lot of applications such as Breadth first search incorporate graph traversals, while other benchmarks such as page rank involve intensive computations on vertex properties. Though low-level hardwired implementations [2], [4], [8], [11], [10] have demonstrated high computing efficiency on both CPUs and GPUs, programmers need high-level programmable frameworks to implement a wide variety of complex graph applications to solve general real-world graph problems. Therefore, graph processing heavily depends on specific frameworks composed of data structures, programming models and basic graph primitives to implement various functionalities. Previous research efforts propose many graph frameworks on both CPUs [14], [27], [30], [31] and GPUs [5], [12], [17], [47] to hide complicated details of operating on graphs and provide basic graph primitives.

In this paper, we adopted and studied IBM System-G [30] graph framework, which is a state-of-the-art and comprehensive graph computing library used by several industrial solutions. Like most previous graph frameworks [5], [12], [14], [27], [31], System-G embraces the vertex centric programming model, where a vertex is the basic element of a graph. The vertex properties and the outgoing edges are attached to the same vertex data structure. The data structure of all vertices is stored in an adjacency list, and the outgoing edges inside a vertex data structure also form an adjacency list of edges.

B. Target Graph Benchmarks

The graph applications we studied in this paper are from a graph benchmark suite, graphBIG [30], which is implemented with basic graph primitives from IBM System-G graph framework. Most benchmarks in graphBIG have a CPU OpenMP version and a GPU CUDA version. By manipulating data structures from IBM System-G in CUDA kernels, the GPU implementations in graphBIG also share the same graph framework including the vertex centric programming model. During the initialization, graph data in the CPU main memory is converted and transferred to the GPU device memory.

The graph workloads can be grouped into two types. The first type includes benchmarks computing on graph structures. For example, traversal-based applications, such as Breadth first search, begin from a vertex (root) in the graph, systematically navigate or update their neighbors until all reachable vertices have been visited. For this group of applications, only a subset of vertices is typically active at a given point in the execution. They often introduce a large number of memory accesses but limited arithmetic operations. Their irregular memory behavior results in extremely poor spatial locality in the memory hierarchy. The second group consists of benchmarks operating on rich vertex properties. For instance, computation-based applications, such as page rank, frequently update vertex properties. They incorporate heavy arithmetic computations on vertex properties and intensive memory accesses leading to hybrid workload behaviors. Most vertices are active in all stages of the second type of applications. We selected, compared and studied six common graph benchmarks in this paper. We introduce their details as follows:

- **Breadth First Search** traverses a graph by starting from a root vertex and exploring the neighbor nodes first. The traversal parallelism can be exploited by vertex capture, in which each thread picks a vertex and searches among its neighbors.
- **K-Core** finds a maximal connected sub-graph where all vertices have degree at least \( K \). The algorithm repeatedly deletes vertices whose degree is less than \( K \) until no such node is left.
- **Single Source Shortest Path** calculates the minimum cost paths from a root vertex to each vertex in a given graph. We only address graphs with non-negative weights in this paper. The algorithm iteratively relaxes vertices and proceeds in a greedy manner by relaxing only the shortest path vertex at each iteration.
- **Graph Coloring** partitions a graph into independent sets. One set contains vertices sharing the same color. The algorithm launches multiple iterations, each of which is responsible for labeling one color. For each vertex, the algorithm compares its color with that of its neighbors. If the color of a vertex happens to be the largest among its neighbors, it is marked by the current iteration color.
- **Page Rank** uses the probability distribution to compute page rankings. The rankings are also probabilities which specify the likelihood that a person on the Internet will visit a page. The rank of each vertex is computed by \( PR(u) = \frac{1}{N} \sum_{v \in N(u)} \frac{PR(v)}{K(v)} \), where the PR of a vertex \( u \) is decided by the PR of each vertex \( v \) in its neighbor set \( N(u) \) divided by its outgoing edge number \( K(v) \).
- **Triangle Count** measures the number of triangles that are formed in a graph when three vertices are connected to each other. The algorithm forms the neighbor set for each vertex \( S_{N(v)} \), computes the intersection of \( S_{N(v)} \) for each edge, sums the numbers of intersection sets and divides it by two at each vertex.
C. Graph Topology

The performance of graph applications is heavily influenced by the topology of graph datasets. We studied how topologies impact the benchmark performance via following metrics. The eccentricity $\epsilon(v)$ of a vertex $v$ in a given connected graph $G$ is the maximum graph distance between $v$ and any other vertex $u$ of $G$. The diameter $d$ of a graph is the maximum eccentricity of any vertex in the graph ($d = \max_{v \in V} \epsilon(v)$). The Fiedler value of the graph is the second smallest eigenvalue of the Laplacian matrix of $G$. The magnitude of this value exhibits how well connected the graph is. For traversal-based applications such as Breadth first search, traversal iteration number is proportional to the eccentricity and the Fiedler value. The vertex degree indicates the number of edges connected to a vertex. The average vertex degree and the vertex degree distribution of a graph reflect the amount of parallelism. Large vertex degree variations introduce substantial load imbalance during graph traversals. Real-world graph can be categorized into two types: the first has a large diameter with evenly distributed degree, e.g., road networks; and the second includes small eccentricity graphs with a subset of few extremely high-degree vertices, e.g., social networks. We chose different datasets from both categories, and generated several synthesized graphs with diameters varying from small to huge in Section III.

D. Intel Xeon Phi Architecture

1) Overall Architecture: Intel Xeon Phi is a series of MIC processors targeted at supercomputing and server markets. It is fully compatible with the x86 instruction set and allows the fast deployment of standard parallel shared memory programming tools, models and libraries such as OpenMP. The KNL [36] is the second generation MIC architecture manufactured by 14nm technology and has been widely adopted by many supercomputing data centers such as the national energy research scientific computing center [3].

The detailed architecture of KNL is shown in Figure 1. It is built by up to 72 Atom (Silvermont) cores, each of which is based on a low operating frequency 2-wide issued OoO micro-architecture supporting four concurrent threads (SMT). Additionally, every core has two VPU s that support SIMD instructions such as SSE/2, AVX2 and AVX512 that is a new 512-bit advanced vector extension of SIMD instructions for the x86 instruction set. A VPU can execute up to 16 single precision operations or 8 double precision floating point operations in each cycle. Two cores form a tile sharing a 1MB 16-way L2 cache and a caching home agent (CHA), which is a distributed tag directory for cache coherence. All tiles are connected by a 2D Mesh network-on-chip (NoC).

2) MCDRAM: The KNL main memory system supports up to 384GB of DDR4 DRAM and 8~16GB of 3D stacked MCDRAM. The MCDRAM significantly boosts the memory bandwidth, but the access latency of MCDRAM is actually longer than that of DDR4 DRAM [29]. As Figure 2 shows, MCDRAM can be configured as a parallel component to DDR4 DRAM in main memory (flat mode), a hardware managed L3 cache (cache mode) or both (hybrid mode). The flat mode offers the MCDRAM high bandwidth and the DDR4 DRAM low latency by software interfaces. However, programmers have to track the location of each data element and manage the software complexity. On the contrary, the cache mode reduces the workload of programmers by transforming the MCDRAM to a software-transparent direct mapped cache where the data and its tag are stored in one row. The hybrid mode combines the other two modes.

3) Cache Clustering Mode: Since all KNL tiles are connected by a Mesh NoC where each vertical and horizontal link is a bidirectional ring, all L2 caches are maintained coherent by the MESIF protocol. To enforce cache coherency, KNL has a distributed cache tag directory organized as a set of per-tile tag directories (shown as CHA in Figure 1) that record the state and location of all memory lines. For any memory address, by a hash function, KNL identifies which tag directory recording that address. As Figure 3 shows, the KNL cache can be operated in five modes including All-to-All, Hemisphere, Quadrant, SNC-2 and SNC-4. When a core confronts a L2 miss, it sends a request to look up a tag directory. The directory finds a miss and transfers this request to the memory controller. At last, the memory controller fetches data from the main memory and returns it to the original core. In the All-to-All mode, memory addresses are uniformly hashed across all tag directories. During the L2 miss, the core may send a request to a tag directory physically located in the farthest quadrant from the core. After the directory finds a miss, it may also send this request to a memory controller located in a third quadrant. Therefore, a L2 miss may have to traverse the entire Mesh to read one line from the main memory. The Quadrant (Hemisphere ) mode divides a KNL chip into four (two) parts. During the L2 miss, the core still needs to send a request to any tag directory on the chip, but the data associated to the target tag directory must be in the same part that the tag directory is located. The memory accesses from a tag directory are managed by its local memory or
Intel Xeon Phi MIC processors rise as a fusion of multi-core CPUs and high-throughput GPUs, so that it can offer the advantages of both hardware platforms. The many OoO cores, VPUs executing AVX512 SIMD instructions, and high bandwidth MCDRAM empower KNLs to boost computing throughput over multi-core CPUs. On the other hand, compared to GPUs, it is easier for KNLs to support some basic and important graph primitives such as deleting a vertex or an edge without any external assistance. Previous physical-machine-based works [7], [8], [16], [24], [44] find that the first generation Xeon Phi, Knight Corner, has poor performance when processing graphs due to its feeble cores. Although a recent simulator-based work [2] characterizes the performance of multi-threaded graph applications on a MIC processor composed of simple single-issue in-order cores, it fails to consider the architectural enhancements offered by KNLs, e.g., OoO cores, SMT, cache clustering modes, VPUs and MCDRAM. To our best knowledge, this work is the first to characterize and analyze the performance of multi-threaded graph applications on the KNL MIC architecture. In this paper, we try to answer four key questions about parallel graph processing on KNLs: ① Compared to contemporary computing platforms including a GPU and a multi-core CPU, how is the KNL performance when processing graphs? ② What is the optimal configuration for a KNL to gain the best performance of graph applications? ③ Which KNL hardware component is underutilized when running a state-of-the-art graph framework? and ④ How to get the optimal configuration and fully utilize the KNL?

### III. Experimental Methodology

In this paper, we adopted and studied six benchmarks including Breadth first search (BF), single source shortest path (SS), graph coloring (GC), K-Core (KC), triangle count (TC) and page rank (PR) from graphBIG [30]. All benchmarks are listed in Table I. Each benchmark contains a CPU OpenMP version and a GPU CUDA version. Due to the absence of PR CUDA code in graphBIG, we adopted a GPU vertex-centric implementation from VertexAPI2 [12]. We compiled codes on GPU by nvcc (V8.0.61) with CUDA-8.0.

| Workload               | Abbr. | State | Description              |
|------------------------|-------|-------|--------------------------|
| Breadth First Search   | BF    | graphBIG (CPU) | computation on graph structure |
| Single Source Shortest Path | SS    | graphBIG (CPU) | computation on graph structure |
| Graph Coloring         | GC    | graphBIG (CPU) | computation on graph structure |
| kCore                  | KC    | graphBIG (CPU) | computation on graph structure |
| Triangle Count         | TC    | graphBIG (GPU) | computation on graph structure |
| Page Rank              | PR    | graphBIG (GPU) | computation on vertex property |

The graph inputs for our benchmarks are summarized in Table I, where Degree denotes the average vertex degree of the graph and IterBF describes the average BF iteration number computed by searching from 1000 random root vertices. roadNet_XX (road) are real-world road networks where most vertices have an outgoing degree below 4. amazon0312 and ego-Twitter (social) are two real-world social networks typically having scale-free vertex degree distribution and a small diameter. delaunay (delaunay) datasets are Delaunay triangulations of random points in the plane that also have extremely small outgoing degrees. hugetrace and hugetric (huge) are meshes taken from individual frames of a dynamic sequence that resembles two-dimensional adaptive numerical simulations. They have extremely small outgoing degree and need a large number of iterations during BF traversals. Like social networks, kroncker (kron) datasets have large average vertex outgoing degree and can be traversed by only several BF iterations. rgg_n_2_x (rgg) are random geometric 2\(^-\) -vertex graphs, where each vertex is a random point in the unit square and edges connect vertices whose Euclidean distance is below \(0.55 \cdot \frac{\ln n}{n}\). These datasets cover a board range of topologies impacting the traversal speed. We selected graph datasets from the University of Florida Sparse Matrix Collection [10] and the Stanford SNAP [23]. We also used the synthetic graph generator [18] in dataset sensitivity studies.

To evaluate our graph benchmarks, we chose and compared three hardware platforms including a CPU, a GPU and a KNL MIC processor. The machine configurations are shown in Table II. The KNL achieves slightly larger peak single point float throughput than the KNL does. However, compared to GDDR5, MCDRAM provides much larger memory bandwidth. In this paper, we aim to understand the performance of multi-threaded graph application kernels, and thus all results ignore disk-to-memory and host-to-device data transfer time. We adopted the Intel VTune Performance Analyzer and the Nvidia visual profiler to collect characterization results.
The GPU primary weakness is the load imbalance problem introduced by its sensitivity to graph topologies in traversal-based graph applications. The GPU achieves the worst performance, only when it suffers from serious load imbalances. Otherwise, the GPU can always obtain the shortest execution time. For BF, the GPU shines on graphs with a small diameter and large vertex degree, e.g., social and kron. In these cases, the KNL secures the second best position, while the CPU is the worst performer. Huge traversal parallelism exists in these graphs with a small diameter and large vertex degree, therefore, the more cores one platform has, the better performance it can achieve. However, compared to the CPU, the GPU gets even longer execution time when searching on graphs with a large diameter and small vertex degree, e.g., road, delaunay, huge, and rgg. The same observation can be also found in [40]. There is little traversal parallelism in graphs with a large diameter and small vertex degree, so the fat OoO CPU cores prevail due to their powerful sequential execution capability. The KNL is still the second best searcher on graphs with poor traversal parallelism. As another traversal-based graph benchmark, SS shares the same trend as that of BF. However, the atomic exchange operations updating vertex distances hurt performance more, when there are more threads working concurrently. So, the KNL always has the longest execution time. For TC, 64 OoO cores with SMT support easily saturate the low DDR4 DRAM bandwidth by generating a large number of cache misses every cycle. Because of the limited DDR4 DRAM bandwidth, the KNL has the worst performance. For KC, the intensive atomic operations modifying the vertex property recording outgoing degree also make the KNL performance the worst among three computing platforms. For GC and PR, the algorithm maintains a large number of active vertices in the frontier resulting in huge processing parallelism. More cores indicate better performance, and thus the KNL is faster than the CPU. The GPU is impaired by serious load imbalances when running GC and PR datasets.

This work does not try to answer which type of hardware platform is the best for parallel graph processing, since the platforms we selected have different hardware configurations such as operating frequencies, core numbers, cache sizes, etc.
micro-architecture details and power budgets. By allocating more hardware resources and power budgets, theoretically speaking, any platform can outperform others. For instance, if a CPU processor is equipped with 64 fat OoO cores operating at 4.2GHz, it may prevail when running most graph applications. Instead, by comparing against the other two platforms, we demonstrate the emerging KNL MIC processor can become one of the most promising alternatives to CPUs and GPUs, because of its encouraging graph processing performance.

B. MCDRAM

The performance difference made by MCDRAM is also exhibited in Figure 4. We configured MCDRAM in both flat mode (KNL-MCDRAM-Flat) and cache mode (KNL-MCDRAM-Cache). When configured MCDRAM as a part in main memory, the performance of BF, SS, GC and KC slightly degrades, since these benchmarks are sensitive to the memory latency rather than the memory bandwidth. Though MCDRAM is able to substantially boost the memory bandwidth and support more concurrent pending memory requests, the access latency of MCDRAM is longer than that of DDR4 DRAM [29]. Only TC and PR are more sensitive to the memory bandwidth and accelerated obviously by MCDRAM, because 64 OoO cores on KNL produce a huge number of simultaneous memory accesses when running these two applications. Compared to KNL-MCDRAM-Flat, KNL-MCDRAM-Cache decreases the KNL performance a little, since the MCDRAM-based L3 cache cannot cover all memory requests and introduces extra DDR4 access latency.

C. Threading

1) Thread Scaling: We show the graph application performance with varying OpenMP thread numbers on the KNL in Figure 5. In the CPU code of each benchmark from graphBIG, there are two kernels to implement the same function. One is serial version for one single thread, and the other is a parallel implementation for ≥2 threads. For some benchmarks such as TC (with road and delaunay datasets), the configuration with two threads is even slower than the serial code with only one thread due to the thread synchronization overhead. With a smaller number of threads (<16), there are not enough working threads to do the task, and thus no benchmark obtains good performance. With an increasing number of threads, the execution time decreases for all benchmarks. However, with a very large number of threads (>256), the execution time significantly rises, since the thread synchronization
overhead dominates again and degrades the performance of most benchmarks. The best performance of each benchmark is typically achieved by 32 ∼ 512 threads. Our real-machine result on thread scaling matches the observation from the previous simulator-based work [2].

However, the previous work [2] does not consider the effect of SMT or oversubscription. Both mechanisms allow multiple independent threads of execution on a core to better utilize hardware resources on that core. To implement SMT, some hardware sections of the core (but not the main execution pipeline) are duplicated to store the architectural state. When one thread is stalled by long latency memory accesses, the SMT stores its state to the backup hardware sections and switches the core to execute another thread. The SMT transforms one physical KNL core to four logic cores, each of which supports one thread. All benchmarks with some datasets, e.g., GC with huge and PR with road, fulfill their shortest execution time by the SMT. In contrast, the oversubscription requires the assistance from software such as OS and the OpenMP library to switch threads, when the running thread is stalled. For applications suffering from extremely intensive memory accesses, like TC with delaunay and PR with huge, the oversubscription supports more concurrent threads and outruns the SMT. When running these applications, compared to the penalty of long latency memory requests, the OS context switching overhead is not significant.

2) The Optimal Thread Number: We define the optimal thread number as the thread number configuration obtaining the shortest execution time for each benchmark. Figure 6 describes the optimal thread number for all applications with all datasets. There is no universal optimal thread number, e.g., the physical core number or the logic core number, that can always have the best performance for all applications with all datasets. Different applications require distinctive optimal thread numbers for the shortest execution time. Moreover, even for the same application, the optimal thread numbers for various graph datasets are different.

3) Thread Placement and Affinity: Because of the OpenMP library, we can configure the thread placement and affinity by KMP AFFINITY=X.granularity=Y. Here, X indicates the thread placement and has two options: assigning thread n + 1 to an available context as close as possible to that of thread n (Compact) or distributing threads as evenly as possible across all logic cores (Scatter). And Y denotes the context granularity and includes two choices: allowing all threads bound to a core to float between different contexts (Core) or causing each thread to be bound to a single context (Thread). The performance comparison between all configurations of thread placement and affinity is shown in Figure 7 where each bar represents one X-Y combination and all bars are normalized to Compact-Core. From Figure 7 we see that Compact configurations with Core and Thread have longer execution time, since Scatter configurations better utilize all physical cores and distribute memory requests evenly among all memory channels. In two Scatter configurations, granularity Thread slightly reduces the execution time, because it scatters threads with consecutive id numbers sharing similar application behaviors to different physical cores. SMT and oversubscription work better when threads with different application behaviors run on the same physical core. When one thread is stalled by memory accesses, the core is switched to other threads that unlikely confront memory instructions in near future due to their distinctive application behaviors.

![Fig. 7. Performance comparison between configurations of thread placement and affinity (normalized to Compact-Core).](image)

![Fig. 8. Performance comparison between various compilation options (normalized to O0).](image)

D. Vectorization

We compiled graph programs with compiler options including O0, O2 and O3 with various vectorization choices. O0 represents the fast compilation without any optimization. Both O2 and O3 start to perform basic loop transformations and the vectorization of MMX and SSEn (n = 2, 3, 4), and O3 applies more advanced loop optimizations. Through AVXm (m = 2 or 512), we compiled applications into AVXm instructions with all other O3 optimizations. NOVEC does not vectorize codes, but practices all other O3 optimizations. The performance of graph benchmarks with different vectorization options is shown in Figure 8. The code without any loop optimizations or vectorization (O0) has the longest execution time, while O2 and O3 outperform O0 on all benchmarks. The implementation of state-of-the-art graph frameworks such as IBM System G [30] do not explicitly represent vertices or edges by floating point or integer arrays. Instead, vertices and edges are encapsulated into lists or maps in graph frameworks, and thus it is difficult for icc to vectorize these data structure. Moreover, basic graph primitives such as graph traversal can barely utilize SIMD instructions. So, compared to NOVEC, AVXm makes trivial performance improvement for the graphBIG implementations of graph applications.

We define the VPU utilization as \( \frac{T_{VPU}}{T_{Total}} \), where \( T_{VPU} \) is the VPU busy time and \( T_{Total} \) denotes the total execution time. The VPU utilization compiled with O3 (and AVXm) is shown in Figure 9. For each graph application, the VPU utilization with any complication options is lower than 30%, indicating the severe underutilization of the SIMD VPUs. The SSE is 128-bit, while the AVX2 (AVX512) is 256(512)-bit. The wider the SIMD instruction is, the longer latency it requires to collect...
its operands, since it has more operands that might be missed in the L1 cache. And hence, AVX512 generally has the largest VPU utilization. The outliers include AVX512 on KC and O3 on PR. For the same source code, more instructions can be compiled by narrower SIMD options. A larger volume of narrow SIMD instructions also increases the VPU utilization.

E. Cache Clustering Mode

The performance comparison between various cache clustering modes is shown in Figure 11. In All-to-All, when there is a L2 miss on a core, it could send this memory request to a tag directory in another quadrant. The tag directory may transfer this request to a third quadrant. Hemisphere (Quadrant) divides the KNL chip into two (four) parts. The main memory accesses from one part are managed by one local memory controller. During a L2 miss, the memory request may be also sent to a tag directory in another quadrant. But the tag directory transfer this request to its only local memory controller. Hemisphere and Quadrant are managed by hardware and transparent to OS. In contrast, SNC-2 (SNC-4) also separates the chip into two (four) parts and exposes each of them as a separate NUMA domain to OS. SNC-4 has the lowest local memory access latency, but longer latency than that of Quadrant when a memory request goes crosses NUMA boundaries. To fully utilize SNC modes, the code must be optimized to have NUMA awareness. Compared to All-to-All and Hemisphere, a core has shorter L2 cache miss latency in Quadrant. Since L2 cache miss rates are high among all graph benchmarks, Quadrant always gains better performance over All-to-All and Hemisphere modes. Benchmarks in the graphBIG suite are not aware of NUMA and suffer from frequent communications between different NUMA regions, so SNC-2 and SNC-4 significantly prolong the benchmark execution time.

F. Execution Time Breakdown

To understand bottlenecks of applications, we show the KNL and CPU execution time breakdown of all bench-

![Fig. 9. VPU utilization when compiled with O3, AVX2 and AVX512.](image_url)

marks with the graph input of delaunay_n19 in Figure 11. delaunay_n19 is a graph with a large diameter and limited traversal parallelism. Bad Speculation is the time stall due to branch misprediction. Retiring denotes the time occupied by the execution of useful instructions. Front-End Bound indicates the time spent by fetching and decoding instructions, while Back-End Bound means the waiting time due to a lack of required resources for accepting more instructions in the back-end of the pipeline, e.g., data cache misses and main memory accesses. We further break the Back-End Bound into L1/2/3 Cache Bounds, DRAM Bound and Other, where X Bound is the time spent in memory accesses in X and Other describes the time stall due to other reasons such as page walk. Graph applications are extremely memory intensive, and thus the Back-End Bound costs the largest portion of execution time on both platforms. On average, it costs 70.88% and 95.24% of the execution time on the KNL and the CPU respectively. Compared to the CPU, it costs the KNL more time to fetch, decode and retire instructions due to its simpler OoO cores. In the Back-End Bound, the KNL spends most of the execution time in accessing L1 cache, while the CPU uses most of the execution time to visit DRAM. The KNL has 64 cores, each of which computes on a smaller number of vertices residing mainly in the L1 cache. But the CPU cache hierarchy has smaller access latency and each core operates on larger working sets containing more vertices mostly stored in DRAM.

G. Dataset Sensitivity Analysis

We generated synthetic graph datasets with varying numbers of vertices, average vertex degrees and vertex distributions by the PaRMAT graph generator [18]. The dataset sensitivity studies on the KNL are shown in Figure 12. The R-MAT value is decided by three parameters a, b, and c. We always enforced b = c. To produce different skewnesses, we adopted the parameters from [43] and set the ratio (rmat) between a and b to 1 (Erdős Rényi model), 3 (real-world case) and 8 (extremely skewed). In Figure 12(a), we fixed the average vertex degree to 20 and rmat to 3. With an increasing number of vertices, it takes longer time for all applications to finish, since they share the vertex centric programming model and the problem size increases. We fixed the vertex number to 100K and rmat to 3 in Figure 12(b). The enlarging average vertex degree also increases the execution time of all graph applications. Particularly, the processing time of TC increases exponentially, since an increasing number of edges produce more triangles. In Figure 12(c) we set the number of vertices...
and average vertex degree to 1K and 20 respectively, and explore the \textit{rmat} value among 1, 3 and 8. For BF and SS that are traversal-based applications, as graph skewness increases and graph eccentricity decreases, the execution time shrinks. Higher-skewed graphs have a smaller diameter resulting in faster traversals. On the contrary, the other graph benchmarks suffer from longer execution time and severer load imbalance problem, when their datasets are more skewed.

V. PRIOR ART

The research area of graph processing has seen efforts in various directions, ranging from clusters [14], [27], [28], [37], [38] to out-of-core [15], [20], [21], [34], [41] and in-memory [31], [33], [35], [40] and MCDRAM, on the performance of multi-threaded graph applications like breadth first search [16], page rank [8] and graph coloring [11]. In future, instead of optimizing a single benchmark, we need to create a fully vectorized graph framework offering AVX512 friendly primitives to support a wide variety of graph applications on KNLs. Moreover, we should incorporate a OS-based [26] or memory-based [25] NUMA aware memory management technique into future graph frameworks, so that the graph applications can benefit from the lowest local memory access latency provided by SNC-4 without incurring large communication overhead between NUMA regions. The future graph frameworks on KNLs also need to be rewritten with heterogeneous memory supporting libraries such as MEMKIND to allocate latency sensitive pages to the DDR4 DRAM and bandwidth sensitive pages to the MCDRAM.

VI. CONCLUSION AND FUTURE WORK

In this paper, we present a performance characterization to show the potential of the KNL processor on parallel graph processing. We further study the impact of KNL architectural innovations, such as many OoO cores, VPUs, cache clustering modes and MCDRAM, on the performance of multi-threaded graph applications. To fully utilize the KNL, in future, we need to overcome the challenges from both hardware angle and software perspective.

First, from the hardware angle, the KNL supplies many architectural features that can be configured by knobs. Different graph applications may favor different configurations. For instance, different graph benchmarks require distinctive numbers of threads to achieve the best performance. Even for the same graph benchmark, various graph inputs need different numbers of threads to attain the shortest execution time. Furthermore, some applications benefit from the high bandwidth MCDRAM, others may be improved by the low latency DDR4 DRAM. Therefore, it is vital to have auto-tuning tools to search the optimal configuration of these knobs to achieve the best performance on KNLs. Previous works propose exhaustive iteration-based optimizations [9], [19] and machine-learning-based tuning techniques [13], [22], [39]. For the emerging KNL processor, we believe that future auto-tuning schemes have to consider not just the MIC architecture, but the heterogeneous main memory system.

Second, from the software perspective, though a state-of-the-art multi-threaded graph framework fully optimized for traditional multi-core CPUs can run on the KNL, we observe that the hardware resources such as VPUs are underutilized and the advanced software-managed architectural features, e.g., the SNC-4 cache clustering mode and the MCDRAM flat mode, may even hurt the performance of graph applications. Previous efforts [7], [8], [16] optimize graph data structures and primitives to better utilize AVX512 instructions and vectorize graph applications like breadth first search [16], page rank [8] and graph coloring [11]. In future, instead of optimizing a single benchmark, we need to create a fully vectorized graph framework offering AVX512 friendly primitives to support a wide variety of graph applications on KNLs. Moreover, we should incorporate a OS-based [26] or library-based [25] NUMA aware memory management technique into future graph frameworks, so that the graph applications can benefit from the lowest local memory access latency provided by SNC-4 without incurring large communication overhead between NUMA regions. The future graph frameworks on KNLs also need to be rewritten with heterogeneous memory supporting libraries such as MEMKIND to allocate latency sensitive pages to the DDR4 DRAM and bandwidth sensitive pages to the MCDRAM.

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