Efficient Hardware Implementation of Incremental Learning and Inference on Chip

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Abstract—In this paper, we tackle the problem of incrementally learning a classifier, one example at a time, directly on chip. To this end we propose an efficient hardware implementation of a recently introduced incremental learning procedure that achieves state-of-the-art performance by combining transfer learning with majority votes and quantization techniques. The proposed design is able to accommodate for both new examples and new classes directly on the chip. We detail the hardware implementation of the method (implemented on FPGA target) and show it requires limited resources while providing a significant acceleration compared to using a CPU.

Index Terms—deep learning, artificial neural networks, incremental, FPGA, hardware.

I. INTRODUCTION

Deep Neural Networks (DNNs) based methods offer state of the art performance in many domains such as computer vision and speech recognition [11]. They rely on large quantities of available data and hundreds of millions of trainable parameters, which require significant memory capacities and computational power. As a consequence, their implementation on embedded systems is a challenge. Several approaches have been introduced aiming at reducing DNNs size and complexity, such as using product quantization (PQ) to factorize DNNs weights [2], [3], binarizing both DNNs weights and activations [4]–[6], pruning DNN connections [7], [8], or replacing the spatial convolution by a shift operation followed by 1 × 1 convolution [9], [10]. These methods ease the implementation of big and complex DNNs on embedded systems [11]–[13] as far as the inference part is concerned. However, because it requires storing the whole dataset and causes increased complexity, the training of DNNs is in most cases still performed offline.

In the literature multiple works have tackled the question of Learning On Chip (LOC) [14]–[17]. In the context of deep learning, a key problem is the use of the stochastic gradient descent algorithm, that requires accessing the training dataset multiple times, and thus storing all of it in memory. Methods that do not require storing the whole dataset in memory are referred to as “incremental learning” in the literature. An incremental learning [18]–[25] solution is defined as learning sequentially one (or few) example(s) at a time without the need to access previously processed data. Unfortunately the incremental part of the learning process comes with a loss in accuracy that might be too damageable for some applications.

Recently authors have proposed a solution named Transfer Incremental Learning with Data Augmentation (TILDA) to considerably increase the accuracy of incremental learning techniques by combining transfer learning with quantization techniques and majority votes [26]. The term “transfer learning” refers to the use of pre-trained DNNs to obtain new representations of input signals [27], [28]. In this work, we propose a hardware implementation of TILDA [26]. We show that the proposed hardware solution requires limited resources while providing substantial gains in processing time compared to a CPU. We also show in Table I that the method is able to compete with state-of-the-art non-incremental transfer learning alternatives.

II. PROPOSED METHOD

Let us first introduce notations (extracted from [26]). TILDA is made of four main ingredients: 1) a pre-trained and fixed DNN to perform feature extraction of signals, 2) a vector splitting procedure to project features into low dimensional subspaces, 3) an assembly of NCM-inspired classifiers applied independently in each subspace and 4) a data augmentation scheme to increase accuracy of the classifying process.

The first step consists in performing transfer using the internal layers of a pre-trained DNN acting as a generic feature extractor to compute the feature vector \( \mathbf{x}^m \), corresponding to the input signal \( \mathbf{s}^m \). Since there is already a lot of literature on the subject of hardware implementation of the inference of DNNs [11]–[13], we disregard this first step in the implementation described in this paper and directly consider processing the vector \( \mathbf{x}^m \).

Then, each feature vector \( \mathbf{x}^m \) is split into \( P \) subvectors of equal size denoted \( \{ \mathbf{x}_{c,p}^m \}_{1 \leq p \leq P} \). During training, for each class \( c \) and each subspace \( p \), we produce \( k \) anchor vectors \( \mathbf{y}_{c,p} = [\mathbf{y}_{c,p,1}, ..., \mathbf{y}_{c,p,k}] \) initialised with 0s, and their associated counters \( N_{c,p} = [n_{c,p,1}, ..., n_{c,p,k}] \) also initialised by 0s.

Then, each time an input training vector is processed, an anchor vector is identified to be updated. The update simply consists of computing a new anchor vector obtained as a barycenter of the old one with weight given by its counter and the input subvector with weight 1, then incrementing the counter. This procedure is detailed in Algorithm I.

During the prediction phase, for each subspace, anchor vectors are divided by their corresponding counters and used
Algorithm 1 Incremental Learning of Anchor Subvectors

Input: streaming feature vector $x^m$

for $p := 1$ to $P$ do
  for $i := 1$ to $k$ do
    $d_i = \|x_p - y_{c,p,i}\|_2$
    $R_i = d_i n_{c,p,i}$
  end for
  $\hat{k} = \arg\min R_i$
  $y_{c,p,\hat{k}} \leftarrow y_{c,p,\hat{k}} n_{c,p,\hat{k}} + x^m_{c,p}$
  $n_{c,p,\hat{k}} \leftarrow n_{c,p,\hat{k}} + 1$
  $y_{c,p,\hat{k}} \leftarrow y_{c,p,\hat{k}} / n_{c,p,\hat{k}}$
end for

for nearest-neighbour search. More precisely, each subpart $x_p$ obtained from input signal $s$ is weakly classified using the nearest-neighbour anchor vector in part $p$. Finally, a majority vote is performed to aggregate these weak classifications.

To further improve the method performance, data augmentation is used at both prediction and training phases. The training data-augmentation is used to artificially enrich the training dataset, whereas the prediction data-augmentation is used to obtain multiple decisions that are aggregated using a second majority vote.

III. HARDWARE IMPLEMENTATION

In this paper, we assume that a generic feature extraction is performed by an external CPU, and provides feature vectors $x^m$ to the FPGA. Consequently, we introduce a hardware implementation to compute the incremental classifier part.

A. Data Quantization

All data and signals were quantized on $n = 18$ bits fixed-point representation, which enables to use only 1 dedicated multiplier block (Xilinx DSP Block) for each multiplication. In addition, we perform local quantization by setting the number of integer bits $m \leq n$ at each step of the algorithm. In the subsequent figures depicting hardware blocks, we include the width of each bus in italics. The number $m$ of integer bits at each step of the implementation changes as follows:

- Feature-vector, Anchor-vector: $m = 5$
- Distance: $m = 10$
- Address, Counter: $m = 18$
- Distance+Counter: $m = 16$
- Anchor-vector+Counter: $m = 10$
- Anchor-vector+Feature-vector: $m = 10$

B. Hardware architecture

An overview of the hardware architecture is presented in Figure 1. Each input feature vector $X^m$ is split into $P$ subvectors, and processed on $P$ Processing blocks in parallel. Each processing block $p$ gets a subvector, as well as an address that is generated by the counter L-P block. Each processing block outputs the class associated to a subvector. The obtained classes $(c_p)_{1 \leq p \leq P}$ are used to compute a Parallelized Majority vote, and classify the input feature vector $X^m$. Finally, Sequential Majority vote is used to output the class of the original signal when data augmentation is performed to classify unlabelled data.

1) Processing block: We use this component to learn or classify a subvector. This component has three inputs: feature subvector, learning-processing signal (L-P), and address (generated by Counter/L-P) and has only one output, the obtained class of a feature subvector one-hot encoded on $C$ bits, where $C$ is the number of classes. Given a feature subvector $x^m_p$, we first compute the euclidean distance between $x^m_p$ and $y^i_p$ (where $y^i$ is the first anchor vector addressed by address generator), multiply the distance by anchor subvector’s counter, and store the result in the register $r_p$ in Compare Distance block. We
repeat the same process using each $(y_p^j)_{i \leq j \leq i + k}$, compare the result with the $r_p$ value, and store the smallest one in $r_p$. Finally, Compare Distance block outputs the index of the nearest $y_p^j$ from $x_m$. Given this index, Distance register outputs the same index and the class of anchor subvector corresponding to the index. It also outputs a validation signal $val$, which is equal to 1 when the nearest $y_p^j$ from $x_m$ has been determined. During learning process ($L-P=1$), when $val$ signal is equal to 1, R-W becomes 0 and we use the feature subvector and index from Distance Register block through multiplexer to modify the memory content according to Algorithm 1. The inverse of indexes are stored in Look-up tables and multiplied by the output of the Distance Register block (cf. Figure 2).

2) Counter/L-P: This component is an ordinary counter, which counts from 0 to Modulo value. Counter/L-P uses a signal (L-P) which is equal to 1 when learning, and 0 when test. Modulo value is set to $k$ when learning, to generate only $k$ different addresses in order to read only anchor vectors of a specific class. During test, it is set to $Ck$, in order to read all anchor vectors.

3) Memory: The Memory block contains two memory blocks (Xilinx UltraRam technology), one to store anchor vectors (URAM A-V), and the other one to store corresponding counters (URAM Counters). Addresses are provided by Counter/L-P. It is also performs the multiplication/division of an anchor vector and its corresponding counter, and the sum between an anchor vector and an input feature vector.

4) Majority vote: Class vectors $e^p$ are one-hot encoded on $C$ bits. Parallel Majority vote computes a bitwise addition over all $(e^p)_{1 \leq p \leq P}$ vectors. The $C$ results are compared sequentially, to obtain the class index $c$ attributed to the unlabelled feature vector $x_m$. Sequential Majority vote is computed only when using data augmentation. This block takes as input only one class vector $e^p$ and performs an addition between each bit of the input class vector and the $c$ inner register. A final comparison is performed between each $c$ results, which outputs a global predicted class vector.

During training, when compare distance block compares two distances, compute distance block computes a new distance between input feature vector and another anchor vector. Thus, the learning phase is $k + 3$ clock cycles per feature vector. Precisely, it takes $k$ cycles to compute/compare distances, 1 cycle to multiply anchor vector with its corresponding counter, 1 cycle to add the result with the input feature sub vector and increment its counter and 1 cycle to divide the result by this incremented counter. During classification process, Sequential majority vote needs at least $R$ clock cycles $R$ represents the number of feature vectors resulting form data augmentation) to give an output, Parallel majority vote needs at least $CkR$ clock cycles to classify $R$ feature vectors, and Processing block is classifying subvectors of $R$ input feature vector during $CkR$ clock cycles. In the proposed architecture, These three blocks work at the same time, thus $CkR$ cycles are needed to classify an unlabelled feature vector, with $CkR$ cycles to compute distances, repeated $R$ times to classify all feature vectors resulting from data augmentation.

![Fig. 2. Hardware architecture of Processing block.](image)

| TABLE I | ACCURACY COMPARISON OF TILDA, MLP AND SVM |
|----|----|----|----|----|
| TILDA | TILDA-DA | MLP | SVM |
| CIFAR100 | 69.6% | 65.16% | 68.6% | 67.6% |
| CIFAR10 | 88.7% | 86.6% | 90% | 89.2% |
| Imagenet50 | 76% | 74.4% | 75.2% | 75% |

| TABLE II | FPGA RESULTS FOR THE OUR PROPOSED ARCHITECTURE ON VU13P (XCVU13P-FGG2104-1-E) ($T = 2048$, $P = 16$, $K = 30$) |
|----|----|----|----|----|----|
| Proposed method | 13 |
| Memory usage (bits) | 11059488 | 6553600 |
| Look-up Tables (LUT) | 152546 | 95654 |
| DSP | 2064 | 2048 |
| Maximum frequency (MHz) | 208 | 204 |
| Learning delay (ns) | 158.2 | 5 |
| Classifying delay (ns) | 1442 | 1470 |
| Energy consumption (W) | 7 | 13 |
| Accuracy (%) | 87 | 82 |

IV. RESULTS

TILDA achieves an accuracy on par with a MultiLayer Perceptron (MLP) with one hidden layer of 1024 units or a Support Vector Machine classifier (SVM) (c.f. Table I).
TILDA-DA is TILDA method without data augmentation and Imagenet50 represents 50 ImageNet classes which have not been used to train the CNN. Unlike MLP and SVM, TILDA is an incremental method which learns one example at the time, and does not perform an expensive computational backpropagation during training. Moreover, it should be noted that TILDA outperforms other incremental learning methods while using less computational resources.

The proposed hardware architecture has been implemented and validated by software simulation over a batch of examples. We provided synthesis results of the architecture on a Xilinx Ultra Scale VU13p (xcvu13p-figd2104-1-e) Field Programmable Gate Array (FPGA) (Table I).

Performance estimates are given for the CIFAR10 for $P = 16$, $K = 30$ and $C = 10$, yielding an accuracy of 89.7%/87.7% with/without data augmentation, instead of 88.7%/86.6% obtained for 32 bits encoding. To obtain feature vectors, we use inception V3 (29) ($T = 2048$). 2048 DSPs are used to compute distances and $P = 16$ more to multiply/divide anchor vectors by their corresponding counters. Power consumption and maximum clock frequency of the whole system are estimated to about 8 Watts and 208 MHz. The estimated time needed to learn/classify an input vector is $158.2/1442$ ns at maximum clock frequency, corresponding to an acceleration factor of $10^4$ when compared with a software simulation delay using an 17 870 (2.93 GHz) processor.

V. CONCLUSION

In this paper we introduced an architecture for incremental learning on chip. As such, the proposed method is able to learn one example at a time, and does not require to store the whole dataset to perform training. The proposed architecture allows an embedded system to accommodate new data from scratch and classify previously unlabelled inputs, and more important, performs the learning on chip. Future work will introduce hardware architecture and implementation of the pretrained CNN to propose a complete embedded solution.

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