In this work, a nanowire p-type metal–oxide–semiconductor field-effect transistor (PMOSFET) coaxially having a Si core and a Ge peripheral channel is designed and characterized by device simulations. Owing to the high hole mobility of Ge, the device can be utilized for high-speed CMOS integrated circuits, with the effective confinement of mobile holes in Ge by the large valence band offset between Si and Ge. Source/drain doping concentrations and the ratio between the Si core and Ge channel thicknesses are determined. On the basis of the design results, the channel length is aggressively scaled down by evaluating the primary DC parameters in order to confirm device scalability and low-power applicability in sub-10-nm technology nodes.

1. Introduction

Ge is rapidly regaining considerable interest as an important semiconductor material for applications to high-speed low-power integrated circuits (ICs). Ge has approximately 4.2- and 2.6-fold higher bulk hole and electron mobilities, respectively, than Si, and a high Si CMOS processing compatibility.1 In particular, Ge is a promising channel material for p-type metal–oxide–semiconductor field-effect transistors (PMOSFETs) since its hole mobility is the highest among the well-known group IV and III–V semiconductor materials that have been used for device fabrications [1]. Although Ge is an indirect-bandgap material, it has a higher radiative recombination probability than Si, since Ge has a local minimum at $k = 0$ in the momentum space, which improves the probability of spontaneous emission. The electron affinities of Si and Ge are 4.0 and 4.05 eV, respectively, and the energy bandgap ($E_g$) of Ge is about half that of Si. The smaller $E_g$ of Ge allows further scaling of drive voltage.4 Also, its relatively low melting point leads to the low-temperature activation of source/drain (S/D) dopants at 400–500 °C,5,6 which facilitates the formation of shallow junctions and necessitates a high-$x$/metal gate stack that is usually constructed at a low thermal budget. Owing to these virtuous features, there has been consistent effort in realizing both electron and optical devices based on Ge including nanowire Ge PMOSFETs, Ge-on-insulator (GOI) MOSFETs, Ge light-emitting diodes (LEDs), and lasers.3,4,7–13 To obtain a GOI substrate as the platform for Ge electronics, a Ge condensation technique has been employed as illustrated in Fig. 1.14–19 Although a silicon-on-insulator (SOI) substrate is a prerequisite in obtaining the GOI substrate through the condensation technique, SOI can be replaced with bulk Si in preparing the starting material to reduce the cost.20,21 By either the partial or whole condensation of Ge out of the SiGe alloy epitaxially grown in the geometrically confined Si area, the active regions in various shapes fabricated from Ge can be constructed easily.

In this work, a novel nanowire Ge PMOSFET coaxially having a Si core and a Ge peripheral channel is proposed and optimally designed. The Ge channel can be formed through a Ge condensation technique on a Si nanowire. Owing to the benefits from the device structure and channel material, a stronger gate controllability, a higher current drivability, and a more robust immunity against short-channel effects (SCEs) are expected from the proposed device.22,23 The nanowire Ge PMOSFET is optimally designed by rigorous device simulations24 and its potential applicability in sub-10-nm logic technology nodes is evaluated.

2. Device structure and simulation approach

Figures 2(a) and 2(b) show the schematic of the proposed device and the energy-band diagram along the cutline on a plane passing through the nanowire center. The material and structural configurations of the device are demonstrated in

![Fig. 1.](Color online) Schematic view of Ge condensation processing.

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Fig. 2. (Color online) Proposed Ge nanowire MOSFET. (a) Bird’s eye view of the device structure. Here, $x$ is the Ge thickness, which is controlled from 0 to 10 nm in the simulation. (b) Energy-band diagram from the cutline on the plane passing through the nanowire center obtained by simulation.

Although the $E_g$ of Si and Ge are 1.12 and 0.66 eV, respectively, at room temperature, the large difference in $E_g$ is mostly projected to the valence band offset (VBO) since Si and Ge have very small electron affinity differences of 4.0 and 4.05 eV, respectively. By making use of these properties of Si and Ge heterojunction, holes can be effectively confined in the Ge region, which will be the channel material with high hole mobility. By electrical isolation between Si and Ge through the large VBO, it is not substantially probable that the Si core acts as a leakage path for hole current conducting through the Ge channel.

To obtain simulation results with higher accuracy and reliability, various models were adopted simultaneously, including the vertical and parallel electric-field-dependent mobility model, concentration-dependent mobility model, band-to-band tunneling model developed by Hurkx et al., bandgap narrowing model, Fermi–Dirac statistics, and quantum-mechanical model. A two-dimensional (2D) rectangular structure was constructed first and rotated to build a three-dimensional (3D) structure having cylindrical symmetry to include more supporting models available only in 2D simulations and obtain a better convergence of numerical calculations. To suppress the S/D parasitic resistance and meet the gate pitch requirement, the distance between the S/D contacts to the gate edge was fixed at 20 nm. The saturation currents obtained from the design work are higher than those suggested by the most recent technology roadmap (ITRS), as will be shown in a later section. Furthermore, empirical saturation velocities of electrons and holes in Ge were employed in the simulations for a higher reliability.

The S/D doping concentration was optimized in terms of DC and AC parameters including on- ($I_{on}$) and off-state ($I_{off}$) currents, current ratio ($I_{on}/I_{off}$), drain-induced barrier lowering (DIBL), subthreshold swing ($S$), and transconductance ($g_m$). The simulated device channel length ($L_g$) and Si:Ge thickness ratio were fixed at 50 nm and 5 nm : 5 nm, respectively. The p-type (p${}^+$) S/D doping concentration was controlled from $10^{16}$ to $10^{20}$ cm$^{-3}$ for the optimization. The doping concentration of the n-type channel was fixed at 1$\times$10$^{15}$ cm$^{-3}$. $I_{on}$ and $I_{off}$ are defined as the currents where the gate voltage ($V_{GS}$) is equal to $-0.85$ and 0 V, respectively, at the on-state drain voltage ($V_{DS}$). The drive voltage ($V_{DD}$) of $-0.85$ V has been assumed in accordance with the requirements for low-power (LP) and high-performance (HP) applications in the most recent technology roadmap. The ratio was calculated to evaluate logic switching characteristics. There have been two conditions of drain biases: one is low at $-50$ mV and the other is high at $V_{DS} = V_{DD} = -0.85$ V in tracing the transfer curves. Threshold voltage ($V_{th}$) was extracted by the constant current method at $I_D = 10^{-4}$ A, and DIBL was obtained as the difference in $V_{th}$ at high and low $V_{DS}$ values. $S$ was calculated to be the reciprocal of the maximum slope in the subthreshold region. Furthermore, to have a glimpse of the AC performance, the maximum available transconductance ($g_{m,Max}$) values was extracted under each S/D doping condition. Although the $g_m$ of a MOSFET is extracted at a certain operating point in many cases, how large $g_m$ can be possibly obtained from a device over a wide range of gate operating voltage without pinning to a specific $V_{GS}$ may provide a higher practicability for general purposes, particularly when it comes to an unknown device. Thus, the maximum available $g_m$ ($g_{m,Max}$) is more importantly considered in this work.

The Si:Ge thickness ratio was optimized through device simulations. The doping concentration of $5 \times 10^{17}$ cm$^{-3}$ was chosen from the permissible range in optimizing the Si:Ge thickness ratio considering the convenience in fabrication and the high device reliability. Here, the total thickness of Si and Ge regions was fixed at 10 nm for securing a small foot-print. Simulations have been performed with the variation of Ge thickness from 0 to 10 nm by 1 nm steps. In the case of a 10-nm-thick whole Si channel, since the device is already completely turned off at $V_{GS} = -0.4$ V, the transfer curve was extracted by sweeping $V_{GS}$ from 0.2 down to $-1.5$ V. The simulated device $L_g$ was fixed to be 50 nm. The Si:Ge thickness ratio was optimized in terms of DC and AC parameters including $I_{on}$ and $I_{off}$, $I_{on}/I_{off}$, DIBL, $S$, and $g_{m,Max}$ in the same manner as that in which the first simulations were performed.

Finally, $L_g$ was controlled from 200 down to 7 nm under the thickness condition of Si : Ge = 2 nm : 8 nm, selected from the permissible thickness ratio range. By carrying out the series of simulations, the scalability of the proposed device was closely investigated through $I_{on}$ and $I_{off}$, $I_{on}/I_{off}$,


DIBL, $S$, and $g_m$ while emphases were made on performance optimization in the first and second tasks.

### 3. Results and discussion

#### 3.1 Optimization of S/D doping concentrations

Figure 3 shows the $I_D$–$V_{GS}$ transfer curves of the proposed nanowire Ge PMOSFETs with different S/D doping concentrations at $V_{DS} = V_{DD} = -0.85$ V. The S/D doping concentrations are $10^{16}$, $10^{17}$, $10^{18}$, $5 \times 10^{18}$, $10^{19}$, $2 \times 10^{19}$, $3 \times 10^{19}$, and $10^{20}$ cm$^{-3}$. A very low doping concentration is not capable of drawing a high $I_{on}$ and also an excessively high doping concentration is not desirable for the suppression of $I_{off}$. Figures 4(a) and 4(b) show $I_{on}$ and $I_{off}$ and $I_{on}/I_{off}$, respectively. For a better current drivability, the S/D doping concentration must be higher than $5 \times 10^{18}$ cm$^{-3}$, and for a lower $I_{off}$, a doping concentration of $10^{19}$ cm$^{-3}$ or lower should be designed in order to minimize the leakage caused by band-to-band tunneling. The maximum $I_{on}/I_{off}$ ratio is obtained at the doping concentration of $5 \times 10^{18}$ cm$^{-3}$. $I_{on}$ increases faster than $I_{off}$ as the doping concentration increases until reaching $5 \times 10^{18}$ cm$^{-3}$, while $I_{off}$ increases faster than $I_{on}$ above this point, which provides an optimum condition for maximizing the $I_{on}/I_{off}$ ratio at $5 \times 10^{18}$ cm$^{-3}$. Figure 5 depicts DIBL, where the reference current for extracting $V_{th}$’s by the constant current method is $I_{D} = 10^{-8}$ A. As can be confirmed by Figs. 4(a) and 4(b), $I_{off}$ becomes impermissibly high at the S/D doping concentration of $10^{20}$ cm$^{-3}$. The mathematically extracted DIBL is impractically large, and thus, it is determined that the S/D doping concentration is required to be no higher than $3 \times 10^{19}$ cm$^{-3}$ for maintaining a small DIBL of around 30 mV/V. Figure 6 demonstrates $S$ as a function of S/D doping concentration. $S$ does not notably degrade as the doping concentration increases but is tied to a plausibly small value near 60 mV/dec, the theoretical limit in the presence of thermionic emission at 300 K, at doping concentrations of $10^{19}$ cm$^{-3}$ and below. $S$ (mV/dec) is defined as

\[
S = \ln 10 \cdot \frac{m k T}{q} = \ln 10 \cdot \frac{k T}{q} \left( 1 + \frac{C_{dm}}{C_{ox}} \right) \cong 60 \left( 1 + \frac{C_{dm}}{C_{ox}} \right).
\]

Here, $k$ is the Boltzmann constant, $T$ is the temperature in K, and $q$ is the unit charge in C. $C_{dm}$ and $C_{ox}$ are the depletion and gate oxide capacitances seen by the gate, respectively. The radical extension of depletion regions from S/D ends toward the channel center occurs as the S/D doping concentration increases, which makes the channel less sensitive to the gate, and the change in depletion length by $V_{GS}$ decreases. The thinner depletion by the gate increases $C_{dm}$ and the swing becomes worse as shown in Fig. 6 and the radical degradation is observed above $10^{19}$ cm$^{-3}$. $g_{m,Max}$ shows a monotonic increase with S/D doping concentration, as shown in Fig. 7. A high $g_{m,Max}$ reaching $10^{-4}$ S would be warranted at $10^{18}$ cm$^{-3}$ and above. The first derivative of the $I_D$–$V_{GS}$ curve is located at $V_{GS}$ values smaller than $-0.85$ V ($|V_{GS}| < 0.85$ V) for the devices with S/D doping concentrations below $10^{19}$ cm$^{-3}$. However, above this doping concentration, there is no local maximum in the $g_m$–$V_{GS}$ curve but $g_m$ monotonically increases

![Fig. 3. (Color online) Transfer curves of the Ge nanowire MOSFETs with different S/D doping concentrations.](image-url)

![Fig. 4. (Color online) Current characteristics of the Ge nanowire MOSFET. (a) $I_{on}$ and $I_{off}$ and (b) $I_{on}/I_{off}$ ratio as functions of S/D doping concentration.](image-url)

![Fig. 5. (Color online) DIBL as a function of S/D doping concentration of the Ge nanowire MOSFET.](image-url)
as $V_{GS}$ becomes more negative. Although all the $g_{m,\text{Max}}$ values at moving $V_{GS}$’s are provided in the figure to demonstrate all the possibilities, those obtained from S/D doping concentrations higher than $10^{19}\text{ cm}^{-3}$ might not be substantially practical in designing for low-power applications since the local maximum $g_{m}$’s are located even below $V_{GS} = -1.0\text{ V}$, which is lower than the targeted drive voltage of $-0.85\text{ V}$.

### 3.2 Optimization of thickness of Ge peripheral channel

Considering the variations of the DC and AC parameters of the proposed nanowire Ge PMOSFET including $I_{on}$, $I_{off}$, $I_{on}/I_{off}$, DIBL, $S$, and $g_{m}$, the optimized device performance is expected in the S/D doping concentration range between $5 \times 10^{18}$ and $10^{19}\text{ cm}^{-3}$ at a thickness ratio of Si core : Ge channel $= 5\text{ nm} : 5\text{ nm}$. Here, the permissible S/D doping concentration is chosen to be $5 \times 10^{18}\text{ cm}^{-3}$ from the design window for optimizing the ratio between the Si core and Ge channel thicknesses at the given total semiconductor nanowire radius of 10 nm. Taking the higher process viability and lower performance deviation into account, the lower limit of $5 \times 10^{18}\text{ cm}^{-3}$ has been selected as an optimal S/D doping concentration.

Transfer curves from the devices with different Ge channel thicknesses are shown in Fig. 8 with the S/D doping concentration of $5 \times 10^{18}\text{ cm}^{-3}$ at $V_{DS} = -0.85\text{ V}$. The total nanowire radius (Si core + Ge peripheral channel thicknesses) and $L_g$ are fixed to be 10 and 50 nm, respectively. The device with the whole Si channel (Ge 0 nm : Si 10 nm) has a lower $I_{off}$ ($I_{D}$ at $V_{GS} = 0\text{ V}$) owing to the lower probability of band-to-band tunneling by the relatively large $E_g$ of Si ($1.12\text{ eV}$) compared with that of Ge ($0.66\text{ eV}$). On the other hand, its current drivability is lower than that in the case where the Ge channel is beneath the gate oxide since the $V_D$ of the whole-Si-channel device significantly shifts toward the left-hand side, which is also not desirable for realizing low-voltage operation. The nanowire PMOSFETs with Ge peripheral channels show two decades higher $I_{off}$ than that of the whole-Si-channel device, and it is confirmed from Fig. 8 that a larger portion in Ge thickness has an effect of reducing $I_{off}$. Figure 9(a) depicts $I_{on}$ along with $I_{off}$ with increasing Ge thickness. $I_{on}$ monotonically increases and saturates above the Ge thickness of 3 nm as shown in the figure. At the same time, $I_{off}$ decreases in this region with Ge thickness. To achieve a higher current drivability and better switching characteristics, Ge thicknesses of 3 nm and above would be desirable in the design optimization, as can be confirmed from Fig. 9(a). The $I_{on}/I_{off}$ ratio in the case of embedding the Ge channel is prominently higher than that in the case of employing only Si in the nanowire channel and it increases with Ge thickness ratio as depicted in Fig. 9(b). The gate metal workfunction is fixed to be $4.08\text{ eV}$ for a fair comparison and an efficient simulation design, and the corresponding metal can be Al having a clean CMOS processing compatibility. Figure 9(c) shows the potential contours in the devices with Ge thicknesses of 3 nm (left) and 8 nm (right). Compared with the case of 3 nm thickness, that of 8 nm demonstrates a high potential in the Ge channel region. The high potential originates from the workfunction difference between the poorly doped Ge channel and the gate. As shown in Fig. 9(d), holes are the majority carrier making up the off-state current. Thus, a higher potential makes the holes in the source junction see a higher potential energy barrier in the channel direction, and the source hole injection into the channel by diffusion becomes more difficult in the case of the 8-nm-thick Ge channel. The fundamental reason for this lies in the fact that Ge has a higher electrical permittivity than Si, by which Ge experiences smaller potential gradients in the radial direction. Figure 10 plots DIBL as a function of Ge thickness. DIBL is kept to be as small as near $13\text{ mV/V}$, which reveals that the device structure and material design present strong immunity against the SCEs. Also, the variance in DIBL is confined to a small window, within $5\text{ mV/V}$, over the entire controlled Ge thickness range. Figure 11 shows $S$ as a function of Ge thickness, where the distribution is concentrated plausibly near $60\text{ mV/dec}$, the theoretical lower
limit in the drift-diffusion carrier transport, for all the simulated Ge thicknesses up to 10 nm. $g_{m,\text{Max}}$ is depicted as a function of Ge thickness in Fig. 12. $g_{m,\text{Max}}$ demonstrates a monotonic increase in the entire region, except in the case of the whole-Si-channel device, and the Ge thickness for an optimal design is suggested to be above 5 nm where $g_{m,\text{Max}}$ higher than 40 $\mu$S is obtained.

Obtaining a Ge channel thicker than 5 nm without dislocation or defect sites can be challenging since the critical thickness of Ge on Si is around 5 nm. However, the proposed device in this work can be fabricated by Ge condensation with only minimal dislocation and defect formation. Also, the critical thickness of the Ge epitaxy layer on the Si nanowire structure is enhanced and the stress decreases as the Ge layer becomes thicker. Owing to the lack of systematic experiments on critical thickness in the case of condensation processing, it can be safe to reference the results of the epitaxial growth of Ge on Si, and a problematic thickness can be discarded in an actual device realization. Since the nanowire channel surface is basically omnidirectional, the highly angle-dependent strain effects on the on- and off-state current characteristics through the band structure modification become complicated. The simulation results in this work can provide guidelines in designing the device performance without fully including the interfacial status and the strain effects at this moment. Moreover, studies on more realistic phenomena affecting the device performances should be carried out as one of the related future works.

3.3 Evaluation of length scalability of the proposed Ge PMOSFET

From the results of the optimization of Ge thickness, the common set of thickness ranges determined by respective parameters indicates that channels of 5 nm thickness and above should be permissible in designing the proposed device. Si core : Ge peripheral channel = 2 nm : 8 nm is cho-

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Fig. 9. (Color online) Current characteristics and graphical analysis results of the Ge nanowire PMOSFET. (a) $I_{on}$ and $I_{off}$ and (d) $I_{on}/I_{off}$ ratio as functions of Ge channel thickness. (c) Potential contours at $V_{GS} = 0$ V and $V_{DS} = -0.85$ V at Ge thicknesses of 3 (left) and 8 nm (right). (d) Electron and hole current densities for Ge thicknesses of 3 and 8 nm.
to ensure a high $g_{m,\text{Max}}$ to evaluate the length scalability down into the sub-10-nm regime. The optimum S/D doping concentration is constantly assumed to be $5 \times 10^{18} \text{ cm}^{-3}$. Figure 13 shows the transfer curves from the devices with different $L_g$’s ranging from 200 down to 7 nm (200, 100, 50, 30, 20, 10, and 7 nm). As $L_g$ decreases, the transfer curves tend to be right-shifted by SCEs including DIBL and degradation in $S$ as examined previously. The same set of device parameters is investigated as $L_g$ is scaled down. Both $I_{on}$ and $I_{off}$ increase as $L_g$ decreases as shown in Fig. 14(a). The $I_{on}/I_{off}$ ratio is invariant with $L_g$ from 200 down to 50 nm but remarkably rolls off from 50 to 7 nm, generally showing a monotonic decrease as shown in Fig. 14(b). Normalized saturation currents at each $L_g$ are extracted as depicted in
Fig. 14(c) to confirm whether the current drivability of the proposed device meets the requirements suggested by the most recent technology roadmap. The currents are normalized by the channel diameter (Si core + Ge channel) of 20 nm. The nominal values of normalized saturation currents are listed in Table I. Also, the first and second rows in Table II show the targeted saturation current of the Ge multi-gate (MuG) PMOSFET and the ratio between a saturation currents of the Ge MuG NMOSFET and PMOSFET. A simple calculation leads to the saturation current requirement of the Ge MuG PMOSFET as inserted in the third row. It is confirmed from the tables that the proposed device in this work satisfies the requirements. Also, it is revealed that the S/D parasitic resistances have been well suppressed and do not become a substantial hindrance in meeting the requirements. Figure 15 depicts DIBL as a function of $L_g$ of the Ge nanowire MOSFET.

![DIBL as a function of $L_g$ of the Ge nanowire MOSFET.](image)

Table I. Saturation current of the proposed Ge nanowire PMOSFET as a function of $L_g$.

| $L_g$ (nm) | $I_{d,sat}$ ($\mu A/\mu m$) |
|-----------|-----------------------------|
| 7         | 558.54                      |
| 10        | 506.49                      |
| 20        | 428.48                      |
| 30        | 402.87                      |
| 50        | 367.80                      |
| 100       | 299.86                      |
| 200       | 218.02                      |

Table II. Calculated prediction of saturation current of Ge PMOSFET based on Ge MuG NMOSFET by ITRS.28)

| Year   | $I_{d,sat}^a$ ($\mu A/\mu m$) | $I_{d,sat}^b$ ($\mu A/\mu m$) |
|--------|-------------------------------|-------------------------------|
| 2016   | 589                           | 1.24                          |
| 2017   | 574                           | 1.22                          |
| 2018   | 556                           | 1.21                          |
| 2019   | 550                           | 1.20                          |
| 2020   | 533                           | 1.19                          |
| 2021   | 537                           | 1.18                          |
| 2022   | 461                           | 1.16                          |
| 2023   | 458                           | 1.15                          |
| 2024   | 395                           | 1.14                          |
| 2025   | 393                           | 1.13                          |
| 2026   | 334                           | 1.12                          |
| 2027   | 295                           | 1.11                          |

a) n-channel b) p-channel

Fig. 16. (Color online) $S$ as a function of $L_g$ of the Ge nanowire MOSFET.

![$S$ as a function of $L_g$ of the Ge nanowire MOSFET.](image)

Fig. 17. (Color online) $g_{m,Max}$ as a function of $L_g$ of the Ge nanowire MOSFET.

![$g_{m,Max}$ as a function of $L_g$ of the Ge nanowire MOSFET.](image)

Here, $W$ is the channel width and $C_{ox}$ is the oxide capacitance. The smaller $g_{m,Max}$ in the region of $L_g < 30$ nm is attributed to the weaker gate controllability over the channel and the smaller carrier responsivity to the gate. For the region of $L_g > 30$ nm, decreasing $g_{m,Max}$ results from the lower current drivability inversely proportional to $L_g$ as can be predicted using Eq. (2). However, $g_{m,Max}$ is generally plotted to be higher than 30 $\mu S$ and $g_{m,Max} = 31.95 \mu S$ is obtained at $L_g = 7$ nm.

$$g_m \equiv \frac{W}{L_g} \mu C_{ox} V_{DS} \left( \frac{W}{L_g} \right)^2 \left( \frac{W}{L_g} C_{ox} (V_{GS} - V_{th}) \right).$$

(2)
4. Conclusions

In this work, we proposed and optimized a nanowire Ge PMOSFET having a Si core and a Ge peripheral channel by device simulations. The criteria for device optimization were primary DC and AC parameters including $I_{on}$, $I_{off}$, $I_{on}/I_{off}$ ratio, DIBL, $S$, and $g_m$. The S/D doping concentration and Si:Ge thickness ratio were optimized, and then, the scalability of the proposed device was closely investigated by scaling down the channel from 200 down to 7 nm. The optimal S/D doping concentration was found to be $5 \times 10^{18}$ cm$^{-3}$ at $V_{DD} = -0.85$ V and a Ge channel thicker than 5 nm out of a total Si + Ge thickness of 10 nm was revealed to be desirable for preparing a set of better DC and AC parameters. The proposed nanowire Ge PMOSFET with a channel length of 7 nm demonstrated permissible device performance characteristics including $I_{on} = 1.58 \times 10^{-5}$ A, $S = 89.5$ mV/dec, and $g_{m,max} = 3.195 \times 10^{-5}$ S, which supports the potential for LP and HP applications in sub-10-nm technology nodes.

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