Defect related effects on the reliability and performance of an embedded DRAM cell designed with MOSFETs with alternative gate dielectrics

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Abstract: The design of an embedded DRAM based on MOSFETs with alternative gate dielectrics is presented and analysed. Design and evaluation of NMOS devices with high-k dielectric gate insulators and DRAM circuits took place. Reliability parameters of the NMOS devices constructed with (Ba,Sr)TiO₃ gate dielectrics were examined. A 90 nm technology model and the BSIM4 Spice equations were used in order to derive the device behaviour and the DRAM circuit performance. The simulation revealed low output currents for the MOSFETs and higher decay times for the DRAM circuits constructed using the devices with the alternative gate dielectrics.

1. Introduction

The need of reducing power dissipation and chip size in low-voltage high-density embedded RAMs (e-RAMS) lead researchers to develop new devices such as MOS Transistors made with gate dielectrics other than SiO₂. During the last five years, the idea of applying MOSFETs with new gate dielectrics on the design and fabrication of RAMs has emerged as the future technique capable to keep and even increase the required performance of RAM circuits when dimensions keep shrinking [1-4].

In the ULSI regime for DRAM, storage densities of 256 Mb and beyond need to be maintained, while the dimensions of a high-density storage cell are scaled down to less than 1 µm. This fact necessitates that the conventional SiO₂ dielectric layer thickness is reduced by a scaling factor in order to obtain the high storage charge density of about 30–40 fC µm⁻² needed for DRAM operation. Moreover, the need to implement these devices into circuits, created the need to develop design techniques capable to accommodate the new devices into the existing electronic design tools and techniques.

In the present paper we demonstrate the design and simulation of a DRAM cell with a 1T-1C architecture using 90 nm technology MOSFETs with alternative gate dielectrics. A certain case is examined, regarding the very high dielectric constant material (Ba₁₋ₓSrₓ)TiO₃ (BST). The effects of process related defects and materials issues are examined in terms of parasitic capacitances and current leakage. First, NMOS devices are designed and simulated and then, an embedded DRAM circuit using the 90 nm technology is constructed and its performance is analysed. A layout is given and the timing performance of the memory circuit is examined.

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2. Device and circuit design
The NMOS single units were designed by taking into account reliability issues regarding the presence of interface traps, trapped oxide charges and leakage currents [2]. Considering a CMOS performance, parameters related to material processing and deposition need also to be counted for. The parameters that need to be taken into consideration for the modelling are: The dielectric constant ($\varepsilon$), the threshold voltage ($V_t$), the leakage currents ($J_g$) and process related phenomena inserted into the $K_{p,n}$ parameter defined as $\frac{1}{2} \mu_{n,p} C_{ox}$, where $\mu$ is the carrier mobility and $C_{ox}$ the oxide capacitance. Dimensions scaling analysis using the new dielectric constant, needs to be made, after calculating the Equivalent Oxide Thickness (EOT) for the MOSFET gate.

The MOS device under consideration uses as a gate dielectric material (Ba$_{1-x}$Sr$_x$) TiO$_3$ (BST) with $\varepsilon=320$ and $x=0.8$ [5]. The relevant scaling and the equations for the simulation used were those of the BSIM4 model of Spice with the parameters being altered accordingly in order to take into account the presence of the new gate dielectric [6,7,8]. The data used for the simulation were taken from literature reports on experimentally measured values obtained from devices constructed by high-k dielectrics deposited on Si substrates [5 and references therein].

3. Simulation, results and discussion
Simulation was made using the BSIM4 equations for the MOSFET, where for the construction of the single MOS device the 90 nm, 6 metal CMOS technology was used with 1.0V source voltages [5]. The BSIM4 model parameters used were set to $VTHO=0.3V$, $W=0.300 \mu m$, $L=0.100 \mu m$ while the TOXE parameter was selected to take the value reported in the literature for leakage currents that is below a certain value ($10^{-8}$ Acm$^{-2}$), and it was equal to 70 nm. In detail, in BSIM4 the basic equation describing the drain current, which flows through the channel to the source is given in by the expression [6]:

$$I_{DS} = \frac{I_{DSS}}{1 + \frac{1}{C_{th} V_{A,off}}} \left(1 + \frac{V_{DS} - V_{DSS}}{V_{A,BL}}\right) \left(1 + \frac{V_{DS} - V_{DSS}}{V_{A,BTS}}\right) \left(1 + \frac{V_{DS} - V_{DSS}}{V_{A,BL}}\right)^{NF}$$

where,

$$I_{DSS} = \frac{W_{eff} \mu_{eff} C_{ox,IV} V_{GSTEFF}}{L_{eff}\left(1 + V_{DSS}^{*} (\varepsilon_{SAT} L_{q})\right)} \left[1 - \frac{A_{sat} V_{DSS}}{2kV_{GSTeff} + 2kT/q}\right] V_{DS}$$

and all the parameters are defined in [6].

Figure 1. The $I_{d}$-$V_{ds}$ curves for the NMOS devices with a) SiO$_2$ and b) BST.

The use of such an expression requires a detailed examination of the various parameters appearing. Thus the use of the stepwise procedure described in [4] needs to take place in order to derive all the required values. This procedure did take place and as a result the $I_{d}$-$V_{ds}$ characteristics of the NMOS appear in figure 1, where the Equivalent Oxide Thickness (EOT) value for the SiO$_2$ device used for
comparison was 7.2 nm. In this case, the values of all the parameters used in the above equations were calculated using experimental data published in the literature together with the suitable methodology [7,8]. Analysis of their effects was considered using [9] for leakage current implementation in CMOS technology and replacing the SiO$_2$ values with those of BST in the relevant equations.

![Figure 2. The NMOS device and the various capacitances.](image)

In addition to the current analysis, the parasitic capacitances due to process and materials related phenomena needed to be taken into account. These capacitances were introduced into the BSIM4 equations using literature reported values of related parameters that have been calculated for similar structures using the methods described in [7,8] for devices with high-k dielectrics, while the corresponding capacitances are depicted in figure 2.

![Figure 3. The layout of the embedded DRAM cell using the 90nm design rules.](image)

The parasitic capacitances effects can be countered for, if the values of the relevant parameters are known in advanced. In this exercise, the parasitic capacitances were introduced using values of the density of interface states at the dielectric/Si interface, of the bulk trapped charges in the dielectric and effects due to metallization (voltage shift), obtained by literature reports on the same material [5 and references therein]. The values of $D_\text{it}$ used were $1.2 \times 10^{12}$ eV$^{-1}$cm$^{-2}$, the trapped charges had a density of 90 nC/cm$^3$, while the capacitor dielectric was also BST.

The constructed NMOS devices were then used to design an embedded DRAM circuit of the 1T-1C architecture. Its layout, designed using a lambda based rule, appears in figure 3. In order to examine the DRAM characteristics, a simulation of the Read/Store (R/S) process was made where the simulation was initiated by the requirement of a single bit R/S process.
The DRAM performance appears in figure 4. In figure 4a, the behaviour of a DRAM constructed with NMOS devices with SiO\textsubscript{2} is depicted while in figure 4b, the same results appear for the DRAM with the devices having the BST dielectric. It is shown that the value ‘1’ is being held for 224 ns in the case of the BST devices, a much larger value compared to the 37 ns of the SiO\textsubscript{2} case. Thus the DRAM cell with the MOSFET made of a high-k gate dielectric can hold the right value for a substantially larger time than that made of conventional SiO\textsubscript{2} MOSFETs. The above result is directly connected to the fact that at DRAM circuits a periodic refresh operation is always required to compensate for the steady leakage of charge from the storage nodes and to ensure the conservation of data. In this case, the refresh operation needed to recharge the DRAM cell capacitor of a cell made with conventional SiO\textsubscript{2} MOSFET should be completed in shorter time than the operation to refresh the cells made of MOSFETs with high-k dielectrics.

4. Conclusions and further work
Effective construction of a DRAM using MOSFETs with alternative gate dielectrics was demonstrated by suitable simulation and the MOS devices were used in the design of an embedded DRAM circuit. The presence of defect related phenomena was investigated and their effect on the device and circuit performance was evaluated. Future work involves the study of the device behaviour after the introduction of secondary processes occurring during R/S process (i.e. tunneling or Fowler-Nordheim currents) and such a work is currently on.

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