Device performances analysis of p-type doped silicene-based field effect transistor using SPICE-compatible model

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Abstract

Moore's Law is approaching its end as transistors are scaled down to tens or few atoms per device, researchers are actively seeking for alternative approaches to leverage more-than-Moore nanoelectronics. Substituting the channel material of a field-effect transistors (FET) with silicene is foreseen as a viable approach for future transistor applications. In this study, we proposed a SPICE-compatible model for p-type (Aluminium) uniformly doped silicene FET for digital switching applications. The performance of the proposed device is benchmarked with various low-dimensional FETs in terms of their on-to-off current ratio, sub-threshold swing and drain-induced barrier lowering. The results show that the proposed p-type silicene FET is comparable to most of the selected low-dimensional FET models. With its decent performance, the proposed SPICE-compatible model should be extended to the circuit-level simulation and beyond in future work.

1. Introduction

In the modern lives, the computing power of digital devices has been improved by the technology innovations in the miniaturisation of semiconductor transistors [1]. The famous Moore’s Law will soon experience its fundamental limit because of various constraints in bulk silicon (Si) technology, especially in the sub-10-nm atomic scales [2–4]. Therefore, the more-than-Moore development of the alternative field-effect transistors (FETs) has attracted much attention in the nanoelectronic research communities. Numerous industrial and public funds and programmes were initiated globally to overcome these “roadblocks” for long-terms advances in computing technology beyond Moore’s Law [5].

Among the options in the more-than-Moore race, two-dimensional (2D) materials have emerged as the prospective contenders owing to their atomically thin structure. Following the success of graphene since 2004 [6], research activities regarding 2D materials are intensely stimulated. Until now, more than 1800 exfoliable 2D candidates are theoretically predicted based on density-functional theory (DFT) [7], among which silicene could play a major role in future transistors owing to its outstanding carrier mobility [8] and compatibility with the
cutting-edge Si wafer technology [9]. Silicene was also shortlisted as a potential material for transistor miniaturisation in the International Roadmap for Devices and Systems (IRDS) [10].

In 2015, Tao et al. [9] fabricated the first silicene-based transistor operating at room temperature. Moreover, silicene nanosheets have successfully been fabricated on various substrates in their buckled [11–13] and planar [14] forms. However, the deposition of silicene monolayers on metals substrates is less practical viable for transistor applications, as compared to the direct growth on insulating layers, such as dielectrics or oxides [15]. This shortcoming can be addressed by using computational modelling and simulation while waiting for the breakthrough in silicene-based fabrication techniques.

Concerning the computational models of silicene-based transistors [16, 17], rigorous efforts were invested by many groups of researchers. The absence of bandgap in pristine silicene did not halt its exploration for nanotransistor applications. In spite of the challenges, various bandgap engineering techniques have been explored, and such examples include confinement through silicene nanoribbons (SiNRs) [18–20], co-decoration [21], and doping [22–24]. Among the aforementioned techniques, doping is the most commonly employed technique in the semiconductor industry to alter the electronic properties [25]. Furthermore, the performance of SiNR FETs are sensitive to their device dimensions [20, 26]; and it is still a major challenge to precisely control the widths of nanoribbons even for the established graphene monolayers [27]. Therefore, a uniformly aluminium (Al) doped silicene monolayer was proposed to engineer the bandgap of silicene, producing the AlSi$_3$ monolayer. In addition, a SPICE-compatible model was created to facilitate studies beyond the device-level simulation [28], such as the gate and logic levels.

Fig 1 shows the schematic diagrams of the proposed AlSi$_3$ FET and the simplified top-of-the-barrier (ToB) nanotransistor circuit model. In this study, we developed of a SPICE-compatible model for the proposed AlSi$_3$ FET from the ToB transistor model and benchmarked its device performance metrics with other published low-dimensional transistor models. Section 2 describes the modelling procedures to obtain the current-voltage (I-V) characteristics and the respective model evaluation methodology. Section 3 discusses the device performance of AlSi$_3$ FET with respect to its close low-dimensional contenders. Finally, Section 4 includes the conclusion of this work and future work recommendation.

2. Methodology

This section describes the overall modelling procedures employed in this study, where the overall flowchart is shown in Fig 2.

2.1. ToB nanotransistor and SPICE models

The atomic structure of the AlSi$_3$ monolayer (as shown in Fig 1) was adapted from published DFT study [29]. By using the derivation from time-independent Schrödinger equation [30], the electronic transport effective mass was then obtained by using nearest neighbour tight-binding (NNTB) model and parabolic band assumptions as $m^*_{\text{e}} = 0.235m_0$ and $m^*_{\text{h}} = 0.255m_0$ for electrons and holes, respectively. The material-level modelling was shown in details in our previous work [22].

Table 1 summarises the device parameters of the AlSi$_3$ FETs. In the ToB nanotransistor model [31], net induced mobile charge can be obtained by $\Delta P = (P_S + P_D) - P_0$ where $P_S$ and $P_D$ are the non-equilibrium charge densities at the source and drain terminals, respectively, and $P_0$ is the equilibrium charge density. The self-consistent potential $U_{\text{SCF}}$ at the ToB is obtained...
by using

\[ U_{SCF} = -q \left( \alpha_G |V_{GS}| + \alpha_D |V_{DS}| + \alpha_S V_S - q \frac{\Delta P}{C_S} \right), \]  

where \( q \) is the constant for electric charge and the total terminal capacitances is expressed as \( C_S = C_G + C_D + C_S \). Because the source terminal is always set to be zero, \( \alpha_S \) can be ignored. In an ideal FET, the perfect gate and drain control parameters \( \alpha_G = 1 \) and \( \alpha_D = 0 \) [18] are used to mimic the ideal I-V characteristics. However, the default gate and drain control parameters \( \alpha_G = 0.880 \) and \( \alpha_D = 0.035 \) [31] were used in this work.

Subsequently, the current-voltage (I-V) characteristics of p-type AlSi\(_3\) FET can be obtained in terms of \( V_{DS} \) and \( V_{GS} \), by employing Landauer-Büttiker ballistic transport equation [31] along with Fermi-Dirac integral solutions [32], given as

\[ |I_{DS}(|V_{GS}|, |V_{DS}|)| = \frac{gW}{h^2} \sqrt{\frac{m^*_e q^2 (k_B T)^3}{2\pi^3}} \left\{ \log[1 + e^{\beta E_F(V_{GS}|V_{ON})}] - \log[1 + e^{\beta E_F(V_{GS}|V_{ON})}] \right\}, \]
with the normalised energies of

$$\eta_s(|V_{GS}|, |V_{DS}|) = \frac{E_F - U_{SCF}(|V_{GS}|, |V_{DS}|)}{k_B T},$$  \hfill (3)$$

$$\eta_d(|V_{GS}|, |V_{DS}|) = \frac{E_F - U_{SCF}(|V_{GS}|, |V_{DS}|) - q|V_{DS}|}{k_B T},$$  \hfill (4)$$

for source and drain, respectively. In the equations, \( g \) is the degeneracy factor (set as 2 to include up and down spins); \( h \) is the Planck’s constant; and \( k_B \) is the Boltzmann constant. \textbf{Fig 3(A)} shows the I-V characteristics for AlSi\textsubscript{3} FET produced by the ToB nanotransistor model.

Following that, the results from ToB nanotransistor were further used to create the SPICE model to allow cross-platform and non-iterative simulation. Moreover, SPICE models are one of the essential tools in the IC design industry for simulation [28]. Before creating the SPICE model, a non-linear regression model [33] was employed to fit the self-consistent potential.

\begin{table}[h]
\centering
\caption{The device parameters of AlSi\textsubscript{3} FETs.}
\begin{tabular}{ll}
\hline
Parameters & Values \\
\hline
Band structures & NNTB \\
Hole effective mass, \( m^*_h \) & 0.255\( m_0 \) \\
Bandgap, \( E_g \) & 0.78 eV \\
Oxide material & SiO\textsubscript{2} \\
Oxide thickness, \( t_{OX} \) & 1.5 \text{ nm} \\
Temperature, \( T \) & 300 K \\
\hline
\end{tabular}
\end{table}

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$U_{SCF}$ given as

$$U_{SCF}(|V_{GS}|, |V_{DS}|) = \sum_{k=0}^{5} \sum_{j=0}^{k} P_{j,k-j} (|V_{GS}| + |V_{DS}|^{k-j}),$$  \hspace{1cm} (5)$$

where the coefficients $P_{j,k-j}$ for each respective $|V_{GS}| |V_{DS}|^{k-j}$ term were computed and optimised using MATLAB curve fitting tool. By using the MATLAB Curve Fitting tool, it was found that the lower orders of polynomial equations fail to fit the USCF well and, as a result, are unable to reproduce accurate I-V characteristics. Therefore, the fifth-order polynomial equation (highest number of order available in the MATLAB Curve Fitting tool) is chosen.
although the resulting equation is slightly long. The expansion of Eq (5) and the respective coefficients $P_{ij(k-j)}$ are attached along with the SPICE model library files in the S1 File. Fig 3 (B) shows the I-V characteristics for AlSi$_3$ FET produced by the SPICE model.

2.2. Model evaluation

In this subsection, a statistical method is employed to evaluate the accuracy of the SPICE model with respect to the ToB nanotransistor model for the proposed AlSi$_3$ FET. The models were evaluated by using the normalised root-mean-square-deviations (RMSD) \cite{29}, given as

$$\text{RMSD} = \frac{\sqrt{\sum_{i=1}^{N} (p_i - q_i)^2 / N}}{\max(p_i, q_i) - \min(p_i, q_i)} \times 100\%,$$

where $N$ denotes the total number of data, $p_i$ and $q_i$ are the values of $i^{th}$ data for the ToB nanotransistor model and the SPICE model, respectively. Fig 4(A) shows the I-V characteristics

Fig 4. Comparison between the ToB nanotransistor model and SPICE model of the AlSi$_3$ FET. The empty dots in (a) represent the results of the ToB nanotransistor model while the solid lines in (a) represent the results of the SPICE model.

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combining the results of the ToB nanotransistor model and the SPICE model. The point-by-point differences to compute RMSD are plotted in Fig 4(B). Overall, 0.91% of RMSD is produced by the SPICE model when it is benchmarked with the results from the ToB nanotransistor model, indicating that the model has produced a decent fit.

3. Performances analysis and discussion

We can analyse the device performances by extracting the device metrics from the proposed p-type AlSi₃ FET model. Fig 5 shows the graphical extraction approach to obtain on-to-off current ($I_{on}/I_{off}$) ratio, subthreshold swing (SS), and drain-induced barrier lowering (DIBL). The proposed AlSi₃ FET produces an $I_{on}/I_{off}$ ratio of $2.6 \times 10^5$, a SS of $67.8 \, mV/\text{dec}$, and a DIBL of $48.2 \, mV/\text{V}$.

In this work, we compared our proposed p-type AlSi₃ FET with respect to other low-dimensional FETs. We have selected other published works on low-dimensional FETs to fairly assess the device performance of the proposed AlSi₃ FET. The selected published models include co-decorated SiNR FET [21], 27-ASiNR FET [20], Si nanowire (SiNW) FET [34], Si thin sheet FET [35], carbon nanotube (CNT) FET [36], graphene nanoribbon (GNR) FET [37], black phosphorene (BP) FET [38], and monolayer molybdenum disulfide (MoS₂) FET [39]. To concisely compare the device performance metrics, the comparisons are presented as bar graphs as shown in Fig 6. Regarding the $I_{on}/I_{off}$ ratio, the performance of AlSi₃ FET model is slightly inferior to 27-ASiNR FET [20] and MoS₂ FET [39]. Regarding the SS, AlSi₃ FET model is also

![Fig 5. Definitions of the device performance metrics of a FET.](https://doi.org/10.1371/journal.pone.0264483.g005)
slightly higher than the 27-ASiNR FET [20]. Concerning the DIBL, AlSi$_3$ FET model is also outperformed by 27-ASiNR FET [20] and CNT FET [36]. However, the challenges remain owing to the fabrication compatibility of non-Si-based materials and the difficulty to precisely control the widths of nanoribbons [27, 40]. Therefore, the proposed AlSi$_3$ FET model is still a prospective alternative for future nanotransistor applications.

4. Conclusion

In this paper, we have investigated a SPICE-compatible model for p-type uniformly Al-doped silicene FET. Following that, the device performance of the proposed model is compared with
other published low-dimensional nanotransistors. Although the proposed silicene FET is slightly inferior to a few competitors, silicene-based FETs are still one of the potential ways for more-than-Moore nanoelectronic applications owing to its Si-based nature. This work can be extended by performing further circuit-level simulation beyond the transistor device level by using the proposed SPICE model.

Supporting information

S1 File. SPICE model.

(DOCX)

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References

1. Leiserson C.E., Thompson N.C., Emer J.S., Kuszmaul B.C., Lampson B.W., Sanchez D., et al. There’s plenty of room at the Top: What will drive computer performance after Moore’s law?, Science, 368 (2020). https://doi.org/10.1126/science.aam9744 PMID: 32499413

2. Waldrop M.M., More than Moore, Nature, 530 (2016) 144–148. https://doi.org/10.1038/530144a PMID: 26863965

3. Hao Y., Xiang S., Han G., Zhang J., Ma X., Zhu Z., et al. Recent progress of integrated circuits and optoelectronic chips, Science China Information Sciences, 64 (2021) 1–33. https://doi.org/10.1007/s11432-021-3235-7
4. Karbalaei M., Dideban D., Heidari H., Improvement in electrical characteristics of Silicon on Insulator (SOI) transistor using graphene material, Results in Physics, 15 (2019) 102806. https://doi.org/10.1016/j.rinp.2019.102806

5. Khan H.N., Hounshell D.A., Fuchs E.R., Science and research policy at the end of Moore’s law, Nature Electronics, 1 (2018) 14–21. https://doi.org/10.1038/s41928-017-0005-9

6. Novoselov K.S., Geim A.K., Morozov S.V., Jiang D., Zhang Y., Dubonos S.V., et al. Firsov, Electric field effect in atomically thin carbon films, Science, 306 (2004) 666–669. https://doi.org/10.1126/science.1102896 PMID: 15499015

7. Klinkert C., Szabó Á., Stieger C., Campi D., Marzari N., Luisier M., 2-D materials for ultrascaled field-effect transistors: one hundred candidates under the ab initio microscope, ACS nano, 14 (2020) 8605–8615. https://doi.org/10.1021/acsnano.0c02983 PMID: 32530608

8. Vogt P., De Padova P., Quaresima C., Avila J., Frantzeskakis E., Asensio M.C., et al. Silicon: compelling experimental evidence for graphene-like two-dimensional silicon, Phys. Rev. Lett., 108 (2012) 155501. https://doi.org/10.1103/PhysRevLett.108.155501 PMID: 22587265

9. Tao L., Cinquanta E., Chiappe D., Grazianetti C., Fanciulli M., Dubey M., et al. Silicene field-effect transistors operating at room temperature, Nature nanotechnology, 10 (2015) 227. https://doi.org/10.1038/nnano.2014.325 PMID: 25643256

10. IEEE, International roadmap for devices and Systems (IRDS). https://irds.ieee.org/, 2021. (Accessed 11 November 2021).

11. Huang L., Zhang Y.-F., Zhang Y.-Y., Xu W., Que Y., Li E., et al. Sequence of silicon monolayer structures grown on a Ru surface: From a herringbone structure to silicene, Nano Lett., 17 (2017) 1161–1166. https://doi.org/10.1021/acs.nanolett.6b04804 PMID: 28098458

12. Stępnia&-Dybala A., Krawiec M., Formation of Silicene on Ultra-Thin Pb (111) Films, The Journal of Physical Chemistry C, (2019). https://doi.org/10.1021/acs.jpcc.9b04343

13. Hsu H.-C., Lu Y.-H., Su T.-L., Lin W.-C., Fu T.-Y., Single crystalline silicene consist of various superstructures using a flexible ultrathin Ag (111) template on Si (111), Semicond. Sci. Technol., 33 (2018) 075004. https://doi.org/10.1088/1361-6641/aaad88

14. Stępnia&-Dybala A., Dyniec P., Kopciuszy&-ski M., Zdyb R., Jalochowski M., Krawiec M., Planar silicene: a new silicon allotrope epitaxially grown by segregation, Adv. Funct. Mater., 29 (2019) 1906053. https://doi.org/10.1002/adfm.201906053

15. Kolmer M., Zuzak R., Steiner A.-K., Zajac L., Engelund M., Godlewski S., et al. Fluorine-programmed nanozipping to tailored nanographenes on rutile TiO2 surfaces, Science, 363 (2019) 57–60. https://doi.org/10.1126/science.aav4954 PMID: 30608480

16. Zhao J., Liu H., Yu Z., Quhe R., Zhou S., Wang Y., et al. Rise of silicene: A competitive 2D material, Prog. Mater Sci., 83 (2016) 24–151. https://doi.org/10.1016/j.pmatsci.2016.04.001

17. Chuan M.W., Wong K.L., Hamzah A., Rusli S., Alias N.E., Lim C.S., et al. 2D Honeycomb Silicon: A Review on Theoretical Advances for Silicene Field-Effect Transistors, Current Nanoscience, 16 (2020) 595–607. https://doi.org/10.2174/15734137156661907090120019

18. Kaneko M., Tsuchiya H., Kamakura Y., Mori N., Ogawa M., Theoretical performance estimation of silicene, germanene, and graphene nanoribbon field-effect transistors under ballistic transport, Applied Physics Express, 7 (2014) 035102. https://doi.org/10.7567/APEX.7.035102

19. Mahmoudi M., Ahangari Z., Fathiipour M., Improved double-gate armchair silicene nanoribbon field-effect transistor at large transport bandgap, Chinese Physics B, 25 (2015) 018501. https://doi.org/10.1088/1674-1056/25/1/018501

20. Poljak M., Impact of Width Scaling and Parasitic Series Resistance on the Performance of Silicene Nanoribbon MOSFETs, IEEE Trans. Electron Devices, (2020). https://doi.org/10.1109/TED.2019.2953658 PMID: 32099264

21. Kharadi M.A., Malik G.F.A., Shah K.A., Khanday F.A., Sub-10-nm silicon nanoribbon field effect transistor, IEEE Trans. Electron Devices, 66 (2019) 4976–4981. https://doi.org/10.1109/TED.2019.2942396

22. Chuan M.W., Wong K.L., Hamzah A., Rusli S., Alias N.E., Lim C.S., et al. Electronic properties and carrier transport properties of low-dimensional aluminium doped silicene nanostructure, Physica E: Low-dimensional Systems and Nanostructures, 116 (2020) 113731. https://doi.org/10.1016/j.physe.2019.113731

23. Gooran-Shoorakchaly A., Ahmaddchaly A.A., Soleimani-Amiri S., Gholipour M., Design of a Low-Power Short-Channel Electrostatically Doped Silicon Nanoribbon FET, IEEE Trans. Electron Devices, 68 (2021) 1956–1961. https://doi.org/10.1109/TED.2021.3058337
24. Chuan M., Lau J., Wong K., Hamzah A., Alias N., Lim C., et al. Low-dimensional modelling of n-type doped silicene and its carrier transport properties for nanoelectronic applications, Advances in nano research, 10 (2021) 415–422. https://doi.org/10.12989/anr.2021.10.5.415

25. Spear W., Le Comber P., Substitutional doping of amorphous silicon, Solid State Commun., 88 (1993) 1015–1018. https://doi.org/10.1016/0038-1098(93)90284-7

26. Chuan M.W., Riyadi M.A., Alias N.E., Sultan S.M., Tan M.L.P., Impact of phonon scattering mechanisms on the performance of silicene nanoribbon field-effect transistors, Results in Physics, 29 (2021) 104714. https://doi.org/10.1016/j.rinp.2021.104714

27. Celis A., Nair M.N., Taleb-Ibrahim A., Conrad E., Berger C., De Heer W., et al. Graphene nanoribbons: fabrication, properties and devices, J. Phys. D: Appl. Phys., 49 (2016) 143001. https://doi.org/10.1088/0022-3727/49/14/143001

28. Paydavosi N., Venugopalan S., Chauhan Y.S., Duarte J.P., Jandhyala S., Niknejad A.M., et al. BSIM—SPICE models enable FinFET and UTB IC designs, IEEE Access, 1 (2013) 201–215. https://doi.org/10.1109/ACCESS.2013.2260816

29. Ding Y., Wang Y., Density functional theory study of the silicene-like SiX and XSi3 (X = B, C, N, Al, P) honeycomb lattices: The various buckled structures and versatile electronic properties, The Journal of Physical Chemistry C, 117 (2013) 18266–18278. https://doi.org/10.1021/jp407666m

30. Wong K.L., Chuan M.W., Hamzah A., Rusli S., Alias N.E., Sultan S.M., et al. Electronic properties of graphene nanoribbons with line-edge roughness doped with nitrogen and boron, Physica E: Low-dimensional Systems and Nanostructures, 117 (2020) 113841. https://doi.org/10.1016/j.physe.2019.113841

31. Rahman A., Guo J., Datta S., Lundstrom M.S., Theory of ballistic nanotransistors, IEEE Trans. Electron Devices, 50 (2003) 1853–1864. https://doi.org/10.1109/TED.2003.815366

32. Kim R., Lundstrom M., Notes on Fermi-Dirac Integrals (3rd Edition), 2008. https://arxiv.org/abs/0811.0116

33. Chin H.C., Lim C.S., Wong W.S., Danapalasingam K.A., Arora V.K., Tan M.L.P., Enhanced device and circuit-level performance benchmarking of graphene nanoribbon field-effect transistor against a nano-MOSFET with interconnects, Journal of Nanomaterials, 2014 (2014). https://doi.org/10.1155/2014/879813

34. Chiu H.C., Lim C.S., Tan M.L.P., Phonon scattering effects in drain-current model of carbon nanotube and silicon nanowire field-effect transistors, Science of Advanced Materials, 8 (2016) 1028–1035. https://doi.org/10.1166/sam.2016.2687

35. Lee Y., Park G.-H., Choi B., Yoon J., Kim H.-J., Kim D.H., et al. Design study of the gate-all-around silicon nanosheet MOSFETs, Semicond. Sci. Technol., 35 (2020) 03LT01. https://doi.org/10.1088/1361-6641/ab6bab

36. Tan M.L.P., Long channel carbon nanotube as an alternative to nanoscale silicon channels in scaled MOSFETs, Journal of Nanomaterials, 2013 (2013) 162. https://doi.org/10.1155/2013/831252

37. Eshkalak M.A., Faez R., Haji-Nasir S., A novel graphene nanoribbon field effect transistor with two different gate insulators, Physica E: Low-dimensional Systems and Nanostructures, 66 (2015) 133–139. https://doi.org/10.1016/j.physe.2014.10.021

38. Lam K.-T., Dong Z., Guo J., Performance limits projection of black phosphorous field-effect transistors, IEEE Electron Device Letters, 35 (2014) 963–965. https://doi.org/10.1109/LED.2014.2333368

39. Mohammad Tabatabaei S., Noei M., Khaliji K., Pourfath M., Fathi pour M., A first-principles study on the effect of biaxial strain on the ultimate performance of monolayer MoS2-based double gate field effect transistor, J. Appl. Phys., 113 (2013) 163708. https://doi.org/10.1063/1.4803032

40. Ma L., Wang J., Ding F., Recent progress and challenges in graphene nanoribbon synthesis, Chemphyschem, 14 (2013) 47–54. https://doi.org/10.1002/cphc.201200253 PMID: 22615215