Performance Implications of NoCs on 3D-Stacked Memories: Insights from the Hybrid Memory Cube

Ramyad Hadidi, Bahar Asgari, Jeffrey Young, Burhan Ahmad Mudassar, Kartikay Garg, Tushar Krishna, and Hyesoon Kim
Georgia Institute of Technology
Email: {rhadidi,bahar.asgari,jyoung9,burhan.mudassar,kgarg40}@gatech.edu, tushar@ece.gatech.edu, hyesoon@cc.gatech.edu

Abstract—Memories that exploit three-dimensional (3D)-stacking technology, which integrate memory and logic dies in a single stack, are becoming popular. These memories, such as Hybrid Memory Cube (HMC), utilize a network-on-chip (NoC) design for connecting their internal structural organizations. This novel usage of NoC, in addition to aiding processing-in-memory capabilities, enables numerous benefits such as high bandwidth and memory-level parallelism. However, the implications of NoCs on the characteristics of 3D-stacked memories in terms of memory access latency and bandwidth have not been fully explored. This paper addresses this knowledge gap by (i) characterizing an HMC prototype on the AC-510 accelerator board and revealing its access latency behaviors, and (ii) by investigating the implications of such behaviors on system and software designs.

I. INTRODUCTION

In the past decade, the demand of data-intensive applications for high-performance memories has pushed academia and industry to develop novel memories with larger capacity, higher access bandwidth, and lower latency. To this end, JEDEC-based memories (i.e., DDRx), have evolved into three-dimensional (3D)-stacked DRAMs, such as High Bandwidth Memory (HBM) [1]. While such memories are compatible with traditional architectures and JEDEC standards, they do not provide desirable scalability. Therefore, a scalable generation of 3D-stacked memories with packet-based communication have been introduced. Thanks to packet-switched networks and serial links, these novel 3D-stacked memories can exploit both internal and external networks to extend their capacity and scalability. An example of such memories is the Hybrid Memory Cube (HMC), which consists of vertical memory layers called vaults and a logic layer which consists of memory controllers (vault controllers) connected via an internal network. The characteristics of this underlying network plays an important role in the overall performance of these memories.

Logic and memory integration within 3D stacks has motivated researchers to explore novel processing-in-memory (PIM) concepts within the architecture of 3D-stacked memories using simulation [2]–[8]. However, few researchers have studied actual prototypes of memories similar to the HMC [9]–[11]. In particular, to the best of our knowledge, no experimental work has sought to characterize the bandwidth and latency [1] impacts of the internal NoC on the performance of the HMC. Such characterizations are important for the design of PIM units built around/inside the HMC because their internal routing characteristics also affect logic layers and application mappings for these devices. In order to gain insights into the impacts of NoC in 3D-stacked memories, we evaluate the performance characteristics of an HMC 1.1 [12] prototype. Figure 1 presents the full-stack overview of our system, which includes user configurations, memory trace files, software, and high-contention traffic situations, for which we use two combinations of software and digital designs (i.e., Verilog implementations on the FPGA). Our results reveal latency and bandwidth behaviors across various access patterns, the latency distribution and quality of service (QoS) within a particular access pattern, and bottlenecks within the HMC and associated infrastructure. This paper contributes the followings. (i) This is the first study, to the best of our knowledge, that explores the impacts of the internal NoC of the HMC, a prototype of packet-switched 3D-stacked memories, on its characteristics. (ii) It discusses how and why the internal NoC impacts applications and subsequently, how future system and application designs should effectively incorporate the HMC. (iii) It presents a detailed analysis of latency distribution within an access pattern caused by the internal NoC of HMC, and its consequences.

Our analyses characterize access properties for both low- and high-contention traffic situations, for which we use two combinations of software and digital designs (i.e., Verilog implementations on the FPGA). This section

1 This paper uses the term latency and round-trip time interchangeably.

II. BACKGROUND

In this paper, we focus on the HMC 1.1 specification (Gen2) [12], currently available for purchase. This section

Fig. 1: An overview of our system, and NoC of the HMC.
presents background on HMC structure and relevant information on packet-based memories for our analysis.

A. HMC Structure

The HMC 1.1 consists of eight DRAM dies stacked on top of a logic die, vertically connected by 512 Through-Silicon-Vias (TSVs) [15]. As Figure 2 illustrates, the layers of HMC are divided into 16 partitions, each of which is called a vault with a corresponding memory controller in the logic layer, the so-called vault controller [16]. Each vault employs a 32-byte DRAM data bus [12], enabled by 32 TSVs. A group of four vaults is called a quadrant, connected to an external full-duplex serialized link, a 16- (full-width) or eight-lane (half-width) connection running at speeds of 10, 12.5, or 15 Gbps. As a result, the maximum bandwidth of a two-link half-width HMC device with a 15 Gbps link is:

\[
\text{BW}_{\text{peak}} = 2 \times \text{link} \times 8 \times \text{lane}/\text{link} \times 15 \text{ Gbps} \times 2 \text{ full duplex} = 480 \text{ Gbps} = 60 \text{ GB/s}.
\] (1)

The size of a DRAM layer in Gen2 (HMC 1.1) devices is 4 GB. Thus, each of the 16 partitions is 32 MB. Also, as the size of a bank is 16 MB [12], the number of banks is equal to:

\[
\#\text{Banks}_{\text{HMC1.1}} = 8 \text{ layers} \times 16 \text{ partitions/layer} \times 2 \text{ banks/partition} = 256 \text{ banks}.
\] (2)

![Fig. 2: 4 GB HMC 1.1 internal structure.](image)

The header of a HMC 1.1 request packet (see Section II-B for more details) contains a 34-bit address field, but two high-order bits are ignored in a 4 GB HMC. Figure 3 shows the internal address mapping of HMC 1.1 for various block sizes from 32 to 128B [12], as well as the low-order-ordering mapping of sequential blocks to vaults and then to banks within a vault. For a block size of 128B (Figure 3a), an OS page, usually 4 KB, would be mapped to two banks over all 16 vaults so that serial accesses utilize bank-level parallelism (BLP). The vaults that each contain a part of a page are connected using with an internal NoC, whose characteristics impacts the overall bandwidth and latency of the system.

B. Packet-based Memories

Unlike memories with JEDEC-based bus interfaces (e.g., DIMM or HBM), HMC uses a packet-based interface to transfer packets over data links. Packet-based memories exploit internal and external NoCs for scalability; vaults in an HMC are connected internally and up to eight HMCs can be connected via external links. As the HMC interface uses high-speed serialization/deserialization (SerDes) circuits, these networked implementations achieve higher raw link bandwidths than traditional, synchronous, bus-based interfaces. Unlike traditional memories, the access latency of a packet-based memory includes additional steps for packet processing, such as packet creation, port arbitration, flow control and serialization/deserialization [12]. These overheads are amortized by using large numbers of queues and ports (up to nine in our infrastructure) for sending packets, high BLP, and high-speed transmission to and from the HMC device.

Similar to IP-based networks, the communication of HMC is layered which includes physical, link, and transaction layers. The physical layer is responsible for serialization, deserialization, and transmission while the link layer handles low-level communication and flow control for packets over the high-speed physical connections. The transaction layer defines request and response packets, their fields, and controls high-level flow and retry. The HMC controller uses three types of packets: flow, request, and response packets. Flow packets do not contain a data payload, while request and response packets are used for performing reads and writes from and to the HMC (Figure 4a and b). The 16-byte elements that instruct packets are called flits, and the size of data payload of each packet varies from one to eight flits. The least-significant flit of packets is transmitted first across the link. Flow control and integrity of packets are performed by fields of one-flit head and tail [12]. Accordingly, Table I shows each HMC transaction size in flits.

![Fig. 3: 4 GB HMC 1.1 address mapping with maximum block sizes of (a) 128B, (b) 64B, and (c) 32B.](image)

TABLE I: HMC read/write request/response sizes [12].

| Type       | Read         | Response       | Write         | Response       |
|------------|--------------|----------------|---------------|----------------|
| Data Size  | Empty        | 1~8 Flits      | 1~8 Flits     | Empty          |
| Overhead   | 1 Flt        | 1 Flt          | 1 Flt         | 1 Flt          |
| Total Size | 1 Flt        | 2~9 Flits      | 2~9 Flits     | 1 Flt          |

III. Methodology

This section introduces our infrastructure for evaluating an HMC and includes details on its hardware, firmware (i.e., digital design on the FPGA), and software.
Fig. 4: (a) A flow packet (no data), and (b) a request/response packet with 32B of data.

A. Infrastructure

We utilize a Pico SC-6 Mini [17] machine that incorporates an EX-700 [14] backplane, a PCIe 3.0 x16 board with 32 GB/s bandwidth to the host. The EX-700 backplane can accommodate up to six AC-510 [13] accelerator modules, each of which contains a Kintex Xilinx FPGA [2] and a 4 GB HMC 1.1 (similar to Figure 2). We employ one AC-510 in our evaluations. The HMC and the FPGA on an AC-510 module are connected with two half-width (8 lanes) links operating at 15 Gbps, so the bi-directional peak bandwidth is 60 GB/s, as Equation 1.

B. Firmware and Software

We use two combinations of firmware and software to perform experiments, GUPS and multi-port stream implementations, shown in Figure 5. Each combination integrates a custom logic on the FPGA, and a software counterpart. First, we describe the common components in the firmware on the FPGA. The FPGA uses Micron’s HMC controller [18] to generate packets for the multi-port AXI-4 interface between the FPGA and the HMC. On the software side, a Pico API and device driver are used to initialize the logic on the FPGA and provide an environment in which an OS communicates with the FPGA. The Pico API provides software methods to access the HMC through the FPGA with a direct path for packets. However, because the software runs at a rate of 4 MHz on the host, this solution cannot fully utilize the bandwidth of the HMC. Also, since maximum frequency of the FPGA is low (187.5 MHz), to generate more requests, the FPGA uses nine copy of the same module, called ports. Each port contains a monitoring logic (not in the critical path of accesses) for measuring various statistics such as the total number of read and write requests and the total, minimum and maximum of read latencies. We will further discuss the details of the access latency in Section III-C.

To observe the behavior of the NoC within the HMC with various traffic patterns and contention levels, we utilize two implementations as follows: (1) GUPS (Figure 5a), a vendor-provided firmware that measures how frequently we can generate requests to “random” memory locations; and (2) multi-port stream implementation (Figure 5b), a custom firmware which generates requests from a memory trace file using Xilinx’s AXI-Stream interface. The GUPS implementation is best suited to investigate NoC behavior under high contention, while multi-port stream implementation does the same task under low contention. For both implementations, the number of active ports and their access patterns are configured independently. With GUPS, each port has a configurable address generation unit that is able to send read only (ro), write only (wo), or read-modify-write (rw) requests for random, or linear mode of addressing. Also, by forcing some bits of the address to zero/one by using address mask/anti-mask, requests can be mapped to a specific part of the HMC. To perform experiments for each port, we first set the type of requests and size, their mask and anti-mask, and then we activate the port. While the port is active, it generates as many requests as possible for 10 seconds, and then it reports the total number of accesses (read and write), maximum/minimum of read latencies, and aggregate read latency back to the host. In this paper, the type of requests are ro, unless stated otherwise. Our current firmware implementations do not support ACKs after writes, so accurate measurements of write latency would only be possible with added monitoring logic specifically for writes. We plan to address this limitation in future work. However, since we study the internal NoC of the HMC, any type of requests that consume resources will reveal the behavior, bottleneck, and impacts of the NoC.

For the multi-port stream implementation, we have developed a multi-threaded software that reads a memory trace file for each port and populates buffers on the host. Then, by using Xilinx’s AXI-Stream interface to each port (wrapped in a PicoStream API call 19), we efficiently transmit commands such as access types, sizes, and data through their dedicated streams. After issuing requests and waiting for responses, each port transmits read data and their addresses back to the host. In fact, the FPGA reads stream data continuously until it reads all the data, such that each port reads data from its dedicated stream in every cycle. In both GUPS and multi-port stream implementations, we calculate the average access latency of reads by dividing the aggregate read latency by the total number of reads. We calculate bandwidth by multiplying the number of accesses by the cumulative size of request and response packets including header, tail and data payload (shown in Table 1), and dividing it by the elapsed time.

C. Contributing Factors to Access Latency

As Section II-B discussed, access latency of packet-based memories includes additional latencies. In this section, to determine the actual contribution of HMC in access latency, we quantify contribution of the HMC controller and data transmission. In both implementations, the monitoring logic measures various statistics of accesses. For latency, this logic measures the number of cycles from when a read request is submitted to the HMC controller (on the FPGA) until the cycle when the port receives the read response. Then, it reports back the aggregate read latency and total number of read accesses, from which we calculate average access latency for the HMC. We inspect the latencies associated with each module in the transmit (TX) and receive (RX) paths by time stamping requests and reading the stamps for each module. Figure 6 presents the latency deconstruction of the TX path after a request is submitted to the HMC controller. Each external link is connected to an hmc_node module, which consists of five TX_ports that correspond to a port. Since
the AC-510 has two links to the HMC, this means 10 ports are available on the FPGA, but one is reserved for system use.

After a request is submitted to the HMC controller (1) in Figure 6 (in the GUPS implementation by the Data Gen. unit, and in the multi-port stream implementation by Glue Logic), the TX_port unit converts it to flits and buffers up to five flits in the FlitsToParallel unit (2), which takes ten cycles or 53.3 ns (based on the max frequency of the FPGA at 187.5 MHz). Then, flits from each port are routed to subsequent units in a round-robin fashion by an arbiter (3). This routing latency is between two to nine cycles. Afterwards, Add-Seq#, Req. Flow Control, and Add-CRC units contribute a latency of ten cycles (4, 5, and 6, respectively). These units add fields in packets for reordering and data integrity. (See Section II-B) Moreover, if the number of outstanding requests exceeds a threshold, the request flow-control unit sends a stop signal to the corresponding port (7) requesting a pause in the generation of memory access requests. For low-contention latency measurements, the request flow-control unit does not stop the transfer of any flit. Finally, flits are converted to the SerDes protocol (12) and serialized (8 and 9, respectively), which takes around ten cycles. In addition, transmitting one 128B request takes around 15 cycles (10). Overall, up to 54 cycles, or 287 ns, are spent on the TX path. Similarly, for a packet, 260 ns are spent on the RX path. In total, 547 ns of measured latency is related to link transfers and packet generation on the FPGA.

IV. RESULTS

This section presents various detailed latency and bandwidth analyses under high- and low-contention traffics with GUPS and multi-port stream implementations, respectively.

A. High-Contention Access Latency

To achieve a broad perspective of the HMC properties, we perform experiments that access various structural abstractions in the HMC. Figure 7 illustrates the latency and bandwidth relationship for requests to the HMC. Figure 7 also shows that as the accesses become less distributed, the latency of accesses increases. As the figure illustrates, access latency varies from 24,233 ns for 128B requests targeting a single bank, to 1,966 ns for 32B requests spread across more than two vaults. Less distributed access patterns (e.g., one bank) have higher latency because they benefit less from BLP. Furthermore, the latency of small requests is always lower than that of large requests because (i) the granularity of the DRAM bus within each vault is less than the data size, always has an overhead of one flit (i.e., 16B). For this reason, the bandwidth efficiency of read responses with 16B and 128B data sizes are $\frac{16}{16+16} = 50\%$.
and $128/128+16 = 89\%$, respectively. Also, for retransmission of a packet (because of transmission failure, flow control, or CRC failure), each port must track outstanding requests, so each port can handle a limited number of outstanding requests at a time. Small requests, compared to large requests, underutilize this limited number of slots for keeping smaller data, which results in low bandwidth utilization. In summary, large packet sizes utilize available bandwidth better at the cost of added latency. Also, for reducing access latency, accesses should be carefully distributed to exploit BLP and avoid bottlenecks.

**B. Low-Contention Access Latency**

To examine low-contention latencies, we measure the access latency of the HMC while limiting the number of read requests to the 16 banks within a vault. Then, for each number of read requests, we report average latency across all vaults. To tune the number of accesses and the size of request packets, we use the multi-port stream implementation. Figure 8 depicts that as the number of requests in a stream increases from one to 55, the average latency increases from 0.7\,µs to 1.1\,µs for the request size of 16B, and from 0.7\,µs to 2.2\,µs for the request size of 128B. In other words, we observe two behaviors: 1) when the number of request packets is small, the size of request packet does not effect the latency; 2) when the size of request packets is larger, the HMC experiences more variations in latency. Since the request flow control unit (Figure 9) is only activated with a large number of outstanding requests, we are certain that approximately 547\,ns of all latencies for the small number of requests in Figure 8 belongs to FPGA and data transmission stages (see Section III-C for more details). Therefore, the contributing latency of HMC under low load (i.e., no load) is 100 to 180\,ns, which includes the latency of DRAM access ($t_{RD} + t_{CL} + t_{RP}$) is around 41\,ns for HMC [5], [20], TSV transmission, vault controller, and internal NoC. However, as the number of requests increases, with the same BLP, queuing delay in both the HMC and the FPGA increases, which results in an order of magnitude higher delays. Note that since HMC utilizes a packet-switched interface to memory controllers in its logic layer, the observed average latency of HMC is higher than that of traditional DRAMs.

Figure 9 illustrates a wider range for the number of read requests in a stream access than that shown in Figure 8. In this Figure 9, we observe that when the number of requests increases up to 100, average access latency increases linearly. After that, the latency stays approximately constant when the number of requests grows. By assuming a hypothetical queue for requests, we infer that until the time that the queue is not full, the latency of each request equals to its serving time plus its waiting time, the sum of the serving time of all previous requests in the queue. We can write the average latency of $n$ requests as $\sum_{i=0}^{n} (iS)/n$, in which $S$ is the serving time of a request. Therefore, the latency seen by each request is correlated to the number of requests in the queue. In the region, where latency remains constant, the queue is always full, so the latency of a request equals to it serving time plus the waiting time for all requests in a the queue (i.e., $n = \text{Queue}_{\text{size}}$). Thus, the linear region represents a partially utilized system, and the constant region represents a fully utilized system. Section IV-F will provide further details on bandwidth and bottlenecks. To recap, even for low-contention traffic, NoC and queuing delay contribute significantly in the HMC access latency.

**C. Quality of Service Analysis**

In this section, our goal is to ascertain how latency varies within an access pattern (e.g., accesses distributed in four vaults) as a result of the packet-switched interface of the HMC, and subsequently, how this will affect the QoS of applications. In other words, despite its high bandwidth (thanks in part to serialization, and high BLP in a small area), NoC adds uncertainty to access latencies. Therefore, optimizing the access patterns in an application would not be sufficient to guarantee a precise QoS. Also, the effects of latency variations on QoS are important because they impact latency-sensitive applications, and because multi-threaded and parallel architectures will still stall for the slowest thread, which causes work imbalance. In our experiments, as a case study, we use four ports with the GUPS implementation to generate read accesses to four vaults (1\,GB in total). During which, three ports always access the same vaults, and a fourth port iterates over all possible vaults.

**Fig. 8:** Average latency of low-load accesses for various request sizes for the number of requests in the range of one to 55.

**Fig. 9:** Average latency of low-load accesses for various request sizes for the number of requests in the range of one to 350.

**Fig. 10:** Maximum observed latency in accessing four vaults, three of which are the same. Accessing vault numbers (a) one (3x) and all vaults; and (b) five (3x) and all vaults.
Figure 11 illustrates the maximum observed latency for two series experiments, in which three ports access vault number one and five, respectively. The figures depict, when the fourth port accesses the same vault as the other ports (i.e., vault numbers one and five in Figures 10a and b, respectively) the maximum observed latency increases up to 40% relative to other accesses. Furthermore, when we are not accessing the same vault, maximum observed latency varies notably. For instance, the maximum variations are around 200, 330, 400, 600 ns for 16B, 32B, 64B, and 128B size of requests, respectively. In short, even within the same access pattern, NoC causes considerable latency variations, which will have a noticeable impact on QoS of an application, even when its access patterns are optimized.

D. High-Contention Latency Histograms Per Vault

To understand the impact of accessing various combinations of vaults on performance, we extend the experiments of the previous section, which accessed four vaults using the GUPS implementation (i.e., high contention). For instance, accesses to four consecutive vaults (e.g., 0, 1, 2, and 3) that share network resources may have higher latency than accesses spread among non-consecutive vaults (e.g., 0, 4, 8, and 12) do. To test this hypothesis, we access all possible combinations of four different vaults (i.e., equal to 1820 combinations, or $n!/(k!\times (n-k)!)$ for $n = 16$ and $k = 4$) with various request sizes and calculate the average access latency among four vaults. Then, we associated the calculated average latency with every vault in that combination. Figure 11 illustrates our results for various sizes in heatmaps where a row represent the latency histogram of a vault. In other words, in a row, the color of a rectangle represents the normalized value of the number of accesses in that latency interval against the total number of accesses to the corresponding vault (i.e., 455). As the figure shows, each vault has a different latency behavior. For instance, in Figure 11, we observe that the histogram of vaults differs substantially (e.g., vault numbers 5, 6, and 7). Although we can investigate these figures in more detail, a quick takeaway is that purely optimizing the general access patterns of an application would not guarantee a particular latency. In other words, Figure 11 presents a case study with a four vault access pattern, in which the only factor of variation is vault IDs that determine the physical location of a vault within the 3D stack. Therefore, since other factors such as latency interval against the maximum number of accesses in that row. Figures 13a, b, c, and d, show colormaps for various request sizes of 16B, 32B, 64B, and 128B, respectively. In Figure 13a, we observe that for gaining the lowest latency (i.e., lowest row), we should avoid accessing vault numbers 9 to 12.

As Figure 11 shows, for each request size, although all the vaults have a similar average latency, the distribution of latencies are different among vaults. For a better illustration, Figure 12 depicts the average latency of all vaults and the standard deviation for various packet sizes. We observe that the standard deviation of latencies is 20, 40, 110, and 90 ns for request sizes of 16, 32, 64, and 128B, respectively. Note that 68% of a population is within $(\mu + \sigma$, $\mu - \sigma)$, in which $\mu$ and $\sigma$ are average and the standard deviation of that population, respectively. While average latencies per vault are similar for a particular request size, the distribution per vaults covers a broad range. Compared to smaller request sizes, larger request sizes have more variations in latency, because large request sizes occupy larger buffer spaces than small request sizes do. Also, large requests incur extra delays because of reordering and packetizing. Therefore, small request sizes are good candidates for guaranteeing a high quality of service. However, as discussed in Section IV-A, small request sizes have low bandwidth efficiency and generally provide lower bandwidth utilization than large request sizes.

E. High-Contention Vault Histograms Per Latency Interval

To explore the contribution of vaults to high and low latencies, each row of Figure 13 depicts contributing vaults for each latency interval and illustrates the histogram of them. The intensity of the color of a rectangle shows the normalized value of the number of that particular appearance of vault in that latency interval against the maximum number of accesses in that row. Figures 13a, b, c, and d, show colormaps for various request sizes of 16B, 32B, 64B, and 128B, respectively. In Figure 13a, we observe that for gaining the lowest latency (i.e., lowest row), we should avoid accessing vault numbers 9 to 12.
In fact, Figure 13 provides a guide for avoiding certain vaults that incur high latencies, but it will not guarantee particular access latencies for a specific vault. For instance, based on Figure 11, vault number 2 has the highest contribution to the lowest latency interval, and it similarly has a high contribution for the highest latency. Therefore, the conclusion that accessing only vault number 2 will guarantee the lowest latency is not correct. However, in the same figure, the chance of incurring lower latency increases by avoiding vaults numbers 9 to 12. Even though we cannot reach a unanimous conclusion about the latency of each vault and the hierarchy of NoC in the HMC, we can conclude that the effects of NoC and vault interactions are not trivial.

F. Requested and Response Bandwidth Analysis

To further investigate potential HMC networking bottlenecks and bandwidth, we use the GUPS implementation to tune request rate by changing the number of active ports from 1 to 9 ports. The number of active ports is a proxy for the requested bandwidth because it has a direct relationship with the number of issued requests with the GUPS firmware design. Figure 14 presents the relationship between the number of active ports and the response bandwidth for various request sizes. In this figure, sloped lines determine access patterns in which no bottleneck occurs. In contrast, flat lines depict access patterns in which a bottleneck (e.g., vault bandwidth limitation) exists. As discussed in Section IV-A, we observe that accessing eight banks within a vault saturates the internal 10 GB/s bandwidth of a vault for request sizes of 16 and 32B. In addition, for 64 and 128B request sizes, accessing four banks saturates the internal bandwidth of a vault. Thus, within a vault, depending on the size of requests, increasing BLP to more than eight or four banks will not provide higher bandwidth. In fact, as Figure 5 presents, for accessing a 4KB OS page in the HMC, requests are first spread over vaults and then banks. In other words, for the maximum block sizes of 64 and 128B (Figure 3a and b), a 4KB OS page resides in two and four banks of every vault, respectively. Therefore, accessing a single page in these configurations naturally avoids this bottleneck. However, this conclusion is not true when the maximum block size is set to 32B, as shown in Figure 5. Also, we can extend this insight to more than one OS pages sequentially allocated in the address space. For instance, for 128B maximum block size and request sizes of 128B, accessing to more than four sequentially allocated OS pages would invoke this bottleneck. In brief, for effectively utilizing the limited bandwidth of vaults within the HMC, application access patterns must be operated for increasing vault-level parallelism and then bank-level parallelism.

Compared to traditional DRAM memories, HMC supplies a higher amount of bandwidth and concurrency due to the high number of vaults and independent vault controllers. Figure 14 exhibits this point by showing that for request sizes of 128B, distributed access patterns to more than two vaults quickly reach the bottleneck of the external bandwidth of two links. This is a limitation of our particular HMC infrastructure (two half links from the FPGA to the HMC), as the number and width of HMC links can be increased as can the speed and efficiency of the FPGA infrastructure (i.e., HMC controller and associated firmware). Since HMC uses bi-directional links, issuing only read requests results in an asymmetric usage of the available bandwidth. In other words, read requests only can fully utilize response bandwidth, and write requests only can fully utilize request bandwidth. Previous studies [9], [21] have investigated this asymmetry, and proposed issuing a mix of read and write requests to address it. In addition to optimizing access patterns, applications should also balance the ratio of read and write requests for effectively utilizing bi-directional bandwidth of stacked memory networks.
V. RELATED WORK

Previous work has characterized the HMC [9–11], [21], from which Schmidt et al. [9] agreed with our measured bandwidth and latency. Although these studies have explored emulated HMC and earlier HMC prototype chips, they have not studied the performance impacts of the HMC NoC. Other recent studies have focused on designing an efficient NoC for HMC. Zhan et al. [22] proposed solving issues that show up in a NoC coupled with HMC, such as traffic congestion, uncoordinated internal and external networks, and high power consumption by co-optimizing networks both inside each HMC and between cubes. Their proposed unified memory network architecture reuses the internal network as a router for the external network, which allows for remote access bypassing while also providing high bandwidth for local accesses. The authors also proposed reducing communication loads and using power gating to further decrease power consumption for an overall 75.1% reduction in memory access latency and a 22.1% reduction in energy consumption. Azarkhish et al. [23] proposed a low latency AXI-compatible interconnect, which provides the required bandwidth for HMC infrastructure so that it supports near memory computation. Their simulation results show that the main bottleneck for delivered bandwidth is the timing of DRAM layers and TSVs. Also, their analysis on PIM traffic with increased requesting bandwidth on the main links showed that when the host demands less than 120 GB/s no saturation occurs. In another work, Fujiki [24], et. al proposed a scalable low-latency network by using a random topology based on communication path length, using deadlock-free routing, and memory-mapping in granularity of a page size. Their full-system simulation models show that this method reduces cycles by 6.6%, on average, and that random networks with universal memory access out-perform non-random, localized networks.

VI. CONCLUSION

In this paper, we evaluated a real-world prototype of a 3D stacked memory with an internal NoC, the HMC, using two combinations of software and digital design focused on high- and low-contention traffic. From our experiments we conclude the followings about NoC effects in the HMC and potentially in future stacked memories. (i) Large and small packets provide a trade-off of effective bandwidth versus latency as a result of buffering, packetization, and reordering overheads. In contrast with traditional DDRx systems, this trade-off enables tuning of memory accesses for optimizing bandwidth versus latency. (Section IV-A, IV-D) (ii) As future memories become denser with more links and vaults, queuing delays will be a serious concern for packet-based memories such as HMC. Effective solutions should focus on optimizing queuing on the host controller side and at vault controllers. (Section IV-B) (iii) The internal NoC complicates QoS for memory accesses because of meaningful variations in latency even within an access pattern. Smaller packets ensure improved QoS at a cost of reduced bandwidth. (Section IV-C, IV-D and IV-E) (iv) Limited bandwidth within a vault means that mapping accesses across vaults then banks is a key to take advantage of for better bandwidth utilization and lower latency. (Section IV-A and IV-F) (v) Finally, the packet-based protocol creates an asymmetric bi-directional bandwidth environment that applications should be aware of and optimize for the proper mix of reads and writes for effectively utilizing external bandwidth. (Section IV-A and IV-F)

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