A Gate-All-Around In$_2$O$_3$ Nanoribbon FET With Near 20 mA/µm Drain Current

Zhuocheng Zhang, Zehao Lin, Pai-Ying Liao, Vahid Askarpour, Hongyi Dou, Zhongxia Shang, Adam Charnas, Mengwei Si, Member, IEEE, Sami Alajlouni, Ali Shakouri, Haiyan Wang, Mark Lundstrom, Life Fellow, IEEE, Jesse Maassen, and Peide D. Ye, Fellow, IEEE

Abstract—In this work, we demonstrate atomic-layer-deposited (ALD) single-channel indium oxide (In$_2$O$_3$) gate-all-around (GAA) nanoribbon field-effect transistors (FETs) in a back-end-of-line (BEOL) compatible process. A maximum on-state current ($I_{ON}$) of 19.3 mA/µm (near 20 mA/µm) and an on/off ratio of 10$^6$ are achieved in an In$_2$O$_3$ GAA nanoribbon FET with a channel thickness ($t_{IO}$) of 3.1 nm, channel length (L$_{ch}$) of 40 nm, channel width (W$_{ch}$) of 30 nm and dielectric HfO$_2$ of 5 nm. Short-pulse measurements are applied to mitigate the self-heating effect induced by the ultra-high drain current flowing in the ultra-thin channel layer. The record high drain current obtained from an In$_2$O$_3$ FET is about one order of magnitude higher than any conventional single-channel semiconductor FETs. This extraordinary drain current and its related on-state performance demonstrate that ALD In$_2$O$_3$ is a promising oxide semiconductor channel with great opportunities in BEOL compatible monolithic 3D integration.

Index Terms—Indium oxide, amorphous oxide semiconductor, gate-all-around nanoribbon transistor, BEOL compatible, atomic layer deposition.

I. INTRODUCTION

Advanced oxide semiconductors are widely investigated and applied as thin-film transistor channels for display applications over the past decades [1], [2], [3]. Very recently, they are explored for back-end-of-line (BEOL) compatible transistor channels for monolithic 3D integration [4], [5], [6], [7]. Among these materials, atomic layer deposited (ALD) In$_2$O$_3$ shows excellent transport properties with mobility beyond 100 cm$^2$/V·s and its field-effect transistors (FETs) exhibit remarkable performance including large on-state current ($I_{ON}$) over 2-3 mA/µm in both depletion and enhancement-mode operation, on/off ratio up to $10^7$, sub-threshold swing (SS) as low as 63 mV/dec, and high stability in H$_2$ environment [8], [9], [10], [11], [12], [13], [14]. Meanwhile, the ALD technique offers wafer-scale film synthesis, accurate thickness control, smooth surface, high conformity and uniformity on 3D structures and a low thermal budget process below 300 °C [9], [10], [11], [12], [13], [14].

In this work, scaled single-channel In$_2$O$_3$ nanoribbon FETs with gate-all-around (GAA) structure and various channel length (L$_{ch}$) of 40 nm – 1 µm and channel width (W$_{ch}$) of 30 nm – 1 µm are fabricated under BEOL compatible conditions. On-current ($I_{ON}$) is enhanced to 4.3 mA/µm at drain voltage of 1 V in a device with L$_{ch}$ of 40 nm and W$_{ch}$ of 1 µm compared to the previous bottom or top-gated ALD In$_2$O$_3$ FETs [9], [13]. To resolve the self-heating issue due to the ultrahigh current in the ultrathin channel, the channel width scaling and short-pulse measurements are applied. The self-heating effect is mitigated significantly after these two approaches and a maximum $I_{ON}$ of 19.3 mA/µm is observed at a drain voltage of 1.7 V in a 30 nm wide nanoribbon FET by pulsed I-V measurements. This extraordinary drain current density is the highest ever obtained from a single-channel transistor [14].

II. EXPERIMENTS

Fig. 1(a) and 1(b) show the device schematic of a single-channel In$_2$O$_3$ GAA FET in 3D model and cross-section view in source/drain direction respectively. A fabrication process flow is presented in Fig. 1(c). The device fabrication started with solvent cleaning of p+ Si substrate with 90 nm thermally grown SiO$_2$. Then, 10 nm Al$_2$O$_3$ was grown by ALD at 175 °C to obtain a smooth surface and a bi-layer photoresist lithography process was applied for the sharp lift-off of Ni by electron-beam evaporation as the bottom gate metal. Next, 5 nm HfO$_2$ bottom dielectric was grown by ALD at 200 °C, using [(CH$_3$)$_2$N$_2$]Hf (TDMAHf) and H$_2$O as Hf and O precursors. 3.1 nm In$_2$O$_3$ was grown by ALD at 225 °C with (CH$_3$)$_3$In (TMIn) and H$_2$O as In and O precursors. N$_2$ was used as carrier gas at a flow rate of 40 sccm and the base pressure is 1500 mTorr. The film thickness was confirmed by transmission electron microscopy (TEM) and ellipsometry. Channel isolation was done by dry etching (BCl$_3$: 15 sccm; BCl$_3$: 15 sccm; and N$_2$).
Fig. 1. Device schematic of an In$_2$O$_3$ GAA nanoribbon FET with T$_{IO}$ of 3.1 nm and dielectric of 5 nm HfO$_2$ in (a) 3D model (b) cross-section view in S/D direction. (c) Fabrication process flow of the In$_2$O$_3$ GAA nanoribbon FETs. (d) EDS cross-section image of an In$_2$O$_3$ GAA FET with L$_{ch}$ of 40 nm.

Ar: 60 sccm; pressure: 0.6 Pa) and Ni was deposited to serve as the source/drain electrodes, patterned by electron beam lithography. A top dielectric of 5 nm HfO$_2$ was then grown by ALD at 200 °C. Finally, the gate metal was surrounded by e-beam evaporation of 40 nm Ni with dry etching first to connect the top and bottom gates. As can be seen, single layer In$_2$O$_3$ with channel thickness (T$_{IO}$) of 3.1 nm is surrounded by 5 nm HfO$_2$ dielectric and 40 nm Ni gate stack. 3.1 nm thick In$_2$O$_3$ layer was chosen to realize the record high drain current of the devices. Even thicker In$_2$O$_3$ layer leads to the fact that the devices cannot fully pinch-off since the thickness is beyond the maximum depletion width of the In$_2$O$_3$ layer. Notice that the whole fabrication process has a BEOL compatible low thermal budget of 250 °C.

III. RESULTS AND DISCUSSIONS

Fig. 2(a) and 2(b) present the transfer and output characteristics of a typical In$_2$O$_3$ GAA FET with $L_{ch}$ of 1 µm and $W_{ch}$ of 1 µm. Well-behaved switching characteristics with on/off ratio over 10$^4$ and a clear drain current saturation at large drain voltage (V$_{DS}$) are observed. I$_{ON}$ reaches 500 µA/µm at V$_{DS}$ of 2.5 V. All I$_{ON}$ are simply normalized by $W_{ch}$ since the channel thickness T$_{IO}$ is much smaller than $W_{ch}$. The gate leakage current (I$_{G}$) is at the level of 10$^{-9}$ mA/µm and the on/off ratio is limited by the off-state current (I$_{OFF}$) that can be probed. Further increasing negative gate bias will lead to the dielectric hard breakdown of 5nm HfO$_2$. Fig. 2(c) and 2(d) show the transfer and output characteristics of a short channel In$_2$O$_3$ GAA FET with $L_{ch}$ of 40 nm and $W_{ch}$ of 1 µm. A maximum I$_{ON}$ of 4.3 mA/µm is achieved at V$_{DS}$ of 1 V. Further increasing V$_{DS}$ results in the unstable devices due to ultrahigh current density induced Joule heating in the nanometer-thin In$_2$O$_3$ channel [13], [15]. $V_T$ is near constant for devices with different $L_{ch}$ and maximum transconductance ($g_m$) exceeds 10$^3$ S/µm due to 5 nm thin HfO$_2$ dielectric. The relatively negative $V_T$ is attributed to the large electron carrier concentration in the channel and the Fermi level ($E_F$) located highly above the conduction band edge ($E_C$). Further lowering In$_2$O$_3$ thickness will enhance the bandgap due to the quantum confinement effect and shift $E_C$ toward $E_F$. The reduction of carrier density results a positive shift of $V_T$ and a decrease of drain current, which can be considered as a tradeoff between channel thickness and maximum drain current [8].

Channel width scaling of the In$_2$O$_3$ ribbon is also investigated. Fig. 3(a) illustrates a false-color top-view scanning electron microscope (SEM) image of a fabricated GAA In$_2$O$_3$ nanoribbon FET with a $W_{ch}$ of 50 nm. Similar electrical measurements are performed and the extracted I$_{ON}$ versus $W_{ch}$ of different devices from 1 µm down to 30 nm is plotted in Fig. 3(b) with SS of 100-120 mV/dec. It is surprising that I$_{ON}$ becomes approximately three times larger as the channel narrows with no obvious $V_T$ shift. Two factors are accounted for such current enhancement. First, the electric field induces a higher carrier density at the channel edge due to the GAA geometry and the edge gradually takes a larger portion of the conductance in the channel width scaling. Etched In$_2$O$_3$ ribbon edges might lead to a charge neutrality level (CNL) located even deeper inside the conduction band, thereby enhancing edge conduction. Second, better heat dissipation is realized due to a larger perimeter to area ratio in a narrower ribbon. Fig. 3(c) and 3(d) present the transfer and output characteristics of an In$_2$O$_3$ GAA nanoribbon FET with $L_{ch}$ of 40 nm and $W_{ch}$ of 30 nm. A maximum I$_{ON}$ of 11.4 mA/µm is achieved at a V$_{DS}$ of 1 V. The narrow ribbon structure leads to the enhanced on-state performance as shown in Fig. 3(d) and also...
Fig. 3. (a) False-color top-view SEM image of an In$_2$O$_3$ GAA nanoribbon FET with W$_{ch}$ of 50 nm. (b) $I_{ON}$ and $V_T$ of the In$_2$O$_3$ GAA nanoribbon FETs under channel width scaling from 1 $\mu$m down to 30 nm. Each point is from at least 3 devices. (c) Transfer and (d) output characteristics of a typical In$_2$O$_3$ GAA nanoribbon FET with L$_{ch}$ of 40 nm and W$_{ch}$ of 30 nm, showing maximum $I_{ON}$ of 11.4 mA/µm at $V_{DS} = 1$ V. (e) $I_{G}$ of In$_2$O$_3$ GAA FET with L$_{ch}$ of 40 nm and W$_{ch}$ of 30 nm.

the improved off-state performance as shown in Fig. 3(c) due to the GAA structure and a better gate control, in contrast to the off-state performance of a wider channel device presented in Fig. 2(c).

To further probe the potential of the device performance, a pulsed I-V measurement is implemented. A data averaging time of 500 ns, $V_{GS}$ and $V_{DS}$ pulse width of 1 $\mu$s and pulse period of 100 ms are set to minimize the self-heating effect and improve device reliability. Fig. 4(a) and Fig. 4(b) present the pulsed transfer and output characteristics of an In$_2$O$_3$ GAA nanoribbon FET with L$_{ch}$ of 40 nm and W$_{ch}$ of 30 nm. A record high $I_{ON}$ of 19.3 mA/µm is achieved at $V_{DS}$ of 1.7 V, demonstrating the remarkable current carrying capacity of ALD In$_2$O$_3$. The off-state current in the transfer curve is limited by the resolution of the pulsed I-V setup while a real on/off ratio over $10^6$ is shown in Fig. 3(c) in DC measurements. The thermal time constant of this scaled device is around tens of nanoseconds since the two sets of data measured by DC and pulse setup can merge perfectly, indicating the thermal equilibrium state is achieved within the pulse width of 1 $\mu$s.

DFT simulations of a 3.0 nm thick slab of single crystal In$_2$O$_3$ were performed to study its electronic properties [16], [17]. Fig. 4(c) shows the band structure of the conduction states. In$_2$O$_3$ has simple electronic bands, with a single zone-centered band up to 0.5 eV, in contrast to most of III-V compound semiconductors such as GaAs which possess a satellite band near $E_C$. High electron density in In$_2$O$_3$ enables $E_F$ to occupy high energy states in the conduction band, where the majority of the conducting electrons have high band velocity. Fig. 4(d) presents the ideal ballistic transport properties, including the ballistic current density and average electronic velocity, versus carrier concentration. The ultra-high drain current is a product of high electron density and high average band velocity [17]. First, $E_F$ in the 3.1 nm-thick In$_2$O$_3$ is located deeply in the conduction band, being different from Si or other conventional semiconductors, so that a high carrier density around $4 \times 10^{13}$ cm$^{-2}$ can be achieved. Second, a single conduction band in In$_2$O$_3$ with relatively low effective mass of 0.19 m$_0$ and density of states leads high $E_F$ located in conduction band once high carrier density is populated. It leads high band velocity at $E_F$ and beneficial high average band velocity. The velocity increases rapidly with high carrier concentration is illustrated by the pink curve in Fig. 4(d). A velocity $>3 \times 10^7$ cm/s can be achieved with carrier density at the level of $4 \times 10^{13}$ cm$^{-2}$. These two factors lead to a record high $I_{ON}$ of 20 mA/µm. Note that this simulation only provides a qualitative guidance of device performance, since it considers an ideal single crystal of In$_2$O$_3$ and the ballistic transport limit. The real devices are much more complicated with an amorphous oxide channel, a channel length longer than the mean free path and non-negligible interface and bulk defects. In addition, further investigation on device reliability is still needed so as to make ALD In$_2$O$_3$ a competitive candidate as a channel material in practical BEOL applications.

IV. CONCLUSION

In summary, single-channel In$_2$O$_3$ GAA nanoribbon FETs are demonstrated in a BEOL compatible process. A record high $I_{ON}$ of 19.3 mA/µm is achieved through short-pulse measurements, channel width scaling and improved heat dissipation in smaller devices. This work demonstrates a surprising result in the field of electronic materials and devices that such an amorphous oxide semiconductor can offer the record high current density. ALD In$_2$O$_3$ as a novel channel material shows great promise in monolithic 3D integration.
REFERENCES

[1] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, “Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors,” Nature, vol. 432, no. 4016, pp. 488–492, Nov. 2004, doi: 10.1038/nature03090.

[2] K. Nomura, A. Takagi, T. Kamiya, H. Ohta, M. Hirano, and H. Hosono, “Amorphous oxide semiconductors for high-performance flexible thin-film transistors,” Jpn. J. Appl. Phys., vol. 45, no. 5B, pp. 4303–4308, May 2006, doi: 10.1143/JJAP.45.4303.

[3] T. Kamiya, K. Nomura, and H. Hosono, “Present status of amorphous In–Ga–Zn–O thin-film transistors,” Sci. Technol. Adv. Mater., vol. 11, no. 4, Feb. 2010, Art. no. 044305, doi: 10.1088/1468-6996/11/4/044305.

[4] S. Li, M. Tian, Q. Gao, M. Wang, T. Li, Q. Hu, X. Li, and Y. Wu, “Nanometer-thin indium tin oxide for advanced high-performance electronics,” Nature Mater., vol. 18, no. 10, pp. 1091–1097, Oct. 2019, doi: 10.1038/s41563-019-0455-8.

[5] M. Si, J. Andler, X. Lyu, C. Niu, S. Datta, R. Agrawal, and P. D. Ye, “Indium–Tin–Oxide transistors with one nanometer thick channel and ferroelectric gating,” ACS Nano, vol. 14, no. 9, pp. 11542–11547, Sep. 2020, doi: 10.1021/acsnano.0c03978.

[6] S. Samanta, K. Han, C. Sun, C. Wang, A. V.-Y. Thean, and X. Gong, “Amorphous IGZO TFTs featuring extremely-scaled channel thickness and 38 nm channel length: Achieving record high $G_{m,\text{max}}$ of 125 μS/μm at V_D of 1 V and Ion/Ioff of 350 μA/μm,” in Proc. IEEE Symp. VLSI Technol., Jun. 2020, pp. 1–2.

[7] W. Chakraborty, B. Grisafe, H. Ye, I. Lightcap, K. Ni, and S. Datta, “BEOL compatible dual-gate ultra thin-body W-doped indium oxide transistor with ion $\gg$10 μA/μm, SS = 73 mV/dec and Ion/Ioff ratio $\gg$ 4 x $10^9$,” in Proc. IEEE Symp. VLSI Technol., Jun. 2020, pp. 1–2.

[8] M. Si, Y. Hu, Z. Lin, X. Sun, A. Charnas, D. Zheng, X. Lyu, H. Wang, K. Cho, and P. D. Ye, “Why In$_2$O$_3$ can make 0.7 nm atomic layer thin transistors,” Nano Lett., vol. 21, no. 1, pp. 500–506, Jan. 2021, doi: 10.1021/acs.nanolett.0c03967.

[9] M. Si, Z. Lin, A. Charnas, and P. D. Ye, “Scaled atomic-layer-deposited indium oxide nanometer transistors with maximum drain current exceeding 2 A/mm at drain voltage of 0.7 V,” IEEE Electron Device Lett., vol. 42, no. 2, pp. 184–187, Feb. 2021, doi: 10.1109/LED.2020.3043430.

[10] M. Si, A. Charnas, Z. Lin, and P. D. Ye, “Enhancement-mode atomic-layer-deposited In$_2$O$_3$ transistors with maximum drain current of 2.2 A/mm at drain voltage of 0.7 V by low-temperature annealing and stability in hydrogen environment,” IEEE Trans. Electron Devices, vol. 68, no. 3, pp. 1075–1080, Mar. 2021, doi: 10.1109/TED.2021.3053229.

[11] M. Si, Z. Lin, Z. Chen, and P. D. Ye, “First demonstration of atomic-layer-deposited BEOL-compatible In$_2$O$_3$ 3D fin transistors and integrated circuits: High mobility of 113 cm$^2$/Vs, maximum drain current of 2.5 mA/μm and maximum voltage gain of 38 V/V in In$_2$O$_3$ inverter,” in Proc. Symp. VLSI Technol., 2021, pp. 1–2.

[12] A. Charnas, Z. Lin, Z. Zhang, and P. D. Ye, “Atomically thin In$_2$O$_3$ field-effect transistors with 10$^{17}$ current on/off ratio,” Appl. Phys. Lett., vol. 119, no. 26, Dec. 2021, Art. no. 263503, doi: 10.1063/5.0075166.

[13] P.-Y. Liao, M. Si, Z. Zhang, Z. Lin, and P. D. Ye, “Realization of maximum 2 A/mm drain current on top-gate atomic-layer-thin indium oxide transistors by thermal engineering,” IEEE Trans. Electron Devices, vol. 69, no. 1, pp. 147–151, Jan. 2022, doi: 10.1109/TED.2021.3125923.

[14] M. Si, Z. Lin, Z. Chen, X. Sun, H. Wang, and P. D. Ye, “Scaled indium oxide transistors fabricated using atomic layer deposition,” Nature Electron., vol. 5, no. 3, pp. 164–170, Mar. 2022, doi: 10.1038/s41928-022-00718-w.

[15] P.-Y. Liao, M. Si, Z. Zhang, Z. Lin, and P. D. Ye, “BEOL-compatible, ALD-grown In$_2$O$_3$ top-gate FETs with maximum drain current of 3 A/mm through thermal engineering and pulse measurement,” in Proc. Int. Symp. VLSI Technol., Syst. Appl. (VLSI-TSA), Apr. 2022, pp. 1–2.

[16] P. Giannozzi, S. Baroni, N. Bonini, M. Calandra, R. Car, C. Cavazzoni, D. Ceresoli, G. L. Chiarotti, M. Cococcioni, I. Dabo, A. D. Corso, S. D. Gironcoli, S. Fabris, G. Fratesi, R. Gebauer, U. Gerstmann, C. Gougoussis, A. Kokalj, M. Lazzeri, L. M. Santos, N. Marzari, F. Mauri, R. Mazzarello, S. Paolini, A. Pasquarello, L. Paulatto, C. Sbraccia, S. Scandolo, G. Sclauzero, A. P. Seitsonen, A. Smogunov, P. Umari, and R. M. Wentzcovitch, “QUANTUM ESPRESSO: A modular and open-source software project for quantum simulations of materials,” J. Phys., Condens. Matter, vol. 21, no. 39, Sep. 2009, Art. no. 395502, doi: 10.1088/0953-8984/21/39/395502.

[17] Z. Lin, M. Si, V. Askarpour, C. Niu, A. Charnas, Z. Shang, Y. Zhang, Y. Hu, Z. Zhang, P.-Y. Liao, K. Cho, H. Wang, M. Lundstrom, J. Maassen, and P. D. Ye, “A nanometer-thick oxide semiconductor transistor with ultra-high drain current,” 2022, arXiv:2205.00357.