Comparison techniques using phase – loop locked (PLL) and synchronous references frame (SRF) controller to mitigate voltage flicker

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Abstract. Voltage flicker is one of the vital disruptions in electrical distribution power systems. An electric arc furnace is considering as one of the major causes of voltage flicker due to it an unbalanced, nonlinear and time-varying behaviours. Distribution Synchronous static compensator (D-STATCOM) has been shown to be a competent and dynamic device to compensate voltage flicker in power system. This paper presents a comparison between Phase-Loop Locked (PLL) Controller and Synchronous References Frame (SRF) Controller technique for 6-pulse D-STATCOM to compensate voltage flicker due to electric arc furnace load. To observe the effectiveness of the proposed technique, testing has been conducted on IEEE 13 distribution bus test system. The simulation results show the effectiveness of 6-pulse D-STATCOM using PLL Controller compare to the SRF Controller techniques to alleviate the fast-varying voltage flicker.

1. Introduction
Voltage flicker is extremely hazardous to electrical loads, as their required stable voltage to function properly [1]. Electric arc furnace (EAF) are known as the most voltage fluctuation source due to the consuming very large active and reactive time varying powers during the melting and refining processes which cause irregular voltage oscillation in point of common coupling (PCC). This leads to undesirable effect on the electric light sources, performance of electronic components in the protective relays and shortening they lifetime [2].

The D-STATCOM based on the Voltage Source Converter (VSC) is a competent FACTS device for flicker mitigation better than Static Var Compensator (SVC) in term of fast response and flexible control [3]. However, the effectiveness of the D-STATCOM depend on the effectiveness of the control algorithm that has been used to extract the references voltage or current components to compensate the voltage fluctuation in power system.

The modified Synchronous References Frame (SRF) method based on Instantaneous Current Component ($i_d – i_q$) theory has been introduced in [4] and [5]. This method is similar to the current SRF method. The different between these methods in term of the generating references for the transformation angle. In this method, the compensating currents are taken from the instantaneous active and reactive current components of the nonlinear load thus produce non-constant transformation angle due to voltage harmonics and imbalances. This method has ability to reduce the flicker level into perceptible level.
However, the delay time response in control system is detected due to the used of two high pass filter components in this method. Therefore, the new controller scheme for 6-pulse D-STATCOM using PLL controller with PWM based on Hysteresis Current Control (HCC) switching as presented in [6] has been proposed to mitigate voltage flicker due to EAF load. It is expected to has a capability to mitigate voltage flicker for different flicker frequencies range of 8.8 Hz and 25 Hz compare to the SRF controller techniques.

2. Electric arc furnace model as voltage flicker source
The arc furnace model based on nonlinear differential equation is used to create the dynamic and multi-valued V-I characteristic of EAF load [7]. The steady-state (V-I) characteristic of the arc furnace presented as in Figure 1 using equation (1) is derived according to the principle of energy conversion for the electric arc furnace arc. It observed that, the anode-cathode voltage remains constant while the current is still changing in time once the arc ignition has been started [11][14].

\[ k_1 r^n + k_2 r \frac{dr}{dt} = \frac{k_3}{r^{m+2}} i^2 \]

Where:
- \( r \) is the arc radius
- \( i \) is the instantaneous arc current
- \( k_n \) is the proportionality constant for the model (\( n = 1,2,3 \))
- \( n \) is the arc cooling constant (\( n = 1,2,3 \))
- \( m \) is to reflect the fact that the arc may be hotter in the interior if it has a larger radius (\( m = 1, 2, 3 \))

In this research, the value of \( k_1=2750, k_2=1 \) and \( k_3=15.5 \) are chosen to indicate the EAF melting condition. The voltage fluctuation at PCC are then be calculated by using equation (2) which known as percentages of voltage fluctuation [3, 8-9].

\[
\text{Percentages of voltage fluctuation} = \left( \frac{U_{\text{max}} - U_{\text{min}}}{U_{\text{nom}}} \right) \times 100\% \tag{2}
\]

Where:
- \( U_{\text{max}} \) is the value of maximum voltage
- \( U_{\text{min}} \) is the value of minimum voltage
- \( U_{\text{nom}} \) is the average value of normal operating voltage

By using maximum permissible voltage fluctuations curve as indicates in [10], the value that obtained from equation (2) is observed either the voltage fluctuation will cause the irritation to the system when the magnitude of the voltage fluctuate exceed certain thresholds.
3. The modelling and control system of D-STATCOM

The D-STATCOM is a shunt-connected FACTS device. It is consists of a step-down transformer with leakage reactance, three-phase Pulse Width Modulation (PWM) with associated anti-parallel diodes and dc link capacitor to control the active power flow to the system as show in Figure 2 [10-11][14].

![Figure 2. D-STATCOM with the PLL Controller](image)

The D-STATCOM is in inductive condition if VSI output voltage, $U_{vsi}$ is greater than the AC voltage source at PCC, $U_{pcc}$. In this state, the current, $I$ flows through the leakage reactance, $X$ from the AC system to the D-STATCOM. Meanwhile, the D-STATCOM is in capacitive condition if the AC voltage source at PCC, $U_{pcc}$ is greater than the VSI output voltage, $U_{vsi}$. In this state, the current, $I$ flows through the leakage reactance, $X$ from the AC system to the D-STATCOM. In other condition, no power exchange occur if the amplitudes of the system and inverter voltage are equal [11][14]. The ability of D-STATCOM to inject or absorb reactive power to or from the power network, depend on the reactive current, $I$ drawn by synchronous compensator as indicate in equation (3).

$$I = \frac{(U_{pcc} - U_{vsi})}{X}$$ (3)

From equation (3), it is noticed that the magnitude of the AC system voltage, $U_{pcc}$, the inverter voltage, $U_{vsi}$ and leakage reactance, $X$ are important in order to reduce the voltage flicker into below maximum permissible voltage fluctuation curve [10].

3.1. Phase-Loop Locked (PLL) controller

The extraction of unit vector templates without using any transformation to generate the references voltage consist of two control loops as shown in Figure 3 [10-12][14].

![Figure 3. The Unit Vector Templates Generations of Phase-Loop Locked (PLL)](image)
The first control loop based on the extraction of the three-phase voltage fluctuation at PCC. The PLL will employ the voltage at PCC as references in order to produce the phase angle for the references source current. Equation (4), (5), and (6), express the PLL output and phase shift which used to generate three phase unity sinusoidal references source currents.

\[
U_{pcc}^A = \sin(\theta) \tag{4}
\]
\[
U_{pcc}^B = \sin(\theta - 120^\circ) \tag{5}
\]
\[
U_{pcc}^C = \sin(\theta + 120^\circ) \tag{6}
\]

The second control loop known as DC voltage control loop used to control the maximum value of the references source current, \(I_{m}\). In addition, the PI controller will control the part of the fundamental references source current, \(I_{mref}\) by comparing the measured DC voltage, \(U_{dc}\) with a references DC voltage, \(U_{dcref}\). The output from PI controller is then being added with a constant that equal to the maximum magnitude of the fundamental PCC current, \(I_{fpcc}\) and hence determine the magnitude references source current, \(I_{m}\). The maximum value of the references source current, \(I_{m}\) is being multiplied with the equation (4), (5) and (6) to obtain the references source current signals, \(I_{ref}\) for each phase as derived in equation (7), (8) and (9) [10][11][14].

\[
I_{refA} = U_{pcc}^A \sin(\theta) \times I_{m} \tag{7}
\]
\[
I_{refB} = U_{pcc}^B \sin(\theta - 120^\circ) \times I_{m} \tag{8}
\]
\[
I_{refC} = U_{pcc}^C \sin(\theta + 120^\circ) \times I_{m} \tag{9}
\]

3.2. **Hysteresis current control of pulse width modulation scheme**

The hysteresis comparator output with suitable band (±h) will determine the switching pattern of the inverter as shown in Figure 4.

![Hysteresis current control of pulse width modulation scheme](image)

**Figure 4.** The HCC Techniques of PWM Scheme

If the source current signal, \(I_s\) exceeds a predefined hysteresis band (HB), the gate, \(G_n\) will send 0 logic value to turn OFF the upper switch in the half-bridge and turned ON the lower switch. Meanwhile, if the source current, \(I_s\) reaches the goes below the HB, the gate, \(G_n\) will send 1 logic value to turn ON the upper switch in the half-bridge and turned OFF the lower switch [10-11][14].

4. **Voltage fluctuation by electric arc furnace model**

The IEEE 13 distribution system [14] as illustrated in Figure 5 used to represent a medium-sized industrial plant with a utility supply at 69 kV and the local distribution system operates at 13.8 kV [10][11][14].
Firstly, the non-linear of EAF load are connected at bus 3 (PCC) with different flicker frequencies of 8.8 Hz and 25 Hz. The connection of this EAF at bus 3 will cause the erratic variation of the arc resistance and causes variation in EAF voltage and hence caused voltage fluctuation not only at bus 3 as shown in Figure 6 but also other load that connected to the PCC.

![IEEE 13 Distribution System with EAF Load and D-STATCOM FACTS Device](image)

**Figure 5.** The IEEE 13 Distribution System with EAF Load and D-STATCOM FACTS Device

![Dynamic variation of arc resistance](image)

(a)

![Variation of EAF voltage](image)

(b)

![Voltage flicker at bus 3 without Mitigation Device](image)

(c)

**Figure 6.** 8.8 Hz flicker frequency (a) Dynamic variation of arc resistance (b) Variation of EAF voltage (c) Voltage flicker at bus 3 without Mitigation Device
From Figure 6, it is noticed that the measurement at bus 3 produced the result of $V_{\text{max}} = 10.78$ V and $V_{\text{min}} = 10.43$ V. By using equation (2), the percentages of voltage fluctuation at bus 3 is 3.3003 %. It indicates that the voltage flicker at bus 3 is exceeded the allowable limit of 1.4 % and the mitigation devices are required to reduce the fluctuation.

5. Test system
To discover the effectiveness of the proposed scheme when compared to the SRF techniques, the variation of fluctuation frequency between lowest to highest frequency of 8.8Hz and 25Hz are carefully studied. The DSTATCOM with PLL controller are installed at PCC have capabilities to stabilizes the voltage at bus 3 by reducing the voltage variation as shown in Figure 7. The maximum and minimum value of voltage that have been measured in Figure 7 then being substitute in equation (2) and the percentage of fluctuation has been reduced to 1.3454 % as compare to 3.3003 %. This resulting percentage of voltage fluctuation is below the maximum permissible level of 1.4 %.

![Figure 7. Three Phase Voltage at Bus 3 with PLL Controller at 8.8 Hz Frequency](image)

Table 1 shows the capabilities of PLL and SRF controller on IEEE 13 distribution bus test system to mitigate the voltage fluctuation at lower fluctuation frequencies of 8.8 Hz. It shows that, the both controller has capability to keep the voltage fluctuation below the maximum permissible voltage fluctuation curve of 1.4 % as well as SRF techniques in [6].

| Bus bar | Percentages of Voltage Fluctuation Without Compensator (%) | Percentages of Voltage Fluctuation with Compensator (%) | Maximum Permissible Voltage Fluctuation Based on IEEE Std. 141-1993 (%) |
|---------|-----------------------------------------------------------|---------------------------------------------------------|------------------------------------------------------------------|
|         | PLL Controller | SRF Controller | PLL Controller | SRF Controller |
| Bus1    | 0.2309         | 0.2309         | 0.2309         | √               | √               |
| Bus2    | 0.2309         | 0.2309         | 0.2309         | √               | √               |
| Bus3    | 3.3003         | 1.3454         | 1.2951         | √               | √               |
| Bus4    | 1.2727         | 0.6355         | 1.0919         | √               | √               |
| Bus5    | 1.1848         | 1.0554         | 1.0526         | √               | √               |
| Bus6    | 3.3003         | 1.3461         | 1.2975         | √               | √               |
| Bus7    | 3.3003         | 1.3461         | 1.2975         | √               | √               |
| Bus8    | 3.3003         | 1.3461         | 1.2975         | √               | √               |
| Bus9    | 3.2787         | 1.3422         | 1.0695         | √               | √               |
| Bus10   | 3.4976         | 1.25           | 1.25           | √               | √               |
| Bus11   | 3.2967         | 1.2138         | 1.3423         | √               | √               |
| Bus12   | 3.0014         | 1.0724         | 1.3316         | √               | √               |
| Bus13   | 5.1026         | 0.3245         | 0.5405         | √               | √               |
The both controllers are also has been tested for the high flicker frequencies of 25 Hz. The simulation results show in Table 2 indicate that the PLL controller have capability to detect and mitigate the voltage fluctuation not only at bus 3 (PCC) but also the heavy loads connected to it. By using equation (3), it indicates that the percentages of flicker for all the flicker frequencies are below the maximum permissible limit of voltage fluctuation. However, it is differ when using the SRF techniques in [6] which only the voltage fluctuation at bus bar 1, 2, 3, 4, 5, 6,7 and 8 that connected closed to the PCC is mitigate but not capable to mitigate the voltage fluctuation for the bus bar that connected far from PCC such as bus bar 9,10,11,12 and 13. It is due to the increasing of unbalanced factor that cause the decoupling between real power loop and reactive power loop is degraded. It is thus degraded the capability of the DSTATCOM with the SRF techniques as the flicker frequency increase.

| Bus bar | Percentages of Voltage Fluctuation Without Compensator (%) | Percentages of Voltage Fluctuation With Compensator (%) | Maximum Permissible Voltage Fluctuation Based on IEEE Std. 141-1993 (%) |
|---------|----------------------------------------------------------|--------------------------------------------------------|---------------------------------------------------------------------|
| Bus1    | 0.2309                                                   | 0.2309                                                  | √                                                                   |
| Bus2    | 0.2309                                                   | 0.2309                                                  | √                                                                   |
| Bus3    | 2.9287                                                   | 1.2903                                                  | √                                                                   |
| Bus4    | 1.3667                                                   | 0.9132                                                  | √                                                                   |
| Bus5    | 1.174                                                    | 0.79681                                                 | √                                                                   |
| Bus6    | 3.0246                                                   | 1.6807                                                  | √                                                                   |
| Bus7    | 3.0217                                                   | 1.6807                                                  | √                                                                   |
| Bus8    | 3.1147                                                   | 1.6807                                                  | √                                                                   |
| Bus9    | 3.2345                                                   | 3.0848                                                  | X                                                                   |
| Bus10   | 3.1949                                                   | 4.5113                                                  | X                                                                   |
| Bus11   | 2.7548                                                   | 2.5974                                                  | X                                                                   |
| Bus12   | 3.8462                                                   | 2.5839                                                  | X                                                                   |
| Bus13   | 3.3149                                                   | 3.0612                                                  | X                                                                   |

Note:
√ means the percentages flicker is below maximum permissible voltage fluctuation of 1.7 (%)  
X means the percentages flicker is above maximum permissible voltage fluctuation of 1.7 (%)
6. Conclusion
The proposed control algorithm which considers voltage as references value for both voltage control loop and DC link control loop will effectively affect the accuracy of the mitigation and the time response of the controller. It is shows that the proposed techniques not only have ability to reduce voltage flicker at PCC but also manage to reduce voltage fluctuation at the bus that connected far from D-STATCOM into below maximum permissible voltage fluctuation curve for various flicker frequencies range. The linearity that exist in this proposed controller allow the detection time is relatively fast compare to the SRF technique by injected the reactive power below 0.1s at Point of Common of Coupling.

Acknowledgement
The author would like to extend their gratitude to Universiti Teknologi MARA for supports on the project in term of scholarship and financial support.

References
[1] Sun J Czarkowski D and Zabar Z 2002 Voltage flicker mitigation using PWM-based distribution STATCOM IEEE Power Engineering Society Summer Meeting Chicago, IL, USA, 1, p. 616-621.
[2] Baggini A 2008 Handbook of Power Quality: John Wiley & Sons.
[3] Leinonen A and Laketic N 2018 Advanced technology to ensure EAF grid flicker compliance 2018 IEEE International Conference on Environment and Electrical Engineering and 2018 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I&CPS Europe), Palermo, p. 1-4.
[4] Mienski R Pawelek R and Wasiak I 2004 Shunt compensation for power quality improvement using a STATCOM controller: modelling and simulation Generation, Transmission and Distribution, IEEE Proceedings 151, p. 274-280.
[5] Alzate A Escobar A and Marulanda J J 2011 Application of a D-STATCOM to mitigate arc furnaces power quality problems in PowerTech 2011 IEEE Trondheim, p. 1-6.
[6] Srinath S Selvan M P and Vinothkumar K 2010 Comparative evaluation of performance of different control strategies on UPQC connected distribution system in Industrial and Information Systems (ICIIS), 2010 International Conference, p. 502-507.
[7] Acha E Semlyen A and Rajakovic N 1990 A harmonic domain computational package for nonlinear problems and its application to electric arcs Power Delivery IEEE Transactions on 5, p. 1390-1397.
[8] Belkhayat M Edwards J Hoonchareon N Marte O and Stenberg D 1995 Transients in Power Systems Purdue University.
[9] Short T 2004 Electric Power Distribution Handbook CRC Press LLC.
[10] IEEE 1994 IEEE Recommended practice for electric power distribution for industrial plants IEEE Std 141-1993, p. 1-768.
[11] Jamaludin N F and Abidin A F 2013 Phase-Locked Loop (PLL) controller for distribution synchronous static compensator (DSTATCOM) to mitigate voltage flicker 2013 IEEE 7th International Power Engineering and Optimization Conference (PEOCO).
[12] Faiz J and Zafari A 2010 A novel algorithm for determination of reactive currents in STATCOM for voltage flicker mitigation Journal Electrical Systems (JES).
[13] Selvan M P and Srinath S 2011 A combined mode of control for unified power quality conditioner connected to a low voltage distribution system Australian Journal of Electrical & Electronics Engineering 8, p. 257-270.
[14] Jamaludin N F Abidin A F Anuar N Shamsuddin S A 2016 Mitigation of voltage flicker using phase-lock loop (PLL) controller of distribution synchronous static compensator (D-STATCOM) International Journal Of Simulation, Systems, Science & Technology (IJSSST) 17, 41,41.1-41.6.