High Speed Power Efficient CMOS Inverter Based Current Comparator in UMC 90 nm Technology

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ABSTRACT
A novel power-speed efficient current comparator is proposed in this paper. It comprises of only CMOS inverters in its structure, employing a simple biasing method. The structure offers simplicity of design. It possesses the very desirable features of high speed and low power dissipation, making this structure a highly desirable one for various current mode applications. The simulations have been performed using UMC 90 nm CMOS technology and the results demonstrate the propagation delay of about 3.1 ns and the average power consumption of 24.3 µW for 300 nA input current at supply voltage of 1V.

Keyword:
CMOS Inverter
Current Comparator
Power dissipation
Propagation delay
Transconductance

1. INTRODUCTION
Current mode signal processing in CMOS technology has received great interest in the past few decades [1]-[9]. Of numerous current mode building blocks that exist, a current comparator is one fundamental block that finds usage in various applications such as temperature sensors, photo-sensors, current Schmitt Triggers, current-mode Analog to Digital converters, oscillators, current to frequency converters, neural networks, function generators etc. [10]-[20].

For an efficient current comparator, the most important requirement is a fast time response followed by its accuracy. Numerous architectures of current comparators have been put forth in the literature but the earliest known true CMOS current comparator was proposed by Frietas and Current in [20]. This structure was based on the use of a simple current mirror for current comparison purpose. However, it was limited by its speed of operation. To improve upon this limitation, the current comparators using a nonlinear positive feedback were proposed in [22]-[23]. In [22] the first true low input impedance current comparator was proposed. This circuit used a source follower input stage to obtain low input resistance but it suffers from longer response time for low input currents, which limits its performance. [23] Proposed two CMOS current comparator structures to obtain better resolution and offset than that attained with [22]. One of these structures utilizes current switching as in [22] to obtain a linear transient evolution dominated by a Miller capacitance. Second structure, the current steering comparator an alternate principle to reduce Miller effect exhibits better transient response along with high-resolution. But the positive feedback applied at the input led to a lower sensitivity which, in turn, lowered the speed for low input levels. Various structures subsequently were proposed in [24]-[30] to overcome the limitations posed by the previous structures, each having its own respective merits and demerits. In [24], the structure of [22] has been modified to include...
class AB operation in order to reduce the voltage swing, thus resulting in greater speed at small input currents. The structure proposed in [25] is a modification of [22] to obtain a fast response time along with low input impedance by appending two inverters to the structure of [22]. Further, in [26] the structure of [22] has been modified for reducing delay times. It employs diode-connected NMOS and PMOS transistors that restrict the input transistors from entering deep subthreshold region of operation. Since this structure requires two wide width diode-connected transistors stacked together, hence it leads to the complication in the circuit topology.

Many structure employ feedback mechanism in order to reduce in put resistance, thereby increasing the speed. Such structures have been reported in [27]-[30]. [27] Employs a resistive feedback network in a current-source inverting amplifier at input stage of [22] in order to reduce the input resistance. This leads to a high speed current comparator that offers low input resistance for increased input current sinking and sourcing capabilities. [28] Proposes a continuous-time current comparator to achieve short response delay time, low power consumption, small area and process robustness. It employs a CMOS complementary amplifier two resistive-load amplifiers and two CMOS inverters. A transistor working in linear region serves as the negative feedback resistor of the CMOS complementary amplifier. The structure offers low input and output impedance, owing to the resistive feedback. These low input and output resistances decrease the voltage swings thereby reducing the response time of the circuit. [29] Employs a feedback system to the input stage of [22] that allows high-speed operation at low currents and also consumes lesser power than [22]. The current comparator in [30] is developed by applying positive feedback concept around an active block namely CC-II and gives a high speed response.

Further, [31]-[34] employ various biasing techniques to reduce input impedance and hence achieve higher speeds of operation while maintaining lower power consumption. Specifically, simple biasing method is used in [31] and [33] whereas [32] uses negative feedback scheme at the transimpedance stage with an aim to achieve a very large loop-gain while maintaining the transformed voltage signal gain at the lowest swing in order to achieve speed.

The quest to develop more efficient structures that meet the criteria of high speed and accuracy along with additional features such as low power dissipation is on-going. Authors have also proposed two such structures in [34]-[35]. In [34], a current comparator comprising a current difference stage, a gain stage with non linear feedback and an output stage has been proposed. It uses a current mirror structure as a current difference stage and a CMOS inverter is used as the output stage for rail to rail swing. Further, in [35] a low power, high speed and high resolution current comparator has been proposed as an improvement upon [22] wherein the gain stage has been modified leading to a significant improvement in the delay.

In this paper, we have proposed a high speed, low power current comparator structure employing only CMOS inverters as the basic building blocks. A CMOS inverter is a fundamental block in the digital integrated circuit design techniques. It finds wide usage in implementation of various structures as reported in [36]-[40], that are made exclusively out of CMOS inverters thus offering symmetry of structure, endowed with all qualities of the CMOS inverter. The current comparator proposed in this work has highly desirable features of speed and power efficiency with ease of operation using UMC 90 nm CMOS technology.

2. PROPOSED CURRENT COMPARATOR

The proposed high speed and low power consumption current comparator design based on conventional CMOS inverter is shown in Figure 1. The architecture consists of three stages of CMOS inverters: a bias stage ($A_1$), an input stage ($A_2$) which accepts the input current pulse and translates it into corresponding voltage level and an output stage ($A_3$) to obtain a full swing output.
Figure 1. Proposed CMOS inverter Based Current Comparator Structure (a) transistor configuration, (b) equivalent symbol representation

The operational concept of proposed current comparator design can be elucidated as follows. $A_1$ comprises of a shorted gate drain CMOS inverter (M1-M2). The primary function of this stage is to provide a constant voltage bias of about $V_{DD}/2$ to the input stage $A_2$. Around this common mode voltage of $V_{DD}/2$, the voltage signal swing at X can be maintained as small as possible and situated exactly around the inverter threshold voltage of $A_2$. This ensures a very high speed operation of the current comparator. The transistor lengths and widths ratios $W_1/L_1$ and $W_2/L_2$ of $A_1$ are set in order to obtain the required bias. This can be verified by equating the saturation drain current equation of PMOS and NMOS since both M1 and M2 being diode connected MOSFETs will operate in the saturation region of operation.

$$\mu C_{ox} \left( \frac{W}{L} \right)_1 (V_{gs} - V_{th})^2 (1 + \lambda V_{ds}) = \mu C_{ox} \left( \frac{W}{L} \right)_2 (V_{gs} - V_{th})^2 (1 + \lambda V_{ds})$$  \hspace{1cm} (1)

$$\left( \frac{W}{L} \right)_1 = \mu C_{ox}(V_{gs} - V_{th})^2 (1 + \lambda V_{ds})$$

$$\left( \frac{W}{L} \right)_2 = \mu C_{ox}(V_{gs} - V_{th})^2 (1 + \lambda V_{ds})$$  \hspace{1cm} (2)

For small channel lengths, $\lambda$ (channel modulation coefficient) cannot be ignored. Hence, by fixing the channel length and substituting the typical values of technology dependent parameters like $\lambda$, $V_t$ and $k'(\mu C_{ox})$, the aspect ratios of two devices can be calculated using eq (1) and (2). The input stage $A_2$ also serving as the transimpedance stage consists of M3-M4. In this novel approach, the input current $I_{in}$ which is the difference of signal and reference current is injected into the drain terminal of input stage. A corresponding voltage level with respect to the input current pulse is generated at node X. Essentially; this voltage level appearing at X is a potential drop across $r_{o3} || r_{o4}$ where $r_{o3}$ and $r_{o4}$ are output resistances of M3 and M4 respectively. This is also a measure of net transimpedance in the circuit. Note that an output resistance $r_{o3}$ is approximately inversely proportional to the drain current $I_{ds}$, i.e. $r_{o3} = 1/(\lambda I_{ds})$ in saturation region of operation. The key point here is that the $I_{in}$ should vary the voltage at X by a small amount only which can be sensed by the output stage. This ensures the high speed operation of the comparator circuit. Dimensions of M3-M4 are chosen taking into consideration the inverse relationship between the drain current and $r_{o3}$ to ensure a large sensitivity of $V_x$ with respect to $I_{in}$. Thus, even a small input signal will cause large variations in the potential at node X. At the same time, the absence of any input signal will cause the potential at X to drop, thereby resulting in a low voltage level at X. Non-idealities in the form of finite input impedance of output stage will affect the performance of the circuit.

The voltage generated at node X feeds the transistors of output stage (M5-M6). The transistor pair (M5-M6) senses the distinctions applied in the form of gate voltage and outputs high or low voltage as logic ‘1’ or logic ‘0’. This inverter ($A_3$) produces full swing output without degrading the speed of the circuit.
3. RESULTS AND ANALYSIS

The proposed current comparator topology based on CMOS inverters have been designed using 90 nm CMOS technology parameters and Analog Virtuoso Environment of the Cadence Software. The sizes of the transistors are listed in Table 1. The simulations are performed at a supply voltage ($V_{DD}$) of 1 V. The input current varying between 0 and 300 nA is injected and compared. Figure 2 illustrates the transient input–output characteristics of the proposed current comparator along with the instantaneous power dissipation of the structure. A short average propagation delay of 3.1 nsec is observed at the specified input current, reinstating the operating frequency range of circuit between 200 MHz- 400 MHz.

Table 1. Transistor Sizes

|   | W    | L    |
|---|------|------|
| M1| 1.32µ | 0.18µ |
| M2| 0.2µ  | 0.18µ |
| M3| 4.5µ  | 1.0µ  |
| M4| 1.5µ  | 2.0µ  |
| M5| 1.32µ | 0.18µ |
| M6| 0.2µ  | 0.18µ |

Figure 2. Transient Response showing (a) Input Current and Output Voltage and (b) Instantaneous Power Dissipation of the proposed structure when $I_{in} = 300$ nA.
Power dissipation for various input currents is one of the characteristics of this circuit. The instantaneous power dissipation of the circuit is shown in Figure 2(b). Based upon this characteristic, the average power dissipation is calculated to be 24.3 µW at 1 V for 300 nA input current. To exhibit the performance of the circuit at current greater than, 1 µA, the circuit performance is evaluated at 2 µA and the same is depicted in Figure 3. The simulation results show that a six fold increase in current doesn’t escalates the power consumption of the circuit by the same amount. Besides, the propagation delay reduces substantially for currents greater than 1 µA thereby increasing the speed of comparator considerably.

The average propagation delay of the circuit, under different input currents are presented in Figure 4(a) and the variation of average propagation delay with supply voltage has been illustrated in Figure 4(b). As expected, the delay decreases as the supply voltage increases because of increase in drain current.
Temperature variations and Process parameters have significant impact on the performance of CMOS circuits. To illustrate the robustness of proposed architecture, average propagation delay and power dissipation have been calculated for various values of temperature ranging from as low as -5°C to as high as 150°C. From Figure 6(a), as temperature increases from -5°C to around room temperature the delay decreases and then delay increases almost linearly with temperature due to decrease in drain current. Similar temperature variations have been simulated for power dissipation of proposed current comparator (Figure 6(b)). In these simulations both maximum and minimum values of power have been illustrated. The noteworthy aspect of the power model is that even with large variations in temperature (-5°C to 150°C), the power dissipation remains almost constant. Furthermore, the difference between maximum and minimum propagation delay is not more than 2 ns.

![Figure 5. Average Power Dissipation vs. Input Current](image)

Figure 5. Average Power Dissipation vs. Input Current

![Figure 6. (a) Average Propagation Delay vs. Temperature, (b) Power Dissipation vs. Temperature](image)

Figure 6. (a) Average Propagation Delay vs. Temperature, (b) Power Dissipation vs. Temperature

Figure 7 illustrates the variation of output voltage with temperature in a much eloquent manner.
To further exemplify the functionality of the circuit, the proposed design has been simulated for all the process corners as shown in Figure 8.

The structure proposed in [22] is one of the pioneering works in terms of the design of a current comparator. [23]-[30] have reported various current comparators that are a modification of [22]. Of all these, [24] gives the highest speed and lowest power dissipation. Hence, a comparison of the performance parameters of the proposed current comparator to those reported in [22] and [24] has been drawn and same has been reported in Table 2. It can be seen that the proposed structure offers fastest response and reasonably low power dissipation at the lowest supply voltage of 1V with a much lower input current. Figure 9 illustrates the output response of [22] while that of [24] has been illustrated in Figure 10.
Table 2. Comparison of Proposed Current Comparator with Popular Architectures [22] and [24]

| Process | Supply Voltage (V) | Minimum Input Current | Avg Propagation Delay (ns) | Power Dissipation (µW) | Power-Delay Product (fJ) | No. of Transistors |
|---------|-------------------|-----------------------|---------------------------|-----------------------|------------------------|-------------------|
| Traff [21] | 90 nm | 1 | 5 µA | 3.35 | 120.2 | 112.57 | 4 |
| Tang [23] | 90 nm | 1 | 10 µA | 4.6 | 112.57 | 517.8 | 14 |
| Proposed | 90 nm | 1 | 300 nA | 3.1 | 24.3 | 93 | 6 |

4. CONCLUSION

A fast and power efficient current comparator has been reported comprising solely of CMOS inverters, thus offering symmetry of structure. The proposed current comparator provides a commendable performance in comparison to the other popularly used current comparators as reported in the literature. The proposed structure has been simulated on 90 nm technology and operates at a supply voltage of 1V.

REFERENCES

[1] Tomazou C, Lidgey FJ, Haigh D. Analogue IC Design The Current-Mode Approach. U K IEE. 1990.
[2] Tomazou C, Lidgey FJ, Haigh D. Switched-Currents: An Analogue Technique for Digital Technology. U K IEE. 1993.
[3] Wang Z. Current-mode CMOS integrated circuits for analog computation and signal processing A tutorial. *International Journal of Analog Integrated Circuits Signal Processing*, 1991; 1: 287-295.
[4] Yuan F. CMOS Current-Mode Circuits for Data Communications. *Springer*. 2007; XVIII: 290, 2007.
[5] Ismal M, Fiesz T. Analog VLSI Signal and Information Processing. *New York McGraw-Hill*, 1994.
[6] Maslenikow O, Pawlowski P, Soltan P, Berezowski R. Current-mode digital gates and circuits: concept, design and verification. 2002 9th International Conference on Electronics, Circuits and Systems. 2001; 2: 623-626.
[7] Hassan H, Anis M, Elmasry M. MOS current mode circuits: analysis, design, and variability. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*. 2005; 13(8): 885-898.
[8] Layos MC, Haritantis I. Second order current mode circuits based on the general current conveyor. 1990 Third IEEE International Conference on Electronics, Circuits, and Systems. 1996; 1: 362-365.
[9] Kurnaz M, Minaei S, Goknar IC. Time delay calculation in current-mode circuits. 2013 8th International Conference on Electrical and Electronics Engineering (ELECO), 2013: 349-352.
[10] Crolla P. A fast latching current comparator for 12-bit A/D applications. *IEEE Journal of Solid State Circuits*, 1982; SC-17: 1088-1093.
[11] Robert J, et al. Novel CMOS pipelined A/D converctor architecture using- current mirrors, *Electronic Letters*, 1989; 25: 691-692.
[12] Nairn D, Salama C. Current-mode algorithmic analog-to-digital converters. *IEEE Journal of Solid-State Circuits*, 1990: 25: 997-1004.
[13] Chong CP. A technique for improving the accuracy and the speed of CMOS current-cell DAC. *IEEE Transactions on Circuits and System*. 1990; 37: 1325-1327.
[14] Nairn D, Salama C. A ratio-independent algorithmic analog-to digital converter combining current mode and dynamic techniques. *IEEE Transactions on Circuits and Systems*. 1990; 37: 1325-1327.
[15] Wang Z. Design methodology of CMOS algorithmic current A/D converters in view of transistor mismatches. *IEEE Transactions on Circuits and Systems*. 1991; 38: 660-667.
[16] Eom SW, Em SW. Current-mode cyclic ADC for low power and high speed applications. *Electronic Letters*. 1991; 27: 818-820.
[17] Wey C. Concurrent error detection in current-mode A/D converters. *Electronic Letters*.1991; 27(25): 2370-2372.
[18] Yamamoto M, et al. *Switched current F/I and I/F converters*. 1991 European Conference on Circuit Theory and Design-91, ECCTD-91. 1991. 25.
[19] Current K, Current J. CMOS current-mode circuits for neural networks. 1990 IEEE International Symposium on Circuits and Systems. 1991; 4: 2971-2974.
[20] Hamiane M. A CMOS-based Analog Function Generator: HSPICE Modeling and Simulation. *International Journal of Electrical and Computer Engineering*, 2014; 4(4): 532-538.
[21] Freitas D, Current K. CMOS current comparator circuit. *Electronic Letters*. 1991; 19(17): 695-697.
[22] Traff H. Novel approach to high speed CMOS current comparators. *Electronic Letters*. 1992; 28(3): 310-312.
[23] Dominguez-Castro R, Medeiro F, Delgado-Restituto M. et al. High Resolution CMOS Current Comparators: Design and Applications to Current-Mode Function Generation. *International Journal of Analog Integrated Circuits and Signal Processing*, 1995; 7 (Special Issue on Current-Mode Circuits): 149-165.
[24] Tang ATK, Tomazou C. High performance CMOS current comparator. *Electronic Letters*. 1994; 30: 5-6.
[25] Tang X, Pun KP. High-performance CMOS current comparator. *Electronic Letters*. 2009; 45: 1007-1009.
[26] Ravezz L, Stoppa D, Della-Beta GF. Simple high-speed CMOS current comparator. *Electronic Letters*. 1997; 33: 1829-1832.
[27] Min BM, Kim SW. High performance CMOS current comparator using resistive feedback network. *Electronic Letters*. 1998; 34: 2074-2076.
[28] Chen L, Shi B, Lu C. Circuit Design of a High Speed and Low Power CMOS Continuous-time Current Comparator. *International Journal of Analog Integrated Circuits and Signal Processing*. 2001; 28: 293-297.

[29] Banks D, Tournazou C. Low-power high-speed current comparator design. *Electronic Letters*. 2008; 44: 171-172.

[30] Chavoshisani R, Hashemipor O. A high-speed current conveyor based current comparator. *Microelectronics Journal*. 2011; 42: 28-32.

[31] Ziaabakhsh S, Alavi-Rad H, Alavi-Rad M, Mortazavi M. The design of a low-power high-speed current comparator in 0.35-μm CMOS technology. 2009 Quality of Electronic Design. 2009; 107-111.

[32] Moolpho K, Ngarmnil J, Sitjongsataporn S. A high speed low input current low voltage CMOS current comparator. 2003 International Symposium on Circuits and Systems. 2003; 1: I-433-I-436.

[33] Ziaabakhsh S, Rad HA, Saberkari A, Shokouhi S.B. An ultra high speed low-power CMOS integrated current comparator. 2008 3rd International Design and Test Workshop. 2008; 159-164.

[34] Sridhar R, Pandey N, Bhatia V, Bhattacharyya A. High Speed High Resolution Current Comparator and its Application to Analog to Digital Converter. *Springer’s Journal of Institution of Engineers India Ser. B*, DOI 10.1007/s40031-015-0189-1.

[35] Sridhar R, Pandey N, Bhatia V, Bhattacharyya A. On improving the performance of Traff's comparator. 2012 IEEE 5th India International Conference on Power Electronics (ICPE). 2012; 1-4.

[36] Agrawal N, Paily R. A threshold inverter quantization based folding and interpolation ADC in 0.18 μm. *International Journal of Analog Integrated Circuits and Signal Processing*. 2010; 63(2): 273-281.

[37] Suadet A, Kasemwan V. A CMOS inverter-based class-AB pseudo differential amplifier for HF applications. *IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC-2010)*, 2010; 14.

[38] Hsia SC, Lee WC. A very low-power flash A/D converter based on CMOS inverter circuit. Fifth International Workshop on System-on-Chip for Real-Time Applications, 2005; 107-110.

[39] Kolodziejski W, Machowski, W, Jasielski, J, Kuta S. Low voltage charge-pump-based VCO circuits using CMOS inverters as building blocks. *International Conference on Signals and Electronic Systems*. 2008; 147-152.

[40] Al A, Ibne Reaz MB, Jalil J, Mohd. Ali Mohd. AB. An Improved A Low Power CMOS TIQ Comparator Flash ADC. *TELKOMNIKA Indonesian Journal of Electrical Engineering*. 2014; 12(7): 5204-5210.

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