Design of DC Magnet Power Supply System for ITER Static Magnetic Field Test Facility

Xi Deng, Li Jiang, Ya Huang, and Ge Gao

Abstract—International Thermonuclear Experimental Reactor (ITER) static magnetic field (SMF) test facility requires a dc power supply with low voltage, high current, and low harmonics under high power density. Due to the limitation of switching loss, there is a contradiction between the output current capability and the output ripple. Large output current usually leads to low switching frequency, and low switching frequency will generate a large number of harmonics. To solve the problems, a topology based on the interleaving parallel buck converter is used and tested in this article. Moreover, the topology is realized with only a small number of switching metal–oxide–semiconductor field-effect transistors (MOSFETs). This article introduces the system design scheme and control method in detail. The analysis of harmonic and simulation is carried out. The validity of the proposed scheme and control strategy was confirmed by experiments, and the power supply system can supply a large current of 12.23 kA and has the ability of low ripple.

Index Terms—Interleaving parallel buck converter, International Thermonuclear Experimental Reactor (ITER), large output capability, multilevel, static magnetic field (SMF) test facility.

I. INTRODUCTION

The maximum static magnetic induction in the space around the International Thermonuclear Experimental Reactor (ITER) tokamak device exceeds 200 mT [1]–[4]. Such a high space magnetic field will affect the operational stability and reliability of the entire nuclear fusion device system. To study the impact of the ITER tokamak device’s ultrahigh spatial magnetic field distribution on the device components during operation, a high current and high stability power supply are needed to establish a corresponding test magnetic field to test the key components of the tokamak device. The test facility mainly consists of an inductance coil, cooling system, adjustable power supply, the electronic device under test (EUT), and auxiliary equipment, as shown in Figs. 1 and 2.

The design of the static magnetic field (SMF) magnet power supply faces challenges, due to the requirement of high current and low harmonics under high power density. To get high output current ability, the switching frequency of the switching device is low, which leads to an increase in the output ripple, which in turn affects the stability of the power supply. Meanwhile, to maintain the stability of the system, the filter parameters of the power supply need to be increased, which reduce the power density of the system. There are similar technical requirements (high current, low voltage, and low current ripple) for other power supplies, such as the in-vessel power supply for experimental advanced superconducting tokamak (EAST). Since the power supply requires a four-quadrant operation, the H-bridge carrier phase shift (CPS) multilevel technology is applied to solve the contradiction between high power and low harmonic by increasing the equivalent switching frequency [5], [6], but the CPS multilevel
H-bridge contains many switching devices, so its complexity has risen to a large extent. This article proposes a topology based on the interleaving parallel buck converter. This interleaving parallel buck converter can effectively achieve high current output and high stability at the same time by eliminating low-order harmonics and increasing the equivalent switching frequency. The interleaving parallel buck topology is easy to achieve redundancy and ensure reliability. Moreover, this multilevel topology needs only a small number of switching tubes, which reduce the total cost of equipment. The validity of the proposed scheme and control strategy was confirmed by simulation and experiments.

II. TOPOLOGY OF SMF TEST FACILITY POWER SUPPLY

SMF test facility power supply has the characteristics of large output current and high output stability, which needs switching device with high switching frequency and high output current. Integrated gate commutated thyristor (IGCT) and injection enhanced gate transistor (IEGT) can output large current and high voltage, but its switching frequency is low. High-voltage insulated gate bipolar transistor (IGBT) cannot output high current. Considering the output characteristics of the above switching devices, medium-voltage IGBT and metal–oxide–semiconductor field-effect transistor (MOSFET) are good choices. In this article, MOSFET MD680HFN100B3S with 680-A rated current and 10-kHz switching frequency is applied to ensure high resolution and high precision current control. Since the switching frequency of MOSFET is high, the dynamic current sharing problem of parallel MOSFET is difficult to solve. So, the topology of the interleaving parallel buck converter, shown in Fig. 3, is adopted in this article. Each buck circuit uses an independent industry standard rectifier module and is connected in parallel. The equivalent frequency exceeds 120 kHz. The interleaved trigger modulation method is described in detail in the next section.

The power supply system of the SMF test facility consists of 24 power units. All 24 power units are connected in parallel to output 250–12230 A. Each power unit can convert the ac grid input into a dc constant current of a specified size. The output current of each power unit is 0–570 A. The power unit is consisted of an electromagnetic interference (EMI) filter, industry-standard rectifier module, three parallel buck modules, control and protection module, communication module, and auxiliary power system, as shown in Fig. 4.

We divide 24 power modules into two groups. Among them, the buck circuits of 12 power modules in each group are interleaved in parallel. The main technical indexes of the system are shown in Table I.

III. INTERLEAVING PARALLEL MODULATION METHOD

A. Modulation Method Based on Interleaved Trigger Method

In the parallel power supply system, the switch device driving modes of each module are divided into three types, as shown in Fig. 5. Synchronous triggering refers to an identical driving signal for driving the respective switch modules. The total inductor ripple current is superimposed and increased in this case. The independent triggering method means that the switching frequency of each module is inconsistent. When using this method, the total inductor ripple current is superimposed randomly and irregularly. For interleaved trigger method, the switching frequency of each module is the same, and the drive signal has a regular phase difference. So, the
current ripple of each module will cancel each other out. The harmonic of the parallel system will be reduced. The design adopts a 12-phase interleaved trigger buck topology. For convenience, this article takes a four-phase interleaved trigger buck topology as an example for subsequent analysis.

The four-phase interleaving parallel buck converter topology is shown in Fig. 6. \( Q_1, Q_2, Q_3, \) and \( Q_4 \) are the switching devices of the four-phase parallel buck modules. \( V_{g1}, V_{g2}, V_{g3}, \) and \( V_{g4} \) are the gate voltages of the four switching devices \( Q_1, Q_2, Q_3, \) and \( Q_4 \), respectively. The phases of the driving signals of the four switching devices are shifted by 90°. The switching function of the four-phase interleaving parallel modulation method is shown in Fig. 7.

When the circuit operates, the output voltage of the circuit depends on the duty ratio of the buck module. Since the four buck module is connected in parallel, the output current is increased up to four times the single-module current amplitude. The equivalent switching frequency of the output current is four times that of the single module. The total output current of the interleaving parallel buck modules exceeds 570 A, and the equivalent frequency is 120 kHz. The circuit adjusts the output current by adjusting the output duty ratio of the buck circuit.

Assuming that the inductance of each phase and the branch devices of the converter are ideal, the charge and discharge of the inductance are linear, take \( 0 < DT \leq T/4 \) working mode for analysis. In one cycle, the working process of the converter in continuous mode can be divided into eight parts, as shown in Fig. 8.

During \( t_0 \sim t_1, T/4 \sim t_2, T/2 \sim t_3, \) and \( 3T/4 \sim t_4, \) the switch device of corresponding branches 1–4 is turned on, respectively, and the corresponding branch inductance is charged by the voltage source. The current flowing through this inductor increases. The inductance of other branches is discharged, and its current drops. The capacitor is charged. At other times, all branch switches \( Q_1, Q_2, Q_3, \) and \( Q_4 \) are closed, its branch inductances \( L_1, L_2, L_3, \) and \( L_4 \) are discharged, and freewheeling is carried out through diodes \( D_a, D_b, D_c, \) and \( D_d. \)

### B. Analysis of Inductor Current Ripple and Harmonic

According to the above analysis, the working process of the circuit is repetitive, with \( T/4 \) as a cycle. When the circuit is analyzed in the first \( T/4 \) period \( (0 < DT \leq T/4) \), it can be seen that switch \( Q_1 \) is turned on during \( t_0 \sim t_1 \), and the currents of the inductors \( L_2, L_3, \) and \( L_4 \) are all reduced. During \( t_1 \sim T/4, \) all the switches are turned OFF. All the inductor currents are reduced. Assuming that each phase is working in continuous mode, the duty cycle of all phases, the delay of the drive signal, the turn-on voltage drops of the power device, and the parasitic resistance of each phase are the same. It can be deduced that the inductor current ripple of each path is

\[
\begin{align*}
\Delta i_{L1} &= \frac{V_{in} - V_o}{L_1} DT = \frac{V_o (1 - D) DT}{L_1} T \\
\Delta i_{L2} &= \Delta i_{L3} = \Delta i_{L4} = -\frac{V_o}{L_2} DT = -\frac{V_o}{L_3} DT = -\frac{V_o}{L_4} DT
\end{align*}
\]

where \( \Delta i_{L1}, \Delta i_{L2}, \Delta i_{L3}, \) and \( \Delta i_{L4} \) represent the inductor current ripple of each phase. After linear superposition, the
the number of parallel phases. Under the conditions of open-loop ideal parameters, such as four phases, the current ripple is zero when the duty cycle is 0.25, 0.5, and 0.75. In practical closed-loop applications, the regulator automatically adjusts the duty ratio to adapt to disturbances of load or power, so it does not meet the working conditions of zero ripple. At the same time, near the point where the current ripple is zero, the current ripple amplitude corresponding to different phase numbers changes very little.

Fig. 10(b) shows the function of $K'$ and duty cycle under different phases, where $K'$ is the ratio of current ripple of different phases interleaving buck converter to a current ripple of a single buck converter. In general, the more phases, the stronger the harmonic elimination ability. For the same phase, the harmonic elimination capability varies with the duty cycle. When the duty cycle is small or large, the ripple of the output current can be significantly reduced by increasing the number of phases of the converter.

For the application background in this article, according to Table I, the current ripple needs to be less than 0.5%. That is, the current ripple needs to be less than 61.15 A at 12.23 kA. The inductance $L = 6.83 \mu$H, the input voltage $V_{in} = 48$ V, the switching frequency $f = 10$ kHz, and $V_{in}/L_f = 702$ A. So, according to (4), the total current ripple peak value of N-phase interleaved trigger buck topology is shown in Fig. 11.

Since the current ripple is required to be less than 61.15 A, the number of phases $N$ needs to be greater than 4. The design needs to leave a margin for the current ripple, and it can be seen from the figure that the reduced amplitude of the current ripple decreases with the increase of the number of phases. Considering comprehensively, 12-phase interleaving parallel is selected.

C. Fourier Analysis of Current Harmonic of Interleaving Parallel Buck Topology

The inductor current ripple waveform of a single buck converter in continuous conduction mode (CCM) is shown in Fig. 12. The time-domain representation for one period of the
The inductor current waveform is given by

\[ i(t) = \begin{cases} \frac{\Delta i}{\Delta t} \cdot t + I_{\text{out}} - \frac{\Delta i}{\Delta t}, & 0 \leq t \leq DT \smallsetminus \left(\frac{\Delta t}{(1-D)T/2}\right) \\ \frac{\Delta i}{\Delta t} \cdot (t - DT/2), & DT/2 \leq t \leq T - DT/2 \\ \frac{\Delta i}{\Delta t} \cdot (t - T), & T - DT/2 \leq t \leq T. \end{cases} \tag{5} \]

where \( I_{\text{out}} \) is the mean value of the inductor current and \( \Delta i \) is the fluctuation value of the inductor current.

To facilitate the calculation of the Fourier series, the coordinate axis in Fig. 12 is shifted to make the inductor waveform symmetric about the origin. The graph after coordinate transformation is shown in Fig. 13 [7]. The waveform amplitude is between \( -\Delta i/2 \) and \( \Delta i/2 \). The intersection of the waveform and the horizontal axis is \( 0, T/2, \) and \( T \). The time-domain representation for one period of inductor current waveform after a coordinate shift is given by

\[ i(t) = \begin{cases} \frac{\Delta i}{\Delta t} \cdot t, & 0 \leq t \leq DT/2 \\ \frac{\Delta i}{\Delta t} \cdot \left( t - DT/2 \right), & DT/2 \leq t \leq T - DT/2 \\ \frac{\Delta i}{\Delta t} \cdot \left( t - T \right), & T - DT/2 \leq t \leq T. \end{cases} \tag{6} \]

The Fourier series of the above inductor current is given as

\[ i_N(t) = \frac{a_0}{2} + \sum_{k=1}^{\infty} \left[ a_k \cdot \cos(k\omega t - \phi_k) \right] \]

\[ \cdots + b_k \cdot \sin(k\omega t - \phi_k) ] \tag{7} \]

where \( n \) refers to the nth buck circuit and \( k \) is the harmonic order. \( \phi_n \) denotes the phase shift angle of the nth buck circuit.

The form is related by

\[ \phi_n = (n - 1) \cdot \frac{2\pi}{N}. \tag{8} \]

Since the function \( i(t) \) is an odd function, the Fourier series of an odd function will not contain a cosine term, but only a sine term. So

\[ a_0 = 0 \tag{9} \]

\[ a_k = 0. \tag{10} \]

The coefficient \( b_k \) is as follows:

\[ b_k = \frac{2}{T} \int_{0}^{T} i(t) \sin(k\omega t) dt \]

\[ = -\frac{\Delta i(-1)^k}{k^2D(1-D)\pi^2} \sin[k(1-D)\pi]. \tag{11} \]

The Fourier series (7) is converted into cosine standard form as follows:

\[ i(t) = \frac{a_0}{2} + \sum_{k=1}^{\infty} A_k \cdot \cos(k\omega t - \phi_k), \tag{12} \]

When applying the substitution

\[ \frac{a_0}{2} = 0 \tag{13} \]

\[ A_k = \sqrt{a_k^2 + b_k^2} = b_k \tag{14} \]

\[ \phi_k = \tan^{-1}(b_k/a_k) = \frac{\pi}{2} \tag{15} \]

\[ \theta_{hk} = k\phi_n + \phi_k = k\phi_n \pm \frac{\pi}{2}. \tag{16} \]

We can get the following equation:

\[ i(t) = \sum_{k=1}^{\infty} b_k \cdot \cos(k\omega t - \phi_k). \tag{17} \]

To simplify the analysis, (17) can be expressed as a phasor

\[ A_k \cdot e^{-j\theta_k} = (b_k \cdot e^{-j\phi_k}) \cdot e^{-j\theta_k}. \tag{18} \]

The topology is a four-phase buck converter, \( N = 4 \). The phasor in (18) can be deduced as follows.

1) When \( k = 1 \), the phasor of the four-phase buck converter is

\[ (b_1 \cdot e^{-j\phi_1}) \cdot e^{-j\pi}, (b_1 \cdot e^{-j\phi_1}) \cdot e^{-j2\pi}, (b_1 \cdot e^{-j\phi_1}) \cdot e^{-j3\pi}, (b_1 \cdot e^{-j\phi_1}) \cdot e^{-j4\pi}. \]

2) When \( k = 2 \), the phasor of the four-phase buck converter is

\[ (b_2 \cdot e^{-j\phi_2}) \cdot e^{-j\pi}, (b_2 \cdot e^{-j\phi_2}) \cdot e^{-j2\pi}, (b_2 \cdot e^{-j\phi_2}) \cdot e^{-j3\pi}, (b_2 \cdot e^{-j\phi_2}) \cdot e^{-j4\pi}. \]

3) When \( k = 3 \), the phasor of the four-phase buck converter is

\[ (b_3 \cdot e^{-j\phi_3}) \cdot e^{-j\pi}, (b_3 \cdot e^{-j\phi_3}) \cdot e^{-j2\pi}, (b_3 \cdot e^{-j\phi_3}) \cdot e^{-j3\pi}, (b_3 \cdot e^{-j\phi_3}) \cdot e^{-j4\pi}. \]

4) When \( k = 4 \), the phasor of the four-phase buck converter is

\[ (b_4 \cdot e^{-j\phi_4}) \cdot e^{-j\pi}, (b_4 \cdot e^{-j\phi_4}) \cdot e^{-j2\pi}, (b_4 \cdot e^{-j\phi_4}) \cdot e^{-j4\pi}, (b_4 \cdot e^{-j\phi_4}) \cdot e^{-j6\pi}. \]

The relative position and amplitude of the inductor current harmonic of a four-phase buck converter are shown in Fig. 14. The first, second, and third harmonics are interleaved to cancel each other, while the fourth harmonics are superimposed on each other. Similarly, the 4Nth, (4N + 1)th, (4N + 2)th, and (4N + 3)th are staggered and offset, while the 4Nth harmonics are superimposed.

Therefore, there is only the 4Nth harmonic in the total inductor current. The fundamental harmonic of the total inductor current starts from the fourth harmonic, which reduces the amplitude of the fundamental harmonic, improves the frequency of the fundamental harmonic, and improves the EMI characteristics of the system.

Fig. 15 shows the simulation harmonic distribution of single buck topology and four-phase interleaved trigger buck
We use MATLAB (Simulink) for simulation. $L_1 = L_2 = L_3 = L_4 = 50 \mu H$, dc voltage source $= 50$ V, load resistance $= 2.3 \text{ e-3 } \Omega$, load inductance $= 4.5$ mH, and switching frequency $= 10$ kHz. It can be seen that the total harmonic distortion (THD) of the four-phase topology is greatly reduced compared to single-phase topology, and there is only the $4N$th harmonic in the total inductor current in the four-phase topology.

Fig. 16 shows that using 12 interleaved parallel buck circuits, the 1st, 2nd, 3rd, …, 11th harmonics are canceled, and the 12th harmonics are superimposed. The $12N$th, $(12N+1)$th, $(12N+2)$th, and $(12N+3)$th are staggered and offset, while the $12N$th harmonics are superimposed.

### IV. EXPERIMENTAL RESULTS

To verify the correctness of the calculation results, a test system platform is built, as shown in Fig. 17. The equipment is divided into two power cabinets and a control cabinet. Each power cabinets consist of 12 power units. It is necessary to generate precise pulse width modulation (PWM) drive signals, and TMS320F28377 (Digital Signal Processor of Texas Instruments) is adopted to produce precise PWM drive signals for all 24 power units. The switching period is $100 \mu s$, and the phase difference is $30^\circ$. The maximum output of the power supply is 12.23 kA.

The test inductor currents of different grades are shown in Fig. 18. In Fig. 18(a) and (b), 1.5- and 12.23-kA inductance
current is stable and can be run for a long time. To observe the actual current response-ability effectively, the reference voltage changes step by step and keeps approaching the maximum current setting value. In Fig. 18(c), the actual inductance current is shown. The response time is short, and the tracking process is stable and reliable.

In Fig. 18(d), the stability of the power supply is 0.24%, which meets the stability requirement of less than 0.5%.

V. CONCLUSION

This article proposed a multilevel topology based on the interleaving parallel buck converter. This interleaving parallel buck converter can achieve high current output and low harmonics. Meanwhile, this multilevel topology requires only a small number of switching devices, which can reduce control complexity and the total cost. The multiparallel topology achieves redundancy and ensures reliability. The validity was confirmed by experiments.

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