Memristor-transistor hybrid ternary content addressable memory using ternary memristive memory cell

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Abstract
A memristor-transistor hybrid ternary content addressable memory (MTCAM) with a memristor-based ternary memory cell is proposed. New emerging devices like memristors have recently been explored to overcome the limitations of CMOS-based memory circuits. The memristor is used as a binary memory cell in these MTCAM designs to replace a CMOS-based memory cell. This proposed design used a memristor as a ternary memory cell by exploiting its variable resistance characteristics. The associated wiring is reduced almost by a factor of 2 as a ternary cell is used instead of two binary cells. Area efficiency is further enhanced as the MTCAM cell is comprised of two transistors and two memristors (2T2M). A segmentation technique of match line along with a robust write/search operation method is presented to enhance the search speed of the proposed MTCAM. Simulation based on a mathematical model of memristor is presented and analysed using 65 nm TSMC MOS model parameters. Corner simulations and Monte Carlo simulations are carried out to substantiate the robustness of the design against process variation. Simulation results show the worst search delay of 0.75 ns and the energy/bit/search of 0.866 fJ for the 128 × 128 bit MTCAM.

1 | INTRODUCTION

Large data computation requires massive parallel processing with heavy memory access traffic [1,2]. Content addressable memory (CAM), a widely used hardware search engine for high-speed parallel data search applications [3], provides the capability to search data across an entire memory and returns the address in a single clock cycle [4,5]. Ternary content addressable memory (TCAM) adds more flexibility in the search operation by providing a third state called Mask (‘don’t care’) state. The ‘X’ state provides a group-search option, that is, searching a portion of the word when necessary instead of searching the whole word. This additional ‘X’ state makes TCAM more powerful in searching by returning match condition regardless of the input search data [6]. TCAM, with its high throughput, is a promising solution for systems that deal with large data, such as a high-speed search engine, data base engine, data mining and multimedia processing [7–9].

CAM density has improved significantly over the past two decades with aggressive CMOS technology scaling [10]. Aggressive scaling of CMOS technology steadily increases the power density of the chip causing a heating problem [11,12]. TCAM needs 2-bit memory to accommodate the third state, ‘X’. Multiple (12–16) transistors are thus needed to form TCAM cells, which require large area and, eventually, high power consumption [4]. This area and power constraint limits the usage of CMOS-based TCAM in network and classification applications [13,14]. New emerging devices such as magnetotunnelling junction-based devices [15], metamaterials-based optical nano circuits [16], carbon nanotube field effect transistors [17] and memristors [18,19] are being explored to find solutions for these area and power limitations of their CMOS counterpart.

Memristor, among the new devices, is suitable for TCAM because of its compatibility with CMOS, higher search speed and area efficiency [14,20]. The authors in [21] proposed a memristor-CMOS hybrid TCAM with eight transistors and...
four memristors. The design used memristors as a storage element and transistors as searching and matching elements, and the consumed energy for 1-bit mismatch was 275.7 fJ. A six-transistor and two-memristor TCAM was proposed with complex wiring which is, however, difficult to lay out [22]. A five transistor and two memristor TCAM was proposed with memristors in an anti-serial position [23]. The memristors were combined in voltage divider configuration during search operation. Another four transistor and two memristor TCAM was proposed where two separate cells were formed with two transistors and one memristor each [24]. All these proposed TCAMs used a memristor as a binary storage cell and two separate memristor bit-cells were used to replace the memory cells of CMOS-based TCAM architecture [25,26]. Reductions in required energy and area were achieved while most of these designs were using separate wiring for each binary cell and thus, complexity in layout. On the other hand, memristor-based multi-valued memory design was proposed where several resistance levels of the memristor were used to store ternary or quaternary data [27]. The multi-value characteristics of the memristor may be used to design TCAM where a single ternary-level memory cell would store all three logic levels.

The authors propose a novel two-transistor and two-memristor hybrid ternary content addressable memory cell designed with a memristor-based ternary memory cell. The memristor pair is connected in anti-serial position (connected in series but opposite in polarity) to form the ternary memory cell. The ternary memory cell would store logic-0 and logic-1, as well as local masking bit (logic-X) required for TCAM. Another contribution is a simple writing and searching technique which is operated through only two lines. A pair of lines is used to write data to the memory cell and the same pair of lines is shared during the search operation. The usage of a single memory cell and a single pair of lines reduces the wiring to a minimum, which results in efficient usage of the area of the proposed TCAM cell. Two voltage levels along with $V_{DD}$ are used: one to write data and the other to search data. The proposed searching technique also provides global masking option (don’t care search bit). A search transistor is used for discharging the match line when a mismatch occurs. The search transistor is controlled by the voltage at the memory cell output node. The memory cell appears as an orthodox voltage divider during the search operation. A reduction in the number of transistors and wiring provides an area benefit compared to previous designs.

Section 2 describes some introductory concepts on memristor as a ternary memory cell. Section 3 presents the design and operation of the proposed MTCAM. Section 4 shows the results obtained from SPICE simulations. Section 5 discusses the performance of the TCAM. Finally, the conclusion is given in Section 6.

## 2 MEMRISTOR

Memristor, the fourth fundamental circuit element [18], has attracted the attention of researchers for last decade since its practical realisation in the HP lab [19]. The nanoscale miniaturisation in an ultra-high packing density along with the inherent non-volatile storage capacity and low latency make it a popular device for memory-associated research [28–30]. Memristor is compatible with CMOS for hybrid design while it can be scaled beyond the CMOS technology [31]. There exists a relationship between the flux (time integral of voltage) and electric charge through the memristor. The resistance of the memristor is directly set by the current flow through the device. The device possesses two extreme resistance values: high-resistance state (HRS) and low-resistance state (LRS). It is possible to set other intermediate resistance values by controlling the magnitude or duration of voltage applied across the device [27]. The current flow that causes a change in resistance is a function of time and applied voltage across the device [19]. The resistance may even be unchanged if a low voltage is applied for a short time period. This phenomenon of memristor is used to read the stored data without modifying it. The variable resistance characteristics of memristor leverages encoding multiple states corresponding to different resistance values. The memristor resistance is used herein to encode three states: state-0 for logic-0, state-1 for logic-1 and state-X for logic-X. The non-volatile characteristics of memristor holds the resistance levels and hence the stored data.

Literature on memristor cited mathematical models to express its operational behaviour [32–36]. The resistance change in real memristive devices is rather related to the atomic migration induced by the applied voltage than by the current flow [35]. Models with a voltage threshold are physically better justified than those with a current one [35]. The Biolek et al. model [35] of memristive system with threshold is used herein. This model provides a realistic expression by considering the boundary conditions and the threshold type switching behaviour. According to this model, the resistance of the memristor (memristance) increases when the voltage across it, from the doped to undoped region, is higher than a certain threshold voltage, $V_{TM}$. Similarly, the resistance decreases when a voltage higher than $V_{TM}$ is applied in the reverse direction. The resistance change depends on the time duration of the applied voltage. The memristance is considered as an internal state variable, $x \equiv R$ and the device state can be defined by the following equations [35]:

\[
I = x^{-1}V_M \quad (1)
\]

\[
\frac{dx}{dt} = f(V_M)W(x, V_M) \quad (2)
\]

\[
f(V_M) = \beta(V_M - 0.5(|V_M + V_i| - |V_M - V_i|)) \quad (3)
\]

\[
W(x, V_M) = \theta(V_M)\theta(R_{OFF} - x) + \theta(-V_M)\theta(x - R_{ON}) \quad (4)
\]

The memristors in this design have $LRS$, $R_{ON} = 2 \text{ k}\Omega$, HRS, $R_{OFF} = 200 \text{ k}\Omega$, threshold voltage $V_{TM} = 1 \text{ V}$, the constant $\beta = 10^{13}$ and $\theta()$ is the step function. The authors in [37–39] customised the parameters of a memristor by adjusting the process recipe such as manipulating the thin-film growth
conditions, variation of annealing time after deposition, variation of partial pressure of oxygen gas, etc. A memristor with multilevel stable resistance states from 1 to 200 kΩ has been reported in [37].

3 | PROPOSED MTCAM WITH TERNARY STORAGE CELL

This section describes the design of the proposed MTCAM and discusses its write and search operations.

3.1 | Proposed MTCAM cell design

The proposed MTCAM cell is comprised of two memristors, m₁ and m₂, and two transistors, M₁ and M₂, as shown in Figure 1. The m₁ and m₂ memristor pair is connected in anti-serial position (connected in series but opposite in polarities) and together they form the storage cell of the proposed MTCAM. The resistance characteristics of the memristor are used to write data in the cell [19]. To write (store) the logic-1 (high) bit, m₁ would be set to maximum equivalent resistance, R₁H and m₂ would be set to minimum equivalent resistance, R₁L. To write (store) the logic-0 (low) bit, m₁ would be set to minimum equivalent resistance, R₁L and m₂ would be set to maximum equivalent resistance, R₁H while both m₁ and m₂ would be set to some intermediate equivalent resistance, Rₐ to write the logic-X (don’t care) bit. The function table of the proposed MTCAM is shown in Table 1. An access transistor, Mₐ, is connected in series with the memristor pair. Mₐ isolates the cell from other cells and thus reduces the sneak path effect [40]. The gate of Mₐ is connected to the cell enable port, E, which would control the write or search operation of the cell. The gate of the search transistor, Mₘ, is connected at the output terminal of the memory cell, which is the node between m₁ and m₂ (CO). The drain of Mₘ is connected to the match line, ML and its source is grounded. Write high (WH) and write low (WL) lines are connected at two ends of the memory cell. These two lines would be used to write ternary data in the memory cell. The same lines would be shared for search operation as search high (SH) and search low (SL), respectively.

3.2 | MTCAM masking

TCAM provides more flexibility in the search operation by allowing partial search through masking. The data word stored in the cells may include don’t care bit (local mask) and the search vector may also have don’t care bit (global mask). The proposed design offers both local masking and global masking. The masking conditions are shown in Table 2. If any of the masking condition occurs in any portion of the data word or search vector, the search transistor(s) of that portion would remain OFF and the match line would show match (charged).

3.3 | MTCAM organisation

The proposed MTCAM would store 128 words, each word having 128 ternary bit cells as shown in Figure 2. A word is formed by connecting 128 MTCAM cells side-by-side in a row. All the cells in a row are connected to the same enable line and same match line (ML). All 128 cells in a column are connected to the same write/search lines. Figure 2 shows the organisation of word lines where data pattern is stored bit by bit in Cell₀ to Cellₙ, for each word. WH and WL lines are used to write ternary data to the cell and E, as E = 1, enables the write operation through the transistor Mₑ.

WH and WL provide the required voltage drop across the anti-serial memristor pair, m₁ and m₂, and set three different states of the cell with three different resistance levels in each memristor of the pair. One set of WH and WL lines is connected to one cell of each word line of the same priority. This allows the proposed design to write one word in the memory cells in a single cycle. Each cell is connected to the match line, ML through Mₑ. Each word line has its own ML, and the match line sense amplifier (MLSA) connected at the end of each ML shows ‘match’ or ‘mismatch’. Cells of a single-word line are connected to the corresponding ML in NOR logic, as shown in Figure 3a, to ensure faster speed with longer word length [41]. The match line would be charged to VDDS when the precharge signal, CH, is low. The input vector is applied through the lines SH and SL to search the stored data. The memristor pair acts as a resistive voltage divider during search operation with enable signal, E = 1. The operation of Mₑ is controlled by the voltage at the memory cell output node, CO. The match line would remain charged (high) for matched condition, while it would be discharged (ground) through transistor Mₑ, even if only one bit of the search vector does not match (mismatch) with the corresponding stored data bit. SH and SL would share the same lines with WH and WL.

3.4 | Match line design

All the cells in a word are connected to a single ML in NOR logic. The search operation would be completed in two steps—first precharge and then evaluation. ML would be precharged with VDDS at the beginning of every search operation. The search transistor of a cell would conduct if mismatch occurs during the evaluation period and ML would be discharged through the conducting transistor.

Thus ML would remain charged if, and only if, all the bits of a search key are matched with all the bits of the stored cells in a word. As the search transistors are connected to ML in parallel, large word size would contribute a large parasitic load to ML. This results in lower speed of operation and high leakage current that leverage wrong search operation [14,42]. Our solution, presented in Figure 3(c), is to split ML into four segments to reduce this capacitance effect. Cell₀ to cell₃₁ are connected to segment-1 of ML, cell₃₂ to cell₆₃ to segment-2, cell₆₄ to cell₉₅ to segment-3 and cell₉₆ to cell₁₂₇ are thus connected to segment-4. Each segment of ML is connected to a
charging transistor, $M_{CH}$, a reset transistor, $M_{RS}$, and an inverter as shown in Figure 3(a). The output of the inverter of a segment is connected to the reset terminal of the next segment. This would allow a single mismatch in any segment to propagate to the final segment, segment-4. A sense amplifier, MLSA, is connected to segment-4, which would hold the state of ML (search result) even after the search operation is completed. MLSA consists of two back-to-back inverters and two transistors as shown in Figure 3(b). MLSA would copy ML during search period when search enable, $SE = 1$. After completion of the search operation, $SE = 0$ and MLSA would hold the data until the next search operation.

3.5 | Write operation

Three different resistance levels, corresponding to three bits —logic-1, logic-0 and logic-X, are stored in the memristor pair by controlling the direction and duration of the applied voltage across the cell. To perform the write operation, a write voltage, $V_{WRITE}$, is applied across the memristor pair which is high enough to modify the equivalent resistances of the memristors [35]. As the memristors are connected in series with opposite polarity, the non-linearity of memristance reduced significantly due to their complementary action [43]. To write logic-0 in the cell, WL is set at $V_{WRITE}$ and WH is low (ground), with the enable signal E being high (Figure 1). This would set the equivalent resistance of $m_2$ to high ($R_{H2}$) and that of $m_1$ to low ($R_{L1}$). This is also the initialisation process of the memory cell for writing. For initialisation, E of all word lines would be kept high to activate all the cells. To write logic-1 in the memory cell, WH is set at $V_{WRITE}$ and WL is low, and the equivalent resistance of $m_1$ would be high ($R_{H1}$) and that of $m_2$ below ($R_{L2}$). Writing logic-X is similar to that of logic-1, but for a shorter duration, which would set the equivalent resistances of both $m_1$ and $m_2$ to an intermediate level ($R_{M}$). The non-volatile characteristics of the memristor would hold the stored data. Writing data word by word in this process may require a little extra time, which would be offset by the fact that the write operation is a relatively more rare event than the search operation [44]. Figure 4 shows the write operation of the MTCAM and corresponding resistance levels of the memristors.

3.6 | Search operation

To perform the search operation, a search voltage, $V_{SEARCH}$, is applied across the memristor pair for a short duration. The short duration and low magnitude of $V_{SEARCH}$ would not be enough to modify the stored data. The enable signal, E, would be much higher than $V_{SEARCH}$ to ensure $M_E$ would work in the linear region having a relatively small transistor switch-on resistance. The memristor pair would act as a voltage divider and a voltage, $V_{CO}$, would appear at the cell output node, CO, in the presence of $V_{SEARCH}$. $V_{CO}$ would turn ON the transistor $M_S$ for $V_{CO} \geq V_{TH}$ where $V_{TH}$ is the threshold voltage of $M_S$. The match line, ML, would be precharged to $V_{DD}$ and $M_S$, with $V_{CO} \geq V_{TH}$, would discharge ML to ground state. This would occur in the case of mismatch. For match condition, $M_S$ would be in the cut-off region with $V_{CO} < V_{TH}$ and ML would remain charged.
To search for logic-0, SL is set at $V_{\text{SEARCH}}$ and SH is low (ground) with enable signal E being high, and the voltage appears at the cell output node CO as shown in Equation 5 where $R_{\text{TOTAL}} = R_1 + R_2$, and the values of $R_1$ and $R_2$ depend on the stored logic of the cell as listed in Table 1.

To search for logic-1, SH is set at $V_{\text{SEARCH}}$ and SL is low with enable signal E being high, and the voltage appears at the cell output node CO as shown in Equation 6 and again, as above, $R_{\text{TOTAL}} = R_1 + R_2$, with $R_1$ and $R_2$ depend on the stored logic of the cell as listed in Table 1.
write logic-1, WH was set at $V_{\text{WRITE}}$ and WL was grounded with $E = 3.3$ V so that $m_1$ would be written a state-1 ($R_{m_1}$) and $m_2$ would be written a state-0 ($R_{m_2}$). The equivalent resistance, $R_1$ of the memristor $m_1$ rose to 200 kΩ (state-1) in 22.17 ns. The equivalent resistance of the other memristor $m_2$ was down to 34 kΩ (state-0) as $m_2$ is in anti-serial position of $m_1$. This is the lowest possible resistance that would be obtained by a memristor with the chosen parameters. The authors used $R_{\text{ON}}$ ≈ 2 kΩ, but achieved 34 kΩ as the lowest resistance because of the anti-serial arrangement of the memristors. When the resistance of $m_1$ increases, most voltage is dropped in $m_1$ and the voltage across $m_2$ falls down. The modification of $m_2$ stops once the voltage across it falls below 1 V, the threshold voltage of the memristor.

$$V_{CO} = \frac{R_1}{R_{\text{TOTAL}}}(V_{\text{SEARCH}} - V_{ds,M_2})$$

$$V_{CO} = \frac{R_2}{R_{\text{TOTAL}}}(V_{\text{SEARCH}} - V_{ds,M_2} + V_{ds,M_1})$$

To write logic-0, WH was grounded and WL was set at $V_{\text{WRITE}}$ with $E = 3.3$ V so that $m_1$ would be written a state-0 and $m_2$ would be written a state-1. The equivalent resistance of the memristor $m_1$ was down to 34 kΩ (state-0) and that of $m_2$ rose to 200 kΩ (state-1) in 29.15 ns. To write logic-X, both $m_1$ and $m_2$ would be written state-X. WH was set at $V_{\text{WRITE}}$ and WL was grounded with $E = 3.3$ V, as was done to write logic-1, but for a shorter duration. The equivalent resistances of both $m_1$ and $m_2$ were found to be 44 kΩ (state-X) in 11.11 ns. All these parameter values are listed in Table 3. The simulated waveforms of writing logic-1, logic-0 and logic-X, along with initialisation (Reset) are shown in Figure 4. All three logic writings are shown in a single graph, whereas only one of those would be performed to write/store data in a cell.

4.2 Simulation of search operation

Search operation begins with the charging operation of ML. The charging transistor, $M_{\text{CH}}$, was set conducting for 0.2 ns through the signal CH, and ML was charged to $V_{DD}$ (1 V). After charging of ML, a search voltage, $V_{\text{SEARCH}} = 0.7$ V was applied across the memory part of the MTCAM cell that results in a specific voltage at the cell output node, $V_{CO}$, depending on the stored data in that memory cell. For match condition, $V_{CO}$ was found as 0.098 V and for mismatch 0.597 V. For example, if the stored data of a cell is logic-1, $m_1$ is 200 kΩ and $m_2$ is 34 kΩ. A total of 86% of the voltage would be dropped across $m_1$ and 14% across $m_2$. To search logic-1,
TABLE 3  Synthesis results of the ZT2M MTCAM

| Parameter       | Value  |
|-----------------|--------|
| RH (State-1)    | 200 kΩ |
| RL (State-0)    | 34 kΩ  |
| RM (State-X)    | 44 kΩ  |
| VCO (mismatch)  | 0.597 V|
| VCO (match)     | 0.098 V|
| VCO (X-Match)   | 0.350 V|
| Average power   | 1.154 µW|
| Energy/bit/search| 0.866 fJ|
| Cell layout area| 6.11 µm²|

we would set SH at 0.7 V with grounded SL. Corresponding V CO would be 0.098 V, which is below the threshold voltage of MS. As the gate of MS is connected at V CO, MS would remain in the cut-off region and ML remains charged, which results in a match condition. On the contrary, if we search logic-0, we should set SL at 0.7 V with grounded SH. Corresponding V CO would be 0.597 V, which is above the threshold voltage of MS. This time MS would be conducting and ML would be discharged through MS that results in mismatch condition. These parameter values are listed in Table 3. The threshold voltage of MS was set at 0.51 V by appropriate selection of W/L ratio.

The match condition and a 4-bit mismatch condition of match line are shown in Figure 5.

For local mask condition, both m₁ and m₂ were set at 44 kΩ each. V SEARCH was applied across the memory cell to search logic-1 or logic-0 and V CO was found to be 0.35 V in both cases. MS remained at the cut-off region with this 0.35 V and ML remained charged, which resulted in a match condition. For a global mask condition, both SH and SL were assigned with 0 V, which resulted in 0 V at the V CO regardless of the resistance values of m₁ and m₂. This kept MS in the cut-off region, ML remained charged, which resulted again in match condition.

5 | PERFORMANCE AND ANALYSIS

The simulation results of the 128x128 MTCAM array show 22.17 ns is required to write logic-1 and 29.15 ns to write logic-0. In the proposed design the authors used 24.6 ns to write logic-1 and 32.4 ns to write logic-0. These writing times satisfy 10% variation limits. The memristors reach their maximum and minimum resistance values corresponding to the logic levels in 22.17 and 29.15 ns, respectively. The resistance values do not change after that time period even if the writing voltages continue. On the other hand, with 24.6 and 32.4 ns writing times, the memristors would still reach their target resistance values with a 10% shorter writing time period. This ensures the expected voltage levels at the cell output node. A time of 11.11 ns is required to write logic-X and both memristors are set at 44 kΩ resistance. However, 10% variation in writing time changes the resistance values, low at 38 kΩ to high at 52 kΩ. The corresponding voltage level varies from 0.3 to 0.4 V at the cell output node, instead of 0.35 V, during the search operation. The worst case happens at 0.4 V, which is still below 0.51 V, threshold voltage of the search transistor, MS. It was found that MS still remains at the cut-off region during the search operation, even with a 25% variation in write time of logic-X state. The worst case V CO for logic-X state was found at 0.469 and 0.472 V during the search operation with 25% more and 25% less write time, respectively.

Corner simulations were carried out in Fast and Slow corners in order to verify the robustness of the design against process variation. The Fast corner simulation results in lower search delay and lower search energy, while the Slow corner simulation results in a higher search delay and higher search energy. The search energy for the Fast corner was lower as a result of a lower search time. Table 4 shows the variations of corner simulations. The write times for logic-1 and logic-X did not change for either corner, as the ME is connected in series with very high resistance. The write time for logic-0 was 28.46 ns for the Fast corner and 29.78 ns for the Slow corner, both are inside the design time of 32.4 ns. The V CO for different logic states were the same as those found in simulations of the typical model.
The impacts of deviation of memristor resistances, $R_{H}$ and $R_{L}$, and the cell output voltage, $V_{CO}$, on the search result were further verified by Monte Carlo simulations. All parameters of memristor and transistor threshold voltage, $V_{TH}$, were varied 10% for the simulations. Figure 6 shows that the maximum value of $R_L$ was 36 kΩ and the minimum was 31 kΩ, while the maximum value of $R_H$ was 220 kΩ and the minimum was 180 kΩ. The effect of this resistance variation on $V_{CO}$ for 1-bit mismatch is presented in Figure 7, which shows the maximum $V_{CO}$ was 0.612 V and the minimum was 0.582 V for a mismatch condition, while the designed value was 0.597 V. The lowest value of $V_{CO}$ was found to be 0.582 V, well above $V_{TH}$, which would turn on $M_s$. The maximum $V_{CO}$ was 0.114 V and the minimum was 0.087 V for a match condition.

The ML voltage remains near $V_{DD}$ if a match condition occurs during the search operation. The search time was determined as the time difference between 50% rise time of the precharge signal, CH and 50% fall time of the ML voltage during mismatch. The time required to evaluate mismatch depends on the total number of mismatches. For a single bit mismatch in a 128-bit row, the worst case scenario, the search time was 0.75 ns. The time to detect mismatch falls sharply with an increase in the number of mismatch bits, and the search time was down to 0.579 ns with only a 2-bit mismatch. The search time was recorded when mismatch occurs in the first segment of ML. The simulation result shows a 0.08 ns delay added in each segment of ML, so the delay would be 0.24 ns less if the mismatches occur in the last segment of ML. The search delay due to a different number of mismatches is shown in Figure 8. Another study on search delay is presented in Figure 9, which shows the variation of search time with word length of the proposed MTCAM. The variation of search time using Monte Carlo simulations is presented in Figure 10, which shows that the maximum search time was 0.808 ns and the minimum was 0.724 ns, while the designed search time was 0.75 ns.

The search time was further analysed for parasitic RC components using the Cadence Quansys QRC extraction tool. Figure 11 shows the layout of one TCAM cell. The effect of the parasitic RC components on search time for 50% fall was calculated as

$$t_{PR} = 0.69R_{PR}C_{PR}$$

where $t_{PR}$ is the delay caused by the parasitics when the ML falls to 50% of the precharge voltage, $R_{PR}$ is the parasitic resistance and $C_{PR}$ is the parasitic capacitance. $t_{PR}$ was calculated as 22.56 fs for the presented design.

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**TABLE 4** Comparison of corner simulations

| Parameter                     | Typical | Fast  | Slow  |
|-------------------------------|---------|-------|-------|
| Search delay (ns)             | 0.75    | 0.51  | 0.99  |
| Energy ($\mu$J/bit/search)    | 0.866   | 0.763 | 0.959 |
transistor during the Slow simulation results in a higher energy dissipation. A summary of the corner simulations is presented in Table 4.

The specifications of the proposed MTCAM are summarised and compared with some other published designs in Table 5. With only two transistors, the authors proposed MTCAM with a minimum number of devices. The use of a ternary memory cell, unlike other published TCAM, makes the design more area-efficient as a lower number of devices and wirings would be required. The device is also faster compared to other TCAMs as only one transistor per cell is connected to the match line. The segmentation of the match line further reduces the search delay. Search energy is also comparable with published memristor-based designs.

6 | CONCLUSION

A novel hybrid memristor-CMOS TCAM with ternary memory cell has been presented. All three possible data bits are stored in the single ternary memory cell, which reduces the associated wiring approximately by a factor of 2. A further reduction in area is achieved as the MTCAM cell consists of only two transistors and two memristors. A robust write/search operation technique has been presented. Appropriate match line segmentation has been added to improve the search time. The robustness of the design was verified with Fast and Slow corner simulations. Parasitic RC components were analysed using Cadence Virtuoso Layout-XL and Quantus QRC extraction tools. Simulation results illustrate the fast search speed and low power consumption of the design. Variations of different parameters were patterned by Monte Carlo simulation. The
128-bit MTCAM may further be extended for larger word lengths with an additional 80 ps delay contributed by every 32-bit segment.

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