Approximate analytical channel potential model of poly-Si thin film transistors operated in the strong inversion region under the high gate and low drain biases

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Abstract. An approximate analytical channel potential model of polycrystalline silicon thin film transistors operated in the strong inversion region under the high gate and low drain biases is proposed. Thus, the linear relationship between the channel potential and the drain voltage is derived in the strong inversion region under the above bias condition when the polysilicon layer is ultrathin. This model agrees with the two-dimensional-device simulation results under different gate voltages, different drain voltages and different channel lengths. By comparing the relative errors between the model and the simulation results, it presents that this model is more suitable under the higher gate voltage $V_g$ or the lower drain voltage $V_d$, regardless of the channel length. And this approximate analytical model is helpful in solving the two-dimensional-device problem by one-dimensional Poisson’s equation since the drain bias is taken into account in the channel potential.

1. Introduction
In recent years, polycrystalline silicon thin film transistors (poly-Si TFTs) have been the essential electronic devices in flat panel displays (FPDs) [1]. For their applications, an indispensable circuit simulation is a key issue for their large scale circuitry. As a result, an accurate and efficient compact model of the poly-Si TFTs is required in the simulation. The surface-potential-based model structure is a choice for the new generation compact MOSFET models and the approach is recognized as both the most physical and the most difficult to implement. In the surface-potential-based models, the key issue is the calculation of the surface potential.

In order to calculate the surface potential, if we start from the basic Poisson’s equation, the carrier density is needed. In order to well characterize it, the distribution of the channel potential, which is defined as bulk-referenced quasi-Fermi potential, is required. However, there are few discussions about the model of the channel potential. Or just a given value is assigned to the channel potential without discussing its dependence on the applied biases and the device structure parameters [2-4]. And if the channel potential is arbitrarily given, the relevant model is essentially a one-dimensional analysis.
In this paper, an approximate analytical channel potential model of poly-Si TFTs with the ultrathin polysilicon layer in the strong inversion region under the high gate and low drain biases is presented and is verified by the two-dimensional-device simulator MEDICI under various gate voltages, drain voltages and channel lengths. It is helpful in solving the two-dimensional-device problem by one-dimensional Poisson’s equation since the drain bias is taken into account in the channel potential.

2. Model formulation

In the vicinity of the surface, for n-type poly-Si TFTs, the channel potential \( V_c(y) \) is defined as \( V_c(y) \equiv \varphi_n(y) - \phi \), where \( y \) is an arbitrary point along the channel, \( \varphi_n(y) \) is the electron quasi-Fermi potential at the arbitrary position along the channel in the vicinity of the surface and \( \phi \) is the Fermi potential at the bulk [5].

According to the previous work [6], for n-type poly-Si TFTs with the ultrathin polysilicon layer, the drain current can be expressed as:

\[
I_d(y) = \frac{W \mu_s}{\sqrt{2}} \int_{0}^{qN_{as}/L_g \cdot t_{channel}} \left[ qN_{as}/L_g \cdot t_{channel} \cdot \frac{L_g}{1+g_s \cdot \exp\left(\frac{E_s}{q} / q+\phi - \Psi_s\right)} - C_{ox}(V_g - V_f - \Psi_s)\right] dV_c
\]

where \( I_d \) is the drain current, \( W \) is the channel width, \( \mu_s \) is the surface mobility, \( q \) is the electron charge, \( N_{as} \) is the active acceptor concentration, \( t_{channel} \) is assumed as \( \frac{1}{e} \cdot \sqrt{\frac{2\Psi_s e_s}{qN_{as}}} \), \( \Psi_s \) is the surface potential, \( e_s \) is the silicon permittivity, \( N_f \) is the acceptor type grain-boundary surface state (areal) density, \( L_g \) is the grain size, \( E_s \) is the energy level difference between the trap level and the intrinsic level, \( \phi_f \) is the thermal voltage, \( C_{ox} \) is the unit gate oxide capacitance, \( V_g \) is the gate voltage, \( V_f \) is the flat band voltage.

Meanwhile, in the strong inversion region, the first-order approximation of the surface potential is \( \Psi_s \approx 2\phi_f + V_c \), where \( V_c \) is equal to 0 V and the drain bias \( V_d \) at the source and drain electrode, respectively [7].

So when in the strong inversion region under the high gate and low drain biases, in the integrand of (1), all terms related to \( \Psi_s \) become neglectable compared with that with \( V_g \). So the integrand of (1) can be determined by the term with \( V_g \). And it is almost constant depending on \( V_g \). Therefore, (1) can be approximately rewritten as

\[
I_d(y) = -\frac{W \mu_s}{y} [C_{ox}(V_g - V_f)]V_c(y)
\]

At \( y=L \),

\[
I_d(L) = -\frac{W \mu_s}{L} [C_{ox}(V_g - V_f)]V_d
\]

With (2) and (3), the approximate analytical channel potential model

\[
V_c(y) = \frac{V_d}{L} V_d
\]

is derived.

3. Result and discussion

The approximate analytical channel potential model of poly-Si TFTs in the strong inversion region under the high gate and low drain biases has been compared with the two-dimensional-device
simulator MEDICI via different gate voltage $V_g$, drain voltage $V_d$ and channel length $L$. And in the simulator, the model [8, p 3-111, 3-113] SRH (Shockley-Read-Hall recombination with fixed lifetime), ARORA (a concentration and temperature mobility model based on the work of Arora et al.) and SRFMOB (an effective mobility is calculated at semiconductor-insulator surfaces using an effective electric field) are involved. According to the MEDICI User Guide, if there is an Ohmic contact, the minority and majority carrier quasi-Fermi potentials are equal and are set to the applied bias of that electrode [8, p 2-73]. Since the source side is biased at 0 V, the quasi-Fermi potential at the source electrode, which equals to the bulk Fermi potential, is equal to 0 V. Therefore, the electron quasi-Fermi potential in the MEDICI is the same as the channel potential in this paper.

In figure 1, the correlation of the channel potential with the relative position ($y/L$) in the channel is shown under the various gate voltage $V_g = 15$ V, 20 V and 30 V while the drain voltage $V_d = 1$ V and the channel length $L = 10 \ \mu m$. And the model presents the well agreement with the simulation results. Moreover, since the term with the gate voltage plays a more important role in (1) under the higher gate bias, the model agrees with the simulation better.

In figure 2, the correlation of the channel potential with the relative position in the channel is shown under the different $V_d = 0.1$ V, 0.5 V and 1 V while $V_g = 15$ V and $L = 10 \ \mu m$. The model presents the well agreement with the simulation results. Furthermore, the smaller drain bias is, the more excellent agreement it achieves since the term related to $\Psi_f$ in (1) turns to be less.

In figure 3, the correlation of the channel potential with the relative position in the channel is shown under the various $L = 5 \ \mu m$, 10 $\mu m$ and 25 $\mu m$ while $V_g = 30$ V, $V_d = 1$ V. The model presents the well agreement with the simulation results and is less affected by the different channel lengths.

In order to have an explicit insight on the differences between the model and the simulation results, the relative errors are compared under the different $V_g$, $V_d$ and $L$ in figure 4. In figure 4 (a), the relative error decreases to 2% under the higher gate voltage $V_g = 30$ V. The relative error is within about 2% under the lower drain voltage $V_d = 0.1$ V shown in figure 4 (b). And no obvious differences can be found in various channel lengths in figure 4 (c). It can be concluded that under the higher $V_g$ and lower $V_d$, this approximate analytical model (4) can better depict the channel potential along the channel, regardless of the channel length.

4. Conclusion

The approximate analytical channel potential model of poly-Si TFTs with the ultrathin polysilicon layer in the strong inversion region under the high gate and low drain biases is obtained. The channel potential shows a linear dependence on the drain bias with the ratio factor $y/L$. Compared with the two-dimensional-device simulation results, this model is proved under different gate voltages, drain voltages and channel lengths. And the relative error decreases to about 2% under the higher gate voltage and the lower drain voltage respectively and is less affected by the different channel lengths. It presents that this model is more suitable under the higher $V_g$ and lower $V_d$, regardless of the channel length. And this approximate analytical model is helpful in solving the two-dimensional-device problem by one-dimensional Poisson’s equation since the drain bias is taken into account in the channel potential.

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Figure 1. The correlation of the channel potential with the relative position ($y/L$) in the channel under the different gate voltages.

Figure 2. The correlation of the channel potential with the relative position ($y/L$) in the channel under the different drain biases.

Figure 3. The correlation of the channel potential with the relative position ($y/L$) in the channel under the various channel lengths.

Figure 4. Relative errors between the model and the simulation are compared under the various gate, drain voltages and channel lengths.