Characterization and modeling of on-chip via stacks for RF-CMOS applications

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Abstract This work proposes an experiment-based characterization and modeling approach for interconnection channels including via stacks as vertical transitions. A daisy chain structure implemented in a 0.18 \( \mu \text{m} \) RF-CMOS process is used for developing and verifying the validity of the proposal. The usefulness of the models is shown by assessing the impact of the vias in a practical resonant rotary traveling wave oscillator (RTWO). The oscillation frequency of the RTWO is reduced 13.7 \% when the via stack models are included.

key words: on-chip vias, RTWO, CMOS RF process, S-parameters extraction.

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

In the design of integrated circuits (ICs) for RF applications, vias are generally still considered as RC elements $[1, 2, 3, 4]$. However, as the operation frequency of ICs increases, the inductive behavior of on-silicon vias (OSV) and vertical interconnections must be considered as in the case of PCB, RDL, and TSV technologies $[5, 6, 7, 8, 9, 10]$. The previously performed analyses reported in $[11, 12]$ included the characterization of the electromagnetic behavior of via arrays and stacks; in this case, however, the results were obtained only through full-wave simulations. It is interesting to point out the fact that these simulation results indicate that increasing the area of the via array, and consequently the number of vias within the array, not necessarily reduce the associated parasites due to that inductive behaviors become more relevant than the resistive losses when the interconnections are operating at high frequencies. Actually, electromagnetic simulations allow to observe that this is originated by the fact that the current within the array is not uniformly distributed due to proximity and current crowding effects; hence, the current tends to confine in the outer vias of the array as frequency increases. In consequence, this served as motivation to carry out the corresponding experimental confirmation and the proposal of an electrical model that allows for the representation of via arrays in SPICE-like programs while accounting for these high-order effects. According to the above, in this work, a daisy chain structure with two different via stacks in a 0.18 \( \mu \text{m} \) technology was manufactured, simulated, and modeled $[13, 14, 15]$. The circuit model presents a maximum average error of 5.1 \% for the return loss (i.e., $|S_{11}|$) when compared with experimental data. Furthermore, with the purpose of measuring the impact of these inter-metalic elements in the performance of RF applications $[16, 17, 18, 19, 20, 21]$, the via stack circuit model is applied here for representing a RTWO. The importance of this particular application example relies on the fact that this type of oscillators allow fulfilling the design requirements for high frequencies applications (i.e. within the gigahertz range) $[22, 23, 24, 25, 26]$. Thus, the considered resonant RTWO is composed by two differential transmission lines with a given characteristic impedance but including geometric discontinuities like via stacks that cause variations in the overall electrical performance. Results in the time domain are included here to visualize the significant signal delay introduced by the via stacks.

2. Description of prototype

Fig. 1.a) shows a perspective of the daisy chain structure under investigation, whereas a photograph of the structure is presented in Fig. 1.b). The selection of this inter-chip communication channel is because of its wide use in ICs implemented in RF-CMOS processes $[27, 28]$. The structure consists of two vertical via stacks with different connection areas and asymmetric structure, which allows for representing a realistic scenario where a signal is guided along a microstrip line, taken down to a stripline level, and finally brought back to a microstrip line by employing via stacks. Notice in these figures that the via stacks are located between metal 6 (i.e., the top metal) and metal 3, which are commonly used in RFIC for the transmission of high frequency signals between local and global networks $[29]$. In this regard, details of the via arrays used to form the vertical transition between metal layers are illustrated in
Fig. 1.c). The short via stack includes $5 \times 34$ vias per metal level and a connection area of $3.2 \times 20 \, \mu m^2$, whereas the long via stack includes $34 \times 34$ vias per level of metal. For the latter, the connection area is $20 \times 20 \, \mu m^2$. Through the systematic simulation of several structures, it was found that reducing the length of the stack below a certain limit considerably increases the effect of the associated parasitic resistance, which will eventually yield the unpractical application of the transition in an actual interconnection channel. For this reason, it was determined that the stack with a length of 3.2 um can be considered close to the bottom limit for the used technology. It is also important to mention that within the frequency range considered in this work, a 3.2-um length via array still exhibits the frequency-dependent current distribution effect explored here. In addition, during the design of the final prototype, it was necessary taking into consideration the available area within the test-chip, the probe pitch used to collect the electrical measurements, and all the design rules established for the technology.

3. Modeling methodology

Firstly, the daisy chain interconnection was represented by means of a 3D model simulated using a full-wave solver while considering the material specifications given by the manufacturer. Aluminum is the metal used to form the interconnects in the technology where the final prototype is implemented, while silicon dioxide is used as field oxide; therefore, the conductivity and permittivity provided by the manufacturer for these materials were used. It is necessary to point out, however, that since the nominal permittivity of the dielectric layers is reported to slightly vary at the different process levels [13, 32], these variations were considered during the simulations. Afterwards, each part of the structure, including the via stacks, was modeled using a T circuit for the corresponding electrical representation. In addition, the probing pads are modeled by means of a capacitance of 34.4 fF based on the data given by the manufacturer and a calculated AC resistance of 0.12 Ω. The electrical values for the circuit representation of the microstrip lines and the stripline were extracted from the full-wave simulations results obtained using the Keysight’s EMpro electromagnetic simulation software [30]. Afterwards, circuit model parameters were obtained through an optimization applying the ADS circuit simulator [31]. Furthermore, with the measured structure, an asymmetrical and two symmetrical daisy chains were simulated, one for each type of stacks. These structures were simulated with the objective to obtain and improve the accuracy of the circuit models for via stacks. Using the circuit model for the pads, the microstrip lines, and the stripline, the via stacks circuit models were de-embedding from the full wave simulated data and from the measurements. The final model of the measured daisy chain and its electrical values are show in the Fig. 2. It is important to remark the fact that, as expected, the model parameters present a dependence on frequency and exhibit lower LC values for the short via stack in comparison with the long via stack.

4. Results

The $S$-parameters obtained from the equivalent circuit model and from full-wave simulations were compared with experimental results. The average maximum error for the $S$-parameters between the circuit model and the data measured in the magnitude is 5.06 % and for the phase is 1.89 % (Fig 3). For the case of the full-wave simulations, the pads are considered by including their electrical circuit
models. The full wave simulation shows differences in the $S_{21}$ parameter in comparison with the extracted from the experimental data due to the effect of the dummy structures used in the manufacture process. In Fig. 3, the difference between the simulated and measured the return loss curves, as well as in the magnitude of the insertion loss curves has a low value (below 7.5%), which indicates that the coupling effect and the overall loss of the structures is predicted with accuracy. On the other hand, for the phase of the insertion loss, the error at the highest frequency is 11.2%. This error indicates that the simulated phase constant, given by the imaginary part of the propagation constant, varies from the actual phase constant exhibited by the structure. This variation is due to the difficulty of accurately representing the effective permittivity of a practical structure where the dielectric properties of the layers at different layers is not exactly the same. Besides, metal dummies are used to maintain uniformity and planarity among the different interconnection layers, which also impact the effective permittivity experienced by a signal guided through the interconnect. Bear in mind also, that including the exact pattern of these structures in the simulated structure is not possible and thus an effective representation of it was used. The dummy structures consist of metal squares (aluminum) with an area of $3 \times 3 \ \mu m^2$ distributed across the dielectric in the different metal layer whose function is assured the material density to avoid error in the chemical-mechanic polish processes [32]. In this regard, even though the dummy structures were included in the EM simulation, it is difficult to duplicate the exact pattern used for the distribution and shape of these dummies due to the complexity introduced, among other effects, by the process variations. On the other hand, as part of the circuit model, an inductance $L_{coupling} = 0.35 nH$ was added to model the parasitic path between the input and output microstrip lines forming the structure. Moreover, there exists a lossy capacitive ground connection between the microstrip and the via stacks represented by the capacitances $C_{loss1}$, $C_{loss2}$ and the resistors $R_{loss1}$, $R_{loss2}$, which model the effect of the metal dummies in the daisy chain. The model also includes a coupling capacitance between the two microstrips with a value of 2.75 pF.

As an additional validation of the proposal, the via stack models were used for simulating the output signal for a RTWO with a reference operation frequency of 20.2 GHz and dimensions of $410 \times 410 \ \mu m^2$, $W = 20 \ \mu m$ and $S = 20 \ \mu m$. There are 8 compensator stages and the via stacks are located between the resonator and compensators (Fig. 4). The reference RTWO is designed using a standard methodology considering the via connections as ideal [33] and the Fig. 5 shows the results of the electrical simulation for output signal when the proposed via stack models are used. Consider that the target oscillation frequency at the output of an RTWO is 20 GHz; thus, when designing the circuit using a model that neglects the effect of the vias, the corresponding result in Fig. 5 shows a frequency of oscillation very close to the desired value. Nevertheless, when including the effect of the vias, an error higher than 12.5% is obtained; which points out the requirement of considering the parasites introduced by these transitions. As can be seen from the figure, using the short via stack model there is reduction of 2.7 GHz (13.3%) in comparison with the reference output signal and with long via stack model the reduction increases to 2.8 GHz (13.8%).

Fig. 3. $S$ parameters obtained from measurements, applying full wave simulations, and the proposed circuit model.

Fig. 4. Schematic view for the connection between the resonator and compensator in the RTWO using the short via stack.

Fig. 6 shows the frequency spectrum for RTWO output signals where it can be seen that by including the circuit models of the analyzed stacks in the design, the harmonics also are influenced which it causes distortion in the RTWO output signal. This result shows that using via stacks with a small connection area introduces a less severe impact for the transmission in RF applications due the presence of the proximity effect which affect the behavior of the RLC elements in the via stack by depending of the frequency of the transmitted signal. The proximity effect can be explained as the interaction of the magnetic field between closer conductors. This interaction reduces the current density in the conductor due to the flux cancellation and it can be seen as an increase of the impedance. The proximity effect is more notorious with the increase of the frequency and the number of closer conductors [11].
5. Conclusion

In the presented work, via stacks were modeled using experimental and simulated data. An asymmetrical daisy chain structure in a 0.18 \( \mu \)m RF technology was used to obtain the measured data and the simulated data corresponds to full wave representations from different parts of the structure. The methodology applied shows that using full wave representations for de-embedding makes possible to characterize a structure with vertical asymmetric interconnections with a good exactitude, introducing an error below 5.06 \% in average. The effect of these interconnections in a RTWO as a RF application, shows that the via stacks introduce a filtering effect in this type of oscillators, reducing its operation frequency up to 13 \%. Finally, the filtering effect observed in the RTWO would be present in many RF applications decreasing the signal integrity for transmission between global and local interconnections. This effect will increase with the technological scaling due to a greater number of metal layers in more advanced CMOS processes. Also the via effect will have greater influence for higher frequencies and longer via stacks due the present of the proximity effect that increases the LC parasites in these type of interconnections.

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References

[1] I. Ciofi, et al.: “Modeling of Via Resistance for Advanced Technology Nodes,” IEEE Trans. Electron Devices 64 (2017) 2306 (DOI: 10.1109/TED.2017.2687524)
[2] H. Lee, J. K. Park and J. T. Kim: “A unified system level error model of crosstalk and electromigration for on-chip interconnect,” IEICE Electron. Express 14(2017) 20161194 (DOI: 10.1587/elex.14.20161194)
[3] J. Jiang, et al.: “Design optimization for capacitive-resistively driven on-chip global interconnect,” IEICE Electron. Express 12 (2015) 20150111 (DOI: 10.1587/elex.12.20150111)
[4] X. Ma, et al.: “A novel delay optimization method for a critical path in VLSI design,” IEICE Electron. Express 10 (2013) 20130446 (DOI: 10.1587/elex.10.20130446)
[5] J. Xu, et al.: “A Survey on Modeling Strategies for High-speed Differential Via between Two Parallel Plates,” IEEE EMCSI (Aug2017) 527 (DOI: 10.1109/ISEMC.2017.8077926)
[6] R. Cecchetti, et al.: “Analytical evaluation of scattering parameters for equivalent circuit of through silicon via array,” Electron. Lett. 51 (2015) 1025 (DOI: 10.1049/el.2015.1265)
[7] F. Wang, J. Huang and N. Yu: “A novel guard method of through-silicon-via (TSV),” IEICE Electron. Express 15 (2018) 20180421 (DOI: 10.1587/elex.15.20180421)
[8] F. Wang, G. Wang and N. Yu: “Equivalent circuit model of through-silicon-via in slow wave mode,” IEICE Electron. Express 14 (2017) 20171025 (DOI: 10.1587/elex.14.20171025)
[9] D. H. Jung, et al.: “Through silicon via (TSV) defect modeling, measurement, and analysis,” IEEE Trans. Compon. Packag. Manuf. Technol. 7 (2017) 138 (DOI: 10.1109/TCAPT.2016.2631731).
[10] F. Wang, J. Huang and N. Yu: “A high-pass filter based on through-silicon via (TSV),” IEICE Electron. Express 16 (2019) 20190098 (DOI: 10.1587/elex.16.20190098)
[11] C. Sanabria and M. Linares-Aranda: “An analysis of On-Silicon-Vias Stack in RF-CMOS Processes,” IEEE Lat. Amer. Symp. Circuits and Systems (Feb 2018) 1 (DOI: 10.1109/LASCAS.2018.8399970)
[12] C. Sanabria, R. M. G. Higuera and M. Linares-Aranda: “A simple Model of Inter-Metallic Connections (vias) in CMOS Resonant Rotary Traveling Wave Oscillator (RTWO),” Int. Conf. on Electrical Engineering, Computing Science and Automatic Control (Oct 2017) 1 (DOI: 10.1109/ICEEE.2017.8108860)
[13] United Microelectronics Corporation: “0.18 um Mixed-Mode and RFCMOS 1P6M Metal Metal Capacitor Process Interconnect Capacitance Model,” Ver.1.3P3, 2009
[14] L. Zhang, Z. Li and K. Chakrabarty: “Built-In Self-Diagnosis and Fault-Tolerant Daisy-Chain Design in MEDA Biochips,” IEEE International Test Conference (ITC) (Nov 2018) 1 (DOI: 10.1109/TEST.2018.8624847)

[15] K. Nitsu, et al.: “Daisy chain transmitter for power reduction in inductive-coupling CMOS link,” IEICE Trans. Electron E90-C (2007) 829 (DOI: 10.1093/ietele/e90-c.c.829).

[16] S. Ogawa, et al.: “Millimeter-wave transmission line with through-silicon via for RF-MEMS devices,” IEICE Electron. Express 10 (2013) 20130565 (DOI: 10.1587/elex.10.20130565)

[17] S. Kousai: “Recent progress in CMOS RF circuit design,” IEICE Electron. Express 11 (2014) 20132011 (DOI: 10.1587/elex.11.20132011)

[18] K. Takahashi, et al.: “Evolution of Millimeter-Wave Multi-Antenna Systems in the IoT Era,” IEICE Trans. Electron 10 (2017) 809 (DOI: 10.1587/transele.E100.C.809)

[19] J. Bae, et al.: “An oscillator-based sensor using a capacitive metal mesh for sensitive detection of dielectric materials in the terahertz region,” IEICE Electron. Express 15 (2018) 20180669 (DOI: 10.1587/elex.15.20180669)

[20] F. A. Khaleel and M. N. Abbas: “Ultra low power and highly linearized LNA for V-band RF applications in 180 nm CMOS technology,” IEICE Electron. Express 14 (2017) 20170066 (DOI: 10.1587/elex.14.20170066)

[21] M. Ataei, et al.: “Transformer feedback millimeter-wave VCO with capacitance cancellation technique in 0.18-µm CMOS,” IEICE Electron. Express 8 (2011) 780 (DOI: https://doi.org/10.1587/elex.8.780)

[22] M. Sawaby, et al.: “Design and Optimization of a 94GHz Rotary Traveling Wave Oscillator for mm-Wave Applications,” IEEE Int. Symp. Circuits and Systems (May 2015) 2844 (DOI: 10.1109/ISCAS.2015.7169279)

[23] Z. Bai, et al.: “A 2-GHz Pulse Injection-Locked Rotary Traveling-Wave Oscillator,” IEEE Trans. Microwave Theory and Techniques 64 (2016) 1854 (DOI: 10.1109/TMTT.2016.254475).

[24] R. Kuttappa, et al.: “Stability of Rotary Traveling Wave Oscillators under Process Variations and NBTI,” IEEE Int. Symp. Circuits and Systems (Sept 2017) 1 (DOI: 10.1109/ISCAS.2017.8050435).

[25] N. Nouri and J. F. Buckwalter: “A 45-GHz Rotary-Wave Voltage-Controlled Oscillator,” IEEE Trans. Microwave Theory and Techniques 59 (2011) 383 (DOI: 10.1109/TMTT.2010.2097712).

[26] J. Chien and L. Lu: “A 32-GHz Rotary Traveling-Wave Voltage Controlled Oscillator in 0.18-µm CMOS,” IEEE Trans. Microwave and Wireless Lett. 17 (2007) 724 (DOI: 10.1109/LMWC.2007.905634).

[27] Y. Tsubouchi, et al.: “A 12.8-GHz Daisy Chain-Based Downlink/F Employing Spectrally Compressed Multi-Band Multiplexing for High-Bandwidth, Large-Capacity Storage Systems,” IEEE Journal of Solid-State Circuits 54 (2019) 1086 (DOI: 10.1109/JSSC.2018.2889704)

[28] Chong-Jin Ong, B. P. Silva and H. Chen: “Procedure for length matching of daisy-chained clock and command/address/control signal traces including via length compensation,” IEEE Electromagnetic Compatibility Magazine 8 (2019) 54 (DOI: 10.1109/MEMC.2019.8753443)

[29] R. O. Nunes and R. L. de Orio: “Effect of Lines and Vias Density on the BEOL Temperature Distribution,” Symposium on Microelectronics Technology and Devices (Aug 2018) 1 (DOI: 10.1109/SBMicro.2018.8511319).

[30] EMpro software. (2019) https://www.keysight.com/en/pc-1297143/empro-3d-em-simulation-software

[31] ADS software. (2019) https://www.keysight.com/en/pc-1297113/advanced-design-system-ads

[32] United Microelectronics Corporation: “0.18 µm Mixed-Mode and RFCMOS 1.8V/3.3V 1P6M Metal Metal Capacitor Process Topological Layout Rule,” Ver.2.10 p.1, 2009

[33] L. Wu, et al.: “Design of 110-152 GHz Rotary Traveling Wave Oscillators in 65 nm CMOS Technology,” IEEE SOUTHEASTCON (March 2014) 1 (DOI: 10.1109/SECON.2014.6950662)