Threshold voltage instability and polyimide charging effects of LTPS TFTs for flexible displays

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In this paper, we investigate the $V_{th}$ shift of p-type LTPS TFTs fabricated on a polyimide (PI) and glass substrate considering charging phenomena. The $V_{th}$ of the LTPS TFTs with a PI substrate positively shift after a bias temperature stress test. However, the $V_{th}$ with a glass substrate rarely changed even with increasing stress. Such a positive $V_{th}$ shift results from the negative charging of fluorine stemmed from the PI under the gate bias. In fact, the C–V characterization on the metal–insulator-metal capacitor reveals that charging at the SiO$_2$/PI interface depends on the applied gate bias and the PI material, which agrees well with the TCAD simulation and SIMS analyses. As a result, the charging at the SiO$_2$/PI interface contributes to the $V_{th}$ shift of the LTPS TFTs leading to image sticking.

Recently, flexible displays have attracted considerable attention as next-generation drivers in display industries. Because low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFT) have the advantages of low temperature process integration and high mobility, they have rapidly become popular in flexible displays and applications. However, the usage of excimer laser annealing (ELA) for the crystallization of amorphous silicon (a-Si) and chemical vapor deposition (CVD) for the process of gate insulation produce hysteresis loops in the device characterization, due mainly to the material and physical constraints of defects and non-uniformity.

In turn, such intrinsic limitations impact fluctuations of electric current that flows into the organic light emitting diodes (OLED), leading to TFT instability and display performance disturbance, including halo and image sticking. In addition, moisture and oxygen penetration are serious deficiencies of all plastic substrates available for OLED flexible display applications. In particular, OLED's lifetime decreases when exposed to oxygen and moisture. When fabricating a device on a flexible plastic substrate, an inorganic layer (barrier) such as SiO$_2$, SiNx, or Al$_2$O$_3$ is deposited on the plastic substrate to prevent moisture and oxygen from penetrating into the OLED. Although the main causes of residual images on OLED displays are inherently related to the process variation of the backplane process and deterioration of the OLED material, TFT instability can aggravate image sticking under low frequencies and always-on-display applications. A few papers are available for the elucidation of the mechanism and reliability physics of the positive $V_{th}$ shift of p-type LTPS TFT and image sticking in regards to the substrate material, process integrity, and bias stress test conditions.

In this paper, information is given to elucidate the mechanism of the positive $V_{th}$ shift when the gate bias is applied to p-type LTPS TFTs fabricated on PI, as compared to a glass substrate. In order to probe the effects of charging on LTPS TFTs, three different metal-insulation-metal (MIM) capacitors were prepared for the C–V characterization. Finally, we delve into $V_{th}$ shift behaviors in the material properties of PI associated with the vertical structure of LTPS TFTs. The secondary ion mass spectrometry (SIMS) physical characterization and TCAD simulation are focused on the fluorine profile at the interface and effects of the polarity of charging on $V_{th}$ shift behaviors.

Results and Discussion

$V_{th}$ shift behaviors of LTPS TFTs fabricated on PI and glass substrates. Figure 1a shows the $I_D$–$V_G$ plot of p-type LTPS TFTs with glass and PI substrates on the top gate structure, before and after a gate stress of approximately 30 V for 4,000 s at 70 °C. In Fig. 1b, $\Delta V_{th}$ after BTS was plotted as a box plot using 5 TFTs fabricated on the glass and PI substrate. On average, the $\Delta V_{th}$ of the TFT fabricated on glass showed a slight change, less than −0.02 V, and the $\Delta V_{th}$ of the TFT fabricated on the PI showed a positive shift with an average 0.83 V. In addition, $I_{on}$
increased from $2.08 \times 10^{-5}$ A to $2.46 \times 10^{-5}$ A, and field effect mobility increased from 85 to 113 cm$^{-2}$. However, under the identical stress conditions, the parameters of the LTPS TFT fabricated on glass substrate are rarely changed. It is somewhat interesting to note that the $V_{th}$ of p-type LTPS TFTs with a PI substrate is positively shifted under the negative gate bias. It is speculated that the negative charging is generated from the PI substrate below the gate insulation layer.

In order to further probe the positive $V_{th}$ shifts, 4-pad evaluation was conducted. As shown in Fig. 2a, a bias of 50 V was applied to the floating gate adjacent to the LTPS TFT to minimize the effects of the poly channel on electrical charging in the PI substrate. $V_{th}$ behaviors are shown in Fig. 2b. As shown, the LTPS TFT with a glass substrate demonstrates stabilized $V_{th}$ behaviors throughout stressing at 70 °C up to 80,000 s. Note that Region I, II, and III represent the temperature and bias conditions used; 70 °C without bias, 70 °C with 50 V, and room temperature without bias, respectively. From Region I to II, the $V_{th}$ of the TFT with a PI substrate increases and positively shifts with increasing time. The $V_{th}$ tends to decrease and then return to the initial $V_{th}$ after 1 h in Region III. In turn, Region III is intended to observe the recovery behaviors of the $V_{th}$ of the LTPS TFT with a PI substrate. Since the recovery of the $V_{th}$ observed in Region III could result in display image disturbance, such as image sticking defined as residual images, efforts in electrical and physical characterization are inevitable.

One would argue that the positive $V_{th}$ shifts of the TFT with a PI substrate mentioned are related to design flaws somehow associated with the layout design of the metal route, which can impact TFT stability as electrical fields arise from adjacent metals near TFT devices. However, such artifacts were eliminated by design review throughout circuit simulation.

Since the $V_{th}$ stability of TFT devices plays an important role for display image performance, particularly for image sticking, the relationship between the $\Delta V_{th}$ vs. image sticking was investigated. Using the checkerboard test pattern, the image sticking index is estimated by comparing luminance changes before and after stressing. The white area adjacent to black patterns in the checkerboard becomes darker after stressing, which indicates
image sticking. Figure 3 shows the correlation between PI charging induced $\Delta V_{th}$ and image sticking. It is shown that the larger the $\Delta V_{th}$, the higher the propensity for image sticking. These results show that the correlation between $V_{th}$ shift and image sticking needs to be further discussed with electrical and physical characterization.

MIM capacitor fabrication, C–V measurement and physical SIMS characterization. In an effort of probing the $V_{th}$ behaviors mentioned above, three different metal–insulator-metal (MIM) capacitors, such as Ag/PI/Ag, Ag/SiO$_2$/Ag and Ag/SiO$_2$/PI/Ag were prepared for the C–V measurements conducted by varying voltage at a frequency of 100 kHz. SiO$_2$ is the barrier layer of the LTPS TFT, and the thickness and process conditions are the same with the measured TFT. Figures 4a–d show the schematics of the vertical structure for the MIM capacitors, i.e., Ag/SiO$_2$/Ag, Ag/PI/Ag, Ag/SiO$_2$/PI/Ag, and the cross-sectional analysis of the MIM capacitor. An Ag metal electrode was sputtered onto the spin-coated PI and SiO$_2$, deposited using the PECVD process. As a result, the PI and PI/SiO$_2$ function as the insulators between the metal electrodes.

Using Eq. (1), the physical dimension, dielectric constant, and capacitance of each capacitor are estimated and summarized in Table 1.

$$\frac{1}{C_{\text{Total}}} = \frac{1}{C_{\text{SiO}_2}} + \frac{1}{C_{\text{PI}}} + \frac{1}{C_{\text{PI/SiO}_2}}$$

(1)

Figure 5 shows the results obtained from the C–V measurements. It is apparent that changes in capacitance depend on the MIM capacitors. The capacitances of the SiO$_2$ and PI dielectric insulators between the Ag
electrodes rarely change, even with increasing voltage (see Fig. 5a,b). However, the capacitance of the SiO$_2$/PI dielectric tends to increase with increasing voltage. It was also found that the magnitude of capacitance turns into the initial state after 1 h of halting bias, as shown in Fig. 5c. In Fig. 5d, the capacitance of the SiO$_2$/PI rapidly increases with increasing voltage. Such results agree well with the recovery of the $V_{th}$ described in Fig. 2b. Thus, it is legitimate that the positive $V_{th}$ shift of a TFT with a PI substrate is attributed to charging between the SiO$_2$ and PI interface. As such, charge generation at the interface between the SiO$_2$ and the PI plays an important role for TFT device stability, particularly for the PI substrate.

In sequence, SIMS analysis is adopted to explicate the positive $V_{th}$ shifts of p-type LTPS TFTs with a PI substrate. To understand the effects of PI on the $V_{th}$ shift, two different PIs with low and high crosslink density, named PI-A and PI-B, were chosen to prepare the Ag/SiO$_2$/PI/Ag capacitor. We first suspected that oxygen or moisture had penetrated from the PI. Changes in hydrogen ions (H$^-$), hydroxyl group (OH$^-$), and oxygen ions (O$^-$) before/after bias stress of Ag/SiO$_2$/PI/Ag capacitors were confirmed through SIMS analysis. Figure 6 shows the results of SIMS analysis before and after bias stress of MIM capacitors fabricated based on PI-A and PI-B. There was no change in H$^-$, OH$^-$, or O$^-$ before/after bias stress, confirming that there was no penetration of oxygen or moisture from PIs. Figure 7 shows the correlation between the fluorine profile at the SiO$_2$/PI interface and capacitance, characterized by SIMS and C–V measurement. Comparatively, the SIMS analyses revealed that PI-A has a higher fluorin content than PI-B at the interface (see Fig. 7a,c). In consequence, C–V measurements shown in Fig. 7b,d show that the capacitance of the MIM capacitor with PI-B is rarely changed even with increased stressing at 70 °C. It has been reported that the negative fluorine ions, F$, are subjected to transfer and trapped in the SiO$_2$ under the bias$^{14}$. As a result, SIMS analyses evidences that a mobile ion F$^-$ in the SiO$_2$/PI interface contributes to the positive shifts of LTPS TFTs with a PI substrate. This suggests that the amount of charging generated in the PI is dependent on the material property of the PI. Hence, the material property of the PI is a crucial factor that can influence LTPS TFTs with a PI substrate. It has been also found that PI charging that significantly affects TFT reliability can be successfully suppressed by the selection of a proper PI with high volume resistivity$^{15}$. However, the charge generation and transfer into the barrier layer remained in unripe areas.

### Table 1. MIM capacitance and parameters from C–V measurement.

| Thickness (um) | SiO$_2$ | PI | PI/SiO$_2$ |
|---------------|---------|----|------------|
| Capacitance (F) | 6.37 $\times$ 10$^{-9}$ | 7.56 $\times$ 10$^{-10}$ | 9.39 $\times$ 10$^{-11}$ |
| $\Delta Q/q$ for 30 V stress (/cm$^2$) | 2.7 $\times$ 10$^{10}$ | 5.3 $\times$ 10$^{10}$ | 2.0 $\times$ 10$^{10}$ |

![Figure 5. C–V characterization for 3 different MIM capacitors with increasing voltage; (a) Ag/SiO$_2$/Ag, (b) Ag/PI/Ag, (c) Ag/SiO$_2$/PI/Ag, and (d) the dependency of the MIM capacitors on the applied voltage.](image)

In sequence, SIMS analysis is adopted to explicate the positive $V_{th}$ shifts of p-type LTPS TFTs with a PI substrate. To understand the effects of PI on the $V_{th}$ shift, two different PIs with low and high crosslink density, named PI-A and PI-B, were chosen to prepare the Ag/SiO$_2$/PI/Ag capacitor. We first suspected that oxygen or moisture had penetrated from the PI. Changes in hydrogen ions (H$^-$), hydroxyl group (OH$^-$), and oxygen ions (O$^-$) before/after bias stress of Ag/SiO$_2$/PI/Ag capacitors were confirmed through SIMS analysis. Figure 6 shows the results of SIMS analysis before and after bias stress of MIM capacitors fabricated based on PI-A and PI-B. There was no change in H$^-$, OH$^-$, or O$^-$ before/after bias stress, confirming that there was no penetration of oxygen or moisture from PIs. Figure 7 shows the correlation between the fluorine profile at the SiO$_2$/PI interface and capacitance, characterized by SIMS and C–V measurement. Comparatively, the SIMS analyses revealed that PI-A has a higher fluorin content than PI-B at the interface (see Fig. 7a,c). In consequence, C–V measurements shown in Fig. 7b,d show that the capacitance of the MIM capacitor with PI-B is rarely changed even with increased stressing at 70 °C. It has been reported that the negative fluorine ions, F$, are subjected to transfer and trapped in the SiO$_2$ under the bias$^{14}$. As a result, SIMS analyses evidences that a mobile ion F$^-$ in the SiO$_2$/PI interface contributes to the positive shifts of LTPS TFTs with a PI substrate. This suggests that the amount of charging generated in the PI is dependent on the material property of the PI. Hence, the material property of the PI is a crucial factor that can influence LTPS TFTs with a PI substrate. It has been also found that PI charging that significantly affects TFT reliability can be successfully suppressed by the selection of a proper PI with high volume resistivity$^{15}$. However, the charge generation and transfer into the barrier layer remained in unripe areas.
TCAD simulation for charge generation at the interface between the SiO$_2$ and PI. Based on empirical data collected from reliability assessments, Silvaco TCAD was used to simulate the effects of charging at the SiO$_2$/PI interface on the TFT transfer curve. Figure 8 shows the $I_D$–$V_G$ plot of an LTPS TFT with a PI substrate. As shown, the negative charging in the SiO$_2$/PI interface shifts the $V_{th}$ to the positive direction, while the positive charging results in a negative $V_{th}$ shift. Accordingly, when $-2 \times 10^{11}$/cm$^2$ charging is generated at the interface between the SiO$_2$ and the PI, the estimated $V_{th}$ shift toward the positive direction is 0.84 V.

Table 2 contains the estimated TFT parameters, such as $V_{th}$, $\mu_{FE}$, subthreshold swing (SS), and on/off ratio, based on the given charge injections shown in Fig. 8.

Figure 9 is given to explain the hole concentration of an LTPS TFT with a PI substrate with the bias condition at $V_{GS} = -30$ V and $V_{DS} = -0.1$ V. The Reference (black filled circle) and $-2 \times 10^{11}$/cm$^2$ (blue filled triangle) represent the LTPS TFT with and without charging at the SiO$_2$ and PI interface. Recall that $2 \times 10^{11}$/cm$^2$ is obtained from the C-measurement summarized in Table 1. As shown in the inlet in Fig. 9, when the negative bias is applied to the gate of the LTPS TFT, hole carriers tend to be accumulated near the channel and then

Figure 6. Hydrogen, hydroxy group and oxygen profiles obtained by SIMS measurements of capacitors before/after bias stress; (a) Ag/SiO$_2$/PI-A/Ag and (b) Ag/SiO$_2$/PI-B/Ag.

Figure 7. SIMS characterization of Ag/SiO$_2$/PI/Ag capacitor focused on fluorine profile at the interface; (a, b) with PI-A type and (c, d) with PI-B type. Note that PI-A is less crosslink density than PI-B.
exponentially decrease. However, when negative charging exists at the PI substrate, hole concentration decreases then increases below the channel depth of 30 nm. It is known that the negative charges at the interface between the SiO2 and PI result in an early turn-on Vth leading to increased field effective mobility and Ion, which is similar to the ID–VG characteristic observed from the double gate TFTs16,17. Hence, the state of charging at the interface determines the characteristics of the LTPS TFTs with a PI substrate.

Conclusions
Considering the direction of Vth shift of p-type LTPS TFTs with gate bias stress, the charge trapping mechanism, depending on the type of the substrate in the top gate structure, are comprehensively investigated. Unlike the glass substrate, the positive Vth shift of p-type LTPS TFTs with a PI substrate under the BTS test results from the negative charging of fluorine at the interface between the SiO2 and PI is proven by C–V measurement and SIMS characterization. In fact, the fluorine stems from the PI substrate under gate bias stress. Furthermore, TCAD simulation reveals that the direction of the Vth shift strongly depends on the polarity of charge trapping at the SiO2 and PI interface. The larger Vth shifts are prone to the higher propensity of image sticking. Hence,
care must be taken for the selection of PI in order to ensure display image performance in advanced flexible display technologies.

Methods

P-type LTPS TFTs were fabricated on either a PI or glass substrate through the standard backplane process, in which plasma enhanced chemical vapor deposition (PECVD) was used for a-Si and SiO₂ (barrier) deposition and crystallized into poly-Si by using excimer laser annealing (ELA). Thus, the vertical structure of the p-type LTPS TFTs consists of the gate/gate insulator/poly-Si/buffer/barrier/PI or glass substrate on the top gate structure. In a pixel circuit driver, 4/4 μm transistor and 200 μm/200 μm capacitance were monitored by I–V and C–V measurement. V₉₀ behaviors were monitored as a function of bias stress on the gates of the LTPS TFTs. To probe electrical charging in PI, three different metal–insulator-metal (MIM) capacitors, Ag/Pt/Ag, Ag/SiO₂/Ag, and Ag/SiO₂/Pt/Ag, were prepared for the C–V measurements. Changes in capacitance were measured as a function of voltage level. Moreover, the effects of charging in PI on the LTPS TFTs were taken into account by selecting different types of PIs such as PI-A and PI-B. Fluorine profiles were carefully analyzed by SIMS characterization. Finally, the effects of PI charging on the LTPS TFTs were consummated by using TCAD simulation.

Received: 20 July 2020; Accepted: 6 April 2021
Published online: 16 April 2021

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Acknowledgements

This work was supported by the Industrial Human Resources and Skill Development Program (P0012453, Next-generation Display Expert Training Display Expert Training Project for Innovation Process and Equipment, Materials Engineers) funded by the Ministry of Trade, Industry, and Energy (MOTIE, Korea). And we thank Yun Jung Jang from Korea Institute of Science and Technology (KIST) for helping us perform the ToF-SIMS experiments.

Author contributions

H.K., J.P., T.K., J.S. and B.C. designed this work. H.K. and S.B. fabricated the devices, and H.K., J.P., T.K., S.B., J.S. and B.C. measured the electrical characteristics of the devices and performed analysis. H.K performed SEM plots extracted through TCAD simulation. All authors discussed the findings and contributed to writing the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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