High Gain Boost Converter with Reduced Voltage in Capacitors for Fuel-Cells Energy Generation Systems

Javier Loranc-Coutiño 1, Carlos A. Villarreal-Hernandez 1, Jonathan C. Mayo-Maldonado 1, Jesús E. Valdez-Resendiz 1, Adolfo R. Lopez-Núñez 2, Omar F. Ruiz-Martinez 3,* and Julio C. Rosas-Caro 4,*

1 Faculty of Engineering, Instituto Tecnologico y de Estudios Superiores de Monterrey, Av. Eugenio Garza Sada 2501, 64849 Monterrey, Mexico; a00813600@itesm.mx (J.L.-C.); a01350242@itesm.mx (C.A.V.-H.); jc Mayo@itesm.mx (J.C.M.-M.); jesusvaldez@itesm.mx (J.E.V.-R.)
2 Laboratory of Electrical and Power Electronics, Tecnologico Nacional de Mexico/ITS Irapuato, Carretera Irapuato-Silao km 12.5 Colonia El Copal, 36821 Irapuato, Mexico; adolfo.lopez@itesi.edu.mx
3 Faculty of Engineering, Universidad Panamericana, Josemaria Escriva de Balaguer 101, 20290 Aguascalientes, Mexico
4 Faculty of Engineering, Universidad Panamericana, Alvaro del Portillo 49, 45010 Zapopan, Mexico
* Correspondence: ofruizm@up.edu.mx (O.F.R.-M.); crosas@up.edu.mx (J.C.R.-C.);
Tel.: +52-44-4263-4071 (O.F.R.-M.); +52-33-1918-1065 (J.C.R.-C.)

Received: 30 July 2020; Accepted: 28 August 2020; Published: 10 September 2020

Abstract: This work presents a power-electronics based system for renewable energy applications, the system is driven with an only one switch quadratic type boost converter, the discussed converter is based on a stack of switching stages which provide a large voltage gain, a desirable feature for fuel cell generation systems, the converters gain function is the quadratic boost-type converters; furthermore, the topology can be extended. The major benefit of the topology is that there is not a capacitor that sustains the entire output voltage, in contrast to other similar topologies in which there is a capacitor rated to the output port voltage, there is no high voltage capacitor in this system. Experimental verification is presented to confirm the system principles; experiments included a fuel cell emulator that was built and used for the experiments.

Keywords: renewable energies; dc–dc converter; PEMFC-power-conditioning stage; step-up converter

1. Introduction

Step-up converters are widely used in electronic systems, such as green energy production systems like those based on fuel cells or photovoltaic panels. Converters applied to those applications usually require to step-up the low voltage provided by the fuel cell to meet the requirements of grid-tie inverters.

Several solutions exist that can fulfill the challenge and achieve high voltage conversion ratios, for example, topologies based on magnetic coupling such as transformers and/or coupled inductors [1–3]. Another plausible solution is the use of transformer-less topologies, which can be built with commercial components (off-the-shelf), which is an advantage for magnetic coupling-based converters, transformer-less topologies provide a reduced size solution. Transformer-less converters can be based on several principles such as (1) voltage multipliers based on switched capacitors [4,5]; (2) combination of circuits which input are parallel connected, and which outputs are connected in series [6–8]; (3) quadratic topologies [9,10], etc.

This article presents a boots type dc–dc converter with quadratic voltage gain and a reduced number of active components (it uses only one transistor). Previously presented in [11], in this case,
the converter is intended to be used with a fuel-cell based renewable energy generation system, the converter quadratic-gain makes it a good option for the fuel-cell based application, in which a low voltage with variable amplitude requires to be boosted and regulated, the converter under study is based on a stackable structure of several switching stages, their main characteristic is a relatively high voltage gain given in a quadratic type gain equation, a desirable feature for fuel cell generation systems. The major benefits of the quadratic converter are: the output voltage is provided by all capacitors connected in additive series, in contrast with other circuits that have several capacitors, including a large capacitor that sustains the (relatively large) voltage at the output port. The system operation and the major benefits of the proposed system are corroborated with experimental results; a fuel cell emulator was built and used for the experimental results.

2. Quadratic Boost Converter

This section describes the discussed topology; the principle operation is also described. The quadratic topology is displayed in Figure 1; it is made by the MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor): $s$, fast recovery diodes: $s_1$, and $s_2$, capacitors: $C_1$, and $C_2$, and inductors: $L_1$, and $L_2$.

![Figure 1](image_url)

Figure 1. Quadratic boost type converter with low energy stored in capacitors: (a) circuit schematic, (b) equivalent switching state in the case the MOSFET is closed, (c) equivalent switching state in the case the MOSFET is open.

2.1. Qualitative Comparison with Other Boost Type Converters

The classical boost topology and the quadratic boost topology are displayed in Figure 2. The major benefit of the quadratic converter shown in Figure 1, against the classic quadratic boost topology in Figure 2b, is that the output port voltage isn’t provided with only one capacitor, that capacitor would have to be rated to the output voltage, which is relatively high, the output port voltage in the discussed topology is provided with a series connection of the input port voltage and two both capacitors of the converter, each of them rated to a fraction of the output voltage.

![Figure 2](image_url)

Figure 2. Traditional topologies: (a) Boost converter, (b) Quadratic boost converter.
Former quadratic types of topologies in the state-of-the-art are presented in [9,10,12–14]. For example, [9,14] in which a similar single-switch quadratic converter is presented, but in that case, only one capacitor has a reduced voltage compared to the traditional converter, and the output capacitor still supports the total output voltage, and stores the larger amount of energy.

In Figure 3, we illustrate the voltage stress across capacitors versus the duty ratio D in the discussed topology and the quadratic boost topology.

![Voltage stress comparison for each capacitor.](image)

Voltage stresses in Figure 3 are normalized to (divided over) the input source voltage, for instead, if D = 0.6, the voltage in C2 for the new converter is around the input source voltage multiplied by four, while it is around six times the input voltage for the traditional converter, it is clear that for the entire range of duty cycle values, the voltages in capacitors for the topology in Figure 1 are always smaller than the voltage in capacitors for the topology in Figure 2b. This allows for reducing the price and volume of the system.

There are quadratic types of topologies in the state-of-the-art that perform switching ripple cancelation, in which series capacitors have shifted voltage ripple, for example, [15,16], in that case, those converters require at least two transistors and a particular PWM (Pulse-Width Modulation) strategy.

2.2. Mathematical Model and Operation Principle of the Converter

This section provides the mathematical model of the converter considering ideal components; this model can provide a reference for the converter operation. Losses produced by parasitic components tend to limit the real voltage gain of the converter; this limitation is derived and explained in Section 2.4.

The converter has two switching states, which are shown in Figure 1, those switching states can be used to derive the averaging model of the circuit, the derived model, which assumes that the voltage in capacitors and current through inductors have a small ripple, and inductors $L_1$ and $L_2$ operate in CCM (Continuous Conduction Mode).

When the transistor is closed, see Figure 1b, diode $s_1$ is also closed and conducts the current $i_{L1}$, the diode $s_2$ is open since it is inversely polarized with $(V_g + V_{C1})$. In a similar manner, $s_2$ is inversely polarized with $(V_g + V_{C1} + V_{C2})$, which is actually the output port voltage. $i_{L1}$ rises during this switching state with a derivative equal to $V_g/L_1$, and $i_{L2}$ is also rising in this switching state with a derivative equal to $(V_g + V_{C1})/L_2$. The mathematical model of the switching state would be given by Equations (1)–(4).

\[
L_1 \frac{d i_{L1}}{dt} = V_g \tag{1}
\]

\[
L_2 \frac{d i_{L2}}{dt} = V_g + V_{C1} \tag{2}
\]

\[
C_1 \frac{d V_{C1}}{dt} = i_{L2} - \frac{v_o}{R} \tag{3}
\]
\[ C_2 \frac{dC_2}{dt} = -\frac{v_o}{R} \]  \hfill (4)

In the other switching state, shown in Figure 1c, the current \( i_{L_1} \) drops with a derivative equal to \(-V_{C_1}/L_1\), the diode \( s_1 \) closes charging capacitor \( C_1 \), the current \( i_{L_2} \) also decreases with a derivative equal to \(-V_{C_2}/L_2\), the diode \( s_2 \) closes charging capacitor \( C_2 \), diode \( s_1 \) is inversely polarized with \( V_{C_2} \). The mathematical model of this state would be given by Equations (5)–(8).

\[ L_1 \frac{di_{L_1}}{dt} = -v_{C_1} \]  \hfill (5)

\[ L_2 \frac{di_{L_2}}{dt} = -v_{C_2} \]  \hfill (6)

\[ C_1 \frac{dv_{C_1}}{dt} = i_{L_1} - \frac{v_o}{R} \]  \hfill (7)

\[ C_2 \frac{dv_{C_2}}{dt} = i_{L_2} - \frac{v_o}{R} \]  \hfill (8)

The voltage at the output port \( V_o \), see Figure 1, is given by the sum of voltage in all capacitors plus the input \( V_o = V_g + V_{C_1} + V_{C_2} \).

Considering the inductors current and capacitors voltage as state variables, the model of switching stages can be averaged to get the non-linear large-signal model given by Equations (9)–(12).

\[ L_1 \frac{di_{L_1}}{dt} = dv_g - (1 - d)v_{C_1} \]  \hfill (9)

\[ L_2 \frac{di_{L_2}}{dt} = d(v_g + v_{C_1}) - (1 - d)v_{C_2} \]  \hfill (10)

\[ C_1 \frac{dv_{C_1}}{dt} = -di_{L_2} + (1 - d)i_{L_1} - \frac{v_o}{R} \]  \hfill (11)

\[ C_2 \frac{dv_{C_2}}{dt} = (1 - d)i_{L_2} - \frac{v_o}{R} \]  \hfill (12)

where \( d \) is the duty ratio, the proportion of time in which the transistor is closed, it is calculated by dividing the time period in which the MOSFET is closed over the full commutation or switching period \( T_S \); the large-signal model can be used to get the equilibrium or steady-state. By zeroing the derivatives in Equations (9)–(12), the equilibrium would be described by Equations (13)–(16).

\[ V_{C_1} = \frac{D}{1 - D} V_g \]  \hfill (13)

\[ V_{C_2} = \frac{D}{(1 - D)^2} V_g \]  \hfill (14)

\[ I_{L_1} = \frac{1}{(1 - D)^2} \frac{V_o}{R} \]  \hfill (15)

\[ I_{L_2} = \frac{1}{(1 - D)^2} \frac{V_o}{R} \]  \hfill (16)

While the output voltage \( V_o \) is given, as mentioned, by Equation (17).

\[ V_o = V_g + V_{C_1} + V_{C_2} = \frac{1}{(1 - D)^2} V_g \]  \hfill (17)

Equation (17) is (as expected) the quadratic gain of the boost converter.

From Figure 1 and the mathematical model of the switching stages, the principle of operation can be explained in the following manner:
(1) When the transistor is closed, see Figure 1b, inductors have positive voltage (while capacitors have negative current), which results in an increase of the energy stored in inductors, the current in inductors have a positive derivative, equations, inductor $L_1$ is getting charged with energy coming from the input source $V_g$ (see Equation (1)), while inductor $L_2$ is getting charged with energy coming from both the input source $V_g$ and capacitor $C_1$ (see Equation (2)).

(2) When the transistor is open, see Figure 1c, capacitors have positive current (while inductors have negative voltage), which results in an increase of the energy stored in capacitors, inductor $L_1$ transfer energy to capacitor $C_1$ and inductor $L_2$ transfer energy to capacitor $C_2$.

(3) The energy flows from the input source to $L_1$, when the transistor is closed, from $L_1$ to $C_1$ when the transistor is open, from $C_1$ (and $V_g$) to $L_2$ when the transistor is closed, from $L_2$ to $C_2$ when the transistor is open, and from $C_2$ (and $C_1$, and $V_g$) to the load during all the time.

(4) The energy conservation produces that since the output voltage is larger than the input voltage, with a voltage gain given by Equation (17), the input current is larger than the output current with the same proportion. This can be observed from Equation (15), the dc input current is the same as $I_{L1}$ since the capacitor $C_1$ cannot drain dc current.

2.3. Extending the Topology to an N to the Power Boost Converter

The discussed circuit can be extended to an N to the power exponential boost converter; Figure 4 shows the generalized converter with N switching stages.

![Generalized extension of topology.](image-url)

A general expression for the output port voltage gain can be derived by observing that inductor $L_3$ is charged (when the switch is on) by the input port voltage plus the sum of all capacitors in the previous switching stages, inductor $L_1$ is charged only with $v_g$, inductor $L_2$ is getting charged by $v_g + v_{C1}$, inductor $L_3$ is charged with $v_g + v_{C1} + v_{C2}$, etc. The dynamic equation of $L_3$ would be written as

$$L_3 \frac{dI_{L3}}{dt} = d(v_g + v_{C1} + v_{C2}) + (1 - d)(-v_{C3})$$  \hspace{1cm} (18)

The dynamic equation of $L_N$ would be written as Equation (19).

$$L_N \frac{dI_{LN}}{dt} = d(v_g + v_{C1} + \ldots + v_{C(N-1)}) + (1 - d)(-v_{CN})$$  \hspace{1cm} (19)
The voltage in capacitor $C_3$ would be expressed as Equation (20).

$$V_{C3} = \frac{D}{(1-D)}(V_g + V_{C1} + V_{C2})$$  \hspace{1cm} (20)

The voltage in the capacitor $C_N$ would be expressed as Equation (21).

$$V_{CN} = \frac{D}{(1-D)}(V_g + V_{C1} + V_{C2} + \ldots + V_{C(N-1)})$$  \hspace{1cm} (21)

The output voltage of a converter with three switching stages would be expressed as Equation (22).

$$V_{out(N=3)} = (V_g + V_{C1} + V_{C2} + V_{C3})$$  \hspace{1cm} (22)

This can be solved by remembering Equation (23).

$$V_g + V_{C1} + V_{C2} = V_g \frac{1}{(1-D)^2}$$  \hspace{1cm} (23)

By substituting Equation (23) in Equation (20), the voltage $V_{C3}$ can be expressed as Equation (24).

$$V_{C3} = \frac{D}{(1-D)}\left(V_g \frac{1}{(1-D)^2}\right) = V_g \frac{D}{(1-D)^3}$$  \hspace{1cm} (24)

By considering Equations (20) and (23), the output voltage of a converter with three switching stages would be expressed as Equation (25).

$$V_{out(N=3)} = \left(V_g \frac{1}{(1-D)^2} + V_g \frac{D}{(1-D)^3}\right)$$  \hspace{1cm} (25)

$$V_{out(N=3)} = V_g \left(\frac{1}{(1-D)^2} + \frac{D}{(1-D)^3}\right) = \frac{V_g}{(1-D)^3}$$ \hspace{1cm} (26)

Equation (26) is the cubic boost topology gain, with observations made in this procedure, Equation (19) can be rewritten as Equation (27).

$$L_N \frac{di_N}{dt} = d(v_{out(N-1)}) + (1-d)(v_{CN})$$  \hspace{1cm} (27)

from which the voltage in the capacitor $C_N$ can be expressed as Equation (28).

$$V_{CN} = \frac{D}{(1-D)}(V_{out(N-1)})$$  \hspace{1cm} (28)

and the output voltage of a converter with $N$ switching stages would be expressed as Equation (29).

$$V_{out(N)} = V_{out(N-1)} + \frac{D}{(1-D)}(V_{out(N-1)}), \quad V_{out(N)} = V_{out(N-1)}\left(1 + \frac{D}{(1-D)}\right) = V_{out(N-1)}\frac{1}{(1-D)}$$  \hspace{1cm} (29)

Each switching stage multiplies the previous voltage gain with a factor of the traditional boost gain; each switching stage adds an exponential to the previous voltage gain.

$$V_{out(N)} = V_g \frac{1}{(1-D)^N}$$  \hspace{1cm} (30)
2.4. Real Voltage Gain Considering Inductor ESR (Equivalent Series Resistance)

The analysis provided in Section 2.2, does not include parasitic components, which affect the real voltage gain of the converter, especially those in the charging and discharging loop of inductors. This section is dedicated to analyzing this effect; for more information about the effects on parasitic components, readers may refer to [17–27].

The real gain, which considers losses, is smaller than the ideal, the main lossy element that limits the real gain is the inductor losses modeled as an equivalent series resistor ESR, due to the complexity of the circuit, the calculation requires an intermediate step. Therefore, we analyzed the real gain in a converter that contains only one inductor and capacitor, see Figure 5.

![Converter with only one inductor and one capacitor.](image)

Figure 5. Converter with only one inductor and one capacitor.

Observe that the circuits in Figure 5 contain the inductor ESR; when applying the averaging technique, this ESR would appear as a voltage drop in the inductors voltage equations, which according to the equivalent circuits in Figure 5b,c, can be expressed as Equations (31) and (32).

\[
\frac{L}{dt} \frac{d i_L}{d t} = d(v_L - R_Li_L) + (1 - d)(-v_C - R_i, L)
\]  
(31)

\[
\frac{C}{dt} \frac{d v_C}{d t} = d\left(-\frac{v_{out}}{R}\right) + (1 - d)(i_L - \frac{v_{out}}{R})
\]  
(32)

Equations (31) and (32) can be simplified to Equations (33) and (34).

\[
\frac{L}{dt} \frac{d i_L}{d t} = d v_L - (1 - d)v_C - R_Li_L
\]  
(33)

\[
\frac{C}{dt} \frac{d v_C}{d t} = (1 - d)i_L - \frac{v_{out}}{R}
\]  
(34)

The output voltage \( v_{out} \) is the series connection of the input voltage \( v_L \) plus the capacitor’s voltage. From Equations (33) and (34) the equilibrium can be derived, as well as in the last section, the state variables must be constant in the equilibrium, and by zeroing the left–hand–side of Equations (33) and (34) the steady-state can be expressed as Equations (35) and (36).

\[
0 = DV_L - (1 - D)V_C - R_LI_L
\]  
(35)

\[
0 = (1 - D)I_L - \frac{V_L + V_C}{R}
\]  
(36)

From Equation (36), the inductor current may be expressed as Equation (37).

\[
I_L = \frac{V_L + V_C}{D^*R}
\]  
(37)
By substituting Equation (37) into Equation (35), the capacitor voltage may be expressed as Equation (38).

\[
V_C = V_g \left( D - \frac{R_L}{D' R} \right) \left( (1 - D) + \frac{R_L}{(1 - D) R} \right)
\] (38)

The output voltage \(v_{out}\) is the series connection of the input voltage \(v_g\) plus the capacitor voltage (see Figure 5a), and then, by adding \(v_g\) plus Equation (38), the output voltage is expressed as Equation (39).

\[
V_{out} = V_g \frac{1}{(1 - D) + \frac{R_L}{(1 - D) R}}
\] (39)

The output voltage port gain of the converter topology in Figure 5, which considers the equivalent series resistance in the inductance is calculated as Equation (40).

\[
G = \frac{V_{out}}{V_g} = \frac{1}{(1 - D) \left( 1 + \frac{R_L}{(1 - D)^2 R} \right)}
\] (40)

Equation (40) shows the same gain of the classical boost converter when considering parasitic resistance that limits the voltage across the inductor, those parasitic resistances may consider only the inductors ESR, or it may consider other parasitic resistances that appear in series with the inductor, such as the on-resistance in the MOSFET.

Equation (40) may also be represented in a circuital manner, as Figure 2a [13].

The circuit in Figure 6 is based on transformers with \((1 - D):1\) turns ratio. The circuit representation of Equation (40) allows us to derive a general representation of the converter since the circuital representation of the cascade connection of switching stages is simpler to solve than in the algebraic equations.

![Figure 6](image_url)

**Figure 6.** (a) Equivalent circuit to Equation (40), (b) two cascaded converters equivalent circuit, (c) simplifying two converters into one.

If two switching stages are connected in a manner, then the second converter is the load of the first one, both converters may be represented by Figure 6b, the input source and the first resistor may be pushed to the secondary side of the first transformer [13], and the total circuit would be equal to the
one shows in Figure 6c, similar to Figure 6a and have the gain represented by Equation (40) when the total inductor resistance is written as Equation (41).

\[ R_L = \frac{R_{L1}}{(1 - D)^2} + R_{L2} \]  

(41)

In the same manner, three switching stages in cascaded would have the same gain in Equation (40) when the total inductor resistance would be

\[ R_L = \frac{R_{L1}}{(1 - D)^3} + \frac{R_{L2}}{(1 - D)^2} + R_{L3} \]  

(42)

Finally, if \( N \) switching stages are connected in cascaded, Equation (40) holds when the total inductor resistance is

\[ R_{LT} = \frac{R_{L1}}{(1 - D)^{2(N-1)}} + \frac{R_{L2}}{(1 - D)^{2(N-2)}} + \ldots + \frac{R_{LN-1}}{(1 - D)^{2(N-(N-1))}} + \frac{R_{LN}}{(1 - D)^{2(N-N)}} \]  

(43)

2.5. Component Selection

Passive components are usually selected according to the desired maximum ripple, when the switch is on, see Figure 2a, both inductors are getting charged; in this switching state, their current ripples are calculated with Equations (34) and (35).

\[ \Delta i_{L1} = \frac{V_g}{2L_1} DT_S \]  

(44)

\[ \Delta i_{L2} = \frac{V_g + V_{C1}}{2L_2} DT_S \]  

(45)

where \( T_S = 1/f_S \) is the converter’s switching period, the inverse of the switching frequency, from Figure 4, the current ripple in an arbitrary inductor \( L_x \) (when the switch is on) can be expressed as Equation (46).

\[ \Delta i_{Lx} = \frac{(V_g + V_{C1} + \ldots + V_{C(x-1)})}{2L_x} DT_S \]  

(46)

From Figure 2b, when the switch is off, both capacitors are getting charged, their voltage ripples mathematical expressions are Equations (47) and (48).

\[ \Delta v_{C1} = \frac{(I_o - I_{L1})}{2C_1} (1 - D) T_S \]  

(47)

\[ \Delta v_{C2} = \frac{(I_o - I_{L2})}{2C_2} (1 - D) T_S \]  

(48)

From Figure 4, the current ripple in an arbitrary capacitor \( C_x \) (when the switch is off) can be expressed as Equation (46).

\[ \Delta v_{Cx} = \frac{(I_o - I_{Lx})}{2C_x} (1 - D) T_S \]  

(49)

From Figure 2b, when the switch is on, both capacitors are getting charged with and, their voltage ripple is calculated with Equation (46). From the provided equations, passive components can be chosen to meet the desired percentage of the switching ripple.

When the MOSFET is open, see Figure 1, it sustains the output voltage, which is expressed by Equation (17) in the case of the base topology (Figure 1), and it is expressed by Equation (30) for the case of the generalized topology (Figure 4). The MOSFET must be then rated to the maximum output
voltage plus a safety range, to ensure the voltage will not overpass the rated voltage. New silicon carbide devices are usually rated to a larger voltage compared to traditional silicon-based MOSFETS.

When the MOSFET is closed, it drains the summation of the current through both inductors, in the case of the base topology (Figure 1), and then, their RMS current can be calculated as Equation (50).

\[ I_{S(RMS)} = (I_{L1} + I_{L2}) \sqrt{1 + \frac{1}{3} \left( \frac{\Delta I_{L1} + \Delta I_{L2}}{I_{L1} + I_{L2}} \right)^2} \] (50)

For the generalized topology, see Figure 4, the transistor current is the summation of the current through all inductors; in that case, their RMS current can be calculated as Equation (51).

\[ I_{S(RMS)} = (I_{L1} + I_{L2} + \ldots + I_{Lx}) \sqrt{1 + \frac{1}{3} \left( \frac{\Delta I_{L1} + \Delta I_{L2} + \ldots + \Delta I_{Lx}}{I_{L1} + I_{L2} + \ldots + I_{Lx}} \right)^2} \] (51)

3. Experimental Results with the Fuel Cell Emulator

A dynamic model of a PEMFC (Proton-Exchange Membrane Fuel Cell) using a hardware-in-the-loop set-up was implemented to validate the implementation of the proposed converter under a realistic scenario, as is illustrated in Figure 7. The PEMFC model was programmed using LabVIEW, a data acquisition hardware, and a controlled DC source as an actuator. In particular, we measure the output current of the emulated PEMFC and define in a dynamic manner, the corresponding value of voltage according to the first principle model of the cell.

![Figure 7. Fuel cell emulator with hardware control.](image)

An algorithm based on the fuel cell equations was developed in the LabView environment and ran on a CompactRIO system, the idea is to measure the current drawn from the fuel cell and with that current to compute the voltage at terminals that a real cell would have. The CompactRIO controls the power supply in real-time, which is an independent system from the dc–dc converter, which has its own closed-loop control; the entire system is a hardware-in-the-loop real-time system.

The studied converter is feed by the programable DC source. This emulation is done in real-time using a National Instruments cRIO 9039 and a DC power source Keysight N6953A.

The realization of the fuel cell model is based on the Nernst reversible voltage equation based on four voltage components [28–30], i.e.,

\[ V_{fc} = E_{Nernst} - V_{act} - V_{conc} - V_{ohm} \] (52)
where $E$ represents the Nernst voltage $V_{act}$ is the activation loss, $V_{conc}$ is the concentration loss, and $V_{ohm}$ is the ohmic loss. Figure 8 shows the electrical model representation of the FC (Fuel Cell). The voltage at the output port varies according to the electric load. As mentioned before, three types of losses occur within the model; they are classified as activation, concentration, and ohmic losses.

![Electrical circuit model of the PEMFC.](image)

### 3.1. Cell Reversible Voltage

The Nernst voltage or the reversible voltage corresponds to the potential at the output port of the FC with no-load. In [30] a modified version of the equation of this voltage drop is presented with a term that considers the temperature, $P_{O2}$ and $P_{H2}$ are the partial pressures of oxygen and hydrogen, respectively.

$$E_{Nernst} = 1.229 - 0.85 \times 10^{-3}(T - 298.15) + 4.31 \times 10^{-5}T \left[ \ln(P_{H2}) + \frac{1}{2} \ln(P_{O2}) \right]$$  \hspace{1cm} (53)

### 3.2. Activation Voltage Drop

Activation voltage losses have a greater impact when low currents circulate through the cell [31].

$$V_{act} = -[\xi_1 + \xi_2 T + \xi_3 T \ln C_{O2} + \xi_4 T \ln(I_{FC})]$$  \hspace{1cm} (54)

where $I_{FC}$ is the fuel cell current demanded by the load and $\xi$'s are parameters for the fuel cell model, and their values are based on kinetic, thermodynamic, and electrochemical theoretical equations.

$$C_{O2} = \frac{P_{O2}}{5.08 \times 10^{6} e^{-498/T}}$$  \hspace{1cm} (55)

### 3.3. Concentration Voltage Drop

Concentration or diffusion losses occur when there’s a change in the concentration of reactants; on the contrary of the activation losses, this has a greater impact at very high current, this can be seen in Equation (56).

$$V_{conc} = -B \ln \left(1 - \frac{J}{J_{\max}} \right)$$  \hspace{1cm} (56)

### 3.4. Ohmic Voltage Drop

The ohmic losses occur because of electrode resistance, current collectors, and polymeric membrane. They are proportional to the current that circulates in the fuel cell.

$$V_{ohm} = I_{FC}(R_{M} + R_{C})$$  \hspace{1cm} (57)
where RC is the transfer of protons resistance through the membrane with a value of 300 $\mu\Omega$ and $R_M$ is the membrane resistance expressed with Equation (58).

$$R_M = \left( \frac{\rho M l}{A} \right)$$ (58)

The polarization curve of the PEMFC is depicted in Figure 9, and the parameters of the Avista fuel cell stack 500 W are shown in Table 1.

![Figure 9. Polarization curve of the PEMFC.](image)

### Table 1. Avista 500 W fuel cell stack parameters.

| Param. | Value | Param. | Value |
|--------|-------|--------|-------|
| $n$    | 32    | $\xi_1$ | -0.948 |
| $T$    | 333 °K | $\xi_2$ | $0.00286 + 0.0002\ln A + (4.3 \times 10^{-5})$ |
| $A$    | 64 cm$^2$ | $\xi_3$ | $7.6 \times 10^{-5}$ |
| $l$    | 178 $\mu$m | $\xi_4$ | $-1.93 \times 10^{-4}$ |
| $P_{H_2}$ | 1 atm | $\psi$ | 23 |
| $P_{O_2}$ | 0.2095 atm | $i_{max}$ | 469 mA/cm$^2$ |
| $B$    | 0.016 V | $i_n$ | 3 mA/cm$^2$ |
| $R_C$  | 0.0003 $\Omega$ | $i_{max}$ | 30 A |

#### 3.5. Important Voltage and Current Signals

In Figure 10, we show a picture of the experimental prototype, which can corroborate some of the features of the converter, e.g., its small compact design even though it exhibits a much higher (quadratic) voltage gain, with respect to traditional topologies.
A controller is implemented to regulate the output port voltage. The diagram of the controller is depicted in Figure 11, which encompasses an input-current control loop as well as an output–voltage loop. The control was designed by using the small signal linearization approach [13], despite equations obtained from the averaging technique being non-linear (for example see Equations (9)–(12)) the small signal approach allows us to design a stable converter for a certain operation region by following the technique in part II of [13].

This is a convenient control architecture considering that it only requires two sensors for the input current and the output voltage, even though it is a high-order controller with four dynamic equations. The parameters of the experiment are shown in Table 2.

![Figure 10. Picture of the experimental prototype.](image)

![Figure 11. Schematic of the closed-loop controller.](image)

**Table 2. Parameters of the experiment.**

| Parameter                  | Value/Information                  |
|----------------------------|-----------------------------------|
| Input voltage              | 36 V                              |
| Output voltage             | 250 V                             |
| Switching frequency        | 50 kHz                            |
| Inductor $L_1$             | Ferrite core pot 330 µH, 74 mΩ    |
| Inductor $L_2$             | Ferrite core pot 820 µH, 154 mΩ   |
| Capacitor $C_1$            | Film polypropylene 20 µF          |
| Capacitor $C_2$            | Film polypropylene 20 µF          |
| MOSFET                     | IPW65R037C6 650 V                 |
| Diode                      | BYV229400 on voltage 1.05 V       |
| Load                       | BK precision electronic load 250 W|
| Controller gains $k_1$, $k_2$, $g_1$, $g_2$ | 100, 0.01, 10, 0.05 |
The control is designed in such a way that a stable output voltage is achieved indirectly by regulating the input current. The input-current control loop is implemented by a proportional and integral controller. This is because the quadratic converter has a non-minimum phase characteristic with respect to the output voltage, which is an instability condition for boost converters. The control loop is designed according to the consideration that a stable operation-point is achieved in steady-state, a linearization around this point was carried out, and the proportional and integral controllers were designed.

The transfer function of the converter can be expressed as Equation (59)

$$TF_{\text{converter}} = \frac{7.236s^4 + 3.568 \times 10^5s^3 + 7.785 \times 10^8s^2 + 2.008 \times 10^{13}s + 1.653 \times 10^{16}}{s^4 + 400s^3 + 6.113 \times 10^7s^2 + 1.826 \times 10^{10}s + 3.695 \times 10^{14}}$$

(59)

Figure 12 shows the bode plots of the converter both for both the open-loop and closed-loop operation.

In Figure 12, we include the comparison between the ideal polarization function of the FC and the experimental measurements that were performed to validate its behavior.

Some of the experimental measurements in terms of oscilloscope traces, as well as the dynamics of the FC emulator, are displayed in Figure 14, under continuous variations using a resistive load. In the case of Figure 14, the output voltage of the emulator (Vout) (not from the converter) which was built with the programable power source (see Figure 7) is changed un purpose, to perform the test, the closed-loop controller of the converter, adjust their duty cycle, requiring more current from the emulator (Iout) (which would be the input current of the converter), in order to maintain the output voltage, in which a resistive load is connected.

In Figure 15, we show the experiment result of the quadratic topology with stackable switching stages using a dc power source.

In order to show the effectiveness of the controller, we evaluated the dynamic response of the converter under continuous variations at the input-voltage. The results of this experiment are shown in Figure 16. It can be corroborated that the output voltage remains practically constant.
Figure 13. Polarization curve of the PEMFC (Proton-Exchange Membrane Fuel Cell) emulator in LabVIEW with a resistive load.

Figure 14. Experimental response of the PEMFC emulator operating with a resistive load.

Figure 15. Important waveforms of the quadratic topology in the open-loop case.

Finally, in Figure 17, we show the dynamic response of the converter in closed-loop when connected to the PEMFC emulator under continuous variations at the output load or the converter. Notice that the voltage remains constant, displaying a robust performance and providing a high-voltage gain, which makes it suitable for the proposed application.
Figure 16. Dynamic response of the converter in closed-loop under continuous variations on the input voltage.

Figure 17. Waveforms of the quadratic boost converter operating under load changes using the fuel cell emulator.

A final test was performed in which an LC filter ($L = 45 \, \mu H$ and capacitor $C = 20 \, \mu F$) was added between the fuel cell and the dc–dc converter, this to ensure the operation in the case a filter is required to smoot the current waveform, the test result was successfully, the voltage of the FC emulator was changed and the controller of the converter adjusts the current to successfully maintain their output voltage in a constant value, see Figure 18.

Figure 18. Waveforms of the final test, dynamic response under voltage changes including an LC filter.
3.6. Efficiency and Cost Comparison

An efficiency comparison was performed, with parameters in Table 2, for both the traditional quadratic boost converter and the converter under study, which can be a so-called new quadratic boost converter, the result is shown in Table 3 and Figure 19.

Table 3. Efficiency (in percentage) for converters with parameters of Table 2.

| P_{out} | 25  | 50  | 75  | 100 | 125 | 150 | 175 | 200 | 225 | 250 |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Traditional QBC | 94.87 | 94.73 | 94.52 | 94.28 | 94.04 | 93.80 | 93.55 | 93.31 | 93.06 | 92.79 |
| New QBC | 94.96 | 94.77 | 94.53 | 94.29 | 94.04 | 93.79 | 93.53 | 93.28 | 93.03 | 92.79 |

Figure 19. Efficiency comparison (Table 3).

The internal operation of the converter has some differences. For example, in the new converter, when the switch is on, C1 drains the current through L2 when the switch is on, as well as in the traditional quadratic boost, but in this case, it also drains the output current at the same time. On the other hand, in the traditional converter, the output current is drained by C2 all the time. When the switch is off, the current through C1 in the proposed converter is I_{11} - I_{out}, while in the traditional case is I_{11} - I_{L2}, which is a smaller value.

Despite the differences in the internal operation, there is no significant change in the efficiency; furthermore, capacitors usually dissipate a small percentage of the converter losses, their equivalent series resistance ESR is in the order of milliohms. Due to the similarity of efficiencies (see Table 3 and Figure 19), we can conclude the size of the converter (due thermal design) is not affected.

The efficiency is not the main advantage of the converter since it is similar to the available technology. The advantages of the converter topology are the cost, and the size, a capacitor is larger and more expensive as the voltage rating increases (for the same capacitance). For example, C1 sustains a voltage of 59 V in the example of Table 2, and C2 sustains a voltage of 95 V, against the traditional quadratic boost converter in which C1 sustains a voltage of 155 V in the same example, and C2 sustains a voltage of 250 V.

The cost comparison is focused on the capacitor selection, as other components have the same voltage and current rating in both the new and the traditional quadratic boost converter, Table 4 shows examples of capacitors of the same brand (Kemet) and type (film capacitors), which can be used to synthesize the converter, the information was obtained from Digi-Key, and the voltage rating was chosen for around 160% the voltage they need to sustain, which is a common practice for safety reasons, all capacitors are 10 µF, which is a common value (the capacitance of 20 µF can be obtained with two paralleled capacitors).

It can be observed from the selection, then for capacitors of the same type and capacitance, the increase of the voltage represents an increase on the cost and volume, the largest output capacitor of the traditional quadratic boost converter has to sustain 250 V, to achieve a safety over rating of 60%, we need to choose a 400 V capacitor, which volume and cost stand out others.
Table 4. Kemet capacitor selection for converters.

|                     | Kemet Part Number | Unit Cost | Max Voltage | Volume     | ESR       |
|---------------------|-------------------|-----------|-------------|------------|-----------|
| New Converter       | R60ER51004040K    | $3.94     | 100 V DC    | 4924 mm$^3$| -         |
| Traditional Converter | C4ATDBW5100A30J  | $5.85     | 250 V DC    | 19,008 mm$^3$| 3.1 mΩ    |
|                     | R75GR510050H0J    | $4.97     | 160 V DC    | 26,118 mm$^3$| 4.8 mΩ    |
|                     | R75MW510050H3J    | $7.91     | 400 V DC    | 43,923 mm$^3$| 4.8 mΩ    |

4. Conclusions

This article studies a boots type dc–dc converter with quadratic voltage gain and reduced number of active components (it uses only one transistor), is intended to be used with a fuel-cell based renewable energy generation system, the discussed converter is based on a stackable structure of several switching stages, their main characteristic is a relatively high voltage gain given in a quadratic type gain equation, a desirable feature for fuel cell generation systems. The major benefits of the quadratic converter are: (1) the output voltage is provided by all capacitors connected in additive series, in contrast with other circuits that have several capacitors, including a large capacitor that sustains the (relatively large) voltage at the output port; (2) the system operation and the major benefits of the proposed system are corroborated with experimental results; a fuel cell emulator was built and used for the experimental results.

Author Contributions: Authors J.C.R.-C., O.F.R.-M., and A.R.L.-N. contributed with the conceptualization of the article, from the power electronics point of view; J.C.M.-M. and J.E.V.-R. contributed with the control methodology; C.A.V.-H., J.L.-C., and A.R.L.-N. contributed with the software, validation, and formal analysis, doing basically most of the investigation; J.E.V.-R. and J.C.R.-C. wrote the draft and manuscript preparation. All authors have read and agreed to the published version of the manuscript.

Funding: This research was partially funded by Universidad Panamericana, through the program “Fomento a la Investigación UP 2020”, and project “Análisis de convertidores duales dobles” UP-CI-2020-GDL-01-ING. The APC was partially funded by the aforementioned project and partially by the Universidad Panamericana Dirección Institucional de Investigación.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Ibanez, F.M.; Echeverria, J.M.; Astigarraga, D.; Fontan, L. Multimode step-up bidirectional series resonant DC/DC converter using continuous current mode. *IET Power Electron.* 2016, 9, 710–718. [CrossRef]
2. Vázquez, N.; Medina, F.; Hernández, C.; Arau, J.; Vázquez, E. Double tapped-inductor boost converter. *IET Power Electron.* 2015, 8, 831–840. [CrossRef]
3. Vidales, B.; Madrigal, M.; Torres, D. High stepping DC/DC topology for voltage source converters in low power renewable energy applications. In Proceedings of the 2016 IEEE PES Transmission & Distribution Conference and Exposition-Latin America (PES T&D-LA), Morelia, Mexico, 20–24 September 2016; pp. 1–5.
4. Mayo-Maldonado, J.C.; Valdez-Resendiz, J.E.; Sanchez, V.M.; Rosas-Caro, J.C.; Claudio-Sanchez, A.; Puc, F.C. A novel PEMFC power conditioning system based on the interleaved high gain boost converter. *Int. J. Hydrog. Energy* 2019, 44, 12508–12514. [CrossRef]
5. Rosas-Caro, J.C.; Sanchez, V.M.; Vazquez-Bautista, R.F.; Morales-Mendoza, L.J.; Mayo-Maldonado, J.C.; Garcia-Vite, P.M.; Barbosa, R. A novel DC-DC multilevel SEPIC converter for PEMFC systems. *Int. J. Hydrog. Energy* 2016, 41, 23401–23408. [CrossRef]
6. Villarreal-Hernandez, C.; Mayo-Maldonado, J.C.; Escobar, G.; Loranca, J.; Valdez-Resendiz, J.E.; Rosas-Caro, J.C. Discrete-time Modeling and Control of Double Dual Boost Converters with Implicit Current-Ripple Cancellation Over a Wide Operating Range. *IEEE Trans. Ind. Electron.* 2020. [CrossRef]
7. Rosas-Caro, J.C.; Manzella-David, F.; Mayo-Maldonado, J.C.; Gonzalez-Lopez, J.M.; Torres-Espino, H.L.; Valdez-Resendiz, J.E. A Transformer-less High-Gain Boost Converter With Input Current Ripple Cancelation at a Selectable Duty Cycle. *IEEE Trans. Ind. Electron.* 2013, 60, 4492–4499. [CrossRef]
8. Choi, S.; Agelidis, V.G.; Yang, J.; Coutelier, D.; Marabeas, P. Analysis, design and experimental results of a floating-output interleaved-input boost-derived DC-DC high-gain transformer-less converter. *IET Power Electron.* 2011, 4, 168–180. [CrossRef]

9. Morales-Saldana, J.A.; Loera-Palomo, R.; Palacios-Hernandez, E.; Gonzalez-Martinez, J.L. Modelling and control of a dc-dc quadratic boost converter with R2P2. *IET Power Electron.* 2014, 7, 11–22. [CrossRef]

10. Lopez-Santos, O.; Martinez-Salamero, L.; Garcia, G.; Valderrama-Blavi, H.; Zambrano-Prada, D.A. Steady-State Analysis of Inductor Conduction Modes in the Quadratic Boost Converter. *IEEE Trans. Power Electron.* 2017, 32, 2253–2264. [CrossRef]

11. Valdez-Resendiz, J.E.; Rosas-Caro, J.C.; Mayo-Maldonado, J.C.; Llamas-Terres, A. Quadratic boost converter based on stackable switching stages. *IET Power Electron.* 2018, 11, 1373–1381. [CrossRef]

12. Chincholkar, S.H.; Jiang, W.; Chan, C. A Normalized Output Error-Based Sliding-Mode Controller for the DC–DC Cascade Boost Converter. *IEEE Trans. Circuits Syst. II Express Briefs* 2020, 67, 92–96. [CrossRef]

13. Erickson, R.; Maksimovic, D. *Fundamentals of Power Electronics;* Power Electronics Ser; Springer: New York, NY, USA, 2001.

14. Loera-Palomo, R.; Morales-Saldaña, J.A. Family of quadratic step-up dc-dc converters based on non-cascading structures. *IET Power Electron.* 2015, 8, 793–801. [CrossRef]

15. Lopez-Santos, O.; Mayo-Maldonado, J.C.; Rosas-Caro, J.C.; Valdez-Resendiz, J.E.; Zambrano-Prada, D.A.; Ruiz-Martinez, O.F. Quadratic boost converter with low-output-voltage ripple. *IET Power Electron.* 2020, 13, 1605–1612. [CrossRef]

16. Mayo-Maldonado, J.C.; Valdez-Resendiz, J.E.; Garcia-Vite, P.M.; Rosas-Caro, J.C.; del Rosario Rivera-Espinosa, M.; Valderrabano-Gonzalez, A. Quadratic Buck–Boost Converter with Zero Output Voltage Ripple at a Selectable Operating Point. *IEEE Trans. Ind. Appl.* 2019, 55, 2813–2822. [CrossRef]

17. Ayachit, A.; Reatti, A.; Kazimierczuk, M.K. Small-signal modeling of PWM dual-SEPIC DC-DC converter by circuit averaging technique. In *Proceedings of the IECON 2016-42nd Annual Conference of the IEEE Industrial Electronics Society,* Florence, Italy, 23–26 October 2016; pp. 3606–3611.

18. Luchetta, A.; Manetti, S.; Piccirilli, M.C.; Reatti, A.; Kazimierczuk, M.K. Comparison of DCM operated PWM DC-DC converter modelling methods including the effects of parasitic components on duty ratio constraint. In *Proceedings of the 2015 IEEE 15th International Conference on Environment and Electrical Engineering (EEEIC),* Rome, Italy, 10–13 June 2015; pp. 772–777.

19. Luchetta, A.; Manetti, S.; Piccirilli, M.C.; Reatti, A.; Kazimierczuk, M.K. Effects of parasitic components on diode duty cycle and small-signal model of PWM DC-DC buck converter in DCM. In *Proceedings of the 2015 IEEE 15th International Conference on Environment and Electrical Engineering (EEEIC),* Rome, Italy, 10–13 June 2015; pp. 772–777.

20. Kazimierczuk, M.K. *Pulse-Width Modulated dc–dc Power Converters,* 2nd ed.; John Wiley & Sons: Hoboken, NJ, USA, 2015.

21. Davoudi, A.; Jatskevich, J.; Chapman, P.L. Simple method of including conduction losses for average modelling of switched-inductor cells. *Electron. Lett.* 2006, 42, 1246–1247. [CrossRef]

22. Iftikhar, M.U.; Lefranc, P.; Sadarnac, D.; Karimi, C. Theoretical and experimental investigation of averaged modeling of non-ideal PWM DC-DC converters operating in DCM. In *Proceedings of the 2008 IEEE Power Electronics Specialists Conference,* Rhodes, Greece, 15–19 June 2008; pp. 2257–2263.

23. Davoudi, A.; Jatskevich, J.; Chapman, P.L. Averaged modelling of switched-inductor cells considering conduction losses in discontinuous mode. *IET Electr. Power Appl.* 2007, 1, 402–406. [CrossRef]

24. Luchetta, A.; Manetti, S.; Piccirilli, M.C.; Reatti, A.; Kazimierczuk, M.K. Derivation of network functions for PWM DC-DC Buck converter in DCM including effects of parasitic components on diode duty-cycle. In *Proceedings of the 2015 IEEE 15th International Conference on Environment and Electrical Engineering (EEEIC),* Rome, Italy, 10–13 June 2015; pp. 778–783.

25. Davoudi, A.; Jatskevich, J.; Rybel, T.D. Numerical state-space average-value modeling of PWM DC-DC converters operating in DCM and CCM. *IEEE Trans. Power Electron.* 2006, 21, 1003–1012. [CrossRef]

26. Amir, S.; Zee, R.V.D.; Nauta, B. An Improved Modeling and Analysis Technique for Peak Current-Mode Control-Based Boost Converters. *IEEE Trans. Power Electron.* 2015, 30, 5309–5317. [CrossRef]

27. Davoudi, A.; Jatskevich, J.; Chapman, P.L. Numerical Dynamic Characterization of Peak Current-Mode -Controlled DC–DC Converters. *IEEE Trans. Circuits Syst. II Express Briefs* 2009, 56, 906–910. [CrossRef]
28. Gebregergis, A.; Pillay, P. Implementation of fuel cell emulation on dsp and dspace controllers in the design of power electronic converters. In Proceedings of the 2008 IEEE Industry Applications Society Annual Meeting, Edmonton, AB, Canada, 5–9 September 2008.

29. Wang, C.; Nehrir, M.H.; Shaw, S.R. Dynamic models and model validation for pem fuel cells using electrical circuits. *IEEE Trans. Energy Convers.* 2005, 20, 442–451. [CrossRef]

30. Voottipruex, K.; Sangswang, A.; Naetiladdanon, S.; Mujjalinvimut, E.; Wongyoa, N. Pem fuel cell emulator based on dynamic model with relative humidity calculation. In Proceedings of the 2017 14th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON), Phuket, Thailand, 27–30 June 2017; pp. 529–532.

31. Lee, H.S.; Jeong, K.S.; Oh, B.S. An experimental study of controlling strategies and drive forces for hydrogen fuel cell hybrid vehicles. *Int. J. Hydrog. Energy* 2003, 28, 215–222. [CrossRef]