Revisiting the theory of ferroelectric negative capacitance

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Abstract—In this paper we revisit the theory of negative capacitance, in a (i) standalone ferroelectric, (ii) ferroelectric-dielectric, and (iii) ferroelectric-semiconductor series combination, and show that it is important to minimize the total Gibbs free energy of the combined system (and not just the free energy of the ferroelectric) to obtain the correct states. The theory is explained both analytically and using numerical simulation, for ferroelectric materials with first order and second order phase transitions. The exact conditions for different regimes of operation in terms of hysteresis and gain are derived for ferroelectric-dielectric combination. Finally the ferroelectric-semiconductor series combination is analyzed to gain insights into the possibility of realization of steep slope transistors in a hysteresis free manner.

I. INTRODUCTION

Reducing the supply voltage while maintaining the performance is one of the key focus areas of current device research, which would enable reduction of power consumption up to the system level [1]. It is well known that the long high energy tail of the Fermi-Dirac distribution of carrier population at the source junction does not allow the MOSFET current to be changed by any more than a decade for every 60 mV change in the gate voltage at room temperature. This is a fundamental bottleneck of MOSFET operation that limits the supply voltage scaling. Ways to beat this subthreshold slope limit of 60 mV/decade have been intensely investigated in the past [2]-[6].

To this end, ferroelectric negative capacitance FET (FerroFET) was proposed [6] where the gate insulator of a MOSFET is replaced by a ferroelectric material. With an increase in the gate voltage (over a certain range), the internal “negative capacitance” of the ferroelectric forces the voltage drop across itself to decrease, which in turn increases the channel surface potential of the semiconductor by a value which is more than the change of the gate voltage. Such a gain mechanism between the external gate voltage and the internal channel surface potential allows for a larger change in drain current than what is predicted by 60 mV/decade, even though the current-surface potential relationship is still limited by the tail of the Fermi-Dirac distribution [6]-[10].

One question that is frequently asked in this context is whether it is possible to maintain such voltage gain in a hysteresis free way so as to achieve the eventual goal of reducing supply voltage of digital logic. In the recent past, there have been a number of efforts to investigate this, both theoretically [6]-[11] and experimentally [12]-[13]. However, a clear understanding of the mechanism of such devices is still lacking in the literature, which is partly due to the solution methodology typically adopted - by minimizing the Gibbs free energy for the ferroelectric and then equating the ferroelectric polarization at the minimum energy point to the charge per unit area of the series capacitance [6]-[13]. Unfortunately, this does not necessarily minimize the total Gibbs free energy of the combined system since both components (ferroelectric and series capacitance) can have complex dependence of free energy on appropriate state variable. It turns out that although both the approaches gives rise to same results for a linear capacitor placed in series with the ferroelectric, the results can be quite different when the series capacitance is non-linear in nature (for example, semiconductor channel).

Our aim in this paper is threefold: (i) to establish a theory based on the minimization of Gibbs free energy of the whole system, (ii) to find the exact conditions for hysteresis free gain in a ferroelectric-dielectric series combination to check if it is possible to have a design window for such operation, and (iii) to understand a FerroFET operation using a one dimensional FerroMOSCAP analysis to elucidate whether a sub-60 mV/decade operation is possible in a hysteresis free manner.

The rest of the paper is organized as follows: The method of Gibbs free energy minimization is established using a simple example of two linear dielectric capacitors in series in sec. II. The concept of negative capacitance is then explained using a single standalone ferroelectric capacitor in sec. III. This is followed by a detailed analysis of ferroelectric-dielectric series combination in sec. IV. The FerroMOSCAP analysis is performed in sec. V which is followed by discussion on some practical aspects in sec. VI. Conclusions that can be drawn are presented in sec. VII.

II. METHOD OF GIBBS FREE ENERGY MINIMIZATION

When a system is excited by an external stimulus $X$, and if $Y$ is an appropriate internal state variable, the system reorganizes $Y$ in such a manner that the Gibbs free energy of the whole system is minimized. To explain this, we use a simple example of two capacitors, with $C_1$ and $C_2$ being the capacitance per unit area, connected in series and excited by an external voltage $V$, as shown in the inset of Fig. I. For isothermal process and in the absence of any stress, the Gibbs free energy ($\Delta G$) of a dielectric capacitor is just the electrostatic energy $\int D \cdot dE$, where $D$ is the displacement.
vector and $\vec{E}$ is the electric field. In this paper, we assume all quantities to be uniform in-plane and perform one dimensional analysis, removing the vector signs for simplicity. $D$ then becomes equal to the charge per unit area ($Q$) at the capacitor plates. The $\Delta G$ of the combined system is given by

$$\Delta G = \frac{Q^2}{2C_1} + \frac{Q^2}{2C_2} - QV$$

where $V$ is the external supply voltage. For a given $V$, the system will settle $Q$ in such a way that $\Delta G$ is minimized, i.e. $\frac{\partial \Delta G}{\partial Q} = 0$ and $\frac{\partial^2 \Delta G}{\partial Q^2} > 0$, which gives rise to the well known result of combined capacitance $C = \frac{Q}{V} = \frac{C_1 + C_2}{C_1 C_2}$. The same result is readily obtained electrostatically by equating the charges on the capacitor plates, i.e. $C_1(V - V_i) = C_2V_i$ where $V_i$ is the internal node voltage. It’s interesting to note from Fig. 1 that when $\Delta G$ is minimized, both $\Delta G_1$ and $\Delta G_2$ are above their individual minimum due to non-monotonic dependence of $\Delta G_{1,2}$ on $Q$. This leads to an important conclusion that when a system stabilizes in its Gibbs free energy minimum, the subsystems may not necessarily be in their individual energy minimum with respect to the internal state variable.

III. A STANDALONE FERROELECTRIC CAPACITOR

Using the phenomenological treatment of Landau, and ignoring any surface and domain boundary effect, the Gibbs free energy of the ferroelectric capacitor is given by [17]

$$\Delta G_f = t_f \times (\alpha_1 Q^2 + \alpha_{11} Q^4 + \alpha_{111} Q^6 - E_f Q)$$

where $E_f$ is the constant field within the ferroelectric and is an independent excitation variable. $Q$ is charge per unit area of the capacitor plate, and $\alpha_i$ are the Landau coefficients of the ferroelectric and are summarized in Table I for PbZr$_{0.52}$Ti$_{0.48}$O$_3$ (PZT) [18] and BaTiO$_3$ (BTO) [19]. Using $\frac{\partial \Delta G_f}{\partial Q} = 0$, we find

$$E_f = 2\alpha_1 Q + 4\alpha_{11} Q^3 + 6\alpha_{111} Q^5$$

The results are summarized for PZT in Fig. 2 which shows that as $E_f$ is increased from a large negative value, the free energy of the ferroelectric increases, and the system gradually moves from stable (green dot) to metastable state (black dot). On further increase of electric field, the ferroelectric remains in the metastable state as long as there is an energy barrier between the current state and the newly created stable state. Finally, the ferroelectric reaches the red dot point at an electric field equal to the coercive field, where all energy barrier is removed and the polarization of the ferroelectric abruptly changes as it moves to the other free energy minimum. In the process of such a hysteretic polarization jump, the ferroelectric exhibits a transient negative capacitance as it moves through the states where $\frac{\partial^2 \Delta G}{\partial Q^2} < 0$. However, a standalone ferroelectric does not traverse the negative slope portion in the $Q$-$E_f$ curve [red solid line in Fig. 2(a)-(b)], since this line corresponds to the locus of the local maxima in the free energy landscape where the ferroelectric is not allowed to stabilize.

IV. A FERROELECTRIC CAPACITOR IN SERIES WITH A CONSTANT CAPACITOR

This situation is schematically shown in Fig. 3. It has been proposed in the past [6] that the negative capacitance can be accessed in a hysteresis free way by adding a dielectric capacitor in series. Such a combination has been generally analyzed [6]-[11] by first minimizing the Gibbs free energy of the ferroelectric assuming the electric field within the ferroelectric ($E_f$) is the independent excitation, and then equating the polarization at the ferroelectric free energy minimum to the charge per unit area of the capacitor plate. Such an approach does not necessarily minimize the total $\Delta G$ of the ferroelectric/dielectric combination.

| Parameters | PZT [18] | BTO [19] |
|------------|---------|---------|
| $\alpha_1$ (mF$^{-1}$) | $-5.2393 \times 10^{-2}$ | $-3.2851 \times 10^{-2}$ |
| $\alpha_{11}$ (mF$^{-2}$ C$^{-1}$) | $5.8252 \times 10^{-2}$ | $-0.380 \times 10^{-2}$ |
| $\alpha_{111}$ (mF$^{-3}$ C$^{-4}$) | $1.5639 \times 10^{-2}$ | $4.3000 \times 10^{-4}$ |

Fig. 1. Gibbs free energy ($\Delta G$) of two capacitors (1 and 4 F/m$^2$ in series, with an applied bias $V = 5$ V. The individual Gibbs free energy of the two capacitors ($\Delta G_{1,2}$) and the battery ($\Delta G_B$) are also shown. The minima of $\Delta G_{1,2}$ do not coincide with total free energy minimum.

Fig. 2. (a): $\Delta G$ of a standalone Pb$_{0.52}$Zr$_{0.48}$TiO$_3$ (PZT) capacitor, plotted as a function of $Q$ for varying electric field. (b): $Q$ and (c): $\Delta G$, plotted as a function of electric field across it. The green, black and red dots show absolutely stable, metastable and unstable states.
Before discussing further we state few assumptions that we take in the analysis presented in the rest of the paper: (i) The ferroelectric is perfectly uniform and is governed by the bulk expression in Eq. 2. Any relaxation due to domain boundaries is ignored. (ii) The ferroelectric-dielectric has a perfect interface with no added strain or charge. (iii) The leakage current through the whole stack is negligible.

The Gibbs free energy of the ferroelectric/dielectric combination under applied bias $V$ is given by

$$\Delta G = t_f \left[ \alpha_1 Q^2 + \alpha_{11} Q^4 + \alpha_{111} Q^6 \right] + \frac{Q^2}{2C} - QV$$

where $t_f$ is the thickness of the ferroelectric film, $C = \epsilon_0 \epsilon_c / t_c$, $\epsilon_0$ is the permittivity of free space, $\epsilon_c$ is dielectric constant, and $t_c$ is the thickness of the dielectric film. Using $\frac{\partial \Delta G}{\partial Q} = 0$, we get

$$V = (2\alpha_1 t_f + \frac{1}{C})Q + 4\alpha_{11} t_f Q^3 + 6\alpha_{111} t_f Q^5$$

Note that the condition in Eq. 3 only dictates that $\Delta G$ is at an extremum. To make sure that $\Delta G$ is minimized, we need $\frac{\partial^2 \Delta G}{\partial Q^2} > 0$, which in turn confirms that the net differential capacitance ($C_T$) of the whole system is positive since $C_T = \frac{\partial^2 \Delta G}{\partial Q^2}$. We can solve Eq. 3 to obtain the states of the combined system at a given $V$.

A. Condition for hysteresis-free operation

Noting that the primary cause for hysteresis in a system is the existence of two free energy minima separated by an energy barrier, we argue that the sufficient condition for hysteresis-free operation is that the system should have only one free energy minimum. Mathematically, this would mean that the $\Delta G-Q$ curve (which is a polynomial of degree 6) will have less than two points of inflection, or the equation

$$\frac{\partial^2 \Delta G}{\partial Q^2} = 0$$

will have less than two solutions for real $Q$. Using Eq. 4, Eq. 6 becomes

$$Q^4 + \frac{2\alpha_{11}}{5\alpha_{111}} Q^2 + \frac{1}{30\alpha_{111}}(2\alpha_1 + \frac{1}{Ct_f}) = 0$$

which gives

$$Q^2 = \frac{1}{2} \left[ -\frac{2\alpha_{11}}{5\alpha_{111}} \pm \sqrt{\left( \frac{2\alpha_{11}}{5\alpha_{111}} \right)^2 - \frac{2}{15\alpha_{111}} \left( 2\alpha_1 + \frac{1}{Ct_f} \right) } \right]$$

1) Case I - Second order phase transition ($\alpha_{11} > 0, \alpha_{111} > 0$): From Eq. 8 by observation, $Q$ has no real solution for

$$\frac{1}{Ct_f} > -2\alpha_1$$

which corresponds to absence of points of inflection, leading to hysteresis-free operation with a single minimum. As a sanity check, this condition also ensures that the coefficient of $Q^2$ in Eq. 5 is positive. On the other hand, for $\frac{1}{Ct_f} < -2\alpha_1$, $Q$ will have only 2 real solutions corresponding to conventional bistable $\Delta G-Q$ curve.

2) Case II - First order phase transition ($\alpha_{11} < 0, \alpha_{111} > 0$): (i) For no real solution of $Q$, the term under the square root is less than zero, which reduces to

$$\frac{1}{Ct_f} < -2\alpha_1$$

for hysteresis free operation.

(ii) For only 2 real solutions of $Q$ (which correspond to bistable states as in case I),

$$-\frac{2\alpha_{11}}{5\alpha_{111}} - \sqrt{\left( \frac{2\alpha_{11}}{5\alpha_{111}} \right)^2 - \frac{2}{15\alpha_{111}} \left( 2\alpha_1 + \frac{1}{Ct_f} \right) } < 0$$

which reduces to

$$\frac{1}{Ct_f} < -2\alpha_1$$

which is exactly the same condition we obtained for $\alpha_{11} > 0$.

(iii) For $-2\alpha_1 < \frac{1}{Ct_f} < -2\alpha_1 + \frac{6\alpha_{11}}{5\alpha_{111}}$, there exist 4 points of inflection for real values of $D$, which correspond to three minima in $\Delta G$ leading to two hysteresis windows.

B. Condition for differential gain

For enhancement in capacitance (or differential voltage gain), we must have $C_T > C$. Again using the fact that $C_T = \frac{\partial^2 \Delta G}{\partial Q^2}$, we obtain the following inequality:

$$Q^4 + \frac{2\alpha_{11}}{5\alpha_{111}} Q^2 + \frac{\alpha_1}{15\alpha_{111}} < 0$$

This leads to a certain range of operation where we expect to have capacitance gain:

$$0 < Q^2 < -\frac{\alpha_{11}}{5\alpha_{111}} + \sqrt{\left( \frac{\alpha_{11}}{5\alpha_{111}} \right)^2 - \frac{\alpha_1}{15\alpha_{111}}}$$

This same condition holds good for both first and second order ferroelectric materials.

Although we were able to treat the problem analytically owing to simple linear nature of the charge-voltage relation of the dielectric capacitor, for a more general analysis, we...
need numerical simulation. The steps are shown in Fig. 3 At a given external voltage $V$, we choose charge $Q$ as the internal state variable and create a look-up table based on the general charge-Gibbs free energy relation of the generic capacitor $C$ and the ferroelectric. The total $\Delta G$ is then found as $\Delta G = \Delta G_f + \Delta G_c + \Delta G_B$, where $\Delta G_B$ is the free energy of the power supply. We choose all $Q = Q_0$ for which the total Gibbs free energy $\Delta G$ has extrema, of which the minima correspond to either stable or metastable states, and the maxima correspond to the unstable states (hence ignored).

Figures 4 summarizes the results for varying thickness of PZT (with $\alpha_{11} > 0$) deposited on 25nm thick SrTiO$_3$ (STO). Dielectric constant ($\varepsilon_r$) of STO is assumed to be 200. The thickness of the PZT layer in the top, middle and bottom rows are 10nm, 100nm and 150nm, respectively. We clearly see that the total $\Delta G$ maintains its single minimum character for top and middle rows, leading to hysteresis free operation. The corresponding charge per unit area ($Q$) plot in Fig. 4(b) and (f) indicate that the PZT goes through negative capacitance (negative slope of the $Q-V_f$ plot in red where $V_f$ is the voltage drop across the ferroelectric regime), although the slope for the whole system ($Q-V$ plot) remains positive (in blue), in agreement with the single minimum $\Delta G$ plot in Fig. 4(a) and (e). When the ferroelectric layer is very thick, $\Delta G_c$ cannot completely compensate the double minimum behavior of $\Delta G_f$ [Fig. 4(i)] and thus the combined system shows hysteretic character as observed in Fig. 4(j). In Fig. 4(c), (g) and (k), the corresponding internal node voltages $V_i$ are plotted as a function of external voltage $V$ showing quasi-linear dielectric, hysteresis-free gain, and hysteretic behavior, respectively. This point is further clarified in the differential capacitance plots in the last column (d, h, and l), where the total capacitance ($C_T$) becomes larger than the dielectric series capacitance ($C$) in a hysteresis-free way in (d) and (h), and with hysteresis in (l).

For the case of $\alpha_{11} < 0$, we choose the example of varying thickness of BaTiO$_3$ (BTO) on 25nm STO, and the results are summarized in Fig. 5 based on Landau parameters listed in Table II from ref. [19]. We clearly observe three different regimes of operation, in accordance with Table II. One important difference from the $\alpha_{11} > 0$ case is that the gain region splits away symmetrically from $V = 0$ and appears at some nonzero $\pm V$. With larger $t_f$, correspondingly two hysteresis windows open up, and eventually with further increment of $t_f$, they converge to a single large hysteresis window.

C. Peak capacitance in hysteresis-free operation

In the case of hysteretic jump, there is an abrupt change in charge, which gives rise to infinite differential capacitance at the steep jump point. On the other hand, in the case of hysteresis free operation, we can find the peak capacitance by noting that the total capacitance $C_T$ as

$$\frac{1}{C_T} = \frac{\partial^2 \Delta G}{\partial Q^2} = t_f (30\alpha_{111}Q^4 + 12\alpha_{11}Q^2 + 2\alpha_1) + \frac{1}{C} \quad (14)$$

Clearly, $C_T$ is maximum when

$$Q(5\alpha_{111}Q^2 + \alpha_{11}) = 0 \quad (15)$$

which is satisfied for either $Q = 0$ or $Q = \pm \left(-\frac{\alpha_{111}}{\alpha_{11}}\right)^{1/2}$. Noting that for $C_T$ to be maximum, we need $\frac{\partial^2 \Delta G}{\partial Q^2}(\frac{\alpha_{111}}{\alpha_{11}}) = 360\alpha_{111}t_f + 24\alpha_{11}t_f > 0$, we easily find that for second order ferroelectric ($\alpha_{11} > 0$), we obtain maximum $C_T$ at $Q = 0$. On the other hand, for first order ferroelectric ($\alpha_{11} < 0$), the maximum is reached for $Q = \pm \left(-\frac{\alpha_{111}}{\alpha_{11}}\right)^{1/2}$. Clearly, $C_T$ is single peak function for second order ferroelectric materials where, while for first order ferroelectric materials, it exhibits a double peak characteristics at symmetric $V$. This is in agreement with our observation in Fig. 4(h) and also in Fig. 5. The corresponding maximum capacitance is given by

$$C_T^{max} = \begin{cases} 
\left[\frac{1}{C} + 2\alpha_1 t_f\right]^{-1} & \text{if } \alpha_{11} > 0, \\
\left[\frac{1}{C} + 2\alpha_1 t_f - \frac{6\alpha_{111}}{5\alpha_{11}} t_f\right]^{-1} & \text{if } \alpha_{11} < 0
\end{cases}$$

which is in excellent agreement with the simulation predicted peak capacitance in Fig. 4(h).

| Regime of operation | $\alpha_{11} > 0, \alpha_{111} > 0$ | $\alpha_{11} < 0, \alpha_{111} > 0$ |
|---------------------|---------------------------------|---------------------------------|
| Hysteresis free (single minimum) (R1) | $\frac{1}{C_f} > -2\alpha_1$ | $\frac{1}{C_f} > -2\alpha_1 + \frac{6\alpha_{111}}{5\alpha_{11}}$ |
| Hysteric (double minima) (R2) | $\frac{1}{C_f} < -2\alpha_1$ | $\frac{1}{C_f} < -2\alpha_1 + \frac{6\alpha_{111}}{5\alpha_{11}}$ |
| Hysteric (three minima) (R3) | - | $-2\alpha_1 < \frac{1}{C_f} < -2\alpha_1 + \frac{6\alpha_{111}}{5\alpha_{11}}$ |

Fig. 5. $Q-V$ characteristics of a varying thickness ferroelectric (BTO) with first order phase transition ($\alpha_{11} < 0, \alpha_{111} > 0$), placed in series with 25nm thick STO showing transition from hysteresis-free to double-hysteresis window to single hysteresis window regimes.
V. A FERROELECTRIC CAPACITOR IN SERIES WITH A SEMICONDUCTOR (FERROMOSCAP)

We now turn our attention to what happens when a semiconductor is in series with a ferroelectric in a MOSCAP configuration. The primary difference with the previous case is that the areal charge density in the semiconductor is no more a linear function of voltage, rather a more complex function given by \( Q = \pm \sqrt{2e_i k_B T N_A} \left[ \left( e^{-\phi_s' + \phi_i'} - 1 \right) + \frac{n_i^2}{N_A^2} \left( e^{\phi_i' - \phi_s'} - 1 \right) \right]^{1/2} \) (16),

where \( \phi_s' = \frac{q_i}{k_B T} \phi_s \) is the surface potential, \( e_i \) is the dielectric constant of the semiconductor, \( k_B \) is the Boltzmann constant, \( T \) is the temperature, \( N_A \) is the doping density and \( n_i \) is the intrinsic carrier concentration. We use similar method as described in the flow chart in Fig. 3 for numerical simulation of the FerroMOSCAP structure. The fact that this charge is significantly less when compared with the typical charge across the ferroelectric for a wide range of input voltage, the charge-voltage relationship becomes distorted for the whole system. The semiconductor surface potential \( \phi_s \) and the charge per unit area \( (Q) \) of the ferroMOSCAP are shown in Fig. 6 as a function of gate voltage \( V \) for different semiconductor doping \( (N_A) \) and PZT thickness \( (t_f) \) combinations. The system may encounter different unstable regions, which correspond to the local maxima in total \( \Delta G \) and we explicitly show them in Fig. 6 by the negative slope regions in \( \phi_s \). Such instabilities are accompanied by a hysteretic jump in \( \phi_s \), as indicated by the arrows. Larger substrate doping slows down the build-up of charge in the system (with \( V > 0 \)) which in turn results in wider hysteresis window. On the other hand, thickness of the ferroelectric controls the return path, with larger hysteresis window for larger \( t_f \), as expected. It’s important to note that, for simplicity, we have assumed same Landau parameters for different thickness of PZT in Fig. 6.

To gain insights into such \( Q-V \) characteristics, in Fig. 7 we show the \( \Delta G \) of the whole system as a function of \( \phi_s \) for similar conditions as the red traces in Fig. 4(a),(b). The two strong minima on the left and the right in Fig. 7(a) are primarily governed by the strong ferroelectric polarization. However, the seemingly flat portion in the energy landscape can actually possess a number of local minima [Fig. 7(b)], which are governed by the way the charge is modulated in the semiconductor. In particular, as \( V \) is increased from a large negative value, the system stabilizes itself at the accessible minimum in \( \Delta G \) for every \( V \), and \( \phi_s \) is traced accordingly. This is explained in Fig. 7 by the open (forward sweep) and closed (reverse sweep) circles, which correspond to the sweeps indicated in red in Fig. 6(a) and (b).

VI. DISCUSSION

Before we conclude, let us discuss some important points:
Fig. 6. (a): Surface potential ($\phi_s$) versus applied gate bias ($V$) and (b): charge per unit area ($Q$) versus surface potential ($\phi_s$) for PZT/Si stack with different PZT thickness $t_f$. $N_A$ is kept fixed at $10^{14}$ cm$^{-3}$. Any gate leakage due to low band offset between PZT and Si has been neglected. The negative slopes in all the plots correspond to local maxima in the total $\Delta G$ of the system (shown in Fig. 7) and hence unstable, forcing hysteretic jumps shown by the dotted arrows. The black dashed-dotted lines in (a) indicate unity gain (corresponding to 60 mV/decade). (c)-(d): $t_f$ is kept fixed at 2 nm, and doping density in Si is varied as intrinsic, $10^{14}$ cm$^{-3}$ and $10^{16}$ cm$^{-3}$.

Fig. 7. Total $\Delta G$ of the PZT/Si stack [with same conditions as the red curves in Fig. 6(a), (b)] plotted as a function of surface potential $\phi_s$ for different gate voltage $V$. The relatively flat portion in (a) is zoomed in (b) to show the local minima states which control the system as low gate bias. The open and solid circles represent the state of the system in forward and reverse sweep, respectively, which is in agreement with Fig. 6(a) and (b).

(i) Effect of domains: In the whole analysis presented in this paper, we ignored any domain and interface effect, which in reality can significantly perturb the device characteristics. For example, domain nucleations may result in non-uniform feedback from the dielectric in series and hence the conditions for the different regimes of operation as tabulated in Table II may not be met exactly. As shown in [21], thinning down the ferroelectric may be helpful to reduce such non-uniformity.

(ii) Leakage issues: When a dielectric capacitor is placed in series with a ferroelectric, the ferroelectric forces a large amount of charge across the dielectric, which can easily drive the dielectric to operate close to breakdown. For example, with a ferroelectric polarization of $50\mu\text{C/cm}^2$ and dielectric $\epsilon_c$ of 50, the field across the dielectric capacitor is $\sim 10\text{MV/cm}$. A lower $\epsilon_c$ or higher polarization will make the field even higher. This may increase the leakage, particularly when the ferroelectric has a relatively low barrier offset.

(iii) Region of operation: For a FerroFET, in the subthresh-
old regime, the semiconductor offers a very small capacitance and provides a large negative feedback to the ferroelectric and it becomes difficult to extract an overall gain between the surface potential and the external gate voltage. Thus sub-60 mV/decade operation at subthreshold may be difficult to achieve in such a configuration. However, when the transistor is in inversion, the effective capacitance of the semiconductor increases significantly providing a less negative feedback to the ferroelectric. Thus above threshold voltage, the charge of the semiconductor offers a very small capacitance and provides a large negative feedback to the ferroelectric, due to strong mismatch of charge between the two, it becomes difficult to obtain such gain avoiding hysteresis, particularly in the subthreshold regime, and hence achieving a subthreshold slope below 60 mV/decade becomes difficult to achieve in hysteresis free manner. However, such a structure may be useful to reduce the overdrive voltage of the transistor, eventually reducing the chip supply voltage. Searching for ultra-thin, low polarization ferroelectric with a large band offset with the semiconductor will have important technological implications in this direction.

VII. CONCLUSION

In conclusion, we have investigated three different configurations, namely (i) a standalone ferroelectric, (ii) a ferroelectric in series with a dielectric capacitor, and (iii) a ferroelectric in series with a semiconductor. We pointed out that in all the cases, it is important to minimize the total Gibbs free energy of the whole system (and not just the ferroelectric) to reach to the correct solution for the states. By using this methodology, we found that it is possible to achieve hysteresis-free capacitance enhancement in a ferroelectric-dielectric combination. However, when a semiconductor is placed in series with the ferroelectric, due to strong mismatch of charge between the two, it becomes difficult to obtain such gain avoiding hysteresis, particularly in the subthreshold regime, and hence achieving a subthreshold slope below 60 mV/decade becomes difficult to achieve in hysteresis free manner. However, such a structure may be useful to reduce the overdrive voltage of the transistor, eventually reducing the chip supply voltage. Searching for ultra-thin, low polarization ferroelectric with a large band offset with the semiconductor will have important technological implications in this direction.

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