Upgrades to the CSC Cathode Strip Chamber electronics for HL-LHC

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ABSTRACT: The luminosity, latency, and trigger rate foreseen at the High Luminosity LHC (HL-LHC) present challenges to efficient readout of the Cathode Strip Chambers (CSCs, [1]) of the CMS end cap muon detector. Upgrades to the electronics are targeted for the inner rings of CSCs in each station, which have the highest flux of particles. The upgrades comprise digital cathode front end boards for nearly deadtimeless and long trigger latency operating capability, new DAQ boards that transmit data from the detectors with higher-bandwidth links, and a new data concentrator/interface to the central DAQ system that can receive the higher input rates.

KEYWORDS: Front-end electronics for detector readout; Wire chambers (MWPC, Thin-gap chambers, drift chambers, drift tubes, proportional chambers etc)
1 Introduction

The HL-LHC is projected to achieve an instantaneous luminosity as high as $0.75 \times 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$. CMS is planning on increasing the Level 1 Accept (L1A) latency from 3.4 $\mu$s to 12.5 $\mu$s and the rate from 100 kHz to 750 kHz [2].

The electronics of the CSC chambers is shown in figure 1. The performance of the CSC system was seen to match or exceed the design specifications during Run 1 [3]. It is foreseen that, in the absence of upgraded electronics, the more demanding conditions of the HL-LHC will lead to inefficiencies. There are three expected sources of inefficiency. The first is buffer overflow in the Switch Capacitor Arrays (SCAs) of the Cathode Front-End Boards (CFEB) of the inner chambers. The second is Anode Local Charged Track boards (ALCT) with insufficiently deep data buffers in all chambers. The third is from inadequate bandwidth of optical links between the DAQ Motherboards (DMB) and the Front-End Driver (FED). Several boards must be upgraded to remove these limitations and hence avert the failure of CSC readout at the HL-LHC.

The CSC electronics consist of two readout paths, the trigger path [4] and the data path [5]. The trigger path provides low granularity data, to be used by the trigger system, every 25 ns. The trigger primitives, formed by the CSC system, are called Local Charged Tracks (LCT). A LCT in a chamber is a pattern of hits compatible with a charged particle passing through the chamber. When the TMB has a Cathode LCT (CLCT) and Anode LCT (ALCT) correlated in time, it forms and sends an LCT signal to be used by the L1 Muon Track Finders [6] to reconstruct muon tracks.

The full-granularity data path is only read out upon the receipt of an L1A. The full-granularity data readout is orchestrated by the DMB. Upon receiving a trigger signal, the DMB collects the high granularity data payload from the other boards and sends them to the FED over an optical link. This data rate will significantly increase with the L1A rate. Plans for upgrading the rate capabilities of the data acquisition system are currently still under discussion, but the minimum specifications for the upgrade are already well understood.
Figure 1. An overview of the CSC readout system. Several parts of this system must be upgraded to handle the HL-LHC conditions. This proceeding particularly focuses on the CFEB, ALCT, TMB, DMB, and the FED system.

2 Buffer overflow in SCAs on CFEB boards

The voltages corresponding to the charge deposited on the cathode strips are buffered in SCAs. The buffers are used to store the information between an initial fast pre-LCT trigger and the L1A. Upon receipt of an L1A the buffers are used for storage during digitization by Wilkinson ADCs. An increase in L1A latency requires an increase in the depth of this buffer. A solution to this potential buffering failure is to use flash ADCs to digitize the signal continuously and to buffer it as a digital rather than analog signal. Selected electronics of the innermost ring of CSC station 1 (ME1/1) were upgraded during LHC Long Shutdown 1 (2013-2014) because among other reasons, a similar buffering failure was expected at even lower luminosities due to the higher rates in this region. In particular, the CFEBs were replaced with Digital CFEBs (DCFEBs) which were developed for this upgrade. The HL-LHC will require this same upgrade in the other inner ring CSC stations, ME2/1, ME3/1, and ME4/1. The highest rates other than in ME1/1 are seen in ME2/1. The location of the different types of chambers can be seen in figure 2.

2.1 Probabilistic queuing model

A queuing model [7] was used to project event loss up to the HL-LHC luminosity at various L1A rates. This model was verified with data by injecting pulse patterns, generated via Monte Carlo simulation of HL-LHC conditions, into a CFEB. The model shows good agreement with the data, as shown in figure 3.

The model was then applied to ME3/1 and ME4/1. With a L1A rate from 100 kHz to 750 kHz, all three rings were observed to lose more than 10% of events at the target instantaneous luminosity of $0.75 \times 10^{35}$ cm$^{-2}$ s$^{-1}$, as shown in figure 4.
Figure 2. The Muon Spectrometer of CMS, showing the different locations of CSC chambers in the current CMS muon system.

Figure 3. Data loss model applied to CFEB specifications in ME2/1 chambers. Good agreement with pulse injection data is seen.
Figure 4. Queuing model applied for Level 1 trigger rates of 300 kHz and 750 kHz in ME2/1, ME3/1, and ME4/1. 300 kHz trigger rates were studied to understand potential changes to the CMS HL-LHC plan.

2.2 Upgrading CFEBs to DCFEBs and TMBs to OTMBs

A comparison of the two boards can be seen in figure 5. This upgrade is to be extended to the rest of the inner ring chambers. The same queuing model as described in section 2.1 was applied to the DCFEB and acceptable performance was observed as seen in figure 6. Upgrading to DCFEBs also requires upgrading the corresponding Trigger Mother Boards (TMB) to Optical TMBs (OTMBs) that support the optical trigger data links from the DCFEBs.

3 ALCT data loss

The Virtex E FPGA used on the original version of the ALCT mezzanine board does not have enough block RAM to store anode hits during the HL-LHC L1A latency of 12.5 us. These boards will be replaced by a new Spartan-6 mezzanine board that was developed for the ME4/2 chambers that were installed in Long Shutdown 1. For the inner ring chambers, the ALCT boards will be modified to send output data on an optical link of higher bandwidth.
Figure 5. Top-side pictures of the original CFEB (left) and the replacement DCFEB (right).

Figure 6. The queuing model applied to CFEB (left curve) and DCFEB (right curve) with ME2/1 rates to confirm acceptable performance well beyond HL-LHC conditions.
Table 1. The expected per-chamber data rates in the stations where the electronics will be upgraded. The first row shows the projected rates for only the DCFEB data. The second row shows the rate also including the ALCT and OTMB data.

| Station | ME1/1 | ME2/1 | ME3/1 | ME4/1 |
|---------|-------|-------|-------|-------|
| ODMB Rate (DCFEBs) | 6.1 Gbps | 3.3 Gbps | 2.2 Gbps | 2.2 Gbps |
| ODMB Rate (total) | 10.0 Gbps | 5.4 Gbps | 3.7 Gbps | 3.5 Gbps |

4 Data path upgrades

The data transmission bandwidth will be heavily affected by the increase in trigger rate during the HL-LHC era. The expected HL-LHC data rates are presented in table 1. The minimum link bandwidth required is 10 Gbps, but a bandwidth of up to 20 Gbps would give a desirable safety margin. The DMBs must be replaced with a modified version of the Optical DAQ Motherboard (ODMB) to be able to support the optical signal from the new DCFEBs and the optical links to the FED system must also be upgraded. Currently the DMBs receive data from the DCFEBs through copper links, and send data to the FED via a 1 Gbps optical link. This would require replacing at least some of the optical receivers in the FED system, but it is foreseen to replace the entire VME-based FED system with a new μTCA or ATCA system and all of the receivers will be upgraded in the process.

5 Installation schedule

These upgrades are planned to be installed at different times depending on the location within the experiment. Sufficient access time for removal, refurbishment, and reinstallation of the on-chamber electronics is only possible during the second LHC Long Shutdown period (LS2) currently planned for 2019-2020, so upgrades of the CFEBs and ALCTs on the ME2/1, ME3/1 and ME4/1 chambers will be performed then. Upgrades of ALCTs on the remaining chambers and of the rest of the back-end system will be performed during the third LHC Long Shutdown period (LS3) currently planned for 2023-2024.

6 Future studies

Current efforts are focused on understanding how increasing background doses and rates at HL-LHC will affect chamber longevity, readout electronics, trigger algorithms, and offline muon reconstruction. The new Gamma Irradiation Facility (GIF++) facility at CERN utilizes a 14 TBq Cs-137 source to simulate effects of increased neutron backgrounds at HL-LHC and a muon beam to check performance. Figure 7 is a display of an event recorded by one CSC irradiated at GIF+++ with a muon and several background hits from gammas. This illustrates how challenging recognizing muon hits will be in the HL-LHC environment. Chamber aging studies are the main goal of the program at GIF++. All of these studies and developments are part of the CMS Phase II muon upgrade program, which will be detailed in a Technical Design Report to be published at the end of 2017.
Figure 7. An event display, from GIF++ data, with a muon track and additional hits due to background gammas. The grey area in the Strip Hit display appears for CFEBs which did not pretrigger, and therefore were zero-suppressed.

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