Design Techniques for High-Efficiency Envelope-Tracking Supply Modulator for 5th Generation Communication

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Abstract—This brief provides a brief tutorial on designing a high efficiency envelope-tracking supply modulator with recent techniques. Design challenges for 5G communication applications are given. Detailed techniques covering topology derivation, multi-level and fast-speed switching converter design considerations, voltage step-up and -down function implementations, linear amplifier bandwidth improvements and measurement setup are discussed, providing design guidelines and considerations.

Index Terms—Envelope tracking, supply modulator, power amplifier, 5G communication.

I. INTRODUCTION

THE 5TH generation (5G) mobile communication is developing rapidly over the world. The 5G New Radio (NR) in the sub-6GHz frequency band enables up to 100/200 MHz signal bandwidth, which is much faster than 4G long-term-evolution (LTE) communication with 20/40/60 MHz bandwidth. With the much higher wireless data rate, future applications, such as auto-pilot with car communication, long-distance surgery, and industry Internet-of-Things (IoT) will come to fruition. However, 5G communication also features a higher peak-to-average power ratio (PAPR) around 10 dB, which significantly reduces the radio-frequency (RF) power amplifiers (PA) efficiency to below 10%. Such a low efficiency brings high power consumption that will significantly reduce the battery run time and cause thermal issues. Therefore, it is essential to solve this critical efficiency problem.

A PA system is mainly composed of the PA and its supply modulator (SM) that supplies the PA. As shown in Fig. 1(a), the input RF signal of the PA has a changing magnitude. If the SM provides a constant supply voltage, the energy due to the dropout voltage between the supply and the envelope is wasted. Dynamic power supply technology, such as envelope tracking (ET) as shown in Fig. 1(b), has been proposed to improve the efficiency of PAs by adapting the PA’s supply voltage with RF envelope signal. For ET, the SM tracks the instantaneous changes in the envelope. Thus to keep a decent voltage profile after tracking, the SM bandwidth is required to be higher than the signal being tracked. The overall PA system efficiency is the PA efficiency times the SM efficiency. A well-designed SM could boost the overall efficiency to around 40% [1]. Moreover, in 5G communication, the RF PA has a more stringent linearity requirement. ETSM would reduce the AM-PM distortion and help with the linearity.

The requirements on the ETSM for 5G NR are extremely challenging. First, the envelope bandwidth is 2—5 times the signal bandwidth. To ensure the linearity of PA, the bandwidth of ETSM needs to be higher than twice of the envelope bandwidth, which is around 1 GHz. Second, the PAPR is increased from 3.4 dB to 10 dB, which means that the dynamic range of the envelope is also increased significantly. Typically, the envelope could be changing from 0.5 V to 6 V in nanoseconds. Third, the required instantaneous maximum output power of SM is about 10 W [2]. Thus, it becomes a great challenge for ETSM to achieve an efficiency higher than 80%, a bandwidth around 1 GHz, an output voltage ranges from sub-1V up to 6 V, and an output power around a couple of Watts, all at the same time.

To solve the aforementioned design challenges, research groups over the world have proposed many design techniques. With those techniques, optimized design can be achieved with a better tradeoff between efficiency, bandwidth, voltage range, and output power. In this tutorial brief, we would...
like to provide a system-level guideline of state-of-the-art techniques of ETSM designs. We are going to discuss in the following four dimensions, covering the innovations and important design considerations on the topology, the design of switching converters in terms of multi-level implementation and control method for fast speed, the implementation of step-up-and-down functions, the linear amplifiers bandwidth extension, as well as providing detailed guidelines on performing measurements.

II. TECHNIQUES ON HYBRID TOPOLOGIES

To increase the tracking bandwidth without sacrificing efficiency, a hybrid topology of using a linear amplifier to assist a switching converter, as shown in Fig. 2(a), was proposed by Wang et al. in 2007 [3]. It was improved by later arts for more advanced communication protocols [1]–[23]. The choice of the topologies is the first and most important step of the supply modulator design.

A. Hybrid Topologies of Linear Amplifier Assisting Switching Converter and the Limitations

The main idea is to track the fast-changing envelope with a wideband linear Class-AB amplifier while a switching converter senses the linear amplifier output current (i_d) and amplifies it to the switching converter current (i_a). In this way, i_a is regulated to a minimal value. Assume that the efficiency and output power of the switching converter and linear amplifier are $\eta_d$, $P_{od}$ and $\eta_a$, $P_{oa}$ respectively. And the ratios of them can be written as:

$$\frac{i_d}{i_a} = \alpha \quad \text{and} \quad \frac{P_{od}}{P_{oa}} = \beta.$$ (1)

In the frequency range, $\alpha$ and $\beta$ both have high gain at low frequency and low gain at high frequency. Thus, the linear amplifier with low efficiency provides the high-frequency power, while the switching converter with high efficiency provides the low-frequency power. Since most of the power is distributed within the signal bandwidth, the hybrid topology can still have comparatively high efficiency.

With the stringent requirements of 5G communication, this basic hybrid topology can no longer provide a decent efficiency. The efficiency of the supply modulator can be expressed as

$$\eta = \frac{P_{od} + P_{oa}}{P_{od}/\eta_d + P_{oa}/\eta_a} = \frac{1}{\frac{1}{\eta_d} + \frac{\beta}{\eta_a} + \frac{\beta}{\eta_d}}.$$ (2)

To improve the efficiency, we need to first increase both $\eta_a$ and $\eta_d$, then increase the portion of the power provided by the switching converter over the frequency span (increase $\beta$).

In 5G communication, higher voltage is required to achieve higher power and wider dynamic range, so the switching converter can only adopt high-voltage or stacked-low-voltage devices in its power stage. With those devices, obtaining high efficiency at high switching frequency is difficult because the switching loss will be dominant at high frequency. This means that the bandwidth of the switching converter is limited, forcing the linear amplifier to provide more portion of total power at higher 5G bandwidth, thus reducing the overall efficiency.

B. AC-Coupling Topology

To increase the efficiency of the linear amplifier, an AC-coupling topology as shown in Fig. 2(b) are proposed [4]–[7]. An AC-coupling capacitor C_{AC} is added between the outputs of the linear amplifier (V_{LA}) and the switching converter (V_{PA}), isolating V_{LA} from V_{PA} in DC. V_{LA} now only provides AC current to V_{PA}. The output voltage of the linear amplifier V_{LA} is lower than V_{PA}, and in this way the supply voltage of the linear amplifier V_{DDL} can be reduced, hence reducing the power consumption of the linear amplifier.

To further increase the efficiency, a hybrid topology of a fast buck and a slow buck is proposed in [5]. The low-efficient linear amplifier is replaced by a moderate-efficient 3-level buck converter. To track the fast envelope, it switches at 80 MHz. The 3-level power stage stacks low-voltage devices, so it has a lower switching loss than traditional 2-level buck to maintain a reasonable efficiency at high switching frequency. It also features a lower inductor current ripple and output voltage ripple to avoid large switching noise at V_{PA}.

However, to fulfill 5G requirements (e.g., a high bandwidth around 1 GHz, a large output voltage range from sub-1V up to 6 V, and a power deliverability of several Watts), the fast 3-level converter needs to work at more than 1 GHz, which will deteriorate the efficiency and introduce issues related to the switching noise. Another improved hybrid topology consisting of a fast buck, a slow buck and a linear amplifier was proposed [8] to support 5G NR-100MHz communication as shown in Fig 3. The high-efficiency slow buck still provides the low-frequency power while the moderate-efficiency fast buck provides the mid-frequency power and the linear amplifier only provides the very high-frequency power. To divide the power between the fast buck and the linear amplifier, a feed-forward envelope signal is applied to the fast buck to increase its response speed. To avoid the currents from the fast buck and linear amplifier running in opposite directions, the linear amplifier current is also fed back to the fast buck. The current from the fast buck has some gain over the linear amplifier current so it can help minimize i_a. By doing so,
the mid-to-high frequency power is well distributed between the fast buck and the linear amplifier, enabling linear amplifier provide less power, and improve the overall efficiency. As a result, this topology achieved a better tradeoff between efficiency, bandwidth and noise.

### III. Switching Converter Implementations

#### A. Multi-Level Power Stages

To support higher voltage, using stacked-low-voltage devices in advanced technologies such as 65 nm and beyond can be more efficient than thick-oxide devices, e.g., LDMOS or IO devices, due to the much smaller switching loss. For example, in 65 nm, the area can be reduced to \( \sim 25\% \) by using stacked devices [24], [27], which can significantly reduce the switching losses to work at higher frequency. It becomes even more beneficial at more advanced technologies as the minimum length of core devices scale much more than their rated voltage.

Another benefit of using multi-level power stages is because of the smaller voltage swing and higher equivalent switching frequency. With a 3-level power stage, the switching node swinging is \( \frac{1}{2} V_{DD} \) instead of \( V_{DD} \) of a 2-level buck converter. With the equivalently doubled frequency, the inductor current ripple is reduced to \( \frac{1}{8} \) [24], which can reduce the conduction loss with smaller root-mean-square current. Or on the contrary, a smaller power inductor can be used to improve large-signal response or power density.

However, multi-level converters have their own concerns. First, take a 3-level topology for example, due to timing mismatches, parasitics, and power consumption to drive the two stacked transistors, the \( C_{FLY} \) will be derived from \( \frac{1}{2} V_{DD} \) and needs to be well balanced. Otherwise, not only the inductor current ripple will increase, but there will be over-voltage stress on the power transistors. The \( C_{FLY} \) balancing can be done via a calibration loop to adjust the duty-cycle [25], or as part of the hysteretic control (to be discussed in the next section). Second, the system complexity is increased, as each stacked power transistor is switched individually and must be operating within its safety margin. Multiple floating domains will need to be carefully designed with ensured reliability, especially during startup or transients. Third, even if well balanced, the \( C_{FLY} \) needs to be carefully selected and implemented. Due to the periodical charging and discharging with inductor current, the \( C_{FLY} \) may have a large ripple, especially considering equivalent series inductance (ESL) and equivalent series resistance (ESR) and at high-current and fast-switching operations. These ripples will create extra voltage stresses on the stacked power transistors, and could become a major limitation to increase the power capacity and switching frequency. To reduce the ripple and ensure long-term reliability, extra voltage margin may need to be reserved; \( C_{FLY} \) needs to be large enough [10]; and more advanced low-inductance packaging techniques, such as SMD-on-Chip [26], together with low-ESL and low-ESR SMD capacitors, can be used.

#### B. Closed-Loop Control for Multi-Level Converters

A faster switching converter can better offload the power from the linear amplifier for a higher system efficiency. For a switching converter, the speed is generally limited by small-signal bandwidth and large-signal response.

Linear control techniques such as voltage- or current-mode PWM control have small-signal bandwidth limitations, which is \( \sim 1/3 \) of the switching frequency when well optimized. However, system stability considering significant variations in LC components, loading currents, and process, voltage and temperature (PVT) conditions, is always a concern. As a result, the small-signal bandwidth will be further compromised. For multi-level converters, the same control-to-output transfer function as a 2-level buck converter has been derived in [27], [28]. With higher equivalent switching frequency and the ability to adjust duty-cycle in shorter intervals, the small-signal bandwidth could be slightly relaxed compared to a 2-level converter.

Even if the control loop is fast enough to saturate the inductor charging or discharging slope at full thrust, the dynamic speed is still limited by large-signal LC responses. The smaller the LC, the faster the inductor current and output voltage will be able to be charged or discharged. As a result, switching at a higher frequency will not only relax the small-signal bandwidth, but also enables the use of smaller LC to improve the large-signal response while maintaining an acceptable voltage ripple. The component form-factor and power density can also benefit from higher switching, however, higher switching losses thus efficiency degradation is one of the major trade-offs. Higher frequency operation also brings challenges in the controller design because of circuit delays, and requires extra efforts to function properly, for example, by designing delay-free logic [29], or replacing the traditional time-based ramp-cutting PWM controller with voltage-controlled delay line [30].

Nonlinear control techniques, such as hysteretic control [10], [16], do not have small-signal limitations, so the response can be much faster. A voltage-mode controlled 3-level converter has been proposed in [16]. As shown in Fig. 4 (a), a 3-level converter has 4 different states (S1-S4). In a linear PWM-controlled 3-level converter, the states will rotate between \( S_1-S_2-S_3-S_4 \) for a voltage conversion ratio (VCR) larger than 0.5, and \( S_2-S_1-S_2-S_3 \) for VCR<0.5, respectively, and the transition between the VCR>0.5 and VCR<0.5 modes can be automatically achieved. However, for non-linear control, the decisions to choose among the four states are not straight-forward and can be described as follows. First, the four states can be classified into two categories: the charging and discharging of the inductor, and the charging and discharging of the \( C_{FLY} \). Then, if VCR<0.5, the switching node \( V_X \) will be switched between \( \frac{1}{2} V_{DD} \) and \( V_{DD} \). If the \( V_{O}<V_{REF} \), the inductor should be charged and \( V_X =V_1 \), which only \( S_2 \) can achieve. If the \( V_{O}>V_{REF} \), the inductor should be discharged, and \( V_X =\frac{1}{2} V_{DD} \). Both \( S_1 \) and \( S_3 \) satisfy this condition, so whether to work in \( S_1 \) or \( S_3 \) will be determined by the \( C_{FLY} \) balancing. If the \( C_{FLY} \) differential voltage \( V_{CF} \) is smaller than \( \frac{1}{2} V_{DD} \), \( C_{FLY} \) will be charged, thus \( S_1 \) should be chosen; otherwise \( S_3 \) will be chosen. A similar approach can apply for the VCR<0.5 condition. By listing the operation states versus different conditions in a truth table as in Fig. 4 (b), control logic can be designed to regulate \( V_O \) to \( V_{REF} \) by charging or discharging the inductor, and regulate the voltage of \( C_{FLY} \) \( (V_{CF}) \) to \( \frac{1}{2} V_{DD} \) by charging or discharging \( C_{FLY} \).

### IV. Voltage Step-Up and Step-Down Functionalities

To achieve a high efficiency and a compact system size, most of the supply modulators are designed to be directly
The four operation states of a 3-level buck converter. (b) Truth table for voltage-mode hysteretic control.

Fig. 5. Schematic of dual-power-line buck and the waveforms.

connected to a lithium-ion battery. The voltage of a lithium-ion battery can range from 2.5 V to 4.2 V with a typical value at 3.7 V. However, the output of the supply modulator can range from 0.5 V to 6 V for 5G applications. So the supply modulator is required to have both step-up and step-down functions dependent on the specific input and output voltages.

In the AC-coupling topology in [4], the supply voltages for the linear amplifier and the switching converter are $V_{BAT}$, but it can provide an instantaneous higher output voltage due to the voltage boosted up by the AC-coupling capacitor. However, the higher-than-$V_{BAT}$ voltage cannot maintain for a long time as the inductor current is going to decrease with the switching node $V_X$ lower than the output voltage $V_{PA}$, then the linear amplifier would not have enough current ability to support the output. Moreover, the maximum output voltage is still limited to $V_{BAT} + V_{AC}$ and would not be able to cover the full input and output voltage ranges. In [5], the switching converter is a buck-boost converter instead of the traditional buck converter while the linear amplifier is still powered by the battery and relies on the voltage boosted up by the AC-coupling capacitor.

In later arts, a buck-boost (BB) converter is usually included in the SM to generate a stable and high voltage $V_{BB}$ as the supply for the switching converter and linear amplifier with enough headroom to generate the maximum $V_{PA}$ [17], [18]. The buck-boost was cascaded with a buck converter rather than directly use the buck-boost as the switching converter because a buck-boost has slow response with a right-half-plane (RHP) zero. With the additional higher-than-battery voltage $V_{BB}$, dual-power-line (DPL) buck converter is proposed in [17] and [18] as shown in Fig. 5. When $V_{PA}$ is lower than $V_{BAT}$, it switches between $V_{BAT}$ and ground like a typical buck converter. When $V_{PA}$ is higher than $V_{BAT}$, it switches between $V_{BB}$ and $V_{BAT}$ (return to battery, R2B) instead of ground (return to ground, R2G). R2B has better efficiency and less noise compared to R2G. First, $V_{BB}$ is generated from $V_{BAT}$ with some power loss. At the same output voltage, with R2B, the voltage level at switching node is between $V_{BAT}$ and $V_{BB}$, which is higher than that of R2G, so it switches to $V_{BB}$ for less time and for the rest of the time it draws current from $V_{BAT}$ directly. Thus, better efficiency can be achieved. Second, the voltage swing at switching node is smaller ($V_{BB} - V_{BAT}$) instead of ($V_{BB} - GND$). This also helps reduce noise.

While enjoying all the benefits, the body-bias switch of the PMOS connecting $V_{BAT}$ needs to be carefully handled. When the DPL buck switches between $V_{BAT}$ and GND, the body of the PMOS should be connected to $V_{BAT}$, so the body diode is pointing from $V_{SW}$ to $V_{BAT}$ in case of conducting negative inductor current during the dead time. In the other case, when it switches between $V_{BB}$ and $V_{BAT}$, the body should be connected to $V_{BB}$, which is the highest the voltage, and the body diode is pointing from $V_{BAT}$ to $V_{SW}$ to conduct current during the dead time. It is challenging that the body-bias switch must be fast and precisely synchronized with the gate driving signal.

The DPL buck has 2 major advantages compared with traditional buck. However, when looking at the bigger picture of the SM, with a buck-boost converter cascading a DPL buck converter, compared with a single-stage converter, the overall efficiency will be degraded and the cost and volume will be higher. To overcome those limitations, a single-stage novel buck-boost converter without RHZ is proposed in [19]. By adding a flying capacitor, the switching node can change between GND, $V_{BAT}$ and 2$V_{BAT}$. A step-up function is thus implemented and at the same time the dynamics are similar to a traditional buck converter. In latest art [2], the novel BB is directly used as the switching converter and a micro-BB only supplies the linear amplifier with much smaller current ratings.

V. WIDE-BANDWIDTH LINEAR AMPLIFIER

A. General Concept

The most commonly used linear amplifier design is shown in Fig. 6. It consists of a high-gain OTA stage as the first stage, in which a class AB bias is merged, an output stage as the second stage, and a feedback network. The class AB bias is used to eliminate the cross-over distortions. The loading of the supply modulator is a PA in parallel with a high-frequency capacitor of around 100 pF to filter out the high-frequency
TABLE I
COMPARISON OF DIFFERENT STRATEGIES IN STATE-OF-THE-ART ET WORKS

| Efficiency | AC-Coupling Topology [4-7] | Multi-Level Power Stage [6, 10] | Non-Linear Control for SW Converter [16] | Buck-Boost with DPL Buck [17], [18] | Hybrid Buck-Boost [2], [19] | Core Device & Buffer [8], [17] |
|------------|-----------------------------|---------------------------------|------------------------------------------|------------------------------------|-----------------------------|-----------------------------|
| Linear     | ✓                           | -                               | -                                        | -                                  | -                           | -                           |
| Switching  | -                           | ✓                               | -                                        | -                                  | -                           | ×                           |
| Linear Amplifier Bandwidth | -               | -                               | -                                        | -                                  | -                           | ✓                           |
| Switching Converter Response | -               | ✓                               | -                                        | -                                  | -                           | -                           |
| Voltage Step-Up &-Down | -               | -                               | -                                        | -                                  | -                           | -                           |
| Chip Area  | -                           | x                               | -                                        | -                                  | -                           | -                           |
| External Components | x              | ✓                               | -                                        | -                                  | -                           | -                           |
| Complexity | x                           | x                               | ✓                                        | ✓                                  | ✓                           | -                           |

✓ means beneficial; × means non-beneficial; – means not relevant.

Fig. 6. Schematic of linear amplifier.

Fig. 7. (a) Core device with cascode I/O device configuration; (b) Wideband voltage-buffer-compensated linear amplifier with passive zero compensation.

ripples of the PA. For basic analysis, PA can be modeled as a constant resistor in the range of several ohms.

When the loop is closed, it is vital to know the pole-zero locations in frequency analysis. The dominant pole $p_1$ is at the gate of the output transistor. Since $C_{AC}$ is larger than 1 $\mu$F, it can be approximated as a wire shorting $V_{LA}$ and $V_{PA}$ in linear amplifier frequency discussions. The output pole $p_2$ generated from $R_L$ and $C_L$ is around 100 MHz, which is close or even smaller than the required UGF. For 4G application, the required UGF is around 100 MHz and miller compensation was adopted to separate $p_1$ and $p_2$. For the rest of the circuits, to provide high transconductance, the input pairs have a large size, which brings large input capacitance and forms a pole with the feedback resistors. The input pole can be canceled by the feed-forward capacitor $C_{C}$. The first stage usually has a high-frequency parasitic pole, which can be pushed to high frequency with reasonable circuit design.

B. Methods to Extend the Bandwidth

For 5G communication, with AC-coupling topology, the linear amplifier is required to provide up to 5V output with around 1 GHz UGF. To achieve such wide bandwidth, core devices with small parasitic capacitances are adopted for the signal paths. To sustain the high voltage, I/O devices are stacked to protect the core devices [17]. Even with core devices, the pole at the gate of the power transistor is still around 100 MHz. Considering the output pole, 1-GHz UGF cannot be achieved by miller compensation.

To extend the bandwidth, voltage buffer plus passive-zero compensation was proposed in [8] as shown in Fig. 7. A voltage buffer has low input capacitance and low output resistance. It is inserted between the first stage and the second output stage to push $p_1$ to frequency higher than UGF. Then a passive-zero network in front of the voltage buffer is employed to cancel $p_2$ by generating a zero at $1/R_{ZC}$. The dominant pole now becomes $1/R_{O1CZ}$. With a DC gain of $G_{m1}R_{O1}G_{mL}R_L$, the UGF is at $G_{m1}G_{mL}R_L/CZ$ and can be wider than $p_1$ and $p_2$. Wide bandwidth can thus be achieved at the cost of higher current consumption in the voltage buffer.

VI. MEASUREMENT GUIDELINES

Measurement setups for ET system are typically complicated. Fig. 8 shows an example of such a measurement setup [31]. The Keysight N7614B signal studio software is used to generate both the envelope and RF signals. It also provides timing alignment and digital pre-distortion (DPD) functions. The RF data is sent to a vector signal generator, such as Keysight N5172B, which generates the PA’s input RF signal. At the same time, the studio sends the respective envelope data to an arbitrary waveform generator, such as Keysight 33622A, which provides the envelope signal to the ETSM.

The PA’s output is then measured with a vector signal analyzer to observe its output power and linearity performance and the results are sent back to the studio. The waveform generator, the vector signal generator and the vector signal analyzer are synchronized and refer to the same 10-MHz clock to make
sure of the same base frequency. The timing between the envelope path and the RF path must be strictly aligned for best performance. A rough timing delay between the two paths is first obtained by observing the envelope and RF signals in an oscilloscope. Then the precise alignment can be done by the N7614B automatically as it can adjust the delay in steps of picoseconds and at the same time monitor the results from the vector signal analyzer. After time alignment is done, DPD can be enabled in the N7614B to achieve the best PA performance. For the PCB design, PA and supply modulator are closely placed and wire-bonded in the same PCB, and a very short connection between them needs to be guaranteed.

VII. CONCLUSION

This tutorial brief describes the state-of-the-art design techniques as listed in Table I to address the challenges in high-efficiency supply modulators for 5G communications. Design considerations including topology selection and derivation, multi-level switching converter implementation, linear and non-linear controls for fast dynamic response, voltage step-up-and-down functions and wide-bandwidth linear amplifier frequency compensations are discussed. Circuit techniques are presented and practical design and measurement guidelines are suggested.

REFERENCES

[1] M. Hassan, P. M. Asbeck, and L. E. Larson, “A CMOS dual-switching power-supply modulator with 8% efficiency improvement for 20MHz LTE Envelope Tracking RF power amplifiers,” in Proc. IEEE Int. Solid-State Circ. Conf. (ISSCC), Feb. 2019, pp. 238–240.

[2] S.-C. Lee et al., “A hybrid supply modulator with 10dB ET operation dynamic range achieving a PAE of 42.6% at 27.0dBm PA output power,” in Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC), Feb. 2015, pp. 1–3.

[3] S. Sung et al., “86.55% peak efficiency envelope modulator for 1.5 W 10 MHz LTE PA without AC coupling capacitor,” in Proc. IEEE Symp. VLSI Circuits, Jun. 2015, pp. C342–C343.

[4] J. S. Paek et al., “A –137 dBmHz noise, 82% efficiency AC-coupled hybrid supply modulator with integrated buck-boost converter,” IEEE J. Solid-State Circuits, vol. 51, no. 11, pp. 2757–2768, Nov. 2016.

[5] M. Hassan, L. E. Larson, V. W. Leung, and P. M. Asbeck, “A combined series-parallel hybrid envelope amplifier for envelope tracking mobile terminal RF power amplifier applications,” IEEE J. Solid-State Circuits, vol. 47, no. 5, pp. 1185–1198, May 2012.

[6] P. Mahmoudidaryan, D. Mandal, B. Bakkaloglu, and S. Kiaei, “A 91%-Efficiency envelope-tracking modulator using hysteresis-controlled three-level switching regulator and slew-rate-enhanced linear amplifier for LTE-80MHz applications,” in Proc. IEEE Int. Solid-State Circ. Conf. (ISSCC), Feb. 2019, pp. 428–430.

[7] C.-Y. Ho et al., “An 87.1% efficiency RF-PA envelope-tracking modulator for 80MHz LTE-Advanced transmitter and 31dBm PA output power for HPUE in 0.153μm CMOS,” in Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC), Feb. 2018, pp. 432–434.

[8] T. Nomiyama et al., “A 2TX supply modulator for envelope-tracking power amplifier supporting intra- and inter-band uplink carrier aggregation and power class-2 high-power user equipment,” in Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC), Feb. 2018, pp. 434–436.

[9] J. Baek et al., “A voltage-tolerant three-level buck-boost DC-DC converter with continuous transfer current and flying capacitor soft charger achieving 96.8% power efficiency and 0.87μs/V DVS rate,” in Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC), Feb. 2020, pp. 202–204.

[10] M. Tan and W.-H. Ki, “A 100 MHz hybrid supply modulator with ripple-current-based PWM control,” IEEE J. Solid-State Circuits, vol. 52, no. 2, pp. 569–578, Feb. 2017.

[11] S.-H. Yang et al., “A single-inductor dual-output converter with linear-amplifier-driven cross regulation for prioritized energy-distribution control of envelope-tracking supply modulator,” in Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC), Feb. 2017, pp. 36–37.

[12] W. Leng et al., “Envelope tracking supply modulator with trellis-search-based switching and 160MHz capability,” IEEE J. Solid-State Circuits, vol. 57, no. 3, pp. 719–733, Mar. 2022.

[13] Y.-T. Hsu, Z.-Y. Lin, J.-J. Lee, and K.-H. Chen, “An envelope tracking supply modulator utilizing a GaN-based integrated four-phase switching converter and average power-tracking-based switch sizing with 85.7% efficiency for 5G NR power amplifier,” IEEE J. Solid-State Circuits, vol. 56, no. 10, pp. 3167–3176, Oct. 2021.

[14] X. Liu, C. Huang, and P. K. T. Mok, “A high-frequency three-level buck converter with real-time calibration and wide output range for fast-DVS,” IEEE J. Solid-State Circuits, vol. 53, no. 2, pp. 582–595, Feb. 2018.

[15] X. Liu, C. Huang, and P. K. T. Mok, “A 50MHz 5W 3V 90% efficiency 3-level buck converter with real-time calibration and wide output range for fast-DVS in 65nm CMOS,” in Proc. IEEE Symp. VLSI Circuits (VLSIC), Jun. 2016, pp. 1–2.

[16] Z. Xia and J. Stauth, “A two-stage cascaded hybrid switched-capacitor DC-DC converter with 96.9% peak efficiency tolerating 0.6V/μs input slew rate during startup,” in Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC), Feb. 2021, pp. 256–258.

[17] X. Liu, C. Huang, and P. K. T. Mok, “Dynamic performance analysis of 3-level integrated buck converters,” in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), May 2015, pp. 2093–2096.

[18] X. Liu, P. K. T. Mok, J. Jiang, and W.-H. Ki, “Analysis and design considerations of integrated 3-level buck converters,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 63, no. 5, pp. 671–682, May 2016.

[19] C. Huang and P. K. T. Mok, “An 84.7% Efficiency 100MHz package bondwire-based fully integrated buck converter with precise DCM operation and enhanced light-load efficiency,” IEEE J. Solid-State Circuits, vol. 48, no. 11, pp. 2595–2607, Nov. 2013.

[20] Q. Huang, C. Zhan, and J. Burn, “A 30MHz voltage-mode buck converter using delay-line-based PWM control,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 65, no. 11, pp. 1659–1663, Nov. 2018.

[21] N7614B Signal Studio for Power Amplifier CDR, DPD and ET Test, Technical Overview, Keysight Technol., Santa Rosa, CA, USA, Aug. 2017.