Realization of a microelectrofluidic platform

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Abstract. We report on the development of a low cost, manufacturing process for a three-dimensional network, microelectrofluidic platform. The platform consists of multiple levels of fluidic channels and electrical circuits. The inter-level channels and circuits are connected through via holes and conductor-filled via holes respectively. The medium surrounding these channels and circuits is a polymeric material, in this case, PMMA. In this research, 2 separate chips have been made: a multi-layer fluidic network and a multi-layer electrical interconnect. The future goal would be to integrate both chips into one. The process involves the hot embossing of channels on thin sheets of PMMA and the deposition of metal circuits using the conductive paste printing technique. Both processes are low cost in terms of capital investment and in terms of raw materials used to make the chips. Backend processes include multi-layer bonding, via drilling, dicing and final assembly. A 4-layer fluidic network and a 4-layer electrical interconnect based on the PMMA substrate have been fabricated through a cheap and simple process. Testing shows fluidic and electrical transmission through the multi-layer chips.

1. Introduction

As the demand for microfluidic devices increases, there is a need for a low cost fabrication process that is capable of mass production. The earlier devices are mostly made of silicon, silicon oxide or glass partly due to the adoption of the MEMS fabrication processes. Structural integrity and dimensional control are very good when using both materials. Glass is also popular because its capillary and electroosmotic effects with water are strong. However, material and manufacturing cost is an issue when the chip is meant for single use. Hence, there has been a huge interest in the fabrication of microfluidic devices out of polymers in recent years. The availability of thick photoresists like the Microchem Su-8 and the Clariant AZ4620 has also been timely. Su-8 structures up to 1.2 millimetres thick and microfluidic devices fabricated out of Su-8 has been reported [1]. Another method used is the soft lithography of PDMS on an Su-8 mould. The cast PDMS can be sealed either with permanent bonding to another PDMS film or to a glass substrate [2]. Direct milling and laser machining [3] on polymers have also been reported. These processes are good for prototyping or small scale production. For mass production, replication technologies such as hot embossing and injection moulding would have to be used. Microfluidic devices can be classified into limited-function lab-on-chip (LOC) and micro total analysis system (μTAS). Most LOCs are single function and single layer devices such as mixers, separation channels, etc. Micro total analysis systems, on the other hand, are more complicated and can perform many functions such as mixing, reaction, separation, etc on a single chip. It can also consist of active valves and pumps to direct flow of fluids and metal electrodes for detection. As demand for more functions on chip increases, micro total analysis systems would become more common. Multi-layer devices consisting of channels,
metallization, components on every layer would be the answer to high performance, multi-functional, high density microfluidic chips.

2. Design

One chip for testing multi-layer fluidic channels was fabricated. It required 4 layers of PMMA stacked on top of one another. As shown in Fig. 1, fluidic channels were hot embossed on the bottom 3 layers while the top layer (Level 0) acted as a cover with inlet/outlet holes (1 mm in diameter) for the chip. Inter-level via holes also existed on the second (Level 1) and third (Level 2) layers. Figure 2 shows the design of the chip as seen from the top. As seen, channel 1 is located at level 1, channel 2 goes across levels 1 and 2, and channel 3 goes across levels 1, 2 and 3. Channel widths of 200 μm were used. Inter-level via holes were 0.5 mm in diameter.

A hybrid mould (or stamp) for hot embossing was fabricated based on FR4 material, a glass fibre reinforced epoxy in which printed circuit boards are commonly made of. The 1.6 mm thick FR4 has a layer of copper (~ 34 μm thick) on one surface. A pattern of raised structures from one of these copper surfaces was created using nickel electrolytic plating. A photo-sensitive film was used to act as a mask. Nickel plating was then conducted to fill up the trenches formed by the photo-sensitive film. The photo-sensitive film was then removed. Multiple moulds were created in one process with an FR4 sheet of 400 mm x 400 mm. The FR4 was then diced into individual moulds of 55 mm x 55 mm. Average roughness of the copper surface from profilometry is 0.4 μm. This is due to the topography of the underlying FR4 material. The average height of the nickel patterns is 38 μm. Figure 3 shows a typical profilometric scan across a nickel feature.
Figure 4 shows the design of the electrical interconnect chip. It also consists of 4 layers of PMMA. Three traces were designed. Trace 1 spans across levels 0 and 1, trace 2 spans across levels 0, 1, 2 and trace 3 spans across all levels. Inter-level traces were connected through vias filled with conductive paste. Six contact pads on level 0 were used for electrical testing.

3. Fabrication

The fabrication of the chips was a multi-step process based on polymer processing techniques. The main processes were hot embossing for the creation of channels in polymer substrates, and conductive paste printing to create electrical lines and to fill vias. This was followed by a few backend processes such as micro-drilling, dicing, thermal bonding and final assembly.

3.1. Fluidic network

All three layers of channel patterns would be created by the hot embossing process. The process is a polymer replication technology suitable for mass production. As illustrated in Fig. 5, the process consists of a stamp or mould (with positive and negative relief structures) that is pressed against a polymer substrate that has been heated to a temperature that is normally above the glass transition temperature of the polymer material. A holding time is necessary under heat and pressure to allow the
polymer to flow completely to form the patterns. Upon cooling down and separation of the stamp and polymer substrate, a reversed image of the stamp pattern would be imprinted on the polymer surface. The hot embossing machine used is a bench-top hydraulic press with a capacity of 15 tonnes load. It is fitted with two 100 mm diameter heated platens (top and bottom) and these are connected to a temperature controller. A thermocouple is embedded into one of the platens. Cooling is achieved through the air and through water cooled plates attached to the platens. A chiller circulates water through the two cooling plates. Typical heating and cooling rates are 10 °C/min. and 5 °C/min. respectively. The substrate used is a commercially available 1 mm thick PMMA sheet. The material is optically clear with an average surface roughness of 0.02 \( \mu \)m. Dynamic mechanical analysis indicated the glass transition temperature to be \( \sim 110 \) °C. Thermal mechanical analysis on the sample showed an average thermal coefficient of expansion of \( 10^{-4}/K \). The hot embossing was carried out at 130 °C under 0.33 kg/mm\(^2\) pressure for 10 minutes and the sample was removed at 85 °C. Figure 6 shows a typical hot embossed channel. A 1 mm hole had been drilled at the location for an inter-level via. Complete flow of the PMMA around features on the mould was achieved. Feature dimensions (width and depth) were well replicated from the mould.

![Fig. 5 The hot embossing process.](image)

![Fig. 6 Scanning electron micrograph of a channel embossed in PMMA. A through hole had been drilled through the PMMA.](image)
After hot embossing, the PMMA substrates were diced to uniform shapes. The inlet/outlet holes and inter-level via holes were created on a router drill machine. It is a bench-top setup with CNC and machine vision alignment. Holes down to 0.2 mm can be drilled on the machine. In this research, inlet/outlet holes on the cover layer were 1 mm while inter-level via holes were 0.5 mm in diameter. As seen in Fig. 6, the hole is burr free and the positioning of hole is good to within 10 μm.

After the holes were drilled, the PMMA substrates were thermally bonded together using the hot embossing machine. More process control was required as compared to hot embossing of the channels. A surface treatment procedure was also required. Alignment between PMMA layers had to be carried out. Process parameters especially temperature had to be properly controlled since blockage and deformation of channels would pose problems. The bonding process developed was able to bond all 4 layers of PMMA in one step lasting 5 minutes without channel blockage and fluid leakage when tested.

3.2. Electrical interconnection
A stencil printer from MPM Corporation was used to create conductive traces on the PMMA sheets. A 325 mesh 15” x 15” metal screen was used. A photo process similar to photolithography was used to create the master patterns on the screen. All 4 layers of electrical design were created in one screen. The paste used is a low temperature cure silver-filled epoxy from Emerson & Cumming. Both electrical traces and inter-level vias were filled with this material. A layer by layer trace printing, via filling, thermal cure and bonding process was used.

4. Results and discussion
Figure 7(a) showed a bonded multi-layer fluidic chip. After thermal bonding the chip was fitted with inlet/outlets connectors (supplied by Nanoport) and was connected to tubing and a syringe. Tests revealed that fluid was able to pass all 4 layers of channels and vias without leakage. Figure 8 shows a cross-sectional scanning electron micrograph of a typical channel and fluid flow in a channel. As seen in Fig. 8(a), the channel was not blocked and the overall dimensions (width and depth) were maintained. However, the shape deviated from that of a rectangular cross section due to deformation especially at the corners. More process control of the bonding process would improve the situation.

Figure 7(b) showed a bonded multi-layer electrical interconnect chip. The traces were 200 μm in width and the vias were 1 mm in diameter. Separate printing tests using a test pattern showed that features down to 100 μm can also be printed. Electrical testing on the chip indicated connection through all the layers of the chip.

Fig. 7 Bonded multi-layer fluidic chip (a), bonded multi-layer electrical interconnect chip (b)
5. Conclusions

A 4 layer fluidic chip and a 4 layer electrical interconnect chip based on PMMA, were fabricated. Channels 200 μm in width and inter-level vias 500 μm in diameter were created using the hot embossing and micro-drilling processes. In the electrical chip, traces 200 μm in width and vias 1 mm in diameter were filled with silver epoxy using a printing technique. Fluidic and electrical tests indicated that both chips were working well. A simple, low cost fabrication process based on polymer processing was also developed. The process has a short cycle time suitable for mass production. This work will pave the way for more research to integrate both fluidic and electrical networks in one platform and to introduce functional components on the chip.

References

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