A Close Loop Low-Power and High Speed 130 nm CMOS Sample and Hold Circuit Based on Switched Capacitor for ADC Module

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Abstract. A sample and hold (S/H) block is typically used as an analogue to digital interface in the analogue to digital converter (ADC) system. Since ADC is widely used in processing signals, the power consumption of the ADC must be lowered to conserve energy. Therefore the S/H circuit must be of a low powered too. Sampling phase and hold phase are the two phases of the operation cycle of the S/H circuit. Switched capacitor (SC) techniques have been developed in order to allow the integration on a single silicon chip of both digital and analogue functions. By controlling switches around the SC, the SC circuit works by passing charge into and out of a capacitor. SC circuits are suitable for on chip implementations because they replace a resistor with switches and capacitors. In this research, a closed-loop sample and hold circuit based on SC is designed and simulated with Cadence EDA tools. The schematic, layout, and simulation of the circuit is done using generic Silterra 130 nm technology file. All the analysis is done using Virtuoso Analog Design Environment. Layout and schematic are drawn using Virtuoso Schematic Editor and Virtuoso Layout Editor, Calibre is used for post layout simulation. The closed loop S/H circuit based on SC is successfully designed and able to sample and hold the analogue input waveform. The power consumption of the circuit is 0.919 mW and the propagation delay is 64.96 ps.

1. Introduction

Signal processing plays a major role in many systems of on chip application. With the progress in complementary metal oxide semiconductor (CMOS) technology, analogue to digital converter (ADC) plays an important component for digital signal processing (DSP) because most signals in the natural world such as voltage, current, and voice are analogue [1]. Switched capacitor (SC) circuits are widely used in all signal processing and circuits due to their accurate parameters governed by capacitor ratio. Switched-capacitor circuits play a critical role especially in mixed signal and analog to digital interfaces. They implement a large class of functions, such as sampling, filtering and digitization. With increasing demand for high-resolution and high speed in data acquisition systems, the performance of a sample-and-hold (S/H) circuit is becoming more and more important. S/H circuit is required as the interface in a high speed ADCs to improve the ADCs performance [2]. The S/H circuit is used to sample an analog signal and store its value for a finite length of time. Hence, S/H circuit is a very important building blocks in data converter systems [3]. The use of the S/H circuit allows most dynamic errors of ADC’s to be reduced especially those occurring with high frequency input signals.
Therefore, the sample and hold circuit must exhibit a better performance than the ADC in terms of accuracy, speed, and power dissipation. This research embarks on designing of a low power and high speed sample and hold circuit with the aim of increasing the performance of a high speed ADCs.

Several SC S/H amplifiers had been designed by previous research. However the design was implemented in bigger CMOS technology (180 nm and above) [3, 5-11] and uses more than 1.5V power supply [2-3, 8-11]. However, not many are using 130 nm CMOS technology [12, 13]. The power consumption in all of these designs are considered high. Hence, this research is proposing a design of SC S/H circuit using 130 nm CMOS technology and utilizing a 1.5 V power supply with the aim of producing a SC S/H circuit with low power consumption and a very high speed. The total power is the summation of static power and dynamic power [14].

2. Close loop sample and hold based on series switched capacitor

Figure 1 shows a close loop S/H circuit with series switched-capacitor. The operation of the circuit is based on the transition of phases which are the sample phase and the hold phase. Basically, the sample phase is conducted when switches G1 and G2 are in on mode while G3 is in off mode. As for the hold phase it is vice versa. The operational amplifier in the circuit is used to control the unity gain of the output signal and close loop route to maintain the precision of the output signal.

However, turning off a transistor may introduce an error voltage in switched capacitor circuits. Circuits such as ADCs, digital to analog converters (DAC), and CMOS image sensor pixels are limited in performance due to the effects known as charge injection and clock feedthrough [15, 16]. The charge injection is due to discharge of the triode region of drain and source voltages point and the clock feedthrough is due to parasitic capacitances between source gate and drain gate. Both bring disturbance to the output signal in nonlinear form. To overcome this, series switched-capacitor is used in the close loop S/H circuit being designed. The charge injection error can be reduced greatly if the transistor is turned off in saturation instead of in triode region [17].

3. Methodology

The S/H circuit being designed in this research is a combination of current mirror (refer to Figure 2), operational amplifier (refer to Figure 3) and series switched-capacitor. The full-schematic design is illustrated in Figure 4. The circuit has several input and output ports. In this design, nMOS transistor is used as a switch to control charges and discharges of the capacitor. Figure 5 shows the switched signal of G1, G2 and G3. The time for charging and discharging is 0.01 ns and 0.05 ns respectively within the 0.06 ns period (T) of times. The hold or discharge time is longer than the sampling or charge time in order to minimize the clock feedthrough injected by parasitic capacitance.
Figure 2. Current sources schematic design

Figure 3. Amplifier schematic design
Figure 4. Full schematic design

Figure 5. Switched signal of G1, G2 and G3
Nyquist criterion for frequency sample and input frequency are being determined by (1). Nyquist rate are essential to avoid aliasing during sampling process.

\[ F_{\text{sample}} \geq 2 f_{\text{input}} \]  

(1)

The sample frequency is equal to \( 1/T = 1.67 \times 10^{10} \) Hz and input frequencies are varied from 1.0 GHz to 8.0 GHz. It is obtained that the minimum input frequency is at \( 1.0 \times 10^{10} \) Hz and the maximum input is \( 1.6 \times 10^{10} \) Hz. Through the given formula, as along as the input is not over than \( 1.67 \times 10^{10} \) Hz the sampling process will not be affected by aliasing.

4. Analysis and result of schematic design

The circuit in Figure 4 has been simulated and the result is discussed in this section.

4.1 Transient, DC and AC Analysis

For the simulation, the circuit was tested with the amplitude of the input signal varied from 1.5 V to 0.125 V. The input frequency is set at 1.25 GHz in sinusoidal waveform. The capacitor is set at 1 pF. By using Virtuoso Analog Design Environment, the DC and AC analysis were done several times along with the transient analysis. In order to have a result of smooth output with less error of charge injection and clock feedthrough, the input signal needs to be operated in saturation region. It is found the input with 0.5 V showed the best output result with merely smooth waveform and less parasitic signal interrupted as shown in Figure 6.

![Figure 6: The final result](image-url)
4.2 Static power and dynamic power
The total average power is the summation of static power and dynamic power. Equations (2) and (3) represent the equations for static power (Pstat) and dynamic power (Pdyn) respectively. Istat is the static current and Cl is the load capacitance.

\[ P_{\text{stat}} = I_{\text{stat}} \times V_{\text{dd}} \]  
\[ P_{\text{dyn}} = C_l \times V_{\text{dd}} \langle \text{averages} \rangle \times \text{frequency} \]

Table 1 shows the analysis of the static power for the components in the circuit. The total static power for the S/H circuit is 0.992 mW. The dynamic power for each component cannot be obtained because the input varies, however, the total dynamic power is -72.2 µW. The result obtained shown the S/H circuit is consuming less power.

| No | Name devices | Static Power (Watts) | Total Power (Watts) |
|----|--------------|----------------------|---------------------|
| 1  | In           | 1.270\times10^{-5}   | 6.452\times10^{-11}|
| 2  | Amplifier    | 9.790\times10^{-4}   | 9.199\times10^{-4}  |
| 3  | NMOS 1       | 1.971\times10^{-7}   | 7.377\times10^{-18} |
| 4  | NMOS 2       | 1.950\times10^{-7}   | 1.53\times10^{-18}  |
| 5  | NMOS 3       | 2.011\times10^{-15}  | 7.377\times10^{-18} |
|    | Total        | 9.921\times10^{-4}   | 9.199\times10^{-4}  |

5. DRC, LVS and PEX of layout design
The layout of the current mirror circuit, operational amplifier, series switched capacitor along with all other pMOS and nMOS transistors, capacitor and resistor which make up the whole circuit has been constructed. The full-layout design requires all the Silterra rule check in design rule check (DRC), layout versus schematic (LVS) and parasitic extraction (PEX) simulation to ensure the design is satisfactory conformed to the design requirement and circuit functionality before being fabricated [18].

Figure 7 shows the layout for the amplifier circuit along with the current source circuit. As shown in the figure, the layout for the resistor in the current source circuit occupies a large area as expected. The full-layout design for the S/H circuit is shown in Figure 8. In the figure, the layout for the capacitor takes the large area as compared to the rest of the circuit components. The full-layout is done using 130 nm technology, hence the total area taken is very small. For the layout design, the CALIBRE application tools of DRC, LVS and PEX have shown the layout design matched with the schematic design and obey the Silterra rules. Thus, the layout design is ready to be sent out to semiconductor manufacturer for fabrication.
Figure 7. The layout of amplifier circuit with current source

Figure 8. The S/H circuit full-layout
6. Result analysis

Table 2 shows the power consumption of the S/H circuit in this research and several other references. Although the technology files are different, still it can be said the power consumption of the circuit in this research is comparable to others. Thus it can be stated that the S/H circuit in this research has been designed successfully. It should be noted that this circuit is designed using a smaller technology file and less power supply that might contributed to the achievement.

Table 2. Power consumption

| Technology Files | Power Supply (V) | Power Consumption (mW) |
|------------------|------------------|------------------------|
| This research    | 130 nm           | 1.5                    | 0.92                   |
| [3]              | 180 nm           | 3.3                    | 11                     |
| [8]              | 180 nm           | 3.3                    | 20                     |
| [9]              | 180 nm           | 1.8                    | 61                     |
| [11]             | 180 nm           | 1.8                    | 6.5                    |

In order to measure the speed of the circuit, the differences between input and output transient time must be obtained. To get an effective propagation for the output signal, the input signal is set up to 1.6 GHz. Table 3 shows the result and the propagation delay for the S/H circuit in this research is found to be 64.96 ps. The delay can be considered very small and comparable to others even though some of the circuits are designed using different technology.

Table 3. Propagation Delay

| Technology Files | Power Supply (V) | Propagation Delay (ns) |
|------------------|------------------|------------------------|
| This research    | 130 nm           | 1.5                    | 0.064962               |
| [12]             | 130 nm           | 1.2                    | 5                      |
| [5]              | 90 nm            | 0.9                    | 10.212                 |
| [5]              | 180 nm           | 1.2                    | 10.232                 |

7. Conclusion

Based on the analysis of the designed circuit of the close loop S/H circuit, the output waveform produced are as expected and the circuit is able to sample and hold an analogue signal. The selected period of the switched-capacitor to charge and discharge is in reliable values and suitable in designing a S/H circuit. The current source circuit being designed is able to provide the right amount of current for the operational amplifier to operate close to unity mode. The total power consumption for the circuit is based on average power calculation of the power supply. In conclusion, the proposed S/H circuit which is designed in 130 nm CMOS technology using 1.5 V supply has been designed successfully. The power consumption is 0.919 mW and the propagation delay is 64.96 ps. The power consumption is considered low and the speed of the circuit is very fast.

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