Compact gate-based read-out of multiplexed quantum devices with a cryogenic CMOS active inductor

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(Dated: February 10, 2021)

In the strive for scalable quantum processors, significant effort is being devoted to the development of cryogenic classical hardware for the control and readout of a growing number of qubits. Here we report on a cryogenic circuit incorporating a CMOS-based active inductor enabling fast impedance measurements with a sensitivity of 10 aF and an input-referred noise of 3.7 aF/sqrt(Hz). This type of circuit is especially conceived for the readout of semiconductor spin qubits. As opposed to commonly used schemes based on dispersive rf reflectometry, which require mm-scale passive inductors, it allows for a markedly reduced footprint (50µm × 60µm), facilitating its integration in a scalable quantum-classical architecture. In addition, its active inductor results in a resonant circuit with tunable frequency and quality factor, enabling the optimization of readout sensitivity.

An ingenious use of the laws of quantum mechanics has led to a new computing paradigm, generally known as quantum computing, that promises exponential speed-up in the solution of certain types of problems. Using a prototypical quantum processor with 53 operational superconducting quantum bits (qubits), a ground-breaking experiment was recently able to perform a first experiment towards quantum supremacy, triggering more extensive research on such a goal. Practical implementations of quantum computing, however, are expected to require much larger numbers of physical qubits.

Solid-state implementations seem to offer the best scalability prospects. While superconducting qubits are currently the leading platform, semiconductor spin qubits are emerging as a serious contender owing to the possibility to leverage the integration capabilities of silicon technology. In both cases, the quantum processor can only function at very low temperature, typically below 0.1 K (only recently, it was shown that silicon qubits could be operated even above 1 K with limited loss of fidelity).

In a scale-up prospect toward increasingly large numbers of qubits, the introduction of classical cryogenic electronics positioned as close as possible to the qubits is widely considered as a necessity. Various solutions have been proposed and partly demonstrated to a first proof-of-concept level. These include low-temperature (de)multiplexers, analog-to-digital and digital-to-analog converters, low-noise amplifiers, RF oscillators, transimpedance amplifiers, and digital processors. In a DRAM-like strategy, these cryogenic components can significantly reduce the number of electrical lines running through the host cryostat, thereby limiting the associated heat load and increasing interconnect reliability. A CMOS-based cryogenic controller operating at 3K was recently reported enabling high-fidelity operations on an electron-spin two-qubit system. As far as qubit readout is concerned, however, relatively little has been done. Measuring the qubit state requires detecting small variations in the impedance of an LC tank circuit coupled to the qubit, which is commonly done through rf reflectometry. The inductive element of this tank circuit consists of a surface-mount inductor or a microfabricated superconducting coil. Even for this second case, the corresponding footprint is relatively large (~mm²) and hence hardly compatible with large-scale qubit integration.

Here we propose an alternative readout technique involving a cryogenic CMOS-based active inductor with a compact design. Besides its reduced footprint favoring scalability, this CMOS inductor offers the possibility to tune the characteristic frequency and the quality factor of the resonator, which is instrumental in optimizing measurement sensitivity. As opposed to conventional reflectometry, our method consists in measuring the tank impedance at resonance. The cryogenic read-out circuit is composed of a current source exciting the LC tank, an amplifier to read the voltage response, and a multiplexed capacitor bank to select different devices under test (DUT). We characterized the circuit sensitivity and tunability at 4.2 K demonstrating its capability to measure capacitances as low as 10 aF. By applying our technique to a gate-coupled MOSFET co-integrated on the same chip we reveal typical signatures of quantized electronic states.

I. IMPEDANCEMETRY

Capacitive spectroscopy of gate-controlled quantum-dot devices allows the detection of electronic quantum states within the structure, including the firstly occupied electron states. For enhanced detection sensitivity at high speed, the gate capacitance of the device under test (DUT), represented as a single-electron transistor in Figure 1b, is connected to an inductance to form an LC resonator. In a gate-coupled read-out scheme of the quantum state, the response of the tank at cryogenic temperature excited near resonance frequency is conveyed back to room temperature for probing and analysis, usually with homodyne I-Q detection. The phase of the tank response becomes an image of the change in DUT capacitance (see Figure 1a) through the relation $\phi = Q\Delta C/C_p$ around $f_r$ with $Q$ the resonator quality factor and $C_p$ the parallel capacitance.

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Figure 1. **Integration of measuring circuitry for scalable readout of quantum capacitance.** a, Schematic signals of the complex scattering coefficient $S_{11}$ and impedance $Z_{11}$ of a resonant circuit in, respectively, reflectometry and impedancemetry. b, Comparison between a typical reflectometry setup (left) and the proposed impedancemetry setup (right) for the measurement of the quantum capacitance $C_q$ of a single-electron transistor. Impedancemetry leverages cryogenic electronics to achieve higher integration of the measurement circuitry by getting rid of bulky directional couplers. Red (respectively green) arrows represent voltages (resp. currents). Red-green arrows emphasize the voltage-current interdependence due to signal propagation in 50Ω lines.

Figure 1b shows a schematic comparison for resonance experiments between the commonly used method of reflectometry and the here employed method of impedancemetry. Reflectometry uses voltages to excite and probe the resonator via the scattering or transmission parameters, based on propagating waves. To isolate the incoming and outgoing signals, directional couplers or circulators are used.

Impedancemetry uses currents to excite and probe the resonator via the impedance parameters without the need of bulky coupling elements. The incoming signal $V_{in}$ at the resonant frequency $f_r$, generated at room temperature, is converted in a current $I_{in} = G_m V_{in}$ with a voltage-controlled current source of transimpedance $G_m$ at the base-temperature stage. The input current $I_{in}$ creates a voltage $V_{out} = Z_{r} I_{in}$ through the tank impedance $Z_{r}$ that carries the information about the DUT capacitance. $V_{out}$ is conveyed to a low-power unity-gain amplifier (follower) placed nearby the DUT to reduce parasitic capacitance $C_{par}$. Main amplification is placed at a higher temperature (typically 4.2 K) to benefit from higher cooling power.

Impedancemetry has the advantage over reflectometry that the 50Ω impedance matching plays no role in the optimization of the resonant circuit depending on the inductor and the parasitic capacitors. However, the cryogenic circuitry required by impedancemetry generates extra noise compared to reflectometry, which needs to be minimized. The impedance of the resonator naturally filters out-of-resonance components (see Figure 1a) such as low-frequency flicker noise from electronics. In the perspective of quantum computing involving a qubit matrix, $V_{in}$ could contain a comb of excitation frequencies to excite a set of frequency-selective resonators (see Supplementary Material I with an estimation of the scaling for large qubit arrays).

In the case of impedancemetry, without the need of directional couplers, the footprint of the read-out circuitry is reduced. Using modern CMOS technologies with sub-100nm nodes, the additional circuitry of current sources and followers easily fits on a chip with size comparable to the hundreds of qubits chip (<mm$^2$) such that the total footprint is limited by the size of passive µH inductance occupying a few mm$^2$. The connection fan-out of a qubit matrix, originating from different-scale objects, increases the average interconnection length, thus lowers the detection sensitivity with important parasitic capacitance. The applied high magnetic field (∼1 T) required to separate spin states via the Zeeman effect prevents an effective use of ferrite materials for reducing the inductance size. Active inductances consisting of transistors and capacitors can reach an inductance density as high as a few mH/mm$^2$ which is 3 to 4 orders of magnitude higher than passive inductances (see Supplementary Material I for the scaling analysis). In the following, important issues of dissipation and noise of the realized active inductance will be treated in relation to sensitive capacitance detection.

**II. ACTIVE INDUCTANCE**

The active inductance behavior is realized by transforming a capacitor $C_q$ into an inductance $L = C_L/G_{m1} G_{m2}$ via two transistor devices of transimpedance $G_{m1}$ and $G_{m2}$ forming a gyrator. The non-ideal finite conductance and parasitic capacitance of the transistors set the resonant frequency $f_r$ and quality factor $Q$. More advanced active inductance architectures incorporate a negative resistor in parallel to the inductance in order to improve $Q$ up to a few hundred with independent tuning of the inductance value $L$ and the quality factor $Q$. Fine calibration of the tunable inductance value using variable capacitors leads to a precise definition of the resonant frequency value, ideal for optimal frequency-multiplexing of large qubit matrices. The tunability of the $Q$-factor enables different modes of read-out. High-$Q$ gives a precise measurement of quantum capacitance to calibrate qubit matrices. Lower-$Q$ is more suitable for fast read-out during quantum computation.
III. INTEGRATED CIRCUIT DESIGN

The impedancemeter circuitry was integrated on a single chip with multiplexed quantum devices using the Fully-Depleted Silicon-On-Insulator (FD-SOI) CMOS technology. The FD-SOI technology is very well suited for high-speed cryogenic applications\textsuperscript{29} with lower variability than bulk technologies\textsuperscript{30}, less sensitivity to carrier freeze-out, and threshold-voltage tuning with the use of the back-gate\textsuperscript{31}. The integration of classical circuitry with small-enough transistors that exhibit quantum properties is a plus to validate efficiently new circuit architectures\textsuperscript{16,19,32}.

The realized integrated circuit contains the current source, the active inductance with addressable capacitor banks for tunability, the multiplexed DUTs, and the amplification stage (Figure 2a, b). During design, we focused on bringing down the footprint and power consumption of the active inductance being the main original component of our circuit. The complete amplification and current generation was added on-chip to facilitate testing the concept of impedancemetry at 4 K. In the absence of high-frequency models of FD-SOI transistors at cryogenic temperatures, we designed the integrated circuit with accurate room-temperature models supplied by the foundry\textsuperscript{33}. The evolution of transistor characteristics towards the lowest temperatures was extrapolated from the temperature variation in foundry models but also from acquired 4.2 K data of single transistors\textsuperscript{30,31}.

The active inductance follows a known NMOS-based Karsilayan-Schaumann architecture\textsuperscript{34,35}. The gyrator is made of a single-ended negative transconductance $-G_{m,1}$ and a differential transconductance stage $G_{m,2}$. The gyrator transforms a tunable capacitance $C_L$ into an inductance $L(C_L) = C_L/G_{m,1}G_{m,2}$. An added metal-oxide-metal (MOM) capacitor $C_p$ of 136 fF parallel to $L$ controls the resonant frequency $f_r = 1/2\pi\sqrt{L/C_p}$. No dependence in temperature is expected for MOM capacitors\textsuperscript{36}. Adding $C_p$ makes the measuring circuit less sensitive to the DUT-capacitance with the increased tank capacitance but avoids the influence of unknown parasitic capacitances at cryogenic temperatures (e.g., substrate parasitics). Hence, the resonant frequency $f_r$ is set by $C_p, C_L$, and $G_{m,1,2}$. $C_L$ is implemented with one main metal-oxide-metal (MOM) capacitor of 362 fF in parallel with two digitally-controlled binary-weighted MOM capacitors of 68 and 136 fF (see Supplementary Material II). At room temperature, the emulated $L$ ranges from 5.3 to 8.4 fH to reach $f_r$ from 128 to 165 MHz (see Supplementary Material III). The estimated power consumption of the resonator is 85 mW and corresponds to a footprint of 8.5 fH/qubit assuming a $10 \times 10$ frequency-multiplexed array of qubits with frequency resolution of 5 MHz in a 1 GHz bandwidth.

Adding a capacitance $C_R$ at the foot of the differential transconductance stage allows to introduce a negative resistance in series with the active inductance, leading to higher $Q$-factor with an increased parallel effective resistance $R(C_R, C_L)$. The $Q$-factor of the active inductance defined as $Q = R(C_L, C_R) \sqrt{L(C_L)/C_p}$ depends on $C_R$ and $C_L$. By tuning $C_L$, then $C_R$, $L$ and $Q$ can be adjusted to any desired value apart from possible instabilities. To tune the $Q$ factor, we choose to cover a wide range of $C_R$ values in steps of 23 fF by selecting 4 binary-weighted MOM capacitors of 23, 46, 92, and 184 fF. From room-temperature simulations, these settings allow to cover a wide range of quality factors $Q$ from 7 to 300, including the unstable states with negative $Q$ (see Supplementary Material III).

The voltage-controlled current source exciting the resonator is made of a current mirror combined to an RC bias tee. The bias tee superimposes DC signals from the diode transistor to set the DC operating point of the current source and AC signals from the excitation input $V_{in}$ to generate the AC current $I_{in}$. The RC filter of the bias tee consists of $R_{bt}$ (polysilicon resistor of 10 MΩ) and $C_{bt}$ (MOM capacitor of 406 fF) to reach a characteristic frequency of 39 kHz. As no large signals $V_{in}$ are required, the current source operates in subthreshold regime with a bias current of only 0.1 µA to minimize its conductance for a negligible impact on the resonator and obtain a desirable low conductance for nA-current excitation. From foundry models, we get for the current generating transistor a transconductance $g_{m} = 3.4$ nA/mV and bandwidth of 3.5 GHz (see Supplementary Material III).

To investigate the active inductance circuit with different DUTs, we added an addressable bank of 6 capacitors. Three MOM capacitors of 2, 4, and 8 fF have the purpose of calibrating the active inductance on known values. Three additional MOSFETs (M0, M1, M2) of width 80 nm and length 28, 60, and 120 nm are used as test-bench for the investigation of quantum properties. The source and drain voltage of the quantum MOSFETs are grounded when unselected and polarized at $V_{bias}$ when selected. The differential transconductance stage of the active inductance copies the DC common-mode voltage $V_{cm}$ to the DUT gate potential, such that the DC gate voltage $V_{gs} = V_{cm} - V_{bias}$ can be varied via $V_{bias}$ (see Figure 2).

Once excited by $I_{in}$, the tank voltage is amplified, then sent through a unit-gain buffer for detection at room temperature via meter-long cable. The amplifier is a common-source N-type single-stage and the 1:1 buffer is a common-drain N-type single stage (see Figure 2a). Based on room-temperature simulations, the amplifier has a gain $A$ of 15 dB and a bandwidth of 1.8 GHz for a power consumption of 150 mW. The buffer reaches a bandwidth of 92 MHz for a cable capacitance of 50 pF and a power consumption of 2.4 mW. The net amplification at 165 MHz becomes 8 dB.

Transistor noise translates into transconductance noise that generates perturbing variations into the parameters determining the active inductance. A varying $L$ modulates $f_r$ and generates phase noise in $V_{out}$. The phase noise spectrum of $V_{out}$ around the carrier frequency $f_r$ extracted from room-temperature steady-state simulations (SST) exhibits a flicker component (see Supplementary Material III) on time-scale >10 ns, induced by a noisy modulated $L$. For a typical $Q$ of 81 with sufficiently fast measurements to avoid 1/f noise, we get a phase noise of 0.002 °/√Hz that gives an input-referred noise of 3.2 aF/√Hz.

Voltage excitation and homodyne detection are performed at room temperature with an all-digital lock-in amplifier (Figure 2c). Different configurations for single (I) and double
Figure 2. Setup with on-chip electronics. a, On-chip circuit implementation of the active inductance (pink), current excitation (green), test capacitor bank (blue), and amplification stage (red). For clarity, the bias MOSFETs operating in DC are drawn of smaller size than MOSFETs in the high-frequency signal chain. b, Simplified view of the on-chip resonant circuit placed at 4.2 K with tunable resonator, DUT, current excitation, and voltage amplification, linked to room-temperature phase-sensitive electronics via meter-long cables. c, Room-temperature homodyne detection with single (I) and double (II) demodulation of the circuit output $V_{out}$ and generation of voltage excitation $V_{in}$ at modulation frequencies $f_1$ (150-200 MHz) and $f_2$ (1 kHz).

(II a,b) demodulation are further described in the following section when needed.

IV. IMPEDANCEMETRY CIRCUIT CHARACTERIZATION

Without the assistance of low-temperature models, the operating point of the circuit had to be determined experimentally starting from room-temperature settings of bias voltages and currents. The increase in threshold voltage of NMOS (resp. PMOS) transistors at 4.2 K is compensated by applying a back-gate voltage of 1.2 V (resp. −2 V). The optimal cryogenic common-mode voltage $V_{cm} = 0.48$ V was obtained while monitoring the tank impedance via repeated frequency sweeps until a typical resonance behavior up to 200 MHz emerges for the lowest values of $C_L$ and $C_R$. The gain of the low-temperature amplification stage at $f_r$ is optimized with respect to the current bias of amplifier and buffer (see Supplementary Material IV). The main results of the impedancemetry with respect to tunability and detection sensitivity are shown in Figure 3.

The amplitude and phase of $V_{out}$ using single homodyne detection (I) without any connected DUT are shown in Figure 3a for the 4 $C_L$ values from 362 to 566 fF and two $C_R$ values chosen between 0 and 322 fF depending on $C_L$. $V_{out}$ at maximal amplitude was kept equal to 1.8 mV by adjusting $V_{in}$ to avoid non-linearities coming from non-linear MOSFETs behavior. The resonance frequency $f_r$ varies by 5.1% from 189.1 to 199.0 MHz by tuning $C_L$. The quality factors $Q$ extracted from a linear fit of the phase around $f_r$ are shown in Figure 3b. The $Q$ values range from 80 to 250, and can be tuned by a factor $> 2$ for every $C_L$ by adjusting $C_R$. These data demonstrate that $Q$ can be tuned almost independently of the resonance frequency with a frequency variation of less than 0.22% across the entire $C_R$ range (see Figure 3b).

For the minimum value of $C_L$ with the highest resonance frequency, we calibrate the capacitance sensitivity of the circuit for each $Q$ by switching on and off the DUT MOM capacitors $C_m = 2$, $3$, and $8$ fF and using double homodyne detection (II a) (see Figure 3c). The capacitance sensitivity $\alpha$ is extracted from a least-square linear fit of the phase change $\Delta \phi = QC_m/C_p \equiv \alpha C_m$ for a given $Q$ as shown in Figure 3d. The sensitivity $\alpha$ increases linearly with $Q$ from 0.76 to 1.9 °/fF. From the linear fit in Figure 3d, we obtain $C_p = 137$ fF, in good agreement with the designed value (136 fF). In usual circuits without an additional input capacitance, the parasitic capacitance of the MOSFETs determines the resonance frequency. In future design with accurate cryogenic compact models, this capacitance can be reduced significantly leading to higher resonance frequency and improved sensitivity.

From $C_p$ and $f_r$, we are now able to deduce the inductance value $L$. By adjusting $C_L$, $L$ varies from 2.42 to 5.18 µH. For a total footprint of $60 \mu m \times 50 \mu m$, the active inductance density of $1.73$ nH/mm$^2$ is five orders of magnitude higher than previously used passive inductors (55 nH/mm$^2$) and three orders of magnitude higher than superconducting inductors.
Figure 3. Characterization of the resonant circuit at 4.2 K for capacitance detection. a, Amplitude and phase of the demodulated circuit output $V_{out}$ for several active inductance settings. The resonance frequency shifts to lower frequency as the inductance value increases with increasing $C_L$ (different colors). The continuous line (low-$Q$) and dashed line (high-$Q$) show the signals for different values of $C_R$. b, Data points for the resonance frequency $f_r$ when the extracted $Q$ is tuned with $C_R$. The colored bars of width given by the written maximal deviation indicate the low dispersion of $f_r$ for fixed $C_L$ when varying $Q$ with $C_R$. c, Measured phase shift for MOM capacitor $C_m$ of 2, 4, and 8 fF in several $Q$-factor settings. The capacitance sensitivity $\Delta \phi/C_m$ of the circuit is extracted from the slope with a least square fit at given $Q$. d, Capacitance sensitivity extracted from $c$ as a function of the $Q$ factor. A least square linear fit of $\Delta \phi/C_m(Q)$ allows to extract the capacitance $C_p$ parallel with the active inductance.

(1.6 µH/mm$^2$)$^{37}$.

V. CAPACITANCE RESOLUTION

We now turn to the resolution in capacitance of the set-up, we derive the input-referred noise in aF/$\sqrt{\text{Hz}}$ from the signal-to-noise ratio (SNR) as a function of the integration time $t_{int}$. For this, we generate a capacitance change by continuously connecting and disconnecting $C_m = 2$ fF at a rate of 1 kHz. Using the demodulation method (I), the square-wave of the phase $\phi$ at $f_r$ with a rise time given by the integration time is used to extract the signal power $P_{\text{sig}}$ and noise power $P_{\text{noise}}$ by separating the corresponding frequency components in the power spectrum (see Supplementary Material IV). The resulting $\text{SNR} = P_{\text{sig}}/P_{\text{noise}}$ is used to extract the capacitance resolution given by the equivalent $C_m(\text{SNR} = 1) = C_m/\text{SNR}$ shown in Figure 4 as a function of $t_{int}$ from 100 ns to 100 µs. A capacitance of 1 fF can be detected with an integration time of 1 µs with $\text{SNR} = 1$. The capacitance resolution follows a square-root law with $t_{int}$ from which we extract the equivalent input-referred noise of 3.7 aF/$\sqrt{\text{Hz}}$, two orders of magnitude higher than the best reported sensitivity using an ultra-low noise SQUID amplifier$^{38}$.

As correlated noise appears on time scales longer than 1 ms originating probably from the $1/f$ flicker noise of the transistors, we add a second demodulation (IIa) at the capacitance switching frequency of 1 kHz to remove phase noise originating from a varying $L$. The 1 kHz square-wave $\phi$ from (I) with an integration time of 100 µs is demodulated by (IIa) at 1 kHz to obtain its amplitude $|\phi|$. The capacitance resolution as a function of the second integration time for the 1 kHz demodulation is extracted by taking the ratio of the average and the standard deviation of the $|\phi|$ signal and is shown in Figure 4. With an integration time of 1 s, the resolution becomes as low as 10 aF.

VI. QUANTUM CAPACITANCE MEASUREMENTS

With the calibrated impedancemetry circuit, we are able to detect the gate quantum capacitance $C_{gg}$ of the multiplexed tiny MOSFETs (M0, M1, M2 in Figure 2a) similar to the ones used to implement spin qubits$^7$ or single-electron transistors for read-out with CMOS technology. Measurements will be presented for M2 with a gate length of 120 nm and a gate width of 80 nm. The other available device shows similar behavior (see Supplementary Material V).

The total gate capacitance $C_{gg}$ of such devices corresponds to the sum of the capacitance to drain, source, back-gate, and MOSFET channel of which the gate to channel capacitance depends highly on the gate-source voltage $V_{gs}$ controlled by...
the DC component of $V_{\text{bias}}$ (see Figure 2a). As $C_{\text{gg}}$ of nanometric devices is extremely small compared to $C_p$, we don’t expect to have sufficient SNR for small capacitance variations at reasonable integration times. Better sensitivity can be obtained by modulating $V_{\text{gs}}$ (method Iib) to measure after demodulation the first derivative $dC_{\text{gg}}/dV_{\text{gs}}$ as $C_{\text{gg}}$ varies a lot in a small $V_{\text{gs}}$ window.

While the resonator impedance is probed at 199 MHz, $V_{\text{gs}}$ is modulated at 1 kHz with mV-range excitation on $V_{\text{bias}}$ (see Figure 2bc). The obtained result with a relatively large 25 mV $V_{\text{gs}}$ modulation (shown in Figure 5a) is reminiscent of the typical gate capacitance variation around threshold voltage $V_{\text{th}} \simeq 0$ V at $V_{\text{bg}} = 6$ V. $C_{\text{gg}}$ (see inset of Figure 5a) reflects the typical behavior for a FET capacitance from the subthreshold regime $V_{\text{gs}} < V_{\text{th}}$ to the strong inversion regime $V_{\text{gs}} \gg V_{\text{th}}$. Upon decreasing the amplitude of the $V_{\text{gs}}$ modulation to only 3.1 mV, the observed $dC_{\text{gg}}/dV_{\text{gs}}$ signal in Figure 5b reveals a fine structure around $V_{\text{th}}$ consisting of successive peak-dip oscillations. Following numerical integration, these features result in a series of peaks in $C_{\text{gg}}$, which we interpret as quantum contributions to the capacitance coming from electrons tunneling in and out of localized quantum states within the transistor channel.

To further identify these quantum states, we acquire $dC_{\text{gg}}/dV_{\text{gs}}$ for different back-gate voltage $V_{\text{bg}}$ from 2 to 6 V as shown in Figure 5c. As $V_{\text{bg}}$ increases, all observed features shift to lower $V_{\text{gs}}$ with a slope close to the ratio $\beta$ of gate-channel capacitance $C_{g-ch}$ over the backgate-channel capacitance $C_{bg-ch}$ alike the $V_{\text{th}}$-shift with back-gate for similar FET devices. For $V_{\text{bg}} > 4$ V, all features have a coupling ratio of 10 except for one with a lower coupling 8.6 attributed to an impurity closer to the back-gate interface. No anomalous impurity structure is detected in the smaller 60 nm × 80 nm device (see Supplementary Material V). At lower $V_{\text{bg}}$, the coupling increases with $V_{\text{gs}}$ from 10 to 14 as the electron-filled inversion layer is brought back to the top-interface.

These measurements of integrated quantum devices demonstrate that the capacitive signature of structure in the electronic density of states of quantum dots can be probed via impedancemetry.

VII. CONCLUSIONS

We reported an integrated circuit that performs impedancemetry of a resonator coupled to a quantum dot at cryogenic temperatures. The active inductance of the resonator allowed the controlled tuning of the resonance frequency and quality factor, which will be of importance for optimal frequency-spectrum crowding in multiplexed read-out schemes. The employed multiplexing of nanometric quantum devices with on-chip switches could be beneficial for reduced power per qubit in a scalable multi-qubit architecture. Novel read-out architectures with cryogenic electronics, such as the active inductance, have the potential to increase scalability and flexibility in the design and exploitation of quantum processors.

Further work towards lower noise and lower power design with more accurate high-frequency models at cryogenic temperatures will improve the final performance. Measuring multiplexed out-of-chip capacitances of quantum devices will be also promising for the screening of quantum devices with a simpler experimental setup than reflectometry. In the long run, the realization of tailored high-end analog electronics at cryogenic temperatures will improve and accelerate the up-scaling of quantum processors.

METHODS

Fabrication details. The impedancemetry chip was designed in a commercial CMOS FD-SOI 28nm technology with low-$V_{\text{th}}$ (LVT) thin-oxide (GO1) transistors. The chip is wire-bonded onto a QFN48 package directly soldered on a 4-layer PCB with FR4 substrate.

Measurement set-up. The FR4 PCB is placed at the end of a dip-stick enclosed in a metallic container filled with a small amount of helium gas for thermal exchange with a liquid He bath (see Supplementary Material VI). A PCB-mounted thermometer ensures a precise monitoring of the PCB temperature. High-frequency lines of $V_{\text{in}}$ and $V_{\text{out}}$ are routed on the PCB from the chip package to the SMA coaxial connectors via top-layer 50Ω-matched coplanar waveguide with ground plane and via fencing. Supply lines are decoupled from environmental noise with PCB-mounted capacitors (0.1, 1, 10µF) and conveyed to room temperature with copper wiring. All other DC lines are conveyed to room-temperature with 50 – 130Ω constantan wiring. At room temperature, electronic apparatus comprises a multi-channel low-noise 21-bit digital-to-analog converter, and a 600 MHz lock-in amplifier.
Figure 5. Quantum capacitance measurement of an integrated MOSFET with channel length 120 nm and width 80 nm. a, Measurement of the first derivative of the gate capacitance $C_{gg}$ with respect to $V_{gs}$ by applying a gate-source AC excitation of 25 mV. The inset shows the capacitance $C_{gg}(V_{gs})$ computed from the integrated signal of the derivative. b, Expanded view of $dC_{gg}/dV_{gs}$ around the off-on transition of the MOSFET measured with a smaller excitation of 3.1 mV. The resolved features are signatures of quantized electronic states in the measured capacitance of the MOSFET channel. c, Evolution of $dC_{gg}/dV_{gs}$ with the back-gate voltage $V_{bg}$ and the gate-source voltage $V_{gs}$. The indicated slopes $\beta = dV_{bg}/dV_{gs} \approx C_{g-ch}/C_{bg-ch}$ represent the relative coupling strength of the detected quantized states with respect to back- and front-gate.

**DATA AVAILABILITY**

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

**REFERENCES**

1. Peter W. Shor. Polynomial-Time Algorithms for Prime Factorization and Discrete Logarithms on a Quantum Computer. arXiv:quant-ph/9508027, January 1996. arXiv: quant-ph/9508027.
2. Lov K. Grover. Quantum Mechanics Helps in Searching for a Needle in a Haystack. Physical Review Letters, 79(2):325–328, July 1997.
3. I.M. Georgescu, S. Ashhab, and Franco Nori. Quantum simulation. Reviews of Modern Physics, 86(1):153–185, March 2014.
4. Frank Arute, Kunal Arya, Ryan Babbush, David Bacon, Joseph C. Bardin, Rami Barends, Rui Biswas, Sergio Boixo, Fernando G. S. L. Brandao, David A. Buell, Brian Burkett, Yu Chen, Zijun Chen, Ben Chiaro, Roberto Collins, William Courtney, Andrew Dunsworth, Edward Farhi, Brooks Foxen, Austin Fowler, Craig Gidney, Marissa Giustina, Rob Graff, Keith Guerin, Steve Habegger, Matthew P. Harrigan, Michael J. Hartmann, Alan Ho, Markus Hoffmann, Trent Huang, Travis S. Humble, Sergei V. Isakov, Evan Jeffrey, Zhang Ji, Divan Kafri, Kostyantyn Khechadzhi, Julian Kelly, Paul V. Klimov, Sergey Knysh, Alexander Korotkov, Fedor Kostitsa, David Landhuis, Mike Lindmark, Erik Lucero, Dmitry Lyakh, Salvatore Mandrà, Jarrod R. McClean, Matthew McEwen, Anthony Megrant, Xiao Mi, Kristel Michielsen, Masoud Mohseni, Josh Mutus, Ofer Naaman, Matthew Neeley, Charles Neill, Murphy Yuezhen Niu, Eric Ostby, Andre Petukhov, John C. Platt, Chris Quintana, Eleanor G. Rieffel, Pedram Roushan, Nicholas C. Rubin, Daniel Sank, Kevin J. Satzinger, Vadim Smelyanskiy, Kevin J. Sung, Matthew D. Turchick, Amit Vainsencher, Benjamin Villalonga, Theodore White, Z. Jamie Yao, Ping Yeh, Adam Zalcman, Hartmut Neven, and John M. Martinis. Quantum supremacy using a programmable superconducting processor. Nature, 574(7779):505–510, October 2019.
5. Yiqing Zhou, E. Miles Stoudenmire, and Xavier Waintal. What Limits the Simulation of Quantum Computers? Physical Review X, 10(4):041038, November 2020.
6. Craig Gidney and Martin Ekerå. How to factor 2048 bit RSA integers in 8 hours using 20 million noisy qubits. arXiv:1905.09749 [quant-ph], December 2019. arXiv: 1905.09749.
7. R. Maurand, X. Jehl, D. Kotekar-Patil, A. Corna, H. Bohuslavský, R. Lavriëville, L. Hutin, S. Barraud, M. Vinet, M. Sanquer, and S. De Franceschi. A CMOS silicon spin qubit. Nature Communications, 7:13575, November 2016.
8. Matias Urdampilleta, David J. Niegemann, Emmanuel Charron, Baptiste Jadot, Cameron Spence, Pierre-André Mortemousque, Christopher Bäuerle, Louis Hutin, Benoît Bertrand, Sylvain Barraud, Romain Maurand, Marc Sanquer, Xavier Jehl, Silvano De Franceschi, Maud Vinet, and Tristan Meunier. Gate-based high fidelity spin readout in a CMOS device. Nature Nanotechnology, 14(8):737–741, August 2019. Number: 8 Publisher: Nature Publishing Group.
9. C. H. Yang, R. C. C. Leon, J. C. C. Hwang, A. Saravia, T. Tanttu, W. Huang, J. Camirand Lemyre, K. W. Chan, K. Y. Tan, F. E. Hudson, K. M. Itoh, A. Morello, M. Pioro-Ladrière, A. Laucht, and A. S. Dzurak. Operation of a silicon quantum processor unit cell above one kelvin. Nature, 580(7803):350–354, April 2020. Number: 7803 Publisher: Nature Publishing Group.
10. D. R. Ward, D. E. Savage, M. G. Lagally, S. N. Coppersmith, and M. A. Eriksson. Integration of on-chip field-effect transistor switches with dopantless Si/SiGe quantum dots for high-throughput testing. Applied Physics Letters, 102(21):213107, May 2013.
B. Cardoso Paz, Loick Le Guevel, Gerard Billiot, Xavier Jehl, Silvano De Franceschi, Marcos Zurita, Yuvan Thonnart, Maud Vinet, Marc Sanquer, Romain Maurand, Aloysius G. M. Jansen, and Gail Pillonnet. A 110nm 295μW 28nm FD-SOI CMOS Quantum Integrated Circuit with a 2.8GHz Excitation and na Current Sensing of an On-Chip Double Quantum Dot. In 2020 IEEE International Solid-State Circuits Conference - (ISSCC), pages 306–308, San Francisco, CA, USA, February 2020. IEEE.

Jiang Gong, Yue Chen, Fabio Sebastiani, Edouard Charbon, and Masoud Babaie. 19.3 A 200-mW 4- to 5-GHz Cryogenic Oscillator with an Automatic Common-Mode Resonance Calibration for Quantum Computing Applications. In 2020 IEEE International Solid-State Circuits Conference - (ISSCC), pages 308–310, February 2020. ISSN: 2376-8606.

M. L. V. Tagliaferri, A. Crippa, S. Cocco, M. De Michielis, M. Fanciulli, G. Ferrari, and E. Prati. Modular Printed Circuit Boards for Broadband Characterization of Nano-Electronic Quantum Devices. IEEE Transactions on Instrumentation and Measurement, 65(8):1827–1835, August 2016.

5. Le Guevel, G. Billiot, B. Cardoso Paz, M. L. V. Tagliaferri, S. De Francesco, G. Pillonnet, and E. Prati. Low-power transimpedance amplifier for cryogenic integration with quantum devices. Applied Physics Reviews, 7(4):041407, December 2020. Publisher: American Institute of Physics.

Jeroen Petrus Gerardus Van Dijk, Bishnu Patra, Sushil Subramanian, Xiao Xue, Nodar Samkharadze, Andrea Corna, Charles Jean, Farhana Sheikh, Esdras Juarez-Hernandez, Brando Perez Esparrza, Huzafia Rampurawala, Brent R. Carlson, Suresh Ravikumar, Carla J. Barbé, and M. Vinet. A Scalable Cryo-CMOS Controller for the Wideband Frequency-Multiplexed Control of Spin Qubits and Transmons. IEEE Journal of Solid-State Circuits, pages 1–1, 2020. Conference Name: IEEE Journal of Solid-State Circuits.

E. Schrieck, F. Sebastiani, and E. Charbon. A Cryo-CMOS Digital Cell Library for Quantum Computing Applications. IEEE Solid-State Circuits Letters, pages 1–1, 2020. Conference Name: IEEE Solid-State Circuits Letters.

Simon Schaal, Alessandro Rossi, Virginia N. Cirianno-Tejel, Tsung-Yeh Yang, Sylvain Barraud, John J. L. Morton, and M. Fernando Gonzalez-Zalba. A CMOS dynamic random access architecture for radio-frequency readout of quantum devices. Nature Electronics, 2(6):236–242, June 2019.

Andrea Ruffino, Tsung-Yeh Yang, John Michniewicz, Yatao Peng, Edouard Charbon, and Miguel Fernando Gonzalez-Zalba. Integrated multiplexed microwave readout of silicon quantum dots in a cryogenic CMOS chip. arXiv:2101.08295 [cond-mat, physics:physics, physics:quant-ph], January 2021, arXiv:2101.08295.

Xiao Xue, Bishnu Patra, Jeroen P. van Dijk, Nodar Samkharadze, Shusil Subramanian, Andrea Corna, Charles Jean, Farhana Sheikh, Esdras Juarez-Hernandez, Brando Perez Esparrza, Huzafia Rampurawala, Brent Carlson, Suresh Ravikumar, Carla J. Barbé, and M. Vinet. Integrated multiplexed microwave readout of silicon quantum dots in a cryogenic CMOS chip. arXiv:2009.14185 [cond-mat, physics:physics, physics:quant-ph], September 2020. arXiv:2009.14185.

A. Crippa, R. Ezzouch, A. Aprà, A. Amisse, R. Laviéville, L. Hulin, B. Bertrand, M. Vinet, M. Urdampilleta, T. Meunier, M. Sanquer, X. Jel, R. Maurand, and S. De Franceschi. Gate-reflectometry dispersive readout and coherent control of a spin qubit in silicon. Nature Communications, 10(1):2776, December 2019.

Guoji Zheng, Nodar Samkharadze, Marc L. Noordam, Nima Kalhor, Delphine Brousses, Amir Sammak, Giordano Scappucci, and Lieven M. K. Vandersypen. CMOS-based cryogenic control of silicon quantum circuits. arXiv:2009.14185 [cond-mat, physics:physics, physics:quant-ph], September 2020. arXiv:2009.14185.

Fei Yuan. CMOS Active Inductors and Transformers. Springer US, Boston, MA, 2008.

A. Ilker Karsilaylan and R. Schaumann. A high-frequency high-Q CMOS active inductor with DC bias control. In Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems (Cat.No.CH37144), volume 1, pages 486–489 vol.1, August 2000.

Lucas Nyssens, Arka Halder, Babak Kazemi Esfèh, Nicholas Planès, Denis Flandre, Valéryia Kilibytyska, and Jean-Pierre Raskin. 29-nm FD-SOI CMOS RF Figures of Merit Down to 4.2 K. IEEE Journal of the Electron Devices Society, 8:646–654, 2020. Conference Name: IEEE Journal of the Electron Devices Society.

Bruna Cardoso Paz, Loick Le Guevel, Michaël Cassé, Gérard Billiot, Gail Pillonnet, Aloysius Jansen, Sébastien Haendler, André Juge, Emmanuel Vincent, Philippe Galy, Gérard Ghibaudo, Maud Vinet, Silvano de Franceschi, Tristan Meunier, and Fred Gaillard. Integrated Variability Measurements of 28nm FDSOI MOSFETs down to 4.2 K for Cryogenic CMOS Applications. In 2020 IEEE 33rd International Conference on Microelectronic Test Structures (ICMTS), pages 1–5, May 2020. ISSN: 2158-1029.

3. R. Maurand, M. Cassé, M. Samkharadze, A. G. M. Jansen, R. Maurand, S. Haendler, A. Juge, E. Prati, M. Vinet, S. de Franceschi, T. Meunier, F. Gaillard, and Institut Néel. Variability Evaluation of 28nm FD-SOI Technology at Cryogenic Temperatures down to 100mK for Quantum Computing. IEEE Symposium on VLSI Technology (In Press), 2020.

S. Bonen, W. T. Chen, I. Jiang, D. R. Daughton, G. C. Adam, S. Jordànescu, M. Pájatean, I. Giangiu, H. Fia, L. E. Gutierrez, W. T. Chen, N. Messaoudi, D. Harme, A. Müller, R. R. Mansour, P. Asbeck, and S. P. Voinigescu. Cryogenic Characterization of 22-nm FDSOI Technology for Quantum Computing ICs. IEEE Electron Device Letters, 40(1):127–130, January 2019. Conference Name: IEEE Electron Device Letters.

T. Poiron, O. Rozeau, P. Scheer, S. Martinie, M. Jaud, M. Minondo, A. Gubier, J. C. Barbé, and M. Vinet. LETI-UTSOI2.1: A Compact Model for UTBB-FDSOI Technologies—Part II: DC and AC Model Description. IEEE Transactions on Electron Devices, 62(9):2760–2768, September 2015.

Haipiao Xiao and Rolf Schaumann. A 5.4-GHz high-Q tunable active-inductor bandpass filter in standard digital CMOS technology. Analog Integrated Circuits and Signal Processing, 51(1):1–9, April 2007.

H. Barthelemy and W. Rahajandraibe. NMOS transistors based Karsilaylan, L. Le Guevel, M. Cassé, G. Billiot, G. Pillonnet, A. G. M. Jansen, R. Maurand, S. Haendler, A. Juge, E. Prati, M. Vinet, S. de Franceschi, T. Meunier, F. Gaillard, and Institut Néel. Variability Evaluation of 28nm FD-SOI Technology at Cryogenic Temperatures down to 100mK for Quantum Computing. IEEE Symposium on VLSI Technology (In Press), 2020.

Bruna Cardoso Paz, Loick Le Guevel, Michaël Cassé, Gérard Billiot, Gail Pillonnet, Aloysius Jansen, Sébastien Haendler, André Juge, Emmanuel Vincent, Philippe Galy, Gérard Ghibaudo, Maud Vinet, Silvano de Franceschi, Tristan Meunier, and Fred Gaillard. Integrated Variability Measurements of 28nm FDSOI MOSFETs down to 4.2 K for Cryogenic CMOS Applications. In 2020 IEEE 33rd International Conference on Microelectronic Test Structures (ICMTS), pages 1–5, May 2020. ISSN: 2158-1029.

B. Cardoso Paz, L. Le Guevel, M. Cassé, G. Billiot, G. Pillonnet, A G M Jansen, R. Maurand, S. Haendler, A Juge, E. Prati, P. Galy, G. Ghibaudo, M. Vinet, S. de Franceschi, T. Meunier, F. Gaillard, and Institut Néel. Variability Evaluation of 28nm FD-SOI Technology at Cryogenic Temperatures down to 100mK for Quantum Computing. IEEE Symposium on VLSI Technology (In Press), 2020.
ysis of On-Chip Microwave Passive Components at Cryogenic Temperatures. \textit{arXiv:1911.13084 [physics, physics:quant-ph]}, November 2019.
\textit{arXiv: 1911.13084}.

J. M. Hornibrook, J. I. Colless, A. C. Mahoney, X. G. Croot, S. Blanvillain, H. Lu, A. C. Gossard, and D. J. Reilly. Frequency multiplexing for readout of spin qubits. \textit{Applied Physics Letters}, 104(10):103108, March 2014.

F. J. Schupp, F. Vigneau, Y. Wen, A. Mavalankar, J. Griffiths, G. A. C. Jones, I. Farrer, D. A. Ritchie, C. G. Smith, L. C. Camenzind, L. Yu, D. M. Zumbühl, G. A. D. Briggs, N. Ares, and E. A. Laird. Radio-frequency reflectometry of a quantum dot using an ultra-low-noise SQUID amplifier. \textit{arXiv:1810.05767 [cond-mat, physics:physics, physics:quant-ph]}, June 2020. \textit{arXiv: 1810.05767}.

ACKNOWLEDGEMENTS

This work was partly supported by the European Union’s Horizon 2020 research and innovation program under Grant Agreement No. 810504 (ERC Synergy project QuCube).

COMPETING INTERESTS

The authors declare a patent application FR1914651, filed on December 17th 2019.
Supplementary Material: Compact gate-based read-out of multiplexed quantum devices with a cryogenic CMOS active inductor

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I. READ-OUT SCALING OF LARGE QUBIT ARRAYS

Figure S1. Reflectometry and scaling of large qubit arrays using directonnal couplers and passive inductors. a) Circuitry for simultaneous read-out of large arrays of qubits using reflectometry with frequency multiplexing. To address \( N \times N \) qubits in an array, \( N \) resonators at different resonant frequencies \( f_{r,i} \) are each coupled to a row of \( N \) qubits frequency-multiplexed with \( f_{m,j} \). Resonators are probed with the scattering parameter \( S_{11} \) by sending a voltage excitation made of a frequency-comb \( f_{r,i} \). The incoming wave \( RF_{in} \) and outgoing \( RF_{out} \) wave are separated with a directional coupler. The resonator frequency is defined by the 50 \( \Omega \) matching of the equivalent impedance of all resonators and differs from the LC resonant frequencies. \( RF_{out} \) is sent to room-temperature demodulation with an amplifier. Typical frequency-spectrum crowding is represented in b-c. Frequency multiplexing for a given finite bandwidth and given read-out time imposes an upper-bound on the array size \( N \). As an example, for a read-out time of 1 \( \mu s \) and bandwidth of 1 GHz, \( N \times N \) can only be as high as 100. To further increase the number of qubits, each tile containing \( N \times N \) qubits with the required circuitry is duplicated \( m \) times. The input frequency-comb voltage excitation \( RF_{in} \) is common to all tiles while the output signal \( RF_{out} \) requires for each of them a coaxial line. d) Scaling laws in \( m \) and \( N \) and the typical footprint for the circuit elements. The footprint of reflectometry is limited by the directional coupler size of \( \sim 1 \text{ cm}^2 \) (red square in a).

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Figure S2. **Impedancemetry and scaling of large qubit arrays using passive inductors.** 

**a.** Circuitry for simultaneous read-out of large arrays of qubits using impedancemetry with frequency multiplexing. To address $N \times N$ qubits in an array, $N$ resonators at different resonant frequencies $f_{r,i}$ are each coupled to a row of $N$ qubits frequency-multiplexed at $f_{m,j}$ for current excitation via voltage-controlled current sources. Each resonator filters the out-of-resonance components within the frequency comb $f_{r,i}$ of input excitation. The voltage responses of each resonator are added together and sent through an amplifier to room-temperature demodulation for signal recovery of every single qubit response. Typical frequency-spectrum crowding is represented in **b-c** for the input and output signals. Frequency multiplexing for a given finite bandwidth and given read-out time imposes an upper-bound on the array size $N \times N$. As an example, for a read-out time of 1 µs and bandwidth of 1 GHz, $N \times N$ can only be as high as 100. To further increase the number of qubits, each tile containing $N \times N$ qubits is duplicated $m$ times. The input frequency-comb voltage excitation $RF_{in}$ is common to all tiles while the output signal $RF_{out}$ requires for each of them a coaxial line. 

**d.** Scaling laws in $m$ and $N$ and the typical footprint for the circuit elements. The footprint of impedancemetry is limited by the inductor size (red square in **a**). Passive inductors with footprint of 1 mm$^2$ can be replaced by controllable active inductors with a footprint of only 0.001 mm$^2$ to improve the circuitry scalability.

| Element   | Footprint (mm$^2$) | Scaling |
|-----------|-------------------|---------|
| Qubits    | $10^{-8}$         | $m \times N^2$ |
| Source    | $10^{-3}$         | $m \times N$  |
| Followers | $10^{-3}$         | $m \times N$  |
| Amplifiers| 0.1               | $m$       |
| Inductors | 1                 | $m \times N$  |
II. DESIGN OF THE INTEGRATED CIRCUIT

Figure S3. **Design implementation of the impedancemetry chip.** Details of the components with transistor dimensions in the integrated circuit. The capacitor banks used as variable capacitors ($C_L$, $C_R$, and $C_m$) are detailed in Figure S4 and S5. Each transistor dimension is indicated as $m \times \frac{W}{L}$ with $W$ (resp. $L$) the gate-finger width (resp. length) of the gate in $\mu$m and $m$ is the number of fingers. The indicated current references of the diode-mounted transistors are generated at room temperature (see Figure S16).

Figure S4. **Design implementation of the variable capacitors.** **a**, Implementation of the variable capacitor $C_R$ at Node$_R$ in Figure S3. The 4 binary-weighted MOM capacitors are selected with NMOS switches activated by the selection bits $SEL_R[3 : 0]$ for $C_R$ variation from 0 to 345 fF. **b**, Similar implementation of $C_L$ with 3 binary-weighted MOM capacitors in parallel from 362 to 566 fF.
Figure S5. **Multiplexing of the Device Under Test (DUT).** a. Design implementation of the capacitor bank with 3 MOM capacitors for capacitive calibration and 3 nanometer-sized MOSFETs for quantum capacitance measurements. The MOM capacitors are selected with NMOS switches. The MOSFETs are selected with a pair of pass-gates as detailed in b. When the MOSFETs are unselected, the drain and source are set to ground while the selected-MOSFET drain and source are linked to \( V_{\text{bias}} \) to change \( V_{\text{gs}} \). Pairs of pass-gate are made complementary (when one is OFF, the other one is ON) with one inverter as shown in c.

| ID | Block name           | Area (mm\(^2\)) | Contribution (%) |
|----|----------------------|------------------|------------------|
| 1  | Current generation   | 0.0013           | 33               |
| 2  | Active inductance    | 0.0017           | 41               |
| 3  | Capacitor bank       | 0.00067          | 17               |
| 4  | Amplifier            | 0.000035         | 0.86             |
| 5  | Follower             | 0.00035          | 8.7              |
|    | **Total**            | **0.0040**       | **100**          |

Figure S6. **Layout and footprint of the impedancemetry circuit.** a. Layout view of the impedancemetry circuit. The labeled areas correspond to the circuit block names of table b. The bottom inset shows a zoomed window for the measured quantum devices. Each device is surrounded by dummies to improve the fabrication quality of the nanometer-sized devices. b. Table of the occupied area of each block for a total footprint of 0.004 mm\(^2\).
III. SIMULATION RESULTS AT 300 K

Figure S7. Impedance of the active inductance from simulations at 300 K. a-d. Complex impedance of the active inductance for a few $C_R$ values with $C_L$ equal to: a 362, b 420, c 498, and d 566 fF. e-h. Quality factor $Q$ of the active inductance as a function of $C_R$ extracted from the tank impedance. In a-d (respectively e-h), stable resonance data with $Q \geq 0$ are shown in continuous lines (resp. round markers) while unstable resonance data with $Q < 0$ are shown as dashed lines (resp. square markers). i. $Q$ as a function of the resonant frequency $f_r$ showing small dispersion. j. Evolution of $f_r$ with $C_L$ at all $C_R$ values.
Figure S8. Voltage-to-current conversion for the current excitation of the tank from simulations at 300 K. Transimpedance $G_m$ and bandwidth of the current generation as a function of frequency extracted from foundry models at 300 K.

Figure S9. Amplifier and follower characteristics from simulations at 300 K. a. Gain of the amplifier as a function of frequency extracted from AC simulations with foundry models at 300 K. b. Gain of the follower loading a 50 pF cable capacitance at the chip output. c. Total amplification of amplifier and follower as a function of frequency. Despite large cable capacitance from 4.2 K to 300 K stage, the unity-gain bandwidth of 467 MHz allows to keep the gain above 1 at the resonant frequencies $f_r$.

Table I. Noise contribution from linear AC simulations at 300 K. Listed noise contributions of the 7 transistors generating 84% of the total output noise of the impedancemetry chip extracted from foundry models at 300 K. The listed transistor devices belong to the active inductance which constitutes the main source of noise in the circuit.

| Rank | Device | Contribution |
|------|--------|--------------|
| 1    | P1     | 25%          |
| 2    | N1     | 23%          |
| 3    | P1’    | 14%          |
| 4    | P2     | 10%          |
| 5    | N4     | 5%           |
| 6    | N2     | 4%           |
| 7    | N3     | 3%           |

Figure S10. Phase noise of the impedancemetry setup from 300 K simulations. Phase noise as a function of the frequency offset with respect to the resonance frequency of the tank $f_r = 167$ MHz extracted at the chip output from Steady STate (SST) simulations at 300 K with foundry models. The plateau above about 100 Hz with the cut-off around $\sim 2$ MHz is the phase noise behavior we could expect from a linear AC noise analysis. The cut-off corresponds to the width of the resonant peak $\kappa \sim f_r/Q \simeq 2.1$ MHz with the quality factor $Q = 81$. From the plateau value of $2 m^2/\sqrt{Hz}$ we estimate the input-referred noise to $3.7 aF/\sqrt{Hz}$. The appearance of a flicker component in the phase noise is the evidence of the mixing between $1/f$ low-frequency noise and the tank high-frequency signal. This additional non-linear noise is attributed to transistor noise that translates into noise contribution to the inductance $L$ and quality factor $Q$ resulting in low-frequency noise up-mixing.
IV. COMPLEMENTARY DATA OF THE RESONANT CIRCUIT AT 4.2 K

Figure S11. Amplifier and follower optimization at 4.2 K. a, Output voltage $V_{\text{out}}$ at the tank resonant frequency $f_r = 199$ MHz as a function of the amplifier power at 4.2 K. To maximize the gain, we choose the operating power of the amplifier at 150 µW. b, Output voltage $V_{\text{out}}$ at the tank resonant frequency $f_r = 199$ MHz as a function of the follower power at 4.2 K. To maximize the gain, we choose the operating power of the follower at 2.4 mW.

Figure S12. Extraction of the signal-to-noise ratio. a, Signal of the phase output after single demodulation (I) at the tank frequency $f_r$ when the DUT capacitance $C_m = 2$ fF is continuously connected and disconnected at a 1 kHz rate. b, Fourier power spectrum of $\phi$ with the typical signature of a square wave with exponential transients with the harmonics $2n+1$. The signal power spectrum related to the square wave is isolated in d and the time-domain signal trace is recovered in e by inverted Fourier transform. The signal power $P_{\text{sig}}$ is computed by integrating the power spectrum of the signal. f, Noise power spectrum in $\phi$ extracted as the complementary power spectrum to the signal spectrum shown in b. The noise power $P_{\text{noise}}$ is computed by integrating the power spectrum of the noise. e, Time-domain noise extracted from f. The signal-to-noise ratio is extracted as the ratio of $P_{\text{sig}}/P_{\text{noise}}$ and is equal to 5.7 for an integration time $t_c$ of 55 µs in this example.
Figure S13. **Correlated noise in the resonator output signal at 4.2 K.**

**a.** Magnitude and phase of the output signal after demodulation at the resonance frequency (method I). Clear correlations between magnitude and phase are observed as a function of time. Both the Spearman $\rho_S$ and Pearson $\rho_P$ computed on the entire time-trace exhibit strong anti-correlation between phase and magnitude with values of about $-0.8$. These correlations appear roughly after a 1 ms time-scale.

**b.** 2D histogram in the I-Q plane of the data in **a**. The non-gaussian banana-shaped spot distribution reflects the evidence for correlated noise in the I-Q plane. This noise is attributed to transistor noise that leads to a noisy inductance value $L$ and quality factor $Q$. 

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**Correlations:**

$\rho_P = -0.80$

$\rho_S = -0.79$
V. MEASUREMENT OF THE GATE CAPACITANCE OF A DIFFERENT DUT

Figure S14. Measurement of the N-type DUT transistor with \( L = 60 \text{nm} \) and \( W = 80 \text{nm} \). a, First derivative of the gate capacitance \( \frac{dC_{gg}}{dV_{gs}} \) of a N-type MOSFET gate-capacitance as a function of the gate-source voltage \( V_{gs} \) measured with the impedancemetry setup at 4.2 K. Oscillations in the derivative capacitance is a sign of quantum capacitance from confined electronic state in the MOSFET channel. b, \( \frac{dC_{gg}}{dV_{gs}} \) evolution with front-gate \( V_{gs} \) and back-gate \( V_{bg} \) voltages. All features shift to lower \( V_{gs} \) for increasing \( V_{bg} \). No traces attributed to an impurity state with an anomalous slope as seen in Figure 5 in the main text are detected for this device. These measurements are the same as presented in the main paper (Figure 5) for a longer device with \( L = 120 \text{nm} \) and \( W = 80 \text{nm} \).
VI. EXPERIMENTAL SETUP

Figure S15. **Experimental setup of the cryogenic sample holder.** Picture of the PCB (a) with soldered QFN48 (b), and wire-bonded integrated circuit (c). The PCB mounted at the end of a dip-stick is enclosed in a metallic tube filled with He gas for thermal exchange with a liquid helium bath at 4.2 K. High frequency signals are routed to SMA connectors at the end of the PCB with grounded coplanar waveguides and conveyed to room temperature with coaxial cables. SMD capacitors close to the chip reject the noise at sensitive voltage nodes (V\textsubscript{DD}, V\textsubscript{SS},...).

Figure S16. **Instrumentation with connections to the chip.** The chip is anchored at 4.2 K while all the equipment for voltage and current references, excitation, and signal detection are placed at room-temperature. The chip power supply lines V\textsubscript{DD} and V\textsubscript{SS} are generated from a low-noise voltage source and conveyed with copper wiring to avoid voltage drop along the line. Supply voltages are stabilized at cryogenic temperature with 3 discrete SMD capacitors (2 ceramic capacitors of 0.1 and 1 µF and 1 tantalum capacitor of 10 µF) placed on the PCB close to the chip pins. Current references are generated by applying a command voltage across a resistor R using the Sense (S-V) and Force (F-V) of the low-noise voltage sources. The 6 resistors R of 0.20, 0.40, 0.47, 0.90, 1.4, and 200 kΩ are placed in a grounded metallic enclosure for shielding from environmental noise. DC voltages on high-Z inputs (arriving on transistor gates, or back-gate wells) are applied with a low-noise voltage source with constantan wiring to reduce heat conduction from 300 to 4.2 K. The chip excitation V\textsubscript{in} and the output voltage V\textsubscript{out} conveyed with coaxial SMA lines are generated and treated by a lock-in-amplifier with 50 Ω-matched ports. A DC block at V\textsubscript{out} prevents DC currents from the buffer output to flow in the 50 Ω port. A thermometer anchored at the PCB ground back-plane is used to monitor the PCB temperature to detect eventual heating above base temperature.