A Generalized Strong–Inversion CMOS Circuitry for Neuromorphic Applications

Hamid Soleimani and Emmanuel. M. Drakakis

Abstract

It has always been a challenge in neuromorphic field to systematically translate biological models into analog electronic circuitry. In this paper, a generalized circuit design platform is introduced where biological models can be conveniently implemented using CMOS circuitry operating in strong–inversion. The application of the method is demonstrated by synthesizing a relatively complex two–dimensional (2–D) nonlinear neuron model. The validity of our approach is verified by nominal simulated results with realistic process parameters from the commercially available AMS 0.35 µm technology. The circuit simulation results exhibit regular spiking response in good agreement with their mathematical counterpart.

1 Introduction

Researchers in the neuromorphic community intend to mimic the neuro-biological structures in the nervous system using electronic circuitry. To do so different approaches have been developed so far:

1. Special purpose computing architectures have been developed to simulate complex biological networks via special software tools [1–5]. Even though these systems are biologically plausible and flexible with remarkably high performance thanks to their massively parallel architecture, they run on bulky and power-hungry workstations with relatively high cost and long development time.

2. Digital platforms are good candidates nowadays for implementing such biological and bio-inspired systems. Most digital approaches [6–15], use digital computational units to implement the mathematical equations codifying the behavior of biological intra/extracellular dynamics. Such an approach can be either implemented on FPGAs or custom ICs, with FPGAs providing lower development time and more configurability. Generally, a digital platform benefits from high reconfigurability, short development time, notable reliability and immunity to device mismatch. Although, the digital platform’s silicon area and power consumption is comparatively high compared to its analog counterpart.

3. Analog CMOS platforms are considered to be the main choice for direct implementation of intra– and extracellular biological dynamics [16–24]. This approach is very power efficient, however, model development and adjustment is generally challenging. Moreover, since the non–linear functions in the target models are directly synthesized by exploiting the inherent non–linearity of the circuit components, very good layout is imperative in order for the resulting topology not to suffer from the variability and mismatch particularly CMOS circuits operating in subthreshold.

To address the challenges explained in #3, in this paper we propose a novel approach enabling researcher in the field to systematically synthesize biological mathematical models to CMOS circuitry operating in strong–inversion. To the best of our knowledge, this is the first systematic strong–inversion circuit capable of emulating such nonlinear bilateral dynamical systems. The application of the method is verified by synthesizing a relatively complex neuron model and transistor–level simulations confirm that the resulting circuits are in good agreement with their mathematical counterparts. Further application of the proposed circuitry on different case studies is left to the interested readers.

2 A Novel Strong–inversion CMOS Circuitry

In this section, a novel current–input current–output circuit is proposed that supports a systematic realization procedure of strong–inversion circuits capable of computing bilateral dynamical systems at higher speed compared to the previously proposed log–domain circuit. The validity of our approach is verified by nominal simulated results with realistic process parameters from the commercially available AMS 0.35 µm technology.
Figure 1: The “main core” including the initialization circuit highlighted with red color.

The current relationship of an NMOS and PMOS transistor operating in strong–inversion saturation when $|V_{DS}| > |V_{GS}| - |V_{th}|$ can be expressed as follows:

$$I_{Dn} = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right)_n (V_{GS} - V_{th})^2$$  \hspace{1cm} (1)

$$I_{Dp} = \frac{1}{2} \mu_p C_{ox} \left( \frac{W}{L} \right)_p (V_{SG} - V_{th})^2$$  \hspace{1cm} (2)

where $\mu_n$ and $\mu_p$ are the charge–carrier effective mobility for NMOS and PMOS transistors, respectively; $W$ is the gate width, $L$ is the gate length, $C_{ox}$ is the gate oxide capacitance per unit area and $V_{th}$ is the threshold voltage of the device.

Setting $k_n = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right)_n$ and $k_p = \frac{1}{2} \mu_p C_{ox} \left( \frac{W}{L} \right)_p$ in (1) and (2) and differentiating with respect to time, the current expression for $I_A$ (see Figure 1) yields:

$$\dot{I}_A = \sqrt{k_n I_A} \dot{V}_{GS_1}$$  \hspace{1cm} (3)

$$\dot{I}_A = \sqrt{k_p I_A} \dot{V}_{SG_2}$$  \hspace{1cm} (4)

(3) and (4) are equal, therefore:

$$\dot{V}_{SG_2} = \sqrt{\frac{k_n}{k_p}} \dot{V}_{GS_1} = \beta \dot{V}_{GS_1}$$  \hspace{1cm} (5)

where $\beta = \sqrt{\frac{k_n}{k_p}}$. Similarly, we can derive the following equation for transistors $M_3$ and $M_4$:

$$\dot{V}_{SG_4} = \sqrt{\frac{k_n}{k_p}} \dot{V}_{GS_3} = \beta \dot{V}_{GS_3}$$  \hspace{1cm} (6)

The application of Kirchhoff’s Voltage Law (KVL) and applying the derivative function show the following relations:

$$\dot{V}_C = -(\dot{V}_{GS_1} + \dot{V}_{SG_2})$$  \hspace{1cm} (7)

$$\dot{V}_C = +(\dot{V}_{GS_3} + \dot{V}_{SG_4})$$  \hspace{1cm} (8)

where $V_C$ is the capacitor voltage and $V_b$ the bias voltage which is constant (see Figure 1). Substituting (5) and (6) into (7) and (8) respectively yields:

$$\dot{V}_C = -\dot{V}_{GS_1} \cdot (1 + \beta)$$  \hspace{1cm} (9)

$$\dot{V}_C = +\dot{V}_{GS_3} \cdot (1 + \beta)$$  \hspace{1cm} (10)
Setting the current $I_{out} = I_B - I_A$ in Figure 1 as the state variable of our system and using (9) and the corresponding equation for $I_B$, the following relation is derived:

$$
\dot{I}_{out} = \dot{I}_B - \dot{I}_A = 2\sqrt{k_n I_B V_{GS}} - 2\sqrt{k_p I_A V_{GS}},
$$

(11)

by substituting (9) and (10) in (11):

$$
\dot{I}_{out} = (\sqrt{I_A} + \sqrt{I_B}) \cdot \frac{2\sqrt{k_n V_C}}{2 + \beta}.
$$

(12)

Bearing in mind that the capacitor current $I_{Cin}$ can be expressed as $CV_C$, relation (12) yields:

$$
\dot{I}_{out} = (\sqrt{I_A} + \sqrt{I_B}) \cdot \frac{2\sqrt{k_n I_{Cin}}}{(2 + \beta)C}.
$$

(13)

One can show that:

$$
\frac{(2 + \beta)C}{2\sqrt{k_n}} \cdot \frac{I_{out}}{I_{dc}} = \frac{(\sqrt{I_A} + \sqrt{I_B})}{I_{dc}} \cdot I_{Cin}.
$$

(14)

Equation (14) is the main core’s relation. In order for a high speed mathematical dynamical system with the following general form to be mapped to (14):

$$
\tau \dot{I}_{out} = F(I_{out}, I_{ext})
$$

(15)

where $I_{ext}$ and $I_{out}$ are the external and state variable currents, the quantities $\frac{C}{I_{dc}}$ and $I_{Cin}$ must be respectively equal to $\frac{2\sqrt{k_n}}{(2 + \beta)}$ and $\frac{F(I_{out}, I_{ext})I_{dc}}{(\sqrt{I_A} + \sqrt{I_B})}$. Note that the ratio value $\frac{C}{I_{dc}}$ can be satisfied with different individual values for $C$ and $I_{dc}$. These values should be chosen appropriately according to practical considerations (see Section V.G). Since $F$ is a bilateral function, in general, it will hold:

$$
I_{Cin} = \frac{I_{Cin}^+ (I_A, I_B, I_{ext}, I_{dc})I_{dc}}{(\sqrt{I_A} + \sqrt{I_B})} - \frac{I_{Cin}^- (I_A, I_B, I_{ext}, I_{dc})I_{dc}}{(\sqrt{I_A} + \sqrt{I_B})}
$$

(16)

where $I_{Cin}^+$ and $I_{Cin}^-$ are calculated respectively by a root square block (see Figure 2(a) and $I_{ext}$ is separated to + and – signals by means of splitter blocks. Note that $I_{dc}$ is a scaling dc current and $\tau$ has dimensions of second(s). Since $I_{Cin}$ can be a complicated nonlinear function in dynamical systems, we need to provide copies of $I_{out}$ or equivalently of $I_A$ and $I_B$ to simplify the systematic computation at the circuit level. Therefore, the higher hierarchical block shown in Figure 2(b) is defined as the NBDS (Nonlinear Bilateral Dynamical System) circuit [16] (see Figure Figure 2(b)) including the main block and associated current mirrors. The form of (15) is extracted for a 1–D dynamical system and can be extended to $N$ dimensions in a straightforward manner as follows:

$$
\tau_N \dot{I}_{out_N} = F_N(I_{out}, I_{ext})
$$

(17)

where $\frac{C_N}{I_{dc_N}} = \frac{2\sqrt{k_N}}{(2 + \beta)}$ and $I_{Cin_N} = \frac{F_N(I_{out}, I_{ext})I_{dc_N}}{\sqrt{I_{A_N} + \sqrt{I_{B_N}}}}$. 

Figure 2: (a) The “main block” including the main core and two current–mode root square blocks and a bilateral multiplier. (b) The final high speed circuit including the “main block” with several copied currents (the current mirrors are represented with double circle symbols).
Figure 3: (a) Transistor level representation of the basic Root Square block. The current mirrors are represented with double circle symbols. (b) Transistor level representation of the MULT core block. The current mirrors are represented with double circle symbols.)

3 Basic Electrical Blocks

3.1 Root Square Block

This block performs current mode root square function on single-sided input signals. By setting \((\frac{W}{L})_{1,2} = 4 \times (\frac{W}{L})_{3,4}\), considering \(I_1, I_2, I_3\) and \(I_4\) as the currents flowing respectively into \(M_1, M_2, M_3\) and \(M_4\) and all transistors operate in strong-inversion saturation, the governing TL principle for this block becomes (highlighted with dotted blue arrow):

\[
\frac{1}{2}(\sqrt{I_1} + \sqrt{I_2}) = \sqrt{I_3} + \sqrt{I_4} \tag{18}
\]

By pushing specific currents (copied by current mirrors) according to Figure 3 (a) into the TL’s transistors we have:

\[
\begin{align*}
I_1 &= I_2 = I_{\text{in}} + I_{\text{out}} + I_b \\
I_3 &= I_b, \quad I_4 = I_{\text{in}}
\end{align*}
\]  \tag{19}

Substituting (19) into (18) yields:

\[
\frac{1}{2} \times (\sqrt{I_{\text{in}} + I_{\text{out}} + I_b} + \sqrt{I_{\text{in}} + I_{\text{out}} + I_b}) = \sqrt{I_{\text{in}} + I_b} \tag{20}
\]

By squaring both sides of (20):

\[
I_{\text{in}} + I_{\text{out}} + I_b = \sqrt{I_{\text{in}} + I_b} \cdot I_b \tag{21}
\]

and finally:

\[
I_{\text{out}} = 2\sqrt{I_{\text{in}} \cdot I_b} \tag{22}
\]

3.2 MULT Core Block

This block is the main core forming the final bilateral multiplier which is introduced in the next subsection. The block contains six transistors as well as two current mirrors. By assuming \(I_1, I_2, I_3\) and \(I_4\) as the currents flowing respectively into \(M_1, M_2, M_3\) and \(M_4\) and the same \(\frac{W}{L}\) aspect ratio for all transistors operating in strong-inversion saturation, the KVL at the highlighted TL with dotted blue arrow yields:

\[
\sqrt{I_1} + \sqrt{I_2} = \sqrt{I_3} + \sqrt{I_4} \tag{23}
\]

By forcing specific currents (copied by current mirrors) according to Figure 3 (b) into the TL’s transistors we have:

\[
\begin{align*}
I_1 &= I_b, \quad I_2 = I_{\text{out}} \\
I_3 &= I_4 = \frac{1}{2}(I_{\text{in}} + \frac{I_{\text{out}}}{2} + I_b)
\end{align*}
\]  \tag{24}
Substituting (24) into (23) yields:

$$\sqrt{I_{\text{out}}} + \sqrt{I_b} = 2\sqrt{\frac{1}{2}(I_{\text{in}} + \frac{I_{\text{out}}}{2} + I_b)}$$

(25)

By squaring both sides of (23):

$$\sqrt{I_{\text{out}}} \cdot I_b = I_{\text{in}} + \frac{1}{2} I_b$$

(26)

and:

$$I_{\text{out}} = \frac{(I_{\text{in}} + \frac{1}{2} I_b)^2}{I_b}$$

(27)

3.3 Bilateral MULT Block

This block is able to perform current mode multiplication operation on bilateral input signals. If inputs are split to positive and negative sides we have:

$$\begin{align*}
X &= X^+ - X^- \\
Y &= Y^+ - Y^-.
\end{align*}$$

(28)

The multiplication result can be expressed as

$$XY = X^+Y^+ + X^-Y^- - (X^-Y^+ + Y^-X^+).$$

By extending equation (27) to \(\frac{I_{\text{in}}^2}{I_b} + \frac{I_{\text{out}}}{4} + I_{\text{in}}\) for every basic MULT core block, the output signal constructed by a positive and negative side can be written as:

$$I_{\text{out}} = \frac{(X^+ + Y^+)^2}{I_b} + \frac{(X^+ + Y^+)}{4} + \frac{(X^- + Y^-)^2}{I_b} + \frac{(X^- + Y^-)}{4} + \frac{I_b}{4}$$

$$- \frac{(X^- + Y^-)^2}{I_b} - \frac{(X^- + Y^-)}{4} - \frac{(X^+ + Y^-)^2}{I_b} - \frac{(X^+ + Y^-)}{4} - \frac{I_b}{4}$$

(29)

and by further simplifications:

$$I_{\text{out}} = \frac{I_{\text{out}}^+}{I_b} - \frac{I_{\text{out}}^-}{I_b} = \frac{2XY}{I_b}$$

(30)

3.4 Circuit Realization of FHN neuron model

The systematic synthesis procedure provides the flexibility and convenience required for the realization of nonlinear dynamical systems by computing their time-dependent dynamical behavior. In this subsection, we
showcase the methodology through which we systematically map the mathematical dynamical models onto the proposed electrical circuit. Here, the application of the method is demonstrated by synthesizing the 2–D nonlinear FitzHugh–Nagumo neuron model. In the FHN neuron model \([25]\) with the following representation:

\[
\dot{v} = v - \frac{v^3}{3} - w + I_{ext}
\]

\[
\dot{w} = 0.18(v + 0.7 - 0.8w)
\]

where \(v\) and \(w\) describe the membrane potential’s and the recovery variable’s velocity, the state variables in the absence of input stimulation remain at \((v, w) \approx (−1.2, −0.6)\), while these values go up to \((v, w) \approx (2, 1.7)\) in the presence of input stimulation. According to this biological dynamical system, we can start forming the electrical equivalent using \([17]\):

\[
\begin{aligned}
I_{out_v} &= F_v(I_{out_v}, I_{out_w}, I_{ext}) \\
I_{out_w} &= F_w(I_{out_v}, I_{out_w})
\end{aligned}
\]

where \(I_{dc_v} = 80\, \mu A, I_{dc_w} = a \cdot I_{dc_v} = 6.4\, nA\). \(F_v\) and \(F_w\) are functions given by:

\[
\begin{aligned}
F_v(I_{out_v}, I_{out_w}, I_{ext}) &= I_{out_v} - \frac{I_{ext}^2}{I_{out_v}^2} - I_{out_w} + I_{ext} \\
F_w(I_{out_v}, I_{out_w}) &= (I_{out_v} + I_c - \frac{I_{ext}^2}{I_{out_v}^2})
\end{aligned}
\]

where \(I_b = 3\, \mu A, I_c = 0.7\, \mu A, I_d = 0.8\, nA\) and \(I_g = 1\, nA\).

Schematic diagrams for the FHN neuron model is seen in Figure 5, including the symbolic representation of the basic TL blocks introduced in the previous sections. According to these diagrams, it is observed how the mathematical model is mapped onto the proposed electrical circuit. The schematic contains two NBDS circuits implementing the two dynamical variables, followed by two MULT and current mirrors realizing the dynamical functions. As shown in the figure, according to the neuron model, proper bias currents are selected and the correspondence between the biological voltage and electrical current is \(V \iff uA\).

4 Discussion

Here, we demonstrate the simulation–based results of the high speed circuit realization of the FHN neuron model. The hardware results simulated by the Cadence Design Framework (CDF) using the process parameters
of the commercially available AMS 0.35 µm CMOS technology are validated by means of MATLAB simulations as shown in Figure 6. For the sake of frequency comparison, a regular spiking mode is chosen. Generally, results confirm an acceptable compliance between the MATLAB and Cadence simulations while the hardware model operates at higher speed (almost 1 million times faster than real-time). Table 1 summarizes the specifications of the proposed circuit applied to this case study. As shown in the table, the circuit uses a higher $V_b$ compared to the subthreshold version to force the circuit to operate in strong-inversion region. This comes at the expense of higher power consumption (95000 times higher than the subthreshold version).

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