A Single Universal \(n\)-bit Gate for Reversible Circuit Synthesis

Ahmed Younes*
Department of Mathematics and Computer Science
Faculty of Science, Alexandria University
Alexandria, Egypt

May 7, 2014

Abstract

Many universal reversible libraries that contain more than one gate type have been proposed in the literature. Practical implementation of reversible circuits is much easier if a single gate type is used in the circuit construction. This paper proposes a reversible \(n\)-bit gate that is universal for reversible circuits synthesis. The proposed gate is extendable according to the size of the circuit. The paper shows that the size of the synthesized circuits using the proposed gate is comparable with the size of the synthesized circuits using the hybrid reversible libraries for 3-in/out reversible circuits.

Keywords: Reversible circuit; Universal gate; Circuit Optimization; Group Theory.

1 Introduction

Reversible logic [1, 9] is one of the hot areas of research. It has many applications in quantum computation [12, 21], low-power CMOS [7, 3] and many more. Synthesis of reversible circuits cannot be done using conventional ways [25].

A lot of work has been done trying to find an efficient reversible circuit for an arbitrary reversible function [8, 15, 19, 20]. A method is given in [13], where a very useful set of transformations for Boolean quantum circuits is shown. A lot of work has been done trying to find an efficient reversible circuit for an arbitrary multi-output Boolean functions by using templates [16, 17] and data-structure-based optimization [22]. A method to generate an optimal 4-bit reversible circuits has been proposed [11]. Benchmarks for reversible circuits have been established [18].

Recently, the study of reversible logic synthesis problem using group theory is gaining more attention. Investigation on the universality of the basic building blocks of reversible circuit has been done [24, 4]. A relation between Young subgroups and the reversible logic synthesis problem has been proposed [5]. A comparison between the decomposition of reversible circuit and quantum circuit using group theory has been shown [6]. A GAP-based algorithms to synthesize reversible circuits for various types of gate with various gate costs has been proposed [26].

The aim of any reversible circuit synthesis algorithm is to synthesize a reversible circuit for a given specification with the smallest possible number of gates. The reversible circuit synthesis algorithm should specify a gate library to be used during the synthesis process. Many gates libraries have been suggested in the literature. All suggested gates libraries consist of more than one type of gates such as NOT (N), Feynman (C), Toffoli (T3), Fredkin (F) and Peres (P) gates. Gate libraries such as NCT, NCF and NCP have been studied. It can be easily shown that the larger the number of basic gates used in the gate library, the smaller the number of gates in the synthesized circuit. Assume that there is a gate library for \(n\)-bit circuits contain \(2^n!\) gates, then all synthesized circuits will be of size one.

Another reason that all suggested gate libraries in the literature contain more than one gate type is that none of the suggested gates is universal for reversible computing. Toffoli and Fredkin gates are reversible gates that are proved to be universal for non-reversible computation by showing that they can function as NAND gate.

NAND gate is a classical non reversible gate that is universal for classical circuit design. NAND gate is preferred over other universal classical set of gates such as AND/OR/NOT and AND/XOR/NOT because using single type of gates in the synthesis process makes the circuit cheaper. NOR gate is another universal gate.

*ayounes2@yahoo.com or ayounes@alexu.edu.eg
Although a digital circuit can be implemented with AND/OR/NOT, classical computers are built almost exclusively on NAND and NOR gates even with a little increase in the size of the circuit because of technology considerations; that is, using a single type of gates might be cheaper to implement, for example OR gate can be implemented by 3 NAND gates connected together.

The aim of this paper is to suggest a new reversible gate that is universal for reversible circuit design. This is important as it is cheaper in practice to make lots of similar things than a bunch of different things (different gates). All results shown in the paper have been obtained using the group-theory algebraic software GAP [10]. Some results shown in this paper matches the results obtained by other methods such as [23] and [26].

The paper is organized as follows: Section 2 gives a short background on the synthesis of reversible circuit problem and shows the reduction of the problem to be handled by permutation group. Section 3 analyzes the universality properties of common universal reversible libraries in the literature. Section 4 introduces the proposed pure universal reversible library and shows its properties. The paper ends up with a conclusion in Section 5.

2 Basic Notions

In this section, the basic notions for reversible circuit synthesis, permutation group, the relationship between reversible logic circuits and permutation group theory will be reviewed.

Definition 2.1 Let \( X = \{0,1\} \). A Boolean function \( f \) with \( n \) input variables, \( x_1, \ldots, x_n \), and \( n \) output variables, \( y_1, \ldots, y_n \), is a function \( f : X^n \rightarrow X^n \), where \( (x_1, \ldots, x_n) \in X^n \) is called the input vector and \( (y_1, \ldots, y_n) \in X^n \) is called the output vector.

Definition 2.2 An \( n \)-input \( n \)-output Boolean function is reversible (\( n \times n \) function) if it maps each input vector to a unique output vector, i.e. a one-to-one, onto function (bijection).

There are \( 2^n! \) reversible \( n \times n \) Boolean functions. For \( n = 3 \), there are 40,320 3-in/out reversible functions.

Definition 2.3 An \( n \)-input \( n \)-output (\( n \)-in/out) reversible gate (or circuit) is a gate that realizes an \( n \times n \) reversible function.

Definition 2.4 When an \( m \)-in/out reversible gate \( U \) is applied on an \( n \)-in/out reversible circuit such that \( m \leq n \), then \( U \) will be denoted as \( U^n_{i_1 i_2 \ldots i_m} \) where \( \{i_1, i_2, \ldots, i_m\} \) are the \( m \) wires spanned by \( U \) in order.

Definition 2.5 A set of reversible gates that can be used to build a reversible circuit is called a gate library \( L \).

Definition 2.6 A universal reversible gate library \( L_n \) is a set of reversible gates such that a cascading of gates in \( L_n \) can be used to synthesize any reversible circuit with \( n \)-in/out.

Definition 2.7 A universal reversible gate sub library \( SL_n \) is a set of reversible gates such that \( SL_n \subseteq L_n \) that can be used to build any reversible circuit with \( n \)-in/out.

Definition 2.8 Consider a finite set \( A = \{1,2,\ldots,N\} \) and a bijection \( \sigma : A \rightarrow A \), then \( \sigma \) can be written as,

\[
\sigma = \begin{pmatrix}
1 & 2 & 3 & \ldots & N \\
\sigma(1) & \sigma(2) & \sigma(3) & \ldots & \sigma(N)
\end{pmatrix},
\]

i.e. \( \sigma \) is a permutation of \( A \). Let \( A \) be an ordered set, then the top row can be eliminated and \( \sigma \) can be written as,

\[
(\sigma(1), \sigma(2), \sigma(3), \ldots, \sigma(N)).
\]

Any reversible circuit with \( n \)-in/out can be considered as a permutation \( \sigma \) and Eqn.3 is called the specification of this reversible circuit such that \( N = 2^n \).
The set of all permutations on \( A \) forms a symmetric group on \( A \) under composition of mappings \([14]\), denoted by \( S_N \) \([2]\). A permutation group \( G \) is a subgroup \([14]\) of the symmetric group \( S_N \). A universal reversible gate library \( L_n \) is called the generators of the group. Another important notation of a permutation is the product of disjoint cycles \([2]\). For example, \( (1, 2, 3, 4, 5, 6, 7, 8) \) will be written as 
\[
(1, 3, 5, 6)(7, 8).
\]
The identity mapping "()" is called the unit element in a permutation group. A product \( p \ast q \) of two permutations \( p \) and \( q \) means applying mapping \( q \) then \( p \), which is equivalent to cascading \( p \) and \( q \).

The one-to-one correspondence between a \( n \times n \) reversible circuit and a permutation on \( A = \{1, 2, \ldots, N\} \) is established as done in \([26]\). In the permutation group references, \( A \) begins from one, instead of zero. Therefore, we have the following relation \([26]\): \( < X_N, X_{N-1}, \ldots, X_1 > \equiv \text{index}(X_N, \ldots, X_1) - 1 \). Using the integer coding, a permutation is considered as a bijective function \( f : \{1, 2, \ldots, N\} \rightarrow \{1, 2, \ldots, N\} \). Cascading two generators is equivalent to multiplying two permutations. In what follows, a \( n \times n \) reversible gate is not distinguished from a permutation in \( S_N \).

![Figure 1: A hypercube network with (a) 2 vertices, (b) 4 vertices, (c) 8 vertices and (d) 16 vertices.](image)

**3 Universal Reversible Libraries**

**3.1 1-bit Reversible circuits**

\( \text{NOT} (N) \) gate is a 1-bit gate that flips the input unconditionally. There are 2 possible reversible circuits with 1-in/out. \( N_1^1 : (x_1) \rightarrow (x_1 \oplus 1) \equiv (1, 2) \) is sufficient to realize these two circuits, i.e. universal for 1-bit circuits. The action of the disjoint cycle of the \( N_1^1 \) gate can be seen on a hypercube of 2 nodes as shown in Fig.1a where the \( N_1^1 \) gate maps vertex-1 to vertex-2 and vice versa. The cascading of two \( N \) gates gives the identity.

**3.2 2-bits Reversible circuits**

For 2-in/out reversible circuits, there are 24 possible circuits. The \( N \) gate cannot be used to synthesize all the 2-in/out reversible circuits. There are two possible \( N \) gates as follows,

\[
\begin{align*}
N_1^2 : (x_1, x_2) &\rightarrow (x_1 \oplus 1, x_2) \equiv (1, 2)(3, 4), \\
N_2^2 : (x_1, x_2) &\rightarrow (x_1, x_2 \oplus 1) \equiv (1, 3)(2, 4).
\end{align*}
\]

These 2 \( N^2 \) gates can realize only 4 possible reversible circuits out of the 24 2-in/out reversible circuits. The action of the disjoint cycle of \( N_1^2 \) and \( N_2^2 \) gates can be seen on a hypercube of 4 nodes as shown in Fig.1b as edge mapping, where \( N_1^2 \) acts as a mapping between edge-(1, 2) and edge-(3, 4), while \( N_2^2 \) acts as a mapping between edge-(1, 3) and edge-(2, 4). No direct vertex mapping using \( N^2 \) gates which is the required mapping for the universality of a library.
Feynman (C) gate, also known as CNOT gate, is a 2-bit gate with control bit and target bit. The C gate flips the target bit if the control bit is set to 1. There are two possible C gates for the 2-in/out reversible circuits as follows,

\[
\begin{align*}
C_{12}^2 & : (x_1, x_2) \rightarrow (x_1, x_2 \oplus x_1) \equiv (3, 4), \\
C_{21}^2 & : (x_1, x_2) \rightarrow (x_1 \oplus x_2, x_2) \equiv (2, 4).
\end{align*}
\]

The action of the disjoint cycles of the \(C_{12}^2\) and \(C_{21}^2\) gates act as vertex mapping on the hypercube of 4 nodes between vertex-3 and vertex-4, and vertex-2 and vertex-4 respectively. A library that contains \(N_2^1, N_2^2, C_{12}^2, C_{21}^2\) is universal for 2-in/out reversible circuits. It can be shown using GAP that a permutation group with generators \(\{N_2^1, C_{12}^2, C_{21}^2\}\) or \(\{N_2^2, C_{12}^2, C_{21}^2\}\) is of size 24, i.e. a gate library that contains \(C_{12}^2\) and \(C_{21}^2\) with any of the \(N_2^i\) gates is universal for 2-in/out reversible circuits.

### 3.3 3-bits Reversible circuits

There are 40320 possible 3-in/out reversible circuits. The N gate and the C gate cannot be used to synthesize all the 3-in/out reversible circuits. There are 3 possible \(N\) gates as follows,

\[
\begin{array}{cccc}
  x_1 & \oplus & \oplus & \oplus \\
  x_2 & \oplus & \oplus & \oplus \\
  x_3 & \oplus & \oplus & \oplus \\
\end{array}
\]

\(N_3^1 : (x_1, x_2, x_3) \rightarrow (x_1 \oplus 1, x_2, x_3) \equiv (1, 5)(2, 6)(3, 7)(4, 8), \\
N_3^2 : (x_1, x_2, x_3) \rightarrow (x_1, x_2 \oplus 1, x_3) \equiv (1, 3)(2, 4)(5, 7)(6, 8), \\
N_3^3 : (x_1, x_2, x_3) \rightarrow (x_1, x_2, x_3 \oplus 1) \equiv (1, 2)(3, 4)(5, 6)(7, 8).
\] (5)

The 3 \(N_3^i\) gates act as face mapping on a hypercube of 8 nodes as shown in Fig. 2-c. \(N_3^1\) is a mapping between left face (LF) and right face (RF), \(N_3^2\) is a mapping between upper face (UF) and down face (DF), and \(N_3^3\) is a mapping between front face (FF) and back face (BF). The \(N\) gate is not universal for 3-in/out reversible circuits since it can realize only 8 possible circuits from the 40320 circuits. For n-in/out reversible circuits, there are \(n\) possible \(N\) gates.

There are 6 possible \(C\) gates for the 3-in/out reversible circuits. They act as edge mapping, for example, \(C_{12}^3\) acts as a mapping between the upper edge and lower edge of RF. A gate library with \(C_3^3\) gates can realize a total of 168 reversible circuits as shown in Table 1. The \(C\) gates for 3-in/out reversible circuits are as follows,

\[
\begin{array}{cccccc}
  x_1 & \oplus & \oplus & \oplus & \oplus & \oplus \\
  x_2 & \oplus & \oplus & \oplus & \oplus & \oplus \\
  x_3 & \oplus & \oplus & \oplus & \oplus & \oplus \\
\end{array}
\]

\(C_{12}^3 : (x_1, x_2, x_3) \rightarrow (x_1, x_2 \oplus x_1, x_3) \equiv (5, 7)(6, 8), \\
C_{13}^3 : (x_1, x_2, x_3) \rightarrow (x_1, x_2, x_3 \oplus x_1) \equiv (5, 6)(7, 8), \\
C_{23}^3 : (x_1, x_2, x_3) \rightarrow (x_1, x_2, x_3 \oplus x_2) \equiv (3, 4)(7, 8), \\
C_{21}^3 : (x_1, x_2, x_3) \rightarrow (x_1 \oplus x_2, x_2, x_3) \equiv (3, 7)(4, 8), \\
C_{32}^3 : (x_1, x_2, x_3) \rightarrow (x_1, x_2 \oplus x_3, x_3) \equiv (2, 4)(6, 8), \\
C_{31}^3 : (x_1, x_2, x_3) \rightarrow (x_1 \oplus x_3, x_2, x_3) \equiv (2, 6)(4, 8).
\] (6)

Toffoli (T3) gate is a 3-bit with 2 control bits and target bit. T3 gate flips the target bit if control bits are set to 1. There are three possible T3 gates for the 3-in/out reversible circuits as follows,
third input is set to 1. For 3-in/out reversible circuits, there are 3 possible libraries with 5 gates, these sub libraries contain the 3 $T$ gates. The smallest sub library contains 5 gates. There are only 3 universal sub libraries. There are only 4 sub libraries that are universal as NT library. The main NT library consists of 6 gates. There are 64 possible sub libraries of gates from the main NT library, not every sub library is universal. There are only 4 sub libraries that are universal for 3-in/out reversible circuits. The smallest universal sub library contains 4 gates. There are only 21 universal sub libraries with 4 gates, for example, a group with generators $\{N^3, T_{321}, T_{3123}, T_{3132}, T_{3312}\}$ is of size 40320. The average size of circuits synthesized with the NT library is 5.865 as shown in Table 4. Using $N^4$ gates, $C^3$ gates and $T^3$ gates form another universal library for 3-in/out reversible circuits known as NCT library. The main NCT library consists of 12 gates. There are 4096 possible sub libraries of gates from the main NCT library. There are only 1960 sub libraries that are universal for 3-in/out reversible circuits. The smallest universal sub library contains 4 gates. There are only 21 universal sub libraries with 4 gates, for example, $\{N^3, C^3_{13}, C^3_{23}, T^3_{1321}\}$ and $\{N^3, C^3_{31}, T^3_{123}, T^3_{132}, T^3_{312}\}$ are universal sub libraries from the NCT library with 4 gates. The average size of circuits synthesized with NCT library is 5.865 as shown in Table 4.

Fredkin ($F$) gate is another 3-bit gate. $F$ gate performs a conditional swap on two of its inputs if the third input is set to 1. For 3-in/out reversible circuits, there are 3 possible $F$ gates as follows,

\[
F^3_{123} : (x_1, x_2, x_3) \rightarrow (x_1, x_3, x_2) \equiv (6, 7), \\
F^3_{132} : (x_1, x_2, x_3) \rightarrow (x_2, x_1, x_3) \equiv (4, 7), \\
F^3_{321} : (x_1, x_2, x_3) \rightarrow (x_2, x_1, x_3) \equiv (4, 6).
\] (8)

The $F$ gate introduces new type of mapping over the hypercube of 8 nodes. The $F$ gate maps vertices over the diagonal of a face, for example, $F^3_{123}$ is a mapping between vertex-6 and vertex-7 over the diagonal of RF. A gate library of $F^3$ gates is not universal since it can realize only 6 3-in/out reversible circuits. A gate library of $N^3$ gates and $F^3$ gates is also not universal since it can realize 1152 circuits out of the 40320 circuits.

The NCF library is a universal library with 12 gates. It has been introduced to get an average size of synthesized circuits of 5.655 better than the NCT library as shown in Table 4. There are 4096 possible sub libraries of the main NCF library with 2460 universal sub libraries. The smallest universal sub library contains 4 gates better than the NT and there are 60 universal sub libraries with 4 gates, for example, the gate libraries $\{N^1, C^1_{13}, F^1_{123}, F^3_{321}\}$ and $\{N^3, C^3_{22}, C^3_{32}, F^3_{321}\}$ are universal for 3-in/out reversible circuits.

Peres ($P$) gate is another 3-bit gate. The function of the $P$ gate combines the function of $T$ gate and $C$ gate in a single gate. For 3-in/out reversible circuits, there are 6 possible $P$ gates as follows,
A little work has been done on the construction of universal libraries for n-bit reversible circuits due to the complexity of the problem. The GT (Generalized Toffoli) library has been proposed. The GT library contain and extended version of T3 gate in addition to the gates in the NCT library, for example, the T4 is a 4-bit gate with 3 control bits and single target bit. The T4 gate flips the target bit if all control bits are

Figure 6: The 6 possible P gates for 3-bit reversible circuits.

The P gate introduces another new type of mapping over the hypercube of 8 nodes. It introduces a full path over the vertices of a plane through the diagonal to visit every vertex and return to the starting vertex. For example, \( P_{23}^3 \) and \( P_{32}^3 \) traverse RF starting from vertex-5, \( P_{13}^3 \) and \( P_{31}^3 \) traverse the DF starting from vertex-3, while \( P_{12}^3 \) and \( P_{21}^3 \) traverse FF starting from vertex-2. A gate library of \( P^3 \) gates is not universal since it can realize only 5040 3-in/out reversible circuits. A gate library of \( P^4 \) gates and \( N^3 \) gates is universal since it can realize the 40320 circuits. The NP library contains 9 gates. There are 512 possible sub libraries of the main NP library with 333 universal sub libraries. The smallest universal sub library contains 3 gates better than NCT and NCF libraries and there are 18 universal sub libraries with 3 gates, for example, the gate libraries \{N_3^3, P_2^3, P_3^3\} and \{N_3^3, P_3^3, P_2^3\} are universal for 3-in/out reversible circuits. The NP library gets an average size of synthesized circuits of 5.516 better than the NCT and the NCF libraries as shown in Table 4.

Many combinations of the above gates have been used to propose different universal reversible libraries, for example, NCP, NCTF, NCPT and NCPF. The main aim of proposing a new universal reversible library is to synthesize circuits with smaller size. It can be easily shown that the higher the number of gates used in the library, the smaller the size of the synthesized circuits. Using many types of gates in a library will produce smaller circuits but will make the implementation of circuits a hard problem.

The NCP library is a universal library with 15 gates. The average size of synthesized circuits is 4.838 as shown in Table 4. There are 32768 possible sub libraries of the main NCP library with 26064 universal sub libraries. The smallest universal sub library contains 3 gates. There are 30 universal sub libraries with 3 gates, for example, the library \{N_3^3, C_{13}^3, P_3^3\} is universal for 3-in/out reversible circuits.

The NCTF library is a universal library with 15 gates. The average size of synthesized circuits of 5.33 as shown in Table 4. There are 32768 possible sub libraries of the main NCTF library with 23132 universal sub libraries. The smallest universal sub library contains 4 gates. There are 105 universal sub libraries with 4 gates, for example, the library \{N_3^3, C_{12}^3, T_{321}, F_{321}\} is universal for 3-in/out reversible circuits.

The NCPT library is a universal library with 18 gates. The average size of synthesized circuits of 4.73 as shown in Table 4. There are 262144 possible sub libraries of the main NCPT library with 217384 universal sub libraries. The smallest universal sub library contains 3 gates. There are 36 universal sub libraries with 3 gates, for example, the library \{N_3^3, P_2^3, T_{3}^{3_{123}}\} is universal for 3-in/out reversible circuits.

The NCPF library is a universal library with 18 gates. The average size of synthesized circuits of 4.597 as shown in Table 4. There are 262144 possible sub libraries of the main NCPF library with 220188 universal sub libraries. The smallest universal sub library contains 3 gates. There are 42 universal sub libraries with 3 gates, for example, the library \{N_2^3, P_3^3, F_{3_{123}}\} is universal for 3-in/out reversible circuits.

3.4 n-bit Reversible Circuits

A little work has been done on the construction of universal libraries for n-bit reversible circuits due to the complexity of the problem. The GT (Generalized Toffoli) library has been proposed. The GT library contain and extended version of T3 gate in addition to the gates in the NCT library, for example, the T4 is a 4-bit gate with 3 control bits and single target bit. The T4 gate flips the target bit if all control bits
are set to 1, the T5 is a 5-bit with 4 control bits and single target bit. The T5 gate flips the target bit if all control bits are set to 1, and so on.

\[
\begin{array}{cccccc}
 n & 1 & 2 & 3 & 4 & 5 \\
 1 & 1 & 2 & & & \\
 2 & 2 & & 6 & & \\
 3 & & 6 & 12 & 4 & \\
 4 & & & 12 & 20 & 5 \\
 5 & 5 & 20 & 30 & 6 & \\
 6 & 6 & 30 & 60 & 105 & 42 \\
 7 & 7 & 42 & 105 & 140 & 105 & 42 \\
\end{array}
\]

Figure 7: The reciprocal of Leibniz Harmonic Triangle.

The GT4 library is the GT library for 4 bits with 32 basic gates. It contains 4 \( N^4 \) gates, 12 \( C^4 \) gates, 12 \( T^3 \) gates and 4 \( T^4 \) gates. The GT5 library is the GT library for 5 bits with 80 basic gates. It contains 5 \( N^5 \) gates, 20 \( C^5 \) gates, 30 \( T^3 \) gates, 20 \( T^4 \) gates and 5 \( T^5 \) gates. The distribution of gates for the \( GT^n \) library is according to the reciprocal of Leibniz Harmonic triangle as shown in Fig.7. The total number of gates for the \( GT^n \) library can be calculated as follows,

\[
\text{num\_gates}(GT^n) = n \sum_{r=0}^{n-1} \binom{n-1}{r},
\]

where \( n \) is the number of bits and \( r \geq 0 \) is the number of controls per gate type, for example, \( r = 0 \) for \( N \) gate and \( r = 1 \) for \( C \) gate. The GT4 library is a universal library with 32 gates. The smallest universal sub library contains 5 gates, for example, the library \{\( N^4, C^4, T^4_{132}, T^4_{1234}, T^4_{12345} \}\) is universal for 4-in/out reversible circuits. The GT5 library is a universal library with 80 gates. The smallest universal sub library contains 6 gates, for example, the library \{\( N^5, C^5, T^5_{123}, T^5_{1234}, T^5_{12345}, T^5_{123452}, T^5_{123455} \}\) is universal for 5-in/out reversible circuits. The GT6 library is a universal library with 192 gates. The smallest universal sub library contains 7 gates, for example, the library \{\( N^6, C^6, T^6_{125}, T^6_{1235}, T^6_{123456}, T^6_{123456} \}\) is universal for 6-in/out reversible circuits.

4 Universal Reversible Gate

This section proposes a universal \( n \)-bit reversible gate for \( n \)-in/out reversible circuits for \( n \geq 2 \). For \( n = 1 \), \( N \) gate is sufficient. The proposed gate is extendable according to the value of \( n \), i.e. an extended \( n \)-bit version of the gate is universal for \( n \)-in/out reversible circuits.

4.1 2-bit Gate

\[
\begin{array}{c}
 x_1 \\
 x_2 \\
 G^2_{12} \quad G^2_{21}
\end{array}
\]

Figure 8: The possible \( G^2 \) gates for 2-bit reversible circuits.

The \( G^2 \) gate is a 2-bit gate. It combines the action of \( N \) and \( C \) in a single gate, i.e. one bit is flipped if the other bit is set to 1 then the second bit is flipped unconditionally. For 2-in/out reversible circuits, there are 2 possible \( G^2 \) gates as follows,

\[
\begin{align*}
G^2_{12} : (x_1, x_2) &\rightarrow (x_1 \oplus 1, x_2 \oplus x_1) \equiv (1, 3, 2, 4), \\
G^2_{21} : (x_1, x_2) &\rightarrow (x_1 \oplus x_2, x_2 \oplus 1) \equiv (1, 2, 3, 4).
\end{align*}
\]

The \( G^2 \) gate introduces a new type of mapping over the hypercube of 4 nodes. It performs a full path mapping over all the vertices of the hypercube through the diagonal to visit every vertex and return to
the starting vertex. It can be shown using GAP that a permutation group with the 2 generators \(G_{212}\) and \(G_{221}\) is of size 24, i.e. a cascade of these two gates are sufficient to implement any of the 24 2-in/out reversible circuits.

4.2 3-bit Gate

The G3 gate is a 3-bit gate. It combines the action of \(N\), \(C\) and \(T3\) in a single gate, i.e. one bit is flipped if the other two bits are set to 1 then second bit is flipped if one of the remaining bits is set to 1. The last bit is flipped unconditionally. For 3-in/out reversible circuits, there are 6 possible G3 gates as follows,

\[
\begin{align*}
G_{3123} &: (x_1, x_2, x_3) \rightarrow (x_1 \oplus 1, x_2 \oplus x_1, x_3 \oplus x_1 x_2) \equiv (1, 5, 3, 7, 2, 6, 4, 8), \\
G_{3132} &: (x_1, x_2, x_3) \rightarrow (x_1 \oplus 1, x_2 \oplus x_1 x_3, x_3 \oplus x_1) \equiv (1, 5, 2, 6, 3, 7, 4, 8), \\
G_{3213} &: (x_1, x_2, x_3) \rightarrow (x_1 \oplus x_2, x_2 \oplus 1, x_3 \oplus x_1 x_2) \equiv (1, 3, 5, 7, 2, 6, 4, 8), \\
G_{3231} &: (x_1, x_2, x_3) \rightarrow (x_1 \oplus x_2 x_3, x_2 \oplus 1, x_3 \oplus x_2) \equiv (1, 3, 2, 4, 5, 7, 6, 8), \\
G_{3312} &: (x_1, x_2, x_3) \rightarrow (x_1 \oplus x_3, x_2 \oplus x_1 x_3, x_3 \oplus 1) \equiv (1, 2, 5, 6, 3, 4, 7, 8), \\
G_{3321} &: (x_1, x_2, x_3) \rightarrow (x_1 \oplus x_2 x_3, x_2 \oplus x_3, x_3 \oplus x_1) \equiv (1, 2, 3, 4, 5, 6, 7, 8).
\end{align*}
\]

The G3 gate introduces a new mapping over the hypercube of 8 nodes. It performs a full mapping path over all the vertices of the hypercube through the edges and the diagonals of different faces to visit every vertex and return to the starting vertex, for example, \(G_{3123}\) starts from vertex-1, traverses BF as follows: \(1 \mapsto 5 \mapsto 3 \mapsto 7\), then go to FF by the mapping \(7 \mapsto 2\), then traverses FF as follows: \(2 \mapsto 6 \mapsto 4 \mapsto 8\), then returns to vertex-1 by the mapping \(8 \mapsto 1\). It can be seen that every G3 traverses the hypercube using 2 opposite faces, for example, \(G_{3123}\) and \(G_{3213}\) traverse the hypercube using BF and FF through different paths, \(G_{3132}\) and \(G_{3312}\) traverse the hypercube using UF and DF, while \(G_{3321}\) and \(G_{3312}\) traverses the hypercube using LF and RF.

It can be shown using GAP that a permutation group with the 6 generators of G3 is of size 40320, i.e. a cascade of these 6 gates are sufficient to implement any 3-in/out reversible circuits. The main G3 gates library consists of 6 gates. There are 64 possible sub libraries of gates from the main G3 library, not every sub library is universal. There are 51 sub libraries that are universal for 3-in/out reversible circuits. The smallest sub library contains 2 gates. There are 9 universal sub libraries with 2 gates, these sub libraries contain any two G3 gates not starting with the same mapping, for example, a library with \(G_{3123}\) and \(G_{3132}\) is not universal since they start by the same mapping \(1 \mapsto 5\), while a library with \(G_{3213}\) and \(G_{3231}\) is universal. It can be verified using GAP that a group with generators \(\{G_{3123}, G_{3213}\}\) is of size 40320. The average size of circuits synthesized with the G3 library is 6.402 as shown in Table 8. This average is better than a comparable library with 6 gates which is \(NT\). The maximum number of gates to realize any 3-in/out reversible circuits is 8 similar to \(NCT\) and \(NCF\) and the size of the gate library is smaller than other gate libraries such as \(NCP\), \(NCTF\), \(NCTP\) and \(NCPF\). The G3 gate library is the only pure gate library that contains only one type of gates. Realization of G3 gates using different gates is shown in Fig.10.

\[
\begin{align*}
x_1 & \quad N \quad \equiv \quad \oplus \quad \equiv \quad \oplus \\
x_2 & \quad C \quad \equiv \quad \ominus \quad \equiv \quad \bigcirc \\
x_3 & \quad T3 \quad \oplus \quad \equiv \quad \oplus \quad \equiv \quad \oplus
\end{align*}
\]

Figure 10: Realization of G3 gate using different gates.
| Lib | Lib Size | #specs |
|-----|----------|--------|
| N   | 3        | 8      |
| C   | 3        | 168    |
| T   | 3        | 24     |
| F   | 3        | 6      |
| P   | 6        | 5040   |
| NF  | 6        | 1152   |
| NT  | 6        | 40320  |
| NP  | 9        | 40320  |
| NCT | 12       | 40320  |
| NCF | 12       | 40320  |
| NCN | 15       | 40320  |
| NCTF| 15       | 40320  |
| NCP | 15       | 40320  |
| NCTF| 18       | 40320  |
| NCPF| 18       | 40320  |
| G3  | 6        | 40320  |

Table 1: The universality of different libraries for 3-in/out reversible circuits.

| Lib | Lib Size | Num of Sub Libs | Num of Uni Sub Libs | Utilization |
|-----|----------|------------------|----------------------|-------------|
| NT  | 6        | 64               | 4                    | 6.25%       |
| NP  | 9        | 512              | 333                  | 65%         |
| NCT | 12       | 4096             | 1960                 | 47.85%      |
| NCF | 12       | 4096             | 2460                 | 60.00%      |
| NCP | 15       | 32768            | 26064                | 79.54%      |
| NCTF| 15       | 32768            | 23132                | 70.59%      |
| NCP | 18       | 262144           | 217384               | 82.92%      |
| NCPF| 18       | 262144           | 220188               | 83.99%      |
| G3  | 6        | 64               | 51                   | 79.68%      |

Table 2: Utilization of gates in universal sub libraries.

| Size of min Uni Sub Lib | Num of Sub Libs with min size | Num of Uni Sub Libs with min size | Utilization |
|-------------------------|-------------------------------|-----------------------------------|-------------|
| NT                      | 5                             | 6                                 | 50%         |
| NP                      | 3                             | 84                                | 21.42%      |
| NCT                     | 4                             | 495                               | 4.24%       |
| NCF                     | 4                             | 495                               | 12.12%      |
| NCP                     | 3                             | 455                               | 6.59%       |
| NCTF                    | 4                             | 1365                              | 7.69%       |
| NCPT                    | 3                             | 816                               | 4.41%       |
| NCPF                    | 3                             | 816                               | 5.14%       |
| G3                      | 2                             | 15                                | 60%         |

Table 3: Utilization of gates in smallest universal sub libraries for 3-in/out reversible circuits.
| Min Len | NT | NP | NCT | NCF | NCP | NCTF | NCPT | NCPF | G3 |
|---------|----|----|-----|-----|-----|------|------|------|----|
| 0       | 1  | 1  | 1   | 1   | 1   | 1    | 1    | 1    | 0  |
| 1       | 6  | 9  | 12  | 12  | 15  | 18   | 18   | 18   | 6  |
| 2       | 24 | 69 | 102 | 101 | 174 | 143  | 228  | 248  | 36 |
| 3       | 88 | 502| 625 | 670 | 1528| 1006 | 1993 | 2356 | 207|
| 4       | 296| 3060|2780|3413|8968|5021|10503|12797|1097|
| 5       | 870|13432|8921|11378|23534|15083|23204|27974|4946|
| 6       | 2262|21360|17049|17970|6100|17261|4733|2106|13819|
| 7       | 5097|1887|10253|6759|0|1790|0|0|14824|
| 8       | 9339|0|577|30|0|0|0|0|5208|
| 9       | 12237|0|0|0|0|0|0|0|
| 10      | 8363|0|0|0|0|0|0|0|
| 11      | 1690|0|0|0|0|0|0|0|
| 12      | 47  |0|0|0|0|0|0|0|
| Avg     | 8.5 |5.516|5.865|5.655|4.838|5.33|4.73|4.597|6.402|
| LibSize | 6   |9  |12  |12  |15  |15   |18   |18   |6  |

Table 4: Minimum size of 3-bit reversible circuits using different libraries.

4.3 n-bit Reversible Gate

The G4 gate is a 4-bit gate. It combines the action of N, C, T3 and T4 in a single gate, i.e. one bit is flipped if the other three bits are set to 1, then the second bit is flipped if two of the remaining bits are set to 1, then the third bit is flipped if the remaining bit is set to 1. The last bit is flipped unconditionally. For 4-in/out reversible circuits, there are 24 possible G4 gates as follows,

\[
G_{1234} : (x_1, x_2, x_3, x_4) \rightarrow (x_1 \oplus 1, x_2 \oplus x_1, x_3 \oplus x_1 x_2, x_4 \oplus x_1 x_2 x_3), \\
G_{1243} : (x_1, x_2, x_3, x_4) \rightarrow (x_1 \oplus 1, x_2 \oplus x_1, x_3 \oplus x_1 x_2 x_4, x_4 \oplus x_1 x_2), \\
G_{1324} : (x_1, x_2, x_3, x_4) \rightarrow (x_1 \oplus 1, x_2 \oplus x_1, x_3 \oplus x_1 x_2 x_4, x_4 \oplus x_1 x_2), \\
G_{1342} : (x_1, x_2, x_3, x_4) \rightarrow (x_1 \oplus 1, x_2 \oplus x_1 x_4, x_3 \oplus x_1 x_2, x_4 \oplus x_1), \\
G_{1423} : (x_1, x_2, x_3, x_4) \rightarrow (x_1 \oplus 1, x_2 \oplus x_1 x_4, x_3 \oplus x_1 x_2 x_4, x_4 \oplus x_1 x_2), \\
G_{1432} : (x_1, x_2, x_3, x_4) \rightarrow (x_1 \oplus 1, x_2 \oplus x_1 x_4 x_3, x_3 \oplus x_1 x_4, x_4 \oplus x_1), \\
G_{2134} : (x_1, x_2, x_3, x_4) \rightarrow (x_1 \oplus 1, x_2 \oplus x_1 x_3, x_3 \oplus x_1 x_2, x_4 \oplus x_2 x_3 x_1), \\
G_{2143} : (x_1, x_2, x_3, x_4) \rightarrow (x_1 \oplus 1, x_2 \oplus x_1 x_3, x_3 \oplus x_1 x_2 x_4, x_4 \oplus x_2 x_3), \\
G_{2314} : (x_1, x_2, x_3, x_4) \rightarrow (x_1 \oplus 1, x_2 \oplus x_1 x_4 x_3, x_3 \oplus x_1 x_2, x_4 \oplus x_2 x_3 x_1), \\
G_{2341} : (x_1, x_2, x_3, x_4) \rightarrow (x_1 \oplus 1, x_2 \oplus x_1 x_3 x_4, x_3 \oplus x_1 x_2, x_4 \oplus x_2 x_3 x_1), \\
G_{2413} : (x_1, x_2, x_3, x_4) \rightarrow (x_1 \oplus 1, x_2 \oplus x_1 x_3 x_4 x_3, x_3 \oplus x_1 x_2 x_4, x_4 \oplus x_2 x_3 x_1 x_4), \\
G_{2431} : (x_1, x_2, x_3, x_4) \rightarrow (x_1 \oplus 1, x_2 \oplus x_1 x_3 x_4 x_3 x_1, x_3 \oplus x_1 x_2 x_4, x_4 \oplus x_2 x_3 x_1 x_4), \\
G_{3124} : (x_1, x_2, x_3, x_4) \rightarrow (x_1 \oplus 1, x_2 x_3, x_2 \oplus 1, x_3 \oplus x_2 x_4 x_1, x_4 \oplus x_2 x_3 x_1), \\
G_{3142} : (x_1, x_2, x_3, x_4) \rightarrow (x_1 \oplus 1, x_2 x_4, x_2 \oplus 1, x_3 \oplus x_2 x_4 x_1, x_4 \oplus x_2 x_3 x_1), \\
G_{3214} : (x_1, x_2, x_3, x_4) \rightarrow (x_1 \oplus 1, x_2 x_3, x_3 \oplus 1, x_4 \oplus x_2 x_3 x_1, x_4 \oplus x_2 x_3 x_1), \\
G_{3241} : (x_1, x_2, x_3, x_4) \rightarrow (x_1 \oplus 1, x_2 x_3, x_3 x_1, x_4 \oplus x_2 x_3 x_1, x_4 \oplus x_2 x_3 x_1), \\
G_{3412} : (x_1, x_2, x_3, x_4) \rightarrow (x_1 \oplus 1, x_2 x_3, x_3 x_1 x_4, x_4 \oplus x_2 x_3 x_1, x_4 \oplus x_2 x_3 x_1), \\
G_{3421} : (x_1, x_2, x_3, x_4) \rightarrow (x_1 \oplus 1, x_2 x_3, x_3 x_1 x_4 x_3, x_4 \oplus x_2 x_3 x_1, x_4 \oplus x_2 x_3 x_1), \\
G_{4123} : (x_1, x_2, x_3, x_4) \rightarrow (x_1 \oplus 1, x_2 x_3 x_4, x_2 \oplus 1, x_3 \oplus x_2 x_4 x_1, x_4 \oplus x_2 x_3 x_1), \\
G_{4132} : (x_1, x_2, x_3, x_4) \rightarrow (x_1 \oplus 1, x_2 x_3 x_4, x_3 \oplus 1, x_4 \oplus x_2 x_3 x_1, x_4 \oplus x_2 x_3 x_1), \\
G_{4213} : (x_1, x_2, x_3, x_4) \rightarrow (x_1 \oplus 1, x_2 x_3 x_4, x_3 \oplus x_1 x_2 x_4, x_4 \oplus x_2 x_3 x_1), \\
G_{4231} : (x_1, x_2, x_3, x_4) \rightarrow (x_1 \oplus 1, x_2 x_3 x_4, x_3 \oplus x_1 x_2 x_4 x_3, x_4 \oplus x_2 x_3 x_1), \\
G_{4312} : (x_1, x_2, x_3, x_4) \rightarrow (x_1 \oplus 1, x_2 x_3 x_4, x_3 \oplus x_1 x_2 x_4 x_3 x_1, x_4 \oplus x_2 x_3 x_1), \\
G_{4321} : (x_1, x_2, x_3, x_4) \rightarrow (x_1 \oplus 1, x_2 x_3 x_4, x_3 \oplus x_1 x_2 x_4 x_3 x_1 x_4, x_4 \oplus x_2 x_3 x_1). 
\] (13)
\[ G_{1234} : (1, 9, 5, 13, 3, 11, 7, 15, 2, 10, 6, 14, 4, 12, 8, 16), \]
\[ G_{1243} : (1, 9, 5, 13, 2, 10, 6, 14, 3, 11, 7, 15, 4, 12, 8, 16), \]
\[ G_{1324} : (1, 9, 3, 11, 5, 13, 7, 15, 2, 10, 4, 12, 6, 14, 8, 16), \]
\[ G_{1342} : (1, 9, 2, 10, 5, 13, 6, 14, 3, 11, 4, 12, 7, 15, 8, 16), \]
\[ G_{1423} : (1, 9, 3, 11, 2, 10, 4, 12, 5, 13, 7, 15, 6, 14, 8, 16), \]
\[ G_{1432} : (1, 9, 2, 10, 3, 11, 4, 12, 5, 13, 6, 14, 7, 15, 8, 16), \]
\[ G_{2134} : (1, 5, 9, 13, 3, 7, 11, 15, 2, 6, 10, 14, 4, 8, 12, 16), \]
\[ G_{2143} : (1, 5, 9, 13, 2, 6, 10, 14, 3, 7, 11, 15, 4, 8, 12, 16), \]
\[ G_{2143} : (1, 5, 9, 13, 2, 6, 10, 14, 3, 7, 11, 15, 4, 8, 12, 16), \]
\[ G_{2314} : (1, 3, 9, 11, 5, 7, 13, 15, 2, 4, 10, 12, 6, 8, 14, 16), \]
\[ G_{2341} : (1, 2, 9, 10, 5, 6, 13, 14, 3, 4, 11, 12, 7, 8, 15, 16), \]
\[ G_{2413} : (1, 3, 9, 11, 2, 4, 10, 12, 5, 7, 13, 15, 6, 8, 14, 16), \]
\[ G_{2431} : (1, 2, 9, 10, 3, 4, 11, 12, 5, 6, 13, 14, 7, 8, 15, 16), \]
\[ G_{3124} : (1, 5, 3, 7, 9, 13, 11, 15, 2, 6, 4, 8, 10, 14, 12, 16), \]
\[ G_{3142} : (1, 5, 2, 6, 9, 13, 10, 14, 3, 7, 4, 8, 11, 15, 12, 16), \]
\[ G_{3214} : (1, 5, 3, 7, 9, 11, 13, 15, 2, 4, 6, 8, 10, 12, 14, 16), \]
\[ G_{3241} : (1, 2, 5, 6, 9, 10, 13, 14, 3, 4, 7, 8, 11, 12, 15, 16), \]
\[ G_{3412} : (1, 3, 2, 4, 9, 11, 10, 12, 5, 7, 6, 8, 13, 15, 14, 16), \]
\[ G_{3421} : (1, 2, 3, 4, 9, 10, 11, 12, 5, 6, 7, 8, 13, 14, 15, 16), \]
\[ G_{4123} : (1, 5, 3, 7, 2, 6, 4, 8, 9, 13, 11, 15, 10, 14, 12, 16), \]
\[ G_{4132} : (1, 5, 2, 6, 3, 7, 4, 8, 9, 13, 10, 14, 11, 15, 12, 16), \]
\[ G_{4213} : (1, 3, 5, 7, 2, 4, 6, 8, 9, 11, 13, 15, 10, 12, 14, 16), \]
\[ G_{4231} : (1, 2, 5, 6, 3, 4, 7, 8, 9, 10, 13, 14, 11, 12, 15, 16), \]
\[ G_{4312} : (1, 3, 2, 4, 5, 7, 6, 8, 9, 11, 10, 12, 13, 15, 14, 16), \]
\[ G_{4321} : (1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16). \]

Extending the $G$ gate for $n$-bits is trivial as shown in Fig. 11. It can be shown using GAP that a permutation group with the $n!$ generators of $G_n$ is of size $2^{n!}$, i.e., a cascade of these $n!$ gates are sufficient to implement any $n$-in/out reversible circuits.

![Figure 11: Extensions of $G_n$ gate.](image)

The main $G_n$ gates library consists of $n!$ gates. There are $2^{n!}$ possible sub libraries of gates from the main $G_n$ library. The smallest universal sub library always contains only 2 gates, for example, the sub library \{G_{42341}, G_{41234}\} is universal for 4-in/out reversible circuits. The sub library \{G_{512345}, G_{423451}\} is universal for 5-in/out reversible circuits and the sub library \{G_{624561}, G_{654326}\} is universal for 6-in/out reversible circuits. It has been verified for $n \leq 10$ using a random gate generator on GAP that a sub library with 2 gates of size $n$ is universal for $n$-in/out reversible circuits.

## 5 Conclusion

Circuit implementation using a single type of gates is much easier than using a gate library with more than one gate type. The paper showed that common universal libraries should contain more than one gate type. This paper proposed a new gate type that is universal for $n$-in/out reversible circuits.

There is no systematic method to extend existing universal libraries to work over higher order circuits. The proposed gate is extendable in a trivial way to work over $n$-bit reversible circuits.
There is a trade-off between the number of gates used in a universal library and the size of the synthesized circuit. The paper showed that only 2 combinations of size $n$ of the proposed gate can be used to synthesize any arbitrary $n$-in/out reversible circuits. Using only 2 gates in the library might not produce a short circuit, i.e. the cascading of gates might be too long. The analysis of universal sub-libraries for the proposed gate and the existing hybrid universal sub-libraries to find the best sub-library with minimum number of gates that produce an efficient circuit is an extension to this work.

References

[1] C. Bennett. Logical reversibility of computation. *IBM Journal of Research and Development*, 17(6):525–532, 1973.

[2] J.D. Dixon and B. Mortimer Permutation groups. New York: Springer, 1996.

[3] A. De Vos, B. Desoete, A. Adamski, P. Pietrzak, M. Sibinski, and T. Widerski. Design of reversible logic circuits by means of control gates. In *Proceedings of the 10th International Workshop on Integrated Circuit Design, Power and Timing Modeling, Optimization and Simulation*, pages 255-264, 2000.

[4] A. De Vos, B. Raa and L. Storme Generating the group of reversible logic gates. Journal of Physics A: Mathematical and General, 35(33): 7063–7078, 2002.

[5] A. De Vos and Y. V. Rentergem From Group Theory to Reversible Computers. International Journal of Unconventional Computing, 4(1): 79-88, 2008.

[6] A. De Vos and S. De Baerdemacker Symmetry Groups for the Decomposition of Reversible Computers, Quantum Computers, and Computers in between. *Symmetry*, 3(2): 305-324, 2011.

[7] A. De Vos, B. Desoete, F. Janiak, and A. Nogawski. Control gates as building blocks for reversible computers. In *Proceedings of the 11th International Workshop on Power and Timing Modeling, Optimization and Simulation*, pages 9201–9210, 2001.

[8] G. W. Dueck and D. Maslov. Reversible function synthesis with minimum garbage outputs. In *Proceedings of the 6th International Symposium on Representations and Methodology of Future Computing Technologies*, pages 154–161, 2003.

[9] E. Fredkin and T. Toffoli. Conservative logic. *International Journal of Theoretical Physics*, 21:219–253, 1982.

[10] The GAP Group. GAP – Groups, Algorithms, and Programming, Version 4.6.3; 2013. [http://www.gap-system.org](http://www.gap-system.org)

[11] O. Golubitsky and S.M. Falconer and D. Maslov. Synthesis of the optimal 4-bit reversible circuits. In *Proceedings of the 47th Design Automation Conference*, pages 653-656, 2010.

[12] J. Gruska. *Quantum Computing*. McGraw-Hill, London, 1999.

[13] K. Iwama, Y. Kambayashi, and S. Yamashita. Transformation rules for designing CNOT–based quantum circuits. In *Proceedings of the 39th Conference on Design Automation*, pages 419–424. ACM Press, 2002.

[14] M.I. Kargapolov and Ju.I. Merzljakov Fundamentals of the theory of groups. Berlin: Springer, 1979.

[15] D. Maslov, G. W. Dueck, and D. M. Miller. Fredkin/Toffoli templates for reversible logic synthesis. In *Proceedings of the ACM/IEEE International Conference on Computer-Aided Design*, page 256, 2003.

[16] D. Maslov, G. W. Dueck, and D. M. Miller. Simplification of Toffoli networks via templates. In *Proceedings of the 16th Symposium on Integrated Circuits and Systems Design*, page 53, 2003.

[17] D. Maslov and C. Young and D. M. Miller and G. W. Dueck. Quantum circuit simplification using templates. Design, Automation and Test in Europe, pages 1208-1213, 2005.
[18] D. Maslov. Reversible logic synthesis benchmarks. [Online]. Available: http://www.cs.uvic.ca/~dmaslov/.

[19] D. M. Miller and G. W. Dueck. Spectral techniques for reversible logic synthesis. In Proceedings of the 6th International Symposium on Representations and Methodology of Future Computing Technologies, pages 56–62, 2003.

[20] D. M. Miller, D. Maslov, and G. W. Dueck. A transformation based algorithm for reversible logic synthesis. In Proceedings of the 40th Conference on Design Automation, pages 318–323, 2003.

[21] M. Nielsen and I. Chuang. Quantum Computation and Quantum Information. Cambridge University Press, Cambridge, United Kingdom, 2000.

[22] A. K. Prasad and V. V. Shende and K. N. Patel and I. L. Markov and J. P. Hayes. Data structures and algorithms for simplifying reversible circuits. J. Emerg. Technol. Comput. Syst., 2(4), October 2006.

[23] V. V. Shende, A. K. Prasad, I. L. Markov, and J. P. Hayes. Synthesis of reversible logic circuits. IEEE Trans. on CAD, 22(6):710–722, 2003.

[24] L. Storme, A. De Vos, G. Jacobs Group Theoretical Aspects of Reversible Logic Gates. Journal of Universal Computer Science, 5(5): 307–321, 1999.

[25] T. Toffoli. Reversible computing. In W. de Bakker and J. van Leeuwen, editors, Automata, Languages and Programming, page 632. Springer, New York, 1980. Technical Memo MIT/LCS/TM-151, MIT Lab for Computer Science (unpublished).

[26] G. Yang, X. Song, W. N.N. Hung, M. A. Perkowski, and C.-J. Seo. Synthesis of reversible circuits with minimal costs. CALCOLO, 45:193–206, 2008.