THIN-FILM SILICON FIELD-EFFECT TRANSISTORS FOR SENSOR MICROSYSTEMS

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The electrodes of the transistor on both sides of the transistor are possible in the thin-layer single-crystal film. Thus, in the structure shown in Figure 1, due to the location of the common source in front of the shutter, the effective length of the channel is reduced by half and, accordingly, the same number of times the speed increases. However, this technology of forming thin-film field-effect transistors is quite complex and expensive.

![Fig. 1. The structure of a thin-field field-effect transistor with a halved channel length](image)

The technology of thin-film transistors (TFT) based on amorphous or polycrystalline silicon is much simpler and cheaper. Interest in such transistors has grown somewhat in recent years due to the technological compatibility with liquid crystal elements of flat screens, displays with elements of amorphous silicon solar cells, as well as the possibility of creating three-dimensional integrated circuits and control units for image sensor arrays. From the point of view of high-speed film transistors, there is no prospect for non-single-crystal material due to the low mobility of charge carriers (0.1–10) cm² / V·s in the amorphous (15–100) cm² / V·s in the Si-field. However, the possibility of increasing the degree of integration in Integrated Circuits, reducing parasitic capacitance, channel length and, finally, obtaining three-dimensional integration of thin-film transistors with promising elements of high-speed Large Integrated Circuits.

In addition, progress is possible in the single crystallization of film transistors, such as laser recrystallization, and may eventually bring them to the forefront of high-speed ultrahigh frequency electronics.
Therefore, we consider the physical and technological features of TFT formation on amorphous silicon, on polycrystalline silicon, and on the SOI structure.

Figure 2, shows the basic structure of TFT on amorphous silicon (α-Si:H). Designed to switch currents, such transistors had a ratio of currents in the open and closed states of more than 5-6 orders of magnitude, and the current through the gate per unit width of the gate length of 10 micrometer was $10^{-8}$ A/μm. The effective mobility in TFT with a shutter length $\lambda = 1 \, \mu m$ was only $1 \, \text{cm}^2 / \text{V} \cdot \text{s}$.

![TFT on amorphous α-Si:H(1-gate insulator,2-glass substrate,3-gate).](image)

The main feature of the physics of TFT on α-Si is the presence of the tail of localized states of mobility and many centers of capture in the forbidden zone. The tail of such localized states determines the characteristics of the device at voltages above the threshold, and the distribution of impurity levels - the very value of the threshold voltage $V_{Ti}$ characteristics at voltages below the threshold. Depending on the specific technological conditions of the formation of the structure of the TFT law, the distribution of impurity levels and tails of localized states in the forbidden zone can differ significantly. This difference in technology determines the difference between the theoretical models of TFT.

Due to the high density of surface states at the interface α-Si - insulator, the value of the threshold voltages of TFT is quite large (5-10V). Due to the low mobility and small number of large charge carriers, the typical value of the drain current is hundreds of microamperes per millimeter of shutter gate of about ten volts.

Experimental TFTs were also formed on so-called hydrogenated amorphous silicon (α-Si:H). To reduce the resistance of the drain-source in the open state, the distance between them is realized at a minimum of about 1 μm, and the resistance of the drain-source areas is reduced by multi-charge implantation of phosphorus (P ++). SiO$_2$ or Si$_3$N$_4$ of different composition, formed by different methods, is used as an insulator in the gate. Slow degradation of TFT under the action of applied voltage (electric formation) was observed in experimental samples, which is due to both the change in the number of metastable fast states α-Si:H and the number of slow charge capture in silicon nitride (Si$_3$N$_4$) or SiO$_2$. This is a big disadvantage of TFT. This instability is due to the frequency of hydrogen used in the formation of α-Si:H.

As a substrate for TFT on α-Si use glass, monocrystalline silicon, sital with a thermally grown layer of SiO$_2$ (Al$_2$O$_3$).

The gate, as shown in Fig. 2, is usually created in the substrate, which allows you to make a small gap between the drain-source areas, and, accordingly, the resistance in the open state. To improve the parameters of TFT, it is advisable to use the technology of qualitative formation of α-Si:H.

TFT in the field - Si. Despite the relatively simple low-temperature technology of obtaining TFT on α-Si, such TFT can be used only at low frequencies due to the low mobility of electrons ($\mu < t \, \text{cm}^2 / \text{V} \cdot \text{s}$). TFT in the field - Si have ample opportunities
for use in modern electronic circuits, as the field mobility of electrons can already reach 100 cm$^2$/V·s. However, such a high value of mobility was obtained using a high-temperature process of forming poly-Si (630°C), which is incompatible with the use of inexpensive glass as a substrate. This high-temperature technology also makes it difficult to use poly-Si in TFT as an active load of logic elements in digital IC. We have developed a low-temperature (<580 °C) technology for the deposition of poly-Si by the decomposition of disilane Si$_2$H$_6$ in a low-pressure reactor on borosilicate glass. The grain size of the field-Si is 10–50 nm. The length and width of the channel between the drain-source regions using this technology were 10 and 15 μm, respectively, and the threshold voltage was 3–8V, which is slightly lower than in the TFT on α-Si:H. The ratio of the current in the open state to the current in the closed state reached $10^4$ (4 orders of magnitude), and the field mobility was 50–80 CM$^2$/V·c.

The main feature of charge transfer through the Si-field, which determines the volt-ampere characteristics of TFT, are the so-called intercrystalline potential barriers (between grains) and capture centers at the grain boundaries. The height of such a potential barrier $\varepsilon_b$ determines the magnitude of the field mobility of charge carriers ($\mu e = \exp \cdot \varepsilon_b/kT$) and is formed by charges at the capture centers at the grain boundaries. The electrophysical parameters of poly-Si can be changed by means of both photonic and laser annealing with a change in grain size, and recrystallization of poly-Si in mono-Si.

A significant reduction in the parasitic capacitances of the FT by removing the bond through the substrate can be achieved by forming transistor structures on single-crystal epitaxially grown silicon films on the insulating substrate. Such structures, which are called silicon on the insulator (SOI) are made of sapphire (SOS), spianel, Si$_3$N$_4$, SiO$_2$. So far, due to the imperfection of the epichars and the boundary of the silicon-substrate section, it has not been possible to create a high-steep FT. However, when using low-temperature epitaxy in electron-cyclotron resonance reactors and multi-charge high-energy ion implantation, it is possible to raise the quality of SOI and form FT as high-speed transistors.

Figure 3 shows a diagram of the technical section of TFT SOI, formed on a silicon substrate: A feature of such a transistor is an ultra-thin active layer of intrinsic silicon (100 - 150 nm).

![Diagram of TFT SOI](image)

Fig. 3. The structure of TFT, formed on the basis of mono-Si grown on the insulator (SOI).

Due to the ultra-thin layer of mono-Si in such a transistor, the effects associated with the shortening of the channel (0.5 μm) are very weak. The second feature of this
structure, shown in Fig. 3, is the presence of MOS-gate not only on the upper side of the active layer of mono-Si, but on the side of the substrate, which opened new functionalities for the use of such a transistor in three-dimensional circuits. The presence of a floating substrate reduces the skin effect and increases the slope of the transistor in the subthreshold region. The great advantage of this technology is that it allows to form complementary pairs of transistors with a small switching time ($\tau_D = 36-50\text{ps}$) at a channel length of 1 $\mu\text{m}$.

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АНАЛІЗ ВПЛИВУ ВИСОТИ ПАДІННЯ ЧАСТИНКИ ПРОМИВНОГО РОЗЧИНИ ТА КУТА НАХИЛУ ВІБРОПЛОЩИНИ НА ЕФЕКТИВНІСТЬ ЙОГО ОЧИЩЕННЯ БУРОВИМ ВІБРОСИТОМ

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Промивний розчин зі свердловини подається на обладнання системи очищення. Першим етапом очищення промивного розчину є бурове вібросито, де відбувається грубе очищення від частинок найбільшого діаметра (розміром до 75 мкм) [1]. Промивний розчин потрапляє на віброплощину з завантажувального бункера (накопичувальної ємності), яка розміщена на деякій відділі $h$ від ситополотна (рис. 1).

Чим більша віддала $h$, тим більшу початкову швидкість $v_0$ отримує частина. Ця швидкість визначається як $v_0 = \sqrt{2gh}$, де $g$ – прискорення вільного падіння. В кожен момент часу віддала $h$ змінюється, оскільки вібросито пересміщується на величину амплітуди коливань $A$, тобто максимальне значення становить $h$, а мінімальне буде рівне величині $h_1=h-A$. Отже, початкова швидкість частинки промивного розчину змінюватиметься в залежності від положення вібросито: в нижньому положенні вона буде максимальною ($v_0$ на рис.2), а в верхньому – мінімальною ($v_1$ на рис.2). Величина $h$ обмежується висотою буртиків вібросито, оскільки після відбиття частинка від вібросито можливи виліт за межі робочої зони. Зі збільшенням висоти підйому бункера $h$ над віброситом початкова швидкість руху частинки зростатиме (рис. 2). За