Resistive Switching Characteristics of Al/Si$_3$N$_4$/p-Si MIS-Based Resistive Switching Memory Devices

Hee-Dong Kim,* Min Ju Yun and Sungho Kim†

Department of Electrical Engineering, Sejong University, Seoul 05006, Korea

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In this study, we proposed and demonstrated a self-rectifying property of a silicon nitride (Si$_3$N$_4$)-based resistive random access memory (RRAM) device by employing p-type silicon (p-Si) as the bottom electrode. The RRAM devices consisting of Al/Si$_3$N$_4$/p-Si are fabricated by using a low-pressure chemical-vapor deposition and exhibited an intrinsic diode property with non-linear current–voltage (I–V) behavior. In addition, compared to the conventional metal/insulator/metal (MIM) structure of Al/Si$_3$N$_4$/Ti RRAM cells, the operating current over the entire bias region for the proposed metal/insulator/semiconductor (MIS) cells is dramatically lower because the introduced p-Si bottom electrode efficiently suppresses the current in both the low- and the high resistance states. Then, the results mean that when p-Si is employed as a bottom electrode, the Si$_3$N$_4$-based RRAM cells can be applied to selector-free RRAM cells.

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I. INTRODUCTION

Currently, many researchers have tried to explore a new memory concept, i.e., two-terminal resistance-change-based memories because the size of conventional capacitance-based nonvolatile memory (NVM) memory cells will be approaching its scaling limit [1, 2]. Among various kinds of new memory concepts, resistive-switching random-access memories (RRAM) consisting of various metal oxides and metal nitrides have been proposed as very promising candidates because of their simple metal/insulator/metal (MIM) structures, low-voltage and high-speed operation, and high density features [3,4]. Nevertheless, some issues in respect of reliability should be solved if new NVMs are to be realized in terms of unit-cell and array-cell levels. First, in the unit cell, the current levels for SET and RESET operations should be lowered below the sub-micro-ampere level to reduce power consumption and improve device’s reliability, such as endurance, by optimizing the active layer and the structures of RRAM devices [5]. That is, if variations in the operating parameters are to be reduced, more reliable deposition methods to achieve uniform resistive switching (RS) films, such as atomic layer deposition (ALD) or chemical vapor deposition (CVD), should be employed in place of physical vapor deposition (PVD) because achieving uniform RS films on entire wafer is very difficult when the conventional PVD method is used [6]. Moreover, in an array, the disturbance (or crosstalk) induced at junctions between neighboring cells should be controlled because leakage paths are formed due to reversely-biased cells [7]. In relevant work experience, some kinds of selectors, for example, extrinsic diodes in unipolar mode cells or transistors combined with bipolar RS (BRS) cells, have been investigated to solve the issue [8,9], which is the so-called one diode-one resistor (1D1R) or the one transistor-one resistor (1T1R). However, the 1D1R and the 1T1R structures with increased feature cell sizes in an array might be a shortcoming in terms of the device’s integration and mass production. Therefore, if stored data is to be protected from the leakage current during the reading operation and the current read-margin is to be increased, RRAM architectures having self-selector function should be realized.

To capture BRS cells into an array structure, in this work, we investigate the RS behavior for a current limiter with an Al/Si$_3$N$_4$/p-Si structure for the applications are a RRAM by using CVD method, which can provide a film of more reliable quality for the active layer compared to the conventional PVD method. In this structure, the Si$_3$N$_4$ layer exhibits BRS behaviors while the p-Si bottom electrode acts as a bottom electrode, as well as the selector (or current limiter), in the positive bias region. The electrical properties, as well as read margins, were investigated.

*E-mail: khd0708@sejong.ac.kr; Fax: +82-2-3408-4329
†E-mail: sungho85.kim@sejong.ac.kr; Fax: +82-2-3408-4329
II. EXPERIMENTS AND DISCUSSION

For fabricating the metal-insulator-silicon (MIS) sample preparation, we used (100)-oriented p-type silicon (p-Si) wafers as the starting substrates, which acted as bottom electrodes in this system. An 8-nm-thick Si$_3$N$_4$ layer was subsequently deposited by using low-pressure CVD (LPCVD) at 750 °C by using the reaction of dichlorosilane (SiCl$_2$H$_2$) with ammonia (NH$_3$) gas. Then, the Si$_3$N$_4$/p-Si structure was cleaned by using a standard sulfuric acid and hydro-peroxide mixture (SPM) for 10 min. The thicknesses of the Si$_3$N$_4$ stacks were confirmed to be 8 nm by using spectroscopic ellipsometry and α-step profiling. Then, the X-ray diffraction (XRD) patterns for the Si$_3$N$_4$ films were measured to reveal their structural properties. Figure 1(c) shows that the Si$_3$N$_4$ films have a face-centered cubic crystal structure, with the marked diffraction peak observed at 36.5°, 42.2° and 53.6° originating from the 220, 311 and 400 planes, in the scanned range of 30° – 60°. To confirm the roughness of the Si$_3$N$_4$ films, the surface morphology of the Si$_3$N$_4$ films, we used atomic force microscopy (AFM) to observe and the results are as shown in Fig. 1(d). The AFM micrograph shows that the Si$_3$N$_4$ films were uniform deposited with a root-mean-square (RMS) surface roughness of ~4 nm over a 500 × 500 nm$^2$ area. After the films had been dried in nitrogen gas, we continually deposited a 100-nm-thick top Al electrode with a 100-μm diameter by using a sputtering system, and we made a bottom indium (In) contact on the substrate for an Ohmic contact. Figure 1(a) shows the finished structures of proposed Al/Si$_3$N$_4$/p-Si cells. In addition, in order to compare the MIS-based RRAMs with the MIM-based RRAMs, we additionally fabricated Al/Si$_3$N$_4$/Ti structures, as shown in Fig. 1(b). The electrical properties of the RRAM samples were measured by using a Keithley 4200 semiconductor parameter analyzer.

First, to study the BRS properties of the Al/Si$_3$N$_4$/p-Si (MIS) and the Al/Si$_3$N$_4$/Ti (MIM) RRAM cells, we investigated their dc current—voltage ($I$ – $V$) characteristics at room temperature. In the Al/Si$_3$N$_4$/Ti RRAM cells, in virgin state (i.e. the high resistance state (HRS)) we performed the forming process in the positive bias region, and the forming was observed at +7 V. Then, the BRS is achieved by sweeping dc $I$ – $V$ in the following
Fig. 2. (Color online) $I - V$ characteristics of (a) the Al/Si$_3$N$_4$/Ti structure and (b) the proposed Al/Si$_3$N$_4$/p-Si structure on a linear scale.

sequence: $0\text{ V} \rightarrow -1\text{ V} \rightarrow 0\text{ V} \rightarrow +1\text{ V} \rightarrow 0\text{ V}$, as shown in Fig. 2(a). A SET process from the HRS to the low resistance state (LRS) is performed at around $+0.7\text{ V}$ with a compliance current (CC) of 100 mA. For example, the RRAM cell can be switched from the HRS to the LRS. Subsequently, the current of the cell gradually drops at about around $-0.7\text{ V}$ when the bias voltage is swept in the negative voltage region, indicating that the state is switched back from the LRS to the HRS. On the other hand, the MIS samples also exhibits a BRS behavior in the dc $I - V$ curve when the voltage is swept in the following sequence: $0\text{ V} \rightarrow -15\text{ V} \rightarrow 0\text{ V} \rightarrow +15\text{ V} \rightarrow 0\text{ V}$, as shown in Fig. 2(b). As a result, compared with the MIM sample, in the negative bias region, for the MIS sample, the current at the LRS is lowered from $\sim 30\text{ mA}$ (or $3.82\text{ MA/m}^2$) at $0.2\text{ V}$ to $13\mu\text{A}$ (or $1.65\text{ kA/m}^2$) at $1\text{ V}$, and the current at the HRS is decreased from $\sim 8\text{ mA}$ (or $1.01\text{ MA/m}^2$) to $\sim 30\text{ pA}$ (or $3.82\text{ mA/m}^2$) at $1\text{ V}$. Therefore, compared to the current ratio (CR) between the HRS and the LRS of two samples, an increased CR of $< 10^6$ was observed in the MIS structure, as shown in Figs. 1(a) and (b). This might be due to the current suppression effect caused by using a $p$-Si bottom electrode. In addition, the current is limited over the entire positive bias region and we have achieved a non-linear $I - V$ curve, leading to an asymmetric $I - V$ curve. Especially, during the voltage sweep in the positive bias to RESET the device, no RS behavior can happen, which shows that the proposed MIS structure exhibits an intrinsic rectifying property. It can suppress the positive bias current, like a diode, even when conduction paths are formed in the LRS. In addition, we observed similar current levels at the LRS but greatly different current value at the HRS, which might be explained by the MIM samples having relatively more conducting filaments (CFs) in the active layer than the MIS samples, which were generated via the SET process. As a result, even after the RESET process, in the MIM samples some CFs may still exist in the active layer, and a higher carrier transfer through their CFs may be induced at the HRS compared to the MIS samples.

Then, so as to study the conducting mechanism for the MIS Si$_3$N$_4$-based memory cell, we tried to replott the dc $I - V$ curves by using other models, such as the space-charge-limited current (SCLC), Ohmic behavior, and Poole-Frenkel current ($I_{P-F}$) equation [8–10]. From the result, the curves at the HRS and the LRS were found to match SCLC behavior well, as shown in Fig. 3. In this figure, we used a log-log scale in order to reveal the power law relation ($I \propto V^n$). In the negative voltage region, the slopes of the HRS and the LRS are about 1 in the low voltage region, which corresponds to the Ohm’s law ($I \propto \sim V^1$). However, the currents for both the HRS and the LRS follow a square dependence on the voltage, corresponding to the Child’s square law ($I \propto \sim V^2$). Finally, the current of the HRS increases very quickly at the trap-filled limit voltage ($V_{TFL}$), corresponding to a steep increase with increasing voltage. The carrier
transport behavior is consistent with the modified SCLC mechanism incorporating the Poole-Frenkel effect [8–10]. Consequently, the result shows that the basic switching mechanism of the Si$_3$N$_4$-based RRAM is closely related to the electron trapping and de-trapping processes in nitride-related electron traps or dangling bonds. For example, current paths can be formed within the Si$_3$N$_4$ films through the trap-to-trap hopping process of electrons (SET process) if the majority of the electron traps are occupied. In contrast, if the majority of the electron traps are empty, the current paths are broken via the electron de-trapping process (RESET process).

Finally, in order to suppress the read interference caused by parasitic sneak current paths in the CBA structures, we employed MIS-based RRAM devices consisting of Al/Si$_3$N$_4$/p-Si structures. In the $I – V$ curve characteristics, we observed a nonlinear selection behavior (at low voltages for both biases) and a Schottky diode property with current rectifying in the positive bias region, as shown in Fig. 2(b). Therefore, the intrinsic current limit behavior in the positive bias region can suppress disturbance between adjacent elements during the reading process. To further discuss the selector property of the proposed RRAM devices, we evaluated the read margin voltage ($\Delta V$) normalized to the pull-up voltage ($V_{pu}$) by using Kirchhoff’s equation, and the results are shown in Fig. 4. As a result, the MIM Si$_3$N$_4$ RRAM is subject to interference phenomena caused by sneaky leakage paths over a 2 × 2 CBA while the proposed MIS structure covers 17 × 17 arrays during the read operation because of its current limit property at low voltages.

III. CONCLUSION

In summary, to integrate bipolar resistive switching (BRS) cells into array structures, we proposed Al/Si$_3$N$_4$/p-Si MIS structures for applications to array RRAM and demonstrated the feasibility of achieving a self-rectifying resistive switching behavior in this cell. As a result, we observed an asymmetric $I – V$ curve in the positive and the negative bias regions as well as a non-linear property in $I – V$ curve when MIS structures were used, the read margins abruptly increased from 4 to 300 compared to the MIM structures. Therefore, this device can potentially simplify the fabrication process in high-density array applications.

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