Silicon-doped indium oxide – a promising amorphous oxide semiconductor material for thin-film transistor fabricated by spin coating method

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Abstract. Silicon-doped indium oxide (In-Si-O or ISO) has been investigated as the channel material of thin-film transistor (TFT) for the application of next generation flat panel displays. Because solution processing is simple, low cost and low power consumption in comparison with physical vapor deposition, it is a potential candidate for TFTs fabrication. We have been exploring research on TFT using ISO system via spin coating method. In this work, the performance of 3 at.% Si-doped indium oxide TFT has been improved with the highest mobility of 3.8 cm²/Vs without the passivation layer.

1. Introduction
For the application of flat panel displays, single crystal silicon has been often used as the channel material of thin-film transistor (TFT) because of high performance although it is expensive and lack of flexibility. Poly crystal silicon is less expensive; however, the existence of grain boundaries reduce the carrier mobilities. Amorphous silicon is the low cost and flexible, but the performance was the worst because the covalent bond sp³ σ states dramatically reduced carrier mobilities in amorphous phase [1]. Therefore, conventional amorphous silicon was unable to apply for thin-film transistor in application of high precision flat panel display.

Recently, amorphous In-Ga-Zn-O system was reported by Prof. Hosono group with great mobility and high transparency [2-5]. Thanks to that, amorphous doped indium oxide materials have been investigated as the channel material of thin-film transistor in application of flat panel display. Among many doped elements for indium oxide system, Si is one of the high rated element because the energy bonding of Si-O is stronger than that of In-O: the Si-O bond dissociation energy is 799 kJ mol⁻¹ while
that of In-O is 346 kJ mol\(^{-1}\) [6]. Hence, in silicon-doped indium oxide (In-Si-O or ISO) system, a small amount of Si can significantly contribute to decrease oxygen deficiency phenomenon, stabilizing the structure of indium oxide [7-12].

ISO TFTs have been fabricated by physical vapour deposition and exhibited high mobility around 10 to 20 cm\(^2\)/Vs [9-11]. Compared to physical vapour deposition, spin coating process is a promising method for fabrication of TFT because of its simplicity, low cost and low power consumption [13-19]. Especially, it is easy to change the concentration of Si doping to characterize the Si doping effect and can be applied in large area. For those above reasons, recently we have first investigated ISO TFT via spin coating method [20-21]. In this work, the performance of ISO TFT has been improved to satisfy the operation.

2. Experimental method

The ISO solution was prepared by dissolving indium chloride powder into acetonitrile solvent with molarity of 0.05 M. A small amount of ethylene glycol was added as a minor solvent in order to achieve the uniform film with the volume ratio of ethylene glycol per acetonitrile was 1/50. It is because acetonitrile has a low boiling temperature, evaporating quickly during spin coating process; as a result, the film could not be deposited well. Hence, the existence of high boiling temperature solvent (ethylene glycol in this case) plays an important role in the formation of film [22]. The solution made by the mixture of low boiling temperature solvent (main solvent) and high boiling temperature (minor solvent) is popular in spin coating method. Tetraethyl orthosilicate was added into prepared solution with the molar ratio of 3% as for Si-doping purpose. After that, the solution was stirred by a magnetic stirrer to dissolve indium chloride powder well in the solvent of acetonitrile, ethylene glycol and tetraethyl orthosilicate.

A heavily doped p-type single crystal (100) wafer with 250 nm thickness of thermally oxidized SiO\(_2\) layer on the surface was purchased from Electronics and Materials Corporation Limited, and used in this work as a substrate. The substrate was sonicated in acetone of 10 minutes, and dipped in sodium hydroxide 1 M of 5 minutes to modify the surface property of substrate from hydrophobic to hydrophilic via the attachment of the functional group -OH. Because the prepared ISO solution was a polar solution, so to obtain the wetting contact between substrate and solution, hydrophilic surface of substrate is essential. Then the solution was dropped on the prepared substrate and spin coated with the speed of 3000 rpm in 30 seconds. After that, the sample was dried at 100 °C by a hot plate in 5 minutes. The spin coating and drying process were repeated 4 times to achieve the desired thickness around 10 nm (according to x-ray reflectivity measurement). Finally, the samples were annealed at different temperature from 300 to 600 °C (step of 100 °C) in atmosphere in 1 hour.

To fabricate the thin-film transistor, 200-nm-Al-source electrode and drain electrode were deposited by thermal evaporation through a stencil mask. The mask was designed with various channel length from 50 to 350 µm (with a 50-µm step). The structure of ISO TFT and the fabricated ISO TFT are illustrated in Figure 1(a) and (b). The transfer characteristic (the drain current \(I_D\) versus the gate-source voltage \(V_{GS}\)) and output characteristic (the drain current \(I_D\) versus the drain-source voltage \(V_{DS}\)) of ISO TFT were indicated by a Keysight B2912A system. Because the applied \(V_{GS}\) was up to 80 V, so the mobility was estimated in the saturation regime as following equation:

\[
\mu = \frac{2L}{WC_i} \left( \frac{\partial \sqrt{I_D}}{\partial V_{GS}} \right)^2
\]

where \(L\) and \(W\) are the channel length and width, \(C_i\) is the capacitance per unit area of the gate insulator, and \(V_{GS}\) is the gate-source voltage [23-24].
Figure 1. (a) The cross-section structure of the ISO TFT. (b) The fabricated ISO TFT with 7 different channel lengths between 50 and 350 µm (a 50-µm step) based on the view from left to right side.

3. Results and discussion

Figure 2. The plot of $I_D^{1/2}$ versus the gate-source voltage $V_G$ of the best performance ISO (3 at.% Si) TFT annealed at 400 °C in air with $L = 50$ µm and $W = 1000$ µm. The circle mark is the raw data from experiment while the solid line is the linear fitting line. The figure includes the microscope image of the ISO TFT.

In our recent studies, x-ray diffraction, x-ray reflectivity and thermal desorption spectroscopy measurements revealed that ISO thin films fabricated by this procedure were amorphous form without organic residues, and their thickness, density, RMS roughness were about 10 nm, about 6 g/cm$^3$ and less than 1 nm, respectively [12,20,21]. Besides, the ISO TFTs were examined under numerous conditions such as ageing effect, Si-doping effect, the dependent on annealing temperature and the dependent on the film thickness for optimization [21]. It is suggested that the optimal fabrication involved the annealing temperature of 400 °C in atmosphere in 1 hour. In this work, in order to eliminate extrinsic effect reducing the device performance, by repeating the fabrication process many times in clean room and shorten the gap time between NaOH treatment and spin coating step, at the moment, the highest mobility we have achieved is approximately 3.8 cm$^2$/Vs without the passivation layer as shown in Figure 2. Here, the applied gate-source voltage increased from -40 to 80 V while the
drain-source voltage was 40 V: the measurements were conducted at the saturation region. From the square root of $I_D$, the slope of the fitting line was used to estimate the saturated mobility based on equation (1) and the intercept of the fitting line with x-axis was defined as the value of the threshold voltage. The result showed that the threshold voltage was around 0 V although there was an enhancement of $I_D$ in the experimental data around $V_{GS} = 0$ V. It is due to the traps at the interface of substrate and ISO films. To solve this problem, the substrate should be cleaned well by additional processes to remove contaminants completely.

As the report by Han et al, the presence of ozone in annealing process not only contributed to high performance of TFT but also reduced the annealing temperature [22]. As the next work for further reduction of oxygen vacancy, we also consider to anneal the ISO thin films in ozone or mixture of ozone/oxygen environment to increase the performance of solution-processed ISO TFT.

4. Conclusions
By improving fabrication process of our recent work in which the 3 at.% Si-doped indium oxide thin films were manufactured by the spin coating technique, investigated on various fabrication condition, and the best mobility was exceed 1 cm$^2$/Vs, we achieved the highest mobility up to 3.8 cm$^2$/Vs. Further work will be continued to increase the performance of solution-processed ISO TFTs for high precision displays.

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