Puppeteer: A Random Forest-based Manager for Hardware Prefetchers across the Memory Hierarchy

Furkan Eris1, Marcia S Louis1, Kubra Cilingir1, José L. Abellán2, Ajay Joshi1
1ECE Department, Boston University; 2CS Department, UCAM;
{fe, marcia93, kubra joshi}@bu.edu, jlabellan@ucam.edu

Abstract—Over the years, processor throughput has steadily increased. However, the memory throughput has not increased at the same rate, which has led to the memory wall problem in turn increasing the gap between effective and theoretical peak processor performance. To cope with this, there has been an abundance of work in the area of data/instruction prefetcher designs. Broadly, prefetchers predict future data/instruction address accesses and proactively fetch data/instructions in the memory hierarchy with the goal of lowering data/instruction access latency. To this end, one or more prefetchers are deployed at each level of the memory hierarchy, but typically, each prefetcher gets designed in isolation without comprehensively accounting for other prefetchers in the system. As a result, individual prefetchers do not always complement each other, and that leads to lower average performance gains and/or many negative outliers. In this work, we propose Puppeteer, which is a hardware prefetcher manager that uses a suite of random forest regressors to determine at runtime which prefetcher should be ON at each level in the memory hierarchy, such that the prefetchers complement each other and we reduce the data/instruction access latency. Compared to a design with no prefetchers, using Puppeteer we improve IPC by 46.0% in 1 Core (1C), 25.8% in 4 Core (4C), and 11.9% in 8 Core (8C) processors on average across traces generated from SPEC2017, SPEC2006, and Cloud suites with ∼10KB overhead. Moreover, we also reduce the number of negative outliers by over 89%, and the performance loss of the worst-case negative outlier from 25% to only 5% compared to the state-of-the-art.

I. INTRODUCTION

Instruction and data prefetching [16] are commonly used in today’s processors to overcome the memory wall problem [61]. The key idea behind prefetching is identifying the current memory access pattern and predicting addresses to proactively fetch instructions and data into the cache to avoid cache misses. Prefetching hides the large memory access latency, and in turn, improves processor performance. As a result, modern processors employ multiple prefetchers to cover a wide range of applications. Consequently, existing prefetchers do not improve the performance of all applications; in some cases they hurt application performance by prefetching the wrong memory addresses [31]. These incorrect prefetches use up the precious memory bandwidth and the limited space in the cache hierarchy. This increases data and instruction access latency, which hurts application performance.

To evaluate a prefetcher’s performance, we can use scope and accuracy as the metrics [5, 29]. A prefetcher with high prefetching accuracy usually has limited scope, i.e., it is very good at identifying a limited number of memory access patterns and can accurately prefetch data/instructions if those specific memory access patterns exist. However, such a prefetcher fails to identify other memory access patterns. Conversely, a prefetcher with broad scope caters to a wide variety of memory access patterns, but it has low accuracy. Effectively, we need to find a balance between the accuracy and scope of the prefetcher. One way to balance scope and accuracy is to use multiple high accuracy prefetchers at each level of the memory hierarchy, as is the case in AMD and Intel processors [1, 2, 6, 19]. Each prefetcher is customized to identify a specific type of memory access pattern and make a prefetching prediction. However, having multiple prefetchers operating at each level in the memory hierarchy can lead to the following issues:

- Given that each prefetcher is trained independently to track a specific type of traffic and simultaneously share microarchitectural resources, prefetchers can sabotage each other during runtime. A prefetcher may trigger prefetch requests that evict cache lines that another prefetcher has accurately prefetched. This behavior leads to a loss in performance, wasted memory access bandwidth, and increased power consumption.
- Different prefetchers (either at the same level or across levels in the memory hierarchy) latch onto memory access patterns at different speeds. So a prefetcher’s prediction can be influenced by the traffic generated by other prefetchers. These differences in temporal behavior can cause faulty synchronization among prefetchers and lead to a drop in application performance.

Essentially, prefetchers compete for resources, and at times, sabotage each other. To validate our argument, we use trace[1] generated from SPEC2017, SPEC2006, and Cloud benchmark suites and run these traces on an OoO processor that uses a different prefetcher at each level of the memory hierarchy (details of the particular evaluation methodology in Section IV). We execute these traces using two state-of-the-art prefetcher solutions – IPCP [39] and EIP [48], who were the winners of prior prefetching competitions [43–45]. These prefetcher solutions use different prefetchers at each level of the memory hierarchy, i.e., different prefetcher system configurations (PSC). Both prefetcher solutions improve

1 A trace is a group of instructions that represent a specific behavior. One or more traces can be used to represent the behavior of a benchmark. For example, a benchmark with consistent looping behavior can be represented by one trace corresponding to a single iteration of the loop. One or more unique representative traces are generated from each benchmark [42].

2 A PSC specifies which prefetcher is switched ON at each level of the memory hierarchy. We denote a PSC using the following format

<preference-in-L1I$><preference-in-L1D$><preference-in-L2I$><preference-in-L2D$>
Fig. 1: Motivational Example - Performance of a processor when using IPCP and EIP prefetchers. Here we show the 20 traces with the highest difference in performance out of 232 traces that we evaluated. The performance compared to the no prefetching case. However, IPCP (no-icp-ipcp-nl) (further details on the types of prefetchers are given in Table V) shows better performance over EIP in 100 out of 232 traces with the largest performance gain of 56% in 602.gcc_s-2226B. EIP (EIP-nl-spp-no) shows better performance over IPCP in the remaining 132 traces and has the largest performance gain of 89% in server_036.

In Figure 1, we show a subset of traces that have a significant difference in their IPC when using IPCP and EIP prefetcher solutions. The standard methodology would have us select EIP because it has on average 7.8% performance gain over IPCP, but that would come at the cost of having a performance loss for 100 out of the 232 traces.

One way to address this problem is to have multiple different prefetchers at each cache level and switch ON a prefetcher based on the current program phase. For example, one prior work that has attempted to leverage multiple prefetchers in the same level of the memory hierarchy is by Kondugli et al. [29]. The authors propose a ‘composite prefetcher’, which uses a priority queue as the control algorithm to select a prefetcher at a single level in the memory hierarchy. While this approach provides benefits, the ‘composite prefetcher’ priority queue is designed offline for a given set of applications. For previously unseen applications, we will not necessarily see any performance improvement. Furthermore, the control algorithm will not scale well as we increase the number of prefetchers in the system and target different levels in the memory hierarchy.

What is really needed is a manager that can successfully manage multiple prefetchers at each level in the memory hierarchy and has a low overhead. This manager will choose the PSC that is suitable for the current phase of an application. The chosen PSC should have prefetchers that complement each other for the current phase, reduce memory access overhead, and in turn improve application performance. Given that multiple prefetchers are available at each level in the memory hierarchy, this ‘manager’ will effectively determine which prefetcher should be ON/OFF at each level in the memory hierarchy, both across different phases of an application and across applications. In this paper we propose a machine learning (ML)-based hardware manager called Puppeteer that selects the PSC at runtime. Contrary to the prior work [32], [46], [62] that focuses on training the ML model to improve the prefetch address prediction accuracy of the ML model, we train the ML model of Puppeteer to increase the overall system performance (quantified as IPC). Using our unique training strategy, we are able to specifically target training for application phases where the swing in IPC is much higher than in other regions. Thereby, we tailor Puppeteer for these phases and achieve high targeted-application-phase accuracy instead of just high overall model prediction accuracy.

To manage the prefetchers across multiple cache levels at runtime, we propose a multi-regression ML-based approach. We use the observed IPC of the various PSCs for different phases of each application to train our ML model. We train a unique random forest regressor per PSC (in our case, we have 5 different PSCs, which we pruned down from the 300 possible PSCs – more details about this in Section [V], to create a suite of random forests regressors. For features used in the ML model, we use events that can be tracked using hardware performance counters and whose behavior does not change with the choice of PSC, i.e., PSC-invariant events. An example of such an event is the number of branch instructions in an application. The branch instruction count does not change with the choice of PSC. Using only PSC-invariant events, we can limit the number of executions per trace we must account for during training, making it easier to train the ML model in Puppeteer (more details about the training approach are in in Section [V]). In summary, the contributions of our work are as follows:

- We propose a novel ML-based runtime hardware manager called Puppeteer to manage the various prefetchers across the memory hierarchy to improve processor performance.
- We design Puppeteer to use a set of PSC-invariant events (which can be tracked using hardware performance counters) as inputs and predict the PSC for the next instruction window. We co-optimize the hardware design and the ML model of Puppeteer with the goal of maximizing the overall application performance while minimizing the area overhead. At runtime, at the end of an instruction window, Puppeteer predicts the IPC for each PSC and selects the PSC with the highest predicted IPC for the succeeding instruction window.
- We train Puppeteer to maximize processor performance instead of the prefetch address prediction accuracy. We use only 10% of the data for training to prevent overfitting and design Puppeteer with a low hardware overhead (∼10KB). For the 232 traces we experiment with, Puppeteer achieves an average performance gain of 46.0% in 1 Core (1C), 25.8% in 4 Core (4C), and 11.9% in 8 Core (8C) processors on average compared to a system with no prefetching. Moreover, we ensure Puppeteer reduces negative outliers. When using Puppeteer, we observe an 89% reduction in the number of outliers, down to 8 outliers from 53, and a 20% reduction in the IPC loss of the worst-case outlier compared to the state-of-the-art prior prefetcher managers.

An instruction window is group of instructions that are executed sequentially at runtime. We experimented with different instruction window sizes and did not see a large change in the performance of Puppeteer. We set the size to 100,000 instructions.
• Finally, to the best of our knowledge, Puppeteer is the only manager that targets all cache levels in the memory hierarchy.

II. BACKGROUND AND RELATED WORK

A. Heuristic-based Prefetcher Managers

When a processor executes an application, there is a diverse set of interactions among the compute, memory and communication components of a computing system. These interactions are dependent on the processor (micro)architecture and the application, thus effectively making the processor a big finite state machine with an extremely large state space. This makes it difficult to use deterministic techniques, which consider all possible states, for hardware management. As a result, over the past 20-30 years, heuristics algorithms have been used for hardware management, including for prefetcher management such as static priority queue-based approaches [29], [47] and rule-based prefetcher throttling approaches [12]–[15], [21], [23], [33], [55]. These algorithms have low memory/area overhead and improve processor performance for the average case. However, with the ever-increasing complexity of processors and the diversity of applications, heuristic algorithms are no longer effective. Heuristic algorithms are extremely dependent on the hardware/operating conditions, and cannot easily adapt to variations at runtime.

B. ML-based Prefetcher Managers

ML methods have been gaining traction in place of heuristic methods for achieving superior prefetcher management performance [5], [22], [24], [32], [34]. ML algorithms can extract the non-intuitive interactions between the different prefetchers. Prior methods on prefetcher management configure or train the manager, which typically predicts which PSC to use for a given application, using values of hardware events collected for a single fixed PSC (generally, the default PSC [5], [24], [32], [46]). Using an ML model trained using only a single fixed PSC would make sense if the prefetcher system always uses that single fixed PSC at runtime. However, at runtime the PSC changes. If the values of the hardware events are highly dependent on which PSC is being used, using a dataset generated using a fixed PSC for training leads to a low-accuracy ML model for the prefetcher adaptation. To address this concern, we train our ML model using PSC-variant hardware events (i.e., events that are not dependent on the PSC, e.g., the number of branch instructions).

We observe a wide variation in the complexity of the ML algorithms used in prior work. We list the prior work in Table I. Some of the algorithms are simple and either use small datasets or use datasets that do not accurately portray the runtime environment as they use PSC-variant events and only train data of one fixed PSC. As a result, these algorithms cannot achieve good accuracy at runtime [24], [32], [46]. Other algorithms, such as neural networks, are too complex and their size increases prohibitively with the size of the dataset [5]. Moreover, some prior works focus on hardware adaptation only from the perspective of accuracy without worrying about the hardware implementation [22], [24], [32], [46].

Contrary to the prior work, we jointly account for accuracy of the ML model and hardware overhead when designing Puppeteer. Puppeteer is complex enough to provide good accuracy on a wide variety of applications. At the same time, Puppeteer is not too complex (as demonstrated in Section III-D) to be implemented in hardware and scales well with the size/complexity of the dataset. Furthermore, Puppeteer is agnostic of the underlying internal mechanics of the prefetchers and can be easily retrained for a new prefetcher that is introduced in a new system. Additionally, to the best of our knowledge, Puppeteer is the only manager that targets all cache levels in the memory hierarchy.

C. Overview of Existing Prefetchers

The focus of our work is on a prefetcher manager and our manager can work with any type of prefetcher. Broadly, we can split prefetching techniques into several categories. We can have regular-pattern-based, i.e., stride-based prefetchers [25], [59], irregular-pattern-based, i.e., stream-based prefetchers [8], [54], prefetchers that track both regular and irregular patterns [27], [51], and region-based prefetchers [18], [58]. A very good comprehensive survey on prefetchers can be found in Falsafi et al. [16].

ML-based algorithms can be used for predicting the addresses of the instructions/data that should be prefetched at each cache level in the memory hierarchy. The ML-based solutions include table-based reinforcement learning [4], [40], linear model-based reinforcement learning [63], perceptron-based neural networks [17], [41], Markov chain model [35], and LSTM-based neural networks [7], [20], [37], [47], [52], [53], [56], [62], [64] to predict memory access patterns. As ML algorithms get more powerful, and the techniques to compress these algorithms become more sophisticated, ML-based prefetchers will become common place in processors.

TABLE I: Overview of the Related Work on Prefetcher Managers - We use NA when the paper lacks information about the respective metric. In the last column, ‘software’ indicates the software prefetcher. For IPC, we report average IPC gain in 1C.

| Work | # PF | # Cache Levels Managed | IPC Gain Over Baseline PSC | IPC Gain Over No Prefetching | Heuristic or ML | Overhead |
|------|------|------------------------|-----------------------------|-------------------------------|----------------|----------|
| [27] | 1    | 1                      | Only reports accuracy       | Heuristic                     | Software       | NA       |
| [29] | 1    | 1                      | 5%                          | 41%                           | Heuristic      | 4.6KB    |
| [24] | 1    | 1                      | 7.8% (6% from 1 application)| NA                            | Heuristic      | Software  |
| [26] | 0    | 1                      | 11%                         | NA                            | Heuristic      | Software  |
| [42] | 4    | 2                      | Only reports ML accuracy    | Heuristic                     |Software        |         |
| [56] | 4    | 2                      | Only reports ML accuracy    | ML                            | Software       |         |
| [5]  | 1    | 1                      | TPF targets 2 levels       | 2.27%                         | ML             | ~39KB    |
| [22] | 4    | 1                      | -1% to 5.6%                 | -1% to 8.5%                   | ML              | Software  |
| [24] | 1    | 1                      | -5% to 1%                   | 23%                           | ML              |         |
| Puppeteer | 7 | All (4)               | 14.7%                       | 46%                           | ML              | 10KB     |
III. PUPPETEER DESIGN

A. Puppeteer System-Level Overview

In Figure 2 we show the system-level design of an example prefetcher system that uses Puppeteer. The prefetcher system consists of eight different prefetchers (Pf1 to Pf8), which is typical in modern high performance processors such as Intel i9 [2] and AMD Ryzen7 [1]. These eight prefetchers track different memory access patterns and prefetch data from main memory to last-level cache (LLC), from LLC to L2$, and from L2$ to L1$. Pf1 and Pf2 target instruction lines to bring into L1IS, Pf3 and Pf4 prefetch data into L1DS, Pf5 and Pf6 prefetch data into L2$, while Pf7 and Pf8 target data to bring into LLC. These prefetchers compete among them for cache and memory resources. Even across memory levels, a wrong prefetch request from lower levels of memory can harm the performance of prefetchers at higher levels of memory. These prefetchers can sometimes act overly aggressive, and can adversely affect each other, in turn leading to loss of application performance. There are many heuristics-based algorithms that use simple inputs such as accuracy of the prefetchers or memory bandwidth utilization to throttle prefetchers in such adverse scenarios [12], [13], [21], [23]. These heuristic algorithms are designed to have low overhead, and hence are highly optimized for the prefetchers in a given prefetcher system.

Puppeteer works as a manager of all prefetchers and complements the heuristic algorithms used in the given prefetcher system. At runtime, Puppeteer periodically updates the PSC, i.e., it sets which prefetcher should be ON and which should be OFF at each level in the memory hierarchy. To update the PSC, Puppeteer uses an ML model with the PSC-invariant hardware events, collected from hardware performance counters (HPCs) as inputs. While low-overhead heuristic algorithms are still required to make extremely low latency decisions at the cycle level, Puppeteer provides additional adaptability by leveraging the power of ML and thereby increasing the performance. Effectively, heuristic algorithms such as throttling are used in the system to constantly regulate the short-term behavior of the prefetchers, while Puppeteer controls the longer-term system-level behavior (across hundreds of thousands of cycles).

B. Puppeteer Algorithm

For the ML-based Puppeteer algorithm we considered a classification-based approach and a regression-based approach. The classification-based approach has been used by prior works because it is relatively easy to train offline and has lower hardware overhead compared to regression. The regression-based approach has potential for higher performance and has better tolerance to variability compared to classification during runtime when trained offline.

Classification vs. Regression: To train Puppeteer, as a classification problem we created a dataset using thresholding method similar to prior works [3], [24], [32], [34]. Here, a trace is run using all available PSCs. A PSC is given a label of “1” if the IPC when using that PSC is within some threshold (in the case of the prior work the threshold is 0.5%) of the IPC when using the ideal PSC. Multiple PSCs can pass the chosen threshold for a given program phase and we then end up using the PSC that is predicted as “1” with the highest probability. Otherwise, the PSC receives a label of “0”. Using such a classification approach leads to sub-optimal results. As an example, consider we have four different traces.

As an example, consider we have four different traces. Let us say we classify the first three out of the four traces correctly and the fourth one incorrectly – i.e. we are able to identify the correct PSC for the first three traces, but not the fourth trace. So, our classification accuracy is 75%. This means that the first three traces will have performance that is within 0.5% of their ‘ideal’ performance. However, the performance of the fourth trace could be 100% worse or just 0.51% worse than the ‘ideal’ performance. This variation in the performance is not accounted in the classification-based model. Furthermore, this problem is not unique to the given example. Any classification-based method would have a similar issue because all labeling methods used to create the dataset for the classification algorithm will certainly lose some amount of information.

In contrast, a regression-based approach accounts for the value of IPC gain/loss and not just if there is IPC gain/loss, when deciding the PSC. Given that the regression algorithm is trained on the IPC values directly, the quantitative information of IPC gain/loss is not lost, and the regression algorithm can learn the magnitude of a good or bad prediction. In particular, the regression algorithm will be used to predict an IPC value for each PSC for a given instruction window. Then, we choose the PSC with the highest predicted IPC value.

---

4Here accuracy of a prefetcher is quantified as the fraction of the total prefetches that were actually useful, and is calculated as #prefetches referenced by the program divided by total #prefetches. Note, this prefetcher accuracy is not the same as the ML model accuracy. Scope is calculated as total #misses eliminated by the prefetcher divided by the total #misses when prefetching is disabled.
**Suite of Regressors vs Single Regressor:** When using regression algorithms, we have two options: (i) use a single regressor, where all data collected from all the PSCs are used to train that single regressor; or (ii) use a suite of regressors, where each PSC will have a dedicated regressor. Using a suite of regressors leads to a more customized solution that has higher accuracy as compared to using a single regressor. Conceptually, this is because in a single regressor, we maximize the accuracy across all PSCs instead of maximizing the accuracy of each PSC separately, whereas, in a suite of regressors we train a dedicated regressor for each PSC. In this way, we indirectly jointly increase the scope and accuracy of the overall prefetching system.

In our work, we use a suite of regressors where we implement each regressor using random forest, i.e. one random forest trained per PSC, due to its simple implementation, its robustness to noise in the dataset, its lower overhead (compared to other ML algorithms such as neural networks), and its higher accuracy (compared to other ML algorithms such as decision trees) [30], [38].

We have multiple trees per forest and we allow each tree to split at locations that are unique to the PSC associated with the forest. The leaves of each tree in the forest specify the predicted IPC value for the PSC. For each forest i.e. each PSC, we calculate the average of the predicted IPC values obtained from all the trees in the forest, and then choose the PSC with the highest average predicted IPC. Given that each forest has multiple decision trees, our method has higher tolerance to wrong decisions by the trees, where even if some of the trees give wrong decisions, other trees can compensate.

In Figure 3 we conceptually show the differences between the four different options discussed above: (a) single classifier, (b) single regressor (c) a suite of classifiers, and (d) a suite of regressors. Respectively, the leaf nodes in (a) contain the PSC choice directly, (b) have the predicted highest IPC among all the PSCs, (c) the probability value of a given instruction window belonging to the given PSC (of which we choose the highest one), and (d) the predicted IPC value for a given PSC which will be averaged per tree in a given RF and compared with the other averaged predicted PSC values from the other RFs (of which we will choose the highest). For (a) and (b) the PSCs are traversed simultaneously, since the PSCs share a single algorithm, while for (c) and (d) each PSC has a unique algorithm we traverse.

**C. Puppeteer Training**

To train Puppeteer we need to generate a representative dataset. Consider the case where we have a single prefetcher, Pf, at only one level in the memory hierarchy. Here the number of PSCs ($N_{psc}$) = 2, i.e., Pf=OFF and Pf=ON. For two consecutive instruction windows, we will have $N_{psc}^2 = 4$ possible scenarios: (i) Pf=OFF → Pf=OFF, (ii) Pf=ON → Pf=OFF, (iii) Pf=OFF → Pf=ON, and (iv) Pf=ON → Pf=ON. With $N$ number of instruction windows and $N_{trace}$ number of traces, the number of different possible scenarios will then be $N_{trace} \times N_{psc}^N$. When $N$ increases, the number of different scenarios will increase exponentially, hence including each unique scenario in the dataset for training is not feasible. To handle this problem, we propose to use only PSC-invariant events as our features. An example of a PSC-invariant event is the number of conditional branches, which is not affected by the choice of PSC. We check the variance of each hardware event value (for 180 total hardware events that we can track) for each PSC. We identify 59 events whose values vary by less than ±10% from their mean value across all PSCs. We further reduce the number of events by eliminating the redundant events that track similar behavior and have high correlation with each other. Table 1 shows the final 6 events we choose to track trace behavior. After we have identified our PSC-invariant events that will be the features and the PSCs that will be the choices of our ML model, we collect an IPC value per PSC for each instruction window as our ground truth.

Using the features and IPC values we have collected, we then form our suite of random forest regressors wherein we train a separate forest for each PSC using CART (classification and regression trees) [57]. CART is a greedy recursive search algorithm that maximizes information by splitting the data at each node using one feature. Each child node is split recursively until there is no information gain from splitting a child node. We limit the total number of decision nodes in Puppeteer to keep the size of Puppeteer smaller than L1S. With this limitation in mind, we conduct a hyper-parameter search and determine that the number of estimators (trees per random forest) should be 5 and the number of max nodes should be 100 per tree.

**D. Puppeteer Microarchitecture Design**

Figure 4 shows the microarchitecture details of Puppeteer. We use a single port SRAM array called Node MEM to store information about the nodes that form the trees of each random forest in Puppeteer. We load the random forest-based Puppeteer model into the Node MEM at startup using
HPC 0

HPC 1

HPC 5

Controller

Node MEM

Load Unit

Root Index Table

Best PSC Unit

Comparator

PSC 1 Forest

PSC 2 Forest

PSC 3 Forest

Fig. 4: Puppeteer Hardware Design - Puppeteer is made up of a Node MEM - SRAM array, a max logic unit, and several register files. firmware. Each entry of Node MEM corresponds to one node in one of the random forests and it consists of the following fields: (i) A 3-bit HPC ID field that specifies which PSC-invariant event, i.e., which hardware performance counter (HPC), is used by that node to make a decision. The 3-bit encoding enables the node to use one of 6 different PSC-invariant events (see Table II). (ii) A 16-bit Threshold field (threshold value is determined during training), which is employed by the node to decide if the decision path should branch left or right. In our problem 16 bits provide enough precision for the ML model weight values. (iii) A 12-bit Left Node Value (LNV) field, and (iv) a 12-bit Right Node Value (RNV) field. These LNV and RNV fields represent child node indices for internal nodes of a tree. For the leaf nodes of a tree, we use these LNV and RNV fields to indicate the predicted IPC value of a PSC. We differentiate between child node index and predicted IPC using (v) a 1-bit Type field. We use a separate 1-bit Type field for LNV and RNV.

At the end of every instruction window, Puppeteer calculates the predicted IPC for each PSC in the next instruction window by traversing the trees of the associated forest and using the PSC-invariant event values for the current window as inputs. For each forest, the controller in Puppeteer reads the Node MEM index of the root node for the first tree from Root Index Table (RIT) and loads the Node MEM entry for the root node using a Load Unit into a register. Next, the HPC ID in the loaded Node MEM entry is used to load the corresponding PSC-invariant event value into a second register. Then the Threshold value, stored in the first register, and PSC-invariant event value stored in the second register are compared using the Comparator. Based on the Comparator output, we choose to traverse down to the left child or the right child. The Controller then uses the corresponding index value from LNV or RNV to find the next node in Node MEM. The Controller continues traversing the tree until it loads a predicted IPC value corresponding to a leaf from the Node MEM. The above steps are repeated for the remaining trees in the forest, and then we calculate the average of the predicted IPC values obtained from all the trees in that forest. The Best PSC Unit in the Controller stores the ID of the PSC with the highest predicted IPC value. Every time the Controller finishes traversing a forest, the predicted IPC value of that forest, i.e., PSC, is compared with the predicted IPC value stored in the Best PSC Unit using the Comparator. If the new predicted IPC value is higher than the current value, the Best PSC Unit updates the predicted IPC value and the ID of the PSC. Once all forests have been traversed i.e., all PSCs have been evaluated, Puppeteer chooses the entry stored in the Best PSC Unit as the PSC for the next instruction window.

We determined that a maximum depth of 10 per tree is more than sufficient to accurately determine the best PSC. In our evaluation we use a prefetcher system with $N_{psc}=5$ (given in Table VI and discussed in detail in Section IV). We need a total of 2250 nodes to design the trees in Puppeteer, and these nodes require a 10.75 KB-sized Node MEM (compared to a typical L1S of 32 KB). Other than Node MEM, we require a $5 \times N_{psc}$-entry RIT where each entry is 13-bit wide (12 bits for the root node index and 1 valid bit), a 12-bit comparator containing comparison logic and two registers, a load unit, and a register to store the best PSC information in the Controller.

Discussion of the hardware overhead in more detail in Section IV.

IV. EVALUATION METHODOLOGY

We use ChampSim [44] for our analysis, where we model one core (1C), four core (4C), and eight core (8C) processors to have multiple prefetchers at each level of the cache – private L1S, L1D, private L2S and shared LLC (more details provided in Table II). We train Puppeteer using data collected from a 1C and 4C OoO processor and then evaluate it on 1C, 4C, and 8C OoO processors. In the 4C and 8C processors, we have a private Puppeteer per core. Each private Puppeteer utilizes the 6 PSC-invariant events per core and makes independent decisions. For our evaluation we use a diverse set of 232 traces generated from SPEC2017 [11], SPEC2006 [10], and Cloud [45] benchmarks.

In Table III we list the notations used for all the static PSCs and the runtime managers (that change PSC at runtime) that we have evaluated. In our evaluation, we normalize all IPC values to the same state-of-the-art baseline as PPF [3], i.e., SPP [27] (no-no-spp-no). We compare Puppeteer against the best static PSCs from competitions, i.e., IPCP (no-iccp-iccpp-nl) and EIP (EIP-nl-spp-no); as well as managers such as the final version of the algorithm developed by Jimenez et al. that uses trial periods to latch onto the PSC [24] (J3), Pythia that is an RL-based algorithm developed by Bera et al. [4] (PY)8, a multi-layer-perceptron similar to Bhatia et al. [5] (NN), and a binary-tree (BT) based algorithm [32] - where Liao et al. tried several different ML methods (such as decision trees and NN) and concluded that decision trees are the best choice.

A. Training Approaches for ML-based Prefetcher Managers

When evaluating any new idea, a widely used approach in the industry is to use all available evaluation data.

8Note that Bera et al. used SHIP [60] for their cache replacement policy and perceptron as their branch predictor. We tested with their settings as well as with using Pythia with hashed-perceptron and LRU, and observed on average that Pythia with hashed-perceptron with LRU has 12% higher IPC. Hence, we use hashed-perceptron and LRU similar to all the other comparison points in this paper.
TABLE II: Simulated System Parameters

| Component          | Simulated Parameters                                      |
|--------------------|-----------------------------------------------------------|
| Core               | One to four cores, 4GHz, 4-wide, 256-entry ROB            |
| TLBs               | 64 entries TLB, 64 entries DTLB, 1536 entry shared L2 TLB |
| L1 IS              | 32KB, 8-way, 3 cycles, PQ: 8, MSHR: 8, 4 ports            |
| L1 DS              | 48KB, 12-way, 5 cycles, PQ: 8, MSHR: 16, 2 ports          |
| L2 S               | 512KB, 8-way, 10 cycles, PQ: 16, MSHR: 32, 2 ports        |
| LLC                | 2MB/core, 16-way, 20 cycles, PQ: 32Xcores, MSHR: 64Xcores |
| DRAM               | 4GB 1 channel/1-core, 8GB 2 channels/multi-core, 1600 MT/sec |

| Hardware Event     | Properties                                      |
|--------------------|-------------------------------------------------|
| L1T/PAGES_READ_LOAD| L1S Pages Read on Load.                          |
| L1D/PAGES_READ_LOAD| L1D Pages Read on Load.                          |
| L1D/STORE_ACCESS   | L1DS Store Access.                               |
| BRANCH RETURN      | Branch Returns.                                  |
| NOT BRANCH         | Not Branches.                                    |
| BRANCHCONDITIONAL  | Conditional branches.                            |

TABLE III: Static PSCs and Managers Evaluated - We list the static PSCs from the prior prefetching competitors, the manager algorithms from prior work, and the different flavors of Puppeteer.

| Algorithm Notation | Explanation | Static PSC or Manager | Training Dataset |
|--------------------|-------------|-----------------------|------------------|
| NO                 | No prefetching is used. PSC = no-no-no-no       | Static PSC         | Not trained      |
| IPCP               | Winner of DPC3 [43], PSC = no-ipcp-ipcp-no        | Static PSC         | Not trained      |
| EIP                | Winner of IPC3 [45], PSC = EIP-1-ap-no         | Static PSC         | Not trained      |
| PY                 | RL-based algorithm named Pythia [1]            | ML-based Prefetcher | Online           |
| J3                 | Heuristic-based algorithm [23]                  | Manager            | Not trained      |
| NN                 | Multi-layer-perception [1], Manager              | Manager            | 1C               |
| BIC                | Decision tree algorithm by Liao et al [12]     | Manager            | 1C               |
| B4CS               | Decision tree algorithm by Liao et al [12]     | Manager            | 4CS              |
| B4CM               | Decision tree algorithm by Liao et al [12]     | Manager            | 4CM              |
| PIC                | Puppeteer [14]                                  | Manager            | 1C               |
| PSIC               | Puppeteer [14]                                  | Manager            | 4CS              |
| PICM               | Puppeteer [14]                                  | Manager            | 4CM              |

We are using a ML-based approach and are cognizant of the fact that we do not want to overfit our model using all available data for training the ML model. So here, we compare three different approaches for constructing the training dataset for Puppeteer. For training, we have 232 traces × 10,000 instruction windows per trace = 2,320,000 instructions windows. For each approach, we limit the training data in different ways. Note that we are still training at the instruction window-level and performing 10-fold cross-validation on the training set for all approaches. We give the percentage of data used to construct each training dataset in Table IV.

In the first approach, we severely limit the data and randomly select 10% of the instruction windows at random time intervals to form the training dataset, i.e., 90% of the instruction windows are not seen during training. The idea behind this approach is that we are training the algorithm to recognize low-level memory access behavior. This approach does not overfit the model because the behavior of the benchmarks when collecting the training data would be different from the behavior of the benchmarks when we use the trained Puppeteer. This difference is because when collecting training data we do not change the PSC, while when using Puppeteer the PSC can potentially change for each instruction window. In the second approach, we generate the dataset by leaving 20% of the traces out of the training dataset and using 60% of the instruction windows from the remaining 80% traces for training. We use a 60-40 split of the instruction windows to avoid overfitting the model to the 80% of traces in the training set. Given traces are constructed to represent unique behaviors in each application, our training set will not have information on all the unique behaviors of a given benchmark. This means that some of the traces from other benchmarks are assumed to be from the same distribution of these missing traces or else there will be no way for the algorithm to train for these regions. In the third approach, we generate the dataset by leaving 20% of the benchmarks out of the training dataset and using a 60-40 split of the instruction windows belonging to the remaining 80% benchmarks for training. In this approach, whole benchmarks are not considered during training. Here too, we choose a 60-40 split of the instruction windows to avoid overfitting the model to the 80% of benchmarks in the training set. Similar to the second approach it is assumed that some of the other benchmarks will be similar in behavior to the missing benchmarks and cover their memory access behavior.

In a 1C processor, when using Puppeteer on unseen benchmarks, for the first, second, and third approaches, we observe an average IPC gain of 11.3%, 9.8%, and 6.6%, respectively, over SPP. In the second and third approaches, we see that Puppeteer has lower performance gain than the first approach. Despite having 3% more instruction windows for training in the third approach compared to the second approach there is a 3.2% drop in performance. Furthermore, in the first approach we use only 10% of the total number of instruction windows for training (5 × less instruction windows than the other approaches), yet this approach performs 1.5% and 4.7% better than the other two approaches. This implies that the second and third datasets is trained on an insufficient number of unique memory accesses patterns, leading to low performance observed during runtime execution. Therefore for the rest of our evaluation we train all ML-based prefetcher managers using the first approach. As mentioned earlier, Puppeteer can always be retrained and updated via firmware.

B. 1C, 4C and 8C Workload Formulation

We run 1C and 4C experiments using a 200M instruction warmup phase and 1B instruction detailed simulation phase, while for 8C we use 200M instruction warmup phase and 250M instruction detailed simulation phase. We generate a total of 232 traces from SPEC2017, SPEC2006, and Cloud benchmarks. We create two flavors of trace sets for the 4C and 8C experiments: a single-type trace set where each core runs the same trace, and a mixed-type trace set where each core runs a unique trace. Therefore we have 5 data suites in total: 1C, 4C single-type trace set (4C STS), 4C mixed-type trace set (4C MTS), 8C single-type trace set (8C STS), and 8C mixed-type trace set (8C MTS). We use hashed-perceptron for branch predictor and least-recently used (LRU) policy for cache replacement policy provided by ChampSim. To construct our mixed-type trace sets, we first split the 232
TABLE IV: Dataset training approaches. Here % Benchmarks indicates the percentage of benchmarks were used during training, % Traces indicates the percentage of traces from the available benchmarks were used during training, and % Inst. Win. indicates the percentage of instructions windows from the available traces were used during training. The last columns indicates overall the percentage of instruction windows were using during training.

| Approach | % Benchmarks | % Traces | % Inst. Win. | Total % of all Inst. Win. used for training |
|----------|--------------|----------|--------------|------------------------------------------|
| # 1      | ALL          | ALL      | 10%          | 10%                                      |
| # 2      | ALL          | 80%      | 60%          | 48%                                      |
| # 3      | 80%          | ALL      | 60%          | 51%                                      |

TABLE V: Initial Prefetcher Options - We show the regular and irregular prefetcher options we used at each cache level to construct our set of 300 PSCs. We reduce the number of PSCs down to 5 PSCs before training.

| L1I$ | L1D$ | L2$ | L2$ | LLC |
|------|------|-----|-----|-----|
| No Prefetcher | No Prefetcher | No Prefetcher | No Prefetcher | No Prefetcher |
| Next-line [16] | Next-line | Next-line | Next-line | No Prefetcher |
| FNL-MMA [49] | IPCP [49] | IPCP [49] | IPCP [49] | IPCP [49] |
| DJOLT [48] | MLOP [48] | SPP [48] | KPCP [50] | Ig-Stine [16] |
| EIP [48] | Bingo [48] |

traces into 6 groups based on ascending execution latency. Then we randomly select a trace from a given group per core and construct a mixed-type trace group. We cover all permutations of the various latency groups. This way we have diversity in the traces running on the cores. For example, in a 4C processor, we can assign a trace from group 2 to core0, a trace from group 3 to core1, a trace from group 4 to core2, and a trace from group 5 to core3. This can be represented as 

\[ \text{2} \times \text{3} - \text{4} - \text{5} \]. Therefore we have 360 experiments (6 options for 

\[ \text{core0} \times 5 \text{ options for core1} \times 4 \text{ options for core2} \times 3 \text{ options for core3} \] in 4C MTS for 6 latency groups and 4 selected traces (1 for each core). For 8C MTS, since the number of experiments increases and the experiments take quite long, we replicate the same latency group for 4 of the cores. For example, we can use \[ 1 - \text{1} = \text{1} - 1 - 4 - 4 - 4 - 4 = 4 \text{ for an 8C experiment. However, instead of 6 groups as in the 4C system, we use 10 groups for the 8C system, to cover a more granular variety of behavior and instead of permutations we use combinations with replacement. Therefore, we have 55 (2 traces selected from 10 latency groups with replacement, i.e., \( C_{10}^{2} \)) experiments for 10 groups and 2 selections. Note that, even if the latency group is the same, since we choose a trace randomly from a latency group, the trace can still be different for each core.

C. Generating ML Models and PSC Pruning

To generate the 1C dataset (PSC and associated IPC values), we run the 1C experiments using all possible PSCs generated from the prefetcher options that are available in the ChampSim repository, the 1st place (IPC P [39]), 2nd place (Bingo [3]), and 3rd place (MLOP [50]) winners of the 3rd data prefetching competition (DPC3 [43]), and the 1st place (EIP [48]), 2nd place (FNL+MMA [49]), and 3rd place (DJOLT [56]) winners of the 1st instruction prefetching competition (IPC1) [45]. To reduce the hardware overhead of Puppeteer, we avoid including multiple PSCs that cover the same traces. To this end, we initially ran 20 traces for 20M instructions with all possible PSCs (5 prefetching options in L1I$ \times 5$ prefetching options in L1D$ \times 6$ prefetching options in L2$ \times 2$ prefetching options in LLC = 300 PSCs). We summarize the different prefetchers that we evaluated in Table [VI].

For each trace, we sort the PSCs based on the corresponding IPC values in descending order. We generate a new table for each trace, where the table contains the top 10 PSC entries for the trace and combine these tables to form a super-table that contains the top 10 PSCs for all traces. Note that a PSC may be in the top 10 for more than one trace. We sort the PSCs in descending order based on the number of traces for which the PSC is in the top 10. Starting from the top, we select just enough PSCs to improve performance of all the 20 traces. We picked the PSCs that have the best performance with minimal coverage overlap while reducing the number of unique prefetchers (to reduce the hardware overhead). In Table [VI], we show the final 5 PSCs that we selected. These PSCs give good performance for the maximum number of traces. We show the prefetcher used at each cache level. It is interesting to note that the best Prefetchers from DPC3 and IPC1 – IPCP and EIP – are not used in the top 5 choices for PSCs. This shows that the state-of-the-art prefetchers designed in isolation may not be the best choice of prefetchers when used with other prefetchers.

We collect the 4C STS and 4C MTS datasets, in the same way as the 1C dataset – the only difference is that the data is collected per core. We then train BT and Puppeteer using datasets collected from 1C, 4C STS, and 4C MTS. We denote the different flavors of the two algorithms as P1C, P4CS, and P4CM for Puppeteer; and B1C, B4CS, and B4CM for BT.

V. EVALUATION RESULTS

A. Puppeteer in a 1C Processor

In this section, we present the processor performance analysis when using Puppeteer in 1C, 4C and 8C processors, a sensitivity analysis of how Puppeteer’s performance varies with cache size, and we explore the trade-off between performance improvement and hardware overhead when using Puppeteer. We evaluate Puppeteer using scope, accuracy, and power metrics. For the analysis presented in Sections [V-A] and [V-D], we assume a total hardware overhead budget of 10KB for storing the Puppeteer model, and
that Puppeteer generalizes quite well and has learned the underlying architectural phenomena. Compared to B1C for B4CS and B4CM, we observe 1% and 2% lower average performance, respectively. Furthermore, the performance loss for the worst case outlier increases to 30%. Finally, one thing to note about J3 is that its average IPC gain is 2.1% lower than B1C, yet the negative outliers are less in both quantity and magnitude. This is because J3 makes more conservative changes compared to BT since the algorithm cycles through the PSCs as part of a constantly ongoing trial phase. This means that, in a production capable system, J3 might have been more viable compared to BT. This is because processors have to ensure all applications retain or increase their performance across new processor generations.

B. Puppeteer in a 4C Processor

Here we discuss the use of Puppeteer trained using 1C, 4C STS and 4C MTS datasets, in a 4C processor. These cases are represented by P1C, P4CS and P4CM, respectively. In Figure 7 we show the IPC distribution of Puppeteer, and the various prior works in a 4C system while running 4C STS data suite. We observe that the average IPC gain of P1C over the no-prefetcher case is 25.8%. Compared to B1C, P1C has 4.2% higher average performance. The worst-case performance loss in B1C has gone up to 45%, while the worst-case loss of P1C is at only 19%. The number of traces that lose performance is 61 for B1C, while P1C has just 24 traces that lose performance. Compared to IPCP, EIP, NN, PY, and J3, our P1C achieves 10.8%, 4.8%, 8.7%, and 6.8%, 3.7% average IPC gain, respectively. One key observation here is that although P1C has only been trained on 1C data, it is still applicable to the 4C case and provides a clear advantage over prior work. This is important given that as the number of cores increases, the number of unique combinations of different traces that we will need to run in the multi-core processor increases exponentially (for a 4C processor we need to cover 2^32 \times 2.89 billion trace combinations). Therefore, generalization using only 1C data is an important aspect to consider when comparing ML-based algorithms. To further test Puppeteer and BT, we train both algorithms with 4C STS and 4C MTS data suites. For Puppeteer we observe that P4CS has 1.2% and P4CM has 2.2% better performance compared to P1C (see Figure 7). While for BT, B4CS has 4.0% and B4CM has 2.9% better performance compared to B1C. This means that Puppeteer is better at learning the underlying (micro)architectural behavior with a variety of traces running concurrently compared to the same trace running on all the cores. In contrast BT requires data collected specifically from the same set of experiments to achieve better performance.

In Figure 8 we show the IPC distribution of Puppeteer and the various prior work when running 4C MTS. P1C achieves 23% average performance gain over no prefetching. P1C’s average performance gain is also very close (<0.6% difference) to the average performance gain of P4CS and P4CM. Once again, we observe that Puppeteer is superior to BT in this regard with B1C achieving 5% lower performance.
Fig. 7: Normalized Performance of 4C Processor Running STS - Performance distribution of Puppeteer and prior work normalized to SPP. Here the reported performance is average performance across all the cores. See Table I for the notations used along the X-axis.

Fig. 8: Normalized Performance of 4C Processor Running MTS - Performance distribution of Puppeteer and prior work normalized to SPP. Here the reported performance is average performance across all the cores. See Table I for the notations used along the X-axis.

Fig. 9: Normalized Performance of 8C Processor Running STS - Performance distribution of Puppeteer and prior work normalized to SPP. Here the reported performance is average performance across all the cores. See Table I for the notations used along the X-axis.

Fig. 10: Normalized Performance of 8C Processor Running MTS - Performance distribution of Puppeteer and prior work normalized to SPP. Here the reported performance is average performance across all the cores. See Table I for the notations used along the X-axis.

gain than P1C. B1C’s performance gain is also 4% lower than B4CS and 4.5% lower than B4CM. When we observe the outliers, B1C has 23 outliers while P1C has only 3. While the worst case outlier in B1C has 7% performance loss compared to SPP, P1C has only 0.4% loss. Compared to IPCP, EIP, NN, and PY, J3, our P1C (and also P4CS and P4CM) achieves 14.5%, 5%, 12.8%, and 11.9%, 4.4% average IPC gain, respectively.

C. Puppeteer in an 8C Processor

Here we discuss the use of Puppeteer trained using 1C, 4C STS and 4C MTS datasets, in an 8C processor. These cases are represented by P1C, P4CS and P4CM, respectively. We conduct this 8C processor analysis to test if Puppeteer scales to a larger number of cores. For an 8C processor running STS, we observe several interesting trends (see Figure 9). P1C has 11.9% average IPC gain over no prefetching, which is 4.8% higher than B1C. With P4CS and P4CM our IPC gain is 12.7% and 12.9%, respectively, over the no prefetching case. This means that to train Puppeteer for a multicore processor, we should have at least some data corresponding to a multicore processor in our dataset. It should be noted that, compared to the no prefetching case, P1C, P4CS and P4CM have lower IPC gain in the 8C processor than the 4C processor, which in turn has lower performance gain than the 1C processor.

This is because prefetching is much harder to do in multi-core processors. The overall benefit of prefetching goes down in multi-core processors and Puppeteer has lower possible peak performance. Comparatively, B1C has almost 0% performance gain over SPP. Even a static PSC, namely EIP, has 5.5% higher average IPC compared to B1C. P1C also gives comparable performance to B4CS and B4CM even though P1C was not trained using any data from a multicore processor. When we observe the outliers, B1C has 83 outliers with worst case performance loss of 62%; while, P1C has 47 outliers with worst case performance loss of 35%. Compared to IPCP, EIP, NN, PY, and J3, our P1C achieves 5.9%, 0.2%, 6.5%, and 4.4%, 1.2% average IPC gain, respectively.

When using the 8C MTS (see Figure 10), we observe similar trends to when using 8C STS. P1C has 2% better average IPC than B1C and comparable performance to B4CS and B4CM. P4CS and P4CM achieve 4% and 4.4% better average IPC compared to B1C. Compared to IPCP, EIP, NN, and PY, J3, our P1C achieves 6.9%, 1.6%, 6.6%, 7.6%, and 3.1% average IPC gain, respectively.

D. Puppeteer Performance vs Different Cache Sizes

In this subsection we discuss how the performance of BT, SPP and Puppeteer varies with cache size. We train both models only using data collected on a 1C processor with 32KB L1I$, 48KB L1D$, 512KB L2$, and 2MB LLC. In Figure 11 we show the average IPC values of BT (i.e. B1C), SPP, and Puppeteer (i.e. P1C) for $0.5 \times$, $1 \times$, $1.5 \times$, and $2 \times$ the nominal L1$ and L2$ sizes. P1C is affected by L1$ size slightly more than L2$ size but the difference is small (at most 0.4% more performance at $2 \times$ L1$ compared to $2 \times$ L2$). At $0.5 \times$ L1$ size P1C has 1.5% lower performance compared to the performance of P1C at nominal cache size. At $2 \times$ L1$ size P1C has 1.1% better performance compared to the performance of P1C at nominal cache size. At all cache sizes, P1C performs at least 1% better than B1C with the largest performance difference of 2.3% at nominal cache size. SPP performance swings by 5.5% between the $2 \times$ L1$ and the $0.5 \times$ L1$, and by 3.7% between the $2 \times$ L2$ and the $0.5 \times$.
L1$. In contrast, P1C has only a 2.9% swing. This means that with P1C we are already operating close to the possible peak performance and so increasing the cache size does not have a significant effect on the performance.

### E. Puppeteer Performance vs Different Hardware Overheads

In this subsection we study the performance of Puppeteer and NN when we have four different hardware overhead budgets – 1KB, 5KB, 10KB, and 100KB. Here we train a different Puppeteer model and a NN model for each hardware overhead budget. In Table VII we show the total area and power required for the NN and Puppeteer. All designs in Table VII are such that they need less than 1% of the instruction widow time to choose a PSC. We calculate the power, area, and delay values using Cadence Genus and SRAM array compiler for 22 nm GLOBALFOUNDRIES® (GF22FDX) [9].

To select a PSC, Puppeteer just traverses through the random forest for each PSC. If we evaluate all 5 forests in series, where we will require a maximum 250 comparison operations (5 forests × 5 trees per forest × 10 comparisons for 1KB, 5KB, and 10KB; 20 comparisons for 100KB) = 250 or 500 comparisons), it will take less than 0.5% of the total time required to execute the 100K instructions in the instruction window (assuming each instruction takes on average a clock cycle). Thus, we end up using the chosen PSC for 99.5% of the instruction window for Puppeteer. In contrast, the NN will require a multiply and addition operation for each weight, as well as a division and ReLu function at the end of each layer to determine the PSC. Due to the heavy computation required, as the size of the NN increases, to choose a PSC in less than 1% of the instruction window time, NN will need to parallelize the operations, which will require additional logic and memory components.

In Figure 12 we show the average IPC for 1C for the differently sized models. As it is immediately apparent, Puppeteer provides good performance improvement even when using a small model that fits within 1KB, while NN does not provide any performance improvement until we use a model that requires 10KB. At 10KB model size, a 1C processor with a NN manager has 11.8% lower average IPC as compared to a 1C-processor with Puppeteer. The NN also has almost 3× larger area and 11× larger power as compared to Puppeteer. If we compare 100KB NN to 1KB Puppeteer, then using Puppeteer provides 11.6% performance improvement, while NN provides 9.7% performance improvement while the area and power of 100KB NN is 76× and 185×, respectively, that of Puppeteer. Therefore, NN is not suitable for hardware prefetcher adaptation.

### F. Puppeteer Power Analysis

In Figure 13 we show the average power consumed in the caches for various static PSCs and the prior managers compared to Puppeteer. Compared to the no prefetching case, overall Puppeteer has 65% higher power consumption. Compared to BT (average of B1C, B4CS, and B4CM), Puppeteer (average of P1C, P4CS, and P4CM) has 9% lower power average. While NN and J3 have 6.3% and 2.2% lower average power than Puppeteer, as we have discussed they also have significantly lower average IPC. For the static PSC, EIP is extremely power hungry, with the highest average power that is 20.4% more than Puppeteer. IPCP and NO have lower power consumption than Puppeteer but they also have the worst performance among all options we have considered.

### G. Puppeteer’s impact on Accuracy and Scope

In Figure 14 we compare the prefetching scope of the prior works and Puppeteer. Here we determine scope as the number of total misses reduced by the prefetcher or prefetching system, divided by the total number of misses with prefetching disabled. We observe very limited scope across the 4 levels of the memory hierarchy for NN and J3. This is probably one of the reasons these options have lower performance than BT and Puppeteer. Comparing BT (average of B1C, B4CS, and B4CM), Puppeteer (average of P1C, P4CS, and P4CM), in L1D$ and L2$ BT achieves a marginal difference with 0.5% broader scope than Puppeteer. In L1I$ cache BT actually has 3.3% broader scope compared to Puppeteer. However, Puppeteer has 4.8% broader scope compared to BT in LLC. Intuitively, since LLC penalties are more important than L1I$, L1D$, and L2$ penalties, this is a better outcome.

| Algorithm | Area (µm²⁻¹) | Area Norm. | Power (µW) | Power Norm. |
|-----------|-------------|------------|------------|-------------|
| Puppeteer 1KB | 5,000 | 1× | 4.7 | 1× |
| Puppeteer 5KB | 10,000 | 2× | 8 | 1.7× |
| Puppeteer 10KB | 18,000 | 3.6× | 9 | 1.9× |
| Puppeteer 100KB | 140,000 | 28× | 39 | 8.3× |
| NN 1KB | 17,000 | 3.4× | 14 | 3× |
| NN 5KB | 40,000 | 8× | 65 | 13.8× |
| NN 10KB | 35,000 | 11× | 100 | 21× |
| NN 100KB | 380,000 | 76× | 80 | 189× |

**TABLE VII: Power and Area for various sizes of Puppeteer and NN:** Here we use SRAM compiler for designing Node MEM, and design the compute logic using RTL and then synthesize it using Cadence Genus for GF22FDX® [9]. Power is given over one instruction window. Norm. values are w.r.t. to Puppeteer 1KB values.
Fig. 13: Average power of Puppeteer and prior work normalized to SPP: Here 1C = 1C data suite, 4CS = 4C single-type trace set data suite, 8CM = 8C mixed-type trace set data suite, 8CS = 8C single-type trace set data suite, and 8CM = 8C mixed-type trace set data suite.

Fig. 14: Average scope of Puppeteer and the prior works in a 1C processor: See Table III for the notations used along the X-axis.

Fig. 15: Average prefetching accuracy of Puppeteer and the prior works in a 1C processor: See Table III for the notations used along the X-axis.

Experimentally, our results also support this outcome since Puppeteer has better performance than BT.

In Figure 15 we compare the prefetching accuracy of Puppeteer and the prior works. Here accuracy of a prefetcher is measured as the number of misses that a prefetcher or prefetcher system has reduced compared to the case when prefetching is disabled, divided by the number of misses caused by the prefetcher. Puppeteer is better than the other options in L1I$ and L1D$, but comparable in L2$. In LLC, J3 fares better than the other options with only 1.5% lower accuracy than Puppeteer. In case of BT and NN, Puppeteer achieves 21% better accuracy compared to BT and 28% better accuracy compared to NN. It is also of note that since the accuracy of Puppeteer in L1I$ is 6.7% better compared to BT, this better accuracy plays a role in compensating for the broader L1I$ scope of BT compared to Puppeteer.

H. Puppeteer-based Temporal variations in PSC

In Figure 16 we show the temporal behavior of P1C, B1C, and J3 while running 429.mcf-217B as an example. Figure 16a shows the percentage of time for which each PSC was used by each manager algorithm when executing 1.2B instructions of 429.mcf-217B. In Figure 16b, we show the IPC values and the PSC used in each instruction window for a small slice of the same trace. We would like to note three interesting observations: (i) From Figure 16a, both B1C and P1C use *ful-bingo-spp-no* for the 80% of the instruction windows, yet the performance difference between the two is around 20% over the whole trace. This means the PSC chosen in the remaining 20% of the instruction windows have a larger influence on the overall performance. (ii) In the first 25 instruction windows after the 5000th instruction window, there is a large variation in IPC gain when using B1C as compared to P1C, while all three algorithms converge to the same performance and same PSC during the last 25 instruction windows. This shows that P1C does a better job at predicting the PSC in different regions of an application. (iii) J3 uses the same PSC as P1C yet has lower performance in the first 25 instruction windows. This illustrates that changing the PSC has a cumulative effect on IPC. The choice of PSC made by P1C in prior instruction windows allowed P1C to gain more performance in the given instruction windows compared to J3.

VI. CONCLUSION AND FUTURE WORK

In this work, we introduce Puppeteer, a novel ML-based prefetcher manager designed using custom tailored random forests. We train a dedicated random forest for each PSC, which allows the random forest to retain more information in a smaller amount of hardware. For the 232 traces that we evaluated, Puppeteer achieves an average performance gain of 46.0% in 1C, 25.8% in 4C, and 11.9% in 8C compared to a system with no prefetching. Puppeteer also reduces the number of negative outliers by 89%. As future work, we will explore a unified design of a ML-based manager that selects from an array of ML-based prefanchers. In addition, we will also consider online training to further improve the performance of Puppeteer.
[47] J. Rogers, “Effects of an lstm composite prefetcher,” 2019.
[48] A. Ros and A. Jimborean, “The entangling instruction prefetcher,” IEEE Computer Architecture Letters, vol. 19, no. 2, pp. 84–87, 2020.
[49] A. Szenez, “The full mma instruction cache prefetcher,” 2020.
[50] M. Shakerinava, M. Bakshahilpour, P. Lotfi-Kamran, and H. Sarbazi-Azad, “Multi-lookahead offset prefetching,” 2019.
[51] M. Shevgoor, S. Koladiya, R. Balasubramonian, C. Wilkerson, S. H. Pugsley, and Z. Chishliti, “Efficiently prefetching complex address patterns,” in 2015 48th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO). IEEE, 2015, pp. 141–152.
[52] Z. Shi, A. Jain, K. Swersky, M. Hashemi, P. Ranganathan, and C. Lin, “A neural hierarchical sequence model for irregular data prefetching,” 2019.
[53] Z. Shi, A. Jain, K. Swersky, M. Hashemi, P. Ranganathan, and C. Lin, “A hierarchical neural model of data prefetching,” in Proceedings of the 26th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, 2021, pp. 861–873.
[54] S. Somogyi, T. F. Wenisch, A. Ailamaki, B. Falsafi, and A. Moshovos, “Spatial memory streaming,” ACM SIGARCH Computer Architecture News, vol. 34, no. 2, pp. 252–263, 2006.
[55] S. Srinath, O. Mutlu, H. Kim, and Y. N. Patt, “Feedback directed prefetching: Improving the performance and bandwidth-efficiency of hardware prefetchers,” in 2007 IEEE 13th International Symposium on High Performance Computer Architecture. IEEE, 2007, pp. 63–74.
[56] A. Srivastava, A. Lazaris, B. Brooks, R. Kannan, and V. K. Prasanna, “Predicting memory accesses: the road to compact ml-driven prefetcher,” in Proceedings of the International Symposium on Memory Systems, 2019, pp. 461–470.
[57] D. Steinberg, “Cart: classification and regression trees,” in The top ten algorithms in data mining. Chapman and Hall/CRC, 2009, pp. 193–216.
[58] Z. Wang, D. Burger, K. S. McKinley, S. K. Reinhardt, and C. C. Weems, “Guided region prefetching: A cooperative hardware/software approach,” in 30th Annual International Symposium on Computer Architecture, 2003. Proceedings. IEEE, 2003, pp. 388–398.
[59] T. F. Wenisch, M. Ferdman, A. Ailamaki, B. Falsafi, and A. Moshovos, “Practical off-chip meta-data for temporal memory streaming,” in 2009 IEEE 15th International Symposium on High Performance Computer Architecture. IEEE, 2009, pp. 79–90.
[60] C.-J. Wu, A. Jaleel, W. Hasenplaugh, M. Martonosi, S. C. Steely Jr, and J. Emer, “Ship: Signature-based hit predictor for high performance caching,” in Proceedings of the 44th Annual IEEE/ACM International Symposium on Microarchitecture, 2011, pp. 430–441.
[61] W. A. Wulf and S. A. McKee, “Hitting the memory wall: implications of the obvious,” ACM CAN, vol. 23, no. 1, pp. 20–24, 1995.
[62] Y. Zeng and X. Guo, “Long short term memory based hardware prefetcher: a case study,” in Proc. Memsys, 2017, pp. 305–311.
[63] N. Zhang, K. Zheng, and M. Tao, “Using grouped linear prediction and accelerated reinforcement learning for online content caching,” in 2018 IEEE International Conference on Communications Workshops (ICC Workshops). IEEE, 2018, pp. 1–6.
[64] P. Zhang, A. Srivastava, B. Brooks, R. Kannan, and V. K. Prasanna, “Raop: Recurrent neural network augmented offset prefetcher,” in The International Symposium on Memory Systems, 2020, pp. 352–362.