Near Threshold Computation of Partitioned Ring Learning With Error (RLWE) Hardware Accelerator on Reconfigurable Architecture

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Abstract

The Ring Learning With Error (RLWE) algorithm plays a crucial role in Post Quantum Cryptography (PQC) and Homomorphic Encryption (HE). The security of existing classical crypto algorithms is reduced in quantum computers. The adversaries can store all encrypted data, and once quantum computers become available, they can potentially expose this encrypted data. To address this emerging threat, researchers and cryptographers are actively developing and exploring quantum-resistant cryptographic algorithms like RLWE. On the other hand, the HE allows operations on encrypted data which is appropriate for getting services from third parties without revealing confidential plain-texts.

The Field Programmable gate Array (FPGA) based PQC and HE hardware accelerators like RLWE is much cost-effective than processor based platform and Application Specific Integrated Circuit (ASIC). FPGA based hardware accelerators still consume more power compare to ASIC based design. Near Threshold Computation (NTC) may be a convenient solution for FPGA based RLWE implementation. This paper implements RLWE hardware accelerator which has 14 subcomponents. This paper creates clusters based on the critical path of all 14 subcomponents. Each cluster is implemented in an FPGA partition which has the same biasing voltage $V_{ccint}$. The clusters that have higher critical paths use higher $V_{ccint}$ to avoid timing failure. The clusters have lower critical paths use lower biasing voltage $V_{ccint}$. Any timing error causes fr NTC can be caught by the RAZOR flipflop used in each subcomponents of RLWE. This voltage scaled, partitioned RLWE can save $\sim 6\%$ and $\sim 11\%$ power in Vivado and VTR platform respectively. The resource usage and throughput of the implemented RLWE hardware accelerator is comparatively better than existing literature.

Keywords: FPGA partition, Low Power, Post Quantum Cryptography, Ring Learning With Error

1. Introduction

Lattice based cryptography is currently considered as one of the most secure solutions compared to classical cryptographic schemes. The discrete logarithm (Elliptic Curve Cryptography), RSA and ECDSA classical schemes are used to secure modern Internet communications. These asymmetric key crypto-systems are based on the hardness of prime factor and discrete logarithm. However, asymmetric key crypto-systems are no longer secure under quantum attacks. Even in brute force, Grover’s quantum algorithm \cite{1} reduces the searching space of symmetric key cryptography: Advanced Encryption Scheme (AES) from $O(2^n)$ to $O(2^{n/2})$, where $n$ is the key size. Therefore the security AES-256 is comparable to AES-128 in quantum computer. However, no such computationally strong quantum computer has been developed yet. IBM and Google have claimed to develop such computationally extensive quantum computers within a few years. Post-quantum crypto algorithms generally deal with non-quantum operations but it strongly resists both classical and quantum attacks. Mainly there are four post quantum cryptography schemes are avialable: (i) Code based cryptography, (ii)Lattice based cryptography, (iii)Hash based cryptography and (iv)Multivariate quadratic cryptography. Among all these schemes lattice based cryptography (LBC) is computationally efficient. On 2005, O. Regev \cite{2} first introduced a lattice based cryptography (LBC) scheme name as Learning With Error (LWE). Later LBC becomes more popular for its significant theoretical progress \cite{2,3}. The LBC becomes more suitable for real life applications when it was implemented in software and hardware platform by articles...
On the other hand, post-quantum cryptography finds its application in more advanced schemes such as fully homomorphic encryption, which allows the operations on the encrypted data without revealing any information to the third party.

For hardware implementation of RLWE as PQC and HE, designer can choose two platforms: FPGA or ASIC. In practical, FPGA based PQC and HE hardware accelerators like RLWE is much cost-effective compared to ASIC. However, FPGA based hardware accelerator is less energy efficient compared to ASIC because of its programmable switch. An experimental study shows power consumption of 8 bit full adder in Xilinx XC4003A is 100 times more compared to CMOS ASIC platform. The implementation of 8-bit adder in FPGA platform consumed the power 4.2mW/MHz at 5V and the same implementation in ASIC consumed 5.5uW/MHz at 3.3V. The power consumption of FPGA based design is crucial specially for battery powered embedded system. NTC may be an appropriate solution to reduce the power consumption of FPGA based RLWE implementation.

To the best of our knowledge, all the existing RLWE implementations focus on speed and resource optimization whereas, this is the first reported work which tries to reduce power consumption of RLWE.

1.1. Related Work

O. Regev introduced the first hardness proof of LWE cryptography in 2005. Later, various hardware and software implementation of LWE were proposed. There are many literature which implemented various subcomponents of RLWE algorithm. The polynomial multiplication, polynomial division and gaussian sampler used to generate error polynomials are the most challenging subcomponents of RLWE. Howe et. al proposed a hardware architecture for a standard lattice based cryptography (LWE) on a Spartan-6 FPGA platform in 2016. The primary contribution of this paper is area optimization of Gaussian Sampler by balancing area and performance. Poppelman et al. reported a hardware implementations of Gaussian sampler of RLWE accelerator. They implemented Cumulative Distribution Table (CDT) based Gaussian sampler on reconfigurable hardware. Authors also compared CDT based implementation with Knuth Yao algorithm. Roy et al. implemented Gaussian sampler for sampling from the discrete gaussian using Knuth Yao algorithm. Poppelman et al. implemented a polynomial multiplier which stores all twiddle factors in a dedicated memory required for NTT computation. Article reduced the key size of the conventional LWE schemes and implemented a compact and efficient LWE hardware. The article compared LWE hardware and software implementations with Lindner and Peikert’s design. Article introduced LWE-matrix and LWE-polynomial and compared these variants of LWE. Article discarded the idea of LWE-matrix because of its large area consumption, they have only implemented RLWE-polynomial. Poppelman et al. implements an efficient hardware of RLWE on Virtex 6 FPGA which can fit on a low-cost Spartan-6 FPGA. This hardware accelerator improved the work of. Article proposed a lightest RLWE encryption scheme by reducing the resource, compared with the high speed implementation of. Roy et al. implemented a compact ring-LWE coprocessor on Virtex 6 FPGA where they optimized NTT polynomial multiplication and reduced the computation cost of the twiddle factors by avoiding the pre-computation overhead. A variation of the Native Title Research Unit (NTRU) Encrypt system with a quantum security reduction is used in article. Its security is based on the standard model’s LWE problem in polynomial rings. All the above mentioned RLWE implementations have mostly focussed on area versus speed issue. More speed causes more area and more area causes more power consumption. Without affecting the datapaths (area vs speed), the conventional low power solutions mostly deal with clock gating, power gating, dynamic voltage and frequency islands, retention power gating, save and restore power gating architectures. To the best of our knowledge, this is the first RLWE hardware accelerator based on dynamic voltage island concept where different voltage islands run with near threshold voltages.

1.2. Proposed RLWE

The literature of RLWE competes the growing high speed applications by increasing throughput of the architecture. The throughput is mostly achieved by more parallelism which causes more power consumption. Power consumption is a severe concern for embedded systems but existing literature has not explored the possibilities of NTC in any PQC and HE implementations. To the best of our knowledge our proposed RLWE is the first NTC in FPGA and ASIC platform. In our implementation we designed a RLWE dedicated hardware which has 14 subcomponents. The critical path of all these subcomponents are measured and based on the critical path, 4 cluster algorithms create groups with these 14 subcomponents. The FPGA is partitioned and different partitions has different biasing.
voltage $V_{ccint}$. The group having higher value of critical path is placed in a partition which have higher $V_{ccint}$ and the group having lower value of critical path is placed in a partition which have lower $V_{ccint}$. The primary contribution of our paper is stated below:

- This paper designs and implements RLWE crypto algorithm in Artix-7 (xc7a100tcsg324-3, 28nm) commercial FPGA and other 3 different academic FPGAs. The implemented RLWE hardware accelerator has 14 subcomponents such as Random Number Generator (RND), Poly_div, NTT Controller, Polynomial Multiplier, Read only Memory (ROM), Scanner, Datapath Controller, Convolution Controller, Poly_add, reader, Distance, Row Column Controller and 2 dual port Random Access Memory (RAM).
- The cluster algorithms create groups of subcomponents which have similar critical paths. Different groups are placed in different FPGA partitions. Each partition runs with different $V_{ccint}$. The groups with lower critical path are placed in a lower $V_{ccint}$ partition and the groups with higher critical path are placed in a higher $V_{ccint}$ partition. The timing errors causes from the reducing $V_{ccint}$ are handled by the Razor Flipflops.
- The proposed FPGA based voltage scaled RLWE can save 11% power consumption in VTR tool. The throughput, resource and power consumption of proposed RLWE is reasonably better compared to existing RLWE.

The rest of the paper is organised as follows: Sec. 2 states the background of the RLWE algorithm followed by Sec. 3 which gives a preliminary idea about hardware implementation of RLWE. Next, in Sec. 4 the The tool flow of the proposed model is described. In Sec. 5 the four cluster algorithm used to partition the FPGA is discussed and in Sec. 6 and Sec. 7 the proposed algorithm to calculate biasing voltage and results are stated respectively. Finally, Sec. 8 concludes the paper

2. The Ring-LWE Schemes

The Learning With Error (LWE) was proposed by O. Regev in [20] 2005. The LWE become popular because it is developed in secure lattice based cryptosystem which resists quantum attacks. Later LWE achieves computational efficiency and it reduces the key size by adopting polynomial Ring [17]. The LWE schemes perform in $R_q = \mathbb{Z}_q[x]/<f>$, where $f$ is irreducible polynomial of degree $n - 1$, and $n = 2^k \geq 1$ and a prime $q$ is chosen such a way that $q \equiv 1 \mod 2^n$. There is an error distribution called discrete Gaussian distribution $\chi_\sigma$ with the standard deviation $\sigma > 1$ and mean 0. The LWE scheme defined as follows:

- KeyGEN($a$): choose $r_1, r_2 \in R_q$ sampled from $\chi_\sigma$. Let $p = r_1 - a \ast r_2$. The public key is $(a, p)$ and private key is $r_2$. The polynomial $a \in R_q$ chosen uniformly during the key generation.
- Encryp($a, p, m$): choose error polynomials $e_1, e_2, e_3 \in R$ sampled from $\chi_\sigma$. Then compute the cipher text as a polynomial
  \[ c_1 = a \ast e_1 + e_2 \]
  \[ c_2 = p \ast e_1 + e_3 + \tilde{m} \]
  where $\tilde{m} = \text{misencode}(m)$ and $c_1$ and $c_2$ are the encrypted message.
- Decryp($c_1, c_2, r_2$): Decryption process requires to compute below equation.
  \[ m' = c_1 \ast r_2 + c_2 \]
  Thereafter, to get the original message $m$, it needs to decode $m'$.

3. Hardware Architecture of RLWE

The proposed RLWE has 14 components such as Random Number Generator (RND), Polynomial Divider (Poly_Div), NTT Controller, Polynomial Multiplier, Polynomial Subtraction (Sub_mod), Scanner, Datapath Controller, Convolution Controller, Polynomial Adder (Poly_add), reader, Distance, Row Column Controller and 2 dual port Random Access Memory (RAM). The main components in the architecture are: the memory file, Gaussian sampler, random number generator, NTT controller and datapath controller. The brief description of all hardware components are stated below:
3.1. Random Number Generator (RND)

This paper uses Trivium Random number generator to generate error polynomial $e_1$. In our application the secret key required for the RLWE is predefined. In real application the secret key should be generated randomly which can be done by the Trivium Random Number Generator. Trivium require one key and initialize vector to generate random numbers.

3.2. Polynomial Divider (poly_div)

The polynomial divider is required to divide polynomials. The resultant value of all the arithmetic operations stated in equ. 1, equ. 2 and equ. 3 need to bring under $R_q = \mathbb{Z}_q[x]/<f>$. 

3.3. Dual Port RAM

This RAM stores the public key, message, gaussian sample value required for RLW execution. The dual port memory architecture allows parallel reading and writing operation of polynomial coefficients. The RLWE needs to handle huge number of polynomial coefficients. The parallel read write operation of these polynomial coefficients increases the RLWE throughput significantly.

3.4. Datapath Controller

The Datapath Controller has three sub components such as: Polynomial Multiplier, Polynomial Adder(poly_add) and Polynomial Subtraction(Sub_mod) which are used to multiply, addition and subtraction of the polynomials. 

3.4.1. Polynomial Multiplier

The polynomial multiplier (poly_mul) is required to multiply $a$ and $e_1$ in equ. 1 and $p$ and $e_1$ in in equ. 2. The implemented polynomial multiplier is based Fast Fourier Transform (FFT) which has the lowest timing complexity among all available algorithm for polynomial multiplier.

3.4.2. Polynomial Adder (poly_add)

The polynomial Adder (Poly_add) is required to add polynomials $a \ast e_1$ and $e_2$ in equ. 1 and $p \ast e_1$, $e_3$ and $\tilde{m}$ in equ. 2. In this implementation we used usual process of polynomial addition. This block reads coefficients of polynomials from RAM and add them one by one.

3.4.3. Polynomial Subtraction (Sub_mod)

The Polynomial Subtraction (Sub_mod) is required to subtract polynomials. This block is required when Polynomial Divider (poly_div) will perform. The working principal of polynomial subtraction is similar to polynomial addition. The negative number is complemented here.

3.5. Convolution Controller

The convolution controller decides whether addition or multiplication will be executed. This block used to control the Datapath Controller.

3.6. Reader

The reader block perform loading operation to load the coefficients of polynomials and Gaussian noise coefficients. It also encode the message bit before make into cipher text.

3.7. NTT Controller

In RLWE scheme, polynomial multiplication is one of the the main operation of the encryption and decryption process. hardware implementation of coefficient wise multiplication of two polynomial functions is computationally expensive. Therefore, we convert the coefficient wise representation to point wise representation using the Number Theoretic Transformation (NTT). NTTController performs the NTT operation on the polynomial functions $a$, $p$, $r_2$, $e_1$, $e_2$, $e_3$ to generate $\tilde{a}$, $\tilde{p}$, $\tilde{r}_2$, $\tilde{e}_1$, $\tilde{e}_2$, $\tilde{e}_3$.
3.8. Gaussian Sampler: scanner, distance, row column controller

The Gaussian Sampler is based on Knuth Yao Sampler \[19\]. The Knuth Yao Sampler is a tree based sampler which stores the binary expansion of the samples in a probability matrix. This probability matrix stores probabilities of the samples. Roy et al.\[7\] implemented the first hardware of Gaussian sampler using Knuth Yao algorithm which used pre-computed table of the probability matrix. Knuth Yao algorithm uses a random walk model for sampling process. This sampling process creates a discrete distribution generating (DDG) tree using the probability matrix. Our Gaussian Sampler has three subcomponents such as: scanner, distance, row column controller modules which are dedicated for traversing the tree, scanning the bit from the ROM and calculate the distance in the tree of visited node and intermediate node. The detail of the Knuth Yao sampler and DDG tree are describe in \[19\].

3.8.1. Scanner

Scanner block performs the scanning operation on the ROM block. It scans the bits from a ROM word. When all bits are read from a ROM word then it fetch next ROM word to scan.

3.8.2. Row ColumnController

Row ColumnController has two registers: an up counter named as column_length and a down counter named as row_number. The column_length stores the length of the different column length of the probability matrix. At the first step of column scanning process, row_number is initialized by the column_length. If the row_number reaches to zero, the column scanning process is completed.

3.8.3. Distance

The distance block requires to construct the DDG tree of the probability matrix. For this purpose a subtracter is used to control the random walk. When the subtracter value is \(< 0\), then it indicates completion of the sampling operation. After the completion of the sampling operation, the row column controller selects current row_number as a sample output.

4. Tool Flow

This paper uses two environments 1)Python-Vivado and 2) Python-VTR. In Python-Vivado environment, the vivado generates the synthesis report which includes timing report of RLWE. The timing report consists of all timing related information of RLWE including the critical path length of all design paths. This timing report is sent to python environment to cluster the 14 subcomponents of RLWE using cluster algorithms mentioned in Sec. 5. This python environment generates the Xilinx Design Constraints (XDC) file which mentions coordinates of all 14 subcomponent of RLWE in FPGA floor. This coordinates of RLWE subcomponents are generated based on the partition or cluster. This XDC then includes in the implementation process of of Vivado environment. The Vivado used Artix 7, 28 nm FPGA. The VTR \[20\] also uses the same process as mentioned for Vivado. VTR generates Synopsys Design Constraint (SDC) file instead of XDC. The VTR uses 3 academic FPGAs: 22nm, 45nm and 180nm.

5. Cluster Algorithms

This paper analyses four cluster algorithms to group the different sub components of RLWE hardware accelerator. All these four algorithms follow different set of rules to find the similarity of the data in the data distribution. Based on our design requirements, this paper implements four cluster algorithms as stated below:

5.1. K-Means Clustering

K-Means cluster algorithm performs on data to find K divisions to satisfy a certain criteria. Firstly, it computes the distance between the data points and the randomly initialized centroids \[21\]. Thereafter, it creates cluster based on the distance of the data and the centre. This iterative process is repeated until the criteria of the functions converges to the local minimum. Euclidean distance is used to compute distances between the data. Its time complexity is \(O(Kn)\), where \(K\) is number of cluster and \(n\) is number of data. As shown in Table 1, the K-Means algorithm creates 5 clusters and each cluster is placed in each FPGA partition. The \(V_{comp}\) of Partition−1, Partition−2, Partition−3, Partition−4 and Partition−5 are 0.96, 1.00, 0.97, 0.98 and 0.94 respectively.
5.2. DBSCAN

DBSCAN cluster algorithm works on the assumption that clusters are in high-density regions and outliers tend to be in low-density regions. Unlike the K-Means algorithm, DBSCAN does not require the number of clusters beforehand. This algorithm finds the number of clusters \( \epsilon \text{ and } \text{minpoint} \). The \( \epsilon \): is a radius of the circle around a particular point that is to be considered as in the neighborhood of the other point. The \( \text{minpoint} \): is the threshold on the least number of points in the circle to be considered as core points. At the first step of DBSCAN choose an arbitrary point \( p \). DBSCAN assumes a circle which radius is \( \epsilon \) and centre is at \( p \). All the data points comes under this circle is grouped in a cluster. If there are less number of points than the \( \text{minpoint} \), \( p \) point is considered as noise. In a newly created cluster, if all points are marked as accessed, then same process used to deal with unvisited points and create a new cluster. This process will continue until all points are marked in cluster or noise. The main advantage of DBSCAN algorithm over the other algorithm is that it can identify the outlier point as a noise. The time complexity of this algorithm is \( O(n) \) for reasonable \( \epsilon \). As shown in Table 2, the DBSCAN algorithm creates 6 clusters. However the offline voltage calibration algorithms stated in Sec. 6.1 merge 6 clusters into 3 FPGA partitions, such as (i) FPGA Partition-1: Cluster - 1, Cluster - 2 and Cluster - 6 placed into FPGA Partition-1 where \( V_{ccint} = 0.96 \). (ii) FPGA Partition-2: contain Cluster - 3 where \( V_{ccint} = 0.98 \). (iii) FPGA Partition-3: Cluster - 4 and Cluster - 5 placed into FPGA Partition-3 where \( V_{ccint} = 0.97 \).

5.3. Mean-Shift Clustering

Mean Shift cluster \([23]\) algorithm is based on the concept of Kernel Density Estimation (KDE). KDE assumes that the data points are sampled from a probability distribution and estimate the distribution by a weight function named as Kernel on each point of the data set. Among many kernels, the Gaussian kernel is the most popular. The mean shift algorithm works in such a way that the points climb uphill to the nearest peak on the KDE surface by iteratively shifting of each point of the data set. It starts with a selected random point as a center of the kernel. It considers a circle which has certain radius in the data set. The kernel is then moved towards a higher density region by shifting the centroid towards the mean of the points within the said circle. The mean shift cluster does not need prior knowledge of the number of clusters. It needs only one parameter: bandwidth to determine the number of clusters. This clustering algorithm is computationally expensive compared to K-means algorithm and its time complexity is \( O(n \cdot \log(n)) \). As shown in Table 3, the K-Means algorithm creates 4 clusters and each cluster is placed in each FPGA partition. The \( V_{ccint} \) s of Partition - 1, Partition - 2, Partition - 3 and Partition - 4 are 0.96, 1.00, 0.97 and 0.98 respectively.

5.4. Hierarchical Clustering

At the first step, Hierarchical cluster \([24]\) algorithm considers every point as different clusters. Thereafter it computes distance matrix between two clusters based on a distance measurement method (in this case Euclidean distance). Then it merges two clusters which have the smallest distance. This process will repeat until all clusters grouped into a single cluster. The dendogram creates a binary tree for visualizing the hierarchy of clusters. The number of clusters can be determine from the dendogram. This algorithm is computationally expensive for large datasets, having a time complexity of \( O(n^2) \) where \( n \) is the number of data-points. As shown in Table 4 the Hierarchical Cluster algorithm creates 6 clusters. However the offline voltage calibration algorithms stated in Sec. 6.1 merge 5 clusters into 3 FPGA partitions, such as (i) FPGA Partition-1: Cluster - 1, Cluster - 5 placed into FPGA Partition-1 where \( V_{ccint} = 0.96 \). (ii) FPGA Partition-2: Cluster - 2 and Cluster - 4 placed into FPGA Partition-2 and fall into same voltage island where \( V_{ccint} = 0.98 \). (iii) FPGA Partition-3: contain Cluster - 3 where \( V_{ccint} = 0.97 \).
6. Voltage Calibration and Error Control Unit

The most challenging part of NTC is (i) Actual voltage allocation for specific FPGA partition and (ii) Detect run time timing errors.

6.1. Offline Voltage Calibration Algorithm

The proposed voltage scaled RLWE has 14 hardware components. These hardware components have different critical paths. The 4 cluster algorithms mentioned in Sec. 5 group these 14 components in different voltage island. Each FPGA partition has different biasing voltage \(V_{CCint}\). The designer knows if the critical path of a hardware components is more, it needs more amount of \(V_{CCint}\) to avoid timing failure. However, designer does not know the actual amount of \(V_{CCint}\) required for particular length of critical path. This calibration of \(V_{CCint}\) depends on several design constraints, such as number of partition \(P\), critical path \(C_i\) and critical region \((V_{ccintmax} - V_{ccintmin})\) as shown in Fig. 2. This Offline Voltage Calibration Algorithm has two parts: (i) Average Critical Path of each Partition shown in Algorithm 1 (ii) Voltage Scaling of each Partition shown in Algorithm 2.

Calculation of average critical path \(CP_k\) describes in Algorithm 1. Total critical path \(A_{critical}\) of each partition is computed in Line 4 of Algorithm 1. Thereafter, Line 6 calculates the average critical path \(CP_k\) of \(k^{th}\) partition based on \(A_{critical}\) and number of components \(N(k)\) in \(k^{th}\) partition. The distributed scaled voltage \(VP_k\) for each partition is computed by Algorithm 2. It calculates voltage \(V_{r/c}\) for per unit critical path from \(V_{ccintmax}\) and \(V_{ccintmin}\) as shown in Line 5. After that, the biasing voltage \(VP_k\) of the \(k^{th}\) partition is calculated depends on the \(V_{r/c}\), average critical path \(CP_k\) and \(V_{ccintmin}\). The entire RLWE starts running with the calculated biasing voltages \(VP_k\) for its different FPGA partition. As the \(VP_k\) falls in the critical region shown in 2 the timing errors may occurred.

6.2. Timing Errors

Despite of accurate \(V_{CCint}\) allocation, NTC on RLWE may causes timing errors. This paper designs a timing error control unit which uses razor flip in the datapath of each RLWE subcomponents. The razor or shadow flipflop
in FPGA platform is driven by a delayed clock [25]. We have assumed that one or more timing pathways leading from any of the source registers terminate at a circuit register \( R \). The shadow register \( S \) samples the same data as the main register \( R \), but it does so on a delayed clock \( DCLK \) that is delayed from \( CLK \) by \( T_{del} \). Any data that enters the circuit after \( R \) samples but prior to \( S \) samples will result in a disparity between the two registers, which is identified by the error flag \( F \). This razor flipflop is put in the datapaths of the subcomponents. Razor increases the resource consumption, but it also has the ability to detect runtime timing errors in RLWE caused by near-threshold biasing voltage. Fig.3 displays the timing diagram for the razor. If Razor finds any error in particular partition of the FPGA the biasing voltage of that partition will be increased by one step. Following the method suggested in [26], the voltage boosting circuit can be constructed externally.

![Figure 2: Voltage behaviour for \( V_{CCint} \)](image)

![Figure 3: Razor Timing Diagram of Fault Detection](image)

**Table 1: K-Means Cluster**

| Cluster | Hardwares | Critical Paths(ns) | \( V_{CCint} \)(Volt) | FPGA Partition |
|---------|-----------|-------------------|----------------------|----------------|
| 1       | Dual port ram:1 | 2.217             | 0.96                 | 1              |
|         | Dual port ram:2  | 2.217             |                      |                |
|         | Row Column Controller | 1.9              |                      |                |
|         | Distance         | 1.9               |                      |                |
|         | reader Wrapper   | 2.394             |                      |                |
|         | Poly_add         | 2.101             |                      |                |
| 2       | Datapath         | 8.603             | 1.00                 | 2              |
| 3       | Scanner          | 3.332             | 0.97                 | 3              |
|         | ROM              | 3.654             |                      |                |
| 4       | Polynomial multiplier | 5.327         | 0.98                 | 4              |
| 5       | NTT Controller   | 1.17              | 0.95                 | 5              |
|         | Convolution Controller | 1.725     |                      |                |
|         | Poly_div         | 1.323             |                      |                |
|         | rand             | 1.412             |                      |                |
Table 2: DBSCAN Cluster

| Clusters | Hardwares                  | Critical Paths(ns) | $V_{ccint}(Volt)$ | FPGA Partitions |
|----------|----------------------------|-------------------|------------------|----------------|
| 1        | Dual port ram:1            | 2.217             | 0.96             | 1              |
|          | Dual port ram:2            | 2.217             |                  |                |
|          | reader Wrapper             | 2.394             |                  |                |
|          | Poly_add                   | 2.101             |                  |                |
| 2        | Row Column Controller      | 1.9               | 0.96             | 1              |
|          | Distance                   | 1.9               |                  |                |
|          | Convolution Controller     | 1.725             |                  |                |
| 3        | Datapath                   | 8.603             | 0.98             | 2              |
| 4        | Scanner                    | 3.332             | 0.97             | 3              |
|          | ROM                        | 3.654             |                  |                |
| 5        | Polynomial multiplier      | 5.327             | 0.97             | 3              |
| 6        | NTT Controller             | 1.17              |                  | 1              |
|          | Poly_div                   | 1.323             | 0.96             |                |
|          | rand                       | 1.412             |                  |                |

Table 3: Mean-Shift Cluster

| Cluster | Hardwares                  | Critical Paths(ns) | $V_{ccint}(Volt)$ | FPGA Partition |
|---------|----------------------------|-------------------|------------------|----------------|
| 1       | Dual port ram:1            | 2.217             |                  | 1              |
|         | Dual port ram:2            | 2.217             |                  |                |
|         | Row Column Controller      | 1.9               | 0.96             |                |
|         | Distance                   | 1.9               |                  |                |
|         | reader Wrapper             | 2.394             |                  |                |
|         | Poly_add                   | 2.101             |                  |                |
|         | NTT Controller             | 1.17              |                  |                |
|         | Convolution Controller     | 1.725             |                  |                |
|         | Poly_div                   | 1.323             | 0.96             |                |
|         | rand                       | 1.412             |                  |                |
| 2       | Datapath                   | 8.603             | 1.00             | 2              |
| 3       | Scanner                    | 3.332             | 0.97             | 3              |
|         | ROM                        | 3.654             |                  |                |
| 4       | Polynomial multiplier      | 5.327             | 0.98             | 4              |

Table 4: Hierarchical

| Cluster | Hardwares                  | Critical Paths(ns) | $V_{ccint}(Volt)$ | FPGA Partition |
|---------|----------------------------|-------------------|------------------|----------------|
| 1       | Dual port ram:1            | 2.217             |                  | 1              |
|         | Dual port ram:2            | 2.217             |                  |                |
|         | Row Column Controller      | 1.9               | 0.96             |                |
|         | Distance                   | 1.9               |                  |                |
|         | reader Wrapper             | 2.394             |                  |                |
|         | Poly_add                   | 2.101             |                  |                |
|         | Convolution Controller     | 1.725             |                  |                |
| 2       | Datapath                   | 8.603             | 0.98             | 2              |
| 3       | Scanner                    | 3.332             | 0.97             | 3              |
|         | ROM                        | 3.654             |                  |                |
| 4       | Polynomial multiplier      | 5.327             | 0.98             | 2              |
| 5       | NTT Controller             | 1.17              |                  | 1              |
|         | Poly_div                   | 1.323             | 0.96             |                |
|         | rand                       | 1.412             |                  |                |
Algorithm 1 Average Critical Path of each Partition

Require: \( n', P \) \( \rightarrow k \leftarrow 0, 1, 2, \ldots P \)

1: \( A_{\text{Critical}} \leftarrow 0 \)
2: for \( k \leftarrow 1 \) to \( P \) do
3: for \( i \leftarrow 1 \) to \( N(k) \) do
4: \( A_{\text{Critical}} \leftarrow A_{\text{Critical}} + C_i \)
5: end for
6: \( CP_K \leftarrow A_{\text{Critical}} / N(k) \)
7: end for

Algorithm 2 Voltage Scaling of each Partition

Require: \( V_{cc_{\text{int}}} \), \( V_{cc_{\text{min}}} \), \( CP_K \)

1: \( T_{\text{Critical}} \leftarrow 0 \)
2: for \( k \leftarrow 1 \) to \( P \) do
3: \( T_{\text{Critical}} \leftarrow T_{\text{Critical}} + CP_K \)
4: end for
5: \( V_{r/c} \leftarrow \frac{V_{cc_{\text{max}}} - V_{cc_{\text{min}}}}{T_{\text{Critical}}} \)
6: for \( k \leftarrow 1 \) to \( P \) do
7: \( VP_k \leftarrow V_{cc_{\text{min}}} + CP_K \times V_{r/c} \)
8: end for

7. Result and Implementation

As stated in Sec. 5, 4 cluster algorithms are implemented by using Scikit-learn library of python. The entire framework uses two environments (i) Commercial Vivado tool with Artix-7 FPGA (ii) VTR tool for 22nm, 45nm and 130nm academic FPGAs. This paper proposes two different architectures of RLWE encryption scheme for the parameter set \( (n, q, s) : (256, 7681, 11.32) \). The first approach implements RLWE hardware accelerator without voltage scaling, whereas the second RLWE architecture is designed with different voltage partitions. Presently, there is no FPGA which supports multiple \( V_{cc_{\text{int}}} \). Therefore, the power results are carried out separately where one partition is considered as an individual circuit. Both of these two designs should only be studied for critical region as shown in Fig. 3. However the design and tool constraints have forced us to study both the designs for critical region as well as guard band region. The \( V_{cc_{\text{int}}} \) of each partitions are calculated by algorithm 1 and 2.

7.1. Vivado and VTR: Voltage Region: \( V_{cc_{\text{int}}} = 0.95 \) volt to \( V_{cc_{\text{int}}} = 1.05 \) volt

The guard band voltage region of Artix-7 is \( V_{cc_{\text{int}}} = 0.95 \) volt to \( V_{cc_{\text{int}}} = 1.05 \) volt. Though academic FPGAs on VTR platform supports voltages of critical region, for sake of better comparative study we have implemented 14 components of RLWE with voltage range of \( V_{cc_{\text{int}}} = 0.95 \) volt to \( V_{cc_{\text{int}}} = 1.05 \) volt for both Vivado and VTR. Table 5 shows Vivado 28nm Artix-7, VTR 22nm, VTR 45nm and VTR 130nm can save 4.34%, 1.19%, 1.18% and 1% power respectively.

7.2. VTR: Voltage Region: \( V_{cc_{\text{int}}} = 0.5 \) volt to \( V_{cc_{\text{int}}} = 1.3 \) volt

Unlike VTR, Vivado does not allow any \( V_{cc_{\text{int}}} \) below 0.95 and above 1.05. As shown in Table 6, different number of clusters generated from K-Means, Mean-Shift, DBScan and Hierarchical algorithms consider voltage region from \( V_{cc_{\text{int}}} = 0.5 \) volt to \( V_{cc_{\text{int}}} = 1.3 \) volt for 22nm, 45nm and 130nm in VTR flow.
Table 5: Power Consumption of Vivado and VTR: Voltage Region: $V_{ccmin} = 0.95$ volt to $V_{ccmax} = 1.05$

| Our Design Under 25° Ambient Temperature & 100 MHz Clock | Cluster algorithms | Partition No. | $V_{com}$ Volt | Vivado 28nm | VTR 22nm | VTR 45nm | VTR 130nm |
|-------------------------------------------------------------|-------------------|---------------|----------------|-------------|-----------|-----------|-----------|
| Without Voltage scaling                                     | NA                | NA            | 1.00           | 22.45       | 46.44     | 59.09     | 190.38    |
| Voltage scaled                                              | K-Means           | Partition-1   | 0.96           | 21.48       | 45.89     | 58.402    | 188.49    |
|                                                            |                   | Partition-2   | 1.00           |             |           |           |           |
|                                                            |                   | Partition-3   | 0.97           |             |           |           |           |
|                                                            |                   | Partition-4   | 0.90           |             |           |           |           |
|                                                            |                   | Partition-5   | 0.95           |             |           |           |           |
| % of Reduction                                              |                   |               | 4.34           | 1.19        | 1.18      | 1.005     |           |
| Without Voltage scaling                                     | NA                | NA            | 1.00           | 22.45       | 46.44     | 59.09     | 190.38    |
| Voltage scaled                                              | Mean-Shift        | Partition-1   | 0.96           | 21.62       | 45.94     | 58.46     | 187.2     |
|                                                            |                   | Partition-2   | 0.97           |             |           |           |           |
|                                                            |                   | Partition-3   | 1.00           |             |           |           |           |
|                                                            |                   | Partition-4   | 0.98           |             |           |           |           |
| % of Reduction                                              |                   |               | 3.73           | 1.10        | 1.09      | 1.09      | 1.09      |
| Without Voltage scaling                                     | NA                | NA            | 1.00           | 22.45       | 46.44     | 59.09     | 190.38    |
| Voltage scaled                                              | DBSCAN            | Partition-1   | 0.96           | 21.16       | 45.87     | 58.38     | 188.5     |
|                                                            |                   | Partition-2   | 0.96           |             |           |           |           |
|                                                            |                   | Partition-3   | 0.97           |             |           |           |           |
|                                                            |                   | Partition-4   | 0.98           |             |           |           |           |
| % of Reduction                                              |                   |               | 5.78           | 1.21        | 1.21      | 0.99      |           |
| Without Voltage scaling                                     | NA                | NA            | 1.00           | 22.45       | 46.44     | 59.09     | 190.38    |
| Voltage scaled                                              | Hierarchical      | Partition-1   | 0.96           | 21.62       | 45.94     | 58.46     | 188.6     |
|                                                            |                   | Partition-2   | 0.96           |             |           |           |           |
|                                                            |                   | Partition-3   | 0.97           |             |           |           |           |
|                                                            |                   | Partition-4   | 0.98           |             |           |           |           |
|                                                            |                   | Partition-5   | 1              |             |           |           |           |
| % of Reduction                                              |                   |               | 3.73           | 1.10        | 1.09      | 0.93      |           |

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Table 6: Power Consumption for VTR, Voltage Region: \( V_{\text{cin}} = 0.5 \) volt to \( V_{\text{cin}} = 1.3 \)

| Our Design Under 25\(^{\circ}\) Ambient Temperature & 100 MHZ Clock | Cluster algorithms | Partition No. | \( V_{\text{TR}} \) | VTR 22nm | VTR 45nm | VTR 130nm |
|---|---|---|---|---|---|---|
| Without Voltage scaling | NA | NA | 1.00 | 46.44 | 59.09 | 190.38 |
| Voltage scaled | K-Means | Partition-1 | 0.96 | 41.41 | 52.69 | 179.55 |
| | | Partition-2 | 1.00 | | | |
| | | Partition-3 | 0.97 | | | |
| | | Partition-4 | 0.98 | | | |
| | | Partition-5 | 0.95 | | | |
| % of Reduction | 10.83 | 10.82 | 5.68 |
| Without Voltage scaling | NA | NA | 1.00 | 46.44 | 59.09 | 190.38 |
| Voltage scaled | Mean-Shift | Partition-1 | 0.96 | 41.71 | 53.28 | 181.2 |
| | | Partition-2 | 0.97 | | | |
| | | Partition-3 | 1 | | | |
| | | Partition-4 | 0.98 | | | |
| % of Reduction | 10.19 | 9.83 | 4.82 |
| Without Voltage scaling | NA | NA | 1.00 | 46.44 | 59.09 | 190.38 |
| Voltage scaled | DBSCAN | Partition-1 | 0.96 | 41.27 | 52.77 | 178.2 |
| | | Partition-2 | 0.96 | | | |
| | | Partition-3 | 0.97 | | | |
| | | Partition-4 | 0.98 | | | |
| % of Reduction | 11.15 | 10.71 | 6.38 |
| Without Voltage scaling | NA | NA | 1.00 | 46.44 | 59.09 | 190.38 |
| Voltage scaled | Hierarchical | Partition-1 | 0.96 | 41.48 | 53 | 181.1 |
| | | Partition-2 | 0.97 | | | |
| | | Partition-3 | 0.98 | | | |
| | | Partition-4 | 1 | | | |
| % of Reduction | 10.69 | 10.32 | 4.89 |

Table 7: Comparison of our design with other RLWE encryption schemes

| Design | Parameters \((n,q,s)\) | Device | Slice Registers/FF | Slice LUT | DSP BRAM | Critical Path (ns) | Throughput (bps) | Year |
|---|---|---|---|---|---|---|---|---|
| Our Design | (256,768,11.32) | Artix-7 | 695,595 | 346 | 2 | 1 | 2.539 | \( \sim 7.2 \times 10^6 \) | 2022 |
| RLWE | (256,768,11.32) | V6LX75T | 1506/725 | 1256 | 1 | 12 | - | \( \sim 9.73 \times 10^6 \) | 2013 |
| | (512,12289,12.18) | V6LX75T | 1887/746 | 595 | 1 | 14 | - | \( \sim 9.33 \times 10^6 \) | 2013 |
| RLWE | (256,768,11.32) | V6LX75T | -953 | 1536 | 1 | 3 | - | \( \sim 10.69 \times 10^6 \) | 2014 |
| | (512,12289,12.18) | V6LX240T | 143396/473 | 298016 | - | - | - | \( \sim 3.18 \times 10^6 \) | 2014 |
| | (256,4096,3.39) | S6LX45 | 1866/480 | 4804 | 1 | 5 | - | \( \sim 10.58 \times 10^6 \) | 2016 |
| | (256,768,11.32) | XC7A200 | 2122/620 | 5648 | 6 | 8 | - | \( \sim 16.99 \times 10^6 \) | 2018 |
| | (256,4096,3.39) | S6LX45 | 18864/480 | 6152 | 1 | 73 | - | \( \sim 0.32 \times 10^6 \) | 2018 |

As an example, K-Means algorithm generates five partitions. Algorithm calculates average critical path \( CP_k \) of
Table 6 shows adoption of voltage scaling technology reduces dynamic power consumption.

\[ \text{V}_{\text{ccint}} = 0.957 \approx 0.98, \text{V}_{\text{ccint}} = 0.955 \approx 0.95. \]

In Table 5, our voltage scaling method in same voltage ranges, reduces the dynamic power consumption 3.73% to 5.78% in Vivado environment and reduces 0.93% to 1.24% in VTR environment. Table 6 shows adoption of voltage scaling technology reduces dynamic power consumption 10.19% to 11.15%, 9.83% to 10.82% and 4.82% to 6.38% for 22nm, 45nm and 130nm VTR flow respectively. Table 7 shows comparison of resource and throughput of our RLWE hardware accelerator with existing literature. Though our paper does not claim any architectural contribution, Table 7 reports that resource usage and throughput are significantly better compared to existing RLWE.

8. Conclusion

This paper implements a low power RLWE hardware accelerator in Artix-7 28nm commercial FPGA, 22nm, 45nm and 130nm academic FPGA using Vivado and VTR tool. The proposed methodology creates clusters of subcomponents of RLWE based on its critical path. The FPGA floor is partitioned and different clusters are placed in different FPGA partitions. The clusters which have higher average critical path is connected with higher biasing voltage and the clusters which have lower average critical path is connected with lower biasing voltage to avoid the timing failure. This paper proposes an algorithm to calculate the actual biasing voltage required for certain amount of average critical path of a partition based on the available FPGA technology \( \text{V}_{\text{ccint}_{\text{min}}}, \text{V}_{\text{ccint}_{\text{max}}} \) and number of partitions. The Razor flipflop used in each subcomponents of RLWE can detect any timing error causes for NTC computation. This voltage scaled, partitioned RLWE can save \( \sim 6\% \) and \( \sim 11\% \) power in Vivado and VTR platform respectively. The resource usage and throughput of the implemented RLWE hardware accelerator is comparatively better than existing literature. Full version of this manuscript is available in IEEE Access [28].

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