A low power consumption and cost-efficient SEU-tolerant pulse-triggered flip-flop design

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Abstract A power-efficient Single Event Upset (SEU) -tolerant pulse-triggered flip-flop design is presented. The dual-modular redundant design takes advantage of concise formation of pulse-triggered designs, and avoids the disadvantages of it, such as high power consumption. Clock-gating scheme is applied to reduce power consumption. The static configuration and the avoidance of contention mechanism led to the balance of power consumption, speed and SEU tolerance. The SEU tolerance is evaluated by means of SEU cross section, which is significantly lower than conventional D flip-flop. The proposed flip-flop is designed in 55nm CMOS technology to evaluate performances. The proposed design achieves the lowest power consumption, which is even lower than conventional D flip-flop. Although the speed is sacrificed, the lowest power-delay product is achieved among hardened designs. The proposed design provides solution to speed-insensitive and power-constrained applications.

key words: single event upset, radiation hardening, power-efficient, flip-flop

Classification: Integrated circuits

1. Introduction

The scaling of the semiconductor technology leads to a higher vulnerability of integrated circuits to radiation-induced transient faults [1, 2, 3]. An erroneous change of the state held in a storage cell caused by a particle strike is called Single event upset (SEU), which is the key contributor to the overall system soft error rate in modern VLSI circuits [4]. The SEU robustness of flip-flops is essential to ensure the overall reliability since flip-flop is one of the major elements in many digital designs [5, 6]. Radiation Hardening by Design (RHBD) is an important technique to mitigate SEU in flip-flops as it works in commercial CMOS technology with no violation of design rules. The immunity against SEU is obtained through dedicated circuit design, with acceptable overheads [7, 8, 9, 10, 11, 12, 13].

Flip-flops occupy a large portion of chip area and contribute a significant part of overall power in the system. It has been reported that flip-flops and last sections of clock distribution network that directly drive flip-flops account for 90% of the clock system power [14, 15, 16]. It is crucial to design low-power radiation-hardened flip-flops with low penalties to meet strict demands of the industry. Redundant formation of hardened designs often causes high overheads. Pulse-Triggered Flip-Flop (PFF) is an option to help in penalty reducing or area diminishing due to its simple and compact structure [17, 18]. However, high power consumption due to redundant switching activities and contention mechanism is usually an issue [14, 19, 20, 21].

In this paper, we introduce a novel power-efficient dual-modular redundant SEU-tolerant pulse-triggered flip-flop design with clock-gating scheme and a static configuration to achieve cost-efficient SEU-immunity. The dual-modular design is formed by two concise PFFs and a C-element. It employs delayed clock signals to control the data paths and the logic keepers. No redundant switching activity occurs in internal nodes when input data remain constant. Clock-gating technique is adopted to suppress unnecessary switching activity of clocked transistors and local clock generator. Contention problem is avoided by breaking the logic keepers during the write phase. As a result, the power consumption is reduced. Simulations under 55nm CMOS technology indicate that compared with previous works, the proposed hardened flip-flop attains SEU tolerance with lower power consumption. The power-delay product is same as state-of-art hardened PFF. The power consumption is even lower than conventional master-slave D flip-flop (MS-DFF) at low data activities.

The rest of this paper is organized as follows: Section II has a brief discussion about previous works. Section III describes the proposed SEU-tolerant flip-flop. Section IV covers the implementation, simulation results and comparison to some previous designs. Section V concludes this paper.

2. Background

The conventional D flip-flop is susceptible to SEU [22, 23]. A common hardening technique involves replacing the dual-inverter latch in the flip-flop with a robust storage cell, such as the popular Dual Interlocked Storage Cell (DICE) [24] or Quatro [25]. The classic master-slave DICE flip-flop (MS-DICE FF) employs two DICE cells as storage elements. When any single node of the DICE cell is affected by a false transient, the state can be corrected by unaffected nodes.
This scheme faces high penalties on silicon area and power consumption [26, 27]. Some works restructure the flip-flop by Triple-Modular Redundancy (TMR) [28, 29]. The D flip-flop is replicated three times and the correct data will be extracted by a majority voter. However, TMR is limited by high area, power and delay overheads [8]. Dual-modular flip-flops based on C-element [30] achieves higher cost efficiency than TMR. For example, BISER [31]. The C-element virtually works as an inverter when the input values at the two input ports are identical. The area and power overheads are two times higher than conventional D flip-flop. A true single phase clock flip-flop named TSPC-DICE is area and speed efficient. However, the pre-charge action and the contention problem at the beginning of the write phase lead to high power consumption [20, 32]. Pulsed-Quatro is based on Quatro cell and two transfer gates. This structure shows low cell size but is power hungry [33]. Pulsed-DICE latch design is a cost-efficient PFF design [13], which clearly shows the superiority of pulse-triggered designs. But the reduction in power is limited because of unnecessary switching activities of clocked transistors and the pulse generator. Techniques in saving power of PFFs have been widely explored, for example, clock-gating techniques. Since plenty of power is usually dissipated by clocked transistors and local clock generator, clock-gating techniques could conditionally disable local clock signals when the input keeps unchanged to reduce power dissipation [21, 34].

3. Proposed design

As illustrated by Fig. 1, the proposed circuit is a dual-modular redundant PFF with clock-gating scheme. It consists of a clock signal generator, two copies of the internal circuits, and a C-element as the output stage. The input signal propagates through two identical data paths and converge to the C-element. Two cross-coupled inverter pairs controlled by four NMOS pass-transistors store the value. NMOS pass-transistors MN3, MN4, MN7 and MN8 are embedded into two cross-coupled inverter pairs to block them during the write phase. To avoid risks and leakage current, the threshold voltages of INV1, INV2, INV4, INV5 are lowered. MN1~MN9 are low threshold voltage NMOS transistors which can reduce the leakage current. A clock generator with clock-gating scheme generates delayed clock signal CLK2, as well as delayed and inverted clock signals CLKB1 and CLKB2. The duration of the write phase depends on the interval between rising edges of CLK and CLK2. Differential signals Data and B1 are applied to a multiplexer to generate a gating signal CTRL. If the input Data is different from the output Q, CTRL will be set to 1 before the rising edge of CLK, therefore CLKB2 follows CLKB1, and CLK2 is a delayed signal of CLK. If the input Data and the output Q are the same, CTRL will be set to 0, thus CLKB2 remains 1 and CLK2 remains 0, redundant transitions of CLKB2 and CLK2 will be eliminated.

The operation of the proposed flip-flop is explained as follows. Assume that output Q and input Data are different before the rising edge of the clock signal CLK, the timing diagram is shown in Fig.2. \( t1 \) is the falling edge of CLKB1, \( t2 \) is the rising edge of CLK2. CLK stays at 0 before the rising edge, the delayed and inverted clock signal CLKB1 stays 1. Data signal gets inverted and passed to B1 and B2. CTRL is set to 1 by the multiplexer, thus CLK2 is set to be inversion of CLKB1, which is 0. Off transistors MN2, MN6, MP1, MP2 isolate the input data from internal nodes. Since MN4 and MN8 are on, two cross-coupled inverter pairs (INV2 with INV3, INV5 with INV6) maintain the stored value. When the rising edge of CLK arrives, B1 and B2 are passed to C1 and C2 respectively by MN2 and MN6, the input data writes into the dual-inverter latches. CLKB1 and CLKB2 turn into 0, therefore MP1 and MP2 are turned on to assist rewriting C1 and C2. Furthermore, MN1, MN5, MN4 and MN8 are switched off, the cross-coupled inverter pairs are cut off during the write phase before the rising edge of CLK2, preventing contention mechanism between pull-up and pull-down branches. The input data signal overwrites the stored value and propagates through the C-element to output Q. CLK2 is then pulled up at \( t2 \) to turn on MN3 and MN7. Since the propagation paths of input data are cut off and the cross-coupled inverter pairs are reformed, the value of Data gets stored in the circuit. After that write phase and
before the next rising clock edge, CLK and CLKB1 will not equal to 1 at the same time, CLKB2 will not be 0 when CLKB1 is 1, therefore the input data paths will keep shut, the value stored in the inverter pairs will not change. If Data does not change, CTRL will be set to 0, therefore CLKB2 will be 1 and CLK2 will be 0. The cross-coupled inverter pairs are never broken. When Data changes, CTRL will switch to 1 at the negative half cycle of CLK, CLKB2 and CLK2 are controlled by CLKB1. Since one of CLKB2 and CLK2 will be set to 1, the cross-coupled inverter pairs will keep the stored value. If output Q and input Data are the same at the rising edge of CLK, the value of internal nodes are refreshed and will keep unchanged, CLKB2 and CLK2 will not make transitions.

It is possible for a high energy particle strike to induce a false transient at one of the internal nodes. In the keep phase, when CLK is 0, CLKB2 will be pulled up, transient faults before node B1 will be masked by turned-off transistors MN2, MN9, MP1 and MP2; In other conditions, unmasked false transients at any node may upset one of the keeper logics. However, any false value caused by single bit upset will be blocked by the C-element, therefore the output node Q stays at correct value, and the latches are refreshed at every clock cycle. Similar nodes are placed as far as possible in the layout to avoid charge sharing. When high energy particle strike occurs in the write phase, if the input data is identical to the output data, the circuit is still robust because the C-element will keep the output unchanged. However, only if the input Data and output Q are different, there will be a chance for the output to be erroneous. But the chance is small as the duration of the write phase is short relative to the clock cycle.

The pulse generator is a combinational circuit lacking regenerative feedback, which means any effect on the pulse generator would be transitory. The pulse generator is sized up to ensure high speed operation, thus it would take a large amount of charge to affect this circuit [33]. When output Q is 1, a false transient at A1 or B1 on the keep phase has a potential to result in erroneous CTRL signal. However, when CLKB1 is 1, it makes no difference for CLKB2 and CLK2 whether CTRL is 0 or 1. When CLKB1 is 0, an erroneous CTRL could only affect the state of CLKB2 and CLK2. But whether CLKB2 is pulled up through MP3 or driven by CLKB2 through MN9, input data paths will be shut, thus no erroneous latching action will occur. The logic keepers will not be cut off whatever because CLKB2 and CLK2 are inverse to each other. Furthermore, CLK will be 0 and CLKB1 will be 1 before the write phase for half a clock cycle, therefore Data will set B1 to correct value. If Q happens to be 1 and Data happens to be 0 and an erroneous CTRL arises right before the write phase, increased delay and contention problem will occur, inducing extra power consumption. But with properly arranged sizes of inverters, the output data would still be correct.

Pulse-triggered designs usually increase the total power dissipation due to redundant switching activities and current contention mechanism occurring between pull-up and pull-down branches [20]. Note that the cross-coupled inverter pairs are cut off in the write phase, hence there is no short-circuit path when rewriting the stored value, any contention between the incoming signal and the internal data is avoided. When input Data keeps unchanged, CLKB2 keeps high and CLK2 keeps low, hence redundant transition in the clock generator is decreased, and the number of transistors controlled by CLK and CLKB1 in the flip-flop is 4. As a result, the power dissipation is reduced.

4. Simulation results and comparison

The layout of the proposed flip-flop has been designed in a commercial 55nm CMOS process as can be seen in Fig. 3, which can be used as standard cell. Post-simulations were performed in Cadence at 1.2v power supply and room temperature (27 °C).

4.1 SEU tolerance

For illustration, a current pulse was injected at internal nodes to emulate false transients induced by particle strikes. The false transients were modeled by a traditional double-exponential function [4], as shown by Eq. (1):

$$I = \frac{Q_{\text{total}}}{\tau_\alpha - \tau_\beta} \left( e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}} \right)$$

where $Q_{\text{total}}$ is the amount of charge deposited by the particle strike, $\tau_\alpha$ is the junction collection time constant, and $\tau_\beta$ is the ion track establishment constant. The deposited charge was set to 100 fC. Injections have been performed at all the internal nodes. When an internal node was affected by false transients, the error was blocked by either the C-element or the transmission gates. The output data of the proposed flip-flop were not affected by false transients. An erroneous CTRL signal does not incur an improper function. The scenarios where the transient faults are injected at node C1 and Qb1 are shown in Fig. 4 as examples. As can be seen in Fig. 4(a), the first false transient current is injected at 10.2ns, where CLK is 0 and the flip-flop is in keep phase. The output Q is high and C1 is low before the injection. The value of C1 is driven to high by the false transient current after 10.2ns. However, the output Q keeps unchanged. When the rising edge of CLK arrives at 10.5ns, C1 is driven by INV4 thus
the value of C1 is refreshed by the input. It takes 190ps to correct the value of C1. The second false transient current is injected at 14.2ns which is 300ps before the write phase. C1 is driven from high to low by the transient current and the output Q stays correct. When the rising edge of CLK arrives at 14.5ns, C1 is rewritten by the input data. The value of C1 recovers after about 190ps. The timing in Fig. 4(b) is the same as Fig. 4(a). Injections were also performed in the keep phase when CLK is 1, and similar results were obtained.

The SEU cross section of the proposed flip-flop was evaluated using the Monte Carlo simulation model reported in [35]. Two 1024-stage shift register chains formed by conventional master-slave D flip-flop and the proposed design respectively were designed at layout level. The operating frequency was 160 MHz. Four typical incident ions with different linear energy transfer (LET) were considered. The SEU cross section was simulated under two different data patterns, the input data were constant “0” for the first pattern and constant “1” for the second. As can be seen in Fig. 5, the proposed design shows higher LET threshold and reduces the SEU cross section by more than an order of magnitude compared with conventional D flip-flop. The single events occurring around the rising edges of the clock signal are considered as the main cause of the upsets for the proposed design.

4.2 Area, power, and delay

Table I. Comparison of Number of transistors, Cell size and timing parameters.

| Flip-flop design | Cell size(μm²) | Clock-to-Q delay (ps) |
|------------------|---------------|----------------------|
| Proposed flip-flop | 22.2 | 58.2 |
| MS-FF | 12.7 | 36.8 |

Table II. Comparison of area, delay and power consumption normalized to the MS-FF for different SEU-tolerant flip-flop designs.

| Flip-flop design | Cell size(μm²) | Clock-to-Q delay (n.u.) | Power(n.u.) | PDP(n.u.) |
|------------------|---------------|------------------------|-------------|----------|
| Proposed flip-flop | 1.75 | 1.58 | 0.67 | 1.06 |
| Pulsed-DICE [13] | 1.33 | 1.01 | 1.05 | 1.06 |
| Pulsed-Quatro [33] | 1.18 | 1.67 | 1.97 | 3.29 |
| MS-DICE FF [24] | 2.95 | 1.40 | 1.80 | 2.52 |
| TSPC-DICE [32] | 1.46 | 1.73 | 1.82 | 3.15 |
| Quatro FF [25] | 2.36 | 0.95 | 2.72 | 2.58 |
| Work in [25] | 2.5 | 1.02 | 2.73 | 2.78 |
| BISER [10] | 2.74 | 1.56 | 2.27 | 3.54 |

The power consumption versus data switching activities is shown in Fig. 6. Table I presents the layout area and speed performance of the flip-flop as compared to conventional master-slave D flip-flop at 1GHz clock frequency. Clock-to-Q delays are represented by the average values of the values for high-to-low and low-to-high transitions. The area and power penalties of the clock generator are both included for comparison. The total area consumption is 74.8% higher than conventional D flip-flop. The average increase in delay is 58.2%. The proposed design shows similar power consumption to conventional D flip-flop at 40% data activity.
When data activity is lower than 25%, which is a general situation, the proposed SEU-tolerant design shows even lower power consumption than the conventional D flip-flop. The performances of some existing designs have been reported in literatures [10, 13, 24, 25, 32, 33]. Data in these literatures have been extracted and normalized to the conventional D flip-flop for comparison. The power consumption in 10% data activity is used since the data activity being less than 20% is common in ICs [33]. Table II compares the normalized cell size, delay, power, and PDP (power-delay product).

As a trade-off, SEU-tolerant flip-flops commonly consume more power than conventional D flip-flop, but the proposed design achieves lowest power consumption with acceptable overheads. The power consumption is even lower than the conventional D flip-flop. The lowest PDP is shown by two PFFs, which is the proposed design and pulsed-DICE latch in [13]. The area overhead of pulsed-DICE latch is 24% less than the proposed design. However, the proposed design shows the same PDP as pulsed-DICE latch, with 36% less power consumption, and the area overhead is acceptable. As a trade-off, the delay is increased, these data indicate that the proposed design is suitable for applications which are power-constrained but insensitive to speed.

4.3 SEU Tolerance Against Process Variation
The effect of process variation is investigated through Monte Carlo simulations. For illustration, the result of 5000 Monte Carlo simulations where 100fC charge is injected at node C1 is shown in Fig. 7. The timing of the SET injection is the same as that of Fig. 4. The functionality and SEU tolerance were not affected by process variation. Similar simulations are carried out at different sensitive nodes to validate the SEU tolerance. The total power consumption and average delay time under process variations is shown in Fig. 8 and Fig. 9. The curves in these figures were obtained by the density estimator of Cadence. As can be seen, the power consumption was robust against PVT variations. However, because CLK2B is driven by NMOS pass transistor, the standard deviation of delay time is relatively high. Increasing the size of the pass transistor MN9 could be a mitigation to that problem, and it is suggested again that the proposed design is more suitable for low-power applications which are insensitive to speed.

6. Conclusion
This paper introduces a low-power dual-modular redundant pulse-triggered flip-flop design with SEU-immunity. It utilizes the concise formation of PFFs to reduce area penalty. The proposed design avoids redundant transitions and cuts off the keeper logics during the write phase to eliminate contention mechanism. Clock-gating scheme is adopted to reduce redundant transitions. Low threshold voltage NMOS transistors are used to reduce leakage current.

The proposed flip-flop has been designed in a 55nm CMOS technology at layout level and can be used as a standard cell. Simulation results showed that the SEU cross section of the proposed design is more than an order of magnitude smaller than unhardened D flip-flop. The design showed superiority in power-efficiency over previous SEU-tolerant designs, even lower power consumption than conventional D flip-flop was achieved at low data activities. The area overhead was acceptable, which was 75% more than conventional D flip-flop. The delay penalty was 58% as a trade-off, but the power-delay product was lowest among hardened designs. Monte-Carlo simulations are also carried out to verify the performance and SEU tolerance under process variations. In conclusion, the proposed design suits power-constrained applications with lower speed restriction.

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