The High-Reliability Optimization of Dead-Time Circuit for Push-Pull DC-DC Converter

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Abstract. Aiming at the problem of common conduction state in push-pull DC-DC converter's power transistor, an optimization solution by improving pulse width modulation (PWM) mode and reasonable setting parameters of the transformer and the inductance was proposed. The solution was analyzed in detail and test of the optimized circuit are carried out. The results show that the optimized circuit can effectively eliminate common conduction state, make the converter have a suitable dead-time and greatly improve the reliability of the converter.

Keywords: Power transistor; Common conduction state; PWM.

1. Introduction
The push-pull DC/DC converter is widely used in conversion from DC low voltage to DC high voltage due to its high-frequency transformer with high utilization, high output power and simple drive circuit [1]. It is mainly composed of push-pull inverter and output rectifier filter circuit. The two power tubes in the push-pull inverter operate in alternating conduction state, it is necessary to prevent the two tubes from conducting simultaneously when designing.

In the control cycle of a pulse width modulation, under normal conditions, the working state of two power switches: transistors or metal-oxide-semiconductor field-effect tubes ("MOS tube" for short) are in alternating conduction or simultaneous cutoff. When two power switch transistors or MOS tubes are simultaneously conducting at a certain moment or time within a cycle; this state is called a "common conduction state". The occurrence of this state causes two primary coils of transformer to directly produce a short circuit, which is equivalent to two leads, so that the input end and output ground of DC voltage are directly connected between the power switch transistor collector and emitter, or between MOS tube drain and source, collector or drain current increases sharply, the switch tube is vulnerable to excessive current stress and breakdown burnout, the occurrence of "common conduction state" should be avoided in the design [2-4]. In this paper, the circuit with common conduction is designed and improved.

2. Principle of Push-Pull Converter
The push-pull converter consists of PWM pulse width modulation circuit, power amplifier circuit, rectifier filter, sampling feedback circuit and voltage-stabilizing circuit, which adopts the circuit structure of two coils working in turn on the primary side of the transformer, namely two power switching transistors or MOS tubes are driven by two signals with adjustable pulse width and 180° phase
difference, thus alternately conducting, converting DC voltage to AC voltage and then outputting it to the secondary coil of the transformer through the transformer, the energy outputs the driving load after rectified and filtered, as shown in Fig. 1. There is a certain time interval from the cutoff of MOS tube V1 to the coming of PWM2 pulse making the MOS tube V2 conduction, namely the dead zone. During this period, the two tubes are cut off, the drain voltage of the tubes are power input $V_{in}$.

![Fig. 1 principle of push-pull DC/DC converter](image1)

**3. Optimized Design**

**3.1. Optimization of pulse width modulation way**

The major role of pulse width modulation (PWM) is to adjust the duty cycle of PWM pulse in accordance with the output voltage feedback, and further drive the power device to make the output DC voltage stable and reliable.

In fact, the adopted pulse width modulation method produced two-way PWM pulse with common conduction state, the circuit diagram is shown in Fig.2. The PWM1 and PWM2 with the common conduction state are directly input to the MOS tubes V1 and V2, and their control timing is shown in Fig.3, and the measured waveform is shown in Fig.4.

![Fig. 2 circuit diagram before improvement](image2)

![Fig. 3 timing diagram of PWM pulse with common conduction state](image3)
In allusion to above situation, the phase inversion is carried out on the PWM pulses from the pulse width modulator, which will enter the gates of two MOS tubes, the reverse-phase circuits composed of transistors and peripheral circuits are added behind the PWM1 and PWM2 respectively, which make the two-way PWM pulse with commom conduction state invert the phase to come into being the dead zones between the gate of the MOS tube V1 and the gate of the MOS tube V2, so that the two-way PWM wave entering the V1 and V2 grid have dead zones, as shown in Fig.5.

When PWM1 output is low level, the base current of transistor Q1 is zero, the voltage between the base and emitter is zero, and the transistor is in the cutoff state. And the DC input power supply 28V charges MOS tube V1 through the resistor R1, which gate is high. At the same time, PWM2 output is high level, the gate of MOS tube V2 is low.

When PWM1 outputs high level, the collector and emitter of transistor Q1 breakover, the tube is in the deep saturation, and the gate of MOS tube V1 is low. At the same time, PWM2 outputs low level, and the gate of MOS tube V2 is high.

The two-way PWM waveform with common conduction state is reverted through reverse-phase to form the timing as shown in Fig.6, so that the waveform entering the MOS tube gate has the dead zone.
3.2. Optimization of transformer and filter inductance

The DC input voltage provides primary load current and primary excitation current in the MOS tube’s conduction stage of push-pull circuit. When the conducting MOS tube is cut off, the output filter inductance current cannot change suddenly, the polarity is reverted, when its front-end electric potential is one diode conduction voltage drop lower than the ground or a diode voltage drop higher than the negative output voltage, the rectifier diode is conducted, plays the role of follow current and flows through the output inductance current. The current flowing through the rectifier diode is not just the output inductance current. Due to the fly back effect, the exciting current built in the primary of the transformer during the conduction is converted to half of the secondary without flowing current based on the turn ratio. During the dead zone time, it is the current flowing through this semi secondary that keeps the magnetic density of the transformer magnetic core [5].

To sum up, when one MOS tube is turned off and another MOS tube is cut-off state, part of the total exciting current of the transformer is converted to a secondary based on the turn ratio, and the follow current continues in this secondary. At this point, rectifier diodes in all secondaries follow current and bear about half of the corresponding filter inductance current, rectifier diodes in one of the secondaries bears a part of the converted primary exciting current.

As shown in Fig.5, when the MOS tube V1 is conducted, the anode of the rectifier diode V5 is positive, and V5 transmits current to the load via the filter inductance L1. When MOS tube V1 is cut off, the dead zone begins, the current of L1 is divided equally in the rectifier diode V3 and V5, the role of V3 and V5 is equivalent to the freewheel diode. As long as the sum of the current flowing through V3 and V5 is equal to the current flowing through L1, its cathode will be clamped the voltage which is one diode voltage drop below the ground.

However, when V1 is cut off, due to the fly back effect, the part of the excitation current is transferred to the secondary 4-5 and flows through L1 via V3. If the excitation current of transformer is greater than the L1 current, then the V3 and V5 cathode voltages increase to higher than the ground potential in the dead zone. When the inductance quantity of the filter inductor is too large or the current which DC output is too low, the cathode voltage of V3 and V5 will also increase to higher than the ground potential in the dead zone. The increase of this voltage causes the increase of secondary volt-seconds.

When V1 is conducted, the other end of the transformer primary 1-2 is positive, and the magnetic core rise along the hysteresis loop, namely moves from B1 to B2. The actual value of the rise is proportional to the voltage of primary 1-2 and V1 conduction time. When V1 is cut off and V2 is conducted, the namesake in the primary 2-3 is positive, and the magnetic core drops from B2 to B1 along the hysteresis loop, as shown in Fig.7.

![Hysteresis Loop](image)

Fig. 7 hysteresis loop

When V1 is conducted, if the number of volt-seconds applied to the primary 1-2 is equal to the number of volt-seconds applied to the primary 2-3 when V2 is conducted, the magnetic core will rise from B1 to B2 in one cycle, and then return to B1 again. When the number of secondary volt-seconds increases, correspondly the number of primary volt-seconds increases. As the voltage of the primary 1-2 cannot be changed, the conduction time of V1 will increase. When the number of volt-seconds
increases, the dead zone of V1 will disappear. Therefore, the reasonable setting of the transformer and filter inductance parameters can make the MOS tube have the dead zone.

3.3. Transformer design
The quality of the transformer design directly affects the efficiency, temperature rise, output electrical performance parameters, life and reliability of the entire power supply.

The design steps of transformer are as follows:

(1) The selection of magnetic core. When selecting the magnetic core of transformer, its volume must meet the output power requirements, which is mainly determined by the operating frequency, magnetic flux density amplitude, magnetic core area, framework window area, and current density of each coil. These parameters are related to each other. It should be to try to reduce the size of the transformer to reduce the temperature rise in selection.

(2) The number of turns of the primary coil is determined. According to Faraday law of electromagnetic sensibility, the induced electromotive force of the transformer primary coil is:

$$E_{rms} = 4NfB_{pk}A_e$$  \hspace{1cm} (1)

In the formula: $N$ is the number of turns of the coil; $f$ is the frequency; $B_{pk}$ is the peak of magnetic flux density; $A_e$ is the effective magnetic circuit area.

By converting the formula (1), it can be obtained that the number of turns of the transformer primary coil is:

$$N_P = \frac{E_{rms}}{4fB_{pk}A_e}$$  \hspace{1cm} (2)

(3) The number of turns of the secondary coil is determined. According to the principle when the primary and secondary volt-seconds are consistent, the number of turns $N_S$ of the secondary coil can be obtained by $V_i/V_o = N_P/N_S$:

$$N_S = \frac{V_o \times N_P}{V_{in}}$$ \hspace{1cm} (3)

In the formula: $V_i$ is the DC input voltage; $V_o$ is the output voltage.

(4) The wire size is determined. Whether the primary coil or the secondary coil, the wire size is determined by the coil current. The primary winding current $I_P$ is:

$$I_P = \frac{P_o}{V_{in} \eta}$$ \hspace{1cm} (4)

In the formula: $P_o$ is the output power; $\eta$ is the power efficiency. The bare wire area $A_{wp}$ of the wire can be obtained from the primary coil current $I_P$ and current density $J$:

$$A_{wp} = \frac{I_P \times 0.707}{J}$$ \hspace{1cm} (5)

The wire specification can be determined by table look-up via the bare wire area $A_{wp}$ [6].

(5) Coil layout
The most important factor to be considered in transformer design is the temperature rise. The temperature rise of the transformer relies on the magnetic core loss (namely iron loss) and the coil loss (namely copper loss).

In order to further reduce the heat loss in the design improvement, the primary and secondary cross winding structure is adopted in the transformer winding, namely, the first layer is the primary, the middle layer is the secondary, and the last layer is the primary.

3.4. Inductance design
In the optimized design, the inductance magnetic core is reselected and the parameters are re-optimized. In order to ensure that the inductance can work continuously, it needs to meet:
\[
\frac{(V_i-V_o) T_{on}}{L_o} = 2I_{dc} \quad (6)
\]

In the formula: \( V_i \) is the input voltage of filter inductance; \( V_o \) is the output voltage of filter inductance; \( T_{on} \) is the MOS tube conduction time in one cycle; \( I_{dc} \) is the minimum output current. Plugging \( V_o = V_i \left( \frac{2 T_{on}}{T} \right) \) and \( T_{on} = D \times T \) (\( D \) is the PWM wave duty cycle) into formula (6):

\[
L_o = \frac{(2.5(1-2D)V_o T)}{I_{on}} \quad (7)
\]

\( D \) takes \( 0.4 \sim 0.45 \), then \( L_o \) is \( 0.95 \sim 1.9 \) mH.

4. Tests and Verification

The actual product is optimized and tested via theoretical analysis, the gate source voltage \( U_{GS} \) and drain source voltage \( U_{DS} \) waveform of MOS tubes \( V1 \) and \( V2 \) are recorded when the power supply input is 28V.

Fig.8 shows the voltage waveforms when PWM1 and PWM2 waveforms enter into the base of transistors \( Q1 \) and \( Q2 \), there is about 1.3 \( \mu s \) to 1.4 \( \mu s \) common conduction time between the base and emitter voltage waveforms of the two tubes.

![Fig. 8 transistor input waveform after optimized design](image)

(1) Transistor base and emitter waveform 1

(2) Transistor base and emitter waveform 2

Fig. 9 is the gate source voltage waveforms when PWM1 and PWM2 separately enter into MOS tube \( V1 \) (yellow waveform) and \( V2 \) (blue waveform) after going through the inversion circuit. Fig. 9(1) is the \( U_{GS} \) waveform when \( V1 \) tube is cut off and \( V2 \) tube is not conducted, Fig. 9(2) is the \( U_{GS} \) waveform when \( V2 \) tube is cut off and \( V1 \) tube is not conducted. It can be seen from the figure that there is about 0.8 \( \mu s \) dead zone time in the two \( U_{GS} \) waveforms.
Fig. 9 input waveform of MOS tube after optimized design

Fig. 10 is the drain source voltage waveforms of MOS tubes V1 and V2, Fig. 10 (1) is the UDS waveform when V1 tube is cut off and V2 tube is not conducted, Fig. 10(2) is the UDS waveform when V2 tube is cut off and V1 is not conducted. It can be seen from the figure that there is about 1.68 μs to 1.8 μs dead zone time in two tubes U_{DS} waveforms.

Fig. 10 output waveform of MOS tube after optimized design
5. Conclusion

In allusion to the circuit with common conduction state, the design is improved from changing the aspects of pulse width modulation and reasonably setting the transformer and inductance, so as to eliminate the common conduction state of MOS tubes, and its input waveform and output waveform have dead zone, which effectively improves the reliability of the push-pull circuit and realizes the stability of the product.

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