Scaling silicon-based quantum computing using CMOS technology

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As quantum processors grow in complexity, attention is moving to the scaling prospects of the entire quantum computing system, including the classical support hardware. Recent results in high-fidelity control of individual spins in silicon combined with demonstrations that these qubits can be manufactured in a similar fashion to field-effect transistors, create an opportunity to leverage the know-how of the complementary metal-oxide-semiconductor (CMOS) industry to address the scaling challenge at a system level. Here, we review the prospects of scaling silicon-based quantum computing using CMOS technology. We consider the concept of a quantum computing system, which we decompose into three distinct layers — the quantum layer, the quantum—classical interface and the classical layer — and explore the challenges involved in their development, as well their assembly into an architecture. Silicon offers the enticing possibility that all layers can, in principle, be manufactured using CMOS technology, creating an opportunity to move from distributed quantum-classical systems to integrated quantum computing solutions.

Quantum computers have demonstrated computational advantage [1, 2]. As the technology continues to develop, scaling quantum computing systems as a whole becomes increasingly important and will be essential to building a machine with sufficient error-free computing resources to run quantum algorithms that can solve problems of societal value. Fault-tolerant quantum computing requires resilience against errors. Topological quantum computing models based on non-Abelian anyons — such as Majorana zero modes — offer protection at the qubit level [3, 4]. However, the most technologically promising routes to fault-tolerant quantum computing are based on the standard quantum computing paradigms that use noisy qubits in combination with quantum error correction (QEC) [5, 6]. In this scheme, topological protection is achieved by distributing the logical information over a number of physical qubits, as long as each satisfy a maximum error rate in the combined initialization, manipulation and readout. The most forgiving QEC method, the surface code, sets a 1% upper bound [7]. The exact physical qubit overhead (per logical qubit) depends strongly on the error rate but considering state-of-the-art qubit fidelities, it will likely be a figure in excess of a thousand. QEC is then expected to take the number of required physical qubits to many thousands and possibly millions for economically significant algorithms [9, 10] and to many millions or billions for some of the more demanding quantum computing applications such as Shor’s factorization algorithm [11]. Large-scale integration is hence a requirement to implement QEC schemes and a technological challenge for the most advanced quantum computing platforms relying on superconductors, semiconductors, ion traps or photonic circuits as the physical hosts for the qubits [12, 15].

Developments in the field of nanodevice engineering have shown that qubits can be manufactured in a similar fashion to field-effect transistors (FET) [18–20], creating an opportunity to leverage the integration capabilities of the semiconductor industry to address the up-scaling challenge. Silicon-based quantum computing offers a number of key technological advantages favouring large-scale integration: (i) A small qubit footprint, of the order of $100 \times 100 \text{nm}^2$, and potentially commensurate I/O electronics [21]; and (ii) compatibility with established very large-scale integration (VLSI) techniques of the CMOS industry that routinely manufacture billions of quasi-identical transistors on the size of a fingertip. These ingredients could allow compact fault-tolerant quantum processors that can fit in conventional cryostats without requiring the technically challenging development of new large-scale infrastructures [22]. Furthermore, a quantum processing unit (QPU) will likely be a sub-module of a larger information processing system that also contains analog and digital electronics. In such a scenario, CMOS could enable hybrid integration of quantum and classical technologies, facilitating data management and fast information feedback between them. And, even before a fault-tolerant quantum computer is built, compact CMOS manufacturing could deliver multi-core NISQ QPUs [23], ideal for hybrid quantum-classical algorithms that benefit from massive parallelisation [21, 25].

In addition to the technological benefits, silicon offers favourable physical properties that allow qubits with long...
coherence times to be created. The qubits are encoded by localized spins at deep cryogenic temperatures and finite magnetic fields. The simplest example is the spin $\frac{1}{2}$ of a single electron (or hole) electrostatically confined in a quantum dot (QD) \[^{26}\]. Alternatively, the nuclear spin of individual dopants can be used \[^{27}\]. Quantum dots can now be manufactured on demand in a silicon metal-oxide-semiconductor (MOS) nanodevice (typically Metal-SiO$_2$-Si) \[^{28}\] or in a Si/SiGe heterostructure \[^{16}\] (Fig. 1). Recently, large enhancements in spin coherence have been achieved by isotopic enrichment of the silicon lattice. The 5% naturally occurring spin-carrying isotope, $^{28}$Si, is the major source of decoherence in silicon, whereas the dominant $^{29}$Si isotope has zero nuclear spin. By enriching to nearly pure $^{28}$Si, with only 800 ppm of $^{29}$Si remaining, inhomogeneous spin-dephasing times ($T_2^*$) and spin-coherence times ($T_2$) exceeding 100 $\mu$s and 20 ms, respectively, have been measured for electron spins, placing silicon as one of the most coherent solid-state systems in nature \[^{28}\]. For optimal performance, silicon qubits are cooled down to a few tens of millikelvin under magnetic fields of the order of 1 T but these parameters may be relaxed in the future to allow operation above 1 K \[^{29, 30}\] and at just 150 mT \[^{31}\].

Silicon spin qubits are initialized and readout using spin-to-charge conversion techniques \[^{32–36}\], they are coherently manipulated via magnetically- or electrically-driven electron-spin-resonance for single-qubit operations \[^{16, 37–39}\] and spin-exchange-based methods for two-qubit logic \[^{39}\]. Thanks to the increase in coherence, advancements in high-frequency readout techniques, and optimized spin projection mechanisms, all these steps have now been performed with fidelities above the requirements of the surface code. More particularly, a gate set at the surface code error threshold has been recently demonstrated on a two-qubit device \[^{40, 41}\]. These are promising initial results for this relatively recent approach to quantum computing, and indicate that building a fault-tolerant quantum computer based on silicon technology is a realistic proposition. However, several technological challenges lie ahead. So far, most advances have been achieved with small-scale devices (one-, two- and recently six-qubit systems) fabricated in academic cleanrooms, offering relatively modest level of process control and reproducibility \[^{17, 42–44}\]. From this point onwards, a route to increase fidelities well beyond fault-tolerant thresholds in a reproducible way across large arrays of qubits needs to be established. Recent results on qubits fabricated in industrial settings \[^{18–20}\] may shed some light on how to achieve this goal, see Fig. 1-e-h.

In this Review, we explore the scaling prospects of quantum computing systems based on CMOS technology. We first consider the concept of a quantum computing system and its different elements. We then examine the challenges at the quantum layer and the challenges involved when designing classical CMOS circuits at cryogenic temperatures, which affect both the quantum–classical interface and the classical layer. Finally, we consider the functional assembly of the layers into a system architecture.

**A QUANTUM COMPUTING SYSTEM**

The problem of scaling requires a shift in the thinking process beyond the few-qubit quantum processor proof-of-principle demonstrations to a full stack perspective: that is, a quantum computing system (QCS) \[^{45}\]. Researchers have already started to tackle this problem, producing blueprints of what a large-scale quantum computer could look like in silicon \[^{21, 46–48}\]. These proposals share a common basic idea. In particular, the future silicon QCS should be composed of three distinct layers – the quantum layer or quantum processing unit (QPU), the quantum-classical interface and the classical layer – all of which could potentially be manufactured using CMOS technology, at least to a certain extent (Fig 2-a, b).

The configuration of the quantum layer is primarily dictated by the physical requirements of the surface code (Fig 3): a two-dimensional distribution of physical qubits with nearest-neighbour interactions \[^{8}\]. The qubits are split into data qubits (qubits in which the computational quantum states are stored) and measurement qubits (qubits performing error detection). Measurement qubits come in two types: X and Z syndrome qubits, which contribute to the measurement of bit-flip and phase-flip errors, respectively. Each X-type and Z-type qubit is made to interact in an anticlockwise sequence with the four adjacent data qubits and then measured to extract information of the system (stabilizer). The stabilizers can be measured repeatedly without perturbing the quantum state of the system. However, once one or more errors occur, the outcome of a stabilizer measurement changes. By correlating stabilizer outputs, the location of an error can be identified and then corrected. In silicon, the surface code could be implemented in a $^{28}$Si substrate, by distributing, in a square array, individually-addressable nanometre-scale MOS structures to form few-electron QDs, plus additional gates in between to control, locally, the exchange interaction between spins. Given the projective nature of spin readout, the surface code could be implemented in a $2 \times 3$ QD sublattice, using planar designs \[^{21}\], or in a canonical $2 \times 2$ sublattice, although this would involve using 3D integrated structures (Fig 3-b) \[^{49}\].

The quantum-classical interface will handle the control and readout of the individual qubits, as well as the routing and input/output data management of the large number of signals required to operate the QPU \[^{50}\]. This layer contains signal generators, (de)modulators, analog-to-digital (ADCs) and digital-to-analog converters (DACs), amplifiers for control and readout and (de)multiplexing for I/O management (Fig 2-b).

The classical layer is designed to assist in the QEC process by taking the outputs of the QPU via the quantum-classical interface and correlating them, in classical logic,
with a concrete error type, location and time step. Errors can be generally corrected in software but in order to enable universal quantum computation, including non-Clifford operations, fast feedback between readout and control would be necessary. Furthermore, the classical layer is expected to compile the quantum algorithms into a sequence of interleaved control and readout steps of the relevant qubits. This layer contains a processing unit (field-programmable gate array (FPGA); or application-specific integrated circuit (ASIC)) that, within the cooling power constraints of cryogenic systems, should be placed in close proximity to the rest of the layers to reduce latency in feedback operations.

The physical architecture of the QCS is still a matter of debate. In fact, it is likely that a number of approaches could be followed. The flexibility in the physical arrangements of the layers and the square-grid distribution of the QDs in the QPU evoke image sensors as an example of the foreseeable future for CMOS-based quantum computing (Fig 3). Charge coupled devices (CCDs) or CMOS image sensors, competing image technologies, both fulfill their image recording purposes but with a different set of specifications given their different levels of integration [51]. In both technologies, the physical layout is constituted by a two-dimensional array of unit cells (pixels). In the case of CCD, charge-to-voltage conversion occurs via shifting charges sequentially to a global amplifier sitting at the periphery. However, in the case of CMOS sensors, such as active-pixel sensors, readout occurs in a distributed manner with a first stage of amplification at the pixel level, followed by column and global amplification at the periphery (Fig 3). The different architectures result in a different set of technical specifications that can be tailored to the specific application. CMOS-based quantum computing could follow a similar path of development in which some architectures could have either local or global electronics for control and readout. Global techniques are likely to simplify the integration process and deliver architectures sooner, while local integration will provide enhanced functionality. We note that although the analogy works in first order approximation, qubits present radical differences to pixels. Qubits have comparably smaller footprints than photodiodes and qubit-to-qubit interactions need to be managed. These differences impose restrictions for local electronics that will require technological innovation beyond state-of-the-art image sensors.

### CHALLENGES AT THE QUANTUM LAYER

There is flexibility in the path ahead as the optimal qubit cell is still to be defined (Fig 3). However, the abstract description of a quantum machine presented above has some clear consequences on the required conditions to build a QCS. We thus highlight areas where silicon quantum information processing could benefit from the know-how of the CMOS industry starting with the QPU.

**Qubit arrays**

The first challenge involves the use of commercial-scale CMOS manufacturing lines to enable the fabrication of dense two-dimensional arrays of individually addressable gate-defined QDs with gate-controlled tunnel barriers. The unit cell of the qubit is likely to contain additional commensurable electronics either in-plane or in a 3D geometry. Here, we exclusively concentrate on the QD array. The characteristic footprint of the gate electrodes that have been used to defined few-electron QDs in CMOS platforms has been of the order of 40 x 40 nm (width and length) with a gate pitch of 70 nm [18, 52–54], although these dimensions may differ depending on the exact gate stack. The dimensions are in line with the 22 nm CMOS node and are not likely to pose a critical problem. However, the routing of the individual lines is a challenge. To allow 2D geometries, ideally, the gate interconnect should be placed directly above the location of the QDs, a feature that is yet not possible in modern technology nodes. In addition, the necessity to have a tightly packed exchange gate in between adjacent QD gates to control the interaction between spins, presents a challenge. Currently, there is no standard CMOS technology node that could deliver the required exchange gate layout. Research efforts are being devoted to developing multi-gate-layer processes in CMOS foundries that will enable configuring exchange gates. So far, two technological paths have been pursued to introduce the exchange gates: (i) three levels of overlapping gates [59, 55] and (ii) self-aligned barrier gates [19, 50].

Currently, modules containing linear and bilinear arrays of QDs are being explored [51, 57–60] in which NISQ algorithms [23] or logical qubits could be implemented. This modular approach could help to tackle the scaling problem in successive approximations, first by producing 1D arrays, then by combining them in 2D arrays with sparse connectivity. This concept would leave space between modules that could then be used to alleviate some of the problems associated with the gate contact routing and the location of the control and readout electronics. The idea could help to develop compact qubit unit cells with embedded electronics to finally produce a fully-connected 2D architecture. The options to build up complexity by coupling individual modules are varied. A possibility could be to directly connect linear or bilinear arrays of qubits at square junctions where couplings between x- and y-oriented arrays could be engineered. As we shall see later, it has also been suggested that medium range solutions like QD couplers [62] and floating gates [60] or long range coherent links such as photon-mediated interactions between spins [63] or even physical transfer of spins using shuttling [64] could be used to couple coherently distant modules.
High-fidelity control

When using electrons as the spin carrying particle, silicon-based spin qubits coming from research laboratories have so far reached single-qubit fidelities exceeding 99.9% in 200 ns [65], and two-qubit fidelities of 98% in 5 µs [17] and recently over 99% [10, 11]. While there is room for improvement, the objective is to achieve gate-set fidelities well above 99% across a large array of qubits on timescales of the order of a microsecond or less to enable fast QEC protocols and minimise computation time.

Single-qubit rotations are typically achieved with electron spin resonance (ESR) techniques that require the delivery of pulsed oscillatory magnetic or electric fields (as in the case of electric dipole spin resonance (EDSR)), in the 5 to 40 GHz range. Electron spin resonance requires either the fabrication of on-chip antennas [66] to provide localized control of groups of qubits (Fig. 1), or the placement of the chip within a uniform oscillatory magnetic field, such as that produced by a resonant microwave cavity to enable control of the entire qubit array [27]. The resonant microwave signal can be pulsed to drive single spin rotations in-phase (X rotations) or in quadrature (Y rotations) [38]. Alternatively, a continuous wave signal can be applied and qubits can be tuned in and out of resonance making use of the Stark shift using local pulses at the qubit gate [67]. Stark shift can also be used to realise Z rotations by exploiting the electrical tunability of the g-factor [20]. X and Y rotation rates in experiments to date on electron spins have been limited to a few MHz due to the heat associated with producing B-field pulses with sufficient amplitude at the qubit location.

While on-chip microwave transmission line antennas have been successfully used for ESR control of few-qubit systems [17, 28, 39], the approach does not scale well as the number of antennas would grow with the number of qubits, posing complex microwave challenges and subjecting the processor to heat generated by the microwave currents passing through the transmission lines. One solution is to use a global AC magnetic field [27]. The most obvious candidate for such a global ESR field is to use a conventional 3D microwave cavity. However, the metal gates, interconnects and bond wires adversely affect the quality factors of such resonators [68], while the quantum processor chip is subject to alternating electric fields, generating induced currents that could interfere with the operation of the QPU and the control and read-out electronics. In recent experiments, however, a new type of compact dielectric resonator, constructed from potassium tantalate (KTaO3), has been used to demonstrate ESR of single electron spins in a SiMOS QD device [69] and coherent control [70]. The KTaO3 is a quantum paraelectric material that has a high dielectric constant at cryogenic temperatures which serves to concentrate the AC magnetic field it generates into a compact microwave mode volume. This enables large, and uniform, AC magnetic fields to be delivered to the qubit plane, while minimising the external microwave power that needs to be delivered to the resonator.

In contrast with ESR control, EDSR induces spin rotations by making use of spin-orbit coupling that converts oscillatory electric fields into oscillatory magnetic fields in the reference frame of the electron [37, 71]. Typically, micro-magnets are necessary to generate intense magnetic field gradients that translate into synthetic spin-orbit coupling with sufficient strength to drive coherent spin rotations. Using Co micro-magnets in split geometries in a plane above the qubit layer (Fig. 1), rates up to tens of MHz have been reached [65]. However, the increased spin-orbit coupling created by the micro-magnet field gradient also makes the qubit susceptible to electrical noise, which can limit $T_2$ [65, 72] and may substantially reduce the relaxation time, $T_1$ [73]. So far the split magnet geometry has been appropriate to control and independently address one-dimensional arrays of qubits [14, 74]. For two-dimensional arrays, the micro-magnet geometry will need to be redesigned to provide a suitable magnetic field gradient and addressability across the array, for example, by miniaturization to nanometric structures and by placing multiple magnets in grids [73]. The impact of these new geometries on the strength of the magnetic field gradients will need to be studied and, if insufficient, new materials with higher remanence will need to be explored.

On the other hand, intrinsic spin-orbit coupling, of which there is enhanced evidence in low symmetry QDs [52], or in holes rather than electrons [76], may facilitate scaling since manipulation will not require additional elements in the qubit cell. In fact, very promising recent results have shown that finFET-based single hole spin qubits can be controlled close to the fault-tolerant threshold at 1.5 K, thanks to the fast spin-orbit-driven spin rotations (147 MHz) and the weak hyperfine coupling leading to $T_2^* = 440$ ns [20, 77].

Two-qubit gates are based on the exchange interaction between neighbouring spins. The exchange strength $(J)$, which depends on the wavefunction overlap between participating spin particles, can be varied by changing the voltage detuning between QDs (asymmetric tuning) [39] or by tuning the potential barrier between QDs (symmetric tuning) [78, 81]. Symmetric tuning is less sensitive to charge noise allowing exchange coupling operations at a sweet spot where the $J$ has zero derivative with respect to voltage detuning. The short-range nature of the exchange interaction and the preference for symmetric tuning, impose the tightest restriction on the gate layout as explained above: a QD gate pitch of the order of 70 nm and an exchange gate in the space between of adequate footprint to tune the exchange interaction by several orders of magnitude between the ON and OFF states (when $J/h$ should be much smaller than the single- and two-qubit gate speeds).

Two-qubit gates can be performed in two distinct ways, either via exchange modulation or resonantly. Exchange modulation involves pulsing the exchange interaction.
Depending on the pulse scheme, a CPhase \cite{39} or a √SWAP gate \cite{34, 81} can be implemented. In the latter case, a subnanosecond two-qubit gate has been demonstrated for P-donor spins in silicon \cite{81}, emphasizing the speed advantages of gate-voltage pulses over resonant two-qubit gate schemes. Resonant two-qubit gates involve turning on the exchange interaction and performing ESR/EDSR on the coupled two-spin system to perform a CROT gate \cite{17, 42}. CPhase gates set the benchmark for two-qubit gate fidelity: 99.5% in 100 ns \cite{40}.

Besides two-qubit gates driven by direct exchange interaction, other proposals suggest incorporating larger multi-electron QDs that could extend the spin-spin interactions beyond nearest neighbours \cite{29}. These QD mediators have been demonstrated to extend the spin interaction in an electrically-controlled manner over 800 nm in GaAs \cite{62}, and could free up space in between qubits for gate routing while maintaining the full 2D connectivity. However, mediator QD level spacing must be larger than the energy of the thermal fluctuations and the excitation spectrum of the control voltage pulses \cite{82}. Given the smaller effective mass of silicon compared to GaAs and the dependence of the level spacing on the size of the dot, this will reduce the range over which fast spin interactions could be driven in silicon by approximately a factor of 3. An experimental proof of mediator dots in silicon remains to be demonstrated. Another proposal that could extend the range of qubit interactions over intermediate distances is that of floating gates \cite{83}. However, due to its electrostatic nature, it would be most effective in qubits implemented in the magnetic number subspace \( m_s = 0 \) of two-particle singlet-triplet qubits \cite{84}, whose charge density is strongly dependent on the total spin number.

Going beyond one and two-qubit interactions, control at scale requires careful management of crosstalk between closely spaced qubits. Research should be directed towards assessing how manipulating target qubits impacts idling qubits (or even simultaneously addressed qubits) and determine compensation signals to minimise this crosstalk. Benchmarking of the optimal gate-set in terms of fidelity, operation timescales and impact on idling qubits must be undertaken.

**High-fidelity readout**

To implement fast feedback in active error correction protocols, high-fidelity readout must be performed in timescales significantly shorter than the spin coherence time \cite{85}. Ideally, this timescale should be shorter than the duration of single- and two-qubit gates to avoid becoming the bottleneck in QEC. The latter requires achieving readout fidelities well above 99% in a few microseconds or less. Readout of spins in silicon is achieved via spin-dependent tunnelling processes such as Elzerman readout \cite{82} or Pauli spin blockade \cite{80}, where spins tunnel selectively to a charge reservoir or to a spin polarized QD, respectively. Tunnelling under these conditions translates the spin information to a charge-based signal that can be read using sensitive electrometres.

The most commonly used are three-terminal charge sensors such as the single-electron transistor (SET) \cite{87}, where a current flowing through the device is strongly dependent on the local charge environment. The SET can be used to detect single-electron tunnelling events in the time domain but its bandwidth is limited to a few tens of kilohertz by RC parasitics at its output port. The bandwidth can be extended to hundreds of kilohertz using amplifiers in close proximity \cite{88} or even to tens of megahertz when using high-frequency LC impedance matching techniques, i.e. the rf-SET \cite{89, 90}. With these two approaches, readout fidelities of 99.9% in 6 µs \cite{91}, and 99% in 1.6 µs \cite{92} have been achieved, respectively. These electrometres need to be placed in close proximity to the qubits and require two charge reservoirs to function complicating the use of this method at scale in dense qubit arrays.

More compact approaches are currently being developed. A two-terminal charge sensor, the rf single-electron box (SEB) \cite{93, 94}, uses dispersive readout techniques to detect the variable capacitance of a QD. Changes in the surrounding charge environment modify the bias point of the SEB, which in turn produce a rf response conditional to the charge state of the sensed element. Although its demonstrated fidelity is still limited (99% in 1 ms \cite{95}), it may prove a valuable technique for upscaling. An even more compact method, \textit{in-situ} dispersive readout (IDR), simplifies the architecture by removing the charge sensor and charge reservoirs altogether and directly embedding the qubit in a radio- or microwave frequency electrical resonator \cite{76, 96-102}. The state of the qubit, which in effect is a state-dependent capacitor \cite{103}, can be directly inferred from the oscillatory state of the resonator. With this methodology a readout fidelity of 98% in 6 µs has been obtained \cite{104}.

High-frequency techniques bring the benefit of simultaneous readout via frequency-domain multiple access (FDMA) \cite{105}. Additionally, time-division multiple access (TDMA) techniques could reduce the total number of resonators by performing qubit readout in a sequential manner using a common resonator \cite{106}. Furthermore, dispersive readout techniques, either rf-SET and IDR, not being limited by shot-noise, can be used in conjunction with quantum-limited Josephson parameter amplification to speed up the readout \cite{107}.

In the case of high-frequency techniques, the footprint of the resonator (or inductor in lumped-element configurations) poses a significant challenge in terms of scaling with typical values in excess of 100 × 100 µm \cite{104}. To solve this challenge, high inductance density materials will be necessary. Josephson metamaterials, formed by arrays of Josephson junctions, present one of the highest inductance per unit length and may be a compact solution \cite{108} but their integration within a CMOS process appears to be complex. High kinetic inductance materi-
Stacks with minimized trapped charge densities below affect the static and dynamic properties of the qubits. Development remains critical since charged defects can affect the thermal budget to cope with the self-diffusion between narrow strips a few micrometers long. Granular aluminium with $L_K = 2 \text{nH/sq}$ could be an even more compact alternative \[113, 114\].

If SET readout is to be pursued, research efforts should be directed at increasing the bandwidth even further by directly integrating low-power low-noise amplifiers on chip with minimal footprint capable of addressing several SETs via multiplexing techniques. The community should also think of ways to go beyond charge sensors and IDR by adapting concepts from classical electronics to resolve the fF-scale capacitance associated with quantum tunnelling between adjacent QDs \[115, 116\]. A compact solution that could be integrated on-chip with a footprint commensurable to the qubit size will facilitate the massively parallel readout required for QEC codes.

Qubit variability

One of the greatest challenges is the necessity to manufacture high-fidelity qubits at scale. Although VLSI technology guarantees a high level of reproducibility, variability acquires a much higher degree of importance in the quantum realm, since quantum device performance varies significantly with parameters like the tunnel coupling or the valley-splitting, both of which can be affected by a single atomic defect \[117, 119\]. Special emphasis should be put on the quality of the interfaces and on the purity and crystallinity of the materials.

From a channel material perspective, the development of isotopically enriched Si or Si/Ge stacks will be necessary to provide nuclear spin-free active substrates, which are key to suppressing the spin dephasing associated with the hyperfine interaction. Modules including $^{28}\text{Si}$ enriched silane for Si, as well as $^{73}\text{Ge}$ depleted germane for SiGe will need to be developed. Critical issues will need to be addressed such as the correct level of isotopic enrichment, the optimal thickness of the isotopically enriched channel taking into account performance, cost and the thermal budget to cope with the self-diffusion between natural and enriched silicon layers \[120\].

From a gate stack/dielectric perspective, material development remains critical since charged defects can affect the static and dynamic properties of the qubits. Stacks with minimized trapped charge densities below $10^{11}$ cm$^{-2}$ will be required. This is likely to rule out high-k dielectrics known to have a large density of defects at the SiO$_2$/high-k interface ($10^{11} - 10^{12}$ cm$^{-2}$) and put an emphasis on high quality Si-SiO$_2$ interfaces, which can have defect densities as low as $5 \times 10^{10}$ cm$^{-2}$. Furthermore, due to the necessity to operate at cryogenic temperatures, the effect of thermal contraction of different materials will need to be studied and minimised. Thermal contraction mismatch between the gate stack and the device body can lead to defect/strain generation \[121, 122\] resulting in enhanced variability in the physical location of the QDs. Doped polycrystalline silicon gates are likely to minimise these effects. Tungsten, with a thermal expansion coefficient similar to that of silicon (4.5 x $10^{-6}$ K$^{-1}$ vs 2.6 x $10^{-6}$ K$^{-1}$), may be an interesting candidate for lower resistivity gate material.

The impact of metal gate granularity on the variability of the gate voltage for QD formation should also be minimised to avoid workfunction fluctuations \[123, 124\].

Considering now the variability in spin qubit operation frequencies, this is primarily determined by the variability in electron (or hole) G-tensor due to spin-orbit coupling, which in turn is influenced by a number of device and materials-related parameters, including interface roughness \[126\] and valley occupancy \[127\]. For electron spins in MOS QDs, the variations on the g-factor are typically $\Delta g/g \approx 10^{-2}$ \[119\]. These variations could be partially mitigated by Stark shift but the strengths experiementally demonstrated ($\Delta g/g \approx 10^{-3}$ \[126\]) remain too low to for full compensation. The level of variability in G-tensor components for electron spins is also dependent upon the orientation of the static magnetic field with respect to the silicon crystal axes but when the field is aligned along the [100] axis the variability is strongly suppressed \[122\]. Operating in the low magnetic field regime will also reduce qubit-to-qubit frequency variations. After applying these strategies, residual variability in qubit resonance frequencies could be managed by gradient ascent pulse engineering (GRAPE) \[129\].

Finally, variability associated with process changes will also need to be rapidly evaluated at scale to provide statistical evidence of improvement. High-throughput characterization techniques, e.g. based on low temperature (< 4 K) wafer-scale probe stations or cryogenic multiplexers \[130, 132\], will need to be developed to correlate process-induced variability, and help identifying routes for its control and optimization. Furthermore, given the time requirement to tune multiple gate voltages to bias levels where qubits can be operated, the field will strongly benefit from the development of computer-assisted autotuning routines for qubit initialization and parameter extraction \[133, 134\]. Once sources of variability are minimised, techniques to cope with residual variation will need to be developed, perhaps by constructing machine learning models that anticipate qubit performance from room-temperature diagnostic data.
Modelling

In order to speed up our understanding of the parameters that have an impact on qubit performance, microscopic modelling is necessary. The methods to model qubit devices are inspired by techniques used in the CMOS community to understand, for example, disorder and scattering. The main differences with respect to standard CMOS modelling are that, for qubits, modelling needs to be done in the one/few charge regime and rather than simulating electrical currents, the models need to address charge densities and wavefunctions.

From a methodological perspective, finite volume Poisson solvers can initially be used to compute the electrostatic potential in the active region of the device. From there, two methods can be used to compute the figures of merit such as electron filling, valley-splitting, tunnel coupling, g-factor, exchange coupling strength, etc. The first calculates the $N$ single-particle states in the electrostatic potential using either a multi-band $k \cdot p$ or a tight-binding (TB) model. The second leverages existing tool suites and modified effective mass theory.

Up to now, these tools have mostly been used a posteriori to explain valley-splitting, EDSR for electron spins, and to model Rabi frequency. Because more statistical data are now being generated, it might be possible to actually build a complete QCAD (Qubit Computer Aided Design) suite that goes from a microscopic description all the way to qubit array simulation.

CHALLENGES FOR CRYO-CMOS DESIGN

Designing electronic circuits at deep cryogenic temperatures poses some challenges that apply both to the quantum-classical interface and the classical layer. In the following subsections, we describe the impact of temperature on device parameters, power dissipation restrictions and communication latency.

Temperature effects at the device level

Conventional integrated circuit design uses established transistor compact models and passive circuit equivalents that enable predicting the circuit performance before manufacture. Those models needed to be redeveloped for cryogenic temperature operation. In a preliminary exploratory phase, individual technologies were studied at low temperatures which enabled establishing some important initial rules of thumb about transistor performance at cryogenic temperatures and allowed constructing preliminary models.

Bipolar technologies and old CMOS technologies above the 160 nm node are ruled out either because of freeze out of carriers below 4 K or because of the non-linear transistor behaviour, commonly referred to as the “kink effect”, which occurs at $V_{ds} \geq 1.2$ V. However, in general, modern CMOS technologies, both bulk silicon and fully-depleted silicon-on-insulator devices, operate at deep cryogenic temperatures although with modifications that present a weak temperature dependence below 4 K. Firstly, the threshold voltage ($V_{th}$) increases because of bandgap widening, carrier density scaling, and incomplete ionization with typical enhancements for n-type devices of 0.1-0.2 V. Such shifts may compromise technologies with low supply voltage ($V_{dd}$), pointing towards low $V_{th}$ or back-gated silicon-insulator-technologies as optimal choices for deep cryogenic design. The detrimental effect of the increase in $V_{th}$ on the on-state current, $I_{on}$, is partially compensated by an increase in mobility because of the reduced phonon population. Furthermore, the subthreshold swing in MOSFETs decreases because of the reduced thermionic transport down to the level of 10 mV/dec where it saturates to a value proportional to the extent of the conduction-band tail associated with shallow defect states. Although this represents a substantial reduction with respect to room temperature, it is far from the Boltzmann limit of 0.8 mV/dec and 20 $\mu$V/dec at 4 K and 100 mK, respectively. Furthermore, figures of merit such as on-off current ratio, $I_{on}/I_{off}$, and $g_m/I_D$, significantly improve at 4 K, aspects that are expected to enhance the performance of both digital and analogue circuits at cryogenic temperatures. In terms of passive components, quality factors improve at low temperatures. However, there are also disadvantages: Impedance mismatch deteriorates and $1/f$ noise becomes more prevalent due to the reduction of the thermal noise with respect to room temperature which creates different requirements when managing noise.

These initial findings have enabled moving to the next phase of cryogenic IC design in which heuristic knowledge and advanced compact models can be used to design analog and digital circuits to meet high-level specifications. In what follows, the field needs to move on to mass-scale characterisation of transistors and circuits to generate established cryogenic compact models and electronic computer-aided design (ECAD) tools for deep cryogenic temperatures.

Power consumption and communication latency

Active QEC protocols require fast feedback between measurement and control. Utilizing a classical processing unit at room temperature to process the readout outputs and determine the gate sequences to correct for errors can be problematic. Sitting approximately 1.5 m away from the quantum layer, the distance imposes a minimum latency time of 30 ns which becomes comparable, for example, to two-qubit gate times mediated by the exchange interaction. A distributed computer architecture will ultimately limit the bandwidth and pose synchronization challenges. Cryo-electronic circuits in close
proximity with the qubit layer are then desirable to reduce the impact of latency on the efficiency of QEC protocols. However, dynamic operation at cryogenic temperatures puts some tight restrictions on the power budget and presents a concern of up to what level co-integration at millikelvin temperatures, where qubits operate best, may be possible. At 4 K the available cooling power is a few watts whereas at 100 mK is typically below 1 mW. Considering that transistors will have to be (dis)charged at radio or microwave frequencies, dynamic power dissipation is a concern. But several solutions may be put in place to address this challenge:

First of all, recent results indicate that the operation of silicon spin qubits may be performed within error correction thresholds at elevated temperatures (1.1-1.45 K) bridging the gap between the quantum and cryo-electronics by enabling a higher cooling power budget [29, 30, 163]. It must be noted that, so far, operation at higher temperature has been achieved at the cost of reduced fidelity. QEC correction will then require a larger number of physical qubits and associated classical electronics, increasing the overall power consumption. The optimal trade-off between fidelity and cooling power will need to be studied and determined. Further research directed to overcome the deterioration of qubit performance as temperature is increased will benefit the field, for example by using readout methods based on Pauli spin blockade which can provide high fidelity at elevated temperatures [95] or by minimising the increase of charge noise as temperature is increased [163].

Secondly, a new branch of IC design should emerge with the objective to deliver dynamic performance with ultra-low power consumption to meet the demanding specifications for low temperature operation. Since dynamic power dissipation increases with the square of the voltage, the strategy could entail exploring technologies and designs that can operate at ultra-low supply voltages of just a few hundred millivolts. Given the substantial decrease in sub-threshold swing at deep cryogenic temperatures this is a realistic proposition. Here, technologies with $V_{th}$ tuning capabilities like back-gated SOI or even new technology nodes with $V_{th}$ designed for optimal low-power cryogenic operation may provide a solution. We restrict our discussion of power consumption to dynamic rather than static power consumption, the latter being dominated by leakage currents through the channel, which are substantially reduced by two to three orders of magnitude at deep cryogenic temperatures [162].

Thirdly, since dissipation occurs on resistive elements, superconducting interconnects may be used to reduce the impact of dynamic losses, increase signal transmission and reduce the phononic heat flow from the cryogenic electronics to the qubits. However, power is still required to charge transistor gates and cable capacitances which, if not operated adiabatically, will eventually be dissipated. Low-power superconducting electronics such as RSFQ [164] or nTron circuits [165] could also be used instead of CMOS but are yet less evolved.

### Challenges at the Quantum-Classical Interface

As opposed to classical circuits, quantum computers need to have every logic gate individually controlled by external inputs. Furthermore to control and readout spin qubits, high-frequency analog signals are needed. In the following subsections, we describe these aspects that pert ain the quantum-classical interface.

**Signal Routing (I/O Management)**

Brute force approaches by wiring each qubit and exchange gate electrodes to room temperature electronics do not scale well as they require macroscopic electrical wiring and extensive heat load management. Efficiently delivering control and readout signals to increasingly more complex quantum circuits, while reducing the number of room temperature inputs per qubit, is a key challenge in developing a large-scale universal quantum computer [166, 167].

One solution is to explore shared-control approaches in which QDs, as well as tunnel barriers, are controlled by common gates, mimicking the structure of CCD sensors. The approach relies on a high level of uniformity at the quantum layer, for example, by loading a single electron on individual QDs with a single common voltage. It has been recently shown that the standard deviation on the voltage required to load the first measurable electron on 40 nm silicon CMOS technology approaches this requirement [154] but further improvements will need to be made. Furthermore, variability in the tunnel coupling will be important in shared control schemes requiring spin shuttling and would need to be engineered to be controllable within an order of magnitude across the array [47]. High quality material stack and fabrication techniques will be needed to achieve this level of uniformity and this is were advanced CMOS fabrication could make a difference.

While advances are made on reducing variability, parallel efforts should focus on developing addressing methods that deliver independent signals to each gate with a smaller number of resources, for example by using row-column addressing methods as in dynamic random access memory (DRAM) and CMOS image sensors. Qubit cell matrices with row-column addressing could provide independent control over $N$ qubits with $O(\sqrt{N})$ room temperature resources by sacrificing simultaneous operation [21]. Memory functionality will need to be added in the form of floating capacitors to retain voltages at the relevant gates for a period much longer than the coherence time of the qubits [168-170]. To extend the retention time and minimise unwanted voltage drifts at the gate, thicker gate oxides and low operation gate voltages will be beneficial. Efficient readout of such arrays could be achieved by using mixed high-frequency readout methods combining FDMA and TDMA [171].
Control and readout electronics

A common feature for control and readout electronics is the necessity to generate IQ-modulated radio or microwave signals while additionally, for readout, reflected signals need to be demodulated. A generic architecture amenable to integration is one of a radio transceiver, with the difference that it must be designed to operate at cryogenic temperatures. Figure 2b shows such an architecture [172], where one can recognize the readout path, represented by multiplexers, amplifiers, demodulators, and ADCs. Typically, the voltage of the devices to be read is just a few tens of microvolts and, when using reflectometry techniques for sensing, the reflected amplitudes to be measured may even be smaller. Therefore, there is a need for amplifying the signals before demodulating them. Traditionally, this task is performed by a cryogenic high-electron-mobility low-noise amplifier (LNA), with low noise equivalent temperature ($T_N$) – this figure determines the noise level of the measurement and is typically of the order of a few Kelvin. Furthermore, it requires an amplification of the order of 40 dB or more to minimise the impact of subsequent amplifying stages placed at room temperature. Circulators are typically placed in between the QPU and the LNA to minimise interference between forward and backward travelling waves (not shown). Readout can be multiplexed in time (TDMA) and/or in frequency (FDMA). In the latter case, the bandwidth of the LNA becomes an important factor due to the need to spectrally pack several readout tones in the same channel. Thus, typically bandwidths of the order of a gigahertz or higher are desirable. Although LNAs are typically manufactured using InP, SiGe-based amplifiers with $T_N = 2$ K have been demonstrated and could be integrated with CMOS or SiGe BiCMOS [173]. Recently, several of these elements have been integrated on a chip to provide a compact alternative to distributed readout electronics for high-frequency gate-based readout: (i) an integrated CMOS transceiver addressing the 6-to-8 GHz band including, on a single chip operating at 4 K, RF amplifiers, I/Q downconversion mixers, and baseband amplifiers and filters [174] and (ii) a fully integrated 5-to-6.5 GHz I/Q receiver operating at 3.5 K, also incorporating a low-noise MW amplifier as well as readout signal generation [175].

To reduce further $T_N$, quantum-limited amplifiers such as the Josephson parameter amplifier (JPA) could be used in conjunction with dispersive readout sensors [107], an approach routinely used for superconducting qubits [1]. The JPA in phase-preserving mode enables reducing the readout time by an order of magnitude with respect to conventional cryogenic amplifiers and in phase-sensitive mode could enable going beyond the quantum limit using quadrature squeezing. For large amplification bandwidth necessary for FDMA, travelling wave amplifiers (TWPA) may be used. And for full-integration, parametric amplifiers based on the dissipationless quantum capacitance of silicon QDs could be explored [115].

The control path in Fig. 2b shows DACs, IQ modulators and rf amplifiers aimed to assist controlling the qubits, potentially through multiplexing. Spin control is achieved through local oscillators that are IQ modulated to create a series of carefully timed envelopes. In recent demonstrations using cryo-CMOS integrated circuits [176,178], operation has been based on a programmable frequency, spanning from 1 to 20 GHz, so as to allow for sufficient flexibility in the type and number of qubits that can be controlled. More recently, the digital section of the control has grown substantially, to perform sophisticated modulation of $4 \times 32$ frequencies, which are upconverted only in the last rf stage [177]. This approach has been used to control electron spin qubits in SiGe with the same fidelity as with commercial instruments at room temperature and could deliver the desired performance at power consumption compatible with 4 K operation for several tens of qubits simultaneously (1 mW/qubit) [179]. Recently, a fully integrated cryo-CMOS chip combining both control MW signals in the 11-to-17 GHz range and readout on the 200-to-600 MHz range based for rf-SETs has been demonstrated at 4 K [180].

More generally, to link the impact of the control and readout electronics on qubit fidelity, a simulation framework SPINE (SPIN Emulator) [181] has been developed. SPINE enables determining the minimum set of specifications for the control and readout electronics in order not to become the bottleneck in QPU performance. It does so by linking a qubit’s time evolution with the time varying signals generated by the classical electronics.

CHALLENGES AT THE CLASSICAL LAYER

After the analog readout is performed, digital decoding of the qubit measurements and the formulation of a response to control them with an appropriate set of signals needs to be put in place. For this, the classical logic will need to operate significantly faster than qubits to read, identify the error, and produce the response with high fidelity. Even if the operation timescales for silicon qubits could be pushed down to 10 or 100 ns, this could still be managed with current classical processors with clock rates at 3 GHz. However, in terms of classical processor performance, error decoding at scale may pose a challenge. Assuming QEC cycles [8] in the submicrosecond regime, reading a million qubits and determining whether errors have occurred will require processing > 1 Tbits/s. The most suitable processor architectures to handle the data efficiently while minimizing power consumption will need to be investigated.

Digital circuits are much less problematic than analog, due to the large noise margins. The first circuits have been based on reconfigurable architectures, in particular FPGAs [132, 152, 182]. FPGAs could operate normally in deep-cryogenic temperatures and all the functions could be activated. Independently, QEC algorithms have been designed and implemented in room temperature
FPGAs [183]. The current trend is to combine these advances into FPGAs operated at cryogenic temperatures improving the feedback speed and reducing latency in QEC or enabling surface code decoding through machine learning techniques [184]. FPGAs will likely be used to enable fast back and forth communication in QEC but also in hybrid quantum-classical algorithms like the Variational Quantum Eigensolvers (VQE) [24] and quantum approximate optimization algorithms (QAOA) [25].

Another aspect relevant to classical logic performance at low temperature is that reduced leakage currents can make DRAMs essentially static, thereby enabling significant reduction in real estate utilization or alternatively in the increase of memory available to the controller. A considerable increase of memory could enable more sophisticated waveforms to counter the effects of simultaneous control of an increasing number of qubits and to enable true scalability.

**CHALLENGES AT THE ARCHITECTURE LEVEL**

To build a QCS, the quantum and classical layers and their interface need to be assembled in a functional manner. This raises the question of what the best system configuration is and what temperature the different function blocks should be placed at. These layers can be almost independently optimised. So far, the approach has been bottom-up, thinking of the optimal quantum layer and building all the way up.

One of the big advantages of silicon in terms of scaling, its small qubit footprint, also poses some challenges in terms of system design: The I/O problem, and the location of the classical electronics with respect to the quantum layer. All considerations apart from that of power consumption indicate that monolithic integration would be optimal. However, if the classical electronics is co-located in the plane with the quantum layer, the 2D array necessary for QEC would be broken. With these requirements in mind, several architectures have been proposed with varying levels of integration going from full 3D integration to 2D modular designs to account for limitations, leverage know-how and validate elementary designs (Fig. 4).

3D Integration: The current variability of the voltages used to confine the charges and to tune the coupling between adjacent QDs, suggests individual gate addressing. To manage the large gate overhead researchers have proposed to co-locate floating memory units with embedded control transistors (similar to 1T-1C DRAM modules) to minimise the number of I/O connections [21]. These memory units enable individual biases for each QD and exchange gate in a row/column addressed matrix but require of periodic voltage refreshing. Though indeed this architecture solves the challenge of managing local variability and the I/O problem, this proposal relies on aggressive technological assumptions: short gate pitch, 3D integration of quantum and classical electronics, and the management of crosstalk between signal in the gigahertz regime, aspects that have not yet been routinely demonstrated by the semiconductor industry.

An alternative monolithic 3D integrated architecture has been proposed with the focus on integrating readout on chip and providing a simpler way of initializing the qubits using two-layers: the bottom one for electrometre and reservoir definition, and the top one to encode qubits [49]. One advantage of the proposal is that enables implementing the surface code in a $2 \times 2$ QD sub-lattice since every qubit has a dedicated rf sensor capable of spin readout, whereas the aforementioned design requires a $2 \times 3$ sub-lattice. [21] due to the necessity to do projective Pauli spin blockade readout (Fig. 3b). 2D Integration: Subsequent proposals simplified the architecture by moving to planar designs. The floating gate arrangement was replaced by a 2D monolithic design including three gate layers: row, column and diagonal, to control the QDs and the horizontal and vertical exchange, respectively [47]. Readout and control electronics is displaced to the periphery by making use of dispersive readout and multiplexed microwave signals. Although compatible with current technology, the architecture relies on shared control that requires a level of uniformity still to be demonstrated.

2D Modular: Recently, researchers proposed modular 2D sparse geometries to relax the fabrication and variability constraints [30, 46, 48]. The concept offers flexibility to accommodate the gate layouts to individually tune QDs and exchange interactions in local registers and introduces the concept of long-distance coupling between spatially separated registers. Separated qubit registers could alleviate wiring problems, reduce crosstalk and free up space to co-locate classical electronics modules. Several methods for long-distance coherent coupling over distances varying from microns to millimetres exist but the most widely studied rely on charge or spin shuttling [185, 186], or microwave-photon-mediated spin-spin interactions [187]. For shuttling, two mechanisms exist: (i) Surface acoustic waves (SAW) [188] and (ii) CCD-inspired tunnelling between adjacent QDs [189, 191]. SAW-based spin transfer is most effective in piezoelectric materials and has been used to displace an electron spin between two AlGaAs/GaAs-based QDs separated by 6 µm with up to 90% fidelity [192]. The feasibility of this mechanism in silicon remains to be investigated but it will possibly require the use of additional piezoelectric materials. On the other hand, CCD-inspired shuttling has been demonstrated in silicon: individual electrons have been transferred over micrometer distances [190] and coherent spin shuttling has been achieved between two adjacent QDs with an average fidelity of 99.4% [62]. Demonstrating coherent spin transfer in a QD array spanning micrometres length scales with high fidelity remains to be demonstrated. It would be necessary to minimise the local g-factor differences between QDs with the strategies described above.
mediated interactions via real or virtual microwave photons are not yet at the threshold for fault tolerance due to the difficulty to achieve coherent coupling rates between a single spin and a photon largely exceeding the spin and photon decay rates. However, results on large coherent coupling rates in industry-fabricated double QDs [102] and the progress on developing high-impedance resonators [104] may lead to fault-tolerant fidelities in the near future.

OUTLOOK

We have examined how scaling silicon-based quantum computing could benefit from using CMOS fabrication lines and have drawn attention to the system-level design of a quantum computer: a holistic perspective that includes the quantum layer, the quantum-classical interface and the classical processing unit. Silicon offers the enticing advantage that all these different layers could, in principle, be manufactured using CMOS processes opening opportunities for compact system integration and low-cost manufacturing. Small silicon-based quantum processors may be readily manufacturable using CMOS technology; for large-scale fault-tolerant processors further development beyond the current capabilities of VLSI technology will be required but we foresee no fundamental roadblock. We have highlighted here the key engineering challenges and provided directions for how to address them.

The transition from fabrication at industrial-grade research and technology organizations to standard silicon foundries provides an opportunity for all of the different layers of a QCS. In particular, establishing a global Multi-Project Wafer prototyping service for silicon quantum circuits, with a larger flexibility in the violation of design rules, could have profound influence in the development of silicon-based quantum computing. It could lead to standardization, increased fabrication throughput, and improved accessibility to quantum devices and circuits. It could also reduce the timescales to the final goal: creating a large-scale fault-tolerant quantum computer.

The realization of large-scale quantum computer will require a synergy between researchers with expertise in the control of elementary quantum systems and specialists in systems engineering from the semiconductor industry. Of equal value will be the promotion of specialised degrees that explore the boundaries between quantum physics and engineering, in order to train new professionals with simultaneous expertise in Pauli matrices and Verilog-A. We hope this Review will help stimulate the curiosity of the required range of researchers — from specialists in the CMOS community to new graduate students — who can join the exciting endeavour of building a large-scale silicon-based quantum computer.

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AUTHOR CONTRIBUTIONS

All authors contributed to the writing of the manuscript.

COMPETING INTEREST

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M.V., S.D.F., T.M. and A.S.D. declare no financial competing interest.

[1] Arute, F. et al. Quantum supremacy using a programmable superconducting processor. *Nature* **574**, 505–510 (2019).
[2] Zhong, H.-S. et al. Quantum computational advantage using photons. *Nature* **370**, 1460–1463 (2020).
[3] Sarma, S. D., Freedman, M. & Nayak, C. Majorana zero modes and topological quantum computation. *Npj Quantum Inf.* **1**, 15001 (2015).
[4] Karzig, T. et al. Scalable designs for quasiparticle-poisoning-protected topological quantum computation with majorana zero modes. *Phys. Rev. B* **95**, 235305 (2017).
[5] Lidar, D. & Brun, T. *Quantum Error Correction* (Cambridge University Press., 2013).
[6] Devitt, S. J., Munro, W. J. & Nemoto, K. Quantum error correction for beginners. *Rep. Prog. Phys.* **76**, 76001 (2013).
[7] Campbell, E. T., Terhal, B. M. & Vuillot, C. Roads...
towards fault-tolerant universal quantum computation. Nature 549, 172–179 (2017).

[8] Fowler, A. G., Marriotti, M., Martinis, J. M. & Cleland, A. N. Surface codes: Towards practical large-scale quantum computation. Phys. Rev. A 86, 32324 (2012).

[9] Bauer, B., Wecker, D., Millis, A. J., Hastings, M. B. & Troyer, M. Hybrid quantum-classical approach to correlated materials. Phys. Rev. X 6, 31045 (2016).

[10] Reifer, M., Wiebe, N., Svore, K. M., Wecker, D. & Troyer, M. Elucidating reaction mechanisms on quantum computers. Proc. Natl. Acad. Sci. 114, 7555–7560 (2017).

[11] Shor, P. W. Polynomial-time algorithms for prime factorization and discrete logarithms on a quantum computer. Siam J. Comput. 26, 1484–1509 (1997).

[12] Monroe, C. & Kim, J. Scaling the ion trap quantum processor. Science 339, 1164–1169 (2013).

[13] Devoret, M. H. & Schoelkopf, R. J. Superconducting circuits for quantum information: An outlook. Science 339, 1169–1174 (2013).

[14] Awschalom, D. D., Bassett, L. C., Dzurak, A. S., Hu, E. L. & Petta, J. R. Quantum spintronics: Engineering and manipulating atom-like spins in semiconductors. Science 339, 1174–1179 (2013).

[15] Knill, E., Laflamme, R. & Milburn, G. J. A scheme for efficient quantum computation with linear optics. Nature 409, 46–52 (2001).

[16] Kawakami, E. et al. Electrical control of a long-lived spin qubit in a Si/SiGe quantum dot. Nat. Nano. 9, 666–670 (2014).

[17] Huang, W. et al. Fidelity benchmarks for two-qubit gates in silicon. Nature 569, 532–536 (2019).

[18] Maurand, R. et al. A CMOS silicon spin qubit. Nat. Commun. 7, 13575 (2016).

[19] Zwerver, A. M. J. et al. Qubits made by advanced semiconductor manufacturing (2021). URL https://arxiv.org/abs/2101.12650

[20] Camenzind, L. C. et al. A spin qubit in a fin field-effect transistor (2021). URL https://arxiv.org/abs/2103.07369

[21] Veldhorst, M., Eenink, H. G. J., Yang, C. H. & Dzurak, A. S. Silicon CMOS architecture for a spin-based quantum computer. Nature 549, 172–179 (2017).

[22] Electrically driven electron spin resonance in a slanting zeeman field. Nat. Phys. 4, 776–779 (2008).

[23] Lekitsch, B. et al. A single-atom electron spin qubit in silicon. Nature 489, 541–545 (2012).

[24] Vinet, M. et al. A two-qubit logic gate in silicon. Nature 526, 410–414 (2015).

[25] Noiri, A. et al. Integrated silicon qubit platform with single-spin addressability, exchange control and single-shot singlet-triplet readout. Nat. Commun. 9, 4370 (2018).

[26] Zajac, D. M. et al. Resonantly driven CNOT gate for electron spins. Science 359, 439–442 (2018).

[27] Vandersypen, L. M. K. Scaling up semiconductor spin qubits. APS March Meeting V35.00002 (2021).

[28] Jones, N. C. et al. Engineering the quantum-classical interface of solid-state qubits. NPJ Quantum Inf. 3, 34 (2017).

[29] Li, R. et al. A crossbar network for silicon quantum dot qubits. Sci. Adv. 4, eaar3960 (2018).

[30] Boter, J. M. et al. A sparse spin qubit array with integrated control electronics In 2019 IEEE International Electron Devices Meeting (IEDM), 31.4.1–31.4.4 (2019).

[31] Vinet, M. et al. Towards scalable silicon quantum computing. In 2018 IEEE International Electron Devices Meeting (IEDM), 6.5.1–6.5.4 (2018).

[32] Cressler, J. D. Silicon Earth : Introduction to the Microelectronics and Nanotechnology Revolution (Cambridge University Press, 2009).

[33] Crippa, A. et al. Electrically driven electron spin resonance mediated by spin-valley-orbit coupling in a silicon quantum dot. NPJ Quantum Inf. 4, 6 (2018).

[34] Veldhorst, M. et al. An addressable quantum dot qubit with fault-tolerant control-fidelity. Nat. Nano. 9, 981–985 (2014).

[35] Yang, C. H. et al. Operation of a silicon quantum processor unit cell above one Kelvin. Nature 580, 350–354 (2020).
Ansaloni, F. et al. Single-electron control in a foundry-fabricated two-dimensional qubit array. Nat. Commun. 11, 6399 (2020).

Zajac, D. M., Hazard, T. M., Mi, X., Nielsen, E. & Petta, J. R. Scalable gate architecture for a one-dimensional array of semiconductor spin qubits. Phys. Rev. App. 6, 54013 (2016).

Geyer, S. et al. Self-aligned gates for scalable silicon quantum computing. App Phys Lett 118, 104004 (2021).

Hutin, L. et al. Gate reflectometry for probing charge and spin states in linear Si MOS split-gate arrays. In 2019 IEEE International Electron Devices Meeting (IEDM), 37.7.1–37.7.4 (2019).

Chanrion, E. et al. Charge detection in an array of CMOS quantum dots. Phys. Rev. App, 024066 (2020).

Gilbert, W. et al. Single-electron operation of a silicon-CMOS 2x2 quantum dot array with integrated charge sensing. Nano Lett. 11, 7892 (2020).

Duan, J. et al. Remote capacitive sensing in two dimensional quantum dot arrays. Nano Lett. 10, 7123 (2020).

Jones, C. et al. Logical qubit in a linear array of semiconductor quantum dots. Phys. Rev. X 8, 021058 (2018).

Malinowski, F. K. et al. Fast spin exchange across a multielectron mediator. Nat. Commun. 10, 1196 (2019).

Burkard, G., Gullans, M. J., Xi, X. & Petta, J. R. Superconductor-semiconductor hybrid-circuit quantum electrodynamics. Nat. Rev. Phys. 2, 129–140 (2020).

Yoneda, J. et al. Coherent spin qubit transport in silicon (2020). URL https://arxiv.org/abs/2008.04020

Yoneda, J. et al. A quantum-dot spin qubit with coherence limited by charge noise and fidelity higher than 99.9%. Nat. Nano. 13, 102 (2018).

Dehollain, J. P. et al. Nanoscale broadband transmission lines for spin qubit control. Nanotechnology 24, 15202 (2012).

Laucht, A. et al. Electrically controlling single-spin qubits in a continuous microwave field. Sci. Adv. 1, e1500022 (2015).

Kong, W.-C. et al. Introduction of dc line structures into a superconducting microwave 3D cavity. Rev. Sci. Inst. 86, 023108 (2015).

Vahapoglu, E. et al. Single-electron spin resonance in a nanoelectronic device using a global field. Sci. Adv. 7, eabg9158 (2021).

Vahapoglu, E. et al. Coherent control of electron spin qubits in silicon using a global field (2021). URL https://arxiv.org/abs/2107.14622

Kawakami, E. et al. Gate fidelity and coherence of an electron spin in an Si/SiGe quantum dot with micromagnet. Proc. Natl. Acad. Sci. 113, 11738–11743 (2016).

Struck, T. et al. Low-frequency spin qubit energy splitting noise in highly purified 6H-Si/SiGe. Npj Quantum Inf. 6, 40 (2020).

Borjans, F., Zajac, D. M., Hazard, T. M. & Petta, J. R. Single-spin relaxation in a synthetic spin-orbit field. Phys. Rev. App. 11, 44063 (2019).

Simion, G. et al. A scalable one dimensional silicon qubit array with nanomagnets. In 2019 IEEE International Electron Devices Meeting (IEDM), 30.2.1–30.2.4 (2020).

Singh, K., Clarke, J. S., Veldhorst, M. & Vandersypen, L. M. K. Quantum dot devices, US-2020135864-A1 (2017).

Crippa, A. et al. Gate-reflectometry dispersive readout and coherent control of a spin qubit in silicon. Nat. Commun. 10, 2776 (2019).

Bosco, S., Hetényi, B. & Loss, D. Hole spin qubits in Si finFETs with fully tunable spin-orbit coupling and sweet spots for charge noise. Phys. Rev. X Quantum 2, 010348 (2021).

Martins, F. et al. Noise suppression using symmetric exchange gates in spin qubits. Phys. Rev. Lett. 116, 116012 (2016).

Reed, M. D. et al. Reduced sensitivity to charge noise in semiconductor spin qubits via symmetric operation. Phys. Rev. Lett. 116, 110402 (2016).

Shim, Y.-P. & Tahan, C. Barrier versus tilt exchange gate operations in spin-based quantum computing. Phys. Rev. B 97, 155402 (2018).

He, Y. et al. A two-qubit gate between phosphorus donor electrons in silicon. Nature 571, 371–375 (2019).

Malinowski, F. K. et al. Spin of a multielectron quantum dot and its interaction with a neighboring electron. Phys. Rev. X 8, 011045 (2018).

Shulman, M. D. et al. Demonstration of entanglement of electrostatically coupled singlet-triplet qubits. Science 336, 202 (2012).

Petta, J. R. et al. Coherent manipulation of coupled electron spins in semiconductor quantum dots. Science 309, 2180–2184 (2005).

Laucht, A. et al. Roadmap on quantum nanotechnologies. Nanotechnology 32, 16 (2021).

Ono, K., Austing, D. G., Tokura, Y. & Tarucha, S. Current rectification by Pauli exclusion in a weakly coupled double quantum dot system. Science 297, 1313–1317 (2002).

Kastner, M. A. The single-electron transistor. Rev. Mod. Phys. 64, 849–858 (1992).

Le Guevel, L. Low-power transimpedance amplifier for cryogenic integration with quantum devices. App. Phys. Rev. 7, 041407 (2020).

Schoelkopf, R. J., Wahlgren, P., Kozehevnikov, A. A., Delsing, P. & Prober, D. E. The radio-frequency single-electron transistor (rf-SET): A fast and ultrasensitive electrometer. Science 280, 1238–1242 (1998).

Angus, S. J., Ferguson, A. J., Dzurak, A. S. & Clark, R. G. A silicon radio-frequency single electron transistor. App. Phys. Lett. 92, 112103 (2008).

Curry, M. J. et al. Single-shot readout performance of two heterojunction-bipolar-transistor amplification circuits at millikelvin temperatures. Sci. Rep. 9, 16976 (2019).

Connors, E. J., Nelson, J. & Nichol, J. M. Rapid high-fidelity spin-state readout in Si/Si-Ge quantum dots via rf reflectometry. Phys Rev App. 13, 024019 (2020).

House, M. et al. High-sensitivity charge detection with a single-lead quantum dot for scalable quantum computation. Phys. Rev. App. 6, 044016 (2016).

Ciriano-Tejel, V. N. et al. Spin readout of a CMOS quantum dot by gate reflectometry and spin-dependent tunneling. Phys. Rev. X Quantum 2, 010353 (2021).

Urdampilleta, M. et al. Gate-based high fidelity spin readout in a CMOS device. Nat. Nano. 14, 737–741 (2019).
[96] Wallraff, A. et al. Strong coupling of a single photon to a superconducting qubit using circuit quantum electrodynamics. *Nature* **431**, 162 (2004).

[97] Colless, J. I. et al. Dispersive readout of a few-electron double quantum dot with fast rf gate sensors. *Phys. Rev. Lett.* **110**, 46805 (2013).

[98] Gonzalez-Zalba, M. F., Barraud, S., Ferguson, A. J. & Betz, A. C. Probing the limits of gate-based charge sensing. *Nat. Commun.* **6**, 6084 (2015).

[99] Mi, X. et al. A coherent spin–photon interface in silicon. *Nature* **555**, 599–603 (2018).

[100] Pakkiam, P. et al. Single-shot single-gate rf spin readout in silicon. *Phys. Rev. X* **8**, 41032 (2018).

[101] West, A. et al. Gate-based single-shot readout of spins in silicon. *Nat. Nano.* **14**, 437 (2019).

[102] Ibberson, D. J. et al. Large dispersive interaction between a CMOS double quantum dot and microwave photons. *Phys. Rev. X Quantum* **2**, 020315 (2021).

[103] Mizuta, R., Otxoa, R., Betz, A. & Gonzalez-Zalba, M. Quantum and tunneling capacitance in charge and spin qubits. *Phys. Rev. B* **95**, 045414 (2017).

[104] Zheng, G. et al. Rapid gate-based spin read-out in silicon using an on-chip resonator. *Nat. Nano.* **14**, 742–746 (2019).

[105] Hornebrook, J. M. et al. Frequency multiplexing for readout of spin qubits. *App. Phys. Lett.* **104**, 103108 (2014).

[106] Schaal, S. et al. A CMOS dynamic random access architecture for radio-frequency readout of quantum devices. *Nat. Elect.** **2**, 236 (2019).

[107] Schaal, S. et al. Fast gate-based readout of silicon quantum dots using Josephson parametric amplification. *Phys. Rev. Lett.* **124**, 067701 (2020).

[108] Stockklauser, A. et al. Strong coupling cavity QED with gate-defined double quantum dots enabled by a high impedance resonator. *Phys. Rev. X* **7**, 11030 (2017).

[109] Samkharadze, N. et al. High-kinetic-inductance superconducting nanowire resonators for circuit QED in a magnetic field. *Phys. Rev. App.* **5**, 44004 (2016).

[110] Mazin, B. A. Microwave kinetic inductance detectors Ph.D. thesis, California Institute of Technology (2004).

[111] Vissers, M. R. et al. Low loss superconducting titanium nitride coplanar waveguide resonators. *App. Phys. Lett.* **97**, 232509 (2010).

[112] Shearwood, A. et al. Atomic layer deposition of titanium nitride for quantum circuits. *App. Phys. Lett.* **113**, 212601 (2018).

[113] Grünhaupt, L. et al. Loss mechanisms and quasiparticle dynamics in superconducting microwave resonators made of thin-film granular aluminum. *Phys. Rev. Lett.* **121**, 117001 (2018).

[114] Grünhaupt, L. et al. Granular aluminium as a superconducting material for high-impedance quantum circuits. *Nat. Mat.* **18**, 816–819 (2019).

[115] Esterli, M., Otxoa, R. & Gonzalez-Zalba, M. Small-signal equivalent circuit for double quantum dots at low-frequencies. *App. Phys. Lett.* **114**, 255305 (2019).

[116] Maman, V. D., Gonzalez-Zalba, M. & Pályi, A. Charge noise and overdrive errors in dispersive readout of charge, spin, and majorana qubits. *Phys. Rev. App.* **14**, 064024 (2020).

[117] Culcer, D., Hu, X. & Sarma, S. D. Interface roughness, valley-orbit coupling, and valley manipulation in quantum dots. *Phys. Rev. B* **82**, 205315 (2010).

[118] Rahman, R. et al. Engineered valley-orbit splittings in quantum-confined nanostructures in silicon. *Phys. Rev. B* **83**, 195323 (2011).

[119] Ferdous, R. et al. Valley dependent anisotropic spin splitting in silicon quantum dots. *Npj Quantum Inf.* **4**, 26 (2018).

[120] Mazzocchi, V. et al. 99.992% 28Si cvd-grown epilayer on 300 nm substrates for large scale integration of silicon spin qubits. *Journal of Crystal Growth* **509**, 1–7 (2019).

[121] Lo, C. et al. Hybrid optical-electrical detection of donor electron spins with bound excitons in silicon. *Nat. Mat.* **14**, 490–494 (2015).

[122] Thorbeck, T. & Zimmerman, N. M. Formation of strain-induced quantum dots in gated semiconductor nanostructures. *AIP Adv.* **5**, 87107 (2015).

[123] Zhang, Q. et al. Experimental study of gate-first finFET threshold-voltage mismatch. *IEEE Trans. Electron Devices* **61**, 643–646 (2014).

[124] Zeng, Z., Triozon, F. & Niquet, Y.-M. Carrier scattering in high-k/metal gate stacks. *J. Appl. Phys.* **121**, 114503 (2017).

[125] Brauns, M., Amitonov, S. V., Spruijtjenburg, P.-C. & Zwanenburg, F. A. Palladium gates for reproducible quantum dots in silicon. *Sci. Rep.* **8**, 5690 (2018).

[126] Huang, W., Veldhorst, M., Zimmerman, N. M., Dzurak, A. S. & Culcer, D. Electrically driven spin qubit based on valley mixing. *Phys. Rev. B* **95**, 75403 (2017).

[127] Veldhorst, M. et al. Spin-orbit coupling and operation of multivalley spin qubits. *Phys. Rev. B* **92**, 204101 (2015).

[128] Tanttu, T. et al. Controlling spin-orbit interactions in silicon quantum dots using magnetic field direction. *Phys. Rev. X* **9**, 21028 (2019).

[129] Khaneja, N., Reiss, T., Kehlet, C., Schulte-Herbrüggen, T. & Glaser, S. J. Optimal control of coupled spin dynamics: design of NMR pulse sequences by gradient ascent algorithms. *J. Magn. Reson.* **172**, 296–305 (2005).

[130] Puddy, R. K. et al. Multiplexed charge-locking device for large arrays of quantum devices. *App. Phys. Lett.* **107**, 143501 (2015).

[131] Pauka, S. et al. Characterizing quantum devices at scale with custom cryo-CMOS. *Phys. Rev. App.* **13**, 054072 (2020).

[132] Wuetz, B. P. et al. Multiplexed quantum transport using commercial off-the-shelf CMOS at sub-Kelvin temperatures. *Npj Quantum Inf.* **6**, 43 (2020).

[133] Baart, T. A., Eendebak, P. T., Reichl, C., Wegscheider, W. & Vandersypen, L. M. K. Computer-automated tuning of semiconductor double quantum dots into the single-electron regime. *App. Phys. Lett.* **108**, 213104 (2016).

[134] Moon, H. et al. Machine learning enables completely automatic tuning of a quantum device faster than human experts *Nat. Commun.* **11**, 4161 (2020).

[135] Venitucci, B., Li, J., Bourdet, L. & Niquet, Y. Modeling silicon CMOS devices for quantum computing. In *2019 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, 1–4 (2019).

[136] Mohiyaddin, F. A. et al. Multiphysics simulation design of silicon quantum dot qubit devices. In *2019 IEEE International Electron Devices Meeting (IEDM)*, 39.5.1–39.5.4 (2019).

[137] Gamble, J. K. et al. Valley splitting of single-electron Si MOS quantum dots. *App. Phys. Lett.* **109**, 253101
[138] Iberson, D. J. et al. Electric-field tuning of the valley splitting in silicon corner dots. *App. Phys. Lett.* **113**, 53104 (2018).

[139] Bourdet, L. et al. All-electrical control of a hybrid electron spin/valley quantum bit in SOI CMOS technology. *IEEE Trans. Electron Devices* **65**, 5151–5156 (2018).

[140] Bourdet, L. & Niquet, Y.-M. All-electrical manipulation of silicon spin qubits with tunable spin-valley mixing. *Phys. Rev. B* **97**, 155433 (2018).

[141] Venitucci, B. & Niquet, Y.-M. Simple model for electrical hole spin manipulation in semiconductor quantum dots: Impact of dot material and orientation. *Phys. Rev. B* **99**, 115317 (2019).

[142] Hommille, H. et al. A reconfigurable cryogenic platform for the classical control of quantum processors. *Rev. Sci. Inst.* **88**, 45103 (2017).

[143] Kangar, A. Subthreshold behavior of silicon MOSFETs at 4.2 K. *Solid State Electron.* **25**, 537–539 (1982).

[144] Hanamura, H. et al. Operation of bulk CMOS devices at very low temperatures. *IEEE J. Solid-State Circuits* **21**, 484–490 (1986).

[145] Balestra, F., Audaire, L. & Lucas, C. Influence of substrate freeze-out on the characteristics of MOS transistors at very low temperatures. *Solid-State Electron.* **30**, 321–327 (1987).

[146] Broadbent, S. B. CMOS operation below freezeout. In *Proceedings of the Workshop on Low Temperature Semiconductor Electronics*, 43–47 (1989).

[147] Balestra, F. & Ghibaudo, G. Brief review of the MOS device physics for low temperature electronics. *Solid-State Electron.* **37**, 1967 – 1975 (1994).

[148] Simoen, E. & Claeyss, C. Impact of CMOS processing steps on the drain current kink of nMOSFETs at liquid helium temperature. *IEEE Trans. Electron Devices* **48**, 1207–1215 (2001).

[149] Yoshikawa, N. et al. Characterization of 4 K CMOS devices and circuits for hybrid Josephson-CMOS systems. *IEEE Trans. Appl. Supercond.* **15**, 267–271 (2005).

[150] Hong, S. et al. Low-temperature performance of nanoscale MOSFET for deep-space rf applications. *IEEE Electron Device Lett.* **29**, 775–777 (2008).

[151] Coskun, A. H. & Bardin, J. Cryogenic small-signal and noise performance of 32 nm SOI CMOS. *2014 IEEE MTT-S International Microwave Symposium (IMS2014)* (2014).

[152] Hommille, H. A. R. Cryogenic electronics for the readout of quantum processors. Ph.D. thesis, Technical University Delft (2019).

[153] Beckers, A., Jazaeri, F. & Enz, C. Cryogenic MOSFET threshold voltage model *ESSDERC* –, 94–97 (2019).

[154] Yang, T. et al. Quantum transport in 40-nm MOSFETs at deep-cryogenic temperatures. *IEEE Electron Device Lett.* **41**, 981–984 (2020).

[155] Bohuslavskiy, H. et al. Cryogenic subthreshold swing saturation in FD-SOI MOSFETs described with band broadening. *IEEE Electron Device Lett.* **40**, 784–787 (2019).

[156] Beckers, A., Jazaeri, F. & Enz, C. Theoretical limit of low temperature subthreshold swing in field-effect transistors. *IEEE Electron Device Lett.* **276**–279 (2019).

[157] Patra, B. et al. Characterization and analysis of on-chip microwave passive components at cryogenic temperatures. *IEEE J. Electron Devices Soc.* **8**, 448–456 (2020).

[158] Patra, B. et al. Cryo-CMOS circuits and systems for quantum computing applications. *IEEE J. Solid-State Circuits* **53**, 309–321 (2018).

[159] Incandela, R. M. et al. Characterization and compact modeling of nanometer CMOS transistors at deep-cryogenic temperatures. *IEEE J. Electron Devices Soc.* **6**, 996–1006 (2018).

[160] Hart, P. A. T., Babaie, M., Charbon, E., Vladimirescu, A. & Sebastiani, F. Subthreshold mismatch in nanometer CMOS at cryogenic temperatures. *IEEE J. Electron Devices Soc.* **8**, 797–806 (2020).

[161] Gały, P. et al. Cryogenic temperature characterization of a 28-nm FD-SOI dedicated structure for advanced CMOS and quantum technologies co-integration. *IEEE J. Electron Devices Soc.* **6**, 594–600 (2018).

[162] Beckers, A. et al. Characterization and modeling of 28-nm FD-SOI CMOS technology down to cryogenic temperatures. *Solid-State Electron.* **159**, 106–115 (2019).

[163] Petit, L. et al. Spin lifetime and charge noise in hot silicon quantum dot qubits. *Phys. Rev. Lett.* **121**, 76801 (2018).

[164] Likharev, K. K. & Semenov, V. K. RSFQ logic/memory family: a new Josephson-junction technology for sub-terahertz-clock-frequency digital systems. *IEEE Trans. Appl. Supercond.* **1**, 3–28 (1991).

[165] McCaughan, A. N. & Berggren, K. A superconducting-nanowire three-terminal electrothermal device. *Nano Lett.* **14**, 5748–5753 (2014).

[166] Franke, D., Clarke, J., Vandersypen, L. & Veldhorst, M. Rent’s rule and extensibility in quantum computing. *Microprocess. Microsyst.* **67**, 1 – 7 (2019).

[167] Reilly, D. J. Challenges in scaling up the control interface of a quantum computer (2019). URL https://arxiv.org/abs/1912.05114

[168] Opatovár, S. J. et al. A cryogenic CMOS chip for generating control signals for multiple qubits. *Nat. Elect.* **4**, 64–70 (2021).

[169] Xu, Y. et al. On-chip integration of Si/SiGe-based quantum dots and switched-capacitor circuits. *App. Phys. Lett.* **117**, 144002 (2020).

[170] Hasler, J. et al. Cryogenic floating-gate CMOS circuits for quantum control. *IEEE Trans. Quantum Eng.* **2**, 1–10 (2021).

[171] Ruffino, A. et al. Integrated multiplexed microwave readout of silicon quantum dots in a cryogenic CMOS chip (2021). URL https://arxiv.org/abs/2101.08295

[172] Charbon, E. et al. Cryo-CMOS for quantum computing. In *2016 IEEE International Electron Devices Meeting (IEDM)*, 13.5.1–13.5.4 (2016).

[173] Weinreb, S., Bardin, J. C. & Mani, H. Design of cryogenic SiGe low-noise amplifiers. *IEEE Trans. Microw. Theory Tech.* **55**, 2306–2312 (2007).

[174] Prabowo, B. et al. 13.3 A 6-to-8 Ghz 0.17 mw/qubit cryo-CMOS receiver for multiple spin qubit readout in 40 nm CMOS technology. In *2021 IEEE International Solid-State Circuits Conference - (ISSCC)*, **64**, 212–214 (2021).

[175] Ruffino, A. et al. 13.2 A fully-integrated 40-nm 5-6.5 Ghz cryo-CMOS system-on-chip with I/Q receiver and frequency synthesizer for scalable multiplexed readout of quantum dots. In *2021 IEEE International Solid-State Circuits Conference - (ISSCC)*, **64**, 210–
Bardin, J. C. et al. A 28 nm bulk-CMOS 4-to-8 GHz <2 mW cryogenic pulse modulator for scalable quantum computing. In 2019 IEEE International Solid-State Circuits Conference - (ISSCC), 456–458 (2019).

Patra, B. et al. A scalable cryo-CMOS 2-to-20 GHz digitally intensive controller for 4x32 frequency multiplexed spin qubits/transmons in 22 nm finFET technology for quantum computers. In 2020 IEEE International Solid-State Circuits Conference - (ISSCC), 304–306 (2020).

Van Dijk, J. P. G. et al. A Scalable Cryo-CMOS Controller for the Wideband Frequency-Multiplexed Control of Spin Qubits and Transmons. IEEE J. Solid-State Circ. 55, 2930–2946 (2020).

Xue, X. et al. CMOS-based cryogenic control of silicon quantum circuits. Nature 593, 205–210 (2021).

Park, J. S. et al. A fully integrated cryo-MOS SOC for qubit control in quantum computers capable of state manipulation, readout and high-speed gate pulsing of spin qubits in Intel 22 nm finFET technology. In 2021 IEEE International Solid-State Circuits Conference - (ISSCC), 208–210 (2021).

van Dijk, J. P. G. et al. Impact of classical control electronics on qubit fidelity. Phys. Rev. App. 12, 44054 (2019).

Lamb, I. D. C. et al. An FPGA-based instrumentation platform for use at deep cryogenic temperatures. Rev. Sci. Inst. 87, 14701 (2016).

Fu, X. et al. A microarchitecture for a superconducting quantum processor. IEEE Micro 38, 40–47 (2018).

Varsamopoulos, S., Bertels, K. & Almudever, C. G. Decoding surface code with a distributed neural network-based decoder. Quantum Machine Intelligence 2, 1–12 (2020).

Flentje, H. et al. Coherent long-distance displacement of individual electron spins. Nat. Commun. 8, 501 (2017).

Hermelin, S. et al. Electrons surfing on a sound wave as a platform for quantum optics with flying electrons. Nature 477, 435-438 (2011).

Borjans, F., Croot, X. G., Mi, X., Gullans, M. J. & Petta, J. R. Resonant microwave-mediated interactions between distant electron spins. Nature 577, 195–198 (2020).

Bertrand, B. et al. Fast spin information transfer between distant quantum dots using individual electrons. Nat.Nano. 11, 672-676 (2016).

Fujita, T., Baart, T. A., Reichl, C., Wegscheider, W. & Vandersypen, L. M. K. Coherent shuttle of electron-spin states. Npj Quantum Inf. 3, 22 (2017).

Mills, A. R. et al. Shuttling a single charge across a one-dimensional array of silicon quantum dots. Nat. Commun. 10, 1063 (2019).

Mortemousque, P.-A. et al. Enhanced spin coherence while displacing electron in a 2D array of quantum dots (2021). URL https://arxiv.org/abs/2101.05968

Jadot, J. et al. Distant spin entanglement via fast and coherent electron shuttling. Nat. Nano. 16, 570-575 (2021).
FIG. 1. Silicon QD devices. (a) Scanning electron microscope (SEM) image of an accumulation mode Si/SiGe heterostructure. Two layers of gates, bottom (light grey) and top (dark green) are designed to form two QDs (centre of image) and a single-electron transistor for readout (right). The structure contains a micromagnet in an upper metal layer (light green) to produce a magnetic field gradient. The green dot indicates the position of a QD used in ref. [16]. (b) Cross-sectional schematic of a Si/SiGe QD device. (c) SEM image of a metal-oxide-semiconductor multi QD device with QD gates (G1-4), confinement gate (CB), reservoir gate (RG), an integrated single-electron transistor (green) and microwave antenna for magnetic resonance spin control (blue) used in ref. [17]. (d) Cross-sectional view of the MOS QD device in (b). (e) SEM image of a CMOS p-type double QD on an etched silicon-on-insulator nanowire used in ref. [18] and schematic cross section (f). SEM (g) and TEM image (h) of a hole spin double QD device in a self-aligned double layer gate structure. L1(2) are 2 dimensional hole gas (2DHG) accumulation layers. G2, 3 are qubit control gates and G1 control the tunnel coupling [20].
FIG. 2. A quantum computing system. (a) Schematic representation of the main layers of a QCS. (b) A more detailed representation of a QCS including the interconnection between modules. The quantum-classical interface uses (de)multiplexers to facilitate input/output data management. These components could operate using time-domain and frequency-domain multiplexing. Control and readout micro- and radio-wave tones are produced by IQ modulation and amplification and readout signals are detected after amplification via IQ demodulation. The digital controller is used for fast feedback between the classical and quantum units, especially for hybrid quantum-classical algorithms and quantum error correction, and also to send the quantum computer instructions received from a classical computer. It interfaces with the rest of the layers via ADC/DACs.
FIG. 3. Two-dimensional arrays. (a) Graphical representation of a two-dimensional qubit array with nearest neighbour interactions necessary to implement the surface code. The hollow circles are data qubits and the black circles are error detection qubits, either X or Z syndrome, redrawn from [8]. Yellow and green ellipses represent two qubit interactions with the X- and Z- syndrome qubits, respectively. (b) Schematic representation of two ways of assigning data (grey) and syndrome qubits (dark grey) in a two-dimensional gate electrode array with tunable exchange gates (light grey). (Left) Standard 2x2 qubit sublattice (delimited by the red dashed line) requiring vertically integrated readout [49]. (Right) Extended 2x3 qubit sublattice (delimited by the blue dashed line) with two additional syndrome qubits to enable readout in the plane [21]. (c) Graphical representation of a digital image sensor formed by a two-dimensional array of photodiodes (pixels) combined with filters to detect specific wavelengths (RGB). (d) Schematic of a three-transistor active pixel sensor, including a reset transistor for the photodiode (RST), a source-follower readout transistor and a selection transistor addressed via row-column inputs. (e) Cross-section schematic of a single-electron MOS quantum dot with possible combinations of classical electronics. Left) Row-column access transistor for 2D addressing. Top) LC resonant circuit for dispersive readout where the MOS structure plays the role of variable capacitor. Right) Local amplification at the cell level.
FIG. 4. Challenges. Summary of the different challenges to scale silicon-based quantum computers using CMOS technology divided into the Quantum Layer, the Quantum-Classical Interface, the Classical Layer and the Architecture. The 2D modular and 3D integrated schematic architectures are from ref. [46] and ref. [21], respectively. The photograph of the FPGA, indicated in red, in the section Classical Layer is from ref. [142]. The simulation exemplifying device modelling is from ref. [138].