Readout system with on-board demodulation for CMB polarization experiments using coherent polarimeter arrays

Koji Ishidoshiro, Makoto Nagai, Takeo Higuchi, Masaya Hasegawa, Masashi Hazumi, Masahiro Ikeno, Osamu Tajima, Manobu Tanaka, Tomohisa Uchida

Abstract—B-modes are special patterns in cosmic microwave background (CMB) polarization. Degree-scale B-modes are smoking-gun signatures of primordial gravitational waves. The generic strategy of CMB polarization experiments is to employ a large number of polarimeters for improving the statistics. The Q/U Imaging ExperimenT-II (QUIET-II) has been proposed to detect B-modes by using the world's largest coherent polarimeter array (2,000 channels). A unique detection technique using QUIET's polarimeters, which comprises a modulation-demodulation scheme, enables us to directly extract polarization signals. The extracted signals are free from unpolarized components and intrinsic 1/f noise. We developed a data readout system for the QUIET-II experiment. We employed a “master” clock strategy, on-board demodulation functions, and end-to-end Ethernet connections for logical simplicity and high-density compact electronics for physical compactness. A clock module acts as a single master and guarantees phase matching between the modulation by the polarimeters and the on-board demodulation by ADC modules. Each ADC module has 64 ADC chips in the VME-6U single slot size. Both modules have hardware processors for Ethernet TCP/UDP. All these modules and control computers are connected via end-to-end Ethernet. Physical compactness and logical simplicity enable us to easily handle a large number of polarimeters, while maintaining quality of the B-mode experiments. The developed electronics (the clock modules and the ADC modules) fulfill these requirements. Tests with a setup similar to that of the real experiment proved that the system works appropriately. The performance of all system components is validated to be suitable for B-mode measurements.

Index Terms—Readout electronics, Cosmic microwave background, Demodulation, ADC

I. INTRODUCTION

DETECTION of primordial gravitational waves could provide a new and unique window on the very early universe [1]. Although various approaches for detecting them [2–4], the most promising approach is the measurement of B-modes, which are odd-parity patterns in cosmic microwave background (CMB) polarization. Because B-modes are very faint (< 100 nK), it is important to detect a large number of CMB photons for achieving sufficient sensitivity. The Q/U Imaging ExperimenT (QUIET) is a ground-based experiment that aims to detect the B-modes in the Atacama Desert in Chile, which is 5,080 m above sea level. At the initial phase of the QUIET experiment (QUIET-I), we observed CMB polarization in the 95 (43) GHz bands with 360 (72) channels of coherent polarimeter elements (polarimeter array). The obtained upper bounds for the B-modes are one of the most stringent limits to date; however, they are still limited by statistical errors [5]. An upgrade of the experiment (hereafter referred to as QUIET-II) has been proposed to achieve better sensitivity with a larger polarimeter array. Its primary goal is to detect B-modes at \( r \approx 0.01 \) by using 2,000 channels composed of 500 elements of four-output polarimeters, where \( r \) is the tensor-to-scalar ratio that indicates the intensity of the primordial gravitational waves [6].

We developed a readout system for the QUIET-II experiments. For handling the QUIET-II polarimeter array, we employed a master clock strategy, on-board demodulation functions, and end-to-end Ethernet connections for logical simplicity and developed high-density electronics to achieve physical compactness. The master clock strategy guarantees phase matching between modulation and demodulation. Since polarization signals are modulated to suppress polarization noise and unpolarized components, phase matching and demodulation functions are essential requirements for the system. The on-board demodulation has the advantage of reducing the load of data transfer. Furthermore, physical compactness is also important to attach the system on a telescope mount to avoid picking up unexpected noise on the cables between the polarimeter array and the readout system. In this paper, we describe the system design and prototype tests.

II. EXTRACTION OF THE POLARIZATION SIGNAL

A. QUIET polarimeter

A single QUIET polarimeter enables us to directly measure the Stokes \( Q \) and \( U \) parameters that characterize linear polarization. The polarimeters are polarization-sensitive coherent detectors using high electron-mobility transistor (HEMT) amplifiers, which have been widely used in CMB experiments [7–9]. They are suitable for detecting CMB polarization below 100 GHz. The polarimeter consists of a septum polarizer and strip-line-coupled monolithic microwave integrated circuit devices (Fig. 1). Input radiation is split into right and left circular polarizations \( (E_R \text{ and } E_L) \), respectively) by the spectrum polarizer. In the devices, the two polarization signals are modulated and coupled and then the power of the coupled signals is converted to analog outputs. In the polarimeter outputs, the Stokes parameters appear as the modulation components.
The QUIET collaboration developed a polarimeter-on-a-chip, which replaces waveguide-block components with the devices [10]. The resulting package has a footprint size of 2.5 cm × 2.5 cm (95 GHz band) and 5 cm × 5 cm (43 GHz band) in QUIET-I. This breakthrough technology enabled us to build a large polarimeter array.

B. Modulation/demodulation scheme

An HEMT amplifier is known to have a 1/f noise whose knee frequency is high approximately 1 kHz. A modulation/demodulation scheme is employed to extract the polarization signal without any contamination from the 1/f noise and unpolarized components [10]. The block diagram of the modulation is shown in Fig. 1. The input $E_R$ and $E_L$ to the devices are amplified by HEMTs. Then, the amplified polarizations are modulated by phase switches, each of which has two microwave paths. Path selection is controlled by p-intrinsic-n diodes. The difference among these path lengths corresponds to a half-wavelength of the measured CMB. The phase switch varies the phase of the CMB signal by 180°, which simply flips the sign of the CMB signal, and there is no sign flip for noises. Applying carrier clocks to the diodes offers periodic phase (sign) modulation. The two amplified and modulated polarizations are recombined by couplers. Four voltage-biased square-law Schottky diodes detect the power of the coupled signals.

Suppose we implement the modulation only for one side, e.g., $E_R$, then the polarimeter outputs (or diode receiving power) can be expressed as follows (see Appendix):

$$D(t) = c_1(t)P + c_1(t)^2R + |c_1(t)|^2N_1(t),$$

(1)

where $P$ is proportional to $g_1g_2Q$, $-g_1g_2Q$, $g_1g_2U$, and $-g_1g_2U$ for each diode, $R$ corresponds to the power of the right circular polarization, i.e., $(g_1^2E_R^2)$. $N_1(t)$ is the intrinsic noise of the HEMT amplifier on the side of $E_R$. $g_1$ and $g_2$ are gains of the HEMT amplifier, and $c_1(t)$ is the primary modulation term. We can set $c_1(t_{2p}) = +1$ and $c_1(t_{2p+1}) = -1$ in case of ideal modulation. Here, $p$ is the normalized time index with a half period of $c_1(t)$ and $D(t_P)$ is the averaged value during the $p^{th}$ half period. Polarization $P$ can be extracted from the difference of each state, i.e., $\Delta D = D(t_{2i}) - D(t_{2i+1})$. In Eq. (1), we drop the terms that are related to the noise from another HEMT amplifier.

The modulation by the real polarimeter is not perfect, e.g., $c_1(t_{2p}) = +1$ and $c_1(t_{2p+1}) = -(1 - c_1)$, where $c_1$ is a small nonzero value. As a result, residual terms that are related to the $R$ and $N_1(t)$ appear. These residuals can be eliminated by the secondary modulation for another side [11]. With the secondary modulation for $E_L$, the polarimeter output can be described as follows:

$$D(t) = c_1(t)c_2(t)P + c_1(t)^2R + c_2(t)^2L + |c_1(t)|^2N_1(t) + |c_2(t)|^2N_2(t),$$

(2)

where $L$ and $N_2$ indicate the power of the left circular polarization ($\propto g_2^2E_L^2$) and the intrinsic noise on the side of $E_L$, respectively. Here, $c_2(t)$ is similar to $c_1(t)$, i.e., $c_2(t_{2q}) = +1$ and $c_1(t_{2q+1}) = -(1 - \epsilon_2)$, where $\epsilon_2$ is a small nonzero value that indicates imperfection of the second modulation and $q$ is the normalized time index with the half period of the second modulation. This time period is longer than that of the primary modulation. Only the first term in Eq. (2) has the phase information of both modulations. Therefore, the series of difference allows us to extract the polarization ($P$) without any contamination. This scheme is called demodulation. We implement this function in the readout system.

III. SYSTEM DESIGN

A. System structure

The system structure is shown in Fig. 2. The logical simplicity of our structure is possible because of the master clock strategy, on-board demodulation functions, and end-to-end Ethernet connections. Clocks acts as carriers to indicate phase states for the modulation. They should be in-phase between the polarimeter and the readout system. To retain phase matching, we employ clock modules that work as a single “master.” The clock modules generate well-matched carrier clocks and distribute them to the polarimeter array and analog-to-digital converter (ADC) modules. Each ADC module performs digitization and on-board demodulation for 64 channels. Having a sub-board in addition to a main board, a single ADC module houses 64 ADC chips (32 chips each on the main board and the sub-board) in a versal module eurocard (VME) 6U single slot size (Fig. 3). All circuits for the ADC chip control and on-board demodulation are implemented in a single field programmable gate array (FPGA). Such high-density and compact modules are suitable for attaching to the telescope mount, which is a basic scheme to suppress the noise picked up on the cable between the polarimeters and the ADC modules.

The demodulated data in the ADC modules are transmitted to a readout computer via Ethernet transmission control protocol (TCP) [12]. To control both modules from the computer, user datagram protocol (UDP) is also used. TCP and UDP in both modules are implemented by a hardware-based processor called SiTCP [13]. Although to handle TCP and UDP, an additional FPGA or CPU is usually required, we do not need them because of the advantages of SiTCP.
B. Specifications of the ADC chip

Analog-to-digital (A/D) conversion is synchronized with an A/D clock. Its sampling rate \( f_{A/D} \) is determined to avoid ringing spikes during the phase flip. The ringing spikes appear for 15–20 \( \mu \)sec. We can avoid the effects of the spikes by masking these periods. To optimize the masking region with a precision better than 10\%, \( f_{A/D} > 666 \) kHz is required.

The system should be able to measure signals ranging from the CMB temperature (2.7 K) to room temperature (300 K). Suppose the responsivity of the polarimeter is \( \approx 10 \) mV/K, which is the highest among QUIET-I polarimeters, then the ADC dynamic range \( V_d \) should be at least \( V_d > 3,000 \) mV.

The noise level of the QUIET-II polarimeter is expected to be \( \approx 10^{-3} \) mV/Hz\(^{1/2}\), assuming a sensitivity of 500 \( \mu \)K/\( \sqrt{\text{channel}} \) (250 \( \mu \)K/\( \sqrt{\text{polimeter}} \)). Considering the individual differences among the polarimeters, the lowest noise level may be \( \approx 3 \times 10^{-4} \) mV/Hz\(^{1/2}\). With a safety factor of 10, we have to determine the ADC resolution \( R \) to fulfill the following equation:

\[
\frac{\Delta A/D}{\sqrt{6f_{A/D}}} \text{ mV/Hz}^{1/2} < 3 \times 10^{-5} \text{ mV/Hz}^{1/2}, \tag{3}
\]

where \( \Delta A/D \) is the least significant bit defined as \( \Delta A/D = V_d/2^R \). The left-hand side of Eq. (3) is the ADC quantization noise estimated from the root mean square of the quantization noise \( (\Delta A/D/\sqrt{12}) \) divided by the square of the band width \( f_{A/D} \) and the amplification of it by \( \sqrt{2} \) to obtain a one-sided spectrum.

For the ADC chip parameters, the allowed region based on the above requirements under the condition \( V_d = 4,096 \) mV is shown in Fig. 4. We use a commercial ADC chip, AD7674 [14], that has an 18 bit resolution with \( f_{A/D} = 800 \) kHz and \( V_d = 4,096 \) mV. For the ADC chip control as well as the on-board demodulation, we use a system clock with \( f_{sys} = 40 \) MHz.

This frequency is selected such that it is sufficiently high to operate the ADC chips in the serial interface mode but sufficiently low to allow easy handling. In principle, a slower system clock is possible when we select the parallel interface mode. However, such an interface requires more electronic circuitry and a larger FPGA on board, which is contrary to the objectives of designing a high-density compact module.

C. Modulation/demodulation frequencies and data recording rate

The demodulated data can be downsampled at the data recording rate \( f_{\text{record}} \) without any loss of CMB information. This rate determines the sampling of the sky. The mount for the QUIET-II experiment is desired whose scan speed \( \theta_{\text{scan}} \) is \( 6^\circ/\text{s} \) at the maximum with a full width at half maximum (FWHM) of 0.1° for the angular resolution \( (\Delta \theta) \). The relationship \( 2 \times \theta_{\text{scan}} \times 1/f_{\text{record}} < \Delta \theta \) should be satisfied, where a factor of two is introduced by the sampling theorem. This relationship requires \( f_{\text{record}} > 120 \) Hz. Under this condition, we should also consider avoidance of the aliasing effect of AC power frequency and its harmonics.

Two types of carrier clocks are sent to both polarimeters and ADC modules. The frequency of the primary carrier \( f_{c1} \) must be higher than the knee frequency of the \( 1/f \) noise, which mainly occurs from the HEMT amplifier of the polarimeter. Its typical knee frequency is \( \approx 1 \) kHz. To minimize the occurrence of ringing spikes, we minimize \( f_{c1} \). Therefore, \( f_{c1} = 4 \) kHz is the natural selection.

The frequency of the secondary carrier \( f_{c2} \) should be downscaled to the frequency of \( f_{c1} \) by an even number, 

\[
f_{c2} = \frac{f_{c1}}{2n} \quad (n \text{ is an integer number}). \tag{4}
\]
This frequency is possibly lower than the knee frequency of the $1/f$ noise. The lower bound of $f_{c2}$ is $f_{\text{record}}$ and we choose $f_{c2} = f_{\text{record}} = 125$ Hz.

We summarize the specifications of the clocks in Table I.

### IV. Clock Module

We developed 19 inch 2U size clock modules (Fig. 5). A single module has seven RJ45 slots on the front panel and 21 flat cable (20 pins) connector slots on the surface of the board. The rightmost RJ45 slot is used for communication with the computer via TCP/UDP. All other input/output signals are at the level of LVDS. Furthermore, all functions are controlled by FPGA (XC6SLX75) in the module. Its firmware is stored in an electrically erasable programmable read-only memory (AT93C46).

The module logic consists of two parts: a “reference selector” and a “clock generator” as shown in Fig. 6. The selector performs the function of selecting a reference clock. The clock generator has two functions: generating the clocks on the basis of the reference clock and transmitting them to the ADC modules as well as the polarimeters. Because of space limitations for the clock distribution slots, we use two clock modules to handle 2,000 channels: master and slave. The internal quartz crystal resonator produces the clocks as listed in Table I. The carrier clocks are distributed from the RJ45 slot to another board to control the carrier bias level of the polarimeters. The last RJ45 input slot is reserved to test the timing of TCP/UDP. A single flat cable is used for delivering the clocks to the single ADC module. Two clock modules (the master and slave) can deliver the clocks to the 42 ADC modules (which have a combined capability of handling 2,688 channels). The phase differences among the delivered carrier clocks were confirmed to be at most 2.4 nsec. This is also a sufficient performance compared with the ADC sampling interval of 1.25 μsec ($=1/f_{\text{record}}$).

### V. ADC Module

The ADC module has a VME-6U single slot size (Fig. 3). A single module consists of a main board and a sub-board. Each board has 32 ADC chips (AD7674) with 32 buffer amplifiers (AD8028) and a Dsub78 connector for 32 pairs of differential inputs with eight analog grounds. By using the sub-board, we successfully doubled the number of ADC chips compared with that in the previous generation ADC modules [15], [16]. A single module has the capability of handling 64 channels in total by using a single FPGA (XC6SLX150) on the main board. We plan to use 32 modules to handle 2,000 inputs from the polarimeters.

Each module works at +5 V and 3 A, i.e., 15 W. A VME crate supplies the power to the ADC modules. All clocks are provided from the clock module via VME P2 user-defined clock in the module. The internal quartz crystal resonator (KC7050C40.0000C3WE0) in the module also generates a 40 MHz clock. The reference selector chooses the master clock from these two options. The internal clock is useful for laboratory testing when a GPS clock is not used. The master clock is duplicated and these two clocks are output via two RJ45 slots. We found that the phase delay between them is 0.8 nsec, which is a suitable specification for the 40 MHz (25 nsec period) system clock.

Each module has an RJ45 slot to receive the reference clock. The use of the same cable length as that of the reference output slots in the master clock guarantees the same phase delay for the two reference clocks. In each module, the clock generator produces the clocks as listed in Table I. The carrier clocks are distributed from the RJ45 slot to another board to control the carrier bias level of the polarimeters. The last RJ45 input slot is reserved to test the timing of TCP/UDP. A single flat cable is used for delivering the clocks to the single ADC module. Two clock modules (the master and slave) can deliver the clocks to the 42 ADC modules (which have a combined capability of handling 2,688 channels). The phase differences among the delivered carrier clocks were confirmed to be at most 2.4 nsec. This is also a sufficient performance compared with the ADC sampling interval of 1.25 μsec ($=1/f_{\text{record}}$).

| Table I: Frequencies of clocks used in the system. |
|----------------------------------|----------------|
| Clock                        | Frequency   |
| System clock ($f_{\text{sys}}$) | 40 MHz      |
| A/D clock ($f_{A/D}$)          | 800 kHz     |
| Primary carrier ($f_c$)        | 4 kHz       |
| Secondary carrier ($f_{c2}$)   | 125 Hz      |
| Recording rate ($f_{\text{record}}$) | 125 Hz |

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### Fig. 6. Functional diagram of the clock module. The master and slave are identical modules. The reference selector is only used in the master module. All functions are implemented in a single FPGA.
pins with a digital ground. The digital and analog grounds are connected via a zero-ohm connection at one location. An electrically erasable programmable read-only memory (AT93C46) records the IP address for the TCP/UDP communication. The FPGA firmware is stored in a serial flash memory (M25P64-VMF).

A. Firmware logic

The polarimeter output includes ringing spikes induced by the phase flip, which must be masked. The top of Fig. 7 shows a schematic example of the digitized polarimeter output stream \( D(t_i) \) with the ringing spikes, where \( i \) is the time index of the digitization rate \( (f_{\text{A/D}} = 800 \text{ kHz}) \). Digitized ringing spikes are masked by multiplying a masking function \( m(t_i) \) which has the value 0 when "mask" = true and 1 when "mask" = false (see an example in Fig. 7). For studying the ringing spikes, 64 raw digitized streams can be recorded during 300 \( \mu \text{sec} \), which is limited by the size of the internal memory of the FPGA. We nominally mask one sample before and 13 samples after the phase change. The duration of the mask can be redefined via UDP by using the external computer.

The demodulator in the ADC module extracts the polarization signal from the masked stream \( m(t_i)D(t_i) \) as follows:

\[
F_{\text{demod}}(t_i) \equiv s^I_k(t_i)s^Q_k(t_i)m(t_i)D(t_i),
\]

where

\[
s^I_k(t_i) = \begin{cases} +1 & \text{if } 0 \leq t_i < T_k/2 \\ -1 & \text{if } T_k/2 \leq t_i < T_k \end{cases}
\]

(6)

\[
s^Q_k(t_i) = \begin{cases} s^I_k(t_i + nT_k), & \text{if } k = 1, 2, T_k = 1/f_{ck} \text{ and } n \text{ is an integer. Here, } s^I_k(t_i) \text{ is in-phase with the carrier } c_k(t_i). \text{ Summation is performed for all } 6,400 \text{ points to form a } 125 \text{ Hz } \text{“Demod” stream:}
\end{cases}
\]

\[
\text{Demod} \equiv \sum F_{\text{demod}}(t_i).
\]

The extracted Demod stream is proportional to the Stokes \( Q \) or \( U \) parameters. Demodulation eliminates the \( 1/f \) noise below \( f_{\text{c1}} \).

In case of quadratic phase demodulation (Quad), the Stokes \( Q \) or \( U \) parameters are also suppressed:

\[
\text{Quad} \equiv \sum s^Q_k(t_i)s^Q_k(t_i)m(t_i)D(t_i),
\]

where

\[
s^Q_k(t_i) = \begin{cases} +1 & \text{if } 0 \leq t_i < T_1/4 \\ -1 & \text{if } T_1/4 \leq t_i < 3T_1/4 \\ +1 & \text{if } 3T_1/4 \leq t_i < T_1 \end{cases}
\]

(11)

\[
s^Q_k(t_i) = \begin{cases} s^Q_k(t_i + nT_1). & \text{if } k = 1, 2 \end{cases}
\]

(12)

(13)

(14)

It is useful to monitor the Quad stream, because it only contains the noise whose level is the same as in the Demod stream.

A simple summation without demodulation is used to extract the total power (TP) corresponding to the Stokes parameter \( I(\propto R + L) \):

\[
\text{TP} \equiv \sum m(t_i)D(t_i),
\]

in which the intrinsic noise terms \( (N_1 \text{ and } N_2) \) are neglected.

The demodulator is implemented in the FPGA for each input (Fig. 5). Using a pseudo-polarization signal input, we confirmed that the demodulator works appropriately, as shown in Fig. 9. The injected signal consists of a sinusoidal polarization signal (600 mV peak-to-peak amplitude at 5 mHz) and an offset that drifts at 400–500 mV.

B. Intrinsic noise

We measure the intrinsic noise with a 50 \( \Omega \) termination for each input. Figure 10 shows the noise spectra in one of the channels. The \( 1/f \) components, which are obtained from the buffer amplifier, in the TP spectrum are completely suppressed in both Demod and Quad spectra. The expected knee frequency of the polarimeter \( 1/f \) noise is approximately 1 kHz [10]. Thus, \( 1/f \) noise suppression is well guaranteed.
Fig. 9. Demod, Quad and TP streams with a pseudo-polarization signal input. The signal is appropriately extracted in each stream. The input polarization is a sinusoidal wave. The baseline drift as shown in the TP stream is completely suppressed in the Demod and Quad streams.

Fig. 10. Noise spectra of TP, Demod and Quad with a 50 Ω termination for the input. The components of the 1/f noise are completely suppressed in the Demod and Quad spectra. The white noise levels of the Demod and Quad spectra are $2 \times 10^{-5}$ mV/Hz$^{1/2}$, which fulfills the requirement.

The measured noise floor in the Demod spectrum for each channel is shown in Fig. 11. We confirmed that the noise level is better than the requirements given in Sec. III-B.

C. Linearity

A linear response with respect to the input voltage level is required for the experiments. The top panel of Fig. 12 shows a typical response as a function of the input voltages. Responsivity as a function of the input voltages is also shown in the bottom panel of Fig. 12. Within the $-1,900$ to $1,900$ mV input range, we did not find any non linearity effects above $7 \times 10^{-3}$ (We nominally use the $-1,900$ to $1,900$ mV range.). The averaged responsivity within the above range and non linearity as a function of channels are shown in the middle panels of Fig. 11. Here, non linearity is defined as the difference between the maximum and minimum responsivities in the $-1,900$ to $1,900$ mV range. We discovered slight non-uniformity among channels, i.e., $2 \times 10^{-3}$, in the standard deviations of averaged responsivity. Non linearity and non uniformity are lower than $10^{-2}$, which is the requirement to reduce a mimic $B$-mode intensity at $r = 10^{-5}$.

The requirement is determined when we do not have any calibration for the non linearity. We measure the Stokes parameters $Q$ and $U$ with different channels. The polarization angle on the sky ($\phi$) is reconstructed with the measured responses for Stokes $Q$ and $U$.

$$\phi = \frac{1}{2} \tan^{-1} \left( \frac{a_U U}{a_Q Q} \right),$$

where $a_Q$ and $a_U$ are the channel responsivities to measure $Q$ and $U$ at a given input power, respectively. The non linearities of $Q$ and $U$ and their non uniformity ($a_U \neq a_Q$) shifts the measured angle from the real value. Such an angle shift $\Delta \phi$ creates mimic $B$-modes [17]:

$$C^B_{\ell} = C^E_{\ell} \sin^2(2\Delta \phi),$$

where $C^E_{\ell}$ is the $E$-mode power spectrum at the given angular wave-number $\ell$. We confirmed that the magnitude of non linearity and the sign and magnitude of the non uniformity of the responsivities are random, as shown in the middle panels of Fig. 11. Therefore, the mimic $B$-modes are smeared with the square of the number of channels (2,000 channels). To determine the $B$-modes at $r = 10^{-5}$ without any calibration for ADC responsivity, non linearity and non uniformity should be less than $10^{-2}$.
A single ADC module generates 768 byte (4 byte \(\times\) 3 streams \(\times\) 64 ADC chips) of demodulated data with the rate \(f_{\text{record}} = 125\) Hz. Sixteen bytes of header information are added for each sample. The aggregate flow rate with the 32 ADC modules is 25 Mbps.

A 4 byte time counter is a component of the header. The counter is incremented by the edges of the 125 Hz carrier clock and it can be reset by a reset pulse. The pulse is controlled by the clock module. In the real observation, a pulse is sent at the beginning of continuous data taking. The typical duration of the data taking is approximately 1.5 hours. From the value of the time counter and the reset time calibrated with a GPS, we can find the time at which each data is demodulated.

We tested timing synchronization among the components by applying a 25 Mbps load to a prototype system. We constructed the system with one master clock module and four ADC modules, one readout computer, and another computer as a “dummy ADC module” (Fig. 13). They were physically connected via one Ethernet switch (D-Link, DES-1050G). The dummy ADC module sent 22 Mbps of dummy ADC data to the control computer using 28 different ports. Its data rate corresponds to that of the 28 ADC modules. In this setup, the situation in QUIET-II is effectively reproduced in terms of the data transfer and the system organization scheme relationship. Therefore, we virtually constructed the readout system for the QUIET-II experiment.

We took data continuously for 16 hours with periodic (0.1 Hz) pulse signal injections into the ADC modules. We did not find any data loss or inconsistency among the time counters in the data. In addition, we confirmed timing synchronization among the ADC modules from the edge of the injected signals. Synchronization among the modules is confirmed with the edge of the injected signals.

B. Measurement of polarization with a polarimeter

By using a prototype polarimeter [18], we examined the functions of the readout system, i.e., the mask for the ringing spikes and the extraction of the polarization signal. To study the mask, we analyzed the raw digitized data during 300 \(\mu\)sec
level shifts due to the offset power variation were expected. The power (unpolarized radiation) also varied periodically with the angle when the polarimeter was rotated by a frequency of about 0.1 Hz. The offset of polarization irradiated to the polarimeter, the polarization system, E. (19) were generated by the calibration system [19]. We observed the expected patterns in each stream. We also thank Fermi National Accelerator Laboratory for providing us with the ADC module design for the QUIET-I experiment. Special thanks to Professor Bruce Winstein who strongly encouraged our development of the system. We also acknowledge Jet Propulsion Laboratory and California Institute of Technology for providing the QUIET-II polarimeter. We also thank Fermi National Accelerator Laboratory for providing several electronics to control the polarimeter. We wish to thank Open Source Consortium of Instrumentation...
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