A Scalable and Energy Efficient GPU Thread Map for \(m\)-Simplex Domains

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Abstract

This work proposes a new GPU thread map for \(m\)-simplex domains that improves its speedup along with the \(m\)-dimension and is energy efficient compared to other state of the art approaches. The main contributions of this work are i) the formulation of an improved new block-space map \(\mathcal{H} : \mathbb{Z}^m \mapsto \mathbb{Z}^m\) for regular orthogonal simplex domains, which is analyzed in terms of resource usage, and ii) the experimental evaluation in terms of speedup and energy efficiency with respect to a bounding box approach. Results from the analysis show that \(\mathcal{H}\) has a potential speedup of up to \(2x\) and \(6x\) for 2 and 3-simplices, respectively. Experimental evaluation shows that \(\mathcal{H}\) is competitive for 2-simplices, reaching \(1.2x \sim 2.0x\) of speedup for different tests, which is on par with the fastest state of the art approaches. For 3-simplices \(\mathcal{H}\) reaches up to \(1.3x \sim 6.0x\) of speedup making it the fastest. The extension of \(\mathcal{H}\) to higher dimensional \(m\)-simplices is feasible and has a potential speedup that scales as \(m!\) given a proper selection of parameters \(r, \beta\) which are the scaling and replication factors of the geometry, respectively. In terms of energy consumption, although \(\mathcal{H}\) is among the highest in power consumption, it compensates by its short duration, making it one of the most energy efficient approaches. Lastly, further improvements with Tensor and Ray Tracing Cores are analyzed, giving insights to leverage each one of them. The results obtained in this work show that \(\mathcal{H}\) is a scalable and energy efficient map that can contribute to the efficiency of GPU applications when they need to process \(m\)-simplex domains, such as Cellular Automata or PDE simulations.

Keywords: GPU Computing, Thread Mapping, Scalable, Simplex Domains, Energy Efficiency, GPU Resource Usage

1. Introduction

GPU computing has become a well established research field in the last years \(^1\) thanks to the increasing performance of GPU hardware and the existence of a general purpose programming model, being CUDA \(^2\) and OpenCL \(^3\) the most known implementations of such model. Notorious advancements have been made to better understand how data-parallel algorithms can be more efficient on the GPU architecture. Some of these advancements include the improvement of thread access patterns for coalesced memory access \(^4\), reduction of thread branching \(^5\), better use of the \(L_1\) programmable cache \(^6\), fast stencil computations \(^7\), efficient reduction algorithms \(^8\), multi-GPU acceleration \(^9\) and most recently the mapping of different computational patterns to tensor cores \(^10\) as well as ray tracing cores \(^11\). One performance aspect of GPU computing that is also being researched in the last years is the study and design of efficient GPU thread maps for data-parallel domains with complex geometries \(^12\). Several problems exhibit a non-boxed shape data domain in which data-parallel GPU computation must be mapped. Examples of such problems are regular orthogonal \(m\)-simplex domains, which exist when working with half-triangular matrices, or when doing a cellular automata simulation on a discrete voxel-based tetrahedron. A regular orthogonal \(m\)-simplex is an \(m\)-dimensional polytope, where its facets are equal, define a convex hull and one of its vertices has all of its incident facets orthogonal one to each other. The discrete voxelized/cell-like version, denoted \(\Delta^m\), is of interest in data-parallel computations and is composed of unitary volumetric elements with location \(x = \{x_1, x_2, \ldots, x_m\}\) that satisfy

\[
\Delta^m_t \equiv \{ x \in \mathbb{Z}_t^m | 0 \leq x_i \leq n \land x_1 + x_2 + \ldots + x_m \leq n \}
\]  

where the absolute Manhattan distance from any element \(x\) to the orthogonal corner of the \(m\)-simplex cannot be greater than \(n\). Mapping GPU threads efficiently to a regular orthogonal \(m\)-simplex is not straightforward in the GPU programming model, because it was designed for box-shaped domains.

This work proposes a new map \(\mathcal{H} : \mathbb{Z}^m \mapsto \mathbb{Z}^m\) for mapping GPU threads onto regular orthogonal \(m\)-simplex domains efficiently. The map assigns thread-blocks in parallel space to unique locations in the \(m\)-simplex shaped data, using \(O(1)\) arithmetic operations. A dedicated analysis is devoted to the special cases of 2-simplex and 3-simplex domains, where new efficient maps are proposed and described, based on a binary self-similar organization of sub-orthotopes. The approach can offer a parallel space improvement of \(\sim 2x\) and \(\sim 6x\) for \(m = 2\) and \(m = 3\), respectively, that results in a potential performance improvement given that the maps costs \(O(1)\) arithmetic operations and no \(m\)-th roots are required. Experimental results support

\(^1\)For simplicity, sentences using just the term simplex/simplex will also refer to the regular orthogonal ones.
the theoretical bounds, showing that $\mathcal{H}$ is competitive in 2-
simplices, the fastest one in 3-simplices, and energy efficient.
For the higher dimensional case, an analysis shows that build-
ing an efficient set of self-similar orthotopes is possible with a
potential speedup of $m!$, given optimal values are found for the
scaling and replication factors, $r$ and $\beta$ respectively.

This work improves from a previous conference publication
[23] by including an improved formulation and a full experi-
mental evaluation using more comparison approaches, ad-
ditional tests and several GPUs. Also, it extends the previous
work by including a complete evaluation of energy efficiency
for all approaches, as well as new insights for leveraging Ten-
or and Ray Tracing cores in modern GPU architectures.

2. The Problem of Mapping GPU Threads onto Simplices

The GPU programming model offers four constructs\footnote{This work uses CUDA’s naming scheme. OpenCL names are (1) work-
element, (2) work-group and (3) work-space, respectively.} that allow the execution of highly parallel algorithms: (1) thread, (2)
block, (3) grid and (4) kernel. Threads are the smallest work ele-
ments and they are in charge of executing the instructions of a
GPU kernel, which is the main parallel program written by the
programmer. A block is an intermediate structure that contains
a set of threads organized as an Euclidean box. Blocks provide
fast shared memory access as well as local synchronization for
all of its threads. The grid is the largest construct of all three
and it keeps all blocks together spatially organized for the ex-
ecution of a GPU kernel. These three constructs are illustrated in
Figure 1 and play an important role when mapping process-
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in Figure 1 and play an important role when mapping process-

For every GPU computation there is a stage where threads,
which live in grid space, get mapped to different locations in
data space. This mapping is defined as

$$ f(x) : \mathbb{Z}^k \rightarrow \mathbb{Z}^m $$  

where $k$-dimensional locations $x = (x_1, x_2, ..., x_k)$, in grid space,
map to $m$-dimensional locations $y = (y_1, y_2, \cdots, y_m)$ in data
space, typically as an injective or bijective function. GPU para-
allel spaces can be formally described as orthotopes $\Pi^m_k$ in $m
= 1, 2, 3$ dimensions that contain discrete elements organized in

blocks. Each element corresponds to a thread that must be as-
signed to the data domain.

A known approach for mapping threads in GPUs is to build a
bounding-box (BB) of volume $f(1 \times l_1 \times l_2 \cdots l_k)$ where $l_i$
is the length of the data space in the $i$-th dimension. Without loss
of generality, we can assume a regular geometry to express the
bounding box volume as $n^l$ where $n$ is the needed length to
cover the entire data domain in all dimensions. Using the map

$$ f(x) = x $$  

one can obtain the corresponding location of every thread in
data space. Such map is highly convenient, simple and efficient
for the class of problems where the data space is an orthotope as
well, such as vectors, tables, images, matrices or other arbitrary
box-shaped data domains. However, this approach is no longer
convenient neither efficient once data domains start taking other
shapes.

There is a class of highly parallelizable problems where
data organizes in the form of a regular simplex. Computations
such as the Euclidean distance matrix (EDM) [26, 27, 28], col-
cision detection [29], adjacency matrices [30], cellular automata
simulation on triangular domains [31], matrix inversion [32] and
even the $n$-body problem [33, 34, 35], among others, follow
the shape of a regular orthogonal 2-simplex. Here, such simplex
is denoted as $\Delta^2_n$, with $n$ its length along one dimension, and its
working space is $V(\Delta^2_n) = n(n + 1)/2 \in O(n^2)$. The problem
is that for this class of problems the default bounding-box (BB)
GPU mapping approach turns out to be inefficient because the
orthotope of parallel space, denoted $\Pi^2_k$, produces $n^2$ threads,
where $n(n - 1)/2 \in O(n^2)$ are unused, as shown in Figure 2.

![Figure 2: The bounding-box approach almost doubles the number of threads.](image)

The problem is not restricted just to two-dimensional cases.
Simulation applications that act on voxelized or cell-like regu-
lar tetrahedrons, such as PDEs or Cellular Automata, also em-
ploy a 3-simplex. In the 3-simplex class, the interaction space
is $V(\Delta^3_n) = n(n + 1)/6 \in O(n^3)$ elements, organized as
a discrete regular orthogonal tetrahedron. Once again, the def-
ault bounding-box (BB) approach turns out to be inefficient as
it generates a parallel space $V(\Pi^3_k)$ with $O(n^3)$ unnecessary
threads (see Figure 3).

The issues recently described are two specific cases of the
problem of mapping an $m$-orthotope to a regular orthogonal
$m$-simplex, while matching their volumes at least asymptotically.
Figure 4 illustrates the geometry of discrete orthogonal sim-
plices for $m = 1, 2, 3$.

\footnote{CUDA offers up to $k = 3$. Higher dimensional orthotopes can be still be represented by linearizing down to 3-dimensions.}
where an induction \([36]\) can prove its formula, based on the fact
that the volume of an \(m\)-simplex is the sum of the volumes of \(n\) stacked
\(m\)-simplices of lengths \(1, 2, 3, \ldots, n\), i.e.,
\[
V(\Delta_{n+1}^m) = \sum_{i=1}^{n} V(\Delta_i^m)
\]
and when combined with the properties of sums of binomial
coefficients, leads to formula \((4)\).

The parallel space efficiency challenge arises when trying to
process an \(m\)-simplex domain with GPU computing, as its
parallel programming model can only manage orthotopes of
threads, namely \(\Pi_n^m\), and not arbitrary shapes as simplices. Al-
though the bounding-box approach will work and is simple to
implement, its main problem is that in the limit \(n \to \infty\), the
fraction of extra parallel space of \(V(\Pi_n^m)\) that lies outside of the
\(m\)-simplex approaches to
\[
\alpha(\Pi, \Delta_n^m) = \lim_{n \to \infty} \frac{V(\Pi_n^m)}{V(\Delta_n^m)} - 1 = m! - 1
\]
thus being inefficient in terms of parallel space as all the ex-
tra thread-blocks must be discarded at run-time through con-
tingual or arithmetic filters. The implication is a performance
penalty at the mapping stage of any kernel execution. More-
over, these extra thread-blocks can produce a negative impact
on the performance of multiple concurrent kernels as they could
make use of hardware resources that could be potentially avail-
able to other kernels.

One solution, used in the past years, is to enumerate all
threads or thread-blocks of a given orthotope in sequence, and
then use this enumeration as an indexing scheme. Such an-
approach allows to formulate a map \([22, 23, 24]\) of the form \(\lambda : \mathbb{Z}^1 \to \mathbb{Z}^m\) with \(V(\Pi_n^m) = O(V(\Delta_n^m))\). Although \(\lambda\) can be com-
putable by elementary and arithmetic functions, it also requires
the computation of \(m\)-th order roots as part of the solution of an
\(m\)-th order equation, which limits the range of problem size \(n\)
due to potential numerical error in the mapping of thread coor-
dinates. Moreover, the method is restricted to \(m \leq 4\) as no gen-
eral analytical solutions are available for polynomials of \(m > 4\).
Finding a different kind of map, free of these problems, would
improve the state of the art regarding GPU thread maps for sim-
plex domains.

The limitations described can be overcome, in great part,
by taking advantage of the dimensionality available in the par-
allel space, which was an aspect not exploited by the enumera-
tion principle proposed in the past \([24]\). Although parallel GPU
spaces cannot have a geometry different from an orthotope, they
still are topologically equivalent to an \(m\)-simplex and a self-
similar set can match the desired domain. Therefore, finding an
homeomorphism of the form \(\mathcal{H} : \mathbb{Z}^m \to \mathbb{Z}^m\) would produce a
map, efficient in parallel space and with zero dimensional dis-
tance which would free it from the computation of expensive
\(m\)-th roots.

3. Related Work

One of the earliest works in mapping the GPU efficiently
onto a 2-simplex is by Jung et. al. \([37]\) in 2008, whom pro-
posed a rectangular box strategy (RB) for accessing and storing
a triangular matrix (upper or lower) more efficiently on GPU.
Data structures become practically half the size with respect to
classical methods based on the full matrix. The strategy was
originally intended to modify the data space (i.e., the matrix),
however one can apply the same concept to the thread space.
One disadvantage of RB is that it only works on 2-simplices,
i.e., applying the idea at higher dimensions produces unneces-
sary threads.

Ries et. al. contributed with a parallel GPU method for the
triangular matrix inversion \([32]\). The authors identified that the
parallel space indeed can be improved by using a recursive par-
tition (REC) of the grid, based on a divide and conquer strategy.
The approach takes \(O(\log_3(n))\) time by doing a balanced parti-
tion of the structure, from the orthogonal point to the diagonal.
Q. Avril et. al. proposed a GPU mapping function for collision
detection based on the properties a upper-triangular map \([29]\). The map is a thread-space function \(u(x) \to (a,b)\),
where \(x\) is the linear index of a thread \(t_x\) and the pair \((a,b)\) is a
unique two-dimensional coordinate in the upper triangular ma-
trix. Since the map works in thread space, the map is accurate
only in the range \(n \in [0, 3000]\) for a simplex of side length \(n\).

Navarro et al. proposed a block-space map, denoted \(\lambda\), for
2-simplices and 3-simplices \([22, 23, 24]\), based on the solu-
tion of an \(m\) order equation that is formulated from the lin-
ear enumeration of the discrete elements. The authors report
performance improvement for 2 and 3-simplices. By being a
block-space map, the authors report correct mapping coordi-
nates up to problems of \(n = 62900\) for the 2-simplex case and
up to \(n = 1546\) for the 3-simplex case. Beyond these problem
sizes, the map requires 64-bit floating point square roots (FP64)
which penalize the speedup.
This work explores a new concept of a map, denoted \( \mathcal{H} \), that costs \( O(1) \) time and is as fast as \( \lambda \) and RB methods, while being free of numerical precision dimensional limitations. The proposed map \( \mathcal{H} \) preserves locality at block-level and only uses integer arithmetic and bit-shift operations for its computation, making it an exact map by design.

4. Formulation of \( \mathcal{H} \)

The formulation of \( \mathcal{H} \) focuses on the special cases \( m = 2, 3 \), where the mapping can also be supported by illustrations, although it is not limited to just those dimensions, as explained later in Section 6. Also, the analysis first assumes \( n \) as a power of two \( i.e., \ n = 2^k \) with \( k \in \mathbb{Z}_+ \), and later in sub-section 4.2 expands to the general case of \( n \in \mathbb{Z}_+ \). The case when \( m = 1 \) is not considered in the analysis as both the orthotope and simplex match in geometry thus no special map is required.

For the rest of the manuscript, the concept of an efficient map will be based on the following definition:

**Definition 4.1.** An efficient map is a function \( \mathcal{H} : \mathbb{Z}_2^n \rightarrow \mathbb{Z}_2^n \) that can map any thread coordinate \( \omega_x, \omega_y, \omega_z \) from a parallel space \( \Pi^2 \) of volume \( V(\Pi^2) = V(\Delta^n_2) \pm o(n^m) \), onto a unique location in \( \Delta^n_2 \), using \( O(1) \) arithmetic or bitwise operations, excluding explicit transcendental operations and roots.

The following sub-sections formulate maps for \( \Delta^n_2 \), \( \Delta^2_2 \) and analyze their efficiency according to Definition 4.1.

4.1. Mapping to 2-Simplices

Given a 2-simplex, denoted as \( \Delta^n_2 \), with \( n \) being its side length, its space \( V(\Delta^n_2) \) is given by the triangular numbers

\[
V(\Delta^n_2) = \frac{n(n + 1)}{2}. \tag{7}
\]

Each location of the 2-simplex is a \((x, y)\) pair where \( x + y \leq n \) satisfies when the origin is at the orthogonal vertex. The goal is to find an orthotope \( \Pi^2 \) with an asymptotic volume of \( O(V(\Delta^n_2)) \) and an efficient map \( \mathcal{H} \), that with \( O(1) \) arithmetic operations, assigns threads of \( \Pi^2 \) to unique locations in \( \Delta^n_2 \).

**Lemma 4.1.** There exists a set \( S^n_2 \) of self-similar regular orthotopes where \( V(S^n_2) = V(\Delta^n_2) \).

**Proof.** Let \( S^n_2 \) be a set of self-similar regular orthotopes where its total volume is defined by the recurrence

\[
V(S^n_2) = \left(\frac{n}{2}\right)^2 + 2V(S^{n/2}_2) \tag{8}
\]

where the largest regular orthotope of \( S^n_2 \) has dimensions \( \frac{n}{2} \times \frac{n}{2} \) and the initial condition is \( V(S^2_2) = 0 \). The expansion of Eq. (8) produces the geometric series

\[
V(S^n_2) = 2^0 \left(\frac{n}{2}\right)^2 + 2^1 \left(\frac{n}{2}\right)^2 + \cdots + 2^{\log_2(n)-1} \left(\frac{n}{2^\log_2(n)}\right)^2 
\]

\[
= \frac{n^2}{2} \log_2(n) \left(\frac{1}{2}\right)^\log_2(n). \tag{9}
\]

where its reduction via \( \sum_{i=0}^k d^i = \frac{d^{k+1} - 1}{d-1} \), results in

\[
V(S^n_2) = \frac{n^2}{2} \left(1 - \log_2(n) \left(\frac{1}{2}\right)^\log_2(n)\right) \tag{10}
\]

\[
= \frac{n^2}{2} - \left(\frac{1}{2}\log_2(n) - 1\right) \frac{n}{2} - 1 \tag{11}
\]

\[
= \frac{n(n - 1)}{2} = \Delta^2_2. \tag{12}
\]

Given that its possible to represent a 2-simplex as a set of regular orthotopes, it is now necessary to group them as a grid to fit in the GPU programming model.

**Lemma 4.2.** A set \( S^n_2 \) can be organized into a single irregular super-orthotope \( \Pi^2_{2,n-1} \) of dimensions \( \frac{n}{2} \times n - 1 \).

**Proof.** In the expansion of formula (9), each term can be thought as the contribution of a sub-set of \( 2^i \) regular orthotopes of equal size, each one of dimensions \( \frac{n}{2^i} \times \frac{n}{2^i} \), where \( i \) is the \( i \)-th level of recursion. When considering whole sub-sets, we have that its space is \( 2^i \times \frac{n}{2^i} = \frac{n}{2^i} \times \frac{n}{2} \) and therefore it is possible to stack these sub-sets to form a super-orthotope \( \Pi^2_{n/2,n-1} \) whose height is the result of the geometric series \( \sum_{i=1}^{\log_2(n)} \frac{n}{2} = n - 1 \).

Figure 5 left, illustrates the super-orthotope and how all sub-sets stack into different layers.

![Figure 5: \( \Pi^2_{2,n-1} \) (left) and \( \Delta^2_2 \) (right) are two different organizations of \( S^n_2 \).](image)

**Theorem 4.3.** Given a discrete orthogonal 2-simplex \( \Delta^2_{n-1} \), there exists a map \( \mathcal{H} : \mathbb{Z}_2^n \rightarrow \Pi^2_{2,n-1} \) to \( \Delta^2_{n-1} \) that is efficient by Definition 4.1.

**Proof.** The proof proceeds by construction. Let \( S^n_2 \) be a set of self-similar orthotes which by Lemma 4.1 matches \( \Delta^2_{n-1} \) in space. By Lemma 4.2, all regular orthotopes of \( S^n_2 \) can be organized to form an irregular super-orthotope \( \Pi^2_{n/2,n-1} \). For convenience, the origin of \( \mathbb{Z}_2^n \) plane is redefined at the top left corner of \( \Pi^2 \) and the vertical axis points down (Figure 5). The point \( \omega = (\omega_x, \omega_y) \) is defined as the two-dimensional coordinate of a discrete unit in \( \Pi^2 \), which corresponds to a thread-block, \( i.e., \) not a thread but a group of threads. Lemma 4.2 also establishes...
that sub-orthotopes share the same stack height level only if they are equal in size. Such property allows to compute the stack height level \( b \) of any discrete element of \( \Pi^2 \) as

\[
b = 2^{\lfloor \log_2(\omega_x + 1) \rfloor}
\]

as well as

\[
q = \left\lfloor \frac{\omega_x}{\omega_y} \right\rfloor
\]

which is the index of the orthotope for which the pair \( \omega \) belongs to, at level \( b \), from left to right. Finally, arithmetic operations between \( \omega, b, q \) produce the map

\[
\mathcal{H}(\omega) = (\omega_x + qb, \omega_y + 2qb + 1)
\]

which is efficient by Definition \( \text{4.1} \) as \( V(\Pi^2) = V(\Delta^2_{n+1}) + o(n^3) \) satisfies using \( O(1) \) arithmetic operations excluding roots.

The map \( \mathcal{H} \) from Eq. \( \text{16} \) is a considerable improvement over previous proposed maps based on the enumeration principle as it does not use square roots. Regarding the number of sequential steps, it is also more efficient than the recursive map by Ries et. al which was graphically similar but required \( O(\log_2(n)) \) \( \text{32} \) time. Additionally, since blocks have a constant size of \( \rho^2 \ll n \) (with \( \rho \) the number of threads in each dimension of the block), any extra number of threads only occurs at the diagonals or lower boundary, which is asymptotically \( \leq 2n\rho^2 \in o(n^3) \).

The computation of \( \mathcal{H} \) requires a constant number of arithmetic operations, as well as two transcendental functions in \( \mathbb{Z}_r \): \( \lfloor \log_2(\omega_x + 1) \rfloor \) and \( 2^{\lfloor \log_2(\omega_x + 1) \rfloor} \). In general, function \( \lfloor \log_2(\ldots) \rfloor \) can be computed fast on GPU by using the relation

\[
\lfloor \log_2(x) \rfloor = \text{bits} - \text{clz}(x)
\]

where \( \text{bits} \) is the number of bits of the word and \( \text{clz} \) counts the number of leading zero bits of \( y \), which is an efficient hardware-level instruction available in GPUs. The exponential \( 2^{\lfloor \log_2(\omega_x + 1) \rfloor} \) is computed as

\[
2^{\lfloor \log_2(\omega_x + 1) \rfloor} = 2^{\text{bits} - \text{clz}(\omega_x + 1)}.
\]

Considering that the two transcendental functions can be computed using bit-level operations, and that the parameters are reused by registers, it is expected that the parallel space improvement from \( O(n^2) \) to \( O(n) \) unnecessary threads can indeed result in a significant performance improvement, which for the case of 2-simplices can be up to \( 2 \times \) \( \text{22} \) \( \text{24} \). Moreover, since no square roots are required, \( \mathcal{H} \) has the potential to be faster and more precise than previous mapping techniques based on the enumeration principle \( \text{22} \) \( \text{22} \) \( \text{24} \).

### 4.2. Extending \( \mathcal{H} \) to the general case \( n \in \mathbb{Z}_r \)

The analysis of \( \mathcal{H} \) has assumed problems with sizes of the form \( n = 2^k \). For general \( n \), we present three extensions, with the third being the chosen and most efficient one.

1. **Approach \( n \) from above**: build a single orthotope \( \Pi^2_1 \), where \( n' = 2^{\lceil \log_2(n) \rceil} \) and filter out the threads outside the domain. This approach keeps simplicity at the cost of adding extra threads. The main disadvantage is for values of \( n = 2^k + c \) when \( c \) is a small number, *i.e.*, \( c \ll 2^k - 2^k \), as it can generate up to \( 4x \) the number of necessary threads.
2. **Approach \( n \) from below**: apply a set of super-orthotopes \( \Pi^2_n, \Pi^2_{n-1}, \Pi^2_{n+1}, \ldots \), where \( n_i = \log_2 \left( n - \sum_{i=1}^{k-1} n_i \right) \) for \( i \geq 2 \), \( n_1 = \lceil \log_2(n) \rceil \), plus a set of additional maps for the sub-regions that remain un-mapped below each simplex, at each level. This approach, while not adding extra threads, adds complexity in the algorithm and sequential steps.
3. **Concurrent Trapezoids**: This approach combines the ideas of the other two; it extends the mapped geometry to a trapezoid instead of a simplex, and assumes kernel concurrency, which is a feature that exists in actual GPU architectures. The idea is to launch, concurrently, a set of special orthotopes that map onto trapezoids in the data domain. The set of concurrent trapezoids follows the principle of approaching \( n \) from below, except for the smallest one that approaches the remaining size from above. This last trapezoid triggers when \( 2^{\lceil \log_2(n) \rceil} - n_k < T \), with \( T \) an arbitrary threshold value that serves as a mechanism to limit the size of the trapezoids set.

The **Concurrent Trapezoids** approach is the most efficient one in terms of map efficiency because of the following three features: (1) it works concurrently, keeping the cost of \( O(1) \) time unchanged, (2) the set of trapezoids will be small as the triggering condition for the last trapezoid has a high probability to occur at an early stage (only on rare occasions will produce a set of \( \log_2(n) \) elements which is the worst case) when using an adequate threshold, and (3) a small modification in the expression of \( \mathcal{H} \) makes the map reusable even when the mapped domain is now a trapezoid instead of a simplex. Figure \( \text{6} \) illustrates the idea behind the **concurrent trapezoids** approach.

![Figure 6: The concurrent trapezoids approach for a simplex of \( n = 27 \) with threshold of \( T = 1 \).

Under the **Concurrent Trapezoids** approach, \( \mathcal{H} \) receives three extra parameters that are common for all threads; i) an offset \( \delta(x, y) \) to specify the starting coordinate of each trapezoid map
4.3. Mapping to simplices.

Given a discrete orthogonal $3$-simplex $\Delta^3_n$, a set $S^3_n$ of self-similar orthotopes produces a space of $V(S^3_n) = V(\Delta^3_{n-1})$.

Proof. Let $S^3_n$ be a set of self-similar regular orthotopes where its total volume is defined by the recurrence

$$V(S^3_n) = \left(\frac{n}{2}\right)^3 + 2V(S^3_{n/2}) = \frac{n^3}{2} \sum_{i=1}^{\log_2(n)} \left(\frac{1}{4}\right)^i.$$  

(21)

A reduction via geometric series produces

$$V(S^3_n) = \frac{n^3 - n}{6} = V(\Delta^3_{n-1}).$$  

(22)

Here the diagonal plane is not considered, thus $V(S^3_n) = V(\Delta^3_{n-1})$. The way how $S^3_n$ (red cubes) is placed onto $\Delta^3_n$ (gray region) is illustrated in Figure 7.

Although the extra red regions can be re-used by mapping them onto their upper tetrahedron-like regions, recursively, packing the entire set into a super-orthotope of regular base $\frac{a}{2} \times \frac{b}{2} \times \frac{c}{2}$ (which is the idea behind $H$ in 2-simplices) will introduce a fraction of extra thread-space.

Lemma 4.5. Given a set $S^3_n$ with a half-size sub-division scheme, packing $S^3_n$ into a super-orthotope of regular base $\frac{a}{2} \times \frac{b}{2} \times \frac{c}{2}$ introduces a fraction of extra thread space.

Proof. The largest sub-orthotope of the set $S^3_n$ has dimensions $\frac{a}{2} \times \frac{b}{2} \times \frac{c}{2}$, therefore two of the dimensions of the super-orthotope $\Pi_{a,b,c}$ will necessarily be $a = \frac{a}{2}, b = \frac{b}{2}$ acting as the regular base. The third dimension will stack the rest of the sub-sets of regular orthotopes. At recursion level $k$, $S^3_n$ provides $2^{k-1}$ regular orthotopes of size $(\frac{a}{2^k})^3$, increasing the third dimension of $\Pi^3_{a,b,c}$ by $\frac{a}{2^k}$. This extra space induced on $\Pi^3_{a,b,c}$ by the height increase is a stack of size $\frac{a}{2^{k+1}} \times \frac{b}{2} \times \frac{c}{2}$. When $k > 1$ the elements provided by $S^3_n$ are not sufficient to fill the $k$-th stack, i.e.,

$$\sum_{i=1}^{2^{k-1}} \left(\frac{n}{2^k}\right)^3 = \frac{n^3}{2^{2k+1}} \leq \frac{n^3}{2^{2k+2}}.$$  

(23)

Therefore, the super-orthotope $\Pi_{a,b,c}$ containing $S^3_n$ will necessarily have empty spaces at each stack level. □

By Lemma 4.5, $H$ will not be efficient by Definition 4.1 as it introduces an extra space of $O(n^3)$. Nonetheless, such map may still be useful in practice as long as the extra space is a small fraction of $\Delta^3_n$. A convenient way to pack the sub-orthotopes in thread space is to displace the first major cube below and begin the stacking process horizontally from level $k \geq 2$. Such approach produces a super-orthotope $\Pi^3_{a,b,c}$ of dimensions $(\frac{a}{2}) \times (\frac{b}{2}) \times (\frac{c}{2})^{(n-1)}$ for $a, b, c$, respectively (see Figure 8, left).

While the packing approach is not perfectly efficient, in the infinite limit of $n$, the extra fraction of space of $\Pi^3_n$ over $\Delta^3_{n-1}$, denoted as $\alpha(\Pi^3_n, \Delta^3_n)$, is

$$\alpha(\Pi^3_n, \Delta^3_{n-1}) = \lim_{n \to \infty} \frac{V(\Pi^3_n)}{V(\Delta^3_{n-1})} - 1 = \lim_{n \to \infty} \frac{3n^2(n-1)}{16(\log_2(n+1))} - 1 = \frac{1}{8}$$  

(24)

Figure 7: The organization of $S^3_n$ (red) on $\Delta^3_{n-1}$ (grey).

Figure 8: A practical packing scheme to map $S^3_n$ onto $\Delta^3_{n-1}$.
which is 12.5% of $V(\Delta_3^3)$. Such amount of thread space constitutes a small fraction compared to a bounding-box strategy that surrounds the tetrahedron and generates practically 600% of the space of $\Delta_3^3$. Therefore, while $\Pi^3$ is not an efficient super-orthotope, there is still potential performance improvement that can be exploited by GPUs assuming a time efficient $O(1)$ cost map $\mathcal{H}$ can exist.

**Theorem 4.6.** For any discrete 3-simplex $\Delta_3^{n+1}$, there exists a time efficient map $\mathcal{H} : \mathbb{Z}_2^n \rightarrow \mathbb{Z}_2^n$ from $\Pi_3^{(2,n;3(n-1)/3)}$ to $\Delta_3^{n+1}$ that requires only $O(1)$ arithmetic or transcendental operations.

**Proof.** Analogous to Theorem 4.3, for convenience in the GPU programming model, the origins of both $\Pi_3^{b,c}$ and $\Delta_3^3$ are placed at the lower-right corner as shown in Figure 7 with the axes aligned to the orthogonal facets. It is worth noticing that the $z$ axis point upwards. By Lemmas 4.4 and 4.5 there exists a super-orthotope that contains the set $S_{n,2}$ with each sub-set of equally sized regular orthotopes organized by stack levels, except for the first sub-orthotope that is treated as a special case for being displaced from the stacking pattern.

Let $h(\omega)$ be an auxiliary block-space mapping of the single sub-orthotope of size $(n/2)^3$ onto the center of the tetrahedron, defined as

$$h(\omega) = \omega + (0, n/2, 1, 0). \quad (25)$$

For the $b, q$ parameters, they keep the definitions from Theorem 4.3 as the mapping layout allows projection onto the plane with an additional consideration for the extra spaces that fall out of $\Delta_3^3$ (the red spaces from Figure 7), for which the position is transposed in $x, y$ and complemented in $z$, acting as a hinge. With these settings, the combination of the parameters $\omega, q, b$ and the auxiliary function $h(\omega)$ allow the formulation of

$$\mathcal{H}(\omega) = \begin{cases} h(\omega), \quad \omega \in S_3^{1/2} \\ (\omega, + b, \omega, + 2qb + 1, \omega, - n/2), \quad \text{otherwise} \end{cases} \quad (26)$$

When the mapped blocks fall outside $\Delta_3^{n+1}$, then its coordinates are remapped following a hinge like pattern. Defining $L = (\omega_i \mod b, \omega_j \mod b, \omega_k \mod b)$ as the local coordinates of $\omega$ in their corresponding $S^3$ region, the hinge movement becomes $H(\omega) + (b - 1 - 2L, b - 1 - 2L, 2b - 1 - L)$. This map is only time efficient, i.e., $T(h(\omega)) + T'(H(\omega)) = O(1)$.

It is possible to make $\mathcal{H}$ fully efficient, i.e., to satisfy condition $V(\Pi^3) = V(\Delta_3^3) + o(n^n)$ of Definition 4.1 by including concurrent GPU kernel executions in the analysis. Such approach would allow to create multiple parallel spaces, one for each stack level of equally sized sub-orthotopes, without needing to pack them into a single super-orthotope. The number of simultaneous parallel spaces would be limited by the maximum number of concurrent kernels supported by the GPU, which as of 2022 is up to 128 concurrent kernels. In practice, such limit is sufficiently large for many applications as the number of stack levels is in the order of $O(\log_2(n))$. Furthermore, the map works in block-space which acts as an extra factor for reaching larger problem sizes. The next Section presents experimental performance results for $\mathcal{H}$ using 2-simplex and 3-simplex tests, running on different GPUs. The results are compared to state of the art approaches.

5. Experimental Evaluation

The proposed map $\mathcal{H}$, as well as state of the art approaches, are measured and compared against the bounding box approach. This gives a total of four approaches (Figure 9) to be compared:

- **RB**: Rectangular box [27]
- **\(a\)**: Lambda map [3, 24]
- **DP**: CUDA’s Dynamic Parallelism
- **\(\mathcal{H}\)**: New proposed map

All approaches are available to the community at [https://github.com/temporal-hpc/simplex-gpu-mappings](https://github.com/temporal-hpc/simplex-gpu-mappings).

### 5.1. Experimental Design

Four different computational patterns are tested on 2-simplex and 3-simplex domains. These are listed in Table 1.

| Test                        | 2-simplex | 3-simplex |
|-----------------------------|-----------|-----------|
| 1) [MAP] Only map           | *         | *         |
| 2) [ACCUM] +1 Accumulation  | *         | *         |
| 3) EDM Euclidean Distance Matrix | *       | *         |
| 4) [CA] Cellular Automaton  | *         | *         |

These tests serve to know what is the impact of application work in the overall speedup through an improved mapping. The first test, MAP, is a GPU kernel with no application work, i.e., just the thread mapping stage. It uses C++ volatile variables in order to prevent the compiler to optimize the mapping stage as it is not used afterwards. This kernel should reflect the theoretical speedup as it is mostly mapping work. The ACCUM test is a kernel where each mapped thread adds +1 to its corresponding data-element in the simplex domain. It is a memory-bound kernel as it does 1 read, 1 write and only 1 addition on each data element. The EDM test computes the Euclidean distance matrix, that is the distance $d(p_i, p_j)$ at each data-element of the simplex with location $i, j$. This test is a medium intensity application with more arithmetic work than the accumulation test, as it computes a square root for each data-element. Lastly, the cellular automaton computes John Conway’s game of life [31] on a simplex structure for fixed number of steps, with periodic boundary conditions for the 2-simplex, and free boundary conditions (fixed dead cells on the boundary) for the 3-simplex case. This test is a more intense memory-bound application which serves as a case where improvements to the mapping stage could have a lesser impact on performance.

The average running time as well as the power consumption are measured during kernel execution. Sufficient repeats are employed for each test in order to reach a statistical standard error of less than 1%. Then, plots of speedup (over the bounding-box approach) and energy efficiency are computed from these values.

The hardware used for all tests is detailed in Table 5. The TITAN GPUs share the same system while the A100 GPU is from a DGX A100 node of the Patagón supercomputer of Austral University of Chile [38].
5.2. Speedup and Energy Efficiency for 2-simplices

Figure 10 presents the speedup of each mapping technique over the bounding box approach, under different tests (columns) and GPUs (rows). In the MAP test (first column), \( \mathcal{H} \) and RB reach the theoretical speedup of \( 2\times \) over the Bounding box approach, for all GPUs. With the TITAN RTX, the \( \lambda \) map performance gets reduced to \( 0.5\times \) of speedup once \( n \geq 32154 \). The reason is because GPU has very few FP64 units, and at that problem size (with block size \( 16 \times 16 \) which is the fastest) the map needs to switch from FP32 to FP64 precision in the computation of a square root, otherwise it generates incorrect coordinates. The DP approach also fails to reach the maximum speedup for all GPUs. Instead it reaches up to \( 1.25\times \) of speedup in the best case using the A100 GPU. In the ACCUM test (second column), the maximum speedup is \( \sim 1.2\times \), with \( \mathcal{H} \) within the fastest maps. The RB map is also within the fastest, and DP becomes competitive as well once the problem size is large enough. In the case of \( \lambda \), it stays with the fastest maps as long as the GPU has sufficient FP64 units, otherwise it underperforms with \( \sim 0.4 \) of speedup as in the TITAN RTX. For the EDM2D test (third column), speedup is unstable at small problem sizes, but stabilizes at medium to high values. Here, both \( \mathcal{H} \) and RB stay competitive through all the range of \( n \), followed by \( \lambda \) (except when running in the TITAN RTX GPU) and DP. For the CA2D test (fourth column), the maximum speedup is \( 1.25\times \) and is achieved by all approaches using the A100 GPU. On the TITAN RTX GPU the fastest approaches are \( \mathcal{H} \) and RB, followed by DP and lastly \( \lambda \). It is worth noticing that in this case the performance of \( \lambda \) did not drop because the fastest version used thread blocks of size \( 32 \times 32 \), allowing the FP32 square root to be precise for the whole range. In the TITAN V GPU all approaches reach a speedup of \( \sim 1.15\times \) for large \( n \).

Figure 11 shows the power consumption in the case of the A100 GPU. As a global observation, the duration of all curves are in the same proportion of the speedups reported above. For the MAP test the peak power is near \( \sim 100W \), reached by all approaches except for DP which reaches a peak slightly above 90W. For the ACCUM test, \( \mathcal{H} \) has an intermediate consumption of up to \( \sim 180W \), while \( \lambda \) is the most power consuming one with a peak of \( \sim 210W \). In the EDM2D test, \( \lambda \) reaches the Max Thermal Design Power (TDP) of the A100 GPU, which is 400W. Here \( \mathcal{H} \) is positioned in the middle again, being less consuming than RB, and slightly more than DP. The reference Bounding approach oscillates between 270W and 300W. In the last test, the CA2D, \( \mathcal{H} \) and RB reach the same peak power consumption while DP is the less consuming one.

Figure 12 presents the energy efficiency of all approaches running on the A100 GPU. The bar charts represent the energy efficiency using the metric of number of elements per second (EPS) per Watt (EPS/W), while the numerical labels at the top of each bar show the total energy used for that particular run. In terms of energy efficiency, which is in log-Y scale, \( \mathcal{H} \) stays on average as one of the most energy efficient approaches, shared by RB and DP. On the other hand, the \( \lambda \) approach is the less energy efficient one.
5.3. Speedup and Energy Efficiency for 3-simplices

In the case of 3-simplices, the RB approach is discarded because it cannot be extended efficiently to 3D, as $n/2 \times n/2 \times n$ orthotope is double the necessary space and the arithmetic operations involved would require further research as it will be more complex. The map $\lambda$ is also discarded because it generates a 3-simplex ($i < j < k$ condition) in which no vertex has all of its incident facets orthogonal \([24]\), breaking the $x + y + z \leq n$ condition. Therefore 3-simplex tests consider $\mathcal{H}$ and two possible approaches using Dynamic Parallelism (DP). The first one ($DP_{\text{vanilla}}$) is the default extension of the DP approach for 2-simplices, while the second one ($DP_{\text{hinge}}$) implements the hinge idea of $\mathcal{H}$, as in Figure\([7]\) now using DP.

Figure\([13]\) presents the speedup of $\mathcal{H}$ and the DP approaches over BB, using different 3-simplex tests and GPUs. In the MAP test (first column) $\mathcal{H}$ approaches to $\sim 6x$ of speedup, matching the theoretical expected value. For the DP variants, the $DP_{\text{hinge}}$ version exhibits a higher speedup than the vanilla variant. On the ACCUM test (second column) $\mathcal{H}$ is the fastest map again.
but this time the speedup reaches up to ~ 3×. The DP variants show similar performance for the TITAN GPUs, and favors the hinge variant in the A100 GPU. Lastly, on the CA3D test (third column), \( H \) reaches a maximum speedup near ~ 1.5× followed by the DP approaches.

Figure 13 presents the power consumption time series for all tests running on the A100 GPU. It is worth noticing that the power consumption behavior for the MAP test puts \( DP \) and \( H \) as the approaches with less power peak. On the ACCUM and CA3D test \( H \) increases its peak power consumption surpassing the other approaches, but is the first one in making the power consumption curve to go down. Figure 13 presents the energy efficiency of all approaches running on the A100 GPU. This plots show more easily which map is the most energy efficient in terms of elements per second per Watt. Overall \( H \) stands as the most energy efficient one along with \( DP_{\text{hinge}} \).

6. Considerations for extending \( H \) to higher dimensions

The formulation of \( H \) for the 2-simplex and 3-simplex followed specific designs for their corresponding dimensions. Although the map takes constant time in both cases, it is worth noticing that for the 3-simplex it was necessary to introduce 12% of extra parallel volume in order to fit the set \( S_n^m \) on \( \Pi_n \) as a single-pass map, unless multiple parallel spaces are assumed in the model. When generalizing the approach to \( m \)-simplices, it is important to first verify if \( V(S_n^m) = V(D_n^m) + o(n^m) \) satisfies or not, and if not then analyze how much extra space is introduced. In the general case, the volume of a set \( S_n^m \) of self-similar regular orthotopes is

\[
V(S_n^m) = (rn)^m + \beta V(S_{rn}^m) = (rn)^m \sum_{i=0}^{\log_{1/r}(n)-1} (\beta r^m)^i 
\]

(27)

where \( r \) is the scaling factor and \( \beta \) the arity or multiplicity of the recursion. Applying the geometric series, the expression becomes

\[
V(S_n^m) = (nr)^m \left( \frac{\beta r^m \log_{1/r}(n) - 1}{\beta r^m - 1} \right) 
\]

(28)

\[
= \frac{n^m - \beta^{\log_{1/r}(n)}}{1/r^m - \beta}. 
\]

(29)

One can verify that setting \( r = 1/2 \) and \( \beta = 2 \) leads to equations 13 and 22 for \( m = 2, 3 \), respectively.
Theorem 6.2. Finding an efficient set requires to find parameters \( r, \beta \) such that it minimizes the target function \( V(S^m_n) - V(\Delta^m_n) \). The constraints are \( \beta > 1, 1/r > \beta \) as well as \( 1/r, \beta \in \mathbb{Z}^+ \).

Additional considerations include that \( \beta \text{opt} / (m^3) \) should not grow too fast as it has an impact on what is the initial \( n_0 \) for which \( V(S^m_n) \geq V(\Delta^m_n) \) holds. As an example, a value of \( r = 1/(m-1/m) \) produces the required \( m! \), making \( \beta \) a free parameter to be adjusted with \( \beta \geq 2 \). Choosing \( \beta = 2 \) provides a set \( S^m_n \) that covers \( \Delta^m_n \) from a certain \( n \geq n_0 \), where \( n_0 \) is a value that increases with \( m \). It is possible to bring \( n_0 \) closer to the origin by increasing \( \beta \), however the extra volume increases as well, presenting a trade-off. What is interesting is that from \( n \geq n_0 \), the parallel space is practically \( m! \) times more efficient than a bounding box approach, presenting a great potential for transforming this space improvement into a performance one.

7. Insights for Leveraging Tensor/Ray-Tracing Cores

Since 2018, GPU architectures have been introducing two new types of ASICs (Application Specific Integrated Circuits) onto the chip, i) Tensor cores (TC) and ii) Ray-tracing (RT) cores to further speedup Deep Learning and Real-time graphics applications, respectively. Leveraging the multiple TCs and RT cores that sit on a modern GPU depends on the application and how well it can reformulate its computation in terms of TC and RT operations.

7.1. Leveraging Tensor Core Units

The tensor core exposes the matrix multiply accumulate (MMA) operation: \( D_{\text{non}} = A_{\text{max}} \times B_{\text{non}} + C_{\text{max}} \) with different \( m \times n \times k \) formats\(^4\) to choose from depending on the numerical precision: \( 16 \times 16 \times 16 \) or \( 8 \times 32 \times 16 \) for FP16, \( 16 \times 16 \times 8 \) for TF32, or \( 8 \times 8 \times 8 \) for FP64, among others. Each MMA operation requires a dedicated warp of threads (32 threads), therefore parallelism granularity is at the warp level. Adapting \( H \) to TCs requires the reformulation of its computation, first by proposing a matrix layout to place its variables/coefficients and second by producing the desired computation from the fused multiply add (FMA) operations that take place in each row-column product

\(^4\)Internally, the GPU schedules how the operation is decomposed into even smaller matrices, such as \( 4 \times 4 \), to be processed by each TC.
of the MMA. In the case of $\mathcal{H}$, given the map is at block-level, an efficient adaptation should try to obtain several block coordinates for each MMA executed. An efficient adaptation of $\mathcal{H}$ to TCs would employ a format where the product $A \times B$ acts on non-square matrices, as the FMA operations are relatively short in length. The TF32 format $16 \times 16 \times 8$ can be an attractive solution if more precision is required, or the FP16 format $8 \times 32 \times 16$ to increase the number of simultaneous block coordinates, although at less precision. In any case, the layout is to place the constants of Eq. (16) or (19) as rows in $A$, and the $x,y$ block-related inputs for $\mathcal{H}$ as pairs of columns in $B$. Eq. (32) expresses the mentioned TC layout acting for two blocks (distinguished by the super-indices in $B$) in the case of 2-simplices, under a format of $m \times n \times k = 4 \times 4 \times 2$ just for simplicity.

$$D = \begin{bmatrix} a_2 & a_3 \\ a_3 & a_4 \end{bmatrix} \times \begin{bmatrix} b_{11} & b_{12} & b_{13} & b_{14} \\ b_{21} & b_{22} & b_{23} & b_{24} \end{bmatrix} + \begin{bmatrix} c_{x_1} & c_{y_1} & 0 & 0 \\ c_{x_2} & c_{y_2} & 0 & 0 \\ 0 & 0 & c_{x_5} & c_{y_5} \\ 0 & 0 & c_{x_6} & c_{y_6} \end{bmatrix}$$

$$D = \begin{bmatrix} a_1 & a_2 \\ a_3 & a_4 \end{bmatrix} \times \begin{bmatrix} b_{11} & b_{12} & b_{13} & b_{14} \\ b_{21} & b_{22} & b_{23} & b_{24} \end{bmatrix} + \begin{bmatrix} c_{x_1} & c_{y_1} & 0 & 0 \\ c_{x_2} & c_{y_2} & 0 & 0 \\ 0 & 0 & c_{x_5} & c_{y_5} \\ 0 & 0 & c_{x_6} & c_{y_6} \end{bmatrix}$$

(32)

The are four constants $a_1, a_2, a_3, a_4$, and the product $A \times B$ generates a block coordinate for each block twice. This is to allow threads to add their local coordinate on top of it, through the addition of matrix $C$. The resulting matrix is $D$ which contains the definitive positions per-thread to access the simplex domain. It is worth mentioning that this multi-block approach can be further improved by the use of the recent thread block cluster construct, which allows to group several CUDA blocks and synchronize them to share data, such as matrix fragments.

### 7.2. Leveraging Ray Tracing Cores

Ray Tracing (RT) cores are hardware-implemented pipelines that accelerate the process of querying the collision of a ray with a set of geometric primitives, such as triangles in 3D space. Internally, RT cores employ a hardware-implemented bounding volume hierarchy (BVH) to handle its irregular memory access patterns on the BVH more efficiently. Although the standard application of RT cores is to accelerate the generation of photo-realistic computer graphics from a 3D scene, it is still possible to use the ray-triangle intersection query as a fast tool to solve other kinds of problems, such as thread mapping.

In the case of thread mapping to a simplex domain, RT cores can contribute with a fast hardware accelerated framework that works similar to Dynamic Parallelism, to explore a non-boxed data domain during execution. Moreover, given that RT cores work in a fully dynamic context, it opens the possibility of mapping threads to fully dynamic changing domains, dropping the static restriction assumed in $\mathcal{H}$ and making it a general purpose mapping. A possible idea to leverage RT cores for simplex domains is to load the simplex as a voxel type geometry in 3D space, and launch waves of rays at different levels of thickness. This would generate a dynamic discovery process where the first waves of rays do a coarse-grained exploration, useful for discarding the 3D space with no simplex data. The process would gradually refine rays until they become voxel grained and access the data elements. The only limitation is that the hardware BVH was designed for 3D space.

### 8. Discussion and Conclusions

This work presented a new map, $\mathcal{H}$, for mapping blocks of threads onto $m$-simplex domains. The map was entirely formulated for the 2-simplex and 3-simplex cases, obtaining theoretical upper bounds on speedup and thread usage efficiency over a standard bounding-box approach. It was also experimentally evaluated and compared to other state of the art approaches, showing that $\mathcal{H}$ is competitive with respect to the other alternative approaches, reaching up to 2x of speedup just for the mapping stage, and between 1.1x ~ 1.3x of speedup under different tests. For 3-simplices it was overall the fastest map, approaching the theoretical 6x for the mapping stage, and between 1.5x ~ 3.2x under different tests. When comparing $\mathcal{H}$ with the state of the art approaches, we note that it is the only map that does exhibits a favorable performance and numerical precision in both 2D and 3D cases. Moreover, $\mathcal{H}$ is potentially extendable to higher dimensions offering up to $m!$ more efficiency. This generalization to $m$-simplices presents a challenge though, as obtaining an optimal set of orthotopes with minimal extra volume becomes an optimization problem where the scaling and replication parameters, $r, \beta$ respectively, produce a trade-off between extra space and the starting value $n_0$ from which the mapping can take place. Knowing what parameters are the optimal for building a self-similar set of orthotopes for any $m$-simplex, as well as find general methods for packing $S^m_n$ into super-orthotope are indeed interesting questions that deserve further study.

In terms of power consumption, $\mathcal{H}$ showed that although it achieves high power consumption during execution, it compensates by having a shorter duration, leading to reach among the highest values of elements per second per Watt (EPS/W). This makes $\mathcal{H}$ energy efficient, as for the same amount of energy it can process more elements than other approaches.

This work also analyzed the possibility of leveraging both Tensor Cores (TC) and Ray Tracing (RT) Cores that are otherwise unused during a regular CUDA application. A preliminary analysis shows that it is indeed feasible to implement mappings using these special purpose cores. In fact, TC can serve to speedup $\mathcal{H}$ directly, while RT core units show that it can offer a dynamic mapping approach more general than $\mathcal{H}$. Future research can work on implementing such approaches considering the modern 2022+ GPU architectures, and measure what is the empirical acceleration that these special purpose cores can provide to the thread mapping process.

As a conclusion, this work has shown that $\mathcal{H}$ is an scalable and energy efficient solution that can be of great interest researchers working on applications that need to execute long simulations on simplex structures, such as PDEs or Cellular Automata.

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