Analysis of the Electrical Parameters of SOI Junctionless Nanowire Transistors at High Temperatures

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ABSTRACT This work studies the effects of the temperature variation, from 300K to 500K, on the electrical parameters of SOI n-type and p-type junctionless nanowire transistors. The temperature influence on the threshold voltage, subthreshold slope, and the effective carrier mobility were analyzed. The mobility scattering mechanisms were analyzed and show that nanowire devices have the phonon scattering as their major component, although there is a significant component of the ionized impurity scattering that can be identified as well. These electrical parameters were also analyzed for short channel devices with a channel length of 40nm. P-type devices showed higher degradation with the temperature as the doping concentration is higher than n-type devices.

INDEX TERMS Threshold voltage, subthreshold slope, carrier mobility, high temperature, junctionless, nanowires, SOI.

I. INTRODUCTION

Triple-gate SOI nanowire transistors are still considered an excellent structure for the further reduction of transistors dimensions maintaining the good control of the channel charges. This multigate architecture allowed for the creation of the Junctionless Nanowire Transistor (JNT) that has a uniformly and heavily doped silicon layer, with no junctions between the source/drain and the channel. It is necessary to fully deplete the channel region to turn the device off, by the combination of the appropriate channel doping, gate workfunction, oxide charges, and temperature.

The JNT shows excellent electrical parameters with short channels [1] with near ideal subthreshold slope and strong suppression of the short channel effects [2], [3], and its characteristics show great potential for digital and analog applications [4]. These excellent parameters are obtained by the adoption of narrow fin widths and also allowing further integration of these devices on the integrated circuit as the device dimensions are reduced [5].

Fig. 1 presents the schematics of a junctionless nanowire transistor and its physical dimensions. The additional doping at the source and drain reduces the series resistance of these devices.

Different from inversion-mode transistors, JNTs have two conduction mechanisms when it is turned on, the bulk conduction and the accumulation conduction. When the gate voltage reaches the threshold voltage ($V_{TH}$) but is smaller than the flat-band voltage ($V_{FB}$), the bulk conduction is present in the interior of the silicon layer as the depletion coming from the gate insulator to the silicon body starts reducing with the appearance of a conduction path. When the gate voltage equals the $V_{FB}$ the channel becomes completely neutral and the device is in the onset of the accumulation conduction, presenting an interfacial layer near the gate oxide. For higher gate voltages both conduction mechanisms coexist but the accumulation conduction becomes dominant because of the exponential dependence of the accumulation carrier density on the surface potential [6], surpassing the bulk conduction.
For the analysis of the effective carrier mobility of the transistors, the distinction between these two main methods of conduction must be made clear, i.e., the flat-band voltage ($V_{FB}$) has to be accurately extracted. For the bulk conduction, the main mobility scattering mechanisms are the Coulomb scattering, due to the high doping of these devices, and the phonon scattering, due to the temperature [7]. The accumulation conduction has an additional scattering component of the surface roughness at higher gate voltages [8].

In general, when MOSFETs are included in an integrated circuit they are prone to work with temperatures higher than the room temperature [9]. So, the good understanding of the temperature increase effects on the performance of MOSFETs is crucial for the precise design of circuits [10], [11].

The effects of the high temperatures on the electrical characteristics of the triple-gate junctionless nanowire transistors have been reported in [1], [7], [12]–[18]. In these works, several aspects of the junctionless nanowire transistors were studied as a function of the high temperature. In [14] it was presented a drain current model for JNT for an extended temperature range. The JNT model of threshold voltage dependence with temperature was presented in [18] and these devices were experimentally studied in [1], [12], [17] with short channel and in [7] for long channel length. Similarly [1], [12], [13] also studied the Inverse Subthreshold Slope. In [7], [13] it was analyzed the carrier mobility as a function of the temperature which shows the impact of the scattering mechanisms on these devices. In [17] it was studied the impact of the series resistance on the n and p-type junctionless devices with different channel lengths as well as a study on the zero temperature coefficient. The characteristics of junctionless nanosheets as a function of the temperature were analyzed in [15]. Electric characteristics like DIBL and $I_{ON}/I_{OFF}$ were analyzed in [1] and the impact of the temperature on the off current was also analyzed in [7], [15], [20]. In [16] it was presented a simulated study on the characteristics of junctionless transistors for short channel devices.

This article presents the effects of high temperatures on the electrical parameters of n-type and p-type narrow triple-gate junctionless nanowire transistors with long and short channel devices. It complements the previously mentioned studies, which are mainly focused on n-type transistors in a smaller temperature range, with an analysis of the carrier mobility extracted with the Split C-V method from room temperature up to 500K.

II. DEVICES FABRICATION

The experimental devices used in this work are long channel ($L = 10\mu m$) and short channel ($L = 40nm$) n-type and p-type junctionless nanowire transistors fabricated in Silicon-on-Insulator (SOI) wafer with a buried oxide thickness of 145nm. The fin height ($H_{FIN}$) is 9nm and fin width ($W_{FIN}$) is 13nm. The devices have 50 parallels fins to increase the gate area and allow for capacitance measurements. They have an equivalent oxide thickness (EOT) of 1.3nm and 5nm thick metal gate (TiN), followed by polysilicon to complete the gate stack. The channel doping of these junctionless nanowire transistors was adjusted accordingly to result in symmetrical threshold voltages at room temperature [2].

The channel doping and the flatband voltage were extracted by the method proposed in [19]. For the n-type JNT the donor doping concentration is approximately $N_D = 5.10^{18} \text{cm}^{-3}$ and the flatband voltage is $V_{FB} = 0.7V$ at 300K. For the p-type JNT the acceptor doping concentration is approximately $N_A = 1.10^{19} \text{cm}^{-3}$ with symmetrical flatband voltage of $V_{FB} = -0.7V$ at 300K.

III. EXPERIMENTAL RESULTS

The I-V and C-V curves were measured from 300K to 500K using a Low Temperature Microprobe (LTMP) system from MMR Technologies and a B1500A Semiconductor Analyzer. The temperature controller of LTMP system ensures accuracy better than 100 mK for the chuck temperature in the overall range of temperatures evaluated.

Fig. 2. shows the drain current as a function of the gate voltage curves obtained in the several temperatures for n-type and p-type junctionless nanowire transistors both in linear and logarithmic scales. The long channel devices were biased with $|V_{DS}| = 50 \text{ mV}$. From these curves, one can see a clear Zero Temperature Coefficient (ZTC) point for both types of transistors, where there is no variation of drain current with the temperature [17]. One can see that this point varies between each type of JNT, where for n-Type the ZTC is around $V_{GS} = 0.65$ and for p-type the ZTC is around $V_{GS} = 0.8V$. This increase of gate bias for the pMOS ZTC gate voltage is related to the series resistance and the incomplete ionization of these devices [17]. One can also see that the $I_{DS}$ of n-type transistors is about three times higher than the $I_{DS}$ of p-type transistors at $|V_{GS}| = 1V$ as the hole mobilities are lower than the electron mobility. It can also be seen that there is an increasingly higher leakage current ($I_{DS}$) for $V_{GS} = -0.5V$ for nMOS and $V_{GS} = 0.5V$.
for pMOS) as the temperature is increased. This effect is associated with the trap-assisted tunneling for both n-type and p-type junctionless transistors [20].

From this curve, we can see that as the device reduces the channel length there is a high increase in the drain current, although here the short channel effects show a high influence on these devices. We can also see that for the n-type device as we increase the temperature the same effects as the long channel device happens for short channel devices, the increase in the drain current, the decrease in $V_{TH}$, and the increase in the inverse subthreshold slope for both drain bias. The ZTC also appears for the n-type device. However, for the p-type device, there is a different effect on the drain current as the increase in temperature show at first an increase in drain current for both drain bias. The ZTC point also does not happen for this p-type device, which we can infer that there is not a balanced compensation between the threshold voltage and the carrier mobility in this device.

Similar results were obtained using TCAD simulations of short-channel JNT with high doping concentration showing no ZTC point [16] and experimentally in [12] for channel length of 100nm. The effect of the series resistance also contributes to the absence of the ZTC as it is related to the incomplete carrier ionization [17], which is much higher on the analyzed p-type transistors due to the higher doping concentration.

Using the data from Fig. 2 for both types of transistors the threshold voltage and inverse subthreshold slope were extracted for each temperature.

Fig. 3 shows the inverse subthreshold slope as a function of the temperature for both n-type and p-type transistors. From these curves, we can see that both types of transistors show similar values, slightly higher than the theoretical limit for the inverse subthreshold slope for each temperature.
The inverse subthreshold slope of JNT can be calculated by eqn. (1) [21], which is directly influenced by the body factor n and the temperature.

\[
SS = \left(1 + 2 \frac{\sinh(L_G/(2\lambda_{TG}))}{\sinh(L_G/\lambda_{TG})}\right) \frac{kT}{q} \ln(10)n
\]  

(1)

In the eqn (1), \(\lambda\) is the characteristic length, \(k\) is the Boltzmann constant, \(T\) is the absolute temperature, and \(q\) is the electron charge.

The JNT body factor n can be evaluated by the eqn. (2) [21].

\[
n = 1 - \left[\frac{1}{C_{OX}} - \frac{2Q_{SI}}{qN_{A,D} \varepsilon_{SI}(2W_{FIN} + W_{FB})^2}\right] \times \left[\frac{1}{C_{OX}^2} + \frac{2(V_{BS2} - V_{BS})}{qN_{A,D} \varepsilon_{SI}W_{FIN}}\right]^{-\frac{1}{2}}
\]  

(2)

And \(Q_{SI}\) is the charge of the device given by eqn. (3) [21].

\[
Q_{SI} = qN_{D}W_{FIN}H_{FIN} - 2C_{BOX}(V_{FB} - V_{BS})
\]  

(3)

Here \(C_{OX}\) is the gate oxide capacitance per unit of length, \(C_{BOX}\) is the buried oxide capacitance per unit of length, \(V_{FB}\) is the flat band voltage, \(\varepsilon_{SI}\) is the silicon dielectric permittivity, \(V_{BS}\) is the back-gate voltage and \(V_{BS2}\) is the smoothing function for the continuous transition between \(V_{FB}\) and \(V_{BS}\).

The p-type device has a slightly higher subthreshold slope as it has a higher doping concentration in the channel than the n-type one. As the device is in full depletion in the subthreshold regime, the inverse subthreshold slope is determined by the body factor. As expressed in eqn. (2), the body factor is related to the device dimensions and the doping concentration. In the evaluated temperature range, the subthreshold slope presents an almost linear increase with temperature, with a rate of 0.182 mV/dec K for p-type and 0.195 mV/dec K for the n-type long channel transistors.

For short channel devices, we can see that the n-type device presents excellent electrostatic control of the gate, with SS in the same order as for the long-channel transistor in the whole temperature evaluated, while the p-type device is showing a higher degradation from the short channel effects, as we compare with the long channel one. However, no additional degradation for the short channel p-type device due to the temperature rise has been identified. The tendency of the SS is similar to that presented in [1], [12], [13]. Inversion mode devices also show a higher degradation of SS for short channel devices compared to JNT as analyzed in [13], due to the longer effective channel length of JNT in the subthreshold regime [22].

Fig. 4 shows the absolute value of the threshold voltage (\(V_{TH}\)) as a function of the temperature for long and short channel devices. For the n-type device, the threshold voltage decreases linearly with temperature increase, while for the p-type device it increases linearly with the increase of the temperature. For the long-channel n-type JNT the \(V_{TH}\) changes from 0.54V at 300K to 0.45V at 500K with a rate of \(-0.39 \text{mV/K}\). For the p-type transistor the \(V_{TH}\) changes from \(-0.57\)V at 300K to \(-0.45\)V at 500K with a rate of \(0.561 \text{mV/K}\). The threshold voltage variation with the temperature can be evaluated by eqn. (4) [18],

\[
\frac{\partial V_{TH}}{\partial T} = \frac{\partial V_{FB}}{\partial T} - \left(\frac{q}{\varepsilon_{SI}} \left(\frac{A}{P}\right)^2 + \frac{qA}{C_{OX}}\right) \frac{\partial N_{D}}{\partial T} + \frac{1}{q} \frac{\partial \Delta E_0}{\partial T}
\]  

(4)

where \(V_{FB}\) is the flatband voltage, \(A = W_{FIN} \cdot H_{FIN}\), and \(P = W_{FIN} + 2H_{FIN}, \Delta E_0\) is the variation of the minimum energy level in the conduction band due to the quantum confinement.

Fig. 5 depicts the calculated terms of equation (4): the term on the left side of the equation is the threshold voltage dependencies with the temperature (\(\theta_1\)), the first term on the right side of the equation is the flatband voltage dependence with the temperature (\(\theta_1\)) and the second term is the doping concentration dependence with the temperature (\(\theta_2\)), following the equations given in [18] for both n-type and p-type devices. The last term of equation (4) has a low variation with the temperature and can be neglected in the analysis.
The flatband voltage variation with the temperature is dependent on the Fermi potential and the Bandgap variations, and the second term of (4) is dependent on the channel doping of the device with temperature, which is influenced by the geometric parameters of the device.

For the n-type device the dependence of the doping concentration with temperature was calculated, resulting in approximately \( -0.07 \text{mV/K} \) at 300K and becomes very small at higher temperatures where most of the dopants are ionized. This result also shows that the threshold voltage variation with the temperature is different from the flatband voltage variation, especially at room temperature. For the p-type devices, the doping concentration dependence with the temperature shows a much higher value than the n-type devices as the incomplete ionization becomes more important for this device due to its higher doping concentration. This, in turn, produces different values of the threshold voltage variation with the temperature and the flatband voltage variation with the temperature. These devices’ doping concentration is near the Mott transition, which means they behave similar to metals, but the incomplete ionization reduces this concentration and affects the threshold voltage [17].

The experimental slope obtained is in accordance with [1], [7], [13], [17] but with slightly smaller values for junctionless nanowire devices and in case of lower doping on the channel the calculated threshold voltage variation with the temperature is reduced. Inversion mode devices also show higher threshold voltage variation values than JNT in [13]. The lower the doping and the smaller the fin width the more influence the first term of the flatband voltage with the temperature have on the threshold voltage [18].

From the threshold voltage variation with the temperature for short channel devices, we can see that as the channel length is decreased it increases the influence of the temperature on the device characteristics. The dependence of the threshold voltage with the temperature almost double compared with the long channel devices, which is associated with the larger charge sharing between the gate and source/drain electrodes as the temperature increases, making the short-channel transistors more sensible to temperature increase. It becomes even worse for higher doping concentrations, as clearly seen in Fig. 4 for the p-type device. This larger threshold voltage variation with temperature also shows that the variation with the mobility is not enough to balance these two parameters and create a ZTC point.

Fig. 6 show the capacitance as a function of the gate voltage for 300K to 500K. These curves show that the gate-to-channel capacitance varies with the temperature for gate voltages from \( V_{\text{TH}} \) to \( V_{\text{FB}} \). The conduction mechanism with the increase in temperature reduces the maximum depletion of the silicon layer and therefore allows the device to begin the bulk conduction at a lower gate voltage.

To analyze the sharp rise of the capacitance at a lower temperature the slopes of the capacitance at bulk conduction were extracted. The slope is around 1.27 pF/V at 300K and decreases to around 0.78 pF/V at 500K for n-type devices. This shows a slower rise of the capacitance which is 30% lower than the rise of the capacitance at room temperature. This is the result of the difference between the threshold voltage and the flatband voltage, since the former has a higher degradation with temperature, and produces different slopes for each temperature. For p-type devices, the slope is around 1.2 pF/K at 300K, and 0.712 pF/K at 500K, showing slightly reduced values of the slope, meaning that for p-type devices the capacitance rises slower with the increase in gate voltage that can be attributed to the flat band variation with the temperature being higher than the threshold voltage variation with the temperature. Above the flat band voltage, the devices tend to the gate oxide capacitance where the channel is completely neutral and there is not a significant change due to the temperature variation.

The Split-CV [23] method was used for the mobility extraction as it is a reliable method for the extraction of the electron mobility in junctionless devices [3] and can be applied for n and p-type transistors. For the measured devices, the series resistance can be neglected because of their long channel length and parallel fin structure. The effective mobility (\( \mu_{\text{eff}} \)) can be extracted by eqn. (5). To relate
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FIGURE 7. Effective electron and hole mobility for several temperatures from 300K and 500K as a function of the charge density.

the mobility with the charge density \( N \) eqn. (6) was used.

\[
\mu_{\text{eff}} = \frac{L_G^2 I_D S}{V_{D S} \int_{-\infty}^{V_{G S}} C_{G C}(V_{G S}) dV_{G S}} \tag{5}
\]

\[
N = \frac{1}{L_G W_{\text{eff}} q} \int_{-\infty}^{V_{G S}} C_{G C}(V_{G S}) dV_{G S} \tag{6}
\]

Here \( \mu_{\text{eff}} \) is the effective mobility, \( I_D S \) is the drain current, \( V_{D S} \) is the drain voltage, \( V_{G S} \) is the gate voltage, \( C_{G C} \) is the gate-to-channel capacitance, \( q \) is the electron charge and \( W_{\text{eff}} \) is the effective width \( W_{\text{eff}} = W_{\text{FIN}} + 2H_{\text{FIN}} \). Equation (5) uses data from both the I-V and C-V curves to extract the effective mobility whereas the charge density only uses data from C-V curve.

Fig. 7 shows the effective electron and hole mobility as a function of the charge density for 300K to 500K for both p and n-type junctionless nanowire transistors. For the charge density around \( 1.5 \times 10^{12} \text{ cm}^{-2} \) the electron mobility of all n-type devices shows similar values of \( 40 \text{ cm}^2/\text{V.s} \) and at around \( 0.8 \times 10^{12} \text{ cm}^{-2} \) the hole mobility of all p-type devices shows similar values of \( 5-7.5 \text{ cm}^2/\text{V.s} \). For larger charge densities one can see a clear mobility reduction as the temperature is increased for both types of devices.

Fig. 8 shows the mobility of all devices as a function of the temperature at the charge density of \( 5 \times 10^{18} \text{ cm}^{-3} \) as a function of the temperature of the nanowire devices.

40%. This drop-in mobility is similar to demonstrated in [13] for n-type long channel devices at higher temperatures. To further analyze the mobility dependence on the temperature and relate it with the scattering mechanisms, the exponential temperature coefficient has been used. Following the carrier mobility description with the temperature in eqn. (7) [24]:

\[
\mu \propto T^{-\alpha} \tag{7}
\]

Here \( T \) is the temperature and \( \alpha \) is the temperature coefficient. The extracted temperature coefficients for n-type devices show an exponential coefficient of approximately \(-1\) from 300K to 500K, which shows the degradation of approximately 0.26cm²/V.s/K, while for p-type devices, the temperature coefficient is around \(-0.87\), which shows degradation of approximately 0.1cm²/V.s/K.

It is known that for a highly doped JNT the phonon scattering has a temperature coefficient of \(-1.5 \) [7]. On the other hand, due to the high doping concentration, the ionized impurity scattering mechanism has a temperature coefficient of \(+1.5\). Then, these two components would cancel each other showing a small dependence of the mobility on the temperature if the doping concentration is high enough [7].

As demonstrated in Fig. 8 the devices studied here show a temperature coefficient around \(-1\) for n-type devices, indicating that the main scattering component is the phonon scattering, as \( \alpha \) is close to \(-1.5\), similarly for the p-type device with a coefficient of \(-0.87\) shows that, although it has a doping concentration of around \( 1.10^{19} \text{ cm}^{-3} \) it still does not compensate the Coulomb scattering and the phonon scattering. It shows that the p-type devices still have a high degradation of the mobility with the temperature. Comparatively the mobility of the n-type devices suffers more from the phonon scattering than p-type devices, and p-type devices have a slightly higher ionized impurity scattering as the device shows higher doping concentration.

Now we are going to present a study of the high temperature on the electric characteristics of short channel junctionless nanowire transistors with a channel length of
40nm for DIBL and $I_{ON}/I_{OFF}$. Fig. 9 shows the DIBL as a function of the temperature. The n-type device also shows good control of the channel charges as the DIBL of this device stays around 50mV/V as the temperature is increased to 500K. The p-type device shows much higher DIBL values as the temperature increases. Similar tendencies for DIBL in short channel devices were observed in [1].

Fig. 10 shows the on current as a function of the off current extracted for $|V_{DS}| = 1$V, with $|V_{GS}| = 1$V for the on current and $|V_{GS}| = 0$V for the off current. Here we can see that the degradation of the off current goes almost over a decade for each step of 100K. And comparatively the on current shows little variation with the temperature. Similar results show that the degradation of the off current with temperature is also much larger than the degradation of the on current [1], [7], [15], [20]. Fig. 11 shows the $I_{ON}/I_{OFF}$ of these devices as a function of the temperature for the nMOS and pMOS JNT with a channel length of 40nm. Here we can see that at room temperature the devices have a ratio higher than $2.10^7$ for n-type devices and about $5.10^5$ for p-type devices. The degradation for the p-type devices is related to the short channel effects previously demonstrated, leading to increased off current which is, in turn, a consequence of the subthreshold slope increases with the temperature. Although the n-type devices show better $I_{ON}/I_{OFF}$, this ratio drops at the same rate as the off current for over a decade for every 100K.

IV. CONCLUSION

This work analyzed the electrical parameters for long and short channel n and p-type Junctionless Nanowire Transistor in the temperature range from 300K to 500K. The threshold voltage was analyzed and shows the difference between the flatband and threshold voltage dependence with temperature affects the other electric characteristics of the transistor. The gate capacitance demonstrated that the temperature increase influences the capacitance increase rate between its minimum and maximum values. The effective mobility was analyzed and shown a reduction with temperature. Using the temperature coefficient for mobility degradation with temperature it has been possible to verify that phonon scattering is the dominating mechanism reducing the mobility for both types of devices. While p-type devices comparatively with n-type devices show a slightly higher ionized impurity scattering and slightly reduced phonon scattering. It was possible to see that for short channel n-type JNT presents good parameters comparable to the long channel devices for SS and $V_{TH}$. For the p-type devices that have higher doping concentration, it affects the parameters especially the threshold voltage as a function of the temperature.

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