DNA: Differentiable Network-Accelerator Co-Search

Yongan Zhang∗1 Yonggan Fu∗1 Weiwen Jiang∗2 Chaojian Li1 Haoran You1 Meng Li3 Vikas Chandra3 Yingyan Lin1

Abstract

Powerful yet complex deep neural networks (DNNs) have fueled a booming demand for efficient DNN solutions to bring DNN-powered intelligence into numerous applications. Jointly optimizing the networks and their accelerators are promising in providing optimal performance. However, the great potential of such solutions have yet to be unleashed due to the challenge of simultaneously exploring the vast and entangled, yet different design spaces of the networks and their accelerators. To this end, we propose DNA, a Differentiable Network-Accelerator co-search framework for automatically searching for matched networks and accelerators to maximize both the task accuracy and acceleration efficiency. Specifically, DNA integrates two enablers: (1) a generic design space for DNN accelerators that is applicable to both FPGA- and ASIC-based DNN accelerators and compatible with DNN frameworks such as PyTorch to enable algorithmic exploration for more efficient DNNs and their accelerators; and (2) a joint DNN network and accelerator co-search algorithm that enables the simultaneous search for optimal DNN structures and their accelerators’ micro-architectures and mapping methods to maximize both the task accuracy and acceleration efficiency. Experiments and ablation studies based on FPGA measurements and ASIC synthesis show that the matched networks and accelerators generated by DNA consistently outperform state-of-the-art (SOTA) DNNs and DNN accelerators (e.g., 3.04× better FPS with a 5.46% higher accuracy on ImageNet), while requiring notably reduced search time (up to 1234.3×) over SOTA co-exploration methods, when evaluated over ten SOTA baselines on three datasets.

1 Introduction

Powerful deep neural networks (DNNs)’ prohibitive complexity stands at odds with the limited resources of daily life devices and has raised various environmental concerns (Strubell et al., 2019), motivating intensive studies of efficient DNN solutions. Early works merely explore from either the algorithm or hardware level. For example, compression techniques attempt to trim down DNNs’ complexity, while on the hardware level representative FPGA- and ASIC-based accelerators (Chen et al., 2016; Du et al., 2015; Zhang et al., 2018b) develop customized micro-architectures (e.g., # of memory hierarchies and processing elements (PEs), PE array dimension and shape, size of different memories, and network-on-chip (NoC) design) and algorithm-to-hardware mapping methods (e.g., loop tiling strategy, loop size, and loop order) to boost DNN acceleration efficiency. Later, hardware-aware neural architecture search (HA-NAS) (Cai et al., 2018; Wu et al., 2019a; Tan et al., 2019) emerged to automate the design of efficient network structures (e.g., # of layers and channels, size of kernels, and layer operations). Recently, it has been recognized that maximizing DNN accelerators’ efficiency requires joint exploration of both the networks and their accelerators (the latter refers to the accelerators’ micro-architectures and mapping methods hereafter) (Hao et al., 2019; Abdelfattah et al., 2020; Li et al., 2020b; Lin et al., 2019).

Despite their promise, existing works have yet to unleash the great potential of jointly optimizing DNNs and their accelerators. The key challenges include (1) the prohibitively large joint space consisting of the coupled yet different network and accelerator spaces with extremely sparse optima, (2) non-differentiable hardware costs, and (3) how to algorithmically describe a generic accelerator search space. We aim to tackle the aforementioned challenges, and make the following contributions:

• We propose DNA, a Differentiable Network-Accelerator co-search framework (see Fig. 1) that enables a joint search of DNNs’ network structures and their accelerators’ micro-architectures and mapping methods, promising to largely boost the efficiency and expedite the development of DNN accelerators.

• We develop Differentiable Accelerator Search (DAS), a generic differentiable accelerator search engine for exploring the large and discrete design space of both
DNA: Differentiable Network-Accelerator Co-Search

Differentiable Network-Accelerator (DNA) Co-Search

Input
Task Application
Hardware Resources

Differentiable Network-Accelerator Search (DNS) Engine

Hardware Feedback
Co-Search

Differentiable Accelerator Search (DAS) Engine

Proxy Task
Task Loss
Hardware Efficiency

Generic Network Design Space
Differentiable Search Algorithm

Proxy Task
Energy
Latency

Generic Accelerator Design Space
Differentiable Search Algorithm

Output
Optimal Networks
Optimal Accelerators

Figure 1: An illustration of our DNA co-search framework, which accepts target tasks and accelerator specifications and then automatically generates matched DNNs and their accelerators to maximize both task accuracy and hardware efficiency.

DNN accelerators’ micro-architectures and mapping methods. DAS distinguishes itself from existing accelerator searches which mostly adopt RL-based methods and thus are limited in scalability and performance.

• We construct a Generic DNN Accelerator Design Space (GADS) that is applicable to different DNN accelerators including both FPGA- and ASIC-based ones. Such a GADS can serve as a key enabler for algorithmically exploring both (1) DNN accelerators’ large and discrete design space and (2) hardware-driven efficient DNNs.

• Through FPGA measurements and ASIC synthesis, extensive experiments and ablation studies validate DNA’s effectiveness and superiority: DNA generated networks/accelerators consistently outperform SOTA DNNs/accelerators, while requiring a notably reduced search time compared to SOTA co-exploration methods. We also visualize DNA generated accelerators to provide insights towards efficient DNN accelerators.

2 RELATED WORKS

Hardware-Aware NAS (HA-NAS). HA-NAS has been developed to automate the design of efficient DNNs. Early works (Tan et al., 2019; Howard et al., 2019; Tan & Le, 2019) utilize RL-based methods, and thus suffer from substantial search time and costs, limiting their scalability. Later, motivated by DARTS (Liu et al., 2018), differentiable HA-NAS (Wu et al., 2019a; Wan et al., 2020; Jin et al., 2019; Li et al., 2020b) emerged to greatly improve both the search and hardware efficiency, respectively. However, existing HA-NAS methods (1) mostly consider hardware costs (e.g., FLOPs or latency) on one given device/accelerator and (2) have not yet fully explored the hardware design space. For maximizing DNNs’ acceleration efficiency determined by both the networks and their underlying hardware, it is highly desired to jointly search for both the networks and their hardware accelerators.

DNN accelerators. DNNs’ powerful performance and prohibitive complexity have motivated extensive research in customized DNN accelerators. Given a DNN and its acceleration specification, SOTA accelerators (Du et al., 2015; Chen et al., 2017; Zhao et al., 2020; Li et al., 2020a) explore different micro-architectures and algorithm-to-hardware mapping methods to maximize data reuses and thus acceleration efficiency. Early works rely on experts’ manual design, which can be very time consuming and require cross-disciplinary knowledge in algorithm, micro-architecture, and circuit design. Recently, there has been a growing interest in design flow (Xilinx Inc., a; Chen et al., 2005; 2009; Rupnow et al., 2011) and DNN accelerator design automation (Wang et al., 2016; Zhang et al., 2018a; Guan et al., 2017; Venkatesan et al., 2019; Wang et al., 2018). However, these works mostly explore the accelerator design space, leading to sub-optimal solutions.

Software/Hardware co-exploration. Jointly exploring the networks and their accelerators has been shown to be promising (Hao et al., 2019; Abdelfattah et al., 2020; Yang et al., 2020; Jiang et al., 2020; Li et al., 2020b). For exam-
Despite their promise, there is still much room to further enlarge the extent of co-exploration and thus improve the achieved performance. First, existing works have not yet considered a generic accelerator space including both the micro-architectures (e.g., # of memory hierarchies/PEs, PEs’ dimension/shape, size of different memories, and NoC design) and the mapping methods (e.g., loop tiling strategy, and loop size/order), which is also a key challenge for co-search/exploration. Second, the RL-based methods (Hao et al., 2019; Abdelfattah et al., 2020; Yang et al., 2020) adopt RL-based controllers to search for the networks and to determine which of the two ASIC accelerators should be selected; and (Li et al., 2020b; Choi et al., 2020) extend differentiable NAS to network and accelerator co-search. Despite their promise, there is still much room to further enlarge the extent of co-exploration and thus improve the achieved performance. First, existing works have not yet considered a generic accelerator space including both the micro-architectures (e.g., # of memory hierarchies/PEs, PEs’ dimension/shape, size of different memories, and NoC design) and the mapping methods (e.g., loop tiling strategy, and loop size/order), which is also a key challenge for co-search/exploration. Second, the RL-based methods (Hao et al., 2019; Abdelfattah et al., 2020; Yang et al., 2020) adopt RL-based controllers to search for the networks and to determine which of the two ASIC accelerators should be selected; and (Li et al., 2020b; Choi et al., 2020) extend differentiable NAS to network and accelerator co-search. Despite their promise, there is still much room to further enlarge the extent of co-exploration and thus improve the achieved performance. First, existing works have not yet considered a generic accelerator space including both the micro-architectures (e.g., # of memory hierarchies/PEs, PEs’ dimension/shape, size of different memories, and NoC design) and the mapping methods (e.g., loop tiling strategy, and loop size/order), which is also a key challenge for co-search/exploration. Second, the RL-based methods (Hao et al., 2019; Abdelfattah et al., 2020; Yang et al., 2020) adopt RL-based controllers to search for the networks and to determine which of the two ASIC accelerators should be selected; and (Li et al., 2020b; Choi et al., 2020) extend differentiable NAS to network and accelerator co-search.

3 THE PROPOSED DNA FRAMEWORK

This section describes our DNA framework. We first provide an overview and the problem formulation, and then DNA’s co-search algorithm, followed by DNA’s two search engines and the proposed generic accelerator search space.

3.1 DNA: overview and formulation

As mentioned in Sec. 1, the challenges of effective network-accelerator co-search include (1) the prohibitively large and irregular joint space versus very sparse optima excelling at both accuracy and efficiency, as shown in Fig. 2, (2) non-differentiable hardware costs, and (3) the lack of a generic accelerator search space description.

Our DNA framework aims to tackle the first of the aforementioned challenges via gradient-based optimization to effectively and efficiently identify the optimal network and accelerator pairs. As shown in Fig. 1, DNA accepts user-defined datasets, target performance (e.g., task accuracy and hardware efficiency), and resource constraints as inputs to automatically generate matched pairs of DNNs and their accelerators to maximize both the accuracy and efficiency given the resource constraints. DNA consists of two search engines: (1) the DAS engine integrated with a generic accelerator design space, which enables differentiable search to handle the accelerators’ large and discrete design space, and (2) the DNS engine, built upon SOTA differentiable NAS works (Wu et al., 2019a). Formally, we can formulate DNA’s optimization as:

$$\min_{\omega} L_{val}(\omega^*, NET(\alpha)) + \lambda L_{hw}(NET(\alpha), HW(\gamma^*))$$

(1)

$$s.t. \quad \omega^* = \arg \min_{\omega} L_{\text{train}}(\omega, NET(\alpha)),$$

(2)

$$s.t. \quad \gamma^* = \arg \min_{\gamma} L_{\text{hw}}(NET(\alpha), HW(\gamma))$$

(3)
Algorithm 1 DNA’s differentiable network-accelerator co-search algorithm.

Input: supernet weight $\omega$, the network space $\text{NET}(\alpha)$, the accelerator space $\text{HW}(\gamma)$, the total search epoch $\text{max\_epoch}$

Output: the optimal network $\text{optimal\_net}$ and the optimal accelerator $\text{optimal\_accelerator}$

while epoch $< \text{max\_epoch}$ do

Obtain optimized accelerators $\text{HW}_{m}^\ast (m = 1, ..., M)$ using Eq. 7 for $M$ DNNs sampled from the current network distribution $\text{NET}(\alpha)$ and calculate the average hardware cost for each operator based on Eq. 4

for one training epoch do

update $\omega$ based on Eq. 2

update $\alpha$ based on Eq. 1 where $L_{hw}$ is calculated using Eq. 5

end

Derive $\text{optimal\_net}$ by selecting the operator with the maximal weighted coefficients for each layer based on Eq. 6

Derive $\text{optimal\_accelerator}$ for the optimal $\text{optimal\_net}$ based on Eq. 7

return $\{\text{optimal\_net}, \text{optimal\_accelerator}\}$

where $L_{train}$ and $L_{val}$ are the task loss of training and validation, respectively; $\omega$, $\alpha$, and $\gamma$ are the supernet weights (Liu et al., 2018), DNNs’ structure parameters (i.e., architecture parameters in (Liu et al., 2018)), and the accelerator parameters, respectively; $\text{NET}(\alpha)$ and $\text{HW}(\gamma)$ denote the network and the accelerator space parameterized by $\alpha$ and $\gamma$, respectively; and $L_{hw}$ is the hardware-cost loss determined by both the network and its accelerator.

Despite its simplicity in formulation, it is in general intractable to analytically solve Eq. 1–Eq. 3. DNA integrates its DNA and DAS engines to simultaneously search for optimally matched networks and accelerators at much improved search efficiency, as illustrated in Fig. 3.

3.2 DNA: the joint search algorithm

Here we describe DNA’s co-search algorithm. There are two practical challenges to design a differentiable co-search algorithm for effectively navigating through the network and accelerator joint space. First, ideally the hardware-cost penalty for each layer-wise network operator should be obtained when being executed on the final searched optimal accelerator, which is not yet available at each co-search epoch as the optimal network is still unknown, i.e., an chicken-and-egg problem. Second, the network is searched by regularizing $\alpha$ in a layer-wise manner (see Eq. 6), while the accelerator $\gamma$ is determined by the whole DNN (see Eq. 7) due to the global accelerator parameters shared among all the layers, e.g., the loop-order in Tab. 1.

To address these challenges, DNA obtains the hardware-cost loss $L_{hw}$ at each co-search epoch by approximating the final optimal accelerator using the accelerator optimized for the network consisting of layer-wise operators that associate with a high probability. The hypothesis is that the network operators that have higher probabilities are also more likely to appear in the final optimal network, and thus, the corresponding optimal accelerators are likely to be the final optimal one. Specifically, at each epoch, DNA samples $M$ networks from the current network distribution $\text{NET}(\alpha)$ and obtains the optimal accelerator for each of them using its DAS engine (see Sec 3.4); the hardware-cost loss of each operator is then obtained using its average hardware cost on the $M$ optimal accelerators generated from the previous step. For example, the hardware cost of the $k$-th operator in the $l$-th layer $O_{lk}$ is formulated as:

$$E_{\text{NET}-p(\text{NET}|\alpha)}(L_{hw}(O_{lk}, \text{HW}^\ast)) \approx \frac{1}{M} \sum_{m=1}^{M} L_{hw}(O_{lk}, \text{HW}_{m}^\ast)$$

where $\text{HW}_{m}^\ast$ is the optimal accelerator generated using DNA’s DAS engine (see Eq. 7 in Sec. 3.4) for the $m$-th sampled network, and $L_{hw}(O_{lk}, \text{HW}_{m}^\ast)$ is the hardware-cost loss of accelerating the operator $O_{lk}$ using the accelerator $\text{HW}_{m}^\ast$. As a result, the hardware-cost loss of the whole DNN in Eq. 1 can be formulated in a layer-wise manner:

$$L_{hw}(\text{NET}(\alpha), \text{HW}(\gamma^\ast)) = \sum_{l=1}^{L} \sum_{k=1}^{K} \alpha_{lk} E_{\text{NET}-p(\text{NET}|\alpha)}(L_{hw}(O_{lk}, \text{HW}(\gamma^\ast))) \approx \frac{1}{M} \sum_{l=1}^{L} \sum_{k=1}^{K} \sum_{m=1}^{M} \alpha_{lk} L_{hw}(O_{lk}, \text{HW}_{m}^\ast)$$

Essentially, the hardware-cost loss $L_{hw}$ at each co-search epoch is approximated using the weighted sum of the approximated hardware cost for all the layer-wise operators. The co-search algorithm of DNA is summarized in Alg. 1, the effectiveness and superiority of which are consistently validated in our experiments (see Sec. 4). For example, DNA boosts the search efficiency by orders-of-magnitude while leading to superior accuracy and hardware efficiency.

3.3 DNA: the DNS engine

The DNS engine can be realized by leveraging SOTA differentiable NAS works. First, for the network search space, we
consider the SOTA hardware-friendly search space in (Wu et al., 2019a) which searches the kernel size, channel expansion ratio, and group number for each building block; Second, for the network search algorithm, we adopt the SOTA differentiable one with Gumbel-Softmax in (Wu et al., 2019a), which computes the output of the l-th layer $A_l$ as a weighted sum of all candidate operators:

$$A_l = \sum_{k=1}^{K} \alpha_{lk} O_{lk}(A_{l-1})$$

where $K$ denotes the total number of layer-wise candidate operators, $O_{lk}$ denotes the $k$-th operator for the $l$-th layer, and $\alpha_{lk}$ denotes the weighted coefficient of $O_{lk}$.

### 3.4 DNA: the DAS engine

EDD (Li et al., 2020b) attempts a pioneering step to differentiably co-search the network and its accelerator, their search space is yet limited to include only one accelerator parameter (i.e., the parallel factor) within their accelerator template. Their parallel factor can be analytically fused into the theoretical computational cost (e.g., the number of FLOating-point OPerations or FLOPs) in their framework. However, such a fuse strategy is not always applicable to naturally non-differentiable accelerator parameters such as the loop size and loop order, which are critical to the hardware efficiency (Chen et al., 2016; Venkatesan et al., 2019). A more general and efficient accelerator search engine is thus highly desired to unleash the potential of network-accelerator co-search.

Our DAS engine aims to close the above gap and realizes a generic differentiable accelerator search engine built on top of our GADS (see Sec. 3.5). Specifically, we reformulate Eq. 3 and propose a differentiable method to solve it:

$$\gamma^* = \min_{\gamma} \sum_{s=1}^{S} GS(\gamma^s) \times L_{hw}(NET(\alpha^s), HW(GS(\gamma^1),..., GS(\gamma^S)))$$

where the accelerator $HW$ is characterized by its accelerator parameters $\gamma^s$ ($s = 1, ..., S$), which is a normalized vector representing the probability of the corresponding choice of its represented accelerator parameter, and $GS(\gamma^s)$ denotes Gumbel-Softmax sampling (Gumbel, 1948; Maddison et al., 2014) of the $s$-th accelerator parameter $\gamma^s$.

Unlike NAS, different options of one accelerator parameter are NOT additive, i.e., cannot be formulated as a sum weighted by the probability as in (Liu et al., 2018). As such, for each accelerator parameter, we apply Gumbel-Softmax sampling (Gumbel, 1948; Maddison et al., 2014) to sample only one choice $GS(\gamma^s)$ of the $s$-th accelerator parameter. Once all the accelerator parameters are sampled, the corresponding DNN accelerator’s hardware efficiency can be obtained using SOTA accelerator performance estimators, where in this work we refer to (Xu et al., 2020) for FPGA-based accelerators and (Wu et al., 2019b; Parashar et al., 2019) for ASIC-based accelerators. We then multiply the resulting hardware-cost loss with the sampled $GS(\gamma^s)$ and relax to Gumbel-Softmax (Jang et al., 2016) during backpropagation for estimating the gradients.

### 3.5 Generic Accelerator Design Space (GADS)

Similar to NAS, a generic accelerator search space is a prerequisite for algorithmic accelerator exploration and optimization. However, it is challenging to develop such a space for DNN accelerators due to their large and discrete design space. First, there are numerous choices for the algorithm-to-hardware mapping methods (i.e., how to temporally and spatially schedule all the DNN’s operations to be executed in the target accelerators). Second, there are many ways to design the accelerators’ micro-architectures, which are characterized by the number of memory hierarchies and PEs, the size of each memory hierarchy, the shape and size of the PE array, and the NoC design (Chen et al., 2017).

| Memory Hierarchy | Loop-order | Loop-size |
|------------------|------------|-----------|
| DRAM             | TBS        | -         |
| Global Buffer    | TBS        | TBS       |
| PE array         | -          | TBS       |
| Register File (RF) | TBS       | TBS       |

| NoC design | Max # of PEs | Pipeline/Multi-cycle |
|------------|--------------|----------------------|
| TBS        | TBS          | TBS                  |

We construct a generic accelerator search space as shown in Tab. 1 by leveraging the commonly used nested for-loop accelerator description (Chen et al., 2016; Parashar et al., 2019; Yang et al., 2016; Zhang et al., 2015; Zhao et al., 2020) which naturally bridges the accelerator’s micro-architectures and mapping methods with DNNs’ network parameters. More details about the nested for-loop description can be found in the appendix. Next, we introduce each accelerator parameter in Tab. 1:

**loop-order**: the orders of the loops within each memory hierarchy, each of which has a total of $n$ data dimensions. As such, $n$ loops correspond to an $n$-item ordering problem. To be compatible with the proposed DAS engine in Sec. 3.4, where each accelerator parameter should have all possible choices parameterized by the corresponding $\gamma$ vector (see Eq. 7), we formulate the loop-order as a problem of picking one choice from a total of $n$ options without replacement for $n$ times (e.g., $n = 6$ considering the number of data dimensions in DNNs).

**loop-size**: the size of each loop in the for-loop description. The product of all loop-sizes associated with each data dimension needs to equal the corresponding algorithm-
mic dimension, because the nested loop sizes as a whole dictate the total number of execution iterations. Then, intuitively, the possible choices for a certain loop’s size are all the choices that the corresponding data dimension can be factorized into.

NoC design: the parallel execution pattern of MACs (multiply–accumulate operations) when accelerating DNNs on an accelerator, which is determined by the PE array style. In this work, we consider three NoC options following the common practice, as inspired by SOTA accelerators (Chen et al., 2016; Zhang et al., 2015; Zhao et al., 2020):

- parallelizing the computation over the output partial sums, where the dimensions of output channels, output rows, and output columns are executed in parallel.
- parallelizing the computation over the kernels, where the dimensions of output channels, input channels, kernel rows, and kernel columns are executed in parallel.
- parallelizing the computation over both the kernel and output dimensions, where the dimensions of output channels, kernel rows, and output columns are executed in parallel.

max number of PEs: the maximal number of PEs in the design which can range from 1 to a specified value and are determined by the area constraint.

pipeline/multi-cycle: a binary choice between a chunk-based pipeline micro-architecture of the DNN accelerator and a multi-cycle micro-architecture shared by all layers, inspired by SOTA FPGA-based accelerators (Zhang et al., 2018b; Shen et al., 2017), with each of the two choices having different designs. For example, if the chunk-based pipeline micro-architecture is chosen, the allocation of different DNN layers to different chunks would be a hyperparameter and often differ for different DNN structures and accelerators. In our DAS, each layer’s assignment can be formulated and parameterized by a $\gamma$ vector. Also, depthwise convolutions are assigned to a different set of chunks considering their unique structures as compared to vanilla convolutions.

4 EXPERIMENT RESULTS

In this section, we first introduce the experiment setup, and then evaluate DNA over both SOTA (1) HW/SW co-exploration works and (2) HA-NAS methods. Next, we present ablation studies to evaluate DNA’s co-search algorithm and DAS engine. Finally, we visualize DNA’s searched network and accelerator and discuss the insights.

4.1 Experiment setup

4.1.1 Evaluation baselines and datasets

For evaluating DNA over SOTA co-exploration works, we consider (1) three co-exploration FPGA baselines: HS-Co-Opt (Jiang et al., 2019), BSW (Abdelfattah et al., 2020), EDD (Li et al., 2020b) and (2) three co-exploration ASIC baselines: NASIC (Yang et al., 2020), NHAS (Lin et al., 2019), and DANCE (Choi et al., 2020). For benchmarking over SOTA HA-NAS methods, we consider four baselines: EfficientNet-B0 (Tan & Le, 2019), FBNet (Wu et al., 2019a), FBNet-V2 (Wan et al., 2020), and ProxylessNAS (Cai et al., 2018). For evaluating DNA’s DAS engine, we consider both expert-designed and tool-generated SOTA accelerators in (Qiu et al., 2016; Xiao et al., 2017; Zhang et al., 2018b). Our experiments consider three datasets: CIFAR-10, CIFAR-100, and ImageNet.

4.1.2 Software experiment setup

Search and evaluation on CIFAR-10/100. Search space: we adopt the same search space as (Wu et al., 2019a), except the stride settings for each group (i.e., a set of blocks with the same number of output channels), in order to adapt to the resolution of the input images in CIFAR-10/100. In particular, we follow the stride settings of MobileNetV2 on CIFAR-10/100 in (Wang et al., 2019), which is $\{1, 1, 1, 2, 1, 2, 1\}$ for all the seven groups. Search settings: the search for the optimal DNNs and accelerators adopts 50 epochs with a batch size of 64. In particular, we (1) update the supernet weights on half of the training dataset using an SGD optimizer with a momentum of 0.9 and an initial learning rate of 0.025 associated with a cosine decay, and (2) update the network parameters on the other half of the training dataset using an Adam optimizer with a momentum of 0.9 and a fixed learning rate of 3E-4. Like SOTA differentiable NAS methods, we apply Gumbel-Softmax on the network parameters and treat each parameter option’s weighted coefficients as their contribution to the supernet, following (Wu et al., 2019a), where the initial temperature is set to 3 and decayed by 0.92 at each epoch. Meanwhile, for updating the hardware accelerator parameters, we conduct updates at each epoch using an SGD optimizer with a momentum of 0.9 and a fixed learning rate of 1E-9. Evaluate the derived networks: for training the derived networks from scratch, we follow (Liu et al., 2018) and adopt an SGD optimizer with a momentum of 0.9 and an initial learning rate of 0.01 associated with a cosine decay. Each network is trained for 600 epochs with a batch size of 96.

Search and evaluation on ImageNet. Search space: we adopt the same search space as (Wu et al., 2019a) which is a SOTA search space for generating efficient DNNs via NAS. Search settings: we follow the same hyper-parameter settings as (Wu et al., 2019a) for searching on ImageNet, while additionally updating the hardware accelerator parameters at each epoch using an SGD optimizer with a momentum of 0.9 and a fixed learning rate of 1E-9. Specifically, the search for both the optimal network and accelerator adopts 90 epochs with each having a batch size of
we train the de-

DNA achieves a 1234.3

192; we first update the supernet’s weights on 80% of the training dataset using an SGD optimizer with a momentum of 0.9 and an initial learning rate of 0.1 associated with a cosine decay, and then update the network structure parameters on the remaining 20% of the training dataset using an Adam optimizer with a momentum of 0.9 and a fixed learning rate of 1E-2. The initial temperature of Gumbel-Softmax is set to 5 and then decayed by 0.956 at each epoch. Evaluate the derived networks: we train the derived networks using an SGD optimizer with a momentum of 0.9 and an initial learning rate of 0.05 associated with a cosine decay. Each network is trained for 180 epochs with a batch size of 512.

Hardware cost and hyperparameters. We adopt Frame-Per-Second (FPS), latency, or Energy-Delay-Product (EDP) as the hardware-cost loss (i.e., $L_{hw}$ in Eq. 1) to compare with various baselines and set $M = 10$ for Eq. 4 in all the experiments. We empirically find that $M$ can trade-off the search time and stability, i.e., smaller $M$ reduces the search time while its resulting accelerators might be sub-optimal (e.g., their efficiency does not meet the specification). Our observation is that the performance of our DNA is not sensitive to $M$ for $M > 5$, and we thus choose $M = 10$.

4.1.3 Hardware experiment setup

Accelerator evaluation methodology. To evaluate DNA’s generated accelerators, we adopt standard FPGA and ASIC evaluation and implementation flows. For evaluating FPGA-based accelerators, we employ the Vivado HLS design flow (Xilinx Inc., a). Note that during the search for FPGA-based accelerators, DNA makes use of a SOTA accelerator performance predictor (Xu et al., 2020) to obtain fast and reliable estimation. For evaluating ASIC-based accelerators, we use SOTA accelerator performance estimation tools Timeloop (Parashar et al., 2019) and Accelergy (Wu et al., 2019b) during and after the search. As (Parashar et al., 2019; Wu et al., 2019b) suggest, the unit energy and latency are obtained using CACTI7 (Balasubramonian et al., 2017) and Aladdin (Shao et al., 2014) based on a commercial 32nm or 45nm CMOS technology depending on that of the baselines for a fair comparison.

4.2 DNA over SOTA co-exploration works

Search efficiency. Here we benchmark our DNA over SOTA co-exploration works (Jiang et al., 2019; Abdelfattah et al., 2020; Li et al., 2020b; Yang et al., 2020) in terms of the search space size and search time. As shown in Tab. 2, DNA can handle a remarkably larger (e.g., 2.21E+48 vs. 3.63E+49) joint search space while requiring the shortest search time (e.g., 4.2 vs. 5184 GPU hours), as compared to all the SOTA baselines. Specifically, on ImageNet DNA achieves a 5.46% and 0.7% higher accuracy with a 3.04× and 1.94× higher FPS under a 450 and 900 Digital-Signal-Processor (DSP) limit, respectively, as compared to HS-Co-Opt (Jiang et al., 2019) and EDD (Li et al., 2020b); on CIFAR-100 DNA achieves a 1234.3× speed-up in search time when handling a 6.1E+38× larger search space, resulting in a 7.35% better accuracy and 1.18× higher FPS. This set of evaluations validates that DNA’s differentiable co-search can indeed handle a notably larger joint space with much improved search efficiency, enabling both fast development and superior performance.

Achieved FPS on FPGA. Here we compare DNA’s generated accelerators with those of the co-exploration baselines, HS-Co-Opt (Jiang et al., 2019) and BSW (Abdelfattah et al., 2020), in terms of the achieved FPS and accuracy under the same FPGA resource budgets and datasets, as shown in Fig. 4. We can make two observations from this evaluation. First, DNA generated accelerators consistently achieve the highest FPS with the same or even a higher accuracy, validating DNA’s advantage. Specifically, on CIFAR-10 with

| Method target on FPGA | Dataset | Network Space | Accelerator Space | Joint Space | Search Time (GPU Hours) | DSP Limit | Accuracy (%) | FPS |
|----------------------|---------|---------------|-------------------|-------------|-------------------------|-----------|--------------|-----|
| HS-Co-Opt (Jiang et al., 2019) DNA (Proposed) | CIFAR-10 | 1.15E+18 | 1.15E+18 | 103.9 | 450 | 96.10 (10.91) | 52.4 (11.48×) |
| BSW (Abdelfattah et al., 2020) DNA (Proposed) | CIFAR-100 | 4.20E+05 | 3.63E+09 | 5184 | 512 | 72.00 | 54.5 |
| HS-Co-Opt (Jiang et al., 2019) DNA (Proposed) | ImageNet | 2.22E+18 | 2.22E+18 | 266.8 | 450 | 70.24 | 10.5 |
| EDD (Li et al., 2020b) DNA 8-bit (Proposed) | ImageNet | 3.65E+19 | 900 | 75.10 (10.67) | 78.1 (11.94×) |

| Method target on ASIC | Dataset | Network Space | Accelerator Space | Joint Space | Search Time (GPU Hours) | Area (mm²) | Accuracy (%) | EDP (J × clock cycle) |
|----------------------|---------|---------------|-------------------|-------------|-------------------------|-----------|--------------|----------------------|
| NASAIC (Yang et al., 2020) DNA (Proposed) | CIFAR-10 | 1.70E+03 | 1.67E+09 | 4.6 | 3.34E+03 | 92.62 | 1.62E+06 |
| DNA (Proposed) | ImageNet | 9.85E+20 | 2.21E+48 | 4.2 (1.1×) | 5.92E-01 | 96.50 (3.88) | 4.99E+03 (1324.0×) |
Figure 4: DNA generated FPGA-based accelerators over those of SOTA co-exploration works HS-CO-Opt (Jiang et al., 2019) and BSW (Abdelfattah et al., 2020), where we adopt the same DSP limits as the baselines, i.e., 450/512/450 on CIFAR-10/100/ImageNet, respectively.

a 450 DSP limit, DNA boosts the FPS by $1.48 \times \sim 3.39 \times$, while offering a $8.01\% \sim 10.91\%$ higher accuracy over HS-Co-Opt; on CIFAR-100 with a 512 DSP limit, DNA achieves a $1.18 \times \sim 3.44 \times$ higher FPS while boosting the accuracy by $0.35\% \sim 5.15\%$ over BSW; and on ImageNet with a 450 DSP limit, DNA achieves a $3.04 \times$ higher FPS with a $5.46\%$ higher accuracy as compared to HS-Co-Opt. Second, under various resource settings and datasets, DNA’s generated accelerators can trade-off the achieved FPS and accuracy (e.g., a higher accuracy at the cost of a reduced FPS) under the given FPGA resource budget.

Achieved EDP/latency on ASIC. For evaluating DNA generated ASIC-based accelerators, we consider three SOTA co-search works, NASAIC (Yang et al., 2020), NHAS (Lin et al., 2019), and DANCE (Choi et al., 2020), based on their reported metrics and the same settings (e.g., precision, area, and dataset). Fig. 5 shows the benchmarking over NASAIC, from which we can make two observations. First, DNA generated accelerators achieve a much improved EDP while leading to a higher accuracy as compared with NASAIC, e.g., 324.0× EDP reduction together with a 3.88% improvement in accuracy. Second, similar to the experiments for designing FPGA-based accelerators, we can see that DNA generated ASIC-based accelerators can flexibly trade-off between the achieved accuracy and efficiency (i.e., EDP here). Note that the surprisingly higher EDP and area for NASAIC, as noted in Tab. 2, is caused by the much reduced hardware utilization due to their design consideration of heterogeneous tasks, leading to severely low utilization when executing one task. Tab. 3 summarizes the evaluation results over NHAS, where DNA adopts the same dataset (ImageNet), network precision (4-bit), and accelerator metric (latency) as the NHAS baseline. We can see that DNA generated accelerators outperform NHAS in all aspects: a 0.96% higher accuracy on ImageNet while having a 20.89% and 6.3% reduction in the required latency and area, respectively. Additionally, we benchmark DNA over the reported results of DANCE (Choi et al., 2020) under the same settings, where a 16-bit network precision is adopted to be comparable with DANCE. As shown in Tab. 3, DNA achieves both better hardware performance and higher accuracy, with a 3.50% higher accuracy on ImageNet while having a 64.94% and 22.34% reduction in the latency and area, respectively.

4.3 DNA ablation: DNA over SOTA HA-NAS works

In this sub-section, we evaluate DNA over SOTA HA-NAS works. Specifically, we compare the acceleration efficiency of DNA generated accelerators and SOTA HA-NAS generated networks when they are accelerated by their optimal accelerators, which are generated by the DAS engine under a DSP constraint of 900 (the maximum one in a ZC706 board (Xilinx Inc., b)) to maximize the achieved FPS, as summarized in Fig. 6. Note that we consider two kinds of precision, i.e., 16-bit and 8-bit, and we adopt 8-bit for a fair comparison over EDD with searched precision and adopt 16-bit when comparing with all other HA-NAS works.

Table 3: Evaluating DNA generated ASIC-based accelerators over NHAS (Lin et al., 2019) and DANCE (Choi et al., 2020) under the same setting.

| Optimization Methods | Accuracy (\%) | Latency (ms) | Area (mm²) | Precision (bit) |
|----------------------|--------------|--------------|------------|----------------|
| NHAS (Lin et al., 2019) | 70.74 | 1.58 | 5.87 | 4 |
| DNA (Proposed) | 71.70 | 1.25 | 5.50 | 4 |
| NHAS (Lin et al., 2019) | 68.70 | 8.13 | 2.73 | 16 |
| DNA (Proposed) | 72.20 | 2.85 | 2.12 | 16 |

Figure 5: Accuracy vs. EDP of DNA generated ASIC-based accelerators over three SOTA co-exploration designs on CIFAR-10 in NASAIC (Yang et al., 2020).
to maintain their reported accuracy. We can see that (1) compared with EDD in searched precision, DNA (8-bit) achieves a 0.7% higher accuracy and 1.94x higher FPS; and (2) compared with SOTA HA-NAS methods, DNA (16-bit) achieves a 1.48x higher FPS while having a +0.7% higher accuracy over FBNet and a 1.60x higher FPS with comparable accuracy (-0.1%) over EfficientNet-B0.

Figure 6: Accuracy vs. FPS of DNA and SOTA HA-NAS generated networks (Tan & Le, 2019; Wu et al., 2019a; Wan et al., 2020; Cai et al., 2018) and EDD (Li et al., 2020b).

4.4 DNA ablation: co-search algorithm

Experiment setting. To evaluate our DNA’s effectiveness and necessity, we consider sequential search (SEQ-Opt) on the same search space and MobileNetV2 (Sandler et al., 2018) optimized by DAS as our baseline. For the former, we first use DNA’s DNS engine to search for the optimal DNN structure that minimizes the task loss and a theoretical computational loss, i.e., FLOPs, and then adopt DNA’s DAS engine to search for the corresponding optimal accelerator of the resulting DNN from the previous step. For the latter, the FPS/EDP of MobileNetV2 are obtained from the optimal accelerator searched by DNA’s DAS engine. For a fair comparison, we ensure that the DSP/ASIC area is the same for all experiments.

Results. Fig. 7 shows the achieved accuracy vs. FPS/EDP on both FPGA/ASIC, indicating that DNA’s co-search algorithm consistently outperforms the baselines. In particular, for the case on FPGA, we can see that (1) DNA outperforms MobileNetV2 and its optimal accelerator with a 1.64x improvement in FPS and a 0.82% higher accuracy; and (2) DNA achieves a 1.63x improvement and a 1.01% higher accuracy over the SEQ-Opt baseline. For the case on ASIC, we can make the observations that (1) DNA outperforms MobileNetV2 and its optimal accelerator with a 0.51x reduced EDP and a 0.27% higher accuracy; and (2) DNA achieves a 0.88x reduced EDP and a 0.58% higher accuracy over the SEQ-Opt baseline. This set of experiments validate both the necessity of co-search and the effectiveness of DNA’s co-search algorithm.

We also evaluate DNA’s co-search algorithm over a random search by comparing their searched accelerators in the same joint search space, as summarized in Tab. 4. Specifically, we first conduct random network search by randomly sampling 300 DNNs, then perform random accelerator search by randomly sampling 300 accelerators for each network, and finally select the DNNs and paired accelerators that together achieve the best accuracy-FPS trade-offs. The observation is that random network search tends to result in small networks (higher density in the adopted SOTA network space) with inferior accuracy, while the random accelerator search cannot find an efficient accelerator even for small networks.

4.5 DNA ablation: DAS over SOTA DNN accelerators

The proposed DAS is one key enabler of our DNA framework. To evaluate its efficacy, we compare the hardware efficiency of the DAS generated accelerators with SOTA accelerators under the same datasets and models. We consider three representative FPGA-based accelerators including (Qiu et al., 2016; Xiao et al., 2017; Zhang et al., 2018b), when accelerating two networks (AlexNet and VGG16) on ImageNet. The results in Tab. 5 show that our DNA generated accelerators outperform both expert-designed and tool-generated SOTA accelerators under the same dataset, DNNs, and FPGA resources. For example, DAS generated accelerators achieve up to 2.12x improvement in throughput on VGG16 under the same setting. The consistent better performance of our DAS generated accelerators validates the effectiveness of our DAS in navigating the large and discrete design space of DNN accelerators to search for optimal DNN accelerators. Note that when using DAS to

Table 4: Evaluating DNA over random network and accelerator search on CIFAR-100 evaluated on FPGA.

| Search Strategy          | Accuracy (%) | FPS   |
|--------------------------|--------------|-------|
| random network/accelerator search | 70.3 - 75.1  | 31.9 - 82.5 |
| DNA (Proposed)           | 74.6 - 78.1  | 64.7 - 158.6 |
Table 5: Our DAS generated FPGA accelerators vs. SOTA FPGA accelerators on a Zynq XC70Z45 FPGA, when accelerating SOTA networks (VGG16 and AlexNet) on ImageNet at a frequency of 200MHz.

| Network       | Resource Utilization | DAS generated | SOTA networks (VGG16 and AlexNet) |
|---------------|----------------------|---------------|------------------------------------|
| VGG16         | 680/900 DSP          | 262           | 230                                 |
| VGG16         | 824/900 DSP          | 137           | 291 (1.11x - 1.22x)                |
| VGG16         | 780/900 DSP          | 247           | 272 (1.10x)                        |
| AlexNet       | 723/900 DSP          |               |                                    |
| AlexNet       | 808/900 DSP          |               |                                    |
| AlexNet       | 704/900 DSP          |               |                                    |

Figure 8: Visualizing a DNA generated network and accelerator, which achieves a 75.6% accuracy on ImageNet and 42 FPS on a ZC706 FPGA, where the block definition follows (Wu et al., 2019a) with $k_3\times e_6$ denoting the building block associated with a kernel size of 3 and a channel expansion ratio of 6. X/Y, R/S, and C/K denote the dimensions of a convolution (see the bottom right figure), i.e., output feature width/height, kernel height/width, and input/output channel, respectively.

4.6 Visualizing DNA’s searched network and accelerator

To better understand the superior performance of DNA generated networks and accelerators, Fig. 8 visualizes a DNA generated network and accelerator on ImageNet, corresponding to the 16-bit DNA in Fig. 6 where it achieves an accuracy of 75.6% and a FPS of 42 under an FPGA DSP limit of 900 (the maximum one in a ZC706 board (Xilinx Inc., b)). First, we can see that the resulting network tends to select skip connections and adopt larger channel numbers, i.e., it trades the depth for the width to ensure both higher accuracy and hardware efficiency when being executed on the searched accelerator. Second, on the accelerator side, to maximize the potential throughputs, we observe that the generated accelerator employs a chunk-based pipeline micro-architecture, i.e., the whole network is partitioned and assigned to multiple pipelined chunks (sub-accelerators) in a non-consecutive manner which can be better tailored to optimize different layers’ specific dimensions as elaborated in (Shen et al., 2017). Furthermore, we observe that the chunks for the early layers in the network tend to parallelize more in the feature height/width dimensions, while the deeper layers parallelize the input/output channel dimensions, adapting to the dimensions which have more parallelism opportunities.

5 Conclusion

We propose DNA, a generic differentiable network-accelerator co-search framework for automatically searching for matched DNN structures and accelerators to maximize both task accuracy and hardware efficiency. DNA is made possible by: (1) a new co-search algorithm that can efficiently navigate over the prohibitively large joint network and accelerator search space to handle the large and discrete accelerator search space; and (2) a generic differentiable accelerator search engine which integrates gradient-based optimization and our constructed generic accelerator search space to enable simultaneous search of DNNs’ structures and accelerators; and (2) a generic differentiable accelerator search engine which integrates gradient-based optimization and our constructed generic accelerator search space to handle the large and discrete accelerator space. Extensive experiments and ablation studies based on FPGA measurements and ASIC synthesis validate that DNA generated networks and accelerators consistently outperform all the SOTA baselines in terms of both task accuracy and hardware efficiency (even better than expert-designed ones yet requiring a much reduced development time), while notably boosting the search efficiency. As such, DNA promises to greatly close the gap between rapidly growing DNNs and DNN accelerators’ slow development.
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