Efficient Modified Booth Multiplier for Signal Processing Applications

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Abstract

The two's complement approach plays a vital role in reducing Partial product Rows count in signed bit multiplier. In this paper proposed a multiplier which reduces the partial product rows by Modified Booth techniques with less delay. This high performance 2’s complement multiplier is used in embedded cores. This work was implemented in the Xilinx software and simulation results were obtained for the different applications. Applications such as FIR filter and Image processing requires high accuracy and smaller size multipliers. The image and filter interfacing is done with the help of MATLAB software.

Keywords: Image Processing, MATLAB, Modified Booth Technique, Partial Product, Xilinx

1. Introduction

The hardware effectiveness strongly depends on most cases of performance in computing multiplications in the multimedia, Three Dimensional graphics and signal processing applications, because the multiplication is most widely used these areas. This application field is having algorithm countersigned and it is given in the literature reference. In the great enactment embedded Digital Signal Processors have single cycle throughput and latency, which is the imperative building blocks. Multipliers must be greatly heightened to adequate within the prerequisite sequence time and power budgets. The short bit-width multipliers are the alternative fitting solicitation which supports the design of SIMD units. The elementary construction slabs use short bit-width multipliers. Complement multipliers like 2’S Complement multipliers less than 32 bits are being used vastly in Field Programmable Gate Arrays (FPGAs).

The rudimentary algorithm for multiplication is constructed on the familiar methodology. This progression has three core segments: 1) Generation of Partial Product terms (GPP), 2) Reduction of Partial Product terms and 3) Carry Propagation Adder stage. Each bit of the multiplier is taken and multiplied with the multiplicand terms to produce Partial product rows. Let the multiplier and multiplicand are X and Y then X×Y on n bits is having the arrangements like xn-1 …… x0and yn-1 …… y0 then ith row is generated by shifting left by one bit position with n bit zeros if yi=0 otherwise shift the X itself when yi is 1. Here n number of Partial Product rows is generated.

To decrease the quantity of partial product rows the Modified Booth Encoding Technique (MBET) is used, which also makes the GPP as faster one. Furthermore extensively used MBET is radix-4 technique for the reason that the number of PP rows abridged by half. This technique also provides very simple method to generation of multiples of multiplicand.

The 2’s complement n×n bit multiplication with radix-4 MBET was explained in detail, with maximum of [n/2]+1 rows of PP. The each row of PP has any one of the possible values from the followings: all 0’s (or) ±X(or) ±2X. The for merrow of the negative encoding is...
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retained simply by means of specific 2’s complement and sign extension prevention.

The reduction of PP is done by tree reduction method described in 9-13. The intermediary accumulation is not significant, upshot of this stage is an outcome epitomized in redundant carry-save method. The final addition is done the last two rows in non-redundant (single row) form.

| $Y_{2i+1}$ | $Y_{2i}$ | $Y_{2i-1}$ | General PP Rows |
|-----------|---------|------------|----------------|
| 0         | 0       | 0          | $(0)\times X$  |
| 0         | 0       | 1          | $(1)\times X$  |
| 0         | 1       | 0          | $(1)\times X$  |
| 0         | 1       | 1          | $(2)\times X$  |
| 1         | 0       | 0          | $-2\times X$   |
| 1         | 0       | 1          | $-1\times X$   |
| 1         | 1       | 0          | $-1\times X$   |
| 1         | 1       | 1          | $(0)\times X$  |

The planning of the sections is likely to be as follows: In Section 2, the MBET is fleetingly revised and investigated. In Section 3, the MBET reduction scheme for GPP is projected. In Section 4, the signal processing applications were discussed. As a final point, Section 5, deliver estimates and evaluations.

2. Modified Booth Recoded Multipliers

The radix-Z=2$^4$ MBET gives a reduction of (n/z) rows and it needs to generate all possible multiplication of X, like $-Z/2 \times X$ to $+Z/2 \times X$. By the radix-4 method the generation of $0$ or $\pm X$ or $\pm 2X$ is made much unpretentious form, as it needs just left shifting of bits in X. For the MBET with high radix will lead to produce more products of X.

The sign augmentation counteractive action technique to the 8 $\times$ 8 multiplier is given in the Figure 2. The neg signal is required in 2’s complement form (like neg0, neg1, neg2, and neg3 as in Figure 2) which is accumulated in Least Significant Bit Position of each PP row, if 2’s complement generation is needed. Hence for n $\times$ n bit multiplication, half of the n bit (n/2) PP are needed with maximum PP rows of (n/2)+1.

Since high regularity of the circuit layout for n$^2$ is accomplished in 4x2 compressors, it is extensively used. A further delay may be introduced for reduction of additional rows. If Wallace tree reduction is correctly used then this delay can be reduced. Still this necessitates a row of n Half Adders.

In the extraordinary enactment processor, when n is power of 2, this issue is very common incident that the critical path of multiplier has to fit within the clock period. The design for such multiplier is given in 2, for n of 16 bit maximum PP rows are 9 with 6 XOR gates having equivalent reduction. If the maximum rows are 8 then the tree reduction abridged to 1 XOR gate. On the other hand with regular layout, it is likely to use 4x2 adders for row height of 8 with 6 XOR gate delay in the reduced tree.

3. Reduction of PPR

It is to be noted that, to upturn the speed in generation of PP rows, parallel generation of first row along with the
bits in the last row as shown in the Figure 3. To accomplish this the primary row generation must be abridged.

The projected hint is specified here:

- The MSB bit generation of first row and the negation bit can be repeated 3 times as shown in Figure 3. For each row of MSB the separate negation bit is added at the last.

The remaining bits of first row except 3 MSB bits are generated by parallel circuitry.

The Parallel generation of remaining rows (Except 1st row) is done by the circuit shown in the Figure 4.

The steps 1 to 3 are engendered autonomously and hence it is faster than other PP generation method. Since the step 1 is generating faster first row, the critical path delay achieves the required goal line.

4. Applications

The extensively used multiplier unit applications such as specified underneath are the 2’s complement multipliers. The most important two applications are explained here.

- FIR filter
- Image processing (Histogram Equalization)

4.1 FIR Filter

FIR stands for Finite Impulse Response, which means that the response to an individual impulse is going to stop at some point in time. In processing of signal, FIR filter could be a channel whose drive reaction or reaction to any limited length information is of limited length, therefore of it settles to zero in limited time.

In a DT FIR filter with order value N, the highest half is associate degree Nphase circuit with N plus 1faucet. Every element delay may be a z operator in Z-transform notation. The yield y of a LTI scheme is decided by convolving its signaling x with its impulse response b. For a discrete-time FIR filter, the output may be a prejudiced total of this and a predetermined variety of forementioned tenets of the input.

The output is:

\[ y(n) = z_0 x(n) + z_1 x(n-1) + \ldots + z_N x(n-N) = \sum_{k=0}^{N} b_k x(n-k) \]
Where:
- The input signal is \( x[n] \),
- The output signal is \( y[n] \),
- Filter coefficients are \( b_i \),
- Filter order is \( N \); an Nth order filter has \( N+1 \) relations on the rightward aspect. The \( x[n-i] \) in these relations are normally remarked as faucets, supported the assembly of a nominated electric circuit that in several usage or square charts gives the deferred contributions to the augmentation operations. One may talk about a fifth request/6-tap channel, for instance.

### 4.2 Histogram Equalization

A duplicate histogram may be a sort of histogram which is a graphical illustration of the tonal dispersion amid an advanced picture. It plots the amount of pixels for each tonal worth. By gazing at the histogram for a chose picture a watcher will be ready to pick the entire tonal conveyance at a look.

![Figure 6. Histogram (red) and cumulative histogram (black) of an image.](image)

These ways get to regulate the image to form it easier to research or improve visual quality. The even hub of the diagram speaks to the tonal varieties, while the vertical pivot speaks to the measure of pixels in that particular tone. The left part of the even pivot speaks to the dark and dim ranges, the inside speaks to medium dim and along these lines the paw viewpoint speaks to lightweight and unadulterated white zones.

![Figure 7. Histogram (red) and cumulative histogram (black) of an image.](image)

Thus, the bar chart for an awfully dark image can have the bulk of its information points on the left aspect and center of the graph. Conversely, the bar chart for an awfully bright image with few dark areas and/or shadows can have most of its information points on the proper aspect and center of the graph.

Picture histogram is a unit blessing on a few chic advanced cameras. Picture takers will utilize them as partner degree help to show the dispersion of tones caught, and regardless of whether picture detail has been lost to smothered highlights or passed out shadows. Histogram deed could be a particular instance of a great deal of general class of histogram remapping techniques.

![Figure 8. Output in Binary.](image)

### 5. Results and Discussion

The simulation results for various modules are given. The code for all the modules are written in the VHDL language using Xilinx and simulated with Modelsim along with the RTL schematic and output waveforms. Output
6. Conclusion

The MBET with radix-4 for n x n bit 2’s complement multiplier reduces the PP rows by (n/2) and it is extended up to (n/2)+1 rows with sign extended bits. To reduce the delay in first row generation, special hardware circuitry is proposed in this paper. This special undecomposable circuitry assures that the faster generation of first PP rows and hence the delay is bounded within the standard methods. This will also guarantee the faster and parallel generation of PP rows.

The tree diminution is made easy to achieve both regularity and delay in the layout. This work is compared with the recent proposal by considering different applications such as FIR filter and Image processing to ensure the same performance is been delivered with no delay in multipliers. These applications are widely used in industries and the same can be applied to rectangular multiplication with minor modifications in MBET.

7. References

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