Parallel Performance of ARM ThunderX2 for Atomistic Simulation Algorithms

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Abstract—Atomistic simulation drives scientific advances in modern material science and accounts for a significant proportion of wall time on High Performance Computing facilities. It is important that algorithms are efficient and implementations are performant in a continuously diversifying hardware landscape. Furthermore, they have to be portable to make best use of the available computing resource.

In this paper we assess the parallel performance of some key algorithms implemented in a performance portable framework developed by us. We consider Molecular Dynamics with short range interactions, the Fast Multipole Method and Kinetic Monte Carlo. To assess the performance of emerging architectures, we compare the Marvell ThunderX2 (ARM) architecture to traditional x86_64 hardware made available through the Azure cloud computing service.

Index Terms—ARM, ThunderX2, parallel, Molecular Dynamics, Fast Multipole Method, Kinetic Monte Carlo

I. INTRODUCTION

High performance computing (HPC) hardware, which until recently has been dominated by Intel (CPU) and Nvidia (GPU) chipsets, is undergoing a rapid diversification. This is particularly evident in accelerators where Intel, AMD and Nvidia have been joined by competitors such as Graphcore and Google’s TPU cloud service. In the CPU space a resurgent AMD EPYC processor has made market share gains, while ARM is emerging as a genuine contender with the Marvell ThunderX2 processor which powers the UK Tier-2 HPC Isambard cluster (run by GW4 and the Met Office), and Amazon’s Graviton2 chip, which is another ARM offering. Particularly keenly anticipated has been Fujitsu’s A64FX processor which powers the new Fugaku supercomputer that has taken the top spot in the Top500 list and 4th place in the Green500 list at the time of writing.

The arrival of Fugaku also marks a significant step towards exascale which is seeing significant research investment globally. Programmes such as the Exascale Computing Project (US), the European High-Performance Computing Joint Undertaking (EU) and ExCALIBUR (UK) are exploring hardware and software approaches needed to attain and exploit exascale. One particularly promising approach are domain specific languages which allow the automatic generation of performant code for a wide range of architectures. The performance portable molecular dynamics (PPMD) framework for molecular simulation, developed in our group, is an example of this.

To assess the capabilities of PPMD on a range of architectures, we present a performance comparison of three relevant algorithms and models implemented in PPMD. We compare traditional HPC architectures based on Intel Skylake, AMD Naples/Rome with novel ARM hardware consisting of Marvell ThunderX2 CPUs.

II. BACKGROUND

Computational modelling has become firmly established as a third approach to complement theory and experiments. Over many years of research a range of algorithms have been developed by the scientific community to simulate processes that occur in materials. These methods have been modified and extended to best leverage the available computing hardware. In this section we introduce the three different algorithms studied in this paper and discuss the implementations that we used to compare the performance and parallel efficiency on four different chip architectures.

A. Short-ranged Molecular Dynamics

The first method which we investigated is an important component of classical Molecular Dynamics (MD) calculations with short range interactions. As a representative model system we consider liquid Argon, which can be modelled by a large number $N$ of particles contained in cuboid domain with periodic boundary conditions. These particles interact through a pairwise potential, which is a function of the positions of the two interacting particles. At each step of a MD simulation the forces exerted on each atom by all other atoms are computed. These forces are used to increment the momentum and update the position of the atoms by applying Newton’s equations of motion.

For our numerical experiment we use the Lennard-Jones interatomic potential

$$V_{LJ}(r) = 4\epsilon \left[ \left( \frac{\sigma}{r} \right)^{12} - \left( \frac{\sigma}{r} \right)^{6} \right], \quad (1)$$

where $r$ is the interatomic distance between two interacting atoms. The strength and shape of the potential are described...
by the constants $\epsilon$ and $\sigma$, which depend on the physics of the system under study. For the rest of the paper we implicitly assume that all quantities are measured in suitable physical units. Note that this potential and the corresponding force can be evaluated with 1 division and 25 additions/multiplications which is computationally cheap in comparison to alternative potentials. For example, evaluating the Buckingham potential [3] involves square root and exponential operations.

In principle the computation of all $N(N-1)/2$ pairwise interactions is an $O(N^2)$ operation. To reduce the computational cost the interactions are typically approximated with a potential that is truncated at a given interatomic distance $r_c$. In this case each particle only interacts with an on average fixed number of other particles which reduces the computational complexity to $O(N)$.

An implementation of this MD algorithm must perform two main operations efficiently. Firstly, all pairs of atoms that could be within $r_c$ of each other must be identified. Secondly, for each of those pairs of atoms the interatomic potential must be evaluated. Since evaluation of the potentials is typically an operation with high arithmetic intensity, it will benefit from vectorisation on modern chip hardware.

A common technique to identify all interacting pairs of atoms is to decompose the simulation domain into cells with a side length that is at least $r_c$ and only consider interactions with atoms in neighbouring cells. This domain decomposition (DD) allows parallelisation with a distributed memory approach. We use the Message Passing Interface (MPI) to distribute the simulation domain over MPI ranks. Since the neighbours of a particular atom are often stored on another MPI rank, each sub-domain is extended with a halo region. For PPMD this is described in detail in [4]. Note that efficient algorithms exist for the nearest neighbour communication between adjacent sub-domains [5].

Our implementation stores pairs of particles in a matrix based data structure, described by Rapaport [6], known as a neighbour list. This storage format is suitable for threaded shared memory environments such as CUDA and OpenMP.

The PPMD framework described in [1] exploits parallelism using MPI and OpenMP. Pairwise- and single-particle- operations are described in a Domain Specific Language (DSL) implemented in Python. Efficient C code is automatically generated for a range of target architectures.

### B. Long-ranged Molecular Dynamics

In addition to short-ranged forces, MD simulations of charged atoms must also consider long-range electrostatic interactions. In this case, the pairwise potential cannot be truncated at some fixed cutoff radius $r_c$. A variety of different algorithms exist [7]–[11] to compute these interactions with varying efficiency depending on the simulated system and computing hardware.

Here we use the Fast Multipole Method (FMM) [12], [13], which is an $O(N)$ algorithm, to compute long-ranged electrostatic interactions. In the FMM algorithm a hierarchical grid is constructed on the simulation domain and the centre of each cell on all levels is the origin of a “multipole” expansion or “local” expansion. The accuracy of the FMM depends on the number of terms used for these expansions.

At the start of the algorithm, multipole expansions of the charges in each of the cells on the finest level are constructed. These multipole expansions are recursively translated and combined in the upward pass of the FMM. In the downward pass multipole expansions are translated into local expansions which describe the potential field in the centre of the cell. At the end of the tree traversal the local expansion in each cell describes the electrostatic potential induced by all charged atoms outside that cell and its nearest neighbours. Finally, the electrostatic interactions between atoms in a cell and its nearest neighbours are computed by directly evaluating the pairwise Coulomb potential as discussed in the previous section.

An efficient implementation of the tree traversal must consider the translation and combination of expansions between cells in the grid hierarchy and manage distribution of work over CPU cores. A more in-depth discussion of our FMM implementation is provided in [4].

### C. kinetic Monte Carlo

Kinetic Monte Carlo (KMC) can be used to investigate time dependent phenomena such as charge transport in semiconductors. In a reaction free KMC [14]–[16] simulation of a photovoltaic cell or battery, $N$ charged atoms can hop between adjacent sites of a (generally unstructured) lattice. At each step hops are considered for all mobile charges in the system but only one hop is accepted with a probability that is proportional to the so called “hopping rate” or “propensity”. In materials such as semi-conductors, the hopping rates are a function of the change in electrostatic energy of the moving charge.

In [17] we developed a new algorithm to perform the computation of these differences in electrostatic energy with $O(N)$ computational complexity by using the local expansions described in the FMM algorithm. KMC, along with our electrostatic algorithm, is very well suited to parallel architectures: Firstly, differences in electrostatic energy for all potential moves can be computed independently. Secondly, when a move is accepted all local expansions can be updated to reflect the accepted move in parallel. Only the final accepted move as to be communicated between all processors.

### III. Setup and Results

#### A. Platforms and Configuration

We used two HPC facilities to assess the performance of PPMD. An Azure based platform of traditional x86_64 hardware and the UK Tier 2 Isambard facility. This allows comparison between traditional x86 architectures and novel ARM processors while using state-of-the-art hardware. In Table 1 the node configurations on both machines are provided.

On the Azure platform Intel MPI 2018.4 and the Intel Compiler 19.0.5 were used. As Isambard system is a Cray XC50 system we used Cray mpich 7.7 along with the GNU compiler version 9.2.0. The Cray compiler was not used for the Cray compiler cannot be called on compute nodes which
TABLE I
OVERVIEW OF NODE ARCHITECTURES. PEAK FLOATING POINT RATES (RPEAK) ARE COMPUTED ASSUMING THE LISTED CLOCK SPEED AND FLOPS/CYCLE. NUMERICAL EXPERIMENTS WERE PERFORMED USING THE LISTED NUMBER OF MPI RANKS AND OPENMP THREADS FOR EACH NODE.

| Platform | Processor          | Core Count | Clock Speed (GHz) | FLOPs/cycle | Bandwidth (GB/s) | Rpeak (TFlops) | MPI rank count | OpenMP thread count |
|----------|--------------------|------------|-------------------|-------------|------------------|----------------|----------------|-------------------|
| Azure    |                    |            |                   |             |                  |                |                |                   |
| HC44     | Intel Platinum 8168| 44         | 2.1               | 8           | 318              | 1.08           | 8              | 8                 |
| HB60     | AMD EPYC 7551      | 60         | 2.0               | 8           | 263              | 0.96           | 15             | 4                 |
| HB120    | AMD EPYC 7V12      | 120        | 2.45              | 16          | 350              | 4.70           | 30             | 4                 |

The potential was truncated at a cutoff radius \( r_c \) of 2.5 and we set \( \sigma = 1, \epsilon = 1 \). The neighbour list was rebuilt at least every 10 steps with a 2.75 cutoff. In Figure 1 we plot the time taken per simulation step, for each of our test platforms, as the number of nodes is increased while keeping \( N \) fixed in a strong scaling experiment.

This particular benchmark is tailored to reach a strong-scaling limit at a relatively small node count. In this limit the number of atoms per CPU core is relatively low (<1000) hence, at this density and cutoff, the cost of potential evaluations is small in comparison to bookkeeping and communication. In particular, this benchmark computes and communicates (MPI_Allreduce) the potential and kinetic energy at each step.

Inspection of binaries reveals that on the Intel and AMD processors the Intel compiler produced AVX2 instructions. On Isambard, GCC did not vectorise the loops that evaluate the potential. To investigate further, we modified the generated code that evaluates the pairwise potential to include OpenMP SIMD pragmas and recompiled using the ARM compiler version 20.1. SIMD instructions were emitted and the single node time per step improved to 0.081s from 0.091s.

For the FMM benchmark (Section II-B), \( N = 4 \times 10^5 \) atoms were arranged in a cubic lattice with spacing \( \alpha = 6.6 \). To prevent oppositely charged atoms from collapsing onto each other a repulsive short-range Lennard-Jones potential with cutoff \( r_c = 4.0 \) was added. We configured the FMM with ten expansion terms and six levels in the hierarchical grid. In Figure 2 we plot the time taken per simulation step, for each of our test platforms, as the number of nodes is increased while keeping \( N \) fixed in a strong scaling experiment.

We observe that for the FMM benchmark GCC produced vector instructions for both the direct interactions and for the expensive multipole to local expansion operations. In our FMM implementation the number of processors that can do useful work on each grid level in the upward and downward pass is limited by the total number of cells on that level. If the number of cores is greater than the number of cells on a level then some cores will be idle, which impacts parallel scaling.
Finally, for the KMC benchmark (Section II-C), \( N = 10^6 \) charged atoms were placed on a cubic lattice. At each lattice site atoms may hop in one of six directions assuming that the destination site is not occupied. Consequently, at each step approximately \( 7 \cdot 10^6 \) energy evaluations are performed. The electrostatic solver was configured to use 12 expansion terms which, as is described in detail in [17], is sufficient to achieve a mean relative error in the potential energy of \( \approx 10^{-5} \). In Figure 3 we plot the time taken per step for each of our test platforms as the number of nodes is increased while keeping \( N \) fixed in a strong scaling experiment.

![Figure 3. KMC strong scaling experiment. Time per step plotted against number of nodes for each HPC platform. Dashed black indicates ideal scaling.](image)

As expected, since the algorithm can be parallelised over particles, the KMC benchmark scales very well as the ratio of computation to communication is high. The only communicated data are the details for the accepted move. Even for the smallest sub-domains (at the largest node counts) there is enough computational work for the communication time to be negligible. Inspection of binaries reveals that GCC did vectorise some expensive loops, such as bookkeeping operations. However not all performance critical loops were vectorised. We recompiled certain expensive operations with the ARM compiler, which produced vector instructions, but did not observe a performance improvement.

IV. CONCLUSION

In this paper we presented strong scaling results for the implementation of three algorithms highly relevant in atomistic simulation. All algorithms were implemented in our performance portable PPMD framework. In terms of strong scaling efficiency, the Isambard platform performed competitively in comparison to the Azure platform. In our FMM benchmark, which were using a very established compiler. The results presented here show that further development of our code generation system (in collaboration with the compiler developers) is necessary to implement algorithms which are more efficient on the ARM hardware. Future work should investigate, from a microarchitecture standpoint, the performance difference between the HB60 cores and the ThunderX2 cores which theoretically both perform 8FLOPs/cycle.

ACKNOWLEDGMENTS

This project has received funding from the European Unions Horizon 2020 research and innovation programme under grant agreements No 646176 and No 824158. This research made use of the Balena High Performance Computing (HPC) Service at the University of Bath and the Isambard UK National Tier-2 HPC Service (http://gw4.ac.uk/isambard/). Isambard is operated by GW4 and the UK Met Office, and funded by EPSRC (EP/P020224/1). We thank the University of Bath ARC team and Red Oak Consulting for providing their expertise when running on the Azure platform.

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