Edgeless and Purely Gate-Defined Nanostructures in InAs Quantum Wells

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Nanostructures in InAs quantum wells have so far remained outside of the scope of traditional microfabrication techniques based on etching. This is due to parasitic parallel conduction arising from charge carrier accumulation at the physical edges of samples. Here we present a technique which enables the realization of quantum point contacts and quantum dots in two-dimensional electron gases of InAs purely by electrostatic gating. Multiple layers of top gates separated by dielectric layers are employed. Full quantum point contact pinch-off and measurements of Coulomb-blockade diamonds of quantum dots are demonstrated.

InAs is a semiconductor material of strong spin-orbit interaction, low effective mass and large g-factor, for which it has gained recent interest. It arises, for instance, from proposals for investigating topological phenomena. One-dimensional InAs nanowires combined with superconductors are expected to be a host system for Majorana physics1–5. Composite quantum wells were proposed to show the quantum spin Hall effect6–11. For potential future applications of topological quantum computation which require upscaling to a large number of qubits, it would be advantageous to start from a 2-dimensional structure12–14, which would severely simplify integration. Therefore, developing functional nanostructures made from InAs two-dimensional electron gases is a natural starting point. Control over Coulomb islands or nanostructures is paramount for these kinds of experiments.

Yet, up to date, convincing nanostructures in InAs two-dimensional electron gases have not been realized with the exception of a few attempts with trench-etched quantum point contacts15–17. We believe that the reason lies in the trivial edge conduction recently reported in InAs18,19 and InAs/GaSb quantum wells20–22. However, in InAs nanowires this problem seems not to occur and exquisite control over single and multi-dot systems has been reported23. For InAs, the Fermi level is pinned in the conduction band at the surface24,25. The origin of this Fermi level pinning is not clear yet, but possible reasons are discussed in Refs. 18 and 20.

The effect of this Fermi-level pinning is illustrated in Figs. 1(a) and (b). The top panel of Fig. 1(a) shows an InAs two-dimensional electron gas with an etched mesa, the bottom panel its band edge diagram as a function of the real space coordinate x. The edges of the etched mesa form a surface, where the Fermi level is pinned in the conduction band. When the bulk of the two-dimensional electron gas is populated by carriers, this does not cause any problems. However, if the gate pushes the Fermi level into the band gap in the bulk [Fig. 1(b)], the Fermi level remains pinned in the conduction band at the edges. This causes electron accumulation24,25 in the triangular potential well created at the edges [indicated in red in Fig. 1(b)]. When measuring transport through such a structure (into the plane of Fig. 1), these accumulated electrons form a parasitic channel which conducts in parallel, as they are not or only weakly affected by the gate20,26. The standard semiconductor nanofabrication approach is therefore not feasible in this case.

FIG. 1. (a) InAs two-dimensional electron gas (red dashed line) confined by the edges of an etched mesa (top), and corresponding band edge diagram (bottom). (b) Same structures as in (a), but with a gate (yellow) on top charged with a negative voltage, thus depleting the two-dimensional electron gas. Due to the pinned Fermi level, electrons accumulate in the triangular potential well at the edges (shaded red in band edge diagram), leading to trivial edge states (red dots in top panel). (c) Schematic view of the cross-section of the heterostructure and the fabricated layer sequence. Ohmic contacts are colored in orange, the frame gate in yellow, and the fine gates in light red. (d) Schematic top view of the sample showing the lateral structure consisting of Ohmic contacts in an exemplary 4-point configuration, the rectangular frame gate, and fine gates defining a quantum dot. The color code is the same as in (c).

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In this paper, we propose a gate geometry that circumvents the parasitic edge conduction. We use a heterostructure containing a 15 nm InAs quantum well with an electron density \( n = 5.5 \times 10^{-11} \text{ cm}^{-2} \) and a mobility of \( \mu = 1 \times 10^5 \text{ cm}^2/\text{Vs} \) in-between two 50 nm AlSb barriers with a 3 nm GaSb capping layer. The heterostructure composition below the lower barrier is identical to the one used in Ref. 19. The layer and fabrication sequence explained in the following is depicted in the schematic cross-section of the device shown in Fig. 1(c) and in the schematic top view displayed in Fig. 1(d). In a first step, Ohmic contacts of (Ge/Au/Ni/Au) were deposited. Then, a 30 nm dielectric layer of Al\(_2\)O\(_3\) was deposited by atomic layer deposition at a temperature of 150 °C.

In the next we deposited a frame-shaped gate of Ti/Au (10/70 nm) on the outside of the Ohmic contacts, which will be referred to as frame gate in the following. The frame gate is paramount to circumventing the trivial edge conduction. Upon depletion of the electron gas underneath, the inner part of the sample containing the Ohmic contacts without a physical edge or surface at which electrons could accumulate, is decoupled from the outside part.

The deposition of a second 30 nm Al\(_2\)O\(_3\) film by atomic layer deposition allows for depositing fine Ti/Au (5/25 nm) gates forming a nanostructure on top [see Fig. 2(a)], employing electron beam lithography and metal evaporation. The nanostructures measured in this manuscript are a quantum point contact consisting of a split gate with 200 nm separation and a quantum dot formed by a semicircular top gate and three finger gates forming a right and left barrier and a plunger gate. An optical and scanning electron micrograph of a finished sample are shown in Fig. 2(a).

We first characterize the frame gate in order to show that it completely disconnects the two-dimensional electron gas bulk from the boundaries. These measurements have been done at \( T = 1.3 \text{ K} \) using AC lock-in techniques. We apply a bias voltage between a contact on the outside part of the two-dimensional electron gas [not shown in Fig. 1(d)] and the contacts on the inside. The results can be seen in Fig. 2(b) where we plot the conductance (blue curve and axis) and the resistance (red curve and axis) as a function of \( V_{\text{FG}} \), the voltage applied to the frame gate. At \( V_{\text{FG}} = 0.8 \text{ V} \), the conductance drops to zero as the two-dimensional electron gas underneath the frame gate is fully depleted. This voltage agrees with the expected depletion voltage taking into account the capacitance and electron density of the structure. At the same voltage, the resistance increases rapidly up to \( 10^7 \Omega \), which was the maximum detectable resistance in our measurement setup. From this result we deduce that the regions of the two-dimensional electron gas in- and outside the frame gate are sufficiently decoupled from each other. Together with a full pinch-off in a quantum point contact measurement this will prove that our gate geometry circumvents the parasitic trivial edge conduction.

![Fig. 2](image_url)

**FIG. 2.** (a) Optical (left, center) and scanning electron micrograph (right) of a sample similar to the quantum dot sample used in this paper. (b) Conductance (blue) and resistance (red) between two contacts on the in- and outside of the frame gate as a function of voltage applied to the frame gate. (c) Conductance through a quantum point contact as a function of the voltage applied symmetrically to the split gates.

In order to investigate whether this is the case, we measure a split gate quantum point contact in a 4-terminal geometry using AC lock-in techniques at \( T = 1.3 \text{ K} \). In Fig. 2(c) we show the conductance \( G \) as a function of the voltage \( V_{\text{QPC}} \) applied to both quantum point contact gates. Full pinch-off can be reached at \( V_{\text{QPC}} = -1.95 \text{ V} \), which demonstrates that there is no parasitically conducting channel present underneath the gates. Quantized conductance steps or a 0.7-anomaly are not visible, due to the resonances likely caused by disorder in the channel.

In the following we investigate another sample with a frame gate. It contains finger gates for forming a quantum dot as seen in the scanning electron micrograph in the right panel of Fig. 2(a). These measurements were performed in a dilution refrigerator with a base temperature of \( T = 60 \text{ mK} \) using AC lock-in techniques in a 2-terminal measurement. In a first step, we demonstrate that also the narrower quantum dot gates fully pinch off the two-dimensional electron gas. For this purpose, we apply a voltage \( V_{\text{all}} \) to all four quantum dot gates [colored red in the schematic of the gate layout in the inset of Fig. 3(a)] and operate the device as a quantum point contact. As seen in Fig. 3(a) the electron gas can be pinched off also in this geometry. Again resonances caused by disorder appear on the conductance curve.

We now tune the gates such that we form a small metallic island in-between the gates. We apply a voltage \( V_{\text{FG}} \) to the plunger gate to change the occupation of the quantum dot while measuring its conductance \( G \). The result of this measurement is displayed in Fig. 3(b),
where the red gate of the inset indicates the gate being swept. Sharp, evenly spaced conductance resonances indicate charging the quantum dot with single electrons.

In Fig. 3(c) we show a color plot of the quantum dot conductance while varying the applied DC source-drain bias voltage $V_{SD}$ (x-axis) in addition to $V_{PG}$ (y-axis). Coulomb-blockade diamonds are visible and from their extent in $V_{SD}$ we can determine a charging energy $E_C \approx 1$ meV which agrees with estimations based on the capacitance of the island. This is an approximate value, as the outlines of the Coulomb diamonds are not very sharp and they increase in size for more negative $V_{PG}$. From the size of the quantum dot and the electron density in the wafer we estimate the number of electrons in the dot to be $N \approx 400$. Neither excited states nor signatures of single particle levels are visible.

In Fig. 3(d), the conductance of the quantum dot is shown as a function of the voltages $V_{LB}$ and $V_{RB}$ applied to the left and the right barrier, respectively, in order to elucidate the tunability of the system. Charging both gates to more negative voltages we pass multiple Coulomb resonances, indicating that electrons are being expelled from the dot. The overall conductance decreases when both voltages are more negative, which is a sign of closing the tunnel barriers and therefore signals standard quantum dot operation.

Using the measurements Figures 2(c) and 3(d) we determine the lever arms of the quantum dot gates to be $\alpha_{PG} = 0.05$ for the plunger gate, $\alpha_{LB} = 0.08$ for the left barrier, and $\alpha_{RB} = 0.06$ for the right barrier, respectively. These values are within expectations considering the distance of the two-dimensional electron gas from the gates and the geometry of the structure. This indicates standard quantum dot operation in InAs quantum wells, like in technologically more mature two-dimensional electron gas systems like GaAs and Si. Such a performance has not been demonstrated before to the best of our knowledge.

In conclusion, we demonstrated a technique which allows operating nanostructures such as quantum point contacts and quantum dots in InAs quantum wells by circumventing parasitic trivial edge conduction. This was achieved by separating the sample edge from the bulk of the two-dimensional electron gas with the frame gate. Quantitative analysis of the nanostructure conductance is still severely limited by disorder. It may be overcome by improving material quality, which is independent of the device geometry introduced here. The frame gate could in principle also be applied to other narrow-band material systems that suffer from similar undesired edge conduction or Fermi-level pinning issues.

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