Abstract—Triangle counting (TC) is a fundamental problem in graph analysis and has found numerous applications, which motivates many TC acceleration solutions in the traditional computing platforms like GPU and FPGA. However, these approaches suffer from the bandwidth bottleneck because TC calculation involves a large amount of data transfers. In this paper, we propose to overcome this challenge by designing a TC accelerator utilizing the emerging processing-in-MRAM (PIM) architecture. The true innovation behind our approach is a novel method to perform TC with bitwise logic operations (such as AND), instead of the traditional approaches such as matrix computations. This enables the efficient in-memory implementations of TC computation, which we demonstrate in this paper with computational Spin-Transfer Torque Magnetic RAM (STT-MRAM) arrays. Furthermore, we develop customized graph slicing and mapping techniques to speed up the computation and reduce the energy consumption. We use a device-to-architecture co-simulation framework to validate our proposed TC accelerator. The results show that our data mapping strategy could reduce 99\% of the computation and 72\% of the memory WRITE operations. Compared with the existing GPU or FPGA accelerators, our in-memory accelerator achieves speedups of 9× and 23.4×, respectively, and a 20.6× energy efficiency improvement over the FPGA accelerator.

Index Terms—Triangle Counting, Processing-In-MRAM, Architecture, Data Mapping

I. INTRODUCTION

Triangles are the basic substructure of networks and play critical roles in network analysis. Due to the importance of triangles, triangle counting problem (TC), which counts the number of triangles in a given graph, is essential for analyzing networks and generally considered as the first fundamental step in calculating metrics such as clustering coefficient and transitivity ratio, as well as other tasks such as community discovery, link prediction, and Spam filtering [1]. TC problem is not hard but they are all memory bandwidth intensive thus time-consuming. As a result, researchers from both academia and industry have proposed many TC acceleration methods ranging from sequential to parallel, single-machine to distributed, and exact to approximate. From the computing hardware perspective, these acceleration strategies are generally executed on CPU, GPU or FPGA, and are based on Von-Neumann architecture [1–3]. However, due to the fact that most graph processing algorithms have low computation-memory ratio and high random data access patterns, there are frequent data transfers between the computational unit and memory components which consumes a large amount of time and energy.

In-memory computing paradigm performs computation where the data resides. It can save most of the off-chip data communication energy and latency by exploiting the large internal memory inherent bandwidth and inherent parallelism [4–5]. As a result, in-memory computing has appeared as a viable way to carry out the computationally-expensive and memory-intensive tasks [6–7]. This becomes even more promising when being integrated with the emerging non-volatile STT-MRAM memory technologies. This integration, called Processing-In-MRAM (PIM), offers fast write speed, low write energy, and high write endurance among many other benefits [8–9].

In the literature, there have been some explorations on in-memory graph algorithm accelerations [10–13], however, existing TC algorithms, including the intersection-based and the matrix multiplication-based ones, cannot be directly implemented in memory. For large sparse graphs, highly efficient PIM architecture, efficient graph data compression and data mapping mechanisms are all critical for the efficiency of PIM accelerations. Although there are some compression methods for sparse graph, such as compressed sparse column (CSC), compressed sparse row (CSR), and coordinate list (COO) [10], these representations cannot be directly applied to in-memory computation either. In this paper, we propose and design the first in-memory TC accelerator that overcomes the above barriers. Our main contributions can be summarized as follows:

- We propose a novel TC method that uses massive bitwise operations to enable in-memory implementations.
- We propose strategies for data reuse and exchange, and
data slicing for efficient graph data compression and mapping onto in-memory computation architectures.

- We build a TC accelerator with the sparsity-aware processing-in-MRAM architecture. A device-to-architecture co-simulation demonstrates highly encouraging results.

The rest of the paper is organized as follows: Section II provides some preliminary knowledge of TC and in-memory computing. Section III introduces the proposed TC method with bitwise operations, and Section IV elaborates a sparsity-aware processing-in-MRAM architecture which enables highly efficient PIM accelerations. Section V demonstrates the experimental results and Section VI concludes.

II. PRELIMINARY

A. Triangle Counting

Given a graph, triangle counting (TC) problem seeks to determine the number of triangles. The sequential algorithms for TC can be classified into two groups. In the matrix multiplication based algorithms, a triangle is a closed path of length three, namely a path of three vertices begins and ends at the same vertex. If A is the adjacency matrix of graph G, \( A^3[i][i] \) represents the number of paths of length three beginning and ending with vertex \( i \). Given that a triangle has three vertices and will be counted for each vertex, and the graph is undirected (that is, a triangle \( i \rightarrow p \rightarrow q \rightarrow i \) will be also counted as \( i \rightarrow q \rightarrow p \rightarrow i \)), the number of triangles in \( G \) can be obtained as \( \text{trace}(A^3)/6 \), where \( \text{trace} \) is the sum of elements on the main diagonal of a matrix. In the set intersection based algorithms, it iterates over each edge and finds common elements from adjacency lists of head and tail nodes. A lot of CPU, GPU and FPGA based optimization techniques have been proposed \([1-3]\). These works show promising results of accelerating TC, however, these strategies all suffer from the performance and energy bottlenecks brought by the significant amount of data transfers in TC.

B. In-Memory Computing with STT-MRAM

STT-MRAM is a promising candidate for the next generation main memory because of its properties such as near-zero leakage, non-volatility, high endurance, and compatibility with the CMOS manufacturing process \([9]\). In particular, prototype STT-MRAM chip demonstrations and commercial MRAM products have been available by companies such as Everspin and TSMC. STT-MRAM stores data with magnetic-resistances instead of conventional charge based store and access. This enables MRAM to provide inherent computing capabilities for bitwise logic with minute changes to peripheral circuitry \([9][13]\).

As the left part of Fig. 1 shows, a typical STT-MRAM bit-cell consists of an access transistor and a Magnetic Tunnel Junction (MTJ), which is controlled by bit-line (BL), word-line (WL) and source-line (SL). The relative magnetic orientations of pinned ferromagnetic layer (PL) and free ferromagnetic layer (FL) can be stable in parallel (P state) or anti-parallel (AP state), corresponding to low resistance \( (R_{AP}) \) and high resistance \( (R_{AP} > R_{P}) \), respectively. READ operation is done by enabling WL signal, applying a voltage \( V_{\text{read}} \) across BL and SL, and sensing the current that flows \( (I_{P} \text{ or } I_{AP}) \) through the MTJ. By comparing the sense current with a reference current \((I_{\text{ref}})\), the data stored in MTJ cell (logic ‘0’ or logic ‘1’) could be readout. WRITE operation can be performed by enabling WL, then applying an appropriate voltage \((V_{\text{write}}) \) across BL and SL to pass a current that is greater than the critical MTJ switching current. To perform bitwise logic operation, as demonstrated in the right part of Fig. 1 by simultaneously enabling WL\( i \) and WL\( j \), then applying \( V_{\text{read}} \) across BL\( k \) and SL\( k \) \((k \in [0, n-1])\), the current that feeds into the \( k \)-th sense amplifier (SA) is a summation of the currents flowing through \( MT.I_{i,k} \) and \( MT.I_{j,k} \), namely \( i_{i,k} + I_{j,k} \). With different reference sensing current, various logic functions of the enabled word line can be implemented.

III. TRIANGLE COUNTING WITH BITWISE OPERATIONS

In this section, we seek to perform TC with massive bitwise operations, which is the enabling technology for in-memory TC accelerator. Let \( A \) be the adjacency matrix representation of a undirected graph \( G(V,E) \), where \( A[i][j] \in \{0,1\} \) indicates whether there is an edge between vertices \( i \) and \( j \). If we compute \( A^2 = A \ast A \), then the value of \( A^2[i][j] \) represents the number of distinct paths of length two between vertices \( i \) and \( j \). In the case that there is an edge between vertex \( i \) and vertex \( j \), and \( i \) can also reach \( j \) through a path of length two, where the intermediate vertex is \( k \), then vertices \( i, j, \) and \( k \) form a triangle. As a result, the number of triangles in \( G \) is equal to the number of non-zero elements \( (\text{nnz}) \) in \( A \cap A^2 \) (the symbol ‘\( \cap \)’ defines element-wise multiplication here), namely

\[
TC(G) = \text{nnz}(A \cap A^2)
\]  

Since \( A[i][j] \) is either zero or one, we have

\[
(A \cap A^2)[i][j] = \begin{cases} 
0, & \text{if } A[i][j] = 0; \\
A^2[i][j], & \text{if } A[i][j] = 1. 
\end{cases}
\]  

According to Equation (2),

\[
\text{nnz}(A \cap A^2) = \sum \sum_{A[i][j]=1} A^2[i][j]
\]

Because the element in \( A \) is either zero or one, the bitwise Boolean AND result is equal to that of the mathematical multiplication, thus
\[ A^2[i,j] = \sum_{k=0}^{n} A[i][k] \cdot A[k][j] = \sum_{k=0}^{n} AND(A[i][k], A[k][j]) \]
\[ = BitCount(AND(A[i][*], A[*][j]^T)) \]

in which BitCount returns the number of ‘1’s in a vector consisting of ‘0’ and ‘1’, for example, BitCount\( (0110) = 2 \).

Combining equations (1), (3) and (4), we have
\[ TC(G) = BitCount(AND(A[i][*], A[*][j]^T)), \]
in which \( A[i][j] = 1 \)

Therefore, TC can be completed by only AND and BitCount operations (massive for large graphs). Specifically, for each non-zero element \( A[i][j] = 1 \), the \( i \)-th row \( (R_i = A[i][*]) \) and the \( j \)-th column \( (C_j = A[*][j]^T) \) are executed AND operation, then the AND result is sent to a bit counter module for accumulation. Once all the non-zero elements are processed as above, the value in the accumulated BitCount is exactly the number of triangles in the graph.

![Graph Data](image)

Fig. 2: Demonstrations of triangle counting with AND and BitCount bit-wise operations.

Fig. 2 demonstrates an illustrative example for the proposed TC method. As the left part of the figure shows, the graph has four vertices, five edges and two triangles \((0 - 1 - 2 - 0 \text{ and } 1 - 2 - 3 - 1)\), and the adjacency matrix is given. The non-zero elements in A are \( A[0][1], A[0][2], A[1][2], A[1][3], \) and \( A[2][3] \). For \( A[0][1] \), row \( R_0 = 0110 \) and column \( C_1 = 1000 \) are executed with AND operation, then the AND result ‘0000’ is sent to the bit counter and gets a result of zero. Similar operations are performed to other four non-zero elements. After the execution of the last non-zero element \( A[2][3] \) is finished, the accumulated BitCount result is two, thus the graph has two triangles.

The proposed TC method has the following advantages. First, it avoids the time-consuming multiplication. When the operation data are either zero or one, we can implement the multiplication with AND logic. Second, the proposed method does not need to store the intermediate results that are larger than one (such as the elements in \( A^2 \)), which are cumbersome to store and calculate. Third, it does not need complex control logic. Given the above three advantages, the proposed TC method is suitable for in-memory implementations.

IV. SPARSITY-AWARE PROCESSING-IN-MRAM ARCHITECTURE

To alleviate the memory bottleneck caused by frequent data transfers in traditional TC algorithms, we implement an in-memory TC accelerator based on the novel TC method presented in the previous section. Next, we will discuss several dataflow mapping techniques to minimize space requirements, data transfers and computation in order to accelerate the in-memory TC computation.

A. Data Reuse and Exchange

Recall that the proposed TC method iterates over each non-zero element in the adjacency matrix, and loads corresponding rows and columns into computational memory for AND operation, followed by a BitCount process. When the size of the computational memory array is given, it is important to reduce the unnecessary space and memory operations. We observe that for AND computation, the non-zero elements in a row reuse the same row, and the non-zero elements in a column reuse the same column. The proposed data reuse mechanism is based on this observation.

Assume that the non-zero elements are iterated by rows, then the current processed row only needs to be loaded once, at the same time the corresponding columns are loaded in sequence. Once all the non-zero elements in a row have been processed, this row will no longer be used in future computation, thus we can overwrite this row by the next row to be processed. However, the columns might be used again by the non-zero elements from the other rows. Therefore, before loading a certain column into memory for computation, we will first check whether this column has been loaded, if not, the column will be loaded to a spare memory space. In case that the memory is full, we need to select one column to be replaced with the current column. We choose the least recently used (LRU) column for replacement, and more optimized replacement strategy could be possible.

As demonstrated in Fig. 2 in step 1 and step 2, the two non-zero elements \( A[0][1] \) and \( A[0][2] \) of row \( R_0 \) are processed respectively, and corresponding columns \( C_1 \) and \( C_2 \) are loaded to memory. Next, while processing \( A[1][2] \) and \( A[1][3] \), \( R_1 \) will overlap \( R_0 \) and reuse existing \( C_2 \) in step 3, and load \( C_3 \) in step 4. In step 5, to process \( A[2][3] \), \( R_1 \) will be overlapped by \( R_2 \), and \( C_3 \) is reused. Overlapping the rows and reusing the columns can effectively reduce unnecessary space utilization and memory WRITE operations.

B. Data Slicing

To utilize the sparsity of the graph to reduce the memory requirement and unnecessary computation, we propose a data slicing strategy for graph data compression.

Assume \( R_i \) is the \( i \)-th row, and \( C_j \) is the \( j \)-th column of the adjacency matrix \( A \) of graph \( G(V,E) \).
Given that most graphs are highly sparse, the needed space to store the graph can be trivial. Moreover, the proposed format of compressed graph data is friendly for directly mapping onto the computational memory arrays to perform in-memory logic computation.

**C. Processing-In-MRAM Architecture**

Fig. 4 demonstrates the overall architecture of processing-in-MRAM. The graph data will be sliced and compressed, and represented by the valid slice index and corresponding slice data. According to the valid slice indexes in the data buffer, we load the corresponding valid slice pairs into computational STT-MRAM array for bitwise computation. The storage status of STT-MRAM array (such as which slices have been loaded) is also recorded in the data buffer and utilized for data reuse and exchange.

As for the computational memory array organization, each chip consists of multiple Banks and works as computational array. Each Bank is comprised of multiple computational memory sub-arrays, which are connected to a global row decoder and a shared global row buffer. Read circuit and write driver of the memory array are modified for processing bitwise logic functions. Specifically, the operation data are all stored in different rows in memory arrays. The rows associated with operation data will be activated simultaneously for computing. Sense amplifiers are enhanced with AND reference circuits to realize either READ or AND operations. By generating $R_{ref,AND} \in (R_{pP, R_{pAP}})$, the output by the sense amplifier is the AND result of the data that is stored in the enabled WLs.

**Algorithm 1: TCIM: Triangle Counting with Processing-In-MRAM Architecture.**

**Input:** Graph $G(V,E)$.

**Output:** The number of triangles in $G$, $TC_G = 0$.

Represent $G$ with adjacent matrix $A$; for each edge $e \in E$ with $A[i][j] = 1$ do:

- Partition $R_i$ into slices;
- Partition $C_j$ into slices;

for each valid slice pair $(R_{sk}, C_{sk})$ do:

- $TC_G \leftarrow$ COMPUTE $(R_{sk}, C_{sk})$;

return $TC_G$ as the number of triangles in $G$.

**COMPUTE** (Slice 1, Slice 2)

- Load Slice 1 into memory;
- if Slice 2 has not been loaded then:
  - Replace least recently used slice with Slice 2;
  - Load Slice 2 into memory;

return BitCount(AND(Slice 1, Slice 2)).
For the circuit-level simulation, we design a Verilog-A model for 1T1R STT-MRAM device, and characterize the circuit with 45nm FreePDK CMOS library. We design a bit counter module based on Verilog HDL to obtain the number of non-zero elements in a vector. Specifically, we split the vector and feed each 8-bit sub-vector into an 8-256 look-up-table to get its non-zero element number, then sum up the non-zero numbers in all sub-vectors. We synthesis the module with Synopsis Tool and conduct post-synthesis simulation based on 45nm FreePDK. After getting the device level simulation results, we integrate the parameters in the open-source NVSim simulator [16] and obtain the memory array performance. In addition, we develop a simulator in Java for the processing-in-MRAM architecture, which simulates the proposed function mapping, data slicing and data mapping strategies. Finally, a behavioural-level simulator is developed in Java, taking architectural-level results and memory array performance to calculate the latency and energy that spends on TC in-memory accelerator. To provide a solid comparison with other accelerators, we select from the real-world graphs from SNAP dataset [17] (see TABLE II), and run comparative baseline intersect-based algorithm on Inspur blade system with the Spark GraphX framework on Intel E5430 single-core CPU. Our TC in-memory acceleration algorithm also runs on single-core CPU, and the STT-MRAM computational array is set to be 16 MB.

TABLE I: Key parameters for MTJ simulation.

| Parameter                      | Value |
|--------------------------------|-------|
| MTJ Surface Length             | 40 nm |
| MTJ Surface Width              | 40 nm |
| Spin Hall Angle                | 0.3   |
| Resistance-Area Product of MTJ| 10⁻¹² Ω · m² |
| Oxide Barrier Thickness        | 0.82 nm |
| TMR                            | 100%  |
| Saturation Field               | 10⁶ A/m |
| Gilbert Damping Constant       | 0.03  |
| Perpendicular Magnetic Anisotropy | 4.5 × 10⁵ A/m |
| Temperature                    | 900 K |

B. Benefits of Data Reuse and Exchange

TABLE III shows the memory space required for the bitwise computation. For example, the largest graph com-lj will need 16.8 MB without incurring any data exchange. On average, only 18 KB per 1000 vertices is needed for in-memory computation.

When the STT-MRAM computational memory size is smaller than those listed in TABLE III, data exchange will happen. For example, with 16 MB, the three large graphs will have to do data exchange as shown in Fig. 4. In this figure, we also list the percentages of data hit (average 72%) and data miss (average 28%). Recall that the first time a data slice is loaded, it is always a miss, and a data hit implies that the slice data has already been loaded. So this shows that the proposed data reuse strategy saves on average 72% memory WRITE operations.

Fig. 4: Overall processing-in-MRAM architecture.

Fig. 5: Percentages of data hit/miss/exchange.
C. Benefits of Data Slicing

As shown in TABLE IV, the average percentage of valid slices in the five largest graphs is only 0.01%. Therefore, the proposed data slicing strategy could significantly reduce the needed computation by 99.99%.

| Dataset            | Percentage of Valid Slices |
|--------------------|---------------------------|
| ego-facebook       | 7.017%                    |
| email-enron        | 1.607%                    |
| com-Amazon         | 0.014%                    |
| com-DBLP           | 0.036%                    |
| com-Youtube        | 0.013%                    |
| roadNet-PA         | 0.013%                    |
| roadNet-TX         | 0.007%                    |
| com-lj             | 0.006%                    |

TABLE IV: Percentage of valid slices.

D. Performance and Energy Results

TABLE V compares the performance of our proposed in-memory TC accelerator against a CPU baseline implementation, and the existing GPU and FPGA accelerators. One can see a dramatic reduction of the execution time in the last columns from the previous three columns. Indeed, without PIM, we achieved an average 53.7× speedup against the baseline CPU implementation because of data slicing, reuse, and exchange. With PIM, another 25.5× acceleration is obtained. Compared with the GPU and FPGA accelerators, the improvement is 9× and 23.4×, respectively. It is important to mention that we achieve this with a single-core CPU and 16 MB STT-MRAM computational array.

| Dataset            | This Work w/o PIM | GPU [3] | FPGA [3] |
|--------------------|-------------------|---------|----------|
| ego-facebook       | 5.399             | 0.15    | 0.093    |
| email-enron        | 9.545             | 0.146   | 0.22     |
| com-Amazon         | 20.344            | N/A     | N/A      |
| com-DBLP           | 20.803            | N/A     | 0.295    |
| com-Youtube        | 61.309            | N/A     | 0.413    |
| roadNet-Pa         | 77.320            | 0.169   | 1.291    |
| roadNet-TX         | 94.379            | 0.173   | 1.586    |
| roadNet-PA         | 146.858           | 0.18    | 2.342    |
| com-LiveJournal    | 820.616           | N/A     | 3.304    |

TABLE V: Runtime (in seconds) comparison among our proposed methods, CPU, GPU and FPGA implementations.

As for the energy savings, as shown in Fig. 6 our approach has 20.6× less energy consumption compared to the energy-efficient FPGA implementation [3], which benefits from the non-volatile property of STT-MRAM and the in-situ computation capability.

VI. CONCLUSION

In this paper, we propose a new triangle counting (TC) method, which uses massive bitwise logic computation, making it suitable for in-memory implementations. We further propose a sparsity-aware processing-in-MRAM architecture for efficient in-memory TC accelerations: by data slicing, the computation could be reduced by 99.99%, meanwhile the compressed graph data can be directly mapped onto STT-MRAM computational memory array for bitwise operations, and the proposed data reuse and exchange strategy reduces 72% of the memory WRITE operations. We use device-to-architecture co-simulation to demonstrate that the proposed TC in-memory accelerator outperforms the state-of-the-art GPU and FPGA accelerations by 9× and 23.4×, respectively, and achieves a 20.6× energy efficiency improvement over the FPGA accelerator.

Besides, the proposed graph data compression and mapping strategies are not restricted to STT-MRAM or TC problem. They can also be applied to other in-memory accelerators with other non-volatile memories.

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