Reduced pole to pole voltage deviations through stopping MMC blockading loss of terminals below DC faults

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Abstract. Allergy of voltage supply converters to DC, faults are recognized as the essential obstacle in the direction of significant implementation of meshed DC networks. Because of low flood current capability of Insulated gate bipolar transistor (IGBT), the converters are blocked under excessive currents to prevent permanent damage to the modules converter blocking off all at once interrupts the power float and reasons a significant strength imbalance in together the AC and DC grid. This paper aims to develop dependability and safety of DC networks per the support of stopping harm of terminals below DC faults. The fault response of a modular-multilevel converter is studied analytically and via simulations. It recognized that the Modular-multilevel converter (MMC) goes through quite a few tiers beneath a DC fault, and every stage has distinct dynamics. The effect of the converter showing too occupied into reason.

DC grid topology has a fundamental force on safety structure diagram and performance if a pair of converters linked to the same bus, fault contemporary is shared between the converters and fault modern-day slope of each person converter is reduced. Converter blocking off can, as a result, disallowed and protection device necessities container be relaxed. Temporary MMC blocking off studied like every other approach for keeping off the loss of terminals underneath DC faults. The gain of this strategy is low safety gadget value and decreased affect regular grid operation. A thermal valve model developed to investigate peak thermal stress on antiparallel diodes. Coordination between MMC self-protection and fault detection relays proposed, as nicely as the use of converter DC circuit breaker (DCCB) for backup protection.

1. Introduction
The reason for this paper is to introduce the device, show its strolling precept, and evaluate it in opposition to picks for stopping MMC blockading in DC grids. The assessment is carried out by exploration investigation and examined through the potential of Electromagnetic transient (EMT) simulations. A novel Electronically Controlled Capacitive Energy Storage (CCES) technique proposed for improving the safety and reliability of DC grids. The CCES schematic proven in Figure 1.

The structure is positioned throughout the DC bus, in parallel by the MMC. Separate, single DC line is proven used for uncomplicatedness, though it expected that there are a couple of traces related to the bus. The CCES has double equal poles (even if the MMC is monopolar); besides, its principal issue is a capacitor financial institution in addition to the total capacitance of CB. Other indispensable factors on every pole are anti-parallel thyristors T1 and T2, surge arrester SA and mechanical change SM. Non-
essential elements are an RL filter (RF, LF) and a grounding resistor RG. Directory p mentions to the superb magnate while Directory n denotes to the terrible magnate.

Figure 1. CCES schematic and its definition on a DC bus

The CCES operates with the aid of collecting the pre-charged capacitor financial institution to the DC bus while high DC voltage deflection is revealing. By offering superb or mediocre cutting-edge as required, CCES stabilizes DC voltage which brings the following benefits:
1. Reduced fault modern-day contribution from the MMC.
2. Reduced DC voltage drop.
3. Reduced pole voltage deviations.
4. Improved transient stability.

These advantages can finally use to lengthen or avoid MMC blocking in a range of scenarios. Since CB is pretty extensive, it is a way to reason reflexion problems.

2. Monitoring system
The CCES manipulate layout is proven in Figure2 It has an easy frame, and contain two subsystems - the defect discernment subsystem and the arrester detour. The two poles are managed separately but utilize the same manage device layout.
The management system has two fundamental functions - connecting the capacitor bank to the DC bus when a fault is found out and defending the surge arrester in opposition to excessive currents. Both of these functions are fulfilled through firing thyristors (T1 or T2). Error discovery will, in most instances, be performed by using exterior relays due to the need to assorted CCES process with DCCBs on the same bus. The CCES begins if a fault is found out on any of the associated lines. With the intention of decrease activation time, the arrester passes by prompts each time the arrester modern-day exceeds a predefined threshold ($\pm \Delta I_{SA,max}$), for instance, at some stage in capacitor charging. Additionally to defending flow arresters in opposition to thermic overload, this common-sense supply excess in case of fault detection failure as high arrester cutting-edge would set off T1 is firing below a DC fault. Using($\Delta I_{SA,max}$) peak thyristor voltage strain can be estimated from the surge arrester's V-I characteristic.

3. **Operation underneath pole-to-pole faults**

When a DC fault occurs, thyristors $T_{1P}$ and $T_{1n}$ are fired, bypassing the arresters and connecting CB at once to the DC bus. The same electrical circuit of a CCES-protected DC bus beneath a pole-to-pole fault proven in Figure 3. For simplicity, $I_{MMC}$, $I_c$, and $I_L$ signifies contemporary fault elements superimposed on their pre-defect values. Fault current increase (FCI).
Figure 3. Equivalent circuit of CCES-protected DC bus below a pole-to-pole defect

The CCES operates on the fault cutting-edge because complete fault modern-day of the bus depends on the main on $L_{CSL}$ and $V_{DC}$ (which stays fairly constant), $I_L$ is only marginally elevated by using the addition of $C_B$. However, considering the two sources now related in parallel, the modern-day provided by CCES decreases MMC’s fault contemporary. This result be able to be recorded as:

$$I_{MMC} = I_L - I_C$$

$$I_{MMC}(t) = I_1 \sin(\omega_1 t) - I_2 \sin(\omega_2 t)$$

Where:

$$\omega_{1,2} = \pm \sqrt{[2I_{CSL}CB + \frac{C_{MMC}(2L_{CSL} + L_{MMC})}{L_{MMC}} - \frac{8L_{CSL}C_B L_{MMC} C_{MMC}}{L_{MMC}^2}]}^{1/2}$$

$$I_1 = \frac{V_{DC}(0)}{2L_{CSL}C_B L_{MMC}} \times \frac{1}{\omega_1} (\omega_2^2 - \omega_1^2)$$

$$I_2 = \frac{V_{DC}(0)}{2L_{CSL}C_B L_{MMC}} \times \frac{1}{\omega_2} (\omega_2^2 - \omega_1^2)$$

Equ. (2) indicates that, with the CCES in the system, the MMC’s fault cutting-edge reaction is a mix of two sinusoids with exceptional hesitation at the beginning to be against every other. From Equ. (3), it is evident that the extension in $C_B$ reduces each attribute frequencies, ensuing in slower MMC FCI. However, the CCES additionally reduces MMC’s fault current magnitude. Since this is not obvious from Equ. (3) - (5), Another property of CCES-based safety got via differentiating (2) which produce the expression for MMC’s error modern-day slope:

$$\frac{dI_{MMC}}{dt}(t)/d_t = \frac{V_{DC}(0)}{2L_{CSL}C_B L_{MMC}} \times \frac{1}{\omega_2^2} - \omega_1^2 \times [\cos(\omega_1 t) - \cos(\omega_2 t)]$$

According to Equ. (6), the slope of the MMC’s fault cutting-edge at fault onset (t = 0) is zero. This result is very one-of-a-kind from the mistake reaction of a sole MMC whose preliminary fault modern-day slope received as $V_{DC}(0)/(L_{MMC} + 2L_{CSL})$. Low preliminary fault present-day slope is especially recommended for safety structures with brief fault neutralization time because the resulting MMC FCI is very small.

4. Test system

CCES-based safety validated on a three-terminal DC network proven in Figure 4. The important energy machine parameters given in Table 1 MMCs 1 also 2 are the same converters linked to controllable energy exporter representing the offshore wind field. The converters are working in a grid-forming mode, controlling AC voltage. MMC 3 is an onshore converter linked to the onshore AC net. The converter regulates DC voltage and has a strength rating equal to the cumulative power ranking of MMCs 1 and 2. The onshore net is symbolizing as a voltage supply with internal RL impedance. To allow a reasonable
contrast between the results. Meanwhile, MMC three has equal per-unit parameters as MMCs 1 and 2, scaled only by using its energy ranking.

![Diagram of three-terminal DC grid with CCES protection](image)

**Figure 4.** Three-terminal DC grid with CCES protection

| Component | Parameter | Value |
|-----------|-----------|-------|
| MMC 1 and 2 | MMC power rating | 1000 MVA |
| | Arm inductance | 60 mH |
| | Cell capacitance | 8 mF |
| MMC 3 | MMC power rating | 2000 MVA |
| | Arm inductance | 30 mH |
| | Cell capacitance | 16 mF |
| | Nominal DC voltage | ± 320 kV |
| | Cells per arm | 400 |
| | Transformer voltage rating | 372 / 360 kV |
| | Series transformer reactance | 0.15 p.u. |
| MMC 1, 2, 3 | Nominal AC voltage | 372 kV |
| | Nominal AC frequency | 50 Hz |
| | Short circuit ratio | 10 |
| | X / R ratio | 10 |

Base quantities for per-unit analysis again in Table 2 for completeness.
Table 2. Base units for per-unit analysis

| Parameter         | Value  |
|-------------------|--------|
| Base DC voltage   | 640 kV |
| Base DC current   | 1.6 kV |
| Base arm current  | 1.7 kA |
| Base AC voltage   | 303.74 kV |
| Base AC current   | 2.2 kA |

5. Simulation and Results
Simulation circuit is shown in Figure 5 as a continuous current line of (300 km) in the event of a failure, we can control the fault using pi control signal control that separates the converter from work.

Figure 5. simulation of project
Control circuit shown in Figure 6 used in Long transmission lines that exceed (800 kilometers) used for these distances. If the transmission lines increase, they collapse and become a load, to avoid these losses in equipment and lines. We convert the current by means of a rectifier to a continuous wave to be one wave and one line, for example, under the seas, and between the states.
The important parameters given in Table 3. Which includes parameters three-phase voltage source in series with RL branch, and implements a 3-φ transformer 600MVA, a bridge of selected power electronics devices when model is discretized suggested snubber values for most applications the internal inductance L on of diodes and thyristors should be set to zero. Simulink logical is used to control the breaker operation when the external switching time option is selected and use parallel RLC branch to add or remove elements from the branch.

| Parameter                                      | Value      |
|------------------------------------------------|------------|
| Phase –to-phase voltage (Vrms)                 | 315e3      |
| Phase angle of phase A(degree)                 | 120        |
| Frequency (HZ)                                 | 60         |
| Source resistance (ohms)                       | 0          |
| Source inductance(H)                           | 46.671e-3  |
| Base voltage (vrms ph-ph)                      | 0          |
| Parameters of three-phase Transformer 600MVA   |            |
| Winding 1 connection (ABC terminals)           | Yg         |
| Winding 2 connection (abc terminals)           | Delta (D1) |

**Figure 6.** Control circuit simulation
Type Three single-phase transformers
Parameters Rectftr Universal Bridge
Number of bridge arms 3
Snubber capacitance Cs (F) 50e-9
Snubber resistance Rs (Ohms) 2000
Parameters three-phase parallel RLC branch
Branch type RL
Resistance R (ohms) 12.41
Inductance L (H) 23.264e-3
Parameters DC Fault implements a circuit breaker
Initial status 0
Switching times (s) 0.5
Snubber resistance Rs (ohm) inf
Breaker resistance Ron (ohm) 0.1
Snubber capacitance Cs (F) 0

Figure 7 shows the current and voltage of the three-phase source, and DC voltage the moment it malfunctions.

- The first signal shows the three-phase voltage when the fault occurs and the distortion appear.
- The second shows the three-phase current when the fault occurs and the distortion appear.
- The third one present constant voltage when the fault occurs and the distortion appear.

The constant current calculate according to the equation:
\[ I_{dc} = \frac{V_{dc1} - V_{dc2}}{R} \]

And to calculate the constant voltages according to the equation:
\[ V_{dc} = \frac{V_{dc1} + V_{dc2}}{R} \]
By using a voltage regulator, current regulator, and a device pi control, we can instantly protect the circuit when the fault occurs, as in Figure 8

- The first signal represents the constant current during the fault as well as the reference signal (Blue) in order to compare the increase or decrease in the current.
- The second represent the change in the trigger, during the fault.
- The third one represents the fault current.

![Figure 8. Indicates when the malfunction removed](image)

6. Conclusions
The DC grid protection device, CCES, has shown to convey a couple of advantages to DC networks:
1- It avoids MMC blocking off below DC errors through decreasing present-day fault involvement plus voltage release of the MMC. By way of an outcome, DCCB inductors can decrease, and price active mechanical DCCBs can utilize.
2- It reduces pole voltage deviations and avoids MMC blockade below pole-to-ground errors in regular monopole networks.
3- It ameliorates transient DC grid constancy.
4- It appreciably minimize DC overvoltages, inclusion savings in fee of overvoltage preservation.

The effect of CCES on everyday grid operation considerably reduced through the use of surge arrester coupling, which creates a dead-band round nominal DC bus voltage internal of which the CCES successfully disconnected from the bus. If the dead-band voltage exceeded, the surge arrester turns into a short circuit, and CCES gives or absorbs DC as imperative to stabilize the grid. Parallel construction of surge arresters with thyristors ensures that each the contemporary arrester rating and thyristor voltage evaluation minimized, lowering the measurement and price of these components.

The estimated price of CCES for 1 GW MMC station is around 30 M€, while the scheme weight is one hundred fifty tons. This cost considerably decreased than the cost of a protection gadget primarily based on hybrid DCCBs or FB MMC. Since only one CCES wanted per DC bus, the CCES will exhibit extra economic incentive like DC grids enlarge with additional converters and electricity drift paths. On the downside, some expand in DCCB energy absorbers may additionally be wanted.

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