EM Modelling Considerations for mm-Wave On-Chip Antennas

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Abstract—We investigate the inaccuracy of resonant frequency ($f_0$) estimation incurred by some common simplifications in electromagnetic (EM) simulation of mm-wave on-chip antennas. Using an 88 GHz patch antenna as a device under test (DUT), it is found that using a 2.5D planar EM solver produced highly inaccurate results. Including the bulk silicon and thin nitride in the model stack affected an improvement of 0.8% in estimating $f_0$ while replacing individually modelled via arrays with equivalent blocks, and accounting for the etch factor, marginally improved both the estimation of $f_0$ and reflection coefficient $|S_{11}|$. It is shown that, with the correct modelling choices, the error in $f_0$ can be reduced to below 50 MHz at E-band, which is within the measurement variation of 880 MHz.

Index Terms—Finite element analysis, millimetre-wave integrated circuits, numerical simulation, patch antennas.

1. Introduction

Millimeter-wave on-chip antennas present many challenges to full system-on-chip (SoC) integration [1], including low gain and large footprint. Both problems can be assessed accurately through reliable first-iteration full-wave electromagnetic (EM) modelling [2], [3]. Full-wave 3D EM modelling of large on-chip passive devices is complicated by the extreme aspect ratios and thin dielectric layers, both of which contribute to large mesh sizes. The high frequency also exacerbates the losses associated with surface roughness and the etch factor. This complex modelling environment often necessitates simplifications of the model geometry [4], such as 2.5D (as opposed to full 3D) modelling[5], the omission of probe pads [6] and of some dielectric layers [7]. The inevitable effect of these simplifications is the reduced first-iteration accuracy, with a deviation of several hundred MHz [7] for the resonant frequency ($f_0$) of resonant patch antennas above 60 GHz.

In this paper, we investigate a number of simplifications used in the EM modelling of mm-wave on-chip antennas and quantify how each affects the accuracy estimation of $f_0$ in resonant patch antennas implemented in the back-end-of-line (BEOL) of a typical BiCMOS process. In addition to the effect of BEOL stack first conducted in [8], this work investigates the effect of via geometry simplification, etch factor and solver choice.

2. Device under test

A simple square patch antenna (figure 1)[8] was fabricated in BEOL of the GlobalFoundries 8HP SiGe BiCMOS process (7 metal layer BEOL). The 818 × 818 μm patch is located on the top thick (±4 μm) (AM) aluminium layer and suspended over a large, solid copper ground plane (1070 × 938 μm) on MQ layer at a height of ±9.6 μm below AM. The patch is fed with an AM-MQ microstrip line of width 12.54 μm and length 200 μm, which is excited by ground-signal-ground (GSG) probe arrangement of 100 μm pads and 150 μm pitch. The ground pads are stitched to the large MQ ground plane with via array stacks of 39 × 39 μm.

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Figure 1. 88 GHz patch antenna: a) HFSS simulation model. b) Micrograph of the antenna under test. c) Embedded and de-embedded measurement results

The device under test (DUT)’s $S_{11}$ is measured through wafer-probing, with three devices measured to establish measurement error margins. Both probe-tip calibration using line-reflect-match (LRM) standards on a ceramic substrate and second-tier de-embedded using on-chip thru-reflect-line (TRL) standards results are shown in figure 1(c), where the measured $f_0$ ranges between 87.72 to 88.6 GHz and $|S_{11}|_{\text{min}}$ from -13.69 dB to -12.12 dB in the embedded case. Due to a discrepancy in the definition of the THRU and REFLECT standards on-chip, a minor de-embedding error results in $|S_{11}| = +0.33$ dB out-of-band. With this result established, different EM modelling approaches were investigated.

3. EM modelling comparisons

3.1. Effects of stack-up and pads

Three versions of the 7ML BEOL stack-up (using the 3D layout design procedure in [2]) were investigated (figure 2). Stack “A” omits the FEOL and terminates on the lowest M1 metal routing layer. Stacks “B” and “C” both include the bulk silicon terminated in a perfect electric conductor (PEC) and heterogeneous SiO$_2$ across the BEOL. Stack “C” also includes a thin nitride ($\varepsilon_r = \pm 6.8$) layer above the bulk Si substrate as opposed to an oxide layer ($\varepsilon_r = \pm 4$), in stack “B”. The results in figure 2(d) indicate marginal variation between stacks “B” and “C”, both for embedded and de-embedded measurements, while stack “A” may be disregarded in the further analysis due to the significant discrepancy. The background plots in grey represent the measured results.

Figure 2. Comparison of BEOL stacks : (a) Stack “A”, (b) Stack “B”, (c) Stack “C”, (d) Simulated results, with embedded pads are shown in solid lines and de-embedded results with dashed lines[8].
3.2 Effect of via simplification

To evaluate via simplification effect on the modelling accuracy, solid via blocks (figure 3(b)) are used instead of arrays of vias, using stack “B” and embedded pads. The results in figure 3(c) indicate no considerable loss of accuracy in estimating either \( f_0 \) or \( |S_{11(min)}| \), as the resulting changes of 87.3 MHz and -12.49 dB are within the measurement error range as demonstrated in figure 1(c).

3.3 Effect of etch factor

Using stack “C”, the effect of etch tapering [9] is investigated by including and omitting a 71° etch angle. The resulting variation of 360 MHz in \( f_0 \) and 0.35 dB in \( |S_{11(min)}| \) shown in figure 4, indicates very little effect on modelling accuracy when compared to the measurement error in figure 1(c).
3.4. Effect of solver choice
Using stack “C”, 2.5D planar and 3D finite elements method (FEM) solvers were also evaluated with identical simulation settings. The comparison in figure 5 clearly indicates the inaccuracy incurred in using this approach, despite the advantages in reduced solver time [3].

3.5. Consolidated selections
By using Stack “C”, with embedded pads, with 71° etch taper, consolidated vias and FEM solver, the comparison in figure 6 is obtained. Less than 50 MHz and 1.7 dB are incurred in estimating $f_0$ and $|S_{11(\min)}|$, respectively.

4. Conclusion
We have presented a comparison of different EM modelling approaches using an 88 GHz patch antenna in BiCMOS as DUT. It was found that the thin-metal approximation in the 2.5D planar solver yielded significant inaccuracy, while a FEM solver could estimate $f_0$ and $|S_{11(\min)}|$ accurately to within 50 MHz (0.056% error) and 1.7 dB when the bulk silicon, consolidated via arrays, and the etch factor are included in the EM model. Future work will extend this analysis to an investigation of the antenna’s radiation pattern.

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