Linearization of power amplifiers with mismatched output impedance using on-line digital pre-distortion structure

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Abstract  This letter introduces a novel on-line digital pre-distortion structure for linearizing RF power amplifier under the output impedance mismatch conditions. Unlike traditional off-line structures, the proposed structure updates its weight parameters adaptively synchronizing with the power amplifier load impedance. Furthermore, this letter analyses with a MOSFET model and proves that the output conductance of MOSFET are relevant to nonlinearity of power amplifier with variable load impedance. To verify this structure and the analysis, a simulation on MATLAB Simulink was built using a N-channel MOSFET based on Shichman-Hodges model. Proposed on-line Digital Pre-Distortion structure significantly acquired better linearity performance with variable load impedance than conventional off-line structures.

key words: linearization technique, output impedance mismatch
Classification: Microwave and millimeter wave devices, circuits, and hardware

1. Introduction

Cellular mobile communication is stepping into its fifth generation. With continued escalation requirements for higher efficiency, compensating the nonlinearity of radio frequency system has courted much attention [1, 2]. However, the nonlinearity of whole system largely derives from Power Amplifier (PA) [3–6].

Researchers have put forward massive linearization technologies [7–13] for PA. Digital Pre-Distortion (DPD) system was proved an efficient [14, 15] and adaptive [16, 17] one among all the techniques. However, linearity performance degrades severely when antenna mismatched with PA output impedance even with traditional off-line DPD applied [18]. Off-line DPD structure needs frequent retraining process when dealing with dynamic environments [19].

To overcome the drawback of off-line structure, this letter introduces an adaptive on-line DPD structure. Our structure is able to rapidly and stably follow the variable load impedance and achieves excellent linearity performance.

2. Output impedance mismatch conditions

When load impedance mismatch with output impedance, no additional voltage was reflected to transistor. To study the additional voltage in the mismatch conditions, we use a MOSFET transistor formula modelled by previous researchers [20]. Transistor current \(I_{\text{trans}}(t)\) is expressed in Eq. (1):

\[
I_{\text{trans}}(t) = \sum_{p=1}^{p} C_{i,p}[1 + \gamma_{p} V_{DS}(t)]u^{p}(t).
\]

Here \(u(t)\) denotes transistor input signal. \(C_{i,p}\) represents static and dynamic nonlinearity characteristic of transistor. \(V_{DS}(t)\) is the output voltage of transistor. Variable load impedance will cause \(V_{DS}(t)\) to change, which is scaled by output conductance of transistor \(\gamma_{p}\). Note that \(\gamma_{p}\) is mainly determined by channel-length modulation parameter \(\lambda\) in longer MOSFETs [21]. As a consequence, the nonlinearity of transistor may change with different load impedance.

3. Proposed on-line DPD structure

Conventional off-line DPD structure is a typical indirect learning structure [22, 23]. Its inverse model of PA requires identification after each transmission. As analyzed above, the nonlinearity of transistor changes simultaneously with load impedance. Thus an on-line DPD structure is more reliable under the variable load impedance conditions. On-line structure exposes two challenges in comparison to off-line one [24, 25]. First one is to keep adaptive algorithm converging under variable conditions. The second is to compensate the loop delay of the system in real-time. So we designed amplitude divider and Loop Delay Estimation (LDE) respectively as showed in Fig. 1. Amplitude divider is a simple divider operation that gives the estimated amplitude gain \(G_{n}\), which is used to pre-scale baseband signal instead of normalizing output signal of PA.

Loop delay consists of integer part as well as fractional part. As showed in Fig. 2, the latency throughout the RF components is \((\tau_{n} + \theta_{n})\) times of sampling period. Here \(\tau_{n}\) and \(\theta_{n}\) represent the estimated integer and fractional LDE separately. \(G_{n}\) denotes the estimated voltage amplitude gain.
of PA, which is estimated between integer and fractional LDE procedure.

The structure of integer LDE consists of delay units, multipliers and comparators, the latency index of the maximum cross-correlation [26] results is the estimation of integer LDE. The LMS procedure of calculating fractional LDE is presented as Eq. (2), Eq. (3) and Eq. (4). \( x_\theta(n) \) is the output of a three-points Lagrange interpolation filter [27] with the fractional delay of \( \theta \). The symbol \( \mu \) is an empirical constant represents for the speed of convergence, which is set to 0.25.

\[
|x_\theta(n)| = \frac{1}{2} \theta(\theta - 1) \cdot |x(n + 1)| + (1 + \theta)(1 - \theta) \cdot |x(n)| + \frac{1}{2} \theta(\theta + 1) \cdot |x(n - 1)|. \tag{2}
\]

\[
e_n(\theta) = \frac{G_n}{G_0} |x_\theta(n)| - |y(n)|. \tag{3}
\]

\[
\theta_{n+1} = \theta_n - 2\mu \frac{\partial e_n(\theta)}{\partial \theta} e_n(\theta). \tag{4}
\]

RLS algorithm is capable of rapid convergence yet sensitive to the amplitude of signals [28]. For the sake of stabilizing algorithm, our approach is to avoid using the ever-changing \( G_n \) to achieve normalization and let RLS algorithm following the impedance mismatch status.

![Fig. 1. Proposed on-line DPD structure.](image1.png)

**Fig. 1.** Proposed on-line DPD structure.

![Fig. 2. LDE and amplitude divider structure with real-time processing.](image2.png)

**Fig. 2.** LDE and amplitude divider structure with real-time processing.

5. Results

Both structures compensate the nonlinearity of PA in ACPR for about 22dB as presented in Fig. 3. But as output impedance mismatch status getting worse, the linearity of the traditional off-line DPD deteriorates. Yet the POLDPD structure retains great linearity.

![Fig. 3. ACPR performance comparison along with the imaginary part of load impedance increasing.](image3.png)

**Fig. 3.** ACPR performance comparison along with the imaginary part of load impedance increasing.

Comparison of ACPR error between POLDPD and traditional off-line DPD with \( \lambda = 0.05V^{-1} \) (left) and \( \lambda = 0.5V^{-1} \) (right).

![Fig. 4. Comparison of ACPR error between POLDPD and traditional off-line DPD with \( \lambda = 0.05V^{-1} \) (left) and \( \lambda = 0.5V^{-1} \) (right).](image4.png)

**Fig. 4.** Comparison of ACPR error between POLDPD and traditional off-line DPD with \( \lambda = 0.05V^{-1} \) (left) and \( \lambda = 0.5V^{-1} \) (right).
6. Conclusion

An adaptive on-line digital pre-distortion structure is proposed in this letter. Simulation result reveals that this structure is far superior to the off-line structures in compensating the nonlinearity under the variable load impedance situations, where the nonlinearity is proved relevant to the output conductance of transistor. The simulation carried out in this letter only studied one of the factors that may affect the nonlinearity under the mismatch conditions. Therefore, further studies should work on a realistic PA and the proposed structure should be pruned either.

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