A 500–2500 MHz fully integrated CMOS power amplifier with multilayer series inductors

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Abstract A broadband matching network used to provide a suitable load resistance for the MOSFET over a large frequency range is one of the keys to realize a broadband fully integrated CMOS power amplifier (PA). However, the broadband off-chip matching network will occupy large printed circuit board area and bring more parasitic effects. The broadband on-chip matching network suffers from large chip area. The paper presents a fully integrated matching network, which replaces the standard inductors (STIs) with the multilayer series inductors (MSIs), for expanding the bandwidth and reducing the chip size. The fully integrated matching network is applied in a broadband PA, which achieves a good performance in the measured 133% fractional bandwidth from 500 MHz to 2.5 GHz. The maximum power-added efficiency (PAE) achieves 42.5 % and the saturation output power reaches 24 dBm. The chip area is 0.4 mm² at TSMC 0.18 μm technology process. It draws 100 mA from 3.3 V supply voltage and the static power consumption is less than 0.3 W.

Keywords: broadband, CMOS PA, matching network, multilayer series inductors (MSIs)

Classification: Electron devices, circuits and modules (silicon, compound semiconductor, organic and novel materials)

1. Introduction

Meeting the demands of multiple-wireless communication applications (e.g., Internet of Things), the variety of protocols rises continuously, such as TD-CDMA, DVB-T, 802.11b/n, Zigbee and etc. A broadband transmitter needs to be compatible with these protocols for achieving miniaturization and improving integration [1, 2, 3]. As a key component of the transmitter, a power amplifier (PA) is used for transmitting large power signal. Unfortunately, due to the parasitic parameters of the PA, the large-signal performances are decreased in high frequency band and the bandwidth is difficult to be extended [4, 5]. Thus, expanding the bandwidth of PA is one of the important tendencies of future.

Several techniques are proposed to expand the bandwidth of the PA in the past years that are classified into two categories. Decreasing the parasitic effects of MOSFET, which consists of negative feedback PA [6, 7], stack PA and cross-coupled structure [8, 9], is the first way. However, the bandwidth of the cross-coupled and the negative feedback structure cannot be expanded indefinitely and the output power is usually low. The optimal impedance of the stacked PA can be close to 50 Ω with a simple matching network. However, the higher supply voltage of the stacked PA brings more power consumption.

The second way is to optimize the matching network for broadband application, which is divided into the off-chip and on-chip. The off-chip matching network occupies large PCB area and brings more parasitic effects. The way for realizing the broadband fully integrated PA consists of the distributed PA [10], transmission line PA [11, 12, 13], switched-capacitor PA [14, 15] and transformer-based PA [16, 17]. The bandwidth of the distributed PA is easy to be expanded, but the distributed PA occupies large chip area and brings high power consumption. The switched-capacitor PA is used to enhance the efficiency over the wide frequency band, however, the linearity of the switched-capacitor PA will be decreased. The transmission line PA has high frequency sensitivity and occupies large chip area. The lower-frequency limit of the transformer-based PA is larger than 2 GHz that is not compatible with the mainstream protocols.

In this paper, the multilayer series inductors (MSIs) are utilized to replace the standard inductors (STIs) for expanding the bandwidth of the matching network and reducing the chip size in a fully integrated matching network. A 500–2500 MHz CMOS PA, which is applied in a broadband transmitter, utilizing this method is presented in this paper. The paper is organized as follows. The MSI and a fully integrated matching network are presented in Section 2, and the proposed method is used in a broadband PA. Section 3 shows the measured results of the 500–2500 MHz PA. The conclusions are given in Section 4.

2. An on-chip matching network using MSIs

The broadband matching network is usually realized in two ways. The real frequency technique [18, 19, 20] is the first way. The equivalent impedance provided by the real frequency technique varies with frequency. Nevertheless the calculation and the structure of the matching network are complicated. The filter-type matching network, which depends on certain equivalent impedance by compromising the equivalent impedance over the wide bandwidth, is the second way [21, 22, 23]. The filter-type matching network is easy to be realized by the EDA software and the computational complexity is low, however, the complex structure occupies large chip area in broadband applications.

The traditional filter-type matching network is formed by the cascade of multiple networks in the broadband application, and the bandwidth (BW) of the RLC network is related

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BW = \omega / Q \quad (1)

Thus, the quality factor of the inductor in the RLC network needs to be decreased for expanding the bandwidth. The quality factor of the STI fabricated by CMOS process is not low enough at the high frequency. Thus, the additional resistors are inserted to the STIs for decreasing the quality factor. Nevertheless, the additional resistance composed of several large resistors in parallel for reducing the technical difference occupies large chip area and increases the difficulty in layout design. The connection lines of the resistors always use the base metal that will increase the substrate loss of the matching network. In order to achieve higher output power, differential structure is always applied in CMOS PA design. Inserting the series structure of inductor and resistor into the matching network in parallel will enhance the mismatch of differential structure, which directly affects the linearity of PA. Meanwhile, the density of inductance of the STI, which occupies large chip area, is low.

As plotted in Fig. 1, the MSI can solve the problems mentioned above. The proposed MSI made up of Metal 4 and Metal 5 in parallel and Metal 6 in series achieves the low quality factor and the high density of inductance. As plotted in Fig. 2, the insertion loss of the standard inductor and the additional resistor (SIR) is nearly equal to the insertion loss of the MSI in the low frequency band under the same inductance and quality factor. The MSI do not need the base metal as the connection lines that will reduce the substrate loss of the device, and thus the absolute value of the insertion loss of the MSI is lower than the SIR in the high frequency. However, the size of the SIR is almost three times the size of the MSI as shown in Table I. The multilayer metal in the MSI increases the density of inductance, and the lower metal is much thinner than the top metal that will provide larger parasitic resistance and the lower quality factor at the high frequency. Stacking Metal 5 and Metal 4 can decrease the high frequency effects for avoiding introducing excessive static losses. The inductance of the MSI is much larger than the STI at the same size, and the parasitic resistances are almost the same at the low frequency. The quality factor of the SIR is smaller than the MSI at low frequency band. With an increase of the frequency, the proximity and the skin effect enhance gradually. The quality factor of the MSI will decrease rapidly, and thus provide a low quality factor over the whole frequency range. The MSI enhances the density of inductance and provides a low quality factor over a large frequency range, which ensures stable performance of the matching network. The quality factor and the inductance of the STI and the MSI at the same size are demonstrated in Fig. 3 that prove the previous conclusion. The inductance of the MSI is more than twice the inductance of the STI. The quality factor of SIR is larger than MSI at high frequency. Thus, the MSI can replace the STI in broadband applications and save the chip area. The measured and simulated results of the proposed MSI are demonstrated in Fig. 4. The outer diameter and the width of the proposed MSI are 95 μm and 9 μm, respectively. The inductance is equal to 2.3 nH and the quality factor is less than 5.7 from 500 MHz to 2.5 GHz. The error between the simulated and measured results is mainly due to the selection of the simulation precision and the de-embedding arithmetic. Increasing the simulation precision and the de-embedding arithmetic, however, enhances the
complexity in calculation, and the error is small and lies in an acceptable range.

Compared with the off-chip matching network, the fully integrated matching network can decrease the parasitic effects and the design complexity of the printed circuit board. The actual matching network, which replaces the STIs with the MSIs, is shown in Fig. 5. According to the formula (1) and Fig. 3, the MSIs can be applied to expand the bandwidth of the matching network and the density of inductance is larger than the STIs. Meanwhile, the MSIs do not need additional resistors to reduce the quality factor for expanding the bandwidth. For reducing the mismatch of differential structure, the transformers are used to connect the passive device and MOSFET by the single and differential terminal, respectively. As shown in Fig. 5, the L1, L2 and L3, which are the MSIs, are employed for expanding the bandwidth of the matching network and reducing the chip size. The maximum AC current swing of the output matching network at saturating output power ($P_{sat}$) is lower than 186 mA which is also in an acceptable range. A transformer in the input matching network is used as an inductor in series for converting the high capacitive impedance at the gate to the low impedance. The output matching network is converted by a traditional third-order bandpass network. An on-chip transformer utilized in the output matching network is plotted in Fig. 6 and the measured results of the insertion loss are higher than $3.6$ dB. The transformer is used as the power combiner and realizes the function of impedance conversion. The primary coil of the transformer used as the load inductance of the PA saves the chip area. The patterned ground shield under the transformer is applied for decreasing the loss of substrate.

A 500–2500 MHz transmitter, which is compatible with long distance communication application and the wireless mobile communication system [24, 25, 26], is applied to mobile ad-hoc network (MANET). The fully integrated matching network utilized in the broadband PA is the key component of the proposed transmitter. The core of PA uses the cascode structure for enhancing the breakdown voltage and output power. The gate length of CG transistors, which employ the thick gate-oxide transistors to prevent the devices of the cascode structure from breaking down, is 350 nm. The maximum output voltage swing at $P_{sat}$ is lower than 7.9 V, which is much smaller than the maximum allowable voltage swing. Thus, the bandwidth PA can keep a long-term reliability. The circuit of the 500–2500 MHz PA, which consists of a broadband PA, a bandgap and a power detector (PD), is demonstrated in Fig. 5. The power detector is employed to detect the transmitting power. The bandgap is used to provide a stable bias voltage for the gate bias of the cascode PA.

3. Measured results and analysis

The chip photo of the proposed CMOS PA, which is fabricated using a TSMC 0.18 µm technology process, is demonstrated in Fig. 7. The size is 0.4 mm² without the test pads and the performances of the PA are measured on package.

The simulated and measured S-parameter from 500 MHz to 2.5 GHz is shown in Fig. 8. The S22 and S11 are smaller than $-8.3$ dB and $-11.5$ dB, respectively. The S21 achieves 12.5–13.6 dB. The error of the simulated and measured S-parameter in Fig. 8 is due to the parasitic parameters of the PCB and package. As shown in Fig. 9, the logarithm of the small-signal stability ($\lg K$) is more than 1.18. As plotted in Fig. 10, the single-tone signal performances are measured from 500 MHz to 2.5 GHz. The 1 dB output compression point ($P_{1dB}$) reaches 20.5–21.3 dBm and the $P_{sat}$ achieves 22.5–24 dBm. The peak of PAE in Fig. 11 and Fig. 12 reaches 42.5 % at 700 MHz. The saturation PAE is more than 34.4 % over the whole frequency range. The capacitance between the gate and the drain terminal cannot be completely eliminated by the matching network. Thus, the power gain,
Fig. 9 The measured $K$ of the broadband PA.

Fig. 10 The measured power gain of the broadband PA.

Fig. 11 The measured PAE at $P_{1\text{dB}}$ and $P_{\text{sat}}$.

Fig. 12 The measured PAE of the broadband PA versus output power.

Fig. 13 The measured IMD3 of the broadband PA.

Table II

| Ref. | Bandwidth (GHz), (%) |
|------|----------------------|
| [27] | 4-7, 15-20          |
| [28] | 6-8, 20              |
| [29] | 1-5, 10-15           |
| [30] | 2-4, 20              |
| This work | 2-4, 20              |

| Ref. | $P_{\text{sat}}$ (dBm) | Gain (dB) | PAE (%) | Size (mm$^2$) | CMOS Process (nm) |
|------|------------------------|-----------|---------|--------------|------------------|
| [27] | 15-20                  | 19-22     | 12-15   | 0.6          | 180              |
| [28] | 15-20                  | 19-22     | 12-15   | 0.7          | 180              |
| [29] | 15-20                  | 19-22     | 12-15   | 0.7          | 180              |
| [30] | 15-20                  | 19-22     | 12-15   | 2.3          | 180              |
| This work | 15-20                  | 19-22     | 12-15   | 0.4          | 180              |

Table II Results and comparison.

the output power and the PAE are decreased in the high frequency band. Moreover, the third order intermodulation distortion (IMD3) with the output spectrum for tone-spacing of 2 MHz versus output power of the PA is plotted in Fig. 13. The IMD3 is less than $-36.6$ dBc, while the output power ($P_{\text{out}}$) is less than 20 dBm.

Table II [27, 28, 29, 30] compares the proposed PA to the state-of-the-art broadband PA. The proposed filter-type matching network, which replaces the STIs with the MSIs, provides higher output power and larger bandwidth compared with the real frequency technique. The relative bandwidth of the CMOS PA with the proposed filter-type matching network is larger than the traditional filter-type PA and the chip area is smaller.

4. Conclusions

This paper provides a fully integrated matching network, which replaces the STIs with the MSIs, for expanding the bandwidth and reducing the chip size. The method applied in a broadband CMOS PA achieves a good performance in the measured 133% fractional bandwidth from 500 MHz to 2.5 GHz. The small signal gain is higher than 12.5 dB. The $P_{\text{sat}}$ is more than 22.5 dBm and the average saturation PAE is larger than 34.4% over the whole frequency range with a 3.3 V supply.

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