A Fast-Lock Low-Jitter PLL Based Adaptive Bandwidth Technique

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Abstract. An adaptive-bandwidth phase-locked loop (PLL) presented in this paper is a multi-function, general purpose frequency synthesizer. Ultra-wide input and output ranges along with best-in-class jitter performance allow the PLL to be used for almost any clocking application. To reach wide output range and optimal jitter performance, adaptive bandwidth technique is applied to guarantee the stability of the loop. Furthermore, a fast-lock circuit is used to improve locking speed. The PLL is implemented in a 65nm CMOS process, while the core occupies 0.05mm² and measurement results shows that the adaptive bandwidth PLL can generate clock with frequency from 200MHz to 1.6GHz. The measurement results also show good robustness of the PLL over temperature and supply voltage variation. The measured RMS jitters at 1.6GHz is less than 0.8ps when the supply noise under the 1% of itself. The fast-lock process lasts less than 3us, and the complete lock time is determined as 1000 input cycles.

1. Introduction

PLLs are widely used for generating the different clocks required in ASIC and SoC design. As CMOS technology scales, it becomes more challenging to design circuit that meets the specifications under all process, voltage, and temperature (PVT) conditions. PLL designs, one of the challenges is ensuring that the frequency range of the voltage-controlled oscillator (VCO) is wide enough to cover the desired frequency points under all condition.

The performance of the fixed bandwidth PLL is limited which can be improved by adaptive bandwidth technique. We all know that the ring oscillator (RO) based due to the small area and the wide frequency tuning range [1][2], but the RO often has poor phase noise. In addition, different module in a PLL has different transmission performance of phase noise, it needs to find suitable bandwidth to keep the loop stable. The RO based PLLs with self-bandwidth control techniques [3][4] are attractive to solve these problems. There also have some un-self controlled circuit techniques to realize adaptive bandwidth have been published [5][6]. However, those loop band adjustment modules occupy much area. In this paper, we propose a low-jitter wideband ring-oscillator based self-biased charge pump PLL. on the one hand, combining with a simple voltage-to-current (V-I) module and a current controlled oscillator (CCO) that cover wide frequency range, the PLL can provide a wide range of frequencies; on the other hand, adaptive bandwidth technique can make the PLL keep optimal bandwidth and jitter performance.

This brief is organized as followed: First, the architecture of PLL, including the operating principle of adaptive bandwidth, is described. Second, the circuit implementation of each key component in the PLL is presented. Then, the measurement results from a test chip fabricated in a 65nm CMOS are discussed.
2. PLL Architecture
Fig.1 shows the architecture of the proposed adaptive wideband PLL. With excellent supply noise immunity, the PLL is ideal for use in noisy mixed-signal SoC environments. The PLL consists of a phase/frequency detector (PFD), a self-biased charge pump (SBCP), a loop filter (LPF), a proposed voltage –to-current (V-I) and a CCO, high speed and wide range dividers, and a fast locking module.

![PLL Architecture Diagram](image)

Comparing the input reference clock and feedback clock through PFD, PFD exports UP and DOWN for two branches, the one branch controls the switch of CP after voltage conversion, the other one branch convey to V-I module to control the switch of current source together with the division ratio of feedback divider. After LPF, the output voltage of CP control drive current of CCO through V-I, the output signal of CCO was divided into two branches through shaping by buffer, the first branch is FOUT, the second branch is VCO FB which is used to get feedback clock by feedback divider. Input reference clock and feedback clock control the fast lock module as well.

For the third orders charge pump PLL, the bandwidth of loop can be approximated as:

\[ f_c = \frac{I_{CP} K_{VCO} R}{2\pi N} \quad (1) \]

Where \( I_{CP} \) is the charging and discharging current of the CP, \( K_{VCO} \) is the gain of the VCO (which is related to \( I_{CCO} \) of CCO), \( R \) is the equivalent resistor of loop filter, and \( N \) is the division ratio of the divider. To achieve optimized balance between phase noise performance and loop stability, the bandwidth \( f_c \) of PLL should change follow \( f_{ref} \) of PLL. The bandwidth is adjusted by \( I_{CP}, K_{VCO} \) and \( R \), which are adjusted between each module. For the PLL:

\[ K_{CCO} = \frac{\omega_0}{2I_{CCO}} \quad (2) \]

\[ I_{CCO} = M \cdot I_{CP} \quad (3) \]

Where \( \omega_0 \) is the output frequency. The relation of \( I_{CCO} \) and \( I_{CP} \) is shown as formula (3), because \( R \) changes small, we can know that the bandwidth only related to the input frequency and proportion coefficient [7]. Through the adjustment of the bandwidth, we can reduce the jitter of PLL loop and increase the effective output frequency range of VCO. Furthermore, isolated analog supply (2.5V) allows for excellent supply rejection in noisy SoC applications by voltage-to-voltage conversion.

3. Building blocks implementation

3.1. Charge pump
Figure 2. Charge-pump structure.

The self-biased charge pump, shown in Fig. 2. There is a full differential double switch of CP, and the input signals are opposite with traditional CP to control switches in order to ensure the output signal correspond to the module V-I and CCO. CP is the second major PLL noise contributor, the differential structure is essential. Better RMS jitter performance is achieved by suppressing power supply common noise. Two pairs of charge pump are designed to alleviate the charge sharing using a unity gain converter. The biased current source of CP is produced by Vctrl and conveyed by low-voltage current mirror. The output signal, Vctrl, control the current sources in CP and V-I module.

3.2. V-I Structure and CCO Module

Fig. 3 shows the schematic of module V-I and Ring CCO. The V-I module include current source control part and current source generate part. As shown in fig. 3 (a), the input signals of current source control part are the output signals of PFD and division ratio of FBDIV, the current source control module produce many paired digital signals, the weight of the two part account for 64 and 46 respectively. Then, the output voltages convey to current source generator part to control MOS switch. We can know that the current source structure is same to the current biased structure in CP, and they both controlled by Vctrl, the difference is their numbers are proportional, so that $I_{CP}$ is proportional to $I_{vco}$. There are two output current sources, Vvco and Vfb. In current source generator part, except some basic normal open current source branches only charge to Vvco to ensure that the CCO oscillate, each current source to Vvco corresponding charge to Vfb. Because of the two opposite switch control, current switchover between Vvco and Vfb, which can eliminate the charge sharing when Vvco=Vfb. Furthermore, each current source to Vfb corresponding connect to GND, which can ensure the current source will not shut down when the Vctrl changes. When Vvco needed to change, we can adjust Vfb to the same as Vvco through AMP to keep Vvco=Vfb shown as fig. 4(a), because it doesn’t matter that Vfb has bigger voltage fluctuation, it is effective to avoid charge sharing effect and suppress the noise of switch. Finally, we get Vvco to control the drive current of the ring oscillator.
As shown in fig.3 (b), the proposed CCO frequency range allows PLL to be optimized for minimum jitter or minimum power. Fig.4 (b) shows the post-layout simulation result of the tuning curve of the CCO at different corners. The tuning range is simulated by sweeping the input voltage $V_{vco}$ controlled by V-I module. It shows that the CCO can cover the frequency range from 200MHz to 3.5GHz at different corners.

3.3. Fast-Lock Module

As shown in fig.5 (a), the fast locking module includes three parts, start decision, Voltage conversion and sampling hold, they are shown as fig.5 (b)(c)(d) respectively. The signal sequence diagram of the first part is shown as fig.6, it shows that the fast locking module will work (signal D is
effective) when the frequency of feedback divider is less than frequency of reference, after the voltage conversion, the voltage signal controls the sampling hold circuit charge up to the capacity of LPF to increasing the loop speed.

4. Implementation and measurement results
The proposed PLL was implemented in 65nm CMOS process. The core area is 0.05mm². The supply voltage is 1.2V and 1.5V. The measurement results show the PLL can generate frequency range from 200MHz to 1.6GHz. Fig.8 shows the spectrum at carrier frequency of 800MHz, the reference spur is -54dBm. The measured RMS jitters at 1.6GHz is less then 0.8ps when the supply noise under the 1% of itself. The fast-lock process lasts less then 3us, and the complete lock time is determined as 1000 input cycles.

5. Summary
An adaptive bandwidth low-power low-jitter 8MHz to 1600MHz PLL was proposed and implemented in 65nm CMOS process, and input range is 1MHz to 800MHz. The output range is increased by post divider. The adaptive bandwidth increases both the input and the output range with no stability problems. The self-biased CP and proposed V-I structure maintain the loop bandwidth process independent. A simple RO is developed to minimize the power consumption and area. And a fast-lock structure is adopted to increase the locking speed of the PLL.
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