Design space exploration of neural network activation function circuits

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Design Space Exploration of Neural Network Activation Function Circuits
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Abstract—The widespread application of artificial neural networks has prompted researchers to experiment with FPGAs and customized ASIC designs to speed up their computation. These implementation efforts have generally focused on weight multiplication and signal summation operations, and less on activation functions used in these applications. Yet, efficient hardware implementations of nonlinear activation functions like Exponential Linear Units (ELU), Scaled Exponential Linear Units (SELU), and Hyperbolic Tangent (tanh) are central to designing effective neural network accelerators, since these functions require lots of resources. In this paper, we explore efficient hardware implementations of activation functions using purely combinational circuits, with a focus on two widely used nonlinear activation functions, i.e., SELU and tanh. Our experiments demonstrate that neural networks are generally insensitive to the precision of the activation function. The results also prove that the proposed combinational circuit based approach is very efficient in terms of speed and area, with negligible accuracy loss on the MNIST, CIFAR-10 and ImageNet benchmarks. Synopsys Design Compiler synthesis results show that circuit designs for tanh and SELU can save between \(3.13 \times 7.69\) and \(4.45 \times 8.95\) area compared to the LUT/memory based implementations, and can operate at 5.14GHz and 4.52GHz using the 28nm SVT library, respectively. The implementation is available at: https://github.com/ThomasMrY/ActivationFunctionDemo.

Index Terms—Artificial Neural Networks; Activation Functions; Exponential Linear Units (ELU), Scaled Exponential Linear Units (SELU), Hyperbolic Tangent (tanh).

I. INTRODUCTION

Artificial neural networks (ANN) are deployed in a wide range of applications, such as image recognition, speech recognition, and natural language processing. Speeding up neural network inference and reducing power consumption have become essential in order to enable ANN adoption in edge devices where low-power and low-latency are required. Current CPUs and GPUs are ill-suited for this class of devices, leading many researchers to pursue custom FPGA or ASIC accelerators.

ANNs consist of neurons, which sum incoming signals and apply an activation function, and connections, which amplify or inhibit passing signals. When the neuron’s activation function is nonlinear, the two-layer neural network becomes a universal function approximator [1]. Various nonlinear equations, such as sigmoid, logistic, tanh, Rectified linear unit (ReLU), Scaled Exponential Linear Unit (SELU), etc. [2] have been used to implement activation functions. Researchers in [3] show that nonlinear activation functions affect the learning and generalization capabilities of ANNs.

The rationale for focusing on the efficient implementation of exponential functions is twofold: (a) exponential functions are used in several activation functions, such as ELU, SELU, tanh, and sigmoid, and (b) the ELU [4] and SELU [5] functions have been shown (i) to significantly decrease training time, (ii) to push mean activations closer to zero, (iii) to not require batch normalization, and (iv) to alleviate the vanishing gradient problem. For example, the SELU activation function provides lower and upper bounds on the gradient variance and removes the vanishing/exploding gradient problem. Therefore, we expect a wider adoption of these activation functions in the future and attempts to reduce their hardware area, latency, and power consumption.

However, straightforward implementation of the aforementioned nonlinear activation functions in hardware is very expensive because most of these equations require exponentiation and division [6]. Most of accelerators do not implement an ISA [7]–[9] but rather create modules individually, therefore preventing designers from amortizing the costs of physical activation functions. Thus, besides pushing for the efficient execution of the matrix multiplication operations, special attention should also be paid to the other components of the ANN acceleration hardware. This holds true for the activation function. Each neuron in the hidden and output layers needs an activation function. Therefore, small implementation inefficiencies in the activation function can quickly add up. In fact, to achieve a significant speedup, hardware accelerators possess thousands or more processing elements (PEs). Hence, the number of hardware activation function components can be significant, and efforts to optimize activation function circuits could dramatically decrease ANN area and power requirements [10]. For example, if the tanh function is implemented using a 10-bit output and 1000 data points, the storage of the function values will require a 10Kb memory structure. Having hundreds of these modules in a design would require multiple megabits of storage. Indeed, in [11], the authors compare 8-bit neurons ReLU and tanh/sigmoid activation functions. They show that replacing the ReLU with tanh increases the neuron area by 20% and neuron energy by 36%.

In general, nonlinear functions like tanh cannot be effectively approximated using only combinational logic. However, deep neural networks can tolerate low precision operations, therefore lending themselves to such approximations. Using purely combinational logic has the benefits of providing low latency with small area overhead compared conventional ROM-based approaches. We illustrate this point using the tanh and SELU functions. Their implementations are generalized and open-sourced.

In this work, we explore the design space trade-offs of neural network activation function circuits. In particular, we focus on the efficient implementation of activation functions using purely combinational logic for higher clocking speed and smaller area overhead. The rest of this paper is organized as follows: previous works are introduced in Section II, in Section III and IV we present a detailed implementation of the SELU and tanh functions, Section V summarizes the experimental results and Section VI concludes this paper.

II. RELATED WORK

Various approaches have been proposed for implementing activation functions in hardware. Generally, these methods fall into two categories: piecewise approximations and look-up table (LUT) based approaches [12]. In this work, we consider the six most commonly used approaches to make the review concise. On the whole, high-fidelity approximations tend to use more resources and have higher latencies, while low-fidelity implementations incur approximation losses but are faster and require fewer hardware resources. In Figure 1, we plot the approximation of the \(e^x\) curve with methods 1, 2, 4 and 5. Method 3 (CORDIC algorithm [13]) and method 6 (Optimized
LUT-based method) are omitted as they require too much resource to be directly implemented in hardware.

A. Storing function values in LUTs

Look-up tables (LUT) are the most commonly used method to implement activation functions in hardware. The function values are divided into equal sub-ranges and each sub-range is approximated by a value stored in a LUT. For LUT implementations, raising precision requires increasing the sampling rate, adding more storage and increasing latency.

B. Storing parameters in LUTs

Instead of storing the function values directly, this method keeps the function slope and the function intercept in the LUT. The function value can then be calculated using the following formula, where \( k \) is the slope and \( b \) is the function intercept. This approach is a general form of storing function values in LUTs with \( k = 0 \) (cf. II-A).

\[
y = kx + b
\]

This method leads to a small improvement on the accuracy, but it also has to store more data and uses an adder and a multiplier to calculate the function values.

C. CORDIC algorithm

The third method is the CORDIC algorithm. It uses shift, addition and subtraction operations approximate the nonlinear activation function. The CORDIC algorithm requires less area than storing the parameters in LUTs, but more clock cycles and hardware modules are required to compute the activation function. While the algorithm achieves higher approximation accuracy, its increase in latency may not be suitable for deployment in low-latency edge devices.

D. Taylor series expansion

The Taylor series expansion can be used to approximate a nonlinear activation function to any precision. The expansion formula is of the form:

\[
f(x) = \sum_{n=0}^{\infty} \frac{f^{(n)}(0)}{n!} (x - x_0)^n
\]

This method does require multipliers and several clock cycles to perform the calculation.

E. Approximation formula

The method introduced in [14] uses the following formula to approximate the exponential function:

\[
e^x \approx Ex(x) = 2^{1.44x}
\]

(3)

Based on this formulation, one can calculate the sigmoid function as:

\[
\text{Sigmoid}(x) = \frac{1}{1 + 2^{-1.44x}} \approx \frac{1}{1 + 2^{-1.5x}}
\]

(4)

whereas the tanh function can be calculated as:

\[
tanh(x) = 1 - 2\text{Sigmoid(}-2x\text{)}
\]

(5)

The method requires four cycles to approximate the sigmoid function. The authors designed a structure to calculate the expression \( 2^{-1.5x} \), which takes two cycles. An add and a division operations are also performed and take one cycle each. For the tanh function approximate an additional clock cycle is required. The implementation of this approximation formula uses fewer resources than the CORDIC approach, but its latency is still high.

F. Optimized LUT-based method

This approach is an optimized LUT-based method combined with a Taylor series expansion. The equation is expanded up to the fifth-order:

\[
tanh(x) \approx x - \frac{x^3}{3} + \frac{2x^5}{15}
\]

(6)

When \( 0.04 \leq x^5 \leq 0.02 \), one can use the approximation \( \tanh(x) \approx x \). By solving the inequality, one gets \( x \geq 0.39 \), and \( \tanh(2.99) \approx 1 \). Only the values in the \([0.39, 2.99]\) range need to be stored.

In all, LUT based methods need storage/memory and an extra pipeline stage for the memory access. All these methods, except the one that stores function values in LUTs, either require relatively complex calculations/logic or several clock cycles to minimize the approximation error. According to our experiments in Section V, ANNs are generally insensitive to activation function precision. This is a key insight that allows us to simplify the approximation method without sacrificing the system accuracy. In the following sections, we analyze the activation functions and present our proposed combinational circuit based implementation method.

III. ACTIVATION FUNCTIONS EXPLORATION

In this section, we discuss the nonlinear activation functions realized using our proposed design approach. We define the sigmoid and tanh function as:

\[
\text{sigmoid}(x) = \frac{1}{1 + e^{-x}}, \quad \tanh(x) = \frac{e^x - e^{-x}}{e^x + e^{-x}}
\]

(7)

Compared to sigmoid function, the tanh function passes through zero and can be approximated as \( y = x \) around zero. As a result, when the absolute value of the input is small enough, one can perform the matrix operation directly, therefore, the training process is relatively easy. In principle, sigmoid and tanh have similar expressive ability, but in practice, sigmoid is equivalent to an activation function with a bias. It still needs the real bias term to offset its influence, which can affect the optimization. Therefore, the tanh function is used more often. Furthermore, it converges faster than the sigmoid function.

The tanh function has been shown experimentally to outperform the sigmoid function. There are two reasons for this: the output of the tanh function is normalized around 0, producing both positive and negative outputs. The sigmoid is not, introducing a systematic bias. Second, when the output of the neuron restricted to \([1, 1]\) the activation is more likely to be close to 0, so the neurons are generally
less saturated with \textit{tanh} than with \textit{sigmoid}, allowing gradients to better propagate and speeding up learning [15].

In [5], the authors introduced the \textit{SELU} function and analytically proved that neuron activations converge towards zero mean and unit variance. This allows networks with \textit{SELU} activations to train deeper models, speed up learning, and use stronger regularizers without sacrificing accuracy. This is the main motivation behind focusing our work on the efficient implementation of exponential functions.

We define ELU and \textit{SELU} as:

\[ ELU(x) = \begin{cases} 
  x & \text{if } x > 0 \\
  a e^x - a & \text{else} 
\end{cases} \]

\[ SELU(x) = \lambda ELU(x). \]

Here \( \lambda = 1.0507 \) and \( a = 1.6733 \).

IV. Activation Function Implementation

A. Implementation of the tanh function

In this section, we introduce our method for implementing the \textit{tanh} activation function using exclusively combinational circuits. We consider only the intervals where the function changes significantly.

1) Properties of the \textit{tanh} function: \textit{Tanh} is an odd function, meaning that it is symmetric with respect to 0. In order to approximate it, we only need to observe the positive half of the function. As it converges to 1, we approximate its value in the range \([0, 1] \) for the targeted precision in this work.

We divide the activation function range into \( 2^k \) segments evenly with the step \( \frac{1}{2^k} \). The approximation error depends on the number \( k \), which controls the sampling density. The larger the \( k \) is, the lower the approximation errors are, but more complex the implementation. During training, the exact \textit{tanh} function is used to calculate the gradients, since the approximate function is non-differentiable. The approximated function is used for the forward pass.

2) Encoding the value of the activation function: After selecting a sampling rate, we choose the output value’s integer and fractional parts bit-width. The integer part is either 0 or 1. For the illustrative case, in order to simplify the complexity of the combinational logic, we choose 7-bits to encode the output value of the activation function: 1-bit for the integer part and 6-bits for the fractional part.

3) Generating the Karnaugh map for the \textit{tanh} function: Boolean functions can be expressed in their canonical form: by listing the input values on the left side of the truth table and the output values on the right side, we get a Karnaugh map. Figure 2 shows the Karnaugh map for one of the \textit{tanh} activation bits. By analyzing the map, one can derive the needed circuit for implementing the bit. We repeat this procedure for all the bits of the \textit{tanh} activation function.

| TABLE 1 |
| --- |
| \textbf{AND plane} |
| \( p_1 \) & \( \{p_{15}, p_{16}, p_1\} \) |
| \( p_2 \) & \( \{p_{15}, p_{16}, p_1\} \) |
| \( p_3 \) & \( \{p_{15}, p_{16}, p_1\} \) |
| \( p_4 \) & \( \{p_{15}, p_{16}, p_1\} \) |

| \textbf{OR plane} |
| --- |
| \( Y_0 \) & \( \{p_{15}, p_{16}, p_1\} \) |
| \( Y_1 \) & \( \{p_{15}, p_{16}, p_1\} \) |
| \( Y_2 \) & \( \{p_{15}, p_{16}, p_1\} \) |
| \( Y_3 \) & \( \{p_{15}, p_{16}, p_1\} \) |

This reduces the number of individual circuits. As an illustration, here is the expression of one bit of the output value:

\[ Y_i = X_0 X_i + X_i X_0 + X_0 X_1 X_0 + X_1 X_0 \]

\[ X_i \text{ refers to the } i+1 \text{-th bit of the input value, and } Y_i \text{ refers to the second bit of the output value.} \]

4) Combinational logic for the \textit{tanh} function: Finally, we can implement the logic expression using an RTL language to get the logical circuits. As for the negative part of the function, since the \textit{tanh} is an odd function, we can deliver the sign bits to the output directly. If we use \( g(x) \) to represent the ladder function between \([ -2, 2] \), the approximated activation function \textit{tanh} can be written as follows:

\[ \text{tanh}(x) = \begin{cases} 
  1 & x \geq 2 \\
  2 & 2 \geq x \geq -2 \\
  -1 & -2 \geq x \n\end{cases} \]

5) Simulation and validation: Once we have the RTL module, we need to simulate it to check the logic expression and make sure it approximates the desired function. Next, we analyze the time delay of the combinational circuit and check whether the activation function lies on the critical path of the design. After functional and timing testing, if there exist any race conditions or hazards, we change the Karnaugh map to remove them.

After simplifying the logic expression, we obtain the final expressions of the \textit{tanh} function as illustrated in Table 1.

B. Implementation of the \textit{SELU} activation function

We demonstrate in this section the implementation of the \textit{SELU} function using only combinational circuits.

1) Properties of the \textit{SELU} activation function: From the formula 8, the positive part of the \textit{SELU} function is linear, so we only need to approximate the negative part. Considering \( e^{-3.875} \approx 0.0208 \approx 0 \), if the input value is less than \(-3.875\), the output value is \(-\alpha\), \( \alpha \) being a static predetermined parameter. We then divide the interval \([-3.875, 0]\) into \( k \) segments evenly.

2) Encoding the value of the activation function: We encode the input value with 5 bits. To maintain precision, we encode the output value into 8-bits, 1 bit for the integer part and 7-bits for the fractional part. In this way, it can be represented as \textit{tanh} 8 5.

3) Generating the Karnaugh map for the \textit{SELU} function: We can construct the truth table and Karnaugh map in a similar fashion as described in Section IV.A.3. From the Karnaugh map, we draw the Karnaugh circle to get the simplest logical expression without race condition and hazards. In total, we arrive at 31 logical expressions. Here we show an illustration using one bit of the output value:
\[ Y_i = X_{i,1}X_{i,2} + X_{i,3}X_{i,4} + X_{i,5}X_{i,6} + X_{i,7}X_{i,8} + X_{i,9}X_{i,10} + X_{i,11}X_{i,12} + X_{i,13}X_{i,14} + X_{i,15}X_{i,16} + X_{i,17}X_{i,18}; \]  
\[ Y_{i+1} = A_i + B_i + Y_i; \]

\[ X_i \] refers to the \( i \)-th bit of the input value, and \( Y_i \) refers to the second bit of the output value.

In Figure 3, each color block refers to a product, and the logic expression is the sum of all the products. The blocks that have the same color refer to the same product.

![Karnaugh map of one of the output bits of SELU activation function](image)

4) Combinational logic of the SELU function: The approximation of SELU using purely combinational logic is shown in Table II. The table shows the final complete logic expressions. We define the SELU function using the formulation shown in equation 13. It is worth noting that we only define it on the \((-3.875, 0)\) interval, as the function is linear for \( x \geq 0 \) and constant for \( x \leq -3.875 \).

\[ \text{SELU}(x) = \lambda f(x) \]
\[ \begin{align*}
0 \leq x &< -3.875 \\
-3.875 &\leq x
\end{align*} \]

5) Simulation and validation: The purpose of the simulation is the same as in the case of the tanh activation function. As more variables may lead to race conditions and hazards more easily, all possible combinations should be simulated.

More accurate approximations can be achieved by increasing the number of bits for inputs and outputs. Increasing the number of bits in the input helps break the function into more linear segments. Whereas, a larger number of bits in the output representation boosts its precision. In all, using higher bit-widths improves the approximation accuracy but also leads to more complex circuits.

V. EXPERIMENT

Look-up table based designs are the most common implementation of activation functions. Therefore, in our comparative study, for the baseline designs, we implement the tanh and SELU functions using look-up tables. The function values storage based implementation is denoted as \((\text{ROM}_y)\) and the parameters storage based one is \((\text{ROM}_k,b)\). Their construction uses LUTs and follows the procedures described in Section II. Their comparison with the proposed combinational circuit based approach is done in terms of approximation error, power, area, and network accuracy.

The evaluation is conducted in a two-step, software-hardware approach. First, we evaluate the approximation method in software using PyTorch to verify the neural network accuracy. It is worth noting that the procedure may run multiple iterations to find out an appropriate bit-width. Second, for a selected bit-width, the full neural network is implemented in hardware. We then perform circuit-level analysis on the RTL code and deploy it on the FPGA board for further system-level validation.

A. Approximation Error

The average errors for the three different methods – the proposed combinational circuit based approach, ROM_y and ROM_k,b – are shown in Table III. The errors for the tanh and SELU functions are bounded to the ranges \( 2 < x < 2 \) and \(-3.875 < x < 0 \), respectively. The average error is calculated using the following formula:

\[ \text{Average Error} = \left( \frac{1}{N} \sum_{i=1}^{N} |P_i - A_i| \right) \times 100\% \]

\[ \text{TABLE II}

| Input | SELU \& tanh 8-bit Implementation |
|-------|----------------------------------|
| \( X_{i,1} \) | \( X_{i,2} \) |

\[ \begin{align*}
\text{Table III}

| Active Function | Tanh-2,4 | SELU-8,5 |
|-----------------|----------|----------|
| \( \text{index} \) | \( \text{AE} \) | \( \text{Area(\mu m^2)} \) | \( \text{AE} \) | \( \text{Area}(\mu m^2) \) |
| \( \text{Our method} \) | 4.19% | 97.65 | 2.22% | 137.59 |
| ROM \( y \) | 4.19% | 306.12 | 2.22% | 612.24 |
| ROM \( k,b \) | 0.52% | 751.44 | 0.17% | 1162.93 |

P is the function value, A is the approximate value, and N represents the number of sample points. Since piecewise linear approximation is used in our proposed method, the average error is the same as in the function values storage approach (\( \text{ROM}_y \)) and larger than when the parameters are stored (\( \text{ROM}_k,b \)). The parameters storage approach does use more resources for this slight accuracy improvement (cf. V-B).

B. Resources Analysis

To get more accurate results, we synthesized the different designs using a 28nm SMV library. The absolute time delays for the tanh and SELU functions are 0.1947ns and 0.221ns. This means that the combinational logic can operate at the maximum frequencies of 5.14GHz (tanh) and 4.52GHz (SELU). The area overheads of the tanh and SELU implementations are shown in the Table III.

The proposed combinational circuit based method implementation of the tanh function saves 68.1% and 87.0% in area compared to function

\( \text{TABLE III} \)

\[ \begin{align*}
\text{COMPARISON OF AE(AVERAGE ERROR) AND AREA}
\end{align*} \]
values storage approach (ROM_y) and the parameters storage method (ROM_k_b), respectively. For the SELU function implementation, the area savings are 77.53% and 88.17% over ROM_y and ROM_k_b, respectively. The three methods are deployed on the Xilinx VCTV2000T FPGA board. The power consumption results are reported in Figure 4.

One clock cycle is needed to get the function value from the LUT for both the ROM_y and ROM_k_b approaches. For the ROM_k_b, two clock cycles are needed for the linear function computation. On the other hand, the proposed method is purely combinational.

C. Inference Accuracy

In this section, we focus on the network accuracy. We use Pytorch with bit-wise operations to approximate the activation functions. We train the neural networks using the original, full precision activation function implementations. Then in the validation phase we replace the activation functions with their approximation function circuits. We make no attempt to retrain the network after changing the activation function. Since such an attempt may remove accuracy losses incurred by quantizing the activation functions.

| TABLE IV PERFORMANCE OF OUR METHOD ON ANN COMPARED WITH ORIGINAL DESIGN |
|-----------------------------------------------|
| MNIST | CIFAR-10 | ImageNet (Top1/Top5) |
|-------|----------|---------------------|
| Tanh(Original) | 96.15% | 87.17% | 42.39%/67.61% |
| Tanh_k 5 | -0.2% | -5.07% | -8.16%/-8.94% |
| Tanh_k 7 | -0.0% | -1.96% | -7.83%/-8.42% |
| Tanh_k 7 6 | +0.0% | -0.29% | -7.23%/-8.0% |
| SelU(Original) | 97.67% | 86.79% | 39.26%/63.342% |
| SelU_k 5 | +0.04% | -4.15% | -0.122%/+0.458% |
| SelU_k 7 | +0.01% | -4.47% | -0.004%/+0.866% |
| SelU_k 8 5 | +0.37% | -0.69% | +0.386%/+1.278% |

We test the proposed method with LeNet on the MNIST dataset, VGG-16 on the CIFAR-10, and AlexNet on the ImageNet dataset. The experimental results show an accuracy loss of 0.05% and an increase of 0.37% compared to the original network on MNIST using tanh_k 7 4 and SELU_k 8 5, respectively. In case of the CIFAR-10 experiments, we get an accuracy loss of 1.96% and 0.69% for tanh_k 7 4 and SELU_k 8 5. For the experiments on the ImageNet, the accuracy losses are 7.83% on top-1 and 8.42% on top-5 under tanh_k 7 4, while there are gains of 0.368% on top-1 and 1.278% on top-5 for the SELU_k 8 5. The results of the comparative study of the exact implementation and the proposed approximation method are summarized in Table IV. When the quantization method is applied, the network inference accuracy increases. The overall effect of the quantization precision on the inference accuracy follows the pattern observed in other studies [16].

VI. CONCLUSION

In this work, we propose an efficient approximation scheme for activation functions using purely combinational logic, which takes only one clock cycle. We should its implementation and performance on two widely used activation functions, i.e., tanh and SELU. We conduct a comparative study of the proposed method with other widely used methods, i.e., storage based approaches. Based on the average approximation errors, our method has the best performance to circuit complexity ratio. Activation quantization bears little effect on network accuracy. The hardware implementation of the proposed activation functions is realized using the 28nm SVT library to further validate the efficiency of the proposed approach in terms of area and timing delay. Area reductions of 68.1% and 87.0% for the tanh function, and 77.53% and 88.17% for the SELU function are recorded when compared with the two baseline LUT-based activation function implementations (ROM_y and ROM_k_b).

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