Third-Order Elliptic Lowpass Filter for Multi-Standard Baseband Chain Using Highly Linear Digitally Programmable OTA

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Abstract. In this paper, a third-order elliptic lowpass filter is designed using highly linear digital programmable balanced OTA. The filter exhibits a cutoff frequency tuning range from 2.2 MHz to 7.1 MHz, thus, it covers W-CDMA, UMTS, and DVB-H standards. The programmability concept in the filter is achieved by using digitally programmable operational transconductors amplifier (DPOTA). The DPOTA employs three linearization techniques which are the source degeneration, double differential pair and the adaptive biasing. Two current division networks (CDNs) are used to control the value of the transconductance. For the DPOTA, the third-order harmonic distortion (HD3) remains below -65 dB up to 0.4 V differential input voltage at 1.2 V supply voltage. The DPOTA and the filter are designed and simulated in 90 nm CMOS technology with LTspice simulator.

1. Introduction
Multi-standard systems have become indispensable in today wireless and wireline communication. Through these systems, it is possible to connect to networks using a variety of communication standards inducing Bluetooth, W-CDMA, UMTS, DVB-H and IEEE 802.11a/g standards. The multi-mode filter is a fundamental component in these systems. It serves as a channel selector by adjusting its bandwidth with regards to the targeted standard specifications[1], [2].

The main adopted structures for implementing the multi-mode filter are the Gm-C, active-RC and MOSFET-C. For high frequency and low power application, the Gm-C structure is preferable due to the open loop operation of the operational transconductor amplifier (OTA). On the other hand, the active-RC and MOSFET-C structures consume high power in the high-frequency applications because they use local feedback around the active elements [3]. The main disadvantage of the Gm-C filter is the high nonlinearity due to the open loop operation of the used OTA. Hence, many techniques have been reported in the literature in order to enhance the linearity of the OTA [4].

The paper is organized as follow: Sec. 2 presents the design of the digitally programmable OTA and the current division network. Sec. 3 illustrates the proposed third-order elliptic lowpass filter. The simulation results of the DPOTA and the complete filter are given in Sec. 4. In [5], the same proposed DPOTA is used to implement a 4th-order Butterworth lowpass filter for multi-standard receiver baseband chain. However, the elliptic transfer function has the best selectivity among all other types.
2. Digitally Programmable OTA

The presented DPOTA circuit employs three different linearization techniques [6], [5]. The first technique is the source degeneration using MOS transistors [7] in which a resistance is connected between the two sources of the differential pair’s transistors. The resistance can be implemented by a resistor or by MOS transistors working in the linear region. In the case of using a resistor of value \( R \), to improve the linearity significantly a large \( R \) is needed. However, the overall transconductance will be limited \( (G_m \approx 1/R) \). The second technique is the adaptive biasing [8], the concept of adaptive biasing allows the input voltage to contribute in the biasing current. Hence, the non-linear term is canceled by the input voltage. The third technique is the double differential pair, which enhances the linearity performance by canceling the third-order distortion[9]. A common mode feedback circuit (CMFB) is added to the balanced OTA. The CMOS realization of the balanced OTA is shown in Fig. 1. Each of the following pairs of transistors are identical \((M_1, M_2), (M_3, M_4), (M_5, M_6)\) and \((M_7, M_8)\). The transistors \( M_5, M_6, M_7, M_8 \) operate in linear region. Then the output differential current of the first source degenerated differential pairs is given by

$$I_o = I_1 - I_2 = \sqrt{2K_{n1}I_{T1}}V_d\sqrt{1 - \frac{K_{n1}V_d^2}{8a_1^2I_{T1}}}$$

where \( a_1 = 1 + (K_{n1}/4K_{n3}) \). From Taylor expanding, the third-order distortion is canceled if the following condition is satisfied

$$\frac{I_{T1}}{I_{T2}} = \left(\frac{K_{n1}}{K_{n3}}\right)^3\left(\frac{a_2}{a_1}\right)^6$$

By proper transistors sizing and choosing proper biasing currents according to (2), the third-order harmonic distortion can be eliminated. However, due to mobility degradation effect, the third-order harmonic can be reduced only. The biasing voltage \( V_b \) is used to bias the squaring circuits in order to achieve the maximum linearity.

![Figure 1. The CMOS realization of the proposed OTA.](image)

The squaring circuit [8] is added to the proposed OTA to make the biasing currents adaptive to the input voltage. Then the non linear terms in each differential pair is reduced.
2.1. The current division network

The programmability concept in the presented DPOTA is introduced by using two current division network circuits [10] as shown in Fig. 2. The adopted CDN based on cascaded NMOS current division cell (CDC) by PMOS CDC. It has no restriction on the number of the controlling bits due to the supply voltage limitation where the voltage levels are generated from one cell to another. Moreover, the structure of the CDC has the advantages of the low input impedance and high output impedance. Hence, no need for virtual ground nodes [10]. Also, this CDN can divide bidirectional input current and the transistors matching requirements are relaxed since only the transistors within each CDC required to be matched.

Each of the two output currents ($I_{o1}, I_{o2}$) of the proposed OTA in Fig. 1 is connected as input for one CDN. The two CDNs are controlled by 3-bit word ($a_0, a_1, a_2$). The 3-bit CDN circuit divides the input current with controlling factor ($\alpha$), that can be expressed as

$$\alpha = \frac{1}{2^n} \left(1 + \sum_{i=0}^{n-1} 2^i a_i \right)$$

(3)

where $n$ is the number of the digital control bits. The adopted tuning technique preserve the overall linearity performance of the proposed OTA. The overall output currents of the proposed digital programmable OTA is given by

$$I_{out1} = -I_{out2} = \alpha(a_0, a_1, a_2) G_m (V_1 - V_2)$$

(4)

where $G_m$ is the transconductance value. The current gain $\alpha(a_0, a_1, a_2)$ is a function of the digital control bits as explained in (3).

3. Third-Order Elliptic Lowpass Filter Design

A third-order elliptic lowpass filter is designed using the presented DPOTA. The elliptic transfer function has the best selectivity, however it suffers from the ripples in pass and stop bands. The passive implementation of the filter is shown in Fig. 3. Fully differential implementation of the filter using seven identical DPOTA and five capacitors is shown in Fig. 4, where the passive inductor is implemented by four DPOTA ($G_{m3} - G_{m6}$) based on gyrator-C structure. $G_{m2}$ and $G_{m7}$ implement active resistors and $G_{m1}$ acts as buffer transconductance. The values of the capacitors are extracted such that to make the tuning over WCDMA (2.2 MHz), UMTS (5 MHz) and DVB-H (7 MHz) standards. The capacitance of $C_1$, $C_2$, $C_3$ and $C_4$ are 0.2 pF, 0.2 pF, 50 fF and 0.2 pF, respectively. The cutoff frequency of filter can be tuned digitally from...
2.2 kHz to 7.1 MHz by changing the digital input of the DPOTA. More pass-band gain can be achieved by increasing the transconductance of $G_{m1}$.

![Figure 3. The passive prototype of the third-order elliptic lowpass filter.](image)

Figure 4. The active implementation of the third-order elliptic lowpass filter.

4. The Simulation Results

4.1. DPOTA simulation
The proposed circuit is validated through simulation tests. LTspice simulator is used with 90 nm BSIM4 (level 54) technology under ±0.6 V supply voltage. Fig. 5 shows the transconductance of the proposed programmable OTA while $\alpha$ is varied from 0.125 to 1 with 0.125 steps. The values of the transconductance can be controlled from 11.65 $\mu$A/V to 93.5 $\mu$A/V. The output differential current versus the input differential voltage is shown in Fig. 6. The linearity performance of the proposed OTA is evaluated by measuring the third harmonic distortion (HD3) of the differential output current while the input voltage frequency is 10 MHz and peak to peak amplitude is varied from 0.1 V to 0.5 V. Fig. 9 shows that the HD3 remains below -60 dB. The bandwidth of the OTA is varying from 68 MHz to 74.2 MHz as shown in Fig. 10. Fig. 7 shows the input referred noise spectral density which is inversely proportional to $\alpha$, at 1 MHz and for ($\alpha = 0.125$) it is 268 nV/$\sqrt{Hz}$ while for ($\alpha = 1$) it is 139.6 nV/$\sqrt{Hz}$. The overall power consumption of the OTA is 669 $\mu$W as shown in Fig. 8.

4.2. The filter simulation
The proposed filter in Fig. 4 is simulated in 90 nm CMOS technology with LTspice simulator. The filter consumes 4.68 mW under 1.2 V supply voltage. The magnitude response of the filter in Fig.11 shows the tuning range from 2.2 MHz to 7.1 MHz. The filter simulation results are summarized in table 2. The DC gain, cutoff frequency, the input referred noise and the third-order inter-modulation distortion at an input voltage of 200 mV$_{pp}$, amplitude with frequencies 0.8 MHz and 0.9 MHz for LPF are given.
Figure 5. The transconductance of the proposed programmable OTA while $\alpha$ is varied from 0.125 to 1 with 0.125 steps.

Figure 6. The output differential current of the proposed programmable OTA while $\alpha$ is varied from 0.125 to 1 with 0.125 steps.

Figure 7. The input referred noise for minimum and maximum $\alpha$.

Figure 8. The total power consumption.

Table 1. Main specifications of the proposed DPOTA

| Specifications               | This work          |
|------------------------------|--------------------|
| Supply voltage (V)           | ± 0.6              |
| Power dissipation ($\mu$W)   | 669                |
| Transconductance ($\mu$A/V)  | 11.65 - 93.5       |
| Controlling bits             | 3                  |
| Input referred noise ($\text{nV}/\sqrt{\text{Hz}}$) | 268.5 - 139.6     |
| Technology                   | 90 nm              |
Figure 9. The third-order harmonic distortion of the differential output current at the maximum transconductance value.

Figure 10. The frequency response of the proposed programmable OTA while \( \alpha \) is varied from 0.125 to 1 with 0.125 steps.

Figure 11. The magnitude response of the filter.

| Parameter                  | W-CDMA | UMTS  | DVB-H |
|----------------------------|--------|-------|-------|
| Cutoff Frequency (MHz)     | 2.2    | 4.5   | 7.1   |
| DC Gain (dB)               | -1.15  | 0.09  | 0.99  |
| IM3 (dB)                   | -27    | -36.54| -47.3 |
| Input referred noise (nV/\sqrt{Hz}) | 451.6  | 370.7 | 447.3 |
5. Conclusion
A digital programmable OTA with linearity enhancement has been proposed. The adopted linearity techniques are the source degenerated using MOS transistor, double differential pair and the adaptive biasing. The tuning capability is introduced by using 3-bit current division network. The adopted tuning technique preserves the overall DPOTA linearity performance. The DPOTA consumes 669 μW under 1.2 V supply voltage. The proposed DPOTA performance has been evaluated through LTspice simulator using 90 nm technology. The simulation results shows HD3 of the DPOTA is below -60 dB up to 0.5 V differential input voltage. A third-order elliptic lowpass filter is designed using the proposed DPOTA. The filter cutoff frequency can be tuned from 2.2 MHz to 7.1 MHz which makes it suitable for multi-standard systems.

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