Runtime Enforcement of Programmable Logic Controllers

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With the advent of Industry 4.0, industrial facilities and critical infrastructures are transforming into an ecosystem of heterogeneous physical and cyber components, such as programmable logic controllers, increasingly interconnected and therefore exposed to cyber-physical attacks, i.e., security breaches in cyberspace that may adversely affect the physical processes underlying industrial control systems.

In this paper, we propose a formal approach based on runtime enforcement to ensure specification compliance in networks of controllers, possibly compromised by colluding malware that may tamper with actuator commands, sensor readings, and inter-controller communications. Our approach relies on an ad-hoc sub-class of Ligatti et al.’s edit automata to enforce controllers represented in Hennessy and Regan’s Timed Process Language. We define a synthesis algorithm that, given an alphabet $P$ of observable actions and a timed correctness property $e$, returns a monitor that enforces the property $e$ during the execution of any (potentially corrupted) controller with alphabet $P$, and complying with the property $e$. Our monitors correct and suppress incorrect actions coming from corrupted controllers and emit actions in full autonomy when the controller under scrutiny is not able to do so in a correct manner. Besides classical requirements, such as transparency and soundness, the proposed enforcement enjoys deadlock- and diverge-freedom of monitored controllers, together with scalability when dealing with networks of controllers. Finally, we test the proposed enforcement mechanism on a non-trivial case study, taken from the context of industrial water treatment systems, in which the controllers are injected with different malware with different malicious goals.

CCS Concepts: • Security and privacy → Formal security models; Cyber-physical systems security.

Additional Key Words and Phrases: Runtime enforcement, control systems security, PLC malware

1 INTRODUCTION

Industrial Control Systems (ICSs) are physical and engineered systems whose operations are monitored, coordinated, controlled, and integrated by a computing and communication core [53]. They represent the backbone of Critical Infrastructures for safety-critical applications such as electric power distribution, nuclear power production, and water supply.

The growing connectivity and integration in Industry 4.0 has triggered a dramatic increase in the number of cyber-physical attacks [31] targeting ICSs, i.e., security breaches in cyberspace that adversely affect the physical processes. Some notorious examples are: (i) the Stuxnet worm, which reprogrammed Siemens PLCs of nuclear centrifuges in the nuclear facility of Natanz in Iran [35]; (ii) the CRASHOVERRIDE attack on the Ukrainian power grid, otherwise known as Industroyer [58]; (iii) the recent TRITON/TRISIS malware that targeted a petrochemical plant in Saudi Arabia [19].

One of the key components of ICSs are Programmable Logic Controllers, better known as PLCs. They control mission-critical electrical hardware such as pumps or centrifuges, effectively serving as a bridge between the cyber and the physical worlds. PLCs have an ad-hoc architecture to execute simple repeating processes known as scan cycles (IEC 61131-3 [1]). Each scan cycle consists of three phases: (i) reading of sensor measurements of the physical process; (ii) execution of the controller

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code to compute how the physical process should evolve; (iii) transmission of commands to the actuator devices to govern the physical process as desired.

Due to their sensitive role in controlling industrial processes, successful exploitation of PLCs can have severe consequences on ICSs. In fact, although modern controllers provide security mechanisms to allow only legitimate firmware to be uploaded, the running code can be typically altered by anyone with network or USB access to the controllers (see Figure 1). Published scan data shows how thousands of PLCs are directly accessible from the Internet to improve efficiency [52]. Thus, despite their responsibility, controllers are vulnerable to several kinds of attacks, including PLC-Blaster worm [59], Ladder Logic Bombs [28], and PLC PIN Control attacks [5].

Extra trusted hardware components have been proposed to enhance the security of PLC architectures [45, 46]. For instance, McLaughlin [45] proposed a policy-based enforcement mechanism to mediate the actuator commands transmitted by the PLC to the physical plant. Mohan et al. [46] introduced a different architecture, in which every PLC runs under the scrutiny of a monitor which looks for deviations with respect to safe behaviours. Both architectures have been validated by means of simulation-based techniques. However, as far as we know, formal methodologies have been rarely used to model and formally verify security-oriented architectures for ICSs.

Runtime enforcement [22, 40, 56] is a formal verification/validation technique aiming at correcting possibly-incorrect executions of a system-under-scrutiny (SuS). It employs a kind of monitor [23] that acts as a proxy between the SuS and the environment interacting with it. At runtime, the monitor transforms any incorrect executions exhibited by the SuS into correct ones by either replacing, suppressing or inserting observable actions on behalf of the system. The effectiveness of the enforcement depends on the achievement of the two following general principles [40, 56]:

- **transparency**, i.e., the enforcement must not alter correct executions of the SuS;
- **soundness**, i.e., incorrect executions of the SuS must be prevented.

In this paper, we propose a formal approach based on runtime enforcement to ensure specification compliance in networks of controllers possibly compromised by colluding malware that may tamper with actuator commands, sensor readings, and inter-controller communications. combined with automatic recovery mechanisms.

Our goal is to enforce potentially corrupted controllers using secure proxies based on a subclass of Ligatti et al.’s edit automata [40]. These automata will be synthesised from enforceable timed correctness properties to form networks of monitored controllers, as in Figure 2. The proposed enforcement will enjoy both transparency and soundness together with the following features:

- **determinism preservation**, i.e., the enforcement should not introduce nondeterminism;
- **deadlock-freedom**, i.e., the enforcement should not introduce deadlocks.
divergence-freedom, i.e., the enforcement should not introduce divergencies;
mitigation of incorrect/malicious activities;
scalability, i.e., the enforcement mechanism should scale to networks of controllers.

Obviously, when a controller is compromised, these objectives can be achieved only with the introduction of a physically independent secure proxy, as advocated by McLaughlin and Mohan et al. [45, 46], which does not have any Internet or USB access, and which is connected with the monitored controller via secure channels. This may seem like we just moved the problem over to securing the proxy. However, this is not the case because the proxy only needs to enforce a timed correctness property of the system, while the controller does the whole job of controlling the physical process relying on potentially dangerous communications via the Internet or the USB ports. Thus, any upgrade of the control system will be made to the controller and not to the secure proxy. Of course, by no means runtime reconfigurations of the secure proxy should be allowed as its enforcing should be based on the physics of the plant itself and not on the controller code.

Contribution. First of all, we define the attacker model and the attacker objectives in an enforced ICS architecture such as that depicted in Figure 2. Then, we introduce a formal language to specify controller programs. For this very purpose, we resort to process calculi, a successful and widespread formal approach in concurrency theory for representing complex systems, such as mobile systems [16] and cyber-physical systems [39], and used in many areas, including verification of security protocols [3, 4] and security analysis of cyber-physical attacks [38]. Thus, we define a simple timed process calculus, based on Hennessy and Regan’s Timed Process Language (TPL) [29], for specifying controllers, finite-state enforcers, and networks of communicating monitored controllers.

Then, we define a simple description language to express timed correctness properties that should hold for a (possibly unbounded) number of scan cycles of the monitored controller. This will allow us to abstract over controllers implementations, focusing on general properties which may even be shared by completely different controllers. In this regard, we might resort to one of the several logics existing in the literature for monitoring timed concurrent systems, and in particular cyber-physical systems (see, e.g., [9, 24]). However, the peculiar iterative behaviour of controllers convinced us to adopt the sub-class of regular expressions that can be recognised by finite automata whose cycles always contain at least one final state; this is the largest class of regular properties that can be enforced by finite-state Ligatti et al.’s edit automata (see Beauquier et al.’s work [10]). In Section 5, we express a wide class of correctness properties for controllers in terms of (our) regular properties.

After defining a formal language to describe controller properties, we provide a synthesis function $\langle|-|\rangle^P$ that, given an alphabet $P$ of observable actions (sensor readings, actuator commands, and
inter-controller communications) and a deterministic regular property \(e\) combining events of \(P\), returns an edit automaton \(\langle e \rangle^P\). The resulting enforcement mechanism will ensure the required features mentioned before: transparency, soundness, determinism preservation, deadlock-freedom, divergence-freedom, mitigation and scalability. Then, we propose a non-trivial case study, taken from the context of industrial water treatment systems, and implemented as follows: (i) the physical plant is simulated in Simulink [44]; (ii) the open source PLCs are implemented in OpenPLC [8] and executed on Raspberry Pi; (iii) the enforcers run on connected FPGAs. In this setting, we test our enforcement mechanism when injecting the PLCs with 5 different malware, with different goals.

Outline. Section 2 describes the attacker model and the attacker objectives. Section 3 gives a formal language for monitored controllers. Section 4 defines the case study. Section 5 provides a language of regular properties to express controller behaviours; it also contains a taxonomy of properties expressible in the language. Section 6 contains the algorithm to synthesise monitors from regular properties, together with the main results. Section 7 discusses the implementation of the case study when exposed to five different attacks. Section 8 is devoted to related work. Section 9 draws conclusions and discusses future work. Technical proofs can be found in the appendix.

2 ATTACKER MODEL AND ATTACKER OBJECTIVES

In the following sections, we will propose an enforcement-based architecture for ICSs (as those depicted in Figure 2) to counter attacks complying with the following attacker model:

- malware injected in one or more PLCs may forge/drop actuator commands, modify sensor readings coming from the plant, forge/drop inter-controller communications;
- malware injected in different PLCs of the same field communications network may collaborate/communicate with each other to achieve common objectives;
- the attacker runtime behaviour may vary as it may depend on the received sensor signals and the communications with other PLCs;
- malicious alterations of sensor signals at network level, or within the sensor devices, are not allowed (they are out of the scope of this paper);
- scan cycles must be completed within a specific time, called maximum cycle limit, which depends on the controlled physical process; if this time limit is violated then the controller stops and throws an exception [59]; we assume that the injected malware never violates the maximum cycle limit because not interested in causing the immediate shutdown of a PLC;
- the enforcers added in the architecture are physically independent secure proxies with no Internet or USB access, and connected with the controller via secure channels; as a consequence, the measurements transmitted to the supervisory control network will not be corrupted;
- runtime reconfigurations of secure proxies are not allowed.

Thus, in general, the attacker objectives can be resumed in alteration/forgery of PLC actuator commands and/or communication messages between PLCs to eventually affect the evolution of the controlled physical processes, and/or transmit fake signals to the supervisory control network.

3 A FORMAL LANGUAGE FOR MONITORED CONTROLLERS

In this section, we introduce the Timed Calculus of Monitored Controllers, called TMC, as an abstract formal language to express networks of controllers integrated with edit automata sitting on the network interface of each controller to monitor/correct their interactions with the rest of the system. Basically, TMC extends Hennessy and Regan’s Timed Process Language (TPL) [29] with monitoring edit automata. Like TPL time proceeds in discrete time slots separated by tick-actions.

Let us start with some preliminary notation. We use \(s, s_k \in \text{Sens}\) to name sensor signals; \(a, a_k \in \text{Act}\) to indicate actuator commands; \(c, c_k \in \text{Chn}\) for channels; \(z, z_k\) for generic names.
Controllers. In our setting, controllers are nondeterministic sequential timed processes evolving through three main phases: sensing of sensor signals, communication with other controllers, and actuation. For convenience, we use five different syntactic categories to distinguish the five main states of a controller: $\text{Ctrl}$ for initial states, $\text{Sleep}$ for sleeping states, $\text{Sens}$ for sensing states, $\text{Com}$ for communication states, and $\text{Act}$ for actuation states. In its initial state, a controller is a recursive process waiting for signal stabilisation in order to start the sensing phase:

$$\text{Ctrl} \ni P ::= X$$

$$\text{Sleep} \ni W ::= \text{tick}.W \mid S$$

The main process describing a controller consists of some recursive process defined via equations of the form $X = \text{tick}.W$, with $W \in \text{Sleep}$; here, $X$ is a process variable that may occur (free) in $W$. For convenience, our controllers always have at least one initial timed action tick to ensure time-guarded recursion, thus avoiding undesired zeno behaviours [30]: the number of untimed actions between two tick-actions is always finite. Then, after a determined sleeping period, when sensor signals get stable, the sensing phase can start.

During the sensing phase, the controller waits for a finite number of admissible sensor signals. If none of those signals arrives in the current time slot then the controller will timeout moving to the following time slot (we adopt the TPL construct $\lfloor \cdot \rfloor \cdot$ for timeout). The syntax is the following:

$$\text{Sens} \ni S ::= \lfloor \sum_{i \in I} s_i.S_i \rfloor \mid C$$

where $\sum_{i \in I} s_i.S_i$ denotes the standard construct for nondeterministic choice. Once the sensing phase is concluded, the controller starts its calculations that may depend on communications with other controllers governing different physical processes. Controllers communicate with each other for mainly two reasons: either to receive notice about the state of other physical sub-processes or to require an actuation on a physical process which is out of their control. As in TPL, we adopt a channel-based handshake point-to-point communication paradigm. Note that, in order to avoid starvation, communication is always under timeout. The syntax for the communication phase is:

$$\text{Com} \ni C ::= [\sum_{i \in I} c_i.C_i] \mid [\vec{c}.C] \mid A$$

In the actuation phase a controller eventually transmits a finite sequence of commands to actuators, and then, it emits a fictitious system signal end to denote the end of the scan cycle. After that, the whole scan cycle can restart. Formally,

$$\text{Act} \ni A ::= \bar{a}.A \mid \text{end}.X$$

Remark 1 (Scan cycle duration and maximum cycle limit). The scan cycle of a PLC must be completed within a specific time, called maximum cycle limit, which depends on the controlled physical process; if this time limit is violated the controller stops and throws an exception [59]. Thus, the signal end must occur well before the maximum cycle limit of the controller. We actually work under the assumption that our controllers successfully complete their scan cycle in less than half of the maximum cycle limit. The reasons for this assumption will be clarified in Remark 4. Please, notice that it is easy to statically derive the maximum duration of a scan cycle expressed in our calculus by simply counting the maximum number of tick-prefixes occurring between two subsequent end-prefixes.

The operational semantics in Table 1 is along the lines of Hennessy and Regan’s TPL [29]. In the following, we use the metavariable $\alpha$ to range over the set of all (observable) controller actions: $\{s, \bar{a}, \bar{c}, c, \text{tick}, \text{end}\}$. These actions denote: sensor readings, actuator commands, channel transmissions, channel receptions, passage of time, and end of scan cycles, respectively. Notice that at our level of abstraction we represent only the observable behaviour of PLCs: internal computations are not modelled within PLCs; although, we do have $\tau$-actions to express communications between two PLCs, as the reader will notice in Table 2.
Remark 2 (Attacker model and end-signal). In our abstract representation of PLCs, the end-signal is not really part of the (possibly compromised) PLC program but it is rather a system signal denoting the end of a scan cycle. As a consequence, in accordance with our attacker model, we assume that this fictitious signal cannot be dropped or forged by the attacker.

Monitored controllers. The core of our enforcement relies on (timed) finite-state Ligatti et al.’s edit automata [40], i.e., a particular class of automata specifically designed to allow/suppress/insert actions in a generic system in order to preserve its correct behaviour. The syntax is as follows:

\[ \mathbb{E} \text{edit} \ni E, F ::= \text{go} \mid \sum_{i \in I} \lambda_i, E_i \mid X \]

The special automaton \( \text{go} \) will admit any action of the monitored system. The edit automaton \( \sum_{i \in I} \lambda_i, E_i \) enforces an action \( \lambda_i \), and then continues as \( E_i \), for any \( i \in I \), with \( I \) finite. Here, the symbol \( \lambda \) ranges over: (i) \( \alpha \) to allow the action \( \alpha \), (ii) \( \neg \alpha \) to suppress the action \( \alpha \), and (iii) \( \alpha_1 \prec \alpha_2 \), for \( \alpha_1 \neq \alpha_2 \), to insert the action \( \alpha_1 \) before the action \( \alpha_2 \). Recursive automata \( X \) are defined via equations of the form \( X = E \), where the automata variable \( X \) may occur (free) in \( E \).

The operational semantics of our edit automata is given via the following transition rules:

\[
\begin{align*}
\text{(Go)} & \quad \frac{}{\text{go} \overset{\alpha}{\longrightarrow} \text{go}} \\
\text{(Edit)} & \quad \frac{j \in I}{\sum_{i \in I} \lambda_i, E_i \overset{\lambda_j}{\longrightarrow} E_j} \\
\text{(RecE)} & \quad \frac{X = E \quad E \overset{\lambda}{\longrightarrow} E'}{X \overset{\lambda}{\longrightarrow} E'}
\end{align*}
\]

Our monitored controllers, written \( E \ni \{J\} \), consist of a controller \( J \), for \( J \in \text{Ctrl} \cup \text{S1eP} \cup \text{S1etS} \cup \text{C0min} \cup \text{Act} \), and an edit automaton \( E \) enforcing the behaviour of \( J \), according to the following transition rules, presented in the style of [42]:

\[
\begin{align*}
\text{(Allow)} & \quad E \overset{\alpha}{\longrightarrow} E' \quad J \overset{\alpha}{\longrightarrow} J' \\
\text{(Suppress)} & \quad E \overset{\alpha}{\longrightarrow} E' \quad J \overset{\alpha}{\longrightarrow} J' \\
\text{(Insert)} & \quad E \overset{\alpha_1 \prec \alpha_2}{\longrightarrow} E' \quad J \overset{\alpha_2}{\longrightarrow} J'
\end{align*}
\]

Rule (Allow) is used for allowing observable actions emitted by the controller under scrutiny. By an application of Rule (Suppress), incorrect actions \( \alpha \) emitted by (possibly corrupted) controllers \( J \) are suppressed, i.e., converted into (silent) \( \tau \)-actions. Rule (Insert) is used to insert an action \( \alpha_1 \) before an action \( \alpha_2 \) of the controller. In the following, the metavariable \( \beta \) will range over the same set of actions as \( \alpha \), together with the silent action \( \tau \).
Here, we wish to stress that, like Ligatti et al. [40], we are interested in deterministic (and hence implementable) enforcement. With the following technical definitions we extract from enforcer actions $\lambda$ both: (i) the controller triggering actions, and (ii) the resulting output actions.

**Definition 1.** Let $\lambda \in \{\alpha, \bar{\alpha}, \alpha_1 < \alpha_2\}$ be an arbitrary action for edit automata, we write $\text{trigger}(\lambda)$ to denote the controller action triggering $\lambda$, defined as: $\text{trigger}(\alpha) = \alpha$, $\text{trigger}(\bar{\alpha}) = \bar{\alpha}$ and $\text{trigger}(\alpha_1 < \alpha_2) = \alpha_2$. Similarly, we write $\text{out}(\lambda)$ to denote the output action prescribed by $\lambda$, defined as: $\text{out}(\alpha) = \alpha$, $\text{out}(\bar{\alpha}) = \tau$ and $\text{out}(\alpha_1 < \alpha_2) = \alpha_1$. Given a trace $t = \lambda_1 \cdots \lambda_n$, we write $\text{out}(t)$ for the trace $\text{out}(\lambda_1) \cdots \text{out}(\lambda_n)$.

Now, we provide a definition of deterministic enforcer along the lines of Pinisetty at al. [50].

**Definition 2 (Deterministic Enforcer).** A edit automaton $E \in \mathbb{Ed}it$ is said to be deterministic iff in every term $\sum_{i \in I} \lambda_i, E_i$ that appears in $E$ there are no $\lambda_k$ and $\lambda_j$, for $k, j \in I, k \neq j$, such that $\text{trigger}(\lambda_k) = \text{trigger}(\lambda_j)$ and $\text{out}(\lambda_k) = \text{out}(\lambda_j)$.

Finally, we can easily generalise the concept of monitored controller to a field communications network of parallel monitored controllers, each one acting on different actuators, and exchanging information via channels. These networks are formally defined via a straightforward grammar:

$$\mathbb{FNet} \ni N := E \rightarrow \{f\} \mid N \parallel N$$

with the operational semantics defined in Table 2.

Notice that monitored controllers may interact with each other via channel synchronisation (see Rule (ChnSync)). Moreover, via rule (TimeSync) they may evolve in time only when channel synchronisation may not occur (our controllers do not admit zeno behaviours). This ensures maximal progress [29], a desirable time property when modelling real-time systems: channel communications will never be postponed.

**Definition 3 (Execution Traces).** Given three finite execution traces $t_c = \alpha_1 \cdots \alpha_k$, $t_e = \lambda_1 \cdots \lambda_l$, and $t_m = \beta_1 \cdots \beta_n$, for controllers, edit automata and monitored controllers, respectively. We write: (i) $P \xrightarrow{t_c} P'$, as an abbreviation for $P = P_0 \xrightarrow{\alpha_1} \cdots \xrightarrow{\alpha_k} P_k = P'$; (ii) $E \xrightarrow{t_e} E'$, as an abbreviation for $E = E_0 \xrightarrow{\lambda_1} \cdots \xrightarrow{\lambda_l} E_l = E'$; (iii) $N \xrightarrow{t_m} N'$, as an abbreviation for $N = N_0 \xrightarrow{\beta_1} \cdots \xrightarrow{\beta_n} N_n = N'$.

In the rest of the paper we adopt the following notations.

**Notation 1.** As usual, we write $e$ to denote the empty trace. Given a trace $t$ we write $|t|$ to denote the length of $t$, i.e., the number of actions occurring in $t$. Given a trace $t$ we write $\hat{t}$ to denote the trace obtained by removing the $\tau$-actions. Given two traces $t'$ and $t''$, we write $t' \cdot t''$ for the trace resulting from the concatenation of $t'$ and $t''$. For $t = t' \cdot t''$ we say that $t'$ is a prefix of $t$ and $t''$ is a suffix of $t$. 

| ParL | N_1 \xrightarrow{\alpha} N'_1 | (ChnSync) | N_1 \xrightarrow{c} N'_1 \parallel N_2 \xrightarrow{\tau} N''_1 |
|-----|-------------------------------|-----------|---------------------------------|
| ParR | N_2 \xrightarrow{\alpha} N'_2 | (TimeSync) | N_1 \xrightarrow{\text{tick}} N'_1 \parallel N_2 \xrightarrow{\text{tick}} N''_1 |

Table 2. LTS for field communications networks of monitored controllers.
4 USE CASE: THE SWAT SYSTEM

In this section, we describe how to specify in TMC a non-trivial network of PLCs to control (a simplified version of) the Secure Water Treatment system (SWaT) [43].

SWaT represents a scaled down version of a real-world industrial water treatment plant. The system consists of 6 stages, each of which deals with a different treatment, including: chemical dosing, filtration, dechlorination, and reverse osmosis. For simplicity, in our use case, depicted in Figure 3, we consider only three stages. In the first stage, raw water is chemically dosed and pumped in a tank $T_1$, via two pumps $pump_1$ and $pump_2$. A valve connects $T_1$ with a filtration unit that releases the treated water in a second tank $T_2$. Here, we assume that the flow of the incoming water in $T_1$ is greater than the outgoing flow passing through the valve. The water in $T_2$ flows into a reverse osmosis unit to reduce inorganic impurities. In the last stage, the water coming from the reverse osmosis unit is either distributed as clean water, if required standards are met, or stored in a backwash tank $T_3$ and then pumped back, via a pump $pump_3$, to the filtration unit. Here, we assume that tank $T_2$ is large enough to receive the whole content of tank $T_3$ at any moment.

The SWaT system has been used to provide a dataset containing physical and network data recorded during 11 days of activity [27]. Part of this dataset contains information about the execution of the system in isolation, while a second part records the effects on the system when exposed to different kinds of cyber-physical attacks. Thus, for instance, (i) drops of commands to activate $pump_2$ may affect the quality of the water, as they would affect the correct functioning of the chemical dosing pump; (ii) injections of commands to close the valve between $T_1$ and $T_2$, may give rise to an overflow of tank $T_1$ if this tank is full; (iii) integrity attacks on the signals coming from the sensor of the tank $T_3$ may result in damages of the pump $pump_3$ if it is activated when $T_3$ is empty.

Each tank is controlled by its own PLC. The programs of the three PLCs, expressed in terms of ladder logic, are given in Figure 4. In the following, we give their descriptions in TMC.

Let us start with the code of the controller PLC$_1$ managing the tank $T_1$. Its definition is given in terms of two equations to deal with the case when the two pumps, $pump_1$ and $pump_2$, are both off and both on, respectively. Intuitively, when the pumps are off, the level of water in $T_1$ drops until it reaches its low level (event $l_1$); when this happens both pumps are turned on and they remain so...
Thus, for instance, when the pumps are off the valve is closed (command \( \text{off} \)). Otherwise, if the level of the tank is high (signal \( h \)) then the pumps are turned on (commands \( \text{on} \) and \( \text{on} \)) and the valve is closed (command \( \text{off} \)). If the level is low (signal \( l \)) then the pumps are turned off (commands \( \text{off} \) and \( \text{off} \)) and the valve is open (command \( \text{on} \)). Finally, if the tank is at some intermediate level between low and high (signal \( m \)) then PLC1 listens for requests arriving from PLC2 to open/close the valve. Precisely, if the PLC gets an open_req request then it opens the valve, letting the water flow from \( T_1 \) to \( T_2 \), otherwise, if it gets a close_req request then it closes the valve; in both cases the pumps remain off. If the level of the tank is high (signal \( h \)) then the requests of water coming from PLC2 are served as before, but the two pumps are eventually turned off (commands \( \text{off} \) and \( \text{off} \)).

PLC2 manages the water level of tank \( T_2 \). Its code consists of the two equations to model the filling (state \( \uparrow \)) and the emptying (state \( \downarrow \)) of the tank. Formally,

\[
P_{\uparrow}^2 = \text{tick} ( \{ l_2, [\text{open} \_ \text{req}, \text{end} \_ \text{P}_2] \} \text{end} \_ \text{P}_2 + m_2, [\text{open} \_ \text{req}, \text{end} \_ \text{P}_2] \} \text{end} \_ \text{P}_2 + h_2, [\text{close} \_ \text{req}, \text{end} \_ \text{P}_2] \} \text{end} \_ \text{P}_2 + h_2, [\text{close} \_ \text{req}, \text{end} \_ \text{P}_2] \} \text{end} \_ \text{P}_2)
\]
\[
P_{\downarrow}^2 = \text{tick} ( \{ l_2, [\text{open} \_ \text{req}, \text{end} \_ \text{P}_2] \} \text{end} \_ \text{P}_2 + m_2, [\text{open} \_ \text{req}, \text{end} \_ \text{P}_2] \} \text{end} \_ \text{P}_2 + h_2, [\text{close} \_ \text{req}, \text{end} \_ \text{P}_2] \} \text{end} \_ \text{P}_2 + h_2, [\text{close} \_ \text{req}, \text{end} \_ \text{P}_2] \} \text{end} \_ \text{P}_2)
\]

Here, after one time slot, the level of \( T_2 \) is checked. If the level is low (signal \( l_2 \)) then PLC2 sends a request to PLC1, via the channel \( \text{open} \_ \text{req} \), to open the valve that lets the water flow from \( T_1 \) to \( T_2 \), and then returns. Otherwise, if the level of tank \( T_2 \) is high (signal \( h_2 \)) then PLC2 asks PLC1 to close the valve, via the channel \( \text{close} \_ \text{req} \), and then returns. Finally, if the tank \( T_2 \) is at some intermediate level between \( l_2 \) and \( h_2 \) (signal \( m_2 \)) then the valve remains open (respectively, closed) when the tank is refilling (respectively, emptying).

Finally, PLC3 manages the water level of the backwash tank \( T_3 \). Its code consists of two equations to deal with the case when the pump \( \text{pump}_3 \) is off and on, respectively. Formally,

\[
P_{\text{off}}^3 = \text{tick} ( \{ l_3, \text{off} \_ \text{end} \_ \text{P}_3 \} \text{end} \_ \text{P}_3 + m_3, \text{off} \_ \text{end} \_ \text{P}_3 \} \text{end} \_ \text{P}_3 + h_3, \text{off} \_ \text{end} \_ \text{P}_3 \} \text{end} \_ \text{P}_3 + h_3, \text{off} \_ \text{end} \_ \text{P}_3 \} \text{end} \_ \text{P}_3)
\]
\[
P_{\text{on}}^3 = \text{tick} ( \{ l_3, \text{off} \_ \text{end} \_ \text{P}_3 \} \text{end} \_ \text{P}_3 + m_3, \text{off} \_ \text{end} \_ \text{P}_3 \} \text{end} \_ \text{P}_3 + h_3, \text{off} \_ \text{end} \_ \text{P}_3 \} \text{end} \_ \text{P}_3 + h_3, \text{off} \_ \text{end} \_ \text{P}_3 \} \text{end} \_ \text{P}_3)
\]
Here, after one time slot, the level of tank $T_3$ is checked. If the level is low (signal $l_3$) then PLC$_3$ turns off the pump $pump_3$ (command off$3$), and then returns. Otherwise, if the level of $T_3$ is high (signal $h_3$) then the pump is turned on (command on$3$) until the whole content of $T_3$ is pumped back into the filtration unit of $T_2$.

**Examples of correctness properties and attacks.** In a system similar to that described above, one would expect a number of properties capturing the correct functioning of system components. Let us provide a few examples of such correctness properties and some specific attacks that may potentially invalidate these properties.

A first property might say that if PLC$_1$ receives a request to open the valve between tanks $T_1$ and $T_2$ then the same valve will be eventually closed early enough to prevent water overflow in tank $T_2$. This property certainly holds when the system is not exposed to any attack. However, a malware injected in PLC$_1$ might try to undermine this property by tampering either with the actuator dedicated to the valve or with the requests of PLC$_2$ to open/close the valve. In particular, a malicious request to open the valve might be forged by an attacker injected in PLC$_2$. Thus, another desired correctness property might say that whenever the tank $T_2$ is full then PLC$_2$ will never ask for incoming water from tank $T_1$. Finally, another expected property might say that $pump_3$ will never work without enough water in tank $T_3$. Again, an attacker injected in PLC$_3$ might try to undermine this property by tampering either with the actuator dedicated to the pump or with the sensor measuring the level of tank $T_3$.

In Section 7.3 we will provide formal definitions for patterns template of structured correctness properties that are suitable for enforcing correct behaviours of our PLCs.

### 5 A FORMAL LANGUAGE FOR CONTROLLER PROPERTIES

In this section, we provide a simple description language to express correctness properties that we may wish to enforce at runtime in our controllers. As discussed in the Introduction, we resort to (a sub-class of) regular properties as they allow us to express interesting classes of properties referring to one or more scan cycles of a controller. The proposed language distinguishes between two kinds of properties: (i) **global properties**, $e \in \mathbb{P}_{\text{g}}$, to express general controllers’ execution traces; (ii) **local properties**, $p \in \mathbb{P}_{\text{l}}$, to express traces confined to a finite number of consecutive scan cycles. The two families of properties are formalised via the following regular grammar:

\[
  e \in \mathbb{P}_{\text{g}} ::= p^* \mid e_1 \cap e_2 \\
  p, q \in \mathbb{P}_{\text{l}} ::= e \mid p_1; p_2 \mid \bigcup_{i \in I} \pi_i . p_i \mid p_1 \cap p_2
\]

where $\pi_i \in \text{Events} \triangleq \text{Sens} \cup \text{Act} \cup \text{Chn}^* \cup \{\text{tick}\} \cup \{\text{end}\}$ denote atomic properties, called events, that may occur as prefix of a property. With an abuse of notation, we use the symbol $\epsilon$ to denote both the empty property and the empty trace.

The semantics of our logic is naturally defined in terms of sets of execution traces which satisfy a given property; its formal definition is given in Table 3. However, the syntax of our logic is a bit too permissive with respect to our intentions, as it allows us to describe partial scan cycles, i.e., cycles that have not completed. Thus, we restrict ourselves to considering properties which builds on top of local properties associated to complete scan cycles, i.e., scan cycles whose last action is an \textit{end}-action. Formally,

**Definition 4.** Well-formed properties are defined as follows:

- the local property $\text{end} . e$ is well formed;
- a local property of the form $p_1; p_2$ is well formed if $p_2$ is well formed;
- a local property of the form $p_1 \cap p_2$ is well formed if both $p_1$ and $p_2$ are well formed;
We write $$[p^*]$$ as follows:

$$[p^*] = \{e\} \cup \bigcup_{n \in \mathbb{N}^+} \{(t \mid t = t_1 \cdot \ldots \cdot t_n, \text{ with } t_i \in [p], \text{ for } 1 \leq i \leq n\}$$

$$[e_1 \cap e_2] = \{t \mid t \in [e_1] \text{ and } t \in [e_2]\}$$

$$[e] = \{e\}$$

$$[p_1 \cap p_2] = \{t \mid t \in [p_1] \text{ and } t \in [p_2]\}$$

$$[p_1; p_2] = \{t \mid t = t_1 \cdot t_2, \text{ with } t_1 \in [p_1] \text{ and } t_2 \in [p_2]\}$$

$$[\bigcup_{i \in I} \pi_i; p_i] = \bigcup_{i \in I} \{t \mid t = \pi_i \cdot t', \text{ with } t' \in [p_i]\}$$

Table 3. Trace semantics of our regular properties.

- a local property of the form $$\bigcup_{i \in I} \pi_i; p_i$$ is well-formed if either $$\pi_i; p_i = \text{end} \cdot e$$ or $$p_i$$ is well-formed, for any $$i \in I$$;
- a global property $$p^*$$ is well-formed if $$p$$ is well-formed;
- a global property $$e_1 \cap e_2$$ is well-formed if both $$e_1$$ and $$e_2$$ are well-formed.

In the rest of the paper, we always assume to work with well-formed properties. Moreover, we adopt the following notations and/or abbreviations on properties.

**Notation 2.** We omit trailing empty properties, writing $$\pi$$ instead of $$\pi \cdot e$$. For $$k > 0$$, we write $$\pi^k \cdot p$$ as a shorthand for $$\pi \cdot \ldots \cdot \pi \cdot p$$, where prefix $$\pi$$ appears $$k$$ consecutive times. Given a local property $$p$$ we write $$\text{events}(p) \subseteq \text{Events}$$ to denote the set of events occurring in $$p$$; similarly, we write $$\text{events}(e) \subseteq \text{Events}$$ to denote the set of events occurring in a global property $$e \in \mathcal{P}_{\text{top}}D$$.

Given a set of events $$\mathcal{A} \subseteq \text{Events}$$ and a local property $$p$$, we use $$\mathcal{A}$$ itself as an abbreviation for the property $$\bigcup_{\pi \in \mathcal{A}} \pi \cdot e$$, and $$\mathcal{A} \cdot p$$ as an abbreviation for the property $$\bigcup_{\pi \in \mathcal{A}} \pi \cdot p$$. Given a set of events $$\mathcal{A}$$, with $$\text{end} \notin \mathcal{A}$$, we write $$\mathcal{A}^{\leq k}$$, for $$k \geq 0$$, to denote the well-formed property defined as follows: (i) $$\mathcal{A}^{\leq 0} \triangleq \text{end}$$; (ii) $$\mathcal{A}^{\leq k} \triangleq \text{end} \cup \mathcal{A} \cdot \mathcal{A}^{\leq k-1}$$, for $$k > 0$$. Thus, the property $$\mathcal{A}^{\leq k}$$ captures all possible sequences of events of $$\mathcal{A}$$ whose length is at most $$k$$, for $$k \in \mathbb{N}$$. We write $$\text{PEvents}$$ to denote the set of pure events, i.e., $$\text{Events} \setminus \{\text{end}\}$$. Finally, we write $$\text{PUEvents}$$ to denote the set of pure untimed events, i.e., $$\text{Events} \setminus \{\text{end}, \text{tick}\}$$.

Note that our properties are in general nondeterministic. However, since we are interested in deterministic enforcers, in the following we will focus on deterministic enforcing properties.

**Definition 5 (Deterministic properties).** A global property $$e \in \mathcal{P}_{\text{top}}D$$ is said to be deterministic if for any sub-term $$\bigcup_{i \in I} \pi_i; p_i$$ appearing in $$e$$, we have $$\pi_k \neq \pi_h$$, for any $$k, h \in I, k \neq h$$.

### 5.1 Local properties

As already said, local properties describe execution traces which are limited to a finite number of scan cycles. Let us present a number of significant local properties that can be expressed in our language of regular properties. In the following, we assume a fixed maximum number of actions, $$\text{maxa}$$, that may occur within a single scan cycle of our controllers, i.e., between two subsequent $$\text{end}$$-actions.

#### 5.1.1 Basic properties. They prescribe conditional, eventual and persistent behaviours.

**Conditional.** These properties say that when a (pure) untimed event $$\pi$$ occurs in the current scan cycle then some property $$p$$ should be satisfied. More generally, for $$\pi_i \in \text{PUEvents}$$ and $$p_i \in \mathcal{P}_{\text{top}}L$$, we write $$\text{Case}(\bigcup_{i \in I} (\pi_i, p_i))$$ to denote the property $$q_k$$, for $$k = \text{maxa}$$, defined as follows:

- $$q_k \triangleq \text{end} \cup \bigcup_{i \in I} \pi_i; p_i \cup (\text{PEvents} \setminus \bigcup_{i \in I} \{\pi_i\}).q_{k-1},$$ for $$0 < k \leq \text{maxa}$$
- $$q_0 \triangleq \text{end}.$$

When there is only one triggering event $$\pi \in \text{PUEvents}$$ and one associated local property $$p \in \mathcal{P}_{\text{top}}L$$, we have a simple conditional property defined as follow: $$\text{Cnd}(\pi, p) \triangleq \text{Case}(\{(\pi, p)\}).$$
Formally, for the second event \( \pi \) bounded persistency prescribes that an event \( \pi \) continues for at most \( m \) consecutive scan cycles. Of course, the triggered local property \( p \) may span over a finite number of scan cycles (see Figure 5). Formally, we write \( \text{PCnd}_m(\pi, p) \), for \( \pi \in \text{PUEvents} \) and \( m > 0 \), for the property \( q^m_{\text{maxa}} \) defined as follows:

\[
\begin{align*}
q^h_0 & \triangleq \text{end}.d^{-1}_{\text{maxa}} \cup \pi.p \cup (\text{PEvents}\{\pi}\}) . q^h_{k-1}, \text{ for } 1 < h \leq m \text{ and } 0 < k \leq \text{maxa} \\
q^h_0 & \triangleq \text{end}.d^{-1}_{\text{maxa}}, \text{ for } 1 < h \leq m \\
q^1_k & \triangleq \text{end} \cup \pi.p \cup (\text{PEvents}\{\pi}\}) . q^1_{k-1}, \text{ for } 0 < k \leq \text{maxa} \\
q^0_0 & \triangleq \varepsilon.
\end{align*}
\]

Obviously, \( \text{Cnd}(\pi, p) = \text{PCnd}_1(\pi, p) \).

**Bounded eventually.** In this case, an event \( \pi \) must eventually occur within \( m \) scan cycles. Formally, for \( \pi \in \text{PUEvents} \) and \( m > 0 \), we write \( \text{BE}_m(\pi) \) to denote the property \( q^m_{\text{maxa}} \) defined as follows:

\[
\begin{align*}
q^h_0 & \triangleq \text{end}.d^{-1}_{\text{maxa}} \cup \pi.p \cup (\text{PEvents}\{\pi}\}) . q^h_{k-1}, \text{ for } 1 < h \leq m \text{ and } 0 < k \leq \text{maxa} \\
q^h_0 & \triangleq \text{end}.d^{-1}_{\text{maxa}}, \text{ for } 1 < h \leq m \\
q^1_k & \triangleq \pi.p \cup (\text{PEvents}\{\pi}\}) . q^1_{k-1}, \text{ for } 0 < k \leq \text{maxa} \\
q^0_0 & \triangleq \pi.\text{end}.
\end{align*}
\]

**Bounded persistency.** While in \( \text{BE}_m(\pi) \) the event \( \pi \) must eventually occur within \( m \) scan cycles, bounded persistency prescribes that an event \( \pi \) must occur in all subsequent \( m \) scan cycles. Formally, for \( \pi \in \text{PUEvents} \) and \( m > 0 \), we write \( \text{BP}_m(\pi) \) to denote the property \( q^m_{\text{maxa}} \) defined as follows:

\[
\begin{align*}
q^h_0 & \triangleq \pi.p \cup (\text{PEvents}\{\pi}\}) . d^{-1}_{\text{maxa}} \cup (\text{PEvents}\{\pi}\}) . q^h_{k-1}, \text{ for } 1 < h \leq m \text{ and } 0 < k \leq \text{maxa} \\
q^h_0 & \triangleq \text{end}.d^{-1}_{\text{maxa}}, \text{ for } 1 < h \leq m \\
q^1_k & \triangleq \pi.p \cup (\text{PEvents}\{\pi}\}) . q^1_{k-1}, \text{ for } 0 < k \leq \text{maxa} \\
q^0_0 & \triangleq \pi.\text{end}.
\end{align*}
\]

**Bounded absence.** The negative counterpart of bounded persistency is bounded absence. This property says that an event \( \pi \) must not appear in all subsequent \( m \) scan cycles. Formally, for \( \pi \in \text{PUEvents} \) and \( m > 0 \), we write \( \text{BA}_m(\pi) \) to denote the property \( q^m_{\text{maxa}} \) defined as follows:

\[
\begin{align*}
q^h_0 & \triangleq (\text{PEvents}\{\pi}\}) \cup \pi.p \cup (\text{PEvents}\{\pi}\}) . q^h_{k-1}, \text{ for } 0 < h \leq m \\
q^0_0 & \triangleq \varepsilon.
\end{align*}
\]

5.1.2 **Compound conditional properties.** The properties above can be combined together to express more detailed PLC behaviours. Let us see a few examples with the help of the use case of Section 4.

**Conditional bounded eventually.** According to this property, if a triggering event \( \pi_1 \) occurs then a second event \( \pi_2 \) must eventually occur between the \( m \)-th and the \( n \)-th scan cycle, with \( 1 \leq m \leq n \). Formally, for \( \pi_1, \pi_2 \in \text{PUEvents} \) and \( 1 \leq m \leq n \), we define \( \text{CBE}_{[m,n]}(\pi_1, \pi_2) \) as follows:

\[
\text{CBE}_{[m,n]}(\pi_1, \pi_2) \triangleq \text{Cnd}(\pi_1, (\text{PEvents}^{\leq \text{maxa}})^{m-1}; \text{BE}_{n-m+1}(\pi_2)).
\]
Intuitively, if the event $\pi_1$ occurs then the event $\pi_2$ must eventually occur between the scan cycles $m$ and $n$. In case we would wish that $\pi_2$ should not occur before the $m$-th scan cycle, then the property would become: $\text{Cnd}(\pi_1, \text{BA}_{m-1}(\pi_2), \text{BE}_{n-m+1}(\pi_2))$.

As an example, we might enforce a conditional bounded eventually property in PLC$_1$ of our use case in Section 4 to prevent water overflow in the tank $T_2$ due to a misuse of the valve connecting the tanks $T_1$ and $T_2$. Assume that $z \in \mathbb{N}$ is the time (expressed in scan cycles) required to overflow the tank $T_2$ when the valve is open and the level of tank $T_2$ is low. We might consider to enforce a property of the form $\text{CBE}_{[1,w]}(\text{open}_{\text{req}}, \text{close})$, with $w < z$, saying that if PLC$_1$ receives a request to open the valve, then the valve will be eventually closed within at most $w$ scan cycles (including the current one). This will ensure that if a water request coming from PLC$_2$ is received by PLC$_1$ then the valve controlling the flaw from $T_1$ to $T_2$ will remain open for at most $w$ scan cycles, with $w < z$, preventing the overflow of $T_2$.

Conditional bounded persistency. Another possibility is to combine conditional with bounded persistency to prescribe that if a triggering event $\pi_1$ occurs then the event $\pi_2$ must occur in the $m$-th scan cycle and in all subsequent $n - m$ scan cycles, for $1 \leq m \leq n$. Formally, for $\pi_1, \pi_2 \in \text{PUEvents}$ and $1 \leq m \leq n$, we write $\text{CBP}_{[m,n]}(\pi_1, \pi_2)$ to denote the property defined as:

$$\text{CBP}_{[m,n]}(\pi_1, \pi_2) \triangleq \text{Cnd}(\pi_1, (\text{PEvents}^{\leq \text{maxa}})^{m-1}, \text{BA}_{n-m+1}(\pi_2)).$$

As an example, we might enforce a conditional bounded persistency property in PLC$_3$ of our use case in Section 4 to prevent damages of pump$_3$ due to lack of water in tank $T_3$. Assume that $z \in \mathbb{N}$ is the minimum time (in terms of scan cycles) required to fill $T_3$, i.e., to pass from level $l_3$ to level $h_3$, when pump$_3$ is off. We might consider to enforce a property of the form $\text{CBP}_{[1,z]}(l_3, \text{off}_{\text{p3}})$, to prescribe that if the tank reaches its low level (event $l_3$) then pump$_3$ must remain off (event $\text{off}_{\text{p3}}$) for $z$ consecutive scan cycles. This will ensure enough water in tank $T_3$ to prevent damages on pump$_3$.

Notice that all previous properties have a single triggering event $\pi_1$; in order to deal with multiple triggering events it is enough to replace the conditional operator with the case construct.

Conditional bounded absence (also called Absence timed [24]). Finally, we might consider to combine conditional with bounded absence to formalise a property saying that if a triggering event $\pi_1$ occurs then another event $\pi_2$ must not occur in the $m$-th scan cycle and in all subsequent $n - m$ scan cycles, with $1 \leq m \leq n$. Formally, for $\pi_1, \pi_2 \in \text{PUEvents}$ and $1 \leq m \leq n$, we write $\text{CBA}_{[m,n]}(\pi_1, \pi_2)$ to denote the property defined as follows:

$$\text{CBA}_{[m,n]}(\pi_1, \pi_2) \triangleq \text{Cnd}(\pi_1, (\text{PEvents}^{\leq \text{maxa}})^{m-1}, \text{BA}_{n-m+1}(\pi_2)).$$

Intuitively, if the triggering event $\pi_1$ occurs then the event $\pi_2$ must not occur in the time interval between the $m$-th and the $n$-th scan cycle.

As an example, we might enforce a conditional bounded absence property in PLC$_2$ of our use case in Section 4 to prevent water overflow in the tank $T_2$ due to a misuse of the valve connecting the tanks $T_1$ and $T_2$. Assume that $z \in \mathbb{N}$ is the time (expressed in scan cycles) required to empty the tank $T_2$ when the valve is closed and the tank $T_2$ reaches its high level $h_2$. Then, we might consider to enforce a property of the form $\text{CBA}_{[1,w]}(h_2, \text{open}_{\text{req}})$, for $w < z$, to prescribe that if the tank reaches its high level (event $h_2$) then PLC$_2$ may not send a requests to open the valve (event $\text{open}_{\text{req}}$) for the subsequent $w$ scan cycles. This ensures us that when $T_2$ reaches its high level then it will not ask for incoming water for at least $w$ scan cycles, so preventing tank overflow.

5.1.3 Compound persistent conditional properties. Now, we formalise in our language of regular properties a number of correctness properties used by Frehse et al. for the verification of hybrid systems [24]. More precisely, we formalise bounded versions of their properties.
Bounded minimum duration. When a triggering event $\pi_1$ occurs, if a second event $\pi_2$ occurs within $m$ scan cycles then this event must appear in at least all subsequent $n$ scan cycles (see Figure 6). Formally, we can express this property as follows:

$$\text{MinD}(\pi_1, \pi_2, m, n) \triangleq \text{Cnd}(\pi_1, \text{PCnd}_m(\pi_2, \text{BP}_n(\pi_2))).$$

Note that the property $\text{MinD}(\pi_1, \pi_2, m, n)$ is satisfied each time $\text{CBP}_{[m,m+n]}(\pi_1, \pi_2)$ is. The vice versa does not hold as in $\text{CBP}_{[m,m+n]}(\pi_1, \pi_2)$ the event $\pi_2$ is required to occur in the whole time interval $[m, m+n]$, while, according to $\text{MinD}(\pi_1, \pi_2, m, n)$, the event $\pi_2$ might not occur at all.

Bounded maximum duration. When an event $\pi_1$ occurs, if a second event $\pi_2$ occurs within $m$ scan cycles then the same event $\pi_2$ may occur in at most all subsequent $n$ scan cycles. Formally, we can represent this property as follows:

$$\text{MaxD}(\pi_1, \pi_2, m, n) \triangleq \text{Cnd}(\pi_1, \text{PCnd}_m(\pi_2, (\text{PEvents}^\leq\text{maxa})^n; \text{BA}_1(\pi_2))).$$

The property $\text{MaxD}(\pi_1, \pi_2, m, n)$ is satisfied each time the property $\text{CBP}_{[m,m+n]}(\pi_1, \pi_2)$; $\text{BA}_1(\pi_2)$ is. Again, the vice versa does not hold.

Bounded response. When an event $\pi_1$ occurs, if a second event $\pi_2$ occurs within $m$ scan cycles then a third event $\pi_3$ appears within $n$ scan cycles. Formally, we can express this property as follows:

$$\text{BR}(\pi_1, \pi_2, \pi_3, m, n) \triangleq \text{Cnd}(\pi_1, \text{PCnd}_m(\pi_2, \text{BE}_n(\pi_3))).$$

Bounded invariance. Whenever an event $\pi_1$ occurs, if $\pi_2$ occurs within $m$ scan cycles then $\pi_3$ will persistently occur for at least $n$ scan cycles. Formally, we can express this property as follows:

$$\text{BI}(\pi_1, \pi_2, \pi_3, m, n) \triangleq \text{Cnd}(\pi_1, \text{PCnd}_m(\pi_2, \text{BP}_n(\pi_3))).$$

5.1.4 Bounded mutual exclusion. A different class of properties prescribes the possible occurrence of events $\pi_i \in \text{PEvents}$, for $i \in I$, in mutual exclusion within $m$ consecutive scan cycles. Formally, for $\pi_i \in \text{PUEvents}$, $i \in I$ and $m \geq 1$, we write $\text{BME}_m(\bigcup_{i \in I} \{\pi_i\})$, for the property $q_{\text{maxa}}^m$ defined as:

- $q_k^h \triangleq \text{end}.q_{\text{maxa}}^{h-1} \cup \bigcup_{i \in I} \pi_i.((\bigcap_{j \in I \setminus \{i\}} \text{BA}_h(\pi_j)) \cup (\text{PEvents} \setminus \bigcup_{i \in I} \{\pi_i\}).q_{k-1}^h$, for $1 < h \leq m$ and $0 < k \leq \text{maxa}$
- $q_0^0 \triangleq \text{end}.q_{\text{maxa}}^{-1}$, for $1 < h \leq m$
- $q_k^1 \triangleq \text{end} \cup \bigcup_{i \in I} \pi_i.((\bigcap_{j \in I \setminus \{i\}} \text{BA}_1(\pi_j)) \cup (\text{PEvents} \setminus \bigcup_{i \in I} \{\pi_i\}).q_{k-1}^1$, for $0 < k \leq \text{maxa}$
- $q_0^1 \triangleq \epsilon$.  

As an example, we might enforce a bounded mutual exclusion property in the PLC1 of our use case of Section 4 to prevent chattering of the valve, i.e., rapid opening and closing which may cause mechanical failures on the long run. In particular, we might consider to enforce a property of the form $\text{BME}_3(\text{state}(\text{open}, \text{close}))$ saying that within 3 consecutive scan cycles the opening and the closing of the valve (events $\text{open}$ and $\text{close}$, respectively) may only occur in mutual exclusion.

In Table 4, we summarise all local properties represented and discussed in this section.
As expected, the previously described local properties become global ones by applying the Kleene-operator $\ast$. Once in this form, we can put these properties in conjunction between them. Here, we show two global properties, the first one is built top of conditional bounded persistency properties and the second one is built on top of a conditional bounded eventually property.

As a second example, we might consider a more involved global property relying on conditional bounded eventually within our use case of Section 4. Assume $z \in \mathbb{N}$ being the time (expressed in scan cycles) required to overflow the tank $T_1$ when the level of the tank $T_1$ is low and both pumps are on and the valve is closed. Then, the property would be $(\text{CBP}_{\lceil \frac{w}{z} \rceil}(l_1, \overline{\alpha_{\overline{m}}}))^\ast \cap (\text{CBP}_{\lceil \frac{w}{z} \rceil}(l_1, \overline{\alpha_{\overline{n}}}))^\ast$, with $w < z$, saying that if the tank $T_1$ reaches its low level (event $l_1$) then both pump$_1$ and pump$_2$ must be on (events $\alpha_{\overline{m}}$ and $\alpha_{\overline{n}}$) in all subsequent $w$ scan cycles, starting from the current one.

As a second example, we might consider a more involved global property relying on conditional bounded eventually, persistent conditional, and bounded persistency. Basically, the property says that whenever an event $\pi_1$ occurs then a second event $\pi_2$ must eventually occur between the $m$-th scan cycle and the $n$-th scan cycle, with $1 \leq m \leq n$; moreover, it must occur for $d$ consecutive scan cycles, for $1 \leq d$ (see Figure 7).

**Table 4. Overview of local properties.**

| Case | Definition |
|------|------------|
| Persistent conditional: | for $m$ scan cycles, if $\pi$ occurs then $p$ should be satisfied |
| Bounded eventually: | event $\pi$ must eventually occur within $m$ scan cycles |
| Bounded persistency: | event $\pi$ must occur in all subsequent $m$ scan cycles |
| Bounded absence: | event $\pi$ must not occur in all subsequent $m$ scan cycles |
| Conditional bounded eventually: | if $\pi_1$ occurs then $\pi_2$ must eventually occur in the scan cycles $[m, n]$ |
| Conditional bounded persistency: | if $\pi_1$ occurs then $\pi_2$ must occur in all scan cycles of $[m, n]$ |
| Conditional bounded absence: | if $\pi_1$ occurs then $\pi_2$ must not occur in all scan cycles of $[m, n]$ |
| (Bounded) Minimum duration: | when $\pi_1$, if $\pi_2$ in $[1, m]$ then $\pi_2$ persists for at least $n$ scan cycles |
| (Bounded) Maximum duration: | when $\pi_1$, if $\pi_2$ in $[1, m]$ then $\pi_2$ persists for at most $n$ scan cycles |
| Bounded response: | when $\pi_1$, if $\pi_2$ in $[1, m]$ then $\pi_3$ appears within $n$ scan cycles |
| Bounded invariance: | when $\pi_1$, if $\pi_2$ in $[1, m]$ then $\pi_3$ persists for at least $n$ scan cycles |
| Bounded mutual exclusion | events $\pi_i$ may only occur in mutual exclusion within $n$ scan cycles |

**Fig. 7.** A trace satisfying the just mentioned property for some $m, n = m + 4$ and $d = 4$.

### 5.2 Global properties

As expected, the previously described local properties become global ones by applying the Kleene-operator $\ast$. Once in this form, we can put these properties in conjunction between them. Here, we show two global properties, the first one is built on top of conditional bounded persistency properties and the second one is built on top of a conditional bounded eventually property.

As a first example, we might consider a global property saying that whenever an event $\pi$ occurs then all events $\pi_i$, for $i \in I$, must occur in the $m$-th scan cycle and in all subsequent $n-m$ scan cycles, for $1 \leq m \leq n$. Formally, for $\pi, \pi_i \in \text{PUEvents}$, $i \in I$, and $1 \leq m \leq n$: $\bigcap_{i \in I} (\text{CBP}_{[m,n]}(\pi, \pi_i))^\ast$.

We might enforce this kind of property in PLC$_1$ of our use case of Section 4. Assume $z \in \mathbb{N}$ being the time (expressed in scan cycles) required to overflow the tank $T_1$ when the level of the tank $T_1$ is low and both pumps are on and the valve is closed. Then, the property would be $(\text{CBP}_{\lceil \frac{w}{z} \rceil}(l_1, \overline{\alpha_{\overline{m}}}))^\ast \cap (\text{CBP}_{\lceil \frac{w}{z} \rceil}(l_1, \overline{\alpha_{\overline{n}}}))^\ast$, with $w < z$, saying that if the tank $T_1$ reaches its low level (event $l_1$) then both pump$_1$ and pump$_2$ must be on (events $\overline{\alpha_{\overline{m}}}$ and $\overline{\alpha_{\overline{n}}}$) in all subsequent $w$ scan cycles, starting from the current one.

As a second example, we might consider a more involved global property relying on conditional bounded eventually, persistent conditional, and bounded persistency. Basically, the property says that whenever an event $\pi_1$ occurs then a second event $\pi_2$ must eventually occur between the $m$-th scan cycle and the $n$-th scan cycle, with $1 \leq m \leq n$; moreover, it must occur for $d$ consecutive scan cycles, for $1 \leq d$ (see Figure 7). Formally, the property is the following:

$$(\text{CBE}_{[m,n]}(\pi_1, \pi_2))^\ast \cap (\text{Cnd}(\pi_1, \text{PCnd}_{d}(\pi_2, \text{PEvents} \leq \text{max} \cdot \text{BP}_{d-1}(\pi_2))))^\ast$$

for $\pi_1, \pi_2 \in \text{PUEvents}$, with $1 \leq m \leq n$ and $d \geq 1$. Intuitively, the property $(\text{CBE}_{[m,n]}(\pi_1, \pi_2))^\ast$ requires that when $\pi_1$ occurs the event $\pi_2$ must eventually occur between the $m$-th scan cycle and the $n$-th scan cycle. The remaining part of the property says if the event $\pi_2$ occurs within the $n$-th scan cycle (recall that $m \leq n$) then it must persist for $d$ scan cycles.
In this manner, we might strengthen the conditional bounded eventually property given in Section 5.1 for PLC1 of our use case to prevent water overflow in the tank T2. Let \( z \in \mathbb{N} \) be the time (expressed in scan cycles) required to release in \( T_3 \) the (maximum) quantity of water that the tank \( T_2 \) may accumulate in \( w \) scan cycles. The first part of the property says that if PLC1 receives a request to open the valve (event \( \text{open}_{\text{req}} \)) then the valve must be eventually closed (event \( \text{close} \) must eventually occur) within at most \( w \) scan cycles. The remaining part of the property says that when PLC1 receives a request to open the valve (event \( \text{open}_{\text{req}} \)), if the valve gets closed (event \( \text{close} \)) within the \( w \)-th scan cycle, then it must remain closed for the \( d \) consecutive scan cycles. Here, \( d \) depends both on the maximum level of water reachable in \( T_2 \) in \( w \) scan cycles and on the physical law governing the water flow from \( T_2 \) to \( T_3 \).

6 MONITOR SYNTHESIS

In this section, we provide an algorithm to synthesise monitors from regular properties whose events are contained in (the set of events associated to) a fixed set \( \mathcal{P} \) of observable controller actions. More precisely, given a global property \( e \in \mathcal{P}_{\text{To}} \mathcal{P}_{\text{G}} \) the algorithm returns an edit automaton \( \nu \in \text{Edit} \) that is capable to enforce the property \( e \) during the execution of a generic controller whose possible actions are confined to those in \( \mathcal{P} \). The synthesis algorithm is defined in Table 5 by induction on the structure of the global/local property given in input; as we distinguish global properties from local ones, we define our algorithm in two steps.

**Remark 3.** We recall that, according to the operational semantics defined in Table 1, all controller actions \( a \) are observable and they basically coincide with the set \( \text{Events used to build up the enforcing properties defined in Section 5.} \) As a consequence, we will synthesise enforcing monitors that may observe any action of the controller under scrutiny and may act consequently.

The monitor \( \nu \ | \ p^+ \ | \ G \) associated to a global property \( p^+ \) is an edit automaton defined via the recursive equation \( X = \{ p \} \nu X^p \), to recursively enforce the local property \( p \). The monitor \( \nu \ | \ e_1 \land e_2 \ | \ G \) is given by the cross product between the edit automata \( \nu \ | \ e_1 \ | \ G \) and \( \nu \ | \ e_2 \ | \ G \), to accept only traces that satisfy both \( e_1 \) and \( e_2 \); the definition of the cross product between two edit automata recalls that for finite state automata, and it is reported in the appendix in Table 6. The monitor \( \nu \ | \ p_1 \land p_2 \ | \ G \) is given by the cross product between the edit automata \( \nu \ | \ p_1 \ | \ G \) and \( \nu \ | \ p_2 \ | \ G \). The monitor \( \nu \ | \ p_1 \land p_2 \ | \ G \) is given by the automaton \( \nu \ | \ p_1 \ | \ G \), where \( Z = \{ p_2 \} \nu X \); basically \( Z \) ties the final states of the automaton enforcing \( p_1 \) with the initial state of the automaton enforcing \( p_2 \) (e.g., \( \nu \ | \ e \ | \ G \nu X = \{ e \} \nu Z \), for \( Z = \{ p_2 \} \nu X \)). The monitor associated to a union property \( \cup_{1 \leq i \leq n} p_i \) does the following: (i) allows all actions associated to the events \( \pi_i \), (ii) inserts an action associated to some admissible event \( \pi_i \) only when the controller wishes to prematurely complete the scan cycle, i.e., it emits an \( \text{end} \)-action, and (iii) suppresses any other action except for \( \text{tick} \)- and \( \text{end} \)-actions.

Thus, the mitigation of the enforcement is actually implemented in the monitors synthesised from union properties. In practise, when the controller under scrutiny complies with the property enforced by the monitor, the two components, monitor and controller, evolve in a tethered fashion (by applying rule (Allow)), moving through related correct states. However, if the controller gets somehow corrupted (for instance, due to the presence of a malware) then the two components will get misaligned reaching unrelated states. In this case, the enforcer mitigates the attack by suppressing the remaining actions emitted by the controller (by applying rule (Suppress)) until the
Without any involvement of the controller, via one or more applications of the rule (Insert), the violation of the maximum cycle limit whose consequence would be the immediate shutdown of the controller [59].

As said in Section 2, a malware that aims to take control of the plant has no interest in delaying the scan cycle and risking the violation of the maximum cycle limit whose consequence would be the immediate shutdown of the controller [59].

### Proposition 2 (Deterministic preservation). Given a deterministic global property \( e \in \mathcal{P} \) over a set of events \( \mathcal{P} \). The edit automaton \( \mathcal{A}(e) \) is deterministic.

**Remark 4.** Note that even when the controller is completely unreliable and the monitor inserts an entire safe trace, the assumption made in Remark 1 ensures us that the enforced scan cycle always ends well before a violation of the maximum cycle limit.

Now, we calculate the complexity of the synthesis algorithm based on the number of occurrences of the operator \( \cap \) in \( \mathcal{e} \) and the dimension of \( \mathcal{e} \), \( \text{dim}(\mathcal{e}) \), i.e., the number of all operators occurring in \( \mathcal{e} \). Intuitively, the size of a property is given by the number of operators occurring in it.

**Definition 6.** Let \( \text{dim}() : \mathcal{P} \rightarrow \mathbb{N} \) be a property-size function defined as:

\[
\begin{align*}
\text{dim}(p^*) & \triangleq \text{dim}(p) + 1, \\
\text{dim}(\mathcal{e}) & \triangleq 1, \\
\text{dim}(\mathcal{e}_1 \cap \mathcal{e}_2) & \triangleq \text{dim}(\mathcal{e}_1) + \text{dim}(\mathcal{e}_2) + 1, \\
\text{dim}(\mathcal{p}_1 \cap \mathcal{p}_2) & \triangleq \text{dim}(\mathcal{p}_1) + \text{dim}(\mathcal{p}_2) + 1, \\
\text{dim}(\bigcup_{i \in I} \mathcal{a}_i \cdot \mathcal{p}_i) & \triangleq |I| + \sum_{i \in I} \text{dim}(\mathcal{p}_i).
\end{align*}
\]

**Proposition 1 (Complexity).** Let \( e \in \mathcal{P} \) be a global property and \( \mathcal{P} \) be a set of actions such that events \( \mathcal{e} \subseteq \mathcal{P} \). The complexity of the algorithm to synthesise \( \mathcal{A}(e) \) is \( O(|\mathcal{P}| \cdot m^{k+1}) \), with \( m = \text{dim}(e) \) and \( k \) being the number of occurrences of the operator \( \cap \) in \( e \).

In the following, we prove that the enforcement induced by our synthesised monitors enjoys the properties stated in the Introduction: determinism preservation, transparency, soundness, deadlock-freedom, divergence-freedom, and scalability. In this section, with a small abuse of notation, given a set of observable actions \( \mathcal{P} \), we will use \( \mathcal{P} \) to denote also the set of the corresponding events.

Given a deterministic global property \( e \), our synthesis algorithm returns a deterministic enforcer (according to Definition 2), i.e., an enforcer that can be effectively implemented. Formally,

1As said in Section 2, a malware that aims to take control of the plant has no interest in delaying the scan cycle and risking the violation of the maximum cycle limit whose consequence would be the immediate shutdown of the controller [59].
Let us move to transparency. Intuitively, the enforcement induced by a deterministic property \( e \in \mathbb{P}_{\mathbb{D}} \mathbb{G} \) should preserve any execution trace satisfying \( e \) itself (Definition 2 at pag. 5 of [40]).

**Theorem 1 (Transparency).** Let \( e \in \mathbb{P}_{\mathbb{D}} \mathbb{G} \) be a deterministic global property, \( \mathcal{P} \) be a set of observable actions such that \( \text{events}(e) \subseteq \mathcal{P} \), and \( P \in \mathbb{C}_\tau \mathbb{I} \) be a controller. Let \( t = a_1 \cdots a_n \) be a trace of the controller \( P \) with \( t \in [e] \). Then, (1) \( t \) is a trace of the edit automaton \( \langle e \rangle^\mathcal{P} \), and (2) there is no trace \( t' = a_1 \cdots a_k \cdot \lambda \) for \( \lambda \in \{ \alpha \}_{\alpha < k} \) for some \( \alpha \).

Basically, conclusion (1) says that all execution trace \( t \) (of a controller \( P \)) satisfying the enforcing property \( e \) are allowed by the associated enforcer \( \langle e \rangle^\mathcal{P} \), while conclusion (2) says that allowing the trace \( t \) is the only possible option in the enforcement (this follows by the determinism of \( e \)).

Another important property of our enforcement is soundness [40]. Intuitively, a controller under the scrutiny of a monitor \( \langle e \rangle^\mathcal{P} \) should only yield execution traces which satisfy the enforced property \( e \), i.e., execution traces which are consistent with its semantics \([e]\) (up to \( \tau \)-actions).

**Theorem 2 (Soundness).** Let \( e \in \mathbb{P}_{\mathbb{D}} \mathbb{G} \) be a global property, \( \mathcal{P} \) be a set of observable actions such that \( \text{events}(e) \subseteq \mathcal{P} \), and \( P \in \mathbb{C}_\tau \mathbb{I} \) be a controller. If \( t \) is a trace of the monitored controller \( \langle e \rangle^\mathcal{P} \Rightarrow \{ P \} \) then \( i \) is a prefix of some trace in \([e]\) (see Notation 1 for the definition of the trace \( i \)).

Here, it is important to stress that in general soundness does not ensure deadlock-freedom of the monitored controller. That is, it may be possible that the enforcement of some property \( e \) causes a deadlock of the controller \( P \) under scrutiny. In particular, this may happen in our controllers only when the initial sleeping phase does not match the enforcing property (\( e \)).

**Definition 7.** For \( k \in \mathbb{N}^+ \), we say that \( p \in \mathbb{P}_{\mathbb{D}} \mathbb{L} \) is a \( k \)-sleeping local property, only if \([p] = \{ t \mid t = t_1 \cdot \ldots \cdot t_n, \text{ for } n > 0, \text{ s.t. } t_i = \text{tick}^k \cdot t'_i \cdot \text{end}, t'_i \notin t'_1, \text{ and } 1 \leq i \leq n \} \). We say that \( p^* \) is a \( k \)-sleeping global property only if \( p \) is, and \( e = e_1 \cap e_2 \) is \( k \)-sleeping only if both \( e_1, e_2 \) are \( k \)-sleeping.

The enforcement of \( k \)-sleeping properties does not introduce deadlocks in \( k \)-sleeping controllers. This is because our synthesised monitors suppress all incorrect actions of the controller under scrutiny, driving it to the end of its scan cycle. Then, the controller remains in stand-by while the monitor yields a safe sequence of actions to mimic a safe completion of the current scan cycle.

**Theorem 3 (Deadlock-freedom).** Let \( e \in \mathbb{P}_{\mathbb{D}} \mathbb{G} \) be a \( k \)-sleeping global property, and \( \mathcal{P} \) be a set of observable actions such that \( \text{events}(e) \subseteq \mathcal{P} \). Let \( P \in \mathbb{C}_\tau \mathbb{I} \) be a controller of the form \( P = \text{tick}^k \cdot S \) whose set of observable actions is contained in \( \mathcal{P} \). Then, \( \langle e \rangle^\mathcal{P} \Rightarrow \{ P \} \) does not deadlock.

Another important property of our enforcement mechanism is divergence-freedom. In practice, the enforcement does not introduce divergence: monitored controllers will always be able to complete their scan cycles by executing a finite number of actions. This is because we limit our enforcement to well-formed properties (Definition 4) which always terminates with an \text{end} event. In particular, the well-formedness of local properties ensures us that in a global property of the form \( p^* \) the number of events within two subsequent \text{end} events is always finite.

**Theorem 4 (Divergence-freedom).** Let \( e \in \mathbb{P}_{\mathbb{D}} \mathbb{G} \) be a global property, \( \mathcal{P} \) be a set of observable actions such that \( \text{events}(e) \subseteq \mathcal{P} \), and \( P \in \mathbb{C}_\tau \mathbb{I} \) be a controller. Then, there exists a \( k \in \mathbb{N}^+ \) such that whenever \( \langle e \rangle^\mathcal{P} \Rightarrow \{ P \} \) \( \rightarrow \) \( E \Rightarrow \{ J \} \), if \( E \Rightarrow \{ J \} \) \( \rightarrow \) \( E' \Rightarrow \{ J' \} \), with \( | t' | \geq k \), then \text{end} \( t' \).

Notice that all properties seen up to now scale to field communications networks of controllers. This means that they are preserved when the controller under scrutiny is running in parallel with other controllers in the same field communications network. As an example, by an application
of Theorems 1 and 2, we show how both transparency and soundness scale to field networks. A similar result applies to the remaining properties.

**Corollary 1 (Scalability to networks of PLCs).** Let \( e \in \mathcal{P}_{\text{observable}} \) be a global property and \( \mathcal{P} \) be a set of observable actions, such that \( \text{events}(e) \subseteq \mathcal{P} \). Let \( P \in \mathcal{C} \) be a controller and \( N \in \mathcal{FNet} \) be a field network. If \( (\langle |e| \rangle \mathcal{P} \triangleright \{P\}) \parallel N \xrightarrow{t} (E \triangleright \{J\}) \parallel N' \), for some \( t, E, J \) and \( N' \), then

- whenever \( P \xrightarrow{t'} J \), with \( t' = \alpha_1 \cdots \alpha_n \in [e] \), the trace \( t' \) is a trace of \( \langle |e| \rangle \mathcal{P} \) and there is no trace \( t'' = \alpha_1 \cdots \alpha_k \cdot \lambda \) of \( \langle |e| \rangle \mathcal{P} \) such that \( 0 \leq k < n \) and \( \lambda \in \{-\alpha_{k+1}, \alpha < \alpha_{k+1}\} \), for some \( \alpha \);
- whenever \( \langle |e| \rangle \mathcal{P} \triangleright \{P\} \xrightarrow{t'} E \triangleright \{J\} \) the trace \( t' \) is a prefix of some trace in \([e] \).

7 OUR ENFORCEMENT MECHANISM AT WORK

In this section, we propose an implementation of our enforcement mechanism in which monitors, running on field-programmable gate arrays (FPGAs) [61], enforce open source PLCs [8], running on Raspberry Pi devices [25], and governing a physical plant simulated in Simulink [44]. The section has the following structure. In Section 7.1, we argue why FPGAs are good candidates for implementing secure proxies. In Section 7.2, we describe how we implemented the whole enforcement architecture for the use case of Section 4. In Section 7.3, we test our implementation injecting the enforced PLCs with five different malware aiming at causing three different physical perturbations: tank overflow, valve damage, and pump damage. The attacks have been chosen to cover as much as possible the attacker model of Section 2. In particular, they include: a drop of the actuator commands of the valve, an integrity attack on the water-level sensors, a forgery of the actuator commands of the valve, a forgery of the message requests to open/close the valve, and a forgery of the actuator commands of the pumps. Section 7.4 discusses the performance of our implementation.

7.1 FPGAs as secure proxies for ICSs

Field-programmable gate arrays (FPGAs) are semiconductor devices that can be programmed to run specific applications. An FPGA consists of (configurational) logic blocks, routing channels and I/O blocks. The logic blocks can be configured to perform complex combinational functions and are further made up of transistor pairs, logic gates, lookup tables and multiplexers. The applications are written using hardware description languages, such as Verilog [60]. Thus, in order to execute an application on the FPGA, its Verilog code is converted into a sequence of bits, called bitstream, that is loaded into the FPGA.

FPGA are assumed to be secure when the adversary does not have physical access to the device, i.e., the bitstream cannot be compromised [32]. Recent FPGAs support remote updates of the bitstream by relying on authentication mechanisms to prevent unauthorised uploads of malicious logic [32].
Nevertheless, as said in the Introduction and advocated by McLaughlin and Mohan [45, 46], any form of runtime reconfiguration should be prevented. Summarising, under the assumption that the adversary does not have physical access to the FPGA and she cannot do remote updates, FPGAs represent a good candidate for the implementation of secure enforcing proxies.

7.2 An implementation of the enforcement of the SWaT system of Section 4

The proposed implementation adopts different approaches for plant, controllers and enforcers.

**Plant.** The plant of the SWaT system is simulated in Simulink [44], a framework to model, simulate and analyse cyber-physical systems, widely adopted in industry and research. A Simulink model is given by blocks interconnected via wires. Our Simulink model contains blocks to simulate water tanks, actuators (i.e., pumps and valves) and sensors (see Figure 9). In particular, water-tank blocks implement the differential equations that model the dynamics of the tanks according to the physical constraints obtained from [27, 43]. Actuation blocks receive commands from PLCs, whereas sensor blocks send measurements to PLCs. For simplicity, state changes of both pumps and valves do not occur instantaneously; they take 1 second. We ran our Simulink model on a laptop with 2.8 GHz Intel i7 7700 HQ, 16GB memory, and Linux Ubuntu 20.04 LTS OS.

**Controllers.** Controllers are defined in OpenPLC [8], an open source PLC capable of running user programs in all five IEC61131-3 defined languages [1]. Additionally, OpenPLC supports standard SCADA protocols, such as Modbus/TCP, DNP3 and Ethernet/IP. OpenPLC can run on a variety of hardware, from a simple Raspberry Pi to robust industrial boards. We installed OpenPLC on three Raspberry Pi 4 [55]; each instance runs one of the three ladder logics seen in Figure 4.

**Enforcers.** Enforcers are implemented using three NetFPGA-CML development boards [63]. Our synthesis algorithm is implemented in Python to return enforcers written in Verilog, and checked for correctness using ModelSim. The Verilog code is then compiled into a bitstream and executed in the FPGA. More precisely, our algorithm in Python takes as input a JSON file containing the property to be synthesised and other relevant informations, such as the number of input/output signals and a fixed priority among admissible safe output signals. Then, the property is parsed by means of the ANTLR parser [48]. After the parsing, our algorithm implements the synthesis of Table 5 to derive the enforcing edit automaton; this is written down into a JSON file. At this stage, the derived edit automaton is still somewhat abstract, as both end- and tick-actions are explicitly represented. Finally, the algorithm compiles the edit automaton into an enforcer written in Verilog, where the above abstractions are implemented. In particular, the passage of time (i.e., tick-actions) is represented and monitored via clock variables, while the end of scan cycles (i.e., end-actions) is implemented via specific code to synchronise enforcers and controllers, relying on clock variables. Thus, before each scan cycle the enforcer forwards the current inputs (coming from the plant) to the controller. Then, when the scan cycle is completed, it receives from the controller all the current...
outputs, and forwards them to the actuators. In the meanwhile, the enforcer monitors the passage of time via its clock variables, and when the scan cycle is completed (i.e., the controller sends all outputs) it moves to the state corresponding to the following scan cycle. Finally, in our FPGAs we also write some code to implement an UDP-based network connecting together enforcers, PLCs, and the simulated plant.

The code of the three PLCs, the algorithm in Python, the enforcers written in Verilog, and the Simulink simulations can be found at: https://bitbucket.org/formal_projects/runtime_enforcement.

### 7.3 The enforced SWaT system under attack

In this section, we consider five different attacks targeting the PLCs of the SWaT system to achieve three possible malicious goals: (i) overflow the water tanks, (ii) damage of the valve, (iii) damage of the pumps. In order to simulate the injection of malware in the PLCs, we reinstall the original PLC ladder logics with compromised ones, containing some additional logic intended to disrupt the normal operations of the PLC [28]. In the following, we will discuss these attacks, grouped by goals, showing how the enforcement of specific properties mitigates the attacks by preserving the correct behaviour of the monitored PLCs.

#### Tank overflow. Our first attack is a DoS attack targeting PLC\(_1\) by dropping the commands to close the valve. In the left-hand side of Figure 10 we show a possible implementation of this attack in ladder logic. Basically, the malware remains silent for 500 seconds and then it sets true a malicious `drop` variable (highlighted in yellow). Once the variable `drop` becomes true, the `valve` variable is forced to be false (highlighted in red), thus preventing the closure of the valve.

In order to prevent attacks aiming at overflowing the tanks, we propose the following three enforcing properties, one for each PLC, respectively:

- \( e_1 \triangleq (\text{CBP}_{[1,m]}(h_1, \overline{\text{off}_1}))^* \cap (\text{CBP}_{[1,m]}(h_1, \overline{\text{off}_2}))^* \), an intersection between two conditional bounded persistency properties to enforce PLC\(_1\) to prevent water overflow in \( T_1 \). This property ensures that both pumps `pump_1` and `pump_2` are off, for \( m \) consecutive scan cycles, when the level of \( T_1 \) is high (measurement \( h_1 \)). Here, \( m < n \) for \( n \in \mathbb{N} \) is the number of scan cycles required to empty \( T_1 \) when its level is high, both pumps are off, and the valve is open.

- \( e_2 \triangleq (\text{CBP}_{[1,u]}(h_2, \overline{\text{close}_\text{req}}))^* \), a conditional bounded persistency property for PLC\(_2\) ensuring that requests to close the valve (event `close_req`) are sent for \( u \) consecutive scan cycles when the level of water in tank \( T_2 \) is high (measurement \( h_2 \)). Here, \( u < v \) for \( v \in \mathbb{N} \) is the number of scan cycles required to empty the tank \( T_2 \) when the level is high and the valve is closed.

- \( e_3 \triangleq (\text{CBP}_{[1,w]}(h_3, \overline{\text{on}_3}))^* \), a conditional bounded persistency property for PLC\(_3\) to ensure that `pump_3` is on for \( w \) consecutive scan cycles when the level of water in tank \( T_3 \) is high.
(measurement $h_3$). Here, $w < z$ for $z \in \mathbb{N}$ is the time (expressed in scan cycles) required to empty the tank $T_3$ when the level is high and $pump_3$ is on.

Now, let us analyse the effectiveness of the enforcement induced by these three properties. For instance, in the upper graphs of Figure 11 we report the impact on the tanks $T_1$ and $T_2$ of the DoS attack previously described, when enforcing the three properties $e_1$, $e_2$ and $e_3$ in the corresponding PLCs. Here, the red region denotes when the attack becomes active. As the reader may notice, despite repeated requests to close the valve coming from PLC$_2$, the compromised PLC$_1$ never closes the valve causing the overflow of tank $T_2$. So, the enforced property $e_1$ is not up the task.

In order to prevent this attack, we must guarantee that PLC$_1$ closes the valve when PLC$_2$ requests so. Thus, we should enforce in PLC$_1$ a more demanding property $e'_1$ defined as follows: $e_1 \cap \text{CBE}_{[1,1]}(\text{close\_req, close})$. Basically, the last part of the property ensures that every request to close the valve is followed by an actual closure of the valve in the same scan cycle. The impact of the malware on PLC$_1$ when enforcing the properties $e'_1$, $e_2$, $e_3$ is represented in the lower graphs of Figure 11. Now, the correct behaviour of PLC$_1$ is ensured, thus preventing the overflowing of the water tank $T_2$. In these graphs, the green highlighted regions denote when the monitor detects the attack and mitigates the activities of the compromised PLC$_1$. In particular, the monitor inserts the commands to close the valve on behalf of PLC$_1$ when PLC$_2$ sends requests to close the valve.

Having strengthened the enforcing property for PLC$_1$ one may think that the enforcement of $e_2$ in PLC$_2$ is now superfluous to prevent water overflow in $T_2$. However, this is not the case if the attacker can compromise PLC$_2$. Consider a second attack to PLC$_2$, an integrity attack that adds an offset of $-30$ to the measured water level of $T_2$. We show a ladder logic implementation of such attack in the right-hand side of Figure 10 where, for simplicity, we omit the initial silent phases lasting 500 seconds. The impact on the tanks $T_1$ and $T_2$ of the malware injected in PLC$_2$ in the presence of the enforcing of the properties $e'_1$ and $e_3$, respectively, is represented on the upper graphs of Figure 12. Again, the red region shows when the attack becomes active. As the reader may notice, the compromised PLC$_2$ never sends requests to close the valve causing the overflow of the water tank $T_2$. On the other hand, when enforcing the three properties $e'_1$, $e_2$, $e_3$ in the three
Fig. 12. Tank overflow: integrity attack on PLC₂ when enforcing $e'_1, e_3$ (up) and $e'_1, e_2, e_3$ (down).

PLCs, the lower graphs of Figure 12 shows that the overflow of tank $T_2$ is prevented. Again, the green highlighted regions denote when the monitor detects the attack and mitigates the commands of the compromised PLC₂. Here, the monitor inserts the request to close the valve on behalf of PLC₂ when $T_2$ reaches a high level.

Valve damage. We now consider attacks whose goal is to damage the valve via chattering, i.e., rapid alternation of openings and closings of the valve that may cause mechanical failures on the long run. In the left-hand side of Figure 13 we show a possible ladder logic implementation of a third attack that does injection of the commands to open and close the valve. In particular, the attack repeatedly alternates a stand-by phase, lasting 70 seconds, and a injection phase, lasting 30 seconds (yellow region); then, in the injection phase the valve is opened and closed rapidly (red region). With no enforcement, the impact of the attack on the tanks $T_1$ and $T_2$ is represented on the upper graphs of Figure 14, where the red region denotes when the attack becomes active. From the graph...
associated to the execution of $T_1$ the reader can easily see that the valve is chattering. Note that this is a *stealthy attack* as the water level of $T_2$ is maintained within the normal operation bounds.

In order to prevent this kind of attacks, we might consider to enforce in PLC$_1$ a bounded mutual exclusion property of the form $e''_1 \triangleq (\text{BME}_{10000}(\text{open, close}))^*$ to ensure that within 10000 consecutive scan cycles (10 seconds) openings and the closings of the valve may only occur in mutual exclusion. When the property $e''_1$ is enforced in PLC$_1$, the lower graphs of Figure 14 shows that the chattering of the valve is prevented. In particular, the green highlighted regions denote when the monitor detects the attack and mitigates the commands on the valves of the compromised PLC$_1$.

A fourth attack with the same goal of chattering the valve may be launched on PLC$_2$, by sending rapidly alternating requests to open and close the valve. This can be achieved by means of an *integrity attack* on the sensor of the tank $T_2$ by rapidly switching the measurements between low and high. In the right-hand side of Figure 13 we show parts of the ladder logic implementation of this attack on PLC$_2$, where, for simplicity, we omit the machinery for dealing with the alternation of phases. Again, the attack repeatedly alternates between a *stand-by phase*, lasting 70 seconds, and a *active phase*, lasting 30 seconds. When the attack is in the active phase (red region) the measured water level of $T_2$ rapidly switches between low and high, thus, sending requests to PLC$_1$ to rapidly open and close the valve in alternation.

The impact of this attack targeting on PLC$_2$ in the absence of an enforcing monitor is represented in the upper graphs of Figure 15, where the red region shows when the attack becomes active. Notice that the rapid alternating requests originating from PLC$_2$ cause a chattering of the valve. On the other hand, with the enforcement of the property $e''_1$ in PLC$_1$, the lower graph of Figure 15 shows that the correct behaviour of tanks $T_1$ and $T_2$ is ensured. In that figure, the green highlighted regions denote when the enforcer of PLC$_1$ detects the attack and mitigates the commands (on the valve) of the compromised PLC$_2$. Notice that in this case no enforcement is required in PLC$_2$.

**Pump damage.** Finally, we consider attacks whose goal is the damage of the pumps, and in particular pump$_3$. In that case, an attacker may force the pump to start when the water tank $T_3$ is
empty. This can be done with a fifth attack that injects commands to turn on the pump based on a ladder logic implementation similar to that seen in Figure 10. The impact of this attack to tank $T_3$ in the absence of enforcement is represented on the left-hand side graphs of Figure 16, where the red region shows when the attack becomes active. As the reader may notice, $pump_3$ is turned on when $T_3$ is empty.

Now, we can prevent damage on $pump_3$ by enforcing on PLC$_3$ the following conditional bounded persistent property: $e'_3 \triangleq (\text{CBP}_{1,w}[(I_3, \text{off}_3)])^\ast$. The enforcement of this property ensures that $pump_3$ is off for $w$ consecutive scan cycles when the level of water in tank $T_3$ is low, for $w < z$ and $z \in \mathbb{N}$ being the time (expressed in scan cycles) required fill up tank $T_3$ when the pump is off. Thus, when the enforcement of the $e'_3$ is active, the lower graphs of Figure 16 shows that the correct behaviour of $T_3$ is ensured, thus preventing pump damage. In that figure, the green highlighted regions denote when the monitor detects the attack and mitigates the commands (of the pumps) of the compromised PLC$_3$. More precisely, the enforcer suppresses the commands to turn on the pump when the tank is empty, for $w$ consecutive scan cycles.

Fig. 15. Valve damage: integrity attack on PLC$_2$ in the absence (up) and in the presence (down) of enforcement.

7.4 Discussion

In this section, we rely on the Vivado Design Suite 15.2 analysis tool to do a performance analysis of our implementation.

As to the hardware resources used by our FPGAs, we measured them in terms of lookup tables and registers used during the enforcement. The number of them depends on the number of states of the enforcers implemented in the FPGAs. And this number is proportional to the number of scan cycles involved in the enforced (local) property. In particular, for each scan cycle, the number $k$ of states of the enforcer depends on the monitored input/output signals and their admissible values. For instance, for scan cycles taking 10 ms (0.1kHz), an enforced local property lasting 10 seconds will cover 1000 consecutive scan cycles, and the synthesised enforcer would have $k \approx 1000$ states. In our experiments, when enforcing properties covering 1000 scan cycles the hardware resource use reaches 5%; for 10000 scan cycles the resource use rises to 13%.
As for the execution speed of the enforcement, in general all FPGAs are capable of running at a speed of 100 MHz (or higher). The actual execution speed depends on the complexity of the underlying code, in our case the enforcer, plus some extra code to implement the network communication protocol (UDP). In our experiments, FPGAs ran with a frequency of 1 MHz while PLCs ran with a frequency of 0.1-1kHz. Thus, the overhead introduced by the FPGAs is negligible, independently on the size (the number of states) of the enforcer implemented in the FPGAs. We recall that in Remark 1 we assumed that our enforced controllers successfully complete their scan cycle in less than half of the maximum cycle limit (just in case the scan cycle should be entirely corrected by the enforcer). However, using FPGAs as enforcers this constraint can be actually relaxed.

Finally, concerning the communication latency between enforcers, many FPGAs support high speed and low latency communications, which are the ones used in industrial control contexts [47]. We used FPGAs with Ethernet ports supporting 1 Gbps speed, i.e., with 100 microseconds latency. Furthermore, thanks to our result of scalability (Corollary 1), a network of enforcing FPGAs introduces a negligible overhead in terms of communication latency and hardware resources.

8 RELATED WORK

The notion of runtime enforcement was introduced by Schneider [56] to enforce security policies via truncation automata, a kind of automata that terminates the monitored system in case of violation of the property. Thus, truncation automata can only enforce safety properties. Furthermore, the resulting enforcement may obviously lead to deadlock (actually termination) of the monitored system with no room for mitigation.

Ligatti et al. [40] extended Schneider’s work by proposing the notion of edit automata, i.e., an enforcement mechanism able of replacing, suppressing and inserting system actions. Edit automata are capable of enforcing instances of safety and liveness properties, along with other properties such as renewal properties [12, 40]. In general, Ligatti et al.’s edit automata are deterministic automata with an enumerable number of states, whereas in the current paper we restrict ourselves to finite-state edit automata equipped with Martinelli and Matteucci’s operational semantics [42]. Ligatti et al. [40] studied a hierarchy of enforcement mechanisms, each with different transformational capabilities: Schneider’s truncation automata, suppression automata, insertion automata, and finally, edit automata that combine the power of suppression and insertion automata. They defined different notions of enforcement, and in particular the so called precise enforcement (Definition 2, pag. 5) which basically corresponds to the combination of our notion of transparency and soundness, proved in Theorems 1 and 2, respectively.

Bielova and Massacci [12, 13] provided a stronger notion of enforceability by introducing a predictability criterion to prevent monitors from transforming invalid executions in an arbitrary manner. Intuitively, a monitor is said predictable if one can predict the number of transformations
used to correct invalid executions. In our setting, in case of injection of a malware which may act in an unpredictable manner, this approach appears unfeasible.

Falcone et al. [21, 22] proposed a synthesis algorithm, relying on Streett automata, to translate most of the property classes defined within the safety-progress hierarchy [41] into (a slight variation of) edit automata. In the safety-progress hierarchy, our global properties can be seen as guarantee properties, for which all execution traces that satisfy a property contain at least one prefix that still satisfies the property. However, it should be noticed that they consider untimed properties only; as already pointed out before, timed actions play a special role in our enforcement and they cannot be treated as untimed actions.

Beauquier et al. [10] proved that finite-state edit automata (i.e., those edit automata we are actually interested in) can only enforce a sub-class of regular properties. Actually they can enforce all and only the regular properties that can be recognised using finite automata whose cycles always contain at least one final state. This is the case of our enforced regular properties, as well-formed local properties in \( \mathbb{P} \cap \mathbb{L} \), always terminate with the “final” atomic property \( \text{end} \).

Pinisetty and Tripakis [51] studied the compositionality of the enforcement of different regular properties \( p_1, \ldots, p_n \) at the same time, by composing the associated enforcing monitors. The idea is to replace a monolithic approach, in which a monitor is synthesised from the property \( p_1 \cap \ldots \cap p_n \), with a compositional one, where the \( n \) monitors enforcing the properties \( p_i \) are somehow put together to enforce \( p_1 \cap \ldots \cap p_n \). The authors of [51] proved that runtime enforcement is not compositional with respect to general regular properties, neither with respect to serial nor parallel composition. On the other hand compositionality holds for certain sub-classes of regular properties such as safety (or co-safety) properties. Here, we wish to point out that our notion of scalability is different from their notion of compositionality, as we aim at scaling our enforcement on a network of PLCs and not on multiple regular properties on the same PLC.

Bloem et al. [14] defined a synthesis algorithm that given a safety property returns a monitor, called shield, to enforce untimed properties in reactive systems (which have many aspects in common with control systems). Their algorithm rely on a notion called \( k \)-stabilization: when the design reaches a state where a property violation becomes unavoidable for some possible future inputs, the shield is allowed to deviate for at most \( k \in \mathbb{N} \) steps; if a second violation happens during the \( k \)-step recovery phase, the shield enters a fail-safe mode where it only enforces correctness, but no longer minimises the deviation. However, The \( k \)-stabilizing shield synthesis problem is unrealisable for many safety-critical systems, because a finite number of deviations cannot be guaranteed. Humphrey et al. [33] addressed this problem by proposing the notion of admissible shields which was extended and generalised in Könighofer et al. [34] by assuming that systems have a cooperative behaviour with respect to the shield, i.e., the shield ensures a finite number of deviations if the system chooses certain outputs. The authors presented a synthesis procedure that maximises the cooperation between system and environment for satisfying the required enforced properties. This approach has some similarities with our enforcement in which a violation of a property during a scan cycle induces the suppression of all subsequent controller actions until the PLC reaches the end of the scan, so the monitor can insert a safe trace before permitting the completion of the scan cycle.

Pinisetty et al. [50] proposed a bi-directional runtime enforcement mechanism for reactive systems, and more generally for cyber-physical relying on Berry and Gonthier’s synchronous hypothesis [11], to correct both inputs and outputs. Pinisetty et al. express safety properties in terms of Discrete Timed Automata (DTA) which are more expressive than our class of regular properties. Thus, an execution trace satisfies a required property only if it ends up on a final state of the corresponding DTA. However, as not all regular properties can be enforced [10], they proposed a more permissive enforcement mechanism that accepts execution traces as long as there is still the possibility of
reaching a final state. Furthermore, due to the instantaneousness of the synchronous approach, their enforcement actions are applied in the same reaction step to ensure reactivity. On the contrary, in our approach the enforcement takes places before the conclusion of scan cycles which are clearly delimited via end-actions. Our notion of deterministic enforcers is taken from Pinisetty et al. [50]. Moreover, when inserting safe actions, our synthesised enforcers follows Pinisetty et al.’s random edit approach, where the inserted safe action is randomly chosen from a list of admissible actions.

Pearce et al. [49] proposed a bi-directional runtime enforcement over valued signals for PLCs, by introducing smart I/O modules (similar to our secure proxy) between the PLCs and the controlled physical processes, to act as an effective line of defence. The authors express security properties in terms of Values Discrete Timed Automata (VDTA), inspired by the DTA of Pinisetty et al. [50]. Unlike DTA, VDTA support valued signals, internal variables, and guard conditions. As in Pinisetty et al. [50], the paper adopts the synchronous hypothesis [11] to correct both inputs and outputs; thus, their enforcement actions are applied in the same reaction step to ensure instantaneous reactivity. The authors do not consider attacks that may tamper with inter-controller communications: their attackers may only manipulate sensor signals and/or actuator commands. Finally, their semantics requires that every enforcer knows the state of all relevant signals and commands in a given system. Thus, as written by the same authors, a networked system featuring multiple I/O modules may significantly complicate the enforcement, as pertinent I/O for a security policy may not be locally available. As a consequence, unlike us, their enforcement does not naturally scale to networks of controllers; we believe this is basically due to the fact that they do bi-directional enforcement. Last but not least, like them, we implement enforcers via FPGAs to ensure efficiency and security at the same time. In particular, when inserting safe actions our implementation fixes a priority between admissible safe actions, similarly to their selected edit approach. However, our implementation differs from theirs in at least the following aspects: (1) our FPGAs do enforce PLC transmissions (with a negligible latency); (2) our enforcement is uni-directional and hence our FPGAs need to know only the state of signals and commands of the corresponding enforced PLCs; (3) as a consequence, our FPGAs can be networked to monitor field communications networks paying only negligible overhead in terms of computational resources and communication latency.

Aceto et al. [6] developed an operational framework to enforce properties in HML logic with recursion ($\mu$HML) relying on suppression. More precisely, they achieved the enforcement of a safety fragment of $\mu$HML by providing a linear automated synthesis algorithm that generates correct suppression monitors from formulas. Enforceability of modal $\mu$-calculus (a reformulation of $\mu$HML) was previously tackled by Martinelli and Matteucci [42] by means of a synthesis algorithm which is exponential in the length of the enforceable formula. Cassar [18] defined a general framework to compare different enforcement models and different correctness criteria, including optimality. His works focuses on the enforcement of a safety fragment of $\mu$HML, paying attention to both uni-directional and bi-directional notions of enforcement. More recently, Aceto et al. [7] developed an operational framework for bi-directional enforcement and used it to study the enforceability of the aforementioned safety fragment of HML with recursion, via a specific type of bi-directional enforcement monitors called action disabling monitors.

As regards papers in the context of control system security closer to our objectives, McLaughlin [45] proposed the introduction of an enforcement mechanism, called C$^2$, similar to our secure proxy, to mediate the control signals $u_k$ transmitted by the PLC to the plant. Thus, like our secured proxy, C$^2$ is able to suppress commands, but unlike our proxy, it cannot autonomously send commands to the physical devices in the absence of a timely correct action from the PLC. Furthermore, C$^2$ does not seem to cope with inter-controller communications, and hence with colluding malware operating on PLCs of the same field network.
Mohan et al. [46] proposed a different approach by defining an ad-hoc security architecture, called Secure System Simplex Architecture (S3A), with the intention to generalise the notion of “correct system state” to include not just the physical state of the plant but also the cyber state of the PLCs of the system. In S3A, every PLC runs under the scrutiny of a side-channel monitor which looks for deviations with respect to safe executions, taking care of real-time constraints, memory usage, and communication patterns. If the information obtained via the monitor differs from the expected model(s) of the PLC, a decision module is informed to decide whether to pass the control from the “potentially compromised” PLC to a safety controller to maintain the plant within the required safety margins. As reported by the same authors, S3A has a number of limitations comprising: (i) the possible compromising of the side channels used for monitoring, (ii) the tuning of the timing parameters of the state machine, which is still a manual process.

The present work is a revised extension of the conference version appeared in [36]. Here, we provide a detailed comparison with that paper. In Section 2 we specified the attacker model and the attacker objectives. In Section 3, we adopted a simplified operational semantics for edit automata, in the style of Martinelli and Matteucci [42]. In Section 5, we have extended our language of regular properties with intersection of both local and global properties. With this extension we have expressed a wide family of correctness properties that can be combined in a modular fashion; these properties include and extend the three classes of properties appearing in the conference paper. In Section 6, we have extended our synthesis algorithm to deal with our extended properties: both local and global intersection of properties are synthesised in terms of cross products of edit automata. Notice that, compared to the conference paper, our enforcement mechanism does not rely anymore on an ad-hoc semantic rule (Mitigation) to insert safe actions at the end of the scan cycle, but rather on the more standard rule (Insert) together with the syntactic structure of synthesised enforcers. As stated in Proposition 1, now our synthesis algorithm depends on the size and the number of occurrences of intersection operators of the property in input. Last but not least, in this journal version we provide an implementation of our use case based on: (i) Simulink to simulate the physical plant, (ii) OpenPLC on Raspberry Pi to run open PLCs, and (iii) FPGAs to implement enforcers. We have then exposed our implementation to five different attacks targeting the PLCs and discussed the effectiveness of the proposed enforced mechanism.

In a preliminary work [37], we proposed an extension of our process calculus with an explicit representation for malware code. In that paper, monitors are synthesised from PLC code rather than correctness properties. The focus of that paper was mainly on: (i) deadlock-free enforcement, and (ii) intrusion detection via secure proxies. Here, it is worth pointing out that the work in [37] shares some similarities with supervisory control theory [15, 54], a general theory for automatic synthesis of controllers (supervisors) for discrete event systems, given a plant model and a specification for the controlled behaviour. Fabian and Hellgren [20] have pointed out a number of issues to be addressed when adopting supervisory control theory in industrial PLC-based facilities, such as causality, incorrect synchronisation, and choice between alternative paths. However, as our syntheses regard only logical devices (no plant involved), we are not affected from similar problems.

Finally, Yoong et al. [62] proposed a synchronous semantics for functions blocks, a component-oriented model at the core of the IEC 61499 international standard [2] used to design distributed industrial process measurement and control systems. In contrast to the scan cycle model followed in the current paper (IEC 61131 [1]) prescribing the execution of a sequential portion of code at each scan cycle, the event-driven model for function blocks relies on the occurrence of asynchronous events to trigger program execution. Yoong et al. [62] adopted a synchronous approach to define an execution semantics to function blocks by translating them into a subset of Esterel [11], a well-known synchronous language. Here, we wish to point out that our PLC specification is given
at a more abstract level compared to that of [62], and it complies with the sequential scan cycle standard IEC 61131, rather than the event-driven standard IEC 61499.

9 CONCLUSIONS AND FUTURE WORK

We have defined a formal language to express networks of monitored controllers, potentially compromised with colluding malware that may forge/drop actuator commands, modify sensor readings, and forge/drop inter-controller communications. The enforcing monitors have been expressed via a finite-state sub-class of Ligatti et al.’s edit automata. In this manner, we have provided a formal representation of field communications networks in which controllers are enforced via secure monitors, as depicted in Figure 2. The room of manoeuvre of attackers is defined via a proper attacker model. Then, we have defined a simple description language to express timed regular properties that are recognised by finite automata whose cycles always contain at least one final state (denoted via an end-action). We have used that language to build up formal definitions for pattern templates suitable for expressing a broad family of correctness properties that can be combined in a modular fashion to prescribe precise controller behaviours. As an example, our description language allows us to capture all (bounded variants of the) controller properties studied in Frehse et al. [24]. Once defined a formal language to describe controller properties, we have provided a synthesis function $\langle \cdot \mid \cdot \rangle$ that, given an alphabet $\mathcal{P}$ of observable controller actions and a deterministic regular property $e$ consistent with $\mathcal{P}$, returns a finite-state deterministic edit automaton $\langle e \rangle_{\mathcal{P}}$. The resulting enforcement mechanism will ensure the required features advocated in the introduction: transparency, soundness, deadlock-freedom, divergence-freedom, mitigation and scalability.

As a final contribution, we have provided a full implementation of a non-trivial case study in the context of industrial water treatment, where enforcers are implemented via FPGAs. In this setting, we showed the effectiveness our enforcement mechanism when exposed to five carefully-designed attacks targeting the PLCs of our use case.

As future work, we wish to test our enforcement mechanism in different domains, such as industrial and cooperative robotic arms (e.g., Kuka, ABB, Universal Robots, etc) which are endowed with control architectures working at a fixed rate [57]. More generally, we would like to consider physical plants with significant uncertainties, in terms of measurements noise and physical process uncertainty. This is because significant plant perturbations might falsely indicate that the monitored controller is under attack, inducing our enforcers to take erroneous correcting actions. To address such challenges we would like to implement in our enforcers well-know control-theory algorithms, based on linear difference equations, to correctly estimate the state of the physical plant even when affected by significant uncertainties. Finally, we would like to enhance our enforcers to deal with malicious alterations of sensor measurements due to compromised sensor devices. In order to do so, we intend to integrate our secured proxies with physics-based attack detection mechanisms [17, 26].

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In order to prove the results of Section 6, in Table 6 we provide the technical definition of cross product between two edit automata used in the synthesis of Table 5. As the first three cases are straightforward, we explain only the fourth case, the cross product associated to \( \text{Prod}^P_{\lambda} (\sum_{i \in I} \lambda_i, E_i, \sum_{j \in J} v_j, E_j) \)

Here, we use the abbreviation \( \lambda.E \oplus \lambda'.E \) to denote the automaton \( \lambda.E + \lambda'.E \) if \( \lambda \neq \lambda' \), and, the automaton \( \lambda.E \), if \( \lambda = \lambda' \). Thus, the product does the intersection of those addends \( \lambda_i, E_i \) and \( v_j, E_j \),

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Here, we use the abbreviation \( \lambda.E \oplus \lambda'.E \) to denote the automaton \( \lambda.E + \lambda'.E \) if \( \lambda \neq \lambda' \), and, the automaton \( \lambda.E \), if \( \lambda = \lambda' \). Thus, the product does the intersection of those addends \( \lambda_i, E_i \) and \( v_j, E_j \),
with \((i, j) \in H\), for which: (a) the prefixes have the same output (e.g., \(\lambda_i = \alpha\) and \(\nu_j = \alpha < \alpha'\)), (b) the prefixes are not suppressions, (c) the product of their continuations \(E_i\) and \(E_j\) “is not empty”, i.e., it is not a suppression-only automaton. For the other addends \(\lambda_i.E_i\) and \(\nu_j.E_j\) which do not comply with the above conditions (i.e., \((i, j) \notin H\)), the product results in a suppression-only automaton.

Let us prove the complexity of the synthesis algorithm formalised in Proposition 1. For that we need three technical lemmata. The first lemma shows that our synthesis algorithm always returns an edit automaton in a specific canonical form.

**Lemma 1 (Canonical Form).** Let \(e \in \mathbb{P} \cap \mathbb{P}_G\) and \(\mathcal{P}\) be a set of actions such that events(e) \(\subseteq \mathcal{P}\). Then, either \(\langle e \rangle \mathcal{P} = E\) or \(\langle e \rangle \mathcal{P} = Z\), with \(Z = E\), for \(E\) of the following form:

\[
E = \begin{cases} 
\sum \alpha_i.E_i + \sum \alpha_i < \text{end}.E_i + \sum_{\alpha \in Q} -\alpha.F, & \text{if end } \notin \bigcup_{i \in I} \alpha_i \\
\sum \alpha_i.E_i + \sum_{\alpha \in Q} -\alpha.F, & \text{otherwise.}
\end{cases}
\]

where \(\alpha_i \in \mathcal{P}\), \(Q = \mathcal{P} \setminus \left( \bigcup_{i \in I} \alpha_i \cup \{\text{tick}, \text{end}\} \right)\), and \(E_i\) and \(F\) edit automata. A similar result holds when \(e\) is replaced with some local property \(p \in \mathbb{P} \cap \mathbb{P}_L\).

**Proof.** The proof is by induction on the structure of the property \(e\). The most interesting case is when \(e = e_1 \cap e_2\). Then, \(\langle e_1 \cap e_2 \rangle \mathcal{P}\) returns \(\prod^\mathcal{P}_{\mathcal{X}}(\langle e_1 \rangle \mathcal{P}, \langle e_2 \rangle \mathcal{P})\). By inductive hypothesis, \(\langle e_1 \rangle \mathcal{P}\) and \(\langle e_2 \rangle \mathcal{P}\) have the required form. We prove the case when

- \(\langle e_1 \rangle \mathcal{P} = \sum \alpha_i.E_i + \sum \alpha_i < \text{end}.E_i + \sum_{\alpha \in Q} -\alpha.F', \text{ with } Q_1 = \mathcal{P} \setminus \left( \bigcup_{i \in I} \alpha_i \cup \{\text{tick}, \text{end}\} \right)\) and end \(\notin \bigcup_{i \in I} \alpha_i\)

- \(\langle e_2 \rangle \mathcal{P} = \sum_{j \in J} \alpha_j.F_j + \sum_{\alpha \in Q} -\alpha.F, \text{ with } Q_2 = \mathcal{P} \setminus \left( \bigcup_{i \in I} \alpha_i \cup \{\text{tick}, \text{end}\} \right)\) and end \(\notin \bigcup_{j \in J} \alpha_j\).

The other cases are similar or simpler. For any \(i \in I\) and \(j \in J\), we have: (i) out(\(\alpha_i\)) = out(\(\alpha_j\)) if and only if \(\alpha_i = \alpha_j\); (ii) out(\(\alpha_i < \text{end}\)) = out(\(\alpha_j\)) holds if and only if \(\alpha_i = \alpha_j\). We recall that out(\(\neg\alpha\)) = \(\tau\). Thus, the set \(H\) of the definition of cross product in Table 6 for \(\prod^\mathcal{P}_{\mathcal{X}}(\langle e_1 \rangle \mathcal{P}, \langle e_2 \rangle \mathcal{P})\) is equal to \(\{(i, j) \in I \times J : \alpha_i = \alpha_j \text{ and } \prod^\mathcal{P}_{\mathcal{X}_{i,j}}(E_i, F_j) \neq \bigcup_{\alpha \in \mathcal{P} \setminus \{\text{tick}, \text{end}\} - \alpha.X_{i,j})\text{, with } X_{i,j} = \prod^\mathcal{P}_{\mathcal{X}_{i,j}}(E_i, F_j)\}

As a consequence, we derive

\[
\prod^\mathcal{P}_{\mathcal{X}}(\langle e_1 \rangle \mathcal{P}, \langle e_2 \rangle \mathcal{P}) = \sum_{(i, j) \in H} \alpha_i.X_{i,j} + \sum_{(i, j) \in H} \alpha_i < \text{end}.X_{i,j} + \sum_{\alpha \in Q} -\alpha.X
\]

with \(Q = \mathcal{P} \setminus \left( \bigcup_{(i, j) \in H} \alpha_i \cup \{\text{tick}, \text{end}\} \right)\). It remains to prove that end \(\notin \bigcup_{(i, j) \in H} \alpha_i\). Since end \(\notin \bigcup_{i \in I} \alpha_i\) and end \(\notin \bigcup_{j \in J} \alpha_j\), then there is no \((i, j) \in H\) such that \(\alpha_i = \text{end}\). Thus, end \(\notin \bigcup_{(i, j) \in H} \alpha_i\), as required. \(\square\)
By an application of Lemma 1, we derive a second lemma which extends a classical result on the complexity of the cross product of finite state automata to the cross product of (synthesised) edit automata.

**Lemma 2.** Let \( e_1, e_2 \in \mathbb{P}_{\mathbb{R} \times \mathbb{D} \times \mathbb{G}} \) and \( \mathcal{P} \) be a set of observable actions. Let \( v_1, v_2 \) be the number of derivatives of \( \langle e_1 \parallel \mathcal{P} \rangle \) and \( \langle e_2 \parallel \mathcal{P} \rangle \), respectively. The complexity of the algorithm to compute \( \text{Prod}_{\mathcal{P}}^\delta (\langle e_1 \parallel \mathcal{P} \rangle, \langle e_2 \parallel \mathcal{P} \rangle) \) is \( O(|\mathcal{P}| \cdot v_1 \cdot v_2) \). A similar result holds for edit automata derived from local properties \( p_1, p_2 \in \mathbb{P}_{\mathbb{R} \times \mathbb{D} \times \mathbb{L}} \).

The third lemma provides an upper bound to the number of derivatives of the automaton \( \langle e \parallel \mathcal{P} \rangle \).

**Lemma 3 (Upper bound of number of derivatives).** Let \( e \in \mathbb{P}_{\mathbb{R} \times \mathbb{D} \times \mathbb{G}} \) be a global property with \( m = \dim(e) \), and \( \mathcal{P} \) be a set of observable actions. Then, the number of derivatives of \( \langle e \parallel \mathcal{P} \rangle \) is at most \( m^{k+1} \), where \( k \) is the number of occurrences of the symbol \( \cap \) in \( e \).

**Proof.** The proof is by structural induction on \( e \). Let \( e \equiv e_1 \cap e_2 \) and \( m = \dim(e_1 \cap e_2) \). By definition, the synthesis function recalls itself on \( e_1 \) and \( e_2 \). Obviously, \( m_1 + m_2 = m - 1 \) with \( m_1 = \dim(e_1) \) and \( m_2 = \dim(e_2) \). Let \( k, k_1 \) and \( k_2 \) be the number of occurrences of the symbol \( \cap \) in \( e_1 \) and \( e_2 \), respectively. We deduce that \( k_1 + k_2 = k - 1 \). By inductive hypothesis, \( \langle e_1 \parallel \mathcal{P} \rangle \) has at most \( m_1^{k_1+1} \) derivatives, and \( \langle e_2 \parallel \mathcal{P} \rangle \) has at most \( m_2^{k_2+1} \) derivatives. As the synthesis returns the cross product between \( \langle e_1 \parallel \mathcal{P} \rangle \) and \( \langle e_2 \parallel \mathcal{P} \rangle \), we derive that the resulting edit automaton will have at most \( m_1^{k_1+1} \cdot m_2^{k_2+1} \) derivatives. The result follows because \( m_1^{k_1+1} \cdot m_2^{k_2+1} = m^{k+1} \). \( \square \)

**Proof of Proposition 1 (Complexity).** For any property \( e \in \mathbb{P}_{\mathbb{R} \times \mathbb{D} \times \mathbb{G}} \) and any set of observable actions \( \mathcal{P} \), we prove that the recursive structure of the function returning \( \langle e \parallel \mathcal{P} \rangle \) can be characterised in the following form: \( T(m) = T(m - 1) + |\mathcal{P}| \cdot m^k \), with \( m = \dim(e) \), and \( k \) the number of occurrences of \( \cap \) in \( e \). The result follows because \( T(m) = T(m - 1) + |\mathcal{P}| \cdot m^k \) is \( O(|\mathcal{P}| \cdot m^{k+1}) \). The proof is by case analysis on the structure of \( e \), by examining each synthesis step in which the synthesis process \( m = \dim(e) \) symbol.

Case \( e \equiv e_1 \cap e_2 \). Let \( m = \dim(e_1 \cap e_2) \). By definition, the synthesis \( \langle e_1 \cap e_2 \parallel \mathcal{P} \rangle \) call itself on \( e_1 \) and \( e_2 \), with \( m_1 = \dim(e_1) \) and \( m_2 = \dim(e_2) \) symbols, respectively, where \( m_1 + m_2 = m - 1 \). Let \( k \) be the number of occurrences of \( \cap \) in \( e \) and \( k_1, k_2 \) be the number of occurrences of \( \cap \) in \( e_1 \) and \( e_2 \), respectively. We deduce that \( k_1 + k_2 = k - 1 \). By an application of Lemma 2, the complexity of the algorithm to compute \( \text{Prod}_{\mathcal{P}}^\delta (\langle e_1 \parallel \mathcal{P} \rangle, \langle e_2 \parallel \mathcal{P} \rangle) \) is \( O(|\mathcal{P}| \cdot v_1 \cdot v_2) \), where \( v_1 \) and \( v_2 \) are the number of derivatives of \( \langle e_1 \parallel \mathcal{P} \rangle \) and \( \langle e_2 \parallel \mathcal{P} \rangle \), respectively. By an application of Lemma 3, we have that \( v_1 \leq m_1^{k_1+1} \) and \( v_2 \leq m_2^{k_2+1} \). Thus, the number of operations required for the cross product between \( \langle e_1 \parallel \mathcal{P} \rangle \) and \( \langle e_2 \parallel \mathcal{P} \rangle \) is \( O(|\mathcal{P}| \cdot m_1^{k_1+1} \cdot m_2^{k_2+1}) \). Thus, we can characterise the recursive structure as: \( T(m) = T(m_1) + T(m_2) + |\mathcal{P}| \cdot m_1^{k_1+1} \cdot m_2^{k_2+1} \). We notice that the complexity of this recursive form is smaller than the complexity of \( T(m-1) + |\mathcal{P}| \cdot m^k \).

\(^2\)These numbers are finite as we deal with finite-state edit automata.
Case \( e \equiv p^* \). In order to prove this case, as \( m = \dim(p^*) = \dim(p) + 1 \) and \( \langle p^* \rangle_P \triangleq X \), for
\( X = \langle p \rangle_P \rangle_P \), we proceed by case analysis on \( p \in \mathcal{P}_{\tau \oplus \mathcal{L}} \). Thus, we consider the local properties \( p \in \mathcal{P}_{\tau \oplus \mathcal{L}} \). We focus on the most significant case \( p = \bigcup_{i \in I} \pi_i \). We have that \( m - 1 = \dim\left( \bigcup_{i \in I} \pi_i \right) \).

By definition, the synthesis \( \langle \bigcup_{i \in I} \pi_i \rangle_P \rangle_P \) consumes all events \( \pi_i \), for \( i \in I \). The synthesis algorithm re-calls itself \( |I| \) times on \( p_i \), with \( \dim(p_i) \) symbols, for \( i \in I \). Furthermore, let \( l \) be the size of the set \( \mathcal{P} \), the algorithm performs at most \( l \) operations due to a summation over \( \alpha \in \mathcal{P} \setminus \left( \bigcup_{i \in I} \pi_i \cup \{\text{tick, end}\} \right) \), with \( | \mathcal{P} \setminus \left( \bigcup_{i \in I} \pi_i \cup \{\text{tick, end}\} \right) | < l \). Thus, we can characterise the recursive structure as \( T(m) = \sum_{i \in I} T(\dim(p_i)) + l \). Since \( \sum_{i \in I} \dim(p_i) = m - 1 - |I| \leq m - 1 \). The resulting complexity is smaller than that of \( T(m - 1) + |\mathcal{P}| \cdot m^k \).

\[ \square \]

**Proof of Proposition 2 (Deterministic preservation).** We reason by contradiction. Suppose there is a sum \( \sum_{i \in I} \lambda_i \cdot E_i \) appearing in \( \langle e \rangle_P \) such that \( \text{trigger}(\lambda_k) = \text{trigger}(\lambda_j) \) and \( \text{out}(\lambda_k) = \text{out}(\lambda_j) \), for some \( k, j \in I, k \neq j \). We proceed by case analysis on the structure of the property \( e \). Let us focus on the case \( e = \bigcup_{i \in I} \pi_i \). The other cases are simpler. Then, \( \langle e \rangle_P \) is equal to \( Z \), for
\[ Z = \sum_{i \in I} \langle \pi_i \rangle_P \rangle_P + \sum_{\alpha} \langle \alpha \rangle_P \rangle_P, \quad \text{if } \alpha \in \bigcup_{i \in I} \pi_i \]
\[ Z = \sum_{i \in I} \langle \pi_i \rangle_P \rangle_P + \sum_{\alpha} \langle \alpha \rangle_P \rangle_P, \quad \text{otherwise} \]
and \( Q = \mathcal{P} \setminus \left( \bigcup_{i \in I} \pi_i \cup \{\text{tick, end}\} \right) \). Since \( e \) is deterministic (Definition 5) it follows that \( \pi_h \neq \pi_i \), for any \( h, i \in I, h \neq i \). As a consequence, it cannot be \( \lambda_k = \pi_h < \text{end} \), for \( h \in I \), and \( \lambda_j = \pi_i < \text{end} \), for \( i \in I \), \( h \neq i \), because \( \text{out}(\lambda_k) = \pi_h \neq \pi_i = \text{out}(\lambda_j) \). Thus, the only chance for \( Z \) to be nondeterministic is that \( \lambda_k = \pi_h, h \in I \), and \( \lambda_j = \pi_i < \text{end} \), for \( i \in I \), in the case \( \text{end} \notin \bigcup_{i \in I} \pi_i \). However, this is not admissible because \( \text{end} \notin \bigcup_{i \in I} \pi_i \) implies \( \text{trigger}(\lambda_k) = \pi_h \neq \text{end} = \text{trigger}(\lambda_j) \).

\[ \square \]

In order to prove Theorem 1, we need prove that the cross product between edit automata satisfies a standard correctness result saying that any execution trace associated to the intersection of two regular properties is also a trace of the the cross product of the edit automata associated to the two properties, and vice versa.

**Lemma 4 (Correctness of Cross Product).** Let \( e_1, e_2 \in \mathcal{P}_{\tau \oplus \mathcal{G}} \) (resp., \( p_1, p_2 \in \mathcal{P}_{\tau \oplus \mathcal{L}} \)) and \( \mathcal{P} \) be a set of actions such that events \( (e_1 \cap e_2) \subseteq \mathcal{P} \) (resp., events \( p_1 \cap p_2 \subseteq \mathcal{P} \)). Then, it holds that:

- If \( t \) is a trace of \( \prod_X^\mathcal{P} (\langle e_1 \rangle_P, \langle e_2 \rangle_P) \) (resp., \( \prod_X^\mathcal{P} (\langle p_1 \rangle_P, \langle p_2 \rangle_P) \)), then \( \text{out}(t) \) is prefixed by some trace in the semantics \( \langle e_1 \cap e_2 \rangle \) (resp., \( \langle p_1 \cap p_2 \rangle, \langle p_1 \rangle_P \rangle_P \)).
- If \( t \) is a trace in \( \langle e_1 \cap e_2 \rangle \) (resp., \( \langle p_1 \cap p_2 \rangle \)) then there exists a trace \( t' \) of \( \prod_X^\mathcal{P} (\langle e_1 \rangle_P, \langle e_2 \rangle_P) \) (resp., \( \prod_X^\mathcal{P} (\langle p_1 \rangle_P, \langle p_2 \rangle_P) \)) such that \( \text{out}(t') = t \).

**Proof of Theorem 1 (Transparency).** We prove a stronger result. Let \( e \in \mathcal{P}_{\tau \oplus \mathcal{G}} \) be a global deterministic property and \( P \in \mathcal{C}_{\mathcal{I}_1} \) be a controller such that \( P \rightarrow J \), for some trace \( t = a_1 \cdots a_n \). If \( t \) is the prefix of some trace in the semantics \( \langle e \rangle \) then the following sub-results hold:

1. There exists a unique \( E \) such that \( \langle e \rangle_P \rangle_P \longrightarrow E \) where either \( E = \langle p' \rangle_P \rangle_P \) or \( E = Z \), with \( Z = \langle p' \rangle_P \rangle_P \), for some \( p' \in \mathcal{P}_{\tau \oplus \mathcal{L}} \) and some automaton variable \( X \).
2. There is a trace \( t' \in \langle p \rangle_P \rangle_P \) such that \( t \cdot t' \) is a prefix of some trace in \( \langle e \rangle \).
3. There is no trace \( t'' = a_1 \cdots a_k \cdot \lambda \) for \( \langle e \rangle_P \) such that \( 0 \leq k < n \) and \( \lambda \in \{ -a_{k+1}, \alpha < a_{k+1} \} \), for some \( \alpha \).

These three sub-results imply the required result. We proceed by induction on the length \( n \) of trace \( t \).

- **Base case: \( n = 1 \).** That is \( t = \alpha \), with \( \alpha \in \text{Sens} \cup \text{Chn}^* \cup \text{Act} \cup \{\text{tick, end}\} \). We proceed by induction on the structure of \( e \).

Case \( e \equiv p^* \), for some \( p \in \mathcal{P}_{\tau \oplus \mathcal{L}} \). We prove the following three results:
• i) there exists a unique $E$ such that $\langle p \rangle \vdash^\alpha_X \Pi' \rightarrow E$ and either $E = \langle p \rangle \Pi' \vdash^\alpha_X$ or $E = Z$, with $Z = \langle p' \rangle \Pi'_X \rightarrow$, for some $p' \in \Pi \tau \Pi \Pi \Pi$ and some automaton variable $X'$;

• ii) there is a trace $t' \in \Pi [p]$ such that $\alpha \cdot t'$ is a prefix of some trace in $[p]$;

• iii) there is no $\lambda \in \{ -\alpha, \alpha' < \alpha \}$ such that $\langle p \rangle \Pi'_X \rightarrow^\lambda F'$, for some $F'$.

As $\langle p \rangle \Pi [p] \equiv X$, with $X = \langle p \rangle \Pi'_X \rightarrow$, results i) and ii) and iii) imply the required facts (1) and (2) and (3) for $e = p^\Pi$. We proceed as follows: first, we prove items i) and ii) by induction on the structure of $p$, and then we prove item iii) by contradiction.

We prove items i) and ii). We focus on the most significant cases: $p = \bigcup_{\iota \in I} p_\iota, p_1 \equiv p_1 \cap p_2$. The other cases are similar or simpler.

Let $p \equiv \bigcup_{\iota \in I} p_\iota, p_1$. In this case, $\alpha$ is a prefix of some trace in $[p]$ and $\langle p \rangle \Pi'_X \rightarrow$ returns $Z'$, for

$$Z' = \left\{ \sum_{\iota \in I} \pi_\iota \cdot p_\iota \Pi'_X + \sum_{\iota \in I} \pi_\iota \cdot \langle \iota \rangle \Pi'_X + \sum_{\iota \in I} \pi_\iota \cdot -\alpha', \Pi' \cdot Z', \text{ if } \Pi \not\equiv \bigcup_{\iota \in I} \pi_\iota \right\}$$

where $Q = \Pi \setminus \left( \bigcup_{\iota \in I} \pi_\iota \cdot \{ \text{tick, end} \} \right)$. Since $\alpha$ is a prefix of some trace in $[p]$ and $\pi_\iota \not\equiv \varepsilon$, for any $\iota \in I$, and $e$ is deterministic, then we derive that $\alpha = \pi_k$, for a unique index $k \in I$.

• Let us prove i). Since $k$ is the unique index such that $\alpha = \pi_k$, we derive that $\langle p \rangle \Pi'_X \rightarrow^\alpha E$ is the unique transition labeled $\alpha$ such that either $E = \langle p \rangle p_k \Pi'_X$ or $E = Z_1$, with $Z_1 = \langle p \rangle p_k \Pi'_X$.

• Let us prove ii). Since $P \not\equiv J$ and $\alpha = \pi_k$, by inductive hypothesis there exists $t' \in [p_k]$ such that $\alpha \cdot t'$ is a prefix of some trace in $[\pi_k \cdot p_k]$, and hence also in $[p]$, as required.

Let $p \equiv p_1 \cap p_2$. In this case, we have that $\alpha$ is prefix of some trace in $[p]$ and the synthesis $\langle p \rangle \Pi'_X \rightarrow$ returns the edit automaton $E = \prod_X^\Pi \langle p \rangle \Pi'_X, \langle p \rangle \Pi'_X \Pi'_X$.

• Let us prove i). By definition of cross product in Table 6, the most interesting case is when

$$\langle p \rangle \Pi'_X = \sum_{\iota \in I} \lambda_\iota, E_\iota \text{ and } \langle p \rangle \Pi'_X = \sum_{\iota \in J} \phi_{\iota, J} F_{\iota, J}.$$  

In this case,

$$E = \prod_X^\Pi \langle p \rangle \Pi'_X, \langle p \rangle \Pi'_X \Pi'_X = \sum_{(\iota, j) \in H} (\lambda_\iota, X_{i,j} + v_j, X_{i,j}) + \sum_{\alpha \in Q} (-\alpha, Z),$$

for $X_{i,j} = \prod_{X_{i,j}} (E_i, F_j) \in Q = (\Pi \setminus \{ \text{tick, end} \}) \setminus \bigcup_{(i, j) \in I} (\lambda_\iota, v_j) \text{ and } H = \{(i, j) \in I \times J : \text{out}(\lambda_\iota) = \text{out}(v_j) \neq \tau \text{ and } \prod_{X_{i,j}} (E_i, F_j) = \sum_{\alpha \in \Pi \setminus \{ \text{tick, end} \}} (-\alpha, X_{i,j}) \}$. Now, since $\alpha$ is a prefix of some trace in $[p]$, then $\alpha$ is a prefix of some trace in both $[p_1]$ and $[p_2]$. Thus, since $P \rightarrow J$, by inductive hypothesis there exists a unique $E$ such that $\langle p \rangle \Pi'_X \rightarrow^\alpha E$ and, either $E = \langle p \rangle p_1 \Pi'_X$ or $E = Z_1$, with $Z_1 = \langle p \rangle p_k \Pi'_X$, for some $p_1 \in \Pi \tau \Pi \Pi \Pi$. Similarly, there exists unique $F$ such that $\langle p \rangle \Pi'_X \rightarrow^\alpha F$, and either $E = \langle p \rangle p_2 \Pi'_X$ or $F = Z_2$, with $Z_2 = \langle p \rangle p'_2 \Pi'_X$, for some $p'_2 \in \Pi \tau \Pi \Pi \Pi$. Since $\langle p \rangle \Pi'_X = \sum_{\iota \in I} \lambda_\iota, E_\iota$ and $\langle p \rangle \Pi'_X = \sum_{\iota \in J} \phi_{\iota, J} F_{\iota, J}$, then we have that there exist $i \in I$ and $j \in J$ such that $E = E_j$ and $F = F_j$. By Lemma 4 and by definition of cross product, we have that $(i, j) \in H, \alpha = \lambda_\iota$ and $E = \prod_{X_{i,j}} (E_i, F_j), \text{ with } X_{i,j} = \prod_{X_{i,j}} (E_i, F_j) = \prod_{X_{i,j}} (E_i, F_j)$. Thus, since $E$ and $F$ are unique, it follows that $E \rightarrow_X X_{i,j}$ is the only possible transition for $E_p$ with label $\alpha$. Finally, we have that $\prod_{X_{i,j}} (E, F) = \prod_X (\langle p \rangle p_1 \Pi'_X, \langle p \rangle p_2 \Pi'_X) = \langle p \rangle p_1 \cap p_2 \Pi'_X$, as required.

• Let us prove ii). As $E \rightarrow_X \prod_{X_{i,j}} (E, F) = \prod_X (\langle p \rangle p_1 \Pi'_X, \langle p \rangle p_2 \Pi'_X) = \langle p \rangle p_1 \cap p_2 \Pi'_X$, by Lemma 4 we derive that $\langle p \cap p \rangle \Pi' \not\equiv 0$. Thus, there exists $t' \in [p \cap p \Pi']$. Again, by Lemma 4 it follows that $E \rightarrow_X \prod_{X_{i,j}} (\langle p \rangle p_1 \Pi'_X, \langle p \rangle p_2 \Pi'_X) \rightarrow E'$, for some $E'$, with $\alpha \cdot t'$ prefix of some trace in $[p \cap p \Pi']$, as required.

We have proved items i) and ii), for any $p \in \Pi \tau \Pi \Pi \Pi$. It remains to prove item iii) namely, if $\langle p \rangle \Pi'_X \rightarrow E$ then there is no $\lambda \in \{ -\alpha, \alpha' < \alpha \}$ such that $\langle p \rangle \Pi'_X \rightarrow F$, for some $F$. By Lemma 1 we
have that $\not{\bowtie}_\alpha^\mathcal{P} \equiv E'$ for $\not{\bowtie}_\alpha^\mathcal{Q} \equiv Z$, with $Z = E'$ for $\alpha \in \mathcal{P}, Q = \mathcal{P} \setminus \{\cup \alpha_i \in \{\text{tick, end} \}\},$ and $E$ and $E''$ edit automata. Since $\not{\bowtie}_\alpha^\mathcal{P} \rightarrow E$.\[\text{for some } \lambda \in \{-\alpha, \alpha' < \alpha\} \text{ and automata } \mathcal{F}. \text{ Since } \alpha = \alpha_k, \text{ with } k \in I, \text{ we derive that } \alpha \notin \mathcal{Q} = \mathcal{P} \setminus \{\cup \alpha_i \in \{\text{tick, end} \}\},$ that is $\lambda$ is an insertion, $\lambda = \alpha' < \alpha$, for some $\alpha'$. As in $E'$ the only insertions are of the form $\alpha_i < \text{end}$, it follows that $\alpha = \text{end}$ and $\text{end} \notin \cup \alpha_i$. However, since $\text{end} \notin \cup \alpha_i$ it follows that $\alpha = \alpha_k \neq \text{end}$. Contradiction.

Case $e \equiv e_1 \cap e_2$, for some $e_1, e_2 \in \mathbb{P}_\mathbb{G}$. This case can be proved with a reasoning similar to that of the case $p_1 \cap p_2$.

- Inductive case: $n > 1$, for $n \in \mathbb{N}$. Suppose $P \rightarrow J$ such that $t$ is a prefix of some trace in $[e]$. Since $n > 1, P \rightarrow J$, for some trace $t'$ such that $t = t' \cdot \alpha$. As $t$ is a prefix of some trace $t'$ in $[e]$ then $t'$ is a prefix of some trace in $[e]$ as well. Thus, by inductive hypothesis we have that:

1. There exists a unique $E'$ such that $\not{\bowtie}_\alpha^\mathcal{P} \rightarrow E'$, and either $E' = \not{\bowtie}_\alpha^\mathcal{P}$ or $E' = Z$, with $Z = \not{\bowtie}_\alpha^\mathcal{P}$, for some $p' \in \mathbb{P}_\mathbb{G}$ and some automaton variable $X$.

2. There is a trace $t''$ in $[p']$ such that $t' \cdot t''$ is a prefix of some trace in $[e]$.

3. There is no trace $t''' = \alpha_1 \cdot \alpha_k \cdot \lambda$ for $\not{\bowtie}_\alpha^\mathcal{P}$ such that $0 \leq k < n - 1$ and $\lambda \in \{-\alpha_{k+1}, \alpha' < \alpha_{k+1}\}$, for some $\alpha'$. Since from (1) $E'$ is unique and either $E' = \not{\bowtie}_\alpha^\mathcal{P}$ or $E' = Z$, with $Z = \not{\bowtie}_\alpha^\mathcal{P}$, we have to prove: i) there exists a unique $E''$ such that $\not{\bowtie}_\alpha^\mathcal{P} \rightarrow E''$, and either $E'' = \not{\bowtie}_\alpha^\mathcal{P}$ or $E'' = Z$, with $Z = \not{\bowtie}_\alpha^\mathcal{P}$, for some $p'' \in \mathbb{P}_\mathbb{G}$ and some automaton variable $X'$; ii) there is a trace $t' \in [p'']$ such that $\alpha \cdot t'$ is a prefix of some trace in $[p'']$; iii) there is no $\lambda \in \{-\alpha, \alpha' < \alpha\}$, such that $\not{\bowtie}_\alpha^\mathcal{P} \rightarrow F$, for some $F$. These three facts can be proved as previously done for the base case, $n = 1$.

In order to prove Theorem 2 we need a couple of technical lemmata.

**Lemma 5 (Soundness of the Synthesis).** Let $e \in \mathbb{P}_\mathbb{G}$ be a global property and $\mathcal{P}$ be a set of observable actions such that $\text{events}(e) \subseteq \mathcal{P}$. Let $\not{\bowtie}_\alpha^\mathcal{P} \rightarrow \ldots \rightarrow \not{\bowtie}_\alpha^\mathcal{P} \rightarrow E$ be an arbitrary execution trace of the synthesised automaton $\not{\bowtie}_\alpha^\mathcal{P}$. Then,

1. for $t = \text{out}(\lambda_1) \cdot \ldots \cdot \text{out}(\lambda_n)$ the trace $t$ is a prefix of some trace in $[e]$;
2. either $E = \not{\bowtie}_\alpha^\mathcal{P}$ or $E = Z$, with $Z = \not{\bowtie}_\alpha^\mathcal{P}$, for some $p' \in \mathbb{P}_\mathbb{G}$ and some automaton variable $X$.

**Proof.** We proceed by induction on the length of the execution trace $\not{\bowtie}_\alpha^\mathcal{P} \rightarrow \ldots \rightarrow \not{\bowtie}_\alpha^\mathcal{P} \rightarrow E$. Base case: $n = 1$. In this case, $\not{\bowtie}_\alpha^\mathcal{P} \rightarrow E$. We proceed by induction on the structure of $e$.

Case $e = p^*$, for some $p \in \mathbb{P}_\mathbb{G}$. We prove by induction on the structure of $p$ the following two results: i) for $\beta = \text{out}(\lambda), \bar{\beta}$ is a prefix of some trace in $[p]$, and ii) either $E = \not{\bowtie}_\alpha^\mathcal{P}$ or $E = Z$, with $Z = \not{\bowtie}_\alpha^\mathcal{P}$, for some $p' \in \mathbb{P}_\mathbb{G}$ and some automaton variable $X$. As $p^* \mathcal{P} \equiv \mathcal{X},$ for $X = \not{\bowtie}_\alpha^\mathcal{P}$, results i) and ii) imply the required results (1) and (2), for $e = p^*$. We show the cases $p \equiv p_1 \cap p_2$ and $p \equiv p_1 \cap p_2$, the others cases are similar or simpler.

Let $p \equiv p_1 \cap p_2$, and $\not{\bowtie}_\alpha^\mathcal{P} \rightarrow E$. We prove the two results i) and ii) for $p \neq \epsilon$, the case $p_1 = \epsilon$ is simpler. By definition, $\not{\bowtie}_\alpha^\mathcal{P} \rightarrow \not{\bowtie}_\alpha^\mathcal{P}$ returns $\not{\bowtie}_\alpha^\mathcal{P} \rightarrow \not{\bowtie}_\alpha^\mathcal{P}$, for $Z' = \not{\bowtie}_\alpha^\mathcal{P}$, and $Z' \neq X$. As a consequence, from $p_1 \neq \epsilon$ and $\not{\bowtie}_\alpha^\mathcal{P} \rightarrow \not{\bowtie}_\alpha^\mathcal{P} \rightarrow E$ it follows that $\not{\bowtie}_\alpha^\mathcal{P} \rightarrow E_1$, for some $E_1$.

- Let us prove i). Since $\not{\bowtie}_\alpha^\mathcal{P} \rightarrow E_1$, by inductive hypothesis we have that $\bar{\beta}$ is a prefix of some trace in $[p_1]$. Thus, $\bar{\beta}$ is a prefix of some trace in $[p_1 \cap p_2]$, as required.
Let us prove ii). Again, since $\langle p_1 \prod_1 \rangle \xrightarrow{\lambda} E_1$, by inductive hypothesis either $E_1 = \langle q_1 \prod_1 \rangle$ or $E_1 = Z_1$, with $Z_1 = \langle q_1 \prod_2 \rangle$, for some $q_1 \in \mathcal{PTDL}$ and some automaton variable $Z'$. Let us analyse $E_1 = \langle q_1 \prod_1 \rangle$ (the case $E_1 = Z_1$, with $Z_1 = \langle q_1 \prod_2 \rangle$, is similar). As $E_1 = \langle q_1 \prod_1 \rangle$ with $Z' = \langle q_2 \prod_1 \rangle$, by definition of the synthesis algorithm it follows that $E_1 = \langle q_1 \prod_1 ; p_2 \prod_1 \rangle$, as required.

Let $p \equiv p_1 \cap p_2$ and $\langle p_1 \cap p_2 \prod_1 \rangle \xrightarrow{\lambda} E$. By definition, the synthesis algorithm applied to $\langle p_1 \cap p_2 \prod_1 \rangle$ returns $E = \text{Prod}(\langle p_1 \prod_1 \rangle, \langle p_2 \prod_1 \rangle)$. Let us prove the results i) and ii).

Result i) follows directly from Lemma 4.

Let us prove ii). By inspection of the definition of cross product in Table 6, the most interesting case is when $\langle p_1 \prod_1 \rangle = \sum_{i \in I} \lambda_i E_i$ and $\langle p_2 \prod_1 \rangle = \sum_{j \in J} v_j F_j$. In this case,

$$E_p = \text{Prod}(\langle p_1 \prod_1 \rangle, \langle p_2 \prod_1 \rangle) = \sum_{(i,j) \in H} (\lambda_i X_{i,j} \oplus v_j X_{i,j}) + \sum_{\alpha \in Q} -\alpha Z,$$

for $X_{i,j} = \text{Prod}_{X_{i,j}}(E_i, F_j)$ and $Q = (\mathcal{P} \setminus \text{tick}end) \setminus \bigcup_{(i,j) \in H} \{\lambda_i, v_j\}$ and $H = \{(i,j) \in I \times J : \text{out}(\lambda_i) \neq \text{out}(v_j)\} \neq \emptyset$ and $\text{Prod}_{X_{i,j}}(E_i, F_j)$ is defined for $\alpha \in Q$. We prove the result for the case (a); the case (b) can be proved in a similar manner. Since $\lambda \in \bigcup_{(i,j) \in H} \{\lambda_i, v_j\}$ we have that $\lambda = \lambda_i$ or $\lambda = v_j$, for some $i, j \in H$. By definition of cross product, it holds that $\langle p_1 \prod_1 \rangle \xrightarrow{\lambda} E_i$ and $\langle p_2 \prod_1 \rangle \xrightarrow{v_j} E_j$, with $\text{out}(\lambda_i) = \text{out}(v_j) = \text{out}(\lambda)$. Thus, by inductive hypothesis we have that: (1) either $E_i = \langle q_1 \prod_1 \rangle$ or $E_i = Z_1$, with $Z_1 = \langle q_1 \prod_2 \rangle$, for some $q_1 \in \mathcal{PTDL}$; (2) either $F_j = \langle q_2 \prod_1 \rangle$ or $F_j = Z_2$, with $Z_2 = \langle q_2 \prod_2 \rangle$, for some $q_2 \in \mathcal{PTDL}$. Therefore, by definition of cross product we derive that $\text{Prod}_{X_{i,j}}(E_i, F_j) = \text{Prod}(\langle p_1 \prod_1 \rangle, \langle p_2 \prod_1 \rangle)$. Finally, by definition of our synthesis it follows that $\text{Prod}(\langle p_1 \prod_1 \rangle, \langle p_2 \prod_1 \rangle) = \langle p_1 \prod_1 ; p_2 \prod_1 \rangle$, as required.

Case $e = e_1 \cap e_2$ for some $e_1, e_2 \in \mathcal{PTDG}$. This case can be proved with a reasoning similar to that seen in the proof of case $p_1 \cap p_2$. 

Inductive case: $n > 1$, for $n \in \mathbb{N}$. Suppose $\langle e \prod \rangle \xrightarrow{\lambda_1} \ldots \xrightarrow{\lambda_n} E$, for $n > 1$. $\langle e \prod \rangle \xrightarrow{\lambda_1} \ldots \xrightarrow{\lambda_n} E \xrightarrow{\lambda_n} E$. Thus, by induction, we have that:

1. for $t' = \text{out}(\lambda_1) \ldots \text{out}(\lambda_{n-1})$ the trace $t'$ is a prefix of some trace in $[e]$, and
2. either $E' = \langle q' \prod \rangle$ or $E' = Z$, with $Z = \langle q' \prod \rangle$, for some $q' \in \mathcal{PTDL}$ and some automaton variables $Z$ and $X$.

Since either $E' = \langle q' \prod \rangle$ or $E' = Z$, with $Z = \langle q' \prod \rangle$, then to conclude the proof it is sufficient to prove that given $\langle q' \prod \rangle \xrightarrow{\lambda_n} E$ and $\beta_n = \text{out}(\lambda_n)$, it holds that $\beta_n$ is a prefix of some trace in $[p']$. For that we resort to the proof of the base case.

In the next lemma, we prove that, given the execution traces of a monitored controller, we can always extract from them the traces performed by its edit automaton and its monitored controller in isolation.

**Lemma 6 (Trace Decomposition).** Let $E \in \mathcal{Edit}$ be an edit automaton and $J \in \mathcal{Ct1}$ be a controller. Then, for any execution trace $E_0 \Rightarrow \{J_0\} \xrightarrow{\beta_1} \ldots \xrightarrow{\beta_n} E_n \Rightarrow \{J_n\}$, with $E_0 = E$ and $J_0 = J$, it hold that (1) $E_{i-1} \xrightarrow{\lambda_i} E_i$, with $\beta_i = \text{out}(\lambda_i)$, and (2) either $J_{i-1} \xrightarrow{\alpha_i} J_i$, with $\alpha_i = \text{trigger}(\lambda_i)$, or $J_i = J_{i-1}$, for $1 \leq i \leq n$.

**Proof.** The transition $E_{i-1} \Rightarrow \{J_{i-1}\} \xrightarrow{\beta_i} E_i \Rightarrow \{J_i\}$, for $1 \leq i \leq n$, can be only derived by applying one of the following rule: (Allow), (Insert), (Suppress). In the case of an application of rule (Allow), $E_{i-1} \xrightarrow{\alpha_i} E_i$ and $J_{i-1} \xrightarrow{\alpha_i} J_i$ with $\beta_i = \alpha_i = \lambda_i$. Hence,
out(\lambda_i) = trigger(\lambda_i) = a_i, as required. In the case of rule (Insert), \( E_{i-1} \triangleright \{ j_{i-1} \} \xrightarrow{\beta_i} E_i \triangleright \{ j_i \} \) derives from \( E_{i-1} \xrightarrow{\alpha_i} E_j \) and \( j_{i-1} \xrightarrow{\alpha_i} j_i \), for some \( \alpha_i = \alpha \). Thus, \( out(\lambda_i) = out(\alpha < \alpha_i) = \beta_i \) and \( j_{i-1} = j_i, as required. Finally, in the case of rule (Suppress), \( E_{i-1} \triangleright \{ j_{i-1} \} \xrightarrow{\beta_i} E_i \triangleright \{ j_i \} \) derives from \( E_{i-1} \xrightarrow{\alpha_i} E_i \) and \( j_{i-1} \xrightarrow{\alpha_i} j_i \), for some \( \alpha_i \), with \( \beta_i = \tau \) and \( \lambda_i = \neg a_i \). Hence, \( out(\lambda_i) = \tau \) and trigger(\lambda_i) = a_i, as required.

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**Proof of Theorem 2 (Soundness).** Let \( t = \beta_1 \cdot \ldots \cdot \beta_n \) be a trace s.t. \( \langle e \rangle^P \triangleleft \{ P \} \xrightarrow{t} E \triangleleft \{ J \} \), for some \( E \in E_{\text{dict}} \) and some controller \( J \). By an application of Lemma 6 there exist \( E_i \in E_{\text{dict}} \) and \( \lambda_i \), for \( 1 \leq i \leq n \), such that: \( \langle e \rangle^P \xrightarrow{\lambda_1} E_1 \xrightarrow{\ldots} \lambda_n \xrightarrow{E_n} E = \text{with} \beta_1 = out(\lambda_1). Thus, \( t = out(\lambda_1) \cdot \ldots \cdot out(\lambda_n) \). By Lemma 5, \( t \) is a prefix of some trace in \([e]\), as required.

**Lemma 7 (Deadlock-freedom of the synthesis).** Let \( e \in P \circ P G \) be a global property and \( P \) be a set of observable actions s.t. events(e) \( \subseteq \mathcal{P} \). Then the edit automaton \( \langle e \rangle^P \) does not deadlock.

**Proof.** Given an arbitrary execution \( \langle e \rangle^P \xrightarrow{\lambda_1} \ldots \xrightarrow{\lambda_n} E \), the proof is by induction on the length \( n \) of the execution trace. By an application of Lemma 5 we have that either \( E = \langle p \rangle^X \) or \( E = Z \), with \( Z = \langle p \rangle^X \), for \( p \in P \circ P \mathbb{L} \) and some automaton variable \( X \). Hence, the result follows by inspection of the synthesis function of Table 5 and by induction on the structure of \( p \).

**Proof of Theorem 3 (Deadlock-freedom).** Let \( t \) be a trace such that \( \langle e \rangle^P \triangleleft \{ P \} \xrightarrow{t} E \triangleleft \{ J \} \), for some edit automaton \( E \) and controller \( J \). By contradiction we assume that \( E \triangleleft \{ J \} \) is in deadlock. Notice that, by definition, our controllers \( J \) never deadlock. By Lemma 7 the automaton \( \langle e \rangle^P \) never deadlock as well. Consequently, we have that for any transition \( J \xrightarrow{\alpha} J' \) there is no action \( \lambda \) for \( E \), such that the monitored controller \( E \triangleleft \{ J \} \) may progress according to one of the rules: (Allow), (Suppress) and (Insert). By an application of Lemma 5, we have that either \( E = \langle p \rangle^X \) or \( E = Z \), with \( Z = \langle p \rangle^X \), for some \( p \in P \circ P \mathbb{L} \) and some automaton variable \( X \). Now, by Lemma 1, we have that

\[
\langle p \rangle^X \triangleleft \{ \alpha_i \} E_i \xrightarrow{\sum \alpha_i < \text{end.} E_i + \sum \neg \text{-} \alpha.F \text{ if end } \notin \cup \alpha_i E_i + \sum \neg \text{-} \alpha.F \text{ otherwise.} \}
\]

for \( \alpha_i \in \mathcal{P}, Q = \mathcal{P} \setminus \{ (\cup \alpha_i) \cup \{ \text{tick, end} \} \}, \) and \( E_i \) and \( F \) edit automata. In both the cases \( \langle p \rangle^X \) may only deadlock the enforcement when the controller may only perform \( \text{tick}-\)actions. From this fact, we derive \( J = \text{tick}^h.S \), for \( 0 < h \leq k \). Since \( \text{tick}-\)actions cannot be suppressed, we have that \( t = t' \cdot \text{tick}^{k-h} \), for some possibly empty trace \( t' \) terminating with an end. By an application of Theorem 2, \( t = t' \cdot \text{tick}^{k-h} \in [e] \). And since \( e \) is \( k \)-sleeping we derive \( p = \text{tick}^k.p' \), for some \( p' \). Since \( \langle e \rangle^P \) is sound (Lemma 5) we derive that \( E = \langle p \rangle^X = \langle \text{tick}^k.p' \rangle^X \). Finally, \( h > 0 \) implies \( E \xrightarrow{\text{tick}} E' \), for some \( E' \), in contradiction with what stated four lines above.

**Proof of Theorem 4 (Divergence-freedom).** Let \( e \in P \circ P G \) be a global property in its general form, given by the intersection of \( n \geq 1 \) global properties \( p_i^* \cap \ldots \cap p_n^* \), for \( p_i \in \mathbb{LP} \), with \( 1 \leq i \leq n \). As \( e \) is well-formed, according to Definition 4 also all local properties \( p_i \) are well-formed. This means that they all terminate with an \( \text{end} \) event. Thus, in all global properties \( p_i^* \), for \( 1 \leq i \leq n \), the number of events within two subsequent \( \text{end} \) events is always finite. The same holds for the property \( e \). Now, let \( t \) be an arbitrary trace such that \( \langle e \rangle^P \triangleleft \{ P \} \xrightarrow{t} E \triangleleft \{ J \} \), for some edit automaton \( E \) and controller \( J \). And let \( k = \max_{1 \leq i \leq k} k_i \), where \( k_i \) is the length of the longest trace of \([p_i]\), for \( 1 \leq i \leq n \). Thus, if \( E \triangleleft \{ J \} \xrightarrow{t} E' \triangleleft \{ J' \} \), with \( |t'| \geq k \), and since by Theorem 2 we have that \( t \cdot t' \) is a prefix of some trace \([e]\), then \( \text{end} \in t' \).

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