Cryogenic Characterization and Modeling of Standard CMOS down to Liquid Helium Temperature for Quantum Computing

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Abstract. Cryogenic characterization and modeling of 0.18\textmu m CMOS technology (1.8V and 5V) are presented in this paper. Several PMOS and NMOS transistors with different width to length ratios (W/L) were extensively characterized under various bias conditions at temperatures ranging from 300K down to 4.2K. We extracted their fundamental physical parameters and developed a compact model based on BSIM3V3. In addition to their I-V characteristics, threshold voltage ($V_{th}$) values, on/off current ratio, transconductance of the MOS transistors, and resistors on chips are measured at temperatures from 300K down to 4.2K. A simple subcircuit was built to correct the kink effect. This work provides experimental evidence for implementation of cryogenic CMOS technology, a valid industrial tape-out process model, and promotes the application of integrated circuits in cryogenic environments, including quantum measurement and control systems for quantum chips at very low temperatures.

Keywords: Cryogenic electronics, MOSFETs, characterization, modeling, threshold voltage, kink effect, liquid helium temperature.
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1. Introduction

Cryogenic electronics have good prospects in application ranging from space exploration to infrared focal plane array [1–3], and has been studied for use in quantum computing in recent years [4–7]. A quantum computer comprises a quantum processor and a classical electronic control system [8]. The quantum processor works in a dilution refrigerator at deep-cryogenic temperatures down to the millikelvin range (Fig. 1), while the electronic readout and control system is implemented using room-temperature (RT) laboratory instruments [9,10]. The requirements for wiring between the cryogenic quantum processor and the RT readout controller are becoming more expensive and less reliable as quantum chips become increasing complexed and highly integrated [5]. Cryogenic complementary metal-oxide-semiconductor (Cryo-CMOS) technology can greatly reduce the thermal noise caused by non-ideal long signal lines and improve the signal-to-noise ratio and sensitivity of the quantum chip signals. Obtaining purer quantum control and readout signals with low delay efficiently improves quantum chip performance. Quantum Processors work in dilution refrigerators with maximum effective cooling powers of several hundreds $\mu$W. This constraint is relaxed at the liquid helium temperature (LHT) 4.2K, where moderate power dissipation is tolerable. Fig. 2 shows the future quantum interface using Cryo-CMOS technology, we need to implement ADC (Analog Digital Converter), DAC (Digital Analog Converter), oscillator, FPGA (Field Programmable Gate Array), and other integrated circuits at cryogenic temperatures. Unfortunately Cryo-CMOS faces several challenges, including the power limitation of refrigerators, and interconnection, packaging and device modeling [11–13].

The first problem to solve when designing Cryo-CMOS circuits is transistor modeling. SPICE model act as a bridge between device characteristics and IC design. BSIM3 [14], which is an industry-standard model, is valid from 230K to 430K for submicron processes. However, MOSFET characteristics change at lower temperatures because of freeze-out effect, which has led to a requirement for SPICE model development for cryogenic temperatures [15–20]. Previous work has demonstrated that CMOS technologies have been characterized at temperatures down to 4K [21–23]. However, BSIM model parameters have only been extracted down to 77K, and no systematic modeling of PMOS and NMOS devices with different width-to-length ratios are performed under different bias conditions at lower cryogenic temperatures, to the best of our knowledge [1,24–27].

In this paper, characterization of SMIC 0.18 $\mu$m CMOS transistors and a compact SPICE model based on BSIM3v3 [14] are presented from 300K down to 4.2K. It is an aluminum interconnect process, compared with copper, aluminum has better electrical properties at low temperatures [28, 29]. Temperature-dependent parameters are revised at 4.2K and the model shows good agreement with measurement results. The 0.18 $\mu$m process $V_{th}$ and resistance of active area are measured from 300K to 4.2K for the first time. This work is the first BSIM SPICE model range down to 4.2K for standard CMOS technology; the model can be applied directly to device and circuit electronic design automation (EDA) simulations.
2. Measurement Setup

Measurements of CMOS transistors with two different oxide thicknesses and a wide range of device sizes were performed, as shown in Table 1. The sample chips were first pasted and wire bonded to chip-carriers using Al-wire bonds (Fig. 3(a)). These chip-carriers were then immersed in liquid nitrogen (77 K) and liquid helium (4.2 K) using a dipstick. A schematic of the cross-section of the setup is shown in Fig. 3(c). The dipstick consists of a 1.8m steel pipe with a breakout box for cables placed at the top end and two dual in-line package(DIP) lock sockets at the lower end of the pipe. In total, 36 cables (enamel insulated wire) are used for the DC connections, including four cables for the temperature sensor. The temperature sensor is a Rh-Fe thermometer with a 1.2K-325K measurement range. The cable resistance is 0.3-0.4Ω, it is negligible compared with the resistance of MOSFET which is several hundreds or thousands ohms. Because the pipe can move up and down through a vacuum flange, the temperature can be shifted from 4.2K in the liquid phase to approximately 250K in the helium vapour at the top of the Dewar.

Table 1. SUMMARY OF CHARACTERIZED DEVICES

| Technology | SMIC 0.18um Bulk CMOS Process |
|------------|-------------------------------|
| Oxide      | Thin(3.6nm) Thick(11.9nm)     |
| Norminal Voltage | 1.8V 5V                      |
| Type       | NMOS  PMOS NMOS  PMOS         |
| W/L[um/um] | 100/0.18 100/0.18 100/0.6 100/0.5 |
|            | 10/10 10/10 10/10 10/10       |
|            | 10/0.6 10/0.6 10/2 10/2       |
|            | 10/0.2 10/0.2 10/0.65 10/0.55 |
|            | 10/18 10/18 10/0.6 10/0.5    |
|            | 10/16 10/16 10/0.5 10/0.45   |
|            | 0.22/0.18 0.22/0.18 0.3/0.6 0.3/0.5 |

All the MOSFET electrical measurements were performed using a Keysight B1500A semiconductor device analyzer, as shown in Fig. 3(b). For the thin-oxide NMOS, we measured transfer characteristics in both linear (drain-source voltage $V_{DS} = 50$ mV) and the saturation regions ($V_{DS} = 1.8V$) under various substrate bias voltages, along with the output characteristics under zero substrate bias(bulk-sourc voltage$V_{BS}=0V$) and reverse bias voltage($V_{BS}=-1.8V$) for various gate voltages($V_{GS}$). For the thick-oxide MOS, bias condition were increased to 5V; while for PMOS, the bias conditions were reversed. The resistance measurements were performed using a Keysight 3458A Digital Multimeter with 8½ Digit precision.

3. Characterization

The characteristics of CMOS transistors at different cryogenic temperatures are shown in Fig. 4. As shown in Fig. 4(b) and Fig. 4(c), threshold voltage increases as temperature decreases because of carrier freeze-out in the MOSFET channel region and thus a higher gate drive voltage is required to inject carriers into the channel region. $V_{th}$ varies approximately linearly with temperature, especially in the PMOS. Impurity freeze-out becomes important for temperature lower than 150K for shallow-energy-level dopants. At liquid nitrogen temperature, weak freeze-out takes place, which is mainly annoying for lightly doped drain (LDD) devices. At very low temperatures (<10 K), donor or acceptor impurities currently used to dope the semiconductor are fully frozen-out, at liquid helium temperature, practically no carriers remain in the bands if no field is applied [17-20].

Fig. 4(a) shows that $I_{DS}$ increases as temperature decreases, because the series resistance decreases as shown in Fig. 4(f), and mobility increase at cryogenic temperatures [12]. In low impurity concentration situations, such as p-well, the resistivity decreases due to an increase of mobility down to liquid nitrogen temperature [24]. However, carrier freeze-out causes a steep increase in n-well resistivity at liquid helium temperature. Other resistances drop with decreasing temperature down to liquid helium temperature. The resistance of the salicide’s heavy-doped N/P active area is reduced by 2/3 when compared with the RT value. The resistance of the unsalicide’s heavy-doped N active area is reduced by 1/3 when compared with the...
Figure 4. (a): $I_{DS}-V_{DS}$ curves at different cryogenic temperatures of thin-oxide NMOS, $V_{DS}=0V \rightarrow 1.8V$, $W/L=10\mu m/10\mu m$, $V_{GS}=1.8V$, $V_{BS}=0V$. (b): $I_{DS}-V_{GS}$ curves at different cryogenic temperatures of thin-oxide NMOS, $V_{DS}=0V \rightarrow 1.8V$, $W/L=10\mu m/10\mu m$, $V_{DS}=0.05V, V_{BS}=0V$. (c): $V_{th}$ of CMOS transistors at different cryogenic temperatures. (d): $G_{m}$ of MOSFETs at different cryogenic temperatures. (e): $G_{m}$ of MOSFETs at different cryogenic temperatures. (f): resistors on chip at different cryogenic temperatures, the six lines from top to bottom are N++ salicide area, W/L=2\mu m/100\mu m; P++ salicide area, W/L=2\mu m/100\mu m; Al metal square, 0.23\mu m*0.23\mu m*10000; N+ poly salicide, W/L=0.18\mu m/100\mu m; N Well in STI, W/L=20\mu m/100\mu m; Unsalicide N+, W/L=2\mu m/100\mu m
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Figure 5. I_{DS}-V_{GS} curves (a,b,e,f) and I_{DS}-V_{DS} curves (c,d,g,h) of thin-oxide NMOS at LHT. Device size (W/L) is 10\mu m/10\mu m. (a)-(d): before extraction, (e)-(h): extraction results, measured data: dashed lines; simulated data: solid lines. (a),(e): V_{BS}=0V\rightarrow-1.8V, V_{DS}=0.05V; (b),(f): V_{BS}=0V\rightarrow-1.8V, V_{DS}=1.8V; (c),(g): V_{GS}=0V\rightarrow1.8V, V_{BS}=0V; (d),(h): V_{GS}=0V\rightarrow1.8V, V_{BS}=-1.8V.

RT value. In particular, Aluminum resistance drops drastically because of reduced lattice vibrations. This gives a great advantage to reducing noise caused by CMOS switching and power-supply line resistances. This is an advantage of Cryo-CMOS technology compared with RT CMOS technology.

The kink effect at the LHT is shown in Fig. 6 and is caused by the LDD freezing out and substrate freeze-out. Impurity ionization will decrease as temperature decreases, especially in the light-doped regions near the source and drain. When the source-drain voltage becomes very high, impurity ionization will be activated to restrain the freeze-out effect under strong electric fields, CMOS transistors turn on for the second time [16]. This freezing effect causes the source-drain parasitic resistance to decrease and then turn to normal. The second reason is the substrate freeze-out, since at very low temperatures the MOS structure has a type of floating substrate potential within the depletion region. Although the applied substrate voltage on the backside of the device is fixed, the depletion region is in a floating state. In this structure, the majority carrier current (substrate current) cannot reach the substrate contact and thus flows through the substrate to the source. Due to the increase of the majority carrier current with increasing drain voltage, flowing through the substrate to the source at increasing drain voltage, this substrate potential within the depletion region increases and causes a decrease of the threshold voltage, for sufficient drain voltage. Therefore, at very low temperature, we obtain an excess drain current which creates a kink in the current-drain voltage characteristics [18]. Additionally, the measured saturation current value is less than the simulated value of BSIM3v3 model because of the channel freeze-out effect (Fig. 5(a-d)).

Ion to Ioff ratio (turn-on current and turn-off current ratio) is a typical parameter for MOSFET in digital integrated circuits. Ion to Ioff ratio maintains high value at cryogenic temperatures as shown in Fig. 4(d). The standard process CMOS can work well as a switch at low temperatures for digital circuits with low static power consumption, which is of great significance to the limited cooling power. Gate transconductance(G_m) indicates the gate-to-source current control capability. G_m increases when temperature increases (Fig. 4(e)), increase of G_m will supply wider bandwidth for the same power budget. Hence, MOS can work in analog circuits if it is modeling accurate.

4. Modeling

BSIM3 is a semi-empirical but accurate compact model for submicron process. We continue to adopt BSIM’s mode and use semi-empirical methods to modeling CMOS device at very low temperatures. Our object is to extend the BSIM model in submicron process to cryogenic temperatures, focus on the accuracy of the model. Fitting errors between simulation with default parameters and LHT measured data are generally higher than 60% under all bias conditions (Fig. 5(a-d)), while the BSIM3v3 model achieves a good degree of fitting at RT. First, the extraction procedure is performed using BSIMProPlus. The extraction process performed in the following procedure is based on physical understanding of the model and local optimization. The procedure can be described as
Figure 6. Cryogenic kink correction. (a)-(l): $I_{DS}$-$V_{DS}$ curves of CMOS at LHT. Device size (W/L): (a)-(d) thin-oxide NMOS 10µm/0.16µm, (e)-(h) thick-oxide NMOS 10µm/10µm, (i)-(l) thick-oxide NMOS 10µm/10µm. (a)-(b), (e)-(f), (i)-(j): before kink correction, (c)-(d), (g)-(h), (k)-(l): kink correction results. Measured data: dashed lines, simulated data: solid lines. (a), (c): $V_{GS}$=0V→1.8V, $V_{BS}$=0V; (b), (d): $V_{GS}$=0V→1.8V, $V_{BS}$=-1.8V; (e), (g): $V_{GS}$=0V→5V, $V_{BS}$=0V; (f), (h): $V_{GS}$=0V→5V, $V_{BS}$=-4V; (i), (k): $V_{GS}$=0V→5V, $V_{BS}$=0V; (j), (l): $V_{GS}$=0V→5V, $V_{BS}$=4V. (m) Sub-circuit resistance of thin-oxide MOSFET versus $V_{DS}$ at LHT, W/L=10µm/0.16µm. (n) Sub-circuit resistance of thick-oxide NMOSFET versus $V_{DS}$ at LHT, W/L=10µm/10µm. (o) Sub-circuit resistance of thick-oxide PMOSFET versus $V_{DS}$ at LHT, W/L=10µm/10µm. (p) Schematic representation of sub-circuit model.
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### Table 2. MODEL PARAMETERS

| Oxide | Thin(3.6nm) | Thick(11.9nm) |
|-------|-------------|---------------|
|       | Nominal Voltage |  |               |
|       | 1.8V | 5V |
| Type   | NMOS | PMOS | NMOS | PMOS |
| Temperature[K] | 300K | 77K | 4.2K | 300K | 77K | 4.2K | 300K | 77K | 4.2K | 300K | 77K | 4.2K |
| Vth0[V] | 0.39 | 0.4671 | 0.296 | -0.607 | -0.5785 | -0.4598 | 0.724 | 1.1391 | 0.31124 | -0.834 | -1.2 | -1.0532 |
| K1 [V⁻¹] | 0.680104 | 0.53197 | 0.696 | 0.87354 | 0.89101 | 0.90354 | 0.8768 | 0.80426 | 0.015 | 0.076605 | 0.00935 |
| K2 | -0.04998 | -0.00013 | -0.00013 | -0.04666 | -0.05506 | -0.0534 | -0.015 | -0.00686 | 0.01878 | 0.0626 | 0.09653 | 0.035749 |
| u0 [cm²/V·s] | 340 | 606.51 | 116.09 | 0.0085 | 0.015369 | 0.000933 | 0.04415 | 0.36688 | 0.00426 | 0.015 | 0.076605 | 0.0035 |
| ua [m/V] | -1E-09 | -4.4E-12 | -4.5E-12 | 2.5E-10 | 2.4E-10 | 3.52E-10 | -3.7E-10 | 1.11E-10 | 3.79E-10 | 2.27E-09 | 8.07E-09 | 4.84E-09 |
| ub [(m/V)²] | 0.236667 | 1.12E-17 | 6.46E-18 | 9.29E-19 | 9.29E-19 | 8.37E-19 | 2.6E-18 | 5.55E-18 | 5.65E-18 | 2.51E-20 | -3.6E-21 | -4.5E-19 |
| uc [1/V] | 1.2E-10 | 3.33E-13 | 3.33E-13 | -7.2E-11 | -1E-10 | -1.7E-10 | 8.38E-11 | 8.48E-12 | 1E-12 | -7.6E-11 | -3E-10 | -4.9E-10 |
| Dvt0 | 1.3 | 0.2165 | 5 | 1.03 | 3.0999 | 4.5143 | 7.46 | 7.46 | 7.46 | 2.8982 | 2.0023 | 26.374 |
| Dvt1 | 0.577164 | 2.3925 | 5 | 0.35 | 0.48288 | 0.14103 | 0.805 | 0.805 | 0.805 | 0.6 | 0.21882 | 0.46447 |
| uc1/V | 0.32 | 0.73655 | 0.1485 | 0.3024 | 0.39778 | 0.65873 | 0.15 | 0.15 | 0.036746 | 0.0655 | 0.006383 | 0.002047 |
| Keta [1/V] | -0.003 | -3.6E-05 | -3.6E-05 | -0.0389 | -0.03197 | 0.05346 | -0.0015 | -0.0015 | -0.00169 | 0.015 | 0.00094 | 0.0013 |

### Table 3. RMS ERROR

| Oxide | Thin(3.6nm) | Thick(11.9nm) |
|-------|-------------|---------------|
|       |  |  | W/L=10µm/0.16µm | W/L=10µm/10µm |
| Default | Revised | Corrected | Default | Revised | Corrected |
| thin-oxide NMOS | 13.37% | 5.74% | 1.71% | 8.94% | 5.71% | 2.41% |
| thick-oxide NMOS | 25.72% | 5.77% | 4.66% | 27.54% | 6.12% | 1.67% |
| thick-oxide PMOS | 174.15% | 4.41% | 1.41% | 58.19% | 3.25% | 0.96% |

*a for thin-oxide NMOS, VBB=−1.8V; for thick-oxide NMOS, VBB=−4V; for thick-oxide PMOS, VBB=−4V.

follows: 1) extract threshold voltage parameters such as $V_{th0}$, $K_1$, $K_2$ through large size device (large W&L); 2) extract carrier mobility parameters such as $\mu_0$, $\mu_a$, $\mu_b$, $\mu_c$ through large size device (large W&L); 3) extract short-channel effect parameters such as $Dv0$, $Dvt1$, $Dvt2$, $Nfactor$ through one set of devices (large and fixed W different L); 4) extract saturation velocity parameters such as $v_{sat}$ through one set of devices (large and fixed W& different L); 5) extract bulk effect parameters such as $a_0$, $ag$ through one set of devices (large and fixed W& different L) [14]. The model parameters are shown in Table 2. The root-mean-square (RMS) error is introduced to estimate the deviation between the results from the measurements and simulations. The RMS error is given by equation (1)

$$ \text{RMS Error} = \sqrt{\frac{1}{N} \sum_{i=1}^{n} \left( \frac{I_{mi} - I_{si}}{I_{th}} \right) \times 100} \quad (1) $$

The value of the threshold current $I_{th}$ can be set appropriately to obtain meaningful results. In this case, $I_{th}$ has been set to the maximum measured value according to BSIMProPlus. After the parameters have been changed appropriately, the RMS error between the simulation results and the test data improves to around 6% (Fig. 5(e-h), Table 3).

However, deviations caused by the kink effect still exist in some devices (Fig. 6(a,b,e,f,i,j)) at LHT. We connected a resistor in series with the substrate to improve the fitting precision as shown in Fig. 6(p), the MOSFET represents the BSIM model with cryogenic parameters and the resistor represents the freeze-out effect in the LDD region and substrate. The resistor value was extracted via Matlab using a polynomial fitting method. The characteristic of the non-linear resistor is shown in Fig. 6(m,n,o). Fig. 6(c,d,g,h,k,l) show the corrected sub-circuit simulation results. Good agreement with the DC measurements was achieved for devices over the entire voltage range at 4.2K as the RMS errors are summarized in Table 3.

### 5. Conclusion

A cryogenic study of SMIC 0.18µm 1.8V/5V CMOS technology down to 4.2K has been presented. We performed a relatively simple apparatus for executing the cryogenic measurements. A compact model based on BSIM3v3 has been proposed to optimize the deviation between measurement results and

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simulations using default parameters. $V_{th}$, Ion to Ioff ratio, $G_{m_{max}}$ and resistors on chip were tested down to 4.2K. Using the resulting database and SPICE model, we can design and simulate integrated circuits for cryogenic applications including quantum computer readout and control systems.

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