PSPICE compact model for power MOSFET based on manufacturer datasheet

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Abstract. In this paper, large signal model for power MOSFET devices is presented. The proposed model includes quasi-saturation effect and describes accurately the electrical behavior of the power MOSFET devices. The large signal model elements will be provided based on the device structure. Furthermore, the model parameters are extracted from measurements considering the voltages depending effect of the nonlinear gate-source, gate-drain and drain-source interelectrode capacitances. Excellent agreements will be shown between the simulated and the datasheet data. Finally, a description of the model will be provided along with the parameter extraction procedure.

1. Introduction
In power electronic circuits, power MOSFET device is widely used thanks to its high input impedance, high switching speed and thermal stability. To sustain high voltage in the off state, the power MOSFET structure contains a thickness and lowly doped drift layer, see Figure 1. In the on state, the extended-drain drift layer turns into high resistance in case of high voltage power MOSFETs [1]. Consequently, the standard power MOSFETs are limited to low voltage applications. The power MOSFETs present two important effects: the quasi-saturation effect [2]–[4] and the capacitive gate-drain effect. Quasi-saturation is observed in output characteristics of power MOSFET as the compression of the drain current curves at high gate voltages. At quasi-saturation regime, the drain current becomes less sensitive to the increase of gate voltage. This phenomenon is due to the carrier velocity saturation in the drift layer [2]–[4]. In other word, the intrinsic accumulation regions between the P-sources introduce gate-drift capacitance limiting the dynamic performance of the power MOSFETs. Therefore, the modeling of the power MOSFET must take into consideration the peculiar characteristics of the power MOSFET structure.

The intrinsic drift layer and the mobility degradation, in accumulation and inversion layers at the surface of silicon [5], make the modeling of power MOSFET more complex. SPICE power MOSFET models must describe accurately the electrical behavior of the device in all bias conditions. In addition, the model must be simple, fast and accurate without any problem of convergence. In literature, various models for power MOSFET were proposed [6]–[16]. These models use a subcircuit consisting of an equivalent circuit of the power MOSFET structure. The subcircuit combines a traditional MOSFET transistor, representing the channel region, with resistances, capacitors and dependent/independent current/voltage sources to model the electrical behavior of the power MOSFET. However, most of these models need proprietary tools to set their parameters or uses constant capacitance to model the gate-source capacitance $C_{GS}$.
A compact improved dynamic model for power MOSFET is presented in this paper. The proposed model is simple and takes into consideration the quasi-saturation effect and the nonlinear interelectrode capacitances. In this model, $C_{GS}$ is modeled by using the Meyer’s simplified capacitance model. The model parameter extraction procedure uses the datasheet data to determine the model parameters. The model features excellent agreement between the simulated and datasheet curves in all regions of operation of the power MOSFET.

In this work, the device samples used to validate the model are the STP36NF06L N-channel standard power MOSFET and the HUF76419S3ST_F085 N-channel trench power MOSFET [17]. For this purpose, section 2 describes the equivalent circuit model with the model’s equations. Section 3 is devoted to the procedure of parameter extraction and section 4 describes the static and dynamic simulation results obtained with the model compared to measurements.

Figure 1. Conventional power MOSFET structure with origin of its subcircuit elements.

2. Model description

Figure 1 shows the power MOSFET structure with the origin of its equivalent circuit. The proposed model is shown in Figure 2. This model uses standard MOSFET to model the channel region in series with JFET to model the drift region [18]. One “effective” gate voltage is added to equivalent circuit to take into account the small variation of the drain current with the gate voltage at the quasi-saturation regime [18]. The Dbody diode represents the intrinsic P-source/N-drift/N+-substrate diode. This diode is very useful because it will be used to take into consideration the breakdown voltage of the power MOSFET by the “BV” SPICE diode parameter, the drain-source interelectrode capacitance $C_{DS}$ and the forward behavior in the case of negative drain-source voltage. The parasitic gate-source capacitance $C_{GS}$ is divided to two capacitances in parallel:

1) The constant capacitance $C_{rs}$ equivalent to the overlap of the gate electrode over the N$^+$ source region plus the capacitance between the gate and source metallizations $C_m$.

2) The nonlinear channel capacitance between the gate and the P-body source $C_{GSB}$.

The nonlinear Miller gate-drain capacitance $C_{GD}$ is added to complete the dynamic model. As shown in Figure 1, $C_{GD}$ is equivalent to the constant oxide capacitance $C_{GDO}$ in series with the depletion capacitance $C_{GDdep}$.


2.1. Static behavior Modeling

The static model is obtained by the channel MOSFET, the JFET transistor, the “effective” gate voltage \( V_{\text{eff}} \) and the Dbody diode, as shown in Figure 2. In this model, the drain current depends on a critical gate voltage \( V_{GSC} \) which is extracted from the \( I_{DS}-V_{GS} \) curve as shown in Figure 3. \( V_{GSC} \) is the value of \( V_{GS} \) at the peak value of the transconductance parameter \( G_m \). For \( V_{GS} \leq V_{GSC} \) the drain current is governed by the channel MOS transistor while for \( V_{GS} > V_{GSC} \) the drain current is governed by the JFET transistor [18]. The expression of the channel drain current is based on the \( n \)th power law MOSFET model [19], [20]:

\[
I_n = \begin{cases} 
0 & \text{if } V_n \leq V_{ns} \\
I_n \left(1 + \lambda_n V_n\right) \left(2 - \frac{V_n}{V_{ns}}\right) & \text{if } V_{ns} < V_n \leq V_{ms} \\
I_n \left(1 + \lambda_n V_n\right) & \text{if } V_n \geq V_{ms} 
\end{cases}
\]

(1)

\[
I_{DSAT} = B \left(V_{GS} - V_{TM}\right)^m
\]

(2)

\[
V_{DSAT} = K \left(V_{GS} - V_{TM}\right)^n
\]

(3)

where \( V_{GS} \), \( V_{DS} \) and \( V_{DSAT} \) are gate-source, drain-source and drain-source saturation voltage, respectively. \( V_{TM} \) is the threshold voltage and \( I_{DSAT} \) is the saturation drain current. \( K \) and \( m \) model parameters control the linear region while \( B \) and \( n \) control the saturation region of operation in output characteristics. The parameter \( \lambda_n \) is added to take into consideration the channel length modulation. The JFET drain current is given by the following equations:
\[ I_{ds} = \beta V_{gs}(2(V_{gs} - V_p) - V_{ds}), \quad V_{ds} < V_{gs} - V_p \]  
(4)

\[ I_{ds} = \beta (V_{gs} - V_p)^2, \quad V_{ds} \geq V_{gs} - V_p \]  
(5)

\( \beta \) (BETA) and \( V_p \) are the JFET transconductance coefficient (A/V\(^2\)) and the pinch-off voltage, respectively. The two JFET SPICE model parameters \( \beta \) and \( V_p \) can be extracted using drain current equation for \( V_{gs} = V_{GSC} \) in linear and saturation regions in the quasi-saturation regime assuming the JFET gate-source voltage \( V_{gs} = V_{eff} = 0 \) [18]. Finally, the “effective” gate voltage \( V_{eff} \) is chosen as a linear function of gate voltage [18]:

\[ V_{eff} = gV_{gs} + V_0 \]  
(6)

The equation parameters \( g \) and \( V_0 \) can be extracted using the measurements drain current at quasi-saturation regime when \( V_{eff} = 0 \).

2.2. Dynamic behavior Modeling

To model the dynamic behavior of the power MOSFET, nonlinear interelectrode capacitances are added to the static model as shown in Figure 2. The parasitic interelectrode capacitances of the power MOSFET structure are divided into three nonlinear capacitances: \( C_{GS} \), \( C_{GD} \), and \( C_{DS} \).

In this paper, \( C_{GS} \) will be estimated by considering its value from blocking condition to conducting condition using the gate charge measurement. The estimated value of \( C_{GS} \) will be inspired by the Meyer’s simplified capacitance model [21]. On the other hand, \( C_{GD} \) and \( C_{DS} \) will be extracted from the measured device interelectrode capacitances (\( C_{rss} \) and \( C_{oss} \)).

2.2.1. Gate-source capacitance

\( C_{GS} \) is the sum of two capacitances: 1) constant capacitance \( C_{GS0} \) \( (C_{GS0} = C_{s} + C_{m}) \) and 2) nonlinear channel gate-source capacitance \( C_{GSB} \), see Figure 1. \( C_{GSB} \) is a MOS type capacitance with the channel P substrate short-circuited to N+ source. Therefore, the modeling of \( C_{GS} \) will be used by a modified Meyer’s simplified capacitance model [21] depending on both gate and drain voltages.

In the OFF state, \( C_{GS} \) is equal to \( C_{GS0} \). In linear region of operation, \( C_{GS} \) will be considered equal to the sum of \( C_{GS0} \) and the total channel capacitance \( C_{GSS} \). In the saturation region, \( C_{GS} \) will be estimated by using the Meyer’s simplified capacitance model, i.e. \( C_{GS0} + (2/3C_{GSB}) \) [21].

In linear region, we choose to add the entire channel capacitance \( C_{GSB} \) to the gate-source capacitance because, unlike the conventional MOSFET, in power MOSFET structure the N-drain is linked to the N+ drain of the power MOSFET, as shown in Figure 1.

As a resume, the nonlinear gate-source capacitance model can be summarized as follows:

\[ C_{GS} = \begin{cases} 
C_{GS0} & \text{if } V_{gs} \leq V_{cm} \\
C_{GS0} + C_{GSB} & \text{if } V_{ds} < V_{DSSAT} \\
C_{GS0} + \frac{2}{3} C_{GSB} & \text{if } V_{ds} \geq V_{DSSAT}
\end{cases} \]  
(7)

\( C_{GS0} \) is the gate-source capacitance in the off state of the power MOSFET device for positive gate voltages. Therefore, this capacitance will be extracted from \( V_{gs} \) curve in the gate charge measurement for \( V_{gs} < V_{TM} \). \( C_{GSB} \) is the capacitance of the channel region between the gate and the P-body source. Thus, \( C_{GSB} \) will be extracted from \( V_{gs} \) curve in the gate charge measurement at the linear region of operation.
In this paper, the nonlinear $C_{GS}$ capacitance is modeled by using an ABM module with replacing this capacitance by a controlled current source:

$$i_a = C_a \times \frac{d}{dt} (V_a)$$

(8)

2.2.2. Gate-drain capacitance

The gate-drain Miller capacitance $C_{GD}$ is a key parameter of the SPICE models for power MOSFETs. This Miller capacitance provides a feedback loop between the output and the input of the circuit limiting the frequency response of the transistor. As it can be seen in Figure 1, unlike the conventional MOS capacitance, $C_{GD}$ of the power MOSFET is a MOS capacitance with the substrate N region connected to drain of the device. Therefore, $C_{GD}$ will be modeled as a MOS capacitance depending on both $V_{GS}$ and $V_{DS}$ voltages ($V_{DG}$ voltage). In this paper, $C_{GD}$ is modeled by a constant oxide capacitance $C_{GD0}$ when $V_{DG} \leq 0$ and by the series association of $C_{GD0}$ with a depletion capacitance $C_{GDdep}$ when $V_{DG} > 0$, see Figure 1. Then the following expressions are used:

$$C_{GD} = C_{GD0} \quad \text{for} \quad V_{DG} \leq 0$$

(9)

$$C_{GD} = \frac{C_{GD0}}{1 + \frac{V_{DG}}{V_{JG}}} \quad \text{for} \quad V_{DG} > 0$$

(10)

where $C_{GD0}$, corresponding to the gate-drain oxide capacitance, is a constant capacitance. $M_{G}$ is the gate-drain grading coefficient and $V_{JG}$ is the gate-drain junction potential. These parameters will be extracted by using the provided datasheet reverse transfer capacitance $C_{rrx}$.

The nonlinear behavior of $C_{GD}$ is estimated by using the transition capacitance of the SPICE diode model [22]. In this paper, $C_{GD}$ is represented by a controlled current source formalism based on the ABM module of SPICE using equation 8 with replacing $i_{GS}$ by $i_{GD}$, $C_{GS}$ by $C_{GD}$ and $V_{GS}$ by $V_{GD}$.

2.2.3. Drain-source capacitance

As it can be seen in Figure 1, $C_{DS}$ is a drain-source junction capacitance. The non-linear behavior of $C_{DS}$ as a direct function of $V_{DS}$ is described by equation 11: as it can be seen in Figure 2, $C_{DS}$ is modeled by the transition capacitance of the SPICE diode model (“Dbody” diode). This diode will also takes into account the breakdown voltage of the power MOSFET and the forward biased behavior.

$$C_{DS} = \frac{C_{DS0}}{1 + \frac{V_{DS}}{V_{JD}}}$$

(11)

$C_{DS0}$ is the zero drain-source bias capacitance, $M_{D}$ is the drain-source grading coefficient and $V_{JD}$ is the drain-source junction potential. $C_{DS0}$, $M_{D}$ and $V_{JD}$ are parameters of the SPICE Dbody diode model.

3. Parameter extraction

The critical gate-source voltage $V_{GSSC}$ parameter is extracted from the transfer characteristic at the peak value of the transconductance $G_m$ as shown in Figure 3.
3.1. Static model parameter extraction

The channel MOSFET model parameters are extracted and specified from measured output characteristics for $V_{GS} < V_{GSC}$ with respect to the extraction procedure introduced in [18]. For $V_{GS} > V_{GSC}$, the JFET and the “effective” gate voltage parameters are extracted from the output characteristics at the quasi-saturation regime. The detailed extraction model parameters procedure can be found in [18].

3.2. Dynamic model parameter extraction

3.2.1. $C_{GD}$ and $C_{DS}$ capacitances

The model parameters of these two capacitances will be extracted from the measured $C_{gs}$ and $C_{oss}$ capacitances: $C_{GD} = C_{gs}$ and $C_{DS} = C_{oss} - C_{gs}$. The zero-bias junction capacitance ($C_{GDO}$ and $C_{DSO}$), the grading junction coefficient (MG and MD) and the junction potential ($V_{JG}$ and $V_{JD}$) parameters can be extracted by using the commonly used methods described in [22]: the three-point CV method or the linear regression with fixed diffusion potential method.

3.2.2. $C_{GS}$ capacitance

For the gate-source capacitance two parameters need to be calculated: $C_{GSO}$ which is the gate-source capacitance in off state and $C_{GSB}$ which is the total channel capacitance when the transistor is in the linear region of operation. These two capacitances are extracted from the gate charge $V_{GS}Q_G$ measurement as shown in Figure 4. Gate charge measurement gives the total amount of charge needed to turn on the power MOSFET from the blocking state. In gate charge measurement, a constant independent current source is applied at the gate terminal to charge the gate capacitance. $1/C_{GSO}$ is equal to the slope of the $V_{GS}Q_G$ curve when $V_{GS}$ is inferior to $V_{TM}$. $C_{GSB}$ is calculated from the slope of the $V_{GS}Q_G$ curve when the transistor enters in linear region, as shown in Figure 4.

![Figure 4. Extraction procedure for the gate-source capacitance.](image)

4. Results and discussion

4.1. Static validation

In [18], it was reported that the static model provides an accurate representation of the static behavior of the power MOSFETs. Figure 5 shows $I_{DS}-V_{GS}$ simulated and datasheet transfer characteristics of the standard power MOSFET. At the quasi-saturation regime, a good agreement between the simulated and the provided datasheet is observed. Unlike the standard power MOSFET models, the error percent introduced by the proposed model remains practically constant with increase of gate-source voltage $V_{GS}$.
4.2. Dynamic validation

The datasheet and the model simulated static reverse and output capacitances for the standard and the trench power MOSFETs are shown in Figures 6 and 7 respectively. Good agreement is observed, however discrepancy is observed in the transition region between low and high $V_{DS}$ voltages. This divergence is due to the non-uniform doping channel region in VDMOS device which make the determination of $C_{GD}$ and $C_{DS}$ grading coefficients more complex [15]. The proposed interelectrode capacitance model gives excellent agreement in case of the standard and the trench devices compared to the datasheet curves.

![Figure 5](image-url)

**Figure 5.** Simulated and datasheet $I_{DS}-V_{GS}$ characteristics of the N-channel standard power MOSFET transistor for $V_{DS} = 1.5$ V and $V_{DS} = 15$ V.

![Figure 6](image-url)

**Figure 6.** Device datasheet (dashed) and SPICE simulated (solid) $C_{rss}$ and $C_{oss}$ of the N-channel standard power MOSFET transistor ($V_{GS} = 0$ V).
Figure 7. Device datasheet (dashed) and SPICE simulated (solid) $C_{rss}$ and $C_{oss}$ of the N-channel trench power MOSFET transistor ($V_{GS} = 0V$).

On the other hand, the dynamic validation is made by the simulated and datasheet gate charge test for the standard (Figure 8) and the trench (Figure 9). As it can be seen, excellent agreement between simulated and measured gate charge test with an average error percentage less than 10% is observed.

Figure 8. Device datasheet (dashed) and SPICE simulated (solid) gate charge results of the N-channel standard power MOSFET transistor.

Figure 9. Device datasheet (dashed) and SPICE simulated (solid) gate charge results of the N-channel trench power MOSFET transistor.
5. Conclusion
An enhanced equivalent circuit model for power MOSFET devices has been presented. The model takes into consideration the nonlinear interelectrode capacitances. The model parameters were extracted from device datasheet informations. Comparison between PSPICE model simulations and datasheet values allow the validation of the model for the trench and standard power MOSFET structures. Future direction of this work can be devoted to give a unified model of all power MOSFET structures in order to capture the switching behavior of the power MOSFET in simulation of power electronic converters.

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