Microtransformer on silicon with CoFeB magnetic core for high-frequency signal applications

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ABSTRACT
This paper presents the development, characterization and application of a microtransformer with a bar magnetic core fabricated on silicon substrate using thin-film technology. The magnetic core, coils, and insulation layers were deposited using only sputtering PVD (physical vapor deposition) or CVD (chemical vapor deposition) processes. As insulation materials, silicon dioxide and silicon nitride are only used. The device is small with a chip size of $1600 \mu m \times 800 \mu m$. The transformer has a turns ratio of 1:1 and achieves a self-inductance of about $40 \text{nH}$. The minimum measured breakdown voltage of the microtransformer is 1250 V(DC). The microtransformer device is applicable for frequencies up to 20 MHz. The device was fabricated on 12-inch silicon substrates on mass production equipment.

INTRODUCTION
One of the most important development challenges for monolithic solutions for Internet of Things (IoT), wireless communication, and many portable devices is the integration of on-chip inductors and transformers with magnetic materials on silicon. Most recent works in this technical field do not only show big improvement in integration technology and magnetic material research but also the development of new micro inductors and microtransformers and their implementation in many applications. New magnetics materials with high magnetic flux density like CoFe and materials with low core losses like CoZrTa, CoFeB were developed and used in microinductors and transformers. Microinductors and microtransformers were realized using different design approaches such as using bar core, closed toroidal cores or racetrack core. The bar magnetic core design is used frequently due to its ease of implementation since only one magnetic layer is used and be fabricated in one process step. On top of that, a uniaxial anisotropy can be realized with such a structure. Closed toroidal core designs can be fabricated in one deposition step and allows flux to flow in the plane but uniaxial anisotropy can not be realized, resulting in poor efficiency. The racetrack core allows for the use of anisotropic material but on the other hand requires complex and expensive fabrication steps. Microtransformers can be used in many applications at high switching frequency of tens of MHz. The most common applications are dc-dc converters (isolated and non-isolated) and digital isolators in SiC or GaN applications.

DESIGN AND FABRICATION OF MICROTRANSFORMER DESIGN
For microtransformer design, a solenoid design approach is chosen. The schematic of microtransformer device is shown in Fig. 1a. The microtransformer features a bar magnetic core with segmented primary and secondary coils. The magnetic core has a bar shape and consists of two magnetic layers, which are separated by a silicon oxide layer. Coils are surrounding the magnetic core and are formed by bottom coil layer, top coil layer and via layer. All these structures are embedded in insulation material. Figure 1b shows a
The microtransformer device was designed using Finite Element Method (FEM) software tool Ansys Maxwell®. The aim of simulation was to find out a design with inductance value in the range of 20 nH – 40 nH for a small chip size 0603 EIA standard (Electronic Industries Alliance). Therefore, completed microtransformer device have a footprint of 1.6 mm x 0.8 mm. Desired breakdown voltage of device was 1 kV. Based on simulation result a design with two separated windings (coils) is defined. A minimum distance between primary and secondary winding is 30 μm. Both windings are identically with 12 turns each. A dimension of turn is 620 μm x 40 μm x 1 μm (L x W x T) with a 10 μm distance between turns. The winding material is copper fabricated using PVD process. The thickness of deposited cooper material is only 1 μm, therefore, the microtransformer device shows an electrical resistance of about 7 Ω, hence this device is suitable for use in signal applications. The inductance of the simulated device is about 30 nH. The coupling factor between primary and secondary coils is about 0.2.

The sputtering target has the stoichiometric atomic composition of 60%Co, 20%Fe, and 20%B. Magnetic properties of deposited CoFeB were measured using vibrating sample magnetometer (VSM). For measurement, the magnetic material was deposited on Si-chips (10 mm x 5 mm). The magnetic flux density Bs of 1.5 T, coercivity of 800 A/m (~10 Oe), and magnetic permeability μr of about 700 were measured. For simulation an effective magnetic permeability is defined by taking in account demagnetization effects (method described in Refs. 21 and 22). A permeability value ρ of 450 is applied for a simulation. The magnetic core consist of two magnetic layers with dimension of 1400 μm x 500 μm with a thickness of 0.4 μm and oxide gap in-between of 0.5 μm. The insulation material is combination of SiO2 and Si3N4.

**Fabrication process**

The fabrication starts with deposition of a buffer silicon oxide layer on 12"-Si wafer. The thickness of a buffer oxide layer is 1 μm.

On top of this layer a 500 nm thick silicon nitride layer is deposited. Silicon oxide and silicon nitride are deposited using CVD (chemical vapor deposition) process. Deposition of an oxide and a nitride layers is necessary for providing enough insulation (higher than 1 kV) between silicon wafer and metal layer. In the next step a silicon oxide layer with a thickness of 1 μm is deposited. After that, the first lithography step for patterning the bottom coil layer is performed. For lithography processes, a 250 nm thick resist is used. Then, the etch step is carried out for crating trenches in the silicon oxide. Next step is the deposition of bottom Cu metal layer. The structuring of metal layers is carried out using damascene process. Therefore, a Cu layer with a thickness of 2 μm deposited. In the next step, a CMP (chemical mechanical polishing) process is carried out for removing unnecessary Cu material and to ensure a bottom metal thickness of 1 μm. In addition, the overall flatness over wafer will be improved what is important for next lithography processes. Next step is the deposition of 500 nm thick silicon nitride layer to ensure an insulation between bottom metal layer and first magnetic layer. Silicon oxide is deposited in the next fabrication step. The thickness of this layer should be the same as a desired thickness of a magnetic core layer. In our case, the core thickness and oxide thickness is 400 nm. Accordingly, the lithography step for patterning trenches for magnetic core is done and trenches are creating by silicon etching (Fig. 2a). Then, the CoFeB magnetic material is deposited with a thickness of 800 nm and the CMP process for forming the core is carried out.

The same procedure as described before is repeated for creating the second magnetic core layer. After that, next Si3N4 insulation layer between second (upper) magnetic layer and top Cu metal layer with a thickness of 500 nm is deposited. Next step is creating of deep via structures for connecting bottom and top metal layers of coil. First, the lithography process is carried out for patterning of vias, than deep via trenches are etched applying a RIE (reactive-ion etching) process. Deep vias have a dimension of 40 μm x 20 μm (L x W) and a depth of 2.3 μm. The via trench is etched through 3 silicon nitride layers and 2 silicon oxide, which in the sum a thickness of 2.3 μm have. In the next step, via trenches are filled with Cu and with CMP polishing process vias are created. Last fabrication step is creating top Cu metal layer. This step is a same as the process step for bottom metal layer. Figure 2b shows a micrograph of completed microtransformer devices.
EVALUATION OF MICROTRANSFORMER DEVICE

Fabricated microtransformers devices are diced and packaged into the open cavity QFN package. The QFN package with dimension 5 mm x 5 mm and a height of 1.35 mm and with eight leads was used. For testing, only four leads were connected. Contact pads of the microtransformer are connected to the package leads using wire bonding. Packaged devices are tested using Agilent Impedance Analyzer E4991A. The devices were measured with a signal oscillating level of 5 mA at 1 MHz. Figure 3a shows characteristics of inductance L, quality factor Q and resistance R versus frequency.

The measured inductance shows a value of about 40 nH, which is higher than simulated value of 30 nH. The higher inductance can be explained by additional inductance of bonding wire, by measurement system errors and by non-optimized fabrication steps. For evaluation measurements, the device are packaged in QFN package. The package size was not optimized for chip size and longer bond wire were used. The long bond wires added additional parasitic inductance to the inductance of the packaged device. Standard wire bond has an inductance value of about 1 nH/mm. The inductance is stable until 15 MHz. The Q factor of device is small and has a maximum value of about 0.5 at 25 MHz. The Q factor is small regarding to the high electrical resistance of device because of applied thin Cu layer thickness of only 1 μm. The electrical resistance of device $R_{DC}$ is about 7 Ω which corresponds with simulated value.

Figure 3b shows a characteristic of inductance over DC-bias. In Fig. 3b, the characteristics at 5 MHz, 15 MHz, and 20 MHz are shown. By increasing of DC-bias, the inductance value is decreasing. At DC-bias of about 60 mA all three curves show almost same value. This current of 60 mA can be defined as saturation current of microtransformer device. The saturation corresponds to a 20%-25% percent drop in inductance ($\Delta L/L$). Also the insulation voltage of device is measured. The minimum measured breakdown voltage of the device was 1250 V$_{DC}$.

TESTING IN HIGH FREQUENCY DATA TRANSMISSION APPLICATION

In order to verify the suitability of the developed microtransformer to be used in signal applications, a simplified data transmission system is built and tested. The simple data transmission system consists of three main blocks as shown in the Fig. 4a. First, it has
a digital controller, which acts as a transmitter generating a unipolar sinusoidal. Second, it has a decoupling network, realized using an R-C network, which blocks the dc component of the transmitted data to avoid transformer saturation. Third, it has a receiver, realized using a second digital controller. Experimental results of the simplified data transmission system are shown in Fig. 4b–d. Figure 4b shows the unipolar transmitted data. Figure 4c shows the bipolar signal after using the R-C network. Figure 4d shows the voltage across the secondary side of the transformer received by the second digital controller. It can be noted from Fig. 4d that the voltage is attenuated at around 200mV compared to 1V after dc blocking, as shown in Fig. 4c. The attenuation takes place as the coupling factor of the transformer is around 20%. It is worth mentioning that in the targeted applications, it is only needed to detect the peaks and the valleys of the transmitted signal, meaning 20% coupling is sufficient in this case.

CONCLUSION

This paper showed the feasibility of fabricating a small signal microtransformer on 12-inch silicon substrates on mass production equipment. The microtransformer has lateral dimensions of 1600 μm x 800 μm and under 10 μm height. The microtransformer was used in a high frequency data transmission system where the system showed a reasonable performance. The future work includes integrating the microtransformer with the data transmission system in one package to form a standalone digital isolator. In addition, a point of further research is to optimize the transformer design to improve the coupling factor of the microtransformer.

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