FlexClock: Generic Clock Reconfiguration for Low-end IoT Devices

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Abstract

Clock configuration within constrained general-purpose microcontrollers takes a key role in tuning performance, power consumption, and timing accuracy of applications in the Internet of Things (IoT). Subsystems governing the underlying clock tree must nonetheless cope with a huge parameter space, complex dependencies, and dynamic constraints. Manufacturers expose the underlying functions in very diverse ways, which leads to specialized implementations of low portability.

In this paper, we propose FlexClock, an approach for generic online clock reconfiguration on constrained IoT devices. We argue that (costly) generic clock configuration of general purpose computers and powerful mobile devices need to slim down to the lower end of the device spectrum. In search of a generalized solution, we identify recurring patterns and building blocks, which we use to decompose clock trees into independent, reusable components. With this segmentation we derive an abstract representation of vendor-specific clock trees, which then can be dynamically reconfigured at runtime. We evaluate our implementation on common hardware. Our measurements demonstrate how FlexClock significantly improves peak power consumption and energy efficiency by enabling dynamic voltage and frequency scaling (DVFS) in a platform-agnostic way.

1 Introduction

Small embedded systems in the form of microcontrollers can be found literally everywhere today. Gadgets, robots, home automation, and industrial controls are examples of the ever growing application fields. The industry provides specialized micro controller units (MCUs) of various kinds. The heartbeat of these tiny computers is some clock signal—or more accurately—many of them. Individual clock sources have diverse properties to serve specific tasks. The choice between them allows for optimizing parameters toward a designated design goal. Depending on whether cost, accuracy, or environmental robustness is desired, resistor-capacitor (RC)-, silicon-, ceramics-, or crystal-oscillators may be preferred. Since no solution fits all needs, most MCU manufacturers provide a multitude of internal and external clock source options. Switching between them is done via MCU internal clock networks that allow routing and scaling of clocks to supply peripheral blocks with the required frequency. We refer to this network as clock tree.

With embedded devices continuously pushing the limits of size, cost, performance, and power frugality, it becomes increasingly important to squeeze the last efficiency bit out of every layer. At the same time, the economy of scale advocates mass-production of general purpose MCUs when developing new IoT devices. The permanent conflict between tight time-to-market requirements and low resource constraints raises the need for trade-offs. Solving this challenge for a specific application on one target platform, though, will often generate little impact on future solutions.

An area where this tussle is very likely to occur are MCU-internal clock (re-)configurations. Solving these complex challenges is fundamentally important whenever energy efficiency is of concern because any switched signal directly affects the power consumption. System clock frequency is thereby a direct control knob to balance between high performance and low power.

Dynamic voltage and frequency scaling (DVFS) is a well-known approach to leverage this effect and reduce power consumption, which potentially saves significant energy. Any software component that wants to apply such generic energy savings, needs control over the clock configuration of the underlying hardware—indeed, that of the application and target platform. We therefore argue for generalizing core DVFS components and turn them into generally available system services of widespread applicability.

In this paper, we introduce FlexClock, a model, architecture, and implementation of a lightweight generic clock configuration module that enables platform independent control of complex, MCU-internal clock trees. Specifically, we focus on the key components needed for a generic, reusable DVFS framework. We believe that this is most versatile in making power saving available across platforms. Our proposed solution makes the following contributions:

1. A flexible scheme for light-weight modeling of complex MCU clock-trees.
2. An interface that provides streamlined access to fine-grained clock control.
3. A cross-platform implementation that can dynamically explore and reconfigure clock-trees during runtime.
4. An easy strategy to integrate the proposed features into existing embedded operating systems so that they benefit from fully automated DVFS.

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In the remainder, Section 2 will work out the inherent properties and challenges of clock trees and sketch the scope of a reusable module for modeling and (re-)configuring clocks. In Section 3 we introduce our concept of FlexClock and report about its implementation. Key performance metrics of this solution are then evaluated in Section 4. Alongside we discuss notable effects and relevant implications. Related work is compared in Section 5. Section 6 summarizes our findings and presents an outlook on future work.

2 The Clock Tree and its Forrest of Problems

Clock trees form the fundamental clock networks within MCUs, which are responsible for distributing and conditioning the clock ticks required for operating almost every internal component. They substantially differ in complexity and implementation – not only between vendors but also between MCU series and models of the same vendor. In addition, clock trees often come with very complex dependencies that are entangled with hardware configurations, hardware constraints, use of peripherals, environmental conditions, and application demands. Modeling a clock tree as a generic reusable component is a hard problem.

Typical IoT or Wireless Sensor Network (WSN) applications avoid this problem by implementing clock tree configurations with static code—only configurable at compile-time. While obviously very efficient w.r.t. code size and execution time, this static pattern does not allow for dynamic reconfiguration at runtime. Platform dependent configurations also lead to compile-time parameters that differ across platforms in terms of syntax and encoding, which makes it hard to discover and understand them for application developers.

Figure 1 displays a simplified example of a typical MCU clock tree. Left are various clock sources of the clock tree—more precisely, the root nodes of multiple clock trees, which overlap in parts. From each source the clock signal is distributed to intermediate nodes such as muxes or different kinds of scalers to finally feed a consumer node such as a timer or the central processing unit (CPU). The clock network also contains gates, which can disable individual peripherals or entire sub-trees.

Optional features and configuration options do not only come with hardware. Similar flexibility is granted at runtime control when specific MCU-internal clock sources or complete tree branches are (temporarily) disabled by software configurations. A simple intuitive approach may suggest that such options could just be added as a part of respective peripheral drivers. Drivers, however, only implement the control over individual devices and cannot manage the coordination of distributed device utilization, which is present if various devices require the signal of an individual clock. Hence, any solution for managing the (re-)configuration of clock trees will face the complexity of evaluating such distributed dependency and will therefore not be simple.

2.1 Common Building Blocks for Clock Trees

Clock trees attain various structures and associated properties as previously described. Most entities that form a clock tree, though, share common functionality and capabilities and effectively serve as the basic building blocks of a clock tree. While in theory a minimal clock tree could just consist of clock sources connected to clock consumers, in practice there are more classes or types of entities, which we collectively refer to as clock nodes. To increase flexibility, additional intermediate clock nodes can be found between sources and consumers that manipulate routing of the clock signals to different destinations or change properties of a clock, such as its frequency, calibration, or duty-cycle. Most common patterns and shared functionality across various forms of clock trees can be found on this level of individual but interconnected clock nodes.

The most primitive form of a clock node is a gate. Its only purpose is to enable or disable a clock signal. If gated, the input signal is not forwarded to its output. Anything connected to the gate output thereby is disconnected from the clock signal. A mux selectively passes on one of its input signals to a single output. This base type is used to choose a clock source from multiple options. Additionally, there are multipliers, e.g., based on phase-locked loops (PLLs), and dividers. Because dividers and multipliers both manipulate the clock signal by scaling its frequency, they can be combined in the group of scalers.

The exact features and implementations of clock nodes may differ between platforms but their high level objective and semantics are shared. In most cases, the interface to the hardware also shares many commonalities. For example, with control patterns based on memory mapped configuration registers, it is very common to program settings by writing values to specific addresses and use bit flags for triggering or observing operations and state changes.

2.2 Configuration Space(s)

Management and encoding of configuration parameters that describe the clock tree and underlying hardware properties need to address several challenges. Properties of the employed hardware but also its individual platform composition with external components must be visible to configuration tools. We differentiate between static properties, static configuration and runtime configuration.

2.2.1 Static Properties

Static properties are expected to be fixed for a specific target platform. Here the term target platform refers to a specific system model consisting of an MCU and components such as connected sensors or crystals. Within static configuration different levels of abstraction apply. Some properties are tied to the employed MCU model (e.g., can a crystal be connected?). The information whether this oscillator...
is actually present on a specific target platform (e.g., a specific smartwatch or an evaluation board) accordingly belongs to another level of abstraction. Static properties therefore should be organized by grouping commonalities for reusability while allowing to overwrite and supplement detailed differences where needed.

2.2.2 Static Configuration

Static configuration concerns parameters that are changeable but there is either no need to change the parameter at runtime or it is too expensive to do so. Like static properties, this configuration is defined at compile time. For example, a product that shall read data from an external Universal Serial Bus (USB)-Stick could statically configure and enable a 48 MHz clock for driving the internal USB peripheral of the MCU. A change of static configuration thus requires an update of the system.

2.2.3 Runtime Configuration

Runtime configuration is applied where system parameters are adapted during operation without changing the firmware. Its data that describes valid configuration options and the code that actually perform the changes need to be contained in the firmware. Reconsidering our USB example, consider our hypothetical device requires a low power consumption. In that case, runtime configuration of the USB peripheral clock becomes highly preferable because it provides an easy way to reduce power consumption while the USB-port is not in use.

Comparing the different configuration types based on these very simplified examples illustrates that there is no single optimal solution that applies to all scenarios. Instead, it depends very much on the application and its requirements if one approach is preferable over another. It also becomes apparent that access to static properties is required for both, static and runtime configuration. Thus, it is favorable to provide static properties in a way that is accessible to both approaches for improved consistency and maintenance. Because of the target domain of very constrained embedded devices, runtime configuration must additionally be expressed very efficiently.

2.3 Complex Clock Configuration Transitions

The complexity of the procedure for changing a clocks frequency (i.e., a clock configuration transition) can be anything from very low when only affecting a single clock instance, to very high when affecting multiple different settings of different nodes. In simple cases the clock may for example be updated on-the-fly by just writing a new pre-scaler value to the corresponding configuration register. The change is immediately applied and a new frequency is in effect. Contrarily, a transition that consist of multiple phases is what we refer to as a complex transition. Following we list several reasons on why complex transitions are needed.

- The frequency change may take additional time to complete during which the frequency could be unstable. Examples for this are PLLs that require some time to synchronize again.
- The clock may not be adjustable on-the-fly. This is particularly a problem when clocks supplied by this node are not allowed to be stopped. A complex transition to

work around this issue is to temporarily switch to another clock source, adapt the original one and eventually switch back.

- The transition may require additional precautions to be taken before the new configuration becomes applicable. Examples for this are adjustments to voltage range or flash access parameters.
- The transition may directly or indirectly affect other parts of the clock tree.

In some situations multiple of these conditions may additionally overlap. Figuring out online what kind of transition is feasible, allowed and preferred can impose significant overhead in terms of processing time. Therefore, it can be beneficial to allow pre-determination of complex clock transition steps to enable fast execution of repeated complex transition procedures.

2.4 Hard Resource Limits

It is worth highlighting the significant challenges associated with scaling down the overhead of a generic solution to the MCU class of devices.

In small embedded systems data structures for encoding properties and managing runtime states can have a significant impact on the memory footprint. Same is true for code performing operations on the clock tree model or the control hardware itself. This does not play very well with constraints of IoT-class devices. Not only dynamic loading of hardware configurations is out of scope but even dynamic memory allocation is preferably avoided to reliably comply with fixed memory budgets. When working on tree structures, recursive implementations are often an easy go-to solution. Though, even for comparatively small clock trees and their possibilities of individual frequency settings the number of considered states imposes significant RAM overhead. These problems therefore either need an implementation that is able to handle the huge state over time by processing it iteratively or thorough analytical solutions to also reduce processing overhead.

By now we introduced the principle behind clock trees and the problems associated with providing a generalized solution to them. In Section 2.3 we introduced the common building blocks we need to be able to flexibly combine into expressive models of higher order clock trees. Albeit in the real world many more types of very specific clock nodes are found, even on platforms with very complex clock trees, we did not encounter any that could not be modeled as a combination of the aforementioned base types. Thus, we argue that this is a reasonable minimal but still expressive set of different base types required to model typical MCU clock trees.

It is worth mentioning though, that in some cases providing more specific implementations can further reduce the overhead. In the next section we will capture the details of the FlexClock concept and implementation.

3 Concept and Implementation of FlexClock

For architecting reusable software components it is crucial to precisely identify and separate specifics from generics and to find an appropriate level of abstraction. With a significant portion of shared behavior and common functionality
sitting at the level of individual clock nodes this is the level we chose to abstract and generalize the hardware facing part of the interface for accessing and configuring the clock tree.

### 3.1 Layered Architecture for Flexibility

Splitting the clock tree into reusable components for modeling and encoding, also requires a generalized interface for accessing base functionality. Generic clock configuration can provide plenty automations and features that may be welcome or even strictly required in one case can transform into unnecessary overhead for a different use case. An absolute must therefore is to incorporate optionality into the architecture. Depending on features required by the application and capabilities provided by the hardware some features may not always be enabled to improve memory overhead in cases where it matters. For example runtime exploration and reconfiguration incurs significant complexity but may not always be needed. A layered architecture helps in that case to move common functionality and reusable patterns to a higher utility layer while keeping only hardware specific details in the lower hardware abstraction layer. Data should  

always be separated from the code that uses it to improve code-reuse and avoid duplication.

Decisions on where to draw lines for features and capabilities that should be optional can not be made completely objectively. Systematically structuring the functionality and configuration options of clocks helps to get a better understanding on what and how needs to be abstracted. Adopting clock configuration is generally done in two distinct ways that are important to differentiate. Changing frequency and changing topology. Scaling frequency shall never affect topology but switching the topology can affect the frequency. Changing topology can have significant impact and implications. One clock source may not be available in a specific (low-power) operating mode of the MCU, or it might have insufficient accuracy for an application. Modeling this explicitly in the lower layer (i.e., as separate functions) retains direct control over these aspects to the upper layer. In cases where applications only use a fixed topology this also gives the flexibility to exclude code only required for topological adjustments while keeping the option to scale frequency.

Even within a single system multiple different clock types and instances exist at the same time. A flat static application programming interface (API) is therefore not sufficient. Every variant would need an additional code branch in and the overhead of this quickly overshoots the overhead for a more dynamic function pointer based interface.

Figure 2 gives an overview on the FlexClock architecture and involved modules. The topmost and lowermost layers, namely the application and hardware, are decoupled from the clock framework itself and thus only displayed for illustrative purposes. The application never has to interact with the clock framework if not aiming for direct manual control. All framework components operating on the Abstract Clock interface are completely agnostic to underly hardware. This abstraction is facilitated by modeling the clock tree based on the following principles. Platform specific configuration options and hardware access description shall always be provided as static data, separated from the clocks base functionality. Wherever possible, reusable implementations of the base types Gate, Mux, and Scaler are to be used. More complex nodes can either be modeled from orchestrated and decorated base types, or optimized custom types can be added for very specific clock nodes. It is important to highlight that this only concerns the hardware abstraction layer and no other part of the framework must be extended.

### 3.2 Property Encoding

Clock nodes can have many configurable and immutable properties. Most important ones are possible configuration options like valid input sources, divider values, and respective values that need to be written to configuration registers. Also, the register addresses itself and constraints on how reconfiguration can be performed needs to be stored. For example whether a clock can be adjusted on the fly or that it (or its parents, children) must be stopped before its frequency can be adapted. Valid configurations require flexible but efficient encoding and mapping to translate between logical and register values.

For binary values bit-fields are employed that split a shared memory region between specific low level drivers and generic high level drivers. Numerical values are encoded using an (extendable) set of mapping types to easily model either sets of distinct values, or ranges within limits. Further memory overhead reductions are achieved by introducing indicators for commonly found implicit numerical value encoding patterns. With that, the memory overhead for mappings between logical and register values can be effectively halved in many cases. Using the previously mentioned bit-fields as modifiers to mapping types gives additional expressiveness with minimized memory overhead.

Instead of saving configuration registers and masks separately for every clock node we leverage the fact that only a limited amount of configuration registers are typically responsible for clock configuration and combine them into a lookup table. With that a specific configuration register can be identified with only a few bits and a single integer can be shared for storing the register id, masking information and bit indexes for common flags like enable and ready states.

All above properties must be provided within separate static data structures to support static memory allocation and allow selective inclusion. This static definitions additionally opens the door to a priori (offline) tweak the encoding to-

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**Figure 2.** The architecture of the overall clock framework for online re-configuration and self adaptation.
wards targeted design goals like less memory usage or faster execution speed. Combining these principles allows easy to understand modeling while still being expressive, memory efficient and leaving flexibility for optimization adjustments.

Descriptions such as frequency multiplier factors between 1 and 8 being configured by writing values from 0 to 7 into a specific register can therefore be encoded by just defining the bounds (1, 8) and using a zero-based implicit register value modifier. Including the condensed configuration register descriptor this requires just two 32-bit integer values to describe the upper layer how to access the hardware registers and what is allowed to be written there.

3.3 Notification & Transaction Mechanism

Interaction between FlexClock and other modules requires methods to request, indicate or block changes. While FlexClock can itself handle clock tree internal dependencies and constraints related to hardware configuration, this does not apply to dependencies that originate from internal state of peripheral drivers or application logic. For example, a clock can be safely turned off if no other component is using it at all. But if another module is using the clock it is up to that module (e.g., a peripheral driver) to block or allow transitions to not interfere with its operation. An Serial Peripheral Interface (SPI) master peripheral driver for example may be capable of dynamic reconfiguration by just adapting its internal prescaler accordingly to maintain the same output frequency. But this reconfiguration shall of course not be allowed during a data transfer. Similarly, increasing the frequency of a specific clock domain could require a higher supply voltage. Therefore, FlexClock must be able to request a higher supply voltage before increasing the frequency. This can also be implemented via the notification system.

To give external modules a chance to completely block clock transitions or trigger reconfiguration procedures after a successful clock transition we employ pre, release, and post hooks that can be registered for any existing clock instance. The return value of the pre-hook indicates whether a specific change is feasible for a module at the moment. If a pre-hook indicates success, the module that registered the hook must be in a state that is prepared for two cases that may happen afterwards. The intended clock-change may be performed and the post hook will be executed immediately after all pre hooks indicated success. After executing the post hook, the respective modules must be back to normal operation mode. If any other hook permits a transition no change will be applied and the release hook will be executed.

3.4 Dynamic Voltage and Frequency Scaling

FlexClock is expected to provide major benefits to implement DVFS as a reusable model for a wide range of target devices. Therefore, this section gives a short overview on aspects of DVFS most relevant for our scope. We will not broadly discuss the theory and instead refer to Castagnetti et al. [6] and Eyerman et al. [8] for a more comprehensive background introduction. Essentially, power consumption of Complementary metal-oxide-semiconductor (CMOS) circuits can be separated into a dynamic and a static part. The dynamic power consumption of a switched circuit is described with \( P = \alpha \cdot C \cdot V^2 \cdot f \). Where \( C \) is the capacitance of the circuit being switched, \( V \) the voltage and \( f \) the frequency. The transistor switching activity (i.e., number of switched transistors) is reflected with \( \alpha \). In the scenarios we focus on (an MCU performing computation) the dynamic share is by far the dominating power consumption share — as we will also show in Section 4.

With \( C \) being a property of the specific device, and \( \alpha \) mostly being dictated by the executed application, the only variables we can influence to lower power consumption for a specific application on a given device are \( V \) and \( f \).

On first sight the squared voltage looks like the major contributor here. But when searching for the configuration with the lowest power consumption there are a few important conceptual and practical aspects to keep in mind.

- The minimum required voltage directly depends on the frequency. Voltage thereby can not be scaled down independent of the frequency.
- The range available for adjustments is significantly more limited for voltage. Even with modern microcontrollers, core voltage often ranges from 1.8 V down to around 1 V. Whereas frequencies can be scaled from tens or hundreds of MHz down to kHz range.
- Time overhead can differ significantly between voltage and frequency. Voltage scaling incurs a relatively static time overhead in the order of several \( \mu \)s per 10 mV. While frequency scaling can be almost instantaneous (e.g., when switching a mux or changing a prescaler value) to taking multiple ms (e.g., when cold-starting an oscillator).
- For the same task an MCU is in most cases operating less efficient at a lower clock frequency because of static (leakage) consumption.

The significant energy optimization potential of DVFS now comes from the fact that software rarely utilizes the full performance provided by the MCU at all times. A mismatch between the performance configuration of the hardware and the utilization by software is therefore directly wasting energy. For example consider execution phases where the MCU is waiting for an operation to finish, like completion of an analog to digital converter (ADC) conversion, reading a slow external sensor, erasing a flash page, or transmitting data. Software does not require full computing performance in those cases, leaving potential to trade not utilized performance for energy savings. With these considerations in mind it seems surprising that DVFS is still not available as a reusable module that can be easily added to an embedded system.

3.5 Performance Utilization to Control DVFS

With FlexClock, DVFS can be applied automatically and transparently to the application. As mentioned before, DVFS optimization potential originates from the (temporary) mismatch of available performance and its utilization. Leveraging this effectively therefore requires precise knowledge on the systems’ state and behavior.
A simple utilization metric often employed on MCUs is shown in Equation 1 as the ratio between the time the CPU executes a task and being idle. We argue that this utilization metric is not well suited to leverage full DVFS potential because it does not consider tasks appearing to utilize the CPU that are in fact limited by other operations that do not require high performance. Thus, we propose using a utilization metric that takes into account the actual performance demand of a task.

\[
pu = \frac{t_{busy}(F_1)}{t_{busy}(F_2)} \cdot \frac{F_1}{F_2}, \quad F_1 < F_2
\]

Equation 2 reflects this by incorporating \( F_i \), referring to the CPU core frequency. A task perfectly scalable would respectively reduce its busy time in the same ratio the frequency was increased. The assumption is therefore that tasks with low \( pu \) values possess high potential for saving energy. In the following section we evaluate this on a real system.

4 Evaluation of FlexClock

In the following we evaluate key performance metrics of FlexClock in terms of functionality, performance, and overhead. Therefore, we explain the features enabled by FlexClock, and quantify how well it fulfills its purpose at what cost for operations. In detail, we first qualitatively highlight improvements enabled by FlexClock and relate its new functionality to alternative mechanisms. Second, we identify parameters affecting applicability and accuracy of FlexClock by benchmarking configurations in static scenarios. Third, performance of applying FlexClock dynamically is quantified in terms of errors, timing overhead, and power savings.

In particular, we use the online clock reconfiguration features exposed by FlexClock for hardware-agnostic DVFS and evaluate the energy savings enabled by it. The performance of those features is investigated separately, giving detailed insight on parameters affecting errors and induced overhead. Results are discussed alongside, outlining limitations to indicate where future work will most likely achieve further improvements.

All experiments are performed on an STM32L476RG MCU using its Nucleo reference platform, making conducted experiments easily reproducible. The MCU is powered through USB via the 3.3 V voltage regulator on the evaluation board. Its current measurement connector (IDD) is directly connected to a highly accurate Keithley DMM7510 digital sampling multimeter [10]. All current measurements provided in following sections are obtained using this fixed supply configuration.

4.1 Functionality Enabled by FlexClock

Key features of FlexClock make static and dynamic clock configuration of advanced clock trees feasible at runtime. Interactive exploration of clock subsystem capabilities improves usability as well as visibility for the developer.

Next, we show how the added level of control furthermore enables systems to reduce peak power consumption and improve energy efficiency in both static and dynamic scenarios.

4.1.1 Lowering Power Consumption

Applications facing (temporary) constraints on peak power consumption can leverage FlexClock to statically throttle clock speed. For example, systems facing critical supply voltage due to low battery may thereby limit power consumption, maintaining reliable operation of the voltage regulator. Energy harvesting systems subject to variable power supply [19, 5] can significantly extend their battery lifetime by throttling the clock frequency [1].

Power consumption can be reduced further by disabling any unused clock sources, internal sub-topologies of the clock tree, or input clocks of deactivated peripherals. Again, this functionality can be applied statically via setup functions or dynamically by active software power management [9] if peripheral usage changes during runtime.

Besides statically enabled and disabled clocks, the clock frequency and the properties of instructions being executed have high impact on the MCU power consumption. To roughly quantify the magnitude of power consumption reductions enabled by FlexClock we perform several micro-benchmarks on our test system. For a reasonable baseline we sweep the clock frequency for all tasks to see how consumption is affected by frequency and task performed.

![Figure 3. MCU current draw behavior for tasks that execute different instructions (divide, add, multiply) at different clock frequencies.](image)
configuration is more energy efficient for a specific task.

An alternative mechanism commonly used to reduce consumption of an MCU device is to duty-cycle its operation using low-power modes (LPMs). Most notable differences to that approach are that an MCU can not perform work while set to LPM operation and the there is no direct control over the active mode performance and consumption.

Table 1 puts the previously stated consumption stats of a slowed down (but still actively processing) MCU into perspective with the static consumption of low power modes that completely stop ongoing execution. It additionally lists time overhead associated with transitioning from the stopped state back to operation mode to continue execution. We measured these numbers using general-purpose input/output (GPIO) instrumentation and our FlexClock test application based on the 2020.07 release of RIOT [3].

| Low Power Mode | Exit Transition Time | Current |
|----------------|----------------------|---------|
| PM0            | 9.3 ms (to main)     | 410.3 nA|
| PM0            | 2.4 ms (to system init) | 410.3 nA|
| PM1            | 9.6 µs (to callback) | 8.4 µA  |

Table 1. Time overhead to transition from a static low power mode till executing a function.

Albeit lowering frequency reduces power consumption, it is not necessarily improving the energy efficiency. Yet, FlexClock also provides mechanisms to automatically improve energy efficiency if possible.

4.1.2 Improving Energy Efficiency

Applications targeting maximum energy efficiency can use FlexClocks capability of optimizing the clock frequency configuration at runtime, reducing the overall spent energy compared to performing the same workload at a fixed frequency setting. Potential to dynamically save energy during execution is always present when the CPU performance is not fully utilized as we briefly noted in Section 3.5 already. Tasks dominated by instructions mostly requiring access to CPU registers or random-access memory (RAM) scale well with frequency and are therefore most efficiently performed at the highest applicable frequency because minimizing execution time also reduces static loss that always occurs with the MCU being active. Contrary, tasks limited by I/O access or other asynchronous interactions execute more efficiently at a lower core frequency. Dynamic switching loss of instructions not contributing to the tasks progress is avoided in those cases which can quickly outweigh any static losses. Leveraging this potential in practice requires some way to detect those conditions at runtime. We evaluate our solution to this in Section 4.1.4.

4.1.3 The Impact of Voltage and Frequency Scaling

With FlexClock we provide means to dynamically control the performance of an MCU at runtime. The previous investigation in [Section 4.1.1] indicates the potential for energy efficiency improvements depends on task characteristics. Additionally, there are several options that influence the effectiveness of applying DVFS. We quantify how individual optimizations affect the average energy efficiency when executing the same workload. Therefore, we measure how the performance of dynamic frequency scaling (DFS), DVFS and further optimizations correspond to energy efficiency changes over the range of previously introduced instruction and memory access types.

Figure 5 shows the result of those measurements by relating frequency changes to its impact on energy efficiency. For the simple DFS case it is visible that any reduction in frequency reduces energy efficiency by more than 30 % when reducing frequency by almost 90 %. Opposed to that DVFS can significantly reduce this negative impact when switching to a lower voltage range is possible, as is the case here for 20 MHz and below. The full potential of DVFS is only utilized when flash wait state adaptation (FWSA) is enabled to reduce flash wait states according to the lower frequency. At 20 MHz this configuration is about 3 % more efficient than operating with the highest frequency. Further improvements are enabled by leveraging DVFS together with both, FWSA and automatic clock gating (ACG). This shows that even for arbitrary tasks and without applying sophisticated dynamic optimizations FlexClock can be used to improve energy efficiency by up to 10 %.

https://github.com/RIOT-OS/RIOT/releases/tag/2020.07
frequency reduction for the linear relation between frequency and current (Section 4.1.1) gives around 70% reduction in current. This puts up the question on how this additional headroom can be further leveraged in cases that do not require full CPU performance.

We address this by first establishing a baseline on how the most efficient frequency differs for different workloads and how energy consumption is affected by this. Opposed to measurements conducted in Section 4.1.1 we do not look at different instructions but workloads that differ in their proportion of computational load and asynchronous operations which can not be sped up by the core frequency. With typical examples being workloads limited by I/O-throughput.

![Figure 6. Energy consumption for performing tasks at their specific energy-optimal core frequency.](image)

We execute a set of tasks at varied frequencies and externally measure the energy spent to complete the task. This serves as our ground truth on which frequency performs a given task with the best energy efficiency. Accordingly, Figure 7 shows that more than 70% energy can be saved by the overall system if a task is most efficiently executed at a low core frequency (8 MHz in this case). It is worth noting that only DFS is applied in this case — which we previously showed to reduce efficiency if applied unconditionally to computation intensive tasks. Also, enabling dynamic voltage scaling (DVS) is expected to further improve this. This again shows that specific task properties are highly valuable information for online energy efficiency optimizations.

### 4.1.4 Assessing Performance Utilization

Tasks scale differently well with available computational performance (i.e., core frequency), as briefly mentioned before. A key component to optimize the core frequency for a specific task being executed is therefore a mechanism to assess a tasks ability and extent to speed up with higher frequencies. We further refer to this metric as performance utilization (PU).

We use FlexClock to implement a PU assessment mechanism that can be performed online on the device itself. Its basic operation principle is to instrument the execution environment (i.e., the operating system or task scheduler) to collect meta information on a task including context switching count and average CPU-time measurements. With this instrumentation in place FlexClock is used to opportunistically adapt the core frequency while collecting measurement points for the PU metric. A task that speeds up with higher frequencies is expected to show a lower average CPU time at higher frequencies and should therefore indicate a higher PU metric value.

To evaluate whether this online-assessed PU metric serves as an adequate input for automatic selection of the most energy efficient core frequency at runtime we perform experiments on our test system. With the previously established ground truth on the most efficient frequency for a given task we are able to correlate it with the new PU metric. Figure 7 displays respective results indicating a strong correlation between the performance utilization metric and the most efficient core frequency.

![Figure 7. Correlation between performance utilization metric and task specific energy-optimal core frequency.](image)

As there are several parameters that influence the accuracy of the PU metric, we look at them separately in the following with explanations on how to mitigate them. It is worth noting that the absolute error against the ground truth PU metric is not necessarily critical because individual performance measures of a task can be compared relative to each other, effectively mitigating offsets.

Figure 8 shows the count of thread activations (context switches) of a thread as the primary source of error. Not waiting for enough thread activations before calculating the PU metric can lead to substantial error with values being up to three times higher than expected. Mitigation of this error is simply to incorporate a threshold for thread activations before using task metrics for PU calculation.

Figure 9 relates the PU assessment error to individual frequency transitions used to obtain changes in task execution speed. Our experiments indicate that combining results of multiple frequency pairs reduces this error.

![Figure 8. Error of online-assessed utilization metric on number of thread activation (schedule context switches).](image)

A similar effect to low thread activation count is visible in Figure 10 for cases where not enough overall CPU-time of a
task is accumulated before the PU metric is calculated. We deliberately used a rather slow timer (32 kHz) to be compatible also with very slow clock frequencies and serve as realistic worst case baseline. It is therefore expected that this error can be significantly reduced by employing a faster timer by reducing quantization artifacts.

Combining the DVFS functions with the PU assessment enables the system to automatically adjust performance for task demands. Figure 11 shows the current profile of the MCU while executing two threads that perform different types of workloads.

One benefits of a higher core frequency (i.e., has a high PU factor) while the other is most efficiently executed at a lower frequency (respectively having a low PU value). Both threads are started directly after each other. After the task is started, a stair pattern is visible related to the execution of the automatic PU-assessment that cycles through available frequency configurations while both threads are still being executed. Following, the respective PU factors are derived for both threads and are output together with debug information via serial connection. The time of this step is heavily dominated by the serial communication with the overhead of the calculation step itself being negligible. The DFS mechanism is then enabled resulting in an over 70 % lower power consumption compared to not applying DFS. Since the DFS execution also slows down with the frequency it is easily visible that less work is performed in the same time. Despite that, the overall energy consumed for the same amount of work is reduced by almost 40 %. It is important to point out that the execution speed of the high-PU thread is not reduced as it still operates at the higher frequency. The reduction in its execution rate is related to both threads being triggered in an alternating pattern as is the case in typical producer-consumer scenarios.

4.2 FlexClock overhead

The overhead of induced by FlexClock is relevant to decide if it is applicable for specific use cases and what cost is associated to its functionality. We evaluate overhead in terms of memory and time required to perform its base operations.

4.2.1 Memory

For the memory requirement we differentiate between data and instructions and also between static and stack requirements. The clock-tree topology model with its associated descriptors and allowed configuration values mostly consist of static data. For other parts such as the clock configurator, the transition manager and the hardware specific code of the individual clock types the instructions dominate. Section 4.2.1 lists the memory overhead of different FlexClock entities.

| Entity                  | Memory Size |
|-------------------------|-------------|
| Config register descriptor | 32 bits     |
| Shared register LUT entry | single pointer |
| Zero based mux option    | single pointer |
| LUT mux option           | single pointer + value |

Table 2. Memory requirement for different FlexClock entities.

4.2.2 Clock Tree Exploration

Clock trees are, as previously described, complex in their structure and configuration. As a developer, the search for valid configurations usually requires to carefully read data sheets and reference manuals. These documents do not follow any common format or structure across manufacturers, inflicting a major obstacle for portable code. FlexClocks common interface substantially improves this by providing a unified way to explore, configure and test clock configurations interactively. For example, consider testing different clock topologies to set up a Pulse-width Modulation (PWM) peripheral for a specific frequency. Instead of reading through each specification document of involved components (e.g., the clock source, intermediate clock nodes, and other possibly affected peripherals) an interactive test application is used directly on the target device to list possible topologies and frequency setting for the given peripheral improving visibility and accessibility for developers.
Figure 11. MCU current draw when performing online performance utilization assessment, comparing automatic DFS with static high frequency operation.

Figure 12 shows how the exploration process scales with the number of possible frequency configurations. This considers exploration for every clock implemented for our target platform for all possible typologies and their respective frequency settings.

As expected, the exploration step can take considerable time because of the huge parameter space, reaching well over two seconds on our target device. Though, overhead for exploring configurations can be considered non-critical for most applications because it is expected to be executed rarely (if at all) and results can easily be cached. For example at boot there may be a phase to determine a few specific configurations which may then be cached to quickly switch between them during later operation. In many cases the exploration step could also be done completely offline. While the proposed model can also be leveraged for that in principle we define this as out of scope for this paper.

The exploration is using a simple brute-force approach that only optimizes by skipping additional steps if configurations can be ruled out based on intermediate nodes violating constraints. We chose this implementation path for several reasons. The main point is to trade runtime overhead that will not be incurred in many cases for a very simple and memory efficient implementation that can easily guarantee exploring all valid configurations. It also provides flexibility to find the best configuration for different optimization goals by simply switching between easy to implement compare functions. For cases that require faster online exploration, future work could consider replacing the brute-force variant with a faster analytical solution.

4.2.3 Time to Change Frequency

The timing requirements imposed on the different operations performed by FlexClock significantly differ. Switching between different frequencies is critical because it is expected to be applied very often – potentially each time a task is scheduled that has a PU metric that does not fit the currently configured frequency.

Figure 13. Timing overhead for simple frequency transitions performed at different clock frequencies.

Figure 14 depicts the time overhead related to individual steps of automatic clock reconfiguration and compares simple to complex transitions. The complex transition displayed uses the previously described brute-force approach to find a valid clock configuration for a given topology of 9
clock nodes. The results indicate that steps related to pre- and post-processing poses more room for improvement than frequency update procedures themselves. It also provides another indicator on why the exploration step should not be performed as part of automated DVFS and instead caching different configurations in those cases facilitates major speedups.

5 Related Work

In this section we present an overview and discussion on work closely related to our main contribution areas of generic clock configuration and its application for DVFS.

Tooling and implementations of clock configuration is no new topic as it is needed in practice. Though, existing work is either not designed for constrained devices, is vendor specific or limited to implementations without deeper systematic performance analysis being published. For example Linux provides the Common Clock Framework (CCF) which handles clock configuration in a unified platform independent way. Though, the targeted devices classes like laptops or smartphones have orders of magnitude more resources compared to tiny MCUs we are aiming for. Moreover, CCF uses the Linux approach of exploring underlying hardware at boot to dynamically load modules and configuration metadata on the clock subsystem via device tree. The implementation uses dynamic memory allocation, recursive operations, and comparatively big data structures, all of which are preferably avoided on resource constrained IoT devices we are targeting.

Simonović et al. [17] argue that a common representation of clock trees would help to mitigate the error prone manual translation from datasheets to different representations that are required by individual development teams for their specific purposes. To tackle this, they propose to avoid manual translation steps by encoding clock trees using a template-based formal language that could eventually be provided by the manufacturer. The building blocks they identified as target for their templates are mostly coherent with our findings discussed in Section 2.1. One notable semantic difference being the distinction between divisors and PLLs instead of using a generic scaler as we propose. As case study they model a rather complex multiprocessor system on a chip but do not share details on the specific application or quantitative performance results.

The huge energy savings enabled by DVFS and related topics attracted researchers in many specialized areas. On the custom chip level there are still significant advancements being made to further reduce energy consumption of chip-internal component primitives such as clock gates [20]. DVFS slowly trickles down to smaller, more constrained target devices, stretching across data centers [4], personal computers, laptops and smartphones to wireless sensor nodes [12, 2].

With D²VFS, Ahmed et al. [1] recently proposed a discrete DVFS variant that moves this further onto the intermittent device class. Their approach scales down frequency and voltage as the capacitor empties due to the MCU operation consumption. This enables an up to 9 times increase of clock cycles available for processing per active epoch, resulting in up to 300% improvement of operation time for intermittent workloads. Significant differences of our work relate to conceptual difference inherent to the intermittent application domain and our additional focus on a unified software component to manage the clock tree. Their solution limits possible frequencies to a small subset of configurations opposed to FlexClock having full control over the clock tree. D²VFS is reactive, strictly following the constraints imposed by the environment and system conditions, whereas our implementation proactively performs assessment and decisions to steer system performance towards given optimization goals.

Songfan et al. [18] also target energy utilization improvements on intermittent devices but focus on the specific aspect of efficient detection of available energy on RF-powered devices, as the availability assessment in this domain is even further constrained than for typical WSN devices [16].

Liu et al. [13] propose EA-DVFS, an energy aware DVFS approach designed for energy harvesting systems that runs tasks at an appropriate clock speed depending on momentary energy availability. They evaluate their approach on a rather powerful embedded system with a processor running up to 1 GHz. Obtained energy saving allowed them to reduce missed deadlines by more than 50%. Their work shows that depending on the context an optimal DVFS solution must consider more parameters than instantaneous power consumption, e.g., dynamic energy availability in their particular case. This underlines our argument that generic clock control should be provided as a flexible reusable tool that reflects specific application needs.

Kulau et al. [12] propose IdealVolting which leverages safety margins of the voltage level specification of manufacturers by undervolting far below the specification limits, enabling energy savings of more than 40%. They argue that common hardware does not provide integrated functionality for undervolting and therefore add external hardware for voltage scaling. In this work we do not aim for undervolting below recommended specification limits and employ hardware with integrated voltage scaling capability. Their work further indicates that undervolting requires clock recalibration, supporting the relevance of generic clock configuration for address this.

Antonio et al. [2] aim for a programmable power management on WSN-class devices that controls DVFS and power gating on the chip level. They design and evaluate a custom CPU based on an open-source 16-bit processor library.
and integrate clock gating and DVFS. As a result they reduced energy consumption of typical WSN workloads by up to 38% for the overall system. Their work is orthogonal to ours as they look into the impact of automatic DVFS being implemented in hardware with a custom design on the register-transfer level. We instead focus on improved software management and control for devices that already provide features for power gating and DVFS. Since devices with those capabilities are becoming more widely available we investigate how this functionality can be uniformly exposed to software layers, bridging the gap between specific hardware capabilities and energy-aware software.

Powell et al. note an increased importance of DVFS in context of body area sensor networks (BASN)s as high energy demands for data transmission advocate for moving processing to the edge, demanding more efficient operation. They analyze the efficiency of DVFS on a commercial off-the-shelf (COTS)-device using a Parkinson tremor detection application that reduces transmissions by pushing processing to the node. Their contribution supports the relevance of our approach with their practical application showing a common problem of general DVFS applicability: after each frequency change they had to manually compensate the Inter-Integrated Circuit (I2C) bus configuration for the new core frequency. Once again providing a practical example for better software support on generic clock control being required to properly manage the side effects of the potentially deeply intrusive actions of DVFS.

6 Conclusion and Outlook

In this paper, we proposed FlexClock as an approach for generic online clock reconfiguration that suits constrained IoT devices. We reduced the complexity of clock dependencies by modeling clock trees as simple reusable base components with a memory efficient way for encoding configuration parameters and constraints. Based on this lean model, we could master the challenges of dynamically exploring and changing clock trees at runtime.

FlexClock eases the implementation of hardware agnostic methods for controlling computation performance and optimizing peak power consumption as well as energy efficiency. Our evaluation revealed a significant potential for online self-adaptation by automatically assessing a performance utilization metric. FlexClock can leverage these potentials.

Our further evaluations concerned overhead and sources of error, which we systematically explored and analyzed. Results provide insights on how performance is affected by individual parameters and how they can be tuned. Comparison with related work confirms that FlexClock fills a gap between complex, hardware-specific configuration and dynamic power management in software, which aims for saving energy wherever possible.

In this work, we already demonstrated how the current implementation of FlexClock can be used to realize a fully automatic DVFS mechanism running on a real system. Future directions of this research are threefold. First, insights and optimizations of our algorithms shall be learned from a supervised long-term deployment. Second, processes that harvest entropy could leverage direct access to clock parameters and metadata for improving accuracy of entropy estimation or generating cryptographically secure random numbers. Third, topics related to clock calibration and synchronization open another research domain that can fundamentally benefit from our generalized, hardware-agnostic access to the clock configuration. As clocks are the critical component for timekeeping and signal generation, we envision manifold applications and use cases thereof.

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