Modeling and Analysis of Switched-Capacitor Converters as a Multi-port Network for Covert Communication

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Abstract—Switched-capacitor (SC) DC-DC voltage converters are widely used in power delivery and management of modern integrated circuits. Connected to a common supply voltage, SC converters exhibit cross-regulation/coupling effects among loads connected to different SC converter stages due to the shared components such as switches, capacitors, and parasitic elements. The coupling effects between SC converter stages can potentially be used in covert communication, where two or more entities (e.g., loads) illegitimately establish a communication channel to exchange malicious information stealthily. To qualitatively analyze the coupling effects, a novel modeling technique is proposed based on the multi-port network theory. The fast and slow switching limit (FSL and SSL) equivalent resistance concepts are used to analytically determine the impact of each design parameter such as switch resistance, flying capacitance, switching frequency, and parasitic resistance. A three-stage 2:1 SC converter supplying three different loads is considered as a case study to verify the proposed modeling technique.

Index Terms—Switched-capacitor converter, covert communication, coupling, modeling, multi-port network.

I. INTRODUCTION

COMMUNICATION channels can be classified into two types such as overt and covert. An overt channel is legitimate and can be obvious to other entities, whereas a covert channel is established between malicious entities to potentially enable transmission of unauthorized content. An example of such content could be sensitive information such as a secret key that is used for encryption and decryption algorithms. The entities could refer to hardware components (e.g., cores of the processor) and/or software applications. In a communication channel, the information is transmitted from one entity to another. The transmitting and receiving ends are often referred to as source and sink, respectively.

The communication medium can be a hardware or software resource that is shared between the source and sink. For instance, a covert communication can be established through the power management units, which control voltage level and operating frequency. A covert channel attack among FPGAs, CPUs, and GPUs that are connected to the same power supply unit, is proposed in [1]. By modulating the core frequency with dynamic frequency scaling (DFS) technique, a covert channel can be established in a multi-core platform [2]. The use of dynamic voltage and frequency scaling (DVFS) allowed to create a covert channel in a TrustZone-enabled system-on-chip (SoC) [3]. Information leakage is enabled by infecting power management unit with a hardware Trojan in the multi-core SoC in [4]. The power budget constraint [5], [6], current management mechanisms [7], and switching noise modulation [8] of power delivery network (PDN) can also create the covert communication between cores of the processor.

Similar to the aforementioned circuit and system components that are shared by multiple entities and used for covert communication, on-chip voltage regulators (VRs) and PDN are also shared by multiple entities and can therefore be used as a communication medium. SC converters are widely used as on-chip VRs in modern integrated circuits (ICs). One of the primary parameters of an SC converter is the equivalent resistance, which characterizes the average ohmic losses. The equivalent resistance is a function of the switch resistance, flying capacitance, switching frequency, duty cycle, and parasitic elements such as equivalent series resistance (ESR) and equivalent series inductance (ESL) [9], [10]. SC converters may share certain components such as switches and capacitors among different entities. Coupling effects of one entity can therefore be observed from another entity. The variations in one of the outputs of an SC converter can cause an observable change in the performance of the another output and vice versa. The coupling effects are investigated in dual- and multi-output SC converters by extending the notion of equivalent resistance in [11], [12].

Although the concept of covert communication between different cores of a processor sharing the same PDN has been demonstrated in [6]–[8], no analytical modeling, which could assess the implications of system parameters and configurations on the bandwidth of covert communication, has been proposed in the literature. A new modeling technique of SC converters that can be used to characterize the covert communication capacity among different circuit entities that share a common PDN is proposed in this paper. By using the concept of multi-port network, the cross-regulation/coupling effects among different load circuitry, which are powered by different stages of SC converters, are characterized.

This paper is organized as follows. The threat model which can be used to establish the covert communication between cores of the processor is presented in Section II. A generalized multi-port network modeling technique that can be used to analyze SC converter covert communication with analytical calculations is proposed in Section III. The accuracy of analyt-
ical modeling technique is verified with extensive simulations in Section IV. The conclusions are drawn in Section V.

II. THREAT MODEL

In the threat model (Fig. 1), two or more entities (e.g., cores, applications, or programs) such as source and sink would like to establish the communication channel. Assume that the source entity has access to sensitive information while the sink entity has access to the network. A common practice to protect the sensitive information is to locate the source in a Trusted Execution Environment (TEE). No overt communication channel can therefore be established between the source and sink.

Due to the shared PDN, it is possible to establish the covert communication channel between cores [6], [8]. As shown in Fig. 1, the power can be delivered and regulated by on-chip VRs. Depending on the architecture of the microprocessor, the VRs can be connected to the cores in different configurations. Certain designs can have a dedicated VR for each core (highlighted in dashed line in Fig. 1). For instance, Qualcomm Snapdragon 800 supports per core DVFS, i.e., there is one VR per each core to control voltage [13]. Alternatively, some implementations can have less number of VRs such that cores are organized in clusters, where each cluster has a dedicated VR. As an example, the ARM big.LITTLE architecture has two clusters of high performance and low power cores [14].

A communication signal can be sent by the source through the PDN by varying the load from heavy to light conditions. This can be implemented by pinning the application to a specific core that could run in either high performance or idle (sleep) modes to encode logical 1 and 0, respectively. Due to the coupling effects (i.e., shared components in PDN), the variations in the load at the source side propagates to other cores. Therefore, the sensitive information can be leaked from the source and sensed by the sink(s).

The variations in load primarily affect the core voltage. In order to decode the signal sent from source, the sink should be able to measure the voltage level with certain sensors. One possible way to measure the variations in voltage could be performed by using the critical path monitor (CPM) sensors, which can be found in, e.g., IBM POWER7+ multicore processors [15]. The CPM sensors detect changes in the timing margin of guardband scheduling. The output of CPM sensors is typically in near-linear relationship with core voltage [16]. In POWER7+ processor, each core has five CPM sensors, which can be accessed with IBM AMESTER software [17].

The operating frequency of each core can have a significant impact on the operation characteristics of respective VRs such as the output voltage and switching frequency. As a result, it is important to select the core frequency in such a way to maximize the bandwidth of the communication channel. The operating frequency of each core is usually controlled by phase-locked loops (PLLs), as shown in Fig. 1, and the frequency of each core can be controlled by software. E.g., Operating Systems (OS) based on Linux have CPUfreq software, which can set the frequency for each core. This software can be accessed with the kernel privileges to implement the attack [2], [4]. Additionally, the location of the source and sink significantly affects the bandwidth of communication signal due to the different level of coupling between cores. A novel modeling technique that accounts for the location of source and sink, core frequency, and other parameters so as to increase the bandwidth of communication signal is proposed in this paper.

III. GENERALIZED MULTI-PORT NETWORK MODEL

This paper focuses on a common type of SC converters used in microprocessor applications called multi-phase SC converters. In multi-phase SC converters, multiple single-output SC converters are used in parallel to supply loads. For example, [18] proposed a 123-phase SC DC-DC converter-ring for microprocessor applications.

A multi-phase SC converter with two stages can be viewed as a two-port network, where each stage supplies a separate load. Moreover, this modeling can be generalized to the multi-port network, where the multi-phase SC converter with N number of stages is providing power to N different loads, as illustrated in Fig. 2. The parasitic resistance, $R_{par}$, is added to account for the location of SC converter stage and its load with respect to the input voltage source. The equal parasitic resistance is chosen to simplify further derivations. Note that $R_{par}$ can have different values.

A. Generalized formulas

The multi-phase SC converter with N number of stages that provides power to N number of loads can be modelled as an
Fig. 2. Multi-phase SC converter with $N$ number of stages supplying $N$ different loads.

$N$-port network, where the average output voltages and load currents can be written as

$$
\begin{bmatrix}
V_{OUT1} \\
V_{OUT2} \\
\vdots \\
V_{OUTN}
\end{bmatrix} =
\begin{bmatrix}
V_{TR1} \\
V_{TR2} \\
\vdots \\
V_{TRN}
\end{bmatrix} -
\begin{bmatrix}
R_{11} & R_{12} & \cdots & R_{1N} \\
R_{21} & R_{22} & \cdots & R_{2N} \\
\vdots & \vdots & \ddots & \vdots \\
R_{N1} & R_{N2} & \cdots & R_{NN}
\end{bmatrix}
\begin{bmatrix}
I_{OUT1} \\
I_{OUT2} \\
\vdots \\
I_{OUTN}
\end{bmatrix}
$$

where $V_{OUTi}$ is the average output voltage and $V_{TRi}$ is the target (no load) output voltage of $i^{th}$ terminal. For the load resistance of the $i^{th}$ terminal, $R_i$, the average output currents are determined by $I_{OUTi} = V_{OUTi}/R_i$.

In R-parameters matrix, intuitively, the $R_{ij}$ represents the amount of coupling from the $j^{th}$ load to the $i^{th}$ load. Therefore, the non-diagonal elements are of the primary parameters to analyze the coupling effects. It should be noted that the dimensions of matrices in (1) depend only on the number of loads. This means that the number of SC converter stages does not have to be $N$ (i.e., several converters may supply the same load).

Additionally, the location as well as the number of the input voltage sources can be different (i.e., distributed power supply [19], [20]), which also does not change the dimension of the matrices. The change in the input voltage location and/or the number of SC converter stages and input voltage sources will only change the values of the elements of R-parameters matrix.

**B. Analytical modeling**

To determine the analytical expressions of R-parameters, one should short-circuit the input voltage source and substitute loads with controllable voltage sources ($V_{Sj}$). In this setup, the effect of the filter/output capacitors is neglected, which is an appropriate assumption because the filter capacitors are usually much larger than the flying capacitors. As a result, (1) can be re-written as

$$
\begin{bmatrix}
I_{OUT1} \\
I_{OUT2} \\
\vdots \\
I_{OUTN}
\end{bmatrix} =
\begin{bmatrix}
Y_{11} & Y_{12} & \cdots & Y_{1N} \\
Y_{21} & Y_{22} & \cdots & Y_{2N} \\
\vdots & \vdots & \ddots & \vdots \\
Y_{N1} & Y_{N2} & \cdots & Y_{NN}
\end{bmatrix}
\begin{bmatrix}
V_{S1} \\
V_{S2} \\
\vdots \\
V_{SN}
\end{bmatrix}
$$

Each element of the Y-parameters matrix can be found as

$$
Y_{ij} = -\frac{I_{OUTi}}{V_{Sj}}; V_{Sj} = 0, k \neq j \quad (i, j, k \in \{1, 2, \ldots, N\})
$$

where $V_{Sj}$ is the voltage source connected to the $j^{th}$ output terminal and $V_{Sk}$ is a voltage source of zero value connected to the remaining output terminals. In this way, the Y-parameters matrix (Y) are determined, which then can be transformed into R-parameters matrix (R) by inversion as

$$
R = Y^{-1}.
$$

Since the value of voltage sources are controlled and known, the main goal is to find the output current expressions. This can be achieved by assuming either slow switching limit (SSL) or fast switching limit (FSL) operation modes based on the switching frequency.

As a case study, let us consider a three-stage 2:1 SC converter, which is shown in Fig. 3. Each stage of this circuit operates in two phases (charge and discharge) while producing $N = 3$ output voltages that are equal to half of the input voltage.

In FSL approximation, the switching period is quite small (i.e., the switching frequency is large), allowing the capacitors to behave as a constant DC voltage sources because there is not enough time to charge or discharge within one switching sub-interval [21]. By following the proposed methodology, the FSL R-parameters matrix can be written as

$$
R_{FSL} = \begin{bmatrix}
R_{par} + 2r & R_{par}/2 & R_{par}/2 \\
R_{par}/2 & 3R_{par}/2 + 2r & R_{par}/2 \\
R_{par}/2 & R_{par}/2 & 2R_{par} + 2r
\end{bmatrix}
$$

From (5), the non-diagonal terms are the functions of corresponding parasitic resistance values. This means that the coupling effect is only due to the parasitic resistance ($R_{par}$), and the switch resistance ($r$) values do not have an impact on the coupling. Such observation can be explained with the fact that SC converter stages share only the parasitic resistance between each other. In other words, the charge that is provided to each load is flowing through certain parasitic resistances that
are common to some or all loads depending on the configuration. In contrast, the charge that is flowing to a particular load depends only on the switch resistance of that load (i.e., it does not depend on the switch resistance of other loads because the charge is not flowing through them). Furthermore, it can be observed that $R_{12} = R_{21}, R_{13} = R_{31}, R_{23} = R_{32}$. This means that the pair of outputs/loads affect each other in the equal amount. Therefore, the covert communication may exist in two directions. Additionally, (5) shows that the cross-regulation/coupling effects between the second and third loads are two times larger than in the first-second and the first-third pairs. This behavior is caused by the location of the SC converter stages with respect to the input voltage source. Since the second and third loads are located the farthest from the input voltage source, the amount of coupling is the largest between them. The larger amount of coupling corresponds to a larger bandwidth of covert communication. Therefore, it is important to find the pair of loading conditions that lead to the largest coupling to maximize the bandwidth of covert communication channel.

In SSL approximation, the switching period is quite large (i.e., the switching frequency is small) such that the capacitors in an SC converter have enough time to completely charge or discharge within one switching sub-interval [21]. In this case, the switch resistance can be approximated to be zero. By following the proposed methodology, the SSL R-parameters matrix can be written as

$$R_{SSL} = \begin{bmatrix} \frac{1}{4Cf} & 0 & 0 \\ 0 & \frac{1}{4Cf} & 0 \\ 0 & 0 & \frac{1}{4Cf} \end{bmatrix}.$$ 

(6)

As shown in (6), all non-diagonal terms are zero. This means that during the SSL operation mode (low switching frequency), there is no coupling effect between loads.

IV. SIMULATION OF COVERT COMMUNICATION

In this section, the covert communication among the individual stages of a three stage SC converter is investigated. In Section IV-A, the simulation setup is explained and the results are compared with proposed analytical modeling. In Section IV-B, the communication is established in a more practical circuit setup considering parasitic resistance of PDN between off-chip VR and on-chip SC converter stages, parasitic capacitances, and switching noise inserted by other circuitry.

A. Comparison of analytical modeling with simulations

To establish a covert communication channel, the same circuit used in the case study is chosen (Fig. 3). The simulation parameters are listed in Table I. Switches are designed in 28 nm FDSOI process. One way to control the output current is to vary the load resistance. By setting the load resistance to 100 $\Omega$, the output current becomes very small in the order of 10 mA. Similarly, at the load resistance of 15 $\Omega$, the output current is in the order of 50 mA. These values are specifically chosen for the circuit parameters (Table I). Let us assume that bit ‘1’ is encoded when the load resistance is 100 $\Omega$ while bit ‘0’ is encoded when the load resistance is 15 $\Omega$. Alternatively, a ‘1’ is sent by reducing the workload and therefore current consumption and ‘0’ is sent by increasing the workload in the source entity. At the same time, the sink is assumed to have a load resistance of 100 $\Omega$. A covert communication throughput of 2 Mbits/s is obtained in the simulations with a potentially higher bandwidth. The bandwidth depends on the response time of SC converters. If the communication throughput is selected to be higher than the channel bandwidth, SC converters will not be able to respond to the change in load, and in turn no meaningful communication would be established between the source and sink.

The output voltage waveforms for each load at a switching frequency of 200 MHz (FSL mode) are shown in Fig. 4. In this case, the information is sent from the source by changing the value of load $R_1$. The signal propagation from the source to the sinks can be observed. For example, in Fig. 4, the amplitude variation of signal at the source side (i.e., at the output of first SC converter stage) is approximately 115 mV, whereas the amplitude variation of the received signal is 23 mV at the second and third SC converter stages.

To quantify the coupling effects and communication bandwidth, the amplitude variation of the voltage ($\Delta V$) is measured. After that, the change in two values is recorded. Particularly, the average voltage at the output and input nodes of SC converter stages is measured over the time period when the bit ‘0’ and bit ‘1’ are transmitted. Note that this time period corresponds to the steady-state operation region of SC converter (i.e., the response/transient time is not considered).

| Parameter | Value |
|-----------|-------|
| Input voltage $V_{IN}$ | 2 V |
| Flying capacitance $C_1, C_2, C_3$ | 1 nF |
| Filter/load capacitance $C_{O1}, C_{O2}, C_{O3}$ | 10 nF |
| Parasitic resistance $R_{par}$ | 1 $\Omega$ |
| Switching frequency $f$ | 200 MHz |

Fig. 4. Output voltage waveforms at the switching frequency of 200 MHz. The information is sent from the first SC converter stage by varying $R_1$. |
The amplitude variation of voltages at various nodes when the information is sent from load $R_1$, $R_2$, $R_3$ is shown in Fig. 5. The amplitude $\Delta V$ for each node increases with switching frequency of SC converter and then saturates at FSL region, where the coupling effects are the largest (5).

From Fig. 5(a), the changes in workload of the source entity located in the first SC converter stage (i.e., $R_1$) induces the same changes in voltage of sink entities located in the second and third SC converter stages. Particularly, $\Delta V_{OUT2} = \Delta V_{OUT3}$ and $\Delta V_{IN2} = \Delta V_{IN3}$. This can be explained with the fact that $R_{32} = R_{31}$ in (5). From Fig. 5(b), the changes in workload of the source entity located in the second SC converter stage (i.e., $R_2$) induces approximately two times larger changes in voltage of the sink located in the third SC converter stage compared to voltage changes of the sink located in the first SC converter stage. Particularly, $\Delta V_{OUT3} = 2\Delta V_{OUT1}$ and $\Delta V_{IN3} = 2\Delta V_{IN1}$. This is due to the fact that $R_{32} = 2R_{12}$ in (5). With a similar reasoning (i.e., $R_{23} = 2R_{13}$), the changes in workload of the source entity located in the third SC converter stage (i.e., $R_3$) results in the following relation: $\Delta V_{OUT2} = 2\Delta V_{OUT1}$ and $\Delta V_{IN2} = 2\Delta V_{IN1}$ (Fig. 5(c)).

Therefore, the developed analytical model (5) can successfully predict the relative impact of one entity on another entity. In this way, an adversary may choose the locations of the source and sink such that the coupling effects are maximized. In this case study, the highest coupling effects exist between the second and third SC converter stages.

### B. Simulation considering practical design choices

In this subsection, the covert communication channel is established in more realistic circuit setup. First, the parasitic resistance $R_{par}$ is modeled as an effective grid resistance. In Fig. 6, $R_{grid}$ represents a section resistance of PDN with a grid structure which is common in modern ICs, $R_{ver}$ is the resistance between the grid and SC converter stage, and $R_{off-chip}$ is the off-chip resistance. This structure models the PDN between off-chip VR and on-chip SC converter stages. $R_{off-chip} = 1 \, \Omega$, $R_{ver} = 0.1 \, \Omega$, $R_{grid} = 0.6 \, \Omega$ are chosen to allow around 200 mV voltage drop at the output of SC converter stage in the worst case scenario, which corresponds to the 20% of maximum (ideal) output voltage.

The individual stages of a 2:1 SC converter is assumed to have the same circuit structure as shown in Fig. 3. The only exception is that the top and bottom plate parasitic capacitances are added for each flying capacitance. Particularly, 1% and 5% of flying capacitance are used to model the top and bottom plate parasitic capacitances, respectively (i.e., 10 pF and 50 pF) [22]. Additionally, the transistors are simulated in 28 nm FDSOI process similar to Section IV-A.

In a practical setting, the switching noise caused by other circuit blocks may induce certain fluctuations in the PDN which in turn may degrade the covert channel. To model this effect, the switching noise is added at each load. This is realized with a linear-feedback shift register (LFSR) which acts as a pseudo random number generator. Depending on its bit sequence, a random amount of load is consumed at certain time instances creating switching noise. The switching noise of approximately 20 mV is added to each load, which corresponds to 2% voltage variation with respect to ideal output voltage. Such a value is chosen because in the threat model it is assumed that the attacker could pin a certain application to a specific core and, hence, control the switching activity to a certain degree (see Section II for more details).

Note that the switching noise degrades the received signal quality (i.e., average amplitude variation of output voltage at the sink side) by approximately 3-4 mV, which is lower than the original 20 mV. Therefore, the effect of switching noise can be reduced by sampling multiple measurements and estimating the average value. However, this may result in the lower throughput.

Three SC converter stages and loads are placed in such a way to have the similar relationship of resistances as shown in Fig. 3. As a result, by using the previous analysis in Section IV-A, it can be argued that the strongest communication channel can be established between the loads #2 and #3 (see Fig. 6 for notation). For more precise values, one may calculate the effective resistances between nodes and re-calculate the R-parameters matrix to determine the largest coupling.

As shown in Fig. 7, where the information is sent from the third SC converter stage (i.e., load #3 in Fig. 6), the received bit signals could still be distinguished. The amplitude voltage variations are determined by finding the difference in the average values when the bit is ‘0’ and ‘1’. The variations in the output voltage values are estimated to be $\Delta V_{OUT1} = 29.3 \, \text{mV}$, $\Delta V_{OUT2} = 36.8 \, \text{mV}$, and $\Delta V_{OUT3} = 106.8 \, \text{mV}$. Since $\Delta V_{OUT1} < \Delta V_{OUT2}$, it is confirmed that the largest coupling exists between the loads #2 and #3. As discussed in Section II, the IBM POWER7+ multicore processors [15], [23] may use CPM sensors to detect changes in voltage. Particularly, the CPM sensors have a resolution of 21 mV. In Fig. 7, the throughput is equal to 2 Mbits/s. However, because of the sensor limitation, e.g., CPM sensor can sample every 32 ms, the actual throughput may be limited to 31 bits/s.
In this work, a novel covert communication channel between SC converter stages which share the same PDN is introduced. This vulnerability could be used to establish an inter- or intra-core covert communication channel. By using the proposed multi-port network modeling technique, the bandwidth of covert communication channel between different entities is analyzed. In particular, the impact of circuit components such as switch resistance, capacitance, switching frequency, parasitic resistance, off-chip resistance, and location of source and sink is investigated with the proposed analytical model. This model can be used both by an attacker to increase the coupling or a circuit designer to minimize the coupling. As a case study, a three-stage 2:1 SC converter is used to demonstrate the effectiveness of the proposed modeling technique. The analytical model is verified with extensive simulations.

V. CONCLUSION

Fig. 6. Simulation setup that utilizes 28 nm FDSOI transistor models and considers the PDN parasitic impedances for the covert communication.

Fig. 7. Output voltage waveforms at the switching frequency of 200 MHz with added parasitic capacitances and switching noise at loads. The information is sent from the third SC converter stage.

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