Input Current Ripple Reduction in a Step-Up DC–DC Switched-Capacitor Switched-Inductor Converter

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ABSTRACT This paper presents research results related to the concept of a high-voltage-gain DC-DC converter with a low input current ripple. In the proposed topology, a low-volume DC-DC switch-mode boost converter operates in parallel with a switched-capacitor voltage multiplier (SCVM). The overall converter achieves a four-fold voltage gain, but the voltage stress of the transistor and the diode of the boost converter is only half of the output voltage. This is achieved by applying the specific topology of the proposed converter. Furthermore, the boost part uses a low-volume choke as it operates in the discontinuous conduction mode (DCM). The parallel operation of the boost converter and the SCVM decreases the current stress in some components of the multiplier. This paper presents a concept of the hybrid converter, an analytical model for the selection of components and switching parameters, an efficiency model, and the verification of the converter operation through simulation tests and experiments.

INDEX TERMS DC–DC converter, switched-capacitor, high-gain converter, boost converter.

I. INTRODUCTION
DC-DC conversion based on switched-capacitor (SC) circuits allows a high-voltage-gain converter [1] to be achieved that can be optimized for low volume or high efficiency. One of the major problems of the switched-capacitor (SC) DC-DC converters is their pulsating input current. The input current ripple is associated with the method of operation of the SC circuits that is based on the charging and discharging of the switched capacitors in various configurations. This is clearly seen in SC voltage multipliers [2]–[4], such as a classic multiplier discussed in [2], or the converter presented in [3], where the input current can be approximated by a rectified sinusoidal shape. In other types of SC series-parallel converters, like those presented in [4], the input current is even deteriorated by zero-current periods that occur between the sequences of pulses, or an inequality of pulses occurs [5].

A low-ripple input current is especially important in some applications. In photovoltaic systems (PV), the input current ripple may affect the Maximum Power Point (MPP) operation quality. In [6]–[11], high-voltage-gain converters with SC circuits are proposed for renewable energy systems, where the problem of input current ripple is overcome by the topology and control concept. In [6], high voltage gain is generated by voltage multipliers which extend the boost converters, and low voltage ripple level is ensured by the interleaved operation of the units. The single unit is composed of a boost converter and a multiplier in series connection. Publication [7] presents a solution of a high-voltage-gain converter, where the topology of the converter allows to achieve continuous input current and utilizes two inductors of 1.96 mH and 1.35 mH. The interleaved technique used in the DC-DC converter concept for renewable energy systems is presented in [8]–[10]. The mentioned topologies combine SC circuits and switch-mode operation with the use of inductors and can be optimized toward a low number of switches. In [11], a charge pump and coupled inductors are used for high step-up DC-DC conversion in a photovoltaic AC module with voltage gain in the range of 2.9 to 10. The converter has low volume and is built using a transformer with magnetizing inductance of about 24 µH, one transistor, and three diodes. However, the input current ripple is not reduced as much as in the converter proposed in this paper. The application of high-voltage-gain converters with SC and switched-inductor (SI) circuits is also proposed for fuel cell applications in vehicles [12], [13].

The concept of interleaved technique is a common method that allows for a decrease in the input current ripple of a
converter. It is demonstrated in [8]–[10] for renewable energy applications, but also in articles [14]–[20], which present high-voltage-gain converters with SC circuits. The converters proposed in [14]–[17] are built as a hybrid switched-capacitor/switched-inductor (SC/SI) structure with inductors on the input side. This allows for a decrease in the input current ripple by the utilization of the proposed topology and control concept, as well as the use of the SC structure for adequate voltage gain achievement. In [14], cancelation of the input current ripple is demonstrated, and the experiments were carried out with inductors of 140 µH and 330 µH.

In references [18]–[23], an interleaved operation of pure SC converters is presented. In [18] and [19] the charging and discharging states of the switched capacitors in parallel connected units, as well as the connection to the load, are phase shifted. From the input current quality viewpoint, this gives a substantial reduction in the ripples. The high-gain converter with improved efficiency presented in [20] uses distributed stray inductances and operates in an interleaved SC structure with a common input and output capacitor, resulting in a reduction in current ripple. In [21], a step-up converter based on the interleaved operation of the SC and the boost parts is presented. It ensures a reduction in the ripple of the input current. Furthermore, on the output side each part charges one of two series capacitors which gives the output voltage control by the boost converter. The resonant SC converter presented in [22] can also operate in an interleaved mode. The benefit of the input current ripple reduction was explained in the case of the voltage multiplier, which uses very small resonant inductors. In [23], a converter with series output capacitors charged in an interleaved mode by SC circuits is demonstrated. The application of very small inductances allows one to operate with oscillatory currents in front of each SC unit. An adequate phase shift of the currents gives a significant ripple reduction in the input current of the converter. The hybrid converter proposed in this paper exhibits a lower number of switches compared to concepts presented in [20]–[23], which is presented in more detail further in this article. In [24], some topologies of automatic interleaved Dickson switched-capacitor converters are presented. The converter uses two transistors and circuits composed of diodes and capacitors, as well as a low-volume inductor in the resonant topology.

In the demonstrated case of the converter with triple voltage gain, the input current ripple achieved is below 10%.

Another concept for input current ripple cancelation in a high-gain DC–DC converter with an SC structure is presented in [25]. The converter uses an input choke and auxiliary L and C components in a circuit that absorbs the AC component of the current. The application of DC–DC switch-mode circuits integrated with the SC structure allows design of a high-voltage-gain converter with regulation possibility, as shown in [26], where various types of converters with an inductive storage cell are presented. In a converter with an input DC–DC boost part, the input current ripple can be decreased compared to those of a classic boost converter or a pure SC converter. The conduction losses and voltage stress across the components of the boost converter are also reduced. Various examples of hybrid converters that integrate SC and switch-mode circuits are presented in [26]–[32]. Further positive qualities such as low component count, high voltage gain, and output voltage regulation ability can be found in these concepts. In some cases, the input current ripple is significantly reduced, which is demonstrated in a converter equipped with an inductor of 220 µH [26], and in that with inductors of 1.1 mH and 0.55 mH [30].

The hybrid converter presented in this paper allows a significant reduction in the input current ripple by an active switch-inductor (SI) part operating in parallel to a specific SC converter. It utilizes an additional switched-inductor circuit with a very low inductance compared to those used in the majority of hybrid SC/SI converters presented in the literature. This is one of the very positive characteristics of the converter presented. Furthermore, the operation of the SI converter decreases current stress in some SC circuits, allowing for a decrease in its losses and volume. The next advantage is seen in the size of the components for the SI converter. It operates in the boost topology and converts the energy from the input capacitor to an internal capacitor in the SC converter where the voltage is equal to half of the output voltage. This is possible thanks to the application of the innovative SC topology [3], which finally allows the design of an SI converter for low voltage stresses of their devices. The SI part used in the proposed hybrid converter requires a very low choke inductance, as the boost converter operates in the DCM mode with a voltage gain of less than two. This is an advantage compared to the majority of switch-mode or hybrid converters that use chokes of substantial volume.

In the proposed parallel configuration, the output capacitor of the switch-mode converter is charged by the SC circuit as well. Since the switch-mode converter operates with a low duty cycle, it does not regulate the output voltage, and the whole converter operates as a voltage multiplier with a constant four-fold voltage gain.

The major contribution of the paper lies in the analytical determination of the parameter components, switching strategy, power sharing between the SC and boost (SI) parts of the converter, and an analytical model of efficiency, as well as in computer simulations and experimental verification of the converter operation and its efficiency. Together with the previously published conference paper [34], this work introduces a novel topology of the high-gain DC–DC step-up converter with reduced input current ripple achieved by a parallel operation of an SCVM converter and a switch-inductor circuit equipped with a low-volume inductor.

The proposed hybrid converter maintains the favorable qualities of SC converters [1]–[5], such as high voltage gain, simple control, high efficiency, high power density, and minimization of the values of the magnetic components, which can lead to the elimination of ferrite cores from the design.

The input current ripple can be filtered by passive input circuits. This typical approach requires the use of LC components of adequate volume. However, these circuits can affect
the transient response of the converter and should be designed with consideration of the dynamic behavior of the closed-loop control system.

This paper is organized as follows. Section 2 introduces the concept of the proposed converter, and its subsections contain analytical models useful for the selection of the converter components. Section 3 presents the results of the computer simulation and the determination of the current stresses of the SC converter components that are useful for the efficiency model demonstrated in Section 4. The operation of the converter and the efficiency model have been confirmed by experiments, whose results are presented in Section 5. All results obtained here lead to the positive conclusions described in the last section of this paper.

II. CONCEPT OF THE HYBRID CONVERTER

The concept of the proposed hybrid converter is presented in Fig. 1 in [34]. The converter is composed of a specific switched-capacitor voltage multiplier (SCVM) [3] and a switch-mode boost converter that directs its inductor current to an internal capacitor of the SCVM. The input current of the SCVM converter is composed of pulses, as in the classic converter presented in [33]. Therefore, the current of the parallel switch-mode boost converter should fill the gaps between the pulses. The appropriate mode of operation is the DCM, where the current of the boost converter is composed of triangle pulses with a phase shift in relation to the SCVM current. The shift time is adjusted to ensure that the boost converter pulse is exactly in place of the gap in the SCVM current.

A. VOLTAGE GAIN

The concept of the proposed converter assumes that the operation of the SC multiplier determines the total voltage gain, and the switch-mode converter allows for cancelation of input current ripple and reduction in current stress of the components of the SCVM.

The SCVM operates in a two-stage mode presented in Fig. 2. In the first stage, the capacitor \( C_1 \) is being charged from the source, and the capacitor \( C_3 \) is being charged from \( C_2 \). The voltage across capacitor \( C_2 \) is determined by the configuration in the second stage of operation where capacitor \( C_2 \) is being charged from \( C_1 \) and the source connected in series. The average voltage on capacitor \( C_1 \) is equal to \( U_{in} \) and that on capacitors \( C_2 \) and \( C_3 \) is \( 2U_{in} \). Such an operation ensures that the output voltage is maintained at a constant level equal to about \( 4U_{in} \) and the voltage on the internal capacitor \( C_2 \) at a level equal to about \( 2U_{in} \). Therefore, the boost circuit, composed of elements \( S_b, D_b, \) and \( L_b \), operating in the DCM mode with the duty ratio \( D < 0.5 \), charges the capacitor \( C_2 \), but does not significantly affect the converter voltage gain, which is equal to \( G_U \approx 4 \).

B. THE INPUT CURRENT RIPPLE REDUCTION

The SC and SI subcircuits can be controlled independently. The main positive characteristic of the proposed hybrid converter is the ability to reduce the input current ripple. To achieve the appropriate phase shift between both components of the input current, the control of both subcircuits should be adequately synchronized. From Fig. 4, it is seen that the pure SC converter [3] operates with pulses of its input current. It can be filtered by passive circuits on the input, but in connection with the SI circuit, the problem of the input current ripple is significantly decreased (current \( i_{in} \)).

Figure 4 presents the operation concept of this converter, which is based on adequate switching of the SI circuits with respect to the SC part. The input current of the boost converter \( (i_{inb}) \) reaches its maximum at the time when the SCVM current \( (i_{ins}) \) reaches zero. It is not required to add any current to the SCVM current \( (i_{ins}) \) at the time when it reaches its maximum; therefore, the boost converter operates in the deep DCM mode using a low-volume choke.

It is also important that the operation of the SI part allows a decrease in the energy converted by the SCVM and the current stresses of components \( S_1, S_2, D_1, D_2, L_1, \) and \( C_1 \).
C. SELECTION OF PARAMETERS OF THE SCVM PART
The LC parameters of the SCVM converter are determined by the output power, the switching frequency, and the requirements for the resonant choke design. The energy is transferred by the switched capacitors, but the resonant inductor is required to avoid inrush currents in the SC circuits. It is justified to use a stray inductance or an air-based choke for this purpose. The aforementioned energy can determine the resonant inductance $L_i$ ($i = 1 - 3$). The design of the LC circuits in the SCVM can be achieved in the steps presented in Table 1. The issues of selecting LC components in SCVM converters are analyzed in [2] and [33].

After selecting $L_i$ and $f_S$, the capacitance $C_i$ ($i = 1 - 3$) is adjusted to achieve the resonant frequency close to the switching frequency. The presence of dead time increases conduction losses in the SCVM converters and should be minimized. The selected capacitance $C_i$ can be oversized from a converter power viewpoint. Under such conditions, the capacitor $C_i$ is not fully discharged in a switching cycle, but operates with a voltage ripple. The power limit of the SCVM depends on the parameter $C_i f_S$, which is presented in [33].

D. SELECTION OF PARAMETERS OF THE BOOST PART
The model of the desired waveforms in the hybrid SCVM/boost converter with reduced ripples of the input current is presented in Fig. 5.

The combination of the final waveforms should comply with the following assumptions:
- Both input currents reach the same maximum value $I_m$ – time points $t_2$ and $t_6$.
- The crossing of the waveforms occurs when both currents reach the value $I_m/2$ – the time point $t_4$. This means that the sum of the waveforms ($i_{in}$) reaches the value $I_m$ at the time point $t_4$.
- The input current of the boost converter reaches its maximum value just in the middle of the dead time (time point $t_6 = t_5 + T_{dt}/2$. In the particular case: $T_{dt} = 0$ and then $t_6 = t_5 = t_7$).
The current of the boost converter has an ideal linear waveform and the SCVM current is purely sinusoidal.

Starting from the time point \( t_2 \) (Fig. 5), the SCVM current is described by the function:

\[
i_{\text{inS}} = I_m \cos(\omega_0 t)
\]

where \( \omega_0 \) is the resonant pulsation in the SCVM circuits, \( \omega_0 = 2\pi f_0 = 2\pi/T_0 \), and \( T_0 + 2T_{dt} = T_S \).

Starting from the time point \( t_4 \), the boost current has the following derivative:

\[
\frac{di_{Lb}}{dt} = \frac{I_m}{2} \left( \frac{t_0}{2} - t_4 \right) = \frac{I_m}{2} \left( \frac{t_5}{2} - t_4 \right) + T_{dt} = \frac{U_{in}}{L_b}
\]

At time \( t_4 \), \( i_{\text{inS}} = I_{in}/2 \) and during the time interval \( (t_5 - t_4) \), equal to 1/6 of the half-period \( T_0/2 \), the SCVM current falls to zero. Therefore:

\[
\frac{I_m}{2} \left( \frac{t_5}{2} - t_4 \right) + T_{dt} = \frac{U_{in}}{L_b}
\]

The relationship which connects the inductance of the boost converter and the parameters of the SCVM as well as the input voltage, load, and the used dead time is the following:

\[
L_b = \frac{U_{in}}{I_m} \left( \frac{T_0}{6} + T_{dt} \right)
\]

To achieve the filtering effect, the SCVM and boost converter switching signals should have an adequate phase shift. Assuming that the phase shift of a pulse of the SCVM current is zero, the phase shift of the boost converter is determined by the time point \( t_3 \) (Fig. 5). Using the symmetry of the \( i_{Lb} \) waveform around the time point \( t_4 \), the following relationship is true:

\[
t_4 - t_3 = t_6 - t_4 = \frac{T_0}{12} + \frac{T_{dt}}{2}
\]

The point \( t_4 \) has position \( 5/6T_0/2 \) (5/6\( \pi \)) and the boost converter control time shift is the following:

\[
t_3 = t_4 - \frac{T_0}{12} - \frac{T_{dt}}{2} = \frac{5}{12}T_0 - \frac{1}{12}T_0 - \frac{1}{2}T_{dt}
\]

The average value of the boost converter current is as follows:

\[
D = \frac{t_6 - t_3}{T_0 + 2T_{dt}} = \frac{2T_0 + T_{dt}}{T_0 + 2T_{dt}} = \frac{T_0}{2} + \frac{T_{dt}}{T_0 + 2T_{dt}}
\]

Assuming that the dead time is negligible \( (T_{dt} \approx 0) \), the boost duty cycle approaches the value:

\[
D \approx \frac{1}{3}
\]

Relationship (8) confirms that the boost converter can operate with the proposed SCVM. The boost should charge the internal capacitor \( C_2 \) where the voltage is maintained by the SCVM converter at the level of \( 2U_{in} \). Therefore, the boost converter, as a current-source-type converter, can charge the capacitor \( C_2 \) operated with duty cycle \( D = 0.33 \).

In the next step of the design of the hybrid converter parameters, the maximum current \( I_{in} \) (Fig. 5) should be calculated. In a single SCVM converter, it depends directly on the load (under the fixed parameters of the resonant circuits). In a hybrid converter, the switch-mode boost converter transfers some of the energy, causing the SCVM input current to decrease. In the DCM mode, the average input current of the boost converter can be calculated from a triangle function in the time period \( T_S/2 \):

\[
i_{\text{av}} = \frac{2}{T_S} \left( \frac{1}{2} \frac{T_0}{3} I_m \right) = \frac{I_m T_0}{3 T_S}
\]

The power of the boost part of the converter is then the following:

\[
P_b = U_{in} I_m \frac{1}{3} T_0
\]

Similarly, the power of the SCVM part can be expressed as

\[
P_{SCVM} = \frac{2}{\pi} U_{in} I_m \left( \frac{T_S}{T_S} - \frac{2T_{dt}}{T_S} \right)
\]

Assuming a very short value of the dead time \( T_{dt} \approx 0 \), \( T_S \) tends to \( T_0 \) and the power of the boost converter is expressed by the simplified formula:

\[
P_b = \frac{1}{3} U_{in} I_m
\]

For \( T_{dt} \approx 0 \), the input current of the SCVM converter is composed of the pulses described as:

\[
i_{\text{inS}} = \text{abs}[I_m \sin(\omega_0 t)]
\]

The average value of this current is the following:

\[
i_{\text{inSav}} = \frac{2I_m}{\pi}
\]

The power of the SCVM part of the converter can be expressed by

\[
P_{SCVM} = U_{in} I_{inSav} = \frac{2}{\pi} U_{in} I_m
\]
TABLE 2. Assumed and calculated parameters of the hybrid converter.

| Step | Description and calculated parameter | Equation No. | Example calculation |
|------|--------------------------------------|--------------|---------------------|
| 1    | The oscillation period                | \( \omega_b = \frac{1}{\sqrt{LC}} = 0.71 \times 10^4 \) rad/s; \( f_b = 114 \) kHz; \( T_b = \frac{2 \pi}{f_b} = 8.77 \) \( \mu \)s |
| 2    | Power sharing between the SCVM and the boost part of the converter | (16) \( P_b = 206 \) W; \( P_{SCVM} = 394 \) W |
| 3    | Maximum value of SCVM input current pulses | (15) \( I_{in,SCVM} = I_{in} = \frac{200}{200} = 1 \) A |
| 4    | Inductance of the boost converter \((L_b)\) | (4) \( L_b = \frac{U_{in} (L_b + \Delta L)}{100 (8.77 \times 10^{-4})} = 23.7 \) \( \mu \)H |
| 5    | The delay of the control signal for the boost converter \((t_b)\) | (6) \( t_b = \frac{1}{3} t_{in} - \frac{1}{3} t_{dt} = 2.92 \) \( \mu \)s |

From (16), it is seen that the boost converter transfers approximately 34% of the power of the hybrid system (Fig. 1). Thus, it reduces the power of the SCVM converter and the current stresses of its components.

The power of the SCVM and the switch-mode part of the converter is

\[ P_{SCVM} = \frac{P_{SCVM}}{P_b} = \frac{\frac{2}{3} U_{in} I_{in}}{\frac{1}{3} U_{in} I_{m}} \approx 1.9 \]  

(E. SELECTION OF THE BOOST CONVERTER PARAMETERS FOR A 600 WATT HYBRID SYSTEM)

Table 2 presents the assumed and calculated parameters of the hybrid converter in figures.

From the relationship (4), it is seen that the boost inductance \((L_b)\) is a function of the input voltage, the resonant frequency of the SCVM circuits and the dead-time. The inductance \(L_b\) can be minimized by a decrease in the dead-time and an increase in the resonant frequency \(f_0\). This allows to minimize the \(LC\) parameters in the SCVM part as well. Fig. 6 presents graphs that show in figures the example relationships between the required boost inductance \(L_b\) (4) and the dead time, the resonant inductance of the SCVM converter, power, and the SCVM resonant frequency. From these results, it is seen that both inductances (in the boost and SCVM converter) can be minimized simultaneously. The limit of the minimization of the inductances is determined by the maximum value of the currents and switching losses (as the switching frequency increases when smaller inductances are applied in the converters). Another very important conclusion concerns the relationship between the inductance \(L_b\) and the output power. It is very interesting that for higher power, a lower value of inductance is required in the boost part of the hybrid converter.

III. SIMULATION RESULTS

Some simulations were performed to verify the operation of the converter and the analytical findings, as well as to measure the current and voltage values. The parameters of the
simulation model are presented in Table 3. During the tests, the inductance of the boost converter remained constant.

Figure 7 presents steady-state waveforms of the input currents in the converter. According to the assumed operating model, the total input current \( i_{in} \) is significantly improved by cancelation of its pulses.

In Figure 8, the waveforms of currents in particular branches of the converter are demonstrated. The current load is important for the selection of components and the estimation of conduction losses. The current stress of switches and diodes is limited as they conduct current only in every second pulse of operation.

The voltages across capacitors of the converter can be seen in Fig. 9. The four-fold total voltage gain is confirmed, as well as the voltage levels on the capacitors \( C_2 \) and \( C_3 \), which are twice the input voltage.

In the proposed converter, the voltage stress of the switches (Fig. 10) is limited to the input voltage level \( U_{in} \) (transistors \( S_1 \) and \( S_2 \)) and to the doubled input voltage \( 2U_{in} \) (transistors \( S_3 \) and \( S_4 \)). This is very favourable, as the output voltage is \( 4U_{in} \). The voltage stress of the diodes is limited to \( U_{in} \) and \( 2U_{in} \) as well, as seen in the simulation results presented in Fig. 11.

When the output power varies, the reasonable operation method for the converter is to maintain both maximum currents at the same level:

\[
I_{SCVM_{max}} = I_{b_{max}} \tag{18}
\]

Under condition (18) and fixed \( L_b \), the proportion of powers is a function of the output power: \( \Delta_P = \frac{P_{SCVM}}{P_h} = f (P_{out}) \).
Fig. 12 presents the operation of the converter, designed for $P_{\text{out}} = 600 \text{ W}$, under various output powers and measured input currents and power. Based on the simulation results (Fig. 12), the proportion of power $\Delta P$ can be expressed as the following function of the output power:

$$\Delta P = f(P_{\text{out}}) = 310.18 \left( P_{\text{out}}^{0.805} \right)$$

(19)

For the sake of further analysis, the SCVM part of the hybrid converter has been divided into two parts: SCVM\textsubscript{A} and SCVM\textsubscript{B}. The first part, SCVM\textsubscript{A}, consists of components $S\textsubscript{1}$, $S\textsubscript{2}$, $L\textsubscript{1}$, $C\textsubscript{1}$, $D\textsubscript{1}$, and $D\textsubscript{2}$. The second part, SCVM\textsubscript{B}, contains the following elements of the SCVM ($S\textsubscript{3}$, $S\textsubscript{4}$, $L\textsubscript{3}$, $C\textsubscript{3}$, $D\textsubscript{3}$, and $D_{\text{out}}$).

The output voltage regulation in a conventional way is not applicable when the control duty cycle of the SI boost converter is below 50%. The boost converter operates in parallel with the SCVM\textsubscript{A} that has a constant two-fold voltage gain. Operating with $D < 50\%$, the SI circuit charges the
ever, the boost converter operates under favorable conditions of energy transferred by SC circuits.

Conduction losses decrease in SCVMs due to the decrease in the conduction and switching losses in the SC circuits. The parallel operation of the SC network and the boost converter in the proposed hybrid system allows for a decrease in the power losses of the boost converter. Fig. 13 shows a comparison of the converter operation depending on the duty cycle of the boost converter. Matlab/Simulink simulation results at $P_{out} = 600$ W.

capacitor $C_2$. This decreases the power of the SCVM_A, but does not affect the overall voltage gain.

For $D > 50\%$, the SI boost converter allows controlling the voltage across capacitor $C_2$ in the range $u_{c2} > 2U_{in}$. In such a case, the SCVM_A part of the converter cannot charge the capacitor $C_2$ (SCVM_A has a twofold voltage gain and stops operating when $u_{c2} > 2U_{in}$). Therefore, the boost converter converts 100% of the power and the input current ripple reduction is deteriorated. Such an operation can be useful in some special cases of fault-tolerant operation. However, these are not rated conditions for the proposed converter and can require a different design approach than in the case of interleaved operation of the SC and SI input parts of the converter.

Using this stage of operation, the voltage gain characteristic becomes the following:

$$G = 4$$ for $D \leq 0.5$  
$$G = 2 \left( \frac{U_{in}}{1 + D} \right)$$ for $D > 0.5$ in the CCM mode

IV. MODEL OF EFFICIENCY

The parallel operation of the SC network and the boost converter in the proposed hybrid system allows for a decrease in the conduction and switching losses in the SC circuits. Conduction losses decrease in SCVMs due to the decrease of energy transferred by SC circuits.

Additional power losses arise in the boost converter. However, the boost converter operates under favorable conditions from a switching loss point of view:

- The boost converter charges the internal capacitor $C_2$ whose voltage is two times lower than the output voltage of the proposed hybrid converter. This allows one to decrease the turn-off losses of the transistor $S_b$;

- $Q_{on}$ losses are eliminated as the boost operates in the DCM mode.

The conduction loss can also be limited by selecting transistor $S_b$ with a low $R_{DS(on)}$ value. A decrease in the voltage stress of the switch $S_b$ is a very positive characteristic of the proposed converter for the transistor with a low $R_{DS(on)}$.

For calculating the conduction losses, the average and rms values of currents in the particular branches of the converter can be determined on the basis of the input current. A similar method was proposed in [4]. The maximum value of the input current pulses depends on the input voltage and power and can be easily determined by assuming a sinusoidal shape of the current. 

Fig. 8 presents simulation results of the currents in the converter with estimated values of the average and rms values of the currents in branches.

The proportion of the power of the SCVM_A to that of the boost converter is fixed for an operating point determined by the design of the boost inductance and the phase shift of the converter control given in the analysis above. This proportion varies when the converter operates with a dead time and when the output power is changed (19), (Fig. 12). Therefore, in the efficiency model, the proportion $\Delta P$ of the powers of both parts of the converter will be determined using the function (19) that corresponds to the demonstrated case of the design.

It is assumed that the currents of both the SCVM and the boost parts reach the same maximum value $I_{in}$ (Figs. 5 and 12). This current can be determined as a function of the input voltage, converter power, switching frequency, and dead time. In this section, the current $I_{in}$ is computed for a zero dead time.

The converter power $P_{in}$ is the sum of powers of both converter parts

$$P_{in} = P_b + P_{SCVM}$$

where $P_b$ and $P_{SCVM}$ are given by (10) and (11), respectively.

From the topology of the hybrid converter, it is seen that the first part of the SCVM (SCVM_A) operates in parallel to the boost converter with the power

$$P_{SCVM_A} = P_{in} - P_b = P_{in} - \frac{P_{in}}{1 + \Delta P} = P_{in} \frac{\Delta P}{1 + \Delta P}$$

$$= \frac{2}{\pi} U_{in,SCVM} I_{m}, \quad U_{in,SCVM} = U_{in}$$

From (23), we obtain the following:

$$I_{m} = \frac{\pi P_{in}}{2} \frac{\Delta P}{U_{in} \left( 1 + \Delta P \right)}$$

The currents of the SCVM_A are (Fig. 8)

$$I_{S1} = I_{S2} = I_{m} / \sqrt{2}; \quad I_{D1av} = I_{D2av} = 2 / \pi I_{m}$$

(25)

The second part of the SCVM (SCVM_B) operates with full power, and its input voltage $U_{in,SCVMB}$ is equal to $2U_{in}$:

$$P_{SCVMB} = P_{in} = \frac{2}{\pi} U_{in,SCVMB} I_{m2},$$

$$U_{in,SCVMB} = 2U_{in}$$

(26)
From (23), we obtain the following:

$$I_{m2} = \frac{\pi}{4} \frac{P_{in}}{U_{in}}$$  \hspace{1cm} (27)

The currents of the SCVM\textsubscript{B} are (Fig. 8)

$$I_{S3} = I_{S4} = I_{m2}/\sqrt{2}; \quad I_{D3av} = I_{Doutav} = 2/\pi I_{m2}$$  \hspace{1cm} (28)

Both SCVM\textsubscript{A} and SCVM\textsubscript{B} parts are voltage doublers [2]. The efficiency of the MOSFET-based voltage doubler is determined by the resistances of its components, the voltage drops on the diodes, the input voltage, and the power of the doubler. The conduction losses $\Delta P_{Slk}$ in the circuit of charging of the cell capacitor and the losses $\Delta P_{Slk}$ in the circuit of charging of the output capacitor are the following:

$$\begin{align*}
\Delta P_{Sl1} &= r_{Sl}I_{S1}^2 + \Delta U_{D1}I_{D1av}, \\
\Delta P_{Sl2} &= r_{Sl}I_{S2}^2 + \Delta U_{D2}I_{D2av}
\end{align*}$$  \hspace{1cm} (29)

in the SCVM\textsubscript{A}, and

$$\begin{align*}
\Delta P_{Sl1} &= r_{S1}I_{S1}^2 + \Delta U_{D3}I_{D3av}, \\
\Delta P_{Sl2} &= r_{S4}I_{S4}^2 + \Delta U_{Dout}I_{Dout\_av}
\end{align*}$$  \hspace{1cm} (30)

in the SCVM\textsubscript{B}, where $I_{S1}$-$I_{S4}$ are the rms values of the transistor currents, $r_{S1}$-$r_{S4}$ denote the total resistance, including that of the MOSFET, in the circuit of charging and discharging the switched capacitor, respectively. $I_{D1av}$-$I_{D3av}$ and $I_{Doutav}$ are the average values of the diode currents, $\Delta U_{D1}$-$\Delta U_{D3}$ and $\Delta U_{Dout}$ are the voltage drops across the diodes. It is assumed that the voltage drops across the diodes remain constant in their conducting state.

The conduction losses $\Delta P_{C1}$ in both SCVM\textsubscript{A} and SCVM\textsubscript{B} converters are the sum of the aforementioned losses

$$\Delta P_{C1} = \sum_{k=1}^{4} r_{Sl}I_{Sl}^2 + \sum_{k=1}^{3} \Delta U_{Dk}I_{Dk} + \Delta U_{Dout}I_{Dout}$$  \hspace{1cm} (31)

There are also conduction losses $\Delta P_{C2}$ in inductance $L_2$, which is not included in any of the aforementioned doublers. The current $I_{L2}$, shown in Fig. 8, is equal to $-I_{S3}$ in stage I and to $I_{S2}$-$I_{S4}$ in stage II. Therefore, its minimum in stage I is $-I_{m2}$ (27), its maximum in stage II is $I_{m} - I_{m2}$ (24), (27), and its rms value is equal to

$$I_{L2} = \sqrt{\frac{I_{m2}^2 + (I_{m} - I_{m2})^2}{2}}$$  \hspace{1cm} (32)

The conduction losses $\Delta P_{C2}$ are

$$\Delta P_{C2} = r_{L2}I_{L2}^2$$  \hspace{1cm} (33)

where $r_{L2}$ is the resistance of the circuit with $L_2$.

There are also conduction losses $\Delta P_{C3}$ in the boost part of the converter

$$\Delta P_{C3} = r_{Sb}I_{Sb}^2 + \Delta U_{Db}I_{Dbav}$$  \hspace{1cm} (34)

where $I_{Sb}$ is the rms value of the transistor $S_b$ current, and $r_{Sb}$ denotes the total resistance, including that of transistor $S_b$, in the circuit with inductance $L_b$. $I_{Dbav}$ is the average value of the diode $D_b$ current and $\Delta U_{Db}$ is the voltage drop across this diode. Both $I_{Sb}$ and $I_{Db}$ currents are linear (Fig. 5); thus,

$$I_{Sb} = I_{m}\sqrt{\frac{2I_{m}L_b}{3U_{in}f_S}}, \quad I_{Dbav} = \frac{I_{m}^2 L_b}{U_{in}f_S}$$  \hspace{1cm} (35)

The turn-off switching loss of transistors $S_1$-$S_4$ is zero, due to the ZCS switching. However, there is a turn-on switching loss, associated with charging and discharging the output capacitances of the MOSFETs. The latter also refers to the transistor $S_b$. The total turn-on switching power loss $\Delta P_{sw\_on}$ is

$$\Delta P_{sw\_on} = \Delta W_{sw\_on\_av}$$  \hspace{1cm} (36)

where $\Delta W_{sw\_on\_av}$ is the energy lost at turn-ons in all MOSFETs’ resistances in a single switching cycle. A way to calculate these losses is presented in [36].

The transistor $S_b$ is turned off at maximum current $I_m$, which involves a turn-off switching loss $\Delta P_{sw\_off}$

$$\Delta P_{sw\_off} = \Delta W_{sw\_off\_av}$$  \hspace{1cm} (37)

where $\Delta W_{sw\_off\_av}$ is the energy lost at the turn-off of transistor $S_b$ in a single switching cycle. This loss can be calculated based on [36] and the results of the measurements.

The overall loss is the sum of all the aforementioned losses

$$\Delta P = \Delta P_{C1} + \Delta P_{C2} + \Delta P_{C3} + \Delta P_{sw\_on} + \Delta P_{sw\_off}$$  \hspace{1cm} (38)

and the efficiency of the converter is given by

$$\eta = 1 - \frac{\Delta P}{P_{in}}.$$  \hspace{1cm} (39)

The results of this analysis are used in Fig. 21 to compare the measured efficiency of the converter with the theoretical one.

The tolerance of passive components or their parameter variation may lead to an operation with unequal time durations of current pulses. To maintain the ZCS conditions, the time between pulses (the dead-time determined by the time interval $T_3$-$T_7$ in Fig. 5) should be designed to be long enough. However, a dead time that is too long is not favorable due to the deterioration of efficiency in the SCVM converter that was proven in [33]. On the other hand, the SC converter operation above the resonant frequency is not dangerous, but may lead to a decrease in the output voltage. Such cases of operation were analyzed in [2] for a voltage doubler. In the converter presented in this paper, the operation above the resonant frequency is also allowed because the current of any inductor can flow through the diodes when the transistors are turned off.

V. EXPERIMENTAL VERIFICATION

This chapter presents the results of the hybrid converter measurements performed on the experimental setup. During the experiment, the operation of the converter and the higher harmonic content in its input current were verified. Moreover, the efficiency characteristic of the proposed converter was compared with that of the pure SCVM converter and with a theoretical one.

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\textit{R. Stala et al.: Input Current Ripple Reduction in Step-Up DC–DC Switched-Capacitor Switched-Inductor Converter}
FIGURE 14. Experimental setup of the proposed converter.

TABLE 4. Parameters of the experimental setup.

| Parameter            | Value                                |
|----------------------|--------------------------------------|
| Input voltage        | 100 V                                |
| Output Power         | 585 W (resistive load)               |
| Switching frequency  | 95 kHz                               |
| Input capacitor      | 4.7 μF (KEMET R76 series) + 100 μF electrolytic capacitor |
| Output capacitor     | 4.7 μF (KEMET R76 series) + 100 μF electrolytic capacitor |
| Resonant capacitors  | 1.5 μF (KEMET R76 series)            |
| Resonant inductors   | 1.3 mH (Wurth Elektronik 7443556130) |
| Transistors          | SCVM circuit part: IPB50R140CP (V_{ds} = 550 V, R_{on} = 140 mΩ) 
                      | BOOST circuit part: IPW60R070C777 (V_{ds} = 650 V, R_{on} = 70 mΩ) |
| Diodes               | SCVM circuit part: STTH30L06G (I_{f} = 30 A, V_{f} = 1.0 V, V_{rem} = 600 V) 
                      | BOOST circuit part: IDW2G65C5B (I_{f} = 20 A, V_{f} = 1.5 V, V_{rem} = 600 V) |
| PCB                  | FR4, 2 layers, 35 μm                  |

A. EXPERIMENTAL SETUP

All the parameters of the components used in the experimental setup, as well as other relevant experimental conditions, are collected in Table 4. The laboratory setup is presented in Fig. 14 where the SCVM part is visible on the top of the stack and the switch-mode section is placed on the bottom. The test results were obtained with the use of discrete chokes in the SCVM, but the setup allows for an operation at higher frequencies with air-based resonant chokes.

B. EXPERIMENTAL RESULTS

Figure 14 presents the oscillogram of the input currents and the output voltage in the proposed converter. These are the essential results that confirm the operation of the proposed concept and the cancelation of the input current ripple. In the waveforms presented, the pulsating SCVM input current (i_{inS}) and the phase-shifted input current of the boost converter (i_{inB}) are seen. The combination of these two DC-DC converters, as shown in Fig. 1, allows reducing the overall pulsation of the input current (i_{in}) of the SCVM converter.

The proposed modification does not have any negative impact on the voltage gain of the converter, which is proven by the converter output voltage recording (u_{out}). During the experiment, the proposed converter was operating at the output power of 585 W while powered up from a 100 V DC source. Under such conditions, the converter achieves a four-fold voltage gain, which is in line with the theoretical considerations and the results of the simulation research.

The waveforms visible in Fig. 15 were also recorded as a text file. This was done in order to perform the fast Fourier transform (FFT) analysis on it and investigate the exact
FIGURE 17. Waveforms of AC components of currents and voltages in the proposed hybrid converter in steady state: 1) input current of the SCVM converter, 2) input current of the switch-mode boost converter, 3) voltage across resonant capacitor \( C_1 \), 4) voltage across resonant capacitor \( C_2 \). Test conditions: \( U_{in} = 100 \text{ V} \), \( P_{out} = 585 \text{ W} \).

The amount of higher harmonic content in the currents \( i_{inS} \) and \( i_{inb} \). The spectral analysis calculations have been carried out with the usage of MATLAB software and the results are shown in Fig. 16. From the obtained graphs, it follows that the input current of the hybrid converter contains much fewer higher harmonics than the input current of the pure SCVM converter.

Figure 17 presents the waveforms of the basic converter currents and voltages across the resonant capacitors \( C_1 \) and \( C_2 \). To obtain a full view of the recharging processes that take place in the proposed converter, an analysis of the voltage across capacitor \( C_3 \) (Fig. 18) is needed. All voltage waveforms shown in Figs. 17 and 18 present voltages recorded in the AC mode to expose the charging and discharging processes that take place in resonant capacitors and are crucial for the analysis of the operating principle.

The waveforms presented in Figs. 17 and 18 show that the resonant capacitors \( C_1 \) and \( C_3 \) are being charged and discharged at the same time. Furthermore, the charging of capacitor \( C_2 \) starts when capacitors \( C_1 \) and \( C_3 \) start to discharge, which is exactly in line with the previously assumed operating principle of the converter.

The proposed converter allows for reducing the drawbacks of the classic SCVM converter and maintaining all its positive characteristics. This is visible in Fig. 19, where the voltage stresses of the transistors operating in the converter output stage are shown. In this part of the proposed circuit, the expected voltage stresses are the highest, like in a classic SCVM converter. From the properties of the SCVM topology, it follows that the voltage stresses across the switches in this part of the converter are equal to only half of the classic SCVM converter output voltage. This benefit is very valuable from the perspective of the selection of semiconductor elements and is also present in the proposed hybrid converter.

Other experimental tests were associated with the efficiency of the hybrid and pure SC converters. The results presented in Fig. 20 show that the peak efficiency of the hybrid converter is about one percentage point above that of the pure SCVM. Additionally, the efficiency characteristic of the hybrid converter seems to be stable, while that of the classic SCVM starts to decrease for higher loads. This proves that the proposed converter might be a better solution for use in higher power applications.

FIGURE 18. Waveforms of AC components of currents and voltages in the proposed hybrid converter in steady state: 1) input current of the SCVM converter, 2) input current of the switch-mode boost converter, 3) voltage across resonant capacitor \( C_2 \), 4) voltage across resonant capacitor \( C_3 \). Test conditions: \( U_{in} = 100 \text{ V} \), \( P_{out} = 585 \text{ W} \).

FIGURE 19. Relevant currents and voltages across transistors \( S_3 \) and \( S_4 \). 1) AC components of current of SCVM converter part; 2) AC components of current of BOOST converter part; 3) voltage across transistor \( S_3 \); 4) voltage across transistor \( S_4 \).

FIGURE 20. Comparison between the efficiencies achieved by the pure SCVM converter and the hybrid converter. At each measured point, the equality of maximum currents is maintained \( I_{inb\text{max}} = I_{inS\text{max}} \), as in Fig. 12.
VI. CONCLUSION

In this paper, a novel concept and results of investigations of a parallel converter composed of switched-capacitor (SC) circuits and a switch-mode converter are presented. The proposed hybrid converter demonstrates the following several advantages compared to a pure SC converter:

- The input current ripple is reduced significantly;
- The application of the switch-mode part connected in parallel to the SC converter reduces the current burden of the SC converter, and the total cost of the converter may not rise when the hybrid concept is introduced;
- The efficiency of the hybrid converter is higher than that of the classical SCVM for higher values of power; thus, the proposed converter might be a better solution for use in higher power applications;
- The switch-mode converter, built in the boost topology, operates in the deep DCM mode with a low duty cycle. Therefore, its choke has a small inductance and volume;
- The boost converter operates with a low output voltage (two times lower than the output voltage), which allows the use of high-quality semiconductor switches of low cost;
- Very favorable design relationships show that the inductance of the boost converter should be decreased as the power of the converter increases. Similarly, when the resonant inductance of the SCVM part is designed smaller, the boost inductance is also decreased. This makes it possible to minimize the volume of the entire hybrid converter;
- As the input current ripple is significantly reduced, the proposed converter could be attractive for application in photovoltaic systems. In a DC-AC PV system, the proposed DC-DC converter allows to increase the voltage of the PV arrays to a range of the rated DC-link voltage of the inverter. Since the DC-DC multiplier does not regulate power, the MPPT algorithm should be implemented for inverter control. A similar approach is used in PV systems that operate without DC-DC converters. Reference [35] shows a concept of the MPPT method for a single-stage grid-connected PV system with a single-phase inverter. The presence of a multiplier in the conversion system may, of course, affect its dynamic behavior;
- The major qualities of the proposed converter are compared with the state-of-the-art and are demonstrated in Table 5. The selected cases for comparison contain SC converters operating in the interleaved configuration [18]–[24]. As the proposed converter uses low-volume chokes in both SC and switch-mode parts, a detailed comparison with interleaved SC converters is valuable;
- When optimization towards the number of components utilization is critical, the proposed converter can be selected among the concepts compared in Table 5. Pure SC converters, such as the solution presented in [20], use a large number of switches, but allow the ripple of the input current to be reduced without the use of discrete

### Table 5. Comparison of parameters among the proposed converter and switch-capacitor converters with decreased current ripples.

| Parameters                  | Proposed converter | Ref. [18]–[19] | Ref. [20] | Ref. [21] | Ref. [22] | Ref. [23] | Ref. [24] case G=4 |
|-----------------------------|--------------------|----------------|-----------|-----------|-----------|-----------|-------------------|
| Structure                   | Parallel: SC and boost | Interleaved: SC parts | Interleaved: SC parts | Parallel: Interleaved SC and boost | Series output capacitors | Interleaved: SC multiplier | Interleaved: SC parts | Interleaved: Dickson |
| Input current ripple decrease | yes               | yes            | yes       | yes       | yes       | yes       | yes               |
| Voltage gain                | G = 4             | G = 0.75       | G = 6 (Extension possible) | Regulated: \(U_{in}=100\, V\) | \(U_{out}=1.0\, V\) | \(U_{sb}=1.5\, V\) | \(U_{sw\_on}=20\, \mu A\) |
| Voltage stress of transistors | In SC part: min: \(U_{sw\_4}\) max: \(U_{sw\_2}\) in boost part: \(U_{sw\_3}\) | - | - | min: \(U_{sw\_6}\) max: \(U_{sw\_5}\) | min: \(U_{sb}\) (boost part output < \(U_{in}\) max: \(U_{sw\_out}\) | \(U_{in}\) | \(U_{sb}\) | \(U_{sw\_off}\) (G = 5.6, G = 7.5) | G = 2, G = 3 | G = 3 (G = 3 and extension possible) |
| Transistor count            | 5 k | 12k | 21 | 8 (G = 3) | 4 (G = 2) | 12 | 2 |
| Diode count                 | 5 0 0 13 | 8 (G = 3) | 4 (G = 2) | 0 | 6 |
| Switched-capacitor count    | 3 \(\mu\) F | 2k | 10 | 4 | 3 | 6 |
| Inductor count and inductance | 1.9 \(\mu\) H | 1 | 80 | 2x | 500mH | 1x | 20 \(\mu\) H |
| Peak efficiency             | >95 [\%] | - | >94 [\%] | >94 [\%] | >95.5 [\%] | Appro x. 96.9 [\%] | 98% |

*\(k\) - number of interleaved units in the concept of a converter

- the data are not presented exactly in the reference publication

Figure 21 shows a comparison between the measured efficiency of the hybrid converter (Fig. 20) and the theoretical efficiency given by (39). There is a good convergence between both characteristics.
inductors and with lower voltage stress of the switches. The converter presented in [24] uses a very low number of transistors, but the converter proposed in this paper exhibits a favorable low number of diodes and capacitors; the other class of hybrid converters utilizes switch-mode converters with larger inductors, which allows for low-ripple input current and regulation capability. Reference converters from that area of concepts are described in Introduction with example values of the used inductances.

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