Variability Aware Read and Write Channel Models for 1S1R Crossbar Resistive Memory with High Wordline/Bitline Resistance

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Abstract—Crossbar resistive memory with 1S1R structure is attractive for low-cost and high-density nonvolatile memory application. As technology scales down to single-nm regime, the increasing resistivity of wordline/bitline becomes a limiting factor to device reliability. This paper presents write/read communication channels while considering the line resistance and device variabilities by statistically relating the degraded write/read margins and the channel parameters. Binary asymmetric channel (BAC) models are proposed for the write/read operations and array capacity results are presented. Simulations based on these models suggest bit-error rate of devices are highly non-uniform across the array. These models provide quantitative tools for evaluating the trade-offs between memory reliability and device parameters, such as array size, technology nodes, and aspect ratio, and also for designing coding theoretical solutions for crossbar memory.

I. INTRODUCTION

The crossbar resistive memory, whereby bistable memristors are placed at the crosspoint of wordlines and bitlines, is one promising candidate for the next generation nonvolatile memory due to its inherent 4F² device density and its simple crossbar structure [1]. Meanwhile, as technology scales down to single-digit-nm, the simultaneously scaled wordline/bitline resistance becomes more a limiting factor to device reliability and hence memory scalability [2].

Many literatures have shown that even moderate line resistance significantly degrades the reliability of the write and read operation. The degradation of the read and write margins due to high line resistance for the worst-case memory cell, i.e., the cell that is furthest from the source and ground, are studied in [2], [3], [4]. The adverse effect of the line resistance on the read and write margins for cells across the memory array are studied in [5], [6] by solving system of Kirchhoff’s current law (KCL) equations. While most of the studies focused on the degradation of the write/read margin, it remains unclear how the degraded write/read margin affects the system level reliability metric, e.g., the bit-error rate (BER). Therefore, a study on the write and read channel models while considering the high line resistance could be beneficial for system engineers and ECC designers when designing next generation storage systems.

Moreover, all the aforementioned studies on the write/read margin assumes deterministic High Resistance State (HRS) and Low Resistance State (LRS) for the memory device whereas the HRS and LRS are nondeterministic in nature [7], [8]. A study on the write/read channel models, which is done probabilistically, allows us to take the resistance variability of LRS and HRS into consideration.

It is demonstrated in [5] that, when considering the line resistance, the write margins are nonuniform across the array. This memory specific non-uniformity can be leveraged to design better ECC for memory. In [9], the authors designed a non-stationary polar code targeting non-uniform BER by characterizing this non-uniformity empirically. In [10], the authors propose to use ECC targeting the typical BER instead of the worst-case BER to improve system performance. A theoretical characterization of the non-uniform channel properties also provide quantitative tools for more ECC works in a similar direction.

We enlist our main contributions of this work:

• Binary Asymmetric Channel models for writing to and reading from memory devices in crossbar memory, parameterized by device parameters, array size, wordline/bitline resistance and device location.
• The incorporation of non-deterministic HRS and LRS in the reliability analysis.
• Capacity results for crossbar resistive memory while considering the high line resistance.

The content of this paper is organized as follows. Section II provides background on crossbar resistive memory and the read/write operation. The circuit models and the variabilities we studied are also discussed in Section II. Section III presents the channel characterization for the write operation. Section IV presents the channel characterization for the read operation. The write and read channels are combined in Section V. Capacity results for both a single cell and the entire array based on the concatenated channel are also presented in Section V. We simulate arrays with various parameters and present the results in Section VI. We conclude and discuss future research in Section VII.

II. PRELIMINARY

A. 1S1R Crossbar Memory Background and Model

In crossbar resistive memory array, the logical state 0 or 1 is represented by the HRS or LRS of a memory cell, respectively. For bipolar memristor, the state of a cell is switched from LRS to HRS (Reset Operation) or from HRS to LRS (Set Operation) by applying a positive or negative voltage across the memory cell, receptively. For the write operation, we consider the V/2 write scheme as it is usually more energy-efficient than the V/3 write scheme [3]. In particular, when writing to a selected cell, the wordline and bitline of the selected cell are biased at the write voltage (Vw_set or Vw_reset) and 0, respectively, while...
other wordlines and bitlines are biased at \( V_w/2 \) to prevent unintentional write, as shown in Fig. 1.

![Fig. 1: Circuit model for writing to a 8 \times 8 array](image1)

For the read operation, we consider the current-mode sensing scheme as it is reported to have a smaller latency compared with the voltage-mode sensing scheme [3]. When reading a selected cell, a read voltage \( V_r \) is applied on its wordline and all other wordlines and bitlines are grounded. The current through this cell is sensed by the sensing amplifier located at the end of its bit line and is then used to determine the state of the selected cell, as shown in Fig. 2.

![Fig. 2: Circuit model for reading from a 8 \times 8 array](image2)

In this paper, we focused on crossbar resistive memory with the widely used 1 selector 1 resistor (1S1R) structure, where highly nonlinear selectors are connected in series with the memristors to prevent write and read disturbs. For both write and read operations, when the voltage across a selector is close to the applied voltage \( V_w \) or \( V_r \), we say this selector is fully selected and we assume it has resistance \( r_{sf} \); when the voltage across a selector is close to 0, we say this selector is un-selected and we assume it has resistance \( r_{su} \). For the write operation, since other cells on the wordline and bitline of the selected cell have voltage close to \( V_w/2 \) across them, we say the selectors for those cells are half-selected and we assume they have resistance \( r_{sh} \).

**B. Memristor Variability and Model**

In this paper, we consider two variabilities of memristor, the non-deterministic write operation and the non-deterministic resistance value for each resistance state. It is widely observed that the switching operations of memristor are stochastic and follow log-normal switching time distributions, where their parameters depend on the applied voltages [11], [12]. Our models for the switching time distributions are adopted from [11] and more details are provided when we talk about write channel in Section III.

Previous works on the degradation of read and write margins due to high line resistance assume deterministic resistance states, e.g., HRS resistance is 10000\( \Omega \) and LRS resistance is 100\( \Omega \). Meanwhile, due to both device to device variation and cycle to cycle variation, the resistance of each states are highly non-deterministic [7], [8]. To incorporate this variability into our reliability analysis, we use random variables to represent the resistance of the memory cells. We assume they are i.i.d. and their conditional distributions, conditioned on the their states, follow log-normal distributions. For example, let i.i.d. Bernoulli\( (\theta) \) random variable \( S_{ij} \) denote the state of cell \((i,j)\), \( S_{ij} = 1 \) for LRS and \( S_{ij} = 0 \) for HRS. Let \( R_{ij} \) be the associated random variable denoting the resistance of cell \((i,j)\). Then our models assume:

\[
\ln(R_{ij}|S_{ij} = 1) \sim N(\mu_L, \sigma_L^2),
\]

and

\[
\ln(R_{ij}|S_{ij} = 0) \sim N(\mu_H, \sigma_H^2).
\]

**III. WRITE CHANNEL**

We denote the state we want to write to cell \((i,j)\) by \( X_{ij} \) and the state actually written by \( Y_{ij} \). The writing operation is also affected by the previous state of cell \((i,j)\). Let \( S_{ij} \) and the associated resistance value to be \( R_{ij} \). We assume that when the previous state is the same as state we want to write, the write operation is always successful, i.e.,

\[
P(Y_{ij} = 1|X_{ij} = 1, S_{ij} = 1) = 1,
\]

and

\[
P(Y_{ij} = 0|X_{ij} = 0, S_{ij} = 0) = 1.
\]

When the previous state is not the same as state we want to write, a sufficient write voltage and a sufficient write time is required to change the state of the cell. Due to high line resistances, the effective write voltage on a cell could be much smaller than the desired write voltage, i.e., the write margin is decreased. We denote the effective write voltage on a cell \((i,j)\) to be \( \hat{V}_w(r^*_{ij}, i,j) \) where \( r^*_{ij} \) is a realization of \( R_{ij}^* \). With similar method described in [5], \( \hat{V}_w(r^*_{ij}, i,j) \) can be obtained by solving system of KCL equations using the circuit model described in II.A. We map the degraded write margin to the decreased write reliability by considering the log-normal switching time distribution. With fixed switching time \( t_{set} \) and \( t_{reset} \), the log-normal switching time distribution leads to the following:

\[
P(Y_{ij} = 1|X_{ij} = 1, S_{ij} = 0, R^*_{ij} = r^*_{ij})
\]=
\[
\int_{-\infty}^{t_{set}} \frac{1}{\sqrt{2\pi\sigma_{set}}} \exp \left[ -\frac{\ln(\frac{\ln t_{set}}{2\sigma_{set}^2})}{2\sigma_{set}^2} \right] dt
\]

\[
=1 - Q \left( \frac{\ln t_{set} - \ln(r^*_{ij})}{\sigma_{set}} \right),
\]
When reading from the cell \((i,j)\), we consider the current-mode sensing scheme and a fixed threshold detector. Let \(I_r^{(ij)}\) be the current sensed by the sensing amplifier, which can be calculated by solving system of KCL equations. \(I_r^{(ij)}\) is hence dependent on the cell location, the resistance of the selected cell, and the resistances of unselected cells. Let \(Z_{ij}\) be the detected state of the selected cell and \(I_{th}\) be the threshold current, the threshold detector is as follows:

\[
Z_{ij} = \begin{cases} 
0, & I_r^{(ij)} \leq I_{th} \\
1, & I_r^{(ij)} > I_{th}
\end{cases}
\]  (7)

With the threshold detector above, the decision error probabilities are:

\[
P(Z_{ij} = 1|Y_{ij} = 0) = P(I_r^{(ij)} > I_{th}|Y_{ij} = 0),
\]  (8)

and

\[
P(Z_{ij} = 0|Y_{ij} = 1) = P(I_r^{(ij)} \leq I_{th}|Y_{ij} = 1).\]  (9)

This leads to the binary asymmetric channel, depicted in Fig. 4, for the read operation with

\[
p_3^{(ij)} = P(Z_{ij} = 1|Y_{ij} = 0) \quad \text{and} \quad p_4^{(ij)} = P(Z_{ij} = 0|Y_{ij} = 1).\]

### IV. Read Channel

A. Closed form Expression with Ideal Selectors

Since the sensed current need to be obtained by solving system of equations, equation (8) and (9) do not give a closed form expression for the channel parameters. Meanwhile, if we consider ideal selectors, i.e., selectors with \(r_{sf} = 0\) and \(r_{sh} = \infty\), closed form expression can be derived.

With ideal selectors, the part of the circuit connected to half-selected and un-selected selectors can be neglected, resulting in a simplified circuit with just the selected cell and its wordline/bitline. With this simplified circuit, \(I_r^{(ij)}\) is a function of the random variable \(R_{ij}\), which represents the resistance of the selected cell. We have:

\[
I_r^{(ij)} = \frac{V_r}{ir_w + jr_b + R_{ij}}.
\]  (10)

Plugging (10) into (8) and (9), and using the assumption that \(R_{ij}\) is conditionally (on \(Y_{ij}\)) log-normally distributed, we obtained the following closed form expression for \(p_3\) and \(p_4\):

\[
p_3^{(ij)} = P\left(\frac{V_r}{ir_w + jr_b + R_{ij}} > I_{th}|Y_{ij} = 0\right)
\]

\[
= P\left(R_{ij} < \frac{V_r}{I_{th} - ir_w - jr_b}|Y_{ij} = 0\right)
\]

\[
= Q\left(\frac{\mu_H - \ln\left(\frac{V_r}{I_{th} - ir_w - jr_b}\right)}{\sigma_H}\right),
\]  (11)

\[
p_4^{(ij)} = 1 - p_3^{(ij)}.
\]
are independent. The capacity of the memory array readily follows:

\[ C_{\text{array}} = \max_{q_{ij}} I(X_m^n; Z_m^n) \]

\[ = \max_{q_{ij}} H(Z_m^n) - H(Z_m^n|X_m^n) \]

\[ = \sum_{i=1}^{m} \sum_{j=1}^{n} \max_{q_{ij}} H(Z_{ij}) - H(Z_{ij}|X_{ij}) \]

(14)

where \( X_m^n = X_{11}, \ldots, X_{mn} \) and \( Z_m^n = Z_{11}, \ldots, Z_{mn} \). The third equality follows directly from the independence between \( Z_{ij}(s) \) and the independence between \( X_{ij}(s) \).

VI. SIMULATIONS RESULTS

Based on our models presented in the previous sections, we simulate multiple arrays to explore how memory parameters affects the memory reliability metrics, such as the bit-error rate (BER) and the averaged capacity. Since this work is mainly focused on the adverse effect of line resistance, we only vary the array size, aspect ratio and line resistance in our simulations. Other memory parameters are kept the same and summarized in Table 1. The parameters chosen in this table by no means represent any real memory device. Instead, the parameters are chosen to represent a moderate reliability level, with a BER on the level of \( 10^{-3} \) in the best case scenario.

TABLE I: Summary of Parameters

| Symbol | Parameters | Simulation Values |
|--------|------------|-------------------|
| \( m, n \) | Array Size \((m \times n)\) | varies |
| \( V_{w, \text{set}} \) | Set voltage | -5V |
| \( V_{w, \text{reset}} \) | Reset voltage | 5V |
| \( V_r \) | Read voltage | 3V |
| \( q \) | Prior symbol probability of 0 | 0.5 |
| \( r_w \) | Wordline interconnect resistance | \(10\Omega - 100\Omega\) |
| \( r_b \) | Bitline interconnect resistance | \(10\Omega - 100\Omega\) |
| \( r_{sh} \) | Fully selected selector resistance | 0 |
| \( r_{su} \) | Half selected selector resistance | \(\infty\) |
| \( r_{su} \) | Unselected selector resistance | \(\infty\) |
| \( \mu_L \) | Associated mean of LRS distribution | \(4 \ln(10)\) |
| \( \mu_H \) | Associated mean of HRS distribution | \(6 \ln(10)\) |
| \( \sigma_L \) | Associated std of LRS distribution | \(0.3 \ln(10)\) |
| \( \sigma_H \) | Associated std of HRS distribution | \(0.3 \ln(10)\) |
| \( \alpha_{\text{set}} \) | Parameter for the median set time | 0.25 |
| \( \beta_{\text{set}} \) | Parameter for the median reset time | 4.25 |
| \( \alpha_{\text{reset}} \) | Parameter for the median set time | -0.25 |
| \( \beta_{\text{reset}} \) | Parameter for the median reset time | 4.25 |
| \( \sigma_{\text{set}} \) | Associated std of set distribution | 0.5 |
| \( \sigma_{\text{reset}} \) | Associated std of reset distribution | 0.5 |
| \( t_{\text{set}} \) | Switching time for set operation | 100\(\mu s\) |
| \( t_{\text{reset}} \) | Switching time for reset operation | 100\(\mu s\) |
| \( I_{th} \) | Read decision threshold | 30\(\mu A\) |

In Fig. 6 we first present the BER of each cell in a \(1024 \times 1024\) array to illustrate the spacial variation of reliability due to the line resistance. According to [2], the chosen \(10\Omega\) line resistance corresponds to the resistance per junction of Cu wire with 20nm technology nodes. With this moderate line resistance, we observe an order of magnitude BER difference between the best-case cell, located closest to
the voltage source, and the worst-case cell, located furthest from the voltage source. Due to line resistance, the cell which is further from the source and sensing amplifier, suffers from a lower voltage delivery during the write operation and a higher resistance interference during the read operation.

Next, in Fig. 7 we present the averaged capacity per cell for arrays with various size and line resistances, with aspect ratio fixed to be 1. We observe that a larger line resistance, which corresponds to a smaller technology node, deteriorates the averaged capacity almost linearly. This trade-off thus must be taken into consideration when scaling the memory, as it presents a trade-off between the sometimes desired high aspect ratio and a high averaged capacity for memory designers.

VII. CONCLUSION AND FUTURE WORKS

In this paper, we proposed the read and write channel model for the 1S1R crossbar resistive memory while considering the nondeterministic nature of the memory device. Future researches are in the direction of leveraging the channel information to improve memory reliability. These researches include system level approaches such as finding the optimal read threshold and coding theoretic approaches such as designing LDPC codes with unequal error correction capability.

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| Array Size     | 128 × 128 | 64 × 512 | 32 × 512 |
|---------------|-----------|----------|----------|
| Averaged Capacity | 0.9924 | 0.9918 | 0.9897 |
| Array Size     | 16 × 1024 | 8 × 2048 | 4 × 4096 |
| Averaged Capacity | 0.9845 | 0.9745 | 0.9573 |