Top-Down Fabricated Reconfigurable FET With Two Symmetric and High-Current On-States

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Abstract—We demonstrate a top-down fabricated reconfigurable field effect transistor (RFET) based on a silicon nanowire that can be electrostatically programmed to p- and n-configuration. The device unites a high symmetry of transfer characteristics, high \( \text{ON/OFF} \) current ratios in both configurations and superior current densities in comparison to other top-down fabricated RFETs. Two NiSi₂/Si Schottky junctions are formed inside the wire and gated individually. The narrow omega-gated channel is fabricated by a repeated SiO₂ etch and growth sequence and also with the Center for Advancing Electronics Dresden (CfAED), TU Dresden, 01062 Dresden, Germany, and also with the Center for Advancing Electronics Dresden (CfAED), TU Dresden, 01062 Dresden, Germany, also with the Center for Advancing Electronics Dresden (CfAED) under Grant EXC 1056. The review of this letter was arranged by Editor K. J. Kuhn. (Corresponding author: Maik Simon.)

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Several RFETs have been experimentally demonstrated based on bottom-up grown Si or Ge nanowires [7]–[11], carbon nanotubes [12] or two-dimensional materials [13]–[16]. Low band-gap channel materials like Ge are beneficial to increase the current close to CMOS levels [17]. However, a geometrically well-controlled and CMOS-compatible fabrication has so far only been achieved by a top-down fabrication on base of silicon-on-insulator (SOI) wafers or poly-Si films [18]–[30]. Yet, the comparably high band gap of Si demands for high electric fields to induce strong tunneling currents which can be best achieved in narrow channels with a multigate architecture. Note that in contrast to Schottky barrier (SB) MOSFETs, the SBs in RFETs cannot be reduced for just one carrier type. Instead, a high symmetry of the IV-characteristics in p- and n-configuration is desired to ensure switching delay indifference. This can be enabled by a precise alignment of gate and Schottky contact metal work functions and stress in the wire. Additionally, RFETs need to be optimized towards high ON-currents for fast calculations and low OFF-currents for a low standby-power consumption.

The current densities of the device in this work are the highest reported so far for top-down fabricated RFETs. Furthermore, the \( \text{ON/OFF} \) ratios are very high and the transfer characteristics are almost symmetric for both configurations.

II. DEVICE FABRICATION

The RFET in this work is fabricated from a commercial SOI wafer with a 20 nm thick, (001) oriented and lightly p-doped (10\(^{15}\) \( \text{cm}^{-2} \)) device layer on top of a 100 nm thick buried SiO₂ layer. Fig. 3 gives an overview of the process flow. A 3.98 \( \mu \)m long nanowire channel is created in \( <110> \) direction by using an electron beam lithography (EBL) defined hydrogen silsesquioxane (HSQ) pattern as hard mask for a reactive ion etching process [31]. The etching employs SF₆, CHF₃ and O₂ at a ratio of 15:6:5 and a pressure of 0.1 Torr.

After removing the residual HSQ and native oxide by a dip in HF, the SiO₂ gate dielectric is formed by rapid thermal
Fig. 1. (a) Colored SEM top-view image of the RFET featuring a control gate (CG) and a program gate (PG). (b) Transmission electron microscopy image of a cut through the PG in Fig. 1a showing a nanowire channel with omega-shaped gate stack. Carbon coating originates from creation to source/drain (S/D) contact formation.

Fig. 2. Schematic of the RFET band structure for different voltage settings. The polarity of the voltages at drain and program gate (PG) determines the p- or n-configuration. By tuning the control gate (CG) voltage to the same polarity, carriers are injected at the source by tunneling through the Schottky junction. The NiSi2/Si Schottky junctions are covered by the gates. (d) Electronic symbol of the RFET.

Fig. 3. Process flow for transistor fabrication from nanowire (NW) creation to source/drain (S/D) contact formation.

Fig. 4. Highly symmetric transfer characteristics of the RFET for a drain voltage of 1 V (n-configuration) and −1 V (p-configuration), both in a double sweep. Equal ON- and OFF-currents as well as a high ON/OFF ratio in both configurations are achieved. Gate charging and leakage currents (grey) remain low even for high reverse VCG.

III. DEVICE CHARACTERISTICS

Both Schottky junctions of the RFET are gated individually by a so-called program gate (PG) at the drain and a control gate (CG) at the source side (see Fig. 2). NiSi2 has a work function close to middle of the band gap of Si, with a slightly larger SB for electrons than for holes. For electrical characterization, the substrate and the source terminal are grounded. By changing the polarity of the drain voltage \( V_D \) and program gate voltage \( V_{PG} \), the RFET can be toggled between p- and n-configuration by blocking undesired carrier injection from the drain. For \( V_{PG} \geq V_D > 0 \) V, hole injection from the drain is blocked by the large energy barrier, so the RFET is in n-configuration. To turn the transistor ON, a sufficiently high voltage is applied at the CG. This induces Fowler-Nordheim tunneling of electrons through the source-sided Schottky junction. For p-configuration the polarities of all voltages are simply inverted so that holes are injected from the source side in the ON-state.

Annealing at 875°C. X-ray photoelectron spectroscopy reveals a TiN ratio of 47:53 and capacitance-voltage measurements a work function of 4.81 eV of the TiN. Further, a stack of 3 nm Ti and 37 nm Pt is deposited by sputtering and structured by means of an EBL-based lift-off. The resulting \( \Omega \)-shaped gate architecture can be seen in Fig. 1b. TiN is then etched around the gates by a mixture of H2O, ammonia water and H2O2.

Source/drain contact areas are defined by another EBL. The oxide shell is locally removed by a dip in NH4F buffered HF and 40 nm Ni are sputtered. After removing undesired Ni by a lift-off, a rapid thermal anneal at 450°C in forming gas atmosphere is performed to intrude Ni into the wire to create atomically sharp NiSi2/Si Schottky junctions below the gates [31].
grown oxide shell of a nanowire can induce changes in the band structure. This results in a reduced barrier height and effective tunneling mass of electrons which increases the on-current in n-configuration [34]. For holes the compressive stress has opposite effects so that p- and n-current can be equilibrated for a suitable oxidation time. Stress by the metal gate may also contribute to this current equalization [34]. In any case, the omega-geometry applies the stress of the gate stack almost ideally from all sides to the channel.

Transfer characteristics in Fig. 4 show that the on-current in p-configuration (803 nA) is in fact only factor 1.6 larger than in n-configuration (516 nA). Note that this symmetry is achieved for equal absolute gate voltages $|V_{CG}| = |V_{PG}| = 2.8$ V. Considering the narrow cross-section (circa 56 nm²), a remarkable current density of up to 14.3 mA/µm² is achieved. Higher total currents can be achieved by stacking multiple nanowires and reducing the channel length [2], [23], [35]. For a stack of multiple 10 nm wide nanowires and gate spacings and widths of both 10 nm, on-currents per width are simulated to reach that of low-standby-power CMOS transistors of the 5 nm node [35], [36].

Our RFET further offers a low hysteresis and a high on/off current ratio for both configurations when considering $V_{CG} = 0$ V as off-state. The off-current even remains low for high reverse CG voltages because the gate leakage currents are very low and – in contrast to SB-MOSFETs – a reverse carrier injection from drain is effectively blocked by the PG.

Fig. 5 compares the results to prior art Si-based RFETs based on uniform benchmark criteria to accommodate for their versatile architectures and measurement settings. The gate at the drain is always considered as the PG while the independent gate at the source or in the middle of the channel is the CG. The operation points are chosen for equal absolute voltages in both configurations whenever possible, i.e. for $V_{DS} = -V_{DP}$, $V_{PGN} = -V_{PGP}$ and $V_{CGN} = -V_{CGP}$. Note that if p-configuration has been unusually measured at positive $V_D$, all voltages refer to this as the real ground potential. Then $V_S = -V_D$ at source is the real drain potential. Amongst the applicable operation points, the maximal current densities (on-state) and the current at $V_{CG} = 0$ V (off-state) are extracted. This work presents the first bottom-up fabricated Si-based RFET to exceed the high on-current densities of the bottom-up RFET [9]. Coincidently, the on-currents are similar and the on/off ratio is very high for both configurations.

The subthreshold swing $SS$ reaches 128 mV/dec for p- and 142 mV/dec for n-configuration. Lower values down to 63 mV/dec (6 mV/dec with impact ionization) for bottom-up fabricated RFETs have only been reported when the CG controls the middle of the channel to create potential barriers for already injected carriers [23], [26], [28]. In this work by contrast the CG is at the Schottky junction and directly tunes the injection of carriers. This gating approach has always resulted in $SS \geq 150$ mV/dec in silicon-based RFETs [8]–[10], [25].

Output characteristics are presented in Fig. 6 for simultaneously varied potentials at CG and PG. The current saturates when the carriers can leave the channel at drain without a barrier. A deferred and non-linear rise of negative curvature is notable in the n-configuration being typical for Schottky-junction-based devices [37], [33]. It probably originates from the tunneling barrier for electrons at the drain caused by the $V_{PG}$ to $V_D$ potential difference. As $V_D$ rises, the barrier width decreases, leading to the initially exponential increase in tunneling transmission. By contrast, due to the lower NiSi₂-Si Schottky barrier for holes than for electrons, the holes can already tunnel with high probability in p-configuration even for low $V_D$. With increasing $V_D$, the thermal emission increases so that $I_D$ rises linearly. For low gate voltages in n-configuration a slightly risen current at high $V_D$ can be observed. It originates from the reverse injection of holes from the drain due to the rising gate-drain potential difference.

IV. SUMMARY

A reconfigurable FET with symmetric transfer characteristics is fabricated in a top-down manner. It exhibits minimal hysteresis, high on- and low off-currents for both, n- and p-configuration. This shows the importance of a narrow nanowire channel and encasing gate especially for RFETs.

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