Article

Analysis and Design of Harmonic Rejection Low Noise Amplifier with an Embedded Notch Filter

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Abstract: This paper presents the analysis and design of the harmonic rejection (HR) low-noise amplifier (LNA) with the fully passive source degeneration notch filter. The proposed HR LNA provides the rejection for the strong harmonics (3rd) of the local oscillator (LO) frequencies, where the HR mixer does not provide sufficient HR performance. The proposed 3rd harmonic notch filter modulates the source degeneration factor and the impedance matching performance thereafter. This effect further helps the blocking of the harmonic signal. The proposed LNA provides 11 dB gain at the fundamental frequency (2.1 GHz) while rejecting the 3rd harmonic component by 37 dBc. Compared to the conventional LNA, the 3rd harmonic notch performance is improved by 23 dB. Additionally, the LNA achieves a minimum noise figure of 3.1 dB, third order input intercept point (IIP3) of 0.5 dBm, input reflection (S11) below −10 dB from 1.8 GHz–2.3 GHz operational frequency range, and consumed 19 mW of power from a 1.2 V supply.

Keywords: down-conversion mixer; harmonic-rejection; local-oscillator; notch-filter; receiver; source-degeneration LNA

1. Introduction

The switching mixer down-converts the harmonics of the local oscillator (LO) signal and corrupts the desired signal in RF receivers. The de-sensitization due to the harmonics is not the exception for the narrow-band receivers. In the architecture of a radio-frequency (RF) receiver, the frequency conversion circuit, also known as a down-conversion mixer, is used to shift the desired RF channel signal to either the base-band or intermediate-frequency (IF). A frequency translation can be achieved by breaking the linear time-invariant (LTI) property and the linear time-varying switching mixer is the norm for modern RF receivers due to its superior performance in terms of the conversion gain and noise figure [1–3].

The switching mixer, on the other hand, is notorious for harmonic spurious issue, where the square-wave-like local oscillator LO signal down-converts the interferences at the harmonics of the LO fundamental frequency (ωo) [4]. This harmonic alias is a serious problem for broadband radio, where the larger blockers are passed upon the receiver without any pre-filtering (attenuation) and thus harmonic rejection (HR) mixer has to be used, albeit with a circuit complexity and an in-sufficient HR performance [5,6].

An HR issue is considered irrelevant for narrowband radio along with the off-chip filtering components. However, recent trends favor the wide-band analog front-end in order to cover vastly different frequency bands and to lower the cost of the RF transceiver, especially in Long Term Evolution (LTE) [7]. Thus, blocker signals may reach the HR mixer where the harmonic alias rejection is usually in the range of 40–50 dBc only [5,6,8].
We propose the HR LNA with a source degeneration notch filter embedded within the amplifying stage. The novelty of the proposed HR LNA is due to features which include: (1) the harmonic filtering occurs before the current to voltage conversion in the load of the LNA and thus the desensitization due to the strong blockers is prevented in the first stage of the receiver chain; (2) the harmonic rejection requirement on the HR mixer is significantly relaxed with the help of HR LNA; (3) the proposed source degeneration notch filter is fully passive and incurs no additional current consumption, and; (4) the source degeneration factor is modulated for the rejection of 3rd harmonic and the blockers around 3\(\omega_o\) of the LNA is reflected across the antenna-LNA interface.

2. Proposed Notch LNA

Figure 1 shows the proposed LNA architecture which is based on the inductor degenerated LNA architecture [9]. Instead of the inductor degeneration, the proposed LNA has the LC resonator as the degeneration component, where the desired resonance is at 3\(\omega_o\). The degeneration capacitor \(C_s\) is employed to form a parallel LC notch filter at the 3\(\omega_o\) to provide the required filtering of the third harmonic components.

The impedance \((Z_s)\) of the LC resonator with finite quality factor \((Q_s)\) of the inductor is expressed as [10]

\[
Z_s(s) = \frac{1}{s \cdot C_s} \left| \left( R_s + s \cdot L_s \right) \right|
\]

\[
Z_s(s) = \frac{R_s \cdot (1 + s \cdot \frac{L_s}{R_s})}{1 + s \cdot \frac{L_s}{Q_s} \cdot C_s + s^2 \cdot L_s \cdot C_s} = \frac{R_s \cdot (1 + s \cdot \frac{L_s}{R_s})}{1 + s \cdot \frac{1}{\sqrt{L_s \cdot C_s}} + \left( \frac{s}{\omega_s} \right)^2},
\]

where \(R_s\) is the series resistance due to the finite \(Q_s = \frac{\omega_o L_s}{R_s}\) of the inductor and \(\omega_s = \frac{1}{\sqrt{L_s \cdot C_s}}\) is located at 3\(\omega_o\) harmonic frequency (3\(\omega_o\)). Then, the effective input impedance \((Z_{in})\) exhibits two distinct characteristics at the desired operating frequency range \((\omega_o)\) and undesired 3\(\omega_o\) harmonic frequency range (3\(\omega_o\)).
With $g_{m1}$ as the trans-conductance of $M_1$, $Z_{in}(s)$ can be expressed as

$$
Z_{in}(s) = s \cdot L_g + \frac{1}{s \cdot C_{gs}} + Z_s \cdot (1 + \frac{g_{m1}}{s \cdot C_{gs}})
$$

$$
\approx R_s + \frac{g_{m1}}{C_{gs}} \cdot L_s + s \cdot (L_g + L_s) + \frac{1}{s \cdot C_{gs}}, \text{ around } \omega_o
$$

$$
\approx Q_s^2 \cdot R_s + s \cdot L_g + \frac{\omega_o^2 \cdot Q_s^2 \cdot R_s}{s \cdot (C_{gs} + C_s)}, \text{ around } 3\omega_o,
$$

Equation (3) manifests the large real impedance ($R_s$) and the series parasitic resistance of the inductor load, $L_s$, around $\omega_o$. From the simulation, $Q(\omega_o)$ and $Q(3\omega_o)$ are obtained to be 4.74 and 0.18 respectively. Then, $G_m$, recorded a boosting factor of 4.74 at $\omega_o$.

The proposed LNA with a source degeneration notch filter is advantageous for the gain at the fundamental frequency ($\omega_o$). The effective trans-conductance of the proposed circuit before the current to voltage conversion in the load can be expressed as follows.

$$
G_m = Q(s) \cdot \frac{g_m}{1 + g_m \cdot Z_s(s)}.
$$

where $Q(s)$ is the effective quality factor of the input impedance ($Z_{in}(s)$) and depends on the operating frequency ranges as depicted below [4].

$$
Q(\omega_o) = \frac{1}{\omega_o \cdot 2RE_m \cdot C_{gs}}.
$$

$$
Q(3\omega_o) = \frac{3\omega_o \cdot L_g}{Q_s^2 \cdot R_s + R_{ant}}.
$$

Equations (8) and (9) are calculated based on the frequency-dependent source degeneration impedance, whose impedance ($Z_s(s)$) behaves as an inductor ($\approx L_g$) and a resistor ($\approx Q_s^2 \cdot R_s$) at the fundamental ($\omega_o$) and 3rd harmonic ($3\omega_o$) frequencies. $R_{ant}$ is the impedance seen into the direction of antenna (usually 50 ohms). From the simulation, $Q(\omega_o)$ and $Q(3\omega_o)$ are obtained to be 4.74 and 0.18 respectively. Then, $G_m$, recorded a boosting factor of 4.74 at $\omega_o$.

The output impedance of the proposed LNA at $\omega_o$ is $Q_s^2 \cdot R_d$, where $Q_d$ and $R_d$ refers to the quality factor and the series parasitic resistance of the inductor load, $L_d$. Then, stand-alone LNA requires the output buffer, whose impedance is ideally matched to the measurement port (=50 Ω). Figure 2 shows the schematic of the source follower circuit, from the figure, the transistors $M_{b2}$ and $M_{b3}$ constitute the main trans-conductor and the current bias respectively. Neglecting the body effect, the output impedance of the source follower buffer is given by

$$
R_{out} = \frac{1}{g_{mb2}},
$$

where $g_{mb2}$ is the transconductance of the source trans-conductor ($M_{b2}$).

Table 1 lists the device used in the LNA and output buffer. The design procedure of the harmonic rejection LNA is as follows. We choose the optimum quality factor of the input impedance at $\omega_o$, which is also the function of $C_{gs}$ (and device width of main trans-conducting transistor, $M_1$). The current
consumption of the amplifier is dictated by the power budget. In our design, the proposed LNA consumed 15.8 mA and subsequently we could determine the dc bias, trans-conductance of $M_1$, and the overdrive voltage of $M_1$. Required real impedance of 50 Ω along with the resonance at $\omega_0$ dictates the inductance at the source and the gate. The capacitor at the source has the desired harmonic resonance at $3\omega_0$ and thus we could easily determine the required capacitor size given the inductance ($L_s$). The transistor $M_2$ as the cascoded device as well as the load resonator ($L_d$, $C_d$) are carefully designed while optimizing the current transfer due to $M_2$ and maximizing the load impedance at $\omega_0$.

![Schematic of the source follower output buffer.](image)

**Figure 2.** Schematic of the source follower output buffer.

**Table 1.** Device Dimension.

| Component | Size       |
|-----------|------------|
| $M_1$     | (450 µm/40nm) |
| $M_2$     | (300 µm/40nm) |
| $L_s$     | 1.7 nH     |
| $C_s$     | 500 fF     |
| $L_d$     | 4 nH       |
| $C_d$     | 700 fF     |
| $L_g$     | 15 nH      |
| $M_{1b}$  | (3 µm/40nm) |
| $M_{2b}$  | (13.5 µm/40nm) |
| $C_{AC}$  | 4.2 pF     |
| $R_{bias}$| 2.0 KΩ     |

### 3. Verifications

The proposed LNA was implemented with TSMC 40 nm CMOS technology and verified with Cadence Virtuoso. The final layout of the proposed LNA with an embedded notch filter is shown in Figure 3.
Due to the large value of the gate inductor ($L_g$) required, it is placed off-chip, providing much higher quality factor than the on-chip realization. A total area of 0.441 mm $\times$ 0.731 mm including the pad was achieved. An important compromise was made between lower metal layers and higher metal layers to avoid too much parasitic capacitance effect which leads to frequency shift and gain reduction. The lower metals are used in the layout of the LNA core to minimize parasitic capacitance effect. The LC resonators are positioned relatively far from each other and also the active devices, hence the need to employ high metal layers to minimize series resistance on the connecting metals.

The frequency response of $Z_{in}(s)$ is shown in Figure 4. The LNA exhibits a real impedance of about 50 $\Omega$ around the fundamental frequency while presenting extremely high impedance at $3\omega_o$ as presented in Equation (3). At $3\omega_o$, the effective resistance is a function of the antenna resistance and the square of the effective quality factor.
to occur around $3\omega_0$. The LC resonator’s reactance increases extremely near the cut-off frequency resulting in a gain reduction of about 14 dBc without the notch filter. With the addition of the notch filter, the attenuation is further improved at $3\omega_0$ by 23 dBc. The gain difference for the conventional and the proposed embedded notch filter LNA is only 1.5 dB at the fundamental frequency (2.1 GHz).

![Figure 5](image-url)

**Figure 5.** Gain performance of the proposed notch LNA compared to the conventional LNA.

Figure 6 shows the input reflection of the conventional versus the proposed LNA. The input reflection ($S_{11}$) is below $-10$ dB for a frequency range of 1.9 GHz–2.5 GHz without the notch filter. However, $S_{11}$ with the notch filter has a frequency range of 1.8 GHz–2.3 GHz. It clearly shows a slight frequency shift, which is as a result of the degeneration capacitor ($C_d$) and other undesired parasitic effects resulting from the layout.

![Figure 6](image-url)

**Figure 6.** Input reflection ($S_{11}$) performance of the proposed notch LNA compared to the conventional LNA.
The large signal noise figure performance of the proposed LNA is depicted in Figure 7. The large blocker tone at $3\omega_o (=6.3$ GHz) is imposed on the LNA input while its power is varied from $-10$ dBm to $30$ dBm. The proposed LNA exhibits 0.2 dB higher NF compared to the conventional LNA. On the other hand, the benefit due to the proposed notch LNA is evident from the large-signal NF results with $>15$ dBm blocker level.

![Figure 7](image1.png)

**Figure 7.** Large signal noise figure performance of the proposed notch LNA compared to the conventional LNA.

The source follower buffer with an output impedance of $\frac{1}{\text{g}_{\text{mb}}^2}$ is designed to achieve an output reflection of less than $-20$ dB as shown in Figure 8.

![Figure 8](image2.png)

**Figure 8.** Output reflection ($S_{22}$) performance of the proposed notch LNA compared to the conventional LNA.
The LNA also demonstrated a very good input third-order intercept point (IIP\textsubscript{3}) performance of about 0.5 dBm as shown in Figure 9.

![Figure 9. Input third-order intercept point (IIP\textsubscript{3}).](image)

Table 2. Performance Comparison of Conventional versus Proposed Notch LNAs, [input power = −50 dBm].

| Architecture | Frequency | Sensed at V\textsubscript{a} (dBm) | Sensed at V\textsubscript{b} (dBm) |
|--------------|-----------|----------------------------------|----------------------------------|
| Conventional | 2.1 (GHz) | −39.7                            | −37.98                           |
|              | 6.3 (GHz) | −55.64                           | −65                              |
| Notch        | 2.1 (GHz) | −39.54                           | −38.7                            |
|              | 6.3 (GHz) | −65.44                           | −87                              |

Table 2 gives the power at the gate of the input transistor and that of the drain of the cascode transistor when fed with an input signal tone of −50 dBm. The power gain/attenuation is obtained by assigning output ports at nodes V\textsubscript{a} and V\textsubscript{b} shown in the schematic of Figure 1. The gain/attenuation is observed at both the fundamental and third harmonic frequencies which are very close to that of the S\textsubscript{21} parameter for the conventional as well as the notch LNA.

A comparison of this work with other related works is given in Table 3. Some of the works in (Table 3) did not provide explicit performance for the harmonic rejection and thus are estimated from the gain (S\textsubscript{21}) performance. Our work demonstrated the best harmonic rejection performance with a superior noise figure and better linearity.
Table 3. Performance Comparison.

| Specification | This Work | [11] | [12] | [13] | [14] | [15] | [16] | [17] |
|---------------|-----------|------|------|------|------|------|------|------|
| Harmonic Rejection (dBc) | 37 | 12 | 14* | 10* | >20 | 20 | 29 | 18* |
| Gain (dB) | 11 | 18.7 | 10.34 | 30 | 12–24 | 13.4–14+ | 24.2a | 16.5 and 11.1 |
| NF (dB) | 3.1 | 4.8 | 3 | 2.8 | 3.5–5.84 | 4.4* | 6.4a | 3.1 and 3.7 |
| Supply (V) | 1.2 | 1.2 | 1.8 | 1.2 | 1.2 | 1 | 1.2 | NA |
| IIP3 (dBm) | 0.5 | –2 | –27, –22 | –11 | –15 to –12 | –3.3 to –2.8* | –12.5 | –4.84 –8.31 |
| Pconsumption (mW) | 19 | 12.4 | 24.1 | 14 | 8.64 | 23.8b | 9.6 | NA |
| Technology (CMOS) | 40 nm | 240 nm | 180 nm | 130 nm | 65 nm | 65 nm | 65 nm | 180 nm |

* Harmonic rejection performance is estimated from their gain performance. † Simulation results for LNA only. a Receiver. c Cascaded noise figure.

4. Conclusions

In this paper, the harmonic rejection LNA with an embedded notch filter as the source degeneration component is proposed to enhance the filtering of 3rd harmonic signals in an RF receiver system. The frequency-dependent source degeneration impedance, the LNA input impedance, as well as the signal gain/attenuation at both the fundamental and 3rd harmonic frequencies of the notch filter are analyzed, and the various equations give an accurate relation with that of the simulated results. The simulation results verify that the proposed LNA can attenuate third harmonic signals by 37 dBc while providing a sufficient gain of 11 dB at the fundamental frequency. The LNA demonstrated the noise figure of 3.1 dB with a large blocker tone of 5 dBm at 3ωo imposed upon the LNA input.

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