PECVD and Thermal Gate Oxides on 3C vs. 4H SiC: Impact on Leakage, Traps and Energy Offsets

T. Gutt, a,b H. M. Przewlocki, a,b, K. Piskorski, a A. Mikhailov, b and M. Bakowski b

a Institute of Electron Technology, Warsaw 02-668, Poland
b Acreo AB, Kista SE-164 40, Sweden

Energy-band model offsets, trap density distributions and gate leakage characteristics of MOS capacitors with PECVD and thermal gate oxides on 3C-SiC and 4H-SiC were compared. The difference in trap energy distributions between the polytypes confirmed the lesser 3C-SiC polytype vulnerability to near-interface traps (NIT), which are alternatively found in high density in the 4H-SiC.

It was also shown that the quality of the PECVD oxides obtained in this experiment were comparable to that of the thermal oxide. Only a slight increase of leakage current was observed in the PECVD oxides due to oxide inhomogeneity in the lower electric field interval of the Fowler-Nordheim range. Finally, the energy band model of the SiC MOS devices was described quantitatively for different combinations of polytype and oxidation method, which illustrated the influence of technological processing on the energy offsets and potentials, and could be used for further development of the devices and processes.

© The Author(s) 2015. Published by ECS. This is an open access article distributed under the terms of the Creative Commons Attribution 4.0 License (CC BY, http://creativecommons.org/licenses/by/4.0/), which permits unrestricted reuse of the work in any medium, provided the original work is properly cited. [DOI: 10.1149/2.0101509jss] All rights reserved.

Manuscript submitted March 30, 2015; revised manuscript received July 27, 2015. Published August 6, 2015. This was Paper 1986 presented at the Cancun, Mexico, Meeting of the Society, October 5–9, 2014.

Silicon carbide (SiC) is particularly suitable for manufacturing of medium and high power field effect transistors. The two SiC polypotypes, i.e. cubic 3C and hexagonal 4H, most commonly used for that purpose, differ, however, in many aspects, which influence the operation of the electronic devices. The most important difference is in the width of the energy gap, 2.4 eV in 3C-SiC and 3.26 eV in 4H-SiC, which influences trapping properties of typical SiO2:SiC interface defects, and determine such MOS system energy offsets as effective contact potential difference, for instance. High density of traps and their continuous distribution across the band-gap in case of the thermal SiO2:SiC interface, causes carrier mobility degradation in MOS devices on SiC. Hence the possibility of achieving low temperature gate oxides with low density of interface traps using layer deposition techniques such as PECVD has been intensively investigated in SiC.

However, the leakage current in such oxides may be higher than in the thermal SiO2. Since it is one of the most important factors deciding about MOSFET operation in high voltage/temperature modes, the leakage current must also be strictly controlled.

Taking all that into account, the purpose of this work was to compare the important features of MOS devices, namely interface trap distributions, gate leakage behavior and energy band model offsets on both 3C-SiC and 4H-SiC polytypes and two oxide preparation methods – thermal SiO2 and post-deposition treated PECVD.

**Experimental**

Samples.— Characterized were two lots of wafers fabricated by Acreo AB. The 3C-SiC lot consisted of two n-type (001) 3C-SiC 3° wafers. The 200 μm thick substrates from Hoya, with the doping density of 5 × 1018 cm−3 were covered at Acreo by a 12 μm thick n-type epitaxial layer with nitrogen doping of 7 × 1015 cm−3. One of the wafers was thermally oxidized in wet oxygen under atmospheric pressure for one hour at a temperature of T = 1150°C, while the second wafer had the SiO2 layer deposited by PECVD at T = 300°C. This second wafer was further annealed for 3 hours in wet oxygen at a temperature of T = 950°C. The oxide thickness on both wafers was approx. 60 nm. The wafers were divided into quarters and different metals (Al, Au, Ni), were deposited on each quarter by ion beam sputtering, as well as polysilicon which was deposited by chemical vapor deposition (CVD). Circular gates were formed by lift-off in case of metal gates and by etching in case of polysilicon.

The 4H-SiC lot consisted of two n-type (0001)-orientation wafers having the epi-layers of similar width and doping as in the 3C case: one with the gate oxide fabricated in a standard thermal oxidation process under atmospheric pressure at 1250°C in N2O:N2(1:3) ambient for 14 hours, and the second with a PECVD silicon nitride/silicon dioxide gate stack. Deposition of the silicon nitride / silicon dioxide stack by PECVD method was performed in the following process: 50nm/45nm were targeted, chuck temperature 300°C, HF Power 20W with subsequent oxidation in dry oxygen at 1150 degrees for three hours at normal pressure. The PECVD oxide thickness was equal to 45 nm, and in case of the thermal oxide the thickness was equal to 53 nm. Each wafer was divided into four quadrants corresponding to deposited different electrode metals – namely Al, TiW, Ni and Au.

In both cases the semi-transparent electrodes were made (gate thickness xg ≈ 25 nm) in order to enable photo-electric measurements.

Measurements.— The interface trap distributions were measured by conductance method on Agilent 4294A impedance analyzer. The C(V)/G(V) characteristics of a number of MOS capacitors were measured in the frequency range from 100 Hz to 1 MHz at the room temperature T = 295 K and in the gate voltage interval from accumulation to deep depletion, covering the interface traps in the upper part of the energy gap. The parallel conductance Gp was calculated from the measured G(V). In order to position the parallel conductance Gp spectra in the energy scale the following procedure was adopted. The substrate doping concentration ND was established from the slope of the C−2(V) characteristic in depletion using the standard method. Using the doping concentration, ND, it was possible to calculate the ideal capacitance vs. surface potential or band bending, C(φs), characteristics. The gate voltage vs. band bending mapping, V vs. φs, was achieved by matching the measured C(V) vs. the ideal C(φs) characteristics at equal capacitance values C.

The energy band model offsets were established using our own specialized equipment for photo-electric measurements and our original measurement methods. The methods used were described in detail in. Generally, they consist in measuring the interaction of light having specific properties (defined wave length, power and spot size), with the examined MOS structure through a transparent gate of the thickness of about 25 nm in the case of most metals.

The band diagrams are determined by a combination of photoelectric and optical measurements. In photoelectric measurements, photocurrents are generated by the light beam of variable wavelength λ illuminating the device under test (DUT) from the gate side. The origin of the photocurrent depends on the polarity of the gate bias supplied by the measurement system. In case of positive gate bias supplied by the system the photocurrent consists of electrons photo-emitted from

*Electrochemical Society Active Member.

**E-mail:** tgutt@iee.waw.pl
Figure 1. Trap density distributions $D_{it}$ measured in the samples on 4H- and 3C-SiC. Each curve presents a $D_{it}(E)$ characteristic of a specific (gate metal):oxide preparation method:(substrate polytype) combination. Typical density levels of NIT, carbon clusters and dangling bonds are marked after Krieger et al.\textsuperscript{2}

the substrate, over the potential barrier, $E_{aS}$, at the substrate-dielectric interface, drifting toward the gate, while in case of negative gate bias the photocurrent consists of electrons photo-emitted from the gate, over the potential barrier, $E_{aG}$, at the metal gate - dielectric interface, drifting toward the substrate. Due to the interference of light in the gate stack, the light power absorbed by the electron emitter (substrate or gate) changes with changing the wavelength of light illuminating the DUT. Hence, the dependence of light power absorbed by the emitter on the wavelength of light has to be found. This is done by the optical methods, using the ellipsometric/spectrophotometric determination of the gate electrode and gate stack thickness, as well as of the refractive, $n$, and extinction, $k$, coefficients of materials constituting the MOS structure, in function of the photon energy, $\nu$. Two ellipsometers – J.A. Woolam VASE and Horriba-Jobin-Yvon VUV2 (deep UV), were used for the purpose of this investigation. Once the thickness of the layers and the $n(\nu)$ and $k(\nu)$ characteristics of the materials of gate, dielectric and substrate are known, the dependence of the fractions of light power reflected from the structure, $R(\nu)$, transmitted through the gate, $T(\nu)$, and absorbed by the substrate, as well as the fraction absorbed by the gate, $A(\nu)$, can be calculated by the methods described e.g. in.\textsuperscript{7,12} The Fowler measurement method\textsuperscript{2,11} is applied to determine the barrier heights at the gate-SiO\textsubscript{2} interface, $E_{aG}$, and at substrate-SiO\textsubscript{2} interface, $E_{aS}$. The effective contact potential difference, $\phi_{cS}$, was determined using our original photoelectric measurement method, which in our opinion is the most accurate of the existing $\phi_{cS}$ measurement methods.\textsuperscript{3}

The gate leakage current measurements were taken on Agilent B1500AB Device Analyzer.

Results

Trap distributions.— One of the most important differences between 3C-SiC and 4H-SiC polytypes is the width of the energy gap. The distance from the valence band $E_{V}$, which is assumed common in all SiC polytypes, to the conduction band of 3C is 2.36eV, while that of 4H is 3.23 eV,\textsuperscript{11} which makes 3C based MOS devices less vulnerable to the interface traps located above 2.36 eV.

Based on the assumption that all SiC polytypes share the same $E_{V}$ level, in order to compare the interface trap distributions it is convenient to use the $E_{V}$ as the base level. In Fig. 1 we present trap density $D_{it}$ energy distributions measured in the 3C-SiC and 4H-SiC samples. The energy axis shows the energy distance of a trap $E_{it}$ from the top of the valence band $E_{V}$ (from right to left) and is common for all samples. Each curve presents a $D_{it}(E)$ characteristic of a specific gate metal:oxide type:substrate polytype combination. As it could be expected, the $D_{it}$ values in the vicinity of $E_{V}$ in 4H-SiC are essentially higher than those in 3C-SiC, irrespective of the oxide preparation method.

In general, three different types of traps are responsible for the distribution of $D_{it}$ in SiC:SiO\textsubscript{2} interfaces.\textsuperscript{2} First, the dangling bonds, which can be passivated by hydrogenation, hence they contribute in very small density. Second, the carbon clusters located at the interface, formed during oxidation of SiC from the residual carbon which is not volatilized as CO or CO\textsubscript{2}, and which exist in the interface in very high density, distributed continuously across the band-gap. Third, the so called near interface traps (NIT), which exist in very high densities at approximately 70 meV below the bottom of the conduction band in 4H-SiC. According to Afanas'ev\textsuperscript{,1} they are probably caused by oxygen vacancy defects ($O_3\equiv O_3$) or Si\textsubscript{2}C\textsubscript{2}H\textsubscript{2}S\textsubscript{2}H\textsubscript{2} defects ($O_3\equiv O_3$) located in the oxide at 1.5–2 nm from the interface at an energy position of 2.77 eV below the conduction band edge of SiO\textsubscript{2}. The energy distribution of NITs is narrow and electrons have to overcome a barrier $\phi \approx 0.2$ eV in order to be captured by or emitted from the NITs.\textsuperscript{2} In case of 3C-SiC NITs are located in the conduction band and do not contribute to $D_{it}$.

It is also worth to notice that the nitridation of the SiO\textsubscript{2}:SiC interface in the 4H sample would lower the $D_{it}$ level compared with the 3C sample.

The results of our experiments are shown in Fig. 1 in the identical way as done by Krieger.\textsuperscript{2} Due to the limitation of the conductance method, only the upper part of the $D_{it}$ distributions could be measured, hence the 4H measurements are shown above 2.4eV, and 3C above 1.4eV from their common valence band level.

One can notice that in Fig. 1 the $D_{it}$ distributions achieved for both oxide preparation methods and for all gate electrode materials within the specific SiC polytype are gathered pretty close together with very little scatter due to good interface quality.

Comparing those results with the Krieger's\textsuperscript{2} we can notice that the results fit the same chart pretty well, both as to the magnitude of the $D_{it}$ and with respect to the energy depth. We can observe the NIT region in the 4H sample. Then the band of traps generated by carbon clusters. The presence of carbon clusters in PECVD samples can be explained by the thermal oxidation step after oxide deposition used for improvement of the oxide breakdown properties. The dangling bonds seem to be passivated and their density is entirely screened by the carbon cluster traps in all samples.

We can also see that the densities of interface traps achieved in this experiment, both for PECVD and thermal oxides, are lower than reported by Krieger.\textsuperscript{2}

Leakage currents.— Another interesting difference between the samples can be demonstrated in the gate leakage currents. In Fig. 2 we present the averaged leakage current density vs. electric field ($J$-$F$) characteristics, measured in all four samples.

First, it can be noticed that the difference between the leakage currents in 3C and 4H samples is huge. Since the 3C-SiC substrates used in this study were known to have much higher density of dislocations than the 4H-SiC substrates, we may attribute that difference in leakage properties to high density of defects in 3C-SiC.

Second, there is a very small difference in the leakage current density between the PECVD and the respective thermal gate oxide within 4H-SiC samples. The leakage currents in both samples on 4H-SiC are lower by two decades than those on 3C. Especially in the electric field interval below 6 MV/cm. Above that field the leakage current increases steeply.

The further investigation of the PECVD and the thermal oxide leakage in higher electric field - above 6 MV/cm (only positive gate voltages taken into account) - leads to a conclusion that the main leakage mechanism in this interval is Fowler-Nordheim's.

Figure 3 presents the $J$-$F$ characteristics from Fig. 2 in Fowler-Nordheim model coordinates. The Fowler-Nordheim model results in a straight line (negative proportionality) of the $\ln(J/F^2)$ on the inverse of the electric field. As shown in Fig. 3, the 4H-SiC $J$-$F$-characteristics
Figure 2. Gate leakage current density vs. electric field in 3C and 4H samples for PECVD and thermal oxide preparation methods and Au electrode.

Figure 3. Data from Fig. 2 presented in Fowler-Nordheim coordinates. The slope of the linear part of the 4H-SiC/THERMAL characteristic is 1.6863 \times 10^8 \text{V/cm}.

in the thermal oxide samples reveal dominating Fowler-Nordheim mechanism in the 6 MV/cm to 8 MV/cm range.

In the 5 MV/cm to 7 MV/cm interval, the |J|-F characteristics exhibit higher inhomogeneity in the PECVD oxide layer compared with the thermal oxide, resulting in a deviation from the straight line F-N model.

Energy-band model.— The two most important problems related to the quality of the SiC-dielectric interfaces are: - high densities of interface states (1–2 orders of magnitude higher than Si-SiO₂ interface), which are responsible for low mobility of carriers in channels of MOS transistors; and the problem of achieving required and stable values of the MOS transistor threshold voltage \( V_T \). This latter problem is in other words the problem of the Effective Work Function Difference tuning in the MOS system. In light of the expected growth of applications of MOS systems on Wide Band-Gap semiconductor substrates this problem will soon become of prime importance for device engineers. Solving that problem requires exact knowledge of the energy band model offsets.

| Structure | \( E_{BG} \) eV | \( E_{BS} \) eV | \( E_{VG} \) eV | \( E_{VS} \) eV | \( \chi \) eV | \( \phi_F \) V | \( \phi_{SO} \) V | \( V_{GB} \) V |
|-----------|----------------|----------------|----------------|----------------|---------------|---------------|---------------|---------------|
| PECVD     | 3.43           | 5.47           | 5.47           | 3.43           | 3.09          | -0.961        | 0.097         | 0.126         |
| thermal   | 3.478          | 5.731          | 5.422          | 3.169          | 2.499         | -1.412 -0.112 | 0.527         |

The most important energy-band model offsets in a MOS capacitor consisting of the Al gate electrode, PECVD oxide gate insulator, on the 3C-SiC and 4H-SiC substrate are presented in Table I. The meaning of the offset values is given in Fig. 4. It is worth noticing that due to technological reasons some offsets differ in 3C and 4H samples, although those differences are not related to the substrate in any way, e.g. Al-SiO₂ barrier height \( E_{BG} \).

In the second example, presented in Table II, we compare 4H-SiC Al gate capacitors having thermal or PECVD gate insulator. It is important to notice that all energy offsets depend on the technological process history and may differ from those referenced in the literature. Hence, in device design it is reasonable to use the verified, measured parameters in order to be able to tune the energy offsets to required values.

Conclusions

The trap energy distributions shown in Fig. 1 demonstrate considerably higher density of traps in 4H-SiC compared to 3C-SiC close to the conduction band. That higher density of traps is caused by the NIT traps. In case of the 3C polytype the NIT traps are located in the conduction band, hence they do not influence the MOST channel operation. That confirms the advantage of the 3C polytype with respect to SiC MOST operation requirements where low trap density and high carrier mobilities are required.

Comparing PECVD versus thermal oxide, a slight increase of leakage is observed in the PECVD oxides due to oxide inhomogeneity.

The energy band model of the SiC MOS devices was determined quantitatively. The methodology and the results obtained prove repeatability and may be used for further development of the devices and processes.
References

1. M. Levinshtein, S. Rumyantsev, and M. Shur, Properties of Advanced Semiconductor Materials, John Wiley & Sons, UK (2001).
2. M. Krieger et al., Mat. Sci. Forum, 645-648, 463 (2010).
3. H. M. Przewlocki, Solid State Electron., 45, 1241 (2001).
4. A. I. Mikhaylov, A. V. Afanasyev, V. V. Luchinin, S. A. Reshanov, and A. Schöner, MRS Proceedings, 1693 (2014).
5. R. Singh and A. R. Hefner, Solid State Electronics, 48, 1717 (2004).
6. M. Nawaz, Active and Passive Electronic Components, 2015 (2015), art. ID 651527.
7. E. H. Nicollian and J. R. Brews, MOS (Metal-Oxide-Semiconductor) Physics and Technology, (Wiley, New York, 1982).
8. D. K. Schroder, Semiconductor Material and Device Characterization, 2nd ed. (Wiley, New York, 1998).
9. V. V. Afanasiev, Internal Photoemission, Elsevier, 2008.
10. K. Piskorski et al., Opto-Electron. Rev., 20, 67 (2012).
11. V. V. Afanasiev, Microel. Eng., 448, 241 (1999).
12. C. N. Berglund and R. J. Powell, J. Appl. Phys., 40, 5093 (1969).
13. R. H. Fowler, Phys. Rev., 38, 45 (1931).
14. L. M. Lin and P. T. Lai, J. Appl. Phys., 102, 054515 (2007).