A random-access-memory cell based on quantum flux parametron with three control lines

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Abstract. In this study, we proposed a random-access memory (RAM) cell composed of adiabatic quantum-flux-parametron (AQFP) circuits as a component of large-scale AQFP RAMs. The memory cell is composed of a storage QFP gate and a readout AQFP gate, which is controlled by three control currents \( I_0 \), \( I_y \), and \( I_z \). \( I_y \) is used to control an input datum. \( I_x \) is a column selection current for the write operation. \( I_s \) is a row selection current for both write and read operations. The control current margins evaluated in the simulation are larger than +/- 30%. We designed the memory cell of the size of 50 \( \mu \)m x 40 \( \mu \)m by using AIST high-speed standard process, and verified the correctness of its operation by experiments. It was shown that the amplitude of the control currents is compatible with the output currents of AQFP logic.

1. Introduction

Semiconductor integrated circuits have improved the performance by decreasing the feature size owing to the advancement of microfabrication technologies. However, an increase in heat generation from a chip due to the higher integration density becomes a crucial problem, which limits the enhancement of the performance of the present semiconductor integrated circuits.

Superconducting circuits are attracting attention as an integrated circuit technology for realizing high-end computers in the next generation because they can operate faster and consumes much less energy compared with the semiconductor circuits. Energy-efficient superconducting circuits based on rapid single flux quantum (RSFQ) circuits [1] have been proposed recently, which include eSFPQ [2], ERSFQ [3], RQL [4], and LV-RSFPQ [5]. We have been developing adiabatic quantum flux parametron (AQFP) circuits based on QFP circuits [6], which are extremely energy efficient superconducting circuits [7-10]. The AQFP circuit is a promising superconducting circuit for realizing ultra-low-power computing systems because the operating frequency can be 5 to 10 GHz and the bit-energy is about six orders of magnitudes lower than that of CMOS.

Large-scale random-access memories (RAMs) are necessary for realizing high-performance computing systems. There are several studies on large-scale memories using superconducting latching logic [11], partially using RSFPQ logic [12], and fully using RSFPQ logic up to date [13-14]. However,
for the generous use of the advantage of the AQFP circuits, reduction of the energy consumption of the memories is essential. Although flip-flops based on AQFP circuits have been proposed in previous study [15-17], their circuit area is not small enough for making high-density large-scale memories. Any RAMs for large-scale memories compatible with AQFP circuits have not been realized yet.

We aim to realize an AQFP-based RAM as a cache memory whose input/output signals are compatible with those of the AQFP circuits. Even though AQFP signals can be converted to SFQ pulses, the AQFP RAM is necessary for decreasing the access time of AQFP computing systems. The AQFP circuits use bipolar signals with amplitude about several tens of microampere. For example, +50 μA of current represents logic “1” and -50 μA of current represents logic “0”. Since the amplitude of control currents required for the memory cells in [11-14] is larger than 100 μA, we have to develop a memory cell drivable by the AQFP signals.

In this study, we have proposed a RAM cell composed of AQFP circuits with three control lines as a component of a large-scale AQFP RAM. The RAM cell is compatible with AQFP circuits, where the control currents are bipolar and their amplitude is the same level as that of the output current of AQFP gates. We have designed and implemented the RAM cell, whose cell size is 40 μm x 50 μm, using the AIST high-speed standard process (HSTP) [18]. The correct functions were obtained with large control current margins.

2. AQFP RAM system

An AQFP RAM system we proposed in this study is shown in figure 1. The RAM system consists of decoders, memory cells, multi-input OR gates, and a multiplexer (MUX), all of which are composed of AQFP circuits. The memory cells form a two dimensional array, where each cell is selected by three control currents, that is an x-direction current (I_x), a y-direction current (I_y) and a data input (I_d). The x-direction current (I_x) is commonly used in both write and read operations. In the write operation, a memory cell is selected by I_x and I_y and datum is written by I_d. In the read operation, memory cells in the same row are selected by I_x and the one of them is chosen by the multiplexer. The decoder of the

![Figure 1. An AQFP RAM system proposed in this study.](image)
AQFP RAM outputs a positive or negative signal to the selected address depending on its read/write modes and its input datum.

3. AQFP RAM cell with three control lines

Figure 2, 3, and 4 show a schematic, layout, and microphotograph of the AQFP RAM cell with three control lines proposed in this study, respectively. The 3D inductance extractor, InductEx [19], was used for extracting the value of self and mutual inductances from the layout. To obtain the compatibility with AQFP circuits, the RAM cell is composed of AQFP circuits. It consists of a storage QFP gate, which stores 1-bit information, and a read AQFP gate, which readsout the information stored in the storage gate. The storage QFP gate is biased by a DC current \( I_{wb} \) so that the QFP has a double-well-potential and behaves as a flip-flop with bistable states. It should be noted that the nonadiabatic switching occurs essentially in the memory cell when the stored datum is rewritten. The input of the read AQFP gate is offset by a DC current \( I_{rb} \) so that the readout of the gate becomes logic “0” when the memory cell is not selected. This is satisfied by setting the condition, \( I_{w2} > 0 \), because the read AQFP gate should not go to “1” state regardless of the state of the storage QFP gate when \( I_s \) is not enabled (when \( I_x \) is positive in this design), where \( I_{w2} \) and \( I_{x2} \) are the input current of the read AQFP gate caused by \( I_{fb} \) and \( I_s \), respectively.

![Figure 2. Schematic of an AQFP RAM cell with three control lines.](image)

A simulation result of the AQFP RAM cell with three control lines is shown in figure 5. The RAM cell uses three control currents \( I_a, I_y, \) and \( I_s \) for write and read operations, where \( I_d \) corresponds to input...
datum to be written, $I_y$ is the column selection current for the write operation and $I_x$ is the row selection current for both write and read operations. Logic “1” is written to the RAM cell when the directions of all three control currents are positive, while logic “0” is written when all of them are negative. The information stored in the RAM cell corresponds to the direction of the current $I_{st}$ in figure 2. The positive direction of $I_{st}$ means logic “1” and the negative direction means logic “0”. In the read operation, the RAM cells in the same row are read simultaneously when the direction of the current $I_x$ is negative. The readout current $I_{ro}$, which flows synchronously with the clock current $I_{clk}$, is equal to the readout result of the RAM cell.

We assume that the control currents $I_{dx}$, $I_y$, and $I_x$ are generated by AQFP circuits and that they are bipolar signals. The AQFP RAM system is driven by four phase clocks. The current $I_x$ and the clock current $I_{clk}$ are delayed by 90 and 180 degrees compared with the currents ($I_{dx}$, $I_y$), respectively. Because $I_x$ is control current for both write and read operations, the read gate must be excited by the clock current at the right time.

**Figure 3.** A layout of an AQFP RAM cell with three control lines.

**Figure 4.** A microphotograph of an AQFP RAM cell with three control lines.

**Figure 5.** A simulation result of an AQFP RAM cell with three control lines.
The simulated energy consumption of the 1-bit AQFP RAM cell operating at 5 GHz is ranging from 8 zJ to 10 zJ depending on its read/write operation modes. As the worst case scenario, we included bit-line and word-line drivers in each memory cell, which amplify the bipolar control currents \( I_d \), \( I_y \), and \( I_x \) for each memory cell. Relatively large energy consumption compared with a single AQFP gate [18] is

\[ I_{dc} \] while \( I_r \) is applied. The operation margin will be decreased if \( I_d \) and \( I_y \) are applied when the read gate is excited by the clock current \( I_{dc} \).

There exists a small offset current at the input of the storage gate caused by the DC current \( I_{wb} \) and the asymmetry of the layout. The parasitic magnetic coupling between the DC current line for \( I_{wb} \) and the inductances of the storage gate causes this offset in the storage gate. To obtain correct operation, the RAM cell designed in this study requires a DC offset current \( I_{offset} \), which is superposed on the control line for \( I_d \). The role of \( I_{offset} \) is the cancelation of the offset current caused by \( I_{wb} \). The DC offset current \( I_{offset} = 98 \mu A \) was applied in this simulation.

A measurement result of the RAM cell designed in this study is shown in figure 6. Several stages of AQFP buffers are connected to the RAM cell and the logic state of the last AQFP buffer is readout by using a dc-SQUID, which were magnetically coupled to the last buffer [7]. The result verifies that the write “1” and read “1” operation, and the write “0” and read “0” operation are successfully performed. Besides the operations for half-selection and non-selection modes are correctly obtained. It was also confirmed that the RAM cell is compatible with AQFP circuits because the amplitude of three control currents \( I_d \), \( I_y \) and \( I_x \) are the same level as the amplitude of output currents of AQFP circuits. The DC current \( I_{offset} = -45 \mu A \) was applied in the measurement. The polarity of \( I_{offset} \) is different from the simulation results, probably due to the unknown parasitic couplings in the actual device structure.

Simulated and measured operation margins of the RAM cell are shown in figure 7. It can be seen from the figure that while the margin for the DC current \( I_{wb} \) is as small as \( +/- 7\% \), the margins for control currents are larger than \( +/- 30\% \) in the simulation. It should be noted that \( I_{wb} \) can be applied by using the external current source, therefore its amplitude can be easily adjusted. From the figure one can also see that the measured margins for the control currents are shifted to the right side. However, we obtained the mostly reasonable measured margins because \( I_r \) has a wider operation margin than that of \( I_d \) and \( I_y \), and the critical margin appears in \( I_{wb} \).
due to the non-adiabatic switching of the AQFP RAM cell caused by the back action (the gate-to-gate interaction of AQFP gates). We can estimate the average energy consumption of the 4-kbit AQFP RAM to be 36 aJ ≈ (4 kbit) x (9 zJ) per clock period at 5 GHz operation because a memory system is implemented by simply connecting the AQFP RAM cell with bit-line drivers in two dimensional structure and the most of the energy is consumed in the memory cell array.

4. Conclusion
We proposed, designed and measured an AQFP RAM cell controlled by three control lines for read and write operations. The cell size is 40 μm x 50 μm and fabricated by using the AIST high-speed standard process. We confirmed correct operations of the RAM cell by measurements and showed that the amplitude of the data write current, the row and column selection current are compatible with the output current of AQFP circuits.

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