Organic electronic memory based on a ferroelectric polymer

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Abstract. Measurements of the capacitance of metal-insulator-semiconductor capacitors and the output characteristics of thin film transistors based on poly(3-hexylthiophene) as the active semiconductor and poly(vinylidenefluoride-trifluoroethylene) as the gate insulator show that ferroelectric polarisation in the insulator is stable but that its effect when poled by depletion voltages is partially neutralised by trapping of electrons at or near the semiconductor interface. Nevertheless, the combination of materials is capable of providing an adequate memory function.

1. Introduction
Organic thin film transistors (TFT) are an attractive option for low cost electronic applications and much progress has been made in fabricating prototype circuits for active matrix displays and for RFID applications [1,2]. To extend the range of applications there is a need to develop and optimise the performance of non-volatile memory devices that are compatible with the solution-processing fabrication procedures used in Plastic Electronics. A possible candidate is an organic TFT incorporating the ferroelectric co-polymer poly(vinylidenefluoride-trifluoroethylene), P(VDF-TrFE) as the gate insulator.

2. Device concept
Although TFTs are generally considered to be dynamic devices the basic operating mechanism relies on electrostatic attraction as the means for switching on the device as seen in Fig.1(a). Here a negative voltage, \(-V_G\), applied to the gate electrode attracts holes to the interface of the p-type organic semiconductor poly(3-hexylthiophene), P3HT, with the insulating P(VDF-TrFE) thus creating an accumulation layer. When a negative voltage, \(-V_D\), is applied to the drain electrode then a hole current, \(I_D\), flows through this layer from source to drain which, in the linear regime \(V_D<(V_G-V_T)\) is given by

\[
I_D = \frac{W}{L} \mu C_i (V_G - V_T) W_D
\]

and in the saturation regime \(V_D>(V_G-V_T)\) by

\[
I_D = \frac{W}{2L} \mu C_i (V_G - V_T)^2
\]

where \(W\) and \(L\) are the width and length of the induced channel, \(\mu\) the hole mobility, \(C_i\) the capacitance per unit area of the gate insulator and \(V_T\) the threshold voltage for the device [3]. If the
electric field applied to the gate insulator exceeds the coercive field of P(VDF-TrFE) then ferroelectric domains will be established whose remanent polarisation, see Fig. 1(a), will contribute additional electrostatic forces drawing additional holes into the channel. This in turn increases the channel conductance and hence the current flow between source and drain. Furthermore, if $V_G$ is reduced to zero, the remanent polarisation will maintain the device in its ‘ON’ state until it is reversed, after which the device should turn ‘OFF’.

These same processes can be observed by measuring the capacitance of a Metal-Insulator-Semiconductor (MIS) capacitor formed from the same materials (Fig. 1(b)). When the device is in accumulation, $-V_G$, the measured capacitance will be that of the gate insulator. When $V_G$ is positive, the P3HT layer is driven into depletion and the capacitance decreases owing to the formation of an immobile space charge region at the interface which has a capacitance inversely proportional to its width. At sufficiently positive $V_G$ the P3HT is completely depleted and the measured capacitance becomes constant and equal to the series sum of the insulator and gate layers. As in the case of the TFT if, in accumulation, the coercive field was exceeded resulting in a remanent polarisation with the orientation shown in Fig. 1(b) this will maintain the capacitor in accumulation as $V_G$ is swept from negative to positive voltages. Only when this polarisation is reversed at sufficiently high positive gate voltages will the normal depletion behaviour be observed in the device.

These basic concepts will now be used to explain results obtained from TFTs and MIS capacitors based on P3HT and P(VDF-TrFE). It will be shown, however, that additional interfacial effects occur which limit the efficiency of such devices as memory elements.

3. Experimental
All devices were prepared in a class 1000 Clean Room by sequentially spin coating two layers of P(VDF-TrFE) (65/35 mol %) from a 2- butanone solution onto a clean glass substrate furnished with evaporated Al electrodes. The semiconducting layer was spin-coated from a P3HT/chloroform solution after drying the P(VDF-TrFE) film at 120°C for ~12 hours under vacuum. The devices were completed by vacuum evaporating top gold electrodes (capacitors) or gold source/drain interdigitated electrodes with an aspect ratio, $W/L = 1485$ for the TFTs. All devices were then annealed at 90°C for 12 hours under vacuum. Typical insulator and semiconductor layer thicknesses were 0.3 μm and 0.05-0.08 μm as measured on reference samples with the Dektak 3 ST surface profiler. Dielectric measurements were performed with the Novocontrol Alpha A impedance analyzer in a temperature controlled nitrogen atmosphere with bias voltages applied to the Al electrode. TFT characteristics were measured under nitrogen using an Agilent 4155C Semiconductor Parameter Analyzer.

4. Results and Discussion
Fig. 2 show the capacitance-voltage plots obtained for the MIS capacitor using the programmed voltage cycle shown in the inset. Utilising this combination of uni- and bi-polar voltage sweeps Dickens et al [4] and Bauer [5] were able to decouple the underlying current-voltage characteristic of
their ferroelectric capacitors from effects associated with the reversal of ferroelectric polarisation. Similarly, because the measured capacitance per unit area, $C_m$, can be expressed as

$$C_m = C_i + \frac{dP}{dV}$$

(3)

where $dP/dV$ represents a voltage-induced change in the remanent polarisation, employing such a voltage sweep sequence also allows purely capacitive effects to be distinguished from the reversal of remanent polarisation as seen in Fig. 2. On the initial sweep to positive or negative voltages, the capacitance plots exhibit broad maxima. The return sweep and subsequent unipolar sweeps (dotted curves) show only the underlying behaviour expected of a MIS capacitor based on a p-type semiconductor i.e. essentially constant capacitance in accumulation, $-V_G$, but decreasing to a lower value as the semiconductor becomes fully depleted at positive values of $V_G$.

We conclude, therefore, that since the maxima only occur on the first voltage sweep after polarity reversal and appear at approximately ±20 V, corresponding to the coercive field, $E_C \sim 60$ MV/m of P(VDF-TrFE), then they must arise from the reversal of polarisation in the ferroelectric insulator.

Interestingly, after reversing the polarisation during the positive voltage sweep, the device was expected to remain fully depleted until the subsequent negative voltage sweep had reached -20V when the polarisation reversed again. The rise in capacitance at low positive voltages on the return voltage sweep has been taken by some authors [6] as evidence that remanent polarisation is not stable in such devices. On the contrary, our measurements confirm that it is stable and is reversed only when the coercive field is exceeded. We have argued that after polarisation reversal in the depletion regime, $+V_G$, electrons must drift from the depleted semiconductor into trap states at the surface of the P(VDF-TrFE) [7].

Similar effects are observed in the output characteristics of the TFT shown in Fig. 3. Here the device was subjected to a series of programmed sweeps of the drain voltage, $V_D$, this time in sequences of two unipolar negative cycles in odd numbered programmes, P1, P3, etc. (see inset of Fig. 3) followed by two unipolar positive cycles during the even numbered programmes P2, P4, etc. In every cycle the coercive field of the ferroelectric was exceeded so that the remanent polarisation was reversed many
times. Starting with programme P1 prior to any poling of the ferroelectric it is seen that, with $V_G = 0$ V, the device was clearly OFF with no evidence for the enhancement of conductivity by remanent polarisation. However, sequential sweeps to ±40 V, caused $I_D$ to increase so that by the first cycle of programme P5, $I_D$ had reached a maximum of about $-10 \mu A$ at -15V and continued to increase thereafter, eventually saturating at about $-17 \mu A$ at -20 V. The current maxima, observed during the first negative cycle, occurred therefore at voltages corresponding to the coercive field and coincided with peaks in the gate current caused by polarisation reversal, $dP/dt$ in the ferroelectric. The maxima in $I_D$, however, were much greater than those for $I_G$ and must arise from the effect of polarisation on $I_D$ rather than from gate current flowing to the drain. This being the case, then after reversing the remanent polarisation, $I_D$ should have decreased to the low values corresponding to the initial OFF state observed in P1.

Two interesting points emerge from the data. Firstly, ferroelectric polarisation builds up over many cycles. Such a phenomenon has been reported by others in PVDF [8] and P(VDF-TrFE) [9] capacitors and has been shown to be related to microstructural changes in the polymer. Secondly, $I_D$ did not turn off after polarisation reversal but decreased to lower values and then followed a common curve both on the return voltage sweep and in the subsequent unipolar sweep. This is consistent with the C-V plots in Fig. 2 which show that after poling with depletion voltages, the device returns to accumulation, the condition required for the flow of source-drain current in the TFT, at $V_G \sim 0$ V. The transistor output characteristics confirm, therefore, that although polarisation reversal occurs at negative $V_D$, sufficient negative charges must also become trapped at the semiconductor/insulator interface to maintain a partially conducting hole channel. To neutralise the interface positive charges of the remanent polarisation as well as the shift in threshold voltage to $\sim 0$ V, requires that in excess of $\sim 10^{13}$ electrons/cm² must be trapped close to the interface [7]. While there is sufficient discrimination between the values of $I_D$ for the two polarisation states, the effectiveness of the memory would be greatly improved if the number of trapping sites could be reduced. An alternative approach may be to block the injection of electrons from the semiconductor by introducing an electron blocking layer at the interface.

5. Conclusions
The results discussed above provide clear evidence that, contrary to previous reports, the remanent polarisation in organic TFTs based on the ferroelectric polymer P(VDF-TrFE) is stable but when poled with depletion voltages electrons are injected from the semiconductor into trap states in or at the insulator/semiconductor interface. A possible approach to reducing this effect is suggested.

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