L_9 = 25 \text{ nm} \text{ InGaAs/InAlAs high-electron mobility transistors with both } f_t \text{ and } f_{\text{max}} \text{ in excess of 700 GHz}

Hyeon-Bhin Jo^1, Do-Young Yun^1, Ji-Min Baek^1, Jung-Hee Lee^1, Tae-Woo Kim^2*, Dae-Hyun Kim^1*, Takuya Tsutsumi^3, Hiroki Sugiyama^3, and Hideaki Matsuzaki^3

^1School of Electronics Engineering, Kyungpook National University, Daegu, Republic of Korea
^2School of Electrical Engineering, University of Ulsan, Ulsan, Republic of Korea
^3NTT Device Technology Laboratories, Kanagawa, Japan
E-mail: twkim78@ulsan.ac.kr; dae-hyun.kim@ee.knu.ac.kr

Received March 14, 2019; revised April 6, 2019; accepted April 15, 2019; published online May 1, 2019

In this paper, we report an L_9 = 25 nm InGaAs/InAlAs HEMT on InP substrate that delivers excellent high-frequency characteristics. The device exhibited a value of maximum transconductance (\(g_{m,\text{max}}\)) = 2.8 mS \mu m^{-1} at \(V_{DS} = 0.8\) V and on-resistance (\(R_{ON}\)) = 279 \Omega \mu m. At \(I_D = 0.56\) mA \mu m^{-1} and \(V_{DS} = 0.5\) V, the same device displayed an excellent combination of \(f_t = 703\) GHz and \(f_{\text{max}} = 820\) GHz. To the best of the authors’ knowledge, this is the first demonstration of a transistor with both \(f_t\) and \(f_{\text{max}}\) over 700 GHz on any material system. © 2019 The Japan Society of Applied Physics

The epitaxial layer structure used in this work was grown on a 3 inch semi-insulating InP substrate using metal-organic chemical-vapor-deposition. From top to bottom, the epitaxial layer structure consisted of a 30 nm thick heavily-doped multi-layer cap (In_{0.52}Ga_{0.47}As/In_{0.52}Al_{0.48}As), a 3 nm thick InP etch-stopper, a 9 nm thick In_{0.52}Al_{0.48}As barrier/spacer with Si doping, a 9 mm thick indium-rich InGaAs quantum-well channel, and a 200-nm In_{0.52}Al_{0.48}As buffer on the InP substrate. Details on the material growth were reported in Ref. 18. Key aspects are as follows: (i) a multi-layer cap to lower S/D ohmic contact resistance, and (ii) an In_{0.52}Ga_{0.47}As/In_{0.53}Ga_{0.47}As (1/5/3 nm) composite-channel to improve carrier transport properties. As reported previously, the Hall mobility (\(\mu_{\text{Hall}}\)) was measured to be 13 500 cm^2 V^{-1} s^{-1} with a two-dimensional electron gas density of approximately 3 \times 10^{12} cm^{-2} at 300 K.

The device fabrication was nearly the same as in previous report from our group. (17) This is a two-step recess process with a gate-to-channel distance, \(t_{\text{max}}\), of approximately 5 nm. Source-to-drain spacing (\(L_{\text{SD}}\)) was scaled down to 0.8 \mu m, and a non-alloyed metal stack of Ti/Mo/Ti/Pt/Al (5/10/10/200 nm) was used to form S/D ohmic contact. After a gate recess process, a SiO_2-assisted T-gate with a metal stack of Pt/Ti/Pt/Al was formed. Figure 1(a) shows a cross-sectional scanning-electron-microscope image prior to the gate metallization process. Figure 1(b) shows a cross-sectional transmission-electron-microscope (TEM) image after the gate process. The inset of Fig. 1 (b) is an enlarged TEM image of the gate foot region, indicating that the gate length (\(L_g\)) was as small as 25 nm.

Figure 2(a) shows the DC output characteristics of our representative InGaAs/InAlAs HEMTs with \(L_g = 25\) nm. The devices possessed a small value of \(R_{ON} = 279\) \Omega \mu m, which was due to the combination of the capping layer design and the optimized ohmic process. The contact resistance (\(R_C\)) of approximately 40 \Omega \mu m was measured from the transmission-line-method measurement. As shown in Fig. 2(b), the same device delivered the maximum transconductance (\(g_{m,\text{max}}\)) of 2.8 mS \mu m^{-1} at \(V_{DS} = 0.8\) V. More importantly, reasonable subthreshold characteristics, such as subthreshold-swing (S)
of 100 mV/decade and drain-induced-barrier-lowering (DIBL) of 120 mV V$^{-1}$, were demonstrated even in such a short-$L_g$ device. Figure 2(c) shows the measured $g_m$ of the same device as a function of drain current density ($I_D$) for various values of $V_{DS}$. Notice that the device possessed a fairly broad range of high $g_m$ over $I_D$, which would be highly beneficial to a diversity of applications.

The microwave characteristics of our representative InGaAs/InAlAs HEMTs were characterized from 1–50 GHz using an Agilent PNA system with off-wafer calibration. On-wafer open and short patterns were utilized to subtract pad-related capacitance and inductance components from measured scattering parameters (S-parameters). Figure 3(a) plots a measured short-circuit current-gain ($\left| h_{21} \right|$), a Mason’s unilateral gain ($U_g$), and a maximum stable gain (MSG) after de-embedding pad-related parasitic components for the device with $L_g = 25$ nm and $W_g = 2 \times 20$ $\mu$m at $V_{DS} = 0.5$ V and $V_{GS} = 0.15$ V near the peak $g_m$ bias condition. We
obtained a value of \( f_1 \) = 703 GHz by extrapolating the measured \( |h_{21}|^2 \) with a slope of \(-20 \text{ dB/decade}\) using a least-squares fit. As shown in Fig. 3(a), the measured \( U_g \) did exhibit a sharp peaky behavior which was also seen in other groups’ results. As a consequence, \( f_{\text{max}} \) could not be directly extracted from the measured \( U_g \). Instead, we constructed a small-signal model shown in Fig. 3(b), in order to estimate \( f_{\text{max}} \) accurately from a well-behaved \( U_g \) with a single-pole system. It is true that there exists inconsistency between the measured and the modeled \( U_g \) especially in the low-frequency regime. This is due to the fact that our small-signal model did not take the effect of impact-ionizations in the InGaAs QW channel into account. Nevertheless, this kind of the small-signal model has provided a reasonable estimate on \( f_{\text{max}} \) since the effect of the impact-ionizations diminishes as the measured frequency goes over 10 GHz. In this way, a value of \( f_{\text{max}} = 820 \text{ GHz} \) was obtained, which is identical to one from the modeled MSG/MAG. It is remarkable that the device delivered both \( f_T \) and \( f_{\text{max}} \) above 700 GHz at the same bias condition.

Table I shows small-signal model parameters, together with each delay time component as defined in Ref. 24. Here, transit time \( (\tau_T) \) is the carrier’s transit time under the gate from the edge of the source to the edge of the drain, while extrinsic delay \( (\tau_{\text{ext}}) \) is related to the parasitic charging delay due to extrinsic gate capacitances \( (C_{g_{\text{ext}}} \text{ and } C_{gd_{\text{ext}}}) \) and parasitic delay \( (\tau_{\text{par}}) \) to the RC time delay due to the series resistances \( (R_S \text{ and } R_D) \). Note that both extrinsic gate capacitances came mostly from the T-shaped gate structure. First of all, note that the excellent high-frequency response was due to a very high value of an intrinsic transconductance \( (g_{\text{m,int}}) \) of 4.425 mS\( \mu \text{m}^{-1} \) even in the device with \( L_g = 25 \text{ nm} \), as shown in Table I. However, it should be emphasized that the portion of \( \tau_T \) constitutes only by 20\%, indicating that a majority portion of the device’s intrinsic high-frequency characteristics was contaminated with unwanted parasitic components, such as series resistances and extrinsic gate capacitances. Unless decreasing a majority portion of both \( \tau_{\text{ext}} \) and \( \tau_{\text{par}} \), a further reduction of \( L_g \) would lead to a marginal improvement in \( f_T \). Figure 4 plots the extracted \( f_T \) as a function of \( I_D \) for the same device with various values of \( V_{DS} \). Consistent with the \( g_m \) against \( I_D \) in Fig. 2(c), the device yielded a wide range of \( f_T \) in excess of 600 GHz. At \( I_D \) of around 0.1 mA\( \mu \text{m}^{-1} \), which is a typical choice of the bias condition for most of LNA designs, our device already displays \( f_T \) over 400 GHz. Finally, Table II summarizes the historical evolution of HEMT technologies, together with key results \( (g_m, R_{\text{ON}}, f_T \text{ and } f_{\text{max}}) \). Since GaAs pseudomorphic-HEMTs (PHEMTs) exhibited the first demonstration of both \( f_T \) and \( f_{\text{max}} \) over 100 GHz\( \text{26} \) InGaAs/InAlAs HEMTs with \( x > 0.53 \) have provided a record combination of \( f_T \) and \( f_{\text{max}} \)\( 7,8,20,22-26,30 \) and our results represent the first demonstration of both \( f_T \) and \( f_{\text{max}} \) over 700 GHz.

In this paper, we demonstrated an \( L_g = 25 \text{ nm} \) InGaAs/InAlAs HEMT with an outstanding combination of DC and high-frequency characteristics. At its heart, the indium-rich InGaAs channel was utilized with superior Hall mobility of 13 500 cm\(^2\)V\(^{-1}\) s\(^{-1}\) at 300 K, and the gate length \( (L_g) \) was successfully scaled down to 25 nm while maintaining the electrostatic integrity of the device. In particular, the device with \( L_g = 25 \text{ nm} \) exhibited \( R_{\text{ON}} = 279 \Omega \mu \text{m} \), \( g_m = 2.44 \text{ mS} \mu \text{m}^{-1} \), \( f_T = 703 \text{ GHz} \) and \( f_{\text{max}} = 820 \text{ GHz} \) at \( V_{DS} = 0.5 \text{ V} \), respectively. To the best of our knowledge, this is the first demonstration of both \( f_T \) and \( f_{\text{max}} \) in excess of 700 GHz on any transistor on any material system.

| \( \text{Table I.} \) Small-signal model parameters of the \( L_g = 25 \text{ nm} \) InGaAs/InAlAs HEMT at \( V_{DS} = 0.5 \text{ V} \) and \( V_{GS} = 0.15 \text{ V} \), together with delay time components. |
|---|---|---|---|---|---|---|---|---|---|
| \( C_{g_{\text{ext}}} \text{[fF]} \) | \( g_{\text{m,int}} \text{[mS]} \) | \( R_{\text{ext}} \text{(}\Omega \mu \text{m}^{-1}\) | \( C_{gd_{\text{ext}}} \text{[fF]} \) | \( \tau_T \text{[fs]} \) | \( \tau_{\text{par}} \text{[fs]} \) | \( R_S \text{(}\Omega \mu \text{m}^{-1}\) | \( R_D \text{(}\Omega \mu \text{m}^{-1}\) | \( f_{\text{max}} \text{[GHz]} \) |
| 0.4106 | 0.1904 | 0.0848 | 0.0164 | 0.275 | 22.8 | 4.425 | 0.7353 |
| 0.15 | 138 | 138 | 46.7 | 112 | 66.2 | 707 | 703 |
Table II. Summary of the historical evolution of HEMT technologies together with key device parameters.

| References | Year reported | $L_g$ [mm] | Channel/Substrate | $R_{ON}$ [Ω$\mathrm{μm}$] ($V_{DS}$ [V]) | $g_{m,\max}$ [mS $\mu$m$^{-1}$] ($V_{DS}$ [V]) | $f_T$ [GHz] | $f_{max}$ [GHz] |
|------------|---------------|------------|-------------------|-------------------------------|--------------------------------|----------------|----------------|
| 26         | 1988          | 150        | In$_{0.75}$Ga$_{0.25}$As/InP | 1428 (0.8) | 0.65 (1.0) | 152 (1.0) | 230 (2.0) |
| 27         | 1992          | 50         | In$_{0.8}$Ga$_{0.2}$As/InP | 625 (0.2) | 1.69 (0.8) | 343 (0.8) | 250 (0.8) |
| 28         | 1994          | 100        | In$_{0.8}$Ga$_{0.2}$As/InP | N/A | 1.55 (1.0) | 305 (1.0) | 340 (1.0) |
| 20         | 2001          | 45         | In$_{0.75}$Ga$_{0.25}$As/InP | 1300 (0.4) | 1.0 (N/A) | 400 (1.0) | 469 (1.0) |
| 21         | 2008          | 30         | In$_{0.8}$Ga$_{0.2}$As/InP | 600 (0.5) | 1.83 (0.5) | 609 (0.5) | 609 (0.5) |
| 22         | 2008          | 50         | In$_{0.8}$Ga$_{0.2}$As/InP | 750 (0.4) | 1.62 (0.6) | 557 (0.6) | 718 (0.6) |
| 29, 30      | 2013          | 25         | In$_{0.8}$Ga$_{0.2}$As/InP | 270 (0.4) | 3.05 (1.0) | 610 (1.2) | 1500 (1.2) |
| 1           | 2013          | 60         | In$_{0.8}$Ga$_{0.2}$As/InP | 400 (0.3) | 2.11 (0.5) | 710 (0.5) | 478 (0.5) |
| 7, 8        | 2017          | 75         | In$_{0.75}$Ga$_{0.25}$As/InP (Asymmetric recess) | 500 (0.2) | 1.9 (1.0) | 250 (1.0) | 1300 (1.0) |
| This work   | 2019          | 25         | In$_{0.8}$Ga$_{0.2}$As/InP | 279 (0.4) | 2.8 (0.8) | 703 (0.5) | 820 (0.5) |

Acknowledgements This work was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (2017R1D1A3B03035746) and in part by SK-Hynix.

1) E.-Y. Chang, C.-I. Kuo, H.-T. Hsu, C.-Y. Chiang, and Y. Miyamoto, APEX 6, 034001 (2013).
2) Y. Shiratori, T. Hoshi, M. Ida, E. Higurashi, and H. Matsuzaki, IEEE Electron Device Lett. 39, 807 (2018).
3) R. Lai et al., 2007 IEEE Electron Device Meeting, 2007, p. 609.
4) S. B. Kang, D. W. Kim, M. Urteaga, and M. K. Seo, IEEE Int. Symp. on Radio-Frequency Int. Tech., 2017 8048279.
5) W. R. Deal, 2014 39th Int. Conf. on Infrared, Millimeter, and Terhertz waves (IRMMW-THz), 2014, p. 1.
6) K. M. K. H. Leong et al., IEEE Microwave Wirel. Compon. Lett. 25, 397 (2015).
7) T. Takahashi, Y. Kawano, K. Makiyama, S. Shibah, M. Sato, Y. Nakasha, and N. Hara, IEEE Trans. Electron Devices 64, 89 (2017).
8) T. Takahashi, Y. Kawano, K. Makiyama, S. Shibah, M. Sato, Y. Nakasha, and N. Hara, Appl. Phys. Express 10, 024102 (2017).
9) G. Dambrine, J.-P. Raskin, F. Danneville, D. Vanhoenacker Janvier, J.-P. Colinge, and A. Cappy, IEEE Trans. Electron Devices 46, 1733 (1999).
10) M. Malmkvist, E. Lefebvre, M. Borg, L. Desplanque, X. Wallart, G. Dambrine, S. Bollaert, and J. Grahn, IEEE Trans. Microwave Theory Tech. 56, 2685 (2008).
11) T. Takahashi, K. Makiyama, M. Sato, T. Hirose, and N. Hara, IEEE Int. Conf. on Indium Phosphide and Related Materials, 2008.
12) F. Fanneville, L. Poulain, Y. Tagro, S. Lepilliet, B. Dormieu, D. Gloria, P. Scheer, and G. Dambrine, Int. J. Numerical Model. 27, 736 (2014).
13) J. Schleeh, G. Aelesig, J. Halomen, A. Malmros, B. Nilsson, P. A. Nilsson, J. P. Starks, N. Wadefalk, H. Zirath, and J. Grahn, IEEE Electron Device Lett. 33, 664 (2012).
14) J. Schleeh, H. Rodilla, N. Wadefalk, P.-A. Nilsson, and J. Grahn, IEEE Trans. Electron Devices 60, 206 (2013).
15) E. Cha, G. Moschetti, N. Wadefalk, P.-A. Nilsson, S. Bevilacqua, A. Pourkabirian, P. Starksi, and J. Grahn, IEEE Trans. Microwave Theory Tech. 65, 5171 (2017).
16) Y. Yang, N. Wadefalk, J. W. Kooi, J. Schleeh, G. Moschetti, P.-A. Nilsson, A. Pourkabirian, E. Cha, S. Tuizi, and J. Grahn, 2017th IEEE MTT-S Int. Microwave Symp., 2017, p. 176.
17) H.-B. Jo, J.-M. Baek, D.-Y. Yun, S.-W. Son, J.-H. Lee, T.-W. Kim, D.-H. Kim, T. Tsutsumi, H. Sugiyama, and H. Matsuoka, IEEE Electron Device Lett. 39, 1640 (2018).
18) H. Sugiyama, H. Matsuoka, H. Yokoyama, and T. Enoki, 2010 22nd IEEE Int. Conf. on Indium Phosphide and Related Materials, 2010, p. 1.
19) A. Bracale, V. Ferlet-Cavrois, N. Fel, D. Pasquet, J. L. Gautier, J. L. Pelloie, and J. Du Port de Pontharras, Analog Integr. Circuits Signal Process. 25, 157 (2000).
20) K. Shinohara, Y. Yamashita, A. Endobi, K. Hikosaka, T. Matsu, T. Mimura, and S. Hiyamizu, IEEE Electron Device Lett. 22, 507 (2001).
21) D.-H. Kim and J. A. Del Alamo, IEEE Electron Device Lett. 29, 830 (2008).
22) D.-H. Kim and J. A. Del Alamo, 2008 IEEE Electron Device Meeting, 2008 4796796.
23) D.-H. Kim and J. A. Del Alamo, IEEE Electron Device Lett. 31, 806 (2010).
24) D.-H. Kim, B. Brar, and J. A. Del Alamo, 2011 IEEE Electron Devices Meeting, 2011, p. 13.6.1.
25) S. W. Moen, B. C. Jun, S. H. Jung, D. S. Park, J. K. Rhee, and S. D. Kim, IEEE Electron Device Lett. 31, 806 (2010).
26) D.-H. Kim, B. Brar, and J. A. Del Alamo, IEEE Electron Devices Meeting, 2011, p. 13.6.1.
27) L. D. Nguyen, P. J. Tasker, D. C. Radulescu, and L. F. Eastman, 1988 IEEE Electron Device Meeting, 1988, p. 176.
28) L. D. Nguyen, A. S. Brown, M. A. Thompson, and L. M. Jelloain, IEEE Trans. Electron Devices 39, 2007 (1992).
29) M. Wojtowicz, R. Lai, D. C. Streit, G. I. Ng, T. R. Block, K. L. Tan, P. H. Liu, A. K. Freudenthal, and R. M. Dia, IEEE Electron Device Lett. 15, 477 (1994).
30) X. Mei et al., IEEE Electron Device Lett. 36, 327 (2015).
31) K. M. K. H. Leong, X. Mei, W. H. Yoshida, A. Zamora, J. G. Padilla, B. S. Gorospe, K. Nguyen, and W. R. Deal, IEEE Trans. Terahertz Sci. Technol. 7, 466 (2017).