The Silicon Electron Multiplier Sensor

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Abstract

The Silicon Electron Multiplier (SiEM) is a novel sensor concept for minimum ionizing particle (MIP) detection which uses internal gain and fine pitch to achieve excellent temporal and spatial resolution. In contrast to sensors where the gain region is induced by doping (LGADs, APDs), amplification in the SiEM is achieved by applying an electric potential difference in a composite electrode structure embedded within the silicon bulk using MEMS fabrication techniques. Since no gain-layer deactivation is expected with radiation damage, such a structure is expected to withstand fluences of up to $10^{16} \text{n}_{eq}/\text{cm}^2$. Various geometries and biasing configurations are studied, within the boundaries imposed by the fabrication process being considered. The effective gain, the field in the sensor, the leakage current and breakdown conditions are studied for cell sizes in the range of $6 - 15 \mu m$. Simulations show that gains in excess of 10 can be achieved, and studies of the time structure of the induced signals from a charge cloud deposited in the middle of the sensor show that time resolutions similar to other sensors with internal gain can be expected. Plans for the manufacture of a proof-of-concept sensor and for its subsequent characterisation are discussed.

1. Introduction

Charged particle detection in the innermost region of high energy physics collider experiments combines the challenges of high fluence and high occupancy with the need for measurements with excellent spatial and time resolution. While demand for spatial resolutions below $10 \mu m$ is now commonplace, an ever increasing number of applications now require in addition a time resolution below 50 ps [1-5]. Existing solid state detector technologies suffer various limitations. While thin planar technology allows fluences of several times $10^{16} \text{cm}^{-2} \text{s}^{-1}$ to be reached, and can in principle reach time resolution as low as 30 ps [6], the limited signal amplitude makes this difficult to exploit. High fluences can also be reached with 3D technologies, and thanks to the decoupling between the drift direction and charge deposition direction, the Landau fluctuation contribution to the time resolution becomes sub-leading. Hence, time resolution below the 20-30 ps range have been measured [7,8]. Nonetheless, 3D technologies suffer high capacitance, fill factor reduction and it will be difficult to reach pitches lower than 50 $\mu m$ with present technologies. Another approach consists of amplifying the signal within the sensors, such as done in the LGADs [9] family. Gains of around 10 allow time resolutions in the range 20 – 30 ps to be reached. Recent variations of the LGAD design address the limitation in segmentation (iLGAD [10], trenched LGAD, AC-LGADs, ...). However LGADs suffer gain loss for fluences above $2 \times 10^{15} \text{n}_{eq}/\text{cm}^2$ [11] due to acceptor removal in the $p+$-doped gain layer.

We propose here a novel sensor design, the silicon electron multiplier (SiEM), which provides intrinsic gain together with a pixel pitch better than 10 $\mu m$, without reliance on shallow doping. The SiEM is expected to be more radiation hard than LGADs while providing similar time resolution.

2. Sensor description

2.1. Detection principle

As shown in Figure 1, the SiEM can be delineated into two regions. In a conversion and drift layer, primary charge carriers are created by the passage of minimum ionising particles (MIPs) through the sensor which then drift under the influence of an electric field towards an amplification and induction layer. In this layer, a region of high electric field is generated in the material to achieve primary charge multiplication by impact ionisation. The high electric field is achieved by applying electric potentials to a composite conductive structure buried in the bulk of the material. The drift of the secondary charges in this region induces a signal on the readout electrode. The exact geometry of the multiplication and induction regions depends on the bulk material as well as the fabrication process that can be achieved. For the design proposed in this paper, as illustrated in Figure 1, the bulk of the sensor consists of a reversed biased n-in-p silicon junction. The readout side is etched, leaving cylindrical Si-pillars which are terminated with the n+ implant and metal contact to the readout electrodes. A composite structure consisting of two conductive grid electrodes separated by a dielectric is deposited in the etched region. A difference of potential is applied to the two grid electrodes creating a high field region in the silicon pillars. The amplification is achieved in the pillars and charges drifting in this region induces a signal on the readout electrodes. The amplification electrodes can be biased either via bonding in a dedicated etched area, or through

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metallisation running along the pillar wall in one of the etched region.

Deep reactive ion etching process (DRIE) followed by successive deposition and patterning of dielectric and metal electrode is a possible approach to the making of this device. Constraints associated to this fabrication technique are considered in the following, in particular the interplay between the depth of the etch, the thickness of the dielectric layers that will be deposited on the wall and the distance needed between the pillar wall and the metal electrodes to ensure no connection is left between the top and bottom of the pillars. Alternative fabrication approaches may lift such limitations. Single buried electrode structures may also be envisaged and will be discussed in section 4.

2.2. Geometry description

The text in this section will refer to Figure 2 shows a cross-section of the SiEM design, identifying the most important dimensions. The thickness of the drift region (D) and the pitch (p) between pillars can be optimised depending on the application. Large thickness associated with small pitch readout could be used to reconstruct the direction of the impinging particle while a thin drift region is preferred for fast timing application, in order to minimise the time distribution centroid of the signal and thus improving on time resolution [6].

In the double buried electrodes geometry the electrode closest to the readout electrode is numbered 1 while the one closest to the drift region is numbered 2. The pillar width (w), the pillar height (h), and the pillar pitch (p), as well as the electrodes geometry, their widths (w₁, w₂) and the inter-electrode distance (d) are the principal drivers which define the electric field shape and its intensity. A few other geometrical parameters are shown in Figure 2 and are related to the expected process limitation. The distances g₁ and g₂ are the guard distances between the electrodes and the pillar wall while t designate the thickness of the dielectric between the bottom of the bulk and the electrode which is the first electrode to be deposited in the considered fabrication process.

In the following sections the behaviour of the device and the impact of these dimensions on the behaviour of the device is investigated using simulations.

3. Sensor behaviour

3.1. Setup

The TCAD device simulator Synopsis Sentaurus [12, 13] version S-2021.06 has been used to perform the simulation of the proposed structure. The 2D-mesh has been made by the Sentaurus Structure Editor with mesh cell sizes ranging from 200 to 10 nm. The PARDISO solver [14, 15] along with the Canali mobility model [16], Slotboom band gap model [17, 18, 19], and the vanOverstreaten - de Man impact ionization model [20] have been applied for quasi-static simulations. In transient simulations, the HeavyIon charge deposition is used.

Unless otherwise specified, the values for the geometrical dimensions defined in 2.2 are the following: the silicon bulk
parameters are defined by $D=50\,\mu m$, $p=10\,\mu m$, $h=6\,\mu m$ and $w=2\,\mu m$ while the electrode geometry is given by $d=1\,\mu m$ and $t_d=0.5\,\mu m$. A slice of the sensor corresponding to one single pillar, as shown on the left of Figure 2, is referred to a “cell”.

The geometry description in simulation reflects the expected constraints coming from the expected production process. In particular it is expected that when a layer of silicon oxide is deposited along the wall, it is also expected that to prevent metal remaining on the pillar walls, a guard of at least $0.5\,\mu m$ is introduced between the edge of the electrodes and the pillar wall. The minimal value of $g_2$ depends on $t_d$, while the minimal value of $g_1$ depends both on $d$ and $t_d$.

In the default configuration the electrode 1 is as large as possible, i.e. $w_1=5.7\,\mu m$ while the electrode 2 is retracted from its maximal size in order to have $w_2=w_1$ and thus provide a simple to interpret field geometry to start with. The default voltage configuration used for the electrode biasing is the following: while the readout electrode is at ground level, the potential of electrode 1, $V_1$, is set at $-5\,V$ and $V_2$, the potential of electrode 2 can vary to produce the electric field needed for amplification with $V_2=V_1-\Delta V$. The potential of the back-side electrode $V_{bias}$ is constantly $-30\,V$ below $V_2$ to ensure the depletion of the structure.

3.2. Electric field and leakage current

In Sentaurus TCAD quasi-stationary simulations, the voltages $V_1$, $V_2$ and $V_{bias}$ are ramp up simultaneously and linearly. During the voltage sweep, the leakage current at each step is evaluated, leading to a characteristic curve similar to the I-V of a planar sensor, even though the device is not bipolar. When the target voltages are reached, the electric field and other figures of merit discussed in 3.4 are evaluated. Figure 3 shows the I-V characteristic of a cell for a $\Delta V$ ramp up to a potential of $235\,V$. At low voltages, the I-V curve follows a reversed biased diode-like shape, until it reaches the saturation leakage current. At this point both the pillar and the drift region are depleted and the leakage current is low enough to allow primary charge particle detection ($\sim 0.1pA$ per cell). As $\Delta V$ increases, the field eventually gets large enough for the creation of secondary charges through impact ionisation. The leakage current increases as the thermal electrons get multiplied in the pillar. In this regime high field is concentrated at the top of the pillar as illustrated in Figure 4. Values of the electric field between 200 and $300\,kV/cm$ can be achieved in the silicon while keeping the field in the silicon oxide below $3\,MV/cm$.

For the default pillar width of $2\,\mu m$, above $\Delta V$ of $200\,V$ a sustained avalanche develops along the pillar wall, where the field is the highest. This avalanche, which leads to the breakdown of the device, is illustrated in Figure 4b.

The role played by $w$, the pillar width, was investigated and is illustrated in Figure 5. In these simulations $V_1$ is kept constant, while $\Delta V$ is varied for different pillar widths. The I-V curves display similar behaviour to the one of Figure 3, but a higher $\Delta V$ is required to reach charge multiplication for thicker pillars. This is due to the fact that for the same potential difference applied to the amplification electrodes, a lower electric field amplitude is achieved in the center of the pillar. Furthermore, the electric field just before breakdown voltage is reached is lower for thicker pillars since the breakdown is initiated at the pillar wall where the field is the highest. This reduces the expected maximum amplification capacity of thicker pillars. With the DRIE based process, widths of down to $w=0.6\,\mu m$ can most likely be achieved. A pillar size of $2\,\mu m$ is used in the rest of the

![Figure 4](image-url)  
Figure 4: Maximum electric field amplitude reached just before the sensor enters breakdown ($\Delta V=180\,V$) (a) and the current density just after breakdown ($\Delta V=195\,V$) (b). On figure (a) the black lines represent the electron velocity streamlines.
Max electric field [kV/cm] vs. $\Delta V$ for different pillar widths. Saturation of the electric field amplitude is due to polarisation effects that occurs when current flows in breakdown conditions.

Studies reported here. Note that, larger pillars are also of interest since, as will be discussed in 3.4, other parameters than the maximum electric field in the center of the pillar are relevant to the amplification mechanism.

3.3. Signal amplification

In the previous paragraph it was shown that fields above 200 kV/cm can be created in the pillar without breakdown of the device. Primary charge should thus be multiplied by impact ionisation in the pillar, providing internal gain to the sensor. Transient simulations are used to probe the multiplication mechanism. A charge cloud of 80 electron–hole pairs is deposited in the drift region center, and propagated in the device until all charges are collected at the electrodes. During the charge transport, the induced currents at the electrodes are recorded and further processed in order to extract the gain and the signal shape. The gain is defined as the ratio of integrated current on the readout electrode by the input charge. The integrated charge at the readout electrode is leakage current subtracted. In Figure 6a the currents from transient simulations using different $\Delta V$ are displayed. Although the signal induced at the readout electrode in Figure 6a is the one of interest for MIP detection, the signal induced on backside electrode is interesting to understand the signal formation and is show in Figure 6b.

At $\Delta V = 10$ V the device exhibits no gain. On the backside electrode the primary holes induce a signal from $t=0$ ns until all holes have reached the electrode. This signal mainly induced by the holes drifting towards the backside electrode looks very much like what would be observed on a pad sensor, as suggested by the distribution of the weighting potential of the backside electrode shown on Figure 7b. On the read-out electrode however, only the charge moving in the pillar induces signal. The signal only start when the electrons reach the buried electrodes. Charges moving in the drift region are shadowed by the amplification electrode as expected from the low weighting potential variation seen in Figure 7a.

At $\Delta V > 100$ V, when the electrons reach the top of the pillar, where the electric field is the highest, they generate secondary charges. Secondary holes drift back to the readout electrode inducing the second wave of signal starting at $\delta t$. The amplitude of this second wave depends on the amount of charge multiplication. The gain can be clearly seen from looking at the amplitude of the signal induced on the readout electrode, where the total secondary electron signal is added to the one from the primary electrons. In this configuration, the gain vary from $\sim 2$ for $\Delta V = 140$ V to slightly above 10 for $\Delta V = 180$ V. It can be
visualised on the Figure 6a by comparing the area under the curves at \( \Delta V = 140 \) V and \( \Delta V = 180 \) V with the area under the \( \Delta V = 10 \) V in which the field is too low for multiplication to occur.

Figure 7: Weighting potentials of the readout electrode (a) and backside electrode (b). The representation is rotated by 90° with respect to the other figures.

Figure 8: Electric field in pillar for different biasing configurations

\[ \Delta V=180 \text{V, } V_1=-5 \text{V} \]

\[ \Delta V=40 \text{V, } V_1=-100 \text{V} \]

3.4. Optimisation of the device

In the previous paragraphs, the configuration, both in terms of electrode geometry and in terms of biasing scheme is close to that of a typical GEM detector [21], with the high field region located in the interstice of the multiplication electrodes structure as illustrated in Figure 6a. In the following, configurations where the high field region goes further into the pillar are investigated. In particular, high field can be generated by a difference of potential between electrode 1 and the readout electrode. This configuration could be achieved with a single electrode and, as illustrated in Figure 8b the highest field is shifted towards the readout electrode. A well chosen balance between those two configurations would, on one hand, prevent generation of a localised high field which could initiate breakdown either in the silicon or in the silicon oxide and, on the other hand, increase the fraction of the pillar volume where charge multiplication can occur. This can be achieved by changing the electrode geometry or by modifying the biasing scheme, as discussed in the following paragraphs.

**Figure of merit.** In general, gains of above a factor 10 are targeted. It is nonetheless useful to define additional variables in order to understand the advantages or limitations of each configuration. The maximum electric field in the silicon, \( E_{\text{Si max}} \), and in the silicon oxide, \( E_{\text{SiO}_2 \text{ max}} \), indicate if a configuration is close to a breakdown conditions. High values of average electric field in the pillar, \( < \text{E} > \) reflect higher field achieved over a larger region of the pillar, especially when \( E_{\text{Si max}} \) is not large. Finally the barycenter position of the electric field along the pillar axis, \( < \text{Z} >_E \), give information on the position of the high field and how localised the field is. The closer it is to one electrode the more peaked it is, the closer to the pillar center, the more spread along the pillar it is. For this variable not to depend too much on the geometry, it is normalised by the height of the pillar, \( h \). Ideal configurations have high \( < \text{Z} >_E \) and as low \( E_{\text{Si max}} \) and \( E_{\text{SiO}_2 \text{ max}} \) as possible.

**Interplay between \( V_1 \) and \( \Delta V \).** The impact of the biasing scheme on the aforementioned figures of merit is studied in the following. \( \Delta V \) is scanned in steps of 5 V until breakdown and for different values of \( V_1 \). The resulting gain and figures of merit are reported in Figure 9. As expected it is possible to achieve gain above a factor 10 with different balances of \( V_1-\Delta V \), nonetheless the way amplification is achieved in the structure is very different. If \( \Delta V \) is large while \( V_1 \) is small, high electric field amplitudes are reached both in the silicon pillar, as shown in Figures 9a and in the dielectric, as shown in Figure 9b. Depending on the quality of the oxide this could lead to breakdown in the dielectric. When the gain is obtained by high difference of potential between the readout electrode and the electrode 1, ie. \( V_1 \) is large and \( \Delta V \) small, the field in the silicon reaches very high values close to the readout electrode and becomes the most likely cause of breakdown of the structure. In contrast, for \( V_1 \) values between 50 V and 75 V, for which gains of above a factor 10 can be achieved with settings of \( \Delta V \) above 110-60 V. These settings limit the field in the silicon below 250-300 kV/cm and in the silicon oxide below 3-1.7 MV/cm) which would provide a more robust operation point further away from breakdown. The field barycenter position along the pillar height in Figure 9c is, as expected, the closest to the readout electrode for large \( V_1 \), close to the amplification electrodes in the default biasing scheme, but more central with the “robust operation” scheme which indicates that the pillar is better filled with electric field. This is further supported by the fact that at this point the average electric field shown in Figure 9d is high.

**Electrode geometry.** A similar distribution of the regions of high electric field amplitude all along the pillar can be achieved by modifying the electrode geometry. When retracting the electrode 1, ie. \( W_1 < W_2 \), the lower part of the pillar receives a contribution from the difference of potential between the electrode
Figure 9: The maximum field in silicon and silicon oxide, \( E_{\text{Si max}} \) (a), and \( E_{\text{SiO}_2 \text{ max}} \) (b) evolution in the \((V_1, \Delta V)\) phase-space is presented, together with the evolution of the field barycenter, \( <Z>_E \) (c) and the average value of the field in the pillar, \( <E> \) (d). The gain is overlaid in each figure. Simulation were performed on about 60 points of the \((V_1, \Delta V)\) phase space and cubic 2D-interpolation is used to obtained a continuous representation.

I and the readout electrode. In Figure 10, the gain as function of \( \Delta V \) is shown for various geometries of the amplification electrodes, from the default geometry where \( w_1 = w_2 \) to geometries with ever smaller dimension of \( w_1 \ (< w_2) \) down to the complete removal of electrode 1. The more retracted electrode 1 is, the lowest \( \Delta V \) needs to be in order to achieve the same gain. This is due to the fact that the smaller \( w_1 \) is the more of the pillar is filled with high electric field, even though the maximum field is lower.

This approach can be combined with modification to the \((V_1, \Delta V)\) balance. The barycenter \( <Z>_E \) and gain variation as function of the biasing configuration are shown in Figure 11. As expected lower \( \Delta V \) allow to reach the high gain region, and overall larger gains can be achieved.

Inter-electrode spacing. In the default configuration, an inter-electrode spacing of \( d = 1 \mu m \) is considered. In the DRIE based process, after the patterning of the electrode 2 metal layer, silicon oxide is deposited before depositing electrode 1. During this phase, about 60-70% of the silicon oxide thickness \( d \) will also be deposited along the pillar wall. Thus, for larger values of \( d \), \( g_1 \) is also larger. The variation of the gain with increasing \( d \) is studied. In order not to mix effects, and although it was shown in the previous paragraph that \( w_1 < w_2 \) can be beneficial, we keep \( w_1 = w_2 \) while varying \( d \), i.e. \( w_1 \) is determined by \( g_1 \) and the electrode 2 is shortened to have the same length than electrode 1. The height of the pillar has been modified for each inter-electrode spacing in order to keep a constant distance, of 7 \( \mu m \), between the readout electrode and electrode 1. This was done to limit the dependency of the study on factors other than the spacing of the amplification electrodes. The gain evolution with \( d \) is shown as function of \( \Delta V \) in Figure 12. Since the inter-electrode distance is larger, a larger \( \Delta V \) is need to achieve the same gain. On the other hand the breakdown voltage is higher and the highest gain that can be achieved is larger with larger \( d \) as a bigger volume of the pillar is filled with high electric field.
amplitude. Gains of up to a factor 40 are observed for \(d=3 \mu m\) at \(\Delta V=320 \text{V}\). Together with optimised retraction of the electrode and/or different \(V_1/\Delta V\) balance, higher gains are likely to be achievable.

### 3.5. Optimisation for time resolution

While full simulations of the deposition, drift and amplification of primary charge carrier from MIPs, are needed to estimate the true time resolution of the sensor, the impact of some of the sensor parameters on the time structure of the signal can be assessed already. The time distribution of the signal induced on the readout electrode by the secondary electrons is driven by the time of arrival of the primary electrons at the amplification region. Following the arguments for sensor with internal gain in \([6]\) and assuming the time for the secondary electrons to drift through the pillar is small, the time resolution of SiEM will be dominated by the time it takes for electrons to drift through region \(\mathbb{D}\). Following \([6]\), the centroid time standard deviation will thus be given by \(\Delta t = \frac{1}{\omega} \frac{\Delta V}{V_{bias}}\) where \(\omega\) is a factor that depends on the charge deposition fluctuation and the sensor thickness (\(\omega \sim 0.3\) in this configuration) and \(T_e\) is the time it takes electrons to drift through \(\mathbb{D}\). For \(V_{bias} = V_2-30 \text{V}\), TCAD simulation gives \(T_e \sim 500 \text{ps}\) thus \(\Delta t \sim 40 \text{ps}\). But \(T_e\) can be further reduced by reducing region \(\mathbb{D}\) thickness or by operating at larger electric field in \(\mathbb{D}\) to increase the electron velocity. With gains of a factor 10 and above, a sensor thickness of as low as 25 \(\mu m\) should provide sufficient signal for detection. For 25 \(\mu m\) thickness and \(V_{bias} = V_2-30 \text{V}\), the field amplitude increase by a factor two, resulting in a 50% increase in the electron velocity. Such a modification would lead to \(T_e \sim 170 \text{ps}\) thus \(\Delta t \sim 15 \text{ps}\). The time resolution of the sensor will also be affected by the fact that the drift distance towards the induction region \(\mathbb{Q}\) will vary as a function of the lateral position of the primary charge carrier in \(\mathbb{Q}\). Indeed, as the primary charge carriers will drift along the electron velocity streamlines visible in Figure [3] their total drift distance will vary as a function of their initial transverse position. The in-homogeneity in the drift path depends on the ratio of the pitch to the pillar width. The lower it is, the smaller the in-homogeneity. The standard deviation of the drift path as function of the transverse position of the primary electrons is illustrated in Figure [3]. For the default 2 \(\mu m\) width and \(V_{bias} = V_2-30 \text{V}\), it varies from 0.3 \(\mu m\) to 1 \(\mu m\) for pitch varying from 6 \(\mu m\) to 15 \(\mu m\). The standard deviation of the drifting time for uniform transverse position distribution then varies from 5 ps to 23 ps. This contribution is sub-leading with respect to the contribu-

\(^1\)The thickness of region \(\mathbb{Q}\) is small with respect to the thickness of region \(\mathbb{D}\) and the electron velocity in \(\mathbb{Q}\) is expected to be close to saturation.
tion from the centroid time standard deviation which may range from 15 to 40 ps depending on the thickness of \( \mathcal{O} \) and the electric field amplitude in this region.

4. Discussion and future work

**Impact ionisation model.** In the results presented so far, the van Overstraeten - de Man impact ionisation model \[20\] has been used. Several models are available and the I-V characteristic curve shown in Figure 3 have been recalculated using the University of Bologna \[22\], and the ”New” University of Bologna \[23\] models, as well as the Okuto - Crowell \[24\] and the Lackner \[25\] models for impact ionisation. The results are compared in Figure 4. The I-V characteristics and all the curves show similar increase of the leakage current, corresponding to charge multiplication, over about a 50 V range before reaching breakdown conditions. The main difference between the various models is the values of \( \Delta V \) at which charge multiplication appears, with the van Overstraeten - de Man model predicting charge multiplication about 20 V earlier than the other models.

**Response to minimum ionising particles.** A complete estimation of the time resolution that can be achieved by such sensor requires on one hand to simulate the interaction of MIP with the sensor, and on the other hand to study the impact of the front-end electronics on the signal. The MIP simulation is performed with Garfield++ \[26\]. A full study of the impact of the sensor geometry and field configuration will be the topic of a future publication, but preliminary studies have been performed to understand the compatibility of the gain estimated in TCAD from a charge cloud deposited in the center of the bulk, as described in section 3, and the gain estimated from the amount of charge induced on the readout electrode by a MIP going through the detector with and without considering impact ionisation. In Figure 12 the result of the gain evaluated with Garfield++ is compared to the gain evaluated with the transient simulation of Sentaurus TCAD, using an identical setup, i.e. the deposit of a charge cloud in the center of region \( \mathcal{O} \). For the configuration which have been studied, \( d=3 \mu m \) and \( w_1=3 \mu m \), the gain estimation with the two methods agree to within five percent.

**Number of electrodes.** In order to provide further amplification and a better control of the field in the pillar, and providing the guard distance between the electrode and the pillar wall can be respected, geometries can be considered with more than two stacked amplification electrodes. Conversely, simpler geometries with a single electrode are also interesting, as they could be made with simpler fabrication flow and no more overlay constraint between electrode 1 and electrode 2. As shown in the discussion on electrode geometry, namely on Figure 10 a single electrode geometry can indeed achieve gain. In those configurations, the smaller the guard between the electrode and the pillar wall, and the smaller the width over height pillar ratio, the better. It prevents highly peaked electric field on the edge of the pillar just above the readout electrode.

**Alternative materials.** Any semi-conductor could be used for the bulk provided the band-gap is low enough to produce significant amount of charge carriers. Whereas depleted silicon offers more charges per MIP for low leakage current, silicon carbide and diamond are intrinsically more radiation resistant and while less electron holes pairs from ionisation by MIPs are expected, the amplification structure could compensate for it.

**Alternative processes.** The default process, based on DRIE, will be studied in the coming year. In parallel, an alternative process based on metal assisted chemical etching in liquid or gaseous phase \[27, 28\], followed by plating of the etching catalyst will be studied. It could achieve high aspect ratio pillars without significant guard distance between the pillar wall and the electrode. This process could be ideal for single electrode geometries. In the case of diamond bulk, graphitisation of the
diamond by laser could be used to produce the embedded electrode as is the case in 3D sensor applications [29].

Possible adverse effects. It is possible that DRIE etching generates low quality silicon surface terminations, leading to higher leakage currents. Annealing of the surface and slow growth of a thermal oxide should allow this effect to be minimised. Another concern is that filling the etched area with silicon oxide could produce adverse effect after irradiation due to ionization in the oxide. To some extent the build up of charge at the silicon interface should be prevented by the presence of the buried amplification electrodes which may collect the slow moving holes in the oxide before they reach the interface. This will be further studied in simulation. Indeed, if the dielectric is strictly needed in between electrode 1 and electrode 2 in the double electrode configuration, filling up the rest of the etched region is expected to ease the under bump metallisation deposition, but alternative techniques can be investigated.

The production of a demonstrator will be a key achievement to study the impact of those effects and assess the real performance of the device.

5. Conclusion

A new approach to achieve internal gain in solid state detector has been presented. The Silicon Electron Multiplier (SiEM) combines a conversion region where the passage of a MIP creates charge carriers, and an amplification and induction region where the charge multiplication occurs and the moving charges induce signal on the readout electrode. Simulations are used to assess and optimise the relevant geometry variables. The expected performance is estimated through simulations as well for a geometry that could be implemented in silicon with a process based on deep reactive ion etching.

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