Analysis of Asymmetrical Cascaded Multi-Cell Multilevel Inverter Employing Multicarrier Level Shifting PWM Technique on Different Loads

K. B. Bhaskar¹, T. S. Sivakumaran² and M. Devi²

¹Bharath University, Chennai – 600073, Tamil Nadu, India; jaibhaskar15@gmail.com
²Department of EEE, Arunai College of Engineering, Tiruvannamalai – 606603, Tamil Nadu, India; sivakumaranphd@gmail.com, devimogan@gmail.com

Abstract

Background: Multilevel inverters are very exciting alternative for intermediate and other high power drives. The Multicell group is widely growing owing to its advantages such as simplicity in circuit configuration with modularity and expandable. This paper proposes a new circuit configuration of 15 level cascaded H bridge Multicell Inverter which is the mixed form of flying capacitor and cascaded group. Methods: This work suggests a novel structure of new multilevel multicell inverter. The conventional structure uses two positive switch and two negative switch. Here the proposed inverter uses only one positive switch and only one negative switch. The circuit with one DC voltage along with one positive and negative switch forms a cell. Interconnection of more than one cells form multicell structure which is used to generate multilevel output. This multilevel inverter uses asymmetric voltage sources to produce multiple levels at the output. Here, Level Shifting Pulse Width Modulation (PWM) system is used to generate the switching signals to the inverter. Findings: The simulation of the proposed work shown with few number of semiconductor switches, is capable of achieving 15 levels at the output. Incorporating the Level Shifting PWM technique, the Total Harmonic Distortion (THD) has been reduced. Application: The proposed Multicell Multilevel inverter is used to drive the induction motor. Further controllers like PI, Fuzzy and Neuro can be added to reduce the THD and to develop the power quality.

Keywords: Asymmetric Voltage Sources, Level Shifting Pulse Width Modulation (LSPWM), Multicell, Multilevel Inverter, Total Harmonic Distortion (THD)

1. Introduction

Generally the converters are two types called as voltage source converter and current source converter. In Voltage Source Inverter (VSIs) have the independent control of output voltage i.e output voltage waveform. Similarly the current source inverter has an independent control of output current. i.e output current waveform. To maintain the quality of the power, the inverters (conversion of DC to AC by means of power electronic switches) are essential to produce the output voltage waveform to be followed or to be resembled as that of the sinusoidal waveform. This can be achieved only by using Multilevel inverters of multiple output levels resembling the sinusoidal shape.

In ¹ the Bypassed diode technique is used for conventional H-bridge multilevel inverter topology which cuts down the number of switches is introduced. In ² the H-bridge inverter topology with few switch count technique is introduced thereby reducing number of controllable switches introduced in conventional multilevel inverter. It dramatically reduces the circuit complexity, cost and also it reduces total harmonic distortion.

In ³ a new method is carried out for both symmetrical and asymmetrical inverter was suggested. In ⁴ the quantity of output levels is increased so as to improve the quality of a multilevel inverter. It uses an asymmetrically voltage sources with minimum switches than that of the
conventional one. In a 21-level Multi Level Inverter (MLI) with the planned converter topology using few switches by PWM technique is discussed. In it proposes an asymmetrical voltage source multilevel inverter for high power applications and also concentrated on reduction of THD.

In represents a new configuration of three-phase multilevel asymmetrical cascaded voltage source inverter. This structure consists of series-connected sub-multilevel inverters blocks. In a different configuration based on different DC bus voltage for a cascade H-Bridge multilevel inverter. The prime objective of this work is to compare two different symmetrical and asymmetrical arrangements. In a novel three phase multilevel inverter with a few number of switching devices. The Multilevel power converter has been introduced as a substitute for high power and medium voltage circumstances.

In this paper the proposed cascaded H bridge multicell multilevel inverter can produce output of 15 numbers of voltage levels with reduced number of switches where the cells are connected in cascaded manner which uses MC-LS-PWM technique to produce the switching signals for the inverter. Also the effectiveness of the inverter is tested with different loads.

## 2. Multicell Converters

One DC source and two semiconductor switches formed as one cell. In two semiconductor switches connected back to back with DC source. The circuit which is connected with many number of cells is called as Multicell converter. The inverter classification as shown in Figure 1.

**Figure 1.** Classification of inverters.

There are two types of cells in the circuit one is P-cell which produces positive levels and another one is N-cell which produces negative levels. The combinations of these cells are called as Multilevel Multicell inverters.

### 2.1 Cascaded Multilevel Inverter (CMI)

On the basis of the series connected three-level output voltage cells this multilevel inverter is constructed as shown in Figure 2.

![Four-Level Cascaded H Bridge Multicell Inverters](image)

**Figure 2.** Four-level Cascaded H bridge Multicell inverters.

This topology requires a complex multi secondary transformer as this circuit structure needs an isolated voltage source. The output voltage of multilevel converter is accordingly sum of output voltage of every single cell attaining a extreme level of $2n + 1$ output voltage levels, where $n$ is the number of cells in series per phase. Identifying a faulty cell incase of any internel fault is a special features of this configuration and faulty cell can be easily inaccessible and interchanged by a new cell through an external switch without switching off of the inverter. On the other hand during interchanging the faulty cell, the maximum output voltage in the faulty leg is minimized to:

$$V_{rN} = \sum_{l=2}^{n} V_{rl}$$  \hspace{1cm} (1)

$$V_i = V_i^N (1 - f/n)$$  \hspace{1cm} (2)

where $f$ is the number of faulty cells.

### 2.2 Flying Capacitors (FC)

In 1992, Meynard introduced Flying capacitor topology. By connecting two level cells, flying capacitor topology is developed, as shown in Figure 3, hence, output of the converter is given as,

$$l = q + 1$$  \hspace{1cm} (3)

where $q$ is the number of cells connected.
For a proper operation, the dc-link voltage on each cell must accomplish with:

\[ V_{ci} = I V_{dc} / q \]  \hspace{1cm} (4)

By applying redundancy states in a different way the above condition can be reached by the inverter itself. A complex input transformer is not required in FC, this is considered as an advantage for FC over CM, If internal fault occurs in one cell, the number of levels may get decrease but the maximum output voltage will be same.

\[ l_f = l - f \]  \hspace{1cm} (5)

An alternative topology proposed in this paper is mixed multicell converter which has two switches along with a DC source is connected in a cascaded fashion to obtain multilevel outputs\(^13\). This topology uses a three cells array to produce 15 voltage levels at the output of each leg, as seen in Figure 4.

Advantage of H- Bridge Inverter is, combinations are increased to attain the desired voltage level, That too it does not require more number of capacitors and semiconductors when compared with FC and CM topologies for the same number of output levels\(^17\).

### 3. Control Strategies

#### 3.1 Types of Control Strategies

Generally, need of modulation techniques is to produce the shape of the output waveform as close as to shape of the sinusoidal waveform in order to achieve high efficiency by eliminating the lower order harmonics and there by reducing the total harmonic distortion\(^15\). Researches on reduction of THD have given rise to many control techniques\(^16\).

The Figure 5 shows the classification of modulation techniques based on their switching frequency of the multilevel inverters. For high switching application the switches (power semiconductors) should have many number of commutations in one fundamental frequency which in turn makes the commutation complex for high switching frequency. Researches on these topics reveals that classic carrier-based sinusoidal PWM (SPWM) with
level shifting technique can reduce switching losses and
the commutation is made simple.

3.2.1 Multi Carrier Based Level Shifting Pwm
(MC-LS-PWM)

Multilevel Inverters requires multiple carriers to produce
multiple output voltage levels. In general, m level inverter
requires (m-1) carriers. Level shifting means frequency
of carrier signal is similar and also their peak to peak
amplitude is also same. The only difference is that there is
a level shift between two carrier waveforms.

There are three major kinds of LSPWMs depending
on how the carriers are disposed:
- Phase Disposition (PD), where all the carriers are in
  phase with each other Figure 6.
- Phase Opposition Disposition Square (POD), where
  all the carriers beyond the level of reference are in
  phase with each other, but in opposition with those
  of the Figure 7.
- Alternative Phase Opposition Disposition (APOD),
  where each carrier band is in opposition with each
  other Figure 8.

Figure 6. Phase Disposition (PD) Level Shifting PWM
technique.

Figure 7. Phase Opposition Disposition (POD)
Level Shifting PWM technique.

Figure 8. Alternate Phase Opposition Disposition
(APOD) Level Shifting PWM technique.

In this paper we have used the Phase Disposition (PD)
Level Shifting PWM technique. Here we use 14 carriers to
produce output of 15 voltage levels. In PD Level Shifting
PWM technique all the 14 carriers have the same peak to
peak amplitude as well as same frequency. They differ by
their level shifts. In PD all the carriers have same phase
disposition. They donot vary with phase. The carrier
waveform is shown in the Figure 6.

4. Proposed Multi Cell Multilevel
Inverter

A cascade multilevel inverter contains many number of
H-bridge (single-phase full bridge) inverter connected
in cascaded fashion. The proposed cascaded multi cell
multilevel inverter is a mixed version of cascaded and
flying capacitor multi cell inverter. Here the positive
switch and the negative switch were connected to the dc
source which we call as cell. These cells are connected in
cascaded fashion to produce the output levels. Then these
voltages are fed through normal single phase inverter
to produce the positive and negative voltage levels. The
circuit is shown in Figure 9.
In the proposed 15 level inverter we have three cells connected in cascaded fashion. The cell 1 has two switches \( S_1 \) and \( S_1' \). The switch \( S_1 \) is called positive switch used to produce positive voltage and the switch \( S_1' \) is called negative switch used to produce negative voltage.

Here we use asymmetric dc voltages whose voltage levels are given as \( V \) for cell 1, 2\( V \) for cell 2, 4\( V \) for cell 3 etc. Each H-bridge has separate dc source. Each DC source is accompanied with one single-phase full-bridge inverter. The output voltages of each cells are connected in series inorder to produce multilevel output at the inverters.

Their peak to peak voltage available is the addition of all the voltage sources. In our case the peak to peak voltage is 7\( V \). Here, we used voltage of about 40\( V \). So we produce the output voltage of about 280\( V \). The operation is similar to that of the cascaded H-Bridge inverter. Each cell produces output levels of +\( V \), -\( V \) and Zero volts. The comparison of components between conventional and proposed inverter is shown in Table 2.

### Table 1. Switching table for 15-level asymmetrical Cascaded multicell converter

| Output voltage levels | Auxiliary switches | Main switches |
|-----------------------|--------------------|--------------|
| 7\( V \)              | \( 1 \ 0 \ 0 \ 1 \ 1 \ 1 \ 0 \ 0 \ 0 \) |              |
| 6\( V \)              | \( 1 \ 0 \ 1 \ 1 \ 0 \ 0 \ 0 \ 1 \) |              |
| 5\( V \)              | \( 1 \ 0 \ 1 \ 0 \ 1 \ 0 \ 1 \ 0 \) |              |
| 4\( V \)              | \( 1 \ 0 \ 1 \ 0 \ 0 \ 0 \ 1 \ 1 \) |              |
| 3\( V \)              | \( 1 \ 0 \ 0 \ 1 \ 1 \ 1 \ 0 \ 0 \) |              |
| 2\( V \)              | \( 1 \ 0 \ 0 \ 1 \ 0 \ 1 \ 0 \ 1 \) |              |
|                       | \( 1 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \) |              |
|                       | \( 0 \ 1 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \) |              |
|                       | \( -1 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \) |              |
|                       | \( -2 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \) |              |
|                       | \( -3 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \) |              |
|                       | \( -4 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \) |              |
|                       | \( -5 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \) |              |
|                       | \( -6 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \) |              |
|                       | \( -7 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \) |              |

### Table 2. Comparison of components between conventional and proposed inverter

| Sl. No. | Components | Cascaded Inverter (for one phase) | Proposed Multicell Inverter (for one phase) |
|---------|------------|-----------------------------------|--------------------------------------------|
| 1       | DC sources | 7                                 | 3                                          |
| 2       | Switches   | 28                                | 10                                         |

A fifteen-level cascaded converter, for example, which has three DC sources and three full bridge converters. The switching pattern to produce 15 voltage levels is shown in the Table 1.

### 5. Simulation Results

**5.1 Asymmetrical Cascaded Multicell 15-Level Inverter with Normal PWM Method with RL Load**

#### 5.1.1 Simulation Model of Single Phase Asymmetrical 15-Level Cascaded Multicell Inverter
Analysis of Asymmetrical Cascaded Multi-Cell Multilevel Inverter Employing Multicarrier Level Shifting PWM Technique on Different Loads

5.1.2 Three Phase 15 Level Output Voltage Waveform Employing Pulse Generator
The output voltage waveform of 3-phase 15 level proposed cascaded H bridge multi cell inverter using pulse generator is shown in Figure 11. The cascaded 15-level inverter output signal is shown in the Figure 10. The output voltage of 280 volts is produced by using inputs of about 40V, 80V, 160V respectively.

5.1.3 FFT Analysis Using Pulse Generator

5.2 Simulation with Multi-Carrier Level Shifting PWM (MC-LS-PWM)
5.2.1 Waveform of Multi-Carrier Level Shifting Pwm (MC-LS-PWM) for 15 Levels
5.2.2 Three Phase Voltage Output Waveform using Multi-Carrier Level Shifting PWM (MC-LS-PWM) with RL Load

5.2.3 FFT Analysis Using Multi-Carrier Level Shifting PWM (MC-LS-PWM)

Figure 11. Three Phase 15 level Output Voltage Waveform employing Pulse Generator.

Figure 12. FFT analysis using pulse generator.

Figure 13. Waveform Of 15 levels Multi-Carrier Level Shifting PWM (MC-LS-PWM).
5.3 Three Phase 15 Level Cascaded Multilevel Inverter using Level Shifting Multicarrier PWM (MC-LS-PWM) with Induction Motor Load

5.3.1 Three Phase 15 Level output Voltage using Level Shifting Multicarrier PWM (MC-LS-PWM) with Induction Motor Load
5.3.2 Three Phase 15 Level Output Current using Level Shifting Multicarrier PWM (MC-LS-PWM) with Induction Motor Load

5.3.3 Speed Waveform

5.3.4 Torque Waveform

6. Conclusion

The 15 level cascaded multicell inverter was simulated in MATLAB simulink. The simulation results show that the multilevel is achieved with less number of switches with minimum THD. By implementing the LS PWM technique.
the THD has been further reduced. Since the number of switches has reduced the switching losses reduces and the controller is simple to design and there is no complex calculations in MC-LS-PWM.

6. References

1. Murugesan M, Ramani K, Thangavel S. A Hybrid Multilevel Inverter with Reduced Number of Switches for Induction Motor Drive. African Journal of Scientific Research. 2011; 4(1):1-15
2. Murugesan M, Sakthivel R, Muthukumaran E, Sivakumar R. Sinusoidal PWM Based Modified Cascaded Multilevel Inverter. International Journal of Computational Engineering Research (IJCER). 2012; 2(2):529-39.
3. Ahmed RA, Mekhilef S, Ping HW. New multilevel inverter topology with reduced number of Switches. In: Proceedings of the 14th International Middle East Power Systems Conference (MEPCON’10), Cairo University, Egypt; 2010 Dec. p. 565-70.
4. Lade HK, Gupta P, Shrivastava A. Modelling and Simulation of Three-phase Induction Motor Fed by an asymmetrically Configured Hybrid Multilevel Inverter. International Journal of Engineering and Computer Science. 2013 Dec; 2(12):3566-71.
5. Jithin JJ, Benuelsathish Raj A. A New Topology For A Single Phase 21 Level Multi Level Inverter Using Reduced Number of Switches. International Journal of Engineering Research and Technology (IJERT). 2013; 2(2):1-6.
6. Patel D, Chaudhari HN, Chandwani H, Damle A. Analysis and Simulation of Asymmetrical Type Multilevel Inverter using Optimization Angle Control Technique. International Journal of Advanced Electrical and Electronics Engineering, (IJAEEE). 2012; 1(3):81-86.
7. Belkamel H, Mekhilef S, Masoud A, Naeim MA. Novel three-phase asymmetrical cascaded multi level voltage source inverter. IET Power Electronics. 2013; 6(8):1696-706.
8. Mahalakshmi G, Jeyalakshmi P. Analysis of 31 level cascade inverter using MATLAB. International Journal of Advances in Engineering and Technology (IJASET). 2013 Nov; 6(5):2093.
9. Ramu J, Prakash SJV, SatyaSrinivasu K, Pattabhi Ram RND, Vishnu Prasad M, Hussain M. Comparison between Symmetrical and Asymmetrical Single Phase Seven Level Cascade H-Bridge Multilevel Inverter with PWM Topology. International Journal of Multidisciplinary Sciences and Engineering (IJMSE). 2012; 3(4):16-20.
10. Kumar N, Gupta S, Phulambrikar SP. A Novel Three-Phase Multilevel Inverter Using Less Number of Switches. International Journal of Engineering and Advanced Technology (IJEAT). 2013; 2(4):157-60.
11. Puviasari R, Dhanasekaran D. Interleaved Boost Converter Fed DC Machine with Zero Voltage Switching and PWM Technique. Indian Journal of Science and Technology. 2015 Feb; 8(4). Doi no: 10.17485/ijst/2015/v8i4/6043
12. Arul Kumar P, Subramaniam N. P. Chaotic Triangular Carrier Based Non-Deterministic SPWM Strategy for Voltage Source Inverter Drives. Indian Journal of Science and Technology. 2015 May; 8(9). Doi no: 10.17485/ijst/2015/v8i9/60075
13. E. Nanda Kumar, R. Dhanasekaran, R. Mani, “Optimal Location and Improvement of Voltage Stability by UPFC using Genetic Algorithm (GA)”,Indian Journal of Science and Technology,2015 June, 8(11), Doi no:10.17485/ijst/2015/v8i11/71778
14. Prabhakaran G, Kannan V. Design and Analysis of High Gain, Low Power and Low Voltage a-Si TFT based Operational Amplifier. Indian Journal of Science and Technology. 2015 July; 8(16). Doi no: 10.17485/ijst/2015/v8i16/59228
15. Soumya V, Raghavendra Shirodkar, Prathiba A, Kanchana Bhaaskaran VS. Design and Implementation of a Generic CORDIC Processor and its Application as a Waveform Generator. Indian Journal of Science and Technology. 2015 Aug; 8(18). Doi no:10.17485/ijst/2015/v8i18/76856
16. Aslam P, Memon M. Aslam Uqaili, Zubair A, Memon A, Asif Ali, Ahsan Zafar. Combined Novel Approach of DWT and Feedforward MLP-RBF Network for the Classification of Power Signal Waveform Distortion. Indian Journal of Science and Technology. 2014 Jan; 7(5). Doi no:10.17485/ijst/2014/v7i5/50158
17. Jose Rodriguez. Mixed Multicell Cascaded Multilevel Inverter. IEEE International Symposium on Industrial Electronics, 06/2007.