Electrical characteristics of multilayered HfO$_2$ – Al$_2$O$_3$ charge trapping stacks deposited by ALD

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Abstract. Electrical and charge trapping properties of atomic layer deposited HfO$_2$-Al$_2$O$_3$ multilayer stacks with two different Al$_2$O$_3$ sublayer thicknesses were investigated regarding their implementation in charge trapping non-volatile memories. The effect of post deposition annealing in oxygen at 600°C is also studied. The decreasing Al$_2$O$_3$ thickness increases the stack’s dielectric constant and the density of the initial positive oxide charge. The initial oxide charge increases after annealing to $\sim 6 \times 10^{12}$ cm$^{-2}$ and changes its sign to negative for the stacks with thicker Al$_2$O$_3$. The annealing enhances the dielectric constant of the stacks and reduces their thickness preserving the amorphous status. Nevertheless the annealing is not beneficial for the stacks with thicker Al$_2$O$_3$ as it considerably increases leakage currents. Conduction mechanisms in stacks were considered in terms of hopping conduction at low electric fields, and Fowler-Nordheim tunnelling, Schottky emission and Poole-Frenkel effect at higher ones. Maximum memory windows of about 12 and 16V were obtained for the as-grown structures with higher and lower Al$_2$O$_3$ content, respectively. In latter case additional improvement (the memory window increase up to 23V) is achieved by the annealing.

1. Introduction

The high-$k$ dielectrics based on transition metals oxides have attracted substantial interest for the past 20 years as a solution to scaling issues of advanced ultra-high density microelectronic devices [1,2]. The properties of the high-$k$ materials, the fabrication techniques and conditions have been tailored to obtain ultra-thin films allowing the replacement of thermal SiO$_2$ and SiON as a gate dielectrics in filed effect transistors (FET) and storage capacitors of dynamic random access memories. The intensive investigations revealed that these materials are prone to a high density of bulk traps. A lot of efforts have been paid to overcome this problem. The presence of bulk traps in the high-$k$ oxides, although considered as a drawback from advanced FET and storage capacitors point of view, can be regarded as quite interesting and the efficient trapping and retention of charge to be used in other micro(nano)electronic device applications.

Non-volatile memory devices and in particular flash memories became extremely widely used recently. The flash memory cell is built on floating gate FET. The dimensions of the floating gate cell have been shrunk continuously to ensure density growth pace of $\sim 2 \times$ every 2 years [3]. As the scaling of floating gate memory approaches the innate limitations of this technology several solutions based on
different memory effects have been proposed [4]. Among them charge-trapping memory (CTM) has received a lot of attention for its full compatibility with the current floating gate technological process. The charge in CTM is stored in spatially discrete traps in the bulk of the dielectric layer instead of the floating gate. The trap rich materials as high-\(k\) metal oxides are excellent charge trapping (CT) medium, moreover the future flash devices will require high perimittivity gate dialectics [4] as well.

\(\text{HfO}_2\) is one of the most heavily investigated high-\(k\) dielectrics. The maturity of \(\text{HfO}_2\) technological process ensured its introduction in Intel Penryn and Samsung A7 processors. Furthermore, some recently published results demonstrate that \(\text{HfO}_2\) can be implemented as CT layer in future flash memories [4,5]. It was also proposed that the CT characteristics of \(\text{HfO}_2\) could be substantially boosted by introduction of Al into its matrix, by creation of \(\text{HfO}_2/\text{Al}_2\text{O}_3\) laminated stacks [6,7]. The effect of Al into \(\text{HfO}_2\), however, is far from well understood and more studies clarifying the role of Al are needed. In this work we report electrical characteristics of multilayer \(\text{HfO}_2/\text{Al}_2\text{O}_3\) stacks prepared by atomic layer deposition and their dependence on the \(\text{Al}_2\text{O}_3\) content and oxygen annealing. The charge trapping in the structures was also addressed.

2. Experimental procedure

Multilayered \(\text{HfO}_2/\text{Al}_2\text{O}_3\) CT stacks were deposited on p-type (100) Si wafers with resistivity 6–8 Ωcm. Prior to the deposition the substrates were chemically cleaned. Two types of stacks with different \(\text{Al}_2\text{O}_3\) content (thickness of sublayers) were grown in Savannah-100 ALD system at a temperature of 135°C. Trimethylaluminum precursor was used for \(\text{Al}_2\text{O}_3\) deposition and tetrakis(dimethylamido)hafnium was used for \(\text{HfO}_2\). The oxidant was deionized \(\text{H}_2\text{O}\). First \(\text{Al}_2\text{O}_3\) films of 10 or 30 cycles were grown on Si followed by 30 cycles of \(\text{HfO}_2\) deposition. The \(\text{Al}_2\text{O}_3\)-\(\text{HfO}_2\) deposition sequence was repeated 10 times, resulting in multilayered stacks with identical thickness of \(\text{HfO}_2\) and variant \(\text{Al}_2\text{O}_3\) one, referred to as HA3/1 and HA1/1 in case of 10 and 30 \(\text{Al}_2\text{O}_3\) cycles respectively (figure 1). Part of the samples received Post Deposition Annealing (PDA) in dry \(\text{O}_2\) at 600°C for 20 min. The overall thickness, \(d\) was evaluated by Woolman M2000D ellipsometer in spectral range of 500–1000 nm. \(d\) of as-grown HA3/1 stacks is 49.2 nm and 65 nm for the HA1/1 ones. PDA reduces the thickness of the stacks. The reduction of \(d\) is stronger (7.7 %) for the thinner HA3/1 samples while for HA1/1 stacks the decrease is ~5.4%, resulting in \(d=45.4\) nm (HA3/1) and 61.5nm (HA1/1). The crystallinity of the structures and their surface morphology were examined by X-Ray Diffraction (XRD) and Atomic Force Microscopy (AFM), respectively. MOS capacitors with Al top (gate) and backside electrodes fabricated by sputtering were used for the electrical characterization. The square Al top electrodes (area of \(10^4\) cm\(^2\)) were patterned by photolithography. All electrical measurements were carried out in dark chamber employing Agilent 4980A LCR meter for capacitance-voltage (\(C-V\)) characteristics, and Keithley 236 SMU for the current-voltage (\(I-V\)) ones.

3. Results and discussion

![Figure 1. Schematic cross section of the investigated structures.](image-url)
Both types of as-grown stacks are amorphous as revealed by XRD analysis. The spectra of HA3/1 and HA1/1 layers are identical showing only features due to crystalline Si substrate. (XRD data is illustrated for HA3/1 structure in figure 2(a)). The PDA does not change the amorphous status of the films, despite the ellipsometrically obtained thickness reduction, i.e. PDA densifies stacks but their amorphous structure is preserved. The surface morphology of HA3/1 stacks is presented in figure 2(b) and c before and after PDA, respectively. Noticeable differences between the two types of as-grown CT structures were not observed (the average roughness, $R_a$ of HA3/1 layers is 0.433 nm and it is slightly lower 0.407 nm for HA1/1). PDA, however, slightly smoothens the surface ($R_a = 0.426$ and 0.334 nm for HA3/1 and HA1/1, respectively).

The initial $C$-$V$ characteristics of the as-grown and annealed structures measured in the frequency range $f = 1$kHz to 1MHz are presented in figure 3. The curves were obtained in a narrow applied voltage range in which the charge trapping is negligible. The hysteresis of the 1MHz $C$-$V$ curves is $\approx 0.05$V. As evidenced from figure 3 the capacitance in accumulation does not depend on $f$. The stack capacitance

![Figure 2. XRD spectra (a) and AFM data for HA3/1 samples before (b) and after annealing (c).](image)

![Figure 3. Initial $C$-$V$ curves obtained at different frequencies of HA3/1 (a) and HA1/1 (b) stacks before and after annealing, (designated by □ symbol).](image)
Leakage currents of stacked HA3/1 (a) and HA1/1 (b) capacitors before and after PDA. 1 and 2 denote the first and the second consecutive measurements in $+V$. Inset: $J$ in negative biases of the as-grown stacks vs. applied electric field.

was evaluated by Kar’s technique [8] and was further used to determine the effective dielectric constant $\varepsilon_{eff}$. $\varepsilon_{eff}$ of the as-grown HA3/1 and HA1/1 are 17.7 and 15.5, respectively. PDA increases the dielectric constant of the stacks. $\varepsilon_{eff}$ ~19 is obtained for the annealed HA3/1 samples and ~18 for the annealed HA1/1 ones. The increase of $\varepsilon_{eff}$ after PDA is in a good agreement with the observed reduction of $d$ and is most likely result of stacks’ densification. A significant difference in the initial oxide charge of the stacks $Q_{ox}$ (i.e. the charge present in the structures, prior to any carrier injection) as well as its response to the PDA is found upon variation of Al$_2$O$_3$ content. $Q_{ox}$ of both types of as-grown CT layers is positive. The structures with low amount of Al$_2$O$_3$, however, demonstrate much higher $Q_{ox}$ up to ~2.7×10$^{12}$ cm$^{-2}$ than capacitors with thicker Al$_2$O$_3$ sublayers (~6×10$^{11}$ cm$^{-2}$). PDA increases the density of $Q_{ox}$, up to ~6.4×10$^{12}$ for both stacks. But while for HA3/1 samples $Q_{ox}$ preserves its sign and $C$-$V$ curves after annealing are shifted towards more negative $V$, in case of HA1/1 the oxide charge is negative, $C$-$V$ curves are shifted to the positive $V$ (figure 3). The high positive $Q_{ox}$ is responsible for the observed dependence of the inversion capacitance of HA3/1 structures on $f$. The high positive $Q_{ox}$ inverts the Si surface, so the area outside the capacitor serves as a supply for minority carriers (electrons) into the inversion layer ensuring that their density follows at some extent the measurement signal frequency. As a result the inversion capacitance is higher than $C$ determined by the depletion layer. The effect is better pronounced in the annealed HA3/1 capacitors which have higher $Q_{ox}$, i.e the inversion is stronger, and $C$ in inversion approaches at 1 kHz the values of $C$ in accumulation (figure 3(a)). The shift of $C$-$V$ curves and the hysteresis for HA3/1 stacks at $f<1$ MHz can be attributed to the combined effect of the slow and fast interface states. PDA enhances these effects implying that the treatment generates additional defects near and at the very interface. Although hysteresis of $C$-$V$ curves is not observed for HA1/1, the decreased slope of the curves after annealing is a clear indication of increased density of fast interface states. The difference in $Q_{ox}$ between HA3/1 and HA1/1 layers is probably related to the negative fixed oxide charge in Al$_2$O$_3$ [10] and additional positive and negative volume charges in Al$_2$O$_3$ and HfO$_2$. All these charges depend strongly on $d$ if it is in the nanometer range as well as deposition conditions and thermal treatments and can lead to $Q_{ox}$ variations in a broad range.

Figure 4 shows the leakage current density, $J$ vs. applied gate voltage of the as-grown and annealed structures. Two consecutive curves were measured at $+V$ (indicated with 1 and 2). $J$-$V$ characteristics for both stack types under both voltage polarities are similar: an initial slow increase of $J$ with $V$ is followed by an abrupt one at high $V$ (an indication of conduction mechanism change). After the negative bias sweep, $J$ at the first measurement under $+V$ is higher (especially in the low voltage range) than $J$.
obtained at the second one. This behaviour is symptomatic for charge trapping phenomena. Under high negative $V$ positive charge build-up takes place (via hole injection form Si and/or electron detrapping in the insulator). After the bias polarity switch this positive charge enhances the electric field near the negative substrate, increasing $J$. Further, the positive charge is compensated and even surmounted by the trapped injected electrons resulting in lower $J$ during the second measurement. As seen, the trapping is better pronounced for the stacks with lower $\text{Al}_2\text{O}_3$ content, for which the voltage shift at $4\times10^{-8}\text{ A/cm}^2$ is $-8\text{ V}$, while for HA1/1 the maximum voltage shift is $-6\text{ V}$. The additional $J-V$ measurements (not shown here) at $+V$ does not result in significant extra voltage shift of the curves, suggesting that at the first $V$ sweep the positive charge is released and all electron traps are almost entirely filled. A comparison of the leakage currents of as-grown HA3/1 and HA1/1 capacitors as a function of the applied electric field $E$ (defined as $V/d$) is shown in the inset of figure 4(b). ($J$ only for negative $V$ is presented, as for these voltages the Si is in accumulation and the whole $E$ is applied across the dielectric.) Both structures exhibit almost identical $J$ at low fields, the steeper $J$ increase, however, occurs at higher $E$ in case of HA1/1 layers. So, thicker $\text{Al}_2\text{O}_3$ sublayers provide an improvement of the leakage currents in the high $E$ region because larger part of the stacks consists of high band gap dielectric ($\text{Al}_2\text{O}_3$). PDA seems to improve to some extent $J$ of HA3/1 structures mainly in the high $V$ region (the reduction is more distinct at positive biases). The charge trapping feature of $J-V$ curves at $+V$ is preserved and even enhanced after PDA. The annealing affects $J$ of HA1/1 layers in opposite manner: a substantial increase of $J$ is detected for both $V$ polarities. The lower current of annealed HA1/1 samples at $+V$ compared with $J$ at $-V$ is probably due to the high negative $Q_{ox}$, preventing the injection of electrons from Si. Because of the large $J$ of the annealed HA1/1 layers they will not be further considered.

We briefly discuss the conduction mechanisms of the stacks based on the $J-E$ characteristics obtained at room temperature and negative $V$. The following analysis, however, should be regarded only as tentative since generally the temperature dependence of $J$ is required for reliable identification of operating conduction mechanisms. Moreover, the charge trapping in the layers can severely affect $E$ and complicate the analysis. The insets of figure 5 exhibit log-log plots of $J-V$ curves before and after annealing, indicating nearly Ohmic behaviour (resulting from hopping of thermally excited electrons from one trap to another [9]) up to $V$ at which $J$ abruptly increases. The deviation of the log-$J$ vs. log-$V$ slope from 1.0 (sub-Ohmic behaviour) can be attributed to the charge trapping. Three commonly found conduction mechanisms in high-$k$ films: Fowler-Nordheim tunnelling (FN), Schottky emission (Sch) and Poole-Frenkel conduction (PF) [9] were invoked to explain the current in the stacks. As evidenced, the best fit of experimental $J-E$ curves is obtained by a combination Ohmic conduction and PF.

![Figure 5](image-url)

**Figure 5.** Experimental and simulated $J-E$ curves using a combination of Ohmic conduction and Fowler-Nordheim tunnelling, Poole-Frenkel effect and Schottky emission. For FN tunnelling curves corresponding to two barrier heights are presented. (a) HA3/1; (b) HA1/1. Insets: log-$J$ vs. log-$V$.
mechanism. The values of dynamic dielectric constant $K_r$ (square of refractive index, $n$) and compensation factor $r$ used for PF fit are: 3.7 and 1.5, and 3.9 and 2 for as-grown and annealed HA3/1 layers; and 3.4 and 1.2 for the HA1/1 stacks. These values agree very well with the elipsometrically measured $n$, ($n \approx 1.9-1.96$ and 1.94-2 for as-grown and annealed HA3/1 stacks, respectively; and 1.82-1.89 for as-grown HA1/1 ones). The combination of Ohmic mechanism and FN fails to describe the high field part of $J$; besides the obtained barrier height, $\phi_{b,FN}$ is higher than expected for Al/HfO$_2$ one. A decent interpretation can be made by Schottky emission with barrier height $\phi_{b,Sch} \sim 1$ eV and the same $K_r$ as in PF; the fit can be further improved but in all cases leads to values of $K_r$ not consistent with $n$. Taking into account also the symmetry of $J-V$ curves in respect to the zero bias we are inclined to attribute the conduction to bulk limited mechanisms – hopping conduction and PF effect.

The charge trapping in the stacks was evaluated by applying square voltage pulses with an amplitude, $V_{\text{pulse}}$ from ±5 to ±32V and duration of 1 s, and subsequent measurement of 1 MHz $C-V$ curves. The supplying of $+V_{\text{pulse}}$ is referred as Program operation while the supplying of $-V_{\text{pulse}}$ is noted as Erase one. The shift of the $C-V$ characteristics indicative of the trapping in layers is illustrated in figure 6a for as-grown HA3/1 stacks. After positive pulse $C-V$ curve shifts to more positive $V$ revealing negative charge trapping; the reverse pulse moves the curve backwards. The difference between the flatband voltage, $V_{fb}$ of the curves obtained after Program and Erase operation defines so called memory window, $\Delta V$. ($V_{fb}$ is the applied voltage at which the electric field at Si surface is zero, i.e. there is not Si band bending. $V_{fb}$ is being determined from the $C-V$ curves as the voltage at which $C$ equals the calculated value of the flatband capacitance [11]). Figure 6(b), (c) summarize the evolution of $V_{fb}$ after Program/Erase operations as well as the value of obtained memory windows as a function of $V_{\text{pulse}}$. Substantial $\Delta V$ is obtained for the HA3/1 stacks and PDA additionally extends $\Delta V$ form ~17V to ~23V at $|V_{\text{pulse}}|=32V$. 

**Figure 6.** $C-V$ curves of as-grown HA3/1 stacks after applying voltage pulses for 1s (a) and evolution of the flatband voltage with the amplitude of the voltage pulse for HA3/1 (b) and HA1/1 samples(c).
The comparison of figure 6(b) and (c) indicates that Al$_2$O$_3$ content in stacks affects the evolution of $V_{fb}$ due to the changes in the charge trapping processes and/or different nature of participating traps. For HA1/1 stacks up to $|V_{pulse}| \sim$ 15 V, $\Delta V$ is rather small, and the $V_{fb}-V_{pulse}$ dependence suggest accumulation/generation of positive charge. The capture of electrons occurs at higher $|V_{pulse}|$. The processes of charge trapping/detrapping, retention and endurance characteristics as well as comprehensive analysis of the conduction mechanism will be presented in more details in future work.

4. Conclusion
The dielectric properties of multilayered Al$_2$O$_3$-HfO$_2$ stacks can be effectively modified by the thickness of Al$_2$O$_3$ sublayers. The alumina content affects mainly the effective dielectric constant, the initial oxide charge and its response to the thermal treatments, while the impact on the leakage currents is weak. The conduction mechanisms of the stacks is not affected by the Al$_2$O$_3$ content and the current is governed by hopping conduction and Poole-Frenkel mechanism. The post deposition annealing densifies the stacks and increases the density of the existing defect states in case of stacks with thinner Al$_2$O$_3$ and introduces new type of defects in structures with higher Al$_2$O$_3$ content manifested via the change of the oxide charge sign. The higher trap density of stacks with smaller Al$_2$O$_3$ content ensures wider memory window, which is further widened by oxygen annealing. Different type of defects participate in the charge trapping and in the conduction in these stacks, since the leakage is improved after annealing. PDA is not suitable for stacks with higher Al$_2$O$_3$ content. The results suggest that alumina content should be carefully optimized to obtain maximum performance.

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