Gate defined zero- and one-dimensional confinement in bilayer graphene

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We report on the fabrication and measurement of nanoscale devices based on bilayer graphene sandwiched between hexagonal boron nitride bottom and top gate dielectrics. The top gates are patterned such that constrictions and islands can be electrostatically induced by applying appropriate voltages to the gates. The high quality of the devices becomes apparent from conductance quantization in the constrictions at low temperature. The islands exhibit clear Coulomb blockade and single-electron transport.

Confinement of charge carriers in graphene has been heavily investigated since graphene flakes on a substrate were first measured.1,2 Nanopatterning graphene into nanoribbons or small islands has been a widely used strategy for both zero- and one-dimensional confinement.3–7 Unfortunately, as a result of the etching process that is used for nanopatterning, the edges of the devices are very rough. This edge disorder, aggravated by substrate-induced disorder, leads to rather irregular device behaviour. For instance no quantized conductance was observed in etched constrictions, the transparency of barriers varied non-monotonously with gate voltage, no atom-like shell-filling has been observed in quantum dots and in many cases quantum dots fell apart into multiple islands.

Last year, suspended single layer graphene sheets nanorowed by current induced heating showed quantized steps in conductance of $2e^2/h$ as the Fermi wavelength was varied.8 Presumably these constrictions were not only narrow but also short, as observed in recent transmission electron microscope measurements 9, reducing the effects of edge disorder. However, the formation of these constrictions is hard to control, making it difficult to reproduce these results. Clean ribbon edges can be obtained reproducibly by unzipping carbon nanotubes, and a well-behaved quantum dot formed in such a nanoribbon was recently reported.10 Barriers were formed at metal Schottky contacts, but such barriers are not tunable, limiting follow-up work. Moreover, as the ribbons are not obtained lithographically but are dispersed from solution, they face many of the limitations of the carbon nanotube they originate from.

The ideal device would confine charge carriers in the bulk, far from (disordered) edges, have well controlled tunnel barriers, and enjoy all the design freedom offered by lithography. All these requirements can be satisfied using patterned electrostatic gates, provided a band gap is present. This calls for the use of bilayer graphene rather than monolayer graphene, as in bilayers a band gap can be induced by an electric field perpendicular to the layers.11,12 An additional requirement for clean confinement is to minimize substrate-induced disorder. Substrate disorder can be eliminated in suspended devices with suspended top gates, as shown in recent work by Allen et al.14 However, it would be highly desirable to realize devices of comparable quality on a substrate, as this would facilitate integration of complex devices. Currently the cleanest gate dielectric available for graphene devices is hexagonal boron nitride (hBN), and mobilities reported on such substrates approach those of suspended devices.15

Here we report 1-dimensional and 0-dimensional electrostatic confinement in bilayer graphene sandwiched in hBN dielectrics. The devices have split top gates and a global back gate, which we bias so that a gap is opened. The Fermi level is tuned inside the gap in the regions below the top gates so that they become insulating. Depending on the combination of top gates that is biased, we form 1-dimensional channels or 0-dimensional islands.

A schematic and AFM image of a device is shown in Fig. 1. We first deposit a 14 nm thick hBN flake by mechanical exfoliation on a silicon wafer coated with a silicon oxide ($\text{SiO}_2$) layer of thickness $t_{\text{SiO}_2} = 285$ nm. On top of the hBN we transfer a bilayer graphene flake ($\sim 22\mu$m long and $\sim 3\mu$m wide, its bilayer nature was
confirmed by Raman spectroscopy) using a dry transfer method following the protocol of Ref. 13 (at a temperature of 100 °C to remove any water absorbed on the surface of the graphene and hBN flakes). The sample was subsequently annealed in an oven at 400 and 450 °C (Ar 2400 sccm, H2 700 sccm) to remove residues induced by the transfer process. Cr(5 nm)/Au(95 nm) electrodes are fabricated using electron-beam lithography (EBL). We annealed the samples again (same flow rate as the first annealing step, T = 300, 350 and 440 °C) to remove fabrication residues. This did not give the desired sample quality. Hence we applied the recently developed mechanical cleaning technique 14 followed by dry transfer of a 50 nm thick hBN flake, which will act as top gate dielectric. In a two-step EBL process we deposited Cr/Au top gates. We defined several gate patterns between the contacts on this flake and report here on two ‘quantum dot’ top gate structures, one with a lithographic diameter of 320 nm (device A) and one of 250 nm (device B). The separation between the top gates that together define a barrier is less than 30 nm. For device B, TG1 and TG2 were unintentionally connected.

This specific graphene sample was cooled down multiple times. The maximum overall mobility measured at T=35 mK was ~ 36000 cm2/Vs (four-terminal configuration). The overall mobility measured during the last cool-down was much lower ( ~ 6000 cm2/Vs, two-terminal configuration). This degradation of electronic quality was caused by exposure to an electron beam during imaging in a scanning electron microscope. Nevertheless we believe that the graphene sandwiched in hBN remained of high quality.

We set the back gate to a large negative voltage and tune the top gate to a voltage that compensates for the doping induced by the back gate. For typical values \( V_{BG} = −50 \) V and \( V_{TG} = 9 \) V the displacement field \( D = 0.6 \) V/nm, which translates into a theoretically predicted band gap of ~ 50 meV. 11, 17, 18 As in earlier work, the transport gap is substantially smaller 12, 19 but still large enough to realize quantum confinement, as we will see.

In Fig. 2a, we show a top gate trace at a large negative back gate voltage, taken at low temperature. Clearly visible is a region of suppressed conductance, with a remarkably clean transition region on the hole side, and a somewhat less clean transition and lower conductance on the electron side. This behavior can be expected since the leads are p-doped by the backgate, and a pnp-junction is formed on the electron side. The pnp-junction decreases the transparency of the device as the charge carriers have to crosser tunnel through the induced band gap. On the hole side the conductance suppression with top gate voltage is very smooth and well behaved. This is in strong contrast to similar top gate sweeps for graphene nanoribbons, which exhibit very irregular pinch-off characteristics when the Fermi energy is swept into the transport gap. 4, 5, 7

Zooming in on the steep flank of the pinch-off curve, we observe several plateaus in conductance, with a value that is independent of \( V_{BG} \) (Fig. 2b). The traces have been corrected for filter resistance, current amplifier input resistance and for a background resistance \( R_B \) consisting of contact resistance, Maxwell spreading resistance and graphene lead resistance. The last two terms are dependent on back gate voltage. For each value of \( V_{BG} \) we subtracted a value of \( R_B \) comparable to the two-terminal resistance \( (R_{2T}) \) of the graphene flake with all top gates at ground (see inset fig. 2b), fine tuning \( R_B \) such that the conductance \( G \) at the upper plateau is \( 6e^2/h \). The other two plateaus consequently appear at \( G = 4e^2/h \) and \( G = 2e^2/h \). The same sequence of steps was observed for device A. (In device B, a less well developed feature can be seen just below \( G = 3e^2/h \), which does not appear in device A: its origin is unclear.) This behavior is consistent with transport through one-
In the field regime, the plateau at 6\( e^2/h \) magnetic field on the 1D channels (device B). In the low-field regime the background resistance was determined by aligning the plateaus near \( G=4e^2/h \) and in the high field regime by aligning the plateaus near \( G=8e^2/h \). (b) Extracted top gate voltages at the plateau centres versus magnetic field. By fitting a linear curve to the large field data we obtain \( C_{TG1k2} = \frac{1546}{49} \) A.U. \( \approx 1.04 \) F/m\(^2\). The value for \( C_{TG1k2} \) extracted from the \( \nu = 8 \) data is very similar.

The 2\( e^2/h \) steps in conductance are surprising given that there is both spin and valley degeneracy in bulk bilayer graphene, so 4\( e^2/h \) steps are expected. The same observation was recently made on suspended gate-defined bilayer constrictions [14] but it remains to be understood. Increasing the temperature to 440 mK did not change the general behavior. Lowering the bias to 50 \( \mu \)V (lock-in measurement with an AC excitation of 10 \( \mu \)V) did not change the appearance of the plateaus either. Both a larger bias and a higher temperature smoothened out universal conductance fluctuations, as can be expected.

We can estimate the width of the constriction from the position of the plateaus in top gate voltage with respect to the conductance minimum (Fig. 2). We see that as subbands become occupied, the width of the constriction increases from \( W_1 \approx 90 \) nm to \( W_3 \approx 120 \) nm for device A and from \( W_1 \approx 80 \) to \( W_3 \approx 160 \) nm for device B, which is characteristic of a smooth confining potential (with \( W_n \) the constriction width for the \( n \)-th subband). The lithographically defined separation between the respective top gates was less than 30 nm for both devices. This implies that the channel extends below the top gates, which can be expected given the modest band gap induced underneath.

In Fig. 3a we explore the influence of a perpendicular magnetic field on the 1D channels (device B). In the low-field regime, the plateau at 6\( e^2/h \) quickly disappears, but the plateaus at 4\( e^2/h \) and 2\( e^2/h \) remain visible. At large fields, plateaus in conductance develop at 4\( e^2/h \) (\( \nu = 4 \)) and 8\( e^2/h \) (\( \nu = 8 \)), typical values for the quantum Hall effect in bilayer graphene. [23] This transition from size confinement to magnetic confinement occurs when the cyclotron radius (\( r_c \)) is equal to or larger than \( W_n/2 \). [24] By extrapolating the positions of the plateaus for \( n = 2 \) and \( \nu = 4 \), we can determine a cross-over magnetic field of 0.9 \pm 0.2 \) T and estimate the size of the constriction based on \( r_c \) (Fig. 3b). This gives \( W_2 = 76 \pm 18 \) nm. The agreement with the estimate based on the plateau positions (\( \sim 120 \) nm) is better than a factor two.

When we induce two barriers by appropriate gate voltages, the device behaviour changes drastically. Fig. 4a shows a gate voltage scan of TG2 while TG1 and TG3 are also biased (device A). We see sharp conductance peaks separated by regions of strongly suppressed conductance, which is characteristic of Coulomb blockade. [23] As expected for Coulomb peaks, their position on one gate voltage axis varies smoothly (linearly) when another gate voltage is swept (Fig. 3a). We note that the resistance in Coulomb blockade is orders of magnitude larger than the sum of the two barrier resistances, which saturates around \( h/e^2 \) (Fig. 2), indicating each gate couples to
The Coulomb peak spacing exhibits a standard deviation of 1.4 mV, compared to an average peak spacing of 4 mV (device B). Irregular peak spacings can, in principle, originate from quantized level spacing contributions. However, no excited state features are visible in the Coulomb diamonds so it is not clear that level spacing is responsible for the peak spacing variation. Instead the reason may be the breakdown of the constant-interaction model, for instance due to disorder-induced variations in the island size or position as charge carriers are added one by one, or a second island capacitively coupled to the main island.

From the Coulomb diamonds and peak spacing we can obtain information on the dimensions and location of the island. For the dataset of Fig. 4b (device A), the addition energy $E_{\text{add}}$ is 0.35 ± 0.02 meV. When we neglect orbital energies, $E_{\text{add}} = 2E_c$, where $E_c$ is the charging energy. Using $E_c = \frac{e^2}{2\varepsilon C_d}$, we can calculate the total capacitance of the dot, $C_2 = 0.46 ± 0.03 \text{ fF}$. From the slope of the Coulomb diamond edges, we find that $C_2$ is dominated by the source and drain capacitances ($C_s = 0.10 ± 0.024 \text{ fF}$, $C_d = 0.30 ± 0.033 \text{ fF}$), which makes it difficult to estimate the island size from $E_{\text{add}}$ and $C_2$.

Instead, we compare the measured top gate capacitances with top gate capacitances simulated using a 3D Poisson equation solver (Ansoft Maxwell). From the average Coulomb peak spacing $\Delta V_{TG2}$ we extract a capacitance $C_{TG2} \sim 45 \text{ aF}$. $C_{TG3}$, $C_{TG1}$ and $C_{PG}$ are comparable. The calculated capacitance between a circular island of 320 nm in diameter and a metal plate with a 320 nm hole, 50 nm above the island, is 40 aF, about as large as each measured top gate capacitance by itself. We thus infer that the island is formed in the central region uncovered by the top gates and extends underneath all the gates. This is consistent with the quantum point contacts extending underneath the split gates as discussed above (see also [14]). Presumably lateral confinement is less tight in these devices than in GaAs split gate devices, due to the much smaller band gap.

Finally, we investigate whether the dot is weakly or strongly tunnel coupled to the leads by inspecting the line shape of the Coulomb peaks at low bias voltage. In Fig. 5b, we overlay on the data a fit by a hyperbolic cosine function and by a Lorentzian function. The former fits the data much better, indicating that the dot is in the weakly coupled regime, where temperature determines the linewidth rather than tunnel coupling to the reservoirs. Doing the same analysis for 50 peaks we find that they are consistently in the weakly coupled regime. We extract an electron temperature of 69 ± 14 mK.

Concluding, we show evidence for one-dimensional and zero-dimensional confinement in substrate supported bilayer graphene split gate devices. Transport through a single-barrier device shows signs of conductance quantization and in double-barrier devices clear Coulomb blockade is observed. Further development of this platform will enable us to study the rich physics of quantum confined charge carriers in bilayer graphene. Questions to be addressed include how electron-electron and electron-phonon interactions, and spin and valley lifetimes are modified by the confinement.

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