Design and vlsi implementation of a decimation filter for hearing aid applications

*1Purushothaman V, 2Rama devi R and 3Manjula S

1Department of Electronics and Communication Engineering, Sathyabama Institute of Science and Technology, Chennai, India.
2Department of Electronics and Instrumentation Engineering, Sathyabama Institute of Science and Technology, Chennai, India.
3Department of Electronics and Communication Engineering, Rajalakshmi Institute of Technology, Chennai, India.

*PurushothamanV@gmail.com

Abstract. Roughly 10% of the total common people experience some kind of hearing misfortune, yet just little level of this measurement utilize the portable amplifier. The shame related with wearing a portable amplifier, client disappointment with listening device execution, the expense and the battery life. Using computerized signal handling the advanced portable amplifier currently offers what the simple listening device can't offer. As of now low power VLSI design is more preferable in digital designs. More and more individuals around the globe experience the ill effects of hearing misfortunes. The expanding normal age and the developing populace are the principle explanations behind this. The pulverization channel utilized for portable amplifier is planned and executed both in MATLAB and Very High Speed Integrated Circuit Hardware Description Language. The obliteration channel is structured utilizing the circulated number-crunching multiplier in Very High Speed Integrated Circuit Hardware Description Language. Each computerized channel structure is reproduced utilizing Matlab and its total engineering is caught utilizing Simulink. The subsequent engineering is equipment productive and expends less force contrasted with traditional decoding channels. Compared with the decoding FIR-FIR engineering, the structured decoding channel design utilizing Comb-half band FIR-FIR adds to an equipment sparing and decreases the force scattering.

Keywords: IIR Filters, FIR Filters, Digital Hearing Aids, Sigma Delta Analog to Digital Convertor

1. Introduction

In modern technology the dependency on radio frequency (RF) correspondence handsets accentuates both higher joining, to satisfy customer need for minimal effort, low-power, little structure factor individual specialized gadgets, and the capacity to adjust to various correspondence guidelines. Higher combination can be acquired by utilizing recipient structures and circuit methods that dispose of the requirement for outside parts. Using a beneficiary design that can choose channel sifting on chip at modulation band takes into consideration the customization important to adjust to numerous correspondence norms.
Many applications require simple to-computerized change and hence become mainstream since it accomplishes expanded execution and adaptability by moving sign handling intricacy from simple to advanced hardware. Oversampling utilizes an inspecting rate that is a lot more noteworthy than the transmission capacity of the sign of intrigue. Advanced data handling systems is utilized to carry additional separating, decode and even do under sampling process. The scope of human hearing is commonly viewed as 20 Hz to 20 Kilo Hz, yet the ear is unquestionably responding to voice frequency between 1 Kilo Hz to 4 Kilo Hz. Thus it is added helpful to structure an amplifier application working inside the predefined recurrence go. Amplifiers are one of numerous cutting edge, versatile, computerized frameworks requiring power proficient structure so as to draw out battery life. Listening devices perform signal preparing capacities on sound signs. With the coming of numerous new sign preparing strategies, their necessity for higher computational capacity has squeezed power utilization.

Remote media transmission principles right now utilized all through the world have channel transfer speeds extending from 6.25 kilo Hz to 1.728 Mega Hz. A multiplexer is utilized to select one of the base band channel separating in the computerized area and carries Sigma-delta analog to digital convertor conversion with an extensive powerful range that can oblige select channels just as the ideal. It should likewise have the option to adjust to the different powerful range prerequisites and examining paces of the guidelines that are actualized. An extensive unique range sigma-delta modulator can be utilized to attain the necessities for various norms. Sigma-delta analog to digital converter is a minimal effort, minimal-transfer speed, minimal-power, increased-goal analog to digital convertor and utilized in many applications including information securing, correspondences, signal preparing and instrumentation. A portable amplifier application utilizes the increased sampling rate and comprises of a last yield goal of the analog to digital convertor. This work centers mostly around the plan and usage of the decimator.

2. Development of Digital Hearing system
Roughly 10% of the populace experiences some consultation misfortune, anyway just a little level of this class really utilizes an amplifier. There are a few components influencing market infiltration. Initially, there is the shame related with wearing a listening device. Second is client disappointment with the gadgets not living up to their desires, third is the expense related with the new advanced adaptations of listening devices.

The ongoing improvement of business listening devices with computerized signal handling abilities has permitted the improvement progressed signal preparing strategies to help the consultation weakened. The outcome for the wearer of the portable amplifier is more exact sound generation with least bending and clamor. Practically the entirety of the biggest amplifier makers have computerized listening device items available, and of the 6 million portable amplifiers sold in 2001, roughly 20% were advanced gadgets. So as to meet the little size and super low force prerequisites of listening devices, the current arrangements resort to unique reconfigurable ASIC gadgets for every amplifier structure. By upgrading to a monetarily accessible DSP approach which can be programmed according to custom needs, the listening device organizations can reduce altogether their price, subsequently a bigger segment of the populace with a reduced value, enhanced class computerized instrument.

In last few decades there has been increase in the quantity of advanced listening devices available in the market. Two well-known approaches of amplifiers that are accessible, behind the ear (BTE) and Completely in Canal (CIC). Regardless of their greater expense, they were generally welcomed by clinicians and customers.

Computerized listening devices today play out an assortment of cutting edge advanced sign handling calculations, for example, commotion decrease and input dropping. Consequently listening devices present difficulties for force and territory prerequisites (for manufacture chip) contrasted with other compact gadgets. It is essential to decide if advanced listening devices are enhanced for customers who faced hearing aid problem; it is additionally critical to concentrate on the prevalent preparing and highlights of these hearing aid gadgets. Computerized amplifiers cannot be depicted, as these devices are a different substance from simple listening devices. Computerized essentially
demonstrates that the simple waveform is changed over in to a line of number for handling, help sadly; there is nothing characteristically mysterious about this cycle. There for, computerized isn't prevalent on the grounds that its advanced, but since advanced sign preparing (DSP) permits fabricates to listening devices with upgrade handling and highlights.

2.1. Sigma-Delta analog to digital convertor
Analog to digital converters are classified based on relying the inspecting rate. The primary variant examples the simple contribution at the nyquist recurrence fn with the end goal that \( fs \geq 2B \), where \( fs \) is the testing recurrence and \( B \) is the transfer speed of the information signal. The second kind of ANALOG TO DIGITAL CONVERTORs tests the simple contribution at a lot increased operating frequencies greater than the nyquist recurrence and are brought over examining analog to digital converters, sigma-delta analog to digital converter. In sigma-delta analog to digital converter, the information data is examined at an increased testing recurrence.

\[ fs = KX \]

Figure 1 depicts the overall graph and a short depiction of a sigma delta Analog to digital converters. The modulator modulates the input signal signals which are close to higher frequency band components set by the increased sampled proportion and changes over the simple information data into a heartbeat thickness balanced computerized data having both the first info data and the undesirable out-of-band data. A de-multiplexer selects one of the modulator channels having band other than base band. For a given clock frequency the modulator coordinates with the decimator simultaneously. In Figure 1, the modulator indicated is of first request with a 1-piece quantize and creates a 1-piece yield. The yield of the decimator is appeared as N-bit computerized information, where N is the yield goal of the analog to digital convertor and is subject to the increased testing proportion. The request for the decimator relies upon the request for the modulator.

2.2. Modulator
This block is an integral part of a sigma-delta Analog to digital converters. The order at which the modulator is operating and the level of sampling the input decides the modulator performance in the architecture. Since the modulator utilizes the guideline of oversampling the requirement for antialiasing channel is mitigated and the simple info signal can straightforwardly be tested utilizing the oversampling clock.

2.3. Decimator
The cycle of carefully changing over the testing pace of a sign from a certain increased data rate \( fs \) to a decreased data rate \( fn \) is called decimation. Decoding in severe sense implies decrease by 10 percent yet in signal handling capability implies a decrease in inspecting speed by any factor. Fundamentally a decimator is an advanced low In channel, which additionally plays out the activity of test rate decrease. The sigma-delta modulator does activity of commotion molding and consequently the clamor is pushed to higher frequencies so the decoding stage following the modulator can sift through this commotion over the cutoff recurrence, \( fn \). The band restricted sign would then be able to be resampled by disposing of \( K − 1 \) examples out of each \( K \) tests, where \( K \) being the oversampling proportion. By averaging \( K \) tests out of the quantized sigma-delta yield, the decoding channel accomplishes a high yield goal and furthermore the recurrence of the yield information is at double the info signal data transmission which is the nyquist rate.

3. Design and implementation of structure of the proposed filter
The proposed filter structure comprises of demolition channel for incorporating with a current planned modulator along with a total sigma-delta Analog to digital converters. The utilization of multi-stage decoding channel which implies the single decoding channel is supplanted by fell channels. In this section, we are going to discuss the channel design utilized in the proposed architecture, which comprises of filter models, qualities and disadvantages. The initial phase in structuring a decoding
channel is to choose which sorts of channels will be utilized and where decoding will happen. This part investigates the issues engaged with picking channel design for a listening device application. The general intensity of a few models is thought about, bringing about the three-phase engineering that is picked to execute this channel.

Decoding channels must be simple and also proficient due to the necessity of sifting which is generally carried at an increased data rate. A sigma-delta analog to digital convertor creates a piece data bits at a increased data rate of 1.28 Mega Hz. This bits are given as input to the decoding channel and are reduced by means of data rate to 20 Kilo Hz. The architecture utilize a decimation factor of 16 to down sample the bit streams from the decoding channel from 1.28 Mega Hz to 80 kilo Hz. We have picked a In band of 4 Kilo Hz in light of the fact that the ear is delicate to all voice signal inside 4 Kilo Hz band. The channel has an In band wave of 0.001, that compares to the level reaction of the channel. Since the progress band is a little level of the examining rate, the channel will have numerous taps, and the zeros will be nearer to one another making the channel be more complex to simple architecture. The traditional demolition channel is actualized by this strategy, and the suggested framework mitigates issues introduced in traditional approach by utilizing a multiple stage approach having varied data rate. The force utilization is straightforwardly relative to the quantity of taps and the working recurrence. The specification of the proposed filter channel is given in Table 1.

Table 1. Filter specifications.

| Specification          | Value         |
|------------------------|---------------|
| Sampling frequency (Fs)| 1.48 Mega Hz  |
| Decimation factor (M)  | 8             |
| In band frequency      | 8 Kilo Hz     |
| In band ripple         | 0.002         |
| Center frequency       | 18 Kilo Hz    |
| Decimation filter stages(N) | 5          |

3.1. Implementation of the Comb Filter

![Comb Filter Diagram](image)

**Figure 1.** The multi stage filter architecture.
The contribution of the decoding channel is produced from a sigma-delta modulator running at 1.28 Mega Hz. Guard channel can be intended to introduce an indent at every one of the voice channels that will avoid interference between the base-bands. In addition, decoding channel does not requires multiplier and comprises of basic activities reasonable at increased frequencies. The response of the decoding channel is a low In channel with a more keen cutoff. Because of these reasons, look over channels are utilized for the main phase of decoding.

4. RESULTS AND DISCUSSIONS.

The proposed Decimation filter architecture is synthesized using Xilinx FPGA Device. Here 1.28 Mega Hz input signal is processed using ADC Sigma Delta modulator and obtained as Digital output. The input and output signal of ADC sigma delta modulator are shown in Figure 2 and Figure 3. The Digital input signal feeds to the FIR filter and the response of the low pass filter output is shown in Figure 4.

4.1. The ADC conversion from sigma-delta modulator

Figure 2 Input signal at 1.28Mega Hz

Figure 3 Output signal

Figure 4 The low pass filter output
4.2. The DAC conversion from sigma-delta modulator

The Digital output response of the low pass filter output is processed to the DAC sigma Delta modulator and produce the time domain output signal. The input, output signal and low pass filtered response are shown in Figure 5, 6 and 7.

Figure 5 Input signal at 4 Kilo Hz

Figure 6 Output signal
5. VHDL SIMULATION RESULTS.
The Comb-half-band FIR-FIR channel plan and decoding FIR-FIR channel structure. The decoding half band FIR-FIR channel configuration utilizes less equipment contrasted with the decoding FIR-FIR channel structure. The force utilization is less utilizing decoding half band FIR-FIR channel configuration contrasted with the decoding FIR-FIR channel is shown in Table 2.

| Cells used         | Slices | Slice Flip Flops | 4-LUT | logic | Shift registers |
|--------------------|--------|------------------|-------|-------|-----------------|
| Comb-FIR- FIR      | 698    | 1574             | 743   | 658   | 165             |
| Comb-half-band-FIR | 635    | 1274             | 703   | 583   | 125             |

Table 3 depicts that the suggested decoding channel utilizing Comb-half-band-FIR-FIR. It utilizes minimal equipment and adds to equipment sparing and a force sparing contrasted with the decoding FIR-FIR design.

| Decimation filter architectures | No of taps | Power consumption |
|---------------------------------|------------|-------------------|
| 5-stage Comb-FIR-FIR            | 20         | 62mW              |
| 5-stage Comb-half-band-FIR-FIR  | 10         | 52 mW             |

6. CONCLUSION
The decoding half-band FIR-FIR demolition channel is planned utilizing Matlab and checked for constant execution utilizing Simulink. The decoding channel is intended for 6-piece information input data bits. The channel comprises of 13 pieces, and the away from the pass band the signal got weak by a gain factor of ~ 66 dB. What's more, the appropriated number juggling multiplier is utilized for executing in Very High Speed Integrated Circuit Hardware Description Language. In particular, we look at the relative force utilization of two plans; the cell use for each structure is acquired utilizing the combination description. The suggested decoding channel design utilizes minimal equipment and adds to an equipment sparing contrasted with the decoding FIR-FIR engineering. Pulverization channels for
sound applications use FIR channels on account of the straightforwardness with which direct stage can be accomplished. Be that as it may, direct stage over the whole band isn't frequently needed.

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