Room temperature single electron transistor with two-dimensional array of Au–SiO₂ core–shell nanoparticles

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Abstract

The composite nanoparticles of gold core coated with SiO₂ shell have been fabricated into 2-dimensional array on a silicon surface by a simple self-assembly method combined with the technique of AFM (atomic force microscopy) nanolithography. The double-barrier-tunneling junction with AFM tip was also fabricated for the room-temperature single-electron tunneling study, by which the AFM tip was orientated on the surface of the SiO₂ coated gold composite nanoparticles. The 2D array shows well-pronounced Coulomb staircases with a period of 200 mV at room temperature, demonstrating single electron transistor behavior.

Keywords: AFM nanolithography; Single electron tunneling; Coulomb staircase; Self-assembly; 2-Dimensional array; Au–SiO₂ core–shell nanoparticle

1. Introduction

Single-electron tunneling (SET) at room temperature has attracted growing attention due to its potential applications in future nano-electric devices [1]. Recently, the use of metal or semiconductor clusters surrounded by a shell of organic ligands has been proposed as single electron transistors and has the potential to overcome the miniaturization and integration limits of conventional Si transistors [2,3], which can extend to a size range of a few nanometers or even less. The ability to fabricate these single-electron transistors into one-dimensional (1D), 2-dimensional (2D) or 3D structures has been regarded as a major challenge associated with incorporating nanoscale SET architectures into electronic devices for many years [4]. Considerable research efforts have been invested in developing different bottom-up and self-assembly procedures to obtain 1D, 2D or 3D arrangements of clusters with the accurate control of dimension, composition, and other properties [5].

Samuelson et al. [6] reported having manipulated gold nanoparticles using atomic force microscopy, and assembling GaAs nanowires into designed patterns using prefabricated and strictly size-selected gold nanoparticles. Photolithography [7], micro-contact printing [8] and electron beam lithography techniques are often used to form patterns of nanoparticles on a micrometer scale. Especially, Matsunoto et al. [9] first presented a new artificial pattern formation method based on the scanning tunneling microscope nano-oxidation process. Schmid et al. [10] fabricated the planned nano-patterns of [Au₅₅(Ph₂PC₆H₄SO₃Na)₁₂Clₖ] clusters on smooth silicon surfaces using a ‘bottom-up’ fabrication methodology based on the selective self-assembly strategy. Zhongfan Liu et al. [11] also fabricated the highly controlled-array of gold nanoparticles on a silicon surface by the self-assembly method combined with the AFM nanolithography technique. However, the single electron tunneling properties of these fabricated 2D cluster arrays were seldom studied.

Here, we fabricated 8 nm gold nanoparticles capped with an SiO₂ shell into a 2D array on a silicon surface by the AFM nanolithography method combined with the self-assembled technique. We also report the fabrication of a double-barrier-tunneling junction with AFM tip for room-temperature single-electron tunneling studies, by which the AFM tip was orientated on the surface of Au–SiO₂ core–shell composite nanoparticles. The sample showed a well-pronounced Coulomb staircase with a period of 200 mV at
room temperature, demonstrating single electron transistor (SET) behavior.

2. Experimental procedure

2.1. Materials

The following materials were obtained from Aldrich and used as received: HAuCl₄·3H₂O (>98%), sodium citrate, NaBH₄, tetraethoxysilane (TEOS), aminopropyltrimethoxysilane (APTMS), 3-chloropropyltrimethoxysilane (CPTS) and octadecyltrichlorosilane (OTS). The other reagents were of analytical grade. All H₂O was purified by a Narnstead Nanopure H₂O purification system (resistance = 18.1 MΩ cm).

2.2. Preparation of gold colloids

Gold colloids were prepared by the NaBH₄ reduction method. Typically, a gold sol was prepared by adding 1 mL 1%wt HAuCl₄ aqueous solution, 2 mL 38.8 mM sodium citrate aqueous solution and 1 mL 0.75% NaBH₄ aqueous solution into 90 mL water at room temperature. This gold colloid has an average diameter of about 8 nm and an absorption maximum of 525 nm.

2.3. AFM nanodegradation and assembly of Au–SiO₂ composite nanoparticles

The Si substrates cleaned by Piranha solution (H₂SO₄/H₂O₂=7:3, v/v), and sonicated by Milli-Q water, were immersed into 1 mM OTS/hexadecane solution to form a self-assembled OTS monolayer (SAM). The OTS coated-Si substrates were immersed in 1 mM CPTS/ethanol solution to fill the pinholes in OTS SAM. The AFM coated-Si substrates were immersed in 1 mM CPTS/ethanol solution to fill the pinholes in OTS SAM. The AFM coating process was performed with an atomic force microscope (Seiko II, SPA-300HV) operated at tapping mode. The current–voltage curves were obtained by positioning the AFM tip above one SiO₂ coated gold composite particle at room temperature.

3. Results and discussion

The TEM images of Au–SiO₂ composite nanoparticles (Fig. 1a) clearly show the typical core–shell structure of Au–SiO₂ composite nanoparticles. These gold nanoparticles, with a diameter of 8 nm, are completely and uniformly capped by an SiO₂ shell with a thickness of around 6 nm. Through the electron diffraction pattern of Au–SiO₂ particles shown in the inset of Fig. 1b, the polycrystalline structure of Au particles can be clearly identified by the weak rings and some scattered spots. The lattice phase of SiO₂ shell was not found, indicating that the SiO₂ shell was amorphous. These results show that the composite nanoparticles are composed of amorphous SiO₂ and crystallized gold nanoparticles.

Fig. 2a shows the AFM images of OTS SAM coated on a silicon surface. In OTS monolayer, some pinholes were observed, which must be removed because the Au–SiO₂ composite nanoparticles could be selectively deposited there, and to influence the nano-oxidization pattern. Some small silane molecules such as PTS (phenyltrichlorosilane) and CPTS were assumed to be helpful in filling these pinholes [11]. Fig. 2b shows an AFM image of an OTS-modified silicon surface that has been retreated by CPTS solution. These pinholes were removed as had been expected.

The template of 2D array was obtained by a programmed voltage pulse between the conductive AFM tip and OTS-coated silicon. The OTS monolayer was locally degraded from the AFM tip-confined surface regions. These regions became hydrophilic, while the un-confined regions continued to be hydrophobic. At the same time, an electrochemical reaction occurred in the nanoscale electrochemical cell composed of an AFM tip, the silicon substrate, and the water column adsorbed from the atmospheric water vapor. The AFM tip-confined silicon was locally oxidized into silicon oxide by anodic oxidation. These regions then became protruded due to the volume expansion from silicon (12.0 cm³/mol) to silica (19.4 cm³/mol). As a result, these regions became terminated with OH groups following sonication in CCl₄, ethanol and Milli-Q water. During this process, the pulse voltage, route and time can be controlled in the program for obtaining different patterns. Fig. 2c shows the pattern of oxidized 2D SiO₂ dots arrayed by this nano-degradation process. The height of the oxide dot is about 0.8 nm and the dot diameter obtained from the half-height width of the AFM image is around 80 nm. The section analytical result shows...
Fig. 1. (a) TEM and HRTEM images of Au–SiO₂ core–shell composite nanoparticles, the inset is an enlarged view of one Au–SiO₂ composite nanoparticle marked by the arrow, and (b) the electron diffraction pattern of composite nanoparticle.

Fig. 2. AFM images of (a) OTS-modified silicon. Places marked by circles indicate the ‘pinholes’; (b) silicon modified by OTS and CPTS; (c) the oxide dots array on an OTS-modified silicon surface by the AFM nano-degradation process; (d) 2D array of Au–SiO₂ CSNs on the AFM tip-confined assembling template. The section analytical data are also given for the images in (c) and (d).
that inter-dot spacing is uniform at around 160 nm, which indicates that the nano-degradation process is stable and controllable. The diameter of the oxide dot is an important factor in deciding the dimension of devices and is dependent on the humidity, applied voltage, and pulse time. By optimizing the experimental parameters, oxide dots that array with a dot diameter as small as 15 nm were also obtainable on hydrogen-passivated silicon [11].

Fig. 2d shows AFM images of the 2D array of Au–SiO₂ composite nanoparticles on the AFM tip-confined silicon template. These composite nanoparticles were fabricated into one regular array, guided by the original SiO₂ dots array, with each oxide dot attracting only one composite nanoparticle. The average height of the dot treated by composite nanoparticle solution is about 21 nm, as shown in the section analytical result, indicating that silica coated gold composite nanoparticles are adsorbed on these original dots array. The diameter of adsorbed composite nanoparticles is then estimated to be around 20 nm, which is consistent with the diameter of Au–SiO₂ composite nanoparticles shown in TEM images. The inter-particle spacing is also around 160 nm, similar to that before attracting composite nanoparticles. This result demonstrates that the area-selective Au–SiO₂ CSNs were successfully oriented on the silicon surface and formed the designed patterned-array by using the AFM tip-confined guiding template. It appears obvious that this approach offers great hope regarding extension of the line-widths of nanoelectrical devices down to 100 nm, and may open the door to a large variety of nanoelectronic applications.

The diameter of these dots (80 nm) attracting composite nanoparticles in AFM images appeared to be the same as that of the original oxidized dots. This could be attributed to the tip convolution effect in the AFM image, which leads to the adsorbed particles not being distinguishable from the original oxidized dots. At the same time, the tip-induced degradation might not be perfect and might not uniformly occur in the AFM nano-degradation process. This uncertainty may affect the deposition of composite nanoparticles.

In the process of investigating SET properties, the AFM tip must be directly orientated on the surface of SiO₂ coated gold composite nanoparticles to form a double tunneling junction (shown in the inset of Fig. 3a). The previous experimental difficulties of clearly resolving the very small clusters and of exact tip positioning made the data reproducibility very low, resulting in the problem of systematic and deductive SET investigations. In the present work, the investigated SET properties were very stable and had higher reproducibility because of the uniformity of these Au–SiO₂ composite nanoparticles. The current (I) and dI/dV vs bias-voltage (V) curves of the Au–SiO₂ array at room temperature are shown in Fig. 3. The sample shows a well-pronounced Coulomb staircase whose period is about 200 mV. The electrostatic charging energy of the sample calculated from the step width of the voltage is about 100 meV, remarkably higher than the thermal excitation energy at room temperature (~ 26 meV). From the staircase width value of 200 mV, the tunneling capacitance Cₓ can be estimated to be 8.0×10⁻¹⁹ F by Cₓ = eΔVₛₑ. Furthermore, the step width of the Coulomb staircase ΔVₛₑ for this sample was increased to about 150 mV after heat-treatment. The effect should originate from the increase of junction capacitance for the heat-treated sample. The junction capacitance can be described by the following [12]:

\[ C_j = \varepsilon_r \varepsilon_0 S d \]  

where Cj is the capacity of the tunnel contact, \( \varepsilon_r \) is the dielectric constant of the junction and S and d are the area and thickness of the junction, respectively. The contact area \( S_1 \), between the AFM tip and gold particle, is much smaller than the contact area \( S_2 \) between the gold particle and the substrate, resulting in \( C_1 \ll C_2 \). Therefore, the \( C_x \) can be predigested as \((C_2 + C_0)\) (\( C_0 \) is the self-capacitance of the gold core). The dielectric constant of the SiO₂ shell increases after heat-treatment. Thus, the junction capacitance \( C_2 \) will increase, leading to a decrease of \( \Delta V_{SD} \). Therefore, it has been demonstrated that planar room-temperature single-electron-transistor array can be successfully fabricated.

4. Conclusions

Gold nanoparticles coated with SiO₂ shell have been successfully fabricated into 2D array on a silicon surface by an AFM tip-confined guiding template technique to form 2D single electron transistor devices. The assembled array of Au–SiO₂ composite nanoparticles exhibits a well-pronounced Coulomb staircase whose period is 200 mV at room temperature, which is a promising candidate for future room-temperature single electron transistors.
Although further improvements are still needed to remove some existing defects (e.g. the tip-induced degradation may not be perfect and uniform), the above method is effective in self-assembling SET devices with the line-width reduced to 100 nm.

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