A study and comparison of COordinate Rotation DDigital Computer (CORDIC) architectures

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Abstract—Most of the digital signal processing applications performs operations like multiplication, addition, square-root calculation, solving linear equations etc. The physical implementation of these operations consumes a lot of hardware and, software implementation consumes large memory. Even if they are implemented in hardware, they do not provide high speed, and due to this reason, even today the software implementation dominates hardware. For realizing operations from basic to very complex ones with less hardware, a Co-ordinate Rotation Digital Computer (CORDIC) proves beneficial. It is capable of performing mathematical operations right from addition to highly complex functions with the help of arithmetic unit and shifters only. This paper gives a brief overview of various existing CORDIC architectures, their working principle, application domain and a comparison of these architectures. Different designs are available as per the target, i.e. high accuracy and precision, low area, low latency, hardware efficient, low power, reconfigurability, etc. that can be used as per the application in which the architecture needs to be employed.

Keywords—Givens rotation matrix, scale-factor, CORDIC gain, micro-rotations, rotation and vectoring mode, Repetitive Iteration

I. INTRODUCTION

For years long the digital signal processing applications have been dominated by microprocessors. Though these processors are low cost and flexible enough, they are often not that fast for certain DSP tasks. The reconfigurable logic in computers permits higher speed at the same cost as that of the traditional software approach. Unfortunately algorithms for these microprocessors based systems are not totally compatible with the hardware. Hardware efficient solutions exist but software systems are still dominating the market and have kept these solutions out of the spotlight. In the hardware efficient algorithms, there exists a class of iterative solutions that use only shifts and adds to perform trigonometric and other transcendental functions. This class is called as CORDIC which is an acronym for Coordinate Rotation Digital Computer as stated in \cite{1}, \cite{2} which is used for DSP applications \cite{3}, \cite{4} for fast VLSI implementation \cite{5} and for FPGA designs \cite{6}, \cite{7}.

We know that, there is a need to maintain a trade-off between speed, power, area and accuracy, as benefits in all the design metrics cannot be achieved at the same time. This leads to the demand of approximate designs for error tolerant applications. High power and energy savings can be achieved by introducing tolerable errors in the architecture, which in turn helps to improve the design and quality metrics. We know that DCT is one of the most compute intensive blocks in DSP applications, which demands for an architecture that is capable of reducing its complexity. One such architecture is given in \cite{8} that proposes a low power CORDIC architecture and a low power approximate DCT architecture using the same. Such approximate architectures can be effectively used for DSP applications involving human intervention by efficiently exploiting persistence of vision. Some CORDIC based DCT architectures are also discussed in \cite{9}, \cite{10}, \cite{11}, \cite{12}, \cite{13}, \cite{14}, \cite{15} and \cite{16}. A reconfigurable low power DCT architecture based on data priority is proposed by Lee et al. in \cite{17}.

The remaining paper is organized as follows: Section II explores CORDIC, gives its working principle and different modes, trajectories for which it can work. It also mentions a broad overview of the work covered in these papers (shown in Figure 3). The different existing CORDIC architectures are mentioned in Section III. Results and discussions are made in Section IV and the paper is concluded in Section V.

II. EXPLORING CORDIC AND ITS APPLICATION DOMAIN

As mentioned in section I COrdinate Rotation DDigital Computer i.e. CORDIC is nothing but an easy way of performing simple to very complex mathematical computations. It can very efficiently perform several computing tasks like, calculation of trigonometric functions, real and complex multiplications, division, multiplication, square-roots, cube-roots, finding solutions of linear equations, singular value decomposition, etc. The novelty of CORDIC is that it obtains the results using minimum hardware and using only adders/subtracters, which consume very little area on a chip. So it would not be wrong to state that, it is a less complex and hardware efficient way of performing mathematical computing, applications in image, video processing, robotics, communication systems, etc.

A. The CORDIC Algorithm

The CORDIC algorithm was first introduced in 1959 by Jack E. Volder. It was developed at the aero-electronics department of Convair to replace the analog resolver in the B-58 bomber’s navigation computer. It has been used in applications like 8087 co-processor, pocket calculators, radar signal processors, robotics etc. CORDIC is nothing but a computer which contains a special serial arithmetic unit consisting of shift and addition units, and special interconnections. By using a prescribed sequence of conditional add/subtract operations, the CORDIC arithmetic unit can be controlled and thus used to solve any function.

The main idea behind the working of CORDIC lies in the fact that, the co-ordinates of any vector are nothing but trigonometric returns of the angle it makes with the positive X-axis (cosine and sine values). So, whenever any vector is rotated in space, along with the new co-ordinates, it provides the angle parameters. This concept is the backbone of CORDIC algorithm. The input and output vectors are related with each other by a rotation matrix called as Givens rotation. It helps to find the co-ordinates of the rotated vector.

1) Givens Rotation: It relates the input and output vectors and the relation between the initial and final vector is represented by Givens rotation \[ \begin{bmatrix} \cos \theta & -\sin \theta \\ \sin \theta & \cos \theta \end{bmatrix} \] a rotation in the plane spanned by two coordinates axes. Its general form is,

\[
\begin{bmatrix}
1 & \cdots & 0 & \cdots & 0 & \cdots & 0 \\
\vdots & \ddots & \vdots & \ddots & \vdots & \ddots & \vdots \\
0 & \cdots & c & \cdots & -s & \cdots & 0 \\
\vdots & \ddots & \vdots & \ddots & \vdots & \ddots & \vdots \\
0 & \cdots & s & \cdots & c & \cdots & 0 \\
\vdots & \ddots & \vdots & \ddots & \vdots & \ddots & \vdots \\
0 & \cdots & 0 & \cdots & 0 & \cdots & 1
\end{bmatrix}
\]

The following matrix works in case of 2D,

\[
\begin{bmatrix}
\cos \theta & -\sin \theta \\
\sin \theta & \cos \theta
\end{bmatrix}
\]

When we rotate a vector, it does not move linearly, instead it follows a circular path. Finding out the co-ordinates, when a linear path is followed involves the direct use of Givens rotation and some simple calculations. But for the real rotations involved here, finding the values is somewhat tricky, which is clear from Figure 1. So, to easily find out the end points of the obtained output vector, instead of considering the real rotation, pseudo-rotations are used. These rotations use the Pythagoras theorem to return the co-ordinate values and by further using them, the actual ones are found out.

This helps to reduce the architecture complexity but at the same time introduces an extra term/constant to compensate for the error occurring due to the pseudo-rotation. This term is often referred to as scaling factor.

2) Micro-rotations: For achieving an angular shift, CORDIC breaks it into a number of small angles as shown in Figure 2 and instead of rotating the initial vector by one large angle, it is rotated number of times by the broken angles. This can be called as iterative decomposition of angle of rotation. By doing this, there is ease in rotation and reduction in complexity of the algorithm. The steps wherein every time the vector is rotated are termed as iterations which provide easy understanding of the algorithm. But increasing the iterations above an extent will add to its complexity and hardware cost.

Number of iterations can be limited by, either fixing it or comparison at each stage with the residual angle. These are generally referred as iterations and denoted by \( i \). In CORDIC algorithm, to simplify the micro-rotations, instead of using the direct inverse tangent values, divide by increasing powers of 2 is done. It is also necessary to decide which way the vector is to be rotated i.e. in clockwise or in anti-clockwise direction. This will be known using the value of \( \sigma \), which depends upon the sign of residual angle.

3) The CORDIC Gain: Whenever vector is normally rotated, the co-ordinates it gives are the accurate ones. But when a real rotation is replaced by a pseudo-rotation it gives erroneous co-ordinate values. This is because, whenever a vector is rotated, as that we do here; the length of final vector is more than the actual required one which we would have obtained by real-rotation. The factor by which the original accurate length differs from the obtained one is termed as scaling factor \(( k)\), and is given by the following equation,

\[
k_i = \frac{1}{\sqrt{1 + 2^{-2i}}}
\]

It provides the scaling factor value for a particular value of \( i \). \( k \) is independent of the direction of micro-rotations and it decreases monotonically and finally converges to 0.6705 as number of rotations tends to \( \infty \). The inverse of \( k \) is called as CORDIC Gain. The exact scaling-factor value \([19]\) depends on the number of iterations and is given by the following equation,

\[
k_n = \prod_{i=0}^{n-1} \frac{1}{\sqrt{1 + 2^{-2i}}}
\]

Redundant CORDIC methods with a constant scale factor for sine and cosine computation is mentioned in \([20]\). The
above mentioned equations form the backbone of CORDIC algorithm. These will be used in most of the architectures and are mentioned in the forthcoming sections. The DSP applications today demand low power, error resiliency and high performance. To achieve this, there is a need to design architectures capable of addressing these issues. Most of the image or video processing applications constitute DCT in its architecture, which is considered as the most power hungry block. This research work considers the calculations of the DCT matrix coefficients by employing CORDIC algorithm to ensure reduced hardware and software complexity.

CORDIC is used in its rotation mode of operation to generate the cosine values of some specific angles, which are nothing but the DCT matrix coefficients and can be found out using various CORDIC architectures. In a DCT matrix of particular dimension the value of angles for which the coefficients need to be found out is fixed. Thus, in this case, angle recoding scheme can be used, as it is efficient only if we previously know the value of angles for which the cosine values are to be generated.

Scaling factor also plays an important role in determining the latency and complexity of operation. A scale-free design is thus to be exploited, so that the design metrics are improved. As the image processing applications involve human intervention, persistence of vision can be exploited so as to get nearly accurate results, which means that approximation is to be done. It is clear that CORDIC uses adders in its hardware, so instead of using accurate adders, approximate adders can be utilized which will consume less power and provide with tolerable errors in the results.

The concept of hybrid angles is also to be employed as it would limit the iterative nature of CORDIC to a certain extent and introduce partial parallelism. To reduce the number of iterations and avoid data dependency, lookahead approach proves beneficial, as it is capable of performing more than one rotation in a single iteration. The above mentioned concepts will be used to propose a novel error tolerant and energy efficient CORDIC architecture.

### III. Literature Survey

This section covers various CORDIC architectures and the advantages and limitations associated with them that have been studied during the literature review.

#### A. Conventional CORDIC Architecture

Proposed in the year 1959, [1] is the very first CORDIC architecture, which talks about the basic architecture of CORDIC, the input and output relation, rotations, the gain, modes of operation etc. which are also discussed here. The input and output vectors are related by Givens Rotation [18] as stated in equation 5 and it is modified to equation 6

\[
\begin{bmatrix}
  x_{i+1} \\
  y_{i+1}
\end{bmatrix} = \begin{bmatrix}
  \cos \theta & -\sin \theta \\
  \sin \theta & \cos \theta
\end{bmatrix} \begin{bmatrix}
  x_i \\
  y_i
\end{bmatrix}
\]

(5)

\[
\begin{bmatrix}
  v_{i+1} \\
  u_{i+1}
\end{bmatrix} = \begin{bmatrix}
  \cos \theta & -\sin \theta \\
  \sin \theta & \cos \theta
\end{bmatrix} \begin{bmatrix}
  v_i \\
  u_i
\end{bmatrix}
\]

(6)

where, \([v_{i+1}]\) is the vector at \((i+1)^{th}\) iteration and \([v_i]\) is the vector at \(i^{th}\) iteration. Let the Givens Rotation matrix be denoted by \(R_g\). \(R_g\) is considered for modifications and \(\frac{1}{\cos \theta}\) is taken out as a common factor, which reduces the matrix to,

\[
\begin{bmatrix}
  1 & -\tan \theta \\
  \tan \theta & 1
\end{bmatrix}
\]

(7)

For calculations in conventional CORDIC this matrix is always considered, as it is convenient to represent \(\tan \theta\) terms of \(2^{-i}\). But it also brings a disadvantage with it, i.e the \(\frac{1}{\cos \theta}\) term which is nothing but the scaling factor as mentioned above. Applying trigonometric rules, the term gets modified to equation 3. Figure 4 shows the basic CORDIC architecture.

The introduction of scaling-factor simplifies the algorithm by saving on angle calculations, but at the same time it introduces the need of multiplier to correct the final vector length/ co-ordinate values. Though it incurs more hardware, we cannot totally neglect it as, it introduces non-tolerable error. Approaches to deal with this issue have been explained further.

To understand the working of CORDIC it is primarily required to know about its mode of operation. CORDIC basically operates in two modes for three trajectories i.e. linear, circular and hyperbolic, depending upon the operation required to perform. The modes are, 1) Rotation Mode and 2) Vectoring Mode. The conventional architecture is given by Figure 4 and the basic equations on which CORDIC relies as mentioned in [19] are,

\[
x_{i+1} = k(x_i \cos \theta_i - y_i \sin \theta_i) = x_i - \sigma_i 2^{-i} y_i \\
y_{i+1} = k(y_i \cos \theta_i + x_i \sin \theta_i) = y_i + \sigma_i 2^{-i} x_i \\
z_{i+1} = z_i - \sigma_i \tan^{-1}(2^{-i})
\]

(8)

(9)

(10)

where, \(z_{i+1}\) is the remaining value of angle after \(i^{th}\) iteration i.e. the residual angle.

1) Rotation Mode: In this mode of operation, the input vector is rotated until the residual angle becomes zero. After every rotation is performed, the residual angle is checked for both its sign and value as, the sign tells about the direction of next rotation and value ensures whether another iteration needs to be performed or not. Generally, the initial values of \(x\) and \(y\) co-ordinates are taken as, 1 and 0 respectively, whereas, \(z\) will contain the angle by which a rotation needs to be performed. The equations [11] and [12] are performed until equation [13] is satisfied.

\[
x_n = k(x_0 \cos \theta_0 - y_0 \sin \theta_0)
\]

(11)

\[
y_n = k(y_0 \cos \theta_0 + x_0 \sin \theta_0)
\]

(12)

\[
z_n = 0
\]

(13)
CORDIC Operating modes
Vectoring Trajectories
1) Trigonometric
2) Hyperbolic
3) Logarithmic

Types of CORDIC
Multiplication
1) Finding Eigen value
2) SVD
3) QR factorization

Applications
Conventional/
Basic
Hybrid
Scale−free

Lookahead

Functions
Matrices
Real and complex

Fig. 3: CORDIC: An overview

2) Vectoring Mode :: Here, the input vector is rotated until its y component gets reduced to zero i.e. the purpose is to take the vector near x-axis, in order to obtain the vector amplitude and phase. $z_n$ will contain the value by which the vector was rotated which in case of rotation mode was used as a residual angle storing register. The equations for this mode, as mentioned in [19] are given below,

$$x_n = k \sqrt{x_0^2 + y_0^2}$$  \hspace{1cm} (14)  
$$y_n = 0$$  \hspace{1cm} (15)  
$$z_n = z_0 + tan^{-1} \left( \frac{y_0}{x_0} \right)$$  \hspace{1cm} (16)  

CORDIC is an algorithm which allows operation in different modes and trajectories as needed for e.g. for normal trigonometric functions it operates in circular mode while for the hyperbolic ones it will work in hyperbolic trajectory. Figure 5 as mentioned in [21] shows rotation mode of CORDIC for all the three trajectories. A reconfigurable architecture which considers both modes for circular and hyperbolic trajectories is mentioned in [22].

Certain limitations of conventional CORDIC architecture are,

i) Need of scale-factor calculation.

ii) Increased latency and data dependency due to iterative nature.

iii) Selection of direction of micro-rotations.

B. Hardware efficient CORDIC architecture (Scale-free CORDIC)

Scale-factor calculation requires a multiplier which incurs extra hardware. But it cannot be totally neglected, as it leads to an intolerable error of $\sim 60\%$. Instead of totally neglecting it, an alternative to scale-factor, such that no loss of accuracy is there, would be a much better solution. Design of scale-free CORDIC, as mentioned in [23], [24], [25] is divided in two steps, first one is the co-ordinate calculation (shown in Figure 6) while the second step is the micro-rotation sequence identification (Table I). A new efficient window-architecture design using completely scaling-free CORDIC pipeline is discussed in [26] and a scale-free hyperbolic CORDIC processor is mentioned in [27].

The Rotation matrix which is given by equation [2] contains sine and cosine terms, which on simplification introduces scaling-factor. If these terms are replaced by their respective Taysors’ series, there would not be any requirement for finding out the scaling factor. Approximation of third, fourth or any order, applied to Taylor series will replace the complex sine and cosine terms by simple terms that can be implemented by simple shift operations. The rotation matrix then gets reduced to,

$$\begin{bmatrix}
1 - \theta^2/2 & -\theta + \theta^3/6 \\
\theta - \theta^3/6 & 1 - \theta^2/2
\end{bmatrix}$$  \hspace{1cm} (17)  

It is obtained after applying third order of approximation to the Taylor series of sine and cosine functions. This helps
to find out the next iteration values and is used in the co-ordinate calculation unit. For identifying the micro-rotations it uses leading-one bit detection technique. The main idea of scale-free CORDIC is restricting the micro-rotations to anticlockwise direction only. The leading-one bit detector is discussed below.

Leading-one bit detector follows the following steps:
i Firstly the angle to be rotated is converted into binary and then into hexadecimal format.
ii Then the leading one bit is found out, calculating from the MSB bit position i.e. starting from count 15 and it is made 0.
iii This is continued up to the point where the value (angle \( z \)) gets reduced to 0.

Certain limitations of scale-free CORDIC are stated below:
i The region of convergence (ROC) provided by scale-free CORDIC is very less and thus it is less suitable for practical applications.
ii Because of the approximation applied to the Taylor series, there is a restriction on the start iteration value index \( i \).
iii It is best suitable only for 16 bit data word length, because if we increase the bit width, the number of iterations increase, thus leading to more complexity.

CORDIC in general is better in terms of hardware requirement, but it consumes more time to generate the output as compared to other methods. So, to overcome this limitation, some CORDIC architectures that have less latency as given in [28], [29] are discussed further.

### C. Lookahead CORDIC architecture

Basic CORDIC is iterative in nature which introduces data dependency due to the following reasons,
1) Next micro-rotation can be done only if the previous rotation has been completed.
2) It is performed on the vector which is obtained by the previous rotation.

Thus, it becomes very difficult to remove data dependency. The only solution to this is, an architecture as discussed in [17] which previously detects the direction of micro-rotation so that
more number of these can be performed in a single iteration. This reduces both, the number of iterations, thus indirectly reducing the latency and data dependency.

One such architecture which employs this concept is Lookup-head CORDIC. Figure 7 shows the block diagram of Lookahead CORDIC. The principle of working is similar to that of a carry lookahead adder. Lookahead means that a number of CORDIC iterations can be computed ahead to finish the iterations at one time. The basic idea of the proposed scheme is to reduce the iteration number directly while maintaining the precision. The design consists of vertical and parallel circuits which help to remove the data dependency. This approach has very low latency which reduces when more iteration are done within a single iteration. Following mentioned are the equations for four consecutive iterations.

\[
x_1 = x_0 - \sigma_0 2^{-0} y_0
\]

\[
y_1 = y_0 + \sigma_0 2^{-0} x_0
\]

\[
x_2 = x_1 - \sigma_1 2^{-1} y_1
\]

\[
y_2 = y_1 + \sigma_1 2^{-1} x_1
\]

\[
x_3 = x_2 - \sigma_2 2^{-2} y_2
\]

\[
y_3 = y_2 + \sigma_2 2^{-2} x_2
\]

\[
x_4 = x_3 - \sigma_3 2^{-3} y_3
\]

\[
y_4 = y_3 + \sigma_3 2^{-3} x_3
\]

These equations will be then used to find out the value of \(\sigma_0, \sigma_1, \sigma_2\) and \(\sigma_3\), which will thus avoid the requirement of more number of iterations, as, number of rotations will be performed in a single iteration. This also eliminates the data dependency which was relevant in the conventional CORDIC architecture, as it was iterative in nature. It is clear from the equations mentioned below. These are obtained by substituting the values of \(x_1, x_2, x_3\) and \(y_1, y_2, y_3\) in the above equations, so as to get a relation between \(x_0\) and \(y_0\) and \(x_4\). The final equations obtained are,

\[
x_4 = x_0 P - y_0 V
\]

\[
y_4 = y_0 P + x_0 V
\]

where,

\[
P = \begin{bmatrix}
2^{-0}(+1) \\
2^{-1}(-\sigma_0 \sigma_1) \\
2^{-2}(-\sigma_0 \sigma_2) \\
2^{-3}(-\sigma_1 \sigma_2 - \sigma_0 \sigma_3) \\
2^{-4}(-\sigma_1 \sigma_3) \\
2^{-5}(-\sigma_2 \sigma_3) \\
2^{-6}(+\sigma_0 \sigma_1 \sigma_2 \sigma_3)
\end{bmatrix}
\]

\[
V = \begin{bmatrix}
2^{-0}(+\sigma_0) \\
2^{-1}(+\sigma_1) \\
2^{-2}(+\sigma_2) \\
2^{-3}(-\sigma_1 \sigma_2 \sigma_0 + \sigma_3) \\
2^{-4}(-\sigma_0 \sigma_1 \sigma_3) \\
2^{-5}(-\sigma_0 \sigma_2 \sigma_3) \\
2^{-6}(-\sigma_1 \sigma_2 \sigma_3)
\end{bmatrix}
\]

These parallel shift \((P)\) and vertical shift \((V)\) circuits are then generated, which are finally used to get the required output values. The conventional CORDIC is iterative in nature and so, the number of iterations in the two data paths of same CORDIC cannot be changed. When there is a need to perform different number of iterations for the two data paths, for a single CORDIC, this approach is the solution. As here, the micro-rotation direction for more iterations is found out previously, data dependency is removed, and so the next iteration no more dependent on the previous ones. This allows performing more rotations in a single iteration, which thus reduces the latency. The drawback it carries is that, it requires extra circuitry for developing the parallel and vertical shift logics, which increases with an increase in the number of iterations performed within a single rotation.
**D. Hybrid CORDIC architecture**

The core idea behind CORDIC algorithm is that the angles are represented in terms of to the power of 2, thus it can be said that the initial angle is a sum of arc tangent constants. The vector will be rotated by these fixed angular values, the only difference being the direction in which it will be rotated. This depends upon the direction of micro-rotation i.e. \( \sigma_i \), which makes it dependent thus making it difficult for parallelization. The hybrid CORDIC architectures [29] as shown in Figures 8 and 9 make it partially parallelized by computing \( \sigma_i \) parallelly without affecting the accuracy of the algorithm.

A greedy algorithm which takes only \( O(n^2) \) operations is developed to perform CORDIC angle recoding. It is proven that this algorithm is able to reduce the total number of required elementary rotation angles by at least 50% without affecting the computational accuracy. AR methods are well-suited for many signal processing and image processing applications where the rotation angle is known a priori, such as when performing the discrete orthogonal transforms like discrete Fourier transform (DFT), the discrete cosine transform (DCT), etc. Types of AR methods include, Elementary-Angle-Set recoding: Using this recoding scheme the total number of iterations could be reduced by at least 50% keeping the same n-bit accuracy unchanged. A similar method of angle recoding in vectoring mode called as the backward angle recoding.

Extended Elementary-Angle-Set Recoding (EEAS): EEAS has better recoding efficiency in terms of the number of iterations and yields better error performance than the AR scheme based on EAS.

Parallel Angle recoding: The AR methods could be used to reduce the number of iterations by more than 50%, when the angle of rotation is known in advance. However, for unknown rotation angles, their hardware implementation involves more cycle time than the conventional implementation, which results in a reduction in overall efficacy of the algorithm.

To reduce the cycle time of CORDIC iterations in such cases, a parallel angle selection scheme can be used in conjunction with the AR method, to gain the advantages of the reduction in iteration count, without further increase in the cycle time. The elementary angles can be tested in parallel and the direction for the micro-rotations can be determined quickly to minimize the iteration period as shown in Figure 8.

CORDIC is iterative in nature, which causes data dependency between different iterations and also within the same iteration. If there is a need to perform different iterations for \( x \) and \( y \) coordinates, it is not possible using the conventional CORDIC, instead, an architecture which removes this data dependency is needed. The next subsection discusses about this in detail.

**E. Angle recoding CORDIC architecture**

Performing iterations until required result is obtained induces complexity if it increases beyond a limit i.e. if we get the necessary accurate output in less than 5 iterations then it is feasible and the hardware is less complex, but if increased beyond this limit, the hardware complexity increases. An architecture which reduces this uses the concept of angle recoding [30]. The purpose of angle recoding (AR) is to reduce the number of CORDIC iterations by encoding the angle of rotation as a linear combination of a set of selected elementary angles of micro-rotations.

For applications where the angle of rotation is known in advance, a method to speed up the execution of the CORDIC algorithm by reducing the total number of iterations is presented. This is accomplished by using a technique called angle recoding, which encodes the desired rotation angle as a linear combination of very few elementary rotation angles. Each of these elementary rotation angles takes one CORDIC iteration to compute. The fewer the number of elementary rotation angles, the fewer the number of iterations are required.
for either of the circular or hyperbolic trajectories and in rotation and vectoring modes as well. The CORDIC is capable of computing various functions, trigonometric, exponential, logarithm, roots, etc. and Figure 11 shows the reconfigurable CORDIC architecture that can perform the mentioned functionality.

![Fig. 10: Parallel Angle Recoding](image)

![Fig. 11: Reconfigurable CORDIC architecture](image)

### G. Radix-4 CORDIC architecture

This is a very old architecture, in which double shifts in each iteration, as compared to the conventional CORDIC are performed. This means that, instead of shifting the vector by \( i \) bits in \( i^{th} \) iteration, it is shifted by \( 2i \) bits in every \( i^{th} \) iteration. In this way it helps in reducing the number of iteration and leads to a significant reduction in the number of cycles for a word serial architecture which in turn reduces the latency. The equations get modified as,

\[
x_{i+1} = x_i + \sigma_i 4^{-i} y_i
\]

\[
y_{i+1} = y_i - \sigma_i 4^{-i} x_i
\]

\[
z_{i+1} = z_i - \alpha_i \sigma_i
\]

Limitation of radix-4 CORDIC: The scaling factor in this design is not constant as in case of the conventional CORDIC. This is because, unlike in the basic CORDIC, where \( \sigma \) carries values -1 and 1, here it carries the values, -2, -1, 1, 2, which restricts the scaling-factor from being a constant value. Thus, it is needed to find out the scaling factor which is more troublesome than conventional CORDIC. So, it incurs extra hardware and cycles to calculate the value of the scale factor. The equation of scaling factor here as mentioned in [31], is modified to equation 33

\[
k = \prod_{i=0}^{\infty} k_i = \prod_{i=0}^{\infty} \sqrt{1 + \sigma_i^2 4^{-2i}}.
\]

More number of iterations also increases the delay. So to overcome this limitation, an architecture which generates the output in less number of iterations, as mentioned next, is a solution.

### H. Repetitive Iteration CORDIC architecture

One of the major drawbacks of Conventional CORDIC is the data dependency due to its iterative nature. It is partially overcome by a repetitive iteration architecture (RICO) [8] as shown in Figure 12 Here, the number of iterations that are to be performed is fixed beforehand and is the same for any value of input angle. The working of this architecture is broadly divided into two units: (i) The \( \sigma \) generation unit and (ii) The shift generation unit.

For avoiding data dependency, the iteration number 0, 1 and 2 are performed in a single step, using a single CC. The coordinates of the vector that has to undergo through these three iterations is determined by rotating twice the initial input vector \( IV(x_{in}, y_{in}) \), where \( x_{in} = 1 \) and \( y_{in} = 0 \) by an angle of 7°. Coordinates of this vector i.e \( OV(x_{out}, y_{out}) \) are used as input x and y values for the 0\textsuperscript{th}, 1\textsuperscript{st} and 2\textsuperscript{nd} iteration. A quality tunable CORDIC with RICO as its core is presented in [32].

### IV. RESULTS AND DISCUSSION

The following sub-sections present the comparison of MATLAB simulation results for the CORDIC architectures discussed in this paper. Some of the CORDIC architectures have been implemented and their performance comparison has been done. The DCT coefficients are generated using different CORDIC architectures and the errors in those coefficients with respect to the accurate DCT coefficients has been provided in Table 11. The DCT coefficients obtained from conventional, lookahead CORDIC and RICO are used to form individual DCT matrices. These matrices are applied on some test images and the corresponding PSNR values have been obtained. Figure 13 shows the qualitative analysis for this.
TABLE II: CORDIC algorithm for various computations

| Required operation | Mode       | Trajectory | Initial value | Final output |
|--------------------|------------|------------|---------------|--------------|
| cosθ, sinθ, tanθ   | Rotation   | Circular   | x<sub>i</sub> = 1, y<sub>i</sub> = 0, θ = θ<sub>i</sub> | x<sub>out</sub> = cosθ, y<sub>out</sub> = sinθ |
| Polar to rectangular | Rotation   | Circular   | x<sub>i</sub> = R, y<sub>i</sub> = 1, θ = θ<sub>i</sub> | x<sub>out</sub> = R cosθ, y<sub>out</sub> = R sinθ |
| coshθ, sinhθ, tanhθ | Rotation   | Hyperbolic | x<sub>i</sub> = 1, y<sub>i</sub> = 0, θ = θ<sub>i</sub> | x<sub>out</sub> = coshθ, y<sub>out</sub> = sinhθ |
| exp(θ)             | Rotation   | Hyperbolic | x<sub>i</sub> = 1, y<sub>i</sub> = 0, θ = θ<sub>i</sub> | exp(θ) = coshθ + sinhθ (using above) |
| tan<sup>-1</sup>a   | Vectoring  | Circular   | x<sub>i</sub> = a, y<sub>i</sub> = 1, θ = 0 | θ = tan<sup>-1</sup>a |
| Rectangular to polar | Vectoring  | Circular   | x<sub>i</sub> = a, y<sub>i</sub> = b, θ = 0 | x<sub>out</sub> = √a<sup>2</sup> + b<sup>2</sup>, θ = tan<sup>-1</sup> b/a |
| Division (1/x)     | Vectoring  | Linear     | x<sub>i</sub> = a, y<sub>i</sub> = b, θ = 0 | x<sub>out</sub> = 1/a, θ = 1/2 ln(a) |

V. CONCLUSION

CORDIC is a class of algorithm which is capable of performing simple to highly complex mathematical operations, functions, etc. by the use of adders and shifters only which makes it both hardware and time efficient. Various types of architectures like the conventional one, a scale-free type of design, lookahead CORDIC i.e. the one employing a concept parallel to that used in a carry lookahead adder (CLA), radix-4 CORDIC, angle recoding, hybrid CORDIC, etc. have been mentioned in the paper. Apart from the survey, these architectures have been used to generate circular trigonometric values for which they are operated in the rotation mode. To solve the purpose MATLAB has been used as it is an easy way to represent the functionality of the architectures and the accuracy of the designs is tested here. Qualitative and quantitative analysis of the mentioned architectures is also done using MATLAB and accordingly the CORDIC architectures have been compared. To verify the efficacy of these architectures, they have been used to obtain the DCT coefficients are found

![Fig. 12: Repetitive Iteration CORDIC Architecture (RICO)](image-url)

TABLE III: Error (%) in DCT values

|                      | CORDIC | Conventional | Lookahead | RICO |
|----------------------|--------|--------------|-----------|------|
| Coefficient ↓        |        |              |           |      |
| a                    | 1.8964 | 3.2422       | 0.387     |      |
| b                    | 0.9958 | 0.2164       | 0.2814    |      |
| c                    | 5.0276 | 1.1065       | 0.1202    |      |
| d                    | 0      | 0.5657       | 0.0282    |      |
| e                    | 7.6673 | 2.4118       | 0.503     |      |
| f                    | 0.47048| 26.6596      | 1.5682    |      |
| g                    | 6.7692 | 3.1794       | 14.7      |      |

TABLE IV: Quantitative analysis

|                      | CORDIC | Conventional | Lookahead | RICO |
|----------------------|--------|--------------|-----------|------|
| Design metrics ↓     |        |              |           |      |
| MSE                  | 0.427  | 9.049        | 0.3296    |      |
| PSNR                 | 53.512 | 38.25        | 52.556    |      |
| SSIM                 | 1      | 0.9932       | 0.99976   |      |
| GMSD                 | 0.000186| 0.00393     | 0.000724  |      |
Fig. 13: Images obtained after DCT and IDCT using different CORDIC architectures (a)-(e): conventional CORDIC, (f)-(j): lookahead CORDIC and (k)-(o): RICO out which is further used to form an 8x8 DCT matrix, to be used to process benchmark images and videos. Finally the architectures are compared on the basis of the design metrics obtained from MATLAB and Design compiler.

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