A Class of Differentiator-Based Multifunction Biquad Filters Using OTRAs

Neeta PANDEY1, Rajeshwari PANDEY1, Rashika ANURAG2, Ritu VIJAY3

1Department of Electronics and Communication Engineering, Delhi Technological University, Main Bawana Road, 110042 Delhi, India
2Department of Electronics and Communication Engineering, JSS Academy of Technical Education Noida, C Block, Phase 2, Industrial Area, Sector 62, 201301 Noida, India
3Department of Electronics, Banasthali University, Vanasthali Road, 304022 Banasthali, India
n66pandey@rediffmail.com, rajeshwaripandey@gmail.com, raashika@jssaten.ac.in, rituvijay1975@yahoo.co.in

DOI: 10.15598/aeee.v18i1.3363

Abstract. This paper presents Signal Flow Graph (SFG) approach-based realization of Single Input Multiple Output (SIMO) filter topologies. A differentiator is placed as basic building block. A total of sixteen variants are derived from the proposed differentiator-based SFG. The Operational Trans-Resistance Amplifier (OTRA), an active block having low parasitics at input terminals, is used to validate the proposed methodology. All the derived filter structures use three OTRAs, six resistors and two capacitors. The filter performance parameters can be adjusted independently. The functional verification of the proposed method is done via SPICE simulations using 0.18 µm CMOS technology parameters from MOSIS.

Keywords
Filter, OTRA, SIMO.

1. Introduction

The Continuous-Time (CT) filters are widely used in consumer electronics, instrumentation, military ordnance, telecommunications and radar systems, etc. Therefore, considerable research efforts have been devoted to developing CT filters based on wide variety of active blocks. The bandwidth of traditional active blocks is limited by closed-loop voltage gain and presence of the parasitic elements influences the performance of filter. The active block, OTRA [1], uses current feedback technique, which makes its bandwidth almost independent of the gain. Additionally, the parasitic impedances at input terminals are low and have negligible effect on circuits. Therefore, OTRA-based CT filters have been investigated in recent past [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19] and they can be categorized as (i) single and (ii) multiple OTRA-based structures. Though single OTRA-based filters [2, 3, 4] and [5] are useful when power consumption is important, they show larger sensitivity to component variation and are less versatile than their multiple OTRA-based counterparts [1, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19]. The salient features of the available multiple OTRA-based CT filters are listed below:

- A single response is available in [1, 5, 7, 8, 10, 15] and [17], whereas [8, 9, 11, 12, 13, 14] and [15] offer multiple responses.
- Single/Multiple output filters [6, 7, 8] and [16] may, however, give other responses by choosing appropriate input excitation terminal.
- Filters [1, 8, 10, 16] and [18] impose condition on component/switch selection for obtaining the responses.

The underlying principle of these filters [1, 5, 9, 10, 11, 12, 13, 14] and [16] is connection of lossy and lossless integrator. In the recent past, the researchers have developed few differentiator-based signal processing and generating circuits [7, 8, 9, 15, 20, 21, 22, 23, 24, 25, 26, 27] and [28] finding applications in the area of control system and biomedical instrumentation. However, the area is not much explored, as evident from the limited literature available. Considering this, differentiator-based SIMO filter topologies designed using SFG-based approach are proposed in this paper and OTRA is used to validate it.
It is pertinent to mention here that SFG-based approach, with integrators, has been employed in [29], [30], [31], [32] and [33].

The paper is arranged in five sections. Section 2 includes the discussion on the proposed SFG, followed by a brief review of OTRA and basic signal processing blocks designed using OTRA. The OTRA-based SIMO filter topologies are also included in the same section subsequently. The non-ideality analysis is given in Sec. 3, followed by simulation results in Sec. 4. The paper is finally concluded in Sec. 5.

2. Circuit Description

2.1. The Proposed SFG

The proposed differentiator-based SFG, which uses two differentiators in forward path, is depicted in Fig. 1. The coefficients $k_i$ ($i \in \{1, 2, 3, 4\}$) may assume value 1 and $-1$. Four different SFGs can be generated from Fig. 1 by selecting the values of $k_1$ and $k_2$ respectively as $(1, 1)$, $(1, -1)$, $(-1, 1)$ or $(-1, -1)$ as depicted in Fig. 2. These SFGs represent four different topologies and are referred respectively as topology 1, topology 2, topology 3 and topology 4. The values of $k_3$ and $k_4$ are chosen so that appropriate transfer functions can be obtained.

Fig. 1: The proposed differentiator-based SFG.

It may be noted that the SFG in Fig. 1 uses an inverting differentiator, followed by a non-inverting differentiator. Alternate SFGs can be derived by placing

- a non-inverting differentiator followed by an inverting differentiator,
- two non-inverting differentiators, or
- two inverting differentiators.

The resulting SFGs are depicted in Fig. 3.

In each SFG in Fig. 3, $k_1$ and $k_2$ may further be selected as $(1, 1)$, $(1, -1)$, $(-1, 1)$ or $(-1, -1)$, thus providing a total to sixteen SFGs, and are shown in Fig. 4.

Fig. 2: SFGs generated from Fig. 1 for $k_1$ and $k_2$ as (a) topology 1, (b) topology 2, (c) topology 3, (d) topology 4.

2.2. The OTRA

The OTRA is an active block with two low-impedance input terminals and a low-impedance output terminal. The circuit symbol of OTRA is given in Fig. 5 and its terminals are characterized by matrix of Eq. (1):

\[
\begin{bmatrix}
V_p \\
V_n \\
V_o
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 \\
0 & 0 & 0 \\
R_m & -R_m & 0
\end{bmatrix}
\begin{bmatrix}
I_p \\
I_n \\
I_o
\end{bmatrix},
\]

where $R_m$ is trans-resistance gain of OTRA. The value of $R_m$ is ideally infinity; therefore, OTRA is generally used in negative feedback configuration.
The OTRA-based realization of voltage addition/subtraction is shown in Fig. 6. It uses five resistors and one OTRA. By equating the currents of inverting and non-inverting terminals, the output of the circuit from Fig. 6 is obtained as:

$$V_o = R_5 \left( \frac{V_1}{R_1} + \frac{V_2}{R_2} - \frac{V_3}{R_3} - \frac{V_4}{R_4} \right). \quad (2)$$

Exchanging \((V_i, R_i)\), where \(i \in \{1, 2\}\) with \((V_j, R_j)\), where \(j \in \{3, 4\}\) in Fig. 6 yields the following relation:

$$V_o = -R_5 \left( \frac{V_1}{R_1} + \frac{V_2}{R_2} - \frac{V_3}{R_3} - \frac{V_4}{R_4} \right). \quad (3)$$

It may be noted that Eq. (3) is inverting form of Eq. (2).
By choosing the values of resistances appropriately, the desired addition-subtraction can be performed. Equation (2) provides non-inverting output, whereas Eq. (3) gives an inverting output.

The OTRA-based circuits of inverting and non-inverting differentiators are given in Fig. 7 and their respective outputs are given by:

\[ V_o = -sCRV_{in}, \quad (4) \]
\[ V_o = -sCRV_{in}. \quad (5) \]

The transfer functions of the topology in Fig. 8(a) are obtained as:

\[ \frac{V_1}{V_{in}} = \frac{k}{D(s)}, \]
\[ \frac{V_2}{V_{in}} = \frac{-k(sR_2C_2)}{D(s)}, \]
\[ \frac{V_3}{V_{in}} = \frac{-k(s^2R_1R_2C_1C_2)}{D(s)}. \quad (6) \]

where

\[ D(s) = 1 + \frac{sR_2R_3C_2}{R_5} + \frac{s^2R_1R_2R_4C_1C_2}{R_4}. \quad (7) \]

The OTRA-based realization of SFGs from Fig. 2 is depicted respectively in Fig. 8(a), Fig. 8(b), Fig. 8(c) and Fig. 8(d). It may be noted that the realizations from Fig. 8(a) and Fig. 8(b) are same as those given in Fig. 8(c) and Fig. 8(d) respectively, since their corresponding \( k_1k_2 \) product terms are the same.
The transfer functions of the topology in Fig. 8(b) are computed as:

$$\frac{V_1}{V_{in}} = \frac{-k}{D(s)},$$

$$\frac{V_2}{V_{in}} = \frac{k(sR_2C_2)}{D(s)},$$

$$\frac{V_3}{V_{in}} = \frac{k(s^2R_1R_2C_1C_2)}{D(s)}.$$  \hspace{1cm} (8)

It may be noted that $V_1$, $V_2$, and $V_3$ respectively represent low pass, band pass and high pass responses. All the transfer functions at different nodes represented by Eq. (8) and Eq. (9) are characterized by following pole frequency ($\omega_0$), bandwidth ($\frac{\omega_0}{Q}$) and quality factor ($Q$):

$$\omega_0 = \left(\frac{R_4}{R_1R_2R_3C_1C_2}\right)^\frac{1}{2},$$

$$\omega_0\frac{Q}{Q} = \frac{R_4}{R_1R_2C_5},$$

$$Q = R_5\left(\frac{R_1C_1}{R_1R_2R_3C_2}\right)^\frac{1}{2}.$$  \hspace{1cm} (9, 10, 11)

It is clear from Eq. (9), Eq. (10) and Eq. (11) that both bandwidth and quality factor can be adjusted independently by varying $R_5$ without modifying the pole frequency. The pole frequency may be varied by changing $R_i$ and $C_i$ ($i = 1, 2$) and quality factor may be kept constant by assuming $R_3 = R_4 = R_5$ and $\frac{R_2}{C_2} = \frac{C_1}{C_1}$. Further, the gain of the filter responses can be changed by varying the value of $k$.

The OTRA-based realizations of the SFGs listed in Fig. 4 are also obtained and omitted for the sake of brevity. The transfer functions are similar to the one given in Eq. (8), Eq. (9) and Eq. (10).

3. The Non-Ideality Analysis

The response of the filter may deviate due to non-ideality of OTRA. Ideally, the trans-resistance gain $R_m$ is assumed to approach infinity. However, in practice, $R_m$ is a frequency-dependent finite value. Considering a single-pole model for trans-resistance gain, $R_m(s)$ can be expressed as:

$$R_m(s) = \frac{R_0}{1 + \frac{s}{\omega}},$$  \hspace{1cm} (12)

where $R_0$ is low-frequency trans-resistance gain. For high-frequency applications, the trans-resistance gain $R_m(s)$ is approximated as:

$$R_m(s) \approx \frac{1}{sC_p}.$$  \hspace{1cm} (13)

where

$$C_p = \frac{1}{R_0\omega_0}.$$  \hspace{1cm} (14)

Taking this effect into account, the transfer functions in Fig. 8(a) in presence of finite transimpedance are computed as:

$$\frac{V_1}{V_{in}} = \frac{k_n}{D_n(s)},$$

$$\frac{V_2}{V_{in}} = \frac{-k_n(sR_2C_2)}{D_n(s)(1 + sR_2C_2)},$$

$$\frac{V_3}{V_{in}} = \frac{-k_n(s^2R_1R_2C_1C_2)}{D_n(s)(1 + sR_2C_2)},$$  \hspace{1cm} (15)

where

$$D_n(s) = (1 + sR_3C_1p) + sR_2C_2\left(\frac{R_3}{R_3} + (1 + sR_2C_2)\right),$$

$$D_n(s) = (1 + sR_3C_1p)(1 + sR_2C_2).$$  \hspace{1cm} (16)

It is clear from Eq. (15) and Eq. (16) that transfer functions modify in presence of non-ideality. These equations reduce to Eq. (5) and Eq. (7) by choosing the operating frequency below min $\left(\frac{1}{\omega_p}, \frac{1}{\omega_p}, \frac{q}{\omega_p}\right)$.

4. Simulation Results

To verify the proposed scheme, the functionality of the filter from Fig. 8(a) is tested through SPICE simulations using CMOS OTRA architecture of 34 and 0.18 μm CMOS process parameters provided by MOSIS (AGILENT). Supply voltages ±1.5 V are taken. The simulation is performed for pole frequency of 159 kHz and unity quality factor. All the resistances are taken as 10 kΩ and capacitor is taken as 100 pF. The simulated frequency response for low pass, band pass and high pass for the circuit from Fig. 8(a) are depicted in Fig. 9. The total power consumption is found to be 6 mW.

The other set of simulations is carried out to show tuning of band pass filter center frequency and gain. The center frequency is varied by changing $R_1$ and $R_2$ simultaneously from 5 kΩ to 20 kΩ in step of 5 kΩ while keeping all other resistances and capacitances at 10 kΩ and 100 pF respectively. This setting leads to constant $Q$ value. Figure 11 shows the simulated band pass response for variation in center frequency and $Q$ with change in resistance. It may be noted that $Q$ varies slightly from unity value, which may be attributed to non-idealities of OTRA.

For variation of band pass response gain while keeping center frequency constant, all resistances except the one connected to input terminal and capacitances are
Fig. 9: Simulated low pass, band pass and high pass responses of the circuit from Fig. 8(a).

Fig. 10: Time domain waveform of low pass response.

The values of $k = 1, 2$ and 4 are taken to obtain gain of 1, 2 and 4, respectively. The simulated response is depicted in Fig. 12, which agrees with theoretical predictions.

The SPICE simulations are also performed to observe the time domain behavior. All resistances and capacitances are kept at 10 kΩ and 100 pF, respectively. A 5 kHz sinusoidal input of 50 mV amplitude is applied to the filter and the low pass transient response is depicted in Fig. 10. Total harmonic distortion is also measured by changing input sinusoid amplitude and its value was found to be within 3 % till 150 mV amplitude. Another simulation is done by applying three sinusoids having frequencies of 10 kHz, 100 kHz and 1 MHz, respectively. Figure 13 shows the input and output waveforms and corresponding frequency spectrums. It is clear that the sinusoid having 1 MHz frequency is significantly attenuated.

Monte Carlo simulations are also done to check robustness of the proposed circuits by considering Gaussian distribution for fifty runs with 5 % variations in all passive components. For brevity, the histogram of circuit from Fig. 8(a) at LPF node output is depicted in Fig. 14; it implies the circuit is well operated within the theoretical frequency.

The performance parameters related to power consumption, THD and output noise are presented in [11], [12], [13] and [14]. The same is placed in Tab. 1. The higher power consumption of the proposed topology in
Fig. 12: Simulated (a) frequency band pass response, (b) $Q$ variation, (c) gain variation and (d) center frequency variation.

Fig. 13: Simulated transient low pass response (a) input and output waveforms and its (b) frequency spectrum.
Tab. 1: Summary of performance parameters.

| Ref. | OTRA implementation | Power consumption (%) | THD (%) | Output noise (µV·Hz⁻¹/²)
|------|---------------------|-----------------------|---------|-------------------------|
| [11] | CMOS based          | 4.04                  | 1.7     | –                       |
| [12] | CFOA based          | 421                   | –       | 4                       |
| [13] | CMOS based          | 2.58                  | 5.7     | 0.722                   |
| [14] | CMOS based          | 1.09                  | 6.74    | 0.316                   |
| Proposed | CMOS based      | 6                     | 3       | 0.140                   |

Fig. 14: Monte Carlo simulation results.

Comparison with other CMOS-based OTRA implementations may be observed. However, the output noise for the proposed topology is lowest.

5. Conclusion

An alternate realization for Single Input Multiple Output (SIMO) filter topologies has been presented in this contribution wherein differentiator is used as basic building block. An SFG is proposed for this purpose, which can further be used to derive sixteen SFGs through proper selection of inverting and non-inverting differentiators placed in loop; and their addition. The active block OTRA is used to verify the concept. All the realizations use three OTRAs, six resistors and two capacitors. The bandwidth and quality factor of these configurations can be adjusted independently of the pole frequency. The functional verification of the proposed method is done through SPICE simulations using 0.18 µm CMOS technology parameters from MOSIS.

References

[1] SALAMA, K. N. and A. M. SOLIMAN. Active RC Applications of the Operational Transresistance Amplifier. *Frequenz*. 2000, vol. 54, iss. 7–8, pp. 171–176. ISSN 2191-6349. DOI: [10.1515/FREQ.2000.54.7-8.171](https://doi.org/10.1515/FREQ.2000.54.7-8.171)

[2] GOKCEN, A. and U. CAM. MOS-C single amplifier biquads using the operational transresistance amplifier. *AEU - International Journal of Electronics and Communications*. 2009, vol. 63, iss. 8, pp. 660–664. ISSN 1434-8411. DOI: [10.1016/j.aeue.2008.05.008](https://doi.org/10.1016/j.aeue.2008.05.008)

[3] CAKIR, C., U. CAM and O. CICEKOGLU. Novel allpass filter configuration employing single OTRA. *IEEE Transactions on Circuits and Systems II: Express Briefs*. 2005, vol. 52, iss. 3, pp. 122–125. ISSN 1558-3791. DOI: [10.1109/TCSII.2004.842055](https://doi.org/10.1109/TCSII.2004.842055)

[4] KILINC, S. and U. CAM. Cascadable allpass and notch filters employing single operational transresistance amplifier. *Computers & Electrical Engineering*. 2005, vol. 31, iss. 6, pp. 391–401. ISSN 0045-7906. DOI: [10.1016/j.compeleceng.2005.06.001](https://doi.org/10.1016/j.compeleceng.2005.06.001)

[5] KILINC, S., A. U. KESKIN and U. CAM. Cascadable Voltage-Mode Multifunction Biquad Employing Single OTRA. *Frequenz*. 2007, vol. 61, iss. 3–4, pp. 84–86. ISSN 2191-6349. DOI: [10.1515/FREQ.2007.61.3-4.84](https://doi.org/10.1515/FREQ.2007.61.3-4.84)

[6] ANURAG, R., N. PANDEY, R. CHANDRA and R. PANDEY. Voltage Mode Second Order Notch/All - Pass Filter Realization Using OTRA. *i-Manager’s Journal on Electronics Engineering*. 2015, vol. 6, iss. 2, pp. 22–28. ISSN 2229-7286. DOI: [10.26634/jele.6.2.3763](https://doi.org/10.26634/jele.6.2.3763)

[7] CHEN, J., H. TSAO and S. LIU. Voltage-mode MOSFET-C filters using operational transresistance amplifiers (OTRAs) with reduced parasitic capacitance effect. *IEE Proceedings - Circuits, Devices and Systems*. 2001, vol. 148, iss. 5, pp. 242–249. ISSN 1359-7000. DOI: [10.1049/ip-cds:20010523](https://doi.org/10.1049/ip-cds:20010523)

[8] CHANG, C.-M., Y.-J. KO, Z.-Y. GUO, C.-L. HOU and J.-W. HORNING. Generation of Voltage-Mode OTRA-R/MOS-C LP, BP, HP, and BR Biquad Filter. In: *10th WSEAS International
[9] CHANG, C.-M., Y.-T. LIN, C.-K. HSU, C.-L. HOU and J.-W. HORNG. Generation of voltage-Mode OTRA-based multifunction biquad filter. In: 10th WSEAS International Conference on Instrumentation, Measurement, Circuits and Systems. Venice: WSEAS, 2011, pp. 21–27. ISBN 978-960-474-282-0.

[10] GOKCEN, A., S. KILINC and U. CAM. Fully integrated universal biquads using operational-transresistance amplifiers with MOS-C realization. Turkish Journal of Electrical Engineering & Computer Sciences. 2011, vol. 19, no. 3, pp. 363–372. ISSN 1303-6203. DOI: 10.3906/elk-1002-416

[11] PANDEY, R., N. PANDEY, S. K. PAUL, A. SINGH, B. SRIRAM and K. TRIVEDI. Voltage Mode OTRA MOS-C Single Input Multi Output Biquadratic Universal Filter. Advances in Electrical and Electronics Engineering. 2012, vol. 10, iss. 5, pp. 337–344. ISSN 1804-3119. DOI: 10.15598/aeve.v10i5.678

[12] SOLIMAN, A. M. and A. H. MADIAN. MOS-C KHN Filter Using Voltage OP AMP, CFOA, OTRA and DCVC. Journal of Circuits, Systems and Computers. 2009, vol. 18, iss. 4, pp. 733–769. ISSN 1793-6454. DOI: 10.1142/S021812660900523X

[13] SOLIMAN, A. M. and A. H. MADIAN. MOS-C Tow-Thomas Filter Using Voltage OP AMP, Current Feedback OP AMP and Operational Transresistance Amplifier. Journal of Circuits, Systems and Computers. 2009, vol. 18, iss. 1, pp. 151–179. ISSN 1793-6454. DOI: 10.1142/S0218126609004995

[14] SOLIMAN, A. M. History and Progress of the Tow–Thomas Biquad Filter Part II: OTRA, CCII, and DVCC Realizations. Journal of Circuits, Systems and Computers. 2008, vol. 17, iss. 5, pp. 797–826. ISSN 1793-6454. DOI: 10.1142/S0218126608004691

[15] DABAS, A. and N. ARORA. Tunable filters using operational transresistance amplifiers. International Journal of Electrical and Electronics Engineering. 2014, vol. 4, iss. 4, pp. 103–112. ISSN 2348-8379.

[16] MULLICK, R., N. PANDEY and R. PANDEY. Multi Input Single Output Biquadric Universal Filter using OTRA. i-Manager’s Journal on Circuits and Systems. 2015, vol. 3, iss. 3, pp. 30–37. ISSN 2322-035X. DOI: 10.26634/jcir.3.3.4783

[17] SENANI, R., A. K. SINGH, A. GUPTA and D. R. BHASKAR. Simple Simulated Inductor, Low-Pass/Band-Pass Filter and Sinusoidal Oscillator Using OTRA. Circuits and Systems. 2016, vol. 7, no. 3, pp. 83–99. ISSN 2153-1293. DOI: 10.4236/cs.2016.73009

[18] CHEN, J.-J., H.-W. TSAO, S.-I. LIU and W. CHIU. Parasitic-capacitance-insensitive current-mode filters using operational transresistance amplifier. IEE Proceedings - Circuits, Devices and Systems. 1995, vol. 142, iss. 3, pp. 186–192. ISSN 1350-2409. DOI: 10.1049/ip-cds:19951950

[19] SINGH, A. K., R. SENANI and A. GUPTA. OTRA, its implementations and applications: a state-of-the-art review. Analog Integrated Circuits and Signal Processing. 2018, vol. 97, iss. 2, pp. 281–311. ISSN 1573-1979. DOI: 10.1007/s10470-018-1311-3

[20] D’AZZO, J. J. and C. H. HOUPPIS. Linear Control System: Analysis and Design. 4th ed. New York: McGraw-Hill, 1995. ISBN 0-07-113295-3.

[21] PANDEY, N. and R. PANDEY. Approach for third order quadrature oscillator realization. IET Circuits, Devices & Systems. 2015, vol. 9, iss. 3, pp. 161–171. ISSN 1751-858X. DOI: 10.1049/iet-cds.2014.0170

[22] LAWANWISUT, S. and M. SIRIPRUCHYANUN. High Output-impedance Current-mode Third-Order Quadrature Oscillator Based on CCCCTAs. In: IEEE Region 10 International Conference (TENCON). Singapore: IEEE, 2009, pp. 1–4. ISBN 978-1-4244-4546-2. DOI: 10.1109/TENCON.2009.5395691

[23] WU, C.-Y., T.-C. YU and S.-S. CHANG. New Monolithic Switched-Capacitor Differentiators with Good Noise Rejection. IEEE Journal of Solid-State Circuits. 1989, vol. 24, iss. 1, pp. 177–180. ISSN 1558-173X. DOI: 10.1109/JSSC.1989.192531

[24] ALDEA, C., S. CELMA and A. OTIN. Low-Voltage Differentiator for VHF Filtering. Analog Integrated Circuits Signal Process. 2002, vol. 33, iss. 2, pp. 107–116. ISSN 1573-1979. DOI: 10.1023/A:1012107813469
[26] PALUMBO, G. and S. PENNISI. Filter Circuits Synthesis with CFOA-Based Differentiators. In: Instrumentation and Measurement Technology Conference (IMTC). Venice: IEEE, 1999, pp. 546–550. ISBN 0-7803-5276-9. DOI: 10.1109/IMTC.1999.776811.

[27] WU, C.-Y., Y. CHENG and J. GONG. The new CMOS 2 V low-power IF fully differential Rm-C bandpass amplifier for RF wireless receivers. In: IEEE International Symposium on Circuits and Systems (ISCAS). Geneva: IEEE, 2000, pp. 633–636. ISBN 0-7803-5482-6. DOI: 10.1109/ISCAS.2000.856408.

[28] LIU, S.-I., J.-H. KUO, H.-W. TSAO, J. WU and J.-H. TSAY. New CCII-based differentiator and its applications. International Journal of Electronics. 1991, vol. 71, iss. 4, pp. 645–652. ISSN 1362-3060. DOI: 10.1080/00207219108925507.

[29] KERWIN, W. J., L. P. HUELSMAN and R. W. NEWCOMB. State-Variable Synthesis forInsensitive Integrated Circuit Transfer Functions. IEEE Journal of Solid-State Circuits. 1967, vol. 2, iss. 3, pp. 87-92. ISSN 1558-173X. DOI: 10.1109/JSSC.1967.1049798.

[30] IBRAHIM, M. A., S. MINAEI and H. KUNT-MAN. A 22.5 MHz current-mode KHN-biquad using differential voltage current conveyors and grounded passive elements. AEU - International Journal of Electronics and Communications. 2005, vol. 59, iss. 5, pp. 311–318. ISSN 1434-8411. DOI: 10.1016/j.aeue.2008.08.003.

[31] SENANI, R., V. K. SINGH, A. K. SINGH and D. R. BHASKAR. Tunable Current-Mode Universal Biquads employing only three MOCCs and all grounded passive elements: Additional New Realizations. Frequenz. 2005, vol. 59, iss. 9–10, pp. 220–224. ISSN 2191-6349. DOI: 10.1515/FREQ.2003.57.7-8.160.

[32] SINGH, V. K., A. K. SINGH, D. R. BHASKAR and R. SENANI. New Universal Biquads Employing CFOAs. IEEE Transactions on Circuits and Systems II: Express Briefs. 2006, vol. 53, iss. 11, pp. 1299–1303. ISSN 1558-3791. DOI: 10.1109/TCSII.2006.882345.

[33] BIOLEK, D. and V. BIOĽKOVA. Universal biquads using CDTA elements for cascade filter design. In: Proceedings of the 7th International Multiconference CSCC 2003. Corfu: WSEAS, 2003. pp. 1–5. ISBN 960-8052-88-2.

[34] KAFRAWY, A. K. and A. M SOLIMAN. A modified CMOS differential operational transresistance amplifier (OTRA). AEU - International Journal of Electronics and Communications. 2009, vol. 63, iss. 12, pp. 1067–1071. ISSN 1434-8411. DOI: 10.1016/j.aeue.2008.08.003.

About Authors

Neeta PANDEY is currently a Professor in Department of Electronics and Communication Engineering, Delhi Technological University. She did her M.E. in Microelectronics from Birla Institute of Technology and Sciences, Pilani and Ph.D. from Guru Gobind Singh Indraprastha University Delhi. She is a life member of ISTE, and Senior Member of IEEE, USA. Her research interests are in Analog and Digital VLSI Design.

Rajeshwari PANDEY is currently a Professor in Department of Electronics and Communication Engineering, Delhi Technological University. She did her M.E. in Electronics and Control from BITS, Pilani, Rajasthan, India and Ph.D. from Faculty of Technology, Delhi University, India. She is a life member of IETE, ISTE and member of IEEE, and IEEE WIE for over 12 years. Her research interests include Analog Integrated Circuits, and Microelectronics.

Rashika ANURAG is currently working as an Associate Professor in Department of Electronics and Communication Engineering, JSSATE, Noida, India. She did her M.E. (Electronics and Control) from BITS, Pilani, Rajasthan, India and Ph.D. from Banasthali University, Banasthali, India. Her research interests include Analog Integrated Circuits, and Microelectronics.

Ritu VIJAY is currently working as an Associate Professor in the Department of Electronics, Banasthali University. She received her B.Sc. (Electronics), M.Sc. (Electronics) and Ph.D. degree from Banasthali University, Banasthali. She has more than fifteen years of teaching experience and has published number of papers in reputed journals. Her research interests include signal processing and image processing.