Design of fast pulse generator for Kicker power supply in HIAF*

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Abstract. Kicker power supply is one of the key components in the injection and extraction system of HIAF (High Intensity Heavy Ion Accelerator Facility, the 12th five-year national big science project). The PFN-Marx generator technology based on solid-state IGBT switch will be applied to HIAF-Kicker power supply. Hundreds of fast pulse signals are required to control these IGBTs. The PFN-Marx generator has many requirements for these control signals, such as adjustable pulse-widths and time-delay. The maximum value of adjustment accuracy of the pulse-widths and delay among multiple control signals need to be 10ns. In this paper, a fast pulse generator circuit based on an emerging ARM-embedded FPGA have been designed for HIAF-Kicker power supply. The test results show that the output performance of the fast pulse generator circuit meets the requirements of the PFN-Marx generator.

1. Introduction
The High Intensity Heavy Ion Accelerator Facility (HIAF) is a new accelerator facility under construction at the Institute of Modern Physics (IMP), Chinese Academy of Sciences [1]. The Kicker power supply is one of the key devices that provides excitation current for the pulsed magnet in the injection and extraction system of HIAF. A solid-state PFN-Marx generator-based technology will be adopted for the HIAF-Kicker power supplies, and IGBTs are used for the discharge switch. Since the limited withstand voltage and current capability of a single solid-state IGBT switch, the quantity of IGBTs in solid-state PFN-Marx generator is very large. The synchronization of multi-channel IGBTs directly affects the output performance of HIAF-Kicker.

The solid-state PFN-Marx generator could break down severely when the synchronization for driving signals is more than 10ns [2]. Screening devices and optimizing circuit layout were usually used to improve synchronization. However, this is a time-consuming and painstaking job and the synchronization of switches cannot be adjusted accurately online while the power supply is operating. The rising time of IGBT driving signals of HIAF-Kicker is about 200 ns, so a fast pulse generator with 10ns adjustment step was designed to produce precise IGBT driving signals. The design based on Cyclone V chip, which integrates FPGA and a dual-core ARM Cortex-A9 MP core processor. In this design, ARM is mainly used to upload and download the control data. The fast pulse generator circuit on FPGA is designed to generate hundreds of fast pulse control signals. For such signals, the time-delay and pulse-widths are adjustable and the adjustment accuracy is 10 ns. The high-accuracy digital control design provide synchronous drive signals for multi-channel IGBTs of PFN-Marx generator, which has a significant advantage over previous adjustment methods.
2. The solid-state PFN-Marx generator on HIAF-Kicker

Compared with PFN (Pulse-Forming Network) and PFL (Pulse-Forming Line), PFN-Marx generator is based on solid-state IGBT switch, which has advantages of smaller size, easy to repair and more flexible to adjust pulse-widths and delay. After the energy storage process has been completed in PFN-Marx circuit, the square wave excitation current can be generated by the solid-state IGBT switch for the magnet load [3].

The work principle of the solid-state PFN-Marx generator is that the charging power supply charges the PFN in parallel through the charging resistor. After the charging process has been completed, the solid-state switches are turned on at the same time. The charging resistor acts as an isolator, and the PFNs in each stage are discharged serially. Each level of PFN modulates the waveform and finally the approximate square wave pulse waveform is obtained on the load. The schematic of the solid-state PFN-Marx generator is shown in Figure 1.

3. The control system structure

The entire control system of HIAF is an Ethernet-based distributed control system. The information such as voltage parameters and pulse-widths need to be quickly sent to Kicker power supply controllers through the Ethernet [4]. In order to make communication easier between the upper control system and the Kicker power supply controllers, we use the Cyclone V SX FPGA, which is integrated with dual-core ARM Cortex-A9 MP Core processor.

The control system structure is showed in Figure 2. In this control structure, the delay and pulse-widths data are sent by the user interface via Ethernet. The ARM stores this information and distributes them to different registers on the FPGA side through the AXI bus bridge. After receiving these data, the fast pulse generator circuit on FPGA generates hundreds of fast pulse control signals. Then we convert these output pulse signals into multi-channel optical signals. These optical signals are transmitted through the optical fiber and then converted into current signals by optical transceiver to the PFN-Marx generator.
4. FPGA-based fast pulse generator

As shown in Figure 3, the programming contents on FPGA include the fast pulse generation module and Avalon bus interface module. The fast pulse generation module contains multiple 16-bit counters. These counters read the delay and pulse-widths data for counting. These data are written in some 32-bit registers on FPGA by ARM through the AXI bus bridge. Among this data the upper 16 bits data represent the delay information and the lower 16 bits data represent the pulse-widths information. After the counting process has been completed the fast pulse generation circuit outputs the fast pulse.

For general external address space access, the CPU requires a user-defined interface control module. The Avalon bus interface module is designed according to the CPU read/write timing. Then the two modules are attached to the AXI bus bridge via the Qsys component. The PLL cores in FPGA are used to multiply the clocks to 100MHz, so that the adjustment accuracy can reaches 10ns.

![Figure 4](image1.png) **Figure 4.** The delay adjustment process of multi-channel driving signals for IGBTs.

![Figure 5](image2.png) **Figure 5.** The pulse-widths adjustment process of multi-channel driving signals for IGBTs.

5. The fast pulse output signals

The design of fast pulse generator was used successfully to driving multi-channel IGBTs of PFN-Marx generator synchronously for HIAF. In this paper, we take three fast output pulses as an example. Figure 4 show the delay adjustment process of each-channel driving signal for IGBTs. The pulse-widths can be adjusted according to the Kicker power supplies’ output waveform as shown in Figure 5. For such signals, the adjustment accuracy is 10 ns. All pulse-widths and delay information are sent through the Ethernet. The synchronization experiment shows that this design can meet the synchronous drive requirements of solid-state PFN-Marx generator for HIAF.

6. Conclusions

In this paper, a fast pulse generation circuit based on an ARM-embedded FPGA structure is designed to generate the accurate IGBT driving signals for PFN-Marx generator of HIAF-Kicker. For such driving signals, the delay and pulse-widths could be adjusted which effectively improve IGBTs’ synchronization of HIAF-Kicker. In this way, the digital driving technology can also improve the stability and synchronization of the injection and extraction system in HIAF. The following work will focus on integrating the fiber interfaces for hundreds of fast pulses into the controller of Kicker power supply systems and giving an optimized fan out scheme to reduce budget.

References

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