Single Inductor Multiple Output Auto-Buck-Boost DC–DC Converter with Error-Driven Randomized Control

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Received: 20 July 2020; Accepted: 17 August 2020; Published: 19 August 2020

Abstract: We propose a single inductor multiple output (SIMO) auto-buck-boost DC–DC converter with error-driven randomized control (EDRC). The conventional controls in a SIMO DC–DC converter supply power to outputs that have been selected in a sequential order. Furthermore, they control the inductor current levels at either edge of a switching period in a steady state to be at the same level to alleviate cross-regulation. However, this limits the flexibility of the converter to respond to changes in load requirements. A sequential selection of light loads results in these loads being selected more often than a load demand, degrading the efficiency for light loads. In addition, limited flexibility leads to delayed responses. This paper introduces an auto-buck-boost topology that selects outputs based on output errors, and instantaneously adjusts the inductor current level. Moreover, we propose a technique for allowing any output to avoid selection when all outputs are fully supplied. The proposed EDRC scheme achieves improvements in efficiency in regards to light loads, cross-regulation, and output driving capability.

Keywords: auto-buck-boost; output error-driven randomized control (EDRC); single-inductor multiple-output (SIMO) DC–DC converters

1. Introduction

Since the early 2000s, researchers have investigated and studied single inductor multiple output (SIMO) DC–DC converters. A SIMO DC–DC converter employs a single inductor (instead of multiple inductors) to convert a DC voltage to multiple DC voltages. Prior to 2005, researchers had proposed SIMO DC–DC converters that regulate only buck outputs or boost outputs [1,2]. In accordance with increasingly diverse power requirements of circuit systems, SIMO DC–DC converters capable of regulating both buck and boost outputs were subsequently proposed [3–5]. The works in [3–5] were designed based on the assumption that the output type for both buck and boost outputs does not change during the operation of the converter. However, in reality, an input voltage variation dependent upon the state of charge (SoC) of a battery affects the output types. The operating modes of the outputs of a SIMO DC–DC converter must change to maintain a constant supply voltage if the SoC of a battery is altered during operation of the converter. The ability to achieve regulation of output voltages through adaptive changes in the operating mode depending on the varying relationship of the input voltage is known as the auto-buck-boost capability [6,7]. In a SIMO DC–DC converter, the outputs of the converter time-share the single inductor of the converter [1–8]. This causes the outputs to become cross-coupled; thus, any abrupt change in an output load will result in changes in all other outputs. This problem is known as the cross-regulation problem [1,2].

Moreover, the limited capacitance of the filtering capacitors connected in shunt to each output limits the current driving capability. Accordingly, there is a need for a design scheme that
enhances performance with regard to both cross-regulation and output-driving capability. Another critical performance indicator regarding SIMO DC–DC converters is the efficiency in light loads. The degradation in efficiency for light loads with low-power outputs is a disadvantage of the SIMO DC–DC converter.

The SIMO converters reported in [1–18], select their respective outputs in a sequential order, and adjust the duty ratio of each of their respective outputs to control the power delivered to the respective outputs, as shown in Figure 1a. In the conventional sequential-order-based output selection scheme, an increase in the duty ratio of a SIMO DC–DC converter output reduces the length of the time duration when the inductor can be energized and de-energized for the other outputs, as the outputs time-share a predetermined time interval, causing cross-regulation.

![Illustrated example waveforms of output voltage of a single inductor multiple output single inductor multiple output (SIMO) converter with three outputs. Control scheme utilizing (a) sequential-order-based output selection [6,7,19,20], and (b) error-based output selection of [14].](image)

In a SIMO DC–DC converter with a discontinuous conduction mode (DCM), to mitigate the cross-regulation arising from the sequential-order-based output selection, the inductor current is energized at a level equal to zero, returned to zero after a power delivery, and maintained at zero until the start of the energizing cycle of the next output [1]. The timing margin of the zero-inductor-current allows the inductor current level at the start of the energizing cycle of the next output to be zero. However, under certain load requirements, this timing margin is not guaranteed. Such load requirements interfere with the initial value of the inductor current at the start of the energizing cycle of the next output. They cause the SIMO DC–DC converter to deviate from the controllable range, causing severe cross-regulation. Accordingly, the output driving capability is limited, and the cross-regulation is not completely resolved. Moreover, the return of the inductor current level to zero after each power delivery causes the inductor current to flow discontinuously, limiting the total supply of output power.

In a SIMO DC–DC converter with a pseudo-continuous conduction mode (PCCM), the inductor current is energized at a level greater than zero, and returned to the level after a power delivery. The level is then maintained until the start of the energizing cycle of the next output [2]. Continuous conduction of the inductor current improves the current driving capability, more so than in the case of a SIMO DC–DC converter with a DCM. In a PCCM scheme, to maintain the inductor current at a constant level, it is mandatory to have a freewheeling technique for circulating the inductor current, shunting the freewheeling cycle. Consequently, in any given time slot, it is necessary to include an additional cycle for shunting the inductor, and the implementation thereof increases the circuit
complexity. Moreover, as in the case of the DCM scheme, under specific load requirements, the related timing margin is not guaranteed. In such cases, severe cross-regulation will occur.

In a control scheme with sequential-order-based output selection, there is a topological disadvantage with regard to efficiency in light loads: in any given time-slot, an output must be selected, regardless of the load–current demand. If an output without a load demand is sequentially selected, it may cause an unwanted output ripple voltage, and a degradation of power efficiency. To alleviate the degradation of efficiency with light loads, the error-based control (EBC) proposed in [14] prioritizes outputs based on output errors, and instantaneously selects output with the maximum output error according to the priority of the output selection, as shown in Figure 1b. Such error-based output selection allows light loads to be selected less often than heavy loads. The EBC adopts a hybrid architecture comprising of a switching converter and an add-on linear regulator to mitigate cross-regulation. The linear regulator instantaneously provides current to any of the output channels requiring additional current because of variations in the load requirements. However, in a SIMO converter with error-based output selection, the topology only regulates buck outputs. Moreover, its design has not been fully investigated in regards to whether it can collectively improve the cross-regulation, efficiency with light loads, and output driving capability.

In this study, we propose a SIMO auto-buck-boost DC–DC converter with error-driven randomized control (EDRC). In the proposed SIMO converter, we use an error-based output selection, which is an extended version of the auto-buck-boost topology. Additionally, we introduce a control scheme for instantaneously adjusting the inductor current level according to the load requirement to lessen cross-regulation, without the need of an additional current supply such as an add-on linear regulator.

This paper is organized as follows. Section 2 presents the control method and architecture behind the EDRC scheme of the proposed converter. Section 3 presents the MATLAB simulation results. Section 4 shows experimental results based on implementing the proposed converter with three buck-boost outputs with discrete components. Section 5 presents a discussion of the proposed converter. Finally, we concluded this work in Section 6.

Figure 2. Power stage of a single inductor buck-boost DC–DC converter and switching control modes of inductor current paths.
2. Proposed SIMO Architecture and Control Scheme

In this section, we introduced the operational principle, condition setting of the deep boost, and architecture of the proposed SIMO auto-buck-boost DC–DC converter with EDRC.

2.1. Error-driven Randomized Control (EDRC) for Auto Buck-Boost SIMO Converter

We used the power stage shown in Figure 2, which is from a non-inverting buck-boost DC–DC converter in the proposed converter, which is capable of simultaneously regulating buck and boost outputs.

Figure 3a,b illustrates inductor current waveforms of two operation modes, inductor power switching mode A (IPSM_A) and inductor power switching mode B (IPSM_B), respectively. IPSM_A mode charges energy in inductor with the energizing phase \( (T_E) \) and delivers the energy to one of the outputs with the de-energizing phase \( (T_D) \), while IPSM_B delivers energy to an output with the bypassing phase \( (T_B) \). If outputs within the range of a typical buck \( (V_O < V_g \text{ or } V_O \ll V_g) \) or mild boost type \( (V_O > V_g) \) are operated in IPSM_A and outputs within the range of the deep boost type \( (V_O >> V_g) \) are operated in IPSM_B, then the converter can support auto-buck-boost as in the control scheme in [19], assuming that regulation is achieved.

We denote the duty of IPSM_A as \( D_A \), and the duty of IPSM_B as \( D_B \). If we set \( D_A \) to always be wider than \( D_B \), then the transition of the operation mode from IPSM_A to IPSM_B for any output can increase the charge supplied to that output, without affecting the size of the time intervals for the next outputs. The relation of \( D_A \) and \( D_B \) can be expressed as follows:

\[
D_A = D_B + \beta
\]  

(1)

Here, \( \beta \) is the difference in duty between the two modes and positive. Next, the relationships of the charges supplied to any output of IPSM_A and IPSM_B can be approximated as follows:

\[
Q_B \approx Q_A + T_S \cdot \beta \cdot I_i
\]  

(2)

Here, \( I_i \) is the inductor current level at the start of an energizing phase. The derivation of Equation (2) is explained in Appendix A. Thus, the transition of the mode from IPSM_A to IPSM_B for...
any output can increase the charge supplied to that output by $T_S \cdot \beta \cdot I_L$, and the increase in the duration of power delivery for the output does not reduce the size of the time intervals for the next output. In this study, we utilized the operation modes IPSM_A and IPSM_B with the adoption of $\beta$, to adjust the inductor current level and amount of charge supplied to the outputs.

The duty ratios of both modes ($D_A$ and $D_B$) were controlled so that the sum of the output errors becomes zero, as in the case of the EBC scheme of [14]. We set the duty difference $\beta$ of the two operation modes to a constant value for simplicity. For a mode transition from IPSM_A to IPSM_B to raise the inductor current, the condition of $\Delta I_{LA} < \Delta I_{LB}$ should be satisfied. The condition is expressed as follows:

$$\Delta I_{LB} - \Delta I_{LA} = \left( -\frac{V_O}{L} \cdot \beta + \frac{V_g}{L} - \frac{V_g}{L} \cdot D_A \right) \cdot T_S > 0 \quad (3)$$

Here, we set the value of $\beta$ to satisfy the condition in Equation (3).

Figure 4a–c shows the waveforms of the proposed EDRC scheme under a steady state, positive step change, and negative step change, respectively, where we presumed that output 1 is of the deep boost type. At the preceding edge of each switching period, the output errors were sampled. The output having the maximum output error was selected based on a comparison of the output errors; the output error was the voltage level resulting from subtracting the output voltage from the reference voltage. We denoted the output error as $V_{error}$.

In Figure 4a, we presumed that load requirement in output 2 is the lowest among all outputs; therefore, the slope of $V_{error_2}$ is the lowest among all outputs while increasing. This makes output 2 the least selected. The error-based output selection also flexibly controls the frequency of selection of the outputs. In Figure 4b, the rise in the load requirement in output 2 at $t_1$ increased the slope of $V_{error}$. It increased the frequency of the selection of output 2. In Figure 4c, the decline in the load requirement in output 2 at $t_4$ decreased the frequency of selection of output 2. This flexible error-based output selection helped to mitigate load regulation.

The control circuit assigns the operation mode to the selected output at the preceding edge of the switching period. In the following, we will explain the criteria for assigning the operation modes.

The proposed converter should raise the inductor current level or widen the power delivery duration in response to a rise in the load requirement. A rise in the load requirement results in an increase in the sum of the output errors. Therefore, the proposed converter monitors the sum of the output errors to detect variations in the load requirement. We denoted the sum of the output errors by $V_{error_sum}$. We adopted two reference voltage levels, $V_{ref+}$ and $V_{ref-}$, for detecting the increase or decrease in $V_{error_sum}$. The reference voltage levels, $V_{ref+}$ and $V_{ref-}$, are voltage levels of the same magnitude but different signs, as shown in Figure 4. $V_{error_sum}$ was sampled at the preceding edge of the switching period, and the control circuit assigns an operation mode based on a comparison of $V_{error_sum}$ with $V_{ref+}$ and $V_{ref-}$.

If the sampled $V_{error_sum}$ is sensed to be smaller than $V_{ref+}$ but greater than $V_{ref-}$, that is $V_{ref+} > V_{error_sum} > V_{ref-}$, then the average inductor current level should be maintained. The control circuit assigns IPSM_A to an output within the range of the typical buck type ($V_O < V_g$ or $V_O \ll V_g$) or mild boost type ($V_O > V_g$). The combination of $T_E$ and $T_D$ in IPSM_A allows for auto-buck-boost regulation to be achieved [24]. The control circuit assigns IPSM_B to an output within the range of the deep boost type ($V_O \gg V_g$), as in [19]. We will cover the criteria for determining the range of the deep boost type in the next section. In Figure 4a, all sampled $V_{error_sum}$ values were sensed to be $V_{ref+} > V_{error_sum} > V_{ref-}$. Therefore, outputs 2 and 3 were operated in IPSM_A, and output 1 was operated in IPSM_B.

Provided that the sampled $V_{error_sum}$ was greater than $V_{error_sum} > V_{error_sum}$, i.e., $V_{error_sum}$ > $V_{error_sum}$, the control circuit assigned IPSM_B, to increase both the inductor current level and power delivery duration. In Figure 4b, the rise in the load requirement in output 2 at $t_1$ increased the slope of $V_{error_sum}$, raising the sampled $V_{error_sum}$ above $V_{error_sum}$ between $t_2$ and $t_3$. Accordingly, all selected outputs were operated in IPSM_B between $t_2$ and $t_3$ as indicated by the N2 mark, whereas
IPSM_B (indicated by the N1 mark) was assigned for supplying the deep boost output. The operation mode of outputs 2 and 3 was switched from IPSM_A to IPSM_B. The mode transition instantaneously increased the inductor current level. In particular, IPSM_B of buck output 3 increased the inductor current level for the entire switching period. This instantaneous adjustment in the inductor current level led to an improvement in the drivable load current and cross-regulation. However, the instantaneously increased inductor current level might cause the output ripple voltage to rise instantly. The simulation and experimental results will show how the output ripple voltage was increased.

**Figure 4.** Illustrated transient waveforms of the proposed EDRC scheme under (a) steady state, (b) a positive step change and (c) a negative step change of load current in output 2. We presume that output 1 is of the deep boost type \( V_O \gg V_g \). The IPSM_B indicated by N1 mark is assigned for supplying the deep boost output, the IPSM_B indicated by N2 is assigned for increasing the inductor current level, and the \( \Phi_{NS} \) indicated by N3 mark is the inductor current freewheeling phase where no output is selected.
If the sampled $V_{\text{error, sum}}$ is sensed to be lower than $V_{\text{ref-}}$, i.e., $V_{\text{error, sum}} < V_{\text{ref-}}$, then the control circuit assigns IPSM$_A$ to decrease both the inductor current level and power delivery duration. In Figure 4c, the decrease in the load requirement of output 2 at $t_5$ reduced the sampled $V_{\text{error, sum}}$ below $V_{\text{ref-}}$ after $t_5$. Thus, all selected outputs were operated in IPSM$_A$ after $t_5$ until the sampled $V_{\text{error, sum}}$ was increased over $V_{\text{ref-}}$. The mode transition from IPSM$_B$ to IPSM$_A$ of output 1 led to a reduction in the inductor current level.

When all outputs are fully supplied, the selection of any output forces that output to be supplied with more load current than it demands, wasting power and increasing the output ripple voltage. Therefore, in such cases, the converter does not select any output. We denoted this technique as “no demand no selection (NDNS). We adopted the reference voltage $V_{\text{ref, NS}}$ for determining whether all outputs are sufficiently supplied, as shown in Figure 4c. If the control circuit senses that all sampled output errors at the preceding edge of a switching period are lower than $V_{\text{ref, NS}}$, then it freewheels the inductor current without selecting outputs, as indicated by the N3 mark.

2.2. Condition Setting of Deep Boost

We set the range of the deep boost based on a comparison of the input voltage and scaled-down output voltage, as follows:

$$V_g < \alpha \cdot V_O$$

where $\alpha$ is a constant scalar factor. We will provide a guideline for choosing $\alpha$ in this section. If $V_g$ increases from below $\alpha \cdot V_O$ to above $\alpha \cdot V_O$, then the operation mode of the output is switched from IPSM$_B$ to IPSM$_A$, assuming that the sampled $V_{\text{error, sum}}$ is sensed to be between $V_{\text{ref+}}$ and $V_{\text{ref-}}$. However, the inductor current changes of IPSM$_A$ and IPSM$_B$ for one switching period, i.e., $\Delta I_{L_A}$ and $\Delta I_{L_B}$, are different. Consequently, a mode transition may cause a change in the inductor current level, resulting in an overshoot of the output voltages.

Figure 5 shows a simulated average overshoot voltage waveform corresponding to $\alpha$ in the proposed converter, in a case where increasing $V_g$ changes the operation mode of output 2. The constant scalar factor $\alpha$ is mathematically in the range between 0 and 1. When $\alpha$ is 0.5, the boundary level for determining the operation mode, $V_g = \alpha \cdot V_O$, is 1.5 V. In the simulation, 1.5 V of $V_g$ was too small to achieve regulation of the output voltage. Therefore, we simulated the average overshoot voltage by varying $\alpha$ in the range between 0.6 and 1. Within this range, an average overshoot voltage below 60 mV was guaranteed. Thus, a designer can set $\alpha$ to ensure that the average overshoot voltage does not exceed a specified value. We selected $\alpha$ as 0.7, as this value produced the lowest average overshoot voltage for the results in Figure 5.

![Figure 5](image)

**Figure 5.** Simulated average overshoot voltage waveform in terms of $\alpha$ of the proposed EDRC scheme, in the case where increasing $V_g$ changes the operation mode of output 2. The simulation environment is as follows: $V_g = 2$ V, $V_{O1} = 1.5$ V, $V_{O2} = 2.5$ V, and $V_{O3} = 3.3$ V.
2.3. Architecture of the Proposed EDRC

Figure 6 shows a block diagram of the proposed EDRC scheme. The analog subtractor comprises of one op-amp and four resistors, and produces the output error voltage. In the maximum output error selector (MOES) block, comparator circuits compare the output errors with each other, and the MOES block selects the output having the maximum output error. An analog adder (comprising one op-amp and four resistors) aggregates the output error voltages to produce V(error_sum). Comparator circuits compare each output error voltage with V(ref_NS) to sense when all outputs are fully supplied. The EDRC operates in a DCM mode when the inductor current becomes zero during the power delivery duration. The zero current detection block detects when the inductor current becomes zero, and is implemented by adopting the method in [1, 25]. The IPSM block determines the operation mode of the output selected by the MOES block. The truth table for the IPSM block is summarized in Table 1.

![Figure 6. Block diagram of the proposed EDRC. Black lines with an arrow represent an analog signal, and gray lines with an arrow represent a digital signal.](image)

| Conditions Based on Comparison of Magnitude of Inputs | Output |
|------------------------------------------------------|--------|
| V_{ref}^+ > V_{error\_sum} > V_{ref}^-             | V_g > \alpha \cdot V_{O(i)} | 0 (IPSM_A) |
| V_{error\_sum} > V_{ref}^+                          | V_g < \alpha \cdot V_{O(i)} | 1 (IPSM_B) |
| V_{error\_sum} < V_{ref}^-                          | - | 1 (IPSM_B) |
| V_{error\_sum} < V_{ref}^-                          | - | 0 (IPSM_A) |
The combination of $T_E$ and $T_D$ allows for the control-to-output transfer function of IPSM$_A$ to have a right half plane (RHP) zero [26–29]. The RHP zero causes a phase lag, and results in the phase margin being negative [26–29]. To make the phase margin positive, multiple works in [29,30] employed a Type III compensation network. Therefore, we employed a Type III compensation network to compensate for $V_{\text{error}_\text{sum}}$ as well, as shown in the duty timing controller (DTC) block.

In the DTC block, the comparator circuit produced a pulse width modulation (PWM) signal for IPSM$_A$, based on receiving the compensated $V_{\text{error}_\text{sum}}$ and ramp signal $V_{\text{ramp}A}$. Likewise, another comparator circuit produced a PWM signal for IPSM$_B$, based on receiving the compensated $V_{\text{error}_\text{sum}}$ and ramp signal $V_{\text{ramp}B}$ (which was delayed by $\beta \cdot T_S$ as compared to $V_{\text{ramp}A}$). The mux block selected one of two PWM signals for receiving the output signal of the IPSM block.

The control logic and gate driver block stored the inputs at the rising edge of CLK; the CLK signal is a clock signal whose period is $T_S$. The rising edge of the CLK signal and the falling edge of $V_{\text{ramp}A}$ were synchronized.

3. Simulation Results

In this section, we used MATLAB to simulate a version of the proposed converter with three outputs, to verify its effectiveness. The simulation environment includes $V_g = 2 \text{ V}$, $V_{\text{out}1} = 3.3 \text{ V}$, $V_{\text{out}2} = 2.5 \text{ V}$, $V_{\text{out}3} = 1.5 \text{ V}$, $f_S = 781 \text{ kHz}$, $L = 5.8 \mu\text{H}$, $C_{\text{out}1} = C_{\text{out}2} = C_{\text{out}3} = 10 \mu\text{F}$, $\alpha = 0.7$, and $\beta = 0.19$.

Figure 7 shows simulated waveforms of the output voltages of the proposed EDRC scheme, in a case where the sampled $V_{\text{error}_\text{sum}}$ was sensed to be within $V_{\text{ref}+} > V_{\text{error}_\text{sum}} > V_{\text{ref}-}$. The outputs were randomly selected. Output 3 was operated in IPSM$_B$ and outputs 1 and 2 were operated in IPSM$_A$, according to a comparison of $V_g$ with $\alpha \cdot V_O$. The pulse width in $S_{O3}$ was wider than those of the remaining outputs; this determined the operation modes of the outputs. The load current of output 3 was 330 mA, i.e., the largest among all outputs. Therefore, output 3 seems to be the most frequently selected. However, the wider power delivery duration of IPSM$_B$ allowed for more power to be received in one switching period than in the cases of outputs 1 and 2. Therefore, output 3 was the least selected output from among all outputs, even though output 3 had the largest load current among all outputs.

Figure 8a,b shows the simulated transient waveforms of the proposed EDRC scheme, where we measured the maximum driving current, load regulation, and cross-regulation. We compared the measurements with the performances measured in the SIMO auto-buck-boost DC–DC converter of [19], based on the PCCM scheme. Figure 8c shows the simulated transient waveforms of the proposed EDRC scheme, but without the NDNS technique. We show the effectiveness of the NDNS technique through a comparison of Figure 8b,c.

In Figure 8a, 0.372 mV/mA and 0.012 mV/mA were the simulated values of load regulation and cross-regulation in response to a driving current of 250 mA, respectively. In Figure 8b, 0.18 mV/mA and 0.01 mV/mA were the simulated values of load regulation and cross-regulation, respectively. The work in [19] achieves 2 mV/mA and 0.67 mV/mA of load regulation and cross-regulation in response to a maximum driving current of 110 mA, respectively. In reality, the load requirement varies, in units of mA/ms. To show the change in the inductor current level and increase in the output ripple voltage, Figure 8 shows the results of simulating extreme cases, in which an increase or decrease in a load current of 250 mA occurred in 1 ns. Nevertheless, the performances of the load regulation, cross-regulation, and maximum driving current as simulated in Figure 8 are improved over those in [19].

The proposed EDRC scheme instantaneously adjusted the inductor current level in response to a change in the load requirement. In Figure 8a, it allowed the inductor current to rise from 0.97 A to 1.3 A with only five cycles, in response to an increase in load current of 250 mA. The instantaneous adjustment of the inductor current level by the proposed EDRC scheme led to improvements in the performances of the load regulation, cross-regulation, and output driving capability.
within the proposed EDRC scheme, and show the guaranteed maximum increase in the output ripple voltage. The selection of an output that does not require a load current among all outputs.

In Figure 8, the load and cross-regulations were measured at 0.46 mV/mA and 0.164 mV/mA, respectively. The proposed EDRC scheme without the NDNS technique achieved worse performances in regards to load regulation and cross-regulation than those in Figure 8, although it achieves better performances than those of [19]. The selection of an output that does not require a load current increased the output ripple voltage (as shown by the boxes with the dashed lines), thereby aggravating load regulation and cross-regulation.

The instantaneous adjustment in the inductor current level can abruptly increase the output ripple voltage. We assumed a worst-case scenario where the output ripple voltage increases in the proposed EDRC scheme, and show the guaranteed maximum increase in the output ripple voltage from the simulation. The worst-case scenario is that the average inductor current level is elevated, and the operation mode is switched from IPSM_A to IPSM_B. We modeled the increase in the output ripple voltage of the scenario in Appendix A, as expressed in Equation (A5). We plotted Equation (A5) regarding D_A in Figure 9. Figure 9 shows that the increase in output ripple voltage was guaranteed to be less than 65 mV.

Figure 10 shows the waveforms of the output voltages and inductor current where V_g was increased from 1.7 to 3.4 V and decreased from 1.7 to 3.4 V at a slope of 0.4 V/ms. The sections of the graph in Figure 10a that are marked by “(b)”, “(c)”, “(d)”, and “(e)” (4 ìs in width) were enlarged in Figure 10b–e, respectively. In these sections, the sampled V_error_sum was sensed to be within V_{ref+} > V_{error_sum} > V_{ref–}. In Figure 10b, the outputs 3, 2, and 1 operated in IPSM_B, IPSM_B, and IPSM_A, respectively, depending on the relationship between V_g and V_{OL}. Likewise, in Figure 10c, the outputs 3, 2, and 1 operated in IPSM_B, IPSM_A, and IPSM_A, respectively, and in Figure 10d,e all outputs operated in IPSM_A. The proposed EDRC scheme maintained constant output voltages by switching the operation mode seamlessly, according to the variation of V_g.
Figure 8. Simulated transient waveforms of the proposed EDRC (a) under a positive step change of load current in output 2 from 10 to 260 mA and (b) under a negative step change of load current in output 2 from 260 to 10 mA. (c) Simulated transient waveforms of the EDRC without adopting the no demand no selection (NDNS) technique under a negative step change of load current in output 2 from 260 to 10 mA. The dashed boxes show when power supply exceeded demand.
Figure 9. Simulated waveforms of the increase in output ripple voltage in terms of $D_A$ when the average inductor current level rises. The simulation is performed based on Equation (A5). The load current is (a) 100 mA, (b) 330 mA, and (c) increased from 50 to 330 mA.

Figure 10. (a) Simulated transient waveforms of output voltage of each node and inductor current while $V_g$ increases from 1.4 to 3.4 V and decreases from 3.4 to 1.4 V. In order to display details of transient signals, Figure from (b) to (e) show enlarged parts marked by (b)–(e) in Figure 10 (a).
4. Experimental Results

We implemented the power stage of the proposed converter and analog part of the control circuit with discrete components, and the digital part of the control circuit with field-programmable gate arrays. Figure 11 shows the photography of the implemented converter on the PCB board. The specifications and component values for the proposed converter are summarized in Table 2. Figure 12 shows the measured waveforms of the output voltages and gate-drive signal on switch $S_E$ in a case where the sampled $V_{\text{error_sum}}$ was sensed to be between $V_{\text{ref+}}$ and $V_{\text{ref-}}$. The output voltage of each output rose, in random order. Outputs 3, 2, and 1 operated in IPSM$_B$, IPSM$_A$, and IPSM$_A$, respectively, depending on the relationship between $V_g$ and $V_{Oi} \cdot \alpha$. The operation mode of each output can be confirmed by the pulse width of the gate-drive signal applied to switch $S_E$. In the waveform of the gate-drive signal, two types of pulse widths are shown, “wider width” and “narrower width”. The “wider width” pulse represents IPSM$_A$, and the “narrower width” pulse represents IPSM$_B$. This waveform also shows that one of the output voltages increased randomly while the duty was low in the steady state.

![Figure 11. Fabricated SIMO auto-buck-boost DC–DC converter. It is implemented with discrete components on PCB board. In the PCB, there are 5 outputs, but only 3 outputs were used in the experiments.](image)

![Figure 12. Measured waveforms of output voltages and gate-drive signal on switch $S_E$ while the sampled is sensed to be between $V_{\text{ref+}}$ and $V_{\text{ref-}}$.](image)

| Specification                          | Value                   |
|----------------------------------------|-------------------------|
| Number of Channels                     | 3                       |
| $V_g$                                  | 1-3.5 V (2 V nominal)   |
| Vout1, Vout2, and Vout3                | 1.5 V, 2.5 V, 3.3 V     |
| Switching frequency                    | 195 kHz                 |
| L(DCR)                                 | 5.8 $\mu$H (5 m$\Omega$) |
| Cout1, Cout2, and Cout3(ESR)           | 39 $\mu$F (15 m$\Omega$) |
| $\alpha$                               | 0.7                     |
| $\beta$                                | 19%                     |

Figure 13 shows the measured transient waveforms. In Figure 13a,b, the load current of output 3 was changed from 33 to 220 mA and from 220 to 33 mA, respectively, where the load currents in the cases of outputs 2 and 1 were $I_{\text{out2}} = 250$ mA, and $I_{\text{out1}} = 220$ mA, respectively. Figure 13c,d shows the load current change in output 2 from 7 to 284 mA and from 284 to 7 mA, respectively, where $I_{\text{out1}} = 220$ mA, and $I_{\text{out3}} = 150$ mA. Figure 13e, f shows the load current change in output 1 from...
5 to 205 mA and from 205 to 5 mA, respectively, where \( I_{\text{out1}} = 220 \text{ mA} \), and \( I_{\text{out2}} = 250 \text{ mA} \). The load and cross-regulations were measured as 0.27 mV/mA and 0.042 mV/mA, respectively, which were based on the calculation of measurement in Figure 13c.

![Figure 12](image-url)  
Figure 12. Measured waveforms of output voltages and gate-drive signal on switch \( S_E \) while the sampled is sensed to be between and where \( V_s = 2 \text{ V} \), \( I_{\text{out1}} = 100 \text{ mA} \), \( I_{\text{out2}} = 104 \text{ mA} \), and \( I_{\text{out3}} = 53 \text{ mA} \).

![Figure 13](image-url)  
Figure 13. Measured transient waveforms of outputs, when one of output load–current changes abruptly, for all cases supply voltage \( V_s \) is 2 V. For each figure, the out load current changed as indicated. Load current of output 3 was changed from 33 to 220 mA (a), from 220 to 33 mA (b). The load current of output 2 changes from 7 to 284 mA (c), and from 284 to 7 mA (d). For Figure (e) and Figure (f), load current of output 1 changes from 5 to 205 mA (e), and from 205 to 5 mA (f), respectively.
In Figure 13c, the output ripple voltages of outputs 1, 2, and 3 increased from 55 to 76 mV, from 42 to 102 mV, and from 53 to 70 mV, respectively, after the occurrence of the transient load. At 0.1 W of total output power, 85.5% efficiency was achieved. At 1.28 W of the total output power, the maximum efficiency of 91.2% was achieved, as shown in Figure 14. To confirm the improvement in efficiency when employing the NDNS technique, we also measured the efficiency when not employing the NDNS technique, as shown by the dashed line in Figure 14. The adoption of the NDNS technique achieved an improvement in efficiency of 1.3% at 0.1 W.

![Figure 14](image.png)

**Figure 14.** Solid line is the measured efficiency of the proposed EDRC scheme versus total output power. Dashed line is measured efficiency without adopting the NDNS technique.

### 5. Discussions

The operation of the proposed converter was verified in the simulation and experimental results sections. In this section, we discussed the performance improvements and techniques that lead to the advantages over the techniques in previous articles. Table 3 compares the performances between the previous and proposed works. In the simulation results, we described the structural advantage of the proposed instantaneous adjustment of the inductor current level in regards to the output driving capability, load regulation, and cross-regulation. The proposed converter achieved 0.042 mV/mA of cross-regulation and 0.27 mV/mA of load regulation in response to a change in load current of 277 mA. Table 3 shows the performance improvements compared to those of the previous works, except for the load regulation of the EBC control in [14].

| Ref [14] | Ref [18] | Ref [19] | Ref [20] | Present Work |
|----------|----------|----------|----------|--------------|
| Published Year | 2015 | 2016 | 2016 | 2020 | - |
| Implementation | Discrete component | 0.35 µm CMOS | 0.35 µm CMOS | 0.35 µm CMOS | Discrete component |
| Input voltage (V) | 4.8 | 5 | 1.85-2.9 | 2.5 | 1.7-3.4 |
| Number of outputs | 2 | 10 | 4 | 4 | 3 |
| Output voltages (V) | 3.3, 1.2 | 3.3 (3), 2.8 (2), 2.5 (2), 1.8 (3) | 3.3, 3, 2.5, 1.8 | 3.4, 3, 2.5, 1.8 | 3.3, 2.5, 1.5 |
| Switching frequency (MHz) | 0.1 | 0.17 | 0.25 | 0.75-1 | 0.195 |
| Peak efficiency (%) | 78 | 88.7 | 89 | 89.5 | 91.2 |
| Light-load efficiency | 77@0.11 W | 83.5@0.14 W | 7%@0.2 W | 83%@0.15W | 85.5%@0.1 W |
| Auto-buck-boost | No | No | Yes | YES | Yes |
| Output driving capability (mA) | 100 | 185 | 110 | 300 | 277 |
| Load-regulation (mV/mA) | 1 | 0.17 | 2 | 0.56 | 0.27 |
| Cross-regulation (mV/mA) | 0.5 | 0.1 | 0.67 | 0.05 | 0.042 |

The EBC control selects outputs based on output errors to improve efficiency in light loads, and employs an add-on linear regulator to alleviate cross-regulation. We introduced a technique
for mitigating cross-regulation by adjusting the inductor current level without a linear regulator, and extend the output selection technique based on output errors to an auto-buck-boost topology.

We introduced the NDNS technique. As shown in Figure 8c in the three dashed-line boxes, the power of 0.45 W was over-supplied. The NDNS technique can save the wasted power. Figure 14 shows that the NDNS technique resulted in an increase of efficiency. An efficiency of 85.5% in the case of the proposed converter was achieved at 0.1 W of the total output power, an improvement over the previous works.

In addition, in our simulation results, we have shown how the NDNS technique could improve performances in the cross-regulation, load regulation, and output ripple voltage. However, an instantaneous adjustment in the inductor current level may cause an abrupt increase in the output ripple voltage. We modeled the increase in the output ripple voltage of the proposed converter in the simulation section. The simulation results show that the increase in output ripple voltage was guaranteed to be less than 65 mV. An increase in the switching frequency can reduce the increase in the output ripple voltage.

To reduce the average inductor current level, the work in [20] allows for the operation modes of outputs within the range of typical buck or mild boost types to include a bypassing cycle. In our scheme, it would be possible to lower the average inductor current level if IPSM_A were to include a bypassing cycle. However, we allowed IPSM_A to consist of only energizing and de-energizing cycles, to reduce the circuit complexity and to instantaneously adjust the inductor current level.

We employed filtering capacitors with a capacitance larger than that of the quoted previous publications in Table 3, as the discrete components used in this study limited the speed of the converter. However, we expected that on-chip fabrication of the proposed converter would increase the switching frequency, and thereby enable the use of 10 µF capacitors. The operation of the proposed converter with 10 µF filtering capacitors was verified through simulation.

6. Conclusions

In this study, we proposed a SIMO auto-buck-boost DC–DC converter with error-driving randomized control. We extended an output selection technique based on output errors to an auto-buck-boost topology, and introduced a technique for instantaneously adjusting the inductor current level. In addition, we introduced the NDNS technique, which does not select any output when the loads are sufficiently supplied. The proposed EDRC scheme achieves performance improvements in efficiency in regards to light loads, cross-regulation, and output driving capability in SIMO auto-buck-boost DC–DC converters.

Author Contributions: H.P. implemented the methodology as well as validating the proposed method and results. S.K. supervised the overall research. All authors have read and agreed to the published version of the manuscript.

Funding: This research was supported by the MSIT (Ministry of Science and ICT), Korea, under the “ICT Consilience Creative Program” (IITP-2019-2017-0-01015) supervised by the IITP (Institute for Information & Communications Technology Planning & Evaluation).

Acknowledgments: The authors performed this work as a part of research projects under the Yonsei Global Talent Fostering Program supported by SK Hynix.

Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

In the Appendix A, we derived Equation (A2) and the equation for the increase in the output ripple voltage of the worst-case scenario in the proposed EDRC, which was employed to plot the waveforms in Figure 9. The amounts of charge supplied to the output of operation mode IPSM_A and
the output of operation mode IPSM\(_B\) are driven by Equations (A1) and (A2), respectively, where \(I_i\) denotes the initial value of the inductor current.

\[
Q_A = D_A' \cdot T_S \cdot \left( I_i + \frac{V_g}{L} \cdot D_A \cdot T_S - \frac{V_o}{2L} \cdot D_A' \cdot T_S \right) \tag{A1}
\]

\[
Q_B = Q_A + T_S \cdot \beta \cdot I_i + T_S^2 \cdot \left( \frac{V_g}{L} \cdot D_A \cdot \beta - \frac{V_o}{2L} \cdot D_A' \cdot \beta + \left( \frac{D_A' + \beta}{2L} \right) \cdot \left( V_g \cdot D_A' - V_o \cdot \beta - V_g \cdot \beta \right) \right) \tag{A2}
\]

In Equation (A2), the \(T_S^2\) term is negligible as compared with the remaining terms. Therefore, Equation (A2) is approximated by Equation (A2).

Figure A1 illustrates a worst-case scenario of an increase in the output ripple voltage. In this scenario, the operation mode is changed from IPSM\(_A\) to IPSM\(_B\), and the average inductor current level is increased from \(I_{\text{L,avr(m)}}\) to \(I_{\text{L,avr(n)}}\), where \(I_{\text{L,avr}}\) is the average inductor current level, \(m\) is the time before the output ripple voltage increase, and \(n\) is the time after the output ripple voltage increase. The increases in the output ripple voltages during the power delivery durations of \(t_m\) and \(t_n\) are expressed by Equations (A3) and (A4), respectively.

\[
\Delta V_{\text{O,avr}} = D_A' \cdot T_S \cdot \left( I_{\text{L,avr(m)}} - I_{\text{O(m)}} \right) / C_{\text{out}} \tag{A3}
\]

\[
\Delta V'_{\text{O,avr}} = D_B' \cdot T_S \cdot \left( I_{\text{L,avr(n)}} - I_{\text{O(n)}} \right) / C_{\text{out}} \tag{A4}
\]

The increase in the output ripple voltage is derived by subtracting Equation (A3) from Equation (A4), and is expressed as follows:

\[
\Delta V_{\text{O,avr}} - \Delta V'_{\text{O,avr}} = \left[ D_A' \cdot \left( I_{\text{L,avr(n)}} - I_{\text{L,avr(m)}} \right) - \left( I_{\text{O(n)}} - I_{\text{O(m)}} \right) \right] + \beta \cdot \left( I_{\text{L,avr(n)}} - I_{\text{O(n)}} \right) \cdot T_S / C_{\text{out}} \tag{A5}
\]

**Figure A1.** Illustration of the worst-case scenario of the increase in an output ripple voltage in the proposed EDRC scheme, where the average inductor current level is increased, and the operation mode is changed from IPSM\(_A\) to IPSM\(_B\).

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