A broadband Doherty power amplifier based on the two-port networks method

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Abstract This paper proposes a simple method for designing a broadband Doherty power amplifier. The two-port network is used to represent the output matching networks and load modulation networks. Then, the relationships between the parameters of the two-port network and the output impedances of the transistors and the impedances of the power amplifier branches at the combiner are derived. The output matching network and the load modulation network are designed based on the parameters of the two-port network. A broadband Doherty power amplifier is designed and fabricated to verify the effectiveness of the proposed method. The measured results show that the saturated output power is 43.5~45dBm and the saturated drain efficiency is 65-75% in 2.1-2.7GHz. And the drain efficiency is greater than 40% at the 6dB power back-off in the same frequency band. And the gain is above 12dB.

key words: Doherty power amplifier; Broadband; two-port network; output matching network; load modulation network

Classification: Microwave and millimeter wave devices, circuits, and hardware

1. Introduction

With the development of wireless communication technology, the amount of data transmitted is greatly increasing. Therefore, high peak-to-average modulation signals are often used to improve data transmission capacity [1-5]. Traditional power amplifiers (PAs) often only maintain high efficiency at saturation, and are not suitable for amplifying the high peak-to-average ratio signals [6-10]. Therefore, some PAs like Doherty has become research interest because of the high efficiency at power back-off [11-16]. However, the bandwidth of Doherty PAs is limited by its offset lines [17-20]. Many methods have been reported to expand the bandwidth of the Doherty PAs [21-24]. In [3], a high efficiency Doherty PA which uses the complex combining load with non-infinity peaking impedance is implemented in 1.1~2.4 GHz. A broadband Doherty PA with a 41% fractional bandwidth is presented, in which the post-matching structure and low-order impedance transformation networks are employed to achieve the broadband performance [4]. In [5], a novel broadband Doherty PA based on the continuous-mode technique is proposed, in which 1.1GHz band is obtained. A modified Doherty PA that increases peak power between 1.35GHz and 2.05 GHz is presented by optimizing peak combining current ratio [6]. In [7], a symmetrical Doherty PA with an extended efficiency range is proposed, where network parameters analytical method is utilized to design combiner circuits for larger than 6 dB power back-off with a symmetrical structure. However, combiner networks of the carrier and peaking PAs are integrated design using the method presented in [7], which results in a narrower bandwidth.

In order to solve the above problems, this paper proposes a simple method based on two-port networks for designing broadband Doherty PAs. The traditional output matching networks of the carrier and peaking PAs and the load modulation network is replaced by two-port networks, respectively. Furthermore, the relationships between the parameters of the two-port networks and the output impedances of transistors and the impedance of the PA branches at the combiner are derived. The optimal broadband output matching and load modulation circuits of the carrier and peaking PAs are designed separately based on the parameters of the two-port networks for obtaining a better bandwidth performance. For validation, a broadband Doherty PA is designed and fabricated.

2. Theoretical analysis

The two-port network diagram of output matching and load modulation networks is shown in Fig.1. And the proposed method omits the offset line in the traditional design process, and only uses the two-port network, which can satisfy the impedances of the carrier and peak PA at both the saturation and power back-off. Zc and Zcl represent the input impedance of the network and the output impedance of the network, respectively.
According to the two-port network principle [25], the relationship between output voltage \( V_{cl} \), current \( I_{cl} \) and input voltage \( V_{c} \), current \( I_{c} \) can be expressed by the ABCD matrix as:

\[
\begin{bmatrix} V_{c} \\ V_{cl} \end{bmatrix} = \begin{bmatrix} A & C \\ B & D \end{bmatrix} \begin{bmatrix} I_{c} \\ I_{cl} \end{bmatrix}
\]  

(1)

The A, B, C and D in the ABCD transfer matrix can be calculated by the S parameter as:

\[
A = (S_{12} + \frac{(1+S_{11})(1-S_{22})}{S_{21}}) / 2
\]  

(2)

\[
B = Z_{0} \left( S_{12} - \frac{(1+S_{11})(1+S_{22})}{S_{21}} \right) / 2
\]  

(3)

\[
C = \frac{1}{2Z_{0}} \left( \frac{1-S_{11}(-1-S_{22})}{S_{21}} - S_{12} \right)
\]  

(4)

\[
D = (S_{12} + \frac{(1-S_{11})(1+S_{22})}{S_{21}}) / 2
\]  

(5)

Where \( Z_{0} \) is the output impedance. Assuming that this two-port network is treated as a lossless network structure, its S-matrix [S] can be derived as follows:

\[
\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = 
\begin{bmatrix} S_{11} & \frac{-S_{22}e^{j\theta_{21}}}{\sqrt{1-|S_{22}|^2e^{j\theta_{21}}}} \\ \frac{S_{21}}{\sqrt{1-|S_{22}|^2e^{j\theta_{21}}}} & S_{22} \end{bmatrix}
\]  

(6)

Where \( \theta_{21} \) represents the phase shift of the parameter \( S_{21} \). And the S matrix parameter can be represented by \( S_{22} \) and \( \theta_{21} \). Then Eq. (6) is substituted into Eq. (2), (3), (4) and (5), ABCD matrix can be expressed as follows:

\[
A = \frac{(1+S_{22})(1+S_{22}e^{j2\theta_{21}})+(1-S_{22})e^{j\theta_{21}}}{2\sqrt{1-|S_{22}|^2e^{j\theta_{21}}}}
\]  

(7)

\[
B = \frac{Z_{0}(1+S_{22})(1+S_{22}e^{j2\theta_{21}})-(1-S_{22})e^{j\theta_{21}}}{2\sqrt{1-|S_{22}|^2e^{j\theta_{21}}}}
\]  

(8)

\[
C = \frac{1}{2Z_{0}} \frac{(1-S_{11})(1+S_{22})}{e^{j\theta_{21}}}
\]  

(9)

\[
D = \frac{(1-S_{11})(1-S_{22})e^{j2\theta_{21}}+(1+S_{22})e^{j\theta_{21}}}{2\sqrt{1-|S_{22}|^2e^{j\theta_{21}}}}
\]  

(10)

According to Eq. (1), the input and output impedance of the two-port network can be converted by ABCD matrix, and the expression is shown as:

\[
Z_{C} = \frac{V}{I} = \frac{Z_{Ga}A+B}{Z_{Ga}C+D}
\]  

(11)

Similarly, according to Eq. (11), the relationship between the Doherty PA impedance at power back-off and that in saturation can be obtained as:

\[
Z_{sat} = \frac{Z_{sat}'A+B}{Z_{sat}'C+D}
\]  

(12)

Where, \( Z_{sat} \), \( Z_{sat}' \) represents the output impedance of the transistor and the output impedance of the PA branches at the combiner in saturation, respectively. Where, \( Z_{back} \), \( Z_{back}' \) is the output impedance of the transistor and the output impedance of the PA branches at the combiner at power back-off, respectively.

According to Eq. (12) and Eq. (13), the four parameters of ABCD in the two equations can be obtained from different impedance values at saturation and power back-off. From Eq. (7)-(10), ABCD can be expressed by \( \theta_{21} \) and \( S_{22} \) in the S parameter. Therefore, these two parameters can also be obtained by the Eq. (7)-(13). Then, according to the S parameter values, the circuit that meets impedance requirements can be designed.

The designed two-port network omits the traditional offset lines compared to the previous designing method, which make it more compact and more advantageous for broadband designing.

3. Design and implementation:

In order to verify the effectiveness of the proposed method, a broadband Doherty PA is designed and fabricated based on the Rogers 4350B (H=30mil) using CGH40010F transistors. Drain bias voltage of the carrier and peak PA is set to 28V. And the gate bias voltage of the carrier and peak PA is -2.7V and -5.5V, respectively. The designed Doherty PA is a symmetrical structure. Therefore, \( Z_{back} \) is 25Ω and \( Z_{sat} \) is 50Ω, according to Doherty theory [26]. From load-pull system, the output impedance \( Z_{sat} \) and \( Z_{back} \) of the transistor at power saturation and 6dB power back-off can be obtained. The values of the ABCD matrix can be calculated from Eq. (12) and Eq. (13), and the parameters of the two-port network can be obtained. The circuit structure and parameters that are finally designed and optimized in the ADS software are shown in Fig. 2.

Fig. 2 The implemented circuit of carrier PA branches and simulated impedances of carrier PA branches at combiner
The simulated impedances are shown in Fig. 2. It can be seen that the impedance of the carrier PA branch is close to 50Ω and 25Ω at power saturation and power back-off, respectively. And it is similar for designing the peak PA branch. The \( Z_{\text{back}} \) is infinity and \( Z_{\text{sat}} \) is 50Ω [27]. The output impedance \( Z_{\text{sat}} \) and \( Z_{\text{back}} \) of the transistor at power saturation and power back-off can be obtained using load-pull system. The values of the ABCD matrix can be calculated from Eq. (12) and Eq. (13). And the two-port network circuit can be designed. The circuit structure and parameters that are finally designed and optimized in the ADS software are shown in Fig. 3. The simulated impedances are shown in Fig.3. It can be seen that the impedance of the carrier PA branch is close to 50Ω and open at saturation and power back-off, respectively.

Fig. 3 The implemented circuit of peak PA branches and simulated impedances of peak PA branches at combiner

4. Measurement and results

The photograph of the fabricated Doherty PA is shown in Fig. 4.

Fig. 4 Photograph of the fabricated DPA

The proposed Doherty PA is measured using continues wave and the results are plotted in Fig. 5, Fig. 6 and Fig.7. It can be seen from Fig. 5 that the saturated output power is 43.5-45dBm and the saturated drain efficiency is 65-75% in 2.1-2.7GHz. And it can be seen from Fig. 6 that the drain efficiency is greater than 40% at the 6dB power back-off in the same frequency band. And the gain is above 12dB.
This paper presents a simple method for designing broadband Doherty PAs based on two-port networks. The traditional output matching and load modulation networks are represented by establishing a two-port network. And the relationships between the required impedance at saturation and power back-off and the two-port network parameters are derived. Then, the two-port network can be designed. This proposed method makes it possible to extend the bandwidth of the Doherty PA by omitting traditional offset lines that limit the bandwidth of the Doherty PA. The measurements show that the saturated output power is 43.5-45dBm in 2.1-2.7 GHz, and the saturated drain efficiency is between 65% and 70%. And the drain efficiency is greater than 40% at 6 dB power back-off and the gain is above 12dB.

4. Conclusion

Performance comparison has been made between the proposed Doherty PA and precisely reported at similar frequency band in Table I, which indicates that the proposed Doherty PA has better performance in output power and gain in a wide frequency range. It can be seen that the fractional bandwidth of DPA in this paper is superior to other DPAs in Ref except Ref. [19] from Table I. But, the output power of the proposed DPA is larger than that of Ref. [19].

**Table I. Performance comparison of broadband high efficiency DPAs**

| Ref | Freq (GHz) | Freq bandwidth | Psat (dBm) | DE@Sat (%) | DE@O PBO 6dB (%) | Gain (dB) |
|-----|------------|----------------|------------|------------|------------------|-----------|
| [15] | 3.3-3.6    | 18.2 %         | 43-44      | 55-66      | 38-45            | >10       |
| [19] | 2.0-2.6    | 26.0 %         | 40.5-42    | 58-70      | 36-55            | 10-12.3   |
| [28] | 2.0-2.5    | 22.0 %         | 42.4-43.4  | 63-77      | 44-61            | 9.1-10.2  |
| [29] | 1.95-2.25  | 14.2 %         | 40-43.5    | 60-64      | 48-50            | 9.2-10.4  |
| [30] | 1.96-2.46  | 22.6 %         | 40-42.7    | 60-65      | 40-44            | 10-12     |
| This work | 2.1-2.7   | 25%            | 43.5-45    | 65-70      | 43-54            | >12       |

**Fig. 7** (a) Measured drain efficiency versus output power and (b) gain versus output power.

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