A high linearity high speed time-interleaved track and hold circuit

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Abstract. This paper presents a high linearity 4GS/s 4-way time-interleaved track and hold circuit in 65nm CMOS process. A high linearity track and hold amplifier is designed for each single channel, which utilizes open-loop structure instead of traditional closed-loop structure used in low speed applications. In the presented design, we introduced clock-boosting switches and buffers applying source degeneration technique to enable the high linearity. Meanwhile signal feedthrough is cancelled by dummy switches. The proposed design finally achieves over 52 dB signal to noise and distortion ratio (SNDR) for a 400 mV input Vpp at 4GS/s sampling rate.

1. Introduction
As bridges connecting analog domain and digital domain, the performance of analog-to-digital converters (ADC) has a tremendous impact on signal processing chains. The rapid development of communication technology and signal processing technology requires higher sampling rate and higher resolution of ADC. Issues exist that it is very difficult for monolithic ADC to meet both the requirements of high speed exceed GS/s and high accuracy in the existing CMOS process, while time-interleaved ADC can improve the speed effectively and ensure the sampling precision [1]. Track and hold circuits with wide bandwidth and high linearity is critical to the design of ADC to accurately acquire the input signal. There are generally two kinds of structure for track and hold circuit of time interleaved ADC, one with front-end sampler and the other without front-end sampler, and they are discussed in [2]. The architecture without front-end sampler is better for high linearity and it can achieve a larger bandwidth. To improve the dynamic performance, the track and hold amplifier (THA) is introduced in [3]. Closed-loop structure has been shown to achieve high linearity up to 16 bits [4], however, it suffers low sampling rate and poor stability due to the existence of the feedback loop. Open-loop structure is widely adopted because of its simple architecture, high speed operation, wide bandwidth [5]. Note, however, that open-loop structure has poor linearity.

This paper demonstrates a 4-way time-interleaved track and hold circuit with high linearity THA in each channel, which offers 4GS/s sampling rate and 52dB SNDR. The rest of the paper is as follows. Section 2 described the architecture of the time-interleaved track and hold circuit and challenges in the design of the proposed track and hold circuit. The circuit implementation is introduced in Section 3. The layout and simulations are shown and discussed in Section 4. Finally, conclusions are drawn in Section 5.
2. Challenges and Architecture

The time-interleaved track and hold circuit proposed by this paper adopts architecture shown in Figure 1. (b), which can achieve a higher bandwidth to ensure the accuracy of the signal at high speed sampling rate since a higher bandwidth means the less impact of bandwidth mismatch between channels to the final SNDR. Mismatch between channels such as offset mismatch, gain mismatch, timing mismatch and bandwidth mismatch would cause spurious tones that would decrease the linearity. They will not be discussed here since they can be calibrated by digital method and may need complex algorithm. Considerations about linearity in this paper are mainly focused on THA in each channel.

THA consists of two sections, sample section for tracking and holding the input signal and buffer section for outputting the step signals sampled from input signal. In high frequency design, signal is connected to the input node through a transmission line with an impedance of 50 ohms, thus a 50 ohms terminal resistance is connected between the input node and the ground to mitigate the reflection of signal. That is to say, we can see a 25 ohms shunt resistance from the input node to the source. Apparently an input buffer with constant high input impedance and low output impedance should be employed in the sample section, which is shown in Figure 2.

![Figure 1. Architectures of time-interleaved ADC: (a) Architecture with a frontend track and hold circuit, (b) Architecture without frontend track and hold circuit](image)

![Figure 2. Track and hold circuit with input buffer to mitigate signal reflection](image)

![Figure 3. (a) Clock-boosting switches (b) Signal feedthrough cancellation](image)
As mentioned before, high speed design usually adopted open-loop THA but it suffers bad linearity. Now we analyze the source of the nonlinearity. Charge injection and clock feedthrough exist when the state of switch changes, charge will be redistributed between parasitic capacitor and sampling capacitor, resulting in the distortion of sampling signal. The magnitude of the distortion is determined by the value of sampling capacitor and the channel length $L$ of the switches. Also the on-resistor $R_{ON}$ of the switches changing along with the input signal introduced spurious tones into the signal, as the switches and sampling capacitor can be seen as a first order system whose bandwidth is determined by $R_{ON}$. This can be solved by the using of clock-boosting switches (shown in Figure 3. (a)). Signal feedthrough cannot be neglected in high speed applications due to the large width $W$ and large parasitic capacitor, it can be cancelled by generating a second feedthrough path with an opposite polarity (shown in Figure 3. (b)). And what's more, the buffers will introduce new nonlinearity, these will be analyzed in detail later.

This paper designed a high linearity THA (shown in Figure 4.) for the time-interleaved ADC. We adopted source follower as input buffer. Clock-boosting switches are used in the system. Finally, we carefully designed a high linearity output buffer whose gain is designed higher than 1 to compensate the gain loss in source follower. The circuit is implemented in full differential form.

3. Circuit Implementation

3.1. Input buffer

In this paper, the source follower is used as input buffer for it has simple structure and good linearity due to its intrinsic feedback. As is shown in Figure 5, we designed a pseudo-differential NMOS source follower. Transfer function of the source follower is:

$$A_V = \frac{g_{m1,2} r_{ds1,2} r_{ds3,4}}{1 + g_{m1,2} r_{ds1,2} r_{ds3,4}} \quad \text{(1)}$$

where $A_V$ is the gain of the source follower, $g_m$ is the transconductor and $r_{ds}$ is the dynamic drain-source resistor of the transistor. When $g_{m1,2} r_{ds1,2} r_{ds3,4} \gg 1$, the transfer function can be seen constant as 1. Actually, the $A_V$ is usually less than 1, and changes with the input signal because of bulk effect. We usually adopted PMOS source follower as PMOS transistors have independent well in standard CMOS process so that the source and substrate can be directly connected. However, the sampling rate of this design is higher than 1 GS/s, so we choose the NMOS source follower. Compared with PMOS, the advantage of NMOS source follower is that it can achieve higher bandwidth due to the faster mobility of carrier electrons in NMOS channel. Higher bandwidth makes NMOS source follower more advantageous in response to signals. This is especially important in high-speed design. The bandwidth of the demonstrate source follower is more than 50GHz and it is worth noting that the gain of the source follower is 0.8.
3.2. Output amplifier
The output buffer isolates the sampling capacitor and the subsequent sub-ADC, compensates for the gain loss of the input buffer, provides an operational amplifier with a gain greater than 1. Taking this into consideration, we designed a telescopic amplifier. The amplifier is implemented by NMOS to achieve higher bandwidth. The input pair adopts cascode structure. Since the nonlinearity of the amplifier mainly comes from the transconductance $g_m$ of the input transistor, we introduce the source degradation technique in the design of the amplifier which mitigates dependence of the transconductance of the input transistor on the input signal.

As is shown in Figure 6, M1 and M2 is the input transistor. M3 and M4 as common gate device can mitigate the miller effect of the parasitic capacitor between the gate and drain on the one hand also it isolates the sensitive output node and large input transistor so that can improve the linearity. R1 and R2 are used as degenerative feedback resistor, which reduce the sensitivity of equivalent transconductance to input signal swing. The resistor $R_3$ reduces the influence of $g_{m3}$ and $g_{m4}$ on the gain of the amplifier. M5 and M6 work as load device, M7 provides the required bias current for the amplifier as the tail current source. The gain of the amplifier is:

$$A_V = -\frac{g_{m1,2}}{1 + g_{m1,2} \cdot R_{1,2} \cdot \frac{R_3}{2} \cdot \frac{1}{g_{m3,4}}} \cdot \frac{g_{m3,4}}{g_{m5,6}}$$

$$A_V \approx -\frac{1}{R_{1,2} \cdot g_{m5,6}} \left(1 + \frac{2}{g_{m3,4} \cdot R_3}\right)$$

when the value of $g_{m3}R_3$ is very large then the gain can be seen as:

$$A_V \approx -\frac{1}{R_{1,2} \cdot g_{m5,6}}$$

Figure 5. Pseudo-differential NMOS source follower

Figure 6. Output amplifier with source degeneration
We can see that the gain is only related to the source resistance and the transconductor of the load transistor, so that the nonlinearity caused by changing \( g_m \) of the input transistor can be effectively reduced. In layout design, the accuracy requirement of the \( R_3 \) is not very high, only a large resistance is needed to meet the requirement. The gain of the demonstrated amplifier is 2 and its bandwidth is 2.1GHz, which meets the requirements of the sampling rate and accuracy.

4. Simulations and Layout

![Figure 7. Layout of proposed track and hold circuit](image)

![Figure 8. The output of a 230MHz sinusoid input signal](image)
The proposed time-interleaved track and hold circuit is implemented in a 65nm process. The design of the circuit and layout and simulations are completed by Virtuoso software of Cadence platform. Figure 7. shows the layout of the designed circuit, which consumes an area of 0.2mm². To simulate the circuit conveniently, we designed an idea verilogA multiplexer to alternately collect four-channel holding signals to realize the sampling rate of 4GS/s. The time domain waveform is shown in the Figure 8. for the track and hold circuit, which is the time-interleaved output. The frequency of the input signal is 230MHz and the peak to peak swing is 400mV. And Figure 9. shows the output spectrum of the track and hold circuit at an input frequency of 230MHz. High linearity with 52dB SNDR is achieved which is shown in the Figure 9.

Figure 9. The output spectrum of a 230MHz sinusoid input signal

In order to further demonstrate the performance of the track and hold circuit, the output signal is analyzed by Fourier transform and spectrum analysis at different input signal frequencies. Table 1. shows the performance of the proposed track and hold circuit across different input frequencies. The peak to peak swing of all input signals is 400mV. A summary of the performance of this design and a comparison to other state-of-the-art circuit can be found in Table 2. The presented track and hold circuit shows good dynamic behavior at 4 GS/s combined with the best linearity.

| Table 1. The performance at different input frequency |
|------------------------------------------------------|
| Fin (GHz)    | 0.019 | 0.23 | 2.8  | 3.8  |
| SNDR(dB)     | 52.58 | 52.031 | 52.2 | 52.75 |
| SFDR(dB)     | 52.58 | 52.03 | 52.21 | 52.76 |
| THD(dB)      | -52.58 | -52.03 | -52.21 | -52.75 |
| ENOB(bit)    | 8.44 | 8.35 | 8.38 | 8.47 |

5. Conclusion
A high linearity high speed time-interleaved track and hold circuit is proposed in this paper with 4GS/s sampling rate and 52dB SNDR. The track and hold THA used in each channel adopts open loop architecture, and high linearity and wide bandwidth input and output buffer are designed to ensure the performance of the track and hold circuit. And what's more, we introduced clock-boosting switches and signal feedthrough technique into the circuit to improve the linearity. The demonstrated circuit in this paper is implemented by 65nm CMOS technology. With different frequencies input signal of 400mVpp, the track and hold circuit achieved 52dB SNDR.
Table 2. Performance comparison to state-of-art time-interleaved track and hold circuit

| Reference          | [6]  | [7]  | [8]  | [9]  | This work |
|--------------------|------|------|------|------|-----------|
| Process            | 0.13 μm | 28 nm | 65nm | 65nm | 65nm      |
|                    | CMOS | CMOS | CMOS | CMOS | CMOS      |
| fsample(GHz)       | 30   | 10   | 5    | 10   | 4         |
| Input swing(Vpp mV)| 600  | 800  | 300  | 800  | 400       |
| THD(dB@finGHz)     | -29@13 | -38@3.75 | -43  | -41.16@5 | -52.75@3.8 |
| SFDR(dB@finGHz)    | 33@13 | -    | 44.6 | 41.18@5 | -52.76@3.8 |
| SNDR(dB@finGHz)    | -    | -    | -    | 41.11@5 | -52.75@3.8 |

6. References

[1] Greshishchev, Y. M., Aguirre, J., Besson, M., & Gibbins, R. 2010. A 40GS/s 6b ADC in 65nm CMOS. *IEEE International Solid-state Circuits Conference*. IEEE.

[2] Louwsma S, Van Tuijl E, Nauta B 2009. *Time-interleaved Analog-to-Digital Converters[M]*.

[3] Dinc H, Allen P E 2009. A 1.2 GSample/s Double-Switching CMOS THA With -62 dB THD[J]. *IEEE JSSC*, 44(3):848-861.

[4] Devarajan S, Singer L, Dan K, et al. 2009. A 16-bit, 125 MS/s, 385 mW, 78.7 dB SNR CMOS Pipeline ADC[J]. *IEEE JSSC*, 44(12):3305-3313.

[5] M. Hasan-Sagha and M. Jalali 2012."Very high speed and low voltage open-loop dual edge triggered sample and hold circuit in 0.18μm CMOS technology," *10th IEEE ICSE*, Kuala Lumpur, pp. 645-648.

[6] H. Orser and A. Gopinath, 2010 A 20 GS/s 1.2 V 0.13μm CMOS Switched Cascode Track-and-Hold Amplifier *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 7, pp. 512-516.

[7] Shahramian S, Voinigescu S P, Carusone A C 2006. A 30-GS/sec Track and Hold Amplifier in 0.13-μm CMOS Technology[C] *IEEE CICC*.

[8] G. Tretter et al. 2013 10-GS/s track and hold circuit in 28 nm CMOS, *ISCDB*, pp. 1–3.

[9] Zhang L, Li D, Zhu Z, et al. 2016 A 10-GS/s 6-bit Track-and-Hold Amplifier for Time-interleaved SAR ADCs in 65-nm CMOS[J]. *JCSC*.