A 9.52 dB NCG FEC scheme and 164 bits/cycle low-complexity product decoder architecture

Carlo Condo, Pascal Giard, Member, IEEE, François Leduc-Primeau, Member, IEEE, Gabi Sarkis and Warren J. Gross, Senior Member, IEEE
Department of Electrical and Computer Engineering, McGill University, Montreal, QC, Canada

Abstract—Powerful Forward Error Correction (FEC) schemes are used in optical communications to achieve bit-error rates below $10^{-15}$. These FECs follow one of two approaches: concatenation of simpler hard-decision codes or usage of inherently powerful soft-decision codes. The first approach yields lower Net Coding Gains (NCGs), but can usually work at higher code rates and have lower complexity decoders. In this work, we propose a novel FEC scheme based on a product code and a post-processing technique. It can achieve an NCG of 9.52 dB at a BER of $10^{-15}$ and 9.96 dB at a BER of $10^{-18}$, an error-correction performance that sits between that of current hard-decision and soft-decision FECs. A decoder architecture is designed, tested on FPGA and synthesized in 65 nm CMOS technology: its 164 bits/cycle worst-case information throughput can reach 100 Gb/s at the achieved frequency of 609 MHz. Its complexity is shown to be lower than that of hard-decision decoders in literature, and an order of magnitude lower than the estimated complexity of soft-decision decoders.

I. INTRODUCTION

Optical communication systems rely on extremely high-speed links that require high degrees of reliability. A Bit Error Rate (BER) lower than $10^{-15}$ and speeds of up to 100 Gb/s are required by the ITU-G.709 standard, a standard that defines the specifications for Optical Transport Networks (OTNs), while even higher speeds are foreseen in next generation standards. To achieve such low BER requirements, powerful Forward Error Correction (FEC) schemes must be employed. Recent approaches to high-performance, high-speed error-correction schemes follow one of two paths: concatenation of (often algebraic) hard-decision codes [1–3] or soft-decision, iterative decoding of inherently more powerful codes, first among all, Low-Density Parity-Check (LDPC) codes [4]. The latter produced high-gain FEC schemes, that however must rely on complex decoding architectures [5–8].

For example in [3], Bose-Chaudhuri-Hocquenghem (BCH) codes [9] are concatenated in a braided scheme and decoded with a hard decision algorithm. The FEC of [3] is reported to achieve 9.35 dB of Net Coding Gain (NCG) at a Bit Error Rate (BER) of $10^{-15}$ with a 7% code overhead. While no decoder architecture is proposed, the estimated latency of the decoding scheme is of 1.15 million bits. With similar overhead, the FEC proposed in [1] uses different BCH codes in a quasi-product structure, achieving high throughput and a 9.19 dB NCG at a high cost in area occupation. The BCH-based product code proposed in [10], with a code length of 98 kbits and rate of 0.937, achieves a 9.4 NCG at BER=$10^{-15}$, without implementation details. Staircase concatenation [2]

has been recently proposed as an efficient and powerful FEC for 100 Gb/s OTNs.

Soft-decision FECs are a relatively recent addition to the FEC world for optical communication. Few soft-decision FECs have been proposed, and no decoder implementations were found in the literature. In [5] two FECs are proposed, a concatenated scheme using Reed-Solomon and LDPC codes, and a triple concatenation of an LDPC code with two algebraic codes. With a total overhead of 20.5%, it was shown that an NCG of 10.8 dB could be achieved. BCH codes and spatially-coupled LDPC codes are used in [6]: a 12 dB NCG is estimated at a BER of $10^{-15}$, obtainable with a 25.5% overhead. The FEC described in [11] concatenates a soft-decision code with a product code, yielding 11 dB NCG at BER=$10^{-15}$ with a 20.5% overhead and a code length of millions of bits.

We introduce in this paper a powerful FEC scheme relying on a product code [12] based on algebraic component codes, that thus belongs to the first category of FECs for optical communications. The proposed FEC can reach very low BER with a code rate comparable with recent OTN FEC solutions. A high-speed, low-complexity decoder architecture for the proposed FEC is designed, tested on a Field Programmable Gate Array (FPGA) and synthesized in 65 nm CMOS technology. We show that our decoder can reach a minimum 100 Gb/s of information throughput at a frequency of 609 MHz, and has a gate count of approximately 1.15 million gates. It has a decoding latency of 319 ns making it suitable for low-latency environments, like data centers.

The rest of this paper is organized as follows. Section II describes the FEC scheme in details, its decoding process and its error-correction performance. In Section III the decoder hardware architecture is portrayed, while implementation and test results are given in Section IV. Section V briefly discusses possible modifications to the decoder architecture along with their implications. Finally, Section VI draws the conclusions.

II. FEC SCHEME

Product codes [12] are a class of error-correction codes constructed by encoding a matrix of information symbols row-wise with a row component code, and subsequently column-wise using a column component code. The twofold encoding acts as a parallel concatenation of the row and column component codes. The choice of the component code has a great impact not only on the error-correction performance of
the product code, but on the speed and encoding/decoding complexity of the FEC scheme as well. BCH codes [9] are a class of widely used algebraic codes, identified by the set of parameters \((n, k, t)\), where \(n\) is the code length, \(k\) the number of information bits, and \(t\) the maximum number of errors that are guaranteed to be correctable. The standard BCH decoding algorithm relies on hard decision, and when \(t = 2\) (and to a lesser extent \(t = 3\)), the general algorithm can undergo substantial simplifications [2], [13] that reduce both latency and implementation complexity. We thus consider BCH codes as a starting point for the construction of our FEC scheme.

While it is not strictly necessary, we assume that the same BCH component code is used to encode both the rows and the columns of the information matrix. We form a \(k \times k\) matrix with the information bits. Each row of the matrix is first encoded into a BCH code, resulting in a \(k \times n\) matrix. Then, each of the \(n\) columns are also encoded into a BCH code to form the \(n \times n\) product-code codeword. Since the BCH component code is systematic, the product code is also systematic. Note that it is equivalent to first encode the columns of the information matrix, followed by the rows. We denote by \(N = n^2\) the length of the resulting product code, and by \(K = k^2\) the number of information bits in a codeword. The code rate of the product code is \(K/N = k^2/n^2\).

While a BCH code with \(t = 2\) guarantees a simple decoding process, a very long product code would be necessary to even get close to OTN’s BER requirements. However, the error correction performance of the product code can be substantially improved at a small cost in code rate by using extended-BCH (eBCH) codes as component codes. An eBCH code of length \(n\) is composed of a BCH code of length \(n - 1\) and of an additional parity bit, which increases the minimum distance of the code by 1. This increased distance can be used to reduce the probability of undetected failure of the component decoder, thereby reducing the number of new errors that are introduced by the component decoder and improving the performance of the product decoder.

Since optical communications require a BER lower than \(10^{-15}\), we must make sure that no error floor occurs at higher BER. The existence of an error floor is usually caused by particular error patterns that are difficult to impossible for the decoder to correct. A post-processing technique that can greatly enhance the error-correction performance of product codes based on polynomial component codes has been proposed in [14]. The product code decoding is performed by alternatively decoding the rows and the columns of the received matrix: it is thus possible to identify rows and columns whose decoding has failed (see Section II-A for more details). Based on this knowledge, the post-processing technique flips the bits at the intersection of failed rows and columns, greatly reducing the contribution of stall patterns to the error floor. This method is also applied in our proposed FEC scheme.

### A. Decoding Algorithm

As previously mentioned, the decoding of product codes can be performed by iteratively decoding the row and column component codes. Each iteration is divided into two half iterations, the first half decoding the rows and the second half the columns. Each row and column of the product code is decoded using the eBCH decoder described in Algorithm 1. The additional parity bit in the eBCH codeword is placed at position \(n\). The \(\text{bch}(\cdot)\) function refers to the standard bounded distance BCH decoder, which returns a flag \(\text{FAIL}\) indicating whether or not the decoder detected a failure, and a vector \(e\) of length \(n - 1\) indicating the location of errors, if applicable. The notation \(x_{i:j}\) with \(i \leq j\) refers to a vector of length \(j - i + 1\) containing elements \(i, i+1, \ldots, j\) of the vector \(x\). The operator \(\oplus\) denotes modulo-2 addition.

The BCH decoder can correct up to \(t\) errors. If there are more than \(t\) errors, the decoder could return another codeword, introducing an undetected failure. However, the parity extension allows detecting failures caused by the presence of \(t + 1\) errors. The eBCH decoder therefore declares a failure if either the BCH decoder detects a failure, or if \(t + 1\) errors are detected, i.e., if \(d + d_e = t + 1\).

The post processing is applied after a predefined number of decoding iterations have been completed. Let us denote by \(R\) \((C)\) the set of row \((column)\) indices for which the component decoder reported a decoding failure. If \(0 < |R| \leq t + 1\) and \(0 < |C| \leq t + 1\), we flip all the bits located at the intersection of a row in \(R\) and of a column in \(C\). Since this may introduce new bit errors, we then decode again all rows and columns whose bits were flipped.

When \(t = 2\), the decoding of the BCH part of eBCH component codes can be substantially simplified by using the Peterson-Gorenstein-Zierler algorithm [13]. As will be shown in Section II-B, codes with \(t = 2\) can achieve very good error-correction performance even at moderately high rates: at the same time, the decoder architecture benefits from reduced complexity and latency. Thus, the \(\text{bch}(\cdot)\) function relies on the specialized algorithm, that differs from standard BCH decoding algorithms [9] in that syndrome values are used directly to find the roots of the error-locator polynomial. Only

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**Algorithm 1: Decoding of eBCH codes**

input : Component codeword \(r\)
output: Updated codeword \(r'\)

begin
  \(\text{FAIL}, e \leftarrow \text{bch}(r_{1:n-1})\)
  if \(\text{FAIL}\) then
    \(r' \leftarrow r\)  // decoding failure
  else
    \(d := \sum_{i=1}^{n-1} e_i\)
    \(d_e := (d + \sum_{i=1}^{n} r_i) \mod 2\)
    if \(d + d_e \leq t\) then
      \(r'_{1:n-1} \leftarrow r_{1:n-1} \oplus e\)
      \(r'_n \leftarrow r_n \oplus d_e\)  // parity correction
    else
      \(r' \leftarrow r\)  // decoding failure

end
two syndromes need to be calculated:

\[
S_1 = \sum_{i=0}^{n-1} r_i \alpha^i, \tag{1}
\]

\[
S_3 = \sum_{i=0}^{n-1} r_i \alpha^{3i}, \tag{2}
\]

where \( r \) is the input to the decoder and \( \alpha \) the primitive element of the BCH Galois Field (GF). Based on the values of \( S_1 \) and \( S_3 \), different cases arise:

- \( S_1 = 0 \) and \( S_3 = 0 \): no errors were detected.
- \( S_1 \neq 0 \) and \( S_3^2 + S_3 = 0 \): one error located at \( \log_\alpha S_1 \) was detected.
- \( S_1 = 0 \) and \( S_3^2 + S_3 \neq 0 \): more than two errors occurred and the decoder declares failure.
- \( S_1 \neq 0 \) and \( S_3^2 + S_3 \neq 0 \): two or more errors occurred. In this case, the decoder attempts to find the roots \( (\rho_1 \text{ and } \rho_2) \) of

\[
x^2 + x + \frac{S_3^2 + S_3}{S_1^2} = 0. \tag{3}
\]

Decoding failure is declared if no roots were found. Otherwise, the decoder detects two errors located at \( \log_\alpha S_1 \rho_1 \) and \( \log_\alpha S_1 \rho_2 \).

B. Code Selection and Error-Correction Performance

Depending on the requirements, the proposed FEC scheme can employ different \( \ell \) BCH component codes. We have evaluated the effect of different code parameters on both the simulated BER and the estimated error floor. Existing FEC schemes for optical communications vary in code length, rate and decoding complexity. The recent trends towards soft-decision decoding led to high NCGs, with code overheads reaching 20% and large estimated decoder area occupations [7], [8], [15]. An overhead of 20% translates into a code rate of approximately 0.833. For our proposed FEC, using the extended-BCH (256,239,2) code as a component code, the resulting product code has a rate of 0.878. We can thus consider shortening the code by \( \ell \) bits, leading to a product code of rate \( \frac{(k-\ell)}{n} \). For rates greater than 0.833, with \( n = 256 \) and \( k = 239 \), the shortening can use any \( \ell \leq 61 \).

Using \( \ell = 61 \), the resulting product code has a length of \((256 - 61)^2 = 38,025\) bits.

Fig. 1 plots the BER for the \((195,178)^2\) product code, along with the error floor, estimated as in [14], with and without the use of post processing. The reported error floor represents the contribution of minimal stall patterns to the error rate. Simulations have been performed on a binary symmetric channel (BSC), and \( p \) represents the input error probability. It can be seen that both the error floor and BER of the considered product code are substantially reduced by post processing. As \( p \) decreases, the BER approaches the estimated error floor, which has been shown to be a tight lower bound on the BER for this code [14]. Table I reports the NCG values achieved by the proposed FEC at different values of \( p \); at the commonly considered BER of \( 10^{-15} \), the bound shown by our FEC has an NCG of 9.52 dB that grows up to 9.95 dB at a BER of \( 10^{-18} \).

As shown in [14], the BER curve reaches the bound earlier than BER\(=10^{-13} \) when four decoding iterations are performed: the trend shown in Fig. 1 lets us assume that the bound will be reached at around BER\(=10^{-15} \) or slightly lower when two decoding iterations are considered.

Fig. 2 shows how the error-correction performance changes as the code rate is kept constant, while \( n, t \), the number of iterations and the application of post processing are varied. The BER of the \((195,178)^2\) product code is shown for two and four decoding iterations, with and without the application of post processing. Increasing the number of iterations results in a substantial improvement at higher \( p \) values. However, the
Table I
NET CODING GAIN VALUES FOR THE PROPOSED FEC.

| \( p \)     | BER  | NCG [dB] |
|------------|------|----------|
| 7 \( \cdot \) 10^{-5} | 10^{-9} | 7.7507   |
| 5 \( \cdot \) 10^{-3} | 10^{-13} | 9.1061   |
| 4 \( \cdot \) 10^{-3} | 10^{-15} | 9.5260   |
| 2.7 \( \cdot \) 10^{-3} | 10^{-18} | 9.9596   |

Figure 3. Product decoder Architecture.

main contribution to the error floor comes from error patterns that the decoder cannot correct, regardless of the number of iterations. Consequently, as \( p \) decreases, the two and four iteration curves converge. This trend can be observed with and without post processing.

The \((219,200)\)^2 product code uses a component code shortened from the \((512, 493, 2)\) eBCH code. It is 26% longer than the \((195,178)\)^2 code. The large amount of applied shortening slows the convergence speed of this code: its curve slope is bound to outperform the \((195,178)\)^2 curve at around BER\(=10^{-12}\). Thus, a larger number of iterations is necessary to fully exploit this code at higher \( p \), decreasing the achievable throughput. Moreover, the decoder architecture would need a significant amount of additional memory, and the trade-off between logic and latency would be less advantageous. Two and four iterations BER curves for a \((321,293)\)^2 product code are plotted as well: it is the smallest product code with \( t = 3 \) and the same rate as the \((195,178)\)^2 product code. It is 171% longer than the \((195,178)\)^2 code. Its error-correction performance is better than the other codes shown in Fig. 2. However, a decoder architecture targeting this code would be significantly more complex. In fact, aside from the use of \( t = 3 \) requiring slightly higher decoding and hardware complexity than \( t = 2 \), the longer code would substantially increase gate count and decoding latency.

III. PRODUCT DECODER ARCHITECTURE

The overall structure of the product decoder is portrayed in Fig. 3. The product code is stored in a \( n \times n \) register matrix acting as a scratch memory. The proposed architecture is sized on the considered \((195,178)\) component code: Section V discusses the necessary modifications in case the code is changed. An array of \( P_c \) component decoders decodes as many product code rows (columns) in parallel. Inputs and outputs of each eBCH decoder are connected to \( \frac{1}{P_c} \) rows and \( \frac{n}{P_c} \) columns of the scratch memory. The outputs of the component decoders flip the bits in the scratch memory that are identified as incorrect: they are ANDed with a valid signal coming from the control module, while the inputs to the component decoders are multiplexed, scanning the rows and the columns in order. The control of the decoder architecture can be greatly simplified in case \( P_c \) is an exact divisor of \( n = 195 \): the proposed architecture has consequently been sized for \( P_c = 13 \), a choice offering a good tradeoff between achievable throughput and hardware complexity.

Product codewords are loaded from an external input buffer into the scratch memory, through a bus as wide as \( P_1 \) eBCH codewords \((P_1 \times n \text{ bits})\). This bus is also connected to the component decoder array, allowing the first half iteration to be performed in parallel to the codeword loading. Each register of the scratch memory is preceded by an XOR gate, that allows the bit-flipping signals coming from the component decoders to correct errors. The proposed architecture has been sized assuming \( P_1 = 2 \).

The scratch memory features two \( n \)-bit failure registers that keep track of which rows and columns have suffered a decoding failure during the last half iteration in which they were involved.

In Section III-A to III-D, we detail the product-decoder architecture and its operation. In particular, we detail the eBCH component decoder, and then divide the decoding process into three conceptual functions: the loading of the product codeword and first half iteration, the standard iterations and the post-processing iteration.

A. Extended-BCH Decoder Architecture

In this section, we describe the designed eBCH decoder architecture, whose functional scheme is portrayed in Fig. 4. Five main blocks can be identified: the syndrome calculation module, that works in parallel to the parity calculation module, the selectors and logarithms module, the error locator module and the bit-flipping and post-processing module. Light gray blocks represent pipeline stages, while the darker gray block is the failure register (described in details in Section III-C1).

1) Syndrome Calculation Module: The syndrome calculation module performs \((1)\) and \((2)\) in parallel on the BCH codeword. All \( \alpha^i \) and \( \alpha^{3i} \) are precomputed and stored as static 8-bit values. Since \( r_i \) is a single bit, each multiplication in \( r_i \alpha^i \) and \( r_i \alpha^{3i} \) requires 8 AND gates. Summations within GF(8) are equivalent to the XOR operation, so each sum in \((1)\) and \((2)\) requires 8 XOR gates. The XOR tree required to perform them all is split between the fourth and fifth stages to shorten the critical path.

2) Parity Calculation Module: The parity calculation module performs \( \sum_{i=1}^{n} r_i \), that requires XORing all \( n \) codeword bits. As this module works in parallel to the syndrome calculation module, and its structure is similar, an internal pipeline stage splits the XOR tree between the fourth and fifth stages as well.
3) Selectors and Logarithms Module: This module performs partial calculations and logarithmic domain conversions that are needed by the error locator module to identify errors. Four 8-bit-wide Lookup Tables (LUTs) are needed to calculate the following quantities:

- \( S_3^3 \), with input \( S_1 \);
- \( \log(S_3^3) \), with input \( S_3^3 \);
- \( n - 1 - \log(S_1) \), with input \( S_1 \);
- \( \log(S_3^3 + S_3) \), with input \( S_3^3 + S_3 \).

Since both \( \log(S_3^3) \) and \( \log(S_3^3 + S_3) \) perform the same operation with different inputs, they are merged into a single LUT.

The summation required by \( S_3^3 + S_3 \) is performed within GF(8), requiring 8 XOR gates. An 8-bit adder is instead required to perform \( \log(S_3^3 + S_3) - \log(S_3^3) \): switching to logarithmic domain allows to avoid a division, but sums are not constrained to GF(8) anymore, and cannot be implemented with an XOR operation. The Selection NORs block in Fig. 4 evaluates the following signals, each of which can be calculated with an 8-input NOR gate:

- \( S_1^3 = 1 \) if \( S_1 = 0 \);
- \( S_3^3 = 1 \) if \( S_3 = 0 \);
- \( (S_3^3 + S_3)^2 = 1 \) if \( S_3^3 + S_3 = 0 \).

These three signals are passed to the error locator module, along with \( n - 1 - \log(S_1) \) and \( \log(S_3^3 + S_3) - \log(S_3^3) \).

To reduce the system’s critical path, an internal pipeline is present in this module. All LUTs are placed before the pipeline stage, along with most calculations, except \( \log(S_3^3 + S_3) - \log(S_3^3) \), that is performed after the registers.

4) Error Locator Module: The error locator module is tasked with the solution to (3) and the unequivocal identification of the status of the eBCH decoding process (no errors, one error, two errors, failure). A 17-bit-wide LUT stores the values of \( \log(\rho_1) \) and \( \log(\rho_2) \), i.e. the logarithm of the roots of (3), along with a validity flag to signal if the roots exist or not. The LUT is addressed through \( \log(S_3^3 + S_3) - \log(S_3^3) \).

Two 8-bit adders compute \( n - 1 - \log(S_1) - \log(\rho_1) \) and \( (n - 1 - \log(S_1)) - \log(\rho_2) \), the error locations in case the decoder detects two errors. The error location in case of a single error is \( n - 1 - \log(S_1) \).

The decoder status is determined on the basis of the signals computed in the selectors and logarithms module, the parity check result, and the validity of the computed roots, through the following set of boolean equations:

- **NoErrors** : \( S_1^3 \land S_3^3 \)
- **Fail1** : \( S_1^3 \land S_3^3 \land (S_3^3 + S_3)^2 \)
- **1Error** : \( (S_3^3 + S_3)^2 \land S_1^3 \)
- **2Errors1** : \( (S_1^3 \land S_3^3) \lor (S_1^3 \land (S_3^3 + S_3)^2) \lor (S_1^3 \land (S_3^3 + S_3)^2) \)
- **Fail2** : \( 2Errors1 \lor (\sum_{i=1}^n r_i \land \text{ValidRoots}) \lor \text{ValidRoots} \)
- **Fail3** : \( 2Errors1 \land (\text{ErrorLoc1} > n - 1 \lor \text{ErrorLoc2} > n - 1) \)
- **Failure** : \( \text{Fail1} \lor \text{Fail2} \lor \text{Fail3} \lor \text{Fail4} \)
- **OneError** : \( \text{1Error1} \land \text{Failure} \)
- **TwoErrors** : \( 2Errors1 \land \text{Failure} \)

The four boldfaced signals are in mutual exclusion and are passed to the bit-flipping and post-processing module along with the two error locations. **OneError** is used to select between the two possible error locations \( (n - 1 - \log(S_1)) - \log(\rho_1) \) and \( (n - 1 - \log(S_1)) \), and **Failure** is stored in one of the two \( n + 1 \)-bit failure registers of the product code decoder, that track eBCH decoding failures among rows and columns.

As with the selectors and logarithms module, an internal pipeline stage reduces the system critical path. The validity of the roots, the second error location and the first four boolean equations are evaluated before the pipeline, while the other boolean equations and selection of the first error location are performed after the registers.
5) Bit-Flipping and Post-Processing Module: According to the provided error locations, this module selects the appropriate signals to correct the errors by flipping bits. The bit-flipping signals are combined and masked following the decoder status and post processing. Each error location is converted to a bit-flipping signal of \( n \) bits, one-hot encoded, and masked according to the status of the decoder:

- No errors or failure: both bit-flipping signals are nulled through AND gates;
- One error: the second error location is nulled through AND gates;
- Two or more errors: the second error location is nulled through AND gates.

The additional parity bit-flipping signal is determined according to Alg. 1.

A post-processing activation signal is received as an input from the product-code decoder control module: it is activated in case \( 0 < |R| < t + 1 \), and the eBCH decoder is currently performing the last decoding iteration on a column of the codeword matrix. Thus, if the status of the decoder is failure and post processing is active, the content of the row-failure register is substituted to the bit-flipping signal. If at the end of the product-decoder iteration \( 0 < |C| \leq t + 1 \), then a last iteration on the rows and columns in \( R \) and \( C \) is issued, otherwise decoding is declared unsuccessful.

B. Codeword Loading and First Half Iteration

The first half iteration can be run in parallel with the loading of the product codeword in the scratch memory. At the first clock rising edge after a reset, the loading of the product codeword and the first half iteration begins.

The loading of the scratch memory is performed row wise, and is depicted in Fig. 5. At each clock cycle, the control module issues up to two reset signals to the scratch memory. When a row is reset, its value is available at the decoder output for one clock cycle, while it is substituted with that of eBCH CW 1 or 2, depending on the row.

- **Clock cycle** 1 \( \rightarrow 90 \): eBCH CW 1 loaded in scratch memory rows 1 \( \rightarrow 90 \), eBCH CW 2 loaded in scratch memory rows 91 \( \rightarrow 180 \). Scratch memory rows 1 \( \rightarrow 90 \) output through Output eBCH CW 1, scratch-memory rows 91 \( \rightarrow 180 \) output through Output eBCH CW 2.
- **Clock cycle** 91 \( \rightarrow 105 \): eBCH CW 1 loaded in scratch memory rows 181 \( \rightarrow 195 \). Scratch memory rows 181 \( \rightarrow 195 \) output through Output eBCH CW 1. These 15 clock cycles could be reduced to 8 if both eBCH CW 1 and 2 were used concurrently: however, all the rows 181 \( \rightarrow 195 \) are connected to the same component decoder, thus 15 clock cycles will be required to use them as inputs anyway.

During the first half iteration, the input of each component decoder is not one of the 15 rows of the scratch memory to which it is connected, but either eBCH CW 1 or 2, depending on the decoder. In this way, the codewords currently being loaded in the scratch memory can bypass the loading itself, and directly be decoded. Fig. 6 shows the input multiplexing and output validation for the first component decoder in the array. The multiplexing of inputs is static and does not change for the whole first half iteration, so that component decoder inputs are as follows:

- **Clock cycle** 1 \( \rightarrow 105 \): eBCH CW 1 input to eBCH 1 \( \rightarrow 6 \) and eBCH 13, eBCH CW 2 input to eBCH 7 \( \rightarrow 12 \).

On the other hand, even if all component decoders have received an input, their outputs must be enabled only for the correct scratch memory rows. Considering that the length of the pipeline within component decoders is that of 6 delay elements, the Valid Output signals issued by the control module follow this pattern:

- **Clock cycle** 6 + 1 \( \rightarrow 15 \): eBCH decoder 1 and eBCH decoder 7 have valid outputs.
- **Clock cycle** 6 + 16 \( \rightarrow 30 \): eBCH decoder 2 and eBCH decoder 8 have valid outputs.
- **Clock cycle** 6 + 31 \( \rightarrow 45 \): eBCH decoder 3 and eBCH decoder 9 have valid outputs.
- **Clock cycle** 6 + 46 \( \rightarrow 60 \): eBCH decoder 4 and eBCH decoder 10 have valid outputs.
- **Clock cycle** 6 + 61 \( \rightarrow 75 \): eBCH decoder 5 and eBCH decoder 11 have valid outputs.
- **Clock cycle** 6 + 76 \( \rightarrow 90 \): eBCH decoder 6 and eBCH decoder 12 have valid outputs.
- **Clock cycle** 6 + 91 \( \rightarrow 105 \): eBCH decoder 13 has valid output.

The validated bit-flipping signal is itself zeroed for all the rows connected to the component decoder except for the correct one (see Correct row selection signals in Fig. 6). The component-decoder internal pipeline ensures that the loading of a codeword has been completed before the component decoder tries to correct it.

C. Standard Iterations

What we defined as standard iterations are the second, third and fourth half iterations. The second and fourth half
iterations decode the columns of the product code, while the third decodes the rows. During these half iterations, all 13 component decoders work in parallel. Thus, each of these lasts \([(195/13) = 15]\) + 6 clock cycles, where 6 is the length of the component decoder pipeline.

The \(\text{currRowIn}\) signal is issued by the control module and scans the rows (columns) connected to each component decoder from 1 to 15, one per clock cycle, so that the input of each component decoder is the scratch memory row (column) identified by Eq. (4):

\[
\text{Input row (column)} = (n_{\text{BCH}} - 1) \times 15 + \text{currRowIn}
\]  

where \(n_{\text{BCH}}\) is the number assigned to a component decoder within the component decoder array.

At the start of each half iteration, all component-decoder outputs are invalid, and are made valid simultaneously when the input data has reached the end of their internal pipeline. The selection of the correct row (column) for the output (see Fig. 6) is made according to the \(\text{currRowOut}\) signal, that is the pipelined version of \(\text{currRowIn}\).

1) Failure Registers: As mentioned before, the row- and column-failure registers are two 195-bit registers that are used to track which rows and columns decoding has failed. The row- (column-) failure register is updated during all half iterations that decode scratch memory rows (columns). They are reset at the start of a corresponding half iteration, and updated with the value of the \(\text{Failure}\) signal coming from all component decoders according to the value of \(\text{currRowOut}\).

Failure registers are used in different stages of the decoding process:

- After the last half iteration, that is always a column half iteration, the column-failure register holds the most up-to-date information about the product-code decoding status. Consequently, the outcome of the decoding of the product codeword can be determined by ORing all the bits in the column-failure register: if the result is 1, at least a column has failed, and general decoding failure is declared. On the contrary, a success flag is raised if all bits in the failure register are zero.

- The row-failure register is used at the beginning of the fourth half iteration to determine if post processing should be applied: details are given in Section III-C2 below.

- The content of both registers is used to determine if the post-processing iteration would be useful or not. If both registers identify between one and three failures, then the post-processing has been successfully applied and the post-processing iteration should be run. More details are provided in the following Sections III-C2 and III-D.

2) Post-Processing Application: The idea behind post processing is that if the number of failed rows and columns is between one and three, some stalling patterns can be circumvented by flipping the bits at the intersection of failed rows and columns. Afterwards, the decoding of the previously failed rows and columns is attempted again.

The same result can be obtained in hardware using a slightly different schedule:

1) At the end of the third half iteration, the row-failure register has a 1 in every position corresponding to a failed row.

2) During the fourth half iteration, every time a column decoding fails, the column-failure register is updated. In case of failure, the bit-flipping signal coming from the component decoder is the all-zero signal, i.e. no bits are flipped. However, if the number of ones in the row-failure register is between one and three, the bit-flipping signal is substituted with the content of the row-failure register. This means that all the bits at the intersection of the recently failed column and all the previously failed rows are flipped.

3) At the end of the fourth half iteration, the number of failed rows and columns is checked.

- If the number of failed rows is zero or more than four, post processing was not applied, and no post-processing iteration is issued.

- If the number of failed rows is between one and three, but the number of failed columns is not, post processing was indeed applied, but additional iterations would be useless. In fact, either there are no failed columns (general successful decoding) or there are more than three (the stall pattern is too large and bit flipping will not correct it).

- If both row and column failures are between one and three, post processing was applied, and we hope that we are now out of the stall pattern. A post-processing iteration is issued.

The modified schedule allows the bit flipping step to be performed concurrently with the fourth half iteration, and its performance is equivalent to the schedule described in [14].

D. Post-Processing Iteration

The post-processing iteration is issued under the conditions portrayed in Section III-C2, and it involves up to three rows and three columns. During the second iteration, each component decoder stores the indices of the first three failed row (column) decodings. These indices are gathered by the
control module that, in case the conditions for a post-processing iteration apply, generates the appropriate control signals (input and output row, output validation) for the row (columns) that were involved in the post-processing application. To reduce the complexity of the control logic, each post-processing half iteration is always supposed to involve three rows (columns), each decoded in a different clock cycle. Thus, each post-processing half iteration lasts $3 + 6$ clock cycles, where 6 is the internal component-decoder pipeline depth.

IV. IMPLEMENTATION RESULTS AND COMPARISON

The decoder architecture described in the previous section has been synthesized in TSMC CMOS 65 nm technology using Cadence RTL Compiler, was verified with Mentor Graphics ModelSim and tested with an Altera FPGA. Table II reports the synthesis results for three target frequencies, in terms of area occupation, gate count, latency and information throughput. The timing constraints have been met for all three frequencies, showing that the proposed architecture can be clocked at 609 MHz, and thus achieve 100 Gb/s of information throughput, even with an older technology node like the 65 nm one. The 193 clock-cycles maximum latency is consistently kept under 1 $\mu$s with all frequencies, while the gate count ranges from 898 kgates at 300 MHz to 1155 kgates when targeting the highest frequency. Supposing that the post processing is applied every time, the design yields a worst case information throughput of 164 bits/cycle. However, post processing is not always necessary, and the post-processing iteration is often not performed. Thus, at a very low BER such as $10^{-15}$, the average throughput tends to the maximum achievable throughput of 181 bits/cycle.

Very few detailed reports of decoder implementations for OTN hard-decision FEC schemes can be found in the literature. To the best of our knowledge, [1] is the most recent: the considered FEC scheme uses a modified product-like concatenation of long BCH codes, resulting in a code length of almost 4 million bits and a code rate of 0.933. At a BER of $10^{-15}$, [1] has an NCG of 9.19 dB, against the 9.52 dB gained by our scheme (see Table I). It achieves a throughput of 110 Gb/s with a latency of 38 $\mu$s, while our decoder reaches 100 Gb/s with a 319 ns latency. The decoder in [1] has been synthesized in 90 nm CMOS technology, and yields a gate count of 3732 kgates at 430 MHz, not including SRAM, against the 1155 kgates of the decoder proposed in this work. Moreover, our decoder only uses registers, no SRAM, and the area these registers occupy is included in the gate count. By comparison, the decoder proposed in [1] utilizes 4 Mbit of SRAM memory.

The more recent braided FEC scheme of [3] yields a 9.35 dB NCG at a BER of $10^{-15}$. However, no decoder implementation results were provided. The FEC code length is of 130 kbits with a code rate of 0.937. The decoding process uses a sliding window approach that can limit the gate count, but can have heavy memory requirements while greatly increasing the latency. The latency is estimated at 1.15 million bits.

Soft-decision FECs for OTN have been considered only in recent years: thus, no decoder implementations were found in literature. Considering the gate count and NCG estimations for soft-decision FECs in [7], it can be seen that the NCG achieved in this work sits in the middle between literature’s hard-decision FECs and soft-decision FECs, while the proposed decoder implementation requires an order of magnitude less gates than soft-decision decoders.

A. FPGA Test and Verification

After post-synthesis functional verification with ModelSim, the product decoder has been implemented on an FPGA within a partial digital communication chain. While random data were generated and encoded on a computer, the remainder of the chain has been synthesized to be run on an Altera DE4 board, a board featuring a large Altera Stratix IV EP4SGX530KH40 FPGA. The product decoder easily fits on this FPGA, and enough spare logic is present for the remainder of the communication chain.

Fig. 7 shows the experimental setup used for testing. The coding bank stores a set of encoded noiseless codewords. Unlike the software simulations used in the design of the FEC scheme, we considered an Additive White Gaussian Noise (AWGN) channel and 2-bit Pulse-Amplitude Modulation (4-PAM). The test setup leverages the Nios II soft-core processor and the UART serial interface over JTAG over USB. As shown in the figure, most of the system is run with dedicated hardware blocks and the software application running on the Nios II processor is exclusively used to monitor the on-going testing results. Once it has setup the chain, the software application periodically reads the performance counters, calculates $p$ and BER, and pushes the results over the UART-over-JTAG-over-USB link to a terminal running on the host PC.

Clocked at 50 MHz, the test setup shows an average measured information throughput of 9.98 Gb/s in the regions of interest, equivalent to a coded throughput of 11.98 Gb/s. Fig. 8 shows a comparison of the expected error-correction performance—frame-error rate (FER) on the left and BER on the right—compared to that of the hardware implementation. Software simulations are for a BSC. For the hardware implementation a bank of 64 random codewords generated with the software encoder are modulated on a Gray-coded 4-PAM.
the number of information bits becomes something else than 178$^2$.

Increasing or decreasing the number of performed standard iterations is a straightforward modification of two configuration parameters. It requires that the maximum value of the iteration counter be changed, along with the iteration value at which post processing is applied.

A change of $t$ requires a different decoding algorithm, so the decoder must be completely redesigned.

A change in code length (meaning a different shortening value, but with the same root BCH code) mandates radical changes to all modules of the decoder. It will affect the size of the scratch memory, the number of rows/columns connected to each component decoder, and the structure of the component decoders themselves. While it is true that the decoding algorithm remains the same, since $t$ is not changed, most eBCH decoder modules are code-length specific and fine-tuned to the proposed FEC scheme. The Selectors and Logarithms and Error Locator modules require minor modifications to accommodate the longer code, but Parity and Syndrome multilevel XOR trees must be redesigned, and similarly the bit flipping signal generation algorithm implemented in the Bit flipping and post-processing module.

The proposed decoder architecture relies on $P_c = 13$ component decoders, that are able to achieve the 100 Gb/s information-throughput specifications with a clock frequency of 609 MHz. The number of clock cycles required to decode a $(195, 178)^2$ product codeword can be expressed as follows:

$$\left(\left\lfloor \frac{P_c}{P_l} \right\rfloor + \min \left( P_c - P_l \frac{P_c}{P_l} , P_l \right) \right) \cdot \left\lfloor \frac{195}{P_c} \right\rfloor + (202 - P_c \frac{195}{P_c}) \left(2L - 1\right) \left\lfloor \frac{195}{P_c} \right\rfloor + (2 + 2L)n_p$$

where $P_l$ is the number of 195-bit loading lanes (currently 2), $n_p$ is the number of pipeline stages in the component decoders (currently 6) and $L$ the number of decoding iterations excluding the post-processing iteration (currently 2). Consequently, the decoding process amounts to 193 clock cycles or:

- 111 clock cycles for the loading of the codeword and the concurrent execution of the first half-iteration;
- 21 clock cycles for the following three half-iterations, for a total of 63 clock cycles;
- 18 clock cycles for the post-processing iteration;
- 1 clock cycle to signal the end of the decoding.

In case throughput requirements are lower, or in case the achievable frequency is higher than 609 MHz, the decoder can be redesigned to meet the new specifications. For example, if the decoder was to be implemented with a deep sub-micron technology node, e.g. CMOS 28 nm, an achievable clock frequency of 1 GHz would likely be possible. In this situation, the 100 Gb/s information-throughput constraint would be met whenever the decoding process lasts at most 316 clock cycles. In this case, a higher number of iterations $L$ or a lower number of component decoders $P_c$ might be considered.
VI. CONCLUSIONS

In this work, we have proposed a novel FEC scheme for OTN. It uses product codes with extended-BCH codes as component codes and a post-processing technique that greatly reduces the error floor. The proposed FEC achieves 9.52 dB of NCG at a BER of $10^{-15}$ and 9.96 dB at $10^{-18}$. A low-complexity, high-speed decoder architecture has been designed, tested on FPGA and synthesized in 65 nm CMOS technology: it yields a worst-case throughput of 164 bits/cycle, i.e. an information throughput of 100 Gb/s at 609 MHz, with a gate count of 1.15 million gates. The proposed FEC brings the error-correction performance of hard-decision FECs closer to that of soft-decision FECs. The complexity of the proposed decoder is lower than that of hard-decision decoders in literature, and an order of magnitude lower than the estimated complexity of soft-decision decoders. The 319 ns latency makes the proposed FEC scheme and decoder suitable for low-latency environments like data centers.

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