Failure Analysis of Intelligent Door Lock Master Control Chip

Yang Lin$^{1,2}$, Xia Jiang$^{1,2}$, Li Rong$^{1,2}$, Xiao Shiman$^{1,2}$, Wu Huasheng$^{1,2}$ and Peng Qi$^{1,2}$

$^1$The fifth electronic research institute of MIIT, Guangzhou, China
$^2$Key Laboratory of MIIT for Intelligent Products Testing and Reliability, Guangzhou, China

E-mail: pengqi@ceprei.biz

Abstract. In recent years, smart door locks having password keyboards, fingerprint recognition and communicating function have seen explosive growth. A large number of enterprises engaged in the manufacture of the intelligent door locks, followed by the associated after-sales problems, and the product without power, no reaction phenomenon caused by the failure of master control chip is relatively common, which greatly affects the user experience. In this paper, a mainstream smart door lock products on the market as the research object, a series of failure analysis and root cause search were executed to find the reasons of failure. The research shows that the main reason for the non-power supply and non-response of the intelligent door lock after sale is the fault of the main control chip. The main control chip fails due to the lack of electrostatic protection, which is directly related to the improper production and assembly process.

1. Introduction

For an intelligent product, the result will be catastrophic when the main control chip appears bad contact, burn out and other failure. The quality of intelligent door lock products is closely related to the personal safety of consumers and public safety. Once the main control chip failure, users often can't open the door or locked in the house, it will have a major impact on consumer safety.

At present, China's intelligent door lock market is in the outbreak period, and there are many startups in the industry. Many traditional door lock enterprises lack the necessary electronic design and production-manufacturing in the production process of turning to intelligent door lock. There are many problems and defects in the design, manufacturing and assembly process of master control chip. Therefore, it must attach great importance to the quality and reliability of the master control chip of intelligent door lock products.

The intelligent door locks have many functions and complex manufacturing processes, the corresponding chip failure phenomenon is also more complex [1]. The smart door lock gathers the core technologies such as fingerprint recognition, face recognition and iris recognition, and has developed from the original single-machine lock to the current Internet of things lock. The improvement of chip quality of intelligent products can be carried out through failure analysis after sale. Failure analysis can effectively make up for the quality problems which cannot be solved in reliability test and evaluation, it was very important to improve the reliability of products. Through failure analysis, it is easy to find out the root cause of product quality problems, as well as preventing
similar phenomena from continuing in the subsequent products, and be able to reverse some improvement plans for the design and manufacturing. Based on this, this paper takes a mainstream intelligent door lock sold in the market as the research object. According to its service performance in the market, a variety of failure analysis techniques and means was adopted to carry out the failure analysis and the root cause search of intelligent door lock master control chip, so as to achieve the purpose of improving product quality and reliability.

2. Failure analysis and root cause search

2.1. Sample and failure information collection

As the object of failure analysis, the failure of intelligent door lock has a certain distribution law. The single point time series distribution was performed for the failure data of intelligent door locks in 2019, as shown in Fig. 1. It can be seen that the main control chip failure problem is the most prominent problem of intelligent door lock, and the failure was mainly concentrated in April, May, and June. Therefore, three samples with the typical chip failure phenomenon will be selected as the research target from April, May, and June, respectively. This choice makes the analysis more scientific, and the failure analysis of selected samples will be carried out later. For the convenience of analysis, we numbered the samples before the failure analysis.

![Figure 1. Failure statistical distribution of intelligent door locks based on the single point time series](image)

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![Figure 2. Details of the circuit board of analytical sample](image)

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2.2. Failure analysis process design
Based on the collection and sorting of after-sales failure information of intelligent door lock products, the design and development of intelligent door lock master control chip and the reverse analysis of the manufacturing process were carried out, and the failure analysis process of master control chip was designed [2-3].

1. Recording the characteristics, sources and batches of failed samples, it can avoid confusion between samples;
2. In order to obtain the electrical curve of the product, and observe whether the sample PCB board has broken circuit, broken circuit and leakage, the non-destructive test analysis is in use;
3. Conducting destructive test and analysis on the samples. To check whether the internal structure of the chip is in good condition, whether there are burn marks, and whether the batting line position is abnormal, SEM scanning electron microscope analysis is needed for further in-depth analysis [4-5].
4. The conclusion of failure analysis can be further verified by the comparison and analysis of the samples with the intact samples.
5. Proposing corrective actions. According to the root cause of the fault, the corrective actions is proposed to evaluate the effectiveness of the corrective measures.

2.3. Failure analysis
Combining with micro environmental stress experienced by product service, the influence factors of leading to failure is carried out, such as the worst circuit test and analysis, batch good parts failure implants, the comparison test and diagnosis of production line, etc. The root cause of failure is confirmed based on failure analysis.

2.3.1. Sample appearance inspection
In order to check whether the sample has been damaged in the process of testing, installation, use and after-sales service, the appearance of the sample was first examined, as shown in Fig. 3. Through visual inspection and microscopic observation, it was found that the surface identifier of the sample was clear, and no abnormal phenomena such as bridging and shedding were observed.

![Figure 3. The front view (left) and the back (right) of the sample](image)

2.3.2. Electrical parameter test and analysis
Through the analysis of electrical parameters, it can help confirm the failure mode and the failure control foot position, and identify partial failure mechanism. The schematic diagram of the sample chip is shown in figure 4. According to the failure information of the sample, the electrical function test and the pin direct current characteristic (I-v characteristic) test were carried out on the sample. Through the test, it was found that I-V characteristic curve of Pin14/Pin15 pin to the power supply/ground wire showed short circuit or low resistance characteristics, as shown in figure 4. At the same time, by comparing the previous failure information, it was found that the SoC of the same
model products had the failure phenomenon to Pin14 and Pin15, and the failure rate was about 1%. For this analysis samples, Pin14/Pin15 port is mainly used for communication with other modules in the door lock based on I2C protocol. It is easy to cause the phenomenon of no power supply, keypad and communication failure light after sale if Pin14 and Pin15 go wrong.

![Figure 4. Circuit principle diagram of master control chip](image)

![Figure 5. The I-V characteristic curve between Pin14 pin and GND (left), Pin15 and VDD (right)](image)

2.3.3. X-ray examination (X-ray analysis)

In order to check whether there is any defect or damage inside the sample package, the X-ray system was used to observe whether there are abnormalities in Pin14/Pin15 pin accessories and connecting wires. Typical X-ray morphologies are shown in the following figure 6. As can be seen from figure 6, there are no obvious abnormal morphologies (such as bond wire fracture, short circuit and foreign matter) in the failed sample.
2.3.4. Scanning acoustic microscope examination

In order to understand the interface of different materials inside the failed sample chip, the acoustic microregion imaging analysis of the sample will be conducted by using the scanning acoustic microscope. The interface bonding between the plastic sealant and the chip, the substrate and the plastic sealant, the plastic sealant and the lead frame, etc. will be observed, typical acoustic observations of the sample are shown in Fig. 7. As can be seen from Fig. 7, no obvious stratification was observed in the failure sample, and the connectivity between each layer was relatively good.

2.3.5. Unseal and locate failure

From the previous analysis, it was found that there were no anomalies in other places except Pin14 and Pin15 pin ports. Therefore, it was preliminarily determined that the pin ports of Pin14 and Pin15 of the chip were abnormal. In order to further determine the failure location, the chip package structure will be unsealed. OBIRCH (laser beam resistance anomaly detection method), optical microscope and scanning electron microscope will be used to observe the failure after unsealing and locate the failure point.

After applying voltage to the Pin14 and GND terminals of the sample, it can be seen that there are obvious impedance change points in the Pin14 port area of the chip, as shown in Fig. 8. When applying voltage to Pin14 and VDD terminals, there are also obvious impedance change points in the Pin14 port area. The same impedance change was found when the voltage was applied to the Pin15 terminal as to the VDD and GND terminals.
To further locate the failure point, we conducted the optical microscopy and scanning electron microscopy (SEM) observation, the internal assembly, bonding point and chip structure of the sample were detected at the same time. It can be seen that the glass passivation layer on the chip surface is complete, and the interior is well metallized. However, there were obvious overcurrent damage in Pin14 terminal and Pin15 terminal as shown in Fig. 10. Through SEM analysis, it can be seen that there is a particularly obvious appearance of voltage breakdown crater near these two ends (Pin14 and Pin15), and the crater is not large. This shows that the electrical stress generated by the crater is small, which is similar to the breakdown morphology caused by electrostatic damage [6-7]. At the same time, the morphology features are consistent with the position of the impedance change point observed by OBIRCH, as shown in figure 8 and figure 9. It can be concluded that the short-circuit ports (Pin14 and Pin15) of the chip belong to the fault point, and the fault presents obvious electrostatic voltage breakdown morphologies.
Electrostatic damage is generally directly related to improper electrostatic protection measures in production, assembly, storage and transportation of products. Enterprises should strictly adopt various electrostatic risk control measures in the process of product storage, turnover and transportation to reduce the risk of electrostatic damage.

3. Conclusion
Based on the failure background information, we can infer from the port damage morphology that the Pin14 or Pin15 ports of the chip were broken by voltage, resulting in the port being subjected to EOS overcurrent damage. From the size of the crater and the extent of damage, it can be judged that the electrical stress is not large, which was similar to the common electrostatic damage breakdown.
morphology. It can be concluded that the small electrostatic stress leads to the breakdown of the master control chip, which leads to the product failure.

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