PARIS and ELSA: An Elastic Scheduling Algorithm for Reconfigurable Multi-GPU Inference Servers

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Abstract—In cloud machine learning (ML) inference systems, providing low latency to end-users is of utmost importance. However, maximizing server utilization and system throughput is also crucial for ML service providers as it helps lower the total-cost-of-ownership. GPUs have oftentimes been criticized for ML inference usages as its massive compute and memory throughput is hard to be fully utilized under low-batch inference scenarios. To address such limitation, NVIDIA’s recently announced Ampere GPU architecture provides features to “reconfigure” one large, monolithic GPU into multiple smaller “GPU partitions”. Such feature provides cloud ML service providers the ability to utilize the reconfigurable GPU not only for large-batch training but also for small-batch inference with the potential to achieve high resource utilization. In this paper, we study this emerging GPU architecture with reconfigurability to develop a high-performance multi-GPU ML inference server. Our first proposition is a sophisticated partitioning algorithm for reconfigurable GPUs that systematically determines a heterogeneous set of multi-granular GPU partitions, best suited for the inference server’s deployment. Furthermore, we co-design an elastic scheduling algorithm tailored for our heterogeneously partitioned GPU server which effectively balances low latency and high GPU utilization.

I. INTRODUCTION

Several hyperscalers are now offering “MLaaS (Machine Learning as a Service)” from cloud datacenters using off-the-shelf CPUs, GPUs, or even custom designed accelerators for ML [1], [2], [3]. For end-users utilizing MLaaS for inference, providing real-time response with strict SLA (service-level agreement) guarantee is of utmost importance. From a MLaaS provider’s perspective however, achieving high server resource utility and system throughput is crucial as it helps optimize the total-cost-of-ownership (TCO) of maintaining the consolidated/virtualized datacenter infrastructure.

Unlike the throughput-bound ML training algorithm, inference is a latency-sensitive workload which favors inference purpose built ML accelerators [3], [4], [5] or even latency-optimized CPUs [6], [7]. GPUs on the other hand have generally been considered ill-suited for latency-critical inference servers as its massive computational throughput and memory bandwidth is hard to be fully utilized under low-batch inference scenarios. Indeed, multiple prior literature motivated the need for inference-optimized ASIC/FPGA solutions [8], [9], [10], critiquing GPUs for its low “effective” throughput and low utilization when deployed for inference. To address such limitation, NVIDIA’s recently announced Ampere architecture provides a feature named Multi-Instance GPU (MIG) that enables the compute and memory resources of one large GPU to be reconfigured into multiple small or medium sized “GPU partitions”. As the partitioned GPUs are virtualized and can be handed over to multiple VMs using hardware support for SR-IOV [11], [12], each GPU partition can function as a standalone GPU with performance isolation guarantees. Such feature can come in handy for MLaaS providers as the reconfigurable GPU can be utilized not only for training (i.e., configured as one big GPU) but also for low-batch inference with the potential to achieve high resource utility (i.e., partitioned into multiple small/medium sized GPUs that suits application’s characteristics).

Given such landscape, a key objective of our study is to study this emerging GPU architecture with reconfigurability to develop a high-performance multi-GPU ML inference server. We first start by characterizing the pros/cons of the reconfigurable GPU when statically partitioned into a homogeneous set of fixed size small (or medium) GPUs. Our characterization reveals several limitations of a homogeneously partitioned multi-GPU inference server. As we explore in this work, determining the optimal GPU partition size requires careful consideration of not just the target ML application’s unique compute/memory needs, but also the input query size (i.e., batch size). However, tackling such multi-dimensional optimization problem via a “one-size-fits-all” approach (i.e., blindly partitioning the reconfigurable GPU into a statically fixed granularity) is not practical as the system architect must painstakingly explore the wide design space of GPU reconfigurability, batch size, and DNN models altogether, leading to suboptimal design decisions and incurring either significant SLA violations or GPU underutilization.

To this end, we propose a sophisticated yet practical Partitioning Algorithm for Reconfigurable multi-GPU Inference Servers (PARIS) that systematically determines a heterogeneous set of multi-granular GPU partitions in a user-transparent manner, best suited for the inference server’s deployment scenario. Compared to a statically partitioned homogeneous GPU inference server, PARIS presents rich opportunities to minimize GPU underutility while still providing enough computation power to satisfy SLA. We also present an...
**ELastic Scheduling Algorithm (ELSA)**, co-designed with our PARIS, which is capable of exploiting the unique heterogeneous compute capabilities of our proposed multi-GPU server for scheduling decisions, effectively balancing low latency and high GPU utilization.

### II. BACKGROUND

#### A. Training vs. Inference in Machine Learning

A deep neural network (DNN) application must first be trained to be ready for deployment in inference use-cases. Under the context of training, the input training dataset is readily available before the learning process is initiated, so establishing a large enough input batch size is trivial (e.g., the input batch size for training can be up to several hundreds to even thousands of inputs per batch [13], [14], [15]). In contrast, batching multiple inputs for inference is challenging as the inference server receives DNN inference queries at varying rates, a function determined by what time of the day the queries are being received, how much popular the deployed service is, and more. In general, several prior work observed that the input query arrival rate for web-based services follow a Poisson distribution with the query size (i.e., batch size) following a log-normal distribution [16], [17], [18], [19]. A high-performance ML inference server must therefore carefully consider both query arrival rate and query size distributions and be provisioned with sufficient amount of compute and memory resources to satisfy SLA.

#### B. GPUs for Training vs. Inference

GPUs have traditionally been optimized in a throughput-centric fashion, employing an area-efficient SIMD-based many-core architecture design backed with bandwidth-optimized memory solutions like GDDRx or HBM [20], [21]. This is in stark contrast to latency-optimized CPUs where the primary design objective is to minimize latency using sophisticated branch predictors, prefetchers, large on-chip caches, etc. Consequently, throughput-hungry ML training algorithms are well suited for GPUs as it can provide much higher throughput (per area) vs. CPUs. Inference however is a latency-critical workload, favoring purpose built ML accelerators optimized for latency or even CPUs over GPUs. As discussed in Section II-A, the batch size of an inference query is typically orders of magnitude smaller than those for training. As a result, the resource demands of inference are generally not high enough to fully saturate the massive compute/memory throughput of GPUs. Inference servers therefore can significantly suffer from low GPU utilization, making it a less favorable choice for TCO-optimized datacenters.

To remedy such situation, vendors have introduced several lightweight, inference-purposed GPUs to the market which are equipped with a (relatively) smaller compute capability (e.g., NVIDIA M4/T4 [22], [23]). Employing these small GPUs for inference servers however has an important tradeoff as it reduces the compute “density” of the inference server, proportional to the performance difference between large vs. small GPUs. Recently announced GPUs therefore are architected with “reconfigurability” that enables them to be setup as one large, monolithic GPU or be partitioned into multiple smaller GPUs, the granularity of which can be chosen by system architects as appropriate per application needs. Below we detail the baseline reconfigurable GPU explored in this paper.

#### C. A “Reconfigurable” GPU Architecture

As this paper utilizes NVIDIA’s MIG-enabled GPU as a vehicle to construct a reconfigurable multi-GPU inference server, we use NVIDIA’s A100 GPU [24] to describe a modern SIMT (single-instruction multiple-thread) based GPU architecture. In the remainder of this paper, we use terminologies defined in NVIDIA’s CUDA programming language [25].

**GPU hardware architecture.** Figure 1 provides an overview of our baseline GPU architecture. The most fundamental computational building block of a GPU is an SM (streaming multiprocessor), which is a SIMD vector processor (but programmed using the SIMT programming semantics which is different than traditional vector programming). Each SM contains a large register-file to enable GPUs to employ massive number of threads to concurrently execute with fine-grained, hardware-level context switching for latency hiding. An SM also contains an L1 cache and scratchpad memory that can capture high-locality datasets within the vicinity of our SIMD processor. Multiple SMs are grouped into a cluster, which is called a GPC (Graphics Processing Cluster) and the SMs within the same GPC share the communication ports to the NoC (network-on-chip). As GPUs are throughput-optimized processors, the NoC is implemented using a high-breadth crossbar. The crossbar that interconnects multiple GPCs are utilized to access the L2 cache/DRAM slices, which allows an L2 cache miss to be routed to the corresponding off-chip memory channel to access DRAM.

**GPU software architecture.** CUDA employs the SPMD (single-program multiple-data) programming model, where a single program (the kernel) gets executed by all the threads that are spawned for execution. The programmer is expected to group the threads into a granularity called thread-blocks or concurrent thread-arrays (aka CTAs) and the hardware-level scheduler is in charge of scheduling CTAs to the SMs for execution. Once a CTA is scheduled to a given SM, it stays there until the entire program’s execution is finalized (i.e., a scheduled CTA does not migrate to other SMs).
Adding reconfigurability to the GPU. In A100, the GPCs (compute) and the L2/DRAM slices (memory) are utilized as basic building blocks to architect a GPU with reconfigurability. Specifically, a GPU partition can be defined at the granularity of a GPC, so A100 which contains seven GPCs can be configured up to seven GPU partitions (each partition having just a single GPC worth of compute capability). Figure 2 illustrates valid GPU partition combinations available in A100, allowing it to be (re)configured into one big GPU (7 GPCs) or multiple small (1 or 2 GPCs) or medium (3 or 4 GPCs) sized GPUs. The reconfigurable GPU is provided with the proper architectural support for SR-IOV (single root input/output virtualization), so each GPU partition is given the necessary hardware-level features to function as a true “standalone” GPU device, i.e., each GPU partition can be handed over to a process or a VM, with performance isolation guarantees.

D. Related Work

Utilizing multi-GPU systems for ML inference and training has been studied extensively in prior literature. DjiNN and Tonic [26] is one of the early works on ML inference servers based on a homogeneous set of GPU devices, presenting an open-source software infrastructure for deploying ML services at datacenters. Recent ML frameworks like TensorFlow Serving [27], AWS SageMaker [28], and NVIDIA Triton Inference Server [29] are also dedicated software packages intended to ease the development of ML inference servers. In terms of ML training, PipeDream [30], GPipe [31], and Megatron-LM [13] (among many others) utilize multi-GPU systems for training large-scale ML models. None of these prior studies utilize the reconfigurable GPU we explore in this paper, rendering the key contributions of our work stand on its own.

In terms of leveraging the idea of heterogeneous computing for ML inference, DeepRecSys [17] employs a heterogeneous CPU-GPU system for servicing recommendation services. MOSAIC [32], uLayer [33], and JointDNN [34] explore the possibility of utilizing the heterogeneous compute capabilities within mobile devices (e.g., CPU, GPU, NPUs, DSPs) for accelerating ML inference. These prior art primarily focus on partitioning the DNN model and scheduling them across the heterogeneous processing units. Our work on the other hand focuses on the partitioning of the reconfigurable GPU hard-
1×1 convolutions as well as depthwise filters. Consequently, ResNet experiences a more steep increase in latency when the GPU partition size is decreased because it’s performance becomes more sensitive to the (relatively) smaller computation power of GPU(1,2) than the lightweight MobileNet. The same principle holds for the compute-intensive BERT, exhibiting the highest increase in latency when smaller GPU partition sizes are employed.

Overall, we conclude that determining an optimal partitioning granularity for reconfigurable GPUs requires careful consideration of each model’s unique algorithmic properties and its compute/memory demands. For instance, our experiment in Figure 3 shows that the optimal partitioning point for ResNet is around GPU(3) as it does not incur significant increase in latency while the achieved GPU utilization is reasonably high. The sweet spot for MobileNet on the other hand is GPU(1) as it achieves approximately 2× higher GPU utility while “only” experiencing a latency increase of 23% vs. GPU(3). In general, our characterization demonstrates the challenges and pitfalls of a “one-size-fits-all” approach, i.e., partitioning the reconfigurable GPU into a homogeneous set of GPU partitions, as no single partitioning granularity could universally fulfill the various DNN model’s computation demands as well as its individual latency goals.

B. Effect of Batch Size on Latency & Server Utility

Along with the individual DNN’s model specific properties, the batch size of a query is another key factor that affects GPU utilization and latency, posing another challenge in finding the optimal partitioning granularity. Inference queries with large batch sizes help increase GPU utilization as it better exploits parallelism and locality across the batched inputs. On the other hand, large batches increase the amount of computations so it can adversely affect the level of SLA violations when the latency is increased to an unacceptable level.

Figure 4 shows the effect of batch size on our reconfigured GPU’s compute utilization and average latency. In general, all models over all GPU partition sizes experience a monotonically increasing GPU utilization and latency as the batch size is increased. However, once the GPU utilization reaches a plateau around 80 – 90%, the latency increases much more rapidly with larger batch sizes. This is because executing with a larger batch size only helps improve GPU utilization incrementally when the utility already neared its peak value, while the proportionally increased computation directly translates into a linear increase in execution time. We hereafter refer to this point as the “max batch size at the knee of the latency curve”, or MaxBatch_knee in short (e.g., denoted as blue diamond shapes for GPU(1) in Figure 4). Naturally, the MaxBatch_knee differs significantly across different GPU partition sizes or DNN model types, with small GPU partitions generally having a smaller MaxBatch_knee while larger GPU partitions having a larger MaxBatch_knee.

Overall, large models like BERT are able to achieve high GPU utilization under small GPU partitions even when the batch size is small. Therefore, executing large batches of BERT on a small GPU(1) is likely to be a poor scheduling decision as the benefits in GPU utility is minimal while the penalty in latency is high. GPU(1) however is a reasonable design point for the lightweight MobileNet as it does a much better job in handling medium-to-large batches, achieving high GPU utility while minimally sacrificing latency.

Given such, one might choose to utilize the results in Figure 4 to manually determine a model specific and batch size specific partitioning point that balances GPU utilization and latency. Unfortunately, the size of an input batch can vary significantly per inference server’s average query size distribution (i.e., a log-normal distribution for datacenter web-servers, Section II-A). As a result, a “one-size-fits-all”, homogeneous partitioning strategy (even if it is hand-tuned...
on a per-model basis) again is not able to robustly capture the various query sizes (i.e., batch sizes) routed to the inference servers.

C. Our Goal: A Heterogeneously Partitioned GPU Inference Server and Its Scheduling Algorithm

A “heterogeneous” multi-GPU ML inference server. Overall, our characterization revealed two key challenges with a homogeneously partitioned multi-GPU inference server. First, a statically chosen, fixed partitioning granularity is not able to efficiently capture the model specific computation diversity of DNNs, failing to achieve low latency and high GPU utilization simultaneously. Second, the dynamically varying input batch size poses another problem because a rigidly configured, single-granular GPU partition size cannot flexibly adapt to the varying computation requirements of input batches. Rather than having multiple, identical instances of a single GPU partition size (e.g., six instances of GPU(1) or three instances of GPU(2)), our proposed Partitioning Algorithm for Reconfigurable multi-GPU Inference Servers (PARIS) partitions the reconfigurable GPUs into a heterogeneous set of GPU partitions. As we detail in the next section, PARIS systematically evaluates both the target model’s inference properties and the input query size distribution to derive a fruitful set of multi-granular partitioning sizes as well as the number of instances to deploy for each partition size. The collection of GPU partitions with heterogeneous compute capabilities enable our proposed ML inference server to flexibly respond and adapt to the model specific compute demands of DNNs as well as the dynamically changing query sizes.

A “heterogeneity-aware” scheduling algorithm. As PARIS enables the inference server’s compute capability to become diverse, a scheduling algorithm that best exploits such heterogeneity is in need. Current state-of-the-art multi-GPU inference servers (e.g., NVIDIA Triton Inference Server [29]) employ a first-idle first-serve (FIFS) scheduling policy where the newly inserted inference query is scheduled to an idle GPU available in the system. As depicted in Figure 5(a), an FIFS scheduling policy is both intuitive and cost-effective for homogeneous multi-GPU system to minimize the number of idle GPUs and reduce average latency. Under our proposed, heterogeneous multi-GPU system however, FIFS can lead to suboptimal scheduling decisions as it fails to accommodate the diverse computation power of our GPUs. In Figure 5(b), we assume a heterogeneously partitioned multi-GPU server with two large and one small GPU. When query $A$ arrives to the server, the FIFS scheduler chooses the small GPU for execution as it is the only idle GPU available. Because the idle GPU is a small one, the latency to service this query is longer than what would have been experienced had the idle GPU been a large one, leading to an SLA violation. Consequently, a better scheduling decision would have been to wait until any one of the large GPUs complete its current query and schedule query $A$ there instead. The baseline FIFS however is unaware of the heterogeneous computing power in our PARIS server, leading to longer latency and aggravating overall performance. We propose an ELastic Scheduling Algorithm (ELSA) that is designed with heterogeneity-awareness in mind, maximally exploiting the potential of the heterogeneous computing power of our PARIS multi-GPU system. We now detail our two proposals, PARIS and ELSA.

IV. PROPOSED ARCHITECTURE: PARIS AND ELSA

A. High-level Overview

Figure 6 provides an overview of a ML inference server employing our two proposals, PARIS and ELSA. In this section, we first make a case for partitioning the reconfigurable GPUs heterogeneously using PARIS (Section IV-B). PARIS utilizes both the model specific inference properties (e.g., latency vs. GPU utility under a target GPU partition size) and the batch size distribution information to systematically generate a heterogeneous set of partitioning granularities as well as the number of instances to deploy for each partition. Our second proposition ELSA is a high-performance scheduling algorithm co-designed with our heterogeneous PARIS inference server (Section IV-C). ELSA uses a heterogeneity-aware, inference latency prediction model to estimate a given query’s SLA slack and determine which among our heterogeneous GPUs are best suited to service the query. As we detail in this section, ELSA’s heterogeneity-awareness helps maximize server utilization while minimizing SLA violations.

B. PARIS

We first discuss the key insights that motivate our PARIS, followed by discussions on its design and implementation.
Key observations. Our characterization in Section III-B revealed that the max batch size at the knee \( \text{MaxBatch}_{knee} \) varies significantly across different GPU partition sizes, with smaller (larger) GPU partitions having smaller (larger) \( \text{MaxBatch}_{knee} \). Based on this characterization study, we make several key observations that motivate PARIS as follows:

1) For any given GPU partition size, having it handle batch sizes larger than its \( \text{MaxBatch}_{knee} \) is not cost-effective as the gains in GPU utilization is minimal while the penalties in latency can be significant.

2) Assuming the input batch size to execute is smaller than the \( \text{MaxBatch}_{knee} \) for a given model, small (medium) GPU partitions are generally more cost-effective when handling small (medium) batch sizes than large GPU partitions as it can achieve high GPU utility while not sacrificing latency.

3) Similarly, large GPU partitions are efficient when handling large batch sizes as it does not incur too high of a latency overhead (thanks to its high computation power) while still achieving high GPU utilization. While scheduling small batches (smaller than the \( \text{MaxBatch}_{knee} \) to large GPU partitions is certainly feasible, it can suffer from low GPU utilization. Consequently, small(er) batches are best when delegated to small(er) GPU partitions rather than scheduling them to large(r) GPUs.

Partitioning with both model specific properties “and” batch size distribution in mind. Figure 7 visualizes our key approach that incorporates both the model specific latency properties as well as the varying input batch sizes as part of our partitioning algorithm. We first conduct a one-time profiling of the [GPU utilization vs. latency] curve per each GPU partition size, which was also used in our characterization in Figure 4. Using the characterization results, we are able to derive each GPU partition’s \( \text{MaxBatch}_{knee} \) for a target DNN model (B1/B2/B3/B4/B5 for the five GPU partition sizes in Figure 7(a)). These \( \text{MaxBatch}_{knee} \) values are then utilized to split the batch size distribution into multiple, non-overlapping segments of batch size ranges ([B0-B1], [B1-B2], ...), where the number of segments matches the number of GPU partitioning granularities we consider in PARIS (Figure 7(b)). The batch size distribution is virtually a probability density function (PDF) that models the likelihood of a particular batch size to be queried to the inference server, one which is known to follow a log-normal distribution in web-services (Section II-A). This function can readily be generated in the inference server by collecting the number of input batch sizes serviced within a given period of time, which PARIS can utilize as a proxy for the batch size distribution PDF. Each of the partitioned batch range segments are then assigned to its dedicated GPU partitions one-by-one, the \( n \)-th smallest batch range segment assigned to the \( n \)-th smallest GPU partition (Figure 7(b)).

The key benefits of our partitioning mechanism is clear. Because the profiled, per-model characterization curves (Figure 4) are used to derive the \( \text{MaxBatch}_{knee} \) values, PARIS can accommodate the model specific utilization-vs-latency trade-off properties into our partitioning algorithm. Additionally, each GPU partition now has a dedicated batch range segment to service that best suits its compute capabilities (which is governed by the batch size distribution and the \( \text{MaxBatch}_{knee} \) values), so PARIS can better handle the diverse query sizes routed to the inference server with high utilization using its heterogeneous GPU partitions.

Determining the number of partition “instances”. As PARIS has now determined which batch size range the partitioned GPUs will be handling, a derivation of how many instances of these GPU partitions should be deployed is required. Two factors must be considered in determining the optimal number of instances to deploy: 1) the likelihood of a particular batch size to be queried to the inference server (which is reflected in the batch size distribution PDF), and 2) the effective inference throughput of a particular GPU partition when handling its responsible batch range segment (which is derived using our profiled characterization graph in Figure 4, i.e., number of queries serviced/second). We use Figure 8 as a driving example to explain our mechanism that derives the number of instances required per each
partition size. We assume that up to two GPU partition sizes are available, each of which has a MaxBatch\textsubscript{knee} value of B1(=2) and B2(=4), respectively. Therefore, the small (large) GPU covers batch size 1/2 (3/4), which accounts for 20+20=40\% (40+20=60\%) of the inference query traffic as estimated through batch size distribution PDF (Figure 8(a)). Consider the small GPU which is measured and estimated (through profiling) to provide an effective inference throughput of 40 and 20 queries/sec for batch size 1 and 2, respectively (Figure 8(b)). Assuming the total number of queries the inference server needs to service is 100, we can expect 20 queries of batch size 1, 2, and 4 each, and 40 queries of batch size 3. Now, because the effective throughput for batch size 1 is two times higher than that for batch size 2 (40 vs. 20 queries/sec), we virtually need 0.5 (=20/40, i.e., number of queries to be serviced for a given batch/effective throughput for that batch) small GPU to sufficiently serve batch 1 queries and another 1 (=20/20) small GPU to service batch 2 queries, requiring 1.5 (=0.5+1.0) small GPUs in aggregate. Similarly, a total of 2.3 large GPUs is in need to fully service batch 3/4 (Figure 8(b)). The ratio of (1.5:2.3)=(number of small GPU instances: number of large GPU instances) can therefore be utilized to determine by what fraction should PARIS divide up the available compute resources within our multi-GPU server (i.e., total number of GPCs per GPU × number of GPUs per server). Below we detail the implementation aspects of PARIS.

Implementation. Algorithm 1 is a pseudo-code of PARIS, putting all of the pieces discussed in this subsection together. The three most important input data to PARIS is 1) the PDF of batch size distribution (Dist[], line 3), 2) a GPU partition’s compute utilization at a particular batch size (Util[], line 4), and 3) the effective inference throughput of a particular GPU partition when executing a particular batch size (Throughput\textsubscript{k,b}, line 5). Assuming there are k possible GPU partition sizes available within the reconfigurable GPU (GPC[], line 2), PARIS first initiates a one-time derivation of the MaxBatch\textsubscript{knee} for each of the k partition sizes using the profiled [GPU utilization-vs-latency] curve (line 6-9). For clarity of explanation, we assume the batch size that a given GPU partition starts exceeding 80\% GPU utilization is the MaxBatch\textsubscript{knee} value, which is stored into B\textsubscript{k} (line 8). Once B\textsubscript{k} is derived, PARIS uses the set of MaxBatch\textsubscript{knee} values to determine the ratio between each GPU partition’s required number of instances (line 10-16), as explained through the example in Figure 8. Finally, the derived relative ratio is used to determine the absolute number of instances a particular GPU partition size should be instantiated with (line 17-26), which is utilized to configure our PARIS-enabled heterogeneous multi-GPU server.

C. ELSA

Once PARIS is applied to our reconfigurable multi-GPU system, the scheduler is given a selection of heterogeneous computing devices it must judiciously utilize for maximum efficiency. As discussed in Section III-C (Figure 5), the baseline FIFS scheduling algorithm fails to accommodate the diverse compute capabilities of our heterogeneously partitioned PARIS system, leading to aggravated latency and GPU utility.

Our ELSA is designed with “heterogeneity-awareness” in mind and consists of three major components:

1) First, we propose a profiling-based approach in estimating a DNN model inference query’s execution time when scheduled to a particular GPU partition.
2) The estimated DNN execution time is then used to calculate the remaining SLA slack time for that query.
3) Finally, the SLA slack time is utilized by our scheduler to dynamically judge which among the heterogeneous GPU partitions would this query be best served by, with minimizing SLA violations as a topmost scheduling objective.

We now detail each of these three components below.

Estimating DNN model execution time via profiling. A key observation of our profile-based approach is that a DNN model’s inference execution time over a target GPU architecture is highly deterministic and predictable. Prior work [35], [36], [37], [38], [39] similarly observed the deterministic nature of DNN inference latency and ELSA’s DNN model execution time estimator leverages such property for slack estimation. Specifically, we conduct an exhaustive, one-time profiling of a target DNN model’s execution time over a target GPU partition size and all possible batch sizes. The latency to collect this information for all the design points we consider is approximately 5 minutes, which is a one-time cost and

Algorithm 1 PARIS

1: procedure PARITIONING\_ALGORITHM()
2: \(\text{GPC}[k] = \text{[Possible configurations of GPU partition size]}\)
3: \(\text{Dist}[\text{b}_1, \text{b}_2, ..., \text{b}_n] = \text{[b}_1, \text{b}_2, ..., \text{b}_n] \) (0 ≤ \(\text{p}_\text{n} \leq 1\))
4: \(\text{Util}_\text{k}[\text{b}_1, \text{b}_2, ..., \text{b}_n] = [\text{u}_1, \text{u}_2, ..., \text{u}_n] \) (0 ≤ \(\text{u}_n \leq 1\))
5: \(\text{Throughput}_\text{k,b} = \text{Throughput of GPU configuration k in batch size b}\)
6: \> Step A: Find MaxBatch\textsubscript{knee} under each GPU partition (one-time cost)
7: \> for \(k = 1 \) to size(GPC) do
8: \> Find \(B_k\) that Util\textsubscript{k}[B_k] ≥ 0.8
9: \> end for
10: \> Step B: Derive the relative ratio of GPU partition instance numbers
11: \> for \(k = 1 \) to size(GPC) do
12: \> \(R_k \leftarrow 0\)
13: \> for \(b = B_k - 1 \) to \(B_k\) do
14: \> \(R_k \leftarrow R_k + \text{Throughput}_\text{k,b}\)
15: \> end for
16: \> end for
17: \> Step C: Determine the absolute number of GPU partition instances
18: \(\text{sum}_R \leftarrow 0\)
19: \> for \(k = 1 \) to size(GPC) do
20: \> \(\text{sum}_R \leftarrow \text{sum}_R + (\text{GPC}[k] \times R_k)\)
21: \> end for
22: \(C = \left(\text{Total number of available GPCs}\right)_{\text{mp}}\)
23: \> for \(k = 1 \) to size(GPC) do
24: \> \(N_k \leftarrow C \times R_k\)
25: \> end for
26: return \([N_1, N_2, ..., N_k]\)
27: end procedure
is amortized over all future inference query services. The resulting profiled data is stored as a two-dimensional lookup table that is indexed using (GPU partition size, batch size) which returns the (profiled) DNN execution time. Because the lookup table separately keeps track of the profiled DNN execution time across different GPU partition sizes, ELSA is able to accommodate the unique compute capabilities of PARIS’s heterogeneous devices into its scheduling algorithm. Below we refer to the estimated DNN execution time via our profiling-based lookup table as $T_{\text{estimated}}$.

**SLA slack time prediction.** Providing fast responsiveness is of highest importance for end-users, so MLaaS providers have strict SLA targets to satisfy to meet QoS requirements. ELSA utilizes our DNN execution time estimator to predict how much slack a particular query has left until violating its SLA target (if any) over a target GPU partition. Equation 1 and Equation 2 summarize our SLA slack prediction model:

$$T_{\text{wait}} = \sum(T_{\text{estimated,queued}}) + T_{\text{remaining,current}}$$  \hspace{1cm} (1)

$$SLA\ slack = SLA_{target} - \alpha(T_{\text{wait}} + \beta \cdot T_{\text{estimated,new}})$$  \hspace{1cm} (2)

Whenever a new service query is received at the server, ELSA first calculates how much time this new query must wait inside a target GPU partition until it gets a chance to be serviced ($T_{\text{wait}}$, Equation 1). As depicted in Figure 9, all GPU partitions have its local scheduling queue that buffers all the queries yet to be executed by the GPU. Consequently, $T_{\text{wait}}$ can be estimated by calculating 1) the total amount of DNN model execution time expected to elapse when all the queries buffered inside the scheduling queue are fully executed ($\sum(T_{\text{estimated,queued}})$), and 2) the remaining DNN model execution time of the query currently being executed by the GPU ($T_{\text{remaining,current}}$). Using our profiling-based DNN execution time lookup table, ELSA can easily derive $\sum(T_{\text{estimated,queued}})$. As for $T_{\text{remaining,current}}$, we employ a timestamp that starts ticking whenever a new query starts execution on a GPU, which we can utilize to measure how much execution time has elapsed since it started executing ($T_{\text{elapsed,current}}$ in Figure 9). Because $T_{\text{estimated,curr}} = (T_{\text{elapsed,current}}+T_{\text{remaining,current}})$, ELSA uses the value of $T_{\text{elapsed,curr}}$ to subtract it from the estimated end-to-end execution time of the query currently executing on the GPU ($T_{\text{estimated,curr}}$) to derive $T_{\text{remaining,curr}}$, allowing us to derive $T_{\text{wait}}$.

As the query’s total wait time inside the server ($T_{\text{wait}}$) counts against SLA, our slack estimation model subtracts this amount from the model specific SLA target ($SLA_{target}$). Additionally, the estimated DNN model execution time of the new query ($T_{\text{estimated,new}}$) should also be accounted for when estimating the remaining SLA slack. As a result, $T_{\text{estimated,new}}$ is also subtracted from the SLA target to derive the final estimated SLA slack remaining for the new query (Equation 2). Note that $\alpha$ and $\beta$ are configurable parameters we employ to tune the SLA slack predictor’s performance in accordance to the unique server environment ELSA is being deployed at.

**Implementation.** With our SLA slack predictor in place, ELSA is able to quantify which among the heterogeneously partitioned GPUs are able to service the subject query without SLA violations (if it is at all possible). Algorithm 2 is a pseudo-code of ELSA, which goes through two primary steps. During the first step, we iterate through all available GPU partitions and calculate the SLA slack had the subject query been scheduled to the subject GPU partition (line 2-9). Note that our scheduling algorithm iterates through the smaller GPU partitions first (line 3-4), prioritizing the scheduling of new queries to smaller GPU partitions if there are multiple GPU partitions that satisfy SLA (line 5-7). This is because, assuming the SLA slack is large enough, servicing a query using a smaller GPU partition is *always* beneficial from a GPU utilization perspective, i.e., if the same query is executed on a larger GPU, it is likely that the resulting GPU utilization will be lower than what it would have been had it executed on a smaller GPU.

In the case where none of the GPU partitions are currently able to satisfy SLA for the new query, we schedule this query to a GPU partition that will take the least amount of service time (line 10-21). As the chances of this new query to fulfill SLA is low, we empirically find that minimizing its presence inside the inference server (i.e., by servicing it as quickly as possible) also minimizes the deteriorating effects it has on other queries that can still satisfy SLA.

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**Algorithm 2 ELSA**

1: procedure ELASTIC_SCHED_ALGORITHM()  
2:  \hspace{1cm} \triangleright Step A: Schedule new query if the GPU partition can satisfy SLA  
3:  \hspace{1cm} Sort GPU partitions in ascending order of partition size  
4:  \hspace{1cm} for each GPU partition $G$ do  
5:  \hspace{2cm} if $SLA > \alpha \times (T_{\text{wait}} + \beta \cdot T_{\text{estimated,new}})$ then  
6:  \hspace{2cm} \hspace{1cm} Schedule query to GPU partition $G$  
7:  \hspace{2cm} \hspace{1cm} return  
8:  \hspace{2cm} end if  
9:  \hspace{2cm} end for  
10:  \hspace{1cm} \triangleright Step B: If Step A failed, schedule query to the GPU partition that can service the new query the fastest  
11:  \hspace{2cm} $t_{\text{min}} \leftarrow \text{INT}_\text{MAX}$  
12:  \hspace{2cm} $G_{\text{min}} \leftarrow -1$  
13:  \hspace{2cm} for each GPU partition $G$ do  
14:  \hspace{2cm} \hspace{1cm} if $t_{\text{min}} > T_{\text{wait}} + T_{\text{estimated,new}}$ then  
15:  \hspace{2cm} \hspace{2cm} $t_{\text{min}} \leftarrow T_{\text{wait}} + T_{\text{estimated,new}}$  
16:  \hspace{2cm} \hspace{2cm} $G_{\text{min}} \leftarrow G$  
17:  \hspace{2cm} \hspace{1cm} end if  
18:  \hspace{2cm} end for  
19:  \hspace{2cm} Schedule query to GPU partition $G_{\text{min}}$  
20:  \hspace{2cm} return  
21: end procedure
Figure 10 provides an illustrative example on the advantages of our heterogeneity-aware ELSA vs. FIFS. As depicted, FIFS fails to realize that query A can lead to significantly longer latency when executed on the small GPU partition, thus violating SLA. In contrast, ELSA uses our SLA slack predictor to acknowledge the potential of such hazardous situation and instead decides to schedule this query to the large GPU partition, avoiding SLA violations.

V. METHODOLOGY

Benchmarks. We study five DNN models used for computer vision (ShuffleNet [40], MobileNet [41], ResNet [42]), natural language processing (BERT [43]), and automatic speech recognition (Conformer [44]). We chose these workloads as they exhibit different levels of compute-intensity (i.e., low (ShuffleNet, MobileNet), medium (ResNet, Conformer), and high (BERT)), thus enabling us to explore the sensitivity of PARIS and ELSA under diverse DNN model’s unique compute/memory requirements.

Query size distribution, query arrival rate. The size of a query determines the input batch size for an inference. Prior work [17], [18], [19] observes that the query size distribution follows a log-normal distribution. Therefore, we model our batch size distribution PDF to follow a log-normal distribution with a batch size ranging from 1 to 32 in our default configuration. In terms of query arrival rates, we employ MLPerf inference benchmark’s recommended Poisson distribution for modeling the rate at which a new query arrives to the inference server. In Section VI-C, we evaluate the sensitivity of PARIS and ELSA under different batch size distributions.

Software. We implemented the software runtime system of our multi-GPU inference server by heavily modifying Facebook’s open-sourced DeepRecInfra [45], a software frame-work that enables the modeling of at-scale datacenter environment’s query size distribution, query arrival rates, and etc (which is configured as discussed above). Our ML inference server is setup on top of Ubuntu 18.04 and PyTorch 1.7.1 backed with CUDA 11.1 and cuDNN 8.0.

Hardware. We conduct our experiments on an Amazon EC2 p4d instance (p4d.24xlarge), which contains 8 NVIDIA A100 GPUs, 96 vCPUs, and 1152 GBs of host memory. As each A100 contains 7 GPCs (Section II-C), a max total of (7 x 8)=56 GPCs can be utilized by PARIS to allocate the appropriate number of GPCs per each GPU partition and instantiate them in our inference server. Note that configuring a homogeneously partitioned multi-GPU server faces several challenges under some of the GPU partition granularities because of the odd-numbered 7 GPCs available per each A100 GPU. For instance, when seeking to configure a homogeneous server with GPU(4), a single A100 can only instantiate one instance of GPU(4) and must leave the remaining 3 GPCs idle. Consequently, the evaluation section (Section VI) primarily focuses on GPU(1,2)/GPU(3)/GPU(7) as the partitioning granularity when studying homogeneous servers configured using small/medium/large sized GPUs, respectively. Below we detail how the number of instances for each GPU partitions is configured for homogeneous and heterogeneous servers.

Configuration of homogeneous vs. heterogeneous GPU partitions.

Table I summarizes our studied server configurations for the five DNN models. There are several things worth clarifying in our evaluation settings and we use the configurations of MobileNet/ResNet/BERT to highlight these points. First, in most of our experiments, we were not able to fully utilize the max 56 GPCs because of the limited number of ways we can practically partition the A100 GPUs while allowing all homogeneous GPU(1,2)/GPU(3)/GPU(7) based servers to use the same number of GPCs (e.g., 56 and 28 GPCs cannot be evenly divided with GPU(3)). Second, note how the total number of GPCs utilized for MobileNet is smaller than those used for ResNet/BERT. We observe that MobileNet’s (relatively) short DNN execution time makes the “total of 48 GPCs, 48 instances of GPU(1)” design point to become completely bottlenecked by the frontend of the inference server (which supplies input queries to the GPUs) because the backend GPU workers consume the incoming queries at a much higher throughput than the queries supplied to the GPUs. Such unbalanced system design point defeats the purpose of comparing different homogeneously partitioned server design points vs. our proposal. Therefore, MobileNet is studied with max 24 GPCs (a design point that all homogeneous servers do not experience the aforementioned frontend bottleneck) for all homogeneous server configurations (with the exception of GPU(7)) as well as PARIS. Because the max 24 GPCs in MobileNet cannot be evenly partitioned using GPU(7), we employ the closest number 28 GPCs (4 instances of GPU(7)) as the homogeneously partitioned large GPU server. Same principle holds for ResNet’s GPU(7) setting.
TABLE I: The set of homogeneous vs. heterogeneous GPU partition configurations we explore in Section VI.

| DNN Model | # of A100 | GPU(1) | GPU(2) | GPU(3) | GPU(7) |
|-----------|-----------|--------|--------|--------|--------|
| ShuffleNet| 4         | 24     | 12     | 8      | 4      |
| MobileNet | 4         | 18     | 18     | 18     | 18     |
| ResNet    | 4         | 24     | 24     | 24     | 24     |
| BERT      | 4         | 4      | 4      | 4      | 4      |

Fig. 11: 95-percentile tail latency (y-axis) and latency-bounded throughput (i.e., the number of queries processed per second that meets a target tail latency, x-axis) for (a) ShuffleNet, (b) MobileNet, (c) ResNet, (d) BERT, and (e) Conformer. For brevity, we only plot GPU(7) and GPU(max) as these two designs provide best average latency-bounded throughput among all baseline designs we study (detailed in Figure 12). (d) BERT does not show GPU(7)+FIFS because GPU(max) equals GPU(7).

where we employ 8 instances of GPU(7) (total 56 GPCs) vs. the total 48 GPCs used under GPU(1,2,3). Because all of our PARIS design points are given only 24/48/42 GPCs for MobileNet/ResNet/BERT as the pool of GPCs for partitioning (i.e., identical to the number of GPC given to GPU(1,2,3) and smaller than the total number of GPCs assigned to GPU(7)), our evaluation provides a conservative estimation of the benefits provided with PARIS and ELSA. While these caveats might give the impression that the usage of reconfigurable GPUs are limited, recall that A100 is the first GPU to employ reconfigurability, so we expect these issues to be resolved in future iterations of GPUs.

**SLA target.** As the precise SLA target numbers per each DNN model are vendor-specific, proprietary information not publicly disclosed, we take the following measure in setting our SLA target when measuring tail latency. For a given query size distribution, we first measure the DNN model’s inference latency with the distribution’s max batch size (32 under our default setting) over GPU(7). The SLA target for a given model is setup as \( N \) times (\( \approx 1.5 \times \) in our default setting) larger than this measured inference latency. This is because the SLA should at least be large enough for a given GPU partition handle. In Section VI-C, we evaluate the sensitivity of our proposal to different SLA targets, i.e., different \( N \) numbers.

VI. EVALUATION

We compare the following six design points in our analysis:

1) [GPU(N)+FIFS]: homogeneous partitioning with GPU(N), \( (N: \) number of GPCs per GPU partition), schedule FIFS

2) [GPU(max)+FIFS]: GPU(max) reports the best performing homogeneous partitioning among all possible GPU(N), schedule FIFS

3) [Random+FIFS]: randomly partitioning the GPU in a heterogeneous manner, schedule with FIFS

4) [Random+ELSA]: randomly partitioning the GPU in a heterogeneous manner, schedule with ELSA

5) [PARIS+FIFS]: heterogeneous partitioning using PARIS, schedule with FIFS

6) [PARIS+ELSA]: heterogeneous partitioning using PARIS, schedule with ELSA

Since there are many design points we explore in this section (e.g., GPU(N) alone contains four design points, \( N=1,2,3,7 \), Table I), some of the figures presented in this section do not show the results for all possible designs for both brevity and clarity of explanation. Specifically, we exclude showing the results exhibiting low performance and use GPU(max) as an optimistic homogeneous partitioning scheme (i.e., it performs as an upper bound design for homogeneous partitioning). Note that we included “Random” partitioning as means to demonstrate the importance of accommodating model properties and batch size distribution when heterogeneously partitioning the reconfigurable GPUs.

A. Tail Latency

In Figure 11, we show latency-bounded throughput as a function of a target tail latency. The vertical lines show the latency-bounded throughput when the target tail latency is setup identically to our SLA. Using this as the comparison point, the best performing homogeneous partition...
GPU(max)+FIFS suffers from 1.1×, 17.4×, 1.2×, 1.1×, and 1.2× worse tail latency than PARIS+ELSA for ShuffleNet, MobileNet, ResNet, BERT, and Conformer, respectively. Here, MobileNet performs best when configured with a GPU partition size of GPU(3) (i.e., GPU(max)=GPU(3)), eight instances of GPU(3), 24=(3×8) GPCs overall, see Table I). As discussed in Figure 4, however, MobileNet suffers from significant GPU underutilization with a medium sized GPU(3) leaving significant room for improvement. Our PARIS observes such opportunity and utilizes the 24 GPCs to construct a heterogeneous group of GPU partitions, specifically 6×GPU(1)+4×GPU(2)+2×GPU(3)+1×GPU(4), which allows PARIS+ELSA to drastically improve tail latency and overall throughput (discussed in the next subsection).

As for ResNet and BERT, these two models’ GPU(max) is determined as GPU(3) and GPU(7), respectively. Because the GPU underutilization under these GPU partition sizes are not as significant under MobileNet, the tail latency improvements with PARIS+ELSA is relatively modest compared to MobileNet. Nonetheless, recall that GPU(max) is an optimistic, upper bound design point of a homogeneously partitioned multi-GPU server. That is, determining the optimal GPU(max) design for homogeneous servers requires the system architect to painstakingly search through the wide design space in a manual, brute-force manner. As discussed in Section IV-B, PARIS is a fully automated algorithm that systematically finds out the optimal partitioning points to pursue without any additional effort from the end-user.

**B. Latency-bounded Throughput**

Figure 12 shows latency-bounded throughput, which is normalized to GPU(7)+FIFS as it provides the most robust performance among all studied homogeneous server configurations. Several key observations can be made from this experiment. First, no single homogeneously partitioned GPU(N) design is able to universally achieve high throughput. For instance, GPU(3)+FIFS provides competitive results vs. our proposal for MobileNet (70% of PARIS+ELSA) and ResNet (94% of PARIS+ELSA). Unfortunately, GPU(3) suffers from substantial throughput degradation for BERT because it cannot provide enough computation power to satisfactorily service this highly compute-intensive ML model. Consequently, GPU(3) suffers from significant SLA violations when BERT is executed with a large batch size, rendering GPU(7) the most robust design when considering all three models. PARIS, on the other hand, is able to identify the need for high computing power within the inference server for BERT, partitioning the 42 GPCs (Table I) into a heterogeneous group of 2×GPU(3)+2×GPU(4)+4×GPU(7). Such heterogeneity allows our proposed inference server to flexibly adapt to the unique DNN computation demands of BERT.

Another important point worth mentioning is the effectiveness of our ELSA algorithm, especially for MobileNet and ResNet. Take MobileNet as an example, which PARIS configures the 24 GPCs into 6×GPU(1)+4×GPU(2)+2×GPU(3)+1×GPU(4). Because the number of large GPUs PARIS has provisioned is relatively small, the scheduler should schedule large batch queries judiciously in order to minimize SLA violations. The heterogeneity-aware ELSA utilizes our SLA slack estimator to predict the likelihood of SLA violations and does a better job handling large batch queries than FIFS, providing high throughput improvements. BERT is the least sensitive to the addition of ELSA in PARIS, as PARIS+FIFS already provides superior performance, leaving little rooms of improvement.

It is interesting to note that a randomly partitioned heterogeneous server performs fairly competitively vs. homogeneous servers, provided it is coupled with our ELSA scheduler. These results highlight the merits of adding heterogeneous compute capabilities into ML inference servers.

Overall, our fully automated PARIS+ELSA demonstrates the importance of incorporating heterogeneity into reconfigurable multi-GPU servers tailored for ML inference.

**C. Sensitivity**

**Batch size distribution.** Figure 13(a) summarizes the sensitivity of our proposal to different log-normal distributions, i.e., when changing the distribution variance values from small to large. Under small variance distributions, the rooms
of improvement a heterogeneous multi-GPU server can fulfill are relatively smaller. This is because under small(er) variance log-normal distributions, the batch sizes tend to be centered around a specific value which gives more likelihood of a specific homogeneous partitioning point to more robustly handle inference queries. Consequently, the throughput improvements provided with PARIS+ELSA compared to the best performing GPU(max) become smaller (larger) with smaller (larger) variance distributions.

**Max batch size.** Figure 13(b) shows the throughput when the maximum batch size within our batch size distribution is changed. As depicted, the efficacy of PARIS+ELSA remains robust across wide ranging max batch sizes.

**Different SLA targets.** We also confirmed PARIS+ELSA’s robustness under different SLA targets. For instance, when the SLA target is setup as \(N = 2.0 \times \) times of the max batch size inference latency \((N = 1.5 \times \) being our default, Section V), PARIS+ELSA provides an average 1.19 \(\times\) reduction in tail latency which translates into an average 1.7 \(\times\) and 1.1 \(\times\) improvement in latency-bounded throughput vs. GPU(7) and GPU(max), respectively.

**VII. CONCLUSION**

We explore an emerging reconfigurable GPU architecture to construct a heterogeneous ML inference server. We first proposed PARIS, a partitioning algorithm for reconfigurable GPUs that systematically determines a heterogeneous set of multi-granular GPU partitions in a user-transparent manner. The heterogeneously partitioned multi-GPU server is orchestrated by ELSA, which is capable of exploiting the unique heterogeneous computing power of PARIS inference server for maximum efficiency. PARIS and ELSA require no additional effort from the end-user and provides high server utilization improvements while guaranteeing SLA.

**REFERENCES**

[1] Google, “Cloud TPU.” https://cloud.google.com/tpu, 2018.

[2] A. W. Services, “Amazon elastic inference.” https://aws.amazon.com/machine-learning/elastic-inference/, 2018.

[3] Habana, “Habana Gaudi and Goya: New Levels of AI Performance, Low Power and Cost Efficiency for Datacenter & Cloud.” https://habana.ai/.

[4] N. P. Jouppi, C. Young, N. Patil, D. Patterson, G. Agrawal, R. Bajwa, S. Bates, S. Bhatia, N. Boden, A. Borchers, R. Boyle, P. Cantin, C. Chao, C. Clark, J. Coriell, M. Daley, M. Dau, J. Dean, B. Gelb, T. V. Ghaemmaghami, R. Gottipati, W. Gulland, R. Hagmann, C. R. Ho, D. Hogberg, J. Hu, R. Hundt, D. Hurt, J. Ibarz, A. Jaffey, A. Jaworski, A. Kaplan, H. Khaitan, D. Killebrew, A. Koch, N. Kumar, S. Lacy, J. Laudon, J. Law, D. Le, C. Leary, Z. Liu, K. Lucke, A. Lundin, G. MacKean, A. Maggiore, M. Mahony, K. Miller, R. Nagarajan, R. Narayanaswami, R. Ni, K. Nix, T. Norrie, M. Osnertick, N. Penukonda, A. Phelps, J. Ross, M. Ross, A. Salek, E. Samadiani, C. Severn, G. Sizikov, M. Snelham, J. Souter, D. Steinberg, A. Swing, M. Tan, G. Thorson, B. Tian, H. Toma, E. Tuttle, V. Vasudevan, R. Walter, W. Wang, E. Wilcox, and D. H. Yoon, “In-datacenter Performance Analysis of A Tensor Processing Unit,” in Proceedings of the International Symposium on Computer Architecture (ISCA), 2017.

[5] Facebook, “Accelerating Facebook’s Infrastructure with Application-specific Hardware,” 2019.

[6] K. Hazelwood, S. Bird, D. Brooks, S. Chintala, U. Diril, D. Dzuhlakoglu, M. Fawzy, B. Jia, Y. Jia, A. Kalto, et al., “Applied Machine Learning at Facebook: A Datacenter Infrastructure Perspective,” in Proceedings of the International Symposium on High-Performance Computer Architecture (HPCA), 2018.

[7] U. Gupta, C.-J. Wu, X. Wang, M. Naumov, B. Reagen, D. Brooks, B. Cottel, K. Hazelwood, M. Hempstead, B. Jia, et al., “The Architectural Implications of Facebook’s DNN-based Personalized Recommendation,” in Proceedings of the International Symposium on High-Performance Computer Architecture (HPCA), 2020.

[8] J. Fowers, K. Otvcharov, M. Papmichael, T. Massengill, M. Liu, D. Lo, S. Alkalay, M. Haselman, L. Adams, M. Ghandi, S. Heil, P. Patel, A. Sapek, G. Weisz, L. Woods, S. Lanka, S. K. Reienhardt, A. M. Caulfield, E. S. Chung, and D. Burger, “A Configurable Cloud-Scale DNN Processor for Real-Time AI,” in Proceedings of the International Symposium on Computer Architecture (ISCA), 2018.

[9] D. J. Moss, S. Krishnan, E. Nurvitadhi, P. Ratuszniak, C. Johnson, J. Sim, A. Mishra, D. Marr, S. Subhaschandra, and P. H. Leong, “A Customizable Matrix Multiplication Framework for the Intel HARPv2 Xeon+FPGA Platform: A Deep Learning Case Study,” in Proceedings of the ACM International Symposium on Field-Programmable Gate Arrays (FPGA), 2018.

[10] E. Nurvitadhi, G. Venkatesh, J. Sim, D. Marr, R. Huang, J. Ong Gee Hock, Y. T. Liew, K. Srivatsan, D. Moss, S. Subhaschandra, et al., “Can FPGAs Beat GPUs in Accelerating Next-Generation Deep Neural Networks?,” in Proceedings of the ACM International Symposium on Field-Programmable Gate Arrays (FPGA), 2017.

[11] VMware, “Single Root I/O Virtualization (SR-IOV).” https://docs.vmware.com/en/VMware-vSphere/7.0/com.vmware.vsphere.networking.doc/GUID-CC21803-30EA-444D-BCBE-618ED8386B9F.html, 2019.

[12] M. Tulloch and W. S. Team, Optimizing and Troubleshooting Hyper-V Networking. Pearson Education, 2013.

[13] M. Shoeybi, M. Patwary, R. Puri, P. LeGresley, J. Casper, and B. Catanzaro, “Megatron-LM: Training Multi-Billion Parameter Language Models Using Model Parallelism,” arXiv preprint arXiv:1909.00853, 2019.

[14] D. Nudigere, Y. Hao, J. Huang, A. Tulloch, S. Srivaharan, X. Liu, M. Ozdal, J. Nie, J. Park, L. Luo, et al., “High-Performance, Distributed Training of Large-Scale Deep Learning Recommendation Models,” arXiv preprint arXiv:2104.05158, 2021.

[15] D. Lepikhin, H. Lee, Y. Xu, D. Chen, O. Firan, Y. Huang, M. Krikun, N. Shazeer, and Z. Chen, “GShard: Scaling Giant Models with Conditional Computation and Automatic Sharding,” 2021.

[16] P. Mattson, V. J. Reddi, C. Cheng, C. Coleman, G. Diamos, D. Kanter, P. Micikevicius, D. Patterson, G. Schmueling, H. Tang, et al., “MLPerf: An Industry Standard Benchmark Suite for Machine Learning Performance,” IEEE Micro, vol. 40, no. 2, pp. 8–16, 2020.

[17] U. Gupta, S. Hisa, V. Saraph, X. Wang, B. Reagen, G.-Y. Wei, H.-H. S. Lee, D. Brooks, and C.-J. Wu, “DeepRecSys: A System for Optimizing End-to-end At-scale Neural Recommendation Inference,” in Proceedings of the International Symposium on Computer Architecture (ISCA), 2020.

[18] J. Li, K. Agrawal, S. Elnikety, Y. He, I.-T. A. Lee, C. Lu, and K. S. McKinley, “Work Stealing for Interactive Services to Meet Target Latency,” in Proceedings of the ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming, 2016.

[19] P. Barford and M. Crowella, “Generating Representative Web Workloads for Network and Server Performance Evaluation,” in Proceedings of the ACM SIGMETRICS joint international conference on Measurement and modeling of computer systems, 1998.

[20] Samsung, “GDDR6 DRAM,” 2021.

[21] JEDEC, “High Bandwidth Memory (HBM2) DRAM,” 2018.

[22] NVIDIA, “NVIDIA Tesla M4.” https://images.nvidia.com/content/tesla/pdf/NVIDIA Tesla-Print-M4-Datasheet_LR.PDF, 2016.

[23] NVIDIA, “NVIDIA T4.” https://www.nvidia.com/content/dam/en-\(\frac{\text{zz}}{}\)/Solutions/Data-Center/tesla-t4-t4/tensor-core-datasheet-951643.pdf, 2019.

[24] NVIDIA, “NVIDIA A100.” https://www.nvidia.com/content/dam/en-\(\frac{\text{zz}}{}\)/Solutions/Data-Center/tesla-t4/t4/tensor-core-datasheet-951643.pdf, 2020.

[25] NVIDIA, “NVIDIA CUDA Programming Guide,” 2021.

[26] J. Hauswald, Y. Kang, M. A. Laurenzana, Q. Chen, C. Li, T. Mudge, R. Godfrey, and J. Tang, “Djinn and Tonic: DNN as a Service and Its Implications for Future Warehouse Scale Computers,” in
[27] C. Olston, N. Fiedel, K. Gorovoy, J. Harmsen, L. Lao, F. Li, V. Rjashekhar, S. Ramesh, and J. Soyske, “TensorFlow-Serving: Flexible, High-Performance ML Serving,” arXiv preprint arXiv:1712.06139, 2017.

[28] Amazon, “Amazon SageMaker.” https://aws.amazon.com/sagemaker/.

[29] NVIDIA, “NVIDIA Triton Inference Server.” https://developer.nvidia.com/nvidia-triton-inference-server.

[30] D. Narayanan, A. Harlap, A. Phanishayee, V. Seshadri, N. R. Devanur, G. R. Ganger, P. B. Gibbons, and M. Zaharia, “PipeDream: Generalized Pipeline Parallelism for DNN Training,” in Proceedings of the ACM Symposium on Operating Systems Principles, 2019.

[31] Y. Huang, Y. Cheng, A. Bapna, O. Firat, D. Chen, M. Chen, H. Lee, J. Ngiam, Q. V. Le, Y. Wu, et al., “Gpipe: Efficient Training of Giant Neural Networks Using Pipeline Parallelism,” Proceedings of the International Conference on Neural Information Processing Systems (NIPS), 2019.

[32] M. Han, J. Hyun, S. Park, J. Park, and W. Baek, “MOSAIC: Heterogeneity-, Communication-, and Constraint-Aware Model Slicing and Execution for Accurate and Efficient Inference,” in Proceedings of the International Conference on Parallel Architectures and Compilation Techniques (PACT), 2019.

[33] Y. Kim, J. Kim, D. Chae, D. Kim, and J. Kim, “μlayer: Low Latency On-Device Inference Using Cooperative Single-Layer Acceleration and Processor-Friendly Quantization,” in Proceedings of the EuroSys Conference (EuroSys), 2019.

[34] A. E. Eshratifar, M. S. Abrishami, and M. Pedram, “JointDNN: An Efficient Training and Inference Engine for Intelligent Mobile Cloud Computing Services,” IEEE Transactions on Mobile Computing, 2019.

[35] M. Gao, J. Pu, X. Yang, M. Horowitz, and C. Kozyrakis, “TETRIS: Scalable and Efficient Neural Network Acceleration with 3D Memory,” in Proceedings of the International Conference on Architectural Support for Programming Languages and Operation Systems (ASPLOS), 2017.

[36] H. Shen, L. Chen, Y. Jin, L. Zhao, B. Kong, M. Philipose, A. Krishnamurthy, and R. Sundaram, “Nexus: A GPU Cluster Engine for Accelerating DNN-based Video Analysis,” in Proceedings of the 27th ACM Symposium on Operating Systems Principles, pp. 322–337, ACM, 2019.

[37] R. S. Kannan, L. Subramanian, A. Raju, J. Ahn, J. Mars, and L. Tang, “GrandSLAm: Guaranteeing SLAs for Jobs in Microservices Execution Frameworks,” in Proceedings of the EuroSys Conference (EuroSys), 2019.

[38] Y. Choi and M. Rhu, “PREMA: A Predictive Multi-task Scheduling Algorithm For Preemptible Neural Processing Units,” in Proceedings of the International Symposium on High-Performance Computer Architecture (HPCA), 2020.

[39] Y. Choi, Y. Kim, and M. Rhu, “Lazy Batching: An SLA-aware Batching System for Cloud Machine Learning Inference,” in Proceedings of the International Symposium on High-Performance Computer Architecture (HPCA), 2021.

[40] N. Ma, X. Zhang, H.-T. Zheng, and J. Sun, “ShuffleNet v2: Practical Guidelines for Efficient CNN Architecture Design,” 2018.

[41] A. G. Howard, M. Zhu, B. Chen, D. Kalenichenko, W. Wang, T. Weyand, M. Andreetto, and H. Adam, “Mobilenets: Efficient Convolutional Neural Networks for Mobile Vision Applications,” arXiv preprint arXiv:1704.04861, 2017.

[42] S. Gross and M. Wilber, “Training and Investigating Residual Nets,” 2016.

[43] J. Devlin, M.-W. Chang, K. Lee, and K. Toutanova, “BERT: Pre-training of Deep Bidirectional Transformers for Language Understanding,” arXiv preprint arXiv:1810.04805, 2018.

[44] A. Gulati, J. Qin, C.-C. Chiu, N. Parmar, Y. Zhang, J. Yu, W. Han, S. Wang, Z. Zhang, and Y. Wu, “Conformer: Convolution-augmented Transformer for Speech Recognition,” 2020.

[45] U. Gupta, S. Hsia, V. Saraph, X. Wang, B. Reagen, G.-Y. Wei, H.-H. S. Lee, D. Brooks, and C.-J. Wu, “Deeprecsys: A system for optimizing end-to-end at-scale neural recommendation inference.” https://github.com/harvard-acc/DeepRecSys, 2020.