Optimal configuration for cascaded voltage source multilevel inverter based on series connection sub-multilevel inverter

Kishor Thakre1*, Kanungo Barada Mohanty1, Vinaya Sagar Kommukuri1 and Aditi Chatterjee1

Abstract: In this study, a new configuration for cascaded voltage source multilevel inverter based on series connection of improved sub multilevel inverter module is presented. An algorithm is proposed to determine the magnitude of dc voltage source to generate a large number of output voltage levels with reduced device count. It is especially suitable for of renewable energy applications. To demonstrate the advantages of proposed configuration, the comparative analysis provided with other multilevel configurations in term of a number of switches, gate driver circuits and blocking voltage on switches. The comparison results confirm that the proposed configuration offers less number of components. Moreover, the magnitude of blocking voltage on switches and losses are lower in the proposed configuration. Multicarrier based sinusoidal pulse width modulation scheme is adopted for generating switching signals using dSPACE real-time controller. To validate the performance of proposed topology under steady state and dynamic condition are carried out using simulation on MATLAB/Simulink and experimental implementation.

ABOUT THE AUTHORS
Kishor Thakre received his BE degree in Electrical & Electronics Engineering from RGPV Bhopal in 2007. In 2009, he received his MTech in Electrical Engineering from NIT Rourkela. He was with UIT-RGPV, Bhopal as a faculty from 2009 to 2013. Currently he is working towards PhD in Electrical Engineering at NIT Rourkela, India.

Kanungo Barada Mohanty received his BE from Sambalpur University, MTech and PhD degrees from IIT, Kharagpur in the years 1989, 1991 and 2002 respectively, in Electrical Engineering. Currently serving as Associate Professor in NIT, Rourkela. Dr Mohanty is a senior member of the IEEE, fellow of the IE (India), Fellow of IETE, and Life Member of Solar Energy Society of India, and System Society of India.

Vinaya Sagar Kommukuri received his BTech in Electrical & Electronics Engineering from KL University in 2007. In 2010, he received his MTech in Power Control & Drives from NIT Rourkela. He is currently pursuing Doctorate degree in Electrical Engineering at NIT Rourkela.

Aditi Chatterjee received her BTech in Electrical Engineering from IGIT Sarang in 2009. In 2013, she received her MTech in Power systems from UCE Burla. She is currently pursuing Doctorate degree in Electrical Engineering at NIT Rourkela.

PUBLIC INTEREST STATEMENT
Multilevel converters have created a new height of interest in the industrial application and research. While the conventional topologies have proved to be an applicable alternative in a wide range of high power medium-high voltage applications, there has been an effective interest in the optimal progression multilevel inverters. Reduction in a number of devices as compared to the conventional multilevel inverters (MLI) has been an important objective in the recently introduced MLI topologies. In this paper, a new configuration for cascaded voltage source multilevel inverter based on the series connection of improved sub multilevel inverter module is presented. An algorithm is proposed to determine the magnitude of dc voltage source to generate a large number of output voltage levels with reduced device count. The comparison results confirm that the proposed configuration offers less number of devices. It is especially suitable for of renewable energy applications.
1. Introduction

Voltage source multilevel inverters (VS-MLI) play an important role for medium and high voltage applications such as AC drives, FACTS, static VAR compensators, hybrid electric vehicles and renewable energy sources. Because of its advantages such as low total harmonic distortion (THD), less voltage stress, better electromagnetic interference and high-quality output voltage waveform (Azeez, Dey, Mathew, & Mathew, 2014; Buticchi et al., 2014; Rodriguez, Bernet, Wu, Pontt, & Kouro, 2007; Rodriguez, Lai, & Peng, 2002; Song & Huang, 2010). However, VS-MLI suffers from several drawbacks such as the number of power switches with related gate driver circuits and protection circuit increases with increase in the number of voltage levels. This increase system complexity, inverter cost, reduces the reliability and efficiency of the inverter. In general, there are three types of topologies for MLI; Neutral point clamped (NPC), or diode clamped, flying capacitor (FC) and cascaded H-bridge multilevel inverters (CHB-MLI) are discussed in Chavarria, Biel, and Guinjoan (2013), Khajehoddin, Bakhshai, and Jain (2008), McGrath and Holmes (2008). The CHB-MLI is most popular topology among three conventional topologies based on its modular structure and less number of component. A CHB-MLI is series connection of H-bridges with isolated DC sources. The magnitude of dc source categorised in to two configurations, symmetric and asymmetric MLI. In symmetric MLI the magnitude of dc sources are equal, on the other hand the magnitude of dc sources are unequal in the asymmetric MLIs (Lu, Marieethoz, & Corzine, 2010; Veenstra & Rufer, 2005). An asymmetric inverter increases the number of output voltage levels for same number of switches. There are two configurations for calculating the magnitude of dc voltage source, i.e. trinary and binary configurations. The trinary configuration generates high number of voltage level as compared to binary configuration (Gupta & Jain, 2012). Another hybrid MLI, have presented in Babaei and Gowgani (2014), Rech and Pinheiro (2007). consist of different MLI topologies with unequal dc volatge source and different switching schemes.

Consequently, in last few years many topologies for symmetrical, asymmetrical structures with reduced switch count and switching schemes have been proposed in Babaei (2008), Babaei and Hosseini (2009), Babaei, Hosseini, Gharehpetian, Haque, and Sabahi (2007), Banaei and Salary (2011), Ceglia et al. (2006), Ebrahimi, Babaei, and Gharehpetian (2012), Gupta and Jain (2014a, 2014b), Haque (2004), Hinago and Koizumi (2010), Jannati Oskuee, Banaei, and Khounjahan (2014), Mokhberdoran, Jannati Oskuee, Toopchi Khosroshahi, et al. (2014), Najafi and Yatim (2012), Ounejjar, Al-Haddad, and Grégoire (2011), Sabahi, Babaei, and Farhadi Kangarlu (2013), Salary, Jannati Oskuee, and Nojafi-Ravadanegh (2015), Shalchi Alishah, Nazarpour, Hosseini, and Sabahi (2015). Some of them are discussed briefly in Babaeei (2008), Babaeei and Hosseini (2009), Babaeei et al. (2007), Banaei and Salary (2011), Ebrahimi et al. (2012), Gupta and Jain (2014a), Haque (2004), Jannati Oskuee et al. (2014), Mokhberdoran et al. (2014), Sabahi et al. (2013), Shalchi Alishah et al. (2015). The topology presented in Babaeei and Hosseini (2009) known as semi-cascaded MLI has an advantage of a lower number of components over conventional CHB-MLI. But, it suffers from maximum blocking voltage (MBV) on switches compared with CHB-MLI. A reconfiguration of semi cascaded MLI introduced in Banaei and Salary (2011), Gupta and Jain (2014a), Jannati Oskuee et al. (2014) which needs less number of components and MBV compared and to Babaeei and Hosseini (2009). Recently, a new topology has been proposed in Mokhberdoran et al. (2014). This topology requires fewer numbers of switches and total power loss are reduced as compared to CHB inverter and its MBV is same as CHB inverter. Another cross connected switch MLI has been proposed in Sabahi et al. (2013), it offers lower number of switches as compared to that given in Mokhberdoran et al. (2014), same MBV as in Gupta and Jain (2014a) and CHB-MLI.
There are some interesting topologies in literature (Babaei, 2008; Babaei et al., 2007; Ebrahimi et al., 2012; Haque, 2004; Shalchi Alishah et al., 2015) based on bidirectional switches, which reduced the large number of components for higher voltage levels as compare to Babaei and Hosseini (2009), Banaei and Salary (2011), Gupta and Jain (2014a), Jannati Oskuee et al. (2014), Mokhberdoran et al. (2014), Sabahi et al. (2013). An effort has been in Haque (2004)) and its expansion in Babaei et al. (2007) to present a new topology with less number of components compared to conventional and topologies presented in Babaei and Hosseini (2009), Banaei and Salary (2011), Gupta and Jain (2014a), Jannati Oskuee et al. (2014), Mokhberdoran et al. (2014), Sabahi et al. (2013). But the proposed topologies (Babaei et al., 2007; Haque, 2004) not able to generates all voltage levels including odd and even.

A topology introduced in Babaei (2008) to overcome the mentioned issue (Babaei et al., 2007; Haque, 2004), but topology uses only single H-bridge which is bound for high voltage applications. Moreover, this configuration needs a large number of bidirectional switches and MBV is high. Another configuration presented in Ebrahimi et al. (2012), which composed of series connection of sub-module with H-bridge for generating the great number of voltage levels. It needs lower number of switches as compare to Babaei (2008) and same MBV. In Shalchi Alishah et al. (2015), a new cascaded MLI has been presented with fewer numbers of switches as compared to Babaei (2008), Ebrahimi et al. (2012). The main drawback of MLIs are requires a high number of switches, gate drivers and MBV across the switches.

Several switching schemes have been presented for multilevel inverters (Farokhnia, Fathi, Salehi, Gharehpetian, & Ehsani, 2012; Gupta, Ghosh, & Joshi, 2008; McGrath & Holmes, 2002; Thakre and Mohanty, 2015; Rathore, Holtz, & Boller, 2013; Sozer, Hawes, Saha, Nguyen, & Torrey, 2014; Meshram & Borghate, 2014) such as carrier based sinusoidal pulse width modulation (SPWM), space vector pulse width modulation (SVPWM), nearest level control and selective harmonic elimination scheme to improve THD and quality voltage waveform. In this paper, an advanced configuration for VS-MLI has been proposed using multicaarrier based on SPWM (McGrath & Holmes, 2002) is used.

This study presents a new configuration for VS-MLI, which can be a solution of all above discussed issues.

2. Proposed configuration
The proposed configuration for a voltage source multilevel inverter is shown in Figure 1. This configuration consists of one H-bridge and a basic unit cell. The basic unit contains \( p \) bidirectional auxiliary switches, which have been presented in Gautam, Gupta, and Kumar (2015), Gautam, Gupta, and Sahu (2016), Odeh and Agu (2016), Raushan, Mahato, and Jana (2016) and \( (p + 1) \) dc sources.

Table 1 shows the look-up table for switching states for different output voltage in proposed sub-MLI; its magnitude of isolated dc source is uniform. Therefore, this MLI is called symmetric VS-MLI. In the proposed configuration the number of output voltage levels, number of switches and gate drivers can be calculated as follows.

\[
N_{\text{LEVEL}} = 2p + 3
\]  

\[
N_{\text{SWITCH}} = N_{\text{MOSFET}} = N_{\text{DRIVER}} = p + 4
\]  

where \( p \) is the number of auxiliary switches in the basic unit. In the proposed VS-MLI the maximum output voltage \( V_{o,\text{max}} \) is

\[
V_{o,\text{max}} = (p + 1)V_{dc}
\]
Figure 2 shows the generalised configuration of proposed cascaded VS-MLI for generating higher voltage level with reduced switch count. The output voltage of cascaded VS-MLI is summation of each sub-MLI voltages, which can be calculated using

\[ V_0 = V_{01} + V_{02} + V_{03} + \cdots + V_{0n} \]  

(4)

The proposed cascaded VS-MLI consists of \( n \) number of sub-MLI with unequal magnitude of dc voltage source. However, in each sub MLI having same magnitude of dc voltage source. The magnitude of the dc source for each sub MLI must be chosen from the following algorithm;

**Sub MLI-1:**

\[ V_{dc,1} = V_{dc} \]  

(5)

In this sub MLI-1, the peak amplitude of output voltage \( (V_{01,\text{max}}) \) is obtained as follows

![Figure 1. Proposed configuration for sub-MLI.](image-url)

### Table 1. Switching states for different output voltage

| States | Switching states | Output voltage \( V_o \) |
|--------|------------------|--------------------------|
| 1      | 0 0 0 ... 0 0 0 1 1 0 0 0 | 0 |
| 2      | 0 0 0 ... 0 1 0 0 0 1 | \( V_{dc} \) |
| 3      | 1 0 0 ... 0 0 0 1 0 0 0 | \( -V_{dc} \) |
| 4      | 0 0 0 ... 1 0 0 0 0 1 | \( 2V_{dc} \) |
| 5      | 0 1 0 ... 0 0 0 1 0 0 | \( -2V_{dc} \) |
| ...    | ...              | ...                      |
| 1 \( p \) | 0 0 0 ... 0 0 0 0 1 | \( (p+1) V_{dc} \) |
| 2 \( p + 1 \) | 0 0 0 ... 0 0 1 1 0 | \( -(p+1) V_{dc} \) |

In this sub MLI-1, the peak amplitude of output voltage \( (V_{01,\text{max}}) \) is obtained as follows
Sub MLI-2:

Therefore, the peak amplitude of output voltage ($V_{02,max}$) is given by

$$V_{02,max} = (p_2 + 1)V_{dc}$$  \hspace{1cm} (6)

Sub MLI-3:

$$V_{dc,2} = V_{dc} + (2V_{01,max}) = V_{dc}(2p_1 + 3)$$  \hspace{1cm} (7)

Therefore, the peak amplitude of output voltage ($V_{02,max}$) is given by

$$(V_{02,max}) = (p_2 + 1)V_{dc,2}$$  \hspace{1cm} (8)

Sub MLI-n:

$$V_{dc,n} = [\{(2p_1 + 3)(2p_2 + 3)\cdots(2p_n + 3)\}]V_{dc}$$  \hspace{1cm} (11)

The number of output voltage levels can be calculated by the following equation:

$$N_{level} = \prod_{j=1}^{p-1} (2p_j + 3)$$  \hspace{1cm} (12)
In the proposed configuration, the number of power switches including auxiliary switches and unidirectional switches is given by

\[ N_{\text{switches}} = (p_1 + p_2 + p_3 + \cdots + p_n) + 4n \]  \hspace{1cm} (13)

By using the proposed algorithm, the maximum amplitude of the output voltage \( (V_{0,\text{max}}) \) is expressed, as follows:

\[ V_{0,\text{max}} = \sum_{j=1}^{n} (p_j + 1) + V_j \]  \hspace{1cm} (14)

3. Optimal configuration

3.1. Maximum number of voltage levels with constant number of switches

The main objective of a multilevel inverter is to generate higher voltage levels with minimum number of switches. The product of number of voltage levels, whose sum is constant, when the numbers of auxiliary switches are same in each basic unit.

\[ p_1 = p_2 = \cdots = p_n = p \]  \hspace{1cm} (15)

Using (13) and (15) can write

\[ \frac{N_{\text{switch}}}{(p + 4)} = n \]  \hspace{1cm} (16)

The value of \( p \) must be determined. Using (12) and (15), the maximum number of output voltage level will be determined as follows:

\[ N_{\text{level}} = (2p + 3)^n \]  \hspace{1cm} (17)

Considering (16) and (17), can express

\[ N_{\text{level}} = \left[ (2p + 3)^{\frac{1}{p+4}} \right]^{N_{\text{switch}}} \]  \hspace{1cm} (18)

Figure 3(a) shows the variation of \((2p + 3)^{\frac{1}{p+4}}\) vs. \( p \). It clear that maximum number of output voltage levels is obtained for \( p = 2 \). Thus, cascaded VS-MLI consisting of two auxiliary switches can produce the maximum output voltage levels.

3.2. Maximum number of voltage levels with constant number of isolated dc sources

As seen from Figure 2, the proposed configuration consist of \( n \) sub MLIs and each of them consist of \((p_j + 1)\) isolated dc sources \((j = 1, 2, \ldots, n)\). Thus, the number of dc sources can be obtained by:

\[ N_{\text{source}} = (p_1 + 1) + (p_2 + 1) + \cdots + (p_n + 1) = \sum_{j=1}^{n} (p_j + 1) \]  \hspace{1cm} (19)

\[ N_{\text{source}} = (p + 1)n \]  \hspace{1cm} (20)

Using (17) and (20), the maximum number of output voltage levels can be written as:

\[ N_{\text{level}} = \left[ (2p + 3)^{\frac{1}{p+1}} \right]^{N_{\text{source}}} \]  \hspace{1cm} (21)

Figure 3(b) shows the variation of \((2p + 3)^{\frac{1}{p+1}}\) vs. \( p \). Thus, the configuration consisting of sub MLIs with one dc source can generate maximum output voltage levels.
3.3. Minimum number of switches with constant number of voltage levels

In this part, the question is which configuration can generate $N_{\text{level}}$ with minimum number switches? Using Equation (18), the total number of switches can be obtained as follows:

$$N_{\text{switch}} = \ln(N_{\text{level}}) \times \frac{(p + 4)}{\ln(2p + 3)}$$  \hspace{1cm} (22)

Since $N_{\text{level}}$ is constant, $N_{\text{switch}}$ will be minimised. Figure 3(c) shows that the minimum number of switches is provided for $p = 2$.

3.4. Minimum number of gate drivers with constant number of voltage levels

In the suggested configuration for cascaded VS-MLI the total number of switches and gate driver circuit are equal. Hence, the minimum number of gate drivers using Equation (22) can be written as follows:

$$N_{\text{drivers}} = N_{\text{switch}} = \ln(N_{\text{level}}) \times \frac{(p + 4)}{\ln(2p + 3)}$$  \hspace{1cm} (23)
3.5. Minimum blocking voltage across the switches with constant number of voltage levels

An essential problem in multilevel inverters is the rating of circuit switches. In all MLIs, current through all switches are same as rated load current. But, this is not for the voltage across the switches. The aim is to find the configuration for cascaded VS-MLI with minimum blocking voltage which can generate constant number of output voltage levels. The maximum magnitude of blocking voltage ($V_{\text{switch}}$) is expressed as follows:

$$V_{\text{switch}} = V_{\text{switch},A} + V_{\text{switch},B}$$  \hspace{1cm} (24)$$

$$V_{\text{switch}} = \sum_{i=1}^{n} V_{\text{switch},A,i} + \sum_{i=1}^{n} V_{\text{switch},B,j}$$  \hspace{1cm} (25)$$

where $V_{\text{switch},A}$ and $V_{\text{switch},B}$ are the maximum magnitude of blocking voltage across the auxiliary and unidirectional switches, respectively. Also $V_{\text{switch},A,i}$ and $V_{\text{switch},B,j}$ shows the maximum value of blocking voltage across auxiliary switches in $j$th sub MLI and unidirectional switches in the $j$th H-bridge, respectively. Hence, Equation (25) can be considered as a criterion to compare different MLIs from the view point of the peak value across the switches (Babaei, 2008; Ebrahimi et al., 2012; Shalchi Alishah et al., 2015). The lower value of the criterion indicates that a minimum voltage across the switches.

As conclude from Figure 2, peak value of blocking voltage across the auxiliary switches in $j$th sub MLI can be expressed, as follows:

$$V_{\text{switch},A,j} = S \times V_j, \quad j = 1, 2, \ldots, n$$  \hspace{1cm} (26)$$

Therefore, the peak value of the blocking voltage across the auxiliary switches can be calculated, as follows:

$$V_{\text{switch},A} = S \times (V_{\text{dc},1} + V_{\text{dc},2} + \cdots + V_{\text{dc,n}})$$  \hspace{1cm} (27)$$

In the Equations (26) and (27), $S$ is determined by the following expression:

$$S = 2 \left[ p + (p - 1) + (p - 2) + \cdots + \left\{ p - \frac{(p - 3)}{2} \right\} \right]$$

$$+ \frac{p + 1}{2} = \frac{3p^2 + 2p - 1}{4} \quad \text{(if $p$ is an odd number)}$$  \hspace{1cm} (28)$$

$$S = 2 \left[ p + (p - 1) + (p - 2) + \cdots + \left\{ p - \frac{(p - 2)}{2} \right\} \right] = \frac{3p^2 + 2p}{4}$$  \hspace{1cm} (29)$$

$$\text{(if $p$ is an even number)}$$

From (5)–(12), (15), (27) and (28), the maximum voltage across auxiliary switches in basic units can be written as follows:

$$V_{\text{switch},A} = S \left[ 1 + (2p + 3) + \cdots + (2p + 3)^{n-1} \right] \times V_{\text{dc}}$$  \hspace{1cm} (30)$$

$$V_{\text{switch},A} = S \left( \frac{N_{\text{level}} - 1}{2p + 2} \right) \times V_{\text{dc}}$$  \hspace{1cm} (31)$$

The maximum value of the blocking voltage across the unidirectional switches in the $j$th H-bridges can be given as follows:

$$V_{\text{switch},B,j} = 2 \sum_{i=1}^{n} V_j = 2 \times (p + 1) \times (2p + 2)^{j-1} \times V_{\text{dc}}$$  \hspace{1cm} (32)$$
The maximum value of blocking voltage across the H-bridge switches can be expressed as follows:

\[ V_{\text{switch,ij}} = \sum_{i=1}^{n} V_{\text{switch,ij}} = V_{\text{dc}}[(2p + 3)^k - 1] = V_{\text{dc}} \times [N_{\text{level}} - 1] \]  

(33)

Hence, the MBV across all the switches of proposed configuration using (24) can be expressed, as follows:

\[ V_{\text{switch}} = V_{\text{dc}} \times \left(\frac{S}{2p + 2}(N_{\text{level}} - 1) + (N_{\text{level}} - 1)\right) \]

\[ V_{\text{switch}} = V_{\text{dc}} \times (N_{\text{level}} - 1) \times \left(\frac{S}{2p + 2} + 1\right) \]  

(34)

The curve is drawn between \((S/(2p + 2)) + 1\) and \(p\) is shown in Figure 3(d). As seen this curve, \(V_{\text{switch}}\) is minimum at \((p = 1)\) for proposed cascaded MLI.

### 3.6. Minimum number of ON-state switches with constant number of voltage levels

In the proposed configuration, the number of ON-state switches \((N_{\text{ON-SS}})\) can be calculated by:

\[ N_{\text{ON-SS}} = (p_1 + p_2 + \cdots + p_n) + p_n \]  

(35)

Using (15)–(17) and (35), the number of ON-state switches is given as follows:

\[ N_{\text{ON-SS}} = (p + 2)n = \ln(N_{\text{level}}) \times \frac{p + \frac{2}{\ln(2p + 3)}}{1} \]  

(36)

As shown in Figure 3(e), the minimum number of ON-state switches to generate maximum number of output voltage levels is obtained for \(p = 1\).

### 4. Switching scheme

The multicarrier based modified pulse width scheme have been used for the proposed topology, the associated signals are shown in Figure 4. A modulating signal, \(F_m(t)\) is a sinusoidal waveform of magnitude \(A_m\) with frequency \(f_m = 50\) Hz and fourteen \((N - 1)\) triangular signal used as carrier \(F_{cr}(t)\) with frequency \(f_{cr} = 2\) KHz for SPWM. Here amplitude of carrier \(A_{cr}\) and carrier above the zero reference are denoted as \(F_{cr+j}(t)\) and those below the zero reference are denoted as \(F_{cr-j}(t), (j = 1 \rightarrow m)\). Carrier signals are arranged such that the band occupy contiguous, in phase opposition disposition level-shift multicarrier SPWM. The amplitude modulation index \((M_a)\) and frequency modulation index \((M_f)\) are defined as

\[ M_a = \frac{A_m}{A_{cr}(N_t - 1)} \]  

(37)

\[ M_f = \frac{f_m}{f_{cr}} \]  

(38)

Each carrier is compared with a modulating wave, the carrier signals above the zero reference, each comparison gives “ON” if the reference signal is greater than the carrier signal and “OFF” otherwise. For all carrier signals below the zero reference, each comparison gives “OFF” if the reference signals greater than the carrier and “ON” otherwise.

\[ g^+(t) = 1, \quad \text{for} \quad f_{m}(t) \geq F_{cr+j}(t) \]

\[ = 0, \quad \text{otherwise} \]  

(39)

\[ g^-(t) = 0, \quad \text{for} \quad f_{m}(t) \geq F_{cr-j}(t) \]

\[ = 1, \quad \text{otherwise} \]  

(40)

The generated signals from comparator are added so as obtained as “combined signal” denotes as

\[ g_{\text{comb}}(t) = \sum_{j=1}^{N} (g^+(t) + g^-(t)) \]  

(41)
The combination signal "g_comb(t)" that acquires the same wave shape as that of the staircase output voltage waveform is shown in Figure 4, the actual switching signals are obtained from combined signal by comparing the desired level signals and generated look-up table.

5. Calculation of losses
The reduction in the number of switches has a significant effect on the inverter losses as the conduction loss depends on ON-state voltage drop of power switches and equivalent resistance and the switching losses depend on the non-ideal operation of power switches. The power losses are calculated as follows.

5.1. Conduction loss
The conduction loss occurs during the ON-state switch. Therefore the conduction loss is determined by product of ON-state voltage drop and current through the device (Raushan et al., 2016). The knee voltage of the auxiliary switch as shown in Figure 1 is the sum of knee voltage of two diodes and a MOSFET. Therefore, ON-state voltage drop across the auxiliary switch can be calculated as follows:

\[ V_{on,A} = V_{on,T} + 2V_{on,D} \]
\[ V_{on,A} = [(V_T + I^\beta \cdot R_T) + 2(V_D + R_D I)] \]  \hspace{1cm} (43)

where \(V_T\) and \(R_T\) are ON-state voltage and the equivalent resistance of MOSFET, respectively. \(\beta\) is a constant dependent on MOSFET parameters. \(V_D\) and \(R_D\) represents ON-state voltage and resistance of the diode, respectively. If the MLI operating at large number of voltage level, the load current can be assumed is almost as a sinusoidal. The instantaneous conduction loss \(P_{cn,n}(t)\) can be given as:

\[ P_{cn,n}(t) = \left[ (V_T + 2V_D)I_o \sin(\omega t) + 2R_D I_o^2 \cdot \sin(\omega t) + R_T \cdot I_o^{\beta+1} \sin^{\beta+1}(\omega t) \right] \]  \hspace{1cm} (44)

In the proposed VS-MLI, \(p\) numbers of auxiliary switches are present accompanied by H-bridge unidirectional switches i.e. MOSFET with body diode. Hence, the instantaneous conduction loss of the unidirectional switches \(P_{c,u}(t)\) can be calculated as:

\[ P_{c,u}(t) = \left[ (N_c(t) + N_o(t)I_o)I_o \cdot \sin(\omega t) + N_o(t)R_o I_o^2 \sin^2(\omega t) + R_T I_o^{\beta+1} \sin^{\beta+1}(\omega t) \right] \]  \hspace{1cm} (45)

To calculate the total conduction loss, it is required to define the switches count, \(N_c(t)\) and diodes, \(N_o(t)\) at any instant in H-bridge. It is noticeable that, output voltage level and operating conditions (in the current direction) affect the quantity of ON-state switches that is time-variant. Considering \(P_{c,u}(t)\) as instantaneous conduction loss of \(n\)th auxiliary switch, The average conduction losses are written as follows:

\[ P_{c,Avg} = \frac{1}{\pi} \sum_{n=1}^{P} \int_0^\pi [P_{cn,n}(t)] d\omega t + \frac{1}{\pi} \int_0^\pi [P_{c,u}(t)] d\omega t \]  \hspace{1cm} (46)

5.2. Switching losses

To calculate the total switching loss of the proposed inverter, the energy loss during ON and OFF-state of a typical power switch with the body diode is considered first and then that amount is applied to the proposed inverter. Suppose that the voltage and current varies linearly during ON and OFF time a switch can be expressed as follows.

\[ E_{on} = \int_0^{t_{on}} v(t) \cdot i(t) dt \]

\[ = \int_0^{t_{on}} \left( \frac{V_{sw}}{t_{on}} \right) \left( - \frac{I}{t_{on}} (t - t_{on}) \right) dt = \frac{1}{6} V_{sw} I_{on} \]  \hspace{1cm} (47)

\[ E_{off} = \int_0^{t_{off}} v(t) \cdot i(t) dt \]

\[ = \int_0^{t_{off}} \left( \frac{V_{sw}}{t_{off}} \right) \left( - \frac{I}{t_{off}} (t - t_{off}) \right) dt = \frac{1}{6} V_{sw} I_{off} \]  \hspace{1cm} (48)

where \(E_{on}\) and \(E_{off}\) are ON-state and OFF-state loss energy and \(t_{on}\) and \(t_{off}\) are the ON and OFF-state period of the switch respectively. \(I\) is the current through the switch and \(V_{sw}\) is voltage across the switch before turned-OFF or turned-ON. The total switching loss can be obtained as follows.

\[ P_{sw} = \frac{1}{f} (N_{on} E_{on} + N_{off} E_{off}) \]  \hspace{1cm} (49)

where \(f\) is the fundamental frequency. \(N_{on}\) is the number of ON-states and \(N_{off}\) is the number of OFF-states. The total power losses of proposed inverter can be obtained using (46) and (49) as
Total power losses, \( P_{loss} = P_{C,avg} + P_{sw} \) \hspace{1cm} (50)

In this study, following parameters are considered to determine the power loss of proposed cascaded VS-MLI:

\[ R_L = 0.25 \, \Omega, \quad R_D = 0.11 \, \Omega, \quad V_L = 2.5 \, V, \quad V_D = 1.2 \, V, \quad \beta = 1, \quad t_{on} = t_{off} = 1 \, \mu s, \quad f = 50 \, Hz. \]

Each isolated DC voltage source has magnitude 12 V. The load resistance is 15 Ω. The mathematical calculation is carried out for each switch (MOSFET) for one cycle using Equations (42)–(50) and total power loss for one second is obtained as 3.624 mW.

Figure 5. Comparison between different topologies in terms of (a) number of required IGBTs, (b) number of gate drivers and (c) magnitude of blocking voltage across the switches.

Source: [1] Babaei and Hosseini (2009), [2] Banaei and Salary (2011), [3] Jannati Oskuee et al. (2014), [4] Gupta and Jain (2014a), [5] Mokhberdoran et al. (2014), [6] Sabahi et al. (2013), [7] Haque (2004), [8] Babaei et al. (2007), [9] Babaei (2008), [10] Ebrahimi et al. (2012), [11] Shalchi Alishah et al. (2015), [12] Salary et al. (2015).
6. Comparative study

In this section, the proposed cascaded VS-MLI has compared with similar asymmetric structure (Babaei, 2008; Babaei et al., 2007; Ebrahimi et al., 2012; Haque, 2004; Shalchi Alishah et al., 2015) and some of symmetrical structure (Babaei & Hosseini, 2009; Banaei & Salary, 2011; Gupta & Jain, 2014a; Jannati Oskuee et al., 2014; Mokhberdoran et al., 2014; Sabahi et al., 2013; Shalchi Alishah et al., 2015) in terms of the number of IGBTs/MOSFETs, gate drivers and MBV across the switches. The comparison between proposed configuration for cascaded VS-MLI and configurations presented in Babaei (2008), Babaei and Hosseini (2009), Babaei et al. (2007), Banaei and Salary (2011), Ebrahimi et al. (2012), Gupta and Jain (2014a), Haque (2004), Jannati Oskuee et al. (2014), Mokhberdoran et al. (2014), Sabahi et al. (2013), Shalchi Alishah et al. (2015) are shown in Figure 5(a). This figure indicates that the proposed configuration requires less number of IGBTs/MOSFETs for same voltage levels compared to other topologies for both symmetrical and asymmetrical structures. Figure 5(b) shows the comparison between gate drivers and number of voltage levels. As conclude from the figure, the proposed configuration and topology presented in Shalchi Alishah et al. (2015) requires fewer gate
7. Results and discussion

To verify the performance of proposed configurations, the simulation using MATLAB Simulink environment and experimental studies are presented, for 15-level inverter based on single sub-MLI as shown in Figure 1 and 25-level inverter using cascaded VS-MLI as shown in Figure 2.

7.1. Simulation results

The equivalent circuit of 15-level inverter of proposed configuration is depicted in Figure 6(a), the circuit consists of six auxiliary, four unidirectional switches and seven DC sources with the magnitude of 12 V, which produce the staircase voltage waveform of maximum output voltage 84 V. A series
R-L branch ($R = 15 \, \Omega$ and $L = 20 \, \text{mH}$) considered as load parameters for all cases. The waveforms of output voltage and load current of the 15-level inverter are shown in Figure 6(b), harmonic spectrum of the 15-level output voltage is shown in Figure 6(c). Another 25-level inverter based on cascaded VS-MLI configuration has been implemented as shown in Figure 7(a). The 25-level inverter requires only two auxiliary switches and four DC supplies with magnitude of $V_1 = 8 \, \text{V}$ and $V_2 = 40 \, \text{V}$. This proposed 25-level inverter generates maximum output voltage of 96 V, 3.96% THD. The waveforms of output voltage and load current of the 25-level inverter are shown in Figure 7(b), harmonic spectrum of the output voltage is shown in Figure 7(c).

7.2. Experimental results
To validate the simulation and effectiveness of the proposed configuration, a prototype of proposed single phase 15-level and 25-level inverter have been developed in the laboratory. The hardware
implementation of 15-level inverter is shown in Figure 8. It consists of IRF540 MOSFETs, which are driven by MCT2E optocouplers. The load parameters are used same as in simulation study. dSPACE DS 1104 real time controller has been used for real-time simulation for switching control design in MATLAB/SIMULINK environment. The developed code of Simulink model of switching algorithm is electronically generated by real time of MATLAB in conjunction with real-time interface of dSPACE. The generated C-code is downloaded into dSPACE hardware for implementation and generation of switching signals for MOSFETs switches. A digital oscilloscope of TEKTRONIX TPS 2014C and power analyser (FLUK-434) are used for recording all the waveforms. The output voltage and load current waveforms of implemented 15-level and 25-level inverter at 2 kHz carrier frequency with harmonic spectrum are shown in Figures 9 and 10. The experimental results have corroborated with simulation results.

To analyse the dynamic performance of the proposed configuration, the change in load at output terminals and a step change in modulation index at input side are considered for 15-level inverter.
The response is shown in Figure 11 for a variation in load. The load variation is obtained by adding extra resistance and thereby load current is changed in inverter. It is observed that the change in load current does not influence the output voltage. A step change in modulation index ($m = 0.6$ and $0.3$ for $0.02$ s) in 1 cycle ($20$ ms) is applied as shown in Figure 12(a). The output voltage levels are reduced to 5-level from 15-level and also load current has been decreased during change in modulation index as depicted in Figures 12(b) and (c).
8. Conclusion
In this study, an optimal configuration for cascaded VS-MLI has been presented. In comparison with other mentioned topologies, the proposed configuration needs the least components count. The reduction in number of components leads to reduce the installation area, cost economy, simple modulation control and less power loss which improves the efficiency of inverter. In addition, the voltage stress on switches has reduced, and also maximise the higher voltage levels. A modified multicarrier based pulse width modulation scheme has presented for proposed 15-level inverter. The performance of proposed cascaded VS-MLI under steady state and dynamic conditions has been verified through simulation and experimental on single phase 15-level and 25-level inverter prototype. The proposed cascaded VS-MLI is to be suitable for high voltage application due to reduced voltage stress on switches.
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Author details
Kishor Thakre1
E-mail: thakrekishor26@gmail.com
Kanungo Barada Mohanty1
E-mail: kmohanty@nitk.ac.in
Vinaya Sagar Kommukuri1
E-mail: vnskommukuri@gmail.com
Aditi Chatterjee1
E-mail: contactaditi247@gmail.com

1 Department of Electrical Engineering, National Institute of Technology Rourkela, Odisha 769008, India.

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