An extensive electrostatic analysis of dual material gate all around tunnel FET (DMGAA-TFET)

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Abstract

In the proposed work an analytical model of a p-channel dual material gate all around tunnel FET (DMGAA-TFET) is presented and its performance is compared with the conventional GAA-TFET. The electrostatic potential profile of the model is obtained using 2-D Laplace’s solution in the cylindrical coordinate system. A quantitative study of the drain current has been carried out using electric field in the z-axis and tunneling path. However the potential and current analysis is prolonged to different combinations of gate length in the DMGAA-TFET model. The results show an improvement in drain current and subthreshold swing as compared to GAA-TFET, which makes this model a potential replacement for low power application. Also the effect of scaling of the gate oxide thickness and cylindrical pillar diameter on the surface potential, initial tunneling point and tunneling current are analyzed.

Keywords: DMGAA-TFET, work function, BTBT tunneling, drain current

Classification numbers: 2.00, 2.07, 3.00, 3.02, 4.00, 4.12, 6.01

1. Introduction

As the conventional metal-oxide-semiconductor field effect transistor (MOSFETs) scaled beyond its physical limit, it suffers from high subthreshold swing (SS), high leakage current (I_{OFF}) and other short channel effects (SCEs) like threshold voltage roll-off and drain induced barrier lowering (DIBL) [1–4]. Many researchers employed a number of multi-gate silicon on insulator metal-oxide-semiconductor (MOS) technology to improve the device performance by enhancing the gate control over channel from various sides [5–8]. However gate all around (GAA) MOS provides highest degree of control over channel and lowest characteristics length with the reduction of various SCEs compared to omega/pi-gate, tri-gate, double-gate and single-gate structures [9–11]. That also demonstrates the maximum scaling capability and strong electric field confinement of the structure. But the key concern of GAA-MOS device is that it offers high subthreshold swing and leakage current in the subthreshold region which makes the device incompatible for low power and steeper switching applications [12, 13].

GAA tunnel FET (TFET) is the likely alternative for MOS technology which has the capability to reduce SS limit and improve the device scaling performance. Also it reduces different SCEs because of gated p-i-n structure. The movement of charge carriers in TFET is due to the non-local band-to-band tunnelling (BTBT) process and is independent of temperature variation [14–18]. It also offers better electrostatic control over the channel due to cylindrical gate confinement [9]. A number of analytical models have been proposed to compute the potential and drain current of multi-gate TFET by using Kane’s model [19–22]. However GAA-TFET provides low on-state drain current and high off-state
leakage current compared to bulk technology due to tunneling process [23]. The improvement of on-current in TFET can be achieved by optimizing the band-gap energy of semiconductors [24]. The gate engineering can be employed to enhance the tunnel current and to optimize the device parameters as proposed by Saurabh et al [25, 26].

In this paper a dual material gate all around TFET (DMGAA-TFET) analytical model is developed which has two regions with different work functions cascaded to each other. The region-1 is having higher work function as compared to region-2. The change in surface potential due to work function difference results in improvement of gate control over tunneling process and thus drain current increases compared to single material. The model provides high tunneling current with reduced DIBL and better scaling of oxide thickness and cylindrical pillar diameter. In this work the entire channel length is considered as 30 nm. The behavior of electrostatic potential and drain current for different combinations of gate length such as L1 = 10 nm and L2 = 20 nm, L1 = 15 nm and L2 = 15 nm, L1 = 20 nm and L2 = 10 nm are observed. The combination L1 = 20 nm and L2 = 10 nm shows better performance compared to other combinations. The effect of scaling of tox and tsio on electrical parameters is also studied.

2. Analytical model of DMGAA-TFET

The cross-sectional view of a p-channel dual material GAA-TFET structure is shown in figure 1. The source and drain regions are heavily doped with pentavalent and trivalent impurity of concentration 10^{20} cm^{-3} respectively. The channel region is un-doped and made up of intrinsic material with negligible trivalent concentration of 10^{15} cm^{-3}. For the given model two different metals having worked function \( \phi_{M1} = 4.9 \text{ eV} \) and \( \phi_{M2} = 4.7 \text{ eV} \) are considered as the gate metal contacts. The entire channel is divided into two regions (region-1 and region-2) as depicted in figure 1. The effective length of these non-overlapping channel regions are L1 and L2 respectively. However the low-k dielectric SiO2 is used as the gate oxide layer having thickness \( (t_{ox}) = 2 \text{ nm} \). The diameter of silicon cylindrical pillar \( (t_{si}) \) is taken as 10 nm. Here the length of both metallic regions is varied keeping the work function and total channel length constant.

The effect of doping concentration of channel on analysis of electrical parameters is neglected as the channel is considered as intrinsic and is lightly doped with a concentration of 10^{15} approximately. The electrostatic potential of both the channel regions have been obtained by solving the 2-D Laplace’s equation which is obtained by neglecting the electron space charge.

\[
\frac{1}{r} \frac{\partial}{\partial r} \left( r \frac{\partial \varphi_j(r,z)}{\partial r} \right) + \frac{\partial^2 \varphi_j(r,z)}{\partial z^2} = 0 \quad j = 1, 2. \tag{1}
\]

Here \( \varphi_1(r,z) \) and \( \varphi_2(r,z) \) denote the electrostatic potentials in the channel region-1 and region-2 respectively. The above equation can be used to compute the surface potential at the gate-channel interface and center potential at the center of cylindrical pillar for both channel regions

\[
\varphi_j(r,z)|_{z=0} = \varphi_{i0}(z), \tag{2}
\]

\[
\varphi_j(r,z)|_{r=\frac{L_j}{2}} = \varphi_{i0}(z). \tag{3}
\]

The solution of above Laplace’s equation in both regions has been resolved using 2nd order polynomial approximation [13]

\[
\varphi_j(r,z) = a_{0j}(z) + r a_{1j}(z) + r^2 a_{2j}(z). \tag{4}
\]

The boundary conditions are required to predict the z-dependent coefficients \( a_{0j}, a_{1j} \) and \( a_{2j} \) for both the regions. The electric field at the center of cylinder and gate-channel interface for both regions are [9]

\[
E_j(r,z)|_{z=0} = a_{1j}(z) = 0, \tag{5}
\]

\[
E_j(r,z)|_{r=\frac{L_j}{2}} = \left. -\frac{d\varphi_j(r,z)}{dr} \right|_{r=\frac{L_j}{2}} = C_{ox}(V_{GS} - V_{FBj} - \varphi_{i0}(z)) \tag{6}
\]

\[
= \frac{C_{ox}}{\epsilon_{si}} a_{2j}(z),
\]

\[
= \frac{C_{ox}}{\epsilon_{ox}} a_{2j}(z),
\]
where

\[ C_{ox} = \frac{2 \varepsilon_{ox}}{t_u \ln \left(1 + \frac{2m}{t_u}\right)}. \]  

(7)

Here \( \varepsilon_{st} \) is the dielectric permittivity of silicon, \( C_{ox} \) is the oxide capacitance, \( \varepsilon_{ox} \) is the permittivity of oxide layer and \( V_{GS} \) is gate-to-source bias. However \( V_{FBi} \) denotes the flat-band voltage of both the regions, which is independent of gate length and can be calculated through the work function of materials

\[ V_{FBi} = \varphi_{Mi} - \varphi_{si}, \]

(8)

where \( \varphi_{Mi} \) and \( \varphi_{si} \) represents the work function of material for \( j_{au} \) region and silicon work function respectively.

The essential boundary conditions at the interface of both the channel regions are required to solve equation (1). The potential profile and lateral electric field for both the regions are same at the interface

\[ \varphi_1(r, z)|_{z=L_1} = \varphi_2(r, z)|_{z=L_1}, \]

\[ \left. \frac{d\varphi_j}{dz} \right|_{z=L_1} = \left. \frac{d\varphi_j}{dz} \right|_{z=L_1}. \]

(9)

(10)

Using the above boundary conditions at the center of the cylindrical pillar, channel-SiO\(_2\) interface and dual region interface, the potential profile of the cylindrical structure is found to be

\[ \frac{\partial^2 \varphi_j(z)}{\partial z^2} + \frac{(V_{GS} - V_{FBj} - \varphi_j(z))}{\lambda^2} = 0, \]

(11)

where \( \lambda \) is known as the natural length of cylindrical structure and is expressed as

\[ \lambda = \sqrt{\frac{\varepsilon_{st}t_u}{4C_{ox}}} \sqrt{\frac{t_u^2\varepsilon_{si} \ln \left(1 + \frac{2m}{t_u}\right)}{8\varepsilon_{st}}}. \]

(12)

The surface potential of the cylindrical structure \( \varphi_j(z) \) is related to the center potential \( \varphi_j(0) \) as \([25]\)

\[ \varphi_j(z) = (H^2 + 1)\varphi_j(0) - H^2(V_{GS} - V_{FBj}), \]

(13)

where

\[ H = \frac{t_u}{4\lambda}. \]

(14)

Differentiating equation (13), we get

\[ \frac{\partial^2 \varphi_j(z)}{\partial z^2} = \frac{\partial^2 \varphi_j(0)}{\partial z^2}. \]

(15)

Now equation (11) becomes

\[ \frac{\partial^2 \varphi_j(z)}{\partial z^2} + \frac{(V_{GS} - V_{FBj} - \varphi_j(0))}{\lambda^2} = 0. \]

(16)

The surface potential for both the channel regions are obtained by solving equation (16).

For region-1 \((0 \leq z \leq L_1)\)

\[ \varphi_{1i}(z) = C_1 e^{\left(\frac{z}{\lambda}\right)} + D_1 e^{-\left(\frac{z}{\lambda}\right)} + V_{GS} - V_{FBi}. \]

(17)

Similarly the surface potential for region-2, \((L_1 \leq z \leq L_1 + L_2)\), is expressed as

\[ \varphi_{2i}(z) = C_2 e^{\left(\frac{z}{\lambda}\right)} + D_2 e^{-\left(\frac{z}{\lambda}\right)} + V_{GS} - V_{FB2}. \]

(18)

For the above expressions the coefficients \( C_1, C_2, D_1 \) and \( D_2 \) can be calculated using the potential boundary conditions at the source and drain end \([27]\)

\[ \varphi_{1i}(z)|_{z=0} = V_{bi}, \]

\[ \varphi_{2i}(z)|_{z=L_1+L_2} = V_{DS}. \]

(19)

(20)

Here \( V_{bi} \) is the built-in-potential, \( V_{DS} \) is the voltage applied at the drain terminal and \( L_1 + L_2 \) is the maximum channel length of the device. Equating equations (17) and (18) using the boundary conditions at source-channel and drain-channel interface, we found

\[ C_1 = \frac{-2k_1(e^{-L_2/\lambda} - e^{-L_1/\lambda}) + 2k_2(e^{-L_2/\lambda} + e^{L_2/\lambda})}{4\sinh ((L_1 + L_2)/\lambda)}, \]

(21)

\[ D_1 = \frac{-2k_1(e^{-L_2/\lambda}) - 2k_2(e^{-L_1/\lambda} + e^{L_2/\lambda})}{4\sinh ((L_1 + L_2)/\lambda)}, \]

(22)

\[ C_2 = \frac{-2k_1(e^{-L_1/\lambda}) + 2k_2(e^{-L_1/\lambda} + e^{L_1/\lambda}) + 2k_3}{4\sinh ((L_1 + L_2)/\lambda)}, \]

(23)

\[ D_2 = \frac{2k_1(e^{L_2/\lambda}) - 2k_2(e^{L_1/\lambda} + e^{L_1/\lambda})}{4\sinh ((L_1 + L_2)/\lambda)}, \]

(24)

where

\[ k_1 = V_{FBi} - V_{GS} + V_{bi}, \]

(25)

\[ k_2 = V_{FBi} - V_{FB2}, \]

(26)

\[ k_3 = V_{FB2} - V_{GS} + V_{DS}. \]

(27)

However the center potentials of both the channel regions can be obtained using equation (13). The center potentials of region-1 and region-2 are expressed as

\[ \varphi_{1i}(z) = (H^2 + 1)\left(C_1 e^{\left(\frac{z}{\lambda}\right)} + D_1 e^{-\left(\frac{z}{\lambda}\right)} + V_{GS} - V_{FBi}\right), \]

\[ - H^2(V_{GS} - V_{FBi}). \]

(28)

\[ \varphi_{2i}(z) = (H^2 + 1)\left(C_2 e^{\left(\frac{z}{\lambda}\right)} + D_2 e^{-\left(\frac{z}{\lambda}\right)} + V_{GS} - V_{FB2}\right), \]

\[ - H^2(V_{GS} - V_{FB2}). \]

(29)

In conventional TFET the tunneling of charge carriers is primarily based on is non-local BTBT mechanism \([28–30]\).
For GAA-TFET the tunneling process is dominant in the lateral direction of cylindrical body. So it is desired to find the lateral field in both the channel regions which helps us to calculate the tunneling current. However the lateral electric fields in both the regions are obtained by differentiating the potential profile in the range of $0 \leq z \leq L_1$ and $L_1 < z < L_1 + L_2$

$$E_1(z) = -\frac{\partial \varphi_1(z)}{\partial z} = -\frac{C_i}{\lambda} e^{-\frac{z}{\lambda}} + \frac{D_1}{\lambda} e^{-\frac{z}{\lambda}},$$

$$E_2(z) = -\frac{\partial \varphi_2(z)}{\partial z} = -\frac{C_2}{\lambda} e^{-\frac{z}{\lambda}} + \frac{D_2}{\lambda} e^{-\frac{z}{\lambda}}.$$ (30)

### 3. Drain current analysis

In non-local BTBT the tunneling of charge carriers starts only when the conduction band of source gets in-line with the valence band of channel region [31]. At zero gate bias a small amount of band bending arises at the source-channel interface, because of the presence of built-in-potential. This condition is known as OFF-state condition of the device as depicted in figure 2(a). In this state the current in the channel is insignificant due to the absence of band-to-band tunneling. Further increase of gate bias results significant amount of band bending. When the applied gate potential attains a critical value ($V_{th}$), the conduction band of source and valence band of channel gets aligned to each other. For $V_{GS} > V_{th}$, the drain current increases exponentially due to the improvement in tunneling volume as depicted by the area under the solid lines in figure 2(b).

In the ON-state the tunneling path is the lateral distance between the two tunneling points $z_1$ and $z_2$. The initial tunneling point is the value of $z$ for which the surface potential changes by an amount of unit band gap energy per elementary charge ($E_g/q$). However this point plays a decisive role in the extraction of drain current. In this model $z_1$ is assumed to lie in the region-1 ($0 \leq z_1 \leq L_1$), because the region-1 is surrounded by the metal with higher work function. So the tunneling distance $z_1$ can be obtained by using the surface potential profile at the interface and at the critical threshold point

$$\varphi_1(z)|_{z=z_1} = \frac{E_g}{q}$$

$$\varphi_1(z)|_{z=z_0} = V_{th}.$$ (32)

$$\varphi_1(z)|_{z=z_1} = \varphi_1(z_2) + \frac{E_g}{q} = C_i e^{k_1} + D_1 e^{-k_1} + V_{GS} - V_{FB1} + \frac{E_g}{q}.$$

$$z_1 = \lambda \ln \left( \frac{(k_1 - E_g/q) - \sqrt{(k_1 - E_g/q)^2 - 4C_iD_1}}{2C_i} \right).$$ (34)

where $E_g$ is the band-gap energy of silicon at equilibrium. $z_1$ can be further reduced by optimizing band-gap energy of semiconductor and increasing the gate potential ($V_{GS}$). Low $z_1$ increases the tunneling path along the channel and hence the drain current is improved. In this model the tunneling volume is not affected by the drain voltage for constant $V_{GS}$. This is because the effect of electron charge injected into the channel from the drain end has been neglected in equation (1).

The drain current can be calculated by integrating BTBT generation rate over the entire tunneling volume in both the radial and lateral directions. However, for the present model the current is obtained in the lateral direction of channel from $z_1$ to $z_2$ using Kane’s direct tunneling phenomena [32]. Here $z_2$ lies in the region-1 due to sharp reduction of the surface potential and $z_2$ lies in the region-2 due to charge accumulation at drain end as shown in figure 2(b). So the drain current is expressed as

$$I_D = \frac{q}{\lambda} \int_{z_1}^{z_2} dz \int_{z_1}^{z_2} dr \left( \frac{E_g}{q} e^{-qB_{kane}/E_g} \right),$$ (35)

where $A_{kane}$ and $B_{kane}$ are tunneling dependent Kane’s parameters having values: $A_{kane} = 4 \times 10^{15}$ m$^{-1/2}$ V$^{-5/2}$ s$^{-1}$ and $B_{kane} = 1.9 \times 10^9$ V m$^{-1}$ [33].

On simplifying equation (35), we get

$$I_D = \frac{q}{\lambda} \int_{z_1}^{z_2} dz \int_{z_1}^{z_2} dr \left( \frac{E_g}{z} e^{-qB_{kane}/E_g} \right).$$ (36)
Here both the channel regions involve tunneling process as \( z_1 < L_1 \) and \( z_2 > L_2 \). Hence the tunneling volume is calculated by integrating the generation rate over both regions and is expressed as

\[
I_D = I_{D1} + I_{D2},
\]

where \( I_{D1} \) and \( I_{D2} \) are the drain current in the channel region-1 and region-2 due to non-local tunneling process. Substituting the value of lateral electric field of both regions, we get

\[
I_{D1} = \frac{I_0 E_l A_{kane}}{\lambda} \left[ -\frac{C_1}{\lambda} \left( \frac{1}{z} - \frac{q B_{kane}}{E_g} \right) \right] L_1 + \frac{D_1}{\lambda} \int_{z_1}^{z_2} dz \frac{1}{z} e^{-\frac{1}{\lambda} \left( \frac{q B_{kane}}{E_g} \right) z},
\]

\[
I_{D2} = \frac{I_0 E_l A_{kane}}{\lambda} \left[ -\frac{C_2}{\lambda} \left( \frac{1}{z} - \frac{q B_{kane}}{E_g} \right) \right] L_2 + \frac{D_2}{\lambda} \int_{z_1}^{z_2} dz \frac{1}{z} e^{-\frac{1}{\lambda} \left( \frac{q B_{kane}}{E_g} \right) z}.
\]

In equation (44) the exponential parameter \( P_2 \ll P_1 \) and \( Q_2 \ll Q_1 \), for \( z_2 > L_2 \). So neglecting the nominal effects of \( P_2 \) and \( Q_2 \) in the drain current analysis, we found

\[
I_D = I_{D1} + I_{D2} = \frac{I_0 E_l A_{kane}}{\lambda} \left[ \frac{C_2 P_{L1}}{\lambda} - \frac{D_2 Q_{L1}}{\lambda} \right] + \frac{D_2 Q_{L1}}{\lambda} \left( \frac{1}{\lambda} + \frac{q B_{kane}}{E_g} \right).
\]

The final drain current expression is obtained as

\[
I_D = \left( I_{D1} + I_{D2} \right) = \frac{I_0 E_l A_{kane}}{\lambda} \left[ \frac{C_2 P_{L1}}{\lambda} - \frac{D_2 Q_{L1}}{\lambda} \right] + \frac{D_2 Q_{L1}}{\lambda} \left( \frac{1}{\lambda} + \frac{q B_{kane}}{E_g} \right).
\]

4. Results and discussion

Figure 3 shows the variation of surface potential along the 30 nm channel for single material and dual material gate. The gate lengths of both the regions are varied and their impact on potential is observed. The dual material having \( L_1 = 20 \) nm and \( L_2 = 10 \) nm produces minimum surface potential and sharp slope as compared to other combinations. This is
because of higher work function and larger gate length of the region-1. The sharp reduction of potential is responsible for increase of the BTBT tunneling volume and drain current. So for this model, current analysis has been done with gate length $L_1 = 20 \text{ nm}$, $L_2 = 10 \text{ nm}$ and results are compared with different combinations of dual gate lengths.

The center potential at $r = 0$ and surface potential at $r = t_{\text{ox}}/2$ of the DMGAA-TFET are compared for different gate voltages in Figure 4. For a constant gate voltage the center potential lies above the surface potential. This is due to higher influence of gate bias at the channel interface. In the present analysis surface potential based approach is followed for the calculation of tunneling current.

The surface potential profile for the proposed model with different gate voltages at a constant drain voltage are illustrated in the figure 5(a). The potential is stuck to built-in-potential ($V_{\text{bi}}$) at the source interface and $V_{\text{DS}}$ at drain interface as per the boundary condition. The surface potential in both the channel regions reduces with increase in gate voltage at $V_{\text{DS}} = -0.1 \text{ V}$. Therefore the slope of the surface potential is getting sharper and the minimum potential is achieved early. The sharp slope of the potential for higher gate voltage indicates the larger tunneling volume. However the potential of entire channel of GAA-TFET varies linearly. This is due to the impact of drain bias over both the channel regions. Figure 5(b) shows the surface potential of the proposed device for various drain voltages. It is observed that the slope of the reduced potential profile is not affected by the increment of the drain voltage as the effect of electron space charge has been ignored in equation (1). Hence there will be no significant drain induced barrier lowering (DIBL) effect in the model, so the tunneling current is not affected by drain bias.

Figure 6 demonstrates the effect of reducing gate oxide thickness and pillar diameter on the surface potential and the results are compared to the conventional GAA-TFET. Unlike the orthodox model, the potential of DMGAA-TFET decreases as we go on reducing $t_{\text{ox}}$ and $t_{\text{si}}$. The potential is minimized further due to the influence of gate bias on channel at low oxide thickness and pillar diameter. Dual material GAA-TFET shows reduced and sharp slope potential profile as compared to single material gate.

Figure 7 shows the behavior of lateral electric field of the model and that has been compared with the different combinations of gate length. It is clearly seen that the electric field varies non-linearly for the entire channel for a constant gate and drain bias and the field exists for both the channel regions. However the lateral field plays a vital role in the calculation of tunneling volume over the entire channel.

The initial tunneling points for different values of gate length as a function of gate voltage are shown in Figure 8. The results are compared to the conventional GAA-TFET. As the gate voltage increases beyond threshold, the charge carriers tunnel from source to channel which results $z_1$. Lower the $z_1$, better the tunneling volume. Inclusion of dual material gate results in low $z_1$, hence improves the device performance. For the proposed model the combination of the gate lengths $L_1 = 20 \text{ nm}$ and $L_2 = 10 \text{ nm}$ yields best result because of sharp slope of surface potential. The sharp reduction of surface potential reduces threshold voltage, hence achieves tunneling earlier.

For a constant gate oxide thickness and cylindrical pillar diameter, $z_1$ reduces with increase in gate voltage beyond threshold. As the gate oxide thickness ($t_{\text{ox}}$) is scaled from 3 to 1 nm for radii of 5 nm, more tunneling volume is achieved because of the reduction of $z_1$ as depicted in Figure 9(a). This is due to the impact of gate bias on channel with low oxide thickness. Reduction in $z_1$ enables the flow of charge carriers for small value of $V_{\text{GS}}$. Similarly Figure 9(b) displays the variation of $z_1$ versus $V_{\text{GS}}$ for different Si pillar diameter for the dual material model. When the diameter of cylindrical pillar reduces, the gate control on the channel is dominant and thereby reduces $z_1$ marginally. Therefore the scaling of $t_{\text{ox}}$ and $t_{\text{si}}$ improves the drain current performance of DMGAA-TFET

Figure 10 shows $I_D$-$V_{\text{GS}}$ characteristics for GAA-TFET in linear and logarithmic scale. The drain current analysis is done for different combinations of gate length as a function of gate voltage. As the gate bias increases beyond threshold, the tunneling current flows from source to drain end along the lateral direction. However the on current performance of dual material gate is better as compared to single material, because of sharp potential reduction and minimum threshold achievement. Here also the gate length combination $L_1 = 20 \text{ nm}$ and $L_2 = 10 \text{ nm}$ yields better performance in comparison with other lengths as the BTBT current primarily influenced by the sharp potential profile near the source-channel interface. The drain current improves exponentially for $V_{\text{GS}} > V_{\text{th}}$ due to dominant tunneling process in both channel regions. Figure 10(b) displays the logarithmic drain current versus $V_{\text{GS}}$. The model produces drain current in the range of $10^{-5} \text{ A}$ compared to single gate model ($10^{-6} \text{ A}$) depicted in figure 10(b). High $I_{\text{ON}}$ and low $I_{\text{OFF}}$ can be achieved because of large $L_1$ and small $L_2$, respectively. So the gate length combination $L_1 = 20 \text{ nm}$ and $L_2 = 10 \text{ nm}$ provides maximum $I_{\text{ON}}$ to $I_{\text{OFF}}$ ratio.
Figure 5. Variation of surface potential along the channel at different (a) gate voltages and (b) drain voltages.

Figure 6. Surface potential distribution of the model with single material gate and proposed dual material gate along the channel due to the variation of (a) gate oxide thickness and (b) cylindrical pillar diameter.

Figure 7. Lateral electric field along the channel length of the device with single material gate and different length based dual material gate.

Figure 8. Variation of initial tunneling point ($z_1$) versus gate voltage for different combinations of gate length.
Figure 9. Impact of (a) gate oxide scaling and (b) cylindrical pillar diameter scaling on initial tunneling point ($z_1$) versus gate voltage.

Figure 10. Characteristics of drain current $I_D$ versus gate voltage $V_{GS}$ for p-channel GAA-TFET with single-material and dual-material gate. The drain current is plotted on (a) linear scale, (b) logarithmic scale.

Figure 11. Characteristics of drain current $I_D$ versus drain voltage $V_{DS}$ for the model (a) with different gate length combination in dual-material gate at constant gate voltage, and (b) with fixed gate length in dual-material gate for different gate voltages.
The $I_D-V_DS$ characteristics for different gate length combinations are shown in figure 11(a) at constant gate bias. In the ON state the drain current is independent of drain voltage, because of the dominancy of gate bias. The independent nature of drain current versus $V_DS$ is due to the fact that the electron space charge has been neglected in the electrostatic potential analysis. At $V_{GS} = -1$ V, the conventional GAA-TFET produces current of order $10^{-10}$ A. This negligible amount of current resulted, because at $V_{GS} = -1$ V the device operates at cut-off. Whereas with the same gate voltage DMGAA-TFET yields higher drain current of order $10^{-8}$ A with low threshold. However the device with higher region-1 dimension gives better on current performance at constant gate voltage. Figure 11(b) shows the $I_D-V_DS$ characteristics of DMGAA-TFET for different gate voltages. It is clearly observed that increase in gate voltage beyond threshold results increment in drain current.

Figures 12(a) and (b) display the effect of $t_{ox}$ and $t_{si}$ variation on drain current. Figure 12(a) shows significant increment of drain current with reduction in oxide thickness for the model, because of the small value of initial tunneling point. This leads to larger tunneling volume in non-local direct tunneling process and hence results large tunnel current. Similarly the effect of scaling of $t_{si}$ on drain current for different combinations of gate length is depicted in figure 12(b). It is clearly observed that high drain current is obtained at lower thickness of the cylinder due to higher influence of gate on channel. The BTBT tunneling takes place faster for small diameter and conversely improves the tunneling current. Comparing the results for different combinations of gate length, $L_1 = 20$ nm and $L_2 = 10$ nm gives better performance. Figures 13(a) and (b) show the effect $t_{si}$ and $t_{ox}$ scaling on $I_D$ versus $V_{GS}$ characteristics of DMGAA-TFET and concluded that higher drain current is achieved at low $t_{ox}$ and low $t_{si}$ due to gate-dominant tunneling process. As we scaled down the $t_{si}$ from 10 to 6 nm, the tunneling current improves by a factor of 10 as given in figure 13(a). However in the subthreshold region ($V_{GS} < V_{th}$), the effect of the variation of $t_{si}$ is insignificant on drain current due to the absence of tunneling of carriers.

Subthreshold swing (SS) can also be calculated for different gate voltages in the subthreshold region and compared
to single-material GAA-TFET as shown in Table 1. DMGAA-TFET produces low SS for $V_{GS} < V_{th}$.

Therefore this model can be a potential candidate for ultra-low power CMOS applications in the near future due to vast improvement of drain current at low subthreshold swing.

### 5. Conclusion

In this paper a 2-D analytical model for p-channel DMGAA-TFET is developed. The work proposes the potential profile of two channel regions for different gate length ratios. This results improved drain current compared to conventional GAA-TFET. The impact of work function, gate length, gate oxide thickness and cylindrical body diameter on the drain current and initial tunneling point are discussed. The drain current is improved approximately by a factor 10 for DMGAA-TFET compared to conventional GAA-TFET. Also the improved SS resulted for the present model (30 ~ 40 mV/decade) allows the device to be a promising candidate for low power and high speed application.

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### Table 1. Comparison of subthreshold swing for different models.

| $V_{DS}$ (V) | $t_{m}$ (nm) | $t_{d}$ (nm) | Subthreshold swing (mV/decade) |
|--------------|--------------|--------------|-------------------------------|
| GAA-TFET     | L = 30 nm    |              |                               |
|              | L$_{1}$ = 10 nm, L$_{2}$ = 20 nm | 38           |                               |
| L$_{1}$ = 15 nm, L$_{2}$ = 15 nm | 38           | 32           |                               |
| L$_{1}$ = 20 nm, L$_{2}$ = 10 nm | 34           | 30           |                               |

| DMGAA-TFET   |              |              |                               |
|--------------|--------------|--------------|-------------------------------|
|              |              |              |                               |
|              |              |              |                               |
|              |              |              |                               |

| DMGAA-TFET   |              |              |                               |
|--------------|--------------|--------------|-------------------------------|
|              |              |              |                               |
|              |              |              |                               |
|              |              |              |                               |

| DMGAA-TFET   |              |              |                               |
|--------------|--------------|--------------|-------------------------------|
|              |              |              |                               |
|              |              |              |                               |
|              |              |              |                               |

| DMGAA-TFET   |              |              |                               |
|--------------|--------------|--------------|-------------------------------|
|              |              |              |                               |
|              |              |              |                               |
|              |              |              |                               |