Type-II Compensation for Automotive Buck Converters Implemented by Fully Integrated Capacitor Multiplier

PAUL COSTE\(^1\), ISTVÁN KOVÁCS\(^1\), MARIUS NEAG\(^{\odot1}\), (Member, IEEE), ALINA-TEODORA GRĂJDEANU\(^{\odot1}\), VLAD-ALEXANDRU IONESCU\(^2\), AND MARINA DANA ŢOPA\(^1\), (Member, IEEE)

\(^1\)Department of Bass of Electronics, Technical University of Cluj-Napoca, 400114 Cluj-Napoca, Romania
\(^2\)Infineon Technologies Romania, 020335 Bucharest, Romania

Corresponding author: Marius Neag (marius.neag@bel.utcluj.ro)

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ABSTRACT This paper presents a solution for full integration of a Type-II compensation circuit for DC-DC buck converters. It employs a novel active circuit based on capacitor multiplier, able to emulate the R-series-C ensemble within the conventional Gm-RC compensation network. The proposed solution was used to design a current-mode DC-DC buck converter for automotive applications. The implementation of key circuits in a 180 nm CMOS process is presented in some detail. Simulation results demonstrate that the converter meets all design requirements: it provides a 5 V output voltage over wide ranges of the input voltage, 6 V to 45 V, and load current, between 10 mA and 300 mA. Its frequency and transient responses compare well against the performance of a similar converter that employs a conventional Gm-RC compensation circuit. It consumes 20 \(\mu\)A more, but requires significantly less die area, than its counterpart. Furthermore, the tuning required to compensate for process and temperature variations is realized by programming the multiplication factor of the capacitor multiplier.

INDEX TERMS Automotive, buck converter, capacitance multiplier, fully integrated DC-DC converter, type II compensation.

I. INTRODUCTION

The buck converter is one of the most popular Switch-Mode Power Supply (SMPS) topology [1]. It is widely used in complex power conversion and distribution systems, e.g. automotive systems, server motherboards, broadband communication boards, etc. [2]. In such systems, multiple converters are connected to a common battery voltage and generate the required local voltage levels such as 1.8 V, 3.3 V and/or 5 V [3], [4]. Fig. 1 presents the simplified block diagram of the buck converter with current mode control and a Type-II Gm-RC compensation network. Usually, \(C_1\), \(C_3\) and \(R_2\) are external components which have to be appropriately sized by the customer in order to maintain loop stability and converter performance over all conditions of operation.

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The quest for ever lower cost and smaller size demands to integrate as much of the system as possible. Full integration of the compensation network is particularly targeted as it reduces the bill of materials down to only the controller IC, the input decoupling and the LC output filter. However, to integrate the compensation network one has to deal with additional design challenges, such as: a). placing high value capacitors on-chip is very expensive, usually prohibitively so in standard CMOS processes b). users want control over key parameters of the compensation network in order to tailor them to their system requirements and c). the circuit topology should allow for a straightforward implementation of digital tuning or trimming, necessary to compensate for process, supply voltage and temperature (PVT) variations. These requirements can be met to some degree by using a high switching frequency and a programmable compensation network based on capacitor and/or resistor matrices. The former
usually leads to large dynamic power losses while the later require large die area.

An effective way to reduce the die area occupied by the integrated compensation network is to implement the large capacitor required by using a capacitor multiplier.

For example, the AO-RC Type-II compensation network presented in [5] is implemented by a floating capacitor multiplier. Reference [6] reports a buck converter with fully integrated compensation network based on a capacitor multiplier; the Gm-RC compensation network implemented by a capacitor multiplier resulted in a fast transient response of the converter presented in [7]. However, these solutions do not meet all the requirements described above: they do not provide for frequency tuning and have been demonstrated only for converters that operate over narrow input voltage ranges.

This paper presents a solution to fully integrate Type-II Gm-RC compensation networks. The $R_2$-series-$C_1$ ensemble shown in Fig. 1 is implemented by a novel capacitor multiplier based on one Gm cell with two outputs. Frequency tuning is realized effectively by programming the multiplication factor.

Section II presents the capacitor multiplier topology and the resulting Type-II compensation network. Mathematical analysis is followed by detailed description of the proposed transistor level implementation. Section III presents a current-mode automotive DC-DC buck converter that uses the proposed Gm-RC compensation designed in a 180 nm CMOS process. Simulation results obtained for this design are compared against the performance of the converter implemented with the conventional Gm-RC compensation, as well as against similar converters published previously. The main points of the topology and circuit implementation presented here are summarized in the last Section, which also discusses the main conclusions drawn from this work.

**FIGURE 1.** Current-mode DC-DC buck converter block diagram with Type-II compensation circuit.

**FIGURE 2.** (a) Block diagram of the capacitance multiplier proposed in [8], [9] and (b) simplified equivalent R-C circuit.

**II. TYPE-II FREQUENCY COMPENSATION NETWORK BASED ON CAPACITOR MULTIPLIER**

A. PROPOSED R-C EMULATOR BASED ON CAPACITOR MULTIPLIER: PRINCIPLE OF OPERATION AND IMPLEMENTATION

The block diagram of the capacitor multiplier introduced in [8] and [9] is shown in Fig. 2 (a). It uses a placed capacitance, $C_{\text{placed}}$, and one transconductor with two outputs called $\text{GmMult}$. A transconductor core realizes the necessary voltage-to-current conversion, then the resulting current, $i_{\text{Gm}}$, is conveyed to two distinct high impedance output stages. The output stages are modelled in Fig. 2 (a) by the current controlled current sources $\text{CCCS}_1$ and $\text{CCCS}_2$, that have the output resistors and capacitors $R_{\text{Out}1,2}$ and $C_{\text{Out}1,2}$. The current provided at $\text{Out}1$, $i_{\text{Out}1}$, is $K$ times larger than the one supplied by $\text{Out}2$, $i_{\text{Out}2}$. A negative feedback loop is closed around the transconductor $\text{GmMult}$ by connecting the output $\text{Out}2$ to the inverting input of the core.

The impedance seen at the circuit input, denoted $Z_{IN}$ in Fig. 2 (a), is purely capacitive if $R_{\text{Out}1}$ and $R_{\text{Out}2}$ can be considered infinitely large and capacitances $C_{\text{Out}1,2}$ can be neglected. In these conditions, the equivalent capacitance can be approximated by:

$$C_{\text{eq}} \approx C_{\text{placed}} \cdot M$$

where $M = 1 + K$ is the capacitance multiplying factor [9].

A more detailed analysis, considering the finite value of $R_{\text{Out}2}$, yields the equivalent impedance depicted in Fig. 2 (b). Besides the capacitance $C_{\text{eq}}$ which retains the expressions given by (1), the $Z_{IN}$ model comprises a parasitic series resistor, denoted $R_S$, and a parallel resistor, denoted $R_P$. The expressions of these parasitic resistors can be approximated as follows:

$$R_S \approx \frac{1}{\text{GmCore} \cdot M}$$

$$R_P \approx R_{\text{Out}1}$$

It follows that the output resistance $R_{\text{Out}2}$ should be made as large as possible in order to maximize the frequency range this circuit can be effectively used as a capacitor multiplier [9].

It was demonstrated in [9] that the effect the finite value of $R_{\text{Out}2}$ has on $Z_{IN}$ can be neglected by comparison; also, that
the capacitances $C_{Out1,2}$ have only a minor impact on $Z_{IN}$, if their values are kept in the hundreds of fF range by using usual design techniques such as cascoding.

A large resistance at the $Out_1$ output can be obtained by using gain boosting as in [9] or another one of the many circuit topologies described in [10]. The starting point for the approach used here is the current mirror with high output impedance introduced in [11], depicted in Fig. 3 (a). An important shortcoming is that the output voltage is limited to $V_{In} - V_{GS,Mfb}$; in general terms, the output voltage is not completely independent of the input voltage. This can be avoided by inserting a cascode transistor in the output path, as shown in Fig. 3 (b). The small-signal output resistance seen at the drain of the additional cascode $M_{cas1}$ can be approximated by:

$$R_{Out1} \approx g_{mMfb} \cdot rds_{Mfb} \cdot rds_{MOut1} \cdot g_m_{Mcas1} \cdot rds_{Mcas1} \quad (3)$$

An additional constant voltage, called $V_{cas}$ in Fig. 3 (b), is necessary to drive the gate of cascode $M_{cas1}$. This also enables the implementation of a second current output, called $i_{Out2}$ in Fig. 3 (b). The second output has a smaller output resistance than the main output, given by (3). Overall, the circuit depicted by Fig. 3 (b) is an effective way to implement a current mirror with two outputs, one with the very large resistance given by (3) and the other with the smaller, yet still fairly large output, resistance of a regular cascoded stage.

Equations (1) and (2) indicate that the structure presented in Fig. 2(a) can be used to implement a wanted R-C network, not only a capacitance multiplier as in [9]. Furthermore, the resulting R-C network has the useful feature that the product $C_{eq} \cdot R_s = C_{placed} / Gm_{CORE}$ does not dependent on the factor $M$.

Fig. 4 presents the proposed circuit implementation of the transconductor $Gm_{MULT}$. It uses a symmetrical topology that comprises an input differential pair with resistive degeneration, implemented by transistors $M_{InP}$, $M_{InM}$ and the resistor $R_{deg}$, and three current mirrors. The differential pair converts the input differential voltage into a signal current that is taken in by the two current mirrors encompassed by dotted-line rectangles. They use the circuit topology shown in Fig. 3 (b) but with complementary implementation. The signal current passing through $M_{InP}$ is conveyed directly to the outputs by the current mirror “B”- encompassed by the dotted-line rectangle on the top-right corner. The signal current passing through $M_{InM}$ is reflected by the current mirror “A” on the top-left corner of the schematic, then conveyed to the outputs by the current mirror “C” at the bottom of Fig. 4. Note that the current mirrors “B” and “C” have two outputs each: the ones with high-output impedance connected at node $Out_1$ and the simple cascoded outputs connected at node $Out_2$. Also, the signal current provided by the high-output impedance $Out_1$ is $K$ times larger than the one provided by the simple cascoded output $Out_2$.

### B. GM-RC FREQUENCY COMPENSATION NETWORK BASED ON THE PROPOSED CAPACITOR MULTIPLIER

Fig. 5 (a) presents the conventional Type-II $Gm$-RC frequency compensation network used for ensuring the stability of buck DC-DC converters [7], [12], [13]. The transconductor $Gm$ converts the difference between the reference voltage $V_{ref}$ and a scaled-down version of the buck output voltage, $V_{fb}$. The resulting current is applied to the RC network formed by $C_1$, $R_2$, $C_3$, and generate the error voltage signal, $V_e$. The transfer function $H(jf) = V_e / (V_{ref} - V_{fb})$ introduced by this circuit into the DC-DC converter loop gain comprises a pole and a zero [12]:

$$H(jf) = \frac{V_e}{V_{ref} - V_{fb}} = -H_{PB} \cdot (1 + \frac{jf}{f_p})$$

where:

$$H_{PB} = -\frac{R_b}{R_1 + R_b} \cdot \frac{Gm_{COMP} R_2 C_1}{C_1 + C_3}$$

$$f_p = \frac{1}{2 \pi R_2 C_1 C_3}; f_z = \frac{1}{2 \pi R_2 C_1}$$

The frequency compensation network provides a phase boost to the overall loop gain of the buck converter. For maximum impact on the phase margin, the phase boost should reach its maximum value at the crossover frequency of the converter loop gain [12], [13]. This condition usually leads to a large value for $C_1$, rendering it difficult and/or expensive to integrate [7]. Another design challenge is to maintain the pole and zero defined by (5) in suitable locations, despite inevitable PVT variations.

The solution proposed here is to replace the $R_2$-series-$C_1$ ensemble with the impedance realized by the capacitance multiplier shown in Fig. 2, as illustrated by Fig. 5 (b). Thus, capacitor $C_1$ and resistor $R_2$ in Fig. 5 (a) are emulated by $C_{eq}$ and $R_s$ from Fig. 2 (b). The parallel resistor shown in Fig. 2 (b), $R_p$, appears as an unwanted component. Its value should be made far larger than the output resistance of the main transconductor, $Gm_{COMP}$, in order to render immaterial
its impact on the operation of the frequency compensating network. This can be achieved by using the circuit implementation proposed in Fig. 4 for the active part of the capacitor multiplier, the transconductor $G_{\text{m\_MULT}}$.

Let us analyze the impact of the following sizing conditions:

$$C_1 = C_{\text{eq}} = C_{\text{placed}} \cdot M$$

(6)

$$R_2 = R_S = \frac{1}{G_{\text{m\_CORE}} \cdot M}$$

(7)

By substituting (6) and (7) into (5) the gain, pole and zero that define the transfer function of the compensation network proposed in Fig. 5 (b) result as follows:

$$H_{PB} = \frac{R_b}{R_1 + R_b} \cdot \frac{G_{\text{m\_COMP}}}{G_{\text{m\_CORE}}} \frac{1}{M + \frac{C_1}{C_{\text{placed}}}}$$

$$f_p = \frac{G_{\text{m\_CORE}} \cdot (M + \frac{C_1}{C_{\text{placed}}})}{2\pi C_3}$$

$$f_z = \frac{G_{\text{m\_CORE}}}{2\pi C_{\text{placed}}}$$

(8)

where $G_{\text{m\_COMP}}$ is the transconductance of the main transconductor within the compensation network and $G_{\text{m\_CORE}}$ is the core transconductance within the $G_{\text{m\_MULT}}$, as shown in Fig. 2 (a).

Equation (8) indicates several advantages of this approach:

- the total capacitance required by the feedback compensation network is reduced substantially.
- the gain $H_{PB}$ depends on ratios of same-type integrated resistors and capacitors, the multiplication ratio, $M$, and the ratio between transconductances $G_{\text{m\_COMP}}$ and $G_{\text{m\_CORE}}$. Therefore, the impact of PVT variation on $H_{PB}$ can be minimized by using a circuit implementation for the main transconductor similar to the one used for $G_{\text{m\_MULT}}$, that is, the circuit presented in Fig. 4.
- one can control the value of the gain $H_{PB}$ and the location of the pole $f_p$ by adjusting the multiplication factor. This can be achieved by simply making programmable the gain of the current mirrors denoted “A” and “C” in Fig. 4.
The following design tradeoff should be considered when choosing the nominal value and tuning range for M: on the one hand, a large nominal value and wide range allows for a substantial reduction of die area and for fine tuning; on the other hand, the larger the M the larger the current consumption and the smaller the smaller the value of \( R \).

III. DESIGN EXAMPLE: AUTOMOTIVE BUCK CONVERTER WITH TYPE-II COMPENSATION NETWORK

A. DESIGN REQUIREMENTS AND CIRCUIT IMPLEMENTATION

The proposed compensation network was used to design a current mode DC-DC buck converter considering specific automotive requirements that included load dump, start impulse, spikes and wide ranges for the input (battery) voltage. These conditions allow for a fair and direct comparison between the two compensation networks.

The conventional Gm-RC compensation network was designed by following the standard approach [13]:

- the unity-gain frequency of the converter loop gain was set to one tenth of the switching frequency, that is, \( f_{0dB} = 50 \text{ kHz} \);
- the zero was placed to one fifth of the unity-gain frequency, that is \( f_z = 10 \text{ kHz} \);
- the pole was placed at half the switching frequency, that is \( f_p = 250 \text{ kHz} \).

The values of passive components within the compensation network were obtained by solving (5) for the values above. The resistors that implement the feedback voltage divider, \( R_1 \) and \( R_b \), were sized so that \( V_{ref} = 5 \text{ V} \) when the reference voltage has the typical value \( V_{ref} = 1.2 \text{ V} \). Table 2 lists the values of all passive components shown in Fig. 5 (a).

For the proposed compensation network shown in Fig. 5 (b) the sizing started with the multiplication factor M. The nominal value of M was set to 4, a value for which the circuit implementation shown in Fig. 4 can provide the wanted frequency characteristics up to a frequency at least one decade above the switching frequency. Furthermore, the gain for the output of the current mirrors A and C, denoted K in Fig. 4, was made programmable. Thus, the value of M can be changed between 3, 4 and 5 by using digital controls. This allows the user to fine-tune the converter frequency characteristics as explained in the previous section and [9].

The feedback resistors \( R_1 \) and \( R_b \) were set to the same values as listed in Table 2 for the conventional Gm-RC compensation network. The other circuit elements shown in Table 5 (b) were sized by solving the set of simultaneous equations (8) for the values obtained for the conventional compensation network.

By design, \( C_{placed} \) is M times smaller than the \( C_1 \). Table 3 lists the resulting values for all circuit elements.

Note that the core transconductor within the capacitance multiplier, \( Gm_{CORE} \), needs to provide a transconductance about 150 times smaller than \( Gm_{COMP} \). This makes it easier to realize the large value for the output resistance required by (2). Also, the capacitance multiplier only needs a fraction of the current required by the \( Gm_{COMP} \) transconductor: overall, \( Gm_{MULT} \) required 20 \( \mu \text{A} \), while \( Gm_{COMP} \) needed 100 \( \mu \text{A} \). Most importantly, the power consumption of both networks had no practical impact on the buck converter efficiency. The total capacitance used by the proposed network is significantly smaller than the one used by the conventional Gm-RC compensation network: 78 \text{ pF} \) against 216 \text{ pF}.

Fig. 6 presents the layout of the compensation network proposed in Fig. 5 (b), with the circuit implementation of the transconductors there shown in Fig. 4.
The conventional Gm-RC compensation network, shown in Fig. 5 (a), requires an area about 3.5 times larger; although it does not need the cell GmMULT, it requires a capacitor four times larger than the Cplaced in Fig. 6, plus a 76.5 kΩ resistor.

The active circuit shown in Fig. 5 (b), used here to emulate the R2-C1 ensemble, comprises a feedback loop closed between Out2 and the inverting input of GmMULT. Its stability needs to be ensured for all operating conditions.

Fig. 7 presents the module and phase frequency characteristics of that loop gain. They were obtained by running simulations of an extracted-RC netlist, considering the entire range of process, supply voltage and temperature (PVT) variations. These results indicate that the loop remains stable over all operating conditions, with the phase margin close to 90 degrees.

Fig. 8 illustrates the impact increasing the multiplication factor M has on the frequency characteristic of the output resistance Rout1. In line with the circuit analysis performed in the previous section, the low-frequency value of Rout1 is remarkably large but it decreases as M increases. However, its value remains relatively large over the frequency range of interested for the application envisaged here: 39 MΩ at 10 kHz which corresponds to FpB value and 2 MΩ at 1 MHz.

B. PERFORMANCE COMPARISON OF THE CONVENTIONAL AN PROPOSED NETWORKS

Fig. 9 presents the frequency characteristics yielded by schematic-only simulations of the two designed compensation networks described in the previous sub-section. The frequency characteristics yielded by an “ideal” compensation network - that is, the standard Gm-RC network shown in Fig. 5 (a) implemented by using an idealized model for GmCOMP and ideal passive components with the values listed in Table 2 – are also depicted in Fig. 9, as a reference.

One notices that there is no significant difference between the frequency characteristics of the designed networks, the
TABLE 4. Summary of Monte-Carlo simulation results, including process, mismatch, temperature and supply voltage: gain at the phase boost frequency ($H_{PB}$), the phase boost frequency ($F_{PB}$), $F_{pole}$, $F_{zero}$.

| Type of compensation circuit | min | typ | max |
|------------------------------|-----|-----|-----|
| $H_{PB}$, [dB]               | 18.1| 19.7| 21.3|
| $F_{PB}$, [kHz]              | 37  | 48.9| 64  |
| $F_{pole}$, [kHz]            | 35  | 47  | 60.2|
| $F_{zero}$, [kHz]            | 7.5 | 9.85| 13.4|
| $F_{pole}$, [MHz]            | 186 | 247 | 330 |

Let us now present results obtained by running simulations on RC-extracted netlists, that include both parasitic resistances and capacitors extracted from the layout shown in Fig 6. Table 4 summarizes the values yielded by Monte Carlo and PVT simulations for the main parameters of the frequency characteristics of the two integrated Gm-RC compensation networks described in the previous sub-section. Again, the differences between them are insignificant. This demonstrates that the impact the offset and internal poles of the additional transconductor Gm$_{MULT}$, used to implement the capacitance multiplier, have on the frequency characteristic of the proposed compensation network can be made negligible by careful design. Fig 10, presents the frequency characteristics realized by the proposed Gm-Cap.Multiplier with M set to 4, over the entire range of process, mismatch, supply voltage and temperature variations. It highlights an essential feature of the proposed circuit: the frequency characteristic key parameters $H_{PB}$, $F_{PB}$ and $F_{ZERO}$ exhibit remarkably small variations.

Fig. 11 highlights an important advantage the compensation network proposed here has over the conventional Gm-RC approach: the possibility to adjust the circuit by changing M. It presents the frequency characteristics realized by the proposed Gm-Cap.Multiplier when the value of M is set to 3, 4 and 5. The gain at the phase boost frequency, $H_{PB}$, can be adjusted between 16.9 dB and 21.2 dB, while the phase boost frequency is maintained at 50 kHz +/− 10 kHz.

Let us now assess the performance of the entire current mode buck converter when using the two compensation networks considered here, the conventional Gm-RC and the proposed one based on the capacitor multiplier. To keep the focus on the comparison between the compensation networks, all the other functional blocks shown in Fig. 1 were replaced by VerilogA behavioral models. Fig. 12 presents the frequency characteristics for the loop gain of the entire buck converter, implemented by using the compensation network proposed here, for typical process, room temperature and nominal supply voltage. These results demonstrate that the converter phase margin can be set to values between 36.2 degrees and 61.6 degrees by varying M between 3 and 5, while the crossover frequency is kept relatively constant, within the range 52 kHz +/− 10 kHz.
FIGURE 12. The buck converter loop gain and phase characteristic when the multiplying factor M is set to 3 (dashed), 4 (continuous) and 5 (dash-dot).

FIGURE 13. Converter responses to a step-down line transient. Top - V_{In} jumping from 13 V to 6 V in 100 ns; Middle – the error voltage, V_{e}; Bottom – the output voltage of the converters with conventional and proposed networks.

The corresponding plots obtained when the conventional Gm-RC compensation network was used instead are also presented in Fig. 12, with continuous line. They overlap the plots yielded by the buck that uses the of the compensation circuit proposed when its multiplication factor M was set to 4.

Fig. 13 presents the buck converter response to a line voltage step, when V_{In} goes down from 13 V to 6 V in 100 ns. This simulation corresponds to the real-life engine start-up case: the automobile starter motor draws hundreds of amperes of current from the battery, pulling down its voltage level for a short period of time [13]. The plots shown in the middle and bottom of Fig. 13 show the error voltage that appears at the output of the compensation circuit (V_{e}) and the buck converter output voltage (V_{Out}). The plots yielded by the two compensation networks analyzed here practically overlap, the converter responses are nearly identical.

FIGURE 14. Converter responses to a step-up line transient. Top - V_{In} jumping from 13 V to 45 V in 100 ns; Middle – the error voltage, V_{e}; Bottom – the output voltage, V_{Out}, of the converters with conventional and proposed networks.

Fig. 14 presents the converter response to another supply voltage step: V_{In} goes up from 13 V to 45 V in 100 ns. This corresponds to the real-life case whereby the vehicle battery gets disconnected from the alternator while being charged. An unsuppressed load dump could generate voltages as large as 35 V to 45 V [16]. In this case, too, the standard Gm-RC and the new compensation network, based on capacitance multiplier, yield practically identical V_{e} and V_{Out} plots.

The load transient performance of the buck converter implemented with the two compensation networks was assessed by considering two cases: i). the load current stepping up, from 100 mA to 300 mA, in 100 ns – see Fig. 15 – and ii). the load current stepping down, from 100 mA to 10 mA, in 100 ns – see Fig. 16. For both test cases, there are no significant differences between the converter responses to these load jumps when using different compensation networks.

FIGURE 15. Converter responses to a step-up load transient. Top - I_{Load} jumping from 100 mA to 300 mA in 100 ns; Middle – the error voltage, V_{e}; Bottom – the output voltage of the converters with conventional and proposed networks.
Simulation results presented in Fig. 12 to Fig. 16 were obtained by using the industry-standard Cadence Virtuoso design environment. They demonstrate that replacing the standard Gm-RC compensation network with the new one described in Section II does not have a negative impact on the converter performance.

The first column in Table 5 lists the main parameters of the buck converter implemented with the compensation network based on capacitance multiplier, obtained for typical process and nominal operation conditions. As predicted by the results listed in Table 4, PVT variations do not have a major impact on the converter parameters, which remain within the limits set by the design requirements listed in Table 1.

However, several converter parameters are significantly impacted by the actual values of external components deviating from their nominal values. This is highlighted by the parameter values listed in the second column in Table 5: they were obtained for the buck converter that used the Gm-Cap. Multiplier compensation with nominal value set to $M = 4$ when the actual values of both $L_{Out}$ and $C_{Out}$ were set at 20% over their nominal values. Similar results are obtained if the compensation network based on capacitance multiplier is used, but in this case the buck parameters can be brought back close to the values obtained in nominal conditions – listed in the first column of Table 5 – by simply setting the multiplication factor $M = 3$ instead of its nominal value, $M = 4$.

### C. COMPARISON AGAINST CONVERTERS PUBLISHED PREVIOUSLY

Table 6 summarizes the performance of the two converters presented in this work – the one which uses the conventional Gm-RC Type-II compensation network and the other that uses the newly proposed capacitor multiplier-based frequency compensation network. To allow for a direct comparison, Table 6 also presents the performance of several previously reported converters that used capacitance multipliers.

Most features and parameters of the converters listed in Table 6 are similar, except for three important points:

i). The two converters presented here can handle a wide input voltage range: 6 V to 45 V, compared to 1.4 V to 4.2 V for the nearest competitor. The wide input voltage range required by automotive applications led to larger values for the external inductor and a longer settling time.

ii). We use a smaller multiplication factor: $M$ takes value between 3 and 5. As explained in Section III, a larger value for $M$ makes it more difficult to ensure the required large output resistance and wide operating frequency range for the cell $G_{MULT}$ shown in Fig. 4. Moreover, simulation results shown in and Fig. 12, and listed in Tables 6 indicate that a wider range for $M$ is not necessary.

iii). Only the newly proposed compensation network based on capacitance multiplier allows for the multiplication factor to be programmed digitally. The usefulness of this feature was demonstrated by the simulation results shown in Fig. 11, Fig. 12 and listed in Table 5.

An important feature for assessing the performance of circuits based on capacitor multipliers is the die area reduction, estimated by comparison with the area necessary for a conventional implementation, based on placed capacitors. Note that a larger multiplication factor does not necessarily equates to a larger area reduction. For example, in [7] the 76 pF capacitor within an R-C compensation network is emulated by a basic capacitance multiplier with $M = 19$ and a placed capacitor of 4 pF. Thus, the die area occupied by the 72 pF placed capacitor was saved (the area occupied by the

| Parameter | Gm-Cap$_{Mult.}$ M=4 | Gm-Cap$_{Mult.}$ M=4 | Gm-Cap$_{Mult.}$ M=3 |
|-----------|----------------------|----------------------|----------------------|
| $L_{Out}$, $C_{Out}$ | nominal | nominal +20% | nominal +20% |
| Load transient Undershoot when $I_{Out}$ ramps down from 300 mA to 100 mA in 100 ns | 78 mV | 85 mV | 80 mV |
| Load transient Overshoot when $I_{Out}$ ramps up from 100 mA to 300 mA in 100 ns | 98 mV | 131 mV | 117 mV |
| Line transient Undershoot when $V_{IN}$ ramps down from 13 V to 6V in 100 ns | 16 mV | 17.5 mV | 15 mV |
| Line transient Overshoot when $V_{IN}$ ramps up from 6 V to 13 V in 100 ns | 14.5 mV | 17 mV | 15 mV |
| MAX $V_{OUT}$ ripple at $V_{IN}=45$ V | 2.2 mV | 2.3 mV | 2.3 mV |
| Phase Margin at $I_{Out}$=100 mA and $V_{IN}$=13V | 51.7 deg | 42 deg | 50 deg |
| $F_{OS}$ Frequency at $I_{Out}$=100 mA and $V_{IN}$=13 V | 50.9 kHz | 42 kHz | 51 kHz |
active circuit is negligible by comparison with the passive devices). Under the same conditions, the circuit proposed here yields a die area reduction at least twice as large, despite its smaller multiplication factor. For \( M = 4 \), the proposed circuit emulates an entire RC network, with \( R = 10.9 \) k\( \Omega \) and \( C = 208 \) pF, by using a 52 pF placed capacitor.

**IV. CONCLUSION**

A new solution for integrating a Type-II compensation circuit for DC-DC buck converters was presented in this paper. The main idea is to emulate the R-series-C ensemble within the standard Gm-RC compensation network by using a novel capacitor multiplier tailored for this task.

The proposed topology for the Gm-Cap.Multiplier frequency compensation circuit was described in some detail, including the key sizing equations. It has two important advantages over the conventional Gm-RC circuit: i) it uses a significantly smaller die area, as it requires a placed capacitor \( M \) times smaller than the one required by the Gm-RC circuit, where \( M \) is the capacitance multiplication factor, and no placed resistor and ii) it provides a simple yet effective solution for frequency tuning, by adjusting the value of \( M \).

A transistor-level implementation of the Gm-Cap. Multiplier circuit was presented. An improved version of a current mirror with large output impedance was developed for this circuit.

In order to prove the effectiveness of the Gm-Cap. Multiplier approach, its performance was compared against the conventional Gm-RC frequency compensation circuit in a real-life design example: a buck converter for automotive applications. The converter had to operate over a wide range of supply voltages, from 6 V to 45 V, with the switching frequency set to 500 kHz. It had to maintain the output voltage \( V_{\text{out}} = 5 \) V with an output voltage ripple no larger than 50 mV and provide a maximum output current of 300 mA. Two versions of the buck converter were designed in a 180 nm standard CMOS process: one used the standard Gm-RC frequency compensation network while the other used the proposed Gm-Cap.Multiplier approach.

Simulation results presented in the paper demonstrated that the converters implemented with the two compensation networks have practically same performances and almost identical frequency and transient responses. The Gm-Cap. Multiplier circuit consumes only 20 \( \mu \)A more than the standard Gm-RC circuit but requires a total placed capacitance \( (C_1 + C_2) \) of only 78 pF, instead of the 216 pF required by its counterpart. Furthermore, it provides an effective way to implement tuning of the converter open-loop frequency characteristics, by making the multiplication factor digitally programmable. This allows the users to reduce the impact factors such as PVT variations inherent to an integrated implementation, and deviations of the actual values of external components from their nominal values, may have on the converter performance.

**REFERENCES**

[1] L.-F. Shi and L.-Y. Xu, “Frequency compensation circuit for adaptive on-time control buck regulator,” *IET Power Electron.*, vol. 7, no. 7, pp. 1805–1809, Jul. 2014.

[2] A. Ghosh and S. Bhattacharyya, “Design and implementation of type-II compensator in DC–DC switch-mode step-up power supply,” in *Proc. 3rd Int. Conf. Comput., Commun., Control Inf. Technol. (CIT)*, Feb. 2015, pp. 1–5.

[3] Q.-Q. Li, X.-Q. Lai, Q. Ye, and B. Yuan, “Fixed-frequency adaptive on-time buck converter with ramp compensation,” *IET Power Electron.*, vol. 9, no. 9, pp. 1801–1807, Jul. 2016.

[4] C. Nan, R. Ayyanar, and Y. Xi, “A 2.2-MHz active-clamp buck converter for automotive applications,” *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 460–472, Jan. 2018.

[5] V.-H. Nguyen, Y. Mo, W. Song, S. Ji, W.-Y. Jung, and H. Song, “A dual-mode 1.8 V-output DC–DC buck converter with on-chip capacitor multiplier in 0.18 \( \mu \)m CMOS,” in *Proc. Int. Conf. Syst. Sci. Eng. (ICSSSE)*, Jul. 2017, pp. 753–756.

[6] K.-H. Chen, C.-J. Chang, and T.-H. Liu, “Bidirectional current-mode capacitor multipliers for on-chip compensation,” *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 180–188, Jan. 2008.

[7] M. Zhou, Z. Sun, Z. Xiao, Q. Low, and L. Siek, “A fast transient response DC–DC converter with an active compensation capacitor module,” in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2018, pp. 1–5.

[8] P. Coste, P. Martari, M. Neag, and V. Ionescu, “Capacitor multiplier with one transconductor cell,” in *Proc. Int. Semiconductor Conf. (CAS)*, Oct. 2019, pp. 195–198.

[9] P. Coste, P. Martari, M. Neag, M. Topa, and V. Ionescu, “Programmable capacitor multiplier based on Gm-cell with two outputs—Topology, circuit implementations and applications,” *Romanian J. Inf. Sci. Technol.*, vol. 24, no. 1, pp. 2–24, 2021.

[10] B. Aggarwal, M. Gupta, and A. K. Gupta, “A comparative study of various current mirror configurations: Topologies and characteristics,” *Microelectron. J.*, vol. 53, pp. 134–155, Jul. 2016.
[11] B. Chunfeng, S. Xingyue, Q. Donghai, and Z. Heming, “A compact low voltage CMOS current mirror with high output resistance,” in Proc. Int. Conf. IC Design Technol. (ICICDT), Jun. 2019, pp. 2–4.

[12] S. W. Lee, “Demystifying type II and type III compensators using op-amp and OTA for DC/DC converters,” Texas Instrum., Dallas, TX, USA, Appl. Note SLVA662, Jul. 2014, p. 15.

[13] R. Ridley, Power Supply Design: Control, vol. 1. Camarillo, CA, USA: Ridley Designs, 2012.

[14] Road Vehicles—Environmental Conditions and Testing for Electrical and Electronic Equipment—Part 2: Electrical Loads, Standard ISO 16750-2, 2012.

[15] Electric and Electronic Components in Motor Vehicles Up to 3.5 t. General Requirements, Test Conditions and Tests, Standard Volkswagen-VW-80000, 2013.

[16] B. Wu and Z. Ye, “Comprehensive power supply system designs for harsh automotive environments consume minimal space, preserve battery charge, feature low EMI,” Analog Dialogue, vol. 53, no. 3, pp. 2–6, 2019.

PAUL COSTE received the B.S. and M.S. degrees in electrical engineering from the Technical University of Cluj-Napoca, Romania, in 2015 and 2017, respectively, where he is currently pursuing the Ph.D. degree in power management and analog front-ends ICs. His research interests include analog and mixed-signal IC design with focus on control circuitry for switched-mode power supplies, linear voltage regulators, low-noise amplifiers, and controlled-gain amplifiers. He is a member of the “Digitally Enhanced RF and Analog IC” Research Group.

ISTVÁN KOVÁCS received the M.Sc. and Ph.D. degrees in integrated circuits from the Technical University of Cluj-Napoca, Romania, in 2011 and 2015, respectively. Since then, he has continued his involvement with this university, both as an Associate Teaching Staff and a Researcher with the Digitally Enhanced RF and Analog IC Design Research Group. He has coauthored over 19 scientific papers and one international patent. He has acquired extensive industrial experience by regularly consulting for industry. His research interests include frequency synthesis, power management integrated circuits, and analog front-ends for sensors and actuators.

MARIUS NEAG (Member, IEEE) received the M.Eng. degree in applied electronics from the Technical University of Cluj-Napoca (TUCN), Romania, in 1991, and the Ph.D. degree from the University of Limerick, Ireland, in 1999. After several years working as a Senior Designer of RF, analog, and mixed-signal ICs in Ireland, the U.K., and the USA, he returned to the academia. Since 2008, he has been at Associate Professor with TUCN, where he co-founded the “Digitally Enhanced RF and Analog IC” Research Group. He has coauthored over 100 scientific papers and three books on analog IC design, as well as three international patents.

ALINA-TEODORA GRĂDEANU received the B.S. and M.S. degrees in electrical engineering from the Technical University of Cluj-Napoca, Romania, in 2011 and 2015, respectively. She is currently pursuing the Ph.D. degree in power management ICs. Her research interests include analog and mixed-signal IC design with focus on voltage regulators and switched mode DC–DC converters. She is a member of the “Digitally Enhanced RF and Analog IC” Research Group.

VLAD-ALEXANDRU IONESCU was born in Bucharest, Romania, in 1986. He received the B.E. and M.E. degrees in electrical engineering from the Politehnica University of Bucharest, Romania, in 2009 and 2011, respectively. Since 2009, he has been working with Infineon Technologies Romania. His current research interests include automotive electronics, power management solutions, functional safety, linear voltage regulators, and circuit design optimization using machine learning methods.

MARINA DANA ŢOPA (Member, IEEE) received the M.S. and Ph.D. degrees in electrical engineering from the Technical University of Cluj-Napoca, Romania, in 1981 and 1998, respectively. Since 1983, she has been with the Department of Basis of Electronics, Technical University of Cluj-Napoca. She is currently a Professor and lectures on signals and systems theory. She has published over 190 papers in journals and conference proceedings, and has contributed to 14 books. Her research interests include analysis and design of electronic circuits; digital signal processing, mainly audio signals; and room acoustics.

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