FPIRM: Floating-point Processing in Racetrack Memories

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Abstract—Convolutional neural networks (CNN) have become a ubiquitous algorithm with growing applications in mobile and edge settings. We describe a compute-in-memory (CIM) technique called FPIRM using Racetrack Memory (RM) to accelerate CNNs for edge systems. Using transverse read, a technique that can determine the number of ‘1’s multiple adjacent domains, FPIRM can efficiently implement multi-operand bulk-bitwise and addition computations, and two-operand multiplication. We discuss how FPIRM can implement both variable precision integer and floating point arithmetic. This allows both CNN inference and on-device training without expensive data movement to the cloud. Based on these functions we demonstrate implementation of several CNNs with back propagation using RM CIM and compare these to state-of-the-art implementations of CIM inference and training in Field-Programmable Gate Arrays. During training FPIRM improves by 2× the efficiency, by reducing the energy consumption by at least 27% and increasing the throughput by at least 18% against FPGA.

I. INTRODUCTION

EDGE computing has become increasingly attractive for accelerating machine learning algorithms, such as convolutional neural networks (CNNs), to support needs of mobile applications. However, edge systems must adhere to constraints often referred to as SWaP (Size, Weight, and Power). For CNN acceleration, Field Programmable Gate Arrays (FPGA) are studied as best possible acceleration engines for low latency small batch inference acceleration while meeting energy requirements of these edge systems.

Spintronic Racetrack Memory [1] (RM) is attractive for Compute in Memory (CIM) as it has the necessary density, i.e., between 1-4F² per cell, while not suffering from endurance concerns of other tiered memory candidates such as phase-change and resistive memories. It also has a low energy consumption of circa 0.1pJ [2] per write and a low access latency of circa 1ns generating excitement for use as main memory [3], [4], particularly for SWaP constrained (e.g., edge) systems.

We present Floating-point Processing in Racetrack Memories (FPIRM). Core to FPIRM are CIM implementations of multi-operand bulk-bitwise operations and addition operations as well as two-operand multiplication operations. We demonstrate floating-point multiplication and addition with FPIRM that enables on-device training using back propagation.

With FPIRM CIM acceleration of deep learning we achieve as much as 5× higher performance than state of the art DRAM CIM which leverages ternary (bulk-bitwise and summation) weight calculations [5], [6] with a nearly 50% reduction in power. FPIRM is 2.8× faster and more than 3× more energy efficient for integer precision (multiplication and addition) than the state-of-the-art RM CIM. We also achieve 18–74% performance improvement and 26–81% reduction in power compared to a low-energy FPGA for 32-bit floating-point precision online training targeting small to moderate CNNs. In particular, FPIRM makes the following contributions:

• FPIRM is, to our knowledge, the first RM CIM approach to implement floating-point addition and multiplication.
• We propose floating-point CIM designed to conduct multi-operand floating-point addition.
• We show that FPIRM outperforms and provides better efficiency for both CIM (inference) and FPGA (training) targeting edge systems.

The remainder of this paper is organized as follows: First, we provide the necessary background on CNNs and RM. Next, we describe the basic concepts of FPIRM, starting with its architecture and how to perform integer operations. We then explain how to perform floating-point multiplication followed by a step-by-step explanation on how to perform FP multi-operand addition. Then, our experimental results compare the improvements of FPIRM with state of the art FPGA architecture, for three ML training benchmarks. Finally, we reach conclusions.

II. BACKGROUND

In this section, we first introduce the elements that compose the CNN inference, then we introduce the additional operations required for training and the difference between these algorithms. In a second time, we introduce the fundamental of RM, and its advantages as a CIM for CNN.

A. Convolutional Neural Network

CNNs are primarily based on the convolution operation, which is a windowed point-wise multiplication accumulation of multiple channels of input features with a set of weights to generate output features. As an example, for the input features \( I \) and weights \( K \) of size \( N \times R_{in} \times C_{in} \) and \( M \times N \times 3 \times 3 \), respectively, the convolution operation for the window at \( m \) (output channel index), \( r \) (row), \( c \) (column) is:

\[
\text{Conv}(I, K)(m, r, c) = \sum_{n=0}^{N-1} \sum_{j=0}^{3} \sum_{t=0}^{3} K_{m,n,j,t} \times I_{n,r+j,c+t}
\]

where \( M \) is the number of output channels, \( N \) is the number of
input channels, \( R_{in} \times C_{in} \) is the size of an input feature map. The inference operation requires convolution steps broken up with activation layers composed of pooling layers to reduce dimensionality of input matrices through average or maximum value operations and ReLU function, a linear function that will output the input if positive and zero otherwise. Once these convolution layers are completed, fully-connected layers are used to provide the classification result. The fully-connected layers can be mathematically written as \( \text{ReLU}(Wx + b) \).

Training of the CNN includes forward-propagation, loss back-propagation, and weight update. During the forward-propagation, which is same as in inference, the values at each activation layer are stored for the weight update. The loss is calculated by a loss function such as Cross-entropy loss [7]. After calculating the loss of the last layer, the loss is propagated layer by layer until reaching the first layer of CNN model, by a process that includes weight rotation, convolution, and channel-wise accumulation. Based on the loss back propagation, the weights are updated in each layer individually based on the weight, activation, and the loss of the activation is determined, typically using gradient descent. The operations in weight updates are depth-wise convolution, element-wise multiplication, and element-wise subtraction.

While deep learning with CNNs presumes calculations with floating-point values, CNN inference calculations can often be reduced to integer computation with as few as 8-bits achieving reasonable accuracy. Recent DRAM CIM work has shown that in many cases this can be further reduced to ternary \( w \in \{-1, 0, 1\} \) [5] or even binary \( w \in \{0, 1\} \) computations [8] operations to replace the multiplications. However, online training for all but the simplest CNNs still requires full 32-bit floating-point computations to work properly. Without this accuracy, the weight updates can be ineffective and possibly even detrimental.

In the next section we describe basic of Racetrack memory that serves as the foundation for FPIRM CIM to accelerate these CNN functions.

B. Racetrack Memory Fundamentals

Spintronic RM is made of ferromagnetic nanowires consisting of many magnetic domains separated by domain walls (DWs) as shown in Fig. 1. Each domain has its own magnetization direction such that binary values are represented by the magnetization direction of each domain, either parallel/antiparallel to a fixed reference. For a planar nanowire, several domains share one/few access point(s) (APs) for read and write operations [9]. DW motion is controlled by applying a short current pulse laterally along the nanowire governed by SL. Random access requires shifting the target domain to align it with an AP (dark blue) and apply a current to read or write the target bit. To avoid data loss when shifting, the blue domains store actual data while the grey domains are overhead domains to prevent data loss. Shift-based writing (Read/Write Port) [10] allows slower current writes to be replaced with orthogonal shifts from fixed magnetic alignment domains to reduce latency and energy.

RM, like many other novel memories including resistive memory CIM crossbars [11], has also received significant attention for CIM, particularly for deep learning [2], [12], [13]. In the next section we describe our FPIRM technique to build CIM approach with RM that can operate at multiple levels of previsions from binary/ternary weight inference to full floating-point precision required for CNN training.

III. FPIRM

The memory architecture concept behind FPIRM is shown in Fig. 2. We follow a DRAM-inspired hierarchical organization consisting of ranks and banks constructed from subarrays built with tiles (Fig. 2a). Each tile is constructed from bundles of RM nanowires shifted together and referred to as a domain-block cluster (DBC) [14], [4]. A DBC can accommodate \( D \) rows with parallel access of all bits belonging to the same row through the parallel APs (Fig. 2b). \( D \in \{16, 32, 64\} \) is the number of data domains per nanowire. Each tile maintains a 512 × 512 shape, akin to DRAM.

To enable CIM processing, a tile may be extended in two ways. A second AP is added to the DBCs in that tile to allow a current to traverse all the domains between the two APs indicated by the orange arrow (Fig. 2b). If spaced within a prescribed transverse read distance (TRD), Transverse Read (TR) can distinguish between resistance levels based on the number of ‘1’s between the APs much like a multi-level cell [15]. Using TR, the local rowbuffer is extended with a CIM Unit that retains a fast (bypass) path for a standard read, but can also convert the one counts from a TR into multi-operand logic and arithmetic based on the TRD (shown for TRD = 7 in Fig. 2c).

Multi-operand AND and OR are naturally determined by sensing the highest (all ones) or lowest (all zeros) resistance levels. Operations of fewer operands can be accomplished by padding with ones or zeros as appropriate. Unlike prior processing using memory approaches FPIRM includes logic to directly compute XOR from the 1’s count which is also the sum \( S \) for addition. All of these bulk-bitwise operations may be computed in parallel across the entire memory row. We also can compute a carry \( C \) and super carry \( C' \) with minimal additional logic. Addition of TRD = 2 operands may be computed directly by activating each nanowire in sequence. For nanowire \( N_i \), \( S_i \) is written to AP \( N_i \) (\( S_i \to N_i \)), while similarly \( C_i \to N_i+1 \) and \( C' \to N_i+2 \) in parallel enabling a carry chain using navy and yellow connections in the CIM.

The CIM block allows logical left and right shifts by both one (orange and blue) and eight (red and green) positions.
These logical shifts are different from RM nanowire shifting which aligns different domains with access points (up and down). The shift by one position along with a small number of predication bits [16] support multiplication using partial product addition. Furthermore, by computing the $S$, $C$, and $C’$ bits in parallel seven operands can be reduced to three, allowing multiplication and reduction over addition to be computed in $O(n)$ time where $n$ is the operand width [13].

The process to compute integer (or fixed-point) computation using FPIRM is shown in Algorithm 1. Addition of TRD − 1 operands may be computed directly activating each nanowire in sequence. For nanowire $N_i$, $i$ represents the nanowire that corresponds to a particular bit position of data in a memory row (see Fig. 2b). $S_i$, computed using the TR of $N_i$ and the CIM Unit (Fig. 2c) is written to AP0 of $N_i$ ($S_i \rightarrow N_i.0$) where $N_i,j$ refers to $N_i$ at AP $j$. Similarly $C_i \rightarrow N_{i+1},1$ and $C_i’ \rightarrow N_{i+2},0$.

The $ADD(O[1..5], w)$ operation of Algorithm 1 describes this in more detail. For each nanowire in sequence, starting with the least significant bit, the $S_i$ is computed using the XOR and written to $O[0]$, which corresponds to $N_0,0$. Given we have $ones_i$ from the SAs such that $\sum_{k=0}^{6} O[k] > i \implies ones_i = 1$ otherwise $ones_i = 0$ we can compute the result using multiplexers such that $M_0$ selects $ones_0$ or $ones_2$ based on $ones_1$, $M_1$ selects $ones_4$ or $ones_6$ based on $ones_5$ and $S$ selects $M_0$ or $M_1$ based on $ones_3$. Similarly, $C$ selects $ones_1$ or $ones_3$ based on $ones_5$ and writes the value in $O[6]_{i+1}$, or $N_{i+1,1}$. $C’$ is $ones_3$ which is written to $O[0]_{i+2}$ or $N_{i+2,0}$. By $i = 2$ all values of $O[0..6]_{i+2}$ may contain data. As the most significant bit is reached, values are not written above $N_{w-1}$. Moreover, just as $S,C,C’$ can be written to $N_{i+1}$, and $N_{i+2}$, simultaneously, when $k$ values are packed into a row, we can activate $k$ nanowires such that $\forall \{0..k-1\} N_{i+k,w}$ generates and writes $S,C,C’$ in parallel.

If it is necessary to add more than TRD − 2 numbers, we use $CSA-REDUCTION(O[0..6])$. CSA-REDUCTION is akin to a Carry-Save Adder (CSA) with more than 3 inputs. A CSA adder computes the $S$ and $C_{OUT}$ from three inputs (e.g., $A,B,C_{IN}$) in parallel before doing a traditional add of $S$ and $C_{OUT}$, which requires traversing the carry chain only once. Similarly CSA-REDUCTION computes $\forall i, S_i$ in bulk-bitwise fashion, followed by $C_i \rightarrow N_{i+1}$, concluding with $C_i’ \rightarrow N_{i+2}$. While ADD takes $w$ cycles to sum five operands, CSA-REDUCTION takes a constant time to reduce seven operands to three operands. Only once there are five or fewer remaining operands is ADD called.

We see this use in $MULTIPLY(O_A, O_B, w)$. First, each bit of $O_A$ is used to determine whether a shifted copy of $O_B$ is copied as a partial product of the multiplication. We leverage the connections from $N_i \rightarrow \{N_{i-1},N_{i+1}\}$ in Fig. 2c to accomplish this along with the predication registers [16] shown in Fig. 2a. Operand $O_A$ is logically shifted left while $O_B$ is logically shifted left so that the predication register which causes a shifted copy of $O_B$ to be retained can be pulled from the zeroth bit of the rowbuffer to simplify the logic that selects the predication bit source. In this instance the least significant bit of each packed operand must have a connection to the predication register. After preparing the partial products they are reduced using CSA-REDUCTION until five or fewer values remain. These values are summed using an ADD.

These operands alone form the basis to conduct binary, ternary, and integer/fixed point CNN inference. In the next sections, we describe floating-point multiplication and reduction over addition required for accurate back propagation used for CNN online training.

IV. FLOATING-POINT TWO-OPERANDS MULTIPLICATION

To conduct floating-point multiplication the operands must be separated into their main components of sign, exponent, and mantissa via masking using bulk-bitwise operation. Using a combination of integer arithmetic on the extracted elements we can compute floating-point multiplication. Given the nature of CNN training where point-wise products are reduced over addition, we leave the products separated to support multi-operand summation.

Presuming the 32-bit floating-point standard of a 23-bit mantissa, an 8-bit exponent (biased by $2^8 - 1$), packed into 64-bits to provide space for the multiplication. First the mantissa $M_i$, exponent $E_i$, and sign $S_i$ of each operand $i \in \{A,B\}$ is masked off with an AND operation and stored separately. The implied leading ‘1’ is also restored to each mantissa with an OR operation. Using integer operations we multiply the two 24-bit mantissas allowing expansion to 48-bits. Because $1.0 \leq \{M_A, M_B\} < 2.0$, then $1.0 \leq M = M_A \times M_B < 4.0$. To normalize we use the top bit, which if ‘1’ executes a predicated
normalization right shift enabled by the CIM unit. We then add the exponents $E = E_A + E_B + (-127(+1))$ using multi-operand integer arithmetic, adding negative 127 due to the normalization factor, and adding 1 if normalization was required when generating $M$. Finally, the sign bit $S = S_A \oplus S_B$ to determine the resulting sign of the multiplication.

We follow the flow in Algorithm 2. First the mantissas of both operands are extracted and reconstructed to include the implicit ‘1’ using bulk bitwise operations as shown in lines 6–8. Calling MULTIPLY from Algorithm 1 the product mantissa is calculated. The normalization process checks the 48th bit (line 11) and uses this to populate the predicate register for a predicated shift operation required to normalize mantissas $M \geq 2.0$ (line 13). This requires that the predicate register must be able to select between bit 0 for multiplication or 47 from the row-buffer to populate the predicate register.

To continue we mask off the exponents (lines 14–16). Next the new exponent must be calculated, we sum the two extracted exponents $E_A$, $E_B$ but must subtract (add negative) 127, which is loaded into the memory location indicated by off set, to deal with the exponent normalization factor. If the mantissa was shifted for normalization, we increase the exponent by one through a predicated storage of 0x800000 into an otherwise empty location denoted as one. Executing the ADD function sums the exponents $E_A$, $E_B$, 0x7F800000 (-127), and optionally 0x800000 as a normalization if the mantissa required normalization. With a 5th 0x0 operand, the new exponent is calculated by adding $w = 8$-bits starting at bit $l = 23$ (line 21). Note, if $E_{31}$ is ‘1’ the exponent has gone out of range (overflow) because either $E > 255$ or $E < 0$. In lines 22–25 the sign is similarly extracted and computed using an XOR. Finally in $M$, $E$, $S$ are returned, but the mantissa remains using 47-bits.

We leave $M$, $E$, and $S$, decomposed to facilitate reduction over floating-point addition described in the next section.

V. FLOATING-POINT MULTI-OPERANDS ADDITION

The addition required in the CNN application is a reduction over addition to combine products of pointwise multiplication within a convolution window. Given the sign, mantissa, and exponents of these products are already segregated, the first step is to determine the maximum exponent within the convolution window and then normalize all the remaining exponents and their mantissas to this value. This process is similar to determining the maximum value during pooling. Copies of the values, in this case the exponents, are sequentially tested via TR from most to least significant bit. If the TR≥1, each word with a ‘1’ is re-written shifted left by one position. The other words are overwritten with a zero vector. This is accomplished by reading the value in the shifted position enabled by the CIM unit. A predicated row reset based on the current tested bit of
the current value is used to zero the “eliminated” values. If the TR=0 all values are cycled through and written back in shifted form. The shifting permits the predication value to be referenced from the same location in the rowbuffer. At the end a TR is conducted and the maximum value is read and written shifted back by 8 as permitted by the CIM unit. This process is repeated with all the participants of the summation over reduction to obtain the maximum value.

For mantissa normalization, we subtract the local exponent with the maximum and use the difference to normalize the mantissa via shifting. First the lowest difference bit is read into the predication register and a predicated logical right shift (read and shift using the CIM unit) is issued. The next bit is for a logical shift by two and we continue by powers of two for each subsequent bit. The connection to \( N_{i+8}, N_{i+1} \), are used to accelerate this procedure.

Next the sign bit of each operand is used as a predication value to invert the mantissa and store ‘1’ in the neighboring row for 2’s complement inversion and summed using integer addition. The resulting summation is subsequently normalized to the 23 bits by complementing negative numbers, normalizing the exponent to correct value. This conduct by creating a copy of the mantissa that is logically shifted to find the first instance of ‘1’ which when found triggers adding the appropriate exponent offset and activates logical shifts to the original mantissa.

We conduct floating-point addition following the flow in Algorithm 3. The function begins by searching for the maximum exponent among the operands in groups of TRD=7 seven (lines 6–16) using \textsc{FindMax} from the helper functions in Algorithm 4 as follows: Starting with the most significant bit \( p \) an OR operation (\textit{isAnyOne}) detects any ‘1’s at that position (line 5). If there is at least one ‘1’ then we eliminate values with ‘0’s at that position because they will be smaller by resetting the rowbuffer and writing them back as 0x0. The algorithm does this by reading each exponent in turn from AP\(_i\), inverts the exp with an XOR with 1 (a \textit{IsOne}) then \textsc{ANDS} this with \textit{isAnyOne} (lines 7–8). A predication bit \textit{pred} is extracted from the row buffer at position \( p = 31 \) and controls the rowbuffer reset (line 10). The nanowires are shifted toward AP\(_0\) and the value is written back to AP\(_1\) (lines 11–12, see Fig. 2b) such that after a round of TRD (= 7 shown in the algorithm) each exponent is written back and stored in its correct original position. If there are no ‘1’s in this position, the predicated logic is never true because \textit{isAnyOne} is zero (line 5), so none of the exponents are eliminated (line 10).

Note, each exponent is logically shifted left by one each time, this is to facilitate reading the predicate from bit \( p \) each round. This ensures the predicate is only selected from position 0, 31, and 47. The final result is logically shifted right by eight to put the maximum exponent value in the correct alignment (line 13). The main function uses \textsc{FindMax} in \( \log_{\text{TRD}=7} \) fashion to find the overall maximum exponent now stored in E.

Next all of the mantissas must be normalized to the maximum exponent and after normalization if their sign is negative inverted in twos complement for summation (Algorithm 3, lines 17–22). The first step uses the \textsc{NormMantissa} helper function (Algorithm 4). First the exponent is subtracted from the maximum exponent (lines 17–18), then each bit is inspected to normalize the mantissa. Again the predication bit is extracted from the same position \( p \) as in the \textsc{FindMax} function. If the highest two bits are true, the mantissa is shifted by 128 or 64 places which results in setting it to 0x0 (lines 19–21). For the next three bits (5:3) 4, 2, and 1 predicted shifts by 8 are executed (line 27), followed by 4, 2, and 1 predicted shifts by 1 (line 26). Note, these mantissas are still “normalized” to bit position 47 not 23 from the multiplication in a prior step, so a shift by 32 is still in scope. After normalization, two storage locations for each value are allocated. If the value is positive the first location gets the mantissa and the second get 0x0. Using predication from the sign bit (also bit position 31) the mantissa is inverted and the second location is written 0x1 (Algorithm 3 lines 20–22).

Once normalized and converted to twos complement form, the mantissas can be summed. Similar to multiply, \textsc{CSA-Reduction} is used to reduce operands from 7 \( \rightarrow 3 \) until there are TRD=2 = 5 or fewer which are then summed using \textsc{Add} (lines 23–32). The last step is to again normalize the resulting mantissa and to reassemble the floating point number. Normalization is done using \textsc{NormSum} helper function (Algorithm 4). Since this addition used twos complement logic we extract the sign from most significant bit of the full 64-bit cell. This becomes the predicate to invert and add 0x1 to make
Algorithm 4 Addition Helper Functions

1: //Find the Maximum Among 7 values
2: function FINDMAX(E[0,6],w=8,o=23)
3:     p ← o + w
4:     for i ← 0: o + w − 1 do
5:         isAnyOne ← CR E[0,6] ↑TR ≥ 1
6:         for j ← 0: 6 do
7:             nIsOne ← E[j] XOR 0xFFFFFFFFFFFFFFFF
8:             pred ← isAnyOne AND nIsOne
9:             RB ← E[j] < 1
10:         predp ? RESET RB test at bit p ⇒ RB ← 0
11:     SHIFT rows upward ↑Shift DWM DBC, reindex E
12:     E[6] ← RB
13: return TR E[0,6] >> 8

14: //Normalize a Mantissa based on Exponent Difference
15: function NORMMANTISSA(M, Max, E,w=8,o=23)
16:     p ← o + w
17:     t ← E XOR 0xFF800000 ↑Invert Exponent
18:     S ← ADD(Max, t, 0x800000, 0, w+1, 0)
19:     for i ← 7: 6 do
20:         isOne ← S[i]; S ← S << 1
21:         if iOne ? M ← 0x0
22:     for i ← 5: 0 do
23:         k ← i mod 3
24:         isOne ← S[k]; S ← S << 1
25:     for j ← 0: 2k do
26:         if i < 3 then isOne ? M ← M >> 1
27:         else isOne ? M ← M >> 8
28: return M

29: //Normalize Mantissa based on Summation and prepare Sum
30: function NORMSUM(M, E)
31:     //Get sign from MSB and if negative, get 2's Complement
32:     sign ← M
33:     for i ← 0: 3 do ⊕Move the sign to bit 31
34:         sign >> 8
35:     sign31 ? M ← M XOR 0xFFFFFFFFFFFFFFFF
36:     sign31 ? M ← ADD(M, o, 0x1, 0, 0, 0, 0, 0, 0, 0)
37: ⊕Copy mantissa, << to find first '1', norm exp with
38:     ⊕predicate, shift mantissa to bit 23
39:     m ← M; m << 1; seenOne ← 0x0
40:     ⊕If Mantissa is higher than bit 47, increase the exp
41:     ⊕Shift the mantissa right to bit position 47
42:     for i ← 15: 0 do
43:         seenThisOne ← m OR seenOne
44:     seenOneFirst ← seenThisOne XOR seenOne
45:     seenOneFirst32 ? expAdd ← i << 23
46:     seenOne ← seenThisOne
47:     seenOne63 ? M ← M >> 1
48:     m ← m << 1
49:     if Mantissa is lower than bit 47, decrease the exp
50:     for i ← 1: 47 do
51:         seenThisOne ← m OR seenOne
52:     seenOneFirst ← seenThisOne XOR seenOne
53:     seenOneFirst32 ? expAdd ← i << 23
54:     seenOne ← seenThisOne
55:     nSeenOne ← seenOne XOR 0xFFFFFFFFFFFFFFFF
56:     ⊕From 47,23, shift the mantissa right to bit position 23
57:     if i < 23 then
58:         seenOne63 ? M ← M >> 1
59:     ⊕From 22...0, shift the mantissa left to bit position 23
60:     if i > 23 then
61:         nSeenOne63 ? M ← M << 1
62:     m ← m << 1
63:     exp ← ADD(E, expAdd, 0, 0, 0, 0, 8, 23) ⊕Add offset to exp
64:     sum ← m ADD 0x7FFFFFFF ⊕Strip leading '1'
65:     sum ← sum OR exp OR sign ⊕Recombine
66: return sum

The mantissa positive (lines 31–36). We then look for the first ‘1’ in the mantissa in relationship to bit 47.

The first bit position requires two storage locations, one to store whether a ‘1’ has been seen seenOne and a second seenThisOne which looks for a ‘1’ at this bit position. seenThisOne is true if we have seen a ‘1’ previously or if there is a one in this round (line 43. The predicate seenOneFirst comes from XOR which is only true on the first ‘1’ (line 44) and the expAdd value is only set once (line 45). Once seenOne is set, we start shifting M to be aligned with bit 23, which requires right shifts if found before bit 23, shown with predicated shifts on seenOne for bits 62:48 (line 47) and 47:24 (line 58). If seenOne is still not seen by bit 22, we start shifting left governed by the seenOne complement nSeenOne until the ‘1’ is found (line 61). The remainder of the function is to combine the normalization exponent offset expADD with E, strip bit 23 and combine the sign, exponent, and mantissa per the floating point standard (lines 63–66).

Note, these algorithms are designed to show the feasibility of the function. In some cases, optimizations for system performance or code optimizations for expediency may have been excluded to maintain clarity. For example, while shown here, we can complete the decomposition and recombination only at the beginning or ending of the full benchmark when communicating with a host processor. Additionally, while shown for 63-bits, we can use the lower 32 bits from the sign shift first and then work from the m to only pull predicates from position 31 (selecting from three positions, 47, 31, 0).

The control for these algorithms comes from the hosts/memory controller. Control of for, if, while, etc. control constructs are governed by the host as they are deterministic and can be entirely unrolled. Moreover, these can be distributed via single instruction multiple data (SIMD) execution throughout the system (e.g., via different subarrays) for massive parallelism. Only the predicated instructions use data-based control, and these presume the instructions will be executed or a nop in its place to remain in lock step with the SIMD execution. Finally, while shown for 32/64 bits, given the row size is 512, 8 items can be packed per row and computed in parallel.

VI. ADDITIONAL OPERATIONS FOR BACK PROPAGATION

During back propagation weight matrices must be rotated 180 degrees, which is equivalent to swapping the values of these relatively small (3×3 up to 11×11) along vertical and horizontal bisecting line of the matrix. We use FPIRM PIM to mask off the individual values of each row using AND, logically shift to the correct position, and recombine using OR. Additionally, the weight update operation: W′ = W − L_R × ∆W where the new weight W′ is a function of the previous weight W the learning weight L_R and the weight difference ∆W calculated via gradient descent method. We also use floating-point FPIRM CIM to compute this function.

VII. RESULTS

FPIRM enables multiple precision modes from binary weight used for inference to floating-point required for effective training. Thus we compare FPIRM for inference against
TABLE I
FPIRM COMPARED TO ACCELERATORS

| Benchmark | Target | Throughput GFLOPS | Power W | Efficiency GFLOPS/W |
|-----------|--------|-------------------|---------|---------------------|
| Lenet-5   | DRAM [6] | 8330 | 32075 | 0.028 | 1.11×10⁶ |
| Ternary [5] | FPIRM | 3.85× | 0 | 0 |
| FPIRM Improvement | | 5.78× | 1.94× | 12.4× |
| Alexnet | DRAM [5] | 84.8 | 490 | 0.93 | 526 |
| Ternary [5] | FPIRM | 2.76× | 2.33× | 3.32× |
| FPIRM Improvement | | 3.32 | 5.89 | 5.45 |
| Integer | RM [12] | 163 | 90.5 | 4.99 | 18.13 |
| FPIRM Improvement | | 2.81× | 1.18× | 3.35× |

Training Improvement Compared to FPGA

| Benchmark | Target | Throughput GFLOPS | Power W | Efficiency GFLOPS/W |
|-----------|--------|-------------------|---------|---------------------|
| Lenet-10  | FPGA [17] | 86.12 | 101.5 | 36.77 |
| FPIRM Improvement | | 1.18× | 5.16× | 6.08× |
| Alexnet | FPGA [18] | 34.52 | 50.72 | 9.97 |
| FPIRM Improvement | | 1.47× | 1.36× | 2.01× |
| VGG-16   | FPGA [18] | 46.99 | 81.95 | 14.37 |
| FPIRM Improvement | | 1.74× | 1.35× | 2.36× |

state-of-the-art DRAM CIM using ternary weights [5], [6] and RM using integer weights [12] as well as FPIRM for training using floating-point operations against energy-efficient FPGAs suitable for Edge systems: Xilinx ZU19EG (Lenet-10) [17] and ZCU102 (Alexnet and VGG-16) [18]. The energy and latency parameters of accessing RM and TR in FPIRM are provided by [2], [15]. The latency and energy consumption for the CIM unit architecture extensions in Fig. 2 were determined by implementing the design with the Cadence ASIC Flow targeting 45nm technology.

A. CNN Inference

During the CNN inference phase, precision can be tuned based on required accuracy. Reduced precision can provide a lower-latency result in situ, which is particularly valuable for edge networks with small batch sizes. For instance, integer, ternary, or binary weight calculation reduces the complexity of addition and multiplication to simpler integer functional units while providing sufficient accuracy compared to more expensive floating-point computation. In fact, ternary and binary forms convert multiplication to much simpler bulk-bitwise (e.g., XOR) operations.

Using bulk-bitwise ternary weight CNN inference FPIRM is more than 3× faster than state-of-the-art DRAM CIM [5], [6] with an approximately 2× power advantage leading to an order of magnitude efficiency advantage for Alexnet². In fact, ternary weight CNN inference with FPIRM is 2–3× faster than even simpler binary weight CNN inference using DRAM CIM [13]. Using integer operations, FPIRM can outperform by nearly 3× and provides more than 3× the efficiency of the latest RM CIM [12]. The results are detailed in Table I. In the next section, we present FPIRM result on CNN training.

B. CNN Training

As training requires a high accuracy and large datasets, which typically can be most efficiently accelerated with a graphics processing unit (GPU). However, given in situ training for low latency with small batch sizes and to maintain SWaP of edge systems GPUs may not be practical for their relatively high power. Sending these large datasets to the cloud for GPU acceleration is also impractical. Given CIM has yet to demonstrate CNN training with floating-point precision, we compare with FPGAs accelerators, which are emerging for in situ edge CNN training [17], [18]. FPIRM is competitive, even outperforming FPGAs by 18–74% with a significant improvement in power. We demonstrate a more than 2× improvement in efficiency even as the complexity of the CNN increases; FPIRM for Alexnet is 2× more efficient, while VGG-16 is 2.36× more efficient. Thus, not only is FPIRM demonstrating that CNN training is possible using CIM, it may even be more practical than FPGAs. When coupled with the high capacity and low energy consumption of RM-based memory, the capabilities for SWaP constrained edge acceleration of deep learning and beyond are impressive and worthy of further exploration.

VIII. CONCLUSION

FPIRM is the first, to our knowledge, approach to enable full CNN architectures in memory, with multiple precision capabilities suitable for tuning both inference and training operations. While floating-point operations have always been a major roadblock for in memory processing, FPIRM can perform these operations efficiently at a speed and energy consumption improving over FPGA technology. In particular, FPIRM is between 18% and 74% faster in term of throughput, and at least 26% better in term of energy, resulting in an efficiency improvement of more than 2× compared to state-of-art FPGAs for small to moderate sized CNNs. FPIRM is the first CIM architecture that is sufficiently re-configurable to provide capabilities and improvements over state-of-the-art techniques for both in situ CNN inference and training for edge computing.

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