Effect of band to band tunnelling (BTBT) on multi-gate Tunnel field effect transistors (TFETs)-A Review

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Abstract. TFETs (tunnel field effect transistor) are providing solution to affairs associated with conventional MOSFET devices such as short-channel effects (SCEs) and limitation of minimum (60 mV/decade) subthreshold slope (SS). TFET is a p-i-n diode which conducts in reverse bias and behaves like a transistor due to tunnelling mechanism of the charge carriers across the barrier called band-to-band tunnelling (BTBT). TFETs face some critical problems like lower ON-state currents and ambipolar behaviour of conduction currents. The purpose of this review is to study a highly efficient TFET which provides significant improvements in \( I_{ON}/I_{OFF} \) ratio with improved ON state current and ambipolar current suppression to enhance the performance of the device. TFET with multigate structure will be studied by using different dielectric and substrate materials. TFET may be considered as promising candidate over MOSFETs in low-power and high-speed switching circuits.

Keywords- TFET, Ambipolar , BTBT, SS

1. Introduction
For maintaining low power with high performance, device scaling technology transformed micrometre dimension era to nanometer dimension era. CMOS scaling in nanometer regime reached on its physical limits and shows some drawbacks such that short channel effects (SCEs), subthreshold leakage current, restricted subthreshold swing (SS) \([1][2][35]\). Operation of MOSFETs depends on thermionic (temperature-dependent) injection of charge carriers. Dependency of SS on thermal temperature \((kT/q)\) limits it to 60mV/decade \([3]\). The subthreshold swing is defined as value of gate voltage required to enhance one decade output current. Subthreshold swing is an inverse of subthreshold slope. For fast switching SS should be less but due to temperature dependency MOSFETs has not ability to achieve SS less than 60mV/decade. Many research groups helps to bridge gap between the conventional CMOS scaling and new era of nanoelectronics devices by providing different device structure, technology and engineering material schemes. Many modifications were made to improve the performance of MOSFET by engineering device geometry and material. By reviewing physics, design and optimization of Tunnel FET (TFET) can be consider as a promising candidate to replace MOSFETs due to its operation of conduction, which is not temperature dependent.
and also have SS less than MOSFET limit [4]. TFET originated from “Esaki diode” also known by another name “tunnel diode” which operates on the principle of quantum tunnelling and provide fast operating speed [5][6]. Tunnel diode was invented in 1957 and Baba [7] in 1992 proposed a new FET called Tunnel FET or surface tunnel transistor (STT).

TFET is novel device technology with different design and conduction mechanism. Basically it is a reverse bias gated p-i-n structure where intrinsic region is sandwich between oppositely doped source and drain (Fig. 1). TFET’s conduction mechanism is based upon band to band tunnelling (BTBT) which is controlled by gate voltage and reverse biasing of p-i-n structure helps in reducing leakage. Quantum mechanical BTBT allow charge carriers to pass through source channel interface and these tunnelling majority charge constitute current in this device. This carrier transport mechanism provides some interesting characteristics which makes TFET suitable and desirable candidate for low power applications. As TFET shows SS less than the theoretical limit imposed by Fermi-Dirac statistics (60 mV/decade) for MOSFET results in faster switching and also demonstrate low device leakage along with low threshold voltage (Vth). Along with these advantages, there are some possible challenges that deteriorate device performance such as low ON current and ambipolarity conduction. These controversies can be resolved by replacing oxide materials with some high-k dielectric materials and by changing architecture design. High-k dielectrics are more thermally stable than low-k dielectric material and also show low leakage current. HfO2 is a high-k dielectric material which is amorphous in nature and show more thermal stability than SiO2. Replacement of SiO2 (low-k) with HfO2 (High-k) dielectric enhances gate control, which results large output current due to faster carrier generation HfO2 increases the switching of device due to its low energy gap. High-k dielectric materials increase oxide capacitance due to its high permittivity and results in high electric field. High electric field and oxide capacitance helps in increasing electron velocity. Thus an improved drain current with improved early voltage is obtained, as charge carriers move faster from source to drain region on the application of gate voltage [44]. Some methods are shown in Fig.3 which helps in upgrading the device performance.

Figure 1. Tunnel field effect transistor
2. Physics of TFET

Conduction mechanism of TFET is different from MOSFET. Conduction in MOSFET is constituted by thermally injected charge carriers, but Quantum BTBT is responsible for the conduction in TFET. Interband tunnelling can be controlled abruptly by band bending at source-channel interface using gate voltage bias. Operation of TFET can be realised by reverse biasing the p-i-n structure with gate voltage modulation.

According to principle, TFET is a device which is ambipolar in nature and shows p-type behaviour when hole-conduction is dominant and vice-versa. This ambipolarity can be suppressed by widening the drain side tunnel barrier, using heterostructures and by designing device with asymmetry in doping level and doping profile [8][9]. Asymmetry also exhibit low OFF state current [10]. Conduction in TFET depends upon the position of conduction and valance band edges in source and channel regions. During OFF state, valance band in channel region remains at lower level than the conduction band in source region. Inhibited BTBT with reverse bias restricts conduction in this device. Thus unavailability of empty states in channel to source region ensures very low off state current [1][30]. On introduction of negative gate voltage (Fig.2b), energy band starts rising upward and a conductive channel opened with the elevation of valance band in channel region. Now channel valance band is higher than source conduction band, a conductive channel is formed due to carriers tunnelling in empty states in the channel region. Energy distribution of carriers depends on the energy window Δϕ. Thus source allows limited energy distribution in the channel through energy window with high energy part cut off [11]. This helps in obtaining SS below 60 mV/ decade (Fig. 2c).

![Figure 2](image_url)

**Figure 2.** (a) p-type TFET with applied different voltages (b) Energy band profile of p-type TFET where dashed blue lines shows OFF state and red lines shows ON state of device (c) Schematic transfer characteristics ; λ = screening tunnelling length; a.u. = arbitrary units; EF = Fermi energy [1].

Grey portion in Fig. (2b) Indicates triangular potential barrier which can be determined by transmission probability of interband tunnelling barrier (T_wKB).

\[
T_{wKB} \approx \exp \left( -\frac{4\lambda \sqrt{2m^*}(E^B)}{3\hbar(E_g+\Delta\phi)} \right)
\]

(1)

T can be calculated [12] by equation (1), known as Wentzel-Kramer-Brillouin (WKB) approximation. Where, \(\lambda\)=screening tunnelling length, \(m^*\) = effective mass and \(E_g\)= band gap. Screening tunnelling length defines geometrical width of transition region present at source-channel interface. WKB
approximation is defining a single imaginary band connection from VB to CB with “least action for tunnelling”. This works only with direct bandgap materials like InAs nanowires and remains disagree with indirect band gap like Si or Ge due to phonon-assisted tunneling (PAT). Luisier and Klimeck [43] tells about three methods on which transfer characteristics of TFETs depends (i) WKB approximation (ii) a quantum transport solver with direct tunnelling only (iii) with direct and PAT.

3. TFET device structures and parameters

Many multigate TFETs are designed to increase the performance of device. A comparison is made to show the performance of different device structures [42]. Also a comparison table (1) is made to check the credibility of device on the basis of simulation results shown in fig 3.

![Simulation results of TFET with Gate-All-Around, Gate stacked Gate-All-Around Double gate and double gate in the form of I_d-V_g curves](image)

**Figure 3.** Simulation results of TFET with Gate-All-Around, Gate stacked Gate-All-Around Double gate and double gate in the form of I_d-V_g curves [42]

**Table 1.** Calculation of different device parameters for some multigate TFET structures [42]

| Device Parameters | Gate Stacked Gate-All-Around TFET | Gate-All-Around TFET | Double-Gate TFET |
|-------------------|----------------------------------|----------------------|------------------|
| V_{th} (Threshold Voltage) [V] | 1.4 | 1.3 | 1.4 |
| SS_{avg} (Average Sub-threshold Swing) [mV/decade] | 127 | 144 | 142.8 |
| I_{off} (OFF Current) [A/µm] | 10^{18} | 10^{14} | 10^{16} |
| I_{on} (ON Current) [A/µm] | 10^{6} | 10^{6} | 10^{7} |
| I_{on}/I_{off} | 10^{12} | 10^{8} | 10^{9} |
| I_{amb} (Ambipolar Current) [A/µm] | 10^{18} | 10^{14} | 10^{15} |
Heterogeneous junctions show better performance than Homogeneous junctions due to its different interface [17]. This can be achieved with the help of low bandgap materials.

![Image of I-V characteristics](image-url)

**Figure 4.** Simulation results of Mg$_2$Si/Si Heterojunction DG-TFET and Si DG-TFET (a) $I_D-V_G$ curve (b) Point sub-threshold swing [17]

From the above results (Fig 4, 5.), we can say that ON current can be enhanced by making a heterojunction at source/Channel junction with the help of narrow bandgap materials.

![Image of Vth and SS comparison](image-url)

**Figure 5.** A comparison between Si and Mg$_2$Si Source TFETs [17]

Fabrication of bilayer TFET can be broadly divided into three steps (i) formation of local back gate and insulator (ii) InAs is bonded onto the Si die (iii) source/drain contact and top gate are formed by processing InAs processing [45].

Fig.(6) shows a chart in which problems associated with TFET is illustrated and some optimized solutions also proposed to resolve these issues. After reviewing different TFETs structures, problem of low on current and ambipolar behaviour have been observed. It is observed that both the issues are
associated with BTBT at both junctions and can be resolved by using various techniques. Some techniques are provided to solve the observed problems [29][32][36][37][38][39][40][41].

3.1 Problem of Low ON state current

TFET solve problems of low subthreshold swing (SS) limitation. For continuous growth of technology, subthreshold swing is an important aspect and many researchers have worked on it and proposed solutions to lowers down it. In 2004, Zhang [13] proposed a new model of SOI TFET with lower SS = 40 mV/ decade at limiting voltage. But issues associated with these TFETs were low ON state current which impacts ION / IOFF ratio too. Boucart proposed a model [14] in which SiO2 low-k dielectric material was replaced by high k dielectric material for improvement in ION / IOFF ratio. MOSFET and double gate TFET also compared on the basis of different aspects in this work. High-k dielectric materials help in increasing oxide capacitance as well as ON current after reduction of oxide thickness of device. Mg2Si resolves many issues such as global warming and finite energy resources due to its natural abundances and also consider as non-toxic. Lower bandgap makes it potential candidate used for thermoelectric material [16][31]. A heterojunction of Mg2Si/Si as source/channel-based DG-TFET is examined using feasibility of Mg2Si layer on Si [17]. Tread-like band diagram of hetero-junction gate dielectric TFET at source-channel junction increase tunnelling due to low barrier width [18][29][32][33]. Gate-all-around structures of TFET are examined for electrostatic analysis, structural analysis, potential curve and current curve analysis in [19][20][21][22].

![Band to Band Tunnelling (BTBT) related issues and approximated solution](image_url)

**Figure 6.** Band to band tunnelling (BTBT) related issues and approximated solution
3.2 Ambipolar Conduction

Ambipolar behavior of TFET [34] is a huge problem in the enhancement of ON current. In 2007, a model was proposed by Verhulst [23] in which gate is overlapped on drain region of TFET for the reduction of ambipolar conduction in channel-drain region. But it results with a drawback of reduced chip density. Choi [18] proposed a model with hetero-gate dielectric for the enhancement in ON state current with the suppression of ambipolar current of TFET. Source side gate insulator was replaced by high dielectric constant material. Device with this arrangement shows fast switching as well as on-current without reducing chip density [18]. Channel and drain terminal was introduced with intrinsic region which helps in reducing leakage and ambipolarity without effecting the ON state current [24][28]. Ambipolar current reduction was obtained by overlapping gate to drain in TFET [25][27]. Drain has overlapped here. Ambipolar behaviour can be controlled varying length of overlapped channel according to requirement. Overlapped gate-drain TFET structure is shown with transfer characteristics are shown in Fig. (7). In 2015, a review article with comparison is given by Bagga [26] to improve ambipolar behaviour in TFET.

By reviewing the literature two major problems with TFETs has been analysed (i) low ON state current (ii) Ambipolar conduction. To resolve these problems and enhance the ON state current of device high electric field is required at source-channel junction and ambipolarity can be diminished by reducing the electric field at channel-drain junction. Electric field can be enhanced by increasing the source doping, using narrow bandgap materials at source, by reducing oxide and body thickness, by changing work-function and using High-k dielectric materials. Here at drain side electric field can be reduced by reducing the drain doping, increasing oxide thickness, widening bandgap, using low-k dielectric material, altering work-function and by overlapping gate over the drain region. A heterojunction TFET with Gate-All-Around geometry using narrow bandgap materials at source can be an optimistic solution of above problems and may be show enhanced performance.

4. Conclusion

TFET is considering as most promising steep-slope switching device with SS less than 60mV/decade which makes it better candidate over the MOSFETs in terms of very low OFF state current, large $I_{ON}/I_{OFF}$ ratio, independent of geometric scaling and most important in reduced SCEs. TFET shows some issue such that low ON states and ambipolar behaviour which can be resolved by some techniques. In this review, above issues are considered and some possible solutions are provided to
resolve it to enhance the performance of device. As both issues depends upon tunnelling in TFET and can be resolved by controlling BTBT. $I_{ON}$ can be enhanced by increasing electric field at source-channel interface and ambipolar suppression can be achieved by reducing electric field at drain/channel interface. By changing doping, materials, device architectures and device dimensions performance of TFET can be increased.

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