Analysing the capacitance–voltage measurements of vertical wrapped-gated nanowires

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Abstract
The capacitance of arrays of vertical wrapped-gate InAs nanowires is analysed. With the help of a Poisson–Schrödinger solver, information about the doping density can be obtained directly. Further features in the measured capacitance–voltage characteristics can be attributed to the presence of surface states as well as the coexistence of electrons and holes in the wire. For both scenarios, quantitative estimates are provided. It is furthermore shown that the difference between the actual capacitance and the geometrical limit is quite large, and depends strongly on the nanowire material.

1. Introduction

Great efforts are currently being made to develop new schemes for the manufacturing of nanowire (NW) devices [1]. For example, recent progress in vertically processed semiconductor NWs with a cylindrically symmetric gate electrode, such as the wrapped insulator-gate field effect transistor [2], have shown great promise for application in future highly scaled electronic devices. Besides the possibility of incorporating wrapped gates for improved gate control, NWs offer other intriguing possibilities not easily accessible to planar designs, such as an inherent one-dimensionality as well as relaxed constraints in terms of combining highly lattice-mismatched materials along the NW channel due to radial relaxation of interface strain [3, 4].

In order to facilitate the development of high performance NW electronic devices, it is important to accurately characterize the doping profile and interface properties of the system as well as further fundamental material parameters. Si-based metal–oxide–semiconductor (MOS) stacks have long benefited from well developed capacitance–voltage (CV) measurement schemes for device characterization. However, similar methods have so far been largely unavailable for NW devices. Recently, CV characteristics of individual Ge NWs on SiO2/Si substrates were measured [5]. Here we are focusing on vertical wrapped-gate NWs for which we have earlier demonstrated a scalable processing protocol for routine CV spectroscopy [6]. An overview of the device structure considered here is given in figure 1. The device consists of an 11 × 11 array of InAs NWs, covered with a 10 nm conformal HfO2 dielectric layer and a top Cr/Au metallization as one of the capacitor electrodes. The capacitance is measured between this gate electrode and the core of the wire, which is connected via the substrate. Details of the fabrication protocol and measurement techniques can be found elsewhere [6]. In this paper we further develop the quantitative as well as qualitative understanding of these measurements, and also discuss various features of the CV characteristics in detail.

2. The model

The nanowires are modelled as cylinders in which the radius of the InAs will be referred to as R_{nw}, whereas R_{gate} is the radius of the InAs and HfO2 together. Typical values are length h = 680 nm, and radial dimensions R_{nw} = 27 nm, R_{gate} = 37 nm.

We assume that the unintentional doping of the NWs is of n-type. By changing the applied gate voltage, V_{gate}, the charge within the NW, Q, can be affected. This defines the
capacitance:

\[ C = \frac{dQ}{dV_{\text{gate}}}. \tag{1} \]

The total charge \( Q \) is the spatial integral over the charge distribution \( \rho(r) \) containing three components \( \rho = e(N_0 - n_e + n_h) \) inside the InAs nanowire. Here, \( e \) is the positive elementary charge and \( N_0, n_e \) and \( n_h \) are the concentrations of ionized donors, electrons, and holes, respectively. The donors are assumed to be entirely ionized at room temperature, as considered throughout this paper. All concentrations are assumed to depend only on the radial distance \( r \) from the centre of the NW. This greatly facilitates the calculations as it reduces the problem to one dimension. Working with homogeneous doping profiles is motivated by averaging over arrays of long wires. However, microscopic fluctuations are neglected by this approach.

The effective density-of-state masses for electrons and holes in InAs are \( m_e^* = 0.023m_e \) and \( m_h^* = 0.41m_e \), respectively [7, 8]. Non-parabolicity effects are neglected, albeit they can cause some quantitative deviations for large positive biases. For the determination of hole concentrations, we use the bandgap \( E_g = 0.54 \) eV for InAs NWs with wurtzite structure [9]. The relative dielectric constant is \( \varepsilon \approx 15 \) both for the InAs NW and the HfO2 insulator [8, 10, 11].

To calculate the capacitance, a Poisson–Schrödinger solver was implemented similar to the one demonstrated in [12, 13]. For a given charge distribution \( \rho(r) \), the cylindrical geometry permits the use of Gauss’s law to solve Poisson’s equation for the electrostatic potential \( \phi(r) \). Thus, we obtain the Hamiltonian

\[ H = -\frac{\hbar^2}{2m_e^*} \nabla^2 - e\phi(r) \tag{2} \]

together with the boundary condition for the wavefunction \( \Psi(R_{\text{trap}}) = 0 \), assuming that the HfO2 layer constitutes an infinite barrier. Due to the cylindrical symmetry of the problem, Bessel functions were used as a basis set for the diagonalization of equation (2), resulting in the wavefunctions \( \Psi_{\nu j}(r, \varphi) \) and corresponding energies \( E_{\nu j} \). Here \( \nu \) and \( j \) are the angular and radial quantum numbers, respectively. The relatively long length of the wires compared to their radial dimensions justifies the use of a 1D density of states along the \( z \)-direction, \( g(E) \). Using Fermi–Dirac statistics the electron concentration is then given by

\[ n_e(r) = \sum_{\nu j} |\Psi_{\nu j}(r)|^2 \int_0^\infty \frac{g(E_z) dE_z}{\exp((E_z + E_{\nu j})/kT) + 1}. \tag{3} \]

Here the electrochemical potential \( E_{\nu} \) was set to zero in the wire, which is used as a reference point throughout this paper. Together with the similarly calculated hole concentration \( n_h \), this provides a new charge distribution \( \rho(r) \). By iterative solution of the Poisson–Schrödinger equation, a self-consistent solution is obtained.

In figure 2, calculated potentials and electron distributions are shown. Figures 2(a) and (b) correspond to a positive electrical potential at the gate electrode. The corresponding bending of the conduction band edge causes electrons to accumulate close to the semiconductor–oxide interface (accumulation mode). Figures 2(c) and (d) correspond to a negative electrical potential at the gate electrode. Here the electrons are depleted close to the surface of the wire (depletion mode).

In the simulation we assume that the insulating oxide layer is neutral of charge and use the corresponding electric potential \( \phi_0(R_{\text{gate}}) \) at the gate as a parameter. However, trapped charges are likely to occur both at the surface of the wire and within the oxide [14]. If an areal charge density \( \sigma \) is present at position \( R_{\text{trap}} \), the potential for \( r \geq R_{\text{trap}} \) is modified according to

\[ \phi(r) = \phi_0(r) - \frac{\sigma}{\varepsilon \varepsilon_0} \ln \left( \frac{r}{R_{\text{trap}}} \right), \tag{4} \]

while \( \phi(r) \) is not affected for \( r < R_{\text{trap}} \). Experimentally, one measures the applied gate voltage \( V_{\text{gate}} \), which is related to the
actual electric potential at the gate via

$$V_{\text{gate}} = \phi(R_{\text{gate}}) + \frac{W_{\text{Cr}} - \chi_{\text{InAsNW}}}{e}.$$  

(5)

Here $W_{\text{Cr}}$ is the work function of Cr and $\chi_{\text{InAsNW}}$ the electron affinity of the InAs in the nanowire. As long as the trapped charges are unchanged they provide a constant bias offset

$$V_{\text{gate}} = \phi_0(R_{\text{gate}}) + V_0$$  

(6)

between the measured bias and the parameter $\phi_0(R_{\text{gate}})$ used in the simulation. As both the magnitude of the trapped charges and the electron affinity of InAs in the wurtzite modification appearing in the nanowire are not a priori known, we use $V_0$ as a fit parameter in the subsequent data analysis.

3. Understanding the experimental data

In figure 3, the experimentally measured capacitance for the device with mean wire radius $R_{\text{nw}} = 27$ nm is shown together with our calculations for different doping densities. The main trend is the increase of capacitance with bias. This can be attributed to the location of charges inside the NW. From Gauss’s law it follows that the change in $Q$ induced by a change in bias will be larger if $\rho(r)$ is affected at large values of $r$. As can be seen in figure 2(b) (corresponding to the operation point 1 in figure 3), the charges are mainly located close to the NW surface in the accumulation region. In contrast, they are close to the centre of the wire at operation point 2; see figure 2(d). This explains why the capacitance is higher at point 1 than at point 2.

The measurements reported here are performed by adding a small AC signal with a frequency of 20 MHz atop the DC gate bias. The impedance is found to be almost completely imaginary, showing a negligible influence of any series resistance to the accumulation capacitance. For positive bias the measured capacitance shows less than 10% frequency dispersion between 50 kHz and 100 MHz, demonstrating good properties of the MOS structure and that a reliable quantitative data analysis can be performed for $V_{\text{gate}} > 0$. In contrast, for $V_{\text{gate}} < 0$ the frequency dispersion is more pronounced, which we attribute to the presence of surface states; see section 3.3.

The calculations provide a capacitance per wire length, as given in figure 3. For the experimentally measured capacitance $C$, the gate–substrate capacitance, which is independent of bias, see [6], has been subtracted, and the result has been divided by an effective length $L$, which has been taken as a second fit parameter in addition to $V_0$. The data shown assume an effective length corresponding to an effective number of 90 wires with the nominal length of 680 nm. This has to be compared with a total of 121 wires in the fabricated array. The difference can be attributed to the lack of electrical connection of some wires and/or variations from the nominal length.

Each fabricated array showed a certain distribution of radii $R_{\text{nw}}$ [6]. To accommodate for this, an ensemble of three different values of $R_{\text{nw}}$ was used in the simulation for each device, while the oxide thickness of 10 nm was held constant. The calculated curves in figures 3 and 4 are the results from such ensembles with appropriate weights for each radius reflecting the measured radius distribution.

In figure 3 it is indicated that different factors, such as geometry, doping, surface states, and inversion (holes), affect the capacitance at different gate voltages. We will in turn explain the contribution from each factor. Measurements indicate that the down-sweep curve (green curve) is closer to equilibrium as time-dependent sweeps are more stable and the up-sweep (yellow curve) relaxes towards the down-sweep curve. Therefore, all fits of our stationary model are made to the down-sweep curve.

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3 We used $R_{\text{nw}} = 25$ nm: $0.5 \times 25$ nm + $0.3 \times 27.5$ nm + $0.2 \times 22$ nm. $R_{\text{nw}} = 27$ nm: $0.4 \times 26$ nm + $0.45 \times 28.5$ nm + $0.15 \times 24$ nm. $R_{\text{nw}} = 28.5$ nm: $0.4 \times 27.5$ nm + $0.45 \times 31$ nm + $0.15 \times 25$ nm. $R_{\text{nw}} = 30$ nm: $0.4 \times 30$ nm + $0.4 \times 32$ nm + $0.2 \times 27.5$ nm. $R_{\text{nw}} = 31$ nm: $0.35 \times 30$ nm + $0.5 \times 32.5$ nm + $0.15 \times 28$ nm.
and different assumed doping densities.

figure 3, which is most clearly seen for the down-sweep

3.3. Surface states

Table 1. Effective number of wires and bias offset $V_0$ resulting in a best fit of the capacitance–bias characteristics for different arrays of NWs and different assumed doping densities.

| $R_{nw}$ (nm) | No. of wires | $N_D = 10^{18}$ cm$^{-3}$ | $N_D = 2.2 \times 10^{18}$ cm$^{-3}$ | $N_D = 4 \times 10^{18}$ cm$^{-3}$ |
|---------------|--------------|-----------------|-----------------|-----------------|
| 25            | 71           | 0.27            | 0.42            | 0.63            |
| 27            | 90           | 0.26            | 0.39            | 0.60            |
| 28.5          | 86           | 0.13            | 0.32            | 0.53            |
| 30            | 90           | 0.12            | 0.28            | 0.51            |
| 31            | 84           | -0.05           | 0.14            | 0.38            |

3.1. Geometry

According to figure 3 the capacitance is independent of the donor concentration in the accumulation mode, but rather depends on the geometry of the wire. The reason is that during accumulation electrons are added close to the semiconductor–oxide interface; see figure 2(b). Thus different doping concentrations result in the same capacitance. The capacitance in this region can therefore not be used to determine the doping concentration. Fitting to the experimental data instead determines the effective length of the wires.

In figure 4, the capacitance (experimental down-sweep) for NWs with different radii $R_{nw}$ are shown. All fabricated arrays have 121 NWs, and the effective number of wires used for fitting $L$ is displayed in table 1. As a general trend, the capacitance increases with the radius $R_{nw}$ as there is a larger surface area of the NWs. Note that the capacitance in the accumulation region is significantly lower than the geometrical capacitance $C/L = 2\pi \varepsilon \varepsilon_0 / \ln(R_{gate}/R_{nw})$, which is $2.48 \times 10^{-18}$ F nm$^{-1}$ for $R_{nw} = 25$ nm and $R_{gate} = 35$ nm. This deviation is strongly dependent on the density of states for the nanowire material; see section 4.

3.2. Doping

As the bias is lowered, the electrons will be depleted in the NW. A large doping concentration provides a positive background charge with a strong attraction for the electrons, requiring a higher negative gate voltage to deplete all the electrons. Thus, the doping concentration strongly affects the slope of the capacitance curve around $V_{gate} = 0$ V. Comparison between fits and experimental data shows that $N_D = 4 \times 10^{18}$ cm$^{-3}$ is too flat while $N_D = 1 \times 10^{18}$ cm$^{-3}$ is too steep. The doping of $N_D = 2.2 \times 10^{18}$ cm$^{-3}$ fits very well up to the ‘kink’ at point 2 of the experimental down-sweep curve in figure 3. This also holds for all devices shown in figure 4. As all devices were manufactured using the same method, this provides a consistent estimate of $2.2 \times 10^{18}$ cm$^{-3}$ for the doping density.

3.3. Surface states

The experimental curves exhibit a ‘kink’ at point 2 of figure 3, which is most clearly seen for the down-sweep curve. For biases below the kink the measured capacitance is significantly larger than the simulation result. In this section we attribute this to the emptying of surface states, situated at the semiconductor–oxide interface.

The surface states are assumed to be located in the forbidden gap [15], and are treated as donors [16]. As the states are located in the bandgap, they remain filled as long as $E_F$ is in the conduction band. Theoretical evaluation of the potential at $R_{nw}$, for the doping of $N_D = 2.2 \times 10^{18}$ cm$^{-3}$, shows that $E_F$ is 0.1–0.2 eV below the conduction band edge at the kink; see figure 2(c). This makes it feasible that the kink is an effect of such surface states. For gate voltages more negative than the one corresponding to the kink, surface states are emptied, which produces the discrepancy between simulations and experiment.

While conduction band electrons as majority carriers can almost adiabatically follow the AC signal at 20 MHz, the filling and emptying of surface states is a slower process. Therefore these states do not directly contribute to the capacitance under our measurement conditions. For lower AC frequencies, we observe an enhancement of the capacitance in the bias region below the kink which we attribute to the direct contribution of surface states. The situation is, however, intricate due to a strong variation of charging times, and its analysis is a matter of ongoing research. Thus we focus on the high-frequency data at 20 MHz here.

Even if the surface states do not directly contribute to the capacitance signal, they affect the capacitance–voltage characteristics indirectly by the presence of a bias-dependent surface charge. This positive charge screens effectively the gate bias from the NW, so that a more negative $V_{gate}$ is needed to deplete the electrons from the wire. This can be quantified using equations (4) and (5). An additional (bias-dependent) surface charge density $\delta \sigma$ at $R_{nw}$ gives an additional shift of the gate bias $V_{gate} = \phi_0(R_{gate}) + V_0 + \delta V$ with

$$
\delta V = \frac{\delta \sigma}{\varepsilon \varepsilon_0} \ln \left( \frac{R_{gate}}{R_{nw}} \right).
$$

This explains the shift of the capacitance curve to lower bias while emptying the surface states. With $\delta V$ being of the order of $-1$ V, positive surface charge densities of $\sim 10^{13}$ cm$^{-2}$ are observed for gate biases far in the depletion region.

To summarize, if surface states are not included in the model, the simulations should be fitted to the part of the down-sweep curve right of the kink. The difference in $V_{gate}$ between experiment and simulation below the kink allows for an estimate of the surface charge density.

3.4. Holes

As the electrochemical potential in the wire starts to approach the valence band, holes will appear. The creation and
potential enters the valence band. From figure 5, we conclude that holes are already occupied slightly before the electrochemical potential entering the valence band at $r$.

In contrast, due to the thermal distribution, electrons. The high effective mass of the holes implies a large density of states, which results in a strong screening. If holes are created, practically no electrons will be removed any longer from the conduction band. The constant electron concentration causes the capacitance curve to flatten out at a finite value. This can be seen for the simulated doping concentration $D$ (cm$^{-3}$) that at the estimated doping concentration $N_D = 2.2 \times 10^{18}$ cm$^{-3}$, inversion will not affect the capacitance for $R_{nw} \lesssim 30$ nm, in accordance with the findings of figure 4.

4. Comparison between different materials

We will now show that equating the capacitance of an NW with its geometrical limit can lead to large overestimates. In figure 6, the theoretically calculated capacitances of InAs, InSb, GaAs and Si NWs are plotted. The effective masses of these materials are 0.023, 0.0145, 0.063 and 0.33 [14], respectively. (For Si the density-of-state mass per conduction band valley was used and the valley degeneracy was explicitly taken into account.) They are all surrounded by HfO2 and have the same geometry, $R_{nw} = 25$ nm and $R_{gate} = 35$ nm, i.e. they have the same geometrical limit. For comparison, the results from a Poisson–Thomas–Fermi solver have been plotted as well. In the Thomas–Fermi approximation, the electron concentration at each point is determined by the distance between the conduction band edge and $E_F$. Multiplying the Fermi–Dirac distribution with the three-dimensional density of states and integrating over the conduction band yields the electron concentration as

$$n_e(r) = \int_0^\infty \frac{2m^*}{\pi kT} \frac{1}{E^{1/2}} dE \exp(E - e\phi(r))/(kT) + 1$$

where the conduction band edge is given by the electrostatic potential times the electron charge $-e\phi(r)$. Again we use $E_F = 0$ as a reference.

Due to the complex band structure of Si, only the Poisson–Thomas–Fermi results have been calculated for this material. The main difference between the two solvers is that classically the electron concentration does not have to be zero at the semiconductor–oxide interface, resulting in a higher capacitance. It is evident that the two models give the same results for a repulsive gate voltage. In this case the electron concentration approaches zero at $R_{nw}$ as the potential surpasses the electrochemical potential; see also [12].
There is a reason why the geometrical capacitance cannot be reached even classically. Let us compare with a metallic coaxial cable. In this case the geometrical limit is reached as all charge is added at the surface. This requires an infinite density of states, which cannot be found in a semiconductor, and thus the geometrical capacitance will not be reached. Materials with a high effective mass, such as Si, have a large density of states and will therefore come closer to the geometrical limit.

Frequently, it is assumed that the capacitance is constant for large positive gate voltages. Both experimental and theoretical results point out that this is not the case: the capacitance is slowly increasing with bias. As the gate becomes more attractive, electrons will be filled higher up in the conduction band. Since the 3D density of states goes as $E^{3/2}$, the density will increase as the bias is raised, resulting in a larger capacitance.

5. Conclusions

It has been shown how information about the doping and surface state concentrations can be obtained for semiconductor nanowires by comparing experimental and simulated capacitance data. The above procedure suggests how the contribution from these two factors can be separated. Analysis shows that the doping density $N_D = 2.2 \times 10^{18}$ cm$^{-3}$ gives good agreement with the experimental data. The surface state charge at full depletion is estimated to be around $10^{13}$ cm$^{-2}$. Finally, the actual capacitance can be significantly smaller than its geometrical limit even in accumulation mode. The difference is of particular importance for nanowires with low effective mass.

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