Coat Circuits for DC–DC Converters to Improve Voltage Conversion Ratio

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Abstract—The voltage conversion ratio of basic dc/dc converters is limited due to the influence of parasitic elements of circuits and components. In this article, a family of passive circuits termed as “coat circuits” are proposed for conventional dc/dc converters. Not only voltage step-up capacity can be improved but also the voltage stress of components can be decreased by adding coat circuits to basic dc/dc converters. Moreover, no additional active switches are needed in the coat circuits, that means the control and driver circuits of the converters are not changed. The Cuk converter with the coat circuit has been analyzed as an example, and a 200 W experimental prototype has been built to verify the validity of the theoretical analysis.

Index Terms—Basic dc/dc converter, coat circuit, voltage conversion ratio.

I. INTRODUCTION

CONVENTIONAL basic dc/dc converters such as buck, boost, buck–boost, Cuk, single ended primary inductor converter (SEPIC), and Zeta circuits are widely used in various industrial and consumer applications. In ideal conditions, by adjusting the duty cycle of the switch, any voltage conversion ratio can be achieved using these converters. However, in actual working conditions, the boost capacity of these converters is greatly limited by parasitic elements of the circuit and the voltage drop across the switch and diode [1]–[3]. This also makes the application of basic dc/dc converters difficult in situations where a wider input and output voltage range or a larger voltage conversion ratio is required [4]–[7].

To achieve a high-voltage conversion ratio, many solutions such as the use of transformers, coupled inductors, cascade structures, switch-capacitors, voltage multipliers (VMs), or combination of aforementioned techniques have been proposed. However, the use of transformer would increase the overall size and cost of the system in situations where isolation is not required [8], [9]. The leakage inductive energy of the coupled inductor needs to be considered as it not only increases voltage stress across the switching devices but also necessitates the deployment of complex snubber circuits [10]–[12]. When cascaded converters are used several stages are required and that apparently increases the cost and reduces the efficiency of the system. Furthermore, it requires high-voltage components at the output stage [13], [14]. Switched capacitor converters have some fundamental problems such as the requirement of large switches, pulsating input current, and complex driving circuit [15], [16]. High-voltage conversion gain can also be achieved by combining the VMs with the conventional boost converters [17]–[23] where some common advantages like adjustable voltage conversion ratio, lower voltage stresses on semiconductor components are evident. However, there are also some common disadvantages, first, at least two-phase interleaved boost converters have to be used together with the VMs, second, the combined duty cycle of the two switches has to be greater than 1 and there are limitations/boundaries of the selectable duty ratios. Based on buck–boost and SEPIC converters, two high step-up dc/dc converters capable of low voltage stress on the switch are proposed in [24] and [25], respectively. These two converters do not need additional switches, the control and drive circuit is as simple as basic dc/dc converters. However, as the topological structure of these two converters is fixed, the high step-up voltage conversion capacity of such converters cannot be changed.

This article presents a family of generalized passive circuits termed as “coat circuits” for dc/dc converters to acquire a variable high-voltage step-up capacity. These circuits are termed as coat circuits because such circuits surround the dc/dc converters like a coat and they only need additional passive elements to fit the voltage conversion ratio requirement akin to tailoring coats for peoples’ body frame requirements. The proposed coat circuits do not need any additional active switches, and they do not affect the control or driver circuit design. Topology, working principles, and performance characteristics of the dc/dc converters with the proposed coats are discussed in Sections II and III, respectively. The accuracy of the theoretical analysis and the converter characteristics are verified by experiments in Section IV.

II. TOPOLOGIES AND WORKING PRINCIPLE

Fig. 1 shows the topologies of the basic dc/dc converters with the proposed coat circuits. The structure of coat circuit for boost and SEPIC converters is identical and there are also two other common characteristics among these coat circuits.
1) All coat circuits are composed of several basic units, and the number of basic units can be adjusted according to the application requirements.
2) Each basic unit of the proposed coat circuits contains two capacitors, one inductor, and one diode.

Fig. 2 shows the topology of the Cuk converter with the coat circuit of two basic cells (Cuk-two basic cells (TBC)). To simplify, Cuk-TBC has been analyzed in Sections II–IV as an example. The assumptions for the analysis are given as follows.
1) All components are considered ideal and all effects of parasitic parameters are neglected.
2) The capacitance of all capacitors is larger enough and the influence of a capacitor voltage ripple is negligible.

Fig. 1. Topologies of the dc/dc converters with the proposed coat circuits. (a) Boost converter. (b) Cuk converter. (c) Buck–boost converter. (d) SEPIC converter. (e) Zeta converter.

Fig. 2. Topology of the Cuk converter with the coat circuit of two basic cells.
discharged as

\[
\begin{align*}
    u_{L1} &= u_{in} \\
    u_{L2} &= u_{C1} - u_{C2} \\
    u_{L11} &= u_{C1} + u_{C11} - u_{C12} \\
    u_{L21} &= u_{C1} + u_{C11} + u_{C21} - u_{C22}.
\end{align*}
\]

Mode 2 \([t_1-t_2]\), Fig. 3(b): Switch \(S_1\) is turned OFF. During this stage, all diodes work in the off-state. The inductor current of \(L_1\) branches off through three paths; first through \(C_1\), \(D_1\), and \(u_{in}\), second through \(C_1\), \(C_{11}\), \(D_{11}\), \(C_2\), and \(u_{in}\), and third through \(C_1\), \(C_{11}\), \(C_{21}\), \(D_{21}\), \(C_{12}\), and \(u_{in}\). The inductor current of \(L_2\) flows through \(D_1\) and \(C_2\), the inductor current of \(L_{11}\) flows through \(D_{11}, C_2\), and \(C_{12}\), the inductor current of \(L_{21}\) flows through \(D_{21}, C_{12}\), and the output stage \((C_{22}/R_L)\). In this interval, \(C_1, C_{11}\), and \(C_{21}\) are charged while \(C_2, C_{12}\), and \(C_{22}\) are discharged, and all inductor currents are decreased as

\[
\begin{align*}
    u_{L1} &= u_{in} - u_{C1} = u_{in} + u_{C2} - u_{C1} - u_{C11} \\
    &= u_{in} + u_{C12} - u_{C1} - u_{C11} - u_{C21} \\
    u_{L2} &= -u_{C2} = -u_{C11} \\
    u_{L11} &= u_{C2} - u_{C12} = -u_{C21} \\
    u_{L21} &= u_{C12} - u_{o}.
\end{align*}
\]

The working principle and analysis process of other converters are similar to the above analysis of Cuk-TBC and as such they are not discussed here.

### III. Performance Characteristics

The performance characteristics of Cuk-TBC are illustrated as an example in this section and the characteristics of other converters of Fig. 1 have been summarized in Table I.

#### A. Voltage Conversion Ratio

By volt-second balance of the inductor \(L_1\), \(L_2\), \(L_{11}\), and \(L_{21}\) as given in (1) and (2), the following formulae can be obtained:

\[
\begin{align*}
    u_C1 &= \frac{u_{in}}{1-D} \\
    u_{C2} &= \frac{D u_{in}}{1-D} \\
    u_{C11} &= u_{C21} = \frac{D_u u_{in}}{1-D} \\
    u_{C12} &= \frac{2D u_{in}}{1-D} \\
    u_0 &= u_{C22} = \frac{3D u_{in}}{1-D}.
\end{align*}
\]

Based on (3), the voltage conversion ratio \((M)\) can be obtained as follows:

\[
M = \frac{u_0}{u_{in}} = \frac{3D}{1-D}.
\]

Extending the above analysis to a converter with \(n\) basic cells

\[
\begin{align*}
    u_{C1} &= \frac{u_{in}}{1-D} \\
    u_{C2} &= u_{C11} = u_{C21} = \cdots = u_{C_{n1}} = \frac{D_u u_{in}}{1-D} \\
    u_{C12} &= \frac{1}{1-D} \\
    u_0 &= u_{C_{n2}} = \frac{(n+1) D u_{in}}{1-D} \\
    M &= \frac{u_0}{u_{in}} = \frac{(n+1) D}{1-D}
\end{align*}
\]

where \(i \in [1, n]\).
TABLE I

COMPARISON OF THE DC–DC CONVERTERS WITH AND WITHOUT THE PROPOSED COAT CIRCUITS

| Topology                  | Boost converter | Buck-boost converters | Cuk, SEPIC, Zeta converters |
|---------------------------|-----------------|-----------------------|-----------------------------|
|                           | with coat circuit | without coat circuit | with coat circuit | without coat circuit | with coat circuit | without coat circuit |
| Number of switches        | 1               | 1                     | 1                           | 1                       | 1               | 1               |
| Number of diodes          | 1+n             | 1                     | 1+n                         | 1                       | 1+n             | 1               |
| Number of inductors       | 1+n             | 1                     | 1+n                         | 1                       | 1+n             | 1               |
| Number of capacitors      | 1+n             | 1                     | 1+n                         | 1                       | 1+n             | 1               |
| Voltage conversion ratio  | 1 + n · D       | 1                     | (n+1) · D                   | D                       | (n+1) · D       | D               |
| Diode and Switch voltage stress | $u_{S1}$ = $u_{D1} = u_{C1} = \frac{u_{in}}{1 - D}$ | $u_{D11} = u_{C1} + u_{C11} - u_{C2} = \frac{u_{in}}{1 - D}$ | $u_{D21} = u_{C1} + u_{C21} - u_{C12} = \frac{u_{in}}{1 - D}$ | $u_{D21} = \cdots = u_{Dn1} = \frac{u_{in}}{1 - D}$ | $u_{o}$          | $u_{o}$          |

B. Voltage and Current Stress of Components

As shown in Fig. 2, the voltage stress on switch $S_1$, diodes $D_1$, $D_{11}$, and $D_{21}$ can be expressed as $u_{S1}$, $u_{D1}$, $u_{D11}$, and $u_{D21}$ respectively. Based on (3), they can be obtained as (7).

Based on (5), extending the voltage stress of diodes of the converter with $n$ basic cells is (8)

$$
\begin{align*}
\frac{u_{S1}}{1 + n \cdot D} = \frac{u_{D1}}{1 - D} = \frac{u_{C1}}{(n+1) \cdot D} = \frac{u_{C11}}{1 - D} = \frac{u_{C21}}{2 - n} = \frac{u_{D21}}{1 - D} = \frac{u_{o}}{(n+1) \cdot D} = \frac{u_{o}}{u_{o} + u_{o}}
\end{align*}
$$

The total voltage stress on diodes of the converter with $n$ basic cells can be calculated as (8), which is the same as the conventional Cuk converter. The voltage stress on switch of the converter with $n$ basic cells is lower than that of the conventional Cuk converter as given in (7). Therefore, the total voltage stress on semiconductor components with the coat circuit will be lower. However, when all the capacitors and inductors are taken into consideration, the total voltage stress on all components with the coat circuit will be higher.

In order to simplify the current analysis, the current ripple of $i_{L1}$, $i_{L2}$, $i_{L11}$, $i_{L21}$, and $i_o$ can be ignored, and their dc values are represented as $I_{L1}$, $I_{L2}$, $I_{L11}$, $I_{L21}$, and $I_o$, respectively. Based on capacitor charge balance requirement of $C_{22}$, $C_{21}$, $C_{12}$, $C_{11}$, and $C_2$, the average current of diodes $D_1$, $D_{11}$, $D_{21}$, and inductors $L_2$, $L_{11}$, and $L_{21}$ are found to be equal to the output average current $I_o$, which can be expressed as

$$
I_{D1} = I_{D11} = I_{D21} = I_{L2} = I_{L11} = I_{L21} = I_o.
$$

To simplify the analysis, the efficiency of the converter is assumed to be 100%. Thus, the input average current $I_{L1}$ is

$$
I_{L1} = I_o \cdot \frac{3D}{1 - D}.
$$

According to Fig. 3(a), the average and rms current of switch $S_1$ can be obtained as

$$
\begin{align*}
I_{S1} = I_o \cdot \frac{3D}{1 - D} \\
I_{S1-RMS} = \sqrt{\left(\frac{3D}{1 - D}\right)^2 \cdot D}.
\end{align*}
$$

When extending the analysis to the converter with $n$ basic cells, (12) can be obtained as

$$
\begin{align*}
I_{D1} = I_{D11} = I_{D21} = \cdots = I_{Dn1} = I_o \\
I_{L2} = I_{L21} = \cdots = I_{Ln1} = I_o \\
I_{L1} = I_{S1} = I_o \cdot \frac{(n+1)D}{1 - D} \\
I_{S1-RMS} = \sqrt{\left(\frac{(n+1)D}{1 - D}\right)^2 \cdot D}.
\end{align*}
$$

C. Characteristics of DC–DC Converters With and Without the Proposed Coat Circuits

The characteristics of basic dc–dc converters with and without coat circuits are shown in Table I. With the number of basic unit $n$ increases, the voltage conversion ratio of basic dc–dc converters is improved and the voltage stress on semiconductor components is decreased. Moreover, no additional switch is needed in coat circuit, which means the control and drive circuit of the converter with the coat circuit is as simple as the corresponding basic dc/dc converter.
IV. DISCONTINUOUS CURRENT MODE AND
BORDERLINE CONDITION

To simply the analysis process, assuming \( L_1 = L_2 = L_{11} = L_{21} = L \), that means peak to peak current ripples of inductor \( L_1 \), \( L_2 \), \( L_{11} \), and \( L_{21} \) are equal as shown in (13) and according to (1)–(3)

\[
\Delta i_{L1} = \Delta i_{L2} = \Delta i_{L11} = \Delta i_{L21} = \Delta i_L = \frac{u_{in} \cdot DT_s}{L}.
\]

As shown in Fig. 5, after the sum of \( i_{L2} \), \( i_{L11} \), and \( i_{L21} \) decreases to zero at \( t_2 \), the current direction of the inductors \( L_2, L_{11}, \) and \( L_{21} \) are reversed as shown in Fig. 6(a). During \( t_2 \) to \( t_3 \), \( i_{L1} \) decreases while \( i_{L2}, i_{L11}, \) and \( i_{L21} \) increase in the negative direction. When the amplitudes of \( i_{L1} \) and the sum of currents \( i_{L2}, i_{L11}, \) and \( i_{L21} \) are equal at \( t_3 \) which is denoted as \( I_3 \), diodes \( D_1, D_{11}, \) and \( D_{21} \) are turned off. During \( t_3 \) to \( t_4 \), \( i_{L1}, i_{L2}, i_{L11}, \) and \( i_{L21} \) are kept constant, as shown in Fig. 6(b).

By applying the principle of inductor volt-second balance to \( L_1, L_2, L_{11}, \) and \( L_{21}, \) (14) and (15) can be obtained as

\[
\begin{align*}
    u_{C1} &= u_{in} \cdot \frac{D+D_M}{D_M} \\
    u_{C11} &= u_{C21} = u_{C2} = u_{C1} \cdot \frac{D}{D+D_M} = u_{in} \cdot \frac{D}{D_M} \quad (14) \\
    u_o &= u_{C22} = u_{in} \cdot \frac{3D}{D_M} \\
    M &= \frac{u_o}{u_{in}} = \frac{3D}{D_M}. \quad (15)
\end{align*}
\]

The duty cycle \( D \) is the control signal of the converter and can be considered known. But \( D_M \) is unknown, and hence another equation is needed to eliminate \( D_M \) to obtain the voltage conversion ratio \( M \).

By capacitor charge balance of \( C_1, C_2, C_{11}, C_{12}, C_{21}, \) and \( C_{22} \), the average current of inductors \( L_2, L_{11}, \) and \( L_{21} \) is equal to the average output current \( I_o \). Additionally, according to the balance of input and output power of the converter, (16) can be deduced. Based on Fig. 5, the average current of inductors \( L_1, L_2, L_{11}, \) and \( L_{21} \) can also be calculated as in (17)

\[
\begin{align*}
    I_{L2} &= I_{L11} = I_{L21} = I_o = \frac{u_{in}}{R_L} \\
    I_{L1} &= \frac{u_{in}^2}{R_L u_{in}} \quad (16) \\
    I_{L2} &= I_{L11} = I_{L21} = \frac{u_{in}DT_s}{2L} \cdot (D + D_M) - \frac{I_M}{3} \\
    I_{L1} &= \frac{u_{in}DT_s}{2L} \cdot (D + D_M) + I_M. \quad (17)
\end{align*}
\]

By using (15)–(17), the voltage conversion ratio of the converter in discontinuous current mode (DCM) can be obtained as follows:

\[
M = \frac{u_o}{u_{in}} = \sqrt{\frac{2R_l D^2 T_s}{L}}. \quad (18)
\]

In the boundary condition mode, the voltage conversion ratio of the CCM is equal to that of the DCM, then from (4) and (18), the boundary factor, which is defined as \( \alpha \) here, can be obtained by (19). If \( \alpha \) is larger than 1, the converter works on DCM and if \( \alpha \) is smaller than 1, the converter works on CCM as

\[
\alpha = \frac{2(1 - D)^2 \cdot T_s \cdot R_L}{9L}. \quad (19)
\]

Extending the above analysis to a converter with \( n \) basic cells, the following equations can be obtained as:

\[
M = \frac{u_o}{u_{in}} = \sqrt{\frac{(n + 2)R_l D^2 T_s}{2L}} \quad (20) \\
\alpha = \frac{(n + 2) \cdot (1 - D)^2 \cdot T_s \cdot R_L}{2L \cdot (n + 1)^2}. \quad (21)
\]

The characteristics of the boost, buck–boost, and other basic dc/dc converters with the proposed coat circuits are summarized in Table II. Expressions for the boundary factor \( \alpha \), as well as for the solutions of the dc conversion ratios in CCM and DCM are given.
### TABLE II
**Summary of CCM–DCM Characteristics for the Basic DC–DC Converters With the Proposed Coat Circuits**

| Topology      | α (α>1, DCM)          | DCM $M$            | CCM $M$            |
|---------------|-----------------------|--------------------|--------------------|
| Boost         | $\frac{(1-D)^2 \cdot T_s \cdot R_L}{2L \cdot (1 + \alpha D)}$ | $\frac{1 + \sqrt{\frac{2(\alpha + 1) \cdot D^2 \cdot T_s \cdot R_L}{L}}}{1 + \frac{\alpha \cdot D}{1 - D}}$ | $\frac{1 + \frac{\alpha \cdot D}{1 - D}}{1 + \frac{\alpha \cdot D}{1 - D}}$ |
| Back-boost    | $\frac{(1-D)^2 \cdot T_s \cdot R_L}{2L \cdot (\alpha + 1)}$ | $\frac{1 + \sqrt{\frac{(\alpha + 1)R_L D^2 T_s}{2L}}}{(\alpha + 1) \cdot D}$ | $\frac{1 + \sqrt{\frac{2(\alpha + 1) \cdot D^2 \cdot T_s \cdot R_L}{L}}}{1 + \frac{\alpha \cdot D}{1 - D}}$ |
| Zeta, Sepic, Cuk | $\frac{(\alpha + 2) \cdot (1-D)^2 \cdot T_s \cdot R_L}{2L \cdot (\alpha + 1)^2}$ | $\frac{1 + \sqrt{\frac{(\alpha + 2) R_L D^2 T_s}{2L}}}{(\alpha + 2) \cdot D}$ | $\frac{1 + \sqrt{\frac{2(\alpha + 2) \cdot D^2 \cdot T_s \cdot R_L}{L}}}{1 + \frac{\alpha \cdot D}{1 - D}}$ |

---

**Fig. 7.** Experimental waveforms of the prototype when the input voltage is 48 V. (a) Duty cycle, input voltage, output voltage, and voltage across $S_1$. (b) Voltage across diodes. (c) and (d) Voltage across capacitors. (e) Inductor currents. (f) Diodes and $S_1$ currents.

**V. EXPERIMENTAL RESULTS**

A 200 W Cuk-TBC experimental prototype has been built to verify the accuracy of the above theoretical analysis. The specifications of the prototype are shown in Table III. The experimental waveforms are shown in Fig. 7. Fig. 7(a) shows the waveforms of $u_{\text{in}}$, $u_{\text{out}}$, $u_o$, and $u_{S1}$, the voltage conversion gain is approximately 8.4 when the duty cycle...
TABLE III
SPECIFICATIONS OF THE EXPERIMENTAL PROTOTYPE

| Parameter | Values |
|-----------|--------|
| Input voltage \((u_{in})\) | 48 V |
| Output voltage \((u_o)\) | 24-400 V |
| Output power \((P_o)\) | 200 W |
| Switching frequency \((f_s)\) | 100 kHz |
| Switch \((S_1)\) | IRFB4332 |
| Diodes \((D_{31}, D_{32})\) | IDT12560C |
| Capacitors \((C_1, C_{11}, C_{21}, C_2, C_{12}, C_{22})\) | 5 \(\mu\)F |
| Inductors \((L_{11}, L_{21}, L_{22})\) | 500 \(\mu\)H |
| Load resistance \((R_L)\) | 800 \(\Omega\) |

TABLE IV
VOLTAGE STRESSES ON ALL COMPONENTS OF THE EXPERIMENTAL PROTOTYPE

| Parameter | Theoretical analysis | Experimental results |
|-----------|----------------------|----------------------|
| Switch \((S_1)\) | 181.1 | 187 |
| Diodes \((D_{11}, D_{21})\) | 181.1 | 187 |
| Inductor \((L)\) | 48 (S_on) | 48 |
| | -133.1 (S_off) | -135 |
| Inductors \((L_{11}, L_{21}, L_{22})\) | 48 (S_on) | 50 |
| | -133.1 (S_off) | -135 |
| Capacitor \(C_1\) | 181.1 | 186 |
| Capacitors \((C_{11}, C_{21}, C_2)\) | 133.1 | 137 |
| Capacitor \(C_{12}\) | 266.3 | 270 |
| Capacitor \(C_{22}\) | 400 | 401 |

Moreover, theoretical analysis and experimental results of the voltage stress on all the components of the prototype are given in Table IV when output voltage is 400 V. The experimental results are nearly to 0.75, which is near to (6). Voltage waveforms across \(D_{11}, D_{11}, D_{21}\) are shown in Fig. 7(b), and voltage stress of the above diodes and \(S_1\) is approximately 187 V, which is consistent with (7). Fig. 7(c) and (d) shows the waveforms of \(u_{c2}, u_{c12}, u_{c22}, u_{c11}, u_{c21}\), and \(u_{c1}\). The average values of \(u_{c1}, u_{c12}, u_{c22}\) are about 185, 267, and 400 V, respectively, and the average value of \(u_{c11}, u_{c21}, u_{c2}\) is approximately 133 V, which is consistent with (5). Fig. 7(e) shows the current waveforms of \(L_{11}, L_{21}, L_{22}\). The dc value of \(i_{L1}\) is about 4 A, and the dc value of \(i_{L2}, i_{L11}, i_{L21}\) is about 0.5 A. Fig. 7(f) shows the current waveforms of \(i_{D1}, i_{D11}, i_{D21}\), and \(i_{D21}\). The dc value of \(i_{D1}\) is about 4 A, and the dc value of \(i_{D11}, i_{D11}, i_{D21}\) is about 0.5 A, which is consistent with (12).

Moreover, the calculated loss distribution of the experimental prototype is shown in Fig. 9(a) when the output voltage is 400 V, the main losses are on switch, diodes, and inductors, which are nearly to 3.05, 1.2, and 3.25 W, respectively. The calculated loss distribution of the experimental prototype is shown in Fig. 9(a) when the output voltage is 400 V, the main losses are on switch, diodes, and inductors, which are nearly to 3.05, 1.2, and 3.25 W, respectively. The thermal image of the prototype is given in Fig. 9(b) under the same working conditions. The ambient temperature is 25.8 °C, and the maximum temperature of the switch is about 50.9 °C. The thermal image has also proved the effectiveness of the calculation results.

The efficiency waveform of the converter under different loading condition is shown in Fig. 8(a). When the output power is 200 W, the maximum efficiency of the converter is nearly to 94.7%. The efficiency waveform of the converter with different output voltages is shown in Fig. 8(b). When the output voltage is 325 V, the maximum efficiency of the converter is nearly to 95%.

Moreover, theoretical analysis and experimental results of the voltage stress on all the components of the prototype are given in Table IV when output voltage is 400 V. The experimental results are the maximum voltage on the components of the prototype, due to the influence from capacitor ripple, the actual voltage stress on all the components of the converter will be higher than that under the ideal condition. Generally, the experimental results match well with those obtained from the theoretical analysis.

The efficiency waveform of the converter under different loading condition is shown in Fig. 8(a). When the output power is 200 W, the maximum efficiency of the converter is nearly to 94.7%. The efficiency waveform of the converter with different output voltages is shown in Fig. 8(b). When the output voltage is 325 V, the maximum efficiency of the converter is nearly to 95%.

The calculated loss distribution of the experimental prototype is shown in Fig. 9(a) when the output voltage is 400 V, the main losses are on switch, diodes, and inductors, which are nearly to 3.05, 1.2, and 3.25 W, respectively. The thermal image of the prototype is given in Fig. 9(b) under the same working conditions. The ambient temperature is 25.8 °C, and the maximum temperature of the switch is about 50.9 °C. The thermal image has also proved the effectiveness of the calculation results.

Fig. 10 shows a graph of conversion ratio \((M)\) versus duty cycle \((D, 0.1 < D < 1)\). The theoretical results are shown in blue while the experiment results are depicted in red. The experimental results are obtained when the input voltage is 10 V and the load resistor is 800 \(\Omega\). Evidently, when the duty cycle smaller than 0.8, the experiment results are close to the theoretical results. It is worth noting that the proposed “coat circuits” can extend the conversion ratio of traditional converter topologies but cannot neutralize the effects of parasitic components on traditional topologies.
A family of coat circuits for basic dc/dc converters to improve voltage conversion ratio have been proposed in this article. Theoretical analysis and experimental results show that the proposed circuits have the following advantages: 1) No additional active switches are needed, and the control and driver circuit are as simple as those of basic dc/dc converters; 2) voltage conversion ratio of the dc/dc converters have been improved effectively, and wide range input–output voltage conversion can be realized; and 3) the number of basic units in the coat circuits can be optimized to meet the requirements of different applications.

APPENDIX

The averaged switch model of the basic dc/dc converters with coat circuits can be obtained by using the circuit averaging method proposed in [3]. The averaged switch model of the Cuk-TBC in CCM is shown in Fig. 11. The symbol $\langle \cdot \rangle$ shows the dynamic changes of the parameter as shown in (A1) and (A2). $T_p$ is transformer primary winding, $T_{s1}$, $T_{s2}$, and $T_{s3}$ are transformer secondary windings (the transformer windings represent the active switch and diode operation in the average switched model).

\[
\begin{align*}
\langle d(t) \rangle_{T_S} &= D + \hat{d}(t) \\
\langle u_{in}(t) \rangle_{T_S} &= U_{in} + \hat{u}_{in}(t) \\
\langle u_a(t) \rangle_{T_S} &= U_a + \hat{u}_{a}(t) \\
\langle u_{C1}(t) \rangle_{T_S} &= U_{C1} + \hat{u}_{C1}(t) \\
\langle i_{Lj}(t) \rangle_{T_S} &= I_{Lj} + \hat{i}_{Lj}(t)
\end{align*}
\]

where $i$ is 1, 2, 11, 12, or 21, and $j$ is 1, 2, 11, or 21.

\[
\begin{align*}
\hat{u}_1 &= \hat{d}(t) \cdot \frac{U_{in}}{D} \\
\hat{i}_1 &= \hat{d}(t) \cdot \frac{I_{p1}}{D} \\
\hat{i}_2 &= \hat{d}(t) \cdot \frac{I_{p11}}{D} \\
\hat{i}_3 &= \hat{d}(t) \cdot \frac{I_{p21}}{D}.
\end{align*}
\]

REFERENCES

[1] W. Li and X. He, “Review of non-isolated high-step-up DC/DC converters in photovoltaic grid-connected applications,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1239–1250, Apr. 2011.
[2] B. Zhu, L. Ren, and X. Wu, “Kind of high step-up DC/DC converter using a novel voltage multiplier cell,” *IET Power Electron.*, vol. 10, no. 1, pp. 129–133, Jan. 2017.
[3] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. New York, NY, USA: Springer, 2001.
[4] F. L. Tofoli, D. C. Pereira, W. J. de Paula, and D. S. Oliveira Júnior, “Survey on non-isolated high-voltage step-up DC/DC topologies based on the boost converter,” *IET Power Electron.*, vol. 8, no. 10, pp. 2044–2057, Sep. 2015.
[5] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, “Step-up DC/DC converters: A comprehensive review of voltage-boosting techniques, topologies, and applications,” *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9143–9178, Dec. 2017.
[6] N. Zhang, G. Zhang, K. W. See, and B. Zhang, “A single-switch quadratic buck–boost converter with continuous input current and continuous output port current,” IEEE Trans. Power Electron., vol. 33, no. 5, pp. 4157–4166, May 2018.

[7] M. R. Banaei, H. Ardi, and A. Farahkar, “Analysis and implementation of a new single-switch buck-boost DC/DC converter,” IET Power Electron., vol. 7, no. 7, pp. 1906–1914, Jul. 2014.

[8] C. Chan, S. H. Chincholkar, and W. Jiang, “Adaptive current-mode control of a high-step-up DC/DC converter,” IEEE Trans. Power Electron., vol. 32, no. 9, pp. 7297–7305, Sep. 2017.

[9] M. Khaliliradeh and K. Abbaspardazeh, “Non-isolated high step-up DC/DC converter based on coupled inductor with reduced voltage stress,” IET Power Electron., vol. 8, no. 11, pp. 2184–2194, Apr. 2015.

[10] A. Ajami, H. Ardi, and A. Farahkar, “A novel high step-up DC/DC converter based on integrating coupled inductor and switched-capacitor techniques for renewable energy applications,” IEEE Trans. Ind. Electron., vol. 30, no. 8, pp. 4255–4263, Aug. 2015.

[11] M. Muhammad, M. Armstrong, and M. A. Elgendy, “Analysis and implementation of high-gain non-isolated DC/DC boost converter,” IET Power Electron., vol. 10, no. 11, pp. 1241–1249, Mar. 2017.

[12] H. Wu, K. Sun, L. Chen, L. Zhu, and Y. Xing, “High step-up/step-down soft-switching bidirectional dc/dc converter with coupled-inductor and voltage matching control for energy storage systems,” IEEE Trans. Ind. Electron., vol. 63, no. 5, pp. 2892–2903, May 2016.

[13] S.-W. Lee and H.-L. Do, “High step-up coupled-inductor cascade boost DC/DC converter with lossless passive snubber,” IEEE Trans. Ind. Electron., vol. 65, no. 10, pp. 7753–7761, Oct. 2018.

[14] X. Zhang, X. Ruan, and Q.-C. Zhong, “Improving the stability of cascaded DC/DC converter systems via shaping the input impedance of the load converter with a parallel or series virtual impedance,” IEEE Trans. Ind. Electron., vol. 62, no. 12, pp. 7499–7512, Dec. 2015.

[15] S. Li, Y. Zheng, B. Wu, and K. M. Smedley, “A family of resonant two-switch boosting switched-capacitor converter with ZVS operation and a wide line regulation range,” IEEE Trans. Power Electron., vol. 33, no. 11, pp. 448–456, Jan. 2018.

[16] B. Wu, S. Li, K. M. Smedley, and S. Singer, “A family of two-switch boosting switched-capacitor converters,” IEEE Trans. Power Electron., vol. 30, no. 10, pp. 6219–6235, Oct. 2015.

[17] B. P. Baddipadiga and M. Ferdowsi, “A high-voltage-gain dc-dc converter based on modified Dickson charge pump voltage multiplier,” IEEE Trans. Power Electron., vol. 32, no. 10, pp. 7707–7715, Jul. 2017.

[18] V. A. K. Prabhala, P. Fajri, Y. S. P. Gouribhatla, B. P. Baddipadiga, and M. Ferdowsi, “A dc–dc converter with high voltage gain and two input boost stages,” IEEE Trans. Power Electron., vol. 31, no. 6, pp. 4206–4215, Sep. 2016.

[19] B. Zhu, Q. Zeng, D. M. Vilathgamuwa, Y. Li, and X. She, “Non-isolated high voltage gain dual-input DC/DC converter with ZVT auxiliary circuit,” IET Power Electron., vol. 12, no. 4, pp. 861–868, Apr. 2019.

[20] L. Müller and J. W. Kimball, “High gain dc–dc converter based on the Cockcroft–Walton multiplier,” IEEE Trans. Power Electron., vol. 31, no. 9, pp. 6405–6415, Dec. 2016.

[21] M. Prudente, L. L. Pittscher, G. Emmendoerfer, E. F. Romaneli, and R. Gules, “Voltage multiplier cells applied to non-isolated DC-DC converters,” IEEE Trans. Power Electron., vol. 23, no. 2, pp. 871–887, Mar. 2008.

[22] B. P. R. Baddipadiga, V. A. Prabhala, and M. Ferdowsi, “A family of high-voltage-gain DC-DC converters based on a generalized structure,” IEEE Trans. Power Electron., vol. 33, no. 10, pp. 8399–8411, Oct. 2018.

[23] B. Zhu, Q. Zeng, Y. Chen, Y. Zhao, and S. Liu, “A dual input high step up DC-DC converter with ZVT auxiliary circuit,” IEEE Trans. Energy Convers., vol. 34, no. 1, pp. 161–169, Mar. 2019.

[24] M. R. Banaei and H. A. F. Bonab, “A novel structure for single-switch nonisolated transformerless buck–boost DC–DC converter,” IEEE Trans. Ind. Electron., vol. 64, no. 1, pp. 198–205, Jan. 2017.

[25] M. R. Banaei and S. G. Sani, “Analysis and implementation of a new SEPIC-based single-switch buck-boost DC-DC converter with continuous input current,” IEEE Trans. Power Electron., vol. 33, no. 12, pp. 10317–10325, Dec. 2018.

[26] F. Evran and M. T. Aydemir, “Isolated high step-up DC-DC converter with low voltage stress,” IEEE Trans. Power Electron., vol. 29, no. 7, pp. 3591–3603, Jul. 2014.

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