Challenges and targets of MRAM-enabled scaled spintronic logic circuits

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Abstract—Two benchmarking methods to analyse spintronic logic circuits based on MRAM technology are described, setting the target specifications to reach the performance of the 7 nm CMOS technology node. The energy-delay product (EDP) is used as a metric to compare a collection of logic circuits using magnetic tunnel junctions (MTJs) as logic input/output ports to 7 nm CMOS. Each method takes different levels of assumptions into account. Here we consider uniform benchmarking including solely input/output ports and majority-inverter-graph-based (MIG) benchmarking. The results highlight the importance of highly energy-efficient transducers that interface between magnetic and electric domains. The MIG-based benchmarking result draws attention to the importance of delays in magnetic computing as considerable contributors to the EDP. Additionally, the realization of fan-out and signal crossing in the magnetic domain is a key prerequisite for the physical implementation of efficient spintronic logic circuits.

I. INTRODUCTION

The ultralow energy associated with magnetization dynamics and nanomagnet switching in combination with the capability to build more expressive logic functions render spintronics a promising beyond CMOS approach \cite{1,2,3}. In particular, enabled by MRAM technologies, the recent demonstration of fully integrated, scaled, and CMOS-compatible logic devices based on magnetic domain wall (DW) transport and interaction has paved the way towards the practical realization of spintronic logic concepts \cite{4}. In this paper, we quantitatively explore the potential and the challenges of building Boolean logic spintronic circuits by quantifying their Energy-Delay product (EDP) as a figure-of-merit using two approaches, namely uniform \cite{5} and majority-inverter-graph (MIG) based benchmarking \cite{6}.

II. OVERVIEW OF THE BENCHMARKING APPROACHES

In uniform benchmarking (Fig. 1a), only the energy and delay associated with inputs and outputs ports are considered. Intermediate logic gates and interconnects between inputs and outputs are not included. This method is applicable to all technological concepts based on signal conversion at inputs and outputs. It provides a limit of the EDP for the total system as well as a target for minimum transducer efficiency when compared to CMOS. For DW-based logic circuits \cite{2} (Fig. 1b), only writing and reading EDPs of the MTJs used to generate and detect the information are considered. The MIG-based benchmarking also includes the spintronic circuitry between inputs and outputs via majority gates (MAJ) and inverters (INV).

Fig. 1. (a) Two approaches to benchmarking with different levels of circuit assumptions used. (b) A schematic of domain wall based spintronic logic circuits enabled by MTJs. The magnetic circuitry is not accounted in uniform benchmarking. (c) Uniform and MIG benchmarking representations of a 1-bit full adder.
the natural logic primitives in this case [7]. Majority-Inverter synthesis provides guidelines for the number of gates and how they are connected at the logic level. However, no physical placement and routing are yet considered. For example, in uniform benchmarking a 1-bit adder (see Fig. 1c) is defined by three inputs and two outputs. By contrast, in MIG benchmarking, six inputs, three MAJs and two INVs are taken into account.

In both benchmarking exercises, we use a set of representative combinational logic circuits (Fig. 2) from the EPFL benchmarking suite [8] with varying input and output bit counts and complexity levels. These circuits were also synthesised with a commercial software in 7nm CMOS technology [9] to compare spintronic circuits with CMOS currently in leading-edge mass production. The CMOS synthesis was optimised for low power and used to set targets for their spintronic counterparts. Both spin-transfer-torque (STT) [10] and spin-orbit-torque (SOT) [11] based MTJ technologies were considered. The energy and delay cost of MTJ based signal writing and reading [12] are summarised in Fig. 3.

### Table 1: Specifications of STT and SOT-MTJs

| Metric      | STT          | SOT          |
|-------------|--------------|--------------|
| CD (nm)     | 50           | 50           |
| \( R_{switch} \) (\( \Omega \)) | 2100         | 200          |
| \( J_{sw} \) (A/m²) | \( 7.7 \times 10^{10} \) | \( 110 \times 10^{10} \) |
| \( t_{write} \) (ns) | 5            | 1            |
| \( t_{read} \) (ns) | 3            | 1            |
| \( P_{read} \) (W) | \( 1.35 \times 10^{-2} \) | \( 2.07 \times 10^{-5} \) |

### III. RESULTS OF UNIFORM BENCHMARKING

Figure 4a shows a comparison of EDPs calculated for CMOS as well as SOT- and STT-MTJ enabled circuits. Circuits such as ‘ctrl’ and ‘router’ have two to four orders of magnitude higher EDP for spintronic circuits than for CMOS. This implies that the MTJ performance must be drastically improved to match CMOS. However, for circuits like ‘log2’ and ‘sqrt’, the spintronic EDP is lower than CMOS allowing a margin for magnetic circuitry to be included. The metric \( q \) defined by

\[
q = \frac{(Area \times Delay)_{CMOS}}{No. of Inputs + No. of Outputs}
\]

can be used to identify the circuits with lower/higher EDP compared to CMOS. Fig. 4b shows that circuits driven by sOT-MTJs with \( q > 10 \) have a remaining EDP budget. The area-delay product of CMOS circuits can be also viewed as a metric of the circuits’ complexity. Note that in this approach, the spintronic systems do not yet include the logic circuit itself, whereas this is included for CMOS. For complex circuits, this leads to a larger advantage of spintronic circuits, which is expected to reduce when the logic circuit is considered. For circuits where the energy-delay cost in writing and reading already exceeds the EDP budget set by CMOS, we apportion the difference in EDP to each individual MTJ, leading to performance targets of individual SOT/STT MTJs. Enhancements of 50x (SOT) to 1100x (STT) are required for MTJ devices, as shown in Fig. 4c. Note that improving writing and reading delays will have a much stronger impact on the EDP compared to improving power consumption since a longer delay also increases energy consumption.

### IV. MAJORITY-INVERTER-GRAPH (MIG) BASED BENCHMARKING

In addition to the minimum number of inputs and outputs considered in uniform benchmarking, we now examine how the majority gates and inverters can form logic circuits between inputs and outputs using MIGs. As an example, Fig. 5a shows a section of the MIG of the ‘ctrl’ circuit. The MIG synthesis was optimized to minimize the number of MAJs, and it assumes that the outputs of MAJ and INV have infinite fan-out and cascading capability in the magnetic domain.

As illustrated in Fig. 5a, there are two additional components revealed by MIG synthesis that needed to be considered in the benchmarking. First, each independent input can potentially drive multiple logic gates at different levels. To minimize the
delay due to signal propagation in long magnetic interconnects, we duplicate each primary input for the deeper logic levels. The increase in the number of inputs is summarized in Fig. 6a. An average factor of $10^\times$ is found for the analyzed circuits, which results in a similar increase of the EDP. Second, the delay of the circuits can be estimated by determining the longest path between inputs and outputs. For example, the longest path for the complete 'ctrl' circuit (Fig. 5b) is formed by 11 gates (8 MAJs and 3 INVs). Ideally, the delay of spintronic circuits should account for both the propagation delay between gates and the operation delay of each gate. However, since no routing and placement have yet been considered, we neglect the propagation delay. The operation delay of each MAJ is estimated to be 0.15 ns, considering a critical dimension of 50 nm (Fig. 7b) and a DW velocity of 750 m/s.[13]. Fig. 6b shows the maximum number of cascaded gates in each circuit and the corresponding total operation time vs. the total delay in CMOS circuits. The data shows that the computing time in spintronic circuits is already one order of magnitude greater than the total delay seen in CMOS circuits, with a large impact on the EDP.

Figure 6c shows the EDP of both CMOS circuits and spintronic circuits accounting for the increased number of inputs as well as for the operation time. The EDPs for all investigated circuits in spintronics are on average two orders of magnitude higher. As previously, we evenly distribute the EDP excess over the budget set by CMOS to all MTJs. As a result, performances of SOT- and STT-MTJs need to be improved by $\sim 300^\times$, and $\sim 5000^\times$, respectively (see Fig. 6d). For a circuit area analysis, we consider footprints of majority and inverter gates using STT-MTJs without accounting for magnetic interconnects. Fig. 7a shows that the area gain for spintronic circuits is not significant when compared to CMOS.
spintronic logic applications. Benchmarking the EDP of spintronic circuits based on Majority-Inverter-Graph synthesis has alleviated by the development of fast 3D magnetic interconnects with low energy costs for information propagation. Alternative further shown that energy-efficient transducers are key elements for competitive spintronic circuits. An enhancement of several spintronic circuits may be limited by fan-out and 2D routing restrictions in magnetic domain (see e.g. Fig. 7c). This can be voltage-based transducers may bridge this gap. Based on guidelines from MIG synthesis, the physical implementation of orders of magnitude is required with respect to current MRAM technology to reach the targets set by CMOS. Potentially, non-Boolean computing concepts may also compare more favorably with CMOS.

V. CONCLUSION AND OUTLOOK

The uniform benchmarking has been used to define an upper EDP bound of transducers as inputs and outputs for Boolean spintronic logic applications. Benchmarking the EDP of spintronic circuits based on Majority-Inverter-Graph synthesis has further shown that energy-efficient transducers are key elements for competitive spintronic circuits. An enhancement of several orders of magnitude is required with respect to current MRAM technology to reach the targets set by CMOS. Potentially, voltage-based transducers may bridge this gap. Based on guidelines from MIG synthesis, the physical implementation of spintronic circuits may be limited by fan-out and 2D routing restrictions in magnetic domain (see e.g. Fig. 7c). This can be alleviated by the development of fast 3D magnetic interconnects with low energy costs for information propagation. Alternative non-Boolean computing concepts may also compare more favorably with CMOS.

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