ABSTRACT

In this paper, we examine the integration potential and explore the design space of low power thermal reliable on-chip interconnect synthesis featuring nanophotonics Wavelength Division Multiplexing (WDM). With the recent advancements, it is foreseen that nanophotonics holds the promise to be employed for future on-chip data signalling due to its unique power efficiency, signal delay and huge multiplexing potential. However, there are major challenges to address before feasible on-chip integration could be reached. In this paper, we present GLOW, a hybrid global router to provide low power opto-electronic interconnect synthesis under the considerations of thermal reliability and various physical design constraints such as optical power, delay and signal quality. GLOW is evaluated with testing cases derived from ISPD07-08 global routing benchmarks. Compared with a greedy approach, GLOW demonstrates around 23%-50% of total optical power reduction, revealing great potential of on-chip WDM interconnect synthesis.

1. INTRODUCTION

As semiconductor technology roadmap extends into deeper sub-micron domain, the development of future high performance low power systems faces many key challenges. Among them, VLSI interconnect plays more and more critical roles due to: (1) growing ratio of interconnect versus gate delay; (2) higher operating frequency and design complexity; (3) challenging interconnect design for low power systems.

To address the interconnect challenges for future computing systems, various alternative techniques have been proposed as potential solutions (e.g., [13]). Among them, nanophotonics devices and interconnect attract active researches (e.g., [3-8]) due to their unique potential to make high speed low power on-chip interconnect.

The many recent advances in nanophotonics devices have demonstrated great on-chip integration potential in nanoscale optical modulators, photo-detectors, couplers, switches, waveguides and WDM (Wavelength Division Multiplexing) devices. Meanwhile researches on photonics device modeling (e.g., [7]) and on-chip integration (e.g., [9-14]) have also introduced new opportunities and challenges to the traditional architectural and physical design methodologies. Specifically, on-chip networks and special architecture designs have been proposed (e.g., [10] [13] [15]) to enable high throughput network communication with on-chip nanophotonic WDM links. Lately, active studies have been carried out to compensate the temperature dependence of nanophotonic devices at both fabrication level (e.g., [16] [17]) and on-chip network level (e.g., [18] [19]) to assist the design and optimization of thermal-reliable and power-efficient optical-electrical systems-on-chips.

At physical design level, however, studies for efficient on-chip photonics interconnect synthesis have been limited. An early work by [10] employed straight line single channel optical waveguides to perform system-on-package optical routing under some timing consideration. However, physical characteristics were not considered for photonic devices. Important issues such as optical link configuration, loss, thermal reliability and signal integrity were not properly studied. In [13], physical-layer effects (loss, power) are applied to photonics Network-On-Chip performance evaluation. Yet without a systematic CAD environment, it is difficult to design photonics architectures with optimal performance meanwhile taking full advantage of the power budget. In [11][12], a photonic interconnect library was presented with a physical synthesis framework for low optical power routing. But thermal reliability and WDM mechanisms were not included.

In this paper, we employ photonics on-chip WDM interconnect (Fig. 1) to achieve high density/capacity in the global routing stage. Based on device characterization and modeling, we propose GLOW, a new hybrid global router for power-efficient thermal-reliable physical synthesis featuring WDM waveguide placement, optical channel allocations and optical-electrical data converter planning. The rest of the paper is organized as follows: in Section 2, we motivate the WDM based optical routing problem under the critical consideration of thermal reliability and summarize the main contributions of this paper. In Section 3, we extend the Optical Interconnect Library (OIL) in [12] by introducing thermal and power related models of nanophotonics devices. In Section 4, we present an overview of our proposed CAD flow, followed by Section 5 and 6, in which we explain the detailed formulation and algorithms for GLOW together with an alternative greedy approach CAT. Section 7 presents the results, followed by conclusion in Section 8.

Figure 1: High routing capacity interconnect using WDM
2. MOTIVATION AND CONTRIBUTIONS

With on-chip WDM providing great signal multiplexing capacity, we motivate a global router to take advantage of WDM channels under various physical design constraints such as thermal reliability and timing. A simple scenario is illustrated in Fig. 2. Given a net (A,B,C,D) to be routed with node A as the driver pin, we aim to find a global routing solution in optical-electrical domain to satisfy:

- Thermal reliability and functionality
- Minimal optical driving power required
- Signal integrity and data conversion quality
- Timing considerations and WDM channel utilization
- Legalization based on opto-electrical domain design rules

**Definition i.** WDM link: A special hybrid on-chip interconnect consisting of electrical wires and optical wavelength division multiplexing devices for large signal capacity.

**Definition ii.** WDM trunk: The nanophotonic WDM waveguide on a WDM link is also referred to as a trunk.

**Definition iii.** WDM channel: The carrier of a modulated photonic signal on a WDM trunk. Each channel is assigned a unique central wavelength $\lambda$. An optical signal can be transmitted on a channel if its wavelength is between $\lambda - \frac{1}{2}BW$ and $\lambda + \frac{1}{2}BW$, where $BW$ is the channel bandwidth.

In Fig. 2, thermal issue refers to the scenario for which on-chip temperature variation causes extra power loss, signal degradation or even malfunction to the nanophotonics devices, such as modulator, photo-detector and WDM waveguide. Without careful planning, an opto-electrical link could fail due to big temperature change. During global routing, regions with excessive thermal variation can be simply set as blockages to avoid. Even for regions with acceptable thermal variation, there are still trade-offs to seek between power efficiency and thermal reliability, e.g., over-optimizing optical power efficiency could result in thermal failure, whereas over-margining the thermal reliability can cause more optical power loss, especially for ring-structure resonators.

Moreover, during routing in the opto-electrical domain, there are extra timing constraints to consider such that the optical-electrical interconnects provide no worse critical path delay than the routing solutions in the electrical domain. For example in Fig. 2, link A→B is routed with Cu interconnect while links A→C, A→D are partially merged with WDM trunks, meanwhile link A→D takes trunk1 due to the thermal blockage between sink D and trunk2. Data links from different nets must be assigned different wavelengths (i.e., channels) when sharing the same trunk.

For high WDM channel utilization rate, sharing onto a single WDM trunk is encouraged unless timing and/or thermal conditions are violated. In this case, path A→C would tend to merge with link A→D onto trunk1, but it is prohibited by the long delay from trunk1 to sink C.

Last but not the least, the final routing solution needs to deliver signals strong enough to be picked up by the photodetector, meanwhile be legalized according to design rules in both optical and electrical domains.

We summarize key contributions of this paper as follows,

- We propose a systematic CAD framework for on-chip WDM synthesis to co-optimize power and thermal reliability
- We develop a new thermal reliability models for nanophotonics devices considering WDM
- We formulate the optimal global routing problem with Integer Linear Programming technique
- We evaluate the CAD framework with various testcases derived from ISPD global routing benchmarks

3. NANOPHOTONICS DEVICE MODELS

We extend [12] with WDM modules to analyze on-chip optical link configurations, taking into account of power, loss, timing, temperature variation and thermal reliability.

3.1 Device Characterization

Based on current photonics fabrication technology, optical signalling has great advantage over low-K Cu interconnect (11ps versus 37ps per mm on Metal5/6) for global nets. Considering the delay overhead introduced by E-to-O and O-to-E data conversions, we define critical length $L_{crit}$ as the dimension of an on-chip link above which nanophotonics yield shorter signal delay than pure Cu interconnects:

$$T_{mod} + T_{det} + \tau_o \cdot L \leq \tau_e \cdot L$$

where $T_{mod}$ is the E-to-O modulation delay/bit and $T_{det}$ is the O-to-E photo-detection delay/bit; $\tau_o$ is signal delay per mm on OWG, $\tau_e$ is the delay per mm on Cu interconnect, $L$ is the length of the link. Solving Eqn. 1 gives us the range of $L$, whose lower boundary defines $L_{crit}$ value in mm. The devices employed in this paper are summarized in Table 1.

3.2 Thermal Reliability for WDM

Current on-chip WDM techniques mainly fall into the following categories: AWG (array waveguide) based, ring resonator based and thin film filter based, among which ring resonator cavity based add-drop filter techniques are most widely employed in architecture designs [13, 15, 19] due to its compact footprint (potential ultra density) and demonstrated high quality factor (Q). However, these devices can be very sensitive to ambient temperature change.

On-chip temperature fluctuation causes the central operating frequency (wavelength) of a photonic device to drift. If such a drift results in an off-set that falls outside the range of operating bandwidth (BW), the device will degrade or even malfunction. Especially for high energy efficiency on-chip WDM devices with ring resonator structure, the quality factor Q [22] (defined as the energy stored in the cavity versus the energy dissipated per unit cycle) is very high and BW is very narrow, thus their temperature sensitivity could lead to signal failure. The relationships between thermal reliability and quality factor Q are:

$$Q = \frac{\text{BW}}{\text{T}_\text{crit}}$$

Table 1: Device and interconnect model details

| Device | footprint | speed | E-power |
|--------|-----------|-------|---------|
| mod    | 30X40um   | 140Gb/s [20] | 20B | 0.7mW |
| detector | 20X20um | 40Gb/s | O-det power | E-power |
| delay  | 11ps/mm  | 1.5dB/cm | width | length |
| WDM    | 20X20um | 1.5dB/cm | 250nm | 300nm |
| Cu     | 3ps/mm   | 40m | 0.4mW | 1.4mm |

Cu interconnect on 22nm technology Metal5/6 with $p=2.2uF/$cm, $R_{junc}=0.022Ohm$, $C_{junc}$: MOSFET models for optimal gate sizing/repeater insertion are from Metal Gate/High-K/strained-Si PTM [21].
**4. OVERALL CAD FLOW**

In this section, we present the overall flow of our systematic CAD framework for low power thermal-aware on-chip WDM integration, using the models from Section 4.

In Fig. 3, we illustrate a top level flow diagram of our proposed method, starting from a given input netlist and on-chip temperature variation profile. The flow consists of 3 major stages: a Pre-routing stage that prepares the electrical netlist and WDM trunk placement; a Global Routing stage that serves as the core formulation of the WDM channel netlist and WDM trunk placement; and a Post-routing stage that further examines the legalization issues in both the optical and electrical domains. We detail the flow in Fig. 3 as follows.

**4.1 Netlist Pre-processing**

Netlist pre-processing step prepares the optical netlist with an initial consideration of the timing condition which guarantees that the circuit timing does not degrade after employing nanophotonics (since each data conversion takes significant time). This step is mainly proposed to derive optical netlist test cases from existing electrical benchmarks such as ISPD07-08 global routing netlists. This step is very critical since it selects proper pins (nets or partial nets) from the electrically placed netlist to synthesize in the Global Routing stage. The selection is designed such that the minimal Manhattan distance of all driver-sink pairs mapped onto the optical domain is lower bounded by the critical length $L_{crit}$. This step serves to yield non-negative timing gain in the optical domain than in the electrical domain. This aligns well with critical length definition and discussions in Section 4. The main technique involved is described as follows,

Pin Clustering: To cluster the electrically placed input netlist based on Manhattan distance using hierarchical clustering method. In this case, we first construct the dendrogram (illustrated in Fig. 4) and then pick out the clusters satisfying the $L_{crit}$ dimension with a depth first search on the dendrogram. The result of this procedure is a set of clusters whose respective geometric medians are mapped to the optical domain as pseudo-pins. These pseudo-pins form the Optical Netlist, while the rest of pins within each cluster remain on the electrical domain and are electrically interconnected to their geometric median. Therefore, only 1 O-to-E or E-to-O conversion is needed per cluster. This procedure is briefly illustrated in Fig. 4, where $a-f$ are pins of certain net in the electrical netlist and $ABD$ are pseudo pins (a partial net) mapped onto the optical plane to represent clusters with edges larger than $L_{crit}$ in the dendrogram. $B$ is the driver pin in optical domain since driver pin $c$ lies in the $bc$ cluster in electrical domain.

**4.2 Initial WDM Trunk Placement**

Initial WDM trunk placement depend on the median of geometry distributions of optical nets in the Optical Netlist and is carried out in a partitioned manner across the whole chip area according to Eq. (5) as a general guideline, until the total number of WDM channels is sufficient to hold the total number of optical nets/links in the netlist.

$$\text{Place}_{trunk} = \text{med}\{\text{med}\{\text{net} \}_i\}_i \in \text{Partition}^k$$

The partition based initial placement executes in steps:
- Continues for both horizontal and vertical directions
- Avoids over-heated regions marked as thermal blockages
- Partition ends when the number of WDM channels are sufficient for the total number of links in the optical netlist.
- Extra WDM trunks may need be added in Post-routing

**4.3 Thermal-aware Low Power Routing**

First, we define timing condition as the condition that guarantees smaller signalling delay on the opto-electrical link than on Cu interconnect. This is a critical consideration since each additional O-E/E-O data conversion brings significant delay. The thermal condition is defined to make sure the local temperature variation does not fall out of the working range of the ring modulators. In case of a violated thermal condition: (1) $Q$ value will be adjusted to trade-off power efficiency for thermal reliability; (2) if (1) can not be done without causing aliases between separate WDM channels, that particular region is set as a thermal blockage.
Algorithm 1 CAT: Channel Assignment for Thermal reliability

Input: (1) Initial WDM trunk placement
Input: (2) Temperature variation profile
Input: (3) Optical netlist
Generate \( L(\text{link}) \) as a set of all unassigned links/nets
Generate \( U(\text{link}) \) as a set of remaining available link resources

for each WDM trunk \( t \).

for each link \( k \) in the optical netlist do

Calculate timing constraint on \((\text{link}_k, \text{trunk}_t)\)
Calculate thermal variation constraint on \((\text{link}_k, \text{trunk}_t)\)
end for

Form set \( S(\text{link}_k) \) by links that satisfy Timing Condition
Sort \( S(\text{link}_k) \) based on ascending index order
Select \( \text{link}_k \in S(\text{link}_k) \) in ascending index order
while \( \text{link}_k \) unassigned AND \( \text{trunk}_t \) has available channels do

Assign \( \text{link}_k \) to WDM \( \text{trunk}_t \)
Update set \( L(\text{link}) \)
end while
end for

if \( U(\text{link}) = \emptyset \) AND \( L(\text{link}) = \emptyset \) then

Execute CAT on unassigned links
end if

return WDM channel assignment AND optical power

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Fig. 5 illustrates the routing problem after Pre-routing stage, with off-chip laser sources whose driving power to each WDM waveguide trunk varies depending on the total number of channels assigned. To constrain the solution space for the global routing stage, we take the shortest distance route when a pin is to connect to certain WDM trunk, i.e., data converters (mod/det) are placed along WDM trunks.

For the core formulation of the Global Routing stage, we propose 2 algorithms: (1) global routing with low power WDM (GLOW) as a major contribution of this paper; (2) channel assignment under thermal consideration (CAT) as a comparison baseline. Details are in Section 4.2 and 6.

4.4 Post Routing Legalization

This stage is mainly to resolve the cases when multiple rings are contending the same geometry location, causing design rule violations in the optical domain. For this paper, we use simple perturbation based re-routing/adjustment techniques, leaving other perspectives to detailed routing stages.

5. CAT ALGORITHM

CAT is designed as a greedy approach for Channel Assignment under Thermal considerations. The basic motivation is to assign optical nets/links to WDM trunks in a sequential manner, meanwhile to combine timing and thermal-awareness constraints locally for each WDM trunk. In particular, CAT picks all the local nets/link satisfying the timing condition and assign the least power consuming links to fill the available channels to certain WDM waveguide, then move onto the next waveguide. If eventually there are still remaining nets unassigned, then the Initial Placement stage will be repeated to include more WDM trunks/channels.

CAT is performed in 3 major steps: first, Initial WDM Trunk Placement; second, Timing and Thermal Condition Calculation; third, Greedy Channel Assignment.

Initial WDM Trunk Placement: The same as Section 4.2 which is used for both CAT and GLOW.

Timing and Thermal Condition Calculation: In this step, all the WDM trunks are traversed in certain order sequentially. For each trunk, timing/thermal conditions for all optical links are calculated and updated.

Greedy Channel Assignment: For the channel assignment, we use a greedy heuristic method which executes in 3 phases: Phase1: Form set \( S(\text{link}_k) \) for WDM \( \text{trunk}_k \) with the optical links that guarantee smaller signalling delay than in the electrical domain. \( S(\text{link}_k) \) is a set of link candidates to be assigned to WDM \( \text{trunk}_k \).

Phase2: Sort the links in \( S(\text{link}_k) \) with Thermal Condition metric in ascending order.

Phase3: Assign links from \( S(\text{link}_k) \) to \( \text{trunk}_k \), in ascending order, until the total number of optical nets assigned reaches \( C_{\text{max}} \). For more details of CAT, please refer to Algorithm 1.

6. GLOW ROUTING ALGORITHM

6.1 ILP Formulation

To formulate the optimal routing problem, we represent the assignment status of channels on WDM trunks with integer binary variables (occupied or available) and use the cross-term variables to model the optical power loss introduced by WDM signal crossings, which is otherwise very difficult to accurately characterize before the channel assignment takes place. Table 2 details all the variables defined.

- \( n, m \): total number of WDM trunks in the row and column directions after initial placement, respectively.
- \( \text{W}_i \): binary variables denoting the assignment status of WDM trunk \( i \). If \( \text{W}_i \) is 0, trunk \( i \) is not assigned any optical nets in the final routing solution, therefore will not be turned on (no input laser power from its optical IO port);
- \( \text{W}_i \): binary variables numerically equal to \( \text{W}_i \) for WDM \( i \), where \( i \in [0, n-1] \), \( j \in [n, n+m-1] \). 0 meaning trunk \( i \) and trunk \( j \) are not physically crossed; vice versa.
- \( S(\text{link}_k) \): integer variables, with 0 meaning link \( k \) is assigned onto WDM trunk \( i \).
- \( \text{sum}_{\text{link}_k} \): integer variables, representing the total number of optical nets assigned onto trunk \( j \) in the final solution.
- \( \lambda_{\text{net}_i} \): binary variables, 0 meaning net \( i \) is assigned onto WDM trunk \( j \) in the global routing; vice versa.

We propose the following objective function for GLOW’s thermal-aware low power routing featuring on-chip WDM:

\[
\text{Minimize} \{ P_{\text{total}} \} \text{ w.r.t } W_i, W_{ij}, S(\text{link}_k), \lambda_{\text{net}_i}, \lambda_{\text{net}_j} \quad (6)
\]

where

\[
P_{\text{total}} = P_{\text{loss}} + P_{\text{dynamic}} \quad (7)
\]

\[
P_{\text{loss}} = P_{\text{cross}} + P_{\text{trunk}\_hm} + P_{\text{ring}\_hm} + P_{\text{path}} \quad (8)
\]

\[
P_{\text{cross}} = \sum_{i \in [0, n-1]} W_{ij} * P_{\text{thm}}^{ij} \quad (9)
\]

\[
P_{\text{trunk}\_hm} = \sum_{i} W_{i} * P_{\text{trunk}\_hm}^{i} \quad (10)
\]
Table 2: Variables/parameters in ILP formulation

| Name                  | Description |
|-----------------------|-------------|
| $P_{total}$           | total laser power consumed |
| $P_{loss}$            | total on-chip laser power loss |
| $P_{dynamic}$         | total on-chip laser power for optical signaling |
| $P_0$                 | base power consumption for a WDM trunk |
| $P_{cross}$           | total power loss due to trunk crossings |
| $P_{thermal}$         | total power loss due to trunk thermal effects |
| $P_{link}$            | total laser power loss when trunk $i$, trunk $j$ cross |
| $P_{link,thermal}$    | thermal related power loss on trunk $i$ |
| $P_{ring}$            | laser power on the rings of link $i$ |
| $W_{ij}$              | BV: allocation status of trunk $i$ and trunk $j$ |
| $W_{0}$               | BV: crossing status of trunk $i$ |
| $S^{trunk}_{link}$    | BV: assignment status of link $i$ onto trunk $j$ |
| $Sum^{trunk}_{net}$   | IV: # of links in net $i$ assigned to trunk $j$ |
| $\lambda^{net}_{trunk}$ | BV: assignment status of net $i$ onto trunk $j$ |
| $T_{var}$             | temperature variation on the rings of link $i$ |
| $\lambda^{net}$       | channel capacity of each WDM trunk |
| $PIN_{max}$           | max pin # in certain net of the optical netlist |
| $temp_{threshold}$    | temperature variation tolerance threshold |
| $\tau_{c}$           | delay per unit length on Cu interconnect |
| $\tau_{o}$           | delay per unit length on optical links |
| $WL_{o}$             | delay overhead by data conversions |
| $WL_{i}$             | Cu wire length on link $i$ |
| $WL_{l}$             | optical wire length on link $i$ |
| HPWL$^{trunk}_{link}$ | half parameter wire length of link $i$ |

\[
P_{ring,thermal} = \sum_{i=1}^{\text{all trunks}} \sum_{j=1}^{\text{all links}} S_{\text{link}}^{\text{trunk}} \times P_{\text{link}}^{\text{ring}} \tag{11}
\]

\[
P_{\text{dynamic}} = \sum_{i=1}^{\text{all trunks}} \sum_{\text{all nets}} \lambda_{\text{net}}^{\text{trunk}} P_{i} + \sum_{i} W_{i} P_{0} \tag{12}
\]

Eq. (11) above gives the objective function of GLOW as the total power $P_{total}$ required to drive the circuit. As shown in Eq. (12), $P_{total}$ is divided into 2 parts: the total optical power loss on chip $P_{loss}$, which is the amount of power the drivers need to compensate for the guarantee of detection conditions on photo-detectors; and $P_{\text{dynamic}}$, the signal switching power on WDM channel carriers. $P_{loss}$ is divided into 4 terms: waveguide crossing power, thermal related WDM trunk power, thermal related ring resonator power and the power to compensate propagation loss of on-chip waveguide.

$P_{\text{dynamic}}$ consists of 2 terms: $P_{0}$ is the base power consumption for each WDM trunk, it is a constant power cost when turning on a N-channel WDM trunk; the 2nd term is the switching power on all WDM channels, which is linearly proportional to the number of channels utilized. Apparently, WDM trunk multiplexing/sharing rate is to be maximized in order to avoid unnecessary $P_{0}$’s.

All power related terms are modeled according to Section 3 and Section 4 Table 2 further details each term.

### 6.2 Physical Design Constraints

We present the detailed mathematical formulations of various routing constraints for GLOW as follows:

- **Timing constraint**: for each optical link, the routing solution must not result in longer signal delay than HPWL estimated delay in the electrical domain:
  \[
  S_{\text{link}}^{\text{trunk}} \left[ \tau_{c} * WL_{o} + \tau_{o} * WL_{i} + \tau_{conv} \right] \leq \tau_{c} * HPWL_{\text{link}}^{\text{trunk}} \tag{13}
  \]

- **Selection constraint**: to make sure each link $i$ is only assigned to one WDM trunk. For each link $i$:
  \[
  j \in \text{all trunks} \sum_{j=1}^{\text{all links}} S_{\text{link}}^{\text{trunk}} = 1 \tag{14}
  \]
  - **Channel capacity constraint**: to make sure each WDM trunk does not exceed its capacity limit. For each trunk $j$:
    \[
    \sum_{i} \lambda_{\text{net}}^{\text{trunk}} \leq C_{\text{max}} \tag{15}
    \]
  - **Detection constraint**: the final optical power at each sink on each link must be large enough to be detected.
  - **Thermal constraint**: for each link (pair of pins from source to sink), local temperature variation be upper bounded by $temp_{threshold}$ to avoid performance degradation or malfunction. For each link $i$ and trunk $j$:
    \[
    S_{\text{link}}^{\text{trunk}} \times T_{var} \leq temp_{threshold} \tag{16}
    \]
  - **Binary/Integer variable constraints**: since $W_{ij}$ and $\lambda_{\text{net}}^{\text{trunk}}$ are introduced to eliminate non-linear terms, the following constraints must be enforced:
    \[
    2W_{ij} \leq W_{i} + W_{j} \leq 1 + W_{ij} \tag{17}
    \]
    where $i \in [0, n-1]$, $j \in [n, n + m - 1]$
    \[
    \frac{2 \sum_{k} S_{\text{link}}^{\text{trunk}}(k) - 1}{2PIN_{\text{max}}} \leq \lambda_{\text{net}}^{\text{trunk}} \leq \frac{2 \sum_{k} S_{\text{link}}^{\text{trunk}}(k) - 1}{2PIN_{\text{max}}} \tag{18}
    \]
    \[
    \frac{2 \sum_{k} \lambda_{\text{net}}^{\text{trunk}}(k) - 1}{C_{\text{max}}} \leq W_{j} \leq 2 \sum_{k} \lambda_{\text{net}}^{\text{trunk}}(k) \tag{19}
    \]

Here $Equation (13)$ and $19$ are enforced for two-fold reasons: (1) we are able to calculate the number of optical nets assigned to certain WDM trunk via optical link related variables; (2) to introduce non-linear relation between $\lambda_{\text{net}}^{\text{trunk}}$ and $S_{\text{link}}^{\text{trunk}}$ under ILP formulation. For this part an intermediate term $Sum_{\text{net}}^{\text{trunk}}$ is introduced by $Equation (20)$:

\[
Sum_{\text{net}}^{\text{trunk}} = \sum_{k} S_{\text{link}}^{\text{trunk}} \tag{20}
\]

$Equation (18)$, $19$, $20$ together make sure that if $Sum_{\text{net}}^{\text{trunk}} = 0$, then $\lambda_{\text{net}}^{\text{trunk}} = 0$; if $Sum_{\text{net}}^{\text{trunk}} > 0$, then $\lambda_{\text{net}}^{\text{trunk}} = 1$.

They serve as a binary comparator meanwhile still preserve the linear programming formulation. $Algorithm 2$ summarizes the pseudo-codes of the main steps of $GLOW$.

### 7. SIMULATION AND TESTING

**Benchmarks and Simulation Setups**: In Table 3 we list 6 optical benchmarks: CK1-6, with net number ranging...
Table 3: Simulation result comparisons between our proposed CAT and GLOW

| Method       | CAT | GLOW |
|--------------|-----|------|
| Net #        | 35  | 70   |
| Pin #        | 95  | 317  |
| Sink #       | 60  | 369  |
| Trunk #      | 8   | 12   |
| Avg. Chan/trunk | -  | -    |
| Total trunk-length | 4.8 | 14.4 |
| Total power  | 1.45| 6.81 |
| Power reduc. % | -  | -    |

* Each WDM trunk has up to 32 available channels at initial placement. Unassigned WDM channels will be turned off after routing.

This paper explores the synthesis of on-chip nanophotonic WDM interconnects and presented GLOW, a low power optical router under thermal-reliability considerations. It is evaluated on various testing cases showing significant optical power reduction compared with a baseline greedy method. We believe a lot of future research can be done to co-optimize the CAD and the nanophotonics technologies in the physical design area.

8. CONCLUSION

In this paper, we show simulation results of CAT and GLOW, with total power consumption normalized to the power value that GLOW gives on CK1. Compared with CAT, GLOW demonstrates around 23%–50% of total power reductions on CK1-6, respectively.

Reasons of such improvement are mainly two-fold: first, CAT only searches for local optimal solutions and assign optical nets/links to WDM trunks in a sequential/local manner, while GLOW aims at global optimal solution with mathematical programming techniques; second, CAT is not aware of the waveguide crossing power, nor does it consider the thermal related ring resonator power-reliability trade-off globally; on the other hand, the ILP formulation of GLOW allows us to model all the key factors of optical power.

Also in Table 3 we show the WDM channel/trunk allocation of CAT and GLOW on CK1-6. We see that compared with GLOW, CAT assigns fewer number of WDM trunks, resulting in a slightly higher number of average WDM channels per trunk and shorter total length of on-chip WDM waveguide. GLOW, however, works by assigning WDM trunks/channels across the chip aiming at the global solution of power consumption minimization under given thermal reliability requirements. This helps GLOW to bring down the total power at the cost of some extra OWG wirelength. This is acceptable since the fabrication costs of straight OWGs are relatively low meanwhile there are resources on the silicon layer for the nanophotonics integration.

In some few cases when there are no feasible solutions exist, the ILP formulation will not return valid WDM channel/trunk allocation strategy and the WDM trunk initial placement must be adjusted (by adding more trunks). In this paper, such adjustments are carried out in a progressive and heuristic manner until feasible integer solutions are found. With accelerated ILP, GLOW manages to locate the optimal solutions for the 6 optical netlists in about 0.2 to 0.9 hours. Such run-time is acceptable as the optical routing problem size is fairly small, i.e., only the top global nets/pins are mapped into the optical domain while the rest nets are routed in the electrical domain.

REFERENCES

[1] McClelland et al. Design and Implementation of an Optical Interconnects for Communications On-Chip. In Proc. Int. Symp. on Physical Design, 2008.
[2] Navin Srivastava et al. Performance Analysis of Carbon Nanotube Interconnects for VLSI Applications. In ICCAD, 2005.
[3] David A. B. Miller. Device Requirement for Optical Interconnects to Silicon Chips. In Proc. of the IEEE, Special Issue on Silicon Photonics, 2009.
[4] Yongping Jiang et al. 80-micron Interaction Length Silicon Photonic Crystal Waveguide Modulator. In Applied Physics Letters, 2005.
[5] Varis Vlasis et al. Scalable Photonic Network for Next Generation Computing Systems. In Europs Congress on Optical Communications, 2008.
[6] C. O’Connor. Optical Solutions for System-Level Interconnect. In Proc. System Level Interconnect Prediction, 2004.
[7] Kyung-Ho Koo et al. Compact Performance Models and Comparisons for Gigascale On-Chip Global Interconnection Technologies. In IEEE Trans. on Electron Devices, 2009.
[8] A. A. Young et al. Optical I/O Technology for Tera-Scale Computing. In IEEE J. Solid-State Circuits, 2010.
[9] Jacob R. Mina et al. Optical Routing for 3D System-on-Chip. In Proc. Design, Automation and Test in Europe, 2006.
[10] Asef Shasham et al. Photonic Networks-on-Chip for Future Gene-ration Chip Multiprocessors. In IEEE Trans. on Computers, 2009.
[11] Duo Ding et al. O-Router: An Optical Routing Framework for Low Power On-Chip Silicon Nano-photonic Interconnects. In Proc. Design Automation Conf., 2009.
[12] Duo Ding et al. OIL: A Nanophotonic Optical Interconnect Library for a New Photonic Networks-on-Chip Architecture. In Proc. System Level Interconnect Prediction, 2009.
[13] Yan Pan et al. Firefly: Illuminating Future Network-on-Chip with Nanophotonics. In Proc. Int. Symp. on Computer Architecture, 2009.
[14] Johnnie Chan et al. PhoenixSim: A Simulator for Physical-Layer Analysis of Chip-to-Chip Photonic Interconnection Networks. In Proc. Design, Automation and Test in Europe, 2010.
[15] Ajay Joshi et al. Silicon-Photonic Clue Networks for Global On-Chip Communication. In Int. Symp. on Networks-on-Chip, 2009.
[16] Jong-Mou Lee et al. Controlling Temperature Dependence of Silicon Waveguide Using Slot Structure. In Optics Express, 2008.
[17] Biewapet Guha et al. CMOS-Compatible Athermal Silicon Microring Resonator. In Optics Express, 2009.
[18] Moonseok Mohamed et al. Power-Efficient Variation-Aware Photonic On-Chip Network Management. In Int. Symp. on Low Power Electronics Design, 2010.
[19] Zheng Li et al. IRIS: A Hybrid Nanophotonic Network Design for High-Performance and Low-Power On-Chip Communication. In J. on Emerging Trends in Computing Systems, 2011.
[20] Po Dong et al. Low Vpp, Ultra-low-energy, Compact, High-speed Silicon Electro-Optic Modulator. In OPTICS EXPRESS, 2009.
[21] Predictive Technology Model, http://ptm.asu.edu.
[22] Payam Rahbii et al. Polymer Micro-Ring Filters and Modulators. In J. of Lighth shines Technology, 2002.
[23] Roef is a CAD Suite for Photonics Device Simulation.