Semiconductor loss calculation of DC–DC modular multilevel converter for HVDC interconnections

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Abstract: DC–DC modular multilevel converter (DC–DC MMC) is an attractive candidate for high-voltage DC (HVDC) interconnections since it can provide the required voltage matching, galvanic isolation and flexible power control abilities. The semiconductor loss of such a DC–DC MMC is a major concern for both system evaluation and parameter design. However, it cannot be measured directly since it is out of the precision range of the high-voltage measuring equipment, and thus, mathematical analysis is considered as a feasible alternative. This paper proposes an accurate off-line loss calculation method for DC–DC MMC modulated by fundamental frequency modulation. Based on the characteristics of the modulation, the switching moments along with the instantaneous voltage and current can be calculated exactly, and the conduction loss and switching loss of each submodule can be expressed in a mathematical way. The calculation results are compared with the simulation results from a comprehensive switched model and show good accuracy performance within a relative error of ±2% under different operating conditions.

1 Introduction

The interconnection of two or more high-voltage DC (HVDC) grids is considered as a vital part of the establishment of future smart grids. It can enhance the reliability and effectiveness of the system by providing mutual power support and reducing the system reserve capacity. In this scenario, high-performance DC–DC converter is required.

Compared with traditional multilevel converters such as flying capacitor converter, neutral-point clamped converter or cascaded converter [1–4], modular multilevel converter (MMC) is a promising candidate due to its low switching frequency, low harmonic content, high level of modularity and simple implementation of redundancy. Many DC–DC topologies have been proposed based on MMC, which can be classified into non-isolated [5–8] and isolated types [9–16]. Non-isolated DC–DC MMC has the advantage of reduced investment cost and is preferable in high voltage, but common ground applications. However, in cases where galvanic isolation is required, the isolated DC–DC MMC with an interlinked transformer is necessary. Such isolated DC–DC MMCs could have many topology variations, as shown in Fig. 1. The structure of submodules could be half-bridge (HB) or full-bridge; for the primary (or secondary) side, the AC-link voltage could be generated with monopolar arrangement structure, or two- or three-arrangement structure according to different HVDC lines and power levels, as shown in Figs. 1a–c.

Different modulation technologies are feasible for such DC–DC MMCs. The quasi-2-level (Q2L) modulation and 2-level (2L) modulation were proposed in [9–12, 14], respectively, where submodules are almost switched synchronously and the AC-link voltage is modulated as trapezoidal or rectangular waveform. With Q2L and 2L modulations, the harmonics of current and voltage will be relatively high and thus leads to more conduction loss. On the other hand, the switching loss can be reduced since zero-voltage-switching is possible. The staircase modulation (or sinusoidal modulation) proposed in [8, 17–19] can ease the transformer design since the AC-link voltage is modulated as a sinusoidal-like staircase waveform. However, the switching loss can be more...
As one of the main operation parameters, the semiconductor loss is a key reference when designing heat dissipating system and selecting the type of devices. For the isolated DC–DC MMC, the total loss mainly consists of two parts: the semiconductor loss and the transformer loss. The transformer loss can be evaluated using simplified resistance model and data provided by the manufacturer [8]. Also, it can be obtained directly with measuring equipment. However, it is not practical to measure the semiconductor loss, since the total loss of semiconductors is usually below several percentages of the rated power, and is out of the precision range of the high-voltage measuring equipment. Therefore, this paper focuses on the calculation of semiconductor losses, and the transformer loss is out of scope. To address this issue, two methods are commonly used for loss calculation. The first approach is to build a comprehensive switched model of the converter using simulation software such as PSCAD/EMTDC and MATLAB/ Simulink [21], and calculate the loss with real-time simulation results. The calculation is highly accurate since the voltage and current can be obtained precisely and the switching and conduction characteristics of the semiconductors can be well described. However, the process is usually complex and time-consuming. Instead, calculating the loss by introducing mathematical analysis is considered as an efficient alternative.

Several techniques have been proposed to calculate the semiconductor loss of MMC for DC–AC conversion. Based on a thermal model, the conduction and switching loss were estimated in [22] by using the simulated current waveforms and specifications of the semiconductor under the premise of a constant junction temperature. Tu and Xu [23] also used simulated waveform of current, and the loss was estimated with junction temperature feedback. Rodrigues et al. [24] used the temperature correction factor to improve the accuracy, and an average strategy was introduced based on an assumption of the switch states. Zhang et al. [25] simplified the switching function into a continuous change rate function, and computational efficiency was further increased by replacing part of the detailed calculation by estimated upper limits. Yang et al. [26] derived a loss model with linear fitting method applied to the relationship between the loss and the current of semiconductors. In the existing literatures, losses are usually estimated by introducing the concept of probability and average. It is because that the switching frequency of the submodules in MMC is uncertain and would be affected by the employed sort-and-selection strategies for voltage balancing control. In this way, the error might be relatively large. Also, when simulated waveforms are used in the mathematical model, the online calculation process could be computationally intensive and time consuming for a large number of submodules.

For the proposed DC–DC MMC, the semiconductor loss calculation can be less complicated. Since the DC–DC MMC consists of two DC–AC MMCs, the existing mathematical methods are still viable. Besides, the reactive power in DC–DC MMC is often controlled to the minimum and the current is easy to be calculated with transmitted active power. These features facilitate the loss calculation, especially when FFM is applied. With FFM, the switching frequency of each submodule can be fixed at the fundamental frequency, and the associated sort-and-selection strategy is performed only once in each fundamental period, so that the switching frequency will not be affected by the voltage-balancing control. With FFM, not only the instantaneous voltage and current, but also the switching moments and state of each submodule can be determined precisely in an analytical way. This makes the loss calculation process not only accurate but also effective since it can be achieved off-line.

According to the aforementioned issues, this paper proposes a semiconductor loss calculation method based on a mathematical model for isolated DC–DC MMC with FFM. The remaining of the paper is organised as follows. In Section 2, the basic structure, modulation method and model of MMC are introduced. In Sections 3 and 4, the semiconductor loss calculation of a submodule and the overall converter are illustrated. The calculation results are compared with a comprehensive switched simulation results in Section 5, and the conclusion is drawn in Section 6.

2 Overview of the isolated DC–DC MMC

2.1 Topology of the isolated DC–DC MMC

For illustrative purpose, the simplest monopolar arrangement DC–DC MMC shown in Fig. 2 is used as an example in this paper. It is briefly introduced as follows:

(i) On the primary and the secondary sides, the monopolar arrangement is used and interlinked by an ideal transformer with turning ratio N, and a leakage inductance L. The coupled arm-inductors are with self-inductances L_up, L_down, and mutual inductances M_up, M_down.

(ii) The structure of submodules is selected as HB and each arm consists of N submodules. For each submodule, the DC-link capacitor C is inserted when the upper switch is turned on and T is turned off, and is bypassed when T is turned on and T is turned off.

(iii) The arm voltages of primary and secondary sides are denoted as V_up, V_down, and V_up, V_down, V_up, V_down are of staircase waveform modulated by FFM.

(iv) The capacitor dividers C_up, C_down are used to provide the middle points for both sides. They are sufficiently large and their voltages are treated as V_up = V /2 and V_down = V /2.

2.2 Modulation of the isolated DC–DC MMC

The FFM proposed in [15] is used for the isolated DC–DC MMC in this paper. As shown in Fig. 1b, each gating signal is strictly
turned on and off only once in a fundamental period $T_0$; and the voltage balancing is achieved by re-matching the gating signals and the submodules at the beginning of each fundamental period. Such a modulation method reduces the switching loss of the submodules.

With such a modulation method, the arm voltage can be determined by the modulation indexes $m_{\text{Up}}$ and $m_{\text{Lp}}$ (for the upper and lower arms in primary side), $m_{\text{Us}}$ and $m_{\text{Us}}$ (for the upper and lower arms in secondary side), which are defined as follows:

$$m_{\text{Up}} = 0.5 - M_d \cos(\omega_i t)$$
$$m_{\text{Lp}} = 0.5 + M_d \cos(\omega_i t)$$
$$m_{\text{Us}} = 0.5 - M_d \cos(\omega_i t - \gamma)$$
$$m_{\text{Ls}} = 0.5 + M_d \cos(\omega_i t - \gamma)$$

where $\omega_i = 2\pi/T_0$, $\gamma$ is the phase-shift angle between AC-link voltages of the primary and secondary sides. $M_d$ and $M_s$ are limited within $[0, 0.5]$, so that $m_{\text{Up}}, m_{\text{Lp}}, m_{\text{Us}}$ and $m_{\text{Ls}}$ can be normalised within $[0, 1]$.

Also, the exact switching moments of each submodule can be obtained so that the switching loss can be calculated precisely. As shown in Fig. 1b, the index $m_{\text{Up}}$ is compared with $N$ DC-levels $L_i (i)$

$$L_i = (2i - 1)/2N, \quad i = 1, 2, \ldots, N$$

Therefore, the switching moments of the $i$th submodule, denoted as $\alpha_i$ and $\beta_i$, can be determined as

$$L_i = 0.5 - M_d \cos(\omega_i t - \gamma)$$
$$1 - L_i = 0.5 + M_d \cos(\omega_i t - \gamma)$$

$\alpha_i$ and $\beta_i$ can be expressed as

$$\alpha_i = \arccos \left( \frac{0.5 - L_i}{M_d} \right)$$
$$\beta_i = 2\pi - \arccos \left( -0.5 + L_i \right)$$

### 2.3 Modelling of the isolated DC–DC MMC

To provide the basis of semiconductor loss calculation, the arm currents should be calculated. Several assumptions are made to simplify the model:

(i) The specifications of each submodule (including the semiconductors and the capacitor) are identical;
(ii) The number of submodules is large and their voltages are well balanced and regarded as equal, so that the harmonic components of the arm voltages are ignored;
(iii) For the same reason, the harmonic voltage and current components of AC-link are also ignored and considered as sinusoidal.

Based on these assumptions, the arm current can be expressed as

$$i_{\text{arm,Up}} = I_{dc,p} + \frac{1}{2} i_{1,p}$$
$$i_{\text{arm,Lp}} = I_{dc,p} - \frac{1}{2} i_{1,p}$$
$$i_{\text{arm,Us}} = I_{dc,s} - \frac{1}{2} i_{1,s}$$
$$i_{\text{arm,Ls}} = I_{dc,s} + \frac{1}{2} i_{1,s}$$

When the DC power $P_{dc}$ is given, the DC current in (6) can be easily calculated as

$$I_{dc,p} = P_{dc}/V_{dc,p} \quad \text{and} \quad I_{dc,s} = P_{dc}/V_{dc,s}$$

The AC components $i_{1,p}$ and $i_{1,s}$ in (6) can also be obtained by using the AC equivalent circuit of the converter presented in Fig. 3, where the primary and secondary sides are regarded as two voltage sources $u_p$ and $u_s$, and the power between primary and secondary sides is transmitted through the equivalent inductor $L_{eq}$. According to Kirchhoff voltage laws, the equivalent circuit can be described as

$$U_p \cos(\omega_i t) = U_s \cos(\omega_i t - \gamma) + L_{eq} \frac{di_{1,p}}{dt}$$

where $L_{eq} = (1/2)L_{eq} + (N/2)L_{eq} + L_{eq}$. $U_p = k_p \cdot M_{dp} V_{dc,p}$ and $U_s = k_s M_{ds} V_{dc,s}$, $k_p$ and $k_s$ are the correction factors from the modulation indexes $M_{dp,s}$ to the fundamental components of the arm voltages, which are introduced because these fundamental components might deviate from $M_{dp,s} V_{dc,p,s}$ especially when the number of the submodules is relatively low. The method to obtain $k_p$ and $k_s$ has been given [20] and thus is not repeated here.

The active power of AC-link can be obtained as

$$P_{ac} = \frac{U_p U_s \sin \gamma}{20 \omega_i L_{eq}}$$

Ideally, the active power of the AC-link $P_{ac}$ equals to $P_{dc}$. Based on (9), it can be seen that when DC power $P_{dc}$, modulation indexes $M_{dp,s}$ and DC voltage $V_{dc,p,s}$ are given, the phase-shift angle $\gamma$ can be obtained, and then the AC component of the arm currents $i_{1,p}$ and $i_{1,s}$ can be easily calculated as

$$i_{1,p} = I_p \sin(\alpha_i \psi_p + \phi_p)$$
$$i_{1,s} = N \cdot i_{1,p}$$

where

$$\gamma = \arcsin \left( \frac{2U_s L_{eq} P_{dc}}{U_p U_s} \right)$$

and

$$I_p = \frac{1}{\omega_i L_{eq}} \sqrt{U_p^2 - U_s^2 \cos^2 \gamma + U_s^2 \sin^2 \gamma}$$

Based on the developed analytical models (7) and (10), the current flowing through the submodules at any switching moments can be calculated and can be used for later loss calculation.
3 Loss analysis of the submodule

The loss of the semiconductors is composed of two parts, the conduction loss and switching loss. Based on the submodule voltage ($V_{dc}/N_p$ or $V_{dc}/N_s$) and current calculated by the models (6), (7) and (10), both types of losses can be calculated according to the different switch states. In this section, the conduction loss and switching loss are calculated, respectively, by taking the submodules of upper arm on primary side as an example.

3.1 Calculation of conduction loss

The switching pattern of the submodules with typical driving signal $g_{on}$ is illustrated in Fig. 4. As shown in Fig. 4, the current path depends both on the switch state and the direction of the arm current. When the arm current is positive, it will flow through switch $T_2$ if the submodule is bypassed as shown in case 1 of Fig. 4, and will flow through diode $D_1$ and charge the capacitor $C_{sm}$ if the submodule is inserted as shown in case 2. When the arm current is negative, it will flow through switch $T_1$ and discharge the capacitor $C_{sm}$ if the submodule is inserted, as shown in case 3, and will flow through diode $D_2$ if the submodule is bypassed, as shown in case 4.

The conduction loss of the semiconductor is resulted from two parts, the conduction resistance and the conduction voltage drop due to the bipolar-device nature of the IGBTs. Taking the certain submodule driven by gate $g_{on}$ in Fig. 4 as an example, the calculations are illustrated as follows:

In case 1, the arm current will flow through the IGBT $T_2$, hence the voltage drop can be expressed as

$$u_{T_2} = U_D0 + R_{CE}I_t$$  \hspace{1cm} (14)

where $U_D0$ and $R_{CE}$ are the threshold voltage and conduction resistance of $T_2$, which can be obtained from the manufacturer datasheet.

In one fundamental period, the conduction loss of $T_2$ can be expressed as

$$P_{cond,1on} = \frac{1}{T} \int_0^{\alpha_{1(on)}} u_{T_2} \delta t + \frac{1}{T} \int_{\alpha_{1(on)}}^{\alpha_{2}} u_{T_2} \delta t \hspace{1cm} (15)$$

where $\alpha_{1(on)}$ presents the turn-on moment of $g_{on}$, which can be calculated by (5), $\alpha_{2}$ is one of the zero-crossing points in one fundamental period of the arm current, as marked in Fig. 4, and can be calculated as

$$\alpha_{2} = \arccos \left( \frac{-2I_{dc,p}}{I_p} \right) + \pi - \phi_t$$ \hspace{1cm} (16)

Substituting (14) and (16) into (15), (15) can be reorganised as

$$P_{cond,1on} = \left( U_{T_2} \delta_{av1} + R_{CE} F_{Trms} \right) \cdot \frac{\alpha_{1(on)} + 2\pi - \alpha_{2}}{2\pi} \hspace{1cm} (17)$$

where $\delta_{av1}$ and $F_{Trms}$ are the average and RMS values of the current flowing through $T_2$ in one fundamental period, which can be given by

$$\delta_{av1} = \frac{1}{T} \int_0^{\alpha_{1(on)}} i \delta t + \frac{1}{T} \int_{\alpha_{1(on)}}^{\pi} i \delta t$$

$$F_{Trms} = \frac{1}{T} \int_0^{\alpha_{1(on)}} i^2 \delta t + \frac{1}{T} \int_{\alpha_{1(on)}}^{2\pi} i^2 \delta t$$ \hspace{1cm} (18)

In case 2, the arm current will flow through the diode $D_1$, hence the voltage drop can be expressed as

$$u_{D_1} = U_D0 + R_DI_t$$ \hspace{1cm} (19)

where $U_D0$ and $R_D$ are the threshold voltage and conduction resistance of $D_1$. Therefore, the conduction loss can be expressed as

$$P_{cond,1on} = \frac{1}{T} \int_0^{\alpha_{1(on)}} u_{D_1} i \delta t \hspace{1cm} (20)$$

where $\alpha_{1(on)}$ is another zero-crossing point of the arm current, as marked in Fig. 4, which can be calculated as

$$\alpha_{1(on)} = \arccos \left( \frac{-2I_{dc,p}}{I_p} \right) - \phi_t$$ \hspace{1cm} (21)

Therefore, (20) can be further deduced as

$$P_{cond,2on} = \left( U_{D_1} \delta_{av2} + R_D F_{Drms} \right) \times \frac{\alpha_{1(on)} - \alpha_{2}}{2\pi} \hspace{1cm} (22)$$

where $\delta_{av2}$ and $F_{Drms}$ are the average and RMS value of the current flowing through $D_1$ in one fundamental period, which can be given by

$$\delta_{av2} = \frac{1}{T} \int_0^{\alpha_{1(on)}} i \delta t$$

$$F_{Drms} = \frac{1}{T} \int_0^{\alpha_{1(on)}} i^2 \delta t$$ \hspace{1cm} (23)

Similarly, in case 3 the conduction loss can be calculated as

$$P_{cond,3on} = \left( U_{T_2} \delta_{av3} + R_{CE} F_{Trms} \right) \cdot \frac{\alpha_{1(on)} - \alpha_{3}}{2\pi} \hspace{1cm} (24)$$
where \( g_{\text{foss}} \) presents the turn-off moment of \( g_{\text{foss}} \), which can be calculated by (5). \( I_{\text{Dam}} \) and \( I_{\text{Dmax}} \) are the average and RMS values of the current flowing through \( T_1 \) in one fundamental period, which can be given by
\[
\begin{aligned}
I_{\text{Dam}} &= \frac{1}{T} \int_{0}^{t_{\text{Dam}}} i_d \, dt \\
I_{\text{Dmax}} &= \frac{1}{T} \int_{0}^{t_{\text{Dmax}}} i_d \, dt
\end{aligned}
\]

(25)

In case 4
\[
P_{\text{cond,4}} = \left( U_{\text{DC,Dam}} + R_s I_{\text{Dmax}} \right) \cdot \frac{\alpha_s - \alpha_{\text{foss}}}{2\pi}
\]

(26)

where \( I_{\text{Dam}} \) and \( I_{\text{Dmax}} \) are the average and RMS value of the current flowing through \( D_2 \) in one fundamental period, which can be given by
\[
\begin{aligned}
I_{\text{Dam}} &= \frac{1}{T} \int_{0}^{t_{\text{Dam}}} i_d \, dt \\
I_{\text{Dmax}} &= \frac{1}{T} \int_{0}^{t_{\text{Dmax}}} i_d \, dt
\end{aligned}
\]

(27)

### 3.2 Calculation of switching loss

The switching loss of the semiconductor consists of the turn-on loss and turn-off loss. The turn-on loss \( E_{\text{on}} \) of IGBT is resulted from the energy loss caused by the discharging of the capacitor between the emitter and collector. The turn-off losses of IGBT and diode \( E_{\text{off}} \) and \( E_{\text{rec}} \) come from the overlap area of voltage and current during the fall time of current. Since the turn-on loss of the diode is far less than turn-off loss, it is ignored in the loss calculation.

Generally, the turn-on and turn-off energy \( E_{\text{on}} \), and \( E_{\text{off}} \) of IGBT, the reverse recovery energy \( E_{\text{rec}} \) of the diode, and the reference voltage and current can be found from the manufacturer datasheet. They can be converted proportionately to adapt the operating condition, as
\[
\begin{aligned}
P_{\text{T,con}} &= \frac{i_r(t)}{I_{\text{off},T}} \cdot \frac{U_{\text{ref},T}}{f_s} \\
P_{\text{T,off}} &= \frac{i_r(t)}{I_{\text{off},T}} \cdot \frac{U_{\text{ref},T}}{f_s} \\
P_{\text{D,rec}} &= \frac{i_r(t)}{I_{\text{off},D}} \cdot \frac{U_{\text{ref},D}}{f_s}
\end{aligned}
\]

where \( f_s = 1/T_0 \) is the fundamental frequency, \( U_{\text{ref},T} \) and \( U_{\text{ref},D} (x = T, D) \) are the reference voltage and current, \( i_r(t), u_r(t) \) represent the instantaneous current and voltage of the semiconductor at the switching moment. Different from calculating the conduction loss, the switching loss is calculated based on the instantaneous state of submodules. Considering that inserting or bypassing a submodule involves a dead-time (a short period during which both IGBTs are turned off in case of shoot-through), the switching loss under different conditions are illustrated in Fig. 5.

(i) The arm current is positive: As shown in the top of Fig. 5a, the submodule is initially bypassed, and at the \( \alpha_{\text{foss}} \) moment, it is inserted into the arm so \( T_2 \) is first turned off, the current is commutated to \( D_1 \), introducing the turn-off loss of \( T_2 \). Such a loss can be calculated as
\[
P_{\text{switch,3,0}} = \frac{i_r(t_v)}{I_{\text{off},T}} \cdot \frac{u_r(t_v)}{U_{\text{ref},T}} E_{\text{off}} \cdot f_s
\]

(28)

After that, \( T_3 \) is turned on. However, no turn-on loss is caused since the current still flows through diode \( D_1 \).

As shown in the bottom of Fig. 5a, when the submodule is initially inserted and needs to be bypassed at the \( \alpha_{\text{foss}} \) moment, turning-off of \( T_1 \) will not change the current path. After a small dead-time, \( T_2 \) is turned on and \( D_1 \) is blocked reversely. Such a situation results in both the turn-on loss of \( T_2 \) and turn-off loss of \( D_1 \), which can be expressed as
\[
P_{\text{switch,3,0}} = \frac{i_r(t_v)}{I_{\text{off},T}} \cdot \frac{u_r(t_v)}{U_{\text{ref},T}} E_{\text{off}} \cdot f_s
\]

(30)

(ii) The arm current is negative: As shown in the top of Fig. 5b, the submodule is initially bypassed and needs to be inserted, so \( T_2 \) should be turned off at the \( \alpha_{\text{foss}} \) moment. However, this will not change the current path. After a small dead-time, \( T_1 \) is turned on and \( D_2 \) is blocked reversely. Such a situation results in both the turn-on loss of \( T_1 \) and turn-off loss of \( D_2 \), which can be expressed as
\[
P_{\text{switch,3,0}} = \frac{i_r(t_v)}{I_{\text{off},T}} \cdot \frac{u_r(t_v)}{U_{\text{ref},T}} E_{\text{off}} \cdot f_s
\]

(31)

As shown in the bottom of Fig. 5b, when the submodule is initially inserted and needs to be bypassed at the \( \alpha_{\text{foss}} \) moment, \( T_1 \) is turned off and the arm current is commutated to \( D_2 \) introducing the turn-off loss of \( T_1 \), which can be calculated as
\[
P_{\text{switch,3,0}} = \frac{i_r(t_v)}{I_{\text{off},D}} \cdot \frac{u_r(t_v)}{U_{\text{ref},D}} E_{\text{off}} \cdot f_s
\]

(32)

Since all the possible conditions are discussed, the switching loss of a specific submodule can be calculated by selecting the formula (29)–(32) based on the practical operation condition, i.e. the switching moment, whether the submodule is inserted or bypassed, and the direction and value of the arm current. All of the above information can be obtained using the derived model in Section 2.

### 4 Loss calculation of the isolated DC–DC MMC

In Section 3, all possible cases of the submodule operation involved with loss calculation are analysed. In this section, the flowchart of calculation is further designed. Since the upper and lower arm are considered to be symmetrical and there is no discrepancy between the specifications of the submodules, the loss from primary side is first calculated as an example in this section.

As can be seen in Fig. 6, the operating parameters, including the rated power \( P_{\text{dc}} \), DC voltages \( V_{\text{dc},1-6} \), and the modulation indexes \( M_{\text{dc},1-6} \), are first input. According to (7), (10), (6), (16) and (21), the expressions of arm current and the zero-crossing points can be obtained. For each submodule, its conduction loss and switching loss will be calculated sequentially.

For the \( i \)th submodule, the conduction loss is first calculated. According to the analysis, in one fundamental period, four cases may occur representing different conduction state of the semiconductors. As can be seen in Fig. 4, one fundamental period is divided into different time zones \( z_{\text{foss}} (x=5) \) based on both the switching moments of the submodule and the zero-crossing points of arm current. By judging the type of case, the conduction state of the semiconductors can be obtained and the conduction loss can be calculated referring to the method introduced with (14)–(27). After calculating the conduction loss of each time zone, the results are accumulated and stored as \( P_{\text{cond,4}} \) which represents for later calculation.

After that, the switching loss of the \( i \)th submodule is calculated. For the switching moments of the submodule \( \alpha_{\text{foss}} \) and \( \alpha_{\text{foss}} \) the direction of the arm current is used for judgement. If the arm

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current is positive at $\alpha_{r_i}$, the switching loss can be calculated with (29). Otherwise, it can be calculated with (31). If the arm current is positive at $\alpha_{f_i}$, the switching loss can be calculated with (30). Otherwise it can be calculated with (32). After finishing the calculation, results are accumulated and stored as $P_{\text{switch}_i}$, which represents for later calculation.

When both the conduction loss and switching loss of the $i$th submodule are calculated, the same process is applied to the next submodule, and then continues until $i > N$, so that the losses of all the submodules of the arm are considered. Since the calculation results of the lower arm in primary side are assumed to be the same as the upper arm, the sum of the calculation results of primary side are added up as

$$P_{\text{loss}_p} = 2 \sum_{i=1}^{N} (P_{\text{switch}_{i}} + P_{\text{cond}_{i}}) \quad (33)$$

The calculation of the conduction and switching loss of the secondary side upper $P_{\text{loss}_s}$ can also be conducted with the same process, the loss of the converter can be finally deduced

$$P_{\text{loss}} = P_{\text{loss}_p} + P_{\text{loss}_s} \quad (34)$$

5 Simulation verification

In order to verify the validity of the proposed calculation method, simulation platform based on a comprehensive switched model of isolated DC–DC MMC with FFM is built in MATLAB/Simulink software. The parameters are shown in Table 1. The semiconductor devices used in this paper are the IGBT modules of Mitsubishi (CM800HC_H66) 3300 V/800A. The parameters of the IGBT and the diode are also shown in Table 1.

In the simulation, the submodules number is $N = 5$, and the arm voltage and current from primary and secondary sides are illustrated in Fig. 7. It is seen that the arm currents $i_{\text{arm}_{\text{Up}},s}$ and $i_{\text{arm}_{\text{Lp}},s}$ are almost sinusoidal and mainly composed of DC and fundamental AC components; and although the arm voltages $v_{\text{arm}_{\text{Up}},s}$ and $v_{\text{arm}_{\text{Lp}},s}$ are staircase waveforms, it is also dominated by DC and fundamental frequency AC component, and can be considered as sinusoidal by ignoring the harmonic components.

To prove the validity of the proposed method, the phase-shift angle is changed from 0.524 to 5.766 rad, and the DC power $P_{\text{dc}}$ is varied from $-108.7$ to $217.3$ kW, as shown in Table 2. The phase and amplitude of arm current from both primary and secondary sides also change along with the phase-shift angle. The calculation results compared with the simulation results of primary and secondary sides are presented in Figs. 8a and 8b, respectively. The relative error $e_r$ is defined as

$$e_r(n) = \frac{P_{\text{cal}}(n) - P_{\text{sim}}(n)}{P_{\text{cal}}(n)} \times 100\% \quad (35)$$

where $P_{\text{cal}(n)}$, $P_{\text{sim}(n)}$ are the calculation and simulation results of number $n$ condition ($1 \leq n \leq 12$).

As shown in Fig. 8c, the relative errors $e_r(n)$ in all conditions are restricted to $\pm 2\%$. Referring to the relative errors ($2.5$–$10\%$) given in the literatures [25–28], the relative error in our study is small enough for submodule thermal design and system evaluation.

To further validate the proposed calculation method, the system is tested under other two different fundamental frequencies, 800 and 1200 Hz. As shown in Fig. 9a, as the frequency increased, the
total semiconductor loss also increases. Moreover, it can be observed in Fig. 9b that the conduction loss is almost unchanged. It is because that the conduction loss only depends on the device parameters and the arm current, which is analysed in (14)–(27). Obviously, the difference of the total semiconductor loss is mainly derived from the switching loss, as can be seen in Fig. 9c. The switching loss is sensitive to the increment of the fundamental

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**Table 1** Simulation parameters

| Parameter of the circuit | Value | Parameter of semiconductors | Value |
|--------------------------|-------|----------------------------|-------|
| $V_{dc,p}$               | 10 kV | $R_{CE}$                   | 0.01 Ω |
| $V_{dc,s}$               | 5 kV  | $U_D$                      | 1 V   |
| $L_{ap}, L_{as}$         | 13.4 mH | $E_{on}$                | 1.1 J  |
| $C_{div,p}, C_{div,s}$  | 10 mF | $E_{off}$                  | 1.05 J |
| $C_{sm}$                 | 600 μF | $R_D$                     | 0.01 Ω |
| $M_{dp}, M_{ds}$         | 0.5   | $U_D$                      | 0.7 V  |
| $N$                      | 5     | $E_{rec}$                  | 0.6 V  |
| $f$                      | 1000 Hz | —                         | —     |

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**Table 2** Parameters of the operation condition

| Number | Phase-shift angle $\gamma$, rad | Rated power $P_{dc}$, kW |
|--------|---------------------------------|--------------------------|
| 1      | 0.524                           | 108.7                    |
| 2      | 1.047                           | 188.2                    |
| 3      | 1.571                           | 217.3                    |
| 4      | 2.094                           | 188.2                    |
| 5      | 2.618                           | 108.7                    |
| 6      | 2.967                           | 377.3                    |
| 7      | 3.316                           | -377.3                   |
| 8      | 3.752                           | -124.6                   |
| 9      | 4.276                           | -196.9                   |
| 10     | 4.8                             | -196.9                   |
| 11     | 5.323                           | -178                     |
| 12     | 5.76                            | -108.7                   |

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**Fig. 6** Flowchart of semiconductor loss calculation

**Fig. 7** Key waveforms of the DC–DC MMC

(a) Arm current and arm voltage of the primary side, (b) Arm current and arm voltage of the secondary side
frequency and increases distinctly, which implies that the fundamental frequency $f_0$ can affect the switching loss directly as analysed in (28)–(32). In both Figs. 8 and 9, the simulation results match well to the calculation results, which proves the validity of the proposed method.

### 6 Conclusion

The paper has proposed a semiconductor loss calculation method for isolated DC–DC MMC with AC-link. Based on the fact that the AC-link is with high frequency, the proposed method has neglected the harmonic components so that the arm voltages and currents can
be simplified and expressed analytically; based on the fact that the DC–DC MMC is modulated by FFM, the switching moments of each submodule have been calculated precisely, and both the conduction loss and switching loss have been expressed in an analytical way. A calculation flowchart has also been provided to calculate the total loss. The calculation results have been compared with the simulation results from a comprehensive switched model, and the proposed method shows good effectiveness within relative errors of ±2%.

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8 References

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