Design of Photovoltaic Inverter Based on STM32 Microcontrollers

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Abstract. In this paper, the STM32 microprocessor is used as the central control core, and a 500W photovoltaic inverter is designed. The inverter adopts a two-stage conversion structure. The high-speed timer of the STM32 microprocessor generates high-resolution PWM and SPWM pulses and drives the first-stage DC/DC converor after driving the chip through UCC27324 and IR2111 respectively. The rectification and the second-stage DC/AC inverter convert the DC signal into a utility frequency. In order to reduce the higher harmonics derived from the DC/AC inverter, the circuit also adopts the principle of LC filter design. Finally, in the Multisim simulation, the operation is stable. The error of the output AC voltage is controlled within 3%. It is said that the inverter has the advantages of high reliability, low harmonic content, and high efficiency.

1. Introduction
Photovoltaic (PV) inverter is the core device for energy conversion of the photovoltaic power generation system, which plays a decisive role in the safety, energy conversion efficiency and stability of the system. Therefore, in order to improve the power generation efficiency and improve the control ability of the photovoltaic power generation system, it is of considerable significance to study a high performance photovoltaic off-grid inverter.

System and Structure
The structural design of the photovoltaic off-grid inverter is shown in Figure 1. It consists of several parts: STM32 microprocessor, conversion circuit, and sampling circuit. The STM32 microprocessor (MCU) generates pulse width modulation (PWM), and sinusoidal pulse width modulation (SPWM) signals to be amplified by the driving circuit to control the MOSFET switch in the conversion circuit, thereby achieving the purpose of boosting and rectifying the input voltage and converting to the DC voltage. The output voltage wave of the conversion circuit is a high-voltage SPWM pulse wave, and a smooth sinusoidal AC voltage wave is obtained after passing through the LC low-pass filter circuit. In order to stably output sinusoidal alternating current, the voltage and current sampling circuit samples the voltage and current signals outputted by the DC/DC converter into a low-voltage DC signal, and then connects to the I/O port of STM32 and converts the data signal and the PWM signal by the built-in ADC. It results in obtaining a modulated PWM signal [1].
Due to the output voltage of the PV array and its instability, in order to provide continuous and stable power supply to the load in this design, the STM32 controls the battery for additional power supply when the PV output voltage is insufficient. The MOSFET of the inverter is in the working stage of high-frequency [2], the heat emitted by the system may cause the inverter system to work at high temperature, and the damage to the electronic device is significant. In order to improve the lifetime of the inverter, the cooling system consisting of a temperature sensor is also designed.

2. Hardware design

2.1. Boost converter circuit
PV modules are easily interfered by various external factors. For this reason, the photovoltaic output voltage fluctuates greatly and needs to be converted to a stable bus voltage by boosting [3]. Therefore, the boost converter circuit shown in Figure 2 is designed. The output current and voltage are 2A and 310V respectively. For this diode D1, it has a strong forward surge withstand capability (SWC) of 30A and a high reverse breakdown voltage of 1000V. The switch adopts an N-channel MOSFET 2SK3070S with a working frequency of 50 kHz, a maximum forward withstand voltage of 600V, and an on-resistance of 0.3 Ω. In order to ensure that the boost converter circuit operates in the continuous mode of the inductor current, the value of the inductor L1 is selected to be ten mH, and the ripple voltage is required to be no more than 1%.

2.2. Single-phase full-bridge inverter circuit design
In order to meet the design requirements for the 500W inverter, the power switch tube IRF840 is selected. As shown in Figure 3, the inverter circuit is composed of four IRF840s to form four bridge arms. Q3 and Q6 form a pair of bridge arms driven by the same group of pulses, and Q4 and Q5 form a pair of bridge arms operated by the same group of pulses [4]. The two sets of complementary drive pulses are PWM pulses that are sinusoidally varied using a duty ratio to drive the bridge arms to convert the DC to the sinusoidal AC power source.

Due to the inherent characteristics of PWM technology, the output voltage of the inverter circuit contains a lot of higher harmonics. Therefore, a low-pass filter is needed at the output to reduce the
harmonic content and smooth the sinusoidal output voltage. The passive low-pass filter network designed in this paper consists of a first-order LC low-pass filter and an EMI filter [5], which filters the SPWM output waveform after power amplification. According to the principle of the LC low-pass filter, the cutoff frequency of the designed LC filter circuit is

\[ f_0 = \frac{1}{2\pi\sqrt{LC}}. \]  

(1)

Since the AC output frequency is 50 Hz for the inverter, the upper limit of the cutoff frequency \( f_z \) of the LC filter is taken as 100 Hz. Considering the speed characteristics of the power components, the frequency of SPWM should not be too high. The \( f_z \) is 17.5KHz in the design, and the cutoff frequency of the filter can be calculated according to the equation (1):

\[ f_0 = \sqrt{f_z f_s}. \]  

(2)

The cutoff frequency is 1323 Hz from the equation (2), and the capacitance \( C_2=4.7 \mu F \) and the inductance \( L_1=2.5 \, mH \) are taken. The parameters for the post-stage EMI filter can take the conjugate inductor of 20\( \mu H \) and the large capacitor (104).

2.3. Drive circuit design

Since the I/O output of STM32 is 3.3V logic level and cannot directly drive the FET, the PWM drive circuit shown in Figure 4 is designed to drive the boost converter circuit. This design uses a dual MOSFET driver UCC27324 to build the drive circuit. The UCC27324 has a simple peripheral circuit and strong driving capability. It is a low power dissipation MOSFET with a supply voltage of VDD of 12V and 3.3V logic level. The output of PWM pulse for STM32 can be connected to the input with the protection resistor. Then the gate of MOSFET powered by STM32 turns on and off.

At the same time, the SPWM driving circuit shown in Figure 5 is also designed. The pins of STM32 can only work normally at a low level. In order to electrically isolate it from the high voltage side, the
2.4. Sampling circuit design

This design is controlled the stable output of AC 310V by regulating the high-voltage DC bus, so the sampling circuit is needed to sample the current and voltage of the high-voltage DC bus. The output signal of the sampling circuit is sent to the ADC of STM32. It is also necessary to consider the electrical isolation between the high side and the control side. Therefore, in the sampling circuit design, the optocoupler isolation amplifier HCPL-7840 is used for current and voltage sampling. The HCPL-7840 is a dedicated current/voltage detection optocoupler that is immune to external magnetic fields, has good linearity, small size, and low cost. Since the specification of the inverter is 500W, considering the back-end inverter efficiency, the boost DC is not exceeded 2A at most. The high-power manganese copper wire resistance of 0.1Ω is selected as the current sampling resistor, and the output current detection circuit is shown in Figure 6. If the output current is I_OUT, according to equation (3), the output current range is reached 3A under the premise that the output detection circuit AD_I is not exceeded 2.5V, which meets the design requirements.

\[
AD_I = 8 \times R37 \times I_{OUT}
\]  

(3)

When designing the output current and voltage detection circuit for the high-voltage DC bus of 310V, it is necessary to select the appropriate resistors for a voltage divider and a current sampling and consider the internal 8x amplification relationship of the linear optocoupler HCPL-7840 and the STM32 internal A/D converter with voltage reference of 2.5V. According to equation (4), when the output voltage is 310V, the voltage detection circuit outputs 1.264V, which is within the range of voltage reference and has a positive voltage margin to meet the design requirements. The output voltage detection circuit is shown in Figure 7.

\[
AD_U = \frac{R_{22}}{R_{21} + R_{22}} \times 8 \times 310
\]  

(4)
Figure 7. DC voltage detection circuit for the output.

In the design of the inverter, most of them are constructed with high-frequency switching tubes, which lead to the temperature rise of the inverter as the operating temperature of the inverter increases. When the temperature is too high, the cooling fan is started. The temperature sensor NTC-10K is selected, which is small and placed directly in the heat sink to make the temperature measurement closer to the inverter temperature. The circuit diagram is shown in Figure 8. The first half is the bridge measurement circuit, the middle is the amplifier circuit dominated by the instrumentation amplifier AD620, and the second half is the voltage clamp and overcurrent protection circuit.

The specific model of the negative temperature coefficient sensor is MF52-103/3435, and the temperature range is from -55°C to 125°C. When the temperature is equal to 25°C, the resistance is 10kΩ. As the temperature increases, the resistance gradually decreases. In this design, it is only necessary to start the cooling fan when the temperature of the inverter heat sink is higher than 45°C, and it is not necessary to know the accurate temperature value in other cases of the inverter. In the circuit design, the instrumentation amplifier is powered by a single power supply. The AD620 outputs the voltage signal only when the temperature of the heat sink is greater than 25°C. Below this value, the output is 0V. This design eliminates the need for the voltage boost circuit on the output side of AD620, simplifying circuit design. Also, the capacitor C14 is filtered out the differential mode noise in the input signal of AD620. The capacitors C15 and C16 have filtered the common mode noise in the input signal, making the temperature data acquisition more accurate. The AD620 has a high common-mode rejection ratio, low noise, and low input offset voltage. It is mainly used in high-precision data acquisition systems. The calculation formula of gain $G$ is

$$G = \frac{49.4K\Omega}{R_{37}} + 1. \quad (5)$$

When setting the gain, it is considered that the output of AD620 should not be higher than 3.3V within the normal operating temperature range of the inverter. Otherwise, the AD620 and the microcontroller are damaged. The current limiting resistors R38 and R39 are designed to limit the overcurrent of AD620 and STM32, respectively, and function as current limiting protection. The output voltage of AD620 is calculated as:

$$V_{th} = 2.5 \times \left( \frac{R_{30}}{R_{20} + R_{30}} - \frac{R_{32}}{R_{31} + R_{32}} \right). \quad (6)$$
3. Simulation Results and Discussion

3.1. Boost converter circuit simulation
In NI Multisim, the boost converter circuit is built for the simulation. When the input voltage is +12V, the simulation output is shown in Figure 9. It can be seen from Figure 9 that the output voltage of the boost converter circuit is about 304V. The ripple is detected after the output voltage is stable. The period of ripple voltage is about 2ms, and the range of ripple voltage is from 100mV to 200mV, which is much smaller than the design requirement (less than 1%).

3.2. Single-phase full-bridge inverter circuit simulation
The single-phase full-bridge inverter circuit is built in NI Multisim for the simulation. The simulation results are shown in Figure 10, Figure 11, Figure 12 and Figure 13. Figure 10 is the SPWM waveform amplified by the optocoupler driving IR2111 chip, channel A is a driving signal of the upper arm, and channel B is a driving signal of the lower arm. It can be seen from Figure 10 that for a short period of time, the two driving signals are all low level, that is, the dead time is in this period, and the function of this time period is to ensure that the switching tubes of the upper and lower arms are not turned on at the same time.
This study is performed Fourier transform analysis on the output voltage waveform of the inverter circuit to obtain the phase, amplitude distribution map and Fourier analysis table of voltage harmonics at different frequencies, as shown in Figure 11. In Figure 11(a), it can be seen that the DC output voltage of the inverter is 0.00778453V and the total harmonic coefficient (THD) is 5.59376%. These two experimental data show that the filter design has a strong inhibitory effect on harmonics. It is greatly reduced the power pollution and improved the power quality. At the same time, it is also improved the stability, lifetime and efficiency of the use of electrical equipment. The distribution of harmonics is shown in Figure 11(b) and (c). The larger amplitude of each harmonic appears at the integral multiple of the fundamental frequency, and its amplitude increasing with frequency is gradually decreased. The amplitude after the ninth harmonic is almost close to zero, and the SPWM inverter is effectively suppressed the low-order harmonics. Therefore, in general, the voltage of low-order harmonic is minimal and is ignored [6].

Figure 11. Fourier analysis of output voltage for the inverter circuit.

Figure 12 is a diagram of the input and output power of the inverter. From the figure, the input and output power of the inverter designed in this paper is a zero-crossing linear relationship. In Figure 12, the inverter efficiency is about 96.5% on average. The data of these simulation results are shown that
the designed inverter has the characteristics of high photovoltaic conversion efficiency and strong output stability.

Figure 12. Input power versus inverter efficiency.

Figure 13 is shown the AC output voltage waveform for the inverter. The peak voltage of the sine wave for the inverter is 304V. The average voltage of the sine wave is about 215V, and the frequency is

\[ f = \frac{1}{2 \times 10.000 \text{ms}} \approx 50 \text{ Hz} \]

The value of the simulated voltage is smaller than the value of the ideal voltage. There is a certain impedance in the circuit that consumes energy. Since the electrical equipment is worked normally at 220±10V, the output error of the inverter designed in this paper is acceptable, and the inverter is suitable for popularization.

Figure 13. Output voltage waveform for the inverter.

4. Conclusion
The inverter is used the STM32 as the main controller to realize sinusoidal alternating current that converts PV DC into AC source. In Multisim simulation, the ripple coefficient is less than 0.1%, which largely avoids the generation of surge voltage and current, and greatly improves the efficiency of the inverter. Due to the harmonic, aging phenomena in cables insulation is accelerated, and the service life of the cable is shortened. The output is analyzed by Fourier to obtain a THD of 5.59%, which proves that the circuit has a strong suppression effect on these harmonics. The inverter conversion efficiency of this design is 96.5%, which is higher than 95% of the current market. Also, the two-stage conversion structure is adopted in this design to make the whole inverter have the advantages of simple structure, small volume, convenience-driven, and low cost. From the above, by introducing a protection circuit, the inverter is protected in time and effectively, improving safety and reliability.

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