Design and evaluation of hybrid SHE+STT-MTJ/CMOS full adder based on LIM architecture

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Abstract. This work aimed at developing a full adder using hybrid magnetic tunnel junction/complementary metal oxide semiconductor (MTJ/CMOS) based on the logic-in-memory architecture (LIM). LIM has emerged as the most promising alternative to the standard von-Neumann architecture in the impedance post-CMOS era. Performance of the hybrid full adder is evaluated in terms of power, delay, power delay product (PDP), and device count. These results are compared with the existing double pass transistor logic-based clocked CMOS (DPTL-C2MOS) full adder. Further, Monte-Carlo simulations on both variants of full adders were conducted to study their performance. Simulation results reveal that the hybrid full adder is superior to the DPTL-C2MOS full adder and can be used in low power and high throughput computing systems in the near future.

1. Introduction
Exponential growth in the field of artificial intelligence, big data, and 5G technology demand high throughput and low power computing system. Though standard von-Neumann architecture has been the workhorse in the computing system for the last few decades, it cannot meet future demands as it poses memory wall problems [1]. Simultaneously, scaling down the technology node to obtain high packing density in the integrated circuits (ICs) poses its own challenges, such as an increase in power dissipation. An increase in the power dissipation, especially in the standby mode, is due to the secondary effects that kick in the standard CMOS technology below 45nm technology [2]. Although the higher clock frequency has increased the operating speed, at the same time, it also increases the dynamic power dissipation of the CMOS ICs. As a combined effect, the heat production in the ICs has been reaching its thermal limit [3]. To tackle this worsening condition, many efforts have been put forth at the device as well as architectural level. Among all the possible solutions, logic-in-memory (LIM) at the architectural level and magnetic tunnel junction (MTJ) at the device level are the most prominent ones [4]. A computational capability is instilled into the memory of LIM. Here the memory stores the information as well as takes part in the computational process [5, 6]. By doing so, the memory

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wall problem that is being seen in the standard von-Neumann architecture is resolved. MTJ is the best suited for LIM, because to its supremacy such as infinite endurance, fast reading capability, non-volatility, high density, 3D integration with the existing CMOS technology [7]. Figure 1 shows the difference between standard von-Neumann architecture and hybrid MTJ/CMOS LIM structure. The hybrid MTJ/CMOS LIM not only avoids the unnecessary flow of data but also reduces the area due to the feasibility of 3D integration on top of the silicon. Most importantly, in LIM, due to non-volatile memory, we can completely switch off the un-utilized blocks without losing the information, and there is no need for a backup and restoration process either. The information stored in the non-volatile memory is readily available for processing as soon as the power is resorted. This saves a significant amount of power in the standby mode [8, 9].

The process of storing the information into the MTJ is called MTJ switching/writing. There are several mechanisms used for the MTJ writing, such as field-induced magnetic switching (FIMS), thermal assisted switching (TAS), spin transfer torque (STT), spin-Hall effect (SHE), voltage assisted switching (VAS) [2]. Though the STT switching mechanism is commercialized in many applications, it suffers from incubation delay due to stochasticity [10]. This lowers the operating speed of the STT-MTJ devices. One can overcome this issue by increasing the write current, but this affects the endurance of the STT-MTJ device by causing the dielectric breakdown over a period of time. These limitations are strongly overcome with the recently introduced SHE-assisted STT (SHE+STT) switching mechanism in a three-terminal MTJ [11]. Here the SHE assists in overcoming the incubation delay and not only speeds up the switching process but also increases the endurance of the MTJ device. Considering all these, in this paper a hybrid SHE+STT-MTJ/CMOS full adder (FA) based on LIM architecture has been developed. Simulations are carried out to study the performance of these hybrid circuits in terms of key performance indicators (KPI) such as output response, power dissipation, power delay product (PDP), and the number of devices utilized. Comparison of these KPIs with the CMOS counterpart, i.e., double pass transistor logic-based clocked CMOS (DPTL-C^2-MOS), is conducted. Monte-Carlo (MC) simulations on hybrid FA is also performed here, to study the power variations by incorporating process and mismatch variations in CMOS and extracted parameters of MTJ that would arise during the fabrication process.

![Figure 1](image-url)

**Figure 1.** (a) Schematic of von-Neumann architecture with logic and memory blocks. Here logic as well as memory blocks are placed separately, and their combined area is X+Y. Interconnects aid the communication between them. (b) 3D integration of MTJ with CMOS in LIM with their combined area as either X or Y [6].

2. Background

2.1. MTJ structure and its switching with SHE+STT mechanism

Figure 2 shows the three-terminal (T1, T2, and T3) structure of SHE+STT-MTJ. T1 is connected to the pinned layer (PL), whereas T2 and T3 are connected to the opposite end of heavy metal (HM). The free layer (FL) is separated from the PL by a thin oxide barrier layer (BL) and is placed in contact with the HM. The HM material possesses a high atomic number...
and converts a charge current into spin current due to high spin-orbit interaction (SOI), i.e., when an unpolarized charge current passes through the HM, due to SOI, electrons with opposite spins move in opposite directions thus generating a spin current in the HM. This effect is called SHE [12]. The relationship between spin current density ($\vec{J}_S$), charge current density ($\vec{J}_C$) and spin polarization ($\vec{\sigma}$) is given in Equation 1 as,

$$\vec{J}_S = \theta_{SH} (\vec{\sigma} \times \vec{J}_C).$$

Where $\theta_{SH}$ is the spin-Hall angle. The $\vec{\sigma}$, $\vec{J}_S$ and $\vec{J}_C$ are all mutually perpendicular to each other. Thus, the SHE generated assists the STT to switch the MTJ from anti-parallel (AP) to parallel (P) state or vice versa. When the MTJ is in AP state, it is considered to be at a high resistance state ($R_{AP}$); on the contrary, when it is in P state, the MTJ is assumed to be of low resistance ($R_{P}$). Figure 2(b) shows switching of MTJ from AP to P state, where a charge current, with density ($\vec{J}_{SHE}$) flow-through HM in the Y-direction and gets converted into the spin current, with density ($\vec{J}_S$) in Z-direction. This $\vec{J}_S$ exerts a torque known as SOT onto the FL’s magnetic orientation. Due to SOT, the orientation of the FL will be tilted from -Z-direction to X-direction. At this point, the MTJ is in a meta-stable state for a brief moment. Now the spin polarized electrons entering from the PL to FL in -Z-direction will exert an STT onto the FL’s magnetic orientation to change it from the X-direction to Z-direction. Hence MTJ switches from AP to P, with the combined effort of SHE and STT currents, and thus we call this switching as SHE-assisted STT switching mechanism. Similarly, switching the p-MTJ from P to AP (Figure 2(c)) can be understood.

**Figure 2.** (a) Three terminal SHE p-MTJ device structure. When PL and FL are pointing in the same direction then MTJ is in P state or else when PL and FL are pointing in opposite direction MTJ is in AP state. Using SHE+STT, MTJ switching take place from (b) AP to P with $J_{SHE}$ in Y- and $J_{STT}$ in -Z-direction. Whereas MTJ (c) P to AP switching take place with $J_{SHE}$ in Y- and $J_{STT}$ in Z-direction [2].
2.2. Logic-in-memory architecture

Block diagram of the hybrid MTJ/CMOS LIM architecture is shown in Figure 3. It consists of three main blocks: (a) sense amplifier (SA) [13], (b) logic network (LN) and (c) MTJ switching circuit [14]. SA detects the logic operations carried-out by the LN and produce OUT and OUT. The LN is a combination of the MOS logic structure and MTJs. Here the volatile inputs are applied to the MOS logic structure, on the contrary non-volatile data is stored in MTJs. MTJ switching/writing block will alter the MTJ resistance from $R_P$ to $R_{AP}$ (thereby its state) or vice versa using the SHE+STT switching mechanism. The amalgamation of MTJs with the MOS logic structure is possible due to their resistance compatibility, ON resistance of the MOS ($R_{ON}$) is less than $R_P$; ($R_{ON} < R_P$) and the OFF resistance of the MOS ($R_{OFF}$) is more than $R_{AP}$; ($R_{OFF} > R_{AP}$).

![Figure 3. LIM architecture with sense amplifier, logic network and MTJ writing circuit blocks [7].](image)

3. Design of hybrid full adder based on LIM

FA circuit is based on hybrid LIM architecture, and it consists of SUM (Figure 5(a)) and CARRY sub-circuit (Figure 5(b)). It produces output and its complement by accessing the differential current flow between the left and right arm. The inputs A and B are given to the MOS logic tree, whereas $C_{in}$ is stored in the MTJ pair (MTJ0-MTJ1). When the MTJ pair is in AP-P configuration, we assume bit “0” is stored; on the contrary, when the MTJ pair is in P-AP configuration, we assume bit “1” is stored. Hybrid FA circuit operates in two phases viz, pre-charge and evaluation phase. In the pre-charge phase, clock (CLK) = “0” and inputs A, B, and $C_{in}$ are applied to the circuit. In the evaluation phase, CLK = “1”, and during this period, processing of these inputs are conducted in the LN to produce the corresponding output and its complement. As discussed earlier, writing the information into the MTJ pair is conducted using the SHE+STT switching mechanism, and this takes place in the pre-charge phase so that this information is available for processing at the LN in the next evaluation phase.

SHE+STT-MTJ writing driver is divided into two parts; control circuitry (Figure 4(a)) and writing core (Figure 4(b)). Table 1 shows the various combinations of input, intermediate signals, and corresponding status of the MTJ pair. When EnW is at logic “0”, writing core is disabled by the intermediate signals (STTP, STTN, SHEP, SHEN = “1010”) of the control circuit, and no writing takes place. Information will be written only when EnW = “1”. When EnW, EnSHE, and Data are “111” respectively, intermediate signals STTP, STTN, SHEP, SHEN will be “1101” respectively. This will turn ON the transistors MP1, MP2, MP3, MN0, MN1, MN3. There are two types of current flowing in the circuit, i.e., SHE and STT current. SHE current path is; Vdda-MP1-MTJ0-MN1-gnd and Vdda-MP3-MTJ1-MN3-gnd. STT current path is; Vdda-MP2-MTJ1-MN3-gnd and Vdda-MP1-MTJ0-MN0-gnd. At this point, the MTJ pair is in a metastable state. After a brief period of time (200ps), EnSHE is made to “0”, forcing
Table 1. Various combinations of input as well as intermediate signals and the corresponding states of MTJs during SHE+STT writing mechanism.

| Input signals | Intermediate signals | MTJ status |
|---------------|----------------------|------------|
| EnW | EnSHE | Data | STTP | STTN | SHEP | SHEN | MTJ0 | MTJ1 |
| 0 | X | X | 1 | 0 | 1 | 0 | X | X |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | Metastable |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | AP-P | P-AP |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | Metastable |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | P-AP | AP-P |

*X represents don’t care condition

Figure 4. Schematic of SHE+STT-MTJ switching circuit consisting of (a) control circuit and (b) writing core [14].

STTP, STTN, SHEP, SHEN = “1100”. This will turn OFF the transistors MP3 and MN1 to stop the flow of SHE current. But STT current continues to flow in the circuit to change the MTJ0-MTJ1 configuration to P-AP, respectively. Similarly, Data “0” can be written into the MTJ pair by suitably changing the input signals, as shown in Table 1.

Working of the hybrid, FA is explained with an example, where ABC_in is set as “010”. In the pre-charge phase, when CLK= “0”, transistors P3 is ON and pull-down (PD) transistor, N3 is OFF. The OUT (SUM/CARRY) and OUT(SUM/CARRY) node voltages will be shared through P3 as a result that both OUT and OUT will be pre-charged to Vdd-Vth. In the evaluation phase, CLK = “1”, transistor N3 is ON, providing a path for both outputs OUT and OUT to gnd through LN. In the MOS logic tree of SUM sub-circuit, inputs A and B will turn ON the transistors M2, M4, M5, M7, whereas the rest of them are OFF. Input C_in will configure the MTJ0-MTJ1 as AP-P. Now there are two paths for the outputs (SUM and SUM) to discharge to ground, i.e., Path1 and Path2. The left-arm path (Path1) has a total resistance of two ON transistors (M5, M7) and one MTJ (MTJ1), and the right arm path (Path2) also has two ON transistors (M2, M4) and an MTJ (MTJ0). Since the MTJ0-MTJ1 are in AP-P
configuration, the total resistance of Path1 \((2R_{ON} + R_P)\) is less than the total resistance of Path2 \((2R_{ON} + R_{AP})\). Hence, though both output nodes start to discharge simultaneously, the discharge current in Path1 finds a less resistive path and discharges to gnd quicker than Path2. As a result, SUM is pulled down to the threshold voltage of P2 hence SUM raised to logic “1”. Whereas SUM continues to discharge and attains logic “0”. This produces SUM as “1” and SUM as “0”. Similarly working of the CARRY sub-circuit can be understood. Figure 6 shows the simulated hybrid FA waveform.

Figure 6. Waveforms of hybrid FA with SUM and CARRY outputs. The highlighted part shows a particular case, where input \(ABC_{in}\) are “010” and their corresponding outputs SUM and CARRY are “10”.

4. Results and discussion
Simulations are carried out with Cadence (IC6.1.7-64b.500.19) 45nm GPDK design kit with the SHE+STT model developed using Verilog-A language [15]. Table 2 shows the MTJ device
parameters set during simulation. Other parameters are maintained as the default values as mentioned in [15]. The writing core transistors are set with \( W = 480 \text{nm} \), whereas the rest of the transistors are set with default \( W = 120 \text{nm} \) and \( L = 45 \text{nm} \). A power supply of \( V_{\text{dda}} = 1.2 \text{V} \) is used for writing core to drive write current, whereas rest of the circuit operates with the power supply of \( V_{\text{dd}} = 1 \text{V} \).

### Table 2. SHE+STT-MTJ parameters set during the simulation [15].

| Parameter | Description                              | Unit | Default value |
|-----------|------------------------------------------|------|---------------|
| \( t_{sl} \) | Free layer thickness                     | nm   | 0.7           |
| \( t_{ox} \) | MgO barrier thickness                    | nm   | 0.85          |
| \( TMR \) | TMR ratio under zero bias voltage        | %    | 200           |
| Shape     | MTJ Surface shape                        |      | circle        |
| \( r \)   | MTJ Surface radius                       | nm   | 16            |
| \( w \)   | Heavy-metal width                        | nm   | 32            |
| \( d \)   | Heavy-metal thickness                    | nm   | 3             |
| \( l \)   | Heavy-metal length                       | nm   | 60            |
| \( \sigma_{TMR} \) | Standard deviation of TMR | % | 3% of \( TMR \) |
| \( \sigma_{t_{sl}} \) | Standard deviation of \( t_{sl} \) | nm | 3% of \( t_{sl} \) |
| \( \sigma_{t_{ox}} \) | Standard deviation of \( t_{ox} \) | nm | 3% of \( t_{ox} \) |

Comparison between hybrid FA and DPTL-C\(^2\)MOS FA in terms of power dissipation, delay, PDP, and device count is shown in Table 3. The dynamic and total power dissipation of hybrid FA is 97.86\% and 47.11\% less than DPTL-C\(^2\)MOS FA respectively. The static power dissipation of the hybrid FA is almost zero when compared to its DPTL-C\(^2\)MOS FA. This is because input \( (C_{in}) \) is stored in the MTJ pair, imparting non-volatility to the hybrid FA. So, in the standby mode, the power supply to the hybrid FA can be completely cut-off without a backup process for the \( C_{in} \) information. \( C_{in} \) information is readily available in the subsequent active mode, and there is no restore process either. However, there is steady-state power dissipation for hybrid FA, which is 2.81\% lesser than DPTL-C\(^2\)MOS FA.

### Table 3. Comparison of hybrid ALU with CMOS-ALU arithmetic operation @500 MHz.

| Particulars | DPTL-C\(^2\)MOS FA | Hybrid FA |
|-------------|---------------------|-----------|
| Static power(nW) | 712\(^a\) | 0\(^b\) (692\(^c\)) |
| Dynamic power(nW) | 621.5 | 13.28 |
| Total power(nW) | 1333.5\(^d\) | 705.3\(^d\) |
| Worst case delay(ps) | 82.17 | 94.94 |
| PDP(aJ) | 109.57 | 66.96 |
| Device count | 48 MOS | 32MOS+4MTJ |

Note: Write circuit is excluded while obtaining the above values.

\(^a\) Power supply can not be turned off in DPTL-C\(^2\)MOS FA, as it is volatile in nature.

\(^b\) In standby mode power is switched off in hybrid FA, as it is non-volatile in nature.

\(^c\) In the steady state condition, static power dissipation is observed.

\(^d\) Total power dissipation = dynamic + static power, in active mode.

A higher delay of 13.45\% is observed in hybrid FA than DPTL-C\(^2\)MOS FA. The delay of hybrid design is comparatively more than its CMOS counterpart; it is because of the dependency of discharge current on the width of N3 transistor (Figure 5). A large N3 transistor would assist to quickly discharge the differential current in the hybrid FA circuit and thereby alleviate the worst-case delay. This can be understood by looking at Figure 7, where the size of the N3...
transistor is varied and it is observed that there is a decrease in delay for the increase in the
N3 transistor size. However, as the N3 transistor size increases, there is an increase in the total
power dissipation also. Hence delay versus power trade-off needs to be balanced in the hybrid
FA circuit.

![Figure 7](image)

Figure 7. Power dissipation, delay and PDP dependency on N3 transistor’s size. As N3
transistor’s width increases, delay reduces, but the power dissipation increases, while PDP
decreases initially but later on increases.

In terms of transistor count, hybrid FA needs 32 MOS, whereas DPTL-C^2MOS FA requires
48 MOS. That means in hybrid FA, the transistor count is less by 33.33% than its CMOS
counterpart and helps to save the silicon area. Moreover, the MTJs of the hybrid FA can be
built on top of the silicon layer, thanks to the 3D integration capability of MTJs. Thus, the die
area for the hybrid FA is lesser as compared to the DPTL-C^2MOS FA.

Table 4. Total power dissipation of DPTL-C^2MOS FA versus hybrid FA with MC simulation
of 200 runs.

| Design type          | Min (nW) | Max (nW) | Mean (nW) | Standard deviation (nW) |
|----------------------|----------|----------|-----------|-------------------------|
| DPTL-C^2MOS FA       | 1195     | 1576     | 1315      | 74.85                   |
| Hybrid FA            | 668.75   | 763.3    | 712.25    | 15.62                   |

Further, MC simulation on DPTL-C^2MOS FA and hybrid FA circuits are conducted for 200
runs to study the process and mismatch variations that may affect its performance during the
nano-scale fabrication, and the total power variation is shown in Table 4. A 3% variations in
TMR, t_{sl} and t_{ox} which follow Gaussian distribution is included for MTJs during MC simulations.
It is observed that hybrid FA dissipates lesser power than DPTL-C^2MOS FA in all three cases,
i.e., min, max, and mean.

5. Conclusion
In this paper, a design and analysis of hybrid FA based on LIM architecture is presented. Due
to the use of SHE+STT-MTJs in the hybrid FA, the challenges posed by the STT-MTJs such
as lower writing speed, high write energy consumption, and risk of dielectric break down are
easily overcome in this design. Compared to the DPTL-C^2MOS FA, the hybrid FA dissipates
significantly lower power and PDP by using a lesser number of transistors. Lower power
dissipation in the hybrid FA is also supported by MC simulation. Moreover, due to the non-
volatility nature of hybrid FA, its static power dissipation in standby mode is almost zero.
So, this hybrid FA based in LIM architecture can be considered as an alternative to standard von-Neumann architecture in computing systems for various applications.

Appendix A. CMOS full adder using double pass transistor logic based clocked circuit

![CMOS full adder using double pass transistor logic based clocked circuit](image)

**Figure A1.** CMOS full adder based on double pass transistor logic based clocked circuit [16,17].

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