Synthesizing Power and Area Efficient Image Processing Pipelines on FPGAs using Customized Bit-widths

Vinamra Benara*, Sahithi Rampalli*, Ziaul Choudhury*, Suresh Purini*, Uday Bondhugula†
*Computer Systems Group
IIIT-Hyderabad
500032, India
†Indian Institute of Science
Dept of CSA
Bengaluru 560012, India
{vinamra.benara@research.iiit, sahithi.rv@students.iiit, ziaul.c@research.iiit, suresh.purini@iiit}.ac.in*, udayb@iisc.ac.in†

Abstract—High-level synthesis (HLS) has received significant attention in recent years, improving programmability for FPGAs. PolyMage is a domain-specific language (DSL) for image processing pipelines that also has a HLS backend to translate the input DSL into an equivalent circuit that can be synthesized on FPGAs, while leveraging an HLS suite. The data at each stage of a pipeline is stored using a fixed-point data type \((\alpha, \beta)\) where \(\alpha\) and \(\beta\) denote the number of integral and fractional bits. The power and area savings while performing arithmetic operations on fixed-point data type is known to be significant over using floating point.

In this paper, we first propose an interval-arithmetic based range analysis \((\alpha\text{-analysis})\) algorithm to estimate the number of bits required to store the integral part of the data at each stage of an image processing pipeline. The analysis algorithm uses the homogeneity of pixel signals at each stage to cluster them and perform a combined range analysis. Secondly, we propose a novel compilation framework in which any range analysis algorithm, be it interval or affine arithmetic, can be deployed with ease. Thirdly, for estimating fractional bit requirements \((\beta\text{-analysis})\), we propose a simple and practical heuristic search algorithm, which makes very few profile passes, as against techniques such as simulated annealing proposed in prior work. The analysis algorithm attempts to minimize the number of fractional bits required at each stage while respecting an application specific quality metric. We evaluated our bit-width analysis algorithms on four image processing benchmarks with regard to quality, power and area metrics. We show that with negligible loss in quality, we obtain up to a factor of 3.8× and 6.2× improvements in power and area respectively, when compared with using floating-point data type.

I. INTRODUCTION

Field-Programmable Gate Arrays (FPGAs) are suitable for accelerating computations from several domains. With respect to performance delivered per Watt, FPGAs are often expected to perform better than GPUs as accelerators. This is especially the case if the data involved in computations has limited range and precision requirements which can be exploited using fine-grained fixed-point data types on FPGAs. Such flexibility either does not exist when using other kinds of accelerators or is available in a very limited way.

There is significant interest in developing domain-specific languages (DSLs) to address productivity, performance, and portability issues in programming modern architectures. Often, a DSL’s goal is also to deliver high performance for multiple architectures from a single source that abstracts away implementation aspects including parallelism, memory allocation and management, and features of the architecture being targeted. Besides general-purpose multi-core CPUs and GPUs, FPGAs are thus an interesting architecture for a DSL compiler to target in a manner transparent to the programmer.

There have been several recent DSL efforts that target FPGAs for image processing pipelines; these include Dark-room [1], Rigel [2], and PolyMage-HLS [3]. While these works have addressed several challenges in compiling DSL to FPGAs, none of them have studied the complementary issue of exploiting application-dependent variable fixed-point data types for power and area savings. Our work can also be viewed as a specific approach in the approximate computing paradigm for the image processing domain, although we do not use any approximate arithmetic operations.

This paper leverages customized precision in a domain-specific context with FPGAs as the target architecture for an automatic compilation framework. We propose, implement, and evaluate our approach for PolyMage. With the PolyMage DSL, FPGAs are targeted by first generating High-Level Synthesis (HLS) code after a realization of several transformations for parallelization and reuse; the HLS code is subsequently processed by a vendor HLS suite (Xilinx Vivado in the case of PolyMage). We study the impact of leveraging the right amount of precision on four benchmarks, and thus study how FPGAs can be fully exploited through a DSL approach. The following are the main contributions of this paper.

1) An interval arithmetic-based approach for estimating...
the integral bit-widths required at various stages of an image processing pipeline: this approach exploits the fact that all pixel signals in each stage of a pipeline are homogeneous in nature.

2) A compilation framework in which any interval analysis technique, be it interval arithmetic or affine arithmetic, can be deployed with ease.

3) A profiling technique to improve the integral bit-width estimates obtained via static interval analysis.

4) The profiling technique is extended to estimate the fractional bits required by using application-specific quality metrics.

5) A thorough experimental analysis relating quality, power and area on four image processing benchmarks.

We demonstrate that dramatic improvement in power and area can be achieved while preserving output quality, and all of this automatically from a domain-specific language that works at a much higher level than HLS.

The rest of this paper is organized as follows. Related work is discussed in Section II and the necessary background is provided in Section III. The range analysis algorithm for integral bit-width estimation is presented in Section IV and the profile driven precision estimation algorithm is discussed in Section V. Experimental evaluation is presented in Section VI and conclusions are presented in Section VII.

II. RELATED WORK

Besides PolyMage [4], Rigel [2], Darkroom [1], HIPAcc [5], and Halide [6] are the other recent domain-specific languages (DSL) for image processing pipelines. Among them, PolyMage, Rigel, HIPAcc, and Darkroom compilers can generate hardware designs targeting FPGAs, and none of these currently optimize designs using bit-width analysis.

There are several works on bit-width estimation in digital signal processing applications using techniques based on interval arithmetic and affine arithmetic [7], [8], [9], [10], [11]. However, these techniques are not scalable and can only be applied to small circuits like low degree polynomial multiplications, 8x8 discrete cosine transform computation etc. which contain very few signals in the order of 10s and 100s. Whereas the techniques proposed in this paper exploits both the image processing domain and the PolyMage-HLS compilation framework to do interval analysis on large image processing pipelines wherein each pixel at every stage of the pipeline constitutes a signal.

Usually, range analysis (integer bits) and precision (fraction bits) analysis are performed separately. For precision analysis, there are search-based heuristics and constraint programming approaches deployed with the goal of minimizing circuit area while not violating the signal error constraint. In this work, we focus on a class of image processing applications that can be expressed as a directed acyclic graph of simple data parallel filters. Ours is the first extensive study on the application of practical interval and profile analyses for estimating integral and fractional bit-widths in image processing applications, and their impact on power and area savings.

Mahlke et al. [12] proposed a data flow analysis based approach for bit-width estimation of integral variables in the PICO (Program-in Chip-out) system for synthesizing hardware from loop nests specified in C. The integral bit-width analysis algorithm due to Budiu et al. [13] is similar to the previous work but uses a different data flow analysis formulation. Stephenson et al. [14] performs integer bit-width analysis through range propagation, again using the data flow analysis framework. Tong et al. [15] proposed the usage of variable bit-width floating-point units which can save power for many applications which does not require the full range and precision provided by the standard floating-point data type. Sampson et al. [16] proposed EnerJ, an extension to Java, which supports approximate data types and computation. However, fixed-point data types and the associated approximate operations are not considered in EnerJ. On the contrary, PolyMage DSL can be enhanced by using the approximate data types as proposed by EnerJ.

Approximate computing has a rich body of works [17], [18], [19]. However, our context of domain-specific automatic HLS compilation is unique. Depending on output quality and the application in question, our approach could either be seen as exploiting customized precision or leveraging approximate computing. In addition to customized precision, we can potentially use approximate arithmetic operations [20], [21] in various stages of computation.

III. BACKGROUND

In this section, we present background on PolyMage DSL and PolyMage-HLS compiler. Then we provide the basics of interval and affine arithmetic analysis necessary to understand the proposed range analysis algorithms in this paper.

A. PolyMage

PolyMage [4] is a domain-specific language and compiler for image processing pipelines, and is available open-source [22]. Listing 1 is an example of a PolyMage DSL program for an image processing algorithm called Unsharp Mask (USM). Figure 1 shows the USM DAG and the sharpened version of the image when USM is applied to it. This class of computations can be expressed as a directed acyclic graph of nodes where each node typically performs a simple data parallel operation on all image pixels. Upsampling, downsampling, convolutions, stencil operations, and reductions are some examples. The entire computation can thus be seen as a composition of these simple kernels, which we refer to as stages or filters.
Computation at the boundaries: this allows producer-consumer level to extract parallelism by performing redundant computation while maximizing data reuse: data parallelism, that exploits various kinds of parallelism available in the HLS compiler and Xilinx Vivado tool chain.

The PolyMage-HLS compiler generates a hardware design expressed in a Hardware Description Language (HDL) such as VHDL or Verilog. Figure 2 shows the entire design flow using the PolyMage-HLS compiler infrastructure, when it was first proposed [4], comprised a optimizing source-to-source translator that generated OpenMP C++ code from an input PolyMage DSL program. Chugh et al. [3] developed an translator that generated OpenMP C++ code from an input PolyMage DSL code for Unsharp Mask.

Listing 1: PolyMage DSL code for Unsharp Mask

```
# PolyMage DSL code for Unsharp Mask

# Params
R = Parameter(Int, "R")
C = Parameter(Int, "C")
thresh = Parameter(Float, "thresh")
weight = Parameter(Float, "weight")

# Vars
x = Variable(Int, "x")
y = Variable(Int, "y")
c = Variable(Int, "c")

# Input Image
img = Image(Float, "input", [3, R+4, C+4])

# Intervals
xrow = Interval(Int, 2, R+1, 1)
xcol = Interval(Int, 0, C+3, 1)
yrow = Interval(Int, 2, R+1, 1)
ycol = Interval(Int, 0, 2, 1)

# Pipeline
blurx = Function([c, x, y], [cr, xrow, xcol], Float, "blurx")
blurx.defn = [ Stencil(img(c, x, y), 1.0/16, 
               [[1, 4, 6, 4, 1]]) ]

blury = Function([c, x, y], [cr, yrow, ycol], Float, "blury")
blury.defn = [ Stencil(blury(c, x, y), 1.0/16, 
                      [[1, 4, 6, 4, 1]]) ]

sharpen = Function([c, x, y], [cr, yrow, ycol], Float, "sharpen")
sharpen.defn = [ img(c, x, y) * ( 1 + weight ) \ + blury(c, x, y) * (-weight) ]

masked = Function([c, x, y], [cr, yrow, ycol], Float, "mask")
masked.defn = [ Select(Condition(absv, "<", thresh), 
                      img(c, x, y), 
                      sharpen(c, x, y) ) ]
```

C. Interval and Affine Arithmetic

With interval analysis, one estimates the range of an output signal \( z \leftarrow f(x, y) \) based on the range of the input signals \( x \) and \( y \), and the function \( f \). For example, if the range of \( x \) and \( y \) are \([x, \bar{x}]\) and \([y, \bar{y}]\) respectively, and \( z \leftarrow x + y \), then the range of \( z \) is \([x + y, \bar{x} + \bar{y}]\). Such range estimation functions have to be defined for different operations that are applied iteratively to obtain the ranges of different intermediate and output signals involved in the computation. Although interval arithmetic is simple and easy to use in to practice, it suffers from the problem of range over-estimation. For example, if the range of a signal \( x \) is \([5, 10]\), then the interval arithmetic estimates the range of the expression \( x \times x \) as \([-5, 5]\) whereas the actual range is \([0, 0]\). This is due to the fact that the interval arithmetic ignores the correlation between the operand signals if there is any.

With affine arithmetic analysis, a signal \( x \) is represented in an affine form as \( x = x_0 + \sum_{i=1}^{n} x_i e_i \) where \( e_i \in [-1, 1] \) are interpreted as independent noise signals and their respective coefficients \( x_i \)'s are treated as the weights associated with them. The interval of the signal \( x \) from its affine form can be inferred as \([x - r, x + r]\) where \( r = \sum_{i=1}^{n} \ |x_i| \). The addition and subtraction operations on two input signals is defined as \( z = x \pm y = (x_0 \pm y_0) + \sum_{i=1}^{n} (x_i \pm y_i) e_i \) and yields the resulting...
signal in its affine form. The correlation between the signals \( x \) and \( y \) is captured by sharing the independent noise signals \( \xi_i, 1 \leq i \leq n \) in their affine forms either partially or totally. Now, when we perform a computation \( x - y \) by considering the signal \( x \) in its affine form, the resulting range will be zero as against the over-estimated range which we get in interval arithmetic analysis. Thus the techniques based on affine arithmetic arrive at better bounds when compared with interval analysis techniques by taking into account cancellation effects in computations involving correlated signals. However, note that if the operation is multiplication, then the resulting signal contains quadratic terms and hence has to be approximated to an affine form. A detailed discussion on affine arithmetic analysis is beyond the scope of this paper and we recommend the reader to Stolfi and Figueiredo [7] for the same.

### IV. Bit-width Analysis

In this section, we first present an interval arithmetic based range analysis algorithm (refer Section IV-B) and followed by that a compilation framework in which any kind of range analysis algorithm can be easily deployed (refer Section IV-C).

When an image processing pipeline such as Harris Corner Detection (HCD) (cf. Figure 3), is implemented on a CPU or a GPU, a programmer is bound to choose a predefined data type such as float, int, or short owing to the underlying architectural constraints. In order to avoid arithmetic overflow errors, the data types have to be chosen conservatively by over-estimation. This leads to unnecessary wastage of memory, thereby memory bandwidth, and the resulting power consumed both due to data transfer and unnecessary extra precision arithmetic performed. However, in FPGAs, it is possible for us to use custom precision for data produced and consumed at various stages of an image processing pipeline. This saves chip area and the power consumed by the hardware design on the FPGA due to the reduced precision arithmetic and internal routing logic. The other natural outcome is the optimal utilization of the available memory resources.

#### A. Variable Width Fixed-Point Data Types

A fixed-point data type is specified by a tuple \((\alpha, \beta)\) where \(\alpha\) and \(\beta\) denote the number of bits allocated for representing the integral and fractional parts respectively. The total bit-width of the data type is \(\alpha + \beta\). The decimal value associated with a fixed-point binary number \(x = b_{\alpha-1} \ldots b_0.b_{-1} \ldots b_{-\beta}\) depends on whether it is interpreted as an unsigned integer or a two’s complement signed integer, and is given as follows:

\[
\text{value}(x) = \begin{cases} 
\sum_{i=\beta}^{\alpha-1} b_i & \text{unsigned} \\
-2^{\alpha-1} b_{\alpha-1} + \sum_{i=\beta}^{\alpha-2} 2^i b_i & \text{2’s complement.}
\end{cases}
\]

This gives us the ranges \([0, 2^\alpha - 2^{-\beta}]\) and \([-2^{\alpha-1}, 2^{\alpha-1} - 2^{-\beta}]\) for unsigned and signed fixed-point numbers respectively. The parameter \(\alpha\) gives the range of values that can be represented and the parameter \(\beta\) indicates that the values in the range can be represented at a resolution of \(2^{-\beta}\). Hence, the range and precision can be improved, by increasing \(\alpha\) and \(\beta\) respectively. In this paper, we overload the term precision to also mean the entire data type \((\alpha, \beta)\), and this can be disambiguated based on context.

Fixed-point data types are useful in image processing applications where the range of values produced during computations is usually limited and the precision requirements are less demanding when compared to many other numerical algorithms. The data type (range and precision) requirement at a stage depends on the input data type and the nature of local computations carried out at that particular stage. Further, overflows during computations can be addressed by using saturation mode arithmetic instead of the conventional wrap around arithmetic operations performed in CPUs and GPUs. This feature is particularly useful in handling image processing pipelines using the approximate computing paradigm. The complexity of arithmetic operations on fixed-point data type \((\alpha, \beta)\) is very similar to that of integer operations on bit-width \(\alpha + \beta\). This results in substantial power and area savings when compared with floating-point computations as demonstrated in this paper.

#### B. Range (\(\alpha\)) Analysis Algorithm

The number of integer bits required at a stage \(I\) denoted as \(\alpha_I\) is a direct function of the bit-width of the input data and the operations it performs on them. The input data here refers to the data supplied to the stage by its predecessor stages in the DAG. Further, the computations on the pixel signals at each stage of DAG are identical and hence their

![Figure 2: PolyMage high-level compilation for FPGAs.](image-url)
corresponding ranges would be the same. This information is implicitly provided by a PolyMage DSL program and is hard to elicit from C like programs. We use this insight to group all the pixel signals at a stage and perform a combined range analysis using interval arithmetic. If the range of the data produced at a stage is $[x, \bar{x}]$, then the number of integral bits $\alpha_t$ required to store the data without overflow is as follows:

$$\alpha = \begin{cases} \max(\lceil \log_2(\lceil |x| \rceil) \rceil, \lceil \log_2(\lceil |\bar{x}| \rceil + 1) \rceil) + 1 & \text{if } x < 0 \\ \lceil \log_2(\lceil |\bar{x}| \rceil + 1) \rceil & \text{otherwise} \end{cases}$$

The number of fractional bits $\beta_t$ required at a stage depends on the application-specific error tolerance or quality metric, and we propose a profile-driven estimation technique in Section [V].

The range analysis algorithm iterates over the stages of a DAG in a topologically sorted order. At each stage, an equivalent expression tree for the computations (point-wise or stencil) is built. Then the range of the pixel signals is estimated by recursively performing interval arithmetic on the expression tree. Algorithm [I] shows the complete description of the bit-width estimation algorithm applied at each stage of the DAG computation. We do not show how an expression such as $x^n$, where $n$ is a compile-time constant, is handled in Algorithm [I] for the sake of simplicity. The interval arithmetic for exponentiation operation, $[x, \bar{x}]^n$, is

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**Algorithm 1** Integral bit-width analysis algorithm applied at each stage of the DAG in topological sorted order.

1: **procedure** COMPUTEBITWIDTH($e$)  
2: \hspace{1em} if $e \cdot data == $ leaf_operand then  
3: \hspace{2em} return $e \cdot bitwidth$  
4: \hspace{1em} else  
5: \hspace{2em} $op \leftarrow e \cdot operator$  
6: \hspace{2em} ($\bar{x}, \bar{\bar{x}}, \alpha_1$) $\leftarrow$ COMPUTEBITWIDTH($e \cdot left$)  
7: \hspace{2em} ($\bar{y}, \bar{\bar{y}}, \alpha_2$) $\leftarrow$ COMPUTEBITWIDTH($e \cdot right$)  
8: \hspace{1em} switch ($op$) do  
9: \hspace{2em} case $+$ : $[z, \bar{z}] \leftarrow [x + y, \bar{x} + \bar{y}]$  
10: \hspace{2em} case $-$ : $[z, \bar{z}] \leftarrow [x - y, \bar{x} - \bar{y}]$  
11: \hspace{2em} case $\ast$ : $[z, \bar{z}] \leftarrow \left[\min([x, \bar{x}], [y, \bar{y}]), \max([x, \bar{x}], [y, \bar{y}])\right]$  
12: \hspace{2em} case $/$ : if $0 \notin [y, \bar{y}]$ then $[z, \bar{z}] = [x, \bar{x}] \cdot [1/y, 1/\bar{y}]$ else $[z, \bar{z}] = [-\infty, +\infty]$  
13: \hspace{2em} end switch  
14: \hspace{2em} $\alpha_t \leftarrow \begin{cases} \max(\lceil \log_2(\lceil |x| \rceil) \rceil, \lceil \log_2(\lceil |\bar{x}| \rceil + 1) \rceil) + 1 & \text{if } x < 0 \\ \lceil \log_2(\lceil |\bar{x}| \rceil + 1) \rceil & \text{otherwise} \end{cases}$  
15: \hspace{2em} return $(z, \bar{z}, \alpha_t)$  
16: \hspace{1em} end if  
17: **end procedure**

**Figure 3:** DAG representation of the Harris Corner Detection algorithm.

**Table I:** Summary of computations in HCD program.

| Stage | Input Stages | Computation |
|-------|--------------|-------------|
| $I_x$ | $\text{img}$ | $\left[ \begin{array}{c} -2 \\ 0 \\ 1 \end{array} \right]$ |
| $I_y$ | $\text{img}$ | $\left[ \begin{array}{c} 1 \\ -2 \\ 0 \end{array} \right]$ |
| $I_{ax}$ | $I_x$ | $I_x(i,j)I_x'(i,j)$ |
| $I_{ay}$ | $I_y$ | $I_y(i,j)I_y'(i,j)$ |
| $I_{xy}$ | $I_x$, $I_y$ | $I_x(i,j)I_y'(i,j)$ |
| $S_{ax}$ | $S_{ax}$ | $A = \left[ \begin{array}{c} 1 \\ 1 \\ 1 \end{array} \right]$ |
| $S_{ay}$ | $S_{ay}$ | $A = \left[ \begin{array}{c} 1 \\ 1 \\ 1 \end{array} \right]$ |
| $S_{xy}$ | $S_{ax}$, $S_{ay}$ | $S_{xy}(i,j)S_{xy}'(i,j) - S_{xy}(i,j)S_{xy}'(i,j)$ |
| $\text{trace}$ | $S_{ax}$, $S_{ay}$ | $S_{xy}(i,j) + S_{xy}'(i,j)$ |
| $\text{Harris}$ | $\text{det}$, $\text{trace}$ | $\text{det}(i,j) - 0.04\text{trace}(i,j)\text{trace}(i,j)$ |
defined as follows.

\[
[z, z'] = \begin{cases} 
[x^n, x'^n] & \text{if } x \geq 0 \\
[x^n, x'^n] & \text{if } x < 0 \\
\{0, \max\{x^n, x'^n\}\} & \text{otherwise}
\end{cases}
\]

Our compiler maps simple expressions such as \(x \times x\) into \(x^2\) as this results in better range estimates. For example, if the range of a signal \(x\) is \([-2, 2]\), then \(x \times x = [-2, 2] \times [-2, 2] = [-4, 4]\), whereas \(x^2 = [-2, 2]^2 = [0, 4]\).

| Stage       | Range          | \(\alpha\) |
|-------------|----------------|-------------|
| Img         | [0, 255]       | 8           |
| \(I_x, I_y\)| \([-85, 85]\)   | 8           |
| \(I_{xy}\)  | \([-85^2, 85^2]\) | 14          |
| \(S_{xx}, S_{xy}\)| \([0.9 \times 85^2]\) | 16          |
| det         | \([-9 \times 85^2, 9 \times 85^2]\) | 17          |
| trace       | \([0.2, 9 \times 85^2]\) | 17          |
| harris      | \([-1.16 \times 9 \times 85^2, 9 \times 85^2]\) | 34          |

Figure 3 shows the DAG corresponding to the HCD benchmark. For the sake of simplicity, instead of showing the PolyMage program, we summarized the computations at each stage in Table I. The range associated with each pixel of input image is \([0, 255]\) as it is an 8-bit image. The required integral bit-width \(\alpha_{img}\) at this stage is 8. Stages \(I_x\) and \(I_y\) compute the derivative of the image along \(x\) and \(y\) axes respectively. The specific 3x3 stencil operations performed by these stages can be noted from the Table I. The stencil operation here can be expanded in the form of an expression as explained before. If the data type corresponds to interval arithmetic cannot be applied on the DSL level programs in the same fashion. In this section, we show how any kind of range analysis technique can be deployed with ease in the PolyMage compilation framework.

Recall that the PolyMage-HLS compiler translates a DSL program into C++ code which the Xilinx Vivado HLS compiler synthesizes into an equivalent circuit for a target FPGA. For example, Listing 2 depicts the code generated corresponding to a PolyMage program which applies a Sobel-x filter on an input image. The generated C++ program can be run in a purely simulation mode after compilation on any processor by providing test input images as stimuli. It can be noted from the Listing [2] that the data type of the stream, line and window buffers are parameterized by the type \(\text{typ}\). It can be a float or any fixed-point data type \((\alpha, \beta)\). During the hardware synthesis or in the simulation mode, using the C++ polymorphism feature, corresponding libraries for the arithmetic operations will be invoked based on the operand types. Now, the parameter \(\text{typ}\) can also be set to an interval type which is defined in a suitably chosen interval analysis library. If the generated C++ program contains a statement \(x = y + z\), then depending on the type of the variables \(x, y\) and \(z\) (like float, ia-type, aa-type etc.), appropriate addition operation will be invoked. For example, in order to perform affine arithmetic analysis on the Sobel-x program, using the Yet Another Library for Affine Arithmetic (YalAA) [25], all we have to do is to define the parameter \(\text{typ}\) appropriately as depicted in Listing 3.

When we run the generated C++ program with this data type definition, the value associated with each pixel in each stage of the pipeline DAG is its affine signal value which contains the base signal and the coefficients for the noise variables. From this the range of every pixel can be derived as explained before. If the data type corresponds to interval arithmetic, then the value associated with each pixel is an interval. Using this approach, any kind of interval analysis technique can be deployed in the PolyMage-HLS compiler trivially.

In the next section, we show that the integral bit-width requirements at various stages could be smaller than the estimates obtained through static analysis. This could be due to the nature of the input images and/or certain correlation between computations on spatially proximal pixels. Furthermore, we show how we can use simple binary search to compute the required fractional bits via program.
#include <hls_stream.h>
#include <malloc.h>
#include <cmath>
#include <arith.h>

void sobel_x(hls::stream<typ> & img, hls::stream<typ> & sobel_x_out)
{
    const int _ct0 = (2 + R);
    const int _ct1 = (2 + C);
    hls::stream<typ> Ix_out_stream;
    hls::stream<typ> img_Iy_stream;
    typ Ix_img_LBuffer[3][_ct1];
    typ Ix_img_WBuffer[3][3];
    typ Ix_img_Coeff[3][3];
    /* Code for the Sobel-x stage follows */
}

Listing 2: Auto-generated restructured HLS code for Sobel-x.

Listing 3: Type definitions for Affine and Interval Analysis.

Listing 3 Type definitions for Affine and Interval Analysis.

profiling using an application-specific error metric. In these estimations of integral and fractional bit-width, we can also exploit the fact that many image processing applications are resilient to small arithmetic overflow/precision errors, to arrive at power and area-efficient hardware designs by using practical estimates for data range and precision.

V. PROFILE-DRIVEN ANALYSIS

Profile-driven analysis can be used to accomplish two tasks. First, the worst-case integral bit-width lengths at various stages obtained via static analysis can be improved. Second, the fractional bits required at each stage can be estimated using an application-specific quality metric. However, the bit-width requirements estimated at each stage using profiling technique naturally depends on the sample input images. Based on the analysis done by Antonio Torralba et al. [26], we hypothesize that the images taken from a certain domain, like for example nature, has similar properties, and hence the bit-width estimates can be carried over to other images drawn from the same domain.

A. Integral Bits

The number of integral bits required at a stage \(i\) denoted as \(\alpha_i\) can be obtained by running the input PolyMage program on a sample distribution of input images. Let \(\alpha_i^s\) be the maximum number of bits required by stage \(i\) to represent a pixel from an image sample \(s\). Then the average number of bits \(\alpha_i^{avg}\) required based on a sample set \(S = \sum_{s \in S} \alpha_i^s / |S|\). Similarly, the worst-case number of bits \(\alpha_i^{max}\) required is \(\max_{s \in S} \alpha_i^s\). We can either use \(\alpha_i^{avg}\) or \(\alpha_i^{max}\) as estimates for \(\alpha_i\). Even if the estimate does not suit certain images, in many application contexts, using saturation mode arithmetic results in satisfying the desired output quality metric. Let \(\alpha_i^{as}\) be the integral bit-width estimation obtained for stage \(i\) through static analysis. For the benchmark programs we have considered, affine arithmetic analysis is not giving any better range estimates when compared with interval analysis. Hence, throughout the rest of the paper, when we refer to static analysis it means interval analysis only.

For our experimentation, we used a subset of 200 randomly chosen images from the Oxford Buildings dataset [27] consisting of 5062 images. The set of 200 images is partitioned into two equal halves: training and test sets. The training set is used to obtain estimates of integral bit-widths at various stages through profiling. The test set is used to evaluate the effectiveness of the bit-width estimates obtained for quality and power. Figure 4 shows the average cumulative distribution of the bit-width required by the integral part of the pixels in various stages of the HCD program on the training data set. Each graph corresponds to a stage of HCD with x-axis representing bit-width requirement of the integral part, and y-axis representing the percentage of pixels, averaged across test images, that can be represented
within a given bit-width. Figure 5a shows the cumulative distribution curve corresponding to stage $I_x$. It can be inferred that 95% of the pixels require less than 5 bits, and all pixels (100%) can be represented using 8 bits. Since stages $I_x$ and $I_y$ are of similar computational nature, we plot the histogram for only $I_x$. Similarly, among $I_{xx}$, $I_{yy}$ and $I_{xy}$, we plot for $I_{xy}$ in Figure 5b and from stages $S_{xx}$, $S_{yy}$ and $S_{xy}$, we plot for $S_{xy}$ in Figure 5c. Figures 5d, 5e and 5f correspond to $I_{det}$, $I_{trace}$ and $Harris$ stages respectively. Table IV shows the bit-width estimates obtained from static and profile-driven analyses. As can be noted from Table IV the bit-width estimates from $\alpha^{\text{max}}$ and $\alpha^{\text{avg}}$ measures are the same for all stages except for the $det$ stage. The estimates from the static analysis match the profile estimates except for the $det$, $trace$ and $Harris$ stages. In general, we expect the profile estimates to be better for stages that occur deeper in the pipeline. Note that the profile estimates also indicate the limit to which the static analysis techniques can be improved by using more powerful approaches. Profile information can be easily obtained by executing the HLS C++ program directly without the need for a heavy weight circuit simulation.

B. Fractional Bits ($\beta$) Analysis

The number of fractional bits $\beta_i$ required at a stage $i$ depends on the application and cannot be estimated in an application independent way as is the case with the integral bits analysis. Estimating the optimal number of fractional bits at each stage for a given application metric turns out to be a non-convex optimization problem in most cases and hence we propose a simple heuristic search technique that requires very few profile passes.

In the profiling technique, we fix the number of integral bits required at each stage based on static or profile-driven analysis and increase the precision $\beta$ uniformly across all the stages. For each value $\beta$, we estimate the application-specific error metric. For the HCD benchmark, the error metric is the percentage of mis-classified corners when compared to a design which uses sufficiently long integral and fractional bits. We can reach an optimal $\beta$ for a given error tolerance via binary search. Then we make a single pass on the stages of the DAG in reverse topologically sorted order. At each stage $I$, we do a binary search on the number of fractional bits required, $\beta_I$, starting from the initial estimate $\beta$ while retaining the application specific quality requirement. Figure 4 summarizes the proposed bitwidth analysis framework.

VI. EXPERIMENTAL RESULTS

In this section, we present a detailed area, power and throughput analysis when variable fixed-point data types are used as against floating-point by considering the following four benchmarks: Harris Corner Detection, Unsharp Mask, Down and Up Sampling, and Optical Flow. Tables IV, V, VIII and IX shows the integral bit-width estimates obtained by static analysis ($\alpha^{\text{avg}}$) and profile analysis ($\alpha^{\text{max}}$ and...
and the fractional bit-width estimates after iteratively dropping the bits by visiting the DAG stages in reverse topological order. Tables III, VI, VII, X compares the performance of three alternate designs using the data types float, $\alpha^{\text{int}}$ and $\alpha^{\text{max}}$. In these tables, the Quality column corresponds to an application specific quality metric, the Power column gives the power when the design operates at a speed specified in the adjacent Clk Period column; latency columns gives the number of clock cycles required to process an HD image; the next four columns (BRAM, DSP, FF, LUT, %slices) summarizes the area usage; the Min Clk Period column gives the maximum frequency of operation for circuit; the next two columns give the throughput and power consumed at the maximum frequency of operation. Figure 8 gives the split of power usage by various components of an FPGA.

We used Xilinx Zedboard consisting of Zynq-XC7Z020 FPGA device and Xilinx Vivado Design Suite 2017.2 version to conduct our experiments. The HLS design generated by our PolyMage DSL compiler is synthesized by the Vivado HLS compiler. All characteristics are reported post Place and Route. We ran C-RTL co-simulations to generate switching activity (SAIF) file for reporting detailed power consumption across the design.

A. Harris Corner Detection

Figure 6 shows the average percentage of pixels correctly classified by the HCD program on the test image set by varying the fractional bits uniformly across all the stages while fixing the integral bit-width estimates obtained via profiling ($\alpha^{\text{avg}}$). It also contains estimates of power consumption with varying fractional bits for the Xilinx ZED FPGA board. It can be noted from the graph that the fractional bits do not affect the accuracy of corner classification, and we thus get more than 99% accuracy even with zero fractional bits. From this graph, we infer that one can obtain close to 100% accuracy by using 8 fractional bits uniformly across all the stages. We then make a backward pass on the stages of the HCD program to drop the fractional bits further without any significant loss in accuracy and the column corresponding to $\beta^{\text{avg}}$ in Table I shows the final fractional bitwidths. Due to space constraint, we do not provide a graph such as Figure 6 for the rest of the benchmarks.

We can notice from Table III that by using bit-width estimates from static analysis, we obtain 99.999% accuracy with a power consumption of 0.263 W. The power savings are $3.8 \times$ lower when compared with the floating-point design. The savings on the percentage of FPGA slices used is around $6.2 \times$. From the last 3 columns of the table, we can notice that the fixed-point designs can operate at a higher frequency achieving better throughput while consuming lesser power.

![Figure 6: Error and power variation for the HCD program by fixing the number of integral bits to profile estimated values $\alpha^{\text{avg}}$ and varying $\beta$ uniformly across all the stages.](image)

B. Unsharp Mask (USM)

The Unsharp Mask (USM) benchmark sharpens an image as depicted in Figure 4. Listing 1 shows the PolyMage DSL code for USM. The input image is blurred across x-axis and y-axis by the stencil stages blurx and blury successively. Then it passes through the sharpen stage, which is a point-wise computation. Finally, the masked stage compares each pixel from the output of the sharpen stage with a threshold value. Depending on whether the pixel value is less than threshold, the corresponding pixel from either the original input image or the sharpened image is chosen for output. We highlight an important observation here: even if we make an error in computing a pixel value from the sharpen stage, as long as it is less than the threshold, the right output pixel is chosen. Based on this observation, we define an error metric that is the fraction of pixels that were misclassified in the masked stage due to variable width fixed-point representation as against floating-point representation. We define a second quality metric that is the root mean squared error between correctly classified pixel values and their floating-point counterparts.

We use the same training and test image set as that of the HCD benchmark. Table IV shows the integral and fractional bit-widths required at various stages of the USM benchmark obtained from static and profiled analysis. It can be noted that the estimates obtained by the static and profiling analyses are the same. Table VII shows that there is a factor of $1.6 \times$ improvement in power when compared to the floating-point design with negligible root mean squared error and classification error. With respect to the number of FPGA slices used, there is a factor of $2.6 \times$ improvement. Table VII also shows the maximum frequency of operation for each of the designs, the throughput at that level and power consumption. From the last 3 columns of the table, we can infer that by operating the fixed-point design at a higher frequency, 6% increase in throughput can be achieved.
Table III: Quality, post place and route power, area and throughput metrics for the HCD program using float and, bit-widths estimated using static analysis and profiling techniques. The fractional bits used are from Table IV.

| Analysis   | Quality (%) | Power (watts) | Clk Period (ns) | Latency (Million) | BRAM  | DSP  | FF  | Zedboard FPGA slices used(%) | Min. Clk Period (ns) | Max. Throughput (MPsps/sec) | Power (watts) |
|------------|-------------|---------------|-----------------|-------------------|-------|------|-----|-------------------------------|---------------------|-------------------------------|---------------|
| Float      | 99.999      | 0.970         | 5.5             | 2.06              | 32    | 113  | 18420| 22961                        | 33.01               | 5.24                          | 190           |
| $\alpha^{\text{avg}}$ | 99.999      | 0.263         | 5.5             | 2.06              | 14    | 12   | 2902 | 2724                         | 5.35                | 4.76                          | 210           |
| $\alpha^\text{min}$ | 99.999      | 0.253         | 5.5             | 2.06              | 14    | 12   | 2848 | 2727                         | 5.32                | 4.68                          | 214           |

Table IV: Comparison of bit-width estimates using profiling technique and static analysis for the HCD program.

| Stage   | $\alpha^{\text{est}}$ | $\alpha^{\text{max}}$ | $\alpha^{\text{avg}}$ | $\beta^{\text{avg}}$ |
|---------|-----------------------|------------------------|------------------------|-----------------------|
| Img     | 8                     | 8                      | 8                      | 8                     |
| $I_x$   | 8                     | 8                      | 5                      |                       |
| $I_y$   | 13                    | 13                     | 4                      |                       |
| $S_{xy}$| 14                    | 14                     | 4                      |                       |
| $S_{xy}$| 17                    | 17                     | 3                      |                       |
| $S_{xy}$| 16                    | 16                     | 3                      |                       |
| det     | 33                    | 30                     | 29                     | 1                     |
| trace   | 17                    | 17                     | 1                      |                       |
| harris  | 34                    | 29                     | 29                     | 1                     |

Table V: Comparison of bit-width estimates using profiling technique and static analysis for the USM benchmark.

| Stage | $\alpha^{\text{est}}$ | $\alpha^{\text{max}}$ | $\alpha^{\text{avg}}$ | $\beta^{\text{avg}}$ |
|-------|-----------------------|------------------------|------------------------|-----------------------|
| Img   | 8                     | 8                      | 8                      | 0                     |
| blur$_x$ | 8                     | 8                      | 8                      | 2                     |
| blur$_y$ | 8                     | 8                      | 8                      | 3                     |
| sharpen | 10                    | 10                     | 10                     | 4                     |
| mask  | 9                     | 9                      | 9                      | 4                     |

while consuming 1.7x lower power.

C. Down and Up Sampling (DUS)

Down and Up Sampling (DUS) benchmark has a linear DAG structure as shown in Figure 7. The image is first downsampled along the $x$-axis in stage $D_x$ and is further downsampled along the $y$-axis in stage $D_y$. It is then upsampled again along the $x$ and $y$ axes in the stages $U_x$ and $U_y$ respectively. For the sake of conciseness, we avoid including the DUS PolyMage code. All four stages comprise stencil computations.

The integral bit-width estimated by the static analysis algorithm is equal to 8 at all the stages of DUS. We use the same set of training images as that of HCD benchmark for estimating the integral and fractional bit-width via profiling. The profile estimates yielded the same integral bit-width requirement of 8 at all the stages. We use Peak Signal to Noise Ratio (PSNR) as a quality metric where the reference image obtained by using a sufficiently wide data type. We set the required PSNR to infinity for which our analyser tuned the fractional bit width shown in Table VIII Table VII shows that there is a factor of 1.7x reduction in power using tuned fixed-point data types when compared with using floating-point data type without loss of any accuracy. With respect to area, there is a 4× improvement in terms of number of slices used. Also, the fixed-point designs use no DSP blocks at all when compared with floating-point design which uses 54 DSPs. At the peak possible frequency of operation, fixed-point design achieves 13.6% increase in throughput while consuming 1.6x lesser power.

D. Optical Flow

The Optical Flow (OF) benchmark computes the velocity of individual pixels from an image frame and its time-shifted version. Our implementation is based on the Horn-Schunck algorithm [28] and consists of 30 stages. The first 10 stages are pre-processing stages and the last 20 stages are obtained by repeating a set of five stages four times. The accuracy of motion estimation can be improved by repeating the 5-stage set more times. Optical flow is a heavily used image processing algorithm in many computer vision applications. There have been many efforts in the past to implement optical flow on FPGAs [29], [30], [31] for power and performance benefits.

Table IX shows the estimated integral bit-widths required at various stages of the Optical Flow benchmark. We notice that for stages deeper in the pipeline, the difference between estimates obtained via static analysis and profiling are substantial. The profile estimates are obtained from a training data set and for testing purpose, we use RubberWhale and Dimetrodon image sequences from the Middlebury dataset [32].

For computing the accuracy, we use the Average Angular Error (AAE) metric as discussed in [33], [34]. The reference motion vectors are obtained by using sufficiently wide fixed-point data types at all stages. Table IX shows the max and average integral bitwidth and the fractional bitwidth obtained for the target error. Table X shows that there is a factor of 1.6× reduction in power, and area (% slices) savings of 2.5× by using a fixed-point design. Further, it can be noted that floating point design uses 168 DSPs as against 68 and 22 DSPs used by static and profile based fixed-point designs.

Figure 8 shows the detailed power analysis for floating-point and fixed-point designs for various benchmark pro-
Table VI: Quality, post place and route power, area and throughput metrics for USM benchmark using float, and using bit-widths estimated using static analysis and profiling techniques.

| Analysis     | Quality (PSNR) | Power (watts) | Clk Period (ns) | Latency (Million) | BRAM | DSP | FF | LUT | Zedboard FPGA slices used(%) | Min. Clk Period (ns) | Max. Throughput (MPixels/sec) | Power (watts) |
|--------------|----------------|---------------|-----------------|-------------------|------|-----|----|-----|------------------------------|---------------------|-----------------------------|---------------|
| Float        | Inf 0.269      | 0.169         | 4.5             | 6.22              | 8    | 46  | 7452| 9012| 12.38                        | 4.33                | 230                         | 0.271         |
| α_{avg}      | Inf 0.159      | 0.169         | 4.5             | 6.22              | 7    | 0   | 5161| 2744| 3.39                         | 4.26                | 234                         | 0.166         |
| α_{avg}      | Inf 0.159      | 0.169         | 4.5             | 6.22              | 7    | 0   | 5161| 2744| 3.39                         | 4.26                | 234                         | 0.166         |

Table VII: Quality, post place and route power, area and throughput metrics for DUS using float, and using bit-widths estimated using static analysis and profiling techniques.

| Analysis     | Quality (PSNR) | Power (watts) | Clk Period (ns) | Latency (Million) | BRAM | DSP | FF | LUT | Zedboard FPGA slices used(%) | Min. Clk Period (ns) | Max. Throughput (MPixels/sec) | Power (watts) |
|--------------|----------------|---------------|-----------------|-------------------|------|-----|----|-----|------------------------------|---------------------|-----------------------------|---------------|
| Float        | Inf 0.269      | 0.169         | 4.5             | 6.22              | 8    | 46  | 7452| 9012| 12.38                        | 4.33                | 230                         | 0.271         |
| α_{avg}      | Inf 0.159      | 0.169         | 4.5             | 6.22              | 7    | 0   | 5161| 2744| 3.39                         | 4.26                | 234                         | 0.166         |
| α_{avg}      | Inf 0.159      | 0.169         | 4.5             | 6.22              | 7    | 0   | 5161| 2744| 3.39                         | 4.26                | 234                         | 0.166         |

Figure 8: Power consumption by individual components on various FPGA various designs.
Table VIII: Comparison of bit-width estimates using profiling technique and static analysis for the DUS benchmark.

| Stage | $\alpha^{in}$ | $\alpha^{max}$ | $\alpha^{avg}$ | $\beta^{avg}$ |
|-------|---------------|----------------|----------------|---------------|
| img   | 8             | 8              | 8              | 0             |
| D{x}  | 8             | 8              | 8              | 3             |
| D{y}  | 8             | 8              | 8              | 6             |
| U{x}  | 8             | 8              | 8              | 8             |
| U{y}  | 8             | 8              | 8              | 10            |

Table IX: Comparison of bit-width estimates using profiling technique and static analysis for the Optical Flow benchmark.

| Stage | $\alpha^{in}$ | $\alpha^{max}$ | $\alpha^{avg}$ | $\beta^{avg}$ |
|-------|---------------|----------------|----------------|---------------|
| Img, Img | 8             | 8              | 8              | 0             |
| I{x}   | 9             | 9              | 9              | 9             |
| I{y}   | 14            | 10             | 10             | 3             |
| Denom  | 15            | 10             | 10             | 3             |
| commonX | 9             | 1              | 1              | 9             |
| commonY| 8             | 7              | 7              | 8             |

Repetitive stages, Instance (1,2,3,4)

Avg, Avg, Avg, Avg: (7,10,18,25), (7,8,8,9), (7,8,8,9), (8,9,9,9)

Common (13,18,25,33), (13,13,13,13), (12,12,12,12), (3,4,5,7), (8,8,9,9), (8,8,9,9), (7,8,9,9)

grams. It shows only the significant components of the dynamic power consumed, and in all the designs, the static power consumption is around 0.122 W.

VII. CONCLUSIONS

The input, output and intermediate values generated in many image processing applications have a limited range. Furthermore, these applications are resilient to errors arising from factors such as limited precision representation, inaccurate computations, and other potential noise sources. In this work, we explored these properties to generate power and area-efficient hardware designs for a given image processing pipeline by using custom fixed-point data types at various stages. We used interval and affine arithmetic based techniques to estimate the number of integral bits required at each stage, and a profile-driven approach to estimate fractional bit-width requirements. The profiling analysis was also able to improve the integral bit-width estimates in some cases by automatically taking into account properties of input image distribution and any correlation between computations on spatially proximal pixels. In addition, the analysis revealed the limit of improvement possible with any static analysis technique for integral bit-width estimation.

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REFERENCES

[1] J. Hegarty, J. Brunhaver, Z. DeVito, J. Ragan-Kelley, N. Cohen, S. Bell, A. Vasilyev, M. Horowitz, and P. Hanrahan, “Darkroom: Compiling high-level image processing code into hardware pipelines,” ACM Trans. Graph., vol. 33, no. 4, pp. 144:1–144:11, 2014.

[2] J. Hegarty, R. Daly, Z. DeVito, J. Ragan-Kelley, M. Horowitz, and P. Hanrahan, “Rigel: Flexible multi-rate image processing hardware,” ACM Trans. Graph., vol. 35, no. 4, pp. 85:1–85:11, Jul. 2016. [Online]. Available: http://doi.acm.org/10.1145/2987824.2925892

[3] N. Chugh, V. Vasista, S. Purini, and U. Bondhugula, “A DSL compiler for accelerating image processing pipelines on FPGAs,” in International Conference on Parallel Architectures and Compilation (PACT), 2016, pp. 327–338.

[4] R. T. Mullapudi, V. Vasista, and U. Bondhugula, “PolyMage: Automatic optimization for image processing pipelines,” in International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2015, pp. 429–443.

[5] R. Membarth, O. Reiche, F. Hannig, J. Teich, M. Körner, and W. Eckert, “Hipacc: A domain-specific language and compiler for image processing,” IEEE Trans. Parallel Distrib. Syst., vol. 27, no. 1, pp. 210–224, 2016.

[6] J. Ragan-Kelley, C. Barnes, A. Adams, S. Paris, F. Durand, and S. Amarasinghe, “Halide: a language and compiler for optimizing parallelism, locality, and recomputation in image processing pipelines,” in ACM SIGPLAN conference on Programming Languages Design and Implementation, 2013, pp. 519–530.

[7] J. Stolfi and L. de Figueiredo, “An introduction to affine arithmetic,” Trends in Applied and Computational Mathematics, vol. 4, no. 3, pp. 297–312, 2003. [Online]. Available: https://tema.sbmac.org.br/tema/article/view/352

[8] S. Vakili, J. M. P. Langlois, and G. Bois, “Enhanced precision analysis for accuracy-aware bit-width optimization using affine arithmetic,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 32, no. 12, pp. 1853–1865, Dec 2013.

[9] J. Cong, K. Gururaj, B. Liu, C. Liu, Z. Zhang, S. Zhou, and Y. Zou, “Evaluation of static analysis techniques for fixed-point precision optimization,” in 2009 17th IEEE Symposium on Field Programmable Custom Computing Machines, April 2009, pp. 231–234.

[10] D. U. Lee, A. A. Gaffar, R. C. C. Cheung, O. Mencer, W. Luk, and G. A. Constantinides, “Accuracy-guaranteed bit-width optimization,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 25, no. 10, pp. 1990–2000, Oct 2006.

[11] L. Zhang, Y. Zhang, and W. Zhou, “Tradeoff between approximation accuracy and complexity for range analysis using affine arithmetic,” J. Signal Process. Syst., vol. 61, no. 3, pp. 279–291, Dec. 2010. [Online]. Available: http://dx.doi.org/10.1007/s11265-010-0452-2
Table X: Quality, post place and route power, area and throughput metrics for the OF benchmark using float, and using bit-widths estimated using static analysis and profiling techniques.

| Analysis      | Quality (AAE (in degree)) | Power (watts) | Clk Period (ns) | Latency (Million) | BRAM | DSP | FF | LUT | Zedboard FPGA slices used(%) | Min. Clk Period (ns) | Max. Throughput (MPixels/sec) | Power (watts) |
|---------------|---------------------------|---------------|-----------------|-------------------|------|-----|----|-----|-------------------------------|-------------------|-------------------------------|--------------|
| Float         | 0.17                      | 0.641         | 6               | 2.07              | 68   | 168 | 44196 | 43548 | 65.28                         | 5.54              | 179                           | 0.683         |
| α+α+α         | 1.60                      | 0.398         | 6               | 2.07              | 60   | 68  | 35522 | 22013 | 32.33                         | 4.90              | 203                           | 0.570         |
| α+α+α         | 1.60                      | 0.388         | 6               | 2.07              | 36   | 22  | 27495 | 18670 | 25.69                         | 4.63              | 215                           | 0.469         |

[12] S. Mahlke, R. Ravindran, M. Schlansker, R. Schreiber, and T. Sherwood, “Bitwidth cognizant architecture synthesis of custom hardware accelerators,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 20, no. 11, pp. 1355–1371, Nov 2001.

[13] M. Budiu, M. Sakr, K. Walker, and S. C. Goldstein, “Bitvalue inference: Detecting and exploiting narrow bitwidth computations,” in *Proceedings from the 6th International Euro-Par Conference on Parallel Processing*, ser. Euro-Par ’00, London, UK, UK: Springer-Verlag, 2000, pp. 969–979. [Online]. Available: http://dl.acm.org/citation.cfm?id=646665.701200

[14] M. Stephenson, J. Babb, and S. Amarasinghe, “Bitwidth analysis with application to silicon compilation,” *SIGPLAN Not.*, vol. 35, no. 5, pp. 108–120, May 2000. [Online]. Available: http://doi.acm.org/10.1145/358438.349317

[15] J. Y. F. Tong, D. Nagle, and R. A. Rutenbar, “Reducing power by optimizing the necessary precision/range of floating-point arithmetic,” *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 8, no. 3, pp. 273–285, Jun. 2000. [Online]. Available: http://dx.doi.org/10.1109/92.845894

[16] A. Sampson, W. Dietl, E. Fortuna, D. Gnanapragasam, L. Ceze, and D. Grossman, “En er: Approximate data types for safe and general low-power computation,” in *Proceedings of the 32Nd ACM SIGPLAN Conference on Programming Language Design and Implementation*, ser. PLDI ’11. New York, NY, USA: ACM, 2011, pp. 164–174. [Online]. Available: http://doi.acm.org/10.1145/1993498.1993518

[17] S. Mittal, “A survey of techniques for approximate computing,” *ACM Comput. Surv.*, vol. 48, no. 4, pp. 62:1–62:33, Mar. 2016. [Online]. Available: http://doi.acm.org/10.1145/2893356

[18] S. Venkataramani, S. T. Chakradhar, K. Roy, and A. Raghunathan, “Approximate computing and the quest for computing efficiency,” in *Proceedings of the 52Nd Annual Design Automation Conference*, ser. DAC ’15. New York, NY, USA: ACM, 2015, pp. 120:1–120:6. [Online]. Available: http://doi.acm.org/10.1145/2744769.2751163

[19] J. Han and M. Orshansky, “Approximate computing: An emerging paradigm for energy-efficient design,” *2013 18th IEEE European Test Symposium (ETS 2013)*, vol. 00, pp. 1–6, 2013.

[20] A. B. Kahng and S. Kang, “Accuracy-configurable adder for approximate arithmetic designs,” in *Proceedings of the 49th Design Automation Conference*, ser. DAC ’12. New York, NY, USA: ACM, 2012, pp. 820–825. [Online]. Available: http://doi.acm.org/10.1145/2228360.2228509

[21] C. Liu, J. Han, and F. Lombardi, “A low-power, high-performance approximate multiplier with configurable parallel error recovery,” in *Proceedings of the Conference on Design, Automation & Test in Europe*, ser. DATE ’14. 3001 Leuven, Belgium: European Design and Automation Association, 2014, pp. 95:1–95:4. [Online]. Available: http://dl.acm.org/citation.cfm?id=2616606.2616722

[22] “PolyMage project on bitbucket. Apache 2.0 license,” 2016, https://bitbucket.org/udayb/polyMage

[23] S. Krishnamoorthy, M. Baskaran, U. Bondhugula, J. Ramamurthy, A. Rountev, and P. Sadayappan, “Effective Automatic Parallelization of Stencil Computations,” in *ACM SIGPLAN conference on Programming Languages Design and Implementation*, 2007.

[24] “The Heterogeneous Image Processing Acceleration Framework,” http://hipacc-lang.org/.

[25] S. Kiel, “Yalaa: Yet another library for affine arithmetic,” *Reliable Computing*, vol. 16, pp. 114–129, 2012. [Online]. Available: http://interval.louisiana.edu/reliable-computing-journal/volume-16/reliable-computing-16-pp-114-129.pdf

[26] A. Torralba and A. Oliva, “Statistics of natural image categories,” *Network: computation in neural systems*, vol. 14, no. 3, pp. 391–412, 2003.

[27] “Oxford Buildings Dataset,” http://www.robots.ox.ac.uk/~vgg/data/oxbuildings/

[28] B. K. Horn and B. G. Schunck, “Determining optical flow,” *Artificial intelligence*, vol. 17, no. 1-3, pp. 185–203, 1981.

[29] J. Diaz, E. Ros, F. Pelayo, E. M. Ortigosa, and S. Mota, “Fpga-based real-time optical-flow system,” *IEEE Transactions on Circuits and Systems for Video Technology*, vol. 16, no. 2, pp. 274–279, Feb 2006.

[30] A. Browne, T. M. McGinnity, G. Prasad, and J. Condell, “Fpga based high accuracy optical flow algorithm,” in *IET Irish Signals and Systems Conference (ISSC 2010)*, June 2010, pp. 112–117.

[31] E. Zhu, Y. Li, and Y. Shi, “Fast optical flow estimation without parallel architectures,” *IEEE Transactions on Circuits and Systems for Video Technology*, vol. PP, no. 99, pp. 1–1, 2016.

[32] “Middlebury Flow Dataset,” vision.middlebury.edu/flow/

[33] D. J. Fleet and A. D. Jepson, “Computation of component image velocity from local phase information,” *Int. J. Comput. Vision*, vol. 5, no. 1, pp. 77–104, Sep. 1990. [Online]. Available: http://dx.doi.org/10.1007/BF00056772
[34] M. Otte and H.-H. Nagel, “Optical flow estimation: Advances and comparisons,” in Proceedings of the Third European Conference on Computer Vision (Vol. 1), ser. ECCV ’94. Secaucus, NJ, USA: Springer-Verlag New York, Inc., 1994, pp. 51–60. [Online]. Available: http://dl.acm.org/citation.cfm?id=189359.189368