Enhancement of the photovoltaic performance of dye-sensitized solar cell using porous silicon layer as photoelectrode

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Abstract. Porous Silicon Dye-sensitized solar cell (PS-DSSC) with N719 Dye was employed as photoelectrode. PS layers were formed on textured crystalline silicon CZ-Si (100) by electrochemical etching (ECE) in hydrogen fluoride (HF) based electrolyte at constant current density for different etching times. The morphological properties of the PS were investigated by scanning electron microscopy (SEM). The optical properties of the textured surfaces are studied using photoluminescence (PL) and reflectivity measurements. The bandgaps of PS from UV-Vis and PL measurements increase to 1.9 eV. The Current-Voltage (I-V) characteristics show that the short-circuit current density Jsc and the open-circuit voltage Voc increased as the porosity of the PS layer increased. These results show an improvement in the efficiency of PS-DSSC.

Keywords. Photovoltaics, Dye-sensitized solar cell, Porous Silicon, Electrochemical etching.

1. Introduction

Lately, photovoltaic devices, especially dye-sensitized solar cells (DSSCs), attract widespread academic and commercial attention by increasing the light-harvesting efficiency (LHE) of photovoltaic devices because of their low cost and higher efficiency[1-5]. Therefore, many approaches were made to improve the LHE, especially the improvement done through the photoanode. For example, plasmonic photoanodes, photonic crystal photoanodes, a porous active layer, hierarchically nanostructured photoanode, scattering layers[6-11].

One of the most critical issues is changing the optical design of the DSSC to improve the absorbance of light through the cell. Despite difficulties facing the researcher, such as losing the light reflectance and dye adsorption on the wide bandgap semiconductor. Scientists were hoping to discover new structures to enhance the light trapping through the photoanode. The texture of the surface plays a vital role in enhancing the conversion efficiency of the photovoltaic solar cell by lowering the reflection of light from the front surface, increasing the light trip inside the cell. As a result, the surface area of the photoanode increases[12-15]. The use of textured surface substrates as photoanode for DSSCs has been reported in some articles recently[16-17]. Thus, DSSC provides an economically and technically credible complementary concept to traditional PN junction photovoltaic devices.
In traditional photovoltaic systems, the semiconductor responsible for both the light absorption and charge carrier transport; on the other side, the two functions are separated here. Light is adsorbed to the surface of a wideband semiconductor, which is absorbed by a sensitizer. Charge separation created at the interface through photoinduced electrons is injected from the dye into the conduction band of the wideband semiconductor and then injected from the conduction band of the semiconductor to the charge collector. The role of dyes with a broad absorption band combining with oxide films of nanocrystalline morphology allows harvesting a large fraction of sunlight. Porous silicon (PS) has attracted much attention in the last years discovered in Bell Laboratories by accident as a byproduct of the wafer polishing process. This material is formed of a nanostructured PS skeleton. Porous silicon is well known for its abundance on the earth, good electrical conductivity, large specific surface area, and easy fabrication. PS is manufactured by electrochemical etching of silicon in hydrogen fluoride (HF) solution. In addition, the etchings methods help manage the morphological properties of PS layers (thickness and porosity). The critical factors in this method are the silicon doping type (P-type, n-type), the HF concentration, the electrolyte type (aqueous, organic, oxidant), the anodization etching time, and the surfactant. In this work, we use a porous silicon substrate as a photoanode in DSSC looked into the possibility of having a light-trapping process. First, we formed three different PS samples by using the electrochemical anodization etching process. Following that, ITO film was deposited on PSi substrates with electron beam sputtering, followed by the deposition of a wide bandgap (TiO₂) layer.

In this work, DSSCs have been constructed. An analysis involving SEM imaging for morphology, Photoluminescence spectroscopy (PL), UV–visible spectroscopy, and current-voltage measurements has been examined to characterize the proposed DSSC. Si substrates with different porosity layers changed both the dye absorption capacity and the optical property, making LHE far better.

2. Experimental

2.1 porous silicon fabrications

PS samples were fabricated by electrochemical etching of Czochralski (CZ) p-type [100] oriented silicon wafers with resistivity from (2 to 5) Ω. Cm and a thickness of 450 µm. firstly cut silicon samples into 1.5 × 1.5 cm² square samples. Before electrochemical etching, the wafers were and then dipped in trichloroethylene (isopropyl) and heated for 5 min then washed in de-ionized water, then dried under a stream of nitrogen (N₂) gas to remove all traces of native oxide. Porous silicon was formed in a Teflon electrochemical cell with two electrodes silicon wafer as an anode and platinum contacts of the electrolyte as a cathode.

The PS was prepared by electrochemical anodization method in an electrolyte of 40 % hydrofluoric acid and 96 % ethanol [HF: C₂H₅OH = 2:1 by volume] at a constant current density of 20 mA/cm², and different etching time 15, 25, and 35 min. The samples were cleaned with acetone and then dipped in ethanol to remove the inorganic residuals, then used N₂ gas to dry the samples. Ethanol is always added to the solution to reduce the surface tension of HF, enabling the H₂ gas created during the reaction to avoid and prevent it from attaching to the etching surface and then enhancing the homogeneity of the resulting PS.

2.2 Preparation of photo-anode for DSSC
Firstly the PS substrate was cleaned with acetone and ethanol and then dried with N₂ gas. Next, the Indium Tin Oxide (ITO) was deposited on the PS layer using the sputtering technique where the system pressure was below 2×10⁻⁷ torr. After the growth, we annealed the samples at 400 °C under vacuum for 20 min. The thickness of ITO thin film is 50 nm. An area of 1x1 cm² was identified on a porous silicon substrate with a thin layer of ITO by using adhesive tape. The adhesive tape was used to define the deposition area and controls the film thickness. A drop of TiO₂ paste is spread by using a glass rod in activating area. The TiO₂ paste was prepared as follows: in a glass mortar, grind 1 gm of commercial TiO₂ powder (Degussa, P25) with 1 ml of distilled water containing (10 % v:v ) acetylacetone (alpha, India), the acetylacetone is used as a dispersing agent. The mixture was then diluted by adding 1 ml of distilled water with continuous grinding. Reducing the suspension's surface tension is done by adding a few drops of triton X-100 (oxford, India) as a surfactant to disperse the TiO₂ nanoparticles in the colloidal. The obtained paste was transferred to a dropper bottle and stored in the dark until use. The paste was then dried on the samples at room temperature for 20 minutes and then sintered at 450 °C for about 30 minutes. After cooling, immersed the TiO₂ electrode in a 1.5x10⁻⁴M solution of the sensitizer dye, namely cis-bis (isothiocyanato) bis(2,2'- bipyridyl-4,4-dicarboxylato) -ruthenium (II) (ruthenium-535, Solaronix) inanhydrous ethanol, for 24 h at room temperature, to absorb the dye on TiO₂. After that period, samples were rinsed with anhydrous ethanol to wash the unattached dye molecules away and dry. A counter-electrode was prepared from platinum on an ITO glass substrate. The two electrodes were put together in a sandwich cell, and the electrolyte was in between them. Two electrolyte solutions were used triiodide/iodine (I⁻/I₃) redox. The triiodide/iodine is prepared by mixing 0.1269 gm Iodine I₂ (0.05M) and 0.830 gm potassium iodide KI (0.5M) with 10 mL of ethylene glycol soluble them very well by continuous stirring.

Figure 1 The schematic diagram for porous silicon dye-sensitized solar cell (PS-DSSC)

3. Results and Discussion

3.1 PS morphology of the surface

Figure 2 shows the surface morphology of porous silicon samples using a scanning electron microscope (SEM) during the etching process. Figure 2 (a) shows the surface morphology before PS formation, whereas the image shows many different sizes of spaced pyramids covered the surface. Figure 2 (b-d) shows the surface morphology after PS formation, which was fabricated with constant current density 20 mA/cm² and different etching times 15, 25, and 35 min at room temperature. The images illustrate the increase in surface area and porosities with different etching times.
Figure 2 SEM image of top view (a) silicon substrate without etching (b) PS formed at 15 min etching time (c) PS formed at 25 min etching time (d) PS formed at 35 min etching time.

Figure (3) shows SEM images for the side view of the pyramids after depositing the ITO layer, which illustrates white light on the edge of pyramids, and TiO$_2$ which appears between and upon the pyramids. The high magnification shows the edge of the pyramid with a white beam of ITO and bubbles of TiO$_2$. In contrast, the ITO thickness is measured and found to be 49.71nm.

Figure 3 Side view of SEM image for ITO and TiO$_2$ on PS layer.

3.2 Optical properties

3.2.1 Photoluminescence (PL) of PS layers and pore size

Figure (4) show the photoluminescence spectra for PS samples with different etching times 15, 25, and 35 min and constant current density 20 mA/cm$^2$ with peaks at 655, 653.7, and 652.6 nm, respectively. The
spectra show a blue shift indicates an increase in energy gap as etching time increased. The energy gap is calculated from

\[ E_g = \frac{hc}{\lambda} = \frac{1240}{\lambda} \]  

(1)

Where \( E_g \) is the Energy gap, \( h \) is Planck’s constant, \( c \) is the speed of light and \( \lambda \) the peak wavelength of the photoluminescence. The average pore diameter was calculated \(^{[36]}\)

\[ E(\text{ev}) = E_g + \frac{h^2}{8d^2} \left[ \frac{1}{m_e} + \frac{1}{m_h} \right] \]  

(2)

The bandgap of bulk silicon \( E_g \) is 1.12 eV, \( h \) is Planck’s constant, the pore diameter is \( d \), \( m_e \) and \( m_h \) is the mass of electron and hole, respectively. substitution with \( E_g \), \( h \), \( m_h \) and \( m_e \), this formula is simplified to

\[ d = \sqrt{\frac{26.948}{E-1.12}} \]  

(3)

The calculated pore diameter (d) is 5.90, 5.88, and 5.87 (nm) for 15, 25, and 35 min etching times. Thus, the pore diameter is decreasing with increasing the etching time.

![Figure 4 Photoluminescence spectra of porous silicon sample with different etching time](image)

3.2.2 Reflectivity

Figure 5(a) shows the reflectance curve with different etching times. UV-Vis spectrophotometry was carried out to study optical changes on silicon after etching. We can calculate the energy bandgap by using the absorbance coefficient \( (\alpha) \) and reflectance spectrograph \( (R) \) \(^{[37, 38]}\).

\[ \alpha = \frac{1}{2t} \ln \frac{R_{\text{max}} - R_{\text{min}}}{R - R_{\text{min}}} \]  

(4)
The absorption coefficient is \( \alpha \) that the film's thickness is \( t \), \( R_{\text{max}} \) and \( R_{\text{min}} \) are the maximum and minimum reflectance in the diffused reflection spectra. The reflectance for any intermediate photon energy is \( R \). The calculated energy gap \( E_g \) computed from\(^{[39]}\)

\[
\alpha h \nu = A (h \nu - E_g)^m
\]  

(5)

The edge width parameter is \( A \), \( m = \frac{1}{2} \) for direct transition, and 2 for indirect transition. As shown in figure 5(b), the graph was a plot between \((\alpha h \nu)^{1/2}\) and \( h \nu \) then drawing the tangent line to determine the energy gap.

![Figure 5 a) Reflectance curve b) The curve to determine the energy bandgap](image)

Table 1 comparison between energy band gaps from UV-Vis spectrophotometry and photoluminescence

| Etching time (min) | Energy band gap (eV) |
|-------------------|---------------------|
|                   | UV      | PL          |
| 0                 | 1.100   | 1.12 (literature) |
| 15                | 1.880   | 1.893       |
| 25                | 1.885   | 1.897       |
| 35                | 1.900   | 1.900       |

3.3 I-V characteristic for PSDSSC

Figure (6) shows the I-V curve for PSDSSC with ruthenium dye for five etching times 0, 15, 20, 25, and 35 min. Table 2 shows the solar cell parameters. The curves show that the \( V_{\text{OC}} \) and \( J_{\text{sc}} \) increases to the highest open-circuit voltage values, 118 mV, and highest short-circuit current density of 0.223 mA/cm² at 35min etching time. Moreover, the fill factor reaches the highest value of 0.42 and six times the conversion efficiency for the 35 min etching time.
Figure 6 current-voltage characteristics of DSSCs fabricated by different etching time

Table (2) performance characteristics of DSSCs fabricated by different etching time

| Time | VOC (volt) | JSC (mA/cm²) | Vmax (volt) | Jmax (mA/cm²) | Pmax (μW/cm²) | F.F  |
|------|------------|--------------|-------------|---------------|---------------|------|
| 0    | 0.034      | 0.170        | 0.020       | 0.085         | 1.700         | 0.29 |
| 15   | 0.070      | 0.091        | 0.040       | 0.052         | 2.080         | 0.33 |
| 20   | 0.074      | 0.159        | 0.039       | 0.102         | 3.978         | 0.34 |
| 25   | 0.084      | 0.209        | 0.049       | 0.122         | 5.978         | 0.35 |
| 35   | 0.118      | 0.223        | 0.079       | 0.140         | 11.060        | 0.42 |

4. Conclusion

Porous silicon (PS) samples were prepared at constant etching current 20 mA/cm² at etching times 15, 20, 25, and 35 min used as photoanode in DSSC show that by increasing etching time, the energy bandgap was increased from 1.12 eV before etching to 1.9 eV after etching. The porosity increased, and the surface area of PS was increased, so we used PS as photoelectrode in DSSC because it helped the dye solution to distribute over a large surface area and absorb much light, which improved the efficiency of DSSC. The best DSSC, which had PS with an etching time of 35 min their efficiency was increased six times more than silicon before any etching.

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