Investigation of Self-heating Effects in Ultrathin FDSOI MOSFETS

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Abstract: This paper contains the design consideration of 18nm FDSOI MOSFET for mitigating the self-heating effects. As the device scaling reaches towards the nano regime, self-heating effects are quite significant. Increase in the lattice temperature will lead to decrease in the mobility and degradation of the drain current. Self-heating effects are investigated in FDSOI MOSFET by comparing different physical parameter variations like gate length, spacer thickness, buried oxide thickness and source/drain/metal contacts. It is being observed that the heat sinks used as metal contacts can reduce lattice temperature up to 62% and spacer size thickness can reduce it by 10%. However the buried oxide box thickness and gate length modifications do not have considerable impact on the self-heating.

1. Introduction
Silicon on insulator (SOI) MOSFET, as the name suggests has silicon layer on the top of insulator layer to build an active device. Insulator layer is usually made up of SiO2. FD-SOI MOSFET has several advantages over bulk MOSFET like the improved subthreshold slope, reduced parasitic capacitance and tolerant to radiations. Hence, FDSOI is always preferred for low-power digital applications along with high speed [1-2].

Concept of Self heating effect (SHE): From the figure 1, it is evident that primary path of energy transport is scattering between electron and optical phonon followed by optical phonon to the lattice. Physical sense is that on application of drain bias to the device, electron gain kinetic energy by lateral electric field and interacted with optical and acoustic bath.

High Electric Field

Hot Electron Transport

τ ~ 0.1ps

Optical phonon Emission

τ ~ 10ps

Acoustic phonon Emission

τ ~ 10ps

Heat Conduction in Semiconductor

Figure 1. Generation of heat due to kinetic energy of particles in semiconductors
Most of the electron energy is stored as an optical phonon bath. The optical phonons have zero group velocity so heat is localized and transferred from optical phonon to acoustic phonon via a harmonic decay process. This process is relatively sluggish therefore a hot spot forms near the drain terminal of the device occurs. In active region the raised temperature leads to increase phonon scattering. Hence phonon scattering results in mobility reduction and subsequently current degradation. This phenomenon is called as self-heating. Majority of the heat is absorbed by the lattice from the optical phonons.

Self-heating in a bulk MOSFET is not that much significant as heat generated near drain terminal is dissipated to the substrate. Whereas in SOI MOSFET, the buried SOI BOX acts as a barrier to the heat. Due to device scaling over the years, SHE becomes more prominent. The only way to reduce the self-heating effects is box or material engineering. The heat generated due to self-heating is dissipated from the device through the source, drain or gate contacts.

The SOI device is simulated using 2D hydrodynamic simulation along with thermodynamic simulation program to examine the device lattice temperature and drain current between terminals.

2. Device design and Simulation Set up

In this section, metal gate conventional FD SOI MOSFET is designed for high performance. The conventional metal gate SOI has physical gate length of 18nm, thickness of channel 10 nm, BOX thickness of 40 nm. Oxide thickness of 1nm is used. The maximum concentration of phosphorus in the S/D region is $10^{20}$/cm$^3$. Channel region is doped with low boron concentration of $10^{17}$/cm$^3$. All the simulations are performed using Sentaurus 2-D TCAD simulator. All the calculations are taken per unit channel width. The thermodynamic model, hydrodynamic models, drift-diffusion transport model and density gradient model are included for device simulations for calculating energy transport of the carrier in transport equation. In this paper the electron temperature is calculated differently than lattice temperature to investigate SHE. The physical dimensions and doping concentration values are chosen as per ITRS standards.

![Doping concentration of an FD-SOI MOSFET.](image)

Physical dimensions and doping concentration of FD-SOI MOSFET are given in table 1. The basic model of electronics used for above device simulation consists of the Poisson and continuity equations. The Poisson equation is

$$ \nabla \cdot (\varepsilon \nabla \phi) = q(p - n + N_D - N_A) \rho_{\text{trap}} $$

Where $\varepsilon$ is electrical permittivity, $n$ and $p$ are electron and hole densities, $q$ is electronics charge.
Table 1. Structure of simulated FD-SOI MOSFET

| Physical Parameter                  | Value   |
|------------------------------------|---------|
| N⁺ Source/drain doping             | 1e20/cm³ |
| P-type Silicon film doping         | 1e17/cm³ |
| P-type Silicon Substrate           | 1.0e17/cm³ |
| Thickness of Source/Drain          | 10 nm   |
| Buried oxide insulator thickness   | 40 nm   |
| Channel length                     | 18 nm   |
| Gate oxide thickness               | 1 nm    |
| Gate work function                 | 4.5eV   |

N⁺ and N⁻ are ionized donors and ionized acceptor respectively. \( \rho_{-\text{trap}} \) is charge densities contributed by traps and fixed charges.

Electron and hole continuity equations are

\[
\nabla \cdot J_n = qR_{\text{net}} + q(\partial n / \partial t) \tag{2}
\]
\[
\nabla \cdot J_p = qR_{\text{net}} + q(\partial p / \partial t) \tag{3}
\]

Where \( J_n \) and \( J_p \) is the electron and hole current densities and \( R_{\text{net}} \) - net electron hole recombination rate.

Shockley-read-hall recombination rate is given by

\[
R_{\text{net}} = \frac{n.p - n_i,\text{eff}^2}{cp(n+n_1)+c_p(p+p_1)} \tag{4}
\]

where:

\[
n_1 = n_i,\text{eff} \cdot e^{E_{\text{trap}}/Kt^4}
\]

and

\[
p_1 = n_i,\text{eff} \cdot e^{E_{\text{trap}}/Kt^4}
\]

The difference between defect level and intrinsic level is called as \( E_{\text{trap}} \). And \( n_{\text{eff}} \) is intrinsic carrier concentration. \( r_p \) and \( r_n \) is electron and hole carrier life time.

It is known that when thickness of material is smaller than phonon mean free path than thermal conductivity of material decreases drastically. Channel length of SOI is taken as 18nm and phonon mean free path is known to be 300nm in silicon material. Hence the hot spot temperature increases. In Monte Carlo simulation which solves BTE, this effect is taken but not in hydrodynamic approach. So modified version of approach of Sondheimer [8] is used.

For semiconductor of thickness \( t \) with \( z \) axis perpendicular to the plane of the film located between \( z=0 \) to \( z=t \) thermal conductivity as a function of \( t \) is given by

\[
K(z) = K_d(T) \left[ \frac{3}{8} \sin^3 x \times (1 - e^{-\frac{z}{2e(T)\cos x}}) \cosh \left( \frac{t-2\pi}{2e(T)\cos x} \right) \right] dx \tag{5}
\]

Where \( \lambda(T) \) is mean free path.

\[
\lambda(T) = \lambda_0 \left( \frac{300}{T} \right) \text{nm}
\]
With the room temperature mean free path $\lambda_0=290$nm, Sentaurus does not provide distance dependent thermal conductivity inside material.

$$K_d(T)=\frac{1}{\kappa_{a} + \kappa_{b} \times T + \kappa_{c} \times T^2}$$

(6)

Where default value at room temperature is

$$\kappa_a = 0.03$cmKW\(^{-1}\)$$

$$\kappa_b = 1.56 \times 10^{-3}$cmW\(^{-1}\)$$

$$\kappa_c = 1.65 \times 10^{-6}$cmKW\(^{-1}\)$$

Sentaurus uses above equation over the thickness of silicon film, in the case of our device thickness is 10nm, so modified value at room temperature as per the approach of Sondheimer are

$$K_a(T) = 0.0664317K_0(T)$$

$$\kappa_a = 0.453311$cmKW\(^{-1}\)$$

$$\kappa_b = 23.7307 \times 10^{-3}$cmW\(^{-1}\)$$

$$\kappa_c = 0.251 \times 10^{-6}$cmKW\(^{-1}\)$$

Change these values of Kappa in sentaurus parameter file and perform the simulations for calculating the SHE.

3. RESULTS AND DISCUSSION

The self-heating effect of FD-SOI MOSFET for 18nm gate length is studied. The self-heating effects of the FDSOI are investigated for different gate lengths, spacer lengths and BOX thickness.

3.1 Quasi stationary Simulations

It is interesting to note that maximum lattice temperature and total heat generated due to reception of carriers at high speed is at the drain terminal. For estimation of lattice temperature, we have calculated surface resistance at gate and substrate contacts. The results shown by simulations are very much comparable to Vasileska et al. [9][10][11] and Etessam et al [12].

As we know that cost factor = "(maximum temperature rise)/(drain current ). Also cost factor for heat generation = "(maximum heat generation)/(drain current). SO cost factor has almost linear variation with drain current for lattice temperature rise and heat generation.

**Figure 3.** Lattice temperature in channel region near drain(y=-5nm) at Vgs=1.2V for varied drain voltage

**Figure 4.** Total heat generated in channel region near drain(y=-5nm) at Vgs=1.2V for varied drain voltage

The reason behind the linear variation is the ballistic transport in the channel where hardly any electron phonon scattering occurs. This variation is more prevalent at lower voltages. For low lattice temperatures of the device we have to operate the device below 1V $V_{DD}$. 
3.2 Thermal Boundary Conditions

Thermal boundary condition required for the device to be fixed in an LSI circuit. Substrate is considered to be an ideal heat sink at 300K.

Figure 7 shows maximum lattice temperature in the device when all the contacts are insulated. It is obvious because no heat sink path provided to the SOI device. As the voltage increases, the lattice temperature and total heat generation will increase. It is being observed that the lattice temperature can be reduced from 1100K fully insulated contacts to 400K without insulating contact. This reduction in the lattice temperature is 62% which is significantly very high. This is possible as the insulating material used near source/drain/gate contacts is having very low thermal conductivity as compared to semiconductors and metals. More insulation to the device contacts is the major cause of self-heating of the device.
3.3 Thermal resistance
Thermal resistance is well-defined as the ratio of the temperature difference between the two surfaces of a material to the rate of heat flow per unit area. Larger value of thermal resistance indicates smaller heat loss. Here thermal resistance

\[
\text{Thermal resistance (R_{th})} = \frac{\text{Maximum Lattice temperature} - 300K}{I_d \times V_d}
\]

![Figure 9. Thermal resistance variation due to varying V_{DS} and at fixed V_{GS}=1.2V](image)

Simulations are performed for variation of drain voltage value from 0.05V to 2.1V at fixed gate voltage of 1.2V. From the figure 9 it can be noted that maximum thermal resistance decline is present in region ranging from 0.3-0.6V, which means escalation in drain current is maximum present at V_{DS}=0.3-0.6V.

3.4 Gate Length Variation
In this section we try to vary physical gate length of FDSOI MOSFET from 18nm to 200nm and simulate the device using hydrodynamic model. Simulation performed at a V_{DS}=V_{GS}=1V for analysing the electrical characterstic and thermal characteristic of the FDSOI MOSFET. For investigation of transfer characteristics of the device, drain voltage is fixed at 1V and varying gate voltage from 0.05V to 1V. The output characteristic are analysed at varying drain voltage from 0.05V to 1.5V and fixed V_{DS}.

![Figure 10. Impact of gate length on self-heating parameter of the ultrathinFDSOI](image)

Figure 10 indicates that maximum lattice temperature is inversely proportional to the gate length which is due to the higher mean free path of the charge carriers.
3.5 BOX Thickness Variation

Optimizing the BOX thickness for utilizing substrate area for heat dissipation is often regarded the most prominent way to reduce the SHE. It is examined that the heat generation is almost identical in the range of 10 to 60nm thickness of the box. So it can be concluded that box thickness variation does not have impact on the SHE.

![Figure 11. Impact of SOI box thickness on lattice temperature](image)

3.6. Spacer Size Variation

The effect of variation of the spacer size is also studied to understand the thermal behaviour of the device. Hence it is analysed that smaller the size of the spacer, lower is self-heating. It can be reduced maximum upto approximately 10% by reducing spacer size from 40nm to 5nm.

![Figure 12. Maximum lattice temperature vs. nitride spacer thickness variation](image)

![Figure 13. Total heat generation vs. nitride spacer thickness variation.](image)

So we can say the heat generations inside the device will be lower for smaller size spacer but at the cost of higher fringing fields.

4. Conclusion and Future Scope

Detailed analysis of self-heating effect in FD-SOI MOSFET using Sentaurus TCAD hydrodynamic simulation under steady state condition is done. As the requirement of lessening of self-heating effects is increasing so it is suggested to use heat sinks at source, drain and gate terminals as metal contacts having higher thermal conductivity. The use of heat sinks can reduce the self-heating temperature up to 62% which is quite significant using metal contacts. We can reduce the self-heating by material or geometrical engineering inside the device. So scaling, spacer size, heat sinks are introduced to analyse the self-heating optimization. It is found that temperature inside the device is increased by 20K only for device scaling from 200nm to 18nm gate length which is insignificant. 5K increase in lattice temperature by varying the BOX thickness from 10nm to 60nm is observed. It is also investigated that the thermal resistance drops drastically whenever VDD applied is 0.3 to...
Cost factor of lattice temperature and total heat inside the device is directly proportional to applied drain voltage. The SOI box is blocking the heat dissipation unlike conventional MOSFET, so box engineering with higher conductive materials is required to be examined for reducing self-heating effects. Another solution to the problem is geometric variation of the buried oxide box which can also be helpful in exploring the optimization of self-heating effects.

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