L- and X-Band Dual-Frequency Synthesizer Utilizing Lithium Niobate RF-MEMS and Open-Loop Frequency Dividers

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Abstract—This article presents an 8.6-GHz oscillator utilizing the third-order antisymmetric overtone (A3) in a lithium niobate (LiNbO3) radio frequency microelectromechanical systems (RF-MEMS) resonator. The oscillator consists of an acoustic resonator in a closed loop with cascaded RF tuned amplifiers (TAs) built on Taiwan Semiconductor Manufacturing Company (TSMC) RF general purpose (GP) 65-nm complementary metal-oxide semiconductor (CMOS). The TAs bandpass response, set by on-chip inductors, satisfies Barkhausen’s oscillation conditions for A3 while suppressing the fundamental and higher order resonances. Two circuit variations are implemented. The first is an 8.6-GHz standalone oscillator with a source-follower buffer for direct 50-Ω-based measurements. The second is an oscillator-divider chain using an on-chip three-stage divide-by-two frequency divider for a ~1.1-GHz output. The standalone oscillator achieves a measured phase noise of −56, −113, and −135 dBc/Hz at 1 kHz, 100 kHz, and 1 MHz offsets from an 8.6-GHz output while consuming 10.2 mW of dc power. The oscillator also attains a figure-of-merit of 201.6 dB at 100-kHz offset, surpassing the state-of-the-art (SoA) oscillators-based electromagnetic (EM) and RF-MEMS. The oscillator-divider chain produces a phase noise of −68.4 and −147 dBc/Hz at 1 kHz and 1 MHz offsets from an 8.6-GHz output while consuming 12 mW of dc power. Its phase noise performance also surpasses the SoA L-band phase-locked loops (PLLs). With further optimization, this work can enable low-power multistandard wireless transceivers featuring high speed, high sensitivity, and high selectivity in small-form factors.

Index Terms—5G, lithium niobate (LiNbO3), microelectromechanical systems (MEMS), oscillator, overtone, phase noise, synthesizers.

I. INTRODUCTION

Currently, the sub-3-GHz frequency bands are too congested to meet the ever-increasing data rates demanded by many cellular users. The call for greater bandwidths and speeds has pushed the 5G radios toward mm-wave frequencies. In the meantime, 5G wireless transceivers are expected to feature higher sensitivity and selectivity while producing longer battery life, all in small-form factors.

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power-hungry phase-locked loop (PLL) referenced to a bulky high Q crystal oscillator (XO). XOs are hardly tunable and generate only low frequencies (<120 MHz), thus necessitating a PLL as a tunable frequency multiplier and leading to a larger footprint, higher power, more spurs, and greater cost [19]. To overcome these shortcomings, we develop a direct frequency synthesizer based on integrating an X-band LiNbO3 RF-MEMS oscillator with complementary metal-oxide semiconductor (CMOS) open-loop frequency dividers. Instead of generating the local oscillator (LO) frequencies from a low-frequency source and “bubble up” through a PLL, our work creates a low-power microwave low-noise source and then “trickle-down” to an LO frequency range from X to L bands via the frequency division. Our approach has the following vital benefits: 1) lower-power consumption; 2) a smaller footprint when compared to off-chip XOs/PLLs; 3) RF carriers with lower-phase noise/jitter for better receiver sensitivity; 4) spurs-free phase noise (unlike PLL) for enhancing receiver selectivity; and 5) a faster response and lower-energy dissipation from removing the overhead for XO startup or a PLL locked to an XO.

To this end, this article presents an X-band oscillator utilizing a third antisymmetric overtone (A3) in a LiNbO3 RF-MEMS resonator and 65-nm CMOS. Two circuit variations have been realized. The first is an 8.6-GHz standalone oscillator with a source-follower buffer for direct 50-Ω-based measurements. The second is an oscillator-divider chain using on-chip frequency dividers for a 1075-MHz output. The standalone oscillator achieves a measured phase noise of −113 dBC/Hz at 100-kHz offset from an 8.6-GHz output while consuming 10.2 mW of dc power. Hence, surpassing the SoA X-band EM oscillators [1]–[4], RF-MEMS oscillators above 5 GHz [15], [20]–[23], and X-band PLLs [24]–[27]. The oscillator-divider chain is characterized by a phase noise of −147 dBC/Hz at 1-MHz offset from a 1075-MHz output while consuming 12 mW of dc power. Its noise performance also surpasses the SoA L-band PLLs [28], [29]. This study can enable low-power wireless transceivers with high speed, high sensitivity, and high selectivity in small-form factors with additional optimization.

The rest of this article is organized as follows. Section II reports on the design and measurements of the antisymmetric mode LiNbO3 MEMS resonators employed to implement the oscillators in this work. Section III then focuses on the design, implementation, and measurement results of the 8.6-GHz oscillator. Section IV explains the design and the implementation of the oscillator-divider chain and reports the measurement results at 1.1 GHz. Finally, Section V compares the results with prior arts and concludes this article.

II. ANTISYMMETRIC MODE LiNbO3 RESONATORS

A. Overview

Antisymmetric Lamb-wave modes (A-modes) are characterized by their antisymmetric vibrational nature about the median plane of the plate. These modes have equal vertical but opposite longitudinal displacement components on the opposite sides of the median plane. The theory defining the resonant frequencies for the excited odd modes can be found in [12]. The resonance of an A-mode resonator is primarily set by the thickness of the LiNbO3 film (t\textsubscript{Li}), and the mode order (m). A smaller thickness would translate to a higher-fundamental frequency; however, this needs careful fabrication and a sophisticated deposition method for thin films to maintain high Q. Empirically, thinner films display worse crystallinity than thicker ones causing degradation in Q. Thinner films are also more susceptible to any fabrication-induced nonuniformity, causing meager yield and uncertainties in setting the center frequency precisely. The overmoding approach helps in achieving higher-resonant frequencies without thinning down the resonator and adding fabrication complexity. It also provides better linearity and power handling due to the larger volume of the device structure.

A high FoM\textsubscript{RES} is crucial for overmode resonances scaling toward microwave frequencies, as shown in Section II-B [12]. Hence, for a resonator using a 650-nm thick Z-cut LiNbO3 film, \(\lambda_1 = 12 \mu m\) and \(m = 3\), A3 resonance rises beyond 6 GHz, which is desired for investigating microwave acoustic oscillators.

The resonator comprised of a three-electrode transducer on top of a mechanically suspended Z-cut LiNbO3 thin-film is shown in Fig. 1(a) and (b). The electrodes connected to signal and ground induce lateral electric fields in the piezoelectric film, hence exciting the resonator into odd-order antisymmetric vibrations. Two identical resonators (A and B) were fabricated, with the dimensions given in the inset of Fig. 1, using a process described in [12]. A 180 nm of copper (Cu) is sputtered and lifted-off as top electrodes. Cu probing pads of \(60 \times 62 \mu m^2\) are electroplated to 3-\(\mu m\) thickness with a 200-\(\mu m\) pitch to reduce the parasitics between the pads.

B. Resonator Measurements

Resonators A and B were measured and characterized using a Keysight N5230A PNA-L network analyzer. A thru-reflect-line (TRL) calibration is done in measurements using on-wafer standards. A multiresonance modified Butterworth-Van Dyke (MBVD) model shown in Fig. 1(c) is used to interpret the measured admittances of resonators A and B shown in Fig. 1(d) and (e), respectively. The MBVD model includes an additional series inductor (\(L_s\)) and a resistor (\(R_s\)) to model the nonnegligible inductance and the surface resistance of the electrodes at high frequencies, respectively. It also incorporates a capacitor of 7 fF and a resistor (\(R_f\)) to model the feedthrough capacitance (\(C_f\)) and the resistive substrate loss, respectively. The resonator also has a static capacitance of 7.5 fF from the interdigitated transducer (\(C_o\)) which is set by the size of the resonator. The loaded quality factor (\(Q_l\)) for each resonance is measured using the 3-dB bandwidth method, while the mechanical quality factor (\(Q_m\)) is extracted via the MBVD model by excluding the electrical loss. \(C_f\) is not de-embedded for catching all the parasitic effects associated with the resonator. \(C_f\) is almost equal to \(C_o\), and hence it is important to be included for accurate oscillator simulations and measurements. \(k^2\) for each resonance is extracted, considering all the device parasitics.
The first five odd-order modes, namely $A_1$, $A_3$, $A_5$, $A_7$, and $A_9$ with resonances at 2.9, 8.6, 14.3, 20, and 25.7 GHz, are characterized. Key measured and extracted parameters, including $Q_l$, $Q_m$, and $k_2^2$, are shown in Fig. 1(d) and (e). For resonator A, $Q_l$ and $Q_m$ are 384 and 424 for $A_3$, 12 and 300 for $A_9$, respectively. For these modes, $Q_m$ varies from 1.1$Q_l$ at 8.6 GHz to 25$Q_l$ at 25.7 GHz, indicating that electrical loss mitigation is crucial at microwave and mm-wave frequencies. While $Q_l \cdot f$ product decreases with the frequency, $Q_m \cdot f$ product increases with the frequency. As investigated in [30], higher order A-modes are better confined between electrodes due to the increasingly larger dispersion mismatch between metalized and un-metalized regions for higher order modes. This feature leads to less acoustic damping loss from the electrodes and less energy loss to the supporting substrate for the higher order modes. Hence, a higher-order mode displays higher $Q_m \cdot f$. Further investigation is needed to understand the dissipation mechanisms quantitatively.

$k_2^2$ decreases from 6.9% for $A_1$ to 0.98% for $A_9$ with a value of 2.2% for $A_3$. The reason behind the degradation of $k_2^2$ with an increasing mode order can be found in [12]. Higher-order resonances translate to a larger phase transition from capacitive to inductive regions which is preferred for stable oscillations. As the FoMRES degrades with the frequency, the phase transition becomes far from ideal (180°). Fig. 1(f) shows that modes $A_3$–$A_{13}$ are capacitive as their phases do not cross the 0° needed at resonance. To excite these higher order modes, extra inductors might be required to be added either in series or in parallel to the resonator hurting its $Q$.

Resonator B has a very similar admittance to resonator A. $A_3$ of resonator B is characterized by a $Q_l$ of 370, a $k_2^2$ of 2.1%, and a FoM$_{RES}$ of 7.7 at 8.6 GHz. Both resonators have an insertion loss of around 10 dB at 8.6 GHz, as shown in Fig. 1(g). This value defines the minimum gain required by a 50-Ω matched oscillator to excite $A_3$.

The series resonant frequency of the tank—the acoustic part of the resonator plus the reactive parasitic elements—(SRF$_{RES}$) can be deduced from the MBVD model. Accounting for $L_s$, SRF$_{RES}$ is around 66 GHz for our device. This SRF value was not captured by our vector network analyzer (VNA) with an upper-frequency limit of 40 GHz. Careful codesign of the resonator, circuit, and integration solutions at microwave frequencies is required if a larger resonator is adopted for a smaller $R_m$. For example, the SRF decreases to 20 GHz for a device with $R_m$ of 20 Ω at $A_3$ and $C_r$ of 75 fF. More studies are required to fully understand the effect of the resonator size on microwave and mm-wave oscillator performance, including its power consumption, phase noise, and tuning range.

III. X-BAND OSCILLATOR

In this section, we introduce the X-band oscillator built on Taiwan Semiconductor Manufacturing Company (TSMC) RF general purpose (GP) 65-nm CMOS and derive circuit parameters for meeting Barkhausen’s conditions. The oscillator is designed to excite $A_3$ of resonator A at 8.6 GHz. Phase noise measurements of the LiNbO$_3$ RF-MEMS oscillator are presented at the end of this section.
A. Architecture

The oscillator consists of an amplifier connected to an RF-MEMS resonator in a positive feedback loop, as shown in Fig. 2(a). The bandpass transfer function of the amplifier allows excitation of $A_3$ while suppressing $A_1$ and other higher order tones. The envisioned amplifier can be realized as an inductively loaded n-type metal-oxide semiconductor (NMOS) common source (CS) transistor. Connecting the resonator between the gate and drain creates a modified Pierce oscillator, as shown in Fig. 2(b).

Alignment of the gain peak frequency with $A_3$, as shown in Fig. 3 (the dashed-line curves), serves to satisfy Barkhausen’s gain condition with minimal power consumption. However, the phase condition is not met by such alignment. The amplifier phase at the peak frequency is around $-180^\circ$, as seen in Fig. 3(a) and the resonator phase at resonance is $0^\circ$, resulting in a loop phase of $-180^\circ$. Placing the CS gain peak at a frequency between $A_1$ and $A_3$ satisfies both conditions, permitting oscillation at $A_3$. Unfortunately, this solution would increase the power consumption due to the lower loop gain (LG) for $A_3$, as the solid-line curves shown in Fig. 3(b). The gain peak frequency depends mainly on the inductor $L$ and the loading capacitor $C_{out}$. $C_{in}$ does not change the peak frequency but affects the LG.

The loading inductor has a set of target metrics, such as $Q$, inductance $L$, and the self-resonant frequency (SRFIND). An inductor designed for a large $Q$ at a frequency between $A_1$ and $A_3$ translates to the design for a small $L$ and a large $C_{out}$. Hence, lower LG at all frequencies. A high $Q$ inductor provides a narrower bandpass response, thus producing a higher-gain suppression of the unwanted tones. For $A_3$ to be minimally affected, the high $Q$ gain peak should be close to the $A_3$ frequency. A larger $L$ and a smaller $C_{out}$ lead to lower $Q$, wider band response, higher LG at all frequencies, and a smaller gain suppression of the unwanted tones. With a lower $Q$ inductor, the design is relaxed in terms of the precise frequency of the gain peak as long as it is between $A_1$ and $A_3$. Simulations anticipating two different sets of $L$ and $C_{out}$ are shown in Fig 4.

The modified Pierce LG response is shown in Figs. 3 and 4. It satisfies the oscillation conditions with a small gain and phase margins. Considering the fabrication, supply voltage, and temperature variations, in addition to post-layout parasitics, the single transistor oscillator would be unpractical. Cascading amplifiers are adopted to have more control over the LG response, such as achieving a wide range of gain and phase margins. The second stage of inductively loaded CS would satisfy the oscillation conditions for $A_1$ and the inductor gains peak frequencies while suppressing the targeted mode.

Three inverting stages are adopted for our oscillator to excite $A_3$. The first and second stages are inductively loaded NMOS CS tuned amplifiers (TAs). The third is a wideband resistive loaded NMOS CS stage that can operate as an amplifier or an attenuator by varying the gate voltage. The last stage controls the voltage swing available at the resonator port, ensuring the linear operation of the resonator. All stages are ac coupled independently to provide the needed bias voltages for...
the transistors and low-noise performance. The TAs bandpass response is determined by the loading inductors \( L_1 \) and \( L_2 \). The inductance values are chosen for a gain peak at 5.7 GHz, a frequency between \( A_1 \) (2.9 GHz) and \( A_3 \) (8.6 GHz). This bandpass response excites \( A_3 \) and suppresses \( A_1 \) and higher order resonances. A low-power source-follower stage is used for 50-\( \Omega \)-based measurements. The oscillator schematic is shown in Fig. 5.

### B. Small-Signal Circuit Analysis

The circuit parameters for meeting Barkhausen’s conditions are derived for fully understanding the oscillator. The process can identify the minimum dc power to start an oscillation and the exact frequency of oscillation. To this end, the oscillator loading is represented by adding \( R_{\text{load}} \) in series to the resonator. As shown in Fig. 5, the loading is represented by adding \( R_{\text{load}} \) in series to the resonator, as shown in Fig. 6. The LG can be expressed as

\[
\text{LG} = A_{\text{transm}} \cdot A_{o1} \cdot A_{o2} \cdot A_{o3}
\]

where \( A_{\text{transm}} \), \( A_{o1} \), \( A_{o2} \), and \( A_{o3} \) are given below

\[
A_{\text{transm}} = \frac{1}{1/y_{\text{in}} + Z_{m} + R_{\text{load}}}
\]

\[
A_{o1} = \frac{1}{sC_{gd1} + g_{m1} + \frac{1}{r_{out1}} + \frac{1}{r_{out2}} + \frac{1}{r_{out3}} + \frac{1}{R_{L}}}
\]

\[
A_{o2} = \frac{1}{sC_{gd2} + g_{m2} + \frac{1}{r_{out2}} + \frac{1}{r_{out3}} + \frac{1}{R_{L}}}
\]

\[
A_{o3} = \frac{1}{sC_{gd3} + g_{m3} + \frac{1}{r_{out3}} + \frac{1}{R_{L}}}
\]

where \( R_{\text{load}} \) is the loading resistance after breaking the loop. \( g_{m1}, g_{m2}, \) and \( g_{m3} \) are the transconductances of \( M_1, M_2, \) and \( M_3, \) respectively. \( c_{gd1}, c_{gd2}, \) and \( c_{gd3} \) are the gate–drain capacitances of \( M_1, M_2, \) and \( M_3, \) respectively. \( r_{out1}, r_{out2}, \) and \( r_{out3} \) are the output resistances of \( M_1, M_2, \) and \( M_3, \) respectively. \( C_{ox} \) is the capacitance due to spiral inductor metals overlap. \( C_{ind} \) is the capacitance from the inductor metal to the substrate. \( R_{sub} \) is the inductor ohmic losses due to eddy currents. \( C_{sub} \) is a fitting parameter. The resonator input impedance \( z_m \) is given as

\[
z_m = \left( \frac{1}{sC_{in}} + sL + R \right) \left( R_m + \frac{1}{sC_{z}} \right) + \left( \frac{R_f + 1}{s} \right)
\]

where \( L \) is the self-inductance from the spiral metallization. \( R \) is the ohmic loss from the finite conductance of the inductor metal. \( C_{ind} \) is the capacitance due to spiral inductor metals overlap. \( C_{ox} \) is the capacitance from the inductor metal to the substrate. \( R_{sub} \) is the inductor ohmic losses due to eddy currents. \( C_{sub} \) is a fitting parameter. The resonator input impedance \( z_m \) is given as

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\]

where \( y_{\text{in}}, y_{\text{out1}}, y_{\text{out2}}, \) and \( y_{\text{out3}} \) are the input admittances of the first, second, and third stage, respectively, and are given as

\[
y_{\text{in}} = \frac{1}{R_{B1}} + sC_{gs1} + sC_{gd1} + \frac{1}{1 + \frac{sC_{gs1}}{1 + \frac{sC_{gd1}}{1 + \frac{sC_{ind1}}{1 + \frac{sC_{ind2}}{1 + \frac{sC_{ind3}}{1 + \frac{1}{R_{L}}}}}}}}
\]

\[
y_{\text{out1}} = \frac{1}{R_{out1}} + sC_{ds1} + \frac{1}{1 + \frac{sC_{gs1}}{1 + \frac{sC_{gs2} + sC_{gd2}}{1 + \frac{sC_{gs3} + sC_{gd3}}{1 + \frac{1}{R_{L}}}}}}
\]

\[
y_{\text{out2}} = \frac{1}{R_{out2}} + sC_{ds2} + \frac{1}{1 + \frac{sC_{gs2} + sC_{gd2}}{1 + \frac{sC_{gs3} + sC_{gd3}}{1 + \frac{1}{R_{L}}}}}
\]

\[
y_{\text{out3}} = \frac{1}{R_{out3}} + sC_{ds3} + \frac{1}{1 + \frac{sC_{gs3} + sC_{gd3}}{1 + \frac{1}{R_{L}}}}
\]

The interstage coupling capacitances are designed to be large enough from affecting the signal transmission at 8.6 GHz. Hence, they are neglected in the above analysis. By solving for \( \text{abs}(\text{LG}) = 1 \) (or 0 dB), the minimal power consumption for starting oscillations is estimated. Moreover,
the frequency of oscillation is estimated by solving phase (LG) = 0. Results based on (1) are shown along with circuit simulated outcome in Fig. 7. The parameters used in (1) to generate Fig. 7 are given as follows: $g_m1 = 7.45$ mS, $g_m2 = 16$ mS, $g_m3 = 9.6$ mS, $r_{out1} = 4.4$ kΩ, $r_{out2} = 1.048$ kΩ, $r_{out3} = 128$ Ω, $C_{gs1} = 32$ fF, $C_{gs2} = 15$ fF, $C_{gs3} = 10$ fF, $C_{gd1} = 4.2$ fF, $C_{gd2} = 4$ fF, $C_{gd3} = 10$ fF, $C_{ds1} = 11$ fF, $C_{ds2} = 14$ fF, $C_{ds3} = 14$ fF, $R_{B1} = 10$ kΩ, $R_{B2} = 14$ kΩ, $L = 400$ Ω, $L_{ind1} = L_{ind2} = 6.35$ nH.

The above equations can guide the analysis of the oscillator small-signal behavior independent of the employed IC technology.

C. Design for Phase Noise

The close-to-carrier noise adds directly to the system noise figure, while the far-from-carrier noise weakens the capability of a receiver to attenuate undesired adjacent channel signals. Both should be reduced in a sophisticated design.

From the resonator standpoint, maximizing power dissipation in the motional branch ($P_m = R_m I^2$) of the resonator without exiting the linear regime (larger $P_m$ reduces far-from-carrier phase noise) produces a better far-from-carrier noise. This can be guaranteed if most of the current passes through the motional arm at resonance ($R_m$) rather than the static arm ($C_s$). However, the oscillator should consume low power for battery-powered mobile applications, leading to the well-known tradeoff between phase noise and power consumption. Resonators with a smaller $R_m$ (thus, a larger resonator if FoMRES is fixed [16]) are preferable for lower far-from-carrier noise. Also, doubling $Q_m$ translates ideally to a lower-6-dB thermal phase noise.

The oscillator bias points, bias circuit design, and transistor flicker noise are all significant contributors to flicker noise. The amplifier should provide enough LG to satisfy Barkhausen’s conditions only for $A_3$ while balancing noise performance and power consumption. To this end, $M_1$, $M_2$, and $M_3$ have lengths of 240, 90, and 70 nm to reduce the impact of flicker noise. Bias voltages and transistor widths are optimized for both flicker and thermal noises with transconductance values given in Fig. 7. The dc currents in $M_1$, $M_2$, $M_3$, and the buffer are 2, 3.2, 2, and 3 mA, respectively, from a 1-V supply. $L_1$ and $L_2$ minimally affect resonator $Q_l$ since their center frequencies are far from 8.6 GHz. Smaller loading resistance for $M_3$ ($R_L$) translates to a better thermal phase noise yet more current consumption. Harmonic balance simulations show that $M_3$ contributes to the noise at 1-kHz offset by 41%, $M_1$ by 35%, and $M_2$ by 20%. For the 1-MHz offset, the noise is dominated by $R_m$ with 24%, $M_1$ with 21%, and $M_3$ with 5% of the total noise.

D. Integration Effects

Figs. 8 and 9 show post-layout stability simulations for the oscillator without and with wire-bonds effects, respectively. A parametric analysis of the impact of the wire-bond length on the oscillator LG was done using the wire-bond model shown in the inset of Fig. 9(a). Apart from the wire inductances, the model includes three additional capacitances to the ground, $C_D$ that captures the distributed capacitances effect over the wire length, and the bonding pads from the MEMS ($C_{MEMS_{pad}}$) and CMOS dies ($C_{CMOS_{pad}}$). $C_{MEMS_{pad}}$ is captured in the standalone resonator measurements,
while the $C_{\text{CMOS, pad}}$ is simulated in the CMOS circuitry. Wire-bonds $Q$ of 30 is assumed in the simulations with different lengths. Fig. 9(a) shows the effect of varying $L_{\text{WB}}$ on the LG, while Fig. 9(b) shows the impact of varying $C_D$ on the LG. Integration parasitics did not affect the parallel resonant frequency ($f_p$) and only slightly lowered the series resonance frequency ($f_s$). Simulations showed that wire-bonds barely load the resonator, as long as the wire inductance gain peak happens far from 8.6 GHz. Phase noise can be recovered by increasing the gate voltage of M1, hence increasing the power consumption. Simulations showed an increase of less than 0.5 mW is needed for the 3-nH wire-bond case to retain the noise.

This parametric study shows that the 8.6-GHz oscillations are resilient to wide variations in wire-bond length.
Resonators are placed close to the edge of the MEMS chip to reduce the wire-bond lengths.

**E. X-Band Measurements**

The TSMC RF GP 65-nm CMOS chip (2 mm × 1 mm) is integrated with the MEMS chip (1.5 cm × 0.5 cm) on a glass substrate via wire bonding. The CMOS circuitry occupying an area of 700 μm × 625 μm is integrated with resonator A as shown in Fig. 10. The oscillator is tested on a probe station where the output is sensed using a 100-μm pitch GSG probe. dc probes with decoupling capacitors are used to deliver the transistor bias voltages. Probing was planned as the measurement method in the design stage to avoid complications from parasitic inductances added to $L_1$ and $L_2$. Phase noise measurements are taken using an R&S FSUP26 signal analyzer and reported in Fig. 11. The oscillator achieves a measured phase noise of $-56$, $-113$, and $-135$ dBc/Hz at 1 kHz, 100 kHz, and 1 MHz offsets from an 8.6-GHz carrier while consuming 10.2 mW of dc power. From Fig. 11, Leeson frequency can be estimated to be around 12 MHz, suggesting a measured loaded $Q$ of 358. This value is lower than the reported value in Fig. 1 due to the integration and circuit loading effects.

**IV. L-BAND OUTPUT**

The X-band oscillator wire-bonded to resonator B is followed by a single-ended-to-differential output stage for conditioning the signals before entering the frequency divider.
TABLE VI

COMPARISON TO THE SoA L-Band RF-MEMS Oscillators

| Resonator | This work | [32] | [33] | [34] | [35] | [36] | [37] | [38] |
|-----------|-----------|------|------|------|------|------|------|------|
| IC Process | LiNbO<sub>3</sub> | FBAR | FBAR | AlN-on-Si CMR | GaN CMR | AlN CMR | AlN CMR | AlN SMR |
| Osc. Freq. (GHz) | 8.6 | 1.5 | 2 | 1 | 1 | 1.05 | 1.16 | 2 |
| Q<sub>0</sub> | 370 | 742 | - | 7100 | 4250 | 1450 | 3760 | 700 |
| k<sup>2</sup> (%) | 2.1 | - | - | - | 0.24 | 1.2 | 0.99 | 0.6 |
| FoM<sub>MEMS</sub> | 7.7 | - | - | - | 10.2 | 17.4 | 36.63 | 4.2 |
| dc Power (mW) | 12 | 1.03 | 0.126 | 7.2 | 4.71 | 3.5 | 4.2 | 4.05 |
| Multiple Frequency Outputs | Yes | 8.6, 4.37, 2.157, 1.07 | No | No | No | No | No | No |
| PN (dBc/Hz) | 1 kHz | -59.4* | -86 | -94 | -75 | -81 | -82.3 | -73** |
| | 1 MHz | -147** | -149 | -150† | -141 | -146 | -173.3 | -157† |
| FoM<sub>OSC</sub> (dB) | 1 MHz | 210.4 | 224 | 201.4 | 194.3 | 201 | 228.4 | 196.9 |

* There are no output pads for measuring the spectra of the 4.3 and 2.15 GHz carriers, but the work can be expanded to include output nodes for these two frequencies. ** Phase noise values measured at 1.07 GHz output. † Value estimated from a plot in [34].

The inputs to the frequency dividers can be level-shifted through the V<sub>C</sub> input shown in Fig. 12(a). The frequency dividers used are simple current mode logic (CML) dividers that operate with moderate input and output swings and very high speeds in submicrometer CMOS [31]. A divide-by-eight circuitry is needed to convert the 8.6-GHz RF-MEMS output to 1.1-GHz output. Hence, division-by-eight is achieved through three stages of divide-by-two circuitry. As shown in Fig. 12(b), the divide-by-two circuit is created by placing two D-latches in a negative feedback loop.

The frequency divider derives its speed from that a differential pair can be quickly enabled and disabled through its tail current source. The design has several metrics, such as the clocking speed that halves after each division, the power budget, and the phase noise. The close-in phase noise of the 1.1-GHz output is limited by the flicker noise generated by the 8.6-GHz oscillator transistors. In contrast, the far-out noise is limited by the last divider stage and the CMOS inverters following it. The total dc power consumption of the L-band circuitry is 12 mW, where the oscillator consumes 6.9 mW and the dividers consume 5.1 mW. In the current chip, the three divider cells are a replica. Power consumed in the divider can be greatly reduced by at least halving the power of each following stage as the clocking speed halves.

Simulations show that the oscillator-divider interface realized through the squarer (buffer inverters following the oscillator) and the single-to-differential circuitry is noisier than the first two high-speed divider stages. This signal preconditioning is crucial for a stable division. The far-from-carrier noise is limited by the last divider stage and the CMOS inverters following it. The total dc power consumption of the L-band circuitry is 12 mW, where the oscillator consumes 6.9 mW and the dividers consume 5.1 mW. In the current chip, the three divider cells are a replica. Power consumed in the divider can be greatly reduced by at least halving the power of each following stage as the clocking speed halves.

In comparison to the X-band oscillators in Tables II and III, the figure-of-merit (FoM<sub>OSC</sub>) of our oscillator surpasses those of the SoA EM and RF-MEMS oscillators above 5 GHz. Moreover, the measured oscillation frequency is the highest reported to date for a MEMS oscillator wire-bonded to CMOS. In comparison to the SoA X-band PLLs in Table IV, the reported 8.6-GHz RF-MEMS oscillator surpasses their phase noise and FoM<sub>OSC</sub> results.

In comparison to the SoA L-band PLLs in Table V, our synthesizer surpasses their phase noise and FoM<sub>OSC</sub> results. This proves our claim that a direct frequency synthesizer based on a high Q RF-MEMS oscillator and open-loop dividers can be beneficial over a PLL referenced to a low-frequency stable source.

In comparison to the L-band RF-MEMS oscillators [32]–[38] in Table VI, our synthesizer with two (potentially four) frequency outputs achieves competitive phase noise results at 1-MHz offset from a 1.1-GHz output. To improve the close-in phase noise for L-band and make it more competitive with prior arts, either increasing the resonator Q<sub>0</sub> or choosing a lower-flicker IC technology for integration (or both) should be considered. A resonator with a Q<sub>0</sub> of 4000 at 8.6 GHz would ideally result in a phase noise around −95 dBc/Hz at 1-kHz offset from 1.1-GHz output using the same active

V. CONCLUSION

In comparison to the X-band oscillators in Tables II and III, the figure-of-merit (FoM<sub>OSC</sub>) of our oscillator surpasses those of the SoA EM and RF-MEMS oscillators above 5 GHz. Moreover, the measured oscillation frequency is the highest reported to date for a MEMS oscillator wire-bonded to CMOS. In comparison to the SoA X-band PLLs in Table IV, the reported 8.6-GHz RF-MEMS oscillator surpasses their phase noise and FoM<sub>OSC</sub> results.

By tuning the inductive loads (L<sub>1</sub> and L<sub>2</sub>) to smaller values, the same oscillator topology can be used to excite higher order resonances. Moreover, adding a switchable capacitor bank parallel to L<sub>1</sub>/L<sub>2</sub> or using a switchable inductor bank can enable the oscillator to hop among different overtones rather than generate a fixed frequency output. Hence, this approach also allows for a potentially ultrawideband tunable frequency generation.

In comparison to the SoA L-band PLLs in Table V, our synthesizer surpasses their phase noise and FoM<sub>OSC</sub> results. This proves our claim that a direct frequency synthesizer based on a high Q RF-MEMS oscillator and open-loop dividers can be beneficial over a PLL referenced to a low-frequency stable source.

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circuitry. Such higher $Q_l$ (11 times fold) would also decrease the resonator motional resistance, leading to better phase noise at 1-MHz offset and lower-power consumption. The higher $Q$ can be potentially achieved by improving the resonator thin-film quality, using metals with lower-mechanical losses for electrodes or SiC or sapphire as a substrate to reduce dielectric loss. For our previous discrete version that uses a similar resonator at the Ku-band [15], increasing the resonator $Q_l$ from 270 to 432 (1.6 times) at 12.9 GHz would surpass the $-95$ dBc/Hz phase noise level at 1-kHz offset from a 1.1-GHz output. Thus, it is more practical to use a low-flicker transistor technology like SiGe rather than improving the resonator $Q_l$ solely. Moreover, injection-locked dividers can minimize the power consumption and the phase noise of the high-frequency dividers, despite trading off the form factor. Other topologies for building the core oscillator, such as cross-coupled differential pairs, might be considered to reduce the power consumption further.

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