Recent Progress on Emerging Transistor-Based Neuromorphic Devices

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Human brain outperforms the current von Neumann digital computer in many aspects, such as energy efficiency and fault-tolerance. Inspired by human brain, neuromorphic computation has attracted increasing research interest. In recent years, emerging neuromorphic devices are widely developed for neuromorphic computing. Herein, the recent progress on transistor-based neuromorphic devices is presented. First, a brief introduction of biological synaptic and neuronal functions is given. Then operation principles and latest progress in neuromorphic transistors, including ion-gate neuromorphic transistors, ferroelectric-gate neuromorphic transistors, and floating-gate neuromorphic transistors, are reviewed and discussed. At last, conclusions and prospects are given.

1. Introduction

The exponential growth of the computing capacity of the von Neumann digital computers has fundamentally changed the way we live, work, and communicate in the past few decades. Improvements in the computing capacity have been mainly driven by the shrinking of the dimension of the complementary metal–oxide–semiconductor (CMOS) transistor. However, given the ever-increasing fabrication costs and impending physical limits, device scaling alone may no longer provide the required performance improvements. In addition, the continuous data exchange between the processor and the memory unit in the von Neumann computing system significantly limits the computing speed and energy efficiency, commonly referred to as von Neumann bottleneck. With the advent of the era of big data, the exponential increase in the amount of data processing has placed critical requirements on the energy efficiency and processing speed of data-centric tasks. The drawbacks of the von Neumann digital computers are more prominent. The era of big data calls for novel energy-efficient computing paradigms.

Our brain is a highly parallel, energy-efficient, and highly fault-tolerant computing system with an ultra-low power consumption of ≈20 W compared with the current von Neumann digital computers. Inspired by the human brain, neuromorphic computing has attracted increasing research interest in recent years. Recently, the software simulation of the human brain based on the von Neumann architecture has made major progress. The software running on the traditional von Neumann digital computer performs calculations through serial processing. Therefore, this approach is energy intensive and unable to effectively emulate the parallel information processing of neural networks. Hardware implementation of the neuromorphic systems, thus, has attracted increasing attention, but newly designed architecture based on the current CMOS transistors often requires a large number of devices to emulate one synapse or a neuron. Taking TrueNorth as an example, this chip integrated 5.4 billion transistors to mimic 1 million neurons and 256 million non-plastic synapses. Plastic synapse emulation needs significantly more transistors. The inefficiency of using CMOS transistors to emulate the human brain originates from the fact that the CMOS transistor and the human brain work in digital versus analog ways, respectively. Human brain is composed of ≈10^{11} neurons and ≈10^{15} synapses, which underlie the function of the human brain. Each neuron can connect with hundreds of other ones with synapses. The ability of the synapse to alter its connection strength according to the neural activities, that is, the synaptic plasticity, is the basis of learning and memory in the neural system. Hardware implementation of synapse and neuron at the device level with emerging electronic/ionic devices is a highly promising candidate for brain-inspired computing. In the past few years, great advances have been made in artificial synapses and neurons with a large variety of two-terminal memristors. Memristors usually have a simple form of a two-terminal structure, which looks like a resistor from the outside. In detail, the structure only consists of three layers, including two electrodes for receiving and sending information, and a “storage” layer between the two electrodes. Unlike a static resistor, memristors can change and retain the internal resistance state according to
the history of the applied voltage and current, behaving like a “memory resistor.”\textsuperscript{12} The ability of the memristor to change its conductance with the external stimuli is similar to the behavior of the synapse to alter its connection strength (synaptic weight) according to the neural activities. Thus, the memristor can act as a synaptic device. When integrated into crossbar arrays, the intermediate computing parameters, such as synaptic weight in the neural network, can be stored as the conductance of the nonvolatile memristor during the computing process. The current at each cross point is the product of the input voltage and the conductance of the memristor following Ohm’s law. The total current at each column is the summation of the current at each point on this column following Kirchhoff’s law. Thus, the vector matrix multiplication can be implemented directly in physical, which is the main computation task in the neural networks but very energy and time intensive for the digital computing system.\textsuperscript{31} The memristor-based crossbar array may realize high integration density because of its simple two-terminal structure. However, for most of the memristors, their fabrication technology still needs to be improved for large-scale integration. The memristor usually shows a really large conductance, which is not desired for power-efficient computing.\textsuperscript{44,49,50} In addition, the memristor usually suffers from the abrupt and stochastic nature of the switching mechanism, which will lead to nonlinear and asymmetrical conductance modulation and large device variations, both of which will limit their performance as artificial synapses.\textsuperscript{51} Moreover, in the memristor arrays, the sneak path current, which flows through the unselected cells, will decrease the computing accuracy. The most practical method to suppress the leaky current is to integrate the memristor with a metal-oxide–semiconductor (MOS) transistor (IT1R), which will lead to a more complicated structure and larger circuit footprint.\textsuperscript{31}

With a control gate, the channel conductance of the transistor can be effectively modulated. Transistor-based neuromorphic devices have attracted increasing attention.\textsuperscript{15,16,52–75} For the emulation of a synapse, the gate is usually used as a pre-synaptic terminal, and the source/drain is used to readout post-synaptic currents. In ion-gate transistors, the motion of ions in the electrolyte is favorable for the emulation of the dynamic characteristics of the biological synapses and neurons.\textsuperscript{16,52,61,62,76–79} The ion electrochemical doping at the dielectric/channel interface makes the transistor favorable for mimicking synaptic weight modulation.\textsuperscript{80–82} In addition, the multi-terminal of the ion-gate neuromorphic transistor enables the device to emulate the information processing function of neurons.\textsuperscript{55,62,79,83} The channel conductance of ferroelectric-gate transistors can be precisely and gradually modulated by the polarization state of the ferroelectric dielectrics using the gate pulses, which makes it favorable for synaptic devices.\textsuperscript{84–86} The floating-gate (FG) transistor has been intensively studied as non-volatile memories.\textsuperscript{87–89} As early as 1996, Diorio et al. proposed an FG silicon MOS transistor for artificial synapse.\textsuperscript{90,91} It has inherently tunable conductance and the advancing to high-density 3D integration, which makes it more attractive for neuromorphic applications.\textsuperscript{92} Therefore, neuromorphic devices based on transistors have attracted considerable attention. Compared with the two-terminal memristive devices, the integration of transistor devices may lead to a larger circuit footprint. However, a multi-input gate structure of the transistor makes it favorable for the integration of neuronal networks.\textsuperscript{79} The capacitive-coupled transistor-based neural networks feature a lower static energy consumption and a better emulation of the neural functionalities.\textsuperscript{134} Furthermore, the transistors have advantages of clear working mechanism and relatively controllable parameters.\textsuperscript{135} In 2019, Fuller et al. proposed an ionic FG memory (the device structure combines an FG transistor with a memristive two-terminal device at the gate), which was proposed for scalable neuromorphic computing.\textsuperscript{94} The synaptic weight readout current was extremely small, which ensures the low power consumption. In this work, the linearity and symmetry of the conductance tuning were greatly improved, which is favorable for the computing accuracy. This work may provide an inspiring optimization idea for neuromorphic device design.

This review focuses on the recent advances and major trends in the field of transistor-based emerging neuromorphic devices. First, we introduce biological synaptic and neuronal functions. Second, operation principles and major advances in neuromorphic transistors, including ion-gate neuromorphic transistors, ferroelectric-gate neuromorphic transistors, and FG neuromorphic transistors, are reviewed and discussed. At last, conclusions and prospects in the field of transistor-based neuromorphic devices are given. In this review, we are focused on the emerging transistor-based neuromorphic devices in emulating synaptic and neuronal functions. The readers who are interested in the materials, structures, mechanisms of the neuromorphic device, and system applications on this topic are encouraged to explore already abundant reviews on this topic.\textsuperscript{14,17,95}  

2. Biological Synaptic and Neuronal Functions

Synapses and neurons are the fundamental information processing units in the human brain. Each neuron can connect with hundreds of other neurons through synapses. As shown in Figure 1a, a neuron is composed of the cell body or soma, dendrites, an axon, and pre-synaptic terminals.\textsuperscript{12} The cell body, or soma, contains the nucleus. It usually gives rise to two kinds of structures: several dendrites and an axon. Dendrites branch out in a tree-like fashion and are the main structure to receive the information from other neurons through synapses. The neuron can integrate the signals received from other neurons. When the amplitude of the integrated signals exceeds the threshold, the neuron will generate an electrical signal, called action potentials, at a specialized region near the origin of the axon called initial segment and from which the signals propagate down the axon. The axon usually extends a distance from the soma, and it can carry action potentials to other neurons. Near the end of the axon, it divides to fine branches, which can contact the dendrites or the soma of other neurons at specialized zones called synapses. The neuron transmitting signals are called the pre-synaptic neuron (PREN). The neuron receiving signals are called the post-synaptic neuron. The PREN transmits signals from its specialized enlarged region of axon’s branches, which is called pre-synaptic terminal. As shown in Figure 1b, when the electrical signal arrives at the pre-synaptic terminal through the axon, it will stimulate the release of chemical substance, called neurotransmitter, to the synaptic cleft. After the release, the neurotransmitter will diffuse across the synaptic cleft and then bind to the receptors on the post-synaptic neuron. The binding leads to the changes of the
membrane potential of the post-synaptic neuron. Then, the information transmits from the PREN to the post-synaptic neuron. Whether synaptic potential has an excitatory or inhibitory effect on the post-synaptic membrane potential totally depends on the receptors on the post-synaptic membrane. The excitatory receptor results in excitatory post-synaptic current (EPSC), and it drives the post-synaptic neuron near the threshold for generating an action potential. The inhibitory receptor leads to inhibitory post-synaptic current (IPSC), and it drives the post-synaptic neuron far away from the threshold for generating an action potential. In the emulation of synapse by transistor-based neuromorphic devices, as shown in Figure 1c, the gate and source/drain are usually used as the pre-synaptic terminal and post-synaptic terminal, respectively. Synapse is the connection between neurons, which can transmit signals between neurons. Each neuron can integrate the signals received from other PRENs. The contribution of one synapse to the information integration can be altered by the neural activity through changing the synaptic connection strength, that is the synaptic weight, which is known as synaptic plasticity. The ability of the synapse to alter its synaptic weight underlies learning and memory in our human brain.

Short-term synaptic plasticity usually lasts from a few milliseconds to seconds. Within this short time frame, the increase and decrease of the synaptic connection strength are called short-term potentiation (STP) and short-term depression (STD), respectively. As one kind of essential short-term plasticity, paired-pulse potentiation (PPF) is a phenomenon that the EPSC amplitude triggered by the second spike (A2) is larger than that triggered by the first spike (A1) when the second spike closely follows the first. As the short-term plasticity can alter the synaptic weight within a short time frame, the synapse can act as a filter by strengthening or depressing the synaptic transmission efficiency. Long-term synaptic plasticity refers to the synaptic weight change that lasts for a long time (a few minutes to weeks, even a lifetime). Long-term reduction/increase of the synaptic weight is known as long-term depression (LTD)/long-term potentiation (LTP). It is believed that the long-term synaptic plasticity is fundamental to learning and memory in our brain.

The notion of synaptic plasticity has been deeply influenced by Hebb’s hypothesis about the synaptic weight modulation by correlated neural activities. Spike-timing-dependent plasticity (STDP), an essential type of Hebbian learning rules, describes the dependence of synaptic weight update on the temporal order of the pre- and post-synaptic spikes. Taking one kind of STDP as an example, if the pre-synaptic spikes lead the post-synaptic spikes in time by tens of milliseconds, the synaptic weight will get stronger, leading to long-term potentiation. On the contrary, if the time order is reversed, the synaptic weight will be weakened, resulting in LTD. The percentage of the synaptic weight change is dependent on the time interval between the pre- and post-synaptic spikes. A small time difference results in a large change of the synaptic weight. A large time difference leads to a small change of the synaptic weight.

3. Ion-Gate Neuromorphic Transistors

3.1. Operation Mechanism of Ion-Gate Neuromorphic Transistors

Figure 2a shows a schematic image of the ion-gate neuromorphic transistor. Electrolyte film with abundant cations (such as H\(^+\) and Li\(^+\)) is used as the electrolyte gate layer. Such electrolyte gate has good electronic insulation characteristics, which is similar to the traditional high-k materials, such as HfO\(_2\), ZrO\(_2\), and Al\(_2\)O\(_3\). In addition, the freely movable ions in the electrolyte can be directionally moved and concentrated under the induction of an electric field. The working mechanism of ion-gate neuromorphic transistors is mainly divided into two types: electrostatic coupling mechanism and electrochemical
doping/de-doping. Among them, as shown in Figure 2b, for ion-impermeable semiconductor materials, ions will move in the electrolyte and accumulate at the electrolyte/gate electrode and electrolyte/channel layer interfaces under the action of the electric field. Due to electrostatic coupling, carriers with opposite signs and equal charge can be induced on the channel layer and the electrode side, forming a dense electric-double-layer (EDL) at the interface. The thickness of the EDL is about 1 nm, so it has a specific capacitance generally greater than 1.0 μF cm⁻². Due to the large capacitance of the electrolyte gate, the pulse voltage that needs to be applied to the gate can be much smaller. Therefore, when emulating synaptic activity, ion-gate neuromorphic transistors can achieve low energy consumption (about 10 fJ spike⁻¹). For ion-permeable semiconductor materials, as shown in Figure 2c, ions can penetrate into the channel layer from the electrolyte under the action of a relatively large electric field, thus directly changing the channel conductance. This working principle is electrochemical doping. Conversely, when a large electric field is applied in the reverse direction, ions that have penetrated into the channel layer will return to the electrolyte. This working principle is electrochemical de-doping. In synaptic electronics, the two mechanisms of electrostatic coupling and electrochemical doping/de-doping are commonly used to emulate the short-term and long-term plasticity of synapses, respectively. In addition, the electrolyte has a strong lateral ionic/electronic coupling effect, which enables the ion-gate transistor to have multiple gate terminals. The multiple input gate structure makes the ion-gate neuromorphic transistor favorable for the emulation of the neuron functions, considering that the neuron receives information from multiple synapses. To date, many types of semiconductor materials and electrolytes are used to fabricate ion-gate neuromorphic devices, which have successfully emulated a variety of synaptic plasticity.

**3.2. Ion-Gate Inorganic Neuromorphic Transistors**

In 2010, Lai et al. constructed one of the earliest ion-gate neuromorphic devices using the RbAg₄I₅ ion conductor layer composite poly[2-methoxy-5-(20-ethylhexyloxy)-p-henylene vinylene] (MEH-PPV) layer as the gate dielectric layer, which is combined with mature Si-based MOS transistor technology. Since then, a lot of innovative work has been carried out to develop and enrich the path of ion-gate neuromorphic transistors. Among them, inorganic semiconductors have good stability and high mobility of carriers, which show great potential in the application of ion-gate neuromorphic transistors. In recent years, there are many inorganic semiconductor materials used in neuromorphic transistors, including carbon nanotubes (CNTs), MoS₂, MoO₃, In₂O₃, indium–tin–oxide (ITO), zinc–tin–oxide (ZTO), indium–zinc–oxide (IZO), indium–gallium–zinc–oxide (IGZO), etc. Kim et al. reported a CNTs neuromorphic transistor with poly(ethylene glycol) monomethyl ether (PEG) gate dielectric. When a positive voltage pulse is applied to the gate of the CNT neuromorphic device, the H⁺ begins to move directionally. Due to the electrostatic coupling effect, a electric-double-layer is formed, which can adjust the carrier concentration in CNTs, resulting in the increase of channel current. After the voltage pulse ends, due to the concentration gradient, the H⁺ near the electrolyte/channel interface will slowly diffuse from the interface to their equilibrium position, so that the channel current continues to decrease until it stabilizes. Based on the electrostatic coupling mechanism and electrochemical doping, the neuromorphic transistor successfully emulated typical synaptic functions, such as EPSC, paired-pulse facilitation (PPF), dynamic logic, long-term enhanced plasticity, long-term inhibited plasticity, and STDP.

In recent years, atomic-layered 2D materials have attracted widespread attention and have shown good application prospects in advanced neuromorphic electronic devices. Graphene is a promising material for high integrated flexible electronic devices due to its excellent thermal stability, ultra-thin-layered structure, and good mechanical properties. Sharbatgi et al. reported concomitant long-term potentiation (LTP) and LTD behaviors using an electrochemically tunable graphene neuromorphic transistor. Then, the gate electrode was used to emulate the presynaptic membrane, and the solid electrolyte of LiClO₄ in poly(ethylene oxide) (PEO) was used to emulate the synaptic cleft of conducting ions between neurons. The structural diagram is shown in Figure 3a. By controlling the concentration of Li⁺ in the graphene layer, the conductance of graphene neuromorphic device can be adjusted accurately and reversibly. When an input current pulse (50 pA, 10 ms) is applied to the graphene device, the channel resistance immediately drops by 30 Ω and then decays to a stable state. At this time, the resistance in steady state is 10 Ω less than that in initial state. This...
phenomenon emulates the synaptic weight change of the excitatory synapse and proves that the permanent change of the conductance is caused by the non-volatile Li$^+$ doping. After applying a series of pulses with different parameters, the behavior of LTP and LTD, as shown in Figure 3b, is also observed. STDP has also been confirmed in this electrochemical synapse by the application of a two-pulse programmable scheme. The successful emulation of various synaptic behaviors indicates that the electrochemistry graphene neuromorphic transistor may become one of the hardware implementation schemes of neuromorphic computing.

MoS$_2$ is considered to be a very promising 2D material with high performance due to enhanced electrostatic control and interlayer van der Waals bonding, which is also widely used in neuromorphic devices.$^{[57,124]}$ Jiang et al. reported the emulations of the brain-like computational systems using a 2D MoS$_2$-based neuromorphic transistor gated by a poly(vinyl alcohol) (PVA) proton conducting electrolyte.$^{[124]}$ The structural diagram is shown in Figure 3c. By regulating multiple presynaptic inputs, spatiotemporal coupling can be performed in such 2D MoS$_2$ neuromorphic transistors. EPSC, PPF, and dynamic filter have been successfully emulated in 2D MoS$_2$ devices. In addition, as shown in Figure 3d,e, multiplicative neural coding and neural gain modulation have been proved successfully. This rate-encoded neuron process can be expressed by the relationship between the average input and output firing rates (i.e., $I$–$O$ relationship). Using the equation $y = kx + b$ to achieve a linear fit to the $I$–$O$ relationship, the change in slope indicates multiplication, and the change in offset (intercept) indicates addition. As shown in Figure 3d, a good linear fit of the $I$–$O$ relationship can be observed. Figure 3e shows the linearly fitted slope ($k$) and $x$-axis intercept ($x_0$) as a function of $V_m$ (modulation voltage applied to $G_m$). The change in slope is the modulation of neuron gain (representing multiplication), and the $x$-axis intercept shifting to the left and right indicates the increase and suppression of excitation (representing addition), respectively. In this multi-terminal neuromorphic device, by controlling the presynaptic input, neuron gain modulation is successfully achieved. This 2D MoS$_2$ neuromorphic device is of great significance for the realization of interesting artificial intelligence in the 2D nanoscale neuromorphic cognitive system.

MOSs have become potential channel materials for neuromorphic transistors due to their high carrier mobility, excellent optical transparency, good stability, and large area preparation.$^{[52,61,132,134]}$ Zhu et al. proposed an IZO neuromorphic transistor.$^{[52]}$ As shown in Figure 4a, without a bottom gate, the applied gate voltage can be directly coupled to the IZO semiconductor through a transverse EDL to achieve lateral regulation. The device is used to emulate a series of short-term plasticity behaviors, including EPSC, PPF, filter behaviors, and the spatiotemporal correlation dynamic logic (as shown in Figure 4b). In addition, the laterally coupled oxide-based neuromorphic transistors can be easily extended to multiple input gates to emulate synaptic interaction functions. The IZO transistor based on proton conductive electrolyte provides a good reference for the subsequent work of neuromorphic devices and has extraordinary significance for synaptic electronics and neuromorphic computing. In 2019, He et al. showed a multi-terminal neural transistor based on the IGZO channel, emulating the dendrite discrimination of different spatiotemporal input modes.$^{[79]}$ First, the device emulates the regulation of synaptic plasticity, such as PPF and filter behaviors. Then, the dendrite recognition of different spatiotemporal input patterns is realized in the multi-terminal neuromorphic transistor. It can greatly reduce the scale and complexity of the neuromorphic system and improve the efficiency of the artificial neural network (ANN). Finally, as an example of spatiotemporal information processing, an
interesting work is proposed to emulate the sound location function of human brain through the multi-terminal IGZO neuromorphic transistor. As shown in Figure 4c, when the sound comes from different directions (pulse voltages are applied on input gates at different moments), the amplitude of the current of post-synaptic neuron1 (POST1) and post-synaptic neuron2 (POST2, the two pairs of source/drain terminals, which are regarded as POSTN1 and POSTN2) will be different. According to the change of these currents, the source direction of the sound can be determined. The ratio of amplitude of $I_{\text{POST2}}$ and $I_{\text{POST1}}$ as a function of the time interval and sound azimuth is shown in Figure 4d. When the time difference is 0 ms, the ratio is 1. When the time difference is between 25 and 1000 ms, the ratio is greater than 1 and increases with the increase of the time difference. When the time difference is between $\frac{1000}{100}$ and $\frac{25}{100}$ ms, the ratio is less than 1 and increases with the increase of the time difference. This method of spatiotemporal discrimination embodies the function of ANN to detect the direction of sound.

### 3.3. Ion-Gate Organic Neuromorphic Transistors

Organic semiconductors stand out in neuromorphic devices because of their own advantages. First, the cost of preparing organic semiconductors is low, which can be directly synthesized by the solution method.\[^{119,121}\] Second, the chemical structure of organic semiconductors can be designed according to specific needs to meet the requirements of neuromorphic devices.\[^{135}\] Third, polymer materials are easy to achieve ion penetration under the action of electric field.\[^{54}\] Fourth, the stretchable flexibility of organic semiconductors makes them more compatible with most materials.\[^{118}\] These advantages make organic semiconductors have great potential applications in flexible electronics, synaptic electronics, and implantable skin electronics.\[^{17,119}\] Now, many organic semiconductors have successfully realized neuromorphic devices, such as pentacene,\[^{74,121}\] poly(3-hexylthiophene) (P3HT),\[^{135}\] sodium4-[2-(2,5-bis(2,3-dihydrothieno[3,4-b][1,4]dioxin-5-yl)thiophen-3-yl)ethoxy]butane-1-sulfonate (ETE-S),\[^{116}\] and poly(3,4-ethylene-dioxythiophene): poly(styrene sulfonate (PEDOT:PSS).\[^{54,118}\]

In 2015, Gkoupidenis et al. reported the simulations of a staircase-like dynamic filtering behavior using a PEDOT:PSS-based neuromorphic transistor gated with a KCl electrolyte.\[^{54}\] The structural diagram is shown in Figure 5a. Due to the electric field, the ions in the electrolyte will penetrate into the PEDOT:PSS polymer to change its hole doping level, and then adjust the current of the channel. When the pulse voltage is removed, the PEDOT:PSS will return to its original state, because the previously injected ions will diffuse back to the electrolyte. The electrochemical synaptic transistor based on PEDOT:PSS realizes typical synaptic behaviors such as PPD (as shown in Figure 5b). As shown in Figure 5c, dynamic filtering is also proved in this organic electrochemical transistor. A series of pulses ($V_{\text{Pre}}$) with variable pulse width $t_p$ (1–9 ms) were applied to the gate electrode, and the post-synaptic current ($I_{\text{Post}}$) was measured as a function of time. The sensitivity of the channel increases when the pulse frequency decreases. This
step-by-step behavior shows that the neuromorphic devices are sensitive to input stimuli and thus can act as dynamic filters. Qian et al. reported a type of poly(3-hexyl thiophene) (P3HT)-based ion-gate neuromorphic transistor, whose structure is shown in Figure 5d. The pulse voltage applied to the gate is used as the input stimulus, and the change of channel conductance represents the synaptic weight. The neuromorphic transistor successfully emulated the EPSC. The electromechanical transistor based on P3HT also achieves self-adjustment (as shown in Figure 5e). When a series of input pulse voltage is applied, the PPF appears on the first two peaks, but then the EPSC value decreases with the continuous stimulate of pulse voltage, which is the same as the adaptability of biological excitatory synapses. In addition, as shown in Figure 5f, the organic neuromorphic transistor also implements the OR logic of double gate regulation. This organic semiconductor ion-gate neuromorphic device combines ionics and electronics to emulate biological functions, paving the way for synaptic electronics, bionic electronics, and neurologically inspired robotics.

4. Ferroelectric-Gate Neuromorphic Transistors

Recently, ferroelectric-gate field-effect transistors (FeFETs) have attracted extensive interest in emulating biological synapses due to the multi-domain polarization switching enabled by the ferroelectric materials and high operating speed. Compared with traditional field-effect transistors, the key feature of the FeFETs is that the gate dielectric is the ferroelectric material. The ferroelectric materials, such as Pb(Zr,Ti)O$_3$ (PZT), poly(vinylidene fluoride) (PVDF), and HfO$_2$-doped ferroelectrics, are usually used in the ferroelectric-gate neuromorphic transistors due to their non-volatile multilevel memory effect. Ferroelectric materials belong to a class of low symmetry crystals with spontaneous polarization states. Figure 6a shows the representative P–E hysteresis loops and the structures of the traditional ferroelectric capacitor, respectively. The saturation P–E loop corresponds to the case that the external electric field exceeds the coercive field ($E_C$), and all the ferroelectric domains align with the external field. The P–E loop reaches the maximum saturation polarization. When the external electric field is removed, the ferroelectric state becomes the remnant polarization ($P_r$) state and can be maintained as long as years in the atmosphere. The sub-loop corresponds to the case that the applied field is less than $E_C$, and the partial ferroelectric domains are switched in the ferroelectric capacitor. Figure 6b shows a schematic diagram of the traditional FeFET structure, the applied gate voltage pulses, the switching states of the multilevel polarization, and the corresponding transfer curves, respectively. The carrier concentration in the channel can be precisely and gradually modulated by changing the polarization state of the ferroelectric dielectrics using the gate voltage pulses. As for neuromorphic transistors, multi-domain polarization switching can be utilized to obtain multilevel channel conductance, which can be used to record the synaptic weights.

In 2017, Oh et al. proposed a ferroelectric-gate neuromorphic device with multilevel states of the remnant polarization. The polarization levels based on partial switching in ferroelectric materials are modulated by the input voltage pulse amplitude, number, width, and frequency. In this work, they obtained 32 levels of remnant polarization states for both...
potentiation and depression. Figure 7a–c shows the three pulse schemes: A–C, respectively. Scheme A consisted of the identical pulses of the amplitude of 1.85 V and the duration time of 50 μs for potentiation, and the pulses of the voltage amplitude of –1.3 V and the duration time of 50 μs for depression. Schemes B and C are pulse schemes with increasing pulse width and increasing voltage amplitude, respectively. A reset pulse of the voltage amplitude of –3.2 V and the duration time of 1 ms was applied to the device before the pulses of schemes A–C, and a voltage pulse of the amplitude of 3.2 V and the duration time of 1 ms was used to read after the pulses of schemes A–C. Figure 7d,e shows the potentiation and depression characteristics of the remnant polarization states of the device, respectively. For schemes A and B, the remnant polarization was gradually saturated. However, for scheme C, the remnant polarization linearly increased/decreased and resulted in 32 levels of polarization states. The reason was that in schemes A and B, the voltage was not changed, and only partial domains had

![Image](https://www.advancedsciencenews.com/)

**Figure 6.** a) Characteristics of P–E loop for different switching states. b) A schematic diagram of the traditional FeFET structure, the applied gate voltage pulses, the switching states of multi-domain partial polarization, and the corresponding transfer curves, respectively. Reproduced with permission.[150] Copyright 2018, IOP Publishing.

**Figure 7.** Three scheme pulses of a) identical pulse with the amplitude of 1.85 V and the duration time of 50 μs for potentiation, and the amplitude of –1.3 V and the duration time of 50 μs for depression, b) increasing pulse width with the increment of 10 μs, and c) increasing voltage amplitude with the increment of ±0.02 V. d) Potentiation and e) depression characteristics of remnant polarization state, respectively. Reproduced with permission.[153] Copyright 2017, IEEE.
switched. Nevertheless, in scheme C, the applied voltage amplitude gradually increased, and the switching domains increased, which lead to the increase of the remnant polarization states. These results reveal that an incremental voltage pulse generates gradually switching ferroelectric domains, which enables a wide range of remnant polarization states. These remnant polarization states correspond to the conductance states in the channel with a linear symmetric change for both potentiation and depression. As a result, these characteristics can be used for the pattern recognition and future high-density neuromorphic systems.

Kim and Lee fabricated a photonic neuromorphic transistor with the improvement of long-term plasticity using ferroelectric polarization. The photonic synapse devices used IGZO as a channel semiconductor. In biological synapses, the repeated stimuli can increase the relaxation time, and the response to the stimuli is called long-term plasticity. In this work, the relaxation characteristics were regulated by the ferroelectric polarization. When two consecutive optical pulses with a width of 1 s were applied to the device, the IGZO photonic device exhibited short-term plasticity behavior. Through changing the optical pulses, the change of the synaptic weight was small and could not maintain a long time, so it is difficult to obtain the LTP. Fortunately, the ferroelectric polarization state can be modulated by voltage pulses applied on the gate. To study the effect of the polarization state on the LTP behavior, ten optical pulses with the width of 2 s and the interval of 1 s were applied to the device to record the changes in synaptic weight. Figure 8 shows the enhanced LTP behavior with the upward and downward polarization states in the ferroelectric material, and the synaptic weight change with various polarization states as a function of the pulse number, respectively.

STDP is considered as an essential characteristic of the Hebbian learning rules in biological neuron network. Jang et al. fabricated a type of ferroelectric-gate organic neuromorphic transistor in a freestanding form with a poly(vinylidene fluoride)-trifluoroethylene (PVDF-TrFE) copolymer. Figure 9a shows the schematic diagram of the ferroelectric-gate neuromorphic transistor structure. PVDF-TrFE film with a thickness of 415 nm was used as the gate dielectric by spin-coating on the Au electrode. Pentacene was evaporated as the organic semiconductor, and the Au was used as the source/drain electrode, respectively. In Figure 9a, we can also see a picture of the fabricated freestanding device. Figure 9b,c shows the symmetric and asymmetric STDP functions, respectively. To examine the two STDP features, presynaptic and postsynaptic spikes were applied with different relative time. To achieve the symmetric STDP function, a single spike was applied to the pre- and post-neurons. When the interval time between the spikes applied on pre- and post-neurons was zero, both the pre- and post-neurons were activated, and the change of the strength was the largest. When the time interval of the both spikes increased, the change of the synaptic strength gradually decreased, which mimicked the symmetric STDP behavior. To obtain the asymmetric STDP function, as shown in Figure 9c, spike trains were applied on the pre- and post-synaptic spike trains. When the interval time between the pre- and post-synapses is over zero, it means that the presynaptic spike arrived before the postsynaptic spike, causing the LTP of the synapse. Nevertheless, when the time interval is less than zero, that is, the presynaptic spike arrived after the postsynaptic spike, resulting in the LTD of the synapse. By applying these pulses, both the symmetric and asymmetric forms of the STDP were simulated.

To achieve the efficient ANN systems on-chip storage, artificial synaptic devices must possess the properties, such as linear conductance modulation, data levels over 32, and low cycle-to-cycle/device-to-device variations. Kim and Lee demonstrated the analog conductance modulation behavior in the FeFET. In this work, the zirconium-doped hafnium oxide (HfZrOx) was used as the gate dielectric, and IGZO was deposited as the semiconductor channel layer, respectively. The HfZrOx thin film was deposited by atomic layer deposition. The IGZO thin film channel material was deposited by radio frequency sputtering. Figure 10a shows the ferroelectric-gate transistors with 64-level conductance states, good linearity with a potentiation of 0.8028, and a depression of 0.6979. Figure 10b shows a two-layer perceptron neural network with 400 input neurons, 100 hidden neurons, and 10 output neurons. The 400 input neurons correspond to 20 × 20 MNIST data, and the 10 output neurons correspond to ten digits. The ANN was trained on 8000 patterns that had been randomly selected from 60 000 images in the training data set. The recognition accuracy was tested on a separate set of 10 000 images from the testing data set. For the ideal synapse neural network, including perfectly linear conductance and 64 conductance states, the recognition accuracy is 94.1%. Nevertheless, the ferroelectric-gate thin film transistor had achieved up to 91.1% recognition accuracy after 125 training epochs, which was comparable to the ideal recognition accuracy, as shown in Figure 10c.

![Figure 8](image-url) The long-term plasticity characteristics of transistors with ferroelectric layer in a) upward and b) downward polarization states, respectively. c) Synaptic weight change with different polarization states as a function of pulse number. Reproduced with permission. Copyright 2020, Wiley-VCH.
Figure 9. a) Schematic device structure of the ferroelectric-gate organic neuromorphic transistor. b,c) Symmetric and asymmetric STDP of the ferroelectric-gate organic neuromorphic transistor, respectively. Reproduced with permission. Copyright 2019, American Chemical Society.

Figure 10. a) Properties of the potentiation and depression of the ferroelectric-gate transistor with incremental pulse scheme. b) Schematic of the two-layer perceptron neural network. c) Simulated recognition accuracy of neural network compared with ideal devices. Reproduced with permission. Copyright 2019, American Chemical Society.
5. FG Neuromorphic Transistors

Compared with the usual field-effect transistor, the FG transistors usually have the same structures with an additional FG embedded in the dielectric, as shown in Figure 11a. Charges (electrons and holes) can be injected into the embedded FG layer during the programming process, and they can be trapped in the FG layer in a non-volatile way, as shown in Figure 11c,d. The trapped charges in the FG layer form the electric field between the FG and the channel. The threshold voltage, thus, can be modulated by the trapped charges. The number of the trapped charges can be precisely modulated by the programming gate pulses (amplitude and duration). Therefore, the channel conductance of the FG transistor can be effectively modulated by the gate pulses. The FG transistors can be used as synaptic devices, because the modulated channel conductance can mimic the synaptic weight.[167–184]

In 2014, Riggert et al. reported a type of FG transistors as memristive devices for neuromorphic computing.[174] As shown in Figure 12a, the memflash device operates in the memristive mode by reconfiguring the three-terminal FG transistor to a two-terminal cell using wiring schema. The synaptic weight is stored as the channel conductance of the FG transistor. High positive and negative voltage pulses applied on the drain are used as programming potentiation and depression pulses, respectively. A low voltage pulse is applied on the drain after each programming pulse to readout the channel conductance of the device in a non-destructive way. The researchers studied the effect of the programming pulse width on the synaptic weight modulation; 175 positive voltage pulses (+10 V) and 175 negative voltage pulses (−7.5 V) of 5, 50, and 100 ms are used as potentiation and depression pulses, respectively. A read pulse of +2.5 V is applied to readout the channel conductance. The experimentally obtained channel conductance is shown in Figure 12b together with the simulated results, which shows that the conductance increases with the increase in the pulse width. To improve the synaptic weight modulation process, the tradeoff between the programming pulses and the energy consumption should be optimized. Then, the effect of the thickness of the tunneling oxide ($d_{\text{ox}}$) on the synaptic weight modulation is studied. As shown in Figure 12c, the potentiation–depression curves for different $d_{\text{ox}}$ are, respectively, normalized to the maximal conductance obtained after 175 potentiation pulses. As a result, the programming pulse voltage decreases with the decrease in the thickness of the tunneling oxide, which can reduce the power consumption.

STDP is an essential type of the learning process in the human brain, which describes the dependence of synaptic weight modulation on the relative time difference between the pre- and postsynaptic spikes.[107,110] Taking one kind of STDP as an example, if the post-synaptic spike is behind the pre-synaptic spikes temporally within a few hundred milliseconds, the synaptic weight will get stronger. Conversely, if the relative temporal order is reversed, the synaptic connection strength will be weakened. Paul et al. reported a type of FG MoS$_2$ synaptic transistor for the emulation of STDP.[168] Graphene between hexagonal boron nitride (hBN) and SiO$_2$ is used as FG. hBN is used as a tunneling layer. As shown in Figure 13a, in the emulation of STDP behaviors, pre- and post-synaptic pulses are applied on the Si$^{++}$ gate through multiplexer in a temporal sequence. The conductance of

Figure 11. a) A schematic structure of an FG transistor. b) Energy band diagram of FG transistors in flat band state. c) Energy band diagrams of hole injection from channel to the FG. d) Energy band diagrams of electron injection from channel to the FG.
the channel is readout by applying a voltage pulse on Si\textsuperscript{++} gate. Figure 13b shows the percentage change in the channel conductance ($\Delta G$) with the relative time interval between pre- and post-synaptic pulses ($\Delta t$). The percentage change in the channel conductance is larger with smaller relative time interval between pre- and post-synaptic intervals.

ANNs excel in areas such as pattern recognition and economic prediction. A crossbar array architecture is used to accelerate the neural network training. An M$\times$N synaptic device crossbar array can emulate an M$\times$N synaptic weight array. He et al. proposed a type of IGZO FG synaptic transistors for the emulation of neural networks.\cite{167} Al$_2$O$_3$ and ITO are used as the tunneling oxide and FG layer. The neural network simulation was performed by CrossSim simulator with Python code. As shown in Figure 14a, the ANN contained three layers. Figure 14b shows the crossbar array of the FG synaptic transistors. The crossbar array can act as “neural core” to perform vector matrix multiplication and parallel rank 1 outer-product update. Three datasets were used to evaluate the neural networks. Figure 14c–e shows the accuracy of training a neural network using the FG transistors and the simulation result of the ideal theoretical numeric accuracy. The simulated neural network based on the FG devices shows almost the same accuracy as the ideal theoretical numeric accuracy. For example, for small digits, the simulated neural network shows a classification accuracy of 95.7%, whereas the ideal accuracy is 96.8%.

6. Conclusions and Prospects

Transistor-based neuromorphic devices have shown great potential for developing future brain-like computing. We have reviewed the recent progress of the transistor-based neuromorphic devices, including ion-gate neuromorphic transistors, ferroelectric-gate neuromorphic transistors, and FG neuromorphic transistors. With the modulation gates, transistor-based neuromorphic devices can flexibly achieve the emulation of synaptic and neuronal functions. Table 1 shows the performance of different types of neuromorphic transistors.

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**Figure 12.** a) Diode configuration wiring scheme of the memflash device to realize the memristive operation mode. b) Experimental and simulated conductance modulation by 175 potentiation pulses (+10 V) and 175 depression pulses (−7.5 V) with different pulse durations. c) Calculated conductance for different tunneling oxide thicknesses modulated by 175 potentiation pulses and 175 depression pulses with the time duration of 3 ms. Reproduced with permission.\cite{174} Copyright 2014, IOP Publishing.

**Figure 13.** a) Schematic diagram of the device for STDP. b) Asymmetric STDP realized in MoS$_2$-based synaptic transistor. Reproduced with permission.\cite{168} Copyright 2019, IOP Publishing.
Ion-gate transistors usually operate at a low voltage due to the extremely large EDL capacitance, which is favorable for the implementation of neuromorphic devices with very low energy consumption. The relaxation of the ion in the gate electrolyte

Table 1. Performance of different types of neuromorphic transistors.

| Transistor type     | Gate dielectric layers | Channel material | Spike voltage | Spike duration | Per spike energy consumption | Function or application                          | Ref. |
|---------------------|------------------------|-------------------|---------------|---------------|------------------------------|------------------------------------------------|------|
| Ion-gate transistor | PEG                    | CNT               | 5 V           | 1 ms          | 7.5 pJ                       | EPSC; PPF                                      | [122]|
|                     | LiClO₄ in PED          | Graphene          | –             | 10 ms         | 500 fJ                       | Long-term potentiation; LTD; STDP               | [123]|
|                     | PVA                    | MoS₂              | 1 V           | 10 ms         | 23.6 pJ                      | Dynamic filter; neural coding and neuronal gain modulation | [124]|
|                     | Nano-granular SiO₂     | IZO               | 0.3 V         | 10 ms         | 45 pJ                        | Spatiotemporal signal processing               | [52] |
|                     | Chitosan               | IGZO              | 2 V           | 25 ms         | 1 nJ                         | Dendrite recognition; spatiotemporal information processing | [79] |
| Ferroelectric-gate transistor | KCl electrolyte    | PEDOT:PSS         | 0.5 V         | 100 ms        | –                            | PPF; dynamic filter                            | [54] |
|                     | PZT                    | ZnO               | 2 V           | 40 μs         | –                            | STDP                                          | [189]|
|                     | P(VDF-TrFE)            | IGZO              | 20 V          | 10 ms         | –                            | EPSC                                          | [190]|
|                     | P(VDF-TrFE)            | Pentacene         | ≥10 V         | 500 ms        | 37.95 nJ                      | EPSC; STDP                                   | [160]|
|                     | HfZrOₓ                 | Si                | 3.7 V         | 100 μs        | –                            | Potentiation; depression                       | [163]|
|                     | HfZrOₓ                 | IGZO              | ≥2            | 10 ms         | –                            | Potentiation; depression                       | [166]|
| FG transistor       | SiO₂/graphene/hBN      | MoS₂              | –4 V/+3 V     | 100 ms        | ≈20 pJ                       | STDP                                         | [168]|
|                     | Al₂O₃/ITO/Al₂O₃        | IGZO              | –4 V/+4 V     | 25 ms         | 0.4 pJ                       | Neural network simulation                     | [167]|
|                     | SiO₂/graphene/hBN      | MoS₂              | –7 V/+7 V     | 100 ms        | –                            | Synaptic weight modulation                     | [191]|
|                     | Si                     | –7.5 V/+10 V      | 3 ms          | –              | Synaptic weight modulation    | [174] |

Figure 14. a) A schematic diagram of an ANN. b) Demonstration of a hardware implemented synaptic weight crossbar array with the IGZO-based FG synaptic transistors. c–e) Classification accuracy as a function of the training epoch for Optical Recognition Handwritten Digits, MNIST, and Sandia file classification datasets. Reproduced with permission.[167] Copyright 2020, IOP Publishing.
enables the ion-gate transistor to simulate the dynamic characteristics of the biological neural systems, which enables the ion-gate synaptic transistors to emulate the short-term synaptic plasticity effectively. Due to strong lateral coupling effect, multi-gate structures enable the ion-gate neuromorphic transistors to achieve the dendritic integrations of neurons. However, most studies only emulate synaptic and neuronal functions by single device. More importantly, how to carry out integrated ion-gate neuromorphic transistor networks in the future may also bring some problems, such as interconnection of transistors, overall energy consumption, and pulse timing under parallel operation. Ferroelectric-gate and FG neuromorphic transistors have realized multi-level channel conductance, long-term plasticity, STDP, and the simulation of ANNs. Ferroelectric-gate transistors hold the advantage of high-speed operation. The neuromorphic devices based on FG transistors may be fabricated using the standard CMOS technology and integrated in three dimensions. However, ferroelectric-gate transistors as well as FG transistors have difficulty in emulating the short-term synaptic plasticity because of its non-volatile memory characteristics. Ferroelectric gate/FG and ion-electrolyte mixture gate dielectrics may be a good solution to solve this problem. In the emulation of ANNs, linear and symmetrical conductance modulation characteristics are also required,[185] which may be improved through device engineering.[94]

Currently, a lot of works have been done at the device level. Different types of neuromorphic devices cannot be simply compared considering the numerous factors, such as structures, materials, and application scenarios. For the application of the in-memory computing based on crossbar arrays, there are several required metrics of the transistor-based synaptic devices. The desired characteristics include small device size (<1 μm² for compact arrays), multiple conductance states (∼100 separable states, or ∼6 bit), linear and symmetric conductance tuning, low energy consumption (< 1 pJ per switching event), low switching noise (< 0.5% of weight range), etc.[186] For the application of faithful brain-like spike dynamic computing, the current work is still in its infancy. The required metrics of the devices in this field need to be further explored and defined.

Brain-inspired energy efficient computing based on neuromorphic devices has made considerable progress. Excitingly, we may directly couple artificial neuromorphic transistor circuits to biological structures. Prosthetic synaptic junction based on the artificial biohybrid synapse could be used for repairing chemical communication between neurons in the future, contributing to the neuro-rehabilitation.[187] We may be able to repair the damaged nervous system at the neuronal and synaptic level using artificial neuromorphic devices. Furthermore, combining the external sensor systems and the artificial synaptic and neuronal information processing system then through bio-interfacing engineering will contribute to prosthetics.[188]

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**Conflict of Interest**

The authors declare no conflict of interest.

**Keywords**

ferroelectric-gate transistors, floating-gate transistors, ion-gate transistors, neuromorphic devices, neuromorphic systems, neuromorphic transistors

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