A simple 24-second timer design for basketball games

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Abstract. In recent years, basketball has been very popular among students, based on the knowledge learned in the course, this paper designed a "basketball game 24 seconds timer design", which can be completed: display 24 seconds countdown; system set external operation switch, control the timer direct zero, start and pause/continuous function. When the counter is decreasing in 24 seconds, the timing interval is 1 second; when the timer decreases to zero, the digital display shows zero and an audible and visual alarm signal is issued. The whole circuit is designed with the help of the theoretical knowledge related to digital circuits and the simulation of the circuit is completed using Proteus software to obtain the expected results.

1. Design Background
Timers can be used in many fields, such as timed alarms, traffic lights, countdown timers in games, and also as a reminder to administer medication at specified times for various to play, capsules, etc. This shows that timers are very commonly used in modern society. In the game of basketball, it is stipulated that a player cannot hold the ball for more than 24 seconds, otherwise it is against the law. Therefore, the "24-second timer design for basketball" can be used to limit the time a player can hold the ball to 24 seconds. Once the player has held the ball for more than 24 seconds, it automatically alerts the player to the infringement.

2. Programme design

2.1. Design ideas
The main functions of the basketball competition timing system include: a 24 second countdown and an end of time alarm. When the game is ready to start, the word 24 is displayed on the screen and when the game starts, the countdown is counted down from 24 to 00 second by second. the counting module is mainly implemented using the 74LS192. When the counter reaches zero, a beep is given.

The design of this timer is modular and consists of 3 main components, namely the timing module, the control module, and the decoder display module. The modular design philosophy used in the design of this timer makes the design simpler, easier and faster. The basketball competition 24 second timer circuit is based on the main functions of clock signal generation, countdown counting, decoding display and alarm.

2.2. Programme design
The 24-second counter circuit consists of five main modules: a second pulse generator, a counter a decoder display circuit, an alarm circuit and a control circuit the main modules of the system are the count
er and the control circuit. The counter completes the 24-second timer, while the control circuit is responsible for the direct clearing of the counter, the start of the count, the pause/continuous count, the display and extinguishing of the decoder display circuit, and the start of the alarm when the timer time is up.

The signal generated by the second pulse generator is the circuit's clock pulse and timing standard. This circuit can be constructed using a 555 integrated circuit or a multi-tuned oscillator consisting of a TTL and non-gate. The decoder display circuit consists of a 74LS48 and a common cathode seven-segment LED display. The alarm circuit consists of a light emitting diode and a buzzer in the experiment. The 24-second counter chip of the main circuit shares a switch for the set and clear terminals. Once the race has started, the countdown timer starts counting down from 24 seconds to 0. When the timing circuit is in the "00" state, a cut-off signal is given by a combinational logic circuit, which allows the signal and the clock pulse signal to cut off the clock through a gate, causing the timer to stop when it reaches 0. The circuit diagram for this design is shown in Figure 1.

A second pulse from the 555 timer with a ten-bit (high) debit output is input to the down terminal of counter U3 via a sum logic as a decimal pulse. When the counter counts to 0, the debit pulse is output from pin (13) of U3 so that the ten-bit counter U2 starts counting. When the counter counts to "00", U2's (13) pin output debit pulse outputs a low level, and the 555 timer output second pulse through a with gate, so as to cut off the second pulse, so that it stops at "00", at the same time, the alarm circuit works. The light emitting diode lights up and the buzzer sounds. When SW2 is closed, U2 and U3 are valid to achieve the reset function, and when SW2 is disconnected, U2 and U3 are invalid to start normal counting. In the counting process, SW3 closed, so that the output signal of 555 timer output through and gate U7 truncated seconds signal, thus buy now pause function, when SW3 disconnected, and start normal counting.

3. part circuit design

3.1. Second pulse generation circuit
The generation of second pulses is done by an oscillating circuit consisting of a 555 timer. It consists internally of two voltage comparators, three equal series resistors an RS trigger, a discharge tube T and a power output stage. It provides two base voltages VCC/3 and 2VCC/3.
The function of the 555 timer is mainly determined by the two comparators. The output voltages of the two comparators control the state of the RS trigger and the discharge tube. If the voltage at the trigger input TR is less than VCC3, the output of comparator C2 is 0. The RS trigger can be set to 1 so that the output OUT = 1 if the voltage at the threshold input TH is greater than 2VCC/3. If the voltage at the threshold input TH is greater than 2VCC/3 and the voltage at TR is greater than VCC/3, then the output of C1 is 0 and the output of C2 is 1, which will set the RS trigger to 0 and make the output low. The pin diagram of the 555 chip is shown in Figure 2.

![Figure 2. 555 chip.](image)

The second pulse generation circuit is shown in Figure 3. The two resistors are 20kΩ and 62kΩ respectively, allowing the 555 timer to generate a pulse with a period of 1s.

![Figure 3. Second pulse generation circuit.](image)

### 3.2. Countdown circuit
The main devices used in the 24-second countdown circuit are the 74LS48, 74LS92 and the digital tube.

The 74LS48 is a 7-segment display decoder with a valid high level output. It operates at 5V and is used to drive common cathode digital tubes. 74LS48 has not only the input (DCBA) and output (Ya–Yg) terminals for the basic functions of a display decoder, but also a test input (LT) and a dynamic zero-out input (RBI), as well as a fading input/dynamic zero-out output (BI/RBO) terminal for both input and output functions. The pin diagram for the 74LS48.

The 74LS192 is a synchronous decimal reversible counter with dual clock inputs and functions such as clear and reset. 74LS92 pinout diagram is shown in Figure 4. Its breakout includes a reset terminal, an add counter terminal, a subtract counter terminal, a non-synchronous input output, a non-synchronous debit output, an input terminal, an output terminal and a clear terminal.
Figure 4. 74LS192 pinout diagram.

The main part of this part of the circuit operates with the input of a clock pulse, which is analysed in detail below.

The way to achieve the countdown function of the counter is to use two pieces of 74LS192 to do the countdown counter of the individual bits (low) and ten bits (high) respectively, and use the low bit of the debit output signal as the high bit of the clock pulse, while the external clock pulse signal is input to the down side of the individual bits (low), so as to achieve the countdown function of the circuit.

When the control circuit gives a low level (active level) to the count inputs of the two chips, it can set them to "24" and at the same time the zero terminal will be grounded. The specific circuit for the countdown timer circuit is shown in Figure 5.

Figure 5. Countdown circuit.

3.3. Control circuits

The control circuit is shown in Figure 6. In this circuit, the borrowed output of the ten bits (high bit) is used as the signal of the stop circuit, when the digital tube shows "00", i.e. the ten bits (high bit) output are low, at this time its borrowed output changes from high level to low level, and the output of the second pulse signal generation circuit is passed through a with logic, and then passed to the down side of the individual bits (This method truncates the second pulse signal and achieves the function of stopping at "00". In addition, when the counter is counting normally, the decimal (high) debit output remains high at all times, and when it is connected to the output of the second pulse generator circuit by an with logic, it is then passed to the individual (low) down terminal, which does not affect the second pulse input.

Using a switch and a with the non-gate, with the non-gate end connected high, the other end through a 1kΩ resistor then connected high, while connected to the switch end, the other end of the switch ground.
With the non-gate output and the two 74LS192 set terminal LOAD connected. When the switch SW2 disconnected, set the number of terminal for "1", at this time the set number of terminal invalid, can count normally, when the switch SW2 closed, set the number of terminal for "0", at this time the set number of terminal valid, can be set to "24 ".

![Control Circuit](image)

**Figure 6.** Control circuit.

### 3.4. Alarm circuits

The alarm circuit is shown in Figure 7. When the circuit is displayed as "00", the use of ten bits (high) of the debit output for "0", plus a non-gate to achieve the work of light-emitting diodes.

![Alarm Circuit](image)

**Figure 7.** Alarm circuit.

### 4. Commissioning and testing

#### 4.1. Faults and solutions during commissioning

After the circuit has been roughly completed, commissioning is required to check the circuit. It is not uncommon for faults to occur during the debugging process. After completing the drawing of this circuit, a simulation was carried out and it was found that the counting period did not match what was expected and that the numbers on the digital tube jumped quickly. From the previous steps taken when designing the circuit, it was clear that the counting period was related to the second pulse generation circuit and that the period was determined by the size of the resistor and capacitor. On inspection, it was found that the size of the capacitor was different from the value calculated during design. After changing the capacitance value to the calculated value, the count period was consistent with the expectation.
4.2. Commissioning and operating results

Using the Proteus circuit simulation software, the circuit is connected for simulation.

When SW2 is closed, U2 and U3 are valid for the reset function, as shown in Figure 8.

![Figure 8. Implementing the reset function.](image1)

When SW2 is disconnected again, U2 and U3 are invalidated at the counting end and start counting normally, as in Figure 9.

![Figure 9. Start of normal counting.](image2)
In the counting process, SW3 closed, so that the 555 timer output output signal through with the gate U7 truncated seconds signal, so as to buy now pause function, when SW3 disconnected, and began to count normally. When SW1 is closed, zeroing is achieved, as in Figure 10

![Figure 10. General Circuit Diagram.](image)

5. Summary
The timer designed in this paper runs in simulation, when SW2 is disconnected, the U2 and U3 set count terminals are valid to achieve the reset function, and then when SW2 is closed, the U2 and U3 set count terminals are invalid and start counting normally. In the counting process, SW3 closed, so that the output signal of 555 timer output terminal through and gate U7 truncated seconds signal, thus buy now pause function, when SW3 disconnected, and start normal counting. When SW1 is closed, zero is achieved. In this way, the basketball timer function designed in this paper is realized. This timer can be applied in small-scale class basketball games and campus basketball games.

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