Transverse Scaling of Schottky Barrier Charge-Trapping Cells for Energy-Efficient Applications

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Abstract: This work numerically elucidates the effects of transverse scaling on Schottky barrier charge-trapping cells for energy-efficient applications. Together with the scaled gate structures and charge-trapping dielectrics, variations in bias conditions on source-side injection are considered for properly operating Schottky barrier cells in low-power or high-efficiency applications. A gate voltage of 5 to 9 V with a drain voltage of 1 to 3 V was employed to program the Schottky barrier cells. Both the non-planar double-gate gate structure and scaled dielectric layers effectively improve the source-side programming. When the gate voltage of 5 V was operated, there were roughly two orders of magnitude greater injected gate currents observed in the ONO-scaled double-gate cells. Five successive programming-trapping iterations were employed to consider the coupling of trapped charges and Schottky barriers, examining the differences in physical mechanisms between different design options. The gate structures, dielectric layers, and gate/drain voltages are key factors in designing transverse scaled Schottky barrier charge-trapping cells for low-power and high-efficiency applications.

Keywords: Schottky barrier; source-side injection; charge-trapping memory; energy-efficient; non-planar double-gate; high-k dielectrics

1. Introduction

Nonvolatile flash memory has become one of the mainstream memories in the semiconductor industry because of the rapid growth of demands for portable and automobile electronics [1–3]. Recently, advances in deep learning and computing technology have made possible the complex internet of things (IOT) and artificial intelligence (AI) applications. Nonvolatile memory-based in-memory or edge computing relies on energy-efficient parallel read cells for their successful applications in the oncoming AI and IOT era [4–8]. In conventional NOR-type flash cells, the drain-side channel hot-electron (CHE) programming suffers from the compromising between the gate and drain biases. Innovative source-side injection Schottky barrier cells eliminate the tradeoffs to provide a promising candidate for energy-efficient applications [9–14].

Low-power operations and high-efficiency performance are the key requirements for energy-efficient nonvolatile memories. Schottky barrier flash cells preserve compact stacked-gate structures as in traditional flash memories. However, for Schottky barrier cells, metallic Schottky barriers are formed in source/drain junction regions. The Schottky barrier cells present distinguish ambipolar...
conduction and source-side injection that are different to those of traditional counterparts [15–18]. Importantly, the scaling mechanism and considerations of Schottky barriers cells are dissimilar from the traditional drain-side injection CHE cells. The channel length scaling of Schottky barrier flash cells was considered previously [10], but the cell scalability of transverse gate stacks and proper minimizing operation biases are still unclear. The non-planar double-gate architecture and scaled high-k materials were fulfilled using CMOS FinFETs technology, while practical knowledge of applying them to Schottky barrier cells for energy-efficient memories remains inadequate [19,20].

This work elucidates the effects of scaling transverse gate structures and dielectric layers on source-side injection Schottky barrier charge-trapping cells. Together with transverse scaling, operation voltages are considered for low-power or high-efficiency applications. Two-dimensional device simulations [21] were employed to investigate the cell characteristics. Successive injection-trapping iteration processes [22,23] were used to investigate the coupling of Schottky barriers and trapped charges during programming, and to explore the differences of reading/programming mechanisms between the scaled and non-scaled Schottky barrier cells. Section 2 details the cell structures and parameters used in numerical simulations. Section 3 explores the effects of using non-planar double-gate structures and scaled charge-trapping layers on current transport and source-side injection. Section 4 investigates the variations of bias conditions on the source-side injection programming of non-planar double-gate Schottky barriers cells. Key device design factors are illustrated to select proper operation voltages. Section 5 examines the simulated results of programming and reading in Schottky barrier charge-trapping cells using successive injection-trapping iterations. Comparisons of cell characteristics were made between the low-power and high-efficiency design options.

2. Device Structures and Numerical Parameters

Figure 1 depicts the schematic structures of (a) traditional single-gate and (b) non-planar double-gate Schottky barrier charge-trapping cells, where a typical silicon-oxide-nitride-oxide-silicon structure was employed. To reduce the numerical simulations to a manageable level, double-gate cells were considered to represent the non-planar FinFET or nanowire-type device cells. Practical approaches to fabricate non-planar Schottky barrier cells can be found in Refs [11,12,24]. Two multi-oxide/nitride/oxide (ONO) layers of 5/6/7 and 3/4/5 nm were used to represent the non-scaled and scaled charge-trapping dielectric layers, which were used in recent charge-trapping cells [25–27]. The equivalent oxide thickness (EOT) of the non-scaled and scaled examples was roughly 15 and 10 nm, respectively. When high-k materials were employed, their equivalent ONO layers were considered here. The dielectric constant of oxide is 3.9 and nitride is 7.5. The detailed material properties of dielectric oxide and nitride layers can be found in Ref. [21]. Long-channel 180 nm cells with fully aligned, uniform junction profiles were utilized to focus on studying the inherent cell characteristics. An n+ workfunction gate and a junction depth, or a silicon body thickness, of 10 nm were employed with a p-type substrate of $1 \times 10^{17}$ cm$^{-3}$. In subsequent studies, the electron current was operated in cell reading and programming.

Two-dimensional device simulations were performed using the thermionic emission and Wentzel–Kramers–Brillouin-based tunneling models [9,21,28,29]. An electron Schottky barrier height of 0.4 eV was employed in metallic source/drain junctions to represent the conventional silicidation workfunction using CMOS technologies [17,30,31]. The detailed discussion of physical Schottky barrier models used in numerical simulations can be found in Ref. [9]. To evaluate the behavior of the source-side electron injection, the impact ionization, lucky-electron, and band-to-band tunneling models were considered to predict the injected gate currents [32–35].
Figure 1. Schematic structures of (a) traditional single-gate and (b) non-planar double-gate Schottky barrier charge-trapping memory cells.

3. Gate Structures and Scaled Dielectrics

3.1. Drain and Gate Currents

Figure 2 shows the electron drain currents of single- and double-gate Schottky barrier charge-trapping cells at a drain voltage ($V_d$) of 1 V, in which the multi-ONO layers of 5/6/7 and 3/4/5 nm were used. The threshold voltage, on–off switching, and on-state electron current rely highly on both the gate structures and dielectric ONO layers. The use of a non-planar double-gate structure or scaled ONO layers improves the driving currents and on–off switching of Schottky barrier cells because of the stronger gate control on the Schottky source barriers. At low gate voltages, the non-planar double-gate cell with minimized dielectric layers can produce one to three orders of magnitude higher drain currents than the single-gate, non-scaled dielectrics cell. At higher gate biases, the scaled non-planar double-gate cell ensures nearly an order of magnitude stronger drain current than the single-gate counterpart.
Figure 2. Simulated drain currents of single- and double-gate Schottky barrier charge-trapping cells with multi-ONO layers of 5/6/7 and 3/4/5 nm at a reading drain voltage of 1 V.

Figure 3 presents the injected gate currents of single- and double-gate Schottky barrier charge-trapping cells with multi-ONO layers of 5/6/7 or 3/4/5 nm at a programming drain voltage of 3 V. From the results shown in Figures 2 and 3, the degree of the gate current enhancement caused by the scaled structures and dielectrics is larger than that of the drain current enhancement, particularly at low gate voltages. When the gate voltage is less than 5 V, there are two to five orders of magnitude greater injection currents observed in the double-gate, ONO-scaled cell, by comparing with the non-scaled single-gate cell. Importantly, such a strong gate current enables an efficient high-efficiency programming, or a substantial reduction in programming gate voltages, in the ONO-scaled double-gate cells. For example, a much smaller gate voltage, such as 4 V, can be utilized in the scaled double-gate cells to ensure a sufficient gate current that is injected in the non-scaled single-gate cell at a programming gate voltage of 9 V.

Figure 3. Numerical gate currents of single- and double-gate Schottky barrier charge-trapping cells with multi-ONO layers of 5/6/7 and 3/4/5 nm at a programming drain voltage of 3 V.

The increased gate currents in the ONO-scaled double-gate cells are caused by the higher electron current and the improved injection efficiency. Figure 4 sketches the injection efficiency of
Schottky barrier charge-trapping cells at a programming drain voltage of 3 V. At low gate voltages, the ONO-scaled double-gate cell can produce much higher efficiency of hot-electron injections than the non-scaled single-gate counterpart. The application of a non-planar double-gate structure or scaled ONO layers in Schottky barrier cells ensures a sufficient hot-electron injection at a smaller programming voltage. However, when the gate voltages are sufficiently high, the enhancement of the injection efficiency by either a double-gate structure or scaled dielectrics is gradually saturated. In such a circumstance, the increase in the gate current is mainly attributed to the raised drain currents. It implies that when the gate voltages are sufficiently high to secure low-resistance Schottky tunnel barriers, the source-side lateral electric field reaches its maximum value to result in a similar injection efficiency.

![Figure 4](image-url)  
**Figure 4.** Injection efficiency of single- and double-gate Schottky barrier charge-trapping cells with multi-ONO layers of 5/6/7 and 3/4/5 nm at a programming drain voltage of 3 V.

### 3.2. Source-Side Injection

Figure 5a sketches the conduction band diagrams of single- and double-gate Schottky barrier cells along the channel surface at a programming gate voltage of 9 V. It can be found that all four types of Schottky barrier cells resemble source-side band-bending of the conduction band diagrams. The source-side electric field depends mildly on the gate structure or dielectric thickness at the relatively high gate voltage of 9 V. Figure 5b displays the conduction band diagrams of Schottky barrier charge-trapping cells at a programming gate voltage of 2 V. Notably, the source-side bending of conduction band diagrams relies highly on both the gate structures and dielectric layers. At the smaller gate voltage of 2 V, the double-gate cells produce a relatively abrupt source-side band bending to enable a high-efficiency injection. For hot-carriers injection programming, the injected probability of the “lucky-electrons” relies highly on the hot carriers that can vertically turn to surmount the dielectric barriers [16,33]. In the Schottky barrier cells, the source-side hot carriers that can gain enough energy laterally to pass over the tunneling dielectric depend exponentially on the lateral electric field around the source-side region [16]. Since the high-efficiency injections can be attained at relatively low gate voltages using the double-gate structures, the bias conditions to proper operating source-side injection double-gate cells will be examined intensively in Section 4.
Figure 5. Conduction band diagrams of single- and double-gate Schottky barrier charge-trapping cells along the channel surface at gate voltages of (a) $V_g = 9\, V$ and (b) $V_g = 2\, V$.

Figure 6 sketches the lateral distributions of injection currents in the single- and double-gate Schottky barrier cells with ONO layers of $5/6/7$ or $3/4/5$ nm. In these examples, the charge-trapping cells were operated at programming voltages of $V_g = 9\, V$ and $V_d = 3\, V$. The ONO-scaled double-gate cell enables the larger injection of source-side hot electrons with a tight distribution. For the peak injection, it offers roughly ten times higher injection than the single-gate cell with non-scaled dielectrics. Since these Schottky barrier cells exhibit similar source-side conduction band diagrams, as shown in Figure 5a, the distributions of injection currents vary weakly away from metallic source junctions. Notably, both the minimization of dielectric layers and the application of the double-gate structure improve the source-side injection programming of Schottky barrier charge-trapping cells. However, the substantial increase in injection currents using the double-gate or scaled dielectrics is mainly attributed to the raised drain currents because of a stronger gate control.
Figure 6. Distributions of electron injection currents in single- and double-gate Schottky barrier cells at programming voltages of $V_g = 9$ V and $V_d = 3$ V.

4. Operation Voltages of Scaled Cells

4.1. Drain Voltage

In this section, the scaled ONO layers of 3/4/5 nm were employed to examine the effects of bias conditions on the source-side injection programming of double-gate Schottky barrier charge-trapping cells. Figure 7 displays the numerical results of current–voltage curves in scaled double-gate Schottky barrier cells at drain voltages from 1 to 3 V. The Schottky barrier cells generate a smaller drain current level than the conventional drain-side CHE cells because of the Schottky barrier formed at the source/channel interface. As shown in Figure 2, the use of the double-gate structure and scaled charge-trapping layers increases the electron driving currents. In the ONO-scaled double-gate Schottky barrier cells, the on-state drain current is larger at a higher drain voltage, but it starts to saturate as the drain voltage drops to around 2 V. The drain voltage weakly affects the on–off switching of double-gate Schottky barrier cells. However, interestingly, a considerable off-state hole current can be triggered in Schottky barrier cells when the drain voltage is too high ($V_d = 3$ V) due to the lower drain Schottky hole barrier. A mild drain voltage of 1 to 2 V can be utilized in cell reading to optimize both the on- and off-current.

Figure 7. Numerical results of drain currents in scaled double-gate Schottky barrier charge-trapping cells as a function of gate voltage at drain voltages from 1 to 3 V.
Figure 8 shows the injection efficiency of double-gate Schottky barrier charge-trapping cells with various drain voltages. A higher drain voltage produces a larger injection efficiency during cell programming. Since the drain-induced lateral field affects the distributions of Schottky source barriers after the cell devices turn on, the injection efficiency varies with the applied drain voltages. However, the enhancement of the injection efficiency produced by a larger drain voltage is gradually reduced from 1 to 3 V, similar to the drain current shown in Figure 7. It implies that a low drain voltage of 2 V is sufficient to ensure a high-efficiency injection in double-gate Schottky barrier cells during cell programming.

![Figure 8. Injection efficiency of scaled double-gate Schottky barrier charge-trapping cells as a function of gate voltage with various drain voltages.](image)

Figure 9 sketches the conduction band diagrams of double-gate Schottky barrier cells along the channel surface with various drain voltages. Unlike the drain-side band bending observed in traditional drain-side CHE cells, drastic conduction band bending occurs around the source-side region in Schottky barrier cells at relatively small drain voltages. Even at a low drain voltage of 1 V, the Schottky source barrier can induce abrupt band bending and a strong electrical field around the source-side region to enable sufficient source-side hot electrons for programming. The higher drain voltage is the more abrupt source-side bending, and thinner Schottky source barriers are induced. Since both the drain current and injection efficiency rely on the profile of Schottky source barriers, the drain current and injection efficiency increase as the drain voltages rise. Notably, the use of the higher drain voltages results in a stronger, and also wider, high-field region for efficient source-side injection.

![Figure 9. Conduction band diagrams of scaled double-gate Schottky barrier charge-trapping cells along the channel surface at various gate and drain voltages.](image)
Figure 10 compares the numerical results of distributions of electron injection currents in double-gate Schottky barrier cells with various drain voltages. In addition to the conduction and injection, the drain voltage plays a key role on controlling the locations of injected electron charges. Since the high-field region is much extended at a larger drain voltage, the 3 V Schottky barrier cell has a considerably wide distribution of the injection current than other counterparts. The effects of the distribution of the source-side injection on cell characteristics will be investigated further using the method of successive injection-trapping iterations.

![Figure 10](image-url)

**Figure 10.** Distributions of electron injection currents in scaled double-gate Schottky barrier cells with various drain voltages at gate voltages of (a) $V_g = 9$ V and (b) $V_g = 5$ V. There are two different axis scales for the two conditions of gate voltages in the vertical axis.

### 4.2. Gate Voltage

In Schottky barriers charge-trapping cells, the conduction and source-side injection of electron carriers depend strongly on the gate voltage as well as the drain voltage. Figure 7 shows the drain currents in scaled double-gate Schottky barrier cells as a function of the gate voltage. For Schottky barrier devices, the mobile carriers thermionically emit over or tunnel through the Schottky source barrier, contributing to the electron drain current. For the scaled Schottky barrier cells, the strong gate-controlled field can induce the source-side band bending earlier to generate efficient Schottky barrier tunneling at a smaller gate voltage. A low gate voltage of about 1 V is sufficient to enable considerable electron channel carriers to pass through the Schottky source barrier. After the cell device turns on, the drain current increases mildly as the gate voltages rise.

Figure 11 presents the distributions of electron injection currents in scaled double-gate Schottky barrier cells with various gate voltages from 5 to 9 V. The larger gate voltage generates a higher injection current in the double-gate Schottky barrier cells. The increase in injection current is coming from both the raised drain current and the enhanced injection efficiency. As shown in Figure 8, the injection efficiency in scaled Schottky barrier cells is a function of the gate voltage. The higher gate voltage is associated with the stronger injection efficiency. Notably, the improved injection efficiency is caused by the redistribution of the channel potential across the Schottky source and drain barriers. Figure 9 sketches the conduction band diagrams of double-gate Schottky barrier cells along the channel surface at two gate voltages of 5 and 9 V. At the higher gate voltage of 9 V, the stronger gate-controlled field results in the more abrupt Schottky source barrier to produce a larger electron drain current. It enables a higher lateral electric field to a stronger source-side injection, also narrowing the distribution of the hot-electrons injection. Figure 10 compares the numerical results of distributions of injection currents in scaled double-gate Schottky barrier cells at gate voltages of (a) 9 and (b) 5 V. Notably, in these examples, there are two different scales for the two conditions of gate voltages in the vertical axis.
The use of the higher programming gate voltage of 9 V produces an increased injection current and a relatively tight distribution because of the enhanced lateral field.

![Figure 11. Distributions of electron injection currents in scaled double-gate Schottky barrier cells with various gate voltages from 5 to 9 V ($V_d = 2$ V).](image)

5. Low-Power and High-Efficiency Cells

5.1. Successive Injection-Trapping Iterations

For the single- and double-gate Schottky barrier charge-trapping cells, the coupling of trap charges and Schottky source barriers produces unique Schottky barrier lowering, and the charge-coupled Schottky barriers must be considered concurrently with the bias conditions during the source-side injection programming. Successive injection-trapping iterations were employed subsequently to evaluate the cell programming and reading properly. The whole programming period was partitioned into five evenly divided intervals. The detailed discussion of the numerical method to estimate charge-trapping mechanisms can be found in Refs. [22,23]. Two cases of Schottky barrier charge-trapping cells were compared subsequently: (1) ONO-scaled double-gate and non-ONO-scaled single-gate cells with similar peak injection currents; and (2) low-power and high-efficiency double-gate cells.

5.2. Scaled Double-Gate and Non-Scaled Single-Gate Cells

In this subsection, the cell characteristics of ONO-scaled double-gate cells are compared with those of the non-ONO-scaled single-gate cells. A low gate voltage of 5 V with a mild drain voltage of 2 V was employed to program the scaled double-gate cells because of its enhanced injections, whereas a gate voltage of 9 V with a drain voltage of 3 V was used in the non-scaled single-gate counterparts. Under such circumstances, the peak values of injection currents are selected to be roughly identical at each programming interval.

Figure 12a depicts the iterative results of the spatial distribution of injection currents in the two types of Schottky barrier cells at each programming interval. The presence of trapped charges adjusts both the transverse and lateral electric field to alter the subsequent distributions of hot-electron injections. Thus, the injection currents are varied at each interval accordingly. Both in the single- and double-gate cells, the injection currents decrease from the first to the last interval. Notably, the peak injections in the two cells are roughly identical at each interval, but the injection currents in the single-gate cell are widely distributed. The total accumulated trap charges are relatively large in the non-scaled single-gate cell. Figure 12b displays the associated conduction band diagrams of Schottky barrier cells along the channel surface at the initial and the fifth programming intervals. The two
Schottky barrier cells exhibit a resembled abruptness of source-side band bending to have similar peak injections. However, the double-gate cell has a shorter high-field region. The distributions of hot-electron injections and relevant trap charges are relatively confined near the source-side region in the scaled double-gate cells.

Using the distributions of trapped charges after the successive programming intervals, Figure 13a presents the current–voltage curves of programmed Schottky barrier cells at reading voltages of 1 V. Both Schottky barrier cells enable appropriate threshold voltage shifts to detect the memory states of programmed cells. Notably, the threshold voltage shifts and the subthreshold swing degradations in the double-gate cells are relatively mild by comparing with those in the single-gate counterparts. The differences in reading characteristics between the two cells are attributed to the distributions of trap charges and the gate-controlled field at reading. The gate-controlled field in the single-gate cells is too weak to lower the charge-coupled Schottky source barrier, generating a small drain current. After the successive programming intervals, the variations in the threshold voltage shifts and subthreshold swing are more pronounced because of the larger trap charges.
Figure 13. (a) Reading currents of two types of Schottky barrier charge-trapping cells after each programming interval ($V_{\text{read}} = 1$ V); (b) associated conduction band diagrams of Schottky barrier cells along the channel surface at reading bias conditions.

Figure 13b sketches the associated conduction band diagrams of these two Schottky barrier cells along the channel surface at identical reading bias conditions. In these examples, the conduction band diagrams were shown at the initial and after the first and last programming intervals. In the scaled double-gate cells, the initial source-side band bending is abrupt to produce a fast on–off switching. After the last injection, the abruptness of source-side band bending is mildly modified to ensure a sound switching of the drain current. As for the single-gate cells, the weaker gate-controlled field induces a smoother source-side band bending at the initial condition. After the iterations, the strong coupling of trap charges and Schottky barriers considerably widens the Schottky source barriers to generate apparent swing-degraded current–voltage curves. Relatively, the ONO-scaled double-gate cell is insensitive to accumulated trap charges, requiring more injections for a favorable threshold voltage shift.

5.3. Low-Power and High-Efficiency Cells

This subsection examines the cell characteristics of low-power and high-efficiency options of scaled double-gate cells with ONO layers of 3/4/5 nm. A low gate voltage of 5 V with a mild drain voltage of 2 V was utilized to represent the low-power cells, whereas a gate voltage of 9 V with a
drain voltage of 3 V was employed in the high-efficiency cells. The programming interval in the high-efficiency cells is reduced to be one tenth of the counterpart cells for comparison.

Figure 14a plots the iterative results of the spatial distribution of injection currents in the two Schottky barrier cells at each programming interval. In these examples, two different scales are displayed for the injection currents in the vertical axis. Both in the low-power and high-efficiency Schottky barrier cells, the injection currents are decreased as the injection time is increased from the first to the last interval. However, the high-efficiency cell offers a slight decrease in injection currents for its strong gate-controlled field. The coupling of Schottky barriers and trap charges is minimized under the large gate voltage of 9 V at each interval. Figure 14b sketches the associated conduction band diagrams of two Schottky barrier charge-trapping cells along the channel surface at the initial and the last programming intervals. The high-efficiency Schottky barrier cell retains the abrupt source-side band bending to ensure significant injection currents at the initial and the last programming intervals. Since the high-field regions are relatively extended into the channel, the source-side injections distribute widely in the high-efficiency Schottky barrier cells.

Figure 14. (a) Iterative results of spatial distributions of injection currents in two Schottky barrier cells. Two different scales adopted in the vertical axis. (b) Conduction band diagrams of programmed cells along the channel surface at the initial and 5th programming intervals.

Figure 15 presents the iterative results of the spatial distributions of trapped charges in the high-efficiency and low-power cells. One-tenth programming periods were utilized in the high-efficiency cell at each interval because of its strong injection current. Notably, the trapped
Charges in the high-efficiency cell are accumulated faster due to the mild decrease in injection currents after iterations. Figure 16a shows the reading current–voltage curves of two programmed Schottky barrier cells after each programming interval. For Schottky barrier devices, the conduction current relies on Schottky source barriers. Thus, the reading characteristics are very sensitive to the presence of programmed trap charges. For the high-efficiency condition, the cell device retains a similar subthreshold swing of current–voltage curves, whereas it produces larger threshold voltage shifts because of more trapped charges. Figure 16b displays the associated conduction band diagrams of the two programmed cells along the channel surface at identical reading bias conditions. In these examples, the conduction band diagrams were plotted at the initial and after the last programming intervals.

For the high-efficiency cell, the lowering of the Schottky source barrier is considerably influenced by the accumulated trapped charges to have apparent threshold voltage shifts after iterations. Differently, the trapped charges in the low-power cells mildly affect the Schottky source barrier after programming, generating a mild variation in band diagrams. The low-power cell produces less injections to trap charges, requiring more programming time for a favorable threshold voltage shift.

**Figure 15.** Iterative results of spatial distributions of trapped charges in two options of scaled double-gate Schottky barrier cells. One-tenth programming periods were employed in the high-efficiency cells at each programming interval.

**Figure 16.** Cont.
6. Conclusions

This study elucidated the scaling of transverse gate-stacked structures on the source-side injection Schottky barrier charge-trapping cells. Both the double-gate structure and scaled ONO layers effectively improve the source-side programming, enabling the use of Schottky barrier cells in energy-efficient applications. A gate voltage of 9 V with a drain voltage of 3 V can be employed in high-efficiency double-gate cells. The programming intervals can be reduced to be one tenth of the non-scaled single-gate counterpart. For low-power options, a low gate voltage of 5 V with a mild drain voltage of 2 V can be utilized to operate the ONO-scaled double-gate cells.

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