Electrical characterization of MOS structures with self-organized three-layer gate dielectric containing Si nanocrystals

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Abstract. SiOx (x = 1.3) films with thicknesses of 50 and 100 nm deposited on c-Si by thermal evaporation of SiO in vacuum were subjected to N2 or two steps N2, 90%N2+10%O2 annealing at 1000 °C for 60 min. The time of the second (N2+10%O2) annealing step was varied in order to vary the depth to which the SiOx films were intentionally oxidized. The I-V and XTEM results obtained confirm that the suggested two steps annealing leads to a formation of three-layer SiO2/SiO2-Si nanocrystals/SiO2 gate dielectric, which contains Si nanocrystals. The nanocrystals are with a diameter of a ~ 4-5 nm and are embedded in a stoichiometric SiO2 matrix. The I-V measurement show that the current through the gate dielectric is limited by a SiO2 region, close to the top surface, formed during the second annealing step. MOS structures subjected to a two step annealing show larger retention times when charged with electrons/holes in comparison with the control or annealed only in N2 structures.

1. Introduction
Dielectric layers containing silicon nanocrystals (Si NCs) have attracted much attention in the recent years because they are promising for application in opto- and microelectronic devices. One possible application is in Si-based light sources [1,2]. The fabrication process of such a source would be compatible with the existing manufacturing infrastructure for silicon integrated circuits. Dielectric layers containing nanocrystals are also promising for usage in “third generation” solar cells [3]. Another possible application of Si nanocrystals is as charge storing nodes in non-volatile memory devices [4]. All these applications require a good knowledge of the structural and electrical properties of the films containing nanocrystals. Normally in non-volatile memory structures based on silicon nanocrystals the gate dielectric is composed of at least three different films: high quality tunnel silicon oxide (SiO2), another silicon oxide film, which contains nanocrystals (SiO2-Si NCs) and finally a third (control) SiO2 layer, which insulates the nanocrystals from the control gate. In most cases each of these layers is obtained in a different deposition system. Another approach is to vary the deposition conditions and/or gas ratio in order to vary the film composition. For example, SiO2/SiO2-Si NCs superlattice structures have been fabricated by thermal evaporation of SiO powder either under high vacuum or in low pressure of oxygen [5-7].
Our previous results [8-11] obtained by Transmission Electron Microscopy (TEM), infra red (IR) spectroscopy and X-ray Photoelectron Spectroscopy (XPS) have shown that furnace annealing of SiO$_x$ ($x = 1.15$ or 1.3, $d_{SiOx} \sim 15$ nm) films at 1000 °C in an inert gas ambient for 60 min causes phase separation and growth of Si nanocrystals in an amorphous matrix by a self-assembling process. The annealed samples exhibit nanocrystals with a diameter of $\sim 4-5$ nm ($x = 1.3$) or $\sim 5-6$ nm ($x = 1.15$) positioned almost in a single plane closer to the c-Si wafer than to the top surface and separated from the c-Si wafer/dielectric interface by an amorphous region with thickness $\geq 3$ nm [10,11]. It has been assumed that the Si nanocrystals grown in the region close to the top surface ($\sim 5-6$ nm) get transformed into SiO$_2$ due to native oxide formation after exposure to air. XPS has shown [10] that the spectra of the Si 2p core level of SiO$_x$ films with $x = 1.3$ changes significantly after high temperature annealing. In the annealed films the amount of excess Si atoms bonded to O in the suboxide network is strongly reduced and only clearly separated peaks corresponding to stoichiometric SiO$_2$ and to pure Si phase were observed. Combining the results obtained by TEM, IR and XPS it was concluded that the high temperature annealing leads to formation of Si nanocrystals in a stoichiometric SiO$_2$ matrix.

The obtained results motivated us to study the influence of an intentional oxidation step during the annealing process in order to fabricate a self-organized three-layer gate dielectric (SiO$_2$/SiO$_2$-Si NCs/SiO$_2$) structure in a controllable way and thus to avoid the deposition of the third SiO$_2$ control layer.

2. Experimental details

Metal-Oxide-Semiconductor (MOS) structures were fabricated by thermal evaporation of SiO at a vacuum of $1 \times 10^{-3}$ Pa on top of n-type crystalline silicon ($\rho = 4-6$ Ω cm). The deposited SiO$_x$ films were with composition of $x = 1.3$ and thicknesses of 50 and 100 nm. For each thickness four sets of samples were fabricated. The samples of the first set were annealed at 250 °C for 30 min in Ar only for stabilization (control samples), while those of the second set were subjected to an additional annealing at 1000 °C in pure N$_2$ atmosphere for 60 min. The 1000 °C annealing of sets 3 and 4 was carried out in two steps keeping the total annealing time equal to 60 min. The first step was an annealing in N$_2$ and the second step was annealing in 90% N$_2$ + 10% O$_2$ atmosphere. The N$_2$, 90%N$_2$+10%O$_2$ annealing times of the thinner films were 55, 5 min (set 3) and 50, 10 min (set 4), respectively, while those of the thicker films were 50, 10 min (set 3) and 45, 15 min (set 4). Thus by varying the time of the second (N$_2$+10%O$_2$) annealing step the depth to which the SiO$_x$ films were intentionally oxidized was varied. Aluminium metallization was carried out through a mask and MOS capacitors with area of $\sim 2 \times 10^{-3}$ cm$^2$ were formed. The structures were characterized electrically by current-voltage (I-V) and capacitance–voltage (C-V) measurements using Agilent B1500A Semiconductor Device Analyzer controlling Agilent E4980A Precision LCR Meter. The polarity of the applied voltage used below concerns the top Al electrode.

3. Results and discussion

Figures 1 (a) and (b) show cross-sectional micrographs (XTEM) obtained by lattice-resolution transmission electron microscopy (TEM) of a control and annealed (1000 °C in N$_2$ for 60 min) SiO$_x$ films with $x = 1.3$ and thicknesses of $\sim 15$ nm. The control layer (figure 1 (a)) exhibits an amorphous structure and a nearly atomically flat c-Si wafer/dielectric interface, while the annealed one (figure 1 (b)) exhibits nanocrystals with a diameter of a $\sim 4-5$ nm positioned almost in a single plane and a rougher interface, 3-4 monolayers [10,11].

Figures 2 (a) and (b) show I-V characteristics of sets 2, 3 and 4 of samples with 50 nm and 100 nm thick SiO$_x$ film, respectively. For both thicknesses the current flow through the dielectric starts at lower voltages for N$_2$ annealed samples (sets 2). For the samples subjected to a 90%N$_2$+10%O$_2$ annealing step (sets 3 and 4) the curves are shifted to higher voltages, respectively higher electric fields, which indicates formation of SiO$_2$ in the region close to the top surface. The I-V shift is better pronounced for the samples with longer oxidation times (see the inset in figure 2 (a), which shows similar I-V characteristics in a linear scale). The difference between the currents through the samples
from sets 3 and 4 at a given positive or negative voltage is more than one order of magnitude for both thicknesses, which can be explained assuming larger depth to which the NCs are oxidized at larger oxidation times.

Figure 1. XTEM micrographs of a control SiO$_x$ film showing an amorphous structure and abrupt interface (a) and an annealed film with nanocrystals in a dielectric matrix and rougher interface, ~0.8 nm or 3-4 monolayers (b).

The difference between the I-V curves of sets 2 and 3 is not so well pronounced, which is consistent with our previous observation [10] that the Si nanocrystals grown close to the top surface get transformed in SiO$_2$ to a thickness of ~5-6 nm, due to native oxidation after exposure to air. Curves 3 and 2 in figure 2 (b) intersect each other at a positive voltage of ~20 V (current of ~4×10$^{-9}$ A) because of the smaller curve slope of the N$_2$ annealed sample.

Figure 2. I-V characteristics of MOS structures with: (a) a 50 nm SiO$_x$ film annealed in N$_2$ (curves 3), N$_2$+5 min O$_2$ (curves 2) and N$_2$+10 min O$_2$ (curves 1) and (b) a 100 nm film annealed in N$_2$ (curves 3), N$_2$+10 minO$_2$ (curves 2) and N$_2$+15 min O$_2$ (curves 1). The inset in figure 1 (a) shows the onset of current injection in a linear scale.

For the samples from sets 3 and 4 (both thicknesses) the current measured at a given positive voltage is much larger than the corresponding current measured at the same negative voltage. For example for set 3 sample with 100 nm thick SiO$_x$ the current at ±25 V is $I_{(25V)} = 7.1 \times 10^{-8}$ A and $I_{(-25V)} =$
-3.5×10⁻⁹ A, while for sample from set 4 the values are \( I_{(25V)} = 2.8 \times 10⁻⁹ \) A and \( I_{(-25V)} = -8.9 \times 10⁻¹¹ \) A. It can be assumed that the main component of the current flowing through the gate dielectric at negative gate voltage is due to electrons, because they have to overcome a much lower barrier at the Al/SiO₂ interface (~ 3 eV) than the holes at the c-Si wafer/dielectric interface (~ 5 eV). Then, the observed large difference between the currents can be explained keeping in mind the increased roughness of the annealed c-Si/SiOₓ interface and assuming that the injection of electrons at positive voltage in the top SiO₂ (formed after 90%N₂+10%O₂ annealing) is from nanocrystals. The increased roughness and NC injection lead to a local enhancement of the electric field [4,12] and thus to a larger current at a given positive applied voltage.

In figure 3 I-V characteristics, measured in positive direction, of control MOS structures and structures annealed in N₂ for 60 min (set 2) are shown for both thicknesses. For the 50 nm structures the current through the control sample starts at a lower voltage compared to the N₂ annealed one, while for the 100 nm samples the conduction starts at approximately the same voltage. For both thicknesses the control samples have shown worse insulating properties compared to the annealed ones, lower voltage and lower current density breakdowns.

**Figure 3.** I-V characteristics of control MOS structures (Ar) and structures annealed in N₂ for 60 min.

In figure 4 the I-V characteristics of samples with the same duration of the 90%N₂+10%O₂ annealing step and having different thicknesses of the SiOₓ layer are shown. As it is seen in spite of the large difference between both dielectric thicknesses, 100 nm and 50 nm, the structures start to conduct approximately at one and the same voltage for both polarities. This observation implies formation of a stoichiometric SiO₂ region, close to the top surface, which limits the current through the gate dielectric in a similar way.

Thus the I-V and XTEM results obtained confirm that the suggested two step N₂, 90%N₂+10%O₂ high temperature annealing leads to formation of three-layer SiO₂/SiO₂-SiNCs/SiO₂ gate dielectric containing Si nanocrystals.

Figures 5 (a) and (b) show high frequency C-V curves of a control and annealed (50 min N₂, 10 min 90%N₂+10%O₂) samples having 50 nm thick SiOₓ layer. Curves 1 and 2 in figure 5 (a) were measured when sweeping the gate voltage from 0 to -4 V and then in the reverse direction. A hysteresis of ~ 0.6 V is seen, which is due to charging and discharging of traps in the SiOₓ layer. After measuring the initial curve, pulses with amplitudes of +10 V, +15 V, -10 V, -15 V, -20 V and duration of 1 s were applied and after each pulse the position of the C-V curve was monitored. The application of the first pulse (+10 V) makes the slope of the C-V curve steeper and shifts it slightly in the positive
direction. The observed change in the curve shape implies charging of c-Si/SiOₓ interface states and some of the SiOₓ bulk traps. The application of the next pulses leads to similar changes; the only difference is the direction in which the C-V curve shifts (positive pulses shift it to higher positive voltages, while negative pulses shift it in the opposite direction). However, even after the highest pulse applied (-20 V) the C-V curve remains to the right of its initial position (curves 1, 2). Another important feature of the control MOS structure is that it loses the bulk trapped charge quite fast (after several minutes).

Figure 5. High frequency (1 MHz) C-V curves of: (a) a control and (b) annealed (50 min N₂, 10 min 90% N₂ + 10% O₂) samples with 50 nm thickness of the SiOₓ layer.

Figure 5 (b) shows the initial C-V dependence (curve 1) and the curves obtained after charging the structure with +10 V, 1 s (curve 2) or -10 V, 1 s (curve 3) pulses. Parallel shifts, corresponding to charging of the nanocrystals with electrons/holes are seen after the application of positive/negative pulse. Before applying each of these pulses the structure was brought to its initial state by applying appropriate bias. The larger shift caused by positive pulse is in agreement with the I-V results shown in figure 2. After increasing the charging pulse amplitudes to ±12 and ±15 V curves 4, 5 and 6, 7 were measured. Besides the parallel shifts on both sides of the initial curve the oxygen annealed MOS structure shows a larger retention time in comparison with the control one; one hour after charging the structure (positively or negatively) the C-V curve remains in the same position.
4. Conclusions

The I-V and XTEM results obtained confirm that the suggested two step N₂, 90%N₂+10%O₂ annealing of SiOₓ films (x = 1.3) at 1000 °C for 60 min leads to a formation of three-layer SiO₂/SiO₂-SiNCs/SiO₂ gate dielectric, which contains Si nanocrystals. The nanocrystals are with a diameter of a ~ 4-5 nm and are embedded in a stoichiometric SiO₂ matrix. The I-V measurement show that the current through the gate dielectric is limited by the SiO₂ region, close to the top surface, formed during the second (90%N₂+10%O₂) annealing step. The MOS structures subjected to a two step annealing can be charged with electrons/holes by applying positive/negative voltage pulses at the control gate and show larger retention times in comparison with the control structures or structures annealed only in N₂.

Acknowledgements

The authors gratefully acknowledge the financial support of the Bulgarian Ministry of Education, Youth and Science under grant NT-4-1, Autonomous University of Baja California and Consejo Nacional de Ciencia y Tecnologia CONACyT, Mexico. The measurements were carried out in part in the Frederick Seitz Materials Research Laboratory Central Facilities, University of Illinois, which are partially supported by the U.S. Department of Energy under grants DE-FG02-07ER46453 and DE-FG02-07ER46471.

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