Non-binary LDPC Decoder Design over Rayleigh Channel for FPGA Implementation

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Abstract
Low Density Parity Check Code (LDPC) is a kind of linear block codes based on sparse check matrix. As a kind of channel coding, whose error performance approach Shannon limits, it has better error correction capability, more flexible structure and lower decoding complexity. Currently most of the LDPC code researches are on the premise of the AWGN channel and BSC channel, which mainly in the range of the binary LDPC codes. According to the above problem, this paper analyzes the various decoding performance of non-binary LDPC codes in Rayleigh channel, and realizes a non-binary LDPC decoder in Rayleigh channel through the FPGA design. The paper begins with an overall discussion of issues surrounding the use of non-binary LDPC codes. And then the bit-error-rate (BER) performances of different non-binary LDPC codes decoding algorithm are compared on the independent Rayleigh fading channel. Finally, this decoder design is implemented based on 5CSEMA5F31C6 FPGA (devised by Altera Company) to illustrate the concepts discussed in the paper.

Keywords: non-binary LDPC codes, Rayleigh fading channel, decoding algorithm, FPGA

1. Introduction
Low-density parity-check (LDPC) codes are first introduced in 1960s [1] and rediscovered by MacKay [2]. Based on message passing algorithm, the bit-error-rate (BER) performance of LDPC codes can be close to the Shannon limit.

Non-binary LDPC codes [3, 4], discovered by Davey and Mackay in 1998 [5], are an extension of binary LDPC over Galois field GF (q) of order q>2. Compared to binary LDPC codes, non-binary LDPC codes have better BER performance, particularly in higher-order modulation. Furthermore, it shows that non-binary LDPC codes can combat burst error and possibly replace the RS codes [6, 7]. Besides, non-binary LDPC codes are confirmed that they outperform both quasi-cyclic LDPC codes and convolution Turbo codes [8]. The construction of the non-binary LDPC codes are more complicated than that of the binary LDPC codes [9]. In [10], Wymeersch introduces a log-domain decoding scheme for non-binary LDPC codes, which is mathematically equivalent to the conventional sum-product decoder for binary LDPC codes. But when q is high enough, the decoding complexity for non-binary LDPC codes becomes very large, and it becomes almost impossible to practice. In [11], Barnaul present a modification of Belief Propagation algorithm that enable us to decode non-binary LDPC codes with a complexity that scales as qlog2(q), q being the field order. However, most of these researches are done on the additive white Gaussian noise (AWGN) channel. In this paper, we mainly discuss the performance of non-binary LDPC codes on Rayleigh fading channel, and design a decoder for non-binary LDPC on Rayleigh channel using FPGA.

This paper is organized as follows. Section II reviews the model of Rayleigh fading channel and the algorithm (weighted variable serial Min-max decoding algorithm, WVSMM) used in this paper. Section III represents the simulation results and comparison with other algorithms performances. The proposed decoder architecture is described in Section IV. We also provide FPGA implementation synthesis and simulation results in Section V. Finally, a conclusion is given in Section VI.
2. Communication Channels and Algorithms Used

2.1. The Overview of Rayleigh Fading Channel

Rayleigh fading channel [12] is a statistical model for propagation environment on the radio signal used by wireless networks [13]. It assumes that the power of a signal passes through a transmission medium will vary randomly which is modeled as Rayleigh distribution. It is a reasonable model for troposphere and ionosphere signal propagation as well as the effect of heavily built up urban environment on radio signals. Raleigh fading channel is most applicable when there is no line of sight between the transmitter and receiver. Under the Rayleigh fading channel, the sampling value of output signal at the time \( k T_s \) is given by:

\[
y_k = a_k x_k + n_k
\]  
(1)

2.2. The Simulation Method of Rayleigh Flat Slow Fading Channel used

Smith proposed a simple method based on the Clarke computer simulation model to simulate Rayleigh flat slow fading channel. The steps of simulation are shown in Figure 1. The specific process is explained below:

**Step1:** Design the number \( N \) (represents \( f_S E_x \)) of the frequency domain points, and the maximum of the Doppler frequency shift \( f_s \). "N" generally values a power of 2.

**Step2:** According to the formula:

\[
\Delta f = 2 f_s \left( \frac{N - 1}{N} \right)
\]  
(2)

Calculate the frequency spacing of two consecutive spectrum lines. Then we can get the period time of fading waveform \( f_T = 1 / \Delta f \).

**Step3:** Generate the complex Gaussian random variable for the positive frequency components at each "N / 2" of noise source.

**Step4:** The positive frequency value takes conjugate to the corresponding negative frequency to obtain a negative frequency component of the noise source.

**Step5:** Multiply the noise source of in-phase and quadrature by decline spectrum \( S_{E_x} \).

**Step6:** On the in-phase and quadrature channels, calculate the signals of frequency domain by Inverse Fast Fourier Transform (IFFT), and obtain two time series with length N.

**Step7:** Take the sum into the square root, which is obtained from step 6, and obtain simulation Rayleigh fading signals N-point time series.

![Figure 1. The Clarke computer simulation model of Rayleigh flat slow fading channel](image)

2.3. Weighted Variable Serial Min-Max Decoding Algorithm (WVSMM Decoding Algorithm)

The steps of the WVSMM decoding algorithm are as follows:

1. Deal with the variable node processing procedure of the variable serial min-max decoding algorithm as follows, so that formula (3) becomes the following Equation (4).

\[
\bar{L}(q_{mn}) = \bar{L}(q_{mn}) - \bar{L}q_{mn}
\]  
(3)
In the formula (4), the first $\tilde{L}(q_{mn}^{\rightarrow})$ is variable node information after updating, the second $\tilde{L}(q_{mn}^{\rightarrow})$ is variable node information before updating.

2. When we consider the convergence property, variable information that before the update or after it should keep consistent, so there will be the formula (5).

$$\lambda_1 = 1 - \lambda_2 = \lambda$$

3. The $\lambda$ in the formula (5) may be referred to the weight factor. Formula (4) changes to the formula (6).

$$\tilde{L}(q_{mn}) = \lambda (\tilde{L}(q_{mn}^{\rightarrow}) - \tilde{L}(q_{mn}^{\rightarrow})) + (1 - \lambda)\tilde{L}(q_{mn})$$

Because of adding the weight factor into variable node processing of non-binary LDPC serial min-max decoding algorithm, so the algorithm is called non-binary LDPC weighted variable serial min-max decoding algorithm (WVSMM decoding algorithm).

3. Simulation Results and Discussion

In this section, we compare the performance of the proposed non-binary decoding algorithm, described in Section II, with the other proposed non-binary decoding algorithm. We use the non-binary code over GF (4) and all codes have a rate of 1/2. The code length is 200 GF(4) symbols and iteration times is 20. To ensure fair comparisons, we use non-binary codes of the same length.

Figure 2 shows the BER performance and compares to the different algorithms. The simulation environments of proposed decoder are BPSK modulation, Rayleigh fading channel, 10bits input quantization. The maximum iteration in the FFT decoder is 20.

Analysis from whole SNR region shows in Figure 2, Min-sum decoding algorithm shows the worst performance, and its entire curve is in the upper side. Then there is the Min-max algorithm, serial Min-max decoding algorithm and so on. Traditional BP decoding algorithm,
whose curve shows at the lowest side, has the best performance. This figure can also be observed that, the performance curve of WVSMM (weighted variable serial Min-Max decoding algorithm) is closest to the traditional BP decoding algorithm, even in some cases, the WVSMM has better performance.

Figure 3 shows the average iteration numbers of decoding cycle when codes decoded with different algorithms. The simulation environments of proposed decoder are BPSK modulation, Rayleigh fading channel, 10 bits input quantization. The maximum iteration in the FFT decoder is 20. Observe the whole SNR region, for one successful decoding cycle, the average iteration numbers of the Min-sum decoding algorithm is largest, followed by the Min-max decoding algorithm. The average iterations required for successful decoding of the traditional BP decoding algorithm is less than the Min-max decoding algorithm. Figure 3 also shows that the average iteration numbers of the WVSMM is smallest, whose curve shows at the lowest side. Overall, the performance of WVSMM decoding algorithm is significantly better than the algorithm mentioned above in this figure.

4. Proposed Decoder Architecture

The hardware decoder [14] operating under the presented mixed domain decoding algorithm has been designed in the form of synthesizable description in VHDL. The decoder has been implemented and verified for a number of GF (q) codes in Virtex-6 FPGA [15] devices. In this section we present the decoder overall structure, synthesis results and some decoding simulation results. We begin with computation unit’s description and then present the decoder structure.

4.1. Variable Node Unit

From the calculation perspective, the update process of a variable node is achieving the formula (7), (8), (9).

\[
\tilde{L}(qq_{mn}) = \gamma_n + \sum_{m \in M(n): mn} \tilde{L}(R_{mn}) \tag{7}
\]

\[
Lq_{mn} = \min(\tilde{L}(qq_{mn})) \tag{8}
\]

\[
L(R^{a}_{mn}) = \max_{n \in N(M:n)}(L(q^{a}_{mn})) \tag{9}
\]
The variable node receives information from two different sources—the intrinsic information vector, and the extrinsic pdf messages from the check nodes which are connected to it through the permutation network. The functionality of the node is implemented as shown in Figure 4.

![Figure 4. Variable node calculation unit](image)

Variable node update process is to collect the initial information, and other information of check nodes. In order to reduce the overall amplitude of variable information without affecting the relative information relationship between each symbol for a variable node, formula (8) obtains the minimum value of each variable node's each symbol information, formula (9) subtracts the minimum value, which obtained by the formula (8), from the latest updates of variable information, then sums weighted with the information stored previously. From the operation process, the calculation unit can complete the variable node update.

4.2. Check Node Unit

From the calculation perspective, the update process of a variable node is achieving the formula (9).

\[
L(R_{\min}^n) = \min_{n \in N(M)} \max_{(L(q_{\min}^n))}
\]

(10)

From the formula, the calculation process is seeking the maximum of logarithmic likelihood information, for code sequence, which satisfies the validation. Then obtain the minimum of the maximum value. This is the essence of the Min-max decoding algorithm. The functionality of the node is implemented as shown in Figure 5.

![Figure 5. Check node calculation unit](image)

4.3. Decoder Architecture

The decoder architecture consists of many blocks as shown in Figure 6. It contains clock module, receiving buffer area, series-parallel conversion, the initial information storage and so on. The details of each block will be discussed in the followings.
Receiving buffer area module is used for message rate conversion. Since the information receiving rate is different from the information processing rate of the decoder (generally, the information processing rate of the decoder is greater than the information receiving rate), this module is required to complete the rate conversion. Series-parallel conversion modules are used to achieve sub-block storage of initial information, and achieve partial parallel decoding.

The initial information storage module is used to store the initial information that is quantized. Then, the check node and variable node message update. Check nodes messages come from the variable nodes messages (at first time, it comes from the initial information), variable nodes messages come from the initial messages and check nodes update messages.

Decoding buffer area module is used to store the code that is decoded. Code verification module is used to judge whether the code (after decoding) is in accord with check equation, and to determine whether to continue the iteration. Parallel-series conversion serially output the decoded codes. Throughout the process, the coordination of various modules is controlled by the clock module.

5. Implementation Results

The simulation result of the decoder proposed in this article is shown in Figure 7. The decoding information is compared with encoding information (without adding noise previously), results are same. It indicates that this decoder is a reasonable design.

In this paper, the decoder design is based on 5CSEMA5F31C6 FPGA devised by Altera Company, with QuartusII14.1, and Modelsim simulation tools. After compiling synthesis, at the frequency of 50MHz clock, the resource consumption shows as follow: ALMs-68%, RAM-56%. The logic resources of this decoder can meet the requirements. It can reach a compromise with resources, rate, and decoding accuracy.
6. Conclusion

We have synthesized a non-binary LDPC decoder. This paper provided a brief overview of non-binary LDPC decoding and Rayleigh fading channel, proposed the VSMM decoding algorithm, and then, we presented the GF (q) LDPC decoder design approach targeted for the FPGA devices. Effectiveness of the presented realization is based on balanced utilization of all types of FPGA resources, particularly making use of the multiplier cores. In order to achieve this, the modified decoding algorithm formulation has been proposed at first. Then we presented the decoder structure, also pointing out some important aspects of FPGA implementation. The synthesis results for serial architecture show that the designed decoder can be implemented in a small part (several percent) of the modern FPGA device resources with moderate throughput. Extension to the architecture achieves higher throughput at the cost of higher FPGA utilization.

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