Effect of gate bias sweep rate on the threshold voltage of in-plane gate nanowire transistor

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Abstract. In\(_2\)O\(_3\) nanowire electric-double-layer (EDL) transistors with in-plane gate gated by SiO\(_2\) solid-electrolyte are fabricated on transparent glass substrates. The gate voltage sweep rates can effectively modulate the threshold voltage (V\(_{th}\)) of nanowire device. Both depletion mode and enhancement mode are realized, and the V\(_{th}\) shift of the nanowire transistors is estimated to be 0.73V (without light). This phenomenon is due to increased adsorption of oxygen on the nanowire surface by the slower gate voltage sweep rates. Adsorbed oxygens capture electrons and cause a surface of nanowire channel was depleted. The operation voltage of transistor was 1.0 V, because the EDL gate dielectric can lead to high gate dielectric capacitance. These transparent in-plane gate nanowire transistors are promising for “see-through” nanoscale sensors.

1. Introduction

Nanowires have attracted intense research interest due to their potential applications in nanoscale optoelectronic devices, logic circuits, and sensors [1–3]. In\(_2\)O\(_3\) nanowire is of particular interest for potential. In particular, the electrical properties of nanowires have a strong influence by adsorption and desorption of ambient active elements onto and from the nanowire surface, due to the large surface area to volume ratio of nanowires [4]. Adsorbed oxygen is easily bound at the oxygen vacancy site of the In\(_2\)O\(_3\) surface. The conductivity of the In\(_2\)O\(_3\) nanowire channel is depleted because the oxygen adsorbed on the surface reacts with free electrons as oxygen ions in the forms of O\(^-\), O\(_2\)\(^-\), or O\(_2^2^-\) [5]. Dayeh et al. reported that the transfer characteristics of InAs top-gated nanowire FETs were affected by gate bias sweep rate due to its influence on donor-type trap levels of the surface [6].

Simple device structure can reduce the preparation cost of the device, in-plane-gate transistor device with source/drain and gate electrodes on the same plane. However, conventional in-plane-gate transistors were fabricated by focused ion beam/electron beam lithography, which are generally complicated and expensive [7, 8]. Up to now, low-cost nanowire transistors with in-plane gate structure have little been reported. In other words, fabrication of these in-plane gate nanowire transistors is still rather challenging.

In this letter, we fabricated in-plane gate In\(_2\)O\(_3\) nanowire transistors gated by SiO\(_2\) solid electrolyte, by using a single nickel TEM grid shadow mask at room temperature. The operation voltage of the nanowire transistors is reduced to 1.5 V due to the extremely large EDL capacitance of SiO\(_2\) solid electrolytes. The threshold voltage (V\(_{th}\)) can be effectively modulated by gate bias sweep rates. Both enhancement mode and depletion mode are realized, and the V\(_{th}\) shift of the nanowire transistors is estimated to be 0.73V (without light).
2. Experimental detail

In$_2$O$_3$ nanowires were synthesized by the vapor liquid solid (VLS) growth mechanism [9]. Figure 1(a) shows the low resolution scanning electron microscopy (SEM) image of the In$_2$O$_3$ nanowires. Notably the surfaces of In$_2$O$_3$ nanowires were clean and smooth. The length of the nanowires was in the range 1–20 mm, and the diameter was about 100 nm, as shown in the inset of figure 1 (a).

The entire process of in-plane-gate nanowire EDL transistors fabrication was performed on a Micromanipulator 1555 probe station at room temperature, the structure of the device is shown in figure 1(b). The fabrication process can be divided into four stages: (1) A 2.0-µm-thick SiO$_2$ solid-electrolyte film was deposited onto the clean ITO glass substrate by the plasma-enhanced chemical vapor deposition (PECVD) method, using SiH$_4$ and O$_2$ as reactive gases at room temperature. (2) A mechanical probe was used to transfer nanowires onto the SiO$_2$ solid-electrolyte film under an optical microscope [10]. (3) The TEM nickel grid mask was placed and fixed on the single In$_2$O$_3$ nanowire under the observation of an optical microscope. (4) After ITO (200 nm) electrodes have been deposited by radio frequency magnetron sputtering, the TEM nickel grid mask was moved from its position slightly. At last, a series of in-plane-gate In$_2$O$_3$ nanowire EDL transistors gated by SiO$_2$ solid-electrolyte solid electrolyte were fabricated. Scanning electron microscope (SEM) image of the nanowire EDL transistor was performed with a Hitachi S-4800 microscope. The electrical characteristics of the in-plane gate In$_2$O$_3$ nanowire EDL transistors were measured with a Keithley 4200 semiconductor parameter analyzer at room temperature in the dark. The capacitance-frequency measurement was performed using a WK 6500B precision impedance analyzer.

Figure 1. (a) SEM image of the In$_2$O$_3$ nanowires. (Inset) High-resolution SEM image of an individual In$_2$O$_3$ nanowire. (b) Schematic of the in-plane-gate nanowire transistor.

3. Results and discussion

Figure 2(a) shows the frequency-dependent capacitance of the SiO$_2$ solid electrolyte gate dielectric. A very high specific capacitance of 1.22 µF/cm$^2$ at 20 Hz due to EDL effect [11]. The figure 2(b) shows the optical transmission spectrum of the entire FETs arrays on the glass substrate in the wavelength range between 200 and 1000 nm. The average transmittance in the visible range (400–800 nm) is about 75%, indicating that the FETs are transparent to visible light.

The electronic properties of in-plane gate nanowire transistors were measured as a function of gate bias sweep rate in different measurement environments. It can be seen from the figure 3 (a) and (b), the threshold voltage and $I_{on}$ of device is different with light and without light. At the same time, a series of $I_d$-$V_{gs}$ curves measured at different gate bias sweep rates (25, 50, 100 and 500 mV/s) at a fixed drain voltage ($V_{ds}$) of 0.8 V under various environments. Since the gate bias sweep rate is the amount of change per unit time and the step of the voltage is independent of the time, the change in the gate bias sweep rate does not affect the step voltage. It is interesting to note that the transfer characteristics consistently shift in the negative direction as the gate bias sweep rates is changed from 25mV/s to 500mV/s. The operation mechanism of the threshold voltage change can be explained by the depletion of electrons by oxygen adsorption on the surface of In$_2$O$_3$ nanowire. Previous reports that the stable oxygen ions are O$_2^-$below 100 °C, O$^-$ between 100 and 300 °C, and O$_2^{2-}$ above 300 °C [12, 13]. The oxygen influence of the In$_2$O$_3$ nanowire transistors would be mainly attributed to adsorption...
of $O_2^-$ ions due to electrical properties of the nanowire transistor is tested at room temperature. Slower gate bias sweep rates imply longer gate biasing time. The oxygen ions would not be easily detached due to captured oxygen ions were strongly bonded by positive gate bias. Thus, slow gate bias sweep rates will cause more oxygen absorption than fast gate bias sweep rates. As a result, the current decreases and the threshold voltage shifts to the positive gate bias direction occur by slower gate bias sweep rates, due to longer gate biasing time. On the contrary, faster gate voltage sweep rates are applied in relatively shorter gate biasing time. Therefore, fast gate voltage sweep rates lead to less oxygen absorption. Thus, the current increases and the threshold voltage shifts to the negative gate voltage direction, as shown in figure 3. The figure 3(a) and (b) are the results of test with light and without light, the results show that the conductivity of the channel under light conditions is few stronger, there may be more carriers produced under with light than without light conditions.

Figure 2. (a) Frequency-dependent specific capacitance of the SiO$_2$ solid-electrolyte. (b) Optical transmittance spectrum of the nanowire transistor. Inset: digital photograph of transistors fabricated on glass. The logo can be clearly seen through the devices.

Figure 3. (a) and (b) transfer characteristics of the same device at $V_{ds}=0.8$V with light and without light.

Figure 4(a) shows the output characteristics ($I_{ds}$–$V_{ds}$ curves) at $V_{gs}$ varied from 0V to 1V in 0.2V steps (without light). A maximum on-current of 3.11 μA was measured at $V_{ds}=0.8$ V and $V_{gs}=1V$. It indicates good current saturation behaviors at high $V_{ds}$ and excellent linear characteristics of $I_{ds}$ at low $V_{ds}$, this shows that a low resistance of the ohmic contact formed between the In$_2$O$_3$ nanowire and ITO source/drain electrodes.

We also measured the leakage current of the device, the leakage current is less than 5nA as shown in figure 4(b). The results strongly indicate that the SiO$_2$ solid-electrolyte is an electronically insulating but solid electrolyte. The EDL formed at the interface induces a rather large electric field on the order of megavolts per centimeter at the EDL region, resulting in a high density of charge carriers at the surface of the In$_2$O$_3$ channel. Such an electrostatic modulation process controls the conductance of the In$_2$O$_3$ channel layer, which is meaningful for low-voltage electrostatic modulation devices.
The field-effect mobilities of the nanowire EDL transistors are estimated by \( I_{ds} = (\mu C) (V_{gs} - V_{th})^2/(2L^2) \), where \( L = 15 \mu m \) is the channel length. The electrolyte gate capacitance per unit length can be estimated as \( C_g = C/L = \frac{2\pi \varepsilon_0 \varepsilon_r}{\ln(1 + 2L_D/d)} \), where \( \varepsilon_r = 2 \) is the dielectric constant of the SiO\(_2\) solid-electrolyte medium, \( \varepsilon_0 \) is the permittivity of free space, and \( d = 100 \) nm is the diameter of In\(_2\)O\(_3\) nanowire. Debye length \( L_D \) is simply defined as the typical distance required for screening the surplus charge by the mobile carriers present in a material [14]. According to the definition of the Debye length, we assume that the thickness of the EDL (1.0 nm) is the Debye length. Thus, \( L_D \) is assumed to be 1.0nm [15, 16]. Based on this model, the saturation electron mobility of In\(_2\)O\(_3\) nanowire transistors as gate bias sweep rate changes from 25 to 500mV/s are estimated to be from 141 to 95 cm\(^2\)/Vs with light, and from 175 to 66 cm\(^2\)/Vs without light, respectively.

![Figure 4](image)

**Figure 4.** (a) Output characteristics of nanowire transistors. (b) The leakage current of the device.

**Table 1.** Summary of the electrical properties of in-plane gate In\(_2\)O\(_3\) nanowire transistor with various voltage sweep rates with light and without light.

| With Light | voltage sweep rate (mV/s) | \( V_{th} \) (V) | \( S \) (mV/dec) | \( I_{ds} \) (\( \mu \) A) | \( \mu \) (cm\(^2\)/Vs) |
|------------|---------------------------|------------------|------------------|--------------------------|---------------------|
| 25         | 0.00                      | 136              | 2.62             | 141.4                    |
| 50         | -0.23                     | 133              | 3.78             | 135.0                    |
| 100        | -0.42                     | 132              | 4.80             | 128.5                    |
| 500        | -0.74                     | 130              | 5.34             | 95.2                     |

| Without Light | gate voltage sweep rate (mV/s) | \( V_{th} \) (V) | \( S \) (mV/dec) | \( I_{ds} \) (\( \mu \) A) | \( \mu \) (cm\(^2\)/Vs) |
|---------------|---------------------------------|------------------|------------------|--------------------------|---------------------|
| 25            | 0.24                            | 135              | 1.88             | 175.8                    |
| 50            | 0.05                            | 134              | 2.48             | 148.4                    |
| 100           | -0.23                           | 136              | 2.62             | 93.5                     |
| 500           | -0.49                           | 131              | 2.74             | 66.6                     |

Table 1 summarizes the electrical performance of in-plane gate nanowire transistors with various gate bias sweep rate (25-500mV/s) with light or without light. The \( V_{th} \) of in-plane gate nanowire transistor with different gate bias sweep rate was calculated from x-axis intercept of the square root of \( I_{ds}-V_{gs} \) plot (Linear Extrapolation (LE) method [17]). Under light conditions, the \( V_{th} \) of the in-plane gate transistor shifts from 0 V to -0.74V when the gate voltage sweep rate changes from 25 to 500mV/s, and the shifts from 0.24 V to -0.49V without light, due to slow gate voltage sweep rates will cause more oxygen absorption than fast gate bias sweep rates, so the threshold voltage shifts to the positive gate bias direction occur by slower gate voltage sweep rates and longer gate biasing time. In the light conditions, the threshold voltage moves in the negative direction due to sensitivity of nanowires. The subthreshold slope \( S = dV_{gs}/d \log I_{ds} \), the smaller \( S \), the easier it is to switch the transistor to an off-state. For this device, the \( S \) is almost identical (134mV/dec), due to \( S \) value is mainly related to the device structure and temperature, which was little affected by the ordinary light and gate voltage sweep rate. The mobility is decreased because the \( V_{th} \) and \( I_{ds} \) changes with various
gate bias sweep rate. Since the mobility of the device is affected by the scattering of carriers, the carrier mobility is high when the density is lower. The change in threshold voltage in the case of light and without light is mainly due to sensitivity of nanowires.

4. Conclusions
We fabricated in-plane gate nanowire transistors using TEM grid mask, and studied the threshold voltage of In$_2$O$_3$ nanowire transistors as a function of gate bias sweep rate. The $V_{th}$ of the transistors could be effectively tuned from 0.24 to -0.49V by ranging the gate voltage sweep rate from 25 to 500mV/s. These in-plane gate nanowire transistors had controllable $V_{th}$, simple fabrication, and low-voltage operation, making them very promising for next-generation low-cost portable “see-through” sensors and other nanoelectronics.

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