Abstract. Electromagnetic interference, caused by the electric power line, affects the signals of electronic instruments, specifically those with low levels of amplitude. This type of signal is known as Common Mode Interference. There are many methods and architectures used to minimize or eliminate the influence of these interferences in electronic instrumentation, the most common is the use of band reject filters to eliminate them. With this objective, we present the analysis, prototyping, developing and testing of a new architecture reconfigurable filter with application in biomedical instrumentation, applied to the reduction of interference in common mode and conservation of components of the useful signal in the same range of noise, by the principle of balancing impedance dynamic using the hardware description software and simulation electronics software. The methodology was tested using a sinusoidal signal in the same standard frequency of an electrocardiogram signal in the same frequency interference (50/60 Hz). Excellent results were obtained in simulation with noise reduction of approximately 97%, while the results of experimental tests showed around 50% reduction. In both cases, the useful signal was preserved, confirming the efficiency of the proposed architecture. The method can be applied to eliminate the interference, which are in the same band the of the useful signal components.
1. Introduction
Electromagnetic Interference (EMI) is a phenomenon that affects at a greater or lesser extent the operation of electro-electronic devices [1]. In the context of noise reduction, that this work is applied. Thus was adapted a new architecture with discrete components, which reduced the interference in common mode ($V_{cm}$), mainly that generated by the electric power line (50/60 Hz), preserving its components in differential mode ($V_d$). As a measure of evaluation of this circuit, have been proposed to measure the results from Biosensors. The circuit design is based on the reconfigurability concept [2], in which a model described in VHDL-AMS [3] allowed to validate the basic principles of operation and then used the software Proteus Isis Schematic Capture [4] to design a test version, using discrete components, and simulate using parameters close to reality. The experimental results came validate and prove by those obtained in simulation.

2. Concept of impedance balancing
Impedance balancing is the ability of symmetry between two circuits. When this measure of symmetry does not exist, then this system is known as an unbalanced circuit, thus causing an "attenuation factor", this factor measures the degree of divergence in relation to electrical symmetry ideal.

The unbalance is one of the factors that lead to increased noise, which is a reality in electronic circuits, mainly when the equipment is under the direct action from EMI. Noises can be reduced using several techniques, some electronic and other mechanical: the most trivial one is to increase the Common Mode Rejection Radio (CMRR) of the circuit signal processing [5]; the other technique would involve the data cables by an external metal mesh. In this context, this article proposes a new architecture using the principle of electronic impedance balancing, dynamically adjusted, to noise reduction in common mode ($V_{cm}$).

Before describing the proposed architecture, a brief introduction about the state of the art on impedance static balancing is presented.

2.1. Measure of unbalance
There is not a specific method for measurement of unbalance. For example, in telecommunications, the loss of signal strength due to the unbalance in telephone wires or terminals, also known as loss unbalance longitudinal (LUL), are measured according to standards of quality control, such as the ANATEL’s 473 standard which, according to Volpato and Magalhes [6], using this parameter, the calculated value of unbalance in the telecommunications cables is around 19.7061 dB (LUL= - 19.7061 dB). This value tends to increase with the increasing distance between the transducer and the input circuits. To control this increase in noise due to the unbalance, it has been presented new proposals, as the architecture of AI indicated by Dobrev and Daskalov [7], which had a reduced $V_{cm}$ range of about 200 times when he used an electrocardiogram signal [8] as a demonstration (Figure 1). The upper graph represents the noise $V_{cm}$, (50 Hz sine wave) and the lower, the differential signal before and after balancing, figures 1a and 1b.

The prototype aimed at eliminating $V_{cm}$ by reducing the impedance unbalance. However, this new approach compared with other methods, has the advantage of the fact that only the common mode noise ($V_{cm}$) undergoes attenuation, while the useful signal components ($V_d$), even in the same frequency noise, is weakly influenced. The balance of the impedance is dynamically controlled by a microprocessor system, and beyond that, the proposed system can be easily programmed to operate in any other band interference, without physically changing the circuit.
3. Theoretical fundamentation

The grounds of the prototype has their roots in Silva [9], however, a new control method of noise reduction using the impedance unbalance based on a new architecture using discrete components, fully adapted and designed to reduce the effect $V_{cm}$ interference in electronic circuits has been presented, which generated even a prototype that proved the mathematical calculations and theoretical results obtained in simulation.

The unbalance of the impedances of the electrodes is compensated dynamically using a counter circuit that controls a bank impedances, which allowed the reduction of common mode noise ($V_{cm}$) in an AI input impedance dynamic balancing by means of a feedback system (RECONFIGURABLE CIRCUIT), Figure 2. The composition and functioning of the prototype are described below.

**Figure 1.** ECG Signal influenced by $V_{cm}$ noise, (a) without balancing and (b) with balancing [7].

**Figure 2.** New architecture adapted from Silva [9].

Being:

- $V_{mc}$ = electrical interference signal in common mode;
• $V_d/2$ = bio-potential signal at each electrode;
• $V_+ e V_-$ = voltages at the input of AI;
• $Z_1 e Z_2$ = impedance of the input electrodes;
• $Z_{C1} e Z_{C2}$ = Dynamically adjustable impedances;
• $Z_{in}$ = input impedances of the AI amplifier;
• Reconfigurable Circuit = circuit responsible for the dynamic control of adjustable impedances;
• $V_0$ = adjusted output signal with minimum interference.

The reduction of the unbalance is viable through a feedback loop (Reconfigurable Circuit) that, due to the variation of maximum amplitude of the output signal ($V_0$), readjust the permitted values of input impedances ($Z_{C1}$ and $Z_{C2}$) to obtain an output signal with minimal interference. This value is achieved when the condition of transfer function (FT), Equation 1 is satisfied, meaning that the common mode noise was canceled.

$$Z_{c1} + Z_1 = Z_{c2} + Z_2$$ (1)

The general equation of a non-feedback amplifier is governed only by their internal components and displayed in Equation 2. However, as the architecture uses the principle of reconfigurability [2] by feedback, the new FT is defined by Equation (3). Still, as the main goal of analysis is the noise component, then only the second part of the equation is taken into consideration (Equation 4), it is directly influenced by the balancing of the impedances of the cables ($Z_1$, $Z_2$, and $Z_{C1}$, $Z_{C2}$), noise ($V_{mc}$) and the gain in differential mode ($A_d$) in the AI inputs. The test, the level of unbalance that can reduce this new architecture, which was the same used in longitudinal telephone cables ($LUL$), where we got the Equations (4 and 5), based on the architecture in Figure 2. And after the appropriate replacements values in Equation 6, predicting the worst case of unbalance for ($Z_{C1} = 2.5 M\Omega, Z_{C2} = 10 k\Omega, Z_1 = Z_2 = 1.2 M\Omega$), the value found was ($LUL = -0.6674 \text{ dB}$).

$$V_0 = V_d A_d + V_{mc} A_{mc}$$ (2)

$$V_0 = \left( \frac{Z_{in}}{Z_{in} + Z_1 + Z_{c1}} - \frac{Z_{in}}{Z_{in} + Z_2 + Z_{c2}} \right) \frac{V_d}{2} A_d + \left( \frac{Z_{in}}{Z_{in} + Z_1 + Z_{c1}} - \frac{Z_{in}}{Z_{in} + Z_2 + Z_{c2}} \right) V_{mc} A_d + V_{mc} A_d$$ (3)

$$V_0 = \left( \frac{Z_{in}}{Z_{in} + Z_1 + Z_{c1}} - \frac{Z_{in}}{Z_{in} + Z_2 + Z_{c2}} \right) V_{mc} A_d$$ (4)

$$LUL = 20 \log\left( \frac{V_2 - V_{c1}}{V_{mc}} \right) (dB)$$ (5)

$$LUL = 20 \log\left( \frac{Z_{C2}}{Z_2 + Z_{C2}} - \frac{Z_{C1}}{Z_1 + Z_{C1}} \right) (dB)$$ (6)

Where: $A_{mc} = \text{is the gain of the amplifier in common mode.}$

4. Materials and Methods
Initially the project was described in the VHDL-AMS language and simulated in the ADVANCE platform from Mentor Graphics [3].
4.1. Project description in VHDL-AMS
In relation to the values of the sources of excitation, was only taken into consideration the common mode signal ($V_{cm}$). This means that when the analysis of simulation results (Figure 3), the useful signal ($V_{d1}$ and $V_{d2}$) will not be present, and only the interference will be displayed, presented an frequency oscillation ($f_{cm}$), and $of_{set} = 0$, meaning that there was no displacement of the reference point (DC level zero).

![Figure 3. Simulation in VHDL-AMS with feedback control.](image)

4.1.1. Simulation results obtained in VHDL-AMS
The results of two simulations in VHDL-AMS, given constant the input ($Z_{in1}$) and varying the other ($Z_{in2}$), are observed in the graphs in Figure 3, where three curves are displayed (listed from top to bottom): the first represents the amplitudes control (Control – Step2); the second, the increment or decrement the resistors bank ($Z_{C2}$) and the third interference signal, represented by ($V_{cm}$).

In the graphs of Figure 3, the interfering signal ($V_{cm}$), is attenuated and maintained at a level of amplitude as low as possible, through the closed loop control, which leads to the balancing of the impedances (Equation 1).

4.2. Design and simulation using proteus software
The design and simulations were also performed using the software Proteus "ISISProfessional v7.0" [4]. The project was divided as shown in Table 1, in which are detailed the elements used in the prototype, along with a brief technical description of each electronic component.

Where:
- COMP. = trade name of the component;
- Q = numeric quantity of each component;
- VALOR COM. = informs the market values;
- DESC. = brief technical description of the element;
- IMP VAR = impedance variable block;
**Table 1.** List and description of components.

| COMPONENT | QTE | COMMERCIAL VALUE | DESCRIPTION |
|-----------|-----|------------------|-------------|
| I.VAR Resistor(Ω) | 12 | 10K, 20K, 40K, 80K, 160K, 320K, 640K, 1280K, 2.55M, 2x100k, 320K, 640K, 1280K, 2.55M, 2x100k | Carbon resistor |
| Analog Switch | 8 | HEF4016 | Analog switch circuit |
| counter | | | |
| AI | 12 | CD4029 | Digital counter circuit |
| FIL LPF Filter | 1 | OP07 | 4th order active filter bandpass 60Hz |
| BPF Filter | 2 | OP07 | Circuit logic bandpass 60Hz |
| CON Circuit logic AND | 1 | 74LS00 | Circuit logic |
| Microcontroller PIC | 1 | 16F877(Microchip, 2010) | Control and A/D converter circuit |

- AI = amplifier instrumentation block;
- FIL = filters block;
- CON = control block.

4.2.1. Functional description

The operation of the circuit will be described according to the algorithm of Figure 4.

The operating system is based on the signal compensation, comprising a component in common mode (\(V_{cm}\)) and a differential mode (\(V_d\)), which are modulated by the input impedances (\(Z_{VAR IAB}\)), formed by a resistors bank. These resistors are connected (dynamically) so that will add a total of 2.55 MΩ, this is possible with the use of analog switches, which are controlled by four-bit counter (4 bits) each, but together can achieve to (8 bits = 256 values). As the signal amplitude is low, it needs to be amplified, which is done by the AI. A sample of the signal after filtered by the 2nd order LPF, the output is sent (\(V_0\)) to be analyzed later. Another sample of the signal goes to the control loop input impedance because what distinguishes this prototype of which have been submitted in earlier work (\([2], [5], [7]\)) is the analysis of noise (\(V_{cm}\)), which is separated from the useful signal (\(V_d\)) by a filter of 4th order BPF with bandwidth of 30 Hz, sufficient to pass only the components of the EMI between 40 and 70 Hz.

Then the signal passes through an A/D converter (implemented by the microcontroller (PIC 16F877)) 8-bit (which is equivalent to one resolution of 19.53 mV). If there is a sudden increase in input \(V_{cm}\), the same microprocessor used in the A/D conversion is programmed (in C language) to perform dynamic control block CONTROL of the impedances (\(Z_{VAR IAB}\)), by compensating the already discretized amplitudes of \(V_{cm}\) with two other digital reference voltages, which oscillate around the offset voltage (\(≈ 2.5\) V) of the microcontroller, as shown in Table 2. This type of control was more effective, using not only the clock, but also control of the count, increasing (UP) or decreasing (DW) of the counter circuits (counter), as tools (Table 1), influencing thus the increase or decreased of the variable impedance (\(Z_{VAR IAB}\)) more efficiently.

4.2.2. Circuit settings

The project description of each subcircuit was distributed in the following subtopics.

**Variable impedance block:** The variable impedance block (\(Z_{VAR IAB}\)), consists of a group of resistances (\(Z_c\)), which are described by Equation 7. The set comes complete with analog
Figure 4. Circuit algorithm.

Table 2. A/D 8 bits converter.

| Voltage(mV) | Decimal | Binary  |
|-------------|---------|---------|
| 0           | 0       | 00000000 |
| 19.53       | 1       | 00000001 |
| ...         | ...     | ...     |
| 2480.31     | 126     | 01111111 |
| 2499.84     | 127     | 10000000 |
| 2519.37     | 128     | 10000001 |
| ...         | ...     | ...     |
| 4980.15     | 254     | 11111101 |
| 4999.68     | 255     | 11111111 |

switches and counters, as detailed in Table 1.

\[
Z_{c2} = R \sum_{1}^{NB} 2^{(NB-1)}
\]  

Where:

- \( R \) = is the first resistance value;
- \( NB \) = the number of bits adopted in the \( A/D \).
**Instrumentation amplifier block (AI):** The amplifier block consists of a high pass filter (HPF) in the input, to minimize the noise below 0.3 Hz (equation 8), beyond AI, where the gain \( G_{AI}(V/V) \) is given by equation 9.

\[
H(S) = \frac{W.C.R}{\sqrt{1 + (W.C.R)^2}} \tag{8}
\]

\[
G_{AI} = 5 + \frac{200K}{R_G} \tag{9}
\]

Where:
- RG = is the gain resistance.

**Low pass/band bass filters block:** The filters were dimensioned based on the RAUCH architecture, in the witch the topology of multiple feedback (MFB) is characterized by high gains and quality factor (Q), and are determined by the general transfer function (Equation 10).

\[
\frac{Z_{out}}{Z_{in}} = -(\frac{Z_3}{Z_5} + \frac{Z_1}{Z_5} + \frac{Z_1.Z_3}{Z_2.Z_5} + \frac{Z_1.Z_3}{Z_4.Z_5})^{-1} \tag{10}
\]

From this standard block, after replaced by their appropriate values of resistances and capacitances equivalent, have been dimensioned other filters: LPF 2nd order, and its corresponding transfer function in Equation (11, 12, 13 and 14), and BPF filter, two blocks cascaded of 2nd order each regulated by a transfer function of Equation (15, 16, 17 and 18), equivalent to a 4th order. All calculated for 3 dB attenuation.

\[
|H(S)|_{LPF} = \frac{a_0}{b_1S^2 + a_1S + (W_0)^2} \tag{11}
\]

\[
a_0 = -\frac{R_2}{R_1} \tag{12}
\]

\[
a_1 = W_0.C_1(R_2 + R_3 + \frac{R_2\cdot R_3}{R_1}) \tag{13}
\]

\[
b_1 = W_0^2.C_1.C_2.R_2.R_3 \tag{14}
\]

\[
|H(S)|_{BPF-2?} = \frac{a_1S}{b_1S^2 + b_2S + (W_0)^2} \tag{15}
\]

\[
a_1 = -(\frac{R_2\cdot R_3}{R_1 + R_3}).C.W_0 \tag{16}
\]

\[
b_1 = (\frac{R_1\cdot R_2\cdot R_3}{R_1 + R_3}).C^2.W_0^2 \tag{17}
\]

\[
b_2 = (\frac{2\cdot R_1\cdot R_3}{R_1 + R_3}).C.W_0 \tag{18}
\]
Control block (CONTROL): The control block is formed by the PIC microcontroller (Table 1) and a DC level shifter circuit to keep a reference of 2.5 volts.

5. Results

Figures 6 to 7 present simulation results obtained from the circuit designed in the PROTEUS software, when applying characteristic signals obtained by biosensors, in order to reduce common mode noise ($V_{cm}$).

5.1. Simulation results

In Figure 5, three graphs are shown, representing the result of simulation of the noise reduction system (no feedback or control), with the application of a bioelectric signal characteristic in the input. The first (top to bottom) represents the signal in common mode and differential after amplified by the AI ($V_{AI-Out}$) constant gain, the second represents the output of the LPF biosignal ($V_{cm} + V_d$) and the third represents the noise in the output of the BPF ($V_{cm}$).

![Figure 5. Biosensor: system without feedback.](image)

In this case, the system has not been feedback and the amplitude of the interference range is approximately between a maximum value ($V_{cm,Max} \approx 1.19Vp$) and a minimum value ($V_{cm,Min} \approx 34.0mVp$), as previously mentioned, $V_d$ is until influenced by $V_{cm}$. This interference is such that the useful signal becomes disguised (hidden) by interference ($V_{cm} \gg V_d$). This relationship begins to change as the impedance matching occurs at the input of AI, due to feedback from the common mode signal, causing a progressive loss of range of $V_{cm}$, without affecting the amplitude of $V_d$. Thus, the useful signal tends become more visible ($V_{cm} \ll V_d$) (Figure 6).

After the feedback circuit, the system generated the graphs in Figure 6. The top graph represents the output of AI ($V_{AI-\text{Out}}$); the second output LPF filter, and the third output BPF filter.

5.2. Experimental circuit

After the theoretical analysis and simulation results, it was made a prototype circuit (Figure 7), where the LPF and BPF filter has been implemented in PSOC microcontroller (CY8C27443).
The prototype tests were performed using as the input sine wave with a frequency of 10 Hz, in the range of an ECG signal influenced by an EMI noise of 50 Hz results were obtained by means of an oscilloscope, and are shown in Figure 8. It can be seen from this figures that the noise reduction ($V_{cm}$) was around 50 times, while the differential mode component ($V_d$), or useful signal, was minimally affected.

6. Discussion

By the analysis of the results obtained, it is concluded that the proposed circuit (described in language VHDL-AMS, simulated on the platform from Mentor Graphics, designed and simulated in software PROTEUS) achieved its primary goal, which consists of reducing the common mode interference ($V_{cm}$) while preserving the useful components of the signals to which the system was proposed ($V_{d1}$ and $V_{d2}$), as shown in Figures 6 and 8b. The gain is kept at low levels in AI, to avoid saturation in the filtering blocks. In the output of the BPF block, the signal
purposely received a higher gain compared to other outlets, the need for analysis or for digital processing, more specific, if necessary. As the graph representative of the noise ($V_{cm}$), we find that the same was suffered attenuation by approximately 97% in biomedical signals application (Figure 6), while the useful signal is preserved($V_{AI−Out}$), as shown in the graphs of Figure 6.

The same results (with reduced around 50% were confirmed when the analysis of the experimental prototype (Figure 8a, 8b).

![Image](image_url)

**Figure 8.** Results obtained with the oscilloscope, (a) circuit without feedback and (b) with feedback.

7. Conclusion
This article addressed the issue of reducing common mode noise, especially those from sources of electromagnetic energy.

Before resolution of the problem, we proceeded to introduce the concept of balancing impedance. After the initial precepts, it was proposed modification architecture of $V_{cm}$ noise reduction by balancing dynamic input impedance ($Z_{VARIB}$).

For this, a circuit was designed in hardware description language ($VHDL_AMS$), simulated on the platform from Mentor Graphics, designed and simulated electronic software (PROTEUS), following almost real parameters of discrete circuits found in the market, and at the end it was build and tested a prototype.
Excellent results were obtained, thus confirming the idea of the proposed architecture and its application to other signs that need to be controlled without the use of complex circuits or filters that will override both the noisy signals (common mode), but also damage the components of the useful signal (or differential).

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