LAB4D: A Low Power, Multi-GSa/s, Transient Digitizer with Sampling Timebase Trimming Capabilities

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Abstract

The LAB4D is a new application-specific integrated circuit (ASIC) of the Large Analog Bandwidth Recorder and Digitizer with Ordered Readout (LABRADOR) family, for use in direct wideband radio frequency digitization such as is used in ultrahigh energy neutrino and cosmic ray astrophysics. The LAB4D is a single channel switched-capacitor array (SCA) 12-bit sampler with integrated analog-to-digital converters (ADC), developed in the TSMC 0.25\textmu m process. The LAB4D, operating at 3.2 GSa/s, contains 4096 total samples arranged in 32 windows, for a total record length of 1280 ns. The 3 dB bandwidth is approximately 1.3 GHz, with a directly-coupled 50\Omega input. This represents a factor of 16 increase in the sample depth and an increase in analog bandwidth in comparison to the previous generation (LAB3) digitizer. Individually addressable windows allow for sampling and digitization to occur simultaneously, leading to nearly dead time-free kHz readout rates. All biases and current references are generated via internal digital-to-analog converters (DACs), resulting in a digi-

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tizer that requires minimal support circuitry. In addition, the LAB4D contains sample cell timebase trimming capabilities, reducing the intrinsic sample-to-sample time variance to less than 5 ps, an improvement of about 80%. This feature allows the LAB4D to be used in precision timing applications and reduces post-hoc calibration requirements.

**Keywords:**
Electronic detector readout concepts, Front-end electronics for detector readout, Analog to digital converter (ADC), Switched Capacitor Array (SCA), Application Specific Integrated Circuit (ASIC).

1. Introduction

There has been an increasing interest in the development of CMOS switched capacitor array (SCA) samplers due to their low-cost and high performance. These devices have been thoroughly written about in high energy physics literature [1][2][3][4][5][6]. Many have accomplished digitization speeds high enough for greater than Nyquist sampling of a GHz analog bandwidth signal. In addition to their use in precision photon timing [7][8], these ≥GSa/s devices are being used in experiments designed to detect neutrinos [9][10][11] and gamma-rays [12]. SCA samplers are cost-effective alternatives to analog-to-digital converters (ADCs) due to their excellent timing, recording, and high resolution amplitude [13][14].

The analog nature of SCA samplers also limits their widespread acceptance, requiring additional resources and time consuming post-hoc calibrations in order to achieve high performance. To simplify the integration and usage of these digitizers by minimizing or sometimes eliminating the need for on-line or off-line calibrations via software, the LAB4 ASIC design was developed with the goal to demonstrate the ability to trim the inherently non-uniform timebase generated by the CMOS voltage-controlled delay line (VCDL) by the ASIC itself, using simple internal digital-to-analog converters (DACs). A further simplification involved moving all previously-external voltage biases and current references
to internal DACs, resulting in the significant reduction of support electronics needed for digitization.

Another limitation of SCA samplers is the long readout time. While data can be acquired at GSa/s rates, data readout typically is significantly slower (tens of MSa/s). At slower rates (~kHz), a high dead time with each readout can be linked to the lack of sufficient derandomization, and the LABRADOR family of ASICs targeted this issue. For example, a 1024 sample readout at 10 MSa/s would result in the digitizer being unavailable for 102.4 µs, which, at a 1 kHz trigger rate would result in 10% dead time. The LAB4 series integrates improvements stemming from the buffered LABRADOR (BLAB) series of ASICs [15] to achieve simultaneous sampling and readout; acting as a 4-event derandomizer by dividing the total number of samples into multiple windows that can be written to or read out separately. This allows a significant reduc-
tion in dead time. Assuming a random trigger probability, the LAB4D would experience only 0.1% dead time under the previous example.

The LAB4D, the fourth revision of the LAB4 design, was fabricated in the TSMC 0.25 μm CMOS (LO) process, and packaged in a 48-pin quad-flat no-leads (QFN) package to reduce parasitic bondwire inductance. A die image of the LAB4D ASIC is shown in Figure 1. The design and performance results of the LAB4D will be discussed.

2. Architecture

A variety of different CMOS switched capacitor array architectures that are similar to the LAB4D have been discussed in the literature [16]. A compact, minimal storage array was used in order to limit the parasitic and storage capacitance of the SCA [17]. The decision to pursue a compact storage matrix architecture was symbiotic with similar designs being explored for Monolithic Active Pixel Sensors (MAPS) for charged particles [18][19].

The LAB4D architecture is a descendant of the LABRADOR-3 (LAB3) design [20], developed for the Antarctic Impulsive Transient Antenna (ANITA), an ultra-high energy neutrino and cosmic ray balloon-borne observatory. The ANITA experiment requires ~100 sampling channels over 200–1200MHz [21]. Commercial flash ADCs were impractical due to cost and power limitations. The LAB3 ASIC has been successfully deployed on four ANITA long-duration balloon flights and the LAB4D is scheduled to be deployed on future missions.

The features of the LAB4D and LAB3 are summarized in Table 1. All of the LABRADOR ASICs have been fabricated in the TSMC 0.25 μm CMOS (LO) process and all previous generations were packaged in a 64-pin plastic thin quad-flat package (TQFP). The LAB4D was the first to utilize a 48-pin QFN package in order to reduce lead inductance and for improved compactness.

The LABRADOR ASIC ADCs feature a usable signal voltage range of 0–2.5V and the LAB4D’s ADC has an effective readout rate of >100 kSa/s. The LAB4Ds were designed as single channel RF digitizers in order to remove bond-
Table 1: Summary of LABRADOR Specifications and Improvements

| Item                                    | LAB3  | LAB4D |
|-----------------------------------------|-------|-------|
| # RF Inputs                             | 9     | 1     |
| Sample-and-hold cells per input         | 260   | 128   |
| Total number of samples                 | 2340  | 4096  |
| # of ADCs                               | 2340  | 128   |
| Sampling speed control                  | Analog Delay-locked loop |
| RMS of sampling intervals              | 50    | 2.5   |
| 3 dB bandwidth for 50 ohm input (MHz)   | 900   | 1300  |
| Sampling speed [GSa/s]                  | 2.6   | 3.2   |
| Package                                 | 128-pin QFP | 48-pin QFN |

wire and on-die coupling that was present in the LAB3. A general overview of the LAB4D signal processing is shown in Figure 2. As this figure shows, The LAB4D consists of a “primary” sampling array arranged as two blocks of 64 sample-and-hold cells which are directly connected to an externally-terminated 50 Ω RF input. These blocks are transferred to one of four 64-sample “intermediate” storage arrays. Two of the intermediate storage arrays (128 total samples each) are then transferred to the main storage array which is organized into 32 “windows”, corresponding to 4096 total samples. See section 2.1 for more details regarding the sampling architecture.

The 128 sampling intervals run in parallel with a voltage-controlled delay line VCDL and delay-locked-loop (DLL). The DLL fixes the total delay to a master clock that is externally-supplied. Using an external on-board 25 MHz clock, the sampling rate is 3.2 GSa/s. A unique feature of the LAB4D is the ability to tune the individual sampling intervals; allowing the mitigation of the

\[^1\text{This is a desired operating point and not a design limitation}\]
Figure 2: Simplified block diagram for the LAB4D. RF signals are sampled in the primary array, transferred to a secondary storage array in 64-sample chunks, and finally to a 128-sample window in the main storage array of 32 windows. Secondary storage alternates between even (A1/A2) and odd (B1/B2) windows depending on the clock cycle. Timing for sampling and transfer is controlled via configurable taps from a DLL driven by the master clock, and controlled and trimmed via internal DACs. Digitization is performed via an on-die Wilkinson ADC, with programmable ramp current and timing. Data is then read out via a serial LVDS output. DLL configuration, digitization control, and DAC values are all programmable via a custom serial interface.

The analog bandwidth of the LAB4D has been expanded in the high frequency region by 400 MHz in comparison to previous generations of the ASIC. The LAB4D has a storage array of 4096 cells, arranged in 32 blocks of 128. For
the ANITA mission, 8 of these blocks will be read out for each event, which at 3.2 GSa/s results in 320 ns duration waveforms for each event; a 100% increase in comparison to the LAB3. Windows in the main storage array can be written to and read from in a random-access manner using an externally-provided write and read address. The window address is selected for readout by an independent RF trigger unit within the ANITA instrument crate. The storage bank acts as a circular buffer, where the write pointer skips the banks reserved for readout so that they are not overwritten until the readout is complete. The selected window is then digitized in parallel via a Wilkinson (ramp) ADC, and then the final digitized data is shifted out using a high-speed LVDS output.

The use of Gray code was also implemented within the reference counter of the Wilkinson ADC converter. The counter is incremented on every rising edge of the externally supplied Wilkinson clock and is distributed to each of the 128 conversion registers. The use of Gray code in the conversion register prevents erroneous outputs that are intrinsic to standard binary counters when there are very small delays between counter bits. Readout speeds of 20 µs per window are practical, resulting in a readout speed of 6.4 MSa/s.

2.1. Sampling Array

As shown in Figure 2, the LAB4D features a unique two-stage sample transfer architecture which allows for an effective doubling of the settling time into the main storage array. In short, this sampling array utilizes what we call a ping-pong intermediate storage cell method where two sets of 64 primary sampling cells are paired with two intermediate storage cells; essentially working as a 4-event derandomizer. Data from the primary sampling cells are transferred in 64-sample chunks to the intermediate storage arrays (labeled A1, A2, B1, and B2). When the 128 total samples of intermediate storage cell 1 (A1 and B1) become “full”, intermediate storage cell 2 (A2 and B2) is then written to; allowing cell 1 to be transferred to an address (WR_ADDR) in the main storage array (labeled “15” in Figure 3) in a subsequent sampling cycle when the write strobe (WR_STRB) is active.
Figure 3: **Upper**: Timing diagram for the two-stage transfer in the LAB4D. Each time period in the timing diagram corresponds to 64 samples. **Lower**: Data flow in the LAB4D sampling array. Samples are first acquired in the 2 chunks of 64 sampling cells, with timing determined by the SMS[1:128] signals from the VCDL. Vbias/Vbias2 are bias voltages which determine the output amplifier drive strength.

It is the alternating between which sampling array and intermediate storage array the sampling cell writes to, that resembles a ping-pong ball constantly changing its side of the table and, hence, the origin of the terminology. The two-stage transfer that is shown, extends the settling time for the secondary array to a full sampling cycle. The result is an improved decoupling of the primary array from the sampling array, which is necessary given the fact that
the main storage array occupies most of the physical space of the ASIC (see Figure 1) and the samples that are being stored must travel long routes across the chip to reach the designated storage cell.

2.2. Timing Generation

As shown in figure 4, timing for the 128 primary sample-and-hold cells in the LAB4D is controlled by taps from the VCDL in the timing generator. The VCDL is a 128-element delay line, with each element consisting of 2 voltage controlled delays, implemented as current-starved inverters.

The total delay of the VCDL is locked to an external clock using a DLL which compares the external clock after propagating through the VCDL to a non-delayed version of the same clock. The phase comparator output then drives a charge pump, which adjusts the VdlyN control voltage, that in turn adjusts the propagation speed of the high-to-low transitions of the first stage of current starved inverter. This signal is common to all 128 delay stages.

Individual delay stage adjustment is done by adjusting separate VtrimT, set via individual DACs for all 128 stages. By trimming these DAC values, the intrinsic differences between current-starved delays due to process variations can be nulled. Identical copies of these delay pairs are used to delay the priming signal (SSP) and the timing signal (SST), which are used to synthesize the actual Track/Hold signal (SMT). SSP precedes SST and sets the SMT signal high, putting this delay stage’s Switched Capacitor into Track mode. The later arrival of SST, which is a direct and delayed copy of the SSTin reference clock, drives SMT into Hold mode. At each stage a copy of the delayed SST edge (TMK) is extracted and used by a programmable timing generator to synthesize required internal timing strobes, such as SSP (which is actually started at the end of the propagation of the previous SSTin cycle, to permit it to be present prior to the arrival of SST).

The primary purpose of the DLL is to compensate for intrinsic changes in current-starved inverter propagation due to changes in temperature. VdlyP does not adjust the critical rising or timing edge of SST, but rather the falling
2.3. Implementation

Characterization of the LAB4D performance was performed using a 12-channel digitizer designed for the ANITA experiment, the *Sampling Unit for Radio Frequencies*, version 5 (SURFv5). The SURFv5 is a CompactPCI-compatible 6U printed circuit board (PCB), with a single Xilinx Artix-7 field-programmable gate array (FPGA) interfacing with all LAB4Ds and providing a CPU interface.
Figure 5: Image of the Sampling Unit for Radio Frequencies, version 5 (SURFv5), used for LAB4D characterization. Each SURFv5 contains 12 LAB4D ASICs, packaged in a 48-pin QFN package. The LAB4Ds are visible on the left section of the board immediately after the RF conditioning components. The printed circuit board dimensions are 6.3 x 9.2 inches.

for data readout and LAB4D configuration. The incoming RF signals are conditioned with a 200–1200MHz bandpass using Mini-Circuits HFCV-145+ low-pass and LFCN-1200+ high-pass filters. In addition, a copy of the incoming signal was coupled off using a Mini-Circuits TCD-13-4X+ for RF power monitoring, and a calibration signal common to all LAB4Ds was coupled in using an identical coupler. Finally, the AC-coupled signal was 50 Ω terminated to an adjustable DC voltage. A total of nine SURFv5s were manufactured, and two SURFv5s have currently been tested and characterized, for a total of 24 LAB4Ds. Performance of the 24 LAB4Ds were broadly comparable. Each SURFv5 was assigned an identifier associated with a popular Oahu surfing location, as shown in Figure 5.
3. Results

The performance of the LAB4D ASIC as implemented on the SURFv5 was characterized to determine its suitability for RF digitization. Specifically, the noise level, linearity, working range, sample-to-sample timing variation, and analog bandwidth were measured. Next, the stability of these measurements with respect to operating temperature was characterized.

Temperature variations were investigated using 3 LAB4Ds which were coupled using thermal paste to a copper heat sink with a Peltier heater/cooler with a separate heat sink on the opposite side, as well as a thermometer for monitoring the LAB4D temperature. Current through the Peltier device was varied to control the LAB4D temperature.

3.1. Noise

Each individual storage cell in the main storage array develops a slightly different DC offset due to non-uniformity in the fabrication process. These offsets, called “pedestals”, must be measured and removed to recover the input signal. Subtraction of the individual pedestal can easily be done at the point when each sample is read out, since each sample’s subtraction is independent. The measured pedestal values for all LAB4D ASICs on a single SURFv5 is shown in Figure 6. The intrinsic pedestal variation results in a relatively minor $\sim 3.7\%$ reduction in total dynamic range.

Once the individual pedestals are measured and removed, a histogram of the measurements for a terminated input was obtained to determine the overall kTC noise contributions of the switched capacitor based sampling cells and the two storage cells of the LAB4D. The observed total noise is roughly saturated by these contributions and was measured to be $2.19 \text{ ch}$, which corresponds to approximately $1 \text{ mV}$ using a nominal DC transfer function of $2 \text{ ch/mV}$. This noise level is broadly consistent with other SCA samplers and previous generation LABRADOR ASICs and is not expected to be an operational limitation.
Figure 6: **Left:** Distribution of measured pedestal values for a typical LAB4D. The input DC voltage for this measurement was 0.74 V. Measured pedestals ranged from 1600–1750 counts, which corresponds to approximately ∼3.7% of the total dynamic range. **Right:** Terminated input histogram. The spread in measured values is 2.19 ADC channels, which corresponds to 1.08 mV using the DC transfer function in the linear region of 2 ch/mV.

### 3.2. Linearity

After pedestal subtraction, the linearity of the digitization of the LAB4D was characterized. This was performed by conducting single-parameter scans of the DC input voltage to the LAB4D. Over a 1 V span from 500–1500 mV, the DC transfer curve shows an integral non-linearity of better than 2.5% for most of the region, as shown in Figure 7. Also shown in this figure, the transfer curve slope varied by approximately 0.1%/1°C. In addition, pedestal offsets were measured to vary by approximately 0.05%/1°C. DC scans were also conducted for 1024 LAB4D sample cells in order to determine the level of dispersion between cells. Gain dispersion within the linear region was measured to be approximately 2% over all cells.

### 3.3. Sample-to-sample timebase variation

The DLL is first optimized by sampling a 235 MHz sine wave. The individual trim DACs are set to a common approximate delay, which assigns a portion of the delay for each element to be controlled by the trim delay, and the remainder to be controlled by the DLL. Because of internal routing in the delay line, even and odd samples are set to different initial values. Then, a sine wave is fit to a
Figure 7: A best linear fit of single-parameter DC scans of a single sample cell at multiple temperatures are shown where there is an integral non-linearity (INL) of better than 2.5% for about 75% of the region.

single window of data and VtrimT is adjusted so that the fit frequency matches the input frequency. An example of this optimization can be seen in Figure 8. At this point, the average sampling speed of the LAB4D is 128 times the external clock, and the sample-to-sample timing variations can then be tuned.

The individual sample timing is then trimmed using the individual trim DACs. Because the DLL acts to keep the overall delay of the VCDL the same, adjustments in any single sample trim DAC will result in the corresponding adjustment of the timing of that sample and all other samples. That is, slowing down a single sample by 1% using the trim DACs will result in the remaining samples speeding up by \( \frac{1}{127} \)% to compensate.

We therefore use an iterative minimization procedure to determine all trim DAC values simultaneously. This is done by measuring the fraction of observed samples where the observed value (relative to the subsequent sample) crosses the DC pedestal (“zero-crossing fraction”), either positive-going or negative-going,
for 8000 separate waveforms. These 8000 waveforms make up a single iteration in the minimization procedures we discuss throughout this text. This fraction is a simple measure of the width of the time sample, and should be constant if the sample timing is regular. For samples that have a zero-crossing fraction greater than the average, the trim DAC value is decreased, speeding up that sample. Likewise, samples that have a lower-than-average zero-crossing fraction are slowed down by increasing the trim DAC value. Global structure in the delay line is compensated for by appropriate initial estimates of the trim DACs.

This procedure is repeated multiple times, which progressively reduces the variation in the timebase. Within approximately 10 iterations (80,000 waveforms), the RMS variation in the sample-to-sample timing is reduced below 5 ps. The iterative procedure eventually (after about 30-40 iterations) reaches RMS timing variations of approximately 3 ps. The improvement in timing over iteration count, as well as the sample-to-sample timing, can be seen in Figure 9. The decrease in improvement below 5 ps is due to the limited statistics of each iteration, rather than an intrinsic limitation of the timebase tuning procedure. The last intrawindow delay ($t_{127} - t_{126}$) contains an unknown extra delay which is currently under investigation, and results in this sample timing being a noticeable outlier from the other samples. This should be further adjustable by...
Routing in the LAB4D delay line results in an odd/even sample initial timing variation, which is eliminated after tuning. The final sample timing is currently under investigation. Improvement in the RMS of the individual sample timings as a function of the number of iterations. The RMS decreases to below 5 ps within 10 iterations (80,000 waveforms), and further reduces to approximately 3 ps after 32 iterations.

assigning more overall delay to the trim DACs in the calibration procedure. The current calibration procedure primarily targets the differential nonlinearity (DNL) of the timebase for simplicity as well as the fact that the largest timebase variations are an even/odd sample systematic. Future procedural improvement will focus on constraining the timebase INL as well. Initial measurements of timing variations of identical pulses in different channels on the SURFv5 currently show an 8 ps RMS variation, indicating that the INL is relatively controlled by the DLL.

Finally, the stability of the timebase with respect to temperature variation was also investigated. First, the DLL was tuned at a temperature of 30°C and a 210 MHz sine wave was digitized by the LAB4D. Data was then taken between 10°C and 60°C in 10°C intervals, with the DLL enabled, and again with the DLL function disabled, in order to investigate the reduction in temperature sensitivity due to the DLL. The sampling rate was manually set by fixing the voltage which controls the common delay in the VCDL via an internal DAC.

The sampling frequency of the LAB4D was determined again using the zero-
crossings of the recorded data, and the sampling frequency versus temperature is shown in Figure 10. With the DLL disabled, the sampling frequency had a strong temperature dependence, between 500 – 2000 ppm/°C. The action of the DLL reduces that temperature dependence to less than 3 ppm/°C.

Temperature variations also affect the regularization of the sampling time-base. To explore this, the trim DACs were briefly calibrated at both 25°C and 50°C, and then the sample-to-sample time variation was measured from 10–75°C in 5°C steps. The DLL was enabled for all tests. These results are also shown in Figure 10. The sampling variations show a strong temperature dependence with temperature variance. However, over a range of ±10 °C the RMS time variations remained within a factor of 2 of their original calibrations.

3.4. Analog bandwidth

The LAB4D analog bandwidth was measured using the impulse response of the SURFv5. The impulse response was used to avoid effects from sam-
sampling persistence [22] which would be present when using a frequency-swept continuous-wave (CW) source. The SURFv5, as was previously mentioned, has an RF input chain consisting of a Mini-Circuits HFCV-145+ and LFCN-1200+ high and low pass filter, respectively, as well as two TCD-13-4X couplers used to couple off a copy of the input signal and to couple in a low-frequency calibration tone. The bandpass of the input chain is primarily determined by the high and low pass filters, which act to block DC and as an antialiasing filter for the digitizer. A high-frequency impulse generated by a Tektronix AWG5104 was digitized by both the SURFv5 and a Tektronix MSO 5204B oscilloscope with a 2 GHz input bandwidth under identical conditions. Waveforms from the SURFv5 were correlated and averaged to produce the upsampled waveform, shown in Figure 11, along with the impulse viewed by the oscilloscope, shown in Figure 12 for comparison.

To extract the small-signal analog bandwidth, the Fourier transform of the impulse response for both the SURFv5 and the oscilloscope were taken using a ±10 ns Hann window around the peak to eliminate effects from reflections due to imperfect input matching at the coaxial cable connections. The SURFv5 input bandpass was then obtained from a test board using a network analyzer and applied to the oscilloscope response. Finally, the LAB4D de-embedded frequency response was obtained by subtracting the measured SURFv5 response.
Figure 13: The response of the SURFv5, the SURFv5 plus the bandpass filter, and the oscilloscope.

Figure 14: LAB4D de-embedded bandwidth measurement.

from the modified oscilloscope response. The oscilloscope and the de-embedded LAB4D response are shown in Figure 13.

The measured -3 dB point of the LAB4D is approximately 1.3 GHz, with a frequency response flat to within 0.5 dB observed up to 1.1 GHz. This is a conservative measurement, as uncertainty in correlating the corresponding waveforms from the SURFv5 when averaging them will reduce the high-frequency response. The low-frequency response is purely determined by the high-pass filter on the SURFv5. The LAB4D has no intrinsic low-frequency limitation and the frequency response below 200 MHz is expected to be flat. This represents a 44% increase over the LAB3, which had a measured -3 dB point of 900 MHz.

4. Summary

A switched capacitor array device developed in the TSMC 0.25 µm CMOS (LO) process which utilizes a unique “ping-pong” intermediate storage array architecture has been designed, fabricated, and characterized. This ASIC, the LAB4D, has a -3 dB upper analog bandwidth limit of greater than 1.3 GHz, a sampling frequency of 3.2 GSa/s (well above Nyquist minimum for the 200-
1200MHz ANITA band), a sample window length of 320 ns, and features the unique ability to tune the timebase sampling offsets, reducing the RMS time variance between sample cells to be reliably less than 5 ps.

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