A Seventeen Multilevel High-Power Application Inverter with Low Total Harmonic Distortion

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Received 21 March 2021; Revised 23 July 2021; Accepted 12 August 2021; Published 3 September 2021

In this paper, a new topology of multilevel inverter (MLI) is designed with a fewer number of components and low total harmonic distortion (THD) for high-power photovoltaic (PV) systems. The key limitations of conventional MLIs are high total harmonic distortion (THD) and the use of a large number of switching components due to which the cost of the overall inverter is high. In conventional MLIs, THD can be significantly reduced by the addition of a large filter element at the input side; however, it will result in increased size and cost. Thus, achieving a pure sinusoidal AC at the output and to maintain a low THD level is a major issue in conventional MLIs. The proposed MLI has the advantage of decreasing the output THD by using a modified form of the cascaded H-Bridge structure and sine pulse width modulation technique. The proposed inverter consists of 6 unidirectional switches and 2 bidirectional switches, and there is no extra requirement for additional voltage balancing capacitors or clinching diodes. The individual switching states and SPWM operation for generating the gate pulses of the proposed MLI are discussed in detail. Relevant waveforms are plotted, equations are derived, and mathematical analysis is carried out. A steady-state analysis of the proposed MLI demonstrates an output voltage with 17 levels while using only four DC sources. Simulation results of the proposed MLI for single-phase and three-phase structures are obtained, and comparison is carried out with existing MLI topologies which shows that the proposed MLI has significantly low THD and better performance. From the results, it is clear that the proposed MLI has a THD of 3.52% in comparison with four conventional MLIs whose THDs are 6.1%, 6.63%, 7.3%, and 9.93%. Moreover, the proposed MLI generates 17 voltage levels by using only 08 switching devices, whereas the conventional MLIs use more than 10 switching devices for the generation of 15 voltage levels.

1. Introduction

Multilevel inverters are a candidate topology for high-voltage and high-power applications in industries nowadays. Multilevel inverters offer various advantages including low THD, simple to deal with, and compact size as compared to conventional inverters [1–4]. Research is ongoing on MLIs, and there are various topologies available in the literature. The selection of MLI for an application is based upon cost, complexity, losses, and THD. Figure 1 shows the shape of the output voltage of a 7-level MLI [5–9].

A diode-clamped MLI is presented in [10, 11]. As clear by its name, diode-clamped MLI requires a propping device. Capacitors are used for the division of DC voltage into
switches. $N - 1$ switch sets are necessary for the $N$ number of required levels. The drawbacks of this topology are that in between number of diodes and the count of levels, the quadratic association is very difficult to compute, especially when it ends up upsetting when the count of levels gets higher [12, 13].

A flying capacitor MLI is very much similar to the diode-clamped MLI. The flying capacitor MLI requires that the capacitor must be previously charged for its operation. Besides the benefits of low THD, precharging of capacitors is troublesome [14].

The fundamental and well-understood topology is cascaded H-Bridge MLI. This type of MLI has been utilized for single as well as three-phase transformations. This type of MLI utilizes a certain type of H-Bridge that comprises a diode as well as switches. During an instance, 3 levels of voltage are necessary for MLI. It can be achieved by a solitary or single H-Bridge in cascaded H-Bridge MLI. In cascaded H-Bridge MLI, fewer components like capacitors and switches are required. It requires fewer segments when contrasted with different procedures. But every H-bridge MLI requires an independent DC source [5].

A switch ladder MLI is presented in [6] which is a modified form of cascaded H-Bridge MLI. This MLI utilizes few components and provides an output waveform that is almost sine waveform, which has low THD. This topology also uses more components [15].

A simple circuit (Op-Amp) controlled voltage source MLI is presented that utilized PWM strategy for harmonics decrease and demonstrates the best way to produce SPWM distinctive Op-Amp circuits where the passive type of filters is utilized toward the output for the reduction of harmonics; in this way, the components of the inverter are increased [16].

Another inverter named cascaded H-Bridge MLI with a phase disposition technique is presented in [17]. This work introduced a single phase of cascaded H-bridge MLI, and more elevated levels of voltages were attained with less number of parts utilizing the phase disposition system. The number of voltage levels was enlarged; however, this circuit incited high THD [17].

Reduced switch count multilevel inverter topologies using the cascaded structure and switched capacitor techniques have been presented to lower the THD level and reduce the number of switching devices [18–20].

2. Proposed MLI

There are numerous kinds of MLI available in the market. A lot of research is going upon MLI. The layout circuit of the proposed work is displayed in Figure 2. It is an altered elucidation of the H-bridge type of MLI topology. The fundamental bit of leeway of the presented work as compared to the previously discussed work is that we can achieve more output levels by utilizing a minimum number of components. The proposed MLI has fewer switches and offers low total harmonic distortion.

The proposed MLI uses two bidirectional switches and six unidirectional switches. Each bidirectional switch is comprised of two IGBTs; hence, there are ten IGBTs and the number of independent power supplies is four. So the number of circuit elements is not much more. The more noteworthy thing in the proposed topology is that it can generate 17 levels with only eight switches. The number of levels and fewer switches assumes a significant job in the efficiency of the inverter. The increased level in output voltage demonstrates that this inverter has a low THD.

3. Steady-State Analysis of Proposed MLI

The operation of the proposed MLI is such that these ten switches are turned “on” and “off” at regular intervals by using sinusoidal pulse width modulation (SPWM). This is achieved by turning the different switches “on” assigning them 1 in binary form. The other switches are considered “off,” assigning them 0 in binary form. In this way, the switching pattern of all the switches can be determined.

3.1. The 1st Switching Pattern.

In the first switching state pattern, the switches $K_1$, $K_2$, and $S_y$ are turned “on” and the switches $K_3$, $K_4$, $S_x$, and $S_y$ are turned “off,” and the closed-loop path can be seen as shown in Figure 3. The output voltage is equal to zero as there is no available path for the input voltage to finish the loop.

So $V_{out}$ is

$$V_{out} = 0.$$  \hspace{1cm} (1)

3.2. The 2nd Switching Pattern.

In the second switching state pattern, the switches $S_1$, $K_4$, and $S_y$ are turned “on” and the
switches $K_1, K_2, K_3, T_1,$ and $S_x$ are kept “off,” so the circuit diagram can be visualized as in Figure 4. So $V_{out}$ is

$$V_{out} = V_1.$$  \hfill (2)

3.3. The 3rd Switching Pattern. In the third switching state pattern, the switches $S_1, K_3,$ and $S_x$ are turned “on” and the switches $K_1, K_2, K_4, T_1,$ and $S_y$ are kept “off,” so the circuit diagram can be visualized as in Figure 5. So $V_{out}$ is

$$V_{out} = -V_1.$$  \hfill (3)

3.4. The 4th Switching Pattern. In the fourth switching state pattern, the switches $T_1, K_2,$ and $S_y$ are turned “on” and the switches $K_1, K_3, K_4, S_1,$ and $S_x$ are kept “off,” so the circuit path is visualized as shown in Figure 6. So $V_{out}$ is

$$V_{out} = V_2.$$  \hfill (4)

3.5. The 5th Switching Pattern. In the fifth switching state pattern, the switches $T_1, K_1,$ and $S_x$ are turned “on” and the switches $K_2, K_3, K_4, S_1,$ and $S_y$ are kept “off,” so the circuit diagram can be visualized as shown in Figure 7. So $V_{out}$ is

$$V_{out} = -V_2.$$  \hfill (5)

3.6. The 6th Switching Pattern. In the sixth switching state pattern, the switches $K_1, K_4,$ and $S_y$ are turned “on” and the switches $K_2, K_3, S_1, T_1,$ and $S_x$ are kept “off,” so the circuit diagram can be visualized as depicted in Figure 8.
3.7. The 7th Switching Pattern. In the second switching state pattern, the switches $S_x$, $K_2$, and $K_3$ are turned “on” and the switches $K_1$, $K_4$, $T_1$, $S_1$, and $S_y$ are kept “off,” so the circuit diagram can be visualized as depicted in Figure 9.

So $V_{out}$ is

$$V_{out} = -2V_1.$$  \hspace{1cm} (7)

3.8. The 8th Switching Pattern. In the eighth switching state pattern, the switches $K_2$, $K_3$, and $S_y$ are turned “on” and the switches $K_1$, $K_4$, $S_1$, $T_1$, and $S_y$ are turned “off,” so the circuit diagram can be visualized as shown in Figure 10.

So $V_{out}$ is

$$V_{out} = 2V_1.$$  \hspace{1cm} (6)

$$V_{out} = 2V_2.$$  \hspace{1cm} (8)
3.9. The 9th Switching Pattern. In the ninth switching state pattern, the switches $K_1$, $K_4$, and $S_x$ are turned “on” and the switches $K_2$, $K_3$, $S_1$, $T_1$, and $S_y$ are turned “off,” so the circuit diagram can be visualized as depicted in Figure 11.

So $V_{\text{out}}$ is

$$V_{\text{out}} = -2V_2.$$  

(9)

3.10. The 10th Switching Pattern. In the tenth switching state pattern, the switches $S_1$, $T_1$, and $S_y$ are turned “on” and the switches $K_1$, $K_2$, $K_3$, $K_4$, and $S_x$ are turned “off,” so the circuit diagram can be visualized as shown in Figure 12.

So $V_{\text{out}}$ is

$$V_{\text{out}} = V_1 + V_2.$$  

(10)

3.11. The 11th Switching Pattern. In the eleventh switching state pattern, the switches $S_1$, $T_1$, and $S_x$ are turned “on” and the switches $K_1$, $K_2$, $K_3$, $K_4$, and $S_y$ are kept “off,” and the circuit path can be visualized in Figure 13.

So $V_{\text{out}}$ is

$$V_{\text{out}} = -(V_1 + V_2).$$  

(11)

3.12. The 12th Switching Pattern. In the twelfth switching state pattern, the switches $K_1$, $T_1$, and $S_y$ are turned “on” and the switches $K_2$, $K_3$, $K_4$, $S_1$, and $S_x$ are kept “off,” and the circuit path can be visualized in Figure 14.

So $V_{\text{out}}$ is

$$V_{\text{out}} = 2V_1 + V_2.$$  

(12)
Figure 20: Circuit used for calculating switching sequence for $K_1$ switch.

Figure 21: Sine wave and Saw tooth wave generated for calculating $K_1$ switch sequence.
3.13. The 13th Switching Pattern. In the thirteenth switching state pattern, the switches $T_1$, $K_2$, and $S_x$ are turned “on” and the switches $K_1$, $K_3$, $K_4$, $S_1$, and $S_y$ are kept “off,” and the circuit path can be visualized in Figure 15.

So $V_{out}$ is

$$V_{out} = -(2V_1 + V_2).$$  \hspace{1cm} (13)$$

3.14. The 14th Switching Pattern. In the fourteenth switching state pattern, the switches $S_1$, $K_3$, and $S_x$ are turned “on” and the switches $K_1$, $K_2$, $K_4$, $T_1$, and $S_y$ are turned “off,” and the circuit path can be visualized in Figure 16.

So $V_{out}$ is

$$V_{out} = V_1 + 2V_2.$$  \hspace{1cm} (14)$$
3.15. The 15th Switching Pattern. In the fifteenth switching state pattern, the switches $S_1, K_4,$ and $S_x$ are turned “on” and the switches $K_1, K_2, K_3, T_1,$ and $S_y$ are turned “off,” and the circuit path can be visualized in Figure 17.

So $V_{out}$ is

$$V_{out} = -(V_1 + 2V_2). \quad (15)$$

3.16. The 16th Switching Pattern. In the sixteenth switching state pattern, the switches $K_1, K_3,$ and $S_y$ are turned “on” and the switches $K_2, K_4, S_1, T_1,$ and $S_x$ are kept “off,” and the circuit path can be visualized in Figure 18.

So $V_{out}$ is

$$V_{out} = 2V_1 + 2V_2. \quad (16)$$

3.17. The 17th Switching Pattern. In the seventeenth switching state pattern, the switches $K_2, K_4,$ and $S_x$ are turned “on” and the switches $K_1, K_3, S_1, T_1,$ and $S_y$ are kept “off,” the circuit path can be visualized in Figure 19.

So $V_{out}$ is

$$V_{out} = -2(V_1 + V_2). \quad (17)$$

All the switching states and voltage equations calculated for different closed-loop paths of the schematic in Figure 2 are reproduced in Table 1.

### 4. Voltage Stress and Switching Loss Estimation

To generate the gate pulses based on the switching sequence, a carrier-based adjustment technique is used. As all the switches turn on and off thousand times in a second, there is switching power loss in each switching device due to the on state current and off state voltage. In order to estimate the switching losses, the loss in switch $K_1$ is calculated theoretically as follows:

- $V_1 = 25$ volts,
- $V_2 = 75$ volts,
- $V_{O} = 200$ rms,
- $F_{SW} = 1$ Khz,
- $I_{O} = 5$ A.

Voltage stress across switch $K_1$ is given as

$$V_{K_1(\text{Stress})} = V_1 = 25 \text{ volts.} \quad (19)$$

Current stress through switch $K_1$ is given as

$$I_{K_1(\text{Stress})} = 5 \text { amperes.} \quad (20)$$

Switching power loss across switch $K_1$ is given as

$$P_{K_1(\text{SW})} = \frac{1}{6} \left[ V_{K_1(\text{Stress})} \star I_{K_1(\text{Stress})} \star F_{SW} \right] \star \left[ t_r + t_f \right]. \quad (21)$$

$t_r$ and $t_f$ have been taken 20 nanoseconds for a typical $N$-channel Mosfet.
Similarly, the switching losses in other switches can be calculated.

5. Generation of Gate Pulses for Switching Operation

To generate the gate pulses based on the switching sequence, a carrier-based adjustment technique is used since it is useful.
in minimizing THD. An example of the implementation of this technique in MATLAB/Simulink is shown in Figure 20, where switching sequence for switch $K_1$ is generated using a constant SPWM technique. Sine wave and sawtooth waveforms (see Figure 21) are used to generate the switching sequence for switch $K_1$ (see Figure 22).

Figure 20 shows the circuit, used for calculating the switching sequence of pulses, for the $K_1$ switch.

Because of playing out the above SPWM method, pulses produced for the $K_1$ switch are shown in Figure 22.

Figure 22 demonstrates the pulses that are obtained by SPWM activity for the further task of the $K_1$ switch. To decide on the on and off states of a switch, a counter is used. For example, the switching sequence generation is demonstrated for the switch $K_1$ as shown in Figure 23. It can be noted that there are 48 states as calculated by the counter that represents the on and off states of the switching sequence for switch $K_1$. Similarly, switching sequences can be computed for all the switches.

Table 2 demonstrates the total 48 switching sequence for all the eight switches utilized in Figure 2.

6. Results and Discussion

The 17-level multilevel inverter with switches and DC sources was implemented in 203 MATLAB/Simulink as shown in Figure 24. Various values used for generating the simulation results as well as the experimental results are given in Table 3.

6.1. Theoretical Results. For the proposed MLI, a voltage in a ratio of 1:3 needs to be selected. There are two DC sources $V_1$ and $V_2$ and overall four DC sources. These DC sources can be replaced by photovoltaic panels such that $V_1 = 25$ V and $V_2 = 75$ V. It means that $V_2$ is three times $V_1$. Results are obtained for a grid voltage of 200 volts at a frequency of 50 Hz. The switching frequency is 1 kHz. By putting the
estimations of $V_1$ and $V_2$ in Table 1, we get the accompanying results in Table 4.

6.2. Simulation Results. The simulation setup is represented in Figure 24. Each switch is modeled by an IGBT in the simulation. The simulated waveforms are in the accompanying figures. The simulation results confirm the expected results as the THD is brought down to 3.52%.

6.2.1. Single-Phase MLI Simulations. The resulting voltage waveform of single-phase MLI is depicted in Figures 25 and 26; it is compared with a clean sinusoidal waveform of the same frequency to get a good visualization of the reduction in THD.

6.2.2. Three-Phase MLI Simulations. In three-phase MLI, the three phases, namely, phase “a,” phase “b,” and phase “c” are depicted in Figure 27. For phase “b,” a 120-degree phase shift is needed w.r.t phase “a.” Also for phase “c,” another 120-degree phase move w.r.t phase “a” or 120-degree phase shift w.r.t phase “b” is needed. Since there are 48 switching patterns, these need to be accommodated in 360 degrees cycle, so

$$\text{Single Interval Gap} = \frac{360}{48} = 7.5 \text{ degrees}. \quad (23)$$
Inverter 17 level
Pure sine wave

Figure 29: 17-level MLI with $t = 0.03$ for phase a and compared with sine wave.

Inverter 17 level with $-127.5$ phase shift

Figure 30: 17-level MLI with $t = 0.03$ for phase b.

Inverter 17 level with $-127.5$ degree phase shift
Pure sine wave

Figure 31: 17-level MLI with $t = 0.03$ for phase b and compared with sine wave.
Figure 32: 17-level MLI with \( t = 0.03 \) for phase c.

Figure 33: 17-level MLI with \( t = 0.03 \) for phase c and compared with sine wave.

Figure 34: 3-phase 17-level MLI with \( t = 0.03 \).
For 120-degree phase move,

\[ \text{Bits shifts} = \frac{120}{7.5} = 16. \quad (24) \]

Therefore, it should be noted that phase “a” will begin at the first switching pattern and phase “b” at the 17th switching pattern and lastly phase “c” will begin at the 33rd switching pattern and then the cycle repeats itself.

(1) Phase a Results. Figures 28 and 29 show simulation waveforms of phase a for a time duration of 30 milliseconds.

(2) Phase b Results. Figures 30 and 31 show simulation waveforms of phase b for a time duration 30 of milliseconds.

(3) Phase c Results. Figures 32 and 33 show simulation waveforms of phase c for a time duration 30 of milliseconds.

(4) 3-Phase Results. Figures 34–37 show simulation waveforms for all three phases of proposed MLI.

6.3 Fast Fourier Transform Analysis for THD. FFT investigation is done in Simulink/MATLAB to locate the total harmonic distortion on the frequency spectrum (see Figures 38 and 39). Total harmonic distortion is a helpful procedure to break down any nonlinear conduct of a framework, which is normally done with the help of fast Fourier transform (FFT). The measured signal is changed from the time domain into the frequency domain (see Figure 39). The changed information can be shown in an FFT spectrum in which the response signal’s magnitude is plotted versus the frequency. Figure 39 shows the FFT spectrum of a 17-level MLI.
Figure 37: 3-phase MLI output with $t = 0.1$ and compared with sine wave.

Figure 38: Input MLI signal.

Figure 39: FFT spectrum of a 17-level MLI.
We record the harmonics up till the 19th harmonics, and we ignore the values after that because those values were too low and almost near to zero. The amplitude of each harmonic is shown in Table 5.

We plugged the values in the THD equation to calculate THD as follows:

\[
\text{THD} = \sqrt{0.1^2 + 2.3^2 + 0.3^2 + 1.7^2 + 0.5^2 + 0.7^2 + 0.7^2 + 0.5^2},
\]

\[
\text{THD} = \sqrt{0.01 + 2.89 + 5.29 + 1.96 + 0.01 + 0.0001 + 0.49 + 0.49 + 0.25},
\]

\[
\text{THD} = \sqrt{11.6401},
\]

\[
\text{THD} = \frac{11.6401}{100},
\]

\[
\text{THD} = 3.52\%.
\]

6.4. Comparison with Other Topologies. A comparison between the number of switches (see Figure 40), number of voltage levels (see Figure 41), and THD (see Figure 42) was conducted between different multilevel inverters and the proposed multilevel inverter. The proposed 17-level MLI uses the SPWM technique for generating the gate signals/pulses. This inverter uses less number of switches, i.e., 8, and generates a maximum number of voltage levels. It also shows a low THD of 3.52%. The THD, where operational amplifier (Op-Amp) circuits were used for pulse generation, turns out to be 7.3% whereas 180° conduction MLI had 9.93% THD and H-Bridge MLI had 6.63% THD. Another multilevel inverter that uses the space vector modulation technique for generating pulses using switch ladder topology offers 6.1% THD.

From the above discussions, it is clear that the proposed MLI is superior to conventional MLI’s in context of THD, number of switching devices, and voltage levels. The main limitation of proposed MLI is the bad regulation of output voltage and complexity in control of active switches.

7. Conclusions

In this paper, a modified form of a multilevel inverter has been successfully designed for high-power applications. The proposed topology has fewer switches due to which the cost is less. The proposed MLI solution does not require any filter at the output and produces less amount of THD. A thorough inquiry and scrutiny are carried out, and overall switching sequences have been evaluated for the proposed MLI. The THD of the system is 3.5%, and also, there is low voltage stress across the switches and the output is a smooth sinusoidal AC. By setting tailored quality metrics, a theoretical comparison is carried out for the proposed MLI and the conventional MLI’s. The results reflect that the proposed MLI has surpassed the conventional MLI in terms of performance, reduced components, and low total harmonic distortion. The theoretical results have been verified by simulation results in MATLAB/Simulink. The results of the simulations align with the theoretical implications. Due to low
THD, the proposed MLI is a well-anticipated candidate for high-voltage/high-power applications. Considering the literature study done upon the MLI, it was seen that the main issue was concerned with the increased components as well as high THD. All of those parameters were improved by using the proposed topology. To reduce more components like DC sources, two capacitors can be used with only one DC source instead of two in the proposed MLI.

Data Availability

All relevant data and its supporting information files are included within the manuscript.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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