Linear multiport photonic interferometers: loss analysis of temporally-encoded architectures

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Implementing spatially-encoded universal linear multiport interferometers on integrated photonic platforms with high controllability becomes increasingly difficult as the number of modes increases. In this work, we consider an architecture in which temporally-encoded modes are injected into a chain of reconfigurable beamsplitters and delay loops, and provide a detailed loss analysis for this and other comparable architectures. This analysis also yields a straightforward and explicit description of the control sequence needed for implementing an arbitrary temporally-encoded transformation. We consider possible physical implementations of these architectures and compare their performance. We conclude that implementing a chain of reconfigurable beamsplitters and delay loops on an integrated lithium niobate platform could outperform comparable architectures in the near future.

I. INTRODUCTION

Photonic linear multiport interferometers play a crucial role in metrology, telecommunications, and fundamental science. While often imagined and realized as acting on spatial modes, it is also possible to consider them acting on any degree of freedom of the radiation field. In particular, there has been recent interest in linear multiport interferometers that act on time-bins [1–5], the temporal degree of freedom of the electromagnetic field.

The standard way to implement an optical unitary transformation acting on a large number of modes, \( U(N) \) for large \( N \), is to decompose it into a series of \( SU(2) \) and \( U(1) \) unitary transformations. It was shown by Reck, et al. [6] that a universal \( N \)-mode interferometer can be built out of \( N(N - 1)/2 \) beamsplitters and \( N \) phase shifters (see Fig. 1 (a)). The operation of the phase shifters is often considered separate from the operation of the multiport interferometer, and so we make this distinction here as well, focusing on the \( SU(2) \) transformations. For reconfigurability and control, in practice these beamsplitters are commonly implemented as Mach-Zehnder interferometers (MZIs) with two controllable phases (see Fig. 1 (c)). More recently, Clements, et al. [7] proposed another way of decomposing \( U(N) \) into \( N(N - 1)/2 \) beamsplitters and \( N \) phase shifters enabling a more compact spatial implementation (see Fig. 1 (b)); other decomposition methods have been proposed as well [8]. However, the engineering and control of large spatially encoded multiports is nontrivial, even if implemented on a photonic chip [9, 10], and, as such, alternative architectures have also been explored.

One alternative architecture to the spatial encodings mentioned above is the so-called dual-loop architecture proposed for Boson Sampling [1, 2], and later experimentally implemented [4]. It makes use of a temporal encoding, and requires just a single fast reconfigurable beamsplitter. A scheme to achieve universal quantum computation based on the dual-loop architecture and measurement-based non-Gaussian gates was also proposed [3, 5]. As a second alternative, in this work we consider a chain-loop architecture, requiring a sequence of \( N-1 \) fast reconfigurable beamsplitters, but potentially incurring lower loss and being more amenable to integration on a photonic chip than the dual-loop architecture.

In Sec. II we review the dual-loop architecture and introduce the chain-loop architecture in detail. We consider all possible losses intrinsic to each architecture and define intuitive expressions to quantify their overall loss, enabling straightforward and direct comparisons. In Sec. III, using both analytic and numerical tools, we argue that these expressions can be understood as useful heuristic approximations to the total loss averaged over all possible optical paths. In Sec. IV, we consider free-space and chip-based implementations of each loop ar-
chitecture, generating sets of possible numbers for use in formulae developed in the two previous Sections. Finally, we briefly discuss possible applications of our chain-loop architecture in Sec. V before concluding in Sec. VI.

II. LOOP-BASED ARCHITECTURES

In this section, we consider two possible architectures that make use of time-bin encoding to implement a multiport interferometer. We first briefly review a spatially-encoded architecture where the loss analysis is particularly simple. For each loop-based architecture, we develop a method to show clearly how the loss accumulates compared to the spatial architecture. We define expressions to quantify the overall transmission of each architecture based on physical intuition, allowing one to easily make comparisons.

A. Spatially-encoded architecture

Although we focus on loop-based architectures in this work, it is still worthwhile to analyze the loss in a spatially-encoded architecture. On the one hand, the performance of spatial encoding on integrated photonic platforms provides a benchmark for loop-based architectures. On the other hand, it builds intuition for the more complicated loss analysis of the loop-based architectures. Later we will see that we can understand the effect of loss in loop-based architectures as simply related to that in a spatially-encoded architecture.

For an integrated platform implementation, the main source of loss is often propagation loss. This loss is proportional to the length of an optical path. We note that there can be additional losses at each MZI due to bending and cross-talk, however we ignore them here since, in principle, MZIs can be made propagation-loss-limited. It can be difficult to define a single expression to quantify the overall loss of this architecture, as light can travel along many different paths through the chip. However we find that a useful choice is to use the loss suffered in traveling across the entire chip. Using this definition of effective loss, we write the overall transmission as

$$\eta_{SE} = \exp \left( -\alpha C L_{MZI} \right) = \eta_g^N, \quad (1)$$

where $\alpha C$ is the loss coefficient per-unit length, depending on the material from which the interferometer is fabricated, and $L_{MZI}$ is the length of each MZI. From Fig. 1 we can see that, theoretically, the minimum chip size is equal to $NL_{MZI}$ while, in practice, the chip size is usually much larger due to the electronic inputs for each MZI [9]. However, this additional size is not a fundamental limitation, and the purpose of this Subsection is simply to provide a reasonable upper bound for overall architecture transmission, so we do not consider a larger chip size here. We note that a second intuitive way to understand Eq. (1) is to divide the chip into $N$ layers of gates (here each gate is one MZI), giving $\eta_g = \exp \left( -\alpha C L_{MZI} \right)$ the physical meaning of transmission per layer.

B. Dual-loop architecture

The dual-loop architecture, proposed by Motes, et al. [1, 2], consists of a single fast tunable beamsplitter or MZI, two fast switches, one inner delay loop, and one (larger) outer delay loop (see Fig. 2 (a)). All interactions between different temporal modes happen at the tunable beamsplitter (yellow box in Fig. 2 (a)). Taking the input time-bins to be separated by time $\tau$, the inner loop must implement a delay of duration $\tau$. A single pass of temporal modes through the inner loop implements the equivalent of a layer of beamsplitters of the Reck scheme [6] of Fig. 1 (b) (see Fig. 2 (b)). Switches (red boxes in Fig. 2 (a)) and the outer loop guide time-bins back to the inner loop to implement more layers, an operation that must be performed $N - 1$ times to realize a universal $N$-mode linear interferometer. As the outer loop must be able to contain all $N$ time-bins, it needs to implement a delay at least $N$ times longer than the inner loop (i.e., $N\tau$).
From Fig. 2 (a) we see that losses in the dual-loop architecture can occur in any of four different components. We use $\eta_g$, $\eta_i$, $\eta_o$, and $\eta_s$ to denote the transmission or efficiency of the MZI (tunable SU(2) gate), the inner loop, the outer loop, and the switches, respectively. Before a time-bin can interfere with the one behind it, it must pass through a switch, the MZI, and the inner loop. Then it can interfere with the subsequent time-bin at the MZI, before passing through a second switch. To implement another layer, the time-bin must pass through the outer loop, after which it is ready to repeat the process of first switch, MZI, and inner loop.

To enable a more direct comparison with the Reck scheme, and make the details clear, we develop a procedure for inserting losses associated with the dual-loop architecture directly on top of a sketch of a Reck scheme (see Fig. 3 for the 4-mode case). In principle, time-bin $j$ can be released by the second switch at the $j^{th}$ layer. However, doing so causes the time-bins to lose their uniform spacing in time, requiring more complicated detection schemes. We note that not allowing the time-bins to be released “early” effectively increases the number of elements some time-bins must pass through (shown in yellow in Fig. 3), which in turn introduces more loss, but that it does not change the optical depth, or lossiest path, of the architecture. Additionally, more balanced losses can be useful for some applications [7]. For all of these reasons, we defer the analysis of architectures that switch time-bins out to detectors as early as possible to future work.

Using red boxes labeled by an “s” to denote switches, yellow boxes labeled by a “g” to denote MZIs, and green boxes labeled by an “i” or “o” to denote inner and outer loops, respectively, the procedure to mock up a Reck scheme to include dual-loop architecture losses is as follows:

1. Sketch the corresponding Reck decomposition for $U(N)$.

2. Add dashed diagonal lines (shown in red in Fig. 3) to separate the $N - 1$ layers.

3. Add $j - 1$ MZIs (shown in yellow in Fig. 3) to each layer $j$ so that each layer contains $N - 1$ MZIs.

4. Add a gate loss to each of the two output modes of each MZI ($2(N - 1)^2$ in total).

5. At each intersection between a dashed line and quantum wire, add two switch losses and one outer loop loss ($N(N - 2)$ sets in total).

6. Within each layer, add an inner loop loss to the lower input mode and/or upper output mode of each MZI ($N^2$ in total).

7. Within each layer, add just two gate losses: one on the lower input mode to the lowest MZI, and one on the upper output mode or the uppermost MZI. These two extra losses are needed to push the first time-bin into the inner loop, and to push the last time-bin out of the inner loop.

8. Finally, add a switch loss to each mode at the beginning and end of the sketch. These indicate that each time-bin needs to pass through a switch whenever it enters or exists the architecture.

Note that one can also begin with the Clements’ decomposition and, following a similar procedure, end up with the same diagram.

Similar to the definition of Eq. (1), we define the effective overall transmission of the chain-loop architecture to be that experienced in travelling the entire interferometer from input mode $i$ to output mode $i'$ (see Fig. 3). As can be seen in Fig. 3, it has the nice feature that it is the same for each mode and independent of the path taken from input to output. In particular, for an $N = 4$ interferometer, each time-bin passes through 6 MZIs, 6 switches, 3 inner loops, and 2 outer loops. In general, this can be written as

$$\eta_{DL} = \left(\eta_s^2\eta_i^2\eta_o\right)^{N-1}\eta_s^{-1}. \quad (2)$$

In Sec. IV we estimate the size of these transmission factors by considering possible realizations in the laboratory. As compared to spatial encodings, the required number of physical beamsplitters in the dual-loop architecture is greatly reduced. However, the introduction of delay loops, in particular the outer loop, as well as fast reconfigurable components, may increase photon loss.
C. Chain-loop architecture

As a compromise between the large potential complexity of spatially-encoded architectures and large potential loss of the dual-loop architecture as $N$ increases, here we consider a chain-loop architecture, making use of temporal encoding and schematically shown in Fig. 4. A chain-loop architecture implementing an $N$-mode universal interferometer consists of $N-1$ MZIs and $N-1$ delay loops. For input time-bins separated by time $\tau$, each loop must implement a delay $\tau$ equal to that of the inner loop of the dual-loop architecture. Note that there is no constraint on the delay $d$ between two adjacent tunable beamsplitters and it can be chosen such that $d \ll \tau$. The number of optical components of the chain-loop architecture increases linearly with the size of the interferometer, whereas the number of optical components of the spatially-encoded architectures increases quadratically. Therefore the control complexity of the chain-loop architecture is reduced with respect to the spatially-encoded architectures. Additionally, there is no need for fast switches in and out of long delay lines in the chain-loop architecture, and therefore the amount of coupling loss is reduced with respect to the dual-loop architecture.

Here, each MZI plus loop in the chain implements a layer of beamsplitters of the Reck scheme of Fig. 1 (b). With reference to Fig. 4, it is seen that the only reductions in transmission are from the MZIs, which we denote by $\eta_i$, and propagation through the delay loops, which we denote by $\eta_g$. To detail and help make clear how these transmission factors accumulate, similar to above, we develop a procedure for inserting losses associated with the chain-loop architecture directly on top of a sketch of a Reck scheme (see Fig. 5 for the 4-mode case). We use yellow boxes labeled with a “g” to indicate MZIs and green boxes labeled with an “i” to indicate loops.

The procedure to mock up a Reck scheme to include chain-loop architecture losses is as follows:

1. Sketch the corresponding Reck decomposition for $U(N)$.

2. Add dashed diagonal lines (shown in red in Fig. 5) to separate the $N-1$ layers.

3. Add $j-1$ MZIs (shown in yellow in Fig. 5) to each layer $j$ so that each layer contains $N-1$ MZIs.

4. Add a gate loss to each of the the two output modes of each MZI ($2(N-1)^2$ in total).

5. Within each layer, add loop loss to the lower input mode and/or upper output mode of each MZI ($N^2$ in total).

6. Finally, within each layer, add just two gate losses: one on the lower input mode to the lowest MZI, and one on the upper output mode or the uppermost MZI. These two extra losses are needed to push the first time-bin into a loop, and to push the last time-bin out of a loop.

As can be seen in Fig. 5, the effective transmission here, as for the dual-loop architecture, is the same for each mode and independent of the path taken from input to output. In particular, for an $N = 4$ interferometer, each time-bin passes through 6 MZIs and 3 loops. In general, this can be written as

$$\eta_{\text{CL}} = (\eta_g^2 \eta_i)^{N-1}.$$  (3)

Comparing with Eq. (2), we find that the effective transmission of the chain-loop is larger than that of the dual-loop by $\eta_g^2 \eta_i$ per layer—exactly the excess loss introduced by the outer loop and switches. However, it is not clear that physical implementations will have the same $\eta_g$ or $\eta_i$ for each architecture, and thus not immediately obvious, even without introducing questions of scalability and control complexity, which architecture is best for a particular application. Before exploring these questions in more detail in Sec. IV, we first place our definitions of $\eta$ on more solid mathematical footing.

III. QUANTIFYING OVERALL TRANSMISSION

Although we can fully describe the lossy interferometer by its transformation on mode operators, it is not immediately obvious how to quantify its effective loss. In the previous section, we proposed using the overall loss connecting input modes $\{i\}$ to output modes $\{i'\}$, as a measure of loss in each loop-based architecture. Although this quantity is by no means rigorous, it carries some physical intuition and is easy to calculate. In the present section, we justify this measure by showing that it can be understood as a kind of average loss over all possible optical paths. Before that, we first briefly review how to mathematically model a multi-mode lossy channel.

An ideal universal multiport interferometer is characterized by the unitary transformation

$$\hat{a} \rightarrow U\hat{a},$$  (4)
lossy channel [11]
tion, the interferometer is characterized by a multi-mode
gate. Not exit immediately after traversing its final required
paths across the interferometer are very close to
⟨η⟩; (ii) ⟨η⟩ is very close to ⟨ηmax⟩ and they each scale with N approximately the
same way. Point 2) indicates that losses suffered by most
paths through the interferometer are very close to ⟨ηmax⟩,
which suggests certain degree of uniformity. Note that
these observations hold throughout extensive numerical
simulations and we just present one set of representa-
tive parameters in Fig. 7. Therefore, ⟨η⟩ may be a more

where \( \hat{a} := (\hat{a}_1, \ldots, \hat{a}_N)^T \) are the annihilation operators for each mode. Any unitary can be decomposed into
a series of nearest-neighbor two-mode SU(2) gates [6, 7]
(physically these gates are usually implemented as MZIs).
Let \( R_{n,m} \) be the \( i \)th two-mode unitary acting on modes
\( n \) and \( m \). Then, for a given decomposition, we have

\[
U = \prod_i R_{n_i, n_i+1}.
\tag{5}
\]

For spatial encoding there will be \( N(N-1)/2 \) such two-
mode gates [6, 7]. For loop-based architectures (see Fig. 3
and Fig. 5) there will be \( (N-1)^2 \) gates because light does
not exit immediately after traversing its final required
gate.

When loss is included, instead of a unitary transformation,
the interferometer is characterized by a multi-modal
lossy channel [11]

\[
\hat{a} \rightarrow A\hat{a} + \sqrt{1 - AA^*} \hat{e},
\tag{6}
\]

where \( 0 < AA^* \leq I \), \( A \) is the process matrix and \( \hat{e} \)
are modes of the environment. The process matrix is
constructed by inserting loss matrices in between two-
mode unitaries

\[
A = \prod_i L_{n_i, n_i+1} R_{n_i, n_i+1}.
\tag{7}
\]

Here \( L_{n,n+1} \) only acts on the \( n \)th and \( (n + 1) \)th modes
and can be written as

\[
L_{n,n+1} = \begin{pmatrix}
\sqrt{\eta_n} & 0 \\
0 & \sqrt{\eta_{n+1}}
\end{pmatrix},
\tag{8}
\]

where \( \eta_n \) and \( \eta_{n+1} \) are the losses suffered by the output
modes of the \( n \)th gate. The values of \( \eta_n \) can be found by
looking at diagrams like those shown in Fig. 3 and Fig. 5.

From Eq. (7) we can see that losses and unitary trans-
forms are mixed together, making the loss analysis non-
trivial. Therefore, to quantify the loss, we follow Ref. [12]
and first exploit the fact that for any \( A \), there exists a sin-
gular value decomposition \( A = V \lambda W \) where \( V \) and \( W \)
are unitary matrices and \( \lambda = \text{diag}(\sqrt{\eta_1}, \ldots, \sqrt{\eta_N}) \). As
we can see from Fig. 6, after the decomposition, losses in
different paths are captured by \( N \) effective and indepen-
dent lossy channels and are completely separated from
the unitary transformation. Therefore, the average value
given by

\[
\bar{\eta} = \frac{1}{N} \sum_{i=1}^{N} \eta_i,
\tag{9}
\]
could be a good measure of the average loss among all
possible paths.

To better understand and compare the definition of
average transmission in Eq. (9) and those in Eq. (2) and
Eq. (3), we resort to numerical simulation. For each ar-
chitecture, we randomly draw unitaries from the Haar
measure, calculate the corresponding process matrix, and
extract its singular values. We then calculate the maxi-
mum, minimum, average, and standard deviation of \( \{\eta_i\} \),
denoted by \( \eta_{\text{max}}, \eta_{\text{min}}, \bar{\eta}, \) and \( \delta \eta \), respectively. In Fig. 7
we plot the average value of these quantities over 50 ran-
dom Haar unitaries for several values of \( N \). We make
two observations from our simulation results: (i) The in-
tuitive definitions of Eqs. (2) and (3) always overestimate
the loss compared to the average \( \langle \bar{\eta} \rangle \); (ii) \( \langle \bar{\eta} \rangle \) is very close
to \( \langle \eta_{\text{max}} \rangle \) and they each scale with \( N \) approximately the
same way. Point 2) indicates that losses suffered by most
paths through the interferometer are very close to \( \langle \eta_{\text{max}} \rangle \),
which suggests certain degree of uniformity. Note that
these observations hold throughout extensive numerical
simulations and we just present one set of representa-
tive parameters in Fig. 7. Therefore, \( \bar{\eta} \) may be a more

FIG. 5. Implementation of a 4-mode interferometer with chain-loop architecture. Each time all 4 time-bins travel through a
loop, one layer of the Reck scheme is applied. Different layers are separated by red dashed lines. Losses resulting from different
optical components are indicated by different boxes: yellow boxes labeled by a “g” for MZIs, and green boxes labeled by “i”
for loops. A detailed procedure outlining how to construct this figure and others like it is given in the main text.

FIG. 6. Singular decomposition of the process matrix. Here \( W, V \) are unitary matrices and \( \{\eta_i\} \) are \( N \) independent lossy
channels. Thanks to this decomposition, we can separate the
losses from the unitary transformation which is convenient for
our loss analysis.
between the maximal and minimal values, and are far more close to the center compared to $\langle \bar{\eta} \rangle$. It is in this sense that we consider the heuristic transmissions defined in Eq. (2) and Eq. (3) as valid measures of average loss. In fact, when the loss is not close to uniform (for instance if we allow time-bins to exit the architecture after they complete the last interaction they need to participate in, causing diagrams in Fig. 3 and Fig. 5 to become triangular in shape) our intuitive definitions are perhaps better measures of the average loss than $\langle \bar{\eta} \rangle$.

IV. POSSIBLE PHYSICAL IMPLEMENTATIONS

In this Section, we consider potential physical implementations of different architectures. Again we first discuss a spatially-encoded architecture, which we later use as a benchmark for temporally-encoded loop-based architectures. We then consider free-space implementations of both loop-based architectures. Although this implementation is not so realistic for the chain-loop when $N$ is large, it is a useful way to give a fair comparison between the two architecture encodings. To overcome problems of size and stability for the chain-loop, we then consider what would be possible with integrated platforms. We expect the chain-loop architecture to benefit most from an integrated design, as it does not require a long delay loop like the dual-loop architecture does. Thus we restrict our consideration of integrated designs to those based on the chain loop architecture. We examine both currently available technology as well as what might be hoped for in the near future.

Although we seek to compare various multiport interferometer architectures, and are not overly concerned with input state generation or output state detection in this work, it is true that generation and detection components could influence $\tau$. On the state generation side, it is not unreasonable to imagine creating input states separated in time by the repetition period of the laser driving their generation. Taking the repetition rate of a state of the art telecommunications-band mode-locked laser to be in the GHz range, we can safely assume that input state time-bins can be as near to each other as 1 ns. As for detection, while current number-resolving detection systems do not operate at these speeds [13], we point out that other detection schemes are possible including multiplexing of number-resolving detectors, and technology is always improving. As such, we compare dual-loop and chain-loop architectures both with a minimum $\tau$ of 1 nanosecond.

A. Spatial encoding with integrated platforms

With its large index of refraction enabling tight bends and small component footprints, silicon is an attractive platform for integrated spatially-encoded interferometers. Recent work implemented 7 layers of MZIs in approximately 1.6 mm [9], giving $L_{\text{MZI}} \sim 235 \mu\text{m}$. Using a propagation loss of 2.4 dB/cm [9] and Eq. (1), we estimate the transmission per layer of this implementation of a spatially-encoded multiport to be $\eta_L \sim 0.987$. If we are more optimistic that one day the propagation loss in silicon-based platforms can be dropped to 0.03 dB/cm [14], this is further improved to a transmis-
sion of 0.998 per layer. In general, we expect spatially-encoded interferometers on integrated platforms to suffer less loss than those of loop-based architectures, due to the absence of any additional lossy components such as delay loops or switches. However, we note that it becomes increasingly difficult to control the MZIs, not to mention sources and detectors, as the number of modes becomes large. It is at this point that loop-based architectures start to become a better option.

B. Dual-loop architecture in free space

In free space, the $\tau$ for the dual-loop architecture could be limited by the fast switches necessary for the reconfigurable beamsplitters and/or switches in and out of the outer delay loop. These switches would be implemented in a fast electro- or acousto-optic material. Commercial bulk, free-space coupled, modulators operate at hundreds of MHz [15], and so here we consider $\tau = 10$ ns.

The inner loop would likely be implemented in free space, leading to $\eta_i \sim 1$, but the outer loop, if required to be long enough, would likely be implemented in fiber. Thus, in addition to any reduced transmission from the switch in and out of the outer delay loop itself, we must also consider coupling loss in and out of the fiber. The refractive index of a silica fiber at 1560 nm is $n \sim 1.4$, and so we estimate an outer loop size $N\tau c/n \sim 2.1$ m. We take the propagation loss in the fiber to be 0.2 dB/km, and thus the transmission to be approximately $\eta_o \sim 0.9999^N$ or $\sim 0.9951$ for $N = 50$.

Lastly, the dual-loop MZI makes use of two free-space coupled modulators, and each switch makes use of one free-space coupled modulator. These have 98% transmission [15]. Additionally, the dual-loop architecture will suffer loss when coupling in and out of the outer delay loop fiber of $\sim 0.3$ dB. Thus, the MZI has a transmission of $\eta_g \sim 0.9604$, and each switch transmission plus coupling efficiency works out to approximately $\eta_g \sim 0.9146$. These, and all other transmission factors discussed in this Section are summarized in Table I.

C. Chain-loop architecture

1. Free space

As with the free-space implementation of the dual-loop architecture, the chain-loop architecture $\tau$ would be limited by free-space coupled modulators to 10 nanoseconds. In fact, in theory nothing would change and we would have $\eta_i \sim 1$, and $\eta_g \sim 0.9604$. However, because the light would not be refocused by the outer delay loop at regular intervals, it requires additional optical components such as lenses, which would introduce loss. Additionally, phase stability over the entire beam path would ultimately limit the number of modes $N$ that a free-space chain-loop architecture could act on. Thus, while it may have an advantage over a free space implementation of the dual-loop architecture for small $N$, a free space implementation of the chain-loop architecture would become impractical for large $N$. For large $N$, it may benefit from being implemented on an integrated platform.

2. Current integrated platform

To get around issues of phase stability and control complexity, we can imagine placing the entire chain-loop structure on a photonic chip. Propagation losses in an integrated platform are larger than in free space or even fiber, but sizes are smaller, and modulators are faster. In particular low-loss integrated lithium niobate electro-optic modulators operating at several GHz have recently been demonstrated [16], and so we can consider lithium niobate as the platform for an integrated chain-loop architecture.

For $\tau = 1$ ns and considering the index of refraction in lithium niobate to be $n \sim 2.2$ at 1560 nm, we estimate a chain-loop architecture delay loop size of $\tau c/n \sim 14$ cm. Taking the propagation loss in the integrated lithium niobate platform to be 2.7 dB/m [17], we have $\eta_i \sim 0.9188$. To implement each tunable gate, the chain-loop architecture must use two integrated lithium niobate modulators for each MZI, each with a loss of $\sim 0.5$ dB [16] which yields $\eta_g \sim 0.7943$.

Note that the 14 cm delay loops can be arranged in a spiral configuration to save space (see Fig. 8), occupying an area on the order of 1 mm$^2$. Even so, we note that only so many of them can be made to fit on a single chip. As a way around this, one can imagine connecting multiple chips (see Fig. 9 for a schematic) to extend the length of the chain indefinitely. Compared to coupling issues for spatial-encoding schemes when they run out of space on chip, with several modes needing to be coupled from chip to chip, here there is just a single spatial mode to couple. However, we do note that integrated chain-loop architectures will run out of space more quickly, and that any chip-to-chip coupling will increase loss. Estimating this coupling loss requires the knowledge of specifics of experimental implementation, we neglect this coupling loss in the present work.

3. Future integrated platform

In the future we can imagine the integrated lithium niobate modulators to be propagation loss limited. As they are only about 3 mm long [18], this would result in $\eta_g \sim 0.9981$. Furthermore, if we imagine propagation losses in integrated lithium niobate to come down to that of certain polished lithium niobate structures [18] or 0.3 dB/m, we would instead have $\eta_i \sim 0.9906$ and $\eta_g \sim 0.9998$. 


FIG. 8. A schematic of an MZI with a delay loop. The MZI consists of two (static) 50:50 beamsplitters and two phase shifters with phases \( \theta \) and \( \phi \). The phase \( \theta \) is used to control the effective transmission and \( \phi \) is simply a phase shift. In practice the delay loop would be arranged in a spiral such that it occupies a small area.

FIG. 9. Chain-loop architecture on chip. Two chips (big grey boxes) are schematically shown. Each small green box on the chip is a MZI plus a delay loop, which is shown in Fig. 8. The small red boxes are couplers that connect different chips. A very large interferometer can be implemented by concatenating more chips.

D. Simulation and performance comparison

Finally, we use the definitions of average loss from Sec. II and Sec. III to compare the performance of loop-based architectures with different physical implementations. We summarize the transmission values discussed in Sec. IV in Table I.

| Component | DL FS | CL FS | CL I, current | CL I, future |
|-----------|------|-------|---------------|-------------|
| Inner loop | \( \sim 1 \) | \( \sim 1 \) | 0.9188 | 0.9006 |
| Outer loop | 0.9999 | N/A | N/A | N/A |
| MZI | 0.9604 | 0.9604 | 0.7943 | 0.9998 |

TABLE I. Transmission efficiencies through components of each considered loop architecture. DL: dual-loop, CL: chain-loop, FS: free-space, I: integrated. We take values consistent with the literature, though note that the chain-loop architecture in free space is limited in size, and that the future values for the chain-loop architecture in an integrated platform may be overly optimistic.

In Fig. 10 (a) we plot the average losses defined in Eq. (2) and Eq. (3). In (b) we plot \( \langle \tilde{\eta} \rangle \) defined in Eq. (9) averaged over 50 random Haar unitaries. We use the data in Tab. I for both subplots. We find that the difference between these two definitions is only noticeable for sufficiently large loss. For the regime where \( \eta > 0.1 \), these two measures are almost indistinguishable. This is confirmed by looking at the two insets, where the average loss is plotted without rescaling. Summarizing these figures, it is obvious that for small, controllable, phase-stable interferometers, a chain-loop architecture implemented in free space is likely the best option. However, as the interferometer gets larger, current integrated modulator technology will limit the utility of the chain-loop architecture on chip, leading the dual-loop architecture in free space to likely be the best option. On the other hand, integrated modulator technology does not need to become all that much better for integrated chain-loop architectures to become the lowest loss option. Comparing the loss per layer of each architecture, namely \( \eta^{2}_{g,DL} \eta_{h,DL}^{2} \eta_{i,DL} \) and \( \eta^{2}_{g,CL} \eta_{h,CL} \), we see that, taking \( \eta_{i,DL} \sim 1 \), when

\[
\eta_{g,CL} \geq \eta_{g,DL} \eta_{h,CL} \sqrt{\eta_{i,DL}/\eta_{i,CL}},
\]

the chain-loop architecture implemented on a chip will be a competitive option.

V. APPLICATIONS

Boson sampling and its variations are probably the most obvious and straightforward applications of loop-based architectures, but are definitely not the only ones. Due to its simplicity, boson sampling is one of the most promising routes to demonstrate quantum supremacy in the near term [19, 20]. Indeed, boson sampling motivated the proposal of the dual-loop architecture [1, 2] and many recent demonstrations of integrated linear optics [9, 10, 16, 21]. With proper modification, loop-based architectures can be adapted to universal quantum computation [3, 5]. Finally, the utility of loop-based architectures is not limited to quantum information processing, for generalized spatial mode converters [22, 23] and optical neural networks [24] are examples of classical optical applications. In the following we describe the aforementioned optical applications in more detail.

A. Boson sampling

A boson sampler, first introduced by Aaronson and Arkhipov in 2010 [25], is a non-universal quantum machine where \( N \) single photons are sent into a \( M \)-mode interferometer, followed by detection with photon-number-resolving (PNR) detectors. A BosonSampling (BS) problem can be formulated based on this setup: given a boson sampler, output a sample from the exact or approximate output photon distribution. It has been
proven that this problem cannot be efficiently solved by any classical computer [25] unless the polynomial hierarchy collapses, which is believed to be highly unlikely in the computer science community [26]. The hardness of BS is rooted in the hardness of calculating permanents, which was proved to be in the \#P-complete complexity class [27]. Due to its experimental simplicity compared to fault-tolerant universal quantum computation, boson sampling is one of the most promising candidates to demonstrate quantum supremacy in the near future [19, 20].

The original proposal by Aaronson and Arkhipov did not consider photon loss, which would be present in any realistic implementation of BS. Therefore, it is paramount to ask if the LOSSYBOSON SAMPLING problem is still hard to simulate. Aaronson and Brod proved that sampling from a lossy boson sampler is still hard if the number of lost photons remains constant as the number of input photons increases — an unrealistic situation, considering the nature of optical loss in physical systems. Later Rahimi-Keshari et al. showed that exact lossy BS is always hard under the assumption of perfect detection [28]. Using quite different methods, both García-Patrón et al. [12] and Oszmaniec and Brod [29] proved that approximate BS is efficiently simulable if the number of remaining photons is $O(\sqrt{N})$. These results eliminate most experimental platforms where the photon loss scales exponentially with the system size.

Computational complexity theorists are concerned with the asymptotic behavior of an algorithm, however any experimental demonstration will always be at some finite problem size. Therefore, questions such as how much transmission $\eta$ is enough for a given input photon number $N$ to achieve a quantum advantage is perhaps more meaningful to an experimentalist. In Ref. [30] the authors presented a quantum supremacy region over the $\eta-N$ plane. In general, the larger the loss the more photons required to show a quantum advantage. For instance, with 50 input photons, $\eta \gtrsim 0.7$ [30] is required to have a non-zero quantum advantage. By looking at Fig. 10, none of the architectures with current experimental parameters can reach this threshold. Even the chain-loop architecture implemented on lithium niobate with optimistic parameters can barely reach this threshold. We note that losses in photon sources and detectors are not included in Fig. 10. Together with the fact that recently a fast classical algorithm has been proposed [31], demonstrations of quantum supremacy using boson sampling are extremely challenging for current technology.

**B. Gaussian boson sampling**

Inspired by a variation of BS [32], Hamilton et al. proposed to replace the single photon input states with single-mode squeezed vacuum states. It is this setup we refer to as Gaussian boson sampling (GBS) [33, 34]. By showing that the output distribution of GBS is directly related to the hafnian of a certain matrix [35], the authors argued that GBS is also a hard problem modulo some conjectures similar to those in the original BS paper [25].

Implementing GBS is expected to be less challenging than implementing BS since single-mode squeezed states can be generated deterministically and with high indis-
tistinguishability. Another important difference between GBS and BS is that post-selection is not an option anymore. This means that we have to consider the lossy GBS problem where the task is to sample from the output distribution of a Gaussian boson sampler. Although a detailed study of lossy GBS has yet to be presented, it is clear that a low-loss scalable implementation will be required, as the inclusion of loss is expected to make classical simulations of GBS easier. On the other hand, classical algorithms for calculating the hafnian and simulating GBS have recently been tested on the Titan supercomputer [36, 37].

We note that it appears likely that GBS could have applications beyond simply demonstrating quantum supremacy. Due to the closeness between the hafnian and graph theory, much progress has been made on using GBS to solve graph-related problems including the search of dense subgraphs [38, 39], calculating perfect matchings of graphs [40], and identifying isomorphic graphs [41]. Interestingly, a slight extension of GBS (to include displacement at the inputs) can be used to sample from the vibronic spectrum of molecules [42, 43]. Finally, a state-preparation scheme based on GBS was recently proposed and significant improvement on previous methods has been shown [44].

The dual-loop architecture not only can implement a universal linear interferometer, but also can be adjusted to achieve universal quantum computation [3, 5]. Similarly, one can straightforwardly adjust the chain-loop architecture to achieve universal quantum computation by introducing measurement-induced non-Gaussian gates [45–48]. The proposed universal quantum computing architecture is shown in Fig. 11. A chain which concatenates \( N \) delay loops and implements an \( N \)-mode linear interferometer is closed to form a loop. The purpose is to repeatedly use the chain to implement linear unitary transformations, which are necessary for universal quantum computation. Between these linear transformations, we can implement measurement-induced gates (either squeezing or non-Gaussian gates) by successively feeding resource states (ancilla modes) into the loop, and performing homodyne detection and feedforward.

### D. Spatial mode converters

In addition to the quantum applications listed above, there are several classical applications of a mesh of \( SU(2) \) operations. Such meshes, encoded spatially, can be used to implement any linear optical transformation, enabling self-aligning optical mode couplers, combiners, trackers, and separators (see Ref. [23] and references therein). Similar techniques could readily be applied to the temporally-encoded chain-loop architecture, which should come with reduced control complexity and small loss in the near future.

### E. Optical neural networks

Artificial neural networks are a computing paradigm for machine learning tasks originally inspired by the human brain [49]. Rather than relying on a program that explicitly tells it precisely what to do at each step, a neural network “learns” from observational data. They have been used successfully for e.g., image and speech recognition. Recently, there has been interest in optical implementations of artificial neural networks [24, 50]. These implementations require a multiport photonic interferometer as well as a nonlinear element, such as a saturable absorber, and promise speed and power efficiencies compared to electronic implementations. Already, a few-layer spatially-encoded multiport photonic interferometer implemented in silicon with the nonlinearity simulated on a computer has demonstrated accuracy comparable to a 64-bit computer for a vowel recognition problem [24]. As control complexity increases, the temporally-encoded chain-loop architecture could become a viable candidate for future optical neural networks.

### VI. CONCLUSIONS

We have presented new loop-based temporally-encoded architecture to implement universal unitary transformation. We also presented a useful and intuitive framework to evaluate the effective overall loss associated with different physical implementations of temporally-encoded linear multiport interferometers. We justified their use...
with analytic and numerical calculations demonstrating that, while they may slightly overestimate the “true” average interferometer loss, they are sufficient to allow for quick and straightforward comparisons, enabling faster progress when comparing interferometric architectures. A procedure is developed for connecting the losses associated with either a dual-loop or chain-loop architecture to the more conventional spatially-encoded architecture, furnishing a clear mapping between spatial and time-encoded decompositions. We expect these results to be useful for targeting the optimal architecture for a diverse range of applications, both quantum and classical. We showed that our chain-loop architecture could outperform dual-loop systems pending realistic near-term improvements to nanophotonic lithium niobate platforms, further motivating experimental efforts to drive down losses in such platforms.

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