On the Computational Power of Spiking Neural P Systems with Self-Organization

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Neural-like computing models are versatile computing mechanisms in the field of artificial intelligence. Spiking neural P systems (SN P systems for short) are one of the recently developed spiking neural network models inspired by the way neurons communicate. The communications among neurons are essentially achieved by spikes, i.e. short electrical pulses. In terms of motivation, SN P systems fall into the third generation of neural network models. In this study, a novel variant of SN P systems, namely SN P systems with self-organization, is introduced, and the computational power of the system is investigated and evaluated. It is proved that SN P systems with self-organization are capable of computing and accept the family of sets of Turing computable natural numbers. Moreover, with 87 neurons the system can compute any Turing computable recursive function, thus achieves Turing universality. These results demonstrate promising initiatives to solve an open problem arisen by Gh Păun.

In the central nervous system, there are abundant amount of computational intelligence precipitated throughout millions of years of evolution. The computational intelligence has provided plenty of inspirations to construct powerful computing models and algorithms1–3. Neural-like computing models are a class of powerful models inspired by the way how neurons communicate. The communication among neurons is essentially achieved by spikes, i.e. short electrical pulses. The biological phenomenon has been intensively investigated in the field of neural computation4. Using different mathematic approaches to describe neural spiking behaviours, various neural-like computing models have been proposed, such as artificial neural networks5 and spiking neural networks6. In the field of membrane computing, a kind of distributed and parallel neural-like computation model, named spiking neural P systems (SN P systems), were proposed in 20067. SN P systems are widely considered as a promising variant of the third generation of neural network models8.

Generally, an SN P system can be represented by a directed graph, where neurons are placed in nodes and the synapses are denoted using arcs. Every neuron can contain a number of spikes and a set of firing (or spiking) rules. Following the firing rules, a neuron can send information encoded in spikes to other neurons. Input neurons read spikes from the environment, and output neurons emit spikes into the environment. The computation result can be embodied in various ways. One of the common approaches is the time elapsed between the first two consecutive spikes sent into the environment9,10 and the total number of spikes emitted into the environment11–13.

For the past decade, there have been quite a few research efforts put forward to SN P systems. Notably, SN P systems can generate and accept the sets of Turing computable natural numbers14, generate the recursively enumerable languages15,16 and compute the sets of Turing computable functions17. Inspired by different biological phenomena and mathematical motivations, lots of variants of SN P systems have been proposed, such as SN P systems with anti-spikes18,19, SN P systems with weight20, SN P systems with astrocyte21, homogenous SN P systems22,23, SN P systems with threshold24, fuzzy SN P systems25,26, sequential SN P systems27, SN P systems with rules on synapses28, SN P systems with structural plasticity29. For applications, SN P systems are used to design logic gates, logic circuits30 and operating systems31, perform basic arithmetic operations32,33, solve combinatorial optimization problems34, diagnose fault of electric power systems35.

SN P systems are known as a class of neural-like computing models under the framework of membrane computing36. Spiking neural network (shortly named SNN) is a well known candidate of spiking neural network.
models\textsuperscript{37}, which incorporates the concept of time into their operating model, besides neuronal and synaptic state in general artificial neural networks. The neuron in SNN cannot fire at each propagation cycle, but only when a membrane potential reaches a specific value. When a neuron fires, it generates a signal which travels to other neurons which, in turn, increase or decrease their potentials in accordance with this signal. In SN P systems, spiking rules, denoted by formal production in grammar theory of formal languages, is used to describe the neuron’s spiking behaviour, which determine the conditions of triggering spiking, the number of spikes consumed, and the number of spikes emitting to the neighboring neurons. The spikes from different neurons can be accumulated in the target neuron for further spiking. In terms of motivation of models, SN P systems also fall into the spiking neural network models, i.e., the third generation of neural network models.

Since SN P systems have more fundamental data structure (spike trains, i.e., binary strings), it performs well in achieving significant computation power with using a small number of units (neurons). It was proved by Gh Păun that 49 neurons are sufficient for SN P systems to achieve Turing universality. But, for conventional artificial neural networks, it was shown that 886 sigmoid function based processors are needed to achieve Turing universality\textsuperscript{38}.

In the nervous system, synaptic plasticity forms the cell assemblies with the self-organization of neurons, which induces ordered or even synchronized neural dynamics replicating basic processes of long-term memory\textsuperscript{39,40}. The self-organizing principle in the developing nervous system and its importance for preserving and continuing neural system development provide us insights on how neural-like networks might be reorganized and configured in response to environment changes. Enlightened by the biological fact, self-organizing artificial neural networks with unsupervised and supervised learning have been proposed and gain their popularity for visualization and classification\textsuperscript{41,42}. It is still an open problem as formulated by Gh Păun in ref. 43, to construct SN P systems with self-organization and to use the system to perform possible computer vision and pattern recognition tasks.

**Results**

In this research, a novel variant of SN P systems, namely SN P systems with self-organization, is proposed and developed. The system initially has no synapse, but the synapses can be dynamically formed during the computation, which exhibits the self-organization behaviour. In the system, creation and deletion rules are used to create and delete synapses. The applications of synapse creation and deletion rules are controlled by the states of the involved neurons, i.e., the number of spikes contained in the neurons. The computational power of the system is investigated as well. As a result, it demonstrates that SN P systems with self-organization can compute and accept any set of Turing computable natural numbers. Moreover, with 87 neurons, the system can compute any Turing computable recursive function, ergo achieves Turing universality.

Before stating the results in mathematical forms, some notations should be introduced. \( N_{\text{SPSO}_{\text{cre}}, \text{del}} \text{ (rule)} \) (resp. \( N_{\text{SPSO}_{\text{cre}}, \text{del}} \text{ (rule)} \)) denotes the family of sets of numbers computed (resp. accepted) by SN P systems with self-organization of degree \( m \), where \( h \) (resp. \( h' \)) indicates the maximal number of synapses that can be created using a synapse creation rule, \( g \) (resp. \( g' \)) is the maximal number of synapses that can be deleted by using a synapse deletion rule, \( r \) (resp. \( r' \)) is the maximal number of rules in each neuron, and the subscript \( \text{all} \) indicates the computation result is encoded by the number of spikes emitted into the environment (resp. the subscript \( \text{acc} \) indicates the system works in the accepting mode). If the parameters are not bounded, i.e., there is no limit imposed on them, then they are replaced with \(*\). \( \text{NRE} \) denotes the family of Turing computable sets of numbers\textsuperscript{44}.

The main results of this work can be mathematically depicted by the following theorems.

**Theorem 1.** \( N_{\text{SPSO}_{\text{cre}}, \text{del}} \text{ (rule)} = \text{NRE} \).

**Theorem 2.** \( N_{\text{SPSO}_{\text{cre}}, \text{del}} \text{ (rule)} = \text{NRE} \).

**Theorem 3.** There is a universal SN P system with self-organization having 87 neurons for computing functions.

These results show that SN P systems with self-organization are powerful computing models, i.e., they are capable of doing what Turing machine can do. Also, they provide potential and theoretical feasibility of using SN P systems to solve real-life problems, such as pattern recognition and classification.

In SN P system with self-organization, it has no initially designed synapses. The synapses can be created or deleted according to the information contained in involved neurons during the computation. In previous work, it was found that the information diversing ability of synapses had some programmable feature for SN P systems, but the computation power of SN P systems without initial synapses is an open problem. Although this is not the first time the feature of creating or deleting synapses investigated in SN P systems, see e.g. SN P systems with structural plasticity, it is quite the first attempt to construct SN P systems has no initial synapses.

**Methods**

In this section, it starts by the mathematical definition of SN P system with self-organization, and then the computation power of SN P systems with self-organization is investigated as number generator, acceptor and function computing devices. It is proved in constructive ways that SN P systems with self-organization can compute and accept the family of sets of Turing computable natural numbers. With 87 neurons, such system can compute any Turing computable recursive function.

**Spiking Neural P Systems with Self-Organization.** Before introducing the definition of SN P system with self-organization, some prerequisites of basic concepts of formal language theory\textsuperscript{45} are recalled.

For an alphabet \( V \), \( V^* \) denotes the set of all finite strings of symbols from \( V \), the empty string is denoted by \( \lambda \), and the set of all nonempty strings over \( V \) is denoted by \( V^+ \). When \( V = \{ a \} \) is a singleton, then we write simply \( a^n \) and \( a^+ \) instead of \( \{ a \}^n \), \( \{ a \}^+ \). A regular expression over an alphabet \( V \) is defined as follows: (1) \( \lambda \) and each \( a \in V \) is
a regular expression; (2) if \(E_i\) and \(E_j\) are regular expressions over \(V\), then \((E_i \cup E_j)\) and \((E_i \cap E_j)\) are regular expressions over \(V\); (3) nothing else is a regular expression over \(V\).

For each regular expression \(E\), a language \(L(E)\) is associated, defined in the following way: (1) \(L(\lambda) = \{\lambda\}\) and \(L(\alpha) = \{\alpha\}\), for all \(\alpha \in V\); (2) \(L(E_1 \cup E_2) = L(E_1) \cup L(E_2)\); (3) \(L(E_1 \cap E_2) = L(E_1) \cap L(E_2)\); (4) \(L(E_1)^+ = L(E_1) \cup L(E_1)^+\) for all regular expressions \(E_i, E_j\) over \(V\). Unnecessary parentheses can be omitted when writing a regular expression, and \((E)^+\) can also be written as \(E^*\). By NRE we denote the family of Turing computable sets of numbers. (NRE is the family of length sets of recursively enumerable languages—those recognized by Turing machines).

An SN P system with self-organization of degree \(m \geq 1\) is a construct of the form

\[
\Pi = (O, s_1, s_2, \ldots, s_m, syn_{00}, in, out)
\]

where

- \(O = \{a\}\) is a singleton, where \(a\) is called the spike;
- \(\sigma_1, \sigma_2, \ldots, \sigma_m\) are neurons of the form \(\sigma_i = (n_i, R_i)\) with \(1 \leq i \leq m\), where
  - \(n_i \in N\) is the initial number of spikes contained in neuron \(\sigma_i\);
  - \(R_i\) is a finite set of rules in neuron \(\sigma_i\) of the following three forms:
    1. (spiking rule): \(E/\alpha a^c \rightarrow a^d; d\), where \(E\) is a regular expression over \(O\), \(d \geq 0\) and \(c \geq p \geq 0\);
    2. (synapse creation rule): \(E'/\alpha a^c \rightarrow + (\alpha'' \sigma, \text{cre}(i))\), where \(E'\) is a regular expression over \(O\), \(\text{cre}(i) \subseteq [\sigma_1, \sigma_2, \ldots, \sigma_m]\) and \(c' \geq p' \geq 1\);
    3. (synapse deletion rule): \(E''/\alpha a^c \rightarrow - (\lambda, \text{del}(i))\), where \(E''\) is a regular expression over \(O\), \(\text{del}(i) \subseteq [\sigma_1, \sigma_2, \ldots, \sigma_m]\)
- \(\text{syn}_{00}\) is a finite set of synapses, which means no synapse is initially set; at any moment \(t\), the set of synapses is denoted by \(\text{syn}_t \subseteq \{1, 2, \ldots, m\} \times \{1, 2, \ldots, m\}\);
- \(in, out \in \{1, 2, \ldots, m\}\) indicates the input and output neuron, respectively.

A spiking rule of the form \(E/\alpha a^c \rightarrow a^d; d\) is applied as follows. If neuron \(\sigma_i\) contains \(k\) spikes, and \(a^d \in L(E), k \geq c\), then rule \(E/\alpha a^c \rightarrow a^d; d \in R_i\) can be applied. It means that \(c\) spikes are consumed and removed from neuron \(\sigma_i\), i.e., \(k - c\) spikes are remained, while the neuron emits \(p\) spikes to its neighboring neurons after \(d\) steps. (It is a common practice in membrane computing to have a global clock defined. The clock is used to mark the time of the whole system and ensure the system synchronization.) If \(d = 0\), then the \(p\) spikes are emitted out immediately, if \(d = 1\), then the \(p\) spikes are emitted in the next step, etc. If the rule is used in step \(t\) and \(d \geq 1\), in then steps \(t, t + 1, \ldots, t + d - 1\) the neuron is closed (this corresponds to the refractory period from neurobiology), so that it cannot receive new spikes (if a neuron tries to send spikes to a neuron in close status, then these particular spikes will be lost). In the step \(t + d\), the neuron fires and opens again status, so it can receive spikes (which can be used starting with the step \(t + d + 1\), when the neuron can again apply rules). It is possible that \(p\) is associated with value 0. In this case, neuron \(\sigma_i\) consumes \(c\) spikes without emitting any spike. Spiking rule with \(p = 0\) is also called forgetting rule, by which a pre-defined number of synapses can be removed out of the neuron. If \(E = \alpha^d\), then the rule can be written in the simplified form \(\alpha a^c \rightarrow a^d; d\) and if \(d = 0\), then the rule can be simply written as \(E/\alpha a^c \rightarrow a^d\).

Synapse creation and deletion rules are used to create and delete synapses during the computation. Synapse creation rule \(E'/\alpha a^c \rightarrow + (\alpha'' \sigma, \text{cre}(i))\) is applied as follows. If neuron \(\sigma_i\) has \(k'\) spikes such that \(a'' \in L(E'), k' \geq c'\), then the synapse creation rule is applied with consuming \(c''\) spikes, creating synapses to connect neuron \(\sigma_i\) to each neuron in \(\text{cre}(i)\) and emitting \(p'\) spikes to each neuron in \(\text{cre}(i)\). If neuron \(\sigma_j\) has \(k''\) spikes such that \(a'' \in L(E')\) and \(k'' \geq c''\), then synapse deletion rule \(E''/\alpha a^c \rightarrow - (\lambda, \text{del}(i))\) is applied, consuming \(c''\) spikes from neuron \(\sigma_i\) and deleting all the synapses connecting neuron \(\sigma_i\) to the neurons from \(\text{del}(i)\). With the synapse creation and deletion rules, \(E'\) and \(E''\) are regular expressions over \(O = \{a\}\), which regulate the application of synapse creation and deletion rules. This means that synapse creation and deletion rules can be used if and only if the neuron contain some particular numbers of spikes, i.e., the neuron is in some specific states. With the applications of synapse creation and deletion rules the system can dynamically rebuild its topological structure during the computation, which is herein defined as self-organization.

One neuron is specified as the input neuron, through which the system can read spikes from the environment. The output neuron has a synapse creation rule of the form \(E'/\alpha a^c \rightarrow + (\alpha'', \emptyset)\), where the environment is labelled by 0. By using the rule, the output neuron creates a synapse pointing to the environment, and then it can emit spikes into the environment along the created synapse.

For each time step, as long as there is one available rule in \(R_i\), neuron \(\sigma_i\) must apply the rule. It is possible that there are more than one rule that can be used in a neuron at some moment, since spiking rules, synapse creation rules and synapse deletion rules may be associated with regular languages (according to their regular expressions). In this case, the neuron will non-deterministically uses one of the enabled rules. The system works sequentially in each neuron (at most one rule from each \(R_i\) can be used), and if parallelism is designed for the system, all the neurons at the same system level have at least one enabled rule activated.

The configuration of the system at certain moment is defined by three major factors which are the number of spikes contained in each neuron, the number of steps to wait until it becomes open and the current set of synapses. With the notion, the initial configuration of the system is \((n_0/0, n_0/0, \ldots, n_m/0, 0)\). Using the spiking, forgetting, synapse creation and deletion rules as described above, we can define transitions among configurations. Any sequence of transitions starting from the initial configuration is called a computation. A computation halts, also called successful, if it reaches a configuration where no rule can be applied in any neuron in the system. For each
successful computation of the system, a computation result is generated, which is total the number of spikes sent to the environment by the output neuron.

System II generates a number \( n \) as follows. The computation of the system starts from the initial configuration and finally halts, emitting totally \( n \) spikes to the environment. The set of all numbers computed in this way by II is denoted by \( N_{\text{II}}(\Pi) \) (the subscript \( \text{all} \) indicates that the computation result is the total number of spikes emitted into the environment by the system). System II can also work in the accepting mode. A number \( n \) is read through input neurons from the environment in form of spike train \( 10^{n-1} \), which will be stored in a specified neuron \( \sigma_{1} \) in the form of \( f(n) \) spikes. If the computation eventually halts, then number \( n \) is said to be accepted by II. The set of numbers accepted by II is denoted by \( N_{\text{II}}(\Pi) \).

It is denoted by \( N_{\text{SPSOall}}(\text{cre}_\epsilon, \text{del}_\epsilon, \text{rule}_\epsilon) \) the family of sets of numbers computed (resp. accepted) by SN P systems with self-organization of degree \( m \), where \( h \) (resp. \( h' \)) indicates the maximal number of synapses that can be created with using a synapse creation rule, \( g \) (resp. \( g' \)) is the maximal number of synapses that can be deleted with using a synapse deletion rule, \( r \) (resp. \( r' \)) is the maximal number of rules in each neuron, and the subscript \( \text{all} \) indicates the computation result is encoded by the number of spikes emitted into the environment (resp. the subscript \( \text{acc} \) indicates the system works in an accepting mode). If the parameters are not bounded, i.e., there is no limit imposed on them, then they are replaced with \( \infty \).

In order to compute a function \( f: \mathbb{N} \rightarrow \mathbb{N} \) by SN P systems with self-organization, \( k \) natural numbers \( n_{1}, n_{2}, \ldots, n_{k} \) are introduced in the system by reading from the environment a spike train (which is a binary sequence) \( z = 10^{n_{k}} \cdots 10^{n_{1}} \cdots 1 \). The input neuron has a synapse pointing from the environment, by which the spikes can enter it. The input neuron reads a spike in each step corresponding to a digit 1 from the string \( z \); otherwise, no spike is received. Note that exactly \( k + 1 \) spikes are introduced into the system through the input neuron, i.e., after the last spike, it is assumed that no further spike is coming to the input neuron. The output neuron has a synapse pointing to the environment from it, by which the spikes can be emitted to the environment. The result of the computation is the total number of spikes emitted into the environment by the output neuron, hence producing \( r \) spikes with \( r = f(n_{1}, n_{2}, \ldots, n_{k}) \).

SN P systems with self-organization can be represented graphically, which is easier to understand than that in a symbolic way. A rounded rectangle with the initial number of spikes and rules is used to represent a neuron and a directed edge connecting two neurons represents a synapse.

In the following proofs, the notion of register machine is used. A register machine is a construct \( M = (m, H, l_{0}, l_{0}, I) \), where \( m \) is the number of registers, \( H \) is the set of instruction labels, \( l_{0} \) is the start label, \( l_{0} \) is the halt label (assigned to instruction \( \text{HALT} \)), and \( I \) is the set of instructions; each label from \( H \) labels only one instruction from \( I \), thus precisely the following forms:

- \( l_{i} : (\text{ADD}(r), l_{j}, l_{k}) \) (add 1 to register \( r \) and then go to one of the instructions with labels \( l_{j}, l_{k} \)),
- \( l_{i} : (\text{SUB}(r), l_{j}, l_{k}) \) (if register \( r \) is non-zero, then subtract 1 from it, and go to the instruction with label \( l_{j} \); otherwise, go to the instruction with label \( l_{k} \)),
- \( l_{i} : \text{HALT} \) (the halt instruction).

As number generator. A register machine \( M \) computes a number \( n \) as follows. It starts by using initial instruction \( l_{i} \) with all registers storing number 0. When it reaches halt instruction \( l_{0} \), the number stored in register \( 1 \) is called the number generated or computed by register machine \( M \). The set of numbers generated or computed by register machine \( M \) is denoted by \( N(M) \). It is known that register machines compute all sets of numbers which are Turing computable, hence they characterize NRE, i.e., \( N(M) = \text{NRE} \), where \( \text{NRE} \) is the family of Turing computable sets of numbers.

Without loss of generality, it can be assumed that in the halting configuration, all registers different from the first one are empty, and that the first register is never decremented during the computation (i.e., its content is only added to). When the power of two number generating devices \( D_{1} \) and \( D_{2} \) are compared, number zero is ignored; that is, \( N(D_{1}) = N(D_{2}) \) if and only if \( N(D_{1}) = \{0\} = N(D_{2}) = \{0\} \) (this corresponds to the usual practice of ignoring the empty string in language and automata theory).

**Theorem 4.** \( N_{\text{SPSOall}}(\text{cre}_\epsilon, \text{del}_\epsilon, \text{rule}_\epsilon) = N_{\text{RE}} \).

**Proof.** It only has to prove \( \text{NRE} \subseteq N_{\text{SPSOall}}(\text{cre}_\epsilon, \text{del}_\epsilon, \text{rule}_\epsilon) \), since the converse inclusion is straightforward from the Turing–Church thesis (or it can be proved by the similar technical details in Section 8.1 in ref. 46, but is cumbersome). To achieve this, we use the characterization of \( \text{NRE} \) by means of register machines in the generative mode. Let us consider a register machine \( M = (m, H, l_{0}, l_{0}, I) \) defined above. It is assumed that register 1 of \( M \) is the output register, which is never decremented during the computation. For each register \( r \) of \( M \), let \( s_{r} \) be the number of instructions of the form \( l_{i} : (\text{SUB}(r), l_{j}, l_{k}) \), i.e., the number of SUB instructions acting on register \( r \). If there is no such SUB instruction, then \( s_{r} = 0 \), which is the case for the first register \( r = 1 \). In what follows, a specific SN P system with self-organization II is constructed to simulate register machine \( M \).

System II consists of three modules--ADD, SUB and FIN modules. The ADD and SUB modules are used to simulate the operations of ADD and SUB instructions of \( M \); and the FIN module is used to output a computation result.

In general, with any register \( r \) of \( M \), a neuron \( \sigma_{r} \) in system II is associated; the number stored in register \( r \) is encoded by the number of spikes in neuron \( \sigma_{r} \). Specifically, if register \( r \) stores number \( n \geq 0 \), then there are \( 5n \) spikes in neuron \( \sigma_{r} \). For each label \( l_{i} \) of an instruction in \( M \), a neuron \( \sigma_{l_{i}} \) is associated. During the simulation, when neuron \( \sigma_{l_{i}} \) receives 6 spikes, it becomes active and starts to simulate instruction \( l_{i} : (\text{OP}(r), l_{j}, l_{k}) \) of \( M \): the
process starts with neuron \( \sigma_i \) activated, operates on the number of spikes in neuron \( \sigma_r \), as requested by \( \sigma_P \), then sends 6 spikes into neuron \( \sigma_j \), which becomes active in this way. Since there is no initial synapse in system II, some synapses are created to pass spikes to target neurons with synapse creation rules, after that the created synapses will be deleted when simulation completes by synapse deletion rules. When neuron \( \sigma_{i_0} \) (associated with the halting instruction \( l_0 \) of \( M \)) is activated, a computation in \( M \) is completely simulated by system II.

The following describes the works of ADD, SUB, and FIN modules of the SN P systems with self-organization.

**Module ADD (shown in Fig. 1): Simulating the ADD instruction \( l_i : (ADD(r), l_j, l_k) \).**

Initially, there is no synapse in system II, and all the neurons have no spike with exception that neuron \( \sigma_{i_0} \) has 6 spikes. This means system II starts by simulating initial instruction \( l_i \). Let us assume that at step \( t \), an instruction \( l_i : (ADD(r), l_j, l_k) \) has to be simulated, with 6 spikes present in neuron \( \sigma_{i_0} \) (like \( \sigma_{i_0} \) in the initial configuration) and no spike in any other neurons, except in those neurons associated with registers.

At step \( t \), neuron \( \sigma_{i_0} \) has 6 spikes, and synapse creation rule \( a^5/a^3 \rightarrow + (a^3, \{l_{i_1}^{(1)}, l_{i_1}^{(2)}, r\}) \) is applied in \( \sigma_{i_1} \). It generates three synapses connecting neuron \( \sigma_{i_0} \) to neurons \( \sigma_{i_1}^{(1)}, \sigma_{i_1}^{(2)} \) and \( \sigma_r \). Meanwhile, it consumes 5 spikes (one spike remaining) and sends 5 spikes to each of neurons \( \sigma_{i_1}^{(1)}, \sigma_{i_1}^{(2)} \) and \( \sigma_r \). The number of spikes in neuron \( \sigma_{i_0} \) is increased by 5, which simulates adding 1 to register \( r \) of \( M \). At step \( t + 1 \), neuron \( \sigma_{i_1} \) deletes the three synapses created at step \( t \) by using rule \( a \rightarrow - (\lambda, \{l_{i_1}^{(1)}, l_{i_1}^{(2)}, r\}) \). At the same moment, neuron \( \sigma_{i_1} \) uses synapse creation rule \( a^5/a^3 \rightarrow + (a^3, \{l_{i_2}, l_{i_2}\}) \), and creates two synapses to neurons \( \sigma_{i_2} \) and \( \sigma_{i_2} \), as well as sends 3 spikes to each of the two neurons. At step \( t + 2 \), neuron \( \sigma_{i_2} \) deletes the two synapses by using synapse deletion rule \( a \rightarrow - (\lambda, \{l_{i_2}, l_{i_2}\}) \). In neuron \( \sigma_{i_2} \), there are 5 spikes at step \( t + 1 \) such that both of synapse creation rules \( a^5/a^3 \rightarrow + (a^3, \{l_{i_2}, l_{i_2}\}) \) and \( a^5/a^3 \rightarrow + (a^3, \{l_{i_2}, l_{i_2}\}) \) are enabled, but only one of them is non-deterministically used.

- If rule \( a^5/a^3 \rightarrow + (a^3, \{l_{i_2}, l_{i_2}\}) \) is chosen to use, neuron \( \sigma_{i_2}^{(1)} \) creates a synapse and sends 3 spikes to neuron \( \sigma_{i_2} \). In this case, neuron \( \sigma_{i_2}^{(1)} \) accumulates 6 spikes, which means system II starts to simulate instruction \( l_i \) of \( M \). One step later, with one spike inside neuron \( \sigma_{i_2}^{(1)} \) uses rule \( a \rightarrow - (\lambda, \{l_{i_2}, l_{i_2}\}) \) to delete the synapse to neuron \( \sigma_{i_2}^{(1)} \) and neuron \( \sigma_{i_2}^{(1)} \) removes the 3 spikes (from neuron \( \sigma_{i_2}^{(1)} \)) by the forgetting rule \( a^3 \rightarrow - \lambda \).

- If rule \( a^5/a^3 \rightarrow + (a^3, \{l_{i_2}, l_{i_2}\}) \) is selected to apply, neuron \( \sigma_{i_2}^{(1)} \) creates a synapse and sends 3 spikes to neuron \( \sigma_{i_2} \). Neuron \( \sigma_{i_2} \) accumulates 6 spikes, which indicates system II goes to simulate instruction \( l_i \) of \( M \). One step later, neuron \( \sigma_{i_2} \) removes the 3 spikes by using forgetting rule \( a^3 \rightarrow - \lambda \), and the synapse from neuron \( \sigma_{i_2}^{(1)} \) to \( \sigma_{i_2} \) is deleted by using rule \( a \rightarrow - (\lambda, \{l_{i_2}, l_{i_2}\}) \) in neuron \( \sigma_{i_2}^{(1)} \).

Therefore, from firing neuron \( \sigma_{i_2} \), system II adds 5 spikes to neuron \( \sigma_r \) and non-deterministically activates one of the neurons \( \sigma_{i_2} \), which correctly simulates the ADD instruction \( l_i : (ADD(r), l_j, l_k) \). When the simulation of ADD instruction is completed, the ADD module returns to its initial topological structure, i.e., there is no synapse in the module. The dynamic transformation of topological structure and the numbers of spikes in neurons of ADD module during the ADD instruction simulation with neuron \( \sigma_{i_2} \) or \( \sigma_i \) finally activated is shown in Figs 2 and 3. In the figures, the spiking rules are omitted for clear illustration, neurons are represented by circles with the number of spikes and directed edges is used to represent the synapses.

**Module SUB (shown in Fig. 4): Simulating the SUB instruction \( l_i : (SUB(r), l_j, l_k) \).**

Given starting time stamp \( t \), system II simulates a SUB instruction \( l_i : (SUB(r), l_j, l_k) \). Let \( s \) be the number of SUB instructions acting on register \( r \) and the set of labels of instructions acting on register \( r \) be \( \{l_{i_1}, l_{i_2}, \ldots, l_{i_s}\} \). Obviously, it holds \( s \in \{l_{i_1}, l_{i_2}, \ldots, l_{i_s}\} \).
Figure 2. The dynamic transformation of topological structure and the numbers of spikes in neurons of ADD module during the ADD instruction simulation with neuron $\sigma_{l_j}$ finally activated.

Figure 3. The dynamic transformation of topological structure and the numbers of spikes in neurons of ADD module during the ADD instruction simulation with neuron $\sigma_{l_k}$ finally activated.

Figure 4. Module SUB simulating the SUB instruction.
At step $t$, neuron $\sigma_1$ has 6 spikes, and becomes active by using synapse creation rule $a^4a^6 \rightarrow + (a^4, [i_1(1), i_2(2)])$, creating synapses and sending 4 spikes to each of neurons $\sigma_{i1}, \sigma_{i2}$ and $\sigma_r$. With 4 spikes inside, neurons $\sigma_{i1}$ and $\sigma_{i2}$ keep inactive at step $t+1$ because no rule can be used. In neuron $\sigma_r$, it has the following two cases.

- If neuron $\sigma_r$ has 5n ($n > 0$) spikes (corresponding to the fact that the number stored in register $r$ is $n$, and $n > 0$), then by receiving 4 spikes from neuron $\sigma_1$, it accumulates $5n + 4$ spikes and becomes active by using rule $a^4(a^6)^n + (a^6, [i_1(1), i_2(2)] | s = i_1, i_2, ..., i_n)$ at step $t+1$. It creates a synapse to each of neurons $\sigma_{i1}, \sigma_{i2}$ and $\sigma_r$ with $s = i_1, i_2, ..., i_n$ and sending 6 spikes to the neurons. By consuming 8 spikes, the number of spikes in neuron $\sigma_r$ becomes $5n + 4 - 8 = 5(n - 1) + 1$ ($n \geq 0$) such that rule $a^4(a^6)^n \rightarrow + (\lambda, [i_2(1), i_2(2)] | s = i_1, i_2, ..., i_n)$ is enabled and applied at step $t+2$. With application of the rule, neuron $\sigma_r$ removes the synapses from neuron $\sigma_r$ to neurons $\sigma_{i1}, \sigma_{i2}$, $s = i_1, i_2, ..., i_n$. Meanwhile, neurons $\sigma_{i1}$ and $\sigma_{i2}$ with $s \neq i$ remove the 6 spikes by using forgetting rule $a^4a^6 \rightarrow + \lambda$, and neuron $\sigma_{i1}, \sigma_{i2}$ removes the 10 spikes by forgetting rule $a^{10} \rightarrow \lambda$. Neuron $\sigma_r$ accumulates 10 spikes (4 spikes from neuron $\sigma_1$, and 6 spikes from neuron $\sigma_r$), and rule $a^{10}(a^6 \rightarrow + (a^6, [i_1(1)])$ is applied at step $t+2$, creating a synapse and sending 6 spikes to neuron $\sigma_{i1}$. In this case, neuron $\sigma_{i1}$ receives 6 spikes, which means system II starts to simulate instruction $I_4$ of $M$.

One step later, the synapse from neuron $\sigma_r$ to neuron $\sigma_{i1}$ is deleted by using synapse deletion rule $a \rightarrow + (\lambda, [i_1(1)])$.

If neuron $\sigma_r$ has no spike (corresponding to the fact that the number stored in register $r$ is 0), then by receiving 4 spikes from neuron $\sigma_1$, it has 4 spikes and rule $a^4(a^6)^n \rightarrow + (a^6, [i_1(1), i_2(2)] | s = i_1, i_2, ..., i_n)$ is used, creating a synapse to each of neurons $\sigma_{i1}, \sigma_{i2}$ with $s = i_1, i_2, ..., i_n$ and sending 3 spikes to the neurons. Neuron $\sigma_r$ remains one spike, and synapse deletion rule $a^4(a^6)^n \rightarrow + (\lambda, [i_1(1), i_2(2)] | s = i_1, i_2, ..., i_n)$ is applied at step $t+2$, removing the synapses from neuron $\sigma_r$ to neurons $\sigma_{i1}, \sigma_{i2}$ with $s = i_1, i_2, ..., i_n$. At the same moment, neurons $\sigma_{i1}, \sigma_{i2}$ with $s \neq i$ remove the 3 spikes by using forgetting rule $a^4 \rightarrow + \lambda$, and neuron $\sigma_{i1}, \sigma_{i2}$ removes 7 spikes by spiking rule $a^4 \rightarrow \lambda$. Having 7 spikes, neuron $\sigma_{i1}$ becomes active by using rule $a^4a^6 \rightarrow + (a^6, [i_1(1)])$ at step $t+2$, creating a synapse to neuron $\sigma_1$ and sending 6 spikes to neuron $\sigma_{i1}$. In this case, neuron $\sigma_{i1}$ receives 6 spikes, which means system II starts to simulate instruction $I_4$ of $M$. At step $t+3$, neuron $\sigma_{i1}$ uses rule $a \rightarrow + (\lambda, [i_1(1)])$ to remove the synapse to neuron $\sigma_{i1}$.

The simulation of SUB instruction performs correctly: System II starts from $\sigma_1$, having 6 spikes and becoming active, and ends in neuron $\sigma_r$ receiving 6 spikes (if the number stored in register $r$ is great than 0 and decreased by one), or in neuron $\sigma_{i1}$ receiving 6 spikes (if the number stored in register $r$ is 0).

When the simulation of SUB instruction is completed, the SUB module returns to its initial topological structure, i.e., there is no synapse in the module. The dynamic transformation of topological structure and the numbers of spikes in involved neurons in the SUB instruction simulation with neuron $\sigma_{i1}$ (resp. neuron $\sigma_{i2}$) finally activated is shown in Fig. 5 (resp. Fig. 6).

Module FIN (shown in Fig. 7) – outputting the result of computation.

Assume that at step $t$ the computation in $M$ halts, i.e., the halting instruction is reached. In this case, neuron $\sigma_1$ in II receives 6 spikes. At that moment, neuron $\sigma_1$ contains 5n spikes, for the number $n \geq 1$ stored in register 1 of $M$. With 6 spikes inside, neuron $\sigma_1$ becomes active by using rule $a^4a^6 \rightarrow + (a^4, [1])$, creating a synapse to neuron $\sigma_r$, and sending 2 spikes to neuron $\sigma_r$. Neuron $\sigma_{i1}$ ends with one spike, and rule $a \rightarrow + (\lambda, [1])$ is used, removing the synapse to neuron $\sigma_{i1}$ one step later.

After neuron $\sigma_1$ receives the 2 spikes from neuron $\sigma_{i1}$, the number of spikes in neuron $\sigma_r$ becomes $5n + 2$ and rule $a^4(a^6)^n/a^6 \rightarrow + (\lambda, [0])$ is enabled and applied at step $t+2$. By using the rule, neuron $\sigma_r$ consumes one spike and creates a synapse to the environment. Neuron $\sigma_1$ contains $5n + 1$ spikes such that spiking rule $a^4(a^6)^n/a^6 \rightarrow a$ is used, consuming 5 spikes and emitting one spike to the environment at step $t+3$. Note that the number of spikes in neuron $\sigma_1$ becomes $5(n - 1) + 1$. So, if the number of spikes in neuron $\sigma_r$ is not one, then neuron $\sigma_r$ will fire again in the next step sending one spike into the environment. In this way, neuron $\sigma_r$ can fire for $n$ times, i.e., until the number of spikes in neuron $\sigma_1$ reaches one. For each time when neuron $\sigma_r$ fires, it sends one spike into the environment. So, in total, neuron $\sigma_r$ sends $n$ spikes into the environment, which is exactly the number stored in register 1 of $M$ at the moment when the computation of $M$ halts. When neuron $\sigma_r$ has one spike, rule $a \rightarrow + (\lambda, [0])$ is used to remove the synapse from neuron $\sigma_r$ to the environment, and system II eventually halts.

The dynamic transformation of topological structure of the FIN module and the numbers of spikes in the neurons of FIN module and in the environment are shown in Fig. 8.

Based on the description of the work of system II above, the register machine $M$ is correctly simulated by system II, i.e., $N(M) = N\rho_{II}(M)$. We can check that each neuron in system II has at most three rules, and no limit is imposed on the numbers of neurons and the synapses that can be created (or deleted) by using one synapse creation (or deletion) rule. Therefore, it concludes $N\rho_{SPSOall} = N\rho_{II} = NRE$.

This concludes the proof.

As number acceptor. Register machine can work in the accepting mode. Number $n$ is accepted by register machine $M'$ as follows. Initially, number $n$ is stored in the first register of $M'$ and all the other registers are empty. If the computation starting in this configuration eventually halts, then the number $n$ is said to be accepted by register machine $M'$. The set of numbers accepted by register machine $M'$ is denoted by $N_{acc}(M')$. It is known
that all the sets of numbers in NRE can be accepted by register machine \( M' \), even using the deterministic register machine; i.e. the machine with the ADD instructions of the form \( I; (ADD(r, l_j, l_k)) \) where \( l_j = l_k \) (in this case, the instruction is written in the form \( l_j; (ADD(r, l_j)) \)).

**Theorem 5.** N-SPSOₐ₊(cre-, del-, rule₂) = NRE.

**Proof.** It only has to prove \( NRE \subseteq N-SPSOₐ₊(cre-, del-, rule₂) \), since the converse inclusion is straightforward from the Turing-Church thesis. In what follows, an SN P system \( II' \) with self-organization working in accepting mode is constructed to simulate a deterministic register machine \( M' = (m, H, \lambda, l_0, I) \) working in the accepting mode. Actually, the proof is given by modifying the proof of Theorem 4.

Each register \( r \) of \( M' \) is associated with a neuron \( \sigma_r \) in system \( II' \), and for each instruction \( l_i \) of \( M' \) a neuron \( \sigma_{l_i} \) is associated. A number \( n \) stored in register \( r \) is represented by \( 5n \) spikes in neuron \( \sigma_r \).

The system \( II' \) consists of an INPUT module, deterministic ADD and SUB modules. The INPUT module is shown in Fig. 9, where all neurons are initially empty with the exception that input neuron \( \sigma_{l_0} \) sends 6 spikes to the two neurons. In neuron \( \sigma_{l_2} \), neuron \( \sigma_{l_1} \) is associated. A number \( n \) stored in register \( r \) is represented by \( 5n \) spikes in neuron \( \sigma_r \).

In the next step, neuron \( \sigma_{l_1} \) receives 5 spikes from neurons \( \sigma_{l_0} \) and \( \sigma_{l_2} \). Each of neurons \( \sigma_{l_1} \) and \( \sigma_{l_2} \) becomes active at step \( t + 2 \). Neuron \( \sigma_{l_2} \) uses rule \( a^3/l_a \rightarrow +l_0, \{I_0, I_1, 1\} \) to create a synapse to neuron \( \sigma_{l_0} \); and neuron \( \sigma_{l_1} \) creates a synapse from each of neurons \( \sigma_{l_0} \) and \( \sigma_{l_2} \). Each of neurons \( \sigma_{l_0} \) and \( \sigma_{l_2} \) has 5 spikes left. From step \( t + 3 \) on, neurons \( \sigma_{l_0} \) and \( \sigma_{l_2} \) fire and begin to exchange 5 spikes between them. In this way, neuron \( \sigma_{l_1} \) receives 5 spikes from neurons \( \sigma_{l_0} \) and \( \sigma_{l_2} \) at each step.

At step \( t + n \), neuron \( \sigma_{l_0} \) receives the second spike from the environment, accumulating 4 spikes inside. At step \( t + n + 1 \), neuron \( \sigma_{l_2} \) fires for the second time by using spiking rule \( a^3/l_a \rightarrow a^5 \), sending 3 spikes to neurons \( \sigma_{l_1} \) and \( \sigma_{l_2} \). Each of neurons \( \sigma_{l_1} \) and \( \sigma_{l_2} \) accumulates 8 spikes. At step \( t + n + 2 \), neuron \( \sigma_{l_0} \) uses synapse creation rule \( a^3/l_a \rightarrow +l_0, \{I_0, I_1, 1\} \), creating a synapse to neuron \( \sigma_{l_0} \) and sending 6 spikes to neuron \( \sigma_{l_1} \). This means that system \( II' \) starts to simulate the initial instruction \( l_0 \) of register machine \( M' \). Meanwhile, neuron \( \sigma_{l_1} \) uses synapse deletion rule \( a^3/l_a \rightarrow -l_0, \{I_0, I_1, 1\} \), removing the synapse from neuron \( \sigma_{l_0} \) to neuron \( \sigma_{l_1} \). In the next step, neuron \( \sigma_{l_1} \) creates a synapse from neuron \( \sigma_{l_0} \) to neuron \( \sigma_{l_1} \) and sends 5 spikes to neuron \( \sigma_{l_1} \) by using rule \( a^7 \rightarrow +a^5, \{1\} \).
From step $t + 3$ to $t + n + 1$, neuron $\sigma_1$ receives 5 spikes in each step from neuron $\sigma_{I_2}$, thus in total accumulating $5(n - 1)$ spikes. Neuron $\sigma_1$ receives no spike at step $t + n + 2$, and gets 5 spikes from neuron $\sigma_{I_2}$ at step $t + n + 3$. After that, no more spikes are sent to neuron $\sigma_{I_2}$. Neuron $\sigma_1$ contains $5n$ spikes, which indicates the number to be accepted by register machine $M'$ is $n$. At step $t + n + 4$, neuron $\sigma_{I_2}$ uses rule $a^5 \rightarrow -(\lambda, [1])$, deleting the synapse to neuron $\sigma_1$.

The dynamic transformation of topological structure of INPUT module and the numbers of spikes in the neurons of INPUT module are shown in Fig. 10.

The deterministic ADD module is shown in Fig. 11, whose function is rather clear. By receiving 6 spikes, neuron $\sigma_{I_2}$ becomes active, creating a synapse and sending 5 spikes to each of neurons $\sigma_{r_1}$, $\sigma_{r_2}(1)$ and $\sigma_{r_2}(2)$. The number of spikes in neuron $\sigma_{r_1}$ is increased by 5, which simulates the number stored in register 1 is increased by one. In the next step, neuron $\sigma_{I_2}$ uses rule $a \rightarrow (\lambda, \{1\})$, removing the synapses from neuron $\sigma_1$ to neurons $\sigma_{r_1}$, $\sigma_{r_2}(1)$ and $\sigma_{r_2}(2)$. In neurons $\sigma_{r_2}(1)$ and $\sigma_{r_2}(2)$, there are 5 spikes. The two neurons become active by using rule $a^5, a^5 \rightarrow +(\lambda, [1])$. Each of them creates a synapse to neuron $\sigma_{l_j}$ and emits 3 spikes to neuron $\sigma_{l_j}$. In this way, neuron $\sigma_{l_j}$ accumulates 6 spikes inside, which means the system $\Pi'$ goes to simulate instruction $l_j$ of $M'$. The synapses from neuron $\sigma_{r_2}(1)$ and $\sigma_{r_2}(2)$ to neuron $\sigma_{l_j}$ will be removed by using synapse deletion rule $a \rightarrow -(\lambda, [1])$ in neurons $\sigma_{r_2}(1)$ and $\sigma_{r_2}(2)$.

Module SUB remains unchanged, as shown in Fig. 4. Module FIN is removed, with neuron $\sigma_{l_h}$ remaining in the system, but having no rule inside. When neuron $\sigma_{l_h}$ receives 6 spikes, it means that the computation of register machine $M'$ reaches instruction $l_h$ and stops. Having 6 spikes inside, neuron $\sigma_{l_h}$ cannot become active for no rule can be used. In this way, the work of system $\Pi'$ halts.

Figure 6. The dynamic transformation of topological structure and the numbers of spikes in involved neurons in the SUB instruction simulation with neuron $\sigma_{l_k}$ finally activated.

Figure 7. Outputting the computation result.
Based on the description of the implementation of system $\Pi'$ above, it is clear that the register machine $M'$ in acceptive mode is correctly simulated by the system $\Pi'$ working in acceptive mode, i.e., $N_{acc}(M') = N_{acc}(\Pi')$.

We can check that each neuron in system $\Pi'$ has at most five rules, and no limit is imposed on the numbers of neurons and the synapses that can be created (or deleted) with using one synapse creation (or deletion) rule. Therefore, it concludes $N_{*SPSO_{acc}}(cre^*, del^*, rule^5) = N_{RE}$.

As function computing device. A register machine $M$ can compute a function $f : \mathbb{N}^k \rightarrow \mathbb{N}$ as follows: the arguments are introduced in special registers $r_1, r_2, \ldots, r_k$ (without loss of the generality, it is assumed that the first $k$ registers are used). The computation starts with the initial instruction $l_0$. If the register machine halts, i.e., reaches HALT instruction $l_h$, the value of the function is placed in another specified register, labelled by $r_t$, with all registers different from $r_t$ storing number 0. The partial function computed by a register machine $M$ in this way is denoted by $M(n_1, n_2, \ldots, n_k)$. All Turing computable functions can be computed by register machine in this way.

Several universal register machines for computing functions were defined. Let $(\varphi_0, \varphi_1, \ldots)$ be a fixed admissible enumeration of the unary partial recursive functions. A register machine $M_u$ is said to be universal if there is a recursive function $g$ such that for all natural numbers $x$ and $y$ we have $\varphi_x(y) = M_u(g(x), y)$. As addressed by Minsky, universal register machine can compute any $\varphi_x(y)$ by inputting a couple of numbers $g(x)$ and $y$ in registers 1 and 2, and the result can be obtained in register $0^{'\text{th}}$.

In the following proof of universality, a specific universal register machine $M_u$ from\(^47\) is used, the machine $M_u = (8, H, l_0, l_1, I)$ presented in Fig. 12. In this universal register machine $M_u$, there are 8 registers (numbered from 0 to 7) and 23 instructions, and the last instruction is the halting one. As described above, the input numbers
(the "code" of the partial recursive function to compute and the argument for this function) are introduced in registers 1 and 2, and the result is outputted in register 0 when the machine $M_u$ halts.

A modification is necessary to be made in $M_u$, because the subtraction operation in the register where the result is placed is not allowed in the construction of the previous Theorems, but register 0 of $M_u$ is subject of such operations. That is why an extra register is needed - labeled with 8 - and the halt instruction $l_h$ of $M_u$ should be replaced by the following instructions:

$$l_{22} : \text{SUB}(0), \ l_{23} : \text{ADD}(8), \ l'_h : \text{HALT}.$$  

Therefore, the modified universal register machine $M'_u$ has 9 registers, 24 ADD and SUB instructions, and 25 labels. The result of a computation of $M'_u$ is stored in register 8.

**Theorem 6** There is a universal SN P system with self-organization having 87 neurons for computing functions.

**Proof.** An SN P system with self-organization $\Pi''$ is constructed to simulate the computation of the universal register machine $M'_u$. Specifically, the system $\Pi''$ consists of deterministic ADD modules, SUB modules, as well as

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**Figure 10.** The dynamic transformation of topological structure of INPUT module and the numbers of spikes in the neurons of INPUT module.
an INPUT module and an OUTPUT module. The deterministic ADD module shown in Fig. 11 and SUB module shown in Fig. 4 can be used here to simulate the deterministic ADD instruction and SUB instruction of $\text{Mu}$. The INPUT module introduces the necessary spikes into the system by reading a spike train from the environment, and the OUTPUT module outputs the computation result.

With each register $r$ of $\text{Mu}$, a neuron $\sigma_r$ in system $\Pi''$ is associated; the number stored in register $r$ is encoded by the number of spikes in neuron $\sigma_r$. If register $r$ holds the number $n \geq 0$, then neuron $\sigma_r$ contains $5n$ spikes. With each instruction $l_i$ in $\text{Mu}$, a neuron $\sigma_{l_i}$ in system $\Pi''$ is associated. If neuron $\sigma_{l_i}$ has 6 spikes inside, it becomes active and starts to simulate the instruction $l_i$. When neuron $\sigma_{l_h}$ (associated with the label $l_h$ of the halting instruction of $\text{Mu}$) receives 6 spikes, the computation in $\text{Mu}$ is completely simulated by the system $\Pi''$; the number of spikes emitted into the environment from the output neuron, i.e., neuron $\sigma_8$, corresponds to the result computed by $\text{Mu}$ (stored in register 8).

The tasks of loading $5g(x)$ spikes in neuron $\sigma_1$ and $5y$ spikes in neuron $\sigma_1$ by reading the spike train $10^{6g(x)-1}10^{y-1}$ through input neuron $\sigma_m$ can be carried out by the INPUT module shown in Fig. 13. Initially, all the neurons contain no spike inside, with the exception that neuron $\sigma_1$ has 15 spikes. It is assumed at step $t$ neuron $\sigma_m$ reads the first spike from the environment. With 16 spikes inside, neuron $\sigma_{l_1}$ becomes active by using rule $a^{16}/a^{16} \rightarrow +(a^4, \{l_4, l_5\})$ at step $t + 1$. It creates a synapse and sends 6 spikes to each of neurons $\sigma_{l_4}$ and $\sigma_{l_5}$. Subsequently, neuron $\sigma_{l_1}$ keeps inactive (for no rule can be used) until the second spike arrives at step $t + g(x)$.

Figure 11. The deterministic ADD module of system $\Pi'$.  

Figure 12. The universal register machine $\text{Mu}$ from $\text{To}$.
Neuron $\sigma_i$ has 6 spikes and uses rule $a^6/a \rightarrow +\lambda(\{I_2,1\})$ at step $t+2$ it creates a synapse to neurons $\sigma_{I_2}$ and $\sigma_1$ and sends 5 spikes to each of the two neurons. Meanwhile, neuron $\sigma_{I_2}$ creates a synapse to neuron $\sigma_{I_1}$ and sends 5 spikes to it. From step $t+3$ on, neuron $\sigma_{I_1}$ sends 5 spikes to neuron $\sigma_{I_2}$ and exchanges 5 spikes with neuron $\sigma_{I_2}$ in each step.

At step $t+g(x)$, neuron $\sigma_{I_0}$ receives the second spike from the environment. By then it accumulates 11 spikes inside. At step $t+g(x)+1$, neuron $\sigma_{I_0}$ fires by using spiking rule $a^{11}/a^2 \rightarrow a^3$, and sends 3 spikes to neurons $\sigma_{I_1}$ and $\sigma_{I_2}$. Each of neurons $\sigma_{I_1}$ and $\sigma_{I_2}$ contains 8 spike, which will be remained in $\sigma_{I_0}$.

At step $t+g(x)+2$, neuron $\sigma_{I_1}$ applies synapse deletion rule $a^7/a \rightarrow -\lambda(\{I_1\})$ and removes the synapse to neuron $\sigma_{I_0}$. Meanwhile neuron $\sigma_{I_0}$ removes the synapse to neuron $\sigma_{I_1}$. The two neurons stop to exchange spikes with each other. At step $t+g(x)+3$, neuron $\sigma_{I_1}$ has 7 spikes and fires by using spiking rule $a^7/a^2 \rightarrow a^3$, and sends 5 spikes to neuron $\sigma_{I_2}$. In the next step, neuron $\sigma_{I_1}$ removes the synapse to neuron $\sigma_{I_2}$, and cannot send spikes to neuron $\sigma_{I_2}$.

In general, in each step from step $t+3$ to $t+g(x)+1$, neuron $\sigma_i$ receives 5 spikes from neuron $\sigma_{I_1}$, in total receiving $5(g(x)-1)$ spikes; at step $t+g(x)+2$, no spike arriving in neuron $\sigma_{I_0}$, and at step $t+g(x)+3$, 5 spikes reaching neuron $\sigma_{I_1}$. In this way, neuron $\sigma_{I_1}$ accumulates $5g(x)$ spikes, which simulates number $g(x)$ is stored in register 1 of $M'_\mu$.

At step $t+g(x)+2$, neuron $\sigma_{I_2}$ contains 8 spikes such that rule $a^8/a^2 \rightarrow +\lambda(\{I_2,1\})$ is used, creating a synapse and sends 6 spikes to each of neurons $\sigma_{I_2}$ and $\sigma_{I_1}$. At step $t+g(x)+3$, neurons $\sigma_{I_2}$ and $\sigma_{I_1}$ create synapses to each other, meanwhile neuron $\sigma_{I_2}$ creates a synapse to neuron $\sigma_{I_1}$. From step $t+g(x)+4$ on, neuron $\sigma_{I_2}$ begins to exchange 5 spikes with $\sigma_{I_1}$ and send 5 spikes to neuron $\sigma_{I_2}$ in each step. At step $t+g(x)+y$, neuron $\sigma_{I_2}$ receives the third spike from the environment, accumulating 3 spikes inside. One step later, it fires by using spiking rule $a^7/a^2 \rightarrow a^3$, sending 2 spikes to neurons $\sigma_{I_1}, \sigma_{I_2}, \sigma_{I_1}$, and $\sigma_{I_1}$. With 2 spikes inside, neuron $\sigma_{I_1}$ removes its synapse to neuron $\sigma_{I_2}$ by rule $a^2 \rightarrow -\lambda(\{1\})$; while neuron $\sigma_{I_2}$ forgets the two spikes by forgetting rule $a^2 \rightarrow a^3$. By receiving 2 spikes from neuron $\sigma_{I_0}$, neurons $\sigma_{I_1}$ and $\sigma_{I_2}$ contain 7 spikes. At step $t+g(x)+y+2$, neuron $\sigma_{I_2}$ fires by using rule $a^7/a^3 \rightarrow a^3$ and sends 3 spikes to neurons $\sigma_{I_2}$ and $\sigma_{I_1}$. The number of spikes in neuron $\sigma_{I_1}$ is $5(y-1)+3$. Neuron $\sigma_{I_1}$ consumes 6 spikes, creates a synapse and sends 6 spikes to neuron $\sigma_{I_1}$. This means system $\Pi^\ast$ starts to simulate the initial instruction $l_0$ of $M'_\mu$.

At step $t+g(x)+y+3$, neuron $\sigma_{I_1}$ has 4 spikes, and it becomes active by rule $a^4/a \rightarrow -\lambda(\{I_1\})$, and removes its synapse to neuron $\sigma_{I_2}$ and ends with 3 spikes. In the next step, neuron $\sigma_{I_2}$ fires by using spiking rule $a^4/a^2 \rightarrow a^2$, emitting 2 spikes to neuron $\sigma_2$. In this way, the number of spikes in neuron $\sigma_2$ becomes $5(y-1)+3+2=5y$, which indicates number $y$ is stored in register 2 of $M'_\mu$.

The deterministic ADD module shown in Fig. 11 and SUB module shown in Fig. 4 can be used to simulate ADD and SUB instructions of $M'_\mu$. The FIN module shown in Fig. 7 can be used to output the computation result with changing neuron $\sigma_i$ into $\sigma_e$.

Until now, we have used

- 9 neurons for 9 registers,
- 25 neurons for 25 labels,
- 20 neurons for 10 ADD instructions,
- 28 neurons for 14 SUB instruction,
- 5 additional neurons in the INPUT module,

![Diagram](image_url)
which comes to a total of 87 neurons. This concludes the proof.

Discussion and Future Works

In this work, a novel variant of SN P systems, namely SN P systems with self-organization, is introduced. As results, it is proven that the systems are Turing universal, i.e., they can compute and accept the family of sets of Turing computable natural numbers. With 87 neurons, the system can compute any Turing computable recursive function, thus achieving Turing universality.

There has been a research focus on the construction of small universal SN P with less computing resource, i.e. less number of neuron in usc.17.48–52. It is of interest that whether we can reduce the number of neurons in universal SN P systems with self-organization as function computing devices. A possible way is to construct ADD-ADD, ADD-SUB and SUB-ADD modules to perform particular consecutive ADD-ADD, ADD-SUB, and SUB-ADD instructions of $M'$.

SN P systems with learning function/capability is a promising direction. Learning strategies and feedback mechanism have been intensively studied and investigated in conventional artificial neural networks. It is worthy to look into these techniques and transplant these ideas into SN P systems with self-organization.

In research of using artificial neural networks to recognize digital English letters, database MNIST (Mixed National Institute of Standards and Technology database) is widely used for training various letter recognition systems,13 and for training and testing in the field of machine learning.14 For further research, SN P systems with self-organization may be used to recognize handwritten digits letters and other possible pattern recognition problems. Since the data structure of SN P systems is binary sequences, an extra task of transmitting letters or pictures into binary sequences should be addressed. A possible way is transmitting digital numbers of pixels of pictures to binary form. Also, local binary pattern method, can be used to transmit pictures to binary forms.

Bioinformatics is an interdisciplinary field that develops methods and software tools for understanding biological data.53 Artificial intelligence based methods and data mining strategy have been used in processing biological data, see e.g.56–62, it is worthy to processing biological data by SN P systems, such as DNA motif finding,63,64 nuclear export signal identification,65,66.

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