Design of a Continuous-Time Loop Filter for \( \Delta \Sigma \) Modulators with Excess Loop Delay

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Abstract

In this paper, we propose a continuous-time (CT) loop filter for minimizing the quantization noise in a Delta-Sigma (\( \Delta \Sigma \)) modulator. We use the impulse-invariant transformation to obtain a CT loop filter from a discrete-time (DT) loop filter. We consider a non-ideal CT \( \Delta \Sigma \) modulator which is affected by the excess loop delay (ELD). The ELD is known to affect the stability and noise shaping performance of the CT \( \Delta \Sigma \) modulator. Our objective is to design the CT modulator whose stability is not affected by the presence of ELD. A design example for a lowpass CT \( \Delta \Sigma \) modulator based radio frequency (RF) receiver is provided for simulations. We also compare the mean squared error (MSE) performance of our modulator with the conventional design.

1 Introduction

The popularity of digital wireless communication applications is causing an increase in the demand for high performance analog-to-digital converters (ADCs). Many engineers and researchers consider Delta-Sigma (\( \Delta \Sigma \)) modulators as their first choice for ADCs to be used in circuit designs. As compared to other analog-to-digital conversion techniques, \( \Delta \Sigma \) ADCs cover the widest conversion region of the resolution-versus-bandwidth plane [1], providing the most efficient solution to digitize diverse types of signals in various signal processing applications [2, 3].

The majority of \( \Delta \Sigma \) modulators in the ADC literature are implemented as discrete-time (DT) circuits such as switched current or switched capacitor [4, 5]. However, there is an increasing interest in designing \( \Delta \Sigma \) modulators using continuous-time (CT) circuitry, because it is generally possible to clock CT \( \Delta \Sigma \) modulators at much higher frequencies as compared to DT \( \Delta \Sigma \) modulators [6]. The maximum clock rate of a typical DT \( \Delta \Sigma \) modulator is limited both by operational amplifier bandwidths and by the fact that the switch capacitor circuit need several time constants to settle down. By contrast, the restriction on operational amplifier bandwidths are relaxed in a CT \( \Delta \Sigma \) modulator because the waveforms vary continuously. Therefore, a CT \( \Delta \Sigma \) modulator can be clocked with a much higher frequency without any significant effect on its performance. Then, for a given oversampling ratio (OSR), the conversion bandwidth of a CT \( \Delta \Sigma \) modulator is greatly increased. In DT domain, aliasing is another issue which is caused by signals at multiple of the sampling frequency that are indistinguishable. Due to this, a separate anti-aliasing filter is required at the input of the DT \( \Delta \Sigma \) modulator to attenuate aliases. On the other hand, anti-aliasing is an inherent property of CT \( \Delta \Sigma \) modulator [9].

The input of the CT \( \Delta \Sigma \) modulator is an analog signal which is sampled and then quantized by using a non-linear quantizer. The non-linear quantizer is usually approximated as a linear device with an added white noise in the digital output. The CT \( \Delta \Sigma \) modulator uses a CT loop filter to reduce the noise due to quantization by pushing the noise away from the desired frequency region [10]. Therefore, the design of a CT loop filter is an important aspect of a \( \Delta \Sigma \) modulator for minimizing the quantization noise.

For high-speed CT designs, it is known that the performance can be affected by several factors such as thermal noise in the input stage, quantizer clock jitter, and quantizer metastability [6]. All of these factors can limit the performance of a CT \( \Delta \Sigma \) modulator. Excess loop delay (ELD) is yet another problem which is being studied by many researchers since it affects the resolution of the CT modulators [7, 8].

In this paper, our objective is to design a CT loop filter for minimizing the quantization noise in a \( \Delta \Sigma \) modulator. We use impulse-invariant transformation to obtain the CT loop filter from the DT loop filter. We consider the non-ideal behavior of the CT modulator in the presence of the ELD, and hence, ensuring the stability of the non-ideal CT \( \Delta \Sigma \) modulator. We also compare the mean squared error (MSE) performance of our proposed CT loop filter with the Schreier’s CT loop filter [10].

2 Continuous-Time \( \Delta \Sigma \) Modulator

A basic single-loop model of a CT \( \Delta \Sigma \) modulator is shown in Fig 1. It consists of three main elements: a quantizer, a loop filter and a digital-to-analog converter
The quantizer performs sampling and quantization to the analog output of the loop filter to obtain a digital signal with added quantization error $e(t)$. The loop filter provides gain for the modulator in such a way that it attenuates the quantization noise which lies in the desired frequency region. The loop filter consists of ideal integrators whose order determines the magnitude of the attenuation level. The element in the feedback of the CT ΔΣ modulator is known as DAC, which converts the digital output of the quantizer into an analog signal. The analog output waveform of the DAC can have different shapes depending on the implementation requirements. The two most common functions used in DAC for generating the output waveforms are non-return-to-zero (NRZ) and return-to-zero (RZ). A NRZ DAC holds the value of the digital signal for one sampling period, whereas a RZ DAC uses only a fraction of the sampling period.

The ΔΣ modulator in Fig. 1 is a non-linear feedback system which can be approximated by its linear model as depicted in Fig. 2. In the linear model, the quantizer is modeled as an error source which has white noise spectrum. The DAC is modeled as a unity gain stage. The two most common functions used in DAC for generating the output waveforms are non-return-to-zero (NRZ) and return-to-zero (RZ). A NRZ DAC holds the value of the digital signal for one sampling period, whereas a RZ DAC uses only a fraction of the sampling period.

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$$Y[s] = \frac{H[s]}{1 + H[s]} \cdot X[s] + \frac{1}{1 + H[s]} \cdot E[s],$$

where $X[s]$ and $E[s]$ are Laplace transforms of the CT input signal $x(t)$ and the error due to quantization $e(t)$, respectively. The Laplace transform of a function $f(t)$ is defined as the function $F(s) = \int_0^\infty f(t)e^{-st}dt$.

The transfer function $H[s]$ represents the gain of the loop filter. The input $X[s]$ and the error $E[s]$ are subject to different transfer functions, which are known as the signal transfer function (STF) and the noise transfer function (NTF), respectively.

Often, a non-ideal filter is utilized at the output of the ΔΣ modulator to recover the information. The non-ideal filter may cause some of the quantization noise to leak into the information signal band [11]. Therefore, we would like to minimize the quantization noise at the output of this filter. Then, the signal $y[n]$ at the output of the non-ideal filter $P[s]$ can be expressed as

$$Y[s] = P[s]STF[s]X[s] + P[s]NTF[s]E[s].$$

From (2), the expression for the quantization noise in $Y[s]$ can be expressed as

$$E[s] = P[s]NTF[s]E[s].$$

Our objective is to minimize the quantization noise $E[s]$ by obtaining the loop filter $H[s]$ such that the $NTF[s]$ suppresses the quantization noise present in the information signal band. For a lowpass ΔΣ modulator, the $NTF[s]$ will act as a high pass filter, which will shape the quantization noise away from the low frequency region.

To design a CT loop filter for minimizing the quantization noise in a ΔΣ modulator, we first design a DT loop filter which meets the performance specifications, and then transform it using the impulse-invariant transformation to the equivalent CT loop filter.

### 2.1 Impulse-Invariant Transformation

Here, we will explain about the impulse-invariant transformation [9] and how it can be used in obtaining a CT loop filter from a DT loop filter.

Suppose we have two modulators in Fig. 3 and Fig. 4 to which we apply the same input waveform. If we simulate each modulator in the time domain, and we find they both produce the same sequence of output
bits, then they are likely to be equivalent modulators. We can guarantee they will produce the same output bit sequence if we ensure that the inputs to their quantizers are the same at sampling instants. At a given instant, each quantizer would then make the same decision about what output bit to produce, and thus the same bits would be combined with the (identical) input to produce the same quantizer input voltage at the next sampling instant. Therefore, we can see that two modulators are equivalent if, for the same input waveform, their quantizer input voltages at sampling instants are equal.

To see how to make use of this in CT modulator design, we take the CT $\Delta \Sigma$ modulator at the top of Fig. 3. Rather than making the sampler implicitly inside the quantizer, we have chosen to make it explicit prior to the quantizer, this does not change modulator behavior. In the bottom part of Fig. 3, we have both opened the loop around the quantizer and zeroed the modulator input. When we do the same thing to a DT $\Delta \Sigma$ modulator in Fig. 4, we have two open-loop diagrams (a CT one and a DT one) to compare.

The input to the CT open-loop diagram is the output bit $y[n]$. This is a DT quantity, it only ever changes at sampling instants. The DAC may be thought of as a discrete-to-continuous converter: it takes a sample $y[n]$ and produces some kind of continuous pulse $y(t)$. This pulse is filtered by the loop filter $H[s]$, then sampled, where it becomes the DT output of the open-loop system $u[n]$ (as well as being the input to the quantizer). In the DT open-loop diagram, the signals never leave the DT domain.

Note that for both CT and DT loops, the input and output of the open-loop diagrams are both DT quantities. We just said that two $\Delta \Sigma$ modulators are equivalent when their quantizer inputs are the same at sampling instants. This would be satisfied if the impulse responses of the open-loop diagrams in Fig. 3 and Fig. 4 were equal at sampling times. Then, it leads to the condition

$$Z^{-1}\{H[z]\} = L^{-1}\{R_D[s]H[s]\}|_{t=nT_s},$$

where $Z^{-1}$ and $L^{-1}$ are inverse $z$-transform and inverse Laplace transform functions, respectively, use to obtain time-domain equivalent as

$$h(n) = [r_D(t) * h(t)]|_{t=nT_s},$$

where $r_D(t)$ is the impulse response of the DAC. This transformation between CT and DT is called the impulse-invariant transformation, because we require the open loop impulse responses to be equal at similar sampling instants. Without loss of generality, we assume the sampling period to $T_s = 1$ for simplicity.

Suppose we obtain a DT loop filter $H[z]$ that gives us particular noise shaping behavior. Then, we can design a CT loop filter $H[s]$ with identical noise shaping behavior by choosing a DAC pulse shape $r_D(t)$, and then using either (4) or (5) to find $H[s]$.

To obtain $H[s]$, we utilize Table 2.1 in [9] which was obtained by solving (4) in the symbolic math program Maple [12].

2.2 Stability of the $\Delta \Sigma$ Modulator
The stability of a CT $\Delta \Sigma$ modulator is greatly affected by the ELD, which is defined as the time delay between the quantizer clock edge and the time when a change in the output of the DAC occurs. ELD is basically caused by the limited speed of the transistors used to implement the quantizer and DAC of a CT $\Delta \Sigma$ modulator. If the time delay shifts the DAC pulse into the next clock cycle, the order of the actual modulator also increases which reduces the modulator stability and it may also affect its’ noise shaping performance [1]. The ELD can be expressed by

$$\tau_d = \rho_0 T_s.$$  

where $\tau_d$ depends on the switching speed of transistors, the quantizer clock frequency, and the number of transistors in the feedback path, as well as the loading on each transistor.

In our proposed CT $\Delta \Sigma$ modulator, the stability of the modulator affected by the ELD is ensured by limiting the maximum out-of-band gain of the $NTF[s]$ which can overload the quantizer. The Lee criterion [13] is often utilized for limiting the maximum magnitude of the frequency response of the $NTF[s]$ such that

$$||NTF[s]||_\infty < \gamma.$$  

For binary quantizers, the value of $\gamma$ is usually set as 1.5 which is equivalent to 3.52 dB.

2.3 Proposed Method
Here, we will summarize our proposed method to obtain a CT loop filter for minimization of the quantization noise $\mathcal{E}[s]$. 

![Fig. 4: Loop filter representation for D.T modulators.](image)
First, we obtain a DT loop filter $H[z]$ by minimizing the quantization noise subject to Lee criterion. The methods proposed in [4, 5, 11] can be used to obtain $H[z]$.

Then, we use the impulse-invariant transformation method to obtain the CT equivalent loop filter $H[s]$ from $H[z]$ by using the equivalence Table 2.1 provided in [9]. The transformations in the Table 2.1 can also be performed by using Matlab.

We derive the NTF $s$ from the $H[s]$, and plot its frequency response for different values of the ELD which show the increase in the out-of-band gain.

The out-of-band gain of the NTF, which may cause the the non-ideal CT ΔΣ modulator to become unstable, will be controlled by reducing the Lee coefficient value. That is, we obtain DT $H[z]$ with a lower value of the out-of-band gain or lower value of the Lee coefficient in the first step. The higher the value of ELD, the lower should be the value of the Lee coefficient.

In the next section, we perform simulations to show the behavior of the non-ideal ΔΣ modulator in the presence of the ELD.

### 3 Simulation Results

CT ΔΣ modulators are proving to be a competitive solution for the implementation of power-efficient ADCs operating in high speed and wide bandwidth applications [3]. In addition to digitizing the incoming signals, CT ΔΣ modulators take advantage of their circuit nature to merge some RF functionalities like out-of-band blocker/interfering-rejection filtering, frequency-mixing process, channel-selection and anti-aliasing filtering [6]. All these functionalities can be embedded within the ΔΣ modulator feedback loop, thus resulting in more compact RF receivers.

A basic wireless receiver consists of a radio frequency (RF) front end, an ADC and a digital baseband processor as illustrated in Fig. 5. The RF front end is used to filter and amplify the received RF signals at the input, and then down convert them to the baseband level.

![Fig. 5: A basic block diagram of a wireless receiver.](image)

The role of the ADC is to sample and quantize the input analog signals and output the digital signals to the baseband processor.

Let us consider a lowpass CT ΔΣ modulator being utilized as an ADC in the RF receiver. Our objective is to minimize the quantization noise in the RF receiver by synthesizing a CT loop filter which reduces the quantization noise in the low frequency region. The input signal to the quantizer is oversampled with an $OSR = 32$.

To obtain CT loop filter $H[s]$, we first design DT ΔΣ modulator loop filter that will meet a given resolution requirement by using the method proposed in [5]. We use the Lee coefficient $\gamma = 1.5$ which limit the maximum out-of-band gain to 3.52 dB for the NTF with no ELD. Then, we transform it to the equivalent CT loop filter by using the impulse-invariant transformation. The Matlab built-in function $d2cm$ is used to perform these transformations for the NRZ DAC pulse case.

We also compare the proposed CT loop filter with the Scherier’s CT loop filter design which is obtained by using the $synthesizeNTF$ function in ΔΣ toolbox [14]. The $synthesizeNTF$ function will give us DT loop filter which is also transformed to CT loop filter using the impulse-invariant transformation.

For the proposed design, the second order $H[z]$ obtained from [5] is given by:

$$H[z] = \frac{0.7103z - 0.4812}{z^2 - 1.857z + 0.8657}$$  \hspace{1cm} (8)

The CT loop filter that yields the desired $H[s]$ for NRZ DAC with no excess delay is computed to be

![Fig. 6: Frequency spectrum of the proposed NTF for different values of the ELD. The dotted line represents the output filter frequency response, while the solid lines represents the NTFs for different values of the ELD.](image)
\[ H[s] = \frac{0.6378s - 0.2462}{s^2 + 0.1442s + 0.009214} \]  \hspace{1cm} (9)

To look at the effect of varying ELD on the stability of the CT ΔΣ modulator, the magnitude response of the proposed NTF for the CT ΔΣ modulator is shown in Fig. 6. It is observed that the higher values of the ELD results in the higher out-of-band gain, which increases the chances of overloading the quantizer. As mentioned before, the Lee coefficient can be utilized to limit the maximum magnitude of the NTF to ensure the stability of modulator. Therefore, the out-of-band gain is reduced by decreasing the value of the Lee coefficient. In Fig. 6, the ELD \( \tau_D = 1 \) gives the maximum out-of-band gain which is equivalent to 16.6 dB. To make it below 3.52 dB for binary quantizers, the Lee coefficient is further reduced to \( \gamma = 1.15 \) dB. However, it is observed that by reducing the value of the Lee coefficient, the modulator becomes more stable at the expense of reduction in the attenuation level of the quantization noise. Hence, there is a trade-off between the modulator stability and the quantization noise reduction level.

The effect of ELD on the NTF poles is illustrated in Fig. 7 for the proposed design and the \( \text{synthesizeNTF} \) design. As the ELD is varied from minimum to maximum values, the poles move toward unit circle with the increasing ELD. The poles of the \( \text{synthesizeNTF} \) are closer to the unit circle boundary than our proposed design, making our design more robust than the \( \text{synthesizeNTF} \) design. Nevertheless, the NTF zeros remain on the unit circle. This is in accordance to the usually seen low influence of ELD on the noise shaping behavior up to a certain amount of ELD.

Fig. 8 shows the MSE values of the quantization noise (3) for the proposed design and the \( \text{synthesizeNTF} \) design. The MSE value is noted for the increasing values of the ELD. We notice that the proposed design performs better than the \( \text{synthesizeNTF} \) design in terms of the MSE performance in the presence of the ELD. The proposed design gives better MSE values because it takes into account the non-ideal output filter \( P[s] \) for the minimization of the quantization noise, while the \( \text{synthesizeNTF} \) does not consider \( P[s] \).

## 4 Conclusions

To minimize the quantization noise in ADC, we obtained a CT loop filter for the ΔΣ modulator. The design procedure requires us to obtain the DT loop filter which is then transformed to the CT loop filter using the impulse-invariant transformation. It is observed that the presence of the ELD affects the stability of the CT ΔΣ modulator. With the increasing ELD, the modulator poles gets close to the boundary of the unit circle, and the NTF out-of-band gain increases as well. The Lee coefficient is utilized to ensure the stability of our modulator at the expense of the noise shaping performance. However, our proposed design gives better noise shaping performance in terms of the MSE as compared to the \( \text{synthesizeNTF} \) design.

## References

[1] M. Ortmanns and F. Gerfers, "Continuous-Time Sigma-Delta A/D Conversion", Springer series in advanced microelectronics, 2006.

[2] LM4670 Filterless High Efficiency 3W Switching Audio Amplifier, Texas Instruments, TI Literature Number SNAS240B, Jun. 2006.

[3] M. M. Ebrahimi, M. Helaoui and F. M. Ghanouchi, "Delta-Sigma-Based Transmitters", IEEE Microwave Magazine, vol. 13, pp. 68-78, 2013.
[4] M. R. Tariq and S. Ohno, "Unified LMI Based Design of $\Delta \Sigma$ Modulators", EURASIP Journal of Advances in Signal Processing, Feb. 2016.

[5] S. Ohno and M. R. Tariq, "Optimization of Noise Shaping Filter for Quantizer with Error Feedback", IEEE Transactions on Circuits and systems I: Regular Papers.

[6] M. Bolatkale, L.J. Breems and K.A.A. Makinwa, "High-Speed and Wide Bandwidth Delta-Sigma ADCs", Springer, 2014.

[7] S. Pavan, "Continuous-Time Delta-Sigma Modulator Design using the Method of Moments", IEEE Transaction on Circuits and Systems-I: Regular Papers, vol. 61, no.6, Jun. 2014.

[8] S. Pavan, "Excess Loop Delay Compensation in Continuous-Time Delta-Sigma Modulators", IEEE Transaction on Circuits and Systems-II: Express Briefs, vol. 55, no.11, Nov. 2008.

[9] J.A. Cherry and W.M. Snelgrove, "Continuous-Time Delta-Sigma Modulators for High-Speed A/D Conversion", Kluver Academic Publishers, 2002.

[10] R. Schreier and G. C. Temes, "Understanding Delta-Sigma Data Converters", Wiley-IEEE Press, 2004.

[11] S. Callegari and F. Bizzari, "Output Filter Aware Optimization of the Noise Shaping Properties of Modulators Via Semi-Definite Programming", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 60, no. 9, pp. 2352-2365-318, Sept. 2013. 1997.

[12] D. Redfern, "The Maple Handbook", Springer-Verlag, New York, 1994.

[13] K.C.H. Chao, S. Nadeem, W.L. Lee and C.G. Sodini, "A Higher Order Topology for Interpolative Modulators for Oversampling A/D Converters", IEEE Transactions on Circuits Systems, vol. 37, no. 3, pp. 309-318, Mar. 1997.

[14] R. Schreier, Delta Sigma Toolbox [Online]. Available: http://www.mathworks.com/Matlabcentral/fileexchange