Selective Lateral Germanium Growth for Local GeOI Fabrication

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High quality local Germanium-on-oxide (GeOI) wafers are fabricated using selective lateral germanium (Ge) growth technique by a single wafer reduced pressure chemical vapor deposition system. Mesa structures of 300 nm thick epitaxial silicon (Si) interposed by SiO2 cap and buried oxide are prepared. H2/Ge vapor phase etching of Si is performed prior to selective Ge growth to remove a part of the epitaxial Si to form cavity under the mesa. By following selective Ge growth, the cavity was filled. Cross section TEM shows dislocations of Ge which are located near Si / Ge interface only. By plan view TEM, it is shown that the dislocations in Ge which direct to SiO2 cap or to buried-oxide (BOX) are located near the interface of Si and Ge. The dislocations which run parallel to BOX are observed only in [110] and [1–10] direction resulting Ge grown toward [010]direction contains no dislocations. This mechanism is similar to aspect-ratio-trapping but here we are using a horizontal approach, which offers the option to remove the defective areas by standard structuring techniques. A root mean square of roughness of ~0.2 nm is obtained after the SiO2 cap removal. Tensile strain in the Ge layer is observed due to higher thermal expansion coefficient of Ge compared to Si and SiO2.

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Selective lateral germanium growth is of great interest. Several techniques to grow high quality Ge on Si are reported e.g. in combination with thermal cycling,2,3 cyclic annealing and etching,4,5 aspect ratio trapping6 and nano hetero epitaxy.7 On the other hand, for optoelectronic devices, Ge-on-insulator (GeOI) substrate is widely used. Wafer bonding technique8 and Ge condensation method9 are used for GeOI wafer fabrication. However, in order to integrate Ge lasers / photodiodes into CMOS technology, local GeOI fabrication on Si-on-buried oxide (BOX) is required because both Si-based devices and Ge-based devices are needed for local GeOI fabrication. In this study, various problems related to Ge growth, etching, and strain distribution in the Ge layer are also discussed.

Experimental

Lateral Ge growth is carried out by using a single wafer reduced pressure (RP) chemical vapor deposition (CVD) system. For sample preparation, epitaxial Si is deposited on SOI wafer of (001) orientation to adjust Si on buried oxide thickness to 430 nm. Then wet oxidation is performed to produce a 300 nm thick SiO2 cap on top of 300 nm thick Si on the buried oxide (BOX). After that the SiO2 cap is patterned by photolithography and etched by buffered HF to form mesa structure. Checkerboard mesa structures and line and space structures with [110] and [100] oriented sidewalls are fabricated.

After that, the wafer is cleaned by standard RCA cleaning followed by HF last dip. Then the wafer is loaded into the RPCVD reactor and baked at 850 °C in H2 to remove residual oxide on the Si surface. Then selective HCl vapor phase etching (VPE) is performed at 850°C to etch Si surface around the mesa and form a cavity under the mesa by lateral Si etching. About 1.5 μm of lateral cavity interposed by SiO2 is formed by selective HCl VPE. Afterwards Ge is deposited selectively in the cavity using a H2-GeH4 source gas at 650°C. To ensure selectivity, small amount of HCl is also added during the selective Ge epitaxy.

Scanning electron microscope (SEM) is used for characterization of the deposited Ge. Scanning transmission electron microscope (STEM) is applied for etching. For STEM sample preparation, focused ion beam (FIB) is used to cut out a lamella at center of the mesa structure. The FIB lamella is cut perpendicular to the sidewall orientation for both [110] and [010] oriented mesa structures. STEM high-angle annular dark field (STEM-HAADF) image is used for characterizing interface of Ge and Si. Nano beam diffraction (NBD) and micro Raman spectroscopy at 514 nm laser wavelength are used for strain distribution analysis in Si and Ge layers. The Raman shift of the Ge–Ge mode ωGe–Ge in the Ge layer and the Si–Si mode ωSi–Si in the Si were measured with respect to the phonon mode energies ωGe–Ge and ωSi–Si as measured in Ge(001) and Si(001) reference bulk crystals respectively. The equivalent in-plane biaxial strain εbi was calculated using the relationships:

\[ \varepsilon_{bi}^{Ge} = \frac{\omega_{Ge-Ge} - \omega_{Ge-Ge}^{0}}{-390} \]  
\[ \varepsilon_{bi}^{Si} = \frac{\omega_{Si-Si} - \omega_{Si-Si}^{0}}{-830} \]  

Results and Discussion

Figure 1a and Fig. 1b show an angle view and cross section SEM image of the sample after HCl VPE, respectively. By the HCl VPE, the Si around SiO2 mesa structures and Si between the BOX and the SiO2 cap are removed. A 1.3 μm to 1.5 μm deep cavity is formed by the HCl VPE. The thickness loss of the BOX and the SiO2 cap are not visible indicating that this HCl VPE process is highly selective to SiO2. No bending is observed at the floating part of the SiO2 cap layer. At the etch front of Fig. 1b, a (331) facet is observed. In the case of the BOX and space structure with [110] Sidewall, no (331) facet but only a (111) facet were observed. The different facet formation of the mesa structure seems to be caused by various HCl VPE directions. The HCl VPE starts from four different sidewalls and corners. Because the etch rate of the corner is faster compared to straight sidewall region, the orientation of the facet becomes only (111) but also additional non-parallel orientations to [110] sidewall. The sample of Fig. 1b is cut at the position whose sidewall is not perpendicular to the cross section surface.

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A cross section STEM image of the sample after HCl VPE and selective Ge growth is shown in Fig. 2. In Fig. 2a, the sidewalls are parallel to [110] and in Fig. 2c parallel to [010] direction. Close up images of interface between Si and Ge of Fig. 2a and Fig. 2c are shown in Fig. 2b and Fig. 2d, respectively. The Ge layers are selectively grown laterally on the Si sidewall in the cavity formed by the HCl VPE. No polygrain formation is observed in the cavity formed in Fig. 2a and Fig. 2c. That shows that the deposition process is highly selective. In Fig. 2c, smaller width of the epitaxial Si pillar after etching is observed compared to that of the mesa structure with [110] sidewall (Fig. 2a) indicating faster etch rate during the HCl VPE. For both samples, complex interface which contains (111), (331), (−331) and (−111) is observed between Si and Ge in Fig. 2b and Fig. 2d. The complex interface seems to be caused by HCl VPE of various etching direction in the mesa structure due to four sidewalls and corners. The sidewall of Si is not perpendicular to the TEM lamella. Dislocations are densely located in the Ge near the interface between Si and Ge for the [110] direction and (c) parallel to BOX. The dislocations in Ge are directed to [111] or [11−1]. Aspect ratio trapping works both [110] and [010] direction (Fig. 2b and Fig. 2d). The dislocations in Ge are also observed in the cross section STEM images in Fig. 3. In Fig. 3a and 3b show plan-view STEM images of a 5 μm square mesa structure with [110] and [010] sidewall after HCl VPE and lateral Ge growth, respectively. For both cases, high density dislocation networks are located near the Si interface only. These high density dislocations are also observed in the cross section STEM images in Fig. 2a – 2d, so they are directed to SiO2 cap or BOX. Long dislocations which run parallel to BOX are observed also. The long dislocations run direct to the [110] and [1−10], independently on the sidewall orientation of mesa structures. Therefore a wide Ge area without any dislocations is formed toward [010] direction.

In Figure 4, an AFM surface roughness image of the 5 μm square mesa structure with [010] sidewall direction is shown after the HCl VPE and the lateral Ge growth followed by removal of the SiO2 cap by buffered HF dip. The interphase between Si and Ge is visible. A step between Si and Ge surface of about ~0.5 nm is observed. The step formation is mainly caused by the cap layer removal. The root mean square of roughness (RMS) of Si and Ge surfaces are ~0.2 nm and ~0.19 nm, respectively. In the case of vertical Ge growth on Si, low temperature seed Ge layer is required to realize smooth surface.4 However, in this case, the low temperature seed Ge deposition process to form two-dimensional smooth surface4 is not required for the selective lateral Ge growth, because the surface of the GeOI is determined by surface roughness of SiO2 cap layer after the HCl VPE process. That gives additional advantage to improve throughput by operating higher growth rate condition at higher temperature.

The strain distribution plots of Si and Ge measured by micro Raman mapping are shown in Fig. 5a and Fig. 5b, respectively. In the Si pillar, ~0.09% of tensile strain is observed (Fig. 5a). This tensile

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**Figure 1.** Angle view (a) and cross section (b) SEM images of sample after HCl VPE. The orientation of the sidewall is parallel to the [110] direction.

**Figure 2.** Cross section STEM images after HCl VPE followed by selective Ge deposition. Orientations of the sidewall of (a) and (b) are parallel to [110] direction and (c) and (d) are parallel to [010] direction. Higher magnification images near interface between Si and Ge are shown in (b) and (d).

**Figure 3.** Plan-view STEM image of 5 μm square mesa structure with (a) [110] and (b) [010] sidewall direction after HCl etching and lateral Ge growth. The sidewall orientation is described with arrow.

**Figure 4.** AFM surface roughness image of 5 μm square mesa structure with [010] sidewall direction after HCl etching and lateral Ge growth. The strain distribution plots of Si and Ge measured by micro Raman mapping are shown in (a) and (b). The [110] direction is indicated by the arrow.
strain level in the Si pillar was also detected from the sample after HCl VPE (before selective growth of Ge). However, no strain in Si on BOX was evidenced in wide plain area of the same wafer, which is located outside of the checkerboard mesa array structure. These results are indicating that the Si on the BOX is not initially strained. Because the interface area between the Si pillar and SiO$_2$ is small, the Si pillar seems to be slipped during the HCl VPE at 850 $^\circ$C due to thermal expansion coefficient difference between Si ($\sim 4 \times 10^{-6}$ K$^{-1}$) and SiO$_2$ ($\sim 5 \times 10^{-7}$ K$^{-1}$). The tensile strain in the Si pillar could be formed during cooling period after the HCl VPE. On the other hand, the Ge around Si pillar is also tensely strained (Fig. 5b). The degree of strain is $\sim 0.25\%$ to $\sim 0.3\%$. The strain of the Ge layer near the edge is weaker compared to that near interface to the Si pillar. Possible cause of the strain compensation could be a slight bending of SiO$_2$ cap layer,
results (Fig. 5a, 6b), it is possible to conclude that the Si pillar is tensely strained and the degree of the tensile strain is lower compared to that in the Ge part. The curves of the relative lattice constant of [400] and [004] direction (averaged in dotted square in Fig. 6a and Fig. 6b) are almost parallel for both the Ge and the Si part (Fig. 6c). This indicates constant strain in lateral direction for both Si and Ge for 400 nm from the interface at least. These results also support the micro Raman measurement already shown in Fig. 5a and 5b. In Fig. 6c, a small reduction of lattice constant in Ge near Si / Ge interface is observed. STEM-HAADF image (Fig. 6d) shows a contrast change in Ge near the interface, indicating presence of Si in the Ge near the interface. Because process temperature is below 650 °C, no or very few Si diffusion in Ge is expected. It seems that the interface between Si and Ge of the STEM lamella is not perpendicular to the lamella. In this case the lower lattice constant of Ge at the interface is caused by projection of non-straight Ge / Si interface.

Conclusions

High quality local GeOI wafers are fabricated using selective lateral Ge growth technique by a single wafer RPCVD system. Mesa structures of 300 nm SiO2 cap and Si on BOX with [110] and [010] oriented sidewall are prepared. Selective etching of Si by HCl followed by selective lateral Ge growth is performed. Lateral aspect-ratio trapping is working in the Ge layer resulting in prevention of dislocation formation after ~150 nm from the Si interface. Dislocations along the Ge growth direction are oriented only in [110] and [1–10] directions. Therefore a wide area of Ge without dislocations is grown toward [010] direction. The deposited Ge exhibit a smooth surface. Tensile strain in the Ge layer is observed due to thermal expansion coefficient difference between Si and Ge. Higher degree of the strain is observed because of additional tensile strain in Si pillar. These results demonstrate the feasibility of the fabrication of local GeOI with high crystal quality. Defective part can be removed by an additional lithography and an etching process.

References

1. S. B. Samavedam, M. T. Currie, T. A. Langdo, and E. A. Fitzgerald, Appl. Phys. Lett., 73(15), 2125 (1998).
2. J. M. Hartmann, A. Abbade, A. M. Papon, P. HOLLiger, G. Rolland, and T. Billon, J. Appl. Phys., 95, 5905 (2004).
3. J. M. Hartmann, J. F. Damlencourt, Y. Bogumilowicz, P. Holliger, G. Rolland, and T. Billon, J. Cryst. Growth, 274, 90 (2005).
4. Y. Yamamoto, P. Zaumseil, T. Arguiroz, M. KITTLer, and B. Tillack, Solid-State Electronics, 60, 2 (2011).
5. Y. Yamamoto, G. Kozloski, P. Zaumseil, and B. Tillack, Thin Solid Films, 520, 3216 (2012).
6. J.-S. Park, J. Bai, M. Curtin, B. Adekore, M. Carroll, and A. Lochtefeld, Appl. Phys. Lett., 90, 052113 (2007).
7. P. Zaumseil, Y. Yamamoto, M. A. Schubert, T. Schroeder, and B. Tillack, Thin Solid Films, 557, 50 (2014).
8. T. Akatsu, C. Deguet, L. Sanchez, A. Allibert, D. Rouchon, T. Signamarcheix, C. Richtarch, A. Bossagol, V. Llop, F. Mazen, J. M. Hartmann, Y. Campidelli, L. Clavelier, F. Letertre, K. Kernevez, and C. Mazure, Materials Sci. in Semiconductor Processing, 9, 444 (2006).
9. S. Nakahara, T. Terazaki, N. Sugiyama, Y. Moriyama, and S. Takagi, Appl. Phys. Lett., 83, 3516 (2003).
10. J. G. Fiorenza, J.-S. park, J. M. Hydrick, J. Li, J. Z. Li, M. Curtin, M. Carroll, and A. Lochtefeld, ECS Transactions, 33(6), 963 (2010).
11. Y. Yamamoto, K. Köpke, and B. Tillack, Thin Solid Films, 517, 98 (2008).
12. G. Capellini, G. Kozloski, Y. Yamamoto, M. Lisker, C. Weng, G. Niu, P. Zaumseil, B. Tillack, A. Ghribi, M. de Kersauson, M. El Kuri, P. Boucaud, and T. Schroeder, J. Appl. Phys., 113, 01351 (2013).
13. F. Pezzoli, E. Bonera, E. Grilli, M. Guzzi, S. Sanguinetti, D. Christina, G. Isella, H. von Känel, E. Wintersberger, J. Stangl, and G. Bauer, Mater. Sci. Semicond. Process., 11, 279 (2008).