INVESTIGATION OF DEVICE PERFORMANCE AND PROCESS CAPABILITY FOR ACCURATE SOFC COST ESTIMATES

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ABSTRACT

Manufacturing and production costs are a major concern for the development and commercialization of solid oxide fuel cells (SOFCs) [1]. A current review of research indicates that device geometries with thin (<30 μm) film layers and reduced stack temperature gradients will be required to meet device performance and reliability requirements [2]. We have developed a process based cost model for high volume manufacturing of SOFC devices [3]. This work investigates the sensitivity of SOFC device manufacturing costs with respect to device performance and reliability requirements. We have incorporated process capability requirements to determine at what performance level process capability must be considered to provide an accurate cost model, enabling a determination of cost viability for device designs prior to manufacturing investment. We have also investigated the cost of process capability against the potential savings in balance of plant costs as device operation temperatures are reduced. Our work indicates that the device designs requiring electrolyte films at less than 30 μm result in a cost difference of up to $50 per unit cell, for traditional screen printing and tape casting processes. Additionally, our investigation indicates that the savings in materials and manufacturing for BOP costs at lower temperatures may not be offset for operation temperatures below 700°C for cell maximum power densities of 1 W/cm². Additionally, cost performance maps are used to indicate optimum performance and operation temperature regimes for 5 kW system cost minimization.

INTRODUCTION

Until recently, the viability of SOFC designs has been based primarily on the performance and reliability characteristics of the device. As the SOFC development cycle has migrated from cell design and laboratory performance testing to the development and integration of manufacturing processes, viability of cell design based on production costs has become a more significant consideration. The performance of numerous anode supported SOFC cell designs has been extensively investigated utilizing a thin film (<30 μm) electrolyte layer [4,5]. The popularity of these designs lies in the reduction of the
stack operating temperatures below 1173 K (800°C) [6]. This reduction in stack operating
temperature enables the use of metallic alloy interconnects and traditional balance of
plant components, offering significant cost reduction when compared to the ceramic
interconnects and high temperature components required for cell operation at
temperatures greater than 800°C.

Additionally, advanced performance and reliability modeling techniques have linked poor
cell performance and cell stack failure to variation in cell operation temperature and cell-
to-cell within stack gas flow [7,8]. These variations may occur as a result of asymmetry
in cell/stack geometry due to poor manufacturing process capability and tolerance
requirements.

Process based cost models (PBCM) [9] have been shown to be effective in modeling
complex cost systems in the absence of historical data. The development of Worcester
Polytechnic Institute’s Alternative Fuel Economics Laboratory (AFEL) SOFC cost model
is well documented in previous literature [10,11]. It is the goal of this work to utilize the
AFEL cost model to investigate the sensitivity of cell and SOFC stack production costs
with respect to device performance and reliability requirements. Within the AFEL cost
model framework, we have investigated the sensitivity of SOFC device within stack
performance and operation temperature gradients on unit cell and system costs. This
analysis enables a determination of cost viability for device designs as a function of
manufacturing process capability prior to manufacturing investment. We have also
investigated the cost of process capability against the potential savings in balance of plant
costs as device operation temperatures are reduced.

**EXPERIMENTAL METHOD**

For our initial case study, anode-supported planar SOFCs were examined. The
electrolyte layer thickness was modeled as the primary input factor for device
performance. Additionally, we have used electrolyte layer thickness tolerances, based on
performance and operation temperature gradient requirements as the primary input for
device reliability. A flow diagram of the AFEL cost model is shown in Figure 1.

We have considered two processing routes: a co-sintered route and a layer by layer
processing route. These routes are described in Figure 2 for the manufacture of planar
SOFCs. For the co-sintered route the layers are tape cast individually and then laminated
and blanked. In the layer by layer route the layers are cast and sintered successively.
Three processes were considered for creation of the electrolyte layers: tape casting,
screen printing and sputtering.

The baseline cell for this study consists of a nickel cermet anode supporting a yttria
stabilized zirconia (YSZ) electrode and a fixed thickness 50 μm Lanthanum Strontium
Manganese (LSM) cathode. Cell operation temperatures were varied from 600-850°C
with performance held at 1W/cm², unless otherwise noted. Stack performance and
operation temperature gradients were varied up to +/- 5% of nominal power density and
+/-2% of nominal operation temperature as indicated. The cost for metallic and ceramic
interconnects and balance of plant components are included within the calculations as
indicated throughout the temperature operation range. The process capability information
for the cost model is based on existing process capability information from high volume ceramic multi-layer capacitors manufacturing, including information available from the literature, interviews with equipment manufacturers and in house processing expertise.

Interconnect and BOP costs were estimated based on cost analysis provided in the literature [12-14]. Interconnect materials considered were ceramic lanthanum chromite-based for high temperature (>800°C) applications and ferritic steel interconnects for lower operation temperatures. BOP considerations include purchased components, raw material and processing costs for POX reformer, fuel and air preparation to include reformers and pre-heaters, pumps, compressors, and balance of system components. System operation is based on a 5 kW stack with a single cell maximum power density of 1 W/cm², 90% H₂ utilization, and 50% efficiency loss in the stack. A summary of interconnect and BOP costs used in this analysis is shown in Table I.
Table I. Interconnect and BOP Cost Estimates used in this analysis.

| Table I. Interconnect Cost Estimates Per Unit Cell |
|---------------------------------------------------|
| Ferritic Stainless Steel | $5.00 |
| Ceramic | $9.00 |
| **BOP cost - 5kW system** | |
| < 800°C | $400.00 |
| >= 800°C | $665.00 |
| Fuel and Air Preparation | | $360.00 |
| Rotating Equipment | $600.00 |
| Balance of System | | $410.00 |
| **Total BOP 5kW stack** | | $1,170.00 |

RESULTS AND DISCUSSION

Unit Cell Cost Effects

The electrolyte thickness tolerances for a operation temperature gradient of 2% of nominal and stack performance gradient of 5% of nominal are calculated using the performance model and graphically represented across the range of electrolyte thicknesses in Figure 3. For example, for a 5kW stack with a cell maximum power density operating at 1 W/cm², at 700°C, to insure a stack temperature gradient of less than 2% (686°C to 714°C) the electrolyte thickness must be manufactured to within a tolerance of 15.5 μm ± 3.5 μm. For this same stack, to insure a performance gradient of less than 5% from nominal (.95 W/cm² to 1.05 W/cm²), the electrolyte thickness tolerance must be held at 15.5 μm ± 3.5 μm.

Figure 3. Electrolyte thickness tolerances for an operation temperature gradient of 2% of nominal and stack performance gradient of 5% of nominal.
The AFEL model determines the most restrictive thickness tolerance levels for performance and reliability requirements and compares these tolerances to processing capabilities to determine processing yield loss. The yield loss is incorporated within the manufacturing cost model to determine cost impacts to the unit cell manufacturing.

Figures 4 and 5 represent the unit cell cost for the electrolyte layer thickness for a range of performance and temperature gradients. Figures 4a and 5a are shown for the layer by layer (TC-SP-SP) manufacturing flow and Figure 4b and 5b are shown for the co-sintered (TC-CS) process flow.

These graphs show a significant difference in unit cell manufacturing costs as performance and temperature gradient requirements are decreased. This cost difference can be attributed to the decreased processing yield as performance and temperature gradient requirements are reduced. For the layer by layer process, the unit cell cost increases up to 500% (>$50 per unit cell) at the thinnest electrolyte layers. The cost difference is shown to be less significant (<$1.00 per unit cell) for the co-sintered process. For both process flows, the cost differences are the most significant at electrolyte thickness levels less than 30 μm, corresponding to the limits of process capability for tape casting and screen printing processes.

Figure 4. Per cell cost ($) across electrolyte thicknesses (μm) for a range of operation temperature gradients; (a) TC-SP-SP process flow; (b) TC-CS process flow.

Figure 5. Per cell cost ($) across electrolyte thicknesses (μm) for a range of performance gradients, TC-SP-SP process flow; (b) TC-CS process flow.
Stack Cost Effects

A secondary investigation of this paper was to incorporate manufacturing process capability into the cost benefit analysis for operation of devices at lower operating temperatures. The lower operation temperature does allow use of lower cost interconnect and BOP components, but typical anode supported designs require low (<30 μm) electrolyte thickness levels, which may result in a higher unit cost basis due to lower process capability impacts.

Figure 6 shows the adjusted stack cost for a 5kW stack across a range of operation temperatures for both layer by layer and co-sinter process flows. For this analysis, a 10% stack performance gradient was used. As expected, a significant shift in stack costs occurs at 800°C. This shift is due to the use of lower cost interconnect and BOP components. However, for both processes, as the operation temperature decreases, the stack costs increase reflecting the yield loss at the lower electrolyte thickness levels. For the layer by layer process (TC-SP-SP), this increase is significant enough to negate the cost benefit of the lower cost interconnect and BOP components. This phenomenon is further highlighted in the contour maps of stack performance and temperature with respect to stack cost shown in Figures 7 and 8. A low cost optimum is shown for both processes at 750°C, and a cell maximum power density of 1.15 W/cm². Outside of this optimum, the costs significantly increase: at higher operation temperatures due to increased BOP and interconnect costs at higher operation temperatures, due to lower process capability at <30 μm electrolyte film thicknesses.

![Figure 6. Total System Cost for 5 kW system as a function of operating temperature for different process flows (+/- 10% cell performance gradient).](image)
CONCLUSIONS

The AFEL performance based cost model has been used to determine the impact of stack performance and reliability requirements on unit cell and stack costs. Our model indicates that stack performance and reliability requirements may impact cost estimates by as much at 500%, (up to $50/unit cell) depending on the level of requirements and process flow used.

Additionally our investigation indicates that the emphasis on low cost SOFCs by reducing the stack operation temperature to less than 800 °C may be compromised as electrolyte thickness levels decrease beyond the manufacturing process capability, typically less than 30 µm for tape casting and screen printing processes. Process maps indicate an optimum for cost minimization at 750 °C for cell maximum power densities of 1 W/cm².
REFERENCES

1. H. Woodward, et al., MRS Proceedings, Solid State Ionics, 756, FF4.10, (2002).
2. SOFC-VIII, S. C. Singhal and M. Dokiya, Editors, PV2003-07, pp. 935-1210, The Electrochemical Society Proceedings Series, Pennington, NJ, (2003).
3. H. Woodward, “A Performance Based, Multi-process Cost Model for Solid Oxide Fuel Cells,” http://www.wpi.edu/Pubs/ETD/Available/etd-0428103-235205/.
4. Solid Oxide Fuel Cells VIII, S.C. Singhal and M. Dokiya, Editors, PV2003-07, pp. 935-1210, The Electrochemical Society Proceedings Series, Pennington, NJ, (2003).
5. N. P. Brandon, et al., Journal of Materials Engineering and Performance, 13(3), 253-256 (2004).
6. Z. G. Yang, J. W. Stevenson, P. Singh, Advanced Materials and Processes, pp. 34-37 (2003).
7. A. C. Burt, et al., in SOFC-VIII, S. C. Singhal and M. Dokiya, Editors, PV2003-07, pp. 1487-1500, The Electrochemical Society Proceedings Series, Pennington, NJ, (2003).
8. D. Larrain, J. Van herle, M. Graetzel, D. Favrat, in SOFC-VIII, S. C. Singhal and M. Dokiya, Editors, PV2003-07, pp.1478-1486, The Electrochemical Society Proceedings Series, Pennington, NJ, (2003).
9. R. Kirchain and F. R. Field III, “Process-Based Cost Modeling: Understanding the Economics of Technical Decisions,” in Encyclopedia of Materials Science and Engineering, Elsevier, (2001).
10. M. Koslowske, “A Process Based Cost Model for Multi-Layer Ceramic Manufacturing of Solid Oxide Fuel Cells,” http://www.wpi.edu/Pubs/ETD/Available/etd-0810103-173353/.
11. H. Woodward, et al., MRS Proceedings, Solid-State Ionics, 756, FF4.10, (2002).
12. Arthur D. Little, “Conceptual Design of POX/SOFC 5kW Net System,” Report to DOE NETL, Reference 71316, (2001).
13. S. J. Visco, et al., in SOFC-VIII, S. C. Singhal and M. Dokiya, Editors, PV2003-07, pp. 1040-1050, The Electrochemical Society Proceedings Series, Pennington, NJ, (2003).
14. E. Fontell, et al., Journal of Power Sources, 131, 49-56 (2004).