Dual priority congestion aware shared-resource Network-on-Chip architecture

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Abstract: Network-on-Chip has become the mainstream interconnection technology for next generation MPSoCs. Exploit of high performance and efficient NoC architecture has been a research hotspot for Network-on-Chip design. In this paper, we present a Dual Priority Congestion Aware Shared-Resource Network-on-Chip architecture (DP-CASR), which could effectively alleviate the resource contention and improve the routing efficiency. Based on 2D-Mesh network, a centralized-distributed hybrid topology is proposed. To make a trade-off between the performance and overheads, both deterministic and adaptive routing metric are introduced in DP-CASR. Compared with typical XY routing and RCA adaptive routing, DP-CASR could achieve higher saturation throughput than that of XY and RCA by 148% and 80% in average, respectively. Moreover, the extra overhead of DP-CASR over 2D Mesh network is only 9%.

Keywords: Network-on-Chip, congestion-aware, adaptive routing

Classification: Integrated circuits

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1 Introduction

Network topology and routing algorithm are the two most important factors that impact on Network’s performance, area overhead and power consumption [1, 2, 3]. Several network topologies have been studied for designing the communication infrastructure [4]. Mesh structure having single core attached with each router is mostly used in industries for practical chip implementation [5]. Although Mesh network is widely accepted for NoC design in both academia and industries, it has some limitations. Mesh network has larger diameter, which means that packets have to cross more number of hops to reach their destinations. The large diameter also means that the network is susceptible to network congestion. The effects of even a single router congested can quickly spread spatially across the NoC topology, which will apply backpressure onto the advancing traffic and eventually halt its flow even when traversing interconnect links of theoretically infinite bandwidth [6].

The performance of NoC is sensitive to the routing algorithm, as it defines the network latency and saturation throughput. Commonly, the adaptive routing algorithm is used in current NoC designs to realize high performance routing and reduce network congestion. Many congestion-aware adaptive routing algorithms have been proposed [7, 8, 9, 10, 11, 12]. All these works collect the network status dynamically, react to adverse conditions, and then act to reduce or correct the impact of elevated network throughput demands by spatially spreading traffic among alternative routes. In these routing algorithms, router owns the regional or even the whole network’s status information. However, single router could only make its own routing decisions which would result in low efficiency from the global perspective. So the usage of the distributed routing metric makes it difficult to alleviate the network congestion for NoC design, both the routing algorithm intricacy and the hardware overheads increase simultaneously.

To improve the resource utilization and achieve higher network performance, a dual priority congestion aware shared-resource Network-on-Chip architecture (DP-CASR) is proposed in this paper. DP-CASR contains the proposed topology and routing algorithm. The proposed topology is a centralized-distributed hybrid network topology. The link resource could be shared by routers. In the proposed routing algorithm, packets are classified into high priority packet and low priority packet according to the relative location of source and destination. To reduce the extra hardware overheads, both deterministic and adaptive routing metric are introduced. Moreover, the local and regional congestion information is used to
support adaptive routing. Experimental results show that DP-CASR could effectively improve network performance. Compared with typical XY routing and RCA adaptive routing, DP-CASR could achieve higher saturation throughput than that of XY and RCA by 148% and 80.4% in average, respectively. In $4 \times 4$ network, DP-CASR could achieve ideal network performance under transpose, shuffle, butterfly and bit reverse traffic, which means that it could provide the potential to avoid the resource contention. In the aspect of cost, DP-CASR only consumes 9% more hardware overheads than 2D Mesh network.

2 Network topology

DP-CASR makes a trade-off between the centralized bus-based interconnection and the distributed NoC-based interconnection. The corresponding network topology is presented in Fig. 1(a). The network implements the wormhole packet switching technique. Based on 2D Mesh topology, the traffic manager (TM), which could be classified into the horizontal TM and the vertical TM, is introduced into the proposed network topology. The horizontal TMs are inserted between two adjacent columns and the vertical TMs are inserted between two adjacent rows. Under the control of TM, it could be seen that the link resource between different columns and rows is shared by routers. Moreover, TM is the crucial component in DP-CASR, and it could remarkably reduce the network diameter and improve the routing efficiency.

3 Routing algorithm

Based on the proposed topology, the corresponding routing algorithm is proposed to exploit more available resource and achieve better network performance.

The example routing paths are shown in Fig. 1(b). In DP-CASR, the packet transmission includes three parts: ① Packet injection, the source router injects packet to the corresponding adjacent TM based on the destination coordinates and congested level of neighbor region, this is called “injection port selection”; ② Link
allocation, TM, which receives requests from neighbor routers, takes the routing information and network congested status into consideration, then it allocates link resource to packet, this is called “transmission output selection”. According to the relative location of destination and current TM, packet would be transmitted to the intermediate router or the destination router; ③ Packet forward, the intermediate router receives packet from neighbor TM and forwards them straight to the next TM without routing computation. For example, if the router receives packet from east port, the packet would be transmitted to west port (the situation is similar to other directions: west to east, south to north, and north to south). From the above description it could be found that when being injected to horizontal TM or vertical TM, packet would only be transmitted by the same type TMs. So there are no cycles in the resource dependence graph. As a result, this deterministic routing metric could avoid dead-lock.

In the proposed algorithm, packets are classified into high priority packet and low priority packet according to the relative locations of source and destination. In routing computation, routers and TMs obtain a list of possible outputs based on location information and give priorities to packet. For high priority packet, the available choice would be only one so that the congestion-aware routing metric is not used. For low priority packet, routers and TMs would select a relatively less congested output to transmit packet. The followings will elaborate the selection algorithms used in router and TM, respectively.

### 3.1 Injection port selection

To improve resource utilization and balance the workload distribution, the injection port selection algorithm is employed in source node to select the port to which packet is injected. The injection port selection algorithm has two steps. First, a possible injection port set is obtained by the source router. If the source node and destination node are in the same row, packet would be injected through east or west port, or if the source node and destination node are in the same column, packet would be injected through south or north port. For the source router, these packets are called high priority packet. Then, if the source node and destination node are in different column and row, there exist two possible injection ports. These packets are called low priority packet. The queue time of each direction are used as the congestion information in injection port selection algorithm. Based on the collected congestion information, the source router would select a less congested direction to transmit packet.

### 3.2 Transmission output selection

Based on the regional and local congestion information, the Transmission Output Selection algorithm is proposed to improve the performance and alleviate the congestion. According to the relationship between destination router and current TM, the packet transmitted in TM also has two categories: high priority packet and low priority packet. The high priority packet, of which the destination router is connected to the current TM, could only be transmitted through the corresponding output. The low priority packet, of which the destination router isn’t connected to the current TM, could be transmitted through any output of the current TM’s.
The allocation for low priority packet has an impact on network performance. It is the key part of the proposed algorithm. To improve resource utilization and routing efficiency, both local and regional congestion information is used in transmission output selection algorithm. The local link statuses reflect the output utilization of current TM, and the next TM’s input link statuses represent the link utilization of the adjacent downstream TM. Both of these two statuses are collected as local and regional congestion information, respectively. Along with the congestion information, the requests of high priority packet are also taken into consideration to obtain idle outputs. An idle output means that both the current output of TM and the corresponding output of next router are available. The low priority packet could be directly transmitted to the next TM. For multiple requests, the Round-Robin scheduling is employed to allocate idle outputs.

In transmission output selection algorithm, the high priority packet, which neglects the congestion information, will be transmitted to the required output. Because of the routing constrains in the proposed algorithm, only one output is available for high priority packet in the final stage TM. So if the required output is not available, the packet has to be stalled.

4 Experimental results

In evaluation, a Verilog-based network simulator is implemented and used. DP-CASR architecture is designed by Verilog HDL in RTL level. To investigate the benefits of the proposed NoC architecture, DP-CASR is compared with the following routing algorithms (they are implemented on 2D-Mesh network): typical XY routing and RCA [10]. The hop latency is 3 cycles for DP-CASR because that the long link is introduced. Meanwhile, the latency is 2 cycles for XY and RCA. The packet length is uniformly distributed between 1 and 8. The simulator is warmed up for 10,000 cycles and then the performance is measured over another 200,000 cycles.

Fig. 2 shows the latency performance of different routing algorithms both in 4 × 4 and 8 × 8 network under six synthetic traffics. In 4 × 4 network, compared with XY and RCA, DP-CASR could significantly improve network performance.
hotspot pattern, the workload is focused in the centre of the network so that it is difficult to handle the resource contention. As a result, the improvement of DP-CASR is not evident. In non-uniform traffic patterns, DP-CASR could achieve ideal network performance, which means it could effectively eliminate the network congestion. In 8 × 8 network, DP-CASR also could realize better performance.

![Figure 3. The saturation throughput](image)

The network saturation throughputs are depicted in Fig. 3. In 4 × 4 network, DP-CASR could improve the saturation throughput to XY and RCA by 107% and 64%, respectively. Moreover, the saturation throughput of DP-CASR in non-uniform traffics could reach 1 flit/cycle/IP, which means DP-CASR could balance the network workload and improve the resource utilization. In 8 × 8 network, DP-CASR could drastically alleviate the resource contention. The saturation throughputs of DP-CASR could also exceed 0.5 flit/cycle/IP. DP-CASR could realize 190% and 97% improvement of saturation throughput to XY and RCA. As the results illustrated, DP-CASR, which could exploit more available routing resource, is an effective adaptive routing algorithm to alleviate network congestion and improve network performance.

### 5 Synthesis results

#### Table 1. Hardware overheads details.

| Component | Area (µm²) | Normalization |
|-----------|------------|---------------|
| Mesh      |            |               |
| Network   | 3,974,317  | 1             |
| Router    | 74,296     |               |
| DP-CASR   |            |               |
| Network   | 4,353,514  | 1.09          |
| Router    | 71,639     | 0.96          |
| TM        | 9,264      | -             |

To evaluate the hardware overheads, DP-CASR architecture and 2D-Mesh network (XY routing) were designed by Verilog HDL in Register-Transfer Level (RTL). A 65-nm CMOS standard-cell library from SMIC Technology is used to synthesize
the NoC designs. The FIFO depth is 16 for both DP-CASR and 2D Mesh. The working clock frequency is set to 1 GHz. Table I summarizes the detailed hardware overheads of 8 × 8 network. Compared with typical wormhole router in 2D Mesh, DP-CASR could reduce router’s hardware overhead. This owes to the proposed “packet forward” algorithm, which could simplify the routing computation during the transmission. On the other hand, TM is introduced into DP-CASR. Compared with router, TM only transmits packets and doesn’t store them so that there is no FIFO used. As a result, the hardware overhead of TM is not large. Moreover, it could be found in Table I that the component area of DP-CASR (which contains 64 routers and 14 TMs) is less than that of 2D Mesh (which contains 64 routers). But from the whole network aspect, the increased overhead of DP-CASR over 2D Mesh network is 9%. This is because TMs in DP-CASR not only collect congestion information from the adjacent routers, but also communicate with the adjacent routers. So the long links are introduced into the network, which need a certain amount of hardware overheads. In general, the extra overhead of DP-CASR is tolerable.

6 Conclusion

In this paper, a Dual Priority Congestion Aware Shared-Resource NoC architecture (DP-CASR) is proposed. To exploit more available routing resource and improve routing efficiency, the congestion-aware routing metrics are introduced both into router and TM. The injection port selection algorithm and the transmission output selection algorithm are proposed to alleviate the resource contention and balance the workload. Experimental results show that DP-CASR could achieve better saturation throughput and average latency performance. Compared with XY and RCA, the improvement of saturation throughput could reach 148% and 80% in average. These results reveal that DP-CASR can effectively alleviate network congestion and improve network performance. Moreover, in the aspect of cost, DP-CASR only consumes 9% more hardware overheads than 2D Mesh network.

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