A Generalized Modulation Method for Common-Mode Voltage Reduction of Dual-Input Three-Level Inverter

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ABSTRACT The dual-input three-level inverter should have the ability to operate in certain areas where the dc-links are unbalanced. This paper proposes a generalized large-medium-zero space vector modulation (GLMZ-SVM) method to obtain high-quality output currents and suppress common-mode voltage (CMV) amplitude simultaneously when the dc-links are unbalanced. In this method, a modified space voltage vector diagram (MSVVD) based on the unbalancing factor is obtained, which is highly asymmetrical compared to the space vector diagram when the dc-links are balanced. Then, a novel sector division method of MSVVD is presented by six medium vectors and six large vectors. In each sector, the large, medium, and zero vectors are used to synthesize the reference voltage vector to reduce the CMV amplitude. The duty cycles of large, medium and zero vectors are calculated based on the modified volt-second balance principle with the unbalancing factor. To further reduce harmonics and avoid switching losses between switching cycles, a symmetrical five-segment switching sequence is designed. Comparisons with conventional methods show that the CMV amplitude of the proposed method is reduced by half and the high-quality output currents are obtained. Both simulation and experimental results validate the correctness of the theoretical analyses and the effectiveness of the proposed scheme.

INDEX TERMS Common-mode voltage (CMV), dual-input three-level inverter, generalized large-medium-zero space vector modulation (GLMZ-SVM), unbalanced dc-links.

I. INTRODUCTION

With the rapid consumption of fossil fuels and environmental pollution problems, renewable energy sources such as solar energy and wind energy have become the trend of global power generation [1], [2]. As the interface between the renewable energy power generation system and the power grid or load, the converter is the core equipment of the energy conversion and control of the renewable energy generation system, which plays an irreplaceable role [3]. Among them, three-level inverter has strong market demand in various fields of power industry. In particular, three-level neutral point clamped (NPC) inverter and three-level T-type (3LT²) inverter play crucial roles in photovoltaic (PV) power generation systems [4]–[6], wind turbine systems [7], and medium voltage ac drives [8]–[10] because of their advantages such as smaller $dv/dt$, higher quality output waveforms, and smaller filter size compared with two-level inverter [11]–[14]. Therefore, it is very feasible and necessary to study three-level inverters.

Dual-input three-level inverters are used in many practical applications. For example, it can be used for dual maximum power point tracking (MPPT) [15] in PV power generation systems. As another example, solar PV panel and battery are linked to the upper and lower capacitors in order to exploit the maximum power from different sources for a hybrid energy storage integrated system [16]. Furthermore, under high power demand conditions (such as mine operating...
Unbalanced neutral point (NP) voltages occur frequently, especially for dual-input three-level inverters. In some special areas [15]–[17], it is necessary to adjust the capacitor voltages asymmetrically. A lot of work has been done on modulation and control strategies under unbalanced NP voltage conditions. A control strategy was designed in [15] to increase the MPPT efficiency of a PV system NPC inverter when the PV modules were respectively connected to separate capacitor voltages. The properties and operations of a hybrid pulse width modulation (PWM) strategy was investigated in [17] for three-level NPC inverters with unbalanced dc-links. However, none of the above mentioned methods considers the problem of common-mode voltage (CMV) suppression.

Excessive CMV can cause motor shaft voltage, bearing current, and common-mode current, which will result in system performance and lifetime degradation [18]. CMV can be suppressed by topology-based method and modulation-based method. The essential idea of the topology-based method is to change the inverter structure or install additional passive or active devices, which increases the cost and size of the system and reduces the system efficiency. Modulation-based method is favoured since no additional auxiliary components are required. For three-level inverters, there are many interesting

and improved modulation strategies to suppress CMV. Zero common mode modulation technique was proposed in [19] that adopted zero vector and medium vector to synthesize the reference voltage vector to generate output voltage. Taking advantage of the switching states that generate zero CMV, a universal space vector PWM for CMV elimination was given in [20] for any levels and phases. However, these methods of eliminating CMV reduced dc voltage utilization and caused large output current harmonic content. A carrier-based modulation strategy and a hybrid multi-carrier PWM method were proposed in [21] and [22], respectively, to decrease the amplitude of CMV. An improved predictive control method based on two-layer vector selection criteria and a modulation technique using large, medium, and zero vectors were studied respectively in [23] and [24] for CMV reduction. These methods are applicable to balanced dc-side conditions, but unfortunately, current distortion occurs when the upper and lower capacitor voltages on the dc side are not equal.

Therefore, aiming at the unbalanced NP voltage condition, a generalized modulation method adopting large, medium, and zero vectors is proposed in this paper, which can not only obtain high-quality output currents, but also reduce the CMV simultaneously. In most literature, CMV suppression and current distortion problems are generally not considered at the same time. In fact, the CMV problem and the NP voltage unbalanced problem are coupled since the small voltage vectors are utilized in the conventional solutions to the two problems. The proposed method decouples these two problems by eliminating the use of small vectors. The modulation method proposed in this paper is denoted as generalized large-medium-zero space vector modulation (GLMZ-SVM) method due to the use of large, medium, and zero vectors for the synthesis of reference vector and the applicability for both balanced and unbalanced dc-link conditions. First, a modified space voltage vector diagram (MSVVD) based on the unbalancing factor is obtained, which is highly asymmetrical compared to the space vector diagram when the dc-links are balanced. Then, a novel sector division method of MSVVD is presented by six medium vectors and six large vectors. Furthermore, utilizing the modified volt-second balance principle based on the unbalancing factor, the duty cycles of the basic vectors for 12 sectors are calculated. Finally, in order to reduce harmonics and avoid switching losses between switching cycles, a symmetrical five-segment switching sequence is designed that starts and ends with zero vector. Both simulation and experimental results show that the proposed scheme can achieve high-quality output currents and suppress the CMV simultaneously, which perfectly overcomes the defects of these two problems.
TABLE 1. Switching state and output voltage.

| Switching states | ON switches \((\pi = a, b, c)\) | \(u_x\) |
|------------------|--------------------------------|--------|
| P                | \(S_{x1}, S_{x2}\)            | \(VP\) |
| O                | \(S_{x2}, S_{x3}\)            | 0      |
| N                | \(S_{x3}, S_{x4}\)            | \(-VN\)|

on the dual-input three-level inverter prototype are given in Section IV and Section V, respectively. Section VI concludes this paper.

II. THREE-LEVEL INVERTER WITH UNBALANCED DC-LINKS

Fig. 1 shows two simplified circuit configurations for dual-input three-level inverters with split dc links, where Fig. 1(a) is a three-level NPC inverter and Fig. 1(b) is a 3LT2L. These configurations differ from the conventional topology in the connection mode between dc-side system and two capacitors. Each capacitor is connected to a set of dc power source at both ends, for example, in the case of two sets of uncontrolled rectifier bridges in a high-power motor drive system to increase capacity.

The upper and lower capacitor voltages on the dc-side are denoted as \(V_P\) and \(V_N\). \(V_{dc}\) is the total dc-link voltage, i.e.,

\[
V_{dc} = V_P + V_N.
\]  

From Fig. 1, the dc-side neutral point O is selected as the reference, and the switching states of each phase leg are denoted as [P], [O] and [N]. Table 1 shows the switching states and output voltages of the three-level inverter.

The CMV is defined as [25]

\[
V_{CM} = \frac{V_{AO} + V_{BO} + V_{CO}}{3},
\]

where \(V_{AO}\), \(V_{BO}\) and \(V_{CO}\) are the inverter output phase voltages, respectively.

SVM methods are widely used due to their many advantages such as good output waveforms, high dc-link voltage utilization, and easy digital implementation [26]. The space voltage vectors can be divided into zero, small, medium and large vectors according to their magnitudes. When the dc-side capacitor voltages are unbalanced, the space vector diagram of three-level inverter will change greatly, and the conventional SVM method will cause the currents to be distorted, which is no longer applicable.

III. PROPOSED MODULATION METHOD

Since the NP voltage imbalance may occur under certain operating conditions, this requires that dual-input three-level inverters should have the ability to work normally in certain areas where the dc-links are unbalanced. To this end, this paper studies the the space vector-based modulation strategy of three-level dual-input inverter, and the proposed scheme is effective for both balanced and unbalanced dc-links.

The unbalancing factor \(k\) is defined as follows to measure the unbalancing degree of capacitor voltages

\[
k = (V_P - V_N)/V_{dc}.
\]

where \(V_{dc}\), \(V_P\), and \(V_N\) are the total dc-link voltage, the upper and lower capacitor voltages on the dc-side, respectively. It follows from (1) and (3) that

\[
\begin{align*}
V_P &= 1 + k V_{dc} \\
V_N &= \frac{1 - k}{2} V_{dc}
\end{align*}
\]

The range of \(k\) can be obtained as

\[-1 < k < 1\]

since \(V_P\) and \(V_N\) are positive values. If \(k = 0\), \(V_P\) and \(V_N\) are equal, which is the case of balanced NP voltage. \(k\) is positive when \(V_P > V_N\) and negative when \(V_P < V_N\), both of which are unbalanced cases.

In these unbalanced cases, the MSVVDs with \(k > 0\) and \(k < 0\) are shown in Figs. 2(a) and 2(b), respectively. As can be seen from Fig. 2, the MSVVDs are quite different from the highly symmetrical space voltage vector diagram in balanced case, and become asymmetrical and considerably complicated.

The calculation formula of voltage vector is

\[
\bar{V}_{ref} = \frac{2}{3} \left( V_{AO} e^{2\pi j/3} + V_{BO} e^{4\pi j/3} + V_{CO} e^{6\pi j/3} \right),
\]

where \(V_{AO}\), \(V_{BO}\), and \(V_{CO}\) are a-, b-, and c-phase output voltages of the inverter, respectively. According to equation (6), the magnitudes of large vectors and zero vectors are \(2V_{dc}/3\) and 0, respectively, while the magnitudes of medium vectors and small vectors are variables related to the unbalancing factor \(k\). Table 2 shows the expressions of the basic vectors and the corresponding CMVs for three-level inverter under unbalanced dc-link condition.

It can be seen that the CMV amplitudes of the bolded basic voltage vectors in Table 2 is relatively high. When synthesizing the reference voltage vector, if these basic voltage vectors with high CMV amplitudes are avoided, and the unbalanced dc-links are taken into account, the three-phase sinusoidal output currents and the CMV suppression can be obtained simultaneously. The proposed modulation method is denoted as GLMZ-SVM method due to the adoption of large, medium, and zero vectors with low CMV amplitudes and its applicability for both balanced and unbalanced dc-links. Sector judgement, detailed duty cycle calculation, and switching sequence design will be given in this section. Sector 1 in Fig. 2 will be taken as a typical example of 12 sectors to illustrate the proposed strategy.

A. SECTOR JUDGEMENT

When the dc-links are unbalanced, a novel sector division method of MSVVD is presented which is shown in Fig. 2. As can be seen from Fig. 2, the MSVVD is divided into
The phase angle of the reference voltage vector $\vec{V}_{\text{ref}}$ is denoted by $\theta$. The angle $\alpha$ is given by the following equation according to the geometric characteristics of the MSVVD:

$$\alpha = \begin{cases} \frac{2\pi}{3} - \arcsin \frac{1}{\sqrt{1 + k^2/3}}, & k < 0; \\ \frac{1}{\sqrt{1 + k^2/3}} - \frac{\pi}{3}, & k \geq 0. \end{cases}$$

### B. DUTY CYCLE CALCULATION

Once the sector of the reference voltage vector $\vec{V}_{\text{ref}}$ is determined, the volt-second balance equation can be specifically obtained for different sectors. Accordingly, the respective duty cycles of large, medium, and zero vectors corresponding to each sector can be derived. For example, assuming that $\vec{V}_{\text{ref}}$ is located in Sector 1, it is synthesized by the nearest three vectors (NTV), i.e., the large vector $\vec{V}_{13}$ [PNN], the medium vector $\vec{V}_{7}$ [PON], and the zero vector $\vec{V}_{0}$ [OOO]. By the calculation formula (6) of voltage vector, $\vec{V}_{13}$, $\vec{V}_{7}$, and $\vec{V}_{0}$ can be expressed as

$$\begin{align*}
\vec{V}_{13} &= \frac{2}{3} V_{dc} \\
\vec{V}_{7} &= \frac{k + 3}{6} V_{dc} + j\frac{\sqrt{3}}{6} (1 - k) V_{dc} \\
\vec{V}_{0} &= 0
\end{align*}$$

The modified space vector diagram of the proposed method is shown in Figure 2. The modified space vector diagram of the proposed method. (a) $k < 0$. (b) $k > 0$.

### TABLE 2. Basic voltage vectors and corresponding CMVs of three-level inverter with unbalanced dc-links.

| Categories      | States | Locations | CMVs                         |
|-----------------|--------|-----------|------------------------------|
| Large vectors   | [PNN]  | $\frac{2}{3} V_{dc}$ | $(V_P - 2V_N)/3$            |
|                 | [PPN]  | $\frac{1}{3} V_{dc} + j\frac{\sqrt{3}}{3} V_{dc}$ | $(2V_P - V_N)/3$            |
|                 | [NPN]  | $\frac{1}{3} V_{dc} + j\frac{\sqrt{3}}{3} V_{dc}$ | $(V_P - 2V_N)/3$            |
|                 | [NPP]  | $-\frac{1}{3} V_{dc}$ | $(2V_P - V_N)/3$            |
|                 | [NPN]  | $-\frac{1}{3} V_{dc} - j\frac{\sqrt{3}}{3} V_{dc}$ | $(V_P - 2V_N)/3$            |
|                 | [PNP]  | $\frac{2}{3} V_{dc} - j\frac{\sqrt{3}}{3} (1 - k) V_{dc}$ | $(2V_P - V_N)/3$            |
| Medium vectors  | [PON]  | $\frac{1+k}{6} V_{dc}$ | $V_P/3$                     |
|                 | [OPN]  | $\frac{1+k}{6} V_{dc} + j\frac{\sqrt{3}}{6} (1 + k) V_{dc}$ | $2V_P/3$                    |
|                 | [NPO]  | $-\frac{1+k}{6} V_{dc} + j\frac{\sqrt{3}}{6} (1 + k) V_{dc}$ | $V_P/3$                     |
|                 | [OPP]  | $-\frac{1+k}{6} V_{dc}$ | $2V_P/3$                    |
|                 | [OOP]  | $-\frac{1+k}{6} V_{dc} - j\frac{\sqrt{3}}{6} (1 + k) V_{dc}$ | $V_P/3$                     |
|                 | [POP]  | $\frac{1+k}{6} V_{dc} - j\frac{\sqrt{3}}{6} (1 - k) V_{dc}$ | $2V_P/3$                    |
| P-type small vector | [ONN] | $\frac{1+k}{6} V_{dc}$ | $2V_N/3$                    |
|                 | [OON]  | $\frac{1+k}{6} V_{dc} + j\frac{\sqrt{3}}{6} (1 - k) V_{dc}$ | $-V_N/3$                    |
|                 | [NNO]  | $-\frac{1+k}{6} V_{dc} + j\frac{\sqrt{3}}{6} (1 - k) V_{dc}$ | $-2V_N/3$                   |
|                 | [NOO]  | $-\frac{1+k}{6} V_{dc}$ | $-V_N/3$                    |
|                 | [NNO]  | $-\frac{1+k}{6} V_{dc} - j\frac{\sqrt{3}}{6} (1 - k) V_{dc}$ | $-2V_N/3$                   |
|                 | [ONO]  | $-\frac{1+k}{6} V_{dc} - j\frac{\sqrt{3}}{6} (1 - k) V_{dc}$ | $-V_N/3$                    |
| N-type small vector | [PPP] | 0 | $V_P$                     |
|                 | [NNN]  | 0 | $-V_N$                     |
|                 | [OON]  | 0 | 0                         |

*Note: The judgement principle of the sector in which the reference voltage vector $\vec{V}_{\text{ref}}$ is located is as follows:

1) if $\theta \in [0, \alpha)$, $S = 1$;
2) if $\theta \in [\alpha, \pi/3)$, $S = 2$;
3) if $\theta \in [\pi/3, 2\pi/3 - \alpha)$, $S = 3$;
4) if $\theta \in [2\pi/3 - \alpha, 2\pi/3)$, $S = 4$;
5) if $\theta \in [2\pi/3, 2\pi/3 + \alpha)$, $S = 5$;
6) if $\theta \in [2\pi/3 + \alpha, \pi)$, $S = 6$;*

*Note: The judgement principle of the sector in which the reference voltage vector $\vec{V}_{\text{ref}}$ is located is as follows:

1) if $\theta \in [0, \alpha)$, $S = 1$;
2) if $\theta \in [\alpha, \pi/3)$, $S = 2$;
3) if $\theta \in [\pi/3, 2\pi/3 - \alpha)$, $S = 3$;
4) if $\theta \in [2\pi/3 - \alpha, 2\pi/3)$, $S = 4$;
5) if $\theta \in [2\pi/3, 2\pi/3 + \alpha)$, $S = 5$;
6) if $\theta \in [2\pi/3 + \alpha, \pi)$, $S = 6$;*

*Note: The judgement principle of the sector in which the reference voltage vector $\vec{V}_{\text{ref}}$ is located is as follows:

1) if $\theta \in [0, \alpha)$, $S = 1$;
2) if $\theta \in [\alpha, \pi/3)$, $S = 2$;
3) if $\theta \in [\pi/3, 2\pi/3 - \alpha)$, $S = 3$;
4) if $\theta \in [2\pi/3 - \alpha, 2\pi/3)$, $S = 4$;
5) if $\theta \in [2\pi/3, 2\pi/3 + \alpha)$, $S = 5$;
6) if $\theta \in [2\pi/3 + \alpha, \pi)$, $S = 6$;*
Define the modulation index $m$ as \[ m = \frac{\sqrt{3}|\overrightarrow{V}_{\text{ref}}|}{V_{dc}}. \] (9)

Since the maximum value of the amplitude of the reference voltage vector $\overrightarrow{V}_{\text{ref}}$ is $\sqrt{3}V_{dc}/3$, the maximum value of $m$ is 1.

It can be obtained by the modified volt-second balance principle based on the unbalancing factor in Sector 1 that

\[
\left\{ \begin{array}{l}
\overrightarrow{V}_{\text{ref}} = \overrightarrow{V}_{13}d_L + \overrightarrow{V}_{7}d_M + \overrightarrow{V}_0d_Z \\
d_L + d_M + d_Z = 1
\end{array} \right.
\] (10)

where $d_L$, $d_M$, and $d_Z$ are the duty cycles corresponding to the large, medium, and zero vectors.

From (8)-(10), the duty cycles $d_L$, $d_M$, and $d_Z$ can be calculated as

\[
\left\{ \begin{array}{l}
d_L = \frac{\sqrt{3}m \cos \theta + \frac{1}{2}k + \frac{3}{2}m \sin \theta}{2k - 1} \\
d_M = \frac{2m \sin \theta}{1 - k} \\
d_Z = 1 - d_L - d_M
\end{array} \right.
\] (11)

where $0 \leq \theta < \alpha$, and $k$ is the unbalancing factor of dc-links. Using the same method, the duty cycles of large, medium, and zero vectors for twelve sectors under unbalanced dc-link condition can be calculated in turn, as listed in Table 3.

### C. SWITCHING SEQUENCE DESIGN

In order to reduce harmonics and avoid switching losses between switching cycles, a symmetrical five-segment switching sequence is designed which starts and ends with zero vector. Taking Sector 1 as an example, the designed switching sequence is [OOO]-[PON]-[PNN]-[PON]-[OOO], as shown in Fig. 3, where Fig. 3(a) is the case for $k < 0$ and Fig. 3(b) is the case for $k > 0$. The overall control block diagram of the dual-input three-level inverter is illustrated in Fig. 4. The unbalancing factor $k$ is obtained by formula (3) to measure the unbalancing degree of the dc-links. The three-phase ac output currents are sampled and converted to dc components by abc/dq conversion, which are compared to the reference currents $i_{{*}d}$ and $i_{{*}q}$. The errors between the reference values and the actual values are then fed to the PI controllers to produce ac output voltages. The output variables of the controllers are taken as the input variables of the proposed modulation strategy.

In the modulation strategy proposed in this paper, the sector number can be obtained by the asymmetrical MSVVD in Fig. 2 and sector judgement principle. Then, according to the modified volt-second balance principle, the duty cycles of the large, medium, and zero voltage vectors in 12 sectors are calculated when the dc-links are unbalanced. Finally, reasonable switching sequences are determined in order to produce PWM signals to control the power switches of dual-input three-level inverter.
IV. SIMULATION RESULTS
To verify the effectiveness of the proposed scheme, simulation tests have been carried out using Matlab/Simulink. The parameters for simulations are summarized in Table 4, and three methods are used for comparison. Method-1 is the SVM method proposed in [27], whose reference voltage vector is always synthesized by the NTV. Method-2 is the conventional LMZ-SVM method for balanced dc-side capacitor voltages case. It uses large, medium, and zero vectors to synthesize the reference vector, which can solve the problems of CMV reduction and dc-link neutral point voltage balance at the same time [24]. Method-3 is the proposed GLMZ-SVM method. The reference currents in simulations are $i_d^* = 20$ A and $i_q^* = 0$ A.

A. SIMULATION RESULTS FOR NEGATIVE UNBALANCING FACTOR
Consider the case where the voltage difference across the upper and lower capacitors is $-60$ V, that is, $k = -0.19$. The simulation results of dc-side capacitor voltages, load currents, CMV, line voltage, and leakage current are presented in Fig. 5. Because the effect of small and medium vectors is taken into account in advance, and the reference voltage is always accurately synthesized by the NTV, Method-1 can obtain high-quality output currents and the total harmonic distortion (THD) of load currents is 1.79 %. However, Method-1 has the disadvantage of high CMV amplitude since all basic voltage vectors are adopted. As shown in Fig. 5(a), the range of CMV amplitude for Method-1 is $-126.7$ V to $83.3$ V. The CMV changes from $(-1 + k)V_{dc}/3$ to $(1 + k)V_{dc}/6$, or from $(-1 + k)V_{dc}/6$ to $(1 + k)V_{dc}/3$ in one period. In addition, the leakage current RMS is $0.31$ A, which does not meet the standard of less than $300$ mA specified by the German standard VDE-0126-1-1 [28]. When Method-2 is applied, since the unbalanced dc-links are not considered, the THD of load currents is 5.59 %, which does not satisfy the requirements of IEEE standard [29] of not more than 5 %. When Method-3 is used, the THD of load currents is reduced to 3.29 %, the minimum CMV amplitude is $-83.3$ V, and the maximum is $23.3$ V. It can be seen that the proposed method obtains three-phase sinusoidal currents and suppresses the CMV simultaneously when the dc-links are unbalanced.

B. SIMULATION RESULTS FOR POSITIVE UNBALANCING FACTOR
Consider the case where the difference between $V_P$ and $V_N$ is $60$ V, that is, $k = 0.19$. The simulation results of dc-side
capacitor voltages, load currents, CMV, line voltage, and leakage current are depicted in Fig. 6. When Method-1 is used, high-quality load currents can be obtained, but the CMV amplitude is high. The leakage current RMS for Method-1 exceeds 0.3 A, without satisfying the requirements of the VDE-0126-1-1 standard. Since Method-2 only considers the balanced dc-links, it is no longer applicable to the unbalanced dc-links. The THD of load currents is 5.56 %, which does not comply with the IEEE standard. When Method-3 is adopted, the THD of load currents is 3.30 % due to the comprehensive consideration of unbalanced dc-links and CMV suppression, which is greatly reduced to meet the IEEE standard compared to Method-2. At the same time, the CMV amplitude range is from −23.3 V to 83.3 V, which is reduced by half compared to Method-1. The leakage current RMS for Method-3 is reduced to 0.17 A, which meets the requirements of the VDE-0126-1-1 standard. In summary, the amplitude of CMV for Method-3 are much smaller than Method-1, and the load current waveforms is more outstanding than Method-2.

The CMV harmonic spectrum of three different methods is shown in Fig. 7. Because the proposed Method-3 only uses large, medium, and zero vectors to synthesize the reference voltage vector, the maximum peak value of CMV is reduced compared to Method-1. Therefore, as can be seen from Fig. 7, compared with Method-1, the attenuation of the CMV harmonic spectrum below the switching frequency is achieved by Method-3.

### V. EXPERIMENTAL RESULTS

Fig. 8 shows an experimental prototype platform constructed for a dual-input three-level inverter to test and verify the performance of the proposed method. The control scheme is carried out by the dSPACE 1005 digital control system and the DS5203 FPGA board. The experimental parameters are as shown in Table 4, which are the same as the simulation parameters.
A. EXPERIMENTAL RESULTS FOR NEGATIVE UNBALANCING FACTOR

For the case of $k < 0$, the experimental results of the dc-side capacitor voltages, CMV, line voltage, and load currents of the three methods are given in Fig. 9. The experimental waveform of leakage current is shown in Fig. 10. The experimental results are consistent with the simulation. The upper and lower capacitor voltages are 130 V and 190 V, respectively, that is $k = -0.19$. Table 5 shows the comparison of the output current THD of three methods for dual-input three-level inverter with different unbalancing degree $k$ on the dc-side. Method-1 takes the unbalanced NP voltage and the distribution of different type small vectors into account in advance, so the reference voltage is always accurately synthesized by the NTV. Therefore, Method-1 can achieve three-phase sinusoidal load currents, as can be seen from Fig. 9. But the CMV amplitude is very high, with a range...
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FIGURE 9. Experimental results of dc-side capacitor voltages, line voltage, CMV, and load currents for $k = -0.19$. (a) Method-1. (b) Method-2. (c) Method-3.

FIGURE 10. Experimental results of leakage current for $k = -0.19$. (a) Method-1. (b) Method-2. (c) Method-3.

of $(-1 + k)V_{dc}/3$ to $(1 + k)V_{dc}/3$, because of the use of all basic voltage vectors. In addition, the leakage current RMS of Method-1 is 0.32 A, which does not meet the standard of less than 300 mA specified by the German standard VDE-0126-1-1. Method-2 can reduce the CMV amplitude to within $(-1 + 3k)V_{dc}/6$. However, as the unbalanced dc-link condition is not considered, the load currents are distorted with THD of 5.89%, which does not satisfy the requirements of IEEE standard. Since the basic voltage vectors with low CMV amplitude are adopted, and the unbalanced dc-link condition is taken into consideration, Method-3 can achieve high-quality current output waveforms and effectively reduce the CMV simultaneously.

B. EXPERIMENTAL RESULTS FOR POSITIVE UNBALANCING FACTOR

For the case of $k > 0$, Fig. 11 exhibits the experimental results of the dc-side capacitor voltages, CMV, line voltage, and load currents for the three methods. The experimental waveform of leakage current is presented in Fig. 12. The difference between the upper and lower capacitor voltages is 60 V, that is $k = 0.19$. It can be seen from Figs. 11(a) and 11(c) and Table 5 that, when the dc-links are unbalanced, the load currents of Method-1 and Method-3 are both sinusoidal, with THD of 2.16% and 3.61%, respectively. The CMV amplitude of Method-1 varies from $(-1 + k)V_{dc}/3$ to $(1 + k)V_{dc}/3$, while that of Method-3 changes from $(-1 + 3k)V_{dc}/6$ to $(1 + 3k)V_{dc}/6$, which means that the CMV amplitude of Method-3 is reduced by half compared to Method-1. Furthermore, the leakage current RMS of Method-1 is 0.33 A, which does not comply with the German standard VDE-0126-1-1. It can
also be seen from Fig. 12 that the leakage current of Method-3 is greatly reduced, which conforms to the German standard VDE-0126-1-1. From the comparison of Figs. 11(b) and (c), it can be seen that the CMV amplitudes of Method-2 and Method-3 are both suppressed. However, when Method-2 is adopted, the load currents is severely distorted with THD of 5.85% since the reference voltage vector cannot be correctly synthesized by Method-2 in the case of unbalanced dc-links, while Method-3 still achieves highly sinusoidal load currents. This is a good indication that the proposed Method-3 can not only obtain excellent load currents, but also successfully reduce the CMV. The experimental results are in good agreement with the simulation results, which verifies the correctness of the theoretical analyses and the validity of the proposed strategy.

VI. CONCLUSION

For the dual-input three-level inverter system, in order to solve the two problems of CMV suppression and output current quality simultaneously when the upper and lower capacitor voltages on the dc-side are not equal, a generalized modulation method is proposed, which uses the large, medium, and zero vectors to synthesize the reference voltage vector. The MSVVD is obtained by using the unbalanced vector. The MSVVD is obtained by using the unbalanced factor calculated by the modified volt-second balance principle based on the unbalancing factor $k$, which has high asymmetry and complexity. A novel sector division method is given by medium and large vectors. The duty cycles of the basic vectors for 12 sectors are calculated by the modified volt-second balance principle based on the unbalancing factor $k$. A symmetrical five-segment switching sequence that starts and ends with zero vector is designed to reduce harmonics. Simulations and experiments verify the effectiveness of the proposed scheme. In addition, the proposed method is simple in principle and avoids additional hardware investment, which does not increase the burden on cost, size, and weight, so it is easy to implement in engineering.

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