Non-blocking programmable delay line with minimal dead time and tens of picoseconds jitter

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We report a non-blocking high-resolution digital delay line based on an asynchronous circuit design. Field programmable gate array logic primitives were used as a source of delay and optimally arranged using combinatorial optimization. This approach allows for an efficient trade-off of the resolution and a delay range together with minimized dead time operation. We demonstrate the method by implementing the delay line adjustable from 23 ns up to 1635 ns with a resolution of 10 ps. We present a detailed experimental characterization of the device focusing on thermal instability, timing jitter, and pulse spreading, which represent three main issues of the asynchronous design. We found a linear dependence of the delay on the temperature with the slope of 0.2 ps·K⁻¹ per a logic primitive. We measured the timing jitter of the delay to be in the range of 7 ps – 165 ps, linearly increasing over the dynamic range of the delay. We reduced the effect of pulse spreading by introducing pulse shrinking circuits, and reached the overall dead time of 4 ns – 22.5 ns within the dynamic range of the delay. The presented non-blocking delay line finds usage in applications where the dead time minimization is crucial, and tens of picoseconds excess jitter is acceptable, such as in many advanced photonic networks.

I. INTRODUCTION

Digital delay line (DDL) is essential tool in experimental physics research and engineering applications. DDLs represent core building blocks in nuclear physics instrumentation, laser synchronization, and photonic networks, where a target delay ranges from nanoseconds to microseconds with sub-nanosecond precision. Tunable delays up to a few microseconds are often needed in correlation measurements of cascade decays. Electronic delays with tens of picoseconds resolution and dynamic range of hundreds nanoseconds are necessary to compensate for the length fluctuations of optical communication channels. DDLs are frequently utilized in photonic quantum technology for photon coincidence detection and switching. These applications require synchronization of several single-photon detectors and active components, like modulators or switches. Delays from tens to hundreds of nanoseconds are needed with precision of tens or hundreds of picoseconds, which corresponds to timing jitter of photonic detectors. Single-photon avalanche diodes may serve as an example of frequently used photonic detectors with 50–300 ps jitter and 10–50 ns dead time (typical values). DDLs should have comparable or lower jitter and dead time to be efficiently combined with these detectors.

DDLs are generally divided into two main groups: blocking and non-blocking. The blocking design typically utilizes system clock as a time reference, counts of which determine the amount of introduced delay between input and output signal. Resolution of this method is constrained to the clock period, however, various sub-clock techniques allow to go beyond the basic clock resolution, e.g. multiple clock signals with introduced relative phase shift or Vernier delay lines. The main disadvantage of this approach is a dead time of the delay line which can be understood as a time of inability to react or process any input signal due to processing of the previous input. This effect occurs naturally due to the usage of the reference clock, and has a value equal to the introduced delay $n \cdot T_{clk}$, where $n$ is the number of time intervals and $T_{clk}$ is the period of reference clock respectively. The dead time reduces DDL throughput and affects statistics of the signal, which significantly limits applications of blocking DDLs in quantum technology.

The non-blocking design typically exploits inevitable intrinsic fixed delay of electronic components or primitives used in construction. One of the most used circuit designs here is so-called tapped delay line, where components are connected serially. Consequently, the signal is extracted from output of the corresponding tap and thus with certain amount of propagation delay. Tapped delay lines typically produce short delays and are often used in combination with synchronous delays.

Traditional platforms used for DDLs are discrete components and microcontroller units. Although, field programmable gate arrays (FPGAs) are becoming more and more utilized in the area of digital delay generators. The main disadvantage of using discrete components is their limited tunability without intervention at hardware level. Microcontrollers offer programability and a wide range of the generated delays up to hundreds of seconds, and granularity in order of tens of nanoseconds. However, they are clock-based, i.e. dead-time limited, and not convenient for sub-nanosecond delay generation. FPGAs offer unique reprogramming flexibility, multi-channel usage and easy implementation of synchronous

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D. delay line provides a programmable delay up to 1.6 \( \mu s \) with the adopted asynchronous design. The developed delay and pulse dispersion as these parameters are crucial for measurement of its temperature dependence, timing jitter, as well as asynchronous structures in the designs. Many custom-built DDLs were demonstrated exploiting combinations of discrete components and FPGA, but recently FPGA-based solutions with both wide dynamic range and fine granularity have been reported. We carefully characterize the performance of the presented device. Particularly, we present the measurement of its temperature dependence, timing jitter, and pulse dispersion as these parameters are crucial for the adopted asynchronous design. The developed delay line provides a programmable delay up to 1.6 \( \mu s \) with the resolution of 10 ps and the maximum dead time of 22.5 ns. In envisioned applications, where high-rate randomly arriving signals from optical or particle detectors are delayed, it provides minimal excess dead time and features timing jitter lower or comparable to commonly used detectors.

II. DESIGN

Our aim is to utilize logic primitives of the FPGA to construct a delay line in such a way that it will guarantee both wide dynamic range and high resolution. The delay line is designed as a sequence of serially connected 24 stages. Each stage contains a delay introducing element and a switching element, which enables to switch between delay stages and thus to chose the desired delay value. In our case, the delay introducing element is an array of LUTs and the switching element is 2-to-1 multiplexer (see Fig. 1a). The route in each stage splits into two, one delaying the input signal, the other propagating the signal with just an intrinsic delay of the multiplexer (zero-delay path). The intrinsic delays contribute to the minimum delay that can be reached by the delay line when all stages are set to zero-delay path. To provide fine granularity for shorter delays, each pair of the first 10 stages is designed to have the same number of LUTs (i.e. 1, 1, 2, 2, ..., 5, 5), since the FPGA manufacturing deals with physical parameters variation and each LUT may have slightly different propagation delay. The number of LUTs in the remaining 14 stages forms a geometric series with geometric factor of approximately 1.6 except for the last stage, in which the number of LUTs was limited to 1729 by the maximum available LUTs of the employed FPGA.

Delays introduced by the individual stages are measured during the calibration of the DDL by the same method used for characterization of the whole device as described in Section IV. The measured values compose a \( 1 \times 24 \) vector \((\tau_0, \ldots, \tau_{23})\). We calculate delays of all possible \( 2^{24} \) stage combinations as a matrix product of the measured values and \( 24 \times 24 \) stage combinations binary matrix:

\[
\begin{pmatrix}
\tau_0 & \ldots & \tau_{23}
\end{pmatrix}
\begin{pmatrix}
0 & 1 & 0 & \cdots & 1 \\
0 & 0 & 1 & \cdots & 1 \\
\vdots & \vdots & \vdots & \ddots & \vdots \\
0 & 0 & 0 & \cdots & 1
\end{pmatrix}
= \begin{pmatrix}
\tau_0 & \ldots & \tau_0 + \cdots + \tau_{23}
\end{pmatrix}
\]

Sorting the obtained vector of variations in ascending order, taking differences of each pair of its values i.e. \( \Delta \tau_n = \tau_{n+1} - \tau_n \) and performing a selection, the vector of delay step values with target granularity can be distilled. The selection algorithm represents a simple linear search through the array of differences \( \Delta \tau \) with a condition which matches the target granularity value. As a result, \( 160 \times 10^3 \) matched delay values with granularity 10 \( \pm 5 \) ps and corresponding binary control words are loaded in the DDL to generate a required delay value. The key point of the proposed design is a tunable trade-off between high dynamic range and fine granularity. Although we picked such values that satisfy requirements of our experiment, i.e. the delay range from 23 ns to 1635 ns and granularity 10 ps, one can modify the design according to one’s needs.

Propagating through a sequence of LUTs results in non-negligible dispersion, which will be discussed in Section IV. The pulse dispersion causes spreading of the propagating pulses, and may negatively affect effective dead time of the DDL, i.e. two pulses with a small temporal separation might not be resolved at the output of

Figure 1: a) Scheme of the presented delay line: individual constituent delay blocks \( \tau_n \) are switched by multiplexers (MUXs) to match optimally the target delay. Pulse shrinking circuits (PSCs) are employed to reduce pulse dispersion, see text for details. b) Photo of the developed device.
III. IMPLEMENTATION

The developed DDL was implemented in Cyclone IV EP4CE6E22C6N FPGA from Altera on a custom-built electronic board. Digital circuit was designed by means of VHDL using the Intel Quartus Prime Lite edition software. Communication of the device with PC via USB to serial converter is performed by STM32F334K8 microcontroller. It also stores selected control words in AT25SF161 16Mbit FLASH memory and controls other parts of the board including the DDL. Input analog signal is converted to digital by LTC6754 fast LVDS comparator to match the FPGA input. The delayed output from FPGA is shifted by SN74LVC4245A voltage level shifter to +5 V level to be compatible with other laboratory devices. Current operation mode is single-channel with straightforward multi-channel extension possibility.

Input signal is connected to the board via SMA connector and is terminated with 50 Ohm. Maximum allowed input voltage ranges from -0.2 V to +5.1 V. However, range from 0 V to +3.3 V is recommended because comparator threshold can be set in this range by the 12-bit digital-to-analog converter which is incorporated in the microcontroller. The comparator contributes to zero-delay path with maximally 1.6 ns considering sufficient overdrive higher than 115 mV\(^2\). The LVDS signal from comparator is received by FPGA and goes through digital delay line described in Section II.

Multiplexers of the DDL are directly controlled by the FPGA-implemented 24-bit shift register, which is loaded externally by the microcontroller with the specified control word. When the signal passes the zero-delay path, it goes through 25 LUTs (input PSC 1 LUT, multiplexers in all stages 24 LUTs), LVDS input buffer, and output buffer. This propagation delay through FPGA is the most significant part of the zero-delay path (ca. 14-16 ns). The average delay per LUT in individual stages, which were measured during calibration, appeared to be dependent on number of LUTs used in the stage. For lower number of LUTs less than 10 the average delay per LUT varies within the range of 350±250 ps per LUT. For larger delay stages (100 LUTs and more) this value converged to 270 ps per LUT. This can be the consequence of that the signal routing and LUTs placement in FPGA was not optimized by any special Quartus Prime tool, e.g. LogicLock, during compilation. Moreover, LUT propagation delay also depends on CMOS process parameters variation. However, the described phenomenon is beneficial in our case because broader set of different values inputs the combinatorial optimization and thus wider range of delays with fine granularity is covered.

A width of the output pulse varies from 4.9 ns to 42.5 ns and depends on input pulse width and provided delay. First PSC contains 15 LUTs and shrinks the pulse to the length of 4.3 ns corresponding to the delay introduced by these LUTs unless the width of the input pulse is shorter. Other PSCs contain only 4 LUTs and shrink the pulse to approximately 1 ns and are implemented before the last five (the largest) stages. When the signal passes only through the stages without PSCs the dead time increases linearly. If one of the last five stages with PSCs is used the dead time is a constant value which is given by the number of LUTs in the corresponding delay element. FPGA output buffer provides pulses of +3.3V level which are converted by level shifter to +5V level. Level shifting contributes to zero-delay path with constant propagation delay which is between 1 ns to maximum of 6.7 ns in dependence on the load capacity. Output of the board is terminated by 50 Ohm resistor in series and lead out through SMA connector.

IV. TEMPORAL PERFORMANCE OF THE DELAY LINE

We characterized the following parameters of the developed DDL: linearity, granularity, jitter, and dead time. All measurements were performed using Lecroy 806Zi-B oscilloscope with a 6 GHz signal bandwidth and 40 GS/s sample rate in real-time mode. At least $5 \times 10^3$ samples were collected for each parameter measurement. Test pulses were generated by 240 MHz arbitrary waveform generator (Tektronix AFG3252) or 2 GHz clock generator (CG635 from Stanford Research) depending on the requirements of the particular measurement. To eliminate inter-channel jitter of the source, its output was split into two parts: one output was used as a signal pulse input for the delay generator, other one served as a reference for oscilloscope. Length of cables were selected, so that relative delay between reference pulse and signal pulse was zero.

We directly measured the zero delay introduced by the device to be 18.808 ns for ambient temperature of 21.5 ± 0.2°C. Also, we performed the calibration of the DDL by measuring the delay of the individual stages resulting in the vector $[\tau_0, \ldots, \tau_{23}]$. In order to verify linearity of the DDL, we measured an actual delay introduced by the DDL when the corresponding target delay was set. We performed this measurement for 20 points uniformly distributed in log-scale, see Fig. 2 (a). The results show linear dependence with unity slope. The upper limit of the generated delay has a value of 1635...
ns. Furthermore, we explored three particular ranges of the DDL output denoted by blue markers in Fig. 2(a) and compared the measured data with the linear fit, see Fig. 2(b). Small deviations from the perfect linear behavior visible in Fig. 2(b) are smaller than temporal jitter and will be discussed in the rest of this section.

Having measured the delay values in the three different regions of a full range of the DDL, we evaluated the differences of the measured consecutive delays to access the granularity, see Fig. 2(c). The target granularity of 10(±5) ps is shown as dashed red lines. The measured granularity fluctuates beyond the target region but it remains within ±100 ps even for the largest delays. We offer several possible explanations of this effect. The main reason is the limited precision of the delay stages calibration caused by temporal jitter of the employed oscilloscope; the details are provided below. Furthermore, it is known that FPGAs are sensitive to process, voltage and temperature variations (PVT). Temperature undoubtedly affects DDL performance, see Section V for the details. The temperature was kept stable within 1 deg during linearity and granularity measurements. FPGAs timing characteristics are influenced also by fluctuations of supply voltage. However, this effect can be neglected because voltage stabilizers were used to ensure sufficiently stable voltage with common laboratory power supply.

To measure the jitter, we utilize the same setup as for the linearity measurement. Instead of the mean value of the measured delay, the standard deviation of the delay (at 50% signal level) was measured using statistical functions of the oscilloscope. The output jitter shows linear dependence on the delay; estimation from the data reads $\sigma_j[ps] = 4.726 + 0.098\tau$, where $\sigma_j$ is the jitter and $\tau$ is the delay in nanoseconds, see Fig. 3(a). The jitter grows linearly with the delay from 7 ps to 165 ps across the delay range, and causes uncertainty of the linearity measurement. Instead of the mean value the granularity fluctuations are smaller than the temporal jitter.

The oscilloscope sample rate of 40 GS/s, equivalent to 25 ps per sample, limits the precision of the performed temporal characterization. The repeated measurements and their statistical processing allow to go beyond the sampling resolution. The inter-channel jitter of the oscilloscope at the level of 20 picoseconds seems to be the ultimate limitation of the precision of our characterization. Furthermore, the calibration precision is also affected, which can explain the observed fluctuations of the DDL granularity. Considering that the calibration errors of 24 stages are independent with the standard deviation $\delta = 20$ ps, the overall standard deviation of the maximum delay reaches $\sqrt{24}\delta$. The peak-to-peak value uncertainty goes up to $6\sqrt{24}\delta = 588$ ps, which is larger than the observed fluctuation of the granularity.

By measuring the pulse width at the output of a FPGA delay line without PSCs we characterized the pulse spreading to be approximately 25 ps/LUT on average. However, due to inability to precisely predict the amount of pulse shrinking performed by PSCs, the overall dead time of the DDL caused by the pulse spreading cannot be computed easily. Instead, we performed a measurement of the maximum repetition frequency, which is transmitted through the DDL. The input square signal is provided by the clock generator. We used a counter (with 2.2 ns pulse-pair resolutions) to acquire the number of pulses at the output, and increased the repetition frequency of the input signal to the level when the output count rate is decreased to 95% of the corresponding input repetition rate. Beyond this maximum frequency, the pulses of the input signal are spread to the whole period of the signal, and cannot be distinguished properly. The dead time of the DDL is defined as half of the period at the maximum frequency, see Fig. 3(b). The minimum measured dead time of the DDL is 4 ns; it is mainly due to the maximum input frequency of the used counter and propagation delay of the level shifter. The maximum dead time does not exceed 22.5 ns, i.e. 1.4% of the maximum delay of the DDL.

V. THERMAL STABILITY AND CALIBRATION

To measure the performance of the developed DDL under varying thermal conditions, a box from thermoinsulating material (Styrofoam) was built. Temperature in the box was monitored by a certified thermometer with the precision of 0.15 deg. Each individual delay stage of the device was examined for thermal dependence in range from 30°C to 60°C with increment of 5°C. A weak linear dependence of the delay on temperature was revealed and will be discussed below.

To verify the linear scaling of the delay time with the temperature, we calculated a delay-temperature coefficient defined as:

$$\beta = \frac{\tau_{\text{max}} - \tau_{\text{min}}}{(T_{\text{max}} - T_{\text{min}}) \cdot N}$$

where $N$ is the number of LUTs used for the delay in each stage; $\tau_{\text{max}}$ and $\tau_{\text{min}}$ are the delay values corresponding to the maximum and minimum temperatures $T_{\text{max}}$ and $T_{\text{min}}$, respectively. Hence $\beta$ represents an average delay increase per Kelvin and a single LUT. In Fig. 3(c) evolution of the $\beta$ over the LUT number can be seen. The values of $\beta$ obtained for small LUT numbers posses low confidence due to the measurement systematic errors. However, for larger number of LUTs, $\beta$ converges to its mean value of 0.2 ps · K$^{-1}$ per LUT. Having calculated $\beta$ one can upload its values into FPGA memory and perform real-time calibration of the delay generator configuration for the particular ambient temperature.

Furthermore, we characterize the temporal dependence of time jitter of the individual delay stages, see Fig. 3(d). The measurement shows no significant changes in the jitter over 30°C.
VI. POSSIBLE IMPROVEMENTS AND EXTENSIONS

The issues of the reported delay generator are mainly the delay dependence on temperature, jitter and dead-time being functions of the delay. Here we propose how these characteristics can be improved.

Temperature stabilization of the whole device may significantly decrease delay dependence on temperature, although the proposed thermal calibration can solve this issue. Input voltage comparators, due to their thermal dependence are also contributing to overall DDL temperature dependence. 

Utilizing latest generation FPGAs with finer CMOS/FET nm technologies may greatly contribute to the DDLs timing performance, mainly improving resolution and jitter characteristics. On the other hand, the reported device performance was primarily limited by our measurement setup precision.

To minimize the zero delay introduced by the DDL, special tools can be used during synthesis stage (Quartus LogicLock), allowing manual placement of the particular LUT blocks, placing them in the particular area of the FPGA chip as close to each other as possible, therefore minimizing propagation delay between individual blocks.

VII. CONCLUSION

We report the novel design and implementation of the digital delay line based on non-blocking asynchronous circuit design. The digital circuitry was realized using FPGA logic primitives (LUTs) chained up into array blocks to form the set of corresponding delay stages. Calibration of these stages and selecting the optimum variations allow to cover a large range of output delays with fine granularity. The presented device was built on custom board using Cyclone IV EP4CE6E22C6N FPGA.

We also implemented pulse shrinking circuits to reduce negative effects of pulse dispersion. Furthermore, we performed a detailed experimental characterization of the delay line. The obtained dynamic range of the generated delay reaches from 23 ns to 1635 ns. The target design granularity was 10±5 ps. The measured granularity deviates from the target range by tens of picoseconds, which is smaller than temporal jitter. We characterized the jitter dependence on the delay to be $\sigma_{\tau} = 4.726 + 0.098 \tau$, where $\sigma_{\tau}$ is the jitter and $\tau$ is the delay in nanoseconds. This corresponds to the jitter from 7 ps to 165 ps within the dynamical range of the device. We measured the device sensitivity to ambient temperature and estimated the delay-temperature coefficient $\beta = 0.2$ ps · K$^{-1}$ per LUT. The developed delay line features dead time, which is a negligible fraction of the output delay. Particularly, the total dead time is 22.5 ns for the maximum delay of 1635 ns. This corresponds to frequency bandwidth of 20 MHz or larger within the dynamic range of the digital delay line, which is sufficient for delaying signals generated by majority of single-photon detectors. Despite the fact that FPGAs are typically not recommended for asynchronous methods in precise timing applications, we believe that this work will facilitate the development of digital delay lines utilizing non-blocking asynchronous design.

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DATA AVAILABILITY

The data that support the findings of this study are openly available in GitHub repository.

REFERENCES

1. J. Marques and C. Cruz, Nucl. Instrum. Methods Phys. Res. A 745, 50 (2014).
2. L. Słotwinyński, P. Krešík, L. Buczak, and M. Lipiński, IEEE Trans. Instrum. Meas. 60, 1480 (2011).
3. A. Boaron, B. Korzh, R. Houlmann, G. Boso, D. Rusca, S. Gray, M.-J. Li, D. Nolan, A. Martin, and H. Zhinden, Appl. Phys. Lett. 112, 171108 (2018).
4. F. Flamini, N. Spagnolo, and F. Sciarra, Rep. Prog. Phys. 82, 016001 (2019).
5. S. Shussarenko and G. J. Pryde, Appl. Phys. Rev. 6, 041303 (2019).
6. C. Zhang, W. Li, Y. Hu, T. Yang, G. Jin, and X. Jiang, Rev. Sci. Instrum. 87, 113107 (2016).
7. J. Hloušek, M. Dudka, I. Straka, and M. Ježek, Phys. Rev. Lett. 123, 153604 (2019).
8. E. Arabul, S. Paesani, S. Tancock, J. Rarity, and N. Dahmoun, IEEE Photon. J. 12, 1 (2020).
9. G. J. Mendoza, R. Santagati, J. Munns, E. Hemsley, M. Piekarek, E. Martín-López, G. D. Marshall, D. Bonneau, M. G. Thompson, and J. L. O’Brien, Optica 3, 127 (2016).
10. C. Xiong, X. Zhang, Z. Liu, M. J. Collins, A. Mahendra, L. G. Helt, M. J. Steel, D. Y. Choi, C. J. Chae, P. H. W. Leong, and B. J. Eggleton, Nat. Commun. 7 (2016).
11. F. Kaneda and P. G. Kwiat, Sci. Adv. 5, eaaw8586 (2019).
12. V. Svarc, J. Hloušek, M. Nováková, J. Fiurášek, and M. Ježek, Opt. Express 28, 11634 (2020).
13. P. Dudek, S. Szczepański, and J. Hatfield, IEEE J. Solid-State Circuits 35, 240–247 (2000).
14. K. Cui, X. Li, and R. Zhu, Rev. Sci. Instrum. 88, 064703 (2017).
15. G. Béard, Proc. Phys. Soc. 90, 131 (1967).
16. J. Straka, J. Grygar, J. Hloušek, and M. Ježek, J. Light. Technol. 38, 4765 (2020).
17. H. U. Jang, J. Bieleck, G. Veshapidez, M. L. Trachy, and B. D. DePaola, Rev. Sci. Instrum. 78, 094702 (2007).
18. A. T. Handa, T. Domalain, and K. Kose, Rev. Sci. Instrum. 78, 084705 (2007).
19. E. E. Eyler, Rev. Sci. Instrum. 82, 013105 (2011).
20 R. Hošák and M. Ježek, Rev. Sci. Instrum. 89, 045103 (2018).
21 Y. Song, H. Liang, L. Zhou, J. Du, J. Ma, and Z. Yue, in 2011 International Conference on Electronics, Communications and Control (ICECC) (2011) pp. 2116–2118.
22 K. Perko and R. Szplet, Meas. Autom. Monit. 61, 311 (2015).
23 S. Berrima, Y. Blaqui`ere, and Y. Savaria, in 2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS) (2017) pp. 918–921.
24 W.-Z. Zhang, X. Qin, L. Wang, Y. Tong, Y. Rui, X. Rong, and J.-F. Du, Rev. Sci. Instrum. 90, 114702 (2019).
25 High Speed Rail-to-Rail Input Comparator with LVDS Compati-
26 ble Outputs, Analog Devices (2015).
26 Octal Bus Transceiver and 3.3V to 5V Shifter With 3-State Out-
26 puts, Texas Instruments (2015).
27 H. Xia, G. Cao, and N. Dong, Rev. Sci. Instrum. 90, 044706 (2019).
28 G. Mazin, https://github.com/glebmmazin/delayline Non-
29 blocking programmable delay line – GitHub repository (2021).
Figure 2: Linearity and granularity of the reported digital delay line. Panel (a) represents full dynamic range; panel (b) shows three particular time ranges to verify the linearity at the fine scale; red solid line stands for linear fit; panel (c) visualizes the granularity computed from the measured data shown in the panel (b). Red dashed lines represent the target granularity range of $10 \pm 5$ ps. Gray area shows 99.7% confidence interval of the delay jitter.

Figure 3: (a) Jitter dependence on the output delay. (b) Measured dead time of the delay line. Dead time grows linearly with the output delay up to value of $2 \times 10^2$ ns. The stepwise behaviour of the remaining part of the curve is a direct consequence of pulse shrinking circuits. (c) Delay-temperature coefficient evolution over LUT number. (d) Jitter temperature dependence for all 24 stages (each line corresponds to individual stage).