Characterization of intrinsic subgap density-of-states in exfoliated MoS$_2$ FETs using a multi-frequency capacitance-conductance technique

Hagyoul Bae, Choong-Ki Kim, and Yang-Kyu Choi
School of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon 34141, South Korea
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A multi-frequency capacitance-conductance technique is proposed for characterizing the intrinsic density-of-states ($g_{\text{int}}(E)$) inside an energy bandgap range ($E_V < E < E_C$) by de-embedding the structure-dependent parameters such as parasitic capacitance and resistance in a fabricated exfoliated molybdenum disulfide (MoS$_2$) field effect transistor (EM-FET). The proposed technique uses the measured frequency-dispersive capacitance ($C_m$) and conductance ($G_m=1/R_m=\omega C_m D_m$) data with the measured dissipation factor $D_m(G_m/\omega C_m)$ at a frequency range of 0.3 kHz to 10 kHz. To extract $g_{\text{int}}(E)$, an equivalent circuit model of the MoS$_2$ FET converted from a two-element model for the parallel-mode ($C_m$-$D_m$) measurement was developed with this technique. © 2017 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).

A two-dimensional (2D) material-based MoS$_2$ field-effect transistor (FET) is known to be a prospective device for possible application in opto-electronic devices, non-volatile memory devices, etc., because of its high luminescence efficiency, high current capability, good transport properties and wide direct bandgap. In particular, with the aid of an exfoliation method, the exfoliated molybdenum disulfide FET (EM-FET) can be fabricated as a single crystal which exhibits high electron mobility ($\mu_e$). Among the electrical characteristics of the EM-FET, the inherent density-of-states (DOS: $g(E)$) of MoS$_2$ between the valence band maximum ($E_V$) and the conduction band minimum ($E_C$) is a critical parameter for estimating the stability and reliability of the EM-FET accompanied with the effect of process conditions and long-term operation, etc. Consequently, the experimental modeling and characterization of $g(E)$ in the MoS$_2$ FET is important to stabilize the device performance. Although the MoS$_2$ FET has been well explored in terms of material properties, electrical performances, and structural advancement, there are only a few studies that have quantitatively investigated the trap distribution. Up to date, a useful and robust technique for extracting the intrinsic $g(E)$ (simply $g_{\text{int}}(E)$) of the MoS$_2$ layer based on experimental capacitance-conductance ($C_m$-$G_m$) measurements with excluding parasitic components, has not been reported yet.

In this work, an extraction technique to estimate $g_{\text{int}}(E)$ from a fabricated EM-FET is proposed by using multi-frequency conductance-voltage measurements after de-embedding parasitic overlap capacitances and contact resistance at the source and drain (S/D). In an equivalent circuit model of the MoS$_2$ channel, conductance is affected by a loss mechanism resulting from the capture and emission of carriers in bulk trap states. The behavior of charges excited from the bulk traps allows us to experimentally extract the energy distribution of $g_{\text{int}}(E)$ in the MoS$_2$ channel. Note that the proposed technique can also be used for the quantitative analysis of $g_{\text{int}}(E)$ in other 2D-material based FETs.

The EM-FET was fabricated by transferring multi-layered MoS$_2$ flakes (4 layers) onto a gate oxide of 90 nm, which was thermally grown on a p$^+$ Si wafer. The p$^+$ Si wafer serves as a back gate (G).
In order to make the S/D contacts, 10 nm of Ti and 100 nm of Au were sequentially deposited after patterning the S/D areas using conventional photo-lithography. Afterwards, the S/D pads were defined through lift-off of the Ti/Au layers. Afterwards, the S/D pads were defined through lift-off of the Ti/Au layers. After channel and S/D formation, the EM-FET was encapsulated with a passivation layer (Al₂O₃=50 nm) and treated with high vacuum annealing (HVA) to protect it from external contaminants, and to remove pre-existing water molecules on the MoS₂ flakes.

The physical thickness of exfoliated MoS₂ flake film was measured by atomic force microscopy (AFM) and Raman spectroscopy as shown in Figs. 1(a) and (b), respectively. As number of MoS₂ layers increase, the in-plane mode at ~383 cm⁻¹ shifts to lower frequencies and the out-of-plane mode ~408 cm⁻¹ shifts to higher frequencies. The number of MoS₂ layers can be found by measuring the distance between two frequency peaks at 383 cm⁻¹ and 407 cm⁻¹ in bulk MoS₂. Thus, the frequency difference between the E₂g¹ and A₁g peaks is 24 cm⁻¹. Then, the MoS₂ flake thickness is approximately 2.7 nm, showing 4 layers.

Fig. 2(a) shows a schematic view of the fabricated EM-FET with the bottom gate structure and the multi-layered MoS₂ channel. Fig. 2(b) illustrates the energy band diagram along the MoS₂ channel depth direction. In the energy band diagram, free charges are excited from localized trap states in the MoS₂ channel by a change of frequency (f) and gate voltage (V GS). Fig. 2(c) shows the whole conversion procedure for extraction of Ctrap in the EM-FET. As shown in (i) of the Fig. 2(c), parallel Cm-Dm is measured by HP agilent E4980A precision LCR meter. After that, we can obtain the Gm and convert to (ii) of the Fig. 2(c), which is a simplified circuit of (iii) of the Fig. 2(c). (iii) of the Fig. 2(c) indicates the equivalent circuit model with bulk trap time constant τtrap=Rtrap Ctrap. In the (iii) of the Fig. 2(c), Ctrap is the capacitance for the V GS-responsive localized charges (Qtrap) over the subgap states and the equivalent resistance Rtrap is for the retardation of charges. The Cm-Dm model obtained from the measured Cm-Dm model can be converted into parallel capacitance (Cp) and parallel conductance (Gp). Finally, Cp-Gp was converted into Ctrap and Rtrap where Ctrap and Rtrap are physical parameters related to the capture and emission of carriers by localized traps, in parallel with the MoS₂ channel capacitance (Cs).

In the measured Cm-Gm curves between the G and S pad, the calculated pad capacitance (Cs-pad) was inevitably included as overlap capacitance. The intrinsic capacitance (Cm-int) calculated from the measured C-V data. Then, the Cm-int without the Cs-pad in the G-to-S configuration can be obtained from

\[ C_{m-int} = C_m - C_{s-pad} \]

As described in Eq. (1), the Cs-pad results in an overestimated gint(E) due to the unavoidable overlap region at the G and S pad. Therefore, the Cm-int needs to be considered to accurately extract gint(E). As shown in Fig. 2(c), the measured Cm-Gm is matched with a physics-based circuit model after de-embedding contact resistance, as below

\[ C_p = C_s + \frac{C_{trap}}{1 + (\omega \tau_{trap})^2} \]

FIG. 1. (a) Physical thickness of the MoS₂ flake measured by AFM. (b) The intensity of the MoS₂ flake in response to a 514 nm wavelength laser in Raman spectroscopy.
FIG. 2. (a) Schematic view of the EM FET. (a) Cross-sectional view of the EM-FET. (b) Energy band diagram along the depth direction of the MoS$_2$ channel. (c) Equivalent circuit model: two-element model for the parallel mode $C_m$-$G_m$ configuration, simplified three element model for the oxide capacitance ($C_{ox}$) including parallel capacitance ($C_p$) and conductance ($G_p$), physics-based four-element model with MoS$_2$ channel capacitance ($C_s$) in parallel with trap capacitance ($C_{trap}$) and trap resistance ($R_{trap}$) for $f$- and $V_{GS}$-dependent $C_m$-$G_m$ characteristics in the EM-FET.

$$\frac{G_p}{\omega} = \frac{\omega G_{m-int} C_{ox}^2}{G_{m-int}^2 + \omega^2 (C_{ox} - C_{m-int})^2} = \frac{q \omega \tau_{trap} D_{trap}}{1 + \left(\frac{\omega \tau_{trap}}{G_p q}\right)^2} \cdot \text{s}$$  \hspace{1cm} (3)

with $\omega=2\pi f$, the time constant $\tau_{trap}=R_{trap} \times C_{trap}$, intrinsic conductance $G_{m-int}$, and density of states $D_{trap}=C_{trap}/q^2$. In Eq. (3), the calculated $G_p/\omega$ has a maximum value at $\omega=1/\tau_{trap}$. Therefore, $D_{trap} (=2G_p/q\omega)$ is obtained from the maximum $G_p/\omega$ at the peak value in the $G_p/\omega$ versus $\omega$ plot as follows:

$$C_{trap} = 2 \times \frac{G_p}{\omega},$$  \hspace{1cm} (4)

$$D_{trap} = g_{int}(E) = \frac{dQ_{trap}(E)/dE}{(W \times L \times T_{MoS2})} = \frac{(dQ_{trap}(E)/dV_{GS})}{(W \times L \times T_{MoS2}) \times q} = \frac{C_{trap}}{(W \times L \times T_{MoS2}) \times q} \text{ [cm}^{-3} \cdot \text{eV}^{-1}].$$  \hspace{1cm} (5)

with the capacitance for the $V_{GS}$- and $f$-responsive trapped localized charges ($Q_{trap}$) inside the energy bandgap, the channel width ($W$), the channel length ($L$), the thickness of the MoS$_2$ ($T_{MoS2}$), and $q=1.6 \times 10^{-19}$ [C]. In order to characterize the energy distribution of the $g_{int}(E)$, the nonlinear relation between the surface potential ($\psi_s$) corresponding to $V_{GS}$ and a specific trap energy level can be obtained from the $C$-$V$ curve through

$$\psi_s = \int_{V_{FB}}^{V_{GS}} \left(1 - \frac{C_{m-int}}{C_{ox}}\right) dV_{GS}[\text{eV}].$$  \hspace{1cm} (6)

In order to analyze the $g_{int}(E)$ in the MoS$_2$ channel, an EM-FET was fabricated with the calculated dimensions: $W = 5 \mu$m, $L=5 \mu$m, and $T_{MoS2}=2.5$ nm (4 layers). Fig. 3 shows the measured $C$-$V$ characteristics ($C_m$ and $G_m$) with frequency-dispersive phenomena over the $f$ range from 0.3 to 5 kHz and $V_{GS}$ range from -5 to 35 V. The measured dissipation factor $D_m (=G_m/\omega C_m)^{1/2}$ is defined
as the ratio of the equivalent series resistance (ESR) and capacitive reactance. The inset shows an optical photograph of the fabricated EM-FET including the measurement configuration. The $G_p/\omega$ vs. $\omega$ plot is represented in Fig. 4. The calculated value of $D_{\text{trap}} = 2G_p/\omega q$ can be obtained from the maximum value of $G_p/\omega$. Therefore $g_{\text{int}}(E) = D_{\text{trap}}$ is extracted from the maximum $G_p/\omega$ through Eqs. (4) and (5).

As shown in Fig. 3, the $f$- and $V_{\text{GS}}$-dependent capacitance values in the subthreshold region ($V_{\text{GS}} < V_T$ [threshold voltage]) are governed by the localized trapped charges ($Q_{\text{trap}}$) affected by $g(E)^9$

In order to map the applied $V_{\text{GS}}$ to specific trap energy levels inside the energy bandgap, the surface potential $\psi_s$ is calculated from the measured $C$-$V$ characteristic by use of Eq. (6).

FIG. 3. Measured $C$-$V$ curves with $f = 0.3, 0.5, 0.8, 1k, 3k, 5k, 10$ kHz and $V_{\text{GS}}=5 \sim 35$ V. The inset shows the optical photograph image of the fabricated EM-FET and schematic view of the $C$-$V$ measurement configuration.

FIG. 4. Frequency- and $V_{\text{GS}}$-dependent $G_p/\omega$ vs. $\omega$ plot. The $C_{\text{trap}}$ is obtained from the peak value of the $G_p/\omega$ (symbol: extracted data, line: fitted data).

FIG. 5. Extracted $g(E)$ and $g_{\text{int}}(E)$ before and after de-embedding parasitic pad capacitance ($C_{\text{pad}}$) from the proposed method.
As shown in Fig. 5, the $g_{int}(E)$ obtained from multi-frequency capacitance-conductance technique was extracted with a range of $7.5 \times 10^{17}$ eV$^{-1}$·cm$^{-3}$ to $1.3 \times 10^{18}$ eV$^{-1}$·cm$^{-3}$ near $E_C$. Model parameters for extraction of $g_{int}(E)$ are summarized in Table I. The extracted values obtained in this work are comparable to those of other reports. Therefore the multi-frequency conductance-voltage technique extracts the energy distribution of traps in the MoS$_2$ FET. This method is also applicable to other 2D-material based FETs.

In conclusion, a technique to extract intrinsic subgap DOS ($g_{int}(E)$) inside the energy bandgap is proposed, using the multi-frequency capacitance-conductance curves in the exfoliated MoS$_2$ FET (EM-FET). By employing the peak values of $G_p/\omega$ vs. $\omega$ plotted as a function of $f$ and $V_{GS}$, the energy distribution of the localized trap states in the MoS$_2$ channel was extracted quantitatively. The proposed technique is expected to be a robust tool for characterizing the trap behaviors, which are influenced by a structure, material, and fabrication process estimating of the instability and reliability of MoS$_2$ FETs.

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1 M. Amani, R. A. Burke, X. Ji, P. Zhao, D.-H. Lien, P. Taheri, G. H. Ahn, D. Kirya, J. W. Ager III, E. Yablonovitch, J. Kong, M. Dubey, and A. Javey, AIP Advances, 7, 075304-5, Bae, Kim, and Choi (2017).

2 S. Bertolazzi, D. Krasnozhon, and A. Kis, ACS Nano, 7, 3246 (2013).

3 G.-H. Lee, Y.-J. Yu, X. Cui, N. Petrone, C.-H. Lee, M. S. Choi, D.-Y. Lee, C. Lee, W. J. Yoo, K. Watanabe, T. Taniguchi, C. Nuckolls, P. Kim, and J. Hone, ACS Nano, 7, 7931 (2013).

4 Y. Y. Illarionov, M. Waltl, M. M. Furchi, T. Mueller, and T. Grasser, in Proceedings of the International Reliability Physics Symposium (2016), p. 1.

5 S. Ghatak, A. N. Pal, and A. Ghosh, ACS Nano, 7, 7707 (2011).

6 W. Zhou, X. Zou, S. Najmaei, Z. Liu, Y. Shi, J. Kong, J. Lou, P. M. Ajayan, B. I. Yakobson, and J.-C. Idrobo, Nano Lett., 13, 2615 (2013).

7 K. Cho, W. Park, J. Park, H. Jeong, J. Jang, T.-Y. Kim, W.-K. Hong, S. Hong, and T. Lee, ACS Nano, 7, 7751 (2013).

8 C.-K. Kim, C. H. Yu, J. Hur, H. Bae, S.-B. Jeon, H. Park, Y. M. Kim, K. C. Choi, Y.-K. Choi, and S.-Y. Choi, 2D Materials, 3, 015007 (2016).

9 K. Choi, S. R. A. Raza, H. S. Lee, P. J. Jeon, A. Pezeshki, S.-W. Min, J. S. Kim, W. Yoon, S.-Y. Ju, K. Lee, and S. Im, Nanoscale, 7, 5617 (2015).

10 H. Li, Q. Zhang, C. C. R. Yap, B. K. Tay, T. H. T. Edwin, A. Olivier, and D. Baillargeat, Adv. Func. Mater, 22, 1385 (2012).

11 D. K. Schroder, in Semiconductor Material and Device Characterization, (Wiley-IEEE Press, 2006), pp. 347–350.

12 S. Kim, A. Konar, W.-S. Hwang, J. H. Lee, J. Lee, J. Yang, C. Jung, H. Kim, J.-B. Yoo, J.-Y. Choi, Y. W. Jin, S. Y. Lee, D. Jena, W. Choi, and K. Kim, Nature Commun., 3, 1011 (2013).

13 H. Bae, C.-K. Kim, S.-B. Jeon, G. H. Shin, E. T. Kim, J.-G. Song, Y. Kim, D.-I. Lee, H. Kim, S.-Y. Choi, K. C. Choi, and Y.-K. Choi, IEEE Electron Device Lett., 37, 231 (2016).

14 M. Takenaka, Y. Ozawa, J. Han, and S. Takagi, in International Electron Device Meeting Tech. Dig. (2016), p. 139.