Improving the dynamics of a synchronous in-phase electric drive in transient modes of synchronization, phasing and control in response of reference signal changes

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Abstract. Synchronous in-phase electric drive is widely used in thermal-imaging and laser scanning systems due to their high accuracy and dynamic characteristics in a wide range of angular velocity control. The purpose of the article is to develop ways to control a synchronous-in-phase electric drive in the modes of synchronization, phasing and control in response of reference signal changes, allowing to improve the dynamic performance of the electric drive and reduce information loss in the scanning system. The method of electric drive phasing that is quasi-optimal in speed has been improved. Recommendations on the organization of transient processes with an abrupt change in the reference signal are formulated. For use in the electric drive control system, a circuit implementation of an impulse frequency-phase discriminator with an extended linear zone in the phase comparison mode has been proposed, it allows to improve the dynamic performance of the electric drive in the modes of synchronization, phasing and control in response of reference signal changes.

1. Introduction

Synchronous in-phase electric drive, which provides high accuracy of angular velocity control, the ability to install the optical system at the beginning of the scan line at the moments of coming of the clocking angle pulses and high speed in transient operating modes in a wide range of angular velocity control, is widely used in optical-mechanical and laser scanning systems as an electric drive of the optical mechanical scanning.

A generalized functional diagram of the synchronous in-phase electric drive is shown in Figure 1, where FU is the Rotation Frequency Unit, PDDU is the phase deviation detection unit of the clocking angle frequency pulses F_{ref} and feedback frequency F_{fb}, CU is the control unit, CLU is a comparison logical unit implemented on the basis of an impulse frequency-phase discriminator (IFPD), CD - correction device, PC - power converter, EM - electric motor, PSS - pulse speed sensor, PS - position sensor.
The internal control loop of the synchronous-in-phase electric drive is implemented in the form of a phase-locked electric drive (PLED), implemented on the basis of the phase-locked loop (PLL) [1], which allows high accuracy and dynamic performance of the electric drive in a wide range of angular velocity control [2-11]. In the phase-locked electric drive, the frequency signal $f_{\text{ref}}$ generated by the precision generator in the FU is used as the signal for the angular velocity setting; the frequency signal $f_{\text{fb}}$ generated at the output of the PSS is used as a feedback signal; and CLU is used as a comparing element.

The external control loop of the synchronous-in-phase electric drive is a phasing regulator (PR), which includes PS, PDDU, and CU. In the PDDU, the angular mismatch of the synchronous-in-phase electric drive is determined in the form of the phase deviation of clocking angle pulses $F_{\text{ref}}$ proportional to it generated in the FU and the angular position pulses of the electric motor shaft $F_{\text{fb}}$ formed at the output of the PS. The required law of synchronous-in-phase electric drive control in phasing mode is implemented in the CU.

The position sensors PS and the pulse speed sensors PSS are a block of PSU Pulse Sensor Unit (PSU) located on the motor shaft.

2. Formulation of the problem

The purpose of the article is to develop methods for controlling the synchronous-in-phase electric drive in the modes of synchronization, phasing, and control in response of reference signal changes, implemented on the basis of IFPD with a 3-fold extended linear zone and allowing improving the dynamic performance of the electric drive.

3. Theory

In the known PLED and synchronous-in-phase electric drive control systems, when the driving frequency is tuned, the PLL circuit is out of sync, and the PLED goes into acceleration or deceleration mode. As a result, when the electric drive reaches the new given speed, resynchronization and phasing [1] are required, which significantly reduces the performance of the synchronous-in-phase electric drive. In this case, a reduction in the transient time can be achieved by organizing transient modes without opening the PLL circuit.

The main reason for the automatic control system (ACS) opening in transient operating modes of the electric drive is the narrow linear IFPD zone in the phase comparison mode; as a result, with large initial conditions in the synchronization mode, repeated outputs to the CLU saturation modes and transfer of the electric drive to the open control mode are possible. It is proposed to improve the
performance of methods for controlling the synchronous-in-phase electric drive in transient operation modes by using IFPD with an extended linear zone in the phase comparison mode of the input pulse sequences $f_{\text{ref}}$ and $f_{\text{f}}$.

The transfer characteristic of an impulse frequency-phase discriminator is represented as a multi-valued static nonlinearity (Figure 2), reflecting the ability to synchronize the PLED in any of the $z$ linear sections defined by the angular distance between the $z$-marks of the PSS [1]. The polysemanticity of nonlinearity is manifested in the fact that in any of these areas the IFPD may be in any of the three states:
- saturation during PLED acceleration ($\gamma = \phi_0/2$),
- phase comparison mode ($\gamma = \Delta \phi$),
- saturation during PLED braking ($\gamma = -\phi_0/2$).

For the implementation of an impulse frequency-phase discriminator with an extended linear zone in the phase comparison mode, as a basis it is possible to use IFPD with additional functionality [12]:
- the formation of the phase error signal $\Delta \phi$ in the saturation modes IFPD,
- the formation of electric drive operating modes indication signals (A - acceleration, B - braking, P - proportional or closed control mode),
- the formation of indication signals of time moments of PLED operating mode change (0/2 - situation of frequency pulses $f_{\text{f}}$ absence between two adjacent frequency pulses $f_{\text{ref}}$, 2/2 - situation of passing two or more frequency pulses $f_{\text{f}}$ between two adjacent frequency pulses $f_{\text{ref}}$).

The transfer characteristic of IFPD with a 3-fold extended linear zone in the phase comparison mode is shown in Figure 3. This characteristic reflects the expansion of the IFPD linear zone to $\pm 3\phi_0/2$ in the synchronization area of the PLED.
A functional diagram of IFPD with an extended linear zone in the phase comparison mode [13] is proposed (Figure 4, where OS is a one-shot, DE is a delay element, LBD is a logical block diagram, AS-adder-subtractor).

![Figure 4. Functional diagram IFPD with extended linear zone](image_url)

The discriminator has two modes of operation: the frequency comparison mode and the phase comparison mode. When frequencies approach each other, the discriminator automatically switches from the frequency comparison mode to the phase comparison mode.

When the frequency of the reference signal $f_{\text{ref}}$ exceeds over the feedback signal $f_{\text{fb}}$, a condition in which, in the interval between the arrivals at the input of two pulses of the frequency $f_{\text{fb}}$, two pulses of the reference frequency $f_{\text{ref}}$ arrive at the input, necessarily occurs. The first pulse sets the inverse output of the phase RS-flip-flop to the logical «1» state; when the second pulse arrives, the second D-flip-flop is set to the logical «1» state. The pulse from the output of the second D-flip-flop is fed to the input of the second one-shot, which forms the output pulse 0/2 of the required duration, ensuring reliable operation of the impulse frequency-phase discriminator. The pulse 0/2 from the output of the second one-shot simultaneously arrives at the R-input of the second D-flip-flop, setting it to the logical «0» state, to the first input of the second AND gate and with a delay $\tau$ equal to the response time of the AND gates, through the logical OR gate and the delay element DE on the sync inputs of the blocking D-flip-flops.

If at the previous moment of time the first blocking D-flip-flop was in the logical «0» state ($B = 0$, $f_{\text{ref}} \geq f_{\text{fb}}$), then at the moment of arrival of the pulse on the sync input of the second blocking D-flip-flop, a logical «1» signal will be generated at its D-input, since the pulse that comes from the second one-shot through the second logical AND gate, will come at a time $\tau$ earlier. As a result, the second blocking D-flip-flop will go into a logical «1» state, forming a signal ($A = 1$, $f_{\text{ref}} > f_{\text{fb}}$) that the reference frequency is over the monitored one. The inverse output of the second blocking D-flip-flop blocks the operation of the second logic NAND gate and the logical "1" state is set at the output $\gamma$ of the impulse frequency-phase discriminator. The state of the first blocking D-flip-flop remains unchanged, since at the moment of arrival of a pulse at its sync input, a logical "0" signal is present at the D-input.

If at the previous moment of time the first blocking D-flip-flop was turned on ($B = 1$), then at the moment of arrival of the pulse on the sync input of the second blocking D-flip-flop, its D-input will be in the logical "0" state, since the pulse from the second one-shot will not pass through the second logic AND gate blocked by the inverse output of the first blocking D-flip-flop. As a result, the logical "0" signal ($A = 0$) is established on the direct output of the second blocking D-flip-flop, and the inverse output is set to the logical «1» state and thereby unlocks the operation of the second logic NAND gate.
The first blocking D-flip-flop switches to the off state \((B = 0)\), since at the moment of pulse arrival at its sync input, a logical “0” signal is present at the D-input. The discriminator moves from the frequency comparison mode to the phase comparison mode. Since the “enable” signals of the logical «1» are fed to the logical NAND gates from the inverse outputs of the blocking D-flip-flops, a discriminator output passes a signal proportional to the phase error \(\gamma = \Delta \phi\), from the inverse output of the phase RS-flip-flop, the output pulses duration of which is proportional to the phase shift of the compared frequencies pulses. With the help of the third logical AND gate the signal \(P\) is formed, corresponding to the phase comparison mode of the discriminator.

When the frequency of the monitored signal exceeds the reference one, the output signal of the discriminator \(\gamma\) is formed similarly (due to the symmetry of the comparator logic), starting from setting the direct output of the phase RS-flip-flop to the logical "1" state.

When the discriminator goes into phase comparison mode, the signal \(P = 1\) appears at the output of the third logical element AND, through which the RS-flip-flop is set to the logical "1" state and the output signal \(P_{ex}\) of the discriminator is formed, which is an indicator of the phase comparison mode with a 3-fold extended linear transmission range of the phase error signal. When the signal \(P_{ex} = 1\) appears, digital keys made on the fourth and fifth logical AND gates are opened, allowing the passage of the A and B signals, respectively, to the adding and subtracting inputs of the adder-subtractor, at the output of which the signal of the phase error \(\Delta \phi_{ex}\) with the 3-fold linear transmission range appears. Adding the signal \(A = 1\) to the signal \(\Delta \phi\) allows to expand the linear zone for determining the phase error to \(3\pi\), and subtracting the signal \(B = 1\) to expand the linear zone for determining the phase error to minus \(3\pi\). A threefold extension of the linear zone of the phase error determination eliminates situations in which the discriminator goes into saturation modes, which can occur under large initial conditions by frequency error when entering synchronization mode, in phase-locked loop synchronization mode, and, as a result, to increase phase-locked loop speed in transient modes of operation.

The RS-flip-flop is reset to the logical “0” \((P_{ex}=0)\) state and, accordingly, the linear zone is 3 times narrowed to the initial state in the case of 0/2 or 2/2 signals re-formation, which corresponds to a step change in the driving (reference) frequency \(f_{ref}\). The 2/2 pulses re-passage situation determination is carried out using the third D-flip-flop, to the informational D-input of which a signal B is fed (corresponding to the first appearance of the pulse 2/2), and to the clock C-input - a 2/2 signal. The 0/2 pulses re-passage situation determination is carried out using the fourth D-flip-flop, the information D-input of which receives a signal A (corresponding to the first appearance of the 0/2 pulse), and the clock C-input receives a 0/2 signal. The reset of the third and fourth D-flip-flops is carried out by the signal P, corresponding to the operation of the discriminator in the phase comparison mode. When a logical "1" signal appears at the output of the third or fourth D-flip-flops to the R-input of the RS-flip-flop, the second logical OR gate passes the logical «1» signal, resetting the RS-flip-flop to the logical «0» state, which corresponds to the end of the discriminator operating mode in the extended linear zone \((P_{ex}=0)\).

The considered functional diagram of IFPD with an extended linear zone in the phase comparison mode can be used in the PLED (Figure 5), which is the basis for building the synchronous-in-phase electric drive with the organization of transient synchronization processes, phasing and testing of the reference signal change without opening the automatic control system.
In this scheme, the $P_{ex}$ signal generated at the third IFPD output is used to control the multiplexer, while the multiplexer output signal is $\gamma_{ex} = \gamma$ in the absence of the $P_{ex}$ signal, and $\gamma_{ex} = \Delta \varphi_{ex}$ with $P_{ex} = 1$.

The control of the synchronous-in-phase electric drive without breaking the ACS (automatic control system) is used in the method of phasing [14] that is quasi-optimal in speed. This method is implemented on the basis of an additional PLL circuit, which in the phasing mode generates a linearly increasing or decreasing reference signal for the PLED with acceleration slightly lower than the maximum acceleration $\varepsilon_m$. The testing of this reference signal can occur without opening the ACS, which allows completing the transition process without additional synchronization and phasing modes.

The technical implementation of this method has been improved by organizing additional control of the PLL circuit [12] in various operating modes of the electric drive (Figure 6, where FD is a frequency divider, CB is a correction block, I is an integrator, CG is a controlled generator, SK is a slave key, PCU - phasing control unit).

In this scheme, the signal $\Phi$ (indication of the phasing mode) is additionally used to control the gain in the CB, which allows realizing different rates of change in the frequency $f'_{ref}$ in acceleration (breaking) and phasing modes. As a result, in the phasing mode of the synchronous-in-phase electric drive, the rate of change of the output frequency of the PLL circuit is less than $\varepsilon_m$, and in the acceleration and breaking modes of the drive exceeds $\varepsilon_m$. Due to this implementation, by the time the phasing mode starts, the output frequency of the PLL circuit ahead of time becomes equal to the
frequency of the $f_{ref}$ reference, which eliminates the time lost in preparing the electric drive for the phasing mode and, as a result, increases the synchronous-in-phase electric drive speed.

This principle of regulation with the use of an additional PLL circuit can be used to organize the control of the PLED during the control in response of a reference signal abrupt change. In this case, the linearly varying output signal of the PLL circuit is used as a reference signal for PLED, which allows the drive to switch from one given speed to another at a lower acceleration value, but without opening the ACS.

As a result, the need for repeated synchronization and phasing modes is eliminated, which increases the performance of the synchronous-in-phase electric drive in transient operating modes and reduces information loss in the scanning system.

4. Findings and conclusion

The article proposes an operation algorithm and a circuit implementation of IFPD with an extended linear zone in the phase comparison mode of the input pulse sequences, on the basis of which the PLED is implemented with an extended working range in the closed-loop control mode during the drive synchronization. The developed PLED circuit can serve as a basis for building a synchronous-in-phase electric drive operating in transient synchronization and phasing modes without opening the ACS, which will improve the dynamic characteristics of the electric drive, primarily its speed, and reduce information loss in the scanning system.

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