Alleviating Datapath Conflicts and Design Centralization in Graph Analytics Acceleration

Haiyang Lin\textsuperscript{1,2}, Mingyu Yan\textsuperscript{1,2,*}, Duo Wang\textsuperscript{1,2}, Mo Zou\textsuperscript{1,2}, Fengbin Tu\textsuperscript{3}, Xiaochun Ye\textsuperscript{1,2}, Dongrui Fan\textsuperscript{1,2}, Yuan Xie\textsuperscript{3}

\textsuperscript{1}\textsuperscript{1}State Key Laboratory of Computer Architecture, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China
\textsuperscript{2}University of Chinese Academy of Sciences, Beijing, China
\textsuperscript{3}University of California at Santa Barbara, CA, USA

ABSTRACT

Previous graph analytics accelerators have achieved great improvement on throughput by alleviating irregular off-chip memory accesses. However, on-chip side datapath conflicts and design centralization have become the critical issues hindering further throughput improvement. In this paper, a general solution, Multiple-stage Decentralized Propagation network (MDP-network), is proposed to address these issues, inspired by the key idea of trading latency for throughput. Besides, a novel High throughput Graph analytics accelerator, HiGraph, is proposed by deploying MDP-network to address each issue in practice. The experiment shows that compared with state-of-the-art accelerator, HiGraph achieves up to 2.2× speedup (1.5× on average) as well as better scalability.

KEYWORDS

graph analytics, datapath conflicts, design centralization, acceleration, domain-specific architecture

1 INTRODUCTION

Graphs exhibit powerful representation capacity for real-world data in a broad range of scenarios, which is accompanied by many graph analytics applications, such as placement [Hu et al. 2004], circuit partitioning [Selvakkumaran and Karypis 2006], and technology mapping [Francis et al. 1990] in EDA flow. Not surprisingly, the demand for high throughput in the execution of graph analytics workloads is ever-growing as the scale of graph data increases.

Recently, plenty of graph analytics accelerators have been well designed to improve throughput by alleviating the critical performance bottleneck, i.e., irregular accesses to off-chip memory. For example, Graphicionado [Ham et al. 2016] and GraphDynS [Yan et al. 2019] leverage a large-capacity on-chip memory to buffer all vertices’ property data on the chip, significantly alleviating irregular off-chip accesses. Even in the case of large-scale graphs, graph slicing can be used to partition the graph into a set of small slices to perform the processing using limited capacity of on-chip memory [Ham et al. 2016].

Unfortunately, on-chip side datapath conflicts and design centralization are becoming increasingly significant bottlenecks on the throughput improvement. To exploit the high-degree parallelism in graph analytics workloads, most of the accelerators are in favor of adopting multiple parallel execution channels. However, due to the irregular connection pattern across vertices, interaction across execution channels is inevitable, which brings two following inefficiencies to previous designs. The first is Datapath Conflicts, which means multiple datapaths that process different vertices compete for the same accessible resource or same dataflow channel, causing serious stall in datapaths. As a result, the overall performance will significantly degrade due to the severe blocking of execution channels. The second is Design Centralization, which means the implementation of design becomes extremely difficult with the increasing amount of execution channels due to the over-intensive interaction across total execution channels, causing frequency decline. For example, on-chip crossbar is a prevalent solution to direct the dataflow between different execution channels [Ham et al. 2016; Yan et al. 2019]. However, it suffers from not only the frequency decline which hinders the pursuit of high throughput, but also a dramatic increase in area and power consumption, when channel number increases [Cagla et al. 2015].

In this work, we observe that the execution channel in the state-of-the-art accelerator is highly pipelined [Ham et al. 2016; Yan et al. 2019], which reveals that increasing the traversal latency of a single edge does not pose significant impact on overall performance. Therefore, inspired by the key idea of trading latency for throughput, we propose a general solution, Multiple-stage Decentralized Propagation network (MDP-network). MDP-network decentralizes the intensive interactions across execution channels to multiple stages and buffers data in each stage. Data in MDP-network is propagated deterministically to next stage until reaching their destinations. On one hand, the multiple-stage and deterministic propagation alleviate datapath conflicts.

On the other hand, the inefficiency of design centralization is avoided since the number of interactive execution channels in each stage is limited to a small number. To facilitate adoption, we provide an open-source automatic generator of MDP-network\textsuperscript{1}. Finally, a novel High throughput Graph analytics accelerator, HiGraph, is proposed by deploying MDP-network to tackle data conflicts and design centralization in practice.

The main contributions of this paper are as follows:

• We identify the inefficiencies including datapath conflicts and design centralization in graph analytics acceleration.

\textsuperscript{1}https://github.com/OpenSource88/MDP-network.git
We propose MDP-network, Multiple-stage Decentralized Propagation network, to alleviate datapath conflicts and design centralization. Besides, an automation tool is developed to generate MDP-network and open source to facilitate its deployment.

We propose HiGraph, a novel high throughput graph analytics accelerator coupled with MDP-network, and implement it in RTL. The experimental results show that compared to the state-of-the-art design, HiGraph achieves up to 2.2× speedup (1.5× on average) as well as better scalability.

2 BACKGROUND AND MOTIVATION

2.1 CSR Format and VCPM

Compressed Sparse Row (CSR) format is a widely used storage-efficient technique to represent graph structures in software frameworks [Gonzalez et al. 2014; Shun et al. 2013] and accelerators [Ham et al. 2016; Yan et al. 2019]. Fig. 1 illustrates that three data arrays, Offset, Edge, and Property, are used to encode a graph. Each Offset entry stores the position of its first neighbor in the Edge Array. The Edge Array maintains destination vertex ID and weight for each outgoing edge. The Property Array holds current property value for each vertex.

Existing graph analytics software frameworks [Fu et al. 2014; Malewicz et al. 2010] and accelerators [Ham et al. 2016; Yan et al. 2019] usually employ Vertex-Centric Programming Model (VCPM) to accomplish iterative graph algorithms. VCPM consists of scatter and apply phases, as shown in Fig. 2. In the scatter phase, each active vertex first aggregates the effect of its property and edge weight via a user-defined function Process_Edge( ), then broadcasts the accumulated influence to update its outgoing neighbors in an additional iProperty Array using user-defined function Reduce( ). In the apply phase, data in the iProperty Array is synchronized to the Property Array using user-defined function Apply( ). VCPM updates the Property Array iteratively until all vertices are inactive.

![Figure 1: An example graph in CSR format.](image)

2.2 Inefficiencies of Previous Designs

By adopting multiple parallel execution channels, as shown in Fig. 3, previous VCPM-based graph analytics accelerators have achieved great throughput improvement. However, due to irregular connection pattern across vertices, interaction across execution channels is inevitable, bringing two following inefficiencies in previous designs.

**Datapath Conflicts:** multiple datapaths that process different vertices compete for the same accessible resource or same dataflow channel, causing serious datapath stall. Fig. 3 demonstrates three types of datapath conflicts existing in graph analytics accelerators with multiple parallel execution channels. Note that to meet the requirement of data-access throughput in such a design, the buffer for each data array is divided into several parts and organized in the fashion of interleaving.

The first datapath conflict occurs in **Offset Array Access,** where two consecutive buffer parts are accessed concurrently to obtain start and end positions in the Edge Array of one active vertex. The second datapath conflict happens in **Edge Array Access,** where a list of edges is accessed simultaneously from multiple buffer parts. The third datapath conflict occurs in **Dataflow Propagation,** where the dataflow is directed according to the destination vertex ID of each edge. Datapath conflicts arise when multiple datapaths require the same accessible resource or same dataflow channel simultaneously. As a result, the execution channels failing in arbitration will be blocked, which inevitably degrades overall performance.

**Design Centralization:** the implementation of design becomes extremely difficult with the increasing amount of execution channels due to the over-intensive interaction across total execution channels, causing frequency decline. In previous graph analytics accelerators, arbitration solution like crossbar is prevalently used to deal with interaction of multiple channels [Ham et al. 2016; Yan et al. 2019]. Fig. 4 demonstrates that the frequency declines sharply with the increasing number of crossbar ports, limiting the throughput improvement. The frequency is determined by the critical path time which is derived from the synthesis result of Synopsys Design Compiler.

**Opportunity:** we observe that the execution channel in the state-of-the-art accelerator is highly pipelined, which reveals that increasing the traversal latency of a single edge has marginal impact on overall performance. It inspires us that we can trade latency for throughput. Thus, it is practical to insert additional stages in the datapath to gradually guide the data to the destination execution channel, which alleviates datapath conflicts. Besides, we can alleviate design centralization by limiting the number of interactive channels in each stage. Based on the above insights, we propose a general solution, MDP-network, to alleviate datapath conflicts and design centralization.

3 MULTIPLE-STAGE DECENTRALIZED PROPAGATION NETWORK

3.1 Design Theory

In this subsection, we first abstract the interaction across execution channels, which brings datapath conflicts and design centralization. Then, we introduce the design theory of MDP-network from a naive solution.

Fig. 5 (a) abstracts the interaction across execution channels in Fig. 3, where data from two input channels is directed to two output channels. Using arbitration, e.g., crossbar, encounters datapath conflicts.

A naive solution for datapath conflicts is to use n-Write-1-Read (nW1R) First-In-First-Out queue (FIFO), which means FIFO can input n datums and output one datum in each cycle. As shown in Fig. 5 (b), 2W1R FIFO is used to direct data to destination channel in each cycle, therefore no input channels would stall unless the FIFO is full. However, it encounters two critical issues when the number of channels increases, as shown in Fig. 5 (c). One is large requirement of buffer capacity. For example, when the number of write ports is 32, the FIFO can accept data only when the remaining capacity is not less than 32. This causes large requirement and low utilization of buffer capacity. Another is design centralization, the
3.2 Automatic Generator for MDP-network

Algorithm 1 describes the simplified workflow of an automatic MDP-network generator. We define radix as the number of FIFO write ports and take radix 2 as an example here. To facilitate the deployment of MDP-network, the algorithm consists of two steps: 2W2R module construction (line 1) and input ports connection (line 2 - line 16). It is straightforward to construct a 2W2R model following the rule shown in Fig. 5 (b). Once the construction is finished, input ports connection is performed to choose the corresponding 2W2R module for input ports in each MDP-network stage.

Fig. 5 (d) presents a toy example of input ports connection for four channels. MDP-network uses two address bits, addr[0:1], to specify four destination channels and constructs \( \log_2 4 = 2 \) stages. In the first stage, we classify all input channels into one group (target_group = 1) since they have the same target range, i.e., output channels 0-3. Channel_step is the difference between two input channel IDs connecting to one 2W2R module (channel_step = 2). So we connect input ports [0, 2] and [1, 3] to two 2W2R modules respectively with addr[1]. Note that we draw two 2W1R modules using the same color in Fig. 5 (d) if they come from one 2W2R module.
4.1 MDP-network for Offset Array Access

Referring to Fig. 3 (a), the access pattern in reading Offset Array is one-to-two, indicating that the algorithm reads two consecutive buffer parts indexed by \( u.ID \) and \( u.ID + 1 \) of source vertex \( u \).

Fig. 6 shows that, to deal with such an access pattern, we first deploy MDP-network to guide source vertices to corresponding output channels, e.g., \( u.ID \) 0 is directed to channel 0. Then it is apparently that each source vertex requires to occupy its corresponding and next read channels, e.g., vertices in channel 0 requires the read channel 0 and 1. In this way, any source vertices in one channel will only have conflicts with those in neighbor channels. Thus we insert an Odd-Even Arbiter to determine vertices in which channels should be issued in current cycle.

The arbiter rule is alternating priority, which means odd and even channels alternately have higher priority to issue vertices. In this way, those vertices in the channel with higher priority can always be issued immediately without considering datapath conflicts and occupy several read channels. The other vertices would be issued only when their destination read channels are not occupied or their target addresses are the same with those who have occupied the read channels.

4.2 MDP-network for Edge Array Access

Referring to Fig. 3 (b), the access pattern in reading Edge Array is one-to-multiple, indicating that one \( \{ \text{Off}, \text{nOff} \} \) requires to access multiple consecutive buffer parts to get edges.

Fig. 6 demonstrates the variant of MDP-network for Edge Array access pattern. We insert Replay Engines to divide \( \{ \text{Off}, \text{nOff} \} \) into several \( \{ \text{Off}, \text{Len} \} \) with an appropriate length. Then we use
PR, the pattern of dataflow propagation is that --

MDP-network to guide data to destination channels and one extra operation is required here. While the target range is becoming smaller as the data is propagated stage by stage, correspondingly, we will split the input length into small output length to make {voltage of 0.8 rise to frequency decline due to the delicate arbitration in read-channels in GraphDynS as four since a larger number would give a critical path of 0.93

Table 1: Configurations used for HiGraph and baselines.

|                  | HiGraph | HiGraph-mini | GraphDynS |
|------------------|---------|--------------|-----------|
| Frequency        | 1GHz    | 1GHz         | 1GHz      |
| #Front-end       | 32      | 4            | 4         |
| #Back-end        | 32      | 32           | 32        |
| On-chip memory   | 16MB    | 16MB         | 32MB      |

4.3 MDP-network for Dataflow Propagation

Referring to Fig. 3, the pattern of dataflow propagation is that multiple input data are directed to multiple output channels. As MDP-network is designed to deal with such a pattern, we directly deploy original MDP-network to this stage to alleviate datapath conflicts and design centralization.

5 EVALUATION

5.1 Experimental Setup

Methodology. We implement HiGraph in RTL with Verilog. We use the Synopsys Design Compiler with the TSMC 12nm standard VT library for synthesis. We give the synthesis tools an operating voltage of 0.8V and a target clock cycle of 1ns. The slowest module has a critical path of 0.93ns including setup and hold time, putting the HiGraph design comfortably at 1GHz. The ID and property data of each vertex are quantified to 19 bits to fully use on-chip memory capacity. The layout of HiGraph is shown in Fig. 7.

Baselines. To compare HiGraph with state-of-the-art work, we prototype GraphDynS in RTL. We set the number of front-end channels in GraphDynS as four since a larger number would give rise to frequency decline due to the delicate arbitration in reading Offset Array. To compare fairly, we also set up HiGraph-mini with the same number of front-end channels. Table 1 shows the configurations for these implementations.

Datasets. Table 2 describes the datasets used for our evaluation. A mixture of real-world graphs - VT, EP, SL, TW and synthetic graphs - R14, R16 are used in the evaluation. Four graph algorithms - BFS (Breadth-First Search), SSSP (Single Source Shortest Path), SSWP (Single Source Widest Path) and PR (PageRank) are used to evaluate HiGraph. For the evaluation on unweighted graphs, random integer weights are assigned.

5.2 Overall Results

Speedup: Fig. 8 shows the speedups of HiGraph and HiGraph-mini normalized to GraphDynS. With the same number of front-end channels, HiGraph-mini achieves 1.19× to 1.85× speedup over GraphDynS, and 1.46× on average. With MDP-network optimization, HiGraph increases the number of front-end channels without frequency decline. Thus, with more front-end channels, HiGraph achieves up to 2.23× speedup over GraphDynS (1.54× on average).

5.3 Effects of Optimizations

A detailed evaluation on the RMAT14 dataset is presented to provide more insights into the effects of our optimizations, as shown in
changes slightly with relatively small radices. Thus, we choose radix 2 in our design.

We run experiments on buffer size of MDP-network. We keep all designs in HiGraph the same except for the dataflow propagation stage, in which we replace MDP-network with FIFO-plus-crossbar design. Fig. 12 demonstrates that MDP-network outperforms FIFO-plus-crossbar consistently with various buffer sizes on the PR algorithm with RMAT14 dataset. We choose 160 entries as the buffer size of FIFO in each channel because the throughput rarely increases with larger buffers. We synthesis MDP-network with buffer size 160 and the area is $0.375\text{mm}^2$ while power is 621.2mW. We also synthesis FIFO-plus-crossbar design with buffer size 128 and the area is $0.292\text{mm}^2$ while power is 508.1mW. The area and power of MDP-network is slightly higher due to the larger buffer, showing that replacing crossbar with MDP-network brings little overhead.

6 RELATED WORK

Prior works focus on optimizing irregular off-chip memory accesses to pursue high throughput of graph analytics [Ham et al. 2016; Ozdal et al. 2016; Rahman et al. 2020; Yan et al. 2019]. By preprocessing [Kyrola et al. 2012] and partitioning [Ham et al. 2016], a large graph can be partitioned into a set of slices to fit the data being irregularly accessed on-chip memory. Moreover, Centaur [Addisie et al. 2020] is an accelerator that only maps high-degree vertices on-chip memory. To further pursue higher throughput, prior accelerators [Ham et al. 2016; Yan et al. 2019] provide parallel execution channels design according to the execution characteristic of graph analytics workloads. Unfortunately, few attention is paid to datapath conflicts and design centralization that have become the critical issues. Using our MDP-network, these issues are alleviated and high throughput is realized.

7 CONCLUSION

In this paper, we identify the inefficiencies in graph analytics acceleration including the datapath conflicts and design centralization. To this end, we propose MDP-network, inspired by the idea of trading latency for throughput. Besides, an automatic generator for MDP-network is developed and open source. Finally, a novel high throughput graph analytics accelerator, HiGraph, is proposed by deploying MDP-network to tackle data conflicts and design centralization in practice. HiGraph archives up to 2.2× speedup (1.5× on average) compared to state-of-the-art accelerator.
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