Razor flip-flop based Detector/Corrector System for Correcting Timing violations in Digital Circuits

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Abstract. In a flip flop, the difference in time between transitions of data input and the active edge of the clock is called its setup time. If the data input changes during this time window, the storage will not be correct. This is called setup time violation. Hold time is the minimum time during which data must be stable after the active edge of the clock. Hold time violation will cause incorrect data storage. The objective of the paper is to design an efficient Detector/Corrector system that monitors and corrects any setup/hold time violations. A Razor flipflop based Detector circuit is proposed in this paper. The Detector block compares data and clock to produce an error signal which in turn makes the Corrector block to correct the clock that assures the desired setup/hold time. The system avoids the setup/hold time violations by simply inverting the clock signal timing. The system is tested using the following digital circuits: ISCAS89 S27 benchmark circuit and a 2x1 multiplexer. Simulation is done using Cadence Virtuoso with 180nm technology. The results are analyzed with existing and proposed detector/corrector systems. The results show that the proposed detector/corrector system is capable of correcting both the setup/hold time violations and also has lesser power consumption when compared with the existing system.

1. Introduction

Setup time and hold time are essential for timing analysis of any digital circuit. In a circuit, only if the setup and hold time value for every flip-flop is met, then the circuit will work properly. If even a single flop does not meet the setup and hold requirements, the entire design will fail. D-type flip-flops are commonly used in sequential circuit design. The input data should not be allowed to switch its state during the setup/hold time duration. This is because, whenever the data makes transition it will take a minimum amount of time to become constant in its current state. Hence these timing constraints if not achieved will produce wrong operation in the flip-flop.
Fig. 1 illustrates the setup time and hold time definition and is given as follows,

1. **Setup Time** ($t_{su}$): The input signal D should arrive at least some time before the rising edge of the clock. This timing requirement is called setup time.

2. **Hold Time** ($t_{hd}$): Similarly, after the rising edge of the clock occurs, the input D should remain constant at least for some time. This timing requirement is called hold time.

In [1], the system consists of a setup/hold time violation Detector. The Detector sends a 2-bit wide control signal to the Corrector. Within the chip, the Detector circuit should be located in the neighborhood of flip-flops because it has to send control signals to the corrector. Corrector circuit is designed with a set of CMOS inverters and a multiplexer. The Corrector can be located either closer to the clock signal generator circuit (for correcting the global clock) or adjacent to the flipflops (for correcting the local clock). Since the Detector/Correction system has a simple design, it is repeated throughout the chip wherever needed. Thus the system is capable of detecting and correcting the setup/hold time violations if any, by using a simple technique. [2] proposes a linear programming based approach for minimizing the number of inserted delays. In [3], the Dynamic Flip Flop Conversion structure proposed, automatically reduces the transparency window if the data arrives late to the critical path flipflops. Statistical Monte Carlo analysis on the critical path of different benchmarks with different TB methods was performed. DFFC is found to be more efficient in higher frequencies and longer critical paths. Common problems of error handling techniques for sequential logic are addressed in [4]. A low-cost shadow cell based approach is proposed. Transient faults and timing violations are detected and corrected by this principle. In [5], low-power method is proposed for timing closure for Ultra Low Voltage (ULV) designs. The work in [5] involves clock tree and data path synthesis. It reduces the required inserted delay and is capable of avoiding hold time violations in the various power saving modes. In this paper, the performance of the detector/corrector system is analyzed using a Benchmark circuit.

The paper is organized as follows: Section 2 explains the block diagram of existing and proposed systems. Section 3 gives the implementation details. Section 4 discusses the simulation results and Section 5 gives the conclusion of the work.

2. **Overall System Block Diagram**
The detector and corrector circuits are designed to achieve required setup and hold time [1]. The general block diagram of designed method is shown in Fig. 2. The system consists of two individual blocks: detector and corrector [1]. The detection/correction system continuously monitors the occurrence of active edge of clock and transitions at the data signals. It adjusts the clock signal timing so as to ensure that the setup/hold time constraints are never violated.

2.1. Detection Circuit

Setup time and Hold time violations are detected by checking the relative switching of data and clock signals. Whenever data changes prior to the positive clock edge or after the positive clock edge then the detector circuit produces a positive pulse. The one shot generator produces a positive pulse whenever there is a low to high transition at the input.

2.1.1. Existing Detection Circuit

The one shot generator present in the existing detection circuit is shown in Fig. 3. The one shot generator is designed with inverter gates and NAND gate. The inverter gate acts as a delay element. The one shot generator designed with one inverter stage is shown in Fig 3(a). Whenever a rising edge occurs at the input signal, the circuit generates a pulse. The pulse width of the shot is proportional to the inverter delay. Since there is only one inverter, the width of the shot is not wide enough to excite the following gate. Hence, a one shot generator using three delay elements (shown in Fig 3(b)) is used. Here three inverters are used for introducing the required delay in the clock. The reason for using the three-inverter circuit is, the setup time/hold time margins depend on the width of the shot. Negative edges can be detected by modifying one shot generator and by adding an inverter at the input path.
Fig. 4 shows the Detection circuit. The circuit consists of two one shot generators. First one shot generator is used for detecting the positive edge of clock and second one is used for detecting the positive edge of data. NAND gate is used to compare the output of the two one shot generators. The detector generates a shot when the clock and data overlaps completely. This indicates a timing violation. As a result, pulsewidth of the shots fixes the desirable setup time/hold time margins.

2.1.2. Proposed Detection Circuit

In the proposed detector circuit, instead of one shot generator (using inverters), Razor flipflop [15] is used to generate the shot. Razor flipflop circuit is shown in Fig. 5. It has two D flipflops. One with a fast clock and another one with a delayed clock signal. At the positive clock edge, if both the D flipflops latch the correct data, then the output of the XOR gate remains low. If both the flipflops do not latch the data correctly, then the output of the XOR gate will become high and thus an one shot is generated. The shot indicates the detection of a timing violation in the circuit tested.
2.2. Correction Circuit

Assume the data edges violate setup time and hold time constraints. In general to rectify the violation, either the clock is moved along the time axis or the buffer is added at the input path. But this arrangement will increase the delay. In this design there is no need to move clock continuously rather it can be corrected by modifying the clock signal timing so as to ensure that the setup/hold time requirements are never violated. Complete correction circuit is shown in Fig 6. The correction circuit consists of multiplexer and delay taps. The multiplexer circuit is designed using 2:3 decoder. The decoder is configured such that it selects the third switch for both $s_1s_0 = “10”$ or $“11.”$ For example if $s_1s_0= 00$, CLKc follows the clock and $s_1s_0=01$ CLKc produces the inverted clock. Thus the system corrects the clock till the required setup time and hold time is achieved.

The full detection circuit along with the counter is shown in Fig 7. The 4bit ripple counter is connected at the detector’s output. The detector detects the violation and sends output pulse to the counter. The counter is designed using TFF. Even though 2 bit counter is sufficient to generate the two bit signal, a 4 bit ripple counter is used in order to maintain stability in the system. The counter performs the increment operation and the MSB 2 bit output forces to the multiplexer. The multiplexers
accept the control signal from the counter and produce the corrected clock to the digital circuit. The extra delay elements inside the correction circuit corrects the timing issues at higher frequencies.

3. Implementation

The existing detector, proposed detector and corrector circuits are implemented to achieve the required setup and hold time. The simulation is done using Cadence virtuoso tool with 180nm technology. The clock frequency used is 1MHz. The detector and corrector blocks are implemented in two digital circuits to detect/correct their timing violations. The digital circuits tested are: 2X1 multiplexer and an ISCAS89 benchmark circuit. ISCAS89 benchmark circuits are a standard set of 31 digital sequential circuits. The model of the benchmark circuit considered for testing is S27 and is shown in Fig. 8.

S27 benchmark circuit is a standard sequential circuit with 4 primary inputs, 3 DFF and one primary output. Here, the next state totally depends on primary inputs. The 2x1 multiplexer considered for testing is shown in Fig.9 below:
4. Simulation Results
The digital circuit to be tested for timing violations is connected as shown in Fig. 2 and the simulation waveforms are obtained. The detection circuit simulation waveforms of clock, data, in, detout, s0, s1 are shown in Fig. 10. Whenever there is an overlap between the clk and data the output of the detector is high, which indicates presence of timing violation in given digital circuit. At the time of high signal in the detector output, the counter performs the increment operation as shown in Fig. 10.

After 8 high signals from the detector, the corrector starts to invert the clock. The inverted clock satisfies the setup/hold time constraint. Thus the timing violations are corrected.

4.1. SIMULATION RESULTS OF S27 BENCHMARK CIRCUIT USING EXISTING DETECTOR/CORRECTOR CIRCUIT
The simulation waveforms obtained by testing the existing detector/corrector system using S27 benchmark circuit is shown in Fig.11. The benchmark circuit considered for testing has hold time violation. Hence the detector produces high output. After 8 high signals from the detector, the corrector inverts the clock (at time instant 50us) as shown in Fig. 10. Hence the violation is corrected.
4.2. SIMULATION RESULTS OF S27 BENCHMARK CIRCUIT USING PROPOSED DETECTOR/CORRECTOR CIRCUIT

The simulation waveforms obtained by testing the proposed detector/corrector system using S27 benchmark circuit is shown in Fig. 12. The benchmark circuit considered for testing has hold time violation. Hence the detector produces high output.

After 8 high signals from the detector, the corrector inverts the clock (at time instant 20us) as shown in Fig. 12. Hence the violation is corrected.
4.3. SIMULATION RESULTS OF 2X1 MULTIPLEXER CIRCUIT USING EXISTING DETECTOR/CORRECTOR CIRCUIT

The simulation waveforms obtained by testing the existing detector/corrector system using the 2x1 multiplexer circuit is shown in Fig.13. The multiplexer circuit considered has both setup time violation and hold time violation. Hence the detector produces high output. After 8 high signals from the detector, the corrector inverts the clock (at time instant 70us) as shown in Fig. 13. Hence the violations are corrected.

Figure 13. Waveforms of 2x1 multiplexer after testing with existing detector/corrector system

4.4. SIMULATION RESULTS OF 2X1 MULTIPLEXER CIRCUIT USING PROPOSED DETECTOR/CORRECTOR CIRCUIT

The simulation waveforms obtained by testing the existing detector/corrector system using the 2x1 multiplexer circuit is shown in Fig.14. The multiplexer circuit considered has both the timing violations. Hence the detector produces high output.

Figure 14. Waveforms of 2x1 multiplexer after testing with proposed detector/corrector system
After 8 high signals from the detector, the corrector inverts the clock (at time instant 20us) as shown in Fig. 14. Hence the violations are corrected.

Table 1 presents the setup and hold time results of the tested circuits before and after correction. It shows the results obtained using the existing detector/corrector system. The correction system corrects the negative timing violation in data path and clock path. The table shows that the benchmark circuit has a hold time of -0.28us initially. The negative value of hold time indicates that there is violation. The benchmark circuit has no setup time violation. After the detector/corrector system is applied the negative hold time is corrected as 25 ns [Because of clock inversion, the hold time now becomes -0.28us + 0.5us = +0.22us = 25ns approximately]. Similarly, the 2x1 multiplexer circuit has a setup time of -0.9 us and a hold time of -8 us, initially. After correction, it has a setup time of 0.59 us and hold time of 69.8ns. Thus the detector/corrector system is capable of correcting setup/hold time violations.

### Table 1. Analysis of Setup and Hold Time using the Existing Detector/Corrector System

| CIRCUIT                        | SETUP TIME (sec) | HOLD TIME (sec) | POWER  |
|-------------------------------|-----------------|----------------|--------|
| S27 benchmark circuit before applying correction | 0.59u           | -0.28u         |        |
| S27 benchmark circuit after applying correction | 5n              | 25n            | 27.43uW|
| Multiplexer circuit before applying correction | -0.9u           | -8u            |        |
| Multiplexer circuit after applying correction | 0.59u           | 69.8n          | 9.22uW |

Table 2. presents the setup and hold time results of the tested circuits after correction. It shows the results obtained using the proposed detector/corrector system.

### Table 2. Analysis of Setup and Hold Time using the Proposed Detector/Corrector System

| CIRCUITS                       | SETUP TIME (ns) | HOLD TIME (ns) | POWER         |
|--------------------------------|-----------------|----------------|---------------|
| S27 benchmark circuit after applying correction | 90              | 70             | 15.34uW (44%) |
| Multiplexer circuit after applying correction | 3               | 7              | 6uW(34% reduced) |

The results show that the timing violations have been corrected by the proposed system. Also, the power consumption of the proposed detector/correction system is reduced when compared with the existing detector/corrector system.

5. Conclusion

In this paper, a Razor flipflop based detector circuit was proposed. The proposed system is tested with ISCAS89 S27 benchmark circuit and 2x1 multiplexer circuits. The proposed detector/corrector...
system successfully detects and corrects both setup time and hold time violations. Hence, the faulty operation in digital circuits can be avoided using the detector/corrector system discussed. The advantage of the proposed detector/corrector system is, the power consumption is lesser than the existing system. The timing violation detector/corrector systems are useful in industrial circuits also.

References
[1] Roozbeh A, Khayrollah H, and Abdollah K 2016 A Simple and Reliable System to Detect and Correct Setup/Hold Time Violations in Digital Circuits IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS 63, 1682 - 1689
[2] Pei-Ci W, Martin D F W, Ivalio N, Sarvesh B, and Vidyamani P, 2014 On Timing Closure: Buffer Insertion for Hold-Violation Removal Proceedings of 51st ACM/EDAC/IEEE Design Automation Conference (DAC), San Francisco, CA, USA
[3] Mehrzad N, Bijan A, and Ali A-K 2014 Dynamic Flip-Flop Conversion: A Time-Borrowing Method for Performance Improvement of Low-Power Digital Circuits Prone to Variations IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, 23 2724 - 2727
[4] Erol K, Felix M and Walter S 2015 Matching Detection and Correction Schemes for Soft Error Handling in Sequential Logic Proceedings of Euromicro Conference on Digital System Design, Madeira, Portugal
[5] Chae K and Mukhopadhyay S 2014 A dynamic timing error prevention technique in pipelines with time borrowing and clock stretching IEEE Trans. Circuits Systems. 61 74 - 83
[6] Wen-Pin T, Chung-Han C, Shih-Hsu H, Shih-Chieh C, Yow-Tyng N, Chien-Yung C 2013 Low-Power Timing Closure Methodology for Ultra-Low Voltage Designs IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, November.
[7] Kao C.-C and Lin K.-C. 2013 Clock skew minimization with adjustable delay buffers restriction IEEE Int. Symp. Next-Generation Electron.
[8] Lim K.-H., Joo D., and Kim T 2013 An optimal allocation algorithm of adjustable delay buffers and practical extensions for clock skew optimization in multiple power mode designs IEEE Trans. Comput.-Aided Des. Integr. Circuits Sys. 32 392 - 405
[9] Takaaki O, Masanori H 2011 Setup Time, Hold Time and Clock-to-Q Delay Computation under Dynamic Supply Noise IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, E 94 A Issue 10, 1948-1953.
[10] Hamed A, Safar H and Massoud P 2010 Analysis and Optimization of Sequential Circuit Elements to Combat Single-Event Timing Upsets IEEE, Proceedings of 2010 IEEE International Symposium on Circuits and Systems, Paris, France.
[11] Su Y.-S., Hon W.-K., and Yang C.-C. 2010 Clock skew minimization in multi-voltage mode designs using adjustable delay buffers IEEE Trans.Comput.-Aided Des. Integr. Circuits Syst. 29 1921 - 1930
[12] Neeraja J 2015 Clock Tree Synthesis based on Wire length Minimization Algorithm International Journal of Current Engineering and Technology 5 1987-1989
[13] Emre S 2007 Exploiting Setup–Hold-Time Interdependence in Static Timing Analysis IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 26 1114 - 1125
[14] Peter A B 2015 Timing violation resilient asynchronous template IEEE International Symposium on Asynchronous Circuits and Systems.
[15] Ernst D, Sung Kim N, Das S, Pant S, Rao R, Pham T, Ziesler C, Blaauw D, Austin T, Flattner K, and Mudge T 2003 Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation Proceedings of the 36th Annual IEEE/ACM International Symposium on Microarchitecture. MICRO-36, San Diego, CA, USA.