A Programmable Frequency Divider with Wide Division Ratio and Input Frequency Range

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Abstract. A programmable frequency divider with wide input frequency and division ratio range is designed in 65nm TSMC RF CMOS technology and presented in this paper. By using the divider-by-2/3 chain, the division ratio of the whole programmable frequency divider covers from 256 to 510. By simulation in Cadence environment, the results show that the programmable frequency divider works correctly when the input frequency varies from 0.2 GHz to 8.8 GHz.

1 Introduction
With the emergence of various wireless communication modes, integrating multiple communication modes on one mobile terminal has become a trend in the development of wireless communication technology. Radio frequency transceivers supporting multi-mode and multi-standard have become a hot research topic. As an important module of the RF transceiver front-end, the frequency synthesizer not only determines the performance of the entire transceiver, but also is one of the keys to achieve the integration of multi-mode and multi-standard wireless transceivers. Many scholars have made a thorough research about multi-mode multi-frequency broadband frequency synthesizers [1-3] which is indispensable in a multi-mode RF transceiver.

The programmable frequency divider as a critical module in multi-mode multi-frequency frequency synthesizers, is required to work under the broadband and high frequency. There are two typical structure of programmable frequency divider: P/S counter structure based on dual-mode prescaler technology[4-6] and divider-by-2/3 cascade structure. Compared with P/S counter structure based on dual-mode prescaler, divider-by-2/3 cascade structure is characterized in that only the first stage unit operates at the highest frequency, and the operating frequency of the latter stage circuit gradually decreases. There is no long delay loop in the entire frequency divider chain, and the feedback path exists only in the adjacent between the two units. in addition, the circuit is composed of the same module, so the reusability is good.

2 Circuit design
2.1 Overall structure of the programmable integer divider
The overall structure of the programmable frequency divider is shown in Figure 1, including a divider-by-2 cell, a CML-TO-CMOS module and a traditional divide-by-2/3 chain. A divider-by-2 cell is added in front of the divide-by-2/3 chain as a prescaler. The divide-by-2/3 chain is composed of 7-Stage divide-by-2/3 cells ,and a signal modout is fed back to the modin of the former stage by each divider cell to control the division ratio to be two or three. The division range(DR)[7] of divide-by-2/3 chain is revealed by equation(1):

\[ DR = 2^n + P_0 + 2P_1 + 2^2P_2 + \cdots + 2^{n-1}P_{n-1} \]  

(1)
Where $P_0, P_1, \ldots, P_{n-1}$ are the control words of each cell, and $n$ is the total number of divide-by-2/3 cells. Obviously we can conclude from Equation (1) that the division ratio range of traditional divide-by-2/3 chain is $2^n - 1$ and specifically in this design is 128–255.

2.2 Divider-by-2

Figure 2 shows the topology diagram of Divider-by-2 constructed by two D-latches employing the source coupled logic (SCL) structure which has very high working frequency. The circuit of D-latch based on SCL is shown in Figure 3. It consists of two sample devices (M1, M2), two hold devices (M3, M4), two control transistors (M5, M6), and a tail current transistor (M7). When CLK is high, M5 turns on and M6 turns off and the latch is in the sample state. M1 and M2 sample the input signal and amplify it to the output. When CLK goes low, it changes to latch state, M5 turns on and M6 turns off, and M1 and M2 are inactive. The cross-coupling transistors M3 and M4 form a positive feedback latch and output the signal. With the resistance load, the maximum and minimum output voltage is $V_{DD}$ and $V_{DD} - I_s$ where $I_s$ is the bias current of tail transistor. There is a remarkable fact that the total delay of the circuit is the sum of the two D-latches’ delay depending on the output resistance and capacitive load. Respectively, we can reduce the $R_L$ and the size of M1, M2 to increase the working frequency. However it will cause the decrease of gain and output swing. So a compromise should be considered here.
In order to improve the stability of the high-speed divider-by-2, reduce its load capacitance and increase the driving capability, a buffer is added following the divider-by-2. The buffer should be designed to minimize the input capacitance and provide a sufficient output swing for the next stage. As is shown in Figure 4, a common-source differential amplifier is used as a buffer which is often used in RF circuits, mainly due to its high operating frequency, deterministic output impedance and character in suppression of common-mode interference.

![Common-source differential amplifier buffer.](image)

Figure 4. Common-source differential amplifier buffer.

We often use the input sensitivity curve to consider characteristics of a divider. A typical input sensitivity curve of divider-by-2 based on SCL structure is shown in Figure 5. It should be noted that when the input frequency is twice of the self-resonant frequency, the required input amplitude is the smallest. This phenomenon can be understood from the perspective of injection locking. When the divide-by-2 is near the self-resonant frequency, the input signal can be locked with a small amplitude, and the larger distance from the self-resonant frequency, the larger input amplitude is needed. At low frequencies, the input amplitude must be large enough so that the transistors can be completely turned on or off, otherwise the sampling tube and the cross-coupling tube will be turned on at the same time and the circuit cannot be divided correctly. At high frequencies, the sharp increase in the minimum input amplitude is mainly limited by the maximum operating frequency of the divider. Since the charge-discharge time constant of the output node is close to the signal period at high frequencies, the output swing cannot be sufficient.

![A typical input sensitivity curve of divider-by-2.](image)

Figure 5. A typical input sensitivity curve of divider-by-2.

2.3 Divider-by-2/3

As is shown in Figure 6, the divide-by-2/3 cell[8] is constructed by four D-latches and three AND-gates. It consists of two parts, one is the prescaler logic, and the other is end-of-cycle logic. The division ratio is determined by prescaler logic under the control of end-of-cycle logic. As is presented in Table...
1, the divide-by-2/3 cell will be divided by 3 when control signal P and modin are both high. It will be divided by 2 in other case. The programmable frequency divider operates as follows: the modin of the last unit will be given a constant logic high signal. When the division ratio of divider-by-2/3 is 3, it will swallow one additional input cycle. So the input frequency is gradually stepped down by the divider chain, with the power consumption gradually reduced.

The D-latch used in the divide-by-2/3 cell can be CMOS static logic, true single phase clock (TSPC) logic, and current mode logic (CML). In this work we used the TSPC logic to reduce the power consumption. It should be noted that the AND-gates in Figure 6 will increase the delay, resulting in the decrease of working frequency. To solve this problem, the AND-gates are merged in the TSPC logic D-latches. Figure 7 shows the circuit of the divide-by-2/3 cell in this design.

| input | Division ratio |
|-------|----------------|
| P&modin = 0 | 2 |
| P&modin = 1 | 3 |

Figure 7. Circuit of divide-by-2/3 cell based on TSPC.

2.4 CML to CMOS Module

The divide-by-2 outputs a differential signal, while the input of divider-by-2/3 requires a single-end signal. So a CML to CMOS module is added between the two stages. The circuit is shown in the Figure 8. The first stage is a differential amplifier but the output signal still does not reach the full swing. Therefore, a two-stage push-pull inverter is connected to it. A large resistor is connected across
the input and output of the first inverter, which provides a negative feedback, forcing the output dc operating point to be fixed near the threshold voltage.

![CML to CMOS module](image)

**Figure 8.** CML to CMOS module.

### 3 Post-simulated Results

The simulation is performed in a cadence environment. When the input of divider-by-2 is added to a dc voltage, a self-resonant waveform is generated, and the self-resonant frequency is 2.58GHz. Figure 9 shows the self-resonant waveform. By the simulation, the result shows the divider-by-2 can work correctly in a wide range of input frequency from 200MHz to 8.8GHz when the input voltage swing is 200mv Vp. Figure 10 shows the transient waveforms at the condition when input frequency is 8.8GHz. In Figure 10, the first waveform is the input signal and the second waveform is output signal.

![Self-resonant waveform](image)

**Figure 9.** Self-resonant waveform.

![Transient waveforms of divider-by-two](image)

**Figure 10.** Transient waveforms of divider-by-two.
The simulation results of the whole programmable frequency divider are presented in Figure 11. The range of division ratio is from 255 to 510. As is shown in Figure 11(a),(b), when the input signal frequency is 8.8GHz and set the division ratio to 255 and 510. The divider can work correctly in both conditions. In Figure 11, the first waveform is the input signal and the second waveform is output signal.

![Division ratio is 256](image1)

![Division ratio is 510](image2)

Figure 11. Transient waveforms of programmable frequency divider

4 Conclusion
A programmable frequency divider based on divider-by-2/3 chain in standard 65nm TSMC RF CMOS technology is presented in this paper. The simulated results show the programmable frequency divider can work correctly when input frequency varies from 0.2GHz~8.8GHz. The division ratio range can be 256~510. Moreover, the power consumption is 3.1mA, when working at the maximum input frequency drawn from the 1.2V supply.

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