A 15 W wireless power receiver with an improved full-wave synchronous rectifier

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Abstract: This paper presents a 15 W wireless power receiver, which integrates an improved full-wave synchronous rectifier. In order to improve the system efficiency, two auxiliary MOSFETs are proposed to balance the conduction losses and the switching losses, and a digital pulse width controller is proposed to compensate the turn off delay to prevent the reverse leakage current. The chip was fabricated with TSMC 0.18 µm 1 poly 5 metal BCD technology with an active area of 3.2 mm × 4.8 mm, and the measured performance of the system efficiency from the DC input of transmitter to the output of the receiver is achieved 88% at 12 V/1 A output.

Keywords: wireless power receiver, full-wave synchronous rectifier, digital pulse width controller

Classification: Integrated circuits

References

[1] C.-Y. Liou, et al.: “Wireless-power-transfer system using near-field capacitively coupled resonators,” IEEE Trans. Circuits Syst. II, Exp. Briefs 63 (2016) 898 (DOI: 10.1109/TCSII.2016.2535042).

[2] Y.-H. Lam, et al.: “Integrated low-loss CMOS active rectifier for wirelessly powered devices,” IEEE Trans. Circuits Syst. II, Exp. Briefs 53 (2006) 1378 (DOI: 10.1109/TCSII.2006.885400).

[3] C. Peters, et al.: “A CMOS integrated voltage and power efficient AC/DC converter for energy harvesting applications,” J. Micromech. Microeng. 18 (2008) 104005 (DOI: 10.1088/0960-1317/18/10/104005).

[4] J. T. Hwang, et al.: “21.8 An all-in-one (Qi, PMA and A4WP) 2.5 W fully integrated wireless battery charger IC for wearable applications,” IEEE International Solid-State Circuits Conference (ISSCC) (2016) 378 (DOI: 10.1109/ISSCC.2016.7418065).

[5] K. Agarwal, et al.: “Wireless power transfer strategies for implantable bioelectronics,” IEEE Rev. Biomed. Eng. 10 (2017) 136 (DOI: 10.1109/RBME.2017.2683520).
1 Introduction

Wireless power transfer (WPT) is wildly used in recent years [1, 2, 3, 4], which has a wide range of applications such as biomedical implants [5, 6] and battery chargers of portable electronic devices [7] and electric vehicles [8]. Mobile phones such as Apple and Samsung have already integrated the wireless power receiver, and the receive power has reached 7.5 W to 10 W level, and it will inevitably trend to 15 W or even larger soon. Until now, most of the WPT applications used in mobile phone are inductively coupled power transfer (ICPT), and most of them are compatible with “Qi” standard. According to the power level, the “Qi” standard classifies the wireless products as baseline power profile (≤5 W) and extended power profile (up to above 30 W). And the “Qi” also specifies the power adjustment methods according to different types of coils. The common method is the dynamic frequency control method, and it specifies the working frequency range, such as from 110 KHz to 205 KHz. Therefore, the power transferring from the transmitter to the receiver can be changed and controlled through changing the working frequency. While from the perspective of the synchronous rectifier in the receiver, the power losses include the conduction losses, the switching losses, and the reverse leakage current. The reverse leakage current is caused by the turn-off delay of the Power MOSFETs, which would degrade the receiver efficiency and impact the overall system performance. The conduction losses depends on the on-resistance and the switch losses depends on the working frequency. And the turn-off delay is introduced by the comparators, logical circuit and drivers.

To improve the system efficiency, two methods are proposed in this paper. Firstly, two auxiliary MOSFETs are proposed to supplement the high-side MOSFETs in the rectifier to balance the conduction losses and the switching losses; secondly, a digital pulse width controller is also proposed and used in the
rectifier to compensate the turn off delay, which effectively prevent the reverse leakage current.

2 Architecture of the wireless power receiving unit

The system architecture of the proposed wireless power receiver is shown in Fig. 1. The wireless power is transferred from the transmitter to the receiver through the inductive coupling of the coils. Then the receiver rectifies the AC power to DC power and provides a DC output to the load. The efficiency of the rectifier has a large impact on the system performance. In this section, we firstly describe the power losses in the rectifier, and then introduce an optimized synchronous rectifier and introduce its realization of each blocks.

2.1 The power losses in the rectifier

In the rectifier, the power losses of the switching MOSFETs mainly include the conduction losses and the switching losses. The conduction losses depend on the on-resistance of the MOSFET, and depends on the width and length of the MOSFET. The on-resistance can be expressed as

\[
R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}.
\]

(1)

The switching losses mainly depend on the gate capacitor. When the MOSFET switch on or switch off, the driver has to charge or discharge the gate capacitor. We use \(Q_g\) to represent the total charges, and then the switching delay time can be simplified as

\[
t_d = \frac{Q_g}{I_g}.
\]

(2)

So the switching losses can be written as

\[
P_{\text{switch-loss}} = IV_{in} \frac{Q_g}{I_g} F_{SW}.
\]

(3)

Here, \(I_g\) is the current charge to the gate, and \(F_{SW}\) is the working frequency. In addition, when the driver circuit drives the Power MOSFET on or off, it has to supply the total charges to the gate capacitor, but it is dissipated at the driver circuit, so the drive losses are also a kind of power losses and can be expressed as
Here, $V_{drv}$ is the drive voltage.

The output capacitive losses are also a kind of power loss, we use $C_{oss}$ to represent the output equivalent capacitance, and the capacitive loss can be expressed as

$$P_{coss} = \frac{C_{oss} V_{in}^2 F_{sw}}{2}. \quad (5)$$

So the total power loss of the Power MOSFET is

$$P_{loss} = I_{rms}^2 R_{on} + IV_{in} \frac{Q_g}{I_g} F_{sw} + V_{drv} Q_g F_{sw} + \frac{C_{oss} V_{in}^2 F_{sw}}{2} \quad (6)$$

### 2.2 An optimized synchronous rectifier

The introduction above indicates that, besides the conduction losses, the rest of the items in Eq. (6) are in proportion to the working frequency. And from the aspect of the “Qi” standard, the working frequency of the WPT is dynamically changing. To improve the efficiency of the rectifier, we apply two auxiliary power MOSFETs (MOS5 and MOS6) to balance the conduction losses and the switching losses. The working mode of the two auxiliary power MOSFETs depend on the working frequency. When the working frequency is lower than a set value, the two auxiliary power MOSFETs are parallelly connected to the two high-side power MOSFETs respectively, as shown in Fig. 2(a). And when the working frequency is higher than the set value, the two auxiliary Power MOSFETs work as passive diodes as shown in Fig. 2(b). The main size of the MOSFETs in the rectifier are listed in Table I.

| MOSFET  | Length | Width | Total.m | Total.width |
|---------|--------|-------|---------|-------------|
| MOS1, MOS2 | 900 nm | 276 µm | 282     | 77.832 mm   |
| MOS3, MOS4 | 900 nm | 330 µm | 320     | 105.6 mm    |
| MOS5, MOS6 | 900 nm | 276 µm | 94      | 25.944 mm   |

As shown in Fig. 2, the power MOSFETs in the rectifier are controlled by a synchronous controller. The architecture of the proposed synchronous controller is shown in Fig. 3, and it is used to generate the bidirectional non-overlapping clocks according to the polarity of the received AC input signal. The synchronous controller is composed of several parts, including two low-side voltage comparators (L_Comp1 and L_Comp2), two high-side voltage comparators (H_Comp1 and H_Comp2), two digital pulse width controllers (DPW1 and DPW2), a frequency comparator (Fre_Comp), and a non-overlapping clocks generator.

The high-side comparators are used to compare the input AC signal with rectified voltage RECT and the low-side comparators are used to compare the input AC signal with ground voltage. The output of those voltage comparators are the main input signals of the non-overlapping clocks generator.
The proposed digital pulse width controller, shown in Fig. 3, is used to control the maximum effective pulse width of the synchronous rectifier. Because unlike the passive diodes, the current flow the MOSFETs are bidirectional. If the timing of turning on and turning off the MOSFETs are not controlled correctly, especially the turn-off delay introduced by the comparators, logical circuit and MOS drives, the current may flow from the DC output to the AC input, and this reverse leakage current severely degrades the power conversion efficiency [9, 10]. While the turn-on delay will not cause any reverse leakage current, we do not need to consider this problem.

Fig. 2. The auxiliary Power MOSFETs work as (a) active diodes (b) passive diodes.

Fig. 3. The synchronous controller.

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The timing diagram of the proposed digital pulse width controller is shown in Fig. 4. It uses the previous AC signal high-level width to generate a high pulse in the current AC cycle, and the high pulse output is shorter than the previous AC
signal high-level width. Before the AC signal is changed from the high level to the low level, the high-pulse signals through the non-overlapping clocks generator control the relevant high-side power MOSFETs to shut off. It could effectively eliminate the turn-off delay of the MOSFETs, and prevent the reverse leakage current and improve the system efficiency.

![Fig. 4. Timing diagram of the digital pulse controller.](image)

The proposed frequency comparator uses a high frequency clock to count the AC signal period. When the AC signal period is larger than a set value, the output of the clocks CLK_N5 and CLK_N6 are equal to CLK_N1 and CLK_N2 respectively, which means that the auxiliary power MOSFETs work as the active diodes. And when the AC signal period is shorter than the set value, the output of the clocks CLK_N5 and CLK_N6 are low, which means that the auxiliary power MOSFETs work as the passive diodes.

The diagram of the non-overlapping clocks generator is illustrated in Fig. 5. The input signals get from the output of the high-side voltage comparators, the low-side voltage comparators, the digital pulse width controllers, and the frequency comparator. The output signals of CLK_N1, CLK_N2, CLK_N3, CLK_N4, CLK_N5, and CLK_N6 are non-overlapping clocks, which are used to control the relevant MOSFETs turn-on and turn-off to achieve a synchronous full wave rectifier. The timing diagram of the synchronous rectifier is illustrated in Fig. 6. Here, f1, f2 and f3 represent different working frequency, and f1 and f3 are lower than the set value, so CLK_N5 and CLK_N6 are equal to CLK_N1 and CLK_N2.

![Fig. 5. The diagram of the non-overlapping clocks generator.](image)
respectively. And $f_2$ is higher than the set value, so the output of the clocks CLK_N5 and CLK_N6 are low.

3 Measurement results

The chip is fabricated with the TSMC 0.18 µm 1 poly 5 metal BCD technology which occupies 3.2 mm $\times$ 4.8 mm and the microphotograph of the chip is shown in Fig. 7. Fig. 8 shows the measured power efficiency of the wireless power system,
The output voltage is 12 V, and the output current is swept from 0.1 A to 1.25 A. The peak power efficiency of the system is 88% at 12 V (output voltage)/1 A (output current).

Table III summarizes the performance of this wireless power receiver and presents a comparison with the state-of-the-art, showing the effectiveness of the proposed structure with comparable system efficiency [4, 7, 11]. It shows the maximum output power of this wireless power receiver could reach 15 W, which is the largest output power listed in Table III, and the highest efficiency.

![Output Current VS Efficiency](image)

Fig. 8. The measured power efficiency of the wireless power system.

### Table II. The main parameters of this wireless power transfer system.

| Parameter                  | Transmitter | Receiver |
|----------------------------|-------------|----------|
| Coil Inductance (µH)       | 10.3        | 10.6     |
| Resonant Capacitance (nF)  | 247         | 204      |
| Resonant Frequency (KHz)   | 100         | 108      |
| Vertical Dimension (mm)    | 4           | 4        |
| Operation Frequency (KHz)  | 110–205     | /        |
| Input Voltage (V)          | 12          | /        |

### Table III. Performance summary of the wireless power receiver system.

| Reference     | [4] | [7] | [11] | This work |
|---------------|-----|-----|------|-----------|
| Technology    | 0.18 µm BCD | N/A | 0.18 µm CMOS | 0.18 µm BCD |
| Working Frequency (KHz) | 100–300 | 100–200 | 100–150 | 110–205 |
| System Efficiency (%) | 63 @2.5 W | (68–72) @ (2.5–5) W | 82 @ peak | 88 @ 12 V, 1 A |
| Lp (µH)       | N/A | N/A | 12.8 mH | 10.3 µH |
| Cp (nF)       | N/A | N/A | 12.8 mH | 10.3 µH |
| Ls (µH)       | N/A | N/A | 400 µF | 10.6 µH |
| Cs (µH)       | N/A | N/A | No Cs | 204 nF |
| Output Voltage (V) | 3.5–5 | 5 | 1.2 | 12 |
| Max Output Power (W) | 2.5 | 5 | 224 µW | 15 |
| Die area (mm²) | 5.83 | N/A | 0.7 ± 0.7 | 3.2 ± 4.8 |

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4 Conclusion

This paper presents a wireless power receiver with an improved full-wave synchronous rectifier. Two methods are proposed to improve the rectifier efficiency: two auxiliary MOSFETs are introduced to balance the conduction losses and the switching losses, and a digital pulse width controller is also introduced to compensate the turn-off delay, which effectively prevents the reverse leakage current. The proposed methods used in the receiver lead to state-of-the-art performance with the receiver demonstrated about 88% efficiency from the output at 12 V, 1 A. From the curve of the efficiency VS output power, it has achieved the efficiency higher than 70% when the output current is above 0.2 A, and this extends the applications of the receiver in different produces.

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