Beyond Nernst Sensitivity of Ion Sensitive Field Effect Transistor based on Ultra-Thin Body Box FDSOI

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Abstract. This paper reports an ultrahigh-sensitive ISFET sensor that is developed using TCAD model of the industrial 22-nm ultrathin body and buried oxide (UTBB) fully depleted silicon-on-insulator (FDSOI) transistors. The modeling method is exploited by changing the potential surface charge depending on the electrolyte pH change and investigating how will it cause the threshold voltage shift of ISFET device and other transfer characteristic parameters. The properties of a user-defined material offered by Silvaco are exploited to simulate the electrolyte behavior. The parameters of silicon semiconductor material (i.e., energy bandgap, permittivity, affinity, and density of states) are set to reconstruct an electrolyte solution. The electrostatic solution of the electrolyte area is investigated by giving a numerical solution for the semiconductor equation inside this area. On the other hand, the strong electrostatic coupling between the front gate and the back gate of FDSOI devices provide an intrinsic signal amplification feature for sensing applications. Utilizing a layer deposited Titanium dioxide (TiO2) as a pH sensing film, pH sensors having a sensitivity ~1250 mV/pH is reported. The small sensing area and the FDSOI-based technology of the device make the sensors ideal for the IoT market.

1. Introduction
CMOS-based micro-technology playing a crucial role in the field of chemical sensing applications. This has been enabled using solid-state sensors that can be implemented in planar form and manufactured using CMOS technology to integrate on a single chip monolithically. Now, this provides an opportunity for chemical sensing platforms to leverage semiconductor technology that may offer advantages such as scalability, miniaturisation, fabrication, and integration with intelligent instrumentation ISFET sensors are the most promising and may satisfy all these opportunities as well as scalability with the developing semiconductor fabrication. Due to its promising application in biological, biochemical and medical detection [1]–[5]., ISFET has received much interest since it was first reported by Bergveld in 1972 [6]. Particularly, much effort has been made to investigate pH-sensitive ISFETs with studies on device structures and pH-sensing membranes aimed at improving the sensitivity and stability of ISFETs [7], [8]. Different methods have been proposed to overcome the Nernst limit, including the use of new materials as sensing films or new structures for ISFET sensors. However, these methods still cannot surpass the limit [9]–[12]. The problem with the Nernst limit has been solved by Cho et al. (2012), who used DG ISFETs with the silicon-on-insulator (SOI) ISFET to beat the Nernst limit of 59.3 mV/pH [13],
[14]. The classical threshold coupling relation between the front and back gates of the thin-film SOI has been reinvestigated [15], [16].

From this relation, DG ISFET sensitivity can be investigated. However, the effect of decreasing ISFET sensing area (channel length) towards the new trend in nanotechnology still need to investigate. Sensing area also geometrical parameter may affect the ISFET sensing properties which not included in this relation. Additionally, the investigation of this relation with the ultra-thin body and box with the highest sensitivity need to validate. Therefore, in this paper, ultrahigh-sensitive and ultralow-power CMOS compatible pH sensors that are developed using previously developed TCAD model[17], of industrial 22-nm ultrathin body and buried oxide (UTBB) fully depleted silicon-on-insulator (FDSOI) transistors have been designed and simulated. Section 2 introduced the summary of our developed TCAD model and how to use silvaco TCAD for ISFET simulation and the description of capacitive coupling model which is utilized to validate our model by calculation the amplification factor. In section 3, the structure and simulation parameters used in this work have been introduced. Finally, the transfer characteristics and sensing properties result and discussions have been described in section 4.

2. Design and simulation methods

2.1. TCAD model

The major challenge is the electrolyte simulation in commercial TCAD because it is not equipped with models, materials, and electrochemical processes that manage ISFET process and its operations [18]. Therefore, our idea exploits the user-defined material property offered by Silvaco to simulate electrolyte solution [19]. The properties of a user-defined material offered by Silvaco are exploited to simulate the electrolyte (solution) behavior. The parameters of silicon semiconductor material (i.e., energy bandgap, permittivity, affinity, and density of states) are reconstructed in an electrolyte solution. Therefore, electrostatic solution of the electrolyte area can be investigated by giving a numerical solution for the semiconductor equation inside this area. Three types of materials are available in Silvaco Atlas, namely, semiconductor, insulator, and conductor. The procedure of defining a new material in Atlas (user-defined) specifies the material name, the user group it belongs to, and the last known atlas about the default material. When these parameters are set in their correct places in the Silvaco input deck code, we can change and manipulate the material properties using MATERIAL statements (i.e., permittivity, energy bandgap, affinity, and density of states) as following [19]:

\[
\text{MATERIAL MATERIAL=ELECTROLYTE USER.GROUP=SEMICONDUCTOR USER.DEFAULT=SILICON PERMITIVITY } = 80 \text{ EG300}=V_1 \text{ NC300}=V_2 \text{ NV300}=V_3
\]

Commercial TCAD allows users to introduce bias-dependent surface charges in the form of interface donor or acceptor traps. The challenge is simulating the updated surface charge density equation described by (16) in the electrolyte pH change model [20]. To introduce this equation to the simulator, interface trap statements are utilized to mimic the surface charge accurately, as follows [19]:

\[
\text{INTTRAP <type> E. LEVEL=} <r> \text{ DENSITY=} <r> \text{ <capture parameters>}
\]

“INTTRAP” activates interface defect traps at discrete energy levels within the bandgap of the semiconductor and sets their parameter values. Device physics has established the existence of three different mechanisms, which add to the space charge term in Poisson’s equation in addition to the ionized donor and acceptor impurities” [19]. Interface traps will add space charge directly into the right-hand side of Poisson’s equation. To calculate the trapped charge in Poisson’s equation, the total charge value is defined by the following:
\[ \sigma_0 = q(N_{tD}^+ - N_{tA}^-) \]  

where \( N_{tD}^+ \) and \( N_{tA}^- \) are the densities of ionized donor-like and acceptor-like traps, respectively. DENSITY and its probability of ionization are represented as \( F_{tA} \) and \( F_{tD} \), respectively. For donor-like and acceptor-like traps, the ionized densities are calculated by the following equations:

\[ N_{tD}^+ = \text{DENSITY} \times F_{tD} \]  
\[ N_{tA}^- = \text{DENSITY} \times F_{tA} \]  

where \( F_{tA} \) and \( F_{tD} \) are given by the following equations:

\[ F_{tA} = \frac{V_n \cdot \text{SIGN} \cdot n + e_{pA}}{V_n \cdot \text{SIGN} \cdot n + V_p \cdot \text{SIGP} \cdot p + e_{nA} + e_{pA}} \]  
\[ F_{tD} = \frac{V_p \cdot \text{SIGP} \cdot p + e_{nD}}{V_n \cdot \text{SIGN} \cdot n + V_p \cdot \text{SIGP} \cdot p + e_{nD} + e_{pD}} \]  

where \( \text{SIGN} \) is the carrier capture cross-sections for electrons and \( \text{SIGP} \) holes. The thermal velocities for electrons and holes are \( V_n \) and \( V_p \), respectively. For donor-like traps, the electron and hole emission rates, \( e_{nD} \) and \( e_{pD} \), are defined by the following [19]:

\[ e_{nD} = \frac{1}{\text{DEGEN.FAC}} V_n \cdot \text{SIGN} \cdot n \cdot e^{E_i - E_t/kT} \]  
\[ e_{pD} = \text{DEGEN.FAC} V_p \cdot \text{SIGP} \cdot n \cdot e^{E_i - E_t/kT} \]  

where \( E_t \) and \( E_i \) are the trap energy level and the intrinsic Fermi level position, respectively. DEGEN.FAC is the degeneracy factor of the trap center. All other modeling details are well described in previous work [21].

2.2. Capacitive coupling model

The shift in threshold voltage for conventional ISFETs is given by the following:

\[ \Delta V_T^{th} = -\Delta \psi_0. \]  

For the DG ISFET with an independently controlled separated DG, when the front-channel is depleted, the conventional top gate affects the threshold voltage of the DG transistor. Therefore, we can rewrite Eq. (3) as follows [14]:

\[ \Delta V_R^{th} = -C_{ox}/C_{Box} \Delta \psi_0 = C_{ox}/C_{Box} V_T^{th}, \]  

where \( V_T^{th} \) and \( C_{Box} \) are back-gate threshold voltage and capacitance, respectively. Therefore, DG ISFET pH-sensitivity can be improved by the ratio of the top oxide or sensing membrane capacitance to the bottom oxide, which is called buried oxide (Box) capacitance. The old version of capacitive coupling relation can thus be modified as follows [16]:

\[ \Delta V_T^{th} = -C_{ox}/C_{Box} \Delta \psi_0 = C_{ox}/C_{Box} V_T^{th}, \]
\[ V_{th}^B = \frac{3T_{ox,B}}{3T_{ox,T} + T_{Si}} V_{th}^T \]  

(10)

where \( T_{ox,T} \), \( T_{Si} \), and \( T_{ox,B} \) are the values of insulator oxide, top silicon body, and Box oxide thickness, respectively. Thus, pH-ISFET sensitivity by using the back gate can be amplified by the thickness ratio of these three parameters, and this ratio is called the ideal amplification factor.

2.3. Structure and simulation parameters

An ISFET device is simulated to check the suitability of the modeling procedure. The cross-section of the ISFET simulation structure is shown in Figure 1. The parameters required for the simulation are shown in Table 1.

![Figure 1. 2D Cross Section of DG ISFET](image)

**Table 1. TCAD Parameters of DG ISFET**

| Parameter                    | Value  | Unit       | Parameter                  | Value          | Unit   |
|------------------------------|--------|------------|-----------------------------|----------------|--------|
| BOX thickness                | 60     | Nm         | k                          | 1.380649×10^{-23} | J/K    |
| Body thickness               | 6      | nm         | S/D doping                 | \(10^{20}\) | cm\(^{-3}\) |
| Channel length               | 22     | nm         | T                          | 300            | K      |
| \( t_{electrolyte} \)       | 700    | nm         | Electrolyte concentration  | \(10^{-3}\)   | Mol/L  |
| \( t_{ox} \)                | 1      | nm         | Oxide permittivity         | 22 Ta\(_2\)O\(_5\) | -      |
| Electrolyte permittivity    | 80     | -          | \(V_{DS} \)                | 50             | mV     |
3. Results and discussion
The electrostatic behavior (transfer characteristics) of a conventional ISFET (SG ISFET) device is simulated. Drain to source current $I_{ds}$ versus the primary reference gate voltage $V_{Ref}$ at various pH values (pH=1 to 12) for TiO$_2$ Stern layer, as shown in Figure 2. The simulation parameters used are the same in Table 1, while the structure is conventional ISFET (SG). The $V_{Ref}$ in Figure 2 considers the primary gate (PG) of SOI ISFET rather than the back gate (BG). The observed increase in threshold voltage could be attributed to the increase in pH values. Furthermore, the threshold voltage ($V_{TH}$) shift according to pH scale change has been shown in Figure 3. As shown, $V_{TH}$ is slightly and stably increased when pH change from 1 to 12. Even when SG ISFET using higher specification material (TiO$_2$) as a sensing membrane and hit the Nernst limit sensitivity by 59.1 mV/pH as well as stable threshold voltage shift, however, handling the SG ISFET may become a challenge of it cannot exceed the Nernst sensitivity limit. Different methods have been proposed to overcome the Nernst limit, including the use of new materials as sensing films or new structures of ISFET sensors, but they still cannot exceed this limit.

![Figure 2. TCAD Simulated ID vs VRef. Characteristics for variety of pH scale for SG ISFET.](image)

![Figure 3. TCAD Simulation Threshold Voltage Shift for SG ISFET.](image)

Therefore, in this paper, the transfer characteristics of an FDSOI ISFET (DG ISFET) device is simulated. The $I_D$ versus back gate (BG) voltage for pH scale from 3 to 10 has been calculated using developed TCAD Atlas as shown in Figure 4. Additionally, the BG voltage shift according to pH change, is extracted as introduced in Figure 5. A shift in threshold voltage is clearly observable owing to the effect of the coupling and the amplification factor. Compared with SG transfer characteristics, the DG transfer characteristics have large shifts in threshold voltage and low drain current consumption, which is fully supported by DG SOI theory [15]. In addition to the amplification factor, the type of sensing membrane also contributes to the capacitive coupling relation. This result implies that the use of different high-k sensing membranes is not enough to overcome the Nernst limit unless the coupling ratio, which can amplify the SG threshold voltage, is used. Additionally, the advantages of commonly used high-k sensing membranes are clearer when DG rather than SG is used. Furthermore, designing of FDSOI ISFET with a small sensing area or small channel length can achieve ultra-highly sensitive device as described by the chart in Figure 6. Figure 6 introduces the validation of this work with Nernst theory in SG ISFET in one side, and with capacitive coupling model which described in section 2 for DG ISFET.
on the other side. As shown in Figure 6, this work was achieved 59.1 mV/pH sensitivity by the primary gate (PG) which hit the Nernst limit sensitivity (59.3 mV/pH) that commonly known in state of the art. Also, the BG sensitivity attains around ~1250 mV/pH sensitivity because of the amplification factor which multiplying by PG sensitivity [22]. That means the enhancement in sensitivity is amplified by ~21 times from SG sensitivity. For more validation, we used the Eq.10 for comparative achieved sensitivity (BG sensitivity) with the sensitivity calculated from capacitive coupling model, as shown in Figure 6.

Evaluated with state-of-the-art, the developed DG FDSOI ISFET exhibits superior sensitivity. Not only in terms of sensitivity, but this sensor also has remarkably better performances in terms of CMOS compatibility and scaling as it avoids the bulky reference electrode, as shown in Table 2.

Figure 4. TCAD Simulated ID vs VRef. Characteristics for variety of pH scale for DG ISFET.

Figure 5. TCAD Simulation Threshold Voltage Shift for DG ISFET.

Figure 6. Comparative Chart of Primary Gate (PG) and Back Gate (BG) of this work with Standard theoretical Models.
4. Conclusion
Titanium dioxide (TiO2) sensing membrane on industrial 22 nm channel length, UTBB FDSOI transistors and high sensitivity ISFET are designed and simulated in this work. We attain around ~1250 mV/pH sensitivity which is 21 times higher than SG sensitivity. This sensitivity achieves good agreement with theoretical models in term of primary and back gate sensitivities. By benchmarked this work with the state-of-the-art works, its peat the last work in terms of sensitivity as well as device scaling values. The advantages of commonly used high-k sensing membranes are clearer when DG rather than SG is used. Furthermore, body thickness not only influences sensitivity toward UTB, but it can also achieve UTBB as well as small sensing area by decreasing channel length. We anticipate that using 50 mV as supply voltage, ultra-high sensitivity and the small device can meet the new trend of biomedical sensors requirements.

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| Parameters | [23] | [24] | This work |
|------------|------|------|-----------|
| Sensitivity (mV/pH) | 453 | 775 | 1250.16 |
| Gate Reference Electrode | Control Gate | Reference Electrode |
| Substrate | SOI | FDSOI | FDSOI |
| Technology Node | 0.18 µm | 28 nm | 22 nm |
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