HyperLogLog Sketch Acceleration on FPGA

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Abstract—Data sketches are a set of widely used approximated data summarizing techniques. Their fundamental property is sub-linear memory complexity on the input cardinality, an important aspect when processing streams or data sets with a vast base domain (URLs, IP addresses, user IDs, etc.). Among the many data sketches available, HyperLogLog has become the reference for cardinality counting (how many distinct data items are in a data set). Although it does not count every data item (to reduce memory consumption), it provides probabilistic guarantees on the result, and it is, thus, often used to analyze data streams. In this paper, we explore how to implement HyperLogLog on an FPGA to benefit from the parallelism available and the ability to process data streams coming from high-speed networks. Our multi-pipelined high-cardinality HyperLogLog implementation delivers 1.8× higher throughput than an optimized HyperLogLog running on a dual-socket Intel Xeon E5-2630 v3 system with a total of 16 cores and 32 hyper-threads.

Keywords—Data-sketch; Cardinality; FPGA; HW Acceleration; HLS;

I. INTRODUCTION

Calculating basic statistics over large data collections is the first step in many data analytic procedures. Either as the direct result of user queries or as an initial step for other, more complex operations on the data, computing the cardinality, item frequency, distribution, heavy-hitters, or top-K elements are nowadays standard operations in both data streaming and as well as over distributed data processing engines. Item frequency, for instance, is essential to identify from a data stream recording web accesses how often individual web pages are accessed. Frequent items [1] are used to identify, e.g., the users that most frequently request a given service. Similarly, cardinality is used to, e.g., determine how many different users are utilizing a given service or how many distinct items are being bought from an e-shop given a list/stream of accesses or purchases.

Common to all these operations is the problem of space complexity. If the domain from where the data set is derived is very large (IP addresses, URLs, user IDs, items available from a catalog), a naive approach to counting becomes linear on the cardinality of the data set, and that might involve potentially millions or even billions of entries to keep track of. As a result, existing systems resort instead to approximation through several techniques collectively referred to as sketch algorithms [2]. These algorithms only provide estimates, rather than accurate counts, for a variety of statistics on the data, but they do so using a fixed amount of space. The algorithms provide well defined analytical bounds on the precision that will be reached as a function of the space used to perform the actual operation. These bounds involve relatively low error margins that are often acceptable when processing large data sets.

In this paper, we focus our attention on the cardinality problem, i.e., how to determine the number of distinct elements on a data collection. This function can be found in many data processing systems and network monitoring applications [3]. For instance, in SQL, it is used to implement COUNT(DISTINCT ...) that returns the number of distinct items in a column. Of the different ways to estimate the cardinality of a multiset, HyperLogLog (HLL) is nowadays the standard algorithm [4]. Google, for instance, uses HLL in BigQuery, a cloud-based distributed data processing system, to estimate the cardinality of data sets with several billion distinct items with errors lower than 1% [5].

In modern cloud and data center environments, the widely adopted separation of compute and storage often means that an operation such as calculating the cardinality of a data set involves reading the data from storage and forwarding it to the computing nodes. It follows that having the ability to perform HLL over streams of data would be very beneficial, especially if it can be done close to the network without involving the CPU, and avoiding expensive copying of the data to memory. With this in mind, we explore the implementation of HLL on an FPGA to benefit from both the inherent parallelism as well as its architectural flexibility. In the paper, we describe the implementation of HLL on an FPGA, how to parallelize it using multiple concurrent pipelines, and how it can be embedded in an FPGA-based Network Interface Card (NIC) supporting TCP/IP to perform the cardinality estimation directly on the network. The main contributions of the paper include:

1) A single-pipelined dataflow architecture implementing HLL on an FPGA with a performance improvement of 2× over the throughput reachable by a single-threaded CPU implementation.
2) A multi-pipelined parallel architecture of HLL with a performance improvement of 1.8× compared to the 16-cores, 32-thread CPU implementation.
3) A design embedding the HLL implementation on a NIC so that it can process data streams arriving through a 100 Gbit/s TCP/IP link. This design highlights the advantage of network-faced processing with FPGAs compared to doing the same operation on a CPU, where it becomes compute bound.

The rest of the paper is organized as follows: Section II provides an overview of background and related work. A detailed explanation of the HyperLogLog algorithm is presented in Section III. We profiled HLL with different data sets to decide on the parameters for hardware implementation. Comprehensive details on the profiled results are described by Section IV. Section V presents the proposed hardware architectures of HLL. The experiments and the results are discussed in Section VI followed by describing the network integration of HLL in Section VII. Finally, Section VIII concludes the paper.

II. BACKGROUND AND RELATED WORK

This work combines ideas from diverse fields of study: data sketch algorithms, specialized hardware solutions, and
in-network data processing.

A. Cardinality Estimation

Data sketch algorithms play an essential role in big data. Their goal is to obtain approximate, yet accurate statistics about the data with sublinear time or space complexity, or both. The statistics gathered by sketches can be used in approximate query processing [6] and are fundamental to perform query optimization [7]–[9] in database management systems (DBMS). Cardinality estimation is a family of sketching techniques that is often used in these mentioned scenarios, besides also being utilized in other diverse application areas such as network security [10], network size estimation [11], and data mining [12]. HyperLogLog [4] is known to be one of the best algorithms, achieving high accuracy over all cardinality ranges and being trivially parallelizable, leading to efficient scale-out implementations [3].

B. Specialized Hardware for Data Processing

Due to stagnating single-core performance in CPUs and the recent slowdown in technology scaling (described as a slowdown in Moore’s Law [13]), specializing hardware has become widespread to achieve high performance and efficiency in data processing systems. Prominent examples include Microsoft’s and Amazon’s deployment of FPGAs in their datacenters [14], [15], Google’s development of a specialized processor called Tensor Processing Unit [16], and Intel embedding FPGAs next to Xeon CPUs in the same package with a coherent interconnect [17].

Specialized hardware solutions to accelerate relational processing operators such as joins [18], [19], aggregation [20], and sorting [21] show increased performance and efficiency. István et al. [22] show that FPGAs can be used to build histograms without affecting the throughput. Kara et al. [23] show that robust and expensive hash functions can be implemented on an FPGA without any reduction in the processing rate, as opposed to performing these hash functions on a CPU. Tong et al. [24], [25] show Count-Min sketch acceleration and its application in high-speed networks.

Cardinality estimation algorithms can also be performed on the data path and most popular algorithms in this domain require robust hashing. Consequently, the FPGA-based implementation of HyperLogLog presented in this paper utilizes similar ideas but expands upon them by presenting an end-to-end cardinality estimation solution.

C. In-network Data Processing

As the datacenter network bandwidth keeps increasing, with 100 Gbit/s recently becoming the norm, the burden on CPUs to process data as quickly escalates. Besides offloading network processing to network interface card (NIC), there are also ongoing efforts to offload parts of the application logic to NICs to reduce the data processing burden of CPUs. Standalone FPGA platforms can also be used as NICs, thanks to efforts in developing FPGA-based TCP/IP [26] or RoCE [27] stacks. In an FPGA-based NIC, the remaining logic on the FPGA chip can be used to perform complex data processing tasks on the received or transmitted data. For instance, Microsoft uses this setup in their datacenters to, e.g., accelerate the Bing search engine [14] or perform low-latency neural network inference [28].

| Table I: 4-bit hash values. |
|-----------------------------|
| 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 |
| 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |

Creating sketches as the data is received from the network can be useful for multiple reasons: (1) The FPGA is better suited to perform complex data processing tasks with high throughput. It can match the 100 Gbit/s line rate when creating the sketch. (2) The FPGA creates the sketch as the data is received, it is practically “for free”. This frees up the CPU to perform other tasks. We integrate our FPGA-based HLL implementation next to an FPGA-based TCP/IP stack to estimate the cardinality at line-rate.

III. HyperLogLog

The HyperLogLog (HLL) sketch is used to determine the cardinality of large multisets without the necessity of storing every data item. It uses hash-based data randomization to approximate this cardinality. The algorithm monitors the maximum leading zero counts of the encountered hash values. Hash values with more leading zeros are less likely. So, their observation indicates a higher cardinality. The hashing algorithm is assumed to produce uniformly distributed hash values.

To understand HLL, assume that the hash function randomly draws the binary representation of a number from the range $[0:15]$ as listed in Table I. If every hash value occurs with the same probability, we observe the following: the probability that the hash has at least one leading zero is 50% ($1/2$); the probability of the hash having at least two leading zeros is 25% ($1/4$); the probability of the hash containing at least three leading zeros is 12.5% ($1/8$), and the probability of the hash containing four leading zeros is 6.25% ($1/16$). Statistically speaking, around 8 elements hashing to different values are needed before encountering a hash starting with three leading zeros. Generalizing, we need to see around $2^k$ elements to observe a hash containing $k$ leading zeros. Conversely, if a maximum of $k$ leading zeros has been seen, one has probably processed $2^k$ different elements. This is the main intuition behind HLL. However, if based on a single measurement, this approach results in a large variance of the estimated cardinality. This is the case, e.g., when we observe a large number of leading zeros in a hash value very early.

The estimation variance, and hence the expected estimation error, is reduced by stochastic averaging [29]. For this purpose, the hash value is divided into two parts: (a) a short bucket index $i$ and (b) a remaining hash $w$. The bucket index splits the stream into disjoint substreams. For each one of them, a designated counter $M[i]$ is maintained that tracks the maximum rank $\phi(.)$ so far observed in the associated subset of hashes where the rank $\phi(w)$ is the number of leading zeros in $w$ plus one. This approach of averaging observations across buckets reduces the error that random occurrences produce.

At any point in time, the cardinality can be estimated by taking the harmonic mean of the estimates implied by the individual bucket ranks. This estimate comes with a standard error. The HLL standard error is $\frac{1}{\sqrt{m}}$ with a space complexity of $O(\varepsilon^{-2}\log n + \log m)$ in the data streaming $(\varepsilon, \delta)$-model [30], [31], where $\varepsilon$ is the confidence parameter, $\delta$ is the approximation parameter of the data stream, and $m$ is the number of buckets.
A practical variant of the original HLL \cite{4} is shown as Algorithm 1. It has four phases:

1) **Hashing**: Every data item from the data stream (multiset) is hashed using a hash function that produces a 32-bit hash value.

2) **Initialization**: Depending on the chosen value of \( p \in [4:16] \), a constant \( \alpha_m \) with \( m = 2^p \) is calculated as listed in line 3 of Algorithm 1. This constant will be used for bias correction. The array \( M[0:m-1] \) of bucket counters is initialized to all 0.

3) **Aggregation**: The first \( p \) bits of each hash value act as an index \( i \) to divide the data stream \( S \) into \( m \) substreams \( S_i \). They identify the associated bucket counter \( M[i] \). The remaining bits \( w \) of the hash value are subjected to the rank computation \( \varrho(w) \). The associated bucket counter will be updated to the maximum of its current value and this newly determined rank. Ultimately, this yields:

\[
M[i] = \max_{w \in S_i} \varrho(w)
\]

4) **Computation**: A raw cardinality estimate is obtained as the product of the harmonic mean of the individual substream cardinality estimates \( 2^{M[i]} \), the substream count \( m \), and the bias correction \( \alpha_m \). To compensate a systematic overestimation of small cardinalities, the algorithm reverts to \texttt{LinearCounting} in these cases as shown in line 15. Intermediate ranges of cardinalities require no correction (line 17). However, when the data set approaches large cardinalities on the order of \( 10^9 \), the 32-bit hash function is increasingly unable to differentiate data items due to hash collisions. The correction of line 22 tries to mitigate this effect.

A hash function producing \( H \)-bit hash values can distinguish at most \( 2^H \) data inputs. So, hash collisions are imminent if the cardinality of the data set approaches \( 2^H \). Fortunately, the memory footprint of HLL does not grow linearly with \( H \). The memory requirements for HLL are determined by the number of buckets and the maximum rank \( \varrho(.) \). For an \( H \)-bit hash function and a precision \( p \), we obtain:

\[
\varrho(.) \leq H - p + 1 \tag{2}
\]

\[
B = 2^p \cdot \log_2(H - p + 1) \tag{3}
\]

Switching from a 32-bit to a 64-bit hash function boosts the accuracy of estimating large cardinalities significantly. Typically, 64-bit hash functions are used to estimate multisets of cardinalities beyond 1 billion \cite{3}. This modification increases the necessary size of each counter by one bit only. Note that this choice renders the large range correction obsolete for all conceivable practical multiset cardinalities.

The accuracy benefits of choosing a 64-bit hash function are obtained at the cost of an approximately doubled compute effort as compared to a 32-bit hash function. In a compute-bounded setting, as on a CPU, this translates into a corresponding reduction of the processing rate. On the other hand, the HLL algorithm is structurally simple enough to quickly become I/O-bound on an FPGA platform. Hence, the accuracy gain can be easily realized by expanding in fabric space rather than by sacrificing throughput. In the next section, we profile the HLL algorithm from a statistical perspective, showing the necessity for a 64-bit hash when approaching high cardinalities.

**IV. HYPERLOGLOG PROFILING**

We profile the HLL algorithm to evaluate its statistical properties. This profiling is independent from any particular platform-specific implementation. We explore the parameter space \( \{p, H\} \in \{14,16\} \times \{32,64\} \) using synthetic data sets. The data sets are generated by randomly sampling the range \([0:2^{32}-1]\). The input sequence is hashed using the Murmur3 hash function \cite{32} of the respective bit width.

The standard error for HLL (of different hash sizes) with \( p = 14 \) is depicted in Fig. 1(a). We consider the maximum, minimum, and median of the standard errors obtained from multiple data points. Clearly, the 32-bit hash HLL estimates the cardinality within reasonable error bounds for cardinalities
The initiation interval is defined as the number of clock cycles up to $10^8$. For data sets with larger cardinalities, the standard error quickly grows beyond 30%, which is often not acceptable anymore. HLL reverts to LinearCounting for cardinalities below a threshold of $\frac{1}{2} \cdot m$. The transition between the estimation schemes occurs at about $40k$ for $p = 14$. This location is identified by a local increase of the observed maximum estimation error of up to 5%. These error curves are similar to the results reported by Heule et al. [3].

To sustain the cardinality estimation beyond $10^8$, we increased the hash size from 32 to 64 bits. This results in a significant reduction of the standard error. To reduce the standard error further, we increased the precision to $p=16$. Fig. 1(b) shows the corresponding standard error variation. A 32-bit hash achieves a standard error less than 2% for all data sets of a cardinality below $10^8$. However, the standard errors surge quickly above 35% beyond this point. In the case of the 64-bit hash, the standard error remains close to 1% for the whole cardinality range. It is to be noted that the theoretical average standard error of HLL is given by $\sqrt{\frac{H}{p}}$. With $p = 16$, the expected standard error is 0.41%. The average standard error of our experiments shown in Fig. 1 stays below this expected average.

Table II summarizes the memory requirements for the explored parameter settings as obtained from (3). Observe that the corresponding standard error variation. A 32-bit hash achieves a standard error less than 2% for all data sets of a cardinality below $10^8$. However, the standard errors surge quickly above 35% beyond this point. In the case of the 64-bit hash, the standard error remains close to 1% for the whole cardinality range. It is to be noted that the theoretical average standard error of HLL is given by $\sqrt{\frac{H}{p}}$. With $p = 16$, the expected standard error is 0.41%. The average standard error of our experiments shown in Fig. 1 stays below this expected average.

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Table II: HyperLogLog memory footprint.

| $p$ [bits] | 14 | 16 |
|-----------|----|----|
| $H$ [bits] | 32 | 64 |
| $\log_2(H-p+1)$ | 5  | 6  |
| $\log_2(H-p+1)$ | 5  | 6  |
| Total memory [KiB] | 10 | 12 |

TABLE II: HyperLogLog memory footprint. The pipeline structure encompassed in blue dashes in Fig. 2 forms the aggregation phase of the HLL algorithm. It processes the incoming data, received from an AXI4 stream interface, tracking the maximum ranks of the substreams in on-chip Block RAM (BRAM). Once all data items have been processed, the buckets module starts forwarding the counter values. This marks the hand-over to the computation phase of the HLL algorithm.

1) Hash Function: We use a 64-bit Murmur3 hash [32] to randomize the 32-bit input data. Murmur3 is a non-cryptographic hash function that is simple to implement while guaranteeing a uniform distribution of hash values [34]. The math and logic (multiply and rotate) operations of the hash function are mapped to the dedicated Digital Signal Processing (DSP) slices [35] of the FPGA. A DSP slice contains pipeline registers to enhance the speed and efficiency of the application. The data flow engine takes advantage of the parallelism offered by the reconfigurable logic by inferring multiple DSP resources and schedules the math operations in a pipeline structure.

2) Index Extractor: The index extractor module is fed with the 64-bit hash values. It extracts the first 16-bits of the hash as an index to identify the corresponding counter. The remaining 48-bits are forwarded to the leading zero detector.

3) Leading Zero Detector: This module determines and forwards the count of leading zeros. It leverages the efficiently synthesizable CountLeadingZero member function of the variable-width integer data type ap_uint<N> provided by the Vivado HLS libraries.

4) Buckets: The bucket counters are mapped onto dual-port BRAM [56] modules of the FPGA. The counters maintain the maximum ranks encountered for their respective buckets. The potential counter update is pipelined itself, first (a) reading the counter value identified by the extracted index, then (b) comparing it to the new computed leading zero count, and, finally, (c) updating the stored maximum if a larger rank has been encountered. Updates to the same counter that arrive during this read-modify-write cycle are merged.

5) Zero Counter and Bypass: This is a pass-through module forwarding the aggregated ranks to the harmonic mean computation. While doing so, it determines the number $V$ of counters that have remained unchanged at a value of zero.

6) Harmonic Mean: This module computes the harmonic mean of the aggregated ranks. Observe that the corresponding summation kernel accumulates powers of two, particularly $2^{-M[j]}$. Thus, these addends can be formed easily from a 1-hot code asserting the corresponding binary fractional bit. They are accumulated onto an arbitrary-precision fixed-point data type of the HLS library [37] with $m$ binary integer digits and $H+p+1$ binary fractional digits to attain an exact sum. After processing all aggregated ranks, the raw cardinality estimate $E$ is computed using HLS-synthesized floating-point arithmetic.

![Fig. 2: A single-pipelined HyperLogLog dataflow engine.](image-url)
7) **Correction:** The correction module replaces small raw HLL cardinality estimates $E$ by estimates obtained through linear counting. This small range correction is triggered when the raw estimate falls below the threshold $E \leq \frac{3}{2} m$ and empty buckets have been observed, i.e. $V \neq 0$. The number of empty buckets serves as an input to the linear counting computation. Using a 64-bit hash function, a large range correction is not required. The final cardinality estimate achieves an accuracy with a typical standard error below 2%.

**B. Parallel Architecture**

As shown in Fig. 3, the HLL aggregation phase can be trivially parallelized into $k$ independent but otherwise identical aggregation pipelines. This allows to scale the input bandwidth of the computation perfectly to $k \times 32$-bit words per cycle at the cost of additional FPGA resources. The input data is simply sliced to feed the individual pipelines. Slicing the multi-word input only implies wiring for the actual data and minimal handshaking with the pipeline inputs. Inputs are processed where they arrive with no active reassignment to particular pipelines. After aggregation, the partial sketches of each pipeline are merged by taking the maximum rank across corresponding buckets by the Merge buckets module. Its complexity is that of a fold. The partial sketches are streamed in parallel and folded bucket by bucket. The following computation phase is identical to the one used in the non-parallel architecture.

**VI. Experiments and Results**

The HLL design is coupled with a Xilinx XDMA bridge IP (a subsystem for PCIe 3.0 x16) [38] on a Xilinx Virtex UltraScale+ FPGA (VCU118) platform [39] serving as a PCIe endpoint for external communication.

The HLL design is driven by 322 MHz (with time period 3.1 ns) clock provided by the CMAC module of the Xilinx UltraScale+ 100G Ethernet subsystem [40]. Thus, with $II = 1$ each pipeline operates at a throughput of $322 \text{MHz} \times 32 \text{bits} = 10.3 \text{Gbit/s}$.

**A. Throughput**

Increasing the number of pipelines in the design allows to scale the throughput until saturating the PCIe bandwidth. This dependency is shown by Fig 4(a). The figure contrasts the practically measured throughput with the theoretical throughput obtained by aggregating the processing rate across all pipelines. Both graphs show the same linear growth up to 10 parallel pipelines. At this point, the PCIe bandwidth is saturated ($10 \times 10.3 \text{Gbit/s} = 103 \text{Gbit/s} > 12.48 \text{GByte/s}$). Adding more pipelines can no longer boost the throughput as the design is I/O bounded (PCIe bound). Thus, for the rest of the PCIe-dependent experiments, we scale the system to at most 10 parallel pipelines.

**B. HLL Standard Error**

We validated our implementation with same data sets as used for the profiling described in Section IV. The standard error of the FPGA-implemented HLL with $p=16$ and using a 64-bit hash matches the standard error curve $HLL_{64}$ in Fig. 1(b).

**C. CPU Performance**

As a baseline, we have implemented HLL using both a 32-bit hash and a 64-bit hash in C++. The 32-bit Murmur3 implementation was optimized using AVX2 technology [41] leveraging, 8-fold vectorization parallelism. The corresponding 4-fold vectorization of the 64-bit hash did not prove beneficial as there is no native 64x64 bit vector multiplication instruction in the AVX2 instruction set. In both cases, the leading zero detection exploits GCC's __builtin_clz, which maps favorably to the native x86 instruction LZCNT that directly implements the desired operation. Threads are used to parallelize the aggregation phase on a dual-socket Intel® Xeon® E5-2630 v3 system with a total of 16 cores, clocked at 2.40 GHz.

Fig. 4(b) shows the analogous performance scaling by increasing the thread-level parallelism of the CPU implementations. It halts and even slightly reverses when the number of forked threads exceeds the native support on the system. The choice of the hash function has a direct impact on the observable performance. The use of the 64-bit hash, which enables the support for cardinalities beyond $10^9$, reduces the performance to about 60% of the one achieved for the 32-bit hash function. In either case, the fully unrolled FPGA implementation outperforms even the fully designated dual-processor system, for the 64-bit hash by more than 80%. As the FPGA-based Murmur3 implementation

![Fig. 3: A multi-pipelined parallel HyperLogLog dataflow architecture.](image-url)

![Fig. 4: HyperLogLog throughput.](image-url)

(a) FPGA throughput vs. #pipelines.  
(b) CPU throughput vs. #threads.
TABLE III: Resources usage of HLL vs. #Pipelines.

| Pipelines | 1   | 2   | 4   | 8   | 10  | 16  |
|-----------|-----|-----|-----|-----|-----|-----|
| BRAM      | 12K | 24K | 48K | 96K | 120K| 192K|
| DSP       | 128K| 256K| 512K| 1M  | 1.6M| 2.5M|
| LUT       | 4K  | 8K  | 16K | 32K | 64K | 128K|
| FF        | 5K  | 10K | 20K | 40K | 80K | 160K|

TABLE IV: Throughput [GByte/s] vs. #Pipelines.

| Pipelines | 1   | 2   | 4   | 8   | 10  | 16  |
|-----------|-----|-----|-----|-----|-----|-----|
| Throughput| 0.05| 0.12| 4.83| 6.77| 8.94| 9.35|

can be unrolled in space to a pipeline with $I = 1$, it achieves a significant speedup over a CPU implementation [23]. The CPU implementation of the HLL is strictly compute-bound by the hash computation even after using AVX2 extensions. The FPGA implementation benefits from the dataflow architecture and the parallel implementation of the hash function. The FPGA-based HLL takes advantage of dataflow architecture that enables to estimate the statistics while data is streamed. The data and statistics arrive almost together in contrast to the CPU implementation.

D. FPGA Resource Utilization

While HLL itself possess a modest memory requirement that grows logarithmically, with the used hash size and $k$ independent pipelines result in FPGA resources utilization shown in Tab. III. The table summarizes the resource utilization for the FPGA-based HLL for 32- and 64-bit hashes, each with precision $p = 16$. Clearly, the resource utilization scales linearly with the number of pipelines. It is the investment of these resources that pay for the gained throughput.

The LUTs and FFs utilization remain under 2%, thus exhibiting its lightweight property in terms of logic resource consumption. Since each pipeline has a dedicated counter-memory, an increase in the number of pipelines is reflected in the BRAM utilization. The maximum usage of this critical resource remains under 6%. The other critical resource is the DSP blocks that are mostly consumed by the hash computation. Slightly more than 10% are consumed by 10 pipelines using a 64-bit hash implementation. On the given device, this resource type would eventually limit further scaling.

VII. HYPERLOGLOG ON TCP/IP NETWORKS

The HLL design is deployed in an FPGA-based NIC featuring a 100 Gbit/s TCP/IP stack [32]. We show that the implementation can process incoming data at line rate.

Fig. 5 depicts the system-level design used to deploy the HLL in the network. The two hosts, A and B, are attached to the network via dedicated PCIe-attached NICs. Host A uses the commercial NIC Mellanox ConnectX-5 [43] across PCIe Gen 3.0 × 16. Host B uses an FPGA-based NIC, which includes a network stack using the UltraScale+ 100G Ethernet Subsystem for a 100 Gbit/s network. This network stack and the integrated HLL implementation are managed by a controller module.

The design is divided into two clock domains: (a) the PCIe clock domain at 250 MHz and (b) the network clock domain established by the serial transceiver interface at 322 MHz for the 100 Gbit/s network. Since the HLL module is processing the data from the network, it is placed in the network clock domain.

We validate the HLL integration on the FPGA-based NIC and measure its sustained throughput for different numbers of parallel pipelines. Data is received over the network from Host A. The network stack on the FPGA-based NIC extracts the data from the received packets to feed the HLL estimation. After processing the whole data stream, the estimation result is sent to Host B’s. Once all the data is streamed, the time taken to compute the cardinality result remains constant, 203 μs, irrespective of the quantity of data, and it stems mainly from the time taken to read all the contents from the counter buckets ($2^{16} \times 3.1\text{ns}$).

The throughput sustained by the receiving NIC is tabulated in Tab. IV. For one and two parallel pipelines, the integrated HLL processing induces significant back-pressure on the network stack, which starts dropping packets. The resulting packet re-transmission cycles push the observable throughput way below 1 Gbit/s. Scaling to more parallel pipelines allows the flow control to work effectively and enables a steady growth of the sustainable throughput. Indeed, four pipelines would be sufficient to saturate 10 and 25 Gbit/s networks, and eight pipelines would be able to handle a 40 Gbit/s network stream safely. In order to accommodate a 100 Gbit/s network, without inducing any back pressure on it, 16 pipelines are needed. The increase in the number of pipelines from 10, sustaining a 12 GByte/s PCIe throughput, to 16, sustaining a 9.35 GByte/s network throughput, comes as a result of supporting network’s bursty behaviour.

As the HLL throughput can be scaled by adding more pipelines and by increasing clock rates, this solution will continue to benefit from the technological improvements of future devices. Currently, HLL on a NIC can achieve a 35% higher processing rate than a 16-core CPU for the same statistical guarantees (Fig. 4(b)). This gives an idea of the potential of our HLL design in improving computational efficiency in cloud settings.

VIII. CONCLUSIONS

We presented how the FPGA-based custom hardware implementation of HyperLogLog can outperform a modern multi-core CPU system. We exploit the programmable logic of the FPGA to implement a parallelized, multi-pipelined HLL. This implementation scales throughput linearly with the number of pipelines, providing an adaptive solution that can be used in a variety of settings (near-storage if the stream comes from NVMe or SSD, on the network data path, or near memory). In the paper, we illustrated this flexibility by discussing two deployments in detail: (a) an FPGA configured as a co-processor and (b) an FPGA functioning as a NIC. Since the standard error of HLL...
depends mainly on the quality of the hash function but the size of the hash function affects performance, we have provided a detailed analysis of error rates and implementation trade-offs on both the FPGA and the CPU. While on the FPGA, the bigger hash function results in a more intense utilization of resources; on the CPU, it leads to computation overhead that severely limits the processing rate. Nevertheless, even with more extensive hash functions, we can still place enough pipelines on the FPGA to saturate the system on its I/O bounds. We see the results as a promising first step to offload the essential operations such as HyperLogLog to FPGA-based accelerators as the performance difference over CPUs can be leveraged to reduce the overall number of machines needed to process extensive data collections without compromising either performance nor result quality.

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