Sinusoidal inverter using pulse width amplitude modulation

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Abstract. In this paper, a technique of single-phase inverter pulse width-amplitude modulation is introduced. This technique is based on tap changer transformer that controls the amplitude of the output voltage. The DC voltage is applied on the primary side of the tap changer transformer with the help of a microcontroller through several semiconductor switches in sequential modality. The tap changer inverter has been analyzed, designed and simulated for four tap inverter using Proteus software. The LCL (low pass filter) is connected on the primary side of the transformer to generate sinusoidal output voltage. In hardware a tap changer inverter has been designed and implemented for four taps inverter. The microcontroller used is minipro, which produces command signal to the switches. The introduced topology has produced large number of levels with decreased total harmonics distortion (THD) in addition to a low cost with isolated multilevel inverter.

Keywords: multilevel inverter, tap changer transformer, total harmonic distortion.

1. Introduction

Dc to ac in power electronics is called dc – ac inverter, which is used in many applications: power supplies, electric vehicles and dc motor speed control [1, 2]. To convert dc power to ac power an inverter is needed with suitable output voltage and frequency. In later years, a magnificent number of industrial applications have begun to request higher power instruments [3]. However, semiconductor power switches the endurance of the medium voltage which has not been outputted resident. A source in medium voltage level is inadequate to directly connect only one switching device, thus the multilevel inverter topology has brought out as a different option for working with medium and high voltage [4]. To control the needed power electronics switches and applications which need high current and high voltage, the multilevel inverter is used [5, 6]. The output achieves near sinusoidal shape, reducing the harmonic as the number of levels increased [7].

Also, to convert it to a sinusoidal signal an appropriate low pass filter is used [8]. The harmonics are reduced by using an LCL filter [9, 10].

In this paper, dc-ac converter is designed in pulse width amplitude modulation technique, using tap changer transformers. Two dc sources are connected on the terminals of switches, and controller circuit to control power switching.

2. Circuit diagram

Using circuit shop v3.00 program to sketch the figure of the circuit diagram for four/five tap inverter which includes two dc sources as input source, power semiconductor switches, filter, tap changer transformer and load.
3. The principle of operation of four taps changer inverter

The Arduino UNO microcontroller applies a controlling signal to the switches S₁, S₂, S₃ and S₄ delay time for closing to limited period. The sequence operates for the switches mentioned above S₁ up to S₄ and the sequence extinguish S₄ down to S₁ then all the switches back to turn off in the same time of the first delay to shape positive half cycle. The negative half cycle is the same procedure above as shown in Table 1.

Table 1 Shows the mode of operation for upper and lower switches to four taps changer inverter.

| Mode  | S₁/S₅ | S₂/S₆ | S₃/S₇ | S₄/S₈ |
|-------|-------|-------|-------|-------|
| Mode 1 | Off   | Off   | Off   | Off   |
| Mode 2 | On    | Off   | Off   | Off   |
| Mode 3 | On    | On    | Off   | Off   |
| Mode 4 | On    | On    | On    | Off   |
| Mode 5 | On    | On    | On    | On    |
| Mode 6 | On    | Off   | On    | Off   |
| Mode 7 | On    | Off   | Off   | Off   |
| Mode 8 | Off   | Off   | Off   | Off   |

Each half cycle equals 10ms by dividing it to nine parts, starts at rest (turn off) equals 1ms. The width of the second level equals 1ms and the width of third level equals 1ms. The width of the fourth level equals 1ms. At the peak value, the sin wave takes more time, therefore the width of the fifth level equals to 2ms. In the center of each level, the magnitude of the time is taken and the angle (Φ) of each one is calculated from Eq. (1), while the magnitude of the output voltage is calculated using Eq. (2).

\[ \Phi = 18t \]  \hspace{1cm} (1)

\[ v_i = v_{max} \sin \Phi \]  \hspace{1cm} (2)
Figure 2. The output voltage of nine levels.

The magnitude of the time is taken in the center of each level, and the calculated angles (Ø) is substituted in Eq. (2) to calculate the output voltage as shown in Table 2.

| t(ms) | Ø(degree) | V(volt) |
|-------|-----------|---------|
| 1.5   | 27        | 22      |
| 2.5   | 45        | 35      |
| 3.5   | 63        | 44      |
| 5     | 90        | 50      |

4. Proteus model
Nine level models are simulated in Proteus software to analyze the FFT as shown in Figure 3.

Figure 3. Model of four tap inverter by Proteus software.
Figure 4 illustrates the output voltage of four tap inverters in Proteus software after and before low pass filter. It is clear that the filter has converted the output wave to a pure sinusoidal form.

![Figure 4](image)

**Figure 4.** Output voltage of Proteus: (a) before the filter (b) after the filter.

In Figure 5, the FFT of the signal before and after the filter shows that the odd harmonics has been reduced.

![Figure 5](image)

**Figure 5.** FFT analysis of the output voltage: (a) before the filter (b) after the filter.
5. Practice implementation of tap changer inverter

Figure 6 explained the circuit practical to three, four, and five taps changer inverter which contained two 12-volt batteries, switches optocouplers, minipro to controls of switching all switches and five taps transformer to generate varying output voltage. The first applied of this circuit in Proteus program and utilization of Proteus output has been done in practice.

![Practical circuit of five taps inverter](image)

**Figure 6.** Practical circuit of five taps inverter.

Figure 7 illustrates the output voltage before and after the filter for four taps inverter. The r. m. s output voltage with filter equals to 187.38 V.

![Output voltage for four taps inverter](image)

**Figure 7.** Output voltage for four taps inverter: (a) before the filter (b) after the filter.
Figure 8 shows the FFT spectrum analysis before the filter for four taps inverter which illustrates the fundamental value and odd harmonics.

Figure 8. The spectrum of FFT analyzed before the filter for four taps inverter.

Figure 9 illustrates the FFT spectrum analysis after the filter for four taps inverter which is explained the fundamental value and the odd harmonics has been reduced.

Figure 9. FFT spectrum analysis after the filter for four taps inverter.

6. Comparison
The comparison between the present results with other related work for THD and the number of switches illustrated in Table 3 [11], [12], [13].

| Parameter | [11] | [12] | [13] | proposed |
|-----------|------|------|------|----------|
| THD %     | 10.47| 11.41| 13.45| 10.04    |
| N_{Switches} | 12  | 16   | 16   | 8        |
7. Conclusion
The structural form of this technique includes a smaller number of switches; thus, the complication is low. The controlling of each switch in this topology is simple compared to other strategies of multilevel inverters. The frequency of switching is low conduces decrease inverter power losses subsequently, increase the efficiency by increasing the number of taps, the THD can be reduced dramatically at the expense of increasing the semiconductor switches.

8. References
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