ABSTRACT: The increasing demand for solar energy has led researchers worldwide to develop new photovoltaic technologies. Among these, perovskite materials are one of the most promising candidates, with a performance evolution unparalleled in the photovoltaic field. However, this thin-film technology is not yet available at a commercial level, mainly due to upscaling issues. This work studied the best design options for upscaling single cells into modules by minimizing electrical losses in the device substrates. The software LAOSS was used to test and optimize different substrate sizes and designs and to predict several performance outcomes from experimentally fabricated single cells. The results showed that it is possible to retain most of the energy production when upscaling from a single cell to a module if the appropriate design for an efficient monolithic device is used. The width of the interconnection zone also plays an important role in device performance and must be carefully optimized during module design. It then demonstrates the importance of having precise laser tools, which are essential for narrow and smooth scribes, and how useful simulation software can be, which, combined with experimental developments, will facilitate efficient module fabrication, aiming to establish it as a feasible and marketable resource.

1. INTRODUCTION

In response to the dramatic climate change due to the excessive use of non-renewable energy sources, the contribution of renewable energy sources to meeting the worldwide energy demands has increased immensely in the last few years. In particular, photovoltaics (PVs) are set to be the fastest growing energy source in the near future, having been classified in 2020 as the world’s cheapest energy source. The importance of this energy source has inspired researchers worldwide to further develop PV technologies. In particular, perovskite solar cells (PSCs) are one of the most promising thin-film solar power harvesting technologies. Reaching from 14.0 to 25.7% power conversion efficiency (PCE) in just 8 years, PSCs have displayed an evolution with no parallel in the PV field. However, some challenges still have to be tackled to make PSCs available at a commercial level: long-term stability, upscaling design, environmental friendliness, effective encapsulation, and economic output are some of the important factors to obtain a reliable technology. Furthermore, since PSC is a thin-film technology, it is important to effectively upscale single cells into large and efficient modules with a reduced dead area, preferably adaptable to flexible substrates and architectural integration. This will have a significant impact on making PSCs suitable for many applications and markets, boosting their growth and usefulness, and particularly addressing building integrated PVs (BIPV) and street furniture applications.

The development of PSCs from small cells to large modules can be challenging mainly due to: (i) difficulty in controlling perovskite morphology and uniformity over large-area devices, which is highly dependent on perovskite deposition methods, (ii) electrical losses in large substrates ascribed to increased series resistance at the transparent conductive oxide (TCO), and (iii) interfacial charge recombination that becomes prominent with increased surface area. Although the spin-coating deposition technique has delivered the best results for laboratory developments, it is not suitable for large-area applications since it does not provide a uniform deposition over large substrates, besides promoting high solution waste. As an alternative, compatible roll-to-roll processes, such as blade coating, slot-die coating, or printing methods, are being widely used for large-scale applications. On the other hand, the TCO coated over glass or polymer substrates of perovskite devices should be highly conductive for driving charges in or out of the cell and transparent for allowing light to reach the photoactive layers. However, since this material is a semiconductor, it presents substantial electrical resistance to charge.
travel. If electrons face high series resistance, they will tend to recombine with holes within the cell, harming the power output and resulting in poor PCE, fill factor (FF), and short-circuit current density ($J_{SC}$). Hence, the way to circumvent this challenge is twofold: enhance the conductivity of the TCO material without compromising transparency or build devices with a short collection path length (<1.0−1.5 cm). In order to accomplish that, the development of perovskite modules has followed mainly two configurations: grid and monolithic. In a grid module, thin metal bars are deposited on top of TCO in order to collect the charges, driving them through the conductive lines while avoiding resistive losses. However, this technique results in additional material costs and a substantial reduction in the module active area. Thus, the most common approach has been through monolithic configuration. Modules built with this design have been showing good performance and promising important breakthroughs for the upscaling of perovskite technologies.

In parallel to hands-on device assembling, simulation tools may be very important to better understand how different dimensions and designs might affect the module’s performance without consuming too much time and materials. Simulation offers the possibility of predicting better options for the device design, understanding the effect of each parameter, and giving important insights for laboratorial work. Hence, this work is fully dedicated to exploring multiple designs and dimensions for a 100 cm$^2$ perovskite module through electrical performance simulation. Some authors have been dedicated to simulation tools in order to better understand how perovskite devices can become better performing. In 2020, Di Giacomo and his team compared electrical simulations and experimental results to evaluate the scaling from small cells to modules, with a special focus on the laser interconnection. 

2. METHODS

Software LAOSS—an electrical module by Fluxim—as used to design, simulate, and optimize large-area PSCs through reduction of electrical losses of the devices; the drawings were made using LibreCAD. The geometry of the device is defined, and it will be specified for each case, followed by the definition of the mesh needs. The mesh used for the finite element method modeling has a 0.1 minimum and maximum edge size when using NetGen as the meshing tool. The focus of this work is the electrical properties, and for this reason, no thermal coupling was considered. It follows the input of the electric correlation between the top and bottom electrodes, that is, the current−voltage ($I$−$V$) curve. For all the simulations (except if mentioned otherwise), the input current−voltage correlation was obtained based on an experimental batch of individual cells prepared as described elsewhere. The proposed PSC device consists of a triple-cation perovskite in a mesoscopic architecture as shown in Figure 1, where fluorine-doped tin oxide (FTO) was used as a transparent conducting oxide.
(TCO), a compact layer of TiO₂ as ETL, a mesoporous layer of TiO₂ as a scaffold, spiro-OMeTAD as HTL, and gold as back contact.

The characteristic curve was achieved for a 1 × 5 cm² active area cell with 8.95% PCE, FF of 0.505, a short-circuit current density of 16.72 mA·cm⁻², and an open-circuit voltage (V_OC) of 1.068 V, as shown in Figure 2. A specific resistance of 0.01 Ω·cm² was considered for the P2 zone, which is the resistance that charges need to overcome for traveling from one sub-cell to the next, that is, the resistance of the interface between the back (usually a metal) and top (TCO) electrodes of different sub-cells. The sheet resistance for the anode side was 7 Ω·sq⁻¹ (the value of the FTO sheet resistance) and 0.407 Ω·sq⁻¹ for the back contact, which corresponds to a layer of gold with 60 nm thickness and 2.44 × 10⁻⁸ Ω·m resistivity at 20 °C. The convergence type used was the absolute residuum, with the norm of the error vector calculated through the root mean square of the residuum, with a 1 × 10⁻¹⁰ tolerance and a maximum of 20 iterations for each element.

3. RESULTS AND DISCUSSION

The PSCs, like other PV technologies, deeply depend on the use of a transparent conductive oxide coated on a rigid or flexible substrate. As mentioned before, a good performing TCO means maximum transparency and conductivity, minimizing optical losses by reflection and electrical losses through the series resistance. The J_SC is one of the most affected PV parameters since, at a high series resistance, the electrons tend to prefer the shunt path, recombining with holes, which reduces the electrical performance of the cell. This phenomenon also traduces into a poor FF. Gao et al. have experimentally studied the effect of enlarging the area of rectangular devices either by increasing the length or width of the PSCs. For large-area single PSCs, increasing the length resulted in a decreased PCE mainly ascribed to the lower J_SC attributed to the recombination during the carrier transport within increased active areas. On the other hand, the increase in width resulted in a dramatic drop of J_SC and FF due to the extended transportation of carriers in the width direction but an increment in the V_OC. However, the increase in V_OC cannot offset the serious decrease in J_SC and FF, resulting in a loss of the output performance. Therefore, increasing the length is the best option for preparing devices with a large active area. Following this achievement, LAOSS software was primarily used to predict the theoretical losses due to TCO resistance when upscaling an individual PSC from 0.2 cm² up to 5 cm² active area. The geometry input in the software was a rectangle with 5 cm length and 1 cm width. For this first simulation, the electrode correlation provided was an experimental J–V curve obtained for a standard cell with 15.22% PCE with 0.2 cm² active area (reference)—Figure 3. A voltage sweep was performed; the simulated characteristic curve comparison with the experimental curve is presented in Figure 4, and the corresponding PV parameters are compared in Table 1.

The input J–V curve is the coupling law between the top and bottom electrodes, which the software considers to be constant over all the device area. Therefore, the slight differences in performance between the simulated and experimental cells are only due to the TCO series resistance, demonstrating that at these dimensions, it practically does not have limitations on the electrical power output of the cells.

On further analysis, the previously simulated 5 cm² device was compared with the experimental best 5 cm² device (Figure 5). The corresponding PV parameters of the experimental cell were 8.95% PCE, a FF of 0.505, a V_OC of 1.065 V, and a J_SC of 16.73 mA·cm⁻².

In this case, there is a large difference between the two J–V curves, which is only narrowed in the voltage limit zone. Actually, the experimentally produced 5 cm² cell has a higher V_OC than the reference one, but the difference is small and it is within the experimental error. However, the other PV parameters, such as PCE, short-circuit current density, and FF, show lower values. There are several reasons for this. First, as stated before, LAOSS only considers the resistive losses of the electrodes, while under real operating conditions, other factors affect the performance of the cell, such as the non-uniform deposition in large-area devices (which could be improved by further laboratory optimization of the deposition), the presence of pinholes, and the interfacial defects created during cell fabrication. One of the major differences is in FF, which varies from 0.702 in the simulated to 0.505 in the best-performing experimental cell. A loss of FF is natural.
during upscaling, not only due to substrate resistance but also largely related to the quality of the perovskite layer and recombination pathways. Therefore, a lower FF for the experimental cell was expected, especially due to the inhomogeneity of the absorber layer. This conclusion also indicates the importance of developing a large-scale deposition method to produce a thin, uniform, and crystalline perovskite layer. Thus, the $J-V$ curve of the 5 cm$^2$ laboratory cell with 8.95% PCE will be used for upcoming simulations, as it represents the real performance obtained when upscaling in the laboratory environment, which is strongly affected by the defects in the large-scale deposition.

These results emphasize the need to divide the entire active area into smaller areas and connect them into sub-modules. Therefore, optimized and logical partitioning is crucial to achieving highly efficient perovskite devices. The interconnection geometry will be evaluated for module configuration, as it together with the scribing optimization enables adequate charge pathways. A monolithic module of $10 \times 10$ cm$^2$ aperture area was simulated with charges traveling horizontally across the entire substrate. In a monolithic module, the sub-cells are connected in series. The P1 scribe isolates different TCO segments, the P2 creates a path to connect two consecutive sub-cells, and the P3 isolates them from each other, as shown in Figure 6. To achieve the best performance, the interconnection zones should always be as narrow as possible to reduce the dead areas in the module. It is also worth mentioning that the scribes should not only be narrow but also as homogeneous and smooth as possible to allow better module fabrication without heat damage or surface roughness that can cause higher resistance for the charge travel.

For module simulations, it is important to establish a gap width for the interconnection zone. Schultz et al. reported a laser-fabricated PSC module with optimized laser parameters to enhance the P2 scribe, resulting in a better performance due to the low resistance between contacts in the P2 zone. A gap width of 0.5 mm and a series resistance in the P2 connection between electrodes of 0.01 $\Omega \cdot \text{cm}^2$ were found. Thus, for this work, the first total interconnection gap (P1 + P2 + P3) was set to 0.5 mm and the minimum scribe width to 0.1 mm. P1 and P3 were set at 0.1 mm, while P2 was set at 0.3 mm (Figure 7). Since P1 and P3 have the sole function of preventing electrical conduction between different sub-cells, they must be as narrow as possible, while P2 is a zone where charges travel from one sub-cell to another. The tiny spaces between the different scribes should be accountable for the width of P2.

Furthermore, it is also important to evaluate the number of sub-cells for the module. For a small division with few sub-cells, the large distance that charges must travel within each cell results in significant resistive losses on the TCO, while too many sub-cells, and consequently too many interconnections, result in excessively dead areas. Therefore, it is important to find an optimal number of sub-cells. To determine this, the LAOSS Full module handling tool was used, which calculates the power outcome of a module in a range of divisions selected by the user, assuming a constant aperture area and no electrical losses or production at the interconnection zones and setting the total interconnection width. The relationship between the power outcome and the number of sub-cells of a module for a 0.5 mm gap is shown in Figure 8.

According to the results obtained, the best-performing module should be divided into 12 sub-cells, with a width of

---

**Figure 5.** Comparison between simulated and experimental $J-V$ curves for 5 cm$^2$ active area of PSCs.

**Figure 6.** PSC module’s monolithic configuration. Red arrows represent the charge flow.

**Figure 7.** Module interconnection zone.
7.875 mm for each cell and 0.5 mm for each interconnection, as represented in Figure 9. However, it is also noticeable that the power loss is negligible for an 8 sub-cell module. This reduced number of sub-cells could be important for mass production of modules, as it is much easier for industrial purposes to build modules with fewer divisions, and apparently with low power losses.

Once all parameters were defined, a voltage sweep up to 12.84 V (obtained by multiplying the number of sub-cells by the $V_{OC}$ of each sub-cell) was simulated in LAOSS. The PV parameters extracted from the $J-V$ curve shown in Figure 10 for the 12 sub-cell module were 8.15% PCE, 0.486 FF, 12.7 V $V_{OC}$ and 16.70 mA cm$^{-2}$ $J_{SC}$.

The simulated results showed minor differences from the experimental single cell used as an input. The verified lower values, especially for the PCE from 8.95 to 8.15% and for the FF from 0.505 to 0.486, could be due to the substrate resistance on the TCO, which causes small resistive losses during charge movement, and the interconnections, which could cause some current losses. These results show that it is possible to build efficient large modules if precise ablation tools are available to perform smooth and narrow scribes, minimizing dead areas and electrical losses in the interconnection zones.

To better understand the constraints caused by the sheet resistance of TCO and the interconnection dimensions, the total gap was set to 1.0 mm, P1 and P3 to 0.2 mm, and the remaining P2 to 0.6 mm. Again, the Full module handling tool was used to evaluate the ideal $10 \times 10$ cm$^2$ module division. The results showed that the ideal division would be nine sub-cells, each with approximately 1.02 cm width (and eight interconnections). For this simulation, all parameters are the same except that the voltage sweep limit is now 9 times the $V_{OC}$ of the cell used, that is, 9.59 V—Figure 11. The PV parameters simulated for the 9 sub-cell module were: 7.78% PCE, 0.477 FF, 9.56 V $V_{OC}$, and 16.7 mA cm$^{-2}$ $J_{SC}$.

The loss in PCE, with a decrease of 4.5% compared to the 12 sub-cell module, was verified. Also, FF drops from 0.486 to 0.477. These changes indicate that the interconnection gap plays an important role in the module performance. Since the simulator outcomes show that wider interconnections should also result in wider sub-cells, the lower performance is likely due to the sheet resistance of the TCO that increases with the width of the sub-cell (higher collection path length).

To better understand this relationship, additional simulations were performed for 1.5 and 2.0 mm gaps, considering P1 and P3 with 0.3 mm width and P2 with 1.2 mm gap device and P1 and P3 with 0.4 mm and P2 with 1.2...
mm for the 2.0 mm gap device. Figure 12 shows a strong decay in the PCE and FF parameters with increasing gap sizes. Therefore, precise laser tools are required to fabricate large-area modules, enabling the reduction of dead areas within the device and thus maximizing its performance. In addition, it has been shown that as the gap size increases, the ideal number of sub-cells of the monolithic module decreases, which in turn allows for a simpler fabrication process. All of these variables must be considered when upscaling photo-electrochemical devices.

The previously optimized PSC module design is particularly interesting for solar farms where the major objective is to produce the maximum electrical power with the minimum area available. Nevertheless, perovskite solar modules are especially interesting for BIPV applications, and their interest is growing within PV applications. Thus, one of the most common approaches is the fabrication of square modules, which can be easily arranged in any pattern, which will be the next study case. The performance of a $10 \times 10$ cm$^2$ square module—same dimensions as those of the devices previously studied—divided into four or nine small sub-cells was evaluated (Figure 13). The red arrows represent the charge flow and dashed lines represent the series interconnection zone, whereas the full lines represent non-conductive segments so that the current is driven in the desired direction to avoid short-circuits. For simulation purposes, the P1 and P3 widths were set to 0.20 mm and the P2 width to 0.60 mm, completing a total of 1.0 mm interconnection gap. The non-conductive segment also has a 1.0 mm width. The simulated $J-V$ characteristics curves were obtained for each of the designs (Figure 14), and the correspondent PV parameters were determined (Table 2). The voltage axis refers to merely one sub-cell of the module for a better comparison between the two curves. All the sub-cells in the device have the same performance.

Both curves show a quick decay of the current density and a very low FF, which is confirmed by the values presented in Table 2. The large distance (about 5 cm for the 2v2 module and 3.3 cm for the 3v3 module) that the charges have to travel to reach the next sub-cell emphasizes the effect of substrate
series resistance, which affects the performance of both modules. The best results obtained for the 3v3 module are due to the smaller dimension of the sub-cells. All parameters were calculated based on the total area and not the active area. The dead area and manufacturing complexity of both modules increase as the number of sub-cells of the 10 cm × 10 cm module increases.

In addition to studying the overall device design, module performance can also be improved by optimizing the sub-cell unit. Some strategies are being used to improve the performance of a strip perovskite cell, such as implementing a hexagonal metal grid or etching the TCO to introduce thin conductive lines that collect charges along the substrate. In both cases, highly conductive materials should be used for the conductive lines to maximize the charge collection and minimize the dead area caused by the conductive line shadow. Therefore, three cases were studied: a strip-shaped cell with a hexagonal gold grid and two etched strip-shaped cells. The performance of a 5 × 1 cm² strip was simulated for each case. A gold grid with a 0.1 cm hexagon radius, 0.1 mm width, and 100 nm thickness was used for the simulation. For etching cases 1 and 2, substrates with 400 nm thick embedded gold lines were generated: in the “etching 1” case, a substrate with a sheet resistance of 6 Ω·sq⁻¹ and a loss of 1.0% of the active area and in the “etching 2” case, a substrate with a sheet resistance of 3 Ω·sq⁻¹ and a loss of 4.8% of the active area. Figure 16 shows the simulated J–V curves for the three cases, and Table 3 compares the PV parameters.

The data obtained from the simulations show that the “hexagonal grid” is the most promising approach in this set of strategies. The hexagonal grid allows charges to be quickly collected by the contacts, reducing resistive losses in the TCO, which leads to an improvement in the J_sc and, consequently, in the global efficiency of the device. However, using this strategy, a 23% loss of active area is obtained due to the grid shadow, constituting the major disadvantage of this strategy. The balance between sheet resistance and dead areas should always be carefully studied, as one is inevitably affected by the other when techniques such as scribe etching or hexagonal grids are used. Therefore, it is important to develop tools to improve the performance of cell units with the thinnest materials without compromising effective charge collection. In addition, the simulation of the “etching 1,” “etching 2,” and “hexagonal grid” was performed with gold, which is a very good conductor but also a very expensive material. The development of cheap yet highly conductive materials could prove very useful in improving the performance of perovskite devices. The values in this simulation are much better than those of the square modules, which is due to the fact that the cell is only 1 cm wide. To form a complete device, these cells must either be electrically connected or assembled into a module.

4. CONCLUSIONS

There are many obstacles in upscaling small-scale perovskite cells to large, efficient, robust, and economically feasible devices. In particular, the TCO substrate is a major source of resistive losses for the generated charges. To better understand the impact of this layer and the best approaches to tackle it, simulation studies are an important tool to test different hypotheses and strategies in less time and without wasting materials. In this work, LAOSS software was used to study many options for upscaling experimentally fabricated devices. Preliminary simulations show that the quality of the perovskite film and active layers also play a large role in device performance. For a 1 cm wide strip, simulations showed that up to 95% of the respective single cell (0.2 cm²) could be preserved, while experimental work resulted in a 41% decrease. Regarding module fabrication, the results highlight the importance of building devices with thin sub-cells, as fully horizontal monolithic modules perform significantly better than square split modules. Nevertheless, the latter option is
more suitable for BIPV applications, so each case should be thoroughly studied to understand which options are beneficial for each PSC use. An ideal division for building a monolithic module could retain 91% of the power production according to the optimization performed with LAOSS. However, this performance depends on the availability of precise and narrow laser tools since the scribe width also plays an important role in the performance of the modules, especially for PCE and FF. In fact, a decrease of 4 and 2% was obtained, respectively, when the interconnection gap width was increased by 0.5 mm.

This work indeed provides important insights into large-scale device building by studying some of the most important variables to be taken into account. Simulation tools are important tools that must go hand in hand with the experimental work to efficiently scale perovskite devices and make them a marketable technology.

Table 3. Simulated PV Parameters for the Different Strip-Shaped Cells

|                | etching 1 | etching 2 | hexagonal grid |
|----------------|-----------|-----------|----------------|
| PCE [%]        | 8.59      | 8.76      | 9.90           |
| V<sub>OC</sub> [V] | 1.07      | 1.07      | 1.07           |
| J<sub>SC</sub> [mA·cm<sup>−2</sup>] | 16.7      | 16.7      | 18.9           |
| FF             | 0.483     | 0.492     | 0.492          |

**ACKNOWLEDGMENTS**

This work was financially supported by LA/P/0045/2020 (ALiCE), UIDB/00511/2020, and UIDP/00511/2020 (LEPABE) and funded by national funds through FCT/MCTES (PIDDAC); Project InPSC – PTDC/EQU-EQU/4193/2021 funded by national funds through the FCT/MCTES (PIDDAC); Project SolarPerovskite—NORTE-01-0145-FEDER-028966 funded by ERDF through NORTE 2020—Programa Operacional Regional do NORTE and by national funds (PIDDAC) through FCT/MCTES; Project 2SMART—engineered smart materials for smart citizens—with reference NORTE-01-0145-FEDER-000054 supported by Norte Portugal Regional Operational Program (NORTE 2020) under the PORTUGAL 2020 Partnership Agreement through the European Regional Development Fund (ERDF).

**REFERENCES**

(1) World Energy Outlook 2020; International Energy Agency, 2020. https://iea.blob.core.windows.net/assets/a72d8a1f-de08-4385-8711-b8a062d6124a/WEo2020.pdf (accessed on May 26, 2022).

(2) NREL. Research Cell Record Efficiency Chart, 2022. https://www.nrel.gov/pv/assets/pdfs/cell-pv-eff-emergingpv-rev211214.pdf (accessed on May 26, 2022).

(3) Li, Z.; Klein, T. R.; Kim, D. H.; Yang, M.; Berry, J. J.; van Hest, M. F. A. M.; Zhu, K. Scalable fabrication of perovskite solar cells. *Nat. Rev. Mater.* 2018, 3, 18017.

(4) Yoon, J. H.; Park, J. K.; Kim, W. M.; Lee, J.; Pak, H.; Jeong, J. H. Characterization of efficiency-limiting resistance losses in monolithically integrated Cu(In,Ga)Se<sub>2</sub> solar modules. *Sci. Rep.* 2015, 5, 7690.

(5) Stolterfoht, M.; Caprioglio, P.; Wolff, C. M.; Márquez, J. A.; Nordmann, J.; Zhang, S.; Rothhardt, D.; Hörmann, U.; Amir, Y.; Redinger, A.; Kegelmann, L.; Zu, F.; Albrecht, S.; Koch, N.; Kirchartz, T.; Saliba, M.; Unold, T.; Neher, D. The impact of energy alignment and interfacial recombination on the internal and external open-circuit voltage of perovskite solar cells. *Energy Environ. Sci.* 2019, 12, 2778–2788.

**AUTHOR INFORMATION**

**Corresponding Author**
Luísa Andrade — LEPABE—Laboratory for Process Engineering, Environment, Biotechnology and Energy, Faculty of Engineering and ALiCE—Associate Laboratory in Chemical Engineering, Faculty of Engineering, University of Porto, 4200-465 Porto, Portugal; orcid.org/0000-0001-5750-1285; Email: landrade@fe.up.pt

**Authors**
Diogo Castro — LEPABE—Laboratory for Process Engineering, Environment, Biotechnology and Energy, Faculty of Engineering and ALiCE—Associate Laboratory in Chemical Engineering, Faculty of Engineering, University of Porto, 4200-465 Porto, Portugal
Vera C. M. Duarte — LEPABE—Laboratory for Process Engineering, Environment, Biotechnology and Energy, Faculty of Engineering and ALiCE—Associate Laboratory in Chemical Engineering, Faculty of Engineering, University of Porto, 4200-465 Porto, Portugal
(6) Mouhamad, Y.; Meroni, S. M. P.; De Rossi, F.; Baker, J.; Watson, T. M.; Searle, J.; Jewell, E. H. Geometrical optimization for high efficiency carbon perovskite modules. Sol. Energy 2019, 187, 129–136.

(7) Di Giacomo, F.; Castriotta, L. A.; Kosash, F. U.; Di Girolamo, D.; Ducati, C.; Di Carlo, A. Upscaling Inverted Perovskite Solar Cells: Optimization of Laser Scribing for Highly Efficient Mini-Modules. Micromachines 2020, 11, 1127.

(8) Kaity, A.; Shubham; Singh, S.; Pandey, S. K. Optimal design and photovoltaic performance of eco friendly, stable and efficient perovskite solar cell. Superlattices Microstruct. 2021, 156, 106972.

(9) Bhattarai, S.; Sharma, A.; Muchahary, D.; Gogoi, M.; Das, T. D. Carrier transport layer free perovskite solar cell for enhancing the efficiency: A simulation study. Optik 2021, 243, 167492.

(10) FLUXiM. Electrical Module. https://www.fluxim.com/electrical-module (accessed on May 26, 2022).

(11) (a) Mesquita, I.; Andrade, L.; Mendes, A. Temperature Impact on Perovskite Solar Cells Under Operation. ChemSusChem 2019, 12, 2186–2194. (b) Castro, D. Optimization and scaling-up of perovskite solar cells deposition. Master Thesis in Chemical Engineering, FEUP, Portugal, July 2020.

(12) Schulte, C.; Fenske, M.; Dagar, J.; Zeiser, A.; Bartelt, A.; Schlattrmann, R.; Unger, E.; Stegemann, B. Ablation mechanisms of nanosecond and picosecond laser scribing for metal halide perovskite module interconnection - An experimental and numerical analysis. Sol. Energy 2020, 198, 410–418.

(13) Loyd, D. H. Physics Laboratory Manual; Thomson Brooks/Cole, 2008. https://www.pdfdrive.com/physics-lab-manual-e13896752.html (accessed on 03/08/2022).

(14) Riza, M. A.; Ibrahim, M. A.; Ahamefula, U. C.; Mat Teridi, M. A. M.; Ahmad Ludin, N. A.; Sepeai, S.; Sopian, K. Prospects and challenges of perovskite type transparent conductive oxides in photovoltaic applications. Part I—Material developments. Sol. Energy 2016, 137, 371–378.

(15) Mouhamad, Y.; Meroni, S. M. P.; De Rossi, F.; Baker, J.; Watson, T. M.; Searle, J.; Jewell, E. H. Geometrical optimization for high efficiency carbon perovskite modules. Sol. Energy 2019, 187, 129–136.

(16) Gao, L.; Chen, L.; Huang, S.; Li, X.; Yang, G. Series and Parallel Module Design for Large-Area Perovskite Solar Cells. ACS Appl. Energy Mater. 2019, 2, 3851–3859.

(17) Ompong, D.; Singh, J. High open-circuit voltage in perovskite solar cells: The role of hole transport layer. Org. Electron. 2018, 63, 104–108.

(18) Kim, W.-K.; Lee, S.; Hee Lee, D. H.; Hee Park, I. H.; Seong Bae, J. S.; Woo Lee, T. W.; Kim, J.-Y.; Hun Park, J. H.; Chan Cho, Y. C.; Ryong Cho, C. R.; Jeong, S.-Y. Cu Mesh for Flexible Transparent Conductive Electrodes. Sci. Rep. 2015, 5, 10715.

(19) Duarte, V. C. M.; Ivanou, D.; Bernardo, G.; Andrade, L.; Mendes, A. Embedded current collectors for efficient large area perovskite solar cells. Int. J. Energy Res. 2021, 46, 5288–5295.