Three channel high dynamic current measurement system for low power systems

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Abstract. The measurement of the dynamic power consumption is a very important task for the characterization and optimization of an energy-autonomous system. In this paper a measurement system is presented that allows the simultaneous measurement of three current ranges from 1 µA to 30 mA at a sample rate of 1 MHz with a selectable supply voltage in the range of 1.8 V to 3.3 V. With this system the full range of low to high power consumption is covered with a high resolution in time, as it is present in a wireless sensor node during data acquisition and wireless communication, respectively.

1. Introduction
In the field of energy harvesting there are two optimization goals in the design of a system: On the one hand the power consumption should be minimal, on the other hand functionality, reliability and availability should be maximized. To achieve this goal a good knowledge about the power consumption is mandatory.

In general, a precise multimeter is sufficient to measure low currents. However, in low power systems used for embedded wireless sensor nodes the supply current varies considerably over time. Energy is saved by turning off, respectively powering down units like wireless transceivers or sensors as soon as they are not needed. However, power consumption is increasing rapidly as soon as power-hungry units are turned on, e.g. the wireless transmitter. This results in a supply current ranging over several orders from a few 100 nA to a few 10 mA. The only system available on the market fulfilling the requirements of a highly dynamic current measurement system is the CX3324A “Device Current Waveform Analyzer” from Keysight. This system is able to measure currents in a range from 100 pA to 10 A with a maximum resolution of 16 bit and a maximum sample rate of 1 GS/s [1]. However, flashing a price tag of a five-figure amount, this system is too expensive to be accepted on a widespread basis.

Therefore, we present in this paper a low-cost current/power measurement system enabling the power analysis of many energy harvesting applications, by measuring currents in a range from 1 µA to 30 mA with a sample rate of 1 MHz and with a supply voltage range from 1.8 V to 3.3 V.

2. Concept and preliminary considerations
In general, a current through a load is measured by converting it into a voltage by a resistor. As the resistor is put in series to the load, a trade-off has to be found between an acceptable voltage drop and the resolution of the current measurement. Furthermore, a change in the supply voltage at the load is
The error introduced by the transistor’s Early effects is compensated in the digital post-processing by a look-up table.

To address this challenge the configuration shown in figure 1a can be used. The current sense resistor $R_s$ is placed in the feedback loop of a non-inverting operational amplifier keeping the supply voltage $U_{\text{supply}}$ of the load constant. The measurement range, respectively the resolution of the current sensing, is now limited to the supply voltage and the output swing of the amplifier. Replacing the sensing resistor by a current mirror (see figure 1b) allows for smaller supply voltages of the whole setup as the collector-emitter-voltage of a typical PNP transistor is in the range of a few 100 mV only. The output current $I_{\text{load}}$ of the current mirror will reflect the supply current in the load at the adjusted supply voltage $U_{\text{supply}}$. To convert this current into a voltage, a sensing resistor or a transimpedance amplifier can be used. However, the problem of limited resolution is still present. This problem can be addressed by using a current mirror which mirrors the current several times (figure 1c). This modification enables a splitting of the measurement range while keeping the output voltage of the amplifier low. Due to the lack of integrated current mirrors with a defined ratio, the current consumption of the whole sensing system is a multiple of the load current.

**Figure 1.** Concepts to measure the supply current through the load $R_{\text{load}}$ while keeping the supply voltage $U_{\text{supply}}$ for the device under test at a constant level.

### 3. Analog circuit design

The implementation of the previously presented concept is shown in figure 2. To minimize the gain error of the current mirror, a well-matched four PNP transistor array (THAT320) is used. An additional PNP transistor connected to the base of the current mirror reduces the error introduced by the base current. For temperature compensation, a small-tolerance 10 Ohm emitter resistor is used for each transistor in the current mirror. As the load current is mirrored three times, the total current through the current mirror can raise to values above 100 mA which cannot be delivered by a standard operational amplifier. Therefore, a NPN transistor controlled by the operational amplifier (OPA827) is used to handle higher currents. Due to oscillations, occurring for several load resistances placing the current mirror in the feedback loop, it is placed between the supply line and the collector of the NPN transistor.

The mirror concept presented here provides two main challenges. First, for the current-to-voltage conversion two approaches would be possible. On the one hand, transimpedance amplifiers could be used. The advantage of this approach would be the independence of the current on the collector-emitter-voltage as it is constant. However, a downside would be the increased complexity of the circuit: The output swing of the amplifier reduces with the ascending load current which would demand for a symmetric power supply. One the other hand, the conversion could be implemented by a simple resistor as it is done in this newly proposed system. A rail-to-rail operational amplifier (OPA4350) connected to the respective resistor is used as a buffer delivering $U_{\text{out}}$ for the ADC input. The error introduced by the transistor’s Early effects is compensated in the digital post-processing by a look-up table.
A second challenge is the introduction of nonlinearities when one of the transistors enters the saturation region due to a high voltage drop on the respective current sense resistor. To avoid the saturation of a transistor an n-channel MOSFET, controlled by the digital circuit, is put in parallel to every current sense resistor to short it when its voltage exceeds the linear region of the bipolar junction transistor in the respective branch of the current mirror. The system is powered from a unipolar 9 V supply enabling also a mobile use without any effort for split supply. Lower voltages for the buffer amplifiers and the digital circuit are generated by two voltage regulators. The supply voltage for the device under test is set in a range from 1.8 V to 3.3 V via a voltage divider with a digital 10 k resistor controlled by the digital circuit.

4. Digital interface and software design
The task of the digital circuit is the digitization and monitoring of the measured voltages as well as the data transfer to a computer for post-processing and data analyses. For the analog-to-digital conversion three single-channel ADCs (MAX11108) are used allowing a simultaneous sampling of all three channels. To prevent the transistor in the current mirror from entering the saturation region the ADC outputs are analyzed continuously. By evaluation the output value of the next-in-size current range an easy and fast control mechanism can be implemented. Introducing a hysteresis by setting an upper and a lower threshold minimizes the switching operations and enables an efficient post-processing of the data. Often, the data transfer to a PC is a bottleneck in a measurement system. To enable a continuous and simultaneous readout of all three channels, a combination of an FPGA (Spartan 6) and the FT232H USB UART/FIFO IC from FTDI is used (see figure 3). The FT232H chip runs in a parallel 245 FIFO mode allowing transfer rates up to 40 MB/s. Unfortunately its internal FIFO Buffer is limited to 1 kB in size resulting sometimes in a discontinuous data stream. Therefore, the FPGA acts as a second FIFO buffer in addition to the readout of the ADCs and the output monitoring. As the FTDI chip runs at a higher frequency than the FPGA respectively the sampling frequency, an overflow of the FPGAs buffer is impossible. On the PC side, a LabVIEW program is running that records and post-processes the data. The user can set the recording time as well as the supply voltage.
5. Measurement results
In figure 4 the transfer characteristic of the measurement system is shown. The load was simulated with a resistor cascade. A strong linear relation with a $R^2 > 0.999$ was found between the load current and the output voltage. The offset error is related to the offset voltage of the buffer amplifier, the gain error is affected by the resistor tolerance as well as by the gain error in the current mirror. A look-up table in the post-processing step can easily compensate both. The results of dynamic measurements are shown in figure 5 and 6. The power consumption of a MSP430 low-power microcontroller is depicted in figure 5. Short interrupts between the change of the low power mode (LPM) as well as the switching frequency of the internal voltage regulator can be clearly seen. When comparing the measured currents to the datasheet values [2] only small deviations can be found. In figure 6 the current consumption of a wireless data logger consisting of a wake-up receiver, a wireless data interface and two temperature sensors during the sensors readout and a wireless transmission is shown. All events can be clearly distinguished by their current consumption. Even the turn on of different modules during a task like the turn on of the amplifiers and the current sources as well as the start of the analog-to-digital conversion during the sensor readout are visible.

![Figure 4](image1.png)
![Figure 5](image2.png)
![Figure 6](image3.png)

Figure 4. Output characteristic of the measurement system over a measurement range from 1 μA to 30 mA for all three measurement ranges.

Figure 5. Current consumption of a MSP430FR5969 microcontroller in different power modes running at 8 MHz and 3 V supply voltage.

Figure 6. Current consumption of a data logger during a sensor readout and a wireless data transmission.

6. Conclusion and outlook
This paper reports the development of a low-cost measurement system able to measure the dynamic supply current of low power systems. With a sample rate of 1 MHz and a measurement range from 1 μA to 30 mA it is suitable for most energy-autonomous embedded systems involving microcontrollers, sensors and wireless transmitters. To set up the recording length and the supply voltage, a user interface is implemented in LabVIEW. This software also allows an initial post-processing and gives a first overview of the current consumption as well as derived quantities like the mean power, min/max power and the energy demand.

References
[1] CX3324A/CX3324 Device Current Waveform Analyzer, datasheet, Keysight, 2017.
[2] MSP430FR59xx Mixed-Signal Microcontrollers, datasheet, Texas Instruments, 2017.