Synthesis of Fault Tolerant Reversible Logic Circuits

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Abstract—Reversible logic is emerging as an important research area having its application in diverse fields such as low power CMOS design, digital signal processing, cryptography, quantum computing and optical information processing. This paper presents a new 4*4 universal reversible logic gate, IG. It is a parity preserving reversible logic gate, that is, the parity of the inputs matches the parity of the outputs. The proposed parity preserving reversible gate can be used to synthesize any arbitrary Boolean function. It allows any fault that affects no more than a single signal readily detectable at the circuit’s primary outputs. Finally, it is shown how a fault tolerant reversible full adder circuit can be realized using only two IGs. It has also been demonstrated that the proposed design offers less hardware complexity and is efficient in terms of gate count, garbage outputs and constant inputs than the existing counterparts.

Keywords—reversible logic; Fredkin gate; parity preserving reversible logic gate; IG gate; fault tolerant full adder circuit

I. INTRODUCTION

Power dissipation is an important factor in VLSI design. Combinational logic circuits dissipate heat in an order of $kT$ ln $I$ joules for every bit of information that is lost, where $k$ is the Boltzmann constant and $T$ is the operating temperature [1]. Information is lost when the input vector can not be uniquely recovered from its output vectors. Reversible logic circuits naturally take care of heating since in a reversible logic every input vector can be uniquely recovered from its output vectors and therefore no information is lost. According to [2] zero energy dissipation would be possible only if the network consists of reversible gates. Thus reversibility will become an essential property in future circuit design.

Synthesis of reversible logic circuits differs from the combinational one in many ways [3]. Firstly, in reversible circuit there should be no fan-out, that is, each output will be used only once. Secondly, for each input pattern there should be a unique output pattern. Finally, the resulting circuit must be acyclic. Any reversible gate performs the permutation of its input patterns only and realizes the functions that are reversible. If a reversible gate has $k$ inputs, and therefore $k$ outputs, then we call it a $k$ reversible gate. Any reversible circuit design includes only the gates that are reversible. In a reversible circuit, the outputs that are not used as primary outputs are called garbage and the input lines that are set to constants are termed as constant inputs. An efficient design should keep the number of garbage outputs to minimum.

Parity checking is one of the widely used error detection mechanisms in digital logic and data communication systems.

This is because most of the arithmetic functions is not parity preserving. If the parity of the input data is maintained throughout the computation, no intermediate checking would be required [4]. A sufficient requirement for parity preservation of a reversible circuit is that each gate be parity preserving [4]. Thus, we need parity preserving reversible logic gates to construct parity preserving reversible circuits. This paper presents a new 4*4 parity preserving logic gate, IG. It is parity preserving, that is, the parity of the inputs matches the parity of the outputs. IG is universal in the sense that it can be used to synthesize any arbitrary Boolean function. It is shown that a fault tolerant reversible full adder circuit can be realized using only two IGs. The presented design does not produce any unnecessary garbage outputs. Minimizing number garbage outputs are the major concern in reversible logic design [3]. The presented fault tolerant full adder block can be used to realize other arithmetic circuit in nanotechnology such as ripple carry adder, carry look-ahead adder, carry-skip logic, and multiplier/divisors.

II. REVERSIBLE LOGIC GATES

A. Basic Reversible Gates

There exist many reversible gates in the literature. Among them 2*2 Feynman gate (FG) [6], depicted in Fig. 1a, 3*3 Peres gate (PG) [7], depicted in Fig. 1b, 3*3 Toffoli gate (TG) [8], depicted in Fig. 1c and 3*3 Fredkin gate (FRG) [9], depicted in Fig. 1d have been studied extensively. Because of their simplicity and quantum realization cost there are design approaches and tools that incorporate them separately or in combination with each other [3][5].

B. Parity Preserving Reversible Gates

Fault tolerance is the property that enables a system to continue operating properly in the event of the failure of some of its components. If the system itself made of fault tolerant components, then the detection and correction of faults become easier and simple. In communication and many other systems, fault tolerance is achieved by parity. Therefore, parity preserving reversible circuits will be the future design trends to the development of fault tolerant reversible systems in nanotechnology. And a gating network will be parity preserving if its individual gate is parity preserving [4].

A few parity preserving logic gates have been proposed in the literature. Among them 3*3 Feynman Double gate (F2G) [4] depicted in Fig. 2a and 3*3 Fredkin gate (FRG) [9] depicted in Figure 2b are one-through gates, which means one of the inputs is also output. Recently Haghparast and Navi...
[10] have proposed a new 3*3 parity preserving reversible gate, namely New Fault Tolerant gate (NFT) depicted in Figure 2c.

From Table 1, 2, and 3 we can see that the gates FRG, F2G and NFT are parity preserving since they satisfy \( A \oplus B \oplus C = P \oplus Q \oplus R \). And any k*k reversible logic gate where the EX-OR of the inputs matches the EX-OR of the outputs will be parity preserving.

C. A New 4*4 Parity Preserving Reversible Gate

This paper presents a new 4*4 parity preserving reversible gate, IG, depicted in Fig. 3. The gate is one-through, which means one of the input variables is also output. The corresponding truth table of the gate is shown in Table 4. It can be verified from the truth table that the input pattern corresponding to particular output pattern can be uniquely determined. The proposed reversible IG is parity preserving. This is readily verified by comparing the input parity \( A \oplus B \oplus C \oplus D \) to the output parity \( P \oplus Q \oplus R \oplus S \).

The newly proposed IG gate is universal in the sense that it can be used for implementing arbitrary Boolean functions as shown in Fig. 4.

D. Design of Parity Preserving TG Circuit

Toffoli gate [8], depicted in Fig.1c, is one of the most important and useful gate in reversible logic circuit synthesis. Therefore implementation of parity preserving Toffoli gate is essential. A parity preserving reversible TG circuit is presented in [4], which is shown in Fig. 5. The circuit requires three reversible gates (one is FRG and two are F2G gates) and produces two garbage outputs. Another parity preserving reversible TG circuit is presented in [10], which is shown in Fig. 6. The circuit requires two reversible gates (one is NFT and one is F2G gate) and produces one garbage output.

E. Evaluation of the Proposed Parity Preserving TG Circuit

The proposed parity preserving reversible TG circuit is more efficient than the existing circuits presented in [4], [10]. Let
\( \alpha = \) A two input EXOR gate calculation  
\( \beta = \) A two input AND gate calculation  
\( \delta = \) A NOT gate calculation  
\( T = \) Total logical calculation

TABLE IV. TRUTH TABLE OF PARITY PRESERVING IG GATE

| A | B | C | D | P | Q | R | S |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

For [4] the Total logical calculation is: \( T = 6\alpha + 4\beta + 2\delta \), for [10] the Total logical calculation is: \( 5\alpha + 3\beta + 2\delta \), and for our proposed parity preserving reversible TG circuit, the Total logical calculation is: \( 4\alpha + 4\beta + 3\delta \). Therefore, the presented design offers less hardware complexity than the existing counterparts.

TABLE V. INPUT COMBINATIONS THAT PRODUCE THE SAME OUTPUT COMBINATIONS IN FULL ADDER CIRCUIT (SHOWN SHADED)

| Input | Output |
|-------|--------|
| A | B | Cin | C1 | C2 | S | Cout | G1 | G2 | G3 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

There are two fault tolerant reversible full adder circuits in the literature [11], [12]. The fault tolerant full adder circuit in [11] requires six parity preserving reversible gates (two FRGs and four F2Gs) and the fault tolerant full adder circuit in [12] uses four FRGs. This paper presents a new design of fault tolerant reversible full adder circuit that uses only two IGs, depicted in Fig. 8. It requires only two clock cycles.

A. Evaluation of the Proposed Full Adder Circuit

Evaluation of the proposed circuit can be comprehended easily with the help of the comparative results given in Table 6.

1) Hardware Complexity: One of the main factors of a circuit is its hardware complexity. It can be proved that the proposed circuit is better than the existing approaches in terms of hardware complexity. For [12] the Total logical calculation is: \( T = 8\alpha + 16\beta + 2\delta \), for [11] the Total logical calculation is: \( 12\alpha + 8\beta + 2\delta \), and for our proposed parity preserving reversible full adder circuit, the Total logical calculation is: \( 8\alpha + 6\beta + 2\delta \). Therefore, the hardware complexity of the proposed parity preserving reversible full adder circuit is less than the existing counterparts.
The full adder is the basic building block in a ripple carry adder. The reversible ripple carry adder using the fault tolerant full adder (FTFA) is shown in Fig. 9 which is obtained by cascading the full adders in series. The output expressions for a ripple carry adder are:

\[ S = A \oplus B \oplus C_i \]  
\[ C_{i+1} = (A \oplus B) \cdot C_i \oplus AB \]  

![Figure 9. Ripple carry adder using the proposed FTFA.](image)

**Evaluation of the Proposed Ripple Carry Adder:** It can be inferred from Fig. 8 and Fig. 9 that for N bit addition; the proposed ripple carry adder architecture uses only 2N reversible IG gates and produces only 3N garbage outputs. Table 7 shows the results that compare the proposed ripple carry adder with those designed using full adders of [11-12]. It is observed that the proposed circuit is better than existing ones both in terms of gate count and garbage outputs.

### IV. Conclusion

This paper presents a new 4x4 parity preserving reversible gate called IG gate and demonstrates its universality by realizing all possible Boolean functions. A novel fault tolerant reversible full adder circuit using the proposed IG gates has also been presented and optimized in terms of gate count, number of garbage outputs and constant inputs. Reversible logic implementation of optimized fault tolerant N-bit ripple carry adder has also been presented. The presented adder architectures using the proposed reversible gate offer less hardware complexity and optimized in terms of area and power consumption.

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