Study and Analysis of Enclosed Gate FET’s

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Abstract. The characteristic and parametric dimensioning of Enclosed Layout (ELT) MOSFET with various geometric sizes and shapes has been taken into consideration for the study of irradiations and leakage at room temperature, which has been confirmed on several technological platforms. Using the most advanced technologies, parametric changes with minimum W /L ratios, layout area and input capacitance to reduce leakage current can improve the performance. The technique of hardening of the MOSFETs in contrary to total-dose radiation effects in space environment built in enclosure to the enclosed transistor for the elimination of edges, responsible of conventional NMOS transistors leakage path creation. High yielding, high level of integration, radiation immune, high speed, low costing and high volume production are the profit advantages of the enclosed layout.

1. INTRODUCTION

With the continual improvements in power consumption, cost and speed of metal oxide semiconductor integrated circuits (MOS-ICs) are meeting the worlds increasing need for electronic devices for automotive, communication, entertainment, computing and other applications [1][2]. Stimulation and enabling of new applications have been seen in turn of these new improvements. Quality of life and productivity have been improved greatly worldwide [3]. Logic gates prices have gone under dramatic drop. Proliferation of electronics has been powered by the prime engine of “Miniaturization” [4][5]. Making of smaller transistors and interconnects brings more fabrication of circuits on each silicon wafer making the circuits economical. Development in speed and power consumptions of the ICs has been the instrumental of miniaturization. Reducing the capacitance is another good thing done by scaling and effectiveness in the power supply voltage in lower power consumption [6][7]. At each technology node, switching frequency rise and doubling of the transistors count per chip has shown reduction in power consumption and capacitance per chip [8][9]. Scaling of conventional bulk CMOS FETs is gradually reaching its limits, as scaling of CMOS technology ensures the continued growth of semiconductor industry [10]. Power, cost and speed per function are improved by scaling with every new technology generation. The cost has gone down for producing each transistor [11] Error! Reference source not found.

Improvement in performances through miniaturization must cope with severe short-channel effects, parasitic capacitance and fundamental limitations of silicon material [13][14]. In order to circumvent these short-channel effects, some semiconductor foundries started investigating various solutions with latest device structures for upcoming generations technology, like of the Fully-Depleted SOIMOSFET, Double-Gate MOSFET, SiGe MOSFET, Junctionless Nanowire FETS, Vertical Slit FET, and Enclosed Layout MOSFET [15] [16].

3D semiconductors simulation has potential of being extremely useful as to the reduced amount of experimentation and fabrication requirement for complex devices when in developing and improving of semiconductor technology [17] [18]. Modelling 3D devices must resolve the scaling of the length, which being the challenge when nonlinear nature of semiconductor physics phenomenon’s in combination to it, requiring the often computational expensive simulation [19]. TCAD have the general ideas same as for the extraction of specific layer mask form either the GDSII or ore compositions and files containing the geometric information for the accessibility of the process of simulator as by the
conversions of these layout masks, also TCAD may have different applications and functions by enabling, the defining of the introductory mesh by user, layer intent, substrate materials, etc. the further providing of simplification in the process of simulation [20][21].

Several technologies have been confirmed irradiations at the room temperature. Room temperature irradiations on several technologies have been confirmed [22][23]. The technique of hardening of the MOSFETs in contrary to total-dose radiation effects in space environment built in enclosure to the enclosed transistor for the elimination of edges, responsible of conventional NMOS transistors leakage path creation [24][25]. High yielding, high level of integration, radiation immune, high speed, low costing and high volume production are the profit advantages of the enclosed layout and stacking [26][27].

By adopting gate-enclosed layout the approach of eliminating the leakage path can be done. Nevertheless, one enclosed-gate transformed from a two-edged-gate layout, having the yielding of circuit, being speed and power might be severely afflicted as of the parametric changes on layout area, minimum and effective W/L ratios, input capacitance, etc. process technologies and enclosed-gate style. Furthermore, the process technologies and enclosed-gate style lead to vary the aforementioned changes in circuit performance. Accordingly, assurance of the performance is equivalently when replacement by enclosed gate on two-edged gate for radiation hardening, it’s decisive to quantitatively define the yielding of NMOS with assorted gate styles and manufactures [28][29].

As the modern electronics advance in performance and speed, an increase in power leads to increase in the number of power rails. Due to optimized driver and minimized parasitic, a stacked-FET device with improved system efficiency. Of the past generations complementary-metal-oxide-semiconductor-FET performance has been enhanced as scaling of the gate stack perform a vital role. Reduced board space and increasing power consumption are the reasons for the high-efficiency, high density power supplies which have been a trend for communications equipment. Enabling of high-efficiency and high density solutions has been switched by stacked-FET [30].

Lack of a universal memory is reflected in diversity of products that is dense, fast, reliable, economical and durable. Which steers to the fragmented breakdown in flash memory device types. For hoarding the huge amounts of data in section, NAND flash chips are typically of higher density from which the data is read periodically, when drafting a technology for the use in applications the companies are hence obligated to make tradeoffs [31].

Section II describes the Future device technology with multigate conventional transistors.

2. Future Device Technologies

Performance, power dissipation, and chip area are the main focus area of the designing of low power circuits. The intensive part of the VLSI CMOS is the deep sub-micron regime. The constraint is to decrease the area of the device by reducing the dimensions. The supply voltage plays a major role in electronic devices in controlling energy consumption. The performance can be achieved by reducing the voltage and voltage of the supply. Power dissipation goes up as the technology scaling down of leakage. Reducing the leakage power dissipation considering device dimensions and relative parameters has been implemented by several technologies [4].

The offering of the capability for scaling to the nanometer dimensionality and continuing of progress, with the use of new semiconductor channel materials which in comparison to the Si have improved transport properties. III-V compound semiconductors, among the new channel materials, are more promising. The III-V semiconductor channel materials in MOSFETs are the brighter choice for the production of a higher mobility channel than silicon. The uses for which greater mobility can be used are to provide high driving current and high outputs or to allow MOSFET to be worked at low voltage for low power. The lower supply voltage of CMOS is around 0.5 V less than the logic with lower performance and lower yield current leading to the issue of higher yield and greater stable leakage current [32][33].

2.1 Multigate Transistor
Double-gate-SOI-MOS-FET was earlier “Fully-Depleted Lean-channel Transistor (DELTA)” when first fabricated, where the device is called “finger”, “fin”, or “leg” as tall and narrow silicon island is of what device is made up of. The FinFET has a structure similar to that of DELTA, called the “hard mask” has an exceptional existence of a dielectric layer on top of the silicon fin. For the avoidance of development of parasitic inversion channel by the use of the hard mask in devices at top corners.

Gate electrode wrapping over the channel region in vertical-channel, which is the planar MOS-FET having the other implementations being the Silicon on Insulator MOSFETs including the Gate-All-Around Device

The Silicon-On-Nothing-MOS-FET, the triangular-wire-MOS-FET, the “Gate-All Around device” being a planar MOS-FET with the channel region being encased over by gate electrode, the Δ-channel SOI-MOS-FET, and the Multi-Fin-XMOS (MFXMOS) are the other applications of vertical-channel and double-gate-SOI- MOS-FET.

Since the two components are not linked, the potential can be distinguished by a double gate and a multi-independent Gate-FET. The principal attribute of the MIGFET is the modulation of the threshold voltages of one of the gates by applying the bias to the other gates. The effects are identical to the body effects in Fully-Depleted-SOI (FDSOI) MOSFETs. Signal modulation is amongst the applications using the MIGFET [34][35].

2.2 Double-Gate and FinFET

The Double-Gate MOSFET as represented in figure 1, demonstrated how the addition of a completely depleted SOI device among two gate electrodes would result in a massive reduction in the short channel effects. This design could provide better control over the area of the depleted channels than the conventional SOI MOSFET, with less impact on the channel in particular, of the electric field through the drain. The first MOSFET produced was the "fully-depleted-transistor-lean-channel." The device was manufactured in the narrow and high-silicon region known as "n." A modification in DELTA has structured FinFET that, apart from an oxidizing surface (called the "hard mask"), has a structure similar to that in the silicon of DELTA. The "hard mask" has been introduced in the high section of the device to avert the genesis of parasites in the inversion corners. MIGFET is a multi-gate device that has unlinked gate electrodes that can be jaded by various voltages. MIGFET's main feature is that the device threshold voltage can be changed by adjusting the potential at one gate [36].

2.3 Gate-All-Around

Gate-All-Around (GAA) FET has been identified to offer the best alternative to short-channel effects (SCE) with higher current-drivability per layout footprint because of vertically-stacked 3D channels [4] shown in figure 2. In comparison to vertical NWs requiring more interruptive technological changes, horizontal GAA NW and NS also have the benefit of being developed with limited deviations from
FinFET (FF) devices.

An effective all-around gate-ring (GAAR) vertical integration MOSFET design, basically a double-gate-shaped Arc-FinFET, that benefits from GAA MOSFET superior gate power, as well as viability. This new structure delivers further benefits of tunable output by adjusting the ring sizes, which provides easy circuit design versatility for specific SoC application performance requirements, particularly for vertical transistors with the same ring size. It can be asserted that the use of vertical GAAR sees a reduction of about 40 percent in the area, accomplished by projecting vertical enclosed geometries in comparison to traditional MOSFETs [37].

2.4 Triple-gate-SOI-MOSFETs
Figure 2 displays triple gate-MOS-FET (TG-MOS-FET) as a thin film that is enclosed with the narrow silicon island on three sides. The tri-gate- MOS-FET and the quantum-wire Semiconductor-on-Insulator (SOI) MOSFET is included in execution. The extending of the sidewall will only to a limited degree increase electrostatic comprehensiveness of the Triple-gate-MOSFETs in the subsections of the gate electrode in the submerged oxide and under the channel area (Π-gate device and Ω-gate device). The electrostatically noticeable Π-gate and Ω-gate device MOSFETs have a significant number of gates between 3 and 4. The current drive strengthening is augmented by a stretched silicon as a gate isolator utilizing a metal gate or dielectric high-capacity [38].

2.5 Surrounding gate (quadruple-gate) SOI MOSFETs
The surrounding-gate MOS-FET is theoretically the structure that suggests the best feasible Electrostatic Integrity and the channel regions optimum possible control of the by the gate. The fabrication of the first surrounding-gate-MOS-FETs was with the enclosing of a gate electrode about an upright silicon pillar as shown in figure 2. Such devices are composed of the CYNTHIA (circular segment device) and the MOSFET (square segment device) column. Recently, planar square or circular cross-sections of circumambulating gate devices have been found. SOI-MOSFET's surrounding gate is fully functional with a length of 5nm and a dia. of 3nm [39].

3. EFFECTS OF CHANNEL SHAPES ON MOSFET
Nanowire field-effect transistors (NWFETs) have recently been increasingly attracted by gate-all-around (GAA) due to their superior gate controls and short channel effects. Instead of the ideal round-shaped and square-shaped, the confinement of limitation of the manufacturing process causing the different
aspect ratio resulting different shapes cross-section of a channel causing to ellipse-shaped or rectangular shaped [40][41].

3.1 S-shaped vertical GAA MOSFET

The vertical S-shaped gate All Around MOSFET is the half channel cross-section. The elongated rotating section of the channel is rounded to remove the corner effect. The SGAA devices are interlaced one by one with a single channel width for designing the channel gap for high-density designs.

An outer section of the attributable system, i.e. an enclosed channel that is half the S-shaped channel (1 s-shaped= 2 MOSFETs), may also be used to produce a high-density design as shown in figure 3 [42][43].

3.2 Funnel-shaped transistors

A funnel-shaped transistor is more resistive towards hot electron effects when functioning close to the drain in the wider channel region. Moreover, this effect can be taken as an advantage by the transistor designs in the future to achieve optimum hot-electron-resistant transistors [44].

It is generally considered that hot electrons induced in the channel region near the drain result in an undesired substrate and gate currents and severely restrict future short-channel transistor efficiency and scalability. That refers in addition to n-channel transistors, which, a relative with their p-channel equivalents, are more prone to hot electron degradation than it would otherwise be. Although being undesirable for standard transistor activity, the hot electron effects are commonly used as the origin of programming of float-gate non-volatile memories quite before hot-electron effects are inevitable in standard transitive operation.

![Funnel-shaped transistors](image)

**Figure 4.** Funnel-shaped transistors

Even though rectangle-shaped conventional transistors are so common and widely employed, it has been suggested to enhance the programming efficiency for non-volatile memory applications to use a floating-gate transistor with a thinner channel region towards the drain area. The probability of counteracting unwanted hot electron effects in standard transistors through the action of funnels shaped transistors as shown in figure 4 in a different mode, i.e. the wide channel region near the drain, is thus interesting to be studied.

3.3 Circular ring-gate MOSFETs
Circular MOSFET ring gate parameters for the extraction from the measurements of parameters connected to a standard lateral part of gateway region are designed to deduct peripheral contributors, linked to sources and drain regions. Designing of the sets of test structures, having the radius $r_g$ to the centre of gate to which it always remains the same as shown in figure 5. The width of gate $W$ can, therefore, be determined by the centre and in all cases, the overall perimeter of the gate is $2W$ [43] [45] [46].

![Figure 5. Ring-gate MOSFET](image)

![Figure 6. SOI H-type body-tied MOSFET](image)

### 3.4 SOI H-type body-tied MOSFET
The drain current may be controlled by the length or width of the door due to its external gate area. Drain current poses a serious problem, particularly in the analog circuit design. Indeed, there is not a layout involving the gate shape effect even in the current version of BSIMSOI [47].

For the first time, a fair and universal SOI H-type body-tied simulation MOSFET design as shown in figure 6 has been suggested. Contrasted to the existing design, the simulation performance of the proposed model has enhanced substantially in the case of a 10% RMS error.

### 3.5 U-shape MOS

![Figure 7. U-shape MOS](image)

U-shaped MOS is MOSFET including a channel of 10 nm and source/drain poly-si. When a uniform thin film is coated on the channel region of each transistor over the full wafer [48] the complete coverage of the whole wafer is not required. A technical method was presented using the source/drain system in which the S / D content acts as a seed for CVD MOS$_2$ formation in the channel region from the source to the drain as shown in figure 7. The design introduced is cost-effective and uses common
fabricating equipment for semiconductors.

It would be difficult to develop large quantities of fast devices working at low power without the exceptional transistor miniaturization. No one disagrees with this state of affairs in the semiconductor industry. A linear transformation of a particular generation of transistors with the same criterion for the scaling mechanism is done employing three design factors (voltage, doping intensity, and physical proportion). The constraints of the scalable-down system are the diminished voltage, vertically and horizontally measuring and enhanced doping levels [49][50]

To cover the factors affecting the MOSFETs in various shapes, therefore moving towards the enclosed gate layout with the elimination of sensitivity and an irradiation factor.

4. GATE ENCLOSED-MOSFET

The architecture techniques for the secure functioning of microelectronic systems under radiation environments such as those in space or nuclear implementations have lately been presented utilizing new CMOS sub-micron technologies. Use moderate net charge trapping and a slight voltage threshold change even after high-dose irradiation, ultra-Thin Power Oxides are inherently resistant to radiation [51].

Although concerning the other gate oxide damaging mechanisms, as of the gain in the low field leakage over oxide by thyself can be activated. Contrarily, thick oxides in the quarantine areas of the CMOS still have their presence and sensitivity to the radiation damage quite can be seen. Altogether, positive charge trapping effects to, rise in various leakage current paths by induction of the development of an inversion layer by the ionizing radiation at the shallow trench corner or beneath the field oxide around NMOS [52][53].

As switching on of parasitic transistors, leading the failure mechanism with the growth of drain-to-source leakage current which MOSFET with gate-enclosed layout can constructively survive, to employing their way to traditional affluent environments and radiation affluent environments.

Slow operating time due to large input capacitance in comparison to the standard layout, and occupying a huge area are the primary flaws of these devices. Such flaws can partially be overcome/compensated by deploying aggressive CMOS techniques like sub-quarter and quarter micron technology [54][55].

Figure 8. The transistor shapes of the gate enclosed are: (a) circular (b) square (c) stretched edge rectangular and (d) square with a corner split at 45°(broken corners). Drain (D), gate (G), spring(S) and gate measurements are shown.

At present, this issue can be dealt with for specific forms: circular, square, or hexagonal as shown in figure 8 [56]. To support this, researchers have evolved original models for identifying the useful aspect ratio W / L of GE devices derived from a logical perspective to the problem. With different layouts of different technologies, experimental calculations have been rendered and measured beginning from a minimum size of 0.25 to 2.5 μm. Numerical simulations were also done in 2.5-μm technology [57][58][59][60].

The role of the parasitic capacitance is assertive as the urge of new electronic devices with higher
resolution and speed, in addition to lower power consumption. More linear and faster devices are resultant of low parasitic with an increase in high performance. Its importance is shown in the communications circuits and multiplexing of the signals to the output in high-speed applications. Consequently, promising characteristics have been shown by the closed or doughnut transistors, were ring transistor being the widely used doughnut topology. The advantage of using this approach as of reducing the parasitic capacitance, which favoring the high operation speed. Drain diffusion in doughnut transistor is encompassed by the transistor C/S, while the permitting of substantial W/L ratios over the side by side connections of various least dimensions cells.

Dominant the role of the parasitic capacitance becomes, with an increase in the urge of the modern electronic devices with the high speed and resolution competence with also the merit of low power consumption. Faster devices and the more linearity is a result of an increase in the dynamic performance as to the low parasitic. Communication signal and the high-speed application as to where the particular importance of this is seen were the multiplexing of multiple signals to the output. Therefore the promising characteristics have been shown by the closed or doughnut transistor having the widely used doughnut topology being the ring transistor. Having this advantageous approach of reducing the parasitic capacitance which favoring the high-speed operations. The transistor channel and source surrounds the drain diffusion in the doughnut transistor, while the permitting of the huge W/L ratios across the side by side connection of various least dimensioned cells with a reduction in the area and perimeter of the yield diffusion. Where the drain terminal has an appearance in the decisive signal path in those applications the large source junction capacitance limits their use. In the field of area and reliability, the ELT proves its ESD (Electrostatic Discharge) performance is better than the standard MOSFETs. But this design is based on ESD measurements performed in the traditional approach. Static, short signal and noise yielding of the ELT are the focus of these models [61][62][63].

4.1 ELT design
ELT in figure 9 is shown in N-channel MOSFETs with an enclosed gate layout and p+ rings, where L is the least distance amid the drain and source, c is the corner length and d is the drain's side length after the drain has been chopped. The diffusion of the drain is enclosed by the source diffusion and the channel.

![Figure 9. Layout diagram of the ELT.](image)

![Figure 10. Electric field in the channel of ELT.](image)

The substrate contact and the source come nearer along with the reduction in drain resistance if the drain is kept in the middle. The square with an angle cut at 45º (broken corners) was chosen for manufacture and area convenience; among the various forms such as circle, rectangle, rectangular with strained sides, octagonal, and square with a corner cut at 45º (broken corners) were also pondered; The current flows mostly in two orthogonal directions in the broken corner geometry, allowing more consistency and compatible systems when compared to the octagonal device [64].

As shown in figure 10, the electric field on the ELT channel is anomalous. The conformal mapping technique is used to solve this electrostatic problem. The ELT could be divided into an edge and corner
transistors, presented in figure 9 in T1, T2, and T3 by observing the electrical field within the channel [65][66][67].

![Figure 9: Electrical Field Within the Channel](image)

**Figure 11.** Approximation of T1 and T2

The barrier between T1 and T2 lies amid A to D, and D lies between αL and C (corner point) as shown in figure 11, channel width (c); the channel length (√2L); α (0.05) is approximate [68].

**Table 1:** The channels effective width and length of T1, T2 and T3.

| Parameters | T1 | T2 | T3 |
|------------|----|----|----|
| Teff       | L  | L√(α² + 2α + 5/2) | √2 |
| Weff       | L₁eff /M₁ | L₂eff /M₂ | c  |

Where,

\[ M₁ = \frac{1}{2a} ln \frac{d}{(d-2\alpha L)} ; \]

And,

\[ M₂ = \frac{\sqrt{\alpha^2 + 2\alpha + 5} ln(1/\alpha)}{1 - \alpha} \]

**4.2 ESD model of ELT**

The grounded-gate NMOS structure is the most simple of the MOS ESD protection devices where the drain leads to a gate and I/O pad, the Body (B) and source (S) shortening with the ground. Figure 12 shows the intersectional side and the corresponding circuit of the grounded-gate ELT [69][70].

The DB junction occurs in contrast to the ground on the I/O sheet, called D, and is reverse-biased till breakdown then there is a multiplication of the avalanche and creation of electron-holes. The substrate current (I_{sub}) due to holes flows through the substrate resistance (R_{sub}) to the ground and a potential (V_B) is developed. As the regions B and S are shortened voltage V_{B}' develops across the BS PN barrier. As the voltage V_{B} is raised the BS junction turns on, triggering the NPN transistor.
This triggers the ELT to be switched on at $V_{t2}$, an ESD signal, and travel to a snap-back area to create a low-impedance low-holding-$V_h$ discharge channel [71].

**Figure 12.** A schematic cross-sectional view of ELT.

### 4.3 ELT model in BSIM

The basic current equation, at any point $x$ along the line, as per BSIM (Berkeley Short channel IGFET Model):

$$I_{ds} = WC_{ox}[V_{gst} - A_{bulk}V_{ds}(x)] \frac{\mu_{eff}E(x)}{1 + E(x)/E_{sat}}$$  

(1)

If $V_{gst} = V_g - V_{th}$, $\mu_{eff}$ is the efficient carriers' mobility, $W$ is the channel width of the device, $C_{ox}$ is the per-unit capacitance, $A_{bulk}$ is used to take bulk charge impact into account, $E(x)$ is the $x$ point electrical field and the saturation of drift velocity occurs at $E(x) = E_{sat}$.

From the Eq. (1)

$$E(x) = \frac{I_{ds}}{\mu_{eff}WC_{ox}[V_{gst} - A_{bulk}V_{ds}(x)] - \frac{I_{ds}}{E_{sat}}} = \frac{dV(x)}{dx}$$

(2)

The channel width is unchanged and consistent of $x$ for a typical MOS device; the channel width is variable of $x$ for the ELT. The ELT is bifurcated into three pieces for measuring $I_{ds}$. The MOS transistors with a trapeziform gate help in an approximation of $T_1$ and $T_2$ and the $T_3$ with regular MOS transistors [72][73][74].

Trapeziform Gate Width:

$$W^{T_1}(x) = d - 2ax$$

(3)

$$W^{T_2}(x) = L - \frac{2(1-\alpha)}{\Delta x} x$$

(4)

For illustration, $T_1$ is measured by integrating $x$ from 0 to $L$, and $V(x)$ is calculated from 0 to $V_{ds}$.  

$$I_{ds}^{T_1} = \mu_{eff}C_{ox}1 \frac{1}{M_1} \frac{1}{M_1+V_{ds}/E_{sat}L} (V_{gst} - A_{bulk}V_{ds}/2)V_{ds}$$

(5)

Where $M_1$ is,

$$M_1 = \int_0^L \frac{1}{W^{T_1}(x)} dx$$

(6)

Considering the velocity saturates effect, then Equation (5) becomes;
\[ I_{ds}^{T_1} = \frac{L}{M} C_{ox} \frac{V_{gst}^2 + A_{bulk} E_{sat} L}{v_{sat}} \]  

(7)

Where, \( v_{sat} \) is the saturated carrier drift velocity, which is;

\[ v_{sat} = \frac{\mu_{eff} E_{sat}}{2} \]  

(8)

The usable channel width and length of \( T_1 \) were determined from the expressions above and the typical BSIM transistors can approximate \( T_1 \). In a similar index, the determination of effective geometry parameters of \( T_2 \) and \( T_3 \) can be done. The BSIM system of \( T_1 \), \( T_2 \) & \( T_3 \) were designed using the functionality of the ELT parameters, and the entire BSIM transistors can be configured as a mixture. ELT’s drain current is;

\[ I_{ds} = 4 (I_{ds}^{T_1} + 2I_{ds}^{T_2} + I_{ds}^{T_3}) \]  

(9)

5. DIODE: STRIPE, SQUARE OR OCTAGONAL

This diode is a fundamental ESD and much less susceptible than an ultra-thin stress gate oxide. ESD is reverse biased during normal operation, but under ESD it biases forward and gives the ESD current a path to the ground. The ESD input to the ground is reverse biased during normal operations. The ESD results are based on the current density distribution depending on geometry. Thanks to the positive silicon electrical conductivity temperature coefficient, silicon areas with higher temperature bears added current and the temperature surge further. It represents a positive feedback called a thermal runaway. Since the current density at the system edge is not fully consistent, this positive feedback can add to current diode filament local development at high current densities. As a result, a local temperature rise ultimately hold-out the failure and leads to collapse zsa [75][76].

![Figure 13. N+ cross-section showing the desired low-resistance current path for negative ESD condition (continuous arrows), in the ESD substrate diode.](image)
Table 2. The three diode measurements are linear, octagonal and square with perimeter and area corresponding geometric parameters.

|                | A) Linear | B) Square | C) Octagonal |
|----------------|-----------|-----------|--------------|
| Perimeter      | \( P_L = 2a \) | \( P_S = 4a \) | \( P_O = 4a - 8x + 4 \cdot x\sqrt{2} \) |
| Area           | \( A_L = w \cdot a \) | \( A_S = a^2 \) | \( A_O = a^2 - 4 \cdot \frac{1}{2} x^2 \) |
| \( P/A \)      | \( \frac{P_L}{A_L} = \frac{2}{w} \) | \( \frac{P_S}{A_S} = \frac{4}{a} \) | \( \frac{P_O}{A_O} = \frac{4a - 8x + 4 \cdot x\sqrt{2}}{a^2 - 4 \cdot \frac{1}{2} x^2} \) |

**Figure 14.** Edge-cutting parameterized (0.1 to 0.5) 3D octagonal Diodes simulation result with TCAD-Maximum Temperature for a 100 ns long ESD occurrence with various N+ area widths: 0.2 μm, 0.4 μm, 0.6 μm and ESD present 1mA, 2 mA and 3mA, respectively.

When most of the current is centered on the diodes edges, it is important to maximize the P / A surface to region ratio. Therefore, colossal I / C parameters should be procured for ESD diode with a small P / A proportion. The linear layout is less favourable, as the P / A ratio of the geometrics in table 1 is the highest P / A for the square diode. For contrast, for larger square diodes the P / A ratio increases. With TCAD simulations this empirical assertion was checked. A template of two dimensions diode, shown in figure 13, it was carried out. The 2D diode model fits the cross-section of one of Table 2.

The N+ region was adjusted to the model variable and the N+ region was fitted with a TLP
trapezoidal current pulse. The current distribution density for N+ area widths 0.2, 0.6 and 1.2 microns collected. The TLP current has been scaled to 1, 3 and 6 mill ampere in the width of the N+ region. The most recent density is always assumed to be on the fringe of the N+ region. A proportion of the current enters the N+ region deeper, although for larger diodes it gets less significant. However, the density under the N+ area essentially leads to the present conduction of the smallest diode when the contrary sides are near together. This design makes better use of the capacity-associated IC layout area for the N+ region. A full ESD system consists of multiple smaller diode sections to achieve secure ESD output with the bulky current power \[77][78]. The ESD quality had only been studied up to now, but capacitance has not been taken into account. Figure 14, shows Edge-cutting parameterized 3D octagonal Diodes simulation result with temperature for a 100 ns long ESD occurrence with various N+ area widths [79].

The Cadence simulations, incorporating the parameters of the layout drawn-out from devised ESD devices, display a wide range despite identical N+ areas. The highest capacitance is in diode 2 with the shortest size. This is due to the large perimeter diode's broad sidewalls capacitance. Consequently, the I/C ratio could not be foremost despite the maximum current ability for the same N+ region. There has been a similar effect. Nonetheless, the I/C of the tiniest square diode yet being greater that of I/C of a rectangular if it corresponds to ESD's current capability. The diode 3–the rectangular diode with
minimum length—could be the best candidate. Every incremental change in diode diameter results in wide perimeter reduction without a substantial reduction in capability (for relevant comparison, the N+ region is held constant).

Figure 15. (a) Schematic image of 3D GAA -field-effect-Transistor, (b) The same as (a), (c)-(d) Double Gate All Around transistor.

Schematic image of the 3D GAA -field-effect-Transistor (GAA FET) with an origin length L_s, gate length L_g, drain length L_d and a diameter d is shown in figure 15(a). Atoms are represented by red dots. The channel of semi conductivity is enveloped in a single yellow layer, which is an oxide. Transportation of electron takes place along the x-axis and y and z are containment directions. Figure 15(b) the same as (a), but for a body-thickness t-body 2-double-dimensional. Figure 15(c-d), is the Double Gate All Around transistor characteristics curves plot using TCAD simulator.

To support research work and speed up the development of new device technologies, advanced technology Computer Assisted Design (TCAD) systems are needed. This calls for precise simulation methods whose main ingredient is the design of bands on which they depend. The latter describes the material properties of the devices discussed, which may decide the usability of the unit entirely.

6. FINDINGS AND RESEARCH GAPS

Over recent decades, continued decline over planar MOS transistors has guided a sustainable development in integrated circuit technology. The technological scaling down contributed to the multiple-faceted development of the integrated circuit (IC) system to enhance performance, speed and ULSI incorporation, etc. Nonetheless, because of severe SCE’s such as DIBL, subliminal swing (SSS), velocity saturation, large drain current, etc. in ultra-small transistors, the efficiency improvement based on a steady downsizing of transistors has reached the choke point. The two- dimensioned effects (SCE and DIBL) are becoming ever more significant as the dimensions of the device reach the sub-micron dimension. Even if the continuous scaling paradigm is implemented, incremental field approximation is null and a field is changed significantly. Owing to a much slower voltage drop in actual circuitry in contrast with the criteria for constant field scaling the field still decreases. Through general scaling theory, this requirement for continuous field scaling has been presented.
In radiation situations, transistors with a gate-closed configuration can be used to avoid any leakage current from beginning via the radiation causing a lateral path under the shallow trench corner. The included configuration of the gate incorporates non-standard device contour and has been studied on the influence of MOSFET attributes. The issue of determining the MOSFET aspect ratio for screened gate-enclosed forms has been clearly outlined by researchers. To contextualize the drain current formulation in a low drain bias, disparate models have been established for this purpose.

For the circular devices, an answer to the subsequent challenge of circular symmetry was suggested for the simplistic model. For rectangular, split square and rectangular MOSFETs growing model complexity was necessary. In certain devices, the transistor has been segregated into two or three separate portions, which provide the total drain current and the proportional value separately. To state the boundary across the corner and edge transistors a suitable parameter ($\alpha$) was mandated.

The electrostatic case has an outspread uniformity in circular devices and the systematic $W/L$ representation is found effortlessly following the extrapolation of the mid-channel. Such an estimate occurs unless the drain radius is bigger than channel length with empirical discoveries. Modeling of the aspect ratio $W/L$ in square and recto-angular devices was centered on the decomposition of the edge and corner transistor Gate Enclosed (GE-MOSFET). A third contribution (linear corner) had to be taken into consideration in broken corner square devices. The solution of the electrostatic issue via a conformal mapping approach enabled such a decomposition possible

Scale-up of the gate stack was a key to improving the efficiency of CMOS-FETs for the earlier generation of technology.

The major benefit of this technique is that the constraints need not all be ramped by one factor compared to the constant field scaling. Nonetheless, the manner the minimal channel length is defined is a downside. Furthermore, the MOSFET scaling comprises a minimum of five main design dimensions ($L_g$, $t_{ox}$, $V_{dd}$, $N_a$, $x_j$). Depending on all five factors, the standard electrical behaviour of the device is under the impact of the SCE and DIBL.

7. CONCLUSION
In these settings, annular transistors are plied, as they operate more accurately and reliably for conditions where radiation can be exposed. Submicron processes can gain radiation intensity by adding narrower oxides that render lower ionization charges, greater substrate doping and entered channel operations. The complexity of the specified rad-hard technique is a low volume requirement and area efficiency logic.

The leakage pathways below the beak of a bird or shallow trench corners are the biggest benefactors to the TID influence of NMOS in progressive CMOS technology accompanied by thin-gate oxides. The typical MOSFET configuration constitutes a drain and a source, divided by a width (W) and length (L) of the channel. The transistor having the drain/source diffusion in the middle, encircled by the channel and source/drain, is GE-MOSFET (or annular MOSFET) Putting the drain amid at hand to the source draws the substrate contact together and decreases the drain resistance. As a result, this setup provides a better yield conduction and is the individual research evaluated. Different possible prospective disseminations can be reported alongside the transistor channel by contrasting traditional and GE transistors.

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