AXES: Approximation Manager for Emerging Memory Architectures

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ABSTRACT

Memory approximation techniques are commonly limited in scope, targeting individual levels of the memory hierarchy. Existing approximation techniques for a full memory hierarchy determine optimal configurations at design-time provided a goal and application. Such policies are rigid: they cannot adapt to unknown workloads and must be redesigned for different memory configurations and technologies. We propose AXES: the first self-optimizing runtime manager for coordinating configurable approximation knobs across all levels of the memory hierarchy. AXES continuously updates and optimizes its approximation management policy throughout runtime for diverse workloads. AXES optimizes the approximate memory configuration to minimize power consumption without compromising the quality threshold specified by application developers. AXES can (1) learn a policy at runtime to manage variable application quality of service (QoS) constraints, (2) automatically optimize for a target metric within those constraints, and (3) coordinate runtime decisions for interdependent knobs and subsystems. We demonstrate AXES' ability to efficiently provide functions 1-3 on a RISC-V Linux platform with approximate memory segments in the on-chip cache and main memory. We demonstrate AXES' ability to save up to 37% energy in the memory subsystem without any design-time overhead. We show AXES' ability to reduce QoS violations by 75% with < 5% additional energy.

Keywords Approximate Computing, Memory Hierarchy, Model-free Control, RISC-V

1 Introduction

As applications become increasingly resource-intensive, trading off performance and energy in battery-powered systems is crucial. Application profiling has revealed memory-accesses as one of the most significant performance, and energy bottlenecks [1]. Approximate memory is an effective way to alleviate the energy bottleneck in memory for applications that can tolerate output errors caused by inexact memory load/store operations; potentially improving energy consumption, leakage power, latency, or lifetime. The inexactness stems from relaxing the need for high-precision storage for some data structures in the application.

Approximation techniques for different types of memories with configurable degrees of approximation have been previously explored [2,3,4,5,6,7], but are typically limited to one or a few levels of the memory hierarchy. A holistic solution would need to manage approximation knobs (e.g., V_DD for SRAM caches, t_REF for DRAM main memory) across the entire memory hierarchy, from cache to main memory, in order to fully exploit memory approximation opportunities. Furthermore, runtime dynamic reconfiguration of approximation knobs is required to fully leverage the performance/energy tradeoff while honoring application goals, e.g., quality of service (QoS) targets, and system constraints, e.g., minimize energy consumption.

Current approximation techniques using runtime dynamic reconfiguration still depend on the design-time modeling of workloads (application along with input) to determine the optimal knobs of operation for a specific system configuration. Such techniques are application-specific and cannot be ported to new systems. However, memory technologies are
changing very rapidly, and design-time workload profiling dependency introduces significant overhead to utilize approximate memory in emerging memory technologies. Furthermore, runtime dynamic reconfiguration across the memory hierarchy requires coordination between multiple knobs (e.g., $L_1V_{DD}$, $L_2V_{DD}$, and DRAM $t_{REF}$). Coordination is challenging because knobs in one layer can affect other subsystems directly or indirectly (e.g., write errors in $L_1$ affect reads in higher layers).

Consider the system shown in Figure 1. The memory hierarchy (in this case: $L_1$ cache, $L_2$ cache, and main memory) exposes tunable knobs (e.g., operating voltage for $L_1$ and $L_2$, and data refresh period for main memory) that control the degree of approximation. Each knob introduces a new degree of freedom and increases the configuration space exponentially. Furthermore, satisfying even a single-objective function poses non-trivial optimization challenges, with an additional level of complexity arising from the optimization of multiple objective functions to determine the optimal system configuration. Researchers have proposed frameworks for exploring the configuration space at design-time and determining static optimal knob settings for an approximate memory hierarchy before deployment [8,9]. More flexible solutions have been proposed to provide dynamic configuration of knobs at runtime but require identifying workload-specific system dynamics at design-time [10,11,12]. Apriori knowledge limits the ability to adapt to changing workloads, and further assumes that the system and workload are observable ahead of deployment. On the other hand, determining the optimal knob configuration for unknown applications and new inputs at runtime is an extremely challenging decision process.

To address these challenges, we develop AXES, a model-free method to tune memory knobs without any previous knowledge about the system (memory-hierarchy as well as the workload). AXES eases the design of systems with approximate memory by enabling deployment without going through design time exploration of configuration knobs. AXES’ methodology is independent of the underlying memory technologies and works regardless of the nature of knobs. Once deployed, AXES can learn the optimal knob configuration for unknown applications, resulting in self-optimizing systems.

The main contributions of this paper are as follows:

1. Enable self-optimization of multi-level memory approximation knobs through AXES, a runtime resource manager using reinforcement learning. Self-optimization is demonstrated by finding the system configuration for unknown workloads at runtime, as well as the dynamic management of quality of service (QoS).

2. Enable coordination between multiple memory system knobs without explicit communication. Coordination is demonstrated through dynamic runtime reconfiguration of multiple knobs by continuously evaluating different subsystem configurations (e.g., ↑ $L_1$ knob, ↓ $L_2$ knob, vs ↓ $L_1$ knob, ↑ $L_2$ knob).

3. An approximate memory management approach that is (a) technology agnostic, (b) application-independent, and (c) can easily be applied to any multi-level memory hierarchy.

4. Experimental case study: A software implementation of AXES is evaluated using an FPGA board with a modified RISC-V processing core to validate the approach.

We believe AXES will enable quick adoption of approximation using a variety of memory nodes.
2 Motivation

The QoS delivered by a given configuration of approximation knobs varies widely based on the application and current input. Even for a fixed workload (application and input), the configuration space grows exponentially with each additional knob (e.g., one knob = 4 states, two knobs = 16 states, three knobs = 64 states). More examples of approximation knobs for different memory technologies are presented in Table 1. In a memory hierarchy, knobs are at least partially interdependent: changing one knob affects multiple subsystems in ways that are complex to predict. (e.g., changing L1 $V_{DD}$ introduces errors in L1, which subsequently propagate to L2.) This makes the configuration problem extremely challenging.

2.1 Case Study

To illustrate this challenge, consider a system equipped with an approximate memory subsystem, as shown in Figure 1. The application’s source code is annotated with a quality monitor and is running on a system that supports approximate memory. The approximate memory subsystem consists of three layers of hierarchy, including an SRAM L1 cache memory, an SRAM L2 cache memory, and a DRAM main memory. These memories have an ‘exact’ and ‘approximate’ region in which application data can be mapped. The degree of approximation varies based on the memory technology: in this work, the voltage level for SRAM cache and refresh rate for DRAM main memory. Approximation can be controlled at each layer of the memory hierarchy, and the knob setting impacts the application QoS measured by the quality monitor. `malloc` calls from the application to the Linux kernel are modified by the developer to indicate which data can be mapped to approximate regions. The complete experimental setup is described in Section 5.

Figure 2 is an illustrative example showing variations in QoS observed across different configurations of L1 and L2 approximation knobs, as well as across different applications. The DRAM knob is fixed for the sake of simplicity. The dots’ size represents the QoS (i.e., number of errors, smaller is better). We observe the effect of configuration knobs on two applications:

- **Application A**: A memory write-read kernel that writes 512 64-bit numbers in the main memory and then reads the numbers from main memory. The QoS metric for this kernel is defined as the total number of bit flips that occur during the write-read cycle. The QoS and average energy for each knob configuration is shown in Figure 2a.

- **Application B**: The Canny-edge detection application as described in Section 5.2. The QoS metric for this application is the $rmse$ (Root Mean Square Error) between the pixels of the approximate runs and the exact runs of the application. The QoS and average energy for knob configurations corresponding to two different inputs (i.e., scenes), B1 and B2, is shown in Figures 2b and 2c respectively.

We make the following key observations: First, we observe that configurations achieving a target QoS vary both within and between applications. In Figure 2, we define a feasible region (dashed rectangle) by identifying the set of configurations that achieve acceptable QoS. Depending on the workload, the feasible regions of operation are different.
Table 1: Examples of approximate memory technology knobs.

| Technology | Memory Type | Technology Knobs | Knob objective | Reference |
|------------|-------------|------------------|----------------|-----------|
| Cache      | SRAM        | Operating Voltage ($V_{DD}$) | Energy savings | ASPLOS’12[13], ESL’15[12] |
|            | STT-RAM     | Read Voltage ($V_{read}$) | Energy savings | HPCA’11[14], CASES’15[14] |
|            |             | Write Pulse Duration ($t_{write}$) |            | ISLPED’17[15] |
| Main Memory | DRAM        | Data Refresh Period ($t_{REF}$) | Energy savings | ASPLOS’11[13], ISLPED’14[14] |
|            |             | Operating Voltage ($V_{DD}$) | Reduce Latency | MICRO’19[16] |
|            | PCM         | Data Comparison Write ($Th$) | Energy savings | Increase lifetime | MICRO’09[6], MICRO’13[5] |

The difference is seen in the varying bounding boxes of Figure 2a (Application A), and Figure 2b (Application B). Even within the same application, the acceptable regions of operation vary based on the dynamic inputs to the application at runtime as seen in Figure 2b (input B1) and Figure 2c (input B2).

Second, we observe that even within the feasible regions, the achieved QoS varies across applications and inputs. In some cases, the outer circle and inner circle are well separated, implying that there is still room for approximation. However, in some cases, the inner circle is very close to the outer circle, implying that the QoS is reaching its threshold.

Third, we observe that even the same configuration of knobs (e.g., L1:0.7 V, L2:0.9 V) have different power characteristics with respect to different applications and different inputs within an application. This results in varying optimal design points (marked with a star).

This simple example demonstrates that even for the same memory technology, it is hard to predict the resulting QoS and energy when knobs are changed in only two layers of the memory hierarchy; i.e., the dynamics between the system and application vary both within and between applications. We expect that finding the optimal configuration for additional layers of a memory hierarchy or new memory technologies will only exacerbate these challenges, with current state-of-the-art techniques (summarized next) insufficient for determining the complex interactions of knob configurations for multi-level approximate memories.

2.2 Approximation: State-of-the-art

2.2.1 Open-loop Control

A popular approximation strategy is to use design-time techniques to find optimal knob configurations [17, 16, 18, 19]. Based on the application profile, approximation knobs are determined before deployment and are expected to meet the QoS requirements throughout the application’s lifetime. For an open-loop system designers must design the system with the worst-case scenario in mind and are unable to exploit the full potential of the approximation knobs at runtime. Additionally, application programmers are burdened with the task of setting memory approximation knobs through intensive profiling of the target workloads at design time [16, 8, 10]. Thus, open-loop control techniques are application-specific and not portable to new systems.

2.2.2 Model-based Closed-loop Control

To address the lack of reconfiguration in open-loop systems, state-of-the-art alternatives reconfigure approximation knobs using closed-loop controllers [20, 21, 22, 23]. The controllers are generated based on a system model identified at design-time. Closed-loop control aims to alleviate the programmer’s burden at design-time by using feedback at runtime. Design-time models consider the difficulty of specifying an under-designed memory’s parameters by measuring the output accuracy in different settings. However, with the number of system parameters on the rise, system identification is becoming impractical for capturing the effects of one knob on another. Coordination in control theory requires a formal Multiple-input-multiple-output (MIMO) method, but designing a MIMO controller requires nontrivial design-time effort. Additionally, such models are rigid: models must be generated for each memory technology, with an underlying assumption that the system is available for observation ahead of deployment. Thus, closed-loop control techniques are also application-specific and suffer from significant design-time overhead.

2.3 Benefits of Model-independence

A static model identified during development does not take into account complex system dynamics (e.g., variability between applications). As the configuration space increases due to the increasing number of knobs, self-learning intelligent agents without apriori knowledge are attractive candidates to find optimal solutions through runtime
Table 2: Memory approximation approaches and the key challenges addressed (* = uniquely addressed by AXES).

| Features                  | EDEN [16] | Control Theory [11] | AdAM [10] | DART [8] | AXES |
|---------------------------|-----------|---------------------|-----------|-----------|------|
| Technology Independent    | ✓         | ✓                   | ✓         | ✓         | ✓    |
| Memory Hierarchy          | ✓         | ✓                   | ✓         | ✓         | ✓    |
| Application Agnostic      |           |                     | ✓         | ✓         | ✓    |
| Coordination              |           |                     | ✓         |           | ✓    |
| Self-Adaptivity           | ✓         |                     |           | ✓         | ✓    |
| Self-Optimization         |           |                     |           | *         | ✓    |
| Model-Independence        | ✓         |                     |           | ✓         | ✓    |
| Real System Evaluation    | ✓         |                     |           | ✓         | ✓    |

observation. Reinforcement learning [24] is a prevalent candidate in the field of self-learning agents, demonstrating success for decision-making for services such as recommendation engines and games. In this work, we utilize a model-free reinforcement learning approach to develop a model-free approximate memory controller that can learn the behavior of knobs through runtime experience. Model-independent control techniques can provide a general-purpose solution, independent of the application and system dynamics.

3 Background and related work

Approximate memory subsystems have been widely explored in the literature [25]. An integral step towards running an approximate application is to identify the non-critical sections of the data elements. Allowing faults in the critical data sections would lead to crashes and would require additional recovery mechanisms. Identifying non-critical data sections can either be done automatically [26, 27, 28], or through explicit programming language support [29]. Upon identifying the non-critical data, various memory approximation strategies can be implemented on systems, determined by underlying memory hardware technology. Table 1 summarizes some of the standard technologies utilized throughout the memory hierarchy, along with the approximation objective. AXES is technology-agnostic and can leverage all of the technology knobs described in Table 1.

Several methods have been proposed in the context of tuning the memory approximation knobs. Table 2 identifies the most recent and relevant research, and compares AXES to these prior works. We define self-adaptivity as the ability to adapt to user-specified application goals or system constraints (e.g., increased target QoS). We define self-optimization as the ability to find desirable system configurations given a fixed goal in the face of external disturbances (e.g., a scene change). Manual schemes rely on designer expertise to optimize approximation knobs (e.g., $t_{REF}$ in DRAM). In EDEN [16], Koppula et al. show the effectiveness of manual tuning for neural networks, which have an intrinsic capacity of tolerating errors in memory accesses. EDEN uses approximate DRAM to reduce energy consumption and increase the performance of DNN inference. EDEN is limited to machine learning workloads and does not apply to a multi-level memory hierarchy. The absence of a runtime quality monitor in EDEN prevents dynamic reconfiguration of the approximation knobs (e.g., row activation delay $t_{RCD}$, operating voltage $V_{DD}$).

Maity et al. [11] have proposed a solution to maintain a quality target at runtime by using classical control theory. Quality configuration tracking is modelled as a formal quality-control problem, and black-box modelling is used to capture memory approximation effects with variations in application input and system architecture. However, this scheme assumes only one level of the memory hierarchy is tuned at runtime and fails to address the problem of coordination between multiple knobs.

In AdAM [10], Teimoori et al. investigate memory approximation by managing approximation knobs across the memory hierarchy. AdAM solves a design-time ILP optimization problem and uses a runtime algorithm to adapt to new tasks by re-estimating the execution time. Although optimization techniques are a natural choice for simple architectural tuning, the lack of a feedback mechanism makes it too rigid for any sort of adaptivity (e.g., unknown inputs, and disturbances from other applications). Furthermore, their use-case only addresses a two-layer memory hierarchy, with an on-chip STT-RAM and an off-chip PCM Main Memory; and the design-time algorithm is technology dependent.

In DART [8], Yarmand et al. propose a framework for a three-layer memory hierarchy (SRAM L1, SRAM L2, and an off-chip DRAM) without any technology-specific assumptions. DART uses a branch and bound algorithm to consider all possibilities at design time, and creates a search tree to perform error probability analysis. Although DART considers the full memory hierarchy, it requires the programmer to: (1) analyze the program during design time, (2) generate a
memory profile for each application that would run on the system, and (3) estimate the worst-case probability of errors that would occur due to under-designed memory. Therefore DART requires a priori knowledge of the application and assumes that the system is available for full observation before deployment.

In the related topic of runtime resource management, machine learning approaches have gained traction recently. Researchers have investigated the feasibility of machine learning methods for quality configuration in the approximation domain [30, 31]. However, conventional machine learning methods require extensive training to learn the correlation between the system’s inputs and outputs. Static models that are defined ahead of deployment fail to handle new situations outside of expected behavior. Online learning methods aim to address this issue and have shown promising results for resource management [32].

AXES incorporates the features highlighted in Table 2 using online learning methods. The AXES’ approach improves upon prior work by eliminating design-time modeling, being memory technology-agnostic, and coordinating multiple knobs at runtime to exploit approximation for multi-level memory hierarchies; enabling quick adoption of approximation for diverse platforms.

4 AXES Methodology

Figure 3 presents the AXES’ realization of the logical architecture described in Figure 1 consisting of the following components: (1) a hardware platform with a processing unit, cache subsystem, and main memory. This hardware controls the degree of approximation at each memory layer by configuring the specific technology knobs available on the platform. Examples of technology knobs are in Table 1. The processor core contains special registers to set knobs (e.g., L1 $V_{DD}$ updated from 0.7 V to 0.8 V) through special instructions. For instance, in our current RISC-V realization of the processor, we deploy unused control and status registers (CSRs) for this purpose, as shown in Figure 5. Instructions that write to these CSRs form an extension of the processor’s ISA (RISC-V in our implementation), and are used to manage approximate elements at runtime. Truffle [13] is another example of a micro-architecture design that efficiently supports these ISA extensions for disciplined approximate programming. Instructions supported through these new CSRs include AX_ENABLE to enable approximation, AX_DISABLE to disable approximation, AX_L1_LEVEL to set the technology-specific knob for Level 1 cache, AX_L2_LEVEL to set the knob for Level 2 cache, AX_DRAM_LEVEL to set the technology-specific knob for DRAM. (3) A loadable kernel module that helps map the high-level knobs (e.g., low approximation) to technology-specific knob values (e.g., $V_{DD}$). For new technologies, the information in the module should be updated to reflect what the available actuation knobs are (e.g., available write pulse duration ($t_{write}$) for STT-RAM). The kernel module also allows applications to indicate which parts of the application’s virtual memory can be placed physically in the approximate regions (explained further in Section 5.3). (4) The user application running on this platform, specifying the non-critical sections of the data using an malloc_approx() call to (3) kernel module. (5) A quality monitor computes the QoS periodically at runtime and reports it to AXES. (6) The current power of the system is sensed using power sensors. (7) The expected QoS specific by the user. Expected QoS can be updated at runtime to adapt to different system objectives (e.g., a strict quality constraint optimizes AXES for more accurate executions, whereas a relaxed quality constraint optimizes AXES for energy savings). (8) The AXES Controller agent is the final component of the architecture and is responsible for runtime control of the memory approximation knobs. The AXES controller agent is a model-free runtime manager for tuning configurable approximation knobs throughout the memory hierarchy. AXES follows the observe-decide-act (ODA) paradigm: the environment is observed through sensors during normal execution, and the decision-making agent is periodically invoked in order to (re)configure the
system using knobs. We design our decision-making logic by first defining our problem as a Markov Decision Process \((S, A, P_a, R_a)\), where \(S\) refers to state space, \(A\) refers to action space, \(P_a\) refers to the transition probabilities from \(S \rightarrow S'\) given action \(A\), and \(R_a\) refers to the expected rewards for selecting action \(a\) in state \(s\). As is common when controlling real systems, we do not know the system dynamics and assume they change continuously. This is a well-known problem, and to address it, we apply an appropriate established reinforcement learning solution, namely temporal difference (TD) learning [34].

4.1 Design Methodology

Our goal is to design a decision-making agent that coordinates each layer in a unified 3-layer memory hierarchy to achieve acceptable application QoS while minimizing energy consumption. First, we must define the structure of our environment.

4.1.1 State Space (\(S\))

The state is a representation of the current system under control. In AXES, we define a state vector that consists of high-level approximation settings (e.g., no/low/medium/high approximation) of each memory layer, as well as the current QoS error:

1. L1D: current level 1 data cache configuration
2. L2: current level 2 shared cache configuration
3. Main memory: current main memory configuration
4. Discretized QoS error \((Q_{threshold} - Q)\), where \(Q\) is the measured QoS, and \(Q_{threshold}\) is the constraint)

This way, the state informs the agent what the current knob settings are, as well as how well they are achieving the goal of meeting the QoS requirement set by the application. This allows us to translate the dynamics between application behavior and hardware configuration. The QoS error is normalized to the worst-case QoS value \((\text{max}_Q)\) to make AXES portable across applications, and high-level knobs allow AXES to be independent of memory technologies.

4.1.2 Action Space (\(A\))

The action space contains all possible operations the agent may take to configure the system each time the agent is invoked. The AXES action vector consists of the relative changes to the high-level knobs for layers in the memory hierarchy:

1. L1D: Increase/Decrease/No change
2. L2: Increase/Decrease/No change
3. Main memory: Increase/Decrease/No change

Initially, the AXES policy does not have any information regarding what actions are desirable and must discover which actions yield the maximum reward in each state via exploration (e.g., when there is no QoS constraint, actions which decrease power yield the maximum reward).
4.1.3 Reward \((R)\)

The reward provides immediate feedback to the agent on how the previous state’s action helped achieve the system goal. In our case, this goal is to find the optimal configuration corresponding to minimum energy with acceptable QoS. Using the normalized power consumed measured at regular intervals, we define the reward in an unconstrained system by Equation 1:

\[
\text{reward}_P = 1 - \frac{\text{Power}}{\text{maxPower}}
\]

\[
\text{reward}_P \in \{x | 0 \leq x \leq 1\}
\]

where \(\text{Power}\) is measured power, \(\text{maxPower}\) is the power consumed when the approximation is disabled at all layers of the memory hierarchy, and \(\text{reward}_P\) is the reward obtained in terms of optimizing power. This function represents a power optimization objective with a target power of zero. In an unconstrained system, operating at the highest power yields no reward, while operating at zero power yields the maximum reward. However, we must constrain the total reward in order to account for the quality threshold.

The policy should take actions which minimize the number of violations of the quality constraint specified by the application developer. Thus, the reward of a quality violation is calculated in Equation 2 as:

\[
\text{reward}_Q = -\frac{Q - Q_{\text{threshold}}}{\text{maxQ}}
\]

\[
\text{reward}_Q \in \{x | -1 \leq x \leq 1\}
\]

where \(\text{reward}_Q\) is the reward obtained by staying within the quality constraint. In case of violations, \(\text{reward}_Q\) is negative indicating that an undesired action was performed by AXES, which led to a QoS violation.

Finally, the reward \((R)\) is calculated from the \(\text{reward}_P\) and \(\text{reward}_Q\) and reported to the agent by Equation 3:

\[
R = \begin{cases} 
\text{reward}_P, & \text{if } Q \leq Q_{\text{threshold}} \\
\text{reward}_Q, & \text{otherwise}
\end{cases}
\]

Algorithm 1 TD(\(\lambda\)) algorithm [24] for determining AXES policy.

|   |   |
|---|---|
| 1: | Algorithm parameters: step size, discount factor, trace decay \(\alpha, \gamma, \lambda \in (0, 1]\) |
| 2: | Initialize \(Q(s,a)\) arbitrarily, for all \(s \in S, a \in A(s)\) |
| 3: | for each episode do |
| 4: |   \(E(s,a) = 0, \forall s \in S, a \in A(s)\) |
| 5: |   Initialize \(S, A\) |
| 6: |   for each step of episode do |
| 7: |     Take action \(A\), observe \(R, S'\) |
| 8: |     Choose \(A'\) from \(S'\) using policy derived from \(Q\) |
| 9: |     \(\delta \leftarrow R + \gamma Q(S', A') - Q(S, A)\) |
| 10: |     \(E(S, A) \leftarrow E(S, A) + 1\) |
| 11: |     for each \(s \in S, a \in A(s)\) do |
| 12: |       \(Q(s,a) \leftarrow Q(s,a) + \alpha \delta E(s,a)\) |
| 13: |       \(E(s,a) \leftarrow \gamma \lambda E(s,a)\) |
| 14: |     end for |
| 15: |     \(S \leftarrow S'; A \leftarrow A'\) |
| 16: | end for |
| 17: | end for |

4.2 AXES Agent: Model-free Control

Given the definition of the environment and goals, we simply need a decision-making mechanism (AXES) to find the optimal policy. Initially, the AXES agent does not have any information regarding the environment and explores the state-space by taking purely arbitrary decisions (actions). It uses temporal-difference (TD) learning [24] to learn directly from raw experiences without a model of the environment’s dynamics. Figure 4 shows the logical structure of the AXES agent and its relation to the environment, i.e., system under control. The agent interacts with the environment through actions, and the environment provides rewards and updated state information to the agent.
Actions that lead the system to optimize power without violating quality constraints are rewarded well. The policy is modeled as a state-action value function by keeping track of all the state variables, along with the possible actions in the form of a table. Q-learning [35] is a popular TD control algorithm. Q-learning aims to learn a state-action value function, $Q$, which directly approximates $q^*$, the optimal state-action value function. A variation of Q-learning combines eligibility traces to obtain a more general method that may learn more efficiently. Eligibility traces look backward to recently visited states and act as short-term memory. This algorithm, where Q-learning is combined with a backward short-term memory using eligibility traces, is known as TD($\lambda$) [34].

AXES uses the TD($\lambda$) algorithm to update and optimize the approximation management policy throughout runtime continuously. The detailed algorithm is outlined in Algorithm 1. The dilemma presented during any controller designer is determining control parameters, whether the implementation uses classical control theory or reinforcement learning. In the TD($\lambda$) algorithm, learning parameters have interpretable meaning, so can be set several ways, e.g., using designer intuition or empirical observation. In our case we determine learning parameters ($\alpha=0.6$, $\gamma=0.1$, and $\lambda=0.95$) empirically by simulating our control logic on system traces for canny. No matter the controller deployed, these parameters must be determined. However, we define our control logic in such a way that the parameters apply to the type of control (i.e., memory approximation knobs), as opposed to the application under control (i.e., edge detection).

A Q-table is formed that maintains the Q-value of each state-action pair (Figure 4). The agent is invoked periodically and performs the following steps during each invocation:

1. Measure the power and QoS to evaluate the reward $R$
2. Update the table ($Q$ values) based on reward $R$
3. Sense the current approximation levels and QoS to determine the current state $S$
4. Given the current state $S$ and updated $Q$ values, select next action $A$

### 4.3 AXES Case Study

As described earlier, Figure 5 outlines the AXES system architecture, with the AXES Controller agent in software responsible for runtime control of the hardware memory approximation knobs. Our implemented environment consists of a unicore RISC-V processor with a three-layer memory hierarchy: L1 SRAM data cache, L2 SRAM shared cache, and DRAM main memory. AXES is implemented in software and runs in userspace. A Loadable Kernel Module
Table 3: System configuration used for AXES evaluation.

| Component                  | Configuration                      |
|----------------------------|------------------------------------|
| Cores                      | 1                                  |
| TLBs                       | Number of entries (16)             |
| L1 D-Cache                 | Number of sets, ways (16kB, 4-way) |
| L2 Cache                   | Number of sets, ways (64kB, 4-way) |
| Floating-Point Unit        | Present                            |
| Main Memory                | Onboard (512MB 800MHz DDR3)        |
| Clock frequency            | 30 MHz                             |

accompanies AXES which incorporates the device specific translations from high-level configurations (e.g., 25% approximation) to technology specific values (e.g., 0.9 V for SRAM caches).

The state vector \( S \) is made up of (1) high-level configurations corresponding to memory layers, and (2) the QoS error. Discrete integer values represent all of the vector values. The L1 and L2 voltage levels \( (V_{DD}) \) are between 0.7-1.0 V in increments of 0.1 V [8]. The main memory refresh periods are 0.1 s, 1 s, 5 s, 20 s [4]. The QoS error is normalized and discretized into 16 buckets of step size \( \log_2{16} \). The inclusion of the QoS error in the state differentiates desirable actions for the same voltage level, depending on the QoS error explicitly.

The action vector \( A \) contains a field for adjusting each of the L1, L2, and main memory knobs. The possible knob configurations are voltage levels for cache L1 and L2 and refresh periods for DRAM main memory. Actions for each knob only consist of increase by one, decrease by one, or remain the same. To keep the action space manageable, we performed a sensitivity analysis on the knob in each memory layer. Figure 5 shows the sensitivity analysis of the approximation knobs on the output QoS and power. We make three observations. (1) As we move up the memory hierarchy (i.e., from L1 to L2 to main memory), the quality is less affected by higher degrees of approximation. (2) The contribution of memory power from individual levels of hierarchy varies. Although main memory techniques can save around 23% DRAM power, when the full memory hierarchy is considered, DRAM’s power savings saturates at 12%. (3) Having four knob configurations captures the range of power/quality trade-off effects while keeping the state-space manageable. We conclude that four knob configurations for each level provide sufficient control for reaching our goal.

Reward \( R \) is calculated based on Equation 3. To evaluate the reward, AXES uses software level sensors to determine the application’s output quality. Although the metric is domain-specific and is generated by a quality monitor, normalizing it to the worst quality keeps AXES domain agnostic. We update \( Q \) values using the reward as specified in Algorithm 1.

To demonstrate the efficacy of AXES for coordinating knobs in the memory hierarchy, we deploy a hardware platform that mimics the effects of approximation. The effect of approximation knobs in each layer in the memory hierarchy is determined using existing models in literature [8, 4].

5 Experimental setup

For the AXES architecture described in Section 4, we describe our experimental setup for the RISC-V hardware platform on which AXES is running (1 in Figure 3). An overview of our evaluation platform is shown in Figure 6. We implement AXES in software running on Openpiton [36], an open-source framework designed to enable scalable architecture research prototypes. We use Openpiton with a single Ariane [37] core, a 64-Bit RISC-V core capable of running Linux. The framework is synthesized on a DIGILENT NexysVideo board, having a Xilinx Artix-7 FPGA(XC7A200T-1SBG484C). The parameters used to synthesize the system are summarized in Table 3.

5.1 Modifications to RISC-V Core

We further modify the Ariane core to support fault injection throughout the memory hierarchy. The synthesized core, running on the NexysVideo board, does not have an option to configure real knobs for approximation. However, we rely on existing works that map device-specific approximation knobs to the observable bit error rates [8, 4]. Thus, we introduce bit errors through fault injection in order to emulate the effect of approximation knobs.

5.1.1 SRAM Fault Injection

The RISC-V specification defines separate addresses for Control and Status Registers (CSRs) associated with each hardware thread [38]. Unused CSRs are utilized by the kernel to communicate information required for the configuration
of the approximation knobs. In Figure 6, additional CSRs are denoted with ①. In particular, the following information is stored in CSRs:

1. L1 data cache Read and Write Bit Error Rate
2. L2 shared cache Read and Write Bit Error Rate
3. Starting and Ending physical address of the non-critical memory segment

The Bit Error Rates correspond to specific memory nodes and are translated from technology-specific values described in Section 5.5. The information from the CSRs is propagated to the ② Memory Management Unit (MMU), where address translation takes place. MMU uses this information to generate an additional approx bit along with the index and tag bits to indicate that this address is within the valid range of approximation. The approx bit generation is repeated whenever a virtual address is converted to a physical address. The approx bit in conjunction with the CSRs for Bit Error Rate is utilized by the cache controller to control the degree of approximation and contain it to the non-critical parts of the application. A Fault Injector (FI) module is used to emulate the effects of approximation by introducing the bit flips on the memory bus. Four FI modules are instantiated in the cache subsystem as shown in Figure 6. The FIs are located in (1) Data Cache Memory emulating the bit flips corresponding to L1 data reads and L2 reads, (2) Write Buffer emulating the bit flips corresponding to L1 data writes, and (3) Miss Unit emulating the bit flips corresponding to L2 writes.

5.1.2 DRAM Fault Injection

DRAM cells store data in capacitors that lose charge over time. In order to keep the data consistent, the DRAM cells have to be refreshed periodically. DRAM cells’ strength is non-uniform due to manufacturing variability, i.e., some DRAM cells lose charge faster than others. The number of bit-flips in DRAM increases as the refresh period increases due to a higher number of DRAM cells losing charge before they are refreshed. These bit-flips also depend on when the data was written into and read from the DRAM. Therefore, implementing a FI module for DRAM requires keeping track of the faulty DRAM cells for each refresh-rate knob and the hold times of the data in each DRAM cell. Given the
DRAM size, maintaining this information requires a lookup table of impractical size on an FPGA. The lookup table also introduces a considerable latency in DRAM reads/writes. To emulate DRAM errors, we implement a software-based FIT for DRAM. Initially, a map `DRAM_MAP` of faulty DRAM cells for the maximum refresh period (20 s) knob is generated randomly using a uniform distribution. The faulty DRAM cells for higher refresh rates are a subset of `DRAM_MAP`. The data being loaded into the DRAM is modified using the `DRAM_MAP` and the current refresh rate knob. The exact read and write accesses to the DRAM are not impacted.

### 5.2 User application and QoS metric

The AXES methodology is well suited for a large class of workloads that have a high intensity of memory operations (e.g., video processing, machine learning). Table 4 summarizes the applications used for AXES’ case study. (1) Canny edge detection [39] algorithm operates on a video streams and marks the edges in each frame. (2) k-means is a machine-learning application [40] which partitions 3 dimensional input points (RGB pixels) into 6 different clusters, and (3) blackscholes [40] is a finance analysis application which solves partial differential equations to perform price estimations.

The applications’ source code is modified to indicate which data elements are non-critical. Several techniques have been explored in the literature [41, 42] to systematically analyze and report how different parts of the application are affected by errors. Depending on the application, there are one or more candidate data segments (e.g., image data, video data, signal data) for accuracy/energy tradeoffs. We identify these segments in the source code, and replace `malloc()` calls to the kernel by `malloc_approx()` calls. For canny, the image buffer is marked as a non-critical section. For k-means, the data structure for the image buffer is modified to separate the non-critical pixel data, and raw pixel information is converted from float representation to unsigned char representation since each pixel value lies between 0 and 255. For blackscholes, the buffer data structure is left unmodified: the non-critical approximate memory consists of a buffer of floats. Thus, errors can impact the bits differently, and in case of extreme approximation may produce relative errors of 100%. The `malloc_approx()` calls are intercepted by a custom Linux Kernel Module, described in next section.

In addition to specifying the non-critical data elements, a quality-monitor specific to the application domain is required. The quality monitor is a lightweight software routine invoked to evaluate the application QoS and used to calculate the reward as described in Section 4.1.3. The QoS metric indicates the quality degradation caused by the configuration of approximation knobs. Typically, application developers generate a software routine that is capable of measuring the quality at runtime. In canny, the QoS is determined by evaluating the Root Mean Square Error (RMSE), which is the mean of pixel differences squared between an exact result and an approximate result. For k-means and blackscholes, the quality monitors are RMSE and Average Relative Error, used directly from AxBench [40]. This software routine is invoked during runtime, and the result of an exact run of the application is compared with an approximate version [43, 44]. The quality evaluation is not repeated for every input so that the benefits of approximation can justify the overhead. Depending on the status of learning, the frequency of quality evaluation should be adapted. A detailed overhead analysis is presented in Section 6.5. If additional cores are available, ground truth comparison can be performed in parallel. In our unicore setup, this incurs unavoidable overhead during the initial exploration phase.

### 5.3 Kernel Support for Approximation Knobs

We develop a Loadable Kernel Module (LKM) as middleware between the user application and CSRs. `malloc_approx()` calls from the applications are intercepted by the LKM, and using `mmap` a contiguous physical segment is allocated. The starting and ending address of the segment is written to additional CSRs. Whenever the user application loads/stores data, the MMU compares the memory address in hardware using these CSRs to check if it is in the non-critical segment.
5.4 Power Model

The evaluation platform does not come equipped with on-board power sensors. Thus, we use Sniper \[45\] simulations and McPAT \[46\], along with existing power models from literature \[8, 4\] for computing the power for different knob settings. Each new input to the application is simulated in Sniper, and McPAT is invoked to estimate the power and energy consumption of different system components. The power and energy are then scaled according to the technology models (described below) to estimate different knob configurations’ power values.

5.5 Error Model

**On-chip SRAM:** When scaling the supply voltage ($V_{DD}$) in SRAM cells, read and write errors are dominant; hence hold failures are not considered here. We use a model for a 6T SRAM for 65 nm node from \[8\] for comparison with related memory approximation work. The Bit Error Rate corresponding to relative power supply voltage is shown in Figure 7a.

**Off-chip DRAM:** We employ the power model proposed in Flikker \[4\]. We assume that the DRAM is partitioned into two sections: (1) 1/4 exact DRAM having a high refresh rate, and (2) 3/4 DRAM having a lower refresh rate based on the approximation knob. The corresponding power model is shown in Figure 7b.

6 Performance Evaluation

In this section, we demonstrate AXES’ ability to learn directly from raw experience, without requiring any model of the environment’s dynamics. These experiments are evaluated against canny.

6.1 Policy Initialization

First, we evaluate AXES ability to learn an optimal policy to minimize energy from scratch. We compare two TD reinforcement learning algorithms: TD($\lambda$) and Q-Learning. The primary difference between the methods is that TD($\lambda$) uses bootstrapping. For both algorithms, we determined the learning parameters empirically using a simulated workload (discussed in Section 4.2).

Without any QoS constraints, approximation knobs should be set to the configuration corresponding to the lowest power. The goal of a policy should be to reach the optimal configuration as quickly as possible. Figure 8 shows the comparison of the two methods, along with the optimal configuration corresponding to maximum energy savings. The plots are averaged over 16 runs to remove the effect of any outliers.

The x-axis in Figure 8 represents frames processed, and the y-axis represents average memory power (normalized to the exact execution) for each episode for canny edge detection application \[39\]. We make two major observations. First, both algorithms can eventually converge to the optimal policy. Second, in Figure 8a when the configuration space is small (i.e., we restrict the allowable knob settings), both Q-learning and TD($\lambda$) converge at an equal rate. However, when configuration space is increased (Figure 8b), TD($\lambda$) can improve its policy faster than Q-learning because it uses short-term memory in the form of eligibility traces. The traces are used to update multiple state-action pairs based on the reward obtained, instead of just one state-action pair in Q-learning at every step. We conclude that with growing complexity in configuration knobs, TD($\lambda$) is the better algorithm. Thus, for the rest of the experiments, we only use the TD($\lambda$) algorithm in AXES.
6.2 Self-optimization

To show that AXES is capable of self-optimizing the approximation knobs in the memory hierarchy within the QoS budget specified by the application, we study AXES’ behavior for unexperienced inputs. We expose an agent with an established policy to varying inputs and compare it to state-of-art approximation management policy DART [8]. DART is a design-time technique that uses a branch and bound algorithm to consider the worst-case effects of all possible approximation knob configurations for a memory hierarchy. We train DART on a set of scenes used during the policy initialization phase. The goal is to honor the QoS constraint specified by the application while maximizing energy-efficiency. In our case, this means keeping the RMSE below a specified value. For a QoS constraint of 10 RMSE DART statically sets the knobs as follows: \( L1 V_{DD} : 0.8 \text{ V} \), \( L2 V_{DD} : 0.8 \text{ V} \) and \( DRAM T_{REF} : 0.5 \text{ s} \). The energy/frame reported in all results is normalized with respect to the knob configuration of \( L1 V_{DD} : 1 \text{ V} \), \( L2 V_{DD} : 1 \text{ V} \) and \( DRAM T_{REF} : 0.1 \text{ s} \).

In Figure 9a, a QoS constraint of 28 (RMSE) has been specified by the user, which is marked with a black line. The key observations here are as follows: (1) Frame 32 is a key-frame where a scene change occurs. Neither of the tested policies has experienced this scene previously, and the scene requires a new configuration of knobs to remain to meet the QoS requirement. In frame 32, DART immediately violates the QoS constraint and continues to do so. AXES can take actions and reach a new configuration while remaining within the quality constraint. Initially, when AXES detects there is an overshoot, it penalizes the current action and takes action to reduce the QoS error. This leads to a conservative state, with more room for QoS relaxation. Then, AXES increases the degree of approximation. In the subsequent cycles AXES self-optimizes until it reaches a stable state. (2) Figure 9b shows the average power for each frame. There is no significant change in power with DART because it uses a fixed knob configuration at runtime. The normalized energy/frame required by AXES is 72.3\%, and normalized energy/frame required by DART is 70.8\%. (3) We define QoS overshoot as the area under curve for the regions of QoS violations during execution. For DART, QoS overshoot is 200 versus 50 for AXES. Thus, DART violates the QoS requirement 4\* more than AXES (Figure 9b). This means that AXES can reduce QoS violations by 75\% with <5\% additional energy. These experiments demonstrate that AXES is self-optimizing, i.e., can continuously learn configurations that meet the QoS constraint when exposed to unknown inputs.
6.3 Coordination

To show that AXES is capable of coordinating interdependent memory knobs, we study AXES’ behavior when exposed to varying quality constraints. The goal is to adapt to new targets specified by the user and reconfigure the knobs to save more energy while processing the frames. Figure 10 shows how AXES behaves in the scenario described. The key observations here are as follows: (1) Figure 10a shows measured QoS compared to the dynamic QoS constraint. Initially, the QoS constraint is 10. At frame 30, it is relaxed and updated to 85, thus exposing an opportunity to conserve energy. Again, at frame 60, the constraint is changed to 30. AXES can self-adapt to find new configuration knobs that meet the constraints each time they are changed. (2) Figure 10b shows the normalized power for each frame. Initially, when the QoS constraint is 10, the memory power is around 80 \%. When the QoS constraint is relaxed to 85 at frame 30, AXES can lower the memory energy consumption by finding a new configuration of knobs and keeps operating in that region until the constraint changes again. Overall, the normalized energy/frame required by AXES is 75.9 \%. Therefore we demonstrated that AXES is capable of (1) self-adapting to new quality constraints specified by applications through coordination, and (2) continuously converging on optimal configurations.
Figure 10: AXES self-adapting to user-specified quality constraints by coordination across the memory hierarchy.

Figure 11: Additional workloads.
6.4 Additional workloads

Figures 11a and 11c show AXES’ result for \texttt{kmeans} with a normalized energy/frame of 76.4\%. Figures 11b and 11d show AXES’ result for \texttt{blackscholes} with a normalized energy/frame of 70.9\%. We observe that even though the interdependent dynamics between all three layers of memory hierarchy and the achievable QoS/power are complex and application-dependent, AXES is able to meet the dynamic quality constraints by continuously finding new configurations corresponding to the new system goals.

6.5 AXES Overhead

All runtime approximation strategies suffer from two primary sources of overhead: (1) calculating the QoS value, and (2) runtime management. As mentioned in Section 5.2, to reap the benefits of approximation, AXES is not invoked for every input once the Q-values have been populated. In most cases, the quality monitor (e.g., the errors between pixels in canny edge detection) is embarrassingly parallel. If an additional core is available, the ground truth comparison can be performed in parallel. If AXES is invoked too frequently, the compute and energy overhead of the ground-truth comparison would not be justified. In Figure 12, we compare the QoS of k-means application at different intervals of invocation (marked with a blue tick). Whenever the system goals change, the subsequent five frames are always updated to adapt to the new setting. We observe that AXES can adjust to new goals with reduced invocation periods, at the risk of potentially missing self-optimization opportunities between invocations. Even ignoring regular invocation completely, AXES can be used in an event-driven manner (e.g., updated at design time when a new system is developed, at runtime when a new application is available for approximation, or when the goals (QoS constraints) change). State-of-the-art alternatives do not self-optimize for these situations for a full memory hierarchy.

In Figure 13, we compare the compute overhead and the energy savings of AXES for various invocation periods based on the number of frames. Based on these observations, we invoke AXES every five frames in all of our evaluations.

The overheads of the current version of AXES are not preventative for the presented architecture and execution scenario. However, the investigated architecture is uncore – in a many-core system, the proposed control structure will not scale well due to configuration complexity if a single agent is responsible for configuring the entire memory system.
Similarly, the current reward calculation is based on the quality reports of a single application utilizing the approximate memory segments – multiple QoS applications running concurrently sharing approximate segments will complicate the agent. We believe a hierarchical or multi-agent architecture would effectively tackle the challenges of more complex systems and are topics for future investigation.

![Figure 13: AXES overhead for different intervals](image)

### 7 Conclusion

In this paper, we address the challenge of designing a technology-agnostic runtime manager for approximate memory hierarchies. To this end, we propose AXES, the first self-optimizing model-free runtime manager for tuning approximation knobs in a unified multi-layer memory hierarchy to achieve acceptable QoS for diverse workloads while minimizing energy consumption. AXES uses temporal difference (TD) learning to learn directly from experience without a model of the environment’s dynamics. We develop an experimental case-study to evaluate AXES on a modified RISC-V processing core. We demonstrate the efficacy of AXES for configuration knobs when: (1) there is no quality constraint, and the system objective is to minimize power, (2) there is a quality constraint, and unknown inputs require reconfiguration of the knobs, and (3) the user dynamically changes the QoS constraints. AXES can automatically control approximate memory hierarchies regardless of memory technology or application. Due to these advantages, we believe that AXES has the potential for developing extremely energy-efficient systems across memory devices, parameters, and technologies.

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