A context-aware gate set tomography characterization of superconducting qubits

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The efficiency of Quantum Characterisation, Verification, and Validation (QCVV) protocols highly hinges on the agreement between the assumed noise model and the underlying error mechanisms. As a matter of fact, errors in Quantum Processing Units (QPUs) incorporate various aspects of context-dependability which are overlooked by the majority of the commonly used QCVV protocols. As QCVV protocols are indispensable when it comes to characterizing and evaluating quantum operations, there is a serious need for a detailed characterization taking into account such aspects. In this work, we address these shortcomings by designing a context-aware version of the gate set tomography (GST) protocol. Our experiment selection approach is based on a polynomial quantification of the accumulation of errors within the designed circuits. Using simulated QPUs, we show that this technique enables a characterization with an inaccuracy reaching $10^{-5}$. Furthermore, we use our proposed protocol to experimentally infer context-dependent errors, namely crosstalk and memory effects, in a publicly accessible cloud-based superconducting qubits platform. Our results show that when the GST is upgraded to include such features of context-awareness, a large coherence in the errors is observed. These findings open up possibilities of drastically reducing the errors within the currently demonstrated QPUs.

I. INTRODUCTION

A quantum state is by essence destructed when measured \cite{1}. Therefore, real-time monitoring of the computational states of QPUs while preserving their quantum aspect is generally unlikely. In combination with being subject to numerous noise mechanisms, this fact implies that the creation of quantum states and the different operations applied to them can only be evaluated indirectly. In quantum computing, these practices are commonly known as QCVV protocols. They consist of sampling sequences of operations and converting the observed measurements into meaningful parameters. Designing efficient QCVV protocols is a major challenge in this field, as they are vital for understanding noise mechanisms \cite{2, 3}, calibrating control signals \cite{4, 5}, developing noise-aware compilers \cite{6}, and providing realistic noise models for simulation backends \cite{7}.

There exist a wide range of QCVV protocols designed for targeting a variety of noise mechanisms \cite{8, 9, 20, 21}. These protocols exhibit an interplay between the number of extracted parameters, the expected accuracy, the number of the measured sequences, and the awareness of systematic errors. For instance, Randomized Benchmarking (RB) protocol is used to infer the depolarizing rate of quantum gates \cite{17}. This protocol owes its high accuracy to its output corresponding to a single parameter (the error rate) and its awareness to State Preparation And Measurement (SPAM) errors. Other examples are quantum state tomography \cite{11, 12, 26} and quantum process tomography \cite{14, 15}. They are used to respectively infer quantum states and quantum operations. These protocols provide a more detailed characterization as their outputs are density matrices and quantum channels. However, unless properly addressed \cite{20, 21}, their standard forms have moderate accuracy, as they are oblivious to systematic errors and based on sampling a relatively small number of sequences. As an alternative, the Gate Set Tomography (GST) protocol provides a more accurate and detailed characterization since it takes into account and evaluates SPAM errors and relies on sampling a larger number of sequences \cite{22, 25}. Although the requirement of measuring a large number of sequences comes with a high time complex-
ity (fridge time), it was demonstrated that involving the GST protocol in the calibration routines leads to a considerable reduction in the underlying operational errors \cite{22, 23}. In other works, data delivered by measuring the GST sequences were used to infer deliberately engineered temporally correlated noise processes \cite{27} and context-dependent errors \cite{28, 30}. However, the state of the art suffers from the lack of GST protocols adapted to capturing sophisticated forms of errors, namely crosstalk in large arrays of qubits (beyond three qubits) and memory effects. These noise mechanisms were not captured by the original GST protocol.

To characterize crosstalk errors in a set of qubits; how a given operation on a target qubit is affected given the operations simultaneously applied to the neighboring qubits, one can conceive two approaches involving the context agnostic GST. The first one is to perform a multiqubit GST on the whole set then trace out the neighboring qubits. This approach is impractical as the operators describing multiqubit gates are massive for sets containing more than 2 qubits. The second alternative is to perform multiple rounds of single-qubit GST on the target qubit. In each round, the target gates are accompanied by a different configuration of gates on the neighboring qubit which enables inferring crosstalk. In this paper, we introduce a context-aware version of the GST protocol. It systematically takes into account spatial correlations which allows inferring the target operations in a multiplicity of scenarios within a single round. Therefore, it reduces considerably the time complexity that comes with the requirement of running multiple rounds of the latter approach while it tackles the impracticality of the first one. Additionally, it also takes into account spatial correlations which allows characterizing memory effects. Therefore, the proposed protocol is a step towards enabling a rigorous assessment of the erroneous behavior of QPUs. In short, the main contributions of this paper are:

- The development and the validation of a new version of the GST protocol based on the refinement of the sequence selection algorithm, allowing a high error characterization accuracy.
- The differentiation of the proposed version by introducing the context-awareness, enabling the characterization of crosstalk errors and memory effects.
- The demonstration of the protocol on Quantum-Inspire’s Starmon-5 chip \cite{31}; the results reveal a relevant context-dependency in the error mechanisms affecting this chip with considerably large reversible parts.

Suppose one possesses a QPU offering the possibility to run a target gate set composed of state preparation, a set of gates $\{G_1, G_2, \ldots, G_n\}$, and a measurement. We assume these operations are governed by a noise mechanism such that each one of these operations corresponds to a well-known operator/superoperator; i.e., state preparation, ith-quantum gate and the measurement respectively corresponds to a state $|\rho_i\rangle\rangle$, a quantum channel $\hat{G}_i$ and a measurement operator $\langle\langle M_0\rangle\rangle$. Therefore, as we know these operators, we can compute the expectation values of any circuit built as a combination with repetition of elements of this gate set. For instance, the measurement applied to a circuit defined by state preparation, a multiqubit GST on the whole set then trace out the measurement applied to a circuit defined by state preparation, ith-quantum gate and the measurement respecting the order of the sequence selection algorithm, allowing a high error characterization accuracy.

$$E_e = \langle\langle M_1 \rangle\rangle \hat{G}_S \hat{G}_S \hat{G}_S \cdots \langle\langle \rho_i \rangle\rangle$$

(1)

Let’s put ourselves in the inverse case where $|\rho_i\rangle\rangle$, $\hat{G}_i$ and $\langle\langle M_0\rangle\rangle$ are unknown and we are given the possibility of sampling a set of $N$ circuits $\{c_1, c_2, \ldots, c_N\}$ with corresponding sequences $\{S^1, S^2, \ldots, S^n\}$ where $S^1 \in \{1, 2, \ldots, n\}^l$. The claim of the GST protocol is that the operators $|\rho_i\rangle\rangle$, $\hat{G}_i$ and $\langle\langle M_0\rangle\rangle$ can be estimated based on the observed measurements \cite{23, 24}. In other words, if the measurement of the circuits on the target QPU generated measurements $\{\hat{E}_{c_1}, \hat{E}_{c_2}, \ldots, \hat{E}_{c_N}\}$, the gate set $|\rho_i\rangle\rangle$, $\hat{G}_i$ and $\langle\langle M_0\rangle\rangle$ is inferred by constructing a set of operations generating similar measurements values. This reconstruction is equivalent to the following optimization problem:

Given: a set of circuits $\{C_i\}$ and the corresponding average of observed measurements $\langle E_i \rangle$ on target QPU: minimize the following L1 loss function:

$$fitness = \sum_i \left| \langle\langle E^{C_i} \rangle\rangle \hat{G}_S \hat{G}_S \hat{G}_S \cdots \langle\langle \rho^{C_i} \rangle\rangle - E_i \right|$$

(2)

where $|\cdot|$ refers to the absolute value. This optimization is identified as a Total Variation Diminishing (TVD) problem whom the freedom degrees are the nontrivial elements of the operators describing the gate set. The fact that the gates are quantum maps together with the Hermiticity and the unit trace of density matrices and measurement operators imply the following linear constraints on their entries:

$$\sqrt{2} \leq p_i, E_i \leq \sqrt{2} \quad \forall \ i, j \in \{1, 2, 3, 4\}$$

(3)

$-1 \leq G_{i,j} \leq 1$

The starting point in our optimizations is the operators corresponding to the perfect target operations (no errors). As there is gauge freedom in these operators \cite{32}, one should ensure that the estimations are close to the perfect operations. Therefore, we intuitively tighten these linear constraints around the perfect operation with a marge of $\pm 0.1$ for gates and $\pm 0.2$ for SPAM operators, and hence, given the perfect operations $\rho^p, E^p$, and $G^p$, these constraints become:

$$\max(p_i^p, p_j^p - 0.2) \leq p_i \leq \min(p_i^p, p_i^p + 0.2)$$

(4)

$$\max(E_i^p, E_j^p - 0.2) \leq E_i \leq \min(E_i^p, E_i^p + 0.2)$$

$$\max(G_{i,j}^p, G_{i,j}^p - 0.1) \leq G_{i,j} \leq \min(G_{i,j}, G_{i,j} + 0.1)$$
Furthermore, the GST relies on sampling a large number of circuit sequences to provide an accurate characterization of the operations within a target QPU. However, sampling any set of circuits sequence does not ensure an accurate characterization. In fact, gate errors can either add up or cancel out. The latter case leads to the insensitivity of the observed measurement to error parameters, and hence, alters the accuracy of the protocol. Therefore, as displayed in Figure 1, the first step of the GST protocol, introduced in the supplementary material, is to design a set of sequences that guarantees the full imaging of the core sequences and the amplification of the manifestations of the targeted errors as these sequences’ length increases. The second step consists of running multiple shots of the circuits designed in step 1 on the target QPU and collecting the observed measurements. Finally, the third step, as we just described in this section, is to estimate the operators describing the gate set using the observed measurements in step 2.

In the next sections, We describe the adaptation of this protocol: i.e. the introduction of context-awareness, to infer temporal and spatial correlation in superconducting qubits and report our findings. Note that we consider it convenient to focus on errors affecting idling gates. This convenience comes from the fact that the impact of the investigated noise mechanisms is better observed/understood when affecting idling errors. Also, the accuracy of the GST protocol characterization of idling gates is very high compared to operational errors. The latter is altered by the gauge equivalence of quantum channels [52] and remain a challenge that we don’t address in depth in this work.

A quantum operation on a set of qubits may induce errors to operations simultaneously applied to neighboring qubits via crosstalk effects. In current superconducting qubits, crosstalk is prominent when C-phase gates are in play [19]. If we look at the geometry of a Starmon-5 chip in Figure 2, we see that qubit Q1 is physically connected to Q2. Also, when a single qubit gate is applied to Q1, Q2 can undergo three different C-phases with Q0, Q3, or Q4. The goal of this subsection is to use the GST protocol to characterize the impact of these C-phases on the operations simultaneously applied to Q1. To do so, we assume that depending on the operations applied to the rest of the qubits of the chip, a quantum gate, say an idling gate $I$, can be described by multiple superoperators $G_{I\{S\}}$. Each superoperator is specific to a context $S_i \in S$.
that is defined by the operations applied to the rest of the qubits of the chips. We include contexts $S_1$, $S_2$, $S_3$ that corresponds respectively to Q2 undergoing C-phases with Q0, Q3, and Q4 (while the two qubits left are idling) and a reference context $S_4$ where all the qubits are idling. Furthermore, to achieve informational completeness, we enable the possibility of including ancillary $R_x$ and $R_y$ rotations on Q1 in the context $S_3$ in our circuits. However, as our main goal is to infer idling gates, these ancillary operations’ corresponding error generators are discarded from matrix $B$ in the germs selection algorithm. Using the genetic algorithm from the MatLab optimization toolbox, the latter provides the following set of germs:

$$g_{ct} = \{I^1, I^2, I^3, I^4 R_x^1, I^3 I^1, I^3 I^4, I^1 I^1 I^4 I^2, I^1 I^4 I^3 I^4, I^2 R_y^1, R_y^1 I^1 R_y^1 I^1 R_y^1, R_y^1 R_y^1 R_y^1 R_y^1, I^2 I^2 I^3 I^3, I^1 R_y^1 I^2 I^2 I^3 I^3, I^1 R_y^1 I^2 I^2 I^3 I^3\}$$

(5)

Note that the upper index $i$ refers to the context. For instance, $I^{1,2,3}$ respectively describe the idling operations on Q1 that is accompanied by Cphases on Q2 together with respectively Q0, Q3, Q4 while the rest of the qubits is idling. Therefore, each of these operations are captured by running 5-qubits gates. Since C-phases in the Starmon-5 are implemented within three times the duration of single-qubit gates, to every single-qubit gate is appended an idling time to ensure the parallelism within the elements of the gate set. Our characterization yields the following Pauli superoperators:

$$G(I|S_1) = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0.0000 & 0.9891 & -0.0079 & 0.0007 \\ -0.0001 & 0.0084 & 0.9900 & -0.0010 \\ 0.0041 & 0.0022 & -0.0000 & 0.9959 \end{pmatrix}$$

(6)

$$G(I|S_2) = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0.010 & 0.9886 & -0.0142 & 0.0033 \\ -0.0001 & 0.0152 & 0.9881 & -0.0024 \\ 0.0051 & 0.0028 & 0.0015 & 0.9950 \end{pmatrix}$$

(7)

$$G(I|S_3) = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0.006 & 0.9910 & -0.0155 & -0.0010 \\ -0.0006 & 0.0164 & 0.9914 & -0.0019 \\ 0.0043 & 0.0029 & 0.0007 & 0.9962 \end{pmatrix}$$

(8)

$$G(I|S_4) = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0.0005 & 0.9969 & -0.0050 & -0.0004 \\ 0.0002 & -0.0036 & 0.9970 & 0.0007 \\ 0.0030 & 0.0005 & 0.0008 & 0.9964 \end{pmatrix}$$

(9)

These operators’ respective diamond distances to the target perfect operators (no errors) $\|G(I|S_i) - I_{\text{perfect}}\|_\diamond$ are 0.0160, 0.0218, 0.0210, and 0.0083. The diamond distance is computed using QETLAB [28] and The CVXPY-package [29, 40]. Furthermore, this characterization allows us to study more features of this noise mechanism. For instance, due to the apparent anti-symmetry of the unitil block with respect to the diagonal, we see a clear resemblance of these matrices to elements of the $SO(3)$ (the group of 3D-rotations). An idling gate that displays such a feature of noise would imply that this form of noise is coherent, and hence, avoidable by inversion. To address this hypothesis, we seek for each operation $G(I|S_i)$ an unitary operator $U$ that minimises $D_i = \|U \ast G(I|S_i) - I_{\text{perfect}}\|_\diamond$. Finding $U_i$ is an optimization problem in which the freedom degrees are the 3 angles that specify $U$. By solving these problems using the SQP algorithm from the Matlab optimization toolbox, we find that for scenarios 1, 2, and 3 it drops to 0.0134, 0.0148, and 0.0119, while there is no apparent improvement in context 4 i.e. 0.0083.

### III. MEMORY EFFECTS

In this section, we address the situation where gate errors are accompanied by an error mechanism that lasts slightly longer than the implementation time of the gates themselves. In this case, we say that the environment has a first-order memory i.e., it alters the current gate differently depending on the previous operation. Therefore, we suppose that each gate is described by multiple superoperators. Each of these superoperators corresponds to a different context that is defined by the previous operation. Suppose we are targeting a gate set composed of an $R_x$, an $R_y$, and an idling gate, $I$. If such memory effects are displayed, each one of these gates has three corresponding superoperators. see Table I

| previous | current | $R_x$ | $R_y$ | $I$ |
|----------|---------|------|------|-----|
| $R_x$    | $G_1$   | $G_4$| $G_7$|
| $R_y$    | $G_2$   | $G_5$| $G_8$|
| $I$      | $G_3$   | $G_6$| $G_9$|

TABLE I. Superoperators representing the applied (current) gates with respect to the previously applied gates

This configuration leads to constraints on the possible circuits. In fact, in order to be valid, a sequence $S = \{1,2,3\}$ should satisfy:

$$S_i \in \{\{1,4,7\}; S_{i-1} \in \{1,2,3\}\} \quad \forall \ (1 < i \leq l) \quad (10)$$

These constraints are injected into the germs selection algorithm and the sequences are built accordingly. As we are inferring how memory effects are affecting idling gates, the six gates $G_1$ to $G_6$ are introduced as ancillary gates, and the errors in $G_7$, $G_8$, and $G_9$ are targeted by our germs selection algorithm. Using the genetic algorithm from the MatLab’s optimization toolbox, our
germs selection algorithm provides the following set:

\[
g_{\text{mem}} = \{ I^1 R_x^1, I^2 R_y^1, I^3 I^1, I^2 R_y^3 I^1 R_x^1, I^1 R_x^3 I^2 R_y^1,
R_y^1 I^1 R_x^1 I^1, R_y^2 R_y^3 R_y^1 I^1, I^2 R_y^3 I^1 R_x^2 I^2 R_y^1,
I^3 R_y^1 R_y^1 I^1 R_x^3 I^1, R_y^2 R_y^3 I^1 I^3 I^1 R_x^1,
R_y^1 I^3 I^2 R_y^3 I^1 I^1 R_x^1 \}\]

(11)

FIG. 3. Quantum circuit corresponding to the sequence (3, 7, 6, 8, 3, 7) where the blue, brown, yellow, and red gates respectively correspond to \(R_x^3, I^1, R_y^3, \) and \(I^3\). This sequence is an example generated by the first preparation fiducial \(\varnothing\), the unprepared \((l=1)\) fourth germ \(I^2 R_y^3 I^1 R_x^1\) \((l=3)\) as an idling gate is included in every state preparation), and the second measurement fiducial \(I^1 R_x^3\). Note that this fiducial’s first gate is in the third context as the last gate of the germ is an idling gate.

where \(f\) is defined by the fiducial sequence’s last gate. We also merge every state initialization with a consecutive idling gate to ensure that the context of the first gate is always 3 (preceded by an idling gate). We also include another idling gate before the final measurement so that the latter is operated only in the 3\(^{rd}\) context (the measurement is not merged with the idling gate). Figure 3 displays a circuit example. We run this designed sequence on qubit Q1 of a Starmon-5. The estimated superoperators of the three idling gates are:

\[
G(I|S_1) = \begin{pmatrix}
1 & 0 & 0 & 0 \\
0.0025 & 0.9987 & -0.0082 & -0.0105 \\
0.0047 & 0.0092 & 0.9971 & 0.0009 \\
-0.0019 & 0.0118 & 0.0062 & 0.9975
\end{pmatrix}
\]

(12)

\[
G(I|S_2) = \begin{pmatrix}
1 & 0 & 0 & 0 \\
0.0074 & 0.9973 & -0.0126 & -0.0071 \\
0.0029 & -0.0160 & 0.9994 & -0.0040 \\
-0.0066 & -0.0022 & 0.0012 & 0.9992
\end{pmatrix}
\]

(13)

\[
G(I|S_3) = \begin{pmatrix}
1 & 0 & 0 & 0 \\
-0.0001 & 0.9971 & -0.0034 & 0.0005 \\
-0.0000 & 0.0040 & 0.9966 & 0.0000 \\
0.0013 & 0.0001 & -0.0005 & 0.9987
\end{pmatrix}
\]

(14)

where \(G(I|S_i)\) corresponds to the idling operator injected at the context \(S_i\) that is defined by the previous gate \(S_1, S_2, \) and \(S_3\) refers to operations preceded by respectively \(R_x, R_y, \) and \(I\). These gates’ diamond distances to the ideal gates \(\|G_i - I\|_d\) are 0.0186, 0.0265 and 0.0057. Seeking and injecting unitaries \(U_i\) that minimise the distances \(\|U_i G_i - I\|_d\) allows to respectively reduce them to 0.0156, 0.0174 and 0.0057.

IV. DISCUSSION AND OUTLOOK

This paper introduces a context-aware version of the GST protocol, i.e., it has the ability to distinguish operations with respect to their context. This adaptation leads to a sharp characterization of errors when they incorporate such context dependencies. To do so, we described the core of our version that consists of a polynomial evaluation of the quality of the circuit sequences. As these evaluation functions admit a polynomial representation, they are computed efficiently. In fact, the fitness function of the germs selection algorithms used in this work take no more than \(\sim 20\) sec in a single core of a cluster node with \(2 \times 2683\) v3 CPUs (\(\sim 2.00\)GHz = 28 cores / 56 threads) and \(24 \times 16GB\) DDR4 = 384GB memory. Furthermore, we evaluate the accuracy of our estimations by using simulated QPUs that fit the assumed model. This evaluation shows that our estimation is two orders of magnitude more accurate than the gate themselves. Moreover, we adapt the GST protocol to take into account and infer spatial correlations; i.e., crosstalk errors. The implementation of the designed protocol on the Starmon-5 chip shows that when a C-phase is applied to neighboring qubits, errors are induced to the studied qubits via crosstalk. Fortunately, a large fraction of these errors is reversible. For instance, \(1 - 0.0119/0.0210 \sim 43\%\) of the errors in Q1’s idling when a C-phase is applied to qubits Q2 and Q4 are coherent. This offers the opportunity of drastically mitigating the errors that are purely due to crosstalk; i.e., in this example a reduction reaching a factor of \((0.0210-0.0087)/(0.0119-0.0087) \sim 4\) is predicted. Next, we addressed the problem of temporal correlation, namely memory effects. This study explicitly shows that when an idling gate is applied after a rotation gate, errors due to memory effects are induced. However, up to 32\% of these errors is reversible which constitutes a reduction of the errors purely due to memory effects by a factor of \(\sim 2\). Note that measuring the sequences for these characterizations (designed for a maximal repetition index 6) took respectively 30 and 24 hours for the crosstalk and memory effects experiments.

To conclude, this work takes a step further the agreement between the assumed noise model by GST protocol and real-life error mechanisms. However, the efficiency of the hereby proposed Context-Aware GST (CA-GST) protocol is altered by sampling errors and the presence of errors mechanisms that reside beyond the assumed models. Nevertheless, due to their hereby demonstrated coherent aspect, this work promises a large reduction in some of the most prominent error mechanisms in this era.

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S-I. CIRCUITS LAYOUT

The GST protocol is based on sampling a predetermined set of circuits. These circuits are tailored with the aspiration of triggering and observing errors within a gate set. A gate set is composed of a set of state preparations, a set of gates, and a set of measurements. To enable the reconstruction of the underlying operations, the sets of state preparations and measurements are required to satisfy Informationally Completeness (IC); i.e., a set of $2^{2n_q}$ ($n_q$ being the number of qubits) operators spanning the space of linear operators that act on the $2^n_q$ dimensional Hilbert space \[ [10, 11] \]. However, most of the qubit technologies, including the one that we are targeting in this work, inherently allow the preparation of the ground state and the measurement on the computational basis (whether or not in the excited state). Therefore, as illustrated in Figure S1 in lieu of applying gate sequences (germs) to an IC set of prepared states and measuring in IC set of measurement bases, each circuit is commenced by a state preparation in the ground state followed by a preparation fiducial (a gate sequence with length $\leq 3$) and terminated by a measurement fiducial followed by a measurement in the computational basis. Injecting the right set of preparation and measurement fiducials is equivalent to the preparation and the measurement in an IC set of states and measurements. Furthermore, the germs should guarantee an all-inclusive manifestation of the target error mechanisms within the gate set elements and this manifestation is expected to come with a higher amplitude as the length of germs grows. In the following, we introduce our selection algorithms allowing us to design efficient fiducial and germ sequences.

FIG. S1. GST sequences composition. Each sequence is composed of a state preparation in the ground state followed by germs “sandwiched” by a set of preparation and measurement fiducials followed a measurement in the computational basis at the end.

S-II. FIDUCIALS SELECTION

In the density matrix and quantum channels formalism, the expectation values of the measurement in a circuit having the form displayed in Figure S1 can be expressed as:

$$ E = \langle\langle M|| f_m G f_p ||\rho_0\rangle\rangle $$

(S1)

Where $||\rho_0\rangle\rangle$ corresponds to the density matrix of the prepared state, $f_p$ is the preparation fiducial’s superoperator, $G$ is the superoperator representing the sequence of $2^l$ germs, $f_m$ is the measurement fiducial’s superoperator and $\langle\langle M||$ is the measurement operator. The intuition behind the introduction of the preparation and the measurement fiducials is to maximize the sensitivity of the observed measurements to every nontrivial entry of the superoperator $G$. By looking at Equation 1, we see that $E$ is a first degree polynomial of these entries and therefore:

$$ E = \sum_{i,j=1}^{i,j=4} a_{i,j} G_{i,j} + a_0 $$

(S2)

Therefore, the ability to sense the elements of the superoperator $G$ in the measurement observed using a set of k preparation and k measurement fiducials are represented in the following vector:

$$ T = \text{vec}t\left( \sum_{p,m=1}^{k} |a_{p,m}^{i,j}| \right) $$

(S3)
where the upper index refers to the circuit defined by a preparation fiducial $p$ and a measurement fiducial $m$. Our fiducial selection algorithm is the following optimization problem:

given a set of all possible fiducials, maximize:

$$ fitness = \text{sum}(T)/\text{var}(T) \quad (S4) $$

The freedom degrees of this optimization problem are the combinations of at most three elements of the gate defining each element of the set of fiducials. To ensure designing informationally over-complete sets of fiducial for single-qubit cases, 6 different fiducials are injected in both sides (preparation and measurement). Note that, especially when considering a smaller set of fiducials, one should make sure that all the elements of $T$ are nonvanishing.

\section{S-III. Germs Selection}

Tailoring a set of circuits that ensures the manifestation of the errors within the gate set is key in the GST protocol. To address this problem, we assume that each gate $G_i$ in the gate set is expressed as its corresponding perfect gate $G_i^0$ preceded by an erroneous part expressed in the exponential form. This separation is expressed in the matrix multiplication form as:

$$ G_i = G_i^0 e^{\mathcal{L}_i} \quad (S5) $$

These error generators $\mathcal{L}_i$ vanish for perfect gates and get larger absolute values when the gate is noisier. Therefore, for gates within the moderate accuracy range, the previous equation admits the following Taylor expansion:

$$ G_i \approx G_i^0 (I + \mathcal{L}_i + \Theta(\mathcal{L}_i)) \quad (S6) $$

$I$ being the identity operator. The manifestation of errors in the observed measurements is related to the dependency of the measurements on the components of these error generators. In fact, since germ $G$ and fiducials $f_m$ and $f_p$ in Equation 1 are built as combinations of gates within gate set $\{||\rho_o||, G_1, ..., G_n, \langle\langle M||\rangle\}$, the expectation value $E_c$ is a polynomial with respect to the components of the error generators $\mathcal{L}_i$ that characterise each gate $G_i$ in the gate set. Storing and processing such polynomials is expensive especially for long depth circuits. Therefore, we track the manifestation of the entry of indices $(j,k)$ of the error generator $\mathcal{L}_i$ (i.e., $(\mathcal{L}_i(j,k)$) in measurement $E^c$ in a circuit $c$ using the simplified quantity

$$ E^c|_{\mathcal{L}_i(b,c)=0} = a_{0,i,j,k} + a_{1,i,j,k}x + \Theta(S7) $$

We see that variable $a_{c,i,j,k}$ represents the magnitude of the impact on measurement $E^c$ by entry $(j,k)$ of the error generator $\mathcal{L}_i$ characterizing the gate element $G_i$. Therefore, for a set of $N$ circuit, we track the impact of the ensemble of the error generators’ entries on the outcome of the measurement using the following vector

$$ A = \text{vec}(\sum_c |a_{c,i,j,k}|) \quad (S8) $$

In other words, each entry in $A$ represents a single entry of the error generator of one of the gates. For each $n$-qubit gate in the gate set, the size of $A$ is increased by $4^n(4^n - 1)$ (which is the number of nontrivial elements in the errors generator). Note that each circuit’s index $c$ is defined by the indices of the SPAM fiducials $p$ and $m$, the germ index $g$, and the repetition index $l$. The repetition of the germs is introduced as the GST protocol is based on sampling a large set of circuits on which an exhaustive search is impractical. However, this simplification reduces the search space of all possible sequences for such a large set of circuits. Fortunately, in the GST protocol is considered a small subset of circuits with a short depth called germs, and, as illustrated by Figure S1, large circuits are built by repeating the germs such that $G^l = G^{l-1}G^{l-1}$. Furthermore, to ensure that the manifestation of the errors is amplified as the $l$ increases, we store each length $l$ in a distinct column in a matrix $B$.

$$ B^l = \text{vec}(\sum_{p,m,g} |a_{1,i,j,k}|) \quad (S9) $$

The matrix $B$ is a juxtaposition of vectors $B^l$ ($1 \leq l \leq L$). In each entry of these vectors is accumulated the amplitude of the polynomial factors in the ensemble of circuits with repetition index $l$ of the entry $(i,j)$ of a gate $k$. Our germs selection algorithm is the following:

given the set of all possible germs, maximize:

$$ fitness = \text{Min}(B^l). \quad (S10) $$

Where $\text{Min}(B^l)$ refers to the smallest value of the vector accumulating the entries of the error generators within circuits with maximal repetition index $L$. The freedom degrees are the combination that defines the set of germs. The fact that the errors should be amplified as $l$ increases is introduced as the following constraint:

$$ B^l_i < B^{l+1}_i \quad (S11) $$

$$ \forall \ 1 \leq l \leq L - 1 , \ 1 \leq i \leq \sum_{k=1} ||G_k|| 4^{nk}(4^{nk} - 1) $$

with $n_k$ being the number of qubits on which the gate $G_k$ acts and $||G_k||$ the number of gates in the gate set. Therefore, maximizing the fitness function enables obtaining circuits with a large accumulation of errors. Furthermore, the constraints ensure the growth of the this accumulation with the repetition index $l$. 

S-IV. ACCURACY EVALUATION

To evaluate the accuracy of our circuit sequence selection algorithms, we compare our protocol’s accuracy with its commonly known counterpart [10]. As the latter was designed to perform the standard GST (agnostic to context-dependent errors), our benchmarks will be restricted on comparing the ability to infer static errors. The target devices of our proposed experiments are a set of simulated QPUs with various known error generators. Due to our knowledge of the operators describing the simulated operations, it is possible to compare the output of both protocols with respect to these operators.

In these experiments, we consider gate sets composed of a state preparation in the ground state, two rotation gates $R_x$ and $R_y$ of an angle $\pi/2$ around the axes $X$ and $Y$, an idling gate $I$, and measurements in the computational basis. This particular gate set was targeted using the reference protocol where the selected circuits were described by the following sequence [10]:

$$f_{ref} = \{ \emptyset, R_z, R_y, R_y R_x, R_x R_z R_x, R_y R_y R_y \}$$

S12

$$g_{ref} = \{ R_x, R_y, I, R_z R_y, R_x R_y I, R_x I R_y, R_y R_y, R_x R_z R_x R_y R_y \}$$

S13

where $f_{ref}$ and $g_{ref}$ respectively correspond to germs and fiducial sequences, $\emptyset$ the empty element (no gate). The repetition (duplicating the germ as in Fig S1) in the reference protocol is done until the germ sequences reach 256 gates. We introduce the same gate set in our circuit sequence algorithms without targeting any context dependency and the germs selection algorithm yield the following set of germs.

$$g = \{ R_z, R_y, I, R_y R_x, R_y R_y, R_y R_x I, I R_y R_x, I R_y R_y R_x R_y \}$$

S14

To ensure having approximately the same number of sequences with the reference protocol, this set of germs is designed for a maximal repetition index of 7. We also design a set of germs $g^6$ that is designed for a maximal repetition index of 6 with longer initial sizes of germs which is closer to the cases we address in the main text. The obtained $G^6$ is the following:

$$g^6 = \{ I I, I R_x, I R_y, R_y I R_y R_x, I R_x R_y R_y, I R_x R_y R_x, R_y R_y I R_y, I R_x R_y, I R_x I R_y, I R_x R_y I R_x I R_y, I R_y R_y I R_x I R_y \}$$

S15

These optimization problems were solved using the genetic algorithm from MatLab’s optimization toolbox with 10 stall generations. We use set $f_{ref}$ as it maximizes our fiducial sequences selection algorithm’s fitness function.

In our comparison, we use the three sets of sequences to characterize sets of simulated QPUs with gates $G_{I}, G_{X90}$ and $G_{Y90}$ incorporating random errors yet with fixed fidelities. Assuming that our protocol produces $\tilde{G}_I, \tilde{G}_{X90}$ and $\tilde{G}_{Y90}$, and the estimation using the reference circuits produces $G_{I}^{ref}, G_{X90}^{ref}$ and $G_{Y90}^{ref}$. We compare the quality of the sequence selection algorithms with the reference by comparing the distinguishability between $\tilde{G}_I$ and $G_I$ and between $G_{I}^{ref}$ and $G_I$. The same approach is applied to evaluate $G^6$ (the superoperator obtained using $g^6$). Figure S2 displays these measures with respect to the diamond norm.

FIG. S2. Achieved accuracy in characterizing idling errors using our protocol and the reference protocol. The blue, red, and yellow lines represent the averaged discrepancy between and 100 randomly generated target gate sets $G_t$ and their GST estimations using the gate sets $g$, $g^6$ and $g_{ref}$. The violet line represents the averaged distance between the $g_t$ and the perfect idling gate. The distances are measured with respect to the diamond norm. Note that in our simulations, a QPU is defined by a gate set. Within this gate set, SPAM operators are defined by a density matrix and a measurement operator having fidelities within a reasonable range. Furthermore, each gate $G$ is generated as a convex sum of 99.9% portion of its corresponding perfect gate (no errors) $G^p$ and another noisy 0.1% portion generated as a random channel. As proposed in [7], the fidelity of these gates is controlled by linearly tuning their error generator $L$ defined by $G = G^p e^L$. In this figure, each data point corresponds to an averaging over a 100 distinct gate set.

In Figure S2 we see that the use of our sequence selection derived circuits leads to a similar accuracy (blue and orange lines) when using the standard circuits (yellow lines). For idling errors, this characterization is highly reliable as its inaccuracy represents 3% of the inaccuracy of the inferred operations themselves (purple lines).