Passivation of SiC device surfaces by aluminum oxide

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Abstract. A steady improvement in material quality and process technology has made electronic silicon carbide devices commercially available. Both rectifying and switched devices can today be purchased from several vendors. This successful SiC development over the last 25 years can also be utilized for other types of devices, such as light emitting and photovoltaic devices, however, there are still critical problems related to material properties and reliability that need to be addressed. This contribution will focus on surface passivation of SiC devices. This issue is of utmost importance for further development of SiC MOSFETs, which so far has been limited by reliability and low charge carrier surface mobilities. Also bipolar devices, such as BJTs, LEDs, or PV devices will benefit from more efficient and reliable surface passivation techniques in order to maintain long charge carrier lifetimes. Silicon carbide material enables the devices to operate at higher electric fields, higher temperatures and in more radiation dense applications than silicon devices. To be able to utilize the full potential of the SiC material, it is therefore necessary to develop passivation layers that can sustain these more demanding operation conditions. In this presentation it will also be shown that passivation layers of Al2O3 deposited by atomic layer deposition have shown superior radiation hardness properties compared to traditional SiO2-based passivation layers.

1. Introduction
Reliability and long-term stability are coming more into focus, as silicon carbide devices are being introduced on the market. Typical reliability issues concern passivation and packaging of semiconductor device structures and in this contribution we will discuss problems related to the passivation layers and the processing of such layers. Important physical properties of a passivating layer on a semiconductor are large dielectric constant, large bandgap and sufficient band offsets between the valence and conduction band edges between the passivating dielectric layer and the semiconductor. A high thermal conductivity and a thermal expansion coefficient of similar magnitude as that of the semiconductor are also desirable. Apart from these properties of the layer itself, it is critical to select a deposition technique and surface pre-treatment that can enhance the overall reliability and electric field durability of the system. Very important for surface passivation is that the interface and near interface regions between the dielectric and the semiconductor contains a low and thermally stable concentration of electronic defects. The presence of such surface defects alters the surface potential, decrease the mobility and increase the recombination of charge carriers, leading to an overall degradation of device performance, both for uni- and bipolar electronic devices, and also optoelectronic devices. Since ideal, defect free, interfaces does not exist in reality, the technology must
aim at minimizing the amount of defects and, maybe even more important, ensure that the defects does not change over time due to thermal stress, electric fields, radiation, or other ambient conditions. Finally, when optimizing passivation technology, it is also important to assess the process integration and compatibility with other SiC processing steps.

The passivation layers used today for commercial SiC devices are mostly inherited from silicon technology, i.e., SiO$_2$. Silicon dioxide is still adequate for the thermal specification and voltage range of today's commercial SiC unipolar devices, although the breakthrough for SiC MOSFETs is severely hampered by the SiO$_2$/4H-SiC gate properties. For bipolar devices the surface recombination is a major issue, for instance in the region between the mesa-etched n-type emitter and the p-type base contact in 4H-SiC bipolar transistors. In this case, the increased surface recombination of a poorly passivated surface strongly lowers the transistor gain [1,2]. Also opto-electronic devices, such as LEDs, or future photovoltaic devices, will suffer from surface recombination, resulting in lower efficiency.

The basic physical behaviour of the SiO$_2$/SiC interface has been extensively studied with pioneering work, for instance by Afanas'ev [3], and there exist today a relatively well established physical model for the interface and near interface regions between SiO$_2$ and the three most common SiC polytypes, 3C, 4H, and 6H. In this model there are two types of defects related to the excess of carbon atoms at the interface, as the Si atoms are consumed in the oxidation process. These defects will give rise to bandgap states which will influence charge carrier transport at the interface. The first type are π-bonded carbon clusters of varying sizes yielding states close to the conduction band and also states distributed through the entire bandgap. Smaller clusters will have levels located close to the conduction band edge, while larger, graphitic-like clusters are more evenly distributed in the bandgap. The smaller C-clusters are also believed to be the reason why SiO$_2$/4H-SiC interfaces presents more difficulties than interfaces with 3C- or 6H-SiC polytypes; since the 4H polytype has a larger bandgap, more of the small C-clusters will be present within the bandgap in this polytype. In 3C and 6H, the states appear in the conduction band and will not be as influential for the charge carrier dynamics. The second type of defects appear on the oxide side of the interface and is often called near interface trap, NIT. The chemical origin is still under discussion, but oxygen vacancies and other intrinsic defects in the oxide have been proposed [4-7].

Large engineering efforts have been made to improve the SiC/SiO$_2$-interface and considerable progress has been made [8]. The techniques that have been attempted have again, to a large extent, been inherited from Si-technology. Many techniques to prepare the surface prior to oxidation has been reported, for instance by UV-exposure [9], ozone treatment [10] and by combing ozone and UV-cleaning [11], but also implantation of nitrogen and other ions to tailor the chemical content at the surface [12-15]. Passivation of dangling bonds at the interface have, for instance, been tried with hydrogen [16] and hydrogen peroxide annealing [17] with some progress, although it seems difficult to assure a thermal stability for these techniques. So far the most fruitful method, and also the most commonly used technique today, is post-oxidation annealing in NO or N$_2$O [18-21]. Although the N-treated SiO$_2$/4H-SiC interfaces have greatly improved the interface quality, the properties are still not as good as for the SiO$_2$/Si system. For instance, the electron surface mobility in the latter case is about 40% of the bulk mobility, while the electron surface mobility for the SiO$_2$/4H-SiC interface is around 10-15% of 4H-SiC bulk mobility. For the density of interface, or near interface, traps concentrations for the SiO$_2$/Si interface is in the low 10$^{19}$ cm$^{-2}$eV$^{-1}$ and at least one order of magnitude higher for SiO$_2$/4H-SiC. Regarding the long term and high temperature reliability, the N-annealed SiO$_2$/4H-SiC systems also needs improvements, especially when going to higher temperature operation where the full benefits of SiC can be utilized.

Although there may be further room for improvements of passivation of 4H-SiC by SiO$_2$, it is not certain that this dielectric is the best choice for SiC, for instance due to the relatively low dielectric constant of 3.8. Several studies show good results with other dielectrics of higher k-values, such as AlN [22,23], Al$_2$O$_3$ [24-28], HfO$_2$ [29,30], but for the reliability it is also important that the band offset is large enough to reduce tunneling across the barrier. The problem is that the dielectric constant is
generally inversely proportional to the bandgap, which means that alternative dielectrics with higher k-values will result in smaller offset and increased leakage. This problem could be overcome by combining layers in dielectric stacks [26,28,29,31], utilizing individual properties of each layer to optimize the overall stack performance. A highly interesting alternative dielectric is aluminum oxide, Al$_2$O$_3$, deposited by atomic layer deposition (ALD). Aluminum oxide has a similar bandgap as SiO$_2$, but has about doubled dielectric strength. It is also very well suited for the ALD process which has several advantages compared to other deposition processes. There are indications that by using this dielectric on 4H-SiC it is possible to avoid the traps in the vicinity of the conduction band (NITs)[27] and results in our group with Al$_2$O$_3$ has confirmed the promising properties and show that the electrical performance can be at least as good as that of SiO$_2$. In addition, it has recently been shown that Al$_2$O$_3$ has a much better ability to withstand ionizing radiation than SiO$_2$ [32,33], and this can be very important since one of the potential applications of SiC devices is in radiation rich environments.

In this report we will have a closer look at Al$_2$O$_3$ on n-type 4H-SiC, which will be compared to SiO$_2$. In Table I the properties two Al-based dielectric materials are compared to SiO$_2$. The table also shows values for AlN, although this material is not discussed further. The focus will be more on engineering and processing aspects -how- than on physical modelling and detailed understanding -why. It will, for instance, be shown that although “standard cleanroom procedures” are performed to clean the surfaces prior to deposition of the dielectric layer, very different results are obtained for slightly different cleaning procedures.

![Table 1. Comparison of some physical properties for SiO$_2$, Al$_2$O$_3$ and AlN, static relative dielectric constant, $\varepsilon_r$, band gap, $E_g$, difference between dielectric conduction band edge and Si and 4H-SiC conduction band edges, and thermal conductivity, $\kappa$.](image)

| Dielectric | Static relative dielectric constant $\varepsilon_r$ | Band gap $E_g$ (eV) | Conduction band offset from Si/4H-SiC (eV) | $\kappa$ (W/cmK) |
|------------|-----------------------------------------------|-------------------|------------------------------------------|-----------------|
| SiO$_2$    | 3.9                                           | 9                 | 3.5/2.7                                   | 0.015           |
| Al$_2$O$_3$| 8                                             | 8.8               | 2.8/1.7                                   | 0.02            |
| AlN        | 9                                             | 6                 | 2.2/1.7                                   | 19              |

2. Experimental methods

For the experiments, n-type epitaxial 4H-SiC grown on 4° off axis substrate wafers from SiC Crystal AG are used. Typically, the nitrogen doping of the epitaxial layer is in the range of $10^{15}$ to $10^{16}$ cm$^{-3}$ and the layer thickness is about 5-10 $\mu$m. One of the objectives of this study is to optimize the surface pre-treatment prior to deposition of the dielectric. The investigated predeposition cleaning procedures include three types, here named A, B, and C. The first surface cleaning procedure (A) is a standard 7 Up/IMEC clean consisting of 5 minutes in 3 l HSO$_4$: 1 l H$_2$O$_2$ solution followed by a de-ionized (DI) water rinse, then 100 second IMEC clean in 6 l DI H$_2$O: 60 ml isopropanol : 60 ml HF (50%) solution and, lastly, a rinse again in DI water. Procedure B consist of a 10 minute week RCA1 clean in 100 ml NH$_4$: 2 l DI H$_2$O : 400 ml H$_2$O$_2$ solution at 60 °C followed by a rinse in DI water then a dip for 30 seconds in HF (1:50) and, lastly, rinsed in DI water for 60 seconds. Finally, procedure C consists of annealing in an Ar ambient at 400 °C for 1 hour in the ALD deposition chamber prior to aluminium oxide deposition. In cases B and C the original samples have undergone procedure A prior to the additional surface processing steps. It is expected that procedure A should clean the surface of all contaminating metals and organic material and removal of the resulting oxide layer, procedure B further removes organic contaminantes and any resulting oxide layer. Finally, the annealing procedure
included in C may further remove contaminants from the sample surface. It is hoped that the differences in surface cleaning procedure will result in a beneficial passivation technique for the SiC surface. For example the organic clean in procedure B could help in reducing the negative electrical charge effects of carbon clusters in the dielectric/4H-SiC interface.

Aluminum oxide is deposited through the atomic layer deposition process (ALD) using trimethyl aluminum (TMA) and H$_2$O at 200 °C for 450 cycles for an aluminum oxide thickness of about 50 nm. The films are deposited using a BENEQ TFS 200 ALD deposition system. The films are subsequently annealed at 500 °C for 60 seconds in N$_2$O by rapid thermal annealing. Reference samples with silicon oxide are formed by depositing the layer using PECVD at 300 °C, followed by N$_2$O annealing at 1150 °C for 60 minutes. Reference samples with thermal oxide, grown at 1250 °C in N$_2$O, are also used. Back side contacts are provided by Ni silicide. The wafers are cut in 1 cm$^2$ samples and top contacts of varying sizes are formed by Al deposition to complete the MIS structures.

The characterization of the samples is mainly performed by electrical measurements, but structural properties and composition of the layers is also measured by scanning electron microscopy, ellipsometry, X-ray diffraction, and Rutherford backscattering spectrometry. These results have been published elsewhere [34]. Electrical characterization is performed in darkness and under controlled temperatures by current voltage (IV) and capacitance voltage (CV) measurements. A probe station together with a HP4156 parameter analyser and a HP4284A LCR meter is used for the IV and CV measurements, respectively.

3. Results and discussion

In order to optimize the cleaning procedures before deposition of dielectrics, three different commonly used cleaning recipes are compared. The details for these procedures, A, B, and C, are described in the previous section and the resulting CV, measured at room temperature, is shown in Fig. 1 for the three different cases. In Fig. 2 we show the values extracted from the CV data in Fig. 1 for dielectric constant, $\varepsilon_r$, flatband voltage shift, $V_{fb}$, and density of interface states, $D_{it}$, the latter estimated by the Terman method. It is obvious that the three different pre-deposition treatments have profoundly different influence on the capacitance of the structure. Procedure B provides the highest dielectric constant (10.2) lowest flatband voltage shift (3.4 V) and lowest $D_{it}$ ($1.6\times10^{11}$ cm$^{-2}$), while procedure C displays the worst values for these parameters, $\varepsilon_r$=7.4, $V_{fb}$=5.9 V, and $D_{it}$=2.9$\times10^{11}$ cm$^{-2}$.

Figure 1. Capacitance versus voltage measurements of MIS structures with ALD-Al$_2$O$_3$ for three different types of surface pre-deposition cleaning procedures, A, B and C, further described in the text.
Figure 2. Values extracted from Figure 1 for a) relative dielectric constant, b) density of interface trap and c) flatband voltage shift for the three different cleaning procedures A, B, and C.

It appears that adding the weak RCA clean to the 7Up/IMEC procedures, provides the most efficient removal of contaminants and natural SiO$_2$, which ensures a homogeneous Al$_2$O$_3$ to form. Cleaning procedure C, including “baking” of the sample in the deposition chamber before deposition, failed, possibly due to insufficient vacuum in the chamber, about 10$^{-6}$ torr. This vacuum may result in a net deposition of contaminants instead of removal. The results obtained also highlights the importance of controlling the basic processes and handling of samples in clean room environment. Such elementary procedures as wafer cleaning often have a stronger influence on the final results than introduction of new dielectrics and ingenious combinations of layers.

The choice of dielectric is of course based on the physical properties of the layers, but the choice is also intimately coupled to the deposition method. Atomic layer deposition is a very attractive method for deposition of thin films with excellent control of thickness over large areas at relatively low temperatures. Deposition of Al$_2$O$_3$ by ALD is in some sense a model example for the technique and the combination of the excellent physical properties of the layer and the deposition technique is a strong motivation for using this system. One problem for Al$_2$O$_3$ is the fixed charge, mostly negative [27], which seems to be related to intrinsic oxide defects. This charge shifts the flatband voltage, $V_{fb}$, in the CV curve to larger positive values. Figure 3 shows an extreme case of flatband voltage shift of about 20 V found in an early sample. It is also seen in the figure that the negative charge can be removed by a thermal anneal in 950 $^\circ$C in Ar atmosphere for 1 hour. The cause for the negative charge is not known, but it is most likely related to the pre-deposition treatments and inadequate removal of native SiO$_2$. However, such a long and high temperature annealing will affect the structure of the Al$_2$O$_3$, which will become more crystalline. This results in grain boundaries and increased current leakage.

For SiO$_2$ on n-type 4H-SiC the oxide charge is most often less than for as-deposited Al$_2$O$_3$. The sign of the charge in the SiO$_2$ case also varies and possible cause for this is that two dominating types of defects, one with positive charge and one with negative charge, compete. Different pre-deposition treatments, as well as growth techniques will decide which defect that will dominate [18]. Figure 4 is an illustration of this, showing CV measurements of a MIS structure consisting of 4H-SiC n-type epi with oxide either deposited by PECVD at room temperature followed by a post-oxide anneal in N$_2$O at 1150 $^\circ$C, or grown in N$_2$O at 1250 $^\circ$C. The samples have identical cleaning procedures prior to the oxidation process. The PECVD deposition process results in positive charges possibly due to charges fixed in the oxide, while the N$_2$O-grown oxide shows negative charge, which could be due to acceptor like traps close to the interface.
Figure 3. CV measurements of a MIS structure with ALD-Al₂O₃ before and after annealing in Ar atmosphere at 950 °C for 1 hour. The fixed negative charges in the oxide, or at the interface, gives a flatband voltage shift of 21 V, but following an anneal, most of this charge is neutralized.

Figure 4. CV measurements of a MIS structure consisting of n-type 4H-SiC epitaxial layers with SiO₂ deposited by PECVD and thermally grown in N₂O at 1250 °C. The PECVD deposited oxide is annealed in N₂O at 1150 °C. An ideal CV curve for the structure without flatband voltage shift is also shown.

Finally, in this brief review, we will consider the electrical breakdown properties of the dielectric. Such measurements are time consuming and often destructive and also needs to be performed on a large number of samples, since the breakdown behavior can differ substantially due to local weak spots from defects or inhomogeneous processing. In order to understand the mechanisms involved in the current conduction, it is also needed to perform measurements at different temperatures. Here we present a comparison between the typical breakdown behaviors for SiO₂ and Al₂O₃ dielectrics on n-type 4H-SiC epitaxial structures. The silicon dioxide samples are the same PECVD samples from which the CV characteristics are shown in Fig. 4, while the Al₂O₃ MIS structures are formed by ALD as described in the experimental section. The samples undergo identical cleaning prior to the dielectric formation using procedure A. The leakage current is shown as a function of forward bias field (positive bias on the top contact) in Figs. 5 and 6 for the SiO₂ and Al₂O₃ dielectrics, respectively. In Fig. 5 it can be seen that the positive bias will accumulate electrons at the 4H-SiC/SiO₂ interface, where Fowler Nordheim tunneling moves electrons across the relatively large barrier (see Table I). These electrons are then transported through the oxide to the top contact by the Frenkel-Poole mechanism, which lowers the barrier for electron emission from electronic states in the oxide bandgap. Around an electric field of 9 MV/cm the dielectric breakdown occurs and the electrons will create a localized conductive path through the oxide. Figure 6 shows the corresponding IV curve for a typical aluminum oxide MIS structure measured at room temperature. Here, a more rapid increase in the current can be seen starting already from 2.5 MV/cm, probably due to Fowler Nordheim tunneling of electrons through lower barrier between the 4H-SiC/Al₂O₃ interface. This type of behavior has also been documented by others [26]. From about 5 MV/cm, phonon-assisted tunneling is the dominating transport mechanism [23] until the dielectric breakdown. Possibly also Frenkel Poole emission is involved in the breakdown, as seen by the increased current between an electric field of 8 and 9 MV/cm. It appears that the lower offset between Al₂O₃ and 4H-SiC conduction bands, compared to the offset for SiO₂ and 4H-SiC conduction bands, may be a limiting parameter for the utilization of Al₂O₃ directly on the 4H-SiC surface. A thin SiO₂ layer could increase the barrier and improve the breakdown properties, but the purity and homogeneity of this layer must be better than what is typically achieved today.
Figure 5. Forward room temperature IV measurements up to the dielectric breakdown of a 4H-SiC MIS structure with SiO$_2$ deposited by PECVD and post-oxide annealed in N$_2$O at 1150 ºC. The breakdown is preceded by a wide range of Frenkel-Poole emission of electrons via oxide defects.

Figure 6. Forward IV measurements at room temperature of a MIS structure consisting of a 4H-SiC epitaxial layer onto which a layer of Al$_2$O$_3$ is deposited by ALD.

4. Conclusions
In this paper we have summarized some results of passivation of 4H-SiC surfaces using Al$_2$O$_3$ as an alternative dielectric to the prevailing SiO$_2$. It has been shown that the state of the surface prior to deposition of a dielectric layer is crucial to the final results and basic processing steps, such as cleaning of samples, may considerably influence the interface properties. By introducing an extra cleaning step to remove carbon related contaminants and native oxides (Procedure B), it was possible to obtain higher dielectric constant, lower flatband voltage shift and reduced concentration of interface states. The radiation hardness of Al$_2$O$_3$ makes it highly attractive for SiC device applications in radiation rich environments, but the reverse bias leakage currents may still be a problem in high voltage applications.

5. References
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