A wideband high dynamic range triple-stacked FET dual-shunt distributed analogue voltage controlled attenuator

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Abstract
The authors present a novel wideband two-dimensional voltage-controlled attenuator (VCA). The proposed design employs both stacked-FET configuration and distributed structure to achieve wideband performance, high power, and high dynamic range simultaneously. A systematic design methodology is also illustrated along with a fabricated prototype to verify the concept. The chip fabricated in a 0.15-μm Gallium Arsenide (GaAs) process exhibiting a measured power at 1-dB compression (P_{1dB}) of 25.5 dBm with a corresponding dynamic range of 32 dB. The insertion loss ranges from 2 to 5 dB over the bandwidth from 2 to 40 GHz. Furthermore, the chip is not only very compact (0.84 mm²), but it also requires only a single positive supply voltage, which makes it more appealing to highly integrated wireless applications.

1 INTRODUCTION
Wideband voltage-controlled attenuator (VCA) is one of the most critical components in measurement instrumentation, high data rate communication systems, and radar systems. Among all the applications, the VCA helps protect the receiver from being damaged by the high input power. A quality system demands a wideband, low insertion loss, high power, and high dynamic range VCA. PIN diode-based VCAs have been widely deployed due to their simplicity and high power handling capability [1]. However, the PIN devices suffer from low dynamic range and high dc power consumption. Furthermore, PIN diodes are either not available in some semiconductor processes or can add extra cost for additional fabrication layers. On the other hand, while digital discrete-step attenuators can provide high resolution, the attenuators require complicated digital control circuits. Thus, they are more suitable for CMOS and SiGe processes [2,3]. Analogue voltage control attenuator using Gallium Arsenide (GaAs) processes have recently attracted more attention because of its simplicity, high power, and low insertion loss. However, to date, few reported GaAs VCAs can achieve wideband, high power, and high dynamic range simultaneously [4–9]. The authors in [6] present the band-pass topology which allows simple and compact VCA design. Nevertheless, it can only achieve low dynamic range and low power. The series/shunt FET configuration, which is among the most popular technique employed in VCA, can provide high dynamic range and good power handling capability but suffers from high insertion loss because of the on-resistance of the series FETs [8–10]. Distributed VCAs, which were first introduced in [4], can achieve very wideband performance. A distributed stacked-FET VCA developed in [5] demonstrates a 30 dBm output power and a bandwidth up to 45 GHz. However, the average insertion loss is 4 dB and the dynamic range is limit to only 26 dB. The low dynamic range is mainly due to the quadruple stacked-FET which significantly increases the on-resistance.

A triple stacked-FET dual-shunt distributed VCA is presented here. The triple stacked-FET configuration is employed to improve the VCA power handling capability. Then, a dual-shunt network is utilised to balance the insertion loss and dynamic range trade-off. Finally, four stacked-FET cells are cascaded in a distributed structure to achieve wide bandwidth and high dynamic range. The original contributions of the paper include:

(i) The use of triple-stacked FET dual-shunt topology is presented and analysed for the first time. In particular, the triple-stacked FET can help improve power, bandwidth, and insertion loss but reduce the dynamic range. On the
other hand, the dual-shunt topology increases dynamic range while degrading bandwidth and loss. Employing both topologies can provide great flexibility to the design.

(ii) The design methodology and trade-off between bandwidth, insertion loss, power, and dynamic range will be illustrated in detail including theoretical analysis and step-by-step design methodology.

(iii) The fully integrated chip can achieve both high dynamic range and high power simultaneously.

The circuit prototype is fabricated using a 0.15-μm enhancement mode (E-mode) GaAs process. Experimental results demonstrated a 2 to 5 dB insertion loss across the bandwidth from 2 to 40 GHz. Moreover, the measured VCA dynamic range is 32 dB with an input power of 25.5 dBm. As compared to [5], this paper provides a detailed analysis of the advantages of the dual-shunt topology such as improving dynamic range without sacrificing power. Secondly, a generalized step-by-step design methodology for stacked-FET distributed VCAs is demonstrated. Finally, the proposed triple stacked-FET VCA shows an improvement of 6 dB in dynamic range and achieves among the highest figure of merit (FOM) as presented in the following sections.

2 | CIRCUIT DESIGN

The circuit schematic of the proposed VCA is presented in Figure 1. The two-dimensional VCA consists of four dual-shunt stacked-FET sections configured in a distributed structure. Each shunt arm employs a triple-stacked FET configuration. Although stacked-FET has been widely exploited in amplifier and VCA design, combining the high power handling capability provided by the stacked-FET and the inherently wide bandwidth of the distributed structure to achieve wideband performance and high power concurrently is an innovative idea. Furthermore, other specifications of the VCA such as dynamic range, insertion loss, and size also need to be taken into consideration. For instance, the stacked-FET topology can significantly degrade the dynamic range when the number of FETs in stack increases. In this paper, the dual-shunt topology is proposed to overcome this limitation. The main advantage of the dual-shunt topology is that it can improve the dynamic range while still maintaining the same power handling capability. Moreover, the idea can also be generalized to three, four, or higher number of shunt arms to compensate for a higher number of FETs in the stack and achieve as high dynamic range as needed. The design and analysis of each feature in the VCA will be discussed in the following sections.

2.1 | Stacked-FET topology

In Figure 1, each transistor is biased in the triode region. In order words, the dc drain-source voltage \( V_{DS} \) is close to 0 V. In the triode region, the equivalent circuit of the FET can be simplified as a parallel RC network. The resistance and capacitance value \( R_0 \) and \( C_0 \) of the equivalent FET circuit can be effectively controlled by the gate-source voltage \( V_{GS} \) [11].

Conventional single transistor VCAs have very limited power handling capability, especially when being deployed in GaAs and CMOS processes [2,3,11]. Therefore, a stacked-FET topology is proposed to overcome such limitations. However, while stacked-FET has been primarily deployed in power amplifiers, very few attenuator circuits use stacked-FET configuration due to the drawback of low dynamic range. Theoretically, the power handling capability will increase proportionally with the number of FETs in the stack at the cost of higher on-resistance and lower capacitance. For example, in our proposed design, when the three FETs are stacked together, the equivalent capacitance and resistance are \( \frac{C_0}{3} \) and \( 3R_0 \) respectively. Although the higher resistance can help alleviate the insertion loss, the attenuation dynamic range is significantly reduced. Furthermore, the higher number of FETs are stacked, the more difficult it is to align the phase mismatch between each FET at high frequencies. Therefore, there is an optimum number of FETs in the stack topology to achieve a good balance among all specifications. To ensure the VCA works properly, the FET needs to operate in the triode region. When the \( V_{DS} \) voltage swing is larger than the knee voltage \( V_{knee} \) (on the positive side) or smaller than the reverse breakdown voltage (on the negative side), the current flowing through the FET will increase rapidly, causing power compression at the VCA output [5,11,12]. Therefore, the maximum power handling capability is limited by either the knee voltage or the reverse breakdown of the transistor [13,14]. In GaAs processes, the knee voltage is typically much smaller than the reverse breakdown. In our proposed triple-stacked FET design, the RF voltage swing is divided equally across three transistors. Hence, the maximum voltage swing for linear operation is \( 3 \times V_{knee} \). Assuming the 50 Ω system, the maximum power handling capability of the VCA can be calculated as:
\[ P_{\text{max}} = \frac{9}{2} \frac{V_{\text{knee}}^2}{50} \]  

(1)

where \( V_{\text{knee}} \) is the knee voltage of the transistor. Note that the maximum voltage swing is the peak voltage of the sinusoidal wave, and the factor of half in the equation is to convert the peak voltage to RMS power.

### 2.2 Dual-shunt VCA design

Although the stacked-FET topology can improve the insertion loss and power handling capability as compared to the conventional single transistor VCA, the main obstacle that limits the usage of stacked-FET in VCA is the low dynamic range caused by the significantly higher resistance. Hence, there is a direct trade-off between power and dynamic range in VCA design. To overcome such trade-off, a dual-shunt topology is proposed in our design. As shown in Figure 1, the two identical shunt arms are placed in parallel. With the same number of FETs in the stack, the effective on-resistance is reduced by half. Therefore, the attenuation dynamic range can be improved while the power handling capability is maintained the same. If the VCA requires higher power, even more FETs in stack can be deployed, and at the same time, the dual-shunt can also extend to three or four-shunt arms in parallel. Theoretically, with this proposed method, the power handling capability can be increased arbitrarily without affecting the VCA dynamic range. It is worth noted that the insertion loss also decreases when the number of FETs in stack increases. Therefore, this design approach will not degrade insertion loss as compared to the conventional single transistor topology.

Figure 2 presents the simulated small-signal S-parameter of the proposed dual-shunt stacked-FET VCA versus the conventional single transistor VCA. The dual-shunt topology can reduce the insertion loss by 2 dB at 10 GHz and up to 3.6 dB at 40 GHz. The input and output return losses are also improved across the entire bandwidth from 5 to 45 GHz. Figure 3 illustrates the attenuation dynamic range of the single-shunt arm triple-stacked FET and dual-shunt arm triple stacked-FET topology. While the two topologies have identical power handling capability, the dual-shunt topology can improve the dynamic range by up to 6 dB. When the resistance \( R_0 \) is small, the improvement becomes more noticeable.

### 2.3 Wideband distributed structure

Figure 4 illustrates a single section of the distributed VCA (including a dual-shunt stacked-FET cell, two series resistors \( R_s \), and two inductors). The inductor loss is modelled as a parasitic resistance \( R_L \). The effective on-resistance and capacitance of the dual-shunt stacked-FET cell is \( \frac{3R_s}{2} \) and \( \frac{2C}{3} \), respectively. The real part will then combine with the series resistor \( R_s \) to form a T-pad attenuator cell. \( R_s \) is the total resistance including the design resistor \( R_s \) and the parasitic resistance \( R_L \). On the other hand, the imaginary part and the series inductor \( L_s \) will create an artificial 50 Ω transmission line. This artificial 50 Ω transmission line will help achieve good input and output good voltage standing wave ratio (VSWR) over a very wide bandwidth [15–18]. The inductance value, which will be realized by a microstrip transmission line, can be calculated as:

\[ L = \frac{4}{3} C_0 Z_0^2 \]  

(2)

In which \( Z_0 \) is the characteristic impedance of the system. In this case, \( Z_0 \) is 50 Ω. The cut-off frequency of the VCA can be expressed as:

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**Figure 2** Simulated S-parameters of the dual-shunt VCA and conventional VCA

**Figure 3** Dynamic range of single-shunt stacked-FET and dual-shunt stacked-FET topologies
\[ f_{\text{cut-off}} = \frac{1}{2\pi \sqrt{LC_{\text{eff}}}} = \frac{3}{4\pi \sqrt{2C_0Z_0}} \]  

(3)

On the other hand, VCA insertion loss and dynamic range are determined by the shunt resistance. Let us define \( A \) as the maximum attenuation of one section in dB. The voltage attenuation factor in linear scale will be

\[ K = 10^{\frac{A}{10}} \]  

(4)

\[ R_{\text{eff}} = \frac{3R_0}{2} = \frac{2Z_0K}{K^2 - 1} \]  

(5)

\[ R_s = Z_0 \frac{K - 1}{K + 1} \]  

(6)

It can be seen in Equation (5) that when the value of \( R_{\text{eff}} \) reduces, the value of \( K \) will increase. With a certain value of \( R_0 \), the value of \( K \) can be calculated by solving Equation (5). Then, \( R_s \) will be given in Equation (6). Although \( R_s \) is a design parameter, its value is fixed when changing the attenuation. The value of \( K \) used to calculate \( R_s \) in Equation (6) is corresponding to the average value of \( R_{\text{eff}} \) across the entire control voltage range (it is the value of \( R_{\text{eff}} \) at \( V_{\text{bias}} = 0.45 \) V in this case). Hence, the VCA can still maintain reasonable input and output return losses at both lowest and highest attenuation states.

Finally, the insertion loss of a single section (attenuation factor when the FET is turned off or \( R_0 = \infty \)) can be expressed as:

\[ \text{IL(dB)} = 20\log \left( \frac{Z_0}{Z_0 + 2R_s} \right) \]  

(7)

In our proposed design, there are four sections in the distributed structure. Hence, the total dynamic range will be \( 4 \times A \) (dB). To summarize the above analysis, the design procedure for a two-dimensional VCA would be as follows:

1. Based on the power handling capability and attenuation dynamic range requirement, determine the device size and the number of FETs in the stack using Equation (1) and simulation. In our design, a triple stack is used to achieve 26 dBm maximum power.

2. Acquire the \( R_0 \) and \( C_0 \) characteristics from a single transistor dc IV simulation. Note that \( R_0 \) and \( C_0 \) are controlled parameters and the values change non-linearly with respect to \( V_{\text{bias}} \).

3. Calculate the inductance \( L \) and series resistance \( R_s \) using Equations (2) and (6). The design resistor \( R_s \) is calculated by subtracting the inductor loss from \( R_s \). The inductor loss can be determined by electromagnetic (EM) simulation at the centre frequency of 20 GHz.

4. Estimate the final specifications: bandwidth (\( f_{\text{cut-off}} \)), dynamic range, and insertion loss. If the specifications do not satisfy the requirement, go back to step 1 to optimize the parameters.

The detailed design parameter values and circuit components of our proposed triple-stacked distributed VCA are presented in Table 1. The value of \( R_0 \) and \( C_0 \) is chosen at \( V_{\text{bias}} = 0.45 \) V, which is in the middle of the \( R_0 \) and \( C_0 \) tuning range, so that we can still maintain good input and output matching over the whole attenuation dynamic range.

![Photograph of the triple-stacked FET dual-shunt distributed VCA (1.4 mm × 0.6 mm)](image)

**TABLE 1** VCA design parameters

| Parameter | Value |
|-----------|-------|
| Number of FETs in Stack | 3 |
| Number of distributed sections | 4 |
| \( R_0 \) at \( V_{\text{bias}} = 0.45 \) V* | 29 \( \Omega \) |
| \( C_0 \) at \( V_{\text{bias}} = 0.45 \) V* | 0.095 pF |
| \( R_s \) | 19 \( \Omega \) |
| Inductance I. | 0.32 nH |
| \( P_{\text{max}} \) | 0.52 W |

*The value of \( R_0 \) varies from 4400 to 18 \( \Omega \) and the value of \( C_0 \) varies from 12.8 to 120 pF over the range of \( V_{\text{bias}} \) from 0 to 0.7 V.

**FIGURE 5** Photograph of the triple-stacked FET dual-shunt distributed VCA (1.4 mm × 0.6 mm)
3 | MEASUREMENT RESULTS

To verify the proposed design technique, a triple-stacked distributed VCA has been fabricated in a 0.15-µm enhancement mode (E-mode) GaAs process [19]. Compared to conventional depletion mode GaAs processes, the E-mode process offers the capability of using a single positive control voltage [20–22]. All the transistors are identical and have a gate width of $2 \times 25 \text{ µm}$. All bias resistors and dc blocking capacitors are realized on-chip. The VCA only requires a single positive control voltage $V_C$. The total chip size is $1.4 \text{ mm} \times 0.6 \text{ mm}$. The chip photograph is shown in Figure 5.

One other advantage of the dual-shunt topology is that it can make the circuit layout more symmetrical. Both small signal and large signal measurement were performed on-wafer using a Keysight vector network analyser PNA-X.

Figure 6a illustrates the measured insertion loss and VSWR of the VCA. The insertion loss ranges from 2 to 5 dB from 1.5 to 40 GHz while both the input and output VSWR are smaller than 1.5 across the entire frequency band.

Figure 6b further illustrates the $S$-parameter at reference state (minimum attenuation) in dB scale. Both input and output return losses are better than 20 dB across the entire frequency band.

FIGURE 6 (a) Measured insertion loss and VSWR and (b) S-parameter at reference state

FIGURE 7 Measured return losses at differential attenuation states (a) $S_{11}$ and (b) $S_{22}$

FIGURE 8 Measured dynamic range over frequency
output return losses are better than 15 dB across the entire bandwidth.

Figure 7 presents the measured input and output return losses of the VCA over the bandwidth at different attenuation levels from $A = 0 \text{ dB}$ (reference state) to $A = 32 \text{ dB}$ (maximum attenuation state). The input and output return losses have a similar response since the layout is symmetrical. The return losses at low attenuation levels are better than those at high attenuation levels. Yet, the return losses maintain better than 10 dB in all cases.

Figure 8 presents the dynamic range of the VCA at different frequencies across the bandwidth. The control voltage is varied from 0.27 to 0.7 V, and the attenuation increases with respect to the increase in control voltage. The attenuation slope and sensitivity to control voltage are mainly determined by the dc current-voltage IV characteristic of the transistors. The lowest dynamic range is 27 dB measured at 10 GHz, and the highest dynamic range is 32 dB measured at 20 GHz. The VCA achieves consistent performance over a wide frequency range.

Figure 9 presents the simulated and measured input power 1-dB compression point ($P_{\text{1dB}}$) of the VCA as a function of frequency. The maximum power handling capability is 25.5 dBm at 15 GHz. The $P_{\text{1dB}}$ is flat up to 25 GHz and slightly roll-off at 40 GHz. Additionally, the measured results are well-correlated with simulation.

Table 2 summarizes the performance of the proposed VCA as compared to previously reported wideband VCAs (both analogue-control VCAs and digital discrete-step VCAs). To provide a fair comparison among different design topologies and semiconductor technologies, we propose a figure of merits (FOM) which includes all the critical specifications of a VCA such as bandwidth, dynamic range, power, and insertion loss. The FOM is defined as follows:

$$\text{FOM} = \frac{\text{BW (GHz)} \times \text{DR} \times P_{\text{1dB}} (W)}{\text{IL}}$$

in which dynamic range (DR) and insertion loss (IL) are in linear scale (i.e. $10^\text{IL} (\text{IL}_\text{scale value} / 10)$), and bandwidth (BW) is in GHz. It can be seen that our prototype achieves the highest FOM among all VCA reported to date. Furthermore, the VCA maintains a relatively small chip size, and only requires a single positive bias voltage.

**Table 2** Comparison with previously published wideband VCAs

| Reference | Bandwidth (GHz) | Average Insertion Loss (dB) | Dynamic Range (dB) | $P_{\text{1dB}}$ (dBm) | Die Size (mm$^2$) | FOM | Topology |
|-----------|----------------|-----------------------------|-------------------|------------------------|-----------------|-----|----------|
| [2]       | 6.6–12.8       | 12.4                        | 28.4              | 13.5                   | 0.71$^1$        | 15  | Reversed saturated digital control |
| [3]       | 10–50          | 2.1                         | 11                | 5                      | 0.15            | 6   | Digital control |
| [4]       | 5–45           | 4                           | 35                | 20                     | 2.34            | 5036| Distributed |
| [5]       | 1.5–45         | 4                           | 26                | 30                     | 0.84            | 6800| Four-stacked distributed |
| [6]       | 24–32          | 3                           | 12                | 0                      | 0.4             | 1   | Band-pass |
| [7]$^*$   | 5–30           | 4.5                         | 25                | 25                     | NA              | 887 | Shunt-FET |
| [8]       | dc–40          | 4                           | 30                | 10–20                  | 1               | 504 | Series/shunt FET |
| [9]$^*$   | 2–18           | 2.7                         | 13                | 26                     | NA              | 68  | Series/shunt FET |
| [10]      | 0.05–16        | 5                           | 25                | 25                     | NA              | 506 | Series/shunt FET |
| [22]      | dc–50          | 1.4 – 2.5                   | 15                | 9 – 27                 | 1.36            | 574 | Series/stacked-shunt FET |
| This work | 2–40           | 3.5                         | 32                | 25.5                   | 0.8             | 9500| Triple-stacked + dual-shunt + distributed |

$^*$High power GaAs MESFET devices

$^5$Size excludes pads
CONCLUSION

A wideband, high dynamic range, and high output power voltage control attenuator has been demonstrated. The VCA employs both stacked-FET configuration and distributed structure to achieve bandwidth and power handling capability simultaneously. More importantly, the dual-shunt topology is proposed to increase dynamic range without sacrificing maximum power. The fabricated 0.84 mm² E-mode GaAs MMIC exhibits an average IL of 3.5 dB with the 3-dB bandwidth which covers from 2 to 40 GHz. The dynamic range varies from 27 to 32 dB and the maximum $P_{\text{dBm}}$ is 25.5 dBm. Last but not least, the VCA only requires a single positive control voltage to operate, which significantly reduces the system complexity.

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