Novel High Holding Voltage SCR with Embedded Carrier Recombination Structure for Latch-up Immune and Robust ESD Protection

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Abstract
A novel CMOS-process-compatible high-holding voltage silicon-controlled rectifier (HHV-SCR) for electrostatic discharge (ESD) protection is proposed and demonstrated by simulation and transmission line pulse (TLP) testing. The newly introduced hole (or electron) recombination region H-RR (or E-RR) not only recombines the minority carrier in parasitic PNP (or NPN) transistor base by N+ (or P+) layer, but provides the additional recombination to eliminate the surface avalanche carriers by newly added P+ (or N+) layer in H-RR (or E-RR), which brings about a further improvement of holding voltage ($V_h$). Compared with the measured $V_h$ of 1.8 V of low-voltage triggered silicon-controlled rectifier (LVTSCR), the $V_h$ of HHV-SCR can be increased to 8.1 V while maintaining a sufficiently high failure current ($I_{t2} > 2.6$ A). An improvement of over four times in the figure of merit (FOM) is achieved.

Keywords: Electrostatic discharge (ESD), Silicon-controlled rectifier (SCR), Holding voltage ($V_h$), Latch-up, Transmission line pulse (TLP)

Introduction
With the development of semiconductor integrated technology and the consistent miniaturization of semiconductor device's feature size, the device damage induced by ESD is becoming more severe. At the cost of large chip area, the conventional devices such as diode and gate grounded N-channel MOSFET (ggNMOS) featuring normal ESD robustness were reported [1]. In order to realize improved ESD capability with a smaller device dimension, the low-voltage triggered silicon-controlled rectifier (LVTSCR) has been considered as an attractive device due to its high-current capability per unit area [2]. For low-voltage applications, owing to the embedded low-trigger voltage ($V_{t1}$) ggNMOS, the LVTSCR with excellent ESD robustness is capable of providing faster ESD response speed than that obtained in conventional SCR. However, the strong inherent positive feedback causes an extremely low $V_h$ (1~2 V), which is responsible for latch-up and transient mis-trigger [3]. Such negative effects can be effectively suppressed by simply increasing $V_h$ [3–11]. The device will be free from the latch-up and transient mis-trigger, while the $V_h$ is higher than the power supply voltage (VDD). Accordingly, The N+ESD region and P+LDD region were added into SCR with additional masks and ion implant steps to improve $V_h$ [3]. However, the ESD robustness may deteriorate due to the additional power dissipation together with the increased $V_h$. In addition, the emitter voltage clamp technology for $V_h$ improvement with acceptable failure current ($I_{t2}$) was also proposed [5]. Nevertheless, the $V_h$ in the aforementioned approaches is non-adjustable which still presents inconvenience and limitation in versatile applications.

In this letter, a novel high-holding voltage silicon-controlled rectifier (HHV-SCR) is proposed and demonstrated by TCAD simulation and TLP testing. The device simultaneously achieves high $V_h$, high $I_{t2}$, and adjustable $V_h$ without any additional masks and steps. The TLP-test was carried out to validate that the $V_h$ can be effectively improved while maintaining a sufficiently
Fig. 1  
a The schematic cross-sectional view of proposed HHV-SCR.  
b The layout diagram of proposed HHV-SCR

Fig. 2  
Simulated snapback I-V characteristics of conventional LVTSCR and proposed HHV-SCR with the \( d_1 \) increasing from 0 \( \mu \text{m} \) to 0.6 \( \mu \text{m} \) at a \( d_2 = 0.5 \mu \text{m} \) and b \( d_2 = 1 \mu \text{m} \).  
c The I-V curves of HHV-SCR with different \( d_3 \) and \( d_4 \) for the fixed \( d_3 + d_4 = 3.5 \mu \text{m} \).  
d The I-V curves of HHV-SCR with various \( V_{d1} \).
high $I_{d2}$. According to the tested results, the HHV-SCR features over four times higher $V_h$ than that in the LVTSCR with the negligible degradation in $I_{d2}$.

**Method**
In this work, a novel high-holding voltage SCR with an embedded carrier recombination structure is investigated. The physical models IMPACT.I, BGN, CONMOB, FLDMOB, SRH, and SRFMOB are used in numerical simulation. Based on the model, H-RR and E-RR are optimized to achieve high $V_h$ and high $P_M$. The fabricated HHV-SCRs and LVTSCR are tested by TLP system.

**Structure and Mechanism**
The schematic cross-sectional view of the proposed HHV-SCR and layout diagram are shown in Fig. 1a, b,
respectively. The newly introduced H-RR and E-RR formed by floating N+ and P+ are identical to the N+ and P+ in the anode and cathode areas, respectively. The floating N+ in H-RR (or floating P+ in E-RR) is placed next to the P+ region in the anode (or N+ region in the cathode). Moreover, the new floating P+ in H-RR (or floating N+ in E-RR) is also located next to the aforementioned floating N+ in H-RR (or floating P+ in E-RR). The low-trigger N+ in H-RR (TN+) and low-trigger P+ in E-RR (TP+) are also fabricated by the same processes as the N+ (or P+) region in the anode (or cathode) to ensure the $V_{th}$ within an acceptable range. As a positive ESD voltage ($V_{ESD}$) rising up to a certain level, the TN+/P-well/TP+ junction with a low-breakdown voltage will breakdown first followed by the snapback of the parasitic transistors triggered by the avalanche current. The strong positive feedback of the parasitic BJTs is responsible for the considerably low $V_{th}$ of the LVTSCR. In the HHV-SCR, the N+ in H-RR (or the P+ in E-RR) will recombine the minority carriers injected from the edge of anode P+ (or cathode N+), which reduces the current gain ($\beta$) of the parasitic PNP (or NPN) and eliminates the surface bipolar effect. Importantly, the P+ in H-RR (or the N+ in E-RR) blocks the surface low-resistance path by recombining the surface electrons (or holes). Compared with the H-RR without P+ (or E-RR without N+), the new P+ in H-RR (or the N+ in E-RR) provides the additional recombination to eliminate the surface electrons (or holes) injected from cathode (or anode) and those induced by impact ionization (shown in Fig. 3a), which brings about the further increasing of $V_{th}$. By combining these modifications, a significant improvement in FOM is verified. The figure of merit (FOM) is cited from [7] and defined as the tolerable power density of single device given by $FOM = (V_{th} I_{t2})/(N \cdot W)$ to evaluate the $V_{th}$ and $I_{t2}$ performance of single device. Generally, accompanied by the improving of $V_{th}$ performance, it still causes the degradation of $I_{t2}$ due to the higher-power dissipation. Therefore, the higher FOM signifies the single device can achieve the higher current capability on the higher $V_{th}$ level ($N$ is the number of the stacking device; $W$ is the device width).

**Results and Discussion**

**Simulated results**

The device characteristics were studied and simulated by TCAD Medici, where the corresponding models such as impact ionization and concentration-dependent mobility model were used. The simulated I-V curves of the LVTSCR and HHV-SCRs are shown in Fig. 2. The $V_{th}$ of the LVTSCR is as low as 1.8 V, while the $V_{th}$ of the HHV-SCR is improved from 4.6 V to 8.1 V with $d_1$ decreased from 0.6 $\mu$m to 0 $\mu$m for $d_2 = 0.5$ $\mu$m. In fact, the smaller $d_1$ is favored for improved recombination capability of N+ in H-RR (or P+ in E-RR) to obtain a lower $\beta$, which explains that the HHV-SCR always achieves the highest $V_{th}$ for $d_1 = 0$ $\mu$m. The simulated results in Fig. 2b indicate that the $V_{th}$ of HHV-SCR is further improved with $d_2$ increased from 0.5 to 1 $\mu$m due to the increasing of device length. For demonstration, the P+ in H-RR (or N+ in E-RR) is also a key factor to

| Table 1 Comparison of experimental results |
|--------------------------------------------|
| Experimental devices | L/W ($\mu$m/$\mu$m) | $V_{th}$ (V) | $I_{t2}$ (A) | $V_{CL}$@1.3 A (V) | FOM (mW/\mu m) |
|----------------------|---------------------|-------------|-------------|-----------------|-------------|
| Conventional LVTSCR  | 15/50               | 1.8(< 5)   | 3.2         | 4.8             | 110         |
| Proposed HHV-SCR     |                     |             |             |                 |             |
| $d_2$ ($\mu$m)       | $d_1$ ($\mu$m)      | $V_0$ (V)  | $I_{t2}$ (A) | $V_{CL}$@1.3 A (V) | FOM (mW/\mu m) |
| 0.5                  | 0.0                 | 17/50      | 8.0         | 3.04            | 8.5         | 490        |
| 0.2                  | 17.4/50             | 7.4        | 3.12        | 8.9             | 460        |
| 0.4                  | 17.8/50             | 6.1        | 3.0         | 8.9             | 370        |
| 0.6                  | 18.2/50             | 5.5        | 2.7         | 9.5             | 300        |
| 1.0                  | 17.5/50             | 8.1        | 2.8         | 8.4             | 450        |
| 0.2                  | 17.9/50             | 8.0        | 2.8         | 8.8             | 450        |
| 0.4                  | 18.3/50             | 7.0        | 3.0         | 8.8             | 420        |
| 0.6                  | 18.7/50             | 6.0        | 2.9         | 9.8             | 350        |

| Table 2 List of Abbreviations |
|------------------------------|
| Abbreviation | Full name |
|----------------|-----------|
| HHV-SCR | High-holding voltage silicon-controlled rectifier |
| ESD | Electrostatic discharge |
| TLP | Transmission line pulse |
| H-RR | Hole recombination regions |
| E-RR | Electron recombination regions |
| ggNMOS | Gate grounded N-channel MOSFET |
| LVTSCR | Low-voltage triggered SCR |
increase $V_h$. The simulated results are shown in Fig. 2c. When the H-RR (or E-RR) with fixed $d_3 + d_4$ is completely formed by heavy doping N+ (or P+) (e.g., $d_3 = 3.5 \, \mu m$, $d_4 = 0 \, \mu m$), the simulated $V_h$ is 7.1 V. By inserting the P+ inside H-RR and N+ inside E-RR with fixed $d_3 + d_4$ (e.g., $d_3 = 2.5 \, \mu m$, $d_4 = 1.0 \, \mu m$), the simulated $V_h$ can be increased up to about 9.5 V. It can be inferred that the new P+ in H-RR (or N+ in H-RR) is effective in recombining surface avalanche electrons (or holes) to block the surface current path. Therefore, a higher $V_h$ is required for the HHV-SCR to sustain the same holding current ($I_h$). The recombination curve alone AA’ line shown in Fig. 3a demonstrates the increasing of recombination rate induced by new P+ in H-RR (or N+ in E-RR). The TN+ and TP+ are adopted to ensure the $V_t$ within an acceptable range. By adjusting the $d_2$ and $d_5$ at the fixed $d_5 + d_2 + d_5$, the $V_{t1}$ of HHV-SCR can be significantly reduced from 12 V to 9.0 V to meet the design window of 5 V circuits with the negligible impact on $V_h$, shown in Fig. 2d. The current distribution diagrams of the simulated devices at the holding point are
also shown in Fig. 3b, c, respectively. Compared with the current distribution in the HHV-SCR with $d_3 = 3.5 \mu m$, $d_4 = 0 \mu m$, the surface current path in proposed HHV-SCR is blocked due to the additional recombination rate benefited from P+ in H-RR and the N+ in E-RR.

Experimental Results

The fabricated devices are tested by TLP system. The total widths (W) of all tested SCR are 50 $\mu m$ and with single finger for the parameter’s comparison (Table 1).

All of the tested devices occupy the similar layout area. The device parameters are shown in Table 2. Figure 4a shows the TLP measurement curves of the HHV-SCRs with $d_2 \neq 0.5 \mu m$ (called devices B1) and the LVTSRR. According to the experimental results, the $V_h$ of HHV-SCR is increased from 5.5 to 8.0 V with the $d_1$ decreased from 0.6 $\mu m$ to 0.0 $\mu m$, which is much higher than 1.8 V obtained in the conventional LVTSRR. As the $d_2$ increases from 0.5 to 1 $\mu m$, the corresponding HHV-SCRs (called devices B2) obtain a higher $V_h$ shown in Fig. 4b. Considering the design window, the clamping voltage ($V_{CL}$) under the given index is also a key parameter to evaluate clamping ability. From the tested results, the $V_{CL}$ of single finger HHV-SCR is also kept within the acceptable range at the HBM = 2 kV ($I_{TLP}=1.3 \ A$) although the finger width is only 50 $\mu m$. However, all devices cannot provide the eligible $V_{CL}$ under the stronger ESD stress due to the high $V_h$ and large dynamic resistance ($R_{dy}$) induced by undersized device width. For satisfying the higher on-chip ESD requirement, the finger width is extended to the acceptable 300 $\mu m$ for $d_1 = 0.6 \mu m$, $d_4 = 0.5 \mu m$, and $d_1 = 0.6 \mu m$, $d_4 = 0 \mu m$. The TLP testing shown in Fig. 5 demonstrates that the HHV-SCR with $d_4 = 0.5 \mu m$ features the extremely low $R_{dy}$ (about 0.7 $\Omega$), superior ESD robustness ($I_{CL} > 10 \ A$) and high $V_h$ of 6.7 V. It can be observed that the $V_{CL}$ is as low as 6.7 V at the $I_{TLP} = 5.4 \ A$ (HBM = 8 KV). Furthermore, the higher $V_h$ benefited from P+ in H-RR (or N+ in E-RR) is also proved, as compared with the TLP curve of SCR with $d_4 = 0 \mu m$. The tested results of 50 $\mu m$ single-finger devices are listed in Table 1.

Conclusion

A novel CMOS-process-compatible HHV-SCR is studied and measured by TCAD simulation and TLP system. Compared with the conventional LVTSRR, the HHV-SCR features significantly improved $V_h$ (an improvement of over 450% in the $V_h$ is achieved) and without sacrificing the chip area. Furthermore, the $V_h$ of the HHV-SCR can be adjusted from 5.5 V to 8.1 V to satisfy the different $V_h$ requirements with negligible degradation in $I_{CL}$. In terms of $R_{CL}$, compared with the conventional LVTSRR, over 200% improvement is also achieved.

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Not applicable.

Authors’ Contributions

ZW proposed the novel structure and was a major contributor in writing the manuscript. ZQ was a major contributor in simulating the devices. LL drew the layouts and tested the devices. MQ verified the results and revised the manuscript. Others authors offered comments and revised the manuscript. All authors read and approved the final manuscript.

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Availability of Data and Materials

All data generated or analyzed during this study are included in this published article.

Competing Interests

The authors declare that they have no competing interests.

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