FPGA-based real-time 105-channel data acquisition platform for imaging system

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# Table of Contents

| Section                              | Page |
|--------------------------------------|------|
| Table of Contents                    | 2    |
| 1 Abstract                           | 3    |
| 2 Previous work                      | 3    |
| 3 System Design                      | 4    |
| 4 Block control                      | 5    |
| 5 Implementation Schedule            | 7    |
| 6 PCB design                         | 7    |
| 7 Test and Evaluation System         | 12   |
| 8 Test Results                       | 13   |
| 9 References                         | 15   |
| 10 Appendix                           | 115  |
1 Abstract

In this paper, a real-time 105-channel data acquisition platform based on FPGA for imaging will be implemented for mm-wave imaging systems. PC platform is also realized for imaging results monitoring purpose. Mm-wave imaging expands our vision by letting us “see” things under poor visibility conditions. With this extended vision ability, a wide range of military imaging missions would benefit, such as surveillance, precision targeting, navigation, and rescue. Based on the previously designed imager modules, this project would go on finishing the PCB design (both schematic and layout) of the following signal processing systems consisting of Programmable Gain Amplifier (PGA) (4 PGA for each ADC) and 16-channel Analog to Digital Converter (ADC) (7 ADC in total). Then the system verification would be performed on the Artix-7 35T Arty FPGA with the developing of proper controlling code to configure the ADC and realize the communication between the FPGA and the PC (through both UART and Ethernet). For the verification part, a simple test on a breadboard with a simple analog input (generated from a resistor divider) would first be performed. After the PCB design is finished, the whole system would be tested again with a precise reference and analog input.

2 Previous work

The signal source (the imager module) has already been designed in previous works. The imager module is a high-power 0.53 THz source module with programmable diversity to adjust the brightness and the direction of light to obtain the desired diffuse lighting conditions in THz imaging applications. The source module consists of a single SiGe BiCMOS chip which operates an array of 16 source pixel incoherently. Each source pixel consists of a primary on-chip ring-antenna and two triple-push oscillators locked 180° out-of-phase. The module provides a total radiated power of up to 1 mW (0 dBm) with 62.5 μW (−12 dBm) per source pixel on average and an EIRP per pixel of 25 dBm. The chip consumes up to 2.5 W from a 2.4 V supply and 3.2 mW from a digital 1.2 V
supply respectively. The module includes a secondary silicon lens, is programmable through a CPLD, and supplied from a USB port. The THz radiation can be recorded with a CMOS 1 k-pixel THz video camera and represent an all silicon solution for real-time active THz imaging.

3 System Design

The purpose of this project is to provide a data acquisition system for the image signal generated by the image module. The major part of this system can be divided into 3 sub-systems, the image module, the signal processing board (including 7 of 16-channel ADC, 4 of 4-channel PGA for each of the ADC, and a reference chip provided for each ADC) and finally a verification & communication system consisting of a FPGA and an Ethernet module to PC.
Based on the previous work done with the design of the imager modules, the main task of this project is to finish the following signal processing and the verification & communication system.

So the first task would be designing the PCB schematic and layout of the signal processing system (ADC, PGA, reference chip) satisfying all the layout and supply bypassing requirements for all 3 chips.

Then we need to realize the system verification using the FPGA along with the communication through the Ethernet or the UART first with simple bread board and finally with the PCB board.

4 Block control

4.1 ADS7953:

Timing requirement:

The Serial data output (SDO) signal includes a 4-bit channel address and a 12-bit conversion result (MSB first). At the 16th falling edge of SCLK, SDO goes to 3-state and the conversion also ends. The Serial data input (SDI) data latched at the rising edge of SCLK, and consists of 16-bit per frame.
At the 2nd SCLK falling edge we need to select a new MUX channel. At the 14th SCLK rising edge we need to start acquisition until next CS falling edge.

The GPO data comes from SDI of previous frame, and the GPO data is refreshed at the falling edge of CS signal. The GPI status latched also at CS falling edge, the corresponding output is on the SDO. The CS signal is pulled high only after the 16th SCLK.

In the real operation, we need to set the ADC in Auto-1 mode, including the following features:

- Scan pre-programmed channels in ascending order;
- Separate “program register” for pre-programming the channel sequencing;
- FFFF default, scan all channels in ascending order.

The corresponding states of control signals are shown in the following figure.
4.2 MCP6G04

| Gain          | MCU Pin’s State                                      |
|---------------|------------------------------------------------------|
| +1 V/V        | Output PIC’s $V_{REF}$ at $V_{DD}/2$                 |
|               | Digital Output High-Z *(Notes 1)*                    |
|               | Output $V_{DD}/2$ PWM signal *(Notes 2)*             |
| +10 V/V       | Digital Output driven Low                           |
| +50 V/V       | Digital Output driven High                          |

| Pin | Description            |
|-----|------------------------|
| 1   | $V_{OUTA}$             |
| 2   | $V_{GSEA}$             |
| 3   | $V_{INA}$              |
| 4   | $V_{DD}$               |
| 5   | $V_{INB}$              |
| 6   | $V_{GSELB}$            |
| 7   | $V_{OUTB}$             |
| 8   | $V_{OUTC}$             |
| 9   | $V_{GSEL}$             |
| 10  | $V_{INC}$              |
| 11  | $V_{SS}$               |
| 12  | $V_{IND}$              |
| 13  | $V_{GSELD}$            |
| 14  | $V_{OUTD}$             |

5 Implementation Schedule

| Event                                      | Date            |
|--------------------------------------------|-----------------|
| Block PCB schematic and layout design      | November 15th, 2015 |
| System verification using bread board      | November 10th, 2015 |
| System PCB schematic design                | November 20th, 2015 |
| System PCB layout design                   | December 1st, 2015 |
| Realization of Ethernet communication with PC | December 20th, 2015 |
| System verification with PCB board         | December 25th, 2015 |

6 PCB Design

6.1 Block schematic and footprint design

6.1.1 ADS7953:
As shown in the figure, the distance between the middle of 2 pin columns is 5.6mm. The pin size is 1.6mm*0.3mm, and the width between the middle of 2 pins is 0.5mm.

As shown in the figure above, for the layout implementation, we need a 1uF capacitor for both analog and digital supply bypass. Also we need a 10uF capacitor at the reference input of the ADC.
Also, for each of the analog input channel, we would follow the requirement shown in the figure above. A 150pF capacitor is sitting at the input of each channel.

6.1.2 MCP6G04

Layout Consideration:
1). Supply bypass

Use a local bypass capacitor (0.01 μF to 0.1 μF) within 2 mm of the VDD pin for good, high frequency performance. It must connect directly to ground.

Use a bulk bypass capacitor (i.e., 1.0 μF to 10 μF) within 100 mm of the VDD pin. It needs to connect to ground, and provides large, slow currents. This capacitor may be shared with other nearby analog parts.

2). Footprint size

The distance between the middle of 2 pin columns is 5.2mm. The pin size is 2.2mm*0.6mm, and the width between the middle of 2 pins is 1.27mm
6.1.3 REF5040

As for the footprint size of the reference chip, we follow the dimension in the figure above. The distance between the middle of 2 pin columns is 4.4mm. The pin size is 1.45mm*0.45mm, and the width between the middle of 2 pins is 0.65mm.

As shown in the figure above, we need a 1uF to 10uF (In the real design I choose 1uF) from supply input of the reference chip to ground. Also we need a 1uF to 50uF capacitor at the output of the reference chip (In the real design I choose 22uF).

6.1.4 Header
We need a 2*10 and a 2*5 header in the processing board. For the PCB footprint size, we set the distance between the centers of 2 holes to be 100mil, the inner diameter to be 2*17.716mil and the outer diameter to be 2*29.526mil.

6.2 System schematic design

As shown in the figure above, the PCB schematic of the signal processing system is implemented including all the necessary supply bypass capacitors and input bypass capacitors.

6.3 System layout design

The following figure shows the dimension demand for the PCB layout board of the signal processing system.
7 Test and Evaluation System

7.1 Simple test on bread board

This simple test platform is based on a bread board, with a 16-channel ADC and a 4-channel PGA on the bread board. The input signal of the PGA is generated by a variable resistor divider (dividing the reference voltage). Then the output voltage of the PGA goes into the channel 0 of the 16-channel ADC. The SDO, SDI, CS (chip select), SCLK (serial clock) signals of the ADC is connected with 4
GPIO ports on the FPGA. And the FPGA is connected to the PC through the UART so that we can see the data output from the serial port window in the PC.

The initial and reset signal for the ADC is connected to 2 switches on the FPGA to make it easier to make the ADC operate in Auto-mode 1.

The developing code for configuring the ADC and UART, along with the Matlab code to get the output data from the UART is included in the appendix of this document. In the code we can choose which channels to be activated when operating in Auto-mode 1.

8 Test Results

The first 2 figures above shows the result from the serial port window on the PC of 2 cases:
1. Only channel 0 and channel1 are turned on;
2. All the 16 channels are turned on.
We can see from the result that only the activated channels will be exporting data and in Auto-mode1 the channels would export data in a serial order from channel 0 to channel 15.

Also, since only channel 0 has the input from the PGA output, all the signals from the other channels of the ADC are almost 0.

![Image](image.png)

The last 2 figures show the result when only channel 0 is turned on and we change the input signal of the PGA through rotating the controlling button of the variable resistor. We can see there're only outputs from channel 0. And also when changing the input signal of the PGA, the system output will change accordingly.
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