A 10-GS/s 8-bit 4-way interleaved folding ADC in 0.18 µm SiGe-BiCMOS

Huasen Liu¹,², Danyu Wu¹, Lei Zhou¹, Yinkun Huang¹, Jian Luan¹, Xuan Guo¹, Dong Wang¹,², Xuqiang Zheng¹, Jin Wu¹, and Xinyu Liu¹a)

¹ Institute of Microelectronics of Chinese Academy of Sciences, Beijing 10029, China
² University of Chinese Academy of Sciences, Beijing 10029, China
a) xyliu@ime.ac.cn

Abstract: In this paper, a time-interleaved 10-GS/s 8-bit analog-to-digital converter (ADC) fabricated in 0.18 µm SiGe BiCMOS technology has been demonstrated. A 4 × 4 input multiplexer with good isolation and wide input bandwidth is proposed, which enables the ADC to support 1/2/4-channel sampling modes. In the track-and-hold (THA) stage, a switched emitter follower (SEF) topology with delayed dummy clock is introduced to minimize the overshoot effect of the SEF output. The ADC achieves spurious free dynamic range (SFDR) > 52 dBc and effective number of bits (ENOB) > 6.8 in low input frequencies. The analog input bandwidth is 5.6 GHz.

Keywords: analog-to-digital converter, analog input multiplexer, SiGe BiCMOS, time-interleaved, track-and-hold

Classification: Integrated circuits

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1 Introduction

Ultra high-speed analog-to-digital converters (ADCs) are playing critical roles in software defined radios, optical communications and high-end test equipment [1, 2, 3]. With the continuous development of digital process, the demand for high performance ADCs in multi-GHz range becomes more and more urgent. The folding-interpolating ADC is a good choice for the ADC with multi-GHz sampling frequency and medium resolution (6–10 bits) [4]. In contrast to the pipelined ADC, it is able to get a higher sampling rate because of no feedback loop in the circuit. Compared with the flash ADC, it uses fewer comparators to get the same precision and keeps the merit of low latency. However, the sampling rate of a single-core ADC is always limited by the devices’ performance. Therefore, the time-interleaved ADC is often adopted to relieve the sampling rate pressure of the single channel ADC [5]. And to satisfy the requirements in many system applications, more and more ADCs working in multi-channel mode are used.

In this paper, a 4-channel time-interleaved 10-GS/s 8-bit ADC fabricated in 0.18 µm SiGe BiCMOS technology has been demonstrated. An input multiplexer with good isolation is proposed to make the ADC able to work in multi-channel modes (1/2/4-channel). A switched emitter follower (SEF) topology is presented to minimize the overshoot effect of the SEF output by using delayed dummy clock. Based on the measurement results, the analog input bandwidth of the ADC can achieve 5.6 GHz. The effective number of bit (ENOB) is above 5.6 and the spur free dynamic range (SFDR) is above 43 dBc in the full range of the first Nyquist zone. The standard figure-of-merits (FOM) is 10.1 pJ/conversion-step.

2 Proposed ADC architecture

The architecture of the proposed ADC operating at 10-GS/s sampling rate is illustrated in Fig. 1. It consists of a 4 × 4 input multiplexer and four interleaved 2.5-GS/s 8-bit folding-interpolating ADCs. The input multiplexer enables the ADC to work in the following three modes: a single 10-GS/s ADC, two channels 5-GS/s ADCs and four channels 2.5-GS/s ADCs. By sending commands to the logic
control unit via the SPI bus, offset error, gain error and time skew error are calibrated by using twelve current steering DACs to convert the errors into analog signals. The outputs of the ADC use 1:2 demux and are converted into standard low voltage differential signals (LVDS) for measurements and applications.

The sub-ADC adopts a two-stage cascaded folding-interpolating structure with a folding factor of 4 in each stage. The overall sixteen folding curves generated by the second-stage interpolating circuit are fed into 16 comparators respectively, whose outputs are encoded to 4 least significant bits (LSBs). To the most significant bits (MSBs), the 5th bit can be directly obtained from the result of the first comparator in the second stage, since its weight corresponds to the first folding interpolating curve generated by the second stage (folding factor = 16). And the 7th bit is obtained by comparing the output of the first folding interpolating curve in the first stage (folding factor = 4). Although the quantization curves of the 6th and 8th bits cannot be directly generated (the corresponding folding factors are 8 and 2 respectively), they can be obtained by processing the specific intermediate signals of the folding amplifiers because the folding factors of the folding curves are all a power of 2. These processing circuits are the analog process units shown in Fig. 1.

The analog process units perform OR operation on the intermediate analog signals, which is not the same as the digital logic that only produces 0 and 1, the specific processing is detailed in [6]. In contrast to the other folding topologies, extra coarse quantizing flash ADC is replaced by these analog process units, which reduces the complexity of the sub-ADC obviously. Hence, only 3 comparators are needed to quantify the 3 MSBs (bit6–bit8). In the practical circuit, three additional comparators are introduced to synchronize the 3 MSBs and the 4 LSBs by using bit5 so that a total of 22 comparators are used. By utilizing the intermediate folding and interpolating signals to obtain the high bits, the number of comparators is reduced.
compared to the common types of folding-interpolating ADCs [7]. In addition, a cascode amplifier is added at the front of the comparator to reduce offset voltage and error rate.

3 Circuit implementation

3.1 Wide band 4 × 4 analog input multiplexer

The analog input multiplexer with good isolation plays an important role in the multi-channel ADC. This paper presents a wide band isolated input multiplexer with the following features:
1. High linearity within the full bandwidth (DC ~ 6 GHz);
2. Keep the channels well isolated (typically >60 dB);
3. Maintain the bandwidth well matched, thus enabling high input bandwidth when operating at 1-ch mode.

The Fig. 2(a) shows the block diagram of the input multiplexer. It is consisted of 16 (4 groups) open-collector buffers, which within the same group are connected to combine the output current. Four input signals are fed into four buffers in each group respectively so that each input channel can route to any sub-ADC freely. In any mode, only one buffer is switched on in each group, keeping a constant output current swing.

The adopted pseudo-differential input buffer based on the half diode-bridge topology achieves high bandwidth and good linearity [8], which is shown in Fig. 2(b). The nonlinearity of this circuit is mainly caused by the limited output impedance of the two current sources. Assume that the input signal increases by \( \Delta V_{in} \), the output voltage can be expressed as

\[
V_{out} = V_{in} + V_T \ln \left( \frac{I_1 - \Delta V_{in}/R_1}{I_1 + \Delta V_{in}/R_1 + \Delta V_{in}/R_2} \right),
\]

by expanding it according to Taylor series, the third harmonic is

\[
HD_3 = \frac{3(I_1 R_1 R_2 + \Delta V_{in} R_1 + \Delta V_{in} R_2)^3}{V_T \Delta V_{in}^2 (2R_2 + R_1)^3},
\]

When \( R_1 \) and \( R_2 \) are large enough, the formula (2) can be simplified as

\[
HD_3 = 20 \log \left( \frac{(I_1 R_1)^3}{9V_T \Delta V_{in}^2} \right),
\]

However, the voltage fluctuations at \( V_{COM} \) and \( V_{out} \) can seriously deteriorate the isolation of the buffer. The detailed circuit of the open-collector buffer is shown in Fig. 2(c). The current sources are all switched off at the OFF state. Above all, the switches \( K_1 \) and \( K_2 \) which are MOSFET switches are introduced to keep the \( V_{COM} \) and \( V_T \) to constant voltages when the buffer is switched off. Both \( Q_1 \) and \( Q_2 \) are reversely biased so the parasitic capacitances of them are suppressed a lot. The simulation of the parasitic capacitances of \( Q_1 \) and \( Q_2 \) versus \( V_{BE} \) at 1 GHz is shown in Fig. 3(a). It can be found that the parasitic capacitance at \( V_{BE} = 0.8 \) V is reduced by nearly 50% compared to that at \( V_{BE} = 0.6 \) V. Moreover, the two switches also provide two low resistance channels to signal ground which increases the isolation greatly. The two switches will be switched off when the buffer is switched to the ON state, so the influence of the introduction of the switches on the
circuit’s bandwidth and linearity is negligible because the parasitic capacitance is mainly determined by $C_{GD}$ when the two switches are switched off. The simulation of the isolation compared to that without the switches is shown in Fig. 3(b). The result shows an isolation above 70 dB between different channels within an input frequency range of 6 GHz. The isolation with switches raises about 46 dB at 1 GHz. In addition, the capacitor $C_{boost}$ is introduced to realize bandwidth boosting by giving peaking at the high frequency.
3.2 Track-and-hold circuit

The track-and-hold amplifier (THA) based on differential SEF is shown in Fig. 4(a). It is composed of an input stage, an SEF stage and an output emitter follower. In the traditional SEF topology [9], a big voltage overshoot will be introduced at the output node of SEF when the sampling switch is switched, which may cause the switch and the post-stage circuit to work in abnormal region and introduce new distortions. In this SEF stage, a dual-switch structure is used, consisting of a sampling switch (Q3 and Q4) and a hold switch (Q1 and Q2). The timing diagram is shown in Fig. 4(b). Each pair of the clocks in each switch are reversed, CK_T and CK_Hd are clocks of the sampling switch while CK_Td and CK_H are clocks of the hold switch. When the SEF changes from hold mode to sample mode, the sampling switch is turned on later than the turn off of the hold switch since the path from node A to Q1 is longer than the path to Q4. When the SEF changes from sample mode to hold mode, the sampling switch and the hold switch are designed to switch at the same time because the switch-off time of the bipolar transistor is longer than its switch-on time, although the path to Q1 is longer. In this timing, the influence of the switch-on/off of the SEF on the voltage at point A can

Fig. 4. (a) The THA of ADC. (b) The timing diagram. (c) The comparison of the two switches.
be generated at approximately the same time, either from the sample to the hold phase or from the hold to the sample phase, which reduces the overshoot voltage effectively. The comparison of the waveforms at node A is shown in Fig. 4(c). The transistor Q8 which is 2/3 size of Q1 is added to decrease the parasitic capacitance at node B and save the voltage margin.

The capacitor \( C_f \) is introduced to cancel the accuracy error caused by the feedthrough [6]. The structure of \( C_f \) is implemented by transistors. After the introduction of \( C_f \), the feedthrough signal relative to the input signal can be expressed as

\[
A_{ff} = 20 \log \left[ \frac{C_{be}}{C_{be} + C_h \left( 1 - \frac{C_f}{C_{be}} \right)} \right].
\]

Moreover, the resistor \( R_S \) is added to relieve the effect that the emitter follower charges and discharges the capacitive load directly will lead to a decrease in linearity because of causing large glitch in the waveform in time domain.

In the common, the base current \( I_b \) needs to be extracted from the sampling capacitor to drive the post-stage circuit in hold mode, the drop of the holding voltage at node A will reduce the accuracy of quantization. Therefore, the output buffer consisting of two stages is adopted in Fig. 4(a). The first stage is similar to the input stage of the multiplexer to provide high bandwidth and good linearity. What’s more, the drop of the holding voltage is linear in this structure since the base current of Q9 is constant. Hence this effect can be greatly offset by the differential configuration. However, a large drive current is often required because the post-stage is usually the input of a folded amplifier, which consists of multiple differential pairs. Therefore, \( I_1 \) is a small bias current to avoid excessive \( I_b \) to be extracted. To make it have a large driving capacity, the second stage is added to drive the post-stage (the folded amplifier). In addition, the negative feedback structure consisting of Q10 and Q12 is introduced to suppress the effect of the output transistors’ \( V_{be} \) modulation effectively.

### 3.3 Self-calibration system

For time-interleaved ADC made in deep submicron process, the digital calibration technique is often used to eliminate the interchannel errors (offset, gain mismatch and time skew) due to process variation. This paper adopts a method of foreground self-calibration to calibrate offset, gain mismatch and time skew between the channels of the time-interleaved ADC. As shown in Fig. 1, we use three independent feedback loops incorporating with FPGA to adjust the three kinds of errors respectively. When the calibration starts, a sinewave is fed into the ADC, the outputs of which are transmitted into the FPGA. Then the three kinds of errors are compared with the corresponding reference in FPGA respectively, and the logically processed results are sent back to the internal control logic of the ADC by the SPI lines. The errors are adjusted inside the ADC by the current DACs. After several cycles of the calibration, the values of the calibration registers will gradually converge to a fixed value respectively. Then the values are locked to fix the output currents of the DACs, and the whole calibration process is completed. Offset, gain mismatch and time skew can be calibrated at the same time. Offset is calibrated by...
adjusting the output voltage of the THA to make sure the average output code of all sub-ADCs is 127.5; gain mismatch is calibrated by regulating the output voltage range of reference ladder in four sub-ADCs; and time skew is calibrated by using the digital controlled delay line (DCDL) module. Both gain mismatch and time skew take the first channel as a reference [10]. As shown in Fig. 5(b), this method of calibration can improve SFDR and ENOB effectively.

4 Measured results

The proposed ADC has been fabricated in 0.18 um SiGe BiCMOS technology. The core ADC consumes 4.9 W from the supplies of 3.3 V and 1.8 V. The die micrograph is shown in Fig. 5(a), the whole chip has a die size of 5.0 mm × 5.2 mm (including pads). The measured output spectrum is shown in Fig. 5(b) when a 450.1 MHz input sine wave is sampled at 10 GS/s. Its signal-to-noise-and-distortion ratio (SNDR) is 41.48 dB and spurious-free-dynamic-range (SFDR) is 48.32 dB. As shown in Fig. 6(a), the measured static performance shows that the DNL is within +0.3/−0.3 LSB and the INL is within +1/−1 LSB. Fig. 6(b) presents the measured ENOB and SFDR versus input frequency at a sampling rate of 10 GHz, the SFDR achieves 52 dB and the ENOB is above 6.8 bits at low input frequency. In the full range of the first Nyquist zone, the SFDR stays above 43 dB.

![Fig. 5.](image1) (a) The die micrograph. (b) Output FFT spectrum.

![Fig. 6.](image2) (a) DNL and INL. (b) SFDR and ENOB versus input frequency.
and the ENOB is beyond 5.6 bits. The full power −3 dB analog bandwidth is 5.6 GHz. The standard figure-of-merits (FOM) is $10.1 \text{pJ/conversion-step (FoM} = \frac{P}{(2^{\text{ENOB}_{\text{Nyquist}}} \times \text{Sample Rate})} \text{). Table I gives a comparison of the ADC performance with similar architectures in SiGe technology.}

| Reference | [6] | [9] | [11] | This work |
|-----------|-----|-----|------|-----------|
| Technology | 0.35 µm SiGe | 0.25 µm SiGe | 0.25 µm SiGe | 0.18 µm SiGe |
| Architecture | TI-FI | FI | FI | TI-FI |
| fs (GSps) | 4 | 10 | 6 | 10 |
| Resolution (bits) | 8 | 8 | 9.5 | 8 |
| ENOB (Nyquist) | 5.6 | 6.8 | 7.3 | 5.6 |
| Power (W) | 3 | 9.1 | 10.2 | 4.9 |
| FOM (pJ/conv)) | 15.4 | 10.2 | 10.8 | 10.1 |

5 Conclusion

In this paper, a 10-GS/s 8-bit ADC which support all 1/2/4-channel sampling modes has been demonstrated. The ADC fabricated in 0.18 µm SiGe BiCMOS technology has a measured analog bandwidth of above 5.6 GHz and Nyquist ENOB of 5.6 bits. The chip integrates with DEMUX, LVDS I/O, offset/gain/clock skew tuning circuits and CMOS controller circuits with SPI interface. The core ADC consumes 4.9 W of power and the whole chip has a die size of 5.0 mm × 5.2 mm (including pads).

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