Hybrid 2D/3D Photonic Integration for Non-Planar Circuit Topologies

Aleksandar Nesic(1,)*, Matthias Blaicher(1,2), Tobias Hoose(1,2), Matthias Lauermann(3), Yasar Kutuvantavida(1,2), Wolfgang Freude(1), Christian Koos(1,2)**

(1) Karlsruhe Institute of Technology (KIT), Institute of Photonics and Quantum Electronics (IPO), Karlsruhe, Germany
(2) Karlsruhe Institute of Technology (KIT), Institute of Microstructure Technology (IMT), Eggenstein-Leopoldshafen, Germany
(3) Now with Infinera Corporation, 140 Caspian Ct., Sunnyvale, California 94089, USA

*aleksandar.nesic@kit.edu, **christian.koos@kit.edu

Abstract We present a concept for realizing crossing-free photonic integrated circuits (PIC) using 3D freeform waveguides. We prove the viability of the approach using a silicon photonic 4 × 4 switch-and-select device. The method is applicable to a wide range of PIC technologies.

Introduction

Photonic integrated circuits (PIC) are often described as the optical analogue of electrical integrated circuits (EIC). However, due to the different natures of light and electricity, some technological problems that are trivial for EIC may present quite a challenge for PIC. For example, complex non-planar circuit topologies often require a large number of crossovers, which can be realized quite easily in EIC by using several conductive layers which are interconnected through vias. PIC design, in contrast, is essentially limited to a single layer, and complex non-planar PIC topologies may require large numbers of planar waveguide crossings (PWC). These PWC lead to signal impairments such as insertion loss, crosstalk, back reflection, or multi-mode excitation. While losses as low as 0.028 ± 0.009 dB and crosstalk of -37 dB at 1550 nm have been reported for optimized high index-contrast silicon photonic PWC with a footprint of 9 × 9 µm², other PIC platforms have lower refractive index contrasts, which makes compact PIC with low loss and low crosstalk difficult. Moreover, for advanced PIC such as the switch-and-select (SAS) switching fabric, the number of PWC can be quite large and non-uniform across different waveguide paths, which is undesirable in particular if strict requirements in terms of crosstalk need to be fulfilled.

In this paper we describe a concept for designing and realizing PWC-free PIC based on three-dimensional (3D) freeform optical waveguides to cross over planar waveguides. The waveguides are realized in-situ by 3D direct laser writing using two-photon polymerization lithography. This technique has previously been used for fabrication of so-called photonic wire bonds that enable low-loss single-mode connections across chip boundaries and is well suited for automated production. In a proof-of-principle experiment, we demonstrate a 4 × 4 SAS device realized in silicon photonics. Moreover, to identify the potential of our approach, we analyze the general case of an m × n SAS switching fabric using graph theory. We show that our approach enables PWC-free implementation by using a number of 3D optical waveguides (3D-WG) that scales as the square root of the number of otherwise required PWC. This result has particular importance for PIC topologies that require a very large number of PWC.

The concept of 3D optical crossovers

The concept of using 3D-WG as crossovers is illustrated in Fig. 1. Fig. 1(a) and (b) show side and top views of a 3D-WG connecting two silicon-on-insulator (SOI) strip waveguides. The top SiO₂ cladding is selectively etched down to the buried oxide (BOX) layer to provide access to inversely tapered SOI strip waveguides that need to be interconnected by the 3D-WG. The 3D-WG is fabricated by direct laser writing and is tapered at its ends to enable low-loss coupling to the SOI waveguides. Fig. 1(c) displays a falsely colored SEM image of two 3D-WG crossovers on our demonstrator device. The positions of the SOI waveguides are automatically detected by machine vision with the help of position markers. The footprint of the 3D-WG amounts to approximately 15 × 160 µm² – more than an order of magnitude smaller than previously demonstrated 3D waveguide crossovers in low index-contrast planar waveguide circuits (PLC).

The PWC-free PIC design principle

For a theoretical analysis of the design approach, we use a SAS switching fabric, and model it with the maximal bipartite graph $K_{m,n}$ consisting of two sets of vertices, where each vertex of the first set (input ports) is connected to each vertex of the second set (output ports). The minimal number of PWC necessary to realize the switch is equal to the crossing number of the associated graph. PIC topologies of different SAS fabrics are depicted in Fig. 2. Two cases must be distinguished: In the first case, waveguides may pass behind the input ports (I₁, I₂, ... Iₘ) or output ports (O₁, O₂, ... Oₙ), Fig. 2(a). This corresponds to an implementation where ports are based on grating couplers on the chip surface. Finding the minimum crossing number $c_{mn}$ and the corresponding topology for such a graph is an NP-complete problem, and up to date, the crossing number formula is only conjectured. The relation is given at the top of Fig. 2(a). Conversely, for butt-coupled fiber interfaces or for fabrics embedded into an on-chip network, waveguides must not pass behind the input ports or the output ports, Fig. 2(b). In this case...
case, the minimum number \( \nu'_{m,n} \) of crossings can be directly calculated along with the optimum topology. Avoiding the PWC by 3D-WG leads to a structure embedded into an on-chip network. The minimum number of required PWC amounts to for the case that waveguides must not pass behind the input ports or the output ports. This corresponds to butt-coupled waveguides bridged by the 3D-WG. The black dashed rectangles denote the areas from which the SiO\(_2\) cladding has been removed. (c) Falsely colored SEM image of the two 3D-WG crossovers on the demonstrator device: Position markers are used to automatically determine the position of SOI waveguide ends, and are not displayed in (a) and (b). The SOI waveguides are covered by the SiO\(_2\) cladding and are invisible on the SEM image.

**Fig. 1:** Concept of 3D optical waveguide (3D-WG) crossovers on the silicon-on-insulator (SOI) platform. (a) Side view, illustrating a polymer 3D-WG, connecting two and crossing over four buried SOI strip waveguides. The SiO\(_2\) cladding has been selectively etched down to the buried oxide (BOX) layer to make the ends of the two SOI strip waveguides accessible. (b) Top view: Both the 3D-WG and the SOI cladding guides are visible. The dashed black rectangles denote the areas from which the SiO\(_2\) cladding has been removed. (c) False-colored SEM image of the two 3D-WG crossovers on the demonstration device: Position markers are used to automatically determine the position of SOI waveguide ends, and are not displayed in (a) and (b). The SOI waveguides are covered by the 3D-WG and are invisible on the SEM image.

**Table 1:** Comparison of the number of needed PWC and 3D-WG for realization of \( n \times n \) SAS switching fabric

| Switch (n x n) | Vertically Coupled | Butt Coupled |
|---------------|--------------------|--------------|
| 4 x 4         | \( \nu_{4,4} \) = 4 | \( \mu_{4,4} = 2 \) |
| 8 x 8         | \( \nu_{8,8} \) = 144 | \( \mu_{8,8} = 18 \) |
| 16 x 16       | \( \nu_{16,16} \) = 3136 | \( \mu_{16,16} = 98 \) |
| 32 x 32       | \( \nu_{32,32} \) = 57600 | \( \mu_{32,32} = 450 \) |
| 64 x 64       | \( \nu_{64,64} \) = 984064 | \( \mu_{64,64} = 1922 \) |

**Experimental demonstration**

For proving the viability of the approach, we use a 4 x 4 switching fabric on the SOI platform based on a topology similar to the one shown in Fig. 2(c). The device contains two 3D-WG, each connecting two SOI strip waveguides. The silicon photonic base structures were fabricated through a commercial foundry using 248 nm optical lithography. For fabrication of the 3D-WG, we used 3D two-photon polymerization lithography. In the SAS structure, each of the four inputs is connected to each of the four outputs by eight 1 x 4 switches, each of which consists of three 1 x 2 switches. Each 1 x 2 switch contains two multi-mode interferers (MMI) couplers and two thermal phase shifters in a balanced Mach-Zehnder modulator (MZM) configuration. In total, the PIC contains 24 1 x 2 switches and 48 thermal phase shifters. The minimum number of drive signals is 16 (two for each of the eight 1 x 4 switches). All phase shifters share a common ground.

We measured transmission spectra for all 16 optical links. To couple light to the chip, we used grating couplers along with a total internal reflection fiber array (TIRFA) at one side, and a single mode fiber (SMF) at the other side. To
waveguide crossings are replaced by 3D freeform realizing non-planar PIC topologies. Planar footprint of the device might be considerably reduced. The results are displayed in Fig. 3(c). In the upper part, blue graphs denote transmission spectra for the 12 links that do not contain 3D-WG, whereas black and red is used for the four links with one 3D-WG. In these measurements, fiber-chip interfaces have already been taken into account by referencing all spectra to the transmission of short SOI waveguide with two grating couplers. For calculating the excess loss of the two 3D-WG bridges, we use a reference transmission spectrum taken through the same output grating coupler, and we consider the length differences of the respective on-chip waveguides. The results are depicted in the lower part of Fig. 3(c); the average losses of the two 3D-WG bridges amount to 3.3 dB and 3.9 dB. These insertion losses are significantly higher than 1.6 dB previously obtained from comparable photonic wire bond structures. This is attributed to a non-optimum waveguide trajectory. We expect that systematic optimization can bring these losses down to approximately 1 dB. Similarly, the rather high on-chip insertion losses of the SOI switch structure (approximately 7 dB at 1550 nm) may be improved. Each path through the switch contains 8 MMI splitters, 4 thermal phase shifters, and up to 6.2 mm of SOI strip waveguides. Assuming optimized devices with MZM insertion losses of 0.33 dB, waveguide propagation losses of 0.6 dB/cm, and reduced waveguide lengths of less than 3 mm, we expect on-chip insertion losses of less than 2 dB for the SOI waveguide structures. Moreover, by using ultra-compact 2 × 2 switching cells based on liquid-crystal phase shifters, the footprint of the device might be considerably reduced.

**Summary**

We have introduced a concept for designing and realizing non-planar PIC topologies. Planar waveguide crossings are replaced by 3D freeform waveguides. In a proof-of-principle experiment, we have demonstrated the viability of the approach using a silicon photonic 4 × 4 switch-and-select (SAS) structure. We further perform a theoretical analysis that shows that the hybrid 2D/3D concept has clear advantages in terms of scalability to port-count SAS switch structures. The design method is independent from the underlying PIC technologies. We believe that the results pave the way towards highly complex non-planar PIC.

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**References**

[1] Y. Ma et al., “Ultralow loss single layer submicron silicon waveguide crossing for SOI optical interconnect,” Opt. Express, Vol. 21, no. 24, p. 29374 (2013).
[2] L. Chen et al., “Compact low-loss and low-power 8×8 broadband silicon optical switch,” Opt. Express, Vol. 20, no. 17, p. 18977 (2012).
[3] M. Deubel et al., “Direct laser writing of three-dimensional photonic-crystal templates for telecommunications,” Nat. Mater., Vol. 3, no. 7, p. 444 (2004).
[4] N. Lindenmann et al., “Photonic wire bonding: a novel concept for chip-scale interconnects,” Opt. Express, Vol. 20, no. 16, p. 17667 (2012).
[5] N. Lindenmann et al., “Connecting Silicon Photonic Circuits to Multi-Core Fibers by Photonic Wire Bonding,” J. Lightwave Technol., Vol. 33, no. 4, p. 755 (2015).
[6] Y. Nasu et al., “Waveguide Interconnection in Silica-Based Planar Lightwave Circuit Using Femtosecond Laser,” J. Lightwave Technol., Vol. 27, no. 18, p. 4033 (2009).
[7] K. Watanabe et al., “Low-loss three-dimensional waveguide crossing using adiabatic interlayer coupling,” Electronics Letters, Vol. 44, no. 23, p. 1536 (2008).
[8] M. R. Garey et al., “Crossing number is NP-complete,” SIAM Journal on Algebraic and Discrete Methods, Vol. 4, no. 3, p. 312 (1983).
[9] R. K. Guy, “Crossing number of graphs,” Lecture Notes in Math., Vol. 303, p. 111, Springer Berlin Heidelberg (1972).
[10] A. Nesic et al., “Graph Models and Algorithms for Designing Photonic Integrated Switches,” publication in preparation.
[11] C. Galland et al., “CMOS-compatible silicon photonic platform for high-speed integrated opto-electronics,” Proc. SPIE, Vol. 8767 (2013).
[12] J. Pfeifle et al., “Silicon-organic hybrid phase shifter based on a slot waveguide with a liquid-crystal cladding,” Opt. Express, Vol. 20, no. 14, p. 15359 (2012).