Construction of Sziklai Pair using Mixed Components

Ramendra Singh, Ankit Tripathi, Vartika Anand
Associate Professor, Dept. of ECE, IPEC Ghaziabad, Assistant Professor, Dept. of ECE, RKGIT Ghaziabad, Assistant Professor, Dept. of ECE, RKGIT Ghaziabad, India.

ABSTRACT: To design Sziklai pair topology for small-signal amplifier circuit with RC coupled voltage divider bias, both BJT and JFET are used. Such a design amplifier circuit can be tuned in the frequency range of 108Hz-620 KHz. The circuit proposed in this paper can amplify audio range signal excursions swinging in the range of 0.1-12mV at 1KHz. Features like high voltage gain, current gain greater than unity, wider bandwidth and considerably low harmonic distortion makes this amplifier superior than earlier announced small-signal Sziklai pair amplifier. Various applications for this proposed amplifier is in Radio/TV receivers, low frequency power sources and other audible range communication applications.

Keywords: RC coupled amplifier, High voltage gain, current gain, harmonic distortion.

1. INTRODUCTION

Sziklai pair amplifier contains two opposite polarity BJTs in its configuration [1][2]. Due to small amount of in-built negative feedback, the current gain factor of Sziklai pair ($s_A = \frac{Q_1 Q_2^+ Q_1}{Q_2}$) is slightly less than Darlington pair ($s_{Dar} = \frac{Q_1 Q_2^+ Q_1^+ Q_2}{Q_2}$) topology but at higher ($>100$) both are approximated to $\frac{Q_1 Q_2}{Q_2}$ [1]-[3]. Both the paired units are often compared due to almost identical ranges of input resistance, output resistance, current gain and voltage gain but possess several disparities in qualitative features [2]. Sziklai pairs hold better linearity, higher switching speed, wider bandwidth and moreover its base turn-on-voltage is only half of Darlington pair [2].

Despite of having many superior qualitative features, Sziklai pairs are usually used in the output stage of push–pull power amplifiers in electronics industry [4]-[5]. Its use in small-signal amplifiers is still to be authenticated and thus is a challenging topic of research [5]-[8]. Contrarily, author's research group recently proposed a model of PNP driven small-signal Sziklai pair amplifier which produces high voltage gain, overcomes the problem of poor response of small-signal Darlington pair amplifier at higher frequency but shows narrow-band frequency response [5],[9]-[10].

The present study is focused around a Sziklai pair which uses PNP transistor at driver stage and N-channel JFET at follower stage. Proposed model of Sziklai pair with appropriate biasing components successfully removes the shortcomings of PNP driven Sziklai pair and is explored as new circuit model of a small-signal amplifier suitable for radio-TV receiver stages and low frequency power sources.
2. CIRCUIT DETAILS

The Proposed circuit of the small-signal amplifier (Fig.1.1) uses a PNP driver transistor (Q2N2907A with =231.7) and N Channel JFET (J2N4393 with \( V_T = -1.422 \)) at follower position in Sziklai pair topology [2],[6]. This is Required for DC bias to established with an additional biasing resistance \( R_A \) and other suitable passive biasing components using potential divider biasing methodology [3], [12].

The simulation is done by PSpice to carry present investigations [13]. The Qualitative performance of the circuit is observed with 1V, 1KHz AC input signal source. Observations are listed for 1mV, 1KHz input signal but the proposed amplifier may produce useful results for 0.1-12mV AC input at 1KHz.

![Fig.1.1. Sziklai pair topology with BJT-JFET hybrid](image)
3. RESULTS AND DISCUSSIONS

![Variation of Maximum voltage gain as a function of frequency](image)

Variation of voltage gain as a function of frequency for both the amplifiers under discussion is depicted in Fig.1.2. Response curves in Fig.1.2 clearly indicate that the proposed amplifier comes up with considerably wider bandwidth than reference circuit with enhanced voltage gain. The Proposed circuit produces enhanced voltage gain, wider bandwidth, reduced current gain and considerably lower THD than PNP Sziklai pair amplifier [5]. In addition, proposed amplifier is found free from poor-response-problem of small-signal Darlington’s amplifier [9]-[10] at higher frequencies and narrow bandwidth restrictions of PNP driven Sziklai pair amplifier [5]. The possible use of the proposed circuit can be established in designing cascadable gain blocks for receivers and 108Hz-505KHz frequency range power sources with observed status of $A_{VG}$ and $A_{IG}$ (both are greater than unity).

The Small-signal AC equivalent circuit of proposed amplifier is drawn in Fig.1.3. Based on simulation results, BJT of the Sziklai unit consists base-emitter resistance $r_{be}=37.7\,\Omega$, collector-emitter resistance $r_{ce}=825\,\Omega$, AC current gain factor $\beta=184$ whereas JFET consists $g_{m}=1.33\times10^{-4}$, drain-source resistance $r_{d}=0.30\times10^{-3}$. Also, $I_b$ is the base current of BJT and $R_B=R_1\parallel R_2$.

![Small-signal AC equivalent of the Proposed Sziklai pair amplifier with BJT-JFET](image)
Applying KCL at C3

\[ \frac{-V_c}{r_c} = \frac{V_c}{r_a} + V_g \cdot g_m \quad \text{where:} \quad R_c = R_E \ || \ R_L \]

\[-V_o \left( \frac{1}{R_c} + \frac{1}{r_a} \right) = V_g \cdot g_m \]

\[ l_3 + l_4 + l_5 = 0 \]

\[ \frac{V_o}{R_A} + \frac{V_o}{r_c} + \beta t_L = 0 \]

\[ V_o = \frac{-\beta t_L}{\left( \frac{1}{R_c} + \frac{1}{r_a} \right)} \]

\[ A_c = V_i = r_t \cdot t_L \]

\[ V_o = \frac{V_o \cdot g_m}{r_t \left( \frac{1}{R_c} + \frac{1}{r_a} \right) \left( \frac{1}{R_A} + \frac{1}{r_c} \right)} \]

Small-signal AC voltage gain of the proposed amplifier (based on Fig.6.3) can be expressed as following –

\[ A_V = \frac{-\beta g_m}{r_t \left( \frac{1}{R_c} + \frac{1}{r_a} \right) \left( \frac{1}{R_A} + \frac{1}{r_c} \right)} \approx \frac{-\beta g_m R_A}{r_t \left( \frac{1}{R_E} + \frac{1}{r_a} \right)} \]

However, small-signal AC current gain can be deduced as –

\[ A_I = \frac{-\beta g_m}{R_E \cdot r_t \left( \frac{1}{R_c} + \frac{1}{r_a} \right) \left( \frac{1}{R_A} + \frac{1}{r_c} \right) \left( \frac{1}{R_E} + \frac{1}{r_a} \right) \left( \frac{1}{R_A} + \frac{1}{r_c} \right)} \approx \frac{-\beta g_m R_A}{r_t \left( \frac{1}{R_E} + \frac{1}{r_a} \right) \left( \frac{1}{R_A} + \frac{1}{r_c} \right)} \]

Negative sign in the expression shows phase reversal of the output voltage [3].

Here it is noteworthy that the presence of additional resistance R_A is essential for biasing in proposed circuit-topology to retain the observed performance. The absense of R_A causes voltage and current gains of the amplifier to dip below unity for any biasing combination [5]-[6]. The corresponding Equations to A_V and A_I also vaerifies this fact due their strong dependency on R_A. Moreover, the permissible range of R_A for proposed amplifier to show meaningful response is 37 \(<R_A<100\).
Refer temperature dependency of various performance parameters of the circuit under discussion. $A_{VG}$ and $A_{IG}$ simultaneously go high but bandwidth goes down with rising temperature up to a critical limit of 38°C. Values of various performance parameters at –30°C temperature are reported to be $A_{VG}$=89.64, $A_{IG}$=1.26, $B_W=812.11$KHz, THD=0.905%, $a_c=145$ $r_+ =30.7$Ω, $g_m=1.76x10^{-4}$ and $r_d=105.34$ whereas at critical temperature 38°C these are observed to be $A_{VG}$=108.08, $A_{IG}$=1.60, $B_W=358.17$KHz, THD=0.855%, $a_c=191$ $r_+ =39$Ω, $g_m=1.26x10^{-4}$ and $r_d=472.80$. However beyond critical temperature both variety of gains gradually fall and make the amplifier purposeless after 45°C. This causes enhancement in $A_{VG}$ and $A_{IG}$. But, after critical temperature, the collision rate of majority carriers with remaining ions in semiconductor channel enhances and causes an effective decrement in their mobility [14]. This decreases the drain current of the JFET based Sziklai pair system and therefore the effective current and voltage gain of the proposed amplifier.

### I: Variation of $A_{VG}$, $A_{IG}$ and $B_W$ with Temperature

| Temp (°C) | $A_{VG}$ | $A_{IG}$ | $B_W$ (KHz) | $A_{VG}$ | $A_{IG}$ | $B_W$ (KHz) |
|-----------|----------|----------|-------------|----------|----------|-------------|
| –30       | 83.45    | 5.74     | 4.73        | 89.64    | 1.26     | 812.11      |
| –10       | 90.46    | 6.31     | 4.76        | 99.69    | 1.36     | 731.89      |
| 0         | 93.70    | 6.59     | 4.78        | 98.52    | 1.42     | 759.49      |
| 5         | 96.96    | 6.87     | 4.79        | 101.18   | 1.47     | 610.84      |
| 10        | 102.11   | 7.34     | 4.80        | 105.53   | 1.53     | 550.24      |
| 15        | 103.22   | 7.42     | 4.80        | 106.77   | 1.57     | 486.66      |
| 20        | 106.13   | 7.64     | 4.80        | 108.08   | 1.61     | 353.39      |
| 25        | 107.65   | 7.82     | 4.80        | 109.42   | 1.63     | 332.14      |
| 30        | 108.12   | 7.96     | 4.81        | 110.03   | 1.65     | 345.71      |

Refer noise analysis of the proposed circuit [13]. Both Input and output noises in the proposed circuit are found considerably low and within the permissible range for small-signal amplifiers. However, output noise (approximate range $10^{-7}$ V/Hz) is observed to be higher than input noise (approximate range $10^{-9}$ V/Hz) at various operating frequency between 100Hz to 1MHz. Moreover, the output noise significantly reduces at elevated temperatures (e.g. 20°C increase in temperature forces output noise to reduce from approximately $10^{-7}$ V/Hz to $10^{-8}$ V/Hz range) [5].

Following the usual track of behavior of small-signal amplifiers, the proposed circuit shows considerable response in reference to the various biasing parameters [5]-[7],[12]. Refer input biasing resistance $R_{SS}$. $A_{VG}$ of the amplifier receives maximum (270.621) at $R_{SS}=10$ and minimum (1.55) at $R_{SS}=10K$ with meaningful amplification in 10 <$R_{SS}$<10K range [7]. Similarly, $A_{VG}$ rises almost linearly with increasing values of drain-emitter resistance $R_{ED}$ up to 20K and beyond this critical limit it gradually acquires a saturation tendency [7],[14]. However, $A_{VG}$ increases non-linearly with source resistance $R_s$, reaches maximum ($A_{VG}=106.021$) at $R_s=10K$, thereafter starts decreasing but the amplifier shows purposeful response in 100 <$R_s$<75K range [7],[12].

Moreover, the hybrid Sziklai pair unit switches-ON at 3V with a fruitful response range of $V_{CC}$ in 3-30V [14]. Correspondingly, $A_{VG}$ rises gradually with increasing values of $V_{CC}$ up to 15V and thereafter falls almost linearly $C_S$ and $C_L$ controls only upper cut-off-frequency $f_H$ of the amplifier and their proper adjustment lead to a tuning which finally ascertain the frequency response of proposed amplifier to peak around a desired frequency [15].
4. CONCLUSIONS

An ideal condition is that a small-signal amplifier is designed using hybrid combination of BJT and JFET in Sziklai pair topology. The Proposed circuit successfully amplifies audio range signal excursions swinging between 0.1-12mV range at 1KHz. High voltage gain (105.552), current gain greater than unity (1.5574), wider bandwidth 505.356 KHz bandwidth and considerably low harmonic distortion (0.89%) are the prime features of this amplifier. This proposed amplifier circuit can be tuned in 108Hz-620 KHz frequency range. Presence of additional biasing resistance $R_A$ is the essential in the proposed circuit to maintain amplification property. There are various qualitative features and small-signal AC analysis of the proposed amplifier suggests its suitability to use in Radio/TV receivers, low frequency power sources and other audible range communication applications.

REFERENCES

[1] George C. Sziklai, *Push-pull complementary type transistor amplifier.*, U.S. Patent 2,762,870, September 11, 1956

[2] Rod Elliott, *Compound pair Vs Darlington pair*, http://sound.westhost.com/articles/cmpd-vs-darl.htm, January 6, 2011

[3] R. L. Boylestad and L. Nashelsky, *Electronic Devices and Circuit Theory*, Pearson Education Asia, 9th ed., 2008, p-641

[4] George C. Sziklai, *Power Amplifiers*, U.S. Patent 2,985,841, May 23, 1961

[5] B. Pandey, S. Srivastava, S. N. Tiwari, J. Singh and S. N. Shukla, *Qualitative Analysis of Small Signal Modified Sziklai Pair Amplifier*, Indian Journal of Pure and Applied Physics, 50, 2012, p-272

[6] S.N. Shukla, B. Pandey and S. Srivastava, *Qualitative Study of a New Circuit Model of Small-signal Amplifier using Sziklai pair in Compound Configuration*, Procd. IEEE-ICSE2012 (Proceedings of 10th IEEE International Conference on Semiconductor Electronics, September 19-21, 2012, Kuala Lumpur), p-600

[7] S.N. Shukla, S. Srivastava, *A New Circuit Model of Small-signal Sziklai pair amplifier*, International Journal of Applied Physics and Mathematics, Vol.3, No.4, July 2013, p-231

[8] S.N. Shukla, B. Pandey, *Two-Stage Small-Signal Amplifier with Darlington and Sziklai pairs*, Procd. IEEE-ICSE-2014 (Proceedings of 11th IEEE International Conference on Semiconductor Electronics, August 27-29, 2014, Kuala Lumpur), (ISBN 978-1-4799-5759-0), IEEE-Xplore, August 2014, p-13

[9] David A. Hodges, *Darlington’s Contribution to Transistor Circuit Design*, IEEE Transactions on Circuits and Systems-I, Vol.46, No.-1, January 1999, p-102

[10] A. M. H. Sayed ElAhl, M. M. E. Fahmi, S. N. Mohammad, *Qualitative analysis of high frequency performance of modified Darlington pair*, Solid State Electronics, 46, 2002, p-593

[11] M.H. Ali, Aliyu Sisa Aminu, *Analysis of Darlington pair in Distributed Amplifier Circuit*, IOSR Jornal of Electrical and Electronics Engineering, Vol.10, Issue 2, Ver.I, 2015, p-77
[12] S. N. Tiwari, A. K. Dwivedi and S. N. Shukla, *Qualitative Analysis of Modified Darlington Amplifier*, Journal of Ultra Scientist of Physical Sciences, 20 No.3, 2008, p-625

[13] M. H. Rashid, *Introduction to PSpice Using OrCAD for Circuits and Electronics*, Pearson Education, 3rd Ed., 2004, p-255

[14] S.N. Shukla, S. Srivastava, *A New Circuit Model of Small-signal Amplifier using JFETs in Darlington pair Configuration*, International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol.2, Issue 4, April 2013, p-1554

[15] A. Motayed and S.N. Mohammad, *Tuned Performance of Small-signal BJT Darlington pair*, Solid State Electronics, Vol. 45, p.p. 369-371, 2001.

Dr. Ramendra Singh is currently working as Associate Professor in IPEC, Ghaziabad. He has completed his Ph.D from Dr. R.M.L. Avadh University, Faizabad, in August 2016 on the topic “Development, Modification and Analysis of Small-signal BJT Amplifiers through PSpice”. His M.Tech is in Digital Electronics & Systems from KNIT, Sultanpur in 2008. He has teaching experience of more than 15 years. He has published papers in 2 international journals & 2 international conferences.

Mr. Ankit Tripathi is currently working as Assistant Professor in RKGIT, Ghaziabad. His M.Tech is in Digital Electronics & Systems from KNIT, Sultanpur in 2011 and B. Tech (Hons.) in ECE from Dr. R.M.L. Avadh University, Faizabad in 2007. He has teaching experience of more than 9 years. He has published papers in 4 international journals & 4 international conferences.

Ms. Vartika Anand is currently working as Assistant Professor in RKGIT, Ghaziabad. Her M.Tech is in Electronics & Communication Engineering from Amity University, Noida in 2013 and B. Tech (ECE) from U.P.T.U. in 2008. She has teaching experience of more than 8 years. She has published papers in 2 international journals & 1 international conference.