A Cost-Effective Design of Reversible Programmable Logic Array

Abstract

In the recent era, Reversible computing is a growing field having applications in nanotechnology, optical information processing, quantum networks etc. In this paper, the authors show the design of a cost effective reversible programmable logic array using VHDL. It is simulated on Xilinx ISE 8. 2i and results are shown. The proposed reversible Programming logic array called RPLA is designed by MUX gate & Feynman gate for 3- inputs, which is able to perform any reversible 3- input logic function or Boolean function. Furthermore the quantized analysis with comparative finding is shown for the realized RPLA against the existing one. The result shows improvement in the quantum cost and total logical calculation in proposed RPLA.

References

- R. Landauer, "Irreversibility and heat generation in the computational process", IBM J. Res. Develop., vol. 5, pp. 183-191, 1961
- C. H. Bennet, "Logical reversibility of computation", IBM J. Res. Develop., vol. 17, no. 6, pp. 525-532, 1973.
- T. Toffoli, "Reversible Computing", Tech memo MIT/LCS/TM-151, MIT Lab for computer science 1980.
- E. Fredkin and T. Toffoli, "Conservative logic", Int J. Theoretical
A Cost-Effective Design of Reversible Programmable Logic Array

Physics, Vol. 11, pp. 219-253, 1985
- R. Feynman, "Quantum Mechanical Computers," Optics News, Vol.11-20, 1985.
- Peres, "Reversible logics and quantum computers," Physical review A, 32: 3266-3276, 1985.
- Ahsan Raja Chowdhury, Rumana Nazmul, Hafiz Md. Hasan Babu, "A new approach to synthesis multiple-output functions using reversible programmable logic array," proceedings of the 19th international conference on VLSI design, 1063-9667, 2006.
- Matthew Moisin and Nagarajan Ranganathan, "Design of a reversible ALU based on a novel programmable reversible logic gates," Physical review A, 32: 3266-3276, 1985.
- Abul Sadat Md. Sayem and Sajib Kumar Mitra, "Efficient approach to design low power reversible logic blocks for field programmable gate arrays," 978-114244-8728-8/11/IEEE 2011.
- H. R. Bhagyalakshmi, M. K. Venkeatesha, "An improved design of a multiplier using reversible logic gates," International journal of engineering science and technology, vol. 2 (8), pp. 3838-3845, 2010.
- G. De Mey and A. De Vos, "The minimum energy for a one bit commutation: a proof of the Landauer limit," proc. 26th international conf. On microelectronics IEEE, 2008.
- Michael P. Frank, "Introduction to reversible computing: motivation, progress, and challenges," proceedings of 2nd international conference on computing frontiers ACM Newyork, 2005.
- Saurabh Sahni, Ankur Bakshi, "Reversible computing: looking ahead of the curve," www.it.iitb.ac.in/~saurabh/documents/revpaper.pdf
- Mjih Haghparast, Mazid Mohammadi, Keivan Navi, "Optimized reversible multiplier circuit," Journal of circuits, systems and computers.
- J. Bhasker, "A VHDL Primer," Third edition, Pearson education.

Index Terms

Computer Science
Integrated Circuits

Keywords
Garbage Outputs Quantum Cost Reversible Gate Reversible Programming Logic Array
Vhdl