Article
A TCAD Study on High-Voltage Superjunction LDMOS with Variable-K Dielectric Trench

Zhen Cao *, Qi Sun, Hongwei Zhang, Qian Wang, Chuanfeng Ma and Licheng Jiao

School of Artificial Intelligence, Xidian University, Xi’an 710071, China; qi_sun0328@163.com (Q.S.); zhw2813532830@163.com (H.Z.); wangq_amber@163.com (Q.W.); machuanfeng1021@163.com (C.M.); lchjiao@mail.xidian.edu.cn (L.J.)
* Correspondence: icaozhen@163.com

Abstract: In this paper, a novel high voltage superjunction lateral double diffused MOSFETs (SJ-LDMOS) using a variable high permittivity (VHK) dielectric trench is presented. A relatively high HK dielectric is in the upper trench, which is connected with the drain electrode to suppress the high electric field (E-field) peak under the drain by the dielectric reduced surface field (RESURF) effect. In addition, a relatively low HK dielectric is at the bottom of the trench. On the one hand, the substrate is effectively depleted by a suitable HK dielectric layer, and the vertical depletion region of the substrate is greatly expanded. On the other hand, the overall vertical bulk E-field distribution is modulated by the E-field peaks generated at the position of varying K dielectric. A more uniform bulk E-field distribution is obtained for VHK SJ-LDMOS, leading to a high breakdown voltage (BV). Compared to the conventional SJ-LDMOS, the blocking voltage per micron of the drift region of VHK SJ-LDMOS has increased by 41.2%. Besides, compared with the SJ-LDMOS with a uniform-K, the BV of VHK SJ-LDMOS is improved by about 9.5%. The condition of the optimal range of the variable high permittivity is also presented. Meanwhile, the proposed VHK SJ-LDMOS has good conduction characteristics and heat dissipation.

Keywords: superjunction; LDMOS; electric field modulation; dielectric RESURF; breakdown voltage

1. Introduction
Superjunction (SJ) power devices can achieve remarkable low on-resistance while achieving high breakdown voltage (BV), breaking the traditional MOSFET silicon limit [1,2]. Lateral double-diffused MOSFETs (LDMOS) using SJ technology (SJ-LDMOS) may be the key element in high voltage (700 V-class) power integrated circuits (PIC) [3,4]. For the purpose of avoiding costly SOI (silicon on insulator) and DI (dielectric isolation) substrate, the bulk silicon SJ-LDMOS with good heat dissipation was developed. To eliminate the substrate assisted depletion effect and improve the performance of SJ-LDMOS, several structures have been reported [5–8]. However, the performance of these devices is still affected by the curvature effect of the N+ drain diffusion and the uneven bulk electric field (E-field) distribution [9,10], which causes the problem that the BV of SJ-LDMOS is prone to saturation as the drift region length (L_D) increases (L_D ≥ 40 µm). Thus, the blocking voltage per micron of the drift region (~13 V/µm) is far less than that of the theoretical value of the silicon drift region for charge-coupled structures (~20 V/µm) [11,12].

In order to optimize the bulk E-field distribution and further improve the trade-off between BV and R_on,sp, we propose a novel SJ-LDMOS (Figure 1b) with a deep trench filled with variable high permittivity (VHK) dielectric under the N+ drain, to suppress the bulk peak E-Field around the edge of the drain diffusion and improve the overall E-field distributions. The main idea of the proposed VHK SJ-LDMOS is to further improve BV by the bulk E-field modulation provide b + -y the VHK dielectric trench. Simulation results show that the blocking voltage per micron of the drift region of VHK SJ-LDMOS has increased by 41.2%, compared with that of the conventional one. Besides, the proposed VHK SJ-LDMOS...
has good conduction characteristics and heat dissipation. The main physics models are
applied to the Sentaurus TCAD simulation, including Mobility (DopingDep High Field
satEnormal), EffectiveIntrinsicDensity (OldSlotboom), Recombination (SRH (DopingDep)
and eAvalanche (CarrierTempDrive)). The criterion of breakdown is BreaCriteria [Current
(Contact = “drain” Absval = 1.0 × 10−7 A]). The main solving model is Coupled [Poisson
Electron Hole].

Figure 1. Three-dimensional view of (a) conventional SJ-LDMOS and (b) VHK SJ-LDMOS.

2. Device Structure and Mechanism

The schematic three-dimensional structure of the proposed VHK-SJ-LDMOS and the
conventional SJ-LDMOS structure is shown in Figure 1. The main feature of the proposed
VHK-SJ-LDMOS structure is with VHK dielectric trench under the N+ drain. According
to the principle of dielectric reduced surface field (RESURF), the VHK dielectric layer is
designed according to different concentrations of N+ drain, N-buffer layer and P-substrate.
In this instance, Pb (ZrxAi1−x) O3 (PZT) is used to form the HK region due to its high
enough permittivity without a complex process [13–16]. The process flow is the same
as the conventional N-buffer SJ-LDMOS except for the implantation of the VHK trench
under the drain region. A relatively high HK dielectric (HK1) in the upper trench, which is
connected with the drain electrode to suppress the high E-field peak under the drain by the
dielectric RESURF [17]. In addition, a relatively low HK dielectric (HK2) compared with
the upper HK dielectric is at the bottom of the trench. In this paper, 3-D device simulations
are conducted at room temperature. The key parameters of the optimized SJ-LDMOS
structures used in the simulation are all listed in Table 1.

Table 1. Device parameters in the simulation.

| Symbol   | Description               | VHK SJ-LDMOS | Cov. SJ-LDMOS |
|----------|---------------------------|--------------|---------------|
| W_N, W_P | N, P drift width (μm)     | 1.0          | 1.0           |
| T_SJ     | SJ layer thickness (μm)   | 2.0          | 2.0           |
| T_B      | Buffer layer thickness (μm)| 3.0         | 3.0           |
| L_GP, L_DP| Gate, drain poly FP length (μm)| 3.0, 2.0   | 3.0, 2.0     |
| t_OX, t_FOX| Gate, field oxide thickness (μm)| 0.04, 0.8   | 0.04, 0.8   |
| L_C      | Channel length (μm)       | 1.5          | 1.5           |
| L_D      | Drift length (μm)         | 30–90        | 30–90        |
| N_S      | Substrate doping (cm−3)   | 1.0–3.0 × 1014| 1.0–2.0 × 1014|
| N_D, N_A | N, P drift doping (cm−3)  | 5.0 × 1016   | 5.0 × 1016   |
| N_B      | Buffer layer doping (cm−3)| 4.0 × 1015   | 3.0 × 1015   |
| K        | K dielectric values (ε_K/ε_0)| PZT (100–400)| –             |
| T_HK     | HK trench depth (μm)      | 30–50        | –             |
| W_HK     | HK trench width (μm)      | 5–8          | –             |
Figure 2 shows the schematic cross-section view and E-field component profiles of VHK SJ-LDMOS. In the off-state, the composite layer of HK and semiconductor under the drain jointly sustains the vertical bias voltage \((V_R)\) of the VHK SJ-LDMOS, which can be qualitatively considered as a semiconductor with an equivalent permittivity of \((\varepsilon_{Si} + \varepsilon_{HK})\). The Variable-K pillar beside the substrate, the drain electrode/VHK/oxide/Si structure can be treated as a metal-insulator-semiconductor (MIS) capacitance [14,15], which makes it easier to deplete a higher \(N_S\) (allowing for a lower resistivity substrate) and a higher \(N_B\) by the assisted depletion effect to decrease \(R_{ON,sp}\).

According to the Poisson equation and dielectric RESURF [17–20], the vertical E-field component \((E_{Si,y})\) is modified by the effective doping concentration \(N_{eff}\) of semiconductor, which can be expressed as

\[
\frac{\partial E_{Si,y}}{\partial y} = \frac{qN_{ID}}{\varepsilon_{Si}} - \frac{2V_R W_{HK} \varepsilon_{HK}}{\varepsilon_{Si} r_y^2} W_{Si} = \frac{qN_{eff}}{\varepsilon_{Si}}
\]

(1)

where \(r_y\) is the depth of the vertical depletion region. \(W_{Si}\) and \(W_{HK}\) are the widths of the semiconductor and HK dielectric, respectively. In order to obtain a uniform vertical electric field, HK trench layers with different dielectric constants are designed according to the semiconductor doping concentration under the drain. The doping concentration of the N+ pillar junction and the N-type buffer layer near the drain end is high, and there is a junction curvature effect, thus a relatively high dielectric layer is needed at the top of the trench to weaken the peak electric field under the drain. However, the doping concentration of the substrate is low, thus a relatively low HK dielectric is at the bottom of the trench. Additionally, because of the change of the K value, a new electric field peak appears to modulate the vertical electric field of the device, thereby achieving the purpose of optimizing the vertical electric field distribution of the device. Under the conditions of the avalanche breakdown, the theoretical \(BV\) of VHK SJ-LDMOS is obtained by the integral of the lateral and vertical E-field component as

\[
BV \approx \text{Min} \left[ \int_0^{r_D} E_{Si,x} \, dx \left( \int_0^{T_{HK1}} |E_{Si,y1}| \, dy + \int_{T_{HK1}}^{T_{HK2}} |E_{Si,y2}| \, dy + \int_{T_{HK2}}^{T_{PK}} |E_{Si,y3}| \, dy \right) \right]
\]

(2)
3. Results and Discussion

3.1. Off-State Characteristics

In Figure 3a, TCAD simulation is calibrated to experimental breakdown characteristics (Ids-Vds) data extracted from N-Buffer SJ-LDMOS [6] and Junction-Isolated Triple RESURF (JITR) LDMOS [3]. With one set of self-consistent parameters, the TCAD simulation results and the experimental data are well matched. Figure 3a shows the simulated breakdown curve of VHK SJ-LDMOS and conventional SJ-LDMOS. Compared to conventional SJ-LDMOS (553 V), the BV of VHK SJ-LDMOS (781 V) is significantly improved by about 41.2% with a low leakage current. Besides, compared with the SJ-LDMOS with a uniform-K (713 V) [16], the BV of VHK SJ-LDMOS is improved by about 9.5%. This is due to the improved vertical E-field distribution of VHK TR LDMOS, which is modulated by the E-field peaks generated at the K variable position and the bottom of the VHK dielectric trench. Thus, the proposed VHK SJ-LDMOS can obtain a higher voltage than the conventional SJ-LDMOS and the SJ-LDMOS with a uniform-K. In Figure 3b, the equipotential contours of VHK SJ-LDMOS are more evenly spaced and the depletion area extends deeper (77 μm) than that of the conventional SJ-LDMOS (49 μm). The P-substrate is completely depleted by the VHK dielectric trench to obtain a much higher BV at the same drift length.
In Figure 4a, when the lateral E-field is optimized to a very uniform degree by RESURF and field modulation technology, etc., the BV does not increase as the LD increases. At this time, in order to further improve BV, the vertical bulk E-field of the device needs further optimization. Figure 4b shows the vertical E-field distribution near the drain end (at X = 44.99 μm). The high E-field peak (E_PK) generated by the curvature effect of the N+ drain diffusion is effectively suppressed by the relatively high HK dielectric layer in the upper trench. Meanwhile, new E-field peaks (E_PK′ and E_PK″) brought about by varying HK dielectric greatly improve the vertical E-field distributions.

Figure 5a shows the dependence of vertical E-field distributions and BV on different K values. Compared to a uniform HK dielectric-filled trench, VHK structure with suitable K combination (K_1 = 300 ε_0 and K_2 = 100 ε_0) has more uniform bulk E-field distributions, thus a higher BV is obtained. The dependences of BV on different ratios of T_HK1 to (T_HK1 + T_HK2) with three different L_SJ (40 μm, 60 μm and 80 μm) are shown in Figure 5b. For a certain W_HK, K_1 and K_2, there is an optimal value of T_HK1 / (T_HK1 + T_HK2) = 1/2 to achieve optimal performance. The dependences of BV on different ratios of K_1 to K_2 with different K_1 values are shown in Figure 5c. At the condition of the optimal range of K_1 / K_2, a higher BV is obtained. The optimal range is 200 < K < 400. Pb (Zr_{0.51–x} Ti_{x}) O_3 (PZT) is a good candidate to realize the high relative permittivity because PZT is easy to etch and can achieve the optimal K values without complex processing. Figure 5d shows the dependences of BV on different ratios of W_HK to (T_HK1 + T_HK2) at different K values and L_SJ. The optimal ratios of W_HK to (T_HK1 + T_HK2) of VHK SJ-LDMOS to ensure that the vertical depletion depth spreading in the substrate, to obtain an optimized BV by the reshaping effect of the HK trench enhanced the vertical electric field strength in the substrate.

3.2. ON-State Characteristics

Figure 6a shows the output characteristics of the conventional SJ-LDMOS and VHK-MOSFET. The V_{TH} (threshold voltage) are both about 2.0 V. At different gate voltages, V_G, the VHK-MOSFET has a higher BV than that of the conventional SJ-LDMOS due to the uniform electric field distribution. The dependences of BV, R_{ON,sp} and figure-of-merit (FOM = BV^2 / R_{ON,sp}) on LD for VHK SJ-LDMOS and the conventional SJ-LDMOS are shown in Figure 6b. It is found that the BV of VHK SJ-LDMOS increases faster and saturates at a longer L_D as the L_D increases (BV > 700 V at L_D = 40 μm).
The thermodynamic transport model, a thermal contact that coincides with a substrate electrode is defined. The keyword hydrodynamic (eTemperature) is specified in the global physics section to activate the hydrodynamic model in TCAD simulation. For the thermal Onset characteristics, the BV dependence of temperature is calculated. For temperature distribution simulations with a non-zero thermal resistance, a thermal contact that coincides with a substrate electrode is defined. The keyword hydrodynamic (eTemperature) is specified in the global physics section to activate the hydrodynamic model in TCAD simulation. For the thermal limits of VHK SJ-LDMOS and conventional SJ-LDMOS, the BV of VHK SJ-LDMOS increases faster and saturates at a longer LD as the LD increases (BV > 700 V at LD = 40 μm).

Temperature distributions in the conventional SJ-LDMOS and VHK SJ-LDMOS are shown in Figure 7a, by S-device simulation. For temperature distribution simulations with the thermodynamic transport model, a thermal contact that coincides with a substrate electrode is defined. The keyword hydrodynamic (eTemperature) is specified in the global physics section to activate the hydrodynamic model in TCAD simulation. For the thermal limits of VHK SJ-LDMOS and conventional SJ-LDMOS, the BV of VHK SJ-LDMOS increases faster and saturates at a longer LD as the LD increases (BV > 700 V at LD = 40 μm).

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contact, a temperature (300 K) is declared. The contact is attached by a thermal resistor with value $5 \times 10^{-4} \text{ cm}^2 \text{K/W}$. A non-zero thermal resistance may be used to emulate heat exchanges of the device with the outside environment. It can be seen from the results that although the high current leads to the temperature of the two devices increasing, the two devices can still work normally with good ruggedness. Figure 7b shows the $R_{\text{on,sp}}$ versus BV for VHK SJ-LDMOS and other existing SJ-LDMOS. As can be seen, VHK SJ-LDMOS exhibits better performance at the BV region (400–1200 V), which is close to the lateral SJ silicon limit under the optimized conditions [21].

![Temperature distributions in the conventional SJ-DMOS and VHK SJ-LDMOS](image)

**Figure 7.** (a) Temperature distributions in the conventional SJ-DMOS and VHK SJ-LDMOS, (b) comparison of $R_{\text{on,sp}}$ versus BV for VHK SJ-LDMOS and other exiting technologies.

A feasible fabrication process of the VHK SJ-LDMOS is exhibited in Figure 8. The proposed VHK SJ-LDMOS fabrication starts with a P-type substrate material (100). In Figure 8a, first, an N-type buffer well and a P-well are formed by ion implantation, then the superjuction layer is formed in the N-type well, and the field oxide layer is formed by local oxidation of silicon (LOCOS) process. Next, source and drain are formed by N+ and P+ type ion implantation, respectively. A gate oxide layer is then grown, and polysilicon is deposited and etched to form a gate electrode, a gate field plate and a drain field plate, as shown in Figure 8b. In Figure 8c, a certain aspect ratio trench is then formed by the trench etch process. A dry oxidation is implemented to obtain a thin SiO$_2$ layer. In Figure 8d, the electrodes of the device are further formed by depositing and etching metal. Based on this process, the proposed device is simulated using SPROCESS as shown in Figure 8f [23]. The key parameters are all listed in Table 2.

![Key process steps for fabricating the proposed VHK SJ-LDMOS](image)

**Figure 8.** Key process steps for fabricating the proposed VHK SJ-LDMOS.
Table 2. Key parameters in the process.

| Step | Region | Mask (µm) | Process | Recipe |
|------|--------|-----------|---------|--------|
| (a)  | P-Sub  | /         | Start   | B/90 Ω-cm/＜100＞ |
|      | N-buffer | 4.0–48.0 | Implantation | As/5 × 10^{12} cm^{-2}/100 KeV/7° |
|      | P-well  | 0–4.0    | Implantation | B/7 × 10^{13} cm^{-2}/150 KeV/7° |
|      | N-pillar | 4.0–48.0 | Implantation | As/5 × 10^{13} cm^{-2}/80 KeV/7° |
|      | P-pillar | 4.0–48.0 | Implantation | As/5 × 10^{13} cm^{-2}/80 KeV/7° |
|      | LOCOS   | 4.0–44.0 | LPCVD SiO₂ | 425 °C, Gas: SiH₄ + O₂ / 500 nm |
| (b)  | Gate Oxide | 1.5–5.0 | Deposit and etch | SiO₂/0.04 µm |
|      | Poly-Si  | 1.5–5.0  | Deposit and etch | PolySilicon / 0.3 µm |
|      | N⁺      | 1.0–2.0  | Implantation  | As/5 × 10^{15} cm^{-3}/80 KeV/7° |
|      | P⁺      | 0–1.0    | Implantation  | B/2 × 10^{15} cm^{-3}/80 KeV/7° |
| (c)  | Trench  | 44.0–48.0 | Etch | Si/30 min/40 µm |
|      | Thin Oxide | /       | Deposit and etch | SiO₂/0.04 µm |
| (d)  | HK₂     | 44.0–48.0 | Deposit and etch | HK/20 µm/(permittivity)100 ε₀ |
| (e)  | HK₁     | 44.0–48.0 | Deposit and etch | HK/20 µm/(permittivity)300 ε₀ |
| (f)  | SiO₂    | 0–0.5, 1.5–44.0 | Deposit and etch | SiO₂ / 1.0 µm |
|      | Metal   | 0–3.0, 42.0–48.0 | Deposit and etch | Al/0.4 µm |

4. Conclusions

In conclusion, a new SJ-LDMOS with a variable high permittivity dielectric trench is presented in this paper. Based on the principle of dielectric RESURF, the VHK dielectric layer is designed according to different concentrations of N⁺ drain, N-buffer layer and P-substrate. The vertical bulk electric field of SJ-LDMOS is improved by the electric field modulation effect of the VHK trench. The results obtained by simulation show that the vertical electric field distribution is effectively enhanced, compared with conventional SJ-LDMOS, the blocking voltage per micron of the drift region of VHK SJ-LDMOS is increased by 41.2% with the same drift length, and the trade-off between BV and R_{on,sp} of VHK SJ-LDMOS is close to the lateral SJ silicon limit with good conduction characteristics and heat dissipation.

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