IMPLEMENTATION OF PASSWORD MANAGER WITH SRAM-BASED PHYSICAL UNCLONABLE FUNCTION

Mohammad Mohammadinodoushan
Northern Arizona University

ABSTRACT

Hacking password databases is one of the most frequently reported cyber-attacks. Current password management systems are based on known and public algorithms. Also, many studies have shown that users select weak passwords. Thus, with the emergence of new powerful computing devices, the passwords based on known algorithms can be disclosed. Using physical unclonable functions (PUFs) for increasing the security level of password management systems is a quite recent method that is proposed to solve this problem. In this method, Addressable PUF Generator (APG) is added to the conventional password management systems. This report is aimed at implementing the password generation scheme using SRAM-based PUF. The bit error is indeed the main issue with using PUFs is addresses in this paper. To solve this issue, Ternary Addressable PUF Generator is used.
1 Introduction

Traditional password (PW) management systems have used the mapping of passwords that were based on the known and public algorithms like hashing and salting [1]. However, research shows that most of the users choose common and weak passwords [2-5]. Thus, with the emergence of new powerful GPUs and computing devices, the PWs can be disclosed by brute force attacks. Another method that has been used in the literature is encrypting a PW with a key saving them in a database. However, the problem with this method is that when the key is disclosed, the PWs are also disclosed. Several systems and methods have been proposed in the literature on using physical unclonable functions (PUFs) for password generator systems to improve the level of security. In this method, Addressable PUF Generator (APG) works as a hardware protection layer. This hardware layer can be added to the software layer that can is commonly used in the PW generator systems. Using APG leads to both cost reduction and security improvement. The organization of the remainder of this document is: Section 2 contains background information about Ternary SRAM PUF, and hash-based PW management/generation schemes. Section 3 includes detailed information about the system design of including the protocol. Part 4 will focus on implementation and the results.
2 Background

2.1 PUF Designs

Many forms of PUFs have been designed in the past, which are reviewed. One type of PUFs is memory-based PUF like SRAM [6, 7] or MRAM PUF [8]. There is an increasing interest in memory-based PUFs since it is possible to make them from memories already existing in many systems. The other advantage of this kind of PUFs over conventional PUFs, is their size and speed, while they need less power comparing to traditional PUFs. Besides, the size of the required PUF is insignificant comparing to the size of the whole memory. Thus, the location of the used PUF can be another secret information, which increases security, when a hacker gets access to the memory. Using memory cells for designing PUFs in security protocol has been used a lot in the previous bodies of research.

2.1.1 SRAM-PUF

Static random-access memory (SRAM) PUFs were discovered, based on the original SRAMs independently and concurrently, by Holcomb [9] et al. [9, 10] and Guajardo et al. [11]. As shown in **Fig. 1**, a typical SRAM cell contains two cross-coupled inverters at its core with two stable states. The random physical mismatch between two is controlled by the power-up behavior, which itself is determined by the manufacturing variability. During power-up, some cells prefer storing 0, and some prefer storing 1. Responses of a PUF are the same in different cycles for these kinds of cells [12, 13].
Fig. 1 SRAM Cell, Source: Adapted from [9-14]
2.2 Addressable PUF Generator (APG)

The structure of Addressable PUF Generator (APG) [15, 16] is shown in Fig. 2. In this architecture, the controller sends an address XY to the memory array to read cells from which challenges and responses are generated. As described in [15, 16], APG can be used to create temporary passwords and authenticate users.

![Image of APG block diagram](image)

Fig. 2 Block Diagram of the APG, Source [17]

2.3 Ternary PUFs

The idea of ternary PUF is to select only the stable cells to generate the PUF output and ignore the other cells. In this section, the method of identifying fuzzy cells in both ternary SRAM and MRAM PUFs are discussed.

2.3.1 Ternary SRAM PUF

As mentioned before, the method to generate PUFs from SRAM arrays is to subject the device to power-off power-on cycles. A significant proportion of the cells always is read as either "0" or a "1". However, a few numbers of SRAM cells have a weak preference or no particular preference at all [17]. Thus, the responses of the PUF is not stable for these cells, which are known as fuzzy cells. The number of fuzzy bits divided by the
total number of bits in the pattern is defined as the SRAM PUF noise [18]. An intuitive approach to solve the issue with fuzzy cells is to read the PUF cells repeatedly and chose only those cells that always provide the same output. In the characterizing (enrollment) phase, the SRAM-PUF cells are read hundreds of times by repeating the power-off power-on cycles. In each cycle of reading, the unstable cells are specified that have different responses against their previous response and denoted by an "X" mark. In this way, it is possible to recognize the cells that can generate stable "0" and "1" and remove those with the "X". The higher number of reads is accompanied by creating a more stable challenge. From now on, only stable PUF cells generate a stable response [19].
3 Protocol

This report focuses mainly on explaining the implantation of the PW generator with APG shown in Fig. 3.

The architecture input is user ID (ID hereafter) and Password (PW hereafter) of the user. The main output of APG that is shown in Fig. 3 is the PUF response [19]. The response of PUF is generated through the following steps:

Step 1- ID and PW are the input of Addressable PUF Generator. Message Digest (MD) of PW is calculated in microcontroller (MCU) with software SHA2-256.

Step 2- The MD of the PW is the input of the "Expander block" in Fig. 3. The details about the Expander block are shown in Fig. 4. The output of the hash (or the input of Expander block) is 32 bytes, 256 bits. Since the size of the used SRAM PUF is 8 kilobytes, 16 bits are needed for addressing a specific SRAM cell. Also, the input of the Expander block, which is 256 bits, can only point to 16 independent addresses. Therefore, the extracted challenge would be 16 bit, which ends with low entropy. Thus, we cannot cover enough number of users. Expander block is designed for increasing the entropy. Increasing the entropy is done by generating longer MD from the original MD. As can be seen in Fig. 4, the left two bytes of the MD are rotated eight times. Then, all the results of shifting MD will be the inputs of SHA2-256, as shown in Fig. 4. The longer message digest is 256 bytes, which are the concatenation of 8 message digests. These 256 are enough to generate a 128-bit challenge/response stream and provide high entropy.
Step 3- The outputs of "Expander block" are 128 addressees of SRAM cells. These addresses include the address of fuzzy cells.

Step 4- The outputs of "Expander block" is revised in the Masking block (Masking fuzzy cells). In this block, the addresses of the fuzzy cells are ignored. The next non-fuzzy cell after each fuzzy cell is considered for extracting the challenge or response of PUF. The output of the masking block is 128 addresses.

Step 5- Each bit of PUF response is obtained in 128 addresses generated in Step 4. Therefore, the response of PUF is 128 bit, as shown in Fig. 3.

![Fig. 3 The implemented architecture for APG with wifire and 1Mbit Cypress SRAM](image)
Fig. 4 Details of "Expander block" shown in Fig. 3 [19]
4 Implementation and results

The APG is implemented using WiFire development boards from Digilent, powered by Microchip [20] and 1-MBIT CYPRESS SRAM[21], as shown in Fig. 5. The SRAM part number is CY7C1021CV26, which is a 1Mbit SRAM arranged in 64 K words every 16 bits. A similar protocol [19] for SAMV71 MCU with Cortex M7 core and 32 Kbyte SRAM is revised to make it compatible with wifire board. The coding environment for coding is Arduino IDE due to its simplicity. The functions used in the code and the result of each function are explained briefly in the next coming sections.

4.1 Receiving data

At the beginning of the program, the ID and password (PW) is sent to microcontroller (MCU) which is WiFire board. MCU captures and echo every single received byte and then the ID and PW in the HEX format to the terminal. The codes in Fig. 6 shows how the data is received, echo back and printed in hex format for ID string:
Serial.print("\n\r Enter your ID\n\r");
recv_char = 0;
i_counter = 0;
while ((recv_char != 'n') && (recv_char != 'r') && (i_counter < MSG_SIZE))
{
    if(Serial.available())
    {
        recv_char = Serial.read();
        Serial.write(recv_char); // echo to terminal
        id_buff[i_counter++] = recv_char; // queue character into buffer
    }
}
id_buff[i_counter-1] = '\0'; // the last character was enter, then replace it with NULL
id_size = i_counter-1;

**Fig. 6** Code used for receiving data of the user

The result of this step is shown in **Fig. 7**

![Image](image.png)

**Fig. 7** Results of receiving and printing the ID and PW
4.2 Processing data and making the address

The results of steps that occur in the "Expander block" are shown in Fig. 8 and Fig. 9. These results are obtained after entering "PasswordManagementWithWifire" and "1-Mbit SRAM" as the "Username" and "Password". As previously mentioned, the output of the hash digest (or the input of the Expander block in Fig. 3) is 32 bytes. As can be seen in Fig. 4, the two most significant bytes of the MD is rotated 8 times. Then, all the results of shifting MD will be the inputs of SHA2-256, as shown in Fig. 4. The results of these eight messages digest are shown in Fig. 9.

Results of Shifting Message Digest:

| MD1 | MD2 | MD3 | MD4 | MD5 | MD6 | MD7 | MD8 |
|-----|-----|-----|-----|-----|-----|-----|-----|
| 16 A8 DE D1 42 09 57 EB 04 2B C4 0F 08 DB 2B 2C 14 52 BB 4D EB 06 63 B5 ED 43 9C 26 7C 15 78 04 |
| 2D 50 DE D1 42 09 57 EB 04 2B C4 0F 08 DB 2B 2C 14 52 BB 4D EB 06 63 B5 ED 43 9C 26 7C 15 78 04 |
| 5A 00 DE D1 42 09 57 EB 04 2B C4 0F 08 DB 2B 2C 14 52 BB 4D EB 06 63 B5 ED 43 9C 26 7C 15 78 04 |
| E5 40 DE D1 42 09 57 EB 04 2B C4 0F 08 DB 2B 2C 14 52 BB 4D EB 06 63 B5 ED 43 9C 26 7C 15 78 04 |
| 6A 81 DE D1 42 09 57 EB 04 2B C4 0F 08 DB 2B 2C 14 52 BB 4D EB 06 63 B5 ED 43 9C 26 7C 15 78 04 |
| D5 02 DE D1 42 09 57 EB 04 2B C4 0F 08 DB 2B 2C 14 52 BB 4D EB 06 63 B5 ED 43 9C 26 7C 15 78 04 |
| AA 05 DE D1 42 09 57 EB 04 2B C4 0F 08 DB 2B 2C 14 52 BB 4D EB 06 63 B5 ED 43 9C 26 7C 15 78 04 |
| 5A 00 DE D1 42 09 57 EB 04 2B C4 0F 08 DB 2B 2C 14 52 BB 4D EB 06 63 B5 ED 43 9C 26 7C 15 78 04 |

Finally, 8 MD (each MD is 32 Bytes) results that are shown in Fig. 9 will be concatenated to generate long MD in Expander block. Therefore, the length of Long MD is 8*32 = 256 Bytes, which is used to generated "128 Addresses for extracting PUF Response". Since just 8 kilobytes of SRAM is used as PUF, we need 16
(2 bytes) bits for addressing a specific cell. Thus, we will have \(256/2=128\) addresses, which are shown in Fig. 10.

### Fig. 10 Generating "128 Addresses for extracting PUF Response" after Masking the fuzzy cells

Each bit of the challenge/Response is extracted in 128 addresses as shown in Fig. eee. The extracted SRAM-PUF response is shown in Fig. 11.

### Fig. 11 128 bit PUF response extracted in 128 addresses shown in Fig. 10

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