An Efficient List Decoder Architecture for Polar Codes

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Abstract—Long polar codes can achieve the symmetric capacity of arbitrary binary-input discrete memoryless channels under a low complexity successive cancelation (SC) decoding algorithm. However, for polar codes with short and moderate code length, the decoding performance of the SC algorithm is inferior. The cyclic redundancy check (CRC) aided successive cancellation list (SCL) decoding algorithm has better error performance than the SC algorithm for short or moderate polar codes. In this paper, we propose an efficient list decoder architecture for the CRC aided SCL algorithm, based on both algorithmic reformulations and architectural techniques. In particular, an area efficient message memory architecture is proposed to reduce the area of the proposed decoder architecture. An efficient path pruning unit suitable for large list size is also proposed. For a polar code of length 1024 and rate $1/2$, when list size $L = 2$ and 4, the proposed list decoder architecture is implemented under a TSMC 90nm CMOS technology. Compared with the list decoders in the literature, our decoder achieves 1.24 to 1.83 times hardware efficiency.

Index Terms—polar codes, successive cancelation decoding, list decoding, hardware implementation

I. INTRODUCTION

Polar codes, recently introduced by Arıkan [1], are a significant breakthrough in coding theory. It is proved that polar codes can achieve the channel capacity of binary-input symmetric memoryless channels [1] and the capacity of any discrete or continuous channel [2]. Polar codes can be efficiently decoded by the low-complexity successive cancelation (SC) decoding algorithm [1] with complexity of $O(N \log N)$, where $N$ is the block length.

Though the theoretical results are exciting, polar codes require very large code block length (for example, $N > 2^{20}$ [3]) to approach the channel capacity using the SC algorithm. Such long block length is impractical in many applications, such as wireless communication systems where the packet size is only several hundred to several thousand bits. For short or moderate length, the error performance of polar codes with the SC algorithm is worse than Turbo or low-density parity-check (LDPC) codes [4].

Lots of efforts [4]–[11] have already been devoted to the improvement of error-correction performance of polar codes with short or moderate lengths. An SC list (SCL) decoding algorithm was proposed recently in [4], which performs better than the SC algorithm and performs almost the same as a maximum-likelihood (ML) decoder [4]. In [5]–[7], the cyclic redundancy check (CRC) is used to pick the output codeword from $L$ candidates, where $L$ is the list size. The CRC-aided SCL algorithm performs much better than the SCL algorithm at the expense of negligible loss in code rate. For example, it was shown [5] that the CRC-aided SCL algorithm outperforms the SC algorithm by more than 1 dB when the bit error rate (BER) is on the order of $10^{-5}$ for a polar code of length $N = 2048$. The belief propagation (BP) algorithm on the factor graph of polar codes was investigated in [9]. It was shown in [9] that finite-length polar codes show superior error floor performance compared to the conventional capacity-approaching coding techniques. In [10], polar codes were shown to be instances of generalized concatenated codes. It was suggested in [10] that the performance of polar codes can be improved by considering them as generalized concatenated codes, and using block-wise near-maximum-likelihood decoding of optimized outer codes.

In terms of the hardware implementations of the SC algorithm, few works have been done. In [12], an FPGA implementation of a polar decoder based on belief propagation was proposed. An efficient semi-parallel SC decoder was proposed in [3], where resource sharing and semi-parallel processing were used to reduce the hardware complexity. An overlapped computation method and a pre-computation method were proposed in [13] to improve the throughput and to reduce the decoding latency of SC decoders. Compared to the semi-parallel decoder architecture in [3], the pre-computation based decoder architecture [13] can double the throughput. A simplified SC decoder for polar codes, proposed in [14], reduces the decoding latency by more than 88% for a rate 0.7 polar code with length $2^{18}$.

The investigation of efficient list decoder architectures for polar codes is motivated by improved error performance of the SCL and CA-SCL algorithms, especially for polar codes with short or moderate length. The tree search list decoder architecture for the SCL algorithm proposed in [15] is the only list decoder architectures for polar codes in the literature to the best of our knowledge. In this paper, we propose the first hardware implementation of the CA-SCL algorithm to the best of our knowledge. Based on both algorithmic and architectural improvements, our decoder architecture achieves better error performance and higher hardware efficiency compared with the decoder architecture in [15]. Specifically, the major contributions of this work are:

1) Message memories account for a significant fraction of an SC or SCL decoder [3], [15]. In this paper, an area efficient message memory architecture is proposed. Besides, a new compression method for the channel messages is used to reduce the area of the proposed decoder architecture.
2) An efficient processing unit (PU) is proposed. For the proposed list decoder architecture, a fine grained PU...
profiling (FPP) algorithm is proposed to determine the minimum quantization size of each input message for each PU so that there is no message overflow. By using the quantization size generated by the FPP algorithm for each PUs, the overall area of all PUs is reduced.

3) An efficient scalable path pruning unit (PPU) is proposed to control the copying of decoding paths. Based on the proposed memory architecture and the scalable PPU, our list decoder architecture is suitable for large list sizes.

4) A low-complexity direct selection scheme is proposed for the CA-SCL algorithm when a strong CRC is used (e.g., CRC32). The proposed direct selection scheme simplifies the selection of the final output codeword.

5) For a (1024, 512) rate-2/3 polar code, the proposed list decoder architecture is implemented for list size \( L = 2 \) and 4, respectively, under a 90nm CMOS technology. Compared with the decoder architecture in [15] synthesized under the same technology, our decoder achieves 1.24 to 1.83 times hardware efficiency (throughput normalized by area). Besides, the proposed CA-SCL decoder has better error performance compared with the SCL decoder in [15].

The rest of this paper is organized as follows. In Section II, polar codes as well as the SCL and CA-SCL algorithms are briefly reviewed. Two improvements of the CA-SCL algorithm are discussed in Section III. The proposed list decoder architecture is described in Section IV. Section V shows the implementation and comparison results of the proposed list decoder architecture. The conclusions are drawn in Section VI.

II. POLAR CODES AND ITS CA-SCL ALGORITHM

A. Polar Codes

A generation matrix of a polar code is an \( N \times N \) matrix \( G = B_N F^{\otimes n} \), where \( N = 2^n \), \( B_N \) is the bit reversal permutation matrix [1], and \( F = \begin{pmatrix} 1 & 0 \\ 1 & 1 \end{pmatrix} \). Here \( \otimes \) denotes the \( n \)th Kronecker power and \( F^{\otimes n} = F \otimes F^{\otimes(n-1)} \). Let \( u_0^{N-1} = (u_0, u_1, \ldots, u_{N-1}) \) denote the data bit sequence and \( x_0^{N-1} = (x_0, x_1, \ldots, x_{N-1}) \) the corresponding encoded bit sequence, then \( x_0^{N-1} = u_0^{N-1}G \). The indices of the encoding bit sequence \( u_0^{N-1} \) are divided into two sets: the information bits set \( A \) contains indices and the frozen bits set \( A^c \) contains \( N - K \) indices. \( u_A \) are the information bits whose indices all come from \( A \), \( u_{A^c} \) are the frozen bits whose indices from \( A^c \).

B. SCL Algorithm

List decoding was applied to the SC algorithm in [4] and the resulting SCL algorithm outperforms the SC algorithm. For a list size \( L \), the SCL algorithm keeps at most \( L \) decoding paths and outputs \( L \) possible decoded codewords \( \hat{u}_0^{N-1}, \hat{u}_1^{N-1}, \ldots, \hat{u}_{L-1}^{N-1} \) where \( \hat{u}_{l,0}^{N-1} = (\hat{u}_{l,0}, \hat{u}_{l,1}, \ldots, \hat{u}_{l,N-1}) \). A low complexity state copying scheme was proposed in [15] to simplify the copying process when a decoding path needs to be duplicated.

For \( l = 0, 1, \ldots, L - 1 \) and \( \lambda = 0, 1, \ldots, n \), let \( P_{l,\lambda} \) be an array with \( 2^{n-\lambda} \) elements: \( P_{l,\lambda}[j] \) contains two messages \( P_{l,\lambda}[j][0] \) and \( P_{l,\lambda}[j][1] \) for \( j = 0, 1, \ldots, 2^{n-\lambda} - 1 \). \( C_{l,\lambda} \) has the same structure as \( P_{l,\lambda} \): \( C_{l,\lambda}[j] \) contains two binary partial sums \( C_{l,\lambda}[j][0] \) and \( C_{l,\lambda}[j][1] \) for \( j = 0, 1, \ldots, 2^{n-\lambda} - 1 \). The SCL algorithm with low complexity state copying [4], [15] is formulated in Algorithm 1. For the decoding of \( u_l \), the SCL algorithm can be divided into the following parts:

- For each surviving decoding path \( l \), compute the path metrics \( P_{l,0}[0][0] \) and \( P_{l,0}[0][1] \) using the recursive function metricComp\((l, i)\) shown in Algorithm 2. For \( i = 1, 2, \ldots, N-1 \), let \( (b_n^{(i)}, b_{n-1}^{(i)}, \ldots, b_0^{(i)}) \) denote the binary representation of index \( i \), where \( i = \sum_{j=0}^{n-1} 2^j b_n^{(i)} \). 

### Algorithm 1: SCL algorithm [4]

**input**: \( n \), the received vector \( y \)
**output**: \( \hat{u}_0^{N-1} \)

1. for \( l = 0 \) to \( L - 1 \) do
2.   for \( \beta = 0 \) to \( N - 1 \) do
3.     \( P_{l,0}[\beta][s] = \Pr(y_{\beta}[s], s = 0, 1 \)
4.   for \( \lambda = 0 \) to \( n \) do
5.     \( r_l[\lambda] = 0 \)
6.   for \( i = 0 \) to \( N - 1 \) do
7.     \( \lambda = \phi(i) \) to \( n - 1 \) do
8.       \( r_l[\lambda] = l \) foreach survived decoding path \( l \) do
9.         metricComp\((l, i)\)
10.         if \( i \in A^c \) then
11.           pathPruning\((P_{0,n,\cdots,P_{L-1,n}})\)
12.         else
13.           if \( i \mod 2 == 1 \) then
14.             pUpdate\((l, n, i)\)
15.         else
16.           foreach survived decoding path \( l \) do
17.             pUpdate\((l, n, i)\)
18.   end for
19.   end for
20. end for

### Algorithm 2: metricComp\((l, i)\) [4]

**input**: \( l, i \)

1. determine \((b_n^{(i)}, b_{n-1}^{(i)}, \ldots, b_0^{(i)}) \) and \( \phi(i) \)
2. for \( \lambda = \phi(i) \) to \( n \) do
3.   for \( k = 0 \) to \( 2^{n-\lambda} - 1 \) do
4.     if \( b_k^{(i)} = 1 \) and \( \lambda = \phi(i) \) then
5.       \( s = C_{l,\lambda}[\beta][0] \)
6.       \( P_{l,\lambda}[k][u] = G(P_{l,\lambda-1}[2k], P_{l,\lambda-1}[2k+1], s) \)
7.       \( = \frac{1}{2} P_{l,\lambda-1}[2k][u + s] \cdot P_{l,\lambda-1}[2k+1][u] \) for \( u \in \{0, 1\} \)
8.     else
9.       \( P_{l,\lambda}[k][u] = F(P_{l,\lambda-1}[2k], P_{l,\lambda-1}[2k+1]) \)
10.      \( = \sum_{u'=0}^{1} \frac{1}{2} P_{l,\lambda-1}[2k][u + u'] \cdot P_{l,\lambda-1}[2k+1][u'] \) for \( u \in \{0, 1\} \)
11.   end for
12. end for
13. end for
\((1 \leq \phi^{(i)} \leq n)\) in Algorithm 2 is the largest integer such that \(\beta_{\phi^{(i)}} = 1\). When \(i = 0\), \(\phi^{(i)} = 1\). Based on the recursive algorithm for computing path metric in [4] and the low complexity state copying algorithm in [15], the path metric computation is formulated in a non-recursive way in Algorithm 2, where \(r_l = (r_l[n - 1], r_l[n - 2], \ldots, r_l[0])\) is the message updating reference index array for decoding path \(l\). For decoding path \(l\), \(r_l[0] = 0\), while all other elements are initialized with 0. Two types of basic operations, denoted as \(F\) and \(G\) operations, respectively, are employed in Algorithm 2:

- **If** \(u_0\) is a frozen bit, for each decoding path, the decoded code bit \(u_{l,i} = 0\), decoding path \(l\) will carry on with \(u_{l,i} = 0\). If \(u_i\) is an information bit, decoding path \(l\) \((l = 0, 1, \ldots, L - 1)\) splits into two decoding paths with corresponding path metrics being \(P_l[n_0][0]\) and \(P_l[n_0][1]\), respectively. There are at most \(2L\) paths after splitting, and \(2L\) associated path metrics. The pathPruning function in Algorithm 1 finds the \(L\) most reliable decoding paths based on their corresponding path metrics.

- For each of the \(L\) surviving decoding paths, the \(pUpdate(l, n, i)\) function shown in Algorithm 3 [4] updates the partial sum matrices that will be used in the following path metric computation.

We make several observations about the path metric computation:

- When \(i = 0\), \(P_{l,1}, \ldots, P_{l,n}\) are updated in serial, and only the \(F\) computation is employed.

- For \(i > 0\), \(P_{l,\phi^{(i)}}, \ldots, P_{l,n}\) are updated in serial. The \(G\) computation is used when computing \(P_{l,\phi^{(i)}}\), while the \(F\) computation is used for the other probability message arrays.

- The computation of \(P_{l,\phi^{(i)}}\) is based on \(P_{r_l[\phi^{(i)} - 1],\phi^{(i)} - 1}\), while the computation of \(P_{l,\lambda}\) \((\lambda > \phi^{(i)})\) is based on \(P_{l,\lambda - 1}\).

**Algorithm 3: pUpdate(l, λ, i) [4]**

```
input : l, λ, i
1 if λ == 0 then return j = [i/2]
2 for β = 0 to \(2^n - λ - 1\) do
3 \(C_{l,λ-1}[2β][j mod 2] = C_{l,λ}[β][0] + C_{l,λ}[β][1]\)
4 \(C_{l,λ-1}[2β + 1][j mod 2] = C_{l,λ}[β][1]\)
5 if j mod 2 == 1 then pUpdate(l, λ - 1, j)
```

The path pruning function, pathPruning, finds the \(L\) most reliable paths, \(a_0, a_1, \ldots, a_L\), and their corresponding decoded bits, \(c_0, c_1, \ldots, c_L\), based on the path metrics. The path metrics of the surviving \(L\) decoding paths are the \(L\) largest ones among \(2L\) input metrics. Once the surviving decoding paths are found, decoding path \(l\) will copy from decoding path \(a_l\). The partial sum computation of decoding path \(l\) is carried on with the binary input \(c_l\).

The pruning scheme in this paper and the path pruning scheme in [11] both try to eliminate decoding paths that are less reliable. However, there are still some differences as shown below.

- The pruning scheme in [11] is used for successive cancellation stack (SCS) decoding algorithm as well as the SCH decoding algorithm, which is a hybrid of SCL and SCS decoding algorithms, whereas our pruning scheme is used for the SCL algorithm.

- For the SCL algorithm, suppose there are \(L\) decoding paths before the decoding of \(u_i\), then the metrics of \(2L\) expanded decoding paths are computed. The pruning scheme in this paper finds the \(L\) largest metrics out of \(2L\) metrics and keeps their corresponding decoding paths. For the pruning scheme in [11], a path will be deleted if its path metric is smaller than a dynamic threshold, \(a_i - \ln(\tau)\), where \(a_i\) is the largest metric of candidate paths, and \(\tau\) is a configuration parameter.

- For the path pruning scheme in [11], the number of deleted paths is not fixed and depends on the configuration parameter \(\tau\), while the number of deleted paths is always \(L\) for the pruning scheme in this paper.

The SCL algorithm implemented in [4] is based on probability domain, where the \(F\) and \(G\) operations in Algorithm 2 are employed. As shown in [6], the \(F\) and \(G\) operations in Algorithm 2 can also be performed over the logarithm domain. For \(u \in \{0, 1\}\), the resulting logarithm domain \(G\) and \(F\) computations are shown in Eq. (1) and Eq. (2), respectively, where \(\max^*(x, y) = \max(x, y) + \log(1 + e^{-|x - y|})\), \(\max^*(x, y)\) can also be approximated with \(\max(x, y)\), resulting in the approximated \(F\) computation in Eq. (3).

**C. CA-SCL algorithm**

In [5], the performance of the SCL algorithm is further improved by the adoption of CRC, which helps to pick the right path from the \(L\) possible decoded codewords. In terms of the fixed point implementation, the CA-SCL algorithm is quite sensitive to saturation. For two decoding paths, it is hard to decide which is better if the metrics of both paths are saturated. In order to avoid message saturation, a non-uniform quantization scheme is proposed in [15]. If the channel messages \((P_{l,0})\) are all quantized with \(t\) bits, all the log-likelihood messages (LLMs) of \(P_{l,\lambda}\) need to be quantized with \(t + \lambda\) bits in order to avoid saturation.

**III. TWO IMPROVEMENTS OF THE CA-SCL ALGORITHM**

In this paper, two improvements of the CA-SCL algorithm are proposed. Firstly, for the \(i\)-th received bit \(y_i\), there are two likelihoods, \(\Pr\{y_i|0\}\) and \(\Pr\{y_i|1\}\). Suppose \(\Pr\{y_i|m\}\) \((m \in \{0, 1\})\) is the smaller one among the two likelihoods. For \(j \in \{0, 1\}\), two log-likelihood messages (LLMs) are defined as

\[
P_{l,0}[i][j] = \log \frac{\Pr\{y_i|0\}}{\Pr\{y_i|m\}}.
\]  (4)

Thus one of the LLMs is always 0, and the other is always non-negative. For the proposed list decoder, only the non-negative LLM and its corresponding binary index \(s\) are stored. As shown in Fig. 1, Msg denotes the stored non-negative LLM, and its corresponding bit index is \(s\). When \(s = 0\), \(P_{l,0}[i][0] = \text{Msg} \cdot P_{l,0}[i][1] = 0\). When \(s = 1\), \(P_{l,0}[i][0] = 0\), \(P_{l,0}[i][1] = \text{Msg}\). If \(t\) bits are needed to quantize a channel LLM, it takes
The probabilities, $p$

Note that $p$ the list size our analysis, we can use three probabilities:

- The probability that the CRC identifies the candidate as
- The probability that the candidate data word is the same
- The probability that the CRC checks fail, since the CRC checksum could be corrupted, a decoding failure is announced if re-transmission is possible; otherwise, pick a data word randomly and output.

The direct selection scheme reduces computational complexity at the expense of possible performance degradation. In this paper, we give an estimation of the frame error rate (FER) degradation. Let $w$ denote the number of the detectable errors for our CRC. Assume all the bits of the final $L$ candidate data words are independently subject to a bit error probability, $p_b$. We calculate the increased FER, $P_e$, caused by the direct selection scheme instead of the ideal selection scheme, which always selects the transmitted data word if it is within the final $L$ candidates. For each candidate data word, there are three probabilities:

- The probability that the candidate data word is the same as the transmitted one is given by $p_1 = (1 - p_b)^K$.
- The probability that the candidate fails the CRC is denoted as $p_2$.
- The probability that the CRC identifies the candidate as the transmitted data word by mistake is denoted as $p_3$, and $p_3 = \sum_{r=w+1}^{K} \binom{K}{r} p_b^r (1 - p_b)^{K-r} = \binom{K}{w+1} p_b^{w+1} (1 - p_b)^{K-w-1}$.

Clearly, $p_1 + p_2 + p_3 = 1$.

Based on above assumptions and definitions, the increased FER

$$P_e \leq p_3 \frac{1 - p_b^L}{1 - p_2} + p_2^L - (1 - p_1)^L.$$  \hspace{1cm} (5)

Note that $p_b$ depends on the signal to noise ratio (SNR) and the list size $L$. For a specific SNR, in order to simplify our analysis, we can use $p_{b,SC}$ to approximate $p_b$, where $p_{b,SC}$ denotes the bit error probability of the SC algorithm. The probabilities, $p_2$ and $p_3$, are also approximated. Though approximated probabilities are employed when calculating $P_e$, the order of $P_e$ still helps us in determining whether our direct selection scheme is applicable. The impact of all the parameters are demonstrated in [4]. When a strong CRC is used, i.e. large $w$, $p_3$ is small, leading to a small $P_e$. On the other hand, a higher data rate leads to a greater $K$ and hence a greater $P_e$.

A. Numerical Results

For a rate 1/2 polar code with block length $N = 1024$, the frame error rate performances of the SC, SCL and CA-SCL algorithms are shown in Fig. 2, where SC denotes the floating-point SC algorithm. CS2-max and CS2-map denote the floating-point CA-SCL algorithm with $L = 2$ and the approximated $F$ computation shown in Eq. (3) and the $F$ computation shown in Eq. (4), respectively. $Si-max-j$ denotes the fixed-point CA-SCL algorithm with $L = i$ and non-uniform quantization scheme with $t = j$, where $t$ is the number of quantization bits for channel probability message. $Si-max-j$ denotes the fixed-point SCL algorithm with $L = i$ and non-uniform quantization scheme with $t = j$. For all simulated CA-SCL algorithms, the CRC32 scheme is employed, and the direct selection scheme is employed to pick the final output codeword from $L$ possible candidates. The generation polynomial of the CRC32 is 0x1EDC6F41.

Graphs showing the frame error rate performance of different algorithms with varying SNR.
When each channel LLM is quantized with 4 bits, the employment of the proposed non-uniform quantization scheme leads to negligible performance degradation. When each channel LLM is quantized with 3 bits, the resulting FER performance is roughly 0.2dB worse than that using 4-bit quantization.

- Using a larger list size ($L > 2$) leads to obvious decoding performance improvement for the CA-SCL algorithm, whereas the SCL algorithm with $L = 2, 4$ has nearly the same decoding performance, especially in the high SNR region. For polar codes with moderate block length (e.g. $N = 2^{11}, 2^{12}, 2^{13}$), similar phenomena has been observed in [5].

In this paper, more simulation results on the proposed direct selection scheme are provided. There are three selection schemes employed in our simulations.

- The proposed direct selection (DS) scheme, which outputs the first codeword that passes CRC.
- Ideal selection (IS) scheme, which always outputs the correct codeword if it exists in the final list.
- Metric based selection (MS) scheme [5], which outputs the codeword that has the maximal path metric among all codewords that have passed CRC.

Still, the polar code of block length $N = 1024$ is used in our simulations. In Figs. 3 to 6, $DS_k$, $IS_k$ and $MS_k$ denote the CA-SCL algorithms with list size $L = k$ under the direct selection scheme, the ideal selection scheme and the metric based selection scheme, respectively. The generation polynomial of the CRC16 used in our simulations is $0x1021$.

As shown in Fig. 3 when code rate is 0.75, the proposed direct selection scheme introduces early error floor for all simulated list sizes while the metric based selection scheme performs nearly the same as the ideal selection scheme. When code rate is 0.5, as shown in Fig. 4 the direct selection scheme performs nearly the same as the ideal selection scheme with list size $L = 2$. When list size $L = 4, 8, 16$, the proposed direct selection scheme shows certain performance degradation compared with the ideal selection scheme, while the metric based selection scheme has little performance degradation. As shown in Figs. 3 and 6 when CRC32 is used, the proposed direct selection scheme performs nearly the same as the ideal selection scheme for both code rates 0.5 and 0.75.

We also calculate the $F_e$’s for all simulated cases in Figs. 3 to 6. We choose SNR = 3.6dB, since DS4, DS8 and DS16 begin to show an error floor in Fig. 3. For the length 1024 polar code, the bit error probability $p_b$ from the SC algorithm is $6.28 \times 10^{-4}$ and $3.04 \times 10^{-6}$ for rate 0.75 and 0.5, respectively. The underlying channel is AWGN and the modulation is BPSK. For CRC16 and CRC32, $w = 2$ [16] and 4 [17], respectively. When CRC16 is used, for each simulated list size, the order of $P_e$ is around $10^{-2}$ and $10^{-10}$ for rate 0.75 and 0.5, respectively. When CRC32 is used, for each simulated list size, the order of $P_e$ is $10^{-4}$ and $10^{-17}$ for rate 0.75 and 0.5, respectively. As shown in Figs. 3 to 6, it is found that the error degradation caused by our DS scheme is big when the corresponding $P_e$ is big (e.g. $10^{-2}$). On the other hand, when $P_e$ is quite small (e.g. $10^{-17}$), our DS scheme leads to little performance degradation.

Based on our calculation results, for a given CRC and code rate, $P_e$ increases with the list size $L$. This observation indicates that the potential performance degradation caused by the DS scheme will increase when $L$ increases. This is consistent with the simulation results shown in Figs. 3 and 6.

IV. EFFICIENT LIST DECODER ARCHITECTURE

For the CA-SCL algorithm, we propose an efficient partial parallel list decoder architecture shown in Fig. 7. The proposed list decoder architecture mainly consists of the channel message memory (C-MEM), the internal LLM memory (L-MEM), $L$ processing unit arrays (PUAs) (PUA0, PUA1, · · · , PUAL−1), the path pruning unit (PPU) and the CRC checksum unit (CRCU). These components are described in details in the following subsections.

A. Message Memory Architecture

The L-MEM stores all the inner LLMs used for metric computation. Since all the LLMs in $P_{l,\lambda}$ need to be quantized
For λ = 1, 2, ⋯, n, since each LLM within $P_\lambda = (P_0, P_1, \cdots, P_{L-1, \lambda})$ is quantized with $t + \lambda$ bits, a regular sub-memory is created for storing LLMs in $P_\lambda$.

- All $n$ sub-memories are combined to a single memory.
- Due to the nonuniform quantization, the width of each sub-memory maybe different. As a result, the concatenated L-MEM is an irregular memory with varying width within its address space. For the proposed memory architecture, the irregular L-MEM is split into several regular memories to fit current memory generation tools.

The proposed L-MEM is a mix of different types of memories, including SRAM, register file (RF) or register. Since SRAM and RF are more area efficient than a register, the proposed L-MEM architecture is better than the register based LLM memory in [15], especially for area restricting applications.

Suppose there are $T$ processing units (PUs) in each PUA shown in Fig. 7, it consumes at most $4LT$ LLMs for one round of computation. For λ = 1, 2, ⋯, n, we store all the LLMs within $P_\lambda = (P_0, P_1, \cdots, P_{L-1, \lambda})$ in a single memory as follows.

- When $2^{n-\lambda+1}L > 4LT$, it takes a sub-memory of $2^{n-\lambda+1}$ words, where each word has $4LT(t + \lambda)$ bits.
- When $2^{n-\lambda+1}L \leq 4LT$, it takes a sub-memory with only one single word, which has $2^{n-\lambda+1}(t + \lambda)L$ bits.

An example of the concatenation of $n = 6$ sub-memories, $(S_1, S_2, \cdots, S_6)$, is shown in Fig. 8(a). For current memory compiler, it is hard to generate an irregular single memory instance as shown in Fig. 8(a).

For the proposed L-MEM architecture, the concatenated irregular memory is split into several regular memory instances as shown in Fig. 8(b), where additional dummy memories are added so that each instance is regular. For general cases, the irregular memory is divided into $\lambda_0 = n - \log_2 T - 1$ regular instances. Depending on the number of words, each memory instance could be implemented with SRAM, RF or registers.  

Compared with the register based LLM memory, the proposed L-MEM architecture is more area efficient due to the following reasons:

- Some sub-memory instances can be implemented with SRAM or RF which is more dense than register based
As shown in Fig. 8(b), most of the LLMs are store in the largest memory instance M_1 which contains
\[ N_w = n - \lambda_o + 1 + \sum_{\lambda=1}^{\lambda-1} \frac{2^{n-\lambda-1}}{T} \] (6)

words, where each word has 4LT(t + 1) bits.

As shown in Eq. (6), N_w is inverse to the number of processing units, T, within a PUA. As a result, the area of the proposed L-MEM depends on T for a fixed block length N = 2^n and t. Taking RF as an example, we show the comparison of area efficiency of RFs with different depth in Table II, where area per bit (APB) denotes the total area of a memory normalized by the number of total bits. The total areas shown in Table II are from a memory compiler associated with a 90nm technology. As shown in Table II the RF with a larger depth has a smaller APB. Hence, given the same amount of bits, it takes a smaller area if those bits can be stored in a RF with a larger depth. For SRAM, the same phenomena has been observed.

**TABLE I**

| depth | 8 | 16 | 32 | 64 | 128 |
|-------|---|----|----|----|-----|
| width | 128 | 256 | 512 | 1024 | 2048 |
| process | 90nm | 90nm | 90nm | 90nm | 90nm |
| total area (\mu m^2) | 24331 | 25022 | 23308 | 42812 | 63811 |
| APB (\mu m^2) | 23.7 | 13.1 | 7.9 | 5.2 | 3.89 |

The C-MEM can be implemented with a simple regular memory, which has \( \frac{N}{T} \) words and each word has 2T(t + 1) bits. Due to the proposed compression of the channel message, each compressed channel message is de-compressed into two LLMs before being fed to the PUs.

**B. Processing Unit Array**

1) **Processing Unit Architecture:** The G and approximated F computations shown in Eq. (1) and Eq. (3), respectively, are used in the metric computation. These two types of basic operation can be performed with the PU shown in Fig. 9 where \( mode = 0 \), the approximated \( F \) computation is performed. When \( mode = 1 \), the \( G \) computation is performed. These four adders in Fig. 9 are shared by both the \( G \) and approximated \( F \) computations. The hardware complexity of the proposed PU is determined by \( p \), which is the width of an output LLM.

**Fig. 9.** Processing unit (PU) architecture for the \( G \) and approximated \( F \) computations

2) **Fine grained PU profiling:** Due to the non-uniform quantization of the LLMs belonging to different message arrays, for each PU, the number of quantization bits, \( p \), for each input LLM should be large enough so that no overflow will happen. According to the fixed point implementation of the CA-SCL algorithm, the quantization of \( P_{1,n} \) (\( l = 0, 1, \cdots, L - 1 \)) needs the most binary bits, which is \( t + n \). For each PUA, it is unnecessary to employ \( T \) PUs with \( p + 1 = t + n \). In this paper, a fine grained PU profiling (FPP) algorithm, shown in Algorithm 4, is proposed to decide \( p \) for each PU.

**Algorithm 4: FPP Algorithm**

```
\begin{algorithm}
\ \input : n, t, \lambda_o = n - \log_2 T - 1
\ \output : p[0], p[1], \cdots, p[T-1]
\begin{algorithmic}[1]
1 \ \for j = 0 \ \to T - 1 \ \do
2 \quad p[j] = t + \lambda_o - 1
3 \ \for \lambda = \lambda_o + 1 \ \to n \ \do
4 \quad \for j = 0 \ \to 2^{n-\lambda} - 1 \ \do
5 \quad \quad p[j] = t + \lambda - 1
\end{algorithmic}
\end{algorithm}
```

For the \( j \)-th PU of PUA_t (\( l = 0, 1, \cdots, L - 1 \)), each LLM input is quantized with \( p[j] \) bits. The proposed FPP algorithm is based on the observation that only \( 2^{n-\lambda} < T \) PUs are needed when computing the updated \( P_{l,\lambda} \) with \( \lambda > \lambda_o \). Thus, in the proposed PUA_t, only \( PU_{l,0}, PU_{l,0}, \cdots, PU_{l,2^{n-\lambda}-1} \) are enabled for the computing of \( P_{l,\lambda} \). Based on the proposed FPP algorithm, each PUA can finish the metric computation without any overflow at the cost of less area consumption.

As shown in Algorithm 4, the bit width of the LLM inputs of a PU is determined by \( n, T \) and \( t \). One example is shown in Table II where \( n = 10, T = 8 \) and \( t = 4 \).

The area saving due to the proposed fine grained profiling algorithm also depends on \( T, n \) and \( t \). For the proposed list decoder architecture, there are \( L \) identical PU arrays, where each array contains \( T \) PUs. In Table II we compare the area
of a regular PU array with that of an array where the input message width of each PU is determined by the fine grained profiling algorithm. As shown in Table III, the area of PU arrays is reduced by 30% to 55% depending on the number of PUs with an array and the block length $N = 2^n$. Here, each channel message is quantized with $t = 4$ bits.

3) Metric Computation Schedule: For the proposed L-MEM, each data word is capable of storing $4TL$ LLMs. Moreover, each word is equally divided into $L$ consecutive parts, where the $l$-th part stores the LLMs corresponding to decoding path $l$. The metric computation schedule is almost the same as that of the parallel SC decoder in [3] except that L PUsAs work simultaneously for $L$ decoding paths, respectively.

When a data word needs to be updated, the write mismatch would happen since L PUsAs generate only $2LT$ updated LLMs during one clock cycle. These L PUsAs need to read two consecutive data words from L-MEM in order to generate $4TL$ LLMs. For the proposed list decoder architecture, as shown in Fig. 7, $L$ write buffers (wBUFs) are employed to store half of $4TL$ LLMs generated by L PUsAs. Once the remaining LLMs are computed, the output selection (OSel) module formats these LLMs in the way that these LLMs are stored in the L-MEM.

Since all the LLMs belonging to $\mathbf{P}_\lambda = (P_0, \lambda, P_1, \lambda, \cdots, P_{L-1}, \lambda)$ with $\lambda > \lambda_0$ are stored in a single data word in L-MEM and the computing of LLMs belonging to $\mathbf{P}_{\lambda+1}$ can only take place once $\mathbf{P}_\lambda$ are updated, an additional clock cycle is needed to read out the LLMs within $\mathbf{P}_{\lambda}$ that have been just written into the L-MEM. This will increase the delay and decrease the throughput of the proposed list decoder. As shown in [3], the bypass buffer, rBUF, is used to temporarily store the messages written into the L-MEM and eliminate the extra read cycle.

C. Path Pruning Unit

For the CA-SCL algorithm, once the path metric computation of decoding step $i$ is finished, each current decoding path splits into two sub decoding paths. However, the list decoder keeps at most $L$ decoding paths. For the proposed list decoder architecture, a path pruning unit (PPU) is proposed to prune the split decoding paths in an efficient way. As shown in Fig. 7, the proposed PPU contains two sub modules, the maximum value filter (MVF) and the crossbar control signals generator (CCG). The MVF generates $L$ path indices $a_0, a_1, \cdots, a_{L-1}$ and $L$ associated decoded bits $c_0, c_1, \cdots, c_{L-1}$. For a current decoding path $l$, both the path metric and partial sum computations will be based on the LLMs and partial sums within decoding path $a_l$, and the decoded code bit for $u_{l,i}$ is $c_i$, $a_l$ and $c_l$ for $l = 0, 1, \cdots, L-1$ are used to control the copying of partial sums and checksums.

1) Maximum Values Filter: Taking list size $L = 8$ as an example, the corresponding MVF architecture is proposed in Fig. 10, where the MVF consists of a bitonic sequence generator (BSG) and a stage of compare and select (CAS) modules. The BSG has 16 inputs ($D_0, D_1, \cdots, D_{15}$) and 16 outputs ($S_0, S_1, \cdots, S_{15}$). Each of them consists of three parts: the path metric, the associated list index and decoded bit. The width of each input and output is $z = x_1 + x_2 + 1$, where $x_1 = t + n$ is the number of bit used to quantize a path metric and $x_2 = \log_2 L$ is the number of bits used to represent a list index.

Each stage of the BSG consists of $\frac{L}{2}$ increase-order sorters (ISs) and $\frac{L}{2}$ decrease-order sorters (DSs), which are shown in Fig. 11(a) and Fig. 11(b), respectively. Both the IS and DS have two inputs and two outputs. For $k = 0, 1$, $S_{I_k} = (L R_{k, l_k}, b_k)$ and $L R_{k, l_k}$ and $b_k$ denote the path metric and its corresponding list index and decoded bit. Besides, $S_{O_k} = (L R_{k, l_k}', b_k')$ for $k = 0, 1$. The IS reorders the inputs such that path metric $L R_{0} \leq L R_{1}$. The output of the comp-max module is 1 when $L R_{0} > L R_{1}$. The DS reorders the inputs such that $L R_{0} \geq L R'_{1}$ and the output of the comp-min module is 1 when $L R_{0} < L R_{1}$.

The BSG reorders the inputs based on the magnitude of path metrics. Let $L S_r (r = 0, 1, \cdots, 15)$ denotes the associated path metric of output $S_r$, the path metrics of the 16 outputs satisfy:

\begin{equation}
L S_0 \leq L S_1 \leq \cdots \leq L S_7, \quad (7)
\end{equation}

\begin{equation}
L S_8 \geq L S_9 \geq \cdots \geq L S_{15}. \quad (8)
\end{equation}

It is proved in [18] that the 8 maximum values among $L S_r$’s are $\max(L S_r, L S_{r+8})$ for $r = 0, 1, \cdots, 7$. Hence, a stage of CAS modules is appended at the outputs of BSG shown in Fig. 10, where CSA$_r$ takes $S_r$ and $S_{r+8}$ as inputs. This stage of CAS modules produce the outputs $O_l = (a_l, c_l)$ for $l = 0, 1, \cdots, L-1$. As shown in Fig. 11(c), the CAS module compares the path metrics of its two inputs and selects the corresponding list index and bit value whose associated path metric is larger.

![Fig. 10. Maximum values filter architecture](image-url)

The metric sorter in [15] has the same function as that of the proposed MVF. We compare the proposed bitonic sorter based MVF module with the metric sorter [15] in terms of area and...
TABLE III

| process | \( n \) | 10  | 15  |
|---------|------|-----|-----|
| \( CPD \) (ns) | TSMC 90nm CMOS | 0.555 | 0.588 |
| regular PU array area (\( \mu m^2 \)) | 27650 | 55259 | 113902 | 225418 | 159051 | 308640 | 602509 | 1212359 |
| fine grained PU array area (\( \mu m^2 \)) | 19280 | 34131 | 59048 | 101377 | 194434 | 190615 | 334927 | 594048 |
| area saving | 30% | 38% | 48% | 55% | 30% | 38% | 44% | 51% |

TABLE IV

| process | metric sorter | proposed MVF |
|---------|---------------|--------------|
| \( L \) | 90nm CMOS | 90nm CMOS |
| \( CPD \) (ns) | 0.45 | 0.85 | 1.8 | 4.1 | 9.6 | 5.2 | 3.7 | 5.2 |
| area (\( \mu m^2 \)) | 1995 | 9199 | 47119 | 241633 | 1392617 | 1580 | 8401 | 30814 |
| area saving | – | 20% | 8% | 34% | 59% | 34% | 59% | 71% |

critical path delay (CPD) under different list sizes. As shown in Table [IV] both modules are synthesized under the TSMC 90nm CMOS technology. The RTL files of the metric sorter are provided by the authors of [15]. As shown in Table [IV] the proposed MVF module is more suitable for large list sizes. For list size \( L = 2 \) to 32, the proposed MVF achieves 8% to 77% area saving. The proposed MVF architecture achieves area saving because the comparator dominates the area for the metric sorter and the MVF modules. For list size \( L \), the metric sorter needs \( N_{MS} = L(2L - 1) \) comparators, while the proposed MVF module needs \( N_{MVF} = 1 + 2 + \cdots + \log_2 L = \frac{L}{2}((\log_2 L)^2 + \log_2 L + 2) \) comparators. When \( L \) is large, \( N_{MS}/N_{MVF} \approx \frac{4L}{\log_2 L} \). Clearly, our MVF module needs fewer comparators.

When \( L = 2, 4, 8 \), compared with the metric sorter, the proposed MVF has longer CPD while achieving area saving. However, the longer delay for the MVF is inconsequential because it is not in the critical path for the decoder architecture when \( L \leq 8 \). When \( L = 16, 32 \), the proposed MVF is better than the metric sorter in terms of both area and CPD. Thus, the proposed MVF is more suitable for large list sizes.

2) Crossbar Control Signal Generator: Due to the lazy copy method [15], when decoding path \( l \) needs to be copied to decoding path \( l' \), instead of copying LLMs from path \( l \) to path \( l' \), the index references \( (r_1 = (r_1[n - 1], \ldots, r_1[0]) \) shown in Algorithm [2] to LLMs of path \( l \) are copied to path \( l' \). For decoding path \( l \), when PUA1 is computing updated LLMs in \( P_l,\lambda \), the crossbar (CB) module shown in Fig. [7] selects input LLMs from decoding path \( r_1[\lambda - 1] \). The CB can be implemented with L-to-1 multiplexors.

![Fig. 11. (a) Architectures of IS (b) Architectures of DS (c) Architectures of CAS (z = x1 + x2 + 1)](image)

The crossbar control signal (CCG) generator computes the control signals of CB, cc0, cc1, \cdots, ccL − 1, where the \( l \)-th output of CB is connected to the cc0-th input. An example of the CCG is shown in Fig. [12] where the proposed CCG consists of \( Ln \) basic update units, \( U_{l,\lambda} \)'s (\( l = 0, 1, \cdots, L - 1 \) and \( \lambda = 0, 1, \cdots, n - 1 \)). As shown in Fig. [12]b, the proposed \( U_{l,\lambda} \) contains an index register \( R_l[\lambda] \) which stores \( r_1[\lambda] \), where \( r_1 \) is the message updating reference index array for decoding path \( l \).

When \( u_i \) is being decoded, the multiplexors in Fig. [12]b are configured so that \( w_{i,\lambda} = r_{ai,\lambda} \) when \( \lambda < \phi(i) \) and \( w_{i,\lambda} = l \) otherwise. \( \phi(i) \) is defined in Section [II-C]. When \( P_l,\lambda \) needs to be computed, the \( \lambda \)-th inputs of the MUX in Fig. [12]a are selected as the outputs of CCG. Once a round of metric computation is finished, \( w_{i,\lambda} \) is written into its corresponding
D. Partial Sum Update Unit and the CRC Unit

In this paper, a parallel partial sum update unit (PSU) is proposed to provide the partial sum inputs to L PUs when performing the G computation. Compared with the PSU in [3], [15], which needs $N - 1$ single bit registers for a decoding path, our PSU needs only $\frac{N}{2} - 1$ single register bits.

Take $N = 2^n$ as an example, the architecture of PSU, which computes the partial sums for decoding path $l$, is shown in Fig. 13 where stage_2 and stage_2 have one and two elementary update units (EUs), respectively. $r_{1,3,0}$, $r_{1,2,0}$, $r_{1,1,1}$ shown in Fig. 13 are single bit registers. $c_l = a_{l,3}$ is the binary input of the PSU. There are three partial sum outputs: $b_{l,3}$, $b_{l,2}$ and $b_{l,1}$ with a width of 1, 2 and 4 bits, respectively. When the LLMs in $P_{l,\lambda}$ need to be updated with the $G$ computation, $b_{l,\lambda}$ is the corresponding partial sum input. The architectures of PSU for other code lengths can be derived from the architecture in Fig. 13. For a polar code with length $N = 2^n$, the corresponding PSU contains $n - 1$ stages: stage_2, stage_2, ..., stage_2, where stage_2 has $2^{n-j}$ EUs for $n \geq j \geq 2$.

When bit index $i$ is even, $c_l$ is stored in $r_{l,0}$, and other registers keep their current values unchanged. When bit index $i$ is odd, bit registers in stage_2, stage_2, ..., stage_2 are updated with their corresponding input. When decoding path index $l \neq a_i$, the updated partial sums of decoding path $l$ should be computed based on the register values in PSU. The switch network (SW) shown in Fig. 13 selects the corresponding bit register value from PSU. The width of the input signal $B_{l,j,k} = \{r_{0,j,k}, r_{1,j,k},\ldots, r_{L-1,j,k}\} \setminus \{r_{i,j,k}\}$ is $L - 1$ bits.

The CRC unit (CRCU) checks whether a codeword passes the CRC. Suppose an $h$-bit CRC checksum is used, the architecture of the CRCU for decoding path $l$ is shown in Fig. 14, where the generation polynomial for the CRC checksum generation is $p(x) = x^h + p_{h-1}x^{h-1} + \cdots + p_1x + 1$. The proposed CRCU is based on a well known serial CRC computation architecture [19]. If the polynomial coefficient $p_k = 0$, the corresponding XOR gate and multiplexer are removed. During the decoding of the first $N - h$ code bits, the control signal $shift_l = 0$ and CRCU computes the $h$-bit checksum of these code bits. The checksum is stored in bit registers $d_{l,0}, d_{l,1}, \cdots, d_{l,h-1}$ shown in Fig. 14. Once the checksum computation is finished, the checksum is compared with the remaining $h$ decoded code bits and the control signal $shift_l = 1$. The checksum and the remaining $h$ code bits are compared bit by bit. The comparison result is stored in the register $cs_l$. The decoded codeword for decoding path $l$ passes the CRC only if $cs_l = 0$. The SW module shown in Fig. 14 is the same as that used in the partial sum computation unit PSU. When $l \neq a_i$, the SW module selects $d_{a_i,k}$ for $k = 0, 1, \cdots, h - 1$.

E. Decoding Cycles

For the proposed list decoder, pipeline registers can be inserted in the paths that pass through the MVF. Let $N_C$ denote the number of cycles spent on the decoding of one codeword. For list decoder architectures based on partial parallel processing [3],

$$N_C = 2N + N \log_2 \frac{N}{4T} + n_p R N,$$

(9)

where $N, T, n_p, R$ denote the block length, the number of PUs per decoding path, the number of pipeline registers inserted in the path pruning unit and the code rate, respectively.

The corresponding throughput $TP = \frac{LNR}{N_C}$, where $f$ is the frequency of the list decoder. The latency $TD = \frac{N_C}{f}$.

F. Scalability of the Proposed List Decoder Architecture

Based on the FER results, our list decoder architecture is more suitable for list sizes since a larger $L$ leads to more performance gain for the CA-SCL algorithm. For the current list decoder architecture in [15], there are two issues when $L$ increases.

- The message memories of the list decoder in [15] are built with registers due to the non-uniform quantization of the logarithm domain messages. Besides, the message memories dominate the whole decoder area. As a result, the memory area of the list decoder is linearly proportional to list size $L$. For a larger list size, the list decoder architecture in [15] will suffer from large area and high power consumption due to its register based memory.
- As shown in Table IV when the list size grows, the metric sorter suffers from large area and long critical path delay, which results in a slower clock frequency of the list decoder. If multiple pipelines are inserted in the metric sorter, the number of cycles for decoding one codeword also increases as shown in Eq. (9).

For our list decoder architecture, these two issues are solved as follows.

- The proposed memory architecture is more area efficient compared to register based memory. Besides, the proposed memory architecture offers a tradeoff between data throughput and memory area. The register based memory [15] remains almost unchanged when the number of PUs changes. However, for the proposed memory architecture, the number of PUs affects the depth-width ratio of the message memories. Hence, the area of message memory can be tuned by varying the number of PUs. Reducing the number of PUs will increase the depth of message memories, which is more area efficient. On the
other hand, reducing the number of PUs will also increase the number of cycles used on decoding one codeword and decrease the data throughput.

- When the list size increases, the proposed MVF is more area efficient and has a shorter critical path delay compared with the metric sorter \([15]\).

As shown in Eq. (6), the depth of the largest LLM memory instance will increase when \(N = 2^n\) increases. Hence, the area efficiency will be improved when \(N\) increases. As a result, our list decoder architecture is more suitable for large block length \(N\).

\[ \text{V. IMPLEMENTATION RESULTS} \]

In this paper, our list decoder architecture has been implemented with list size \(L = 2\) and \(4\) for a rate 1/2 polar code with \(N = 1024\). For each list size, two list decoders with the numbers of \(T = 8\) and 16 PUs, respectively, are implemented and synthesized under a TSMC 90nm CMOS technology. For the L-MEM within each of our list decoder, each sub memory is compiled with a memory compiler if its depth is large enough. Otherwise, the sub memory is built with registers. For all implemented decoders, each channel LLM is quantized with 4 bits in order to achieve near floating point decoding performance. For our list decoders with \(L = 2\) and \(4\), one stage of pipeline registers is used. Since the synthesis results in \([15]\) were based on a UMC 90nm technology, the authors of \([15]\) have generously re-synthesized their decoder architecture using the TSMC 90nm technology. We list both synthesis results and the re-synthesized results provided by the authors of \([15]\) in Table \(V\). To make a fair comparison, we focus on the re-synthesized results.

Based on the implementation results in Table \(V\) we have the following observations.

- The decoder architecture in \([15]\) has higher a throughput than our list decoder architecture. The reason is that the decoder architecture in \([15]\) employs register based memory while the proposed list decoder architecture employs register file (RF) based memories. The read and write delays of an RF are larger than those of a register based memory, respectively.

- On the other hand, our list decoder architecture is more area efficient based on the area comparisons shown in Table \(V\). In terms of the hardware efficiency, our list decoder architecture is better than that in \([15]\). For list decoders with the same \(L\) and \(T\) values, compared with the decoder of \([15]\), our list decoder architecture achieves 1.24 to 1.83 times of hardware efficiency.

Our list decoder is implemented for the \(N = 1024\) polar code because the same block length is used in \([15]\). For larger block length or larger list size, our advantage in hardware efficiency is expected to be greater due to more area efficient LLM memory.

Since the CA-SCL algorithm helps to select the correct one from \(L\) possible decoded codewords \([5]\), the decoding performance of the CA-SCL algorithm is better than that of the SCL algorithm with the same list size in \([15]\). As shown in Fig. \(2\) the proposed CA-SCL decoders in Table \(V\) outperform the SCL decoders in Table \(V\). We note that the number of PUs has no impact on the error performance of the SCL and CA-SCL decoders.

As shown in Fig. \(2\) for the CA-SCL algorithm, increasing the list size results in noticeable decoding gain according to our simulations. As shown in Fig. \(1\), increasing the list size of the SCL algorithm leads to negligible decoding gain especially in high SNR region. For the CA-SCL algorithm, the choice of list size \(L\) depends on the tradeoff between

\[ \begin{array}{|c|c|c|c|}
\hline
\text{algorithm} & \text{CA-SCL} & \text{SCL} \\
\hline
\text{list size } L & 2 & 4 & 2 & 4 \\
\hline
\text{total number of PUs } L T & 16 & 32 & 32 & 64 & 16 & 32 & 32 & 64 & 128 & 256 \\
\hline
\text{channel message quantization bits } t & 4 & 4 & 4 & 4 \\
\hline
\text{process} & \text{TSMC 90nm} & \text{UMC 90nm} \\
\hline
\text{frequency (MHz)} & 500 & 500 & 454 & 476 & 609 & 757 & 684 & 694 & 459 & 314 \\
\hline
\text{total area (mm}^2\text{)} & 0.406 & 0.553 & 0.810 & 1.132 & 1.114 & 1.174 & 2.181 & 2.197 & 1.60 & 3.53 \\
\hline
\text{\(N_C\)} & 3200 & 2816 & 3200 & 2816 & 3200 & 2816 & 3200 & 2816 & 2592 & 2592 \\
\hline
\text{latency (ms)} & 6.4 & 5.63 & 7.04 & 5.91 & 4.37 & 3.71 & 4.67 & 4.05 & 5.64 & 8.25 \\
\hline
\text{throughput (Mbp/s)} & 160R^4 & 181R^4 & 145R^4 & 173R^4 & 224R^4 & 275R^4 & 219R^4 & 252R^4 & 181R^4 & 124R^4 \\
\hline
\text{hardware efficiency (Mbps/mm}^2\text{)} & 394R^4 & 327R^4 & 179R^4 & 152R^4 & 201R^4 & 234R^4 & 100R^4 & 114R^4 & 113R^4 & 35R^4 \\
\hline
\text{normalized hardware efficiency} & 1.83 & 1.30 & 1.67 & 1.24 & 1 & 1 & 1 & 1 & - & - \\
\hline
\end{array} \]

\(\dagger\) Original synthesis results based on a UMC 90nm technology in \([15]\).

\(\ddagger\) Synthesis results based a TSMC 90nm technology, provided by the authors of \([15]\).
error performance and decoding complexity. Better error performance can be achieved by increasing the list size \( L \). For the SCL algorithm, we need to find the threshold value \( L_T \), where little further decoding gain is achieved by employing a list size \( L > L_T \). For the SCL algorithm, the feasible list size should be no greater than \( L_T \) and satisfy the error performance requirement.

Due to the serial nature of the successive cancelation method, the SC based decoders and its list variants suffer from long decoding latency. In terms of throughput, the throughput of SC based decoders is expected to be lower than BP based decoders, since the BP algorithm for polar codes has a much higher parallelism. On the other hand, the BP algorithm for polar codes still suffers from inferior finite length error performance [9], [20]. Current simulation results [9] show that the error performance of the BP algorithm for polar codes is similar to that of SC algorithm, but worse than those of the SCL and CA-SCL algorithms.

VI. CONCLUSION

In this paper, an efficient list decoder architecture has been proposed for polar codes. The proposed decoder architecture achieves higher hardware efficiency and better error performance than previous list decoder architectures.

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