A Design Methodology for Efficient Implementation of Deconvolutional Neural Networks on an FPGA

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Abstract—In recent years deep learning algorithms have shown extremely high performance on machine learning tasks such as image classification and speech recognition. In support of such applications, various FPGA accelerator architectures have been proposed for convolutional neural networks (CNNs) that enable high performance for classification tasks at lower power than CPU and GPU processors. However, to date, there has been little research on the use of FPGA implementations of deconvolutional neural networks (DCNNs). DCNNs, also known as generative CNNs, encode high-dimensional probability distributions and have been widely used for computer vision applications such as scene completion, scene segmentation, image creation, image denoising, and super-resolution imaging. We propose an FPGA architecture for deconvolutional networks built around an accelerator which effectively handles the complex memory access patterns needed to perform strided deconvolutions, and that supports convolution as well. We also develop a three-step design optimization methodology that systematically exploits statistical analysis, design space exploration and VLSI optimization. To verify our FPGA deconvolutional accelerator design methodology we train DCNNs offline on two representative datasets using the generative adversarial network method (GAN) run on Tensorflow, and then map these DCNNs to an FPGA DCNN-plus-accelerator implementation to perform generative inference on a Xilinx Zynq-7000 FPGA. Our DCNN implementation achieves a peak performance density of 0.012 GOPs/DSP.

Keywords—FPGA, Deconvolution, Generative Model, Acceleration

I. INTRODUCTION

Deep learning algorithms have shown extremely high performance on machine learning tasks. In particular, convolutional neural networks (CNNs) have become the state-of-the-art for applications like computer vision and audio recognition [1] [2] [3]. To address the increasing demand for applications that require running neural network algorithms in real time on embedded devices, various high performance hardware platforms for discriminative CNN implementations have been proposed, including the use of distributed GPUs or customized accelerators like FPGAs and ASICs [4] [5]. In particular, FPGA-based accelerators have been proposed because they have lower latency and consume less power than GPUs while being more flexible and configurable than ASICs [6] [7].

However, current FPGA accelerators focus on enhancing the performance of convolutional neural networks (CNNs), not deconvolutional neural networks (DCNNs). Unlike discriminative CNNs that effectively “downsample” the input to produce classification [1], DCNNs are generative models capable of generating data by “upsampling” the input using deconvolution layers [8]. There are many applications of DCNNs, including multi-modal data modeling [9], super resolution [10] and image-to-image translation [11] [12] (see Fig. 1). Such applications motivate us to design an FPGA-based accelerator with the ability to execute deconvolution operations with high throughput and low cost.

There are several issues that must be addressed to design an FPGA-based deconvolution accelerator. First, a direct translation of CPU-optimized deconvolution algorithms to an FPGA will generally lead to inefficient implementations. A suitable adaptation of the deconvolution operation to a hardware substrate such as FPGA is therefore necessary in order to achieve high performance with low implementation complexity. In addition, although recent research shows that discriminative CNNs are robust to low bitwidth quantization [13] [14], it is important to be able to systematically study the effects of such bitwidth reductions on the quality of inference from a generative model such as DCNN implemented with finite precision on FPGA. Thus it is necessary to use metrics which quantify the effects of such approximations in DCNNs in order to achieve an efficient design optimized for performance and power.

To address the issues described above, we make the following contributions in this paper. 1) We create a deconvolution accelerator with reverse looping and stride hole skipping to efficiently implement deconvolution on an FPGA, where our proposed solution, in a nontrivial way, reuses the same computational architecture proposed for implementing a convolution accelerator in [6]. 2) We propose a three-step procedure to design the deconvolution accelerator as follows. A) At the highest design level, we train DCNNs using...
the generative adversarial network method (GAN) [15] and use statistical tests to quantitatively analyze the generative quality under different bitwidth precisions to select the most cost-efficient bitwidth. B) We use the routine model proposed in [6] to explore the design space in order to find the set of high-level constraints that achieves the best tradeoff between memory bandwidth and accelerator throughput. C) We use loop unrolling and pipelining, memory partitioning, and register insertion to further optimize performance. 3) We validate our procedure via two implementations on a Xilinx Zynq-7000 FPGA.

The rest of this paper is organized as follows: Section II provides background on the DCNN and the deconvolution layers. Section III presents our methodology for efficiently implementing an FPGA-based deconvolution accelerator. Section IV explains our three-step design methodology. Section V shows our experimental results. Section VI concludes the paper.

II. DECONVOLUTIONAL NEURAL NETWORK

A deconvolutional neural network (DCNN) converts latent space representations to high-dimensional data similar to the training set by applying successive deconvolution operations in multiple layers [16]. The latent space contains low-dimensional latent variables that provide a succinct (“conceptual”) representations of the possible outputs (e.g. an image). Thus a latent variable may correspond to “chair” with low-dimensional latent variables that provide a succinct representation of the data. The latent space contains low-dimensional latent variables that provide a succinct representation of the data.

![Fig. 2. A DCNN that generates realistic 64x64 indoor scenes based on the use of four deconvolution layers that was trained on the Large-scale Scene Understanding (LSUN) Dataset [17] [18] (Image is taken and adapted from reference [17].)](image)

Fig. 2 shows how a typical deconvolution layer works, where $S$ and $P$ denote the chosen values of stride and padding respectively for a given layer. The pseudo code of a deconvolution layer as implemented in CPU is shown in Algorithm 1 which uses the loop variables defined in Fig. 4.

Algorithm 1 Deconvolution in CPU

```plaintext
1: procedure DECONVOLUTION
2: for $i_c = 0$ to $I_c - 1$ do
3:     for $i_h = 0$ to $I_H - 1$ do
4:       for $i_w = 0$ to $I_W - 1$ do
5:         for $o_c = 0$ to $O_C - 1$ do
6:           for $o_h = 0$ to $K - 1$ do
7:             for $o_w = 0$ to $K - 1$ do
8:               $a_h = S × i_h + k_h - P$
9:               $a_w = S × i_w + k_w - P$
10:              $out[o_c][o_h][o_w] ← (in[i_c][i_h][i_w] × kernel[o_c][o_h][o_w])$
```

By convention we use capital letters e.g. $O_H$ to denote specific parameters of the DCNN whereas small letters e.g. $o_h$ to denote its corresponding loop variable.
of additional hardware blocks which creates overhead or communicating with a host processor which can increase system latencies thereby precluding real-time applications.

Unfortunately Eq. 5 generally results in a non-integer value for \( o_h \), which is invalid [19]. One way to address this problem would be to monitor \( i_h \) so that fractional values can be discarded. However this would consume additional hardware resources and create unnecessary latencies in the system.

### B. Stride Hole Skipping

In this section, we propose a technique called stride hole skipping to ensure \( i_h \) of Eq. 5 is an integer. Toward this end, we recast \( o_h \) in terms of two new variables, \( o'_h \) and \( f_h \) and show that this leads to an effective way of solving the aforementioned problem. First note that a sufficient condition for \( i_h \) to be an integer in Eq. 5 is:

\[
(o_h + P - k_h) \mod S = 0 \tag{6}
\]

Assuming \( \frac{O_H}{S} \) is an integer (\( O_H \) is defined in Eq. 1), we can recast \( o_h \) as follows:

\[
o_h = S \times o'_h + f_h, \quad f_h \in \{0, 1, ..., S - 1\} \tag{7}
\]

Using the definition of \( o_h \) in Eq. 6 we can recast the sufficient condition Eq. 6 in terms of \( f_h \) as below:

\[
(f_h + P - k_h) \mod S = 0 \tag{8}
\]

Eq. 7 implies that we can rewrite \( f_h \) as:

\[
f_h = S - ((P - k_h) \mod S) \tag{9}
\]

This can be verified by plugging in Eq. 9 into Eq. 8 which yields the following identity:

\[
(P - k_h - (P - k_h) \mod S) \mod S = 0 \tag{10}
\]

To prevent \( f_h \) from taking a value equal to \( S \), we enforce the additional condition:

\[
f_h = (S - ((P - k_h) \mod S)) \mod S \tag{11}
\]

By using Eq. 11 to choose values for \( f_h \), we can ensure that \( o_h \) computed from Eq. 7 meets the condition in Eq. 6. Therefore we can avoid the previously mentioned issue of discarding fractional values of \( i_h \) that we would otherwise encounter from a direct application of Eq. 5. The pseudo code for deconvolution on FPGA is shown in Algorithm 2.

#### Algorithm 2 Our FPGA Implementation of Deconvolution

1. **procedure** REVERSEDECONVOLUTION
2.  
3.       \( \text{for } k_h = 0 \text{ to } K - 1 \) do
4.  
5.       \( \text{for } k_w = 0 \text{ to } K - 1 \) do
6.  
7.       \( \text{for } o'_h = 0 \text{ to } \frac{T_{O_H}}{S} - 1 \) do \( \triangleright \) loop \( T_{O_W} \)
8.  
9.       \( \text{for } o_c = 0 \text{ to } \frac{T_{O_C}}{S} - 1 \) do \( \triangleright \) loop \( T_{I_C} \)
10.  
11.   \( \text{for } i_c = 0 \text{ to } \frac{T_{I_O}}{S} - 1 \) do \( \triangleright \) loop \( T_{I_W} \)
12.  
13.   \( \text{COMPUTE}(k_h, k_w, o'_h, o_c, i_c) \)
14.  
15.   \( f_h \leftarrow (S - ((P - k_h) \mod S)) \mod S \)
16.  
17.   \( f_w \leftarrow (S - ((P - k_w) \mod S)) \mod S \)
18.  
19.   \( o_h = o'_h \times S + f_h \)
20.  
21.   \( o_w = o'_w \times S + f_w \)
22.  
23.   \( i_h \leftarrow (o_h - k_h)/S \)
24.  
25.   \( i_w \leftarrow (o_w - k_w)/S \)
26.  
27.   \( \text{out}[i_c][i_h][i_w] \leftarrow \text{in}[i_c][i_h][i_w] \times \text{kernel}[o_c][i_c][k_h][k_w] \)

### IV. THREE-STEP DESIGN METHODOLOGY

#### A. Statistical Analysis

It is important to study the effect of bitwidth reduction on the quality of inference from the generative model. To find out the most cost-efficient bitwidth for DCNNs, we fix \( T_{O_H}, T_{O_W}, T_{O_C}, T_{I_C} \) and study the trade-off between generative quality and implementation complexity over a range of bitwidths using statistical analysis. Quantifying
generative models using traditional techniques such as Kullback-Leibler divergence and log-likelihood are not feasible in high-dimensional settings such as the typical setting deconvolutional neural networks are used in. To overcome this drawback, we apply nonparametric goodness of fit testing. Specifically, we apply the Relative Maximum Mean Discrepancy (RMMD) Test proposed by [20] to measure and compare the performance of our system at different bitwidths.

The RMMD is an extension of the Maximum Mean Discrepancy (MMD) two sample test proposed by [21]. Given samples \( \{X_i\}_{i=1}^m \) and \( \{Y_i\}_{i=1}^n \) from distributions \( P_x \) and \( P_y \) the MMD test statistic is given by:

\[
\text{MMD}^2(X,Y) = \frac{1}{m(m-1)} \sum_{i=1}^m \sum_{j=1}^m k(x_i, x_j) + \frac{1}{n(n-1)} \sum_{i=1}^n \sum_{j=1}^n k(y_i, y_j) - \frac{2}{mn} \sum_{i=1}^m \sum_{j=1}^n k(x_i, y_j)
\]

the null hypothesis \( H_0 : P_x = P_y \) is tested versus alternative \( H_1 : P_x \neq P_y \). In the above equation, \( k \) is the Radial Basis Function given by:

\[
k(x,y) = \exp(||x - y||)
\]

The RMMD test builds upon the standard MMD framework by computing the MMD test statistic between two pairs of distributions. Given samples \( \{X_i\}_{i=1}^m \), \( \{Y_i\}_{i=1}^n \), and \( \{Z_i\}_{i=1}^r \) respectively from the training data, low-bitwidth DCNN, and full-precision DCNN, RMMD tests the null hypothesis \( H_0 : \text{MMD}^2(X,Y) < \text{MMD}^2(X,Z) \) against the alternative \( H_1 : \text{MMD}^2(X,Z) < \text{MMD}^2(X,Y) \). [20] shows that the p-values for testing \( H_0 \) against \( H_1 \) are given by:

\[
p \leq \Phi\left(\frac{\text{MMD}^2(X_m,Y_n) - \text{MMD}^2(X_m,Z_r)}{\sqrt{\sigma_{XY}^2 + \sigma_{XZ}^2 - 2\sigma_{XY} \sigma_{XZ}}}\right)
\]

where \( \Phi \) is the Normal Cumulative Distribution Function. The p-value in the above equation indicates the probability that, based on the observed samples, the distribution based on the low bitwidth DCNN is closer to the training data than the distribution based on the full precision DCNN is to the training data. Using this interpretation:

- a p-value > 0.5 indicates the low bitwidth DCNN is more similar to the training data
- a p-value < 0.5 indicates the full precision DCNN is more similar to the training data

B. Roofline Analysis

The generative quality is determined by choosing the optimal bitwidth using the previously described procedure. Following this we turn to further increasing the throughput by optimizing with respect to \( T_{OH}, T_{OW}, T_{OC}, \) and \( T_{IC} \), which are the height, width, channel size of output block, and channel size of input block respectively (see Fig. 5). This is done using roofline analysis [6]. Fig. 7 shows an example roofline plot where the X axis denotes the number of operations per memory access and Y axis denotes the number of operations per cycle.

![Fig. 7. Roofline Model, adopted from [6]](image)

In this drawing, A, B and C correspond to designs of accelerator with different values of \( T_{OH}, T_{OW}, T_{OC}, T_{IC} \). Design A transfers too much data, so computation speed is low, and therefore falls well beneath the computation roof. Design B lies well beneath the bandwidth roof, which means the system performance is dominated by memory transfers. Design C is more efficient than A and B with its balance between computation speed and memory bandwidth. This technique is described in [6] and is used for the design of convolution accelerators. We apply roofline analysis to design deconvolution accelerator and estimate the computation to communication ratio (CTC) and computational roof (CR) for a given layer.

1) Computation to Communication Ratio: Let \( \alpha_{in}, \alpha_w, \alpha_{out} \) and \( B_{in}, B_w, B_{out} \) denote the trip counts and buffer sizes of memory accesses to input/output feature maps, weights, respectively. The CTC is given by:

\[
\text{CTC} = \frac{\text{total number of operations}}{\text{total amount of external memory access}} = \frac{2 \times I_C \times O_C \times I_H \times I_W \times K^2}{\alpha_{in} B_{in} + \alpha_w B_w + \alpha_{out} B_{out}}
\]

(12)

\[
\alpha_{out} = \frac{O_C}{T_{OC} / T_{OH}}, \alpha_{in} = \alpha_w = \frac{I_C}{T_{IC}}
\]

(13)

\[
B_{in} = T_{IC} \left( \frac{T_{OH} + K}{S} \right) \left( \frac{T_{OW} + K}{S} \right)
\]

(14)

\[
B_{out} = T_{OC} T_{OH} T_{OW}, \quad B_{weight} = T_{OC} T_{IC} K^2
\]

(15)

\[
0 \leq B_{in} + B_w + B_{out} \leq \text{BRAM capacity}
\]

(16)

2) Computation Roof: Let PD denotes the pipeline depth and II is the number of cycles between the start of each loop iteration \( T_{OW} \), the CR is given by:

\[
\text{CR} = \frac{\text{total number of operations}}{\text{number of execution cycles}} = \frac{2 \times I_C \times O_C \times I_H \times I_W \times K^2}{\alpha_{in} R^2 T_{OH} (PD + II(T_{OW} - 1))}
\]

(17)

where

\[
\begin{align*}
0 & \leq T_{OC} T_{IC} \leq (# \text{ of DSPs}) \\
0 & < T_{IC} \leq I_C \\
0 & < T_{OC} \leq O_C \\
0 & < T_{OH} \leq O_H \\
0 & < T_{OW} \leq O_W
\end{align*}
\]
Note that $0 \leq T_{Ox} T_{IC} \leq (\# \text{of DSPs})$ will not hold true when the bitwidth is greater than 18, because the maximum bitwidth of the multipliers used in our implementation is 18-bit [22]. Since we use a bitwidth of 12 in all our experiments this constraint is therefore valid.

C. VLSI Level Optimization

1) Loop Unrolling and Pipelining: Loop unrolling is a key technique of high level synthesis [23]. It works by generating parallel hardware to accelerate FPGA program execution. The innermost loop $T_{Ox}$ and $T_{IC}$ in Algorithm 2 are unrolled and can be executed in a constant amount of cycles $P$, which forms the processing engine as shown in Fig. 8. We also pipeline the loop $T_{Ow}$ with carried dependency of 2.

Fig. 8. Processing Engine

2) Register Insertion: The critical path length and pipeline interval are constrained by the on-chip local memory bandwidth, especially when the size of the processing engine is large. To further improve performance, we insert registers to economize local memory bandwidth, which is illustrated in Fig. 9.

Fig. 9. Insert register to reduce local memory (BRAM) writes

V. Evaluation

A. Statistical Analysis

Previous work such as that described in [24] has shown the effectiveness of using high-dimensional nonparametric tests to determine optimal parameters for generative inference in hardware. For designing the deconvolution accelerator we follow a similar approach and use the RMMD test framework outlined in Section IV A to choose the optimal bitwidth for our system. For this purpose, we trained two DCNNs through the method described in [17] on the MNIST and CelebA Human Face datasets [25]. To study the trade-off between generative quality and system complexity over a range of bitwidths, we determine p-value $\times$ minimum slack and p-value/power as a function of bitwidths. The two curves are shown in Fig. 10. Both curves peak at bitwidth 12, which we take to be a good choice because it represents a high p-value (generative quality) with a low power consumption and high minimum slack.

Fig. 10. Approximate concave curves based on trade-off between generative quality and implementation complexity.

B. Hardware System

We implemented the deconvolution accelerator IP with Vivado HLS (v2016.2). We use $\text{ap\_fixed.h}$ from Vivado Math Library to implement fixed point arithmetic operations with arbitrary bitwidth precision, and use $\text{hls\_stream.h}$ & $\text{ap\_axi\_sdata.h}$ to model streaming data structure. The hardware system is built on a Zynq-7000 FPGA XZ7020 with Vivado Design Suite and Xilinx SDK. The FPGA 7Z020 is programmed with our accelerator IP and the ARM processor is used to initialize the accelerator, set parameters, and transfer data for each layer. An overview of the implementation block diagram is in Fig. 11.

Fig. 11. Overview of Implementation Block Diagram.

C. Experimental Results

Fig. 12 shows some generated faces and digits from our trained DCNNs. Fig. 13 shows the output of DCNNs under different bitwidths for the same input. Visually evaluating degradation of image quality is only feasible in the cases of extremely low bitwidth such as 8 bits. Our proposed methodology provides an analytical framework for quantifying the trade-off between image quality and implementation complexity over a range of bitwidths.

Fig. 14 shows all constraint-admissible design solutions for the first layer of our CelebA DCNN, where the best design is
In this work, we develop an FPGA-based deconvolution accelerator for deconvolutional neural networks and propose a three-step design methodology which first uses statistical analysis to find out the most cost-efficient bitwidth, then explore the design space with roofline model [6] and use VLSI optimization methods to produce the final design. Finally, we implement our method on a Zynq-7000 FPGA and realize a performance density of 0.012 GOPs/DSP.

VI. CONCLUSION

In this work, we develop an FPGA-based deconvolution accelerator for deconvolutional neural networks and propose a three-step design methodology which first uses statistical analysis to find out the most cost-efficient bitwidth, then explore the design space with roofline model [6] and use VLSI optimization methods to produce the final design. Finally, we implement our method on a Zynq-7000 FPGA and realize a performance density of 0.012 GOPs/DSP.

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