CMOS-Memristive Analog Multiplier Design

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Abstract—This paper proposes four quadrant analog multiplier using CMOS-memristor circuit. Currently, there are plenty of analog multipliers using resistors and CMOS transistors. They can attain perfect multiplication but have several disadvantages such as lower processing speed, higher power consumption and larger chip areas. Memristor based circuits are introduced to resolve the mentioned drawbacks. In this paper current mode four quadrant multiplier based on squaring circuits is taken as a framework, and CMOS transistors are replaced with memristors. The circuit design is simulated with SPICE, and variability analysis and performance variation with temperature is performed. The proposed circuit allows faster processing with retained data while dissipating less power retaining the multiplication characteristics.

Keywords- analog multiplier, current-mode, memristors, trans-linear loops.

I. INTRODUCTION

An analog multiplier is a device with two input ports and one output port. The output signal is the product of the two input signals. There are types of multipliers depending on their “quadrants”. From a mathematical point of view, multiplication is a “four quadrant” operation, so that both inputs may be either positive or negative and as output may be also. There are several designs of multiplication circuits [13], [15]. However, these multipliers are limited to signals of one polarity. If both signals must be unipolar, we have a “single quadrant” multiplier, and the output will also be unipolar. If both outputs have either polarity, the multiplier is a “four quadrant” multiplier, and the output is “bipolar” [7], [18]. Multipliers serve in variety of applications including signal processing (amplitude/frequency modulations), ratio determination, variable gain amplifiers, frequency mixers, ring modulators and etc.

There are plenty of analog multiplier circuits implemented with transistors and resistors. This paper presents multiplier with comparatively new device called memristors. Memristors are passive elements [21], where the charge passing at instant of time changes the inner titanium dioxide concentration of memristor. Memristor remembers its last resistance state, meaning that when power is out, it can store the recent data until power is supplied again [3], [11], [14]. It gives several advantages to memristors over transistors. If current passing through the transistor is stopped, all the data are lost without retaining. However this is not the case with memristors, since memristors can retain the data. The second advantage is memristor based circuits consume less power [4], [8]–[10], [13]. Third advantage according to [12] is that memristor based circuits operate faster. However, as mentioned before memristors are passive elements. Thus they can not introduce energy into the circuit and need some active elements. [3] claims that integrating together transistors and memristors is the best due to capability of delivering the same or enhanced functionality with fewer components, thus providing significant savings for both chip area and operating power.

Based on operation, multipliers are divided into two categories weak and strong inversion. The proposed circuit operates in strong inversion. There are two types of strong inversion: first are based on geometric mean and squaring/dividing blocks, second are based on two or three squaring blocks. First type operates only in one quadrant, while second type can show in all four quadrants [2]. The circuit proposed in this paper is based on three trans-linear squaring. Trans-linear loops have no dependence on circuit parameters and supply voltage, also, current relation in their output is pure [5]. This brings several features as precision, simplicity, more linearity, high band width and low power expenditure. Section II of the paper describes circuit design, followed by Math analysis in Section III. Section IV discusses simulation results and then paper is summed up.

II. CIRCUIT DESIGN

A. Squaring circuit

![Squaring circuit schematics](Fig. 1. Squaring circuit schematics)

Squaring circuit is shown in Fig.1. In this circuit transistors M1 and M2 are biased at fixed currents and fixed Gate-Source voltages [16]. Four transistors M1 to M4 form a trans-
linear loop. Output current was transferred by implementing simple current mirror. Assuming threshold voltages are equal: $V_{TH,N} = V_{TH,P} = V_{TH}$ and $K_N = K_P = K$ there are relationships:

$$\sqrt{I_{D1}} + \sqrt{I_{D2}} = \sqrt{I_{D3}} + \sqrt{I_{D4}} \quad (1)$$

$$I_B = I_{D1} = I_{D2}; I_{D3} = I_{out} - I_{in}; I_{D4} = I_{out} \quad (2)$$

Then, by rearranging equations (1) and (2), the squaring equation can be obtained:

$$I_{out} = \frac{I_{in}^2}{16 \times I_B} + I_B + I_{in}/2 \quad (3)$$

Equation (3) indicates that output is sum of squared input, DC current source and half of input current.

B. Multiplier circuit

Fig. 2. Multiplier circuit schematics

Fig. 2. shows the multiplier circuit based on squaring circuit. The circuit constitutes of five pair of transistors in serial connection within the pairs(M1-M2, M3-M4, M5-M6, M7-M8, M9-M10). The pair M1-M2 constructs four squaring circuits with four other pairs [2]. Transistors M1, M7 and M8 are replaced with MS memristors model, since they are in boundary at saturation region. Fig.3 shows the circuit schematics with substituted memristor models. Used technology is 0.18µm CMOS. $V_{dd}=1.8V$ and $I_b=10µA$.

III. MATHEMATICAL ANALYSIS

A. Input-output relationship

Based on a squaring principle, the output current is:

$$I_{out} = I_{o1} + I_{o2} - I_{o3} - I_{o4} = \frac{I_x \times I_y}{8I_b} \quad (4)$$

All the $I$ values are labeled in Fig.3. The input voltage of the circuit is equal to:

$$V_{in} = V_{dd} - V_{th} + \sqrt{\frac{(I_{in} - 4I_b)^2}{16KI_b}} \quad (5)$$

where $V_{th}$ is threshold voltage of CMOS transistors. Then from (5) the input resistance $R_{in}$ can be derived as:

$$R_{in} = \frac{dV_{in}}{dI_{in}} = \frac{1}{4\sqrt{KI_b}} \quad (6)$$

(6) signifies that input resistance is not dependent from input currents. The body-source voltage of a MOS transistor relates the threshold voltage by:

$$V_{th} = V_{th0} + \gamma(\sqrt{2}\phi_b + V_{sb} - \sqrt{2}\phi_b) \quad (7)$$

Even though threshold voltages of NMOS transistors varied or there was a $V_{th}$ mismatch in N type and P type transistors, output current of each squaring circuit could be derived by applying it to each trans-linear loop in Fig.1. Then, with considering $V_{th}$ mismatch output current of multiplier would be equal to:

$$I_{out} = \frac{I_x \times I_y}{8I_b} + \sum_{n=1}^{6} E_i \quad (8)$$

In the equation $E_i$ are DC errors that depend on the threshold voltage mismatch of transistors $\sigma_i$. 

B. Small signal model

The corresponding small signal model of circuit is drawn in Fig.4 $G_i$ are voltage dependent current sources [6]. $G_i = g_m \times V_{gs}$, whereas $R_0 = \frac{1}{M/T}$. Note that for both NMOS and PMOS small signal models are the same. The small signal model for three and four pin Mosfets differ with each other. Although in the circuit four pin CMOS are used, for small signal model three pin model is taken, as fourth pin bulk is connected to either drain or source.

IV. SIMULATION RESULTS

A. Transient analysis

W/L ratios of implemented transistors have significant importance in performance analysis. [1] states that W/L affects transconductance and current capability factors. Initial transistor parameter characteristics as in proposed circuit of [2]
In order to analyze temperature effect on performance, temperature is varied from -50°C to 100°C in steps of 50°C. So four different values are recorded. Usually transistors are more heat sensitive rather than passive elements like resistor, capacitor and inductor [19]. Gate, drain and source currents of transistors changed in response to temperature variation. Characteristics, W/L ratios of several CMOS from Fig. were varied. Table II shows altered ratios. Adjustment has helped to achieve smoother output as will be discussed in next paragraph.

For the transient analysis inputs are \( I_x = 20 \times 10^{-6} \times \sin(2\pi 10^6 t) \) A and \( I_y = 20 \times 10^{-6} \times \sin(2\pi 10^6 t) \) A sinusoidal signals. According to equation (4) output current is multiplication of inputs divided by 8 times DC current source \( I_b \). Since \( I_b \) is equal to 10\( \mu A \), output current is in range of -5\( \mu A \) to +5\( \mu A \). However obtained outputs quiet varied from theoretical expectation. Both Fig.5 and Fig.6 are output waveforms, specifically, Fig.5 draws output before W/L adjustment and Fig.6 is after. Waveforms in pink represent output of [2] proposed circuit with all transistors, while dark-yellow waveforms depict output of memristors installed multiplier. My final achieved multiplication output, i.e. of Fig. 3, is dark-yellow curve in Fig.6. Before transistor width and length adjustment, output has significant amplitude variation between two consequent periods. After adjustment this problem is resolved. Though, peak-to-peak amplitude become from -7\( \mu A \) to +7\( \mu A \), which is a sign of slight amplification. After memristors were placed, in the result curveform each bottom side of second period experienced moderate bend.

**B. DC analysis**

Initially, first input \( I_x \) is swept from -20\( \mu A \) to +20\( \mu A \) in steps of 4\( \mu A \) and \( I_y \) is taken as a parameter. Then, inversely, input \( I_y \) is swept while \( I_x \) is taken as a parameter. In Fig.7 transfer characteristics due to \( I_{out} \) are depicted respectively. Ideally the DC transfer characteristic of the analog multiplier should be linear [17]. However, in Fig.7 input-output relationships are not purely linear. It should be noted that these are the case for memristor installed circuit and it led to slight deviation in linearity relationship.

**C. Temperature analysis**

In order to analyze temperature effect on performance, temperature is varied from -50°C to 100°C in steps of 50°C. So four different values are recorded. Usually transistors are more heat sensitive rather than passive elements like resistor, capacitor and inductor [19]. Gate, drain and source currents of transistors changed in response to temperature variation whereas other elements of circuit do not. These variations near transistors affected output waveform, specifically, higher temperatures tend to increase DC offset (Fig. 7).
D. THD analysis

[2] investigated that their proposed multiplier had no more than 6% of distortion for 100kHz to 50MHz, which can be considered as a very good performance. The Table III below shows THD of proposed circuit for different frequencies. For lower frequencies it has extremely high THD values.

| Frequency | THD% |
|-----------|------|
| 100K      | 175.3|
| 500K      | 132.7|
| 1M        | 124.8|
| 10M       | 55.5 |
| 25M       | 77.4 |
| 50M       | 69.7 |

E. Power dissipation

It is expected that by replacing transistors with memristors the overall power loss would be decreased. Before substitution, circuit dissipated in total 83.5µW. However, after memristors were placed it was 80.6µW. Thus making the circuit to be more power saving.

V. CONCLUSION

In this paper current mode four quadrant analog multiplier circuit with memristors was proposed. The circuit operation is based on MOS trans-linear loops and it employs compact squaring circuits. The input resistance of the squaring circuit is not highly dependent from input currents. The result was that after memristors were replaced some of the performance characteristics improved while others not. In the output waveform bottom side of every second period had moderate bend, also DC analysis was not ideally linear. Total harmonic distortions were large at lower frequencies. The power dissipation of the circuit is observed to be diminished.

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