Implementing efficient balanced networks with mixed-signal spike-based learning circuits

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Abstract—Efficient Balanced Networks (EBNs) are networks of spiking neurons in which excitatory and inhibitory synaptic currents are balanced on a short timescale, leading to desirable coding properties such as high encoding precision, low firing rates, and distributed information representation. It is for these benefits that it would be desirable to implement such networks in low-power neuromorphic processors. However, the degree of device mismatch in analog mixed-signal neuromorphic circuits renders the use of pre-trained EBNs challenging, if not impossible. To overcome this issue, we developed a novel local learning rule for on-chip implementation that drives a randomly connected network of spiking neurons into a tightly balanced regime. Here we present the integrated circuits that implement this rule and demonstrate their expected behaviour in low-level circuit simulations. Our proposed method paves the way towards a system-level implementation of tightly balanced networks on analog mixed-signal neuromorphic hardware. Thanks to their coding properties and sparse activity, neuromorphic electronic EBNs will be ideally suited for extreme-edge computing applications that require low-latency, ultra-low power consumption and which cannot rely on cloud computing for data processing.

Index Terms—balanced networks, neuromorphic computing hardware still remains a challenge, since device-mismatch can cause sub-optimal performance.

To address this issue we present a local discrete learning rule for on-chip training of recurrent spiking neural networks into EBNs, that is optimally suited for mixed-signal neuromorphic circuits. We first validate the rule with high-level behavioural simulation, then we present the mixed-signal neuromorphic circuits that implement it and demonstrate their correct behaviour with low-level circuit simulations in two different experiments.

II. EFFICIENT BALANCED NETWORKS
A. Theoretical Background

Let us assume that we have a population of \( N \) spiking neurons into which \( N_x \) continuous signals are fed using a linear transformation \( \mathbf{F} \). We furthermore assume that the population of \( N \) neurons is fully interconnected by a matrix \( \Omega \) and that we can reconstruct the continuous signal fed into the population using \( \hat{x}_t = \mathbf{D}r_t \), where \( r_t \) is the filtered spike train at time \( t \) and \( \mathbf{D} \) is a predefined decoding matrix so that \( \mathbf{D} \propto F^T \).

Following [7], we can derive the optimal network connectivity of the EBN by assuming that neurons elicit spikes only when they contribute to reducing a loss function, which is mainly governed by the reconstruction error between the input \( x \) and the reconstructed version, \( \hat{x} \). Given a randomly chosen decoding matrix \( \mathbf{D} \), the optimal feedforward (\( \mathbf{F} \)) and recurrent (\( \Omega \)) weights are given by \( \mathbf{D}^T \) and \( -\mathbf{D}^T \mathbf{D} \), respectively. For a full derivation please see [7] and the supplementary information of [11]. This leaves us with one equation describing the membrane potential dynamics of the EBN:

\[
V(t) = \mathbf{F}x(t) + \Omega r(t)
\]

Having introduced the optimal network connectivity of EBNs, we can now derive the discrete learning rule to transform a randomly connected network into an EBN. Instead of calculating the local gradient, as done by the learning rule described in [11], this rule checks whether a certain condition is satisfied and increases or decreases the respective weights by a fixed discrete step size.

Using the described optimal network connectivity and the assumption that the input can be reconstructed using \( \hat{x}_t = \)
\( \mathbf{D}_r \), we can write the membrane potential of the \( n \)-th neuron to be

\[
V_n(t) = D^x_n x(t) - D^r_n \mathbf{D}r(t) = D^x_n (x(t) - \hat{x}(t))
\]

Thus, minimising voltage fluctuations ensures that the projected reconstruction error is reduced. This gives us the chance to minimise the simple loss function for all neurons \( n \):

\[
L = \frac{1}{2} (V^n_{\text{before}} - V^n_{\text{rest}} + V^n_{\text{after}} - V^n_{\text{rest}})^2
\]

where \( V^n_{\text{before}} \) is the \( n \)-th membrane potential before the spike has propagated to the neuron and \( V^n_{\text{after}} \) is the potential after the spike has propagated. Similar to the way the optimal network connectivity was derived in [7], we impose the constraint that a recurrent connection should be changed by some minimal value \( \omega \) if and only if it contributes to the reduction of the loss. Therefore, on each spike that neuron \( n \) receives, two conditions are checked:

**Condition I:**

\[
L(\Omega_{n,k} + \omega) < L(\Omega_{n,k})
\]

If we assume that the input signal does not change too rapidly, we can neglect the relatively small term \( dtF_x(t) \) and can write the voltage at neuron \( n \) after a spike reached this neuron as \( V^n_{\text{after}} = V^n_{\text{before}} + \Omega_{n,k} \), if neuron \( k \) emitted the spike. Note that \( \Omega_{n,k} \) is the recurrent connection from neuron \( k \) to neuron \( n \). Using this relation, we rewrite the loss to

\[
L = \frac{1}{2} (V^n_{\text{before}} + \frac{1}{2} \Omega_{n,k} - 2 V^n_{\text{rest}})^2
\]

Plugging this into the condition yields

\[
(V^n_{\text{before}} + \frac{1}{2} \Omega_{n,k} + \frac{1}{2} \omega - 2 V^n_{\text{rest}})^2 < (V^n_{\text{before}} + \frac{1}{2} \Omega_{n,k} - 2 V^n_{\text{rest}})^2
\]

**Condition II:**

The second condition is completely analogous to the first case with the only difference being that this time we check whether reducing the weight by \( \omega \) would reduce the loss:

\[
L(\Omega_{n,k} - \omega) < L(\Omega_{n,k})
\]

After some reformulating, condition I and II can be summarised in the learning rule below:

\[
\Omega_{n,k} \left\{
\begin{array}{ll}
\Omega_{n,k} + \omega & \text{if } 2V^n_{\text{before}} + \Omega_{n,k} < -\frac{\omega}{2} + 2V^n_{\text{rest}} \\
\Omega_{n,k} - \omega & \text{if } 2V^n_{\text{before}} + \Omega_{n,k} > \frac{\omega}{2} + 2V^n_{\text{rest}} \\
\Omega_{n,k} \text{ else}
\end{array}
\right.
\]

(1)

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**B. Software simulations of the learning rule**

Given a random decoder \( \mathbf{D} \), the recurrent connections of a balanced network are pre-defined. In order to prove the correctness of our learning rule, it therefore suffices to check that, given a random \( \mathbf{D} \), the initially random recurrent weights converge towards the optimal weights given by \( \Omega = -\mathbf{D}^T \mathbf{D} \).

To validate this, we show an experiment where we simulate our learning rule in a population of 20 neurons for 50 iterations on a two-dimensional input that was generated by smoothing white noise with a Gaussian filter. Figure 1 shows how the reconstruction accuracy improves dramatically, while at the same time reducing the average population activity and increasing sparsity (therefore reducing power consumption). Note also how after only a few training iterations, the discrete recurrent matrix visibly approximates the real-valued optimal matrix, depicted in column B. However, due to the discrete nature of the learning rule, with increasing levels of granularity the bounds imposed by the learning rule widen and fewer voltage deviations are penalised, leading to convergence towards non-optimal weight values.

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**III. HARDWARE IMPLEMENTATION**

To implement the proposed learning rule in a neuromorphic processor, we need to be able to store the synaptic weight locally, compare it to the postsynaptic neuron membrane potential, update the synaptic weight, and source/sink the weighted current into/out of the neuron according to the saved state. A general overview of the hardware structure is given in Fig. 2. Input spikes, which typically last tens of nano-seconds, are processed by a spike extender circuit which creates pulses with variable pulse widths that can range from micro- to milli-seconds. This circuit is used to modulate the gain that the synapse has on the postsynaptic membrane potential. As the parameters of this circuit are shared across all synapses, this circuit can be used to effectively implement a synaptic scaling homeostatic mechanism to regulate the excitability of the neuron [12], [13]. The extended pulse is
using the stored signals $V_{\text{INC}}$. The new weight is calculated in the “Counter Logic” block integrated synaptic current is injected into the silicon neuron. 

The learning operation. This is necessary since the learning rule reads the membrane potential of the neuron before the integrated synaptic current is injected into the silicon neuron. The new weight is calculated in the “Counter Logic” block using the stored signals $V_{\text{INC}}$ and $V_{\text{SL}}$. On the falling edge of the input pulse, the updated synaptic weight is finally stored into the seven-bit register, ready to be used when the next spike arrives.

A. Current Steering Digital to Analog Converter

To convert the stored weight value into a current we use a binary weighted current steering DAC topology, where each bit is represented by two NFETs in series. The first acting as a switch, enabling the current path, and the second acting as a current sink scaling the current by the magnitude of the bit. The summed currents are mirrored to a second complementary pair of transistors. The two gate voltages of these transistors are used as the weight bias $V_{\Omega}$ of the excitatory and the inhibitory DPI-synapse. To save power, the DAC is enabled only for the duration of the extended input spike pulse. Figure 3 shows the schematic of the DAC used in our implementation.

B. Learning Rule Module

The learning rule module compares the current representing the post-synaptic neuron’s membrane potential $I_{\text{mem}}$ with the presynaptic weight to evaluate the inequalities of (1). If either one of the inequalities is satisfied, $V_{\text{SL}}$ is set low and $V_{\text{INC}}$ is set according to the decision whether to increment or decrement the weight. If neither of both inequalities is satisfied, $V_{\text{SL}}$ is set high and no update is performed. By representing the weights and variables as currents we can rearrange the inequalities of eq. (1) to yield:

$$ \Omega_{n,k} \left\{ \begin{array}{ll} \Omega_{n,k} + \omega & \text{if } I_{n,k}^{\text{before}} - I_{n,k}^{\text{rest}} - \frac{I_{\text{inc}}}{2} + I_{n,k} < 0 \\ \Omega_{n,k} - \omega & \text{if } I_{n,k}^{\text{rest}} - I_{n,k}^{\text{before}} - \frac{I_{\text{inc}}}{2} + I_{n,k} < 0 \\ \Omega_{n,k} & \text{else} \end{array} \right. $$

(2)

Thanks to Kirchhoff’s current law, the left side of the inequalities in eq. (2) can be easily realized by connecting the currents to a common node. Since the right sides of the inequalities are zero, we only have to check if the current sums are negative to determine if inequalities are satisfied or not. This is accomplished by the circuit illustrated in Fig. 4. The relevant currents are set by the bias voltages on $M_{A3}, M_{C3}$ and $M_{D3}$ which represent the input, while $M_{B3}$ is treated as a hyper-parameter for the learning circuit. To reduce the Early effect and increase linearity, we make use of cascode current mirrors every time we need to mirror the currents. Depending on the sign of the currents in the inequality, the currents are mirrored with either a sourcing ($Source\ A, B$) or draining ($Drain\ C, D$) configuration. All outputs of these current mirrors are connected to a common node, to calculate the value of $I_{T}$. We use a Traff current comparator [17] to check the sign of $I_{T}$. This circuit is used once per inequality, therefore twice per synapse.

IV. RESULTS

As the circuits proposed operate in current-mode, all of the model variables are represented by currents. In the following, we indicate the membrane potential with $I_{\text{mem}}$, and the neuron’s reset and resting potential with $I_{\text{rest}}$ and $I_{\text{reset}}$ respectively. To demonstrate the functionality of the learning rule we performed two basic experiments.

In the first experiment, we train a single plastic synapse, stimulated with spikes at constant frequency, to balance the potential of a post-synaptic neuron around a nominal value $I_{\text{rest}}$. In this experiment, we initially set the neuron’s membrane
Fig. 4. Circuit implementation for the evaluation of the second inequality of eq. (2). The bias voltages on $M_{A3}$ and $M_{B3}$ source the $I_{IR}$ and $I_{SL}$ currents via the cascode mirrors Source A and Source B to Traff’s circuit while Drain D and Drain E drain the currents $I_{before}$ and $I_{Vss,k}/2$. When the inequality is satisfied $V_{out}$ is pulled to $V_{dd}$, and to GND otherwise.

Fig. 5. Changes in the weight value (red trace) and membrane potential state variable (blue trace) over time. The color of the shaded areas indicate either positive, negative or neutral correction of the synaptic weight. The upper and lower thresholds ($I_{upper}$, $I_{lower}$) around $I_{mem}$ indicate the tolerance region within which the learning mechanism stops changing weights.

potential to $I_{reset}$ in order to simulate a state where the postsynaptic neuron was strongly inhibited. Since this is a large deviation from $I_{reset}$ and the goal of the learning rule is to minimise fluctuations around $I_{reset}$, the plastic synapse increases its weight having the effect of strongly and quickly increasing $I_{mem}$ (see red and blue continuous traces in the first few ms of Fig. 5). Due to the inertia of the learning rule, the neuron overshoots, bringing $I_{mem}$ above $I_{reset}$. At this point the learning circuit compensates for this positive deviation and starts to decrease the weight towards a negative value, making the neuron undershoot. Because of the negative feedback nature of the learning mechanism, this process converges to a steady state after a small number of oscillations around the target value where the weight stops changing.

In the second experiment, the neuron receives input from two synapses: A plastic one and a fixed-weight excitatory one. Both synapses have the same time constant and are stimulated with the same spike train with a firing rate of 100 Hz. As in the first experiment, we initialize the neuron to $I_{reset}$, causing the learning rule to increase the synaptic weight. Figure 6 shows the response of the neuron to the two synaptic inputs, as the weight of the plastic synapse changes. Also, in this case the inertia of the learning rule causes the neuron to overshoot. This initial over-correction is then followed by a period of negative plastic weight updates which, compared to Fig. 5, is much longer due to the effect of the non-plastic excitatory synapse. When the negative weight of the plastic synapse brings $I_{mem}$ within tolerance bounds of $I_{reset}$, the weight stops changing, and when $I_{mem}$ falls outside of the tolerance region, the learning mechanism again adjusts the weights accordingly.

These experiments show that, in both cases, the synapse equipped with the learning rule learned to minimise the fluctuations around $I_{reset}$, by either simply reducing its own weight or by balancing the injected current of another synapse in the system. These results demonstrate the correctness of our circuit implementation and, in combination with the network-level simulations validate the proper behaviour of the circuits for implementing neuromorphic electronic EBNs.

V. Conclusion

We developed a novel learning rule that drives a randomly connected network of spiking neurons into a tightly balanced regime for producing EBNs, and presented its hardware implementation using mixed-signal neuromorphic circuits. We demonstrated the expected behaviour of the proposed learning rule with high-level behavioural simulations and the correct behaviour of its hardware implementation using low-level circuit simulations. Future work will be devoted to the design of a prototype chip with the circuits presented and their integration into a large multi-core neuromorphic processor. Further investigations will be carried out to assess the computations that can be done by such devices while harnessing the benefits of EBNs (see for example [8], [18], [19]).
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REFERENCES

[1] C. van Vreeswijk and H. Sompolinsky. Chaos in neuronal networks with balanced excitatory and inhibitory activity. *Science*, 274(5293):1724–1726, Dec 1996.
[2] Yuval Aviel, David Horn, and Moshe Abeles. Memory capacity of balanced networks. *Neural computation*, 17(3):691—713, March 2005.
[3] Y. Shu, A. Hasenstaub, and D. A. McCormick. Turning on and off recurrent balanced cortical activity. *Nature*, 423(6937):288–293, May 2003.
[4] Yashar Ahmadian and Kenneth D. Miller. What is the dynamical regime of cerebral cortex? arXiv e-prints, page arXiv:1908.10101, August 2019.
[5] G. Hennequin, Y. Ahmadian, D. B. Rubin, M. Lengyel, and K. D. Miller. The Dynamical Regime of Sensory Cortex: Stable Dynamics around a Single Stimulus-Tuned Attractor Account for Patterns of Noise Variability. *Neuron*, 98(4):846–860, 05 2018.
[6] Sophie Denève and Christian K. Machens. Efficient codes and balanced networks. *Nature Neuroscience*, 19(5):375–382, 2016.
[7] Ralph Bourdoukan, David G. T. Barrett, Christian K. Machens, and Sophie Denève. Learning optimal spike-based representations. In *Proceedings of the 25th International Conference on Neural Information Processing Systems - Volume 2*, NIPS’12, pages 2285–2293, USA, 2012. Curran Associates Inc.
[8] Alireza Alemi, Christian Machens, Sophie Denève, and Jean-Jacques Slotine. Learning arbitrary dynamics in efficient, balanced spiking networks using local plasticity rules, 2017.
[9] C. Mead. Neuromorphic electronic systems. *Proceedings of the IEEE*, 78(10):1629–36, 1990.
[10] E. Chicca, F. Stefanini, C. Bartolozzi, and G. Indiveri. Neuromorphic electronic circuits for building autonomous cognitive systems. *Proceedings of the IEEE*, 102(9):1367–1388, 9 2014.
[11] Wieland Brendel, Ralph Bourdoukan, Pietro Vertefchi, Christian K. Machens, and Sophie Denève. Learning to represent signals spike by spike. *PLoS Computational Biology*, 16(3):1–23, 03 2020.
[12] G.G. Turrigiano. Homeostatic plasticity in neural networks: the more things change, the more they stay the same. *Trends in Neuroscience*, 22(5):221–227, 1999.
[13] Ning Qiao, Chiara Bartolozzi, and Giacomo Indiveri. An ultralow leakage synaptic scaling homeostatic plasticity circuit with configurable time scales up to 100 ks. *IEEE Transactions on Biomedical Circuits and Systems*, 2017.
[14] C. Bartolozzi and G. Indiveri. Synaptic dynamics in analog VLSI. *Neural Computation*, 19(10):2581–2603, Oct 2007.
[15] C. Bartolozzi, S. Mitra, and G. Indiveri. An ultra low power current-mode filter for neuromorphic systems and biomedical signal processing. In *Biomedical Circuits and Systems Conference, (BioCAS)*, 2006, pages 130–133. IEEE, 2006.
[16] G. Indiveri, B. Linares-Barranco, T.J. Hamilton, A. van Schaik, R. Etienne-Cummings, T. Delbruck, S.-C. Liu, P. Dudek, P. Haßfnger, S. Renaud, J. Schemmel, G. Cauwenberghs, J. Arthur, K. Hynna, F. Follwosele, S. Saighi, T. Serrano-Gotareddona, J. Wijekoon, Y. Wang, and K. Boahen. Neuromorphic silicon neuron circuits. *Frontiers in Neuroscience*, 5:1–23, 2011.
[17] H. Traff. Novel approach to high speed cmos current comparators. *Electronics Letters*, 28(3):310–312, 1992.
[18] M. Boerlin, C. K. Machens, and S. Denève. Predictive coding of dynamical variables in balanced spiking networks. *PLoS Comput. Biol.*, 9(11):e1003258, 2013.
[19] David GT Barrett, Sophie Denève, and Christian K Machens. Optimal compensation for neuron loss. *eLife*, 5:e12454, dec 2016.