Design of a low-power compact CMOS variable gain amplifier for modern RF receivers

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ABSTRACT
The demand for portability has speeded up the design of low-power electronic communication devices. Variable gain amplifier (VGA) is one of the most vulnerable elements of every modern receiver for the proper baseband processing of the signal. CMOS VGAs are generally suffered from low bandwidth and small gain range. In this research, a two-stage class AB VGA, each stage comprising of a direct transconductance amplifier and a linear transimpedance amplifier, is designed in Silterra 0.13-µm CMOS utilizing Mentor Graphics environment. The post-layout simulation results reveal that the VGA design achieves the widest bandwidth of >200 MHz and high gain range from -33 to 32 dB. The VGA dissipates only 2mW from a single 1.2 V DC supply. The core chip area of the VGA is also only 0.026 mm\textsuperscript{2} which is also the lowest compared to recent researches. Such a VGA will be a very useful module for all modern communication devices.

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1. INTRODUCTION
The desire for portability and low cost forces the scientists to design very compact and power-efficient communication appliances [1-3]. The continuous advancement in CMOS technology made the realization of fabricating fully integrated receivers easy maintaining the optimum performance. As a consequence, low-power, portable and low-cost RF communication gazettes such as RFID, Bluetooth, Zigbee, Wi-Fi, WLAN devices are available nowadays [4-8].

The variable gain amplifier is one of the most vulnerable constituents in a receiver for the proper baseband processing of the signal [9-10]. In communication RF receivers, the VGA is normally employed to perform the role of stabilizing the signal processed by the baseband circuitry irrespective of the actual signal strength intercepted by the antenna [11-14]. In portable communication devices, VGA is required to operate with low power supply voltage [15-16] and low power dissipation [17-18]. Advancement in the process technology allows devices with low supply voltages. As a result, most low power integrated circuits use power supply voltages below or less than 1.2 V. Designing a low power, wide bandwidth, and highly linear CMOS VGA is very crucial at low supply voltages [19-20]. Figure 1 shows a typical RF receiver front-end including a variable gain amplifier.

There are two types of realizing the VGA circuits. The first one utilizes a switching scheme to adjust among various passive feedback elements, thus generates discrete gain steps. It is often known as digitally
controlled VGA. The second one is an analog linear-in-dB type, where an analog gain control signal controls an adjustable transconductance or resistance. The architectures have their own advantages and disadvantages [21-22]. It is well known that the negative feedback can be utilized to reduce distortion, provided linear feedback elements are available. Typically, only passive elements meet linearity requirements. Therefore, to utilize passive feedback elements in a VGA, they must be selectively switched into the signal path. Since this type circuits can utilize the benefit of negative feedback, they are still able to achieve decent linearity for large output voltages, but the discrete gain levels can be disadvantages for some receivers. For example, wireless communication systems, the signal phase should be continuous, and therefore, the discrete gain step VGA is not preferred [23-24].

To achieve continuous control of the gain, one or more parameters of the circuit, such as the bias current or the bias voltage, can be continuously varied. The advantage of this type of circuits is that the gain can be varied smoothly between extreme values. The disadvantage is that the linearity of such an amplifier is typically poor. Since altering the bias point of an inherently nonlinear device varies the gain, the only way to achieve acceptable distortion performance is to keep the signal levels low. In analog VGA design, the control mechanism is the prime issue and depending on that several VGA circuit architectures have been proposed by the researchers such as pseudo-exponential function, quasi-exponential function, current steering, feedback tuning, Cherry-Hooper VGA. There are modifications as well as the addition of extra circuits have been reported to these designs to obtain specific performance specifications [25-26]. Most of them have suffered from nonlinearity, low gain, narrow bandwidth and high power dissipation. Therefore, a very compact VGA design with better performance is very important for low-power communication devices. This research illustrates the design of a two-stage low power, wide bandwidth, and compact class AB variable gain amplifier in SilTerra 0.13 µm CMOS process. The proposed VGA overcomes the constraints of the small bandwidth and small gain range at small supply voltages at a very compact die.

2. Research Method

The building blocks of the proposed two-stage VGA circuit are illustrated in Figure 2. Each block comprises of a cascaded linear transconductance amplifier (Gm cell) and a linear transimpedance amplifier (TIA) along with feedback through shunt resistors to keep the bandwidth stable during voltage gain variation. In this design, a source degeneration differential input Gm cell (N1–N2, Rs) and a current mode TIA
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(P1–P6, N3–N6) has been cascaded in order to maximize the bias current efficiency, transconductance at a supply voltage as shown in Figure 3. From the small signal analysis of each stage of the amplifier, the voltage gain of each stage of the two-stage VGA is determined from the values of the Gm and the Rm. The values of the Gm and Rm of the transconductor part can be evaluated as:

\[ G_m = \frac{g_{mi}}{1 + g_m R_m + s R_m C_{gs}} \]  (1)

\[ R_m = -\frac{(R_f A - R_m)}{(1 + A)} \]  (2)

Where \( A \) and \( R_{in} \) correspond to the current gain and the input resistance of the amplifier and \( C_{gs} \) correspond to the gate-source capacitance of the Gm cell. If the value of \( A \) is much greater than unity, the value of \( R_m \) can be considered to be equal to \(-R_f\). This implies that in order to achieve a linear variable gain amplifier, a linear \( R_m \) with high-gain is needed.

\[ A = \frac{g_{mx}}{g_{my} + s C_x} \left( 1 + \frac{g_{my}}{g_{my} + s C_y} \right) \]  (3)

\[ R_m = \frac{1}{(g_{mi} + s C_s)} \]  (4)

Where \( g_{mi}, g_{mx} \) and \( g_{my} \) are transconductance of P1–P2, P3–P6 and N3–N6 respectively. At low frequencies, the value of \( R_m \) can be estimated as:

\[ R_m = -\alpha \left[ 2R_f \left( \frac{1}{g_{mx}} + \frac{C_y}{g_{my}} \left( R_f - \frac{1}{g_{mx}} \right) \right) \right] \left[ 1 + \frac{1}{2} \left( \frac{C_x}{g_{my}} \right) + \frac{C_x}{g_{mi}} + \frac{s^2 C_x C_y}{g_{mi} g_{my}} \right] \]  (5)

It is worth mentioning that, the transistor sizes are kept as small as possible to achieve smaller size without degrading the performance of the amplifier. Two stages of the proposed VGA are tied together with proper impedance matching. Table 1 shows the component sizes used in each stage of the VGA.
Table 1. Components used in the single stage VGA circuit

| Components | Size           |
|------------|---------------|
| P1-P2      | 1/0.13 (µm/µm) |
| P3-P6      | 100/0.13 (µm/µm) |
| N1-N2      | 100/0.13 (µm/µm) |
| N3-N4      | 300/0.13 (µm/µm) |
| N5-N6      | 100.13 (µm/µm) |
| Rs         | 2K            |
| Rf         | 600K          |

3. RESULTS AND ANALYSIS

The VGA, in this research, has been designed and simulated in Eldo RF simulator of the Mentor Graphics utilizing Silterra 0.13-µm standard CMOS process technology. The circuit is powered by a single 1.2 V DC supply. The results presented in this article are post-layout simulation results. Figure 4 and Figure 5 show two types of gain response curves by changing the value of feedback resistor (Rf) from 15k to 500k and source degeneration resistance (Rs) from 10k to 1M, respectively. The VGA shows the highest and the lowest gain of 32dB and -33 dB with Rs=500k, and Rs=15k, respectively. The varying values of Rf from 10k to 1M varies the bandwidth from 30 MHz to 200 MHz. The VGA dissipated approximately 2 mW at the 1.2 V supply voltage.

![Figure 4. Gain responses by varying feedback resistor (Rf)](image)

The Monte Carlo analysis of the proposed VGA for maximum gain is shown in Figure 6. In Monte Carlo analysis, for 50 runs or counts, the values of the maximum gain were between 31.7 dB and 32.7 dB. The results implies that the performance parameters of the VGA were stable within the acceptable range. Figure 7 shows the core layout of the proposed two-stage VGA circuit. In this design, multi-finger structure has been implemented for transistors with large aspect ratios to ensure better conductivity. The dimension of the core VGA is only (160×162) µm².
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4. CONCLUSION

In communication receivers, the VGA is essential to stabilize the uncertain signal strength received at the antenna for proper baseband processing. Wide bandwidth VGA design in downscaled CMOS process is very challenging for the researchers. In this research, a compact design of two-stage class-AB variable gain amplifier in Siltema 0.13-µm CMOS process is proposed to meet the goal. The post-layout simulation results reveal that VGA has the widest bandwidth of >200 MHz and smallest die area of 0.026 mm². It also shows very competitive power dissipation, and gain range.

Table 2. Performance comparison of variable gain amplifiers

| Ref. | CMOS process (µm) | Gain range (dB) | Bandwidth (MHz) | Supply voltage (V) | Power dissipation (mW) | Die area (mm²) |
|------|------------------|----------------|-----------------|-------------------|-----------------------|---------------|
| [17] | 0.18             | -30 to 65      | >32             | 1.8               | 22                    | -             |
| [18] | 0.18             | -39 to 55      | >4              | 1.8               | 20.5                  | 0.42          |
| [26] | 0.18             | 16.4           | -               | 1.8               | 14.4                  | 0.036         |
| [24] | 0.13             | 0 to 57        | >10             | 1.2               | 4.44                  | 0.58          |
| [23] | 0.18             | 60             | -               | 1                 | 0.14                  | -             |
| [25] | 0.18             | -7.5 to 19.5   | -15             | 1.8               | -9.2                  | -             |
| This work | 0.13             | -33 to 32      | >200            | 1.2               | 2                     | 0.026         |
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