A Method for Selection of Power MOSFETs to Minimize Power Dissipation

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Abstract: A balance between static and dynamic losses of a power MOSFET is always desirable for accomplishing the maximum efficiency for a specific power converter. The standard semiconductor theory suggests that a minimum power dissipation in a MOSFET can be achieved by selecting a specific device active area. However, for power circuit designers, the active device area is unknown given that only datasheet parameters are available. Hence, in this paper, we propose a simple method, based on semiconductor theory, to select optimum power MOSFET from a family of MOSFETs using only datasheet parameters. By applying this optimization method to the specific power supply circuit under development, power engineers can select the best transistors to yield lowest power losses for the systems under development.

Keywords: dynamic losses; datasheet parameters; optimization; power dissipation; power MOSFET; static losses

1. Introduction

Power semiconductor devices form the core of the modern power conversion systems. The overall efficiency of the power converters depends mainly on the losses attributed to power semiconductor devices. Therefore, a thorough understanding and selection of the power semiconductor device are required for designing efficient and reliable power converters.

One such popular and widely used power semiconductor device is a power MOSFET. The total power dissipation in a power MOSFET consists of static loss that is determined by the on-resistance and dynamic loss that is determined by the parasitic capacitances [1]. The standard semiconductor theory shows that the total power dissipation has a minimum for specific device active area [2]. This happens because an increase in the active area reduces the on-resistance, reducing static loss, but it increases the parasitic capacitances, increasing the dynamic loss. However, the active device area that minimizes the total power dissipation depends on specific circuit configuration and parameters, such as the on-state current flowing through the power MOSFET and the switching frequency. Because of that, the device manufacturers cannot provide a single optimum MOSFET for all applications and instead offer a family of MOSFETs manufactured by the same process but with different on-resistances [3]. On the other hand, the power circuit designers do not know the active device area and the other needed semiconductor device parameters to determine the minimum power dissipation for a particular application; hence, they cannot use the standard semiconductor theory of active device area to select the MOSFET with the optimum on-resistance.

In this paper, we propose a method for this selection, which is based on semiconductor theory, using only datasheet parameters such as on-resistance and energy related effective
output capacitance. The proposed method is demonstrated by commercial superjunction (SJ) MOSFETs and silicon carbide (SiC) MOSFETs.

2. Proposed Method

The maximum current handling capability of any power MOSFET is generally limited by the on-resistance ($R_{ON}$). The total $R_{ON}$ of a power MOSFET structure comprises many individual resistances connected in series between the drain and the source terminal. However, the contribution of the channel resistance ($R_{CH}$), the accumulation resistance ($R_{A}$), the JFET resistance ($R_{JFET}$), and the drift region resistance ($R_{drift}$) is significantly higher than the rest of the resistances, therefore dominating the value of static losses [2]. It must be noted that all the contributing resistances are inversely proportional to the channel width ($W$) [2,4].

The switching characteristics of a power MOSFET are mainly determined by its intrinsic parasitic capacitances. The parasitic capacitances of the power MOSFET can be classified as input capacitance ($C_{ISS}$) and output capacitance ($C_{OSS}$). At higher voltages and switching frequencies, the dynamic losses due to charging/discharging of $C_{OSS}$ dominate the switching performance [5]. Hence, in this brief, the dynamic power dissipation by $C_{OSS}$ is given more consideration than the influence of $C_{ISS}$.

$C_{OSS}$ comprises gate-to-drain ($C_{GD}$) and drain-to-source ($C_{DS}$) capacitance. Both $C_{GD}$ and $C_{DS}$ span the depletion region, which is directly proportional to $W$; hence, $C_{OSS}$ as a function of $W$ can be expressed as [6,7]:

$$C_{OSS} = LW \sqrt{\frac{q \epsilon N_D}{2V}}$$  \hspace{1cm} (1)

where $q$ is the charge of an electron, $\epsilon$ is the semiconductor permittivity, $N_D$ is the donor doping density, and $V$ is the applied drain-to-source voltage.

Because the power MOSFET datasheets do not show the device parameter $W$, the power circuit designers cannot use it to calculate the resistances and the capacitances and, therefore, cannot use the corresponding equations to select the power MOSFET that will minimize the power losses. On the other hand, $R_{ON}$ and $C_{OSS}$ are available on every datasheet. From the standard semiconductor theory, it is clear that $R_{ON}$ is inversely proportional to $W$ and $C_{OSS}$ is directly proportional to $W$. This means that:

$$R_{ON} \cdot C_{OSS} = \kappa$$  \hspace{1cm} (2)

where $\kappa$ is a constant that groups all technological parameters for the specific family of MOSFETs. The constant $\kappa$ is effectively a figure of merit for a family of MOSFETs. In fact, if we integrate $C_{OSS}$ curve with respect to $V$ and replace $C_{OSS}$ with the integrated charge, $Q_{OSS}$, we obtain a well-known figure of merit: $R_{ON} \cdot Q_{OSS}$ [8]. However, most manufacturers do not provide $Q_{OSS}-V$ curves in the datasheets. Instead, most datasheets provide energy-related effective output capacitance, $C_{o(er)}$. The reason for introducing $C_{o(er)}$ is the nonlinear nature of $C_{OSS}$, which makes it difficult for a circuit designer to analyze power circuits. The constant capacitance $C_{o(er)}$ is defined as the capacitance that gives the same stored energy as $C_{OSS}$ while $V$ is rising from 0 to 80% of the drain-to-source breakdown voltage, and it is given by [9]:

$$C_{o(er)} = \frac{2}{V^2} \int_0^V C_{OSS}(v) \times v \, dv$$  \hspace{1cm} (3)

Because the value of $C_{o(er)}$ is available in most datasheets, it is convenient to use it in (2) instead of the voltage-dependent $C_{OSS}$:

$$R_{ON} \cdot C_{o(er)} = \kappa$$  \hspace{1cm} (4)

The dynamic power dissipation due to charging/discharging of $C_{o(er)}$ is given by [2,10,11]:

$$R_{ON} \cdot C_{o(er)} = \kappa$$  \hspace{1cm} (4)
\[ P_{\text{dynamic}} = f C_{o(e)} V^2 \]  

where \( f \) is the switching frequency. Using (4) and (5) can be expressed in terms of \( R_{ON} \) as:

\[ P_{\text{dynamic}} = \left( f x V^2 \right) / R_{ON} \]  

The static power dissipation can be expressed by the standard equation [1,2,11]:

\[ P_{\text{static}} = D R_{ON} I^2 \]  

where \( D \) is the duty cycle and \( I \) is the root-mean-square drain current. Combining (6) and (7), we can express the total power dissipation in terms of \( R_{ON} \) as the parameter distinguishing different MOSFETs from the same family:

\[ P_{\text{total}} = D R_{ON} I^2 + \left( f x V^2 \right) / R_{ON} \]  

To minimize the total power losses with respect to \( R_{ON} \), the derivative of (8) is set to zero and the optimum \( R_{ON} \) is derived as:

\[ \frac{dP_{\text{total}}}{dR_{ON}} = 0 \Rightarrow R_{ON}(f) = \frac{V}{T} \sqrt{f x D} \]  

Equation (9) shows that \( P_{\text{total}} \) has a minimum for a specific \( R_{ON} \), depending on the values of \( V, f, D, \) and \( I \). In the next section, the proposed method for selection of the optimum \( R_{ON} \) is demonstrated with SJ MOSFETs.

3. Demonstration of the Proposed Method Using SJ MOSFETS

Superjunction devices consist of multiple, alternate highly doped \( n \) and \( p \) semiconductor stripes leading to lower \( R_{ON} \) without sacrificing the blocking voltage. Hence, for the same breakdown voltage, the \( R_{ON} \) of SJ MOSFETs will be much lower than the conventional Si-based planar MOSFETs.

To demonstrate the proposed method described in the previous section, nine Infineon 650 V CoolMOS C3 technology SJ MOSFETs were considered. Individual \( \kappa \) values were calculated using (4) by taking \( R_{ON} \) and \( C_{o(e)} \) values from the respective SJ MOSFET datasheets. The mean of all the individual \( \kappa \) values was equal to \( 1.835 \times 10^{-11} \) \( \Omega \)F, and this value was taken to represent this family of MOSFETs. The values of \( C_{o(e)} \) in the datasheets were given for \( V = 480 \) V, and this voltage was used in (6). Since the SJ MOSFETs have different current ratings, the current of the lowest rated SJ MOSFET current, \( I = 2.5 \) A, was utilized.

Using \( D = 0.5, \kappa = 1.835 \times 10^{-11} \) \( \Omega \)F, \( V = 480 \) V, and \( I = 2.5 \) A, the theoretical static, dynamic, and total losses were calculated and are shown in Figure 1. For the same bias voltage, current, and duty cycle, the total losses for individual SJ MOSFETs were calculated using their respective \( \kappa \) in (8) and are also shown in Figure 1. Despite the variation of individual \( \kappa \) values around the mean value of \( 1.835 \times 10^{-11} \) \( \Omega \)F, the total losses of the commercial SJ MOSFETs follow the trend of the proposed theory, as can be seen from Figure 1. For \( f = 20 \) kHz and \( f = 100 \) kHz, the minimum losses are occurring for \( R_{ON} = 164.5 \) m\( \Omega \) and \( R_{ON} = 367.8 \) m\( \Omega \), respectively. For the power converter operating at \( V = 480 \) V, \( I = 2.5 \) A, and \( f = 20 \) kHz, SJ MOSFETs SPW47N60C3, SPW35N60C3, SPW24N60C3, and SPW20N60C3 are the best selection because they minimize the power loss. However, the selection of the best MOSFET changes for higher frequencies. The maximum switching frequency of 100 kHz was used for this demonstration because \( C_{ISS} \) of CoolMOS C3 family of MOSFETs is quite large, and higher switching frequencies are practically not feasible. For the power converter operating at the same bias voltage and current but at the switching frequency of 100 kHz, SJ MOSFET SPP11N60C3 provides the
minimum power loss. It can be observed from Figure 1 that the optimal $R_{ON}$ increases as the switching frequency increases. This is because the switching losses due to the parasitic capacitances begin to dominate at higher switching frequencies. To minimize the dominant switching losses, a MOSFET with a smaller capacitance has to be selected, and this MOSFET will have a smaller channel width (Equation (1)), which in turn means that $R_{ON}$ of this MOSFET is larger.

![Figure 1. Comparison of the proposed theory at a constant output current of 2.5 A with the commercially available Infineon CoolMOS C3 technology SJ MOSFETs.](image)

For a different family of MOSFETs, corresponding to a different technology process, the constant $\kappa$ has a different value. At Infineon, the CoolMOS CE family of MOSFETs is based on newer and better optimized technology. The $C_{iss}$ of CoolMOS CE family of MOSFETs is lower than that of the CoolMOS C3 family of MOSFETs, enabling them to operable at higher switching frequencies. Hence, in order to show the effectiveness of the proposed method, nine 600 V SJ MOSFETs from the CoolMOS CE family were considered. For CoolMOS CE family, the mean $\kappa = 1.453 \times 10^{-11} \Omega F$ was used to calculate the theoretical static, dynamic, and total losses, as shown in Figure 2. The voltage, current, and duty cycle were kept the same. For $f = 100$ kHz and $f = 500$ kHz, the minimum losses are occurring at $R_{ON} = 327.3 \, \text{m}\Omega$ and $R_{ON} = 731.9 \, \text{m}\Omega$, respectively. Hence, for the power converter operating at 100 kHz, SJ MOSFET IPAW60R280CE should be selected to minimize the power loss, whereas IPAW60R460CE is the best choice when the power converter operates at 500 kHz.

For the case of a higher output current, static losses starts to dominate the dynamic losses. By keeping switching frequency at 100 kHz, the proposed theory was applied to CoolMOS CE family of MOSFETs for higher currents, as shown in Figure 3. It can be seen from Figure 3 that the SJ MOSFET with the lowest $R_{ON}$, i.e., IPAW60R190CE, is the best for power converters operating at output currents higher than 5 A.
from Figure 3 that the SJ MOSFET with the lowest $R_{ON}$, i.e., IPAW60R190CE, is the best for power converters operating at output currents higher than 5 A.

Figure 2. Comparison of the proposed theory at constant output current of 2.5 A with the commercially available Infineon CoolMOS CE technology SJ MOSFETs.

Figure 3. Comparison of the proposed theory at constant switching frequency of 100 kHz with the commercially available Infineon CoolMOS CE technology SJ MOSFETs.
4. Validation

A widely used clamped inductive load circuit was used in LTSPICE to validate the proposed approach. The circuit parameters for the simulation were: $V_{DD} = 480$ V, $I_{DD} = 2.5$ A, $R_G = 25$ $\Omega$, $V_{CC} = 15$ V, $f = 100$ kHz, $D = 0.5$, $t_r = 30$ ns, $t_f = 20$ ns, $L_S = L_D = L_G = 5$ $\mu$H, and a 650 V SiC Schottky diode (SCS320AJ). The CoolMOS C3 family MOSFET models provided by the Infineon were utilized in the configured circuit. These models include the parasitic inductances and capacitances of the power MOSFET. Apart from $C_{DSS}$, the dynamic losses of a power MOSFET are mainly influenced by the transistor switching time and diode reverse recovery. The diode reverse recovery loss is a fraction of transistor switching time loss and hence is neglected in the paper. The transistor switching time loss is attributed to $C_{ISS}$ of the MOSFET, and the power loss due to this switching time can be calculated as [11]:

$$P_{swt} = V \times I \times f \times \frac{(Q_{GS} + Q_{GD})}{I_G} \quad (10)$$

where $I_G$ is the gate current and $(Q_{GS} + Q_{GD})/I_G$ determines the rate of charging/discharging $C_{ISS}$ by the gate driver. The term $(Q_{GS} + Q_{GD})/I_G$ is inversely proportional to $R_{ON}$ for a family of MOSFETs. Hence, for lower $R_{ON}$, higher charge is required, and for higher $R_{ON}$, lower charge is required to charge $C_{ISS}$ of the MOSFET. Charging and discharging of $C_{ISS}$ is through the channel of the MOSFET, and hence for each MOSFET of the same family, the actual $V_{DS}$ waveform depends on $R_{ON}$ of the corresponding MOSFET. In the Miller region, the inductive load fixes the drain current at a constant value $I_D$, which means that $V_{DS}$ can be replaced by $R_{ON} \times I_D$. Therefore, the switching time in (10) becomes independent of $R_{ON}$. The consequence of this observation is that the minimum power dissipation appears at the same $R_{ON}$, regardless of the actual value of $I_G$ and the $R_{ON}$-independent power dissipation due to $I_G$. The constant for the theory was estimated to be 3 W by comparing (6) to the LTSPICE simulation of the already found optimized MOSFET in CoolMOS C3 family, i.e., SPP11N60C3. Hence, the entire theoretical total loss curve for $f = 100$ kHz as shown in Figure 1 was raised by 3 W and was compared with the LTSPICE simulation of each MOSFET, as shown in Figure 4.

![Figure 4](image-url)  
**Figure 4.** Comparison of the proposed theory with LTSPICE simulation on clamped inductive load circuit.

It is quite clear from the simulation results shown in Figure 4 that the switching time and the parasitic inductances of the MOSFET do not impact the selection of the MOSFET and follow a similar trend. Still, the optimized MOSFET to choose from the CoolMOS C3 family is SPP11N60C3.
family for the given circuit conditions is SPP11N60C3. The theory quite matches all the available simulated MOSFETs, which shows the effectiveness of the proposed approach.

5. Application of the Proposed Method to SiC MOSFETs

Wide band gap devices such as SiC MOSFETs have emerged as a potential alternative to conventional Si-based power devices for numerous power converter applications. To demonstrate the proposed method, six commercially available 650 V SiC MOSFETs from ROHM Semiconductor were used. The mean value of $\kappa$ for this family of MOSFETs was $5.775 \times 10^{-12} \Omega F$. The comparison of the transistor loss obtained from (8) and the power losses of individual SiC MOSFETs, at constant output current of 20 A, is shown in Figure 5. As expected, the power loss is minimized by a MOSFET with a higher on-state resistance when the switching frequency is increased. In the specific case of 100 kHz, the MOSFET SCT3022AL minimizes the power loss, whereas the SCT3060AL should be selected for the switching frequency of 500 kHz.

6. Conclusions

A method to select optimum power MOSFET from a family of MOSFETs considering only datasheet parameters, such as $R_{ON}$ and $C_{oer}$, is proposed in this paper. The proposed method is demonstrated with two families of Infineon SJ MOSFETs, CoolMOS C3 and CoolMOS CE. The proposed method is validated in LTSPICE using CoolMOS C3 models provided by the manufacturer. The proposed method is further demonstrated with the SiC MOSFETs family from ROHM Semiconductor. The validation of the proposed method with LTSPICE shows that the average values of current and voltage are sufficient for the purpose of selecting the MOSFET with optimum $R_{ON}$. The simulation with LTSPICE produced typical current and voltage waveforms. That is why the agreement between
the power dissipation obtained by LTSPICE simulation (with the typical waveforms) and the power dissipation obtained with the proposed analytical equation (using the average values of current and voltage) demonstrates that the average values are sufficient for this purpose. By applying this optimization method to the specific power supply circuit under development, power engineers can select the commercial power MOSFET with the specific \( R_{ON} \) that maximizes the power efficiency of the designed circuit.

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