DEPFET active pixel sensors for the vertex detector of the Belle-II experiment

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ABSTRACT: Active pixels sensors based on the DEPFET technology will be used for the innermost vertex detector of the future Belle-II experiment. The increased luminosity of the $e^+ e^-$ SuperKEKB collider entails challenging detector requirements, namely: low material budget, low power consumption, high precision and efficiency, and a large readout rate. The DEPFET active pixel technology has shown to be a suitable solution for this purpose. A review of the different aspects of the detector design (sensors, readout ASICS and supplementary infrastructure) and the results of the latest thinned sensor prototypes (50 µm) are described.

KEYWORDS: Particle tracking detectors; Solid state detectors; Particle tracking detectors (Solid-state detectors)

1On behalf of the DEPFET collaboration.
1 Belle-II and the PXD detector

The SuperKEKB Flavor Factory [1] is under construction at the High Energy Accelerator Research Organization in Tsukuba, Japan. This new factory is an asymmetric energy (4 GeV, 7 GeV) $e^+e^-$ collider working at a center of mass energy of the Y(4S) resonance ($E_{\text{cm}} = 10.58$ GeV). The design peak luminosity is $8 \cdot 10^{35}$ cm$^{-2}$s$^{-1}$, around 40 times higher than the former KEKB Factory. To achieve this luminosity smaller spot-size beams (nano-beam) than those used at KEKB will be used. The beams will be squeezed down by one order of magnitude in both, vertical and horizontal, directions and the beam currents will be doubled [2]. This new installation is expected to start operation at the end of 2014 and an integrated luminosity of 50 ab$^{-1}$ should be collected by 2020.

In order to fully exploit the higher luminosity of the new facility the former Belle detector is being upgraded [2]. This new spectrometer must cope with the higher backgrounds (more radiation damage, occupancy and fake hits production) and event rates, posing a technological challenge both in the sensor and readout electronics designs aspects.

One of the key detectors that drive the physics performance of the whole experiment is the vertex detector. It consists of four layers of double-sided silicon strip detectors in the outer radii layers (SVD [3]) and two layers of high granularity pixel sensors in the inner side, known as PXD [3].

The PXD is intended to improve vertex resolution and will be placed close to the interaction point (IP). Because of the low momentum of the particles in the final state (< 1 GeV), the hit position determination is intrinsically limited due to the multiple Coulomb scattering. This sets a
lower limit of $10 \mu m$ for the spatial resolution in the PXD that can be achieved with a moderate pixel size of $50 \times 50 \mu m^2$. For the same reason the material budget must be kept low, up to a maximum of $\sim 0.2\%$ X0 per layer. The acceptance of the detector must cover the range $17^\circ - 155^\circ$. The detector will be read continuously with a frame time of $20 \mu s$ keeping the occupancy to less than $3\%$ as stated in \cite{2}. This expected occupancy is based on results of simulations where it is assumed that the detector is active all time (i.e. there is no dead time, as it happens with DEPFET sensors) and to which some safety factors have been applied. The continuous readout means that ASICs are “ON” all the time, which together with the restrictions on the material budget limit the options for cooling. Finally, according to the simulations, the radiation dose expected in the inner region of the detector is around 1 Mrad/year or higher.

The DEPFET (DEpleted P-channel Field Effect Transistor) \cite{4} technology was chosen as a baseline. The PXD will consist of two layers of DEPFET pixels at $R = 1.4$ and $2.2$ cm (figure 1). The PXD simulation was tuned using data taken in one of the Test Beams developed by the collaboration over real DEPFET prototypes. Such a detailed simulation gives the flexibility to explore different scenarios and, although the final DEPFET sensors are not yet produced, the results obtained running the full code give confidence that a single point resolution of $\sim 10\mu m$ can be achieved with such configuration.

2 The DEPFET sensor

Each DEPFET pixel consists of a field effect transistor (FET) integrated on a high resistivity n-type completely depleted silicon bulk (figure 2). A deep n-doping implantation creates a minimum of potential for the electrons around $1 \mu m$ underneath the transistor’s gate, in a region called internal gate. The signal electrons created in the substrate by the traversing particles, drift towards the surface of the device due to the electric field configuration and are accumulated in the internal gate. The charge accumulated in the internal gate modulates the current in the pMOS transistor, which is used as readout signal. This architecture allows producing very thin sensors with a high signal-to-noise ratio (SNR). The low capacitance of the internal gate provides an extremely low noise operation. The figure of merit is the $g_q$ factor, which defines the internal amplification of the device in terms of pA per collected electron. The values expected for the final sensors are in the order of $400 \text{pA}/e^{-}$ \cite{5}. After the readout the electrons are removed from the internal gate via a
clear contact (n+ type) that is placed on the periphery of each pixel. The potential barrier between the clear contact and the internal gate is modulated with an additional implant, called cleargate.

Thanks to its specific architecture, the DEPFET sensors provide detection with fast charge collection and internal amplification at the same time. The intrinsic noise is small, in the order of $\sim 50\,\text{nA}$, which makes possible to build thin detectors with an excellent SNR ratio [7]. For instance, in a 75 $\mu$m thick DEPFET sensor the typical signal size in electrons is $S = \sim 6000\,e^-$, which combined with a noise of $N = \sim 50\,\text{nA}$ and a $g_q$ of 400 $\text{pA}/e^-$ results in $\text{ENC} = \sim 125\,e^-$ and hence a final SNR $= \sim 48$. The DEPFET allows for low power operation since the detector is also sensitive in the off-state and the charge stays accumulated in the gate until is read later within a reasonable time (before the gates are saturated with thermal generated carriers). These characteristics made DEPFET also a promising candidate for a future $e^+ e^-$ collider at the energy frontier [6].

2.1 DEPFET pixels matrix

A DEPFET pixel detector is composed of a matrix of small DEPFET structures arranged in a rectangular shape and operated together in a rolling shutter mode (figure 3). The steering signals to operate the matrix, i.e. the pMOS gate signal and the clear, come from the so-called SwitcherB chip [8]. The pMOS drain current is digitized by the DCDB (Drain Current Digitizer) readout chip [9]. All the pixels lying on the same row have the gates and clear contacts connected to the same SwitcherB lines, whereas the ones on the same column have the drains tied together to the same DCDB input as depicted in figure 3. The chips are placed on the periphery of the matrix and connected to pixels through relatively long drain, gate and clear lines, which allows to keep most of the material out of the acceptance region. The source and cleargate contacts are all connected along the matrix. In the case of the Belle-II design, the matrix dimensions are shown in table 1 and consist of 250 $\times$ 768 pixels. For this matrices the drain lines have a length of up to $\sim 65.44\,\text{mm}$ and gate and clear lines of up to $\sim 12.5\,\text{mm}$, which corresponds to the dimensions of the active area of the largest half-modules.
Table 1. The Belle II ladder design parameters for the inner and outer layers.

|                  | Inner Layer (L1) | Outer Layer (L2) |
|------------------|------------------|------------------|
| Nr. modules      | 8                | 12               |
| Nr. half-modules | 16               | 24               |
| Distance to IP (cm) | 1.4            | 2.2              |
| Thickness (µm)   | 75               | 75               |
| Pixels/half-module | 768 × 250     | 768 × 250        |
| Total no. of pixels | 3.072 × 10⁶   | 4.608 × 10⁶     |
| Pixel size (µm²) | 55 × 50          | 70 × 50          |
|                  | 60 × 50          | 85 × 50          |
| Sensitive area (mm²)/half-module | 44.8 × 12.5 | 61.44 × 12.5 |

At any time during operation one pixel row is selected with the external gate and the drain current is measured. It will consist of the sum of the signal electrons and the pedestal present on the pixel. The drain currents of all the pixels in the row are digitized by the DCDB, which features 256 inputs. The pedestals are subtracted afterwards in the digital domain by the DHP chip (Data Handling Processor) [10]. After readout, the charge is cleared and the DEPFET starts to collect charge in the internal gate again. Each of the SwitcherB can drive 32 gate and clear lines.

It has been proven in lab measurements that the read-clear cycle can be done in 92 ns (10.83 MHz row rate) [11]. By using a 100 ns cycle, 76.8 µs would be needed to read out sequentially the full frame of 768 pixel rows. In order to increase the frame readout rate, four rows are read at a time and thus four DCDB devices are needed, as shown in figure 4. Since each of the SwitcherB steers 32 outputs, and each of the outputs is connected to four pixels rows, 6 SwitcherB devices are needed to drive a full half-module matrix. This results in 19.2 µs to read out a full frame, which fulfills the requirement of 20 µs (50 kHz frame rate) for a PXD matrix.

2.2 Sensor thinning

DEPFET sensors for Belle-II are thinned to 75 µm. The thinning of the sensor cannot be done using conventional techniques like backside grinding because, in the DEPFET sensors, the backside is electrically active. For that reason, a special technology has been developed [12]. It consists of an anisotropic etching on bonded wafers to create a thin, self-supporting sensor. Using this procedure, monolithic structures with thin sensors (75 µm in the Belle II case) can be produced directly integrated on a thick frame (450 µm). Such a silicon module needs no additional support structure (figure 5) and has also the advantage of a uniform and small thermal expansion since one only type of material (Si) is used.

2.3 The module concept

A DEPFET ladder consists of two self-supporting half-ladders glued together front to front (figure 4) with a ceramic reinforcement beam.

Three different types of ASICs are bump bonded on the module, namely, the DCDB, the SwitcherB and the DHP. For the bump bonding, a solderable landing pad on the sensor substrate is needed. For that end and other purposes as well, a 3rd metal layer made of copper has been
introduced in the module 3-metal layer structure (figure 6). Passive components such as decoupling capacitors and termination resistors of sizes 01005 and 0201 are also soldered on the module. Signal and power lines are routed on three metal layers, two of aluminum and the top one of copper. With this kind of design, a compact and low material budget can be constructed, as required from the PXD specifications. A breakdown of the detector material (in units of radiation lengths) over the acceptance with the most important contributions is presented in figure 7. The ladder material corresponds to 0.21% X0/layer over the active area. As shown in the figure, there is no contribution from the DCDB and the DHP to the material since they are placed out of the acceptance.

2.4 The readout ASICS

The matrix row control is provided by the SwitcherB [8]. It is implemented in AMS/IBM high voltage 0.18 μm technology. It applies the gate and clear signals to the sensor and it is capable of delivering a high voltage pulse (20 V) for clearing the charges in the internal gate in 15 ns.

The analog frontend is the DCDB [9]. Made in UMC 180 nm technology, this chip has 256 channels and amplifies and digitizes (8 bit) the drain currents of the pixels independently. The
The analog input current receiver of each channel, which is based on a transimpedance amplifier, keeps the drain line potential constant (necessary to achieve fast readout), compensates for variations in the DEPFET pedestal currents, and amplifies and shapes the signal.

The data from the DCDB is transmitted to the DHP [10], built in IBM CMOS 90 nm technology for the first prototypes and moved to 65 nm TSMC for the final version. This chip implements the digital domain and is able to perform the common mode correction, pedestal subtraction, zero suppression and data transmission at 1.6 Gbps. In addition, it is the responsible of the timing signal generation for the rest of the ASICs.

3 Full readout chain and back-end infrastructure

The DEPFET module is interfaced to the external world through a Kapton cable attached at the DHP devices end using paste solder and wire-bonding. Figure 8 depicts the full-scheme from the DEPFET module to the power supply and computing infrastructure, with two passive patch-panels and the DHH (Data Handling Hybrid) in the way through.

The 49 cm long flex Kapton cable connects the data and power patch-panels. The data patch-panel redistributes the fast and slow signaling to the DHH. On the one hand, the DHH gets the timing and trigger signals and the slow control commands from the Belle-II environment and re-transmits it to the DHP devices. On the other hand, it receives the data from the four DHP devices, multiplexes it and transmits it via optical link to the back-end ATCA (Advanced Telecommunications Computing Architecture) architecture computing nodes, where further data buffering and data reduction via ROI (Region Of Interest) selection is performed. The power patch-panel is used to
redistribute the power lines and for filtering and decoupling. The power supply system to operate the DEPFET modules is a complex one in terms of number of different supply channels (∼ 20 voltage levels), noise performance sensitivity and voltage regulation, as described in [13].

4 Performance results

Many beam tests were performed with different types of thick (400 µm) DEPFET sensors in the past, but here we will only focus on the results related to thinned prototypes. In May 2013 a beam test was performed at DESY (Hamburg). The DUT was the so-called PXD6, a 50 µm thin PXD like sensor of 32 × 64 pixels size, together with a DCDB and a SwitcherB. The pixels pitch was 50 × 75 µm² and two different gate lengths of the pixel were evaluated. In this test both the SwitcherB and DCDB were operated at full speed, i.e. 100 ns read-clear cycle. The results show that these sensors exhibit 99% charge collection efficiency. The SNR for MIPs is between 20–40 depending on gate length of the PXD prototype matrix. In figure 9 the charge distribution of one of the prototypes with the baseline design gate length of 4 µm is shown. It features a MPV (Most Probable Value) of 23.9 ± 0.3, and SNR = 41.5 ± 0.4 and a $g_q \approx 450$ pA/e⁻. A resolution of ∼ 10 µm was achieved with these thinned sensors, as shown in the residual distribution plots of figure 10.

Tests with the complete FE readout chain (PXD6 + DCDB + DHP + SwitcherB) have been performed with laboratory test setups. In this case, the same kind of thin sensors matrix was used. After the voltage biasing optimization measurements with a $^{241}$Am radioactive source were performed (figure 11) and also charge collection homogeneity scans. Analysis of the data taken with the complete readout chain and some other final components (such as power supplies, DAQ software and slow control software) is still in progress at the time of writing but some preliminary results of Landau distributions are already available (figure 12).

5 The EMCM — Electrical Multi-Chip Module

The EMCM is an electrically active prototype of a half-module, it is a replica with the exception that it does not contain the DEPFET implantations. The aim of the EMCM is to study and char-
Figure 11. $^{241}\text{Am}$ spectrum, zero-suppression performed with the DHP, $g_q \sim 500 \text{pA/e}^-$. 

Figure 12. Landau distribution 4 GeV $e^-$, perpendicularly incidence, $g_q \sim 500 \text{pA/e}^-$. 

Figure 13. Fully populated EMCM module (left). Bump bonded SwitcherB and passives (right).

6 Thermal studies

The power dissipation of the PXD must be removed with minimal material in the acceptance region. Finite element simulations and laboratory measurements have demonstrated [14] that the detector...
can be cooled by means of 2-phase CO$_2$ through massive structures outside of the acceptance in the module ends, where most of the heat is produced. The center of the ladders has to rely on forced convection with cold dry air. The total power consumption is around 9 W per half-module (0.5 W the SwitcherBs, 6 W the DCDBs, 2 W the DHPs and 0.5 W distributed homogenously along the active area), giving a total power consumption of 360 W for the full detector. The temperature of the sensors (to keep the leakage current at modest levels) and chips (to prevent electro-migration) should not exceed 30°C and 60°C respectively.

The validity of the simulations is corroborated by measurements on a thermal mockup that recreates the PXD detector in conditions similar to the experiment. It was built using silicon dummy modules with integrated resistors and populated with many temperature sensors. It was verified that a combination of active contact cooling with 2-phase CO$_2$ at $-30^\circ$C in the end flanges and convective cooling in the acceptance region is needed to keep temperate around or below the limits. With a room temperature of 25°C, the measurements show that the ladders can be efficiently cooled achieving temperatures below 25°C in both the sensor and SwitcherB area (figure 14). The temperature gradient along the sensor region is kept below 5°C for the entire length with convective and active cooling. An airflow of 2 m/s is enough to decrease and homogenize the temperature distribution (figure 15) [14].

7 Conclusions

A vertex detector based on DEPFET technology is being developed for the new Flavor Factory (SuperKEKB) under construction in KEK (Japan). This machine will deliver a luminosity never achieved before and the requirements for the PXD are stringent in terms of resolution, power consumption and material budget. The experiment will be ready for data taking on 2015 and the PXD entered the construction phase. Several key points of the detector design and construction have already been achieved, such as verifying that a thin sensor can be operated at the nominal speed needed in Belle II and the temperature of the detector can be controlled using the cooling principle adopted by the Collaboration. The full readout chain with most of the final system electronics is being tested in beam-tests at DESY. The construction of EMCM is an important step forward in un-
derstanding how to develop the final size monolithic modules thanks to the feedback it will provide on the metallization process and electrical properties as well as on the commissioning procedures.

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