SlackQ : Approaching the Qubit Mapping Problem with A Slack-aware Swap Insertion Scheme

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Abstract—The rapid progress of physical implementation of quantum computers paved the way for the design of tools to help users write quantum programs for any given quantum device. The physical constraints inherent in current NISQ architectures prevent most quantum algorithms from being directly executed on quantum devices. To enable two-qubit gates in the algorithm, existing works focus on inserting SWAP gates to dynamically remap logical qubits to physical qubits. However, their schemes lack consideration of the execution time of generated quantum circuits. In this work, we propose a slack-aware SWAP insertion scheme for the qubit mapping problem in the NISQ era. Our experiments show performance improvement by up to 2.36X at maximum, by 1.62X on average, over 106 representative benchmarks from RevLib [1], IBM Qiskit [2], and ScaffCC [3].

I. INTRODUCTION

Quantum computing has been considered as a potentially disruptive computation model. In 2019, Google [4] demonstrated “Quantum Supremacy” with its 54-qubit quantum processor that is able to perform a computational task in 200 seconds which would have taken the state-of-art classical supercomputer 10,000 years. In general, quantum computing has significant advantage over classical computing for applications including large number factoring [5], database search [6], and quantum simulation [7].

Labs in academia and industry are now able to build quantum computers with up to 49-72 qubits. IBM [8] released its 53-qubit quantum computer in October 2019 and has made it available for commercial use. Google [9] released the 72-qubit Bristlecone quantum computer in March 2018. Intel [10] and Rigetti [11] respectively have released quantum computing devices with dozens of qubits. Further, a few small-scale quantum computers with less than 20 qubits are made freely available to the public [12], for example, the series of quantum computers provided by IBM Q experience [12].

The physical constraints inherent in quantum architectures prevent quantum algorithms from being directly executed on the device. One of the major constraints that must be accounted for before quantum algorithms can be executed is the qubit connectivity constraint. In the superconducting-based quantum computers (the implementation adopted by major industry players such as IBM and Google), qubits are not fully connected. It follows nearest neighbor (NN) interaction model, enforced by the connectivity of the physical qubits array. If an algorithm requires communication between qubits that are not physically connected, the algorithm cannot be directly executed on the device.

To solve the qubit connectivity problem, any two logical qubits that need to communicate according to the algorithm must be mapped to physical qubits on the device that are neighboring (connected). This is done through one or a sequence of SWAP operation(s). A SWAP operation exchanges the states of two neighboring qubits, in effect “moving” the two qubits. An example is shown in Fig. 1. This dynamic remapping between logical and physical qubits may need to happen multiple times throughout the algorithm.

Inserting swap operations inevitably results in increased gate count and execution time. Previous studies [13], [14], [15], [16], [2], [17] focus on optimizing gate count but not execution time. Execution time is an important measure of the performance of a circuit. Minimal gate count do not necessarily guarantee minimal time. We show an example in Fig. 1 where two qubit mapping solutions yield the same gate count but only one of them is optimal in time.

Optimizing the execution time of a circuit is important not only for optimizing the performance but also for improving the fidelity of a quantum circuit. Quantum computers are not perfect. Qubits are fickle and error prone. As time goes by, a qubit decoheres and error accumulates. The time a qubit can survive without losing its state information with high probability is called coherence time. The longer a circuit has to execute, the more likely it will approach a qubit’s coherence time. IBM proposes the metric of quantum volume [18] for evaluating the effectiveness of quantum computers. One important factor for calculating quantum volume is the maximum depth of a circuit that can be executed by a quantum computer before accumulating a certain amount of error. Here the depth represents the amount of time a circuit executes. Optimizing the depth of a circuit is important as only circuits that fit into the quantum volume can run successfully and generate meaningful computational results. Thus quantum compilers must take the execution time of the generated circuit into consideration.
In this paper, we focus on time-aware qubit mapping. A good time-aware qubit mapper needs to yield a hardware-compliant circuit while having optimal or near-optimal execution time. We discover the key is to find intervals with slack in the circuit and to use the slack to hide the latency of inserted swap operations. We present important considerations for detecting and exploiting slack in the circuit. Our implemented qubit mapper named SlackQ automatically searches for dynamic qubit mappings given an input program on a quantum architecture with arbitrary qubit connectivity. The experiments show that SlackQ improves performance by up to 2.36X, by 1.62X on average, over 106 representative benchmarks from RevLib [1], IBM Qiskit [2], and ScaffCC [3].

II. BACKGROUND AND MOTIVATION

A. Quantum Computing Basics

1) Qubit: A quantum bit or qubit, is the counterpart to a classical bit in the realm of quantum computing. Different from a classical bit that represents either ‘1’ or ‘0’, a qubit is in the coherent superposition of both states. The state $-\psi_\perp$ associated with a qubit is a unit vector in a two-dimensional vector space. The state of a qubit can be represented as

$$|\psi\rangle = \alpha|0\rangle + \beta|1\rangle = \begin{bmatrix} \alpha \\ \beta \end{bmatrix},$$

where $\alpha$ and $\beta$ are two complex numbers such that $|\alpha|^2 + |\beta|^2 = 1$. $\alpha$ and $\beta$ are called amplitudes. Upon the standard measurement, the state $-\psi_\perp$ will collapse into the basis state $-0_\perp$ with probability $|\alpha|^2$ or the basis state $-1_\perp$ with probability $|\beta|^2$. A system of $n$ qubits encodes a state superposition of $2^n$ basis vectors with $2^n$ amplitudes. The classical n-bit system encodes the information of one basis vector in the vector space, but n-qubit system encode the information of $2^n$-dimensional vector space. Operating on one n-qubit state is as if operating on $2^n$ complex numbers at one time. This is one of the reasons for the potential exponential speedup using quantum computing.

2) Quantum Gates: There are two types of elementary quantum gates. One is the single-qubit gate, which is a unitary quantum operation that can be abstracted as the rotation around the axis of the Bloch sphere [19]. A single-qubit gate can also be represented using a 2 by 2 unitary matrix. Important single-qubit gates include the H (Hadamard) gate, and the S (phase shift by $\pi/4$) gate [20].

The second type of gate is the multi-qubit gate. The controlled-NOT (CNOT) is a two-qubit gate that performs the most important role (arguably) in quantum computation. The two qubits involved in a CNOT gate are: the control qubit and the target qubit. If the control qubit is 0, it leaves the target qubit unchanged. If it is 1, it applies a NOT gate to the target qubit. The CNOT gate entangles qubits and allow qubits to communicate. The CNOT gate, H gate, S gate, and T gate together form a universal set called the Clifford+$T$ library. Any quantum algorithm can be implemented using a composition of gates from the universal set.

3) Quantum Circuit: A quantum algorithm can be expressed as a quantum circuit which is composed of a set of qubits and a sequence of quantum operations on these qubits. A quantum circuit can be thought of a quantum algorithm in “assembly language”. There are two different ways to describe the quantum circuits. One way is to use a circuit diagram, in which qubits are represented as horizontal lines. Input is the on the left and output is on the right. Unlike a classical circuit, a quantum circuit must have the same number of input and output qubits. Fig. 1(b) shows an example quantum circuit diagram. Logical qubits are denoted using lowercase letters ($q_1, q_2, ...$) and physical qubits are denoted using uppercase letters ($Q_1, Q_2, ...$). Initially, logical qubits $q_1, q_2, q_3, q_4$, and $q_5$ are mapped to physical qubits $Q_1, Q_2, Q_3, Q_4,$ and $Q_5$. A single-qubit gate is denoted as a square on the line. A CNOT gate is represented as a line connecting two qubits where the control qubit is marked with a dot and the target qubit with a $\oplus$ sign. In this paper, we use the circuit diagram representation to describe examples.

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Fig. 1: (a) Physical qubit connectivity; (b) the original logical circuit (logical qubits $q_1, q_2, q_3, q_4, q_5$ are mapped to physical qubits $Q_1, Q_2, Q_3, Q_4, Q_5$); The gate marked in red is the CNOT gate that cannot be executed due to a connectivity constraint (as $Q_2$ and $Q_5$ are not physically connected). (c) uses 1 swap but the execution time of the circuit is not increased; (d) uses 1 swap but the execution time of the circuit is increased. The operations marked in blue are swap operations. We assume a swap operation can be decomposed into three CNOT gates and each gate takes 1 cycle in this example.
B. Qubit Mapping Problem

To enable the execution of a quantum circuit, the logical qubits in the circuit must be mapped to the physical qubit on the target hardware. When applying a CNOT gate, the two logical qubits involved in the CNOT gate must be mapped to two physical qubits connected to each other. Due to the irregular layout and connectivity of the qubits in the target device, it is sometimes impossible to find an initial mapping that makes the entire circuit CNOT-compliant. The common practice is to insert SWAP operations to remap the logical qubits, whenever a CNOT gate cannot be applied.

A SWAP operation exchanges the states of the two input qubits of interest. As shown in Fig. 2(b), a swap operation is implemented using 3 CNOT gates for architectures with bi-directional links, where a bi-directional link means both ends of the link can be the control or target qubit. Or it can be implemented using 3 CNOT gates plus 4 Hadamard gates for architectures with single-direction links as shown in Fig. 2(c), where a single-direction link means only one end of the link can be the control qubit.

The qubit mapping problem takes a logical circuit and a hardware coupling graph as input and outputs a transformed circuit that fits on the hardware device by inserting SWAP operations. After the transformation, all CNOT gates must be performed on qubits that are connected in the physical architecture. Due to the swaps, a logical qubit may be mapped to different physical qubits at different points in the circuit execution. But, at any given point, a logical qubit will be mapped to exactly one physical qubit since we are only using swaps to move qubits and are not making any copies.

\[
\begin{align*}
\text{(a)} \quad & \quad m \leftrightarrow n \\
\text{(b)} \quad & \quad m \leftrightarrow n \\
\text{(c)} \quad & \quad m \leftrightarrow n
\end{align*}
\]

Fig. 2: Implementation of a SWAP operation: (a) the SWAP notation, where m and n are two logical qubits, after SWAP, m and n exchanged their states, (b) for bidirectional links, where the three CNOT that implement the SWP do not need to use the same control qubit, and (c) for single direction links, where the three CNOT must use the same control qubit.

An example of circuit transformation is shown in Fig. 1 where (a) is the physical connectivity, (b) is the original circuit, (c) and (d) offer two different hardware-compliant circuits generated from the same original circuit.

C. Parallelism in Quantum Circuit

Like in classical computers, parallelism is also important in quantum computers. Parallelism comes from independent operations on different qubits. Gates on the same qubit have to run sequentially. For instance, if a and b are two consecutive gates on the same qubit, and a is before b in the program, then gate b depends on a. Gates that do not share any qubit are independent. A two-qubit gate depend on up to two gates since it involves two qubits. A two-qubit gate has up to two immediate successors in the dependence graph. A dependence graph can be built with respect to the partial order between gates. It is a directed acyclic graph (DAG).

In a transformed circuit, the parallelism could be (1) between the gates in the original circuit (as \(g_2\) and \(g_3\) in Fig. 1(b)), (2) between the SWAP gates that are inserted into the original circuit, and (3) between a gate in the original circuit and a newly inserted gate (as \(\text{swap} \ 3,5\) and \(g_1\) in Fig. 1(c)). A good qubit mapping algorithm should consider all types of parallelism. However, existing studies only consider the first two types of parallelism. Our work is the first one that systematically exploits all type of parallelism.

As shown in Fig. 1, the best two known approaches by Zulehner et al. \cite{16} and Li et al. \cite{13} do not distinguish solution (c) from solution (d) as the two solutions both insert 1 SWAP. And \cite{16} and \cite{13} only optimize the number of gates inserted into the circuit (or the parallelism of the inserted gates), but not the parallelism of the transformed circuit. The solution in Fig. 1(c) is better than Fig. 1(d) as the inserted swap can run in parallel with the gates in the original circuit. This example stresses the importance of time-awareness in SWAP insertion schemes and motivates our work.

III. INSIGHT AND DESIGN

To improve the parallelism between the inserted SWAP operation and the gates in the original circuit, we discover that it is important to exploit the slack intervals in the circuit. The slack represents the idle time in the original circuit for a given set of qubits. The key is to hide the latency of inserted swap operations by using the qubits that are idle at that time of the circuit execution. This forms the main idea of this paper and we insert SWAP operations such that they leverage slack in the circuit as much as possible.

A. Slack

We define slack as the idle time between two consecutive gates on the same qubit(s) and can be used to perform SWAP operation without affecting the total execution time of the entire circuit. The slack time is usually caused by dependence between gates and/or variation of gate count on individual qubits.

The slack time due to dependence between gates only occurs when there are two-qubit gates in the circuit. Recall that a CNOT gate depends on up to two other gates, since CNOT is a two-qubit gate. If the qubits are running at different speeds, one of the other qubits might be ready earlier than the other. The faster qubit thus needs to wait for the slow qubit to finish before the CNOT gate can be executed. On the other hand, if a circuit has a number of qubits, and the number of gates on each qubit is different (even if they are all independent), then some qubits will inevitably be idle at some point of the execution. The slack intervals can be used for inserting swap operations that resolve qubit mapping constraints. An example of slack in the circuit is shown in Fig. 3.
There are two types of slacks in the circuit. One type does not require the rescheduling of the gates, and we define it as **fixed slack**. The other type of slacks may have variable number of cycles, and we denote it as **flexible slack**. A good qubit mapper needs to search globally and exploit both fixed and flexible slack.

**a) Fixed Slack:** An example of fixed slack is shown in Fig. 3(b). Assuming each gate takes one cycle, there is a fixed slack between $g_1$ and $g_2$ on qubit $q_2$. Here it cannot delay $g_2$ or start $g_1$ early if the total execution time needs to remain unchanged. If qubit $q_2$ is used to perform another gate such as the swap operation during the three cycles, it will not affect the execution time of the entire circuit. In this case, the number of cycles that can be used on $q_2$ between $g_1$ and $g_2$ is fixed.

**b) Flexible Slack:** Sometimes fixed slack does not always exist. It is necessary to move the gates in order to create slacks for latency hiding purpose. We show an example Fig. 3(c) and (d), where slack can be created by moving $g_1$. Let’s say $\text{cnot}(q_1, q_2)$ and $\text{cnot}(q_3, q_4)$ are scheduled on cycle 1. The three single-qubit gates on $Q_1$ are scheduled on cycle 2,3,4 respectively. With this going on, $g_3$ expects to be executed on cycle 5 at the earliest. $g_3$ depends on $g_1$. $g_1$ can be scheduled at the second cycle, the third cycle (Fig. 3 (c)) or the fourth cycle (Fig. 3 (d)) without delaying $g_5$. To this end, a slack with zero, one or two cycles can be created between $q_2$ and $g_1$, depending on when $g_1$ is scheduled. And this type of slack between $g_2$ and $g_1$ is flexible. On the other hand, since $g_1$ is not directly executable due to the connectivity constraint in Fig. 3 (a), the more slack intervals before $g_1$ there are, the better it is for hiding the swap latency. In Fig. 3 we show that by moving $g_1$ forward, $q_2$ and $q_3$ can have more slack intervals before $g_1$, and $\text{swap}(3,4)$ is inserted which utilizes the slack, resulting in a total circuit time of 6 cycles only, which is optimal in this case.

It is worth mentioning flexible slack could be cascading as the rescheduling of one gate might affect its descendants or predecessors. For the fixed slack, the gates involved cannot be delayed without affecting the circuit time. Flexible slack allows one or multiple gates to delay start within reasonable time window(s). Flexible slack are more complicated than fixed slack. It is necessary to analyze and exploit flexible slack in a systematic way.

### B. Dynamic Gate Scheduler

We model the resolution of qubit mapping conflicts as a dynamic scheduling process. Gates in the circuit are scheduled as soon as their dependencies are resolved. When a gate cannot be scheduled due to a connectivity problem, we insert a (combination of) swap(s) to change the qubit mapping so that the gate can be executed on the physical device. All the gates that have already been scheduled at one point of scheduling are called the Processed Circuit, and the gates that still await scheduling are called the Remaining Circuit.

Fig. 4 shows an example of how the scheduling works. With initial mapping of $\{q_1, q_2, q_3, q_4\} \rightarrow \{Q_1, Q_2, Q_3, Q_4\}$, the first two CNOTs $\text{cnot}(q_1, q_2)$ and $\text{cnot}(q_3, q_4)$ and the three single-qubit gates on $Q_1$ can be scheduled without remapping. At this point, those gates that are scheduled are part of the Processed Circuit. The remaining two CNOT gates ($g_1$ and $g_3$) that cannot be scheduled are part of the Remaining Circuit. Gate $g_1$ cannot be scheduled because $Q_2$ and $Q_3$ are not connected in the device. Gate $g_3$ cannot be scheduled because $g_1$ must be scheduled before $g_3$ (write-after-read dependency on $Q_2$). The dashed lines divide the circuit into processed part and remaining part.

To minimize the circuit time, we search for swap candidates for $g_1$ that results in maximally hiding swap latencies using circuit slack. Fig. 5 shows the key idea behind the searching for optimal swap candidates. The search reveals multiple hardware-compliant candidates that utilize different sequences of swaps to achieve compliance. We choose the optimal candidate by calculating the Slack Utilization of each candidate, and choosing the one with the best utilization. In Fig. 6 we choose swap candidate $\text{swap}(q_3, q_4)$ since it best hides the swap latency behind the 2-cycle slack shown in Fig. 6 (d). Now $g_1$ is satisfied and scheduling can proceed.

### C. Critical Gates

The gates in the remaining circuit pending scheduling whose dependences have been resolved but connectivity problems haven’t been can be divided into two groups: those on the critical path and those that are not. We denote the gates on the critical path as **critical gates**, and the others as **non-critical gates**. In parallel computing, the critical path length is equal to the execution time when there is enough parallelism. In this case, the critical path is equal to execution time as the maximum parallelism (the maximum number of gates that can run concurrently) is at most the same as the number of qubits. Thus it is important to prioritize the scheduling of critical gates over non-critical gates.

To prioritize critical gates, what we need to do is to resolve the connectivity problems of critical gates as early as possible. Imagine a scenario where two gates have connectivity problems, one gate is critical and the other is non-critical gate. Their connectivity issues cannot be resolved at the same time. Under this situation, we should resolve the critical gate first, as resolving the non-critical gates can be likely delayed without affecting the overall execution time.
We use an example from Fig. 7 to show how criticality can play an important role in determining the overall circuit time. We use a five-qubit quantum machine, whose connectivity is shown in Fig. 7(a). This example circuit consists of 4 CNOTs and 3 single-qubit gates, with $g_1$, $g_2$ scheduled, and $g_3$, $g_4$ not yet scheduled due to connectivity issues. It’s crucial to note that $g_3$ is on the critical path, while $g_4$ is not. The two gates $g_3$ and $g_4$ cannot be resolved at the same time if both of them want to use only one swap, since qubit $C$ is the on the path from $T_1$ to $T_2$, and from $X_1$ to $X_2$. Whether to prioritize $g_3$ over $g_4$ when using the hub qubit $C$ for swap, makes a big difference in terms of circuit time. We show this discrepancy by illustrating two strategies and their resulting circuits.

- **Strategy One - Prioritizing critical gates** Resolve $g_3$ first. Shown in Fig. 7(c), it is necessary to insert swap($q_2$, $q_3$) before $g_3$. After $g_3$ is resolved and scheduled, swap($q_2$, $q_4$) is inserted such that $q_4$ can be resolved. swap($q_2$, $q_4$) can take advantage of the slack on logical qubits $q_2$ and $q_4$, as logical qubit $q_1$ is processing three single-qubit gates. This strategy results in total circuit time of 10 cycles, assuming CNOT and single-qubit gate both have latencies of one cycle.

- **Strategy Two - Not distinguishing critical gates from non-critical path** Resolve $g_4$ first. Shown in Fig. 7(d), it is necessary to insert swap($q_3$, $q_4$) before $g_4$, and let $g_4$ be scheduled. In the meantime, $g_3$ has to wait, which results in the critical path being elongated due to the delay of the execution time of $g_4$ and swap($q_3$, $q_4$). It is because when $g_4$ is being executed, the mapping that allows $g_4$ must be kept, which will delay all the remaining gates. In this case, it is not desirable to delay all the remaining gates as they are on critical path. Delaying gates that are critical will have a more detrimental impact than delaying gates not on critical path. After $g_4$ is resolved, the fastest way to resolve $g_3$ is to swap($q_2$, $q_4$) before $g_3$. This strategy as a whole results in total circuit time of 13 cycles, which is 30% more than strategy one.

It can be seen from this example the later resolving of the non-critical gates are highly likely to overlap with the gates on the critical path, and result in less impact to overall circuit execution.

### IV. Implementation

Based on the design consideration on Section III, we implement a slack-aware qubit mapping framework called SlackQ.

#### A. Overview of SlackQ

Our algorithm is an iterative gate scheduler which dynamically resolves the connectivity issues encountered during the scheduling process. Initially, a dependency graph of the circuit is built. Then we traverse the dependency graph of the circuit...
and schedule the gates one by one. We keep a frontier set of gates ready to be scheduled. When resolving the connectivity issues, we invoke a priority-queue based searcher for swap candidates. It returns hardware-compliant candidates. Among these hardware-compliant candidates, the one that has the best slack utilization is chosen, and the scheduling process proceeds. We describe the algorithm below with respect to the pseudo-code shown in Algorithm 1:

**Step One - Initialization** This step prepares for the searching process. It builds the dependency graph of circuit. It finds the gates that do not depend on any other gates. Then it places those gates into the frontier \( F \). It also initializes the processed gate set \( P \) as empty set, and the remaining gate sets \( R \) as the entire circuit.

**Step Two - Schedule Ready Gates** This step goes through frontier list \( F \). It finds all gates in \( F \) that can be scheduled immediately due to having no connectivity issues according to the current mapping \( \pi \). It schedules all these gates. When finishing the scheduling of one gate, it finds the descendant gate and see if this descendant’s other parent has also been scheduled. If this is the case, the descendant gate’s dependency is resolved. It then places this descendant gate into \( F \). This step is repeated until \( F \) contains no gate that can be scheduled with respect to the current qubit mapping.

**Step Three - Resolve Qubit Mapping Conflicts** We go through the frontier \( F \) again, finding the gates with resolved dependencies but are constrained by the current mapping and are on the critical path of the remaining circuit. Put those gates into a set called \( F_{\text{critical}} \). Run a priority queue based searcher for hardware-compliant mappings. Our mapping searcher here returns a list of hardware-compliant mappings candidates, called \( M \). Among these candidates, it finds the one (call it \( m \)) with the best slack utilization. Then we use the swap sequence associated with \( m \) to update the mapping \( \pi \) and add the swap sequence into the processed circuit \( P \).

**Step Four** Repeat Step Two and Three until all gates are scheduled in the circuit. Return transformed circuit.

In Sections [IV-B] to [IV-D], we describe a few important aspects of this algorithm.

**B. Initialization**

Before calling the scheduler described in Algorithm 1, we initialize the frontier \( F \) and processed circuit \( P \), and the remaining circuit \( R \). Initially, \( P \) is empty and \( R \) is the entire circuit. For \( F \), it creates a Directed Acyclic Graph (DAG) to represent the dependency between quantum operations. Fig. 8 (a) shows an example of a dependency graph from the circuit illustrated in Fig. 1 (b).

**Algorithm 1: Dynamic Gate Scheduler**

**Input:** Frontier \( F \), initial mapping \( \pi \), processed circuit \( P \), remaining circuit \( R \)

**Output:** Transformed circuit \( T \)

while \( F \) not empty do
    \( E = \text{getSchedulableGates}(F, \pi); \)
    while \( E \) not empty do
        \( F_1 = \text{getSchedulableGates}(F, \pi); \)
        for \( g \in E \) do
            \( F_2 = \text{getSchedulableGates}(F, \pi); \)
            for \( d \in g\text{'s children} \) do
                if \( d \text{'s dependency is resolved} \) then
                    \( F_2.add(d); \)
                end
            end
        end
        \( E = F_1; \)
    end
    \( E = \text{getSchedulableGates}(F, \pi); \)
end

\( F_{\text{critical}} = \text{select_critical_gates}(F); \)
\( \text{mapping_candidates} = \text{resolve_conflicts}(F_{\text{critical}}, \pi); \)
\( m = \text{best_slack_utilization} (\text{mapping_candidates}, P, R); \)
\( \pi = \text{update_mapping_with_swaps}(m, \pi); \)
\( P.add(m\text{'s swaps}); \)
end

return \( P \);

**C. Choosing the Best Mapping Candidate**

With multiple hardware-compliant mappings, it is necessary to determine the candidate that has the best slack utilization. The best slack utilization means the inserted swap sequence makes best use of the slack currently existing in the circuit. To evaluate these mapping candidates, for each of them, we tentatively insert the associated swap sequence and monitor...
Algorithm 2: Find the best slack-utilizing mapping

Input: Mapping candidates \( M \), dependency graph \( G \), processed circuit \( P \)

Output: Best slack-utilizing mapping \( m_{\text{best}} \)

smallest_inc = \( \infty \);
CP = getCriticalPath\( (G) \);
for \( m \in M \) do
  \( RG = \) getLastScheduledGateOnEachQubit\( (P) \);
  \( G' = G; \)
  \( G'.addGates(m.\text{swaps}); \)
  \( \text{graph\_updated = True}; \)
  \( \text{circuit\_time = 0}; \)
  while \( RG \) not empty do
    \( RG'' = []; \)
    for \( g \in RG \) do
      \( g.\text{updateTentativeStartAndEndCycle}(); \)
      \( \text{delta = g.\text{tentativeStart} - g.\text{originalStart}}; \)
      if \( g \) is on critical path & \( \text{delta} \geq \text{smallest\_inc} \) then
        \( \text{graph\_updated = False}; \)
        break the while loop;
      end
      if \( \text{delta} \geq 0 \) then
        \( \text{RG'.add(g.\text{children});} \)
      end
      \( \text{circuit\_time = max(circuit\_time, g.\text{tentativeEnd});} \)
    end
    \( \text{RG = RG'}; \)
  end
  if \( (\text{graph\_updated == True} \land \text{circuit\_time} > \text{CP}) \) then
    if \( (\text{circuit\_time} - \text{CP}) < \text{smallest\_inc} \) then
      smallest\_inc = \( \text{circuit\_time} - \text{CP}; \)
      \( m_{\text{best}} = m; \)
    end
  end
end
return \( m_{\text{best}} \);

Given \( F_{\text{critical}} \) and current mapping \( \pi \), it starts searching the state space of all feasible mappings that satisfy \( F_{\text{critical}} \). It picks a node to expand and enumerate all possible parallel one-step swaps as the node’s successors. We use a priority queue that is similar to that in [16]. Unlike the work by [16] where the search stops when the first state node that resolves all connectivity conflicts is retrieved from the priority queue, our search stops after \( m \) expansions since the mapping candidate with minimal swap count is found, or when the gate count of the mapping candidate that is just retrieved has less than or equal to \( k \) times more gates than the minimal swap count.

We set \( m = 20 \) and \( k = 2 \) such that the returned mapping candidate will have reasonable gate counts. After all mapping candidates have been retrieved, we rank them with respect to
the metric of best slack utilization discussed above.

V. EVALUATION

In this section, we evaluate our slack-aware swap insertion scheme (SlackQ) and compare it with the two state-of-the-art qubit mappers, respectively by [16] and [13].

A. Experiment Setup

**Benchmark.** We use 106 benchmarks from RevLib [1], IBM Qiskit [2], and ScaffCC [3]. RevLib comprises of a collection of benchmarks in the domain of reversible and quantum circuit design. Qiskit is a programming framework for quantum computing provided by IBM. ScaffCC is a compilation framework for the Scaffold quantum programming language. These benchmarks feature functionalities from implementing ALU logics, comparing inputs with constant values, ternary counters, to classic quantum algorithms like Quantum Fourier Transform (QFT) and ising model.

**Baseline** We compare our work with two best known qubit mapping solutions [16] (denoted as Zulehner) and the Sabre qubit mapper from [13] (denoted as Sabre). We also compare our results with IBM’s stochastic mapper in Qiskit [2]. Since IBM’s Qiskit mapper is significantly worse in terms of circuit time than all other mappers we have evaluated, we do not show the results. The performance of Qiskit mapper is also noted in the work by [16].

**Metrics** We compare the execution time of the transformed circuits generated by different qubit mapping strategies. It is worth mentioning that our approach can take any gate latency as input parameters and generate transformed circuits based on the input. However, to make evaluation results as close to real machines as possible, we use the results from the studies by [22], [23]. In these studies, different types of quantum architecture are investigated, and the studies reveal that two-qubit gates usually takes around twice as much time as single-qubit gates. Hence we assume single-qubit gates take 1 cycle and two-qubit CNOT gates take 2 cycles in our experiments. The time is reported as the total number of executed cycles.

**Platform** We use IBM’s 20-qubit Q20 Tokyo architecture [13] as the underlying quantum hardware. The qubit mapping approach is implemented in C++ and executed on a Intel 2.4 GHz Core i5 machine, with 8 GB 1600 MHz DDR3 memory.

B. Experiment Analysis

We categorize the 106 benchmarks into four categories. Benchmarks in the first category each has less than 200 gates, and we denote them as mini benchmarks. There are 22 mini benchmarks. The second category has benchmarks with 200 to 1,000 gates. We name this category as small benchmarks. There are 39 small benchmarks. The third category of benchmarks have 1,000 to 10,000 gates. We name it as medium benchmarks and there are 21 benchmarks in this category. The fourth category of benchmarks have 10,000 to 200,000 gates. We refer to it as large benchmarks and there are 24 benchmarks in this category. The results for mini, small, medium, and large benchmarks are presented in Fig. 9, Fig. 10, Fig. 11 and Fig. 12 respectively.

![Speedup for Mini Benchmarks](image1)

Fig. 9: Speedup for Mini Benchmarks (≤ 200 gates)

![Speedup for Small Benchmarks](image2)

Fig. 10: Speedup for Small Benchmarks (≤ 1000 gates)

It can be observed from the results that as the problem size scales, the performance improvement brought by SlackQ improves. For most benchmarks in the mini and small category, the speedup is between 1.1X and 1.5X. However, for the medium and large category, the speedup for most benchmarks is above or around 1.5X. The average speedup for mini benchmarks is 1.45X and for small, medium, and large
benchmarks, the average speedup becomes 1.55X, 1.70X, and 1.86X respectively. The results show that our approach works well in general, and in particular for larger benchmarks.

There are two baselines we compare against: the Zulehner approach and the Sabre approach. For mini and small benchmarks, the Zulehner approach does not seem to perform as well as the Sabre approach. It can be seen from the fact that the relative speedup of SlackQ over Zulehner is usually larger than SlackQ over Sabre. However, the Sabre approach performs worse than the Zulehner approach for medium and large benchmarks. It can be seen that Zulehner and Sabre perform well in different scenarios when compared against each other. Regardless, our approach SlackQ outperforms both of them.

VI. CONCLUSION

The physical layout of contemporary quantum devices imposes limitations for mapping a high level quantum program to the hardware. It is critical to develop an efficient qubit mapper in the NISQ era. Existing studies aim to reduce the gate count but are oblivious to the depth of the transformed circuit. This paper presents the design of the first time-efficient slack-aware swap insertion scheme. Experiment results show that our proposed solution generates hardware-compliant circuits with faster execution time compared with state-of-the-art mapping schemes.

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