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3D integration and measurement of a semiconductor double quantum dot with a high-impedance TiN resonator

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One major challenge to scaling quantum dot qubits is the dense wiring requirements, making it difficult to envision fabricating large 2D arrays of nearest-neighbor-coupled qubits necessary for error correction. We describe a method to ameliorate this issue by spacing out the qubits using superconducting resonators facilitated by 3D integration. To prove the viability of this approach, we use integration to couple an off-chip high-impedance TiN resonator to a double quantum dot in a Si/SiGe heterostructure. Using the resonator as a dispersive gate sensor, we tune the device down to the single electron regime with an SNR = 5.36. Characterizing the individual systems shows 3D integration can be done while maintaining low-charge noise for the quantum dots and high-quality factors for the superconducting resonator (single photon Qo = 2.14 × 10^4 with Qo = 3 × 10^5), necessary for readout and high-fidelity two-qubit gates.

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INTRODUCTION

One major challenge for noisy intermediate-scale quantum (NISQ)-era superconductor and semiconductor qubit systems lies in the wiring interconnect problem1. Unlike classical processors, where of order 10^3 signal lines operate 10^9 transistors, all solid state qubit platforms require at least one independent control line per qubit. In cryogenic solid state platforms, Josephson effect qubits, such as the transmon, capacitively shunted flux, or fluxonium qubit, have a modest overhead of 1–3 lines per qubit for control and readout3–6. Semiconductor spin qubits in accumulation-mode gate-defined quantum dots require between 9 and 13 bias lines per qubit to form the necessary electrostatic environment, with anywhere from 1 to 5 of those lines requiring ≥1 GHz bandwidth to perform high-fidelity qubit control7–12. In order to implement the surface code for quantum error correction, a 2D grid of N × N nearest-neighbor coupled qubits is minimally necessary13. For semiconductor qubits, this requirement is of great practical concern, as the need for dense networks of sub-100 nm sized electrodes to form a large array of coupled spins is major interconnect engineering challenge with current proposals requiring several technical innovations before becoming feasible14.

Fortunately, circuit quantum electrodynamics (cQED) provides a framework where the extreme wiring density requirements for quantum dot spin qubits may be alleviated by using superconducting resonators to mediate long range 2-qubit interactions, providing room for the necessary wiring to form the individual qubit structures. This scheme requires strong qubit-cavity coupling (g ≫ κ, γ) to be viable past the structural engineering to fabricate the devices; here, g is the electron–photon coupling strength, κ is the qubit dephasing rate, and γ is the cavity photon loss rate. Recent work has shown hybrid cQED architectures can reach the strong coupling to the charge, valley-orbit, and spin degrees of freedom as well as facilitate interactions between spin or superconducting qubits, with most demonstrations relying on high-impedance resonators to increase the coupling strength (g ∝ 1/2). Using cavity mediated two-qubit gates reduces the array problem to fabricating N × N copies of single qubit structures (linear dot arrays), which is routine in the lab.

Vertical integration further ameliorates the interconnect problem by allowing some large components to be placed vertically off-chip in a 3D architecture. This approach uses thermomechanical bonding to create electrical contacts between two or more dies using indium22,23. Currently, 3D integrated circuits are the workhorse interconnect solution for high-qubit count superconducting quantum processors, facilitating demonstrations of quantum supremacy and large quantum volumes in solid state quantum processors24,25. In this paper, we demonstrate the viability of 3D integration for spin qubits using a Si/SiGe double quantum dot (DQD) and a vertically integrated high-Q, high-impedance TiN resonator used for dispersive gate charge sensing without degradation in performance of either component.

RESULTS AND DISCUSSION

Design of a 2D array of semiconductor qubits using 3D integration

In Fig. 1a we illustrate a 3-tier stack integration scheme that is conceivable using state of the art 3D integration22,26,27. The base die, a superconducting multichip module (SMMC), serves as a routing layer for high density control wiring, possibly incorporating control and readout circuitry such as cryogenic CMOS, superconducting amplifiers or photodetectors28–30. Superconducting through-silicon vias (TSVs) bring qubit control lines to the the qubit die to the SMMC using indium bump bonds to create electrical contact27. In our design, low-Q readout resonators are integrated onto the qubit chip as they are more tolerant to higher internal losses resulting from multilayer processing necessary to form the spin qubit structures. Readout is done via a mutual inductance to a nearby shorted signal line with the resonator probed in reflection. The top die consists of a network of high impedance, low loss resonators used for cavity mediated two-qubit interactions between distant quantum dot qubits.
Device design

For our experiment, we limit the architecture to the 2-tier stack consisting of two qubits, four coupling bus resonators with voltage bias taps (IV, gray die), and two readout resonators (II, red die) fitting in a 0.16 mm² top down area across two die. Thirteen TSVs (hatched purple, in Fig. 1b) route bias lines for each triple quantum dot vertically into each unit cell. Figure 1c provides a simplified circuit schematic of the unit cell with the elements on the qubit die colored in red and the elements on the coupler die colored in gray. Using this design Fig. 1d shows how a 64 qubit processor can be tiled out in a 4.6 x 1.6 mm² footprint. This design builds upon demonstrated technology and assumes nominal materials parameters that are possible for high-kinetic inductance films (e.g., quantum dot gate design, TSV or Indium bump lithographic dimensions, sheet kinetic inductance, etc.)\[^{22,27,31}\]. We emphasize here this design requires fabrication process development to ensure thermal budget compatibility between the TSV process and the quantum dot fabrication.

Figure 1b shows the CAD design of a lattice unit cell consisting of two qubits, four coupling bus resonators with voltage bias taps (IV, gray die), and two readout resonators (II, red die) fitting in a 0.16 mm² top down area across two die. Thirteen TSVs (hatched purple, in Fig. 1b) route bias lines for each triple quantum dot vertically into each unit cell. Figure 1c provides a simplified circuit schematic of the unit cell with the elements on the qubit die colored in red and the elements on the coupler die colored in gray. Using this design Fig. 1d shows how a 64 qubit processor can be tiled out in a 4.6 x 1.6 mm² footprint. This design builds upon demonstrated technology and assumes nominal materials parameters that are possible for high-kinetic inductance films (e.g., quantum dot gate design, TSV or Indium bump lithographic dimensions, sheet kinetic inductance, etc.)\[^{22,27,31}\]. We emphasize here this design requires fabrication process development to ensure thermal budget compatibility between the TSV process and the quantum dot fabrication.

In order to maximize the probability of reaching strong coupling, we push the resonator into the high-impedance regime using a 50 nm-thick TiN film with a 500 nm wide center pin, and 10.25 μm gap, as shown in Fig. 2b. Using COMOSL Multiphysics to simulate the 3D structure’s influence on the CPW line capacitance and the nominal kinetic inductance of the TiN film (L_k = 9pH/□) we estimate a characteristic impedance of Z_0 = 575Ω with target fundamental frequency of 4 GHz. The high impedance is expected to increase the charge-photon coupling rate by a factor of 3.4 over 50Ω resonators. Higher impedance can be engineered by reducing the TiN center pin thickness and width (L_k ≈ 1/μm) but was not pursued for this study\[^{32}\]. We find the estimates of the inductance and capacitance of the TiN resonator are in good agreement with the experimentally measured range of resonance frequencies 3.985–4.115 GHz from several different samples with nominally identical resonator dimensions.

Galvanic contact between both dies is facilitated by underbump metal pads made from Ti/Pt/Au on the resonator die and Ti/Pd/Ti/Pt/Au on the quantum dot die, which do not form native oxides and can be seen in the optical images in Fig. 1b. To avoid unwanted damping caused by power dissipation of the microwave currents in the resonator to the normal metal pads, they are placed at voltage antinodes and at the end of the quarter wave DC tap where nominally no microwave currents exist for the λ/2 mode, thus preserving the high internal quality factor \[^{32,37}\].

For these data a single layer of aluminum gates are used to form the double quantum dot\[^{18,38}\]. Underneath the gate stack is an ultra thin (~1.7 nm thick) SiO2 layer grown by nitric acid oxidation of silicon (NAOS), which has been shown to be higher quality than similar thickness thermal oxides\[^{39}\]. A scanning electron micrograph with an overlaid Thomas-Fermi simulation of the induced electron gas can be seen in Fig. 3a. The two dimensional electron gas (2DEG) is induced in an 8.6 nm-thick silicon quantum well made from 800 ppm \[^{28}\]Si ~42 nm below the surface. As designed, the gates labeled (P1,P2) are intended for accumulating a double quantum dot and the gates labeled (B1:B2:B3) serve to tune the various tunnel barriers. The other gates labeled (S1:S2:S3:S4) help corral the charges to upper portion of the plunger gates and mitigate unwanted transport currents. The superconducting resonator has a galvanic connection to the gate S1 as a single-layer variant of a split-gate coupler design, which serves to decouple the cavity pin voltage from the neighboring magnetic field, and high internal Q allowing for Z_0 > 1kΩ while maintaining Q_0 > 10^5\[^{33,35,36}\].
quantum dot easing tuning constraints for two-qubit samples. Tuning the device as intended, a double quantum dot (DQD) can be formed and sensed under P1 and P2 using the TiN resonator as shown in Fig. 3c. In the many electron regime the DQD has tunnel rates comparable to the resonator frequency resulting in a visible interdot transition shown in the inset of Fig. 3c.

A third dot can be formed under B2 by repurposing P1 and P2 as barrier gates. For each dot, we use bias spectroscopy to extract the lever arm of the nominal chemical potential gate and find typical lever arms ranging between $\alpha = 0.20-0.25$ eV/V (an example can be seen in supplementary Fig. 3a). In general, we observe good electrical confinement for each dot with charging energies ranging from $E_C = 3-5$ meV (3 meV for the B2 dot and 5 meV for the P1/P2 dots) with orbital slitting $E_{ORB} \approx 1$ meV in the few to single electron regime. Additional parasitic quantum dots were observed under certain bias conditions, likely due to uncontrolled accumulation of 2DEG under the gate electrodes and are a source of low frequency instabilities in the device. These instabilities prevented tunnel coupling at frequencies comparable to the resonator frequency in the single electron regime.

**Quantum dot charge noise characterization**

We next measure the charge noise spectrum the dots experience in order to estimate the charge dephasing rate and evaluate the prospect for strong coupling between the charge and photon degrees of freedom with this design. To do this we use two methods: Coulomb blockade peak tracking and voltage-to-current transduction. Using both methods allows for noise to be characterized over 7 orders of magnitude from $10^{-2}$ to $10^2$ Hz. The first method is performed by repeatedly sweeping the plunger gate voltage (see supplementary material for details) of the dot over the course of a day to monitor its location with a repetition rate of ~0.1 Hz. The data are then fit to a thermally broadened conductance peak defined by

$$I(V_g) = I_{\text{offset}} + \frac{A_0}{4k_BT_e} \cosh\left(\frac{\alpha(V_g - V_{\text{offset}})}{2k_BT_e}\right)^{-2}. \quad (1)$$

From the fits we extract an electron temperature of $T_e \approx 200$ mK (upper bound), peak current $\frac{A_0}{q}$, where $A_0$ is a fitting factor that depends on the biasing of the dot ($A_0 = V_{SD} 4k_BT_e G_{\text{max}} = e^2 V_{SD} (\Gamma r (|r|))$, and the peak offset voltage ($V_{\text{offset}}$). Using the extracted offset voltage for each scan, we generate a corresponding time series from which the power spectral density of the offset voltage can be computed as shown by the black (raw) and red (smoothed) traces in Fig. 3d. We observe a $1/f^\beta$ power law dependence in the offset voltage at frequencies below 1 mHz similar to that observed in stadium style devices, characteristic of Brownian motion in the fluctuating variables. One potential mechanism for the observed spectrum is a very small hysteresis in the peak’s location due to the raster-style sweep causing it to systematically increase (or decrease) in gate voltage. The noise floor of the measurement is due to the perfect zero lag auto-correlation of the time series used to compute the power spectrum. This feature generates a large white noise spectrum (the FFT of a delta-like peak at zero lag) and dominates the high frequency part of the spectrum.

To resolve offset voltage noise below the noise floor of the peak tracking method, we use a second method where we measure fluctuations in the transport current at the point of maximum voltage-to-current transduction and compute the associated current noise power spectrum. Assuming a linear transfer function between voltage and current we can convert the current noise power spectrum to a gate referred voltage power spectrum by computing

$$S_V(f) = \left| \frac{dI}{dV_g} \right|^{-2} S_I(f), \quad (2)$$

where $S_V$ is the power spectral densities of the voltage (current) and $\frac{dI}{dV_g}$ is the derivative of the blockade peak where the gate voltage was set for the data acquisition. Using this method we are able to extract the offset voltage noise spectrum between $2 \times 10^{-3}$ to 100 Hz as shown by the teal trace in Fig. 3b. A moving average filter is used to reduce statistical fluctuations in the data without distorting the overall shape of the signal.

The same data can be subdivided into 10 s traces where each trace’s power spectrum can be averaged producing the dark green spectrum from 0.1 to 10 Hz in Fig. 3b, in agreement with the smoothed data from the single time series. In most spectra from this device we observe a prominent Lorentzian spectrum at high frequencies with a characteristic switching time between 1 and 10 Hz. The spectra measured have an amplitude at $f = 1$ Hz of...
S(f) = 10–36 μV²/Hz comparable with other work. Alternatively, one can cast in terms of chemical potential fluctuations: $S_\mu(f) = a^2 S_e(f) = 0.6–1.5 \mu$V²/Hz, or in terms of offset charge $S_C(f) = \langle e/E C \rangle^2 S_e(f) = 2.4–6 \times 10^{-2} \text{me}^2/\text{Hz}$. These values corroborate recent work that suggests reducing the volume of deposited dielectrics above the quantum dots reduces charge noise. The variation in measured values is somewhat dependent on the tuning of the device, with the lowest numbers corresponding to small source-drain bias $V_{SD} \leq 50 \mu$V (while maintaining $|\frac{d}{dV_{SD}}| > 100 \text{pA/mV}$) and the amplitude of the low frequency switcher. The two methods measured noise amplitudes and exponents that are similar where they cross over around $1–10$ mHz, demonstrating they are complementary techniques to measuring noise in the quantum dot. Elimination of unwanted nearby 2DEGs through use of screening gates could improve the low frequency instability and minimize parasitic switchers coupled to the intended dots. Using measured spectrum, we estimate the charge dephasing rate for an ideal charge qubit at zero detuning with tunnel coupling $2t = h\nu$, as:

$$\frac{\gamma}{2\pi} \approx \left. \frac{d^2 E_{01}}{d^2} \right|_{\nu=0} S_\mu(1 \text{Hz}) \approx \frac{S_e(1 \text{Hz})}{2t} \approx 9 – 22 \text{MHz}.$$  

This suggests for a device where the dots are placed optimally relative to the cavity electrode, strong coupling to the charge degree of freedom should be possible.

**Characterization of the dispersive gate readout**

To evaluate the resonator as a dispersive gate readout, we measure the signal-to-noise ratio (SNR) for observing tunneling resonances where the electron has high susceptibility to the cavity photon’s electric field. We first tune a dot-lead transition to maximize the phase shift in the microwave tone at a fixed power of $\sim 95 \text{dBm}$ on chip. Next, we take $10^4$ measurements of the demodulated IQ voltages when the electron is biased in Coulomb blockade or tunneling resonance with a 50 ms integration time sampled at 100 kSa/s. We then define the measurement axis along the centroids of the raw demodulated IQ blobs and define zero to be the midpoint between the blobs analogous to how one might threshold for singlet-triplet blockade readout. As shown in Fig. 3d, by taking a histogram of the data along the Q quadrature we find the blockade peak voltage is well described by a Gaussian process (solid lines are fits), while the tunneling peak undergoes an additional non-Gaussian process evidenced by the asymmetry of the peak and substantial deviation from the fit. This is possibly due to the low frequency switcher observed in the transport noise data causing the location of the peak to telegraph in voltage space. Curiously, the non-Gaussian shoulder is not present at lower drive powers, suggesting the process is stimulated from the microwave energy in the resonator (see supplemental Fig. 4 for more details).

Defining SNR in terms of the separation of the demodulated peaks ($\Delta$) and the blockade peak standard deviation ($\sigma_b$), we find $\text{SNR} = \Delta/\sigma_b = 5.36$, which compares favorably to PCB integrated reflectometry methods while using somewhat lower powers. We note using $\sigma_b$ instead of $\sigma_e$ inflates the SNR by roughly 20%, as we empirically find the tunneling peak standard deviation ($\sigma_t$) is larger. Compared to other resonator measurement techniques, which define SNR as the power SNR ($\text{SNR}_p = (\Delta/\sigma_p)^2$) we are notably much lower with $\text{SNR}_p > 28.7$ compared to $\text{SNR}_p > 1000$ for similar integration times. The likely reason for the large difference is due to the substantially weaker coupling strength between the resonator and the quantum dots in our system. Based on S1 vs. P1(2) measurements, the lever arm of the resonator gate to the quantum dots is quite small ($\approx 0.05 \sigma_{P1(2)}$).
causing the corresponding difference in the IQ signal during tunneling events to be substantially smaller than plunger coupled devices.

Attempts to tune the coupling strength by tuning the resonator gate voltage are hampered by reductions in the loaded $Q_i$, as discussed later in the text. We emphasize this issue is not intrinsic to the 3D architecture but rather a bug of the single-layer gate layout resulting in poor placement of the quantum dots relative to the cavity electrode. This unfortunately prevents direct measurement of the charge-photon coupling rate as we need $10^4$ photons in the resonator to resolve the electron tunneling resonances. Typical direct coupling measurements require single photon probe powers to minimize driving effects on the qubit. Use of an overlapping gate architecture, which has more precise placement of the quantum dots, will substantially improve this aspect of the device performance. Additional optimizations such as using heterodyne detection with fast sampling DACs or quantum limited superconducting amplifiers can also improve the SNR through noise mitigation.

**Fig. 4** TiN resonator characterization. a Measurement of the resonator fundamental transmission spectra as a function of gate voltage. Inset: extracted Lorentzian fits to the teal and pink traces at $V_{S1} = 0$ mV and $V_{S1} = 300$ mV, respectively. b Extracted loaded quality factor as a function of gate voltage showing an anomalous decrease in the loaded quality factor upon voltage biasing the center pin. A narrow plateau in $Q_i$ occurs between $V_{S1} = \pm 2$ mV where the additional loss is less than the coupling quality factor. c Power dependence of the loaded quality factor at 0 mV and 300 mV center pin bias. We extract a single photon internal quality factor of $Q_i > 3 \times 10^5$ consistent with radiative losses from the large CPW geometry. We estimate degradation of the internal quality factor to $Q_i = 3 \times 10^4$ at $V_{S1} = 300$ mV. Error bars are the 95% confidence intervals of the fit extracted $Q_i$. d Phase noise power spectral density of the resonator with $V_{S1} = 0$ mV by probing the cavity on resonance with the dots empty. We extract a $1/f^6$ with $\beta = 1.98$ noise spectrum in the phase noise for frequencies below 0.1 Hz. e Upper: Resonator frequency shift ($\delta f_t = f_t(V_{S1} = 0) - f_t(V_{S1})$) as a function of voltage bias on the cavity pin. We observe a nonmonotonic modulation in the center frequency. Lower: Zoom-in of a bias region in which multiple TLS-cavity interactions are observed. f Spectral motion of two TLS interacting with the TiN resonator over several hours.

Performing a similar scan over a range $V_{S1} = \pm 400$ mV, we observe a dramatic change in the loaded quality factor with the magnitude of the applied electric field ($\propto |V_{S1}|$), as shown in Fig. 4b. The origin of the anomalous loss mechanism upon voltage biasing the resonator is unclear but likely cannot be attributed to the induced 2DEGs in under the accumulation gates LA or RA, as degradation occurs regardless of the sign of the bias. To extract the internal $Q_i$, we perform power sweeps at two voltage biases, shown in Fig. 4c. Assuming the high power limit at zero voltage bias is defined by the explicit coupling capacitances for probe and readout, we extract $Q_i = 2.31 \times 10^4$ with $Q_i(V_{S1} = 0\text{mV}) = 3 \times 10^5$ and $Q_i(V_{S1} = 300 \text{mV}) = 3 \times 10^4$. To our knowledge, the extracted $Q_i$ at zero voltage bias is the highest measured $Q_i$ in a superconducting-semiconductor hybrid system.

It has recently been proposed that high-impedance resonators may exhibit lowered quality factors due to enhanced phase noise rather than true energy loss, due to fluctuations in the kinetic inductance from charge noise resulting in a corresponding frequency modulation. To see if this was present, we measured the phase noise at low frequencies by probing the transmission phase on resonance (at time $t = 0$) over the course of several hours. We compute the corresponding phase noise power spectral density, as shown in Fig. 4d. We observe a $1/f^6$ dependence of the phase noise PSD below 0.1 Hz, atypical of high $Q$ superconducting resonators. Additionally, when performing the voltage bias studies, we observed the cavity resonance frequency is a nonmonotonic function of the applied voltage bias to the center pin with maximum frequency modulation of 14 kHz, as shown in Fig. 4e. Several reproducible TLS-cavity crossings, inferred by shifts of the resonator frequency, are observed over the ±400 mV tuning range explored. These data suggest the effect is present, but due to their small magnitude (≈3–5 kHz) are insufficient to explain the factor of ~10 reduction in $Q_i$ with application of voltage bias.
We observe these TLS are not fixed in location in voltage space and undergo time dependent spectral diffusion over hours-long timescales, illustrated by the data in Fig. 4f. At this time it is unclear if these defects originate from the quantum dot die or the TiN resonator die or if any of the noise between the two systems is correlated.

In summary, we have described a 3D integration approach to hybrid superconductor- semiconductor quantum processor. We demonstrated such an integration scheme is viable as our system had nearly all necessary ingredients for long range coupling: high single photon quality factor cavities with high-impedance resonators and low- charge noise quantum dots. The remaining ingredient, strong charge-photon coupling may be achieved by using a gate stack that more precisely places the quantum dots relative to the cavity electrode, such as the linear overlapping gate array. Using impedance engineering, single photon loaded quality factors as high as $2.14 \times 10^6$ were measured with an estimated $Q \approx 3 \times 10^5$ placing a photon loss rate bound of $k/2\pi = f/Q \approx 15$ kHz at 4 GHz, which can be easily utilized by lowering the coupling capacitance to probe the resonator (or eliminating it entirely). While the noise data acquired suggests dephasing rates below 30 MHz are possible, potentially sufficient entirely. The signal is amplified by cryogenic and room temperature amplifiers, filtered, and then demodulated by a Marki O416 IQ mixer. The demodulated DC voltages are filtered and sent to a pair of SRS60 voltage preamplifiers at unity gain with a 100 kHz two pole low-pass filter and are then sampled by an NI-DAQ 6216 at 100 Ksa/s with 5 Ksa per point for the data shown resulting in an SNR $\approx 5.36$.

DATAvABILITY

The datasets generated during and/or analysed during the current study are available from the corresponding author on reasonable request.

CODE AVAILABILITY

All data analysis code and COMSOL simulation are available from the corresponding author on reasonable request.

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**AUTHOR CONTRIBUTIONS**

N.H., D.R., D.Y., J.L.Y., W.D.O., R.M. and M.A.E. designed and planned the experiment. N.H. fabricated the quantum dot chip and performed the measurements. D.R., D.Y., J.L., and R.D. developed and fabricated the TiN resonators and the multichip bonding process. R.D. performed the indium bump bonding between the resonator and qubit chips. N.H., R.M. and M.A.E. wrote the manuscript with input from all the other authors.

**COMPETING INTERESTS**

The authors declare no competing interests.

**ADDITIONAL INFORMATION**

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