A novel gate driver for Si/SiC hybrid switch for multi-objective optimization

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Abstract
A novel gate driver with simple functional and structural integration is proposed here, which splits the input gate signal and outputs two separate signals with a dedicated delay time to drive the two constitutional switches, aiming at the cost-effectiveness and power loss reduction of the Si/SiC hybrid switch. The dependency of the hybrid switch’s thermal and efficiency performance on the parameters of the gate driver are theoretically and experimentally investigated in a 9 kW 20 kHz Si/SiC hybrid switch based boost converter. A novel load current dependent gate control strategy is proposed to be implemented in the proposed gate driver to achieve the high conversion efficiency under light to medium load condition and balanced junction temperature between the two internal devices under heavy load conditions. The experimental results based on a 20 kHz boost converter show that the Si/SiC hybrid switch with the novel gate driver and optimal current dependent control strategy offers a 163% and 10% rise in power handling capability, respectively, compared to that using the all-IGBT device and all-SiC MOSFET device, and yet a considerably lower device cost.

1 | INTRODUCTION

In recent years, the SiC power MOSFETs have become the focus of the medium-voltage device innovation to displace silicon IGBTs because it has lower conduction resistance, faster-switching speed, and higher switching frequency capability [1–5]. Commercially available SiC MOSFET (referred as SiC_MOS) with various voltage ratings (650–1700 V) from several major manufacturers have been continuously penetrating and taking over the realm of Si IGBTs, chasing after the power converter system’s compactness and efficiency [6].

Yet despite the promising performance advancement, with a cost-oriented viewpoint, the cost A < sp > -1 < /sp > ($ A < sp > -1 < /sp >) performance poses an obstacle for SiC_MOS primarily due to the costly SiC material and suboptimal fabrication process [7–8]. A cost-effective HyS comprising a primary large current Si IGBT and a small current auxiliary SiC_MOS is proposed, which achieves the cost-performance trade-off in applications [9–12].

A comprehensive cost analysis was performed in [13] to demonstrate the cost viability of the Si/SiC HyS relative to the SiC_MOS. The current sharing behaviour within the HyS was analysed via simulation in [14, 15]. It shows lower switching losses and suppressed oscillations compared to the all-Si IGBT and all-SiC_MOS package layouts, respectively. In [16–19], the specific gate control patterns are investigated and analysed for the HyS to reduce the switching losses and improve the conversion efficiency of the HyS based converter. In [20, 21], a current dependent gate control pattern was reported in voltage source inverter applications to improve the overload capability of the cost-effective HyS.

Although these preliminary studies on the HyS have illustrated their cost superiority, efficiency improvement, and overload capability, some key issues related to the gate control are yet to be solved. First, in some specially designed PWM controller IC applications, the highly integrated design and fixed PWM output channels can’t achieve the flexible gate drive patterns of the HyS conveniently. The reported studies on Si/SiC
HyS demand two discrete gate drivers to ensure a dedicated gate sequence control with the auxiliary digital control unit, such as FPGA, CPLD, or DSP in the double pulse test circuit or converter applications. However, these solutions compromise the cost-effectiveness of the Si/SiC HyS, and increase the complexity of the HyS based power electronics systems. Therefore, a low-cost gate driver solution is needed for the Si/SiC HyS to achieve the benefit of its cost-effectiveness in practical power conversion applications.

Second, a dominating objective using the above-mentioned gate sequence control is to achieve power loss reduction for the Si/SiC HyS, with insufficient consideration of the safe operation below the thermal limit of its constructive switches. To reduce the switching losses of the HyS, agile sequence control was recommended to achieve the zero voltage switching (ZVS) condition of the main IGBT [13, 16–21], where the auxiliary SiC_MOS was turned on prior and turned off shortly after the main IGBT. However, the auxiliary SiC_MOS conducts the full-forward current during these short intervals and undertakes the hard turn-on and turn-off switching operation, which results in the large power loss of the SiC_MOS under the heavy load conditions. The large power loss of the SiC_MOS may result in its junction temperature ($T_{J}$) much higher than that of the main IGBT because of its small chip size and large thermal resistance, which put the auxiliary SiC_MOS at risk of over temperature under heavy load conditions. The overheating may induce reliability degradation or thermal breakdown of the SiC_MOS inside the cost-effective Si/SiC HyS if solely relying on this gate control strategy [22–26]. In [27], it adopted the appropriate fixed gate control delay time of the HyS to achieve the sole optimal control objects such as the minimum power loss or balanced $T_{J}$ of the HyS at a specific load condition. However, the gate control objective and corresponding optimal gate delay time need to vary with the load conditions in some load-variable power converter applications, such as PV and wind power. Different objectives of gate delay time control are preferred under different load conditions of load-variable power converters. For example, the power loss minimization of the Si/SiC HyS is preferred under the light or medium load conditions because the $T_{J}$ of its two internal devices are within their safe operating areas. And the thermal performance optimization between its two internal devices is preferred to avoiding the over-temperature risk of its internal devices under heavy load conditions. Therefore, multiple objective optimizations between the efficiency improvement and thermal safety operation of the Si/SiC HyS based power converter operation over a wide output power range needs to be considered in the gate control profile optimization of the Si/SiC HyS.

To solve these problems, a novel gate driver dedicated to the Si/SiC HyS is proposed, which accounts for the cost-effectiveness and multiple performance optimization objectives. The load current dependent optimal gate profile control is introduced and implemented using the proposed HyS driver to reduce the power loss of the HyS at light to medium load currents and to keep the two inner devices’ $T_{J}$ balance at heavy load current. The operation principle and characteristics of the novel HyS gate driver is introduced and analysed in Section 2. Section 3 introduces the load current dependent optimal control strategy, which is justified using both theoretical and experimental methods employed in this paper. Section 4 concludes the paper.

2 OPERATION PRINCIPLE AND DESIGN OF THE NOVEL HY S GATE DRIVER

The objective of this section is to propose a novel gate driver structure for the Si/SiC HyS specific control patterns and analyse its operation principle. Figure 1 shows the schematic of the HyS. The HyS’s paralleling structure integrates the conduction advantages of the SiC_MOS and the Si IGBT because the SiC_MOS conducts most forward current at small load current condition and the Si IGBT conducts most forward current at large load current condition.

Using the appropriate gate control patterns as shown in Figure 2, the IGBT could achieve the ZVS turning off to reduce the large turn-off switching loss caused by its tail current. Four basic control patterns between the two internal devices of the HyS enable the auxiliary SiC_MOS’s ZVS operation or the main IGBT’s ZVS operation during the turn-on and turn-off process.

During the switching on transient, the IGBT achieves the ZVS turning on and the SiC_MOS undertakes the hard turning on and turn-off operation when using the pattern I and pattern II. When using the pattern III and pattern IV, the IGBT undertakes the hard turning on while the SiC_MOS achieves the ZVS turning on operation. The turn-off operation of the HyS is similar to the turn-on operation.
In this work, a novel gate driver solution as shown in Figure 3 is proposed for the HyS to realize the specific gate control patterns (\( T_{\text{on, delay}} \) and \( T_{\text{off, delay}} \)) and achieve its cost-effectiveness and performance improvement. It utilizes a few components to achieve the mutually independent \( T_{\text{on, delay}} \) and \( T_{\text{off, delay}} \) for its specific drive patterns.

The proposed gate driver consists of the IGBT drive branch, SiC_MOS drive branch, protection union and two totem-pole drives. The two totem-pole drives are used to directly source and sink the high peak current of the IGBT and SiC_MOS during the switching on and switching off transients. The protection unit is used to block the PWM signals and keep the output be driven low when the short-circuit situation or other faults condition occurs. The SiC_MOS branch and the IGBT branch are used to split the single input signal into two separate output signals with independent adjustable \( T_{\text{on, delay}} \) and \( T_{\text{off, delay}} \), which enable the particular gate drive patterns as shown in Figure 2.

### 2.1 Turning on process of the gate driver

Figure 4 shows the turning on process of the HyS’s novel gate driver.

When the output of the \( U_{\text{opt}} \) (optical coupler) is high level, the capacitor \( C_1 \) is charged in the SiC_MOS driver branch. The charging current can be expressed as,

\[
C_1 \frac{dV_{C_1}}{dt} = \frac{V_{CC} - V_{C_1}}{R_4 + R_2 + R_{D1}}
\]

(1)

where \( V_{CC} \) is the positive source voltage, \( V_{C_1} \) is the voltage of the capacitor \( C_1 \), \( R_{D1} \) is the equivalent resistance of \( D_1 \). Because \( R_{D1} \) is very small compared with the \( R_4 \) and \( R_2 \), \( R_{D1} \) can be ignored in Equation (1). The initial voltage of capacitor \( C_1 \) is \( -V_{EE} \). When \( V_{C_1} \) is higher than the reference voltage \( V_{ref1} \), the comparator \( U_1 \) outputs high level, which means the SiC_MOS is turned on. The time of the \( V_{C_1} \) reaches the reference voltage \( V_{ref1} \) is derived as,

\[
t_{\text{on1}} = -(R_4 + R_2) C_1 \ln \left( \frac{V_{CC} - V_{ref1}}{V_{CC} + V_{EE}} \right)
\]

(2)

In the IGBT branch, similar to the SiC_MOS branch, the current flowing through \( R_4 \) and \( R_3 \) to charge the capacitor \( C_2 \) is given as,

\[
C_2 \frac{dV_{C_2}}{dt} = \frac{V_{CC} - V_{C_2}}{R_4 + R_3}
\]

(3)

The initial voltage of capacitor \( C_2 \) is \( -V_{EE} \) too. When \( V_{C_2} \) is larger than \( V_{ref2} \), the comparator \( U_2 \) outputs a high voltage, which means the IGBT is turned on. The time of the \( V_{C_2} \) reaching the reference voltage \( V_{ref2} \) is derived as,

\[
t_{\text{on2}} = -(R_4 + R_3) C_2 \ln \left( \frac{V_{CC} - V_{ref2}}{V_{CC} + V_{EE}} \right)
\]

(4)

\( T_{\text{on, delay}} \) is the time interval between \( t_{\text{on2}} \) and \( t_{\text{on1}} \). It is derived as,

\[
T_{\text{on, delay}} = (R_4 + R_3) C_1 \ln \left( \frac{V_{CC} - V_{ref1}}{V_{CC} + V_{EE}} \right)
\]

\[= (R_4 + R_3) C_2 \ln \left( \frac{V_{CC} - V_{ref2}}{V_{CC} + V_{EE}} \right)
\]

(5)

when \( V_{ref} \) is equal to \( V_{ref2} \), and \( C_1 \) is equal to \( C_2 \), Equation (5) can be simplified as,

\[
T_{\text{on, delay}} = (R_2 - R_3) C_1 \ln \left( \frac{V_{CC} - V_{ref1}}{V_{CC} + V_{EE}} \right)
\]

(6)

Equation (6) means that the value of \( R_3 \) can determine the length and polarity of the \( T_{\text{on, delay}} \) between the two internal devices. When \( R_3 \geq R_2 \), the \( T_{\text{on, delay}} \) is zero or positive, which means the turn-on of the SiC_MOS is equal to or before the IGBT. When \( R_3 < R_2 \), the \( T_{\text{on, delay}} \) is negative, which means the turn-on of the SiC_MOS is after to the IGBT. The length of the \( T_{\text{on, delay}} \) is in proportion to the absolute value of the difference between the \( R_2 \) and \( R_3 \).
2.2 Turning off process of the gate driver

To reduce the IGBT’s large turn-off switching loss caused by the tail current, the ZVS turning off of the IGBT is recommended for the Si/SiC HyS. As shown in Figure 2, the pattern I and pattern III are preferred. Therefore, the $T_{\text{off\_delay}}$ between the two internal devices should be always positive when it is implemented on the novel gate driver. Figure 5 shows the turn-off process of the novel gate driver.

When the output of the $U_{\text{opt}}$ (optical coupler) is low level, the capacitor $C_1$ is discharged in the SiC_MOS driver branch. The discharging current can be expressed as,

$$\frac{-V_{EE} - V_{C1}}{R_1} = C_1 \frac{dV_{C1}}{dt}$$

(7)

The initial voltage of the capacitor $C_1$ is $V_{CC}$. When $V_{C1}$ is lower than the $V_{\text{ref1}}$, the comparator $U_1$ outputs a low voltage, which means the SiC_MOS is turned off. The time of the $V_{C1}$ reaching the reference voltage $V_{\text{ref1}}$ is derived as,

$$t_{\text{off1}} = -R_1 C_1 \ln \left( \frac{V_{\text{ref1}} + V_{EE}}{V_{CC} + V_{EE}} \right)$$

(8)

In the IGBT branch, the discharge current of $C_2$ can be derived as,

$$C_2 \frac{dV_{C2}}{dt} = \frac{-V_{C2} - V_{EE}}{R_{D2}}$$

(9)

The initial voltage of the capacitor $C_2$ is $V_{CC}$. When $V_{C2}$ is smaller than the reference voltage $V_{\text{ref2}}$, the comparator $U_2$ outputs a low voltage, which means the IGBT is turned off. The time of the $V_{C2}$ reaching the reference voltage $V_{\text{ref2}}$ is derived as,

$$t_{\text{off2}} = -R_{D2} C_2 \ln \left( \frac{V_{EE} + V_{\text{ref2}}}{V_{CC} + V_{EE}} \right)$$

(10)

$T_{\text{on\_delay}}$ is the time interval between $t_{\text{off1}}$ and $t_{\text{off2}}$. Because the value of $R_{D2}$ is very small compared to the $R_1$, $t_{\text{off2}}$ is close to zero. Therefore, $T_{\text{off\_delay}}$ is mainly determined by $t_{\text{off1}}$.

$$T_{\text{off\_delay}} \approx t_{\text{off1}} = -R_1 C_1 \ln \left( \frac{V_{\text{ref1}} + V_{EE}}{V_{CC} + V_{EE}} \right)$$

(11)

Equation (11) shows that the length of the $T_{\text{off\_delay}}$ is in proportion to the value of $R_1$.

The resistor $R_1$ and $R_3$ are implemented using two adjustable resistors to change the $T_{\text{off\_delay}}$ and $T_{\text{on\_delay}}$, respectively. The other parameters of the gate driver prototype for the HyS are shown in Table 1.

Table 1: Parameters of the gate driver circuit

| Parameters | Values |
|------------|--------|
| $+V_{CC}$  | +5 V   |
| $-V_{EE}$  | -5 V   |
| $V_{\text{ref1}}$ | 1 V   |
| $V_{\text{ref2}}$ | 1 V   |
| $R_2$      | 15 Ω   |
| $R_3$      | 1 kΩ   |
| $C_1$      | 22 nF  |
| $C_2$      | 22 nF  |

Figures 6 and 7 show the measured $T_{\text{on\_delay}}$ and $T_{\text{off\_delay}}$ between the two internal devices at various $R_3$ and $R_1$, respectively.

When $R_3 < 15 \ \Omega$, the polarity of the $T_{\text{on\_delay}}$ is negative, which means the IGBT is turned on before the SiC_MOS. When $R_3 \geq 15 \ \Omega$, the polarity of the $T_{\text{on\_delay}}$ is zero or positive, which means the SiC_MOS is turned on equal or before the IGBT. The measured results are consistent with Equation (6). When the value of $R_1$ changes, the polarity of the $T_{\text{off\_delay}}$ is always positive, and the measured magnitude of the $T_{\text{off\_delay}}$ is in proportion with the value of $R_1$, which is consistent with the Equation (11).
3 | MULTI-OBJECTIVE OPTIMIZATION OF POWER CONVERTER OPERATION

The objective of this section is to propose a multi-objective gate control strategy for the HyS to combine the advantages of the maximum efficiency gate control strategy and thermal balance gate control strategy.

In [27], the gate drive strategy for the HyS can be controlled at the efficiency strategy, and the thermal balance strategy by adjusting the \( T_{on \_delay} \) or \( T_{off \_delay} \). The efficiency gate control strategy is used to minimize the power loss (referred as \( P_{loss} \)) of the HyS then achieving the high efficiency of the HyS based converter. In the efficiency gate control strategy, the \( P_{loss} \) of the HyS could be minimized by setting the appropriate \( T_{on \_delay} \) or \( T_{off \_delay} \) at a certain output power rating. Because the \( T_{on \_delay} \) or \( T_{off \_delay} \) are determined by the resistor \( R_1 \) and \( R_3 \), the efficiency of the Si/SiC HyS based boost converter can be expressed as,

\[
\eta = \frac{P_{out}}{P_{on} + P_{loss}^{MOS}(R_3, R_1) + P_{loss}^{IGBT}(R_3, R_1) + P_{loss_{\text{others}}}} \tag{12}
\]

where \( P_{loss}^{MOS} \) and \( P_{loss}^{IGBT} \) are the SiC_MOS’s and IGBT’ power losses, respectively. \( P_{out} \) is the output power of the HyS based converter. \( P_{loss_{\text{others}}} \) is the total power losses of other components, for instance, the HyS gate driver losses, inductor losses, and freewheeling diode losses. Therefore, by setting the appropriate value of the resistor \( R_1 \) and \( R_3 \), the high efficiency of the HyS based converter can be achieved.

Because the power loss of the HyS is strongly dependent on the gate control delay times, the balanced junction temperature distribution could be achieved by setting the appropriate gate control delay times of the HyS. Therefore, the thermal balanced gate control strategy is used to achieve the balance \( T_j \) distribution between the two devices inside the HyS then improving the maximum operation temperature safety margin, and ensuring both devices’ \( T_j \) below the junction temperature limits (referred to as \( T_{j\_\text{limit}} \)) at the heavy \( P_{out} \) conditions. The \( T_j \) of the power device can be estimated using Equation \( (13) \).

\[
T_j = T_c + R_{j-c} \cdot P_{loss} \tag{13}
\]

where \( R_{j-c} \), \( P_{loss} \), \( T_j \), and \( T_c \) are the junction to case thermal resistance, device’s total power loss, device’s \( T_j \) and device’s case temperature. Using the thermal balance gate control strategy, the \( T_j \) of the SiC_MOS and the IGBT are equal distribution. Therefore, the \( P_{loss} \) of the SiC_MOS and the IGBT distribution can be expressed as Equation \( (14) \) under the thermal balance condition.

\[
\frac{P_{loss}^{IGBT}(R_3, R_1)}{P_{loss}^{MOS}(R_3, R_1)} = \lambda_R + \frac{\Delta T_c}{R_{j-c}^{IGBT} \cdot P_{loss}^{MOS}(R_3, R_1)} \tag{14}
\]

where \( \lambda_R \) is the junction to case thermal resistance ratio between the two devices. \( \Delta T_c \) is the case temperature difference between the two devices. \( R_{j-c}^{MOS} \) and \( R_{j-c}^{IGBT} \) are the SiC_MOS’ junction to case thermal resistance and IGBT’s junction to case thermal resistance, respectively, which are obtained from their datasheets. Equation \( (13) \) shows that the \( T_j \) of the two devices can be balanced when their \( P_{loss} \) has an optimum ratio by setting the appropriate value of the resistors \( R_1 \) and \( R_3 \). The optimal \( P_{loss} \) ratio of the HyS is also affected by the case temperature deviation and thermal resistance ratio between the two internal devices.

### 3.1 Experiment setup

To compare the efficiency and thermal performance of the HyS at these two different gate control strategies, a Si/SiC HyS based DC/DC boost converter prototype with the proposed gate driver is built and tested as shown in Figure 8 to investigate the efficiency and thermal performance of the HyS under different gate control strategies.

The Si/SiC HyS is constituted with the 1200 V/12.5 A SiC_MOS (C2M0160120D) and the 1200 V/40 A Si IGBT.
Comparison between the thermal balance control strategy and efficiency control strategy

The two gate control strategies of the HyS have different efficiency and thermal performance under heavy and light load conditions. Under the heavy load condition, when the $P_{\text{out}}$ is 9 kW, the measured boost converter’s efficiency and estimated $T_i$ of the two devices inside the HyS at various values of $R_i$ and a constant value of $R_s = 16 \, \Omega$ (means the $T_{\text{on, delay}}$ is constant 0 $\mu$s) are shown in Figure 9.

When the $T_{\text{off, delay}}$ is small, which means the value of $R_i$ is very small, the converter’s efficiency is low. This is because the IGBT’s tail current results in large turn-off switching loss. When the $T_{\text{off, delay}}$ is large, which means the value of $R_i$ is very large, the efficiency of the converter reduces especially at the large $P_{\text{out}}$ rating. It is because the SiC_MOS’s additional conduction loss is increased with the increasing of the gate turn-off delay time especially at the large output current condition. The maximum efficiency of the boost converter is achieved when $T_{\text{off, delay}}$ is about 2.2 $\mu$s and the corresponding $R_i$ is around 190 $\Omega$. When the value of $T_{\text{off, delay}}$ is very small, the $T_i$ of the IGBT is much higher than that of the SiC_MOS. This is because of the large turn-off switching loss caused by the tail current of the IGBT at the short $T_{\text{off, delay}}$ condition. With the increase of the $R_i$, the $T_i$ is decreased, while those of the SiC_MOS are increased. It is because of the decreasing turn-off loss of the main IGBT and the increasing additional conduction loss of the SiC_MOS with the increasing of the $T_{\text{off, delay}}$. When the value of $T_{\text{off, delay}}$ is very large, the $T_i$ of the SiC_MOS is much higher than that of the IGBT. This is because the SiC_MOS’s large additional conduction loss induces the extremely high $T_i$. A too small or too large value of $T_{\text{off, delay}}$ would induce the extremely high $T_i$ of the IGBT or the SiC_MOS approaching their $T_i$ limits. When the $T_{\text{off, delay}}$ is about 1.6 $\mu$s and the corresponding $R_i$ is about 135 $\Omega$, the balanced $T_i$ distribution between the two internal devices can be achieved.

As shown in Figure 9, the maximum efficiency and the thermal balance of the hybrid switch cannot be achieved simultaneously under a certain $P_{\text{out}}$ rating. When the HyS is at the maximum efficiency condition, the corresponding $R_i$ is 190 $\Omega$. However, when the HyS is at the thermal balance condition, the corresponding $R_i$ is 135 $\Omega$. The maximum $T_i$ of the HyS under the balanced strategy is around 49 °C below the $T_i$ limits, while it is only 31 °C below the $T_i$ limits at the maximum efficiency strategy. And these two gate control strategies only induce a conversion efficiency difference of 0.04%. The thermal balance gate control strategy achieves 18 °C lower maximum $T_i$ of the switching devices than the efficiency gate control strategy, which is helpful to reduce the over-temperature risk of the

| No. | Parameters | Values       |
|-----|------------|--------------|
| 1   | $V_{\text{in}}$ | 300 V       |
| 2   | $V_{\text{out}}$ | 600 V       |
| 3   | $P_{\text{out}}$ | 1–12 kW     |
| 4   | $f_s$       | 20 kHz      |
| 5   | $L$         | 1 mH        |
| 6   | $C$         | 2200 $\mu$F |

As shown in Figure 9, the maximum efficiency and the thermal balance of the HyS based boost converter in the steady-state. The FLIR A655sc infrared imager is used to measure the case temperatures of the HyS. Equation (13) is used to calculate junction temperatures of the SiC_MOS and IGBT. The junction to case thermal resistance of SiC_MOS $(R_{\text{th(j-c), MOS}})$ and IGBT $(R_{\text{th(j-c), IGBT}})$ are 0.9 and 0.46 K/$\mu$s, respectively, which are obtained from their datasheets.

$V_{\text{out}}$ is the output voltage; $V_{\text{in}}$ is the input voltage; $D$ is the duty cycle. In this paper, the input voltage and output voltage are 600 and 300 V, respectively. Therefore, $D$ is 50% constant. The average output current rating of the boost converter can be derived as,

$$I_{\text{out}} = \frac{V_{\text{in}}}{(1 - D)R_{\text{load}}}$$  \hspace{1cm}(16)$$

Where $R_{\text{load}}$ is the load resistor. The maximum output power of the boost converter is designed as 12 kW. Therefore, the minimum $R_{\text{load}}$ is 30 $\Omega$ and the maximum average output current is 20 A. Table 2 shows the parameters of the HyS based boost converter.

The HIOKI PW3390 is adopted to measure the efficiency of the HyS based boost converter in the steady-state. When the $T_{\text{off, delay}}$ is small, which means the value of $R_i$ is very small, the converter’s efficiency is low. This is because of the large additional conduction loss caused by the tail current of the IGBT at the short $T_{\text{off, delay}}$ condition. With the increase of the $R_i$, the $T_i$ is decreased, while those of the SiC_MOS are increased. It is because of the decreasing turn-off loss of the main IGBT and the increasing additional conduction loss of the SiC_MOS with the increasing of the $T_{\text{off, delay}}$. When the value of $T_{\text{off, delay}}$ is very small, the $T_i$ of the SiC_MOS is much higher than that of the IGBT. This is because of the decreasing turn-off loss of the main IGBT and the increasing additional conduction loss of the SiC_MOS with the increasing of the $T_{\text{off, delay}}$. When the value of $T_{\text{off, delay}}$ is very large, the $T_i$ of the SiC_MOS is much higher than that of the IGBT. This is because the SiC_MOS’s large additional conduction loss induces the extremely high $T_i$. A too small or too large value of $T_{\text{off, delay}}$ would induce the extremely high $T_i$ of the IGBT or the SiC_MOS approaching their $T_i$ limits. When the $T_{\text{off, delay}}$ is about 1.6 $\mu$s and the corresponding $R_i$ is about 135 $\Omega$, the balanced $T_i$ distribution between the two internal devices can be achieved.

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### Table 2 Parameters of the HyS Boost Converter

| No. | Parameters | Values       |
|-----|------------|--------------|
| 1   | $V_{\text{in}}$ | 300 V       |
| 2   | $V_{\text{out}}$ | 600 V       |
| 3   | $P_{\text{out}}$ | 1–12 kW     |
| 4   | $f_s$       | 20 kHz      |
| 5   | $L$         | 1 mH        |
| 6   | $C$         | 2200 $\mu$F |
HyS. Also, it improves the HyS's maximum output power processing ability and the maximum $P_{\text{out}}$ rating of the HyS based converters.

At the light output power rating, when the $P_{\text{out}}$ is 3 kW, the measured boost converter's efficiency and estimated $T_j$ of the two internal devices of the HyS at various values of $R_1$ and a constant value of $R_3 = 16$ $\Omega$ (means the $T_{\text{on-delay}}$ is constant 0 $\mu$s) are shown in Figure 10.

As shown in Figure 10, the converter's efficiency is improved with the increasing of the $T_{\text{off-delay}}$, while the $T_j$ of the SiC_MOS and IGBT are not obviously changed with the increasing of the $R_1$. This is because the $P_{\text{loss}}$ of the HyS is small under the light load condition. The $T_j$ of the HyS at two gate control strategies are both very low. Therefore, the maximum efficiency gate control strategy is more applicable to the light load conditions.

The calculated maximum $T_j$ of the HyS's internal switches and the measured efficiency of the HyS based converter at two gate control strategies under various $P_{\text{out}}$ ratings are shown in Figure 11.

When the $P_{\text{out}} < 6$ kW, the efficiency of the HyS based boost converter at the efficiency gate control strategy $\approx 0.15\%$ higher than that at the thermal balance gate control strategy. It is because the HyS at the efficiency gate control strategy has a smaller total turn-off switching losses compared to the thermal balance gate control strategy.

When the $P_{\text{out}}$ is larger than 7 kW, the $T_j$ of the HyS at the efficiency control strategy is higher than that at the thermal balance control strategy. This is because the longer $T_{\text{off-delay}}$ at the thermal balance strategy increases the $T_j$ of the HyS, which restricts the maximum $P_{\text{out}}$ handling capacity of the HyS converter. Under the thermal balance gate control strategy, the HyS based boost converter's maximum $P_{\text{out}}$ is 10.5% larger than that under the efficiency gate control strategy when the devices' maximum $T_j$ reach the $T_{\text{limit}}$.

### 3.3 Load current dependent multi-objective control strategy based on the proposed gate driver

If the Si/SiC HyS based converter is solely relying on the efficiency gate control strategy or the thermal balance gate control strategy, there is a severe thermal concern of the HyS's internal switches at the high $P_{\text{out}}$ condition or the efficiency reduction of the converter at the low $P_{\text{out}}$ condition. To combine the advantages of these two gate control strategies within a wide power range, the load current dependent control strategy based on the gate driver is proposed. Its schematic is shown in Figure 12. In general, the load current, DC-link voltage, cooling strategies, and switching frequency of the converter would affect the power loss of the HyS then affecting the optimal gate control strategies of the HyS. However, in the actual converter applications, the DC-link voltage, cooling strategies, and the switching frequency are relatively fixed. Only the load current is a constantly changing value according to the load conditions.
Therefore, in this paper, the load current is used as the operation mode selection indicator of the current dependent control strategy to combine the advantages of the thermal balance gate control mode and the efficiency gate control mode within a wide load condition.

To flexibly alter the gate control strategy of the HyS under different load current, \( R_1 \) inside the HyS driver is replaced with two switches \( S_1 \) and \( S_2 \) in series with \( R_{1-T} \) and \( R_{1-J} \). \( R_{1-T} \) and \( R_{1-J} \) are the optimum \( R_i \) to achieve the efficiency gate control strategy and the thermal balance gate control strategy, respectively. The switches are controlled by a comparator configuration, which compares the output current \( I_{\text{load}} \) with the threshold current reference \( I_{\text{thr}} \). When the output current \( I_{\text{load}} \) is smaller than \( I_{\text{thr}} \), the \( S_2 \) is closed and the \( S_1 \) is open. The HyS's gate control strategy is changed from the thermal balance strategy to the efficiency strategy, so the converter's efficiency is improved at the light load conditions. When the output current \( I_{\text{load}} > I_{\text{thr}} \), the \( S_1 \) is closed and the \( S_2 \) is open. The HyS's gate control strategy is changed from the efficiency strategy to the thermal balance strategy, so the \( T_j \) of the two devices inside the HyS are kept within their specified temperature range with appropriate thermal safety margin at a high \( P_{\text{out}} \) level.

As shown in Figure 11, when the \( P_{\text{out}} > 7 \) kW, the maximum \( T_j \) of the HyS between the efficiency strategy and thermal balance strategy becomes obvious, while the efficiencies of the converter at these two gate control strategies are almost same. Therefore, the threshold current \( I_{\text{thr}} \) is selected to be 12 A, which is corresponding to the \( P_{\text{out}} \) rating of 7.2 kW at the 600 V output voltage condition. The value of \( R_{1-T} \) and \( R_{1-J} \) are selected to be 135 and 190 \( \Omega \), respectively.

When the HyS based converter's \( P_{\text{out}} \) varies from 3 to 9 kW at the 600 V output voltage condition, the measured output voltage \( V_{\text{out}} \), the inductor current \( I_{L} \), IGBT's gate voltage control signal \( V_{GE_{-}\text{IGBT}} \) and SiC_MOS's gate voltage control signal \( V_{GS_{-}\text{MOS}} \) are shown in Figure 13.

When the average current of the inductor is higher than the threshold current reference of 12 A, the \( T_{\text{off}, \text{delay}} \) between the two internal devices' gate voltage signal is decreased within only one switching period cycle. It means that the discharge resistor is quickly altered from \( R_{1-J} \) to \( R_{1-T} \), and the HyS's gate control strategy is altered from the efficiency strategy to the thermal balance strategy. And when the converter's \( P_{\text{out}} \) suddenly varies from 9 to 3 kW, vice-versa.

The measured efficiency of the 40 A single IGBT solution, 40 A single SiC_MOS solution, and the Si/SiC HyS solution with the load current dependent gate control strategy at the 20 kHz switching frequency and various load conditions are shown in Figure 14.

The Si/SiC HyS boost converter's efficiency is almost 0.8% higher than that of the single IGBT based boost converter at the same \( P_{\text{out}} \). When the \( P_{\text{out}} \) is below 6 kW, the efficiency of the single SiC_MOS solution is about 0.29% higher than that of the HyS solution. When the \( P_{\text{out}} \) is 9 kW, the efficiency of the single SiC_MOS solution is only 0.1% higher than that of the HyS solution. It is explained by that the single SiC_MOS's conduction loss is increased dramatically at the high forward current and high \( T_j \) conditions because of the positive temperature coefficient of the SiC MOS, but the conduction loss of the HyS is almost constant because of the main IGBT's drift conduction modulation.

The estimated \( T_j \) of the 40 A single IGBT solution, 40 A single SiC_MOS solution and the Si/SiC HyS solution with the load current dependent gate control strategy at the 20 kHz switching frequency and various output power ratings are shown in Figure 15.

When the \( T_j \) reaches the operation \( T_{j, \text{limit}} \), the 40A single IGBT based boost converter's maximum \( P_{\text{out}} \) is only 4 kW. This is because of the large switching loss of the bipolar Si IGBT under high voltage and load forward current conditions. The \( T_j \) of the single IGBT solution is about 98 °C higher than the HyS solution at 4 kW \( P_{\text{out}} \).

When the HyS based boost converter's \( P_{\text{out}} < 6 \) kW, the single 40 A SiC_MOS's \( T_j \) is lower than that of the HyS solution. It is because the total power losses of the 40A SiC_MOS are smaller than the Si/SiC HyS solution at the low output current condition. When the boost converter's \( P_{\text{out}} \) is higher than 6 kW, the single 40 A SiC_MOS's \( T_j \) is higher than that of the HyS solution. It is because 40 A SiC_MOS's total power losses are...
increased with the increase of the output current rating. However, because of the drift conduction modulation of the main IGBT, the conduction loss of the Si/SiC HyS is almost constant with the increasing of the output current rating. Besides, when the $P_{\text{out}} > 7$ kW, the HyS's gate control strategy is altered to thermal balance gate control strategy, which enables the optimal ratio of the power loss between two internal devices of the HyS to achieve the lower $T_j$ of the switching devices.

When the switching devices’ $T_j$ reach their $T_j_{\text{limits}}$, the maximum $P_{\text{out}}$ of the single 40 A SiC MOS solution and the HyS using the load current dependent gate control strategy are about 9.5 and 10.5 kW, respectively. The HyS’s maximum $P_{\text{out}}$ is $10\%$ larger than that of the single 40 A SiC MOS solutions and is $163\%$ larger than that of the single 40 A IGBT solutions.

4 | CONCLUSION

A novel gate driver solution is proposed for the Si/SiC HyS to achieve its improved cost-effectiveness, high efficiency, and reliable operation in power conversion applications. It makes use of a few components, including resistors, capacitors, and signal diodes to split the single input PWM signal into two separate signals with a specific delay time to realize the HyS’s specific gate control patterns. Compared to the conventional two discrete gate drivers realizing with one complicated auxiliary FPGA, CPLD or DSP, its simplified circuitry keeps the cost-effectiveness of the Si/SiC HyS and reduces the gate control complexity of the HyS based power electronics systems.

The thermal balance gate control strategy and the maximum efficiency gate control strategy of the Si/SiC HyS by setting the specific parameters of the proposed gate driver are extensively investigated and analysed on a boost converter prototype within a wide power range. The HyS’s efficiency gate control strategy could minimize its power loss and achieve the high efficiency of the HyS based converter, especially at the low output power rating. However, there is a severe concern of the SiC MOS’s overheating inside the HyS at heavy load condition. The HyS’s thermal balance gate control strategy keeps the balanced $T_j$ distribution between the two internal devices of HyS within the specified temperature range with appropriate thermal safety margin thus offering a lower operating temperature of the switching devices at the high output power rating. But the maximum conversion efficiency of the HyS can’t be achieved at the low output power condition.

To combine the advantages of the thermal balance gate control strategy and the efficiency gate control strategy within a wide load condition, the load current dependent gate control strategy is proposed and implemented in the novel gate driver. The load current is used as the operation strategy selection’s indicator of the current dependent control strategy. When the HyS based converter’s output power is smaller than a selected reference output power (7.2 kW), the efficiency gate control strategy is selected to achieve high conversion efficiency. When the HyS based converter’s output power is larger than the selected reference output power (7.2 kW), the thermal balance gate control strategy is selected to achieve lower operating temperatures of HyS’s internal devices and reliable operation of the HyS boost converter. Using the proposed novel gate driver with the current dependent control strategy, the Si/SiC HyS solution exhibits marked improvement in the maximum output power processing ability and thermal properties compared to the single SiC MOS and single IGBT solutions.

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