Software Variants for Hardware Trojan Detection and Resilience in COTS Processors

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Abstract—The commercial off-the-shelf (COTS) component based ecosystem provides an attractive system design paradigm due to the drastic reduction in development time and cost compared to custom solutions. However, it brings in a growing concern of trustworthiness arising from the possibility of embedded malicious logic, or hardware Trojans in COTS components. Existing trust-verification approaches, are typically not applicable to COTS hardware due to the absence of golden models and the lack of observability of internal signals. In this work, we propose a novel approach for runtime Trojan detection and resilience in untrusted COTS processors through judicious modifications in software. The proposed approach does not rely on any hardware redundancy or architectural modification and hence seamlessly integrates with the COTS-based system design process. Trojan resilience is achieved through the execution of multiple functionally equivalent software variants. We have developed and implemented a solution for compiler-based automatic generation of program variants, metric-guided selection of variants, and their integration in a single executable. To evaluate the proposed approach, we first analyzed the effectiveness of program variants in avoiding the activation of a random pool of Trojans. By implementing several Trojans in an OpenRISC 1000 processor, we analyzed the detectability and resilience during Trojan activation in both single and multiple variants. We also present delay and code size overhead for the automatically generated variants for several programs and discuss future research directions to reduce the overhead.

Index Terms—Hardware Trojans; COTS; Trojan Resilience

I. INTRODUCTION

In recent years, commercial off-the-shelf (COTS) electronic components have seen increased adoption in diverse domains, including military, avionics, finance, and commercial applications. Since designing a custom hardware product often results in longer deployment period with significant design and manufacturing costs, the use of COTS components prevails even in the most sensitive electromechanical systems such as NASA spacecrafts [1]. However, adopting the COTS flow does not come without its own problems. Security and reliability challenges arise from the fact that COTS component development involves external design and manufacturing facilities. Any of these supply-chain entities could introduce a hidden malicious modification or hardware Trojan in the design to cause a functional failure or leakage of secret information (e.g., encryption keys) during field operation. Existing research on hardware Trojans largely focuses on addressing Trojan insertion in two major supply-chain entities: untrusted foundry and untrusted hardware intellectual property (IP) vendors. Techniques to detect Trojans inserted in an Integrated Circuit (IC) by comparing it with trusted or reference design have been investigated extensively for almost a decade [2]. Unfortunately, these post-silicon detection techniques do not apply to COTS components due to the following reasons:

- For in-house ICs, a golden design is available to the design house, which does not apply to COTS IC.
- Malicious COTS component developers have more flexibility in implementing complex Trojans compared to adversaries at the foundry, since, area, power, and delay constraints cannot be strictly defined during procurement.

Additionally, researchers have proposed several static and dynamic analysis based Trojan detection methods for untrusted soft-IPs obtained from third-party IP (3PIP) vendors. However, they cannot be applied for COTS ICs due to following:

- Approaches for 3PIPs that apply static analysis on the netlist, such as boolean functional analysis [3] and machine learning [4] require white-box accessibility to design. Application of these techniques to COTS ICs would require destructive reverse engineering of the netlist.
- Dynamic approaches that detect Trojans through logic simulation are also not applicable, since the gate-level netlist is often required for the generation of test patterns.

Hence, authentication of COTS electronics is certainly one of the most difficult trust-verification challenges and has not received the attention it needs [2]. A very few ideas have been developed in enabling Trojan resilient computing, specifically in general purpose COTS processors. In the SAFER PATH technique [5], execution of the same program in multiple processing units acquired as individual COTS component from different vendors collectively ensures Trojan resilient computation. This framework requires integration of multiple processing units and various hardware level modifications.

In this paper, we propose a novel and purely software-based solution to enable Trojan detection and resilience in COTS processors during field operation against Trojans that corrupt the program outputs (i.e., modification of variables). During the software integration step of the COTS processor, the program to be executed is divided into several segments...
of codes (defined as compare-blocks). These blocks define the boundaries at which the program states are to be checked during field operation. The code of each compare-block is transformed to a sequential execution of two “variant codes” that are each functionally equivalent to the original code. The program state (relevant variables) after the completion of the first variant is stored temporarily and compared with the resultant state after the second variant is executed. The key idea is that significant differences in frequency and sequence of both opcode and operands among the functionally equivalent variants results in dissimilar switching activities of the internal nets during the execution of individual variants. Therefore, even if a hard to activate Trojan gets triggered in one of the variants and impacts the program states, it will not re-trigger in the same way in any other variant. Even if it does, the impact of the payload (i.e., corruption of critical variable) may not be identical. Dissimilar program states resulting from subsequent executions of two functionally equivalent codes indicate either a Trojan activation or fault propagation. Only during this rare instance, a third variant is executed that is significantly different than the earlier variant codes. A majority voting is executed among the three executions (i.e. variant 1, 2, and 3) to ensure the integrity of the computation even under possible activation of Trojan(s) causing a transient corruption. The proposed solution is distinctive from the other Trojan resilience techniques [5] due to the following:

- It does not depend on redundant processing units or architectural modifications to accommodate voting or synchronization. This translates to shorter time-to-market, lower development cost, and logistical flexibility.
- This can be applied to legacy COTS processors already deployed in the field.
- Since it does not depend on multiple cores or processing elements, acquisition of cores from diverse vendors to evade similar Trojans in all cores is not required.

Please note that we can even run more than three variants (e.g. 5, 7, 9) to improve the probability of withstanding the Trojan without impacting the regular performance, as only two variants would be executed at runtime and others would be invoked upon Trojan activation. Generating a large number of variants of a given program is a non-trivial task. To automatically generate the variants, we have proposed a methodology and tool flow for using existing compiler infrastructure that will require minimal tool development effort and can generate variants for most processor architectures available in today’s market. Overall, we make the following major contributions in this paper:

- We propose a software-based framework that enables Trojan detection and resilience in COTS processors without any design or assembly-time hardware modification. Our technique is one of the very few that are directly applicable to COTS processors.
- We present an automatic variant generation tool flow using LLVM compiler infrastructure that generates the diverse variants using a code similarity metric.
- By analyzing the signal transition data inside a 32-bit RISC microprocessor, we have observed the effectiveness of the tool-generated variants in avoiding activation of the same Trojan in multiple variants.
- We have observed the detection and resilience of the variants against various combinations and sequential Trojan implemented inside the OpenRISC mor1kx CPU [6]. We were able to detect and tolerate [7] majority of the Trojans causing transient corruption.
- We present delay and code size overhead of our approach by generating the variant-integrated code for several C programs in the MiBench suite.

The rest of the paper is organized as follows. Section II briefly describes our threat model. Section III describes our methodology and tool flow. We elaborates the effectiveness of our approach against Trojans and the corresponding overhead in Section IV. Furthermore, we provide discussion on possible attacks and multi core execution of variants in Section V. Finally, we conclude in Section VI.

II. BACKGROUND AND PRELIMINARIES

A. Threat Model

Trojan Insertion Phase: From the third-party IP vendor to the foundry, we assume that a malicious modification of the design can be made at any step of the COTS processor design and manufacturing flow.

Trojan Location: Even though our framework aims to bypass a Trojan within the processor core, a Trojan residing in the cache memory may not be covered. Due to the lack of flexibility in controlling physical read-write location within the cache, such Trojans can experience the desired triggering inputs among multiple variants.

Payload: Our framework focuses on Trojans that corrupts the state of certain registers or wires within the processor that leads to a targeted change in the output (i.e., certain variables) of a program. Such targeted change in program output can be performed by a Trojan that causes a transient corruption once triggered, instead of a persistent corruption. We are not considering a Denial-of-Service (DoS) attacks that simply prevents the normal execution of the program.

Trigger Mechanism: We assume an attacker designs a Trojan based upon some rare activation condition within the

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We broadly classify the large functional trigger space in Table I. COTS IC. The trigger mechanism can be combinational or sequential. If a Trojan triggers in multiple variants and corrupts the program states of each variant similarly, it would not get detected. However, if the activation condition is rare, it is unlikely that the same Trojan will trigger in multiple variants. We broadly classify the large functional trigger space in Table I. Class-1 contains Trojans with simple triggering conditions that are hard to address using our method but can be detected during traditional IP verification phases. Hence, we do not necessarily need to cover them if a directed pre-deployment verification step is present. However, complex trigger mechanisms are likely to activate during logic testing (Class 2) to avoid detection. Such difficult-to-trigger Trojans are better addressed using our proposed method. Trojan activation based on parametric features (voltage, temperature), memory access, page faults, etc., are not considered and are beyond the scope of this work.

B. Existing Work

1) Countermeasures for In-house ICs and 3PIPs: The initial era of hardware Trojan research was focused on post-silicon and run-time detection of foundry inserted Trojans in ICs. As shown in Table I these techniques are mostly either side-channel analysis based [8]–[12] or logic-testing based approaches [13], [14]. Almost all of these techniques rely on one or more of the following requirements: 1) a golden design, 2) golden side-channel signature, and 3) design-time modifications (to implant sensors or to increase observable/controllable points). None of the above-mentioned requirements can be met in COTS IC based development model, rendering such techniques inapplicable. The requirement of design-time modification also inapplicable.

TABLE II

| Approaches | Reference | Detection / Tolerance Phase | HT in IP | HT in IC | HT in COTS IC |
|------------|-----------|-----------------------------|---------|---------|---------------|
| Software Variant | Proposed Approach | Runtime ✓ ✓ ✓ | ✓ | ✓ | ✓ |
| IC Redundancy | SAFER PATH [5] | Runtime X ✓ ✓ | ✓ | ✓ | ✓ |
| IP Redundancy | TrojanGuard [23], HLS [24] | Runtime ✓ ✓ | ✓ | ✓ | ✓ |
| Task Scheduling | [25], [26] | ✓ ✓ | ✓ | ✓ | ✓ |
| Static Analysis | HAL [27], COTD [28] | Pre-Silicon ✓ X | ✓ | ✓ | ✓ |
| Formal Methods | Proof Check [29], Verification [30] | Pre-Silicon ✓ X | ✓ | ✓ | ✓ |
| IP Monitoring | Many-core [31], ISA Power [32] | Runtime ✓ ✓ | ✓ | ✓ | ✓ |
| Side-Channel | Power [33], Delay [10] | Post-Silicon, X ✓ | ✓ | ✓ | ✓ |
| Logic Testing | MERO [15], Region Based [16] | Pre/Post-Silicon X ✓ | ✓ | ✓ | ✓ |
| Design-for-Sec. | Sensors [17], OBISA [18] | Pre/Post-Silicon ✓ ✓ | ✓ | ✓ | ✓ |
| Hardware obfuscation | Logic Encryption [19], HARPOON [18], Camouflaging [20] | Pre-Silicon ✓ ✓ | ✓ | ✓ | ✓ |
| Split Manufacturing | 3D integration [21], 3D integration [22] | ✓ ✓ | ✓ | ✓ | ✓ |

Class of Countermeasure: ∅ Trojan Tolerance, ⊙ Trojan Detection, ⊙ Trojan Prevention

The comparison of variant's outputs facilitates runtime Trojan detection. To facilitate Trojan resilience, three or more variants must be executed in a sequence and their results are compared. “Result” could be the outputs of certain computations in the program as defined by the user (e.g., variables that are considered critical). The comparison of variant’s outputs facilitates runtime Trojan detection. To facilitate Trojan resilience, three or more variants must be executed for majority voting. Therefore, along with the two variants, we integrate additional codes for conditional execution of three or more variants. The code of integrated execution of all variants will replace the original segment of the program from which variants are generated. This process is repeated for all checkpoints in the program as defined by the user. Finally, a single executable is generated from the transformed code. Below we describe these steps in detail.

A. Verification

The COTS processor deployment process is suggested to have a thorough verification step due to the potential trust and reliability issues [35]. This verification step is important since it
complements our proposed solution. As discussed using Table I, the proposed solution has a higher probability of thwarting Trojans with very rare trigger conditions that could be hard to activate using logic testing within a limited time budget. Hence, this step should apply maximum possible test vectors within the limited test time or other verification techniques to detect any easy to activate Trojans.

B. Checkpoint Identification

Before applying any form of transformation to the code, it is necessary to realize the boundaries of variant execution defined as compare-blocks within a program. The end of each block is a checkpoint for comparing the results of a variant pair. The boundary can be within the range of any arbitrary block size where computation can be paused for comparison before moving to the next process. If the user is concerned about Trojan activation in a specific critical region of the code, the compare-block could be described for that region alone. In our current implementation, we support individual functions as compare-blocks.

C. Metric

To estimate the susceptibility of a pair of variants in activating the same Trojan, the $V_S$ metric is formulated. Any two variants of a program ideally should have a diverse frequency and sequence of opcode and operands such that when they execute, the internal activity within the process is very different. Different switching activity of the internal nets during the execution of two variants will significantly decrease the probability of a Trojan being activated in both variants at the same point of execution. If a Trojan is activated only in one variant, the likelihood of detecting the Trojan increases. Even if the same Trojan gets activated in both variants, the impact of the Trojan payload will most likely be different due to the variant code diversity. We prefer to calculate similarity as the case of maximum similarity among two programs are known (i.e., when the programs are identical), which serves as a reference in understanding the value of $V_S$. Besides, measurement of similarity has been well-researched in other domains [36]. Among the large number of variants, the pair that provides minimum similarity can be considered to be most diverse. Quantification of code similarity has received great attention due to its use in metamorphic malware detection [36], [37]. We leverage the technique presented in [36] to calculate code similarity among two variants. To calculate $V_S$, we first segment each instruction of a defined code segment into opcode and operand section. Next, we calculate the counts of all consecutive opcode pairs for each variant as shown in Fig. 2.

The dimensions of the table are $N \times N$, where $N$ is the number of opcodes available in the instruction set architecture. While [36], only performs opcode analysis, we also generate similar count tables for instruction operands as we want to generate variants that are diverse with respect to both instruction and data. The opcode and operand count tables for each variant are flattened and appended as a single vector. We compute $V_S$ by aggregating the element-wise minimum between vectorized opcode and operand sequence count tables for variant pairs as shown in Fig. 2.

Please note that under multithreading and out of order execution, the order of instructions executed at runtime could differ from the sequence present in the assembly code being analyzed for calculating $V_S$. However, the similarity is observed over all consecutive instruction pairs (instead of long sequence of instructions) that are less impacted by such change in execution order. Moreover, if register renaming is supported, the architectural registers that are present at the assembly program are not the same as the physical registers. This could make the operand part of $V_S$ calculation unreliable.

In such a scenario, we can disregard operand similarity for $V_S$ calculation and only utilize the opcode segment.
D. Compiler-based Automatic Variant Generation

We leverage existing compiler infrastructure that will require minimal tool development effort and can generate variants for most processor architectures available in today’s market. Modern compilers provide various optimization passes that transform the code to obtain faster runtime and code size. A large number of code transformations are possible using different optimization passes. Therefore, by applying various combinations and sequences of optimization passes, we can generate a large number of variants. From this large pool of variants, we can identify the best variants using the $V_S$ metric.

Fig. 3 shows the toolflow for the compiler infrastructure using LLVM and Clang in a dotted box. This infrastructure uses a three phase modular design process (i.e., front end, optimizer, and back end) that is amenable to modification. The front end takes a high level source code like C/C++ and maps it to an architecture independent LLVM Intermediate Representation (IR). The LLVM optimizer can apply various transformations to the IR using a series of optimization passes. A user can select a custom series of passes to apply certain transformations and generate a modified IR that is likely to be optimized with respect to code size or runtime. Therefore, by applying different sets of passes to the same IR, we can potentially generate diverse IR codes that are functionally equivalent. When transformed to assembly programs (ALPs), these IR codes are likely to have different usage of opcodes and operands. Using the $V_S$ metric, we can assess all the ALPs and select the variants with lowest similarity among each other.

LLVM contains a large number of distinct passes that leads to infinite number of possible optimization sequences [38]. Therefore, application of all possible pass sequences to find the most diverse variants is not feasible. Prior work on compiler pass selection has focused on the generation of pass sequences for various optimization goals (e.g., code size, power, execution time) using heuristic based search techniques and machine learning. Hence, identification of a database of minimal pass sequences for generating the most diverse set of codes would be a future research. In this work, we used a database of pass sequence generated from the ones presented in [38], [39].

E. Integration of Variants

system() is a standard function in C that executes a specified command by calling the command processor (e.g., UNIX shell or CMD in Windows). The system() function can direct a given program (say host program) to run another program (say external program). After the external program is executed, the control comes back to host and the statements following the system() function continues to execute. We can use the system() function to seamlessly integrate the generated variants. To store the results of each variant we can use fprintf() function in C. Let us assume that there is a compare-block within a given program and we have generated executable of three variants for that block (e.g., v1, v2, v3). To integrate the variants, first we would remove the original compare-block code. In place of the compare-block, we will call the first variant using system(vl), followed by fprintf(filename, variable) to store the state of relevant variable in a file. We will similarly run the second variant and after that additional codes will be included to read-back the two files and compare the variable states among the variants. Following this method, we can run any number of variants and compare their results.

However, because these functions are integrated after the variant generation process, their assembly codes could be identical when used with different variants. An attacker could potentially bypass detection by designing a Trojan that activates based on the execution of these known functions, instead of the original program, allowing the attacker to design a Trojan that activates after each variant (when the identical system call functions are used). To prevent this vulnerability, we can generate diverse implementations of system() and fprintf() using the same framework for variant generation and integrate a different implementation for each variant of the original code segment.

IV. RESULTS

To quantify the effectiveness against Trojans, we perform two major analysis. The first analysis in Subsection IV-A tries to demonstrate that among the extensive design space of possible trigger conditions within a processor, only a very few can activate in multiple variants. The second analysis in Subsection IV-B shows the detection and resilience against hardware Trojans that activate in single and multiple variants. Please note that in both analyses, we only considered Trojans that activate in at least one of the variants of the simulated programs to observe the behaviour of the variants under an attack. However, being able to activate a Trojan is not a requirement for our technique unlike pre-deployment verification [13].

A. Trigger Avoidance Rate Analysis

1) Objective and method: It is critical to understand if the compiler-generated variant-pairs contain trigger conditions that activate in multiple variants. To analyze this we execute one of the variants of a program and observe signals with low but non-zero static probability (SP), A combination of these signals can be used as trigger inputs for creating Trojans that activates when all the trigger inputs to the Trojan become logic high simultaneously. First, we formulate large number of such Trojans of different input sizes (from 4 to 8) that successfully triggers in one of the variants and observe if those hypothetical Trojans activate again during the execution of other variants of the same program. To better understand the trend, we formulate the Trigger Avoidance Rate (TAR) for different variant pairs by...
Fig. 4. Trojan activation analysis for large number of combinational trigger conditions of various input sizes from 4 to 8. For (a), the considered trigger nets have a maximum static probability is 0.05 and for (b), its 0.025. In both cases, a small fraction of the activated trigger conditions in variant 1 reactivates in variant 2 and variant 3. This number decreases as we consider larger trigger inputs (i.e., complex trigger). For (b), the number of activated triggers in all variants are lower compared to (a) due to the smaller static probability range.

By analyzing $TAR$, we seek to answer the following questions: a) What is the probability that an arbitrary valid trigger condition will re-trigger in multiple variants? b) How TAR changes with trigger difficulty of Trojans? c) How the quality of a variant-pair impacts TAR?

2) Simulation process: We generated three variants from a linear feedback shift register (LFSR) program written in C using the LLVM-based framework. We executed these variants in the Plasma processor from OpenCores which is a 32-bit RISC microprocessor [40]. We simulated the IP core in Xilinx Vivado and captured the signal states of the internal wires.

3) Analysis of results: To construct the emulated Trojans we analyzed all the internal signal states from simulation of the Plasma processor during variant-1 execution and calculated the SP of all signals. The value of SP ranges from 0.00 to 1.00, with lower values (e.g., <0.5) indicating that the signal stays at logic-1 state for shorter amount of time throughout the simulation and vice-versa. We divide the low SP signals into two groups, one with SP range between 0.05 to 0.001 and other between 0.025 to 0.001. These nets rarely become logic-1 during variant-1 execution and we can construct Trojan triggers of different input sizes using these nets. As shown in Fig. 4 (a) and (b), for both the SP ranges, we were able to find a large number of combinational trigger conditions of 4, 5, 6, 7, and 8 inputs that activate at least once during variant-1 execution. However, for lower SP range among these two (i.e., Fig. 4 (b)), the number of rare trigger conditions reduces due to the presence of fewer nets in this SP range that activate in variant-1 (e.g., from 18742 down to 9290 for 4-input triggers). The Trojan space also reduces as we consider larger input size of the triggers from 4 to 8 (i.e., complex trigger condition).

As shown in Fig. 4 (a), when variant-1 executes, 18742 trigger conditions can be constructed that have 4 trigger nets with maximum SP of 0.05. However, when we observed those activated Trojans during the execution of variant-2, only 2830 of them activated again. For variant 3, the number is also considerably lower. The number of reactivated Trojans in variant-2 and variant-3 reduces as we consider larger input sizes from 4 to 8. This is also the case for Fig. 4 (b), where the trigger nets are from signals with SP below 0.025. In this case, the number of reactivated Trojans in variant-2 and 3 are even smaller.

To summarize the findings, we utilize the TAR metric. TAR shows the percentage of Trojans that do not reactivate. Hence, a higher TAR value means the same Trojans are less likely to activate across multiple variants. As shown in Fig. 5 (a), the TAR improves for a higher trigger input size. Hence, complex trigger conditions are less likely to reactivate across multiple variants. In Fig. 5 (b), the TAR for signals with lower SP is shown. Compared to (a), the TAR is generally higher for Trojans of the same input size as the signals being considered are less likely to reactivate due to lower SP. Therefore, the LLVM-generated variants are more effective for hard-to-activate Trojans that generally contain larger input size and/or lower SP.

We also note that variant-2 consistently provides higher TAR compared to variant-3. This observation indicates the benefit of choosing variant pairs that are as diverse as possible. The $V S$ between variant pair 1 and 2 is lower (i.e., more
TABLE III
DESIGN OF TROJANS INSERTED IN THE OPENRISC mor1kx CPU AND THEIR IMPACT ON VARIANTS.

| Trojan Name | Insertion location | Trigger Signal | Trigger Type | Payload | Activation in V1/V2/V3 | Output of Variant (Hex) | Detection | Tolerance |
|-------------|-------------------|----------------|--------------|---------|------------------------|-------------------------|-----------|-----------|
| T1          | Execution         | shift_msw[13:0], exec_op[4:0].uclk_flag, clr_u.uclk_overflow_set, taking_u.uclk_op.o, exec_op_movhi.i, exec_op_extz[i:3:0] | Combinational | Invert multiplier’s selection bit | 1/0/0 | V1: 3E56A4C9 V2: 8FFFFF87 V3: 8FFFFF87 | Yes | Yes |
| T2          | Decode            | opc_insn        | Sequential   | Change immediate field value | 1/0/0 | V1: 8FFFFF87 V2: 8FFFFF87 V3: 8FFFFF87 | Yes | Yes |
| T3          | Decode            | fetch_rfa2_addr.i | Sequential   | Change ALU logic operation | 1/0/0 | V1: 8FFFFF66 V2: 8FFFFF87 V3: 8FFFFF87 | Yes | Yes |
| T4          | Decode            | opc_alu         | Sequential   | Invert immediate selection control bit | 1/0/0 | V1: 8FFFFF6D V2: 8FFFFF87 V3: 8FFFFF87 | Yes | Yes |
| T5          | Decode            | fetch_rfa1_addr.i, fetch_rfa2_addr.i, fetch_rfa3_addr.i, fetch_rfa4_addr.i, fetch_rfa5_addr.i, fetch_rfa6_addr.i | Combinational | Change immediate field value | 1/1/0 | V1: 8FFFFF66 V2: 8FFFFF87 V3: 8FFFFF87 | No | No |
| T6          | Decode            | opc_insn        | Sequential   | Change immediate field value | 1/1/0 | V1: 7F3A552A V2: 8FFFFF87 V3: 8FFFFF87 | Yes | No |
| T7          | Decode            | decod_opc_setflag.u | Sequential   | Change ALU logic operation | 1/1/0 | V1: 8FFFFF6C V2: 8FFFFF87 V3: 8FFFFF87 | Yes | No |
| T8          | Decode            | opc_alu         | Sequential   | Invert immediate selection control bit | 1/1/0 | V1: 8FFFFF61 V2: 8FFFFF87 V3: 8FFFFF87 | Yes | Yes |
| T9          | Execution         | exec_op[4:0].u.uclk_flag, clr_u.uclk_overflow_set, taking_u.uclk_op.o, exec_op_movhi.i, exec_op_extz[i:3:0] | Combinational | Invert multiplier’s selection bit | 1/1/0 | V1: 8FFFFF6E V2: E0CB4790 V3: 8FFFFF87 | Yes | Yes |

dissimilar) compared to variant pair 1 and 3. Hence, lower V.S (lower similarity among variant pairs) is beneficial for avoiding multiple triggering of the same Trojan.

B. Detection and Resilience Analysis

1) Objective and method: The goal of this analysis is to understand the effectiveness our solution in detecting and tolerating the activation of Trojans in a single, as well as in multiple variants. While the previous analysis showed that arbitrarily inserted hard-to-activate trigger conditions rarely trigger in multiple variants, it is important to discuss the impact of both single and multiple activation. To facilitate our analysis, we have handcrafted and inserted Trojans inside a processor by altering its hardware description language.

2) Simulation process: We selected the OpenRISC mor1kx CPU with Marocchino pipeline implementation written in Verilog as our target platform for Trojan insertion. The program to be executed on the processor is the Tiny Encryption Algorithm (TEA) written in C. We combined our variant-generation framework with the LLVM backend for openRISC and created the variant-integrated assembly from the C implementation of TEA. Finally, we used a cross-compiler GCC toolchain “or1k-elf-gcc” to create the executable. We used Icarus Verilog along with FuseSoC Linux command-line tool to simulate the executable in the processor.

Since our analysis requires activation of the Trojans during simulation, the trigger circuits are designed based on the internal activity of the processor when the target executable of the TEA program is running. Therefore, first we monitored the waveform of various internal signals of the processor that can serve as valid trigger conditions for the variant-integrated TEA program. Table III shows the location, trigger signals, and trigger type for each Trojan we inserted. For example, the first Trojan T1 is inserted in the execution module of the processor and the second one is inserted in the decoder. A combinational trigger means that the Trojan is activated as soon as the desired trigger value appears on the trigger signals. The sequential triggers are activated only when a desired “sequence” of values appear on the trigger signals. Our threat model primarily focuses on Trojans that try to alter the program output, instead of causing a denial of service through arbitrary or persistent corruption. Therefore, the payload signal for each Trojan is designed to cause a transient corruption of different signals that leads to a faulty encryption result generated by the TEA program.

3) Analysis of results: The first four Trojans (T1-T4) activate only once and impact the first variant while the other five Trojans (T5-T9) activate in multiple variants. Table III shows the activation of the Trojans in different variants and the corresponding encrypted output. If the encryption output does not match for the first two variants, the Trojan gets detected during the comparison and third variant is automatically executed for majority voting. The Trojan is assumed to be tolerated only when the majority voting provides the correct encryption result (i.e., 32’h8FFFFFFF87).

Once Trojan T1 activates, the addition operation in the execution module is performed with a corrupted value. As a result, the processor produces an incorrect encrypted output in the first variant (shown in red fonts). On the other hand, the processor generates the correct output for the second variant as the Trojan stays untriggered. After comparing the result of the first two variants, the Trojan was detected. Due to the mismatch in the result, the third variant got executed and produced correct output as T1 did not reactivated. Activation of Trojan T2 corrupts the immediate value of the instruction that could either be the program’s input data or the memory address. During the activation of T2, the immediate field contained input plaintext that led to a corrupted encryption output in the first
variant but correct result in the second. The Trojan was detected and tolerated in the earlier manner as it does not trigger during the second and third variant. Triggering of Trojan T3 changes the next instruction from addition to multiplication leading to a corrupted encryption result. As the Trojan only activated in the first variant and was dormant in second and third variant, it was detected and the correct encryption result was found from majority voting. Trojan T4 changes the immediate selection bit of the decoded instruction. During the execution of the first variant the Trojan activates and causes the encryption result to change. For the second and third variant, the Trojan did not trigger and got detected and tolerated.

Trojan T5 activated in both the variants and corrupted the encryption output in the same manner. It corrupted the immediate field of the instruction that contains the input plain-text in both the variants. Since the plain-text is identical for all variants, the final impact on the encrypted output remained the same. Protection against such Trojan can be improved with more diverse variants and judicious transformation of register usage for critical data across variants. Trojan T6 and T7 triggers in both first and second variant but unlike T5, they do not corrupt the output in identical manner for both the variants. Therefore, the Trojan is detected due to the mismatch of the output. However, since both the variants generated faulty outputs, correct execution of the third variant could not provide the correct output through majority voting. Such a scenario could be addressed by including more variants (e.g., five or seven). Finally, Trojan T8 and T9 are similar to T6 and T7 as they all activate during first and second variant. However, activation of T8 and T9 during first variant execution do not impact the encryption output. Therefore, by executing the third variant, correct encryption results were found.

C. Overhead Analysis

Fig. 6 and Fig. 7 present the overhead in code size and execution time due to the variant-based execution of several C programs from the MiBench suite and two implementations of Data Encryption Standard (DES) algorithm. Table IV includes variable names and their types that are protected (i.e., compared after variant execution) in each program. It also includes the size of the file where these variables are stored as program output for comparison. The code overhead is calculated by comparing the lines of code in the assembly version of the original program with the variant-integrated one. The variant-integrated program includes codes for three variants and system calls to compare the variables. As shown in Fig. 6, using the left vertical axis, we presented the code size of the original program, individual code size of the three variants, and code size of the variant-integrated solution that contains three variant and additional codes to execute them and compare results. Since the programs are very different with respect to their code size, we used a logarithmic scale for the Lines of Code (LoC). We can observe that the original program and its three diverse variants have similar LoCs. Therefore, our LLVM-based framework is generating variants with similar code sizes, yet diverse with respect to opcode and operands. Using the right vertical axis, we presented the percentage of increase in LoC from the original program to the variant-integrated one. Please note that the overhead reduces gradually as we consider programs with large code size. Assuming the three variants are of similar size, our framework should increase the code size by 200% for any program, but the additional code for integration of variants and comparing the result leads to different overhead depending on the size of the original program. For a small program like qsort with 227 LoC, the additional code for integration (i.e., 1751 LoC) impacts the overhead significantly. However, for a larger program like susan with 8784 LoC the overhead is much lower.

To calculate the execution time, we used performance analyzing tool in Linux called perf. We used the 12-core Ryzen 3900x CPU. Fair comparison of the execution time overhead requires us to use a single core for executing the original program as well as the variant-integrated one. Hence, we disabled all the cores except one to ensure that the program would run only in a single core. The perf tool was used to run each program 10 times and obtain the average execution time. As shown in Fig. 7 using the left vertical axis, we presented the execution time of the original program and the variant-integrated counterpart that executes two variant and compares their results. The overhead could vary depending on

| Program name | Variable Name | Variable Type | Diff Size |
|--------------|---------------|---------------|-----------|
| bitcount     | n             | long Int      | 4 KB      |
| CRC32        | olden,32, charcnt, crc | long Int x 3  | 491 MB    |
| DES          | result        | long long hex | 32 KB     |
| djkstra      | chNode, qNext | long, Int     | 596 KB    |
| FFT          | ReaOut, ImagOut | float, hex  | 948 KB    |
| patricia     | time, addin, s_addit | float, hex  | 1.5 MB    |
| qsort        | array[i].x, array[j].y, array[i].z | Int  | 1.5 MB     |
| rawaudio     | outp          | unsigned char | 102 MB    |
| rawaudio     | outp          | Int           | 74 MB     |
| sha          | data, count, digest | long Int, long hex | 2 MB |
| susan        | out           | unsigned char | 456 KB    |
| Triple DES   | value, plain  | char, long int | 568 KB |

Fig. 6. Code size overhead of our variant-integrated approach for several programs. The left vertical axis denotes lines of code (LoC) and the right one denotes % of increase in LoC for our solution.
As a result, we can also run the compare portion of the code with low code overhead such as Susan and Triple DES incurred in specific cores by assigning the CPU affinity for each variant in parallel in a multi-core system. We can also run each variant processes. This will enable us to run multiple child processes using `execl()` function call From GNU C library. Alternatively, we can also use the `clone()` function call to the main program. The solution could be advanced to detect and tolerate more diverse Trojan payloads such as persistent corruption and information leakage. Currently our framework primarily addresses payloads with transient corruption. Second, static diversity analysis for a variant pair might differ during execution for COTS with out-of-order execution, speculative execution or similar optimizations. We can extend the similarity metric to account for such behavior in COTS IC. Finally, the code size and execution time overhead is also significant. Hence, future research should involve identification of the compiler pass sequence that generates diverse variants with lower overhead.

V. DISCUSSION

A. Trojan Insertion based on the Compare Function

We note that if an attacker is aware of our proposed defense, they may craft a Trojan that will disable the compare logic. However, an attacker would have to enumerate the possible compare instruction instances that can be compiled and executed on the processor to ensure our defense is bypassed. Several variants can be crafted of the compare function – CMP, SUB, XOR, etc. If the attacker chooses to corrupt all possible implementations of compare, the number of impacted instructions would increase the detectability of the Trojan as the corruption across original code variants would be high. As a result, we can also run the compare portion of the code through the variant generation and dynamically choose among a valid set of compare functions during runtime.

B. Other Variants Integration Techniques

In our methodology section, we proposed to use `system()` function call to run our executable variants. The variant execution using `system()` in the main program is a sequential operation. It implies that the execution order after `system()` call will stall until the variant execution completes and returns to the main program. Alternatively, we can also use the `exec()` function call From GNU C Unistd.h library. Using `exec()`, we can run our variants as multiple child processes. This will enable us to run multiple child processes in parallel in a multi-core system. We can also run each variant in specific cores by assigning the CPU affinity for each variant process. Such parallel execution of variants can help reduce the runtime overhead significantly.

VI. CONCLUSION

Existing countermeasures against hardware Trojans are generally inapplicable for COTS components. In this paper, we have drawn attention to this serious problem by discussing the limitations of the existing solutions when it comes to COTS ICs. We have presented a novel solution and associated toolflow for runtime Trojan detection and resilience in untrusted COTS processors through the creation and execution of Trojan-aware software variants. The proposed work relies purely on judicious modification of software and, unlike existing solutions, does not require hardware support or architectural changes. We have shown that by selecting diverse variants using the VS metric, the probability of simultaneous activation of a Trojan in multiple variants can be drastically reduced. We demonstrated the detection and resilience capability of our approach using several sample Trojans implemented in a RISC processor. Even though the proposed solution incurs delay in execution time due to the need to perform multiple version of the program and comparing the results, it is one of the very few solutions that could be used for untrusted COTS processors.

The proposed paradigm can be extended in three major ways. The solution could be advanced to detect and tolerate more diverse Trojan payloads such as persistent corruption and information leakage. Currently our framework primarily addresses payloads with transient corruption. Second, static diversity analysis for a variant pair might differ during execution for COTS with out-of-order execution, speculative execution or similar optimizations. We can extend the similarity metric to account for such behavior in COTS IC. Finally, the code size and execution time overhead is also significant. Hence, future research should involve identification of the compiler pass sequence that generates diverse variants with lower overhead.

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