Scaled indium oxide transistors fabricated using atomic layer deposition

Mengwei Si, Zehao Lin, Zhizhong Chen, Xing Sun, Haiyan Wang and Peide D. Ye

To continue to improve integrated circuit performance and functionality, scaled transistors with short channel lengths and low thickness are needed. But further scaling of silicon-based devices and the development of alternative semiconductor channel materials that are compatible with current fabrication processes are challenging. Here we report atomic-layer-deposited indium oxide transistors with channel lengths down to 8.0 nm, channel thicknesses down to 0.50 nm and equivalent dielectric oxide thickness down to 0.84 nm. Due to the scaled device dimensions and low contact resistance, the transistors exhibit high on-state currents of 3.1 A mm\(^{-1}\) at a drain voltage of 0.5 V and transconductance of 1.5 S mm\(^{-1}\) at a drain voltage of 1.0 V. Our approach provides a promising alternative channel material for scaled transistors with back-end-of-line-processing compatibility.
Articles
Nature Electronics

Articles

Nature Electronics

(ref. 22), measured by atomic force microscopy (AFM), being beneficial to the thickness scaling of ALD In2O3. The device has a channel width ($W_{ch}$) of 2.0 μm for $L_{ch} \geq 40$ nm, whereas $W_{ch}$ of 0.6 μm for $L_{ch} < 40$ nm. The $W_{ch}$ value was accurately defined by electron-beam (e-beam) lithography and dry etching (Supplementary Fig. 1b). A reduced $W_{ch}$ is used to suppress the self-heating effect. Ni by e-beam evaporation is used as the source/drain electrode. The device fabrication process is comprehensively discussed in Methods. Figure 1b shows the high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) with energy-dispersive X-ray spectroscopy (EDX) mapping of a representative In2O3 transistor with $L_{ch}$ of 8.0 nm, $T_{ch}$ of 3.5 nm and hafnium oxide thickness ($T_{ox}$) of 3.0 nm, highlighting the Ni/In/O elements. EDX mapping with Ni/In/Hf/O elements is shown in Supplementary Fig. 1a. $L_{ch}$, defined as the distance between the source/drain Ni electrodes, is measured to be 8 nm in this device. Figure 1c presents the HAADF-STEM with EDX mapping images on a W/HfO2/Al2O3/In2O3/Ni stack, with In2O3 thicknesses ranging from 0.7 to 1.5 nm. The thicknesses of In2O3 are determined by both AFM measurements and transmission electron microscopy (TEM) images (similar to a previous work24). Figure 1d,e shows the $I_D–V_{GS}$ (gate-source voltage) and $I_D–V_{DS}$ characteristics of a representative ALD In2O3 transistor with $L_{ch}$ of 1 μm, $T_{ch}$ of 1.2 nm and 10.0 nm HfO2/1.0 nm Al2O3 as the gate insulator. The device exhibits a high on/off ratio of $>10^{10}$ and negligible hysteresis due to the semiconductor with a relatively wide bandgap and high-quality oxide/semiconductor interface.

Fig. 1 | Schematic, TEM images and I–V characteristics of ALD In$_2$O$_3$ transistors. a. Schematic of an ALD In$_2$O$_3$ transistor. b. HAADF-STEM cross-sectional image with EDX elemental mapping of an In$_2$O$_3$ transistor with $L_{ch}$ of 8.0 nm, $T_{ch}$ of 3.5 nm and 3.0 nm HfO$_2$ as the gate insulator, capturing the 8.0 nm channel length. c. HAADF-STEM cross-sectional images with EDX elemental mapping and AFM measurements of In$_2$O$_3$ transistors with W/HfO$_2$/Al$_2$O$_3$/In$_2$O$_3$/Ni gate stack with $T_{ox}$ ranging from 0.7 nm to 1.5 nm. d,e, $I_D–V_{GS}$ (d) and $I_D–V_{DS}$ (e) characteristics of a representative ALD In$_2$O$_3$ transistor with $L_{ch}$ of 1μm, $T_{ch}$ of 1.2 nm and 10.0 nm HfO$_2$/1.0 nm Al$_2$O$_3$ as the gate insulator. The device exhibits a high on/off ratio of $>10^{10}$ and negligible hysteresis due to the semiconductor with a relatively wide bandgap and high-quality oxide/semiconductor interface.
Fig. 2 | Thickness scaling of ALD In₂O₃ down to 0.5 nm. a–c, \( I_D - V_{GS} \) characteristics of ALD In₂O₃ transistors with \( L_m \) of 40.0 nm; 5.0 nm HfO₂ as the gate insulator; and \( T_{ch} \) of 0.80 nm (a), 0.65 nm (b) and 0.50 nm (c). d–f, \( I_D - V_{GS} \) characteristics of the same ALD In₂O₃ transistors as a–c with \( L_m \) of 40.0 nm; 5.0 nm HfO₂ as the gate insulator; and \( T_{ch} \) of 0.80 nm (d), 0.65 nm (e) and 0.50 nm (f). g–i, \( I_{D,max} \), \( g_m \) and \( g_{ds} \) scaling metrics of ALD In₂O₃ transistors with different \( T_{ch} \) values and with 5 nm HfO₂ as the gate insulator at \( V_{GS} \) of 1 V. Each data point represents the average of at least five devices. Well-behaved transfer and output characteristics with an on/off ratio of >10⁷ are achieved with channel thickness down to 0.5 nm. The impact of the Schottky barrier at the metal/semiconductor interface on the output characteristics is clearly observed with \( T_{ch} \) below 1 nm due to the effect of quantum confinement on the band structure of the ultrathin In₂O₃ film.

wide bandgap of In₂O₃ (~3.0 eV) and negligible hysteresis due to the high-quality oxide/semiconductor interface. This device has a sub-threshold (SS) of 130.4 mV dec⁻¹ at \( V_{GS} \) of 1 V, which can be further reduced by EOT scaling and proper interface engineering.²²,²³

Device scaling
To further improve the performance of ALD In₂O₃ transistors, device scaling is performed including channel length scaling, EOT scaling and channel thickness scaling, where EOT scaling and channel thickness scaling are essential to enhance the gate electrostatic control to improve the immunity to SCEs. \( T_{ch} \) scaling down to 0.5 nm is achieved in this work as shown in the \( I_D - V_{GS} \) characteristics with \( T_{ch} \) of 0.80, 0.65 and 0.50 nm (Fig. 2a–c). The corresponding \( I_D - V_{DS} \) characteristics are shown in Fig. 2d–f. The devices have SS of 109.0, 114.3 and 108.2 mV dec⁻¹ at \( V_{DS} \) of 1 V for \( T_{ch} \) of 0.80, 0.65 and 0.50 nm, respectively. Here 5 nm HfO₂ is used as the gate dielectric. Evidently, even with \( T_{ch} \) of 0.5 nm, well-behaved transfer characteristics with on/off ratios over seven orders are achieved. A functional transistor made of a 3D semiconducting channel material and with \( T_{ch} \) as low as 0.5 nm has never been reported before because of two reasons. First, it is very challenging to achieve an atomically smooth and uniform semiconducting film by conventional thin-film deposition techniques such as sputtering, chemical vapour deposition and so on, resulting in the degradation of electrical performance due to carrier scattering and change in band structures due to roughness. Second, it is difficult to form a good metal/semiconductor contact with low contact resistivity on an ultrathin In₂O₃ film.
First, the layer-by-layer self-limiting growth mechanism ensures an atomically smooth surface and uniform film. Second, the CNL of bulk In₂O₃ aligns at about 0.4 eV above the conduction band edge (Eᵥ); therefore, thick In₂O₃ behaves like a conducting oxide. As a result, the Fermi level is pinned above Eᵥ for a metal/In₂O₃ contact, leading to a low contact resistance below 0.1 Ω mm even at the nanometre scale. The contact resistance was extracted by the transmission line method. Note that the above property is fundamental when searching for a 3D semiconductor with high performance for an ultrathin channel. It is expected that a 3D semiconductor with CNL aligning far above Eᵥ (or far below the valence band edge as the valence band edge (Eₓ) for p-type devices) is necessary to achieve a high-performance transistor with an ultrathin channel at the nanometre scale. Figure 2g–i presents the maximum drain current (I蠹) scaling metrics of In₂O₃ transistors with Lₘ from 1 µm to 50.0 nm, Tₑ of 3.5 nm and Tₘ of 3.0 nm, 3.5 nm and 5.0 nm. I蠹 is extracted at Vₑ – Vₛ = 1 V and Vₓ = 1 V. gₛ is extracted at Vₓ = 1 V. Each data point represents the average of at least five devices. High I蠹 of 1.2 A mm⁻¹ at Vₓ = 1 V and Vₓ = 1 V and gₛ of 1.55 mm⁻₁ at Vₓ = 1 V are achieved.

First, the layer-by-layer self-limiting growth mechanism ensures an atomically smooth surface and uniform film. Second, the CNL of bulk In₂O₃ aligns at about 0.4 eV above the conduction band edge (Eᵥ); therefore, thick In₂O₃ behaves like a conducting oxide. As a result, the Fermi level is pinned above Eᵥ for a metal/In₂O₃ contact, leading to a low contact resistance below 0.1 Ω mm even at the nanometre scale. The contact resistance was extracted by the transmission line method. Note that the above property is fundamental when searching for a 3D semiconductor with high performance for an ultrathin channel. It is expected that a 3D semiconductor with CNL aligning far above Eᵥ (or far below the valence band edge as the valence band edge (Eₓ) for p-type devices) is necessary to achieve a high-performance transistor with an ultrathin channel at the nanometre scale. Figure 2g–i presents the maximum drain current (I蠹) scaling metrics of In₂O₃ transistors with Lₘ from 1 µm to 50.0 nm, Tₑ of 3.5 nm and Tₘ of 3.0 nm, 3.5 nm and 5.0 nm. I蠹 is extracted at Vₑ – Vₛ = 1 V and Vₓ = 1 V. gₛ is extracted at Vₓ = 1 V. Each data point represents the average of at least five devices. High I蠹 of 1.2 A mm⁻¹ at Vₓ = 1 V and Vₓ = 1 V and gₛ of 1.55 mm⁻₁ at Vₓ = 1 V are achieved.
quantum confinement on the band structure of the In$_2$O$_3$ thin film. The drain-current scaling metrics are found to deviate from 1/L (Fig. 2g), indicating that it is more difficult to accumulate carriers in long channels, most likely due to the percolation mechanism. Additional data on SS and threshold voltage ($V_T$) scaling metrics are found to deviate from 1/V$_DS$ (Fig. 3a) and $V_T$ (Fig. 3b). Figures 3c,d show the scaling metrics of the best-performance In$_2$O$_3$ transistors with $L_{ch}$ from 1 mm to 8.0 nm with $T_{ox}$ of 2.5 nm. Lower voltages are used for shorter channel devices to avoid the impact of self-heating on devices.

**Device performance benchmarking**

The performance of scaled ALD In$_2$O$_3$ transistors in this work is benchmarked with state-of-the-art high-performance transistors with an ultrathin channel, such as 2D transistors and oxide semiconductor transistors, using figures of merit of $I_{ON}$, $g_m$, $R_C$, and mobility versus channel thickness (Supplementary Table 1). ALD In$_2$O$_3$ transistors exhibit the largest $I_{ON}$ in the range of 1.0–3.5 nm and the largest $g_m$ below 3.5 nm, among all the known semiconductor thin films to the best of our knowledge (Fig. 5a,b). Such high-performance material and device properties are mainly contributed by the low contact resistance benefiting from the unique CNI alignments in In$_2$O$_3$ (Fig. 5c) and the high mobility in the

---

**Fig. 4 | Channel length scaling of ALD In$_2$O$_3$ transistors down to 8 nm.** a, b. $I_D$-$V_{GS}$ (a) and $I_D$-$V_{DS}$ (b) characteristics of In$_2$O$_3$ transistors with $L_{ch}$ of 8.0 nm, $T_{ox}$ of 2.5 nm and EOT of 0.84 nm. c, d. $I_{D,max}$ (c) and $g_m$ (d) scaling metrics of the best-performance In$_2$O$_3$ transistors with $L_{ch}$ from 1 mm to 8.0 nm with $T_{ox}$ of 2.5 nm. Lower voltages are used for shorter channel devices to avoid the impact of self-heating on devices.

**Fig. 5 | Benchmarking of ALD In$_2$O$_3$ with other ultrathin semiconductors.** a-d. Comparison of $I_{ON}$, $g_m$, $R_C$ and mobility with channel thickness characteristics with other high-performance oxide semiconductor (doped In$_2$O$_3$) devices by sputtering and 2D semiconductor devices (MoS$_2$, WS$_2$, and black phosphorus). The data used in this figure are listed in Supplementary Table 1. ALD In$_2$O$_3$ demonstrates the best performance in terms of $I_{ON}$, $g_m$, $R_C$ and mobility in the 1.0-3.5 nm range compared with all known semiconductor materials to the best of our knowledge.
nanometre scale between 1.0 and 3.5 nm, also benefiting from the atomic thickness control of ALD (Fig. 5d).

Conclusions

We have reported an ALD-based oxide semiconductor transistor technology that shows promising on-state currents—compared with both established and emerging material technologies—when channel thicknesses are fabricated in the range of approximately 1.0–3.5 nm. Our approach takes advantage of the self-limiting growth mechanism of ALD and the unique band structure of In$_2$O$_3$. The conformal deposition on 3D structures by ALD also has the potential to create new opportunities for 3D integration, such as BEOL-compatible transistors for monolithic 3D integration and semiconductor channels for 3D vertical NAND.

Methods

Device fabrication. The device fabrication process is similar to previous work$^{24}$. The device fabrication process started with solvent cleaning of the p$^+$ Si substrate with thermally grown 90 nm SiO$_2$. A bilayer photolithography process (PMGI semiconducting layers and PMMA insulating layers) was used to fabricate ultra-thin In$_2$O$_3$ films with various thicknesses on the p$^+$ Si substrate. The thickness of the bilayer In$_2$O$_3$ film was determined by atomic force microscopy and ellipsometry. The In$_2$O$_3$ films were deposited by ALD at 200 °C with [(CH$_3$)$_2$N]H$_2$O and H$_2$O as the H$_2$O and O precursors, respectively. The In$_2$O$_3$ films were annealed at 350 °C in an N$_2$ environment.

Material characterization. The thickness of the In$_2$O$_3$ films was determined by the AFM,_Keyiff_ Talos F200X operated at 200 kV equipped with Super-X EDX was used for HAADF-STEM imaging. The AFM measurements were carried out on the AFM Dimension 3100 atomic force microscope system. TEM lamella samples were prepared with Helios G4 UX DualBeam scanning electron microscope. FEI Talos F200X operated at 200 kV equipped with Super-X EDX was used for HAADF-STEM imaging.

Device characterization. Electrical characterization was carried out with a Keysight B1500 system and a Cascade Summit probe station in the dark and N$_2$ environment. The electrical characterization was carried out with a Keysight B1500 system and a Cascade Summit probe station in the dark and N$_2$ environment.

Data availability

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request. The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

Received: 14 September 2021; Accepted: 11 January 2022; Published online: 21 February 2022

References

1. Loubet, N. et al. Stacked nanosheet gate-all-around transistor to enable scaling beyondFinFET. In 2017 Symposium on VLSI Technology T230–T231 (IEEE, 2017).

2. Yang, L. et al. High-performance MoS$_2$ field-effect transistors enabled by high-speed black phosphorus field-effect transistors approaching ballistic limit. Sci. Adv. 5, eaau3194 (2019).

3. Chou, A.-S. et al. High on-current 2D nFET of 390 μA/μm at $V_{dd}$=1V using monolayer CVD MoS$_2$ without intentional doping. In 2020 IEEE Symposium on VLSI Technology 1–2 (IEEE, 2020).

4. Shen, P. C. et al. Ultralow contact resistance between semimetal and monolayer semiconductors. Nature 593, 211–217 (2021).

5. Lin, D. et al. Scaling synthetic WS$_2$ dual-gate MOS devices towards sub-nm CET. In 2021 Symposium on VLSI Technology 1–2 (IEEE, 2021).

6. McLellan, C. J., Yalon, E., Smite, K. H., Kaur, A., Urayan, S. V. & Pop, E. F. Current density in monolayer MoS$_2$ doped by Al$_2$O$_3$, ACS Nano 15, 1587–1596 (2021).

7. Nomura, K. et al. Amorphous oxide semiconductors for high-performance flexible thin-film transistors. Jpn. J. Appl. Phys. 45, 4303–4308 (2006).

8. Kamiya, T., Nomura, K. & Hosono, H. Present status of amorphous In–Ga–Zn–O thin-film transistors. Sci. Technol. Adv. Mater. 11, 044305 (2010).

9. Matsubayashi, D. et al. 20-nm-node trench-gate-self-aligned crystalline In–Ga–Zn–O oxide FET with high frequency and low off-state current. In 2015 IEEE International Electron Devices Meeting (IEDM) 6.5.1–6.5.4 (IEEE, 2015).

10. Li, S. et al. Nanometre-thin indium tin oxide for advanced high-performance electronics. Nat. Mater. 18, 1091–1097 (2019).

11. Li, S., Gu, C., Li, X., Huang, R. & Wu, Y. 10-nm channel length indium–tin-oxide transistors with $I_{on} = 1.860 \mu A/\mu m$, $G_{max} = 50.50 \mu S/\mu m$ at $V_g = 1$ V with BEOL compatibility. In IEEE International Electron Devices Meeting (IEDM) 40.5.1–40.5.4 (IEEE, 2020).

12. Samanta, S. et al. Amorphous IGZO TFBTs featuring extremely-scaled channel thickness and 38 nm channel length: achieving record high $G_{on,max}$ of 1255 $\mu S/\mu m$ at $V_g = 1$ V and $I_{on}$ of 350 $\mu A/\mu m$. In 2020 IEEE Symposium on VLSI Technology 1–2 (IEEE, 2020).

13. Chakraborty, W. et al. BEOL compatible dual-gate ultra-thin body-W-doped indium oxide transistor with $I_{on} = 370 \mu A/\mu m$, $SS = 75 \mu V/dec$ and $I_{on}/I_{off}$ ratio $>4x10^4$. In 2020 IEEE Symposium on VLSI Technology 1–2 (IEEE, 2020).

14. Si, M. et al. Indium–tin-oxide transistors with one nanometer thick channel and ferroelectric gating. ACS Nano 14, 11542–11547 (2020).

15. Si, M., Lin, Z., Charnas, A. & Ye, P. D. Scaled atomic-layer-deposited oxide nanometer transistors with maximum drain current exceeding 2 A/mm at drain voltage of 0.7 V. IEEE Electron Device Lett. 42, 184–187 (2021).

16. Han, K. et al. First demonstration of oxide semiconductor nanowire transistors: a novel digital etch technique, IGZO channel, nanowire width down to ~20 nm, and $I_{on}$ exceeding 1.3 A/$\mu m$. In 2021 Symposium on VLSI Technology 1–2 (IEEE, 2021).

17. Si, M., Charnas, A., Lin, Z. & Ye, P. D. Enhancement-mode atomic-layer-deposited In$_2$O$_3$ transistors with maximum drain current of 2.2 A/mm at drain voltage of 0.7 V by low-temperature annealing and stability in hydrogen environment. IEEE Trans. Electron Devices 68, 1075–1080 (2021).

18. Charnas, A., Si, M., Lin, Z. & Ye, P. D. Enhancement-mode atomic-layer thin In$_2$O$_3$ transistors with maximum current exceeding 2 A/mm at drain voltage of 0.7 V enabled by oxygen plasma treatment. Appl. Phys. Lett. 118, 052107 (2021).

19. Si, M. et al. Why In$_2$O$_3$ can make 0.7 nm atomic layer thin transistors. Nano Lett. 21, 500–506 (2021).

20. Si, M., Lin, Z., Chen, Z. & Ye, P. D. First demonstration of atomic-layer-deposited BEOL-compatible In$_2$O$_3$ 3D fin transistors and integrated circuits: high mobility of 113 cm$^2$/V·s, maximum drain current of 2.5 mA/μm and maximum voltage gain of 38 V/V in In$_2$O$_3$ inverter. In 2021 Symposium on VLSI Technology 1–2 (IEEE, 2021).

21. Mourey, D. A., Zhao, D. A., Sun, J. & Jackson, T. N. Fast PEALD ZnO thin-film transistor circuits. IEEE Trans. Electron Devices 57, 530–540 (2010).

22. Kim, H. Y. et al. Low-temperature growth of indium oxide thin film by plasma-enhanced atomic layer deposition using liquid dimethyl[(N-ethoxy-2,2-dimethyloxypropanamido)indium for high-mobility thin film transistor application. ACS Appl. Mater. Interfaces 8, 26924–26931 (2016).

23. Ma, Q. et al. Atomic-layer-deposition of indium oxide nano-films for thin-film transistors. Nanoscale Res. Lett. 13, 4 (2018).

24. Lee, J. et al. High mobility ultra-thin crystalline indium oxide thin film transistor using atomic layer deposition. Appl. Phys. Lett. 113, 112102 (2018).

25. Robertson, J. & Clark, S. J. Limits to doping in oxides. Phys. Rev. B 83, 075205 (2011).

26. Kamiya, T., Nomura, K. & Hosono, H. Electronic structures above mobility edges in crystalline and amorphous In–Ga–Zn–O: percolation conduction examined by analytical model. J. Display Technol. 5, 462–467 (2009).

27. Schroder, D. K. Semiconductor Material and Device Characterization 3rd edn (Wiley, 2006).
Acknowledgements
This work was supported in part by the Semiconductor Research Corporation (SRC) nCore Innovative Materials and Processes for Accelerated Compute Technologies (IMPACT) Center and in part by the Air Force Office of Scientific Research (AFOSR) and SRC/Defense Advanced Research Projects Agency (DARPA) Joint University Microelectronics Program (JUMP) Applications and Systems-driven Center for Energy Efficient integrated Nano Technologies (ASCENT) Center.

Author contributions
P.D.Y. and M.S. conceived the idea and proposed the ALD In$_2$O$_3$ scaling research. M.S. developed the ALD process of In$_2$O$_3$ as a high-performance oxide semiconductor. M.S. and Z.L. performed the device fabrication, electrical measurement and analysis on thickness and EOT scaling of ALD In$_2$O$_3$ devices. Z.L. and M.S. conducted the channel length scaling of ALD In$_2$O$_3$ devices down to 8 nm. Z.C., X.S. and H.W. performed the STEM and EDX measurements. M.S. and P.D.Y. co-wrote the manuscript and all the authors commented on it.

Competing interests
The authors declare no competing interests.

Additional information
The online version contains supplementary material available at https://doi.org/10.1038/s41928-022-00718-w.

Correspondence and requests for materials should be addressed to Peide D. Ye.

Peer review information Nature Electronics thanks Seong Keun Kim and the other, anonymous, reviewer(s) for their contribution to the peer review of this work.

Reprints and permissions information is available at www.nature.com/reprints.

Publisher’s note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

© The Author(s), under exclusive licence to Springer Nature Limited 2022