Low Noise Amplifier Design for IoT Wireless Communication Systems

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Abstract. In the era of Internet of Things (IoT), the Internet has evolved from a simple Internet function of web information access to intelligent functions of identification, position, monitoring, and management of things. Devices in the IoT must transmit data between the devices and equipment connecting to cloud. As a fog computing architecture is established proximally at the local ends of the IoT, the data transmission volume and transmission delay can be effectively reduced. IoT wireless communication is one of the essential items for complete data transmission between the devices and on-line equipment. This paper proposes the low noise amplifier (LNA) design that can be applied to the RF front-end receiver of a 2.45-GHz wireless communication system for IoT applications. The LNA is required to have characteristics of low noise factor and high signal gain in order to amplify weak signals received by the antenna. In this study, the design of 2.45-GHz LNA adopts an architecture of power-constrained simultaneous noise and input matching on the basis of the 0.18-μm CMOS process technology in order to achieve simultaneous noise and input matching at low power conditions. Both the architectures of push-pull and forward substrate bias are also utilized. The LNA demonstrates the characteristics of low noise factor, high gain, and good 1-dB gain compression. The LNA shows good potential for IoT wireless communication system applications.

1. Introduction

The concept of a network of devices was discussed as early as 1982. A modified Coke vending machine at Carnegie Mellon University became the first Internet-connected appliance [1]. It was able to report its inventory and whether the newly loading drinks were cold or not [2]. Mark Weiser’s paper on ubiquitous computing, “The Computer of the 21st century” published in 1991, and academic venues suchlike UbiComp and PerCom brought out a contemporary vision for the Internet of Things (IoT) [3]. In 1999, the concept of “Internet of Things” became more popular through Auto-ID Center of Massachusetts institute of technology (MIT) [4]. Kevin Ashton, one of the founders of the Auto-ID Center, considered radio-frequency identification (RFID) [5-10] to be an essential element of the IoT [11]. RFID tags can be utilized to mark the unique identity of objects in daily life so that individual things are managed and inventoried.

In 2005, the International telecommunication union (ITU) published “ITU Internet Report 2005: IoT” at the world summit on the information society (WSIS), which pointed out the era of “IoT” coming. The ITU proposed to establish an application product architecture with RFID as the concept of the IoT [12]. The report also presented that objects can communicate and exchange information to server in the network environment with Internet-connected.
The concept of the IoT is an integrated sensing technology that can transmit sensed human bio-signals or actual physical signals in the environment to the Internet via wireless or wired communication networks for storage in the cloud. The IoT is a network of physical objects including but not limited to vehicles, buildings, equipment and health monitoring devices. This network utilizes electronic devices including sensors and actuators. In this way, the IoT can access the physical data of the objects in the physical world through the Internet, and thus can be monitored and operated remotely to improve the system optimization performance. The IoT may be further combined with the big data analysis in the cloud and even artificial intelligence, which can effectively transform data into services of multiple fields such as individuals, families, communities, cities, and factories, and realize applications such as smart health care, smart homes, smart cities, and smart factories [13-16].

In IoT applications, devices must transfer data between the devices and equipment connecting to the cloud. A fog computing architecture established at local ends of the IoT can effectively reduce the data transmission volume and delay. IoT wireless communication is one of the essential items for complete data transmission between the devices and on-line equipment. IoT wireless communication is one of the essential items for complete data transmission between the devices and on-line equipment. A low noise amplifier (LNA) [17] plays a significant role in the front-end circuit of the receiver. This is the first-stage active amplifier of the front-end circuit of the receiver. Fig. 1 shows the block diagram of the RF front-end receiver for IoT wireless communication systems. The LNA is required in the RF front-end receiver to amplify weak signals received by the antenna. Therefore, the LNA must have the characteristics of low noise factor and high signal gain.

With the advancement of semiconductor process technology, low power feasibility has increased. However, the LNA circuit architecture most commonly used is dominated by a cascode configuration of common source and common gate architecture. However, such a cascode configuration increases the difficulty of the implementation of low power circuits. Thus, some papers proposed other architectures, such as a folded architecture, to achieve circuit characteristics of low power consumption.

This paper proposes the LNA design that can be applied to the RF front-end receiver of a 2.45-GHz wireless communication systems for IoT applications. The LNA designed utilizes the integrated push-pull and forward substrate bias circuit architecture in this paper. The LNA circuit exhibits low DC power consumption and reasonable gain circuit characteristics.
2. Circuit architecture

2.1. Power-constrained simultaneous noise and input matching
In this paper, the LNA design employed a matching method of LNAs at low power. The matching method is
called power-constrained simultaneous noise and input matching [18] that can obtain simultaneous noise and
input matching at low power conditions. The circuit architecture is shown in Fig. 2. The input impedance can
be expressed as follows:

\[ Z_{in3} = sL_{s3} + \frac{1}{sC_{s3}} + \frac{g_{m3}L_{s3}}{C_{s3}} \]  \hspace{1cm} (1)

where \( C_{s3} \) is the sum of the parasitic capacitor \( C_{gs3} \) and the additional capacitor \( C_{ex3} \), \( g_{m3} \) is the
transconductance of \( M_3 \), and \( L_{s3} \) is the source degenerate inductor. Simultaneous noise and input matching
occurs by tuning \( L_{g3} \), \( C_{ex3} \), \( L_{s3} \), and other parameters until that \( Z_{s3} \) is equal to \( Z_{opt} \) and \( Z_{in3} \) is equal to the
conjugate of \( Z_{opt} \), i.e., \( Z_{s3} \) is the conjugate of \( Z_{in3} \).

Figure 2. Power-constrained simultaneous noise and input matching architecture.
2.2. Push-pull architecture

Fig. 3 shows a current-reuse push-pull architecture. Transistors $M_1$ and $M_2$ are NMOS and PMOS, respectively. Capacitor $C_1$, $C_2$, and $C_3$ are all used for DC-Blocking capacitors. With the same signal gain, the traditional push-pull architecture consumes only a half of the current consumption compared to the common source or common gate architecture. Because $M_1$ and $M_2$ are in the same loop, it is the technology of current reuse [19]. And the equivalent transconductance of the overall circuit can be expressed by the equation

\[ G_{m(total)} = G_{m(nmos)} + G_{m(pmox)} \] (2)

Therefore, the push-pull circuit architecture can still maintain the same gain at a lower current consumption, thereby contribute to the transconduction of the transistors $M_1$ and $M_2$.

2.3. Forward substrate bias architecture

Fig. 4 is the circuit architecture of the forward substrate bias. The threshold voltage $V_{th}$ is adjustable according to

\[ V_{th} = V_{th0} + \gamma (\sqrt{2\varphi_f} - V_{bs} - \sqrt{2\varphi_f}) \] (3)

$V_{bs}$, the voltage of the substrate to the source of the transistor, determines the threshold voltage of the MOS transistor, $V_{th}$. Usually, the substrate and the source of transistor are either connected or reverse biased. In this
study, the substrate and source of the transistor is applied with a forward bias in order to reduce the $V_{th}$ for the improvement of performance. It should be noted that, the first, the forward bias applied to substrate and source has to be biased below P-N junction turn-on voltage of the transistor. And the second, the CMOS process technology must include the deep N-well technology to reduce the noise transmitted through the substrate [20]. TSMC 0.18-μm CMOS process technology is utilized to meet the requirements. The architecture of the forward substrate bias is proposed to reduce the bias voltage and power consumption of the circuit.

2.4. Integrated push-pull and forward substrate bias circuit architecture

Fig. 5 shows the integrated push-pull and forward substrate bias circuit architecture utilized, which leads to the characteristics of low power consumption and reasonable gain. M3 and M4 are NMOS and PMOS, respectively. And C4, C5, and C6 are used for DC Blocking. The PMOS in the circuit reduces the $V_{th}$ in the same way as the NMOS does. This integrated push-pull and forward substrate bias circuit architecture reduces the bias voltage of the LNA to 1.2 V. At such a bias voltage, the LNA operating at 2.3 mA consumes a power of 2.76 mW. The results show that this circuit architecture can achieve low power consumption for the LNA.

3. Circuit characteristics

Agilent ADS and TSMC 0.18-μm CMOS process technology are used for the low power LNA design. Fig. 6 shows the gain characteristics of the designed LNA. At 2.45 GHz, the LNA has a gain of 11.46 dB. Fig. 7 shows the noise factor characteristics of the LNA. At 2.45 GHz, the LNA shows a noise figure of 2.78 dB. In the 2.4–2.485 GHz band, both the input reflection coefficient and the output reflection coefficient are below -10 dB.

![Figure 5. Integrated push-pull and forward substrate bias circuit architecture.](image-url)
4. Conclusion
This paper proposes an LNA circuit design that employs a power-constrained simultaneous noise and input matching method and an integrated push-pull and forward substrate bias circuit architecture for IoT wireless communication systems. The LNA operating at a DC bias of 1.2 V consumes a low power consumption and achieve good RF performance. At 2.45 GHz, the LNA shows the characteristics of 11.46-dB signal gain and 2.78-dB noise figure. The designed LNA demonstrates good performance for IoT wireless communication systems.

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