A General Scheme for Noise-Tolerant Logic Design Based on Probabilistic and DCVS Approaches

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Abstract—The performance of logic function could be affected significantly by the noise effect as the dimension of CMOS devices scales to nanometers. Thus, many pertinent researches about noise-tolerant logic gate have received growing attention. Considering the randomness as the noise’s nature, probabilistic-based approach proves better noise-immunity and three design schemes with the technique of Markov Random Field (MRF) have been proposed in [1]–[3]. In this paper, a general circuit scheme for noise-tolerant logic design based on MRF theory and Differential Cascade Voltage Switch (DCVS) technique has been proposed, which is an extension of the work in [3], [4].

A DCVS block with only four transistors has been successfully inserted to the original circuit scheme from [3] and extensive simulation results based on HSPICE show that our proposed design can operate correctly with the input signal of 1dB SNR. When using the Kullback-Leibler Distance (KLD) as the evaluation parameter, the KLD value of our design decreases by 76.5% on average than [3] which means that superior noise-immunity could be obtained through our work.

I. INTRODUCTION

Numerous performance improvements have been achieved due to the scaling down of CMOS devices in the past decades, but the problem caused by noise effect which may create fatal errors during the circuit operation become significant. Moreover, the decrease on supply voltage also deteriorates the noise-immunity of the circuit since the noise does not decrease proportionally with the supply voltage as explained in [6] and guardband voltage has to be utilized in order to keep the output correct. Thus, extensive pertinent researches about the noise-tolerant circuit design have received growing attention.

In traditional points of view, the Triple-Majority-Redundance (TMR) or Cascade TMR (CTMR) from [7], [8] is a direct idea where the original computation block is duplicated triple or more times and then a vote is made based on the majority results. However, the voter could be also contaminated by the noise and this makes it inappropriate to design noise-immunity circuit. The technique of Razor proposed in [9] has demonstrated big power reduction due to the non-conservative dynamic voltage scaling with the protective mechanism of error-rate monitoring and recovery, but this is a solution mainly focused on sequential logic level and has little effects on basic logic gate such as inverter or nand. In [10], [11], approximate computing is used to achieve more performance or energy-efficiency improvements with part of output precision losses, which can be applied to some fault tolerated designs such as multimedia, recognition or data mining processing, but the error is introduced intentionally by the circuit designers and the inherent noise could create serious erroneous output if the upper bits of the calculation results are not protected from noise impact.

Considering the randomness as the noise’s nature, the aforementioned methods are hard to achieve efficient circuit immunity. Thus, some new approaches have been proposed based on probabilistic theory. The Probabilistic CMOS (PCMOS) illustrated in [12] is an early attempt to exploit the random nature of the CMOS devices to obtain more design space, but the significant parts of the whole computation have to keep correct and further research of noise-immunity to the logic gate cannot be avoided in this work. Another probabilistic-based approach is proposed in [1]–[3] where the noise-immunity of the circuit is constructed by the Markov Random Field (MRF) theory. The MRF theory is developed in [13] and adopted in [1] to solve the problems of the noise impact in logic gate design. As pointed out in [1], the energy of noise signal could be reduced by maximizing the joint probability of the input-output pairs, which comes at a cost of redundant hardware. This work is further optimized in [2], [3] where parts of the gates in the original circuit scheme [1] are removed. In [4], the MRF approach is combined with the technique of Differential Cascade Voltage Switch (DCVS), however, this method only proposed an improved inverter to design xor-nxor gate.

In this paper, a general circuit scheme for noise-tolerant logic design based on MRF theory and DCVS technique has been proposed. A simple DCVS block with only four transistors has been successfully inserted to the Cost-Effective Noise-Tolerant Circuit based on Markov Random Field (CENT_MRF) in [3]. Extensive simulations have been implemented on HSPICE and the results show that our proposed design could operate correctly with the input signal of 1dB SNR. When using the Kullback-Leibler Distance (KLD) as the evaluation parameter, the KLD of our design decreases by 76.5% on average than [3] and superior noise-immunity is presented.

The remainder of the paper is organized as follows: Section 2 reviews the critical related works. Section 3 describes our proposed circuit scheme. Simulation results will be illustrated in Section 4. Finally, conclusions are drawn in section 5.
**II. PRELIMINARY WORKS**

In this section, some related work in [1]–[4] will be described. The original MRF theory will be illustrated first and then the process of mapping this theory into logic circuits [1] will be explained, along with the method to design cost-effective MRF circuit structure in [2]. At last, the work [3] will be explained, along with the method to design cost-effective MRF circuit structure in [2].

A. MRF Theory and Corresponding Logic Circuits

Let us define a network containing a set of variables $X = \{x_0, x_1, ..., x_k\}$ which are connected to each other in a certain mode as shown in Fig[1](a). Each variable $x_i$ can take different values from a specific set $\Omega$ (for example, in digital logic design $\Omega = \{0, 1\}$ and also has its neighborhood called $N_i$ (the set of the variables connected to $x_i$). A set of variable $x_i$ and its $N_i$ is called clique. With all of these definitions, $X$ is called a MRF if $\forall i, P(x_i) > 0$ and $P(x_i | \{X - x_i\}) = P(x_i | N_i)$ [13]. According to the MRF theory, the joint probability of $X$ : $P(x_1, x_2, ..., x_k)$ could be maximized if every clique has the lowest energy $U(x_i)$, which only depends all the variables in clique $c$. As pointed in [1], the combinational logic circuit could be mapped to this MRF graph as shown in Fig[1](b). Noise-immunity can be achieved through "valid minterm feedback loop" by which the logic gate network could be equipped with MRF property and the final correct logic state has lower energy than any other incorrect state (this means the correct output will get the highest probability). For example, in Fig[2](a), the conventional NAND-gate is mapped onto a MRF logic network [1] where the valid minterms $\{\overline{x_0}x_1x_2, \overline{x_0}x_1x_2, x_0\overline{x_1}x_2, x_0x_1\overline{x_2}\}$ are generated and feedback to input signals. This scheme has proved excellent noise-immunity since the final value of each node will tend to converge into the correct logic state due to its MRF property. However, this structure is inappropriate to be used in practical design as too many redundant gates are needed with this direct mapping method. Thus, in [2], this scheme is simplified and a master-and-slave cost effective MRF design is proposed as shown in Fig[2](b). The principles of this simplification are as followings: for the MRF NAND-gate in Fig[2](a), the energy function of this clique is the summation over all the valid minterms $\{\overline{x_0}\overline{x_1}x_2, \overline{x_0}x_1x_2, x_0\overline{x_1}x_2, x_0x_1\overline{x_2}\}$:

$$U(x_0, x_1, x_2) = -(\overline{x_0}\overline{x_1}x_2 + \overline{x_0}x_1x_2 + x_0\overline{x_1}\overline{x_2})$$

(1)

After applying the Boolean difference, the Eq[1] can be rewritten as

$$U(x_0, x_1, x_2) = -((\overline{x_0} + \overline{x_1})x_2 + (x_0x_1)\overline{x_2})$$

(2)

Based on Eq[2] the four valid minterms are merged into two terms $(\overline{x_0} + \overline{x_1})$ and $(x_0x_1)$. In Fig[2](b), these two terms are generated by AND gate and OR gate as the Master part, while the feedback loop connected to the output of Master part is called Slave. With this methodology, large amount of hardware redundancy will be removed as the transistors can be reduced from 60 to 28. The noise-immunity of this circuit scheme is worsen than [1] but very close as described in [2].

B. CENT_MRF in [3] and MRF Circuit with DCVS in [4]

In [3], the master-and-slave scheme for noise tolerant design from [2] is further simplified as the Eq[3] can be re-written:

$$U(x_0, x_1, x_2) = -(\overline{x_0} + \overline{x_1})x_2 + (x_0x_1)\overline{x_2})$$

$$= -(\overline{x_0}\overline{x_1}x_2 + (x_0x_1)\overline{x_2})$$

(3)

Thus, the master part in Fig[2](b) can be reconstructed with only one nand gate and an inverter as shown in Fig[3](a). Based on DeMorgan’s Law, the energy function of basic combinational logic gates can be expressed in a general form:

$$U(x_0, x_1, ..., x_k) = -(C_{function}(x_0, x_1, ..., x_k)x_{k+1} + C_{function}(x_0, x_1, ..., x_k)x_{k+1})$$

(4)

From Eq[4] a general scheme for Cost-Effective Noise-Tolerant Circuit based on MRF (CENT_MRF) is proposed in [3] as shown in Fig[3](b). Less transistors are needed in this scheme than [2] but the effect of noise-immunity is worsen than [2] due to the simplification.

Since the effect of noise-immunity from [2], [3] is worsen than the original design in [1] although numerous transistors have been removed, some compensations for the losing immunity are made in [4] by DCVS technique. However, this method only focused on inverter which is then applied to xor-xnor design and failed to build a general scheme. In next section, our proposed scheme will be described.
In this section, a DCVS block with four transistors has been inserted to the circuit in Fig.3(a) and then a general circuit scheme based on MRF and DCVS technique will be described.

A. Inserting DCVS Block into MRF-Based Circuit

The DCVS scheme shown in Fig.4 also have noise-immunity effect due to its differential operation. Thus, in order to make compensation for the losing immunity in [3], we insert the DCVS block into the circuit from Fig.3(a) which results an improved noise tolerant scheme as shown in Fig.5. The output of conventional NAND_Gate is pushed into the DCVS_Block along with its inverted signal, then the differential output are connected to the Feedback_Loop which results a mixed circuit scheme based on MRF graph and DCVS technique.

Due to this circuit structure, the effect of noise-immunity will be enhanced significantly as shown in Fig.6 Conventional nand-gate, CENT_MRF nand-gate from [3] and our proposed DCVS_MRF nand-gate are simulated with white gaussian noise, in which the SNR of the input signal is 3.5db. It can be seen that the output of conventional nand-gate is filled with serious disturbance and can hardly be used in logic computation. While the output of CENT_MRF nand-gate is much better and our proposed one is the best, from which it is well proved that the combination of DCVS and MPF approaches can produce enhanced noise-immunity and provide sufficient compensation to the previous design in [3].

B. General Scheme for DCVS_MRF Logic Circuit

With aforementioned analysis, the general scheme for CENT_MRF circuit in Fig.3(b) can be modified by inserting DCVS_Block as shown in Fig.7. The outputs of conventional logic gate $C_{function}$ are inverted by $inv$ and then pushed into the DCVS_Block with the original input signal. At last, the FeedbackLoop is connected to the DCVS_Block to construct a complete MRF graph.

![Fig. 4. Differential cascode voltage switch block.](image)

III. PROPOSED CIRCUIT SCHEME

For different logic designs, it only needs to replace the $C_{function}$. This methodology is different from [4] where only the inverter combined MRF and DCVS technique is applied to xor-nxor logic gate design. In our proposed design scheme, the $C_{function}$ in Fig.7 can be replaced by any basic logic gates or even some bigger logic blocks. But as pointed out in [1], [2], the effect of noise-immunity will be weakened if the $C_{function}$ has a big circuit scheme since the DCVS_Block and FeedbackLoop are not enough to eliminate the influence of the circuit noise.

IV. SIMULATION AND CORRESPONDING RESULTS

A. Introduction of Evaluation Parameter and Simulation Setup

To evaluate and prove the efficiency of the proposed circuit scheme, Kullback-Leibler distance(KLD) [5] is adopted to quantify the noise-immunity of conventional logic gate, CENT_MRF logic gate in [3] and our proposed one. In noise-tolerate circuit design, KLD can be used to quantify the difference of two signals based on Eq5 as described in [3] where $S_i$ means the output signal without any noise added to its input and $S_r$ means the output signal with a noisy input. $P_{i,0}$ means the probability of the output as logic "0" for no noise case and other parameters receive their corresponding meanings through its own subscript. From the Eq5, it can be seen that the difference of two signals will shrink if the value of KLD is getting smaller, which means that the effect of noise-immunity is stronger with a smaller KLD value.

$$KLD(S_i, S_r) = P_{r,0} \log_2 \frac{P_{i,0}}{P_{r,0}} + P_{r,1} \log_2 \frac{P_{i,1}}{P_{r,1}}$$  \hspace{1cm} (5)
TABLE I
TRANSISTOR NUMBER AND POWER CONSUMPTION

| Gate Type         | Transistor_Num | Power (µW) |
|-------------------|----------------|------------|
| CENT_MRF_inv [3]  | 12             | 0.316      |
| Proposed_inv      | 16             | 0.318      |
| CENT_MRF_nand [3] | 14             | 0.499      |
| Proposed_nand     | 18             | 0.497      |
| CENT_MRF_xor [3]  | 22             | 0.725      |
| Proposed_xor      | 26             | 0.721      |

nand and xor are listed. Compared to the gates in [3], our proposed noise-tolerated gates have few more transistors but the power consumption is quite close, which means that it is very reasonable to sacrifice little performance to get more efficiency of noise-immunity. Thus, our original purpose to make compensation for the losing immunity in [3] has been successfully achieved with little overhead.

V. CONCLUSION

In this paper, a general circuit scheme for noise-tolerant logic design based on MRF theory and Differential Cascode Voltage Switch (DCVS) technique has been proposed. Simulations results show that the KLD value of our design decreases by 76.5% on average than [3] which means that superior noise-immunity could be obtained with little overhead.

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