Error Rates and Resource Overheads of Repetition Cat Qubits

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We estimate and analyze the error rates and the resource overheads of the repetition cat qubit approach to universal and fault-tolerant quantum computation. The cat qubits stabilized by two-photon dissipation exhibit an extremely biased noise where the bit-flip error rate is exponentially suppressed with the mean number of photons. In a recent work [1], we suggested that the remaining phase-flip error channel could be suppressed using a 1D repetition code. Indeed, using only bias-preserving gates on the cat-qubits, it is possible to build a universal set of fault-tolerant logical gates at the level of the repetition cat qubit. In this paper, we perform Monte-Carlo simulations of all the circuits implementing the protected logical gates, using a circuit-level error model. Furthermore, we analyze two different approaches to implement a fault-tolerant Toffoli gate on repetition cat qubits. These numerical simulations indicate that very low logical error rates could be achieved with a reasonable resource overhead, and with parameters that are within the reach of near-term circuit QED experiments.

I. INTRODUCTION

The theory of quantum fault-tolerance [2–4] ensures that arbitrarily long quantum computations can be reliably performed on a noisy quantum hardware. However, this comes at the price of a tremendous hardware overhead, such that a big focus of the last few decades of research in quantum information theory has been to develop hardware-efficient protocols for universal and fault-tolerant quantum computation [5]. In a recent attempt to reduce this physical resource overhead, we proposed to encode quantum information in a 1D repetition code based on cat qubits [1]. In the large and actively studied family of bosonic quantum codes [6], the cat qubits’ specific encoding stands out by the remarkable property that any error process acting on the bosonic mode mostly produces phase-flip errors in the two-dimensional manifold defining the cat qubit. More rigorously, given an error process of the bosonic mode (say, photon loss) occurring at a rate $\kappa$, and a cat qubit parametrized by a complex amplitude $\alpha \in \mathbb{C}$ and a two-photon dissipation rate $\kappa_{2ph}$ larger than $\kappa$, the effective rate of resulting bit-flips acting on the cat qubit is suppressed exponentially in the average number of photons $\bar{n} = |\alpha|^2$, while the rate of phase-flips increases linearly [7].

Previous works have investigated how to leverage the noise bias of such qubits by adapting appropriately the error correcting codes in order to improve the overall performance of the scheme [8–11]. Here, we take one step further and anticipate that by increasing the average number of photons, the noise bias in the dissipative cat qubits can be made so important that the error suppression provided by the stabilizer code needs only to suppress the remaining dominant error. Indeed, the scaling of the resulting error rates for the encoded cat qubit is somewhat similar to the protection achieved by a 1D repetition code protecting against bit-flips, where the role of the distance $d$ of the code is now played by the average number of photons $\bar{n}$. Interestingly, this inner code ‘distance’ can be augmented without increasing the number of physical quantum systems. In the spirit of Bacon-Shor codes [2, 12], the full protection of the quantum bit of information is achieved by embedding the cat qubit into a dual repetition code protecting against phase-flips, the so-called repetition cat qubit.

Because the family of Bacon-Shor codes does not possess an accuracy threshold, these codes cannot be used alone to achieve arbitrarily low error rates. Rather, in many constructions, a large block of these codes is used at the bottom level to obtain very low logical error rates. Then, to reach arbitrarily low logical error rates, the code needs to be concatenated with any other code possessing a threshold [13, 14]. The interest of using a Bacon-Shor code at the bottom level, in these constructions, is usually that it reduces the overall resource overhead, or to gain access to new logical operations.

However, even without a threshold, it has been shown that a single block of Bacon-Shor code used without concatenation could achieve extremely low error rates at the cost of a reasonable resource overhead [13, 15, 16]. For this reason, Bacon-Shor codes and related constructions are promising candidates for near-term experimental demonstration of quantum error correction and fault-tolerant processing of encoded quantum information. As we will see in this paper, the repetition cat qubit approach is similar: even though strict fault-tolerance requires concatenating the repetition cat qubit with a code that possesses an accuracy threshold, a large enough repetition cat qubit alone already yields extremely low logical error rates with a reasonable resource overhead. This level of protection should allow us to perform useful quantum computations without resorting to code concatenation.

The rigorous characterization of the performance of a given architecture is a tricky task. The obtained performance is highly dependent on the underlying assumptions made about the noise structure, the quantum computer’s architecture, and the types of gates that are con-
sidered. In this paper, we rely on a circuit-based error model for the simulations of the operations in our universal set, both Clifford and non-Clifford. These simulations provide realistic estimates of the expected logical error rates and resource overheads, using physical parameters that are within the reach of the circuit QED experiments in the next few years.

The paper is structured as follows. We recall the repetition cat qubit approach to universal and fault-tolerant quantum computation in Section II. The methodology and the assumptions used to derive the error rates and overhead are discussed in Section III. In Section IV, we estimate the error rate and resource overhead of a repetition cat qubit used as a quantum memory, and of the logical gadgets that admit a transversal construction. We then discuss in Section V the implementation of the non-Clifford resource needed for universality: the Toffoli gate, and give estimation of its performance. In Section VI, we start a discussion around the question of architecture of a quantum processor based on repetition cat qubits. The intention of this discussion is to suggest a few possible research directions rather than providing a final and optimal solution.

II. REPETITION CAT QUBITS FOR FAULT-TOLERANT QUANTUM COMPUTATION

This section summarizes the key results of [1]. The starting point of the approach is the two-photon driven dissipative process that stabilizes cat qubits, and provides an autonomous protection against bit-flips. The suppression of the remaining phase-flip errors is achieved with a 1D repetition code. Then, we recall the set of gates or operations acting on the cat qubit that are compatible with the exponential suppression of bit-flip errors. The operations in this set are combined to design gadgets acting as logical gates on the repetition cat qubit.

A complete theoretical presentation of the two-photon pumped cat qubits can be found in [17], and experimental demonstrations of this proposal in [7, 18, 19]. The two-photon driven dissipative process consists in applying a photon driven dissipative process consists in applying a mode that can only exchange photons in pairs with its environment at a rate \( \kappa_{2ph} \). The Lindblad master equation describing this dynamics is:

\[
\frac{d\rho}{dt} = [\epsilon_{2ph}\hat{a}^\dagger - \epsilon_{2ph}\hat{a}^2, \rho] + \kappa_{2ph} D[\hat{a}^2 \rho] = \kappa_{2ph} D[\hat{a}^2 - \alpha^2] \rho
\]

where

\[
D[\hat{L}] \rho = \hat{L} \rho \hat{L}^\dagger - \frac{1}{2} \hat{L}^\dagger \hat{L} \rho - \frac{1}{2} \rho \hat{L}^\dagger \hat{L}
\]

and \( \alpha = \sqrt{2\epsilon_{2ph}/\kappa_{2ph}} \). This dynamics stabilizes the two-dimensional manifold spanned by the coherent states \( |\alpha\rangle \) and \( |-\alpha\rangle \), or equivalently, by the coherent superpositions of these states, known as Schrödinger cat states:

\[
|C_+^\pm\rangle := N_{\pm}(|\alpha\rangle \pm |-\alpha\rangle)
\]

where \( N_{\pm} = (2(1 + \exp(-2|\alpha|^2))^{-1/2} \) is a normalization factor. Following the convention of [1, 2], the cat states \( |C_+^\pm\rangle \) are chosen to be the \pm 1 eigenvectors of the Pauli X operator for the cat qubit, and the computational basis is defined as:

\[
|0\rangle_c = (|C_+^+\rangle + |C_+^-\rangle)/\sqrt{2} = |\alpha\rangle + \mathcal{O}(e^{-2|\alpha|^2}),
\]

\[
|1\rangle_c = (|C_+^-\rangle - |C_+^+\rangle)/\sqrt{2} = |-\alpha\rangle + \mathcal{O}(e^{-2|\alpha|^2}).
\]

The non-locality of information in the phase space ensures an exponential suppression of bit-flips with the cat size \( |\alpha|^2 \). This raises the hope that a simple quantum error correcting code correcting phase-flips only could be sufficient to achieve fault-tolerance. The simplest choice is a repetition code in the dual basis. The fully protected logical qubit obtained is called the repetition cat qubit. For a distance \( d \) code encoding one repetition cat qubit into \( d \) cat qubits, the \( d - 1 \) stabilizers are \( X_iX_{i+1}, i \in [0, d-1] \) and the logical Pauli operators are \( X_L = X_k \) \( (k \in [0, d-1]) \), \( Z_L = |\ominus\rangle \otimes Z_i \), and \( Y_L = iZ_LX_L \).

We now describe how operations can be performed on a cat qubit. The manipulation of the quantum information encoded in the cat qubit requires special care to preserve the noise structure. More precisely, to carry through the exponential suppression of the bit-flip error rate, any operation performed on the cat qubit has to be bias-preserving, which means two things: it must not convert a phase-flip error into a bit-flip error, and it must preserve the exponential suppression of bit-flips while the operation is being performed. Note that the first requirement automatically rules out certain gates, such as the Hadamard gate \( H = (X+Z)/\sqrt{2} \) (not allowed because \( HZ = XH \)). The second requirement is satisfied if the non-locality of the information in the phase space is maintained during the execution of the gate. More precisely, given a unitary \( U \) on the cat qubit implemented by the dynamics \( \dot{\rho} = \mathcal{L}(\rho) \) in time \( T \), \( (U = e^{T\mathcal{L}}) \), the noise bias is preserved during the execution of the gate \( U \), if the two states \( e^{T\mathcal{L}}(|\pm \alpha\rangle) \) remain distant in the phase space for all times \( t \in [0, T] \).

Fortunately, an important class of operations can be performed in this way. This class includes the preparation of the eigenstates \( |\pm \rangle_c \) of Pauli operator \( X \) (noted as \( \mathcal{P}_{\pm} \)), the measurement of the observable \( X \) (noted as \( \mathcal{M}_X \)), single qubit \( X \) logical gate, rotation of an arbitrary angle \( \theta \) around the \( Z \) axis \( Z(\theta) = \exp(-i\theta Z) \), two-qubit controlled-\( X \)-gate (also called CNOT and denoted CX) and the controlled-\( Z(\theta) \)-gate, and finally the three-qubit controlled-controlled-\( X \)-gate (also called Toffoli and denoted CCX). Performing a CNOT or a Toffoli gate with a bias-preserving process is non trivial. The extra degree of freedom associated with the choice of the complex parameter \( \alpha \) defining the cat qubit plays a crucial role in the design of bias-preserving processes: more precisely, it has been shown that for a conventional two-level system, the CNOT or Toffoli gates cannot be implemented in a bias-preserving manner [11]. For this reason, in previous work on quantum computation with biased-noise qubits [8], these gates were usually discarded. To clarify the important role of the underlying Hilbert space of...
the harmonic oscillator in the bias-preserving implementations of gates, we recall how the X gate and the CNOT gate are realized on cat qubits. The physical realizations of the other above operations are described in [1].

The X gate, swapping the states $|0\rangle_c \approx |\alpha\rangle$ and $|1\rangle_c \approx |\alpha\rangle$, is realized in time $T$ by adiabatically modulating the phase of the two photon drive $c_{2ph} \rightarrow c_{2ph}\exp^{2i\alpha t}$, effectively transforming the two-photon dissipator $\mathcal{D}[\hat{a}^2 - \alpha^2]$ to $\mathcal{D}[\hat{a}^2 - (\alpha e^{i\pi t})^2]$. The instantaneous eigenstates of this time-dependent superoperator are $|\pm \alpha e^{i\pi t}\rangle$, taking an initial state $|\psi(t=0)\rangle = c_0|\alpha\rangle + c_1|\alpha\rangle$ to the state $|\psi(t)\rangle = c_0(\alpha e^{i\pi t}) + c_1(-\alpha e^{i\pi t})$ after a time $t$, resulting in a final state $|\psi(t=T)\rangle = c_0|\alpha\rangle + c_1|\alpha\rangle = X|\psi(t=0)\rangle$.

In order to extend the above single-qubit X gate to a two-qubit controlled-X gate, we must perform the continuous evolution of the dissipator $\mathcal{D}[\hat{a}^2 - (\alpha e^{i\pi t})^2]$ on the target cat qubit (stabilized in the mode $\hat{a}$) only when the control cat qubit (in the mode $\hat{b}$) is in the state $|\alpha\rangle$. Otherwise, the dissipator $\mathcal{D}[\hat{a}^2 - \alpha^2]$ needs to be retained. This can be done through the time-dependent dissipator $\mathcal{D}[\hat{a}^2 - \frac{1}{2}\alpha(\hat{b} + \alpha) + \frac{1}{2}\alpha e^{2i\pi t}(\hat{b} - \alpha)]$ and the constant one $\mathcal{D}[\hat{b}^2 - \alpha^2]$. During the dynamics the instantaneous steady states of the dissipators remain distant in the 4D phase space of the two harmonic oscillators and therefore the exponential bit-flip suppression is maintained. Some amount of phase-flip errors is induced by the finite adiabaticity of the gate. As shown in [1], these non-adiabatic effects can be reduced by using a feed-forward Hamiltonian

$$H = \frac{\pi}{2T} \frac{(a - \alpha)}{2\alpha} \otimes (b^\dagger b - |\alpha|^2) + h.c.$$ 

In presence of the above dissipators and feed-forward Hamiltonian, increasing the gate time $T$ further reduces the phase-flip error probability due to non-adiabatic effects but increases the probability that they are induced by other noise channels such as single photon loss. The gate time $T^*$ that maximizes the CNOT fidelity in presence of single photon loss (occurring at a rate $\kappa_{1ph}$) is given by $T^* = (2\sqrt{\pi})^{-1} \sqrt{1/\kappa_{1ph}\kappa_{2ph}}$ [1].

Before attempting to build logical operations on the repetition cat qubit, an important issue is whether the stabilizers can be measured in a bias-preserving manner. A standard circuit used to perform a quantum non demolition measurement of the stabilizers of a repetition code is depicted in Fig. 1. Since every operation in this circuit can be done in a bias-preserving manner, the circuit itself is bias-preserving. There are other protocols that could equivalently be used for the same purpose, see e.g. [20].

III. ASSUMPTIONS AND METHODOLOGY

A. Assumptions

The repetition cat qubit approach to universal and fault-tolerant quantum computation relies on two different kinds of protection. The two-photon dissipation exponentially suppresses bit-flip errors with the mean number of photons in the cat state, while the rate of phase-flip errors increases only linearly. Next, the repetition code suppresses exponentially the phase-flip errors, provided that the phase-flip error rate of the cat qubit is below the fault-tolerance threshold of the repetition code.

This protection is similar to the one achieved by Bacon-Shor codes [2] [12], with the nice feature that the “distance” of the inner protection provided by the two-photon pumping can be increased without any further hardware overhead. However, similarly to Bacon-Shor codes, because the phase-flip error rate of the cat qubit increases linearly with the mean number of photon, there cannot be a threshold since the effective phase-flip error rate of the cat qubit will eventually exceed the threshold of the repetition code. Nonetheless, this is not an obstacle to obtaining extremely low logical error rates with this approach, by limiting the mean number of photons to a finite value for which the bit-flip error probability is extremely low, and for which the phase-flip error probability is still below the threshold of the repetition code. In our analysis, we limit the size of the cat qubits to $\bar{n} = 10$ photons and assume that the exponential suppression of the bit-flip error rate holds at least up to this cat size.

All the circuits presented in this work are built to implement logical gates on repetition cat qubits, while being fault-tolerant to phase-flip errors only. Indeed, any single bit-flip error occurring on any data qubit during the execution of a circuit can cause a logical bit-flip error. The resulting logical bit-flip error rate can therefore be bounded by simply counting the number of single locations in the circuits where a bit-flip can occur. The numerical simulations of the logical circuits is devoted to estimating the logical phase-flip error rate only, without taking into account the bit-flip errors. For fault-tolerant circuits with respect to phase-flip errors, we define the “phase-flip threshold” to be the highest value of the physical phase-flip error probability $p_{ph}$ for which the logical phase-flip error probability decreases upon an increase of the code distance $d$. 

\begin{figure}[h]
\centering
\includegraphics[width=0.2\textwidth]{fig1}
\caption{Quantum circuit to measure a $X_1 \otimes X_2$ stabilizer of the repetition code (top two qubits). Every operation in this circuit can be done in a bias-preserving manner.}
\end{figure}
FIG. 2. Quantum error correction for a repetition cat qubit used as a quantum memory (here the code distance $d = 3$). The $d - 1$ stabilizers are measured $d$ times, and the measurement results are used in a MWPM decoder. The red stars mark the possible locations of errors.

B. Fault-tolerant simulation of a quantum circuit

The logical error probability of the different logical gates in our universal gate set are numerically estimated by performing Monte Carlo simulations of the circuits implementing these gates. We consider a circuit-based error model which takes into account errors of all operations in the circuit, including identity for the idle qubits. This is a more realistic model than the so-called phenomenological error model as it takes into account the errors of all operations in the circuit, and is best suited for estimating the logical error rate in the context of quantum computation.

The error models for various physical operations of Fig. 2 are provided in [1] and summarized in Table I. While the bit-flip error probability remains exponentially suppressed in $\bar{n}$, applying a noisy CNOT gate, for instance, consists in applying a perfect CNOT gate, followed by a probabilistic application of either identity with probability $1 - 4p$, or a $Z$ error on the control qubit with probability $3p$, or a $Z$ error on the target qubit with probability $p/2$, or a correlated $Z$ error on both qubits with probability $p/2$. Here the parameter $p$ is given by $\bar{n}\kappa_{1\text{ph}}T$ which for the optimal gate time $T^*$ is given by

$$p = (2\sqrt{\pi})^{-1}\sqrt{\kappa_{1\text{ph}}/\kappa_{2\text{ph}}}.$$  \hspace{1cm} (2)

Each circuit is divided into time-steps, where every qubit (both data and ancilla) in the circuit is acted upon at every time step. For simplicity, we fix the duration of these time-steps to be the same as $T$, the duration of CNOT and Toffoli gates. When a qubit is acted upon by a gate at a given time-step, the applied probabilistic error is drawn from the corresponding error model, otherwise, the error is drawn from the identity error model (which corresponds to a phase-flip probability of $p = \bar{n}\kappa_{1\text{ph}}T$).

In order to simulate a given circuit, we fix the code distance $d$ and the value of the physical noise strength $p$ and run the noisy circuit $N$ times. For each trajectory, the output of the syndrome measurements is decoded using a minimum weight perfect matching (MWPM) decoder and a final perfect recovery operation [21]. After the recovery operation, mapping the state back to the codespace, we check whether a logical error has occurred. We then define the logical error probability of the circuit $p_L(d, p)$ as

$$p_L = \frac{N_{\text{fail}}}{N},$$

where $N_{\text{fail}}$ is the number of times a logical error occurred during the $N$ runs. All the circuits simulated in this work are run continuously until at least $N_{\text{fail}} = 500$ logical failures are observed, which ensures that the relative error on $p_L$ is less than 9% with probability 95%. The decoding step is computed efficiently using Dijkstra’s shortest path algorithm [22] to generate the graph of detection events and the minimum weight perfect matching algorithm to match these events [23, 24]. The simulations of the non-Clifford circuits of Section V are slightly more complicated. In general, classical simulations of non-Clifford circuits become rapidly intractable with large distances $d$. However, the particular structure of the circuit and the bias-preserving property of the physical gates makes it possible to efficiently simulate the propagation of errors throughout the circuit. More precisely, the Pauli phase-flip errors either remain Pauli or propagate to a Clifford CZ type error which commutes with the rest of the circuit, up until a point where it meets a measurement that eventually projects it. Importantly, the errors can never propagate to non-Clifford errors. This feature, which is particular to our circuits and error models, is not true in all generality for random non-Clifford circuits, but allows us to numerically simulate the logical error probability for our non-Clifford circuits using only the CHP algorithm introduced in [25]. We refer the reader interested in these implementation considerations to the Appendix. The numerical computations were performed in parallel using the cluster of Inria Paris, composed of 68 nodes.
for a total of 1244 cores. The nodes are divided in a few hardware generations: 28 bi-processors Intel Xeon X5650 of 6 cores, 12 bi-processors E5-2650v4 2.20 of 12 cores, 16 bi-processors XeonE5-2670 of 10 cores, 8 bi-processors E5-2695 v4 of 18 cores, 4 bi-processors E5-2695 v3 of 14 cores. Some data points for the logical Toffoli circuits corresponding to the largest distances and lowest logical error probabilities, for which $\sim 10^8 - 10^9$ trajectories were simulated per point, required up to a week (real time) of computation.

IV. MEMORY AND TRANSVERSAL CLIFFORD OPERATIONS: PERFORMANCE

A. Repetition cat qubit as a quantum memory

In this subsection, we investigate the performance of a repetition cat qubit used as a quantum memory. The QEC is applied to extend the lifetime of a quantum bit of information. In this case, the logical circuit (implementing the logical encoded version of identity operation) simply consists of the error correction step. The $d-1$ stabilizer operators are measured using $d-1$ ancilla qubits. To make the procedure fault-tolerant, the measurements are repeated $d$ times before they are decoded with a MWPM decoder. Since all the operations are bias-preserving and do not convert $X$ and $Z$ errors, we can separately estimate the error probabilities $p_{Z_L}$ and $p_{X_L}$ of logical $Z_L$ and $X_L$ errors occurring per cycle of error correction. Then, the logical error probability is bounded by $p_L = p_{Z_L} + p_{X_L}$.

a. Logical X error probability $p_{X_L}$ The repetition code does not provide any protection against bit-flip errors. Hence, a single bit-flip occurring on any qubit during the execution of the circuit will cause a logical $X_L$ error. The probability that a bit-flip occurs on a given cat qubit during a single time step $T$ is given by $p_X = \kappa_{\text{eff}}(\bar{\alpha}^2, \delta)^T$ where $\kappa_{\text{eff}}(\bar{\alpha}^2, \delta)$ is the effective bit-flip rate $\bar{\alpha} \leftrightarrow | - \bar{\alpha} \rangle$ induced by photon loss at rate $\kappa_{\text{ph}} = \delta_{2\text{ph}}$.

As recently observed in [7], this effective bit-flip rate is exponentially suppressed with the mean number of photons in the cat state $\bar{\alpha}$. In this paper, the bit-flip rate $\kappa_{\text{eff}}(\bar{\alpha}, \delta)$ is numerically estimated by simulating the master equation,

$$\frac{d\rho}{dt} = \kappa_{2\text{ph}}\mathcal{D}[\bar{\alpha}^2 - \bar{\alpha}^2]\rho + \kappa_{1\text{ph}}\mathcal{D}[\bar{\alpha}]\rho.$$ 

These numerical simulations, plotted in the inset of Fig. 4 indicate that $\kappa_{\text{eff}}(\bar{\alpha}, \delta) \propto e^{-c(|\bar{\alpha}|, \delta)|\bar{\alpha}|^2},$ where $c(|\bar{\alpha}|, \delta)$ varies between 2 and 4. Indeed, for small enough $\delta$, and for $|\bar{\alpha}|$ not too large, the exponential suppression occurs at a rate close to $e^{-4|\bar{\alpha}|^2}$. This suppression rate then converges to $e^{-2|\bar{\alpha}|^2}$ for larger values of $|\bar{\alpha}|$.

Including the ancilla qubits, there are $4d^2 + d(d-1)$ locations in the QEC circuit of Fig. 2 where a single physical $X$ error can result in a logical $X_L$ error. Assuming $p_X$ is very small, the resulting logical error probability is simply given by

$$p_{X_L} = [4d^2 + d(d-1)]p_X = [4d^2 + d(d-1)]\kappa_{\text{eff}}(|\bar{\alpha}|^2, \delta)T.$$ 

b. Logical Z error probability $p_{Z_L}$ To estimate $p_{Z_L}$, we perform Monte Carlo simulations of the QEC circuit depicted in Fig. 2 where we neglect physical $X$ errors. Here and in the following simulations, we assume that the classical processing of the measurement outcomes is instantaneous, so no errors are induced on the data qubits while the decoding is performed. In the memory case, we also assume the correction step is perfect, because in this case the correction does not need to be physically applied but rather can be performed in software by updating the Pauli frame [20].

For each run, the repetition cat qubit is initialized in a codeword $|\psi_{\text{in}}\rangle_L$. The stabilizers of the code are measured $d$ times as depicted in Fig. 3. A last round of perfect stabilizer measurements is performed and the history of measurement outcomes is decoded together with this last perfect measurement outcome. This ensures that, after the perfect correction, the output state $|\psi_{\text{out}}\rangle_L$ is back in the code space, either $|\psi_{\text{out}}\rangle_L = |\psi_{\text{in}}\rangle_L$ in which case the error correction was successful, or a $Z_L$ error occurred, $|\psi_{\text{out}}\rangle_L = Z_L|\psi_{\text{in}}\rangle_L$. We plot in Fig. 3 the probability $Z_L$ that a logical error occurred for various code distances $d$ and values of the physical noise strength $p$. The phase-flip threshold for this circuit is $p_{\text{ph}} = 1.9\%$, which, according to the equation (2), corresponds to a ratio between the two-photon dissipation rate and a single photon loss rate $\kappa_{2\text{ph}}/\kappa_{1\text{ph}} = 220$, close to the value achieved in [19]. For a typical cavity lifetime of 1ms and Figure 3. Probability that the error correction circuit of Fig. 2 induces a logical $Z_L$ error on the repetition cat qubit after the correction is performed. The dotted lines correspond to the asymptotic regime and fit the empirical scaling formula $p_{Z_L} = A(\frac{p_{\text{ph}}}{p_{\text{in}}})^\frac{1}{d}$. 

FIG. 3. Probability that the error correction circuit of Fig. 2 induces a logical $Z_L$ error on the repetition cat qubit after the correction is performed. The dotted lines correspond to the asymptotic regime and fit the empirical scaling formula $p_{Z_L} = A(\frac{p_{\text{ph}}}{p_{\text{in}}})^\frac{1}{d}$.
TABLE I. Error models of each gate used in the simulations. Every noisy gate is modeled as a perfect gate, followed by a stochastic error. For each gate, we summarize the Z-type errors and the corresponding probability that we have used in the Monte Carlo simulations. We also assume the ancilla measurement to be faulty with probability $p$. These error models account for non-adiabatic errors and for the effect of single photon loss at rate $\kappa_1 ph$. The parameter $p$ that characterizes the “strength” of the physical error is the error probability of a physical phase-flip during the typical gate time $T$, given by $p = \bar{n}\kappa_1 ph/T$. For the gate time $T$ that maximizes the CNOT and Toffoli gate fidelities, this probability is given by $p = \frac{1}{2}\sqrt{\kappa_1 ph/\kappa_2 ph}$. For simplicity sake, we assume that all the gate times are equal.

| I | Error Probability | $p$ | | $P_{\text{I}Z}$ | Error Probability | $p$ | | $Z$ | Error Probability | $p$ | | $\text{CZ}$ | Error Probability | $p$ | | $\text{CNOT}$ | Error Probability | $p$ | | Toffoli | Error Probability | $p$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| I | $1 - p$ | | | $1 - p$ | | | $1 - p$ | | | $1 - 2p$ | | | $1 - 4p$ | | | $1 - 6p$ | |
| Z | $p$ | | | $Z_1$ | $3p$ | | $Z_2$ | $p/2$ | | $Z_1Z_2$ | $p/2$ | | $CZ_{12}$ | $3p$ | | $CZ_{12}Z_3$ | $p/2$ |

FIG. 4. Estimated number of cat qubits per repetition cat qubit used as a quantum memory, versus the physical noise probability $p$, also given in units of the phase-flip threshold value $p_{\text{th}}$. The different plots correspond to different values of the target logical error probability per QEC cycle, and the numbers on the curves correspond to the mean number of photons $\bar{n} = |\alpha|^2$ in the cat qubits. Inset: Effective bit-flip rate $\kappa_{\text{eff}}(\bar{n}, \delta)$ induced by single photon loss at rate $\kappa_1 ph$ vs. the mean number of photons $\bar{n}$. The different colors correspond to different values of the physical error probability $p$. The two black plain lines are proportional to $e^{-26}$ (top) and $e^{-40}$ (bottom).

cat qubits of size $\bar{n} = 10$ photons, this phase-flip threshold of $1.9\%$ corresponds to a CNOT gate time of about $2\mu$s. It is experimentally reasonable to think that all the other operations can be performed as fast.

Note that the phase-flip threshold for the CNOT error probability is about $92\%$ (see II and Table I). For a depolarizing model where idle qubits, state preparation and measurement, and the CNOT gate all fail with probability $p$, and where the CNOT error model is balanced $p_{Z_1} = p_{Z_2} = p_{Z_1Z_2} = p/3$, the fault-tolerance threshold is slightly above $3\%$ [27], which corresponds to a CNOT error probability around $97\%$. In our case, a higher gate error probability is tolerated because the phase-flips errors of the CNOT mostly occur on the ancilla cat qubits used for the stabilizer measurement.

c. Logical error rate and resource overhead Combining the logical $X_L$ and $Z_L$ errors, we estimate the minimum number of data cat qubits and the minimum number of photons per cat qubit to achieve a target logical error rate $p_L$ for a quantum memory. In Fig. 4 we present this physical overhead as a function of the physical error probability $p$. Quite remarkably, with physical error probabilities of about $1\%$ (corresponding to a CNOT fidelity of $96\%$), very low logical error probabilities of order $10^{-10}$ per QEC cycle can be achieved for a modest number of $70$ modes per repetition cat qubit (twice as much including the ancillary modes) and for experimentally reasonable cat sizes of about $6$ photons. Furthermore, with the specific gate realizations of [1], this physical error probability of $1\%$ can for instance be achieved with a two-photon dissipation rate of $125kHz$, a cavity mode lifetime of about $1$ms and a gate time of about $1.7\mu$s. These numbers indicate that using a repetition cat qubit as a quantum memory is a promising approach to build a long-lived quantum memory in near term experiments.

B. Transversal gates

All logical operations that admit a transversal implementation exhibit a similar performance to the quantum memory. This includes the measurement of $X_L$, the preparation of the logical $|\pm\rangle_L$ states, and the logical CNOT gate. The measurement of the $X_L$ operator is done by measuring all the cat qubits in the $X$ basis, followed by a majority vote on the measurement outcomes. The fault-tolerant preparation of the state $|\pm\rangle_L$ consists in preparing all the cat qubits in the $|+\rangle$ state, and performing a full round of error correction as in Fig. 2. The phase-flip threshold for this preparation is therefore the same as the quantum memory. The logical CNOT gate is
implemented on the codespace by performing a physical CNOT gate between each pair of cat qubits of different logical codeblocks, followed by a separate round of error correction on each logical block. As it can be seen from Fig. 5 the error probability of a logical CNOT gate is similar to that of a quantum memory.

As shown in 1, the set of fault-tolerant gates that can be used to perform universal quantum computation using repetition cat qubits is \( S_L = \{ |\pm \rangle_L, X_L, X_L, CNOT_L, Toffoli_L \} \). In this section we showed that all these gates except the logical Toffoli can be implemented with very high fidelities for modest code sizes. In the next section, we investigate the performance of this non-Clifford gate.

V. NON-CLIFFORD OPERATION: THE TOFFOLI GATE

The Eastin-Knill theorem [28] establishes that a set of transversal logical gates cannot be universal for quantum computation. For many quantum codes, the encoded version of the gates in the Clifford group can be implemented transversally on the code, which, by virtue of the Eastin-Knill theorem, prevents non-Clifford gates to be implemented transversally. The fault-tolerant but not transversal construction of a non-Clifford gate is possible but is usually much more expensive in terms of physical resources than the transversal gates. Thus, most of the focus of such constructions has been devoted to find the most efficient strategies to reduce the associated overhead. A long standing leading strategy inspired from gate teleportation techniques [29] is to prepare encoded versions of magic states and to consume these states as a non-Clifford resource during the computation [30]. The cost of these techniques, initially very expensive in terms of hardware resources, have been greatly reduced thanks to many years of active research [31-38]. In order to avoid magic state distillation and the costly overhead associated with it, a second approach relies on subsystems codes, for which the encoding can be deformed in such a way that the information remains protected from errors but the set of allowed transversal gates changes. This approach includes the “gauge color codes” [39-42] and other code-switching techniques [43]. Along the same lines, a recent proposal proposed to use code deformation techniques to directly implement a fault-tolerant non-Clifford gate on the surface code [44]. A third approach is to combine different codes that have different transversal gate sets using concatenation, to achieve universality in a larger code [45]. Other strategies focus on circuits that are not transversal, yet can still be made fault-tolerant, such as the pieceable fault-tolerant EC where intermediate rounds of error correction are added in well chosen locations of the circuit [46-47], or the flag fault-tolerant EC where additional “flag” ancilla qubits are used to gain more information about the propagating errors [48-49].

In this work, we build on the logical Toffoli gate construction proposed in 1 and investigate two different strategies for fault-tolerance. The first strategy consists in studying the performance of the circuit depicted in Fig. 7. As explained in 1, the intermediate EC in this circuit ensures that the errors do not propagate in an uncontrolled manner. However, in order to ensure the fault-tolerance, one also needs to prevent an accumulation of non-propagating errors in the first and second blocks. As soon as the logical error probability of the Toffoli circuit becomes lower than that of a physical Toffoli gate, the circuit can be made fault-tolerant by using concatenation [40]. The idea of code concatenation is to build a hierarchy of codes within codes iteratively, by replacing all the physical gates in a logical circuit by their logical versions (see e.g [50]). We argue in Subsection VA that with experimentally reasonable physical error rates, the logical error rate of the Toffoli circuits is well below that of the logical one; thus making it possible to use code concatenation.

In Subsection VB we study a second strategy that avoids concatenation and achieves a higher phase-flip threshold and an improved scaling, but comes at the expense of a more complex error correction circuit based on three ingredients. First, the accumulation of non-propagating errors is prevented using the pieceable fault-tolerant protocol described in 1 [46]. Second, this pieceable fault-tolerant protocol requires the measurement of the stabilizers of the code in the middle of the logical Toffoli circuit, at a point where these stabilizers are no longer Pauli operators, but have evolved to Clifford operators under the action of the non-Clifford pieces of the Toffoli circuit. Last, we use a Steane-style error detection [51] decoded with a majority vote on the target block instead of the usual stabilizer measurements decoded with
the MWPM decoder used everywhere else in this work. For the sake of completeness, we recall the Steane QEC procedure. A logical ancilla qubit is prepared in the state $|0\rangle_L$, and logical CNOT is applied between the logical ancilla qubit as control and the logical data as target, as depicted in Fig. 6. Since the control is prepared in the $|0\rangle_L$, the logical CNOT has no effect on the logical state, but the phase-flip errors of the target are copied on the ancilla block and then detected through a simple majority vote. Note that in the usual case, bit-flip errors can propagate from the ancilla block to the target block via the CNOT, which usually requires the logical ancilla state to be verified before it can be used in this protocol. Here, because the cat qubits have no bit-flip errors, and because the CNOT gates are bias-preserving, this verification step is unnecessary.

![Fig. 6. Steane error correction for a distance-3 repetition code protecting against phase-flips. The protocol requires the preparation of the $|0\rangle_L$ state on a logical ancillary qubit (top three lines), and the phase-flip errors of the logical data qubit (bottom three lines) are copied on the ancillary block by the CNOT gates and detected by the ancilla measurements.](image)

A. Fault-tolerance with concatenation

In this subsection, we numerically simulate the circuit of Fig. 7 to estimate the value of the phase-flip threshold with concatenation. This corresponds to the value of the physical error probability below which the logical Toffoli error probability is smaller than the physical one. As soon as the phase-flip error probability is below this threshold, the repetition code can be concatenated with a second repetition code. Note that the concatenation we consider here is that of two repetition codes, in order to make the logical Toffoli circuit fault-tolerant with respect to phase-flip errors only, and to get a phase-flip threshold. This is different from the concatenation that we discussed in the introduction, where the higher level code is chosen to be a code possessing an accuracy threshold with respect to both phase-flip and bit flip errors.

The logical Toffoli gate is built using $d^2$ physical Toffoli gates through the round-robin construction

$$\prod_{i,j\in[0,d-1]} \text{CCX}(i,j,k(i,j))$$

where CCX$(i,j,k)$ denotes a physical Toffoli gate between the $i$-th qubit of the first control block, the $j$-th qubit of the second control block, and the $k$-th qubit of target block. Note that $k(i,j)$ can actually be any mapping $[0,d-1] \times [0,d-1] \to [0,d-1]$, since the gates CCX$(i,j,k_1)$ and CCX$(i,j,k_2)$ act identically on the codespace of the three logical qubits, and we set $k(i,j) = j$ for the rest of the paper.

![Fig. 7. Logical Toffoli circuit for distance 3 repetition cat qubits. After each round of transversal Toffoli gates, a single round of stabilizer measurement is performed on the target block. The outcome of the measurement is decoded together with the history of all outcomes and an appropriate correction is applied. After the circuit, a full error correction stage is performed on all three blocks.](image)

There are two reasons this construction is not fault-tolerant as such. First, because this circuit is not transversal and any qubit of the target block is connected to all the qubits of the first control block, a single Z error acting on a qubit of the target block can be copied many times on the first control block, possibly leading to a logical failure. For example, a Z error occurring on a qubit of the target block before the circuit is executed propagates to the same Z error on the target block, plus a logical CZ gate between the two logical control qubits. This first problem can be solved following the pieceable fault-tolerant method of [46]. More precisely, we split the circuit containing $d^2$ physical Toffoli gates into $d$ transversal pieces of $d$ Toffoli gates each. As shown in Fig. 7 between two pieces, a round of error correction is performed on the target block to catch errors before they spread to the control blocks. Importantly, because the target X operator commutes with the CCX gate, the stabilizers of the target block $\{X_i X_{i+1}, i \in [0,d-1]\}$ are left unchanged by the CCX gates of the circuit and can be measured at any point in the circuit with the circuit of Fig. 1. The logical Toffoli circuit is executed as follows: after each of the first $d-1$ transversal pieces of CCX gates, a single round of stabilizer measurement
is performed on the target block. After each of these pieces, say the $k$-th one, the $k$ outcomes from all the previous measurements rounds are decoded together using a minimum weight matching decoder. The corresponding correction is applied before the $(k+1)$-th piece of the circuit is executed. After the last piece is executed, the usual error correction, composed of $d$ rounds of stabilizer measurements and correction, is performed on the three codeblocks. The fact that a single round of stabilizer measurement is enough during the intermediate error correcting steps can be intriguing. Indeed, since the measurements themselves are faulty, they usually need to be repeated a certain number of times, that scales linearly with the code distance, before the outcome of the first measurement, decoded together with the ones following, can be trusted. Here, a single round is executed independent of the code size, but is decoded using the full history of the previous measurement outcomes. The history of the $Z$ correction applied on the target block is also kept in memory. Thus, after all the $d$ pieces have been executed, a final decoding on all $d$ syndrome outcomes is performed and it becomes possible to know a posteriori which target $Z$ errors have propagated to $CZ$ errors between control qubits and to correct the corresponding $CZ$ before the final QEC round on the control blocks. This is possible because the $Z$ corrections performed on the target block anti-commute with the constant stabilizers of the target block, thus travel without being projected and can be undone later if needed.

The second reason the circuit is not fault-tolerant is because of the accumulation of non-propagating errors on the control qubits. Indeed, each qubit of the two control blocks undergo $d$ gates without the stabilizers of these qubits being measured. Therefore, without further considerations, when increasing the code distance $d$, the probability of $Z$ errors on these control blocks increases and eventually exceeds the fault-tolerance threshold of the repetition code. One way to handle this problem is by concatenation with another repetition code. Indeed, we will see throughout the rest of this subsection that despite the accumulation of non-propagating errors, the circuit of Fig. 7 yields very low logical error probabilities. The existence of a reasonable break-even point (a physical error probability for which one can find a code distance $d$ yielding a lower logical error probability) proves the existence of a concatenation phase-flip threshold. Concatenating a distance $d$ repetition code with itself produces a repetition code of distance $d^2$. The circuit implementing a logical Toffoli on the concatenation of these two codes is very similar to the one depicted in Fig. 7 except that it now includes error correcting steps on the control blocks every $d$ steps. The distance can be further increased by raising the number of levels of concatenation (the concatenation of $k$ repetition code produces a distance $d^k$ repetition code), while the number of steps between two rounds of error correction remains constant (equal to $d$).

In Fig. 8, we simulate the circuit of Fig. 7 incorporating the circuit-based error model with error models provided in Table I. As mentioned above, the absence of a phase-flip threshold can be explained by the accumulation of non-propagating errors: for all values of the physical error probability $p$, there is a finite optimal value of the code distance that achieves a minimum logical error probability. We also plot in Fig. 8 the identity line to visualize the “break-even point” below which the error probability of the logical Toffoli circuit is smaller than that of the physical Toffoli gate. Inset: Minimal value of the logical Toffoli error probability achievable for a given physical error probability. The optimal distance realizing this minimum is indicated on the curve.

\[ p_{Z_L} = \sum_{k=\lceil d/2 \rceil + 1}^{d} \binom{d}{k} p^k (1 - p')^{d-k} \]
where \( p' \approx dp \) is the probability that a given physical qubit of a logical control block is corrupted by a \( Z \) error during the circuits execution (the approximation \( p' \approx dp \) is valid as far as \( dp \ll 1 \)). This infidelity is plotted in plain lines, and, as expected, fits well the numerical values in the regime where the physical error probability \( p \) is small and the code distance \( d \) is large, for which the logical error is entirely set by the accumulation of non-propagating errors.

We used this asymptotic formula to estimate the optimal code distance \( d \) and the associated logical error probability for a given physical Toffoli error probability, as it is precisely the region of the curves where the formula fits very well the numerical values. The results are plotted in the inset of Fig. 8. As it can be observed, even without concatenation, a physical error probability of about \( .25\% \) per Toffoli gate on cat-qubits yields logical error rates of about \( 10^{-10} \) with as few as 60 modes. Now, if the physical error probability per cat-qubit Toffoli gate is about 1%, the same logical error probability of about \( 10^{-10} \) can be achieved with one level of concatenation, concatenating a 9 mode repetition code with a 60 mode one. Following the error model of the appendix achieved for the Toffoli implementation of [I], and assuming a two-photon dissipation rate of \( \kappa_{2ph}/2\pi = 1\text{MHz} \), this physical error probability can be achieved for a cavity lifetime of 1ms. With the recent progress in 3D superconducting cavities, this long lifetime can be typically achieved with cylindrical postcavities [22].

**B. Fault-tolerance without concatenation**

For the circuit of Fig. 7 to exhibit a phase-flip threshold without any concatenation, it is necessary to place additional rounds of error correction on the control blocks in such a way that the number of time-steps between two rounds of error detection does not increase with the code distance. Ideally, we would like to perform a round of error correction on all three logical blocks after each of the transversal pieces of the circuit. This task is complicated by the fact that the stabilizers of the control blocks are not constant throughout the circuit. We label the three logical qubits \( A, B \) and \( C \), where \( C \) is the logical target block and denote by \( X^A \) the X Pauli operator acting on the \( i \)-th physical qubit of block \( A \), where all subscripts are taken modulo the code distance \( d \). The \( k \)-th piece of the circuit \( P_k \) consists of \( d \) transversal Toffoli gates, where the control qubits of block \( A \) have been shifted by \( k-1 \)

\[
P_k = \prod_{i=0}^{d-1} \text{CCX}(i-k+1,i,i).
\]

Let us have a look at the value of the non-constant stabilizers of the two control code blocks \( X^O \) \( X^O \), \( O \in \{A,B\} \), \( i \in [0, d-1] \), after \( k \) pieces of the circuit have been executed. Noting \( U_k = \prod_{j \in [1,k]} P_j \), the stabilizers of

**FIG. 9.** Measurement circuit of the Clifford stabilizer \( X^A X^A_{i+1} \text{CX}^{B,C}(i,i) \text{CX}^{B,C}(i+k,i+k) \).

the two controls blocks \( A \) and \( B \) become under conjugation by this unitary

\[
S_{i,k}^A := U_k X^A_i X^A_{i+1} U_k^\dagger = X^A_i X^A_{i+1} \text{CX}^{B,C}(i,i) \text{CX}^{B,C}(i+k,i+k)
\]

\[
S_{i,k}^B := U_k X^B_i X^B_{i+1} U_k^\dagger = X^B_i X^B_{i+1} \prod_{j=0}^{k-1} \text{CX}^{A,C}(i-j,i) \text{CX}^{A,C}(i+1-j,i+1)
\]

where \( \text{CX}^{R,S}(i,j) \) denotes the CX gate between the \( i \)-th qubit of block \( R \) acting as the control and the \( j \)-th qubit of block \( S \) acting as the target. Note that the stabilizers of the control block \( C \) are constant throughout this evolution

\[
S_{i,k}^C := U_k X^C_i X^C_{i+1} U_k^\dagger = X^C_i X^C_{i+1}.
\]

The evolution of the stabilizers of the control blocks leads to a few issues that need to be handled carefully, to ensure the existence of a phase-flip threshold.

First, the unitary \( U_k \) does not belong to the Clifford group, but to the third level of the Clifford hierarchy [29]. It maps the Pauli stabilizers of the control blocks to Clifford operators. Nevertheless, these Clifford stabilizers can be measured using CCX gates and Clifford gates. The stabilizer \( S_{i,k} \) can be measured in the standard way using one ancilla qubit with the circuit depicted in Fig. 9. Importantly, the measurement of the non-constant stabilizers is bias-preserving as the CX and CCX gates possess this property.

Second, the weight of the stabilizers of control block \( A, S_{i,k}^A \), is constant at all intermediate steps of the circuit (here, by the weight, we mean the number of physical qubits in the support of the associated observable). Unfortunately, this is not the case for the stabilizers of control block \( B, S_{i,k}^B \), whose weights grow linearly with \( k \) the number of pieces. The asymmetry between the two control blocks is a consequence of the particular choice of ordering for the physical Toffoli gates. A symmetric ordering causes the weight of the stabilizers of both logical
blocks to grow linearly with the code distance, but unfortunately it is not possible to order the gates such that the weights of all stabilizers be bounded by a constant. This implies that an increasing depth-$k$ circuit might be needed to measure these stabilizers in the same fashion as in Figure 9. This scaling of the measurement time with the code distance $d$ prevents the existence of a phase-flip threshold.

The solution that we propose to get around this problem is to measure a different set of Clifford observables of constant weight instead of the stabilizers of block $B$. We chose these observables in such a way that the action of the circuit on the codespace is not modified by their measurement, while their measurement still reveals the value of the actual stabilizers. We call these Clifford observables, the “modified stabilizers”. One further trick here is to first perform a round of error correction on the target block $C$ before measuring the non-constant stabilizers of block $A$ and the modified “$B$-stabilizers”. Let us first assume that we can perform an ideal (fault-less) error correction on the target register, mapping the state of the logical block $C$ back to the code space. This means that $X_i^C X_{i+1}^C = +1$ for all $i$. Note that

$$
\prod_{j=0}^{k-1} \text{CX}^{A,C}(i - j, i) \text{CX}^{A,C}(i + 1 - j, i + 1) = \text{CX}^{A,C}(i + 1 - k, i) \text{CX}^{A,C}(i + 1, i + 1)
\times \prod_{j=1}^{k-1} \text{CX}^{A,C}(i + 1 - j, i) \text{CX}^{A,C}(i + 1 - j, i + 1)
$$

and that

$$
\text{CX}^{A,C}(i + 1 - j, i) \text{CX}^{A,C}(i + 1 - j, i + 1) = \frac{1}{2} (I + Z_{i+1-j}^A) + \frac{1}{2} (I - Z_{i+1-j}^A) X_i^C X_{i+1}^C.
$$

As $X_i^C X_{i+1}^C = +1$, we have

$$
S_{i,k}^B = X_i^B X_{i+1}^B \text{CX}^{A,C}(i + 1 - k, i) \text{CX}^{A,C}(i + 1, i + 1),
$$

which admits a constant weight now. It is important to note that these constant-weight “modified $B$-stabilizers” only commute with the $A$-stabilizers if the state of the block $C$ is in the codespace.

The remaining question is whether this procedure still works when the error correction step on the target block is imperfect, thus mapping imperfectly the state of the logical block $C$ to the codespace. In this case, the set of “modified $B$-stabilizers” may not commute with the $A$-stabilizers, thereby forbidding a simultaneous measurement of these two sets. Indeed, in the current error correction approach, the imperfection of the $C$-stabilizer measurements is compensated by the repetition of these measurements and a MWPM decoder. This procedure however requires to repeat the measurements a number of times that scales linearly with $d$ and during which we cannot measure the $A$ and $B$ stabilizers. The final trick to get around this issue is to replace the current error correction procedure of the target block by a single round of Steane-style error correction. Indeed, while the Steane-style error correction step can still be faulty, the output errors are not correlated to the input errors. This means that the measurements of the subsequent $A$ and $B$ stabilizers might be faulty, but these errors remain independent and therefore one can still hope to achieve a phase-flip threshold. The full circuit for the logical Toffoli gate, including the different error correction steps, is depicted in Fig. 10.
FIG. 11. Monte Carlo simulations of the circuit of Fig. 10 using a circuit-based error model. Here, we plot the error probability of the logical Toffoli gate as a function of the error probability of the physical cat qubit Toffoli gate. In the asymptotic regime where the physical error probability is small, the logical error probability now with \( \lceil \frac{d}{4} \rceil \) instead of the usual \( \lceil \frac{d}{2} \rceil \) that we get in the memory case. This is a consequence of the fact that the errors of a single physical qubit of the target block can spread to two different physical qubits within the same logical control block through the stabilizer measurements. Here, the curves are fit to the empirical scaling formula \( A(p_{th})^{d+1} \).

We perform the Monte-Carlo simulations of this circuit, using a circuit-based error model including the error models provided in the Table I. The simulation results are plotted in Fig. 11. These simulations indicate the existence of a threshold corresponding to a physical Toffoli error probability slightly below 3%. A typical physical error probability of 1% that can be achieved with the parameters of the previous subsection should result in a logical Toffoli error probability of \( 10^{-10} \) with as few as 90 data modes. This important overhead reduction, with respect to the previous concatenated case, comes at the expense of a fault-tolerant preparation of logical \( |0\rangle_L \) states that will be consumed by the Steane EC protocol. This logical preparation can be performed by initializing each mode in the coherent state \( |\alpha\rangle \) followed by \( d \) rounds of \( X_iX_{i+1} \) parity measurements and correction by MWPM. This requires to allocate a memory register in which the states are constantly prepared, maintained by EC, and consumed by logical Toffoli gates when needed.

VI. TOWARDS A PRACTICAL ARCHITECTURE

We have investigated the error rates and resource overhead that could be expected using repetition cat qubits. In this work, we have not yet considered the physical restrictions imposed by the particular experimental implementation of the scheme. Typically, a realistic scheme for large scale fault-tolerant quantum computation should possess the following features: a high accuracy threshold such that error rates well below this value can be achieved in the experiments, a universal set of logical gates that can be implemented with a reasonable resource overhead, and an architecture that can be scaled up to a size where the logical error rates match those needed for the targeted computation. The first and the last points are the strongest assets of the surface code approach, and the main reason for its popularity. Indeed, this code combines the advantage of a high accuracy threshold around 1% for a depolarizing noise model \([53]\) and a 2D spatial arrangement of the physical qubits requiring only low-weight stabilizer measurements between nearest neighbours. Here, the transversal Clifford operations presented in Section V are compatible with a 2D architecture and using only couplings between neighbouring qubits. However, the two circuits proposed in Section V exploit an all-to-all coupling between the data cat qubits of the two logical control blocks. Within the particular circuit QED framework that we have in mind for the experimental implementation of repetition cat qubits, this kind of connectivity is less practical and rises a major challenge. Yet, it is worth noting that we anticipate very low logical error rates with only a few tens of cat qubits per logical qubit, which is a drastically lower overhead than those usually envisioned in other QEC schemes. Therefore, the general constraints on the connectivity graph of the physical qubits may be easier to satisfy for near term experiments involving a small number of cat qubits, yet achieving low logical error rates.

While the optimal layout of a large scale quantum computer based on repetition cat qubits is not known yet, here we provide a few possible directions. The connectivity graph for the logical Toffoli circuit of Section VA can be made “local” by swapping the data qubits of the first control block appropriately, as depicted in Fig. 12.

FIG. 12. Logical Toffoli circuit for distance 5 repetition cat qubits including physical SWAPs on the first control block during error correcting stage on the target. The physical SWAP gates ensure a great simplification of the connectivity graph for the implementation of the logical Toffoli gate.
Each physical cat qubit of a given repetition cat qubit now only needs to be coupled to a single cat qubit of another repetition cat qubit. Yet, the intermediate rounds of error correction on the target block are still needed to prevent the propagation of errors. The particular ordering of the physical Toffoli gates in Fig. 12 differs from the circular permutations previously considered. This particular choice corresponds to a permutation that can be implemented with parallel SWAPs in two steps, independently of the code distance. One may wonder whether the same trick can be applied to the second Toffoli circuit (Fig. 10) or a similar fault-tolerant circuit. The existence of a Toffoli circuit ordering that allows us both to measure constant weight Clifford operators for the intermediate error correction steps on the logical control blocks and that can be implemented using a constant depth circuit of SWAP gates is an open problem and requires further investigation.

An important question is whether the SWAP operations can be performed in a bias-preserving manner. The answer is yes, since a SWAP gate can be implemented using three CNOT gates, but there is a more direct way to implement a bias-preserving SWAP gate between two physical cat qubits. In the same spirit as the CNOT gate, this is done by replacing the regular two-photon dissipators \( \hat{L}_a = \hat{a}^2 - \alpha^2 \) and \( \hat{L}_b = \hat{b}^2 - \alpha^2 \) by the following time-dependent operators that combine both modes
\[
\hat{L}_a(t) = \hat{a}^2 - \frac{1}{2} \hat{a} \hat{b} (1 - e^{2i \pi t}) - \frac{1}{2} \alpha^2 (1 + e^{2i \pi t}),
\]
\[
\hat{L}_b(t) = \hat{b}^2 - \frac{1}{2} \hat{a} \hat{b} (1 - e^{-2i \pi t}) - \frac{1}{2} \alpha^2 (1 + e^{-2i \pi t}),
\]
where \( t \in [0, T] \) and \( T \) is the SWAP gate time. The instantaneous joint kernel of these operators is the four dimensional Hilbert space spanned by the coherent states
\[
|\alpha, \alpha\rangle, |\alpha, -\alpha\rangle, |\alpha e^{i \pi/4}, -\alpha e^{-i \pi/4}\rangle, |\alpha e^{i \pi/4}, \alpha e^{-i \pi/4}\rangle.
\]
Recalling that \( |0\rangle \approx |\alpha\rangle \) and \( |1\rangle \approx |\alpha\rangle \), these two dissipation channels implement the correct mapping corresponding to a SWAP gate:

\[
|\alpha, \alpha\rangle \rightarrow |\alpha, \alpha\rangle,
\]
\[
|\alpha, -\alpha\rangle \rightarrow |\alpha, -\alpha\rangle,
\]
\[
|\alpha e^{i \pi/4}, -\alpha e^{-i \pi/4}\rangle \rightarrow |\alpha, \alpha\rangle,
\]
\[
|\alpha e^{i \pi/4}, \alpha e^{-i \pi/4}\rangle \rightarrow |\alpha, -\alpha\rangle.
\]

Another potential solution to build a logical Toffoli circuit compatible with a 2D nearest neighbours architecture without using SWAP gates is to use gate teleportation techniques of 2D. The implementation of a logical Toffoli gate can be done using transversal logical Clifford operations, and an additional ancillary system of three logical qubits prepared in a special state called the “Toffoli magic state”. The bottleneck of this approach is the preparation of this magic state with arbitrarily high fidelity. By exploiting the specific structure of noise in cat qubits, it might be possible to construct a fault-tolerant non-Clifford gate with a similar overhead to the circuits presented in this paper, while being compatible with a 2D local architecture.

VII. CONCLUSION

The realization of high-fidelity quantum operations for large scale quantum processors will most likely involve quantum error correction to achieve fault-tolerance. While this fault-tolerance usually comes at the expense of an important resource overhead, it is pressing to find shortcuts that reduce the overhead requirements to what is achievable in near-term experiments. In this paper, by performing numerical simulations with a realistic circuit-level error model, we showed that the repetition cat qubit is a serious candidate towards achieving a universal gate set with very low error rates while maintaining the physical cost at a minimum. Similarly to the Bacon-Shor codes, the repetition cat qubit scheme does not possess an accuracy threshold, yet it exhibits a pseudo-threshold in an experimentally realistic regime. In this regime, assuming a physical error probability of 1%, a quantum memory with a logical error probability of \( 10^{-10} \) can be realized using 70 physical cat qubits (twice as much including ancilla cat qubits) and an average number of \( \bar{n} = 6 \) photons per mode. The logical gates that are transversal on the repetition code, such as the preparation of the \( |\pm\rangle_L \) states, the measurement of the \( X_L \) operator or the CNOT gate, have a similar performance and overhead. The gate that completes the universal set of logical gates is the Toffoli gate, and cannot be implemented transversally. We proposed two different circuits that realize this gate fault-tolerantly. Assuming a physical error probability of 1% per physical Toffoli gate, the first circuit achieves a logical Toffoli error probability of \( 10^{-10} \) using \( 9 \times 60 = 450 \) cat qubits per logical qubit (900 including ancillae) and one level of code concatenation. The second circuit is fault-tolerant even without concatenation, by using a tailored error detection protocol preventing both the propagation of errors due to the non-transversality and the accumulation of non-propagating errors. This protocol, involving a more complex circuit, requires the preparation of special ancillary states, but results in an overall reduction of the overhead and achieves a logical error rate of \( 10^{-10} \) with only 90 cat qubits per logical qubit (180 including ancillae). A major obstacle to overcome in this approach, is the requirement of all-to-all couplings between the cat qubits to implement the logical Toffoli gate. Although it is possible to simplify the connectivity graph by adding SWAP gates, which can themselves be implemented in a bias-preserving manner as required by the construction, the conception of an optimal 2D architecture for a large scale quantum computer based on repetition cat qubits is still under investigation.

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Region Ile-de-France in the framework of DIM SIRTEQ.

Appendix: Efficient simulation of Toffoli circuits

The simulation of non-Clifford circuits is classically hard. In our case, however, there are a few specific features that enable us to perform the Monte Carlo simulations of all the non-Clifford circuits presented in this work in a classically efficient manner. The first important thing to note is that while the circuits contain non-Clifford Toffoli gates, the propagation of errors in the circuits can never produce non-Clifford errors, as would be the case in all generality. To see this, recall from the error models of Table I that all the 'bare' errors produced by any gates in the Toffoli circuits are of the following form: a Pauli $Z$ error on any data qubit of any logical block, a Pauli correlated $Z_1Z_2$ error on any two pair of data qubits of the two control blocks, a controlled-phase gate $CZ_{12}$ between any two data qubit of the control blocks, or a correlated controlled-phase gate and $Z$ error $CZ_{12}Z_3$ on two data qubit of the control block and a data qubit of the target block. Now, note that none of these errors can become non-Clifford through the Toffoli circuits: the Pauli $Z$ errors of the control blocks commute with the Toffoli gates, while a $Z$ error on the target block evolves through a Toffoli gate as a $Z$ error on the target block together with a controlled-phase error between the two controls:

$$CCX_{1,2,3} \times Z_3 = CZ_{1,2}Z_3 \times CCX_{1,2,3}.$$  

Thus, the only Clifford error that can ever appear anywhere in the circuits is a controlled-phase between any pair of two qubits of the controls blocks, either produced by a Toffoli gate error or by propagation of a $Z$ error on the target block through another Toffoli gate. Once these errors appear, however, they can never propagate further to non-Clifford errors as a controlled-phase gate on the control qubits of a Toffoli gate commutes with the Toffoli gate:

$$CCX_{1,2,3} \times CZ_{1,2} = CZ_{1,2} \times CCX_{1,2,3}.$$  

Thus, several specific ingredients ensure that all the errors we deal with are at most Clifford: the fact that the gates error models are biased, such that we deal only with phase-flip types of errors, the fact that the gates are all bias-preserving, thus preserving the phase-flip nature of errors, and finally the fact that we only use Toffoli gate as non-Clifford resource where the target qubit of any physical Toffoli gate always belong to the same codeblock. Indeed, if we were to use two Toffoli gate in a circuit with the target qubits belonging to two different logical blocks, then a $CZ$ error produced by the first Toffoli gate could evolve to a non-Clifford $CCZ$ error by propagation through the second Toffoli:

$$CCX_{1,2,3} \times CZ_{1',3} = CCX_{1,1',2} \times CZ_{1',3} \times CCX_{1,2,3}.$$  

With these facts in mind, we now detail how the logical error probability of a noisy Toffoli circuit can be simulated efficiently. The first step is to roll a dice to determine the locations and nature of the errors, according to the errors models described above. Then, the errors are propagated through the gates circuit up until a point where they meet a measurement. At this point, the circuit has been decomposed in two different circuits: the first one is perfect, and contains the non-Clifford Toffoli gates, and it is followed by a second one that consists of
the errors only, and contains exclusively Clifford operations. We depict in Fig. 13 one example of this circuit decomposition, for the first piece of the circuit of Fig. 10. The left-hand side of the circuit, which is perfect, is non-Clifford but its effect on the value of the stabilizers is trivial. Actually, since the operators that we measure are “compatible” with the Toffoli pieces of the circuit (see Section 1), in the absence of errors, the results of the measurement of these operators is +1 with unit probability. The only thing that needs to be simulated numerically to get the correct probability distribution for the measurement outcomes is the effect of the error circuit (red box of Fig. 13 (b)) on the measurement results and the remaining errors after the measurements have been executed. However, since this error circuit is Clifford, it can be efficiently simulated using the CHP algorithm [25]. Note that the errors on the target block are always simple Pauli Z errors, even after propagation through any gate of the circuit. Thus, the logical error rate of the target block can actually be simulated separately from the rest, using a simple array of 0, 1 integers.

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