Symbol-Decision Successive Cancellation List Decoder for Polar Codes

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Abstract—Polar codes are of great interests because they provably achieve the capacity of both discrete and continuous memoryless channels while having an explicit construction. Most existing decoding algorithms of polar codes are based on bit-wise hard or soft decisions. In this paper, we propose symbol-decision successive cancellation (SC) and successive cancellation list (SCL) decoders for polar codes, which use symbol-wise hard or soft decisions for higher throughput or better error performance. First, we propose to use a recursive channel combination to calculate symbol-wise channel transition probabilities, which lead to symbol decisions. Our proposed recursive channel combination also has a lower complexity than simply combining bit-wise channel transition probabilities. The similarity between our proposed method and Arikan’s channel transformations also helps to share hardware resources between calculating bit- and symbol-wise channel transition probabilities. Second, a two-stage list pruning network is proposed to provide a trade-off between the error performance and the complexity of the symbol-decision SCL decoder. Third, since memory is a significant part of SCL decoders, we propose a pre-computation memory-saving technique to reduce memory requirement of an SCL decoder. Finally, to evaluate the throughput advantage of our symbol-decision decoders, we design an architecture based on a semi-parallel successive cancellation list decoder. In this architecture, different symbol sizes, sorting implementations, and message scheduling schemes are considered. Our synthesis results show that in terms of area efficiency, our symbol-decision SCL decoders outperform both bit- and symbol-decision SCL decoders.

Index Terms—Error control codes, polar codes, successive cancellation, list decoding algorithm, hardware implementation

I. INTRODUCTION

Polar codes, a groundbreaking finding by Arikan [1] in 2009, have ignited a spark of research interest in the fields of communication and coding theory, because they can provably achieve the capacity for both discrete [1] and continuous [2] memoryless channels. The second reason why polar codes are attractive is their low encoding and decoding complexity. For example, a polar code of length $N$ can be decoded by the successive cancellation (SC) algorithm [1] with a complexity of $O(N \log N)$. However, their capacity approaching can be achieved only when the code length is large enough ($N \geq 2^{20}$) [3] if the SC algorithm is used. For short or moderate code length, in terms of the error performance, polar codes with the SC algorithm are inferior to Turbo codes or low-density parity-check (LDPC) codes [4, 5].

Since the debut of polar codes, a lot of efforts have been made to improve the error performance of short polar codes. Systematic polar codes [6] were proposed to reduce the bit error rate (BER) while guaranteeing the same frame error rate (FER) as their non-systematic counterparts. Although a Viterbi algorithm [7], a sphere decoding algorithm [8] and stack sphere decoding algorithm [9] can provide maximum likelihood (ML) decoding of polar codes, they are considered infeasible, especially for long polar codes, due to their much higher complexity than the SC algorithm. Recently, an SC list algorithm for polar codes was proposed in [10] to bridge the performance gap between the SC algorithm and ML algorithms at the cost of complexity of $O(LN \log N)$, where $L$ is the list size. Moreover, the concatenation of polar codes with cyclic redundancy check (CRC) codes was introduced in [4, 11]. To decode the CRC-concatenated polar codes, a CRC detector is used in the SCL algorithm to help select the output codeword. The combination of an SCL algorithm and a CRC detector is called CRC-aided SCL (CA-SCL) algorithm. [11] shows that with the CA-SCL algorithm, the error performance of a (2048, 1024) CRC-concatenated polar code is better that of a (2304, 1152) LDPC code, which is used in the WiMax standard [12].

Several architectures have been proposed for the SC algorithm. Arikan [11] showed that a fully parallel SC decoder has a latency of $2N - 1$ clock cycles. A tree SC decoder and a line SC decoder with complexity of $O(N)$ were proposed in [13]. These two decoders have the same latency as the fully parallel SC decoder. To reduce complexity further, Leroux et al. [3] proposed a semi-parallel SC decoder for polar codes by taking advantage of the recursive structure of polar codes to reuse processing resources. Assuming that the number of processing elements (PEs) are $P$ ($P = 2^p \leq N$), the latency of the semi-parallel SC decoder is $2N + \frac{N \log_2 \left( \frac{N}{2^p} \right)}{P}$ clock cycles. To reduce the latency, a simplified SC (SSC) polar decoder was introduced in [14] and it was further analyzed in [15]. In the SSC polar decoder, a polar code is converted to a binary tree including three types of nodes: rate-one, rate-zero and rate-$R$ nodes. Based on the SSC polar decoder, the ML SSC decoder makes use of the ML algorithm to deal with part of rate-$R$ nodes in [15]. However, the SSC and ML-SSC polar decoders depend on positions of information bits and frozen bits, and are code-specific consequently. In [17], a pre-computation look-ahead technique was proposed to reduce the latency of the tree SC decoder by half. For the SCL polar decoder, the semi-parallel architecture was adopted in [18]. In [19] Balatsoukas-Stimming et al. proposed an architecture of $L = 4$ to achieve a throughput of 124 Mbps and a latency of 8.25 ms when decoding a (1024, 512) polar code. In [20], Lin and Yan designed an SCL polar decoder with the throughput of 182 Mbps and a latency of 5.63 ms. To reduce the memory requirement, the log-likelihood ratio (LLR) messages are used in [21]. The throughput of existing polar decoders is still not high enough for high speed applications.
Since the low throughput (or long latency) of the SC decoder is due to its serial nature, several previous works attempt to improve the throughput (or latency). In [22], the data bits of a polar code is split into several streams, which are decoded simultaneously. This idea of parallel processing is extended in [23], where the SC decoder is transformed into a concatenated decoder, where all the inner SC decoders are carried out in parallel. Yuan and Parhi proposed a multi-bit SCL decoder [24].

In this paper, we address the throughput/latency issue by proposing symbol-decision SC and SCL decoders, which are based on symbol-wise hard or soft decisions. Since each symbol consists of \( M \) bits, when \( M > 1 \) the symbol-decision decoders achieve higher throughput as well as better error performance. The proposed symbol-decision decoders are natural generalization of their bit-wise counterparts, and reduce to existing bit-wise decoders when the symbol size is one bit. The main contributions of this paper are:

- We propose a novel recursive channel combination to calculate the symbol-wise channel transition probabilities, which enable symbol decisions in SC and SCL algorithms. The proposed recursive channel combination also has a lower complexity than simply combining bit-wise channel transition probabilities. The similarity between the Arikan’s recursive channel transformation and our symbol-wise recursive channel combination helps to share hardware resources to calculate the bit- and symbol-based channel transition probabilities.

- An \( M \)-bit symbol-decision SCL decoder needs to find the \( L \) most reliable candidates out of \( 2^M L \) list candidates. We propose a two-stage list pruning network to perform this sorting function. This pruning network also provides a trade-off between performance and complexity.

- By adopting pre-computation technique [25]. We develop a pre-computation memory-saving (PCMS) technique to reduce the memory requirement of the SCL decoder. Specifically, the channel information memory can be eliminated when using the PCMS technique. Moreover, this technique also helps to improve throughput slightly.

- To evaluate the throughput of symbol-decision SC decoders, we propose an area efficient architecture for symbol-decision SCL decoder. In our architecture, to save the area, adders in processing units are reused to calculate the symbol-wise channel transition probability. We propose two scheduling schemes for sharing hardware resources. We also propose two list pruning network for designs with different symbol sizes.

- We design two-, four-, and eight-bit symbol-decision SCL decoders for a (1024, 480) CRC32-concatenated polar code with a list size of four. Synthesis results show that in terms of area efficiency, our symbol-decision SCL decoder outperforms all existing state-of-the-arts SCL decoders in [19]–[21], [24]. For example, the area efficiency of our four-bit symbol-decision SCL decoder is 259.2 Mb/s/mm\(^2\), which is 1.51 times as big as that of [21]. Our implementation results also demonstrate that the symbol-decision SCL decoder can provide a range of tradeoffs between area, throughput, and area efficiency.

Our symbol-decision decoding algorithms assume that the underlying channel has a binary input, and our symbol-wise channel transformation is virtual and introduced for decoding only. Hence, our work is different from those assuming a \( q \)-ary (\( q > 2 \)) channel (see, for example, [26]).

The decoding schedule (bit sequence) of our symbol-decision decoding algorithms is actually the same as those in [23]–[24], but our symbol-decision decoding algorithms are different from those in [22]–[23] in two aspects. First, our symbol-wise recursive channel transition is different from how transition probabilities are derived in [22]–[24]. Second, the symbol-decision perspective allows us to prove that the symbol-decision algorithms have better frame error rates (FERs) than their bit-decision counterparts [27], while only simulation results are provided in [22], [24] and error performance is not investigated in [23]. There are additional differences between our decoding algorithms/architectures and those in [22]–[24]. For instance, all the bits within a symbol are estimated jointly in our symbol-decision SC algorithm, whereas some bits are decoded independently for the decoder with parallelism two in [22]. Also, while our symbol-decision decoding is introduced on the algorithmic level, the multibit decoder is introduced on the level of decoding operations [24]. Finally, for our symbol-decision SCL decoders, we use the semi-parallel architecture because it is more area efficient than the tree architecture and the line architecture [13].

The rest of our paper is organized as follows. Section II briefly reviews polar codes and existing decoding algorithms for polar codes. In Section III the symbol-based recursive channel combination is proposed to calculate the symbol-based channel transition probability. Moreover, to simplify the selection of the list candidates, a two-stage list pruning network is proposed. In Section IV we introduce a method to reduce memory requirement of list decoders of polar codes by pre-computation technique. In Section V we demonstrate the hardware architecture for symbol-decision SCL decoders. Two scheduling schemes for hardware sharing are discussed. We also propose two list pruning network for different designs: a folded sorting implementation and a tree sorting implementation. A discussion on the latency of our architecture and synthesis results for our implementations are provided in this section as well. Finally, we draw some conclusions in Section VI.

II. POLAR CODES AND EXISTING DECODING ALGORITHMS

A. Preliminaries

We follow the notation for vectors in [1], namely \( u^b_a = (u_a, u_{a+1}, \ldots, u_{a+b-1}, u_b) \); if \( a > b \), \( u^b_a \) is regarded as void. \( u^b_{a,a} \) and \( u^b_{a,a,e} \) denote the subvector of \( u^b_a \) with odd and even indices, respectively.

Let \( W : \mathcal{X} \rightarrow \mathcal{Y} \) represent a generic B-DMC with binary input alphabet \( \mathcal{X} \), arbitrary output alphabet \( \mathcal{Y} \), and transition probabilities \( W(y|x) \), \( y \in \mathcal{Y}, x \in \{0, 1\} \). Assume

\[ W(y|x) = \begin{cases} p_{y|x} & \text{if } x = y, \\ q_{y|x} & \text{if } x \neq y, \end{cases} \]

where \( p_{y|x} > 0 \) and \( q_{y|x} > 0 \).
N is an arbitrary integer and M is an integer satisfying $M|N$. Let $W_{N,M}^{(j)}$ denote a set of $\frac{N}{M}$ coordinate channels: $W_{N,M}^{(j)} : \mathcal{X}^M \rightarrow \mathcal{Y}^N \times \mathcal{X}^{(j-1)M}$, $0 < j \leq \frac{N}{M}$ with the transition probabilities $W_{N,M}^{(j)}(y_1, x_1^{(j-1)M})$, $0 < j \leq \frac{N}{M}$ and $x_{(j-1)M+1}$ denote the output and input of $W_{N,M}^{(j)}$, respectively.

B. Polar Codes

Polar codes are linear block codes, and their block lengths are restricted to powers of two, denoted by $N = 2^n$ for $n \geq 2$. Assume $u = u_1^N = (u_1, u_2, \cdots, u_N)$ is the data bit sequence. Let $F = \{1, 0\}$. The corresponding encoded bit sequence $x = x_1^N = (x_1, x_2, \cdots, x_N)$ is generated by

$$x = uB_N F^{\otimes n},$$

where $B_N$ is the $N \times N$ bit-reversal permutation matrix and $F^{\otimes n}$ denotes the $n$-th Kronecker power of $F$.

For any index set $A \subseteq \{1, 2, \cdots, N\}$, $u_A = (u_i : 0 < i \leq N, i \in A)$ is the sub-sequence of $u$ restricted to $A$. For an $(N, K)$ polar code, the data bit sequence is grouped into two parts: a $K$-element part $u_A$ which carries information bits, and $u_{A^c}$ whose elements are predefined frozen bits, where $A^c$ is the complement of $A$. For convenience, frozen bits are set to zero.

C. SC Algorithm for Polar Codes

Given a transmitted codeword $x$ and the corresponding received word $y$, the SC algorithm for an $(N, K)$ polar code estimates the encoding bit sequence $u$ successively as shown in Alg. 1. Here, $\hat{u} = (\hat{u}_1, \hat{u}_2, \cdots, \hat{u}_N)$ represents the estimated value for $u$.

**Algorithm 1: SC Decoding Algorithm**

1. for $j = 1 : N$
2.  if $j \in A^c$ then $\hat{u}_j = 0$ else
3.  if $W_{N,1}^{(j)}(y, u_{j-1}^{j-1} | u_j) \geq 1$ then $\hat{u}_j = 1$ else
4.  $\hat{u}_j = 0$

To calculate $W_{N,1}^{(j)}(y, u_{j-1}^{j-1} | u_j)$, Arikan’s recursive channel transformation is applied. A pair of binary channels $W_{2A,1}^{(j-1)}$ and $W_{2A,1}^{(2j)}$ are obtained by a single-step transformation of two independent copies of a binary input channel $W_{A,1}^{(i)} : (W_{A,1}^{(i)}, W_{A,1}^{(1)}) \rightarrow (W_{2A,1}^{(j-1)}, W_{2A,1}^{(2j)}).$ The channel transition probabilities of $W_{2A,1}^{(j-1)}$ and $W_{2A,1}^{(2j)}$ are given by

$$W_{2A,1}^{(j-1)}(y, u_{j-2}^{j-1} | u_{j-1}) = \frac{1}{2} \sum_{u_{j-2}} W_{A,1}^{(i)}(y, u_{j-2}^{j-1} | u_{j-1}) W_{A,1}^{(j)}(y, u_{j-2}^{j-2} | u_{j-1} + u_{2j})$$

$$= \frac{1}{2} \sum_{u_{j-2}} \left[ W_{A,1}^{(i)}(y, u_{j-2}^{j-2} | u_{j-1} + u_{2j}) + W_{A,1}^{(i)}(y, u_{j-2}^{j-2} | u_{j-1} + u_{2j}) \right].$$

and

$$W_{2A,1}^{(2j)}(y, u_{2j-2}^{2j-1} | u_{2j}) = \frac{1}{2} W_{A,1}^{(i)}(y, u_{2j-2}^{2j-2} | u_{2j-1} + u_{2j}) + W_{A,1}^{(i)}(y, u_{2j-2}^{2j-2} | u_{2j-1} + u_{2j}).$$

D. Parallel SC Algorithm for Polar Codes

The SC algorithm makes hard-decision for only one bit at a time, as shown in Fig. 1(a). We call it bit-decision decoding algorithm. A parallel SC decoder makes hard-decision for $M$ bits instead of only one bit at a time, as shown in Fig. 1(b).

Without loss of generality, assume $M$ is a power of two, i.e. $M = 2^m (0 \leq m \leq n)$. $\mathcal{M}_j \overset{\text{def}}{=} \{jM - M + 1, jM - M + 2, \cdots, jM\}$, for $0 < j \leq \frac{N}{M}$, $\mathcal{M}_j \cap \mathcal{A}$ and $\mathcal{A}_j \overset{\text{def}}{=} \mathcal{M}_j \cap \mathcal{A}^c$. Given $y$ and $\hat{u}_1^{M-M-M+1}$, $\hat{u}_j^{jM-M+1}$ is determined by

$$\hat{u}_j^{jM-M+1} = \arg \max_{u_{jM-M+1}} W_{N,M}^{(j)}(y, u_{jM-M+1} | u_{jM-M+1})$$

where $|\mathcal{A}_j|$ represents the cardinality of $\mathcal{A}_j$. If $M = N$, this decoding algorithm is exactly a maximum-likelihood sequence decoding algorithm.

![Fig. 1. Decoding of (a) bit-decision vs. (b) M-bit symbol-decision](image-url)
Algorithm 2: SCL Decoding Algorithm [10]

\begin{algorithm}
\begin{algorithmic}[1]
\State $\alpha = 1$;
\For {$j = 1 : N$}
  \If {$j \in A^c$}
    \For {$i = 1 : \alpha$}
      \State $(L_i)_j = 0$;
    \EndFor
  \ElsIf {$2 \alpha \leq L$}
    \For {$i = 1 : \alpha$}
      \State $(L_i)_j = \text{conc}((L_i)_j^{-1}, 0)$;
      \State $(L_{i+\alpha})_j = \text{conc}((L_i)_j^{-1}, 1)$;
      \State $\alpha = 2 \alpha$;
    \EndFor
  \Else
    \For {$i = 1 : L$}
      \State $S[i].P = W_{N,1}^{(j)}(y, (L_i)_j^{-1}[0])$;
      \State $S[i].L = (L_i)_j^{-1}$;
      \State $S[i].U = 0$;
      \State $S[i+L].P = W_{N,1}^{(j)}(y, (L_i)_j^{-1}[1])$;
      \State $S[i+L].L = (L_i)_j^{-1}$;
      \State $S[i+L].U = 1$;
      \State \text{sortDecrement}(S);
      \State $\alpha = L$;
    \EndFor
    \State $\hat{u} = L_1$;
  \EndIf
\EndFor
\end{algorithmic}
\end{algorithm}

E. SCL and CA-SCL Algorithms for Polar Codes

Instead of making a hard decision for each information bit of $u$ in the SC algorithm, the SCL algorithm creates two paths in which the information bit is assumed to be 0 and 1, respectively. If the number of paths is greater than the list size $L$, the most reliable paths are selected. At the end of the decoding procedure, the most reliable path is chosen as $\hat{u}$. The SCL algorithm is formally described in Alg. 2. Without loss of generality, we assume $L$ to be a power of two, i.e. $L = 2^L$. We use $L_i = ((L_i)_1, (L_i)_1, \cdots, (L_i)_N)$ to represent the $i$-th list vector, where $0 < i \leq L$. $S$ is a structure type array with size $2L$. Each element of $S$ has three members: P, L, and U. The function sortDecrement sorts the array $S$ by decreasing order of P. $con((a, b))$ attaches a bit sequence $b$ at the end of a bit sequence $a$, and the length of the output bit sequence $c$ is the sum of lengths of $a$ and $b$.

The CA-SCL algorithm is used for the CRC-concatenated polar codes. The difference between CA-SCL [11] and SCL algorithms is how to make the final decision for $\hat{u}$. If there is at least one path satisfying the CRC constraint, the most reliable CRC-valid path is chosen for $\hat{u}$. Otherwise, the decision rule of the SCL algorithm is used for the CA-SCL algorithm.

III. $M$-bit Symbol-Decision Decoding Algorithms for Polar Codes

A. $M$-bit Symbol-Decision SC Algorithm

Here, we proposed a symbol-decision SC algorithm, which treats $M$-bit data as a symbol and decodes a symbol at a time. Let $Z$ represent the alphabet of all $M$-bit symbols. The symbol-decision SC algorithm deals with the virtual channel $\mathcal{V}_{N}^{(j)} : Z \rightarrow \mathcal{Y}^N \times Z^{(j-1)}$, $0 < j \leq \frac{N}{M}$ with the transition probabilities $W_{N}^{(j)}(y^N, z^{j-1} | z_j)$, where $(y^N, z^{j-1})$ and $z_j = (u_{j M-M+1} \cdots, u_{j M})$ denote the output and input of $\mathcal{V}_{N}^{(j)}$, respectively. Actually, $W_{N}^{(j)}$ is exactly equivalent to $W_{N,M}^{(j)}$ if we consider $X^M$ as the binary vector representation of $Z$. Therefore, the symbol-decision SC algorithm has the same schedule as the parallel SC algorithm in [22]–[24]. However, our symbol-decision SC algorithm has a different approach, called symbol-based recursive channel combination, to compute symbol-based channel transition probabilities $W_{N,M}^{(j)}(y, \hat{u}_1^{M-M} | u_j M-M+1)$, which is our main focus.

B. Symbol-Based Recursive Channel Combination

Assume $u_{i M-M+1}^{M-M+1} = (w_i, w_{i+N}, \cdots, w_{i+N-N})B_{M}F^{\phi m}$ for $1 \leq i \leq \frac{N}{M}$. In [22]–[24], the calculation of the symbol-based channel transition probability $W_{N,M}^{(i)}(y, \hat{u}_1^{M-M} | u_{i M-M+1})$ is based on the following equation, referred to as direct-mapping calculation:

$$W_{N,M}^{(i)}(y, \hat{u}_1^{M-M} | u_{i M-M+1}) = \prod_{j=0}^{M-1} W_{N}^{(j)}(y|y_{j M-M+1}^{(j-1)+\sigma} \oplus \hat{u}_{i+1}^{(j-1)+\sigma} | u_{i+1}^{(j-1)+\sigma} + 1)$$

(7)

where $W_{N}^{(i)}(y|y_{j M-M+1}^{(j-1)+\sigma} \oplus \hat{u}_{i+1}^{(j-1)+\sigma} | u_{i+1}^{(j-1)+\sigma} + 1)$ is calculated by the Arikan’s recursive channel transformations.

Actually, a symbol-based recursive channel combination described in Proposition 1 can be used to calculate $W_{N,M}^{(i)}(y, \hat{u}_1^{M-M} | u_{i M-M+1})$.

Proposition 1. Assume that all bits of $u$ are independent and each bit has an equal probability of being a 0 or 1. Given $0 < m \leq n$, $N = 2^n$, $M = 2^m$, for any $1 \leq \phi \leq m$, $0 \leq \lambda < n$, $\Lambda = 2^\lambda$, $\Phi = 2^\phi$, and $0 \leq \lambda < \frac{M}{2^\phi}$, we say that a $\phi$-bit channel $W_{\Lambda,\phi}^{(i+1)}$ is obtained by a single-step combination of two independent copies of a $\frac{\Phi}{2}$-bit channel $W_{\Lambda,\Phi/2}^{(i+1)}$ and write

$$W_{\Lambda,\Phi/2}^{(i+1)}(y_{1,\Phi/2}^{(i+1)} | u_{1,\Phi/2}^{(i+1)} \oplus u_{1,\Phi/2}^{(i+1)} \oplus u_{1,\Phi/2}^{(i+1)} = W_{\Lambda,\phi}^{(i+1)}(y_{1,\phi}^{(i+1)} | u_{1,\phi}^{(i+1)} \oplus u_{1,\phi}^{(i+1)} \oplus u_{1,\phi}^{(i+1)})$$

(8)

where the channel transition probability satisfies,

$$W_{\Lambda,\phi}^{(i+1)}(y_{1,\phi}^{(i+1)} | u_{1,\phi}^{(i+1)} \oplus u_{1,\phi}^{(i+1)} \oplus u_{1,\phi}^{(i+1)} = W_{\Lambda,\phi/2}^{(i+1)}(y_{1,\phi/2}^{(i+1)} | u_{1,\phi/2}^{(i+1)} \oplus u_{1,\phi/2}^{(i+1)} \oplus u_{1,\phi/2}^{(i+1)}$$

(9)

Similar to the SC algorithm, with the help of the symbol-based recursive channel combination, an $M$-bit symbol-decision SC algorithm can be represented by using a message flow graph (MFG) as well, where a channel transition probability is referred to as a message for the sake of convenience. This MFG is referred to as SR-MFG. If the code length of a polar code is $N$, the SR-MFG can be divided into $(n+1)$ stages $(S_0, S_1, \cdots, S_n)$ from the right to the left: one initial stage $S_0$ and $n$ calculation stages. For the SC
algorithm, all calculation stages carry out the Arikan’s recursive channel transformation. However, for the \(M\)-bit symbol-decision SC algorithm, in the left-most \(m\) calculation stages \(S_n, \ldots, S_{n-m+1}\), called S-COMBS stages, symbol-based channel combinations are carried out. For the rest \((n-m)\) calculation stages \(S_{n-m}, \ldots, S_1\), called B-TRANS stages, the Arikan’s recursive channel transformations are performed. The S-COMBS stages use outputs of B-TRANS stages to calculate symbol-based messages.

For [22–24], we refer to the MFG as the DM-MFG which also consists of two parts; B-TRANS and DM-CAL. The B-TRANS part of the DM-MFG is the same as that of the SR-MFG. However, there is only one stage in the DM-CAL part of the DM-MFG which performs the direct-mapping calculation.

For example, as shown in Fig. 2, the SR-MFG of a four-bit symbol-decision SC algorithm for a polar code with \(N = 8\) has four stages. Messages of the initial stage \(S_0\) come from the channel directly. Messages of the first stage \(S_1\) are calculated with Arikan’s transformations. Messages of the second and third stages \(S_2\) and \(S_3\) are calculated with the DM-MFG which performs the direct-mapping calculation. Stages in the left gray box are the S-COMBS stages. Stages in the right gray box are the B-TRANS stages. Fig. 3 shows the DM-MFG when the direct-mapping calculation is used to calculate symbol-based channel transition probability \(W_{8,4}^{(1)}(y_8^8|u_1^1)\) and \(W_{8,4}^{(2)}(y_7^7,u_1^1|u_5^5)\). Here,

\[
\begin{align*}
v_1^4 &= u_1^1 \oplus v_1^1, \\
v_2^4 &= v_1^4 \oplus v_2^4 = u_1^1 \oplus u_2^2 \oplus u_3^3 \oplus u_4^4, \\
v_3^4 &= v_2^4 \oplus v_3^4 = u_2^2 \oplus u_3^3 \oplus u_7^7 \oplus u_8^8, \\
w_4^4 &= v_3^4 \oplus w_4^4 = u_3^3 \oplus u_4^4, \\
w_5^4 &= v_4^4 \oplus w_5^4 = u_4^4 \oplus u_8^8, \\
w_6^4 &= v_5^4 \oplus w_6^4 = u_5^5 \oplus u_8^8, \\
w_7^4 &= v_6^4 \oplus w_7^4 = u_6^6 \oplus u_8^8, \\
w_8^4 &= v_7^4 \oplus w_8^4 = u_7^7 \oplus u_8^8.
\end{align*}
\]

Fig. 3. The message flow graph of a four-bit symbol-decision SC algorithm for a polar code with a code length of eight by using direct-mapping calculation [22–24].

For the direct-mapping calculation, Eq. (7) needs \((M-1)\) additions. Therefore, a total of \(2^{\log_2(\frac{M}{2})}+(M-1)\) additions are needed to calculate all LL-based symbol-based channel transition probabilities for \(u_1^M|u_{M+1}^M\). Consider the recursive symbol-based channel combination. The S-COMBS stages of the SR-MFG are indexed as 1 to \(m\) from left to right. There are \(2^n-i\) nodes in the \(i\)-th S-COMBS stage and each node is \(2^{M+i-n}\) messages. One addition is needed to compute each LL message according to Eq. (9). Hence, the number of additions needed by the S-COMBS stages to calculate \(W_{N,M}^{(j)}(y_j^j,u_1^1|u_{jM+M-1}^{jM-M+1})\) is \(\sum_{i=1}^{m}2^{2^i}+2^{2\log_2(M)}\).

Actually, if we perform the hardware implementation, the worst case - that all bits of a symbol are information bits - should be considered. Therefore, the recursive symbol-based channel combination can be taken advantage of to reduce complexity of calculating the symbol-based channel transition probability.

For the example shown in Fig. 2, Eq. (7) needs \(2^4(4-1) = 48\) additions to calculate \(W_{8,4}^{(1)}(y_8^8|u_1^1)\). With the symbol-based channel combination, 4, 4 and 16 additions are needed to calculate \(W_{4,2}^{(1)}(y_4^4|v_7^7)\), \(W_{4,2}^{(1)}(v_6^6|v_5^5)\) and \(W_{8,4}^{(1)}(y_8^8|u_1^1)\), respectively. Therefore, our method needs only \(2^4 + 2 \times 2^2 = 24\) additions, which is only a half of those needed by Eq. (7). Table I lists the numbers of additions needed by our recursive method and direct-mapping calculation [22–24] when all \(M\) bits of a symbol are information bits. When \(M = 8\), the number of additions needed by our proposed method is 17% of that needed by the direct-mapping calculation.

**Table I**

| \(M\)  | Proposed method | Direct-mapping calculation [22–24] |
|-------|----------------|----------------------------------|
| 2     | 4              | 4                                |
| 4     | 24             | 48                               |
| 8     | 304            | 1792                             |

The other advantage of the proposed method to calculate the symbol-based channel transition probability is that it reveals the similarity between the Arikan’s recursive channel transformation and symbol-based recursive channel combination. We will take advantage of this similarity to reuse adders and to save area when computing the bit- and symbol-based channel
transitions in our proposed architecture. In [24],
additional dedicated adders are used to calculate the symbol-

In terms of the error performance, the symbol-decision SC
algorithm is not worse than the bit-decision SC algorithm
[27]. Fig. 4 shows the BERs and FERs of symbol-decision
SC algorithms for a (1024, 512) polar codes. SDSC-i

denotes the i-bit symbol-decision SC algorithm. When M = 2 and 4,
the FER performance is the same as that of the bit-decision
SC algorithm. When M = 8, the FER performance is slightly

better.

C. Generalized Symbol-Decision SCL Decoding Algorithm

Similarly, the symbol-based recursive channel combination
is also useful for the SCL algorithm. The symbol-decision
SCL algorithm is more complex than the SCL algorithm,
since the path expansion coefficient is not a constant any
more. In the SCL algorithm, for each information bit, the
path expansion coefficient is two. But for the M-bit symbol-decision
SCL algorithm, the path expansion coefficient is 2|M|, which depends on the number of information bits in
an M-bit symbol. The M-bit symbol-decision SCL algorithm is formally described in Alg. 3. Without any ambiguity, 0
represents a zero vector whose bit-width is determined by the
left-hand operator. The function dec2bin(d, b) converts a
decimal number d to a b-bit binary vector. Eq. (9) is used
to calculate the symbol-based channel transition probability

\[
W_{N,M}(\text{y}, (L_i)_i^{M-M-1})
\]

Eq. (9) is used
to calculate the symbol-based channel transition probability
corresponding to each list, i.e. \( W_{N,M}(\text{y}, (L_i)_i^{M-M-1}) \).

Fig. 5 shows the BERs and FERs of symbol-decision
SCL algorithms for a (1024, 480) CRC32-concatenated polar
code with \( L = 4 \) where the generator polynomial of the
CRC32 is 0x1EDC6F41. This CRC32 is also used in all the
CRC-concatenated polar codes used in the following section.
SDSC-i denotes the i-bit symbol-decision SCL algorithm.
The performances of the symbol-decision SCL algorithms with
different symbol sizes are almost the same.

Algorithm 3: M-bit Symbol-Decision SCL Decoding Algorithm

\[
\begin{align*}
\alpha &= 1; \\
\text{for } j = 1 : \frac{N}{M} &\text{ do} \\
\beta &= 2^{\lfloor AM_j \rfloor}; \\
\text{if } \beta == 1 &\text{ then} \\
\text{for } i = 1 : \alpha &\text{ do} \\
(L_i)_i^{M-M-1} &= 0; \\
\text{else if } \alpha \beta \leq L &\text{ then} \\
d_{AM_j} &= 0; \\
\text{for } k = 0 : \beta - 1 &\text{ do} \\
d_{AM_j} &= \text{dec2bin}(k, |AM_j|); \\
\text{for } i = 1 : L &\text{ do} \\
t = i + kM; \\
S[i].P &= \big| W_{N,M}(\text{y}, (L_i)_i^{M-M-1}) \big|; \\
S[i].L &= (L_i)_i^{M-M-1}; \\
S[i].U &= u_j^{M-M-1}; \\
\text{sortPDecrement}(S); \\
\text{for } i = 1 : L &\text{ do} \\
(L_i)_i^{M} &= \text{conc}(S[i].L, S[i].U); \\
\alpha &= \alpha \beta; \\
\text{end for} \\
\end{align*}
\]

Fig. 5. Error rates of symbol-decision SCL algorithms for a (1024, 480)
CRC32-concatenated polar code with \( L = 4 \).
D. Two-Stage List Pruning Network for Symbol-Decision SCL algorithm

For the $M$-bit symbol-decision SCL algorithm, the maximum path expansion coefficient is $2^M$, i.e. each existing path generates $2^M$ paths. Therefore, in the worst-case scenario, the $L$ most reliable paths should be selected out of $2^M L$ paths. To facilitate this sorting network, we propose a two-stage list pruning network. In the first stage, the $q$ most reliable paths are selected from up to $2^M$ paths that come from expansion of each existing path. Therefore, there are $qL$ paths left. In the second stage, the $L$ most reliable paths are sorted out from the $qL$ paths generate by the first stage. The message flow of a two-stage list pruning network is illustrated in Fig. 6.

![Fig. 6. Message flow for a two-stage list pruning network.](image)

If $q \geq L$, the $L$ paths found by the two-stage list pruning network are exactly the $L$ most reliable paths among the $2^M L$ paths. When $q < L$, the probability that the $L$ paths found by the two-stage list pruning network are exactly the $L$ most reliable paths among the $2^M L$ paths decreases as well. This may cause some performance loss. But a smaller $q$ leads to a two-stage list pruning network with lower complexity.

![Fig. 7. Error rates of the SDSCL-8 decoder for a (1024, 480) CRC32-concatenated polar code with $L = 4$.](image)

In Fig. 8 for a (2048,1401) CRC32-concatenated polar code, the two stage list-pruning network of $q = 4$ helps to reduce the complexity of the SDSCL-4 decoder without observed performance loss when $L = 8$. When $q = 2$ and $L = 8$, the SDSCL-4 decoder has a performance degradation of about 0.1 dB at an FER level of $10^{-3}$, compared with the SDSCL-4 decoder with $q = 8$ and $L = 8$. If $L = 4$, the error performance due to $q = 2$ is very small.

Therefore, the two-stage list pruning network uses an additional parameter $q$ to introduce different trade-offs between error performance and complexity.

IV. PRE-COMPUTATION MEMORY-SAVING TECHNIQUE

Pre-computation technique was first proposed in [25] and can be used to improve processing rate when the number of possible outputs is finite. In [17], the pre-computation technique is used to improve the throughput of the line SC decoder with an additional cost of increased area. Here, our main purpose is to use the pre-computation technique to reduce the memory required by list decoders because the memory of an SCL decoder to store the channel transition probability becomes a big challenge as the list size and code length increase. Henceforth, this memory saving technique is called the pre-computation memory-saving (PCMS) technique. It is worth noting that this memory-saving technique is independent of the decoder architecture and the message representation of SCL decoders.

Let us take the MFG shown in Fig. 2 as an example. For stages $S_0$ and $S_1$, the numbers of pairs of LLs stored by the list decoder are 8 and 4$L$, respectively. Actually, the outgoing message $W_{2,1}^{(1)}(y_1^2|w_1)$ of the top black node in $S_1$ can only be either $W_{2,1}^{(1)}(y_1^2|0)$ or $W_{2,1}^{(1)}(y_1^2|1)$. The outgoing message $W_{2,1}^{(2)}(y_1^2|w_1|w_2)$ can only be one of $W_{2,1}^{(2)}(y_1^2|0|0), W_{2,1}^{(2)}(y_1^2|0|1), W_{2,1}^{(2)}(y_1^2|1|0),$ and $W_{2,1}^{(2)}(y_1^2|1|1)$. Hence, no matter what the list size is, the total number of possible values of outgoing messages of $S_1$ is $2 \times 4 \times 4 \times 4 = 24$. These 24 values provide all information we need for calculations of
further stages. With knowledge of these 24 values, channel LLs are not needed any more.

Generally speaking, the PCMS technique takes advantage of the relationship between messages of $S_0$ (channel LLs), and outgoing messages of $S_1$. By storing only all possible outgoing messages of $S_1$, the PCMS technique helps list decoders save memory.

Let us evaluate the memory saving of the PCMS technique, assuming LL representation is used for the channel transition probability. Without PCMS technique, a list decoder for a polar code with the code length of $N$ has a list size of $L$ stores $(N-2)L + N$ LL pairs. Each pair contains two messages which are associated with the conditional bit being zero or one. The total number of bits used for LL storage is

$$B_{\text{LL}} = 2\left(NQ_{ch} + L \sum_{i=1}^{\log N - 1} 2^i(Q_{ch} + \log N - i)\right)$$

$$= 2(L+1)NQ_{ch} + 4L(N - \log N - Q_{ch} - 1),$$

where $Q_{ch}$ denotes the number of bits used for the quantization of the channel LLs.

With the PCMS technique, the total number of LL pairs needed by a list decoder is $\frac{N}{2}L + \frac{3}{2}N$. The total number of bits needed for LL storage is:

$$B_{\text{PCMS}} = 2\left(\frac{N}{2} + N\right)(Q_{ch} + 1) +$$

$$2L \sum_{i=1}^{\log N - 2} 2^i(Q_{ch} + \log N - i)$$

$$= 3N(Q_{ch} + 1) + LN(Q_{ch} + 3)$$

$$- 4L(\log N + Q_{ch} + 1)$$

$$= B_{\text{LL}} - N(LQ_{ch} + L - Q_{ch} - 3).$$

Therefore, when LL representation is used for messages, the PCMS technique saves $N(LQ_{ch} + L - Q_{ch} - 3)$ bits of memory. The saving is linear with both $N$ and $L$. Consider a polar code with $N = 1024$, a list decoder with $L = 4$ and $Q_{ch} = 4$. Without the PCMS technique, $B_{\text{LL}} = 57104$. With the PCMS technique, $B_{\text{PCMS}} = 43792$. The PCMS technique helps to save 13312 bits of memory, which is 23% of $B_{\text{LL}}$.

The other advantage of the PCMS technique is that it improves the throughput slightly because the messages of $S_1$ are already in the memory and don’t need to be calculated from the channel messages. For example, for a bit-decision semi-parallel SCL decoder with the list size of $L$, if the code length is $N$ and the number of processing units is $P$, the latency saving due to the PCMS technique is $\frac{NL}{P}$ clock cycles.

V. IMPLEMENTATION OF SYMBOL-DECISION SCL DECODERS

A. Architecture of Symbol-Decision SCL Decoders

We propose an architecture of an M-bit symbol-decision SCL decoder shown in Fig. 9. It consists of $M$ MPU blocks (MPU_0, MPU_1, ..., MPU_M-1), a list pruning network (LPN), a mask bit generator (MBG), a message-screening block (MSNG), a control block (CNTL), an output-list generator (OLG) and a CRC checker (CRCC).

An MPU block calculates messages for B-TRANS and S-COMBS messages and updates the partial-sum network by adopting blocks of the SCL decoder in [20]. The additions of S-COMBS stages are carried out by reusing the same hardware resource which is used to calculate messages of B-TRANS stages to reduce the area. Compared with the SCL decoder in [20], the MPU has neither path pruning unit nor the CRC checker. The other improvement for the MPU is that PCMS technique is used here. The architecture of an MPU is shown in Fig. 10. Channel messages are not needed any more due to the adoption of PCMS technique. L-MEM stores messages corresponding to stages of the MFG. For the stage $S_1$, MSEL selects the appropriate messages from L-MEM based on partial sum values and/or the type of calculation nodes. PUs are processing units to calculate LL messages. PSUs is used to update partial-sums. Isel selects messages from LMEM or OSel module for the crossbar (CB) module which chooses proper messages for PUs. OSel outputs messages to L-MEM for intermediate stages and output symbol-based messages to MSNG.
LMEM. Here, \( w_l \) and \( w_M \) are the partial sum for \( w_1 \) and \( w_4 \), respectively, belonging to path \( l \). The detailed information of other blocks in Fig. 10 can be found in [20] and will not be discussed in this paper.

The message-passing scheme in MFG of a polar code is in a serial way, which means that the calculation of a stage depends on the output of its previous stage. The PUs in [20] only carry out the B-TRANS additions. On the other hand, the S-COMBS stages need only additions and a processing unit has four adders. Therefore, in order to save hardware resources, the adders in the processing units is reused to calculate the symbol-based channel transition probability, after these processing units finish calculations for the B-TRANS stages. In other words, additions of both the B-TRANS and the S-COMBS stages are folded onto the same adders in the processing units. As shown in Fig. 11, \( c[0] \) and \( c[1] \) are outputs for the B-TRANS stages; \( d[0], d[1], d[2], \) and \( d[3] \) are outputs for the S-COMBS stages.

.Block MBG provides a mask bit for each path. If there are \( f \) frozen bits in the \( M \)-bit symbol, the number of expanded paths will be \( 2^M - f \). For hardware implementations, we need to consider the worst case and all messages corresponding to \( 2^M \) possible paths are calculated. Each path is associated with a mask bit. When some paths are not needed, due to frozen bits, they are turned off by mask bits. Fig. 12 shows how to generate the mask bit for path \( i \), where \( i = (i_1, i_2, \ldots, i_M) \in \{1, 0\}^M \) (\( 0 \leq i < 2^M - 1 \)) and \( b_j = (b_{j,1}, b_{j,2}, \ldots, b_{j,M}) \) is a frozen-bit indication vector for \( u_{j+1}^{M+1} \). If \( u_{j,M+1}^{M+1} \) is a frozen bit, \( b_{j,t} = 1 \). Otherwise, \( b_{j,t} = 0 \). If \( b_j \) is an all-one vector, all bits of \( u_{j,M+1}^{M+1} \) are frozen bits, called an \( M \)-bit frozen vector. If \( Mask_{bit_i} = 1 \), \( u_{j+1}^{M+1} \) is impossible to be \( i \) and the message corresponding to \( u_{j+1}^{M+1} \) = \( i \) is set to 0 in block MSNG.

Block LPN receives \( 2^M L \) messages from block MSNG, finds the most reliable \( L \) paths, and feeds decision results back to the MPUs. Here, we use two different sorting implementations – a folded sorting implementation and a tree sorting implementation – for different designs. The basic unit for these two implementations is a bitonic sorter [28], which outputs the \( L \) max values out of \( 2L \) inputs. It is referred to as BS_L. The folded sorting implementation needs \( 2^M - 1 \) BS_Ls (BS_L0, BS_L1, ..., BS_L_{2^M-1}). The outputs of the BS_L_{2i} and the BS_L_{2i+1}(0 \leq i < 2^M-2) are connected with inputs of BS_L_i through registers and multiplexers. For the tree sorting implementation with \( 2^M L \) inputs, \( 2^M - 1 \) BS_Ls are needed. The tree sorting implementation can be divided into \( M \) layers. For \( 0 \leq i < M \), there are \( 2^i \) BS_Ls in the \( i \)-th layer. Inputs of the BS_Ls of the \( i \)-th layer are connected with outputs of the BS_Ls of the \( (i + 1) \)-th layer. Fig. 13 and 14 show examples of the folded and tree sorting implementations, respectively, for \( 2^M = 8 \).

Fig. 11. Architecture of a processing unit.

Fig. 12. Architecture for generating a mask bit.

Fig. 13. Architecture for the folded sorting implementation when \( 2^M = 8 \).

Fig. 14. Architecture for the tree sorting implementation when \( 2^M = 8 \).

The folded sorting implementation has a smaller area than the tree sorting implementation. However, the pipeline can be applied to the tree sorting implementation by inserting registers between layers to improve the throughput of the tree sorting implementation.

For the two-stage list pruning network proposed in Sec. III-D, either the folded sorting implementation or the tree sorting implementation can be used for the \( 2^M \)-to-\( q \) sorting function and the \( qL \)-to-\( L \) sorting function.

Block CNTL provides control signals to schedule the hardware sharing for MPUs and decides when to start pruning paths. The signal frz_flag is an indicator which is one when a frozen vector appears. When frz_flag is one, all MPUs use
zero to update the partial-sums instead of outputs of the LPN. In this case, the LPN, the MSNG, and the calculation of S-COMBS stages are bypassed. The OLG stores the output paths. The CRC check if a path satisfies the CRC constraint.

**B. Message Scheduling and Latency Analysis**

To improve area efficiency, for different number of PUs, different scheduling schemes are needed. To reuse the adders of the processing units, the adders of the S-COMBS stages in the MFG must be scheduled properly. Assume the number of the processing units is \( P \). The total number of the adders provided by processing units is \( 4P \). If \( 2^M L \leq 4P \), we use a serial scheduling, which means that there is no overlap for the processing units and the LPN in terms of the operation time, as shown in Fig. 15.

![Fig. 15. Serial scheduling (in clock cycles).](image)

Suppose each addition takes one clock cycle. Then each S-COMBS stage takes one clock cycle to compute messages. Therefore, it takes \( m \) clock cycles for the S-COMBS stages to output messages to the LPN. To save the area, the folded sorting implementation is applied for the serial scheduling.

When \( 2^M L > 4P \geq 2^M2^\frac{M}{2} L \), there are not enough adders to calculate all \( 2^M L \) messages of the stage \( S_i \) in one clock cycle, but all \( 2^M2^{n-i} L \) messages of the stage \( S_i \) \((n+m-1 \leq i \leq n-1)\) can be calculated in one clock cycle. Without increasing the number of adders, \( 2^M L \) cycles are needed. In each cycle, \( 4P \) messages are calculated. To reduce the latency, the overlapping scheduling shown in Fig. 16 is used. In clock cycle \( c_0 \), the first \( 4P \) messages come out. In clock cycle \( c_1 \), the LPN starts work. Therefore, the MPUs and the LPN are working simultaneously for \( 2^M2^{\frac{M}{2}} \) clock cycles. Here, the LPN works in a pipeline way. Hence, the tree sorting implementation is deployed for the overlapping scheduling and a BS_L is connected at the end of the tree sorting implementation in a way shown in Fig. 17 where the number on a line represents the number of messages transmitted through the line.

![Fig. 16. Overlapping scheduling (in clock cycles).](image)

The latency of an \( M \)-bit symbol-decision SCL decoder consists of: the latency for calculating messages of the B-TRANS stages, the latency for calculating messages of the

**Fig. 17. A pipelined tree sorting implementation for the overlapping scheduling.**

S-COMBS stages, and the latency of the list pruning network. \( T_B \) represents the overall number of clock cycles for the calculations of the B-TRANS stages. It is equivalent to the latency of a bit-decision SCL decoder with a code length of \( \frac{N}{M} \) and \( \frac{D}{M} \) processing units:

\[
T_B = \frac{N}{M} \left( \frac{NL/M}{P/M} \log_2 \left( \frac{NL/M}{4P/M} \right) - \frac{NL/M}{P/M} \right),
\]

where the third term, \( \frac{NL/M}{P/M} \), is the latency saving by using PCMS technique. \( T_S \) represent the number of clock cycles for the calculations of S-COMBS stages per symbol. \( T_N \) represents the number of clock cycles needed by the LPN to finish the list pruning after all messages of the stage \( S_n \) are calculated. If \( 2^M L \leq 4P \), the number of clock cycles used to calculate messages for S-COMBS stages is \( T_S = m \). When \( 2^M L > 4P \geq 2^M2^\frac{M}{2} L \), \( T_S = m - 1 + \left[ \frac{2^M L}{4P} \right] \).

More generally, \( T_S \leq \sum_{i=1}^{m} \left[ \frac{2^M L}{4P} \right] \). \( T_N \) is determined by the detailed implementation. Hence, the latency of the symbol-decision SCL decoder is:

\[
T(M) = (1 - \gamma) \frac{N}{M} \left( T_S + T_N \right) + T_B
= (1 - \gamma) \frac{N}{M} \left( T_S + T_N \right) + 2 \frac{N}{M} + \frac{NL}{P} \log_2 \left( \frac{NL}{8P} \right),
\]

(12)

where \( \gamma \) is a ratio of the number of frozen vectors to \( \frac{N}{M} \).

Table II shows the latencies (in clock cycles) for different decoders to decode a (1024, 480) CRC32-concatenated polar code with 64 processing units and \( L = 4 \). We assume a BS_L needs one clock cycle to find the four maximum values out of eight values. For \( M = 2 \) and \( M = 4 \), a folded sorting implementation and the serial scheduling are used. For \( M = 8 \), a pipelined tree sorting implementation and the overlapped scheduling are applied. For \( M = 8 \) and \( q = 2 \), the basic unit in the tree sorting implementation is to find the two maximum values out of eight values, which needs one clock cycles. Therefore, \( T_N = 4 \) when \( M = 8 \) and \( q = 2 \).

![Table II Latencies for different decoders for a (1024, 480) CRC32-concatenated polar code with 64 processing units and \( L = 4 \).](image)

| Decoder | \( \gamma \) | \( T_S \) | \( T_N \) | \( q \) | Latency (\# of cycles) |
|---------|-------------|--------|--------|-----|-------------------|
| SDSCL-2 | 0.445       | 1      | 2      | 4   | 2069              |
| SDSCL-4 | 0.395       | 2      | 4      | 4   | 1634              |
| SDSCL-8 | 0.344       | 6      | 7      | 4   | 1340              |
| SDSCL-8 | 0.344       | 6      | 4      | 2   | 1288              |
The SDSCL-8 decoders provide a higher throughput and a smaller latency than the SDSCL-2 and SDSCL-4 decoders, and occupy larger areas. However the improvements on the throughput and latency are not linear in the symbol size.

Compared with the SCL decoder in [20], the increase of areas of symbol-decision SCL decoders is mainly due to sorting networks because the adders of processing units are reused to calculate both the bit- and symbol-based channel transition probabilities. For the SDSCL-4 decoder, because the sorting network of the SDSCL-4 decoder is only 0.073 mm², there is no need to shrink q further. For the SDSCL-8 decoders, when q = 4, the area of the sorting network is 0.454 mm². However, when q = 2, the sorting network occupies 0.196 mm² which is less than a half of that of q = 4. A smaller q does help the SDSCL-8 decoder achieve a higher throughput, a smaller latency, a smaller area, and a higher area efficiency, but it also introduces an FER performance loss of 0.25 dB to the SDSCL-8 decoder at an FER level of $10^{-3}$ as shown in Fig. 7.

Moreover, we also provide synthesis results for SDSCL-8 decoders without the PCMS technique. The PCMS technique helps the SDSCL-8 decoders gain an area saving of about 0.12 mm².

We've already mentioned that LL messages are used in our designs. If LLR messages [21] are used, symbol-decision SCL decoders can have better area efficiencies than our current designs because the memory requirement for LLR messages are fewer than that for LL messages [21].

VI. CONCLUSION

In this paper, we use the symbol-based recursive channel combination to calculate the symbol-based channel transition probability. We show that based on the LL representation of the transition probability, this recursive procedure needs fewer additions than the method used in [22], [24]. Furthermore, a two-stage list pruning network is proposed to simplify the L-path finding problem. We use the PCMS technique to reduce the memory requirement for list decoders. By applying the PCMS technique, we design an efficient architecture for symbol-decision SCL decoders. Specifically, we introduce two scheduling schemes to perform the hardware sharing. A folded sorting implementation and tree sorting implementation are also discussed. We also implement symbol-decision SCL polar decoders for two-bit, four-bit and eight-bit, respectively, with a list size of four. Our synthesis results show that symbol-decision SCL polar decoders outperform existing SCL polar decoders in terms of the area efficiency. Our proposed methods and architecture provide a range of tradeoffs between area, throughput and area efficiency.

ACKNOWLEDGMENT

We would like to thank the authors of [19] for providing the synthesis results using the TSMC 90nm technology in Table III.

C. Synthesis results

To implement the proposed symbol-decision SCL decoder, we consider only $M = 2, 4$ and $8$. For $M \geq 16$, it is impractical to build list pruning networks. For example, for the worst case of $M = 16$, all the bits of a symbol are information bits, there are $2^{16}L = 65536L$ paths. Even if $L = 1$, to find the maximum value among 65536 values still needs a huge amount of hardware resources and leads to a huge latency.

In our implementations, $L = 4$. Each implementation has 64 processing units. LL messages are used in our designs. The channel LL messages are quantized with 4 bits. A (1024, 480) CRC32-concatenated polar code is used. The synthesis tool is Cadence RTL compiler. The process technology is TSMC 90nm CMOS technology. Our proposed architectures are compared with the state-of-the-arts SCL architectures, in [19]–[21], [24], both bit- and symbol-decision algorithms. The synthesis results in [21] and [20] are also based on a TSMC 90nm CMOS technology. The original synthesis results of [19] and [24] are based on a UMC 90nm and ST 65nm CMOS technologies, respectively.

The synthesis results shown in Table III demonstrate that our symbol-decision SCL polar decoders have higher area efficiencies than the SCL decoders in [19], [20], [24], and [21]. The SCL decoders in [19], [21], [24] have higher clock rates than our designs because it uses registers as storage units. However, in our designs, register files are used.

It is claimed in [22] that the $M$-bit SDSCL decoder could have $M$ times faster decoding speed than the bit-decision SCL decoder, which is much better than our implementation results. Let us review Eq. (12) again. For a fair comparison, suppose the MPUs of the $M$-bit SDSCL decoder has the same architecture as the conventional SCL decoder. Then a conventional SCL decoder with the PCMS technique has a latency of $T(1) = 2N + \frac{NL}{M} \log_2 \frac{NL}{SP}$. The decoding speed gain of the $M$-bit SDSCL decoder is

$$\frac{T(1)}{T(M)} = \frac{2N + \frac{NL}{M} \log_2 \frac{NL}{SP}}{(1-\gamma) \left(\frac{NL}{M} (TS + TN) + (M-1) \frac{NL}{M} \log_2 \frac{NL}{SP}\right)}$$

$$= M - \frac{(1-\gamma)N(TS + TN) + (M-1) \frac{NL}{M} \log_2 \frac{NL}{SP}}{(1-\gamma) \left(\frac{NL}{M} (TS + TN) + 2 \frac{NL}{M} \log_2 \frac{NL}{SP}\right)}$$

(13)

To be exactly $M$ ($M \geq 1$) times faster, $(1-\gamma) \frac{NL}{M} (TS + TN) + (M-1) \frac{NL}{M} \log_2 \frac{NL}{SP}$ should be zero. For $NL > SP$, $T(1)/T(M) < M$, because $TS \geq 0$ and $TN \geq 0$. For $NL = SP$, $TS = TN = 0$ should be satisfied, which means that the calculation of the symbol-based channel transition probability and the list pruning procedure do NOT take any clock cycle. This is impractical. However, $TS$ and $TN$ cannot be zero in a practical design. If $NL < SP$ and $P < NL$, to achieve $M$ times faster, $(T_R + TN) = \frac{(M-1)L \log_2 \frac{NL}{SP}}{(1-\gamma)N} < 5(M-1)$, usually. Therefore, the statement about the decoding speed gain in [22] is too idealistic to be achieved in practice because the practical implementation needs some extra cycles to calculate the symbol-based channel transition probability and to perform the list pruning function.

The SDSCL-8 decoders have a higher throughput and a smaller latency than the SDSCL-2 and SDSCL-4 decoders, and occupy larger areas. However the improvements on the throughput and latency are not linear in the symbol size.
TABLE III
SYNTHESIS RESULTS FOR DIFFERENT DECODERS WITH $L=4$.

| Algorithm                  | Proposed Architectures | [24] | [20] | [19] | [19] | [21] |
|----------------------------|------------------------|------|------|------|------|------|
| $M$                        | Symbol-decision SCL    |      |      |      |      |      |
| 2                         | 4                      | 8    | 2    | 4    | N/A  | N/A  |
| Clock Rate (MHz)           |                        | 500  | 525  | 379  | 400  | 289  |
| Latency (us)               |                        | 4.14 | 3.27 | 3.08 | 3.21 | 2.58 |
| Throughput (Mbps)          |                        | 247  | 313  | 332  | 319  | 398  |
| Area (mm$^2$)              |                        | 1.126| 1.209| 1.669| 1.782| 1.403|
| Area eff. (MHz/mm$^2$)     |                        | 219.4| 259.2| 199.2| 179.1| 283.3|

$\dagger$ The synthesis result in [19] is based on a UMC 90nm CMOS technology.

$\ddagger$ Original synthesis results in [24] are based on an ST 65nm CMOS technology. For a fair comparison, synthesis results scaled to a 90nm technology are used in the comparison.

$\ast$ The design is without the PCMS technique.

APPENDIX

Proof of Proposition [7] According to the definition of conditional probability $Pr(B|A) = \frac{Pr(AB)}{Pr(A)}$,

$$W_{2_{\Lambda}(\phi)}^{(i+1)}(y_1, u_1^{\phi+1}, u_1) | u_1^{\phi+1}) = \frac{W_{2_{\Lambda}(\phi+1)}^{(i)}}{Pr(1_{\phi+1})}.\Pr_{1}(u_1^{\phi+1} | u_1^{\phi+1}).$$

Because all bits of $u$ are independent and each bit has an equal probability of being a 0 or 1,

$$Pr(1_{\phi+1} | u_1^{\phi+1}) = Pr(1_{\phi+1} | u_1^{\phi+1}) = 2^{(\phi+1)} - 1.$$

Therefore,

$$W_{2_{\Lambda}(\phi)}^{(i+1)}(y_1, u_1^{\phi+1}, u_1) | u_1^{\phi+1}) = 2^{(\phi+1)} - 1.$$

According to Eq. [5],

$$W_{2_{\Lambda}(\phi)}^{(i+1)}(y_1, u_1^{\phi+1}, u_1) | u_1^{\phi+1}) = \frac{1}{2} W_{2_{\Lambda}(\phi+1)}^{(i)}(y_1, u_1^{\phi+1} | u_1^{\phi+1}) \cdot W_{2_{\Lambda}(\phi+1)}^{(i)}(y_1, u_1^{\phi+1} | u_1^{\phi+1}).$$

Similarly, we have

$$W_{2_{\Lambda}(\phi+1)}^{(i+1)}(y_1, u_1^{\phi+1} | u_1^{\phi+1}) = 2^{(\phi+1)} - 1.$$

and

$$W_{2_{\Lambda}(\phi+1)}^{(i+1)}(y_1, u_1^{\phi+1} | u_1^{\phi+1}) = 2^{(\phi+1)} - 1.$$

Then, by equations [15] ~ [18], Eq. [9] is obtained.

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