**GaN power IC normally-on and normally-off transistors technology and simulation**

V I Egorkin¹, V A Bespalov¹, O B Kukhtyaeva¹, V E Zemlyakov¹, V V Kapaev¹,² and A A Zaitsev¹

¹National Research University of Electronic Technology, Moscow, Russia, 124498
²P.N. Lebedev Physical Institute of the Russian Academy of Sciences, Moscow, Russia, 119991

**Abstract.** GaN technology has been waiting to be widely adopted because of its specific technical requirements. Integration of transistor and driver in a single die will enable to overcome problems with gate driving, high cost of circuit and low device reliability. This paper demonstrates technology of GaN-on-Si normally-on and normally-off transistor with different p-GaN cap-layer thickness as well as simulation of these devices. The simulation data confirm experimental results. P-GaN cap-layer thickness affects the current channel density: the more p-GaN thickness, the less channel density. The fabricated transistors have a maximum drain current in open state of about 800 mA/mm.

1. Introduction

Gallium nitride (GaN) is excellent material for high switching speed and high-power semiconductor device applications due to its properties namely maximum electric field strength, wide band gap and high saturation electron drift velocity. GaN/Si heterostructure advantages are the ability to use large diameter wafers in the manufacture of nitride group devices, reduction of the device cost, relatively high thermal conductivity and the ability to integrate Si and GaN technology on the same substrate. Present GaN-on-Si technology allows to fabricate improved integral E-mode GaN transistors with high breakdown voltages. Due to the modern level of integration many active and passive devices can be manufactured on the same die as in a planar integral circuit (IC) process (Figure 1). These microcircuits have applications as AC/DC and DC/DC converters, switching power supplies etc. Monolithically driver integration solves problem with parasitic inductance in the gate driver loop. The parasitic inductance results in negative and positive gate spikes that can compromise the power FET reliability over time. Thus a monolithically integrated driver is so far the best solution.

There are many methods to form normally-off transistor namely recessed gate, fluorine treatment of the region under the gate, use of NiOx intermediate layer which after thermal treatment acquires p-type semiconductor properties and cascade configuration. In our opinion the perspective method is use of p-GaN or p-AlGaN layer under the gate. There are some methods to fabricate p-GaN layer: traditional selective RF etching, selective growth and hydrogen plasma treatment of p-GaN area not under the gate. In our previous work [1] we have managed to develop RF etching mode to etch p-GaN layer, heterostructure with additional AlN layer and the design process. AlN is a stop-layer at p-GaN etching and achieves a high energy barrier layer to suppress the leakage current induced by thermionic emission. Opportunity to form normally-on and normally-off transistors in a single die will enable to extend GaN electronic component base.
2. Experiment and simulation

For the experiment 40 nm p-GaN/1nm AlN/12nm AlGaN/1nm AlN/GaN/Si heterostructures were grown by MOCVD. The design process includes formation of alignment marks and isolation, then selective etching of p-GaN to form ohmic contacts and source and drain formation, gate metal deposition and then selective etching of p-GaN, passivation and first level metallisation (Figure 2). There are two ways to form isolation namely by ion implantation or by mesa-etching. Advantage of ion implantation is planarity that facilitates the transistor formation. In the design process gate metal is not heat treated that positively affects the gate region characteristics as p-GaN layer doesn’t degrade. Ti-Al-Ni-Au (20/100/40/30 nm) metallization is used for ohmic contacts. The gate metallization is V-Au. To fabricate p-GaN gate ICP etching process has been worked out. Also we have managed to learn to control of etched p-GaN thickness. Gas mixture containing chlorine and fluorine must be used in etching process (BCl$_3$+SF$_6$, BCl$_3$+CF$_4$ etc.). In this case AlF$_3$ and AlO$_x$ are formed at which etching process stops. To delete this dielectric layer the wafer should be treated in solution of HF/NH$_4$OH or in hydrochloric acid solution.

P-GaN layer provides normally-off behavior of the device but for certain construction. Based on [3] the constructions have been simulated. Simulation has been done with Sentaurus Technology Computer Aided Design (TCAD). Heterostructure with next parameters has been simulated: thicknesses of AlN layers are 1 nm, thickness of AlGaN barrier layer is 12 nm and Al mole fraction in it is 25%, thickness of p-GaN cap-layer is 40 nm (20nm and without p-GaN layer) and Mg concentration in it is about $10^{18}$ cm$^{-3}$. The Al mole fraction is more than in [3] as another task to form transistor with high drain current. Transistors with 1 um gate length, 1.5 um gate-to-source length, 3.5 um gate-to-drain length and different p-GaN thicknesses (40 nm, 20nm and 0nm) were created and simulated. It has been noticed p-GaN cap-layer thickness influences on the current channel density and on type of transistor accordingly (Figure 3, 4).

3. Results

According to the simulation and experiment it has been established the more p-GaN thickness is, the less channel density is (Figures 4, 5). Respectively p-GaN thickness affects the drain current at 0 V gate voltage (Figure 5). Figure 4 shows that minimal channel density is about $2.37 \times 10^{13}$ cm$^{-3}$ which corresponds to normally-on behaviour of device. Figure 3 shows dependence of threshold voltage
(Vth) on p-GaN layer thickness (t_p). Vth is a key parameter that determines transistor behaviour. Our task is to form normally-off transistor with threshold voltage of about 3 V.

The fabricated transistors are normally-on and have a maximum drain current 800 mA/mm in open state, different threshold voltages (from -3 to -2 V) and different drain currents in open state at 0V gate voltage. The experimental data confirm simulation ones (Figures 6-11). Therefore we have simulated the heterostructure with other parameters of layers to manufacture normally-off transistor.

![Figure 2](image1.png)

**Figure 2.** Design process and schematic cross-sectional view of p-GaN gate HEMT: a) GaN-on-Si heterostructure, b) isolation by ion implantation, c) selective etching of p-GaN to form ohmic contacts, d) formation of ohmic contacts and deposition of gate metal, e) etching of p-GaN to form gate.

![Figure 3](image2.png)

**Figure 3.** Dependence of threshold voltage (Vth) on p-GaN layer thickness (t_p).

![Figure 4](image3.png)

**Figure 4.** Dependence of channel carrier density (N_ch) on p-GaN layer thickness (t_p).
Figure 5. Current-voltage characteristics of HEMTs with different p-GaN layer thicknesses at gate voltage of 0 V.

Figure 6. TCAD current-voltage characteristics of the HEMT with 40 nm p-GaN.

Figure 7. Experimental current-voltage characteristics of the HEMT with 40 nm p-GaN.

Figure 8. TCAD current-voltage characteristics of the HEMT with 20 nm p-GaN.

Figure 9. Experimental current-voltage characteristics of the HEMT with 20 nm p-GaN.
4. Conclusion
This work demonstrates the first step to create GaN-on-Si planar IC. We have managed to form normally-off transistor in previous works and today we have managed to simulate and form normally-on transistors with various p-GaN gate thicknesses on a single substrate with our RF etching process. Our simulation results confirm experimental ones. As the simulation is right we have simulated different constructions of heterostructure for normally-off GaN transistor and we are going to form transistors of two types on a single die. Thus we have developed fabrication technology of monolithically integrated driver (normally-on transistor) and normally-off transistor.

Acknowledgments
This work was supported by the Ministry of education and science of the Russian Federation (“Technology development and technological preparation to manufacture transistor crystals based on gallium nitride heterostructures on a silicon substrate with diameter of 150 mm for power converter modules”, grant agreement № 075-11-2019-068 from November 26, 2019).

References
[1] Kukhtyaeva O B, Egorkin V I et al. 2019 Journal of Physics: Conference Series vol. 1410 (Saint-Petersburg, Russia) p.012192
[2] Giandalia M and Kinzer D 2019 PCIM Europe 2019: International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (Nuremberg, Germany)
[3] Chen K J, Haberlen O, Lidow A, Tsai Ch,Ueda T, Uemoto Y and Wu Y 2017 IEEE Trans. Electron Devices 64 779
[4] You S, Li X et al 2019 ESSDERC 2019 - 49th European Solid-State Device Research Conf. (ESSDERC) (Cracow, Poland) pp 158-61