Implementation of Basic and Universal Gates In a single Circuit Based On Quantum-dot Cellular Automata Using Multi-Layer Crossbar Wire

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Abstract: Quantum-dot Cellular Automata (QCA) is one of the most substitutes developing nanotechnologies for electronic circuits, as a result of lower force utilization, higher speed and smaller size in correlation with CMOS innovation. The essential devices, a Quantum-dot cell can be utilized to logic gates and wires. As it is the key building block on nanotechnology circuits. By applying simple gates, the hardware requirements for a QCA circuit can be decreased and circuits can be less complex as far as level, delay and cell check. This article exhibits an unobtrusive methodology for actualizing novel upgraded simple and universal gates, which can be connected to outline numerous variations of complex QCA circuits. Proposed gates are straightforward in structure and capable as far as implementing any digital circuits. The main aim is to build all basic and universal gates in a simple circuit with and without crossbar-wire. Simulation results and physical relations affirm its handiness in actualizing each advanced circuit.

Key Words: Nano-electronics, Quantum cellular automata, Majority logic, QCA designer.

1. INTRODUCTION

In last few decades, scaling the feature size and increasing the processing power have been successfully implemented by conventional lithography based on VLSI design [1]. As the CMOS technologies approach its basic physical points of confinement, there has been broad examination as of late being developed of nanotechnology for future era IC. Gordon Moore has anticipated, in 1965 that the limit of a PC chip would become exponentially with time. From that point forward, the purported Moore’s Law had represented the advancement and execution of microchips. Nanotechnology attracts much more attention from the researcher nowadays. As because the current CMOS technology faces different challenging problems like high power consumption and cannot ignored the difficulties in feature size reduction. A useful summarization report of future technologies has been published by ITRS [2]. Trusting on the unique properties of electronic devices at Nano level feature size, nanotechnology
unlocks new prospects for computing systems and devices. QCA proposed by Lent [3], is an emerging technology that offers an innovative approach for computing at nano-scale by monitoring the position of a single electron. QCA technology has feature like high speed, extremely low power, fast switching speed [4] and much more dense circuit [5], which increases clock frequency of logic circuits and decreases the size and estimated power consumption of those circuits [6]. XOR gate is presumably an imperative part of numerous advanced outlines of complex advanced circuits. The research article propose an advanced XOR gate by which any complex computerized circuit can be implemented, here we execute advanced parity checker circuit using crossbar multilayer. There are different clocking plans, for example, wave clocking which might be more reasonable for molecular QCA. Whatever remains of the research article is sorted out as takes after: In Section 2, the major of QCA innovation and outline methodologies is depicted including QCA clocking and QCA wire concept. Section 3 demonstrate the proposed work done over the earlier work. Segment 4 describes the design and simulation of combine gate using the multilayer gate as well as normal cell for QCA circuits. Section 5 concludes the paper.

2. QCA TECHNOLOGY AND DESIGN APPROACHES

Quantum technology has gradually applied in various fields, Quantum dot cellular automata are projected as a promising nanotechnology for future nano ICs. QCA technology is based on the interaction of bi-stable [7], [8] QCA cells constructed from four quantum dots. The cell is accused of the assistance of two free electrons which are able to tunnel between adjacent dots. These electrons have a tendency to possess antipodal destinations accordingly of their common electrostatic repulsion. Along these lines there exist two proportional enthusiastically negligible courses of action of the two electrons in the QCA cell, however no current directed out of the cell [9], [10] as appeared in Fig. 1.

2.1 QCA Logic Device

These arrangements are denoted as cell polarization P=+1 and P=-1, these two cell polarization P= +1 which represents "1" and P= -1 represents "0", binary information is encoded in the charge configuration of the QCA cell [11], [12]. Not at all like conventional logic circuits in which data is exchanged by electrical current, QCA works by the Columbic communication that associates the condition of one cell to the condition of its neighbours, which results as data change. One of the essential logic gates in QCA is the majority voter (MV).

The essential logic function in majority voter is shown in (1). MV can be acknowledged by just five QCA cells, as appeared in Figure 2(a) and 2(b) shown the logical block diagram of a majority gate.
$MV(A, B, C) = AB + BC + CA$ \hfill (1)

Logical AND (Fig. 3 (a)) and OR (Fig. 3 (b)) function can be implemented from the majority voter by fixing one input (control input) permanently to a 0 or 1. The inverter is another one basic gate in QCA and is shown in Fig. 3(c).
A few favourable circumstances can get utilizing QCA technology as it “edge driven” means information is conveyed to an edge of a QCA block, that is assessed and yield at another edge. This moreover implies that no electrical cables need be steered inside. QCA frameworks ought to be low power, in light of the fact that there is no current flowing. Sufficiently just vitality needs to add to lift the electrons from their ground states. The required space for a circuit is little as in light of the fact that the extent of QCA cells are exceptionally little.

2.2 QCA Wire
A wire is implemented in QCA with a linear array of cells. A simple, 5-cell QCA wire is shown in Figure 4.

Fig.5 shows our simulation results for the QCA wire. The wire is by far the most robust circuit element, with correct operation in the presence of a displacement of up to 12.5%. These results indicate that the simple geometry of the wire has a beneficial effect on the fault tolerance. The primary fault with such a wire results from the addition of unwanted inversion as cells are displaced to the point where the kink energy that couples them goes from a positive to a negative value. Each cell that is coupled to its neighbor with a negative kink energy essentially acts as an inverter. On the other hand, two inverters in series cancel the fault.
2.3 COPLANAR AND MULTI-LAYER CROSSOVER:

We have also investigated the tolerance of the so-called coplanar crossover, which is a signal crossing building block used in QCA circuits that operate on a four phase clock. The coplanar crossover can, under some circumstances, cross signals on one planar layer by taking advantage of certain symmetries between rotated and non-rotated cells. If these cells are perfectly realized, it can be shown that when placed adjacent to each other there will be no crosstalk between them, as shown in Fig. 6.

Previous work has also examined the possibility of multi-layer QCA [Gin et al. 1999]. Using these multi-layer QCA circuits we can effectively cross signals over on another layer. To do this, we require a vertical interconnect. By stacking cells one on top of another we can transmit the signal to another layer where the signal is again transmitted horizontally. The multi-layer crossover is shown in Fig. 6(c).

There are two intermediate layers of cells to prevent any possible crosstalk between the two interconnects. For the multi-layer crossover simulations, the layer-to-layer separation was chosen to be 0.575 nm, 2.875 nm, 5.75 nm, and 11.5 nm for the 1 nm, 5 nm, 10 nm, and 20 nm cells respectively. The Coulombic interaction between stacked cells forces the cells in between to tend to the opposite polarization of the layers above and below.
Unlike present CMOS integrated circuits, where metal layers are used to connect discontinuous sections of a circuit and cannot perform any logic functions, the extra layers of QCA are no different from the base layer. Cells lying in the extra layers are governed by the same Columbic interactions as those lying in the base layer. Thus, extra layers can accommodate computational circuit elements, not just wires. In this way, we believe that multi-layer QCA circuits can be made to consume significantly less area as compared to planar circuits. The layout for the coplanar crossover circuit is shown in Fig. 6(d), whereas the multi-layer crossover circuit is shown in Fig. 6(e).

The simulation results for the coplanar crossover and the multi-layer crossover. Our simulation results indicate that each multi-layer circuit is significantly more fault tolerant than the equivalent coplanar crossover. The very poor performance of the coplanar crossover can be understood in terms of crosstalk between the vertical and horizontal wires. Given a perfect layout, the crosstalk between the two interconnects is zero. The single cell gap in the crossover wire drops the overall coupling between the two horizontal sections by a factor of $1/3232$. The weak coupling renders the nearly floating output section of the horizontal interconnect highly sensitive to crosstalk. Even the smallest displacement can result in sufficient crosstalk between the two interconnects to cause the circuit to operate incorrectly. The robustness of the multi-layer crossover arises from the fact that there are no gaps anywhere along the length of the interconnects, and therefore none of the sections of interconnect are loosely coupled to each other.
Although this building block presents a solution to crossing signals, it may be very difficult to realize in practice. Our objective in this work is not to evaluate the feasibility of such a building block. We are primarily interested in demonstrating that there are options available that will increase the overall displacement tolerance of the coplanar crossover[16].

A wire is implemented in QCA with a linear array of cells. A simple, 5-cell QCA wire is shown in Figure 7.

Fig. 8 shows our simulation results for the QCA wire. The wire is by far the most robust circuit element, with correct operation in the presence of a displacement of up to 12.5%. These results indicate that the simple geometry of the wire has a beneficial effect on the fault tolerance. The primary fault with such a wire results from the addition of unwanted inversion as cells are displaced to the point where the kink energy that couples them goes from a positive to a negative value. Each cell that is coupled to its neighbor with a negative kink energy essentially acts as an inverter. On the other hand, two inverters in series cancel the fault.

Figure 8: Displacement simulation results for the QCA wire.
2.4 QCA CLOCKING

Clocking is performed in one of two ways: zone clocking and continuous clocking. In zone clocking [15], each QCA cell is clocked using a four-phase clocking scheme as shown in Figure 9. The four phases correspond to switch, hold, and release and relax. In the switch phase, cells begin un-polarized and with low potential barriers but the barriers are raised during this phase. In the hold phase, the barriers are held high while in the release phase, the barriers are lowered. In the last phase, namely relax, the barriers remain lowered and keep the cells in an un-polarized state. An alternative to zone clocking, called continuous clocking, involves generation of a potential field by a system of submerged electrodes. The former clocking scheme is adopted in this paper since the CAD tool used for simulation supports zone clocking and further, prior works on adders are only based on this clocking scheme. Primitives in the QCA model consist of a wire, inverter and majority gate.

![Figure 9: QCA clock zones.](image)

3. PROPOSED WORK

In this study we implement a QCA design for realisation of all gates using both simple cellular-dot automata and also using multi-layer crossover circuit. The novelty of this gate besides parameter like delay, number of cell count, majority gate and area is minimal in comparison to most other designs. Attempt is taken to design all the basic and universal gates with minimum cell count shown in figure 10(a) and 10(b). The comparison between various parameter of the circuit such as no. of cell count, time delay and total area consumption with the work available in literature has shown positive results. Complexity in terms of cell count, delay and area of QCA circuit can obtained by QCA Designer. The result indicate that no. of cell count is considerably low in our design shown in figure 10(c).
4. SIMULATION

Fig 10(a): Realisation of all gates using simple QCA circuit.

Fig 10(b): Realisation of all gates using simple QCA circuit with multi-layer crossover.

Fig 10(c): All gate simulation results.
5. CONCLUSION

This article represents the design, implementation and simulation of basic and universal gates in a single circuit using quantum-dot cellular automata with multilayer crossover. This design is efficient in terms of cell count, area. Moreover, considering the less numbers of cell count, area and power consumption.

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