Performance Characterization of Dual-Metal Triple- Gate-Dielectric (DM_TGD) Tunnel Field Effect Transistor (TFET)

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Abstract: Since, Dual Metal Gate (DMG) technology alone is not enough to rectify the problem of low ON current and large ambipolar current in the TFET, therefore, a novel TFET structure, known as dual metal triple-gate-dielectric (DM_TGD) TFET, has been proposed. We have combined the dielectric and gate material work function engineering to enhance the performance of the conventional FET. In the proposed structure, the gate region is divided into three dielectric materials: TiO₂/AI₂O₃/SiO₂. This approach is chosen because high dielectric material alone near the source cannot improve the performance due to increase in fringing fields. This paper presents the detail processing of the proposed structure. We have evaluated and optimized the dc performance of the proposed N-DM_TGD TFET with the help of 2-D ATLAS simulator. The results were compared with those exhibited by dual metal hetero-gate-dielectric TFET, single metal hetero- gate-dielectric TFET and single metal triple-gate-dielectric TFET of identical dimensions. It has been observed that the DM_TGD device offers better transconductance (gm), lower subthreshold slope, lower ambipolar current and larger ON current.

Keywords: Dual metal gate, Dielectric material, TFET, Subthreshold swing, DIBL, Ambipolar current, ON current.

1. INTRODUCTION

Earlier, miniaturization of MOSFET was the effective way to improve the performance of the circuit but in post scaling era the miniaturization of device is not becoming effective due to increased leakage current and short channel effects (SCEs) [1-3]. To overcome these limitations, researchers have proposed many different structures rather than planar in the literature [4-6] particularly multi gates devices and devices fabricated using different materials to replace the standard CMOS technology [7-9]. In nanoscale era, leakage current is major problem in the device which modifies the stable performance of the devices; therefore, suppression of leakage current without compromising the ON current is the major challenge. To control the leakage current, nanowire transistors have been proposed [10-12]. Among these, tunnel field-effect- transistors (TFETs) are considered one of the future devices to replace the planar MOSFETs [13-14]. Although TFET, possess lower subthreshold slope (SS) (< 60 mV/decade) at room temperature, but still, suffers from two main drawbacks; lower ON current and larger ambipolar current [15-16]. The ON current of TFET device can be increased by using high k-dielectric material as a gate insulator [17] on the cost of increased lamb whereas TFET with gate-drain overlap structure have been proposed to reduce ambipolar current [18] on the cost of reduced chip density. In literature, hetero- dielectric gate (HDG) TFET is proposed to overcome these two shortcomings after using a high-k material partially near source to enhance the ON current and SiO₂ near drain to suppress the ambipolar current [19]. Although, HfO₂ has a reasonably high dielectric constant (~25) and a relatively large band gap (5.68 eV) but it is very difficult to convert pure HfO₂ from amorphous to polycrystalline structure during the post- annealing treatment and also having poor interface quality with Si [20] which can be improved by incorporation of nitrogen in HfO₂ on the cost of lower dielectric constant [22]. Due to these reasons, the application of other metal oxides, with a dielectric constant higher than 25, in TFET device is very important. Titanium dioxide (TiO₂) appears as one of the alternative gate dielectric material to replace HfO₂ even though it has relatively small band gap (3.5 eV) [22]. Since, it is difficult to find a single oxide which satisfies high dielectric constant, low interface trap density, high thermal stability, for future gate dielectric, hence bilayer gate dielectrics is an alternative option. Researchers have used titania and alumina as reinforcements to improve the dielectric constant [23].
In the proposed structure, we have chosen TiO$_2$/Al$_2$O$_3$ dielectric materials near the source and SiO$_2$ near drain [24]. According to researchers [25-26], dual metal gate (DMG) structures, having different work function metals (tunneling gate near source and auxiliary gate near drain), are effective way to reduce SCEs in the TFET device without any adverse effect. By considering the advantages associated with heterogeneous dielectric and DMG, this paper presents the combination of both engineering aspects to improve the performance of the TFET. The structure of this paper is given as follows: Section II describes the device structure, and the process flow steps. Section III describes the simulation results and discussion whereas section IV concludes the paper.

2. DEVICE STRUCTURE AND PROCESS FLOW

The processing of the proposed structure (Figure 1(a)) has been done using 2-D Silvaco ATHENA and ATLAS. The process steps follow the standard CMOS process in which P- type (100) SOI structure (tsoi=10 nm, tbox=3 nm) has been chosen to restrict the leakage current. On the top of intrinsic silicon oxide layer has been grown. The asymmetric source and drain doping profiles are obtained by ion implantation of boron dose of 1.0e20 cm$^{-2}$ at 1 KeV (Figure 1(b)(i)) and phosphorous dose of 1.0e18 cm$^{-2}$ at 5 KeV (Figure 1(b)) using nitride mask layer. This also results in steep junction profile as shown in Figure 1(b)(ii). Since, the proposed structure’s gate has been divided into three dielectric materials of thickness of 3 nm, we have first deposited TiO$_2$ near source (Figure 1(c)), second dielectric layer of Al$_2$O$_3$ is deposited using atomic layer deposition (ALD) (Figure 1(d)) and finally third layer of...
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SiO$_2$, near drain, is deposited. After depositing each dielectric material on gate, we have performed selective etching to remove the unwanted layer (Figure 1(e)). The first gate material is etched with a carefully controlled manner and then a second gate material is formed using conventional deposition process. The thickness of auxiliary gate and tunneling gate is 5-nm (Figure 1(f)). Next, using PECVD process, we have formed sidewall spacer after deposition and etching of TEOS layer. We have used sputtering method to put Al-metal on the gate and at the source and drain contacts. Metal pads are defined by photolithography and etch process. The overall fabricated structure of the proposed device is shown in Figure 1(g) [24].

3. SIMULATION RESULTS AND DISCUSSION

We have performed simulations of the proposed structure using 2-D Silvaco ATLAS tool. We have considered the non-local BTBT model, the band gap narrowing model, Fermi-Dirac statistics, Shockley-
Read-Hall (SRH) recombination and Lombardi mobility model during simulation. The values of various parameters during simulation were taken as; gate length $L_g (L_{TiO_2} + L_{Al_2O_3} + L_{SiO_2})= 60 \text{ nm}$, work function of two gate metals are 3.9 eV and 4.3 eV, $t_{ox}= 3 \text{ nm}$, $t_{si}= 10 \text{ nm}$ (hence quantum mechanical effect has been ignored in this study). ON-current ($I_{on}$) in this paper has measured as the drain current when $V_{gs}=V_{ds}= 1 \text{ V}$ whereas ambipolar current ($I_{amb}$) is defined as the drain current when $V_{gs}= -0.2 \text{ V}$ and $V_{ds}= 1 \text{ V}$.

Table 1 gives the simulation results for various combinations of triple dielectric materials as an insulator for the proposed structure at $V_{ds}= 1 \text{ V}$ and $L_{high}$

(\text{ZrO}_2/\text{Al}_2\text{O}_3/\text{SiO}_2)= 20 \text{ nm, } L_{Al_2O_3}=10 \text{ nm and } L_{SiO_2}=30 \text{ nm, } L_{tunnel}=L_{aux}=30 \text{ nm}. \text{ From simulation results, it is observed that TiO}_2/\text{Al}_2\text{O}_3/\text{SiO}_2 \text{ combination as a gate insulator gives about 10% decrease in subthreshold swing SS, significant increase in ON-current and reduction in ambipolar current compared to other combination. These improvements are due to reduced EOT which results in better gate coupling at the source-channel interface and lower leakage current.}

Due to the better performance in terms of ON current, ambipolar current and SS, we have chosen TiO$_2$/Al$_2$O$_3$/SiO$_2$ as a gate insulator for the further investigation of the electrical performance of DM_TGD TFET.

From simulation results, it has been observed that when $L_{TiO_2}=20 \text{ nm, } L_{Al_2O_3}=10 \text{ nm and } L_{SiO_2}=30 \text{ nm}$, larger ON current and lower ambipolar current results in proposed structure. This is due to fact that as $L_{TiO_2}$ decreases, the conduction band (CB) well becomes shallower which makes band-to-band tunneling difficult to occur. Therefore, $L_{TiO_2}=20 \text{ nm}$ is the better choice for the performance improvement. After selecting the proper dielectric lengths, we simulated the TFET for optimizing the lengths of tunnel gate and auxiliary gate.

In TFETs, the electric field plays a very vital role in improving the ON current of the device. As the electric field increases at the tunnel junction, the tunneling probability of the electrons increases, thereby resulting in larger tunneling current. Figure 2(a) shows that the peak electric field occurs near the tunneling junction irrespective of the choice of auxiliary and tunneling

Table 1: Comparison of SS, lamb and ION for Three Different Combinations of Dielectric Materials

| Type of Combination       | Average SS (mV/Decade) | lamb (pA/µm) | ION (µA/µm) |
|---------------------------|------------------------|--------------|-------------|
| ZrO$_2$/Al$_2$O$_3$/SiO$_2$| 47.2                   | 1.82         | 7.6$\times 10^{-2}$ |
| HfO$_2$/Al$_2$O$_3$/SiO$_2$| 47.3                   | 1.82         | 7.6$\times 10^{-2}$ |
| Proposed (TiO$_2$/Al$_2$O$_3$/SiO$_2$) | 42.7                   | 0.181        | 1.11        |
| TiO$_2$/ZrO$_2$/SiO$_2$   | 42.8                   | 1.82         | 1.04        |
| TiO$_2$/HfO$_2$/SiO$_2$   | 42.8                   | 1.82         | 1.04        |

![Electric Field](image1.png)

**Figure 2 (a):** Lateral electric field for different tunnel gate and auxiliary gate lengths.

![Band Diagram](image2.png)

**Figure 2(b):** Band diagram for different combinations of tunnel length and auxiliary length.
lengths. It is also observed that when $L_{\text{tunnel}}=40\ \text{nm}$ and $L_{\text{aux}}=20\ \text{nm}$, electric field takes lower value compared to the other combinations near the drain which suppress the ambipolar current in the device. The larger electric field near the source-channel junction narrows the tunneling width as shown in Figure 2(b) which results in larger tunneling current (Figure 2(c)).

![Figure 2(c): ON current for different combinations of tunnel and auxiliary lengths.](image)

The variation of ambipolar current ($I_{\text{amb}}$) with $V_{gs}$ for different tunnel-gate work function is shown in Figure 2(d). The lower work function metal near source increases the band overlap which result in increased tunneling probability of electrons from valence band to conduction band of the channel.

**Performance Comparison**

After selecting the optimized values of the parameters, we have compared our proposed structure with dual metal hetero-gate-dielectric TFET and the results of various electrical performances are given in Table 2. The proposed device gives higher ON current, lower subthreshold slope and ambipolar current compared to the dual metal hetero-gate dielectric TFET due to high effective dielectric constant, high interface quality and reduced insulating barrier near the source-channel junction which increases the probability of tunneling.

| Different Combinations       | $SS$ (mV/decade) | $I_{\text{amb}}$ (pA/µm) | $I_{\text{on}}$ (mA/µm) |
|------------------------------|------------------|--------------------------|--------------------------|
| Proposed (TiO$_2$-Al$_2$O$_3$-SiO$_2$) | 42.7             | 0.181                    | 11.01                    |
| DMGHD (TiO$_2$-SiO$_2$)      | 56               | 1.3                      | 10.10                    |
| DMGHD (HfO$_2$-SiO$_2$)      | 47               | 0.6                      | 7.60                     |
| DMGHD Stack                  | 77               | 16                       | 1.80                     |

![Figure 3(a): Band Diagram for various TFET structures.](image)
Hetero increases the ON current compared to the dual metal dielectric and gate engineering approach not only reduced short ambipolar tunnel configuration is presented for the suppression of Hetero as lower trap channel junction and controlled leakage current as well as lower trap density.

Transconductance of the device plays a crucial role in determining the cut-off frequency. The variation in transconductance w.r.t. the gate voltage is shown in Figure 3(c). The proposed TFET structure exhibits higher transconductance compared to the single metal/dual metal hetero-gate-dielectric TFET because of increase in tunnelling probability at the source-channel junction and controlled leakage current as well as lower trap density.

Figure 3(b): ION comparison for different structures.

Figure 3(c): Variation of gm with Vgs for proposed and Hetero-dielectric TFETs.

4. CONCLUSION

A TFET device with dual metal triple-gate-dielectric tunnel configuration is presented for the suppression of ambipolar current with improved ON current and reduced short channel effects. The combination of dielectric and gate engineering approach not only increases the ON current compared to the dual metal hetero-gate-dielectric TFET but also reduces ambipolar current, enhances the transconductance and reduces the threshold voltage. The device is fabricated with 2-D Silvaco ATHENA tools based on the optimized parameters and simulated with ATLAS simulator. The choice of lateral combination of TiO2 and Al2O3 side by side as a gate insulator near source reduces the fringe field and enhances the coupling between gate and source which results in increase of the ON current. The dielectric combination near the source also reduces the insulating barrier, trap charge density at the source and produces the high interface quality with reduced leakage current. In future it is required to develop compact analytical models to characterize the proposed structure. These models should be incorporated into spice simulator for deep understanding of the proposed device.

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