Schottky-like barrier characterization of field-effect transistors with multiple quasi-ballistic channels

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The potential barrier height at the interface formed by a metal contact and multiple one-dimensional (1D) quasi-ballistic channels in field-effect transistors (FETs) is evaluated across different carbon nanotube and nanowire device technologies by means of a Landauer-Büttiker-based extraction methodology (LBM) adapted for multiple 1D-channels. The extraction methodology yields values for an effective Schottky barrier height and a gate coupling coefficient, an indicator of the device working at the quantum capacitance limit. The novel LBM-based approach embracing the mechanisms in 1D electronics is compared to the conventional activation energy method not considering such effects. The latter approach underestimates the potential barrier height at metal-channel interfaces in comparison to the novel methodology. A test structure based on a displaced gate device is proposed based on numerical device simulation results towards an improved accuracy of the method.

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I. INTRODUCTION

One-dimensional (1D) field-effect transistor (FET) technologies embrace devices with quasi-ballistic materials and structures as the channel such as carbon nanotubes (CNTs) and nanowires (NWs). Single-tube and single-wire FETs have been useful to understand the corresponding device physics. Transistors with an array of CNTs or NWs as channel have been demonstrated to be suitable candidates for practical low-power high-performance applications. The latter has been boosted by sophisticated techniques developed towards the integration of 1D-arrays-based devices in industry fabrication processes.

In contrast to single-1D-channel devices, multi-tube (MT) or multi-wire (MW) transistors present improved overall device characteristics, e.g., higher driving current capabilities and dynamic figures of merit. However, discussions on transport and injection phenomena in 1D FETs with an array of multiple channels are scarce in the literature. In order to improve 1D electronics technologies, a better understanding of the internal phenomena at metal-1D-channel interfaces within the same device, enabled by a reliable characterization, is required.

The interface characteristics at the metal contact regions and the 1D channel have a significant impact on the device performance. An important characteristic of this interface is the potential barrier height $\Phi_{BH}$ dominated by a Schottky-like barrier height $\Phi_{SB}$ (cf. Figs. (b), (c)). The latter is enabled by the different electronic properties between the tube/wire portions embedded within the metal contact and the uncoated 1D-channel. A weak Fermi level pinning at such interfaces prevents the evaluation of $\Phi_{SB}$ with the Schottky-Mott approach and hence, extraction methods are required for its characterization.

The activation energy method (AEM), originally developed in the context of conventional semiconductor devices, has been used to obtain $\Phi_{SB}$ values in multi-1D FETs in the literature. However, AEM does not cover the physics within the metal-1D-channel interface and it underestimates $\Phi_{SB}$ in contrast to an extraction methodology embracing 1D transport as shown elsewhere for devices with single and multi-1D channels. The latter methodology is identified as the 1D Landauer-Büttiker-equation based method (1D LBM).

In this work, 1D LBM is discussed in detail considering the transport in multi-1D-FETs in contrast to a previous work, where an interpretation of the underlying transport characteristics is missing. Contact interfaces of fabricated CNT- and NW-FET technologies are characterized with 1D-LBM here. Asymmetric gate devices are further investigated with a numerical device
simulator in order to show the impact of the electrostatics on the accuracy of the extracted value.

II. TRANSPORT INJECTION MECHANISMS AND 1D-LBM IN MULTI-1D FETS

A phenomenological analysis of the transport in multi-1D-channel devices is given next by considering that (i) screening effects due to tube/wire interactions are negligible and (ii) there are not Schottky points within the channel. The first can be fulfilled in devices with a relaxed pitch \[14,16\], whereas the latter is achieved in devices with tubes/wires properly aligned, a technology condition achievable for both CNTFET\[31\] and NWFET\[32\] technologies.

In aligned multi-CNT/NW-FETs, the carrier transport can be approximately described by a parallel network of quasi-ballistic channels as qualitatively depicted in Fig. 1(a) where the drain currents flowing through each channel \(I_{D,j}\) have been indicated. For devices with identical parallel channels, the overall transport injection mechanisms can be considered similar to the single-1D-channel Schottky FET, i.e., thermionic and tunneling transport are enabled by \(\Phi_{BH}\) before and after flat-band conditions have been reached as shown with the sketch of the conduction energy band in Fig. 1(b). In practice however, technological variations in the tubes/wires during the fabrication process, e.g., different tube/wire diameters, can lead to non-homogeneous metal-channel interfaces within the same device. The latter has been observed for both CNTFETs and NWFETs where tube/wire diameters impact on \(\Phi_{BH}\)\[25,33-36\]. Hence, the individual flat-band conditions, and hence \(\Phi_{SB}\), differ among the 1D-channels in devices with non-identical contact interface properties. As observed in Fig. 1(c), a 1D-channel-related \(\Phi_{SB1}\) lower than other \(\Phi_{SB2}\) within the same device lead to pure thermionic injection for the whole device at the flat-band condition corresponding to the first channel (CNT\(_1\)/NW\(_1\)), however, tunneling injection is enabled for the first channel at the same bias at which only thermionic current occurs in the second channel (CNT\(_2\)/NW\(_2\)) due to its corresponding flat-band conditions. The characterization of \(\Phi_{SB}\) for each 1D-channel in multtube/multiwire is not trivial due to the different transport injection mechanisms discussed above. Nevertheless, for the overall device performance, the transport injection can be described by an effective \(\Phi_{BH}\) under certain considerations (cf. (i) and (ii) at the beginning of this section).

The total drain current \(I_D\) of multi-1D-FETs at the subthreshold regime can be approximately described as the sum of the individual quasi-ballistic current, given by the 1D-Landauer-Büttiker approach\[29,37\], through each parallel path such as
FIG. 1. (a) Schematic device structure (not at scale) of a buried gate multi-1D channel FET with perfectly aligned \( j \)-tubes/wires. Sketch of the conduction band diagram at different \( V_{GS} \) for an \( n \)-type multi-1D FET considering metal-tubes/wires interfaces with (b) identical and (c) different properties. Each pair of curves in (b) corresponds to one CNT/NW. A top-gate contact (G) is shown in (b) and (c) in order to ease the identification of the gated-channel region. \( E_{F,s/d} \) is the Fermi energy level at the source/drain contact. \( V_{FB} \) is a flat-band voltage and \( I_{th} \) and \( I_{tun} \) are the thermionic and tunneling current, respectively.

\[
I_D = \sum_{j=1}^{n_{t/w}} I_{D,j} \\
\approx \eta \sum_{j=1}^{n_{t/w}} \left\{ \exp \left[ \frac{n_{g,j}}{V_t} (V_{GS} - V_{ot,j}) - \frac{\Phi_{BH,eff} V_t}{V_t} + \frac{n_{d,j} V_{DS}}{V_t} \right] \right\},
\]

where \( n_{t/w} \) is the total number of tubes/wires, \( \eta = (4q^2/h)V_t \) is a constant with \( q \) as the electronic charge and \( h \) as the Planck constant, \( V_t = k_B T/q \) is the thermal voltage with \( k_B \) as the Boltzmann constant and \( T \) the absolute temperature, \( n_g \) and \( n_d \) are gate and drain coupling coefficients, respectively, \( V_{GS} \) and \( V_{DS} \) are the gate-to-source and drain-to-source voltage, and \( \Phi_{BH,eff} \) is an effective potential barrier height at which pure thermionic injection occurs in the multi-1D device. \( V_{ot} \) is the voltage indicating the onset of tunneling mechanisms which in single-tube/wire devices corresponds to the flatband voltage \( V_{FB} \). Eq. (1) has been obtained by considering that the thermionic transmission probability \( T \) is equal to one as expected for sub-\( \mu \)m CNTFETs and
NWFETs, specially at low electric fields \cite{11,12,39,41}. An energy difference of $E_{cc} - E \geq 3k_B T$ has been considered as well, with $E_{cc}$ as the current control energy \cite{37,38} at which transport is enabled. For electron/hole transport, $E_{cc}$ is generally associated to the minimum/maximum of the conduction/valence band within the gated-channel region. After rearranging Eq. (1), an expression for $\Phi_{BH,eff}$ yields \cite{29,38}

$$\Phi_{BH,eff} \approx \frac{n_t}{w} \sum_{j=1}^{n_{/w}} \left[ -\frac{k_B}{q} \alpha_j + n_{g,j} (V_{GS} - V_{ot,j}) + n_{d,j} V_{DS} \right],$$

(2)

where the term $\alpha$ corresponds to the slope of the Arrhenius plots of $\ln (I_D/T)$ versus $1/T$. Eq. (2) reveals a linear relation between $\Phi_{BH,eff}$ and a term embracing a temperature- and drain-induced-electrostatics-dependent potential step $\Phi_{SB,eff}$, identified as an effective Schottky-like barrier height, such as

$$\Phi_{BH,eff} \approx \frac{n_t}{w} \sum_{j=1}^{n_{/w}} \left[ \Phi_{SB,eff} + n_{g,j} (V_{GS} - V_{ot,j}) \right],$$

(3)

from which $\Phi_{SB,eff}$ can be extracted at $|V_{GS} = \min(V_{ot,j})|$. A $V_{GS}$-dependent plot of Eq. (2), valid only for pure thermionic transport, enables the identification of $|\min(V_{ot,j})|$ at a $V_{GS}$ where the linear behavior of $\Phi_{BH,eff}$ vanishes. In contrast to AEM, 1D LBM enables the extraction of the terms $n_d$ and $n_g$, from $\alpha$ and $\partial (\ln I_D) / \partial V_{GS}$, respectively. The extraction of $n_d$ is enabled only if different $V_{DS}$ are evaluated. Notice that the individual characteristics of each 1D-channel required to compute the above equations, e.g., $\alpha$ for each tube/wire, are challenging to obtain in practice, however, experimental data embraces the total contribution of all channels, i.e., the entire sum terms in Eqs. (1)-(3), and hence, the extraction method (1D LBM) can be applied. The methodology is illustrated next with data of fabricated CNTFETs and NWFETs.

For long devices, the extraction method is justified by considering a weak temperature dependence of the scattering mechanisms at low-fields, i.e., $\mathcal{T}$ is considered a constant value. The latter enables to eliminate $\mathcal{T}$ when obtaining $\alpha$ and, subsequently, Eqs. (2) and (3).

III. RESULTS ACROSS CNTFET AND NWFET TECHNOLOGIES

A. Extraction from experimental data

The 1D LBM has been applied to available experimental data in the literature of multi-channel CNTFETs \cite{24,26,42,44} and NWFETs \cite{11,28,45} from different technologies, i.e., different channel
lengths and gate architectures. Additionally, a 1.5 µm-long NWFET, labeled as NWFET\textsubscript{EPFL}, not presented before has been also characterized. The fabrication process for NWFET\textsubscript{EPFL} has been described elsewhere\textsuperscript{46}. Device geometry parameters of the devices under study are summarized in Table I for reference purposes.

TABLE I. Device characteristics (channel/gate length $L_{\text{ch/g}}$, CNT/NW diameter $d$, CNT/NW density $D$, equivalent oxide thickness $EOT$) and gate architectures (global-back-gate GBG, buried-back-gate BG, top-gate TG, gate-all-around GAA) of fabricated multi-channel 1D devices. Missing data are indicated with a $\sim$.

| device   | ref. | gate arch. | $L_{\text{ch}}$ (µm) | $L_{g}$ (µm) | $d$ (nm) | $D$ (µm$^{-1}$) | $EOT$ (nm) |
|----------|------|------------|----------------------|--------------|---------|----------------|------------|
| CNTFET   | 43   | BG         | 0.5                  | 0.74         | –       | –              | 2.5        |
|          | 24   | GBG        | 1                    | 1            | 1.4     | –              | 290        |
|          | 42   | TG         | 24                   | –            | 0.76    | $\geq$ 40     | $\sim$ 280 |
|          | 42   | TG         | 24                   | –            | 0.76 to 1.31 | $\geq$ 40     | $\sim$ 280 |
|          | 20   | TG         | –                    | 2            | 1.3     | –              | –          |
|          | 44   | TG         | 40                   | –            | 0.76    | 15             | $\sim$ 280 |
| NWFET    | 11   | TG         | 0.05                 | –            | 40      | 5.6            | 5          |
|          | 25   | GAA        | 1                    | 1            | 20      | 12             | 46         |
|          | 45   | GAA        | 6                    | 1            | 20      | 12             | 46         |
|          | \textsubscript{EPFL} | GBG | 1.5                | 1.5         | 20      | –              | $\sim$ 25 |

Fig. 2 shows the extraction of $\Phi_{SB,\text{eff}}$ of the 24 µm-long multtube CNTFET\textsuperscript{42} with tube diameters of $\sim$0.76 nm as well as of the 1.5 µm-long NWFET\textsubscript{EPFL}. The transfer characteristics of both devices at different temperature and at a specific $V_{DS}$ are shown in Figs. 2(a) and (b) where the asymmetric ambipolarity of the CNTFET can be observed. The term $\alpha$ has been extracted from the Arrhenius plots of each device shown in Figs. 2(c) and (d) at $V_{GS}$ within the subthreshold regime where Eq. (1) is valid. The more temperatures available, the more accurate the extraction of $\alpha$ is. By obtaining $\alpha$ at each $V_{GS}$, the plots of $\Phi_{BH,\text{eff}}$ shown in Figs. 2(e) and (f) have been obtained from which the onset of tunneling processes at a $V_{ot}$ is identified. In this work, a relative error of $\sim$0.5% between the linear extrapolation and $\Phi_{BH,\text{eff}}$ is considered in order to identify $V_{ot}$. The effective Schottky barrier heights are identified at $V_{ot}$. For the ambipolar CNTFET, both
Schottky barriers for electrons and holes can be identified by considering the bias range in which thermionic emission from each type of carrier is expected to be dominant.

![Graphs showing I_D vs V_GS for CNTFET and NWFET](image)

**FIG. 2.** Extraction of effective Schottky barrier height of (a), (c), (e) a multitube CNTFET and (b), (d), (f) a multiwire NWFET. Transfer characteristics at different temperatures for the (a) CNTFET ($T=180$ K, 220 K, 260 K and 300 K) and (b) NWFET ($T=193$ K and 293 K). (c)-(d) Arrhenius plot at the subthreshold regime; dotted lines are added as a guide for the eyes in order to show the extraction of $\alpha$ at each $V_{GS}$. (e)-(f) $\Phi_{BH,eff}$ over $V_{GS}$ from which the effective Schottky barrier height (for electrons or holes) is extracted; dashed lines are a linear extrapolation and dotted lines are added as a guide for the eyes in order to indicate the extracted values.

The extracted 1D LBM $\Phi_{SB,eff}$s of the CNTFETs and NWFETs under study, including NWFET$_{EPFL}$, have been compared in Fig. [3] with the values obtained with the conventional AEM considering a three dimensional system. Notice that for the ambipolar devices including the CNTFETs with identical device geometry but different CNT diameters distribution reported in$^{42}$, $\Phi_{SB,eff}$ values have been extracted for both $n$-type and $p$-type transport.
In all devices under study, $\Phi_{SB,eff-1DLBM}$ is higher than $\Phi_{SB,eff-3DAEM}$, similar to the case of single-1D-channel devices. The underestimated 3D AEM values with respect to the 1D LBM approach can be explained by (i) a dimensionality issue leading to a $T^2$ factor yielded from a 3D-system consideration in the Arrhenius function rather than the $T$ factor related to 1D interfaces (e.g., see definition of $\alpha$ in Eq. (2)) and (ii) neglected gate and drain coupling coefficients in the underlying equation used in AEM. Further details on the difference between the methods are provided in the Appendix. The higher accuracy of 1D LBM with respect to 3D AEM has been previously demonstrated for single-channel devices.

For the CNTFETs with identical device architectures but different diameter distributions, $\Phi_{SB,eff-1DLBM}$ extracted values are higher (regardless the type of transport) for the device with the largest tube diameter distribution, similarly to the ones obtained by an AEM-like method for these same transistors but in contrast to previous findings in single-tube transistors. This contradiction with the one-channel case has been associated to thermionic injection hindered by tunneling mechanisms in non-homogeneous interfaces in multi-1D channel devices. Furthermore, non-homogeneous channel bands due to tube crossings might also impact the extraction as discussed below (cf. section III.C).

In contrast to AEM, 1D LBM enables the extraction of a device high-performance indicator such as the gate coupling coefficient: $|n_g| \to 1$ indicates an operation regime known as the quantum capacitance limit. Fig. 4 shows the extracted $|n_g|$ of some of the devices under study evaluated at different $T$ and $V_{GS}$ (within the bias region of validity of the method). For the 24 $\mu$m-long CNTFETs, the smaller the diameter the better the control of the gate over the channel is, and hence, it leads to a steeper subthreshold slope as suggested elsewhere and observed.
in the experimental transfer characteristics of these devices\textsuperscript{42}. The highest $|n_g|$ extracted for the NWFET studied here has been achieved for the shortest device\textsuperscript{11}, due to the thin $EOT$ (cf. Table I), i.e., the corresponding high gate capacitance dominates over the wire capacitance. Interestingly, an increasing temperature improves $n_g$ for the CNTFETs while the contrary is observed for the NWFETs. Since the latter can occur due to a trade-off between thermal-dependent phenomena, e.g., contact resistance, scattering mechanisms, etc., a further analysis can be suggested for CNT/NW devices with similar gate and channel architectures, however, this is out of the scope of the present study.

The onset of tunneling mechanisms in the $\Phi_{BH}(V_{GS})$-plot where $\Phi_{SB} = \Phi_{BH}|_{V_{GS}=V_{FB}}$ can be challenging to identify in devices where (i) $n_g$ has a weak $V_{GS}$-dependence\textsuperscript{50} or (ii) additional apparent linear regions of such plot are enabled by transparent contacts\textsuperscript{29}. In order to overcome these challenges, a special test structure to enhance the $\Phi_{SB,eff}$-extraction by 1D-LBM is suggested next for multi-1D-channel devices.

B. Test structure proposal

An experimentally-verified in-house numerical CNTFET simulator using a self-consistent solution of a transport equation and the Poisson equation, presented elsewhere\textsuperscript{14,51,52}, has been used here in order to propose a test structure for improving the $\Phi_{SB,eff}$ extraction. Two $n$-type multi-tube (MT) BG CNTFETs with identical device architectures and channel characteristics but different spacer lengths $L_{sp,x}$ have been studied. The latter architecture diminishes tunneling mechanisms\textsuperscript{31,43} and hence eases the extraction. Schematic cross sections of the simulated devices
are shown in Fig. 5. The metal-CNT interfaces in each device are a combination of the practical case of three parallel non-homogenous tubes within the device channel enabling a different Schottky barrier height each (cf. Fig. 1(c)) 0.05 eV, 0.1 eV and 0.2 eV. The device width is 60 nm yielding a tube density of 50 CNT µm⁻¹ associated to negligible screening effects between tubes.

FIG. 5. Schematic cross sections (not drawn to scale) of simulated CNTFETs with (a) a symmetric buried gate (MTBG1) and (b) an asymmetric buried gate (MTBG2). Gate oxide has a permittivity of 16. For both devices $h_G = 200$ nm, $h_{S/D} = 100$ nm, $t_{ox} = 15$ nm, $L_{S/D} = 50$ nm, $L_G = 200$ nm and $L_{ch} = 500$ nm where as $L_{sp,S}$ and $L_{sp,D}$ are of 150 nm both for (a) and of 250 nm and 50 nm for (b), respectively.

Simulations have been performed at 250 K, 300 K, 400 K and 500 K and $V_{DS}$ equal to 0.2 V over a $V_{GS}$ range between −0.2 V to 0.2 V. Tunneling and scattering mechanisms have been both considered whereas only electron transport has been enabled for simplification purposes. The simulated transfer characteristics at different temperatures of both MT CNTFETs are shown in Fig. 6(a). The 1D-LBM applied to the simulation data yields $\Phi_{SB,eff}$s of 0.17 eV and 0.21 eV for the symmetric and asymmetric gate device, respectively, as shown in Fig. 6(b) where a relative error of $\approx 0.5\%$ between a linear trend and the $\Phi_{BH}(V_{GS})$-plot has been used to identify an extracted flat-band voltage $V_{FB,ext}(=V_{ot,ext})$ and, consequently, to extract $\Phi_{SB,ext}$ for each case. $V_{FB,ext}$ are equal to 0.037 V and -0.007 V for the symmetric and asymmetric devices, respectively.

The conduction band diagrams of the individual CNT channels of both devices in Fig. 7 at $V_{GS} = V_{FB,ext}$ (identified in Fig. 6(b)) reveal the better electrostatic control within the the gated channel region in contrast to the spacers regions, regardless the CNT channel under study. Flat-band conditions are met at $V_{FB,ext}$ only for the metal-CNT interface with highest $\Phi_{SB}$ set in the simulation of the symmetric device (Fig. 7(a)), whereas the onset of tunneling current indicated by $V_{FB,ext}$ for the asymmetric device occurs before flat-band conditions are obtained regardless the CNT channel (Fig. 7(b)). However, the lower $I_{tun}$ obtained with the displaced gate device in comparison to the symmetric structure (see bottom of Fig. 7) at $V_{FB,ext}$ suggests that $\Phi_{SB,eff}$ obtained with the former CNTFET is closer to a barrier height where pure thermionic current occurs.
FIG. 6. Data of simulated symmetric and asymmetric BG MT CNTFETs. (a) Transfer characteristics at $V_{DS}=0.2$ V and different temperature. (b) Schottky barrier height extraction from the barrier height potential plot over $V_{GS}$ (top) and the relative error of such plot related to a linear extrapolation of the pure thermionic response (bottom). Red star (red dot) indicates the point at which $\Phi_{SB,\text{eff}}$ has been extracted for the (a) symmetric and (b) asymmetric device.

Hence, similar to the single-1D-channel devices, a test structure with a displaced gate hindering tunneling injection is suggested towards extracting a Schottky barrier height value closest to the true potential barrier height at metal-CNT interfaces in multi-1D-channel devices. Notice that fabricated asymmetric BG MT CNTFETs suitable for improving high-frequency performance such as the ones demonstrated elsewhere can be exploited for this extraction methodology as well.

FIG. 7. Conduction band diagrams (top) and thermionic and tunneling currents along the device channel (bottom) of the (a) symmetric and (b) asymmetric CNTFETs. Each channel (CNT) is identified by the $\Phi_{SB}$ at the metal-CNT interface set in the simulation.

C. Impact of Schottky points

In the present state of the technologies, CNT-based devices might suffer from crossings within the channel in non-parallel arrays in contrast to NWFETs where an improved control during fab-
fabrication enables parallel arrays. Schottky points (SPs) due to these crossings are related to a potential step in the channel electronic bands and hence, they might impact the transport as well as the pure thermionic energy level required to identify $\Phi_{SB}$ with 1D LBM. In this work, the impact of Schottky points on the extraction method is analyzed by means of the in-house device simulator previously described. Three symmetric BG CNTFETs (cf. Fig. 5(a)) with $L_{ch}$ of 280 nm, an $L_g$ of 230 nm and with a $\Phi_{SB}$ of 0.2 eV have been simulated with different types of SPs. Other simulation parameters are the same as the previous study (cf. Section III.B). In order to ease the discussion, a single-tube is used without loss of generality since similar tube density as in the previous simulation study (cf. Section III.B) has been considered. SPs are induced by doping a certain region of the tube, i.e., transport occurs through non-homogeneous bands. An SP1 (SP2) device has been doped towards increasing (decreasing) the energy level in a 1D channel region. A third device without SP has been simulated as well for reference purposes. Results are shown in Fig. 8.

As shown in Fig. 8(a), the extracted $\Phi_{SB}$ values (with 1D LBM) for the SP2 device and the device without SP are similar to the value of 0.2 eV set in the simulation, whereas for the case of the SP1 device a higher value is obtained. The latter can be explained by the higher energy required not only to overcome the potential barrier at the metal-channel interface but also the potential step within the channel as shown in Fig. 8 for these device in contrast to the others. Therefore, if tube crossings are present within a device, the extracted $\Phi_{SB,eff}$ with 1D LBM is associated to the thermal energy required to the carriers to overcome the highest of both potential steps: at the metal-channel or at any SP within the channel. Hence, the extraction method yields the higher of the potential barriers within the channel and hence, it should be considered as a maximum limit.
for devices with possible tube crossings.

IV. CONCLUSION

The metal-channel interfaces of fabricated FETs with arrays of CNTs and NWs with non-negligible potential barriers have been characterized here by 1D-LBM, an extraction method considering the 1D transport physics. The method extracts an effective Schottky barrier height associated to a potential separating thermionic and tunneling injection. This method overcomes the challenges encountered by conventional methods to characterize devices with non-homogeneous metal-channel interfaces. A high-performance device indicator has been also extracted such as the gate coupling coefficient. The latter helps to identify and quantify the gate control over the channel. Numerical device simulations show the improved accuracy of the characterization if a test structure is used, namely a displaced gated device. The method extracts the highest of the potential barriers in non-homogeneous electron bands within a multi-1D-channel, e.g., due to tube crossings. The methodology presented here is aim to improve the characterization and modeling of multi-1D-channel transistors where a potential barrier at the metal-channel interface can not be neglected.

ACKNOWLEDGEMENTS

This work has received funding from the European Union’s Horizon 2020 research and innovation programme under grant agreements No GrapheneCore2 785219 and No GrapheneCore3 881603, from Ministerio de Ciencia, Innovación y Universidades under grant agreements RTI2018-097876-B-C21(MICI/AEI/FEDER, UE) and FJC2020-046213-I. This article has been partially funded by the European Union Regional Development Fund within the framework of the ERDF Operational Program of Catalonia 2014-2020 with the support of the Department de Recerca i Universitat, with a grant of 50% of total cost eligible. GraphCAT project reference: 001-P-001702.

The authors would like to thank Martin Friedl and Prof. Anna Fontcuberta i Morral from École Polytechnique Fédérale de Lausanne, Switzerland, for providing the experimental data of the NWFET_{EPFL}. 

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DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

APPENDIX. DIFFERENCES OF $\Phi_{SB}$ EXTRACTED WITH 3D AEM AND 1D LBM.

The conceptual and mathematical differences between the novel 1D LBM and the conventional AEM for the characterization of metal-channel interfaces in 1D-devices are given here. For simplification purposes a single-1D-channel case is analyzed, however, this analysis can be extended to multiple-1D-channel devices by following the same considerations provided in Section II.

The mathematical background for AEM is based on the Richardson equation. By considering the thermionic emission of carriers (electrons) overcoming a potential barrier in 1D and an ideality factor of $\sim 1$, the drain current at the subthreshold region is approximately simplified to

$$I_D \approx A A^* T^2 \exp \left[ \frac{1}{V_t} (-\Phi_{BH} + V_{DS}) \right],$$

(A.1)

where $A$ is an effective 3D contact area and $A^*$ is the 3D Richardson constant. By following a similar procedure as the one used to obtain Eq. (2), the expression for the potential barrier within the framework of 3D-AEM is given by

$$\Phi_{BH} \approx -\frac{k_B}{q} \frac{\partial}{\partial T} \ln \left( \frac{I_D}{T^2} \right) + V_{DS} \equiv -\frac{k_B}{q} \alpha_{AEM} + V_{DS},$$

(A.2)

which can be used to extract a $\Phi_{SB}$ value. The underestimation of $\Phi_{SB}$ with 3D AEM in contrast to 1D LBM can be explained by comparing Eq. (2), adapted for single channel devices, and Eq. (A.2). These differences, pointed out in Section II, are the dimension-associated exponential of the temperature in $\alpha$ and $\alpha_{AEM}$ and the lack of both coupling coefficients and a $V_{GS}$-associated term in the AEM case. The latter are missing issues also in an adapted 1D AEM. A quantitative comparison between extracted values with 1D LBM and AEM has been provided in Fig. 3 as well as in previous studies.

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