Bilayer avalanche spin-diode logic

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A novel spintronic computing paradigm is proposed and analyzed in which InSb p-n bilayer avalanche spin-diodes are cascaded to efficiently perform complex logic operations. This spin-diode logic family uses control wires to generate magnetic fields that modulate the resistance of the spin-diodes, and currents through these devices control the resistance of cascaded devices. Electromagnetic simulations are performed to demonstrate the cascading mechanism, and guidelines are provided for the development of this innovative computing technology. This cascading scheme permits compact logic circuits with switching speeds determined by electromagnetic wave propagation rather than electron motion, enabling high-performance spintronic computing. © 2015 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution 3.0 Unported License.

Spintronics has been proposed as a foundation for a new generation of computers in which logical switching is performed through control of electron spin.¹–⁸ The essential requirement of a cascaded logic family in which the output of logic devices can control their switching mechanism⁹ has not yet been proven for spintronics, although a variety of intriguing spintronic switching devices have been proposed¹⁰–¹⁶ or demonstrated.¹⁷–²¹ In this letter, we solve this challenge by applying our recently invented spin-diode logic family²² to bilayer avalanche devices¹⁶ to propose a novel and efficient computing paradigm.

Joo et al. recently demonstrated the nearly ideal spintronic switching functionality of an InSb p-n bilayer channel avalanche spin-diode.¹⁶,²³ Their device functions as a room temperature “spin-diode,” the magnetic analog of an electrical diode, as shown in Fig. 1: the application of an external magnetic field greater than the spin-diode threshold $B_T$ switches the spin-diode from a resistive to a conductive state. In their experiment, $B_T$ is tuned through control of the voltage $V_{bias}$ applied across the device.

In their work, Joo et al. propose a logic structure in which the directions of the input magnetic fields and the magnitude of the bias voltage are used to control the magnitude of the spin-diode current. They experimentally demonstrate circuits that successfully perform the AND and OR functions with two series bilayer devices, the NOT and COPY (that is, inverter and buffer) functions with two parallel devices, and the AND/OR/NAND/NOR functions with two sets of two series bilayer devices in parallel. However, the lack of a strategy for using the output of one logic gate as the input for another gate prevents cascading and precludes the use of the logic structure explained in Ref. 16 for computing.

We propose a novel computing paradigm using the InSb p-n bilayer channel avalanche spin-diodes as the magnetoresistive switching elements for the spin-diode logic family. Spin-diode
FIG. 1. Spin-diode I-B characteristics. The bilayer avalanche spin-diode demonstrated experimentally has been modeled empirically based on Fig. 1b of Ref. 16 with $V_{bias} = 10.30$ V. The spin-diode exhibits nearly ideal behavior, but has a finite “off” resistance and gradual switching.

logic,22,24,25 which we originally developed for InAs/InMnAs heterojunctions,26 is applicable to any two-terminal magnetoresistive device that functions as a spin-diode. In this logic family, a constant bias voltage $V_{bias}$ is applied to all spin-diodes, and the current through each spin-diode is modulated by magnetic fields created by control wires. Binary logic states are represented by the spin-diode currents as state variables: large currents $I_{\text{high}}$ resulting from magnetic fields greater than the threshold $B_T$ are a logical ‘1’, and small currents $I_{\text{low}}$ from fields below $B_T$ are a logical ‘0’. The currents through the spin-diodes are routed through the control wires of other spin-diodes to manipulate their magnetoresistance. This cascading technique allows for the creation of the complex circuits required for computing.

The structure of the control wire and bilayer avalanche spin-diode is shown in Fig. 2. Current in the x-direction through the two control wires creates a magnetic field $B$ at the p-n junction in the y-direction. In contrast to the measurements of Joo et al. in a uniform magnetic field,16 a single $B_T$ value cannot be used and the strength of the magnetic field varies along the y-axis as

$$B(y) = \frac{\mu I_A}{2\pi R_{A,y}} \hat{y} + \frac{\mu I_B}{2\pi R_{B,y}} \hat{y} = \frac{\mu}{2\pi} \left( \frac{I_A}{R_{A,y}} + \frac{I_B}{R_{B,y}} \right) \hat{y},$$

where $\mu$ is the spin-diode permeability, $R_{A,y}$ and $R_{B,y}$ are the respective distances from the control wires to a location at the junction, and $I_A$ and $I_B$ are the currents through the control wires (positive current defined in the $+\hat{x}$ direction). This magnetic field modulates the source-drain current between the two contacts $I_{s-d}$, evaluated along the width $W$ of the p-n junction as

$$I_{s-d} = \int_W I(B(y)) \, dy.$$

FIG. 2. Bilayer avalanche spin-diode basis logic gate. Currents $I_A$ and $I_B$ create a magnetic field across the semiconductor p-n junction that modulates $I_{s-d}$. 
where $J(B\hat{y})$ is the magnetic field-dependent linear current density. Though a physical model of the bilayer avalanche device and the effects of the z-directed component of the magnetic field are beyond the scope of this work, the empirical model shown in Fig. 1 has been developed that approximates the experimental results and is suitable for analysis of this proposed logic family.

Electromagnetic simulations of the bilayer avalanche diode controlled by two control wires demonstrate the logical functionality. With the dimensions experimentally characterized in Ref. 16 (n-region thickness 0.2 µm, p-region thickness 6 µm, channel width 10 µm, channel length 120 µm) and two 1 µm × 1 µm control wires spaced 0.8 µm above the top of the n-region and separated from each other by 1 µm, the linear current density across the junction was simulated with COMSOL. Consistent with Ref. 16, we limit the current to prevent damage to the spin-diodes and ensure a single value for $I_{\text{high}}$. $V_{\text{bias}}$ is extracted from the experimental data as 10.30 V, and worst-case input binary current values of 100 mA (logical ‘1’) and 50 mA (logical ‘0’) were analyzed to show the robustness of the cascaded logic structure despite the exceptionally small 2:1 on/off ratio.

When the control wires are biased in the same direction, the magnetic fields created by $I_A$ and $I_B$ are additive. The magnetic field through the spin-diode is shown in Fig. 3(a) for the various worst-case input current values; the spatial variation implies a non-homogeneous current density through the spin-diode. When either or both control wires carry current $I_{\text{high}}$, the magnetic field at the bilayer junction is large enough to activate the magnetoresistance and permit a source-drain current greater than $I_{\text{high}}$. In the case of both inputs carrying small $I_{\text{low}}$ currents, the output propagates a current smaller than $I_{\text{low}}$. This cascading mechanism thus ensures signal integrity, as noise is attenuated by each logic gate. The electric and magnetic responses to binary digital inputs are listed in the truth table of Fig. 3(b), demonstrating functionality equivalent to the logical OR function, $F = A \lor B$.

![Spin-diode OR gate](image)

**FIG. 3.** Spin-diode OR gate. a) Magnetic field throughout the junction for the various combinations of input control currents. b) Spin-diode current values for logical OR function with current limited to 100 mA as in Ref. 16.
Biasing the control wires in opposite directions causes the fields to counteract. In this case, when both input currents are a ‘1’, the output current is a ‘0’ as shown in Fig. 4. Additionally, as the magnetoresistance is unipolar (asymmetric in regard to magnetic field direction), the output current is $I_{\text{low}}$ when $I_A$ is ‘0’ and $I_B$ is ‘1’. This function is equivalent to $F = A \land \overline{B}$, an AND gate with one inverted input, henceforth referred to as “IAND.”

The OR and IAND functions make up the basis gate set of this bilayer avalanche spin-diode logic family. With this basis set, all Boolean logic functions can be performed. Of critical importance, the logic gates can be cascaded directly, without any additional control or amplification circuitry.

As a demonstration of the application of the spin-diode logic family to bilayer channel spin-diodes, the one-bit half adder in Fig. 5 calculates the binary addition of two input bits (A and B) to generate a sum (S) and carry-out ($C_{\text{out}}$) bit. This circuit computes the half adder function optimized for bilayer avalanche spin-diode logic as

$$S = A \oplus B = (A \land \overline{B}) \lor (B \land \overline{A})$$

$$C_{\text{out}} = A \land B = A \land \overline{1} \land \overline{B}$$

using only five spin-diodes. In general, this logic family requires fewer than half the number of active devices in CMOS, with several representative examples in Fig. 6.

Electromagnetic wave propagation determines the switching speed in bilayer avalanche spin-diode logic, enabling high-performance computing. Whereas the $RLC$ interconnect delay is a growing problem in conventional integrated systems such as CMOS that have voltage as the state variable, charge transfer and accumulation is not a component of the switching process for systems in which current is the state variable. The complete switching delay in spin-diode logic,
FIG. 5. Bilayer avalanche spin-diode logic one-bit half adder. A is an input to the spin-diodes labeled IAND\(_1\), IAND\(_2\), and IAND\(_4\), and B is an input to IAND\(_1\), IAND\(_2\), and IAND\(_3\). The outputs of IAND\(_1\) and IAND\(_2\) are the inputs for OR\(_1\), which produces S. Similarly, C\(_{\text{out}}\) is calculated by IAND\(_4\), which receives as inputs A and the output of IAND\(_3\), which in turn receives B and a constant \(I_{\text{high}}\) as inputs.

\[
t_d = t_{\text{mag}} + t_{\text{sd}} + t_{\text{prop}},
\]

is the summation of the times required for a control wire current to switch a magnetic field in a neighboring spin-diode (\(t_{\text{mag}}\)), the spin-diode magnetoresistance to switch in response to a magnetic field (\(t_{\text{sd}}\)), and the electric field to propagate through the control wire to switch the current (\(t_{\text{prop}}\)). The speeds of all three phenomena are on the order of the speed of light, permitting much higher performance than the picosecond timescale available in the best modern processors.

Furthermore, this extremely fast operation does not result in excessive power consumption. In spin-diode logic, power consumption is primarily a result of the constant flow of current through the spin-diodes, with minimal additional power consumed during the switching process. Assuming a random distribution of signal values in a processor, the power dissipation is

\[
P = P_{\text{dynamic}} + P_{\text{static}} \approx P_{\text{static}} = \frac{(I_{\text{high}} - I_{\text{low}})^2}{2V_{\text{bias}}}
\]

For the initial experimental parameters described by Joo et al. and in this Letter, the static power dissipation of each logic gate is 0.78 W. This is far inferior to CMOS and should be considered as a starting point given a non-optimized unscaled device of micron dimensions, which can be reduced substantially through scaling. The ultimate potential will depend on the device behavior when scaled to nanometer dimensions. It should also be noted that the power is nearly independent of operating frequency, sharply contrasting with CMOS, in which the ideal power consumption is proportional to the operating frequency. (In modern CMOS systems, the parasitic leakage power also poses a major problem.)

| Logic Function    | CMOS Device Count | Bilayer Avalanche Spin-Diode Logic Device Count |
|-------------------|-------------------|-----------------------------------------------|
| Half Adder        | 16                | 5                                             |
| Full Adder        | 28                | 11                                            |
| 2:1 Multiplexer   | 12                | 4                                             |
| SR Latch          | 8                 | 2                                             |

FIG. 6. Logical efficiency comparison between CMOS and bilayer avalanche spin-diode logic.
InSb bilayer avalanche spin-diodes solve the primary challenge of spin-diode logic: magnetic field scaling. As the dimensions are decreased by a scaling factor \( s \), the currents used for creating the magnetic field are decreased by a factor \( s^2 \) to maintain constant current density. The distance between the control wire and p-n junction decreases only by a factor \( s \), resulting in a factor of \( s \) decrease in the magnetic field strength. Post-fabrication control of the magnetic field threshold \( B_T \) has heretofore never been suggested for spin-diode logic, making the voltage-tunable nature of the bilayer avalanche spin-diode an exciting prospect. In particular, a scaling scheme for bilayer avalanche spin-diodes can be envisioned in which the magnetic field strength is decreased with each generation through control of the source-drain voltage.

The reader should consider several variations to the logic structure presented in this letter. First, device count reductions are possible with a wired OR gate due to the use of current as the state variable. The use of a second \( V_{bias} \) applied to some spin-diodes can result in a negative \( B_T \), supplementing the set of basis logic gates. Additionally, more than two control wires may be used, further increasing the complexity of the functions performed by each gate. Finally, the control wires can be oriented to create fields in the perpendicular direction, triggering the positive magnetoresistance also shown in Ref. 16. Logic circuit designs for such devices are explored in Ref. 22.

Bilayer channel spin-diode logic efficiently computes complex logic functions, providing a feasible solution to the challenge of cascading the nearly ideal room temperature spin-diodes demonstrated by Joo et al. 16 In particular, the need for small changes in magnetic field permits spintronic switching with Amperian fields, allowing for spintronic switching speeds dependent on electromagnetic wave propagation and far faster than those possible through spin-transfer torque. The high performance, signal integrity, and compact circuits achieved in bilayer avalanche spin-diode logic opens a spintronic pathway to a new paradigm for the next generation of computing.

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