IR2Vec: A Flow Analysis based Scalable Infrastructure for Program Encodings

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We propose IR2Vec, a Concise and Scalable encoding infrastructure to represent programs as a distributed embedding in continuous space. This distributed embedding is obtained by combining representation learning methods with data and control flow information to capture the syntax as well as the semantics of the input programs.

Our embeddings are obtained from the Intermediate Representation (IR) of the source code, and are both language as well as machine independent. The entities of the IR are modelled as relationships, and their representations are learned to form a seed embedding vocabulary. This vocabulary is used along with the flow analyses information to form a hierarchy of encodings based on various levels of program abstractions.

We show the effectiveness of our methodology on a software engineering task (program classification) as well as optimization tasks (Heterogeneous device mapping and Thread coarsening). The embeddings generated by IR2Vec outperform the existing methods in all the three tasks even when using simple machine learning models. As we follow an agglomerative method of forming encodings at various levels using seed embedding vocabulary, our encoding is naturally more scalable and not data-hungry when compared to the other methods.

1 INTRODUCTION

With the growth of computing, comes the growth in computations. These computations are necessarily the byproduct of implementation of well-defined algorithms [CLRS09] implemented as programs. Thanks to the World Wide Web, these programs have become more accessible in various online platforms starting from programming tutorials to production quality code.

Code snippets from open-source hosting sites [Git08, Bit08], Community Question and Answer sites [ove18] and downloadable binaries along with the relevant information gives rise to “Big Code” [VY16]. A good part of the Big code is largely attributed to several implementations of the same algorithm that differ in a multitude of ways like, their complexity and theoretical metrics of execution, and efficiency of implementation. While Big Data processing itself poses a lot of challenges, analyzing humongous volumes of code poses significant and much harder problems, because of the fact that most of the programming language questions are undecidable as stated by Rice’s theorem [Ric53].

There is an increased need for understanding the syntax and semantics of programs and categorizing them for various purposes. This includes algorithm classification [MLZ+16, RZM11], code search [KBL+17, BOL14], code synthesis [RSK17], Bug detection [WCMAT16], Code summarization [IKCZ16], and Software maintenance [ABBSS14, ABBSS15, APS16, GPKS17].

Many existing works on representing programs use a form of Natural Language Processing for modeling; all of them exploit the statistical properties of the code, and adhere to the Naturalness hypothesis [ABDS18]. These works primarily use Word2Vec methods like skip gram and CBOW [MCCD13], or encoder-decoder models like Seq2Seq [SVL14] to encode programs as distributed vectors.

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We extend the above, and propose an Extended Naturalness hypothesis for Programs to consider the properties of the program by posing the problem of obtaining embeddings as a Data and Control flow problem.

**Extended Naturalness hypothesis.** Software is a form of human communication; software corpora have similar statistical properties to natural language corpora; and these properties along with static and dynamic program analysis information, can be exploited to build effective software engineering tools.

In this paper, we propose IR2Vec, an agglomerative approach for constructing a continuous, distributed vector to represent source code at different (and increasing) levels of IR hierarchy - Instruction, Function and Program. The vectors that are formed lower down the (program abstraction) hierarchy are used to build the vectors at the higher levels.

The initial seed vector to represent entities is learned by considering statistical properties in a Representational learning framework. Using this seed entity vectors, hierarchical vectors for the input program are formed considering the static and dynamic analysis information obtained from data and control flow analysis.

We make use of the LLVM compiler infrastructure [LA04] to process and analyze the code. The input program is converted to LLVM’s Intermediate Representation (IR), and the IR constructs form the entities whose representation is learnt. This makes our approach of representing programs to be source language and target architecture independent.

We show that the embeddings obtained by IR2Vec provide superior results when compared to the previous works [AZLY19, CPWL17, OWG13, MDO14], even though these earlier works were designed to solve specialized tasks, and IR2Vec is generic. We also compare our IR2Vec results with the ones of Ben-Nun et al. [BNJH18]; both have similar motivation in generating generic embeddings using LLVM IR.

We demonstrate the effectiveness of the obtained encodings by answering the following Research Questions (RQ’s) in the later sections:

- **RQ1: How well do the seed embeddings capture the semantics of the entities in LLVM IR?**
  As the seed embeddings play a significant role in forming embeddings at higher levels of Program abstraction, it is of paramount importance that they capture the semantic meaning of the entities to differentiate the different programs. We show the effectiveness of the obtained seed embeddings in Sec. 5.1.

- **RQ2: How good are the obtained embeddings for solving diverse applications?** We show the richness of the embeddings by applying it for different tasks: Program classification, Heterogeneous device mapping, and Prediction of thread coarsening factor in Sec. 5.2, 5.3 and 5.4.

- **RQ3: How scalable is the proposed methodology, and how likely does our method encounter Out of Vocabulary (OOV) words when compared to other methods?** We discuss various aspects by which our encoding is more scalable than the others, and also show that it does not encounter OOV words in Sec. 5.5.

- **RQ4: What is the contribution of data and control flow information to the final embeddings?** We repeat the experimentation with which RQ2 was answered (in Sec. 5) after peeling off the data and control flow information. We thereby show the importance of data flow and control flow information in Sec. 6.

The following are our contributions:

- A unique flow-analysis (program theoretic) based encoding to represent programs as vectors using Data and Control flow Information.
- Proposal of a Concise and Scalable encoding infrastructure using Agglomerative Methodology which in turn is built from the entities of LLVM IR.
• Hierarchy of encodings for Instruction, Function and Program.
• Testing of the effectiveness on a variety of tasks involving Program classification, Heterogeneous device mapping and Thread coarsening.

The paper is organized as follows: In Sec. 3, we give some basic background information. In Sec. 4, we explain the methodology followed to form the data and control flow based encodings at various levels. In Sec. 5, we show Experimentation followed by discussion on results. In Sec. 6, we compare our model with various varieties of its variants so as to show the strength of the proposed encoding. Finally, in Sec. 7, we conclude the paper.

2 RELATED WORKS
Modeling code as a distributed vector involves representing the program as a vector, whose individual dimensions cannot be distinctly labeled. Such a vector is an approximation of the original program, whose semantic meaning is “distributed” across multiple components.

In this section, we categorize some existing works that model codes, based on their representations, the applications that they handle, and the embedding techniques that they use.

Representations. Programs are represented using standard formats like lexical tokens [ABBS15, APS16, CPWL17], Abstract Syntax trees (ASTs) [AZLY18, RVK15], Program Dependence Graphs [ABK18], etc. Then, a neural network model like RNN or its variants is trained on the representation to form distributed vectors.

We use LLVM IR [LLV18c] as the base representation for learning the embeddings in high dimensional space. To the best of our knowledge, we are the first ones to model the entities of the IR—Opcodes, Operands and Types—in the form of relationships and to use a translation based model [BUGD+13] to capture such multi-relational data in higher dimensions.

Applications. In the earlier works, the training to generate embeddings was application specific and programming language specific: Allamanis et al. [ABBS15] propose a token based neural probabilistic model for suggesting meaningful method names in Java; Cummins et al. [CPWL17] propose the DeepTune framework to create a distributed vector from the tokens obtained from code to solve the optimization problems like thread coarsening and device mapping in OpenCL; Alon et al. [AZLY19] propose code2vec, a methodology to represent codes using information from the AST paths coupled with attention networks to determine the importance of a particular path to form the code vector for predicting the method names in Java; Mou et al. [MLZ*16] propose a tree based CNN model to classify C++ programs; Gupta et al. [GPKS17] propose a token based multi-layer sequence to sequence model to fix common C program errors by students; Other applications like learning syntactic program fixes from examples [RSD*17], bug detection [PS18, WSS18] and program repair [XWY*17] model the code as an embedding in a high dimensional space followed by using RNN like models to synthesize fixes. The survey by Allamanis et al. [ABDS18] covers more such application specific approaches.

On the other hand, our approach is more generic, and both application and programming language independent. We show the effectiveness of our embeddings on both software engineering task (to classify programs on a real time dataset) as well as optimization tasks (device mapping and thread coarsening) in Sec. 5.

Embedding techniques. Several attempts [ATGW15, BNJH18, VY16] have been made to represent programs as distributed vectors in continuous space using word embedding techniques for diverse applications. They generate and expose embeddings for the program [BNJH18], or the embeddings themselves become part of the training for the specific downstream task [AZLY19, PS18] without being directly exposed.
Our framework exposes an hierarchy of representations at the various levels of the program — Instruction, Function and Program level. We also believe that, we are the first ones to use program analysis based approaches to form these vectors agglomeratively from the base seed encodings obtained from the IR without using machine learning approaches.

NCC. The closest to our work is Ben-Nun et al.’s Neural Code Comprehensions (NCC) [BNJH18] who represent programs using LLVM IR. They use skip gram model [MSC+13] on conteXtual Flow Graph (XFG) which models data/control flow of the program to represent the IR. The skipgram model is trained to generate embeddings for every IR instruction. So as to avoid Out Of Vocabulary (OOV) statements, they maintain a large vocabulary; one which uses large (> 640M) number of XFG statement pairs. A more thorough comparison of our work with NCC [BNJH18] is given in Sec. 5.5.

3 BACKGROUND

3.1 LLVM and Program semantics

LLVM is a compiler infrastructure that translates source-code to machine code by performing various optimizations on its Intermediate Representation (LLVM IR) [LA04]. LLVM IR is a typed, well-formed, low-level, Universal IR to represent any high-level language and translate it to a wide spectrum of targets [LLV18c] [LLVM lang. Ref]. Being a successful compiler, LLVM provides easy access to existing control and data flow analysis and lets new passes to be added seamlessly.

The building blocks of LLVM IR include: Instruction, Basic block, Function and Module (Fig. 1). Every instruction contains opcode, type and operands and every instruction is statically typed. A basic block is a maximal sequence of LLVM instructions without any jumps. A collection of basic blocks form a function, and a module is a collection of functions. This hierarchical nature of LLVM IR representation helps in obtaining embeddings at the corresponding levels of program.

Analyzing the control flow structure of a program involves building a control flow graph (CFG), a directed graph in which each basic block is represented as a vertex, and the flow of control from one basic block to another is represented by an edge. Within a basic block, the flow of execution is sequential. Characterizing the flow of information which flows into (and out of) each basic block constitutes the data flow analysis. As the combination of data flow and control flow analyses information helps to describe the program flow, we use it for formation of embeddings to represent the program.

The control flow of a program is primarily described by its branches. The prediction of probabilities of conditional branches, either statically or dynamically, is called branch prediction [Muc97].
Static information is obtained by estimating the program profiles statically [WL94]. On the other hand, dynamic information is more accurate and involves dynamic profiling methods [BL92].

Given a source and destination basic block, the probability with which the branch would be taken can be predicted using the block frequency information generated by profiling the code. This probability is called as Branch probability. We try to use this data for modelling the control flow information.

### 3.2 Representational Learning

The effectiveness of a machine learning algorithm depends on the choice of data representation and on the specific features used. Representational Learning is a branch of machine learning that learns the representations of data by automatically extracting the useful features [BCV13].

In a similar spirit, Knowledge Graph embedding models try to model entities (nodes) and relations (edges) of a knowledge graph in a continuous vector space of n-dimensions [WMWG17]. In a broad sense, the input to these algorithms are \( \langle h, r, t \rangle \) triplets, where, \( h, r, t \) are \( n \)-dimensional vectors with \( h \) and \( t \) being Entities, and \( r \) being a Relation in the observed Knowledge Graph.

Of the many varieties available, we use TransE [BUGD+13], a translational representational learning model which tries to learn the relationship of the form \( h + r \approx t \), given the triplet \( \langle h, r, t \rangle \).

### 4 CODE EMBEDDINGS

In this section, we explain our methodology for obtaining code embeddings at various hierarchy levels of the IR. We first give an overview of the methodology, and then describe the process of embedding instructions and basic blocks (BB) by considering the data flow and control flow information to form a cumulative BB vector. We then explain the process to represent the functions and modules by combining the individual BB vectors to form the final Code Vector.

#### 4.1 Overview

The overview of the proposed methodology is shown in Fig. 2. Instructions in IR can be represented as a Relationship Graph, with the instruction entities as nodes, and the relation between the entities as edges. A translational learning model is used to learn these relations (Sec. 4.2). The output of this learning is the dictionary containing the embeddings of the entities and is called Seed embedding vocabulary.

The above dictionary is looked up to form the embeddings at various levels of the input program. The Use-Def and Reaching definition [Hec77, Muc97] information are used to form the instruction vector. In this process we also weigh the contribution of each Reaching definition with the probability with which they reach the current instruction. The instructions which are live are used to form the Basic block Vector. This process of formation of basic block vector using the flow analysis information is explained in the Sec. 4.3. The vector to represent a function is obtained by using the basic block vectors of the function. The Code vector is obtained by propagating the vectors obtained at the function level with the call graph information as explained in Sec. 4.3.3.

#### 4.2 Modelling LLVM IR as relations

**4.2.1 Generic tuples.** The opcode, type of operation (int, float, etc.) and arguments are extracted from the LLVM IR (Fig. 3a). This extracted IR is preprocessed in the following way: first, the identifier information is abstracted out with more generic information as shown in Tab. 1. Next, the Type information is abstracted to represent a base type ignoring its width.

**4.2.2 Code triplets.** From this preprocessed data, three major relations are formed: (1) TypeOf: Relation between the opcode and the type of an instruction, (2) NextInst: Relation between the
opcode of the current instruction and opcode of the next instruction; (3) \( \text{Arg}_i \): Relation between opcode and its \( i^{th} \) operand. This transformation from actual IR to relation (\( <h, r, t> \) triplets) is shown in Fig. 3. These triplets form the input to the representation learning model.

For example, the first store instruction in Fig.3(a) is of integer type with a variable as the first operand and a pointer as the second operand. As shown in Fig.3(b), it is transformed to the corresponding triplets involving the relations TypeOf, NextInst, Arg1, Arg2.

%a.addr = alloca i32, align 4
%b.addr = alloca i32, align 4
store i32 %a, i32* %a.addr, align 4
store i32 %b, i32* %b.addr, align 4
%0 = load i32, i32* %a.addr, align 4
%1 = load i32, i32* %b.addr, align 4
%add = add nsw i32 %0, %1
ret i32 %add

\(<\text{alloca}, \"\text{TypeOf}\", \text{IntegerTy}>\>
\(<\text{alloca}, \"\text{NextInst}\", \text{alloca}>\>
...\n\(<\text{store}, \"\text{TypeOf}\", \text{IntegerTy}>\>
\(<\text{store}, \"\text{NextInst}\", \text{alloca}>\>
\(<\text{store}, \"\text{Arg1}\", \text{VAR}>\>
\(<\text{store}, \"\text{Arg2}\", \text{PTR}>\>
...\n
Fig. 3. Mapping from LLVM IR to relations:(a) LLVM IR and (b) Formation of triplets
4.3 Instruction Vector

The output of learning model is the Seed embedding vocabulary containing the vector representation for every entity of the relation. Let the entities of instruction \( l \), be represented as \( O(l) \), \( T(l) \), \( A_i(l) \) - corresponding to Opcode, Type and \( i^{th} \) Argument of the opcode and their corresponding vector representations be \( \langle O(l) \rangle, \langle T(l) \rangle, \langle A_i(l) \rangle \).

Then, an instruction of format \( O(l) T(l) A_1(l) A_2(l) ... A_n(l) \) is represented as

\[
W_o \cdot \langle O(l) \rangle + W_t \cdot \langle T(l) \rangle + W_a \cdot (\langle A_1(l) \rangle + \langle A_2(l) \rangle + ... + \langle A_n(l) \rangle)
\]  

where \( W_o, W_t \) and \( W_a \) are chosen heuristically so as to give more weightage to opcode than type, and more weightage to type than arguments:

\( W_o > W_t > W_a \)

This resultant vector representing an instruction is the Instruction vector.

4.3.1 Embedding Data flow information. An instruction in LLVM IR may define a variable or a pointer that could be used in another section of the program. The set of uses of a variable (or pointer) gives rise to the use-def (UD) information of that particular variable (or pointer) in LLVM IR [Hec77, Muc97].

In imperative languages, a variable can be redefined; meaning, in the flow of the program, it has different set of lifetimes. Such a redefinition is said to kill the earlier definition of that variable. During the flow of program execution, only a subset of such live definitions would reach the use of that particular variable. This subset of live definitions that reach an instruction is called the Reaching Definitions of the variable for that instruction. We model instruction vector using such Data flow analyses information. Each \( A_i \) which has been already defined is represented using the embeddings of its Reaching definitions. The Instruction Vector for a reaching definition if not calculated, is computed at this instant.

4.3.2 Branches, Control flow and Profile information. Branches are the key in determining the program structure; which in turn, defines the control flow of the program. But, treating all the definitions which reach the current instruction by different paths equally may be misleading. So as to get a precise meaning of the program’s control flow, each path through which the definitions could reach a use should be treated differently.

The key to doing the above is to take into account the probability of the path determined by each branch. This information can be obtained via static analyses techniques which are readily available in compilers. Using BranchProbabilityInfo (BPI), an analysis pass in LLVM, it is possible to get an estimate of the probability with which the control flows from one basic block to another [LLV18a, LLV18b]. The probabilities of all the outgoing edges from a block naturally sum up to one. In program analysis, this information is highly valued and aids other optimization passes like determining hotness of a basic block, and similar instrumentation purposes. We use this BPI information to find the probability with which a definition could reach its use.

4.3.3 Using BPI to construct Instruction Vector. If \( RD_1, RD_2, ... , RD_n \) are the reaching definitions of \( A_j(l) \), and \( \langle RD_i \rangle \) be their corresponding encodings, then,

\[
\langle A_j(l) \rangle = \sum_{i=1}^{n} \sum_{k=1}^{\#paths} p_{ik} \langle RD_i \rangle
\]  

Let \( p_{ik} \) be the probability of definition in instruction \( I_i \) reaching instruction \( I_l \) via path \( k \). Then, \( \sum p_{ik} \) is the sum of the probabilities of all such \( k \) paths reaching the instruction \( I_l \) from instruction
The branch probability between two instructions $I_x$ and $I_y$ corresponds to the probability of reaching $I_y$ from $I_x$.

For the cases where the definition is not available (for example, function parameters), the generic entity representation of “VAR” or “PTR” from the seed embedding vocabulary is used. An illustration is shown in Fig. 4, where the instructions $I_{\text{Source1}}$ and $I_{\text{Source2}}$ reach $I_{\text{Target}}$ as arguments, each with the probabilities labeled on the respective edges.

![Diagram](image)

Fig. 4. Illustration of propagating definitions to reach its use - Definition $I_{\text{Source1}}$ reaches $I_{\text{Target}}$ either directly with a probability $p$ or via $I_{\text{Source2}}$ with a probability $q \times r$. And, definition $I_{\text{Source2}}$ reaches $I_{\text{Target}}$ with a probability $s$. Hence, $\llbracket I_{\text{Target}} \rrbracket = p \llbracket I_{\text{Source1}} \rrbracket + q \times r \llbracket I_{\text{Source1}} \rrbracket + s \llbracket I_{\text{Source2}} \rrbracket$

An instruction is said to be killed when the return value of that instruction is redefined. As LLVM IR is in SSA form [CFR+91, LA04], each variable has a single definition and the memory gets (re-)defined. Based on this, we categorize the instructions into two classes: one which define memory, and one that do not. The first class of instructions is Write instructions, and the second class of instructions is Read instructions.

Embeddings are formed for each instruction as explained above. If these embeddings correspond to a write instruction, future uses of the redefined value will take the embedding of this current instruction—instead of the embedding corresponding to its earlier definition—until it gets redefined. This process of Kill and Update, along with the use of reaching definition for forming the instruction vectors within (and across) the basic block are illustrated in Fig. 5 (and Fig. 6) for the corresponding Control Flow Graph (CFG) respectively.

4.3.4 Resolving Circular Dependencies. While formation of the instruction vectors, circular dependencies between two write instructions may arise if both of them write to the same location and the (re-)definitions are reachable from each other.

For calculating $\llbracket I_4 \rrbracket$, the encoding of $I_4$, in the CFG show in Fig. 7, it can be seen that $RD[I_4] = \{I_3, I_7\}$. Also, $\llbracket I_7 \rrbracket$ is needed for encoding $\llbracket I_4 \rrbracket$ and is yet to be computed, results in a circular dependency:

$$RD[I_7] = \{I_3, I_5\}; \quad \text{But } \llbracket I_5 \rrbracket \text{ is not calculated, yet } \implies \text{Calculate } \llbracket I_5 \rrbracket$$

$$RD[I_5] = \{I_3, I_7\}; \quad \text{But } \llbracket I_7 \rrbracket \text{ is not calculated, yet } \implies \text{Calculate } \llbracket I_7 \rrbracket$$

$\implies \llbracket I_5 \rrbracket \text{ depends on } \llbracket I_7 \rrbracket \text{ and vice versa.}$

1Though this CFG is the classic irreducibility pattern [Hec77, Muc97], it is easy to construct reducible CFGs with circular dependencies.
This problem of circular dependencies can be solved by posing the embedding equations as a set of simultaneous equations to a solver. For example, the embedding equations of $I_5$ and $I_7$ shown in Fig. 7 would be:

$$
[I_5] = W_0([\text{store}]) + W_7([\text{PointerTy}]) + W_0([\text{VAR}]) + W_0(b \ast [I_3]) + W_0(d \ast e \ast [I_5])
$$

$$
[I_7] = W_0([\text{store}]) + W_7([\text{PointerTy}]) + W_0([\text{VAR}]) + W_0(c \ast [I_3]) + W_0(e \ast d \ast [I_5])
$$
If \( p = d \times e \), and \( k_1, k_2 \) are functions of \( \llbracket I_3 \rrbracket \), then Eqn. 3 becomes:

\[
\llbracket I_5 \rrbracket = k_1 + W_d \times p \times \llbracket I_7 \rrbracket \\
\llbracket I_7 \rrbracket = k_2 + W_d \times p \times \llbracket I_5 \rrbracket
\]

The above equations need to be solved to get the embeddings for \( I_5 \) and \( I_7 \).

One possible issue that can arise on resolving the circular dependency is that the system may not always have a unique solution (not reach a fixed point [Heck77, KU76]). For the example shown in the Fig. 7, if \( W_d = 1 \) and \( p = 1 \), then Eqn. (4) would result in a system without a unique solution.

This problem can be overcome by randomly picking one of the equations in the system, and perturbing the probability value \( p \) of that equation to \( p - \Delta \), so that the modified system converges to a solution.

In our entire experimentation shown in Sec. 5, we however did not encounter such a system.

### 4.4 Construction of Code vector from Instruction vector

After computing the instruction vector for every instruction of the basic block, we calculate the Basic Block vector by using the embeddings of those instructions which are not killed. If \( \text{LIVE}[BB_i] \) correspond to the live instruction set of the basic block \( BB_i \) containing the set of instructions \( I \) and whose kill set is represented as \( \text{KILL}[BB_i] \), then the corresponding basic block vector is computed as

\[
\text{LIVE}[BB_i] = \bigcup I - \text{KILL}[BB_i] \\
\llbracket BB_i \rrbracket = \sum \text{LIVE}[BB_i]
\]

The vector to represent a function \( F \) with basic blocks \( BB_1, BB_2, \ldots, BB_b \) is calculated as

\[
\llbracket F \rrbracket = \sum_{i=1}^{b} \llbracket BB_i \rrbracket
\]

Our encoding and propagation also takes care of programs with function calls; the embeddings are obtained by using the call graph information. For every function call, the function vector for the callee function is calculated, and this value is used to represent the call instruction. For the functions, which are resolved during the link time, we just use the embeddings obtained for call instruction. This final vector represents the function. This process of obtaining the instruction vector and function vector is summarized in the Algorithm 1.

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\(^2\)Choosing infinitesimally small \( \Delta \) values could lead to an unbounded increase of the magnitude of the elements in the encoding vector.
If \( \langle F_1 \rangle, \langle F_2 \rangle, \ldots, \langle F_f \rangle \) are the embeddings of the functions \( F_1, F_2, \ldots, F_f \) in the program, then the code vector representing the program \( P \) is

\[
\langle P \rangle = \sum_{i=1}^{f} \langle F_i \rangle
\] (7)

**Procedure** getInstrVec(Instruction I, Dictionary seedEmbeddings)

- \( \langle O \rangle \leftarrow \text{seedEmbeddings}[\text{Opcode(I)}] \)
- \( \langle T \rangle \leftarrow \text{seedEmbeddings}[\text{Type(I)}] \)
- \( \langle A \rangle \leftarrow \emptyset \)
- for each argument \( a \) in I do
  - if \( a \in \text{Function} \) then
    - \( val \leftarrow \text{seedEmbeddings}[^{\text{FUNCTION}}] \)
    - if definition of \( a \) is available then
      - \( val \leftarrow \text{getFuncVec}(a) \)
    - else if \( a \in \{\text{VAR}, \text{PTR}\} \) then
      - if \( a \) is not a use of a definition then
        - \( val \leftarrow \text{seedEmbeddings}[^{'\text{VAR} or '\text{PTR}}] \)
      - else
        - for every reaching definition RD of \( a \) do
          - \( \langle RD \rangle \): Obtain the embedding of RD
          - if \( \langle RD \rangle \) leads to cyclic dependency then
            - Resolve and obtain \( \langle RD \rangle \) as shown in 4.3.4
            - \( p \leftarrow \text{probability of RD reaching } a \)
            - \( val \leftarrow val + (p \times \langle RD \rangle) \)
        - else if \( a \in \text{CONST} \) then
          - \( val \leftarrow \text{seedEmbeddings}[^{\text{CONST}}] \)
        - else if \( a \in \text{address of Basic block} \) then
          - \( val \leftarrow \text{seedEmbeddings}[^{\text{LABEL}}] \)
  - \( \langle A \rangle \leftarrow \langle A \rangle + val \)
- return \( W_o \times \langle O \rangle + W_t \times \langle T \rangle + W_a \times \langle A \rangle \)

**Procedure** getFuncVec(Function F, Dictionary seedEmbeddings)

- \( \langle F \rangle \leftarrow \emptyset \)
- for every basic block \( BB \in F \) do
  - \( \langle BB \rangle \leftarrow \emptyset \)
  - for every live instruction \( I \in F \) do
    - \( \langle I \rangle \leftarrow \text{getInstrVec}(I, \text{seedEmbeddings}) \)
    - \( \langle BB \rangle \leftarrow \langle BB \rangle + \langle I \rangle \)
  - \( \langle F \rangle \leftarrow \langle F \rangle + \langle BB \rangle \)
- return \( \langle F \rangle \)

5 EXPERIMENTATION

We used the SPEC CPU 17 [BLvK18] benchmarks (INT and FP) and Boost library [Boo18] as the datasets for learning the representations. The programs in these benchmarks are converted to LLVM IR by varying the compiler optimization levels (-O0, -O1, -O2, -O3) at random. The resultant IRs are used as the data to learn embeddings by using an open-source implementation of TransE [HCL18].

The training was done with SGD optimizer for 1500 epochs to obtain embedding vectors of 300 dimensions. There were \( \approx 134M \) triplets in the dataset, out of which \( \approx 8K \) relations were unique; from these, we obtain 64 different entities whose embeddings are learnt. These learnt embeddings
of 64 different entities form the seed embeddings. The obtained entities are listed in Appendix A. This information is listed in the Tab. 7.

We heuristically set \( W_o, W_t \) and \( W_a \) to 1, 0.5, 0.2 respectively. We analyzed the effectiveness of the vectors obtained at various levels of the programs which were not used in the process of representation learning.

In this section, we attempt to answer RQ1 by showing the clusters and analogies of seed embeddings, RQ2 by performing various tasks at different levels of the program and RQ3 by doing a study on scalability.

5.1 Evaluation of Seed Embeddings

The effectiveness of the seed embeddings are analyzed by forming their clusters, and by posing analogy questions to demonstrate if the relationship between the entities are captured effectively by the obtained seed embeddings.

5.1.1 Clusters. The entities of the obtained seed embeddings are categorized as groups based on their operations — Arithmetic operators containing the integer and floating point based arithmetic operations, Pointer operators which access memory, Logical operators which perform logical operations, Terminator operators which form the last instruction of the basic block, Casting operators which perform type casting, Type information and Arguments. Clusters showing these groups are plotted using 2-PCA [WEG87] and are shown in Fig. 8.

In Fig. 8(a), we show the relation between various types. It can be observed that vectorTy being an aggregate type can accept any of the other primitive type data and lies approximately equidistant from integerTy, pointerTy, structTy and floatTy.

All integer based arithmetic operators are grouped together and are distinctly separated from floating point based operators as shown in Fig. 8(b). It can also be seen that the arithmetic operators are separated from the arguments (Fig. 8(b)), pointer operators (Fig. 8(e)) and terminator operators (Fig. 8(f)) distinctly. From Fig. 8(c), we can see that the logical operators are also distinctly separated from the arguments.

Fig. 8(d) shows the relationship between arithmetic and casting operators. It can be clearly seen that the integer based casting operators like trunc, zext, sext, etc. are grouped together with integer operators and floating point based casting operators like fptrunc, fpext, fpstrip, etc. are grouped together with floating point operators. On observing Fig. 8(d) and Fig. 8(e), it can be seen that ptrtoint and inttotptr are closer to both integer operators and pointer operators. Fig. 8(e) also demonstrates that the arithmetic operators are clearly distinct from pointer operators.

Logical operators operate on integers and hence they are grouped together with integer operators as observed in Fig. 8(f).

5.1.2 Analogies. Queries of the form \( a : b :: c : ? \) are posed to the learned entity representation vectors. The missing value is computed by \( b - a + c \) and the closest neighbour by Euclidean distance is considered to be the result.

**Syntactic.** The syntactic information include comparing the instructions based on the following:

- Datatypes (For example, integer type zero extension- zext vs. floating point type- fpext)
- Data structures (For example, instruction to shuffle element of vector type - shufflevector vs. instruction to get the address of an element - getelementptr)
- Sequence of instructions which occur together (For example, if load is equivalent to store, then landingpad is equivalent to invoke).

**Semantic.** The semantic information reveals several interesting results:
Fig. 8. Comparison of embeddings of various seed entities

- If signed integer division is equivalent to right shift operation, then integer multiplication is equivalent to left-shift operation.
- If integer to pointer conversion is equivalent to pointer to integer conversion operator, then truncate is equivalent to zero extension operator.

Tab. 2 shows some of the other such obtained analogies which imbibe the syntax, as well as the semantic information. A more detailed table (Tab. 12) can be found in Appendix B.

5.2 Program Classification
We show the effectiveness of the obtained embeddings at the program level by classifying programs from a real time dataset of a competitive programming contest. For this purpose, we construct a
Table 2. Obtained Instruction Analogies

| Syntactic                  | Semantic          |
|----------------------------|-------------------|
| zext : integerTy :: fpext : floatTy | sdiv : lshr :: mul : shl |
| trunc : fptrunc :: icmp : fcmp      | fptoui : uitofp :: fptosi : sitofp |
| load : pointer :: store : constant/variable | sdiv : srem :: udiv : urem |
| fdiv : sdiv :: fmul : mul           | shl : lshr :: or : and |
| call : ret :: switch : label        | shl : ashr :: mul : div |

simple three layered neural network which takes the vectors representing the programs of different classes as input and predicts the class as output. The programs for classification were obtained from the submissions of Google’s longest running annual coding competition, code jam [jam03]. The problems/submissions for each round of every year are available in the public domain.

We evaluate LLVM IR obtained for the C++ solutions from Rounds 1A/1B/1C of the three past years (2015–17). Each round consists of three problem statements, forming nine different problems. Given a working input program, the task is to map it to its problem statement. The dataset consists of ≈ 38K programs. 70% of data were used for training, 15% for validation and 15% for testing. Vectors to represent these programs are generated as described in the earlier sections.

The neural network for this task consists of two stacked dense layers of 80 units each. Batch normalization [IS15] with ReLU as the activation function is used, with a dropout of 25% as regularizer between each layer. The final layer is a softmax layer with 9 units so as to classify programs across 9 different classes. SGD with learning rate of 0.001 and categorical cross entropy is used as the loss function. Given an input vector, the network is trained to predict a class out of the nine classes of programs. We obtain an accuracy of 97.66% on training for 100 epochs.

In Tab. 3, we show the comparison of the accuracy obtained between IR2Vec and other recent methods. On performing the task using Neural Code Comprehension [BNJH18], we hit Out Of Memory (OOM) in the second epoch. For the purpose of comparison, we collected the code vectors of code2vec [AZLY19] for every function of a program and summed them to represent the program. After the formation of program vectors from the code vectors, we perform the experiment with these vectors in the same setup and results are obtained. It can be seen that the accuracy obtained by IR2Vec is superior than the other methods.

| CodeJam classification results |
|-------------------------------|
| code2vec [AZLY19] | inst2vec [BNJH18] | IR2Vec |
| Accuracy | 64.0% | OOM | 97.66% |

5.3 Heterogeneous Device Mapping

In this experiment, we use the embeddings obtained by IR2Vec for the heterogeneous device mapping task proposed by Grewe et al [OWG13] to map the OpenCL kernels to the optimal target device - CPU or GPU in a heterogeneous system.

Function vectors for each kernel obtained using IR2Vec along with the two auxiliary inputs - data size and workgroup size forms the dataset. Gradient boosting classifier with 10 fold cross validation is used to train the model. We use the same dataset and experimental setup as that of Ben-Nun et al. [BNJH18]. Our embeddings are generated at the program level/function level directly without forming a sequential data. So, we use a gradient boosting classifier instead of sequential neural networks (like RNNs or LSTMs). Similar to the earlier methods, we use the runtimes corresponding to the predicted device, to calculate the speedup.

In Tab. 4 and Tab. 5, we show the comparison of prediction accuracy and speed up of IR2Vec with the manual feature-extraction approach of Grewe et al. [OWG13], DeepTune model of Cummins et
al. [CPWL17], and inst2vec (and inst2vec-imm) approaches of Ben-Nun et al. [BNJH18]. It can be seen that IR2Vec outperforms all the other methods in terms of accuracy and speedup obtained by the best performing method.

| Table 4. Prediction accuracy |
|-----------------------------|
| Architecture | Grewe et al. [OWG13] | DeepTune [CPWL17] | inst2vec [BNJH18] | inst2vec-imm [BNJH18] | IR2Vec |
| AMD Tahiti 7970 | 73.38 | 83.67 | 82.79 | 88.09 | 92.38 |
| NVIDIA GTX 970 | 72.94 | 80.29 | 81.76 | 86.62 | 87.00 |
| Average | 73.16 | 81.98 | 82.27 | 87.35 | 89.69 |

| Table 5. Speed-up |
|-------------------|
| Architecture | Grewe et al. [OWG13] | DeepTune [CPWL17] | inst2vec [BNJH18] | inst2vec-imm [BNJH18] | IR2Vec |
| AMD Tahiti 7970 | 2.90 | 3.33 | 3.42 | 3.47 | 3.51 |
| NVIDIA GTX 970 | 1.26 | 1.41 | 1.39 | 1.44 | 1.45 |
| Average | 2.08 | 2.37 | 2.40 | 2.45 | 2.48 |

5.4 Prediction of optimal Thread Coarsening factor

Thread coarsening is the process of increasing the work done by a single thread by fusing together two or more concurrent threads. Thread coarsening factor corresponds to the number of threads which can be fused together. Selection of optimal thread coarsening factor would lead to significant improvement in the speedups of GPU devices [Automatic Optimization of Thread-Coarsening for GraphicsProcessors].

In this experiment, we predict the optimal thread coarsening factor using the same experimental setup and the dataset of Ben-Nun et al. [BNJH18]. Even here, we use gradient boosting classifier with 10 fold cross validation on the embedding vectors obtained by IR2Vec instead of the complicated DNNs to predict the coarsening factor for the four GPU targets.

Table 6 shows the comparison of the speedups achieved by coarsening the threads with the predicted coarsening factor on various GPUs across various methods. It can be seen that except for AMD Radeon, IR2Vec achieves consistently higher speedups when compared to that of other methods.

5.5 Study on scalability and exposure to OOV words

For representing programs using the embeddings learnt by a neural network, the training phase involves exposure to various (and large) combinations of the underlying entities. For example, for generating embeddings using AST paths, the training should cover the space of various permutations and combinations of the underlying constructs that can potentially form a path. Similarly, for generating the embeddings at a statement level of IR, all possibilities of opcode, type and arguments that can potentially form a statement have to be exposed in training. As it can be seen, covering such a huge intractable space is infeasible, and hence undesirable.

When an unseen combination of underlying constructs—either at the AST path level or at the LLVM statement level is encountered during inference—it leads to Out Of Vocabulary (OOV) data.
Table 6. Speedups achieved in thread coarsening

| Architecture          | Magni et al. [MDO14] | DeepTune [CPWL17] | DeepTune-TL [CPWL17] | inst2vec [BNJH18] | inst2vec-imm [BNJH18] | IR2Vec |
|-----------------------|----------------------|-------------------|----------------------|-------------------|------------------------|--------|
| AMD Radeon HD 5900   | 1.21                 | 1.1               | 1.17                 | 1.29              | 1.28                   | 1.23   |
| AMD Tahiti 7970       | 1.01                 | 1.05              | 1.23                 | 1.07              | 1.18                   | 1.30   |
| NVIDIA GTX 480        | 0.86                 | 1.1               | 1.14                 | 0.97              | 1.11                   | 1.16   |
| NVIDIA Tesla K20c     | 0.94                 | 0.99              | 0.93                 | 1.01              | 1.00                   | 1.13   |
| **Average**           | 1.005                | 1.06              | 1.11                 | 1.08              | 1.14                   | 1.21   |

points and performance degradation. Consequently, the methods like (AST based) code2vec [AZLY19] and (LLVM-IR based) NCC [BNJH18] face OOV issues.

On the other hand, IR2Vec forms a finite and relatively small vocabulary of seed encodings, using which the representations at various hierarchies are obtained cumulatively, and hence does not encounter OOV issues. Note that even by training with smaller number of files and maintaining a smaller vocabulary, IR2Vec achieves better performance than the other methods.

A comparison of IR2Vec with code2vec and NCC with respect to training and vocabulary is shown in Tab. 7.

Table 7. Comparison Matrix: code2vec vs. NCC vs. IR2Vec

| Comparison metric         | code2vec [AZLY19] | NCC [BNJH18] | IR2Vec |
|---------------------------|-------------------|-------------|--------|
| Primary embedding         | Function level    | Instruction level | Entity level |
| Files examined            | ≈1.8M             | 24,030      | 13,029 |
| Vocabulary size           | ≈1.5M token/target embeddings | 8,565 statement embeddings | 64 entity embeddings |
| Entities examined         | ≈15M Methods      | ≈640M XFG Statement Pairs | ≈134M Triplets |
| Training time             | 1.5 days on one Tesla K80 | 200 hours on one P100 | 20 minutes on one P100 |

A comparison on the number of OOV entities encountered by code2vec, NCC and IR2Vec on a set of straightforward programs involving family of sorting, searching, dynamic, greedy programs obtained from a online collection of programs [Gee03] is shown in Fig. 9. It can be seen that our method does not encounter any OOVs even when exposed with lesser training data, thereby achieving good scalability.

6 ABLATION STUDY

In this section we try to answer RQ4 by changing the various design aspects of the proposed work and analyse the contribution of each of them.

6.1 Mapping of LLVM IR to relations

We try to analyse the contribution of each relation in the formation of embeddings at entity level. Out of the three relations, TypeOf, NextInst and Arg, we mask each of them separately and observe their impact by studying the resulting analogies.

Triplets are formed from the same dataset using the described process by ignoring one relation at a time. The same experimental setup as explained in the Sec. 5.1.2 has been used. If the desired result is present in the top 5 closest neighbors obtained by Euclidean distance, then it is considered to be a match. Percentage of matching analogies are obtained for the embeddings without TypeOf, NextInst and Arg relations separately and are listed in the Tab. 8 for the analogies given in the
Appendix B. When the TypeOf relation is removed, the analogies like sext : integerty :: fpext : floatty which involve type information fail. Similarly, when the Arg relations are removed, the analogies like call : ret :: switch : label which needs arguments information fail. We can observe that the best value is obtained only when all three relations are considered.

Table 8. Percentage of matching analogies with missing relations

| {NextInst, Args} | {TypeOf, Args} | {NextInst, TypeOf} | {TypeOf, NextInst, Args} |
|------------------|----------------|---------------------|--------------------------|
| Percentage       | 43%            | 69%                 | 38%                      | 77%                      |

### 6.2 Effect of optimization sequences

We study the effect of the compiler optimization sequences (O1, O2, O3) on the program classification task. These optimization sequences are expected to have little or no impact on the obtained results. Optimization sequence is applied on the dataset and then the embeddings are generated. The obtained embeddings are used for classification. Same experimental setup of the task is used and their accuracies are obtained (Tab. 9). This experiment demonstrates the goodness of the obtained seed embeddings irrespective of the optimization levels.

Table 9. CodeJam classification results with various optimization sequences

|          | -00 | -01 | -02 | -03 |
|----------|-----|-----|-----|-----|
| Accuracy | 97.66% | 97.59% | 98.22% | 97.72% |

### 6.3 Contribution of data flow and control flow

We study the importance of the data and control flow information in the final code vector by performing the experiments listed in Sec. 5 by removing the data and control flow information. For this purpose we use two variants of obtaining the Instruction vector.
6.3.1 Symbolic Encoding: Without data and control flow information. In this, we fetch the encodings of the entities of a instruction \( l \) (Opcode \( O(l) \), Type \( T(l) \), and Arguments \( A_i(l) \) from the learnt seed embeddings without using reaching definitions (as explained in Sec. 4). The vector representing \( l \) is obtained using Eqn. 1. The vectors to represent a basic block, function and program are obtained exactly similar to the method in Sec. 4.

6.3.2 Localized Flow encoding: With data and control flow information within the Basic block. For this encoding, we use the encoding of the reaching definition only if the definition is within the basic block. Else, the seed encoding is used.

The results obtained for various experiments, carried out with the same experimental setup with the modified encodings are listed in the Tab. 10.

|                      | Program Classification - Accuracy | Device mapping - Accuracy | Device mapping - Speedup | Device mapping - Speedup |
|----------------------|----------------------------------|---------------------------|--------------------------|------------------------|
| Symbolic             | 73.5%                            | 87.82%                    | 2.44                     | 1.21                   |
| Localized Flow       | 95.5%                            | 89.16%                    | 2.45                     | 1.22                   |
| Proposed model       | 97.66%                           | 89.69%                    | 2.48                     | 1.21                   |

It can be seen that the proposed model performs better than the other variants. We can see the performance improvement over various tasks in the order of the explained model variants in the case of program classification. Similar speedup in the case of thread coarsening can be attributed to the small dataset. In either case, all the variants outperform the existing methods shown in the Sec. 5 for all the tasks.

7 CONCLUSIONS AND FUTURE WORK

We proposed a novel IR based encoding using flow analysis to represent programs with syntactic and semantic information. The seed embeddings were formed by modelling IR as relations, and the encoding was by using a translational model. This encoding was combined with liveness, use-def and reaching definition information, to form vectors at various levels of program abstraction like instruction, function and module.

When compared to earlier approaches, our method is non data-hungry, takes less training time, while maintaining a small vocabulary of only 64 entities. As we use entity level seed embeddings, we do not encounter any OOV issues. We compare our results with various similar approaches and show superior performance results while achieving high scalability. Though the IR gets transformed markedly across various optimization levels, our model remains resilient, and achieves analogous performance gains.

We envision that our framework can be applied to other applications which are beyond the scope of this work. IR2Vec can be extended to classify whether a program is malicious or not by looking for suspicious and obfuscated patterns. It can also be applied for detecting codes with vulnerabilities (like spectre and meltdown), and to identify the patterns of code and replace them with its optimized equivalent library calls. It can even be extended to predict the beneficial optimization sequence of a given program. Among many other applications, we believe that our approach has potential to automatically and program-theoretically synthesize IRs that can be used as test cases.
In future, we also plan to study the theoretical (fixpoint) properties of convergence of the encodings alluded in Sec. 4.3.4; the variety of programs for which solution converges, and for which it always diverge.

We plan to open-source our framework and data in due course of time.

REFERENCES

[ABBS14] Miltiadis Allamanis, Earl T. Barr, Christian Bird, and Charles Sutton. Learning natural coding conventions. In Proc. of the 22nd ACM SIGSOFT International Symp. on Foundations of Software Engineering, FSE 2014, pages 281–293, USA, 2014. ACM.

[ABBS15] Miltiadis Allamanis, Earl T. Barr, Christian Bird, and Charles Sutton. Suggesting accurate method and class names. In Proc. of the 2015 10th Joint Meeting on Foundations of Software Engineering, ESEC/FSE 2015, pages 38–49, USA, 2015. ACM.

[ABDS18] Miltiadis Allamanis, Earl T Barr, Premkumar Devanbu, and Charles Sutton. A survey of machine learning for big code and naturalness. ACM Computing Surveys (CSUR), 51(4):81, 2018.

[ABK18] Miltiadis Allamanis, Marc Brockschmidt, and Mahmoud Khademi. Learning to represent programs with graphs. In International Conference on Learning Representations, 2018.

[APS16] Miltiadis Allamanis, Hao Peng, and Charles A. Sutton. A convolutional attention network for extreme summarization of source code. In Proceedings of the 33nd International Conference on Machine Learning, ICML 2016, New York City, NY, USA, June 19-24, 2016, pages 2091–2100, 2016.

[ATGW15] Miltiadis Allamanis, Daniel Tarlow, Andrew Gordon, and Yi Wei. Bimodal modelling of source code and natural language. In Proceedings of the 32nd International Conference on Machine Learning, volume 37 of Proceedings of Machine Learning Research, pages 2123–2132, Lille, France, 07–09 Jul 2015. PMLR.

[AZLY18] Uri Alon, Meital Zilberstein, Omer Levy, and Eran Yahav. A general path-based representation for predicting program properties. In Proceedings of the 39th ACM SIGPLAN Conference on Programming Language Design and Implementation, PLDI 2018, pages 404–419, New York, NY, USA, 2018. ACM.

[AZLY19] Uri Alon, Meital Zilberstein, Omer Levy, and Eran Yahav. Code2vec: Learning distributed representations of code. Proc. ACM Program. Lang., 3(POPL):40:1–40:29, January 2019.

[BCV13] Yoshua Bengio, Aaron Courville, and Pascal Vincent. Representation learning: A review and new perspectives. IEEE Trans. Pattern Anal. Mach. Intell., 35(8):1798–1828, August 2013.

[Bit08] Bitbucket. Atlassian Bitbucket. https://www.bitbucket.org/, 2008. Accessed 2019-07-16.

[BL92] Thomas Ball and James R. Larus. Optimally profiling and tracing programs. In Proceedings of the 19th ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages, POPL ’92, pages 59–70, New York, NY, USA, 1992. ACM.

[BLvK18] James Bucek, Klaus-Dieter Lange, and Jóakim v. Kistowski. Spec cpu2017: Next-generation compute benchmark. In Companion of the 2018 ACM/SPEC International Conference on Performance Engineering, ICPE ’18, pages 41–42, New York, NY, USA, 2018. ACM.

[BNJH18] Tal Ben-Nun, Alice Shoshana Jakobovits, and Torsten Hoefler. Neural code comprehension: A learnable representation of code semantics. In Proceedings of the 32Nd International Conference on Neural Information Processing Systems, NIPS’18, pages 3589–3601, USA, 2018. Curran Associates Inc.

[BOL14] Sushil Bajracharya, Joel Oshner, and Cristina Lopes. Sourcerer: An infrastructure for large-scale collection and analysis of open-source code. Sci. Comput. Program., 79:241–259, January 2014.

[Boo18] Boost. Boost C++ Libraries. https://www.boost.org/, 2018. Accessed 2019-05-16.

[BUGD+13] Antoine Bordes, Nicolas Usunier, Alberto Garcia-Durán, Jason Weston, and Oksana Yakhnenko. Translating embeddings for modeling multi-relational data. In Proceedings of the 26th International Conference on Neural Information Processing Systems - Volume 2, NIPS’13, pages 2787–2795, USA, 2013. Curran Associates Inc.

[CFR91] Ron Cytron, Jeanne Ferrante, Barry K Rosen, Mark N Wegman, and P Kenneth Zadeck. Efficiently computing static single assignment form and the control dependence graph. ACM Transactions on Programming Languages and Systems (TOPLAS), 13(4):451–490, 1991.

[CLRS09] Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest, and Clifford Stein. Introduction to Algorithms, Third Edition. The MIT Press, 3rd edition, 2009.

[CPWL17] Chris Cummins, Pavlos Petoumenos, Zheng Wang, and Hugh Leather. End-to-end deep learning of optimization heuristics. In 2017 26th International Conference on Parallel Architectures and Compilation Techniques (PACT), pages 219–232. IEEE, 2017.

[Geek03] GeeksforGeeks. C/C++/Java programs. https://www.geeksforgeeks.org, 2003. Accessed 2019-08-15.

[Git08] GitHub. GitHub, Inc. https://www.github.com/, 2008. Accessed 2019-09-10.
[RVK15] V Raychev, M Vechev, and A Krause. Predicting program properties from "big code". In Proc. of the 42nd Annual ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages, POPL ’15, pages 111–124, USA, 2015. ACM.

[RZM11] Nathan Rosenblum, Xiaojin Zhu, and Barton P. Miller. Who wrote this code? identifying the authors of program binaries. In Proceedings of the 16th European Conference on Research in Computer Security, ESORICS’11, pages 172–189, Berlin, Heidelberg, 2011. Springer-Verlag.

[SVL14] Ilya Sutskever, Oriol Vinyals, and Quoc V. Le. Sequence to sequence learning with neural networks. In Proceedings of the 27th International Conference on Neural Information Processing Systems - Volume 2, NIPS’14, pages 3104–3112, Cambridge, MA, USA, 2014. MIT Press.

[VY16] Martin Vechev and Eran Yahav. Programming with "big code". Found. Trends Program. Lang., 3(4):231–284, December 2016.

[WCMAT16] Song Wang, Devin Chollak, Dana Movshovitz-Attias, and Lin Tan. Bugram: Bug detection with n-gram language models. In Proceedings of the 31st IEEE/ACM International Conference on Automated Software Engineering, ASE 2016, pages 708–719, New York, NY, USA, 2016. ACM.

[WEG87] Svante Wold, Kim Esbensen, and Paul Geladi. Principal component analysis. Chemometrics and intelligent laboratory systems, 2(1-3):37–52, 1987.

[WL94] Youfeng Wu and James R. Larus. Static branch frequency and program profile analysis. In Proceedings of the 27th Annual International Symposium on Microarchitecture, MICRO 27, pages 1–11, New York, NY, USA, 1994. ACM.

[WMWG17] Q. Wang, Z. Mao, B. Wang, and L. Guo. Knowledge graph embedding: A survey of approaches and applications. IEEE Transactions on Knowledge and Data Engineering, 29(12):2724–2743, Dec 2017.

[WSS18] Ke Wang, Rishabh Singh, and Zhendong Su. Dynamic neural program embeddings for program repair. In 6th International Conference on Learning Representations, ICLR 2018, Vancouver, BC, Canada, April 30 - May 3, 2018, Conference Track Proceedings, 2018.

[XWY17] Y. Xiong, J. Wang, R. Yan, J. Zhang, S. Han, G. Huang, and L. Zhang. Precise condition synthesis for program repair. In 2017 IEEE/ACM 39th International Conference on Software Engineering (ICSE), pages 416–426, May 2017.
The list of learned entities by IR2Vec is shown in Tab. 11.

| Opcodes       | Types       | Arguments |
|---------------|-------------|-----------|
| add           | floatTy     | CONST     |
| extractelement| integerTy   | FUNCTION  |
| fptoui        | pointerTy   | LABEL     |
| landingpad    | structTy    | PTR       |
| sdiv          | vectorTy    | VAR       |
| switch        | voidTy      |           |
| alloca        |             |           |
| extractvalue  |             |           |
| fptrunc       |             |           |
| and           |             |           |
| fadd          |             |           |
| fsub          |             |           |
| lshr          |             |           |
| sext          |             |           |
| udiv          |             |           |
| ashr          |             |           |
| fcmp          |             |           |
| getelementptr |             |           |
| atomicrmw     |             |           |
| fdiv          |             |           |
| icmp          |             |           |
| or            |             |           |
| shufflevector |             |           |
| unreachable   |             |           |
| bitcast       |             |           |
| fence         |             |           |
| insertelement |             |           |
| phi           |             |           |
| sitofp        |             |           |
| urem          |             |           |
| br            |             |           |
| fmul          |             |           |
| insertvalue   |             |           |
| ptrtoint      |             |           |
| srem          |             |           |
| xor           |             |           |
| call          |             |           |
| fpext         |             |           |
| inttoptr      |             |           |
| resume        |             |           |
| store         |             |           |
| zext          |             |           |
| cmpxchg       |             |           |
| fptosi        |             |           |
| invoke        |             |           |
| ret           |             |           |
| sub           |             |           |
## B LIST OF ANALOGIES

The list of analogies which were used for experimentation is shown below in Tab. 12.

| Based on Arguments                                                                 | Based on Inherent Semantic relations |
|------------------------------------------------------------------------------------|--------------------------------------|
| phi : variable :: load : pointer                                                    | and : or :: mul : shl                |
| call : function :: ret : constant                                                  | shl : lshr :: mul : udiv             |
| call : function :: ret : variable                                                  | shl : ashr :: mul : sdiv              |
| load : pointer :: store : variable                                                 | call : ret :: switch : label          |
| load : pointer :: store : constant                                                 | function : ret : switch : br          |
| alloca : variable :: cmpxchg : pointer                                             | load : store :: landingpad : invoke   |
| inttoptr : pointer :: ptrtoint : variable                                          | invoke : landingpad :: function : call |
| ptrtoint : pointer :: inttoptr : variable                                          | inttoptr : ptrtoint :: trunc : xext   |
| pointerty : pointer :: integerTy : variable                                       | inttoptr : ptrtoint :: trunc : xext   |
| pointerty : pointer :: integerTy : constant                                       |                                      |

| Based on Operands                                                                 |
|----------------------------------------------------------------------------------|
| fadd : fsub :: add : sub                                                        |
| add : fadd :: sub : fsub                                                        |
| fdiv : sdiv :: fmul : mul                                                        |
| add : sdiv :: fadd : fdiv                                                        |
| add : udiv :: fadd : fdiv                                                        |
| trunc : fptrunc :: icmp : fcmp                                                  |
| urem : srem :: udiv : sdiv                                                        |
| zext : fpext :: trunc : fptrunc                                                |
| trunc : sext :: fptrunc : fpext                                                  |

| Based on Operation type                                                         |
|----------------------------------------------------------------------------------|
| fcmp : floatTy :: icmp : integerTy                                               |
| uitofp : integerTy :: fptoui : floatTy                                          |
| inttoptr : integerTy :: ptrtoint : pointerTy                                    |
| insertvalue : structTy :: insertelement : vectorTy                              |
| phi : integerTy :: fadd : floatTy                                               |
| extractelement : vectorTy :: extractvalue : structTy                            |
| fpext : floatTy :: sext : integerTy                                             |

| Based on Return type                                                            |
|----------------------------------------------------------------------------------|
| shufflevector : vectorTy :: getelementptr : structTy                            |
| shufflevector : vectorTy :: getelementptr : integerTy                           |
| shufflevector : vectorTy :: getelementptr : voidTy                              |
| shufflevector : vectorTy :: getelementptr : floatTy                             |
| shufflevector : vectorTy :: getelementptr : pointerTy                           |
| load : pointerTy :: store : voidTy                                              |
| trunc : integerTy :: fptrunc : floatTy                                          |
| ptrtoint : integerTy :: inttoptr : pointerTy                                    |
| add : integerTy :: fadd : floatTy                                              |
| fsub : floatTy :: sub : integerTy                                              |
| fmul : floatTy :: mul : integerTy                                              |
| fdiv : floatTy :: sdiv : integerTy                                              |
| fdiv : floatTy :: udiv : integerTy                                              |
| srem : integerTy :: shufflevector : vectorTy                                    |
| zext : integerTy :: fpext : floatTy                                            |
| sext : integerTy :: fpext : floatTy                                            |
| fptosi : floatTy :: sitofp : integerTy                                          |