Design and Implementation of Finite Time Nonsingular Fast Terminal Sliding Mode Control for a Novel High Step-Up DC-DC Converter

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Abstract: In this paper, a new, high step-up quadratic boost converter with high conversion efficiency is discussed. A storage capacitor and resonant inductor are connected in series with a clamp capacitor through a diode. These compose a voltage multiplier cell, which is applied on the switch of the quadratic boost converter. The clamp capacitor can protect the switch from a voltage spike and absorb energy when the switch turns off; then, the storage capacitor and resonant inductor are charged by the energy stored in the clamped capacitor to increase the voltage transfer gain. In addition, the voltage multiplier cell can also reduce the voltage stresses of power devices. Then, a 16 V input, 200 V output prototype with 80 W nominal power is built up and tested. Furthermore, a finite time fast terminal sliding mode (NFTSM) control is proposed, with constant frequency for the voltageFundamental Building B213:tracking control of this converter. The new NFTSM is obtained by introducing an adjustable nonlinear term into fast terminal sliding mode (FTSM) control, and a singularity problem is avoided. The experiment illustrates that the maximum efficiency of the proposed converter achieves 95% at $D = 0.25$, $V_o = 150$ V. The voltage stress is reduced to half of the corresponding component of the basic boost converter at the same voltage level. Moreover, the proposed NFTSM controller can track the reference signal, and provide a short settling time of about 48 ms with no overshoot, and the system response exhibits strong robustness against 11.7% input voltage disturbance and 30% load variation.

Keywords: high step-up; multiplier cell; quadratic boost converter; fast terminal sliding mode; finite time convergence

1. Introduction

Recently, the fast development of electronics products, such as solar energies, uninterruptible power supplies (UPS), and electric automobiles have been witnessed [1–3]. DC-DC converters has been wildly applied to these applications. However, due to a low and varying input voltage of these applications, the boost converter is a convenient solution for step-up conversion. However, it is difficult for the conventional converter to provide such a high direct-current (DC) voltage gain. Moreover, many power devices of boost converters suffer from overlarge stress at a high output voltage level, leading to decreased efficiency [4].

Some scholars have strived to increase steady voltage gain and efficiency of boost converters. Some structures, such as the cascaded structure or switched-capacitor [5–7] can extend the steady voltage gain at a low cost. However, with the increase of voltage gain, more stages are adopted, leading to a complex circuit and significant current ripple [8]. In some isolated converters [9,10], much high-voltage conversion ratios can be achieved at a relatively low-duty cycle, but the leakage...
inductor of the magnetic elements may give rise to high voltage spikes and inevitable energy decreases. Furthermore, the volume and weight of power transformers are obstacles for a compact converter. A quadratic boost converter with a single switch can also boost the voltage gain with few components [11]. However, most previous converters may suffer from too much voltage stress, leading to reduced the conversion efficiency. The soft switch techniques [12] can recycle the leakage energy of magnetic elements, but at the price of increasing topology complexity. A voltage multiplier cell is a selectable option [13], which can not only alleviate voltage stress, but also improve the voltage gain.

A control strategy is indispensable to stabilize DC-DC converters against external disturbances. Many classical linear control methods which may achieve mediocre performance cannot even guarantee the stability, owing to the strong nonlinear property of boost converters. Therefore, some nonlinear control strategies, such as neural network control, adaptive control, and sliding mode control (SMC) [14–16] have been applied to it. The switch operation on the sliding mode surface of SMC is similar to the two operation states of the DC-DC converter (switch “ON” and “Off”) so that SMC is inherently appropriate to DC-DC converters. Moreover, SMC has characteristics of strong robustness and easy implementation, which is why SMC has generally been used on DC-DC converters. In earlier research, a hysteresis was adopted to relieve chattering and reduce switching frequency [17]. However, the variational switching frequency still exists, which may induce power losses and the electromagnetic interference (EMI) problem. To avoid this disadvantage, a fixed frequency SMC had been proposed [18,19] that can provide a constant operation frequency against external disturbances.

One disadvantage of the lineal sliding mode control is that the system can only converge to the equilibrium points asymptotically, leading to an infinite convergence time theoretically. Afterwards, a terminal sliding mode (TSM) control characterized by a nonlinear sliding mode was developed to guarantee finite-time convergence [20]. It can speed up the convergence rate near the equilibrium point, bringing about improved transient performance. However, this TSM control method cannot deliver a fast convergence speed when the system states have a distance from the equilibrium point. To ensure fast transient convergence in whole state space, a fast terminal sliding mode (FTSM) control was adopted [21]. The FTSM control ensures fast transient convergence in a whole convergence process. However, the previous TSM and FTSM methods may both endure a singularity problem. A few methods have been investigated to overcome this difficulty. One approach is the so-called two-phase control strategy. The trajectory was transferred to a specific region where no singularity occurs. Another approach is to add a saturation function to limit the amplitude of singularity term [22].

It should be noticed that these methods need an extra procedure to eliminate the singularity. In this paper, a novel nonsingular fast terminal sliding mode (NFTSM) is proposed without any additional procedures to avoid the singularity problem.

Also in this paper, a new high step-up converter with voltage multiplier is firstly addressed. This scheme is based on a combination of the quadratic boost converter with the voltage multiplier. Secondly, a novel finite-time NFTSM controller is designed for this converter. Finally, the new NFTSM controller is applied onto the proposed converter. Numerical simulations and experiments are provided to illustrate the effectiveness of the novel converter and controller. The arrangement of this paper is given as follows: the operation principle is introduced in Section 2; Section 3 discusses performance and key parameters; the NFTSM controller is designed and analysed in Section 4; the experimental results are introduced in Section 5; then, Section 6 concludes this paper.

Notations. Throughout this paper, Q is a switch; $L_1$, $L_2$ are input inductors, and $L_r$ is a resonant inductor; $C_1$, $C_o$, $C_r$, $C_c$ are capacitors; $D_1$, $D_2$, $D_3$, $D_4$, $D_o$ are diodes; and $R$ is a load, respectively. $V_{i\{1\}}$ denotes the voltage of across corresponding element; for example, $V_{i\{Q\}}$ represents the input voltage, and $V_{i\{D1\}}$, $V_{i\{D2\}}$, $V_{i\{D3\}}$, $V_{i\{D4\}}$, $V_{i\{D_o\}}$ stand for the voltages across of $D_1$, $D_2$, $D_3$, $D_4$, $D_o$. Analogously, $i_{i\{1\}}$ symbolise the current flowing through the corresponding element; for example, $i_{i\{D1\}}$, $i_{i\{D2\}}$, $i_{i\{D3\}}$, $i_{i\{D4\}}$, $i_{i\{D_o\}}$ represent the current flowing through $D_1$, $D_2$, $D_3$, $D_4$, $D_o$. $i_{i\{Q\}}$, $i_{i\{D2\}}$, $i_{i\{D3\}}$, $i_{i\{C_C\}}$, $i_{i\{C_r\}}$ denote the current flowing through the switch, and $L_2$, $L_r$, $C_C$, $C_r$ respectively. $V_{in}$ represents the input voltage source, and $V_s$ denotes the driving signal of the switch (Q), especially.
2. Topology of the Proposed High Step-Up DC-DC Converter

The proposed converter based on a quadratic boost converter and a clamp circuit consisted of $D_3$, $C_c$, and was applied on the switch ($Q$) to clamp the voltage of the switch and eliminate voltage spikes in the turned-off state. Then, $C_c$, $D_4$, $C_r$, $L_r$ were composed a multiplier cell so that capacitor $C_r$ could absorb energy from $C_c$ during the turned-on state of the switch in a resonant way, and release energy to the load ($R$) and output capacitor ($D_o$) during the turned-off state. By recycling the energy stored in $C_c$, the voltage gain of the proposed converter has been improved. The voltage stresses of output diode $D_o$ and switch $Q$ were halved compared to the conventional boost converter, and the conversion efficiency was promoted, owing to the clamp circuit. More detailed theoretical analyses can be found later on.

2.1. Operational Principles

Figure 1 plots the simplified equivalent circuit of the proposed converter. Some assumptions were postulated to simplify circuit analysis, as the following:

1. The converter works with high operation frequency, and all components are ideal;
2. $L_1, L_2$ are sufficiently large, such that the circuit operates under the current continuous mode (CCM);
3. $C_1, C_o$ are also large enough, such that the voltage across them are considered as a constant.

In accordance with above assumptions, a complete period mainly includes six operation modes, and the simplified equivalent circuit of every mode is shown in Figure 2. It restarts the whole process after mode 6 is finished.

![Figure 1. The equivalent circuit of the proposed converter.](image-url)

Mode 1 ($[t_0-t_1]$), (a): at the instant $t_0$, the switch $Q$ is turned off, $D_1, D_4, D_o$ are reverse biased, and $D_2, D_3$ are conducted. The input source ($V_{in}$) and $L_1, L_2$ release energy to $C_c$ through $D_3$, and to $C_1$ through $D_2$. During this mode, the converter can be modeled as follows:

$$\frac{di_{L1}}{dt} = -\frac{v_{C1}}{L_1}$$  \hspace{1cm} (1)$$

$$\frac{di_{L2}}{dt} = \frac{v_{C1} + v_{in} - v_{Cc}}{L_1}$$  \hspace{1cm} (2)$$

$$\frac{dv_{C1}}{dt} = \frac{i_{L1} - i_{L2} - i_{Cc}}{C_1}$$  \hspace{1cm} (3)$$

$$\frac{dv_o}{dt} = -\frac{v_o}{RC_o}$$  \hspace{1cm} (4)$$

$$\frac{dV_{Cc}}{dt} = i_{L2}$$  \hspace{1cm} (5)$$

where $i_{L1}, i_{L2}, i_{Lr}, i_{Cc}$ denote the current flowing through $L_1, L_2, L_r$, and $C_r$, respectively; $V_{in}, V_o, V_{C1}$ denote the averaged input voltage, output voltage, and the voltage across $C_1$.

Mode 2 ($[t_1-t_2]$), (b): at the instant $t_1$, $D_1, D_4$ are reverse biased, and $D_o$ begins to be conducted. The input source ($V_{in}$) and $L_1, L_2$ release energy to $C_c, C_1, R$, and $C_o$ unceasingly. $i_{L1}, i_{L2}$ decrease...
linearly until the switch is turned on. The resonant inductor current \( i_{Lr} \) increases linearly until it equals the input current \( i_{in} \). In this mode, the new dynamics of this converter can be modeled as follows:

\[
\frac{d i_{Lr}}{dt} = \frac{v_{Cc} + v_{Cr} - v_o}{L_r}
\]

(6)

\[
\frac{d v_{Cr}}{dt} = -\frac{i_{Lr}}{C_r}
\]

(7)

\[
\frac{d v_o}{dt} = \frac{i_{L2} - i_{Cc} - v_o/ R}{C_o}
\]

(8)

\( i_{Cc}=0 \)

Mode 3 ([t2–t3], (c)): at the instances \( t_2 \), \( D_3 \), \( D_1 \), \( D_4 \) is reverse biased, and \( D_2 \), \( D_o \) were conducted. The charging process of \( C_c \) was completed. The input source \( (V_{in}) \) and \( L_1 \), \( L_2 \) release energy to \( R \) and \( C_o \), sequentially. In this mode, the extra dynamics of this converter can be modeled as follows:

\[
\frac{d i_{Lr}}{dt} = \frac{v_{Cr} - v_o}{L_r}
\]

(10)

\[
\frac{d i_{L1}}{dt} = \frac{v_{in}}{L_1}
\]

(11)

\[
\frac{d i_{L2}}{dt} = \frac{v_{in} + v_{C1}}{L_2}
\]

(12)

\[
\frac{d v_{C1}}{dt} = -\frac{i_{L2}}{C_1}
\]

(13)

\( V_{in} \)

\( L_1 \)

\( L_2 \)

\( C_c \)

\( C_o \)

\( R \)

\( i_{Lr} \)

\( v_{Cc} \)

\( v_{Cr} \)

\( v_o \)

\( i_{Cc} \)

\( i_{in} \)

\( i_{L2} \)

\( v_{C1} \)

\( D_1 \)

\( D_2 \)

\( D_3 \)

\( D_4 \)

\( D_o \)

\( t_2 \)

\( t_3 \)

\( t_4 \)

\( (a) \)

\( (b) \)

\( (c) \)

\( (d) \)

\( (e) \)

\( (f) \)
Mode 5 ([t₄–t₅], (e)): at the instances t₄, D₂, D₃, D₆ it is reverse-biased. The resonant process starts when Dₒ is reverse-biased. The diode D₄ transfers energy stored in Cₒ to Cᵣ in a resonant way [23]. D₄ is blocked when half of the resonant period is completed at the instant t₅. It is noticed that the average output voltage of the proposed converter is equal to the average voltage across Cᵣ, plus the voltage of Cₒ. The new dynamics in this mode can be modeled as follows:

\[
d\frac{v_o}{dt} = -\frac{v_o}{R} \quad \text{(14)}
\]

\[
i_{LR} = \frac{(V_{CC} - V_{CR})\sin(\omega_0 t)}{\sqrt{L/C_{eq}}} \quad \text{(15)}
\]

\[
d\frac{V_{CC}}{dt} = -i_{LR} \quad \text{(16)}
\]

\[
C_{eq} = \frac{C_o C_r}{C_o + C_r} \quad \text{(17)}
\]

\[
\omega_0 = \frac{1}{\sqrt{L C_{eq}}} \quad \text{(18)}
\]

where Cₑq denotes the equivalent capacitance of the multiplier cell, and ω₀ is the angular frequency of this cell.

Mode 6 ([t₅–t₆], (f)): at the instant t₅, the resonant process stops, and D₄ is reverse biased. L₁, L₂ store energy from the input source (Vᵢn) and C₁ sequentially until the switch is turned off. A new period restarts from mode 1. In this mode, the new dynamics can be modeled as follows:

\[
i_{LR} = 0 \quad \text{(19)}
\]

Figure 3. Key operation waveforms.
Figure 3 shows the theoretical operation waveforms of some key variables in a case of a duty cycle \( D = 0.5 \) to exhibit operating principles of the converter ulteriorly. The time period from \( t_0 - t_6 \) represents a complete operating cycle, where \( t_0 - t_3 \) represents a duration of the switch turned off, and \( t_4 - t_6 \) represents a duration of the switch turned on.

Observing Figure 3, one can see that the resonant inductor current \( i_{Lr} \) starts to rise at \( t_1 \) until it reaches the value of \( i_{L2} \), and then decreases linearly during \( t_2 - t_3 \). A half period of a resonant procedure is completed during \( t_4 - t_5 \).

2.2. Performance Analysis

2.2.1. The Voltage Gain

To simplify the analysis, only modes 2, 3, 5, and 6 were considered, while modes 1, 4 were neglected due to their short duration and micro-variation of the related variables. During modes 2 and 3, the switch was turned off, and \( L_1 \) and \( L_2 \) started to release energy to \( C_1, C_c, R \). The voltage of inductors functions are described in (1), (2).

When the switch is turned on during modes 5 and 6, \( L_1, L_2 \) start to store energy from the input source \( V_{in} \) and \( C_1 \), demonstrated in (11)–(12). When the circuit arrives at a steady state, using the inductor voltage-second balance principle on the inductors \( L_1 \) and \( L_2 \) in the whole period, the following equations can be achieved:

\[
\frac{di_{L1}}{dt} = -\frac{v_{C1}(1 - D) + v_{in}D}{L_1} = 0 \tag{20}
\]

\[
\frac{di_{L2}}{dt} = \frac{(v_{in} + v_{C1} - v_{Cc})(1 - D) + (v_{in} + v_{C1})D}{L_2} = 0 \tag{21}
\]

where \( D \) denotes the duty cycle.

According to (20)–(21), the steady voltage of \( C_1 \) and \( C_c \) can be obtained by:

\[
V_{C1} = \frac{1 - D}{D} V_{in} \tag{22}
\]

\[
V_{Cc} = \frac{1}{(1 - D)^2} V_{in} \tag{23}
\]

The average voltage of \( C_r \) is equal to the average voltage across \( C_c \) because it is charged by \( C_c \) during mode 5. Moreover, \( C_r \) is connected in series with the output of the quadratic converter. The output voltage gain of this converter is given by:

\[
M = \frac{V_o}{V_{in}} = \frac{V_{Cc} + V_{Cr}}{V_{in}} = \frac{2}{(1 - D)^2} \tag{24}
\]

The voltage gain of boost converter is expressed as:

\[
M_b = \frac{1}{1 - D} \tag{25}
\]

According to [11], the voltage gain of the quadratic boost converter is given by:

\[
M_q = \frac{1}{(1 - D)^2} \tag{26}
\]

The comparison between the voltage gain and duty cycle of the proposed converter and other converters are plotted in Figure 4. According to Equations (24)–(26) and from Figure 4, one can observe that the voltage gain of the proposed converter is higher than that of a conventional boost converter and twice as much as that of quadratic converter under the same duty cycle. The voltage gain of the
converter in [9] where a coupling inductor exists is higher than the proposed converter at the duty cycle under 0.55. However, the proposed converter provides the highest voltage gain among these converters when the duty cycle is larger than 0.55.

![Figure 4. Voltage gain comparison of converters.](image)

2.2.2. The Power Device Stresses

The voltage across the switch (Q) equals \( V_o \) when it is turned off. During modes 1, 5, and 6, \( D_o \) is reverse biased, meaning this voltage of \( D_o \) can be described as follows:

\[
V_{D_o} = V_o - V_{Cr} = \frac{V_o}{2} \tag{27}
\]

The maximum voltage stresses of the switch (Q) and output diode (\( D_o \)) compared with those in [9,10] are given in Table 1. \( n, k \) represent the turns ratio of a coupling-inductor and switching capacitor stages in Table 1. It shows that the voltage stresses are half of those of a quadratic converter and boost converter at the same voltage level. The voltage stress in converters [9,10] changes with the duty cycle. Moreover, the switching voltage stresses of the proposed converter is also smaller than that of converters in [9,10].

| Key Power Devices | The Proposed Converter | The Converter in [9] | The Converter in [10] | The Boost Converter | The Quadratic Converter |
|-------------------|------------------------|----------------------|-----------------------|---------------------|-----------------------|
| \( Q \) \( D_o \) | \( V_o/2 \) \( V_o/2 \) | \( \frac{2V}{3+D} \) \( \frac{2V}{2(1-D)} \) | \( \frac{2V}{2+nDk} \) \( \frac{2V}{2+nDk} \) | \( V_o \) \( V_o \) |

2.3. Key Parameters Design

Input inductances: When the switch is turned on, the current variation of the input inductor \( L_1 \) and \( L_2 \) can be described by:

\[
\Delta i_{L_1} = \frac{V_{in}}{L_1} DT \tag{28}
\]

\[
\Delta i_{L_2} = \frac{V_{in}}{(1-D)L_2} DT \tag{29}
\]

The average current of the input inductor \( L_1 \) and \( L_2 \) in the whole period can be described by:
\[ i_{L_{2ss}} = \frac{V_o}{R(1-D)} \]  
(30)

\[ i_{L_{2ss}} = \frac{V_o}{R(1-D)} \]  
(31)

To ensure that the proposed converter is operating in CCM, the current variation (\( \Delta i_{L_1}, \Delta i_{L_2} \)) of input inductors \( L_1 \) and \( L_2 \) must be smaller than double that of the average current (\( i_{L_{2ss}}, i_{L_{2ss}} \)) in the whole period.

\[ \Delta i_L \leq 2i_{ss} \]  
(32)

According to (28)–(32), the inductances are given by:

\[ L_1 \geq \frac{(1-D)^3DR}{4f} \]  
(33)

\[ L_2 \geq \frac{(1-D)^2DR}{4f} \]  
(34)

where \( f \) denotes the switching frequency.

Stored capacitors: \( \Delta V_{C_o} \), representing the voltage ripple of \( C_o \), can be described by:

\[ \Delta V_o = \frac{i_o DT}{C_o} \]  
(35)

According to (31), the capacitances of \( C_o \) are calculated by:

\[ C_o \geq \frac{V_oD}{\Delta V_o Rf} \]  
(36)

thus, the capacitance of \( C_1 \) is also calculated by

\[ C_1 \geq \frac{V_{C_1D}}{\Delta V_{C_1 Rf}} \]  
(37)

Voltage multiplier capacitors: The maximum output power is limited by the energy stored in \( C_c, C_r \). The output voltage will decrease if the load power increases above that of the nominal output power (\( P_{\text{max}} \)) [24]. In other words, the voltage multiplier will lose voltage boost effect and only operate as a clamp circuit. The capacitance of \( C_c \) should be about ten times larger or more than \( C_r \). The minimum capacitance of \( C_c \) is calculated by:

\[ C_c \geq \frac{P_{\text{max}}}{V_{C_c^2 f}} \]  
(38)

Resonant inductor: Half of the resonant period must be smaller than the duration of the switch turned on.

\[ \frac{T_r}{2} < DT \]  
(39)

where \( T_r \) denotes the resonant period of the voltage multiplier cell, and \( T \) denotes the switching period.

According to (39), the resonant inductance and capacitance must satisfy the following inequality:

\[ \sqrt{L_r C_{eq}} < \frac{D}{\pi f} \]  
(40)

The resonant inductor limits the current variation of the switch. Thus, the inductance can be selected according to the maximum current rate of change of an actual switch device. The minimum inductance is calculated by:
\[ L_r \geq \frac{V_o - V_{C_r}}{\Delta i/dt_{\text{max}}} \]  

(41)

where \( \Delta i/dt_{\text{max}} \) is the maximum current change rate of the switch.

3. Modeling of the Proposed Converter

According to the aforementioned assumption and analysis, modes 1 and 4 were neglected. The current flowing into \( C_c \) was also neglected. The voltages of \( C_c \) and \( C_r \) were considered as a constant. During modes 2 and 3, the switch was turned off, and the relative state equations can be described as (1)–(3) and

\[ \frac{di_{L1}}{dt} = i_{L2} - \frac{v_o}{R_C} \]  

(42)

During modes 5 and 6, the switch was turned on, and the relative state equations can be described as (11)–(14). Thus, the switch model of the proposed converter operating in CCM can be written as:

\[
\begin{cases}
L_1 \frac{di_{L1}}{dt} = V_{in}u - V_{C1}(1 - u) \\
L_2 \frac{di_{L2}}{dt} = V_{in} + V_{C1} - \frac{V_o}{2} (1 - u) \\
C_1 \frac{dV_{C1}}{dt} = -i_{L2} + i_{L1}(1 - u) \\
C_o \frac{dV_o}{dt} = -\frac{V_o}{R} + i_{L2}(1 - u) 
\end{cases}
\]  

(43)

where \( u \) is the control input which takes “0” to be the turned-off state and “1” as the turned-on state of the switch, respectively.

To design the proposed finite sliding mode controller for the converter, the output voltage \( V_o \) was set as the control variable. The tracking error can be explicated as:

\[ e_1 = V_r - V_o \]  

(44)

where \( e_1 \) is the voltage error, and \( V_r \) is the reference voltage.

Taking the derivative of (44), one can obtain a differential equation. Then, substituting (43) into this equation yields:

\[
\begin{aligned}
\dot{e}_1 &= e_2 \\
\dot{e}_2 &= -\frac{e_2}{R C_o} - \frac{(V_{in} + V_{C1} - V_o/2)}{L_2 C_o}(1 - u)
\end{aligned}
\]  

(45)

4. Improved Finite Time Fast Terminal Sliding Mode

Many typical TSM and FTSM can be described as:

\[ S_1 = \dot{x} + k_1 x^p = 0 \]  

(46)

\[ S_2 = \dot{x} + k_1 x^p + k_2 x^a = 0 \]  

(47)

where \( k_1 > 0, k_2 > 0, p > q, a \) is formed of \( q/a \) or \( p/a \), and \( p, q, p/a, q/a \) are both positive odd integers satisfying \( p > q, a \geq 1 \), respectively.

It is evident that TSM (\( S_1 \)) accelerates the convergence rate within the vicinity of the equilibrium point and the state trajectory converges the sliding surface in finite time, owing to the non-linearly term \( x^p \). However, TSM also offers a relatively slow convergence rate when the system trajectory stays at a distance from the equilibrium point. Based on (42), it can be concluded that the dynamics are globally finite-time stable, and it reaches the steady state within the time:

\[ T_1 = \int_0^{\mid x(0) \mid} \frac{1}{k_1 x^p} dx = \left( \frac{p}{k_1 (p-q)} \right) \mid x(0) \mid^{1-p} \]  

(48)

In FTSM, \( k_2 x^a \) guarantees the convergence rate when the system dynamic is far away from the equilibrium point. Moreover, \( k_1 x^p \) determines finite time convergence when the system state trajectory
is close to the equilibrium point. Thus, the dynamic converges quickly in the whole convergence process, and converges to an equilibrium point within the time:

\[
T_2 = \int_0^{\|x(0)\|} \frac{1}{k_1 x^q + k_2 x^p} dx = \frac{p \|x(0)\|^{(p-q)/p}}{p-q} k_1^{(p-q)/q} \int_0^{\|x(0)\|} \frac{1}{x^q + k_2^{1-x/a}} \left( 1, \frac{(q-p)/p, (2q-p)/p-a}{q/p-a}; -k_2 k_1^{-1} x(0)^{a-q/p} \right)
\]  

(49)

where \(F(\cdot)\) represents the Gauss’ Hypergeometric Function \([25]\), and the coefficients of \(\frac{q}{p}, a, k_1, k_2\) attract \(F(\cdot)\) to keep convergent.

In order to accelerate the convergence rate further, an improved NFTSM scheme was proposed as follows:

\[
S_3 = x + k_1 (x + k_3 x^b)^a + k_2 x^c
\]

(50)

where \(k_1 > 0, k_2 > 0, k_3 > 0, b, c\) are also formed of \(q_b/p_b, q_c/p_c\) respectively. \(p_b, q_b, p_c, q_c\) are both positive odd integers satisfying \(1 < c < 2, a > c, b > 1\). It is concluded that the system will arrive at the equilibrium point, and the convergence time is given by:

\[
T_3 = \int_0^{\|x(0)\|} \frac{1}{k_2 x^q + k_1 (x + k_3 x^b)^a + k_2 x^c} dx \leq \int_0^{\|x(0)\|} \frac{1}{k_1 x^q + k_2 x^p} dx = T_2 \leq T_1
\]

(51)

From the above equation, it is observed that the convergence time of \(S_3\) is shorter than \(T_1\) and \(T_2\) because of the extra item, \(k_3 x^b\).

There is a convergence performance comparison between TSM, FTSM, and the improved NFTSM. The following sliding modes are considered:

\[
S_1 = \dot{x} + x^3 = 0, S_2 = \dot{x} + x^3 + x^5 = 0, S_3 = x + (x + x^3)^5 + x^5 = 0
\]

(52)

with the initial value \(x(0) = 10\). The corresponding response curves are given by Figure 5. It can be seen that the improved NFTSM (\(S_3\)) has a faster convergence rate than FTSM (\(S_2\)) and TSM (\(S_1\)).

\[\text{Figure 5. The comparison of convergence performance between NFTSM, FTSM, and TSM.}\]

5. Controller Design of DC-DC Converter

Now, consider the dynamical system (45), according to the scheme of NFTSM, the switching surface is defined as follows:

\[
S_3 = x + k_1 (x + k_3 x^b)^a + k_2 x^c
\]

(53)
For the proposed converter with a single switch, a general control law satisfying the hitting condition can be plotted as:

\[ u = \begin{cases} 
1 = \text{'ON'}, & S_3 > 0 \\
0 = \text{'OFF'}, & S_3 < 0 
\end{cases} \] (54)

To guarantee that the system state stays within the vicinity of the sliding surface, the existence condition derived from Lyapunov’s direct method must be obeyed:

\[ \lim_{S \to 0} S S_3 \dot{} < 0 \]

where \( S_3 \) is the time derivative of \( S_3 \), and is shown as follows:

\[ S_3 = \left[ 1 + k_1a \left( e + k_3eb \right)^{a-1} \left( 1 + k_3be^{b-1} \right) \right] e_2 - k_2 c e_2^{-1} \left( \frac{e_2}{R C_o} + \frac{V_{in} + V_{C1} - V_o/2}{L_2 C_o} \right) (1-u) \] (56)

Substituting (56) into (55) gives the following existence condition:

\[ 0 < \frac{k_2 c e_2^2}{R C_o} \left[ 1 + k_1a \left( e + k_3eb \right)^{a-1} \left( 1 + k_3be^{b-1} \right) \right] e_2 \left( \frac{k_2 c e_2 c^{-1} (V_{in} + V_{C1} - V_o/2)}{L_2 C_o} \right) \] (57)

every coefficient must be satisfied by (57), considering the minimum of the load.

To overcome a variable switching frequency of this system suffering external disturbance, an equivalent sliding mode control with constant operation frequency is adopted. Equating \( \dot{S}_3 = 0 \) (58)

yields the equivalent control input:

\[ u_{eq} = 1 + L_2 C_o \left\{ \left[ 1 + k_1a \left( e + k_3eb \right)^{a-1} \left( 1 + k_3be^{b-1} \right) \right] \left( \frac{i_{in}}{C_o} \right)^{2-c} + \frac{i_{in}}{C_o} \right\} \] (59)

To improve the transient response, an exponential reaching law is chosen, and can be expressed as:

\[ \dot{S}_3 = -k_4 S_3 - k_5 \text{sign}(S_3) \] (60)

where \( k_4, k_5 \) are positive parameters.

When (60) is solved for \( u \), the control input can be obtained as:

\[ u = 1 + L_2 C_o \left\{ \left[ 1 + k_1a \left( e + k_3eb \right)^{a-1} \left( 1 + k_3be^{b-1} \right) \right] \left( \frac{i_{in}}{C_o} \right)^{2-c} + \frac{i_{in}}{C_o} + k_4 S_3 + k_5 \text{sign}(S_3) \right\} \] (61)

Finally, the control input \( u \) and ramp signal \( V_{ramp} = 1 \) with a constant frequency were fed into a pulse-width modulator to produce the practical control input. Thanks to \( u \), the system converged quickly to an equilibrium point within a finite time. It should be noted that no singularity exists during the whole process, owing to \( 0 < c < 2 \).

**Theorem 1.** For the system (45), when the control input is chosen as (61), the system trajectory will then converge quickly to a steady state within a finite time.
Proof of Theorem 1. Consider the Lyapunov function candidate as:

\[ V = \frac{1}{2} S^2 \]  

whose time derivative is

\[ \dot{V} = SS' \]

\[ = -k_2k_4c_1e_1^{e_1-1}S^2 - k_2k_5c_1^{e_1-1}|S| \]  

It can be seen that when \( \dot{e}_1 \neq 0, \dot{V} \leq 0 \), the system state will slide to the sliding mode \( S = 0 \) within a finite time. When \( \dot{e}_1 = 0 \), by substituting (61) into the second equation of (45), one can obtain:

\[ \dot{e}_2 = -\frac{\left[ 1 + k_1a(e + k_3e_2)^{e_2-1} \right]}{k_2c}e_2^{\alpha - c} - k_4S - k_5sgn(S) \]  

Equation (64) can be rewritten as:

\[ \dot{e}_2 = -k_4S - k_5sgn(S) \]  

This equation indicates that \( \dot{e}_2 < -k_5 \) for \( S > 0 \) and \( \dot{e}_2 > k_5 \) for \( S < 0 \). Therefore, the system trajectory will continue moving to an equilibrium point instead of staying on the state of \( e_1 \neq 0 \) and \( e_2 = 0 \). Moreover, it can be assumed that there exists a vicinity of \( e_2 = 0 \), \( |e_2| \leq \delta \) (\( \delta \) is a positive constant) and satisfying \( \dot{e}_2 < -k_5 \) for \( S > 0 \) and \( \dot{e}_2 > k_5 \) for \( S < 0 \), respectively. Therefore, the crossing of trajectories between two boundaries of \( |e_2| \leq \delta \) is achieved in a finite time, and the trajectory from the region \( |e_2| \geq \delta \) reach the boundaries in finite time too. It can be summarized that the system controlled by (61) can converge to \( S = 0 \) from any initial state within a finite time. This completes the proof. \[ \square \]

6. Experimental Results

To illustrate the effectiveness of the previous theoretical analysis, a laboratory prototype of the proposed converter was built and experimented. The related parameters of this system are shown in Table 2.

| Components | \( L_1 \) | \( L_2 \) | \( L_r \) | \( C_1 \) | \( C_r \) | \( C_c \) | \( C_o \) | \( R \) | \( f \) | \( V_{in} \) |
|------------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| value      | 150 \( \mu \)H | 200 \( \mu \)H | 1 \( \mu \)H | 470 \( \mu \)F | 47 \( \mu \)F | 47 \( \mu \)F | 470 \( \mu \)F | 500 \( \Omega \) | 40 kHz | 16 V |

| Components | \( V_o \) | \( k_1 \) | \( k_2 \) | \( k_3 \) | \( k_4 \) | \( k_5 \) | \( a \) | \( b \) | \( c \) |
|------------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| value      | 200 V    | 10       | 3.4      | 33       | 0.1      | 10       | 3        | 2 \( \frac{1}{2} \) | 5 \( \frac{5}{2} \) |

Figure 6 shows the voltage waveforms across the switch and output diode (\( D_o \)), respectively when the output voltage is at 200 V. From (a), it shows that the voltage of the switch equals to 100 V at the “OFF” state, with a small voltage spike about 10 V at the moment when the switch turned off. The subgraph (b) shows that the anode voltage of the output diode (\( D_o \)) to the ground reaches 100 V at the reversed state when the cathode voltage is at 200 V with no voltage spike. One can see that the voltage stress of the output diode arrives at 100 V equalling to half of the output voltage too. Therefore, the voltage stresses of the output diode and switch have been alleviated.

Figure 7a indicates that the switching waveform maintains about four periods in a grid that represents 100 \( \mu \)s against a variational output voltage. One can see that the equivalent control (\( u \)) keeps the switching period constant, at about 25 \( \mu \)s.

The efficiency versus a wide range of duty cycle and output voltage is plotted in Figure 7b. It shows that the peak efficiency reaches 95% at \( D = 0.25, V_o = 150 V \). The efficiency reduces with the
increase of the duty cycle, due to an increasing duty cycle accompanied by a more severe conduction loss of the switch and reverse loss of diodes. In addition, the efficiency, at a 150 V output voltage, only has a small advantage than when the output voltage is 200 V, meaning that the output voltage also has a slight impact on the efficiency. This is because the improved output voltage aggravates the heat loss of inductors and capacitors.

An experiment was also carried out for the performance analysis of the proposed NFTSM controller. The result is given in Figures 8–10. The startup transient response is shown in Figure 8, the output voltage against input voltage variation plots in Figure 9, and the output voltage versus load disturbance is illustrated in Figure 10, respectively.

**Figure 6.** The performance of the proposed converter: (a) the voltage wave of the switch ($Q$); (b) the voltage wave of the output diode ($D_o$).

**Figure 7.** The experiment performance of the proposed converter: (a) the switching frequency against the output voltage variation; (b) the efficiency versus duty cycle and output voltage.

**Figure 8.** The transient response of the system: (a) controlled by the TSM controller ($S_1$); (b) controlled by the FTSM controller ($S_2$); (c) controlled by the proposed NFTSM controller ($S_3$).
Figure 8 shows the transient response of the output voltage. Figure 8c, one can seen that the output voltage controlled by the proposed controller can track the reference value (200 V) with no overshoot, and has a settling time about 48 ms. Figure 8a, the system controlled by the TSM controller ($S_1$) takes 104 ms to reach the reference value (200 V), and the system controlled by the FTSM controller ($S_2$) has a settling time of 64 ms in Figure 8b. We can notice that the proposed controller has a 29.4%, 64.8% settling time improvement than FTSM and TSM, respectively, in this system.

Figure 9 shows the steady output voltage ($V_o$) comparison against input voltage disturbance. The input voltage changes from 17 V to 15 V (11.7%) and then returns to 17 V. From the Figure 9c, the output voltage ($V_o$) response exhibits no obvious variation. Figure 9a, one can see that the output voltage ($V_o$) response controlled by the TSM controller ($S_1$) takes about 100 ms to recover to the reference value, accompanied by a variation of 10 V (5%). The output voltage ($V_o$) response controlled by the FTSM controller ($S_2$) has a 80 ms recovery time, and a variation of 10 V too in Figure 9b. However, a sharp voltage spike was not visible in the three responses.

![Figure 9](image1.png)

*Figure 9. The response of the system versus input voltage variation: (a) controlled by the TSM controller ($S_1$); (b) controlled by the FTSM controller ($S_2$); (c) controlled by the proposed NFTSM controller ($S_3$).*

The steady output voltage response versus the output load variation is demonstrated in Figure 10. Here, resistance changes of $-150 \, \Omega$ ($-30\%$ variation) were added to a nominal output load of 500 $\Omega$, and then the load returned to 500 $\Omega$. Figure 10c, one can see that the output voltage controlled by the proposed controller almost remains constant at the reference value. Figure 10a, the output voltage controlled by the TSM ($S_1$) controller has a slight voltage variation of about 8 V, and takes about 60 ms of recovery time after the moment where the load’s resistance has been decreased, and has a settling time of 25 ms with a variation of 8 V after the moment of the load’s resistance turns back. Figure 10b, the output voltage controlled by the FTSM ($S_2$) controller has 80 ms recovery time with a variation of 5 V after the instant where the load’s resistance is been changed the first time; then, it takes 40 ms to reach the reference signal with a small variation after the moment of the load’s resistance turning back. According to Figures 9 and 10, it can be seen that the proposed NFTSM controller has the strongest robustness amongst the three methods. Based on the above results, it can be noticed that the proposed controller has faster convergence time and greater robustness compared with the TSM ($S_1$) and FTSM ($S_2$) controller. Thus, the proposed control scheme is more superior than the TSM and FTSM control strategies for the high step-up converter. In addition, there was no sharp voltage spike in the voltage waveforms of the switch, diodes, and output voltage at different test conditions, meaning that some low-cost elements can be used.
7. Conclusions

A high step-up DC-DC converter based on a single-switch quadratic boost converter and a limited time converge fast terminal sliding mode control strategy was proposed in this paper. Firstly, the operation modes, performance discussion, and key parameter design of the proposed converter were presented. Owing to the voltage multiplier cell, the voltage gain of the proposed converter was highly enhanced; in particular, the peak efficiency reached 95% at an output voltage range of (100 V–200 V). At the mean time, the voltage stresses of the switch and diodes ($D_3$, $D_4$, $D_0$) were decreased to half of the output voltage, and the conversion efficiency was improved. Then, a new finite-time NFTSM scheme was proposed. This can provide a faster convergence rate and stronger robustness than the conventional TSM and FTSM schemes. In particular, the singularity problem does not exist during the whole convergence process. Finally, the proposed controller was applied to the converter to stabilize it and track the reference signal. The experiment demonstrates that the system controlled by the proposed controller can track the reference voltage with a short settling time of about 48 ms and no overshoot. The strong robustness of the proposed controller against input voltage variation and load disturbances was also verified.

Author Contributions: Y.L. designed the NFTSM controller and accomplished the theoretical proof; J.W. designed the topology of the proposed converter, implemented the experiments, and wrote the paper; H.T. designed the circuit and analysed the data.

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