Improving Multi-Application Concurrency Support Within the GPU Memory System

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ABSTRACT
GPUs exploit a high degree of thread-level parallelism to efficiently hide long-latency stalls. Thanks to their latency-hiding abilities and continued improvements in programmability, GPUs are becoming a more essential computational resource. Due to the heterogeneous compute requirements of different applications, there is a growing need to share the GPU across multiple applications in large-scale computing environments. However, while CPUs offer relatively seamless multi-application concurrency, and are an excellent fit for multitasking and for virtualized environments, GPUs currently offer only primitive support for multi-application concurrency.

Much of the problem in a contemporary GPU lies within the memory system, where multi-application execution requires virtual memory support to manage the address spaces of each application and to provide memory protection. In this work, we perform a detailed analysis of the major problems in state-of-the-art GPU virtual memory management that hinders multi-application execution. Existing GPUs are designed to share memory between the CPU and GPU, but do not handle multi-application support within the GPU well. We find that when multiple applications spatially share the GPU, there is a significant amount of inter-core thrashing on the shared TLB within the GPU. The TLB contention is high enough to prevent the GPU from successfully hiding stall latencies, thus becoming a first-order performance concern.

Based on our analysis, we introduce MASK, a memory hierarchy design that provides low-overhead virtual memory support for the concurrent execution of multiple applications. MASK extends the GPU memory hierarchy to efficiently support address translation through the use of multilevel TLBs, and uses translation-aware memory and cache management to maximize throughput in the presence of inter-application contention. MASK uses a novel token-based approach to reduce TLB miss overheads, and its L2 cache bypassing mechanisms and application-aware memory scheduling reduce the interference between address translation and data requests. MASK restores much of the thread-level parallelism that was previously lost due to address translation. Relative to a state-of-the-art GPU TLB, MASK improves system throughput by 45.2%, improves IPC throughput by 43.4%, reduces unfairness by 22.4%, and MASK performs within 23% of the ideal design with no translation overhead.

1. INTRODUCTION
Graphics Processing Units (GPUs) provide high throughput by exploiting a high degree of thread-level parallelism. A GPU executes a group of threads (i.e., a warp) in lockstep (i.e., each thread in the warp executes the same instruction concurrently). When a warp stalls, the GPU hides the latency of this stall by scheduling and executing another warp. The use of GPUs to accelerate general-purpose GPU (GPGPU) applications has become common practice, in large part due to the large performance improvements that GPUs provide for applications in diverse domains [20, 22, 32, 34, 77]. The compute density of GPUs continues to grow, with GPUs expected to provide as many as 128 streaming multiprocessors per chip in the near future [10, 85]. While the increased compute density can help many GPGPU applications, it exacerbates the growing need to share the GPU streaming multiprocessors across multiple applications. This is especially true in large-scale computing environments, such as cloud servers, where a diverse range of application requirements exists. In order to enable efficient GPU hardware utilization in the face of application heterogeneity, these large-scale environments rely on the ability to virtualize the compute resources and execute multiple applications concurrently [4, 17, 38, 39].

The adoption of discrete GPUs in large-scale computing environments is hindered by the primitive virtualization support in contemporary GPUs. While hardware virtualization support has improved for integrated GPUs [19], the current virtualization support for discrete GPUs is insufficient, even though discrete GPUs provide the highest available compute density and remain the platform of choice in many domains [1]. Two alternatives for discrete virtualization are time multiplexing and spatial multiplexing. Emerging GPU architectures support time multiplexing the GPU by providing application preemption [57, 65], but this support currently does not scale well with the number of applications. Each additional application introduces a high degree of con-
tention for the GPU resources (Section 2.1). Spatial multiplexing allows us to share a GPU among applications much as we currently share CPUs, by providing support for multi-address-space concurrency (i.e., the concurrent execution of kernels from different processes or guest VMs). By efficiently and dynamically managing the kernels that execute concurrently on the GPU, spatial multiplexing avoids the scaling issues of time multiplexing. To support spatial multiplexing, GPUs must provide architectural support for memory virtualization and memory protection domains.

The architectural support for spatial multiplexing in contemporary GPUs is not well-suited for concurrent multi-application execution. Recent efforts at improving address translation support within GPUs [25, 67, 68, 84, 94] eschew MMU-based or IOMMU-based [7, 9] address translation in favor of TLBs close to shader cores. These works do not explicitly target concurrent multi-application execution within the GPU, and are instead focused on unifying the CPU and GPU memory address spaces [6]. We perform a thorough analysis of concurrent multi-application execution when these state-of-the-art address translation techniques are employed within a state-of-the-art GPU (Section 2.1). We make four key observations from our analysis. First, we find that for concurrent multi-application execution, a shared L2 TLB is more effective than the highly-threaded page table walker and page walk cache proposed in [68] for the unified CPU-GPU memory address space. Second, for both the shared L2 TLB and the page walk cache, TLB misses become a major performance bottleneck with concurrent multi-application execution, despite the latency-hiding properties of the GPU. A TLB miss incurs a high latency, as each miss must walk through multiple levels of a page table to find the desired address translation. Third, we observe that a single TLB miss can frequently stall multiple warps at once. Fourth, we observe that contention between applications induces significant thrashing on the shared TLB and significant interference between TLB misses and data requests throughout the GPU memory system. Thus, with only a few simultaneous TLB misses, it becomes difficult for the GPU to find a warp that can be scheduled for execution, defeating the GPU’s basic techniques for hiding the latency of stalls.

Thus, based on our extensive analysis, we conclude that address translation becomes a first-order performance concern in GPUs when multiple applications are executed concurrently. Our goal in this work is to develop new techniques that can alleviate the severe address translation bottleneck existing in state-of-the-art GPUs.

To this end, we propose Multi-Address Space Concurrent Kernels (MASK), a new cooperative resource management framework and TLB design for GPUs that minimizes inter-application interference and translation overheads. MASK takes advantage of locality across shader cores to reduce TLB misses, and relies on three novel techniques to minimize translation overheads. The overarching key idea is to make the entire memory hierarchy TLB request aware. First, TLB-Fill Tokens provide a TLB-selective-fill mechanism to reduce thrashing in the shared L2 TLB, including a bypass cache to increase the TLB hit rate. Second, a low-cost scheme for selectively bypassing TLB-related requests at the L2 cache reduces interference between TLB-miss and data requests. Third, MASK’s memory scheduler prioritizes TLB-related requests to accelerate page table walks.

The techniques employed by MASK are highly effective at alleviating the address translation bottleneck. Through the use of TLB-request-aware policies throughout the memory hierarchy, MASK ensures that the first two levels of the page table walk during a TLB miss are serviced quickly. This reduces the overall latency of a TLB miss significantly. Combined with a significant reduction in TLB misses, MASK allows the GPU to successfully hide the latency of the TLB miss through thread-level parallelism. As a result, MASK improves system throughput by 45.2%, improves IPC throughput by 43.4%, and reduces unfairness by 22.4% over a state-of-the-art GPU memory management unit (MMU) design [68]. MASK provides performance within only 23% of a perfect TLB that always hits.

This paper makes the following contributions:

- To our knowledge, this is the first work to provide a thorough analysis of GPU memory virtualization under multi-address-space concurrency, and to demonstrate the large impact address translation has on latency hiding within a GPU. We demonstrate a need for new techniques to alleviate interference induced by multi-application execution.
- We design an MMU that is optimized for GPUs that are dynamically partitioned spatially across protection domains, rather than GPUs that are time-shared.
- We propose MASK, which consists of three novel techniques that increase TLB request awareness across the entire memory hierarchy. These techniques work together to significantly improve system performance, IPC throughput, and fairness over a state-of-the-art GPU MMU.

2. BACKGROUND

There has been an emerging need to share the GPU hardware among multiple applications. As a result, recent work has enabled support for GPU virtualization, where a single physical GPU can be shared transparently across multiple applications, with each application having its own address space. Much of this work has relied on traditional time and spatial multiplexing techniques that have been employed by CPUs, and state-of-the-art GPUs currently contain elements of both types of techniques [7, 8, 84]. Unfortunately, as we discuss in this section, existing GPU virtualization implementations are too coarse, bake fixed policy into hardware, or leave system software without the fine-grained resource management primitives needed to implement truly transparent device virtualization.

2.1 Time Multiplexing

Most modern systems time-share GPUs [57, 62]. These designs are optimized for the case where no concurrency exists between kernels from different address spaces. This simplifies memory protection and scheduling at the cost of two fundamental tradeoffs. First, it results in underutilization when kernels from a single address space are unable to fully

1In this paper, we use the term address space to refer to distinct memory protection domains, whose access to resources must be isolated and protected during GPU virtualization.

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utilize all of the GPU’s resources [45, 50, 51, 66, 87]. Second, it limits the ability of a scheduler to provide forward-progress or QoS guarantees, leaving applications vulnerable to unfairness and starvation [74].

While preemption support could allow a time-sharing scheduler to avoid pathological unfairness (e.g., by context-switching at a fine granularity), GPU preemption support remains an active research area [33, 79]. Software approaches [87] sacrifice memory protection. NVIDIA’s Kepler [62] and Pascal [65] architectures support preemption at thread block and instruction granularity respectively. We find empirically, that neither is well optimized for inter-application interference.

Figure 1 shows the overhead (i.e., performance loss) per process when the NVIDIA K40 and GTX 1080 GPUs are contended by multiple application processes. Each process runs a kernel that interleaves basic arithmetic operations with loads and stores into shared and global memory, with interference from a GPU matrix-multiply program. The overheads range from 8% per process for the K40, to 10% or 12% for the GTX 1080. While the performance cost is significant, we also found inter-application interference pathologies to be easy to create: for example, a kernel from one process consuming the majority of shared memory can easily cause kernels from other processes to fail at dispatch. While we expect preemption support to improve in future hardware, we seek a solution that does not depend on it.

2.2 Spatial Multiplexing

Resource utilization can be improved with spatial multiplexing [2], as the ability to execute multiple kernels concurrently enables the system to co-schedule kernels that have complementary resource demands, and can enable independent progress guarantees for different kernels. NVIDIA’s stream [62] support, which co-schedules kernels from independent “streams” in a single address space, relies on similar basic concepts, as does application-specific software scheduling of multiple kernels in hardware [45, 66] and GPU simulators [11, 50, 51]. Software approaches (e.g., Elastic Kernels [66]) require programmers to manually time-slice kernels to enable mapping them onto CUDA streams for concurrency. While sharing techniques that leverage the stream abstraction support flexible demand-partitioning of resources, they all share critical drawbacks. When kernels from different applications have complementary resource demands, the GPU remains underutilized. More importantly, merging kernels into a single address space sacriﬁces memory protection, a key requirement in virtualized settings.

Multi-address-space concurrency support can address these shortcomings by enabling a scheduler to look beyond kernels from the current address space when resources are under-utilized. Moreover, QoS and forward-progress guarantees can be enabled by giving partitions of the hardware simultaneously to kernels from different address spaces. For example, long-running kernels from one application need not complete before kernels from another may be dispatched. NVIDIA and AMD both offer products [3, 55] with hardware virtualization support for statically partitioning GPUs across VMs, but even this approach has critical shortcomings. The system must select from a handful of different partitioning schemes, determined at startup, which is fundamentally inflexible. The system cannot adapt to changes in demand or mitigate interference, which are key goals of virtualization layers.

3. BASELINE DESIGN

Our goal in this work is to develop efficient address translation techniques for GPUs that allow for flexible, fine-grained spatial multiplexing of the GPU across multiple address spaces, ensuring protection across memory protection domains. Our primary focus is on optimizing a memory hierarchy design extended with TLBs, which are used in a state-of-the-art GPU [68]. Kernels running concurrently on different compute units share components of the memory hierarchy such as lower level caches, so ameliorating contention for those components is an important concern. In this section, we explore the performance costs and bottlenecks induced by different components in a baseline design for GPU address translation, motivating the need for MASK.

3.1 Memory Protection Support

To ensure that memory accesses from kernels running in different address spaces remain isolated, we make use of TLBs and mechanisms for reducing TLB miss costs within the GPU. We adopt the current state-of-the-art for GPU TLB design for CPU-GPU heterogeneous systems proposed by Power et al. [68], and extend the design to handle multi-address-space concurrency, as shown in Figure 2(a). Each core has a private L1 cache (1), and all cores share a highly-threaded page table walker (2). On a TLB miss, the shared page table walker first probes a page walk cache (3), and if it finds the page, it returns the shared page to the core. If a page walk cache miss occurs, it contacts the shared L2 TLB (4), and if a page walk cache miss occurs, it contacts the L1 TLB (5).

In our evaluation, we provision the page walk cache to be 16-way, with 1024 entries.

Figure 1: Context switch overheads under contention on K40 and GTX 1080.

Figure 2: Baseline TLB designs
3.2 Page Walk Caches

Techniques to avoid misses and hide or reduce their latency are well-studied in the literature. To conserve space, we do not discuss the combinations of techniques that we considered, and focus on the design which we ultimately selected as the baseline for MASK, shown in Figure 2b. The design differs from [68] by eliminating the page walk cache, and instead dedicating the same chip area to 1) a shared L2 TLB with entries extended with address space identifiers (ASIDs) and 2) a parallel page table walker. TLB accesses from multiple threads to the same page are coalesced. On a private L1 TLB miss, the shared L2 TLB is probed (4). On a shared L2 TLB miss, the page table walker begins a walk, probing the shared L2 cache and main memory.

Figure 3 compares the performance with multi-address-space concurrency of our chosen baseline and the design from [68] against the ideal scenario where every TLB access is a hit (see Section 6 for our methodology). While Power et al. find that a page walk cache is more effective than a shared L2 TLB [68], the design with a shared L2 TLB provides better performance for all but three workloads, with 13.8% better performance on average. The shared L2 data cache enables a high rate for page table walks that is competitive with a dedicated page walk cache, and a shared TLB is a more effective use of chip area. Hence, we adopt a design with a shared L2 TLB as the baseline for MASK. We observe that a 128-entry TLB provides only a 10% reduction in miss rate over a 64-entry TLB, suggesting that the additional area needed to double the TLB size is not efficiently utilized. Thus, we opt for a smaller 64-entry L1 TLB in our baseline. Note that a shared L2 TLB outperforms the page walk cache for both L1 TLB sizes. Lastly, we find that both designs incur a significant performance overhead compared to the ideal case where every TLB access is a TLB hit.

Figure 3: Baseline designs vs. ideal performance.

4. DESIGN SPACE ANALYSIS

To inform the design of MASK, we characterize overheads for address translation, and consider performance challenges induced by the introduction of multi-address-space concurrency and contention.

4.1 Address Translation Overheads

GPU throughput relies on fine-grained multithreading [76][80] to hide memory latency. However, we observe a fundamental tension between address translation and fine-grained multithreading. The need to cache address translations at a page granularity, combined with application-level spatial locality, increases the likelihood that translations fetched in response to a TLB miss will be needed by more than one thread. Even with the massive levels of parallelism supported by GPUs, we observe that a small number of outstanding TLB misses can result in the thread scheduler not having enough ready threads to schedule, which in turn limits the GPU’s most essential latency-hiding mechanism.

Figure 4 illustrates a scenario where all warps of an application access memory. Each box represents a memory instruction, labeled with the issuing warp. Figure 4a shows how the GPU behaves when no virtual-to-physical address translation is required. When Warp A executes a high-latency memory access, the core does not stall as long as other warps have schedulable instructions: in this case, the GPU core selects from among the remaining warps (Warp B–H) during the next cycle (1), and continues issuing instructions until all requests to DRAM have been sent. Figure 4b considers the same scenario when address translation is required. Warp A misses in the TLB (indicated in red), and stalls until the translation is fetched from memory. If threads belonging to Warps B–D access data from the same page as the one requested by Warp A, these warps stall as well (shown in light red) and perform no useful work (2). If a TLB miss from Warp E similarly stalls Warps E–G (3), only Warp H executes an actual data access (4). Two phenomena harm performance in this scenario. First, warps stalled on TLB misses reduce the availability of schedulable warps, lowering utilization. Second, TLB miss requests must complete before actual the data requests can issue, which reduces the ability of the GPU to hide latency by keeping multiple memory requests in flight.

![Diagram showing the impact of TLB misses on GPU performance.](image-url)

Figure 5 shows the number of stalled warps per active TLB miss, and the average number of maximum concurrent page table walks (sampled every 10K cycles for a range of applications). In the worst case, a single TLB miss stalls over 30 warps, and over 50 outstanding TLB misses contend for access to address translation structures. The large number of concurrent misses stall a large number of warps, which must wait before issuing DRAM requests, so minimizing TLB misses and page table walk latency is critical.

**Impact of Large Pages.** Larger page size can significantly improve the coverage of the TLB. However, previous work has observed that the use of large pages significantly in-
increases the overhead of demand paging in GPUs. We evaluate this overhead with 2MB page size and find that it results in an average slowdown of 93%.

4.2 Interference Induced by Sharing

To understand the impact of inter-address-space interference through the memory hierarchy, we concurrently run two applications using the methodology described in Section 4.4. Figure 6 shows the TLB miss breakdown across all workloads: most applications incur significant L1 and L2 TLB misses. Figure 7 compares the TLB miss rate for applications running in isolation to the miss rates under contention. The data show that inter-address-space interference through additional thrashing has a first-order performance impact.

Figure 7: Cross-address-space interference in real applications. Each set of bars corresponds to a pair of co-scheduled applications, e.g. “3DS_HISTO” denotes the 3DS and HISTO benchmarks running concurrently.

Figure 8 illustrates TLB misses in a scenario where two applications (green and blue) share the GPU. In Figure 8a, the green application issues five parallel TLB requests, causing the premature eviction of translations for the blue application, increasing its TLB miss rate (Figure 8b). The use of a shared L2 TLB to cache entries for each application’s (non-overlapping) page tables dramatically reduces TLB reach. The resulting inter-core TLB thrashing hurts performance, and can lead to unfairness and starvation when applications generate TLB misses at different rates. Our findings of severe performance penalties for increased TLB misses corroborate previous work on GPU memory designs. However, interference across address spaces can inflate miss rates in ways not addressed by these works, and which are best managed with mechanisms that are aware of concurrency (as we show in Section 7.1).

4.3 Interference from Address Translation

Interference at the Shared Data Cache. Prior work demonstrated that while cache hits in GPUs reduce the consumption of off-chip memory bandwidth, cache hits result in a lower load/store instruction latency only when every thread in the warp hits in the cache. In contrast, when a page table walk hits in the shared L2 cache, the cache hit has the potential to help reduce the latency of other warps that have threads which access the same page in memory. While this makes it desirable to allow the data generated by the page table walk to consume entries in the shared cache, TLB-related data can still interfere with and thrash normal data cache entries, which hurts the overall performance.

Hence, a trade-off exists between prioritizing TLB related requests or normal data requests in the GPU memory hierarchy. Figure 7 shows that entries for translation data from levels closer to the page table root are more likely to be shared across warps, and will typically be served by cache hits. Allowing shared structures to cache page walk data from only the levels closer to the root could alleviate the interference between low-hit-rate translation data and application data.

Interference at Main Memory. Figure 10 characterizes the DRAM bandwidth utilization, broken down between data and address translation requests for applications sharing the GPU concurrently pairwise. Figure 11 compares the average latency for data requests and translation requests. We see that even though page walk requests consume only 13.8% of the utilized DRAM bandwidth (2.4% of the maximum bandwidth), their DRAM latency is higher than that of data requests, which is particularly egregious since data requests that lead to TLB misses stall while waiting for page walks to complete. The phenomenon is caused by FR-FCFS memory schedulers, which prioritize accesses that hit in the row buffer. Data requests from GPGPU applications generally have very high row buffer locality, so a scheduler that cannot distinguish page walk requests effectively de-prioritizes them, increasing their latency.

In summary, we make two important observations about address translation in GPUs. First, address translation competes with the GPU’s ability to hide latency through thread-level parallelism, when multiple warps stall on the TLB misses for a single translation. Second, the GPU’s memory-level parallelism generates interference across address spaces, and between TLB requests and data requests, which can lead to unfairness and increased latency. In light...
of these observations, the goal of this work is to design mechanisms that alleviate the translation overhead by 1) increasing the TLB hit rate through reduced TLB thrashing, 2) decreasing interference between normal data and TLB requests in the shared L2 cache, 3) decreasing TLB miss latency by prioritizing TLB-related requests in DRAM, and 4) enhancing memory scheduling to provide fairness without sacrificing DRAM bandwidth utilization.

5. DESIGN OF MASK

We now introduce Multi-Address Space Concurrent Kernels (MASK), a new cooperative resource management framework and TLB design for GPUs. Figure 12 provides a design overview of MASK. MASK employs three components in the memory hierarchy to reduce address translation overheads while requiring minimal hardware change. First, we introduce TLB-Fill Tokens to lower the number of TLB misses and utilize a bypass cache to cache frequently used TLB entries (1). Second, we design a TLB-Request-Aware L2 Bypass mechanism for TLB requests that significantly increases the shared L2 cache utilization, by reducing interference from TLB misses at the shared L2 data cache (2). Third, we design an Address-Space-Aware DRAM Scheduler to further reduce interference between TLB requests and data requests from different applications (3). We analyze the hardware cost of MASK in Section 7.5.

5.1 Memory Protection

MASK uses per-core page table root registers (similar to x86 CR3) to set the current address space on each core: setting it also sets the value in a page table root cache with per-core entries at the L2 layer. The page table root cache is kept coherent with the CR3 value in the core by draining all in-flight memory requests for that core when the page table root is set. L2 TLB cache lines are extended with address-space identifiers (ASIDs); TLB flush operations target a single shader core, flushing the core’s L1 TLB and all entries in the L2 TLB with a matching ASID.

5.2 Reducing L2 TLB Interference

Sections 4.1 and 4.2 demonstrated the need to minimize TLB miss overheads. MASK addresses this need with a new mechanism called TLB-Fill Tokens. Figure 13a shows architectural additions to support TLB-Fill Tokens. We add two 16-bit counters to track TLB hits and misses per shader core, along with a small fully-associative bypass cache to the shared TLB. Figure 14 illustrates operation of the proposed TLB fill bypassing logic. When a TLB access arrives (Figure 14a), tags for both the shared TLB (1) and bypass cache (2) are probed in parallel. A hit on either the TLB or the bypass cache yields a TLB hit.

To reduce inter-core thrashing at the shared L2 TLB, we use an epoch- and token-based scheme to limit the number of warps from each shader core that can fill into (and therefore contend for) the L2 TLB. While every warp can probe the shared TLB, to prevent thrashing, we allow only warps with tokens to fill into the shared TLB as shown in Figure 14b. This token-based mechanism requires two components, one to determine the number of tokens for each application, and one to implement policy for assigning tokens to warps.

Determining the Number of Tokens. At the beginning of a kernel, MASK performs no bypassing, but tracks the L2 miss rate for each application and the total number of warps in each core. After the first epoch, the initial number of tokens (InitialToken) is set to a fraction of the total number of warps per application. At the end of any subsequent epoch, MASK compares the shared L2 TLB miss rates of the current and previous epoch. If the miss rate decreases or increases from the previous epoch, MASK uses the logic shown in Figure 13b to decrease or increase the number of tokens allocated to each application.

Assigning Tokens to Warps. Empirically, we observe that 1) warps throughout the GPU cores have mostly even TLB miss rate distribution; and 2) it is more beneficial for warps that previously have tokens to retain their token, as it is more likely that their TLB entries are already in the shared TLB. We leverage these two observations to simplify the token assignment logic: TLB-Fill Tokens simply hands out tokens in round-robin fashion to all cores in warpID order. The heuristic is effective at reducing thrashing, as contention at the shared TLB is reduced based on the number of tokens, and highly-used TLB entries that do not have tokens can still fill into the bypassed cache.

Bypass Cache. While TLB-Fill Tokens can reduce thrashing in the shared TLB, a handful of highly-reused pages from warps with no tokens may be unable to utilize the shared TLB. To address this, we add a bypass cache, which is a

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3We empirically select an epoch length of 100K cycles.
small 32-entry fully associative cache. Only warps without tokens can fill the bypass cache.

**Replacement Policy.** While it is possible to base the cache replacement policy on how many warps are stalled per TLB entry and prioritize TLB entries with more warps sharing an entry, we observe small variance across TLB entries on the shared TLB in practice. Consequently, a replacement policy based on number of warps stalled per TLB entry actually performs worse than a reuse-based policy. Hence, we use LRU replacement policy for L1 TLBs, the shared L2 TLB and the bypass cache.

### 5.3 Minimizing Shared L2 Interference

**Interference from TLB Requests.** While Power et al. propose to coalesce TLB requests to minimize the cache pressure and performance impact [68], we find that a TLB miss generates shared cache accesses with varying degrees of locality. Translating addresses through a multi-level page table (4 levels for MASK) can generate dependent memory requests for each level. This causes significant queuing latency at the shared L2 cache, corroborating observations from previous work [12]. Page table entries in levels closer to the root are more likely to be shared across threads than entries near the leaves, and more often hit in the shared L2 cache.

To address both the interference and queuing delay at the shared L2 cache we introduce **TLB-Request-Aware L2 Bypass** for TLB requests, as shown in Figure 15. To determine which TLB requests should be bypassed, we leverage our insights from Section 4.3. Because of the sharp drop-off in L2 cache hit rate after the first few levels, we can simplify the bypassing logic to compare the L2 cache hit rate of each page level for TLB requests to the L2 cache hit rate for non-TLB requests. We impose L2 cache bypassing when the hit rate for TLB requests falls below the hit rate for non-TLB requests. Memory requests are tagged with three additional bits specifying page walk depth, allowing MASK to differentiate between request types. These bits are set to zero for normal data requests, and to 7 for any depth higher than 6.

### 5.4 Minimizing Interference at Main Memory

Section 4.3 demonstrates two different types of interference at main memory. Normal data requests can interfere with TLB requests, and data requests from multiple applications can interfere with each other. **MASK**’s memory controller design mitigates both forms of interference using an **Address-Space-Aware DRAM Scheduler**.

**MASK**’s **Address-Space-Aware DRAM Scheduler** breaks the traditional DRAM request buffer into three separate queues, as shown in Figure 12. The first queue, called the **Golden Queue**, contains a small FIFO queue. For each application, the last queue, called the **Silver Queue**, contains data request from **one selected application**. The third queue, called the **Normal Queue**, contains data requests from all other applications.

**The Golden Queue** is used to prioritize cache misses over normal data requests, and to 7 for any depth higher than 6.

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1. Note that all experiments done in this paper use a depth of 4.
2. We observe that TLB-related requests have low row locality. Thus, we use a FIFO queue to further simplify the design.
Silver Queue, which are prioritized over requests in the Normal Queue. Applications take turns being assigned to the Silver Queue based on two factors: the number of concurrent page walks, and the number of warps stalled per active TLB miss. The number of requests each application can add to the Silver Queue is shown in Equation 1. Application \( App_i \) inserts \( thres_i \) requests into the Silver Queue. Then, the next application \( App_{i+1} \) is allowed to send \( thres_{i+1} \) requests to the Silver Queue. Within each queue, FR-FCFS \([71, 95]\) is used to schedule requests.

\[
\text{thres}_i = \text{thres}_{\text{max}} \frac{\text{Concurrent}_i \times \text{WrpStalled}_i}{\sum_{j=1}^{\text{numApp}} \text{Concurrent}_j \times \text{WrpStalled}_j}
\]  

(1)

To track the number of outstanding concurrent page walks, we add a 6-bit counter per application to the shared TLB. This counter tracks of the maximum number of TLB miss queue, and is used as \( \text{Concurrent}_i \) in Equation 1. To track the number of warps stalled per active TLB, we add a 6-bit counter to the TLB MSHRs, to track the maximum number of warps that hit in each MSHR entry. This number is used for \( \text{WrpStalled}_i \). Note that the Address-Space-Aware DRAM Scheduler resets all of these counters every epoch.

We find that the number of concurrent TLB requests that go to each memory channel is small, so our design has an additional benefit of lowering page table walk latency while minimizing interference. The Silver Queue prevents bandwidth-heavy applications from interfering with applications utilizing the queue, which in turn prevents starvation. It also minimizes the reduction in total bandwidth utilization, as the per-queue FR-FCFS scheduling policy ensures that application-level row buffer locality is preserved.

5.5 Page Faults and TLB Shootdowns

Address translation inevitably introduces page faults. Our design can be extended to use techniques from previous works, such as performing copy-on-write for minor faults \([68]\), and either exception support \([68]\) or demand paging techniques \([6, 65, 94]\) for major faults. We leave this as future work, and do not evaluate these overheads.

Similarly, TLB shootdowns are required when shader cores change address spaces and when page tables are updated. We do not envision applications that make frequent changes to memory mappings, so we expect such events to be rare. Techniques to reduce TLB shootdown overhead \([18, 73]\) are well-explored and can be applied to MASK.

6. METHODOLOGY

We model Maxwell architecture \([63]\) cores, TLB fill bypassing, bypass cache, and memory scheduling mechanisms in MASK using the MAFIA framework \([45]\), which is based on GPGPU-Sim 3.2.2 \([13]\). We heavily modify the simulator to accurately model the behavior of CUDA Unified Virtual Address \([63, 65]\) as described below. Table 1 provides details on our baseline GPU configuration. In order to show changes to memory mappings, so we expect such events to be rare. Techniques to reduce TLB shootdown overhead \([18, 73]\) are well-explored and can be applied to MASK.

**Table 1: Configuration of the simulated system.**

| System Overview | 30 cores, 64 execution unit per core, 8 memory partitions |
|-----------------|---------------------------------------------------------|
| Shader Core Config | 1020 MHz, 9-stage pipeline, 64 threads per warp, GTO scheduler \([72]\) |
| Private L1 Cache | 16KB, 4-way associative, LRU, L1 misses are coalesced before accessing L2, 1 cycle latency |
| Shared L2 Cache | 2MB total, 16-way associative, LRU, 2 cache banks 2 interconnect ports per memory partition, 10 cycle latency |
| Private L1 TLB | 64 entries per core, fully associative, LRU, 1 cycle latency |
| Shared L2 TLB | 512 entries total, 16-way associative, LRU, 2 ports per memory partition (16 ports total), 10 cycle latency |
| DRAM | GDDR5 1674 MHz, 8 channels, 8 banks per rank FR-FCFS scheduler \([71, 95]\) burst length 8 |
| Page Table Walker | 64 threads shared page table walker, traversing 4-level page table |

**TLB and Page Table Walk Model.** We modify the MAFIA framework to accurately model the TLB designs from \([68]\) and the MASK baseline design. We employ the non-blocking TLB implementation used in the design from Pichai et al. \([67]\). Each core has a private L1 TLB. The page table walker is shared, and admits up to 64 concurrent threads for walks. The baseline design for MASK adds a shared L2 TLB instead of page walk caches (see Section 5.2), with a shared L2 TLB in each memory partition. Both L1 and L2 TLB entries contain MSHR entries to track in-flight page table walks. On a TLB miss, a page table walker generates a series of dependent requests that probe the L2 data cache and main memory as needed. To correctly model virtual-to-physical address mapping and dependent memory accesses for multi-level page walks, we collect traces of all virtual addresses referenced by each application (executing them to completion), enabling us to pre-populate disjoint physical address spaces for each application with valid page tables.

**Workloads.** We randomly select 27 applications from the CUDA SDK \([60]\), Rodinia \([22]\), Parboil \([77]\), LULESH \([47, 48]\), and SHOC \([27]\) suites. We classify these benchmarks based on their L1 and L2 TLB miss rates into one of four groups. Table 2 shows the categorization for each benchmark. For our multi-application results, we randomly select 35 pairs of applications, avoiding combinations that select applications from the lowL1miss-lowL2miss category, as these applications are relatively insensitive to memory protection overheads. The application that finishes first is relaunched to keep the SM full and to properly model contention.

We divide these pairs into three workload categories based on the number of applications that are from highL1miss-highL2miss category. 0 HMR contains workload bundles where none of the applications in the bundle are from highL1miss-highL2miss. 1 HMR contains workloads where only one application in the bundle is from highL1miss-highL2miss. 2 HMR contains workloads where both applications in the bundle are from highL1miss-highL2miss.

**Evaluation Metrics.** We report performance using weighted speedup \([30, 31]\), defined as \( \sum_{i} \frac{\text{IPC}_{\text{Shared}}}{\text{IPC}_{\text{alone}}} \). IPCalone is the IPC of an application that runs on the same number of shader cores, but does not share GPU resources with any other applications, and IPCshared is the IPC of an application when running concurrently with other applications. We...
report the unfairness of each design using maximum slowdown, defined as $\frac{\text{IPC}_{\text{Alt}}}{\text{IPC}_{\text{Shared}}}$.

Scheduling and Partitioning of Cores. The design space for core scheduling is quite large, and finding optimal algorithms is beyond the scope of this paper. To ensure that we model a scheduler that performs reasonably well, we assume an oracle schedule that finds the best partition for each pair of applications. For each pair of applications, concurrent execution partitions the cores according to the best weighted speedup observed for that pair during an exhaustive search over all possible partitions.

Design Parameters. MASK exposes two configurable parameters: InitialTokens for TLB-Fill Tokens and $\text{thres}_{\text{max}}$ for the Address-Space-Aware DRAM Scheduler. A sweep over the range of possible InitialTokens values reveals less than 1% performance variance, as TLB-Fill Tokens is effective at reconfiguring the total number of tokens to a steady-state value (shown in Figure 14). In our evaluation, we set InitialTokens to 80%. We set $\text{thres}_{\text{max}}$ to 500 empirically.

7. EVALUATION

We compare the performance of MASK against three designs. The first, called Static, uses a static spatial partitioning of resources, where an oracle is used to partition GPU cores, but the shared L2 cache and memory channels are partitioned equally to each application. This design is intended to capture key design aspects of NVIDIA GRID and AMD FirePro—however, insufficient information is publicly available to enable us to build a higher fidelity model. The second design, called GPU-MMU, models the flexible spatial partitioning GPU MMU design proposed by Power et al. The third design we compare to is an ideal scenario, where every single TLB access is a TLB hit. We also report performance impact for individual components of MASK: TLB-Fill Tokens (MASK-TLB), TLB-Request-Aware L2 Bypass (MASK-Cache), and Address-Space-Aware DRAM Scheduler (MASK-DRAM).

7.1 Multiprogrammed Performance

Figures 17 and 16 compare the weighted speedup of multiprogrammed workloads for MASK, as well as each of the components of MASK, against Static and GPU-MMU. Each group of bars in the figure represents a pair of co-scheduled benchmarks. Compared to GPU-MMU, MASK provides 45.2% additional speedup. We also found that MASK performs only 23% worse than the ideal scenario where the TLB always hits. We observe that MASK provides 43.4% better aggregate throughput (system wide IPC) compared to GPU-MMU. Compared to the Static baseline, where resources are statically partitioned, both GPU-MMU and MASK provide better performance, because when an application stalls for concurrent TLB misses, it does not use other shared resources such as DRAM bandwidth. During such stalls, other applications can utilize these resources. When multiple GPGPU applications run concurrently, TLB misses from two or more applications can be staggered, increasing the likelihood that there will be heterogeneous and complementary resource demand.

Figures 18 compares unfairness in MASK against the GPU-MMU and Static baselines. On average, our mechanism reduces unfairness by 22.4% compared to GPU-MMU. As the number of tokens for each application changes based on the TLB miss rate, applications that benefit more from the shared TLB are more likely to get more tokens, causing applications that do not benefit from shared TLB space to yield that shared TLB space to other applications. Our application-aware token distribution mechanism and TLB fill bypassing mechanism can work in tandem to reduce the amount of inter-application cache thrashing observed in Section 4.2. Compared to statically partitioning resources in Static, allowing both applications access to all of the shared
resources provides better fairness. On average, MASK reduces unfairness by 30.7%, and a handful of applications benefit by as much as 80.3%.

**Individual Application Analysis.** MASK provides better throughput on all applications sharing the GPU due to reduced TLB miss rates for each application. The per-application L2 TLB miss rates are reduced by over 50% on average, which is in line with the system-wide miss rates observed in Figure 18. Reducing the number of TLB misses through the TLB fill bypassing policy (Section 5.2) and the TLB- and application-aware DRAM scheduling policy (Section 5.4) enables significant performance improvement.

In some cases, running two applications concurrently provides better speedup than running the application alone (e.g., RED-BP, RED-RAY, SC-FWT). We attribute these cases to substantial improvements (more than 10%) of two factors: a lower L2 queuing latency for bypassed TLB requests, and a higher L1 hit rate when applications share the L2 and main memory with other applications.

**7.2 Component-by-Component Analysis**

**Effectiveness of TLB-Fill Tokens.** Table 3 compares the TLB hit rates of GPU-MMU and MASK-TLB. We show only GPU-MMU results for TLB hit rate experiments, as the TLB hit behavior for Static and GPU-MMU are similar. MASK-TLB increases TLB hit rates by 49.9% on average, which we attribute to TLB-Fill Tokens. First, TLB-Fill Tokens reduces the number of warps utilizing the shared TLB entries, which in turn reduces the miss rate. Second, the bypass cache can store frequently-used TLB entries that cannot be filled in the traditional TLB. Table 4 confirms this, showing the hit rate of the bypass cache for MASK-TLB. From Table 3 and Table 4, we conclude that the TLB-fill bypassing component of MASK successfully reduces thrashing and ensures that frequently-used TLB entries stay cached.

| Shared TLB Hit Rate | 0 HMR | 1 HMR | 2 HMR | Average |
|---------------------|-------|-------|-------|---------|
| GPU-MMU             | 47.8% | 45.6% | 55.8% | 49.3%   |
| MASK-TLB            | 68.1% | 75.2% | 76.1% | 73.9%   |

Table 3: Aggregate Shared TLB hit rates.

| Bypass Cache Hit Rate | 0 HMR | 1 HMR | 2 HMR | Average |
|-----------------------|-------|-------|-------|---------|
| MASK-TLB              | 63.9% | 66.6% | 68.8% | 66.7%   |

Table 4: TLB hit rate for bypassed cache.

**Effectiveness of TLB-Request-Aware L2 Bypass.** Table 5 shows the average L2 data cache hit rate for TLB requests. For requests that fill into the shared L2 data cache, TLB-Request-Aware L2 Bypass is effective in selecting which blocks to cache, resulting in a TLB request hit rate that is higher than 99% for all of our workloads. At the same time, TLB-Request-Aware L2 Bypass minimizes the impact of bypassed TLB requests, leading to 17.6% better performance on average compared to GPU-MMU, as shown in Figure 19.

| L2 Data Cache Hit Rate | 0 HMR | 1 HMR | 2 HMR | Average |
|------------------------|-------|-------|-------|---------|
| GPU-MMU                | 71.7% | 71.6% | 68.7% | 70.7%   |
| MASK-Cache             | 97.9% | 98.1% | 98.8% | 98.3%   |

Table 5: L2 data cache hit rate for TLB requests.

**Effectiveness of Address-Space-Aware DRAM Scheduler.** While the impact of the DRAM scheduler we propose is minimal for many applications, (the average improvement across all workloads is just 0.83% in Figure 17), we observe that a few applications that suffered more severely from interference (see Figures 10 and 11) can significantly benefit from our scheduler, since it prioritizes TLB-related requests. Figures 19a and 19b compare the DRAM bandwidth utilization and DRAM latency of GPU-MMU and MASK-DRAM for workloads that benefit from Address-Space-Aware DRAM Scheduler. When our DRAM scheduler policy is employed, SRAD from the SCAN-SRAD pair sees a 18.7% performance improvement, while both SCAN and CONS from SCAN-CONS have performance gains of 8.9% and 30.2%, respectively. In cases where the DRAM latency is high, the DRAM scheduler policy reduces the latency of TLB requests by up to 10.6% (SCAN-SAD), while increasing DRAM bandwidth utilization by up to 5.6% (SCAN-HISTO).

**7.3 Scalability and Performance on Other Architectures**

Figure 20a shows the performance of GPU-MMU and MASK, normalized to the ideal performance with no translation overhead, as we vary the number of applications executing concurrently on the GPU. We observe that as the application count increases, the performance of both GPU-MMU and MASK are further from the ideal baseline, due to contention for shared resources (e.g., shared TLB, shared data cache). However, MASK provides increasingly better performance compared to GPU-MMU (35.5% for one application, 45.2% for two concurrent applications, and 47.3% for three concurrent applications). We conclude that MASK provides better scalability with application count over the state-of-the-art designs.
The analyses and designs of MASK are architecture independent and should be applicable to any SIMD machine. To demonstrate this, we evaluate MASK on the GTX 480, which uses the Fermi architecture [61]. Figure 20(b) shows the performance of GPU-MMU and MASK, normalized to the ideal performance with no translation overhead, for the GTX 480 and the GTX 750 Ti. We make three observations. First, address translation incurs significant performance overhead in both architectures for the baseline GPU-MMU design. Second, MASK provides a 29.1% performance improvement over the GPU-MMU design in the Fermi architecture. Third, compared to the ideal performance, MASK performs only 22% worse in the Fermi architecture. On top of the data shown in Figure 20(b), we find that MASK reduces unfairness by 26.4% and increases the TLB hit rates by 64.7% on average than in the Fermi architecture. We conclude that MASK delivers significant benefits regardless of GPU architecture. Aside from this, Table 6 provides an evaluation of MASK on the integrated GPU configuration used in previous work [68]. This integrated GPU has fewer number of GPU cores, slower L2 cache, slower and less bandwidth main memory.

Table 6: Relative performance vs. the ideal baseline.

| Relative Performance       | Maxwell | Integrated GPU [68] |
|----------------------------|---------|---------------------|
| Shared TLB                 | 32.4%   | 38.2%               |
| MASK + Shared TLB          | 78.3%   | 64.5%               |
| Translation Cache          | 46.0%   | 52.1%               |
| MASK + Translation Cache   | 72.5%   | 72.5%               |

From Table 6 we found that 1) MASK is effective in reducing the latency of address translation and able to improve the performance of both the shared L2 TLB and translation cache designs on both off-chip Maxwell GPU and integrated GPU configurations, 2) contention at the shared L2 TLB becomes significantly more severe and causes a significant performance drop in the integrated GPU setup.

7.4 Sensitivity Studies

Sensitivity to L1 and L2 TLB Sizes. We evaluated the performance of MASK for a range of L1 and L2 TLB sizes. We find that for both the L1 and L2 TLB, MASK performs closer to the baseline as the number of TLB entries increases, as the contention at the L1 and L2 TLB decreases.

Sensitivity to Memory Policies. We study the sensitivity of MASK to (1) main memory row policy, and (2) memory scheduling policies. We find that for both the GPU-MMU baseline and MASK, the workload performance for an open-row policy is similar (within 0.8%) when we instead employ a closed row policy, which is used in various CPU processors [36, 37, 40]. Aside from the FR-FCFS scheduler [71, 95], we applied MASK on other state-of-the-art GPU memory scheduler [45] and found that MASK with this scheduler performs 44.2% over the GPU-MMU baseline. We conclude that MASK is effective across different memory policies.

Sensitivity to Different Page Size. We evaluate the performance of MASK with large page assuming ideal page fault latency. We found that applying MASK allows the GPU to perform within 1.8% of the ideal baseline.

7.5 Hardware Overheads

To support memory protection, each L2 TLB cache line adds an address space identifier (ASID). We model 8-bit ASIDs added to L2 TLB entries, which translates to 7% of the L2 TLB size.

TLB-Fill Tokens, uses two 16-bit counters at each shader core. We augment the shared cache with 32-entry fully-associative content addressable memory (CAM) for the bypass cache, and 30 15-bit token counts with 30 1-bit token direction entries to distribute tokens over up to 30 concurrent applications. In total, we add 436 bytes (4 bytes per core on the L1 TLB, and 316 bytes in the shared L2 TLB), which represents 0.5% growth of the L1 TLB and 3.8% of the L2 TLB.

TLB-Request-Aware L2 Bypass uses ten 8-byte counters per core to track cache hits and cache accesses per level, (including for the data cache). The resulting 80 bytes are less than 0.1% of the shared L2 cache. Each cache and memory request requires an additional 3 bits specifying the page walk level, as discussed in Section 5.3.

Address-Space-Aware DRAM Scheduler adds a 16-entry FIFO queue in each memory channel for TLB-related requests, and a 64-entry memory request buffer per memory channel for the Silver Queue, while reducing the size of the Normal Queue by 64 entries down to 192 entries. This adds an extra 6% of storage overhead to the DRAM request queue per memory controller.

Area and Power Consumption. We compare the area and power consumption of MASK using CACTI [59]. We compare the area and power of the L1 TLB, L2 TLB, the shared data cache and the page walk cache. We find that MASK introduces a negligible overhead, consuming less than 0.1% additional area and 0.01% additional power than both shared L2 TLB and page walk cache baselines.

8. RELATED WORK

8.1 Partitioning for GPU Concurrency

Concurrent Kernels and GPU Multiprogramming. The opportunity to improve utilization with concurrency is well-recognized, but previous proposals [56, 66, 87, 92] do not support memory protection. Adriaens et al. [2] observe the need for spatial sharing across protection domains, but do not propose or evaluate a design. NVIDIA GRID [35] and AMD Firepro [3] support static partitioning of hardware to allow kernels from different VMs to run concurrently, but the partitions are determined at startup, which causes fragmentation and under-utilization (see Section 7.1). MASK’s
goal is flexible, dynamic partitioning.

NVIDIA’s Multi Process Service (MPS) [64] allows multiple processes to launch kernels on the GPU, but the service provides no memory protection or error containment. Xu et al. [91] propose Warped-Slicer, which is a mechanism for multiple applications to spatially share a GPU core. Similar to MPS, Warped-Slicer provides no memory protection, and is not suitable for supporting multi-application in a multi-tenant cloud setting.

Preemptive Context Switching. Preemptive context switch is an active research area [83][79][87], and architectural support [57][65] will likely improve in future GPUs. Preemption is complementary to spatial multiplexing, and we leave techniques to combine them for future work.

GPU Virtualization. Most current hypervisor-based full virtualization techniques for GPGPUs [49][8][81] must support a virtual device abstraction without the dedicated hardware support for the Virtual Desktop Infrastructure (VDI) found in GRID [35] and FirePro [3]. Key components missing from these proposals include support for the dynamic partitioning of hardware resources, and efficient techniques for handling over-subscription. Performance overheads incurred by these designs argue strongly for hardware assistance, as we propose. By contrast, API-remoting solutions such as vmCUDA [86] and rCUDA [28] provide near-native performance, but require modifications to the guest software and sacrifice both isolation and compatibility.

Demand Paging in GPUs. Demand paging is an important primitive for memory virtualization that is challenging for GPUs [84]. Recent works on CC-NUMA [8], AMD’s hUMA [5], and NVIDIA’s PASCAL architecture [65][94] support for demand paging in GPUs. These techniques can be used in conjunction with MASK.

8.2 TLB Design

GPU TLB Designs. Previous works have explored TLB designs in heterogeneous systems with GPUs [25][67][68][84], and the adaptation of x86-like TLBs in a heterogeneous CPU-GPU setting [68]. Key elements in these designs include probing the TLB after L1 coalescing to reduce the amount of parallel TLB requests, shared concurrent page table walks, and translation caches to reduce main memory accesses. MASK owes much to these designs, but we show empirically that contention patterns at the shared L2 layer require additional support beyond these designs to accommodate contention from multiple address spaces. Cong et al. propose a TLB design similar to our baseline GPU-MMU design [25]. However, this design utilizes the host (CPU) MMU to perform page walks, which is inapplicable in the context of multi-application GPUs. Pichai et al. [67] explore a TLB design for heterogeneous CPU-GPU systems, and add TLB awareness to the existing CCWS GPU warp scheduler [72]. Warp scheduling is orthogonal to our work, and can be combined to further improve performance.

Vesely et al. analyze support for virtual memory in heterogeneous systems [54], finding that the cost of address translation in GPUs is an order of magnitude higher than in CPUs, and that high latency address translations limit the GPU’s latency hiding capability and hurts performance (an observation in line with our own findings in Section 4.1). We show additionally that thrashing due to interference further slows down applications sharing the GPU. MASK is capable not only of reducing interference between multiple applications (Section 7.1), but of reducing the TLB miss rate in single-application scenarios as well.

Instead of relying on hardware modifications, Lee et al. propose VAST, a software-managed virtual memory space for GPUs [53]. Data-parallel applications typically have a larger working set size compared to the size of GPU memory, preventing these applications from utilizing the GPUs. To address this, VAST creates the illusion of a large virtual memory (without concerns about the physical memory size), by providing an automatic memory management system that partitions GPU programs into chunks that fit the physical memory space. Even though recent GPUs now support demand paging [65], the observation regarding the large working set size of GPGPU programs motivates the need for better virtual memory support, which is what MASK provides.

TLB Designs in CPU Systems. Cox and Bhattacharjee propose an efficient TLB design that allows entries corresponding to multiple page sizes to share the same TLB structure, simplifying the design of TLBs [26]. While this design can be applied to GPUs, it is solving a different problem: area and energy efficiency. Thus, this proposal is orthogonal to MASK. Bhattacharjee et al. examine shared last-level TLB designs [17] and page walk cache designs [16], proposing a mechanism that can accelerate multithreaded applications by sharing translations between cores. However, these proposals are likely to be less effective for multiple concurrent GPGPU applications, because translations are not shared between virtual address spaces. Barr et al. propose SpecTLB [14], which speculatively predicts address translations to avoid the TLB miss latency. Speculatively predicting address translation can be complicated and costly in GPUs, because there can be multiple concurrent TLB misses to many different TLB entries in the GPU.

Direct segments [15] and redundant memory mappings [46] reduce address translation overheads by mapping large contiguous virtual memory regions to a contiguous physical region. These techniques increase the reach of each TLB entry, and are complementary to those in MASK.

8.3 Techniques to Reduce Interference

GPU-Specific Resource Management. Jog et al. propose MAFIA, a main memory management scheme that improves performance of concurrently-running GPGPU applications [45]. The design of MAFIA assumes that parallel applications operate under the same virtual address space, and does not model address translation overheads or accommodate safe, concurrent execution of kernels from different protection domains. In contrast, we model and study the impact of address translation and memory protection. Lee et al. propose TAP [52], a TLP-aware cache management mechanism that modifies the CPU cache partitioning policy [70] and cache insertion policy [42] to lower GPGPU applications’ interference to CPU applications at the shared cache. However, TAP does not consider address translation and interference between different GPGPU applications.

Several memory scheduler designs target systems with
GPUs. Unlike MASK, these designs focus on a single GPGPU application, and are not aware of page walk traffic. They focus on reducing the complexity of the memory scheduler for a single application by reducing inter-warp interference, or by providing resource management for heterogeneous CPU-GPU applications. While some of these works propose mechanisms that reduce interference, they differ from MASK because 1) they consider interference from applications with wildly different characteristics (CPU applications vs. GPU applications), and 2) they do not consider interference between page-walk-related and normal memory traffic.

**Cache Bypassing Policies in GPUs.** Techniques to reduce contention on shared GPU caches employ memory-divergence-based bypassing, reuse-based cache bypassing, and software-based cache bypassing, and sometimes combine these works with throttling to reduce contention. These works do not differentiate page walk traffic from normal traffic, and focus on a single application.

**Cache and TLB Insertion Policies.** Cache insertion policies that account for cache thrashing or future reuse work well for CPU applications, but other previous works have shown these policies to be ineffective for GPU applications. This observation holds for the shared TLB in the multi-address space scenario.

### 9. CONCLUSION

Efficiently deploying GPUs in a large-scale computing environment needs spatial multiplexing support. However, the existing address translation support stresses a GPU’s fundamental latency reducing techniques, and interference from multiple address spaces can further harm performance. To alleviate these problems, we propose MASK, a new memory hierarchy designed for multi-address-space concurrency. MASK consists of three major components that lower inter-application interference during address translation and improve L2 cache utilization for translation requests. MASK successfully alleviates the address translation overhead, improving performance by 45.2% over the state-of-the-art.

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