Simultaneous execution of quantum circuits on current and near-future NISQ systems

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ABSTRACT In the NISQ era, multi-programming of quantum circuits (QC) helps to improve the throughput of quantum computation. Although the crosstalk, which is a major source of noise on NISQ processors, may cause performance degradation of concurrent execution of multiple QCs, its characterization cost grows quadratically in processor size. To address these challenges, we introduce palloq (parallel allocation of QCs) for improving the performance of quantum multi-programming on NISQ processors while paying attention to the combination of QCs in parallel execution and their layout on the quantum processor, and reducing unwanted interference between QCs caused by crosstalk. We also propose a software-based crosstalk detection protocol that efficiently and successfully characterizes the hardware’s suitability for multi-programming. We found a trade-off between the success rate and execution time of the multi-programming. This would be attractive not only to quantum computer service but also to users around the world who want to run algorithms of suitable scale on NISQ processors that have recently attracted great attention and are being enthusiastically investigated.

INDEX TERMS Quantum computing, NISQ, multi-programming, compiler, Crosstalk

I. INTRODUCTION Current processors, called Noisy Intermediate-Scale Quantum (NISQ) [6], are not immune to noise, which causes a high error rate and greatly affects the reliability of the computation.

With the advent of cloud quantum computing systems, quantum computing has become familiar to researchers and developers around the world. The more users and tasks from various demands and backgrounds have increased, the more it is important to maximize the throughput of the NISQ processors. To operate efficiently, executing multiple quantum tasks concurrently can be one solution. However this method is not trivial and involves fundamental challenges [7]–[10].

It is difficult to explain the whole range of errors of computation on NISQ processors by using only information from standard error characterization techniques such as randomized benchmarking [11], [12].

Though quantum tomography estimates statistical reliability of a quantum state, it is requires large amounts of data exponential in the number of qubits for complete state tomography. To maximize the utilization and performance of a NISQ processor, we should take into account not only the standard model of isolated qubits but also the detection model for context-dependent errors, which requires a small cost [13].

In the case of superconducting qubit systems, effects of crosstalk on the gate errors is a serious problem [14], [15]. When multiple quantum circuits (QC) are executed in parallel, as resource usage of the processor increases, unwanted interference may occur due to crosstalk noise between independent QCs, which may affect the calculation results.

In this work, we introduce palloq (parallel allocation of QCs), a system for improving the performance of multi-programming on NISQ processors. Our system consists of two parts: first, the multiple circuit composer to maximize searches for an effective combination of the application circuits (a knapsack-like problem); second, the crosstalk-aware layout method that allocates hardware qubits to multiple
QCs taking into account both local error rate and nonlocal noise (crosstalk). We also take into account the cost of crosstalk characterization and propose a novel detection method. We show the performance of our system by executing dozens to low hundreds of queued quantum tasks as a multi-programming workload on the real-world cloud quantum computing platform, IBM Quantum Experience, and measure the success rate of the individual QCs and total execution time.

This paper is organized as follows. In Sec. II we review the cloud quantum computing environment, quantum multi-programming and crosstalk effect on NISQ processors. In Sec. III first, we describe the crosstalk characterization approach in previous work, then introduce our novel characterization method. In Sec. IV we propose compilation methods for efficient multi-programming. In Sec. V we show the experimental results on quantum processors and evaluate our proposed approach. Finally, we conclude paper in Sec. VI.

II. BACKGROUND
A. CLOUD QUANTUM COMPUTING
With the advent of cloud quantum systems i.e. quantum computing as a service (QCaaS) [16]–[22], many researchers and developers from a variety of domains are becoming quantum users. QCaaS provides the quantum resource that allows opportunities ranging from conducting basic experiments [23] to developing applications that include quantum simulation, quantum machine learning, and optimization [24].

Cloud quantum computing architectures consist of components that include Quantum Processors, Analog Digital control, Real-time control systems, WEB servers and classical databases, the Internet, and End users, as in Fig. 1.

Why use a cloud quantum system instead of a local server or a quantum laptop? In general, there are several reasons for the migration of the service from desktop and corporate server rooms to a cloud platform [25], [26]. For the individual users, the total control of the software, OS and low-level utility, and subsequent revisions to other programs comes with a price. For the service providers, the internet-based service can be developed, tested, and operated on the platform provider’s choice instead of coping with various user’s environments. In the case of quantum computation, the development and operation, which includes daily calibration, of a quantum computer are very expensive and specialized tasks [27], [28]. Languages, tools, and environments for the development of the quantum program are still not sufficient. By providing them comprehensively as cloud services, users can utilize the quantum resources without being bothered by maintenance.

The rapid increase in users, urgent access for limited quantum resources, and the number of queued jobs are becoming serious issues.

B. PERFORMANCE OF QUANTUM COMPUTER
Several metrics for performance analysis of quantum computers have been proposed [29]–[31]. Quantum Computing performance is governed by three factors: 1) the size of the problem that be encoded which is determined by the number of physical qubits on a processor, 2) the size of a quantum circuit that can be faithfully executed, which is mainly determined by error rates of each operation and lifetime of qubits, and 3) the number of circuits that can
be executed per unit time, which is related to the quantum and classical processing speed. In this paper, we focus on the improvements of 2: the output fidelity of QCs, and 3: the number of QCs executed at a time by a quantum multi-programming.

C. QUANTUM MULTI-PROGRAMMING

Quantum multi-programming is a method for improving the throughput and utilization of the NISQ processor by executing multiple QCs simultaneously, instead of keeping the unemployed qubits idle, as shown in Fig. 2. In previous work, several challenges were discussed as follows [7], [8]: 1). Fair hardware resource allocation for every individual task. The difficulty of this issue comes from the variations of characteristics of each physical qubits in the processor including operational error rates and qubit lifetimes [32]. To solve this, the compiler needs to take this error information into account to optimize the circuit. 2). Avoidance of unwanted interference between the individual QC. 3). Optimization of the operational timing of each circuit to minimize the unnecessary decoherence effect. In the case of multi-programming several QCs with different depth (duration of execution), the shorter circuits suffer wait duration until the longer circuit’s operation ends, which may cause the decaying of a quantum state prepared by shorter circuits and reduce the output reliability.

Improving the utilization of the processor by executing multiple programs concurrently can increase the unwanted interference between independent QCs. To reduce serious destructive interference, one option is to monitor and compare the performance of parallel execution and to feed the result into the next execution phase, either single or in parallel [7]. Rather than that, Ohkura [9], and Dou and Liu [10] discussed directly focusing on the crosstalk noise on the device which causes non-local errors on QCs of multi-programming. They tried to characterize the crosstalk in the processor and optimize qubit allocation along with it. The problem is the crosstalk characterization grows quadratically in the number of hardware qubits, as we discuss in Sec. III.

D. CROSSTALK IN NISQ PROCESSOR

Crosstalk is known to be a significant source of noise in the quantum processor. This type of error can be explained from several aspects, but it is simply the unwanted interaction between coupled qubits in the processor. It is known that there is a trade-off between the strength of qubit interaction and the magnitude of unwanted crosstalk noise [33], [34]. One type of crosstalk is caused by simultaneous operations between specific pairs of qubits. In this paper, we focused on the unwanted interaction due to the two qubit (CX gate) operations. This types of crosstalk is known to occur in the current quantum architectures including superconducting systems and trapped ions [35], [36].

The tuning and mitigation of crosstalk directly become big challenges when developing larger processors [34], [37], [38]. There are several software approaches to reducing crosstalk error introduced in previous work. In the case of tunable quantum processors including Google’s architecture [39], we can tune qubit frequencies or control specific couplers to disable and shut down the leakage errors [14], [40].
In contrast, in fixed frequency qubit systems including IBM Q System, we can optimize the circuit scheduler to avoid concurrent execution of correlated qubits in the processor [41]. In this paper, we focused on this fixed qubit system, and provide the solution by a novel layout method in the circuit compilation process.

III. Crosstalk Characterization

To understand the performance of quantum processors affected by local and non-local errors and its ability to concurrently execute multiple QCs, we need to characterize crosstalk in the processor. To simplify the problem, we only take into account how big the average crosstalk on the processor is rather than where these occur, i.e. the location of qubits.

A. The Cost of Characterization

The complexity of crosstalk characterization often scales exponentially with the system size. Recently, several works showed ways to suppress the cost of crosstalk characterization. One practical protocol introduced in [10], [41] is the comparison of the error rate in the case of individual and parallel execution by using Simultaneous Randomized Benchmarking (SimRB). For example, in Fig. 3 some pairs of two-qubit errors can be detected in parallel, e.g. \( (q_i, q_j) \) and \( (q_k, q_l) \). If the error rate from SimRB \( \epsilon(q_i, q_j)|q_k, q_l) \) is significantly different from the individual RB \( \epsilon(q_i, q_j) \), there is an unwanted correlation between them.

The combination of these two-qubit pairs grows quadratically in the size of the processor. To avoid this situation, in a previous study [41], Murali et al. provide some rules to reduce this overhead. 1) Characterize one hop pairs. Through the experiments, they found the tendency of occurrence of crosstalk is limited only at one hop on the IBM Q system they used. This rule is suppressing the detection cost by ignoring the pairs more than one hop apart. They also pointed out some older devices have long-range crosstalk strong enough to be a concern. 2) Characterize high crosstalk pairs only. They also found the existence of crosstalk tends to be stable in time and space.

Although this method can detect crosstalk distribution on the processors, it still takes several hours, and it may be impractical in the current situation because the size of processors is continuously getting bigger, and these experiments are queued and run on the cloud system in the presence of other participants.

B. Physical Buffer and Success Rate

In this section, we introduce a physical buffer, which is the number of idle qubits between QCs, to mitigate crosstalk effect of the concurrent execution of multiple QCs. We conducted a preliminary experiment to quantify how the physical buffer affects the output reliability of individual tasks in the concurrent execution. We used the Toffoli gate as benchmark. Due to the compilation, that includes the SWAP gate that consists of three CX gates and the qubit routing along with the topology of the processor, shown in Fig. 4 for a total of 10 CX gates.

FIGURE 3: Simultaneous Randomized Benchmarking (SimRB) Upper diagram shows ordinary RB on two-qubits. RB applies random clifford operations with varying the length of gates and estimates its error rates. In the case of Simultaneous RB, applying RB on more than two hardware areas and comparing the error rates to single RB case, measure the conditional error rates of hardware qubits. In this research, we only conducted two-qubits RB and SimRB.

We varied the number of physical buffer between circuits and the number of Toffoli gates as parameters to see how the success rates change, shown in Fig. 5. Fig. 6 shows that in only the case of adjacent circuits, i.e. no physical buffer, the success rate significantly drops. With the increase of number of buffer, the success rate is recovered. And this change appears only for circuits of more than 20 CX gates. This leads us to the following insights. For the concurrent execution in practice, 1) we don’t care about crosstalk for the shorter circuits, and 2) there is a threshold number of hops of physical buffer that can improve the output fidelity. And in this case, 1 physical buffer is enough until the CX circuit depth reaches 30.

C. Benchmark of Crosstalk Immunity

Although crosstalk is the major source of error and may decrease the reliability of the concurrent execution, with the increasing number of qubits in the processors, the cost to characterize the noise increase quadratically. We show a novel detection protocol combining RB methods with relatively low detection costs. To analyze the crosstalk tolerance of processors, we utilized the coefficient of variation of gate errors as the metric and compared several processors.
We focus on how the crosstalk impacts the average and variance of error rates. First, we apply RB for every qubit or two-qubit pair in the processor and calculate the average and variance of error rates in the single execution case. Then, we run SimRB for all the qubits at the same time and also calculate the average and variance. Comparison of average and variance of error rates between those two cases leads to the quantitative analysis of crosstalk effects on the whole performance and immunity of the processor.

We conducted this benchmark on several current IBM quantum processors and showed the comparison of those performances in Fig. 7. We measured the CX gate error rate of each processor by utilizing RB. Blue box plots represent the distribution of CX gate error rate and black dots are the error value of each physical two-qubit connection. The orange box plots also represent error rates but in the case of concurrent execution (SimRB). We ran several patterns of CX gates combination that can be executed concurrently and took the average value of error rates of each case.

For all processors, the variance and average error rates increase in the case of concurrent execution, indicating the presence of the crosstalk noise. In particular, IBMQ Toronto, IBMQ Sydney, and IBMQ Manhattan show significant interference by other operations performed on the other regions. The performance of multi-programming directly depends on this crosstalk interference as we discuss in Sec. V.

IV. THE PALLOQ SYSTEM

We propose palloq, a system including layout synthesis for multiple QCs and a job scheduler to manage efficient and high fidelity quantum multi-programming. The detail of procedure are explained in appendix [Pseudocode. We published the source code at [https://github.com/rum-yasuhiro/palloq](https://github.com/rum-yasuhiro/palloq).

The palloq responsible for the compilation phase and the user’s job management which is provided by WEB server in the cloud computing architecture we showed in Fig. 1.

This compiler pass takes several QCs written in OpenQASM [42] and the local gate error information of device as input.

Our layout synthesis consists of a heuristic based on Noise-Adaptive layout which analyzes the device’s calibration data and searches for better allocation using a greedy approach [43]. First, it parses the calibration data and hardware qubit connection to create a weighted graph $G_{HW}(V, E)$. $V$, $E$, and weight represents the physical qubits as the vertices, two-qubit connections of the hardware as the edges, and the reliability $r = 1 - \epsilon$, where $\epsilon$ is error rate of two-qubit operation between physical qubits. In the same way, each input QC is treated as a weighted directed graph $G_{QC}(V, E)$, where vertices $V$ are the qubits in the QC, edges $E$ are two-qubit gates, and weight is the number of two-qubit gates performed on the same two-qubit pair. The compiler searches for the best reliable physical qubits candidates heuristically and allocates them to the highest weighted edges in the...
The circuit’s graph. Repeat this procedure until all the circuit components are placed.

As we discussed in Sec. [III-B] for the shorter circuits, we don’t care about the crosstalk, and for the relatively larger circuits, we only care about the physical distance between circuits and optimize them locally. Our software takes physical qubit distance as input. Every time each circuit is allocated to hardware qubits, then disable the qubits around them to create a distance to others.

V. EXPERIMENTS AND EVALUATION

To evaluate our proposal, we conducted an experiment varying the physical buffer among the multiple circuits. In the entire experiment, we focus on the output reliability and total execution time and hardware usage.

We use small benchmark circuits from previous work [44] as shown in Table 1. The details of the processors and the software we used are shown in Table Tab.3.

A. METRICS

To quantify the performance of our proposed method, we utilized Probability of Successful Trial (PST) [32]. For NISQ system that run the given programs a specified number of times, known as “shots”, the quantum computation outputs the answer as a probability distribution of candidate bit strings. The number of successful trials is defined as how many times the each shots hit the correct bit strings. We chose the benchmark circuits whose computational result includes only one or a small number of answers for the solution space for ease of handling with PST. When the QC finishes successfully without any error, PST is 1.

As a baseline we compare the results from a noisy quantum device to a classical simulator as a noiseless case. PST is defined as follows:

\[
PST = \frac{\text{Number of Successful Trials}}{\text{Number of Total Trials}}
\]  

B. EXECUTION DURATION AND OUTPUT RELIABILITY

First, we prepared 100 QCs from the benchmark set and queued them as an input to our compiler. Varying the physical qubit buffer 0 to 3, we count the output PST and total execution time of concurrent execution.

Fig. 8 shows that PST of 100 circuits varies with physical buffer. For all quantum devices, in the case of buffer more than one, the average PST is better than the case of buffer zero, which is the densest layout and highest throughput per case. Which means, in these experiments, we obtain higher reliability of computation at the expense of throughput of concurrent execution.

Fig. 9 shows total execution time of 100 circuits as we vary physical buffer. For the execution time, we count circuit duration time (dt) of all concurrent execution round and 1 dt = \( \frac{5}{9} \) ns. It shows a larger buffer reduces hardware usage and total execution time linearly. For all devices, around 80% of physical qubits are used in the case of buffer 0. In the case of buffer 2 and 3, the hardware usage is only half of the densest case. On the other hand, for all devices, the total circuit duration time increased by a factor of two from the densest to sparsest.

C. ANALYSIS

Here we describe the trade-off between crosstalk and throughput of concurrent execution. In general we desire the success of computation with higher reliability and throughput. The success rate of concurrent computation, which depends on many factors like gate duration time, measurement duration time, and the size of processors. Based on experimental results shown in Fig. 8, we defined the improvement (gain) of output reliability g as:

\[
g = \max_i(PST_i - PST_j)
\]  

where the \( \overline{PST_i} \) is average value of PSTs of i physical qubit buffered layout of concurrent execution. In this experiment, for all cases, i = 0 and j is 2 or 3. Based on the result shown in Fig. 7, the case of buffer 0 has the highest throughput.

Utilizing the coefficient of variation (CV):

\[
CV = \frac{\sigma}{\mu}
\]
FIGURE 8: Success rate and the physical buffer These box plots represent the distribution of PST of benchmark circuits executed on the real quantum devices.

FIGURE 9: Hardware usage and total execution time

where $\sigma$ is the standard deviation and $\mu$ is the average of the given distribution. In this case, crosstalk presence $ct$ represents the degree of change of variation of CX error rate from RB to SimRB.

Fig. 10 shows the relationship between the presence of crosstalk on the device and gain of improvement by physical buffer.

We used three 27-qubit devices and two 65-qubit devices, and for both cases we can see the positive correlation. Referring to Fig. 9 as we increase the number of physical qubit buffer, the throughput of computation drops. For processors with relatively strong crosstalk, it is worth reducing the throughput to gain the improved output fidelity of the computation.

VI. CONCLUSION

This paper proposed and evaluated a compiler method for concurrent execution of multiple quantum circuits which includes layout and schedule. First, we showed a practical
crosstalk characterization method to reduce the detection cost that is critical for the near-term scale quantum processors. For the evaluation, we show our compiler efficiently processes the multiple quantum circuits avoiding the crosstalk and trade-off between the success rate of quantum circuits and the throughput of the processors.

Also taking into account the crosstalk noise is meaningful not only for improving the performance of multi-programming but also when considering the security of future cloud quantum computation.

**APPENDIX. SETUP FOR EXPERIMENTS**

The quantum circuit for benchmark our proposed software, listed in Tab. 1. The processors we use are listed in Tab. 2. And the version of software packages we use are listed in Tab. 3.

Each experiment was conducted on the dates listed in Tab. 4.

**APPENDIX. PSEUDOCODE**

Here we show the pseudocode of the algorithm we introduced in Sec. [V]

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**REFERENCES**

[1] J. A. Jones, “Quantum computing and nuclear magnetic resonance,” PhysChemComm, vol. 4, no. 11, pp. 49–56, 2001.

[2] J. Clarke and F. K. Wilhelm, “Superconducting quantum bits,” Nature, vol. 453, no. 7198, pp. 1031–1042, 2008.

[3] D. Kielpinski, C. Monroe, and D. J. Wineland, “Architecture for a large-scale ion-trap quantum computer,” Nature, vol. 417, no. 6890, pp. 709–711, 2002.

[4] M. G. Dutt, L. Childress, L. Jiang, E. Togan, J. Maze, F. Jelezko, A. Zibrov, P. Hammer, and M. Lukin, “Quantum register based on individual electronic and nuclear spin qubits in diamond,” Science, vol. 316, no. 5829, pp. 1312–1316, 2007.

[5] J. L. O’Brien, A. Furusawa, and J. Vukšićovic, “Photonic quantum technologies,” Nature Photonics, vol. 3, no. 12, pp. 687–695, 2009.

[6] J. Preskill, “Quantum computing in the NISQ era and beyond,” Quantum, vol. 2, p. 79, 2018.

[7] P. Das, S. S. Tannu, P. J. Nair, and M. Qureshi, “A case for multi-programming quantum computers,” in Proceedings of the 52nd Annual IEEE/ACM International Symposium on Microarchitecture, ser. MICRO ’52. New York, NY, USA: Association for Computing Machinery, 2019, p. 291–303. [Online]. Available: https://doi.org/10.1145/3352460.3358287

[8] X. Dou and L. Liu, “A new qubits mapping mechanism for multi-programming quantum computing,” in Proceedings of the ACM International Conference on Parallel Architectures and Compilation Techniques, ser. PACT ’20. New York, NY, USA: Association for Computing Machinery, 2020, p. 349–350. [Online]. Available: https://doi.org/10.1145/3410463.3414659

[9] Y. Ohkura, “Crosstalk-aware nisq multi-programming,” 2021. [Online]. Available: https://aqua.stf.wide.ad.jp/publications/rum_bthesis.pdf

[10] S. Niu and A. Todri-Sanial, “Enabling multi-programming mechanism in the NISQ era,” arXiv preprint arXiv:2102.05321, 2021.

[11] E. Knill, D. Leibfried, R. Reichle, J. Britton, R. B. Blakestad, J. D. Jost, C. Langer, R. Ozeri, S. Seidelin, and D. J. Wineland, “Randomized benchmarking of quantum gates,” Phys. Rev. A, vol. 77, p. 012307, Jan 2008. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevA.77.012307

[12] J. M. Chow, J. M. Gambetta, L. Tornberg, J. Koch, L. S. Bishop, A. Houck, B. R. Johnson, L. Frunzio, S. M. Girvin, and R. J. Schoelkopf, “Randomized benchmarking and process tomography for gate errors in a solid-state qubit,” Phys. Rev. Lett., vol. 102, p. 090502, Mar 2009. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevLett.102.090502

[13] K. Rudinger, T. Proctor, D. Langharst, M. Sarovar, K. Young, and R. Blume-Kohout, “Probing context-dependent errors in quantum processors,” Phys. Rev. X, vol. 9, p. 021045, Jun 2019. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevX.9.021045

[14] P. Mundada, G. Zhang, T. Hazard, and A. Houck, “Suppression of qubit crosstalk in a tunable coupling superconducting circuit,” Phys. Rev. Appl., vol. 12, p. 054023, Nov 2019. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevApplied.12.054023

[15] D. C. McKay, S. Sheldon, J. A. Smolin, J. M. Chow, and J. M. Gambetta, “Three-qubit randomized benchmarking,” Phys. Rev. Lett., vol. 122, p. 200502, May 2019. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevLett.122.200502

[16] Amazon, Amazon Braket [https://aws.amazon.com/jp/braket/]

[17] D-wave, D-wave Leap, [https://cloud.dwavesys.com/leap/]

[18] Google, Quantum Computing Playground, [https://experiments.withgoogle.com/quantum-computing-playground/]

[19] IBM, IBM Quantum Experience, [https://quantum-computing.ibm.com/]

[20] Microsoft, Microsoft Azure Quantum, [https://azure.microsoft.com/en-us/services/quantum/]

[21] Rigetti, Rigetti Forest, [https://www.rigetti.com/quantum-computing/]

[22] Xanadu, Xanadu Quantum Cloud, [https://www.xanadu.ai/]

[23] S. J. Devitt, “Performing quantum computing experiments in the cloud,” Phys. Rev. A, vol. 94, p. 032329, Sep 2016. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevA.94.032329

[24] A. Montanaro, “Quantum algorithms: an overview,” npj Quantum Information, vol. 2, no. 1, pp. 1–8, 2016.

[25] B. Hayes, “Cloud computing,” Commun. ACM, vol. 51, no. 7, pp. 9–11, Jul 2008. [Online]. Available: https://doi.org/10.1145/1364782.1364786

[26] M. Armbrust, A. Fox, R. Griffith, A. Joseph, R. Katz, A. Konwinski, G. Lee, D. Patterson, A. Rabkin, I. Stoica, and M. Zaharia, “A view of cloud computing,” Commun. ACM, vol. 53, no. 4, pp. 50–58, apr 2010. [Online]. Available: https://doi.org/10.1145/1721654.1721672

[27] S. S. Tannu and M. K. Qureshi, “A case for variability-aware policies for nisq-era quantum computers,” arXiv preprint arXiv:1805.10224, 2018.

[28] D. C. McKay, T. Alexander, L. Bello, M. J. Biercuk, L. Bishop, J. Chen, J. M. Chow, A. D. Córcoles, D. Egger, S. Filipp et al., “Quick backend specifications for openqasm and openpulse experiments,” arXiv preprint arXiv:1809.03452, 2018.

[29] A. D. Córcoles, M. Takita, K. Inoue, S. Lekach, Z. K. Minev, J. M. Chow, and J. M. Gambetta, “Exploiting dynamic quantum circuits in a quantum algorithm with superconducting qubits,” Phys. Rev. Lett., vol. 127, p. 100502, Aug 2021. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevLett.127.100501

[30] T. Lubinski, S. Johri, P. Varosy, J. Coleman, L. Zhao, J. Necaise, C. H. Baldwin, K. Mayer, and T. Proctor, “Application-oriented performance benchmarks for quantum computing,” arXiv preprint arXiv:2110.03137, 2021.

[31] A. Wack, H. Paik, A. Jayadi-Abhari, P. Jurcevic, I. Faro, J. M. Gambetta, and R. Johnson, “Quality, speed, and scale: three key attributes to measure the performance of near-term quantum computers,” arXiv preprint arXiv:2110.14108, 2021.

[32] S. S. Tannu and M. K. Qureshi, “Not all qubits are created equal: A case for variability-aware policies for NISQ-era quantum computers,” arXiv preprint arXiv:2110.03137, 2021.
### TABLE 1: Small Benchmark Circuits.

We picked several small size quantum circuit to benchmark our proposal from the benchmark circuit set called QASMBench [44].

| Benchmark   | Description                        | Qubits | Gates | CX |
|-------------|------------------------------------|--------|-------|----|
| deutsch     | Deutsch algorithm with 2 qubits for $f(x) = x$ | 2      | 5     | 1  |
| grover      | Grover’s algorithm                  | 2      | 16    | 2  |
| linesolver  | Solver for a linear equation of one qubit | 3      | 19    | 4  |
| toffoli     | Toffoli gate                        | 3      | 18    | 6  |
| fredkin     | Fredkin gate                        | 3      | 19    | 8  |
| adder       | Quantum ripple-carry adder          | 4      | 23    | 10 |
| error_correction3 | Error correction with distance 3 and 5 qubits | 5      | 114   | 49 |

**Algorithm 1:** Physical distance layout

**Input:** Queued DAG circuits \(queue\), Processor’s topology graph weighted by CX gate reliability \(G_{HW}\). Buffer to adjacent circuit \(d\)

**Output:** List of Multi-programming circuits with layout as MP

Set MP = empty list;
\(queue := \{G_{HW_S} \in G_{HW} \mid \text{connected subgraph of } G_{HW}\}\);
while length(queue) > 0 do
    \(DAG = queue.pop(0)\);
    if size(max(S)) > size(DAG) then
        Set layout, pending_qubits, prog, hw to empty list;
        Set multi_QC to empty DAG;
        \(G_{QC} \leftarrow \text{convert } DAG\); /* Convert DAG to graph \(G_{QC}\) weighted by number of CX gates */
        pending_qubits \leftarrow G_{QC}.nodes;
        \(q_{prog1}, q_{prog2} \leftarrow \max\{G_{QC}.edges\}\); /* Heaviest program edge */
        pending_qubits.remove(q_{prog1}, q_{prog2});
        prog.append(q_{prog1}, q_{prog2});
        \(q_{hw1}, q_{hw2} \leftarrow \max\{G_{HW_S}.edges \mid \text{size}(G_{HW_S}) > \text{size}(DAG)\}\); /* Most reliable HW qubits */
        while pending_qubits not null set do
            \(q_{prog} \leftarrow \max\{\text{edge}(q_{adj}, q_{in}) \in G_{QC} \mid q_{in} \in \text{prog}\}\);
            \(q_{hw} \leftarrow \max\{\text{edge}(q_{adj}, q_{in}) \in G_{HW_S} \mid q_{in} \in \text{hw}\}\);
            pending_qubits.remove(q_{prog});
            layout.append({q_{prog}, q_{hw}});
            prog.append(q_{prog});
            hw.append(q_{hw});
        end while
        Delete used qubits;
        \(G_{HW}.\text{remove(hw)}\);
        \(G_{HW}.\text{remove}(q \in G_{HW} \mid d - \text{neighbored to } hw)\);
        \(S := \{G_{HW_S} \in G_{HW} \mid \text{connected subgraph of } G_{HW}\}\);
        multi_QC.append(DAG)
    else
        MP.append({multi_QC, layout});
    end if
end while
return MP
TABLE 2: Processors

| Name               | Spec                      | Name               | Spec                      |
|--------------------|---------------------------|--------------------|---------------------------|
| Intel Core i9 processor | 2.3 GHz, 32 GB RAM     | Python             | 3.8.5                     |
| IBMQ Toronto       | Falcon r4 27-qubit QV32   | qiskit             | 0.29.0                    |
| IBMQ Sydney        | Falcon r4 27-qubit QV32   | qiskit-terra       | 0.17.0                    |
| IBM Kawasaki       | Falcon r5.11 27-qubit QV32| qiskit-aer        | 0.8.2                     |
| IBMQ Manhattan     | Hummingbird r2 65-qubit QV32| qiskit-ignis      | 0.5.1                     |
| IBMQ Brooklyn      | Hummingbird r2 65-qubit QV32| qiskit-ibmq-provider | 0.16.0                   |

TABLE 3: Software version

| Experiment                                   | Date-time       |
|----------------------------------------------|-----------------|
| Physical buffer of multiple circuits in Fig. 6 on IBMQ Manhattan | 2021/05/10 - 2021/05/14 |
| Crosstalk detection in Fig. 7 on IBMQ Toronto | 2021/07/09      |
| Crosstalk detection in Fig. 7 on IBMQ Sydney | 2021/07/09      |
| Crosstalk detection in Fig. 7 on IBM Kawasaki | 2021/07/09     |
| Crosstalk detection in Fig. 7 on IBMQ Manhattan | 2021/07/10     |
| Crosstalk detection in Fig. 7 on IBMQ Brooklyn | 2021/07/10     |

TABLE 4: Date and time when experimental data have been taken

magnetic fields,” Phys. Rev. Lett., vol. 101, p. 090502, Aug. 2008. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevLett.101.090502

[37] K. Rudinger, T. Proctor, D. Langharst, M. Sarovar, K. Young, and R. Blume-Kohout, “Probing context-dependent errors in quantum processors,” Physical Review X, vol. 9, no. 2, p. 021045, 2019.

[38] R. Harper, S. T. Flammia, and J. J. Wallman, “Efficient learning of quantum noise,” Nature Physics, vol. 16, no. 12, pp. 1184–1188, 2020.

[39] F. Arute, K. Arya, R. Babbush, D. Bacon, J. C. Bardin, R. Barends, R. Biswas, S. Boixo, F. G. Brandao, D. A. Buell et al., “Quantum supremacy using a programmable superconducting processor,” Nature, vol. 574, no. 7779, pp. 505–510, 2019.

[40] Y. Ding, P. Gokhale, S. F. Lin, R. Rines, T. Propson, and F. T. Chong, “Systematic crosstalk mitigation for superconducting qubits via frequency-aware compilation,” in 2020 53rd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO). IEEE, 2020, pp. 201–214.

[41] P. Murali, D. C. Mckay, M. Martonosi, and A. Javadi-Abhari, “Software mitigation of crosstalk on noisy intermediate-scale quantum computers,” in Proceedings of the Twenty-Fifth International Conference on Architectural Support for Programming Languages and Operating Systems, ser. ASPL ’20. New York, NY, USA: Association for Computing Machinery, 2020, p. 1001–1016. [Online]. Available: https://doi.org/10.1145/3373376.3378477

[42] A. W. Cross, L. S. Bishop, J. A. Smolin, and J. M. Gambetta, “Open quantum assembly language,” arXiv preprint arXiv:1707.03429, 2017.

[43] P. Murali, J. M. Baker, A. Javadi-Abhari, F. T. Chong, and M. Martonosi, “Noise-adaptive compiler mappings for noisy intermediate-scale quantum computers,” in Proceedings of the Twenty-Fourth International Conference on Architectural Support for Programming Languages and Operating Systems, 2019, pp. 1015–1029.

[44] A. Li, S. Stein, S. Krishnamoorthy, and J. Ang, “Qasmbench: A low-level qasm benchmark suite for NISQ evaluation and simulation,” arXiv preprint arXiv:2005.13018, 2020.