A 0.85 V, 4.9 ppm/°C inherent temperature compensated voltage reference with −82 dB PSRR

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Abstract: A novel high PSRR and inherent temperature compensated CMOS voltage reference is present. A resistorless self-biased current source (RLSBCS) is proposed, formed by a gate-source voltage division (GSVD) structure, to achieve a temperature compensated proportional threshold-voltage difference. Meanwhile, a self-cascode structure is adopted to further cancel the residual negative temperature dependence of proposed threshold-voltage difference. Besides, feedback and self-bias techniques are introduced to enhance PSRR. The temperature coefficient is 4.9 ppm/°C in the temperature range of −25°C to 75°C and PSRR at DC is −82 dB with a power consumption of 9.8 nW.

Keywords: CMOS voltage reference, low power, high PSRR, low TC

Classification: Integrated circuits

References

[1] K. N. Leung, et al.: “A 2-V 23-uA 5.3 ppm/°C curvature-compensated CMOS bandgap voltage reference,” IEEE J. Solid-State Circuits 38 (2003) 561 (DOI: 10.1109/JSSC.2002.808328).
[2] R. T. Perry, et al.: “A 1.4 V supply CMOS fractional bandgap reference,” IEEE J. Solid-State Circuits 42 (2007) 2180 (DOI: 10.1109/JSSC.2007.905236).
[3] M. Seok, et al.: “A portable 2-transistor Picowatt temperature-compensated voltage reference operating at 0.5 V,” IEEE J. Solid-State Circuits 47 (2012) 2534 (DOI: 10.1109/JSSC.2012.2206683).
[4] Y. Zeng, et al.: “A 12.8 nA and 7.2 ppm/°C CMOS voltage reference without amplifier,” IEICE Electron. Express 15 (2018) 20171220 (DOI: 10.1587/elex.15.20171220).
[5] Y. Liu, et al.: “An ultralow power subthreshold CMOS voltage reference without requiring resistors or BJTs,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 26 (2018) 201 (DOI: 10.1109/TVLSI.2017.2754442).
[6] Y. P. Tsividis and R. W. Ulmer: “A CMOS voltage reference,” IEEE J. Solid-
1 Introduction

Voltage reference (VR) is a fundamental block in analog and mixed-signal circuit. The conventional Bandgap VR using bipolar transistors usually requires high supply voltage and consumes around µW power [1, 2]. To overcome those disadvantages, the state-of-the-art VRs gradually substitute subthreshold MOSFETs for bipolar transistors [3, 5, 6, 9]. As a result, the supply voltage can reduce to under 1 V and power consumption may be lower to several nW or even pW [4, 7, 8, 10]. Unfortunately, the subthreshold MOSFET circuit commonly employs high values of resistors, which may occupy a large silicon area. Therefore, resistorless circuits have intrinsic advantages.

A resistorless inherent temperature compensation VR with high power supply rejection ratio (PSRR) is proposed in this paper. The presented VR uses gate-source voltage division (GSVD) structure combined with low threshold voltage transistor and high threshold voltage transistor to lower temperature coefficient (TC) and adjust the value of VR. Besides, a negative feedback loop and self-bias techniques will enhance the PSRR of VR.

2 Proposed VR circuit

The proposed VR circuit is shown in Fig. 1(a), which consists of three parts: start-up circuit, auxiliary amplifier circuit and the core of VR circuit. The start-up circuit is used to get rid of the zero-degenerate point. The auxiliary amplifier circuit is for PSRR enhancement, and the core of VR circuit includes an inherent temperature compensation for lower TC. All the MOSFETs are biased in subthreshold region. Transistors from M1 to M_N have low-threshold-voltage, and the other transistors are normal-threshold-voltage transistor.

2.1 Temperature-dependence principle of generated VR

As shown in Fig. 1(a), the core of voltage reference circuit includes GSVD part and self-cascode (SC) part. The gate-source voltage of M0 with normal threshold voltage, \( V_{GS(M0)} \), is divided by transistors M1 to M_N with low threshold voltage. Since \( V_{GS(M0)} \) in subthreshold region is a complementary to absolute temperature
(CTAT) voltage, the voltage at node X will be a divided CTAT voltage with proportionally shrunken negative TC. Then a single stage SC is enough for temperature compensation. The detailed analysis of core of voltage reference is as following.

According to the voltage-current characteristics of transistors in subthreshold region, supposed \( I_0 : I_1 : I_2 : I_3 = K_1 : 1 : K_2 : K_1 \), the aspect ratio of transistors \( M_i \) is \( S_i \) and the aspect ratio of \( M_1 \) to \( M_N \) is the same, then the gate-source voltage of \( M_0, M_1 \) to \( M_X \) and \( M_X + 1 \) to \( M_N \) can be given by three categories:

\[
V_{GS,0} = V_{TH,0} + mVT \ln \left( \frac{I_0}{S_0 I_{SO,0}} \right), \quad V_{GS,1} = \ldots = V_{GS,M_X} = V_{TH,1} + mVT \ln \left( \frac{1 + K_2 I_1}{S_1 I_{SO,1}} \right), \quad V_{GS, MN} = V_{TH,1} + mVT \ln \left( \frac{I_1}{S_1 I_{SO,1}} \right),
\]

where \( m \) is the subthreshold slope factor; \( VT \) is the thermal voltage; \( V_{TH,0} \) and \( V_{TH,1} \) are the threshold voltage of \( M_0 \) and \( M_1 \) to \( M_N \), respectively; \( I_{SO,0} \) and \( I_{SO,1} \) are process-dependent saturation current of \( M_0 \) and \( M_1 \) to \( M_N \), respectively; \( I_1 \) is the current through \( M_2 \).

According to Kirchhoff’s law and three above categories, if we assume \( N \) = \( \frac{V_{TH,0}}{V_{TH,1}} \), the voltage at node X is equal to \( X V_{GS,1} \), which is:

\[
V_X = X \frac{N}{N-1} \left\{ \Delta V_{TH} + mVT \ln \left( \frac{K_1 S_1 I_{SO,1}}{S_1 I_{SO,0}} \right) + \left( N - 1 \right) mVT \ln \left( 1 + K_2 \right) \right\}. \tag{1}
\]

As shown in Eq. (1), the voltage at node X is scaled down by \( X/(N-1) \). Besides, the temperature drift of \( V_X \) is also decreased from three aspects. Firstly, \( V_{TH,0} / V_{TH,1} \) leads to smaller TC compared with \( V_{TH,0} \). Secondly, those terms with \( V_T \) has positive TC characteristics to further reduce the negative TC. Finally, the whole negative TC is decreased by \( X/(N-1) \). By this method, a single stage SC, consisted of \( N_1 \) and \( N_2 \), is enough for temperature compensation. As a result, the output reference voltage of proposed VR is 

\[
V_{ref} = X V_{GS,1} + V_{DS,N1},
\]

specific expression is:

\[
V_{ref} = X \frac{N}{N-1} \left\{ \Delta V_{TH} + mVT \left[ \ln \left( \frac{K_1 S_1 I_{SO,1}}{S_0 I_{SO,0}} \right) \right] + \left( N - 1 \right) mVT \ln \left( \frac{S_1}{S_2} \right) \right\}. \tag{2}
\]

Considering the voltage difference between \( V_{TH,0} \) and \( V_{TH,1} \), and the requirement of \( V_{DS} \geq 100 \text{ mV} \) for proper bias condition, 5 and 2 are chosen for \( N \) and \( X \) in this design, respectively. Therefore, Eq. (2) can be rewritten as:
\[
V_{\text{ref}} = \frac{1}{2} (V_{\text{TH0}} - V_{\text{TH1}}) + mV_T A + mV_T B
\]  
(3)

where \( A = 0.5 \ln(I_{S0}/I_{S0}) = 0.5 \ln[\mu_1(T_0)/\mu_0(T_0)] - 0.5(a_1 - a_0) \ln T \), \( \mu_1 \) and \( a_i \) are carrier mobility and absolute temperature power of carrier mobility of transistor \( M_i \), respectively, \( \mu(T_0) \) is carrier mobility at temperature \( T_0 \); \( B = 0.5 \ln(K_{1S_1}/S_0) + \ln[(1 + K_2)S_{N1}/S_{N2}] \) is a positive temperature-independent constant. In order to investigate the temperature dependence of proposed VR, the TC of reference voltage is given by:

\[
\frac{\partial V_{\text{ref}}}{\partial T} = \frac{1}{2} (\beta_0 - \beta_1) + \frac{\partial [mV_T(A + B)]}{\partial T}
\]  
(4)

where \( \beta_0 \) and \( \beta_1 \) are the TCs for \( V_{\text{TH0}} \) and \( V_{\text{TH1}} \). In the proposed design, \( \beta_0 - \beta_1 < 0 \) is guaranteed and transistors with \(|\partial \mu_0/\partial T| < |\partial \mu_1/\partial T|\) are selected. Hence, \( A \) is smaller than zero with negative TC. Besides, the \( \ln T \) included in \( A \) make absolute negative TC increase with temperature rising. Since \( m \) increases greatly with temperature rising [6], then the third term in Eq. (3) functions as a high-order temperature compensation. Therefore, \( A + B \) is positive at low temperature region and negative at high temperature region. While \( A + B \) turns from positive to negative, \( \partial [mV_T(A + B)]/\partial T \) also turns from positive to negative. Finally, \( \partial V_{\text{ref}}/\partial T \) can be equal to zero again at a certain higher temperature in addition to lower temperature point.

For an optimal TC, 2 and 0.5 are chosen for \( K_1 \) and \( K_2 \). As shown in Fig. 3(a), when \( K_1 \) and \( K_2 \) get 10% larger, the PTAT voltage will be greater than the desired one and the value of VR will increase \([mV_T \ln(1.1)])/2\) and \([mV_T \ln(1.55/1.5)]\) respectively, and vice versa.

### 2.2 Principle of PSRR improvement

For PSRR analyzing, the complete noise paths of VR are shown in Fig. 2. According to Fig. 2, VDD noise can distribute to node B through path 4; path3 and positive feedback loop (PFL); path1 and negative feedback loop (NFL). NFL = \( g_m MP2 (R_0 MP2 || R_A) g_{mN0} (R_0 MP1 || R_{0N0}) \times g_{mN0}/g_{mP0} \) and PFL = \( g_m MP1 (R_0 MP1 || R_{0N0}) g_{mN0}/g_{mP0} \), where \( R_A = [3 + 2/(1 + K_2)]/g_{mN5} \) is the equivalent impedance.
of node A to ground and \( g_{mi} \) and \( r_{oi} \) are the transconductance and output resistance of transistor i. Since \( g_{mMP2}/g_{mM5} = g_{mMP1}/g_{mM0} = g_{mN2}/g_{mN0} \approx 1 \) with \( I_{P0} = I_{N0}, I_{MP1} = I_{M0}, I_{MP2} = I_{M5} \) and \( gm_{r} \approx 1 \) for transistors in subthreshold region, the loop gain of node B is:

\[
T_{\text{loop-B}} = NFL - PFL \approx \left( 2 + \frac{2}{1 + K_2} \right) g_{mM0}(r_{0MP1} \parallel r_{0M0})
\]

(5)

Transistors MC and MR act as loop compensation capacitor and zero resistor for stability enhancement. The total effect of VDD noise at node B can be express as:

\[
PSR_B = \frac{PSR_{\text{path4}}}{1 + T_{\text{loop-B}}} = \frac{(PSR_{\text{path1}}PSR_{\text{path2}} - PSR_{\text{path3}})g_{mN0}/g_{mP0}}{1 + T_{\text{loop-B}}}. \tag{6}
\]

Obviously, \( PSR_B \approx 1 + 1/T_{\text{loop-B}} \) with the same approximation conditions of Eq. (5). Where \( PSR_{\text{path1}} = (g_{mMP2} + 1/r_{0MP2})(r_{0MP2} || R_A), PSR_{\text{path2}} = g_{mM0}(r_{0MP1} || r_{0M0}), PSR_{\text{path3}} = (g_{mMP1} + 1/r_{0MP1})(r_{0MP1} || r_{0M0}), \) and \( PSR_{\text{path4}} = r_{0N0}/(1/g_{mP0} + r_{0N0}). \)

For node A, the loop gain of node A to D to B to A can be calculated as:

\[
T_{\text{loop-A}} = NFL - PFL \approx 3 + \frac{2}{1 + K_2}.
\]

(7)

Therefore, VDD noise at node A is:

\[
PSR_A = \frac{PSR_{\text{path1}} - PSR_B[g_{mMP2}(r_{0MP2} \parallel R_A)]}{(1 + T_{\text{loop-A}})}.
\]

(8)

Considering \( g_{mN1} \approx g_{mN2} \), then \( PSR_{\text{path8}} \approx 2/(5 + 3K_2) \), \( PSR_{\text{path7}} = (g_{mN2} - g_{mN1})/(g_{mN2} + 1/r_{0N1}) = 0 \), the PSRR of proposed VR is \( PSR_{\text{ref}} = PSR_C \times PSR_{\text{path7}} + PSR_A \times PSR_{\text{path8}} \approx PSR_A \times PSR_{\text{path8}} \) then

\[
PSR_{\text{ref}} = \frac{1}{g_{mMP2}r_{0MP2}} - \frac{1}{T_{\text{loop-B}}} \times \frac{1}{(3 + 2K_2)}. \tag{9}
\]

According to Eq. (9), by setting \( 1/T_{\text{loop-B}} \) closed to \( 1/g_{mMP2}r_{0MP2} \), the multiplier can contribute nearly −70 dB to PSRR of VR. At the meanwhile, the multiplier \( 1/(3 + 2K_2) \) will further enhance the PSRR up to −80 dB. As shown in Fig. 3(c), with the increasing of \( K_2 \), the PSRR of VR will be higher.
3 Verification results and discussions

The proposed resistorless low-power VR in Fig. 2 is validated by simulation in 0.35-µm CMOS process. As shown in Fig. 3(a), at the temperature range of −25°C to 75°C, the average value of Vref is 281.7 mV. It depends on the difference between \( V_{TH0}(0K) \) and \( V_{TH1}(0K) \), defined as threshold voltage at 0K temperature point, which is about 570 mV. And Vref varies 140 µV with a TC of 4.9 ppm/°C. The current consumption of proposed VR at 900 mV supply voltage is shown in Fig. 3(b), where the current consumption at 25°C is just 10.9 nA. Additionally, Fig. 3(c) demonstrates the PSRR is \(-82\) dB at DC and \(-62\) dB at 1 kHz without any filter capacitor. The Line regulation (LR) result is shown in Fig. 3(d), the minimum supply voltage is 850 mV.

Table I summarizes the characteristics of the proposed VR and compares it with some previously reported resistorless VRs.

|                  | This work | [2] | [5] | [7] | [9] |
|------------------|-----------|-----|-----|-----|-----|
| process (µm)     | 0.35      | 0.35| 0.18| 0.18| 0.18|
| min VDD (V)      | 0.85      | 1.4 | 1.1 | 0.15| 1.8 |
| Temp (°C)        | −25–75    | −20–100| −15–140| 0–120| −25–120|
| Vref (mV)        | 281.7     | 858 | 755 | 17.69| 1204|
| TC (ppm/°C)      | 4.9       | 12.4 | 34 | 1462.4| 4.6 |
| Power (nW)       | 9.8       | 126000| 4.6 | 0.026| 31050|
| PSRR (dB)        | −82       | −68 | −9 | −64 | −51 |
| Area (mm²)       | 0.032     | 1.2 | 0.0598 | 0.0012| 0.0022|

3 Conclusions

A low-TC high-PSRR VR is presented and implemented with a 0.35-µm CMOS process. The inherent temperature compensation is achieved by GSVD structure. Besides, the proposed PSRR enhancement techniques can greatly improve the capability of noise suppression. The simulation results show that the TC is 4.9 ppm/°C in the temperature range of −25°C to 75°C with a power consume of 9.8 nW and the PSRR is up to −82 dB.

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