Clock Network Synthesis Based on Clock Mesh Technology

Yi Tao\textsuperscript{1,*}, Yu Jing Li\textsuperscript{2,b} and Wu Yang\textsuperscript{3,c}

\textsuperscript{1} Sichuan Institute of Solid State Circuits, Chongqing, P.R. China
\textsuperscript{2} Sichuan Institute of Solid State Circuits, Chongqing, P.R. China
\textsuperscript{3} Sichuan Institute of Solid State Circuits, Chongqing, P.R. China
\textsuperscript{a} ty_sisc@163.com, \textsuperscript{b} lyj_123@qq.com, \textsuperscript{c} WuYang_cq@163.com

Abstract: Circuit Synthesis plays a very important role among all the digital integrated circuit backend design flow. For the purpose of reducing the clocks latency in the design flow, based on the traditional clock network synthesis method, this paper demonstrates a clock synthesis method, which based on clock mesh technology using IC Compiler tool.

1. Background
Circuit Synthesis is a physical implementation phase in digital circuit backend design process, it played a crucial role, because the digital circuit works based on its clocks, so the quality of clock tree make the determination of the speed and power of the digital circuit design. Designer pay much care on the clock network synthesis process, they want the clocks tress be faster, shorter, more balanced.

Now with the reason that digital circuit is more complex and transistors varies a lot in deep sub-silicon process, building a high quality clock tree can be a challenging job to do.

2. Clock Mesh Structure based Clock Tree
Clock meshes are a lot shorted grids of metal that are driven by many clock drivers. The purpose of a clock mesh is to reduce clock skew in both nominal designs and designs across variations such as on-chip variation, chip-to-chip variation, and local power fluctuations. A clock mesh reduces skew variation mainly by shorting the outputs of many clock drivers. The network of drivers from the clock port to the mesh driver inputs is called the premesh tree. The network of shorted clock driver outputs is called the mesh. The structure of clock mesh is shown as below:

Fig. 1 Clock Mesh Structure
2.1. *The Clock Mesh Flow*

The clock mesh flow describes the steps that we processed in IC Compiler tool as below:

![Clock Mesh Flow Diagram](image)

**Fig. 2** Clock Mesh Flow

2.2. *Build Clock Mesh Tree*

First we split the clock signal by using: `split_clock_net -objects {clk} -gate_sizing`, then we reconnect clock signal with the disconnect clock port by using: `adjust_premesh_connection -root clk`, then we create clock mesh tree by using: `create_clock_mesh -load clk -net clk` as follow:

![Clock Mesh Tree](image)

**Fig. 3** Clock Mesh Tree

2.3. *Adding Clock Mesh Drivers*

Clock mesh drivers directly drive the clock mesh loads that include the mesh straps we created before, the loads directly driven by the mesh, and the comb routes used to connect the drivers and loads to the mesh. You can use the add clock drivers command either to add only the clock mesh drivers or to create
a hierarchy of drivers that drive the mesh drivers, starting from the root of the clock tree, highlight cells are the clock mesh drivers which are shown as below:

2.4. Routing Mesh Nets

After you create the mesh drivers and premesh trees, use the router to connect the outputs of the mesh drivers to the nearest clock mesh and the mesh loads to the nearest mesh straps. By default, the tool uses Zroute as the default router as below:

2.5. Analyzing Clock Mesh Circuits

We implement the Clock Mesh Circuit based on SMIC40nm process, and also build a traditional clock tree by using IC Compiler which was Synopsys Company EDA Tool, then we compare the clock tree quality of two different clock tree structures as below:

| Table1  Comparison of Traditional Clock Tree and Clock Mesh |
|-----------------|------------------|
|                  | Traditional Clock Tree | Clock Mesh Tree |
| Clock Skew       | 10.8ps            | 6.5 ps          |
| Longest Clock Path | 100.2 ps          | 80.9 ps         |
| Clock Buffes Number | 680               | 820             |
3. Summary
This paper introduces a clock tree implement methodology based on clock mesh structure, explains the concept of clock mesh trees and also showed how to use the IC Compiler to implement the clock mesh design flow. The comparison of traditional clock tree and clock mesh structure shows that a clock tree based on clock mesh structure has advantage on clock skew and also the length of longest clock path with more clock buffers area, which is good for high performance design in sub-deep process node.

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