Optimization of power output in planar thermoelectric microgenerators based on Si nanowires

C. Calaza 1, I. Donmez 1, M. Salleras 1, G. Gadea 2, J. D. Santos 2, A. Morata 2, A. Tarancón 2 and L. Fonseca 1

1 IMB-CNM, CSIC, Campus UAB, Bellaterra, 08193, Barcelona, SPAIN
2 Catalonia Institute for Energy Research (IREC), 08930, Barcelona, SPAIN

carlos.calaza@imb-cnm.csic.es

Abstract. This work reports the efforts to optimize the output power achieved with all-silicon thermoelectric microgenerators based on MEMS fabrication technology and silicon nanowires as active material. Recent improvements introduced in both the fabrication process and the device design are described, and a set of experimental results obtained with both device types (new vs. old design/process) are provided to assess the impact of the different modifications on thermal and electrical performance, as well as in the overall harvested power.

1. Introduction
The all-silicon thermoelectric microgenerators used in this work are based on an evolution of the silicon microplatforms reported [1], with low thermal conductivity supports for the suspended parts. The Si NW arrays used as active material have been integrated on these platforms using a bottom-up Si NW growth process formerly developed [2], after adapting process parameters to new structures. Modifications of device design and fabrication process sequence are projected to overcome the critical issues affecting performance that were identified in the 1st generation of Si platforms [3].

2. Device optimization
The fabrication process sequence has been rearranged to improve the production yield. After test of a number of feasible orders for the micromachining steps the sequence in Table 1 has been adopted. Starting from SOI wafers with a 15 μm thick doped device layer (0.1 Ω·cm) (<110> surface and flat aligned with vertical <111> planes) and a 500 μm thick handle wafer the microplatforms were created using a new photolithographic mask set with five levels.

A new zigzag arrangement for the low thermal conductivity metal supports has been implemented allowing arbitrarily long membranes without device parts misalignment (Figure 1). This new design provides lower internal resistances due to increased metal/window area ratio. Membranes are released with a 30 min. KOH etch step, while <111> aligned structures for Si NW arrays are preserved. The area covered by the Si3N4 film has been extended to prevent the KOH of coming into contact with the <110> Si surface during the membrane release. This Si3N4 film is patterned to perform a local B implantation on the Si-metal interface regions, which is intended to ensure the contact ohmic behavior after a thermal treatment.
Table 1. Fabrication process sequence.

| Top side                          |
|----------------------------------|
| LPCVD Si$_3$N$_4$ deposition and RIE etch. Patterning with mask #1. |
| B implantation, thermal annealing for activation and SiO$_2$ etch. |
| Metal deposition (Ti/W) and lift-off. Patterning with mask #2. |
| RTA for silicide formation in contact interface. |
| PECVD SiO$_2$ passivation deposition and partial SiO$_2$ RIE etch on pad areas. Patterning with mask #3. |
| PECVD SiO$_2$ and LPCVD Si$_3$N$_4$ RIE etch to expose top Si surface. Patterning with mask #4. |

| Bottom side                      |
|----------------------------------|
| Thick PECVD SiO$_2$ deposition and PECVD SiO$_2$ and LPCVD Si$_3$N$_4$ RIE etch to expose bottom Si surface. Patterning with mask #5. |
| DRIE of the 500 $\mu$m thick Si handle wafer (using protection photoresist on top side). |
| After chip dicing                |
| KOH etch to define top silicon structures and release the metal supporting membranes. |
| BOX removal with HF vapours.     |

Figure 1. New arrangement for the low thermal conductivity membrane supports. a) Dielectric openings are aligned with Si substrate fast etching planes to allow Si under etch during KOH process. b) Number and width of metal lines is maximized to improve the internal resistance. c) Si platform and bars defining NW trenches are aligned with $<111>$ planes to endure this etch process.

The microplatforms obtained with the fabrication process flow described in Table 1 and the new mask set have been characterized (before Si NWs integration) in order to validate the positive impact of the process and design changes in performance parameters.

2.1. Thermal isolation
The impact of the new dielectric membrane used as support for the metal interconnections on platform thermal isolation has been assessed by contrasting the total platform-to-rim thermal conductance of these new devices vs. a reference one using the previous support type (silicon beams). Figure 2 shows the power dissipated in a test element (heater) vs. temperature increase reached in the isolated platform (estimated from heater resistance change after calibration), for three devices with the same active area and different beam or membrane lengths. Despite reduced length (100 $\mu$m membrane vs. 200 $\mu$m beams), thermal isolation achieved with membranes outstrips that of previous silicon bridge supports.

Total platform-to-rim thermal conductance decreases from 1.99 to 1.26 mW/K, pointing out that bridge conductance in old designs accounts for more than one third of total thermal losses, turning into
a significant limiting factor for thermoelectric performance. Negligible change in thermal conductance observed for devices with 100 and 200 μm membrane lengths (i.e. halved membrane contribution) confirms that in new designs the main contributions are linked to the surrounding air and the silicon bars that define the NWs trenches. Thus, longer membranes are not advised as no further benefit is expected in terms of thermal isolation and a major impact can be anticipated on internal resistance.

**Figure 2.** Comparison of platform-to-rim thermal conductance for three samples, a reference device with Si beams (200 μm length): 1.99 mW/K and two devices with Si₃N₄ membranes (100μm and 200μm length): 1.26 mW/K.

2.2. Internal resistance

The impact of process changes used to improve the Si-metal interface was assessed by measuring the contact resistance with a TLM (transmission line method) test structure. Two samples using a 20/200 nm Ti/W stack or a 230 nm W layer as metallization were considered. The TiW sample performed a previous B shallow implantation in contact regions (5e15 at/cm² and 50keV) and both have undergone a rapid thermal annealing at 700°C for 30s to promote the silicide formation.

**Figure 3.** TLM measurement for two samples using 20/200 nm Ti/W and 230 nm W metal stacks, respectively. A rapid thermal annealing at 700°C for 30s was performed in both samples and a previous B implantation (5e15 at/cm² and 50keV) was executed in Ti/W sample.

Both metallizations provide ohmic behavior but TLM results in Figure 3 show that Ti/W improves the contact resistance by almost a factor 4 for pads with equal area. In addition, the adhesion problems observed for samples with pure W layers after passivation removal are prevented with the Ti addition.
3. Power generation

Performance enhancement attained with new microplatforms has been studied using a device with four structures (T1-T4) with a different number of 10 \( \mu \)m wide trenches between hot and cold parts, which allow the growth of silicon NWs with different effective lengths using a single batch process to create 10 \( \mu \)m long P-type silicon NWs (linking the 3 \( \mu \)m wide Si bars between trenches).

After NWs integration, the device under test was packaged to endure high temperatures and placed on a hotplate to evaluate its response in different operating conditions established with a temperature controller. The voltage generated by the thermocouple (Figure 4.a) surges with the increase of the effective NWs length due to a better thermal isolation between the hot and cold parts, which provides a higher temperature difference for each hotplate condition. Nevertheless, the low voltages measured (close to Seebeck coefficient of Si NWs) suggest that thermal gradient across the NWs is in the 1-5°C range. Therefore, progress is still required to integrate a heat exchanger element in device structure.

![Figure 4. a) Thermoelectric voltage generated with devices using the new platform design. Impact of the effective NWs length (1 to 4 trenches). b) Power curves for T3 devices (three NWs trenches) at different temperatures (50 to 300°C, in 50°C steps) using the new optimized platform (dotted line) or the previous design with Si beams (inset).](image)

Despite the limited temperature gradients the increase in generated voltage with the introduction of the membrane supports is higher than 60% when peer T3 devices (three NW trenches) are compared (540\( \mu \)V with beam supports vs. 880\( \mu \)V with new membrane supports, both @350°C). The advance in terms of power is even higher due to the additional enhancement of internal resistance, which has been reduced by a factor 10 (from \( \approx \)50 \( \Omega \) to \( \approx \)5 \( \Omega \)) through metal mask redesign and Si-W electrical contact enhancement. The comparison of power curves obtained with peer T3 devices (three NW trenches, Figure 4.b) shows an improvement of more than one order of magnitude in power levels, from 500 pW obtained with previous platforms [3] to 10 nW achieved with this new optimized version.

Acknowledgments

This work was supported by FP7-NMP-2013-SMALL-7, SiNERGY (Silicon Friendly Materials and Device Solutions for Microenergy Applications), Contract n. 604169.

References

[1] C. Calaza, L. Fonseca, M. Salleras, I. Donmez, A. Tarancón, A. Morata, J. D. Santos, G. Gadea, Journal of Electronic Materials 45 (2016), pp. 1689-1694.
[2] G. Gadea, A. Morata, J.D. Santos, D. Dávila, C. Calaza, M. Salleras, L. Fonseca, A. Tarancón Nanotechnology 26 (19):195302 (2015).
[3] D. Dávila, A. Tarancón, C. Calaza, M. Salleras, M. Fernández-Regúlez, A. San Paulo, L. Fonseca, Nanoenergy 1 (2012), pp. 812-819.