A PWM based readout circuit for optical sensors with adaptive frequency control

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Abstract: This paper proposes a pulse-width modulation-based readout circuit for optical sensors which adopts adaptive frequency control technique to enhance input dynamic range of current sensing systems. The proposed readout circuit is designed and fabricated using a 65 nm CMOS process. The readout IC achieves 100 dB of dynamic range in current sensing system by adaptively controlling the frequency of operating clock.

Keywords: pulse-width modulation, current to PWM converter, optical sensor, photodiode, trans-impedance amplifier, CMOS

Classification: Integrated circuits

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1 Introduction

In a fourth industry revolution, sensors for Internet of Things (IoT) systems are expected to be compact, low-cost, low-power. Among various sensing methods, an optical method using a photodiode is one of the rapidly growing methods due to high speed, small area and its wide range of applications from home applications to healthcare, environment and industrial monitoring [1, 2, 3, 4].

Conventional readout circuit for optical sensors typically utilizes an analog to digital converter (ADC) to quantize the output voltage of a trans-impedance amplifier (TIA), however, there are several disadvantages. For example, a capacitive successive approximation ADC having relative low-power characteristic occupies large area overhead, and a high-resolution sigma-delta ADC consumes significant power [5, 6, 7, 8, 9].

Pulse-width modulation (PWM) is another method for analog quantization, which converts the input current of photodiode to a pulse width signal [2, 3, 4]. Simple capacitive trans-impedance amplifier (CTIA) with digital n-bit counter can

Fig. 1. Block diagrams of (a) the PWM-based readout circuit for optical sensor and (b) the proposed PWM-based readout circuit with adaptive frequency controller.
convert the photocurrent into a n-bit digital signals instead of the ADC. Complexity, power consumption, and effect of environmental noise due to digital on/off nature of the system can be reduced. In the PWM-based readout circuit, current detection range is determined by input capacitance and operating frequency. The input capacitance (C_{IN}) includes photodiode parasitic capacitance (C_{PD}), gate capacitance of the CTIA (C_G), and additional capacitor of the input node (C_{ADD}), as shown in Fig. 1(a). The C_{ADD} is a design parameter, however, the range of C_{IN} we can design is limited by C_{PD} and C_G. The operating frequency of clock signal is a design parameter. To detect lower photocurrent, sufficient clock period is needed, that is, PWM readout circuit having lower operating frequency can detect lower photocurrent. According to the application, the structure, and the production defects of the sensor, the detection range can vary. In this paper, we propose a PWM-based readout circuit for optical sensor with adaptive frequency control. By monitoring the PWM signal, the operating frequency can be adaptively adjusted according to the range of photocurrent.

2 Readout circuit design

Fig. 1(b) shows the block diagram of the proposed readout integrated circuit with adaptive frequency control. The readout IC consists of CTIA, PWM generator, N-bit counter, ring oscillator, and frequency controller.

The CTIA converts a photocurrent into voltage, and the PWM generator makes this analog signal into PWM signal. And this PWM signal is changed into digital codes by N-bit counter. The ring oscillator generates a main clock. The clock signals of the counter and the PWM generator have to be synchronized to properly operate, thus they are operated by divided clocks from the ring oscillator. The counter is operated by CLK_{CNT} which is divided by 2 from the main clock, while the clock of the PWM generator, CLK_{PWM}, is divided by 2^{10}. The frequency controller monitors CLK_{PWM} and the PWM signal in real time. The frequency controller generates 4-bit codes (D_{CTRL}(3:0)) which control the tail current of the ring oscillator by comparing the PWM signal with CLK_{PWM}.

Fig. 2(a) is the block diagram of the CTIA and the PWM generator. It consists of a capacitive TIA, a comparator, and a digital logic. Fig. 2(b) is the timing diagram that summarizes the operation of the current-to-PWM converter for two output conditions of the optical sensor. Current-to-PWM converter is basically operated by CLK_{PWM}. When CLK_{PWM} is HIGH, it enters a conversion cycle to convert I_{PD} of the optical sensor into the PWM signal. When CLK_{PWM} is LOW, a reset cycle, the output of the CTIA, V_{TIA}(t), is reset to common-mode voltage, V_{CM} and the PWM signal becomes LOW.

In conversion cycle, V_{TIA}(t) decreases from V_{CM} to V_{ref} with time and its slope is proportional to I_{PD}. When V_{TIA}(t) reaches to V_{ref} during conversion cycle, PWM signal becomes LOW, as shown in Fig. 2(b) case-1. If I_{PD} is too small or CLK_{PWM} is too fast, V_{TIA}(t) cannot reach to V_{ref}, as shown in Fig. 2(b) case-2. Then the PWM signal maintains HIGH state during conversion cycle, and it means the PWM signal same to CLK_{PWM} signal. Eq. (1) summarizes the pulse width (T_{PW}) of the PWM signal in the case of T_{PW} is less than half of period of CLK_{PWM}.
Photocurrent of optical sensor can vary according to ambient environment, sensor conditions according to its applications. And it causes significant problem to a dynamic range of the PWM-based readout circuit. To adjust this problem, adaptive frequency control scheme is proposed. Fig. 3(a) is the operation process of the proposed frequency control technique. When the PWM signal is generated, the frequency controller compares the PWM signal with CLKPWM. The frequency controller calculates the difference between the two signals. If the difference occurs, the frequency of CLKPWM is maintained. Conversely, when there is no difference between CLKPWM and the PWM signals, the frequency of CLK is lowered every cycle of CLKPWM to track the frequency that can be converted into the PWM signal.

Fig. 3(b) is the block diagram of the frequency controller. The frequency controller consists of a XOR gate, a D-flipflop (DFF), a 2:1 multiplexer (MUX), a 4-bit counter and a 4-bit register. The XOR gate senses CLKPWM and the PWM signals in real time and outputs the difference of them. The DFF stores $D_{\text{sub}}$ of the XOR gate every falling edge of the PWM signal. The non-inverting (EN) and

$$T_{PW} = \frac{C_f \cdot (V_{CM} - V_{ref})}{I_{PD}}$$

(1)
inverting (EN') output of DFF are respectively used as the selection signal of the MUX and the enable signal of the counter. The MUX selectively supplies CLK_{PWM} or VDD as the clock signal of the register according to EN. The 4-bit counter operates when the PWM signal is saturated with CLK_{PWM}. The 4-bit register stores the output of the counter, and the output makes the change of the oscillator frequency by controlling the bias voltage of ring oscillator, as shown in Fig. 3(c). Fig. 3(d) shows the post-layout simulation results of the frequency controller. When the PWM signal equals to CLK_{PWM}, the frequency controller lowers the bias voltage of the ring oscillator. And when the difference between PWM and CLK_{PWM} occurs, the EN goes to HIGH and makes the frequency controller be disable.
The PWM-based readout circuit with the frequency controller was designed using 65 nm CMOS technology and measured with the commercial photodiode having $C_{PD}$ of 28 pF and $I_{PD}$ from 100 pA to 1 uA [10]. Fig. 4(a) and 4(b) show the chip microphotography and measurement setup of the PWM-based readout IC, respectively. The proposed IC occupies 1.12 mm$^2$ including bonding pads and an active area of less than 0.04 mm$^2$.

For efficient photocurrent control, voltage-to-current converter with a variable resistor is implemented on evaluation board. And the PWM signal and digital codes of counter are observed in sampling oscilloscope and logic analyzer, respectively. As shown in Fig. 1(b), CLK$^{PWM}$ and CLK$^{CNT}$ (clock signal for counter) are synchronized. Thus, the ratio of pulse width compared with the period of CLK$^{PWM}$ is more important information than its absolute value. PWM ratio is defined as Eq. (2). PWM ratio has a value between 0% and 50% and proportional to the frequency of CLK$^{PWM}$. If specific $I_{PD}$ indicates 20% of PWM ratio for 10 kHz of CLK$^{PWM}$, for example, then it has 40% of PWM ratio for 20 kHz of CLK$^{PWM}$. Also, final N-bit outputs of the counter for two cases are ideally equal, however,
there can be 1-bit difference due to quantization errors in the procedure of PWM signal to digital conversion.

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\text{PWM Ratio} \ (\%) = \frac{\text{Pulse Width of the PWM Signal}}{\text{Period of } \text{CLK}_\text{PWM}} \times 100
\]  

Fig. 5(a) and 5(b) show the PWM signal with respect to IPD with 1 MHz and 83.33 kHz of CLKPWM. For 10 nA of IPD, each result indicates 93.99% and 7.84%
of PWM ratio. And this difference is almost same to difference of CLK_{PWM} frequencies. Fig. 5(c) shows the frequency of CLK_{PWM} which was adaptively changed by the frequency controller with respect to IPD. From 10 uA to 100 pA, CLK_{PWM} can be adjusted from 5 MHz to 83.33 kHz.

4 Conclusions

A PWM-based readout circuit for optical sensors was studied here. The proposed frequency control technique enables the readout circuit to have wide dynamic photocurrent range. As a result, the proposed readout circuit can be expected to operate generally for various applications, which have various photocurrent output and parasitic capacitance.

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