Upscaling High-Quality CVD Graphene Devices to 100 Micron-Scale and Beyond

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We describe a method for transferring ultra large-scale CVD-grown graphene sheets. These samples can be fabricated as large as several cm$^2$ and are characterized by magneto-transport measurements on SiO$_2$ substrates. The process we have developed is highly effective and limits damage to the graphene all the way through metal liftoff, as shown in carrier mobility measurements and the observation of the quantum Hall effect. The charge-neutral point is shown to move drastically to near-zero gate voltage after a 2-step post-fabrication annealing process, which also allows for greatly diminished hysteresis.

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Graphene is well-known for its desirable electrical properties, and with all of the intense focus on research in the material, new applications are being constantly discovered. While graphene is known to have its best electrical properties when it is single-crystalline and suspended, those attributes are currently not feasible for mass-produced devices. There have been very exciting developments related to improving non-suspended graphene’s mobility on more exotic substrates such as hBN, as well as improving the chemical vapor deposition (CVD) growth process for producing better quality devices with large grain sizes. However, these developments are currently difficult to scale up and automate.

On the other hand, CVD-grown graphene is still the best way to repeatably produce large areas of monolayer graphene, and SiO$_2$ is a well-known substrate that is already integrated into many processes from semiconductor physics to MEMS and beyond. Previous work has shown how to transfer large areas of CVD-grown graphene onto arbitrary substrates and remove contaminants. However, previous CVD-grown graphene on SiO$_2$ devices do not combine the desirable properties of high enough quality electrical characteristics to display the quantum Hall effect (QHE), a charge neutral point (CNP) near zero gate voltage, and a large device size, with typical finished devices being on the order of 10 $\mu$m. Large-scale integration of easily manufactured, high-quality graphene devices is desirable in many different applications, such as graphene transistors, broadband optical modulators and THz antennas.

Challenges arise when fabricating high-quality CVD-grown graphene devices, primarily due to contaminants of all kinds easily attaching to graphene. With each step, much care must be taken to remove any existing organic or inorganic contaminants on the graphene as well as prevent new contaminants from being attached. This paper presents a fabrication method that produces devices with CVD-grown graphene on SiO$_2$ that are hundreds of microns in size and display the QHE.

A sheet of copper is supplied with CVD-grown graphene on only one side. Other sources of CVD graphene on copper typically have graphene on both sides of the foil, and in that case an oxygen plasma can be used to remove graphene from one side. A wet transfer process is used to place the graphene on the substrate, with cleaning steps to remove inorganic and organic contaminants from the bottom of the graphene before transfer. These steps are similar to the method detailed by Liang et al., which itself includes a “modified RCA clean” process.

It is important to be sure that all contaminants from the graphene are removed, as any resist residues can act as dopants and scattering centers to degrade electrical performance, as well as increase contact resistance. Acetone or other common solvents are not sufficient to remove residues from resists such as poly(methyl methacrylate) (PMMA). A common technique to clean small graphene devices is to use current annealing, especially when the graphene is suspended, as it can effectively evaporate many contaminants and allow the graphene to self-heal. Other cleaning methods include mechanical cleaning with atomic force microscopy, exposure to ultra-violet light, ozone treatment, and annealing in vacuum or with gas flow. In the process detailed in this paper, the graphene is cleaned before transfer to a clean substrate, and then cleaned again after fabrication by a 2-step thermal annealing process.

The size of the graphene/copper foil pieces used here is $1\text{ cm} \times 1\text{ cm}$, however, the process can easily be upscaled to sizes of several cm$^2$. PMMA with a molecular weight of 950K is spun onto the graphene/copper foil and dried by air (Fig. 1(a)). A solution of Fe(NO$_3$)$_3$ is prepared with
5 g/100 ml of DI water and the PMMA/graphene/copper stack is placed to float in the solution with the copper side down, then left for at least 10 hours for the copper to etch away (Fig. 1(b)). Subsequently, the graphene stack is transferred to clean DI water at least twice, waiting 5 minutes after each transfer. Similarly to Liang et al., the RCA clean step referred to as Standard Clean 2 is next, with a HCl/H₂O₂/H₂O solution prepared in a 1:1:20 ratio. Once again, the stack is placed on this solution to clean inorganic contaminants not removed by the Fe(NO₃)₃, such as oxides, for 15 minutes (Fig. 1(c)). The stack is then once again transferred to clean DI water at least twice for 5 minutes each. Finally, the RCA clean step known as Standard Clean 1 (SC-1) is performed with a NH₄OH/H₂O₂/H₂O solution in a 1:1:100 ratio for 5 minutes (Fig. 1(d)) to remove organic contaminants. The cleaning time and chemical concentrations of H₂O₂ and NH₄OH in SC-1 are lower than reported in the modified RCA clean process in order to avoid bubble formation. Bubbles that get under the graphene stack can lead to the graphene tearing and are very difficult to remove before transfer. After the SC-1 step is complete, the graphene is again transferred to clean beakers of DI-water twice, waiting 5 minutes after each transfer.

Wafers of thermally grown SiO₂ on p-doped Si are prepared by carefully cutting into appropriately sized pieces with a diamond scribe. Any contaminants are cleaned off with sonication in acetone and then isopropanol before the wafers are dried with a N₂ gun. The SiO₂ is then treated with O₂ plasma in order to make the surface more hydrophilic, so the graphene will stick to it more readily and minimize breakage. Within one minute of the substrate’s O₂ plasma exposure, the PMMA/graphene stack is scooped up and it is all dried in an oven set to 150 °C for 15 minutes (Fig. 1(e) and (f)). Finally, the PMMA is removed with acetic acid (Fig. 1(g)), which more cleanly removes PMMA residue than acetone, while at the same time not attacking either the graphene or the SiO₂ substrate. At this point, the graphene is cleanly transferred to the substrate with minimal cracks or tears (Fig. 1(h)), with most defects existing previous to the transfer process. Many other defects can be explained by bumps, folds, or other surface features in the copper foil that the graphene was grown on. These features make it much less likely for the graphene to transfer tear-free, making it very important to keep the copper foil as flat as possible. As shown in Fig. 2(a) and 2(b), Raman spectra at 532 nm were taken in multiple locations to verify reproducibility of the measurement and uniformity of the graphene monolayer.

Once the graphene is on the target substrate, it must still have metal contacts deposited as well as be patterned into whatever shape is desired. Both of these steps must ideally be done without damaging or contaminating the graphene any more than absolutely necessary. The contacts are defined using photolithography, with a layer of Microchem LOR 5A used between the photoresist and graphene. This bi-layer stack tends to remove much more cleanly than photoresist alone and after removal can result in high-quality devices. In our observation, it also results in a higher final yield of usable devices due to less undesired graphene removal during liftoff. Without a protective layer of LOR, negative photoresists tended to result in much worse yield than positive resists, possibly due to crosslinking of polymer chains during exposure. After exposure and development, a 5 nm layer of Ni is deposited by physical vapor deposition as an adhesion protective layer of LOR, negative photoresists tended to result in much worse yield than positive resists, possibly due to crosslinking of polymer chains during exposure. After exposure and development, a 5 nm layer of Ni is deposited by physical vapor deposition as an adhesion layer, followed by 50 nm of Au (Fig. 1(i)). Liftoff is then performed in a two-phase process. First, the sample is soaked in a bath of acetone, which removes the photoresist and lifts off the excess metal. Since an ultrasonic bath will damage the graphene, excess metal is instead gently removed by squeezing a pipette to agitate the acetone. Second, after all excess metal is removed, the LOR layer is removed by being soaked in Microposit Remover 1165 for five minutes. Finally, the sample is rinsed with isopropanol and dried with a N₂ gun. The result is shown in Fig. 1(j).

For this sample, excess graphene is removed by using photolithography to cover the areas of graphene to be
FIG. 2. (a) Optical microscopy image of a large clean area of graphene (dark purple) on a SiO$_2$ substrate (light purple). Inset: Picture of a 1 cm $\times$ 1 cm SiO$_2$ wafer with CVD graphene on top (dark blue). (b) Raman spectra with a 532 nm laser taken at the colored and numbered spots shown in (a), displayed with an artificial offset for clarity. The defect peak D is very small in all three measurements, which speaks for a high quality of graphene, and the G$^*$ peak is in the expected location. Also, due to the relative height of the G and 2D peaks, which is about one third, we can confirm that we see a monolayer of graphene. (c) Optical microscopy image of a 200 $\mu$m long and 22 $\mu$m wide graphene strip (light blue) on an SiO$_2$ substrate (dark blue) with a contact layout typical for Hall measurements. (Graphene contrast increased for visual effect in (a) and (c)).

protected from O$_2$ plasma. The sample is then chemically cleaned for the final time with acetone and isopropanol, then dried with N$_2$. Fig. 1(k) and 2(c) show the final result.

The sample is then mounted in a probe with air pumped out and replaced with a small quantity of He as an exchange gas. The longitudinal resistance is measured over a range of applied gate voltages at a temperature of 4.2 K at zero magnetic field. The sample is annealed under vacuum for 16 hours at 350 °C to remove all water, including water trapped between the graphene and substrate. The sample is then removed from vacuum and quickly mounted in a probe, and once again annealed in a tube oven under vacuum (Fig. 1(l)) at 140 °C for 72 hours to remove any water absorbed from the atmosphere during mounting. During this time, the 2-point resistance of the Hall bar is observed to steadily increase from approximately 25 kΩ to a new maximum of 57 kΩ.

Fig. 3 shows the increase in peak longitudinal resistance along with a dramatic shift of the charge neutral point (CNP) from $V_g$=27 V to −4 V before and after annealing, respectively, which is evident of the concentration of charged impurities being significantly reduced. The large peak shift is indicative of the removal of a majority of p-type dopants such as water and the settling of the CNP at a negative gate voltage may be due to doping by the metal contacts or contact doping by SiO$_2$ and any contaminants trapped between the graphene and metal during processing. When the sample is re-exposed to atmosphere, the CNP drifts toward the prebake value, though performing the baking process once more moves the CNP back to near-zero gate voltage. Thus, a capping layer is necessary to prevent adsorbates from altering the electrical characteristics of the graphene when exposed to air.

The CNP changes by at most 0.1 V, depending on the direction the gate voltage is swept. When there is still a significant amount of water on the substrate, this hysteresis can easily be on the order of a few or even tens of volts. This effect is typical of graphene on SiO$_2$ and the relatively low hysteresis seen in this sample implies that most of the water has been removed by the previous annealing step.

The magnetic field is then set to 8 T and the gate voltage is scanned once more at 4.2 K. Multiple quantum Hall levels for monolayer graphene were seen, as shown in Fig. 4. Clear plateaux for the Hall resistance, $R_{xy}$, at filling factors of $\nu = \pm 4(n + 1/2)$ and Landau level index $n = 0, 1, ...$ are seen with corresponding drops in the longitudinal resistance, $R_{xx}$. Further magnetoresist-
These measurements show that the fabrication method and contacts, with a distance between the longitudinal contacts of 100 μm.

In summary, we have presented a procedure that results in clean large-area graphene devices of high quality on a SiO2 substrate. The 2-step liftoff aids greatly in unbroken large graphene structures, and the 2-step annealing process as well as other cleaning steps result in a realization of near-ideal mobilities and a low hysteresis with observation of quantum Hall levels. Hence, our processing approach now enables large-scale integration of high-quality graphene layers in devices such as THz-emitters, thermo-power couplers, and possibly flexible thin-film sensors.

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FIG. 4. The longitudinal (solid red line) and Hall resistance (dashed blue line) versus the gate voltage \( V_g \) at fixed magnetic field \( B = 8 \) T measured at 4.2 K, obtained through a standard 4-point-measurement approach, show multiple quantum Hall levels with filling factors labeled. Inset: Schematic of the graphene strip and contacts, with a distance between the longitudinal contacts of 100 μm.

FIG. 5. The charge carrier density (solid red line) and mobility (dashed blue line) versus the gate voltage \( V_g \) at 4.2 K after the final annealing step. The values were obtained by performing magnetoresistance measurements at the displayed values for \( V_g \). Points are connected by B-spline curves. The charge carrier density is linear with respect to gate voltage away from the CNP, which implies the gate oxide provides the dominant capacitive effect which is expected due to the oxide thickness. The rounding of the charge carrier density graph near the CNP is due to charged electron/hole puddles induced by charged impurities, including those in the substrate.

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