BaM: A Case for Enabling Fine-grain High Throughput GPU-Orchestrated Access to Storage

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Abstract—Accelerators like Graphics Processing Units (GPUs) have been increasingly deployed in modern data centers because of their compute capabilities and memory bandwidth. These accelerators have traditionally relied on the “application host code” and the OS running on the CPU to orchestrate their accesses to the data storage devices. CPU orchestration of storage data accesses works well for classic GPU applications, like dense neural network training, where data access patterns are predefined, regular, dense, and independent of the data values, enabling the CPU to partition the storage data into coarse-grain chunks and coordinate the storage device accesses and data transfers to the accelerators. Unfortunately, such a CPU-centric strategy causes excessive CPU-GPU synchronization overhead and/or I/O traffic amplification, diminishing the effective storage bandwidth for emerging applications with fine-grain data-dependent access patterns like graph and data analytics, recommender systems, and graph neural networks. In this work, we make a case for enabling GPUs to orchestrate high-throughput, fine-grain accesses into NVMe Solid State Drives (SSDs) in a new system architecture called BaM. BaM mitigates I/O traffic amplification by enabling the GPU threads to read or write small amounts of data on-demand, as determined by the compute. We show that (1) the BaM infrastructure software running on GPUs can identify and communicate the fine-grain accesses at a sufficiently high rate to fully utilize the underlying storage devices, (2) even with consumer-grade SSDs, a BaM system can support application performance that is competitive against a much more expensive DRAM-only solution, and (3) the reduction in I/O amplification can yield significant performance benefit. These results are achieved by introducing high-throughput GPU data structures like queues and software caches that exploit the massive thread-level parallelism in GPUs to hide long latencies to the SSDs. We have built a prototype BaM system and evaluated its performance on several applications and datasets using different SSD types. The BaM prototype provides, on average, 0.92× and 1.72× end-to-end speed up for BFS and CC graph analytics workload with 4 Intel Optane SSD drives and up to 4.9× for data-analytics workload with one Optane SSD over state-of-the-art solution.

I. INTRODUCTION

There has been a phenomenal growth in GPU compute throughput in recent years. For example, as shown in Table\textsuperscript{I} the compute throughput of NVIDIA GPUs has increased by 452×, from G80 to A100 over a 13-year span \cite{10, 33}. As a result, the compute throughput of A100 (156 TF32 TFLOPS) is one to two orders of magnitude higher than its contemporary CPUs. Although the growth of memory bandwidth for GPUs is less dramatic, 18× as shown in Table\textsuperscript{I} the memory bandwidth of A100 (1.555 TB/s) is about an order of magnitude higher than its contemporary CPUs. A similar trend is also exhibited across AMD GPU generations. With such levels of compute throughput and memory bandwidth, GPUs have become popular compute devices for HPC applications and dominating compute devices for neural network training.

Emerging high-value data-center workloads such as graph and data analytics \cite{2, 36, 44, 52}, graph neural networks (GNNs) \cite{27, 31}, and recommender systems \cite{12, 26, 37, 38, 57} can potentially benefit from the compute throughput and memory bandwidth of GPUs. However, these workloads must work with massive data structures whose sizes typically range from tens of GBs to tens of TBs today and are expected to grow rapidly in the foreseeable future. As shown in Table\textsuperscript{I} the memory capacity of A100, in spite of a 53× increase from that of G80, is only at 80 GB, far smaller than the desired capacity required for these workloads.

An existing solution to the problem of insufficient GPU memory capacity for these massive data structures is to pool together the memory capacity of multiple GPUs to meet the capacity requirement \cite{12, 37, 39, 42, 57} and use fast shared memory interconnects like NVLink \cite{1} for the GPUs to access each other’s memory. The entire data structure is first sharded into the GPU memories. The computation then identifies and accesses the portions that are actually used. This approach has two drawbacks. First, the entire data structure needs to be moved from storage to the GPU memories even if only a portion might be accessed, which can add significantly to the application start-up latency. Second, the data structure size determines the number of GPUs required for the application, which may far exceed the compute resource requirement of the workload.

\begin{table}[h]
\centering
\begin{tabular}{|c|c|c|c|}
\hline
Metrics & G80 (2007) & A100 (2020) & A100/G80 \\
\hline
Compute Throughput & 0.345 SP TFLOPs & 156 TF32 TFLOPS & 452× \\
Memory Capacity & 1.5 GB (GDDR) & 80 GB (HBM) & 53× \\
Memory Bandwidth & 86.24 GB/s & 1553 GB/s & 18× \\
PCIe x16 Bandwidth & 6 GB/s (Gen2) & 32 GB/s (Gen4) & 4× \\
\hline
\end{tabular}
\caption{Dimensions of advances from NVIDIA G80 to A100}
\end{table}
Using the host memory, whose capacity typically ranges from 128GB to 2TB today, to help hold the shared data structure can reduce the total number of GPUs used \[36\]. We will refer to the use of host memory to extend the GPU memory capacity as the DRAM-only solution. Because multiple GPUs tend to share the same CPU and thus the host memory in data center servers, such DRAM-only solutions tend to add only a fraction of the host-memory size to each GPU’s memory capacity. For example, in NVIDIA DGX A100 systems, each host memory is shared by 8 GPUs. Thus, using host memory only extends the effective size of each GPU memory by \( \frac{1}{8} \) of the limited size of the host memory.

With their recent improvement in latency, throughput, cost, density, and endurance, Solid State Drives (SSDs) are becoming plausible candidates for realizing another level of the memory hierarchy. In this paper, we propose to enable the GPUs to use local and/or remote NVMe SSDs as extended GPU memory as a much lower cost and more scalable solution. We will compare the performance of the proposed approach to that of state-of-the-art solutions.

**Proposal:** We propose a novel system architecture called BaM (Big accelerator Memory). The goal of BaM’s design is to extend GPU memory capacity and enhance the effective storage access bandwidth while providing high-level abstractions for the GPU threads to easily make on-demand, fine-grain access to massive data structures in the extended memory hierarchy. In this paper, we present and evaluate the key components and the overall design of BaM that address three key technical challenges in efficiently supporting such on-demand storage accesses for accelerator applications.

First, the traditional memory-mapped file abstraction for on-demand accesses to storage data relies on the virtual address translation mechanism to determine the current location of the accessed data. However, applications that sparsely access massive data structures can incur excessive TLB misses and serialize the parallel accesses made by a large number of GPU threads \[29\]. BaM features a highly concurrent, high-throughput software cache as an alternative. The cache is highly parameterized and can be configured by developers to fit their applications’ needs. With the software cache, BaM does not rely on virtual memory address translation and thus does not suffer from serialization events like TLB misses.

Second, the memory-mapped file abstraction uses page fault handling mechanisms and traditional file system services running on the CPUs to perform required data movement. This CPU-centric model, where the CPU page-fault handler orchestrates data movement, suffers from the low-degree of CPU thread-level parallelism available to the OS page-fault handler. To address this issue, BaM provides a user-level library of highly concurrent NVMe submission/completion queues in GPU memory that enables GPU threads whose on-demand accesses miss from the software cache to make storage accesses in a high-throughput manner. This user-level approach incurs little software overhead for each storage access and supports a high-degree of thread-level parallelism.

Third, to avoid the high-cost of virtual address translation and page fault handlers, application programmers resort to partitioning the data into chunks and writing CPU code to orchestrate data movement according to the needs of each phase of compute. The high cost of CPU-GPU synchronization and traditional file system services push the developers to move data in large granularity. Unfortunately, because the data accesses in our target applications tend to be irregular and sparse, such large data movement granularity results in the transfer of many unused bytes between the SSDs and the CPU/GPU memories, a phenomenon known as I/O traffic amplification, or I/O amplification in short. As shown in prior work \[11\], \[36\], I/O amplification reduces the effective bandwidth of critical resources such as the PCIe links.

Table I shows that for A100, the storage data access bandwidth is limited to the PCIe Gen4 x16 bandwidth, which is 32 GB/s, only about 2% of the A100 memory bandwidth. Further deterioration of storage access bandwidth due to I/O amplification can translate into a significant loss of application performance. Using highly concurrent queues and multiple SSDs in BaM, we establish that the GPU can issue fine-grain I/O requests fast enough to fully utilize the SSD devices and significantly reduce the level of I/O amplification.

To our knowledge, BaM is the first accelerator-centric model where GPUs can identify and make accesses to data where it is stored, be it memory or storage, without relying on the CPU to orchestrate the accesses. While the user-level implementation of storage device queues raises security concerns for traditional monolithic server architectures, the recent data centers’ shift toward zero-trust security models and the corresponding security checking by NICs/DPUs have provided the new system framework for securing accelerator-centric storage access models like BaM.

We have built a prototype BaM system using off-the-shelf hardware components. Evaluation of the BaM prototype system on a variety of workloads with multiple datasets shows that BaM is either on-par with or even outperforms the state-of-the-art solutions.

Overall we make the following contributions. We

1. propose BaM, an accelerator-centric architecture in which GPU threads perform fine-grain, on-demand accesses to data where it is stored, be it memory or storage;
2. enable on-demand, high throughput fine-grain access to storage through highly concurrent I/O queues;
3. provide high-throughput, low-latency caching and software API for programmers to exploit locality and control data placement for their applications; and
4. propose and evaluate a proof-of-concept design for cost-effective scaling the memory capacity for accelerators.

We plan on open-sourcing the hardware and software optimization details so that anyone can build BaM systems.

## II. Background and Motivation

This section presents the important measurements that motivate the BaM design as well as the background information needed to understand the key aspects of a BaM system.
A. Software Overhead of CPU-Centric Approaches

On-demand storage access can be enabled in two ways: 
a) implicit and indirect, and b) explicit and direct. Implicit and indirect access approach can be enabled in CPU-centric model by extending the CPU memory-mapped file abstraction to GPU threads. Starting with the NVIDIA Pascal architecture, GPU drivers and programming model allow the GPU threads to implicitly access large virtual memory objects that may partly reside in the host memory using Unified Virtual Memory (UVM) abstraction \[19\]. Prior work shows that the UVM driver can be extended to interface with the file system layer to access storage when a page is part of a memory-mapped file and is missing from the GPU memory and the host memory \[24\].

The main advantage of this approach is that all storage accesses are simply memory accesses that can be accessed at GPU memory bandwidth as long as the pages that contain the accessed data are in the GPU memory. However, a major issue with this reactive approach is that the software overhead involved in the virtual address translation and page fault handling mechanisms when the accessed data is missing from the GPU memory and needs to be brought into GPU from the storage. Therefore, one can view the maximal page transfer throughput of the UVM implementation to be the upper bound of throughput of an on-demand storage access mechanism for GPUs based on virtual memory address translation and page fault mechanisms.

Each bar in Figure 1 shows the achieved host-memory-to-GPU-memory data transfer bandwidth of the UVM page fault handler on NVIDIA A100 GPU in a PCIe Gen4 system executing BFS graph traversal on six different datasets (See Table IV) where the edgelists are in the UVM address space and initially in the host memory. From Figure 1, the average PCIe bandwidth achieved by the UVM page faulting mechanism is \( \sim 14.52 \text{GBps} \) which is only 55.2% of the measured peak PCIe Gen4 bandwidth, 26.3GBps. From profiling data, the maximum UVM page fault handler rate measured in our experiments is \( \sim 500 \text{K IOPs} \). From Table III, \( \sim 500 \text{K IOPs} \) is only half of the achievable throughput of a Samsung 980pro SSDs and less than 10% of the achievable throughput of an Intel Optane SSDs. Furthermore, the IOPs of the UVM page fault handler is limited due to several factors including a limited amount of resources available to handle TLB misses \[29\] and serial driver implementation \[14\]. In our experiments, we find that the UVM fault handler on the host CPU is 100% utilized during the graph traversal benchmark execution.

With these limitations, even if we were to build a hypothetical system by integrating the file system layer into the UVM driver, and assume no additional overhead, it is impossible for the current UVM implementation to generate requests at a sufficiently high rate to fully utilize even one SSD for fine-grain accesses. Therefore, BaM employs software caching and high-throughput user-level NVMe queues to avoid the TLB and page fault handler bottlenecks and provides explicit and direct access to storage.

B. A Concrete Example of I/O Amplification

A CPU-centric alternative to the page-fault approach requires the programmer to partition the data into chunks and write CPU code to orchestrate data movement according to the needs of each phase of compute. Although this CPU-centric model works well for some classical GPU applications with predefined, regular, and dense access patterns, it is problematic for our target applications such as data analytics. The execution time overhead of the synchronization and CPU orchestration compels the developers to resort to coars-grain data transfers, which exacerbates I/O amplification, as discussed in more detail below.

Take executing analytics queries on the NYC taxi ride dataset (See IV-C for details) as an example. Suppose we ask the question, “Query 1: What is the average trip distance for trips starting in Williamsburg?”. This requires scanning the entire pickup_gid column of the dataset to find the trips that meet the criteria of starting in Williamsburg. Then the trip_dist value for those trips must be aggregated to generate the query result. However, since accesses to the trip_dist column are dependent on values in the pickup_gid column, in the CPU-centric model, the CPU cannot determine which trip_dist values are required. Thus, to leverage the bandwidth of the storage, the state-of-the-art GPU accelerated data analytics framework, RAPIDS \[2\], fetches all rows of both columns from storage to GPU. As only 901k trips start in Williamsburg and thus only 0.05% of the second column will be used. As a result, RAPIDS causes \( 6.34 \times \) I/O amplification for this query.

If the question is modified to “Query 2: What is the average total charge per mile for trips starting in Williamsburg?”, then three columns need to be accessed: pickup_id, trip_dist and total_amt. For this query, RAPIDS causes an I/O amplification of 10.36\( \times \) as it transfers two whole data-dependent columns, trip_dist and total_amt, to GPU memory. The query can be further extended to answer more interesting questions by adding additional data-dependent metrics, like surcharges (Query 3), hail fee (Query 4), tolls (Query 5) and taxes (Query 6). But doing so results in gross I/O amplification in the CPU-centric model as shown in Figure 2. The fine-grained, on-demand storage access capability in BaM mitigates such I/O amplification problems.

C. Latency, Throughput, Queue Depth and Concurrency

The design of a high-throughput storage access system is fundamentally governed by Little’s Law: \( T \times L = Q_d \), where \( T \) is the target throughput, i.e., the desired number of accesses...
SSD device latency

Modelled IOPs (Millions)

20
30
40
50
60
70
80
90
100%
20%
40%
60%
80%
100%

SSD device latency
PCIe overhead
Software latency (io_uring)

324.1us
28.0us
11.1us

Samsung 980pro
Samsung DC 1735
Optane P5800X

Fig. 2: I/O amplification on GPU-accelerated data analytics application using the state-of-the-art RAPIDS [2] system.

Fig. 3: Software overhead in the CPU-centric model for 4KB transfer size. The numbers represent measured total latency.

per second for accessing the storage, \( L \) is the average latency, i.e., number of seconds from the start to the completion of each access, and \( Q_d \) is the minimal queue depth required to sustain the target throughput over a period of time.

If the system can generate access requests at an average rate no less than \( T \), then \( T \) is limited by the bandwidth of the most critical resource (bottleneck) in accessing storage data. In the case of our prototype BaM system, we want to achieve the full potential of the critical resource, PCIe \( \times 16 \) Gen4 connection with 512B and 4KB access granularities [6]. Thus considering measured maximal PCIe \( \times 16 \) Gen4 bandwidth of \(~26\)Gbps, the value of \( T \) for 512B access is \( 26 \)Gbps/512B = 51M/sec and for 4KB access is \( 26 \)Gbps/4KB = 6.35M/sec.

The value of \( L \) depends on the SSD devices used and the interconnect latency. As shown in Figure 3, accessing one Intel Optane SSD over \( \times 4 \) PCIe Gen4 interconnect has an average latency of 11\,us whereas accessing a Samsung 980pro consumer grade SSD over PCIe Gen4 \( \times 4 \) interconnect has an average latency of 324\,us. From Little’s Law, to sustain a desired 51M accesses of 512B each, the system needs to accommodate a queue depth of 51M/\( s \times 11\,us \) = 561 requests (70 requests for 4\,KB) for Optane SSDs. For the Samsung 980pro SSDs, the required \( Q_d \) for sustaining the same target throughput is 51M \times 324\,us = 16,524 (2057 for 4KB).

Note that the “queue depth” could be spread over multiple queues as long as all these queues are being actively served by the SSD device(s). That is, at any moment, the system must be able to have at least 561 concurrent requests in the submission queues in order to be able the sustain the target throughput \( T \). Obviously, one must have many times of this number in concurrently serviceable requests in order to sustain this queue depth and thus \( T \) over a significant period of time.

Assume that for a phase of the application, we have \( X \) concurrently serviceable access requests. Assuming that these requests can be enqueued at a throughput at least as high as \( T \), we can expect that the sustained delivery rate for servicing all the requests is the total number of requests divided by the total amount of time for the delivery \( X/(L + X/51M) \). For \( X \) much larger than \( 51M \times L \), the sustained delivery rate will be close to 51M. As shown in Figure 4 for Intel Optane SSDs

Fig. 4: Assuming PCIe is the bottleneck, the read IOPs that can be potentially supported by different numbers of concurrent requests (\( X \)) at 512B access granularity for respective SSDs.

the application needs to have \(~8\)K concurrently serviceable accesses in each phase of execution while for the consumer grade Samsung 980pro SSD we need about \(~256\)K concurrent accesses to maintain the sustainable delivery rate of 51M at 512B (2K and 64K concurrent access at 4KB for Intel Optane and Samsung 980pro SSDs, respectively). That is, with sufficient number of concurrently serviceable accesses, consumer grade NAND SSDs can achieve comparable throughput as server grade Optane SSDs.

Thus, a system needs to have at least 10 Intel Optane SSDs or up to 50 Samsung SSDs so that the SSDs are not the bottleneck of data storage accesses. Additionally, since all SSDs have much lower throughput for writes than reads, so an application with a significant number of writes will most likely find the SSDs to be the bottleneck.

D. NVMe Queues

The NVMe [6] protocol is the latest standard defined by the industry to enable high-throughput access and to provide virtualization support for both server and consumer grade SSDs. NVMe protocol allows up to 64\,K parallel submission (SQ) and completion (CQ) queues, each with 64\,K entries per device. The NVMe device driver allocates a pool of buffers in the memory for use by the DMA engine of SSD devices for read and write requests. These queues and buffers traditionally reside in the system memory in the CPU-centric model.

An application requesting storage accesses causes the driver to allocate a buffer from the I/O buffer pool for the request and enqueue an NVMe I/O command at the tail of a SQ with a unique command identifier. The driver then writes the new tail value to the specific SQ’s write-only register in the NVMe SSD’s BAR space, i.e., it rings the queue’s doorbell. For improved efficiency, a driver can ring the doorbell once after enqueuing multiple requests into a SQ.

For a read request, the SSD device controller accesses its media and delivers the data into the assigned buffer using its DMA engine. For a write request, the SSD device controller DMAs the data in the buffer into its media. Once a request is serviced, the SSD device controller inserts an entry into the CQ. When the host driver detects that the CQ entry for a command identifier is in place, it retires the request and frees up the space in the queue and buffers for the request. The completion entry also notifies the driver how many entries in the SQ are consumed by the NVMe controller. The driver uses this information to free up space in the SQ. To communicate forward progress, the driver then rings the CQ doorbell with
the new CQ head. For efficiency, an SSD device can insert CQ entries for multiple requests in one transaction.

Figure 5 shows the latency breakdown of an I/O request from a highly optimized CPU software stack, io_uring, to three different NVMe SSDs: a high-end consumer grade SSD as the Samsung 980 Pro and two high-end ultra low latency data-center grade SSDs (the Samsung DC 1735 and Intel Optane P5800X). Clearly, as device latency is reduced, the software overhead becomes a significant fraction, up to 36.4%, of the total I/O access latency. The BaM software cache and high-throughput NVMe queues are designed to eliminate and/or hide such overhead.

III. BaM SYSTEM AND ARCHITECTURE

The goal of BaM’s design is to address insufficient GPU memory capacity and enhance effective storage access bandwidth utilization while providing high-level abstractions for accelerators to make on-demand, fine-grain, high-throughput access to storage. BaM proposes an accelerator-centric computing model in which GPU threads can access data where it is stored, be it memory or storage, without relying on the CPU to orchestrate data movement. To this end, BaM provisions NVMe I/O queues and buffers in the GPU memory and maps the NVMe doorbell registers to the GPU address space. Although doing so enables the GPU threads to access terabytes of data on NVMe SSDs, BaM must address three key challenges in providing an efficient and effective solution:

1) As the NVMe protocol and devices can induce significant latency, BaM needs to leverage the GPU parallelism to keep many requests in flight and efficiently tolerate such latency. (See §III-C)

2) As NVMe devices have very limited bandwidth and GPUs have limited memory capacity, BaM must optimally utilize these resources for applications. (See §III-D)

3) As we aim to evaluate BaM with existing hardware, the BaM hardware and software must overcome the challenges associated with off-the-shelf components. (See §III-F)

This section describes how BaM addresses these challenges.

A. BaM System Overview

An overview of the BaM system architecture is shown in Figure 5. BaM provides high-level programming abstractions, such as N-dimensional arrays and key-value stores, enabling programmers to easily integrate BaM in their existing GPU applications. An application can call BaM APIs to create a map from the abstract data structure to the data block ranges on the NVMe drive. The programmer then instantiates the abstractions by passing the map to a constructor of the abstract data structure. This mapping metadata is enough for the abstraction to find needed data blocks in SSD when required.

Each GPU thread uses the abstraction to determine the block offset for the data being accessed. The thread then indexes the BaM software cache (§III-D) in GPU memory using the offset as a key, as shown in Figure 5. The abstraction also has warp-level coalescer to increase the effectiveness of accesses. If an access hits in the cache, the thread can directly access the data in GPU memory. If the access misses, the thread needs to fetch data from the backing memory. The BaM software cache is designed to optimize the bandwidth utilization to the backing memory in two ways: (1) by eliminating redundant requests to the backing memory and (2) by allowing users to have fine-grain control of cache residency for their data.

If an NVMe SSD is backing the data, the GPU thread enters the BaM I/O stack (§III-C) to enqueue an NVMe request and then waits for the NVMe SSD to post the corresponding completion entry. The BaM I/O stack aims to amortize the software overhead associated with the NVMe protocol (§II-C) by leveraging the GPU’s immense thread-level parallelism, and enabling low-latency batching of multiple submission/completion queue entries to minimize the cost of expensive doorbell register updates in the NVMe protocol and reducing the critical sections in the NVMe protocol. On receiving the doorbell update, the NVMe SSD fetches the corresponding submission queue entries, processes the command to transfer the data between SSD and the GPU memory. At the end of the transfer, NVMe SSD posts a completion entry in the completion queue. After the completion entry is posted, the thread updates the cache state for the key and then can access the fetched data in GPU memory.

B. Comparison With the CPU-Centric Design

When compared to the traditional CPU-centric model shown in Figure 6a, BaM has three main advantages. First, in the CPU-centric model, as the CPU manages the storage data transfer and GPU compute, it ends up copying data between the storage and GPU memory and launching compute kernels multiple times to cover a large dataset. Each kernel launch and termination incurs costly synchronization between the CPU and the GPU. Since BaM allows GPU threads to do both compute and fetch data from storage as shown in Figure 6b, the GPU doesn’t need to synchronize with the CPU as frequently, and more work can be done in a single GPU kernel. Furthermore, the storage access latency of some threads can also be overlapped with the compute of other threads thus improving the overall performance. Second, because the compute is offloaded to the GPU and the data orchestration is managed by the CPU in the CPU-centric model, it is difficult for the CPU to determine which parts of the data are needed and when they are needed, thus it ends up fetching many unneeded bytes. With BaM, a GPU thread fetches the specific data it needs only when it requires it, reducing the I/O amplification overheads that the CPU-centric model suffers. Third, in the CPU-centric model, programmers expend effort to partition the application’s data and overlap compute with data transfers to hide storage access latency. BaM enables the programmer to naturally harness GPU thread parallelism across large datasets to hide the storage access latency.

C. I/O Stack

The BaM I/O stack serves two purposes. First, it enables the GPU threads to use NVMe queues to communicate with NVMe SSDs. Second, it deploys high-throughput queues that
leverage the GPU’s massive parallelism to overcome the challenges associated with the NVMe software stack. Here, we describe how the BaM I/O stack achieves these goals.

1) Enable Direct NVMe Access From GPU Threads: In order to enable GPU threads to directly access data on NVMe SSDs we need to: 1) move the NVMe queues and I/O buffers from CPU memory to GPU memory and 2) enable GPU threads to write to the queue doorbell registers in the NVMe SSD’s BAR space. To this end, we create a custom Linux driver that creates a character device per NVMe SSD in the system, like the one by SmartIO [35]. Applications use BaM APIs to open the character device for the SSD they wish to use.

In the custom Linux driver, BaM leverages GPUDirect RDMA features to allocate and manage NVMe queues and I/O buffers in the GPU memory. BaM uses the `nvidia_p2p_get_pages` kernel API to pin the pages of NVMe queues and I/O buffers pre-allocated in GPU memory and then maps these pages for DMA access from another PCIe device, like NVMe SSDs, using `nvidia_p2p_map_pages` kernel API. This enables the SSD to perform peer-to-peer data reads and writes to the GPU memory.

We leverage GPUDirect Async to map the NVMe SSD doorbells to the CUDA address space so GPU threads can ring the doorbells on demand. This requires the SSD’s BAR space to be first memory-mapped into the application’s address space. Then the BAR space is mapped to CUDA’s address space using the `cudaHostRegisterAPI` with the `cudaHostRegisterIoMemory` flag. Using `cudaHostGetDevicePointer`, the application gets the virtual address that the GPU threads can use to ring the NVMe SSD doorbell registers.

2) High-Throughput I/O Queues: Now that GPU threads can communicate directly with NVMe devices we need to optimize the synchronization between the thousands of GPU threads when accessing the shared queues. As described in [II-D], the NVMe protocol requires the driver to write doorbell values to registers in the SSD BAR space. As these doorbell registers are write-only, when a thread rings a doorbell, say to enqueue an I/O request, it must make sure that no other thread is writing to the same register and that the value it is writing is valid and is a newer value than any value written to that register before. A naive solution would be to acquire a lock before enqueuing a command to the submission queue and ring the doorbell. However, with the thousands of parallel threads on the GPU, such a design will lead to severe latency as all I/O requests will be serialized.

Instead, BaM uses fine-grain memory synchronization to allow many threads to enqueue I/O requests in parallel and only enter a critical section to ring the doorbell. To achieve this we keep the following metadata in GPU memory per submission queue: 1) local copy of the queue head, 2) local copy of the queue tail, 3) atomic ticket counter, 4) turn_counter array, an array of integers the same length as the queue, and 5) a mark bit-vector with as many bits as the length of the queue.

When a thread wants to enqueue a request, it first atomically increments the ticket counter. The returned ticket value can be divided by the queue size to assign the thread an entry in the queue, the remainder, and its turn on that position, the quotient. The thread uses its entry to index into the turn_counter array and polls on the location until its counter value equals the thread’s turn. When it is the thread’s turn, the thread can copy its NVMe command into its assigned position in the queue. After copying, the thread sets the position’s corresponding bit in the mark bit-vector. The thread then races to reset the bit for the current tail in the bit-vector. If it is successful, it enters the critical section to move the tail and it keeps resetting bits in the bit-vector sequentially until either it hits a bit that hasn’t been set or the queue is full. At that point, the thread knows the new tail value and can ring the doorbell with it. The thread then updates the copy of the tail in GPU memory, thus leaving the critical section.

If the thread failed to enter the critical section, it keeps trying until its bit in the mark bit-vector is reset. The main benefit to this approach is that many threads can find their place in the queue and write their command into their corresponding queue entry without requiring any lock. In fact, most threads that enqueue a command into the submission queue won’t even enter the critical section for ringing the doorbell as a single thread that does enter the critical section can move the tail as far as possible.

After the thread’s command is submitted, the thread can poll, without any lock, on the completion queue to find the completion entry for its submitted request. When it finds the completion entry, it must mark the completion queue entry location to be consumed by the head to communicate forward progress to the NVMe controller. Moving the completion queue head and ringing the doorbell with the new head are accomplished the same way threads move the submission queue head; threads race to reset the marker for the current head and the thread that enters the critical section keeps resetting markers until it can’t anymore.

However, before the thread can leave the completion queue critical section it also must update the submission queue head in order to free up space for the next round of commands to be enqueued. Each completion queue entry has a field which lets the NVMe controller communicate to the driver the position it can move the submission queue head. The thread reads this field from the last completion queue entry it could reset.
BaM model
Logical view of BaM design

the marker for. It then iterates from the current submission
queue head until the head value specified in the completion
entry, incrementing each position’s turn_counter value by
one. The thread then updates the submission queue head and
exits the critical section by updating the local copy of the
completion queue head in GPU memory. If a thread notices
the completion queue head has moved past its entry it doesn’t
enter the critical section.

D. BaM Software Cache

The BaM software cache is designed to allow optimal use of
the limited GPU memory and off-GPU bandwidth. Traditional
kernel-mode memory management (allocation and transla-
tion) implementations must support diverse, legacy applica-
tion/hardware needs. As a result, they contain large critical
sections that limit the effectiveness of multi-threaded imple-
mentations. BaM addresses this bottleneck by pre-allocating
all the virtual and physical memory required for the software
cache when starting each application. This approach allows the
BaM software cache management to reduce critical sections,
only requiring a lock when inserting or evicting a cache line. In
turn, the BaM cache supports many more concurrent accesses,
especially when the data is in GPU memory.

When a thread queries the cache with an offset, it directly
checks the corresponding cache line’s atomic state. If it is
valid, the thread increments the reference count of the cache
line. If the accessed cache line was not in the cache, the thread
will lock the cache line, and find a victim to evict, request
the cache line from the backing memory. When the request
completes, the requesting thread unlocks the cache line by
making its state valid and incrementing its reference count.
This locking prevents multiple requests to the backing memory
for the same cache line, exploiting spatial locality in the data
and minimizing the number of requests to the backing memory.
When the thread is done using the cache line, its reference
count is decremented.

The BaM cache uses a clock replacement algorithm. The
cache has a global counter that gets incremented when a thread
needs to find a cache slot. The returned value of the counter
tells the thread which cache slot to attempt to use. If the picked
cache slot is currently mapped to a cache line that has a non-
zero reference count, the thread will move on and increment
the global counter again to attempt to replace the next cache
slot instead. When the thread finds a cache slot pointing to
a cache line with a reference count of 0, the thread attempts
to evict it by setting the cache line state to a transient state.
If successful, the thread will mark the cache line invalid and
change the mapping of the cache slot to point to the cache
line the thread wants to bring in. Otherwise, it will increment
the counter again and attempt to take the next cache slot.

Warp Coalescing: Even though BaM’s software cache
minimizes the number of requests to the backing memory,
it adds additional overhead on each access in the form of
cache line state management. Threads in a warp often contend
among themselves especially when consecutive threads try to
access contiguous bytes in memory. To overcome this, BaM’s
cache implements warp coalescing in software using warp-
level primitives. When threads make an access to the cache, the
__match_any_sync warp primitive is used to synchronize
with other threads in the warp and a mask is computed
letting each thread know which other threads in the warp are
accessing the same offset. From that group, the threads decide
on a leader and only the leader manipulates the requested
cache line’s state. The threads in the group synchronize using the
__shfl_sync primitive, and the leader broadcasts the
address of the requested offset in the GPU memory to the
group. This coalescing is especially useful for reducing access
overhead when the data is already in the GPU memory, as that
is when any added overhead per access is most visible.

E. BaM Abstraction and Software APIs:

BaM’s software stack provides the programmer an array-
based high-level API (BamArray<T>), consistent with array
interfaces defined in modern programming languages (e.g.
C++, Python, or Rust). As GPU kernels operate on such arrays,
BaM’s abstraction trivializes the programmer’s effort to adapt
their kernels so that they operate on entire data sets, as shown
in Listing 1. In contrast, the CPU-centric model requires full,
non-trivial application rewrites to optimally decompose the
compute and data transfers into partitions that fit within the
limited GPU memory.
BaMArray’s overloaded subscript operator hides all of BaM’s complexity from the programmer. The operator enables the accessing threads to coalesce their accesses by picking a leader that queries the BaM cache and makes the I/O request on a miss. When the request completes, the leader thread shares the reference of the cache line with the other threads in the warp. Each thread uses the reference to return the appropriate element of type T to the calling function.

BaM initialization requires allocating some internal data structures that are reused during the application’s lifetime. Initialization can happen implicitly through a library construction if no customization is needed. Otherwise, the application specializes the memory through template parameters to BaM’s initialization call, a standard practice in C++ libraries. We also provide 4 memory implementations for BaMArray: (1) SSDs with BaM’s cache (default), (2) pinned CPU memory with BaM’s cache, (3) pinned CPU, and (4) GPU memory. However, in most cases, specialization and fine-tuning are not strictly necessary, as we show later in § IV where only BaM’s default parameters are used.

F. Design of BaM System Prototype

The design of BaM using the PCIe slots available within a data-center grade 4U server comes with several challenges. The number of PCIe slots available in these machines is limited. For instance, Supermicro AS-4124 system has five PCIe Gen4 ×16 slots per socket. If a GPU occupies a slot it can only access 4 ×16 PCIe devices without crossing the inter-socket fabric. Furthermore, due to the chiplet design of modern multi-core CPUs, even when the 5 PCIe devices per socket access each other, they must cross the intra-CPU fabric. Crossing these different interconnects results in severe performance degradation as packets must be translated for each interconnect, increasing latency and limiting throughput. However, as we discussed in § II-C BaM hardware should support scaling to a large number of NVMe devices to provide the necessary throughput to saturate the ×16 PCIe Gen4 GPU bandwidth, without much overhead.

To address this, we built a custom prototype machine for the BaM architecture using the off-the-shelf components as shown in Figure 7. Table II provides the specification of the major components used for the prototype. BaM prototype uses a PCIe expansion chassis with custom PCIe topology for scaling the number of SSDs. The PCIe switches support low-latency and high-throughput peer-to-peer access between PCIe devices. The expansion chassis has two identical drawers, both of which are currently independently connected to the host. Each drawer supports 8 ×16 PCIe slots (as shown in Figure 7a). We use one ×16 slot in each drawer for an NVIDIA A100 GPU and the rest of the slots are populated with different types of SSDs. Currently, each drawer can only support 7 U.2 (Optane or Z-NAND) SSDs as the U.2 form factor takes up significant space. As the PCIe switches support PCIe bifurcation, a PCIe multi-SSD riser card enables more than 16 M.2 NAND Flash SSDs per drawer. Cascading of drawers, currently under development, will allow us to scale to more SSDs of all types.

SSD Technology trade-offs: Table III lists the metrics that significantly impact the design, cost and efficiency of BaM systems for three types of off-the-shelf SSDs. The RD IOPS (512B, 4KB) and WR IOPS (512B, 4KB) columns show the measured random read and write throughput of each type of SSD at 512B and 4KB granularity respectively. The $/GB column presents the cost per GB for each SSD type, based on the current list price per device, the expansion chassis, and the risers needed to build the system. The Latency column shows the measured average device latency in μs. A comparison of these metrics across SSD types shows that the consumer grade NAND Flash SSDs are inexpensive with more challenging characteristics, while the low-latency drives such as Intel Optane SSD and Samsung Z-NAND are more expensive with more desirable characteristics. For example, for write intensive applications using BaM, Intel Optane drives provide the best write IOPs and endurance.

Irrespective of the underlying SSD technology, as shown in Table III BaM provides 4.4-21.8× advantage in cost per GB, even with the expansion chassis and risers, over a DRAM-only solution. Furthermore, this advantage grows with additional capacity added per device, which makes BaM highly scalable as SSD capacity and application data size increase.

IV. Evaluation

This section presents an evaluation of the prototype BaM hardware/software system and shows that a) BaM can generate sufficient I/O requests to saturate the underlying storage system (see § IV-A). b) Even with one SSD, BaM’s performance is either on-par with or outperforms the state-of-the-art solutions (see § IV-B and § IV-C). c) BaM design is agnostic to the SSD storage medium used, enabling application-specific cost-effective solutions. d) BaM reduces I/O amplification and CPU orchestration overhead significantly for data-analytics
TABLE III: Comparison of different types of SSDs with DRAM DIMM.

| Technology     | Sources | Product | RD IOPs (512B, 4KB) | WR IOPs (512B, 4KB) | Latency (µs) | DWPD | $/GB |
|----------------|---------|---------|---------------------|---------------------|--------------|------|------|
| DRAM           | multiple| DDR4    | >10M                | >10M                | <0.1         | >1000| 11.13|
| Optane         | single  | Intel P5880X | 5.1M, 1.5M         | 1M, 1.5M           | O(10)        | 100  | 2.54 |
| Z-NAND Flash   | single  | Samsung P1735 | 1.1M, 1.6M         | 351K, 351K         | O(25)        | 3    | 2.56 |
| NAND Flash     | multiple| Samsung 980pro | 700K-800K, 700K-800K | 172K, 172K         | O(100)       | 0.3  | 0.51 |

Fig. 7: Prototype implementation of BaM using off-the-shelf components.

Fig. 8: 512B random read and write benchmark scaling with BaM on Intel Optane P5800X SSDs. BaM’s I/O stack can reach peak IOPs per SSD and linearly scale for both random read and write accesses. 4KB random read and write accesses exhibit similar scalability but level off between 3 and 4 Intel Optane SSDs due to saturating the Gen4 ×16 PCIe bandwidth. Similar scaling is observed for Samsung SSDs (not shown for brevity).

A. Raw throughput of BaM measured with micro-benchmarks

Setup: We first evaluate the raw throughput achievable by BaM on synthetic random access micro-benchmarks with Intel Optane SSDs. We map the entire SSD capacity to the GPU address space as described in [I]. We allocate all the available SQ/CQ queue pairs of the SSD into GPU memory with a queue depth of 1024. We then launch a CUDA kernel with each thread requesting a unique random 512-byte block from the SSD. Each thread submits an NVMe request to a designated queue. The queues are designated to the GPU threads in a round-robin scheme. We then vary the number of threads and SSDs mapped to a single NVIDIA A100 GPU. For multiple SSDs, the requests are further distributed across SSDs in a round-robin fashion. We measure I/O operations per second (IOPs) as a metric defined as the ratio of the number of requests submitted by the GPU and the kernel execution time.

Results: Figure 8 presents the measured IOPs for 512B random read and write accesses benchmark. BaM can reach peak IOPs per SSD and linearly scale with additional SSDs for both reads and writes. With a single Optane SSD, BaM only requires about 16K-64K GPU threads to reach near peak IOPs (see Table III). With seven Optane SSDs, BaM achieves 35M random read IOPs and 7.4M random write IOPs, the peak possible for 512B accesses to the Intel Optane SSDs. The maximal number of SSDs in the scaling experiment is currently limited by the drawer capacity of the expansion chassis. Additional scaling will be done once we complete the development of drawer cascading. Similar performance and scaling is observed with Samsung SSDs and also at 4KB access sizes but are not reported here for compactness. These results validate that BaM’s infrastructure software can match the peak performance of the underlying storage system. We next evaluate BaM with application benchmarks.

B. Performance benefit for graph analytics

Setup: First, we evaluate the performance benefit of BaM for graph analytics applications. We use the graphs listed in Table IV for the evaluation. K, U, F, M are the four largest graphs from the SuiteSparse Matrix collection [24] while the UK and Sk are taken from LAW [19]. These graph datasets cover diverse domains including social networks, web crawls, bio-medicine, and even synthetic graphs.

A goal of the BaM is to provide competitive performance against the DRAM-only graph analytics solution. To this end, the target baseline system T allows the GPU threads to directly perform coalesced fine-grain access to the data stored in the host-memory during graph analytics execution [36]. As the input graphs can each fit into the host-memory, we can make a direct comparison of the performance between BaM and T.

We run two graph analytics algorithms, Breadth-first-search (BFS) and Connected Component (CC), with the target system and BaM with different SSDs listed in the Table III. In BFS, each GPU warp is assigned to a node being visited in the...
current iteration, where all threads in the warp collaboratively walk through the node’s neighbor list. The CC implementation follows a similar assignment as BFS except that the application starts by examining all the nodes in the graph, thus exhibiting a more bursty access pattern than BFS. For BFS, we report the average run time after running at least 32 source nodes with more than two neighbors. We do not execute CC on the UK and Sk datasets since CC operates only on undirected graphs. Lastly, we fix the BaM software cache size to 8GB and the cache-line size to 4KB.

**Overall performance with one SSD:** Figure 9 shows the performance of both the target system (T) and BaM with single Intel Optane SSD (B_I), Samsung DC 1735(B_S) and Samsung consumer grade 980 Pro SSD (B_SC). Recall that the target system T benefits from full ×16 Gen4 PCIe bandwidth between the host and GPU, while BaM is limited to the single SSD’s ×4 Gen4 PCIe interface.

Yet, across all the graphs and algorithms, the performance of BaM with Intel Optane SSD (B_I) ranges from slightly faster to 4.4× slower than the target T system without considering the initial file loading time for the T system. This is because with one SSD, the BaM performance is limited by the throughput of the SSD’s ×4 Gen4 PCIe interface. If we include the initial file loading time for the T system, BaM is on average 1.1× and 1.29× faster than the T system for BFS and CC, respectively. In both cases, the GPU compute kernels perform on-demand graph edge data access through the BaM 1D array abstraction. This allows BaM to overlap the data transfers from SSD for some threads with the compute of other threads. In contrast, the target system T needs to wait until the file is loaded into memory before it can offload the compute to GPU. The superior host-memory bandwidth of the T system cannot overcome the initial file loading latency. As a result, BaM achieves higher end-to-end performance.

Samsung DC 1735 and the Intel Optane SSD have similar performance for almost all workloads, since the peak 4KB random read IOPs achieved by both drives is limited by the PCIe ×4 interface. However for two datasets (U and M) in the CC workload, Samsung DC 1735 performs poorly and our initial analysis indicates that this is because of the long tail latency coming from the SSD controller while handling the bursty random access pattern of CC for these two graphs. Shifting focus to cost effectiveness, with one Samsung 980 Pro SSD, BaM prototype is on average 1.97× and 1.85× slower for BFS and CC workload compared to the target system inclusive of file-loading time. These are very encouraging results for consumer-grade SSDs as they provide by far the best value among all the SSD technologies.

**Impact of cache-line size:** We vary the cache-line size of the BaM software cache from 512B to 8KB to understand the impact of access granularity on graph analytics workloads. Recall that the BaM cache-line size determines the granularity of access to the storage. The evaluation is done using a single Intel Optane SSD because of its high IOPs rates (see Table III). From Figure 10 as we decrease the cache-line size from 4KB to 512B, BFS and CC workloads on average slow down by 1.41× and 2.31× respectively. This is because graph workloads exhibit spatial locality within their neighbor lists, and can benefit from larger accesses. Furthermore, our profiling data shows that the BFS and CC application can generate 4.76M IOPs and 4.97M IOPs for 512B access, respectively. This translates to ~2.5GBps and ~6GBps of bandwidth for 512B and 4KB access to storage, nearing the peak achievable bandwidth for one Optane SSD.

Three main findings emerge: a) the workloads running in BaM can generate enough I/O requests to saturate the throughput of the drive. b) the 4K granularity takes advantage of the spatial locality of large neighbor lists in some of the graphs and the extra bytes transferred for smaller neighbor lists don’t deteriorate performance as the PCIe bandwidth is not oversaturated. c) BaM’s fine-grain access reduces I/O amplification, thereby improving the effective bandwidth. Otherwise, the application would have had up to an 8× slowdown upon reducing the cache-line size from 4KB to 512B. Increasing the cache-line size from 4KB to 8KB barely impacts the overall performance. This is because at 4KB the application is near the SSD PCIe bandwidth limit and further increasing the cache-line size does not improve the bandwidth. Similar performance variations and trends are observed in both Samsung devices and are not discussed for brevity.

**Scaling to multiple SSDs:** We scale the number of SSDs and replicate data across SSDs to increase BaM’s aggregated bandwidth. Figure 11 shows the scaling result for Optane SSDs

**TABLE IV: Graph Analytics Datasets.**

| Graph             | Num. Nodes | Num. Edges | Size (GB) |
|-------------------|------------|------------|-----------|
| GAP-krone (G)     | 134.2M     | 4.22B      | 31.5      |
| GAP-unrand (G)    | 134.3M     | 4.29B      | 32.0      |
| Friendster (F)    | 65.6M      | 3.61B      | 26.9      |
| MOLIERE-2016 (G) | 30.2M      | 6.67B      | 49.7      |
| uk-2007-05 (Gk)   | 105.9M     | 3.74B      | 27.8      |
| sk-2005 (Sk)      | 50.6M      | 1.95B      | 14.5      |

Fig. 9: Graph analytics performance of BaM and the Target (T) system with a single Intel Optane SSD. On average, BaM’s end-to-end time is 1.1× (BFS) and 1.29× (CC) faster than the Target.

Fig. 10: Impact of cache-line size on BaM performance for graph analytics with one Intel Optane SSD.
with 4KB cache-lines. Graph analytics workloads using BaM prototype scale well up to two Optane SSDs, beyond which is the point of diminishing returns.

Beyond two SSDs, the graph analytics applications using BaM prototype cannot generate I/O requests at a sufficiently high rate to effectively saturate the additional devices. Even though the application has sufficient I/O parallelism, current GPU kernel implementations [36] and data layout are optimized for exploiting locality and reducing the number of I/O requests rather than maximizing the rate of generating I/O requests in order to hide the long latency. These conflicting goals require design space exploration by sweeping over the work assignment for each thread or increasing work per thread so that the GPU threads can generate I/O requests at a higher rate to fully utilize more than 2 Optane SSDs.

Furthermore, several optimizations in the BaM software stack such as automatically varying the size I/O requests and prefetching are yet to be implemented. We will address these in the future. Yet, BaM with 4 Intel Optane SSD already provides on average 0.92× and 1.72× speedup on BFS and CC applications compared to the target system T with file-loading time. Even without considering file-loading time for the target system T, BaM achieves on average 0.72× and 1.51× speedup for BFS and CC workloads across all the datasets. Similar trends are observed for Samsung SSDs except that Samsung 980 Pro SSD scales well up to 4-10 SSDs before suffering diminishing returns for the graph workloads.

C. IO amplification benefit for data-analytics

Beyond graph analytics, we also evaluate the performance benefit of BaM prototype for enterprise data analytics workloads. These emerging data analytics are widely used to interpret, discover or recommend meaningful patterns in data that is collected over time or from unstructured data lakes. The experiments with data analytics aim to illustrate the benefits of BaM design for reducing I/O amplification and software overhead while working on large structured datasets.

Setup: §II-B discussed the I/O amplification problem with queries on the NYC taxi ride dataset [45]. The dataset consists of 200GB of encoded data organized as 1.7B rows and 49 columns in the Optimized Row Columnar (ORC) Format [45]. We run the six data-dependent queries described in §II-B to compare the performance of BaM against state-of-the-art GPU accelerated RAPIDS [2] v21.10 data analytics framework. One Intel Optane P5800X SSD is used for both the baseline and BaM. We evaluate the baseline with two configurations: a) a cold case with all data in the SSD and b) a warm case where the data has been fetched to the Linux CPU page cache.

Results: BaM with a single Intel Optane SSD outperforms RAPIDS performance in most cases in both cold and warm configurations, as shown in Figure 12. For Q1, the baseline (warm) has a slight advantage over the BaM because it can exploit the entire CPU DRAM bandwidth and PCIe ×16 Gen4 bandwidth to transfer the data between the host and the GPU, whereas BaM is limited by the SSD bandwidth. With the addition of data-dependent metrics, BaM performance increases as shown in Figure 12. The performance gain is attributed to BaM’s reduced I/O amplification due to on-demand data fetching while the baseline must transfer entire columns to the GPU memory. With additional data-dependent metrics, as shown in Figure 2 the baseline (both warm and cold) suffers from even more I/O amplification and software overheads on the CPU to find and move data, and manage GPU memory. However, BaM’s ability to make on-demand access to data as well as overlap compute, cache management, and many I/O requests help it handle multiple data-dependent columns nearly as efficiently as it can the single data-dependent column.

V. RELATED WORK

A. Optimized CPU-centric model

Most GPU programming models and applications were designed with the assumption that the working dataset fits in the GPU memory. If it doesn’t, application specific techniques like tiling are employed to process large data on GPUs [3], [18], [23], [25], [28], [30], [32], [39], [40], [47], [48]. SPIN [18] and NVMMU [53] propose to enable peer-to-peer (P2P) direct memory access using GPUDirect RDMA from SSD to GPU and exclude the CPU from the data path. SPIN integrates the P2P into the standard OS file stack and enables page cache and read-ahead schemes for sequential reads. GAIA [23] further extends SPIN’s pagecache from CPU to GPU memory. Gullfoss [47] provides a high-level interface that helps in setting up and using GPUDirect APIs efficiently. Hippogriffdb [22] provides P2P data transfer capabilities to the OLAP database system. GPUDirect Storage [3] is the most recent product that migrates the data path from CPU to GPU in NVIDIA CUDA software stack using GPUDirect RDMA technology. Similar efforts from AMD are seen in RADEON-SSG product lines [15]. All of these works still employ a CPU-centric model where the CPU is responsible for data orchestration. BaM provides explicit and direct fine-grain access to the storage from GPUs allowing any threads in GPUs to initiate, read and write data to the SSDs.
B. Prior attempts of the accelerator-centric model

ActivePointers [41], GPUs [43], GPUNet [50] and Syscalls for GPU [49] have previously attempted to enable accelerator-centric model for data orchestration. GPUs [43] and Syscalls for GPU [49] first allowed GPUs to request file data from the host CPU. ActivePointers [41] added a memory-map-like abstraction on top of GPUs to allow GPU threads access file data like an array. Dragon [34] proposed to incorporate storage access to the UVM [9] page faulting mechanism. However, all of these approaches rely on the significantly less-parallel CPU to handle the data demands of massively parallel GPUs. Thus, as shown in [41] these approaches end up with gross under-utilization of resources and poor overall performance. Moreover, all of these works do not leverage GPUDirect RDMA capabilities [5] and rely on transferring the data first to the CPU memory and then to the GPU memory.

C. Hardware extensions

Extending the support of non-volatile memories for GPUs has been proposed by directly replacing the global memory with flash memory or closely integrating it with the GPU memory system [50], [51], [54]–[56]. DCS [13] proposed enabling direct access between storage, network, and accelerators with the help of a dedicated hardware unit like an FPGA providing the required translation for coarse-grain data transfers. Enabling persistence within the GPU have recently been proposed [16]. We acknowledge these efforts and further validate the need to enable large memory capacity for emerging workloads. More importantly, BaM aims to use existing hardware and system to provide speed-of-light performance at end-to-end applications with very large real-world datasets.

VI. Conclusion

In this work, we make a case for enabling GPUs to orchestrate high-throughput, fine-grain accesses into NVMe solid state drives (SSDs) in a new system architecture called BaM. BaM mitigates the I/O amplification problem of reading more data than needed by reading or writing at finer granularities on-demand, as determined by the compute code running on these GPUs. Using off-the-shelf hardware components, we implement a prototype of BaM using different SSD types and show on multiple applications and datasets that BaM is a viable alternative to DRAM-only and other state-of-the-art CPU-centric solutions.

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