Design and Implementation of FPGA Based Configurable AI Architecture with Deep Learning Algorithm

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Abstract -Our main aim is to design a reconfigurable FPGA architecture using Network on chip using deep learning which act as a validation algorithm .In the Existing System we were using WiNoC (wireless network on chip) which was not reconfigurable . The energy saving in existing model was 55% whereas the proposed model saves upto 83 % of energy .Within the projected system Deep Learning formula is developed in VLSI design with acceptable model is intended on FPGA SOC chip, by that performance are analysed in terms of error rate, regression rate, confusion rate.

1. INTRODUCTION

A. Network on Chip(NoC)

Network on chip (NoC ) is a communication system on associate degree computer circuit (usually called as a "chip") .Operative technology uses network concept and ways to on-chip communication and that gives progressive enhancements on existing crossbar connections. It can work with different module but one at a time.

B. Parallelism and the scalability

Maximum percentage of similarity is achieved because wires which is present in the links of the operative is forwarded to a lot of signals, this result for all links in the operative to operate at the same time on different information packet. Since the quality of integrated design systems keeps on increasing, a operative provides increased performance and measurability as compared with existing communication model .The algorithm should be designed in such a manner that they should provide massive similarity which in turn utilize the potential of operative.
C. Benefit

In general, Integrated Circuits are created using point-to-point connections with each wire assigned to every signal. For huge models, this may have many drawbacks. Wires occupy lot of space on the chip, and in nano CMOS technology and interconnections have dominance in both parameters i.e performance and power dissipation. Here signal propagation requires multiple clock cycles.

D. Research done on on-chip networks

Barely any specialists guess that NoCs must be compelled to help nature of administration (QoS), explicitly succeed the varying necessities as far as turnout, start to finish postponements, decency, and due dates. Constant calculation, just as sound and video playback, is one of the explanation behind giving QoS support. Be that as it may, current framework usage like VxWorks, RT UNIX working framework or QNX can succeed sub-millisecond timeframe registering while not unique equipment. Committed equipment rationale would be compulsory to grasp time unit exactitude, a degree that is only from time to time required in watch for completion clients. Other inspiration for NoC-level nature of-administration is to help different synchronic clients sharing assets of same chip registering machine all through the overall population distributed computing framework. In these things , equipment QOS rationale allows the administration provider to frame composed understanding assurances on the degree of administration that a client gets, an element that will be regarded alluring by enterprises.

Fig.1:CPLD Development Board
The main devoted investigation gathering on systems on chip was organized at college, in 2007. Another IEEE International meeting on Networks-on-Chip was held in April 2008 at city University.

E. Deep Learning Principle

![Deep learning principle](image)

F. Proposed Methods

1. Network on Chip Creation using VHDL configurable Logic Blocks

2. Deep Learning neural Network Algorithm development

3. Result analysis provides Scalable Best network for the given data processing

2. WORKING

The main motive of our system is that, to make the system function according to how the human brain think. Suppose we want our system to move left, the data is processed from brain to brain sensors to the FPGA controller and at last to the display machine. The brain waves are collected from brain and converted into excel sheets through brain sensors. The excel sheets will vary from patient to patient. The excel sheets we get is the output of the brain sensors. The excel sheets are the input for our system. When they are feed into the system the FPGA controller sense the analog signal and converts it into digital signal. The CPLD hardware then process those signals and gives the same output as input because our motive is to get what is the input. Those input are collected through wave signals and are processed by the hardware to display the output. The processing is done by the deep neural algorithm which is created using VHDL (behavioural model).
Before the above process first we have to complete the process of creating more than one module and connect it into a network, this process is called Network On Chip creation. As a result of this the input from the brain waves i.e. the excel sheets are being processed by the deep neural algorithm which is dumped into the FPGA controller. The FPGA controller learns all the input through the sheets and produces the output accordingly. Basically, the output is same as the input. This artificial intelligence system will have many applications in the medical field as well as manufacturing field.

Note: The brain waves converted to excel sheets though brain sensors which are collected from a site called https://physionet.org/ The brain sensors cost will be more than 15000/- so we are taking the excel directly from the site and feeding as input to the FPGA controller.

In order to check different frequencies output we can add DC motor into the system which will result in change in the speed as frequency changes.

3. ARTIFICIAL INTELLIGENCE & VLSI (AI AND VLSI)

Most of the applications of computing (AI) is to design a skill system which in turn reduces man power but skilled systems technology is just one facet of AI. VLSI style is also an advanced methodology. Moreover, the quality is multi-dimensional. Size and level of detail are a pair of distinctive dimensions. Others embody the hierarchical nature of the design methodology equally as of the self-design. AI languages tend themselves to resolve problems with such quality. These language choices including skilled systems permit a significant begin to resolve a extremely powerful draw back i.e. the verification of the correctness of a method.

HARDWARE DESIGN IMPLEMENTATION Introduction to CPLD Device

Programmable Logic Devices (PLDs) supply big selection of logic capability, features, speed and voltage characteristics and these devices is modified at any time to perform any variety of functions. The CPLDs are efficient in working on wide and sophisticated gating at high speeds. The temporal arrangement model for CPLD is simple to calculate, therefore even before style it will calculate the in to output speeds. CPLDs alter simple style, lower development prices, additional product revenue for cash, and also the chance to hurry your product to promote, etc.

4. RESULT

A. Simulation Result

Fig.3: Simulation output from Model Sim software

We used Model Sim 6.3g software for the simulation of our program. We got the brain waves graph as well as the input and output graphs as pulses.
5. APPLICATIONS AND ADVANTAGES

1. It is a reconfigurable FPGA architecture
2. It is an automated system which will take clock and reset as input and generates the automated output by itself
3. Energy savings up to 83%
4. Easy to make progressive enhancements
5. Can be implemented in medical field
6. Can be used in driverless car.
7. It can be implemented in a disabled person

6. CONCLUSION

We have designed a cheap many core platform which work on BMBI method task. We tend to project an operative style that connects completely different modules with each other, which we'll even selected that modules we'd wish to figure with. This will be referred to as a reconfigurable style. Compared with the normal reserves algorithmic rule, the projected machine learning affected methodology achieves up to 83% saving in energy. In addition, we've developed a deep neural algorithm rule for determination of sophisticated BMBI.

7. REFERENCES

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