An Improved VLSI Design of 16 Bit Data Comparator using Bubble Sorting Algorithm

1Ramesh S M and 4Gomathy B
1Department of ECE
4 Department of CSE
1,4KPR Institute of Engineering & Technology, India
ramesh.sm@kpriet.ac.in, gomathy.b@kpriet.ac.in

2Mahes Kumar P
Dept. of EEE
Lords Institute of Engg & Tech Hyderabad, India
mahes@lords.ac.in

3Balaji G
Electric Power Streering System
Robert Bosch EBS Ltd , India

Abstract - Comparator is an important arithmetic component on a digital circuit. Here the major goal of this project is to design a data comparator, which gives the sparing solution for sorting the data on the basis of power, area, and speed. Sorting is one of the problems in computer engineering/science. In computing system or/and communication systems, many important processes require the sorting of data. Here, the proposed work comprises the design of 16 Bit Comparator with Bubble sorting algorithm. This proposed comparator design is targeted for 6slx4tg144-3 using Xilin ISE compiler tool by verilog model. The bubble sort algorithm also referred to the sinking sort algorithm. By this process, based on the adjancy pair of data, this will swap/interchange their positions/location. Here the proposed system is also design the 16 Bit Magnitude comparator for reducing delay factor of the system and the comparator design uses behavioural style for reducing the power factor. The overall system design optimizes the area by reducing the number of unwanted LUT block in the design. Since this proposed system gives the better result as compared to the conventional method by getting the result of power, area, and delay. The overall design is compiled through Xilinx 14.5 software and it is simulated by Modelsim tool.

Keywords - Data Comparator, Bubble sorting Algorithm, Power, Area and Delay reduction, Verilog

1. Introduction

The comparators are most widely used arithmetic component in digital circuit. Comparator plays a vital role in analogue or digital devices, because it speeds up the conversion process by reducing the power factor. In conventional method uses the CMOS technology for designing the comparator with op-amp circuitry and the magnitude comparator is used to determine the correctness of the value. Here the arithmetical operation is used to determine the less, greater and equal values by comparing one another. This magnitude comparator is in the form of integrated circuit, which is based on TTL (Transistor-to-Transistor Logic) technology. The existing method uses the design of comparator for Sigma Delta Analog to Digital Converters, which is based on CMOS Op-Amp technique. Here this technique uses two comparative modules. That is open loop comparators, regenerative comparators. The open loop comparators are performed based on op-amps without compensation technique, and regenerative components are providing positive feedback to the system. 8Bit comparators are designed with various digital logical unit is used in rank ordering image Applications. Here the SHEAR sorting algorithm is used to sort out the data from the comparator. Parallel and pipelined architecture is designed in [1].

In our proposed system, uses bubble sorting algorithm in logic comparator. The Shear sorting increases the complexity of design, since this proposed method uses bubble sorting algorithm for reducing the power factor and delay. In sorting algorithm, the insertion sorting technique is used in the conventional method, which takes the number of processing stage much. Since the time complexity problem is occurred. The bubble-sorting algorithm is to sort the array of data based on total number of elements in the comparator block, which takes the input data in sequential order. By this use of bubble sorting algorithm, the execution time is minimized and we can also reduce the performance degradation. This algorithm implemented in c language with Turbo C++. The design of Dynamic comparator and Double Tail Comparator has presented in [2]. The comparator design uses the multilevel look ahead design with domino logic for reducing the complexity of design architecture.

This proposed system assembled as follows: Section 2 describes the literature survey of most related papers. Section 3 is the proposed methodology and logical circuit with its schematic view is presented. Section 4 describes the resultant part of each module and its RTL schematic view, comparison with existing method by power, area, and delay factors are provided. Finally, Section V describes the overall conclusion of the proposed work and idea about the future work and its achievable results are described.

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2. Literature Review

[3] has proposed the VLSI architectural design of Data Comparators for the image application of Rank Ordering technique. Here the 8-Bit Data Comparator is designed with Shear sorting algorithm. Various data comparator model is performed in this sorting algorithm. Carry select logic-based data comparator technique reduces the area but it increases the power availability. Two’s complement technique uses the binary to excess one data converter, which reduces the power factor by increasing the number of processor stage. Parallel and pipelined architecture design is used in this various comparator. The bit wise data comparator is used as a magnitude comparator methodology. This uses the multiplexer for resultant logical block. Shear sorting algorithm is used in various comparator logic circuit.

[4] has proposed the design of comparator using CMOS of Op-Amp logic for gain boosting technique. This logic circuit achieve the slew rate and gain value, but the number of LUT block is increased this will increases the area of the system and increases the gain error. Cascade structure is used for comparator logic, which provides the parallel form of architecture design since it reduces the design complexity. The CMOS design of Op-Amp circuitry uses common mode current feedback is used for designing the architecture. This achieves the better result but it increases the complexity of overall design performance. Here SPICE simulator in CMOS technology has performed the Monte Carlo simulation.

[5] has proposed the design optimization procedure for digital mismatch compensation in latch comparators. This latch comparator is a regenerative comparator, which performed by regenerative clock signals. CMOS technology is used to design a comparator with calibration control unit. The Monte Carlo operation is performed before and after offset calibration process. This scheme has been designed in post-layout simulation process. Without the complexity reduction algorithm, likes sorting it causes significant performance degradation.

[6] has presented the VLSI design of Dynamic Double Tail Comparator, which is capable for the application of Data Converters. This comparator design gives the low voltage and low power analysis. Here the tanner EDA tool with 180nm technology was presents for designing the comparator. Clock regeneration is done in dynamic comparator, based on the input signals the clock cycle should be varied since it will improve the input impedance. In Double trail comparator, the reset phase will activate the transistors and other circuit parameters for getting the improve result. This method increases the power factor, when compared to the proposed method.

[7] has proposed the method to design a comparator for the application of sampled data processing. Here the 8-bit macro and multilevel look-ahead circuit is designed. This multilevel circuit uses the domino logic for reducing the complexity of the design. Here 8-bit comparator is designed for multilevel logic circuits with a single clock signal. The signal integrity problem is removed by differential signalling approach, which has identical driver block and a comparator design. It also has adders and multiplier blocks since it increases the area of the design architecture. The logical function is analysed by direct flattening process. Here the dynamic logic design implementation gives the faster operating time.

[8] has proposed for minimizing execution time of bubble sorting algorithm. Here there are two sorting techniques were performed that is Internal and external sorting. The execution time of both the algorithm is based on the input clock cycle. It is an exchange algorithm by performing swap and interchange operation based on the data value. After this array is sorted, the time and delay factor are analysed. This algorithm is implemented in c language of Turbo C++. This algorithm is also capable for the uses of various applications.

[9] has proposed the design of 4-Bit Magnitude Comparator using simulink model. The design of magnitude comparator and its simulink model is presented. Here the simulink environment is possible to design and develop a model by its advance techniques. Based on the logical gates the magnitude comparator design is made. The output of the comparator is showing the three different logic styles of the performance. By this work, the system achieves the resultant value, but the number of multiplexer block is increased in simulink model since it leads to time delay of performance.

[10] has proposed the design of digital comparator with the use of single mode Fabry-Perot laser diodes. Here 2-bit optical based digital comparator is designed with the data rate of 10Gbps. This design is implemented with the cascaded structure, which is based on injection locking beam supporting, and suppression modes. Here the decision making is done in the ALU block. The optical signal processing is used for the high-speed data transmission. The design complexity is increased by using coupler modulator and PPG unit. The result provides the spectrum beam and data wavelength. Based on the bit error rate, the power analysis was modelled.

[11] has presented the design of behaviour model-based comparator using switched capacitor SDM with relaxed DEM timing. By using simulink platform, the comparator based switched capacitor circuit is modelled. This simulink model is efficient to determine charging current at every branch. Sigma-delta- modulator is used to verify the behaviour model. The sampling rate achieves the best result by DEM timing model. This technique is also capable for analogue to digital converter model with pipelined architecture. While performing adaptive double sampling process the clock cycle timing is increased. This will lead to increase in quantization noise and spectrum noise.

[12] has presented the VLSI implementation of hardware algorithm for continuous data sorting approach. Here the problem of continuous data stream is reduced by bubble sorting algorithm. By tagging all these merged data streams into the sorter device, the partial sorting is performed. At each clock cycles, the new data is entered into the sorter device, and another word comes out through the output port. This algorithm is implemented in third order metal CMOS technology by this, the continuous data stream process is used to reduce the delay [18-19].

3. Proposed Method

Comparator design is a digital circuit, which is used in various applications of VLSI designs [13]. The proposed design of data comparator with bubble sorting algorithm
gives the efficient result as compared to the existing method by the way of overall system performance analysis. Here by the use of bubble sorting algorithm, the performance degradation is reduced by tagging the values [14]. The comparator circuit design with bubble sorting algorithm is given in Figure 1.

![Fig. 1: Proposed comparator with bubble sorting block diagram](image1)

The above Figure 1 shows that the design of 16-Bit comparator with bubble sorting algorithm. Initially the input X and Y with 16 bits of data is given to the comparator unit and it performs the comparison of both the input values as lesser, greater, and equals [15],[16]. These input values are arranged in the manner of tagged input array for performing bubble-sorting algorithm. This will reduce the time delay of proposed system.

![Fig. 2: Schematic view of proposed system functional blocks](image2)

Figure 2 shows the RTL schematic view of proposed comparator with bubble sorting technique. The input represents X and Y with each 16 bits of input data. X0 to X3 represents array of input to bubble sorting algorithm each with 4 bits of input data. The variable o1 to o4 represents the sorted output data. The sign of ‘equal’ represents the ‘X=Y’, ‘greater’ represents the ‘X>Y’, and ‘less’ represents the ‘X<Y’.

![Fig. 3: RTL schematic design of a comparator with bubble sorting algorithm](image3)

**Comparator Circuit Design**

The comparator as shown in Figure 3 is a combinational logic circuit which is used to performing comparison between the two input values and it gives the result as lesser, greater and equals [17].

![Fig. 4: RTL view of comparator design](image4)

The above Figure 4 represents the design of comparator with its functional block. The internal structure of data comparator consists of logic blocks, input and output blocks. Here two set of data is given to the comparator logic block, then it performs inverter operation for least data and greater data block directly takes the input from logic block. The equalizer block will compare the output of greater data block, and logic data block then it produces the output. Logical expression is given below,

\[
X < Y: \text{Least} = X' Y \\
X = Y: \text{Equal} = X'Y' + XY \text{ (Least + Greater)} \\
X > Y: \text{Greater} = XY' 
\]

**Bubble Sorting Algorithm**

The bubble-sorting algorithm is used in the comparator block for sort out the resultant value. The sorting is performed by comparing pair of adjacent elements. In these two values, the first bit is greater than second bit, operation performs swap. If not, it performs interchanging bit location.
The above Figure 5 represents the sorting algorithm with 16 bits of data block. The sorting time should be based on clocking function.

Table 1: 16 Bits Data Sorting by Bubble Sorting Algorithm

| STAGE | SORTING DATA | OPERATION |
|-------|--------------|-----------|
| 1     | 14 33 27 36 11 | Input data |
| 2     | 14 33 27 36 11 | 14<33     |
| 3     | 14 33 27 36 11 | 33 >27    |
| 4     | 14 27 33 36 11 | 33<36     |
| 5     | 14 27 33 36 11 | 36>11     |
| 6     | 14 27 33 11 36 | swap      |
| 7     | 14 27 11 33 36 | move      |
| 8     | 14 11 27 33 36 | move      |
| 9     | 11 14 27 33 36 | Sorted data |

The Table 1 represents the sorting data from comparator using bubble-sorting technique. This algorithm will repeatedly be sorting the adjacency element by comparing the two values, if it is in wrong order.

The logical operation of sorting algorithm is given below.

X>Y:
Greater = X1Y2’Y1’ + X2Y2’+X1X1Y1’X=Y:
Equals = X2’X1’Y2’Y1’ + X2’X1Y2’Y1 + X2X1Y2Y1+ X2X1’Y2Y1’

\[
= X2’Y2’ (X1’Y1’+X1Y1) + X2Y2 (X1Y1+X1’Y1’)
\]

\[
= (X1Y1+X1’Y1’) (X2Y2+X2’Y2’)
\]

\[
= (X1 XNOR Y1) (X2 XNOR Y2)
\]

X<Y:
Lesser = X2’Y2 + X1’Y2Y1 + X2’X1’Y1

The above Figure 6 shows the RTL technology schematic view of bubble sorting algorithm. Here the LUT and flip flop blocks are arranged based on logic input.

4. Results

Thus, the design of comparator using bubble-sorting algorithm is designed and simulated the results. The performance should be analyzed based on power, area, and delay.

The above Figure 7 shows that the simulate output of proposed comparator with bubble sorting system.

The above Figure 7 shows that the simulate output of proposed comparator with bubble sorting technique. The input X and Y having 16 bits of input and the output has three different comparison that is equal lesser and greater. The sorted bits also presented in output section, which is represented as ‘o’. Clocking signal is given for sorting algorithm as shown in Figure 8.
Fig. 8: Output for bubble sorting algorithm

The below mentioned tables (see Table 2, 3 and 4) represents the performance analysis report of proposed system which is based on power, area and delay factor. The Table 2 represents the area analysis based on device utilization summary report. Table 3 represents the delay analysis report by clock cycle. Table 4 is the power analysis report taken by Xilinx X Power analyser tool, based on current and voltage, the power factor is analysed (Static and Dynamic).

### Table 2: Device Utilization Summary

| SLICE LOGIC UTILITY          | USED | AVAILABLE |
|-----------------------------|------|-----------|
| No. Of Slice Registers      | 36   | 4800      |
| No. of FF                   | 36   | 129       |
| No. LUT logic              | 96   | 2400      |
| No. Of Bonded IOBs         | 68   | 102       |
| No. Of BUF                 | 1    | 16        |
| No. Of Occupied slices     | 34   | 600       |

The 1% of slice register is used in proposed method. The LUT pair of flip-flops is performed within the slice. The fully used LUT FF pair is 6% of utility. The 68% of Bonded IOBs is utilized for proposed system.

### Table 3: Delay Analysis

| PATH DELAY | TOTAL DELAY | GATE DELAY |
|------------|-------------|------------|
| 6.911ns    | 8.596ns     | 3.597ns    |

The delay analysis is calculated based on the clock time. The total delay is taken by adding delay of logical and routing unit. That is 2.187ns and 6.409ns respectively.

### Table 4: Power Analysis

| PARAMETER | POWER (MW) |
|-----------|------------|
| Signal Power | 25.5       |
| Supply power (Dynamic + Static) | 14.14 (0.45+13.69) |
| Vcc int     | 4.45       |
| Vcc aux     | 2.52       |
| Vcc         | 1          |

Supply power is calculated by adding static and dynamic power. In an on-chip device power, the clocks use 0.45mW power, that is dynamic power. Total peak memory used in this whole system is 4553MB. The total CPU compilation time is 5.29secs.

### Table 5: Comparison Result

| PARAMETER | EXISTING[1] | PROPOSED |
|-----------|-------------|----------|
| Power     | 32mW        | 14.14mW  |
| Area (IOBs) | 80          | 68       |
| Area (Slices) | 199        | 36       |
| Delay     | 15.331ns    | 8.596ns  |

As shown in Table 5, by comparing proposed method with existing method, the result achieves best throughput by area, delay and power reduction. By the use of bubble-sorting algorithm, the execution time is also reduced in CPU and real time execution.
5. Conclusion and Future scope
The design of proposed comparator with bubble sorting algorithm is developed using Verilog code and it is implemented by Xilinx ISE 14.5 suite, which achieves the best result as compared to the conventional method. This proposed method successfully allows getting the improved performance analysis result by area, power and delay factors. The bubble-sorting algorithm provides the best clocking time of CPU. It is a stable algorithm, used to minimize the execution time. By analyzing various conventional methods, the proposed system analysis concluded that the proposed technique is very efficient as compared with existing techniques, which is based on reduced area, minimum delay, and reduced power. In future, the bubble sorting algorithm is improved by reducing number ofadders and this proposed system is also used in various web browser applications.

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