A Novel Carrier-Based PWM Without Narrow Pulses Applying to High-Frequency Link Matrix Converter

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ABSTRACT In order to eliminate narrow pulses completely, this paper presents a novel carrier-based pulse width modulation (CBPWM) strategy applying to high-frequency link matrix converter (HFL-MC). Following the De-Re-couple idea, a single-phase to three-phase MC is equivalent to two full-bridge inverters according to the polarity of input voltage. The voltage of switches in two full-bridge inverters is analyzed and derived the duty cycles of switches according to the relationship between the state and the voltage of the switch. The duty cycles of three phases in the two inverters are integrated into a unified expression to generate the final modulation waves. A dual modulation strategy is proposed to compare modulation waves and a triangular carrier, which can achieve almost constant duty cycle of gating signals regardless of output voltage change. Therefore, the narrow pulses are eliminated fundamentally. Finally, the experimental results are given to show the advantages and the effectiveness of the proposed modulation strategy.

INDEX TERMS Matrix converter, high-frequency link, narrow pulses elimination, carrier-based pulse width modulation.

I. INTRODUCTION

Traditional inverters realize electrical isolation through a line-frequency transformer (LFT). Compared with LFT, the high-frequency transformer comes with some attractive features like small and compact footprint, high power density, and low system cost [1]–[3]. Thus, high-frequency link (HFL) based isolated converters as an alternative solution to LFT-based state-of-the-art converters have been studied extensively in recent years. In addition, since the matrix converter performs a direct AC to AC conversion, dispensing the traditional DC-link capacitors, it has been combined with HFL technology gradually [4]–[6]. At the same time, the combination of these two technologies puts forward higher requirements for control strategies.

Sinusoidal pulse width modulation (SPWM) is a classic and effective method [7]. In [8] and [9], HFL-MC is divided into two full-bridge inverters based on De-Re-coupling idea and a novel integration SPWM strategy is proposed, which achieved HFL-MC adaptive one-step commutation. In [10], a new PWM switching technique for three-phase grid-tie HFL-MC is proposed. This special SPWM strategy minimizes the number of switching transitions of the MC, and has the merits of high-power density and high efficiency compared with the conventional one. SPWM is easy to realize and convenient to control [11], but the modulation strategy has the inevitable drawback of low voltage utilization and high output current harmonic content [12], [13].

In order to solve the problem of voltage utilization, starting from Huber et al. [14], the space vector pulse width modulation (SVPWM) has been a recurring reference point for MC research [15]. Furthermore, in order to realize the smooth connection between MC and high-frequency technology, traditional SVPWM need to be improved accordingly. For example, for a two-stage charging system [16], a new modulation strategy for HFL-MC based on SVPWM and phase shift modulation is proposed. Applied to grid-connected system, this hybrid modulation strategy can control the power factor in the grid and manage the current in battery simultaneously.

On the other hand, the phenomenon of narrow pulses becomes more and more serious with the increasing of switching frequency regardless of the traditional strategies.
SWPM or SVPWM. So, restraining the generation of narrow pulses has become a research hotspot for scholars [17]. In [18] and [19], 3-zero vector modulation was proposed to preserve narrow pulses and improve the output voltage waveform by configuration 3 zero vectors between effective vectors. However, in the case of low voltage modulation ratio, due to the influence of commutation, the output voltage amplitude is much lower than excepted and the waveform is distorted. To address this question, in [20], an optimal SVPWM is introduced, which carries out the delay compensation of driving pulse according to the input voltage sector and the output current to eliminate the effect of commutation delay on output voltage. Thus, the technology of suppressing narrow pulses becomes more mature. In [21], an improved space vector modulation strategy is developed to restrain narrow pulses for implemented AC-DC matrix converters by replacing the zero space vectors with suitable pairs of active ones. In [22], the triple-zero-vector switching pattern and the single-zero-vector switching pattern are utilized by selecting an appropriate commutation time to suppress narrow pulses.

However, although the SVPWM has been improved a lot, the problem of narrow pulses dose not be eliminated fundamentally [23]–[25]. Besides, the SVPWM contains a large number of trigonometric functions, which is complicated in the calculation.

In order to eliminate narrow pulses completely, this paper proposes a new carrier-based PWM (CBPWM) strategy applying to HFL-MC. Compared with the previous strategies, the novel CBPWM has the following advantages:

1) The novel CBPWM strategy can balance the on-off time of each switch in one cycle.

2) The harmonic frequency is doubled while the switching frequency remains unchanged.

3) The expressions of modulation waves are very regular and the generation of gating signals is simple only some basic logical operations.

II. TOPOLOGY OF HFL-MC

The main circuit topology of HFL-MC is shown in Fig.1, in which the turn ratio of the HF transformer is 1 only playing the role of power transmission and galvanic isolation. The primary side of the high-frequency transformer is a basic H-bridge with 4 basic IGBT devices $S_i (i \in \{1, 2, 3, 4\})$ for generating high-frequency square waves and the secondary side is a MC with single-phase input and three-phase output. This single-phase to three-phase MC consists of six bidirectional switches, and each bidirectional switch cell is made up of two common IGBT devices controlled independently. There are 12 switches marked as $S_{ijk} (i \in \{a, b, c\}, j \in \{p, n\}, k \in \{1, 2\})$.

III. DERIVATION OF DUTY CYCLE

Because the input voltage of the MC is high-frequency AC square wave, the control strategy of conventional inverters needs to be improved. The input voltage waveform of HFL-MC is an AC square wave, and the pulse width is constant. When the voltage polarity of the secondary side of the transformer is positive, the first group of switches $S_{ijk} (i \in \{a, b, c\}, j \in \{p, n\})$ actually play the controlling role. And when the polarity is negative, the other group of switches $S_{ijk}$ play the same role. Therefore, inspired by the full-bridge inverter, the single-phase to three-phase MC is naturally equivalent to two full-bridge inverters.

Thus, the first switch group composed by six switches $S_{ijk} (i \in \{a, b, c\}, j \in \{p, n\})$ is the simplified model of MC in the first half cycle, as shown in Fig.2(a) and the other six switches $S_{ijk} (i \in \{a, b, c\}, j \in \{p, n\})$ constitute the second switch group in the second half cycle, as shown in Fig.2(b). Then, the MC is equivalent to two full-bridge inverters in the whole cycle, which reduces the difficulty of control.

Because the MC uses bidirectional switches, it can be equivalent to two groups of conventional voltage source inverters in the circuit structure, some characteristics of traditional inverters still exist in MC.

In the first half cycle of high-frequency square wave, bidirectional switches of the MC are dominated by the first switch group. In addition, the three-phase LC filter and load are combined to compose the three-phase comprehensive load $Z_l (i \in \{a, b, c\})$. Therefore, the circuit topology is simplified a three-phase voltage source inverter (VSI),
is used to establish two equations of the A-phase leg

\[
\begin{align*}
U_d &= u_{a_{j1}} + u_{aO} - u_{bO} + u_{b_{j1}} \\
U_d &= u_{a_{j1}} + u_{aO} - u_{cO} + u_{c_{j1}}
\end{align*}
\]  

(1)

Supplement an equation expressed by A-phase parameters

\[
\begin{align*}
u_{a_{j1}} &= u_{a_{j1}} + u_{aO} - u_{bO} \\
\end{align*}
\]  

(2)

By analyzing (3) and (4) with Fig. 3, it can be concluded that the sum of switch voltage and the output voltage of each phase can be expressed by (5) at any time

\[
u_{a_{j1}} + u_{aO} = u_{b_{j1}} + u_{bO} = u_{c_{j1}} + u_{cO}
\]  

(5)

Because the output voltage is a standard three-phase sinusoidal wave, following (6), it can be seen from equation (5) that the trend of \(u_{aO}\) varies with the switches’ status.

\[
\begin{bmatrix}
u_{aO} \\
u_{bO} \\
u_{cO}
\end{bmatrix} = U_{om} \begin{bmatrix}
\cos \omega_t t \\
\cos (\omega_t t - 2\pi/3) \\
\cos (\omega_t t + 2\pi/3)
\end{bmatrix}
\]  

(6)

where, \(U_{om}\) and \(\omega_t\) are the amplitude of the output voltage and the output voltage angular frequency respectively.

In order to maximize the voltage transmission ratio, it is necessary to maximize the voltage of DC bus \(u_{pO}\). Therefore, it is be set that when the output voltage of phase A is maximize in three phases, the switch \(S_{ap1}\) is in a closed state. And switches \(S_{bp1}\) and \(S_{cp1}\) are set in the same way. It is concluded that the DC bus voltage \(u_{pO}\) is always equal to the maximum phase voltage in the first half period. It can be derived as (7)

\[
u_{pO} = \max (u_{aO}, u_{bO}, u_{cO})
\]  

(7)

Considering (5) and (7), the voltage expression of switch \(S_{ap1}\) is obtained as follows:

\[
u_{a_{j1}} = \max (u_{aO}, u_{bO}, u_{cO}) - u_{aO}
\]  

(8)

Therefore, a conclusion can be drawn that the voltage of the switch \(S_{ap1}\) changes according to the law (8), the expected standard sinusoidal wave can be output at the AC side.

Next, the formula of the duty cycle can be derived based on switches voltage. When the switch \(S_{a_{j1}}\) is on and \(S_{a_{j1}}\) is off, the voltage \(u_{aO}\) between the point a and the imaginary neutral point \(O'\) is \(0.5U_d\) and the voltage \(u_{aO'}\) is \(-0.5U_d\) on the contrary switch state. Thus, the average voltage between point a and the imaginary neutral point \(O'\) is (9)

\[
u_{aO'} = \frac{U_d}{2} - (1 - da) \frac{U_d}{2}
\]  

(9)

where \(da\) is the duty cycle of the upper leg switches of phase A.

In addition, the voltage between the bus p and the imaginary point \(O'\) is a constant.

\[
u_{pO'} = \frac{U_d}{2}
\]  

(10)
Combining (9) and (10), the voltage between the bus p and the point a is obtained in duty cycle $d_a$

$$u_{pa} = u_{pO} - u_{aO} = (1 - d_a) U_d$$  \hspace{1cm} (11)

In Fig.3, the voltage of switch $S_{ap1}$ is equal to $u_{pa}$. Thus, considering (8) and (11), the duty cycle of switch $S_{ap1}$ is expressed by

$$d_a = 1 - \frac{\max (u_{aO}, u_{bO}, u_{cO}) - u_{aO}}{U_d}$$  \hspace{1cm} (12)

The analysis method of switches $S_{bp1}$ and $S_{cp1}$ is the same as that of $S_{ap1}$, and then the duty cycles of the other two legs $d_b$ and $d_c$ can be derived in the same way.

$$d_b = 1 - \frac{\max (u_{aO}, u_{bO}, u_{cO}) - u_{bO}}{U_d}$$  \hspace{1cm} (13)

$$d_c = 1 - \frac{\max (u_{aO}, u_{bO}, u_{cO}) - u_{cO}}{U_d}$$  \hspace{1cm} (14)

And according to the basic principle of the circuit, the duty cycles of the lower-leg switches $S_{an1}$ ($i \in \{a, b, c\}$) and the upper complement each other.

On the other hand, in the second half cycle, the matrix converter is simplified to the second switch group, shown in Fig.2(b). And for A-phase load, the switch $S_{an2}$ of the bus n becomes the main switch replaced $S_{ap1}$. The ultimate goal is to make the on-off time of the switch equal in a cycle, which is equivalent to the connection time of the load and power supply is 0.5$T_S$. In order to achieve this connection time, the duty cycles of main switches in the second half cycle should be $d_a$. Therefore, the duty cycle of $S_{an2}$ is $d_a$, and the duty of the other switch $S_{ap2}$ on the same leg is a complement.

It is easy to conclude that the duty cycle of switches $S_{ap1}$ and $S_{ap2}$ are both $d_a$, although they are in different half cycles. Besides, in the first half cycle, the switch $S_{ap1}$ plays the main role, and the state of $S_{ap2}$ has little effect on the current, but they are opposite in the second. Thus, set the duty cycles of switches $S_{ap1}$ and $S_{ap2}$ in the whole cycle to $d_a$, which can eliminate narrow pulses without increasing the difficulty of control. Meanwhile, the duty of n-bus switches $S_{an1}$ and $S_{an2}$ is $d_a$.

However, when the gating signals of $S_{ap1}$ and $S_{ap2}$ are the same, the commutation problem will occur. According to the previous strategies, when $S_{ap1}$ plays the control role, the state of $S_{ap2}$ is on, providing a path for current. But there is no switch in the on state to provide the path in the novel strategy. In order to solve the commutation problem, the four-step commutation strategy is applied.

Use the same method to distribute the duty cycle of each switch of the other two legs.

**IV. CBPWM STRATEGY**

Generally speaking, SVPWM improves the efficiency of power conversion greatly, but there are a large number of trigonometric functions in the calculation of the duty cycle, which is complicated. Thus, using the derived duty cycle, the carrier modulation strategy is adopted. In addition, PWM wave is a square wave with the pulse width changing, and the law of change is the same as that of modulation amplitude value. According to this principle, the modulation waves with amplitude of 1 can be represented by duty cycle function. Therefore, the modulation waves are obtained as follows:

$$u_{ti} = 1 - \frac{\max (u_{aO}, u_{bO}, u_{cO}) - u_{iO}}{U_d} \quad (i \in \{a,b,c\})$$  \hspace{1cm} (15)

The width of desired driving signal is a constant in each period, so the modulation waves in the second half period needs to be slightly changed according to the different forms of the carrier at this time. But it is worth mentioning that no matter how the carrier form changes, the modulation waves of the second half cycle needs to meet the principles:

1) The opening time consisted of two half cycles must be equal in each cycle.
2) In the whole period, the operation mode of driving pulse generated by carrier wave and modulation waves must be consistent.

In the first half cycle of the high-frequency square pulse, the carrier is a saw-tooth wave. Its period is half of the alternating square wave and the amplitude varies from 0 to 1. On the other hand, assuming that the carrier wave in the second half cycle is the same as the first, the carrier of the whole cycle can be derived as (16).

\[
\begin{align*}
    u_{\text{carr}} &= \begin{cases} 
    \frac{2}{T_S} t, & 0 \leq t < \frac{T_S}{2} \\
    \frac{2}{T_S} t - 1, & \frac{T_S}{2} \leq t < T_S 
    \end{cases} 
\end{align*}
\] (16)

According to the above analysis, taking phase A as an example, the expression of modulation waves in two half cycles is exactly the same and the modulation period \(T_S\) can be divided into four intervals as shown in Fig. 4. The second and third intervals compose a continuous pulse, which the width is \(0.5T_S\). At the same time, the fourth interval and the first interval of the next cycle constitute the off time. For this analysis, the driving signal of switches \(S_{\text{ap}1}\) and \(S_{\text{ap}2}\) is \(S_a1\) in the first half cycle and \(S_a2\) in the second.

\[
S_{a1} = \begin{cases} 
1, & u_{\text{carr}} \geq u_{\text{ra}} \\
0, & u_{\text{carr}} < u_{\text{ra}} 
\end{cases} 
\] (17)

\[
S_{a2} = \begin{cases} 
1, & u_{\text{carr}} < u_{\text{ra}} \\
0, & u_{\text{carr}} \geq u_{\text{ra}} 
\end{cases} 
\] (18)

Analyzing (17) and (18), the two calculation methods are different in different half cycles, which violate the two principles. Thus, the carrier \(u_{\text{carr}}\) needs to be changed.

Set the first half cycle carrier to remain unchanged, and change the second half cycle carrier to a negative slope saw-tooth wave. After this improvement, the first and the second half cycle carriers are combined into an isosceles-triangular wave, which does not cause extra burden to the hardware circuit. So, the carrier changes to (19).

\[
\begin{align*}
    u_{\text{carr}} &= \begin{cases} 
    \frac{2}{T_S} t, & 0 \leq t < \frac{T_S}{2} \\
    -\frac{2}{T_S} t + 2, & \frac{T_S}{2} \leq t < T_S 
    \end{cases} 
\end{align*}
\] (19)

Since the carrier of the second half cycle has changed, according to the above principles, the modulation wave in the second half cycle can be concluded by (20).

\[
u_{\text{ra}}' = 1 - u_{\text{ra}} \] (20)

In this way, the second half cycle modulation wave \(u_{\text{ra}}'\) will change in linkage with the first half cycle modulation wave \(u_{\text{ra}}\), so that the on time of each switch is always \(0.5T_S\). Thus, another advantage is that the novel CBPWM strategy needs to modulate twice in a cycle, but the two pulses are always adjacent, which integrates into a wider driving signal. It is means that although the action frequency of the switches remains unchanged during the operation of the matrix converter, the output side achieves the effect of frequency doubling. The higher-frequency results are obtained without increasing the hardware burden. Therefore, the proposed modulation strategy makes the matrix converter have better characteristics. Fig. 5 shows the diagram of gate pulse with dual modulation waves. The driving signal of the upper leg follows (21).

\[
S_a = \begin{cases} 
1, & u_{\text{carr}} \geq u_{\text{ra}} \\
0, & u_{\text{carr}} < u_{\text{ra}} 
\end{cases} 
\] (21)

Next, the generation process of driving signal is introduced in detail. Fig. 6 shows the generation process of the driving signal of A-phase leg. In order to generate the driving signal \(S_a\) of switches \(S_{\text{ap}k}\) \((k \in \{1, 2\})\), comparing two modulation
TABLE 1. Specifications and parameters of HFL-MC.

| Symbol | Description                                      | Value  |
|--------|--------------------------------------------------|--------|
| $U_d$  | the voltage of DC power supply                   | 200V   |
| $U_{max}$ | Theoretical value of maximum voltage            | 115V   |
| $f_s$  | switching frequency                              | 10kHz  |
| $f_o$  | output voltage frequency                         | 50Hz   |
| $n$    | ratio of high frequency transformer              | 1      |
| $R$    | load resistances                                 | 12Ω    |
| $L_r$  | filter inductors                                 | 0.4mH  |
| $C_r$  | filter capacitors                                | 20µF   |

waves $u_{ra}$ and $u'_{ra}$ with the carrier $u_{car}$, respectively following (21). And the comparison results are named $g$ and $g'$. It is worth noting that the driving signal $S_a$ changes state once in a cycle but is asymmetrical with the carrier. In this case, the final driving signal $S_a$ can be obtained by some simple logic operations on signals $g$ and $g'$. The switching pulse of the front stage H-bridge is the signal $S_1(S_4)$, which is a square wave with the same frequency as the carrier and the duty cycle of 0.5. And the other signal $S_2(S_3)$ is a complement. It can be seen from Fig.6 that the driving signal $S_a$ will shift with the change of modulation waves in a cycle, but the pulse width will remain unchanged. Therefore, the four switches on the A-phase leg switch regularly, and there is no narrow pulse at all.

The other two legs are similar to phase a, so the same analysis process can generate their own pulse signals $S_b$ and $S_c$.

V. EXPERIMENTAL RESULTS

To verify the correctness and effectiveness of the double modulation waves based CBPWM proposed in this paper, the HFL-MC is built in the laboratory as shown in Fig.7. The prototype consists of a controller board, HFL-MC circuit, output filter circuit and three-phase load. The controller board that executes the control program includes a high-performance DSP TMS320F28335 and a Field-Programmable Gate Array EP4CE115F23I7N. The experimental parameters are all listed in Table 1.

![FIGURE 8. The results of the novel CBPWM strategy when the modulation ratio $m = 1$ (a) three-phase voltage waveform after filtering (b) driving signals of HFL-MC (c) the phase voltage $u_a$ of HFL-MC before filtering (d) the result of harmonic analysis.](image)

![FIGURE 9. Set a threshold value of 2µs for the drive signals generated by the traditional SVPWM strategy.](image)
When the modulation ratio $m = 1$, the operation results of the HFL-MC controlled by the novel CBPWM strategy are shown in Fig.8. Fig.8(a) shows the waveform of the output three-phase voltage after filtering. It can be seen that the waveform is a standard three-phase sinusoidal wave and the voltage amplitude is close to the expected value. Because the switches and the filter have internal resistance and the harmonics are filtered out, the output voltage amplitude is less than the ideal value slightly. The load is a symmetrical resistance, so the current waveform is also a sinusoidal wave and the phases of voltage and current is the same. Fig.8(b) shows the driving signals of HFL-MC. The duty cycles of all switches, including the front stage, is approximately 0.5, which realizes all the driving signals can be used to bring the output results closer to the theoretical values. Therefore, the good voltage waveform and the regular pulse signals show that the novel CBPWM strategy proposed in this paper is reasonable.

Fig.8(c) is the actual waveform of the output voltage $u_a$ before filtering. It can be seen that $u_a$ is a pulse wave with a lot of harmonics. Set the maximum harmonic order of Fourier analysis to 400, and the result of this waveform is shown in Fig.8(d). The amplitude of the fundamental component is 110.7V, which is slightly less than the theoretical value due to the loss of switching action and filtering. Although the harmonic content is relatively high, the harmonic frequency is very concentrated and there is almost no low-order harmonic. It is worth noting that the operating frequency of each switch in the HFL-MC is 10kHz, but the harmonic frequency is concentrated at 20kHz, which is completely consistent with the above analysis.

Therefore, the voltage $u_a$ with only high frequency component can be easily transformed into a standard waveform by the LC filter.

In order to further demonstrate the advantages of the novel CBPWM strategy, traditional SVPWM strategy is used as a comparison. It is worth noting that the action of the switch has a certain time in practice, and in order to ensure the safe operation of MC, each commutation has a fixed time. So, some narrow pulses in the ideal driving signal cannot be realized. Therefore, set the minimum threshold value of pulse width to 2µs and the processing result of ideal driving signal is shown in Fig.9. Since an oscilloscope has only four input ports, only the processing results of the phases a and b are displayed. The driving signals $S'_a$ and $S'_b$ are the ideal signals generated by SVPWM strategy, which contains a lot of narrow pulses. The narrow pulses with width less than 2µs are filtered by threshold value and the actual signals $S_a$ and $S_b$ are generated.

The filtered pulse signals are used to drive the HFL-MC, and Fig.10 shows the output results of the SVPWM with the same components. It can be seen from Fig.10(a) that the voltage waveform is symmetric, but the amplitude is lower than that in Fig.8(a). Fig.10(b) shows that the duty ratio of the driving signal varies greatly and still contains a large number of narrow pulses. The harmonic analysis of the a-phase voltage before filtering by the traditional strategy is shown in Fig.10(d). Compared with Fig.8(d), there is much difference between the fundamental amplitude and harmonic rate. After removing narrow pulses, the amplitude of the waveform decreased greatly, and more harmonics were produced. Besides, with the increase of switching frequency,
more narrow pulses will be produced by traditional strategy and the threshold value also influences the character of HFL-MC. Therefore, the maximum output voltage of matrix converter controlled by the traditional strategy is much smaller than the theoretical value.

In addition, the harmonic frequency shown in Fig.10(d) is only the switching frequency. Therefore, it is one of the reasons why the traditional PWM is not as good as the new strategy.

In order to further study the characteristics of the novel CBPWM strategy and the traditional SVPWM, the two strategies are compared and different threshold values are considered. The results are shown in Fig.11. The modulation ratio is selected from 0.5 to 1 and the ordinate is the ratio of the amplitude of the output voltage to the theoretical value. Set the ignored narrow pulse threshold to 2μs and 3μs, respectively. It can be seen from the figure that the output of the new method is higher than that of the traditional SVPWM as a whole. When the modulation ratio is low (e.g. \( m = 0.5 \)), the curves (III) and (V) coincide, which shows that the pulse widths are greater than the threshold. With the increase of the modulation ratio, the current in circuit becomes larger, which leads to the increase of switching loss. So, the voltage conversion rate is decrease slightly. When the modulation ratio is very high (\( m > 0.8 \)), the traditional method will produce many narrow pulses and the larger the threshold value is, the lower the output voltage will be. But the output voltage of the new CBPWM only has running loss, so it is better than the tradition.

In addition, the switching frequency is increased to 20kHz to study the relationship between output voltage and the switching frequency. The higher the switching frequency is, the harmonic amplitude is lower. So, curve (II) is slightly higher than curve (I) in Fig.11. But the previous SVPWM does not have this capability. The narrow pulse is related to switching frequency and modulation ratio. It can be seen from (III), (IV) and (V) that the increase of frequency or \( m \) will cause more narrow pulses to be ignored and the output voltage will be reduced.

The above experiments show that fine output performances can be got by using the proposed modulation strategy and the driving signals of HFL-MC are completely free of narrow pulses.

VI. CONCLUSION

In this paper, a novel CBPWM strategy for HFL-MC is proposed, which can completely eliminate the narrow pulse of gating signals in the whole range of modulation ratio regardless of switching frequency changing. Compared with the previous SVPWM strategy, the novel CBPWM strategy is not affected by the narrow pulse, so it has a higher voltage transfer ratio in practice. And the dual modulation strategy can increase the harmonic frequency without changing the switching frequency. In addition, the modulation waves are concise and regular, which is no need for trigonometric function calculation and sector judgment. Therefore, the proposed strategy has practicality and high efficiency in practical application. Finally, the effectiveness and feasibility of this method are verified by experiments.

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