Low-power-consumption organic field-effect transistors

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Abstract

At present, the electrical performance of organic field-effect transistors (OFETs) has reached the level of commercial amorphous silicon. OFETs show considerable application potential in artificial intelligence, deep learning algorithms, and artificial skin sensors. The devices which can operate with high performance and low power consumption are needed for these applications. The recent energy-related improvement to realize low-power consumption OFETs were reviewed, including minimizing operating voltage, reducing subthreshold swing, and decreasing contact resistance. In this review, we demonstrate breakthroughs in materials and methods to decrease power consumption, providing a promising avenue toward low-power consumption organic electronics.

1. Introduction

Following the seminal paper from Tsumura, in which he demonstrated the first polythiophene-based field-effect transistor in 1986, organic field-effect transistors (OFETs) have received tremendous developments due to the intriguing properties of organic semiconductors, such as flexibility, stretchability, biocompatibility, solution processibility, and low cost \[1—4\]. To date, the field-effect mobility, which is the main character of an OFET device, has increased over 40 cm\(^2\) V\(^{-1}\) s\(^{-1}\). With the improvements in electric performance, the large-scale integration of OFETs have facilitated impressive application demonstrations, including organic light-emitting diode displays, radiofrequency identification tagging, and artificial skin \[5—12\]. To meet the future demand for product miniaturization and high properties, the number and density of transistors need to be increased, thus the heat energy caused by the power dissipation will lead to the degradation of organic materials and the life reduction of devices \[13—19\]. In addition, high power consumption limits the applications of most portable electronics which need an external battery \[20—23\]. All of these demands in applications require transistors to operate with extremely low-power consumption. However, power dissipation of most OFETs suffers from a high operating voltage typically a few tens of volts, which has a quadratic effect on dynamic power consumption \[3, 24—29\]. Furthermore, transistors sizes are also now approaching the point where quantum effects become appreciable, which can lead to an increased gate leakage current due to quantum tunneling and, in turn, an increased static power consumption.

Achieving extremely energy-efficient OFETs is an essential prerequisite for commercial applications. After years of expansive development, significant advancements have been made in fabricating high quality dielectrics, thus reducing the operating voltage and leakage current. Furthermore, the subthreshold slope, which is negative correlation with switching efficiency, has witnessed a significant decrease driven by the process optimization and interface engineering \[6, 30—32\]. Additionally, the contact between semiconductors and electrodes has remarkable reduction, which in turn leads to a low heat dissipation \[33—42\]. Therefore, low-power consumption OFETs are being skyrocketed as a research hotspot. A timely review in this field is not only scientific importance but also technologically imperative.

In this article, we present a comprehensive overview of the recent achievements in low-power-consumption OFETs. First, we focus on dielectric materials used for low-voltage OFETs. Second, we provide an introduction on the reduction of subthreshold slope. Third, we discuss the methods to decrease contact resistance. Finally, we
discuss other low-power-consumption organic devices. This review aims to provide an up-to-date and systematic evaluation covering all energy-related aspects of OFETs.

2. Dielectric materials for OFETs with low-power consumption

Reducing the power consumption of OFETs, which can be achieved by decreasing the applied gate voltage ($V_g$), is necessary to realize the practical applications [43]. The $V_g$ can be expressed as follows:

$$V_g = \frac{Q}{C} = \frac{Qd}{\kappa \varepsilon_0},$$

where $Q$ is the charge density, $C$ is the capacitance of the dielectric, $d$ and $\kappa$ are the thickness and permittivity of the dielectric, respectively, and $\varepsilon_0$ is the permittivity of vacuum [5]. Based on the aforementioned equation, one effective way to reduce the gate voltage is to increase gate dielectric capacitance, which is inversely proportional to $d$ and proportional to $\kappa$. Hence, applying high-$\kappa$ dielectrics and utilizing ultrathin dielectrics are the two main methods to realize high capacitance [44–48]. These alternative materials of dielectrics include, but are not limited to, high-$\kappa$ oxides and polymers, self-assembled monolayers, and electrolytes. In the following sections, we highlight these exemplary materials reported in the literatures (table 1).

2.1. High-$\kappa$ dielectrics

High-$\kappa$ materials, such as Al$_2$O$_3$ ($\kappa \sim 10$), HfO$_2$ ($\kappa \sim 20$), and TiO$_2$ ($\kappa \sim 41$), have been extensively applied to fabricate low-voltage OFETs. Klauk et al demonstrated the OFETs with Al$_2$O$_3$/self-assembled monolayer (SAM) as the dielectrics on flexible, transparent polyethylene naphthalate [5]. The Al$_2$O$_3$ was fabricated by exposing the thermally evaporated Al to oxygen and SAM was grown atop it to avoid high leakage current. A capacitance of 0.7 $\mu$F cm$^{-2}$ and leakage current of $5 \times 10^{-8}$ A cm$^{-2}$ were measured for the dielectrics at an applied voltage of 2 V. As a result, the operating voltages of the p- and n-type OFETs were 1.5 V and 3 V, respectively. The static power dissipation of the complementary was less than 1 nW per logic gate, which indicated the successful production of low-power organic circuits with Al$_2$O$_3$ as the dielectrics. More recently, Tetzner et al demonstrated a room-temperature solution process to fabricate OFETs based on a semiconductor of FS111 [49]. The dielectric (HfO$_2$) was prepared by a sol-gel technique, followed by using photonic curing instead of annealing at 600 °C to suppress the leakage current. The electronic measurements revealed a high dielectric constant of 26. The OFETs exhibited field-effect mobilities of 1 cm$^2$ V$^{-1}$ s$^{-1}$, low subthreshold swing (110 mV decade$^{-1}$), and low operation voltages (< 2 V). Additionally, an electrochemical reaction that processes fully at room temperature can be used for high-quality dielectric formation. Metals used as anodes in aqueous electrolytes can form densely packed oxide thin films through anodization. More importantly, the thickness of the oxide was readily controlled by adjusting the anodization voltage. Jinno et al demonstrated the low-voltage OFETs based on an anodized TiO$_2$/SAM dielectric [50]. The dielectric was fabricated via anodization to form a 40 nm thick oxide layer, followed by the formation of a phosphonic acid layer through self-assembly. The TiO$_2$ with high-$\kappa$ nature

| Materials | Methods | $C_i$ [nF cm$^{-1}$] | $\varepsilon_r$ | Saturated $V_g$ [V] | Organic semiconductor | Mobility [cm$^2$ V$^{-1}$ s$^{-1}$] | References |
|-----------|---------|---------------------|----------------|---------------------|----------------------|-----------------------------|------------|
| Al$_2$O$_3$/SAM | O$_2$ plasma | 370 | 9 | 4 | C$_{60}$-BTBT | 9.8 | [44] |
| Al$_2$O$_3$/SAM | O$_2$ plasma | 700 | 3 | 6 | F$_{65}$CuPc | 0.02 | [5] |
| HfO$_2$ | Sol-gel | 111 | 25 | 6 | PTCDI-C$_{13}$ | 0.27 | [47] |
| HfO$_2$ | Sol-gel | -380 | 26 | 2 | FS111 | 1 | [49] |
| TiO$_2$ | Anodization | 676 | 1.2 | Pentacene | 0.15 | [47] |
| TiO$_2$/SAM | Anodization | 300 | 1 | DNTT | 1.2 | [50] |
| PVA | Spin-coating | -21.9 | -6.2 | 5 | P3HT | 0.12 | [51] |
| SBA | Sol-gel | 2000 | 170 | 5 | Pentacene | 0.141 | [46] |
| SBA | Sol-gel | 2000 | 170 | 3 | NTCDI | 0.04 | [46] |
| P(VDF-TrFE) | Spin-coating | 35 | -2 | P(NDI$_2$OD-T$_2$) | 0.27 | [52] |
| PS/C-NPs | Spin-coating/ sputtering | 51 | 4 | Pentacene | 0.3 | [41] |
| PhO-OTS | Self-assembly | 900 | 2 | Pentacene | 1 | [53] |
| Alk/Stb/Cap | Self-assembly | 2500 | 16 | 1 | F$_{65}$CuPc | 0.06 | [54] |
| P3HT | iCVD | 70–78 | 2.2 | 5 | DNTT | 0.87 | [36] |
| P3HT | iCVD | 70–78 | 2.2 | 5 | PTCDI-C$_{13}$ | 0.71 | [36] |
| PEO-LiClO$_4$ | Spin-coating | 5000 | 2 | Pentacene | 0.01 | [55] |
| [EMIm][TFSA] | Spin-coating | 10 000 | 2 | P3HT | 1.3 | [56] |
| P(VPA-AA) | Spin-coating | 10 000 | 1 | P3HT | 0.012 | [57] |
boosted the unit area capacitance of dielectrics to 3 \( \mu \text{F cm}^{-2} \) and reduced the leakage current (figure 1(a)). Consequently, the thermal evaporated OFETs turned on at the gate voltage of \(-1 \text{ V}\) gate bias (figure 1(b)).

Apart from oxide dielectrics, applying high-\(\kappa\) polymers is also an efficient way to reduce the operating voltage of OFETs [31, 58]. Poly(vinyl alcohol) (PVA) with dielectric permittivity of approximately 7 appeared as a candidate in OFET fabrication. However, PVA has the drawback of instability with moisture because it contains hydroxyl groups. Thus, one common way to improve PVA stability is to crosslink with ammonium dichromate (AD) [39]. The best performance of poly(3-hexylthiphenene)-based OFETs was observed with mobility of 0.12 cm\(^2\) V\(^{-1}\) s\(^{-1}\) and operation voltage of \(-5 \text{ V}\) while the ratio of AD/PVA was 25% / 75% [51]. Furthermore, incorporating high-\(\kappa\) nanoparticles into polymer can also be utilized to enhance the capacitance of the dielectrics [60–64]. The polymeric-nanoparticle composites not only include the merits of inorganic high-\(\kappa\) materials, but also retain the advantages of organic counterparts, such as flexibility and easy processability [62, 65–69]. In 2017, Dastan et al prepared PVA and TiO\(_2\) nanoparticles as the hybrid dielectrics by spin-coating, showing a low leakage current of \(2 \times 10^{-12} \text{ A}\) [70]. Moreover, high-\(\kappa\) ferroelectric polymers, such as polyvinilidenefluoride-trifluoroethylene (P(VDF-TrFE)), having a promising high dielectric permittivity, are potential candidates as the dielectrics in OFETs. However, the OFETs with these polymers as the dielectrics have the drawback of large hysteresis due to the ferroelectric effect [71]. Baeg et al studied the low-hysteresis OFETs with P(VDF-TrFE) and polymethyl methacrylate (PMMA) blend as the dielectrics [52]. The ferroelectric effect caused by the formation of ferroelectric \(\beta\)-phase crystals can be suppressed by adding PMMA. As a result, low hysteresis and low operation voltage (< 2 V) were realized in the blend dielectrics with P(VDF-TrFE):PMMA proportion of 7:3.

2.2. Self-assembled monolayers and multilayers

Other than the above mentioned utilizing high-\(\kappa\) dielectrics in the OFETs, a high capacitance can be realized by applying thin dielectrics. However, this would inevitably result in a markedly improved leakage current due to the defects and tunneling effects at the dielectrics. It turns out that the current leakages can be suppressed by using a highly ordered self-assembled monolayers (SAMs), showing excellent insulating behavior with leakage currents on the order of approximately \(10^{-8} \text{ A cm}^{-2}\) [72–74]. Halik et al found that (18-phenoxycotadecyl) trichlorosilane can be densely packed on a heavily doped silicon wafer due to the \(\pi-\pi\) interactions between the phenoxy end groups of adjacent molecules [53]. With a thickness of 2.5 nm, these dielectrics provided a gate capacitance of 0.9 \(\mu \text{F cm}^{-2}\) to afford the OFETs with a field-effect mobility of 1 cm\(^2\) V\(^{-1}\) s\(^{-1}\), \(I_{\text{on}}/I_{\text{off}} \approx 10^6\), and operation voltages of 2 V.

In addition to the self-assembled monolayers, self-assembled multilayers have been extensively used as dielectrics in OFETs. Marks et al reported low-voltage OFETs with a three-dimensional-crosslinked dielectric deposited by a solution-phase method [34]. The robust dielectrics comprised as follows: hydrocarbon chains, stibazolium layers, and octachlorotrisiloxane layers. Different combinations with the three kinds of SAMs were tested, and the dielectric (hydrocarbon chains + octachlorotrisiloxane layers + stibazolium layers + octachlorotrisiloxane layers) showed the optimal performance in terms of low leakage \((10^{-9} \text{ A cm}^{-2})\), high capacitance \((2.5 \mu \text{F cm}^{-2})\), and high dielectric constant \((16)\). The OFETs with 2.5 nm thick dielectrics can be operated at low threshold voltages (< 1 V).

2.3. Electrolyte dielectrics

Besides high-\(\kappa\) materials and SAMs, a large capacitance can be realized by using electrolytes as the dielectrics due to the formed electric double layers (EDLs) as showed in figure 2(a). By applying a gate voltage, the ions in electrolytes will migrate in the dielectrics and eventually accumulate at the gate-dielectric and dielectric-
semiconductor interfaces on the side of the dielectrics. The charges will then be induced and accumulated at the gate-dielectric and dielectric-semiconductor interfaces on the side of the gate electrodes and semiconductors, respectively, thus the formation of EDLs at each interface [75]. EDLs can be regarded as a nanometer-thick capacitor because the distance between ion and charge layers is approximately 1.0 nm. Therefore, the capacitance value above 1 \( \mu \)F cm\(^{-2}\) is commonly attainable with electrolytes. In the following section, we briefly categorize three kinds of electrolytes, including ionic liquid, ion gel, and polyelectrolytes.

Ionic liquid electrolytes have a set of excellent performance, such as high ionic conductivity, negligible volatility, non-flammability, and thermal stability. Panzer et al utilized a solution-processable PEO-LiClO\(_4\) dielectrics to realize a high capacitance of 5 \( \mu \)F cm\(^{-2}\) [55]. As a result, the operating voltage of the pentacene-based OFETs was only 2 V (figure 2(b)). In addition to ionic liquid electrolytes, ion gel electrolytes have also been chosen as dielectrics to realize a low operating voltage. Lee et al reported 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl) amide ([EMI][TFSI]) based on poly(vinylidene fluoride-co-hexafluoropropylene) (PVDF-HFP) as the dielectrics [56]. The ion gel films can be easily cut and transferred due to their high elasticity. The films can be directly laminated on the top of the semiconductors without the damage. The prepared ion gel dielectrics exhibited a high capacitance of 10 \( \mu \)F cm\(^{-2}\) (figure 2(c)) and the ion gel-gated OFETs can be operated at a low voltage of 2 V and a high on/off ratio of approximately 10\(^6\). Besides, an interesting class of electrolytes called polyelectrolytes have been applied in OFETs. Herlogsson et al recently reported a novel solid-state polyanionic proton-conducting electrolyte based on a random copolymer of vinyl phosphonic acid and acrylic acid (PVPA-AA) [57]. OFETs based on a P(VPA-AA) gate dielectric and P3HT semiconductor were fabricated, operating at an applied voltage of \(-1\) V and demonstrating the short response time of 300 \( \mu \)s.

3. Steep subthreshold slope for reducing power consumption

Reducing the operation voltages by enlarging the capacitance of dielectrics facilitates extraordinary improvements in achieving low-power-consumption OFETs. The subthreshold slope (SS), which determines the gate voltage amount necessary to increase the drain-source current by an order of magnitude in the subthreshold region, must be steep to further reduce the operation voltages [76–78]. The SS is expressed as follows:
Table 2. Recently reported low SS of OFETs.

| Semiconductor | Dielectric | Methods | $C_i$ [nF cm$^{-2}$] | $D_i$ [cm$^{-2}$ eV$^{-1}$] | SS [mV dec$^{-1}$] | References |
|---------------|------------|---------|----------------------|-----------------------------|-------------------|------------|
| Rubrene       | CYTOP      | PVT     | 4.71                 | $3 \times 10^6$            | 65                | [80]       |
| dif-TEADT     | CYTOP      | —       | 1.30                 | $1 \times 10^6$            | 65                | [77]       |
| Pentacene     | La$_2$/SiO$_2$ | RF sputtering | 340               | $1 \times 10^{12}$       | 75                | [81]       |
| DNTT          | AIO$_x$/SAM | —       | 600                  | $2.79 \times 10^{10}$     | 65                | [82]       |
| PDVT-8        | AIO$_x$    | Ink-jet printing | —      |                 | 90                |            |
| DPA           | SAM/AIO$_x$ | Template stripping | 250     | $1.81 \times 10^{11}$ | 66                | [83]       |
| C$_8$-BTBT    | P(VDF-TrFE-) | Spin-coated | 46.3               | $1.92 \times 10^{10}$     | 64                | [84]       |
| C$_8$-BTBT/PS | PVC       | Inkjet-printed circuit technology | 85      | —                | 66                | [85]       |

\[
SS = SS_{\text{theoretical}} \left(1 + \frac{q^2D_i}{C}\right),
\]

\[
SS_{\text{theoretical}} = \ln(10)\nu_{\text{th}} = 59.6 \frac{\text{mV}}{\text{decade}} \quad \text{(at } T = 300 \text{ K)},
\]

where $\nu_{\text{th}}$ is the thermal voltage, $D_i$ is the trap density, and C is the capacitance of gate dielectric. The theoretical minimum value of SS at room temperature ($T = 300$ K) for an ideal OFET is approximately 59.6 mV dec$^{-1}$.

According to the equation, an effective way to realize a steep SS is to enlarge the capacitance of the dielectrics. We have summarized the related work on achieving a high capacitance in section 2. Therefore, the details regarding increasing the capacitance of the dielectrics will not be described herein. Another effective way is to reduce the $D_i$, which comprises the defects in the organic semiconductor bulk and at the semiconductor-dielectric interface [79]. A steep SS can be achieved via the following approaches: (i) reducing the structural defects of organic semiconductors and (ii) improving the surface quality of dielectrics. In addition, steep SS combined with Schottky barrier OFETs (SB-OFETs) can make a breakthrough in the low-power-consumption OFETs. Recently reported low SS of OFETs are summarized in table 2.

3.1. Reducing the trap density of organic semiconductors

Compared with amorphous or polycrystalline semiconductors, the single-crystal semiconductors with fewer grain boundaries and other structural defects have attracted particular attention to achieve a steep SS. Blülle et al grew highly pure rubrene single crystals by physical vapor transport and established bottom-gate and bottom-contact OFETs with the amorphous fluoropolymer CYTOP as the gate dielectrics. The OFETs demonstrated a steep SS of 65 mV dec$^{-1}$ at room temperature (figures 3(a), (b)) [80]. They estimated that the trap density of semiconductor bulk ($D_{\text{bulk}}$) was $1 \times 10^{13}$ cm$^{-3}$ eV$^{-1}$, and equivalently trap density of dielectric interfaces ($D_i$) was $3 \times 10^9$ cm$^{-2}$ eV$^{-1}$. This research demonstrated that highly pure organic single crystals were profoundly required to satisfy the demands for high-performance, low-power-consumption OFETs.

3.2. Improving the surface quality of dielectrics

Apart from improving the quality of organic semiconductors, modifying the dielectric surface can effectively reduce the trap density of the interfaces. The methods for improving the surface quality of dielectrics include using SAM [81, 82, 86], modifying techniques to deposit dielectrics [83], and utilizing new organic materials as the dielectrics [26, 87]. In the following section, we will focus on these methods reported in the literatures.

The application of densely packed SAM is remarkable for modifying the semiconductor-dielectric interface. For example, -OH groups on SiO$_2$ substrate, which work as the interfacial charge traps and hinder the charge transport, are abundant. Maeda et al inserted an n-doped LaB$_6$ layer into the pentacene-SiO$_2$ interface [81]. Such an interfacial modification method can passivate the interfacial traps and enhance the interface quality. Therefore, a steep SS of 75 mV dec$^{-1}$ was achieved.

Additionally, conventional deposition methods of ultrathin high-k oxide dielectrics (HfO$_2$, ZrO$_2$, BaSrTiO$_3$, and ALO$_x$), such as thermal evaporation, have difficulties in forming a high surface quality dielectric. Optimizing the deposition techniques of oxide dielectrics is necessary due to the significant impact of the semiconductor–dielectric interface on SS. Yang et al applied a template stripping method to fabricate a single-crystalline OFET based on the anodized ALO$_x$ dielectric with a nearly defect-free semiconductor–dielectric interface (figure 3(c)) [83]. Si wafer with atomic flat surface was used as a template in this work. A 100 nm Al was thermally evaporated onto the wafer, and the UV-curable adhesive (optical adhesive, OA) was directly put on the Al surface and
pressed using a glass slide. Then, the OA glass was mechanically cleaved from the Si wafer, which induced an Al film with low surface roughness. Therefore, the high-quality AlOₓ by anodization and the low Dit of 1.81 × 10¹¹ cm⁻² eV⁻¹ was realized. Compared with the conventional thermally evaporated Al thin film with surface roughness larger than 1 nm, the template-striping method can achieve an ultra-smooth surface (roughness can decrease to 0.53 nm). This ultra-flat dielectric combined with a single-crystal 2,6-diphenylanthracene semiconductor via physical vapor transport growth was used to fabricate a low-voltage OFET device. As shown in figure 3(d), the ultra-steep SS is 66 mV dec⁻¹ which is ascribed to the high-quality semiconductor–dielectric interface.

Furthermore, polymers have considerable potential for reducing the surface trap states of dielectrics. Several polymers with optimized surface and large capacitance have appealing prospects in achieving steep SS. Xu et al used a bilayer structure of atomic layer-deposited alumina and cyanoethylated pullulan (CEP) layer as gate dielectric [26]. The alumina layer suppressed the leakage current, while the CEP layer not only provided a high-quality surface but also demonstrated a high capacitance, inducing a steep SS of 66 mV dec⁻¹. One advantage of polymer dielectrics is that can be formed by the solution process, which can provide a high-quality interface because the surface tension of the solution is beneficial for maintaining an ultra-flat surface when the solution is dried [28, 85, 88]. Zhao et al used high-κ poly(vinylidenefluoridetrifluoroethylene-chlorofluoroethylene) (P(VDF-TrFE-CFE)) copolymer and low-κ poly(vinyl cinnamate) (PVC) as the bottom and top dielectrics, respectively, via a fully solution process to improve the surface quality [84]. By adjusting the thickness of the two-layer dielectric, they found that a considerably steep SS of 64 mV dec⁻¹ was achieved with a thick gate dielectric layer of 364 nm (the thickness of P(VDF-TrFE-CFE) and PVC is 250 and 114 nm, respectively). This method provides a desirable guideline in achieving a steep SS.

3.3. Schottky barrier OFET with a steep subthreshold slope
The Schottky barrier OFET with steep SS makes a significant breakthrough in low-power consumption. Jiang et al found that PVC can be used as the dielectric to provide a low trap density interface between the semiconductor and dielectric [87]. The dielectric was also utilized to fabricate a subthreshold Schottky barrier OFET (SB-OFET) through an inkjet-printed circuit technology [79]. The printed dielectric was free of dangling bonds and a smooth semiconductor–dielectric interface was formed. Hence, an ultra-steep SS of 60.2 mV dec⁻¹,

Figure 3. (a) Photograph and schematic of the rubrene crystal OFET. The length and width of channel are 100 and 270 μm, respectively; (b) transfer characteristics of the OFET with single-crystal rubrene as semiconductor and with CYTOP as the gate dielectric. Reproduced with permission [80]. Copyright © 2014, American Physical Society. (c) TEM image of completed OFET device fabricated based on the template stripping method; (d) drain–source current of OFET at the subthreshold region. Reproduced with permission [83]. Copyright © 2018, American Chemical Society.
which is the steepest reported SS for OFETs so far, was achieved (figures 4(a)–(c)). Moreover, this excellent dielectric was associated with a good Schottky barrier in the subthreshold regime. The ultra-steep SS for SB-OTFTs is important for high transconductance and transconductance efficiency. Furthermore, the SB-OTFT operation is channel-length independent with a large output resistance (figure 4(d)), which is provided by the Schottky barrier at the source-semiconductor contact. These characteristics are profitable for printed electronics with variations of typical inject-printed feature size. Thus, the SB-OTFT has a high and constant value for high intrinsic gain in the subthreshold regime, which is much larger than that of inorganic SB-TFT and Si-MOSFET. Through the above improvements, the low-voltage, low-power circuits with high gain, high input impedance, and simple and low-cost fabrication OFETs were achieved.

4. Improving contact for decreasing power consumption

In addition to high gate voltages and subthreshold swings. Huge contact resistance is also a limiting factor in the realization of extremely energy-efficient OFETs. Joule heat will be generated at the electrode-semiconductor area in the OFETs due to high contact resistance ($R_c$), which is detrimental to the device stability and increases the power consumption. $R_c$ generally comprises the injection resistance ($R_{inj}$) at the metal-semiconductor interface and the access resistance ($R_{acc}$) between the contacting interface and the transport channel (figure 5(a)) [91–94].

4.1. Improving charge injection

The $R_{inj}$ is caused by the charge-injection barrier between the metal work function and the highest occupied or lowest unoccupied molecular orbits of semiconductors [95]. The currents decrease with the increase of barrier height and barrier width. Therefore, the three major approaches to reduce $R_{inj}$ are as follows: using matched materials as source-drain electrodes, reducing the barrier height by inserting an injection layer between the semiconductor and source-drain electrodes, and decreasing the barrier width by doping the semiconductors [84, 85, 88].

Graphene is suitable as an electrode due to its high mechanical strength and flexibility. Lee et al reported high-performance bottom-contact pentacene-based OFETs with graphene source or drain electrodes by transferring and patterning CVD-grown monolayer graphene films in a room-temperature process [90]. The contact resistance with graphene electrodes was less than two orders of magnitude than that with Au electrodes (figure 5(c)). Consequently, the mobility of the pentacene-based OFETs with graphene as the source–drain electrodes was up to 0.6 cm$^2$ V$^{-1}$ s$^{-1}$, which was 30 times higher than the devices with gold as electrodes (figure 5(d)). Additionally, inserting a charge injection layer at the metal electrode-semiconductor interface is another common approach to decrease injection resistance. Various materials, such as metal oxide, inorganic salts, and organic compounds, have been used as insertion layers. Kano et al reported high-performance OFETs by inserting a thermally evaporated MoO$_3$ layer between Au electrode and C$_8$-BTBT semiconductor [89]. The thickness of MoO$_3$ layer was examined in the range of 2–30 nm, and then 15 nm was determined as the most appropriate thickness. Figure 5(b) shows that resistance of the devices with the Au/MoO$_3$ contact was much lower than that without the MoO$_3$ interlayer. The devices with the Au/MoO$_3$ contact exhibited large mobility of 2.3 cm$^2$ V$^{-1}$ s$^{-1}$ at low operating voltage, whereas the device without the interlayer exhibited mobility of

![Figure 4](image1.png)

![Figure 5](image2.png)
Additionally, doping is an important method that can improve charge injection. Minari et al. deposited 0.3 nm thick iron(III)trichloride ($FeCl_3$) films as the dopant between the vacuum-deposited semiconductor of dioctylbenzothienobenzothiophene ($C_8$-BTBT) films and the evaporated source–drain electrodes of gold films. The device showed high mobility of 7.0 cm$^2$ V$^{-1}$ s$^{-1}$, which was attributed to the decreased barrier width, thus increased charge density in the depletion region. Compared with the OFETs without $FeCl_3$, the contact resistance was reduced from 200 to 8.8 k$\Omega$ cm.

4.2. Reducing access resistance

With the exception of the injection resistance, another important part of the contact resistance is $R_{acc}$, which is caused by charge-transport process in the semiconductor from the electrode–semiconductor interface to the active channel. Therefore, the factors that can affect the access resistance basically are: (1) device structures; (2) the quality of the dielectrics, which influence amount of mobility carriers; (3) the thickness of the semiconductors [89, 96–99].

Depending on the position of the gate and source–drain electrodes, four kinds of OFET structures, namely, bottom-gate bottom-contact (BGBC), bottom-gate top-contact (BGTC), top-gate bottom-contact (TGBG), and top-gate top-contact (TGTC), are related to contact resistance. Peter et al. reduced the access resistance by using the TGTC structure (figure 6(a)) [91]. The TGBC OFETs with $C_8$-BTBT as semiconductor exhibited a lower contact resistance of 1.8 k$\Omega$ cm than that of BGTC OFETs (200 k$\Omega$ cm). As a result, the TGBC OFETs exhibited high average mobility of 5.7 cm$^2$ V$^{-1}$ s$^{-1}$ and on/off ratio of $\approx 10^9$. Besides, Liu et al. found that the quality of dielectrics was important for charge transport because the defects can reduce the amount of mobile charge carries [101]. They used different polymer dielectrics to fabricate $C_8$-BTBT-based OFETs. The devices showed that the contact resistance value differed significantly from 10 to 66 k$\Omega$ cm relying on dielectric. Apart from polymer dielectrics, SAM nano-dielectrics can also be adopted for minimizing the contact resistance. The surface energy of SAM can affect the morphology of the semiconductors that in turn affects the transport of carriers. For example, the orientation of the molecules was upright on the SAM-modified Au instead of being flat on bare Au [102]. In addition to device structure and the quality of the dielectrics, many studies demonstrated...
the reduction of access resistance with the decrease of semiconductor thickness [103–107]. Therefore, two-dimensional (2D) organic semiconductors with a few nanometers exhibit excellent contact behaviors, which can effectively eliminate $R_{\text{acc}}$. Wang et al deposited large area 2D molecular crystal via the floating-coffee-ring-driven assembly (figure 6(a)) [100]. Based on the 2D bilayer crystalline film, the BGTC OFETs were fabricated and exhibited the average and the maximum carrier mobility of up to 5.2 cm$^2$ V$^{-1}$ s$^{-1}$ and 13.0 cm$^2$ V$^{-1}$ s$^{-1}$, respectively. The estimated contact resistance in the OFET device was only 400 $\Omega$ cm.

5. Other low-power consumption devices

Apart from the switching function, the OFETs can be also applied in emerging energy-related devices, such as photodetectors and non-volatile memories (NVM). Herein, we briefly introduce several new attempts and innovative research on low-power-consumption organic phototransistors and organic-based NVMs.

For the application in the next-generation wearable electronics, the organic photodetectors, which are mainly used to achieve the light detection capability by converting incident light into output electrical signals, have emerged as promising candidates due to their tunable optoelectronic properties, good light sensing performance, biocompatibility, and flexibility [108]. Low-power consumption is required while ensuring the high performance of the devices to promote the application of organic photodetectors in wearable devices. Depending on the requirements of next generation electronics, several ways to achieve low-power consumption have been employed in phototransistors. For instance, Namgung et al utilized ionic liquid as the top dielectric, which can achieve a high capacitance, to fabricate a low-power-consumption multimodal photodetector platform with multilayer transition metal dichalcogenides as the semiconductor. The multimodal photodetector platform combined a lateral phototransistor structure and a vertical large-area Schottky photodiode structure (figure 7(a)) [109]. Then, the organic photodetector can be dynamically selected the following modes: photogating (PG) mode, which can achieve the high optical gain characteristic; and photovoltaic (PV) mode, which can realize the fast response characteristic by controlling the gate and drain voltages. In the PV mode, when a $V_g = +0.25$ V is applied to the ionic liquid gate, a large photocurrent can be observed over both electrodes. The device also showed a high responsivity of 1270 A W$^{-1}$ with a small $V_d$ of 0.5 V. In the PG mode, large negative and positive photocurrents can be measured at $V_g = -1$ V and $V_g = +1$ V, respectively. Therefore, the device both worked at low operating voltage on PG and PV modes.

Increasing the capacitance using high-$\kappa$ dielectrics is also an effective approach to realizing low-power consumption photodetectors. Jiang et al utilized the high-$\kappa$ (2-phenylethyl) trichlorosilane and SAM-modified titanium-silicon oxide/hybrid ($h$TSO) as gate dielectric to fabricate phototransistors with the 5,5'-didithienothiophenyl-3,3'-bis(tetradecylthio)-2,2'-bithiophene as the semiconductor (figure 7(b)) [110]. The high-$\kappa$ nature of $h$TSO and the modification of SAM boost the unit capacitance of $h$TSO to 180 nF cm$^{-2}$. The organic phototransistor exhibited a high photosensitivity of 3800 and a good carrier mobility of 0.25 cm$^2$ V$^{-1}$ s$^{-1}$ under a low operating voltage of −3 V.

Decreasing the trap density of dielectric interface can also reduce low-power consumption. Xie et al reported a hybrid phototransistor based on perovskite/organic semiconductor hybrid heterojunctions with a layer of 6,6'-phenyl-C61-butyric acid methyl ester (PCBM) coating as a passivation layer. This layer can accelerate the separation of electron–hole pairs and passivate the perovskite to reduce trap states and grain boundaries of the dielectric interface [111]. In the staggered heterojunction, CH3NH3PbI3–Cl, perovskite was used as the light harvesting layer of the photodetector, and the carrier conducting channel of the photodetector utilized poly-(3,4-ethylenedioxythiophene):poly(styrenesulfonate) (PEDOT:PSS) (figure 7(c)). The device can operate with a low voltage of 0.5 V under 598 nm illumination with approximately 44% enhancement in responsivity ($2.46 \times 10^8$ AW$^{-1}$). PCBM also provided an extra built-in electric field to accelerate the drift of photocarriers.
and to prolong the lifetime of holes. Consequently, the device can have a response speed of approximately five times faster than that without PCBM coating. In addition to the organic phototransistors, researches on NVMs with low-power consumption have also been made significant progress, which we will briefly discuss as follows.

NVMs, which can be divided into three- and two-terminal devices, show a growing demand for low-power consumption with the development of the artificial intelligence. Three terminal devices, such as OFETs with ferroelectric as the dielectrics (Fe-OFETs), which can function as NVMs have attracted considerable attention for many researchers. The power consumption of Fe-OFET NVMs can be decreased by reducing their operating voltage and promoting data switching. For example, Xu et al utilized a P(VDF-TrFE-CTFE) film with low coercive field to develop a Fe-OFET NVM with low operating voltage. Construction of the compound gate dielectric layer was an ultrathin P(VDF-TrFE-CTFE) film sandwiched in between two layers ultrathin high-κ AlOx [112, 114]. The sandwich-structured dielectric layer made a contribution to reduce the operating voltage, depress the gate leakage and improve the mobility. Therefore, the device exhibited a low operating voltage of 4 V and the on-off ratio was over 10^5 at the low P/E voltages of ±4 V. In addition, Pei et al reported ultra-low-power-consumption memory, namely, C8-BTBT-based Fe-OFET NVMs with a high-κ AlOx and ultra-thin P(VDF-TrFE) hybrid dielectric, to reduce the operating voltage and promote the data switching [112]. The device exhibited low voltage, fast operation, and satisfactory performance of low-power consumption due to the ultrathin ferroelectric and the high-quality 2D molecular crystals with excellent charge transport characteristics. The device only needed pJ-level energy consumption (figure 7(d)). Some properties of NVMs, which can be used for applications out of memory space [114], for example, the two-terminal memristors, are associated with brain-inspired neuromorphic computing to simulate the functions of biological synapses, thereby functioning as NVMs [115]. Many researchers have explored low-power-consumption flexible two-terminal memristors based on organic materials. For example, Chen et al reported a low-power organic flexible memristor whose architecture was Al/graphene/parylene/W (G-memristor) based on flexible parylene substrates and the insertion of graphene as a barrier layer, which was the main factor of the device to achieve the low-power consumption (figure 7(e)) [113]. Researchers utilized the intrinsic nanopores on graphene with considerable impermeability to limit the diffusion of metal atoms across the architecture and imparted the formation of the fine conductive filaments during the set process to reduce Al and parylene. In addition, the formation and dissolution of the filaments were closely linked to the resistive switching behavior of the devices. Compared with the memristor without the graphene barrier layer, the average reset current of the G-memristor decreased from...
2.97 to 0.63 mA and the power consumption reduced from 2.15 to 0.149 mW. The G-memristor also demonstrated a low reset current and a programming power consumption by \( \approx 47 \) and \( \approx 14 \) times, respectively.

6. Conclusion

Energy-efficient OFETs have progressed rapidly in the recent years. We outlined some of most promising strategies for realizing low-power consumption, including reducing the operation voltage, achieving a steep SS, and decreasing the contact resistance. The high-\( \kappa \) materials, SAMs, and electrolytes show unique advantages in realizing low operation voltage. The OFETs based on low-defect organic semiconductors and high-quality semiconductor–dielectric interfaces exhibit excellent subthreshold properties. The two main approaches in reducing the contact resistance are as follows: (1) tuning the charge-injection barrier between the metal work function and the highest occupied or lowest unoccupied molecular orbits of semiconductors; (2) decreasing the thickness of the semiconductor.

Despite recent successes in energy-efficient OFETs, more research is necessary to overcome current limitations before organic electronic devices can be seamlessly integrated into our daily life. The physical understanding of transport and structure-property relationships further need to be improved, which in turn supports the development of low-power consumption OFETs. Additionally, as most intrinsic organic semiconductors are based on dynamic non-covalent cross-linked bonds, their mechanical properties are sensitive to temperature. Encapsulation can help increase stability of the low-power consumption OFETs to desired levels. Furthermore, although the power dissipation of a single OFET has been achieved a low level, the technology for fabricating energy-efficient OFET arrays still remains a challenge. Therefore, the development of the fabrication process such as patterning technology will be necessary.

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