Behavior of SiC MOSFET under Short-Circuit during the On-State

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Abstract - This paper presents behavior of SiC MOSFET under short-circuit during the on-state conditions. Although much research has been conducted on the short-circuit characteristics of the first type of SiC MOSFETs, no paper has reported the second type. A set of test benches which can perform the second type of short-circuit are designed. Simulation by LTspice combined with experiments are conducted to evaluate the influences of several important parameters like miller capacitance, gate resistance, gate-source voltage, drain-source voltage on the second type of short-circuit characteristics of 1200 V/36 A SiC MOSFET.

1. Introduction
For a long time, silicon-based power devices dominated the power electronics semiconductor market and power system applications [1]. As a new wide bandgap power semiconductor device, SiC MOSFETs are considered the most likely alternative to silicon devices at medium power applications. Compared to Si MOSFETs or Si IGBTs, SiC MOSFETs have lower on-resistance, stronger high-temperature capability and faster switching speed [2], and are expected to be applied to various solid-state power converters in the future [3]. Although the low- and medium-voltage SiC MOSFET devices have been produced, they have not yet replaced silicon-based devices on a large scale. In addition to higher costs, another major constraint is reliability. In the face of increasingly complex and severe working environments, short-circuit reliability is particularly important.

In general, the short-circuit types of semiconductor devices can be divided into two categories. The first type (SC I) is also called hard-switching fault (HSF), i.e. short-circuit has occurred before the device turns on. The second type (SC II) is also called fault under load (FUL), i.e. short-circuit during the on-state conditions. Considering the behavior of the freewheeling diode in the upper arm, there exists a third type (SC III), i.e. short-circuit occurs when the upper diode is freewheeling [4]. Currently, most work about short-circuit characteristics of SiC MOSFETs focus on the first type as it is easy to implement. Several papers reported the influences of several parameters on the first type short-circuit behavior [5-8]. Single pulse and continuous pulse of short-circuit experiments were performed on commercial SiC MOSFETs, and the experimental waveforms were combined with the thermal imaging to further investigate the degradation process and failure mechanism that limit the device reliability [9]. In reference [10], experimental research and TCAD electro-thermal simulation
were used to describe and analyze the causes of short-circuit failure of SiC MOSFETs, and the effects of certain physical parameters on short-circuit capability were explained through appropriate numerical methods. We can get the FUL behavior of IGBTs in reference [11-13]. However, no papers have reported the behavior of the second type of short-circuit of SiC MOSFETs, neither experiments nor simulation results can be found.

The aim of this paper is to start a discussion about the second type of short-circuit of SiC MOSFETs. In section II, an experimental test bench is designed. In section III, the basic behavior of SC II is obtained by experiment. The FUL behavior of SiC MOSFET and IGBT module are compared. In section IV, the experimental results and simulation results by LTSPICE are used to obtain the influence of several important parameters on SiC MOSFET’s FUL characteristics. Section V concludes the paper.

2. EXPERIMENTAL PROTOCOLS

A. Test Bench Description

Compared to SC I, the implementation of the second type is more demanding. Similar to the method of implementing FUL of IGBT, the test circuit schematic for SiC MOSFET single device is designed as Fig. 1.

![Schematic of short-circuit test circuit](image)

**Fig. 1. Schematic of short-circuit test circuit**

CREE’s second-generation SiC MOSFET is selected as the device under test (DUT). Its main parameters are shown in Table I.

| Part Number | $U_{DS}$/V | $I_{DSS}$/A | $U_{GSmax}$/V | Package   | $R_{DS(on)}$/mΩ |
|-------------|------------|-------------|---------------|-----------|-----------------|
| C2M0080120D | 1200       | 36          | −10/+25       | TO-247-3 | 80              |

In order to achieve the condition of fault under load, one IGBT module is used as a breaker which can short the load when DUT is in on-state. Its voltage and current level are high enough to keep safe operation during short-circuit of SiC MOSFET single device. An Infineon-FF450R17ME4 IGBT module with a rated value of 1700 V/450 A and a short-circuit current of up to 2300 A is chosen as the circuit breaker. The TMS320F2812 development board is selected as the driving signal generation device for the IGBT module and the device under test - SiC MOSFET. In order to facilitate the adjustment of the value of the gate drive voltage and minimize the parasitic parameters of the line, this article has specially designed the drive circuit board for IGBT and SiC MOSFET, both equipped with external drive power interfaces. CREE’s 1200 V/33 A silicon carbide Schottky diode C4D20120D is used as the freewheeling diode. Lstray stands for the original stray inductance of the main loop. L1 is an 800 μH load inductor, CDC is a DC bus capacitor, and UDC is a DC power supply to charge the DC bus capacitor to the set point. In order to avoid voltage overshoot during the turn-off process that...
exceeds the breakdown voltage of the device, the DC bus voltage generally does not exceed 60% of the rated voltage $U_N$ of the device [14]. The maximum DC bus voltage $U_{DC\text{max}}$ of this short-circuit test can be obtained from (1) and the appropriate DC bus capacitors value are chosen as (2). $E_{\text{max}}$ is the estimated maximum energy consumption for a single short-circuit test; $\Delta U_{DC}$ is the DC bus voltage drop caused by a single short-circuit test. To ensure that the DC bus voltage changes little after each short-circuit test, the $\Delta U_{DC}$ is limited to (1%~5%) $U_{DC}$. Therefore, in this paper, two paralleled capacitors rated at 420 $\mu$H/1100 V with low parasitic parameters are selected as the DC power supply. In order to reduce the loop stray inductance, the DC bus capacitors are installed in a laminated-crossover structure and paralleled with a capacitor having smaller stray inductance.

$$U_{DC\text{max}} = U_N \times 60\% = 1200 \times 60\% = 720 \text{ V}$$ (1)

$$C_{DC} = \frac{2E_{\text{max}}}{U_{DC}^2 - (U_{DC} - \Delta U_{DC})^2}$$ (2)

Partial experimental platform hardware is shown in Fig. 2. To facilitate the replacement of SiC MOSFET devices, a TO247-3 package test socket made of temperature-resistant bakelite is installed. The oscilloscope used in the experiment is YOKOGAWA DLM2054 ($BW = 500$ MHz), the voltage probe is a Passive probe ($BW = 500$ MHz), and a PEM CWT3 Rogowski coil ($BW = 30$ MHz, $I_{\text{peak}} = 1200$ A) is selected as the current probe. It should be noted that the Rogowski coil has a 21ns delay determined by the current shunt T&M SSDN-414-01, and the delay of the Rogowski coil needs to be compensated at the oscilloscope during the test.

**B. Timing Diagram**

This experimental platform can implement SC I and SC II easily depending on the coordination of the gate drive signal timing of Breaker and SiC MOSFET. The timing diagram for the SC II test is shown in Fig. 3.

![Fig. 3. Timing diagram for SC II](image-url)
The SiC MOSFET is first turned on at $t_0$, and then the breaker is turned on after the interval $\Delta t_{II}$, SC II occurs. During the $\Delta t_{II}$ period, the current $I_D$ increases linearly, as in (3). The magnitude of this increase depends on the DC bus voltage $U_{DC}$, the load inductance $L_1$ and the time $\Delta t_{II}$. Therefore, the length of $\Delta t_{II}$ depends on the preset desired currents $I_D$, $U_{DC}$ and $L_1$. The short-circuit pulse width $t_{sc}$ of the SC II depends on the time at which the Breaker and SiC MOSFET are both in on-state.

$$I_{D(\Delta t)} = \frac{U_{DC}}{L_1} \Delta t$$

(3)

During the SC II test, it should be noted that the interval $\Delta t_{OFF}$ can’t be set too short, as anomalies may occur due to stray inductance. However, it also can’t be set too long in order to avoid the breaker falling into short-circuit for a long time if the DUT fails to turn off.

C. Test Protocol

In order to fully understand the characteristics of SC II, the experimental test and LTspice simulation are performed in this paper. We leave a cooling time of more than several minutes between every two experiments so as to avoid the influence of the change of the junction temperature caused by the self-heating during the short-circuit process on the next short-circuit test. Through the experimental results we get the basic behavior of SC II and the influence of drain-source voltage $U_{DS}$, and gate-source voltage $U_{GS}$ on the short circuit current $I_D$. Through the simulation results we get the influence of miller capacitance $C_{GD}$ and gate resistance $R_G$ on the short circuit characteristics. Parameters are kept at $U_{GS} = 18$ V, $R_G = 37.5$ Ω, $U_{DS} = 400$ V unless these parameters are the controlled variables.

3. BASIC BEHAVIOR OF SC II

In order to obtain the basic short-circuit characteristics, the experiment is performed by gradually increasing the width of the short-circuit pulse in steps of 1 μs. Fig. 4 shows the short circuit current $I_D$ of SC II. It can be seen that the short circuit current peak is approximately 200 A, more than five times the rated current. The overall characteristics of the waveform is very similar to SC I’s, the current first rise rapidly and gradually decrease after reaching the peak current. The increased temperature due to self-heating affects the on-resistance, which in turn affects the current waveform.

The short-circuit current waveforms of SC I short-circuited 12 μs and SC II short-circuited 8 μs under the same test conditions are placed on the same figure for comparison, as shown in Fig. 5. So we can visually compare the difference between the SC I and SC II short circuit current waveforms of SiC MOSFETs. The SC II short circuit current waveform displays a steeper rising edge, but the
current peak is not too sharper compared with SCI. This is very different from the IGBTs tested by Professor Lutz et al [4]. For IGBTs, the SC II short-circuit current waveforms are significantly different from the SC I, where the current peak of the second type is much larger than the first type’s. We guess there are certain parameters that have an important effect on this, as we will discuss later.

![Experimental short-circuit voltage waveforms of SC II](image)

**Fig. 6.** Experimental short-circuit voltage waveforms of SC II

Take 8 μs short-circuit pulse as an example to introduce the voltage characteristics of SC II, as shown in Fig. 6. The gate-source voltage UGS displays a large overshoot at the beginning of the short circuit. Since the experiment is performed under UGS = 18 V, the overshoot is up to 12V. This overshoot is mainly due to the displacement current through the miller capacitance which is caused by the high dv/dt of drain-source voltage UDS. As for UDS, there exits an overshoot at turn-off which is caused by the high di/dt of drain current ID and the parasitic inductance.

### 4. INFLUENCE OF PARAMETERS

**A. Influence of UGS and UDS**

The influence of the gate-source voltage and drain-source voltage on the second-type of short-circuit characteristics of SiC MOSFETs is the same to that of the first-type short-circuit characteristics, as shown in Fig. 7 and Fig. 8. With the increase of UGS, the short circuit current peak appears slightly ahead in time, and the peak current IDmax of the short circuit current increases nearly linearly. As the drain-source voltage UDS increases, the time to reach the short circuit current peak shortens and the peak value of the short circuit current increases. However, the short circuit current peak amplitude variation between different drain-source voltages at a higher voltage level is smaller than that at a lower voltage level.
B. Influence of RG

After understanding the basic characteristics of the second type short-circuit of SiC MOSFET, this paper further studied the effects of the gate resistance RG and miller capacitance CGD on the SC II characteristics through LTspice simulation to obtain a more comprehensive SC II characteristics.

Keeping other parameters constant, the influence of different gate resistors RG on the behavior of SiC MOSFET under short-circuit during the on-state is simulated. The simulation results are shown in Fig. 9. In the first type of short circuit, as we have studied before, the peak current of the short circuit current decreases with the increase of the gate resistance, as the gate-source leakage current causes a voltage drop across the gate resistance and thus reduces the gate-source voltage. On the contrary, in the second type of short-circuit, with the increase of the gate resistance, the value of the current at the beginning presents an increasing trend. This is because the gate-source voltage under SC II is more seriously affected by the miller capacitance current generated during the rapid rise of the drain-source voltage.
The simulation results of gate resistance’s influence on the gate-source voltage $U_{GS}$ in SC II is shown in Fig. 10. It can be seen that the larger the gate resistance $R_G$, is the more severe the gate-source voltage overshoot at the moment of short-circuit, which is in turn increases the SC II short-circuit current.

Fig. 9. Simulated short-circuit current of SC II under different $R_G$

C. Influence of $C_{GD}$

This paper simulates the effect of different miller capacitor $C_{GD}$ values on the current characteristics of SiC MOSFET under SC II in LTspice, as shown in Fig. 11. It should be noted that the miller capacitance varies with the drain-gate voltage $U_{GD}$, however, we can’t achieve this effect. We put a constant-value high-voltage ceramic capacitor in parallel with the gate and drain, roughly equivalent to adding miller capacitance value. This work is dangerous when applied to experiments, since in short-circuit experiments an oversized miller capacitance may cause the device to explode. We just use simulation to anticipate how different miller capacitance values will affect the second type of short circuit. As shown in Fig. 11, with the increased CGD, the peak value of short circuit current increases, and the peak current shifts to an earlier time. At $\Delta C_{GD} = 200$ pF, the SC II short-circuit current waveform of the SiC MOSFET has clearly reflected the characteristics of the SC II short-circuit current of the IGBT, that is, high short-circuit current peak and high short-circuit current falling slope $di/dt$ after the peak [4]. In this simulation the short circuit current peak of $\Delta C_{GD} = 200$ pF is up to 289A, far higher than that of $\Delta C_{GD} = 0$ pF. It can be speculated that the miller capacitance of SiC MOSFET is smaller than that of IGBT, which may be the main reason why the characteristics of their
SC II short-circuit current differ greatly. The datasheet of DUT shows miller capacitance of 7.6 pF, while the IGBT module’s miller capacitance is up to 1 nF or more. It can be seen that the increase of the miller capacitance during the module manufacturing process will make the second type of short circuit more severe. The strict control of the miller capacitance is not only related to the normal switching characteristics of SiC MOSFET, but also has an important effect on its SC II behavior.

On one hand, as shown in Fig. 12, the different values of miller capacitance CGD affect the rise rate of the UDS during the short-circuit. The rise rate of UDS decreases if the CGD increases, resulting in a longer rising duration.

On the other hand, the magnitude of the gate-source voltage UGS is affected by the miller capacitance and the gate-drain voltage changing rate, as shown in equation (4). Here, UGG is the supplied driving voltage value, Crss is the reverse transmission capacitance i.e. miller capacitance CGD, LG is the gate parasitic inductance, LS is the source parasitic inductance.

\[
U_{GS} = U_{GG} + R_G \cdot C_{gs} \cdot \frac{dU_{GD}}{dt} + L_G \cdot \frac{dI_G}{dt} - L_s \cdot \frac{dI_s}{dt} \quad (4)
\]

So the overshoot of UGS is larger and has a longer duration with a larger CGD, as the inset shown in Fig. 13. This in turn causes a larger short-circuit current peak.
5. CONCLUSIONS

Experimental and simulation investigations on the SC II of SiC MOSFET have been conducted in this paper. The basic behavior of short-circuit current ID, gate-source voltage UGS and drain-source voltage UDS under SC II are obtained from the experimental results. Influences on the behavior of SC II of important parameters like miller capacitance CGD, gate resistance RG, gate-source voltage UGS and drain-source voltage UGD are studied by experiment assisted by LTspice simulation. The short circuit current does not show much difference between SC I and SC II like that of IGBT. With the increase of gate resistance, the value of the short circuit current at the beginning of SC II presents an increasing trend in contrast with SC I. Miller capacitance CGD plays an important role in determining the short circuit current peak. More work, especially experimental research is needed to improve the study of the SC II characteristics of SiC MOSFET, both single device and module.

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