MODEL-DRIVEN AUTOMATIC TILING WITH CACHE ASSOCIATIVITY LATTICES

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ABSTRACT. Traditional compiler optimization theory distinguishes three separate classes of cache miss – Cold, Conflict and Capacity. Tiling for cache is typically guided by capacity miss counts. Models of cache function have not been effectively used to guide cache tiling optimizations due to model error and expense. Instead, heuristic or empirical approaches are used to select tilings. We argue that conflict misses, traditionally neglected or seen as a small constant effect, are the only fundamentally important cache miss category, that they form a solid basis by which caches can become modellable, and that models leaning on cache associativity analysis can be used to generate cache performant tilings. We develop a mathematical framework that expresses potential and actual cache misses in associative caches using Associa-
tivity Lattices. We show these lattices to possess two theoretical advantages over rectangular tiles – volume maximization and miss regularity. We also show that to generate such lattice tiles requires, unlike rectangular tiling, no explicit, expensive lattice point counting. We also describe an implementation of our lattice tiling approach, show that it can be used to give speedups of over 10x versus unoptimized code, and despite currently only tiling for one level of cache, can already be competitive with the aggressive compiler optimizations used in general purposes compares such as GCC and Intel’s ICC. We also show that the tiling approach can lead to reasonable automatic parallelism when compared to existing auto-threading compilers.

Key words and phrases. associative cache, code generation, polyhedral model.
1. Introduction

Tiling has been shown to be a robust and effective transformation for exploiting locality [LRW91] and for parallelism [AL93]. Though general purpose compilers perform some tiling for cache performance, they also tend to rely on heuristic approaches which when lacking information will act conservatively. In the Polyhedral Model [Bas04], a lot of progress has been made regarding how to generate tiled codes [RS92] and how the tiles should be chosen to exploit locality and to extract parallelism [BHR08]. Even in light of that research, the so called tile-size selection problem remains open, leading some researchers to suggest that only empirical auto-tuning can provide the answers [CCH08]. Our research takes a very different approach: at the philosophical level we believe that advances in understanding and modeling of memory hierarchies remain unsolved, and that with greater understanding models of memory and cache can be used to guide tiling algorithms. In particular, we believe that associativity in cache architectures is the fundamentally important though much neglected feature of cache memories, and when better understood can lead to the generation of more accurate cache models. We will first make this argument informally while describing the features of associative cache in Section 1.1. In Section 2.1 we will then begin to describe the modeling framework to provide first a working model of potential cache misses in Section 2.3 and later a working model of actual cache misses in Section 2.4. Then in Section 3 we will describe how this model extends to tiled codes. We will describe a tiling framework and a simulation environment that, taking a specification as input, can build the appropriate cache model for the operation, choose the tiling that minimizes cache misses for a single level of the hierarchy, and then generate the appropriate tiled codes. We will describe performance results of this framework in Section 4. Our work is highly experimental and could be built-upon on many different ways. We discuss those ways and related research in Section 1.2.

1.1. Associative Cache Function.

1.1.1. Cache Specification. In order to fully describe the need for tiling according to associativity, we first describe the mechanism of \( K \)-way set-associative caches. Data is moved in units called lines. All addresses map to several memory-level-lines such as memory-line (meaning a line in DRAM), \( L1 \) cacheline and \( L2 \) cacheline. When data residing at a memory address needs to be accessed, the caches are first checked for the presence of the corresponding line, and it is loaded from the highest (i.e., closest) cache level in which the line is present, at minimum access cost. For a specific cache level, each memory address is mapped deterministically to a certain cache set containing \( K \) possible cache slots or ways. The cache-level functionality can thus be specified by a cache specification \( C = (c, l, K, \rho) \), where \( c \) is the total cache capacity (total bytes that can be stored in the cache), \( l \) the cache line size (number of bytes fetched in one load), \( K \) the associativity (number of cachelines that can reside in one cache set), and \( \rho \) an index \( \rho = 1, \ldots, P \) (the cache’s position in a \( P \)-level memory hierarchy). Such a specified cache has \( N = \frac{c}{lk} \) cache sets, and hence every \((\frac{c}{lk})^\text{th}\) cacheline or \((\frac{c}{RK})^\text{th}\) data element maps to the same set. This simple striding defines the mathematical structure on which our cache models are based.
1.1.2. Cache Miss. When data at a given address must be used, and the associated line is not found in the cache, then a cache miss occurs and an expensive load from a lower memory level ensues. The literature has traditionally differentiated between three categories of cache misses: capacity misses where data needs to be loaded because more cachelines are accessed than can fit into total cache, cold misses where data has never been accessed and thus must be loaded, and conflict misses where a line must be loaded because, although previously in the cache, the line was evicted when too many cachelines were loaded into the same cache set. Typically, associativity is considered a small constant effect [HP11] and is ignored by most cache models [YLR+05, CP03]. We believe that the effects of associativity have been misunderstood and neglected, and further that cache misses in associative caches are better categorized using a single classification: that of conflict misses due to associativity. We justify this informally here and develop it formally in Section 2.4.

1.1.3. Cache Capacity. We first note that cache capacity, though perhaps occasionally a useful approximation for programmers, is neither expressed nor comprehended in cache logic, and can lead to misleading and inaccurate estimations of the data volume accessible to a cache, when accessing tiles or padded array segments. Cache protocols assume the perspective of a single cache set. Since all data map to a given cacheline and all cachelines map to a given set, then only a single set is checked for the presence of the cacheline in question. Correspondingly, only the contents of one set are candidates for eviction. Only in the case where all cache sets are used uniformly does total cache capacity remain a useful quality. Any variation in usage between sets (which is typical) decreases the accuracy of cache capacity as a metric. The example in Figure 1 illustrates how a 2-d array stored in a 2-way associative cache with 4 sets cannot use full cache capacity. The extreme of this effect is called cache thrashing, where consecutively accessed elements map to identical sets, and can be seen as the lower bound of cache capacity usefulness. Since the single measure of cache capacity is variable it does not serve as a suitable model parameter. The cache capacity per set does remain valid, though it should be obvious that per-set cache capacity is treated by the conflict miss category of misses.

Cold misses also do not require any special treatment and can be viewed as a special case of conflict miss. In Section 2.4 we will show that a given set of potential cache misses, meaning a group of cachelines that all map to the same set, can be further categorized as actual cache misses when the reuse distance between successive reuses exceed the cache associativity. In a typical set, the situations that produce this will be when either the cacheline has never been used before (cold misses) or when more than $K$ different cachelines have been used before the reuse (conflict misses). We therefore choose to model cache through the single mechanism of associativity misses and will refer to these as cache-misses. This informal reasoning is made concrete in Section 2.4.

1.1.4. Cache Reuse Policy. The exact mechanism used by a set to decide if a cacheline should be evicted, and which line to evict, is called the eviction policy. We will consider two eviction policies in this paper, which are the most commonly implemented reuse policies in modern hardware – Least Recently Used (LRU) and Pseudo Least-Recently Used (PLRU). Our framework implements model variations
for both policies. Our implementation allows us to see a comparison of these reuse policies and to see which policy appears to match experimental results more closely (and is therefore more likely implemented in the hardware). A detailed description of the policy and the effects that policy choice has on model quality is interesting but deferred to a future paper.

1.2. Related Work. Ghosh et al. [GMM97] describe a mathematical framework for the evaluation of cache misses. Solutions to their Cache Miss Equations (CMEs) correspond directly to the cache misses in a code. However, as pointed out in their work, the CMEs are ultimately intractable. For certain situations, the CMEs can allow users to understand a lot about cache behavior because basic number theory can be used to describe situations when no cache misses arise. They cannot however be used to model accurately general situations when misses do arise. The base mathematical property of the CMEs is the same as in our work. However their work did not realize the inherent lattice structure that is formed by the solution of the CMEs.

CMEs were used in [AGLV02] to drive tiling transformations and a reduction in the ratio of capacity to conflict misses for several benchmarks was shown. However absolute performance of the tilings was not discussed, and the research was continued in a meaningful way. While CMEs may be useful in isolated cases, their ultimately intractable solution space means that their applicability for general transformations is unlikely.

We have expressed cache misses in a concise mathematical formulation for which we believe future work can yield efficient optimal or approximate code generating schemes. To a limited extent, this is already evident in our work. The lattice tiles can be generated quite simply without counting of lattice points, and a relatively simple decision algorithm can be incorporated into the model-based decision-making. However, the model as currently expressed is non-polynomial in execution time. No research to date has constructed tiles based on the associativity characteristics of a memory. [GAK03] contains analysis of various rectangular tiles and observes that lattice tilings would be theoretically superior, but to our knowledge this lead was not followed by the authors or any other researchers.
2. Basic Cache Miss Model

Throughout the discussion we will assume a cache specification \( C = (c, l, K, \rho) \) is given, and we denote by \( N = \frac{C}{c} \) the number of cache sets in it.

2.1. Cache Miss Machinery.

2.1.1. Index Maps. Let \( A \) be a \((m_1, \ldots, m_d)\)-table, w.l.o.g with index set \( Q(A) = [0, m_1 - 1] \times \cdots \times [0, m_d - 1] \cap \mathbb{Z}^d \). In RAM the elements of \( A \) will be spread out into a (typically consecutive) 1-dimensional array which we will denote by \( a(A) \) (or simply \( a \)) of size \( m_1 \cdot \ldots \cdot m_d \). Its elements are \( a_i \) for \( i \in \{0, \ldots, m_1 \cdot \ldots \cdot m_d - 1\} \).

**Definition 1** (index map). Given a \((m_1, \ldots, m_d)\)-table \( A \) with array \( a(A) \), a bijective function \( \phi : Q(A) = [0, m_1 - 1] \times \cdots \times [0, m_d - 1] \cap \mathbb{Z}^d \rightarrow a(A) = [0, m_1 \cdot \ldots \cdot m_d - 1] \cap \mathbb{Z} \) is called an index map for the pair \((A, a)\). Its inverse is \( \phi^{-1} \).

Typical index maps are affine functions like

\[
\phi_c(i_1, \ldots, i_d) = i_1 + m_1(i_2 + m_2(i_3 + m_3(\cdots + m_{d-1}i_d)))) = \sum_{k=1}^{d-1} \sum_{l=1}^{m_k} i_k
\]

(column major order) or

\[
\phi_r(i_1, \ldots, i_d) = i_d + m_d(i_{d-1} + m_{d-1}(i_{d-2} + m_{d-2}(\cdots + m_2i_1)))) = \sum_{k=1}^{d} \sum_{l=k+1}^{m_k} i_k
\]

(row major order). Their inverses can be defined using mod and div.

Since \( a(A) \) is naturally ordered, for each index map \( \phi \) there exists a unique point \( q_A \in Q(A) \) such that \( \phi(q) \) has minimal index in \( a(A) \) such that \( \phi(q_A) = 0 \) (mod \( N \)). This point will be called the base point of \( Q(A) \).

We will mostly consider affine index maps, i.e. \( \phi(x + y) = \phi(x) + \phi(y) \) and \( \phi(\lambda x) = \lambda \phi(x) \). In this case \( \phi(q_A) \) exactly the affine offset. We can furthermore assume that \( \phi \) is monotone wrt. the component-wise ordering of \( Q \) (otherwise we need to consider, e.g., \( \phi'(x_1, \ldots, x_d) = \phi(x_1, \ldots, m_i - x_i - 1, \ldots, x_d) \)).

If \( q_A = 0 \in Q(A) \) we will sometimes say that \( \phi \) is linear (which it is, as a map to the module \( \mathbb{Z} / N \mathbb{Z} \)). Non-linear index maps, like sparse matrix storage using auxiliary mapping arrays, are also interesting, but beyond the scope of this paper.

2.1.2. Iteration Domains. Let two tables \( A \) and \( B \) be given. When we consider an arbitrary pair of elements \( x \in A \) and \( y \in B \) we actually index a single entry in \( A \times B \). For typical computations, like matrix multiplication we will successively access an entire hyperplane of \( A \times B \) (e.g., to compute \((AB)_{ij}\) we will use indices \( \{(i_1, i_2, i_3, i_4) \in Q(A) \times Q(B) : i_1 = i, i_2 = i_3, i_4 = j\} \)). Appealing to this use case we will call any affine subspace of such a product of index sets an iteration domain.

**Definition 2** (iteration domain, operand). Given \( k \) tables \( A_1, \ldots, A_k \) with index sets \( Q(A_i) \in \mathbb{Z}^d \) we call \( Q(A_1, \ldots, A_k) = Q(A_1) \times \cdots \times Q(A_k) \) the joint index set. For any affine subspace \( H = R^{\sum_{i=1}^{d} d_i} \subseteq \mathbb{R}^d \) the set \( Q(A_1, \ldots, A_k) \cap H \) is called a (joint) iteration domain.

The tables \( A_1, \ldots, A_k \) will be called operands. The projection function onto operand \( i \) will be designated by \( \pi_i : Q(A_1, \ldots, A_k) \rightarrow Q(A_i) \).
2.2. Ordering and Distance.

Definition 4 (iteration ordering). Let \( \prec \) be a total order on \( \mathbb{Z}^d \). We will call the restriction \( \prec_D \) of \( \prec \) to a set \( D \subseteq \mathbb{Z}^d \) an iteration ordering on \( D \).

Of course, lexicographic ordering of the indices of the tables yields an iteration ordering, but many other iteration orderings are conceivable and potentially useful for our application. Furthermore, an index map \( \phi_A \) induces an iteration ordering by virtue of the natural ordering of \( a(A) \), but we will often consider the case where the index map order and the iteration order are different.

Definition 5 (subsequent reuse). Let \( \mathcal{R}_i(q_i) \) be a reuse domain of an iteration domain \( D \). Since \( \mathcal{R}_i(q_i) \subseteq D \) then if \( \prec \) is a total order on \( D \) that also defines a total order on \( \mathcal{R}_i(q_i) \). Hence for any non-boundary \( x \in D \), \( \exists y \in D \) with \( x \prec y \) and \( \not\exists z \in D \) such that \( x \prec z \land z \prec y \). We call \( y \) the subsequent reuse of \( q_i \).

| Operation          | algebraic form | constraints |
|--------------------|----------------|-------------|
| Scalar product     | \( A_0 = \sum_k B_k C_k \) | \( \{i_1 = 0, i_2 = i_3\} \) |
| Convolution        | \( A_0 = \sum_k B_k C_{m_k}^{i_k} \) | \( \{i_1 = 0, i_2 = m_k^i - i_3\} \) |
| Matrix multiplication | \( A_{ij} = \sum_k B_{i,k} C_{k,j} \) | \( \{i_1 = i, i_2 = j, i_3 = i, i_4 = i_5, i_6 = j\} \) |
| Kronecker product  | \( A_{m_k(C_{(l-1)+k},m_k(C_{(l-1)+l})} = B_{l,j} C_{k,l} \) | \( \{i_1 = m_k^i (i_3 - 1) + i_5, i_2 = m_k^i (i_4 - 1) + i_6\} \) |

Table 1. Examples of commonly occurring subspaces. Notation: Table \( T \) has index set \( Q(T) = \prod_{j=1}^{d^T} [0, m_j^T - 1] \).

Note that \( H = \mathbb{R}^{\sum_{i=1}^k d_i} \) is a valid iteration domain. Usually the subspace \( H \) will be defined so that the iteration domain remains nonempty. If \( H \) is a linear subspace the iteration domain will be a set of integer points of some sublattice of \( \mathbb{Z}^d \) for \( d = \sum_{i=1}^k d_i \). All iteration domains we consider will have a nonempty affine subspace \( H \) in its definition. For typical examples see Table [1].

Note that this definition is powerful enough to handle temporal constraints on iteration: we can add an artificial 1-dimensional operand whose indices designate the time points, and then add suitable constraints to the set \( H \) to indicate that some combination of indices of the other operands occurs at multiple time points during iteration.

Traditional reuse analysis is based on reuse vectors and reuse distances. This concept is not sufficient for high-dimensional iteration domains where a single vector cannot describe the full reuse potential. We instead define the reuse domain for a given data element of any operand.

Definition 3 (reuse domain). Let the \( k \) operands \( A_1, \ldots, A_k \) give rise to the iteration domain \( Q(A_1, \ldots, A_k) \cap H \). For a given index of any operand \( q \in Q(A_i) \), the reuse domain \( \mathcal{R}_i(q) \) is given by

\[
\mathcal{R}_i(q) = Q(A_1) \times Q(A_2) \times \cdots \times Q(A_{i-1}) \times \{q_i\} \times Q(A_{i+1}) \cdots \times Q(A_k) \cap H \\
= \{x \in Q(A_1, \ldots, A_k) \cap H : \pi_i(x) = q_i\}.
\]

Of course a reuse domain can be considered as a particular iteration domain. In fact, is is the best way to iterate over the subset of indices in the joint iteration domain projecting onto \( q_i \in Q(A_i) \) to ensure perfect reuse.
Definition 6 (distance). Given some set $X \subset \mathbb{Z}^d$ the set of elements between two points $x \in X$ and $y \in X$ (including the smaller and excluding the larger of the two) is designated by

$$[x, y]_X = [x, y]^X = \{ z \in X | x \leq z \land z \prec y \}.$$  

We can thus define a metric on $X$, the distance between $x$ and $y$ in the order restricted to $X$, as $\Delta_X(x, y) := ||x, y|^X| + ||y, x|^X|$ (at least one of the the summands will always be 0 since either $x \prec_X y$ or vice versa). We call $\Delta_X(x, y)$ the distance in $X$ between points $x$ and $y$. If $X$ and $\prec$ are clear from context we write $\Delta$ instead of $\Delta_X$.

2.3. Potential Conflicts. We will first categorize the necessary (but not sufficient) conditions for a cache miss, which we will call a potential conflict. Potential conflicts are the set of points in an iteration domain that map to the same set. This notion is independent of both ordering and reuse and says nothing about the actual cache misses that will be incurred – for this we need to consider orderings (see Section 2.4). First we will define potential conflicts occurring in a single operand, describe the structure of the miss spectrum using a mathematical lattice and then extend both the notion and the structure to define potential conflicts in iteration domains.

Definition 7 (Operand potential conflicts). Let $C = (c, l, K, \rho)$ be a cache specification with $N = \frac{c}{l}$ cache sets. Given a $(m, d)$-table $A$ with array $a(A)$ and an index map $\phi$ we say that $a_i$ is in potential conflict with $a_j$ if $i = j \pmod{N}$. The notion readily extends to all elements of $A$ through use of the index map $\phi$.

What structure emerges from operand potential conflicts? We will restrict attention in the following to affine and bijective index maps, i.e. $\phi(i_1, \ldots, i_d) = \sum_{r=1}^{d-1} w_r i_r + i_d$. Consider the points in $Q = [0, m_1 - 1] \times \cdots \times [0, m_d - 1] \cap \mathbb{Z}^d$, and their image under $\phi$. Then the points of the lattice $NZ = \{ Nz : z \in \mathbb{Z} \}$ in the interval $I = \{0, \ldots, m_1 - 1 \cdots, m_d - 1 \}$ induce a lattice $L = L(C, \phi) \subseteq \mathbb{Z}^d$ such that $\phi(L) = NZ$ since $\phi$ is an affine bijection. (We assume wlog. that $\phi$ maps $0 \in Q$ to $0 \in NZ$, i.e. is actually linear; otherwise consider the affine translate of $L$ by $q_A$.)

What are the generators of $L(C, \phi)$? They can easily be calculated from the definitions: For linear $\phi$ the lattice $L(C, \phi)$ is generated by

$$G = \{ x - y : x, y \in Q, \phi(x) = \phi(y) \pmod{N} \}.$$  

If $G$ is empty, there are no potential conflicts for the operand under $\phi$.

Observation 1. If $\phi(i_1, \ldots, i_d) = \sum_{r=1}^{d-1} w_r i_r + i_d$ is an affine bijective index map for table $A$ under cache specification $C = (c, l, K, \rho)$, then $A_{i_1, \ldots, i_d}$ is in potential conflict with $A_{j_1, \ldots, j_n}$ if and only if they are equivalent modulo $L(C, \phi)$, i.e. if $A_{i_1, \ldots, i_d} = A_{j_1, \ldots, j_n} + l$ for some $l \in L(C, \phi)$.

We will now extend this notion to describe potential conflicts for iteration domains. The notion extends easily to multiple operands as follows if we consider conflicts in memory. Let $A_1, \ldots, A_k$ be tables with index maps $\phi_{A_i}$ and joint iteration domain $Q = Q(A_1, \ldots, A_k)$. We say that two entries $p = (p_1, \ldots, p_k) \in Q$ and $q = (q_1, \ldots, q_k) \in Q$ are in potential conflict if the following condition holds:

$$\exists i \exists j : \phi_{A_i}(p_i) = \phi_{A_j}(q_j) \pmod{N}$$

In order to express this notion in the iteration domain directly, we leverage one existing concept from the polyhedral model \cite{ba}. Let $A_1, \ldots, A_k$ be tables with
iteration domains $Q(A_1), \ldots, Q(A_k)$ and translated self-conflict lattices $q_A + L(A_i)$. The access function mapping an iteration domain vector to an element in operand $A_i$ is $\pi_i : Q(A_1, \ldots, A_k) \rightarrow Q(A_i)$, the projection onto the $i$-th operand domain. The set of all potential misses in $Q(A_1, \ldots, A_k)$ is then
\[
G(A_1, \ldots, A_k) = \bigcup \Gamma_i(A_1, \ldots, A_k)
\]
where
\[
\Gamma_i(A_1, \ldots, A_k) = \{ x \in Q(A_1, \ldots, A_k) \cap H : \pi_i(x) \in q_A + L(A_i), i = 1, \ldots, k \}
\]
\[
= \bigcup_{q \in q_A + L(A_i)} R_i(q).
\]

Iteration domain potential conflicts appear exactly at points in $Q(A_1, \ldots, A_k)$ where multiple operand potential conflicts meet, as can be seen geometrically in Figure 2. Some points are included in $G$ from multiple $G_i$ and can be declared as follows:

**Definition 8** (potential conflict index-set, potential conflict level). A point $x \in G$ has potential conflict index-set
\[
T(x) = \{ i : x \in G_i, i \in \{1, \ldots, k\} \},
\]
and potential conflict level $|T(x)|$. For points $y \in Q(A_1, \ldots, A_k) \setminus G(A_1, \ldots, A_k)$ we set $T(y) = \emptyset$.

The set $G$ and the potential conflict set $T(x)$ together completely describe the potential conflicts in $Q(A_1, \ldots, A_k)$. This machinery will be used in subsequent sections to define, in combination with ordering information, actual cache miss counts.

2.4. **Actual Cache Misses.** We now want to study the geometry of sets of truly conflicting points. As every measure of actual cache misses depends on the ordering taken, we can first describe the conditions under which no such misses arise, or alternatively for the presence of cache misses, independently of the ordering.

**Definition 9** (Actual cache miss presence). Let $C = (c, l, K, \rho)$ be a cache specification with $N = \frac{c}{l}$ cache sets. Given a $(m_1, \ldots, m_d)$-table $A$ with array $a(A)$ and an index map $\phi$ we say that a set $S$ of points in $Q = [0, m_1] \times \cdots \times [0, m_d] \cap \mathbb{Z}^d$ will contain cache misses, if $\{ p \in S : |\{ x \in S : \phi(x) = \phi(p) \ (\text{mod } N)\}| > K \} \neq \emptyset$, i.e. if it contains at least one class of more than $K$ potentially conflicting points.

Note that this definition excludes cold misses (see section 1.3) since their presence is inevitable. Since $L(C, \phi)$ is a lattice we can first only consider sets with potential conflicts that contain $(0, \ldots, 0) \in \mathbb{Z}^d$, as all other nonempty sets behave similarly under a suitable translation. We later define the set of translations that complete the analysis for all sets.

Let us consider a subset $S$ of the integral points in the box
\[
[0, m_1 - 1] \times \cdots \times [0, m_d - 1] \cap \mathbb{Z}^d
\]
versus those in
\[
[0, m_1 - 1] \times \cdots \times [0, m_d - 1] \cap L(C, \phi).
\]

We know from Definition 9 that additional (non-cold) cache conflicts will arise whenever more than $K$ lattice points are contained in $S$. The actual number of
misses seen depends entirely on the ordering taken. The key measure in deciphering total miss volume is the per-set cache pressure between successive reuses of an operand’s data. This concept is similar to the reuse distance notion from basic compiler optimization [DZ03]. Classical reuse distance would reveal the number of total elements loaded between successive reuses of an operand’s data element. In our framework, we are interested in a subset of that number—the number of data elements loaded into a specific cache set between successive reuses, and we are interested in the union of such subsets to give the total measure. The remainder of this section shows how such a measure is formulated. We must first embed knowledge about the ordering taken through the iteration domain.

Let \( C = (c, l, K, \rho) \) be a cache specification and \( D \) the iteration domain. Let \( L(C, A_i) \) be the lattice in \( \mathbb{Z}^{\dim(A_i)} \) generated by \( C \) and operand \( A_i \) (for \( i \in \{1, \ldots, m\} \)). We extend the lattice \( L(C, A_i) \) for \( A_i \) by standard lattices in the other operand’s index spaces to form a \( d \)-dimensional lattice in \( D \) by

\[
\Lambda(C, A_i) = \mathbb{Z}^{d_1} \times \cdots \times \mathbb{Z}^{d_{i-1}} \times L(C, A_i) \times \mathbb{Z}^{d_{i+1}} \times \cdots \times \mathbb{Z}^{d_k}.
\]

Since the cache \( C \) remains constant we will refer to this simply as \( \Lambda(A_i) \). We will denote the projection of a point in \( x \in \Lambda(C, A_i) \) onto the \( i \)-th component of the product by \( \pi_i(x) \).

The joint set of conflicts arising from the operand lattices in \( D \) is given by

\[
\Lambda^D = D \cap \bigcup_{p=1}^{m} \Lambda(A_p).
\]

Each point in this set (which typically is not itself a lattice) represents a potential cache conflict through at least one operand. Some points represent conflicts arising
from multiple operands simultaneously. Counting the maximum possible multiplicity at every point yields an upper bound. But when traversing the points of \( D \) in the order given by \( \prec \) we might benefit from re-use. Assuming perfect reuse, we count one instance of each operand lattice only. This represents the lower bound. Since perfect reuse is atypical, both bounds may deviate significantly from the true number of cache conflicts.

For more information we consider the reuse domain \( \mathcal{R}_i(q) \) for a given index \( q \in Q(A_i) \). Let \( x \in \mathcal{R}_i(q) \) have subsequent reuse \( x' \in \mathcal{R}_i(q) \). The associated distance function \( \Delta(D(x, x')) \) then describes the cache pressure between \( x \) and \( x' \). We will count a cache miss at \( x' \) unless \( \Delta(x, x') \) is low enough to ensure that during traversal of \( A \) in the sequence prescribed by \( \prec \) the data indexed between \( x \) and \( x' \) cannot have evicted \( x \), i.e. when \( \Delta(D(x, x')) \leq K \) and \( x' \in L^D \). Only a single miss occurs when \( \Delta(D(x, x')) > K \), despite the extent to which the cache set handling \( x \) and \( x' \) is overfilled.

Denote the sequence of points of \( A_i \) traversed in the order \( \prec \) by \( S(A_i) = (x_1^i, \ldots, x_n^i) \). Each element in this sequence can be classified either as a ‘miss’ or a ‘reuse’: We call \( x_k^i \) a reuse point for \( A_i \) in \( A^D \) under \( \prec \) if and only if

\[
\{ x^i_j : j < k \land x^i_k \in R_i(\pi_i(x^i_j)) \land \Delta(D(x^i_j, x^i_k)) \leq K \} \neq \emptyset,
\]

i.e. if there exists a point earlier in the sequence for which \( x^i_k \) corresponds to a subsequent reuse, and the traversal distance is less than \( K \), the cache set associativity.

If no such earlier point exists, or if the distance of all these points is too large we call \( x^i_k \) a miss point. This partitions \( S(A_i) = S_{\text{miss}}(A_i) \cup S_{\text{reuse}}(A_i) \).

Given a set \( J \subseteq A^D \) we can thus count the number of cache misses as follows: For each point in \( x \in J \) we consider the potentially conflicting points \( T(x) \) and count only those that are miss points for the respective operand:

\[
\#\text{Misses}_J = \sum_{x \in J} \sum_{p \in T(x)} (1_{S_{\text{miss}}(A_p)}(x))
\]

where \( 1_X(x) \) is the indicator function for \( x \in X \).

This quantity is parametric in the cache specification, the table sizes (where padding may be allowed), the orders induced by the operand layout \( \phi_{A_i} \), but primarily by the iteration ordering \( \prec \). In this paper we will study the minimization problem subject to changes in \( \prec \).

3. Tiling Cache Miss Model and Code Generation

3.1. Tiling for Cache Performance. In Section 1.1 we made some informal observations about cache capacity and described the need to view cache models from the perspective of one cache-set. When considering iteration space tiling, this effect is particularly important. While much important work has been performed on iteration space tiling both using traditional compiler optimizations and in the polyhedral model, (as described in Section 1.2) selection of best-performing tile size and shape has remained more of an art than science, an so called auto-tuning solutions are often relied-upon to compute the best tile. Nowhere in the literature are tiles shaped and sized according to the natural structure imposed by the hardware. In this section we describe how tiles that are constructed according to the cache’s natural associativity lattice exhibit two clear theoretical advantages.
(a) Largest (half-open) rectangle with only 1 interior lattice point has volume 453 (see [GMM99, A7 in Tab. IV]). It is too large to be used in a regular tiling.

(b) Fundamental region of lattice has volume $|\det \begin{pmatrix} 5 & 7 \\ 61 & -17 \end{pmatrix}| = 512$

**Figure 3.** Tile volume difference between rectangular and lattice tiling. For illustration we use the lattice of [GMM99, Fig. 14], generated by $\begin{pmatrix} 5 & 7 \\ 61 & -17 \end{pmatrix}$. Note furthermore that if a rectangular tiling is constructed from a scaled copy of the rectangle containing more than one lattice point the number of integral points can vary across tiles, in a lattice tiling (b) it is constant (except at the boundary). (To simplify the picture instead of all integer points only those whose coordinates are divisible by 10, and the figure has been scaled in a 1:2 ratio in the y-direction.)

Let $A_1, \ldots, A_k$ be operands with index-sets $Q(A_i)$, index-maps $\phi_{A_i}$ and iteration domain $Q(A_1, \ldots, A_k) \cap H$. Let $C = (c, l, k, \rho)$ be a cache specification, and let the lattice $L(C, A_i)$ describe potential cache misses. Consider vectors $(l_1, \ldots, l_m)$ generating the operand lattice $L(C, A_i)$. Typical lattice generators are not aligned with the matrix dimensions, i.e. not simply integral multiples of unit vectors. Hence rectangular regions of the operand index set $Q(A_i)$ will have an unpredictable number of lattice points contained within as illustrated in Figure 3(a). Let us instead
consider half-open parallelepiped tilings that are formed from integral multiples of the lattice basis vectors. An example of such tilings is shown in Figure 3(b). There are two distinct theoretical advantages to such lattice tilings over the rectangular form. Firstly, adjacent tiles of tile (a) contain a variable number of lattice points and will therefore induce a non-constant number of cache misses. The implications of this from a cache perspective may be severe. Even if one rectangular tile was sized very carefully to minimize the number of cache misses, adjacent tiles may have a completely different cache miss behavior. This, combined with the community’s focus on rectangular tilings may explain why it has proven so difficult to provide clear guidance on tile size/shape. Adjacent tiles of type (b) contain identical numbers of lattice points, as long as the tiles are whole. Secondly, the volume of tiles of type (b) can easily be as much as 20% larger than tiles containing the same number of lattice points but of type (a). Even in the small example of [GMM99, Fig. 14] the best rectangular volume is 453, the one chosen by the authors has volume 416, while the parallelepiped volume of type (b) is given by \[ \det \begin{pmatrix} 5 & 7 \\ 61 & -17 \end{pmatrix} = 512, \] a saving of 13% resp. 24%. Greater tile volume can directly lead to greater performance since tile boundaries typically enforce cache misses.

3.2. Tiling Mechanics. We follow the tiling methodology of [GAK03]: A tile is the half-open parallelepiped generated by linearly independent vectors \( \{p_1, \ldots, p_d\} \), so that the matrix \( (p_1 \cdots p_d) \) bijectively identifies the unit cube with a tile, and the lattice points of the standard lattice \( \mathbb{Z}^d \) correspond to the footpoints of the tiles. Given some iteration domain \( D \subseteq \mathbb{Z}^d \) and writing \( H = (p_1 \cdots p_d)^{-1} \) the prototypical tile (or single-tile iteration space) starting at the origin is thus given by

\[ P_D(H) = D \cap \{ x \in \mathbb{Z}^d | 0 \leq x < p_i, i \in \{1, \ldots, d\} \} = \{ x \in D | 0 \leq \|Hx\| < 1 \}, \]

while the set of footpoints (or tile iteration space), i.e., the translation vectors to cover \( D \) with tiles \( P_D(H) \) is

\[ T_D(H) = \{ t | (p_1 \cdots p_d)t + P_D(H) \cap D \neq \emptyset \} = \{ t \in \mathbb{Z}^d | t = \|Hx\|, x \in D \}. \]

This makes \( D \subseteq P_D(H) + H^{-1}T_D(H) \), i.e., the Minkowski sum of \( P_D(H) \) and \( H^{-1}T_D(H) \) is a covering of \( D \).

When \( D \) and \( H \) are clear from the context we will simply write \( P \) for the tile and \( T \) for the translations. Abusing notation we write \( x \in P^t \) to denote \( x \in H^{-1}t + P \), a point in the affine translate of \( P \) by a transformed vector \( t \in T \).

The tiling transformation can be written as

\[ r : \mathbb{Z}^d \to \mathbb{Z}^d, \quad r(x) = \left( \frac{\|Hx\|}{x - H^{-1}[Hx]} \right), \]

i.e., \( r \) assigns to each point \( x \) the respective footpoint in \( T_D(H) \) in the first \( d \) coordinates, and the point inside the tile \( P_D(H) \) in the second \( d \) coordinates.

3.3. Cache Tiling Model. The cache miss counting scheme described in Section 2.4 extends easily to the tiled case. We want to first consider the joint set of conflicts arising from the operand lattices in the tile \( P^t = H^{-1}t + P \) rather than in \( D \), which is given by

\[ A^t = P^t \cap \bigcup_{p=1}^m \Lambda(A_p). \]
We will then consider the reuse domain $\mathcal{R}_i(q)$ for a given index $q \in P^t$. The analysis regarding subsequent points in $P^t$ is identical to that for $D$, and so we define the sequence of points of $\Lambda(A_i)$ traversed in the order $\prec_{A_i}$ by $S^t(A_i) = (x_0^i, \ldots, x_s^i)$, and partition it into miss and reuse as $S^t(A_i) = S_{\text{miss}}^t(A_i) \cup S_{\text{reuse}}^t(A_i)$ like before and restate Equation (1) for the tiled case as

$$\#\text{Misses}_J = \sum_{x \in J} \sum_{p \in T(x)} (1_{S_{\text{miss}}^t(A_p)}(x))$$

for every $J \subseteq \Lambda^t$.

4. Computational Results

In this section we describe computation results of using the associativity lattice tiling framework to accelerate matrix multiplication programs. We do not describe the implementation in any detail, except to say that it is a C++ framework that uses the packages ClooG \cite{Bas02} for loop bound generation and NTL \cite{Sho15} for integer math library support. The implementation currently can only perform tiling of matrix multiplication, along with associated solution checking against a library implementation (BLAS). In future work we will extend this framework to further dense linear algebra and to non matrix operations.

From a set of problem specifications, array layout characteristics, pointers to memory locations, padded dimensions etc, the implementation generates the associativity lattices of the operations and using equation (1) or (4) constructs the appropriate cache miss model. The best in a small search of tiling options is chosen and the the code generated using the tiling specification from section 3.2 and using the CLooG library.
4.0.1. **Lattice Tilings versus Compiler Optimization.** Figure 4 shows computational results of tiling using the associativity lattices against various compilers and flags. In general, the lattice tiling performs much better than expected. Some compilers, such as *pgi* do not seem to be able to enable cache tiling for this problem and their performance is many times slower than our lattice tiling. Compared to unoptimized code (*gcc -O0*), the lattice tiling produces a speed-up of 10 to 20. Against the more typical optimization level *gcc -O2*, our framework gives a speed up of around 2-6 times. Our framework sometimes gives no advantage over *gcc* with aggressive optimization while for other problems, we see a clear 2-3 times speedup. The Intel compiler with aggressive optimization is able to tile for cache usually as well as the lattice tiling.

We consider the performance improvements from lattice tiling surprising because currently we only tile for a single level of the memory hierarchy. These results were obtained by tiling for L1 cache on the Intel Haswell Architecture. In future work, we will present results for multiple levels of tiling.

4.0.2. **Rectangular versus Lattice Tilings.** Figure 4 compares the results of best rectangular tilings versus best lattice tilings. Although we have described clear theoretical advantages of lattice tiles versus rectangular tiling, the two methods appear quite close in performance. The reason for this is that while lattice tiles improve addressable volume they also display worse spatial reuse characteristics, as shown in Figure 5. Given the preliminary state of our implementation we believe that a significant advantage of the lattice tiling for certain problem sizes can be exhibited with a properly tuned code generation procedure as implemented by the compiler optimization passes for rectangular tiles.

4.0.3. **Auto-Threading.** Our tiling implementation also displays basic automatic parallelization capabilities using openMP directives. The speed-up of our generated codes versus *gcc-graphite*, another automatically parallelizing polyhedral compiler, are shown in Figure 6. For the problem size chosen, our framework was able to generate parallel codes that exhibit speed-up on 20 threads of 20 Intel Haswell cores. On the other hand, *gcc-graphite* was able to produce speed-ups only up to 4 threads.
4.0.4. Analysis/Model Cost. The cost of direct evaluation of Equation (4) is exponential and thus an efficient implementation is not possible. This should not be a surprise, since Equation (4) precisely evaluates every case miss in the code region of the iteration domain, and full evaluation of that requires a similar number of data accesses to the code being modeled. In its raw form then, Equation (4) is no improvement over the CME approach described in [GMM97] and could not be incorporated into a compile-time or time optimization framework. Our approach however, unlike the CME approach leads to a solution set with a clear structure that can be exploited in many ways, making it unnecessary to generate the full, intractable solution set. Equation (4) is evaluated for every tile in the domain and for every set in the cache. An improvement to our method would model a few certain tiles for a few certain sets using a sampling approach. The details regarding which tiles and sets to select are sufficient to fill a follow-on paper. However, we believe that sufficient structure is expressed using the lattice framework, and that sufficiently robust mathematical toolsets exist such that only a small fraction of the analysis in (4) can be actually evaluated, while still providing reliable approximate cache miss information about the whole code.

We also here describe an alternative approach, that uses a common-sense tiling mechanism rather than being driven by cache miss modeling. Since lattice tiles can be constructed without counting lattice points explicitly, then a sensible tiling can be constructed by choosing a known number of lattice points to be contained from the operand that is tiled by lattices. We would choose the number of lattice points in the tile to be in the range \([K - \alpha, K + \beta]\). We would expect that \(\beta = 0\) since traversing more than \(K\) points in the operand’s tile would mean that no reuse could occur between tile slices. We would expect that \(\alpha\) would be small, e.g. \(\alpha = 2\) or \(\alpha = 1\). Experimentally we have observed that lattice tiles that contain \(K - 1\) lattice points perform well and so for our experiment this is chosen. The remaining operands will be tiled rectangularly with sizes induced by the first operand’s lattice.
tile shape. The cost of this tiling analysis is dominated by lattice basis reduction using the NTL library, which is not significant for the low dimensional lattices and the (possibly padded) matrix dimensions appearing, which are often powers of two. We envisage a hybrid approach where direct analysis is performed and a small search of modeled tiles is evaluated to decide which of the small sample set is optimal.

References

[AGLV02] J. Abella, A. González, J. Llosa, and X. Vera, Near-optimal loop tiling by means of cache miss equations and genetic algorithms, Parallel Processing Workshops, 2002. Proceedings. International Conference on, IEEE, 2002, pp. 568–577.

[AL93] Jennifer M. Anderson and Monica S. Lam, Global optimizations for parallelism and locality on scalable parallel machines, Proceedings of the ACM SIGPLAN 1993 Conference on Programming Language Design and Implementation (New York, NY, USA), PLDI ’93, ACM, 1993, pp. 112–125.

[Bas02] C. Bastoul, Generating loops for scanning polyhedra, Tech. Report 2002/23, PRiSM, Versailles University, 2002, Related to the CLooG tool.

[Bas04] Cédric Bastoul, Contributions to high-level optimization, Habilitation thesis, Université Paris-Sud, December 2004.

[BHRS08] Uday Bondhugula, Albert Hartono, Jagannathan Ramanujam, and Ponnuswamy Sadayappan, A practical automatic polyhedral parallelizer and locality optimizer, ACM SIGPLAN Notices 43 (2008), no. 6, 101–113.

[CCH08] Chun Chen, Jacqueline Chame, and Mary Hall, Chill: A framework for composing high-level loop transformations, Tech. report, Citeseer, 2008.

[CP03] Calin Căscaval and David A. Padua, Estimating cache misses and locality using stack distances, Proceedings of the 17th Annual International Conference on Supercomputing (New York, NY, USA), ICS ’03, ACM, 2003, pp. 150–159.

[DZ03] Chen Ding and Yutao Zhong, Predicting whole-program locality through reuse distance analysis, Proceedings of the ACM SIGPLAN 2003 Conference on Programming Language Design and Implementation (New York, NY, USA), PLDI ’03, ACM, 2003, pp. 245–257.

[GAK03] G. Goumas, M. Athanasaki, and N. Koziris, An efficient code generation technique for tiled iteration spaces, Parallel and Distributed Systems, IEEE Transactions on 14 (2003), no. 10, 1021–1034.

[GMM97] Somnath Ghosh, Margaret Martonosi, and Sharad Malik, Cache miss equations: An analytical representation of cache misses, Proceedings of the 11th International Conference on Supercomputing (New York, NY, USA), ICS ’97, ACM, 1997, pp. 317–324.

[GMM99] ______, Cache miss equations: A compiler framework for analyzing and tuning memory behavior, ACM Trans. Program. Lang. Syst. 21 (1999), no. 4, 703–746.

[HP11] John L. Hennessy and David A. Patterson, Computer architecture, fifth edition: A quantitative approach, 5th ed., Morgan Kaufmann Publishers Inc., San Francisco, CA, USA, 2011.

[LRW91] Monica D Lam, Edward E Rothberg, and Michael E Wolf, The cache performance and optimizations of blocked algorithms, ACM SIGOPS Operating Systems Review 25 (1991), no. Special Issue, 63–74.

[RS92] J. Ramanujam and P. Sadayappan, Tiling multidimensional iteration spaces for multicomputers, Journal of Parallel and Distributed Computing 16 (1992), no. 2, 108 – 120.

[Sho15] Victor Shoup, NTL: A library for doing number theory, 1990-2015.

[YLR+05] Kamen Yotov, Xiaoming Li, Gang Ren, MJS Garzaran, David Padua, Keshav Pingali, and Paul Stodghill, Is search really necessary to generate high-performance BLAS?, Proceedings of the IEEE 93 (2005), no. 2, 358–386.