Silicon edge-dot architecture for quantum computing with global control and integrated trimming

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A scalable quantum information processing architecture based on silicon metal-oxide-semiconductor technology is presented, combining quantum hardware elements from planar and 3D silicon-on-insulator technologies. This architecture is expressed in the “unit cell” approach, where tiling cells in two dimensions and allowing inter-cellular nearest-neighbour interactions makes the architecture compatible with the surface code for fault tolerant quantum computation. The architecture utilises global control methods, substantially reducing processor complexity with scale: Single-qubit control is achieved using globally applied spin-resonance techniques and two-qubit interactions are mediated by large quantum dots. Further, a solution to device variation is proposed through integration of electronics for individual trimming of quantum dot voltage references. Such a combined set of solutions addresses several major barriers to scaling quantum machines within completely silicon based architectures.

Universal quantum computers with fully scalable architectures are necessary to solve meaningful problems that are intractable on digital computers. Through quantum error detection schemes applied to qubit lattices [1], these computations can be made fault-tolerant. This process involves encoding partitions of many physical qubits into separate logical qubits, and works by invoking a trade-off between the number of physical qubits and their error rates. This approach is expected to result in significant qubit overheads required to achieve meaningful computational capabilities. For example, it is predicted that $O(10^8)$ qubits operating with error rates at or below $10^{-3}$ are required for the non-trivial execution of Shor’s factoring algorithm [2]. This requirement makes scaled architectures in silicon particularly attractive; the low form-factor of a silicon quantum dot produced by 300 nm wafer technologies in contemporary foundries [3–5] results in achievable qubit densities as high as $O(10^3)$cm$^{-2}$, while the compatibility with a highly developed and globally accessible silicon device fabrication industry presents several advantages, ranging from on-chip integration with metal-oxide-semiconductor (MOS) digital hardware [6–8] to high-volume device production and dissemination.

Hardware architecture approaches for fault-tolerant machines within the silicon MOS materials platform have largely focused on devices formed at, or near, a planar silicon / silicon oxide interface [9–13] with the lithographically defined metallic gates (or gate stacks) used to confine and/or define qubits. In direct contrast to these planar device approaches, the concept of an “edge-dot” is introduced to the reader here. Quantum dots of this type are similarly produced in 3D silicon-on-insulator (SOI) technology, where carrier confinement is naturally produced by the electric field concentration in the cross-sectional corner of an etched silicon nanowire, applied by an overlapping gate electrode [14]. The length of the dot in the overlapped region acts to confine the quantum dot in the remaining dimension. These systems have been extended to produce bilinear arrays of quantum dots through the development of “split-gate” devices [15], and can extend into an arbitrary arrays of $2 \times N$ quantum dots [16–18] simply based on the number of electrodes patterned. Recently, the concept of utilising floating gate electrodes [19] as a method to sense or couple charges in parallel running nanowires has been achieved [20, 21], opening this nanowire approach to scalable architectures beyond the dimensions of $2 \times N$.

Here, this approach is conceptually extended by asserting that these quantum dot structures do not need to be produced in the corners of a thin nanowire; but instead these dots can form a $1 \times N$ array along a single edge of some silicon “plateau”, which is of arbitrary width in the dimension perpendicular to the edge defining the dot array. This use of topography within the silicon layer has the potential to combine advantages from two prevalent approaches of forming quantum structures in semiconductors including planar [22, 23] and 3D SOI [3] which have, to date, remained as separately developed host technologies for quantum devices. This work illustrates how this hybridised approach to formation of silicon quantum devices has advantages when approaching the challenge of integrating elements of a quantum-classical interfacing layer [7, 24–26], particularly focusing on the formation of 2D qubit lattices for the execution of error correction codes.

In this paper a “unit cell” hardware sub-structure is presented which directly reflects the tile-like nature of error detection algorithms when applied to the physical qubit layer. Here, the surface code [27] is studied as it has advantages of requiring a 2D qubit lattice with nearest neighbour interactions and can tolerate compound errors as high as 1%. This unit cell approach has additional advantages towards device scalability through the definition of a single, reproduced structure which forms the

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foundations of the quantum machine. Further, through shared control of all cells [10], the input signal overheads required can be drastically reduced [6, 7, 26] to scale with the unit cell size, rather than the total number of physical qubits within the quantum machine.

The remainder of this work is structured as follows: the physical hardware unit-cell is first presented in § I, followed by a discussion in context with the current state-of-the-art on the operations required to execute universal quantum computing with this cell in § II. This physical architecture is mirrored by an algorithmic unit-cell protocol for execution of the surface code, as outlined in § III. This section highlights how the error detection scheme can be implemented while applying completely global electron spin resonance pulses to all spins (data and ancilla) for the execution of the necessary single qubit gates, with the feasibility and control methods discussed in § IV. Finally, it is acknowledged that slight variations in the hardware can easily result in one location of any two different unit cells exhibiting very different behaviour under the same globally applied control conditions. Therefore, for the unit cell approach to be a success, contingencies intrinsic to the hardware cell must be present to ensure enough uniformity can be realised artificially. A method to address this challenge is proposed in § V, through circuitry designed to “trim” the DC voltage offsets supplied to each physical qubit via the integration of non-volatile analogue memories as a silicon MOS hardware overhead. The example presented here integrates floating gate transistors into the control circuitry for each quantum dot.

I. HARDWARE UNIT CELL FOR AN EDGE-DOT ARCHITECTURE

Each hardware unit cell is constructed around a single silicon plateau which facilitates the formation of quantum dot structures along the plateau boundary while also hosting standard techniques seen in planar device formation in locations away from the boundary as shown in Fig. 1a). These include the formation of implantation regions and carrier reservoirs, tunnel barriers and quantum dots. The quantum dots formed at the plateau boundary take advantage of the electric field concentration in the cross-sectional corner due to the overlapping gate electrode, resulting in strong carrier confinement [14, 28]. The length of the gate in the overlapped region acts to confine the quantum dot in the remaining dimension.

A recent scaled architecture proposal [29] illustrated several advantages of how the integration of a spinless mediator quantum dot [30, 31] connected to a charge reservoir could facilitate robustness against certain types of leakage errors in the form of physical charge movement, which would otherwise be highly detrimental to a schemes based on repeated execution of stabilizer cycles. A blueprint for a scaled quantum machine utilising the edge-dot approach, producing a 2D array of qubits interconnected via mediator dots, is illustrated in Fig. 1b).

A more detailed picture of the primitive hardware unit cell for this scaled quantum machine is shown in Fig. 1c-i), including the Front End of Line (FEOL) consisting of the physical qubit layer and supporting hardware defined by the silicon plateau, and Back End of Line (BEOL) consisting of routing metal layers for control. Each corner of the plateau is connected to a neighbouring plateau (the next adjacent hardware cell) via a shared nanowire with patterned split-gate elements acting to form a double quantum dot site. These quantum dots can be populated with charge carriers from the reservoir via the mediator quantum dots [29], and act to house the physical qubits upon which the computations and error correction codes are performed. The charge reservoir consists of an ohmic implantation site illustrated in Fig. 1c) as an exposed central region of the plateau which is directly contacted by a metallic via (black squares in Fig.1d-h). The planar surface of this silicon plateau is further utilised to distribute charge from this central reservoir to each edge through a metallic accumulation gate patterned in polycrystalline silicon (poly-silicon) Layer 1 in Fig. 1d). Tunnel barriers between the accumulated reservoirs and the edge defined quantum dots can be formed either through engineered gaps [3, 32] or dedicated barrier gates [33, 34] seen patterned in poly-silicon Layer 2 in Fig. 1d). The plateau edges are overlapped with gate electrodes in poly-silicon Layer 1 which act to confine elongated quantum dots through the concentration of electric fields in the gate-edge overlap region. The plateaus are interconnected at the corners by a narrow silicon channel, commonly referred to as a “nanowire”, where split-gate technology [15] is used to form a double quantum dot via features in poly-silicon Layer 1 and tunable tunnel barriers via electrodes in poly-silicon Layer 2. The tunnel barriers are utilised to interface quantum structures formed in the nanowires with those formed at the edges of connected plateaus. For the long plateau edges, a mediator quantum dot is formed [31], which serves to transfer qubit information between the quantum dots at each endpoint [29, 30]. The mediator dots have the additional advantage of introducing a means through which quantum information processing hardware elements can be physically separated to allow for efficient signal routing and integration of control or sensing peripherals required at the intra-hardware-cell level. In the example illustrated, the mediator dot is required to be $\sim 5 \times$ the pitch of the BEOL metal routing, allowing for inter-cell connective routing of the FEOL elements as well as routing between metal layers. Space in the FEOL for integrated peripheral hardware can be seen as the (empty) regions between plateaus (grey), amounting to an area approximately equivalent to the plateaus. A diagram illustrating interconnected plateaus is provided in Supplementary Fig. S1.

II. SILICON QUBIT INITIALISATION, READOUT AND CONTROL

For the execution of the surface code cycle, as detailed in § III, two varieties of qubit are utilised simultaneously;
single electron spin qubits for data qubits and singlet-triplet qubits for ancillas (X and Z syndromes). For the control of single electron spins, electron spin resonance (ESR) methods have recently shown control fidelities of up to 99.96% utilising optimised pulse schemes operating over 8 µs timescales. As shown in later sections, pulse optimisation schemes such as these transfer well to globally applied spin manipulation.

For readout, the effect of Pauli spin blockade on inter-dot tunnelling enables in-situ double-dot readout for the syndrome qubit state, with high fidelity single-shot Pauli spin blockade detected in several implementations of silicon MOS quantum devices [39–41]. This readout method, combined with gate-based reflectometry measurement techniques [40, 42, 43] results in a scalable approach to rapidly reading qubit states without the need for integrating additional charge-sensing hardware infrastructure within the FEOL. Some examples in silicon devices have shown readout fidelity of 99.7% in 300 ns [43], with others showing extrapolations to 99.9% fidelity achievable in comparable timescales to the single spin qubit gates [44].

For initialisation, the triplet lifetimes within the spin blockade region is seen to vary based on species, from 200 µs for $|T_0\rangle$ and up to 5 ms for polarised triplets [42, 45], however for initialisation of the singlet state, this triplet lifetime can potentially be reduced through the use of relaxation hot-spots [46, 47], particularly the spin-orbit driven $S/T^Z_1$ anti-crossings found either side of the primary singlet anti-crossing, or through selective tunneling with nearby reservoirs [48, 49].

For two-qubit gates, the nearest-neighbour exchange
interaction has lead to several realisations \([23, 34, 47, 50–52]\), resulting in scaling proposals based on densely-packed two-dimensional arrays of quantum dots \([9, 10]\), or protocols involving the transport of qubits along long chains of dots \([33]\). Other solutions such as photon-mediated two-qubit interactions are accessible through hybrid material platforms \([54, 55]\).

Alternative methods which maintain compatibility with the materials and processes used in the silicon device industry is to mediate a next-nearest-neighbour exchange through empty \([20]\), or multi-electron dots \([31]\). The mediating structures focused upon here take the form of elongated quantum dots which have nearest-neighbour exchange coupling between itself and a quantum dot at each endpoint (see Fig. 1b,c). This elongated quantum dot does not contain any quantum information and only acts to mediate a next-nearest-neighbour interaction between the two sites at each endpoint through the Ruderman-Kittel-Kasuya-Yosida exchange interactions \([30]\). For a multielectron dot occupied by the first two electrons (or equivalent \(S=0\) ground-state), the exchange energy \(J_{DA}\) between a data (D) dot and ancilla (A) dot, through the mediator (M), is approximated by \([29, 30]\)

\[
J_{DA} \simeq \frac{t_{DM}^2 t_{AM}^2}{\varepsilon_{DM} \varepsilon_{AM} \delta_{M}},
\]

where \(t_{DM}\) (\(t_{AM}\)) is the tunnel coupling between the data-mediated (ancilla-mediated) dots, \(\delta_{M}\) is the excited state energy on the mediator with \(\varepsilon_{DM}\) (\(\varepsilon_{AM}\)) the energy detuning of the data (ancilla) dot from the mediator excited state. A final element required for this scheme is coherent shuttling of a single electron spin qubit between double-dot locations. Shuttling has been shown to have negligible effect on spin projection, with a recent study showing spin polarization is maintained when shuttling between two sites with a fidelity of \(>99.9\%\), with \(>99\%\) for phase coherence \([57]\). Further, accurate charge shuttling across arrays of up to 9 dots \([58]\), and relative shuttling uncertainties below 50 parts per million \([59]\) have also been demonstrated.

III. SURFACE CODE UNIT CELL

The algorithmic unit cell representing the surface code is illustrated in Figure 2a), executing an interleaved XXXX and ZZZZ stabilizer. Utilizing strategic timing for state preparation and measurement of syndromes, the code cycle can be made compatible with the “tick-tock” method of executing algorithms using globally applied single qubit Hadamard gates and selective CZ gates \([35]\). The effective CNOT operations are highlighted by coloured grouping of Hadamard and CZ gates in Fig. 2a). The use of globally applied single qubit operations results in all unit cells within the quantum machine being controlled by the same input ESR signal. The approach requires embedding the quantum machine within a large peripheral 3D cavity, and the feasibility considerations for this solution is discussed in § IV. The schematic of a single edge-dot hardware cell capable of executing this stabilizer code is illustrated Fig. 2b). To execute the error correction process across the surface of the quantum machine, the unit cell must be interconnected to adjacent cells. This is achieved by positioning the ancilla...
and data quantum dots on the unit cell boundary, while the mediator dots (which result in the CZ operations between qubit locations), are enclosed within a cell boundary. The inter-cell operations are shown as the grey CZ connections within the surface code protocol in Fig. 2a), executed through the mediators external to the hardware cell boundary in Fig. 2b) where the equivalent dot positions in adjacent cells are indicated by a prime notation (e.g. $X_1', Z_2'$).

Much like the primitive cell of a crystal lattice structure, where elements are shared when located at a vertex, edge or face, the unit cell here contains on average 4 dots and (for this implementation) 3 spin 1/2 particles attributed to qubits, plus an additional 4 mediator dots. The two data qubits D1 and D2 bounding the cells consist of a single spin 1/2 particle, each contained within one of two possible quantum dots $A$ or $B$. During the execution of the code cycle, the data spin qubit is shuttled between the dots $A$ and $B$ in order to access and complete all necessary operations between ancillas. In Fig. 2, dot locations D1$_{A,B}$ and D2$_{A,B}$ are illustrated, with the physical spin qubits indicated in Fig. 2a) as the solid traces while the empty occupancy of dots are denoted by the dashed traces.

A detailed breakdown of the 12 individual time steps within the surface code cycle seen in Fig. 2a) is presented in Supplementary Note S.S1. The use of singlet-triplet based syndrome qubits is compatible with the global ESR in Supplementary Note S. S1. The use of singlet-triplet within the surface code cycle seen in Fig. 2a) is presented while the empty occupancy of dots are denoted by the dashed traces.

IV. GLOBAL CONTROL OF SPINS USING A CAVITY PERIPHERAL

It is asserted that universally applied, or “global”, signals acting as a control input for all qubits across all cells is a desirable property for this approach to scaled quantum systems. Several proposals have also highlighted the potential use of globally applied AC fields for scaled systems of spin qubits, controlling either the entire ensemble of qubits [6], or sub-ensembles [9, 10]. One approach to achieving this is to embed the silicon devices within a microwave cavity [60]. Here, the feasibility of achieving sufficiently uniform global control on the ensemble of single qubit spins within the silicon quantum dot array is discussed.

For electron spins in silicon, the spin-orbit interaction is weak when compared to other semiconductors, but still remains appreciable. The surface-roughness of the Si/SiOx interface is predicted to result in an uncontrollable distribution in the Landé $g$-factor of up to $\delta g = \mathcal{O}(10^{-2})$ [61]. It has been shown that this value is tunable based on changes in the electrostatic field environment [22, 62, 63], however this degree of the Stark shift seen experimentally remains $\Delta g \simeq \mathcal{O}(10^{-4}) - \mathcal{O}(10^{-3})$ [23, 62]. Thus, for a quantum device operating at appreciable applied magnetic field ($B_0 \sim 1T$), the Stark shift of the electron $g$-factor can act as a potential source of local tunability, but cannot compensate for the entire $\delta g$ distribution. Therefore, the quantum machine must operate within the limits of broadband microwave pulsing techniques, requiring fields substantially lower than 1T [6, 10] or otherwise operate with composite pulsing schemes requiring a train of pulses [64]. For this proposal, high $B_0$ fields are necessary for the implementation of the charge leakage protection schemes [29], however pulse trains that are substantially longer than the single qubit $\pi$-rotation time are an undesirable solution as they can absorb significant fractions of the $T_2$ coherence time budget for active qubits. As a compromise, amplitude modulation (AM) techniques can be integrated into the control.

For a quantum gate applied via a resonant microwave AC driving field, it is convenient to define the control signals $I_0(t)$ and $Q_0(t)$ as the in-phase and quadrature components of an envelope function with carrier frequency $\omega_0$ [36]. This carrier is typically set by the Larmor frequency of the individual electron $g$-factor $g_e$, here it is set by the mean of the $\delta g$ distribution. In this rotating frame, the qubit control Hamiltonian appears as

$$H_Q = I_0(t)\sigma_x + Q_0(t)\sigma_y + \delta \omega \sigma_z,$$

where $\sigma_i, i \in \{x, y, z\}$ are the Pauli matrices, and $\delta \omega$ represents the frequency detuning of any single qubit from the mean of the $\delta g$ distribution. Amplitude modulation can be employed as a method to expand the number of resonant peaks in the frequency domain from a single peak at $\omega_0$, to multiple sets of side-bands that are frequency-shifted copies of the pulse envelope set by $I_0(t)$ and $Q_0(t)$. An amplitude modulation scheme which can be utilised to increase the number of resonant peaks output by the cavity from a single peak, to $N$ peaks separated by frequency $\omega_{AM}$ and centred at $\omega_0$ is detailed further in Supplementary Note S.S2. Thus, the Stark shift can operate such that $\delta \omega = 0$ for the qubit Hamiltonian in Eq. (2) by tuning the resonant frequency of each electron to the nearest side-band within the set $\omega_0 \pm n \cdot \omega_{AM}$ for $n \in [0, (N - 1)/2]$ (odd $N$) or $\omega_0 \pm (n + 1/2) \cdot \omega_{AM}$ $n \in [0, N/2]$ (even $N$). It is expected that $N \simeq 10 - 100$ is required to span the frequency bandwidth created by the range of $g$-factor distribution $\delta g = \mathcal{O}(10^{-2})$, given a stark shift range of $\Delta g \simeq \mathcal{O}(10^{-4}) - \mathcal{O}(10^{-3})$.

Recent studies have shown how Gradient Ascent Pulse Engineering (GRAPE) techniques [65, 66] have been utilised to design broadband pulses that can account for local environmental noise, pushing single qubit control fidelity to the limit of incoherence [36]. For systems in which individual qubit tunability is necessary for the uni-
FIG. 3. | Global ESR Control Scheme a) GRAPE pulse envelope executing a Hadamard gate utilising 6× the duration required for a π rotation under a square pulse approach. The black dashed lines indicate a filter function equivalent to a cavity quality factor of Q=250. b) Pulse infidelity as a function of qubit detuning referred to the electron g-factor, comparing the square and GRAPE solutions for the Hadamard gate with positive (solid) and negative (dashed) detuning offsets. c) Maximum infidelity envelope for each of the 10 sidebands for both the GRAPE and Square pulse Hadamard gate methods when embedded within the Amplitude Modulation scheme outlined in the main text. Colour darkens for increasing sideband frequency. The rapid decrease in infidelity as a function of increasing side-band separation ω_{AM} for the GRAPE pulse compared to the Square pulse indicates reduced effects of cross-talk capable for pulse engineering solutions. d) A Controlled-Z (CZ) pulse envelope executed by a square pulse on Exchange energy E_J compared to a GRAPE solution. Globally applied Ch:I, Ch:Q and selectively applied E_J GRAPE signals can be combined to produce a decoupled CZ pulse when E_J GRAPE is combined with Ch:I and Ch:Q signals. A decoupled identity operation on the two qubits is in effect for locations when E_J GRAPE is set to zero. e) Pulse infidelity as a function of g-factor referred detuning offset applied to a single qubit. f) First order filter functions for single-qubit and two-qubit control signals described in a) and d). The filter function given by a Free Induction Decay (FID) over 6 μs is indicated for comparison. The CZ Square pulse is omitted due to close similarity to the FID.

Formity of global control signals across a large array of qubits, these GRAPE methods can also be viewed as a scheme for mitigating errors in qubit tuning. Figure 3a) shows a GRAPE solution for the I_0(t) and Q_0(t) envelopes required to produce a Hadamard gate, delivering a high fidelity operation over a larger bandwidth for robustness against tuning errors or small drifts in δg. The offset error in the tuning via the Stark shift ∆g which the gate can tolerate for given target fidelity can be seen in Fig. 3b). The solution results in a more complex trajectory over the Bloch sphere as seen in Supplementary Figure S2, requiring 6× the time of a π rotation produced by a square pulse with the same amplitude limits (set as a 1 μs square pulse π rotation at B_0 = 1T). The resulting GRAPE pulse has better performance against low frequency noise coupled via the δω term in Eq. (2) as illustrated by the first order filter transfer function in detuning F_2^{(1)} [67] as seen in Fig. 3f). Similar to the methods in Ref. [36], the operation is trained against realistic qubit environmental noise [68]. While GRAPE methods can result in frequency-broadened qubit drive lines offering a robustness to tuning errors, combining this with amplitude modulation results in the presence of multiple broadened side-bands that can also interfere with each other. The infidelity of N=10 simultaneously driven peaks as a function of modulation frequency ω_{AM} is seen in Figure 3c), showing disruptive levels interference between side-bands under small ω_{AM} peak separations, however a much smaller separation in ω_{AM} is seen to be required by a solution utilising GRAPE when compared to the square pulse solution. Figure S3
illustrates the full infidelity-envelope for the amplitude modulation method described in Eq. (S1), where N=10 peaks are simultaneously produced. A limit of $\omega_{AA} > 4\text{MHz}$ is observed to gain a region of Hadamard infidelity $1 - F_H < 1 \times 10^{-3}$ corresponding to a $g$-factor tunability range of $\Delta g \approx 4.5 \times 10^{-4}$ to move between two neighbouring peaks, or equivalently $\Delta V = 22.5\text{mV}$ utilising $\partial g/\partial V = 0.002/V$ motivated from Ref. [23, 62]. The requirement on the Stark shift of $\Delta g \approx 4.5 \times 10^{-4}$ falls within the expected range of $O(10^{-4}) - O(10^{-5})$, although this threshold could be improved through more advanced optimisation acting to reduce the cross-talk.

Pulse engineering methods can also be utilised for two-qubit gates [69], where the globally applied ESR field can assist in decoupling action from local qubit noise. The mediated exchange energy in Eq. (1) can be incorporated 

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Figure 4 illustrates a circuit schematic diagram showing two potential methods for the working principles of the trimming circuit; Fig. 4a) which operates as a source follower (buffer circuit) configuration through reduction of the single setpoint voltage $V_{DD}$ through resistive division and Fig. 4b) which operates through supplying the stored potential as a direct reference for the quantum device. The resistive element $R_D$ within the equivalent circuit of a single quantum dot, is produced by the cumulative gate leakage to ground present in CMOS processes [72]. The circuit elements $M_{T(a,b)}$ shown in Figure 4 are central to performing the trimming, possessing salient characteristics similar to that of a floating-gate MOSFET including a tunable threshold voltage and non-volatility.

By trimming the threshold voltage of the device, the channel resistance in deep sub-threshold operation of the device $M_{T(a)}$ in Fig. 4a) can become comparable to $R_D$, resulting in an active voltage division which reduces the value of $V_{DD}$ down to some desired value (which is presumed in this instance to target a qubit resonance line through the Stark shift discussed in § IV). A more detailed feasibility study of this resistive trimmer configuration is presented in Supplementary Note S. S3. The threshold voltage is tuned through charge storage within the device, converted to a voltage through the capacitance relationship. For $M_{T(b)}$ in Fig. 4b), the stored charge within the device can be more directly converted into a voltage reference in a similar fashion to a previous proposal utilising dynamic random access memory (DRAM) [9]. Here, the voltage reference is delivered directly to the quantum device through a direct connection between the gate electrode defining the quantum dot and the charge storage element within the memory component $M_{T(b)}$. For the solution shown in Figure 4, three additional MOS devices must be integrated for each trimmed object within the unit cell. A cross-bar addressing scheme is utilised for individual trimming devices $M_{T(a,b)}$ across the unit cell, which becomes active during a pre-computation tunning phase for the quantum machine. The threshold voltage is selectively tuned through signal input $V_P$ which is connected, through activated $M_P$, to the $M_T$ trimming devices. Word-line and bit-line voltage $V_{WT}$ and $V_{BT}$ combine through tuning-enable transistors $M_{ET}$, activating a selected $M_P$. Based on the hardware unit cell architecture discussed in § I, the elongated mediator dots which interconnect data and ancilla qubits allow for a certain amount of physical space [29] in-between the silicon plateaus where these devices can be laid out in the FEOL layer, avoiding vertical circuit integration in the form of stacking control transistor layers above the the quantum FEOL [9]. The characteristic of non-volatility assumes operation within a consistent thermal environment and is deliverable by standard MOS memory hardware [71]. This is essential for the device $M_{T(a,b)}$ as, after tuning each device to the desired set-point, the selector crossbar architecture as shown in Fig. 4 becomes idle, allowing the circuitry to be powered down more completely, reducing latent power consumption or heat load. Stability characteristics of the device must be such that the set memory state does not drift appreciably over time, as this would contribute to errors in $\Delta g$. In this instance the stability requirements are defined by the high-fidelity region of the broadband pulses discussed in § IV.

**DISCUSSION**

Here, a solution is proposed to manage resources at the quantum-classical interface within a scaled processor through integration of MOS structures at the FEOL quantum hardware level. The additional hardware is required to combat device-to-device variation which is a principle challenge when scaling quantum machines [73]. The different aspect ratio between the qubit layer and the data processing layers can also complicate this quantum-classical interface [9], which can be avoided through the use of elongated mediator dots [29] or shutting qubits through 1D dot chains [53], as well as de-embedding single qubit control to be executed globally via a 3D microwave cavity [60]. This scaled quantum machine can be achieved through the hybridisation of SOI nanowire technologies [3] with planar quantum dot structures [33], producing an “edge dot” platform where the quantum dots are defined at the geometric boundary of a raised silicon plateau.

The hardware cell presented here is also extremely flexible, with the capacity to be re-configured to operate the surface code for different control schemes. For example, forgoing globally applied ESR of electron spins in the pursuit of an all-electrical control scheme can still utilise this same hardware architecture, with the addition of integrated micromagnet arrays [74] into the FEOL. This approach can potentially utilise the space outside the device in each alternating cell to incorporate diagonal micromagnets between the data qubit locations. This produces an engineered magnetic field gradient across each data-qubit double-dot, which can facilitate single qubit rotations [75]. In combination with the capability of tuning the stark shift via the trimming circuit, the amplitude modulation scheme presented here is also directly transferable to a globally applied EDSR control signal for this implementation.

The type of qubits used in this hardware is also flexibly defined, based on the configuration and number of charges within each double-dot site. It is shown here that this architecture can facilitate a co-existing combination of single-electron spin qubits and two-electron Singlet-T$_0$ Triplet qubits. A similar micromagnet configuration as the one discussed above could also be utilised for an all-electrical control implementation with both data and syndrome qubits defined in the singlet-triplet basis [76]. However, it is noted that approaches involving micromagnets can constitute a deviation from the materials used in the CMOS industry. Without the integrated micromagnet array, all-electrical control can still be achieved in silicon via several implementations. Single-hole spins
with EDSR control [77] leverage higher spin-orbit couplings compared to electrons and singlet-triplet qubits can rely on the naturally present spin-orbit coupling for single qubit rotations [49, 63]. Other all-electrical qubit species involve a (2,1) electron occupancy for the hybrid qubit implementation [78] and (1,0) occupancy for qubits defined in the charge basis [79]. Note that for each of these qubit implementations listed above, tailored control schemes implementing the achievable gate-sets for these qubit varieties must be devised and are considered out of the current scope of this study.

A unit cell approach to constructing scalable quantum information processors benefits from a drastic reduction in input overheads due to high levels of parallelisation between each cell. These hardware-based unit cells can also strongly compliment the tile-like nature of many error correction codes applied to 2D lattices of qubits. In order to successfully carry out this goal, it is necessary to tailor the design and execution towards the use of global signal control strategies such as noise-robust pulses and parallelisation schemes. From the hardware perspective, this also requires the integration of robustness against inter-cell device variations. For any scaled qubit implementation, the variation in qubit control parameters must be overcome. In the case of single electron spin qubits, utilising a 3D cavity as a control peripheral [60] in which the silicon chip is embedded allows for many qubit to be addressed across a large spatial range. However, contemporary results in planar MOS devices show the expected distribution in the electron g-factor [61] far exceeds the range available through Stark-shift tunability [23, 47, 62]. Thus, the concept of tuning via stark shifts must be augmented when operating at appreciable magnetic fields for global operations to be applied to the spin ensemble. Here, the solution presented involves the use of amplitude modulation for the production of discrete side-bands, with the Stark-shift providing individual g-factor tuning towards the nearest band. This approach is subject to a trade-off between the separation between the side-bands given a certain tunable range in g-factor, and the cross-talk between side-bands observed at small separations. As shown here, the same engineered pulses which increase robustness against small tuning deviations in the g-factor can also result in reduced cross-talk between side-bands compared to equivalent square-pulse implementations. With the added design element of intentionally reducing cross-talk between side-bands within the optimisation process, this trade-off between cross-talk and Stark-shift could be further improved. The signals executing the CZ operation can also be made compatible with global control operations through the electrical tuning of the exchange energy between features in the unit cell. Tuning the Stark shift will result in alterations to the $\varepsilon_{DA}\times M$ terms in Eq. (1), however by tuning of the potential on the barrier gates situated between the Dots and the Mediators in Fig. 2b) can compensate via directly tuning the $t_{DA}^2/\varepsilon_{DA}$ ratio, ensuring uniformity in $J_{DA}$ across all sites. The magnitude of $J_{DA}$ can then be modulated through signal $V_M$ applied to the Mediator accumulation gate, which has a linear relationship to both $\varepsilon_{DM}$ and $\varepsilon_{AM}$, resulting in $J_{DA} \propto V_M^2$.

For the global control solutions presented here, the surface code cycle is executed within $\sim 46$ μs ($5 \times \tau_H + 4 \times \tau_{CZ}$), assuming near-negligible electron shuttling times [57]. This is well below the state-of-the-art single-spin coherence time of $T_2^B \approx 9.4$ ms [36] as derived from a Randomized Benchmarking experiment utilising GRAPE pulses. The collective ancilla qubit measurement and initialisation time for this protocol is 12-28 μs depending on the implementation. Current measurements in silicon nanowires have lead to the determination of a PSB signal with >99% fidelity within 5.6 μs [80], leaving approximately a 6-22 μs budget for $|S\rangle$-state initialisation via mediator/reservoirs in the first instance. This time budget can also be extended over multiple code-cycles if necessary, through adopting plaquette sequencing protocols discussed in Ref. [29].

Focusing on the mature CMOS industry for the development of quantum processors has the core benefit of being able to draw upon many different advancements and techniques for information processing and storage [7]. A similar approach for addressing device variation includes embedding a quantum machine into a DRAM-style circuit [9], where the 6T3C/dot cell stores a pre-tuned voltage supplied from a variable source on a capacitor near each quantum dot, and refreshed over a cyclic period. For this approach, the hold-capacitor must be large enough for a sufficiently stable voltage (and thus resonant frequency via the Stark shift in the g-factor) for high fidelity qubit operations. Conversely, this capacitive element must also be small enough not to dominate the integrated dispersive readout signals [81]. In contrast, the method presented here proposes the specific integration of non-volatile memory elements for the storage of these pre-tuned voltage settings. These voltage references are continually applied by the non-volatile elements and are therefore not subject to the same limitations set by capacitive decay constants or cycle-to-cycle variations, but will still be limited by Johnson noise generated by the voltage reference elements in a similar way. Both approaches, however, require a potentially high set-up cost represented by a pre-computation trimming phase which identifies the correct operating conditions for each qubit element, however an advantage for the implementation presented here is that this tuning circuitry has the option to become dormant during computation phases due to the non-volatility of the integrated memory elements, potentially reducing the latent power consumption of the device.

With the addition of trimming internal to the hardware unit cell, the number of inputs required to set the state of the quantum machine can be drastically reduced through the interconnection of cells. This results in a hardware in which the number of inputs scales with the complexity of the unit cell, rather than the number of unit cells required to produce the quantum machine [26], ensur-
ing the extensibility of the qubit platform. The physical layout of the CMOS elements in the FEOL, and the routing between the elements at the quantum-classical interface, is considered to be out of scope for this initial work, however for the solution presented in § V, 48 elements are required per unit cell to connect 16 structures which require trimming (the reservoir accumulation gate, and barriers between the mediators and reservoir are discounted here, as these do not require precise tuning to function). As the area between silicon plateaus is \( \sim (8 \times p)^2 \) for the direct routing solution presented in Fig. 2, where \( p \) is the BEOL routing pitch, this affords an area budget of \( \sim 1.3p^2 \) per control element before the size of these elements impacts the length of the mediator dots which are \( \sim 5 \times p \) in this example. A potential alternative method for spin transfer would be to replace the mediator with a spin-shuttling chain of quantum dots, which has been studied elsewhere [53], and has different trade-offs regarding increased numbers of electrodes and control signals.

While the extension of this architecture towards lattice surgery methods is also considered out of the scope for a study of the individual hardware cell, it is noted that a deviation from globally applied electrical control signals towards grouping regions of the surface into distinct areas, perhaps governed by separate DACs, can facilitate lattice splitting and merging required for lattice surgery [82]. For example, inactivity of CZ mediator signals along a selected row/column results in dormant regions in the surface structure, producing a split between two distinct regions. Further, it is also feasible to have intermittently placed, dedicated control circuitry offsetting entire regions of quantum unit cells in the FEOL, as the surface code has been shown to be robust against both time-resolved, and/or spatial interruptions defects [83]. The exact geometric topology and layout of the quantum VS classical regions in the expanded FEOL is considered to be beyond the scope of the unit cell as studied here.

CONCLUSION

Defining a hardware unit cell which is complimentary to a specific stabiliser code cycle can lead to a highly parallelised approach to the execution of large scale quantum information processing. Here, a case study is presented which utilises a hybrid between two prevalent silicon MOS technologies, combining the advantages of current state-of-the-art solid-state quantum hardware approaches with memory storage techniques. The choice of design to include integrated mediator quantum dots makes the stored quantum information additionally robust against leakage error types which cannot be protected against through standard quantum error detection protocols. The adapted code-cycle presented here allows for the implementation of globally applied single-qubit rotations across the entire ensemble of qubit resonant frequencies, as well as selectively applied two-qubit CZ operations from a global signal source. The inclusion of non-volatile memory elements within the hardware unit cell also reduces the signal overheads to expand with the unit cell size rather than with the number of cells. The result is a complete unit cell approach to constructing a robust quantum information processing machine of arbitrary scale in silicon.

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AUTHOR INFORMATION

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[1] B. M. Terhal, “Quantum error correction for quantum memories,” Reviews of Modern Physics 87, 307 (2015).
[2] J. O’Gorman and E. T. Campbell, “Quantum computation with realistic magic-state factories,” Physical Review A 95, 032333 (2017).
[3] L. Hutin, B. Bertrand, Y.-M. Niquet, J.-M. Hartmann, M. Sanquer, S. De Franceschi, T. Meunier, and M. Vinet, “Soi mos technology for spin qubits,” ECS Transactions 93, 35 (2019).
[4] R. Li, N. I. D. Stuyck, S. Kubicek, J. Jussot, B. T. Chan, F. A. Mohiyaddin, A. Elsayed, M. Shehata, G. Simion, C. Godfrin, Y. Canvel, T. Ivanov, L. Goux, B. Govesan, and I. P. Radu, “A flexible 300 nm integrated si mos platform for electron-and hole-spin qubits exploration,” (IEEE, 2020) pp. 38.3.1–38.3.4.
[5] A. M. J. Zwerver, T. Krähenmann, T. F. Watson, L. Lampert, H. C. George, R. Pillarsetty, S. A. Bojariski, P. Amin, S. V. Amitonov, J. M. Boter, R. Caudillo, D. Correa-Serrano, J. P. Dehollain, G. Droulers, E. M. Henry, R. Kotlyar, M. Lodari, F. Luthi, D. J. Michalak, B. K. Mueller, S. Neyens, J. Roberts, N. Samkharadze, G. Zheng, G. Zietz, O. K. Scappucci, M. Veldhorst, L. M. K. Vandersypen, and J. S. Clarke, “Qubits made by advanced semiconductor manufacturing;” Nature Electronics 5, 184–190 (2022).
[6] L. M. K. Vandersypen, H. Bluhm, J. S. Clarke, A. S. Dzurak, R. Ishihara, A. Morello, D. J. Reilly, L. R. Schreiber, and M. Veldhorst, “Interfacing spin qubits in quantum dots and donors—hot, dense, and coherent,” npj Quantum Information 3, 1–10 (2017).
Applications in an array of CMOS quantum dots, Physical Review Letters 110, 011006 (2012).

J. Duan, A. M. Fogarty, J. Williams, L. Hutin, M. Vinet, and J. J. L. Morton, “Remote capacitive sensing in two-dimensional quantum-dot arrays,” Nano Letters 20, 7123–7128 (2020).

W. Gilbert, A. Saraiva, W. H. Lim, C. H. Yang, A. Laucht, B. Bertrand, N. Rambal, L. Hutin, C. C. Escott, M. Vinet, and A. S. Dzurak, “Single-electron operation of a silicon-CMOS $2 \times 2$ quantum dot array with integrated charge sensing,” Nano Letters 20, 7882–7888 (2020).

M. Veldhorst, J. C. C. Hwang, C. H. Yang, A. W. Leenstra, B. de Ronde, J. P. Dehollain, J. T. Muhonen, F. E. Hudson, K. M. Itoh, A. Morello, and A. S. Dzurak, “An addressable quantum dot qubit with fault-tolerant control-fidelity,” Nature nanotechnology 9, 981–985 (2014).

M. Veldhorst, C. H. Yang, J. C. C. Hwang, W. Huang, J. P. Dehollain, J. T. Muhonen, S. Simmons, A. Laucht, F. E. Hudson, K. M. Itoh, A. Morello, and A. S. Dzurak, “A two-qubit logic gate in silicon,” Nature 526, 410–414 (2015).

D. J. Reilly, “Engineering the quantum-classical interface of solid-state qubits,” npj Quantum Inf. 1, 150111 (2015).

D. J. Reilly, “Challenges in scaling-up the control interface of a quantum computer,” (IEEE, 2019) pp. 31.7.1–31.7.6.

D. P. Franke, J. S. Clarke, L. M. K. Vandersypen, and M. Veldhorst, “Rent’s rule and extensibility in quantum computing,” Microprocessors and Microsystems 67, 1–7 (2019).

A. G. Fowler, M. Mariantoni, J. M. Martinis, and A. N. Cleland, “Surface codes: Towards practical large-scale quantum computation,” Physical Review A 86, 032324 (2012).

A. Corna, L. Bourdet, R. Maurand, A. Crippa, D. Kotekar-Patil, H. Bohuslavskiy, R. Laviéville, L. Hutin, S. Barraud, X. Jehl, M. Vinet, S. De Franceschi, Y.-M. Niquet, and M. Sanquer, “Electrically driven electron spin resonance mediated by spin-valley-orbit coupling in a silicon quantum dot,” npj quantum information 4, 1–7 (2018).

Z. Cai, M. A. Fogarty, S. Schaal, S. Patomäki, S. C. Benjamin, and J. J. L. Morton, “A silicon surface code architecture resilient against leakage errors,” Quantum 3, 212 (2019).

V. Srinivas, H. Xu, and J. M. Taylor, “Tunable spin-qubit coupling mediated by a multielectron quantum dot,” Physical review letters 114, 226803 (2015).

F. K. Malinowski, F. Martins, T. B. Smith, S. D. Bartlett, A. C. Doherty, P. D. Nissen, S. Fallahi, G. C. Gardner, M. J. Manfra, C. M. Marcus, and F. Kuemmeth, “Fast spin exchange across a multielectron mediator,” Nature communications 10, 1–6 (2019).

S. Rochette, M. Rudolph, A.-M. Roy, M. J. Curry, G. Ten Eyck, R. P. Mänginell, J. R. Wendt, T. Phym, S. M. Carr, D. R. Ward, M. P. Lilly, M. S. Carroll, and M. Pioro-Ladrière, “Quantum dots with split enhancement gate tunnel barrier control,” Applied Physics Letters 114, 083101 (2019).
across a one-dimensional array of silicon quantum dots,” Nature communications 10, 1–6 (2019).
[59] A. Rossi, T. Tanttu, K. Y. Tan, I. Isakka, R. Zhao, K. W. Chan, G. C. Tettamanzi, S. Rogge, Andrew S. Dzurak, and M. Möttönen, “An accurate single-electron pump based on a highly tunable silicon quantum dot,” Nano letters 14, 3405–3411 (2014).
[60] E. Vahapoglu, J. P. Slack-Smith, R. C. C. Leon, W. H. Lim, F. E. Hudson, T. Day, T. Tanttu, C. H. Yang, A. Laucht, A. S. Dzurak, and J. J. Pla, “Single-electron spin resonance in a nanoelectronic device using a global field,” Science Advances 7, eaabg158 (2021).
[61] R. Ferdous, K. W. Chan, M. Veldhorst, J. C. C. Hwang, C. H. Yang, H. Sahasrabudhe, G. Klimeck, A. Morello, A. S. Dzurak, and R. Rahman, “Interface-induced spin-orbit interaction in silicon quantum dots and prospects for scalability,” Physical Review B 97, 241401 (2018).
[62] J. C. C. Hwang, C. H. Yang, M. Veldhorst, N. Hendrickx, M. A. Fogarty, W. Huang, F. E. Hudson, A. Morello, and A. S. Dzurak, “Impact of g-factors and valleys on spin qubits in a silicon double quantum dot,” Physical Review B 96, 045302 (2017).
[63] R. M. Jock, N. T. Jacobson, P. Harvey-collard, A. M. Mounce, V. Srinivasa, D. R. Ward, J. Anderson, R. Manginell, J. R. Wendt, M. Rudolph, T. Plumy, J. K. Gamble, A. D. Baczewski, W. M. Witzel, and M. S. Carroll, “A silicon metal-oxide-semiconductor electron spin-orbit qubit,” Nature communications 9, 1–8 (2018).
[64] L. M. K. Vandersypen and I. L. Chuang, “Nmr techniques for quantum control and computation,” Reviews of modern physics 76, 1037 (2005).
[65] N. Khanjea, T. Reiss, C. Kehlet, T. Schulte-Herbrüggen, and S. J. Glaser, “Optimal control of coupled spin dynamics: design of nmr pulse sequences by gradient ascent algorithms,” Journal of magnetic resonance 172, 296–305 (2005).
[66] P. De Fouquieres, S. G. Schirmer, S. J. Glaser, and I. Kuprov, “Second order gradient ascent pulse engineering,” Journal of Magnetic Resonance 212, 412–417 (2011).
[67] T. J. Green, J. Sastrawan, H. Uys, and M. J. Biercuk, “Arbitrary quantum control of qubits in the presence of universal noise,” New Journal of Physics 15, 095004 (2013).
[68] K. W. Chan, W. Huang, C. H. Yang, J. C. C. Hwang, B. Hensen, T. Tanttu, F. E. Hudson, K. M. Itoh, A. Laucht, A. Morello, and A. S. Dzurak, “Assessment of a silicon quantum dot spin qubit environment via noise spectroscopy,” Physical Review Applied 10, 044017 (2018).
[69] H. Ball, M. J. Biercuk, A. R. R. Carvalho, J. Chen, M. Hush, L. A. De Castro, L. Li, P. J. Liebermann, H. J. Slattery, C. Edmunds, V. Frey, C. Hempel, and A. Milne, “Software tools for quantum control: Improving quantum computer performance through noise and error suppression,” Quantum Science and Technology 6, 044011 (2021).
[70] T. Meunier, V. E. Calado, and L. M. K. Vandersypen, “Efficient controlled-phase gate for single-spin qubits in quantum dots,” Physical Review B 83, 121403 (2011).
[71] J. Hasler, N. Dick, K. Das, B. Deguans, A. Moini, and D. Reilly, “Cryogenic floating-gate cmos circuits for quantum control,” IEEE Transactions on Quantum Engineering (2021).
SUPPLEMENTARY FIGURES

FIG. S1. **Integration of unit cells.** The complete tiling of the unit cell FEOL combined with staggered layering of BEOL routing layers is shown. This solution illustrates direct connection of cells, however the space between cells amounts to $\sim (5 \times p)^2$, where $p$ represents the routing pitch, and could be utilised for the layout of hardware in the FEOL such as elements in § V. A solution with integrated supporting hardware would require an alternative routing scheme compared to the one depicted here.

FIG. S2. **Projections of the GRAPE pulse.** a) Oblique view on the Bloch sphere showing the time evolution of the Hadamard pulse optimised through the GRAPE method (blue), with the initial state vector $|\psi\rangle = |\downarrow\rangle$ (reproduced from the main text). The spin trajectory is made clearer through the additional projections of this pulse onto a plane normal to the b) y-axis, c) x-axis and d) z-axis. The Hadamard gate executed by square pulses is also illustrated (red) with a small detuning offset added to accentuate the component of rotation around the x-axis.
FIG. S3. **Amplitude Modulation cross-talk** Fidelity surface for the Amplitude Modulation method described in the main text and Supplementary Note S. S2. Each band is superimposed with the GRAPE solution for the Hadamard as described in the main text. Here N=10 side-bands are shown for increasing side-band separation $\omega_{AM}$.

FIG. S4. **Amplitude Modulation cross-talk** Comparison of the Hadamard gate as executed via a set of square pulses (red squares) against the GRAPE solution (blue circles) for increasing number of sidebands N under the Amplitude Modulation scheme discussed in the main text. It is seen that the degree of cross-talk between sidebands is much higher for the square pulse solution compared to the GRAPE, allowing the GRAPE pulses to be spaced much closer together, catering for a smaller range in the stark-shift of the electron $g$-factor. It is noted that the lowest frequency band for the GRAPE solution has the worst performance, compared to the outermost bands for the square solution. This is attributed to the asymmetry of the GRAPE pulse trace as seen in Fig. 3b in the main text.

**SUPPLEMENTARY NOTES**

S1. **Time-Steps for the Surface Code**

A breakdown of the individual time steps within the surface code cycle is as follows:

1. Initialisation of the $X$ ancilla as a singlet $|S\rangle$. Data qubits located in D1$_A$ and D2$_A$ dots are idle. This time step is also coincident with the measurement of the $Z$ ancilla from the previous cycle (grey in Fig. 2a).

2. Hadamard gates applied to all active spin qubits (D1$_A$,D2$_A$ and individual elements of $X$) coincident with initialisation of the $Z$ ancilla as a singlet $|S\rangle$.

3. Concurrently applied CZ operations, internal to the hardware unit cell, between each element of the $X$ ancilla and D1$_A$ or D2$_A$. These CZ operations are applied via mediator quantum dots [29, 31].

4. Hadamard gate globally applied to all individual spins.

5. Shuttling of the data qubit form within dot location $A$ to $B$. This constitutes a charge shuttling from one side of a nanowire to another.
6. Concurrently applied CZ operations between each element of the Z ancilla and D1 or D2, internal to the hardware unit cell.

7. Hadamard gate applied to all spins. For the X ancilla, these Hadamard operations cancel with the operations form time step 4.

8. Concurrently applied CZ operations between each element of the X ancilla and D1′ or D2′. CZ gates are external to the hardware unit cell, shown as grey in Fig. 2a).

9. Hadamard gate applied to all spin qubits.

10. Shuttling of the data qubit form within dot location B to A.

11. Concurrently applied CZ operations between each element of the Z ancilla and D1′ or D2′. Gates are external to the hardware unit cell.

12. Hadamard gate applied to all active spin qubits coincident with the measurement of the X ancilla. The unassigned Hadamard gate applied to D1A and D2A effectively swaps Z and X ancillas for the next cycle unless a global Hadamard is applied in step 1 of the next cycle.

S2. Amplitude Modulation Scheme

A modulation scheme which can be utilised to increase the number of resonant peaks output by the cavity from a single peak, to N peaks centred at ω0, is given by:

\[ I_N(t) = A_{AM}(\omega_{AM}, N, t) \cdot I_0(t) \]

\[ Q_N(t) = A_{AM}(\omega_{AM}, N, t) \cdot Q_0(t) \]

\[ A_{AM}(\omega_{AM}, N, t) = \begin{cases} 
\sum_{n=1}^{(N-1)/2}[2 \cos \left( \frac{n\omega_{AM}}{2} - n\phi \right)] + 1, & \text{odd } n \\
\sum_{n=1}^{N/2}[2 \cos \left( \frac{(2n-1)\omega_{AM}}{4} - n\phi \right)], & \text{even } n 
\end{cases} \]

\[ \phi = \frac{\omega_{AM} \tau}{2}. \]

(S1)

Here, \( A_{AM} \) is the modulation envelope which results in the replication of the pulse defined by \( I_0(t) \) and \( Q_0(t) \) at frequency detunings separated by \( \omega_{AM} \). For each sideband, a phase correction term \( \phi_f \) is included, which is dependent upon the detuning frequency and pulse duration \( \tau \).

S3. Resistive Trimmer Feasibility

The trimmer configuration in Fig. 4a) of the main text works on the ratio \( R_D : R_{T,ch} \), the system has substantially more tolerance to variations in devices due to fabrication in both the trimming circuitry and quantum dots, as the value of \( R_{T,ch} \) is quasi-continuous [84]. Regarding the necessary operating range for \( V_{QD} \) compared to \( V_{DD} \), and thus the \( R_{T,ch} : R_D \) ratio, by setting \( V_{DD} \) over the nominal value of the second electron \( V_{2e} \) for all quantum dots, when \( R_{T,ch} \ll R_D, V_{QD} \simeq V_{DD} \). Conversely, as the addition voltage \( V_{1e} \) for the first electron on the dot is much larger than the potential equivalent of the addition energy (i.e. \( V_{2e} - V_{1e} \)), thus for \( V_{DD} \simeq V_{2e} \), achieving \( R_{T,ch} \simeq R_D \) results in the condition where \( V_{QD} \simeq V_{DD}/2 < V_{1e} \). Therefore, \( V_{QD} \) can be tuned over the entire voltage range where the dot holds exactly one electron. The key limitation for the operation range of this circuit is the deep sub-threshold (maximum) channel resistance, which is primarily set by the device dimensions.