Non-volatile Complementary Resistive Switch-based Content Addressable Memory

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Abstract — This paper presents a novel resistive-only Binary and Ternary Content Addressable Memory (B/TCAM) cell that consists of two Complementary Resistive Switches (CRSs). The operation of such a cell relies on a logic$\rightarrow$ON state transition that enables this novel CRS application.

I. INTRODUCTION

Lim et al.\cite{1} introduced a new paradigm by exploiting two serially connected non-volatile resistive memory devices (memristors\cite{2}) with opposite polarities. The structure uses a High Resistance State (HRS) and a Low Resistance State (LRS) to encode either logic ‘0’ or logic ‘1’. Consequently, the overall resistance of such device is always around HRS, resulting in significant reduction in the parasitic current paths through neighbouring devices, known as the sneak-paths currents. This device is referred to as a Complementary Resistive Switch (CRS). Fig. 1 summarizes the CRS functionality. If \( p \) and \( q \) indicate resistances of the memristors \( A \) and \( B \), respectively, four different states can be observed. For example, \( p/q \leftarrow L/H \) indicates LRS for \( p \) (memristor \( A \)) and HRS for \( q \) (memristor \( B \)), which is selected as a logic ‘1’. Note that the \( H/H \) state only occurs once in a fresh device. Transitions between the other three states depend on the potential difference across the device terminals. These transitions can be identified by two SET and two RESET thresholds. Absolute values of these thresholds are approximately similar\cite{1, 3}.

Two transitions are possible: logic$\rightarrow$logic and logic$\rightarrow$ON. The first transition indicates a change from \( L/H \) (‘1’) to \( H/L \) (‘0’) or vice versa. This transition needs a high applied voltage \( > V_{\text{th,RESET}} \) that results in a current spike. While a logic$\rightarrow$ON transition requires a voltage that lies between the SET and the RESET thresholds. These transitions conditionally occur depending on the device initial state and the polarity of applied voltage. This condition can be defined as a new fundamental logic operation, known as the ‘material implication’, IMP,\cite{4, 5, 6}. This logic operation results in change in \( q \) depending on the state of \( p \) that is shown as \( p \) IMP \( q \). ‘\( p \) implies \( q \)’ or ‘if \( p \) then \( q \)’. Rosezin et al.\cite{7} introduced crossbar logic via material implication that we call logic$\rightarrow$logic implication. While here we introduce and use a logic$\rightarrow$ON implication for CRS devices.

A logic$\rightarrow$ON transition occur if \( V_{\text{th,SET}} < V(I_{A}) \)-\( V(I_{B}) < V_{\text{th,RESET}} \), and \( p \leftarrow L \) \& \( q \leftarrow H \) (logic ‘1’). Under these conditions state of \( q \) changes to \( L \), which shows that \( p \) IMP \( q \). In this fashion, the device operation can be considered as a Mealy finite state machine whose output value(s) are determined both by its current state and by inputs. Note that, here \( p \) and \( q \) are resistance states, whereas in\cite{7} they are input signals. In this situation, \( p \leftarrow L \) \& \( q \leftarrow L \), a significantly large current can be driven through the device compare to a logic state. The logic$\rightarrow$ON implication is the basic operation to design the CRS-based CAM cell.

Fig. 1. CRS device structure and logical definition of each combination.

Fig. 2 illustrates a behaviour similar to a CRS device using two formed memristors. This measurement highlights that two bipolar memristors connected in series with opposite polarities behave as a CRS device. A fully integrated CRS \( I-V \) characteristics will be more symmetrical. The asymmetry of the \( I-V \) curve is mainly due to: (i) using two different memristors instead of a single CRS device, (ii) different contact sizes of the two memristors, (iii) and possibly fluctuations that affect memristive behaviour during the initial irreversible electroforming process for the memristors. The structure is like a memistor (note the missing ‘r’) device\cite{8}. A possible fabrication technique of a three-terminal resistive switch (memistor) is introduced in\cite{9}.
The functionality of a CRS device is summarised in Table I, where \( R' \) shows the next resistance state, \( R \) illustrates the initial resistance state, and output is a current pulse or spike. After applying a positive or negative bias, depending on the polarity of memristors, the device switches to either the “0” or “1” state. In Fig. 2, the dashed Gray lines are threshold voltages for SET, \( V_{th,S1} \) and \( V_{th,S2} \), and RESET, \( V_{th,R1} \) and \( V_{th,R2} \). In an ideal case, \( V_{th,SET} = V_{th,S1} = |V_{th,S2}| \) and \( V_{th,RESET} = V_{th,R1} = |V_{th,R2}| \). A successful READ operation occurs if \( V_{th,SET} < V_{READ} < V_{th,RESET} \). For a successful WRITE, \( V_{th,RESET} < V_{WRITE} \). Consequently, every voltage below \( V_{th,SET} \) should not contribute any change in the device state.

| State     | \( \Delta V \) | \( R' \)   | Output   |
|-----------|----------------|-----------|----------|
| High (“1”) | \( V_{th,S1} < \Delta V < V_{th,R1} \) | Low (ON) | pulse    |
| High (“1”) | \( V_{th,R1} < \Delta V < V_{th,S2} \) | High (“0”) | spike    |
| High (“0”) | \( \Delta V < V_{th,R2} \) | Low (ON) | pulse    |
| Low (ON)   | \( V_{th,R1} < \Delta V < V_{th,S2} \) | High (“0”) | –        |
| Low (ON)   | \( \Delta V < V_{th,R2} \) | High (“1”) | –        |

There are numerous applications for CRS-based B/TCAM, including pattern matching applications in real-time network intrusion detection, network packet routing, DNA sequencing [10]. Inclusion of CRS devices within a three dimensional hybrid CMOS/nanodevice architecture enables improvements in throughput, density, and power performance relative to state-of-the-art designs [10], [11].

II. PROPOSED CRS-BASED CAM CELL

The proposed structure uses the in-situ computing of memristor and CRS devices, as described in [5]. Here, however, it is compatible with the four-dimensional CMOL (CMOS MOlecular scale devices) architecture that is described in [12] and as its unique feature, it contains CRS devices that is stacked on top of the CMOS layer(s). Fig. 3 summarises the idea. The grey and white modules in Fig. 3(a) represent the CMOS domain and the nano domain implementations, respectively. The red (rectangular) and blue (circle) dots correspond to via connections from the CMOS domain to the nano domain. The implementation is compatible with the CMOL architecture using a Field Programmable Gate Array (FPGA) type structure [12]. The trade-off analysis between other methods in implementing the interface between the CMOS and the nano domain is beyond the scope of this letter. Each cell represents a CAM cell that is entirely implemented in the nano domain. Fig. 3(b) illustrates the CAM cell structure that works for binary CAM and a more flexible type, ternary CAM, applications. For simplicity, the dot colours are chosen to be identical with the via colours in [12]. It has to be stated that connecting the middle electrode (the black line in the CRS symbol) is not allowed because it, firstly, creates new sneak-path currents and, secondly, affects the expected functionality of CRS devices.
Fig. 3 (c) demonstrates the cell functionality. Possible combinations are shown in Fig. 3 (c)-(i) to (v). If the stored data (D) in the complementary cell (consisting of D and D) is “1” and it is matched with the complementary select lines (SL and SL) during the evaluation phase (active En), no path is between the pre-charged ML and SLs. Likewise, if D = SL = “0”, ML remains charged and D = SL vectors all the elements must be matched). The only possibility to discharge ML is the in situation that has been defined as logic→ON implication. This situation can only happen either when D = “1” and SL = “0” or D = “0” and SL = “1”. This path is shown with the dashed red arrows and the corresponding ON state (via) between the nano and CMOS domain is also highlighted. Either of the combinations indicates a mismatched situation a voltage drop occurs on the corresponding ML. Details of the crossbar design and applied voltages are described in [3].

The proposed cell can handle TCAM operation. If a protocol for stored “don’t care” (X) bits can be approved as applying a high voltage (“1”) to the both select lines when bypassing the stored bit is desirable, the logic→ON conditions will never be satisfied and the device keeps its stored data.

A 64 × 8 CAM is simulated and its function is confirmed. In this implementation 16 select lines and 64 match lines are required. Fig. 4 illustrates simulation inputs and results. The stored memory pattern and the search stream are randomly generated and shown in Fig. 4 (a) and (b). For simplicity, in the presentation, we intentionally addressed only one (the 1st) match line, therefore, the expectation is to see ML1 remains unchanged while all other match lines are dropped. The voltage drop must be detectable by the sense amplifier (SA) chain [3]. Nano-wire parasitic resistors are also taken into account.

Figs. 3 (c) and (e) illustrate outputs of matched (solid line) and mismatched (dashed lines) MLs and the evaluation, En, signal (dashed line with circle symbols). The only match line that remains unchanged after activating the enable is the red one. The voltage drop right after activating En occurs due to the fact that each ML acts as the middle node of a voltage divider with an effective pull-up and pull-down resistors. Therefore, another advantage of CRS-based CAM is that the pull-down resistors are initially $R_{HRS}$, whereas a memristor-based array is highly pattern dependent. Fig. 4 (d) demonstrates resistances of two CRS devices, with stored logic “0” or “1” (dashed line) and ON states (solid line). In the mismatched cells a logic→ON transition is observed. The ON resistance of a CRS device is equivalent to $2R_{LRS}$. The outputs then feed into an array of SAs through the red via connections. The design of these SAs requires a detail analysis of the array output for finding optimum values for crossbar memory parameters [3].

Fig. 3. The CAM system, (a), and proposed cell (b). Design is compatible with CMOL architecture. The blue and red via contacts between the CMOS FPGA type array and CRS-based array highlights this compatibility. The logical operation of the B/TCAM cell is shown in (c). ML = C and d demonstrate charged and discharged ML, respectively. Further information regarding the density and the connections (via) between the nano and CMOS domain can be found in [10].

![Fig. 3](image_url)

Fig. 4. Simulation results using Cadence Spectre. The stored and input patterns are shown in (a) and (b), respectively. (c) demonstrates matched and mismatched MLs and the evaluation, En, signal. The yellow region highlights a pre-charge step. (e) demonstrates a more clear picture of (c). Approximately, 80 μs for the worst-case ML to reach the minimum detectable $\Delta V$. (d) illustrates two resistor samples (logic -either “0” or “1”- and ON states).

![Fig. 4](image_url)
pursued. Although, from the fact that comparing today’s mature or advanced technologies with the emerging technologies is not quite fair, but a switching speed and energy analysis of fabricated devices in [3], [4] illustrates that applying higher voltage pulses exponentially increases the switching speed and it reduces overall energy dissipation. It is also observed that more than 80% of the total power is consumed by the nanowires and the device itself consumes 10-100 pJ dynamic energy (30 ns switching time) [4], which is not an outstanding result compared to low-power B/TCAMs. Resistive memories and in particular, CRS devices, demonstrate relatively robust operation, non-volatile memory, high scalability, and promising experimental results for reducing switching time, while maintaining a relatively switching energy, which make them a serious alternative to the conventional CMOS technology [1], [3], [7]. In addition, as the CRS technology matures and the advanced transistor technologies continue to face more challenges, the combination of these two technologies will result in significantly more efficient and denser designs [12].

III. CONCLUSIONS AND FUTURE DIRECTIONS

This paper introduced a CRS-based B/TCAM cell. The proposed cell has been mapped on a CMOL type architecture by introducing via contacts between the CMOS and the nano domains. Relatively robust, low-power, and scalable features of the CRS cell along with the CMOL’s architectural flexibility introduce several advantages for the proposed cell. The cell’s operation relies on the logic→ON state transition that also introduces a novel application of this CRS operation. The CRS-based B/TCAM and the application of the logic→ON transition have potential impact for stimulating pioneering work in CAM applications and CRS-based computing. The projected aim is to design and fabricate a CRS array utilising a non-destructive read-out technique, similar to [13], to enhance overall performance of the memory array and significantly reduce the total number of refreshing cycles. This reduction is an important factor since the endurance requirement in for CRS devices will be relaxed with less refreshing cycles and it may be further relaxed with the increase of memory density.

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