Analytical breakdown voltage model for a partial SOI-LDMOS transistor with a buried oxide step structure

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Abstract
We have developed a simple physics-based two-dimensional analytical off-state breakdown voltage model of a partial buried oxide step structure (PBOSS) silicon-on-insulator laterally diffused metal oxide semiconductor (SOI-LDMOS) transistor. The analytical model includes the expressions of surface potential and electric field distributions in the drift region by solving the 2D Poisson equation. The electric field at the Si–SiO2 surface is modulated by additional electric field peaks developed due to the presence of the PBOSS structure. The uniformly distributed electric field results in improved breakdown voltage. Further, the breakdown voltage is analytically obtained by means of the critical electric field concept, to determine the breakdown characteristics. The model reveals the impact of the critical device design parameters such as thickness and length of the PBOSS structure, doping, and thickness of the drift region on the surface electric field and the breakdown voltage. The proposed model is verified by ATLAS two-dimensional simulations. The analytical model will be useful to design high-voltage SOI-LDMOS transistors for power switching applications.

Keywords Analytical model · Partial SOI-LDMOS · Surface electric field · Electric field modulation

1 Introduction
With the advancements in solid-state technologies, power electronics application is an ever-expanding topic of research and development, [1, 2]. The silicon power devices are useful for mid-range voltage applications ranging from hundreds of watts to several megawatts [3]. Nowadays, the integration of laterally diffused metal oxide semiconductor (LDMOS) power devices into the CMOS platform has high application potential in high-voltage integrated circuit (HVIC) technology, space power systems, data conversion, and electrostatic discharge protection circuits [4–6]. The silicon-on-insulator (SOI)-LDMOS transistor has attracted much attention among the HVIC design community due to its advantages including near-ideal isolation, reduced parasitic active components, and low leakage current [7–10]. Also, the vertical and lateral dielectric isolation prevents the overstress events arising in high-voltage transistors fabricated on SOI substrates [11]. On the other hand, an increase in self-heating, reduction in the breakdown voltage, and hence reduced safe operating area (SOA), are challenging issues [12]. Recently, partial-SOI LDMOS technology [13–15] was reported to overcome the problems observed in conventional SOI-LDMOS transistors. Orouji et al. [16] reported a new PBOSS SOI-LDMOS transistor with a modified step buried oxide structure. It improves the off-state breakdown voltage (\(V_{BR}\)) due to two additional electric field peaks developed in the drift region. An analytical model would be very useful for formulating the design guidelines of advanced semiconductor devices. Moreover, analytical models can provide insight into the physical mechanism and shorten the design time [17, 18]. Several analytical models have been proposed for the surface field distribution of conventional and buried oxide step SOI-LDMOS transistors [19–21]. However, to the best of our knowledge, an analytical model for the PBOSS SOI-LDMOS transistor is still lacking.

In this paper, a two-dimensional analytical model for the PBOSS SOI-LDMOS transistor is presented. The variation in the electric field and potential is modelled by solving the two-dimensional differential equation using the Poisson equation. One-dimensional boundary conditions are
used to solve the Poisson equation. The proposed model is verified with the SILVACO TCAD simulation results for a wide range of device design parameters including the buried oxide step thickness and length of the PBOSS SOI-LDMOS transistor. Also, the model is found to be suitable for the variation in silicon thickness and doping concentration of the drift region for the PBOSS SOI-LDMOS transistor. The investigated structure shows a \( V_{\text{BR}} \) of 170 V, whereas the conventional SOI-LDMOS and the buried oxide step SOI-LDMOS (BOSS-LDMOS) exhibit a \( V_{\text{BR}} \) of 80 and 126 V, respectively. The developed model will have a great impact on the design of the PBOSS SOI-LDMOS transistor to achieve a better trade-off between the different figures of merit (FOMs) for power switching applications.

The paper is organized as follows. In Sect. 2, we present the investigated transistor with dimensions used for device simulation. We also describe the simulation methodologies in this section. Section 3 presents the analytical model formulation. The results are discussed in detail in Sect. 4. The key fabrication steps are presented in Sect. 5, and a summary of the results is outlined in Sect. 6.

2 Investigated device structure and simulation methodology

Figure 1 shows a schematic cross-sectional view of the investigated PBOSS SOI-LDMOS transistor. The device structure used in this investigation is similar to that reported in [16]. A uniformly doped region P-well creates the channel part of the device, with a doping concentration represented by \( N_A \). The drift region is lightly doped, represented by \( N_{Dr} \). A P-layer is used, as shown in Fig. 1, to decrease the thermal effects which are inherent to the SOI-LDMOS transistor. The \( N_{P-layer} \) represents the doping concentration of the P-layer. A step in the buried oxide layer (BOX) is created to enhance the \( V_{\text{BR}} \) by modifying the surface electric field. The thicknesses of the silicon epitaxial layer, the buried oxide, and the step layer are represented by \( t_{Si} \), \( t_{BOX} \), and \( t_{BOSS} \) respectively. The drift region is divided into three regions: region 1, region 2, and region 3. \( L_1 \), \( L_2 \), and \( L_3 \) are the boundaries in the \( x \)-direction for region 1, region 2, and region 3, respectively. The substrate is of P-type and lightly doped. The device parameters of the PBOSS are equivalent to those of the BOSS and conventional SOI-LDMOS transistors. The critical design parameters are given in Table 1.

The investigated devices are simulated by the SILVACO ATLAS 2D device simulator [22]. A well-calibrated device simulation deck is used for the 2D TCAD simulations, as used in our previous works on LDMOS devices [27]. CONMOB, FLDMOB are the mobility-dependent models used for simulation. SRH and Auger recombination models are included to account for carrier generation-recombination. A bandgap narrowing model is invoked for the highly doped regions in silicon. Selberherr’s model is considered for impact ionization according to (1):

\[
a_N = A_N \cdot \exp \left[ -\left( \frac{B_N}{E} \right)^{\beta_n} \right]
\]

(1)

Here, \( E \) is the electric field in the direction of current flow at a particular position in the structure, and the parameters \( A_N \), \( B_N \), and \( \beta_n \) are defined as \( 7.03 \times 10^5 \text{ cm}^{-1} \), \( 1.231 \times 10^6 \text{ V/cm} \), and 1.0, respectively [23]. As the peak electric field is quite sensitive to mesh design, the structure is designed with optimum mesh in the deck.

| Parameters | PBOSS | BOSS | Conventional |
|------------|-------|------|--------------|
| \( L_{Ch} \) | 1 \( \mu \)m | 1 \( \mu \)m | 1 \( \mu \)m |
| \( L_{Dr} \) | 15 \( \mu \)m | 15 \( \mu \)m | 15 \( \mu \)m |
| \( L_1 \) | 5 \( \mu \)m | – | – |
| \( L_2 \) | 10 \( \mu \)m | 7.5 \( \mu \)m | – |
| \( L_3 \) | 15 \( \mu \)m | 15 \( \mu \)m | 15 \( \mu \)m |
| \( t_{ox} \) | 0.05 \( \mu \)m | 0.05 \( \mu \)m | 0.05 \( \mu \)m |
| \( t_{Si} \) | 0.5 \( \mu \)m | 0.5 \( \mu \)m | 0.5 \( \mu \)m |
| \( t_{BOX} \) | 0.5 \( \mu \)m | 0.5 \( \mu \)m | 0.5 \( \mu \)m |
| \( t_{P-layer} \) | 0.5 \( \mu \)m | – | – |
| \( N_{Dr} \) | \( 3.3 \times 10^{16} \text{ cm}^{-3} \) | \( 3.3 \times 10^{16} \text{ cm}^{-3} \) | \( 3.0 \times 10^{16} \text{ cm}^{-3} \) |
| \( N_{P-layer} \) | \( 5 \times 10^{17} \text{ cm}^{-3} \) | – | – |
3 Model formulation

3.1 Potential and electric field expression

Here, it is assumed that the impurity density in the drift region is uniform and that the influence of the charge carriers on the electrostatics of the drift region can be neglected (which requires the Poisson equation and no-transport equation to be solved). Also, assuming that the drift region is under complete depletion for the breakdown condition, the potential function ($\phi$) in regions 1, 2, and 3 are described by the 2D Poisson equation as follows.

$$\frac{\partial^2 \phi_i(x, y)}{\partial x^2} + \frac{\partial^2 \phi_i(x, y)}{\partial y^2} = -\frac{qN_i}{\varepsilon_{Si}}, \quad i = 1, 2, 3 \tag{2}$$

where $q$ is the charge of the electron. Here, $N_i = N_2 = N_3 = N_{Dr}$, $\varepsilon_{Si}$ is the dielectric constant of silicon.

The boundary conditions for the potential and electric field are given as follows:

$$\frac{\partial \phi_i(x, y)}{\partial y} \bigg|_{y = 0} = 0, \quad i = 1, 2, 3 \tag{3}$$

$$\frac{\partial \phi_1(x, y)}{\partial y} \bigg|_{y = t_{Si}} = -\frac{2\phi_1(x, t_{Si})}{t_{sub}} \tag{4}$$

$$\frac{\partial \phi_i(x, y)}{\partial y} \bigg|_{y = t_{Si}} = -\phi_1(x, t_{Si}) - \phi_1(x, t_{Si} + t_{oxi}), \quad i = 2, 3 \tag{5}$$

where, $K = \varepsilon_{Si}/\varepsilon_{ox}$

$$\frac{\partial \phi_1(L_1, y)}{\partial y} \bigg|_{y = 0} = \frac{\partial \phi_2(L_1, y)}{\partial y} \bigg|_{y = 0} \tag{6}$$

$$\phi_1(L_1, y) = \phi_2(L_1, y) = V_1 \tag{7}$$

$$\frac{\partial \phi_2(L_2, y)}{\partial y} \bigg|_{y = t_{Si}} = \frac{\partial \phi_3(L_2, y)}{\partial y} \bigg|_{y = t_{Si}} \tag{8}$$

$$\phi_2(L_2, t_{Si}) = \phi_3(L_2, t_{Si}) = V_2 \tag{9}$$

$$\phi_1(0, 0) = 0, \quad \phi_3(L_3, 0) = V_{DS} \tag{10}$$

At the Si–SiO$_2$ surface, the vertical electric field may be ignored, which results in (3). The electric flux density is continuous across the n-drift region and P-layer. This results in (4). The continuity of the electric flux density at the Si-BOX interface results in (5). Similarly, other boundary conditions (6) to (10) are shown to satisfy Gauss’s law. The solution of two-dimensional Eq. (2) is achieved by the polynomial approach as follows [24]:

$$\phi_i(x, y) = C_{i0}(x, 0) + C_{i1}(x, 0)y + C_{i2}(x, 0)y^2 \tag{11}$$

Substituting the boundary conditions (3)–(5) into (11) leads to a general differential expression for the potential distribution as (12).

$$\frac{\partial^2 \phi_i(x, 0)}{\partial x^2} - \frac{1}{t_i^2} \phi_i(x, 0) = -\frac{qN_i}{\varepsilon_{Si}}, \quad i = 1, 2, 3 \tag{12}$$

$$t_1 = \sqrt{t_{Si}t_{sub} + \frac{r^2}{2}}, \quad i = 1 \tag{13}$$

$$t_{sub} = \frac{1}{2} \left( \sqrt{\left( 1 + \frac{N_{Dr}}{N_{P, \text{layer}}} \right) r_{Si}^2 + \frac{2\varepsilon_{Si}V_{DS}}{qN_{P, \text{layer}}} - t_{Si}^2} \right) \tag{14}$$

$$t_i = \sqrt{\left( \frac{1}{2} r_{Si}^2 + Kt_{Si}t_{oxi} \right)}, \quad i = 2, 3 \tag{15}$$

Solving (12) using (6–10), the potential and electric field distribution are expressed as (16) and (18).

$$\phi_i(x, 0) = p_i + \left[ V_i - p_i \right] \frac{\sinh \left( \frac{x-L_{i-1}}{t_i} \right)}{\sinh \left( \frac{L_i - L_{i-1}}{t_i} \right)} \tag{16}$$

where $p_i = \frac{qN_{Di}r_i^2}{\varepsilon_{Si}}, \quad i = 1, 2, 3.$

When deriving (12) from (2), it can also be shown that

$$\phi_i(x, y) = \left( 1 - \frac{y^2}{2t_i^2} \right) \phi_i(x, 0) \tag{17}$$

The surface electric field is expressed as

$$E_s(x, 0) = \left[ V_i - p_i \right] \frac{\cosh \left( \frac{x-L_{i-1}}{t_i} \right)}{t_i \sinh \left( \frac{L_i - L_{i-1}}{t_i} \right)} - \left[ V_{i-1} - p_i \right] \frac{\cosh \left( \frac{L_i - x}{t_i} \right)}{t_i \sinh \left( \frac{L_{i-1} - x}{t_i} \right)} \tag{18}$$

The expressions of (16) and (18) can be simplified for the BOSS and the conventional SOI-LDMOS transistors using suitable boundary conditions.
The lateral and vertical electric fields at any point can be expressed as (19) and (20), respectively.

\[ E_{lx}(x,y) = \left(1 - \frac{y^2}{t_1^2}\right) E_l(x,0) \]  
(19)

\[ E_{ly}(x,y) = \frac{\phi_l(x,0)}{t_1^2} y \]  
(20)

The surface potential \( V_1, V_2 \) (at point B and point C, respectively) can be solved by the continuity of the electric fields (6) and (8) and expressed as

\[ V_1 = \frac{V_2}{t_2} \frac{1}{\sinh \beta} + \frac{P_2}{t_2} \tanh \frac{a}{2} + \frac{P_1}{t_2} \tanh \frac{b}{2} \]  
(21)

\[ V_{BRA} = t_3 \sinh c \left[ \frac{\frac{t_1}{t_2} + \coth a \coth b}{t_1 \coth b + t_2 \coth a} + \frac{\coth c}{t_3} \right] \]  
(24)

\[ V_{BRB} = t_3 \sinh c \left[ \frac{\frac{t_1}{t_2} + \coth a \coth b}{t_1 \coth b + t_2 \coth a} + \frac{\coth c}{t_3} \right] \]  
(25)

Here, \( a = L_1/t_1, b = (L_2 - L_1)/t_2 \) and \( c = (L_3 - L_2)/t_3 \), respectively.

### 3.2 Breakdown voltage expression

For the PBOSS SOI-LDMOS, additional electrical fields are observed at point B and point C apart from the usual electric field peaks at point A and point D (the pn-junction electric field and the electric field at the nn+ junction, respectively). The expressions for \( V_{BR} \) at points A, B, C, and D are obtained when the peaks of the electric field are equal to the critical electric field \( (E_{crit}) \). The expressions of breakdown voltage are given by (24–29).
The device parameters in Table 1 are used to calculate the critical electric field \( E_{\text{crit}} \) for the PBOSS transistor. The critical electric field is determined by (30) [25],

\[
E_{\text{crit}}^2 = \frac{0.35 \times 10^6}{1 - \frac{1}{3} \log_{10} \left( \frac{N_{\text{Dx}}}{10^{16}} \right)} \frac{V}{cm}
\]

(30)

\[V_{BR,E} = \frac{E_{\text{crit}}^2}{t_{Si}}\]

(28)

\[V_{BR} = \text{Min} \left[ V_{BR,A}, V_{BR,B}, V_{BR,C}, V_{BR,D}, V_{BR,E} \right]\]

(29)

In this paper, the critical electric field \( E_{\text{crit}} \) is determined by (30) [25],

\[V_{BR} = \text{Min} \left[ V_{BR,A}, V_{BR,B}, V_{BR,C}, V_{BR,D}, V_{BR,E} \right]\]

(29)

In this section, the numerical simulation results are compared with the proposed analytical model. The simulation data at the top silicon surface implies the data obtained across cross-section FF' as shown in Fig. 1. Similarly, the simulation results at the bottom silicon interface are considered across cross-section HH' as shown in Fig. 1. The potential and the electric field distributions are shown only for the drift region. Hence, the starting point of the lateral position is the pn-junction, which separates the MOS and drift junction. The device parameters in Table 1 are used to perform the two-dimensional simulation for the PBOSS, BOSS, and conventional SOI-LDMOS transistors. This section is divided into three sub-sections. In the first sub-section, the analytical model for the PBOSS SOI-LDMOS transistor is compared with the BOSS and the conventional SOI-LDMOS transistors. The effect of the BOSS thickness and the length for the PBOSS SOI-LDMOS transistor are studied in sub-section ii. The last sub-section includes the effect of \( t_{Si} \) and \( N_{\text{Dx}} \) for the PBOSS SOI-LDMOS transistor.

Fig. 2 Simulated off-state breakdown characteristics of the conventional, BOSS, and PBOSS SOI-LDMOS transistors
From the simulation studies, it is found that the $V_{BR}$ of the PBOSS SOI-LDMOS transistor is ~170 V, whereas the BOSS and conventional SOI-LDMOS transistors break down at ~126 and ~80 V, respectively as shown in Fig. 2. $V_{BR}$ is measured using the industry-standard constant current (1E-10 A/µm in this paper) measurement method. For the PBOSS SOI-LDMOS transistor, though there is an improvement in $V_{BR}$, the leakage current increases in the off state. This is due to the presence of the additional P-layer which provides a path for the current into the substrate, thereby increasing the leakage current. However, in the Conventional SOI-LDMOS transistor and BOSS SOI-LDMOS transistor the silicon film containing the active devices is thin enough for the junctions to reach through to the buried insulator. The leakage current path is ruled out because there is no current path to the substrate. Figure 3a shows the numerical and analytical profiles of surface potential at cross-section FF' for the investigated transistors at breakdown condition. It changes at the boundary of region 1 and region 2 and the boundary of region 2 and region 3 for the PBOSS SOI-LDMOS transistor. To know the reason behind this improved $V_{BR}$, it is important to study the variation in the electric field both at cross-section FF' and HH' as shown in Fig. 3b and c, respectively. Both the fields are correlated through (19) and (20). For the conventional SOI-LDMOS transistor, the electric field is almost flat at cross-section FF', as shown in Fig. 3b with two usual peaks at the pn-junction (which separates the MOS and drift region) and nn+ junction. The step-like structure in BOX creates an additional electric field peak near the step, as shown in Fig. 3b for the BOSS structure [21]. It is observed that the PBOSS SOI-LDMOS transistor introduces additional electric field peaks apart from the peak at the pn-junction and nn+ junction, as shown in Fig. 3b. The first additional electric field peak is due to the P-layer charges at the region 1 and region 2 boundary. The additional electric field peak is created at the location of carrier inhomogeneities at the silicon surface by redistributing the lateral electric field. The second additional electric field peak is created due to the sudden change in buried oxide step thickness at the region 2 and region 3.

Fig. 3  Variation in the a potential at cross-section FF’, b lateral electric field at cross-section FF, c lateral electric field at cross-section HH’ for the conventional, BOSS, and PBOSS SOI-LDMOS transistors. Here $V_{GS}=0$ V, and $V_{DS}$ is equal to the breakdown voltages of each structure. Solid line: model. Symbol: simulation

Fig. 4  Equipotential contours are shown for the a conventional, b BOSS, and c PBOSS SOI-LDMOS transistors. Here $V_{GS}=0$ V, $V_{DS}$ equals the breakdown voltages of each structure
The applied voltage at the drain end is now shared among all the electric field peaks at breakdown condition. With more uniformity in the surface electric field, the V_{BR} is further improved.

The equipotential contours for the conventional, BOSS, and PBOSS SOI-LDMOS transistors in breakdown condition are shown in Fig. 4a–c, respectively. For the conventional SOI-LDMOS transistor, the equipotential contours are more unevenly spaced, as shown in Fig. 4a. The potential contours are not able to spread into the substrate for the conventional SOI-LDMOS transistor. The equipotential contours are more uniformly distributed for the BOSS SOI-LDMOS transistor than the conventional SOI-LDMOS transistor, as shown in Fig. 4b. It is observed that the equipotential contours are distributed uniformly for the PBOSS SOI-LDMOS transistor, as shown in Fig. 4(c). The potential contours spread to the substrate for the PBOSS SOI-LDMOS transistor. For the PBOSS structure, the P-layer supports a higher electric field, which is originated from the interface between the P-type layer and buried oxide. This leads to a more uniform distribution in the electric field; therefore, the V_{BR} is enhanced significantly.

4.1.1 Effect of the thickness and length of BOSS structure

A part of the applied voltage V_{DS} drops across the buried oxide in the breakdown condition as per (31) [26],

\[
V_{BR} = V_{Si} + V_{BOX} = V_{Si} + E_{F}t_{BOX,eff}
\]  

where V_{Si} and V_{BOX} are the potential across the SOI film and buried oxide. E_{F} and t_{BOX,eff} are the vertical electric field in the BOX and effective buried oxide thickness. As the t_{BOSS} increases, the voltage drop V_{BOX} also increases; hence, the V_{BR} also increases. The surface electric field is increasing with the increase in t_{BOSS} at point C, as shown in Fig. 5a.

![Figure 5](image1.png)

**Fig. 5** Variation in the a lateral electric field at cross-section FF' for different t_{BOSS} (Here V_{GS} = 0 V, V_{DS} equals the breakdown voltage at the corresponding t_{BOSS}) b V_{BR} with t_{BOSS} for the PBOSS SOI-LDMOS transistor. Solid line: model. Symbol: simulation

![Figure 6](image2.png)

**Fig. 6** Variation in the a lateral electric field at cross-section FF' for different L_{2} (Here V_{GS} = 0 V, V_{DS} equals the breakdown voltage at the corresponding L_{2}) b V_{BR} with L_{2} for the PBOSS SOI-LDMOS transistor. Solid line: model. Symbol: simulation
This results in a more uniform distribution in the surface electric field. However, a further increase in t_{BOSS} results in a reduction in V_{BR} as the peak electric field is comparable with the critical electric field and breakdown occurs. The variation in V_{BR} with t_{BOSS} is as shown in Fig. 5b. V_{BR} is increased up 170 V at t_{BOSS} = 1.5 µm. So, there exists an optimum value of t_{BOSS}, where an improved performance in V_{BR} is achieved. As observed in Fig. 5b, V_{BR} is determined by the minimum V_{BR} at point D and point E up to as t_{BOSS} = 1.5 µm. Beyond the optimum t_{BOSS} the drift region will partially deplete when the breakdown occurs and the V_{BR} is determined by V_{BR,A}. Hence, the V_{BR} follows a bell shape curve, as shown in Fig. 5b.

The variation in the surface electric field along the lateral direction is shown for different L_2. It is noted that the L_{BOSS} is measured as L_3-L_2. As L_2 is increased, the length of the BOSS layer L_{BOSS} decreases. Here, L_3 is fixed at 15 µm. At L_{BOSS} = 0 µm, the peak of the surface electric field due to BOSS superimposes on the drain end electric field peak. As L_2 decreases (i.e., L_{BOSS} increases), the electric field peak at point C is noticeable. For L_2 = 11 µm (i.e., L_{BOSS} = 4 µm) the surface electric field distribution is more uniform. There is an optimal value of L_{BOSS} where the V_{BR} is maximum. As the L_{BOSS} increases beyond this optimal value, the peak due to the BOSS layer superimposes with the electric field at the pn-junction, as shown in Fig. 6a. The variation in V_{BR} with L_2 is shown in Fig. 6b. The V_{BR} initially increases with the L_2, and the maximum V_{BR} is found to be 170 V at L_2 = 10 µm i.e. (L_{BOSS} = 5 µm). As L_2 is increased above 12 µm, the V_{BR} falls sharply. It is observed that the V_{BR} follows the value at V_{BR,D} for almost the entire range of L_2. It can be noted that choosing an optimum value of L_2 (which subsequently determines L_{BOSS}) is important for device designers to achieve higher V_{BR}.
4.1.2 Effect of silicon thickness ($t_{Si}$) and doping ($N_{Dr}$)

The effect of silicon film thickness $t_{Si}$ for the PBOSS SOI-LDMOS transistor is shown in Fig. 7. As the $t_{Si}$ increases, the electric field peak is increased at point D to fulfill the RESURF criterion for a given doping concentration of the drift region. It is observed that as the $t_{Si}$ increases, the surface electric field becomes more uniform (as shown in Fig. 7a); hence the area under the electric field is maximum. The $V_{BR}$ initially increases with $t_{Si}$, and it follows the $V_{BR,D}$ up to $t_{Si} = 0.5 \mu m$ (full depletion occurs), as shown in Fig. 7b. A maximum $V_{BR}$ of 170 V is achieved for $t_{Si} = 0.5 \mu m$ and is limited by the vertical breakdown $V_{BR,E}$. As the $t_{Si}$ further increases, the $V_{BR}$ is determined by $V_{BR,A}$ (i.e., the breakdown occurs due to partial depletion).

Figure 8a shows the surface electric field distribution for different $N_{Dr}$. As the $N_{Dr}$ increased from a low doping concentration of $2.0 \times 10^{16}$/cm$^3$ to $3.3 \times 10^{16}$/cm$^3$, the peak of the surface electric field at point D is increased, and full depletion occurs. The maximum $V_{BR}$ is found to be 170 V for $N_{Dr} = 3.3 \times 10^{16}$/cm$^3$. As $N_{Dr}$ increases further, the drift region is partially depleted, and the electric field peak at point A is comparable to the critical electric field. A highly doped drift region acts as an extended drain contact, missing its original role of extended body. The $V_{BR}$ after the optimum $N_{Dr}$ is determined by the $V_{BR,A}$ as shown in Fig. 8b. The model provides a reasonable justification for the bell-shape nature of the $V_{BR}$.

5 Key fabrication process steps

The key fabrication process steps of the PBOSS SOI-LDMOS transistor are shown in Fig. 9. A P-type silicon substrate with different desired doping concentration is used as the starting material. The process begins by masking and separation by implanted oxygen (SIMOX) process 1 and 2 for the buried oxide step structure and BOX structure as shown in Steps 2 and 3, respectively. An ion-implantation process of phosphorous impurity is realized with a corresponding mask to form the n-drift region in Step 4. The heavily doped n+-source/drain, and p+-body dopants are ion-implanted with phosphorous and boron in Steps 5 and 6, respectively. Finally, the gate stack deposition, the ohmic contacts etch, and the electrode formation processes are implemented by using the conventional CMOS processes.

6 Conclusion

We have developed an analytical model of the breakdown field by calculating the variation in the surface potential and electric field for the PBOSS SOI-LDMOS transistor for the first time. The model is formulated by solving the two-dimensional Poisson equation using the polynomial approach. Simple formulae are shown to design and analyze the PBOSS SOI-LDMOS transistor in order to enhance the off-state breakdown voltage. Meanwhile,
there are no fitting parameters used in the model. Using the model, it is possible to predict the optimum device design parameters to achieve maximum breakdown voltage. With the optimum device design parameters, $V_{BR}$ of the PBOSS device is enhanced by $\sim 112\%$ compared with the conventional SOI-LDMOS transistor. The model is also able to provide data for the conventional and BOSS SOI-LDMOS transistors by modifying suitable boundary conditions. The results shown are in fair agreement with the simulated data obtained from TCAD, demonstrating the validity of the technique and simplicity of the model. This study can, therefore, serve as a good analytical tool for the design of high-voltage SOI-LDMOS transistors. It is proposed that apart from physical insight, the lateral surface electric field and potential distributions which are related to current sources (that represent the carrier multiplications) might be useful for the circuit implementation/simulation using LDMOS with PBOSS structures which can be further carried out.

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