Hardware Security in Spin-Based Computing-In-Memory: Analysis, Exploits, and Mitigation Techniques

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Computing-in-memory (CIM) is proposed to alleviate the processor-memory data transfer bottleneck in traditional Von-Neumann architectures, and spintronics-based magnetic memory has demonstrated many facilitation in implementing CIM paradigm. Since hardware security has become one of the major concerns in circuit designs, this paper, for the first time, investigates spin-based computing-in-memory (SpinCIM) from a security perspective. We focus on two fundamental questions: 1) how the new SpinCIM computing paradigm can be exploited to enhance hardware security? 2) what security concerns has this new SpinCIM computing paradigm incurred?

CCS Concepts: • Hardware → Emerging architectures; Non-volatile memory; • Security and privacy → Hardware attacks and countermeasures.

Additional Key Words and Phrases: Computing-in-memory, hardware security, spintronics technology

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1 INTRODUCTION

For traditional Von-Neumann architecture, computation and memory are the two most important units. The computation unit reads data from memory and performs calculations, then stores the results back into memory. Since the late 1990’s, CPU speed has outperformed the speed of memory access, creating the well-known “memory wall” [1]. This becomes even worse in today’s big data era, where data intensive applications need more frequent transfer of larger amount of data between processor and memory. A single memory Read/Write operation consumes two to three orders of magnitude more energy and time than data calculation.

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Computing-in-memory (CIM) is one promising approach to alleviate the memory wall. The basic idea of CIM is to embed computations into memory. The computation could be performed at the same time of memory access, eliminating the time and energy overhead of data movement between processor and memory. In addition, due to the available high bandwidth within memory array, CIM is able to provide massive parallelism, such as the vector operations.

Among the possible CIM implementations, spintronics-based CIM (SpinCIM) has the following advantages. First, spintronics-based magnetic memory has been a promising candidate for the next generation main memory because of its properties such as near-zero leakage, non-volatility, high endurance, and compatibility with the CMOS manufacturing process. In particular, prototype Spin Transfer Torque Magnetic RAM (STT-MRAM) chip demonstrations and commercial MRAM products have been available by companies such as Everspin and TSMC [2][3]. Second, STT-MRAM stores data with magnetic-resistances and accesses data by current-sensing scheme instead of conventional charge based store and access. This enables MRAM to provide inherent computing capabilities with only minor changes to the memory array, making it suitable for CIM implementation.

It is well-documented that security has been previously considered as an afterthought, with performance dominating the design requirements. As a consequence, numerous security vulnerabilities and malicious attacks (such as intentional sensitive data leakages in Meltdown and Spectre [4]) are consistently being discovered. While SpinCIM is newly proposed and still in exploration stage, it gives us the golden opportunity to consider security as a first class requirement at the early design stage. To the best of our knowledge, this paper is the first effort to study SpinCIM from the security perspective. Previously, there are extensive research on applying the emerging spintronic device for security. For example, the stochastic writing features have been used for true random number generation and PUF design [5–7]. Our work is different from these in that we focus on the SpinCIM computing architectures, and investigate the security applications and security issues brought by this new computing paradigm.

Fig. 1 summarizes the motivation and rationale of studying SpinCIM security. We find that the emerging SpinCIM acts as a double-sided sword for hardware security. On the one hand, the new computing paradigm of SpinCIM facilitates the development of certain innovative hardware security solutions. In particular, we will discuss SpinCIM-enhanced security solutions for circuit obfuscation...
and side channel attack prevention. Although both topics have been heavily researched, we believe that SpinCIM based solutions have low performance overhead and are more effective. On the other hand, SpinCIM could also introduce new security vulnerabilities which can be leveraged by the attackers to launch new attacks. For example, typical hardware Trojan requires the insertion or modification of specific circuit for Trojan insertion and activation. While under SpinCIM, attackers are able to achieve Trojan-similar attacks by simply manipulating the thermal conditions or magnetic field, even without the need for any circuit modifications.

The rest of this paper is organized as follows: Section 2 provides the necessary background knowledge on STT-MRAM and SpinCIM, and discusses the recent research advance in hardware security. Section 3 demonstrates the enhanced security solutions for circuit obfuscation and side channel attack thwarting by SpinCIM. New security issues in SpinCIM are studied and discussed in Section 4. Section 5 provides an outlook into the research for SpinCIM security. Finally, Section 6 concludes the paper.

2 PRELIMINARIES
In this section, we provide a brief background introduction on STT-MRAM and SpinCIM as well as the current state of research on hardware security.

2.1 Spin-Transfer Torque Magnetic RAM
STT-MRAM is a promising next generation memory that features non-volatility, fast writing and reading, high endurance, and zero standby power [8–12]. As Fig. 2 shows, a typical STT-MRAM bit-cell consists of an access transistor and a Magnetic Tunnel Junction (MTJ), which is controlled by bit-line (BL), word-line (WL) and source-line (SL). An MTJ consists of one pinned ferromagnetic layer (PL) with a fixed magnetic orientation, one free ferromagnetic layer (FL) whose magnetic orientation can be switched, and one tunneling oxide barrier between PL and FL. The relative magnetic orientations of PL and FL can be stable in parallel (P state) or anti-parallel (AP state), corresponding to low resistance ($R_P$) and high resistance ($R_{AP}$, $R_{AP} > R_P$) of the MTJ cell, respectively. As a result, each MTJ is able to store 1-bit information. In this paper, we assume that the low resistance state is used to represent logic ‘1’, and the high resistance state is used to represent logic ‘0’.

To read out the stored information in an MTJ cell, one needs to enable WL signal, apply a voltage $V_{read}$ across BL and SL, and sense the current that flows ($I_P$ or $I_{AP}$) though the MTJ. By comparing the sense current with a reference current ($I_{ref}$, $I_{AP} < I_{ref} < I_P$) the data stored in MTJ cell (logic ‘0’
Fig. 3. SpinCIM computations in enhanced STT-MRAM array.

or logic ‘1’) could be read out. Writing operation can be performed by enabling WL, then applying appropriate voltage ($V_{\text{write}}$) across BL and SL to pass a current that is greater than the critical MTJ switching current. The specific logic value that is written is dependent on the direction of the write current.

2.2 Spin-Based Computing-In-Memory

CIM efforts can be classified into two categories according to whether they target at application-specific computations [13–15] or general-purpose computations [11, 16–20]. For example, ReRAM has been widely explored and used to implement the matrix-vector multiplication for neural network accelerations with the multi-bit storage property. Compared to other resistive memory devices (such as ReRAM), STT-MRAM has higher write endurance, faster write speed, lower write energy, and limited resistance difference between the distinct resistance states of MTJ. STT-MRAM is widely used to implement bit-wise operations for general in-memory computing paradigm. In this paper, we focus on such general-purpose CIM [16], which can be widely used in all categories of applications.

Due to the current sensing mechanism in STT-MRAM and the fact that current can be accumulated, SpinCIM is able to realize logic functions conveniently. As demonstrated in Fig. 3, by simultaneously enabling word-line $WL_i$ and $WL_j$, then applying $V_{\text{read}}$ across $BL_k$ and $SL_k$ ($k \in [0, n-1]$), the current that feeds into the k-th sense amplifier (SA) is a summation of the currents flowing through $MTJ_{i,k}$ and $MTJ_{j,k}$, namely $I_{i,k} + I_{j,k}$. With different reference sensing current, the sense amplifier will have different outputs under given input patterns, thus different logic functions of the enabled word line can be directly implemented.

In SpinCIM computing paradigm, the core bit-cell and array structure of STT-MRAM remain unchanged. One only needs to make insignificant modifications to the peripheral circuitry (such as sensing circuitry to generate required sensing current) of the memory. Therefore, the impact of introduced SpinCIM on density and efficiency of memory arrays is negligible [16].

In the architecture level, to invoke the different types of operations that can be performed by SpinCIM in the enhanced STT-MRAM array, the instruction set architecture (ISA) of the processor needs to be extended. For SpinCIM computations, the operation type, address of operation data, and address of result are sent to memory, then the operations can be completed within the memory. The overall computation needs only one memory access. As a comparison, traditional computations
need to fetch operation data from memory to processor, perform computations in the processor, then write the result back to memory, which involve \( M + 1 \) \((M\) is the number of operation data that needs to fetch from memory\) number of memory access. Take the \textbf{Add} operation as an example, as shown in Fig. 4, to add two data that are stored in the main memory, the typical four instructions can be replaced by one \textbf{CimADD} instruction in \textit{SpinCIM}. The number of memory operations is reduced from three to one, which is obviously more time and energy efficient.

2.3 Hardware Security

As the root of software, system, and network security, in recent years, hardware security has become a hot topic and attracted attention from both industry and academia [21, 22]. The continually increasing design complexity and cost have led to the globalization of integrated circuit (IC) design and fabrication, where counterfeits may exist in all phases of the supply chain and bring serious security concerns. Design intellectual property (IP) infringement, reverse engineering attacks, hardware Trojans, side channel attacks, and others have caused both security concerns and economic loss in semiconductor industry [21–24]. To ensure the integrity and the trustworthiness of fabricated circuits, various defensive approaches have been proposed. There are passive ones like circuit watermarking/fingerprinting techniques, proactive strategies such as circuit obfuscation and Trojan detection/prevention techniques. Security primitives such as physical unclonable function (PUF) and true random number generator (TRNG) have been proposed to provide authentication and encryption. To reduce the performance overhead of CMOS-based security techniques, researchers have explored to utilize the unique intrinsic properties of emerging devices, for example, in circuit obfuscation strategies, polymorphic gates have been designed with the tunable polarity of SiNW FET [25] and MRAM is used to replace SRAM to configure the functionalities of multiplexers [26, 27]. However, these approaches follow the same design methodology as the previous CMOS-based ones, thus they are still vulnerable to SAT-based attacks. Moreover, to thwart side channel attacks, it needs to slow down the fast operations and to increase the power consumption of low-energy operations to equalize the performance of different memory operations, which brings non-trivial performance overheads [28]. This motivates us to explore the possible solutions to these security concerns with the new \textit{SpinCIM} computing paradigm and investigate the security vulnerabilities in \textit{SpinCIM}. Our work in this paper is different with previous work in that we focus on the \textit{SpinCIM} computing architectures, and investigate the security issues brought by this new computing paradigm.
3 SPINCIM ENHANCED HARDWARE SECURITY

Because of the aforementioned properties of SpinCIM, it can solve some of the long standing challenges in hardware security. In the section, we demonstrate this with examples on how to apply SpinCIM for circuit obfuscation and prevention of side channel attacks.

3.1 Enabling Circuit Obfuscation

Circuit obfuscation has been proposed as one proactive countermeasure against a variety of hardware attacks, such as reverse engineering (RE) and IC/IP piracy, through hiding valuable circuit design information [29, 30]. Since it was proposed in 2012, the fierce race between sharpening the spears of de-obfuscation tools and making the obfuscation shield more robust has quickly elevated the sophistication and maturity level of circuit obfuscation, making it one of the most effective countermeasures against RE-based attacks and IC/IP piracy.

Two major issues exist in current circuit obfuscation techniques. First, the recently proposed SAT-based de-obfuscation attack poses serious threats to the effectiveness of circuit obfuscation techniques. For the current anti-SAT approaches (such as CamoPerturb [31], And-Tree [32], Anti-SAT [33]), they are either vulnerable to bypass/removal attacks [34, 35], or can be revealed by approximate attacks [36, 37]. Second, the delay, power, and area overhead of the state-of-the-art circuit obfuscation strategies are so high that they cannot be applied in commercial circuits, especially when the security requirement is high. For example, an obfuscating units that can be either NAND, NOR, or XOR has $5.1 \times 5.5 \times$ higher power, $4 \times$ larger area, and $1.1 \times 1.6 \times$ longer delay compared to a conventional NAND or NOR logic gate [30].

To meet the above challenges in CMOS-based obfuscation methods, researchers have attempted to exploit the unique properties in post-CMOS emerging devices to perform obfuscation. For example, polymorphic gates have been designed with the tunable polarity of SiNW FET [25], MRAM is used to replace SRAM to configure the functionalities of multiplexers [26, 27], and spintronic devices are designed to be able to perform one of the multiple functionalities with identical layout [38–40]. By utilizing the intrinsic features (such as tunable polarity) in these emerging devices, one can reduce the performance overhead dramatically.

Due to the current sensing property and the fact that current can be accumulated, spintronic is suitable to implement general-purpose computing-in-memory, and such CIM architecture facilitates obfuscating the function that is implemented in the memory array. Therefore, SpinCIM naturally facilitates computing-in-memory and thus obfuscation. Now we elaborate how SpinCIM-enabled
obfuscation solution will have no chip area overhead and can be secure against SAT-based attacks. Recall that in SpinCIM paradigm, some portion of the computation will be completed in the STT-MRAM array to reduce the data transfer between memory and CPU. The SpinCIM instructions, consisting of the type of the operation and the memory address of the operands, will be sent to the memory array. More specifically, memory address of the operands will be sent to the address decoder unit to enable corresponding word-lines, and the type of the operation will be sent to the memory control unit. Then the control unit generates corresponding control signals to complete the computations [16]. Different functions can be implemented with exactly the same hardware memory units and the same peripheral circuitry of STT-MRAM memory array. It is the run-time control signals that will determine the functionality implemented by the STT-MRAM memory array (see Fig. 5). In other words, the portion of computation performed in the STT-MRAM array has been obfuscated naturally. At this point, as long as the designer decides which portion to be implemented in STT-MRAM array, there is no hardware overhead for the obfuscation. To achieve a higher level of obfuscation and protect the peripheral circuit design, the designer may obfuscate the peripheral circuitry in order not to give the attacker any hint on the functions that are implemented in the STT-MRAM array. The peripheral circuit of STT-MRAM array normally only takes a very small percentage of the whole circuit, thus the overhead, if any, will be negligible [16].

As the right half of Fig. 5 shows, an RE attacker might be able to obtain the netlist and be able to solve the portion of the computation that is implemented in the traditional CMOS technology by arithmetic unit, even if it is obfuscated. To perform SAT-based de-obfuscation attacks, the attacker needs to get the gate-level netlist which consists of conventional logic gates and obfuscated gates, the oracle function, and the set of possible functionalities of obfuscated gates. Even if the attacker is able to get the oracle function of the circuit, in SpinCIM-enabled obfuscation, the obfuscated functions that are implemented in the STT-MRAM array appear as identical memory array for an RE attacker, and the obfuscated peripheral circuit reveals nothing about the possible functionalities in SpinCIM. As a result, SAT-based attacks cannot be formed, and this solution will be secure against existing SAT-based attacks. Without the knowledge of this portion of the computation, the incomplete design the attacker has obtained from the traditional CMOS implementation also might become meaningless.

The key challenge for SpinCIM-enabled obfuscation techniques is how to split the functions into CMOS implementation and SpinCIM implementation and how to make them co-operate efficiently at the high level [41, 42]. Those computation-intensive applications with simple few control logic is suitable to be implemented by SpinCIM, and for specific computations, the benefits can be maximized when the operation data are from memory and the result data needs to be stored back to memory. Overall, it needs the device to algorithm level collaborations and much more related research to apply SpinCIM.

3.2 Thwarting Side Channel Attacks

Side channel attacks aim to reveal the sensitive or secret information by analyzing the data that can be obtained during the execution of a computer system through channels such as power consumption profile and timing delay [43]. Since it was first reported, side channel attack has become one of the most powerful and effective attacks and poses threats to the security of computer system [44].

In STT-MRAM array, asymmetry exists in the Read and Write operations, which facilitates statistical analysis. We have performed device and circuit simulations for memory operations. Specifically, at the device level, we jointly use the Brinkman model and Landau-Lifshitz-Gilbert (LLG) equation to characterize MTJ, and the key parameters for MTJ simulation are demonstrated in Table 1. For the circuit level simulation, a Verilog-A core block of STT-MRAM device is designed
to build the circuit with a 45nm free Product Development Kit (PDK) library in Cadence. As demonstrated in Table 2, the latency and current of \textit{Write} are higher than those for \textit{Read}. Furthermore, switching to \textit{P} state is easier than switching to \textit{AP} state, which is known as the polarity-dependent asymmetry for \textit{Write} latency and \textit{Write} current. As a result, writing logic ‘1’ and writing logic ‘0’ incur different latency and current. These features introduce major security vulnerabilities which have been exploited by side channel attackers who can monitor the signatures during memory \textit{Read}/\textit{Write} operations to compromise data privacy [28, 45–47]. For example, as demonstrated in Fig. 6(a), a side channel attacker can monitor the timing information of the data movement into and out of the STT-MRAM memory array when the hardware runs cryptography applications.

To mitigate the security vulnerabilities in the STT-MRAM array, researchers have tried various strategies to wipe out the side channel signatures. Representative ones include parity encoding, short retention, and constant current write techniques [28]. To equalize the performance of different memory operations, these countermeasures need to slow down the fast operations and to increase the power consumption of low-energy operations. This brings significant design overheads in terms of delay and power. Next, as shown in Fig. 6(b), we demonstrate that SpinCIM is able to thwart side channel attacks on STT-MRAM memory array because of the following two features.

\textbf{Increased operation types.} In standard STT-MRAM array, there are only two operations between memory and CPU. The \textit{Read} operation that reads data from specified memory address then sends the data to CPU; and the \textit{Write} operation that receives data from CPU then writes the data into specified memory address. As shown in Table 2, four levels of side channel information during reading ‘1’, reading ‘0’, writing ‘1’, and writing ‘0’ can be monitored and analyzed. A side channel
Table 1. Key Parameters for MTJ Simulation.

| Parameter                        | Value       |
|----------------------------------|-------------|
| MTJ Surface Length               | 40 nm       |
| MTJ Surface Width                | 40 nm       |
| Spin Hall Angle                  | 0.3         |
| Resistance-Area Product of MTJ  | $10^{-12} \Omega \cdot m^2$ |
| Oxide Barrier Thickness          | 0.82 nm     |
| TMR                              | 100%        |
| Saturation Field                 | $10^6 A/m$  |
| Gilbert Damping Constant         | 0.03        |
| Perpendicular Magnetic Anisotropy| $4.5 \times 10^5 A/m$ |
| Temperature                      | 300 K       |

Table 2. Delay and Energy Consumption of Read/Write Operations in Standard STT-MRAM Array.

| Operation | Delay (ns) | Energy (fJ) |
|-----------|------------|-------------|
| Read ‘1’  | 0.6        | 8.611       |
| Read ‘0’  | 0.6        | 7.669       |
| Write ‘1’ | 4.4        | 233.300     |
| Write ‘0’ | 3.3        | 191.400     |

Table 3. Delay and Energy Consumption of Read/Write and SpinCIM Operations in Enhanced STT-MRAM Array.

| Operation | Delay (ns) | Energy (fJ) |
|-----------|------------|-------------|
| Read ‘1’  | 0.63       | 22.69       |
| Read ‘0’  | 0.67       | 23.85       |
| Write ‘1’ | 4.40       | 244.64      |
| Write ‘0’ | 3.30       | 202.70      |
| CimNOT    | 0.60       | 22.20       |
| CimAND    | 0.55       | 22.30       |
| CimOR     | 0.53       | 22.90       |
| CimNAND   | 0.45       | 18.89       |
| CimNOR    | 0.45       | 21.00       |
| CimXOR    | 0.53       | 26.34       |
| CimADD    | 0.53       | 26.32       |

attacker will be able to differentiate the Read/Write operations, and analyze the number of ‘1’/’0’ in a word with statistical methods.

However, in SpinCIM STT-MRAM array [16], there are 11 possible operations. Besides the basic Read and Write operations, it also supports CimNOT, CimAND, CimOR, CimNAND, CimNOR, CimXOR and CimADD operations\(^1\). Table 3 gives the delay and power of these SpinCIM operations. This makes side channel attacks much more complex. For instance, some of the logic computation operations such as CimNOT, CimAND, CimOR, CimNAND, CimNOR, CimXOR and CimADD have similar delay and power

\(^1\)Note that the number of enabled possible logic functions by SpinCIM depends on the peripheral circuits of the STT-MRAM array and it can slightly vary with different SpinCIM implementations.
consumption as Read ‘1’/’0’. Therefore, identifying Read ‘1’/’0’ will become more challenging. As another example, when SpinCIM logic computation results are required to be written into a specific memory address, which means a SpinCIM logic computation operation may be followed by a Write operation. In this case, a SpinCIM computation operation plus a Write ‘0’ operation can obscure a Write ‘1’ operation since they have similar delays and power consumption.

**Reduced data transfers.** In conventional logic computation instructions, the operation data needs to be read from the memory and sent to CPU, the computation result also needs to be sent back to the memory from CPU. The operation data and the result data are transferred between CPU and memory though system bus, giving the side channel attacker more opportunities to exploit the information leakage in the system bus to reveal the transferred data. While in SpinCIM logic computations, only the instructions that include the operation/result data addresses and the operation type are sent to the memory, then all the operations will be completed within the memory. The operation mechanism of SpinCIM decreases the data transfers between CPU and memory, thus reducing the risks of being exploited and attacked by adversary side channel attackers. Note that there are various types of side-channel attacks. For those that exploit the operation type information, SpinCIM may confuse the attacker with the increased number of operation types. And for the cases that the attacker tries to utilize the operation data for secret analysis, SpinCIM prevents the attack from exploiting operation data information leakage in the system bus.

Current consumption trace matters in power-based side channel attacks, and the energy in Table 2 and Table 3 is the integral of the product of current and voltage, which is closely related to the current consumption. Assume that the objective of SCA is to retrieve the internal secret key $k$ of a crypto-algorithm, and the adversary can observe the input $p$ and the overall power consumption. The attacker will find an intermediate result $v$ (such as the current consumption trace) that depends on both $p$ and $k$. By observing the side-channel leakage of $v$, a hypothesis test on the key value $k$ can be created, and it can be expressed as: $L(k^*) = f_{k^*}(p) + \varepsilon$. The function $f_{k^*}$ is dependent on the crypto-algorithm and the specific implementation. The error $\varepsilon$ is an independent noise variable, defined by other unrelated activity in the crypto-implementation and measurement errors [48]. Several types of power-based side channel analysis have been formulated starting from this relation, such as Correlation Power Analysis (CPA) and Simple Power Analysis (SPA). In both cases, for SpinCIM computing paradigm, the increased operation types could increase noise $\varepsilon$, and the reduced data transfer makes the exact formulation of function $f$ more difficult. As a result, SpinCIM offers considerable resilience against side channel attacks.

### 4 SECURITY ISSUES IN SPINCIM

Numerous advantages have been demonstrated in SpinCIM. From the performance perspective, it is able to alleviate the memory wall bottleneck in Von-Neumann computer structures. And from the security perspective, as demonstrated in this paper, it is a natural fit for some protective or preventive hardware security techniques. However, the precondition to apply SpinCIM for performance improvement and security enhancement is that SpinCIM itself should be robust and secure enough. In this section, we analyze the intrinsic security vulnerabilities in SpinCIM, and demonstrate a case study in practical attacking scenarios to gain a glimpse of the security issues within SpinCIM. Finally we discuss some potential mitigation techniques.

#### 4.1 SpinCIM Security Vulnerabilities

In standard STT-MRAM array, the current flowing through SL ($I_{SL}$) has two possible values, i.e. $I_P$ and $I_{AP}$. The TMR ($R_{AP} - R_P / R_P$) usually lies between 100% and 200% [49]. How to sense the current difference accurately to achieve reliable memory read has been a vital challenge for the commercial adoption of STT-MRAM. Both process variations and environmental factors (such as
temperature and magnetic field) can affect the reliability of STT-MRAM. As a result, there have been extensive studies on this reliability issue and corresponding countermeasures, such as increasing TMR and adopting ECC (error-correction codes) strategies [50–56]. In this paper, we focus on the security and reliability issues that emerge with the new SpinCIM computing paradigm.

For SpinCIM operations, the reliability problem is more challenging. Recall that in Fig. 3, for two-input SpinCIM computations, the current flowing through SL is the sum of currents flowing through two MTJs, thus has three possible values, i.e. $I_{P,P}$, $I_{P,AP}/I_{AP,P}$\(^2\) and $I_{AP,AP}$. Therefore, different with normal Read operation, which has only one read margin between $I_P$ and $I_{AP}$, in SpinCIM operations, there are two read margins, one between $I_{AP,AP}$ and $I_{AP,P}$, and the other one between $I_{AP,P}$ and $I_{P,P}$. Simulation results in Fig. 7(a) and Fig. 7(b) demonstrate the read margin in conventional STT-MRAM array and the read margins in SpinCIM-enhanced STT-MRAM array. We can see that each of the SpinCIM read margin is smaller than that in normal Read operation. Specifically, in normal Read operation, the read margin between $I_P$ and $I_{AP}$ is about 5.5 $\mu$A, while in SpinCIM operations, the read margin between $I_{AP,AP}$ and $I_{AP,P}$ is about 3.2 $\mu$A, and the read margin between $I_{AP,P}$ and $I_{P,P}$ is about 2.5 $\mu$A. The small read margins in SpinCIM could result in higher decision failure rates and make it more challenging to ensure reliable computations. This can be exploited by malicious attackers and we will demonstrate a case study in practical scenarios.

\(^2\)This paper assumes $I_{P,AP}$ equals to $I_{AP,P}$, and the rest of the paper will denote both $I_{P,AP}$ and $I_{AP,P}$ with $I_{AP,P}$.
4.2 A Case Study in Authentication System

In this part, we investigate the security vulnerabilities of SpinCIM with a case study of authentication system. It is demonstrated that an attacker is able to bypass the authentication by simply manipulating the thermal conditions of STT-MRAM array.

Authentication system is widely used in most of the information systems and services. It provides access control for protected resources (such as the credit card numbers) by checking whether a user’s credentials match the authorized users database. In normal modes, users are identified with a username and a password. When the username and password are both correct, the user is authorized to access the system. Such access control principle can be implemented with the following high-level programming sentences:

\[
\text{IF (username is correct AND password is correct) }
\text{ THEN validate pass, enter the system!}
\]

In the low-level implementation, it needs to check the username and password that are typed in by the user (represented as \(u_t\) and \(p_t\)) with the username and password items in the authorized users database (represented as \(u_d\) and \(p_d\)). Checking whether two items are identical can be achieved with the XNOR operation: \(x \oplus y = 1\) when \(x\) equals \(y\), otherwise, \(x \oplus y = 0\). To reduce the data transfer bottleneck, the authentication process may be accomplished in the enhanced STT-MRAM array. Thus the user is authorized to the system if and only if:

\[
(u_t \oplus u_d) \land (p_t \oplus p_d) = 1
\]

CimXNOR operation can be typically realized as below [16]:

\[
\begin{align*}
(u_t \oplus u_d) &= (u_t \land u_d) \lor (u_t \land \overline{u_d}) \hfill (2) \\
(p_t \oplus p_d) &= (p_t \land p_d) \lor (p_t \land \overline{p_d}) \hfill (3)
\end{align*}
\]

Assume that a malicious attacker judiciously trigger a certain mistake to perform certain CimAND function as CimOR (the feasibility will be discussed later), then the attacker is able to conduct effective bypass access control attack.

By triggering the CimAND in Equation (1) as CimOR, the judgment becomes:

\[
(u_t \lor u_d) \lor (u_t \land \overline{u_d}) = (u_t + u_d) + u_t + \overline{u_d} = 1
\]

Therefore, the attacker gains access to the system when either the username is correct or the password is correct. The corresponding high-level control sentence is:

\[
\text{IF (username is correct OR password is correct) }
\text{ THEN validate pass, enter the system!}
\]

As a result, even though the attacker is not aware of the passwords, he is able to access the system simply with a correct username. And username is easy to be pirated because it is mostly related to the user’s phone numbers or real names thus easy to guess, and usually not technically protected.

A more powerful attack can be launched to bypass both user and password authentications. By triggering CimAND in Equation (2) as CimOR, it becomes

\[
(u_t \lor u_d) \lor (u_t \land \overline{u_d}) = (u_t + u_d) + u_t + \overline{u_d} = 1
\]
Table 4. Truth Table for CimAND and CimOR Operations.

| Logic | MTJ States | \(I_{\text{SL}}\) | Function |
|-------|------------|------------------|----------|
|       |            | \(I_{\text{AP\textendash}P}\) | CimAND† | CimOR‡ |
| 0, 0  | AP, AP     | \(I_{\text{AP\textendash}P}\) | 0        | 0      |
| 0, 1  | AP, P      | \(I_{\text{AP\textendash}P}\) | 0        | 1      |
| 1, 0  | P, AP      | \(I_{\text{AP\textendash}P}\) | 0        | 1      |
| 1, 1  | P, P       | \(I_{\text{P\textendash}P}\) | 1        | 1      |

† \(I_{\text{ref\textendash}and} \in (I_{\text{AP\textendash}P}, I_{\text{P\textendash}P})\)
‡ \(I_{\text{ref\textendash}or} \in (I_{\text{AP\textendash}P}, I_{\text{P\textendash}P})\)

Fig. 8. Confusion between \(I_{\text{AP\textendash}P}\) and \(I_{\text{ref\textendash}and}\).

Similar manipulation can be applied to Equation (3). Then Equation (1) becomes

\[
1 \text{CimAND} 1 = 1.
\]

Corresponding high-level access control sentence is

IF (ALWAYS TRUE)
{THEN validate pass, enter the system!}

As a result, all users that attempt to gain access to the system, including the illegal users, are authorized to enter the system.

Feasibility of triggering CimAND as CimOR. Table 4 demonstrates the truth table of CimAND and CimOR operations. Only when the two MTJ states are AP and P, CimAND and CimOR have different outputs: logic ‘0’ and logic ‘1’, respectively. Therefore, as demonstrated in Fig. 8, to trick CimAND into CimOR, \(I_{\text{AP\textendash}P}\) needs to be sensed as larger than \(I_{\text{ref\textendash}and}\). Recall that the read margin between \(I_{\text{AP\textendash}P}\) and \(I_{\text{P\textendash}P}\) is smaller than other read margins, it is easier to confuse \(I_{\text{AP\textendash}P}\) with \(I_{\text{ref\textendash}and}\). In this case, the output under AP, P will be mistakenly computed as logic ‘1’, which is the correct output of CimOR.

To evaluate the failure rate of performing CimAND as CimOR operation, we conduct 10000 Monte Carlo simulations for CimAND operations under natural conditions and intentional attack conditions. In the intentional attacking scenario, the target MTJs are dealt with laser heat in the same way as [57]. While the resistance of P-state MTJ is relatively stable under laser heat conditions, the resistance of AP-state MTJ demonstrates an obvious declining trend. Accordingly, under laser heat, \(I_{\text{AP\textendash}P}\) will slightly increase, and be more closer to \(I_{\text{ref\textendash}and}\), resulting in a higher possibility to sense \(I_{\text{AP\textendash}P}\) as larger than \(I_{\text{ref\textendash}and}\). The simulation results in Table 5 validate that the main failure of
Table 5. CimAND Failure Rates Under Natural Conditions and Laser Heat Conditions.

| Failure               | Natural | With Laser Heat |
|-----------------------|---------|-----------------|
|                       | 20°C    | 50°C            | 100°C           |
| $I_{AP,P} > I_{ref-and}$ | 0.5%    | 0.6%            | 4.4%            |
| $I_{AP,AP} > I_{ref-and}$ | 0       | 0               | 0.3%            |

CimAND come from $I_{AP,P} > I_{ref-and}$. Under natural conditions, the failure rate of $I_{AP,P} > I_{ref-and}$ is 0.5%. After intentional laser heat to 100°C, the failure rate of $I_{AP,P} > I_{ref-and}$ increases to 4.4%, which is 8.8× higher than the natural conditions. Such high failure rate of CimAND greatly threatens the security of computer systems that employ SpinCIM.

4.3 SpinCIM Security Vulnerabilities Mitigation

To relieve the reliability problem in SpinCIM computations, extending ECC strategies [16] have been proposed. It tries to detect and correct the sensing errors. However, as demonstrated in Fig. 3, SpinCIM does not sense the individual resistance state of the input MTJs. Instead, only the sum of the currents of the two MTJs matters. Therefore, the extended ECC scheme to correct the sense errors in input MTJs is insufficient in correcting errors in SpinCIM computations.

Recall that the factors that affect the robustness of SpinCIM are the degraded sensing margins and external disturbance. Increasing the TMR of MTJ to increase the sensing margins is one effective way, however, it is out of the scope of this paper and much research has put emphasis on this topic. For the external disturbance, a possible countermeasure is to design sense amplifier in a disturbance-aware way. Take the laser heat disturbance for example, assuming that before laser heated, the three possible MTJ currents are $I_{AP,AP}$, $I_{AP,P}$ and $I_{P,P}$, and after being laser heated, they become $(I_{AP,AP} + \alpha)$, $(I_{AP,P} + \beta)$ and $(I_{P,P} + \gamma)$, respectively, where $0 < \alpha < \beta < \gamma$. Then the reference currents of CimOR, namely $I_{ref-or}$, can be accordingly adjusted from $I_{AP,AP}$ to $I_{AP,AP} + \alpha + \beta$ and $I_{ref-and}$ can be accordingly adjusted from $I_{AP,P}$ to $I_{AP,P} + \beta + \gamma$. Although a preliminary thought of the possible mitigation method is discussed, its implementation detail and its effectiveness need much more further in-depth study. In addition, how to assure the reliability of SpinCIM remains an open question, we may focus on this issue in the future work.

5 OUTLOOK FOR SPINCIM SECURITY

With the unique features of computing, SpinCIM has demonstrated a lot of advantages in facilitating hardware security techniques. For circuit obfuscation techniques, functions that are implemented in enhanced STT-MRAM array can be judiciously hidden from a reverse engineering attacker. As for thwarting side channel attack, SpinCIM reduces the data transfers between CPU and memory thus reduces side channel information leakages, and increases the operation types within the STT-MRAM array, thus complicates the malicious power or timing side channel analysis. However, in addition to these positive features, SpinCIM also exposes some security vulnerabilities due to the degraded read margins and being sensitive to external disturbance. A case study in authentication systems demonstrates that an attacker is able to achieve Trojan-similar attacks by simply manipulating the thermal conditions of STT-MRAM, even without the need for circuit modifications. Possible mitigation methods are discussed while future in-depth study is still needed.

Perhaps the biggest challenge for both SpinCIM and SpinCim security applications is the code mapping and the data mapping problem. Code mapping decides which operations should be executed in memory and which operations should be executed in CPU and how to make them...
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Most of the CIM techniques only support computations when the operation data are stored in the same bank, mapped to different rows, and stored in the same set of columns. Code mapping and data mapping research need collaboration work from the device, logic, architecture and application levels. Only when the SpinCIM computing paradigm becomes mature in all design levels, its application for hardware security can be enriched, and its intrinsic security vulnerabilities can be solved better.

Also previously, security has often been considered as an afterthought, with performance dominating the design requirements, resulting in numerous security vulnerabilities. While SpinCIM is newly proposed and still in exploration progress, it provides an opportunity to reconsider security as a first class requirement at the design stage. Research on SpinCIM security should synchronize with the study in SpinCIM computing paradigm. To this end, more hardware security opportunities and challenges that are related to SpinCIM will emerge with the more and more in-depth investigation in SpinCIM, thus deserves to be given full attention in future works.

6 CONCLUSIONS
Spin-based computing in memory techniques have demonstrated promise in alleviating memory wall challenges in traditional Von-Neumann architectures, thus has attracted attention from both industry and academia communities. In this paper, we have studied SpinCIM from a security perspective. We have investigated the feasibility to enhance hardware security with the unique properties in SpinCIM computing paradigm and found that SpinCIM was a natural fit for some security applications. We have also discussed about the possible security vulnerabilities in SpinCIM and demonstrated with a case study in practical attacking scenarios, then discussed possible mitigation techniques and presented an outlook to the future research for SpinCIM security.

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