Sense amplifier design using CMOS-memristor circuits

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Abstract—With the increase of the speed of computers, timing and power requirements are becoming crucial for memory devices. The main objective of the paper is to modify 180nm CMOS sense amplifier design by using memristive devices and improve the design in terms of on-chip area, power efficiency, resistance to temperatures and speed. To achieve this, NOT gates in the circuit were constructed using memristor and CMOS. The main aim of the paper is to check the effect of memristors on characteristics of sense amplifier. The design was tested on Conventional Current Sense Amplifier (CSA) circuit. Changes in power, area, sensing delay and offset are reported in the paper.

I. INTRODUCTION

Nowadays, SRAMs (Static Random Access Memory) have become irreplaceable part of modern computing architectures. They are mainly used in Level 1 and 2 caches and consist of components such as memory cell array, decoders, sense amplifiers, etc. Sense amplifier is an essential part of SRAM. Its main function is to identify small differences on bitlines and amplify them to noticeable levels before their full charge or discharge. This greatly improves the speed of work of SRAMs, which is very crucial for present-day computer devices. Therefore, the main focus of this paper is to improve existing design of sense amplifiers by adding memristors and checking their progress in terms of performance.

The memristor is the fourth basic circuit element along with resistor, capacitor and inductor, which introduces a relation between flux and charge. In recent years, they are more frequently applied in fields such as neuromorphic systems and signal processing due to their heat efficiency, power efficiency and reliability. Therefore, we explore the possibility of using memristor in sense amplifier design.

This paper is organized as following: Section 1 gives a brief introduction about sense amplifiers and memristors, Section 2 discusses sense amplifier characteristics, which will be investigated, Section 3 shows results of the simulation and Section 4 gives conclusion of this paper.

II. BACKGROUND

A. Sense Amplifier

Sense amplifiers are used to identify very small voltages and currents on the bitlines and amplify them to detectable degree. Conventional current sense amplifier from Fig.1 is composed of classic cross-coupled latch structure, consisting of transistors M1-M4. Additionally, transistor M7 represent circuitry for sense activation and M5,M6,M8 are needed for bitline equalization. The work cycle of sense amplifier consists of 2 phases; precharging phase and sensing phase. This two phases are controlled by PRE and SAEN signals, which can be seen on the Fig.1. First, precharge phase is activated by driving PRE signal low. In this phase, bitlines are precharged to 1.8V. In the second, sensing phase, cross-coupled latch is turned on by driving both signals high. In this phase, output is directed to corresponding pins.

B. Parameters Under Consideration

Two main parameters of sense amplifiers which will be discussed are sensing delay and offset. The effect of temperature and W/L variations on delay and offset will be investigated. Sensing delay is the time between sensing is enabled till the full voltage swing is obtained (stable 1 or 0). Sensing offset is the minimum difference on the bitlines required for proper output of SA.

Other parameters under consideration include power and total area of the circuits.
III. Methodology

A. Proposed Design

The original design has cross-coupled latch structure, which consists of 2 CMOS NOT gates. This two gates can be replaced with memristor and NMOS instead of CMOS and NMOS. The proposed design can be seen on Fig.2. Different circuit parameters are presented in Table 1.

TABLE I: Parameters of proposed circuit.

| Parameter                        | Value         |
|----------------------------------|---------------|
| VDD                              | 1.8V          |
| Reference bitline current        | 100nA         |
| (W/L) for NMOS                   | 0.18µm / 0.36µm |
| (W/L) for PMOS                   | 0.18µm / 0.72µm |
| Bitline Capacitances             | 50pF          |

B. Mathematical analysis

For design of the circuit, it is very crucial to understand the small signal model. The small signal model of the CMOS transistor can be seen on Fig.3. Parameters of small signal model are found using following formulas.

\[ r_o = \frac{1 + \lambda V_{DS}}{\lambda I_D} \]  

\[ r_o = \mu C_{ox} \frac{W}{L} (V_{GS} - V_{th}) \]

The small signal model of proposed design can be seen on Fig.4. Memristor is replaced with resistance in small signal model.

IV. Simulation results

From simulation of the circuit, it was noticed that CSA can detect very small current differences, but the output voltage will be proportionally low. CSA gives full voltage output (VDD) only at high current differences. So voltage offset is very small and may be omitted. For further analysis of the circuit, bitline currents of 1nm and 200nm will be used for 0 and 1 respectively.

A. Effect of W/L variation

For this simulation, widths of M5, M6 and M8 transistors were varied. It was deducted that width variation does not affect the delay of the sense amplifier. It gives output of 0.8V with a delay of 3.3µs for all widths chosen.

B. Area and power calculations

One of the profits of using memristor is small on-chip area in comparison with CMOS transistors. It is known that the area of the CMOS transistor is calculated using following formula

\[ Area = 3 \times Width \times Length \]
Using the above equation, the total area of the original circuit was found to be $2.592 \text{pm}^2$. When the circuit is modified, two PMOS transistors are removed, reducing the area to $2.0736 \text{pm}^2$. This is 20% reduction in area. Considering small area of the memristors, new design will have much smaller on-chip area.

If the bitline current is chosen to be 200nA, power consumption of original circuit is 540nW. For the proposed circuit, power consumption has increased to 566nW.

C. Temperature analysis

The variation of sense amplifier with temperature can be seen on Fig.5. The delay of the amplifier decreases as temperature decreases. Also, the amplitude of output voltage decreases with increasing temperature. So lower temperatures are preferable for the circuit.

![Fig. 5: Proposed Design of CSA](image)

V. Conclusion

In this paper, the design of conventional current sense amplifier with memristive elements was presented. Overall, the same performance in terms of delay and offset was reported with decrease in amplitude of the output for low currents. However, reduction of on-chip area by approximately 20% was reported with memristors. The amount of power has increased by 26nW, which is negligible compared with overall power of the circuit. Additionally, it was noted that the circuit operates better at low temperatures, showing good performance in terms of delay and output amplitude.

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