Energy Storage System Design for a Power Buffer System to Provide Load Ride-through

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Abstract-- The design of a power buffer to mitigate the negative impact of constant power loads on voltage stability as well as enhancing ride-through capability for the loads during upstream voltage disturbances is examined. The power buffer adjusts its front-end converter control so that the buffer-load combination would appear as a constant impedance load to the upstream supply system when depressed voltage occurs. A battery energy-storage back-up source within the buffer is activated to maintain the load power demand. It is shown that the buffer performance is affected by the battery state of discharge and discharge current. Analytical expressions are also derived to relate the buffer-load ride-through capability with the battery state-of-discharge. The most onerous buffer-battery condition under which the load-ride through can be achieved has been identified.

Index Terms-- Constant power load, lead-acid battery, power buffer, power quality, voltage stability.

I. INTRODUCTION

With the increasing wide-spread use of power electronics-based loads in electrical supply systems, important contributing factor of these loads to system stability has been recognized for some time [1]. When an upstream fault occurs and causes depressed voltage or sag, the constant power loads will draw a larger current from upstream source in order to maintain the demand. This in turn causes a larger voltage drop across the source impedance and to a further decrease in the load terminal voltage. Depending on the severity of the sag and the load demand level, the situation could develop into voltage instability or even a system collapse.

To mitigate the aforementioned voltage stability problem, active dynamic power buffer concept has been proposed to decouple the load dynamics from the upstream system during fault. In [2, 3], the authors proposed a power buffer scheme in which a capacitor is used as the form of energy-storage media to balance the mismatch in power between that supplied from upstream system and the load demand during the disturbance interval. The authors assume that the capacitor is of sufficient capacity to meet the power shortfall. Under normal conditions, the buffer scheme in [2, 3] is controlled to maintain unity power factor (UPF) at the point of common coupling (PCC). When voltage sag occurs, however, the buffer in [2, 3] adjusts the front-end converter so that the input impedance of the buffer (observed from the source side) is controlled to assume the same value as that before sag. Hence the input current would decrease proportionally as the load terminal voltage reduces. In this way, voltage drop across the source impedance would also be reduced and the voltage instability problem could be mitigated. The buffer scheme is extended in [4] to deal with unbalanced faults but with the input impedance during disturbance controlled so that the input current is balance and stays within set limit.

In all the above works, it is clear that if the severity of the disturbance is such that the upstream supply system is unable to meet the load demand, the capacitor energy storage device within the buffer must provide the shortfall. Unfortunately, all the analysis in [2-4] has not specifically addressed the design of the energy storage system. The intent of this paper is to fill this gap. In the proposed scheme, a battery energy storage system is used as the back-up power source. In Section II, the power buffer and its operation scheme are presented. Load ride-through capability, as it relates to the battery state of discharge, is analyzed in Section III. Simulation results are given in Section IV to show the effectiveness of the proposed scheme.

II. POWER BUFFER OPERATIONAL PRINCIPLE

There are several topologies proposed for the power buffer. The specific version shown in Fig. 1 is comprised of a three-phase boost converter, controlled through the PWM switching scheme and a series RL filter. The filter controls the level of harmonic generated by the converter. Usually the filter resistance is small compared to the inductance and can be neglected. Such a converter topology would allow it to operate in either rectifying or regenerating modes. It could be controlled to draw almost sinusoidal input current and with a near unity power factor at its terminals. In this system, $V_g$ represents the upstream source-side voltage at the point-of-common-coupling (PCC) of the buffer-load combination. Also, it is assumed that the filter is effective and that of the impedances shown in Fig. 1, only their components at the mains power frequency ($\omega$) need to be considered.

Under normal condition, the PWM switching scheme is controlled to maintain the dc-link voltage ($V_{dc}$) at desirable level and to meet the constant power needed by the load. The control scheme of the buffer system described in Figure 1 is...
The buffer terminal voltage phasor \( V_w \) is given in [4] where controllers have been designed to guarantee system stability and to keep \( V_{dc} \) at nominal level.

\[
V_{wd} = V_{gcd} \left[ R_i^2 + X_i (X + X_i) \right]/\left[ (R_i^2 + X_i^2) \right]
\]

\[
V_{wq} = -V_{gcd} R_i X / \left[ (R_i^2 + (X + X_i)^2) \right]
\]

Real and reactive power flows into the power buffer can be regulated through the control on \( V_w \) in the following way.

Under fault condition, one attempts to maintain the input impedance at the load-buffer terminal constant at the known pre-sag value \( R_{in} + jX_{in} \). This is achieved through controlling the buffer PWM to produce \( V_w \) given in (4). \( R_i \) and \( X_i \) are readily obtained through (3) and as \( V_g \) can be measured online, hence \( V_w \) can be generated. In this way, the power drawn by the buffer is governed by \( R_{in} \) and \( X_{in} \) and is not determined by the power absorbed by the load. In this way, the buffer-load combination is viewed as constant impedance from the source.

The approach described differs from that in [4]. Whereas in controlling power flow from the upstream source into the PCC, the approach in [4] requires the input current be controlled to within pre-set limit, the present approach achieves the power flow control by ensuring the input impedance of the buffer-load combination is exactly the same as that pre-fault. In the latter approach, the power flow into the PCC will be proportional to the square of the PCC voltage magnitude, \( V_g \). Therefore, the input power drawn by the buffer-load connection will decrease during the sag event. Any mismatch in power between that from the PCC and the load demand can be compensated by the energy storage system connected across the dc-link, thus creating a favorable situation in terms of system stability.

On the control system based on the above concept to cater for both balanced and unbalanced sags, negative phase sequence controller is design in the same manner as for the positive phase sequence system. The method is similar to that given in [4].

### III. A NEW POWER BUFFER SCHEME

From Fig. 2, the phasor diagram depicted in Fig. 3(a) can be obtained. When an upstream fault occurs and since the input impedance of the buffer-load combination remains constant at the pre-sag value, \( I_{in} \) would decrease in proportion with the voltage sag depth. From Fig. 3(a) and for a given sag, maximum real power drawn from \( V_s \) occurs when the power flow from source at the PCC is at unity power factor (UPF), i.e., \( I_{in} \) is in phase with \( V_{in} \). The phasor diagram depicting such maximum power transfer condition is shown in Fig. 3(b) and the corresponding power transfer level is
Fig. 3. Phasor diagram describing power buffer at (a) non-unity power factor and (b) unity power factor condition at the PCC.

\[ P_{\text{max}} = V_g^2 / R_{\text{in}} \]  

Hence, in the proposed scheme, once a sag is detected, i.e. \( V_g < V_{\text{g, min}} \), where \( V_{\text{g, min}} \) is typically 0.95 p.u. [5], the power buffer is switched from constant power mode to one of constant impedance mode.

Next the focus is to examine the requirement of the energy storage system when the buffer operates under the constant impedance mode.

A. Circuit Model of Buffer with Battery Storage

Unlike [2, 3] where capacitor has been proposed as the media of energy storage, battery has been considered for incorporation in the buffer scheme in this investigation. With its competitive price, lead-acid battery has become one widely used energy storage device in power systems. Moreover, battery energy storage system possesses the merit of higher specific energy capacity when compared to capacitor [6]. Hence it is likely to be suitable for the present high power application.

The proposed buffer scheme will now be described. Several lead-acid battery models have been reported in the literature [7-11]. One most commonly used model is the Thevenin equivalent representation shown in Fig. 4. In the model, \( E \) is the no-load battery voltage and \( R_s \), the internal resistance. \( R_p \) represents the non-linear contact resistance of the plate to electrolyte and \( C_p \), the capacitance of the parallel plates of the electrolyte and electrode. In practice, these battery parameters are dependent of the state of discharge \( (f) \) of the battery, the level of the discharge current and the battery operating temperature. In the present analysis, however, since it is expected that the battery is to function over short durations, one may assume \( E, R_s, R_p \) and \( C_p \) are constant over the operational period. The battery model would then be suitable for use in analyzing the behavior of the buffer.

From load side of Fig. 1 and Fig. 4, one can obtain the following equations based on basic circuit laws,

\[ \begin{align*}
    i_s &= C_p \frac{dv_p}{dt} \quad i_{cap} = C \frac{dv_a}{dt} \quad i_{hor} = i_p + v_a / R_p \quad i_{cap} = (E - v_{dc} - v_{cp}) / R_s \quad i_{hor} - i_{cap} = \Delta p / v_{dc} \end{align*} \]  

where \( v_{dc}, v_{cp} \) are the voltages across the dc-link and that across the battery capacitance \( C_p \) respectively. \( i_{hor} \) is the current in the battery branch, \( i_p \) is that in the capacitor sub-branch and \( i_{cap} \) is that in the dc-link capacitator. Let \( \Delta p(t) \) be the mismatch power between the power buffer and the constant power load. Under the UPF operating condition at the buffer terminals, \( \Delta p(t) = P_l - P_{\text{max}} \) 

\[ P_l \] represents the load power demand. \( P_{\text{max}} \) is the maximum power defined in (5) and is proportional to \( V_g^2 \).

After some algebraic manipulations of (5)-(7), one obtains the following equations to describe the dynamic behavior of the power buffer over the transient period,

\[ \begin{align*}
    0.5C_p \frac{dv_p}{dt} &= -\Delta p - v_a v_{cp} / R_p + E v_{dc} / R_s - v_{dc}^2 / R_s \quad C_p \frac{dv_p}{dt} = E / R_p - (R_s + R_p) v_{cp} / (R_s R_p - V_{dc}) - v_{dc} / R_s \end{align*} \]  

B. Steady-State Analysis of Power Buffer Operation

From (8), the equations describing the steady state of the buffer are

\[ \begin{align*}
    \Delta P + V_{dc,ss} (v_{cp,ss} / R_s + v_{dc,ss}^2 / R_s - E V_{dc,ss} / R_s) &= 0 \quad V_{dc,ss} / (R_s + R_p) V_{cp,ss} / (R_s R_p - V_{dc,ss}) - v_{dc,ss} / R_s = 0 \end{align*} \]  

where \( \Delta P, V_{dc,ss} \) and \( V_{cp,ss} \) represent steady state values of \( \Delta p, v_{dc,ss} \) and \( v_{cp,ss} \) of (8) respectively.

From (9), the relationship between the steady state voltages \( (V_{cp,ss}) \) across \( C_p \) and the mismatch power \( \Delta P \) in terms of the \( \)dc-link voltage \( (V_{dc,ss}) \) and battery parameters are

\[ \begin{align*}
    V_{cp,ss} &= R_p (E - V_{dc,ss}) / (R_s + R_p) \quad \Delta P = V_{dc,ss} (E - V_{dc,ss}) / (R_s + R_p) \end{align*} \]  

In carrying out this analysis, it is assumed that the transient process following the switching in of the battery bank has ceased. This means that only the battery resistance needs to be considered. The universal battery model given in [10] is then applicable:

\[ E = E_0 - Kf \quad R_s = R_0 - K_{rf} f \]  

In this model, \( E_0 \) and \( R_0 \) are the open circuit terminal battery voltage and the total equivalent battery resistance at full charge respectively. \( R_s \) is the total internal resistance which depends on the battery state of discharge (SOD) or \( f \). \( K \) and \( K_{rf} \) are experimentally obtained constants. When the battery is fully charged, \( f = 0 \). \( f > 0 \) indicates that the battery is in the discharged state. Conversely, \( f < 0 \) shows the battery is over-charged.

Substituting (12) into (11), the relationship between \( V_{dc,ss}, f \) and \( \Delta P \) can be obtained.

\[ V_{dc,ss} = 0.5 [E_0 - Kf + \sqrt{(E_0 - Kf)^2 - 4(R_0 - K_{rf}) f \Delta P}] \]  

Equation (13) allows one to determine \( V_{dc,ss} \) for given battery \( f \) and \( \Delta P \).

Furthermore, by substituting (5) and (7) into (13), one obtains

\[ V_{dc,ss} = 0.5 [E_0 - Kf + \sqrt{(E_0 - Kf)^2 - 4(R_0 - K_{rf}) f (P_l - V_g^2 / R_{\text{in}})}] \]  

Equation (14) relates the variations in \( V_{dc,ss} \) with the voltage magnitude \( V_g \), the battery discharge state \( f \) and the constant impedance \( (R_0) \) considered in Section II and is given by (1).

Typical curves describing (14) are shown on Fig. 5. In this figure, it is seen that for a given sag voltage \( (V_g) \), \( V_{dc,ss} \)
C. Transient Performance of Power Buffer

As mentioned in the last sub-section, one expects the variations of dc-link voltage ($V_{dc,ss}$) are controlled to within a narrow range of its nominal value. Consequently, it is reasonable to analyze the transient performance of (8) in its small-signal form as,

\[
d\delta v_{dc}/dt = -(2V_{dc,ss} + V_{op,ss} - E)\delta v_{dc}/(RC_{dc,ss}) - \delta v_{vp}/(RC_{dc,ss})
\]

\[
d\delta v_{vp}/dt = -\delta v_{dc}/(RC_{p}) - (R_{p} + \beta)\delta v_{vp}/(C_{p}R_{p})
\]

(15)

Stability and transient performance of the system following the battery switch-in may now be analyzed. From (15), one can obtain the transfer function

\[
\frac{\delta v_{dc}}{\delta p} = -(s + \alpha)[(CV_{dc,ss})(s^2 + (\alpha - \beta)s - \gamma - \alpha\beta)]
\]

(16)

where,

\[
\alpha = \frac{R_{p} + R_{p}}{R_{p}C_{p}}, \quad \beta = \frac{E - 2V_{dc,ss} - V_{op,ss}}{R_{p}CV_{dc,ss}}, \quad \gamma = \frac{1}{R_{p}^{2}C_{p}^{2}}
\]

(17)

From the characteristic equation of (16) and using Hurwitz-Routh criterion, stability of the buffer-battery system would be guaranteed if and only if

\[
\alpha - \beta > 0
\]

(18)

\[-\alpha\beta - \gamma > 0
\]

(19)

From (18), one obtains the necessary condition for stability as

\[
V_{dc} > R_{p}C_{p}E/[((R_{p} + R_{p})C_{p} + R_{p}C_{p}(2R_{p} + R_{p}))
\]

(20)

Substituting (10) into (19), $V_{dc,ss}$ must also satisfy the condition

\[
V_{dc,ss} > 0.5E
\]

(21)

Upon closer examination it is noted that the following inequality relationship is always valid,

\[
(R_{p} + R_{p})C_{p} + R_{p}C_{p}(2R_{p} + R_{p}) > 2R_{p}C_{p}
\]

(22)

Hence, one can conclude once (21) is satisfied, (20) would be satisfied automatically.

Under battery discharge mode, $\Delta P > 0$. From (11), it can be determined that indeed, $V_{dc,ss} > 0.5E$. Hence, (21) is always satisfied. Thus the buffer system is always stable and $v_{dc}$ will settle to a constant value following a step change $\Delta P$.

Furthermore, one can also examine the characteristic equation of (16) to obtain the damping ratio $\zeta$ where

\[
\zeta = 0.5(\alpha - \beta)/\sqrt{-\alpha\beta - \gamma}
\]

Substituting (17) into the last expression and since $E = V_{dc,ss}$, $\zeta$ can be expressed in terms of $R_{p}$, $R_{p}$ and $C_{p}$ viz

\[
\zeta = 0.5(R_{p} + R_{p}C_{p})/\sqrt{R_{p}^{2}C_{p}^{2}}
\]

(23)

From (22), the following inequality is obtained

\[
(R_{p} + R_{p})C_{p} + R_{p}C_{p}(2R_{p} + R_{p}) > 2R_{p}C_{p}
\]

Thus, $\zeta > 1$. It can be concluded that the buffer system is
always over-damped.

It is also possible to quantify how each of the battery parameters affects $\zeta$. For example, by partial differentiating (23) with respect to $R_t$, one obtains

$$\frac{\partial \zeta}{\partial R_t} = \left( R_p C - R_p C - R_p C_g \right) \left( 4 R_p \sqrt{R_p C_p C_g} \right)$$  \hspace{1cm} \text{(24)}

Since $C_p$ is of the order of F but $C$ is of the order of mF, the term $R_p C$ can be ignored. Thus $R_p C_p >> R_p C$. Therefore (24) can be simplified to yield

$$\frac{\partial \zeta}{\partial R_t} = -R_p C_p \left( 4 R_p \sqrt{R_p C_p C_g} \right)$$  \hspace{1cm} \text{(25)}

The last sensitivity function has a negative value which indicates that with an increase in $R_t$ would cause a decrease in the damping ratio of the system.

Similarly, the same approach can be applied to the study of the sensitivity of $\zeta$ to $R_p$ and $C_p$ to obtain

$$\frac{\partial \zeta}{\partial R_p} = \left( R_p C + R_p C - R_p C_g \right) \left( 4 R_p \sqrt{R_p C_p C_g} \right)$$  \hspace{1cm} \text{(26)}

$$\frac{\partial \zeta}{\partial C_p} = \left( R_p C_p - R_p C - R_p C_g \right) \left( 4 C_p \sqrt{R_p C_p C_g} \right)$$  \hspace{1cm} \text{(27)}

Both sensitivity functions have positive values. It indicates that $\zeta$ increases with $R_p$ or $C_p$.

Finally, the characteristic equation shows that there are two real negative roots

$$s_1 = 0.5(\alpha - \beta - \sqrt{(\alpha + \beta)^2 + 4\gamma})$$

$$s_2 = 0.5(\alpha - \beta + \sqrt{(\alpha + \beta)^2 + 4\gamma})$$  \hspace{1cm} \text{(28)}

Upon closer examination, it is noted that $\alpha > 0$, $\beta < 0$ and $\gamma > 0$. Hence it can be concluded from (28) that $s_1 << s_2$ and the dynamic performance of the system is primarily dominated by the pole $s_1$.

From [7, 11], it is shown that $R_t$, $R_p$, and $C_p$ vary with the discharge current. From the data shown in [11] for example, one can obtain the values of $R_t$, $R_p$, and $C_p$ and from which the damping ratio $\zeta$ and dominant pole $s_1$ variations with the discharge current can be determined. Typical results are shown in Fig. 6. In this example, one finds that $\zeta$ reaches its maximum value at a discharge current of some 153 A before it progressively decreases as the current increases. The dominant pole changes little as the discharge current increases to 153 A but decreases greatly with further increment of the current.

In the study of buffer system operation, one should therefore select the battery condition which will result in the highest damping ratio and smallest $s_1$ as the worst operating condition. This is because during sag, a higher value of the damping ratio corresponds to a buffer system with slower response characteristic. In Fig. 6, for example, the most strenuous load ride-through condition would correspond to battery discharge current of about 153 A. Hence, by designing the buffer to provide load ride-through under this most strenuous condition, improved and smoother ride-through under other discharge current condition can be guaranteed.

IV. SIMULATION RESULTS

To verify the validity of the operation scheme proposed in this paper, a power buffer model based on 0 for a 50-Hz 415 V system was built using Matlab/Simulink platform. The parameters used in the simulations are shown in Table I.

| $V_p$ | $R_{dc(1000A)}$ | $R_{dc(153A)}$ | $R_{dc(1000A)}$ | $R_{dc(153A)}$ |
|-------|----------------|----------------|----------------|----------------|
| 0.5V  | 61.33 m$\Omega$| 0.072$\Omega$  | 0.216$\Omega$  | 0.461$\Omega$  |
| $R$   | 0.97 m$\Omega$ | 1.39 F         | 6.94 F         |
| $L$   | 10 mF          | 864 V          | $P_l$          |
|       | 100 kW         |

Under pre-sag condition, the dc-link voltage is maintained at 859 V at the modulation index of 0.79. A constant power load of 100 kW is connected to the buffer. Incidents of 10-cycles upstream unbalanced faults are used to study the performance of the buffer system. The data of the buffer system is taken from [2] while that of the battery is from [11].

Due to space reason, only a sample of the simulation results will be included here. The case shown is pertaining to an unbalanced voltage sag which has resulted in 80% positive phase sequence plus 20% negative phase sequence components buffer terminal voltage. The control method of the power buffer is switched from constant power mode to constant impedance mode after the sag is confirmed, 2 ms from sag initiation. The simulation results are shown in Fig. 7.

![Fig. 6 Damping ratio and dominant pole versus battery discharge current.](image-url)
sag voltage. The buffer current overshoot observed in Fig. 7(c) is caused by the controller mode change and the switching in of the battery following the sag occurrence. The 2 ms delay assumed between the instance of the detection of fault and when the buffer control mode change and the battery switch-in has contributed toward the current transient. The transient current reaches some 25% above its pre-sag value for a very short duration. Therefore, the switching device within the buffer has to be rated to carry this transient current momentarily.

Figs. 7 (d) and (e) show the variations of input real- and reactive-powers from the upstream system into the buffer and the real power supplied by the battery, respectively. It can be seen from Fig. 7(d) that the real power supplied by the upstream is reduced to 64 kW or 0.64 p.u. of the nominal value, over the sag period, and that the input reactive power at the PCC is controlled to be zero pre- and post-sag in order to satisfy the UPF operation. From Figs. 7 (d) and (e) one also finds that the real power supplied by the upstream system during pre-fault duration meets the load demand of 100 kW and the combined power supplied by the utility and the battery during sag is maintained at 100 kW, the mismatch power being supplied by the battery energy storage system.

Finally, to verify the influence of the battery parameters on the transient performance of buffer system, two sets of battery parameters corresponding to different discharge current conditions have been used in the simulation. In this example, the same battery used in obtaining Fig. 6 has been assumed herewith. Fig. 7(f) compare the $V_{dc}$ response corresponding to discharge current of 1000 A and that of 153 A. One notes that the response of the latter case, as depicted with dotted line, is less well-damped than that of the higher discharge current. This verifies the finding described in Sub-section III.C.

V. CONCLUSIONS

A new scheme for the design and operation of power buffer is proposed. Under normal network condition, the buffer is to operate under constant power mode. When voltage sag occurs, the buffer is switched into constant impedance mode, so as to mitigate the negative impact of the constant load on voltage stability of the system. The mismatch power between the upstream source and that demanded by the load during the sag is supplied by the battery bank connected to the buffer dc-link. Voltage stability of the power system is therefore enhanced. Furthermore, analytical expressions governing the load ride-through capability and the battery state-of-discharge have been derived. Through an analysis of the buffer-battery transient response characteristic, the most onerous condition under which load ride-through can be achieved has been identified. The steady state and transient performances of the proposed buffer system are verified through simulation. The results have demonstrated the effectiveness of the proposed scheme in mitigating voltage instability due to disturbances occurring in the upstream supply system.

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