A Reconfigurable Convolution-in-Pixel CMOS Image Sensor Architecture

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Abstract—The separation of the data capture and analysis in modern vision systems has led to a massive amount of data transfer between the end devices and cloud computers, resulting in long latency, slow response, and high power consumption. Efficient hardware architectures are under focused development to enable Artificial Intelligence (AI) at the resource-limited end sensing devices. One of the most promising solutions is to enable Processing-in-Pixel (PIP) scheme. However, the conventional schemes suffer from the low fill-factor issue. This paper proposes a PIP based CMOS sensor architecture, which allows convolution operation before the column readout circuit to significantly improve the image reading speed with much lower power consumption. The simulation results show that the proposed architecture could support the computing efficiency up to 11.65 TOPS/W at the 8-bit weight configuration, which is three times as high as the conventional schemes. The transistors required for each pixel are only 2.5T, significantly improving the fill-factor.

Index Terms—processing-in-pixel, visual perception, convolutional neural network, CMOS image sensor.

I. INTRODUCTION

WITH the rapid development of image sensors and computer vision, the machines now can “see” and “understand” the visual world. Among various artificial neural networks, Convolutional Neural Network (CNN) has become dominant in various computer vision tasks and is attracting interest across a variety of domains, including object detection [1], face recognition [2], video compression [3], motion transfer [4], etc.

Although CNN has significantly improved visual systems’ performance, they consume enormous operations and huge storage space, making it difficult for end devices to complete the computation independently. Therefore, data capture and analysis are separately carried out in modern vision systems by sensing devices and cloud computers, respectively. A tremendous amount of data transfer leads to a long delay, slow response, and high power consumption [5]. Moreover, in many vision applications, the systems have to work continuously for monitoring or anomaly detection, i.e., surveillance cameras. The low information density has seriously wasted communication bandwidth, data storage, and computing resource.

Fig. 1. The first layer of CNN is performed by PIP CMOS image sensor and the rest is done with DLA.

To improve the efficiency of modern vision systems, researchers are focusing on reducing the readout power consumption or data density of sensors [6]–[11]. One of the most promising methods is to enable the computing at the sensing units, which has been intensively studied for with traditional algorithms. For example, [12] computes the difference between the new pixel value and the previous value stored on the in-pixel analog memory to detect motion events, and locates the objects by on-chip computing circuits. [13] adopts a Digital Pixel Sensor Array which has memory, readout circuits, and ADC in each pixel to perform row-parallel motion feature extraction. In-sensor computing with CNN has similar ideas. Computing CMOS Image Sensors (CIS) for CNN can be divided into three categories: (1) Processing-Near-Sensor (PNS), (2) Processing-In-Sensor (PIS), and (3) Processing-in-Pixel (PIP). The PNS architecture utilizes on-chip Deep Learning Accelerators (DLA) to shorten the physical distance between the processor and the image sensor [14]–[16]. The PIS architecture is proposed to reduce the data transfer distance, read operations, and analog-to-digital conversions. For example, Redeye performs several layers of CNN computing in CIS by additional analog arithmetic circuits before readout, saving 85% energy due to the reduced read operations [17]. However, it needs many analog capacitors for data storage, leading to a large area overhead and low computational efficiency. PIP is a fully integrated architecture to enable sensing and computing simultaneously. However, they need complicated pixel circuits, which lead to excessive area and power consumption [18], [19].

The convolution operation of the first layer is usually the performance bottleneck in various acceleration algorithms for the following reasons. The first reason is the limited number
of input channels and parameters in the first layer, leading to the challenge in pruning or quantification. For example, the pruning in [20] and quantification in [21] leave the weight of the first layer unchanged, because it is very sensitive to the accuracy of the network. To support the entire network, DLA must be designed in accordance with the requirements of every layer, leading to the hardware complexity and the computing inefficiency. Furthermore, there are many differences between the structure of the first layer and the subsequent layers, so the computing resources cannot be effectively utilized. The PIP architecture is a possible solution that performs the computing of the first layer while sensing with high efficiency.

Based on the above reasons, we propose a novel PIP architecture as shown in Fig. 1 which moves the operations of the first layer to the sensor to improve the resource utilization and computing efficiency of the DLAs. The proposed PIP architecture can enable highly efficient convolution computation in pixels to improve both fill-factor and computing efficiency. The Multiply-accumulate (MAC) operation is achieved by Pulse Width Modulation (PWM) and pixel splicing. The entire pixel array allows massive parallel convolution operations, generating one complete output feature map in four steps when the stride is two, and the filter size is $3 \times 3 \times 3$. Our proposed architecture could also support 60 frames and $128 \times 128$ resolution when the output channel size is 64. Early works such as [12] and [13] only support traditional algorithms and some PIP architectures such as [22] and [23] only support Binary Neural Networks, while our proposed scheme can support various convolution kernels via the proposed “kernel splicing“ method. The projected computational efficiency can be as high as 11.65 TOPS/W, which is three times higher than that in the reported literature [14], [22]–[25].

The rest of this paper is organized as follows: Section II presents the related works. Section III introduces the detailed design of our proposed scheme, including the overview architecture, the pixel circuit, the MAC operation, array convolution, and the implementation of other convolution kernel sizes. Section IV analyzes the simulation results. Finally, the conclusion is drawn in Section V.

II. RELATED WORK

Fig. 2 shows the block diagram of different architectures, including traditional architecture, PNS, PIS, and PIP.

**Traditional architecture (Fig. 2(a)).** As shown in [26], the data capture and data analysis in traditional schemes are usually done in the CIS and server, respectively. As a result, the majority of time and energy is consumed by data transfer. New visual systems should be developed to reduce response time and energy consumption.

**PNS architecture (Fig. 2(b)).** [27] proposed a stacked, backside-illuminated CIS with a Digital Signal Processor (DSP) dedicated to CNN computation. In [28], the signals are quantized by the ramp Analog to Digital Converters (ADCs) and then computed by the on-chip stochastic-binary convolutional neural network processor. Compared with the traditional architecture shown in Fig. 2(a), PNS architectures reduce the energy consumption of data movement. However, the energy consumed by the data readout and quantization is still not optimized.

**PIS architecture (Fig. 2(c)).** In PIS architectures, the computing units are moved to the place before ADC to reduce quantization frequency. Unlike PNS, the computing in PIS is usually done in the analog domain. The CIS in [23] can realize a maximum $5 \times 5$ kernel-readout with a minimum of one stride step for convolution operations. Analog processing units directly process the readout signals without ADCs. In [29], input images are captured in the current mode and transferred to the in-sensor analog computing circuit. However, both schemes only support binary neural networks.

**PIP architecture (Fig. 2(d)).** In PIP architectures, the computing units are integrated with the pixel array. [24] adopted a linear-response PWM pixel to provide a PWM signal for analog-domain convolution. The weights for multiplication are achieved by adjusting the current level and the integral time based on the pixel-signal pulse width. Meanwhile, accumulation is implemented by the current integration. However, the current level is generated by Digital-to-Analog Converter (DACs) according to the weights, which leads to extra power consumption. [18] adopted a pixel processor array-based vision sensor called SCAMP-5. Each pixel contains 13 digital registers and seven analog memory registers to achieve various operations. [22] proposed a dual-mode PIS architecture called MACSen, which has many SRAM cells and computation cells in each unit of the array. Both schemes suffer from a large pixel area and a low fill-factor.

New materials and devices are also developed for PIP architectures to improve the fill-factor. [30] proposed a $WSe_2$ two-dimensional (2D) material neural network image sensor, which uses a 2D semiconductor photodiode array to store the synaptic weights of the network. However, changing the photosensitivity of the photodiode may need additional DACs.
for each pixel to enable massive parallel computing.

**Mixed architecture** It’s usually difficult to conduct all computing tasks with only PIS or PIP architectures. Mixed schemes are thus proposed to achieve the entire neural network computing. In [31], an analog computing circuit is always-on to achieve face detection before ADCs. When faces are detected, the on-chip DLA performs the computing for face recognition in the digital domain, which can be described as a PIS + PNS scheme. [32] fabricated a sensor based on $WSe_2/h – BNIa_2O_3$ van der Waals heterostructure to emulate the retinal function of simultaneously sensing and processing an image. An in-memory computing unit is added after the sensor to make up the PIP + PNS scheme.

### III. Proposed Architecture

This section describes the detailed design of our proposed PIP architecture, as shown in Fig. 5. The MAC operation is achieved by PWM and pixel splicing, significantly improving the pixel density and computing efficiency. The convolution operations are realized by reconfigurable switching at the array level, allowing massive parallel computing for high performance. The architecture supports the first layer of CNN, which has a low acceleration ratio due to small input channels and large feature maps. It is also very sensitive to pruning [20] and quantization [21]. The proposed CIS can work in the Traditional mode to output the raw image.

#### A. Pixel Circuit and MAC Operation

As shown in Fig. 3(a), the digital circuit generates the control signals for the pixel array. The detailed designs of the pixel array and pixel circuit are illustrated in Fig. 3(b) and (c), respectively. The convlink wires (shown as green lines) connect adjacent pixel units with splicing transistors in both row and column directions. Each column readout wire (shown as red lines) connects each column of pixel units to a Sample and Hold (S/H) circuit and column ADC, which are the same as traditional CIS. Fig. 3(c) shows the circuit of a pixel unit containing four pixels. Four exposure control transistors $w_1$ - $w_4$ are connected to a shared FD node. Two reset transistors $RST_x$ and $RST_y$, a source follower $SF$, and a row select transistor $sel$ are shared by four adjacent pixels representing RGGB channels. Two splicing transistors $conv_{out,x}$ and $conv_{out,y}$ control the connection of the convlink wires to the adjacent pixel units in the row direction and column direction, respectively. There are 10 transistors in total for four photodiodes in a pixel unit, and thus each pixel contains 2.5 transistors (2.5T) on average.

Fig. 4 shows the computing flow of the MAC operation with the proposed PIP architecture. The multiplication of photocurrent and weights is realized by controlling the exposure time of photodiodes in each pixel unit. The exposure time of photodiodes is modulated by the weight (8 bit) in the convolution kernel. Pixel splicing method links the FD nodes and averages the multiplication results, thus realizes the accumulation.

Fig. 5 shows the simplified schematic of the proposed pixel in two different modes. Both Traditional and Computing modes include reset stage, exposure stage, and readout stage. The working mechanism of the Traditional mode is the same as the conventional 1.75T pixel array as shown in Fig. 5(a)-(c) and $RST_y$ is set to low to hand over the reset control to $RST_x$. The switch between Computing mode and Traditional mode can adopt an event-driven mechanism. When the target object is identified, the CIS can be switched to the Traditional mode to output the complete raw image.

The timing diagram of the Computing mode is shown in Fig. 6 which only contains four pixels for simplicity. A detailed description of each stage in exposure mode is provided as follows:

1) : In the RESET stage, as shown in Fig. 5(a), transistors $RST_x$, $RST_y$, and $w_1-w_4$ are turned on to reset the potential of the FD node and photodiodes to Vdd. For a Silicon PN photodiode, the rise time is about 5-10 ns [33], which is shorter than our reset time (100 ns). Thus, the photodiode is saturated before the integration begins.

2) : The EXPOSURE stage is started after the RESET stage when $RST$ is de-asserted, as shown in Fig. 5(d). In this stage, the control pulses of exposure signals $w_1-w_4$ are modulated by the weight. The exposure time $t_4$ is proportional to the weight value $w_4$. Assuming that the convolution kernel size is $r \times r$, one of the MAC operation results can be obtained by connecting $r^2$ adjacent pixel units with the convlink wires. We assume $r = 3$ as shown in Fig. 5(d). The circuit of each pixel unit can be simplified as the FD node connected in parallel with an AC current source. With the convlink wires, the nine FD nodes of the adjacent pixel units and nine AC current sources are connected in parallel. Since the photocurrent $I_t$ is unchanged in a short period, the charge $Q$ stored on each of these FD nodes can be expressed as

$$Q = CU_{rst} - \sum_{i=1}^{r^2} (I_i + I_{dc})k w_i$$

(1)

where $k$ is the exposure constant, adjusted by the software according to the external light intensity. $I_{dc}$ is the dark current and $C$ is the capacitance of the FD node. Thus, the charge $Q$ on each FD node represents the average of the products of the photocurrent $I_t$ and the corresponding weight value $w_i$ in the convolution kernel. The potential on FD nodes $U_{conv}$ can be expressed as

$$U_{conv} = U_{rst} - \frac{k}{r^2C} \left( \sum_{i=1}^{r^2} I_i w_i \right) - I_{dc} \frac{1}{r^2} \sum_{i=1}^{r^2} w_i$$

(2)

3) : After the exposure, it is the READOUT stage when $sel$ is asserted, as shown in Fig. 5(e). The weight precision of the convolution kernel used in the system is 8-bit. That is, the weight size of the convolution kernel ranges from -128 to +127. The positive and negative weights of the convolution kernel can be achieved by subtracting two consecutive exposures, as shown in Fig. 6. As $w_1$ and $w_2$ are positive, they are enabled in the first exposure period. The negative $w_3$ and $w_4$ are enabled in the second exposure period. The digital circuits subtract the two readout operations in Fig. 6 after the ADCs, which is expressed as...
$I_{ph}(A) \times \text{Exposure time(s)} = \text{Charge(C)}$

$\sum Q/(nC) = \Delta U(V)$

$U = U^- - U^+ = \frac{k}{rC} (\sum I_i w_i^T - \sum I_i w_i^- + I_{dc} \sum w_i)$

where $\frac{k}{rC}$ is a known constant, $\sum w_i$ is statistically close to zero and $I_{dc}$ is usually much smaller than $I_i$. The voltage $U_{conv}$ represents the sum of the $r^2$ multiplication results, thus achieving MAC operation in-pixel level.

### B. Convolution Operation in Array

After introducing the basic idea of the MAC operation, this section gives a detailed introduction to the overall architecture of the system and the sliding convolution on the entire pixel array.

As can be seen from Fig. 3, the most fundamental component of the pixel array is a pixel unit containing four pixels. Splicing transistors separate the adjacent pixel units. Each column of pixel units includes a column S/H circuit and a column ADC outside the array, which can read the convolution results and convert them into digital signals.

The flow of convolution operation in the array is shown in Fig. 7. In the following example, we assume that the convolution kernel size is $3 \times 3$ and the stride is 2. In Fig. 7, each square represents a pixel unit. The $3 \times 3$ connected active pixel units are defined as a tile. The horizontal and vertical dash lines mean the break of convlink between the tiles. The entire array can be divided into several independent convolution tiles. The MAC operations are enabled simultaneously in all active tiles in each step. We defined three rows of tiles as a group.

As stated in the previous section, the MAC operation can be achieved by connecting the convlink wires of all pixel units...
A group contains 3 rows of tiles. 

Readout a group at once. (The readout path of other tiles are not drawn)

The readout time of an entire step is \( (n_{rd} - 1)T_{rd} \), where \( T_{rd} \) is the readout time for each tile and \( n_{rd} \) is the number of the readout operations in each step. If the reset interval is \( T_{rst} \), and the maximum exposure time is \( T_{expo} \), the reset and exposure stages need to be finished before the next readout operation,

\[
(n_{rd} - 1)T_{rd} > T_{rst} + T_{expo}
\]

As shown in Fig. 11, the exposure and readout sequence of the proposed architecture is similar to Interlaced Readout method [34], which divides the readout time for one frame into \( K \) sub-images. Compared with the conventional Rolling Shutter as shown in Fig. 11 (a), the Interlaced Readout in Fig. 11 (b) reduces the skew and the time lag in these sub-images \( K \) times to support high speed photography, at the cost of the reduction of vertical spatial resolution. Our proposed architecture divides the computing of one frame into 8 groups (each step exposures 2 times for the processing of positive or negative weights) as shown in Fig. 11 (c), which improves the readout speed and resource utilization.
C. Implementation of Different Convolution Kernel Size

We propose a “kernel splicing” method to support different kernel sizes with the same wiring method. As shown in Fig. 12(a), 5×5 convolution operation can be realized by two 5×3 convolution operations. The 5×3 convolution operation is similar to the 3×3 convolution operation. The main difference is that the convlink wires link 5×3 pixel units together in the 5×3 convolution operation. The number of steps is changed to 6 instead of 4 because three steps are required in the column direction to avoid overlapping. Each group still has 3 rows of tiles during readout operation. Another two examples for 7×7 and 9×9 kernel sizes are shown in Fig. 12(b) and (c), respectively. In this way, different kernel sizes can be realized by using the same hardware circuits.

Assuming the kernel size is r×r and the stride is s, the total number of steps is \( \frac{r+1}{s} (r - 1) \), where the ratio \( \frac{r+1}{s} \) needs to round up to an integer if necessary. The equivalent exposure times for each channel are \( \frac{2(r+1)}{s} + 1 \). For a fixed height of the pixel array H (128 in our case), the total number of output rows in each step is \( \frac{H}{r+1} \). Since each readout operation contains three output rows, the minimum ADC conversion rate can be calculated by

\[
T_{ADC(min)} = \frac{2 \cdot nH}{3s} \tag{5}
\]
Algorithm 1 Array Convolution Operation

1: for each step (1-4) do
2:   Divide the array into independent tiles.
3:   for positive and negative weights(+-.) do
4:     for $j = 1$ to $n_{rd}$ (the group serial number) do
5:       Read the results of the three rows of tiles
6:       via three column readout circuits, respectively.
7:       j + 1, j + 2...
8:     end for
9:   end for
10: end for

where $f$ is the frame rate and $n$ is the number of channels. The minimum conversion rate of ADC is proportional to the 
frame rate $f$, the channel number $n$, and the kernel size $r$. It is 
 inversely proportional to the stride $s$.

The actual frame rate $f_{real}$ is defined as the product of frame rate and the output channel number $f \times n$. With a fixed 
maximum exposure time $T_{expo}$, the maximum frame rate can be calculated by

$$f_{real(max)} = \frac{s}{2(r+1)+s(r-1)T_{expo}}$$  (6)

The maximum frame rates and the minimum ADC conversion 
 rates at different kernel sizes are tabulated in Table I. For example, the resolution is $128 \times 128$, the stride is 2, the kernel 
size is $3 \times 3$, the stride is 2, and the output channel number 
is 64, the maximum exposure time is 26.04 us. $f_{ADC(min)}$ is based on $f_{real(max)}$ in each condition. When kernel size 
 increases, the conversion rate of ADC will decrease because both actual frame rate and readout operation frequency 
 decrease. As a result, the maximum frame rate decreases.

IV. Simulation Results

Our proposed architecture was implemented with TowerJazz 0.18 um CMOS process. The circuits are simulated with Cadence Virtuoso and Spectre. An analytic model taken from

Fig. 11. The exposure and readout sequence diagram of (a) conventional Rolling Shutter, (b) Interlaced Readout, (c) Proposed Readout.

Fig. 12. The convolution implementations of kernel splitting. The convolution kernel size is (a) 5×5, (b) 7×7, and (c) 9×9.
TABLE I
RATE CALCULATION WITH DIFFERENT KERNEL SIZES.

| operation condition | minimum ADC conversion rate | maximum real frame rate |
|---------------------|-----------------------------|------------------------|
| 3×3                 | 327.68 KHz                  | 3840                   |
| 5×5 (splicing)      | 234.06 KHz                  | 1371                   |
| 7×7 (splicing)      | 182.04 KHz                  | 711                    |
| 9×9 (splicing)      | 148.95 KHz                  | 436                    |

Fig. 13. The layout design of the proposed pixel.

Fig. 14. The maximum frame rate of proposed CIS working in Computing mode and Traditional mode under different illumination conditions.

The ADC conversion rate is 330 KHz. When the light intensity is low, the exposure time is the main factor to determine the maximum frame rate. When the light intensity is high enough, the ADC frequency limits the maximum frame rate. The frame rate of the proposed CIS in Traditional mode is the same as a conventional 1.75T CIS. The proposed Computing mode requires eight times the exposure time of conventional 1.75T CIS for the convolution operation but reduces the readout density. With strong illumination, our proposed CIS in Computing mode outperforms the conventional 1.75T CIS because of the lower readout density.

A. Linearity Simulation

Although FD node behaves electrically as a capacitor, it is quite different from a real capacitor. That is, the non-idealities of the FD node need to be considered in the simulation. Thus, we use a resistor (R = 8.07e15 Ω, estimated based on the data in [36]) connected in parallel with the FD node to simulate the leakage of the FD node.

Fig. 15 (a) and (b) show the readout voltage $U_{out}$ under different weight and illuminance, respectively. Linear fitting results of both figures show that the $R^2$ are all above 0.98, indicating high linearity and accuracy of the proposed architecture.

B. Performance Analysis

The power consumption and performance comparison under different conditions are tabulated in Table II. The illumination is about 1500 lux. The array size for all situations is 128×128, and the number of output channels is 64. The computing results with 5×5 and 7×7 kernels are estimated based on the kernel splicing. The FoM (pJ/pixel/frame) presents the energy consumed per frame (each channel counts once) per pixel. The computing efficiency (TOPS/W) shows the computing amount divided by power consumption. The total computing amount is calculated as the product of the size of the output array, the number of input channels, the number of output channels, the frame rate, and the computing amount for one kernel. When the kernel size is 3×3, each kernel needs 18 OPs, and the total amount is

$$64 \times 64 \times 4 \times 64 \times 60 \times 18 = 1132462080 \text{ OPs.}$$

The power consumption of ADCs is calculated according to the data in [37]. Advanced CMOS technology will significantly reduce the power consumption of ADC.
Table II shows that the power consumption of our proposed sensor circuit is determined by the frame rate and the convolution kernel size. When the convolution kernel size keeps constant, the power consumption increases with the frame rate. With the same frame rate, the larger convolution kernel size leads to higher power consumption.

Computational efficiency (TOPS/W) changes remarkably in different conditions. The power consumption mainly comes from three parts: the convolution operation, the readout circuit, and the column ADCs. Though the number of convolution operations and the number of readouts vary in the same proportion, the cost of ADCs remains unchanged, leading to increased computational efficiency when the amount of computation increases. For example, the efficiency is 4.62 TOPS/W and the frame rate is 60 fps when the kernel size is 3×3 and the stride is 2. It is increased to 11.65 TOPS/W when the kernel size is 7×7.

FoM (pJ/pixel/frame) increases with the amount of computation but decreases with frame rate because of the same reason as the computational efficiency. It mainly represents the influence of convolution kernel size on power consumption. The increase in convolution kernel size will lead to a rise in
the amount of computation and power consumption.

The change of stride will lead to different amount of computation. If the stride is doubled, the amount of computation and readout times will be reduced to a quarter, which leads to a decrease in power consumption and FoM.

As shown in Table III, the computing efficiency of our proposed architecture is up to 11.65 TOPS/W, which is three times as high as the latest in-sensor computing schemes. Since our proposed architecture integrates MAC operation with the pixel exposure, no additional analog computing circuit is used, leading to this high efficiency. The energy consumption of a single frame of figure has been estimated when a 7×7 kernel is adopted and stride is 2. A traditional CIS + DLA vision system consumes about 133.74 μJ (based on [9], [38]) and the proposed scheme costs only 8.82 μJ, which shows a 15 times reduction of the energy consumption. The energy consumption of the CIS is estimated based on the scaling of resolution and frame rate, and the energy consumption of the DLA is estimated by the product of the computational efficiency of the DLA and the computing amount.

C. Noise Analysis

Operations in the analog domain are affected by undesirable factors such as noise and variations. In this section, we analyze the robustness of our proposed circuits.

The temporal noise and Fixed Pattern Noise (FPN) are the most fundamental nonideality in CIS [26]. The sample noise at the end of integration can be expressed as the sum of: (1) integrated shot noise $Q_{\text{shot}}$, (2) reset noise $Q_{\text{reset}}$, (3) readout circuit noise $Q_{\text{read}}$ due to readout device thermal and flicker (or 1/f) noise, (4) offset FPN due to device mismatches $Q_{\text{FPN}}$, (5) offset FPN due to dark current variation, commonly referred to as dark signal nonuniformity (DSNU), and (6) gain FPN, commonly referred to as PRNU. For a conventional CIS with a CDS operation, the total noise can be estimated by

$$S_2 - S_1 = Q_{\text{shot}} - Q_{\text{1,read}} + Q_{\text{2,read}} + Q_{\text{DSNU}} + Q_{\text{PRNU}}$$

in which the reset noise and the offset FPN are suppressed but the read noise power is increased.

In our proposed scheme, the CIS performs two exposures and readouts for positive and negative weights, respectively. After the subtract operation by the digital circuits, the noise can be estimated by

$$S_p - S_n = (Q_{p,\text{shot}} - Q_{n,\text{shot}}) + (Q_{p,\text{reset}} - Q_{n,\text{reset}}) + (Q_{p,\text{read}} - Q_{n,\text{read}}) + (Q_{p,\text{PRNU}} - Q_{n,\text{PRNU}})$$

in which the offset FPN are suppressed, and most of low frequency noise will be reduced due to the short time interval between two readout (less than 32 us, about 30 KHz).

Therefore, the proposed CIS does not add additional noise. In addition, the MAC operation on the pixel array may benefit the SNR, in the case of a 3×3 kernel this can be explained as

$$\text{noise} = E[\left(\frac{\sum n_{\text{all}}}{9}\right)^2] = \frac{1}{9^2}D(\sum n_{\text{all}}) = \frac{\sigma^2}{9}$$

SNR = $\frac{\text{power}}{\text{noise}} = \frac{9\text{power}}{\sigma^2}$

in which $n_{\text{all}}$ represents the total noise.

D. Algorithm Robustness

Through network simulation with Cifar-10 [39] dataset and Resnet-18, the accuracy of CNN changes with SNR or mismatch as shown in Fig. 16. As the proposed CIS only supports 1st-layer CNN, the rest of the computation is
performed externally. Three normal distributions with different variances of the equivalent capacitors are used to simulate the mismatch, and the distributions are shown in Fig. 16. The results only have a negligible accuracy loss when SNR is more than 40 dB. The typical SNR value for CIS is 40 dB - 60 dB [22]. Fig. 17 shows a comparison of the input RGGB figure and the output feature map of the 1-st layer CNN performed by CPU or the proposed CIS. The mean RMS error for the 1-st layer output of the proposed CIS is shown in Table. IV. As expected with the reduction in the SNR, the RMS error increases.

Because the first layer of CNN is sensitive to pruning and quantization, the conventional network model compression algorithms often leave the first layer untouched. For example, most layers may perform a 4-bit quantization, but the 1-st layer needs at least 8-bit to keep accuracy. In this case, DLAs must support 8-bit computing to support the entire net, which leads to extra costs and reduction of system efficiency. Moreover, due to the small number of input channels, DLAs’ PEs are often not fully utilized for the first layer. Therefore, this design can improve the computational efficiency of the subsequent DLAs, leading to higher performance of the entire machine vision system.

E. Performance under Other Resolutions

In this subsection, we discuss the power consumption, frame rate, and Efficiency of the architecture under different resolutions to show the scalability.

![Image](image_url)

**Fig. 17.** (a) An input test figure (with RGGB pattern). (b) A channel of the output feature map of the 1-st layer CNN performed by the proposed CIS and (c) by CPU.

| SNR   | 60dB | 40dB | 20dB | 0dB  |
|-------|------|------|------|------|
| 5% deviation | 6.78e-3 | 7.12e-3 | 2.25e-2 | 1.77e-1 |
| 10% deviation | 1.13e-2 | 1.15e-2 | 2.43e-2 | 1.77e-1 |
| 20% deviation | 1.80e-2 | 1.82e-2 | 2.80e-2 | 1.78e-1 |

**TABLE IV**

**MEAN RMS ERROR FOR THE 1-ST LAYER OUTPUT IN DIFFERENT CONDITION**

![Image](image_url)

**Fig. 18.** The power consumption under different resolution. The illumination is about 1500 lux.

| resolution | minimum ADC frequency |
|------------|-----------------------|
| 1920×1080  | 2.76 MHz              |
| 1280×720   | 1.84 MHz              |
| 720×480    | 1.23 MHz              |
| 128×128    | 327.68 KHz            |
| 32×32      | 81.92 KHz             |

**TABLE V**

**RATe CALCULATION UNDER DIFFERENT RESOLUTIONS.**

1) **Power Consumption:** Fig. 18 shows the power consumption of the proposed architecture under different resolutions. The power consumption is basically proportional to the amount of calculation thus increases with the resolution. Thus, the computation efficiency is independent of the resolution.

2) **Maximum Frame Rate:** According to Eq. 5, the maximum frame rate limited by exposure time is independent of resolution. As shown in Eq. 5, the minimum ADC frequency is proportional to the height of the array. The minimum ADC frequency under other resolutions is tabulated in Table V. The operation condition is all set to 3×3 kernel and stride is 2.
V. CONCLUSION

In this work, a PIP architecture has been proposed to perform the first layer convolution operation of CNN. It supports a variety of different convolution kernel sizes and parameters. The simulation results have shown that our proposed scheme functions correctly with good linearity. When the convolution kernel is $7 \times 7$, the step size is 2, and the channel number is 64 at 60 fps, the proposed architecture consumes 529.29 uW power and has a computational efficiency up to 11.65 TOPS/W. It is suitable for application scenarios with tight requirements on power consumption, such as daily monitoring and Internet of Things (IoT) devices.

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