A low stray inductance laminated busbar for series-parallel capacitors

GUO Yannan, SUN Peng, CAI Yumeng and ZHAO Zhibin

State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources, North China Electric Power University, Beijing 102206, China

guoyannan@ncepu.edu.cn

Abstract. In the dynamic characteristics test circuit for high-voltage and high-power power electronic devices, the laminated busbar is the main connecting component. The stray inductance of the laminated busbar is one of the key factors that affect the accuracy of the dynamic characteristics. Therefore, a low stray inductance laminated busbar for series-parallel capacitors is proposed, from the perspective of reducing self inductance and increasing mutual inductance. Through finite element simulation, the result of extracting the stray inductance of the laminated busbar is 4.16nH. Compared with the most basic laminated busbar, this stray inductance is very small.

1. Introduction

Since the 21st century, with the development of power semiconductor materials and technology more and more mature, the development of power electronic devices toward the direction of high voltage and high power[1][2]. The dynamic characteristics test for power electronic devices is of great significance for their loss prediction, thermal design, power consumption evaluation, and device reliability[2]. In the dynamic characteristics test circuit of power electronic devices, DC-link capacitor plays the role of voltage stabilization and filtering, and therefore is very important components. Because the laminated busbar has the advantages of low stray inductance, strong ability to pass current, good heat dissipation and low switching noise, it is the preferred connecting component for capacitors[3]. With the development of power electronic devices toward high voltage and high power, a single capacitor usually can’t meet the voltage and capacitance needs of the test circuit at the same time. Thus it is necessary to combine capacitors in series and parallel. The series-parallel capacitors may lead to large stray inductance in the power loop of power electronic devices, which affects the accuracy of the dynamic characteristics of power electronic devices. So it is necessary to reduce the stray inductance of the laminated busbar.

The laminated busbar for series-parallel capacitors has been studied by several scholars at home and abroad. Reference [4] has adopted a circular layout of capacitors, protection circuit elements, and diodes in the IGBT short-circuit test platform to greatly reduce the stray inductance. However, it does not provide design ideas for when components are connected in series. Reference [5] proposes a laminated busbar design method when two capacitors are connected in series, but it is not applicable when more capacitors are connected in series.

In this paper, a low stray inductance laminated busbar is proposed, with taking three series and two parallel capacitors as an example. In this paper, it is proposed that not only the current path’s length but also the current path’s angle are important factors affecting the stray inductance. The finite element
simulation stray inductance extraction result of the the laminated busbar is very small. At the same time, this busbar structure is also applicable to the series-parallel capacitors.

2. Theoretical analysis

2.1. The influence of power loop’s stray inductance on the switching characteristics of SiC devices

A typical double-pulse circuit is usually used to obtain the switching characteristics of SiC MOSFET. The switching characteristics test circuit of SiC MOSFET considering the stray parameters of the power loop is shown in Figure 1[6]. It consists of SiC MOSFET, DC power supply (VDC), SiC MOSFET gate drive circuit (VG), DC-link capacitor CDC-link, load inductance Lload, the freewheeling diode SBD, the laminated busbar for connection and the stray parameters of each component.

Due to the loop stray inductance, the SiC MOSFET will experience an overshoot in the turn-off phase, which increases the turn-off loss and electrical stress of the device. During the turn-on phase of the SiC MOSFET, current overshoot for devices occurs.

The total stray inductance of the power loop includes the stray inductance Lc of the DC-Link capacitor, the stray inductance Lbus of the laminated busbar, the drain equivalent stray inductance LD (LD=LD1+LD2) of SiC MOSFET and the source equivalent stray inductance LS (LS=LS1+LS2) of SiC MOSFET. Among the total stray inductance of the power loop, Lbusbar occupies the largest proportion. In addition, the production process of specific SiC MOSFET and DC-link capacitor is mature and fixed. Therefore, Lc, LS and LD are small values, so the only part that can be changed is Lbus. So the key point of reducing the total stray inductance for the power loop is to minimize the stray inductance of the busbar.

2.2. Theoretical analysis of stray inductance of multilayer busbar

A basic laminated busbar structure consists of conductor layers, which including positive layer and negative layer, and insulating layer. Figure 2 shows the physical structure and equivalent circuit of a double-layered laminated busbar. The structural parameters of the busbar include length(l), width(w), thickness(t), and distance(d) between the two conductor layers.
The total stray inductance of the laminated busbar is not only related to the self inductance, but also related to the mutual inductance induced between the conductor layers. The calculation equation\[7]-\[8]\ for self inductance, mutual inductance and total inductance of double-layered laminated busbar are shown as follows:

\[
\begin{align*}
L_{P(N)} &= \frac{\mu}{2\pi} \left[ \ln \left( \frac{2l}{\omega + t} \right) + \frac{1}{2} - \ln \left( \frac{\omega + t}{l} \right) \right] \\
M &= \frac{\mu}{2\pi} \left[ \ln \frac{\sqrt{l^2 + t^2} + l}{t} - \sqrt{l^2 + t^2} + t \right] \\
L_{\text{total}} &= L_P + L_N \pm M
\end{align*}
\]

where \( \mu \) is the permeability, \( L_P \) and \( L_N \) are the self inductances, \( M \) is the mutual inductance, \( L_{\text{total}} \) is the total inductance.

It can be seen from the equation that the smaller the self inductance value, the larger the absolute value of the mutual inductance whose value is negative, the smaller the total stray inductance value. In terms of physical structure, the laminated busbar should be as short, wide and thin as possible, and the distance between the two conductor layers should be close\[9]\.

In practical, the laminated busbar is complex and irregular, and the current may only flow in a part of the busbar. The optimization method proposed only considering the physical structure is not comprehensive. Therefore, a more comprehensive explanation is: self inductance is mainly related to the length of the current path. The current path should be as short as possible. The mutual inductance between two conductor layers is not only related to the coupling degree, but also related to the angle between current paths. When the angle between the two current paths is an obtuse angle, the magnetic field generated by the current can be canceled, and the mutual inductance \( M \) is a negative value. The greater the angle, the more magnetic field that can be cancelled. Thus, when the mutual inductance value is negative, the coupling degree of the conductor layers should be as large as possible, and the angle of the current paths should be as large as possible.

3. A low stray inductance laminated busbar for capacitors

In this chapter, a low stray inductance laminated busbar is obtained as an example of three series and two parallel capacitors. This method is also applicable to series-parallel capacitors.

Figure 3 shows the schematic diagram of conductor layers and capacitors in the laminated busbar for three series and two parallel capacitors. The individual capacitor is a film capacitor with a capacitance of 50\( \mu \)F and a rated voltage of 900V. This capacitor is a four-terminal capacitor. The laminated busbar conductor layer is divided into four independent parts: positive layer (P layer), higher intermediate potential layer (M1 layer), lower intermediate potential layer (M2 layer), and negative layer (N layer). Besides the exclusion of capacitor connection, the busbar also connects to other parts of the circuit. The connection terminal of current flowing into and out of the laminated busbar are +Link and -Link.
Different capacitor layouts, different terminal positions, and different busbar shapes all determine different laminated busbar. Thus, this paper starts from a basic laminated busbar, and designs different laminated busbars from the point of view of decreasing the self inductance and increasing the mutual inductance of the busbar, as shown in Figures 5, 6, and 7. The current path from +Link to C1(C4), the current path from C1(C4) to C2(C5), the current path from C2(C5) to C3(C6), and the current path from C3(C6) to -Link are defined as current path a, current path b, current path c, and current path d respectively. In the figure, the current path a, the current path b, the current path c, and the current path d are illustrated with black line, white line, green line, and purple line in sequence. In order to make the image intuitive, only half of the current path through the four-terminal capacitor is drawn.

The layout of the capacitors in Busbar I is sequential, with connection terminals +Link and -Link adjacent to each other and located near capacitor C1(C4), as shown in Figure 5. In Busbar I, the length of the current path d is long, so its self inductance is the main component of the total self inductance. The current paths a and b, c and d are orthogonal respectively, so the mutual inductance between these busbar layers is small. The current paths b and c are parallel and isotropic, so the mutual inductance is positive. The coupling degree between the M1 layer and the N layer, the M2 layer and the N layer is not...
large. Although the mutual inductance is negative, the values are so small that can be ignored. Therefore, the self inductance plays a decisive role in the total stray inductance.

In order to reduce the effect of self inductance on the total stray inductance, Busbar II is proposed. For the consideration of symmetry and increasing the coupling degree of conductor layers, the connection terminals +Link and -Link are located at the center of Busbar II, as shown in Figure 6. In Busbar II, the angles between current paths a and b, current paths b and c, current paths c and d are all obtuse. Besides, the coupling degree of P layer and M1 layer, M1 layer and M2 layer, M2 layer and N layer is large. So the total mutual inductance is a negative and large value. Compared with Busbar I, the total current path of Busbar II is longer, so the total self inductance is larger. However, the negative mutual inductance greatly affects the total stray inductance, so the total stray inductance of Busbar II is much smaller than Busbar I. The symmetry of the stray inductance of different busbars has been well improved as well.

Consider further increasing mutual inductance. The layout of capacitors in Busbar III is improved sequential layout, with the capacitors of adjacent levels staggered on both sides of the connection terminal +Link (-Link), as shown in Figure 7. The angles between current paths a and b, current paths a and d, current paths b and c, current paths c and d are all obtuse. Besides, the coupling degree between P layer and M1 layer, P layer and N layer, M1 layer and M2 layer, M2 layer and N layer is large. So the total mutual inductance value is a negative and large value. Compared with Busbar II, Busbar III has a slightly larger self inductance for a slightly longer total current path. However, in Busbar III, the capacitor of adjacent levels are staggered on both sides of the connection terminal to increase the symmetry of the current path between conductor layers. The angle between the current paths of the two conductor layers with negative mutual inductance is nearly 180°, which means the current flowing into and out of the same capacitors in parallel flow in opposite directions. So the effect of mutual inductance is more significant. The negative mutual inductance cancels out the self inductance and further reduces the total stray inductance. In addition, the area of Busbar III is approximately 32% of that of Busbar II, making Busbar III compact and space efficient. This advantage will be even more pronounced for large-capacity and high-voltage capacitors.

4. Simulation validation

The finite element simulation method is used to extract the stray inductance of the above three laminated busbars. According to the actual working conditions of power electronic devices, set a current source with a frequency of 10MHz as the excitation source.

The stray inductance simulation extraction results for different laminated busbars are shown in Table 1. Busbar III increases the symmetry of the stray inductance of different current paths and increases the influence of mutual inductance on the total inductance. The total inductance is greatly reduced, which is consistent with the analysis result.

| Laminated busbars | stray inductance (nH) |
|-------------------|----------------------|
| Busbar I          | 38.29                |
| Busbar II         | 4.40                 |
| Busbar III        | 4.16                 |

5. Conclusion

This paper proposes a low stray inductance laminated busbar for series-parallel capacitors.

a) The two capacitors of adjacent potential are staggeredly distributed on both sides of input (output) terminal, which makes the current flowing into and out of the same capacitors in parallel flow in opposite directions. The laminated busbar structure increases the symmetry of the current paths, so it effectively reduces the total stray inductance.

b) The finite element simulation stray inductance extraction results of the the laminated busbar for capacitor sequential layout, circular layout, and improved sequential layout are 38.29 nH, 4.40 nH, and
4.16 nH, respectively. Although the stray inductance of the laminated busbar for improved sequential layout is not much different from that of the laminated busbar for circular layout, the area of the busbar is only 32% of the former.

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