Si and SiC Schottky diodes in smart power circuits: A comparative study by I-V-T and C-V measurements

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Abstract. In this paper we analyze a possibility of manufacturing and implementation of Schottky diodes in the smart power circuits. Three different Schottky diodes, in three different technologies, are realized in Si and SiC processes. The electrical characterizations with I-V-T and C-V measurements are done for all structures. It is shown that Si based Schottky diodes also are suitable to be integrated in the typical smart power circuits.

1. Introduction
There is increasing interest in integrating Schottky diodes in smart power integrated circuits \cite{1}. Usually MOS diodes are used in standard CMOS technologies. They have usually a non-ideal switching behavior, which brings an offset, which leads to slowly charging the power DMOS gate \cite{2}. They also have parasitic elements and relatively high leakage current. Due to the body effect in MOS structures, the output voltages of charge pumps (typical smart power circuit) with MOS diodes are lower than that of charge pumps with pn or Schottky diodes. Also MOS diodes have relatively high voltage drop which is important to be considered in cases of minimizing supply voltages.

It is difficult to integrate Schottky diode in CMOS IC’s and also there is a big influence of parasitic elements in IC. Problems of lifetime and reliability of these diodes need silicides to be included in CMOS process, which is not always possible.

Smart power circuits are mostly done on Si but also as alternative there are SiC smart power circuits \cite{3}. The properties of silicon carbide make it appropriate material for high temperature, high power and high frequency applications. In development phase, implementation of Schottky diodes in the smart power circuits needs a comparative analysis of these diodes related to the effects of surface and temperature, and materials. In order to do a comparative analysis, in this paper the current-voltage and capacitance-voltage characteristics of Si and SiC Schottky diodes are studied over a wide temperature range from 200 to 450K. The barrier height, ideality factor, series resistance, saturation current are studied related to the mechanisms of carrier transport in the presence of bulk traps and interface states. The comparative analysis of diodes made on these materials give a good overview of both technologies from the aspect of reliability and application of the Schottky diode in integrated circuits.

2. Experimental results
For experimental purposes Schottky diodes are based on n-Si with “small” (Fig 1.) and “large” surface areas Si and SiC Schottky diodes. The Schottky diodes are realized as polygonal areas with Schottky contact between metal and semiconductor. The details for test diodes are given in Table 1. Each of the test groups included 20 samples during measurements.
The current voltage characteristics of a Schottky barrier diode with series resistance $r_s$ and dominant thermionic transport mechanism, with Richardson’s constant $A^*$, is given as:

$$I = A^* T^2 \exp\left(\frac{-q\phi_B}{kT}\right) \left(\exp\left(\frac{qV - Ir_s}{nkT}\right) - 1\right) = I_s \left(\exp\left(\frac{qV - Ir_s}{nkT}\right) - 1\right)$$  \hspace{1cm} (1)$$

The typical forward I-V curves for all three test groups are presented in Fig. 2, and breakdown voltages are given in Table 2. Using I-V data at room temperature, the barrier height $\Phi_B$ is calculated from the current $I_s$, determined by an extrapolation of the log(I) versus V curve to $V=0$. The values obtained by this method are given in Table 2.

| Material                  | Meta | Area          | Bandgap (eV) | $A^*$ (A/cm²K²) | $N_D-N_A$ (cm⁻³) |
|---------------------------|------|---------------|--------------|----------------|-----------------|
| Si “large” area - type A  | Al   | 215µm*215µm  | 1.1          | 112 [5]        | 5*10¹⁷          |
| Si “small” area - type B  | Al   | 35µm*35µm    | 1.1          | 112            | 10¹⁶            |
| 4H-SiC “large” area - type C | Ti   | 190µm*190µm  | 3.2          | 146 [4]        | 8*10¹⁷          |

Under conditions: $V>> kT/q$ and $r_s I << V$, from equation (1) can be found that a plot of $\ln(I/T^2)$ versus $1/T$ at a constant forward bias voltage $V_1$, sometimes called a Richardson plot, has a slope of $-q(\phi_B - V_1/n)$ and an intercept $\ln(AA^*)$ on the vertical axis. As an illustration, the I-V-T curves, for large area Si diode, are shown in Fig. 3. The results for barrier heights obtained by the I-V-T method are also given in Table 2.

![Cross-section of a Si Schottky diode](image1.png)

**Figure 1.** Cross-section of a Si Schottky diode.

![Forward I-V characteristics of Schottky diodes](image2.png)

**Figure 2.** Forward I-V characteristics of Schottky diodes.

By measuring of diode capacitance C, and plotting $1/(C/A)^2$ versus V one obtains a curve with the slope $2/(q\varepsilon_0\varepsilon_r(N_A-N_D))$ and with the intercept on the V axis, $V_i=-V_{bi}+kT/q$. The typical curves are presented in Fig. 4. The barrier height $\Phi_B$ is calculated using barrier $V_{bi}$ for electron in semiconductor determined from the intercept voltage. The net doping density $N_D-N_A$ can be also determined from the slope.
Extraction of $r_S$ and $\Phi_B$ can be done using a function $F$, known as a Norde function [6]. The curve $F(V)$ (Fig. 5) has a minimum, which is used to determine $r_S$ and $\Phi_B$. Really, Norde’s method only well works for ideal Schottky diodes ($n=1$), and this can be the reason why the larger values for $\Phi_B$ are obtained by this method (Table 2).

![Norde plot for Si small area diode](image1.png)

![Norde plot for Si large area diode](image2.png)

![Norde plot for SiC large area diode](image3.png)

**Figure 3.** I-V-T characteristics of large Si Schottky diodes.

**Figure 4.** $(C/A)^2-V$ characteristics of Schottky diodes.

**Figure 5.** Norde plots of Schottky diodes (arrows indicates minima).

The results given in Table 2 can be discussed related to their physical meaning, and the quality and reliability aspects. Two experimental facts in the case of Si Schottky diodes: low barrier heights and ideality factors higher than 1 are in correlation. These results can be explained by an imperfect Schottky contact: local variation of barrier height, presence of thin interface oxide layer, generated new interface states, presence of traps and impurities in interface layer and bulk, imperfections of diode periphery. Following explanation can be done: impurity atoms modify interfacial dipole layer, which cause two significant effects, i.e. barrier lowering effect, and increase of ideality factor. The
traps can influence a trap-assisted electron tunneling. The presence of other transport mechanisms than the thermionic emission leads also to increase of the ideality factor. The fact that there are the imperfections in the Schottky contact means in itself the quality and reliability degradation. According to the results for barrier heights and the ideality factors, larger diode area leads to larger probability to be present the contact imperfections.

Table 2. Overview of results obtained on test diodes at ambient temperature (except for I-V-T method)

| Type   | Slope I-V | n | IS (from I-V method) | φB (V) C-V | φB (V) I-V-T | φB (V) I-V | φB (V) Norde | rs (Ω) | Vbr reverse (V) |
|--------|-----------|---|----------------------|------------|--------------|------------|-------------|-------|----------------|
| A      | 15.32     | 1.09 | 0.16μA | 0.26 | 0.22 | 0.27 | 0.73 | 425 | 42 |
| B      | 15.35     | 1.09 | 0.36pA | Not available | 0.31 | 0.38 | 1.1 | 7.8K | 21 |
| C      | 16.22     | 1.03 | 0.01fA | 1.24 | 0.48 | 1.22 | 1.34 | 116.6 | 600 |

3. Conclusion
The average barrier heights φ_B, determinated by different methods, have approximately the values of 0.25V, 0.35V and 1.23V, for Si large area, Si small area and SiC large area, respectively. φ_B is very sensitive to process induced Schottky contact imperfections. Also all methods are not suitable for all structures, due to their limitations connecting to their conditions of application. The ideality factor n > 1 and its increasing with temperature is an indicator that the contact imperfections and that the other charge transport mechanisms like tunneling and g-r induced effects can take place.

The Si diode (type B) presented here can be used as diode in charge pump circuits (CP) instead of MOS diode. The advantages of using Schottky diode are smaller leakage current, smaller voltage drop and smaller offset. Also it is important to emphasize that this diode was manufactured in standard smart power process without additional technology steps. It has to be pointed out that voltage drop on Schottky diode is (~0.3V), leading to the lower dissipation and better current capability of CP with Schottky diode than one with MOS diode.

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5. References
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