Implementation of Interface Circuit for Digital SQUID with Sub-Flux Quantum Feedback Resolution

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Abstract. Digital SQUIDs with single flux quantum (SFQ) feedback have attracted much attention because of the feasibility of realizing a wide dynamic range and high slew rate for digital magnetometers. To achieve a higher resolution, we studied a digital SQUID with sub-flux quantum feedback. We studied implementation methods for an interface circuit by considering the circuit size, power consumption and signal processing to achieve high-resolution and high-speed operation of the digital SQUID magnetometer. Assuming the decimation filter and the up/down counter implemented on a FPGA board, a 1-bit to 16-bit deserializer with an output frequency of 500 MHz could be used for the interface circuit. The circuit scale was 1940 µm × 1720 µm, and the bias current was 302 mA. From the simulation results, a sufficient wide bias margin could be obtained up to 30 GHz.

1. Introduction
The superconducting quantum interference device (SQUID) is known as one of the most sensitive magnetometers. To use the SQUID as a magnetometer, it is necessary to add a flux locked loop (FLL). In the FLL operation, a feedback coil that is magnetically coupled to the SQUID generates a negative flux which compensates a change in the input signal flux to keep the SQUID working at the flux-locked point. Additionally, the FLL is composed of semiconductor elements that operate at room temperature and the feedback magnetic flux is an analog signal; thus, this type of SQUID is called an analog SQUID. In the analog SQUID, a large feedback magnetic flux (i.e., a large feedback current) is required to cancel a large signal magnetic flux, and the dynamic range is limited. Additionally, the FLL feedback operation that uses room-temperature electronics limits the slew rate of the analog SQUID.

A digital SQUID based on single flux quantum (SFQ) feedback was proposed, in which a single magnetic flux quantum from a comparator was fed back to the SQUID loop, and the flux applied from the input coil to the SQUID loop was increased or decreased by Φ₀ to keep a flux constant [1]. The digital SQUID with SFQ Φ₀ feedback has attracted attention because of its high slew rate and wide dynamic range, using the SFQ logic [2]. However, the flux feedback of a digital SQUID cannot be lower than the minimum unit of the flux quantum Φ₀ and the magnetic field noise of magnetometer using a digital SQUID is 3-5 orders of magnitude higher than that of a magnetometer that uses an analog SQUID [3, 4] because the flux quantum feedback causes quantization noise in the digital SQUID. One way to realize highly sensitive magnetometers with a digital SQUID is to increase the operational speed of the SQUID and employ sub-flux...
quantum (sub-Φ₀) feedback. We designed a highly sensitive magnetometer that maintains a wide dynamic range using a digital SQUID with sub-Φ₀ feedback[5, 6].

Exploring underground resources using time domain transient electromagnetic measurements (TEM) [7] may be a practical application of a digital SQUID magnetometer. Due to its performance, such as its high slew rate and wide dynamic range, a digital SQUID magnetometer is expected to be installed in an airborne TEM exploration system. Although an analog SQUID magnetometer based on an Nb/AlOₓ/Nb Josephson junction is cooled down with liquid helium, a digital SQUID based on SFQ feedback would be cooled down using a mechanical refrigerator for practical use because of its relatively high power consumption. The output digital signals of a digital SQUID magnetometer operating at cryogenic temperatures have a high frequency, and it is necessary to reduce the frequency to transfer data to room-temperature equipment. Because of the power supply for the airborne situation of a mechanical refrigerator, a digital SQUID magnetometer needs a small SFQ feedback circuit and digital interface circuit with a low power consumption.

In this paper, we will discuss implementation methods for an interface circuit, regarding primarily the circuit size and power consumption.

2. Design of a digital filter for a digital SQUID magnetometer

A digital filter, such as a decimation filter, is an indispensable part of an oversampling ADC. As mentioned above, a digital SQUID is a kind of a ∆-type oversampling ADC and needs to process high-speed signals for low-pass filtering of the signal and sample rate reduction. For a Σ−∆-type A/D converter, it is conventional to use a third-order sinc decimation filter because of its quantization noise reduction efficiency [8].

The transfer function of the third-order (k = 3) sinc filter is given by

\[ H(z) = 1 + 3z^{-1} + 3z^{-2} + z^{-3} \]  

for a decimation ratio of N = 2. We designed a third-order sinc filter unit for N = 2 assuming the use of the CONNECT cell library[9] and the resulting unit size of 960 µm × 640 µm. Assuming \( f_{clk} = 5 \text{ GHz} \) and \( N = 2^3 \) for sending digital signal data to a room temperature electronics at 625 MHz, we need three stages of third-order decimation filters and twelve units per 1-bit digital output. Figure 1 (a) shows the designed third-order sinc filter, and (b) shows a schematic of the three-stage decimation filter. This exceeds the chip size used.

The transfer function of a first-order (k = 1) sinc filter is given by

\[ H(z) = 1 + z^{-1} \]  

for a decimation ratio of N = 2 and a three-stage decimation filter will be easily implemented using T-FF cells and confluence buffer cells for inputting binary data from the up/down counter [10]. The quantization noise reduction performance can be estimated by the root-mean-square (RMS) of the difference between signals \( S(t_i) \) and those digitized values \( Ds_i \) at time \( t_i \) as defined by

\[ RMS = \sqrt{\frac{1}{n} \sum_{i=0}^{n} [S(t_i) - Ds_i]^2} \]  

where \( n \) is the total number of digitized \( Ds_1 \), such as \( n = 2^{13} \).

Figure 2 shows the RMS of quantization noise after the M-stage decimation filter for the third-order and the first-order sinc filters. The noise reduction performance of the first-order sinc filter was almost the same as that of the third-order sinc filter. Using first-order sinc filters for the first three stages and then third-order sinc filters for the following two stages, the noise reduction level was the same as that when using five stage third-order sinc filters. Thus, the first
Figure 1. (a) CAD layout of a third-order sinc filter and (b) schematic of three-stage decimation filters that reduce the frequency by 1/8.

Figure 2. RMS of the quantization noise after the M-stage decimation filter for the third-order and first-order sinc filter. Digital sampling was performed at a clock frequency of 8.196 GHz with a quantization unit of one for a 1-MHz sinusoidal signal with an amplitude of 128.

three stages with first-order sinc filters at low temperature and then rest stages with third-order sinc filters on the FPGA at room temperature would be possible.

Figure 3 shows (a) a CAD layout of the three-stage first-order sinc filter (11-bit binary counter) for an 8-bit up/down counter with an input shift register and output shift register for the verilog logic simulation and (b) shows the logic simulation result for the circuit shown in (a) at an operation frequency of $f_{clk}=8$ GHz. The 8-bit binary data (d7 to d0) shows correct up- and down-count operation at 8 GHz, and the decimated 11-bit binary data (q10 to q0) shows also correct up- and down-count operation at 1 GHz ($=8/2^3$ GHz) with a timing delay for the input and output shift registers. The circuit size of the three-stage first-order sinc filters was reasonably reduced; however, there is a still problem with this circuit scale when considering a
practical digital SQUID magnetometer. Because the dynamic range is limited by the capacity of the up/down counter, a 26-bit up/down counter will be required to ensure a dynamic range of 190 dB for airborne TEM applications. It is difficult to mount a digital SQUID with a 26-bit up/down counter, and a first-order decimation filter on-chip because the circuit scale is too large. For this reason, we assume that an up/down counter and decimation filter will be mounted on the FPGA at room temperature, and we attempted to implement a deserializer circuit that reduces the frequency for data transfer to room temperature equipment at low temperatures.

3. Design of a deserializer circuit

We designed first-order decimation filters that can be implemented on a chip. However, the circuit scale was still too large, and a bias current exceeding 1000 mA was required. From the viewpoint of the circuit scale and power consumption, the high frequency 1-bit digital signals obtained by the digital SQUID at low temperature are reduced to a frequency that can be processed by a semiconductor circuit operating at room temperature, assuming the an up/down counter and decimation filter are implemented on the FPGA board. Therefore, we focused on the design of the proposed deserializer circuit [11].

The deserializer circuit is composed of a T-FF and a D2 flip-flop using the CONNECT cell library, and it reduces the frequency by half in one stage. Figure 4 (a) shows a circuit diagram of a deserializer circuit composed of four stages of 1 bit to 16 bit output. This circuit can reduce the frequency of the input signal by 1/16. Figure 4 (b) shows a CAD layout of four-stage deserializer circuit. The circuit size was 1940 µm × 1720 µm, and the bias current was 302 mA. Figure 5 shows the frequency dependence of the bias margin of a four-stage deserializer circuit. In this simulation, a sufficient bias margin could be realized up to 30 GHz. The power dissipation of the digital SQUID magnetometer will be 675 µW in the low-temperature stage. This will be sufficiently low for operation in a 0.5-W Gifford-McMahon cryocooler[12].
Conclusion
In this study, we designed third- and first-order decimation filters. Additionally, we designed a four-stage deserializer circuit. The third-order decimation filter used in Σ-∆ type ADCs has become very large and difficult to implement. Because the digital SQUID is a ∆ type ADC, it was confirmed that the quantization noise reduction effect was practically the same even when the first-order decimation filter was used, and a first-order decimation filter was designed. Reducing the frequency by 1/8 at an operating frequency of 8 GHz was confirmed by simulations. Finally, assuming that an up/down counter and decimation filter are mounted on an FPGA, we designed a deserializer circuit for the frequency reduction circuit that is required to transfer the output data of the digital SQUID at low temperatures to equipment at room temperature. It was confirmed by simulations that the frequency was reduced by 1/16 at an operating frequency of 8 GHz using a four-stage deserializer circuit with a reasonable small circuit size and low power consumption.
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