Common-Ground Transformerless Inverter with Virtual DC Bus Concept for Single-Phase PV Systems

Saad Ul Hasan** Non-member, Hassan Athab Hassan** Non-member
Mark John Scott** Non-member, Yam Prasad Siwakoti† Non-member
Graham Town*** Non-member, Frede Blaabjerg**** Non-member

(Manuscript received July 26, 2019, revised March 29, 2020)

This study investigates a single-phase common-ground transformerless inverter topology for grid-connected photovoltaic (PV) systems. The inverter shares a common ground with the grid and utilizes minimal components for power conversion, making it suitable for use as an integrated microinverter for solar PV modules. The peak of the ac output voltage is the same as the input DC voltage, and a virtual DC bus capacitor is used to provide power during the negative cycle of the inverter. A simple unipolar sinusoidal pulse-width modulation technique is used to modulate the inverter minimizing switching loss, output filter requirements, and output current ripple. Moreover, a double-charging process is employed to minimize the inrush charging current of the virtual DC bus capacitor. Various operating states along with the design guidelines for choosing the constituent components are presented. Finally, some simulation and experimental results are presented for a 1 kW prototype to validate the proposed topology.

Keywords: common mode (CM) current, photovoltaic (PV) systems, transformerless inverter, unipolar sinusoidal pulse width modulation (SPWM), virtual DC bus

1. Introduction

Grid connected inverters for low power photovoltaic (PV) systems usually require single phase inverter systems. These systems have an enormous growth in the recent years due to the decline of PV module prices, government policies to promote clean energy and, advancements in power electronics and semiconductor technology. There has been significant progress in the research and development of new power converter topologies for PV applications, therefore a strong trend can be seen in terms of improving reliability, power density, efficiency and operability of PV systems [1]. 2016 was a record year for solar as the solar power capacity worldwide exceeded 300 GW after the 200 GW and 100 GW marks were crossed in 2015 and 2012 respectively [2].

A single-phase DC-AC inverter is used in low power (< 5 kW) single-phase grid-connected applications. This usually comes with galvanic isolation provided by a line-frequency or a high-frequency (HF) transformer as a part of the inverter topology which could also provide the voltage transformation. As the research trends focus towards compact and portable solutions by utilizing the advancements in power electronics and semiconductor technologies, the conventional iron and copper-based transformers are not preferred as they add to the weight and cost of the power converters whilst reducing power density and efficiency. Therefore, transformerless inverter-based topologies are a preferred choice for reducing the cost and weight with improved efficiency and power density. However, with the exclusion of a transformer from the circuit, the galvanic isolation is lost, which reciprocates to a common mode current due to high frequency Common Mode Voltage (CMV). The CMV is the average value of the voltages between the output terminals and the common reference of the inverter [3]. This CMV depends on various aspects of an inverter circuit and its modulation strategy, leading to the leakage current. The major culprit behind this leakage current is the presence of a naturally occurring leakage capacitor between the PV frame and its ground [4]. Its value depends upon various factors such as atmospheric conditions, dust, humidity, size and structure of PV system [5]. The leakage current adds to the grid current harmonics and system losses. Additionally, conducted and/or radiated electromagnetic interference (EMI) is caused, which is not desired and needs to be kept within allowable limits as per various electromagnetic compatibility (EMC) standards such as IEC 61000, CISPR 32 etc. Most importantly, the leakage current leads to safety concerns and hence it shall be kept under the recommended limits [6,7,8]. Leakage current can always be eliminated by keeping the CMV constant during the operation of the inverter.

Various transformerless inverter topologies have been...
proposed to achieve higher efficiencies and lower leakage currents. These include decoupling of dc side from ac side by clamping CMV during freewheeling states (15–18) or using common-ground configurations (15–20). The CMV clamping based topologies help to reduce the leakage current at the expense of increased number of active and passive components which add to the complexity, cost and size of the inverter. Moreover, as the decoupling of ac and dc side is done with the help of additional switches, the leakage current may not be entirely eliminated as the switch parasitic capacitance still exists (20). Furthermore, the conduction losses increase in such topologies as the number of devices operating in active states are higher. Therefore, common-ground type inverter topologies are preferred, which theoretically eliminate the leakage current completely. In addition to that, the component count is less which increases the efficiency and reduces the cost. Common-ground transformerless topologies employing a capacitor as a virtual DC bus is a popular concept in which the negative cycle of the output voltage is generated by utilizing this capacitor. This idea was first introduced in (19) and has evolved to yield numerous improved topologies in the recent years. The novel topologies presented in (20) offer minimal leakage currents with high efficiencies. This is in addition to the fact that the inrush current phenomenon occurs during the capacitor charging state (19). The capacitor charging current becomes crucial for the case when the virtual DC bus capacitor is charged directly via a switch. A 6-converter is presented in (16) which offers minimal leakage current, output voltage ripples and total required capacitance but the reported efficiency is comparatively low. A novel inverter topology is reported in (17) with increased number of active and passive components, which increases the cost. The concept of “charge pump” in the transformerless inverter topologies has been explained in (21) in which some switches endure high current peaks due to capacitor charging phenomenon. An improved “flying inductor” based topology has been presented in (22) which has the buck-boost capability, but the switch stress and associated losses are increased with the voltage conversion ratio, hence offering a relatively lower efficiency. Various multilevel inverters are also introduced (5, 12) which can reduce the leakage current, however such topologies usually require higher levels of input dc-link voltages along with additional switches.

Several common-ground transformerless inverter topologies are presented and each topology comes with different pros and cons. An optimal common-ground transformerless topology, therefore, is based on the following attributes:

1. Minimal number of active and passive components
2. Smaller filter requirement
3. Flexibly chargeable virtual DC bus capacitor for intermediate energy storage to be utilized during the provision of negative power cycle
4. Minimal leakage current or constant CMV
5. Low switch stress
6. Peak output voltage equal to the input dc-link voltage; and
7. Controlled capacitor charging current

The topology presented in this paper specifically has a major advantage over the common-ground transformerless topologies mentioned in (20) in terms of offering low inrush current which is a major issue associated with the flying capacitor-based inverter topologies.

This paper is organized as follows: Section 2 describes the proposed topology and its principle of operation along with various operation modes. Section 3 describes the comparative analysis of the proposed topology and confers various important parameters related to design and operation of the topology. Simulation and experimental results for a 1 kW inverter are presented in section 4 and the paper is concluded in section 5.

2. Proposed Topology and Principle of Operation

The proposed topology and its modulation pattern are presented in Fig. 1. It contains 5 switches, one diode, one capacitor, one small inductor and a small filter at the output stage. A simple unipolar sinusoidal pulse width modulation (SPWM) technique is used to modulate the inverter to produce the required operation, which further minimizes the output current ripple, switching loss and output LC filter requirements. Additionally, the capacitor $C_D$ is charged by a dedicated switch $S_C$ which is switched at a high frequency, which in-turn can give flexibility in terms of the dimensions of $L$ and $C_D$. $C_D$ is utilized as a virtual DC bus (19) to provide the negative power cycle of the inverter.

2.1 Principle of Operation of Proposed Topology

The proposed topology utilizes a capacitor $C_D$ as a virtual DC bus to provide the negative power cycle of the inverter. This capacitor $C_D$, is charged by a dedicated switch $S_C$, which switches regardless of any switching states of the inverter, and therefore this phenomenon makes this topology more attractive as the capacitor continuously charges while it is supplying the negative power cycle of the inverter. The charging phenomenon is fairly simple as $C_D$ is charged through the inductor $L$ by a double charging process as used in a classical buck-boost DC-DC converter, which is shown in Fig. 2.

As shown in Fig. 2, energy is first stored in the inductor $L$...
and then in the second step, this stored energy is discharged into the capacitor. By using volt-second balance, the voltage across $C_O$ can be expressed as:

$$V_{CO} = V_{PV} \cdot \left( \frac{d}{1-d} \right) \tag{1}$$

The switching conditions of the diode D depends on the switching state of $S_C$:

$$D = \begin{cases} 
0 & \text{for } S_C = 1, \\
1 & \text{for } S_C = 0. 
\end{cases} \tag{2}$$

The rest of the topology consists of 4 active switches ($S_P$, $S_N$, $S_ZP$ and $S_ZN$) and a small LC filter. These switches are modulated using a standard unipolar SPWM. The various switching states are explained in the next sub-section.

### 2.2 Operating States of the Proposed Topology

The operating states of the proposed inverter can be broken down into 3 switching states (positive, negative and zero), as shown in Fig. 3. Note that the red dotted-line shows the active current path, the blue dotted-line shows the charging current path for $C_O$, which always passes through $S_C$, and the violet dotted-line shows the free-wheeling current path.

#### 2.2.1 Positive Cycle (active)

In this state, the switch $S_P$ switches in an SPWM manner to provide positive power cycle of the inverter. The correct switching logic is implemented by comparing the positive half of the modulation signal with a triangular carrier signal. While the switch $S_P$ is being switched to provide the positive half cycle of the inverter, the switch $S_C$ keeps on switching at a higher frequency to precharge the capacitor for its utilization in the negative half cycle. The switches $S_ZP$ and $S_ZN$ remain off during this state. These switches are only used to provide the zero-states so that a unipolar voltage is created before the filter. The switch $S_C$ and diode $D$ switch complementary to each other in alliance with the double charging process. Moreover, only one switch ($S_P$) is being used to provide the positive voltage before the LC filter, carrying the positive load current, and hence minimal conduction losses during this state.

#### 2.2.2 Positive Cycle (zero)

In this state the switches $S_P$ and $S_N$ are off while the switch $S_ZP$ switches in a complimentary manner to that of $S_P$ during the positive cycle to provide the zero state. This creates a unipolar positive voltage before the filter which then generates a clean positive sinusoidal voltage and current to be provided to the load. During this stage, the body diode of $S_ZN$ conducts in series with $S_ZP$ to allow a path for the free-wheeling current and hence provide zero voltage across the filter. Moreover, the switch $S_C$, keeps switching and keeps the capacitor $C_O$ to be precharged at the voltage level same as $V_{PV}$. As the capacitor is not utilized as a DC bus in the positive power cycle, therefore a simple PI controller\(^{24}\) can be implemented to reduce the switching transients to lessen the associated losses.

#### 2.2.3 Negative Cycle (active)

In this state, $S_N$ is switched in an SPWM manner, this is implemented correctly by comparing the negative cycle of the modulation signal with the unipolar negative triangular carrier signal. While switch $S_C$ is being switched at high frequency regardless of any switching states, in this state the precharged capacitor $C_O$ is utilized as a virtual DC bus\(^{19}\) to provide the negative power cycle of the inverter. The switch $S_P$ is off for this entire negative cycle. Since only one switch ($S_N$) is used to provide...
the negative voltage before the LC filter, this leads to lower conduction losses compared to the case of other common-ground transformerless inverter topologies. Both of the switches $S_{ZP}$ and $S_{ZV}$ are off during this state.

2.2.4 Negative Cycle (zero) In this state, $S_P$ and $S_N$ are off while $S_{ZN}$ switches in a complimentary manner to that of $S_N$ to provide a path for the free-wheeling current through the body diode of switch $S_{ZP}$. This creates a zero voltage before the filter; hence a unipolar negative voltage is created before the LC filter during the negative power cycle. The switch $S_C$ keeps on charging the capacitor $C_O$. As the capacitor is used as a DC bus to provide the negative power cycle, therefore a constant voltage equal to $V_{PV}$ is required to be maintained by $C_O$ as the peak amplitude of the negative power cycle is dependent upon $V_{CO}$. A simple PI controller can be utilized to ensure that the power drain from the capacitor is balanced by the charged being filled into it governed by switch $S_C$.

The aforementioned operating states are summarized in Table 1. These states repeat in each consecutive power cycle to create a unipolar positive and negative voltage before the LC filter. This chopper DC voltage is then filtered out of LC filter to provide a clean sinusoidal voltage and current to the load. Note that switching frequency and state of the switch $S_C$ is independent of operating states listed in Table 1. This helps to independently control the voltage across the capacitor and hence any offset in the output AC voltage and current is eliminated. The presented topology being modulated with SPWM leads to small filter requirements, low switching losses, low EMI and low ripple in the output current. Compared with other transformerless inverter topologies, this topology can also be implemented using two industry standard half-bridge modules which has various benefits such as increased power density, quick and cost-effective implementation. Moreover, since wide bandgap (WBG) based HF power converters are very attractive due to the fact that they offer a small size, small filter requirements, high efficiency and portability, therefore customized half-bridge modules such as (30) can be used to implement this topology to achieve contemporary benefits.

3. Comparative Analysis and Design Guidelines

The following sub-sections compare the proposed topology with similar transformerless common-ground topologies to analyse its merits and demerits. Various design guidelines and essential insights related to the proposed topology are presented for better understanding and easy implementation.

3.1 Comparison with Similar Topologies Table 2 presents a comparative overview of the proposed topology considering key parameters such as number of active and passive components required to build the inverter topology, number of semiconductor devices in the load current path, input voltage requirement, output filter requirements, in-rush current consideration, voltage stress across the active switches and leakage current etc.

3.2 Virtual DC Bus Capacitor Sizing The virtual DC bus capacitor is important especially during the negative power cycle; hence the capacitor shall be sized appropriately for a seamless transition of AC waveform from positive to negative cycle. The size of the capacitor is the function of average discharging current drained out of it during the negative power cycle, the carrier switching frequency for the SPWM, modulation index and voltage ripple requirements. The design steps for capacitor size calculation are based on (27). To begin the analysis, the following assumptions are made: i) The current (negative part) provided through $C_O$ forms a pure sinusoidal waveform after passing through the LC filter and ii) The capacitor is fully charged before the negative cycle starts (with or without the PI control).

The control strategy is based on simple SPWM strategy (by comparing a bipolar carrier signal with a reference sinusoidal signal, shown in Fig. 8(a)). The reference signal ($v_{REF}(\theta)$) can be expressed as:

$$v_{REF} = M \sin(\theta)$$

(3)

where $M$ is the modulation index and $\theta = \omega t$. $\omega$ is the angular frequency which is equal to $2\pi f_{grid}$. Note that $f_{grid}$ is 50/60 Hz as per the standards. The RMS value of the output voltage for $S_C$ being switched at 50% duty cycle is given as:

$$V_{OUT} = \frac{M V_{PV}}{\sqrt{2}}$$

(4)

The voltage ripple on the capacitor ($\Delta V_C$) is estimated by the maximum discharging time ($t_{DIS(max)}$), the output current ($I_{ac,max} \sin \theta$) and size of the capacitor ($C_O$):

$$\Delta V_C = \frac{I_{ac,max} \sin \theta \cdot t_{DIS(max)}}{C_O}$$

(5)

The discharging time can be presented as:

$$t_{DIS(max)} = \frac{T_s}{2} (1 + M \sin \theta)$$

(6)

where $T_s$ is the switching period of the carrier frequency signal.

Considering the fact that $\Delta V_C$ reaches it maximum value when $\sin \theta = \frac{V_{out}}{V_{PV}}$ and solving for $\Delta V_C = \frac{V_{out}}{C_O}$, the minimum capacitor size $C_{O,min}$ can be approximated as follows:

$$C_{O,min} \geq \frac{I_{ac,max} M T_s}{2 \Delta V_C}$$

(7)

3.3 Common-mode behavior and Leakage Current

The common-mode voltage ($v_{CM}$) and leakage current ($i_{CM}$) analysis of the proposed topology is presented in this section. An equivalent model for the common-ground transformerless inverter topology presented in this paper is shown in Fig. 4. $Z_G$ corresponds to the ground resistance which is $\sim 5 \Omega$ as per standards and the naturally occurring parasitic capacitance between the photovoltaic (PV) panel and ground ($C_{PV}$) ranges from tens of nF up till µF. The value of $C_{PV}$ depends upon various factors such as atmospheric conditions, size and structure of PV system etc, therefore 100 nF/kW can

| States | $S_P$ | $S_N$ | $S_{ZP}/D$ | $S_{ZV}/D$ | $S_C$ |
|--------|------|------|----------|----------|------|
| Positive (active) | 1 | 0 | 0 | 0 | X |
| Positive (zero) | 0 | 0 | 1/0 | 0/1 | |
| Negative (active) | 0 | 1 | 0 | 0 | |
| Negative (zero) | 0 | 0 | 0/1 | 1/0 | |

X – Don’t care state

Table 1. Summary of the switching states
Table 2. Comparison of Proposed Topology with various other transformerless topologies

| Transformerless inverter topology with intermediate energy storage capacitor | Number of components | No of switches in the load current path | \( V_m \) (V) | Leakage Current (mA) | Output Filter | Voltage stress on semiconductor switches | Inrush current spikes ** | Efficiency (%) |
|---|---|---|---|---|---|---|---|---|
| Proposed topology [25] | 5 | 1 | 2 | 1 (during zero-states) | 400 | = 0 | 0.35 | - | 2.2 | \( V_{m1} = V_{m2} = V_{mN} = 2V_n \) | 95.2 |
| Type-I [20] | 4 | 1 | 0 | 2 | 2 | 400 | = 0 | 0.35 | - | 2.2 | \( V_{m1} = V_{m2} = V_{mN} = V_n \) | 99.2 |
| Type-II [20] | 4 | 1 | 0 | 1 | 2 | 400 | = 0 | 0.35 | - | 2.2 | \( V_{m1} = V_{m2} = V_{mN} = 2V_n \) | 99.25 |
| Type-III [20] | 4 | 0 | 0 | 1 | 1 | 400 | = 0 | 0.8 | - | 10 | \( V_{m1} = V_{m2} = V_{mN} = V_n \) | 97.8 |
| Flying capacitor [26] | 4 | 0 | 0 | 2 | 2 | ≥ 800 | NA | 3 | - | 2.2 | \( V_{m1} = V_{m2} = V_{mN} = 3V_n \) | NA |
| Virtual DC bus [19] | 5 | 2 | 0 | 2 | 2 | 400 | = 0 | 8 | 0.8 | 0.34 | \( V_{m1} = V_{m2} = V_{mN} = V_n \) | 95.2 |
| Extended H-6 type [14] | 6 | 6 | 2 | 3 | 3 | 400 | 1 x 4 | 0.5 x 2 | 2.2 | \( V_{m1} = V_{m2} = V_{mN} = 2V_n \) | 98.2 @ 1 kVA |
| Charge pump [21] | 4 | 2 | 4 | 1 | 2 | 400 | = 0 | 4 | 2 | 2.2 | \( V_{m1} = V_{m2} = V_{mN} = 2V_n \) | 97.4 @ 0.5 kVA |
| Flying Inductor [22] | 5 | 0 | 2 | 2 | 2 | 100 | = 0 | 0.3 | - | 3.3 | \( V_{m1} > V_n \) *** | 92.5 @ 200 kVA |

Where, S= Switch, D= diode, C= Capacitor, L= Inductor, L a, L c, C e = passives associated with the output filter, \( V_m \)= Input voltage for \(-230 \text{ V applications}, \) \( V_{m1} = V_{m2} = V_{mN} = 230 \text{ V applications} \) or not available in the publication, \( \text{** Including input DC capacitor(s)} \) \( \text{** Inrush current analysis is based on the phenomenon of high charging current for the capacitor.} \text{*** Switch stress dependent on the boost factor.} \text{8}

In principle, the common-mode leakage current \( i_{CM} \) is generated by non-uniform or inconsistent common-mode voltage. The common-mode leakage current leads to increased system losses, reduction in the quality of grid current, increased electromagnetic interference (EMI) and safety issues. Consequently, the solution to prevent \( i_{CM} \) in transformerless inverter topologies is to keep the common-mode voltage constant. As per [18], the common-mode voltage \( \left( V_{CM} \right) \) is given as:

\[
V_{CM} = \frac{V_{Pn} + V_{Nn}}{2} \tag{8}
\]

where \( P \) and \( N \) are the positive and negative terminals of the PV panel respectively, and \( n \) corresponds to the ground terminal of AC side. In case of the proposed topology, since there is a common ground and \( N \) is literally shorted with \( n \) in addition to the fact that the peak of AC side is same as the DC input, therefore \( V_{Pn} = V_{PV} \) and \( V_{Nn} = 0 \), which leads to the common-mode voltage expression to be simplified to:

\[
V_{CM} = \frac{V_{PV}}{2} \tag{9}
\]

The above expression mathematically verifies that there is
no leakage current as \( v_{CM} \) is constant and contains no frequency related components.

### 3.4 Voltage and Inrush Current Control of the Virtual DC Bus Capacitor

The capacitor \( C_{o} \), is used as a virtual DC bus to provide the negative power cycle of the inverter, therefore it is required to be charged enough during the provision of negative power cycle to the load. A simple PI control method, shown in Fig. 5, can be used to keep a stable voltage across the capacitor \( C_{o} \). This ensures that the peak of ac voltage in the negative power cycle is same as the positive power cycle and both cycles appear symmetrical and undistorted. In addition to the voltage control across the capacitor, the controller will also ensure optimal switching of \( S_{C} \) which increases the efficiency of the inverter.

Figure 6 shows a comparative investigation with and without a PI controller integrated in the modulation of proposed inverter. It can be noted that the output voltage becomes distorted when \( S_{C} \) is switched at constant duty cycle (50%) with an open loop control. As per the simulation results, a 14% ripple reduction was achieved by using a dedicated PI controller for switching \( S_{C} \).

A double charging process to charge \( C_{o} \), significantly helps to reduce the high charging current problems unlike the other virtual DC bus capacitor based topologies\(^\text{[20]}\text{[21]}\). The direct capacitor charging via a switch leads to overburdened switch current stress\(^\text{[15]}\). In the proposed topology, the capacitor peak charging current is particularly important to consider during the negative power cycle as the capacitor is being drained out and charged simultaneously. This is also noticeable in simulation results shown in Fig. 7 in which the \( i_{C_{o}} \) is measured as the output of the integrated buck-boost which is used to pump-in the charge into the virtual DC bus capacitor.

It must be noted that there is a tradeoff between the handling of the capacitor charging current and establishment of a symmetrical positive and negative power cycle. As the PI control will limit the \( S_{C} \) switching during the positive half cycle which will prevent the losses, and hence increases the efficiency, but on the other hand while the capacitor is used as a virtual DC bus, the \( S_{C} \) will switch more often to keep the capacitor filled with energy, hence the charging current will be severe in this case. Both cases are demonstrated in Fig. 7.

The peak capacitor charging current can be determined based on the understanding that the active state during negative power cycle (see Fig. 3(c)) can be sub-divided into two sub-states; one when \( S_{C} \) is on and another when it is off. These two sub-states, named as active state 1 and active state 2, are shown in Fig. 8 ((b) and (c)).

Assuming a unity power factor, the output current...
waveform will be in phase with the sinusoidal reference as shown in Fig. 8(a). The worst-case condition for the capacitor charging current occurs when the grid current is at the negative peak. For active state 1, when $S_C$ is on, the capacitor current ($i_{Co,1}$) is the grid current ($I_{LF}$) as shown in Fig. 8(b). When the grid current is at its peak during the negative half cycle, the capacitor current will be:

$$i_{Co,1} = -I_{o, pk}$$

during active state 1. Whereas, for active state 2, when $S_C$ is off, the capacitor current ($i_{Co,2}$) can be determined using charge second balance:

$$i_{Co,2} = \frac{D}{1-D} i_{Co,1} \approx i_{Co,1}.$$  (11)

The peak capacitor charging current is approximately $I_{o, pk}$ for the case when $S_C$ is switched to keep the voltage across $C_D$ same as the dc-link voltage. The current carried by the inductor $L$ ($I_L$) during the active state 2 can be determined using KCL as $2 \cdot I_{o, pk}$. Therefore, switch $S_C$ and $D$ must be sized to handle at least twice the load current.

4. Simulation and Experimental Results

The simulations of the proposed topology have been carried out in PSIM and Matlab-Simulink using the PLECS toolboxes to verify its working principle and analyzing various aspects in terms of key waveforms, voltage stress across various semiconductor devices and leakage current etc. Moreover, the thermal analysis and the heat sink calculation was based on (29).

4.1 Simulation Results

The simulation model of 1 kVA of the proposed topology was built as per the parameters listed in Table 3.

The key simulated waveforms for various parameters such as output voltage ($v_{ac}$) and current ($i_{ac}$), chopped DC voltage ($v_{ab}$) before the LC filter and switch-stress across various switches are shown in Fig. 9 which validate the theoretical basis of the proposed topology. The rms value of the output voltage is 220 V with a dc-link voltage of 340 V. The modulation index ($m$) is kept at 0.92 and the corresponding rms value of load current is 4.6 A with a resistive load of 48 Ω. The three-level unipolar voltage before the filter denoted as $v_{ab}$ is also shown which filters out as a smooth sinusoidal voltage and current denoted as $v_{ac}$ and $i_{ac}$ respectively. The voltage stress across various switches is also shown and it is double of the dc-link voltage for $S_P$ and $S_N$ and same as the dc-link voltage for $S_{2P}$ and $S_{2N}$. Moreover, the voltage across $S_C$ and $D$ is also twice the dc-link voltage.

The waveforms of the currents passing through different power switches are shown in Fig. 10 to comprehend in-depth understanding of switching patterns and their amplitude

Table 3. Parameters and components used in simulation

| Parameter                  | Value, Description                  |
|----------------------------|-------------------------------------|
| Power switches             | SIC MOSFET C3M0120090D              |
| Carrier frequency          | 25 kHz                              |
| Line frequency             | 50 Hz                               |
| Virtual DC bus capacitor   | 100 μF                              |
| Filter capacitor           | 2.4 μF                              |
| Filter Inductor            | 0.37 mH                             |
| Inductor for $C_D$         | 0.37 mH                             |
| Switching frequency for $S_C$ | 100 kHz                  |
| Load                       | 48 Ω                                |

Fig. 9. Key simulated waveforms for output voltage/current, unipolar voltage across filter and switch stresses

Fig. 10. Key simulated waveforms for current stress across various switches
levels. It can be noted that since the switch $S_C$ is utilized to provide the charging current of the DC bus capacitor, it experiences the maximum current stress relative to the other switches due to the in-rush charging current phenomenon of $C_D$ especially in the negative power cycle. Moreover, it can be seen that the current flows bi-directionally through the two switches $S_{ZP}$ and $S_{ZN}$ to provide a zero state before the LC filter. The switches $S_P$ and $S_N$ conduct in the positive and negative power cycle respectively.

A simulation model similar to the one shown in Fig. 4 with a value of $C_{PV} = 100 \text{ nF}$ and $Z_G = 5 \Omega$, was built in PSIM environment to analyze the behavior of leakage current. The simulation result for the leakage current is shown in Fig. 11 and it is calculated as 0.041 mA. There is a good match between the theoretical analysis with the simulation results, which are also supported by the experimental results discussed in the following subsection.

4.2 Experimental Results The prototype picture has been shown in Fig. 12 and the switch driving signals were realized via a C2000 Peripheral Explorer Kit by utilization of SimCoder block of PSIM.

4.2.1 Converter Operation Figure 13 presents the key waveforms depicting the correct operation of the proposed topology in validation of the theoretical and simulation-based discussion in the previous sections. It can be noted from the key waveforms shown in experiment results that the rms value of the output voltage is 220 V with a dc-link voltage of 340 V. The modulation index $M$ was kept at 0.92 and it shows a peak efficiency of 95.2% at an output power of 1.6 kW. Additionally, the voltage and current are in-phase for a resistive load of 48 $\Omega$.

The switch stress across the four switches which are operated in an SPWM manner are shown in Fig. 14 which correlate with the simulation results. The switch stress results are captured while the rms value of output voltage was 110 V. The maximum voltage across the two main switches ($S_P$ and $S_N$) which deliver the full load current was double of the dc-link voltage, whereas the voltage across the switches providing zero states ($S_{ZP}$ and $S_{ZN}$) was equal to the dc-link as depicted in Fig. 14. The voltage across $S_C$, and $D$ is also twice the dc-link voltage. Additionally, the diode $D$ was replaced by a SiC MOSFET to be used as a synchronous rectifier to achieve a better switching performance and an enhanced efficiency.

It is evident from the Fig. 15 that the inductor current doesn’t exceed the double of the ac side rms current. Hence the double charging process significantly aids to lessen the inrush capacitor charging current.

4.2.2 Efficiency and Loss Analysis The key parameters given in Table 3 were used for the measurement
of efficiency of the proposed inverter. The graph comparing the efficiency vs load performance of the proposed inverter is shown in Fig. 16. The measurements were done by a high precision power analyzer Hioki PW3390 and maximum efficiency measured was 95.2% at a load of 1.6 kW. A good match can be found between theoretical and experimental losses, which is presented in Fig. 17 and the major loss breakdown pertaining to conduction, switching and switch parasitic capacitor losses is presented in Fig. 18. Additionally, Fig. 19(a) presents the loss breakdown among the power

switching devices. These have been further divided into the switching and conduction losses. Moreover, as expected, most of the losses are contributed by the charging circuitry as shown in Fig. 19(b). The difference between the theoretical and practical losses becomes minimal around 0.8 kVA. Moreover, as the peak current passing through the capacitor charging path is double of the grid current and since both of the switch SC and D are operating at relatively higher switching frequency as compared to the other four SPWM switches, therefore SC and D form a major contribution to both the conduction and switching losses.

4.2.3 Total harmonic Distortion The total harmonic distortion (THD) of the output current was tested using a SIGLENT SDS2104X oscilloscope. The THD was measured as < 2% which meets well with the IEEE standard 519 (30). The waveforms as well as the THD measurements are shown in Fig. 20.
5. Conclusion

This paper presents a common-ground transformerless PV inverter topology which is based on the concept of virtual DC bus capacitor which is charged by a double-charging process through an inductor to minimize inrush current issues in switched capacitor-based power converters. The proposed topology offers minimal leakage current and a simple operation based on unipolar SPWM leads to small filter requirements, low switching losses, low EMI and low ripple in the output current. Additionally, only 1 switch is operated in each active state which helps to reduce the associated conduction losses. Moreover, an MPPT algorithm can be implemented to cater for the intermittent nature of the renewable sources. Finally, the topology can be implemented flexibly with two industry standard half-bridge modules which can reduce cost, ease implementation and achieve high power density paving its implementation as a micro-inverter which can be installed at the back of solar panels.

References

(1) S. Kouro, J.I. Leon, D. Vinnikov, and L.G. Franquelo: “Grid-Connected Photovoltaic Systems: An Overview of Recent Research and Emerging PV Converter Technologies”, IEEE Industrial Electronics Magazine, Vol.9, No.1, pp.47–61 (2015)
(2) SolarPower Europe: “Global Market Outlook for Solar Power 2017–2021”, SolarPower Eur (2017)
(3) T. Kerekes, R. Teodorescu, and M. Lisserre: “Common mode voltage in case of transformerless PV inverters connected to the grid”, IEEE Int. Symp. Ind. Electron., pp.2390–2395 (2008)
(4) M. Calais and V.G. Agelidis: “Transformerless single-phase grid connected photovoltaic systems—an overview”, IEEE International Symposium on Industrial Electronics. Proceedings. ISIE ’98, pp.224–229 (1998)
(5) G. Vazquez, P.R. Martinez-Rodriguez, J.M. Sosa, G. Escobar, and M.A. Juarez: “Transformerless single-phase multilevel inverter for grid tied photovoltaic systems”, IECION Proc. Industrial Electron. Conf., pp.1868–1874 (2014)
(6) T. Kerekes: “Analysis and Modeling of Transformerless Photovoltaic Inverter Systems”, PhD thesis (2013)
(7) H. Xiao and S. Xie: “Leakage Current Analytical Model and Application in Single-Phase Transformerless Photovoltaic Grid-Connected Inverter”, IEEE Transactions on Electromagnetic Compatibility, Vol.52, No.4, pp.902–913 (2010)
(8) O. Lopez, et al.: “Eliminating Ground Current in a Transformerless Photovoltaic Application”, IEEE Transactions on Energy Conversion, Vol.25, No.1, pp.140–147 (2010)
(9) “International Electrotechnical Commission (CISPR) Guidance for users of the CISPR Standards appropriate CISPR EMC Standards applicable to your products, systems and installations”, http://www.iec.ch/emc/pdf/cispreguide2015.pdf, accessed 3rd July 2019
(10) B. Yang, W. Li, Y. Gu, W. Cui, and X. He: “Improved Transformerless Inverter With Common-Mode Leakage Current Elimination for a Photovoltaic Grid-Connected Power System”, IEEE Transactions on Power Electronics, Vol.27, No.2, pp.752–762 (2012)
(11) H. Xiao, S. Xie, Y. Chen, and R. Huang: “An Optimized Transformerless Photovoltaic Grid-Connected Inverter”, IEEE Transactions on Industrial Electronics, Vol.58, No.5, pp.1887–1895 (2011)
(12) B. Ji, J. Wang, and J. Zhao: “High-Efficiency Single-Phase Transformerless PV HBridge Inverter With Hybrid Modulation Method”, IEEE Transactions on Industrial Electronics, Vol.60, No.5, pp.2104–2113 (2013)
(13) Y.R. Kafle, G.E. Town, X. Guochun, and S. Gantan: “Performance comparison of single-phase transformerless PV inverter systems”, IEEE Appl. Power Electron. Conf. Expo. - APEC, pp.3589–3593 (2017)
(14) M. Islam, N. Afrin, and S. Mekhilef: “Efficient Single Phase Transformerless Inverter for Grid-Tied PVG System with Reactive Power Control”, IEEE Transactions on Sustainable Energy, Vol.7, No.3, pp.1205–1215 (2016)
(15) A. Kacmasevicu and A. Hoover: “Managing Inrush Current” (2015)
(16) Q.C. Zhong and W.L. Ming: “A 6H-Converter That Reduces Common Mode Currents, Output Voltage Ripples, and Total Capacitance Required”, IEEE Trans. Power Electron., Vol.31, No.12, pp.8435–8447 (2016)
(17) J.F. Ardasher, Y.P. Siwakoti, M. Sabahi, S.H. Hosseini, and F. Blaabjerg: “A grid-connected single-phase transformerless inverter for PV application”, IEECON Industrial Electron. Conf., pp.2384–2389 (2016)
(18) S.V. Arzago, P. Zschach, and R. Mallwitz: “Highly efficient single-phase transformerless inverters for grid-connected photovoltaic systems”, IEEE Trans. Ind. Electron., Vol.57, No.9, pp.3118–3128 (2010)
(19) Y. Gu, W. Li, Y. Zhao, B. Yang, C. Li, and X. He: “Transformerless Inverter With Virtual DC Bus Concept for Cost-Effective Grid-Connected PV Power Systems”, IEEE Transactions on Power Electronics, Vol.28, No.2, pp.793–805 (2013)
(20) Y.P. Siwakoti and F. Blaabjerg: “Common-ground-type transformerless inverters for single-phase solar photovoltaic systems”, IEEE Trans. Ind. Electron., Vol.65, No.3, pp.2100–2111 (2018)
(21) J.F. Ardasher, M. Sabahi, S.H. Hosseini, F. Blaabjerg, E. Babare, and G.B. Gharehpolian: “A Single-Phase Transformerless Inverter With Charge Pump Circuit Concept for Grid-Tied PV Applications”, IEEE Trans. Ind. Electron., Vol.64, No.7, pp.5403–5415 (2017)
(22) M. Tolig, Arazay, M. Sabahi, E. Babare, and F. Abbas: Aghdam Meinaagh: “Modulated Single-Phase Single-Stage Grid-Tied Flying Inductor Inverter With MPPT and Suppressed Leakage Current”, IEEE Trans. Ind. Electron., Vol.65, No.1, pp.221–231 (2018)
(23) L. Zhang, K. Sun, L. Feng, H. Wu, and Y. Xing: “A Family of Neutral Point Clamped Full-Bridge Topologies for Transformerless Photovoltaic Grid-Tied Inverters”, IEEE Transactions on Power Electronics, Vol.28, No.2, pp.730–739 (2013)
(24) R. Teodorescu, M. Lisserre, and P. Rodriguez: Grid Converters for Photovoltaic and Wind Power Systems: IEEE-Wiley (2011)
(25) S.U. Hasan, B. Shaffer, H.A. Hassan, M.J. Scott, Y. Siwakoti, and G.E. Town: “Common-ground transformerless inverter for solar photovoltaic module”, IEEE Applied Power Electronics Conference and Exposition (APEC), pp.167–172 (2018)
(26) M. Islam, S. Mehlhief, and M. Hasan: “Single phase transformerless inverter topologies for grid-tied photovoltaic system: A review”, Renew. Sustain. Energy Rev., Vol.45, pp.68–80 (2015)
(27) Y. Siwakoti, A. Mahajan, D. Rogers, and F. Blaabjerg: “A novel seven level active neutral-point-clamped converter with reduced active switching devices and DC-link voltage”, IEEE Trans. Power Electron., Vol.34, No.11, pp.10492–10508 (2019)
(28) T. Kerekes, R. Teodorescu, P. Rodriguez, G. Vazquez, and E. Aldabas: “A New high-efficiency single-phase transformerless PV inverter topology”, IEEE Trans. Ind. Electron., Vol.58, No.1, pp.184–191 (2011)
(29) N. Seshasayee: “Understanding Thermal Dissipation and Design of a Heatsink”, TL, Texas Instruments, pp.1–4 (2011)
(30) “IEEE 519-2014 - IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems”, IEEE Power and Energy Society (2014)
(31) TPD3215M: “GaN Power Hybrid HEMT Half - Bridge Module”, pp.1–9 (2016)
(32) Fluke: “Earth Ground Resistance”, Appl. note 2633834 B-EN-N Rev A, p.16 (2019)

Saad Ul Hasan

(Saad Ul Hasan) received his B.S. and M.S. degrees in Electrical Engineering respectively from Bahria University, Islamabad, Pakistan, and Xi’an Jiaotong University (XJTU), Xi’an, China. From September 2011 to July 2013, he was with Power Electronics & Renewable Energy Research Center (PEREC), as a Graduate Student with XJTU. He finished his Ph.D. in Electronics Engineering from Macquarie University, Australia in 2018 and currently working as an honorary Research Associate at University of Technology, Sydney, Australia. During the summer of 2017, he was a visiting scholar at Miami university, Ohio, USA where worked on novel common-ground transformerless inverters for grid connected PV systems. His research interests include DC-DC and DC-AC power converters, EMI suppression in power converters, and wide bandgap (GaN/SiC) based high frequency power converters. Dr. Hasan is a frequent reviewer of APEC, ECCE, IET power electronics, JESTPE and transactions on Industrial Electronics. He is also an active IEEE member and currently serving as Mentor Chair in IEEE NSW section.
Hassan Athab Hassan (Non-member) received B.Sc. degree in Electrical Power Engineering from Basra Technical College, Iraq. He received the M.Sc degree in Electrical and Computer Engineering from Miami University, USA in 2017. From 2009 to 2015, he was a maintenance and operation engineer with the South Oil Company. Currently, he is a senior engineer working for Rumiaia Operation Organization in motor drive section.

Mark John Scott (Non-member) received his B.S., M.S., and Ph.D. degrees in Electrical Engineering from The Ohio State University in 2005, 2013, and 2015, respectively. His work experience includes developing and installing industrial automation hardware and performing validation testing of power electronics for automotive applications. Currently, he is an assistant professor at Miami University in Oxford, Ohio, USA. Dr. Scott researches the design trade-offs associated with using silicon carbide (SiC) and gallium nitride (GaN) power devices in electrified transportation. His investigations focus on the conducted electromagnetic interference (EMI) generated by GaN and SiC based hardware. Additionally, he explores prognostic health management techniques for power conversion hardware based on EMI spectral analysis. Dr. Scott has served as a reviewer for many conferences and journals. He was the Local Arrangements Chair for the 2017 IEEE Energy Conversion Congress and Exposition (ECCE). He is currently the Publicity Chair for the Workshop on Wide Bandgap Power Devices and Applications (WiPDA) and he is serving as the Financial Chair for ECCE 2018, ECCE 2019, and ECCE 2020.

Yam Prasad Siwakoti (Non-member) received the B.Tech. degree in electrical engineering from the National Institute of Technology, Patna, Patna, India, in 2003, the M.E. degree in electrical power engineering from the Norwegian University of Science and Technology, Trondheim, Norway, and Kathmandu University, Dhusikhel, Nepal, in 2010, and the Ph.D. degree from Macquarie University, Sydney, Australia, in 2014. He was a postdoctoral fellow at the Department of Energy Technology, Aalborg University, Denmark (2014–2016). He was a visiting scientist at the Fraunhofer Institute for Solar Energy Systems, Freiburg, Germany (2017/2018). He also served as a Guest Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS (2015/2016). He is also a recipient of the prestigious Green Talent Award from the Federal Ministry of Education and Research, Germany in 2016. Currently he is a Lecturer in the Faculty of Engineering and Information Technology, University of Technology Sydney, Australia. He serves as an Associate Editor of three major journals: IEEE TRANSACTIONS ON POWER ELECTRONICS, IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and the IET Power Electronics. He is also a peer review college member of Engineering and Physical Science Research Council (EPSRC), UK.

Graham Town (Non-member) received the B.E. degree with first class honors from the New South Wales Institute of Technology, Sydney, Australia, in 1984 and the Ph.D. degree from the University of Sydney, Sydney, Australia, in 1992. From 1978 to 1985, he was with Amalgamated Wireless Australasia, where he was a Trainee Engineer, and a Senior Engineer, and worked on a variety of projects including the Inter-scan microwave landing system and the development of first generation optical fiber communication systems. In 1985, he joined the Department of Electrical Engineering at the University of Sydney to undertake research in the area of nuclear magnetic resonance imaging, and was appointed Lecturer in 1991. In 2002 he joined the Department of Electronics at Macquarie University, Sydney, Australia, where he established that University’s undergraduate engineering degree program. He is currently a Professor in the School of Engineering. He is author or coauthor of more than 200 refereed journal and conference papers and several patents. His research contributions have been diverse, including nuclear magnetic resonance imaging and spectroscopy, guided-wave optics and photonics, terahertz wireless technology, power electronics and power systems, and engineering education. Professor Town is a Fellow of the Institute of Engineers Australia, and a Senior Member of the IEEE.

Frede Blaabjerg (Non-member) was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. From 1988 to 1992, he got the Ph.D. degree in Electrical Engineering at Aalborg University in 1995. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. From 2017 he became a Villum Investigator. He is honoris causa at University Politehnica Timisoara (UPT), Romania and Tallinn Technical University (TTU) in Estonia. His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives. He has published more than 600 journal papers in the fields of power electronics and its applications. He is the co-author of four monographs and editor of ten books in power electronics and its applications. He has received 31 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014, the Villum Kann Rasmussen Research Award 2014 and the Global Energy Prize in 2019. He was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018. In 2019–2020 he serves a President of IEEE Power Electronics Society. He is Vice-President of the Danish Academy of Technical Sciences too. He is nominated in 2014–2018 by Thomson Reuters to be between the most 250 cited researchers in Engineering in the world.

548 IEEJ Journal IA, Vol.9, No.5, 2020