An ultrahigh-impedance superconducting thermal switch for interfacing superconductors to semiconductors and optoelectronics

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The ability to interface superconductors with semiconductors is a critically-missing component of the advanced computing ecosystem. At present, a significant number of scalable quantum computing and neuromorphic architectures plan to operate at cryogenic temperatures, using superconductors as the basis of their architecture or as a measurement component. In these architectures, semiconductor systems are often proposed as a top-level control with low-temperature passive components and intermediary superconducting electronics acting as the direct interface to the lowest-temperature stages — this stratification is required because semiconductor-based amplification of small superconducting signals consumes too much power for extensive use at kelvin-scale temperatures. As a result, these architectures necessarily require a low-power superconductor-semiconductor interface that presently does not exist, for example to leverage CMOS coprocessors for classical control of superconducting qubits, or as a means to drive optoelectronics from superconducting detectors. Here we present a superconducting switch device that is capable of translating low-voltage superconducting inputs directly into semiconductor-compatible (>1,000 mV) outputs at kelvin-scale temperatures. As a demonstration of a superconductor-semiconductor interface, we have used the switch to drive an LED in a photonic integrated circuit, generating...
photons at 1 K from a low-voltage input and detecting them with an on-chip superconducting single-photon detector. We additionally characterized the device’s timing response (<300 ps turn-on, ~15 ns turn-off), output impedance limitations (>1 MΩ), and energy requirements (0.18 fJ/µm², 3.24 mV/nW). Despite its simplicity as a thermal device, we found that this device is an extremely promising candidate for a superconductor-to-semiconductor logical interface.

The primary issue with interfacing superconductor electronics with semiconductor electronics is one of bandgap and impedance mismatch. The average superconductor has a bandgap almost a thousand times smaller than that of a semiconductor (e.g. 2.8 mV for Nb versus 1,100 mV for Si). Similarly, the impedances of these systems are differ greatly: a typical transistor element has an effective input impedance in the 10⁴-10⁹ range, while a typical superconducting logic element will have an output impedance in the 0-10¹ range. Due to these mismatches, it is extremely difficult to drive the high-impedance inputs of a semiconductor element to ~1,000 mV using ~1 mV superconductor outputs. At present, there are only two known ways to generate 1,000 mV from a superconducting output: (1) connect several hundred few-millivolt devices (such as Josephson junctions) in series, or (2) allow a superconducting nanowire to latch. Both of these methods come with a handful of downsides, including large static-power consumption, large area, varying input impedances, latching, and poor output-input feedback.

The most successful previous attempts at creating a superconductor-to-semiconductor interface consisted of a superconducting preamplifier stage (e.g. a Suzuki stack) combined with a semiconductor amplifier stage (e.g. HEMTs). This approach was very effective in translat-
ing signal levels, but was power-constrained. In particular, using semiconductor transistors in an amplifier configuration necessarily drew significant static power (\(~1\) mW each), which strongly limited scalability on a cryogenic stage. In related work, a CMOS-latch input was used after the preamplifier to static power, but introduced the need for per-channel threshold calibration. In an alternate approach, it was shown that a \(>1\) V output could be created from a nanowire device such as the nanocryotron, but using the nanocryotron as a means for semiconductor-logic interfacing has proved to have a few issues: (1) creation of the high-impedance state was a hotspot-growth process that takes a nontrivial amount of time, (2) it was hysteretic and not able to self-reset without external circuitry, and (3) output-input feedback was a concern, as the input and output terminals were galvanically connected.

The device we present here is a monolithic switching element that combines a low-impedance resistor input (1-50 \(\Omega\)) with a high-impedance (\(>1\) M\(\Omega\)) superconducting nanowire-meander switch output. The input element and switching element are isolated galvanically but coupled thermally by a thin (25 nm) dielectric spacer. When input current is applied to the resistor, the state of the entire nanowire-meander is switched from superconducting to normal. As can be seen directly in Fig. 1, the input induces an extremely large impedance change in the output: from 0 \(\Omega\) to \(>1\) M\(\Omega\). The power cost of inducing this change is surprisingly small when compared to existing methods, and crucially it can be operated in a non-hysteric (i.e., self-resetting) regime.

As shown in Fig. 1b, the device consists of a 3-layer stack. On the top of the stack is a resistor made from a thin film of normal metal with a small resistance (e.g. 1-50 Ohms). On the bottom of the stack is a meandered nanowire patterned from a superconducting thin film. The
**Figure 1.** High-impedance superconducting switch overview. (a) Scanning electron micrograph of one device (inset) closeup of the nanowire meander. (b) Schematic illustration of the device, showing the three primary layers (resistor, dielectric, and nanowire) as well as contact pad geometry. (c) Resistance data versus input power for several devices and circuit schematic for resistance measurement. Maximum resistance is proportional to device area, with devices 1-4 having areas 44, 68, 92, and 116 µm². (d) I-V curve of one device for three different input powers.
nanowire layer acts as a high-impedance, phonon-sensitive switch, while the resistor layer is used to convert electrical energy into Cooper-pair-breaking phonons. Like related low-impedance thermal devices, between these two layers is a dielectric thermal spacer that has two purposes: (1) thermally coupling the resistor layer to the nanowire layer, and (2) electrically disconnecting the input (resistor) from the output (nanowire switch). The device has four terminals total, with two of the terminals connected to the resistor and two of the terminals connected to the nanowire, as shown in Fig. 1.

The device begins in the “off” state where there is no electrical input to the resistor and the nanowire has a small current-bias. To transition to the “on” state, a voltage or current is applied to the input terminals of the resistor and thermal phonons are generated. The thin dielectric carries phonons generated from the resistor to the nanowire. Phonons with energy \( > 2\Delta \) break Cooper pairs within the nanowire, destroying the superconducting state of the nanowire. Once the superconducting state has been completely destroyed in the entire nanowire, the device is in the on state.

Analogously, this process can be described in terms of an effective temperature: the dielectric layer is thin enough that the phonon systems between the nanowire and the resistor are tightly coupled, meaning the phonon temperature in the nanowire is closely tied to the temperature of the resistor. When enough electrical power is delivered to the resistor, the nanowire is driven above its critical temperature and becomes normal. Since the resistor uniformly generates heat over its area, the entire nanowire is converted from the superconducting state to the resistive state at once, meaning the switch jumps to \( > 1M\Omega \) without any in-plane hotspot-growth delay. Once the device
has switched, current is then driven into the high-impedance output load and a large voltage can be generated.

1 Experimental results

DC impedance measurement When characterizing a switch, of primary importance is its on and off resistance. We measured the steady-state behavior of the switch by applying power to the resistor inputs of several devices and measuring the nanowire resistance with an AC resistance bridge. As can be seen in Fig. [1] each device remained at zero resistance until a critical surface power $P_c$ was reached. When more than $P_c$ was applied to the resistor, the resistance of the underlying nanowire increased rapidly, ultimately saturating at the normal-state resistance of the device. One potential concern was that phonons from the resistor could escape in-plane (e.g. out through the thick gold leads), resulting in wasted power. This type of edge power loss would scale with the length of the edge, and so we measured $P_c$ for devices of several sizes. However, by dividing each device’s $P_c$ by its active area $A$, we found that the devices had critical surface power densities $D_c = P_c/A$ of $21.0 \pm 0.6 \text{nW/µm}^2$. This means power loss through edge effects (e.g. along the substrate plane or into the gold contacts) did not play a role at the scale of device measured here, see the Supplementary Information for more details. As shown in Fig. [1c], the resistance of each device continues to increase beyond $P_c$ – this was likely due to non-uniform dissipation within the resistor element creating local temperature variation. Note that performing this measurement with a low-power measurement technique (such as an AC resistance bridge) was critical in order to limit Joule heating from current passing through the nanowire element. In this experiment, we applied a maximum of 10 nA ($\sim\text{100 pW}$) in order to guarantee that the nanowire
was not heated by the measurement process. The WSi film used for the nanowires had a $T_c$ of 3.4 K, and all measurements were taken at a base temperature of 0.86 K.

**Driving a cryogenic LED** As a means of demonstrating the superconductor-semiconductor interface, we used the switch to dynamically enable a cryogenic LED in a photonic integrated circuit (PIC) using only a low-level input voltage. Shown in Fig. 2, the output from the switch was wirebonded to a PIC that had an LED which was waveguide-coupled to a superconducting nanowire single-photon detector (SNSPD). The switch translated the 50 mV input (Fig. 2b) signal into 1.12 V at the output, enabling and disabling the LED in a free-running mode. Photons produced by the LED were coupled via waveguide into the detector, producing clicks on the detector output (Fig. 2c). The on-state input power of this device was 94.0 µW (55.9 nW/µm²), generating an on-state resistance of approximately 400 kΩ. We note these particular LEDs had a low overall efficiency ($\sim 10^{-6}$ as characterized in Ref. 22), and so the required input power and driving current were necessarily large. Steady-state behavior of the circuit is shown in Fig. 2d, which characterizes the detector response with the switch input power above and below the $D_c$ threshold. We additionally verified that the counts measured on the detector were in fact photons generated by the LED—not false counts due to sample heating or other spurious effects—by reducing the LED bias below threshold and observing no clicks on the detector output, and also by quadrupling the switching input power and observing no heating-induced change in count rate.
Figure 2. Using the switch to drive a photonic integrated circuit at 1 K: powering a cryogenic LED with the switch and reading out the generated light using a waveguide-coupled single-photon detector. (a) Schematic and circuit setup of the experiment (b,c) Switch input and detector output versus time. When $v_{in}$ is high, photons generated by the LED are transmitted via waveguide to a superconducting nanowire single-photon detector, producing detection pulses. (inset) Zoom-in of the detector output pulses. (d) Detector count rates for the experiment with the LED on (red) and off (blue).

Step response We also characterized the transient properties of the device when driving high-impedance loads by placing a 8.7 kΩ on-chip resistor at the output of the device. In this experiment, we applied voltage pulses to the resistor input with a pulse generator and measured the device output, while applying a current bias to the nanowire either below the retrapping current (Fig. 3, red data), or near the critical current (Fig. 3, cyan data). As seen in the circuit diagram of Fig. 3 an output voltage could only be generated when the switch reached a significant resistance ($\gg 1k\Omega$) allowing us to probe the impedance transition of the device. The results from this experiment, shown in Fig. 3, showed that the device could turn-on from its low-impedance state to its high-
impedance state below 300 ps, characterized by a energy-delay product on the order of \( \sim 100 \text{ aJ} \) per square micrometer of device area.

\[
\begin{align*}
\text{Time (ns)} & \quad \text{Power density (nW/\(\mu\text{m}^2\))} \\
0 & \quad 0.18 \text{ fJ/}\mu\text{m}^2 \\
10 & \quad 0.10 \text{ fJ/}\mu\text{m}^2 \\
30 & \quad 
\end{align*}
\]

\( i_b = 3.6 \mu\text{A} \)

\( i_b = 0.8 \mu\text{A} \)

Figure 3. Driving an 8.7 k\( \Omega \) load using the switch. (a) Turn-on delay \( \tau_{\text{on}} \) versus applied input power when the nanowire is biased below the retrapping current (blue, 0.8 \( \mu\text{A} \) bias) and near \( I_c \) (red, 3.6 \( \mu\text{A} \) bias)—the energy-delay product is bias-dependent. (b) Output produced by a 10-ns-wide square pulse to the heater with input surface power density \( D = 50 \text{ nW/}\mu\text{m}^2 \), highlighting the latching and non-latching regimes. Trace data taken with a 1 GHz bandwidth-limited amplifiers and oscilloscope.

Crucially, the impulse-response also demonstrates that this device can self-reset. As highlighted in Fig. [3a], when the nanowire is biased below the retrapping current, it becomes non-hysteretic and returns to the zero-voltage (superconducting) state after the input is turned off. The logic follows simply: below the retrapping current, the self-heating caused by the nanowire bias current does not generate enough power to keep the wire above \( T_c \). Thus, when the additional heating from the resistor is removed, the nanowire is forced back into the superconducting state. This non-latching property is in contrast to existing thin-film nanowire devices previously developed,
and is critical to guarantee device reset in e.g. unclocked systems. We note that even in this regime, there is still a thermal recovery time constant for the device to transition from the normal (on) to superconducting (off) state. We found that fall time was on the order 10 ns, which is consistent with the thermal recovery time constants previously reported for WSi. Additionally, it should be noted that although the nanowire fabricated here has a very high kinetic inductance, the L/R time constant of the switch—that could potentially limit the rise time of the current output—is not a limiting factor. When the device transitions from low- to high-impedance, the expected $\frac{L}{R_s}$ is equal to 0.39 ps.

**Device response below $D_c$** To better understand the response of the device below the critical surface power density $D_c$, we measured the nanowire critical current as a function of power applied to the resistor. The result of this characterization is shown in Fig. 4. For each datapoint, we applied a fixed amount of electrical power to the input resistor and measured the critical current of the nanowire several hundred times, taking the median value as $I_c(P)$. We then extracted an effective temperature for the nanowire by numerically inverting the Ginzburg-Landau relation

$$I_c(t) = I_{c0}(1 - t^2)^{3/2}(1 + t^2)^{1/2}$$

where $I_{c0}$ was the critical current at zero applied power and $t$ was the normalized temperature of the device $T/T_c$ (for this material, the $T_c$ was measured to be 3.4 K).

The data in Fig. 4 show that there is a non-linear relationship between the nanowire temperature and the applied heating power. Under the assumption that in-plane phonon loss remains low, this indicates that the thermal resistance of the underlying substrate is changing with the nanowire temperature. These effects are corroborated in the literature, which suggests that the majority of the thermal resistance of a thin film on a substrate is in the interfacial boundary resistance.23
Critical current and inferred temperature versus input power density. As the input power density is increased, the effective temperature of the meander rises, and its critical current is reduced. The small discontinuity is an experimental artifact from measuring very small critical current values.

2 Analysis and discussion

Although a complete treatment of the dynamics of the device will require a thorough analysis of the coupled electron and phonon systems between the thin films in the material stack, we found that the device behaved approximately as a thermal capacitor in parallel with a thermal resistor. We extracted values of this capacitance and resistance from Fig. 4 and Fig. 3. From that data, we found that the thermal boundary resistance was $1.24 \times 10^{-4} \text{ m}^2 \text{K/W}$, and the thermal capacitance per unit area was $6.87 \times 10^{-5} \text{ J/m}^2 \text{K}$. These values of $R_{th}$ and $C_{th}$ also imply an $R_{th}C_{th}$ intrinsic cooling time of 8.6 ns, which is in accordance with the results of Fig. 3 as well as literature values from WSi-based superconducting nanowire single photon detectors.

A useful figure of merit for these devices is $P_V$, the output voltage generated per unit input power while the switch is on. Due to proportionalities between the device resistance and area, and also between nanowire width and $I_c$, this figure of merit is area- and shape-independent—it depends
only on the materials used and the nanowire configuration. We calculated $P_V$ by first noting that the power required to heat the full area $A$ of a given device was $D_c A$. For a device with nanowires of width $w$, thickness $t$, and fill-factor $f$, the amount of switching resistance generated in that area is $R_s f A/w^2$, where $R_s$ is the nanowire normal-state sheet resistance. For the WSi material used here, the bias current density $J$ was $1.6 \times 10^9$ A/m$^2$ (non-latching) or $7.2 \times 10^9$ A/m$^2$ (latching), and $R_s$ was $590$ Ω/sq. The resulting voltage generated per unit power is then $R_s f J/w^2 D_c$ (thus, independent of device area), and so for the devices characterized in Fig. 1 $P_V$ was 0.72 mV/nW (non-latching) or 3.24 mV/nW (latching).

One potential area of concern when using this device as a switch is the power usage from current-biasing the device. Typically, a current-bias capable of driving high voltages require a large amount static energy dissipation: when using a resistor or MOSFET-based current source as a current bias, to achieve a maximum voltage of $V_{\text{max}}$ will generally require $I_b V_{\text{max}}$ of static power. However, for these devices a better approach will be to use inductive biasing to generate the high-impedance current bias. Superconducting thin films such as the one used here lend themselves particularly well to the generation of large inductances in compact areas, due to their large kinetic inductance. For instance, to generate a 200 mV swing on a CMOS input capacitance of 5 fF requires a bias current of 50 µA being carried by an 80 nH inductor – a trivial amount of inductance to generate with a superconducting nanowire. More importantly, the inductor can be charged only when needed, using a low voltage superconducting element such as a Josephson junction.
3 Conclusion and outlook

This device has a number of favorable features as a communications device between superconducting and semiconducting elements: it provides switch impedances $>1\,\text{M}\Omega$, input-output isolation, low turn-on time, and low-power operation with zero passive power required. Even with the reset-time limitations presented by thermal recovery, this switch has particular applicability for driving optoelectronics on a cryogenic stage such as LEDs or modulators. In applications such as quantum photonic feed-forward experiments or low-power neuromorphic hardware\cite{5}, clicks from efficient superconducting detectors need to be converted to optoelectronic-compatible signals, and a nanosecond-scale thermal recovery is acceptable as long as the initial response is fast. We note for these type of applications, it may be best to configure the device geometry to minimize propagation delay – the propagation delay for powering an LED to 1 V will be much smaller if 1 mA is driven across a switch of 1 kΩ, rather than driving 1 µA across 1 MΩ. It may also be helpful to drive the device with another superconducting three-terminal device\cite{24}, as these can present a purely non-resistive superconducting input and be fabricated in the same step as the nanowire meander.

Looking forward, there are a number of practical methods to enhance the operation of this device, depending on what tradeoffs are acceptable in a given application. The simplest would be to use multiple layers of nanowire; for instance, the on-resistance could be effectively doubled by adding an additional nanowire meander underneath the first (at some minor turn-on energy cost). If power usage is a concern, the on-state power requirements could be decreased by placing the device on a membrane. This would greatly increase the thermal resistance, reducing overall energy cost.
at the cost of increasing the thermal turn-off time. For higher operational frequencies, a different nanowire material could be used (e.g. NbN for a \(\sim 1\) ns thermal reset time). Finally, this device does not fundamentally need to be a thermal device as any method of inducing a phase change in a superconducting film – for instance, utilizing an electric-field induced superconductor-to-insulator transition\(^{25}\) – could be operated equivalently.
**Figure 5.** Design and results of edge-leakage test. (a) Geometry of the edge-leakage test, showing a narrow resistor element (red) routed through the middle of a large nanowire meander (black). (b) Power vs resistivity of edge-leakage test.

**Supplementary information**

In order to determine whether the device had significant in-plane heating, we designed a device with a narrow heater-resistor centered in a nanowire meander. The geometry can be seen in Fig. 5a. In this experiment, we applied power to the resistor and measured the resulting resistance of the nanowire meander. The results, shown in Fig. 5b, indicate that there is very little in-plane heating: at powers around $D_c$, we see a resistance in the nanowire form that is equivalent to the superconducting material directly underneath the resistor becoming normal. Only at much greater applied powers ($\sim 1$ mW) does this resistance increase significantly indicating that a much greater amount of power is necessary to heat the superconducting material in the neighborhood of the resistor.

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Competing Interests  The authors declare that they have no competing financial interests.
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