DepthNet: Real-Time LiDAR Point Cloud Depth Completion for Autonomous Vehicles

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Abstract—Autonomous vehicles rely heavily on sensors such as camera and LiDAR, which provide real-time information about their surroundings for the tasks of perception, planning and control. Typically, a LiDAR can only provide sparse point cloud owing to a limited number of scanning lines. By employing depth completion, a dense depth map can be generated by assigning each camera pixel a corresponding depth value. However, the existing depth completion convolutional neural networks are very complex that requires high-end GPUs for processing, and thus they are not applicable to real-time autonomous driving. In this paper, a light-weight network is proposed for the task of LiDAR point cloud depth completion. With an astonishing 96.2% reduction in the number of parameters, it still achieves comparable performance (9.3% better in MAE but 3.9% worse in RMSE) to the state-of-the-art network. For real-time embedded platforms, depthwise separable technique is applied to both convolution and deconvolution operations and the number of parameters decreases further by a factor of 7.3, with only a small percentage increase in RMSE and MAE performance. Moreover, a system-on-chip architecture for depth completion is developed on a PYNQ-based FPGA platform that achieves real-time processing for HDL-64E LiDAR at the speed 11.1 frame per second.

Index Terms—LiDAR, point cloud, depth completion, convolutional neural network, FPGA

I. INTRODUCTION

In recent years, autonomous vehicles have become a rapidly evolving technology that may revolutionize mobility and transportation systems. To accurately sense vehicle surroundings, cameras are often employed to provide a 2D description of the space. However, in order to transition into the 3D space, two options are usually employed, RGB-D cameras or LiDARs. Nevertheless, limited by the short range (around 10 meters) and weak energy, RGB-D cameras are mostly suited for indoor applications. On the other hand, modern LiDARs are capable of supplying accurate distance information up to 100 meters. In addition, LiDAR performance does not depend on the changes in lighting conditions. These advantages make LiDAR an ideal 3D sensor for outdoor applications such as autonomous vehicles.

One drawback of LiDAR sensor is its data sparsity: When mapping a Velodyne 64 line LiDAR HDL-64E point cloud to its corresponding high-resolution image obtained from a camera, only about 10% of the pixels have depth values. Especially, when laser scan lines encounter transparent or reflective surfaces such as car windows, the depth values are void. Therefore, depth completion is an important task that is aimed to data sparsity problem by generating a complete depth map for every pixels in the camera image and also making corrections of some void values. It is somewhat similar to an interpolation process, but we have to consider the feature of the objects in the 3D point cloud. Depth completion results a dense and precise depth map. When combined with RGB images, depth completion makes it possible for an autonomous vehicle to detect objects in 3D space and predict their movement accurately.

Most of the existing depth completion methods are based on convolutional neural networks (CNNs) that are very complex and can only run on high-power GPUs, such as Nvidia GTX 2080Ti, TITAN X, etc. Considering the limited power supply available in an autonomous vehicle, CNNs targeted on a real-time embedded platforms are much desirable. This calls for a novel CNN architecture with orders of magnitude reduction in the number of parameters and operations while maintaining a comparable performance. In this paper, we focus on addressing this important issue by introducing a two-stage learning method (coarse estimation stage and residual learning stage) and depthwise separable technique. Furthermore, we target the proposed efficient CNN architecture on a PYNQ-based MPSoC FPGA platform and demonstrate real-time LiDAR point cloud processing with superior operation-power ratio.

The contributions of this work can be summarized as follows:

1) A light-weight depth completion neural network is proposed with residual learning method. This neural network significantly reduces the number of parameters by a factor of 26.1, while achieves comparable error performance. Further optimization with depthwise separable technique, the number of parameters is decreased to only 0.53% of the state-of-the-art (SOTA) network [1]. The error performance result is comparable to that of SOTA when evaluating with the depth completion dataset.

2) An efficient hardware architecture is designed for the LiDAR depth completion network. In particular, deconvolution operations are implemented by avoiding all extra multiplication with zeros. By carefully balancing on-chip memory and multipliers, the FPGA implementation can execute the proposed depth completion neural network in real-time at 11.1 frames per second (fps).

3) A PYNQ-based LiDAR sensing and processing system is introduced. By migrating the Velodyne LiDAR driver...
to Linux system, one can use Python command to receive point cloud data and execute the depth completion neural network on hardware. An example work for VLP-16 LiDAR is open sourced and made available at https://github.com/linbaiwpi/VLP16_driver_on_PYNQ

II. RELATED WORK

In general, there are two classes of methods for the depth completion problem, namely classical methods and learning-based methods. The former ones utilize the traditional computer vision algorithms to complete the depth map. Unfortunately, most of them are applicable to RGB-D camera, which are not suitable for LiDAR point cloud. Ku [2] addressed the point cloud depth completion issue by using only basic computer vision operations such as dilation, smoothing, etc. This solution achieved comparable performance to some learning based methods even.

The other solution, learning-based methods, dominant the depth completion solutions, due to the huge success of deep learning for computer vision tasks. Chodosh et al. provided a solution for depth completion by combining compressed sensing and deep learning on Alternating Direction Neural Network (ADNN) framework [3]. Eldesokey et al. further designed a network composed by normalized convolution layer which only contains two channels, depth map and confidential map [4]. In contrast to specially designed convolution kernel above, Ma et al. [1] solved this problem by directly putting the raw sparse depth image into a large 34-layer network. This SOTA performance indicated the regular 2D convolution is able to solve the sparsity if the network is deep enough.

In addition, self-supervised learning methods were adopted recently aiming to avoiding the heavy manually labeling work. Ma further extended a self-supervised depth prediction framework to depth completion by feeding the sparse points into the network and treat them as the ground truth for corresponding pixels.

Because CNNs usually require huge computation capability which results in very high power consumption, tremendous research efforts have been dedicated to high-performance and low-power CNN accelerators for embedded devices such as FPGAs. In [5], the authors proposed a novel architecture for process element array. By exploring the design space, this design well balanced the computation capability and bandwidth requirement. Some works also focused on deconvolution. Liu et al. proposed one CNN architecture for segmentation, where convolution and deconvolution as two peripherals loaded on the system bus [6]. In [7], a high performance deconvolution module was proposed, in which reversed looping and stride hold skipping were employed to improve the performance. Some other implementations were targeted toward specific applications like autonomous driving [8] [9].

III. PROPOSED NEURAL NETWORK

Inspired by the residual learning [10] and the traditional computer vision method [2], we propose a two-stage solution to complete the sparse depth map. In the first stage, coarse depth information is predicted using distance transformation algorithm. And this raw result is further refined by a residual learning network. The entire deep learning framework is shown in Fig. [1]

A. Network Structure

In [2], the empty pixel is filled by dilation operation in very small local patches, which results in a reasonable estimation. This means the depth values of neighbouring pixels are probably very close to each other. Inspired by this finding, a nearest neighbor operation is applied to get a raw depth map before feeding it into the CNN, as a raw estimation of empty pixels. Distance transform, which has a linear complexity, is adopted as the method to find the nearest neighbor. Considering the accuracy of depth completion, a CNN is introduced to refine the raw estimation. Mathematically that is to find the residual error. The final depth map is the combination of raw estimation and residual error. The raw sparse depth map from LiDAR is the input. And then a raw estimation is generated by distance transform for CNN, who refines the raw estimation by finding the residual error. In the end, the final depth map is the raw estimation corrected by the predicted residual error.

The neural network structure is illustrated in Fig. [3] and detailed information (input and output size, channel depth) is listed in Tab. [I]. It is basically an encoder-decoder architecture. The encoder block structures are demonstrated in Fig. [2a]. Except the kernel size of 'conv_a_extra' is 1 × 1, the kernel size of the rest convolutions are 3 × 3. For encoder block 4, there is no feed forward line marked in red. Fig. [2b] illustrates the structure of decoder blocks, in which, the ‘upsample’ operation is deconvolution. Instead of using max pooling, all the down sampling in this network is done by convolution with strides equal to 2 in 'conv_a' and 'conv_a_extra'. The number of channels for each layer is indicated by 'Channel' column in Tab. [I].

B. Network Optimization

Different from the existing neural network based methods [3] [4] [11], the results from [1] concluded that a very deep regular convolution network can also complete depth maps very well. A deep ResNet architecture with 34 layers is utilized in their solution. However, the computation complexity of training ResNet-34 for high-resolution input images is too high to fit on a GeForce RTX2080 Ti GPU with 11GB graphic memory. Therefore, a much lighter structure similar to ResNet-18 is adopted in the encoder of our proposed CNN. By balancing the computation complexity and performance, ResNet-18 is easier to train and more suitable for mobile devices.

To further squeeze the proposed network, we applied the depthwise separable concept to both convolution and deconvolution. Depthwise separable convolution operation is exactly the same as the one used in MobilNetV2 [12]. Similarly, for depthwise separable deconvolution, input feature map has been convoluted for each channel separately. Subsequently, a pointwise convolution is applied to generate the output feature map.
Fig. 1: The deep learning framework for depth completion from LiDAR, where DT is distance transform and CNN is the neural network for residual error learning.

**Fig. 2:**
(a) is the structure of encoder block (block 4 has no feed forward marked in red) and (b) is the structure of decoder block.

### TABLE I: Structure of the proposed CNN (E = Encoder, D = Decoder)

| Name   | Input Size | Output Size | Channel(m,n,k) |
|--------|------------|-------------|----------------|
| In conv| 1216 × 256 × 1 | 1216 × 256 × 32 | 1216 × 256 × 32 |
| E block 1 | 1216 × 256 × 32 | 608 × 128 × 32 | 32, 32, 0 |
| E block 2 | 608 × 128 × 32 | 304 × 64 × 64 | 32, 64, 0 |
| E block 3 | 304 × 64 × 64 | 152 × 32 × 128 | 64, 128, 0 |
| D block 1 | 152 × 32 × 128 | 304 × 64 × 64 | 128, 64, 64 |
| D block 2 | 304 × 64 × 64 | 608 × 128 × 32 | 64, 32, 32 |
| D block 3 | 608 × 128 × 32 | 1216 × 256 × 32 | 32, 32, 32 |
| Out conv1 | 1216 × 256 × 32 | 1216 × 256 × 32 | 1216 × 256 × 32 |
| Out conv2 | 1216 × 256 × 32 | 1216 × 256 × 1 |

**C. Training**

The input feature map size is 256 × 1216 × 1, which is generated by following the methods mentioned in [13] [14]. As the output of CNN, residual error is normalized to [0, 1] as described in [1]. The empty region of output image is filled with the value on top of each line, like [2].

The proposed CNN is implemented by TensorFlow. During training, the batch size is set to 4, and number of epochs is 6. The initial learning rate is 10^{-4} with decreasing by a factor of 2 after each epoch. The CNN is trained using the loss of Mean Square Errors (MSE) and the Adam optimizer function. The training dataset is from KITTI dataset, depth completion task, which supplies collection of sparse LiDAR scans and corresponding semi-dense depth maps as ground truth. Totally, there are 85,898 scans as training samples, 1,000 scans as validation samples and 1,000 scans as test samples.

**D. Evaluation**

In Fig. 4, the performance of our proposed depth completion framework is illustrated. In the upper part of the figure, RGB image, sparse depth map projected from point cloud and the predicted dense depth map are pasted from top to bottom respectively. Based on RGB images and their corresponding predicted depth maps, the 3D RGB model is built and shown at the bottom of Fig. 4. The images and point clouds are all from KITTI depth completion dataset.

The predicted results are evaluated by the following 4 metrics:

1) RMSE: Root Mean Squared Error [mm]
2) MAE: Mean Absolute Error [mm]
3) iRMSE: RMSE of the inverse depth [1/km]
4) iMAE: MAE of the inverse depth [1/km]

The performance comparison between our proposed networks and the SOTA networks are given in Tab. II. Our network (without depthwise separable operation) is 9.3% better and 3.9% worse than the SOTA result [1], in terms of MAE and RMSE respectively. Considering their properties, the MAE represents the average error of the predicted depth map.

\[
MAE = \frac{1}{n} \sum |y_{\text{predict}} - y_{\text{true}}|
\]

While the RMSE is more sensitive to the pixels with large errors in the predicted depth map.

\[
RMSE = \sqrt{\frac{1}{n} \sum (y_{\text{predict}} - y_{\text{true}})^2}
\]

Fig. 3: The structure of proposed CNN.
Fig. 4: Illustration of the proposed depth completion framework performance. From top to bottom: 1) RGB image, 2) point cloud projected to image coordinate, 3) output of DepthNet using point cloud only, 4) 3D depth vision rebuilding.

Lower MAE but higher RMSE means that our network has less average error than that of [1], but has more pixels with large error. Besides, the number of parameters of our network is $9.73 \times 10^5$, which is only 3.8% of the SOTA network $2.54 \times 10^7$ [1].

To further squeeze the network for embedded platforms, we apply the depthwise separable (DS) technique to both convolutions and deconvolutions. This results in 12.8% higher in terms of RMSE and 2.3% less in terms of MAE. From the parameters number point of view, our network with DS requires $1.34 \times 10^5$ parameters. Comparing that of SOTA network, our network with DS reduces the number of parameters by a factor of 189.56. What’s more, the number of operations decreases accordingly. These reductions make this network more suitable for embedded platform in terms of computation complexity and bandwidth requirement.

### IV. Optimization for Hardware

#### A. Network Optimization

To further squeeze the proposed network, we applied the depthwise separable concept to both convolution and deconvolution. Depthwise separable convolution operation is exactly the same as the one used in MobilNetV2 [12]. Similarly, depthwise separable deconvolution completes the operation in two steps as well. The input feature maps have been deconvoluted for each channel separately (depthwise operation). Subsequently, a pointwise convolution is applied to generate the output feature map (pointwise operation). Fig. 5 illustrates the procedures for depthwise separable convolution and deconvolution. During depthwise operation in Fig. 5(a), the operations are not the same as in convolution and deconvolution. Besides, the output feature map size doubles the input size in deconvolution, while they are the same in convolution. Both convolution and deconvolution share the same pointwise operation.

When comparing with their standard counterparts, the parameters number for both convolution and deconvolution consume only $\frac{1}{C_o} + \frac{1}{K^2}$.

$$withoutDS = \frac{K \cdot K \cdot C_i + 1 \cdot C_i \cdot C_o}{K \cdot K \cdot C_i \cdot C_o} = \frac{1}{C_o} + \frac{1}{K^2}$$

#### B. Loop Optimization

Since all standard convolutions are replaced by depthwise separable convolution. The ordinary loop optimization are
(a) Step 1: depthwise operation, for DSC, OP is convolution, and for DSD, OP is deconvolution

(b) Step 2: pointwise operation, for both DSC and DSD, OP is convolution

Fig. 5: Operation comparison between depthwise separable convolution (DSC) and depthwise separable deconvolution (DSD)

down-graded into 3 level nest loops for both depthwise convolution (Alg. 1) and pointwise convolution (Fig. 2) [15]. Concerning to depthwise separable deconvolution, both depthwise and pointwise operations share the same loops as their convolution counterparts. The only difference is the kernel size in depthwise operation [16].

1) depthwise operation: Recalling our previous work [16], convolution and deconvolution could share the same process element if loop 1 is completely unrolled. Besides, limited by number of multipliers and BRAMs on FPGA, the input feature maps are partitioned and processed sequentially. In addition, the loop 3 is partially unrolled. Loop 2 remains intact.

Algorithm 1 Loops for depthwise operation

```
for no in Nof do ▷ channel,loop-3
  for (y,x) in (Noy, Nox) do ▷ feature map,loop-2
    for (ky,kx) in (K,K) do ▷ kernel,loop-1
      F_{out}[no,y,x] += F_{in}[no,y-ky,x-kx] * K[no,ky,kx]
```

2) pointwise operation: The \(1 \times 1\) convolution is mathematically matrix multiplication, which is a 3 cascaded loops. To share the same feature map buffers with depthwise operations, the loop 1 is partially unrolled with the same partition factor as depthwise loop 3.

C. Deconvolution Optimization

As a learnable technique for upsampling, deconvolution is widely used in depth completion tasks. A naive deconvolution operation is demonstrated in Fig. 6 where a convolution unit is reused. This naive deconvolution consists of the following two steps:

1) feature map padding: the input feature map is padded from \(IF_w \times IF_h\) to \((2 \cdot IF_w + 1) \times (2 \cdot IF_h + 1)\). The padded zeros are marked in blue and white in Fig. 6. The blue zeros are compulsory twice the size is required.

2) convolution: applying the convolution to the padded feature map.

Fig. 6: Naive deconvolution using padding and convolution

Based on the description above, most of the computation are wasted in multiplication by zeros. Avoiding these meaningless multiplication will boost the deconvolution speed dramatically.

An efficient deconvolution method is utilized in this paper. Concerning to the same task in Fig. 6, the equations are presented in (1)-(4) accompanied by Fig. 7. The procedure is divided into three steps [16]:

1) padding input feature map: extra top row and left column is required
2) scanning the padded feature map by sliding window in \(2 \times 2\)
3) applying the equations to generate output feature map by \(2 \times 2\) patch

Algorithm 2 Loops for pointwise operation

```
for no in Nof do ▷ output channel,loop-3
  for (y,x) in (Noy, Nox) do ▷ feature map,loop-2
    for ni in Nif do ▷ input channel,loop-1
      F_{out}[no,y,x] += F_{in}[ni,y,x] * K[no,ni]
```

Fig. 7: Optimization of deconvolution [1]
\[ OF_{11} = IF_{11} \cdot K_{11} + IF_{12} \cdot K_{13} + IF_{21} \cdot K_{31} + IF_{22} \cdot K_{33} \] (1)
\[ OF_{12} = IF_{12} \cdot K_{12} + IF_{22} \cdot K_{32} \] (2)
\[ OF_{21} = IF_{21} \cdot K_{21} + IF_{22} \cdot K_{23} \] (3)
\[ OF_{22} = IF_{22} \cdot K_{22} \] (4)

Three examples marked in red, green and blue squares respectively are represented in Fig. 7. By using this, most multiplication by zeros are saved, only the padded \( IF_W + IF_H + 1 \) zeros.

V. SYSTEM ARCHITECTURE

The entire deep learning framework as shown in Fig. 1 for depth completion is partitioned and assigned into ARM processor and FPGA logic. The data capturing and distance transform are handled by OpenCV running on the ARM processor, while the CNN inference part runs on the FPGA logic.

A. Software Task

The ARM processor prepares the sparse depth map for the CNN on FPGA side. This contains three steps:

1) Point cloud capturing: The Velodyne LiDAR driver is implanted as Linux dynamic library and ARM runs the driver to capture point cloud periodically.
2) Sparse depth map generation: It projects the 3D LiDAR coordinate into 2D camera coordinate. Mathematically, this process is matrix multiplication (Fig 8).
3) Distance transform: as mentioned before, it supplies a raw estimation for CNN.

![Fig. 8: Sparse depth map generation, which is coordinate projection from LiDAR to camera](image)

B. Hardware Overview

The CNN inference accelerator consists of the following three parts: 1) Process Engine (PE) computing pointwise convolution, depthwise convolution and deconvolution, and activation function LeakyReLU; 2) Buffers for weights, bias and intermediate feature maps; 3) Control logic which determines the data routing between DDR memory and buffers, between PE and buffers, etc.

1In TensorFlow, deconvolutions require the kernel rotated 180° before calculating. However, there is no rotation action in this example for easier description.

C. Process Engine

According to the structure of neural network in Tab. 1 and Fig. 2 all the operations can be categorized into the following three types: depthwise convolution \( 3 \times 3 \) (including strides=1 and 2), pointwise convolution \( 1 \times 1 \) (including strides=1 and 2), and depthwise deconvolution \( 3 \times 3 \). These three operations are implemented into three separated computing blocks. Input feature maps are fed to the corresponding block by dispatcher according to a pre-defined routine. The structure of computing engine is shown in Fig. 9.

![Fig. 9: Structure of process engine. The upper one is pointwise convolution (pw_conv), the middle one is depthwise convolution (dw_conv) and the bottom one is depthwise deconvolution (dw_deconv).](image)

1) Pointwise convolution: Since pointwise convolution (or \( 1 \times 1 \) convolution) is literally vector matrix multiplication, 32 multiplier arrays (size=32×1) with corresponding 1 sum-32 adder tree and 1 accumulator for each array are implemented in PE. Theadders in this block have higher precision than adders in other computing blocks.

2) Depthwise convolution: Depthwise convolution block utilizes the conventional architecture. 32 multiplier arrays (size=3×3) together with 32 sum-9 adder trees formed the depthwise convolution block.

3) Depthwise deconvolution: The implementation of depthwise deconvolution unit reuses the structure described in Sec. IV-C. The differences between deconvolution block and convolution block is 1) the patch of input feature map is \( 2 \times 2 \) instead of \( 3 \times 3 \) and 2) output 4 elements sequentially instead of 1.

4) Activation Functions: The activation function used in this neural network is Leaky ReLU, whose mathematical expression is

\[ O_{\text{LeakyReLU}} = 0.2 \times \min(x, 0) + \max(x, 0) \]

This design can be easily extend to support other activation functions similar to this one, like ReLU, ReLU6 and etc.
D. Memory Mapping

1) Buffer for parameters: Benefiting from the depthwise separable concept, the total number of parameters are reduced to less than 150K. This makes the parameters loading time reasonable low. Considering the parameter size for on-chip memory is still large, to balance the loading time and resource consumption, on-chip memory for half of the parameters are assigned.

2) Buffer for feature maps: Due to the relative large size of the feature maps and limitation of available on-chip memory, efficient mapping to reduce data communication is necessary. Partial unrolling results in loading same feature maps multiple times, which consequently requires higher memory bandwidth. To alleviate the burden, 10 feature map buffers with size $152 \times 32 \times 32$ are mapped. So that for layers whose channel is less than 256, no data transmitting is needed.

![](image1)

Fig. 10: Extra buffer for pointwise convolution

Besides, one extra feature map buffers with same size but higher precision (or longer bitwidth) is mapped also. They are used for pointwise convolution only, aiming to decrease the precision loss (Fig. 10).

VI. RESULTS AND DISCUSSION

This system has been implemented based on PYNQ open source framework running on Xilinx ZCU104 Development Kit. The test setup is demonstrated in Fig. 11, where LiDAR is connected to ZCU104 board via Ethernet cable. Velodyne LiDAR driver has been modified and loaded into Linux OS as dynamically linked shared object libraries. Users can send Python commands to the ARM processor who receives point cloud from LiDAR and stores it into DDR after pre-processing.

![](image2)

Fig. 11: The overview of test setup

Before sending images into FPGA side, the ARM processor also does DT on the input point cloud. The software and hardware partitioning is illustrated in Fig. 12 When running at 200 MHz, this CNN accelerator can process 1 frame of point cloud within 90.1ms. The total number of operations in this CNN inference is $15.14G$. Therefore, this accelerator achieves the computational capacity at $168.1GOPS$.

![Fig. 12: Hardware and software partitioning in time series](image3)

The hardware resource consumption is summarized in Tab. III. The bottleneck of this design is DSP resources, 98.1% of whom are mapped. Increasing the parallelism results in a large number of extra DSP slice utilisation. Besides, due to the large feature map size, around 87.5% on-chip memory, including both BRAM and URAM, are utilized to buffer as much feature maps or parameters as possible.

| name        | FF   | LUT  | DSP    | BRAM | URAM |
|-------------|------|------|--------|------|------|
| FM buffer   | 0    | 0    | 0      | 0    | 84   |
| weight buffer | 0    | 0    | 0      | 384  | 0    |
| dw conv     | 49559| 55209| 288    | 64   | 0    |
| dw deconv   | 49558| 55208| 288    | 64   | 0    |
| pw conv     | 24624| 36182| 1057   | 2    | 0    |
| others      | 3611 | 5261 | 64     | 31   | 0    |
| Total       | 127352| 151860| 1695   | 545  | 84   |

| name        | FF   | LUT  | DSP    | BRAM | URAM |
|-------------|------|------|--------|------|------|
| FM buffer   | (27.6%)| (65.9%)| (98.1%)| (87.3%)| (87.5%)|
| weight buffer | (0%)  | (0%)  | (0%)   | (98.1%)| (87.5%)|
| dw conv     | (1.8%)| (3.6%)| (0.3%) | (1.2%)| (0.3%)|
| dw deconv   | (1.8%)| (3.6%)| (0.3%) | (1.2%)| (0.3%)|
| pw conv     | (7.3%)| (11.7%)| (3.1%) |
| others      | (0.3%)| (0.5%)| (0.2%) |
| Total       | (27.6%)| (65.9%)| (98.1%)| (87.5%)|

VII. CONCLUSION

In this paper, we first propose a light-weight CNN namely DepthNet for the task of LiDAR point cloud depth completion. When comparing to state-of-the-art networks, DepthNet achieves similar error performance but only uses 3.8% of parameters. Targeted for low-power embedded platforms such as autonomous vehicles, we further optimize the network with depthwise separable technique, which reduces the number of parameters by another factor of 7.3 at the cost of small degradation in error performance. Furthermore, we develop an FPGA system-on-chip that receives LiDAR data as input and produces dense depth maps. When evaluating with Velodyne HDL-64E LiDAR, it successfully demonstrates efficient and precise LiDAR depth completion at 11.1 fps that meets the real-time requirement for autonomous vehicles.

REFERENCES

[1] F. Ma, G. V. Cavalheiro, and S. Karaman, “Self-supervised sparse-to-dense: self-supervised depth completion from lidar and monocular camera,” in 2019 International Conference on Robotics and Automation (ICRA). IEEE, 2019, pp. 3288–3295.

[2] J. Ku, A. Harakeh, and S. L. Waslander, “In defense of classical image processing: Fast depth completion on the cpu,” in 2018 15th Conference on Computer and Robot Vision (CRV). IEEE, 2018, pp. 16–22.

[3] N. Chodosh, C. Wang, and S. Lucey, “Deep convolutional compressed sensing for lidar depth completion,” in Asian Conference on Computer Vision. Springer, 2018, pp. 499–513.
[4] A. Eldesokey, M. Felsberg, and F. S. Khan, “Propagating confidences through cnns for sparse data regression,” arXiv preprint arXiv:1805.11913, 2018.

[5] C. Zhang, P. Li, G. Sun, Y. Guan, B. Xiao, and J. Cong, “Optimizing fpga-based accelerator design for deep convolutional neural networks,” in Proceedings of the 2015 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, 2015, pp. 161–170.

[6] S. Liu, H. Fan, X. Niu, H.-c. Ng, Y. Chu, and W. Luk, “Optimizing cnn-based segmentation with deeply customized convolutional and deconvolutional architectures on fpga,” ACM Transactions on Reconfigurable Technology and Systems (TRETS), vol. 11, no. 3, pp. 1–22, 2018.

[7] X. Zhang, S. Das, O. Neopane, and K. Kreutz-Delgado, “A design methodology for efficient implementation of deconvolutional neural networks on an fpga,” arXiv preprint arXiv:1705.02583, 2017.

[8] Y. Lyu, L. Bai, and X. Huang, “Real-time road segmentation using lidar data processing on an fpga,” in 2018 IEEE International Symposium on Circuits and Systems (ISCAS). IEEE, 2018, pp. 1–5.

[9] J. Peng, L. Tian, X. Jia, H. Guo, Y. Xu, D. Xie, H. Lao, Y. Shan, and Y. Wang, “Multi-task adas system on fpga,” in 2019 IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS). IEEE, 2019, pp. 171–174.

[10] K. He, X. Zhang, S. Ren, and J. Sun, “Deep residual learning for image recognition,” in Proceedings of the IEEE conference on computer vision and pattern recognition, 2016, pp. 770–778.

[11] J. Uhrig, N. Schneider, L. Schneider, U. Franke, T. Brox, and A. Geiger, “Sparsity invariant cnns,” in 2017 International Conference on 3D Vision (3DV). IEEE, 2017, pp. 11–20.

[12] M. Sandler, A. Howard, M. Zhu, A. Zhmoginov, and L.-C. Chen, “Mobilenetv2: Inverted residuals and linear bottlenecks,” in Proceedings of the IEEE conference on computer vision and pattern recognition, 2018, pp. 4510–4520.

[13] W. Van Gansbeke, D. Neven, B. De Brabandere, and L. Van Gool, “Sparse and noisy lidar completion with rgb guidance and uncertainty,” in 2019 16th International Conference on Machine Vision Applications (MVA). IEEE, 2019, pp. 1–6.

[14] J. Tang, F.-P. Tian, W. Feng, J. Li, and P. Tan, “Learning guided convolutional network for depth completion,” arXiv preprint arXiv:1908.01238, 2019.

[15] Y. Ma, Y. Cao, S. Vrudhula, and J.-s. Seo, “Optimizing loop operation and dataflow in fpga acceleration of deep convolutional neural networks,” in Proceedings of the 2017 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, 2017, pp. 45–54.

[16] L. Bai, Y. Lyu, and X. Huang, “A unified hardware architecture for convolutions and deconvolutions in cnns,” in 2018 IEEE International Symposium on Circuits and Systems (ISCAS). IEEE, 2020, pp. 1–5.

[17] Xilinx Inc., “pynq.io,” 2016. [Online]. Available: www.pynq.io