Resistive communications based on neuristors

David Alejandro Trejo Pizzo

Abstract—Memristors are passive elements that allow us to store information using a single element per bit. However, this is not the only utility of the memristor. Considering the physical chemical structure of the element used, the memristor can function at the same time as memory and as a communication unit. This paper presents a new approach to the use of the memristor and develops the concept of resistive communication.

I. INTRODUCTION

The memristor is the fundamental non-linear circuit element, with uses in computing and computer memory. Memristors are basically a fourth class of electrical circuit, joining the resistor, the capacitor, and the inductor, that exhibit their unique properties primarily at the nanoscale.

Theoretically, a memristor is a concatenation of a memory and a resistor that maintains a relationship between the time integrals of current and voltage across a two terminal element. Thus, its resistance varies according to a memristance function.

The original definition of the memristor is derived from circuit theory: besides resistor, capacitor and inductor, there must exist a fourth basic two-terminal element that uniquely defines the relationship between the magnetic flux $\phi$ and the electric charge $q$ passing through the device, or

$$d\phi = M \ast dq$$

A. ReRAM

ReRAM (Resistive Random Access Memory) is a resistive switching memory proposed as a nonvolatile memory. The phenomenon of resistive switching has been observed in a wide variety of materials, however, the mechanism responsible for the switching behavior seems to differ between them. On the basis of I-V characteristic curves, switching behaviors can be classified into two types, unipolar (non-polar) and bipolar.

In unipolar resistive switching, the switching process depends on the amplitude of the applied voltage, but not on the polarity. This type of switching behavior has been observed in many binary metal oxides such as SiO, NiO and CuO.

A memory cell initially in a virgin state, ie prior to the application of any voltage pulse, is in a highly resistive state. When the application of a voltage pulse is high enough, it is put into the device in a low resistance state (LRS). This process is called forming. The rupture value of the dielectric of the material tells us approximately at what range of voltages we should find this threshold voltage for the forming process. After the forming process, the cell from an LRS state is switched to a high resistance state (HRS) by applying a threshold voltage (reset process). Changing from an HRS state to an LRS state is achieved by applying a
threshold voltage that is usually greater than the reset voltage, but less than the forming voltage. In the process of set and forming, the current is limited by the compliant current (Icc) of the control system or, more practically, by adding a series resistor acting as a voltage divider.

II. MEMRISTOR CIRCUITS

For almost fifty years, integrated electronic circuits built with semiconductor devices have provided significant growth in the number of processing elements and memory bits available to system developers.

This growth has provided orders of magnitude improvements in speed, power consumption, and reliability, together with significant reductions in the cost per device but trends like this are direct consequences of frequent miniaturization in the semiconductor fabrication process. According to "Moore Law" this will reach an end soon. When device sizes are no longer scalable, microelectronic technology needs innovations to support novel applications and here comes the memristor.

Memristors are used in hardware neural networks, both to implement different learning algorithms and back propagation. It is also used to build neuromorphic systems (hardware that mimics the brain). Memristors can also be used in analog circuits, for example as reconfigurable resistors to change the properties of the circuit. Another interesting application is the use of memristors as part of logic circuits.

III. RESISTIVE COMMUNICATIONS

We know that neurons communicate with each other through the small spaces between them, in a process known as synaptic transmission (where synapses are the connections between neurons). Information goes from one cell to another by neurotransmitters such as glutamate, dopamine or serotonin, which activate the receptors in the receiving neuron to transmit excitatory or inhibitory messages.

Three main types of synaptic transmission are distinguished. The first two mechanisms constitute the main forces governing the neural circuits and can be replicated using memristor circuits, from now on called "neuristors":

- Exciting transmission: one that increases the possibility of producing an action potential;
- Inhibitory transmission: that which reduces the possibility of producing an action potential;
- Modulating transmission: that which changes the pattern and / or frequency of the activity produced by the cells involved.

As it is shown in "A scalable neuristor built with Mott memristors" and in figure 5 a neuristor can be made with Mott memristors. The channels consist of Motts M1 and M2, each with a characteristic parallel capacitance (C1 and C2, respectively) and are biased with opposite polarity d.c. voltage sources.

A. The conduction mechanism

To support the general function of the nervous system, neurons have evolved unique capabilities for intracellular signaling (communication within the cell) and intercellular signaling (communication between cells). To achieve long distance, rapid communication, neurons have evolved special abilities for sending electrical signals (action potentials) along axons. This mechanism, called conduction, is how the cell body of a neuron communicates with its own terminals via the axon. Communication between neurons is achieved at synapses by the process of neurotransmission.
We can use the neuristor M to achieve this communication as it is shown in figure 6.

To begin conduction, a potential is generated near the cell body portion of the axon, here the Vin of the Q transistor. But whereas an electrical signal in an electronic device occurs because electrons move along a wire, an electrical signal in a neuron occurs because ions move across the neuronal membrane. Ions are electrically charged particles. The protein membrane of a neuron acts as a barrier to ions. Ions move across the membrane through ion channels, here nanowires in a dielectric thin layer, that open and close due to the presence of neurotransmitters.

When the concentration of ions on the inside of the neuron changes, the electrical property of the membrane itself changes. Normally, the membrane potential of a neuron rests as -70 millivolts (and the membrane is said to be polarized). The influx and outflux of ions (through ion channels during neurotransmission) will make the inside of the target neuron more positive (hence, de-polarized). When this depolarization reaches a point of no return called a Vthreshold, a large electrical signal is generated. This is the action potential.

This signal is then propagated along the axon (and not, say, back to its dendrites) until it reaches its axon terminals. An action potential travels along the axon quickly, moving at rates up to 150 meters (or roughly 500 feet) per second. Conduction ends at the axon terminals.

Axon terminals are where neurotransmission begins. Hence, it is at axon terminals where the neuron sends its Vout to other neurons. At electrical synapses, the Vout will be the electrical signal itself. Neuristors communicate with other neuristors with every set and reset action, changing the resistance level and forming nano wires that can save the memory of past memristance levels. This conduction mechanism is what I would like to call resistive communication.

B. A nanoscale communication protocol

Resistive communications is an approach to communicate between physical layers of neuristor with focus in creating neuromorphic circuits. To make this communication mechanism compatible with other nano devices it is essential to use a standard. A conceptual framework provides the organization and structure required to develop conceptual models of nanoscale communication. The IEEE Std 1906.1 Recommended Practice for Nanoscale and Molecular Communication Framework provides this precise, common definition of nanoscale communication and a general framework that balances concepts with broad applicability. This includes metrics, use-cases, and a reference model which it is followed here.

C. Reference model for molecular communications

The core of the simulator has been also extended to model molecular communications based on the pure diffusion process. The UML diagram of classes modeling the Molecular example. Also in this case, the diagram only reports the most important data members and functions, whereas some details about relationships among objects have been omitted.

It is assumed that molecules diffuse into the medium according to Brownian motion. In that hypothesis propagation of this pulse can be analytically modeled by Fick’s laws of diffusion, which expresses the concentration of molecules as a function of distance and time. In particular, the molecular concentration at any point in space is expressed in Equation

\[ c(r; t) = \frac{Q}{(4 \pi D t)^{3/2}} e^{-r^2/4Dt} \]

where

- \( c \) is the molecular concentration
- \( r \) is the distance between sender and receiver
- \( Q \) is the number of molecules released by the sender
- \( D \) is the diffusion coefficient
- \( t \) is the time variable

IV. CONCLUSIONS

The resistive communication presents a model on which to build neuromorphic networks that emulate the functioning of the electrical synapse and the communication of data between neurons. Much work remains to be done to build a
neuromorphic circuit that emulates brain functions, but we are closer to achieving small neural networks to physically build pattern recognition algorithms. The memristor and the neuristor construction are the ideal elements for its physical characteristics to build neural networks and emulate the electrical synapse using the resistive switching phenomenon.

REFERENCES

[1] Zheng Fan, Xudong Fan, A. Li and Lixin Dong, "Resistive switching in copper oxide nanowire-based memristor," 2012 12th IEEE International Conference on Nanotechnology (IEEE-NANO), Birmingham, 2012, pp. 1-4.

[2] Y. Zhang, Y. Li, X. Wang and E. G. Friedman, "Synaptic Characteristics of Ag/AgInSbTe/Ta-Based Memristor for Pattern Recognition Applications," in IEEE Transactions on Electron Devices, vol. 64, no. 4, pp. 1806-1811, April 2017.

[3] M. R. Agghadi, B. Linares-Barranco, D. Abbott and P. H. W. Leong, "A Hybrid CMOS-Memristor Neuromorphic Synapse," in IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 2, pp. 434-445, April 2017.

[4] H. Abnahila, D. Shehada, C. Y. Yeun, C. J. O'Kelly, M. A. Jaoude and B. Mohammad, "Novel microscale memristor with uniqueness property for securing communications," 2016 IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS), Abu Dhabi, United Arab Emirates, 2016, pp. 1-4.

[5] C. Liu, Q. Yang, C. Zhang, H. Jiang, Q. Wu and H. H. Li, "A memristor-based neuromorphic engine with a current sensing scheme for artificial neural network applications," 2017 22nd Asia and South Pacific Design Automation Conference (ASP-DAC), Chiba, 2017, pp. 647-652.

[6] S. Wang, W. Wang, C. Yakopicc, E. Shin, T. M. Taha and G. Subramanyam, "Memristor devices for use in neuromorphic systems," 2016 IEEE National Aerosp. and Electronics Conference (NAECON) and Ohio Innovation Summit (OIS), Dayton, OH, 2016, pp. 253-257.

[7] M. M. Dakeel, A. M. Hassanein, R. A. Fouad and A. G. Radwan, "Memristor-based data converter circuits," 2016 28th International Conference on Microelectronics (ICM), Giza, 2016, pp. 357-360.

[8] S. N. Truong, K. Van Pham, W. Yang and K. S. Min, "Memristor circuits and systems for future computing and bio-inspired information processing," 2016 IEEE Biomedical Circuits and Systems Conference (BioCAS), Shanghai, 2016, pp. 456-459.

[9] M. Khalid and J. Singh, "Memristor Crossbar-Based Pattern Recognition Circuit Using Perceptron Learning Rule," 2016 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS), Gwalior, 2016, pp. 236-239.

[10] I. Gupta, A. Seeb, A. Khiat and T. Prodromakis, "Towards a memristor-based spike-sorting platform," 2016 IEEE Biomedical Circuits and Systems Conference (BioCAS), Shanghai, 2016, pp. 408-411.

[11] J. Secco and F. Corinto, "Memristor-Based Binary Synapses for Deep Neural Networks," CNNA 2016; 15th International Workshop on Cellular Nanoscale Networks and their Applications, Dresden, Germany, 2016, pp. 1-2.

[12] A. Ascoli, R. Tetzlaff, L. O. Chua, J. P. Strachan and R. S. Williams, "DC behaviour of a non-volatile memristor: part I," CNNA 2016; 15th International Workshop on Cellular Nanoscale Networks and their Applications, Dresden, Germany, 2016, pp. 1-2.

[13] I. Vourkas, A. Abusleme, G. C. Sirakoulis and A. Rubio, "1-D Memristor Networks as Ternary Storage Cells," CNNA 2016; 15th International Workshop on Cellular Nanoscale Networks and their Applications, Dresden, Germany, 2016, pp. 1-2.

[14] L. V. Gambuzza, M. Frasca, L. Fortuna, V. Ntinias, I. Vourkas and G. C. Sirakoulis, "A new approach based on memristor crossbar for synchronization," CNNA 2016; 15th International Workshop on Cellular Nanoscale Networks and their Applications, Dresden, Germany, 2016, pp. 1-2.

[15] S. N. Danilin and S. A. Shchanikov, "The research of operation accuracy of a memristor-based artificial neural network with an input signal containing noise and pulse interference," 2016 Dynamics of Systems, Mechanisms and Machines (Dynamics), Omsk, 2016, pp. 1-5.

[16] A. Siemon, S. Ferch, S. Menzel, R. Waser and E. Linn, "Impact of Quantized Conductance Effects of ReRAM Devices on Neuromorphic Networks," CNNA 2016; 15th International Workshop on Cellular Nanoscale Networks and their Applications, Dresden, Germany, 2016, pp. 1-2.

[17] M. Prezioso et al., "Spiking neuromorphic networks with metal-oxide memristors," 2016 IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, QC, 2016, pp. 177-180.

[18] A. Ascoli, R. Tetzlaff, V. Lanza, F. Corinto and M. Gilli, "Memristor plasticity enables emergence of synchronization in neuromorphic networks," 2014 IEEE International Symposium on Circuits and Systems (ISCAS), Melbourne VIC, 2014, pp. 2261-2264.

[19] V. Erokhin, "Organic memristive devices: Architecture, properties and applications in neuromorphic networks," 2013 IEEE 20th International Conference on Electronics, Circuits, and Systems (ICECS), Abu Dhabi, 2013, pp. 305-308.

[20] O. Turel, I. Muckra and K. Likharev, "Possible nanoelectronic implementation of neuromorphic networks," Proceedings of the International Joint Conference on Neural Networks, 2003., 2003, pp. 365-370 vol.1.

[21] C. Liu, Q. Yang, C. Zhang, H. Jiang, Q. Wu and H. H. Li, "A memristor-based neuromorphic engine with a current sensing scheme for artificial neural network applications," 2017 22nd Asia and South Pacific Design Automation Conference (ASP-DAC), Chiba, 2017, pp. 647-652.

[22] A. Vandesompele, F. Walter and F. Rhrbein, "Neuro-evolution of spiking neural networks on Spinnaker neuromorphic hardware," 2016 IEEE Symposium Series on Computational Intelligence (SSCI), Athens, 2016, pp. 1-6.

[23] T. E. Potok et al., "A Study of Complex Deep Learning Networks on High Performance, Neuromorphic, and Quantum Computers," 2016 2nd Workshop on Machine Learning in HPC Environments (MLHPC), Salt Lake City, UT, 2016, pp. 47-55.