High-Frequency Tunable Grounded & Floating Incremental-Decremental Meminductor Emulator and Application

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Abstract

In this paper, a new design has been proposed for the realization of grounded and floating meminductor emulators built with two OTAs and two second-generation current conveyors. The proposed emulators can be configured in both incremental and decremental topology. This paper also proposes the application of meminductor as Amplitude Modulator (AM). The proposed circuits and its application claim that the circuit is much simpler in design and can be utilized in both topologies. The performance of all the proposed circuits has been verified with Cadence Virtuoso Spectre using standard CMOS 180nm. Furthermore, post-layout simulations and its comparison along with non-ideal and Monte Carlo analysis have been carried out in detail.

Index Terms: Current-mode circuits, Floating meminductor emulator, Grounded meminductor emulator, Incremental configuration, Decremental configuration, Pinched hysteresis loop

1. Introduction

Resistor, inductor, and capacitor were three traditional fundamental basic electrical elements; now memristor represents the fourth fundamental element. Memristor was postulated by Chua in 1971 [1] as the fourth basic electrical element but came into highlight only after HP in 2008 fabricated a memristor-based on thin-film TiO2. From then onward, there has been a boom of research in this field. In 1980 this postulation was then generalized to an infinite variety of basic circuit elements in [2] can be generalized into elements quadrangle. Chua’s circuit element quadrangle was then extended to propose higher-order
elements such as Memcapacitor and Meminductor. The meminductor provides a relationship between the charge $q$ and the time integral of flux $\rho$. Unlike capacitor and inductor, meminductor can store information for a very long time without power because of the non-volatility property it possesses. Although the device is still a theoretical concept, but emulators are essential to analyze the characteristics and study its applications. The ref. [3] gives a relationship on the doubly periodic table of circuit elements, also called the four elements torous in correlation with basic circuit element quadrangle consisting of all the four basic electrical elements. Furthermore, an extension of the memristive system to capacitive and inductive elements whose properties depend on the state and history of the system was presented in [4]. Physical characteristics analysis of these memory-based elements along with mathematical examples for memristor, meminductor, and memcapacitors were presented in [5-6].

Several circuits for emulating memristor-less meminductor are proposed in [7-11] while meminductor formed using mutators were proposed in [12-16]. Ref. [7] represents memristor-less current and voltage controlled meminductor emulator using a second-generation current conveyor (CCII), adder, multiplier and a number of passive components. A charge-controlled meminductor emulator using an inductor, Op-Amps, multiplier, transistors, and a number of other passive components was proposed in [8]. In 2014, a practical implementation of the meminductor using a very large number of active and passive components was proposed [9]. This proposed circuit consisted of 4 current feedback operational amplifiers (CFOAs), 1 buffer, 2 Op-Amps, 1 multiplier and some passive components making the circuit itself quite complex and bulky. A flux-controlled meminductor is proposed in [10], but it consists of many active blocks along with passive components. In 2017 a much simpler circuit for simulating meminductor and memcapacitor was proposed using multioutput OTA [11] but circuit uses an inductor and has a low frequency of operation. All the proposed circuits in [7-11] are complex and/or have a low frequency of operation which very much limit their practical use and possesses a severe limitation.

Another method of emulating meminductor is with mutators proposed in [12-16]. Mutator simulating second-order elements using its inherent relationship were proposed in [12-13] represented the simplified meminductor emulator using multiplier approach but the memristor used here is bulky,
complex, and has a low operating frequency. Mutator based on 1 CCII and 3 Op-Amp was proposed in [14] and a meminductor with mutator built using reduced components i.e., 2 CCII, 1 buffer, 1 resistor and 1 capacitor, was proposed in [15]. In 2014 a universal mutator using a large number of the active and passive components was also proposed in [16]. Apart from these mutators, the PSpice model of meminductor and its nonlinear model with its study on device parameters, variations were proposed in [17-18]. The topology in [19] gives detailed composite behavior in series and parallel topologies. Applications of meminductor such as chaotic oscillator and its dynamic studies were presented in [20-22]. Application as a low power filter design was also proposed in [23].

The paper proposes a meminductor emulator built with active blocks consisting of only two OTA and two-second generation current conveyors. The proposed memristor emulators possess the following important features: (i) simple circuitry, (ii) Grounded and floating configuration, (iii) option for both incremental and decremental configurations to increase the range of values of meminductance (MI), and also application flexibility, (iv) high-frequency range of operation, (v) electronic control of meminductance value in addition to the control by frequency and amplitude of the applied voltage signal across emulator.

2. Operational transconductance amplifier (OTA), Second generation Current Conveyor (CCII) and Second-generation current carrying Current Conveyor (CCCII) circuits.

![Circuit symbols of Operational Transconductance Amplifier (OTA), CCII and CCCII](image)

**Fig. 1.** Symbolic representation of (a) OTA, (b) CCII, (c) CCCII

Circuit symbols of Operational Transconductance Amplifier (OTA), CCII and CCCII are shown in Fig.1, while their respective CMOS implementation is shown in Fig. 2(a-c), respectively. $V_B$ controls
the transconductance gain ($G_m$) of the OTA while $I_b$ controls the internal resistance $R_X$ of CCCII which makes the circuit electronically tunable.

The output of an OTA given in Fig. 2(a) for an input $V_m$ is expressed as

$$I_{O_{2}} = \pm G_m V_m, \quad V_{in+} - V_{in-} = \text{differential input}$$

(1)

Where $G_m$ is transconductance of OTA. The routine analysis results in the expression of $G_m$ as

$$G_m = \frac{k}{\sqrt{2}} (V_B - V_{ss} - 2V_{th})$$

Here, $k$ is a parameter of MOS device given by

$$k = \mu_e C_{ox} \frac{W}{L}$$

The $W, L, \mu_e, C_{ox}$ and $V_{th}$ are respectively channel width, channel length, the mobility of the carrier, capacitance per unit area and the threshold voltage of MOS.
Fig. 2. CMOS implementation of (a) OTA circuit, (b) CCII circuit, (c) CCCII circuit

Fig. 2(b) represents the Second Generation Current Conveyor (CCII) whose ideal port relationship is given by

\[
\begin{bmatrix}
I_y \\
V_x \\
I_z
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 \\
1 & 0 & 0 \\
0 & \pm 1 & 0
\end{bmatrix}
\begin{bmatrix}
V_y \\
I_x \\
V_z
\end{bmatrix}
\]
Similar port relationship for Fig. 2(c) i.e. second generation current controlled current conveyor (CCCII) is given by

\[
\begin{bmatrix}
I_y \\
V_x \\
I_z
\end{bmatrix} = \begin{bmatrix}
0 & 0 & 0 \\
1 & R_x & 0 \\
0 & \pm 1 & 0
\end{bmatrix}\begin{bmatrix}
V_y \\
I_x \\
V_z
\end{bmatrix}
\]

Where, \( R_x \approx \frac{1}{\sqrt{2I_B C_{ov}}} \left( \frac{\mu_p W_p}{L_p} + \frac{\mu_n W_n}{L_n} \right) \)

Fig. 3(a-b) shows the frequency response of the OTA and Second-Generation Current Conveyor respectively.

![Frequency response](image)

**Fig. 3.** Frequency response of (a) Operational Transconductance amplifier, (b) Second generation current conveyor

### 3. Proposed grounded meminductor emulator circuit

Schematic diagrams of the proposed grounded and floating meminductor emulators are shown in Fig. 4 and Fig. 5, respectively. The Incremental and decremental nature of meminductor can be configured by switching mechanism among pins w, x, y, and z of circuits as given in Table 1. These mechanisms are applicable to both grounded and floating meminductor emulators.

**Table 1.** Connection topology for pins w, x, y, and z for two modes of operations.

| S. No. | Switch Connections | Mode of operation |
|--------|--------------------|-------------------|
| 1      | w-x; y-z           | Incremental       |
| 2      | w-z; y-x           | Decremental       |
3.1. Grounded meminductor emulator

The proposed grounded meminductor emulator is shown in Fig. 4. Considering incremental type meminductor emulator i.e., pins w, x and pins y, z are interconnected, the input current $I_{in}$ is obtained as

$$I_{in}(t) = I_{x1} = I_{z1} \quad \text{(by port relationship)}$$

Or, $I_{in}(t) = -I_{inB}$  \hspace{1cm} (2)

And $V_{y2} = V_{x2} - I_{x2}R_{x2}$ \hspace{1cm} (by port relationship)

$$V_{y2} = V_{inB} = -\frac{I_{x2}}{SC_2} - I_{x2}R_{x2} = -I_{x2}\left(\frac{1}{SC_2} + R_{x2}\right) \hspace{1cm} (3)$$

$$I_{x2} = I_{z2} = \frac{-V_{y1}}{R_1} = \frac{-Vin}{R_1} \quad \text{as} \ (V_{y1} = V_{x1} = V_{in}) \hspace{1cm} (4)$$

Substituting (4) in (3)

$$V_{in} = V_{inB}\left(\frac{SR_1C_2}{1+SC_2R_{x2}}\right) \hspace{1cm} (5)$$

Dividing (5) by (2)

$$\frac{V_{in}}{I_{in}} = \frac{V_{inB}R_1SC_2}{I_{inB}\left(1+SC_2R_{x2}\right)} \hspace{1cm} (6)$$

Bias voltage $V_{B3}$ is given by
\[ V_{B3} = \frac{1}{C_1} \int I_c(t) \, dt = \frac{G_m^4}{C_1} \int V_{Bin}(t) \, dt = \frac{G_m^4}{C_1} \left( \frac{1 + SC_2 R_{x_2}}{SR_1 C_2} \right) \int V_m(t) \, dt \]

\[ = \frac{G_m^4}{C_1} \left( \frac{1 + SC_2 R_{x_2}}{SR_1 C_2} \right) \phi_m \]  

(7)

where \( \phi_m = \int V_m(t) \, dt \) is the total flux obtained by meminductor.

Substituting (7) into (2), transconductance \( G_{m3} \) is obtained as

\[ G_{m3} = \frac{k}{\sqrt{2}} \left( V_{B3} - V_{ss} - 2V_m \right) = \frac{k}{\sqrt{2}} \left( \frac{G_m^4 (1 + SC_2 R_{x_2}) \phi_m}{SC_1 R_1 C_2} \right) - V_{ss} - 2V_m \]  

(8)

Also

\[ G_{m3} = -\frac{I_{O3}}{V_B} = \frac{I_{mb}}{V_{mb}} \]  

(9)

Using (9) and (8) results in an expression

\[ \frac{I_{mb}}{V_{mb}} = \frac{k}{\sqrt{2}} \left( \frac{G_m^4 (1 + SC_2 R_{x_2}) \phi_m}{SC_1 R_1 C_2} \right) - V_{ss} - 2V_m \]  

(10)

Substituting (10) in (6) gives meminductance of the proposed grounded incremental meminductor emulator is obtained as

\[ L_m = \frac{\phi_m}{I_m} = \frac{RC_2}{1 + SC_2 R_{x_2}} \]  

(11)

Similarly, the change of switch connections to w-z and y-x changes polarity of time variant part of meminductance of (11), resulting in a decremental type meminductance as

\[ \frac{\phi_m}{I_m} = \frac{RC_2}{1 + SC_2 R_{x_2}} \]  

(12)

Equation (10) and (11) can be rewritten as
\[
\frac{V_{in}}{I_{in}} = \frac{SR_{C2}}{\frac{k}{\sqrt{2}}(V_{ss} + 2V_{th}) + \frac{k}{\sqrt{2}}\left(\frac{G_{m4}(1 + SC_{2}R_{X2})}{SC_{1}R_{1}C_{2}}\right)1 + SC_{2}R_{X2}}
\]

(13)

As operating frequency is much less than \(\frac{1}{2\pi CR_{X2}}\) where \(RX_{2}\) is the resistance at input port X of CCII which is usually very low [28] so \((1 + SC_{2}R_{X2}) \approx 1\).

Equation (13) can then be simplified as

\[
L_{M}^{-1} = \frac{\phi_{in}}{I_{in}} \approx \frac{k}{\sqrt{2}R_{1}C_{2}}(V_{ss} + 2V_{th}) \pm \frac{k}{\sqrt{2}}\left(\frac{G_{m4}\phi_{in}}{SC_{1}R_{1}^{2}C_{2}^{2}}\right)
\]

(14)

In equation (13) \(G_{m4}\) can be controllable by external bias voltage \(V_{b4}\) and \(R_{X2}\) is controlled by external current \(I_{b}\) which makes proposed circuit electronically tunable. The equations (11) and (12) represent incremental and decremental meminductance respectively, where for a fixed operating frequency \(\frac{k}{\sqrt{2}R_{1}C_{2}}(V_{ss} + 2V_{th})\) is the constant term and \(\frac{k}{\sqrt{2}}\left(\frac{G_{m4}\phi_{in}}{SC_{1}R_{1}^{2}C_{2}^{2}}\right)\) being the time-varying term as \(\phi_{in}\) is the function of time varying input signal. For \(\phi_{in} = 0\) meminductance attains a constant value in both the topology (incremental and decremental), where for the operator \(\pm\), the + is for incremental and – is for decremental configuration.

3.2. Floating meminductor emulator

![Fig. 5. Schematic diagram of floating meminductor emulator](image)
The floating meminductor emulator is shown in Fig. 5. Considering incremental type meminductor emulator i.e., pins w, x and pins y, z are interconnected. The currents $I_A, I_B,$ and $I_C$ are obtained as

$$I_{in}(t) = I_A = I_{inB} = I_{X1} = I_{Z1}$$  \hfill (15)

also $I_{in}(t) = -I_{inB}$ \hfill (16)

And $V_{Y2} = V_{inB} = V_{X2} - I_{X2}R_{X2}$ \hfill (by port relationship)

$$V_{inB} = -\left(\frac{I_{X2}}{SC_2}\right) - I_{X2}R_{X2}$$ \hfill (17)

Also $I_{X2} = I_{Z2} = \frac{-V_{Y1}}{R_1} = \frac{-V_{in}}{R_1}$

So (17) becomes

$$V_{in} = V_{inB}\left(\frac{SRC_2}{1+SC_2R_{X2} - R_1SC_2}\right)$$ \hfill (18)

Dividing (18) by (16)

$$\frac{V_{in}}{I_{in}} = \frac{-V_{inB}R_1SC_2}{I_{inB}1 + SC_2R_{X2} - SC_2R_1}$$ \hfill (19)

Bias voltage $V_{B3}$ is given by

$$V_{B3} = \frac{1}{C_1}\int I_c(t)dt = \frac{G_{m4}}{C_1}\int V_{inB}(t)dt = \frac{G_{m4}}{C_1}\left(\frac{1+SC_2R_{X2}}{SR_1C_2}\right)\int V_{in}(t)dt$$

$$= \frac{G_{m4}}{C_1}\left(\frac{1+SC_2R_{X2}}{SR_1C_2}\right)\phi_{in}$$ \hfill (20)

where $\phi_{in} = \int V_{in}(t)dt$ is the total flux obtained by meminductor.

Substituting (20) into (2), transconductance $G_{m2}$ is obtained as

$$G_{m3} = \frac{k}{\sqrt{2}}(V_{B3} - V_{ss} - 2V_{in}) = \frac{k}{\sqrt{2}}\left(\frac{G_{m4}\left(1+SC_2R_{X2} - SC_2R_1\right)}{SC_1R_1C_2}\phi_{in} - V_{ss} - 2V_{in}\right)$$ \hfill (21)
Also
\[ G_{m3} = \frac{-I_{O3}}{V_{oB}} = \frac{I_{inB}}{V_{oB}} \]

So (21) becomes
\[ \frac{I_{inB}}{V_{oB}} = \frac{k}{\sqrt{2}} \left( \frac{G_{m4}(1 + SC_2 R_{X2}) \varphi_m}{SC_1 R_1 C_2} - V_{ss} - 2V_{th} \right) \] (22)

Substituting (22) in (19) gives meminductance of the proposed grounded incremental meminductor emulator is obtained as
\[ \phi_{in} = \frac{R_1 C_2}{I_{in}} \left[ \frac{k}{\sqrt{2}} \left( \frac{G_{m4}(1 + SC_2 R_{X2} - SC_2 R_1) \varphi_m}{SC_1 R_1 C_2} \right) + \frac{1}{1 + SC_2 R_{X2} - SC_2 R_1} \right] \] (23)

Similarly, the change of switch connections to w-z and y-x changes polarity of time variant part of meminductance of (23), resulting in a decremental type meminductance as
\[ \phi_{in} = \frac{R_1 C_2}{I_{in}} \left[ \frac{k}{\sqrt{2}} \left( \frac{G_{m4}(1 + SC_2 R_{X2} - SC_2 R_1) \varphi_m}{SC_1 R_1 C_2} \right) + \frac{1}{1 + SC_2 R_{X2} - SC_2 R_1} \right] \] (24)

Equation (23) and (24) can be rewritten as
\[ \phi_{in} = \frac{R_1 C_2}{I_{in}} \left[ \frac{k}{\sqrt{2}} \left( \frac{G_{m4}(1 + SC_2 R_{X2} - SC_2 R_1) \varphi_m}{SC_1 R_1 C_2} \right) + \frac{1}{1 + SC_2 R_{X2} - SC_2 R_1} \right] \] (25)

As operating frequency is much less than \( \frac{1}{2 \pi C_2 R_{X2}} \) where \( R_{X2} \) is the resistance at input port X of CCII which is usually very low [28] and \( R_I \) is assumed to be small, so
\[ (1 + SC_2 R_{X2} - SC_2 R_1) \approx 1. \]

So Equation (25) can be rewritten as
\[
L_M = \frac{\phi_m}{I_m} \approx \frac{RC_2}{\frac{k}{\sqrt{2}}(V_{ss} + 2V_{th}) \pm \frac{k}{\sqrt{2}} \left( \frac{G_m4\phi_m}{SC_1R_1^2C_2^2} \right)}
\]

\[
L_{M^{-1}} = \frac{I_m}{\phi_m} \approx \frac{k}{\sqrt{2}RC_2}(V_{ss} + 2V_{th}) \pm \frac{k}{\sqrt{2}} \left( \frac{G_m4\phi_m}{SC_1R_1^2C_2^2} \right)
\]

In equation (24) \(G_{m4}\) can be controllable by external bias voltage \(V_{B4}\) and \(R_{X2}\) is controlled by external current \(I_b\) which makes proposed circuit electronically tunable. The equations (23) and (24) represent incremental and decremental meminductance respectively, where in (26) for a fixed operating frequency \(k/(\sqrt{2}R_1C_2)\) is the constant term and \(k/\sqrt{2}(SC_1R_1^2C_2^2)\) being the time-varying term as \(\phi_m\) is the function of time varying input signal. For \(\phi_m = 0\) memductance attains a constant value in both the topology (incremental and decremental), where for the operator \(\pm\), the + is for incremental and – is for decremental configuration.

4. **Comparison of meminductor emulators and mutators**

A comparison of available meminductor emulators is given in Table 2 and Table 3. It is observed that most of the emulators use a large number of analog building blocks for implementation and have frequency limitations as well. The CCII and OTA-based emulators proposed in [7-11] are grounded types and use a large number of active components along with one or more other building blocks along with multiplier and adder with the addition to an excessive number of passive components in the count. Such as one in [7] uses 3 CCII, 1 Multiplier, 1 adder, 2 capacitances, and 1 resistance. Furthermore, they do not have electronic tunability as well. Similarly, the mutators in [12-16] have a frequency range of operation is few KHz and are not usable at high frequency. Whereas the proposed grounded and floating meminductor are useful respectively for 10 MHz and 400 KHz. Both the incremental and decremental properties are present in the proposed emulators. An important feature of the proposed meminductor emulator is its ability to control the meminductance value by controlling the transconductance \(G_m4\) by bias voltage \(V_{B4}\) and internal resistance \(R_{X2}\) by \(I_b\).
Table 2. Comparison of meminductor emulators.

| Ref. | Number in count and type(s) of active building blocks used | Passive Elements (C/R/L) | Electronic Tunability | Tech. Used | Max. operating frequency shown |
|------|-----------------------------------------------------------|--------------------------|-----------------------|------------|-------------------------------|
| [7]  | 3 CCII, 1 Multiplier, 1 Adder                            | 2/3/0                    | No                    | CMOS       | 20 Hz                         |
| [8]  | 2 Op-Amp, 2 Current Mirrors, 1 Buffer, 1 Multiplier      | 2/2/1                    | No                    | CMOS       | 300 Hz                        |
| [9]  | 4 CFOs, 1 Buffer, 2 Op-Amp, 1 Multiplier                | 2/6/0                    | No                    | CMOS       | 36.9 Hz                       |
| [10] | 5 Op-Amp, 1 Multiplier                                   | 2/10                     | No                    | CMOS       | 70 Hz                         |
| [11] | 1 Mo-OTA                                                 | 1/1/1                    | Yes                   | CMOS       | 500 Hz                        |

Table 3. Comparison of meminductor mutators.

| Ref. | Number in count and type(s) of active building blocks used | Passive Elements (L/C/R) | Electronic Tunability | Tech. Used | Max. operating frequency shown |
|------|-----------------------------------------------------------|--------------------------|-----------------------|------------|-------------------------------|
| [13] | 1 Op Amp                                                  | 0/1/1                    | No                    | CMOS       | 8 Hz                          |
| [14] | 1 CCII, 3 Op-Amp                                         | 0/1/3                    | No                    | CMOS       | 200 Hz                        |
| [15] | 2 CFOA, 1 buffer                                         | 0/1/1                    | No                    | CMOS       | 400 Hz                        |
| [16] | 3 TOAs, 3 Buffers                                        | 0/2/3                    | No                    | CMOS       | 21.1 Hz                       |

5. Simulations results and discussion

This section deals with the verification of the hysteresis loop between flux and the current, one of the fingerprints of the meminductor. To verify meminductive nature of proposed emulator circuits, simulation with 180 nm CMOS technology has been performed. A supply voltage of +1.2V and -1.2 V for VDD and VSS respectively for the analog blocks used in Fig. 4 and Fig. 5. All the MOS transistors are operated in the saturation region.

5.1. Grounded meminductor simulation result

The grounded meminductor emulator of Fig. 4 is simulated for different frequencies with aspect ratios, as given in Table 4, for MOS transistors. The results for the pinched hysteresis loop obtained for
frequencies of 100 Hz, 500KHz, 1MHz, 5MHz, 8MHz, and 10 MHz are shown in Fig. 6. Here the product of capacitor($C_2$) value and frequency ($f$) is kept constant ($75 \times 10^{-6}$ FaradHz) with $A_m=140$ mV, $V_{BI}=450$ mV. The overlapping of the pinched hysteresis nature of $\Phi$-$I$ curves validates the meminductive behavior of emulators as obtained in (13). Fig.7 shows the relationship between charge $q(t)$ and integral of flux $\rho(t)$. It shows that $q$ is a single-valued function of $\rho$. Therefore, the device the current goes through is a meminductor.

**Table 4. Design Parameters for analog blocks in grounded Meminductor**

| MOS Transistors | W(µm) | L(nm) |
|-----------------|-------|-------|
| $M_{1-4}$       | 12    | 375   |
| $M_{10}$        | 12    | 510   |
| $M_{5-9, M_{11}}$ | 12    | 500   |

| MOS Transistors | W(µm) | L(nm) |
|-----------------|-------|-------|
| $M_{1, M_{3-13}}$ | 12    | 500   |
| $M_{2}$         | 2     | 200   |

**Fig. 6. $\Phi$-$I$ characteristic for grounded meminductor circuit at different operating frequencies for** $V_{in}=140$ mV, $I_b=20u$, $V_{BI}=0.45$ V, $C_2=150$ pf, $R=10$ Ω and constant $C_2 f=75 \times 10^{-6}$ FaradHz
5.2. Floating meminductor simulation result

The floating meminductor emulator of Fig. 5 is simulated for different frequencies with aspect ratios, as given in Table 4, for MOS transistors. The results for the pinched hysteresis loop obtained for frequencies of 500 KHz, 1 MHz, 4MHz, 8MHz and 10 MHz are shown in Fig 8. Here the product of capacitor($C_2$) value and frequency ($f$) is kept constant (75 x 10^{-6} FaradHz) with $A_m=200mV$, $V_{B1}=500mV$. The overlapping of the pinched hysteresis nature of $\Phi$-$I$ curves validates the meminductive behavior of emulators as obtained in (25). Fig.9 shows the relationship between charge $q(t)$ and integral of flux $\rho(t)$. It shows that $q$ is a single-valued function of $\rho$. Therefore, the device the current goes through is a meminductor.

Fig. 7. Locus of $q(t)$ and $\rho(t)$ for grounded meminductor

Fig. 8. $\Phi$-$I$ characteristic for floating meminductor circuit at different operating frequencies for $V_{in}=200 mV$, $I_b=7u$, $V_{B1}=0.5 V$, $C_2=150pf$, $R=5 \Omega$ and constant $C_2f=75*10^{-6}$FaradHz
5.3. Effect of variation of bias voltage of OTA and bias current of CCII on pinched hysteresis loop

It is seen in (13) and (25) that meminductance of emulators depends on transconductance $G_{m4}$ and resistance $R_{X2}$ which is electronically controllable by external bias voltage $V_{B4}$ and current $I_b$. Fig. 10(a) shows the simulation results for signal frequency of 500 KHz, capacitor value $C_1=C_2=150$pf, $A_m=140$ mV at different values of bias voltages (0.45V, 0.4V and 0.35V) for grounded emulator configuration. Fig. 10(b) shows the simulation results for signal frequency of 200 KHz, capacitor value of $C_1=375$pf, $C_2=150$pf, $I_b=7$uA and $A_m=500$ mV at different values of bias voltages (0.3V, 0.45V, and 0.5V) for floating emulator configuration. It is observed in Fig.10 that the pinched hysteresis loop of $\Phi$-I curves increases with the increase of $V_{B4}$ (or $G_{m4}$) as expected. It implies that the memresistance can be controlled by $V_{B4}$.

Similarly, Fig. 10(c-d) shows the variation of the hysteresis loop for the different values of bias current. Fig 10(c) shows the variation of hysteresis loop for grounded topology at $f=500$KHz, capacitor value $C_1=C_2=150$pf, $A_m=140$ mV, $V_{B4}=450$ mv for different values of $I_b$ (15 uA, 17 uA, and 20 uA). Similar simulations are carried out to show the variation of the hysteresis loop for floating topology at $f=200$KHz, capacitor value $C_1=375$pf, $C_2=150$pf, $A_m=500$ mV, $V_{B4}=500$ mv for different values of $I_b$ (3 uA, 5 uA, and 7 uA). In Fig 10(d).
5.4. Effect of varying frequency and capacitance on the pinched hysteresis loop

The effect on Φ-I characteristics for variation of applied signal frequency for a fixed capacitance for both grounded and floating meminductor emulators are shown respectively in Fig. 11(a) and 11(b). Similarly, Fig. 11(c) and 11(d) show the effect of variation of capacitance for a fixed frequency signal for both grounded and floating meminductor emulators, respectively. Fig 11(a) shows the effect of varying frequency at a fixed capacitance of $C_1=7\text{pf}$, $C_2=150\text{pf}$, $A_m=140\text{ mV}$, $I_b=20\text{uA}$ and $V_{B1} = 450\text{ mV}$ for grounded topology. It shows that as frequency increases from 500 KHz – 1MHz for a fixed capacitance value, the hysteresis loop becomes more and more linear which satisfies (13), suggesting the time-varying nature of the loop decreases and ultimately vanishes at a certain frequency. Fig 11(b) shows the effect of varying input signal frequency at a fixed capacitance of $C_1=375\text{pf}$, $C_2=150\text{pf}$, $A_m=
500 mV, $I_b = 7\mu A$ and $V_{B1} = 500$ mV for floating topology. It shows that as the frequency increases from 200 KHz – 8 MHz for a fixed capacitance value, the area under the hysteresis loop gradually reduces to zero in conformity to (25). Similar nature of meminductance variation is found for the case of varying capacitance ($C_1$ and $C_2$) with a fixed frequency of 500 KHz for grounded topology and 200 KHz for floating topology in Fig. 1(c-f).
5.5. Series and parallel combinations of meminductor

The performance of meminductor emulator in series and parallel connections is studied in this section.

The possible circuit connections using grounded and floating meminductor are shown in Fig. 12.

Now, when an input current signal is applied to a circuit with two meminductors connected in parallel with the same polarities, as shown in Fig. 12(a), the flux accumulated in both the meminductors are equal. However, the charge \( q(t) \) is distributed across \( L_{M1} \) and \( L_{M2} \). Therefore, equivalent charge \( q(t) = q_1(t) + q_2(t) \), where \( q_1(t) \) and \( q_2(t) \) are the charge across \( L_{M1} \) and \( L_{M2} \), respectively.

Furthermore, for meminductors connected with the same polarities in series, as shown in Fig. 12(b), the currents flowing through both meminductors are equal. Thus the charge accumulated in each meminductor is also equal, i.e. \( q(t) = q_1(t) = q_2(t) \). The equivalent flux \( \phi(t) \) is distributed across \( L_{M1} \) and \( L_{M2} \). Therefore, we have \( \phi(t) = \phi_1(t) + \phi_2(t) \) Where \( \phi_1(t) \) is the total composite flux and \( \phi_1(t) \), \( \phi_2(t) \) are the flux across \( L_{M1} \) and \( L_{M2} \), respectively. Simulations are conducted to obtain the hysteresis loop by applying a sinusoidal input signal. Fig. 13(a-b) shows that the proposed meminductor emulators
can be used to emulate parallel connections in case of grounded and series connections in case of floating topology. It is observed that proposed emulators work properly under series and configurations.

![Diagram of meminductor combinations](image)

**Fig. 12.** meminductor combinations used in (a) grounded parallel, (b) Floating series with the same polarity

![Characteristic curves](image)

**Fig. 13.** $\Phi$-I characteristic curves for (a) grounded parallel meminductor emulator at 1 MHz for $V_{B4} = 450\text{mV}$, $A_{m} = 140\text{ mV}$, $C_{1} = 75\text{ pf}$, $C_{2} = 150\text{ pf}$ and $I_{b} = 20\text{uA}$, (b) floating parallel meminductor emulator at 1 MHz for $V_{B4} = 500\text{mV}$, $A_{m} = 200\text{ mV}$, $C_{1} = 75\text{ pf}$, $C_{2} = 150\text{ pf}$ and $I_{b} = 7\text{uA}$

### 6. Layout, post-layout simulations, and comparison

Layouts are obtained and post-layout simulations are carried out for both grounded and floating topologies to check the effect of parasitic on the hysteresis and current v/s time plots.

#### 6.1. Layout

Layouts for analog blocks of grounded and floating meminductor emulators have been obtained for post-layout comparison. The view of the layout of the meminductor emulator block is shown in Fig. 14.
Fig. 14. Layout of (a) CMOS based OTA of Fig. 2(a), (b) CMOS based CCII of Fig. 2(b), (c) CMOS based CCCII of Fig. 2(c)

6.2. Pre and post-layout comparison for grounded and floating meminductor emulators

Fig 15(a-b) Φ-I characteristic curves for grounded meminductor emulator at 1 MHz and 10 MHz respectively. Similarly, Fig 15(c-d) shows the Φ-I characteristic curves for floating meminductor emulator at an operating frequency of 100KHz and 1MHz respectively. It is observed in Fig 15 that the pre and post layout results overlap with each other, which reveals that the effect of parasitic on the proposed circuit built using OTA and second generation current conveyor is negligible.
Fig. 15. Pre and Post layout comparison of Φ-I characteristic plot for (a) grounded meminductor emulator at 1 MHz for $V_{B4} =$ 450mV, $A_m = 140$ mV, $C_1 = 75$ pf, $C_2 = 150$ pf and $I_b = 20$ uA, (b) grounded meminductor emulator at 10 MHz for $V_{B4} =$ 450mV, $A_m = 140$ mV, $C_1 = 7$ pf, $C_2 = 150$ pf and $I_b = 20$ uA, (c) floating meminductor emulator at 100 KHz for $V_{B4} =$ 500mV, $A_m = 600$ mV, $C_1 = 750$ pf, $C_2 = 150$ pf and $I_b = 7$ uA, (d) floating meminductor emulator at 1 MHz for $V_{B4} =$ 500mV, $A_m = 200$ mV, $C_1 = 75$ pf, $C_2 = 150$ pf and $I_b = 7$ uA.

6.3 Monte Carlo Analysis

Post layout Monte Carlo (MC) simulation for process mismatch at a frequency of 1 MHz for 200 simulation runs is performed for grounded topology. Similar MC analysis is performed for floating topology at a frequency of 200 KHz for 200 simulation runs. MC results for the hysteresis loop in both grounded and floating topology are shown in Fig 16. Gaussian random variation of standard device parameters is mentioned in Table 5.
Table 5. Deviation values for process and mismatch

| Parameters | Process Deviation | Mismatch Deviation |
|------------|-------------------|--------------------|
| tox        | 0.2e-9            | 0.02e-9            |
| Vth        | 0.04              | 0.004              |
| L          | 2e-9              | 0.2e-9             |
| W          | 2e-9              | 0.2e-9             |
| Cjn        | 0.00015           | 0.000015           |
| Cjswn      | 0.3e-10           | 0.03e-10           |
| Cjswgn     | 0.5e-10           | 0.05e-10           |
| Cgon       | 0.6e-10           | 0.06e-10           |
| hdifn      | 2e-8              | 0.2e-8             |

Fig. 16. Hysteresis loop of MC result for 200 simulation runs (a) for grounded topology (b) for floating topology

Fig. 17 shows the histogram plot for the distribution of samples for meminductance-dependent parameters such as threshold voltage(Vth) and betaeff(K). From the histogram graph, the standard deviation for Vth and K is found to be 32.4 mv and 416 u, respectively, for both topologies.
On analyzing Fig.17, it can be seen that the Hysteresis loop shows a bunch of expected loops as meminductance depends on capacitance, parasitic and other device parameters. However, the loops remain pinched at the origin and the memristive nature is perfectly conserved. It reveals that the proposed circuit has reasonable sensitivity performance with a variation of values of process, mismatch, threshold voltage and other device parameters.

7. Non-Ideal Analysis

7.1 Nonideality effect due to OTA transconductance gain
Fig. 18 shows the non-ideal model of OTA where \((R_i, C_i)\) and \((R_0, C_0)\) are input and output parasitic capacitances and resistances respectively. The capacitances across the input ports are assumed to be equal. The transconductance of non-ideal OTA can be characterized by a single pole roll off model [24-25] giving frequency dependent transconductance at low frequency as,

\[
G_m(s) = G_{m0} \frac{\omega_a}{s + \omega_a}
\]  

(27)

where \(G_{m0}\) is the low-frequency value or open loop transconductance and \(\omega_a\) is the frequency in radians per second for which the transconductance has decreased to 0.707 of its low-frequency value or simply called the first corner frequency. At very high frequency the phase shift of OTA become a monotonically decreasing function of frequency which can be further approximated as [24]

\[
G_m(s) = G_{m0} \frac{\omega_a}{s + \omega_a} e^{-\tau s}, \quad s = j\omega
\]  

(28)

where \(\tau\) denotes excess phase shift whose approx. practical value being 1.25ns [61].

Equation (27) and (28) can be written as

\[
G_m(s) = \gamma G_{m0}, \text{where } \begin{cases} 
\gamma = \frac{\omega_a}{s + \omega_a}, & \text{for low and mid frequency} \\
\gamma = \frac{\omega_a}{s + \omega_a} e^{-\tau s}, & \text{for very high frequency}
\end{cases}
\]  

(29)

Taking into account the non-ideal effects in CMOS implementation of OTA the modified port relationship can then be written as

\[
I_{0 \pm} = \pm \gamma G_{m0}(V_{IN+} - V_{IN-}) = \pm G_m V_{in} = \pm \gamma G_{m0} V_{in}
\]  

(30)

Where trans-conductance gain coefficient from the input terminal to output terminal of OTA is denoted by \(\gamma\), which is ideally taken to be unity.
7.2 Nonideality effect due to Current transfer gain

The port relationship of non-ideal CCII due to transfer gain and impedances using Fig. 19 becomes

\[
\begin{bmatrix}
V_x \\
I_Z \\
I_Y
\end{bmatrix} =
\begin{bmatrix}
\beta(s) & Z_x & 0 \\
0 & \alpha(s) & 1/Z_x \\
1/Z_x & 0 & 0
\end{bmatrix}
\begin{bmatrix}
V_y \\
I_x \\
V_Z
\end{bmatrix}
\]

(31)

Where,

\[L_x = \frac{R_x}{2\pi f_{x,3dB}}, \quad C_y = \frac{1}{2\pi f_{y,3dB}R_y}, \quad C_z = \frac{1}{2\pi f_{z,3dB}R_z}, \quad \beta(s) = \frac{\beta_0}{1 + s/\omega_\beta}, \quad \text{and} \quad \alpha(s) = \frac{\alpha_0}{1 + s/\omega_\alpha}\]

The parasitic impedance at terminal X shows a resistive behavior at lower frequencies and an inductive behavior at higher frequencies. The total X terminal parasitic impedance \(Z_X\), therefore, can be represented as a serial combination of \(R_X\) and \(L_X\). At terminal Y, a parasitic impedance \(Z_Y\) appears consists of a parallel combination of \(R_Y\) and \(C_Y\) where \(R_Y\) is the value of the impedance at a low frequency. At terminal Z, parasitic impedance \(Z_Z\) can be modeled as a parallel connection of resistance \(R_Z\) and capacitance \(C_Z\) where \(RZ\) is the value of the impedance at a low frequency. The value of \(C_Y\) and \(C_Z\) is then computed from the -3 dB cut-off frequency \(f_y\) and \(f_z\) respectively. \(\beta(s)\) and \(\alpha(s)\) represents the voltage and current transfers of the CCII, where \(\beta_0\) and \(\alpha_0\) represent the voltage and current tracking errors of the CCII and \(\omega_\beta\) and \(\omega_\alpha\) representing their corresponding poles, respectively.
7.3 Effect of Nonideality effect due to OTA transconductance gain and Current transfer gain on meminductance equations

Reanalysing the meminductance equation for Fig.4 using (30) and (31) for grounded meminductor configuration results in

\[
\frac{V_{in}}{I_{in}} = Z_{X1} + \frac{SR_C \beta^2}{k\gamma \sqrt{2} (V_{ss} + 2V_{th})} \left( \frac{G_m}{\sqrt{2}} \left( \frac{1 + SC_2R_{X2}}{SC_1R_{C2}} \right) \phi_m \right) \left( \frac{1}{1 + SC_2R_{X2}} \right) \tag{32}
\]

Similar analysis for the floating topology of Fig.5 results in

\[
\frac{\phi_{in}}{I_{in}} = \beta_2 + \frac{SR_C \beta^2}{k\gamma \sqrt{2} (V_{ss} + 2V_{th})} \left( \frac{G_m}{\sqrt{2}} \left( \frac{1 + SC_2R_{X2} - SC_2R_1}{SC_1R_{C2}} \right) \phi_m \right) \left( \frac{1}{1 + Z_{X2}\beta SC_2 - \beta SC_2R_1} \right) \tag{33}
\]

Where,

\[
\beta_2 = \frac{Z_{X1} (1 + Z_{X2}\beta SC_2)}{(1 + \beta SC_2Z_{X2} - \beta SC_2R_1)}
\]

Since the operating frequency is much less than 3dB frequency of both OTA and Current conveyor (Fig.3) therefore \( \beta \approx \beta_0 \approx 1 \) and \( \gamma \approx 1 \). Also \( Z_{X1} \approx R_{X1} \) (as \( L_{X1} \) is very small) and \( \beta_2 \approx R_{X2} \) which on substitution in (32) and (33) results in approximately the same equation as that of (13) and (25) respectively with an addition of constant \( R_{X1} \) in both the equations. Equation (32) and (33) clearly indicates that the trans-conductance gain coefficient and the transfer gain developed due to non-ideal effects in OTA and Current conveyors changes the meminductance value, however, the effect of nonideality may be neglected provided the operating frequency is much lower than the 3dB frequency of both OTA and Current conveyor and \( R_{X1} \) i.e., input parasitic resistance very less (Practical value is in few ohms [28])
7.4 Nonideality effect due to device parasitic on grounded meminductor emulator

Fig. 20 shows the non-ideal model with device parasitic of proposed grounded meminductor emulators. Resistances $R_{eq1}$, $R_{eq2}$, $R_{X2}$, $R_{03}$, $R_{04}$, capacitances $C_{02}$, $C_{03}$, $C_{eq}$ and inductance $L_{X1}$, $L_{X2}$ represents equivalent parasitic resistances, capacitances, and inductances at their respective nodes in Fig. 20.

Let the equivalent impedance at node E, D, B, A and C be $Z_1$, $Z_2$, $Z_3$, $Z_4$ and $Z_5$ respectively where

$$Z_1 = (R_{eq1} + XL_{X1}), \quad Z_2 = (R_{X2} + XL_{X2} + XC_2), \quad Z_3 = (R_{03} \parallel XC_{03}),$$

$$Z_4 = (R_{04} \parallel XC_{eq}) \quad \text{and} \quad Z_5 = (R_{eq2} \parallel XC_{02}),$$

and

$$C_{eq} = (C_1 + C_o), \quad R_{03} = (R_1 \parallel R_i \parallel R_o), \quad R_{eq2} = (R_1 \parallel R_o) \quad \text{and} \quad R_{eq1} = (R_{X1} + R_S).$$

Also on applying KCL at node C and port relationship

$$V_{Y2} = V_b = V_{X2} - I_{X2}R_{X2} = -I_{X2}Z_2 - I_{X2}R_{X2} \quad \text{(by port relationship)} \quad (34)$$

Also on applying KCL at node C

$$I_{X2} = I_{Z2} = \frac{-V_{Y1}}{Z_5} = \frac{-V_{X1}}{Z_5} = \frac{-V_{in}Z_i}{R_i(Z_5 + R_S)} \quad (35)$$

Using (35) in (34) results in
\[ V_{in} = \beta_4 V_B \]  

(36)

Where

\[ \beta_4 = \left( \frac{Z_5 Z_1 + Z_5 R_3}{Z_5 Z_2 + Z_5 R_X} \right) \]

On applying KCL at node B

\[ I_{in} = I_{Z_1} = -I_B \left( \frac{R_B + Z_3}{Z_3} \right) \]  

(37)

Using (36) and (37) results in

\[ \frac{I_{in}}{V_{in}} = \frac{-Z_1}{Z_5} \left( \frac{Z_2 + R_X}{Z_1 + R} \right) \frac{I_B}{V_B} \]  

(38)

Further analysis results in

\[ \frac{I_B}{V_B} = -\frac{K}{\sqrt{2}} (V_{ss} + 2V_{TH}) + \frac{KR_{m5} G_{m4} \phi_m}{\sqrt{2} Z_{04} C_{eq}} + \frac{1}{Z_5} \]  

(39)

So the inverse meminductance equation after substituting (39) in (38) becomes for both the topologies

\[ \frac{I_{in}}{V_{in}} = \frac{1}{\beta_4} \left[ R_B + Z_3 \right] \left( \frac{K}{\sqrt{2}} (V_{ss} + 2V_{TH}) + \frac{KR_{m5} G_{m4} \phi_m}{\sqrt{2} \beta_4 Z_{04} C_{eq}} + \frac{1}{Z_3} \right) \]  

(40)

Typical practical numerical values of CMOS OTA parasitic obtained from routine analysis and [26] can be assumed approximately as \( R_{in} = \infty \), \( R_o = 1M\Omega \), \( C_i = 50 fF \), \( C_0 = 100 fF \) while that of CCII/CCCII obtained from routine analysis and [28] can be assumed in the range of \( R_x \approx \) few Ohms, \( R_Y \approx \) few G\( \Omega \) and \( R_Z \approx \) few M\( \Omega \), while \( L_X \approx \) 150 uH and \( C_y, C_z \) are in the range of few femtofarads which on further substitution gives

\[ Z_1 \approx R_{eq1} \quad , \quad Z_2 \approx R_{X2} + \frac{1}{SC_2} \quad , \quad Z_4 \approx R_{04} \quad , \quad Z_5 \approx \text{few } \Omega \quad , \quad \beta_4 \approx \frac{SRC_2}{1 + SC_2 R_{X2}} \quad , \quad C_{eq} \approx C_i \quad \text{both at low and high frequency and } Z_3 \approx \infty \quad \text{at low and} \]
high frequency respectively and \( \frac{R_B + Z_3}{Z_3} \approx 1 \) as \( Z_3 > R_B \) which on further substitution in (40) gives

\[
\frac{V_{in}}{I_{in}} = \frac{SR_2C_2}{\sqrt{2} (V_{in} + 2V_{in}) \mp \sqrt{2} \left( \frac{G_{m1} (1 + SC_2RX_2) \phi_{in}}{SC_2R_2} \right) 1 + SC_2RX_2}
\]

This is similar to (13). Hence it can be concluded that the effect of parasitic on the proposed grounded circuit at low and high frequencies are very less.

### 7.5 Nonideality effect due to device parasitic on floating meminductor emulator

![Non-Ideal model of proposed floating meminductor emulator](image)

In Fig. 21, let the equivalent impedance at node E, D, B, A and C be \( Z_1 \), \( Z_2 \), \( Z_3 \), \( Z_4 \) and \( Z_5 \) respectively where

\[
Z_1 = \left( R_{q1} + XLX_1 \right), \quad Z_2 = \left( R_{eq3} + XLX_2 + XC_2 \right), \quad Z_3 = \left( R_{03} \parallel XC_{03} \right),
\]

\[
Z_4 = \left( R_{04} \parallel XC_{equ} \right) \quad \text{and} \quad Z_5 = \left( R_{eq2} \parallel XC_{02} \right),
\]

and
\[ C_{eq} = (C_1 + C_o), \quad R_{eq3} = (R_i \parallel R_i \parallel R_o), \quad R_{eq2} = (R_{X2} + R_{s}), \quad \text{and} \]
\[ R_{eq1} = (R_{X1} + R_{s}) \]

Also,
\[ I_{z2} = I_{z2} = \frac{-V_{x1}}{Z_3} = \frac{-V_{x1}}{Z_3} = \frac{-V_{in}Z_3}{R_{i}(Z_1 + R_{s})} \quad \text{(by port relationship)} \quad (42) \]

On applying KCL at node ‘D’ and using the port relationship
\[ V_{y2} = V_B = V_{x2} - I_{x2}R_{x2} = \frac{(-V_{in} \beta_s - I_{z2})}{\beta_4} - I_{x2}R_{x2} \quad (43) \]

where
\[ \beta_s = \frac{1}{R_{s} + R_{eq3} + X_{c2} + X_{LX2}} \]

Substituting (43) in (42)
\[ V_B = V_{in} \left[ 1 + \frac{Z_1(1 + \beta_s R_{c2})}{Z_3(Z_1 + R_{s})\beta_s} \right] \]

Or,
\[ V_{in} = V_B \beta_6 \quad (44) \]

Where
\[ \beta_6 = \frac{(Z_5Z_1 + Z_3R_{s})\beta_s}{(Z_1(1 + \beta_s R_{c2})) - (Z_5Z_1 + Z_3R_{s})\beta_s} \]

On applying KCL at node B
\[ I_{z1} + I_B + \frac{V_B}{Z_3} = 0 \]

Or,
\[ I_{in} = -I_B \left( 1 + \frac{R_B}{Z_3} \right) \quad (45) \]

Dividing (44) and (45)
\[ \frac{I_m}{V_m} = -\frac{1}{\beta_b} \left[ \frac{R_b + Z_3}{Z_3} \right] \frac{I_b}{V_B} \]

Further analysis results in

\[ \frac{I_b}{V_B} = \frac{-K}{\sqrt{2}} \left( V_{ss} + 2V_{th} \right) + \frac{1}{Z_4} \pm \frac{K}{\sqrt{2}} \frac{G_{m4}R_{o3}\phi_m}{\beta_bZ_{o4}C_{eq}} \]

Which on substitution results in

\[ \frac{I_m}{V_m} = \frac{1}{\beta_b} \left[ \frac{R_b + Z_3}{Z_3} \right] \left( \frac{K}{\sqrt{2}} \left( V_{ss} + 2V_{th} \right) + \frac{1}{Z_4} \pm \frac{K}{\sqrt{2}} \frac{G_{m4}R_{o3}\phi_m}{\beta_bZ_{o4}C_{eq}} \right) \] (46)

On applying the typical practical numerical values of CMOS OTA parasitic obtained from routine analysis and [26] can be assumed approximately as \( R_m = \infty, \ R_o = 1M\Omega, \ C_i = 50fF, \ C_0 = 100fF \) while that of CCII/CCCII obtained from routine analysis and [28] can be assumed in the range of \( R_x \approx \) few Ohms, \( R_y \approx \) few G\( \Omega \) and \( R_z \approx \) few M\( \Omega \), while \( L_x \approx 150\) uH and \( C_y, C_z \) are in the range of few femtofarads which on further substitution gives \( Z_1 \approx R_{eq1}, \ Z_2 \approx R_{eq3} + \frac{1}{SC_2}, \ Z_4 \approx R_{o4}, \ Z_5 \approx \) few \( \Omega \), \( \beta_b \approx \frac{SRC_2}{1 + SC_2R_{x2} - SC_2R_i}, \ C_{eq} \approx C_i \) both at low and high frequency and \( Z_3 \approx \infty \) at low and high frequency respectively and \( \left[ \frac{R_b + Z_3}{Z_3} \right] \approx 1 \) as \( Z_3 > R_b \) which on further substitution in (46) for both the topologies results in

\[ \frac{V_m}{I_m} = \frac{k}{\sqrt{2}} \left( V_{ss} + 2V_{th} \right) + \frac{k}{\sqrt{2}} \left( \frac{G_{m4} \left( 1 + SC_2R_{x2} - SC_2R_i \right) \phi_m}{SC_1R_2C_2} \right) \frac{1}{1 + SC_2R_{x2} - SC_2R_i} \] (47)

This is similar to (25). Hence it can be concluded that the effect of parasitic on the proposed circuit at low and high frequencies is very less.
8. Application of meminductor as amplitude modulation (AM)

As an application of the proposed memristive device, an AM modulation scheme with meminductor is carried out. Schematic of various circuits along with implementation using OTA based grounded meminductor emulator is shown in Fig. 22. In Fig. 22(a) a multifunction filter [- - - -] using OTA is given, which can implement both bandpass filter (BPF) and low pass filter (LPF) responses using the components for \(Y_1, Y_2, Y_3, Y_4\) and \(Y_5\) as given in Table 6. The meminductance of meminductor shown in Fig. 22(b) is controlled by the low-frequency message signal \(V_m(t)\) due to which message gets imposed on the high-frequency carrier signal \(V_c(t)\). The output is filtered out by the bandpass filter of Fig. 22(a) centered at the carrier frequency to obtain an Amplitude Modulated wave. The circuit of Fig. 22(c) is used to demodulate the AM signal to recover the message signal.
Fig. 22. Block diagram of (a) current mode multifunction filter, (b) AM modulator circuit using grounded meminductor emulator and filter, (c) coherent demodulator circuit using OTA.

Table 6. Specification for multimode filter components

| Mode       | $Y_1$ | $Y_2$ | $Y_3$ | $Y_4$ | $Y_5$ |
|------------|-------|-------|-------|-------|-------|
| Low pass   | C1    | R2    | C3    | $\infty$ | 0     |
| Band pass  | R1    | R2    | C3    | C4    | R5    |

8.1. Analysis of amplitude modulator and demodulator

The voltage message signal $V_m(t)$ and carrier signal $V_C(t)$ are taken respectively as

$$V_m(t) = A_m \cos(\omega_m t); \quad V_C(t) = A_C \cos(\omega_c t)$$

(48)

The flux imposed to meminductor is given by

$$\varphi_m = \int V_m(t) dt = \int (V_m(t) + V_C(t)) dt = \frac{A_m \sin(\omega_m t)}{\omega_m} + \frac{A_C \sin(\omega_c t)}{\omega_c}$$

(49)

Also,

$$V_m(t) = A_m \cos(\omega_m t) + A_C \cos(\omega_c t)$$

(50)

$$I_{03} = V_B \sqrt{2} \left( \frac{G_m}{C_1} \int V_B(t) dt - V_{ss} - 2V_b \right)$$

(51)

Now using (18), (49) and (50) in (51) and passing it through BPF

$$I_{03} = \beta \cos(\omega_c t) + B_h \left[ \cos(\omega_e + \omega_m) + \cos(\omega_e - \omega_m) \right] + B_h' \cos(\omega_e + \omega_m)$$

(52)

where
\[ \beta_7 = \frac{A_e G_{m4} K}{\sqrt{2C_1}} \left( \frac{1 - R_1 SC_2 + SC_2 R_x x^2}{R_1 SC_2} \right)^2 \]

\[ \beta_8 = \frac{A_e G_{m4}}{2\sqrt{2C_1} \omega_C} \left( \frac{1 - R_1 SC_2 + SC_2 R_x x^2}{R_1 SC_2} \right)^2 \] and

\[ \beta_{\omega m} = \frac{A_e A_m}{\omega_m} \]

It is obvious that (52) is in the form of components of upper side band, lower side band and carrier of standard AM expression. In order to recover message signal from the modulated signal, a coherent product demodulator is used. Demodulator circuit is realized with OTA as multiplier cascaded with OTA based low pass filter as shown in Fig 22(c).

8.2. Simulation of amplitude modulator and demodulator

The parameters used for simulation of amplitude modulator (AM) and demodulator are given in Table 7. Fig.23(a) shows the modulated message signal \( V_S(t) \) obtained at the output of current mode band pass filter in Fig 22(b) and the message signal applied to AM. Fig.23(b) shows the spectrum of the modulated signal obtained by applying rectangular window function present in FFT mode. Fig.20(c) shows the recovered message signal obtained at the output of current mode low pass filter in Fig 22(c).

It confirms that the scheme of AM proposed in this section using meminductor circuit can satisfactorily be utilized. It can further be shown that by varying amplitude of carrier and message signal one can obtain under, over and critical modulations.

Fig.23(d) and Fig.23(e) shows amplitude modulated waveform and its hysteresis loop for one-time period respectively. On analysing Fig. 23(d) and Fig. 23(e) simultaneously, one can observe that the amplitude of the hysteresis loop formed between charge and voltage increases and decreases according to increase and decrease in amplitude of message signal. So, the hysteresis loop itself changes its shape, size, and amplitude according to message signal.

For the first half cycle of the message signal, i.e., for time period A-B in Fig.20(d), the amplitude of the hysteresis loop in Fig. 20(e) decreases from point X to Y in the positive half cycle and point P to Q in a
negative half cycle of the modulated wave simultaneously. This results in the mapping of message amplitude on the carrier signal.

Similarly, for the second half cycle of the message signal i.e. for time period B-C in Fig.23(d) hysteresis loop of Fig. 23(e) increases from point Y to X for the positive half cycle and point Q to P for the negative half cycle of the modulated wave simultaneously leading to the mapping of message amplitude on the carrier signal. Thus, hysteresis loop which is nothing but meminductance slope is freezed as the peak amplitude variation of carrier, i.e., it follows the amplitude of the message signal. From Fig .23(e) we find that the hysteresis loop overlaps each other on each half-cycle.

Table 7. AM circuit simulation parameter

| S.No. | Parameter                              | Value  |
|-------|----------------------------------------|--------|
| 1     | Message signal amplitude Am            | 120 mV |
| 2     | Message signal frequency fm            | 50 KHz |
| 3     | Carrier signal amplitude Ac            | 370 mV |
| 4     | Carrier signal frequency fc            | 1 MHz  |
| 5     | Band Pass filter center frequency      | 1 MHz  |
| 6     | Band Pass Resistance (R_1=R_2=R_3)    | 200 Ω  |
| 7     | Band Pass Filter Capacitance(C_3=C_4) | 150 pf |
| 8     | Capacitance C_1                        | 32 pf  |
| 9     | Capacitance C_2                        | 150 pf |
| 10    | Local carrier amplitude                | 450 mV |
| 11    | Local carrier frequency fc             | 1 MHz  |
| 12    | Low Pass filter cut off frequency      | 50 KHz |
| 13    | Low Pass Resistance R2                 | 200 Ω  |
| 14    | Low Pass Filter capacitance (C_1=C_3)  | 10 pf  |
Fig. 23. The plot of (a) message signal and modulated signal, (b) spectrum of the modulated signal, (c) demodulated signal, (d) waveform of message and carrier for one time period, (e) hysteresis loop of AM for one time period
## 9. Experimental results

To verify experimentally, the proposed meminductor emulator is implemented as shown in Fig. 24(a) and Fig. 24(b) with capacitance (C1) as 40nf (in parallel combination of four 10nf) and commercially available BJT based OTA ICs (CA3080) and CFOA ICs (AD844). The prototype of the circuit is constructed on a breadboard as shown in Fig.24(c). The pinched hysteresis loops for grounded meminductor emulator are obtained for the operating frequency of 820 KHz for a 4V peak to peak input signal as shown in Fig. 24(d). Fig. 24(e) shows the pinched hysteresis loops for floating meminductor emulator at an operating frequency of 910 KHz for a 5V peak to peak input signal. However, because of limitations of operating bandwidth of 2MHz for IC CA3080 as well as parasitic faced due to interconnect of the experimental setup, the operating frequency range of the memristor emulator circuit on a breadboard is found to be close to 1 MHz.

Fig. 24(f) shows the time domain waveform for current and charge (integration of current). Fig. 24(g) shows the time domain waveform for input phi and pho (integration of phi). It can further be noted that both charge and pho curve tend to increase as time increase which justifies that the proposed circuit is a meminductor. It can further be noted that the integration of the input current and phi across the capacitor is performed through the inbuilt integration function in oscilloscope to prevent and kind of loading effect and loss in signal.

Fig. 24(h) shows the time domain waveform for flux and current. Analysis of Fig. 24(h) clearly reveals that the proposed circuit possesses a nonlinear relationship between flux and current and is simultaneously zero, thus verifying passivity.
Fig. 24. Meminductor emulator (a) Grounded Meminductor experimental circuit, (b) Floating Meminductor experimental circuit (c) Prototype on breadboard, (d) Experimental hysteresis loop for grounded meminductor, (e) Experimental hysteresis loop for floating meminductor, (f) Time domain waveform for Current and Charge, (g) Time domain waveform for phi and pho, (h) Time domain waveform for phi and current

10. Conclusion

The proposed meminductor emulators show pinched hysteresis loop and meminductive nature similar to a real meminductive device. They have a simple circuitry built with two OTAs and one two CCII. These emulators are first of their kind, having high frequency of operation. Proposed emulator circuits have been simulated for a frequency range up to 10MHz for grounded and floating in both incremental and decremental topology. Meminductance of proposed emulators is electronically tunable by the bias voltage of OTA and the bias current of CCII. Controllability of the pinched hysteresis loop and meminductance nature of proposed emulators for different frequencies of input signal, passive components, and an external bias voltage is verified by simulation results and has been discussed. Layout, post-layout simulation, and detailed non-ideal analysis are also given. Moreover, an AM modulator has been realized using the proposed meminductor emulator circuit as an application.

References

[1]. Chua LO. Memristor- the missing circuit element. IEEE Transaction on Circuit Theory 1971; 18(5):507-9.
[2]. Chua L. Device modeling via nonlinear circuit elements. IEEE Transactions on Circuits and Systems. 1980 Nov;27(11):1014-44.
[3]. Chua LO. Nonlinear circuit foundations for nanodevices. I. The four-element torus. Proceedings of the IEEE. 2003 Nov;91(11):1830-59.
[4]. Di Ventra M, Pershin YV, Chua LO. Circuit elements with memory: memristors, memcapacitors, and meminductors. Proceedings of the IEEE. 2009 Oct;97(10):1717-24.

[5]. Yin Z, Tian H, Chen G, Chua LO. What are memristor, memcapacitor, and meminductor?. IEEE Transactions on Circuits and Systems II: Express Briefs. 2015 Apr;62(4):402-6.

[6]. Biolek D, Biolek Z, Biolková V. Pinched hysteretic loops of ideal memristors, memcapacitors and meminductors must be ‘self-crossing’. Electronics letters. 2011 Dec 8;47(25):1385-7.

[7]. Fouda ME, Radwan AG. Memristor-less current-and voltage-controlled meminductor emulators. InElectronics, Circuits and Systems (ICECS), 2014 21st IEEE International Conference on 2014 Dec 7.

[8]. Sah MP, Budhathoki RK, Yang C, Kim H. Charge controlled meminductor emulator. Journal of Semiconductor Technology and Science. 2014 Dec;14(6):750-4.

[9]. Liang Y, Chen H, Yu DS. A practical implementation of a floating memristor-less meminductor emulator. IEEE Transactions on Circuits and Systems II: Express Briefs. 2014 May;61(5):299-303.

[10]. Wang GY, Jin PP, Wang XW, Shen YR, Yuan F, Wang XY. A flux-controlled model of meminductor and its application in chaotic oscillator. Chinese Physics B. 2016 Jul 19;25(9):090502.

[11]. Babacan Y. An Operational Transconductance Amplifier-based Memcapacitor and Meminductor. Electrica. 2018;18(1):36-8.

[12]. Biolek D, Biolková V, Kolka Z. Mutators simulating memcapacitors and meminductors. InCircuits and Systems (APCCAS), 2010 IEEE Asia Pacific Conference on 2010 Dec 6 (pp. 800-803). IEEE.

[13]. Pershin YV, Di Ventra M. Memristive circuits simulate memcapacitors and meminductors. Electronics Letters. 2010 Apr 1;46(7):517-8.

[14]. Sah MP, Budhathoki RK, Yang C, Kim H. Mutator-based meminductor emulator for circuit applications. Circuits, Systems, and Signal Processing. 2014 Aug 1;33(8):2363-83.

[15]. Sah, Maheshwar Pd, Ram Kaji Budhathoki, Changju Yang, and Hyongsuk Kim. "A mutator-based meminductor emulator circuit." In 2014 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 2249-2252. IEEE, 2014.

[16]. Yu D, Liang Y, Ju HH, Chua LO. A universal mutator for transformations among memristor, memcapacitor, and meminductor. IEEE Transactions on Circuits and Systems II: Express Briefs. 2014 Oct;61(10):758-62.

[17]. Biolek D, Biolek Z, Biolková V. PSPICE modeling of meminductor. Analog Integrated Circuits and Signal Processing. 2011 Jan 1;66(1):129-37.

[18]. Zhu H, Duan S, Wang L, Yang T, Tan J. The nonlinear meminductor models with its study on the device parameters variation. In Information Science and Technology (ICIST), 2017 Seventh International Conference on 2017 Apr 16 (pp. 497-503). IEEE.

[19]. Yao H, Duan S, Wang L. Composite behaviors of series and parallel meminductor circuits. In Information Science and Technology (ICIST), 2015 5th International Conference on 2015 Apr 24 (pp. 439-444). IEEE.

[20]. Hu Z, Li Y, Jia L, Yu J. Chaotic oscillator based on current-controlled meminductor. In Communications, Circuits and Systems (ICCCAS), 2010 International Conference on 2010 Jul 28 (pp. 820-823). IEEE.

[21]. Yuan F, Wang G, Wang X. Chaotic oscillator containing memcapacitor and meminductor and its dimensionality reduction analysis. Chaos: An Interdisciplinary Journal of Nonlinear Science. 2017 Mar;27(3):033103.

[22]. Xu B, Wang G, Shen Y. A simple meminductor-based chaotic system with complicated dynamics. Nonlinear Dynamics. 2017 May 1;88(3):2071-89.

[23]. Arora A, Niranjan V. Low power filter design using memristor, meminductor and memcapacitor. In Electrical, Computer and Electronics (UPCON), 2017 4th IEEE Uttar Pradesh Section International Conference on 2017 Oct 26 (pp. 113-117). IEEE.

[24]. Parveen, Tahira. Textbook of Operational Transconductance Amplifier and Analog Integrated Circuits. IK International Pvt Ltd, 2013. (5-6)

[25]. Whitaker JC, editor. The electronics handbook. CRC Press; 1996 Dec 23(666-669)

[26]. Deliyannis T, Sun Y, Fidler JK. Continuous-time active filter design. CRC Press; 1998 Dec 16 (241-244)

[27]. Al-Hashimi, B. Current mode filter structure based on dual output transconductance amplifiers. Electronics Letters, 1996; 32(1): 25-26.

[28]. Khateb F, Khateb N, Kubanek D. Low-Voltage Ultra-Low-Power Current Conveyor Based on Quasi-Floating Gate Transistors. Radioengineering. 2012 Jun 1;21(2).