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Charge trapping analysis in sputtered Bi$_x$Se$_{1-x}$ based accumulation-mode FETs

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ABSTRACT

Topological materials have attracted a lot of attention in the field of beyond Complementary Metal Oxide Semiconductor (CMOS) devices. Topological Insulators (TI) have been proposed for future high electron mobility field effect transistor (FET) devices that make the physics of operation and especially the oxide-film interface extremely crucial to understand. The effects of the gate voltage on the charge trapping in TI-based FET devices are reported in this work. Sputtered Bi$_x$Se$_{1-x}$ was chosen as the TI material. The interfacial chemistry was characterized using X-ray photoelectron spectroscopy (XPS), which shows a presence of Mg$^{2+}$ and oxygen impurities. A unique hysteresis behavior was found for the gate transfer characteristics, with respect to the gate voltage. This was attributed to the charge trapping in the gate oxide and across the SiO$_2$/Bi$_x$Se$_{1-x}$ interface. We simulated the effects of charge fluctuations on the resistivity of the film. These devices operate under accumulation mode rather inversion mode. Application of positive gate voltage results in accumulation of electrons in the "n-type" Bi$_x$Se$_{1-x}$ layer resulting in an increase of conductivity. In order to explain the drain current-gate voltage behavior, we used a simple polynomial model to describe the change in the device characteristics due to charge traps. The model was fitted with our experimental results. We further analyzed the gate leakage current, which showed a good match with trap-assisted tunneling (TAT) process that was used to derive trap parameters. The obtained trap parameters show the presence of ultra-deep charge traps contributing to the hysteretic behavior.

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INTRODUCTION

Topological materials, such as Bismuth Selenide thin films, have generated a lot of attention in the field of beyond CMOS devices. Those films are predicted to have highly conducting, spin-polarized, topologically protected surface states, which are robust to impurities and defects.¹⁻⁵ Top-gated devices with FET structures are used to study the transport properties of bismuth selenide based thin films, which make them a strong contender for future logic and memory devices such as high electron mobility transistors, spin memory etc.¹⁻⁵ The operation of these devices relies heavily on the characteristics of the gate dielectric-film interface. Furthermore, several works have demonstrated high charge to spin conversion and vice-versa in bismuth selenide thin films, which make them an extremely popular candidate for spin-orbit torque applications.⁶⁻¹¹ TIs are typically grown by molecular beam epitaxy, which is a high-end process.¹²⁻¹⁴ Recent reports have shown an enhanced spin-orbit torque efficiency in sputtered, polycrystalline bismuth selenide.¹⁷,¹⁸ The record high charge to spin conversion is owed to the quantum confinement effects inside the polycrystalline grains of sputtered TI. This makes bismuth selenide thin films highly compatible with CMOS process. Like any other non-ideal case, the imperfections in the gate oxide and the Bi$_x$Se$_{1-x}$/gate oxide (SiO$_2$) interface can trap charges during device operation. These traps can be a consequence of disorder and defects (points, interstitials, etc) as well as embedded impurities during the fabrication and growth process.¹⁹ These charge traps can largely modify the device properties. Several models have been proposed to explain the device physics and corresponding transport properties, resulting from charge traps and crystal imperfections.²⁰⁻²⁵ However, a detailed study to
characterize and understand the effects of charge trapping in thin films of topological materials is still lacking.

In this paper, we study the effects of charge trapping in the sputtered, polycrystalline Bi$_x$Se$_{1-x}$ (20 nm) thin films with top SiO$_2$ gate. XPS was used to visualize the interfacial chemistry. We used different in-situ sputtering times to etch the capping layer and reach the Bi$_x$Se$_{1-x}$ top surface. Gate voltage – drain current measurements show a hysteresis loop, which could be attributed to charge trapping in SiO$_2$ layer and across the Bi$_x$Se$_{1-x}$ – SiO$_2$ interface. In order to explain these results, we used a simple model to understand the change in device conductivity with charge traps. We further analyzed the leakage current mechanism in the devices using various physical models. Comparisons with experimental data indicate that the charge TAT process could be the dominant gate leakage mechanism, which results in an exponential gate voltage dependence from Wentzel-Kramers-Brillouin (WKB) approximation.

**SAMPLE PREPARATION**

Si/SiO$_2$/MgO(2 nm)/Bi$_x$Se$_{1-x}$(20 nm)/MgO(5 nm) stacks were grown by an eight-target Shamarck ultra-high vacuum magnetron sputtering system. Hall bar devices were fabricated using standard photolithography followed by Ar$^+$ ion milling. Second step of photolithography was used to form a window for gate dielectric deposition. Ar$^+$ etching was done to remove the capping layer and the sample was transferred to the load-lock chamber of a plasma-enhanced chemical vapor deposition system for the deposition of SiO$_2$. This was followed by a lift-off process to remove the oxide layer that is not in the “window region”. The third step of photolithography was applied to create the contact windows followed by another step of Ar$^+$ etching to remove the capping from the contact region. The last step was the deposition of the Ti (10 nm)/Au(100 nm) electrode contact by an e-beam evaporation process.

**CHEMICAL CHARACTERIZATION**

In order to understand the chemical properties of the stack, we performed XPS on the sample. The depth profiling was done via an in-situ Ar$^+$ etching. The original surface shows strong peaks of Mg KLL, which corresponds to Mg Auger peak, Mg 2s and O 1s$^{18}$. C 1s peak was used as calibration during XPS scans. On etching the sample, we start to observe peaks from Bismuth and Selenium. However, some of these peaks were too weak, so we also did high-resolution scans (0.1 eV/step) to look closely at the Bi and Se peaks separately. Stoichiometric composition can get skewed because of the differential sputter etch rate between Bi and Se atoms. Previous results on similar films have shown an over-concentration of Bismuth. There are two major observations from the XPS. Firstly, we detect the Mg through the whole film (fig. 2(a)), which can be seen as Mg 2s and Mg KLL peaks observed at all sputter etch times. These peaks change in magnitude with the film depth. This can be a result of Mg diffusion or the chamber contamination during sputter deposition of films. This is crucial since Mg impurities in Bi$_x$Se$_{1-x}$ can be a major contributor of impurity-based charge traps in the devices. Secondly, there is a change in the shape and position of Bi4f peaks with sputter etch time. Longer results in a shift of the peaks to the left (lower binding energy). Bi$_4$Hf$_{12}$ binding energy for Bi metal and Bi$_2$O$_3$ is 157 eV and 159 eV, respectively. The peak position moves from ~ 159 eV at 3 min sputter etch to ~ 157 eV at 5 min sputter etch. A similar observation can be made for Bi$_4$Fe$_{12}$ peaks (Bi metal = 162.4 eV and Bi$_2$O$_3$ = 164.3 eV). From this, we can make a conclusion that Bi chemical state changes with the depth profile. This strongly hints to the fact that Bi, close to the top interface, is probably oxidized. This oxidation can be a result of cleaning process of the sample, which uses multiple solvents to clean sample surface (also heavily used during the device fabrication), or it can also be from simple atmospheric oxidation over time. There is also a distinct change in the shape of the peak, which becomes sharper at longer etch times, further confirming our hypothesis on oxidized Bi at the top interface.

**THEORY**

Fig. 1(a) shows the device schematic and measurement system. Fig. 1(b,c) shows the cross sectional view of charge traps created during the application of positive and negative gate voltage. In an ideal case, the removal of gate voltage should take the device to its virgin state with no charge accumulation. However, due to charge trapping, the device never returns to its virgin state, thereby giving memory. To explain this hysteresis behavior, we start by using classical Drude’s model of electrical resistivity:

$$\rho = \frac{1}{ne\mu}$$

Here $n$ is the carrier concentration and is the carrier mobility. For the sputtered Bi$_x$Se$_{1-x}$, the majority carriers are electrons (n-type). The charge traps would create a small fluctuation in the carrier density, which would also create a corresponding change in the carrier mobility, in the Bi$_x$Se$_{1-x}$ layer. The change in resistivity can be written as:

$$\frac{d\rho}{\rho} = \frac{dn}{n} + \frac{d\mu}{\mu}$$

Here $dn$ and $d\mu$ refers to the change in carrier density and mobility respectively. The dependence of mobility on the carrier concentration will eventually determine the fluctuations in mobility. The change and carrier concentration and mobility can be written by a first order perturbative term involving a constant ($d\mu = kdn$). The parameter ‘$k$’ relates the fluctuations in mobility due to fluctuations in carrier density. The change in resistivity due to charge trapping hence becomes:

$$\frac{d\rho}{\rho} = \frac{dn}{n} \left[ 1 + \frac{kn}{\mu} \right] = \frac{pdn}{n}$$

The constant $k$ can be evaluated using the semi-empirical relation between carrier concentration and mobility as reported in our previous work:

$$k = \frac{pN_{se}}{N_{se} + N_{eu}}^{\frac{1}{2}}$$

The pre-factor ‘$p$’ essentially determines the corresponding change in resistivity with respect to the change in carrier concentration. Fig. 1(d) shows the simulated results. As can be seen, the prefactor ‘$p$’ reaches a maximum value of around 1.7 for the carrier
density of about $4.4 \times 10^{20} / \text{cm}^3$. Hence near this concentration, a small percentage change in carrier concentration can result in a large change in the resistivity.

The traditional relation between the gate voltage and carrier concentration would be improper for a TI because of the differential surface and bulk carrier density and conductivity. The first thought would be to assume a first order perturbation that would directly connect the carrier fluctuation with gate voltage. In such a case, we can simply assume the change in carrier concentration to be directly proportional to the gate voltage ($\delta n(t_k) \propto \delta V_g(t_k)$), $t_k$ being the $k^{th}$ instant of time. However, this creates a problem with the physics of charge trapping. Traps require some kind of memory with respect to the previous charge trapping ($\delta n(t_k) \propto \delta n(t_{k-1}) \propto \delta V_g(t_{k-1})$). This would mean a second (or maybe even a third) order perturbation ($\delta n(t_k) \propto \delta V_g^2(t_k)$).

$$\delta n = A\delta V_g + B\delta V_g^2 + C\delta V_g^3$$ (5)

Here the coefficients $A$, $B$ and $C$ relate the gate voltage to the change in carrier concentration. This can be put into equation to give a complete model. This in turn will give us a polynomial relationship between resistivity and gate voltage:

$$\rho = A^+ V_g + B^+ V_g^2 + C^+ V_g^3$$ (6)

We use this model to fit our experimental gate transfer characteristics.

**FIG. 1.** (a) Device Schematic, (b) Charge distribution under positive gate voltage, (c) Charge distribution under negative gate voltage, (d) Simulated parameter "p" for different carrier concentrations.

**FIG. 2.** (a) X-ray photoelectron spectroscopy (XPS) for elemental characterization. Each number corresponds to a specific peak position. The peaks for each number are as follows: 1) Bi5d3 2) Se3d 3) Mg2s 4) Bi4f7 5) Bi4f5 6) C1s 7) Se LMM 8) Mg KLL 9) Bi4d5 10) Bi4d3 11) O1s 12) Bi4p3 13) O KLL for different sputter etch times, (b) High resolution XPS for Bi 4f5 and 4f7 peaks for different sputter etch times.
TRANSPORT CHARACTERIZATION

In order to understand the gate transfer characteristics, we measured the resistivity of the film as a function of gate voltage for 2 different devices. Both devices show a strong hysteresis with respect to the gate voltage. We attribute this strong hysteretic behavior to charge trapping in the bulk of the oxide layer, as well as near the Bi$_x$Se$_{1-x}$/SiO$_2$ interface. We started by applying a negative maximum gate voltage of $-10$ V. After that we increased the gate voltage by 1V/s. As we move to the positive gate voltage, we see a drop in the resistivity of Bi$_x$Se$_{1-x}$ film. The physics of operation for our TI device is quite similar to that for the organic or thin film FET. Such devices work by becoming conductive in the accumulation rather than inversion mode, like a traditional mosfet.

Application of a strong negative voltage would theoretically bring the device under inversion mode, but we found that was impossible for our device without breaking the dielectric barrier. The reason could be the high carrier concentration of the Bi$_x$Se$_{1-x}$ film, which would require really high threshold voltage to go to inversion mode. Under the application of high gate voltage for an extended period of time, the traps will eventually get saturated with charges. Hence, the change in resistivity with respect to gate voltage will come to a halt. Fig. 3(a,b) shows the hysteresis along with the 3rd order polynomial fits. Fig. 3(c,d) shows the rate of change of channel resistivity with respect to gate voltage obtained from the above polynomial fit.

In order to further analyze the characteristics of traps we study the gate leakage current of the devices. The gate leakage mechanism can be fairly complicated with many different mechanisms playing roles. Typically, the physics of gate leakage can be divided into 2 categories 1) Classical and 2) Quantum.

Under the classical picture, there are two models that dominate the leakage mechanism: Schottky emission and Poole-Frenkel (PF) effect. Schottky emission is essentially the thermal injection which is also synonymous to hot carrier injection. In this model, the carriers in Bi$_x$Se$_{1-x}$ layer gain enough kinetic energy to channel to the gate electrode. In PF effect, the electrons can get trapped in a localized state. Random thermal fluctuations can give enough energy for the electrons to jump to a nearby localized state. These models connect the leakage current density (J) with the electric field (E) generated by gate voltage. For Schottky emission, log(J) will be linear with $\sqrt{E}$ and Poole-Frenkel effect will give log(J/E) to be linear with $\sqrt{E}$. For our case, both these requirements are not well satisfied. Hence, we can safely ignore the results of Schottky emission and PF effect.

Under the quantum regime, pure tunneling current play major roles in the leakage mechanism. In these tunneling mechanisms, the oxide acts as a barrier with a finite height ($\Phi_{ox}$). Depending on whether the voltage drop across the oxide ($V_{ox}$) is greater or less than the oxide barrier height, tunneling leakage can be further divided into two types i.e Fowler-Nordheim (FN) tunneling ($V_{ox} > \Phi_{ox}$) and Direct tunneling ($V_{ox} < \Phi_{ox}$). FN tunneling consists of electrons tunneling into the conduction band of the oxide layer. In this case, the oxide potential barrier is triangular in shape. Whereas, direct tunneling consists of electron tunneling directly to the gate contact through the forbidden energy gap of the oxide layer. Here, the barrier shape is trapezoidal. However, these tunneling mechanisms become significant only for ultra-thin gate oxide barrier (<3 nm). Therefore, it’d be safe to ignore the tunneling mechanisms for our
case which involves a fairly thick oxide barrier. However, there is a third way through which the carriers can tunnel across the oxide barrier and it is known as trap assisted tunneling (TAT) process. In this process, carriers can tunnel from an occupied trap to an unoccupied trap thereby contributing to the leakage mechanism. The probability of the carriers to tunnel between the traps, for a gate voltage \( V \), is calculated by WKB approximation and is given by:

\[
J = \frac{q^2}{2e}\exp\left(-\frac{2(2m^*q)^{0.5}\phi_{0.5}w}{h}\right)\exp\left(\frac{(2m^*q)^{0.5}w^2V}{\hbar d\Phi_d^{0.5}}\right)
\]  

(7)

Here \( w \) is the distance between nearest traps, \( q \) is the electron charge, \( h \) is the reduced Planck’s constant, \( \theta \) is the electron attempt to escape frequency which is usually taken to be \( 10^{13}/s \), \( m^* \) is the effective electron mass in the film which we have taken to be 0.15\( m_e \). TAT process should give us an exponential relationship between the gate voltage and the leakage current density. Fig. 3(f) shows this property along with the fit. Hence, it is reasonable to assume that, for our case, TAT process is the most dominant mechanism for gate leakage. \( w \) is the smallest distance between traps which is obtained from the fit to be 4.75 nm. \( \Phi_{0.5} \) is the barrier height which was obtained to be around 2.15 eV. This barrier height is much larger than the thermal energy at room temperature (25.7 meV), which makes the charge traps “ultra-deep”.

**CONCLUSION**

In summary, we proposed and fabricated a field effect transistor using sputtered Bi\(_{1-x}\)Se\(_x\). Chemical characterizations by XPS, disclosed the presence of impurities. The gate transfer characteristics indicates the transistor working in the accumulation. Forward and reverse sweep gate voltage indicates a device hysteresis behavior, which is attributed to the charge trapping in the gate dielectric as well as the Bi\(_{1-x}\)Se\(_x\)/dielectric interface. We developed a simple model, taking into account the fluctuations in carrier concentration and mobility. We further investigated the properties of the traps by analyzing the gate leakage current. The physics of the gate leakage is attributed to a trap-assisted-tunneling process. Using our experimental and the theoretical fit, we characterized the characteristics of the traps.

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