Physical principles of operation and basic capabilities of the four channel receiver 1288ХК1Т (mf-01)

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Abstract. In radar detection and radio navigation ensuring the reception of signals transmitted over the meteor channel of radio communication is often controversial[1-3]. Solving these problems requires the ability to synthesize precision signals directly[4, 5] for heterodyning systems in addition to modern analog-to-digital conversion devices, correlation analysis, and statistical processing of signal-noise complex. The step of adapting four channel receivers to dynamically changing conditions of transmitting information may include determining the composition of the signal-noise mixture, determining the phase characteristics of the communication channel, estimating the channel transmission rate, and obtaining QoS information. In addition, adaptation often implies the use of a logical channel control loop, which entails the need for complex feedback procedures. Software-defined radio systems are radio and telecommunication systems that can be tuned to an arbitrary frequency band and receive various types of modulated signal, consisting of programmable equipment with program control. SDR performs a significant part of digital signal processing on a conventional personal computer, signal processor or FPGA. In such systems and complexes, the parameters are changed by software configuration. The article considers the implementation of DDS for heterodyning an intermediate frequency signal on the FPGA basis for four channel receiver 1288ХК1Т (mf-01), which allows you to work with both narrow-band and wide-band communication channels (with simultaneous operation of 4 channels, the band can be expanded) and can be used in modern telecommunication communication systems.

1. Introduction

Microcircuit 1288ХК1Т (MF-01) is intended for the construction of receiving paths of radio communication systems and radar detection. The MF-01 implements the functions of converting the input signal from an intermediate frequency to a low frequency, followed by filtering and decimation of the signal. The use of digital signal processing at an intermediate frequency can reduce the requirements for the analog path and simplify the implementation and / or improve the performance of the system as a whole. The MF-01 chip can be used in cellular systems, such as GSM, IS-136, IS-95, WCDMA or UMTS. The performance of the microcircuit is sufficient for processing four channels of narrowband communication net (GSM, IS-136, IS-95) or one channel of broadband communication net (WCDMA,
UMTS). Based on the MF-01 chip, software-tunable phased and adaptive antenna arrays can be implemented, including Smart Antenna and MIMO technologies.

2. Materials and methods

The MF-01 digital receiver contains four identical channels that implement the functions of heterodyning, decimation, and channel filtering of the input signal[6-8]. Each of the four channels of digital processing includes a digital local oscillator (NCO, X), two cascades of decimation filters with constant coefficients (CIC2, CICN), two cascades of programmable FIR decimation filters of the 64th order (DFIR64) and a complex output signal multiplier (FGAIN).

The structure of the 1288XK1T microcircuit (MF-01) is shown in Figure 1.

![Figure 1. The structure of the 1288XK1T (MF-01) microcircuit.](image)

The digital quadrature local oscillator transfers the spectrum of the input signal from intermediate frequency to low frequency, multiplying the samples of the input signal by the samples of the reference signal. The local oscillator controls the frequency and phase of the reference signal.

Fixed-coefficient decimation filters are designed for preliminary decimation of a signal[9]. Filters are constructed as filters with unit coefficients (CIC - cascaded integrator / comb). The use of these filters is effective for large values of the decimation coefficient. If necessary, these filters can be turned off.

Two stages of programmable FIR decimation filters can be used for subsequent decimation with small decimation coefficients, correction of frequency response distortion caused by CIC-decimator filters and channel filtering.

Each of the cascades of FIR filters allows lowering the sampling frequency from 1 to 16 times. The maximum order of each filter is 64, the filter type is symmetric or antisymmetric. Filters are capable of processing two samples in one period of the VLSI clock frequency. The filters have 32 programmable 16-bit coefficients and are implemented as RCF filters (RAM Coefficient Filter). At a clock frequency of 100 MHz, the sampling frequency of the signal at the output of the 64th order FIR filter is more than 3 MHz, and can be increased by decreasing the filter order[10].

An integrated output signal multiplier allows smooth adjustment of the channel gain and control of the phase of the output signal, which can be used to improve the dynamic range of the processing path, constructing AGCs or PAR systems.

DataStream Routers (MX) allow combining the computing resources of several channels into one to increase the performance of FIR filters. For example, when all four channels are combined, the sampling
frequency of the signal at the output of the 64th order FIR filter at a clock frequency of 100 MHz is more than 12 MHz.

The 1288XK1T digital receiver contains four identical channels that implement the functions of heterodyning, decimation, and channel filtering of the input signal. The input interface provides reception and routing of data streams coming from external analog-to-digital converters. Each channel for digital processing of the address data path includes a digital local oscillator, two cascades of decimation filters with constant coefficients, two cascades of programmable FIR decimation filters of the 64th order and a complex output multiplier.

3. Results

The HTDR quadrature local oscillator transfers the spectrum of the input real signal from intermediate frequency to low frequency, multiplying the samples of the input signal by the samples of the reference signal: sin (ωt) and cos (ωt). The local oscillator controls the frequency and phase of the reference signal.

Decimation filters with constant coefficients equal to unity are intended for preliminary decimation of a signal. The use of filters is effective for large values of the decimation coefficient. Filters can be turned off if necessary.

Two cascades of programmable FIR decimation filters (DFIR) are used for subsequent decimation with small decimation coefficients, correction of amplitude-frequency response distortion caused by CIC decimation filters and channel filtering. Each of the cascades of FIR filters allows lowering the sampling frequency from 1 to 16 times.

The maximum order of each filter is 64; the filter type is symmetric or antisymmetric. Filters are capable of processing two samples in one period of the clock frequency 1288XK1T. Filters have 32 programmable 16-bit coefficients and are represented as FIR filters with coefficients stored in RAM. At a clock frequency of 100 MHz, the sampling frequency of the signal at the output of the 64th order FIR filter is more than 3 MHz and can be increased by decreasing the filter order.

The complex output signal multiplier provides smooth adjustment of the channel gain and control of the phase of the output signal, which can be used to improve the dynamic range of the processing path, to build automatic gain control, or to use the PAA and AAA systems.

Data flow switches allow combining the computing resources of several channels into one to increase the performance of FIR filters. For example, when all four channels are combined, the sampling frequency of the signal at the output of the 64th order FIR filter at a clock frequency of 100 MHz is more than 12 MHz.

The output of the processed signal data is carried out through a 16 or 32-bit parallel buffer of output data, implemented in the form of FIFO, or through a 4 or 8-bit link port. The output process is controlled using a serial (SPI) or parallel (P_PORT) port.

The control device together with the synchronization unit ensures the operation of 1288XK1T, and also allows you organizing the joint work of several microcircuits, including synchronous start-up, cleaning of memory blocks, setting the parameters of the local oscillator and the integrated output multiplier. The devices listed above make up the core (CORE) of the 1288XK1T chip.

JTAG interface provides administrating of internal controls and allows debugging work programs 1288XK1T at a low frequency.

One component of the output sample is obtained by multiplying the input sample of the actual data by the value sin (φ), and its other component is obtained by multiplying the input sample of the actual data by cos (φ), calculated from the current value of the phase φ of the reference signal of the local oscillator stored in the phase accumulator. In parallel, a new value of the phase of the reference signal is calculated.

The output stream of complex data from the multipliers is fed to the input of the rounding device, which reduces the capacity of the data to 20 bits. The maximum sample rate at the input and output of the local oscillator is equal to the clock frequency of the CLK signal.

The frequency and phase of the reference local oscillator reference signal are controlled using 16-bit registers in the following way:
– initial phase: $\frac{2\pi}{2^{36}} \text{PHASE}$; rad,

– local-oscillator frequency: $\frac{F_s \times \text{FRQ}}{2^{32}}$, Hz,

where PHASE – value in binary additional register code X*_NCO_PHASE;
FS – input sample rate;
FRQ – 32-bit value in binary additional code {RX*_NCO_FRQH & RX*_NCO_FRQL}.

Register entry RX*_NCO_PHASE, RX*_NCO_FRQL, RX*_NCO_FRQH does not lead to the immediate change of frequency-change oscillator parameters. The local oscillator parameters are updated with new register values when “1” is written to the “sync_nco” bit of the SYNC register or by an external synchronization signal SYNC_NCO. The transition of the 1288XK1T to the stop state causes the phase accumulator to reset to the value “0”. Updating the local oscillator parameters with new values does not reset the phase accumulator.

4. Discussion
To improve the dynamic range of the SFDR local oscillator reference signal, a pseudo-random noise signal can be added to the phase generator (dithering). The added noise is a pseudo-random noise signal with zero mathematical expectation and a uniform amplitude distribution function. Switching phase dithering on and off is performed by “the pdith_en” field of the RX*_LCFG register independently for each channel [11].

The phase noise generator changes its state synchronously with the phase accumulator. Switching off dithering and the transition of the 1288XK1T to the “Stop” state causes the noise generator to be set to its initial state. This can be used to control the phase noise correlation in the PAA and AAA systems.

In the modes of the complex input signal with frequency conversion, the local oscillators of two channels are used for one signal source. In this case, the local oscillators of the 1st and 2nd channels process I and Q - components of the first signal source. The local oscillators of the 3rd and 4th channels likewise process the quadrature components of the second source. The frequencies and initial phases of the local oscillators in each pair should be the same. In the subsequent routing unit of the output flows of the CIC decimators, the components are added (subtracted) to obtain a complex signal of the converted frequency.

The block diagram of the CIC decimation filters is shown in Figure 2.

![Figure 2. The block diagram of the CIC decimation filters.](image)

The CIC decimation filters block consists of two stages, each of which includes a filter itself, a scaling unit and a multiplexer to turn off the corresponding filter.
5. Conclusion
The 4-channel 1288XKIT SDR receiver allows working with both narrow-band and wide-band communication channels (with simultaneous operation of 4 channels, the band can be expanded) and can be used in modern telecommunication systems.

6. References
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