UV laser drilling of SiC for semiconductor device fabrication

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Abstract. Pulsed UV laser processing is used to drill micro holes in silicon carbide (SiC) wafers supporting AlGaN/GaN transistor structures. Direct laser ablation using nanosecond pulses has been proven to provide an efficient way to create through and blind holes in 400 µm thick SiC. When drilling through, openings in the front pads are formed, while blind holes stop ~40 µm before the backside and were advanced to the electrical contact pad by subsequent plasma etching without an additional mask. Low induction connections (vias) between the transistor’s source pads and the ground on the backside were formed by metallization of the holes. Micro vias having aspect ratios of 5-6 have been processed in 400 µm SiC. The process flow from wafer layout to laser drilling is available including an automated beam alignment that allows a positioning accuracy of ±1 µm with respect to existing patterns on the wafer. As proven by electrical dc and rf measurements the laser-assisted via technologies have successfully been implemented into fabrication of AlGaN/GaN high-power transistors.

1. Introduction

Due to its superior properties GaN-based high-electron mobility transistors (HEMTs) attract much attention for a wide variety of power electronics applications for communications and radar [1]. High-power AlGaN/GaN HEMTs for rf applications are processed on semi-insulating SiC substrates that are typically ~400 µm thick. To boost the performance of these transistors vertical electrical interconnects (vias) with low inductivity between the source pads on the front and the ground electrode on the backside are required. SiC is one of the hardest materials and chemically inert, both of which make micro processing extremely difficult. Up to now, only advanced inductively coupled plasma (ICP) etching can provide significant etching rates of ~1 µm/min. The fabrication of vias through SiC wafers requires time-consuming mechanical thinning to a thickness of ~100 µm [2], thereby diminishing the advantageous excellent heat spreading of the highly conducting SiC. Moreover, plasma etching requires processing of a resistant mask. A novel processing approach is needed to commercialize vias in ~400 µm thick SiC substrates. SiC ceramics have been subject of several studies on ablation by UV [3-6], visible [7, 8], and IR pulsed laser radiation [9] as well as by ultrashort pulses [10-13]. UV laser processing is capable of precise patterning of single crystal SiC [14, 15] and can be used for fabrication of radiation detectors [16] and microelectronic power devices [17]. In this study pulsed UV laser processing using nanosecond pulses was applied to drill through-wafer and blind micro holes into single crystalline SiC. Laser-assisted technologies to form through-wafer vias for high-power transistors processed on 400 µm thick SiC wafers will be presented.
2. Experimental

A frequency-tripled, diode-pumped solid-state laser was used to ensure high processing speed and reliability, high-quality, and precise micromachining of silicon carbide. The 355 nm UV laser delivers 4.5 W average power at 25 kHz repetition rate and provides pulses of <30 ns. The laser was integrated into a class-1 laser-safe micromachining workstation (ILS 500 Air, InnoLas) that is located in an industry-compatible clean room with a 2“-4” process line for III/V semiconductor devices. The turnkey micromachining tool is equipped with an air-bearing XY stage that provides a maximum translation speed of 20 m/min for workpieces of up to 6” in diameter. High-speed galvo scanning optics allows a fast positioning of the laser spot on an area of 10x10 mm². The beam is focused to ~15 µm in diameter with a telecentric F-theta optics having a focal length of 56 mm. Using 4 cameras, image processing, and pattern recognition, an automated beam alignment with an accuracy of ±1 µm is realized for front-to-front as well as front-to-backside alignment [17]. Wafer layout data are imported into the CAD software package GRAFFY© (Durst CAD Consulting GmbH) for process preparation and generation of the executable program code for CNC and galvo scanning operation.

As schematically depicted in figure 1, through-wafer as well as blind holes were drilled in ~400 µm thick semi-insulating SiC substrates of 4H polytype using pulse energies of ~65 µJ at a laser repetition frequency of 20 kHz. The transistor structures grown on these substrates consist of an ~2.5 µm thick GaN-based epitaxial layer that is covered by the contact pad consisting of a metallic stack of ~40 nm titanium, ~120 nm platinum and ~5 µm gold. The laser beam is directly focused to drill holes one at a time. Different hole sizes and cross sections were realized by appropriately guiding the laser beam on the sample. The laser processing was carried out in air atmosphere.

Laser-drilled blind holes were etched by inductively coupled plasma (ICP) etching using an SI 500 ICP system and by reactive ion etching (RIE) using an SI 591 RIE system (both from SENTECH Instruments) without additional protection by a masking material (see figure 1 (b)). The laser-drilled holes formed the pattern to be projected. SiC and GaN were etched in SF<sub>6</sub>-O<sub>2</sub> and BCl<sub>3</sub>-Cl<sub>2</sub> plasmas, respectively [18, 19].

Backside and micro holes were metallized by depositing a titanium/gold seed layer followed by electroplating 5 µm of gold. The structures were examined by scanning electron microscopy (SEM).

3. Results and Discussion

3.1. Through-wafer via processing

The 4H polytype SiC used in this study has an energy gap of 3.23 eV that corresponds to an absorption edge of ~380 nm [20]. In other words, the SiC substrate is well absorbing at the wavelength of 355 nm delivered by the laser. When drilling circular holes with high aspect ratios we observed an oval exit, which can be attributed to the dependence of the reflectivity on the plane of polarization [21,
In this study we applied a partially elliptical motion of the linearly polarized beam to compensate for the non-uniform ablation due to anisotropic reflection from the sidewalls. Additionally, the diameter of the scanned contour was decreased from cycle to cycle to reduce the amount of the reflected light. Sidewalls with an inclination of 3-5° to the vertical were obtained. The sidewalls can be smoothened by repeated contour scans. Taking the mean diameter of the conical holes for calculation, aspect ratios of up to 5-6 have been realized in ~380 µm thick SiC. Depending on the sample thickness and hole diameter, the drilling time is 1-3 s per hole.

Drilling of SiC with an UV laser generates debris that is deposited around the processed spot extending to ~100 µm from the rim. This debris consists of a fluffy deposit that is loosely attached to the surfaces and can easily be wiped away (see figure 2(a)). It can be dissolved in hydrofluoric acid indicating that it mainly consists of silicon dioxide [12]. After cleaning the sidewalls of the holes are covered by a smooth layer of dross (see figure 2(b)). This layer of recast material is <5 µm thick. There are a few discrete spherical particles of solidified melt with typical diameters of <1 µm, in most cases in the order of 200 nm. At the entrance, a little burr can be found that is <4 µm in height.

After completing the front-end processing, 2” wafers with functioning transistors were drilled on-wafer to process vias between source pads of the AlGaN/GaN HEMTs on the front and the ground on the backside of the devices. The wafer’s front was protected by photoresist while the laser drilling was performed from the backside of the wafer (see figure 1 (a)). The precise front-to-backside alignment assures to hit the center of the transistor’s contact pads on the front. After cleaning with hydrofluoric acid the vias were plated through. Figure 2(c) shows a cross section of a via through a 400 µm thick SiC substrate supporting AlGaN/GaN transistor devices. Conical via holes having diameters between ~120 µm on the laser entrance and ~80 µm on the laser exit were fabricated. On-wafer dc measurements and rf characterization of mounted devices revealed no degradation of transistor performance due to collateral damage by laser-assisted via processing. AlGaN/GaN power transistors with through-wafer vias demonstrated 40 W of output power [17].

3.2. Blind via processing
For blind via formation laser drilling of SiC was stopped ~40 µm before reaching the SiC/GaN interface (see figure 1 (b)). The remaining material between the bottom of the laser-drilled hole and the SiC/GaN interface was etched using ICP (denoted by plasma 1 in figure 1 (b)) and, subsequently, the GaN was removed to the contact pads by RIE (denoted by plasma 2 in figure 1 (b)).

Holes with flat bottoms can be created with a Gaussian-shaped beam intensity by coordinating the scanning speed, the beam path on the workpiece, and the pulse repetition frequency of the laser. Figure 3(a) shows the cross section of a hole with a flat bottom in 380 µm SiC. The hole is 320 µm deep and it has an opening of 145 µm and 70 µm at the entrance and the bottom, respectively.
However, when decreasing the side length the hole profile tapers off and the control of a flat bottom is limited by the increasing impact of reflections from the sidewalls. In figure 3(b) the side lengths at the entrance and at the bottom are 75 µm and ~15 µm, respectively. There is 40 µm of SiC remaining below the bottom of the hole. A constant pulse repetition rate of 10 kHz was used. Drilling time was 2 s per hole. After cleaning the debris there is some recast left on the sidewalls particularly in the middle and near the bottom of the hole. At the entrance the sidewalls are smooth. With increasing depth the amount of resolidified material increases. Near the bottom a ~5 µm thick crust of dross is formed. This layer of recast will be removed by subsequent plasma etching and smooth sidewalls are obtained as illustrated in figure 3(c) that shows a hole pre-drilled according to the one in figure 3(b).

The selectivity of the ICP etching of SiC versus GaN with SF₆-O₂ is >100:1, for which the etching process will practically stop at the GaN layer to provide good homogeneity over a whole wafer. If the SiC backside is not protected by a masking layer, for example, such as indium tin oxide, the substrate thickness will decrease when the holes are etched down to the GaN layer. In the case presented here, the thickness decreased from 390 µm at the beginning to ~250-300 µm after 2 hours of ICP etching. The bottom of the hole was enlarged to ~60 µm and the entrance was conically expanded to a side length of ~150 µm. In a second etching step, the GaN layer was removed using a BCl₃-Cl₂ RIE plasma. Again, a high etching selectivity of GaN versus platinum of >10:1 favoured a homogeneous formation of holes stopping at the metallic front contact. In figure 3(c) a detailed view of the excavated front metal is presented showing a smooth etching morphology. It illustrates that the etching process cleanly stops at the platinum layer.

Samples with arrays of holes were processed and subsequently metallized. Resistance measurements through single vias having an aspect ratio of 3-4 revealed a good homogeneity of this via technology. The resistance through ~250-300 µm thick semi-insulating SiC was 27±2 mΩ.

4. Conclusions

Micro processing using nanosecond UV pulses was successfully implemented into back-end processing of advanced high-power AlGaN/GaN HEMTs on 400 µm semi-insulating SiC. Drilling strategies were successfully developed to create through-wafer and blind micro holes that meet the quality requirements for processing low inductance interconnects between source pads of transistors on the front and the ground on the backside of the devices. The laser-drilled blind holes can be etched to the metallic front contact by ICP and RIE without additional mask. Low inductance interconnects could be established by plating both through-wafer and blind vias. The successful implementation of the laser-assisted via formation into device processing was proven by dc and rf transistor performances. Such results demonstrate that laser micro processing of hard and inert materials can be an alternative when conventional lithography and etching technologies fail or are not cost-effective.
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