A design method of CPR for wide voltage design

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Abstract In this paper, we proposed an improved design method of critical path replica (CPR) for wide voltage design. Timing accuracy of CPR in wide operating voltage is improved by applying load matching and transistor-level static timing analysis (TSTA). We applied proposed method to 100 critical paths of iscas’95 benchmark circuits, the results of simulation experiments in SMIC 55 nm shows that the CPR designed by proposed method can operating between 0.3 V–1.2 V with only 0.25% delay error (DE).

Keywords: low voltage, wide voltage, subthreshold, delay line, resilient circuits, low power

Classification: Integrated circuits

1. Introduction

With the development of portable device and IoT, the ultra-low power circuits with wide voltage operating range become popular \cite{1, 2, 3}. As the voltage decreases, the power consumption exhibits a quadratic reduction and there is an optimal point of energy consumption \cite{4, 5, 6}. When the power supply voltage decreases, the circuit timing is sensitive with the PVT variation \cite{7, 8}. Critical path replica (CPR) is a kind of delay line, which mimic the delay of critical path for timing monitoring \cite{9, 10}. CPR is widely used in digital DLL \cite{11}, adaptive and resilient circuits for timing violation detection \cite{12, 13, 14, 15} and asynchronous circuits for delay matching of handshake \cite{16, 17, 18, 19}. However, few literatures study the design method of CPR for wide voltage design. In order to accommodate the needs of wide voltage circuits, it is important to design a CPR that accurately mimics critical path delays over a wide voltage range. Similar to literature \cite{20}, the delay error (DE) of CPR can be defined as follows,

$$DE = \frac{D_{\text{CPR}} - D_{\text{expected}}}{D_{\text{expected}}} * 100\%$$

Where the $D_{\text{CPR}}$ is the delay of CPR and the $D_{\text{expected}}$ is the delay of the critical path with appropriate ratio of margin. We hope that the delay of CPR is greater than and close to the delay of the critical path, so in the case of a CPR margin of 2%, the value of DE cannot be less than $-2\%$. This paper proposed an improved CPR design method based on load matching (LM) and its design flow. Proposed method has applied to 100 critical paths extracted from ISCAS’95 benchmark circuits. The experimental results show that the proposed method can accurately track the delay variation of the critical path over the full voltage range, and pays 35% of the area overhead compared to the inverter line.

2. Literature review

The existing CPR design methods mainly include inverter line \cite{13, 21, 22}, mixed-gate CPR \cite{23, 24} and UDL (Universal Delay Line) \cite{25}. The inverter line is the most commonly used CPR and its design is simple \cite{26, 27}. However, the experiments in the later part of this paper show that its Delay-Voltage characteristics are very different from the real critical paths, with poor DE at wide voltage operating range, so it must be calibrated frequently in practical applications. The mixed-gate CPR is a combination of a plurality of delay lines composed of different gate structures, which have wide voltage operating range, but have a large area overhead. Literature \cite{28} proposed a design method of inverter line by adjusting the W/L of transistor to satisfy the requirement of wide voltage design. However, its delay accuracy has not been improved. In \cite{12}, a UDL (Universal Delay Line) structure (Fig. 1(c)) is proposed to constitute CPR, it can be easily transplanted between designs. The experiment in this paper shows that its DE is large.

Fig. 1. (a) The real critical path (b) mixed gate CPR (c) UDL CPR (d) proposed CPR
3. Proposed method

The delay of logic path is composed of gate delay and wire delay. Wire delay is not sensitive with voltage scaling [29]. In low-voltage circuits, the ratio of wire delay to path delay is small. A critical path simulated at SMIC 55 nm 0.6 V shows that the wire delay only account for less than 2% of total delay. The gate delay is the dominant component of the path delay of the low-voltage circuit, and the gate delay varies greatly with voltage. Under certain PVT conditions, the gate delay is determined by the following formula.

\[ T_{\text{delay}} = f(Tr, C) \]

Where the \( Tr \) is the input transition, \( C \) is the output load. Therefore, we can get CPR of a critical path by mimicking the logical gates through which the critical path passes and the load on the intermediate nodes of the critical path. The load on the node is reflected by its fan-out number. Fig. 1(a) shows an example of a critical path and its corresponding two CPR implementations. Fig. 1(b) is mixed-gate CPR. Tunable delay line is used for delay calibration. Fig. 1(c) is the UDL proposed by [6]. Fig. 1(d) is a CPR designed by proposed method. We proposed the design flow of LM CPR as Fig. 2. The target circuit is a circuit that requires timing monitoring. Performing transistor-level static timing analysis (TSTA) on the target circuit to obtain timing reports of critical paths. TSTA has the accuracy of a SPICE level to identify critical paths accurately. Then, extract the topology of the critical path and the fan-out number of the critical path node \( Ni \) from the timing report. Next, we insert \( Ni-1 \) inverters into the corresponding nodes in the CPR according to the fan-out number of the intermediate nodes of the critical path. At this point, the CPR with the load matching the critical path is obtained, but its delay need to be slightly larger than the critical path by adding a small delay margin. Literature [30] was found through statistical analysis that the delay line formed by the NOR gate has similar Delay-Voltage characteristics with most critical paths. Therefore, the delay margin in this paper is composed of NOR gates. We have conducted Monte-Carlo simulation for local variation by HSPICE, and finally choose 2% margin for CPR. In the end, we get the LM CPR needed for the design.

The selection of critical path is an important issue, which is a tradeoff between area overhead and timing monitoring accuracy. We have applied the method of selecting the critical path for wide voltage design proposed in [8]. The difference is that we apply a more advanced and accurate transistor-level static timing analysis (TSTA) method instead of the traditional gate-level static timing analysis (GSTA) method which has a better accuracy in critical path identification.

We applied proposed method to 100 critical paths of iscas’95 benchmark circuits. Our experimental method is as follows. First, we adjust the CPR delay at 1.2 V to make it 102% of the critical path delay and the extra 2% as the delay margin. Then gradually reduce the voltage to observe the change of DE with voltage. This means that CPR fails when the value of DE is equal to ~2%. The failed point voltage between 1.2 V is the normal operating voltage range of CPR. Fig. 3 is a simulation result of the inverter chain, UDL, mixed-gate and the LM CPR delay with voltage. The vertical axis is the DE of CPR. As shown in the Fig. 3, when the voltage drops to 0.98 V, the delay of the inverter chain starts to be less than the critical path, indicating that it is not suitable for wide voltage applications. UDL does have a much wider operating voltage range and a smaller DE than inverter line, but its failure voltage is still high and is not suitable for subthreshold circuits. Mixed-gate CPR can work correctly over a wide voltage with the penalty of large area and power. The proposed LM CPR has a wide voltage operating range of 0.3 V to 1.2 V and 0.25% DE. Table I shows a comparison with other related works.

![Fig. 2. Design flow of LM CPR](image)

![Fig. 3. DE versus voltage](image)

**Table I.** Compare with other CPRs

|               | Inverter | UDL   | Mixed-gate | Proposed |
|---------------|----------|-------|------------|----------|
| *Active area  | 1        | 0.5   | 4.8        | 1.35     |
| Voltage range | 0.98–1.2 V | 0.68–1.2 V | 0.3–1.2 V | 0.3–1.2 V |
| Max | DE% | 33% | 21% | 3% | 0.25% |

*Active area indicates the area of the total transistors normalized to the inverter line.
4. Conclusion

This paper propose a CPR design method by load matching for wide voltage design. The experiment on 100 critical paths extract from iscas95' benchmark shows that proposed method get a better timing accuracy and wider operating voltage range compared with existed design method.

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