A scalable readout system for a superconducting adiabatic quantum optimization system

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Abstract

We have designed, fabricated and tested an XY-addressable readout system that is specifically tailored for the reading of superconducting flux qubits in an integrated circuit that could enable adiabatic quantum optimization. In such a system, the flux qubits only need to be read at the end of an adiabatic evolution when quantum mechanical tunneling has been suppressed, thus simplifying many aspects of the readout process. The readout architecture for an $N$-qubit adiabatic quantum optimization system comprises $N$ hysteretic dc SQUIDs and $N$ rf SQUID latches controlled by $2\sqrt{N} + 2$ bias lines. The latching elements are coupled to the qubits and the dc SQUIDs are then coupled to the latching elements. This readout scheme provides two key advantages: first, the latching elements provide exceptional flux sensitivity that significantly exceeds what may be achieved by directly coupling the flux qubits to the dc SQUIDs using a practical mutual inductance. Second, the states of the latching elements are robust against the influence of ac currents generated by the switching of the hysteretic dc SQUIDs, thus allowing one to interrogate the latching elements repeatedly so as to mitigate the effects of stochastic switching of the dc SQUIDs. We demonstrate that it is possible to achieve single-qubit read error rates of $<10^{-6}$ with this readout scheme. We have characterized the system level performance of a 128-qubit readout system and have measured a readout error probability of $8 \times 10^{-5}$ in the presence of optimal latching element bias conditions.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Many proposals exist for how to build superconducting quantum computing systems [1, 2], each with their own unique challenges. One such proposal is to enable adiabatic quantum optimization (AQO) using networks of inductively coupled rf SQUID flux qubits [3–5]. In this version of AQO, one first maps an optimization problem of interest onto that of minimizing a classical energy function $V_{IS}$, describing a set of binary variables $i = 0 \cdots N$, each having a possible state $s_{z,i} = \pm 1$, with applied local biases $\epsilon_i$ and pairwise couplings $J_{ij}$:

$$V_{IS} = \sum_{i=0}^{N} \epsilon_i s_{z,i} + \sum_{i \neq j} J_{ij} s_{z,i} s_{z,j}.$$  

One then embeds this potential into a physical quantum Ising spin system with a controllable transverse magnetic field term $T = \sum_{i=0}^{N} \Delta_q s_{x,i}$. This physical system is described by the quantum Ising spin Hamiltonian $H_{IS}$:

$$H_{IS} = T + V_{IS} = \sum_{i=0}^{N} \Delta_q s_{x,i} + \sum_{i=0}^{N} \epsilon_i s_{z,i} + \sum_{i \neq j} J_{ij} s_{z,i} s_{z,j}.$$  

where $s_{x,i}$ and $s_{z,i}$ are Pauli matrices acting on the $i$th spin.

The AQO algorithm proceeds by first initializing the processor in a state wherein all single-spin tunneling energies $\Delta_q$ (proportional to the transverse magnetic field) are much larger than the energy scales involved in the problem of interest. In this case, all spins will readily relax into their ground states. Thereafter, the AQO algorithm for finding an
optimal solution proceeds by smoothly decreasing $\Delta_q$ in time from a large value until it is much less than the energy scales involved in the problem of interest. If the resultant evolution of the state of the processor is adiabatic, then its final state will encode an optimal solution to the problem of interest.

Details of how an Ising spin system with an effective transverse magnetic field is implemented using superconducting flux qubits can be found in [6]. Briefly, rf SQUID flux qubits are used to represent localized spins, with the spin state being encoded directly in the circulating current of the rf SQUID [7]. Each rf SQUID has a local flux bias providing the effective applied longitudinal field term $\epsilon_i$. The effective transverse magnetic field at each spin is realized via the tunneling between the two circulating current states as provided by the presence of at least one Josephson junction in the rf SQUID. Tunable inductive coupling between the rf SQUID flux qubits [8] provides the effective spin–spin coupling terms in the Ising spin Hamiltonian.

The challenge that is addressed in this paper is that of reading the final state of an AQO processor. Note that at the end of the AQO algorithm $\Delta_q$ is negligible, thus naturally terminating the evolution in a state that is diagonal in the qubits’ flux bases. This is in contrast to a general-purpose gate model (GM) quantum information processor in which the final state of the processor could be a superposition state due to appreciable $\Delta_q$. The method presented in this paper for distinguishing the flux in a large number of devices should also find use in classical superconducting logic circuits.

Several methods for reading the state of a flux qubit in its flux basis have been reported upon in the literature to date. One approach is to inductively couple a qubit to a hysteretic dc SQUID and then interrogate the latter device using either a current bias ramp [9, 10] or carefully crafted current pulse [11]. Either way, the objective is to discern the current bias at which the dc SQUID switches into the voltage state, which depends upon the flux imparted to the dc SQUID by the qubit. One key advantage to this readout mechanism is its physical size: dc SQUIDs can be made relatively small, thus providing favorable prospects for utilizing such a readout mechanism in many qubit processors. Furthermore, as shown in this paper, one can design scalable readout biasing architectures based upon dc SQUIDs that make economical use of a limited number of external bias controls. On the other hand, while hysteretic dc SQUIDs were used in early GM quantum computation experiments, they have fallen out of favor due to on-chip heating and back-action on the qubits. The first of these drawbacks could be remedied, in principle, by better thermal design. The second drawback is less of an issue for AQO as the quantum computation itself naturally localizes the state of each qubit by making $\Delta_q$ negligible by the end of the computation, thus inhibiting transitions within the qubit. As such, hysteretic dc SQUIDs could still be of use in designing scalable readout architectures for AQO processors.

Note that readout architectures based upon scalable dispersive techniques [12, 13], which may yet prove to be essential in the development of GM processors, take up significantly more physical space than those based solely upon hysteretic dc SQUIDs. Nonetheless, future developments may eventually make dispersive readout methods an attractive option for an AQO.

While the arguments presented above suggest that the relatively simple hysteretic dc SQUID readout may be useful in the development of large scalable AQO processors, our research has revealed one more drawback of such an approach. It is well known that unshunted dc SQUIDs can resonate when switched into the voltage state, thus acting as an on-chip source of microwave radiation. While this feature has been exploited to resonantly excite flux qubits in novel quantum mechanics experiments [14], this behavior would be highly undesirable in a future functional quantum information processor. We have observed that this behavior is particularly problematic in dense superconducting circuits as the radiation generated by a dc SQUID can resonantly drive multiple flux qubits within its vicinity, thus altering their final states. Part of this issue may simply be an unfortunate choice of rf SQUID parameters: the design pressures in an AQO processor tend to favor flux qubits with large geometric inductances so as to facilitate multiple inter-qubit inductive couplings. Consequently, in order to achieve appreciable $\Delta_q$ during the AQO algorithm, one must lower the designed critical current of the rf SQUID, thus yielding a flux qubit with a relatively low tunnel barrier over which radiation from dc SQUIDs can drive resonant activation. This is clearly unacceptable, as the solution to the optimization problem that has been posed to the processor is then corrupted by the act of reading. The novel approach that we have implemented to remedy this problem is to insert a quantum flux parametron (QFP) [15, 16] between each qubit and its dedicated dc SQUID. The QFP is an rf SQUID that possesses a small inductance, a large capacitance and a very large critical current. Consequently, the QFP possesses a substantially larger tunnel barrier as compared to the flux qubit, which makes its state robust against high frequency radiation emanating from dc SQUIDs in the voltage state. In our architecture, the QFP is used to quietly latch the final state of a given flux qubit with minimal back-action. Thereafter, the final state of the QFP is read using a hysteretic dc SQUID. Thus, the QFP and dc SQUID combination provides a viable route to a scalable readout architecture that is suitable for an AQO processor.

2. Readout circuit design

Figure 1 shows a high level schematic of a small portion of an XY-addressable readout system. Since this paper is focused upon the readout architecture, we have suppressed the details of the flux qubits and their control circuitry and refer the reader to [7, 17] for information concerning those elements. Each qubit in the circuit requires two elements for readout: a dc SQUID and a QFP. Each dc SQUID has two shared control lines: a current bias ($cb_0, cb_1, \ldots$) and a flux bias ($fb_0, fb_1, \ldots$). All QFP latches share a single activation line

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1 For comparison, typical barrier heights in rf SQUID phase qubits reported in the literature are $\sim$1 THz, as compared to $\sim$500 GHz for our flux qubits. When we design our qubits to have tunnel barrier heights that are in excess of $\sim$1 THz, we do not observe resonant activation. Unfortunately, such flux qubits are not optimal for use in AQO as problems related to Josephson junction critical current variation are accentuated.
Figure 1. XY-addressable readout system schematic. Each dc SQUID has two shared control lines: a current bias (cb0, cb1, ...), and a flux bias (fb0, fb1, ...). All QFP latches share a single activation line (‘QFP latch’) and a single flux bias line (‘QFP flux bias’). The qubits are discussed in detail in [7, 17].

Figure 2. (Top) Layout of a portion of an XY readout system. Note that all of the elements are shielded with a ground plane. The region shown above is 47 x 50 μm^2. There are four Nb metal layers: BASE (red), WIRA (blue), WIRB (green diagonal hashed) and WIRC (beige), and RESI (green dotted) is a Ti/Pt resistor layer. Junctions are denoted as AlO\textsubscript{x}/Al (pink circles) and vias are denoted by crossed rectangles. (bottom) Cross section of the planarized fabrication process. All metal layers have a nominal thickness of 300 nm and the dielectric thickness is 200 nm.

At a high level, the readout circuit functions as follows: during the course of an adiabatic quantum computation, all current biases cb\textsubscript{x} and flux biases fb\textsubscript{y} are set to zero, thus ensuring that the dc SQUIDs are in the zero voltage state. In order to decouple the QFPs from the flux qubits, the QFP latch line is set to provide 0\approx\Phi_{0}/2 to all QFPs, thus suppressing their persistent currents to negligible levels. Once the qubits have reached their final states at the end of an adiabatic quantum computation, the waveform sequence depicted in figure 3 is applied to the readout circuitry. First, the QFP latch bias is raised to provide 0\approx\Phi_{0}/2 to all QFPs, thus raising the QFP tunnel barriers (see figure 4), which adiabatically changes the state of each QFP from being the ground state of a monostable potential to being the ground state of a bistable potential. The direction of the resultant ground state persistent current flow about the body of each QFP is determined by the polarity of the flux imparted by the qubit to which each QFP is coupled. At the end of this linear ramp the height of the QFP tunnel barriers ΔU\textsubscript{qfp} has been raised to a sufficiently high level so as to preclude further dynamics (ΔU\textsubscript{qfp} ≫ \hbar/\sqrt{L\textsubscript{qfp}C\textsubscript{qfp}} ≫ k_b T, where T is the temperature of the chip) and the final states of the flux qubits have been latched into the QFPs. Thereafter, a linear current ramp is applied to the bias cb\textsubscript{x} whose maximum amplitude is significantly lower than the maximum dc SQUID switching current I\textsubscript{sw}max amongst the population of dc SQUIDs connected in series with cb\textsubscript{x}, so that only the dc SQUID with a flux bias applied to its fb\textsubscript{y} line is triggered (see figure 5). The timing of a voltage arising across the dc SQUID is then measured: if the flux arising from the QFP increases (decreases) the total flux applied to the dc SQUID address by cb\textsubscript{x} and fb\textsubscript{y}, then switching to the voltage state will happen sooner (later) (see figures 3 and 7). This difference in timing reveals the state of the QFP and therefore
AQO processor. Furthermore, typical AQO architectures require a substantial number of inter-qubit couplings [3] which necessitates larger $L_q$ than may be considered appropriate in the study of flux qubits for implementing GM hardware. As such, the flux qubits in our circuits tend to possess substantially smaller $I_c$ in order to realize appreciable single-qubit tunneling energies $\Delta^q$ over as broad a range of the annealing parameter as is practical. Consequently, our flux qubits appear to be more susceptible to resonant activation by dc SQUID switching transients than other flux qubits reported upon in the literature.

2.2. QFP latch

The QFP is a two-junction rf SQUID, which, in comparison to our flux qubits [7], possesses a lower inductance $L_{qfp} \approx 65$ pH and a substantially higher critical current $I_{c, qfp} \approx 12 \, \mu$A. Consequently, the former device has a maximum $\beta_{qfp} = 2 \pi L_{qfp} I_{c, qfp} \Phi_0 = 2.37$, a maximum persistent current $I_{p, qfp} \approx 10.5 \, \mu$A and a maximum tunnel barrier between its two persistent current states of the order of $\Delta U_{qfp} \approx 3.4 \, $THz (compared with 0.46 THz for the qubit). The effective one-dimensional potential energy of a QFP with identical Josephson junctions can be written as

$$U_{qfp} = -\frac{\Phi_0 I_{c, qfp}}{2 \pi} \cos \left( \frac{\pi \Phi_{latch}}{\Phi_0} \right) \cos \left( \frac{2 \pi \Phi_{latch}}{\Phi_0} \right) + \frac{1}{2} I_{qfp} \Phi_{latch}^2 \Phi_{latch}^2 \Phi_0$$

where $\phi = 2 \pi \Phi_{qfp} / \Phi_0$ is the mean phase across the two Josephson junctions. Note that in tuning $\Phi_{latch}$ from $\Phi_0 / 2$ to $\Phi_0$, $U_{qfp}(\phi)$ morphs from being monostable to being bistable (see figure 4). Raising $\Phi_{latch}$ slowly adiabatically latches the state of each flux qubit into the QFP to which it is coupled. Adiabaticity is guaranteed here due to the large signal from the qubit and the relatively low bandwidth of the QFP latch line, which has a rise time of approximately 1 $\mu$s. Adiabaticity is violated during the latching phase only if there is no signal applied to the QFP, as the two QFP circulating current states are then degenerate in energy in the large $\beta_{qfp}$ limit. Note that, if the qubit state were to be unchanged after dc SQUID switching, then the QFP could be operated fully reversibly: the QFP could then be reset in the presence of the signal to which it was initially latched, so the whole cycle of barrier raising and lowering would then be adiabatic.

One challenge in designing QFPs (or any two-junction rf SQUID) is that junction asymmetry leads to a $\Phi_{latch}$-dependent effective flux offset [7]. This offset limits how small one can make $M_{qfp,qfp}$, as one would like the bimodal qubit signal to straddle any such flux offset for values of $\Phi_{latch}$ about which the QFP becomes bistable. Assuming a typical fabrication spread of 1% in junction critical currents and a maximum $\beta_{qfp} \sim 2.5$, this offset could be up to 4 $\mu$T. For this reason, we had chosen $M_{qfp,qfp}$ such that $2 I_{qfp} M_{qfp,qfp} \approx 10 \mu$T.

There are two other features of the QFP latch that make it useful beyond the qubit state readout method described thus far. Linear detection: by biasing the QFP such that $\beta_{qfp} \sim 1$, it can be used as a preamplifier acting on the signal from the qubit. Realistically, achieving appreciable net flux gain into the

2.1. Qubit signal

For the purposes of reading the final state of the flux qubits in an AQO processor, the relevant signal is the magnitude of the qubit persistent current when the qubit tunnel barriers have been raised to their maxima. The flux qubits used in our circuits are of the type described in [7] and had inductances $L_q \sim 300$ pH, of which 10 pH was reserved for readout, and critical currents $I_{c, q} \sim 2.2 \, \mu$A. During readout, the qubit $\beta_Q = 2 \pi L_q I_{c, q} / \Phi_0 \sim 2$, corresponding to a circulating current of roughly $I_{c, q} \sim 2 \, \mu$A. A typical mutual inductance from the qubit into its corresponding QFP is $M_{qfp,q} \sim 5.4$ pH, leading to a qubit signal as seen by the QFP of $2 I_{c, q} M_{qfp,q} \sim 10 m \Phi_0$.

For the qubit parameters cited above, the maximum tunnel barrier height between flux states would be $\Delta U_q / h \sim 460$ GHz. The design pressures that led to this choice are discussed in detail in [7, 17] and so we only briefly repeat the relevant points herein. While in theory one could design flux qubits with larger $I_{c, q}$ (and thus a larger $\Delta U_q$ to provide immunity to any dc SQUID driving signal) both asymmetry in the qubit junctions and finite precision on the qubit analog flux biases would eventually limit circuit performance as an
dc SQUID requires careful tuning of the QFP and dc SQUID biases. Instead, to readily use the latching detector as a linear preamplifier, we apply flux feedback in software to the QFP body loop, \( \Phi_{\text{qfp}} \), to keep the QFP at its balance point where we have a 50\% probability of measuring it in either of its persistent current states after latching. The required \( \Phi_{\text{latch}}^{*} \) is then a linear representation of the signal from the qubit. At this balanced population point, the QFP has minimal back-action on the qubit and can be used to probe the magnitude of the circulating current of the qubit. We use this mode of operation of the QFP in order to calibrate qubit parameters, as described in [7].

**Figure 5.** Critical current \( I_c \) versus applied flux for a typical dc SQUID. Applying a signal via the fb, line allows a user to shift the operating point on the abscissa for a given row of dc SQUIDs. Then when a current bias is applied to the cb, line, only those SQUIDs whose critical current \( I_c \) has been suppressed will switch.

The method for using a hysteretic dc SQUID for flux detection is discussed in [18] and more generally in [9, 10]. For the implementation discussed herein, current ramp times were typically 10–100 \( \mu s \) and peak voltages from the dc SQUIDs after switching were typically kept much less than the gap voltage of Nb to reduce the heating on chip. The mutual inductance from the dc SQUID to the QFP was \( M_{\text{dc,qfp}} \sim 1.4 \text{ pH} \).

Basic operation of the XY-addressable array of dc SQUIDs is presented in figure 3. To read out the \( i \)th column and \( j \)th row QFP, we set the value of the current in the fb, line in figure 1 to provide a flux bias of approximately 0.35\( \Phi_0 \) into the dc SQUIDs on that row and \( \Phi_{\text{qfp},ij} = 0 \) on all other rows. This results in the selective suppression of the critical current for only the dc SQUIDs in row \( j \) to \( I_c = I_{c0} \cos(\pi 0.35) = 0.45 I_{c0} \). Then, applying a current ramp on the column cb, of maximum amplitude 0.5\( I_{c0} \) will cause the target dc SQUID to switch at a time that gives information about the flux coupled into dc SQUID \( ij \) from its QFP. In other words, the fb, lines are used to row select by flux biasing all dc SQUIDs in the target row to a bias point where a current ramp on the dc SQUID will trigger readout (see figure 5). The cb, lines are used as column selects and all other current biases are kept at zero. After we
have registered an event, the current biases are reset to zero and the
process repeated for all combinations of $i$ and $j$.

For devices with less than a few thousand qubits it is
feasible to provide enough analog lines to run an XY-
addressable readout scheme as described. Modifying this
readout scheme by adding another control direction, for
example an XYZ-addressable readout scheme where X and Z
are summed together into the dc SQUID flux bias, changes
the scaling of the number of required wires to a cube root of
the number of qubits, thereby allowing us to practically scale
up to reading tens of thousands of qubits. If margins on the
XYX-addressable scheme are too low, then we can implement
the QFP shift register method described earlier which uses
a constant number of analog lines. In that case we can use excess
analog lines to decrease readout time or increase operating
margins.

2.4. Electronics

The electronics to run the readout and qubit control were
integrated into a compact rack system with 128 output
channels, a fraction of which were devoted to readout. The
dedicated readout channels had an amplifier, a tunable
comparator chain and retriggerable timers in order to detect
multiple SQUID switching events per channel. For the
purposes of characterizing test circuits, we limited the readout
sequence to a rate of approximately one dc SQUID switching
event/100 μs/channel. Without modifying the line bandwidth
(3 MHz), this could in principle be sped up to roughly
one event/5 μs. Further speed-up could be obtained by
reading multiple columns simultaneously, but we have some
experimental evidence that rf isolation between columns needs
to be improved as dc SQUIDs from different columns can
possibly interfere. With further work, one can likely reach
the bandwidth limitation of the wiring in the refrigerator. For
example, if a particular chip were to have 32 columns of dc
SQUIDs and each line had a bandwidth of 3 MHz, one could
obtain roughly a 50 Mbit s$^{-1}$ readout rate.

2.5. Power consumption

The readout process dissipates energy onto the chip whenever
a dc SQUID is in the voltage state. An upper bound on the
total energy dissipated by the readout process can be estimated
as follows: after the dc SQUID switches to the voltage state,
the large capacitance of the refrigerator wiring and filtering
($C = 2n F$) starts to charge with a rate set by $\frac{dV}{dt} = \frac{I_{\text{switch}}}{C}$,
typically $\sim 500 \mu V \mu s^{-1}$. For simplicity, we ignore the first
several nanoseconds after switching which are dominated by
transients and ringing as the lines are not matched to the high
impedance the dc SQUIDs present upon switching. Until the
dc SQUID reaches a significant fraction of the gap voltage
there is little dissipation on chip. For fast operation we
typically restrict the charging time to less than two to three
microseconds to keep the dc SQUID from charging to the gap
voltage and generating heat. For the data presented in this
paper, though, we allowed many microseconds to pass (see
figure 7). The resulting dissipated energy is $\Delta t \times 2.8 \text{ mV} \times
1 \text{ μA} \sim 28 \text{ fJ}$. If we performed this same inefficient procedure
with a 100 μs readout cycle, we would obtain an average
dissipated power during readout of $\sim 280 \text{ pW}$, which would be
well within the capabilities of a standard dilution refrigerator
to dissipate.

3. Challenges

While we routinely fabricate and operate XY-addressable
readout systems based upon the architecture described herein,
there were some formidable challenges that had to be overcome
in order to operate them to their full potential. While the typical
challenges associated with proper design of cryostat wiring,
filtering and shielding were encountered, we focus here on only
those issues directly related to the readout scheme.

First, challenges related to fabrication yields are typically
soft failures where one loses either a row or a column or even
a single readout element. Since the readout system discussed
herein was typically part of a large integrated circuit, it was
possible to at least study large portions of a circuit even in the
presence of a few fabrication errors.

Related to fabrication yield is the issue of critical current
variation across a chip. For the dc SQUIDs, small variations
of critical current are not a significant issue as there is plenty
of range between OFF and ON switching currents in this XY-
addressing scheme. The more frugal XYZ-addressable scheme
described earlier, though, would come at the expense of a
reduced ON and OFF switching current ratio in the presence
of realistic critical current variations.

Similar to critical current variation, flux offsets of each dc
SQUID lead to reduced ON/OFF margins as well. In practice,
this proved to be the key challenge to operating large-scale XY-
addressable readout schemes in our laboratory. We now use a
combination of passive magnetic shielding and active magnetic
field compensation to achieve fields below 1 nT perpendicular
to the chip. We still typically end up with flux offsets of a
few mΦ0 in QFPs and dc SQUIDs, which may be due to local
magnetic impurities on the wiring or in the magnetic shielding.
Cross-talk, both between off- and on-chip wiring, similarly
reduces operating margins.

For the QFPs, asymmetry in the critical currents of their
two Josephson junctions directly create an apparent flux offset
that competes with the qubit signal, as discussed previously.
Due to the threshold-like latching, small differences in critical
current do very little, while large differences render the device
unusable as the qubit signal cannot overcome the asymmetry-
induced flux bias acting on the QFP. Typical requirements are
less than 2% junction critical current asymmetry in the QFP in
order for the device to be operable.

A further subtle effect, which is relevant to fast operation
of the readout circuit, is thermally induced hysteresis. If one
tries to perform experiments with a fast repetition rate (for
tuned dc SQUID ramps, this rate is typically 100 μs), then
the chip temperature is affected by dc SQUID heating (see
the discussion in section 4 below). This dc SQUID heating
depends quite strongly on when the dc SQUID escapes to
the voltage state, and therefore what signal is applied to the
dc SQUID. We have found that to measure any temperature-
dependent phenomena, such as the transition width of a QFP or
Figure 6. Characterization of QFP flux sensitivity. QFP state after latching as a function of flux added from the QFP flux bias line $\Phi_{qfp}$. The data (circles with error bars) are fitted to equation (4) (solid line), signifying that the detection is thermal-noise-dominated. The transition width is $142 \mu/\Phi_0$, which is to be compared to typical qubit signals of $10\mu/\Phi_0$.

qubit, where one simultaneously requires high speed and high accuracy measurements, we needed to temperature-stabilize the mixing chamber of the dilution refrigerator at 35–40 mK (far above the $<10$ mK base temperature of the refrigerators) and take care to minimize the time the dc SQUID stays in the voltage state.

4. Readout errors

Our research has shown that there are two principal mechanisms response for imperfect readout in our XY-addressable readout. The first mechanism is the thermal noise on the QFP and the second mechanism is the uncertainty in the switching time of the dc SQUID caused by the stochastic nature of the quantum tunneling from the zero voltage state to the voltage state [19]. Each of these error mechanisms will be discussed below.

Examining the first error source, figure 6 shows the measured flux transfer curve of a typical QFP device, as obtained by latching the QFP state in the presence of a constant flux through the QFP flux bias line. The data represent the obtained by latching the QFP state in the presence of a constant measured flux transfer curve of a typical QFP device, as discussed below.

The data (circles with error bars) are fitted to equation (4) (solid line), signifying that the detection is thermal-noise-dominated. The transition width is $142 \mu/\Phi_0$, which is to be compared to typical qubit signals of $10\mu/\Phi_0$.

When operated with dc SQUID current biases tuned to minimize heating, or with sufficient cooling time such as the effective 47 mK data shown in figure 6, we obtain a corresponding flux sensitivity of the QFP of $k_B T/I_{p,qfp} = 142\mu/\Phi_0$. For comparison, the qubit signal coupled to the QFP is of the order of $10\mu/\Phi_0$. This results in practically zero error probability for the latch.

The QFP flux uncertainty $(142\mu/\Phi_0)$ is significantly better than that of its accompanying dc SQUID, which was estimated to be $1.8\mu/\Phi_0$ from the width of its switching distribution. This dramatic difference in sensitivity arises from the fact that dc SQUID noise results from the stochastic nature of quantum tunneling from the zero-voltage to the finite-voltage state with an equivalent temperature of several hundred mK, while the QFP annealing step leads to a thermal uncertainty near the refrigerator temperature of 40 mK.

Focusing now on the second error mechanism, figure 7 shows measured switching histograms of a single dc SQUID for the case when its respective qubit is first initialized in one state (red) and then in the other (blue). While the dc SQUID switching distributions are characteristic of quantum tunneling and thus asymmetric, we can still characterize the dc SQUID sensitivity by the standard deviation of the switching histogram. The abscissa can be converted from time to flux by direct measurement of the shift in switching time as a known amount of flux is applied to the dc SQUID. The resulting dc SQUID sensitivity is $1.8\mu/\Phi_0$ per read and the signal from the QFP latch is $11.9\mu/\Phi_0$, resulting in a measured error probability of the dc SQUID in reading the QFP as small as 0.01. This is a reasonably low error probability, but we require even lower error rates in order to implement a large-scale AQO processor. It is trivial to decrease this dc SQUID limited error by taking more samples of the dc SQUID switching.

\[
P = \frac{1}{2} \left( 1 - \tanh \left( \frac{2\Phi_{qfp} I_p}{k_B T} \right) \right).
\]
time since the QFP maintains its state between these samples. The results of this repeated reading of the dc SQUID on its resolving power are shown in figure 7. After two reads, the dc SQUID sensitivity increases to $1.3m\Phi_0$ and after four reads to $0.9m\Phi_0$. At four reads we obtain an error probability of $10^{-6}$. This error probability includes qubit initialization errors, QFP errors and dc SQUID errors. This behavior, while varying slightly quantitatively, was similar for all eight readouts on the particular test chip used to generate these data.

To demonstrate the performance of a large-scale XY-addressable readout system, we present the results of a system level margin measurement from a 128-qubit chip in figure 8. This particular chip had two flux biases to provide $\Phi_{qfp}$ to the 128 QFPs: the two lines each biased 64 QFPs, with the two groups partitioned depending upon the physical orientation of the QFP body and denoted as ‘horizontal’ or ‘vertical’. The reader is referred to [6] for a description of the 128-qubit chip physical layout. We then studied the error probability of the readout system as a function of horizontal $\Phi_{qfp,h}$ and vertical $\Phi_{qfp,v}$ QFP biases. In order to render the readout test independent of the details of quantum annealing, we prepared the 128 qubits in a known state by setting all of the inter-qubit couplings to zero [18], biasing all qubits using their local flux sources [17] hard to one side and then raising their tunnel barriers. This placed each flux qubit into a known state with flux sources hard to one side and then raising their tunnel coupling to zero [18], biasing all qubits using their local.

Figure 7. Reducing readout errors with repeated dc SQUID sampling of the QFP state. The dc SQUID is interrogated with a 50 $\mu$s long linear current bias ramp. The red and blue curves correspond to different initialized flux states of the qubit (which is then adiabatically transferred to the QFP). The three lines (from thin to thick) correspond to one, two and four averaged reads of the dc SQUID. Once four reads are performed we see no overlap in the dataset, which was four million points. From the thick lines we extract an error probability of $10^{-6}$ that is quoted in the text. The small steps in the switching histograms are due to the resolution of the room temperature electronics. The measurements shown in this plot were obtained from one readout on an 8-qubit chip.

Figure 8. Measured QFP margins on a 128-qubit circuit. Three concentric black rings represent contours where the system returned 1/128, 4/128 and 9/128 failures, respectively, from inside to outside. The dashed blue box indicates the designed operating margins.
5. Conclusions

We have described and implemented a scalable XY-addressable readout scheme that is suitable for a superconducting adiabatic quantum optimization system and measured the readout error rate and margins of an 8- and 128-qubit system, respectively. We conclude that the single-qubit readout error rate can be made less than $10^{-6}$ using the QFP-enabled architecture, which makes readout errors a non-issue for large-scale integrated circuits of the types considered herein. We have experimentally demonstrated a system level error rate of $8 \times 10^{-5}$ using a 128-qubit circuit. We do not expect any significant challenges in further scaling this architecture to about one thousand qubits. Finally, we have briefly discussed both an XYZ-addressable and a QFP shift register based solution that would facilitate scaling up to read even larger numbers of qubits on a single chip.

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