Floating memristor and inverse memristor emulation configurations with electronic/ resistance controllability

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Abstract: This study presents two configurations to realise the behaviour of a floating memristor and an inverse memristor. The modified version of VDCC (voltage differencing current conveyor) termed as MVDCC (modified VDCC) is used to develop the presented emulators. The floating memristor emulator uses a single MVDCC and two grounded passive elements while the configuration of floating inverse memristor emulator is based on two MVDCCs, two grounded resistances and single grounded capacitance. The behaviour of both the circuits can be controlled through applied bias voltage as well as the employed grounded resistances. Both the presented circuits do not employ any external analogue multiplier circuit/IC, which can be considered as the most notable feature of these circuits. This study also describes the mathematical properties of memristor and inverse memristor taking both symmetrical and non-symmetrical models into account. PSPICE simulation tool is used to verify the working of realised emulation circuits using 0.18 μm CMOS process technology. The implementations of realised emulators, employing commercial ICs like AD844, CA3080 and LM13700, have also been presented and validated.

1 Introduction
Memristor was first proposed as a fundamental element by Chua in 1971 [1] which he defined to relate the quantities flux (Φ) and charge (q). Later, when its properties were explored, memristor was found to be the most virtuous element among all the fundamental elements. The reason was its applicability in the wide range of fields like advanced storage devices, neural networks, modelling of primitive cells, neuro-morphic computing etc. It is was found to be the most virtuous element among all the characteristics of memristor, effect of different operating conditions and the work presented in [4–6], different ways to calculate the area enclosed under the lobes and its physical significance is discussed. In [4] a generalised way of calculating the area for mem-elements is reported. In [5] also, it has been shown that the area under the lobes also represents the memory content present in memristor. It is also proved that only fundamental component present in memristor current decides the storage of memristor whereas higher-order components are only responsible for the shape of the VI curve. A new method for finding the area has been derived in [6], which is based on the static characteristics plotted between q and Φ. The study illustrated in [7] examines the necessary conditions for PHL of an ideal memristor. In [8], the modelling of memristor, based on a polynomial integrated Verilog-AMS (Verilog-AMS-POM) is proposed to enable fast circuit and accurate system-level design. Similarly, the study presented in [9] defines different aspects of memristor including basic characteristics, models, fabrications, and circuit designs to provide a complete picture of this concept. Using the various mathematical models developed for the current–voltage relationship of an ideal memristor, the several circuit emulators to realise the memristor behaviour based on modern active elements have been reported by researchers in the last decade. Some of the popular floating memristor emulators have been described in [10–22].
A floating memristor emulator is presented in [10], which is based on one CCTA (current controlled transconductance amplifier) and single CCI (second generation current conveyor). It employs two resistances (one floating and one grounded) along with single grounded capacitance. This circuit does not exhibit the feature of resistor/electronic tunability. In [11], a floating memristor configuration, employing an OA (operational amplifier) and four CCIIs, has been reported. Although the circuit uses single grounded capacitance, the employment of a large number of resistances (floating and grounded) does not make it an optimised configuration. The floating memristor realised in [12] uses a single DDCC (differential difference current conveyor) along with an analogue multiplier. The circuit also employs a resistance and capacitance both in a grounded and floating state. In [13], two different emulators for floating memristor have been presented based on four CCs and single AD633. These circuits realise both positive as well as negative memristance using single grounded capacitance and two resistances. The circuit reported in [14] emulates the behaviour of a floating memristor using single OTA (operational transconductance amplifier), but the configuration cannot be considered as a compact one, due to the use of three external CMOS transistors and two grounded capacitances along with two constant voltage sources. In [15], a floating circuit to emulate the memristive behaviour is presented which employs four CFOA (current feedback operational amplifiers) along with two diodes. This circuit also employs three floating resistances, one grounded resistance and four grounded capacitances. In [16], a multi-output OTA-based memristor emulator has been developed. Although it uses only single grounded capacitance, no facility of electronic tuning has been demonstrated in this work. A floating memristor emulator circuit is proposed in [17], which employs four

2 Related prior work
The impact of this discovery was witnessed, when numerous articles on the memristor properties were published in the succeeding years of 2008. These research papers investigated the properties like the area of the PHL (pinched hysteresis loop), static characteristics of memristor, effect of different operating conditions on the memristor behaviour etc. [3–9].

In [3], static characteristics of memristor using the graphical methods have been explored. The analysis is presented for different models of memristor (current-controlled and voltage-controlled). In the work presented in [4–6], different ways to calculate the area enclosed under the lobes and its physical significance is discussed. In [4] a generalised way of calculating the area for mem-elements is reported. In [5] also, it has been shown that the area under the lobes also represents the memory content present in memristor. It is also proved that only fundamental component present in memristor current decides the storage of memristor whereas higher-order components are only responsible for the shape of the VI curve. A new method for finding the area has been derived in [6], which is based on the static characteristics plotted between q and Φ. The study illustrated in [7] examines the necessary conditions for PHL of an ideal memristor. In [8], the modelling of memristor, based on...
CCIIIs with three OTAs. Along with the employment of seven active elements it also uses six resistances and one grounded capacitance. In [18] single VDTA (voltage differencing transconductance amplifier) based floating memristor emulator has been reported which employs single VDTA along with two grounded resistances, one grounded capacitance and one CMOS voltage multiplier circuit having 14 CMOS transistors. This VDTA based circuit is not very compact due to the use of an excessive number of passive elements and CMOS voltage multiplier. The circuit of floating memristor given in [19] is based on four CCIIIs and one AD633. Along with these active elements it also employs a grounded capacitance and five resistances including both floating and grounded ones. The use of a large number of active and passive elements make this realisation bulky in nature. The memristor emulator reported in [20] uses a CBTIA (current buffered transconductance amplifier) and two grounded capacitance. In [21], a floating memristor emulation circuit is reported, although it uses single CCTA but also employs three passive resistances along with a grounded capacitance. Furthermore, the floating memristor configuration developed in [22] employs two AD844 ICs and two AD633s. Along with the use of a large number of active elements the circuit also requires four grounded capacitances, two grounded resistances and five floating resistances. Therefore, this configuration is quite unsuitable in terms of compactness.

Therefore, it can be concluded from the discussion presented until now, that most of the floating memristor emulator circuits developed so far suffer from one or more unsuitable design features: (i) more than one ABBs (active building blocks) are employed; (ii) employment of more than one capacitances; (iii) floating passive element(s) are used; (iv) use of external voltage multiplier IC/circuit; (v) lack of memristor tuning through employed passive elements; (vi) non-availability of electronic tuning, i.e. memristive behaviour cannot be controlled through biasing voltage and/or current; and (vii) partial utilisation of employed ABB(s).

In addition to design aspects, the performance of circuits reported in [10–22] is also studied. On careful investigation of transient VI characteristics of the memristor emulator reported in [10], it can be observed that the presented emulation circuit exhibits poor frequency dependency, i.e. the lobe area shows a negligible change on increasing the frequency. Therefore, the signature property (the area covered by the lobes should decrease on increasing frequency) of an ideal memristor is not followed. And also from the pulse input response of memductance, it can be observed that the margin between different steps of staircase response subjected to pulse input is not a perfect staircase and having small step size. As compared to the emulators reported in [10–22], the proposed memristor configuration has the following advantageous features:

(i) Employment of single ABB.
(ii) Only two passive elements are employed.
(iii) All the employed passive elements are grounded.
(iv) No use of external voltage multiplier circuit/IC.
(v) Memristor behaviour tunability through employed passive elements and biasing currents.
(vi) No requirements for the matched value of passive elements.
(vii) Wide operating frequency range (order of MHz).
(viii) Lobes are perfectly symmetrical.
(ix) Satisfactory $G_{\text{H}}$ response for pulse excitation.
(x) Lobe area shows ideal frequency dependency as desired in case of memristor.

The use of single ABB, employment of only two grounded passive components and no use of voltage multiplier are the features which confirm the compactness of proposed memristor emulators. Avoiding large-sized electronic circuits and elements is always followed by IC designers and developers. As it increases the chip packaging density and reduces the development cost. Therefore, an emulator circuit of compact size is always a requirement for monolithic integration and also, it is compatible with current market trends.

The resistance/electronic tuning, of presented emulators, is also a very useful feature which offers several advantages like: (i) Without replacing the employed active and/or passive elements, the memductance value and its hysteresis behaviour can be varied. (ii) The tilt of the VI contour can be varied using the biasing voltage or external resistor. It is important because when the memristor is employed in implementing logic devices then this gradient of the HIL defines the resistance values corresponding to the digital logic levels. Now, due to this feature by altering these two resistance states we can control the margin of the memristive logic. (iii) If the memristor emulator is to be employed in the applications like filters, chaotic oscillators and modulators etc. the electronic controllability can be found very useful to control the operation of these applications without any hardware modification.

### 3 Concept of memristor and inverse memristor

Equation (1) defines the current–voltage relationship of memristor

$$i = aV + a \int_{t_0}^{t} v(t) \, dt.$$  

(1)

For sinusoidal input, $v(t) = V_m \sin \omega t$, the memristor current ‘i’ can be obtained as
The current \( i \) can be expressed as

\[
i = a \nu \sin \omega t + \frac{\nu c}{\omega} (1 - \cos \omega t) \sin \omega t.
\]  

(2)

The hysteresis curve of ideal memristor, defined by (2), has been plotted in Fig. 1.

Now, it is interesting to explore the mathematical properties of an unconventional memristor having crossover point shifted from the origin. Applying the simple mathematical concept in (2) it can be understood that the symmetrical nature of ideal memristor is due to the presence of term \((1 - \cos \omega t)\) in product with \(
\sin \omega t\) and pinch-off point exists at the origin. To shift this pinch-off point from the origin a term consisting \('\cos \omega t'\) without associating \('
\sin \omega t\) can be added to (2). This addition may result in non-zero values of pinch-off coordinates due to which non-symmetrical characteristics may be obtained. It may be noted that term \('\cos \omega t'\) in the memristive current equation may be obtained if a derivative term of input voltage \('v'\) is added to (1). It is only true for the sinusoidal excitation.

Therefore, on adding derivative of input sinusoidal voltage in (2), the current \(i(t)\) can be expressed as

\[
i = a \nu \sin \omega t + \frac{\nu c}{\omega} (1 - \cos \omega t) \sin \omega t + \frac{d\nu}{\omega} \cos \omega t.
\]  

(3)

The VI characteristics for (3) are plotted in Fig. 2 and the non-symmetrical nature of (3) can be verified. These plots are presented for different positive and negative values of coefficient \(d' \). It can also be observed that the shift in the pinch-off point position can be controlled by the coefficient \(d' \). Hence the current–voltage relationship given in (3) describes the behaviour of a non-symmetrical memristor having unequal lobe areas.

The coordinates of the shifted crossover point can be found by putting the coefficient of \('\cos \omega t'\) in (3) equals to zero. The voltage coordinate \( 'v_c' \) of the crossover point can be obtained as

\[
v_c = \frac{d\nu}{\omega}.
\]  

(4)

From (4) it can be noted that the peak amplitude of input sinusoidal signal does not affect the shift in crossover point, it only decides the span and shape of the lobes. Similarly, the current coordinate \('i_c'\) of the pinch-off point presented in the VI plane can also be found by putting those values of terms \('
\sin \omega t\) and \('\cos \omega t'\) in (2) at which the crossover occurs on the hysteresis curve. For sinusoidal input, this value equals to \('v_c'\) (defined in (4)).

From (4), it is also verified that the coefficient \('d' \) does not decide the position of the crossover point. The pinch-off point shift, towards the first quadrant or in the third quadrant, only depends upon the coefficient \('d_c' \) and \('d' \). Furthermore, the instance at which the crossover occurs can also be calculated by equating \('
\sin \omega t\) to \('v_c'\) defined in (4). The crossover is observed in second quarter-cycle of sinusoidal input, therefore cross-over instance \( 'i_c2' \) can be obtained as

\[
t_c2 = \frac{1}{\omega} \left( \pi - \sin^{-1} \left( \frac{d\nu}{\omega} \right) \right).
\]  

(5)

Interestingly, the co-sinusoidal term \('\cos \omega t'\) (a derivative of input voltage) can be found in the input current expression of a memristor, if a shunt parasitic capacitance is presented at the input terminals of memristor circuit. This capacitance can shift the cross-over point from origin to the first quadrant (in case of a positive capacitance). In the active element-based memristor emulator circuits, the parasitic capacitances of employed active elements may produce this effect. Therefore, in case of such memristors having non-symmetrical characteristics, the effect of parasitic capacitances can be nullified by selecting the coefficient value of the derivative term in such a way which can shift the cross-over point back to the origin.

The inverse memristor is a concept derived from the mathematical model of a conventional memristor. The inverse memristive behaviour can be obtained by replacing the integral term by a derivative term in the current–voltage expression of the ideal memristor.

Therefore, the current–voltage relation for an inverse memristor can be defined as

\[
i = b \nu \sin \omega t + b \frac{d\nu}{dt} \cos \omega t \sin \omega t.
\]  

(6)

On putting \('v = \sin \omega t'\), (6) becomes

\[
i = b \nu \sin \omega t + a d\nu \cos \omega t \sin \omega t.
\]  

(7)

The transient current–voltage characteristics for (7), is presented in Fig. 3. These VI curves are similar to the memristor characteristics illustrated in Fig. 1. However, in this case, the inverse behaviour is found to be exhibited for operating frequency variation. On increasing the operating frequency from zero onwards, generated PHL changes its shape from a line passing through the origin to a continuously expanding loop, which is pinched at the origin. In other words, the lobe area increases with an increase in operating frequency. Due to this contrasting behaviour, this element can be called as an inverse memristor. An inverse memristor has also been classified as non-ideal memristor [23].

Also, an inverse memristor, when connected in series or parallel with a memristor, can be useful in modifying the behaviour of lobe area variation for a frequency change. It can be used to alter the ever-decaying curve between area and frequency of memristor. In a more clear sense, we can amend the frequency range, after which the memristor becomes almost a linear resistor, by just tuning the coefficients of the connected inverse memristor. This solution not only preserves the hysteresis properties of memristor but also...
memristor can be defined as calculated as

\[ v = \omega b \sin \omega t \]  

Using (8) the 'v' coordinate of the shifted crossover can be calculated as

\[ v_c = \frac{b_1}{\omega b_1}. \]  

From (9), for a sinusoidal excitation, the time instance of crossover 't_c1' and 't_c2' can be computed as

\[ t_{c1} = \frac{1}{\omega} \sin^{-1} \left( \frac{b_1}{\omega b_1} \right) \]  

and

\[ t_{c2} = \frac{1}{\omega} \left( \pi - \sin^{-1} \left( \frac{b_1}{\omega b_1} \right) \right). \]

The area has been a key element to describe the memory properties of memristive elements. Many researchers have tried to interpret the storage capacity of memristor using area enclosed under the lobes and studied the effect of area on the static characteristics of the memristor. It has also been proved mathematically that non-linearity found in the charge-flux curve of memristors is due to only the enclosed area under IV lobes.

Here, the area for an inverse memristor is calculated to study the effect of an extra term (an integral term added to inverse memristive current), which shifts the cross-over point away from the origin. This area has been computed for that lobe whose span is getting increased due to the shifting of cross-over point on adding this extra term. It can also be seen here that at a critical value of the coefficient of integral term, the area becomes zero and lower lobe completely diminishes out resulting in maximum non-symmetry.

Now from the plot given in Fig. 4, it can be observed that analogues to the non-symmetrical behaviour of memristor, the shifting of pinch-off point for inverse memristor depends upon the coefficient \( b_1 \). The shifting of cross-over point results in a reduction of a lobe area giving rise to an increase in another lobe area at the same time. To investigate this effect, the area of the lobe present in the third quadrant has been calculated.

The area \( A_{LL} \) of the lower lobe, exists between pinch off instances \( t_{c02} \) and \( t_{c04} \) shown in Fig. 5 can be given as

\[ A_{LL} = \omega \int_{t_{c02}}^{t_{c04}} \left[ b_1 \sin \omega t + b_1 \cos \omega t \sin \omega t + \frac{b_1}{\omega} (1 - \cos \omega t) \right] \sin \omega t \cos \omega t \, dt. \]  

Now, the lower lobe present in the third quadrant is formed during the negative half cycle (and some period of second cycle) of the input voltage. Therefore the time instances \( t_{c02} \) and \( t_{c04} \) can be computed as

\[ t_{c02} = \frac{1}{\omega} \left( \pi - \sin^{-1} \left( \frac{b_1}{\omega b_1} \right) \right) \]  

and

\[ t_{c04} = \frac{1}{\omega} \left( 2 \pi + \sin^{-1} \left( \frac{b_1}{\omega b_1} \right) \right). \]

The instances given in (13) and (14) can be obtained with the help of 'v_0' given in (9).

On putting the values of time limits from (13) and (14) into (12), the area \( A_{LL} \) can be expressed as

\[ A_{LL} = \left[ -\frac{b_1}{2} \left( \pi \omega - (2/\omega) \sin^{-1} (b_1/\omega b_1) \right) + (3/2) b_1 \omega b_1 \sin^{-1} (b_1/\omega b_1) \right] - \left( b_1 \omega b_1 \sin^{-1} (b_1/\omega b_1) \right) - 2 \omega b_1 \sin^{-1} (b_1/\omega b_1) - 2 b_1 \omega b_1 \sin^{-1} (b_1/\omega b_1). \]

Now at 'v_0 = −1' (negative peak of input), the (9) can be written as

\[ \frac{b_1}{\omega b_1} = -1. \]
Now, on substituting \( i_0 / \omega^2 b_1 = -1 \) in (15), the area of the third quadrant lobe \( A_{LL} \) is found to be zero. Therefore, the critical value of \( i_0 \) at which the third quadrant lobe completely disappears can be given using (16) as

\[
  i_{\text{critical}} = -\omega^2 b_1. \tag{17}
\]

In Fig. 6, it can be seen that on the increase in the negative value of \( i_0 \), the area of the third quadrant lobe is getting reduced and it completely diminished at \( i_0 = -5 \).

4 Idea of voltage differencing current conveyor (VDCC)

VDCC was first put forward by Biolek et al., in their article published in 2008 [24]. VDCC has been employed as an active element in the various signal generation/processing circuits and systems like higher-order active filters, modern oscillators and passive elements simulators etc. [25–27].

5 MVDCC (modified VDCC)

The ideal VDCC, whose CMOS realisation is given in Fig. 7, is a six terminal circuit concept excluding the biasing terminals \( V_{B1} \) and \( V_{B2} \). Now, in this work, we have used the modified structure of VDCC by extracting a Z-terminal to obtain the differential voltages at \( X \). Due to this slight modification in the architecture, it has been termed as MVDCC. The CMOS realisation of this MVDCC is given in Fig. 8. The symbolic representation of MVDCC is same as the VDCC with extra Z-terminal as shown in Fig. 9. The current–voltage matrix of MVDCC is given in (18)

\[
\begin{bmatrix}
I_P \\
I_N \\
I_{Z+} \\
I_{Z-} \\
I_{VZ+} \\
I_{VZ-} \\
I_{VX} \\
I_{WX}
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
g_m & -g_m & 0 & 0 & 0 & V_P \\
g_m & -g_m & 0 & 0 & 0 & V_N \\
0 & 0 & 1 & -1 & 0 & V_{Z+} \\
0 & 0 & 0 & 0 & 1 & V_{Z-} \\
0 & 0 & 0 & 0 & -1 & V_X
\end{bmatrix}

\begin{bmatrix}
V_P \\
V_N \\
V_{Z+} \\
V_{Z-} \\
V_{X}
\end{bmatrix}
\tag{18}
\]

where \( g_m \) is the input stage transconductance of MVDCC, which can be controlled by biasing voltage \( V_{B1} \) according to the relation given in (19)

\[
g_m = k(V_{B1} - V_{th} - V_{SS}). \tag{19}
\]

6 Proposed MVDCC-based floating memristor emulator

The proposed MVDCC-based floating memristor emulator employing single MVDCC block with two grounded passive elements (one capacitance and a resistance) has been shown in Fig. 10.

Now for the circuit given in Fig. 10, the current ‘\( I_2 \)’ is related to the differential input ‘(\( V_1 - V_2 \))’ as follows:

\[
I_2 = g_m(V_1 - V_2). \tag{20}
\]

As the voltages ‘\( V_1 \)’ and ‘\( V_2 \)’ are shorted to ‘\( Z^- \)’ and ‘\( Z^+ \)’ terminals, respectively. The ‘\( V_1 \)’ and ‘\( V_2 \)’ can be defined as

\[
V_1 = V_{Z-} \tag{21}
\]

and

\[
V_2 = V_{Z+}. \tag{22}
\]
Similarly, memristor emulator

Using the terminal relationship for MVDCC and (21) and (22), the current $I_x$ can be expressed as

$$ I_x = \frac{1}{R}(V_{Z_x} - V_{Z_-}) = \frac{1}{R}(V_1 - V_2). $$

Now, the voltage $V_C$ across the capacitor $C_1$ connected at the $W_P$ terminal can be given as

$$ V_{x_+} = V_C = \frac{1}{C_1} \int I_x dt = \frac{1}{R C_1} \int (V_1 - V_2) dt. $$

It can be seen that this voltage $V_C$ is used for biasing purpose, therefore $g_m$ from (19) can be modified as

$$ g_m = k \left( \frac{1}{R C_1} \int (V_2 - V_1) dt \right) - V_{th} - V_{SS} $$

where $k$ is the process parameter defined in (19). Therefore, current $I_2$ from (20) can be calculated as

$$ I_2 = k \left( \frac{1}{R C_1} \int (V_2 - V_1) dt \right) (V_1 - V_2). $$

Similarly, $I_1$ can be defined as

$$ I_1 = g_m (V_1 - V_2). $$

From (27), the $I_1$ can be related as

$$ I_1 = k \left( \frac{1}{R C_1} \int (V_2 - V_1) dt \right) (V_1 - V_2). $$

From (26) and (28) the admittance matrix can be evaluated as

$$ \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} \frac{1}{R C_1} \int (V_2 - V_1) dt - V_{th} - V_{SS} \\ \frac{1}{R C_1} \int (V_2 - V_1) dt \end{bmatrix} \begin{bmatrix} 1 \\ -1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}. $$

From (29), it can be observed that the circuit presented in Fig. 10 realises the behaviour of a floating memristor with memductance $G_M$ as

$$ G_M = k \left( \frac{1}{R C_1} \int (V_2 - V_1) dt + (V_{SS} - V_{th}) \right). $$

It is clear from (30) that the constant conductive part ($G_{M\text{Fixed}}$) and flux dependent part ($G_{M\text{Variable}}$) can be evaluated by comparing (30) with standard memristance equation as follows:

$$ G_{M\text{Fixed}} = k (-V_{SS} - V_{th}) $$

and

$$ G_{M\text{Variable}} = k \left( \frac{1}{R C_1} \int (V_2 - V_1) dt \right). $$

From (31) and (32) it can be observed that both the fixed as well as the variable part of memductance $G_{M\text{Fixed}}$ and $G_{M\text{Variable}}$ are positive which indicates the realisation of decremental memristor.

It is interesting to note that to achieve the multiplication of analogue voltages in memristor current $(32)$ with sin $\omega t$, the designed circuit does not use any external analogue multiplier which is the major advantage of the proposed memristor emulator.

7 Proposed MVDCC-based floating inverse memristor emulator

The circuit, shown in Fig. 11, illustrates the configuration of floating inverse memristor emulator employing two MVDCCs, two grounded resistances and single grounded capacitance.

On circuitual analysis of configuration shown in Fig. 11 the admittance matrix can be found as

$$ \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} k C_2 - R_1 \frac{d}{dt} (V_2 - V_1) + k (-V_{SS} - V_{th}) \end{bmatrix} \begin{bmatrix} 1 \\ -1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}. $$

It can be deduced from (33) that the proposed circuit emulates the behaviour of a floating inverse memristor with realised inverse memductance value, $G_{M\text{Inverse}}$

$$ G_{M\text{Inverse}} = k (-V_{SS} - V_{th}) + k C_2 \frac{R_1}{g_{m2} R_4} \frac{d}{dt} (V_2 - V_1). $$

The value of emulated inverse memductance $G_{M\text{Inverse}}$ depends upon the transconductances $g_{m2}$ and grounded resistances. Which opens the door for tuning of $G_{M\text{Inverse}}$, through the biasing voltages and passive elements employed, along with MVDCCs. The time-independent and time-varying parts in (34), are presented in (35) and (36), respectively

$$ G_{M\text{Fixed}} = k (-V_{SS} - V_{th}) $$

and

$$ G_{M\text{Variable}} = k C_2 \frac{R_1}{g_{m2} R_4} \frac{d}{dt} (V_2 - V_1). $$

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Frequency-dependent behaviour of memristor and inverse memristor

From the memductance expression of presented floating memristor emulator given in (30), it can be deduced that it realises the behaviour of a lossy non-linear inductor which can be viewed as a parallel combination of time-dependent equivalent inductor $L_{\text{time-dependent}}$ and an equivalent resistance $R_{\text{eq}}$. In the $G_M$ expression given in (30), the time-varying part is corresponding to $L_{\text{time-dependent}}$, whose value depends upon the input voltage, having a unit of Henry–Volt and $R_{\text{eq}}$ is represented by the fixed part.

For a sinusoidal input, $V_m\sin(\omega t)$, the minimum value of the inductance $L_{\text{time-dependent}}$ (Henry–Volts) can be calculated as

$$L_{\text{time-dependent}} = \left(\frac{RC}{kV_m}\right).$$

(37)

Similarly, the $R_{\text{eq}}$ can be evaluated as

$$R_{\text{eq}} = \frac{1}{k}(-V_{SS} - V_m).$$

(38)

Now from (37) and (38), the time constant of parallel $L_{\text{time-dependent}} - R_{\text{eq}}$ circuit can be obtained as

$$\tau = \frac{L_{\text{time-dependent}}}{R_{\text{eq}}}.$$ 

(39)

From (39), $\tau$ is obtained as

$$\tau = \frac{RC(-V_{SS} - V_m)}{V_m}.$$ 

(40)

Similarly, for the case of an inverse memristor, the inverse memductance expression given in (34) will be representing a parallel RC circuit consisting, a non-linear capacitance $C_{\text{time-dependent}}$ and an equivalent resistance $R_{\text{eq}}$. From (34), for a sinusoidal input maximum value of $C_{\text{time-dependent}}$ (Farad/volts) and $R_{\text{eq}}$ can be found as

$$C_{\text{time-dependent}} = \left(V_m k \frac{R_1}{R_{\text{Stat}}}ight).$$

(41)

and

$$R_{\text{eq}} = \frac{1}{k}(-V_{SS} - V_m).$$

(42)

And the corresponding $'\tau'$ can be evaluated as

$$\tau = \frac{C_{\text{time-dependent}} R_{\text{eq}}}{R_{\text{Stat}} (-V_{SS} - V_m)}.$$ 

(43)

The critical frequency corresponding to (40) and (43) can be used to define the frequency dependence behaviour of proposed floating memristor and inverse memristor emulator circuits for different ranges of variable $\tau$.

9 Implementation of the presented MVDCC-based memristor and inverse memristor emulators using commercial ICs

There is no commercial IC available, which can implement the function of MVDCC directly. Therefore, to implement the floating memristor emulator shown in Fig. 10 the circuit is converted to the grounded configuration by connecting negative input terminal to the ground. In that case, the employed MVDCC becomes same as VDCC which can be implemented by using commercially available ICs, CA3080 and AD844. The IC-based realisation of memristor emulator shown in Fig. 10 has been depicted in Fig. 12. The circuit employs two CA3080 ICs, single AD844 IC, two grounded resistances and one grounded capacitance.

The implementation presented in Fig. 12, depicts the commercial IC-based realisation of MVDCC-based floating memristor using CA3080 and AD844. Similarly, the inverse memristor emulator presented in Fig. 11 is implemented by using IC AD844 and LM13700 and the circuit is shown in Fig. 13.

10 Application example of proposed floating memristor emulator

To demonstrate the usability of proposed memristor emulator, a memristor–capacitor (MC) low-pass filter (LPF) has been developed and shown in Fig. 14.

The expression for cut-off frequency ($f_c$) and gain $G$ (dB) for the filter of Fig. 14 can be evaluated as
\[ f_c = \frac{G_M}{2\pi C_1} \]  \hspace{1cm} (44)

where

\[ G(M) \approx \frac{10\log\left(\frac{G_M}{\omega C_1}\right)}{\Delta G} \]  \hspace{1cm} (45)

where \( G_M \) is the memductance which can be defined as

\[ G_M = G_{\text{Mean}} \pm \Delta G \]  \hspace{1cm} (46)

where

\[ G_{\text{Mean}} = k(-V_{\text{SS}} - V_{\text{i0}}) \]  \hspace{1cm} (47)

and

\[ \Delta G = \frac{1}{V_{\text{i0}}^2} \frac{1}{R C_1} \cos(\omega t + \phi). \]  \hspace{1cm} (48)

### 11 Simulation results

For the validation of reported floating memristor emulator and inverse memristor emulators, the PSPICE simulation environment with 0.18 \( \mu \)m CMOS technology has been chosen. The CMOS implemented MVDCC shown in Fig. 8 was used with power supply voltages \( V_{\text{PD}} = \pm 0.9 \) V. The \( W/L \) ratios of the employed CMOS transistors in MVDCC implementation are given in Table 1.

![Fig. 15 VI loop generated for MVDCC-based memristor shown in Fig. 10 at various frequencies](image)

![Fig. 16 Behaviour of presented floating memristor emulator for different values of capacitance \( C_1 \)](image)

Table 1 \( W/L \) ratios of CMOS transistors used in Fig. 8

| Transistors | \( W/L \) ratio, \( \mu \)m |
|------------|--------------------------|
| M1–M4      | 3.6/1.8                  |
| M5 and M6  | 7.2/1.8                  |
| M7 and M8  | 2.4/1.8                  |
| M9 and M10, M23 and M24 | 3.06/0.72 |
| M11 and M12 | 9.0/7.2                 |
| M13–M17    | 14.0/0.72                |
| M18–M22    | 0.72/0.72                |
| M25        | 3.6/1.8                  |
| M26        | 3.06/0.72                |

Now to verify the working of the presented floating memristor, the emulator circuit given in Fig. 10 has been simulated for three different operating frequencies of values \( F_{\text{in}} = 500 \) kHz, 1 and 1.5 MHz, respectively. The peak value of the input sinusoidal voltage was taken as \( V_p = 0.1 \) V with passive elements values \( R_1 = 1.45 \) K and \( C_1 = 0.05 \) nF. The generated simulation plots of the transient VI characteristics at different operating frequencies have been given in Fig. 15. The results were obtained at biasing voltage \( V_{\text{BS2}} = 0.8 \) V. From the Lissajous plots presented in Fig. 15, it can be noticed that for \( F_{\text{in}} = 500 \) kHz, the span of lobes is maximum and for \( F_{\text{in}} = 1000 \) kHz, both the lobes present in opposite quadrants cover a smaller area. Furthermore, when the frequency is raised up to 1500 kHz, the lobe area is found to be minimum with more symmetry. Therefore, it can be confirmed from Fig. 15 that on increasing operating frequency giving rise to a reduction in the PHL lobe area, which is a key feature of an ideal memristor. Later the simulation results have been presented to illustrate the effects of different memristor parameters and operating conditions on the transient VI plot of memristor and for this purpose the operating frequency was selected as \( F_{\text{in}} = 1 \) MHz, input voltage as \( V_{\text{p}} = 0.1 \) V and biasing voltage was taken as \( V_{\text{BS2}} = 0.8 \) V.

Firstly, the effect of capacitance value on floating memristor behaviour has been investigated. The plot, given in Fig. 16 shows the VI plots for different values of employed grounded capacitance. It can be noticed from Fig. 16, that the effect of capacitance value variation on PHL is the same as the operating frequency variation, i.e. on increasing the value of grounded capacitance the area covered by the lobes is getting reduced. This may be due to the fact, that the capacitance \( C_1 \) is presented in the memductance expression in product with the frequency \( \omega \). Similarly, the influence of grounded resistance \( R_1 \) has been studied and the corresponding simulation results are provided in Fig. 17, which proves its resistance tunable behaviour. From the plots given in Fig. 17, it can be observed that for \( R_1 = 1.26 \) K, the span of lobe area is larger as compared to the plot corresponding to \( R_1 = 2.94 \) K and the area becomes very small when \( R_1 \) is increased to 8.82 K. Therefore, \( R_1 \) can be effectively used to change the hysteresis behaviour of memristor. The behaviour of the developed floating memristor can also be controlled using biasing voltage \( V_{\text{BS2}} \). This has been shown in the transient VI characteristics presented in Fig. 18 which indicates the electronically tunable nature of emulator circuit. It is clear from the plots shown in Fig. 18, that on increasing \( V_{\text{BS2}} \), area of VI curves is also expanding. The
incline of PHL curve to the input voltage axis, also increases with an increase in bias voltage $V_{BS2}$. Which shows the electronically tunable nature of presented floating memristor emulator.

As it is well known, that memductance of any memristor is a function of applied excitation voltage i.e. the shape of PHL must vary for different input voltages. Therefore, to study this effect, the simulations have been performed for different values of input excitation voltage and plots are presented in Fig. 19.

The response of generated memristor current for a sinusoidal excitation is also illustrated. For this purpose, the simulations have been executed at 1 MHz operating frequency and simulation generated plots are shown in Fig. 20. On careful investigation of the transient VI plots (shown in Fig. 20), it can be seen that due to no phase lagging or leading present in the memristor current, the proposed memristor is purely resistive in nature.

In network applications, it is always practised to use elements in parallel or series combinations depending upon the requirements. The simulation results in Fig. 21 shows the PHLs obtained for series and parallel connections of two similar memristor emulators. It can be observed that for sinusoidal excitation, the parallel combination generates a PHL having a high value of slope (double of that of single memristor) which is due to the fact that parallel combination results into the higher value of current for same excitation input. Similarly, for series combination, the value of resistance becomes twice, therefore, reduces the current to half of that of single memristor and the slope gets halved.

Now the plot, shown in Fig. 22, demonstrates the response of memristance of realised floating memristor with time. The presented memristance versus time curve has been generated for 500 kHz operating frequency. In a cycle of input sinusoidal voltage, the variation of memristance can be understood by the transient hysteresis curve of memristor. It can be observed that except at the point where a half-cycle gets covered, the variation of memristance is quite smooth and the value of the resistance is always positive. The spiking behaviour of the response at the middle of the input voltage cycle is due to the reason that at this instance the hysteresis curve crosses the origin (at which the instantaneous memristance is undefined). Moreover, the non-volatility property of the floating memristor emulator presented in Fig. 10 is investigated.

To verify this property, the emulator circuit has been excited by a pulse voltage having a period of $T_p = 1$ ns and amplitude of $V_{in} = 10$ mv. The values of passive elements were taken as $C_1 = 0.1$ nF, $R_1 = 1.45$ K and the biasing voltage was kept $V_{BS2} = 0.4$ V. When a pulse input is applied to a voltage-dependent memristor (here, we have taken the incremental memristor), its memductance must decrease (increase in the memristance) for repetitive application of pulse excitation. It has also been verified in the current response plotted in Fig. 23.

Using this current plot the behaviour of the $G_M(S)$ for pulse voltage input can also be investigated as shown in Fig. 23. In the absence of the i/p pulse voltage, the memductance $G_M(S)$ remains constant and holds the previously attained value of conductance, therefore, confirms the non-volatility property of memristor.

Now the simulation results for the MVDCCL-based inverse memristor emulator are presented. The emulator circuit, given in Fig. 11, has been simulated for biasing voltage $V_{BS2} = V_{BS} = 0.4$ V. Where $V_{BS2}$ is the biasing voltage of the second stage of MVDCCL and $V_{BS}$ is the biasing voltage of both the input as well as the output stage of MVDCCL. The values of passive elements, grounded resistances and capacitance were chosen as $R_2 = 1.45$ K, $R_4 = 0.4$ K and $C_2 = 0.1$ nF. First of all, the frequency dependency of the inverse memristor behaviour is investigated for peak input voltage $V_p = 0.1$ V. The simulation generated plots depicted in Fig. 24 illustrate the effect of frequency variation on PHL. As discussed in the theory part, the area of IV loop of inverse memristor must expand on increasing operating signal frequency. The same behaviour can be observed in the plots shown in Fig. 24 it is demonstrated that at $F_{in} = 20$ kHz the area is smaller and it slightly expands when the frequency is increased up to 25 kHz and it further increases when $F_{in}$ becomes 30 kHz. Furthermore, the influence of passive elements $R_2$ and $R_4$ is studied and the simulations results are illustrated in Figs. 25 and 26. For this purpose, the applied signal frequency was chosen as $F_{in} = 30$ K. On careful investigation of the simulation results presented in Figs. 25 and 26, it can be stated clearly that both $C_2$ and $R_4$ has the same effect over PHL as it has been witnessed for operating frequency, i.e. expansion of lobes on increasing the parameter value. These plots verify the tunable behaviour of proposed inverse memristor emulator through passive elements.

The behaviour of the floating inverse memristor can also be controlled using biasing voltage $V_{BS}$. It is demonstrated through hysteresis curves presented in Fig. 27 for different values of bias voltages. It can be seen here that in increase in the value of biasing voltage $V_{BS2}$, the area of generated VI lobes increases. The plot corresponding to $V_{BS2} = 0.42$ V has a larger area as compared to

**Fig. 18** Electronically controllable behaviour of VDCC-based memristor on varying biasing voltage $V_{BS2}$ keeping $F_{in} = 1$ MHz

**Fig. 19** VI curves of floating memristor for different peak values of applied sinusoidal input at $F_{in} = 500$ kHz

**Fig. 20** Transient response of input voltage and current at $F_{in} = 1$ MHz

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the VI curve obtained for $V_{BS2} = 0.4\, \text{V}$. From (34), it can be understood that inverse memductance depends upon the applied excitation voltage. Therefore, PHL of inverse memristor must vary for different operating voltages. To study this effect simulation has been performed for different peak values of applied sinusoidal voltage and the results are presented in Fig. 28. The plots, given in Fig. 28 also depict that when the peak value of input voltage $V_p$ increases, the slope of the PHL also become large. Among the three plots presented, the slope has a minimum value for $V_p = 0.075\, \text{V}$, becomes larger for $V_p = 0.1\, \text{V}$ and increases further for $V_p = 0.125\, \text{V}$.

The presented memristor emulator-based LPF shown in Fig. 14 has also been simulated for different values of capacitance $C_2$. The SPICE produced frequency response curves for $C_2 = 6.0, 10.0$ and $14.0\, \text{nF}$ are shown in Fig. 29 where $C_1 = 10\, \text{nF}$ and $R_1 = 1.45\, \text{k}$.

The commercial ICs AD844 and CA3080-based circuits of memristor emulator shown in Fig. 12 has been also validated. The first CA3080 (which is a current-controlled transconductance amplifier) presented in the input stage acts as the input transconductance stage of MVDCC while the AD844 realises the succeeding CFOA stage of the MVDCC. In the presented MVDCC-based circuit of Fig. 10, the capacitor is used to bias the first stage to get the voltage multiplication effect which is required to realise the current–voltage expression of memristor. However, in the ICs-based circuit shown in Fig. 12, the CA3080 has been used, which is a current-controlled IC and its output current cannot be the product of two voltages. Therefore one another CA3080 IC has been used, which converts the voltage into a proportional current for biasing the input stage IC CA3080. In this way, the circuit shown in Fig. 12 is equivalent to the presented VDCC-based memristor emulator.

The passive elements values are taken as $R_1 = 10\, \text{K}, R_2 = 0.33\, \text{K}$, and $C_2 = 10\, \text{nF}$. The biasing current of CA3080 was taken as $I_B$. 
and power supply voltage was kept at ±10 V DC. The transient VI characteristics, of emulation circuit shown in Fig. 12 for different input frequencies (1, 4 and 8 kHz) and peak input voltage of $V_P = 0.5$ V, have been plotted and shown in Fig. 30. It can be noted from Fig. 29 that for 1 kHz operating frequency, the area enclosed under PHL is maximum while for 8 kHz frequency the area is found minimum. In all the characteristics plots, both the first quadrant as well as the third quadrant lobes have excellent symmetry. Such behaviour confirms good memristive behaviour.

To show the effect of resistance $R_2$ the transient VI characteristics have been plotted for different values of $R_2$ (at 8 kHz operating frequency) as shown in Fig. 31.

Similarly, the behaviour of ICs AD844 and LM13700-based inverse memristor emulator shown in Fig. 13 is also investigated. Here the LM13700, which voltage-controlled transconductance amplifier, is used as the input stage of MVDCC and the voltage developed across the inductor is used to bias this IC. Due to which, the differential term in multiplication with input voltage can be obtained. And consequently, the behaviour of inverse memristor can be attained. To validate the behaviour of this circuit the transient VI characteristics for three different frequencies 5, 8 and 10 kHz have been generated. For this purpose, the power supply voltage was chosen as ±12 V DC and the passive element values were selected as; $R_1 = 0.5$ K, $R_2 = 112$ K and $L_1 = 0.1$ H. The biasing voltage of IC LM13700 is selected as $V_B = 30$ V. Fig. 32 shows the corresponding characteristics plots for peak-to-peak input voltage of $V_P = 5$ V. It is interesting to note from Fig. 32 that on increasing the operating frequency the lobe area is getting increased. Which is the just inverse behaviour of a memristor.

### 12 Conclusion

In this paper, emulator circuits for floating memristor and inverse memristor have been presented. MVDCC which is the modified version of conventional VDCC has been used as an active element.
to design the emulation configurations. Firstly, the floating memristor emulator is presented which employ single MVDCC and two grounded passive elements. The realised memductance value can be tuned through both the resistance as well as the biasing voltages. The proposed memristor emulator exhibit excellent frequency dependence behaviour having an large operating frequency range up to several MHzs with perfect symmetry found in the lobes. And also, the staircase response of memristor for pulse excitation proves its non-volatile nature with a high step margin of 1–2 µS (M-Ω). Further, in series/parallel combinations of proposed memristor emulator, the hysteresis behaviour is still existing and follow the characteristics of the employed connection. The second presented configuration is floating inverse memristor emulator, which is based on two MVDCCs, one grounded capacitance and two grounded resistances. Like the proposed memristor emulator, the behaviour of the realised inverse memristor emulator can also be controlled using employed resistance and/or biasing voltages. No employment of any external analogue multiplier circuit/IC is the main advantageous feature of designed emulators. Apart from the mathematical properties for both symmetric and non-symmetric behaviour in the VI plane have been discussed. Furthermore, all the MVDCC-based configurations are verified by performing simulation using PSPIICE for different operating parameters. The emulation circuits have also been implemented using commercial ICs like AD844, CA3080 and LM13700 and corresponding results are presented.

13 References

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